# Comparative Study of FinFET and FDSOI Nanometric Technologies Based on Manufacturing Defect Testability

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# Comparative Study of FinFET and FDSOI Nanometric Technologies Based on Manufacturing Defect Testability


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# *COMPARATIVE STUDY OF FINFET AND FDSOI NANOMETRIC TECHNOLGIES BASED ON MANUFACTURING DEFECT TESTABILITY*

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*Dedicated to my Beloved Parents*

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# RESUME

Avec l'évolution des technologies et notamment la réduction des dimensions, on atteint aujourd'hui les limites de la technologie CMOS planaire traditionnelle dite « Bulk ». En effet à l'échelle nanométrique, on observe une augmentation des effets de canaux courts ainsi qu'une plus grande dispersion des paramètres de fabrication. À 28nm et en dessous, le transistor planaire traditionnel ne permet plus d'offrir un accroissement conséquent des performances des circuits tout en assurant une faible consommation d'énergie. Par ailleurs, on observe aussi une augmentation de la sensibilité aux défauts de fabrication. En effet, la fabrication de structures beaucoup plus petites que la longueur d'onde de la lumière utilisée dans la lithographie moderne, se révèle problématique. De même, dans la gamme nanométrique il est difficile de contrôler la concentration de dopage pour les transistors. En outre, à chaque saut de nœud technologique les structures sont situées plus près les unes des autres, et même la plus petite des impuretés ou des particules métalliques sont susceptibles de créer des courts-circuits ou d'autres défauts. Finalement, l'accroissement du nombre de transistors, lignes de connexion, contacts et vias au sein d'une puce favorise aussi l'apparition de défauts. Ces limitations ont ainsi entraîné une augmentation de la densité des défauts dans les nœuds technologiques avancés, entraînant des difficultés à développer des dispositifs semi-conducteurs fiables.

Deux innovations en matière de procédés technologiques des semi-conducteurs sont apparues récemment comme des alternatives possibles à la technologie CMOS planaire traditionnelle : la technologie FDSOI pour « Fully Depleted Silicon On Insulator » et la technologie FinFET pour « Fin Field Effect Transistor ». Ces deux technologies présentent des propriétés prometteuses pour poursuivre la réduction des dimensions, grâce à un meilleur contrôle électrostatique de la grille sur le canal du transistor pour la technologie FinFET et une diminution des pertes dans le substrat pour la technologie FDSOI. La technologie FDSOI est, comme l'historique procédé de fabrication « Bulk », une technologie MOS planaire, ce qui la place naturellement davantage dans la continuité technologique que la technologie FinFET, qui repose elle sur l'intégration de transistors verticaux. La compétition entre ces deux technologies est rude et de nombreuses études publiées dans la littérature comparent ces deux approches en termes de performance en vitesse de fonctionnement, de consommation, de coût, etc.

Néanmoins, aucune étude ne s'était encore penchée sur leurs propriétés respectives en termes de testabilité ; pourtant l'impact de défauts sur les circuits réalisés en technologies FDSOI et FinFET est susceptible d'être différent de celui induit par des défauts similaires sur des circuits planaires MOS.

Dans ce contexte, l'objectif de cette thèse est de réaliser une analyse comparative de ces différentes technologies en étudiant leurs propriétés de testabilité vis-à-vis des défauts de fabrication les plus courants, à savoir les défauts résistifs de court-circuit et circuit ouvert. L'idée est d'explorer le comportement électrique de portes logiques mises en œuvre dans ces technologies en présence de tels défauts. Un seul défaut sera introduit au même endroit dans toutes les implémentations. Cependant pour la technologie FinFET, parce que nous avons seulement accès à un modèle "académique", la validité des résultats de la simulation reste théorique, notamment en ce qui concerne le comportement dynamique. Nous avons donc limité nos investigations principalement à l'analyse des défauts de court-circuit résistif dans le cadre d'un test statique. A l'inverse, pour les technologies Bulk et FDSOI, nous disposons de modèles industriels complètement validés par des mesures de silicium. Nous pouvons donc être confiants sur la validité des résultats de simulation, à la fois en ce qui concerne les comportements statiques et dynamiques. En conséquence, une analyse plus approfondie est effectuée pour ces technologies, avec des résultats détaillés à la fois dans le cadre d'un test logique ou d'un test en délai, en ciblant soit des défauts de court-circuit résistif ou de circuit ouvert résistif. Les conditions de fonctionnement les plus appropriées en termes de tension d'alimentation, température et tension de polarisation du substrat pour obtenir une couverture maximale des défauts sont analysées. De plus, l'impact de la variabilité du procédé de fabrication sur la détection des défauts est également étudié. Les principales contributions de la thèse sont divisées en six chapitres distincts, qui sont brièvement résumés ci-dessous.

Dans le premier chapitre, une description détaillée des transistors en technologies FDSOI et FinFET est tout d'abord présentée en soulignant les principales différences par rapport à la technologie CMOS traditionnelle. Les deux versions de transistors disponibles en technologie FDSOI, à savoir RVT pour « Regular-$V_T$ » et LVT pour « Low-$V_T$ », sont également détaillées ainsi que la possibilité d'utiliser la polarisation du substrat sous le canal. Les défauts de fabrication classiques en technologies CMOS traditionnelle sont ensuite introduits, ainsi que les nouveaux défauts spécifiques aux nouvelles technologies FDSOI et FinFET. Finalement, une

analyse de l'état de l'art des techniques de test les plus courantes pour la détection de défauts de court-circuit résistif et circuit ouvert résistif est présentée.

Le second chapitre est consacré à l'étude comparative des technologies Bulk, FDSOI et FinFET en présence d'un défaut de court-circuit résistif. L'approche adoptée consiste à insérer le défaut au sein d'un circuit de référence et d'étudier le comportement électrique dudit circuit à l'aide de simulations Synopsys HSPICE, et ce, pour différentes valeurs de la résistance de court-circuit. Le circuit de référence considéré est un bloc logique combinatoire didactique constitué de deux chaînes d'inverseurs et le défaut étudié est un court-circuit résistif inséré entre ces deux chaînes. Pour les technologies Bulk et FinFET, nous avons utilisé l'inverseur élémentaire standard de la bibliothèque industrielle pour implémenter le circuit de référence. Par contre pour la technologie FinFET, nous ne disposons pas d'une bibliothèque de portes élémentaires. Pour cela, un soin tout particulier a donc été apporté pour réaliser le dimensionnement d'un inverseur élémentaire dans cette technologie afin que l'étude comparative soit significative. Le circuit de référence affecté du même défaut a alors été implémenté dans les différentes technologies et des simulations électriques réalisées afin de déterminer la gamme de détectabilité du défaut dans chaque technologie. Pour cela, nous avons utilisé le concept de « résistance critique », qui définit la valeur maximale de la résistance du défaut de court-circuit engendrant un comportement logique erroné. Les résultats montrent que l'on obtient une gamme de détection similaire pour les circuits implémentés en Bulk, FDSOI-LVT et FinFET, et une gamme de détection plus large pour le circuit implémenté en FDSOI-RVT, gamme qui peut encore être étendue en utilisant une polarisation inverse du substrat. Finalement, une étude du comportement dynamique est réalisée afin d'avoir une première idée de l'amélioration apportée par un test basé sur le retard par rapport à un test statique classique pour les trois technologies.

Dans le troisième chapitre, nous approfondissons l'étude de la détection des défauts de court-circuit résistif en technologie FDSOI 28nm dans le contexte d'un test statique. Trois types de court-circuit sont considérés, à savoir, le court-circuit vers la tension d'alimentation, le court-circuit vers la masse et le court-circuit entre portes logiques. Un modèle analytique simple est tout d'abord proposé. Celui-ci permet le calcul de la résistance critique dans diverses conditions de fonctionnement. Ce modèle est basé sur une pré-caractérisation des portes élémentaires de la bibliothèque en terme de résistance de conduction des réseaux de transistors N et P. L'intérêt majeur de ce

modèle est qu'il permet d'évaluer la gamme de détectabilité des défauts ainsi que les conditions de fonctionnement les plus favorables à leurs détections sans effectuer une simulation de défauts. Une analyse détaillée de l'impact de la tension d'alimentation, de la polarisation du substrat et de la température est ensuite réalisée et les améliorations individuelles et combinées apportées par ces différentes conditions de fonctionnement sont quantifiées. Les résultats montrent que les conditions optimales de détection sont une faible tension d'alimentation, une polarisation inverse du substrat et une basse température pour une implantation de type RVT, quel que soit le type de défaut de court-circuit. Dans le cas d'une implantation de type LVT, la détection des défauts de court-circuit vers la masse et de court-circuit entre portes est également optimisée par ces mêmes conditions, alors que la détection des défauts de court-circuit vers la tension d'alimentation est favorisée par une température élevée. Plus généralement, les résultats mettent en évidence que la tension d'alimentation et la polarisation du substrat sont des paramètres prépondérants par rapport à la température, et ce, quel que soit le type de défaut. Un élargissement significatif de la plage de détection peut être réalisé en utilisant uniquement ces paramètres électriques, ce qui est un point important lorsque le coût du test est pris en compte. Finalement, une exploration plus approfondie de l'utilisation de la polarisation du substrat est également réalisée pour les deux types d'implantation RVT et LVT, notamment en envisageant une polarisation indépendante des puits des transistors N et P. Les résultats montrent qu'il n'y a pas d'intérêt à utiliser une telle polarisation indépendante.

Le quatrième chapitre est consacré à l'étude de la détection des défauts résistifs dans le contexte d'un test en délai. Pour cela, nous utilisons le concept de résistance critique dynamique qui est basé sur la différence des retards observés pour le circuit sain entre des simulations réalisées selon les conditions « *Typical* » et « *Slow* » du procédé de fabrication. L'étude est, là aussi, réalisée pour la technologie FDSOI 28nm en implantations de type RVT et LVT, mais les défauts de circuit ouvert résistif sont également pris en compte en plus des défauts de court-circuit résistif. L'influence de la tension d'alimentation et de la tension de polarisation du substrat est également évaluée. Les résultats montrent qu'une tension d'alimentation élevée et une polarisation directe du substrat améliorent la détection des défauts de circuit ouvert résistif alors qu'une tension d'alimentation faible et une polarisation inverse du substrat améliorent la détection des défauts de court-circuit résistif. Par ailleurs, la gamme de détectabilité des défauts de court-circuit est significativement élargie dans le contexte d'un test en délai

par rapport à un test statique. Finalement, on observe qu'une implantation de type LVT est plus favorable à la détection des défauts de circuit ouvert alors qu'une implantation de type RVT est plus favorable à la détection des défauts de court-circuit, avec une meilleure détectabilité pour les défauts de court-circuit vers la masse plutôt que de court-circuit vers la tension d'alimentation.

Dans le cinquième chapitre, nous nous intéressons à l'impact de la variabilité des paramètres du procédé de fabrication sur la détection des défauts de court-circuit résistif. En particulier, une étude comparative des technologies Bulk et FDSOI 28nm est réalisée pour des défauts de court-circuit vers la masse et de court-circuit vers l'alimentation. La notion de résistance critique est étendue dans ce chapitre pour assurer une détection robuste des défauts en présence de variabilité. Les modèles analytiques développés dans le troisième chapitre sont également étendus afin de permettre l'évaluation de l'impact de la variabilité sur la gamme de détectabilité des défauts de court-circuit, en se basant uniquement sur des simulations du circuit sain. Finalement, sur la base de simulations de Monte-Carlo réalisées sous Cadence SPECTRE, les propriétés de testabilité des implantations « Low-$V_T$ » et « Regular-$V_T$ » sont établies pour les deux technologies et les conditions de fonctionnement les plus favorables sont déterminées. Les résultats montrent que, dans ces conditions de fonctionnement les plus favorables, la détection des défauts de court-circuit résistif peut être garantie dans une gamme légèrement plus grande en FDSOI plutôt qu'en Bulk pour les implantations « Regular-$V_T$ », et dans une gamme similaire pour les implantations « Low-$V_T$ ». Les résultats mettent également en évidence l'importance de la prise en compte de la variabilité, dans la mesure où les conclusions sur les conditions les plus favorables déterminées avec des conditions de fabrication typique se révèlent erronées pour certains défauts.

Finalement le dernier chapitre conclut le manuscrit, en résumant les principaux résultats. Cette thèse constitue un premier travail novateur dans le domaine de la testabilité des défauts de fabrication pour les technologies émergentes que sont le FDSOI et FinFET. Un certain nombre de points n'ont toutefois pas été abordés et ouvrent des perspectives pour des travaux futurs, parmi lesquelles on peut citer une étude plus approfondie de la détection des défauts classiques en technologie FinFET si l'on dispose de modèles de simulation industriels validés par du silicium, l'étude de la détection de défauts par des techniques de test en courant (« IddX »), l'étude de défauts

intra-portes et notamment au sein de portes NAND, NOR, etc., l'étude de nouveaux défauts spécifiques aux technologies FDSOI et FinFET.

# ABSTRACT

Fully Depleted Silicon on Insulator (FDSOI) and Fin Field Effect Transistor (FinFET) are new innovations in silicon process technologies that are likely alternatives to traditional planar Bulk transistors due to their respective promising ways of tackling the scalability issues with better short channel characteristics. Both these technologies are aiming in particular at regaining a better electrostatic control by the gate over the channel of the transistor. FDSOI is a planar MOS technology and as a result it is much more in continuity with planar Bulk as compared to the vertical FinFET transistors. The competition between these two technologies is fierce and many studies have been reported in the literature to compare these technologies in terms of speed performance, power consumption, cost, etc. However, these studies have not yet focused on their testability properties while the impact of defects on circuits implemented in FDSOI and FinFET technologies might be significantly different from the impact of similar defects in planar MOS circuit.

The work of this thesis is focused on implementing similar design in each technology and comparing the electrical behavior of the circuit with the same defect. The defects that are considered for our investigation are inter-gate resistive bridging, resistive short to ground terminal (GND), resistive short to power supply ($V_{DD}$) and resistive open defects. Defect detectability is evaluated in the context of either Boolean or Delay based test. HSPICE and Cadence SPECTRE simulations are performed varying the value of the defect resistance and the concept of critical resistance is used to compare the defect detectability range in different technologies. The optimal body-biasing, supply voltage and temperature settings to achieve the maximum defect coverage are determined for these defect types. An analytical analysis is proposed for short defects based on the ON-resistance of P and N networks, which permits to evaluate the value of the critical resistance without performing fault simulations. Testability properties are also established under the presence of process variations based on Monte-Carlo simulations for both Regular-$V_T$ devices (FDSOI-RVT and Bulk-LR) and Low-$V_T$ devices (FDSOI-LVT and Bulk-LL) available for 28nm Bulk and FDSOI technologies.

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# LIST OF ABBREVIATIONS

| | |
|---|---|
| **ATE** | Automatic Test Equipment |
| **ATPG** | Automatic Test Pattern Generation |
| **BB** | Body-Biasing |
| **BOX** | Buried Oxide |
| **BSIM – CMG** | Berkeley Short-channel IGFET Model for Common Multi-Gate |
| **CMOS** | Complementary Metal Oxide Semiconductor |
| **$C_{ox}$** | Capacitance of oxide |
| **CUT** | Circuit Under Test |
| **CV** | Coefficient of Variation |
| **DCR** | Dynamic Critical Resistance |
| **DGFET** | Double Gate Field Effect Transistor |
| **FBB** | Forward Body-Biasing |
| **FDSOI** | Fully Depleted Silicon On Insulator |
| **FinFET** | Fin Field Effect Transistor |
| **FPITCH** | Fin Pitch |
| **GND** | Ground |
| **HFIN** | Height of Fin |
| **IC** | Integrated Circuit |
| **IDDQ** | Integrated Circuit Quiescent Current |
| **IGFET** | Independent Gate Field Effect Transistor |
| **L** | Gate Length |
| **LL** | Low power thin oxide Low-$V_T$ |
| **$L_n$** | Gate Length in N-transistor |

| | |
|---|---|
| **$L_p$** | Gate Length in P-transistor |
| **LR** | Low power thin oxide Regular-$V_T$ |
| **LVT** | Low – $V_T$ |
| **MASTAR** | Model for Analog and Digital Simulation of MOS Transistor |
| **MOSFET** | Metal Oxide Semiconductor Field Effect Transistor |
| **MuGFET** | Multiple-Gate Field Effect Transistor |
| **NBB** | No Body-Biasing |
| **NFIN** | Number of Fin |
| **N-NFIN** | Number of Fins in N-transistor |
| **P-FIN** | Number of Fins in P-transistor |
| **PV** | Process Variation |
| **PVT** | Process Voltage Temperature |
| **RBB** | Reverse Body-Biasing |
| **RBD** | Resistive Bridging Defect |
| **$R_C$** | Critical Resistance |
| **$R_{C\text{-}GND}$** | Critical Resistance for short-to-GND defect |
| **$R_{C\text{-}VDD}$** | Critical Resistance for short-to-$V_{DD}$ defect |
| **RF** | Radio Frequency |
| **$R_{N\text{-}ON}$** | ON-Resistance of N-transistor |
| **$R_{OP}$** | Resistance of Open defect |
| **$R_{P\text{-}ON}$** | ON-Resistance of P-transistor |
| **$R_{SH}$** | Resistance of Short defect |
| **RVT** | Regular – $V_T$ |
| **SCE** | Short-Channel Effect |
| **SoC** | System on Chip |
| **SOI** | Silicon on Insulator |

| | |
|---|---|
| **SS** | Subthreshold Slope |
| **SSI** | Small Scale Integration |
| **TFIN** | Thickness of Fin |
| $\mathbf{t_{FR}}$ | Fall-to-Rise delay |
| $\mathbf{T_{SS}}$ | Worst-case delay (*Slow-Slow* process corner) |
| $\mathbf{T_{TYP}}$ | Typical delay |
| **UTBB** | Ultra Thin Body Buried-oxide |
| $\mathbf{V_{BB}}$ | Back Biasing Voltage |
| $\mathbf{V_{BS}}$ | Body-to-Source Voltage |
| $\mathbf{V_{DD}}$ | Supply Voltage |
| $\mathbf{V_{Diode}}$ | Breakdown Voltage of Diode |
| $\mathbf{V_{DS}}$ | Drain-to-Source Voltage |
| $\mathbf{V_{GS}}$ | Gate-to-Source Voltage |
| $\mathbf{V_T}$ | Threshold Voltage |
| $\mathbf{V_{TH}}$ | Logic Threshold Voltage |
| **VLSI** | Very Large Scale Integration |
| **W** | Width of transistor |
| $\mathbf{W_{eff}}$ | Effective channel Width |
| $\mathbf{W_{min}}$ | Minimum possible width of FinFET transistor |
| $\mathbf{W_n}$ | Width of NMOS |
| $\mathbf{W_p}$ | Width of PMOS |

# 1 Context and Thesis Objectives

## 1.1 Semiconductor Technology Evolution

Over the past few decades, MOS ICs have met the world's growing needs for electronic devices for computing, automotive, communication and other applications with steady improvements in cost, speed and power consumption. Such substantial improvements in turn arouse and enable new applications and fuel the growth of IC sales. This steady growth of the global semiconductor industry has also been driven by the demand for enhancing performance and functionality at reduced cost. In order to meet this entrenched expectation from MOSFETs to continue rapid improvements, the transistor feature size is scaled down ceaselessly, following the famous so-called Moore's law [1]. The "Moore's Law" is an empirical observation of the persistent periodic increase in the level of miniaturization, the formulation that has been accepted as a general consensus states that: "the number of components per chip doubles every 18 months" [2]. This continual cramming of more silicon transistor onto integrated circuits has been the feedstock of exuberant innovation in computing. A simple example of this trend is the progression from Small Scale Integration (SSI) to Very Large Scale Integration (VLSI) devices with many millions of transistors, commonly used in today's computers and electronic appliances.

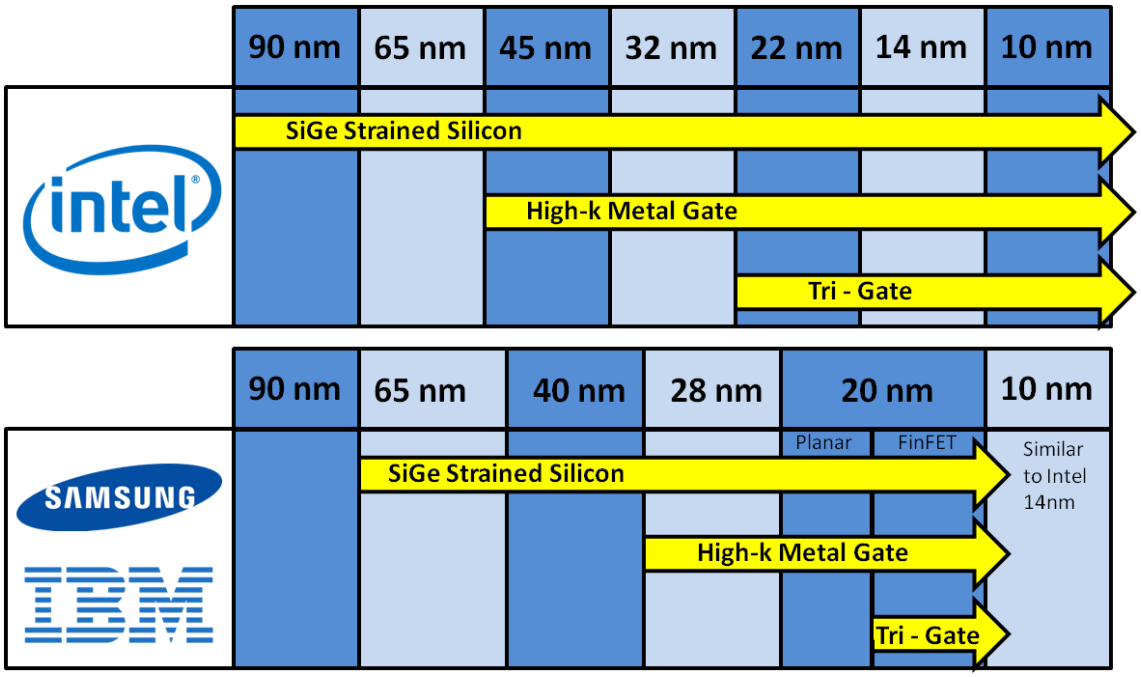



**Figure 1.1: Technology roadmap of various semiconductor industries.**

The scaling of the transistors results in introduction of a new technology generation or technology node. At each new technology node, benefits in terms of higher integration, lower energy consumption and better performances are achieved. The reduction in feature size has also resulted in increased operating frequencies with current commercially available microprocessors operating in the gigahertz range. Thus, semiconductor technology scaling optimizes circuit performance and power consumption with every new technology generation, and allows realization of more and more complex systems [3]. Figure 1.1 representatively depicts the technology roadmap of the leading semiconductor industries like Intel, Samsung and IBM.

## 1.2 Challenges in Advanced Technology Nodes

The more an IC is scaled, the higher becomes its packing density, the higher its circuit speed, the lower its power dissipation. However, these benefits are accompanied by host of challenges like severely increasing short channel effects, process variations and increasing susceptibility to resistive short defects due to higher packaging densities [4]. At 28nm and beyond, the conventional planar bulk transistor has proved to be inadequate in offering the expected higher performances with lower power consumption. In order to calculate the impact of transistor scaling on electrical characteristics, MASTAR (Model for Analog and digital Simulation of mos TrAnsistoRs) has been extensively used in ITRS 2005 Process, Integration, Device and Structure report [5], [6]. Figure 1.2 shows typical values for Drain-Induced Barrier Lowering (DIBL) in Bulk, FDSOI and Double-Gate MOSFETs, as a function of gate length [7]. It is quite evident that at shorter channel length, thin film SOI devices and Double-Gate MOSFETs offers a better electrostatic integrity than the Bulk MOSFETs. Various strain techniques have also been applied to continue the performance growth rate but the boost offered was not in accordance with the increasing manufacturing costs.

In order to continue the technology roadmap, the leading industrial communities came up with their respective promising solutions to tackle the scalability issues with better short channel characteristics [8]. The main idea was to increase the carrier mobility and electrostatic controllability by the gate along with reduced random

dopant fluctuations [9]. STMicroelectronics, recently followed by Global Foundries have already adopted the planar MOS technology called FDSOI (Fully Depleted Silicon on Insulator) as a new innovation in silicon process technology that leverages existing manufacturing approaches to continue transistors down-scaling beyond 28nm [10]. Intel and TSMC have been reported to pursue with the vertical MOS technology known as FinFET (Fin Field Effect Transistor) that comes under the category of a Multiple-Gate Field-Effect Transistor (MuGFET) [11]. Some semiconductor companies like Samsung and IBM currently develop both technologies. The primary innovation lies in the fact that some physical changes are made in the structure of the transistor itself in order to continue with the phenomena of scaling. These emerging technologies claim to be better than the conventional Bulk transistors in terms of speed and power specifications but it is also very important to study them from the testing point of view. Indeed, these physical changes may lead to differences in the impact of defects on the faulty behavior and some other types of defects can be expected from the structurally modified transistors.

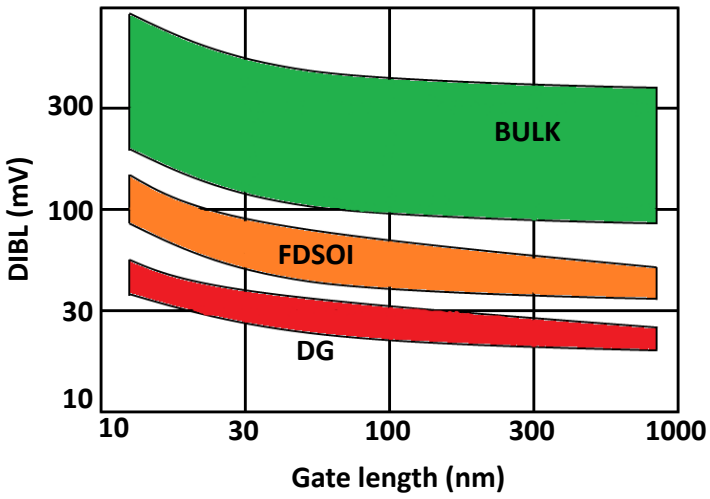



**Figure 1.2: Typical DIBL in Bulk, FDSOI and DG-MOSFET calculated by MASTAR [7].**

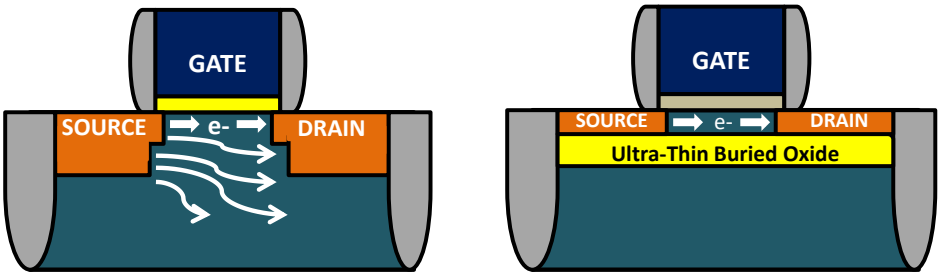
## 1.3 Technology Overview

Fully Depleted Silicon on Insulator (FDSOI) and Fin Field Effect Transistor (FinFET) are likely alternatives to traditional planar Bulk transistors for future

technologies due to their respective promising ways of tackling the scalability issues with better short channel characteristics. We discuss hereafter the innovation of these technologies with reference to conventional Bulk devices.

### 1.3.1 FDSOI Technology

With Bulk-Si devices running into a number of fundamental physical limits, Silicon-on-Insulator (SOI) technology has been proposed to achieve high-speed operations at lower supply voltages thus providing an excellent low-power solution to chip implementation. The innovative Ultra Thin Body Buried-oxide Fully Depleted Silicon on Insulator or UTBB FDSOI delivers the benefits of reduced silicon geometry while maintaining a simple manufacturing process. It is a planar technology and the primary innovation lies in introducing a thin silicon film that actually implements the channel. A thin insulating layer or BOX layer, made by oxygen implantation into Si lies between the top Si layer and the supporting substrate or base wafer as shown in Figure 1.3 [12], [13]. The BOX layer in FDSOI confines the charge carriers in the channel itself in order to avoid the leakage of the charge carriers into the substrate. The silicon film is so thin that no doping in the channel is required and as a result the device is fully depleted.




**(A)** **(B)**

**Figure 1.3: (A) Bulk and (B) FDSOI transistor.**

FDSOI technology reuses almost 90% of the process steps used in 28nm Bulk technology with identical manufacturing tools [12]. In Bulk devices, the current characteristics of each transistor are different because of the difference in the doping levels. However, in FDSOI, since the channel is fully depleted, there are fewer issues of variability. The technology road map has already been designed for FDSOI till 10nm node. Table 1.1 shows the scalability achieved in FDSOI by reducing the thickness of SOI ($T_{SOI}$) and BOX layer ($T_{BOX}$) at advanced technology nodes [9].

The major advantage that FDSOI offers is the feature of wide and effective body biasing [12], [13]. Using body biasing a buried gate is created below the channel because of the presence of an ultra thin buried oxide layer, making it act like a vertical double gate transistor. The characteristics of a FDSOI can be changed by applying different voltages at the top and the buried gate (Body Biasing). By choosing an optimal combination of voltages at these two gates, the transistor characteristics can be transformed for either higher performance or lower power applications. The parasitic current leakage limits the ability to implement body biasing in Bulk technology. The buried oxide layer in FDSOI not only prevents any leakage in the substrate but also allows a much higher voltage at the body, leading to significant boost in the performance. The UTBB FDSOI provides a much better control over its body terminal and as a result supports body biasing more readily than bulk silicon devices. In order to dynamically adjust the switching performances and leakage, a combination of forward and reverse body biasing can be implemented in an optimized manner based on the requirements of the application. The two different $V_T$ options offered are: Regular-$V_T$ (RVT) and Low-$V_T$ (LVT).

**Table 1.1: UTBB FDSOI scalability to 10nm node.**

| **Technology Node** | **28nm** | **14nm** | **10nm** |
|---|---|---|---|
| $T_{SOI}$ (nm) | 7.5 | 6 | 5.5 |
| $T_{BOX}$ (nm) | 25 | 15 | 10 |

### 1.3.2 FDSOI – Regular $V_T$ (RVT)

As shown in Figure 1.4, Regular-$V_T$ (RVT) devices are built on a standard well, with NMOS seated on a P-well and PMOS seated on an N-well. It enables strong Reverse Body Bias (RBB) to cut transistor quiescent leakage. However, the specified value of the back biasing voltage ($V_{BB}$) should be less than half of the summation of the supply voltage ($V_{DD}$) and the breakdown voltage of the diode ($V_{Diode} \approx 0.7V$) created between N and P wells, so that the deep-substrate diode illustrated does not turn on and create excessive leakage. As a result, for a supply voltage of 1V, the maximal positive (or forward) possible body biasing is 0.8V. Although there is no theoretical limitation for negative (or reverse) body biasing, the extreme value used in practice is -1.8V as far as higher voltages are difficult to generate on-chip.

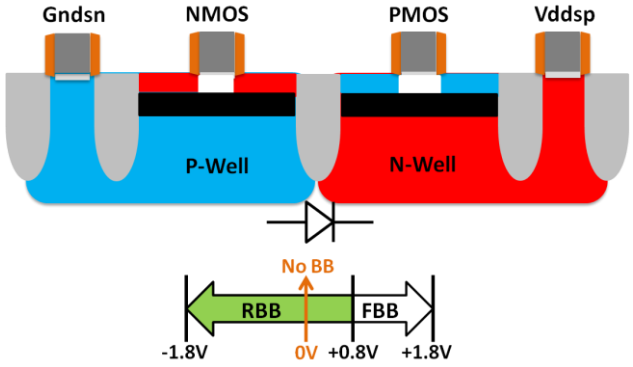



**Figure 1.4: UTBB FDSOI –RVT with the range of Body Biasing.**

The possible range of body biasing for an RVT transistor can be given as [-1.8V, 0.8V], i.e. a wide range of Reverse Body Biasing (RBB) and a significantly smaller range of Forward Body Biasing (FBB). The body and the source terminal in case of PMOS are connected to supply voltage ($V_{DD}$) while in case of NMOS they are connected to ground (GND) terminal. Thus, $V_{BS}$ or voltage across body and source is symmetric in case of a RVT transistor.

### 1.3.3 FDSOI – Low $V_T$ (LVT)

Figure 1.5 presents a Low-$V_T$ (LVT) device built on a flip-well with NMOS seated on an N-well and PMOS seated on a P-well. It enables to apply high Forward Body Biasing (FBB) to improve the switching speed at an expense of leakage. The specified range of body biasing for an LVT transistor is given as [-0.3V, 1.8V], i.e. the value of back biasing, $V_{BB}$, superior to $-V_{Diode}/2$ and inferior in practice to 1.8V.

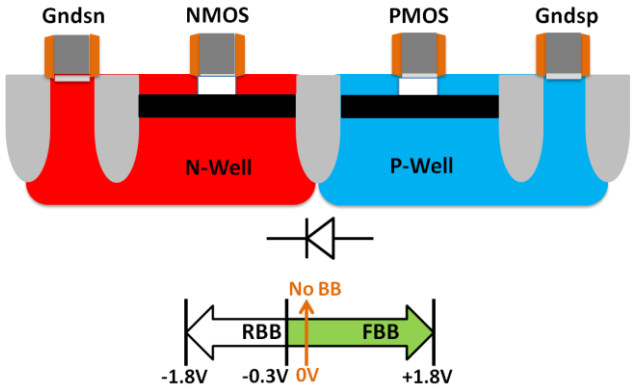



**Figure 1.5: UTBB FDSOI –LVT with the range of body biasing.**

It thus offers a wide range of forward body biasing and a significantly smaller range of reverse body biasing. In case of an LVT transistor, for a PMOS, body terminal is connected to ground (GND) while source is connected to supply voltage ($V_{DD}$). For an

NMOS, both body and the source terminal are grounded. As a result, $V_{BS}$ or voltage across body and source is asymmetric in case of a LVT transistor.

### 1.3.4 FinFET Technology

FinFET technology has been introduced because of relentless increase in the levels of integration. Fin Field Effect Transistor with a raised channel or "Fin" comes under the category of a multiple gate field-effect transistor (MuGFET) [7]. The main idea behind a vertical transistor is to have a better electrostatic control over the channel by wrapping up the gate across the channel in order to reduce the short channel effect [14]. The Figure 1.6 (A) shows a planar Bulk transistor with width "W" and the gate length as "L". The structure of a vertical FinFET transistor can be understood from a planar Bulk transistor as illustrated, i.e. if we cut the planar Bulk transistor into three thirds and let the two sides at the edges to drop down, then we have a structure similar to the vertical FinFET transistor as shown in Figure 1.6 (B).

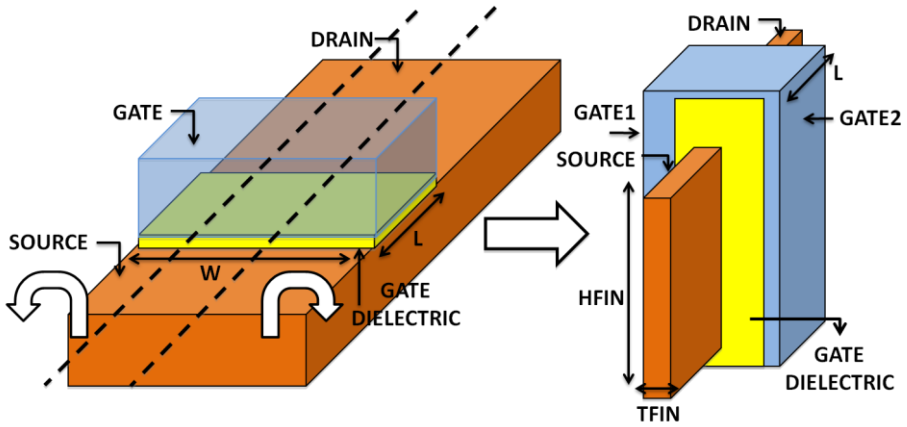



**Figure 1.6: (A) Bulk and (B) FinFET transistor.**

We can thus interpret the effective channel width ($W_{eff}$) of a vertical FinFET transistor as the summation of thickness of fin (TFIN) and twice the height of the fin (HFIN) i.e. the total transistor width is quantized [15], [16]. The gate length "L" remains the same in both cases. Table 1.2 presents some of the parameters that have been extracted from BSIM-CMG (Berkley Short-channel IGFET Common Multi-Gate) model [17]. FPITCH is the summation of spacing between the fin and the fin width; it is limited by lithography pattern capability. Exactly a single fin (NFIN=1) can be placed in one fin pitch. It is also an important parameter to compare the area efficiency with a planar device. The ratio of $W_{eff}$/FPITCH also known as '3D factor' demonstrates the

additional device width from a FinFET as compared to a planar FET due to fin construction [18].

**Table 1.2: Values of the parameters extracted from the model.**

| Parameters | L | TFIN | FPITCH | NFIN | HFIN |
|---|---|---|---|---|---|
| Values (nm) | 30 | 15 | 80 | 1(min.) | 30 |

A vertical FinFET transistor is expected to be much faster than the conventional Bulk devices because of excellent control over the channel by the gate on three sides of the channel. It however suffers from various manufacturing complications. Manufacturing a vertical FinFET transistor is very costly and complex, especially the process of fin formation. In a FinFET on a Bulk substrate, all the fins share a common silicon substrate. However, the fins are physically isolated in case of a FinFET on SOI substrate [19]. It is recommended to use a higher number of smaller fins rather than fewer taller fins, as far as taller fins are structurally unstable [14], [19]. Also, using a higher number of fins leads to more silicon area overhead as the width is also a function of the number of fins "NFIN" of one transistor [15], [16]. However, compared to Intel's 22nm process, the 14nm process's fins are more tightly packed, thinner, taller and fewer in number (per transistor).

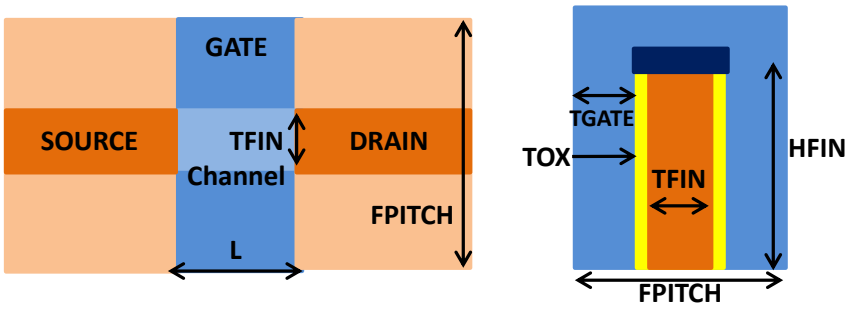



**Figure 1.7: Top and cross-sectional view of a FinFET with a single fin (NFIN=1).**

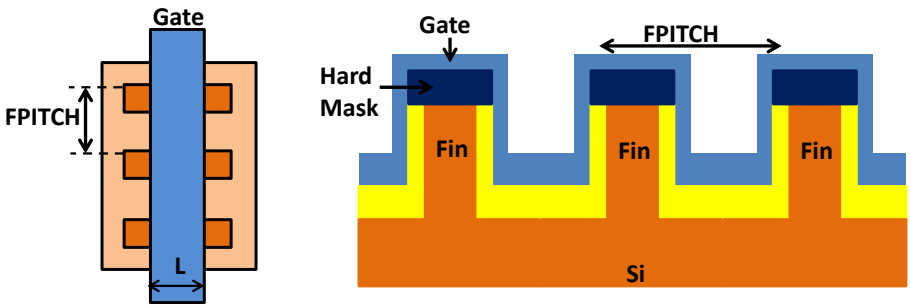



**Figure 1.8: Top and cross-sectional view of a FinFET with multiple fins (NFIN=3).**

In our study we have focused on FinFET on a Bulk substrate with shorted gate i.e. both the front and back gate are physically shorted. A hard mask is present on the top of the silicon fin to prevent the formation of parasitic inversion channel at the top corners of the device. The top gate is thus not functional because of the presence of this hard mask. The top and the cross-sectional view of a FinFET with single fin and a FinFET with multiple fins are shown in Figure 1.7 and 1.8 respectively. The current drive is fixed to a single discrete value for a FinFET with just one fin. However, for a multi fin device the current drive is equal to the current drive of an individual fin multiplied by the number of fins (NFIN) since all individual fins have same thickness and width.

**Table 1.3: Comparison of FinFET and FDSOI technologies [20].**

| Comparison | FDSOI | FinFET |
|---|---|---|
| Metal stack, Design methodology | + | + |
| Leakage mitigation | + | - |
| Dynamic power mitigation | - | ++ |
| Supply chain | - | + |
| Integration Density | - | + |
| Manufacturability | + | - |
| Variability | + | - |
| Performance | - | ++ |
| Design Portability | + | - |
| SRAM memories | ++ | - |
| Analog Design | + | + |
| Future Scaling | - | + |

Table 1.3 presents the comparison of FinFET and FDSOI technologies on a variety of criteria for a hypothetical new SoC design in a sub-20nm process [20]. The 3D architecture offered by FinFET offers a much higher drive current per footprint on the wafer as compared to FDSOI technology. However, the 3D nature of FinFET restricts its usage in analog and RF applications due to high parasitic and capacitances. FDSOI on the other hand is excellent for RF technology and is also more cost effective than FinFET due to lesser mask counts. FDSOI has an advantage over FinFET as far as manufacturing is considered because of the existing use of SOI. In terms of design portability, FDSOI is a clear winner over FinFET because of its closeness to the Bulk process. FinFET devices have a better integration density and are supposed to be better candidate for future scaling.

The competition between FDSOI and FinFET technology is fierce and many studies have been reported in the literature to compare these technologies in terms of performance, power consumption, cost etc. However, the studies have not yet focused on their testability properties. The impact of defects on circuits implemented in FDSOI and FinFET technologies might be significantly different from the impact of similar defects in planar MOS circuit. It is therefore the objective of our work to address this aspect.

## 1.4 Manufacturing Defects

Manufacturing defect is a flaw or physical imperfection that may lead to a fault causing an error that can result in a system failure. Due to unavoidable statistical flaws in the materials and masks used to fabricate ICs, it is impossible for 100% of any particular kind of IC to be defect-free [3]. Semiconductor manufacturing processes may induce permanent defects in a chip during one or more of the process steps involving implantation, etching, deposition, cleaning and lithography due to imperfections. These defects are becoming more common as technologies are scaled down due to changes in materials and fabrication steps of ICs manufacturing processes [21]. Moreover the technology scaling and increasing complexity also give rise to defects which are more subtle and difficult to detect [22], [23]. We discuss hereafter the classical defects such as short and open defects affecting the traditional CMOS technologies followed by some of the new defects specific to the emerging FDSOI and FinFET technologies.

### 1.4.1 Short Defects

A short defect is defined as an unintended connection between two or more otherwise unconnected nodes. Often they are referred to as bridging faults or simply as bridges [24]. A short defect can occur between an internal node and a node connected to ground terminal (GND) or power supply terminal ($V_{DD}$) as shown in Figure 1.9 (A) and (B) respectively.

These kinds of defects can be modelled as a stuck-at fault. However, the stuck-at fault model does not permit to correctly represent the defect behavior in the complete range of realistic defect resistance values. A short defect can also occur between two

internal nodes as shown in Figure 1.9 (C). In this case, the defect is referred to as inter-gate bridge. Here again, the stuck-at fault model fails in adequately predicting the behavior of such defects [21].

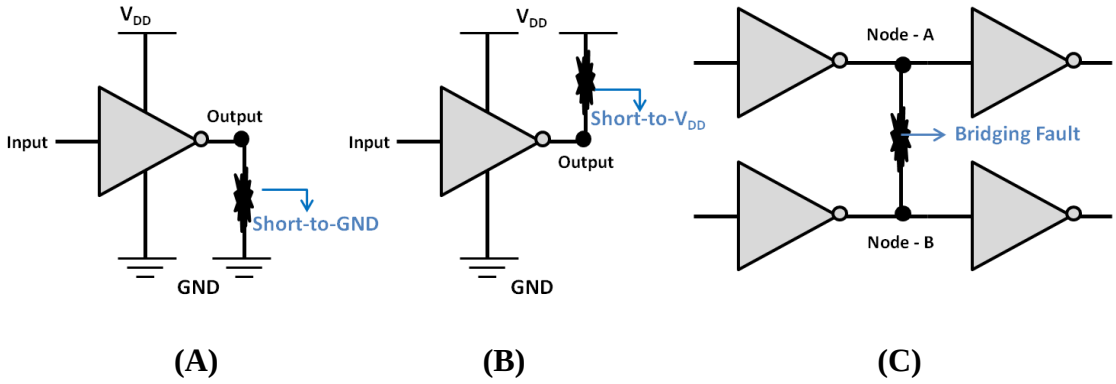



**Figure 1.9: (A) Resistive short to GND terminal (B) Resistive short to $V_{DD}$ terminal (C) Resistive inter-gate bridging fault.**

Short defects may also occur within logic gates (intra-gate bridges) or even within a transistor. As an example, a gate-oxide short is a transistor defect that causes a relatively low impedance path between CMOS gate and the underlying silicon [25]. The generic MOS transistor structure shown in Figure 1.10 illustrates the various gate oxide short defects: gate-drain, gate-source and gate-channel shorts.

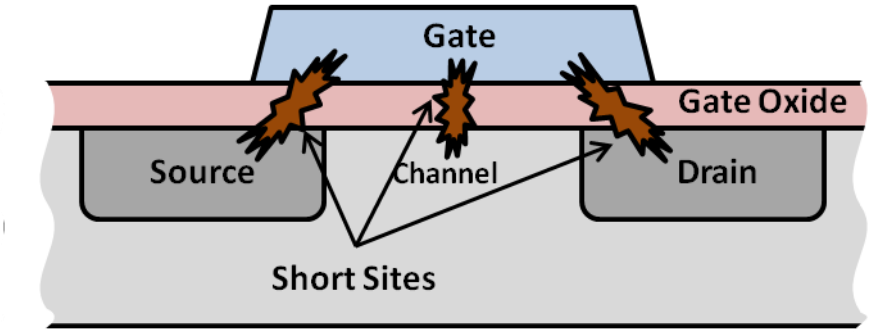



**Figure 1.10: Gate oxide short defects in MOS transistor.**

Resistive short defects are responsible for a large percentage of failures in CMOS technologies and the advent of nanometric technologies with extensive interconnect structures contributes to the need of effective models for this defect. Prolific literature can be found on modeling such defects. A pioneering work on wired bridging fault models was reported in [26], assuming that the values on the bridged nets are both the same (zero bridge resistance) and are the result of an AND or an OR operation between the logic values of the nets, respectively [21]. The *Voting Model*

proposed in [27] was a refinement of the *wired-AND* and *wired-OR* fault models. When one of the gates driving the shorted nodes is stronger than the other gate under all conditions, its output dominated the other gate and determines the resulting logic value on the shorted nodes [28] i.e. one of the nodes always wins the vote regardless of the logical values on the other nodes. However, this model failed to accurately interpret the results for PMOS and NMOS networks with similar strengths. Also, the model assumed that all the downstream gates have the same threshold. The *biased voting model* proposed in [29] overcame these limitations by calculating the voltage values of the bridged nets using an iterative procedure. In order to avoid the time consuming iterative procedure to calculate the intermediate voltage, a direct voting method [30] was proposed. This model facilitated the computation of intermediate voltage between two logic nodes set to opposite values based on just the topological parameters ($W_p$, $L_p$, $W_n$ and $L_n$) and technological parameters ($C_{OX}$, $\mu_n$, $\mu_p$, $V_{Tn}$, $V_{Tp}$…). Later in [31], [32] more interesting models were introduced which permit to take into account the resistance of the bridge. The basic concept of these models is to evaluate the detectable resistance ranges using the concept of critical resistance, i.e. the maximum value of the bridge resistance above which the circuit does not show faulty logic behavior [33]. In a more recent work carried out in [34], the critical resistance was calculated based on the Fitted and Predictive transistor models.

### 1.4.2 Open Defects

An open defect consists of the partial or total breaking of the electrical connection between two points in a circuit which should be electrically connected by design [21]. Failures associated with open defects are common in CMOS technologies. This class of defects is becoming more frequent with technology shrinking due to the increase of vias/contact and partly because of the presence of new process techniques [35], [36]. An open defect can be classified based on its location as:

- **Interconnect opens**: These open defects result in gate input pairs being partially or totally disconnected from their drivers. The physical explanation of interconnect opens can be either a metal or polysilicon crack/void or a defective contact/via [21]. These kind of defects are mostly likely to appear in an interconnect line [37]. Figure 1.11 shows a partially disconnected load from the driver gate.

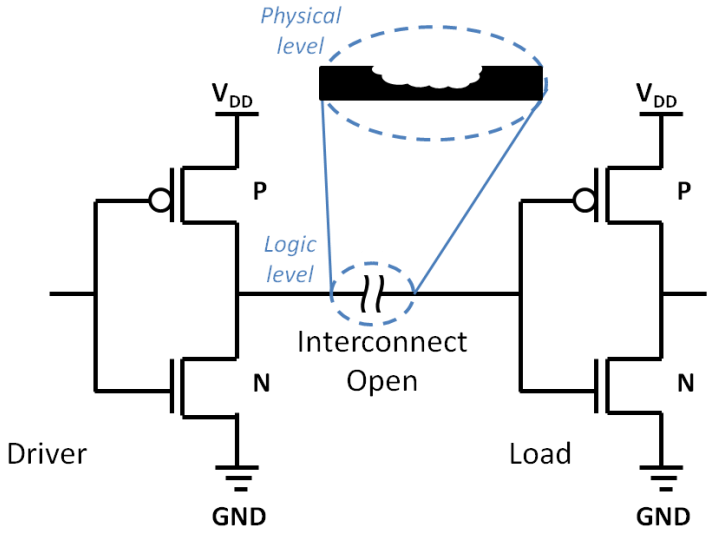



**Figure 1.11: Interconnect open**

- **Intra-gate opens**: These open defects are the one that appears inside the logic gate itself. If the open defect is between the drain/source of one or more transistor then it is known as *Transistor network open*. A disconnection between a single or multiple transistor gate(s) from its (their) driver is called as *Single/Multiple floating gate(s)* and if the defect breaks or weakens the connection between the bulk (body) of an NMOS transistor and GND, or the bulk of a PMOS transistor and $V_{DD}$ then it is termed as *Bulk open*. Figure 1.12 illustrates these intra-gate open defects [21].

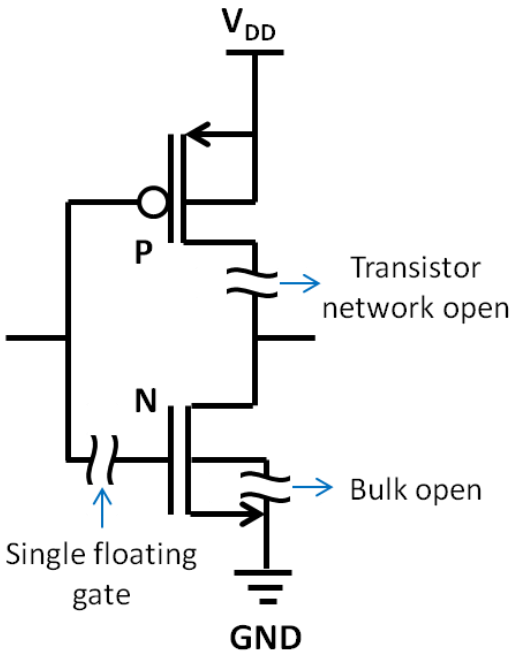
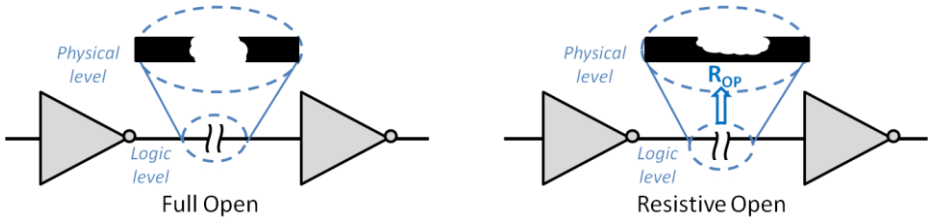



**Figure 1.12: Intra-gate opens [21].**

Apart from their location open defects can also be classified on the basis of its resistance as:

- **Full (or strong) open**: A complete isolation of the electrical connection between the two end points of a line due to the lack of conductive material results into a strong or full open as shown in Figure 1.13(A). A majority of reported open defects in metal lines belong to the class of full opens.
- **Resistive (or weak) open**: A partial disconnection between the nodes at both ends of a line is said to be a weak or resistive open defect. A resistive open weakens the affected signal, which has delay consequences on the transient behavior of the defective circuit [38]. In [39] it was shown that only a non-negligible amount of open defects belonged to the class of weak opens. Figure 1.13(B) shows a partial break on the interconnect which can be modeled as a resistive open defect ($R_{OP}$).




**(A)** **(B)**

**Figure 1.13: (A) Full or strong open defect and (B) Resistive or weak open defect**

Since 1970s, an intensive research effort has been dedicated to model and characterize the behavior of CMOS circuits in the presence of open defects [40], [41]. Some key development in modeling and electrical characterization of circuits with interconnect opens was presented later during the 1990s as it was established that these defects are most likely to appear in an interconnect line [37]. In [42], [43] and [44] the classical model for full opens in interconnect lines capacitively coupled with the neighboring line was presented. The first experimental measurements to deduce the unknown value of the resistance in case of a weak open defect in an interconnecting line were obtained in 2002 [39] and the results showed that a high percentage of the defects were of full nature. Still a special attention has been paid to interconnect resistive opens as they can be modeled like interconnect full opens by replacing the complete disconnection by an open resistance [21]. In comparison to the defect-free case, the presence of an interconnect resistive open defect lead to additional delay in the circuit.

The physical factors influencing this additional delay were experimentally analyzed in [45] and as expected, the delay was found to increase with longer coupling capacitances and higher open resistances. When the resistance of the open is significantly higher than the ON-resistance of the driving gate then the delay increases as the open is located close to the beginning of the line. However, for the low resistive opens, the delay is higher when the open is located in the middle of the interconnect line [46].

### 1.4.3 Defects specific to FDSOI and FinFET

The emerging transistor technology with its significant structural difference from traditional planar devices makes it essential to revisit whether existing fault models are appropriate to detect faults in them. However, FDSOI technology is much more in continuity with planar Bulk. The process steps used for manufacturing FDSOI is almost similar to the one used for Bulk technology. As a result similar manufacturing defects can be expected in FDSOI. The ultra-thin top silicon and the buried oxide (BOX) layer however make them more vulnerable to catastrophic breakdown. With the presence of BOX layer specific to FDSOI technology, the new defect can thereby be the breakdown of this BOX layer itself as shown in Figure 1.14. The break may even run vertically from the Si/buried oxide interface up to the surface of silicon overlayer, posing yield and reliability hazard problems. Thus test strategies may need to be augmented to target them.

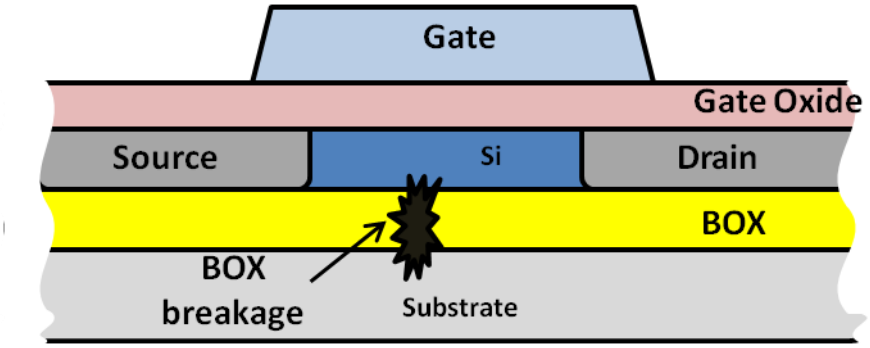



**Figure 1.14: Defect specific to FDSOI – BOX layer breakage.**

FinFET being a vertical transistor technology is significantly different from the conventional planar devices. The existing structural fault models need to take into account the differences in the faulty behavior between traditional planar MOSFET and FinFET. In a traditional planar device, a defect in the active region of the device affects the entire transistor. However, a FinFET device has different number of fins within one transistor to implement different electrical width (explained in Section 1.3.4) and as a

result defects on only one fin or part of the fins would not affect the entire transistor as the other fins keep working. It is unique for FinFET that current channel is made up with integer number of fins. Therefore, the case that defect occur on individual fins is unique for FinFET gate when considering the fault modeling [47].

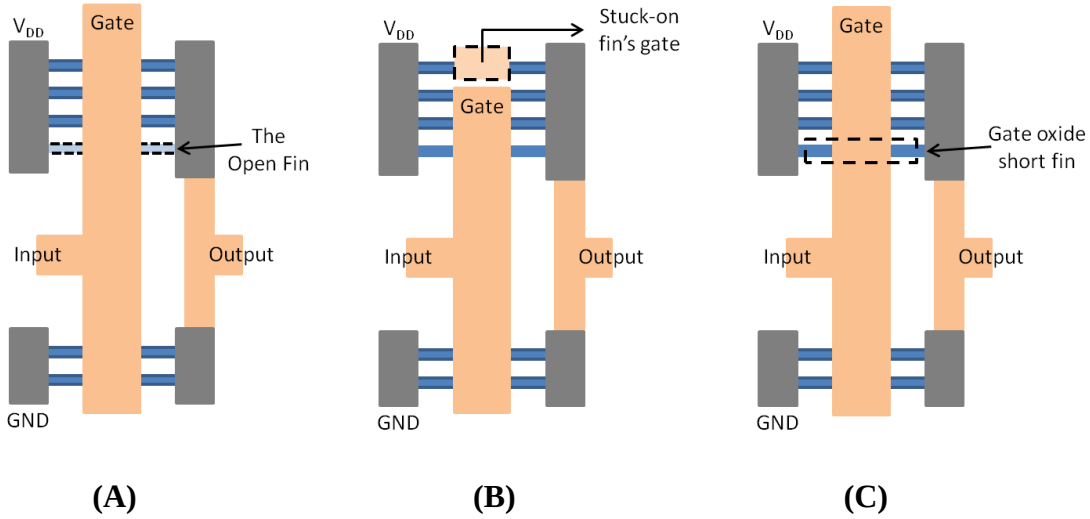



**Figure 1.15: Defect specific to FinFET (A) Cut on the Fins (B) Stuck-on for the Fins (C) Gate Oxide Short for the Fins [47].**

We hereafter discuss some of the defects that are specific to FinFET technology as presented in [47]. Fins in FinFET may get cut off because of over etching considering their extremely small size. Figure 1.15 (A) shows an open fin in the PMOSFET of an inverter. When the number of open fins is not too large, the gate can be considered fault-free. When it exceeds, gate delay fault model can be used and delay fault test vectors can be employed to detect the defect. When all fins are cut off, it behaves as the traditional stuck-open fault [47]. Fins may behave as a wire because of badly doping or break of the fin's crystal structure. This result in stuck-on of fins irrespective of the gate voltage as shown in Figure 1.15 (B) with one of the fin of PMOSFET being stuck-on. With the inefficiency of IDDQ testing at nanometric nodes, delay fault test vectors can be used to detect this kind of defect for a sufficiently large number of stuck-on fins. In addition, the gate oxide in FinFET is as small as only 1nm [48], it is more likely than ever that the oxide may get broken by large electric field. Figure 1.15 (C) illustrates the case of gate oxide short for the fins. Again, with the inefficiency and difficulty of implementation of IDDQ testing for FinFET, delay fault vectors can be utilized for test. Furthermore, because of the special configuration of FinFET, multiple gates may get influenced by a defect such as back gate open,

traditional delay fault model may fail to detect it and new test generation strategies are required [47]. In [49] an analysis of short defects in FinFET based logic cell is performed. It is shown that new test strategies should be developed for FinFET based logic circuits to have circuits with higher quality. In our study we have not targeted the defects that are specific to these technologies as the idea is to carry out a comparative study of the behavior of similar defects in different technologies.

## 1.5 Defect Detectability

It is important that the testing be as thorough as possible to uncover defective chips before they are shipped out [50]. However, according to past microprocessor data, the die size remains relatively constant [51], whereas the number of transistors per chip double every 2 to 3 years. This means that defect densities continue to increase. All these factors when combined with aggressive time-to-market objectives cause test escapes and raise reliability concerns.

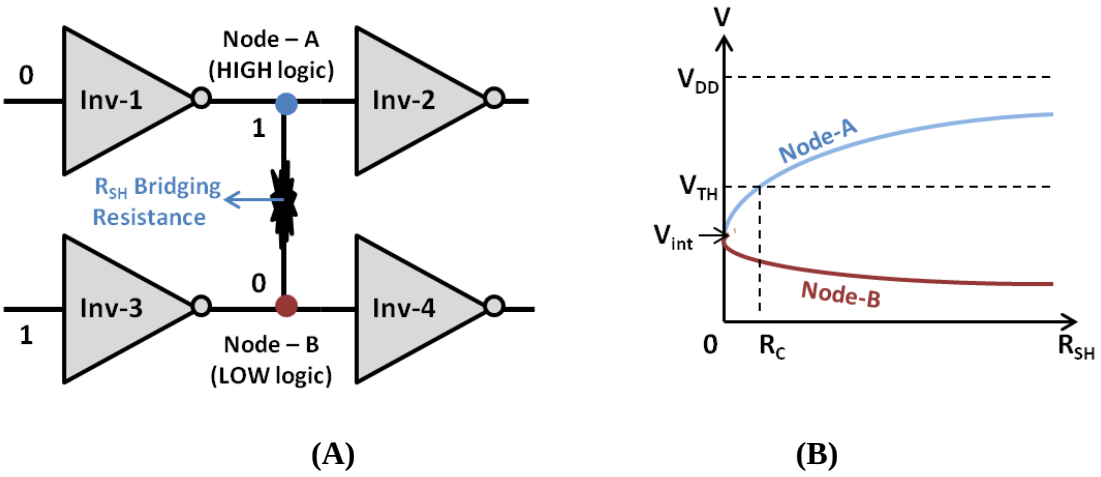
The most common test techniques for detecting defects are logic-based testing, delay-based testing and current-based testing. Operating conditions such as power supply voltage and temperature might also influence defect detection. We discuss hereafter the detectability of resistive short and open defects affecting the traditional CMOS technology.

### 1.5.1 Detectability of Short Defects

This section concisely discusses the detectability of short defects using the common test techniques, together with the influence of power supply and temperature.

- **Logic-Based Detectability**: The presence of a bridge defect may lead to a defective or defect-free effect depending on the value of the bridging resistance. This scheme could be well understood by considering a simple example of bridging defect between two chains of inverters as shown in Figure 1.16 (A) where node-A and node-B are bridged by a resistive short defect ($R_{SH}$). The bridged nets are set to opposite logic values with node-A and B at high and low logic values respectively. In order to obtain the critical resistance ($R_C$), the electrical voltages of the nodes impacted by the bridge are plotted as a function

of the resistive bridge value as shown in Figure 1.16 (B). The critical resistance thus gives the maximum value of the bridge resistance that leads to the logical switching of the downstream gate and its value depends on the location of the logic threshold ($V_{TH}$) and shape of the voltage vs. $R_{SH}$ characteristics. If the unpredictable parameter $R_{SH}$ is smaller than the critical resistance $R_C$ then a faulty logic appears on the output of the driven gate (Inv-1). This scheme is presented in detail in chapter 2.




**(A)** **(B)**

**Figure 1.16: (A) Didactic defective circuit (B) V – $R_{SH}$ characteristics.**

- **Delay-Based Detectability**: Delay-fault testing or transition-fault testing is a mainstream test technique [52], [53] since any resistive defect have an impact on the time response of the circuit. A signal propagating through a defective line causes an additional delay in a transition. If the sum of the defect-free delay and the one added by the defect exceeds the maximum delay permitted, a malfunction can be caused and the defect is detected [54], [55]. This technique is explained in detail in Chapter 4 with respect to the Dynamic Critical Resistance (DCR) that defines the detectability range of the short defects.
- **Current-Based Detectability**: Quiescent current ($I_{DDQ}$) testing has been widely used for the detection of bridging faults. The basic principle of IDDQ testing is based on monitoring the power supply current (IDDQ) once the transient current in the circuit has settled-down. The complementary nature of the p and n-networks in CMOS technologies avoids the simultaneous conduction of both networks, resulting in a negligible static current consumption in the absence of defect. The presence of a defect is detected if the value of the power supply current exceeds a certain threshold value. Figure 1.17 (A) illustrates an inverter

containing a bridge defect ($R_B$) between the output and the power supply. When the input ($V_A$) is in a low logic state, the NMOS transistor is off and the current consumption is only due to leakage current as shown in Figure 1.17 (B). However, when the input ($V_A$) is in a high logic state, NMOS transistor turns on and PMOS transistor turns off. The quiescent current consumption in this case exceeds above the defect free case because of the bridge defect, resulting in the current flow from the power rail to ground through NMOS transistor.

Unlike logic based testing, this technique does not require any fault propagation as the effect of the fault is always observable on monitoring the power supply current. High defect observability can also be achieved using IDDQ testing. However, these benefits are accompanied by the issues related to low test application times [56], [57], [58] but the major concern with IDDQ testing is its longevity with the rapidly shrinking CMOS technology. The defect-free current consumption can no longer be considered nominal anymore but ranging with a statistical distribution [59]. A clear distinction between a defective and defect-free device could be made only if the statistical current distribution of both devices are far enough. However, this is far from reality as shown in [60]. Also, the exponentially increasing leakage current for each new technology node makes it more difficult to determine whether the variation in IDDQ value is due to leakage current or due to a defect.

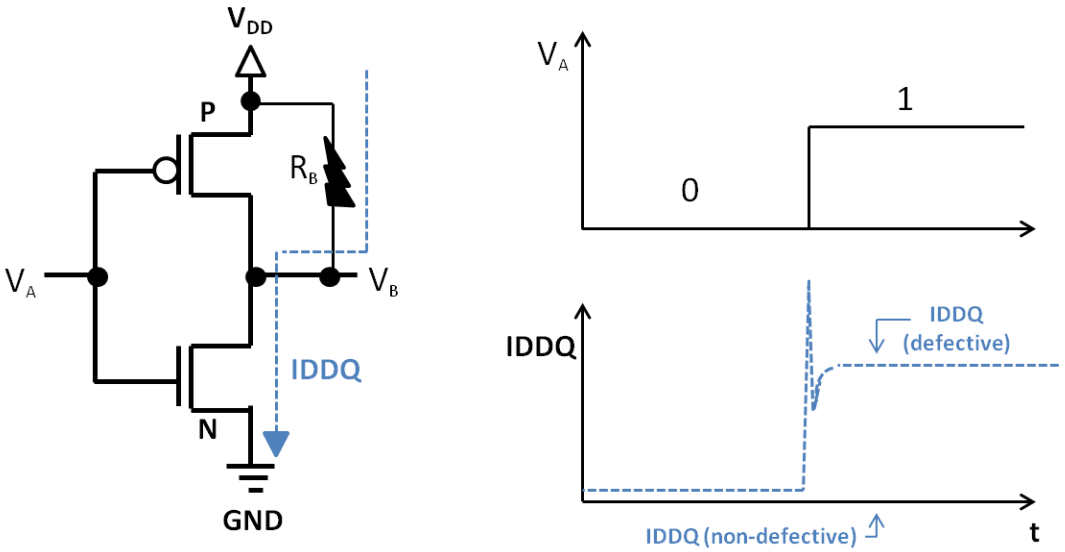



**Figure 1.17: (A) Bridging defect affecting the output of an inverter (B) IDDQ consumption versus the logical signal at the input of defective gate [21].**

- **Influence of Power Supply ($V_{DD}$)**: In order to improve the detectability of resistive short defects, a common technique is lowering the power supply voltage ($V_{DD}$) below the nominal operating value [61], [62]. On switching to a lower power supply, the value of the critical resistance (i.e. the highest bridging resistance which can be detected by means of logic tests) increases and as a result a higher detectability can be achieved for resistive short defects [52], [63]. This technique is easy to implement as it does not require any additional equipment. However, lowering the power supply also decreases the speed of the circuit-under-test there by increasing the overall test-time.
- **Influence of Temperature (T)**: The observability of resistive bridging defects can also be enhanced by the application of temperature. The bridging defect materials such as metal and polysilicon have a positive resistance temperature coefficient thus their resistance increases with temperature. Hence, at low temperature, the value of the bridging resistance decreases and it tends to induce higher IDDQ value there by increasing the defect observability. It should be pointed out that in an industrial test context, achieving a low or high temperature is time consuming, expensive and induces several practical difficulties.

### 1.5.2 Detectability of Open Defects

This section concisely discusses the detectability of open defects using the common test techniques, together with the influence of power supply and temperature.

- **Logic-Based Detectability**: Logic-based methodologies are the most common used techniques for the detection of interconnect open defects. However, they are not always effective. In [43] it was shown that in the presence of interconnect full open, the floating line voltage depends on the trapped charge (unknown constant), the ratio of the parasitic capacitances related to floating line tied to $V_{DD}$ and the sum of all parasitic capacitances. Later in [45], experimental evidences were provided to ensure the dependability of the ratio of the parasitic capacitances on a number of factors such as exact location of opens, floating line length and applied test pattern. It was interpreted that to improve the detectability of interconnect full open defect when carrying out a logic based test, the ratio between these parasitic capacitances should be maximized while testing for stuck-at-1 and minimized while testing for stuck-at-0 [21].

- **Delay-Based Detectability**: Delay testing is a widely used technique for the detection of open defects, but the optimal set of test conditions are not clear yet as performing delay test at nominal test conditions may lead to missing resistive opens. In [53] it was suggested that delay testing should be done at a supply voltage below nominal while in [52] a supply voltage above nominal proved to be better for detectability. Moreover, defects should be sensitized along a longer path to ensure better detectability. The value of the open resistance for which the delay increases above the worst case delay of the fault-free circuit is termed as the critical resistance. Results presented in [64] for a 0.25μm technology showed that for interconnect opens, most critical resistance were about a few MΩ. The history (or memory) effect should also be minimized while performing a delay test [65].
- **Current-Based Detectability**: Quiescent current ($I_{DDQ}$) testing has been widely used for the detection of resistive bridging faults. However, detection of open defects by IDDQ is strongly dependent on cell design and circuit topology [21]. The presence of interconnect full open defect may result in acquiring a voltage in the midrange between $V_{DD}$ and GND i.e. an intermediate voltage on the floating line. This makes both the transistors driven by the floating line in a conducting state, resulting in an extra quiescent current through the conducting path from $V_{DD}$ to GND [66].
- **Influence of Power Supply ($V_{DD}$)**: The modification of power supply ($V_{DD}$) has also been investigated for the detection of interconnect open defects especially by switching to a higher supply voltage [54], [55]. The circuit delay starts decreasing on increasing the supply voltage. However, the delay added by a resistive open defect is almost insensitive to power supply voltage and as a result the overall defect delay becomes more observable. In [67] the dependency of voltage-delay relationship on the location of open defect was exploited by sweeping the power supply value for transistor-related defects and resistive interconnect defects. The results showed that the major impact of switching to lower supply voltage is on the delay added by the transistor-related defects. Apart from using higher supply voltage, a combination of power supply voltage along with stressing time period can be used for enhancing the defect detectability. This technique is termed as the voltage stress technique [68], [69] and the idea is to vary the power supply and stress time in a controlled manner

such that the defects becomes more observable by causing via defects to become opens and oxide thinnings to become oxide breaks [21].

- **Influence of Temperature (T)**: Temperature can also provide a helping hand in detection of resistive open defects. Testing at low temperature or 'Cold-Testing' may improve the observability of resistive opens if the value of open resistance stays constant with the variation in temperature. However, open resistance does vary with temperature and the depending on the temperature coefficient of the resistive open material, delay added by open defect may either increase or decrease. Hence, the resistive open defects that pass the test at nominal temperature may get detected at a temperature different from the nominal one [70].

## 1.6 Research Objectives and Contributions

The work of this thesis is focused on comparing the testability properties of Bulk, FDSOI and FinFET technologies with respect to the most common defects, i.e. resistive short and open defects. The idea is to explore the electrical behavior of logic gates implemented in these technologies in presence of such defects, a single defect being introduced at the same location in all the implementations. Note that because we only have access to an “academic” model for the FinFET technology, simulation results might not be fully representative of industrial manufactured devices, especially regarding the dynamic behavior. We have therefore limited our investigations mainly to the analysis of a resistive short in the context of a static test. In contrast for Bulk and FDSOI technologies, we have access to “industrial” models thoroughly validated through silicon measurements. We can therefore be confident on the reliability of simulation results, regarding both static and dynamic behaviors. In consequence, a more comprehensive analysis is performed for these technologies, with detailed results concerning logic-based and delay-based testing, targeting either resistive short or open defects. The most suitable operating conditions in terms of power supply, temperature and body biasing to achieve maximum defect coverage are analyzed and the impact of process variations on defect detectability is also investigated.

The main contributions of the thesis are divided into six distinct chapters in this manuscript. The content of each chapter is briefly summarized below:

- **Chapter 2** presents the impact of a resistive bridging defect on the electrical behavior of logic gates for Bulk, FDSOI and FinFET transistor technologies. Our approach is based on implementing a similar design in these different technologies with the same resistive bridging short. HSPICE simulations are performed vaying the value of bridging resistance and the concept of critical resistance is used to compare the defect detectability range in the different technologies. We also explored the feature of Body Biasing in the two types of devices available in FDSOI i.e. both Regular – $V_T$ (RVT) and Low –$V_T$ (LVT) by performing a detailed study of the dynamic behavior in order to evaluate the improvement brought by a delay test with respect to a conventional static test for the three different technologies.

- **Chapter 3** demonstrates a detailed analysis for the detection of resistive short-to-ground, short-to-power supply and inter-gate bridging defects in 28nm FDSOI in the context of logic based test, considering the individual and combined improvements brought by Supply Voltage ($V_{DD}$), Body Biasing (BB) and Temperature (T). The optimal Body Biaising, Supply Voltage and Temperature settings to achieve the maximum defect coverage are determined through HSPICE simulations using a didactic circuit implemented with 28nm UTBB FDSOI – RVT and LVT gate libraries. We also propose a simple analytical model based on the ON-resistance of P and N network that enables the computation of the critical resistance in various operating conditions without performing any fault simulation. A deeper exploration of the use of Body Biaisng has also been realized for both the FDSOI implementations.

- **Chapter 4** presents a comprehensive study for detection of both weak resistive open and resistive short defects in the context of delay test for 28nm FDSOI – RVT and LVT implementations. Estimation of the critical resistance is based on the difference in the values of the delays using *Slow* and *Typical* process corners. We also investigate the influence of Supply Voltage ($V_{DD}$) and Body Biaising (BB) in order to determine optimal operating conditions that enhance the detectability range of these defects.

- **Chapter 5** focuses on the comparison of the impact of process variation on the detectability of resistive short detects in Bulk and FDSOI technologies, in the context of logic-based test. We perform the study based on Cadence SPECTRE using 28nm Bulk and FDSOI gate libraries. A comparative study is presented for both Regular-$V_T$ devices (FDSOI – RVT and Bulk – LR) and Low – $V_T$ devices (FDSOI – LVT and Bulk – LL). Based on Monte-Carlo simulations the impact of process variations on the achieved defect detectability range is analyzed under nominal and favorable operating conditions for each implementation.
- **Chapter 6** concludes the manuscript by summarizing the results of this thesis and presenting some future perspectives.

# 2 Resistive bridging defect detection in Bulk, FDSOI and FinFET technologies

# 2.1 INTRODUCTION

The impact of defects on circuits implemented in FDSOI and FinFET technologies might be significantly different from the impact of similar defects in planar MOS circuit. It is therefore the objective of the chapter to address this aspect. We compare the impact of a resistive bridging defect on the electrical behavior of logic gates for Bulk, FDSOI and FinFET technologies. Resistive bridging defects are supposed to be one of the most dominating manufacturing defects for the emerging nanoscale technologies. Some of these defects may escape the traditional test methods and hence become a concern from the reliability point of view [49]. These bridging defects usually lead to a detectable functional failure when the value of the bridging resistance is sufficiently small. However, for a higher value of the bridging resistance, these defects do not produce a functional failure but small delays that can escape detection when traditional test methods are used [71].

A particular care has been taken to design transistors and elementary gates in such a way that the comparative analysis in different technologies is meaningful. After implementing similar design in each technology, we compare the electrical behavior of the circuit with the same resistive bridging defect assuming a similar distribution of resistive short values in the different technologies and we analyze both the static and dynamic impact of this defect. HSPICE simulations are performed varying the value of bridging resistance $R_{SH}$ and the concept of Critical Resistance introduced in [33], [34] is used to compare defect detectability range in the different technologies. We also explored the feature of body-biasing offered in FDSOI and we perform a study of the dynamic behavior in order to have a first idea of the improvement brought by a delay based test with respect to a conventional static test for the three different technologies.

The chapter is organized as follows. Section 2.2 focuses on the design of the elementary transistors and gates used in the didactic circuit implemented in each technology in order to build a reasonable comparison basis. Section 2.3 presents simulation results regarding defect detectability, considering both static and dynamic analysis. Finally, some conclusions and perspectives are drawn in Section 2.4.

## 2.2 Elementary Inverter Gate in the Different Technologies

In order to compare different transistor technologies, a crucial point is to have a similar drawn gate length i.e. 30nm, for all these three technologies. The width "W" for each elementary transistor should also be set in a way such that the comparison between different transistor technologies is meaningful. The width "W" for the NMOS and PMOS in FDSOI-RVT, LVT and Bulk technologies is 200nm and 300nm respectively as the minimum specified width for the standard elementary inverter. The width in case of FinFET technology depends on the height of the fin (HFIN), thickness of the fin (TFIN) and the number of fins (NFIN) [15], [16]. The minimum possible width, $W_{min}$ for FinFET is based on these given physical parameters and can be expressed by Equation 2.1 (taking into account TFIN as explained in Section 1.3.4 of Chapter 1) or by Equation 2.2 (neglecting TFIN), leading respectively to $W_{min}$ = 75nm and $W_{min}$ = 60nm. In our case, we have not considered the thickness of the fin (TFIN) as the top gate is not functioning due to the presence of a hard mask on top of the silicon fin.

$$W_{min} = 2 \times HFIN + TFIN \quad (2.1)$$

$$W_{min} = 2 \times HFIN \quad (2.2)$$

It is practically not possible to individually modify the physical parameters like HFIN and TFIN for each transistor to adapt its width because of a high manufacturing cost. In order to adjust the total width "W" of the FinFET, the minimum width $W_{min}$ of a fin can be multiplied by the number of fins "NFIN" as shown in Equation 2.3.

$$W = W_{min} \times NFIN \quad (2.3)$$

Hence, for a reasonable comparison between these technologies, the number of fins "NFIN" in FinFET should be chosen in such a way that the total width of the FinFET transistor is in the same range than the width of transistor used in FDSOI/Bulk, i.e. a range around 200 to 300nm. In first approximation from Equations 2.2 and 2.3, we can compute that NFIN should lie between 3 and 5.

### 2.2.1 Gate Sizing in FDSOI – RVT and LVT

In this section we explain the design guidelines that lead to consideration of width of PMOS "$W_P$" and width of NMOS "$W_N$" as 300nm and 200nm respectively as specified in the FDSOI-RVT and LVT model of the elementary inverter in 28nm. The

idea is to understand such sizing of the standard inverter in order to take them into account for sizing up the elementary inverter in the FinFET technology for the best possible further comparison of the circuit electrical behavior.

For this, we have simulated a chain of three inverters and we have analyzed both the static and dynamic behaviors. Standard elementary inverters ($W_N$=200nm, $W_P$=300nm and β=1.5) are used for the first and last inverters. For the central inverter, the NMOS width $W_N$=200nm is preserved while the PMOS width $W_P$ is varied from 100nm to 1000nm, corresponding to a ratio β between 0.5 and 5. Results are summarized in Figures 2.1 and 2.2, which report the variation of the logic threshold voltage $V_{TH}$ and variation of the fall-to-rise delay $t_{FR}$ of the central inverter according to the ratio β, for both RVT and LVT devices.

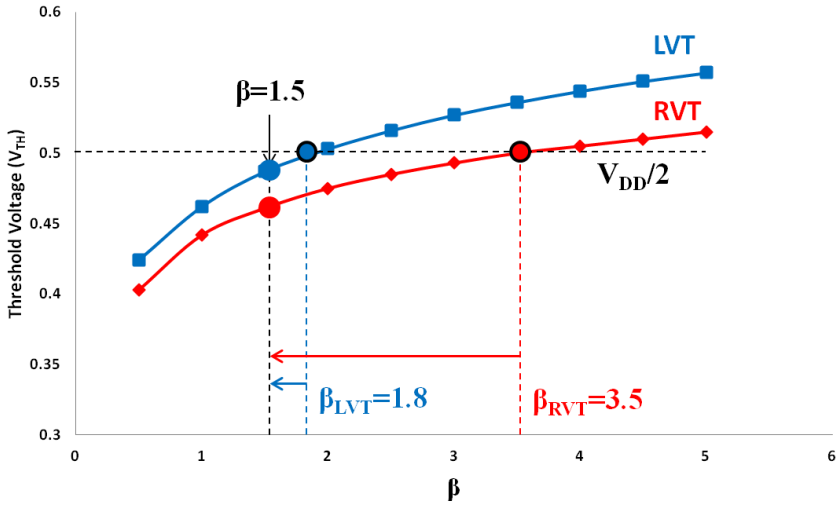



**Figure 2.1: Variation in threshold voltage as a function of β for FDSOI – RVT and LVT.**

These figures reveal that the sizing of the standard elementary inverter actually corresponds to a trade-off between gate characteristics (threshold voltage and input-to-output delay) and area. Indeed from the static point of view, the standard elementary inverter (β=1.5) does not correspond to a perfectly balanced inverter, as the threshold voltage equals 0.46V and 0.49V for RVT and LVT devices respectively. A perfectly balanced inverter with $V_{TH}=V_{DD}/2$=0.5V would require a ratio $\beta_{RVT}$=3.5 and $\beta_{LVT}$=1.8, which corresponds to a PMOS width $W_P$ of 700nm and 360nm for RVT and LVT devices respectively. Therefore, moving from a perfectly balanced inverter to the standard elementary inverter results in a significant reduction of the PMOS width while there is only a small variation of the threshold voltage i.e. 2.6% for LVT and 7.8% for

RVT. Note that the difference in the ratio required for a perfectly balanced inverter in RVT and LVT devices comes from the fact that the source-to-body voltages of the NMOS and PMOS are symmetric in RVT devices while they are asymmetric in LVT devices as explained in Chapter 1. As a result, even without body-biasing, the LVT-PMOS transistor experiences a positive source-to-body voltage which influences its driving capabilities and therefore the gate characteristics.

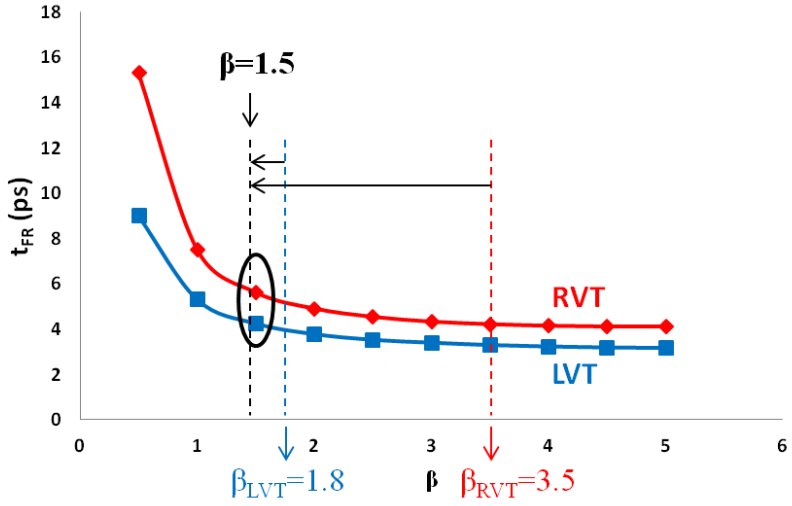



**Figure 2.2: Variation in delay as a function of β for FDSOI – RVT and LVT.**

Regarding the dynamic point of view, as shown in Figure 2.2, the gate delay decreases as the β ratio increases. However here again, moving from a perfectly balanced inverter to the standard elementary inverter permits a substantial gain in area while it induces only a minor variation of the delay. The width of PMOS $W_P$ can be reduced by a factor of 2.3 in FDSOI-RVT and 1.2 in FDSOI-LVT by marginally compromising the delay and logic threshold. Hence, it is clear that the standard elementary inverter from the FDSOI technology is designed with a major concern related to area overhead with respect to threshold voltage and speed performance. In the next subsection, we will investigate on the size of the best equivalent gate in FinFET technology.

### 2.2.2 Gate Sizing in FinFET

In case of FinFET, the width "W" depends on HFIN, TFIN and NFIN (Equations 2.1, 2.2 and 2.3). In order to give a preliminary idea of the behavior of these technologies, we have first compared the current characteristics of FDSOI-RVT and LVT transistors corresponding to the standard elementary inverter with the current

characteristics of FinFET transistors while keeping the characteristic of a Bulk transistor for reference. We have varied the number of fins in FinFET transistors to match the current driving strength with that of FDSOI transistors. For illustration, Figure 2.3 plots the drain current $I_{DS}$ versus the drain-to-source voltage $V_{DS}$ for various N-type transistors controlled with a constant $V_{GS}$=1V. In case of Bulk, FDSOI-RVT and FDSOI-LVT, transistors have a similar width of 200nm, corresponding to the NMOS width specified for the standard elementary inverter. In case of FinFET, the overall width of the transistor is an integer multiple of the minimum width $W_{min}$ depending on the number of fins NFIN. As discussed before, the minimum possible width in FinFET without taking into consideration the thickness of the fin is $W_{min}$=60nm. In order to have a transistor width comparable with Bulk and FDSOI, the possibility is to consider the number of fins either as 3 or 4, which corresponds to a total width of 180nm and 240nm respectively.

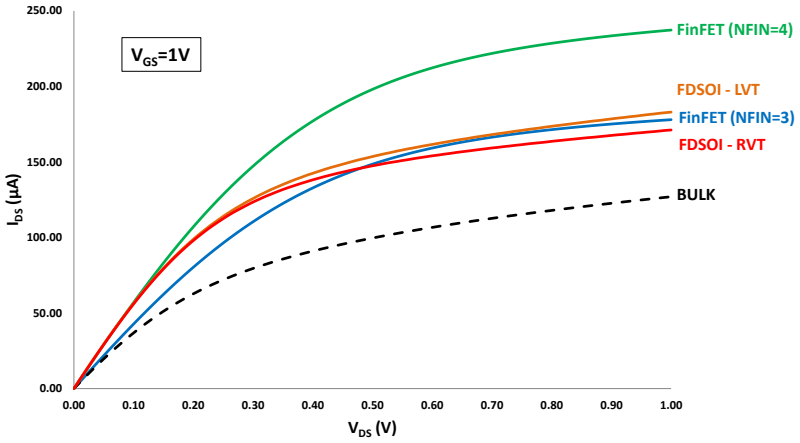



**Figure 2.3: Current characteristics of N-type transistors – Bulk, FDSOI-RVT, FDSOI-LVT, FinFET with NFIN=3 and NFIN=4.**

Analyzing the current characteristics plotted in Figure 2.3, several comments can be drawn. First, the superiority of FDSOI and FinFET technologies over the traditional Bulk technology is clearly illustrated since transistors of similar width implemented in these new technologies exhibit a significantly higher drain current for the same driving gate-to-source voltage. Obviously, this higher current drive capability will result in an improvement in the dynamic performances. Then comparing FDSOI and FinFET transistors in terms of drain current capability, we can see that the FinFET transistor with NFIN=4 has the highest current driving strength which is in agreement with its wider width as compared to transistors in FDSOI technology. The

characteristics of FDSOI-RVT, FDSOI-LVT and FinFET with NFIN=3 are very close. The FDSOI-LVT transistor has slightly higher current drive capability compared to RVT thanks to its lower value of threshold voltage. The drain current characteristic of the FinFET transistor is lower than that of FDSOI-RVT and FDSOI-LVT for low values of the drain-to-source voltage, i.e. from 0 to 0.5V, but then lies between that of FDSOI-RVT and FDSOI-LVT in case of higher values of the drain-to-source voltage. From this preliminary analysis, it seems fairly appropriate to consider N-type FinFET transistors with 3 or 4 fins to build an elementary inverter comparable to the standard elementary inverter of the FDSOI technology.

The next step is then to determine the appropriate sizing of P-type FinFET transistors in order to define an equivalent elementary inverter. To this aim, we have studied the inverter behavior, varying the number of fins of the P-type FinFET transistor. More precisely, we have considered two possible values for the number of fins of the N-type transistor, N-NFIN=3 or N-NFIN=4, as identified from the preliminary analysis. The number of fins of the P-type transistor P-NFIN has been varied from 1 to 15 in case of N-NFIN=3 and from 1 to 20 in case of N-NFIN=4, corresponding to an equivalent ratio $\beta_{FinFET}$=P-NFIN/N-NFIN between 0.25 and 5. Electrical simulations have been realized on a chain of three inverters, analyzing both the static and dynamic behavior. Results are summarized in Figures 2.4 and 2.5, which report the variation of the logic threshold voltage $V_{TH}$ and variation of the fall-to-rise delay $t_{FR}$ of the central inverter according to the ratio $\beta_{FinFET}$.

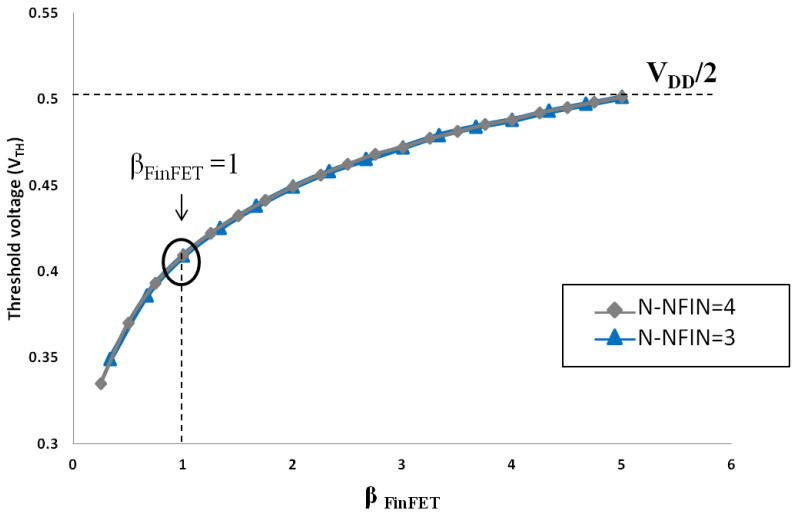



**Figure 2.4: Variation in logic threshold voltage as a function of $\beta_{FinFET}$– FinFET with N-NFIN=3 and N-NFIN=4.**

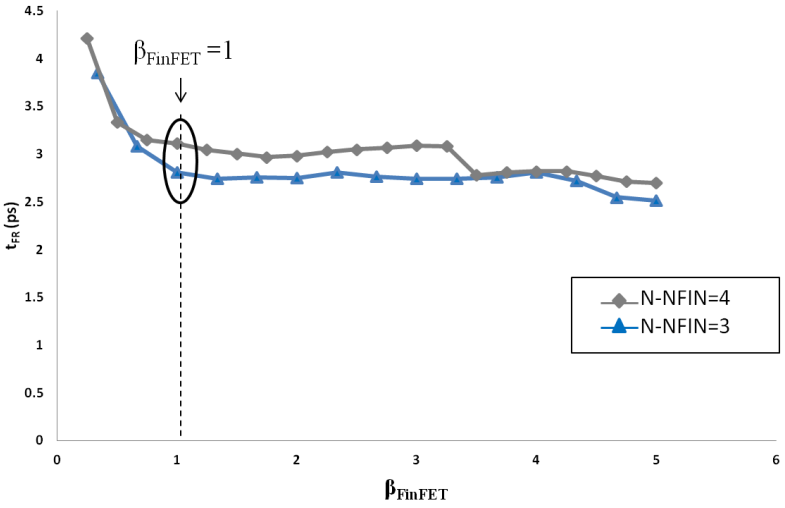



**Figure 2.5: Variation in delay as a function of $\beta_{FinFET}$– FinFET with N-NFIN=3 and N-NFIN=4.**

From these figures, it clearly appears that the variation in threshold voltage and delay exhibit similar trends than that observed in FDSOI. Regarding the threshold voltage, a high value of P-NFIN is necessary to have a logic threshold at $V_{DD}/2$, i.e. a ratio $\beta_{FinFET}$ around 5. However here again, reducing the number of fins of the P-type transistor has a moderate impact on the threshold voltage which remains above 0.4V on a large range of $\beta_{FinFET}$ values from 5 down to 1; a more significant reduction is then observed when the ratio falls below 1. In the same way regarding the dynamic behavior, the delay is almost constant on a large range of $\beta_{FinFET}$ values, from 5 down to 1, and significantly increases only if the ratio $\beta_{FinFET}$ falls below 1. So using similar design consideration as for the standard FDSOI elementary inverter, it seems fairly appropriate to adopt a ratio $\beta_{FinFET}$=1 for the design of the equivalent elementary inverter, which permits to have a substantial gain in area while marginally compromising delay and logic threshold. Note that although the inverter designed with 4 fins has higher current drive capability, it has no specific interest in terms of logic threshold and delay.

In conclusion, FinFET inverters with 3 or 4 fins for both N and P-type transistors appear as good candidates for further comparison with the standard elementary inverter of the FDSOI technology, considering a global trade-off between current characteristics, static transfer function and delay performances. In addition, such sizing of the FinFET inverter seems realistic with regard to existing publications in design [16], [19].

## 2.3 Resistive Bridging Defect Detection

Elementary inverter gate has been sized in each technology with a care of comparable electrical behavior. In order to study Resistive Bridging Defect (RBD) detection in each technology, we setup a simple didactic circuit composed of two inverter chains as shown in Figure 2.6.

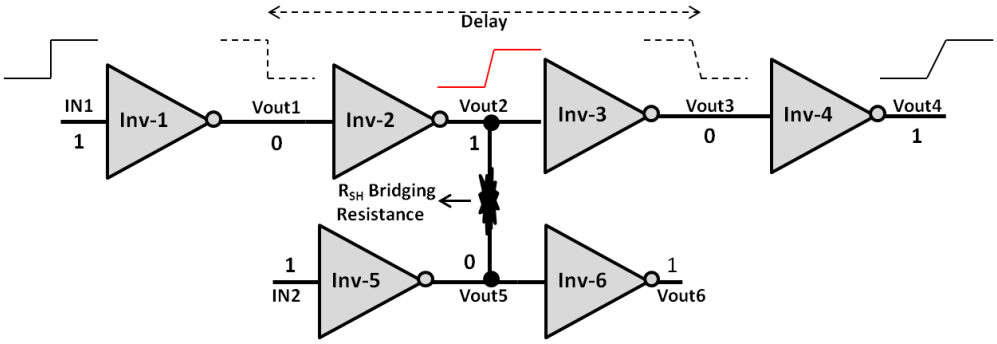


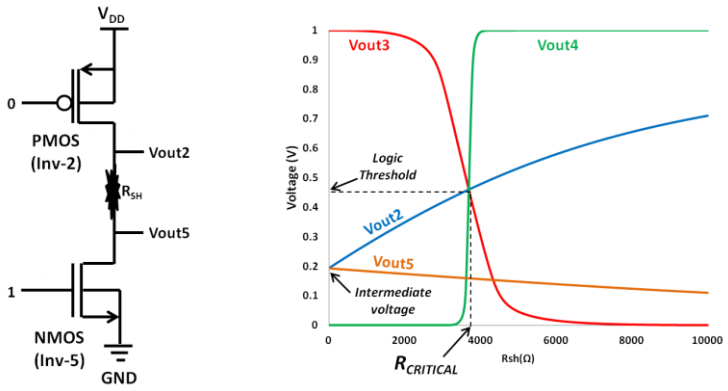

**Figure 2.6: Didactic circuit under the influence of a Resistive Bridging Defect.**

The upper chain has four inverters (INV-1 to INV-4) and it acts as the victim line. The lower chain or aggressor consists of two inverters in series (INV-5 and INV-6). The defect under study is a resistive inter-gate short defect inserted in the middle of the two chains by connecting a variable bridging resistor "$R_{SH}$" between the outputs of INV-2 (Vout2) and INV-5 (Vout5). The sensitization of the defect requires opposite logic values at the two terminals of the bridging resistor; the inputs of the upper and lower chains are therefore both set to a high logic level, which results in a high logic level at the output of INV-2 (Vout2) and a low logic level at the output of INV-5 (Vout5). When the circuit is fault-free, both the upper and the lower chains are completely independent ("$R_{SH}$" is infinite). When the resistive short value decreases, the voltage levels at the output of INV-2 and INV-5 are gradually affected, up to the point at which a downstream gate of one of the lines switches.

In the next subsections, we analyze the static and dynamic impact of this resistive bridging defect in each technology. Note that for the dynamic analysis, the high logic level applied on the input of the upper chain is replaced by a rising transition while the input of the lower chain is kept constant at high logic level.

### 2.3.1 Static Analysis

Let us analyze more in details the static behavior of the didactic circuit in presence of the resistive bridging defect. When the defect is activated, there is a conducting path established from $V_{DD}$ to ground at the location of the defect through the conducting PMOS transistor of INV-2 and the conducting NMOS transistor of INV-5 as shown in Figure 2.7 (A). The detection of the resistive bridging actually depends on the resistor divider formed by the pull-up resistance of the PMOS transistor, the short resistance "$R_{SH}$" and the pull-down resistance of the NMOS transistor.




**(A)** **(B)**

**Figure 2.7: (A) Conducting path established from $V_{DD}$ to GND at the location of the defect (B) Voltage at different nodes as a function of $R_{SH}$ for the circuit in Fig. 2.6, implemented in FDSOI – RVT without body-biasing.**

To illustrate this point, Figure 2.7 (B) plots the electrical voltage of the nodes impacted by the short defect as a function of its resistive value "$R_{SH}$" in the case of FDSOI-RVT implementation. When the value of the resistive short is null ($R_{SH}$=0), i.e. a frank short circuit between the outputs of INV-2 and INV-5, Vout2 and Vout-5 have the same value; this value is denoted as "Intermediate Voltage" and just depends on the competition between the PMOS pull-up resistance of INV-2 and the NMOS pull-down resistance of INV-5. In the case of FDSOI-RVT implementation, this intermediate voltage is equal to Vout2=Vout5=0.17V. This value is lower than the logic threshold (0.46V) for the inverter in this technology, which means that the voltage at the outputs of INV-2 and INV-5 are interpreted as a low logic level. This actually corresponds to a fault-free value for the lower inverter chain, but to a faulty value for the upper one. When $R_{SH}$ increases, Vout5 gradually decreases towards ground while Vout2 gradually increases towards $V_{DD}$. When Vout2 reaches the logic threshold of INV-3, it is then

interpreted as a high logic level and the defect is no longer detectable. The value of $R_{SH}$ at which the voltage at the output of INV-2 intersects with the logic threshold of its downstream gate is known as "Critical Resistance" or "$R_C$" [33]. In the case of FDSOI-RVT implementation, this critical resistance is equal to $R_C$=3.65kΩ. It means that a defect with a short resistance below this value can be detected by logic test, whereas a defect with a short resistance above this value is not detectable. This concept of "Critical Resistance" actually defines the detectability range of the defect. The higher the value of the critical resistance, the larger the detectability range. Note that in our didactic example, there is no value of critical resistance for the lower chain of inverters since Vout5 never intersects with the logic threshold of INV-6 and is always interpreted as a fault-free value whatever the value of the bridging resistance.

Similar study has been performed for the same circuit implemented in Bulk, FDSOI-RVT, FDSOI-LVT, 3-Fin and 4-Fin FinFETs. The noticeable values in each case, i.e. logic threshold, intermediate voltage, and critical resistance are summarized in Table 2.1.

**Table 2.1: Logic Threshold, Intermediate Voltage and Critical Resistance for the didactic circuit implemented in different technologies.**

| Technology | Bulk | FDSOI | | FinFET | |
|---|---|---|---|---|---|
| | | RVT | LVT | NFIN = 3 | NFIN=4 |
| Logic Threshold (V) | 0.52 | 0.46 | 0.49 | 0.41 | 0.41 |
| Intermediate Voltage (V) | 0.42 | 0.17 | 0.30 | 0.28 | 0.28 |
| Critical Resistance $R_C$ (kΩ) | 1.51 | 3.65 | 1.75 | 1.55 | 1.15 |

From this table, we can underline that all implemented inverters have a logic threshold relatively close to $V_{DD}/2$, i.e. 4% higher in case of Bulk, 3 % lower in case of FDSOI-LVT, 8% lower in case of FDSOI-RVT and 20% lower in case of FinFET. Regarding the intermediate voltage, we can notice that it is below $V_{DD}/2$ in all cases, which indicates a higher resistance for the PMOS pull-up transistor than for the NMOS pull-down transistor. However, its value largely differs depending on the implementation. Bulk has the highest intermediate voltage, only 16% lower than $V_{DD}/2$, indicating that conducting PMOS and NMOS transistors have an on-resistance almost in the same range. Regarding FDSOI, the situation radically changes depending on the

device type. RVT has the lowest intermediate voltage, 66% lower than $V_{DD}/2$, which corresponds to an on-resistance of the PMOS transistor more than 4 times higher than the on-resistance of the NMOS transistor. In contrast, LVT has an intermediate voltage only 40% lower than $V_{DD}/2$, which corresponds to an on-resistance of the PMOS transistor about 2 times higher than the on-resistance of the NMOS transistor. Finally for FinFET, the intermediate voltage is 45% lower than $V_{DD}/2$, which corresponds to an on-resistance of the PMOS transistor between 2 and 3 times higher than the on-resistance of the NMOS transistor.

Concerning the critical resistance, it actually depends on both the logic threshold and the intermediate voltage. Indeed, it is evident from Figure 2.7 (B) that the logic threshold should be as high as possible and the intermediate voltage as low as possible to maximize the value of the critical resistance. The essential factor is in fact the difference between these two voltages: the higher this difference, the larger the value of the critical resistance. From the results of Table 2.1, we can observe that, even if Bulk and FinFET have quite dissimilar logic threshold and intermediate voltage, the difference between these two voltages is almost in the same range between 100mV and 130mV. As a result, the critical resistance value is almost in the same range between 1.15kΩ and 1.55kΩ. Regarding FDSOI, the difference between logic threshold and intermediate voltage is marginally higher for LVT implementation, i.e. 180mV, while it reaches 290mV for RVT implementation. As a result, the critical resistance remains in the same range for LVT implementation, i.e. 1.75kΩ, while it attains 3.44kΩ for RVT implementation.

The first conclusions of this analysis are therefore: **(i) Bulk, FinFET and FDSOI-LVT have almost similar testability properties with respect to the detection of resistive short defects by a static test, and (ii) FDSOI-RVT offers a better detectability range.**

To complete this analysis, an interesting aspect to investigate for FDSOI technology is to explore how the use of the body-biasing feature impacts the value of the critical resistance. The same static analysis has therefore been performed, applying either reverse or forward body-biasing to all inverters of the didactic circuit. Note that as mentioned in Section 1.3.2 and 1.3.3 of Chapter 1, the range of reverse and forward body-biasing is different for RVT and LVT devices: $V_{BB}$=-1.8V for RBB and $V_{BB}$=0.8V for FBB in case of RVT devices, while $V_{BB}$=-0.3V for RBB and $V_{BB}$=1.8V for FBB in

case of LVT devices. Results are summarized in Tables 2.2 and 2.3, which report the logic threshold, intermediate voltage, and critical resistance for FDSOI-RVT and FDSOI-LVT under the different body-biasing conditions (RBB, NBB and FBB).

**Table 2.2: Logic Threshold, Intermediate Voltage and Critical Resistance for the didactic circuit implemented in different technologies.**

| **FDSOI – RVT** | | | |
|---|---|---|---|
| Type of BB | RBB (-1.8V) | NBB (0V) | FBB (0.8V) |
| Logic Threshold (V) | 0.47 | 0.46 | 0.46 |
| Intermediate Voltage (V) | 0.13 | 0.17 | 0.18 |
| Critical Resistance $R_C$ (kΩ) | 5.72 | 3.65 | 3.05 |

**Table 2.3: Influence of body-biasing on Logic Threshold, Intermediate Voltage and Critical Resistance – FDSOI-LVT.**

| **FDSOI – LVT** | | | |
|---|---|---|---|
| Type of BB | RBB (-0.3V) | NBB (0V) | FBB (1.8V) |
| Logic Threshold (V) | 0.49 | 0.48 | 0.46 |
| Intermediate Voltage (V) | 0.29 | 0.30 | 0.35 |
| Critical Resistance $R_C$ (kΩ) | 1.95 | 1.75 | 0.88 |

Several comments arise from the analysis of these tables. First, the principal comment is that the most favorable conditions for the detection of a resistive bridging defect are obtained using reverse body-biasing, for both RVT and LVT devices. Indeed, RBB tends to increase the logic threshold and decrease the intermediate voltage, resulting in an increased value of the critical resistance and therefore an improved detectability range. On the contrary, FBB tends to decrease the logic threshold and increase the intermediate voltage, resulting in a lower value of the critical resistance and therefore a degraded detectability range. A second comment is that the impact of RBB is more pronounced on the intermediate voltage than on the threshold voltage. In particular, it can be observed for RVT devices that the intermediate voltage is reduced by 18% when applying RBB while the threshold voltage is only increased by 1%. A similar trend with a smaller magnitude is observed for LVT devices, with a reduction of

about 3% for the intermediate voltage and an increase of less than 1% for the threshold voltage. The combination of the two effects results in a substantial increase in the value of the critical resistance, i.e. +56% for RVT and +11% for LVT. Finally, the last comment concerns the difference in the percentage increase of the critical resistance for RVT and LVT, which comes from the fact that RBB in FDSOI-LVT is limited to -0.3V while strong RBB of -1.8V can be applied in FDSOI-RVT.

To conclude this comparative analysis of the static impact of a resistive bridging defect, Figure 2.8 summarizes the value of the critical resistances obtained for the didactic circuit implemented in the different technologies, i.e. Bulk, FinFET with two different numbers of fins and FDSOI with RVT and LVT devices. The use of RBB is also considered for FDSOI since it has been identified as the most favorable condition for improving the detection of resistive bridging defects.

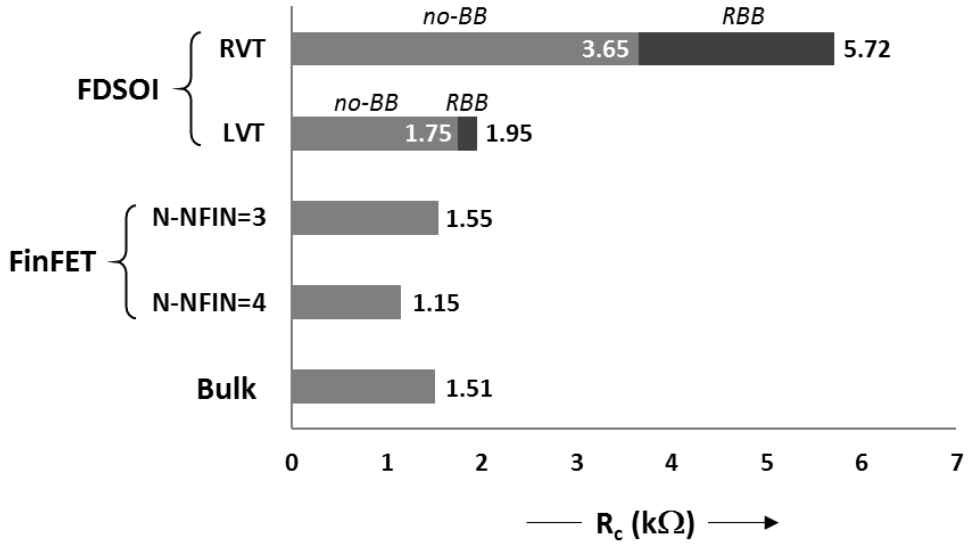



**Figure 2.8: Comparison of Static Critical Resistance for the didactic circuit implemented in different transistor technologies.**

From the testing point of view, FDSOI-RVT offers a clear advantage since it presents the largest detectability range of resistive short defects, which can be further extended by the use of reverse body-biasing. FDSOI-LVT, FinFET and Bulk have similar detectability range. Finally for the FinFET technology, it should be pointed out that there is no specific interest of using an elementary inverter with 4 fins since it presents the same threshold voltage and delay than the inverter with 3 fins but slightly lower detectability range. We will therefore keep only the elementary inverter designed with 3 fins for the dynamic analysis presented in the remaining of the chapter.

### 2.3.2 Dynamic Analysis

The same didactic circuit shown in Figure 2.6 is considered for the dynamic analysis. A fast rising transition is applied at the input of the upper chain while the input of the lower chain is kept constant to $V_{DD}$ (high logic level). The impact of the resistive bridging defect is analyzed by measuring the delay between the falling transition at the output of INV1 and the falling transition at the output of INV3, for the same circuit implemented in different technologies. The objective is to compare the relative deviation in delay induced by the defect for the different technologies.

Before investigating the impact of the resistive defect, let us first compare the performances in terms of delay for the nominal case, i.e. in the defect-free circuit. The nominal delays for each technology case are shown in Table 2.4. As expected, the Bulk technology has slower response than FDSOI and FinFET technologies. Compared to Bulk, FDSOI-RVT presents an intrinsic speed improvement of 40%, which can be further increased up to 48% using forward body-biasing. As expected, FDSOI-LVT is faster than FDSOI-RVT thanks to its lower threshold voltage, with an intrinsic speed improvement of 50%. Moreover because of its large range of forward body-biasing, the benefit of FBB is more pronounced with a speed improvement of 67% compared to Bulk. Finally regarding FinFET, its performance is in the same range than FDSOI-LVT, with a speed improvement of 60% compared to Bulk.

**Table 2.4: Nominal delay for the fault-free circuit of Fig 2.6 implemented in different technologies.**

| **Technology** | **Bulk** | **FDSOI** | | | | | | **FinFET (NFIN=3)** |
|---|---|---|---|---|---|---|---|---|
| | | RVT | | | LVT | | | |
| | | RBB | NBB | FBB | RBB | NBB | FBB | |
| Nominal Delay (ps) | 12.6 | 10.7 | 7.5 | 6.6 | 6.3 | 5.8 | 4.2 | 5.0 |

We have then performed simulations in presence of the defect, varying the value of the short defect resistance "$R_{SH}$". Results are illustrated in Figure 2.9 which shows the relative variation from the nominal delay (defect-free) as a function of the defect resistance "$R_{SH}$", for the circuit implemented in the different technologies. In case of FDSOI implementation, the impact of RBB is also highlighted; the case of FBB is

not included as it doesn't lead to any improvement in terms of detection of resistive bridging defects.

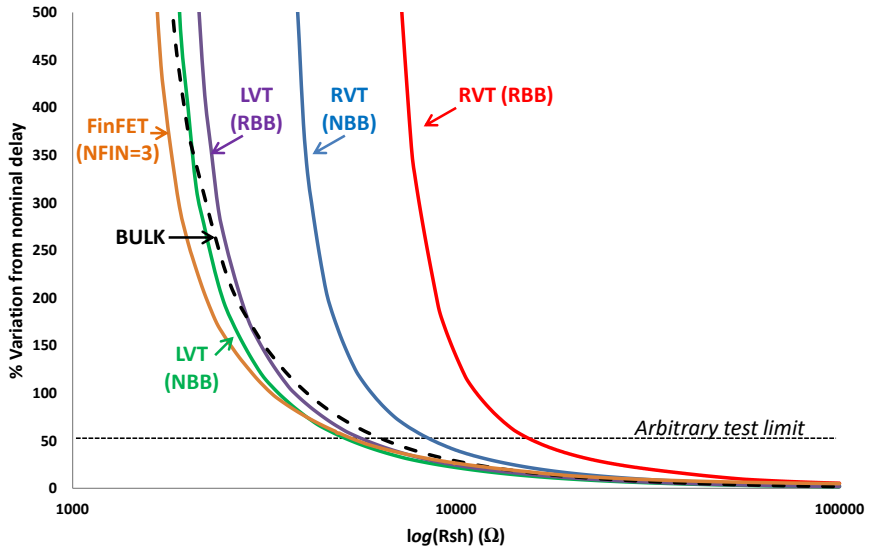



**Figure 2.9: Percentage variation from nominal delay for the fault-free circuit of Fig 2.13 implemented in different technologies.**

This figure shows that, despite the fact that the nominal delay significantly changes between Bulk and FinFET or FDSOI technologies, the impact of the defect on the relative delay variation is very similar for Bulk, FDSOI-LVT and FinFET. We can observe a noticeable difference only in case of FDSOI-RVT, with a shift in the curve towards higher values of the defect resistance corresponding to a larger detectability range. This shift is even amplified when using reverse body-biasing. These results are in complete agreement with the conclusions of the static analysis, i.e. similar detectability properties for Bulk, FinFET and FDSOI-LVT and improved detectability for FDSOI-RVT.

In the view of making a more concrete comparison basis for these different technologies, we have considered an arbitrary test limit that corresponds to 50% variation of delay from its nominal value. We have then evaluated the value of the critical resistance, denoted by "Timing Critical Resistance", corresponding to this test limit. This value gives an idea of the detectability range that can be achieved in the context of a delay-based test. Results are summarized in Table 2.5 for the didactic circuit implemented in different technologies. Here again we can observe that Bulk, FinFET and FDSOI-LVT have a Timing Critical Resistance in the same range, with a slight advantage to Bulk. FDSOI-RVT exhibits much higher detectability range with an

increase of +33% without body-biasing and +142% with reverse body-biasing in the value of the Timing Critical Resistance, compared to Bulk technology.

**Table 2.5: Timing Critical Resistance (50% variation of delay from its nominal value) for the didactic circuit implemented in different technologies.**

| Technology | Bulk | FDSOI | | | | FinFET (NFIN = 3) |
|---|---|---|---|---|---|---|
| | | RVT | | LVT | | |
| | | RBB | NBB | RBB | NBB | |
| Timing Critical Resistance $R_C$ (kΩ) | 6.5 | 15.8 | 8.7 | 5.8 | 5.3 | 5.5 |

Finally to conclude this study, Figure 2.10 compares the value of the static and timing critical resistances for the didactic circuit implemented in the different technologies. This figure shows that, as observed for the traditional Bulk technology, delay testing has also the potential to improve the detectability range of resistive short defects in FDSOI and FinFET technologies, compared to a static test.

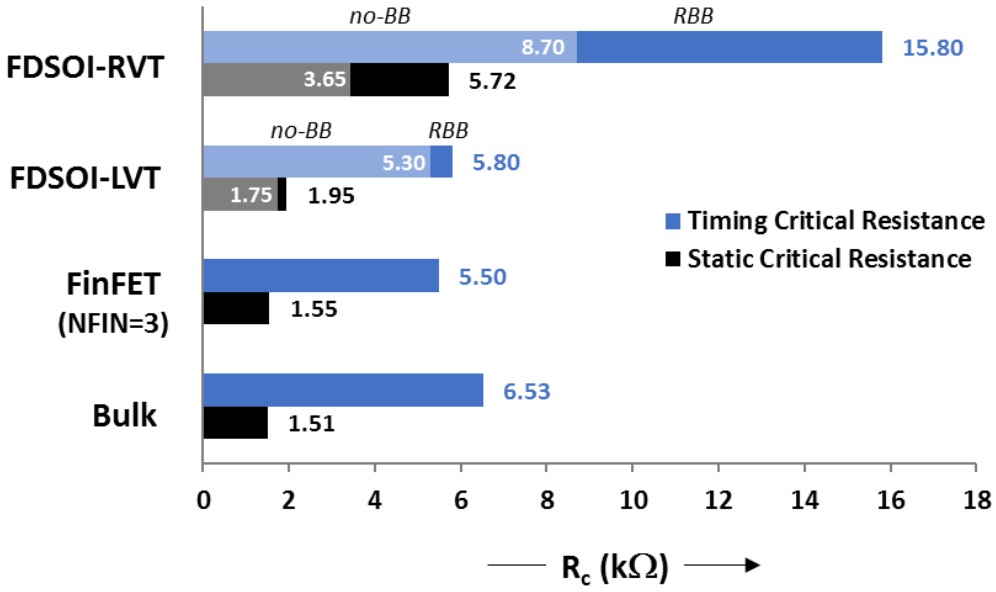



**Figure 2.10: Comparison of Static and Timing Critical Resistances for the didactic circuit implemented in different technologies (Timing Critical Resistance established considering an arbitrary test limit of 50% delay variation).**

Indeed under the assumption of an arbitrary delay test limit set at 50% variation, the critical resistance increases from 1.5kΩ to 6.5 kΩ for Bulk, which

corresponds to an enlargement of the detectability range by a factor of more than 4. In the same way, the critical resistance increases from 1.55kΩ to 5.5kΩ for FinFET and from 1.95kΩ to 5.8kΩ for FDSOI-LVT (with RBB), which corresponds to an enlargement of the detectability range by a factor of about 3. In case of FDSOI-RVT, the improvement factor is slightly lower, i.e. around 2.5, with a value of the critical resistance that increases from 3.65kΩ to 8.7kΩ without body-biasing and from 5.7kΩ to 15.8kΩ with reverse body-biasing. Yet, it should be highlighted that FDSOI-RVT has better detectability properties, and in particular when using reverse body-biasing.

## 2.4 Summary

A comparative study of Bulk, FDSOI and FinFET technologies in presence of a resistive bridging defect has been presented. To this aim, a particular care has been taken to design elementary gates and the complete circuit of study in such a way that the comparative analysis of the circuit behavior in these different technologies is meaningful. Once the experimental setup is established in the different technologies, the static and dynamic impact of an inter-gate resistive bridging defect has been analyzed using the concept of critical resistance, which determines the defect detectability range. The influence of the body-biasing feature offered by the FDSOI technology has also been explored.

Results have shown that Bulk, FinFET and FDSOI-LVT exhibit similar detectability properties, both for the static and dynamic behavior. In contrast, FDSOI-RVT offers a wider detectability range, which can be further extended by the use of reverse body-biasing. However, it should be pointed out that the knowledge of the realistic distribution of resistive short values in the different technologies is missing to draw definitive conclusions. The impact of process variations should also be considered, which is particularly essential for delay test in order to set appropriate test limit. These aspects will be tackled for 28nm Bulk and FDSOI technologies in the following chapters together with the consideration of other classical defects such as short-to-GND, short-to-$V_{DD}$ and resistive opens. Our investigations in the following chapters will be limited to only 28nm FDSOI and Bulk transistor technologies due to the unavailability of an "industrial" model for FinFET technology.

# 3 Influence of Body-Biasing, Supply Voltage and Temperature on the detection of resistive short defects in FDSOI technology

# 3.1 INTRODUCTION

The susceptibility to resistive short defects due to high packaging densities [4] along with the increasing short-channel effects has completely restricted the scaling down of transistor size feature. In order to overcome these issues, technologies featuring fully depleted transistors are entering the mainstream for designs at the 28nm technology node and following ones. FDSOI is a new innovation in silicon process technology and is poised to replace today's MOSFET, providing a much needed relief to IC's from their power and device variation predicaments [72], [73]. Resistive short defects represent a major class of manufacturing defects that can pose a serious reliability risk for nanoscale CMOS technologies. Detectability of short defects has been widely studied in traditional Bulk technology, based on the concept of critical resistance used both in the context of logic test [33], [34] and delay test [74]. The influence of supply voltage and temperature has been investigated [75], as well as the utilization of body-biasing [76] and the impact of PVT (Process, Voltage and Temperature) variations [77]. However, there are only limited studies regarding the detection of resistive short defects in FDSOI technology. A comparative analysis of Bulk, FDSOI and FinFET technologies in presence of an inter-gate resistive bridging defect is performed in [78], limited to nominal supply voltage and temperature conditions.

The objective of this chapter is to presents an in-depth analysis of the impact of body-biasing, supply voltage and temperature on the detection of resistive short defects in FDSOI technology. Three types of short defects are considered for our investigation, namely resistive short to ground terminal (GND), resistive short to power supply terminal ($V_{DD}$) and inter-gate resistive bridging defect. The two implementation options offered by the technology, i.e. Low $V_T$ (LVT) and Regular $V_T$ (RVT) devices are also studied. Defect detectability is evaluated in the context of logic test using the concept of critical resistance. The optimal body-biasing, supply voltage and temperature settings to achieve the maximum defect coverage are determined through HSPICE simulations using a didactic circuit implemented with 28nm UTBB FDSOI gate library. An analytical analysis is also proposed based on the ON-resistance model of P and N networks, which permits to evaluate the value of the critical resistance without performing defect simulations. In addition, this work quantifies the individual as well as

the combined improvements in detection brought by body-biasing, supply voltage and temperature settings for the different defect types and different implementations.

The chapter is organized as follows: Section 3.2 focuses on the circuit under test while Section 3.3 describes the analytical study of the critical resistance. Section 3.4 presents the simulation result regarding defect detectability under various operating conditions and the impact of body-biasing on a broader aspect is shown in Section 3.5. Some conclusions and perspectives are drawn in Section 3.6.

## 3.2 CIRCUIT UNDER TEST

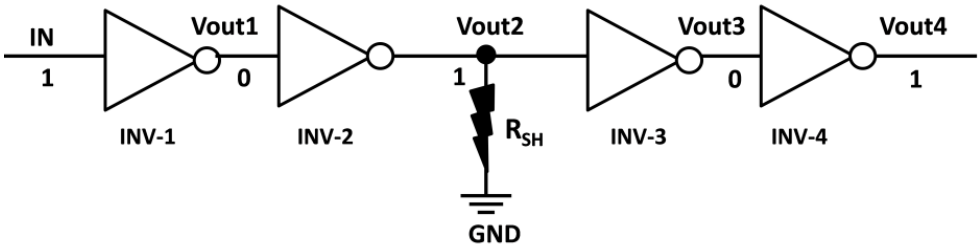
To infer on the comparative study of FDSOI-LVT and FDSOI-RVT devices, simple didactic circuits are implemented in a 28nm UTBB FDSOI technology using standard elementary inverters from the gate library. Electrical simulations are performed using HSPICE. The following three cases are taken into consideration for the study of three different defect types.

### 3.2.1 Resistive short to Ground Terminal (GND)

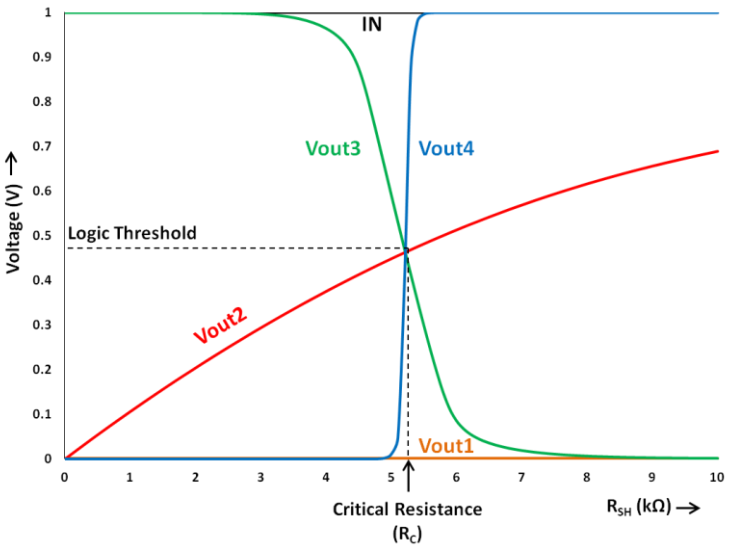
The didactic circuit taken into consideration to perform the study of resistive short to ground terminal is a simple chain of four identical inverters (INV-1 to INV-4). As illustrated in Figure 3.1 (A), the short defect is inserted in the middle of the chain by connecting a variable short resistor $R_{SH}$ between the output of INV-2 (Vout2) and the ground terminal (GND).

A high logic level is applied on the inverter chain input (IN) to sensitize the defect. When the circuit is fault-free, the voltage at the output of INV-2 corresponds to a high logic level. However in presence of the defect, a conducting path is created between $V_{DD}$ and GND through the conducting PMOS transistor of INV-2 and the short resistor $R_{SH}$. In case of a frank short circuit ($R_{SH}$=0), the voltage Vout2 is directly tied to ground; this voltage is obviously interpreted as a low logic level by the following gate (INV-3), which corresponds to a faulty value. As the short resistance $R_{SH}$ increases, the voltage Vout2 gradually increases towards $V_{DD}$. When Vout2 reaches the logic threshold of INV-3, it is interpreted as a high logic level (fault-free value) and the defect is no longer detectable. The maximum value of $R_{SH}$ for which the voltage Vout2 is

interpreted as a low logic level is known as the "Critical Resistance" or $R_C$, as shown in the $R_{SH}$ - V characteristic in Figure 3.1 (B). It means that a defect with a short resistance below this value can be detected by logic test, whereas a defect with a short resistance above this value is non-detectable.




**(A)**



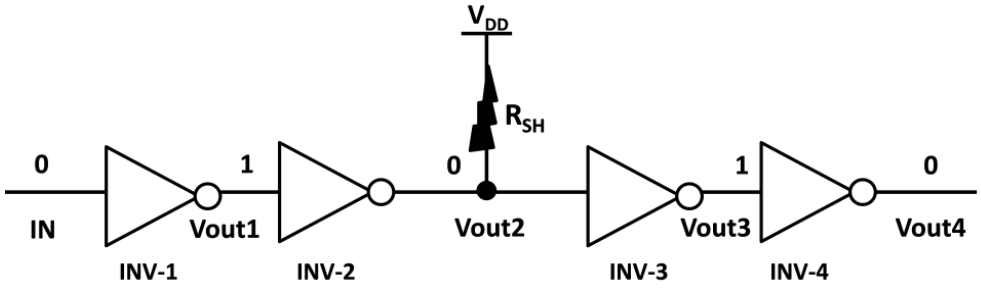

**(B)**

**Figure 3.1: (A) Circuit under test for resistive short-to-GND (B) Voltage at different nodes as a function of $R_{SH}$.**

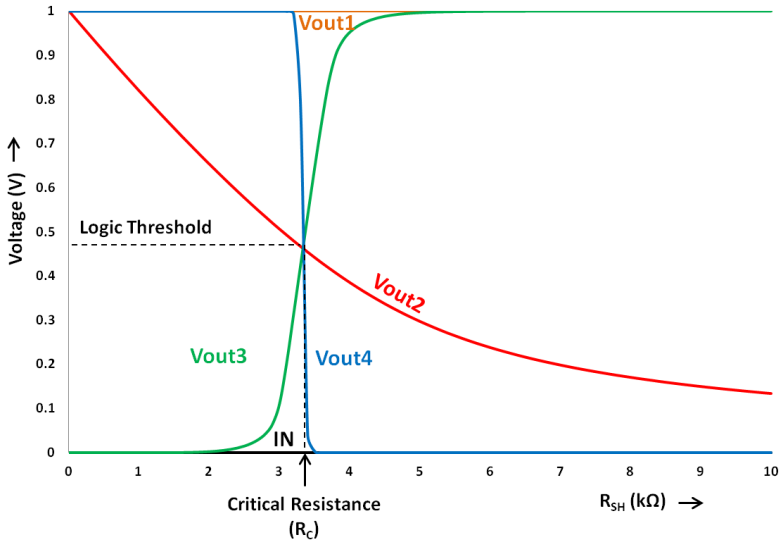
### 3.2.2 Resistive short to Power Supply ($V_{DD}$)

The study of resistive short to power supply is performed with the same didactic circuit composed of four identical inverters (INV-1 to INV-4). As shown in Figure 3.2 (A), the defect is inserted in the middle of the chain by connecting a variable short resistor $R_{SH}$ between the output of INV-2 (Vout2) and the supply voltage terminal ($V_{DD}$); a low logic level is applied on the input (IN) to sensitize the defect. The presence of the defect creates a conducting path between $V_{DD}$ and GND, this time through the short resistor $R_{SH}$ and the conducting NMOS transistor of INV-2. In case of a frank

short circuit, the voltage Vout2 is directly tied to $V_{DD}$ and then gradually decreases towards ground as the short resistance increases. The maximum value of $R_{SH}$ for which the voltage Vout2 is interpreted as a faulty value (i.e. a high logic level) defines the "Critical Resistance" or $R_C$, as shown in the $R_{SH}$ - V characteristic in Figure 3.2 (B).




**(A)**




**(B)**

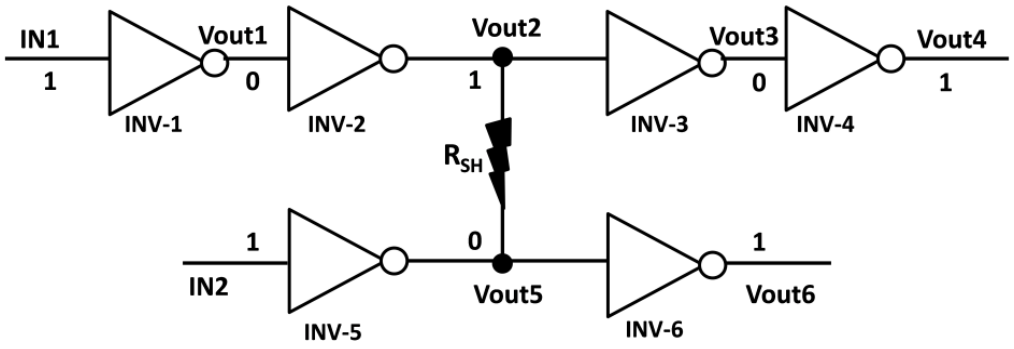
**Figure 3.2: (A) Circuit under test for resistive short-to-$V_{DD}$ (B) Voltage at different nodes as a function of $R_{SH}$.**

### 3.2.3 Inter-Gate Resistive Bridging Defect

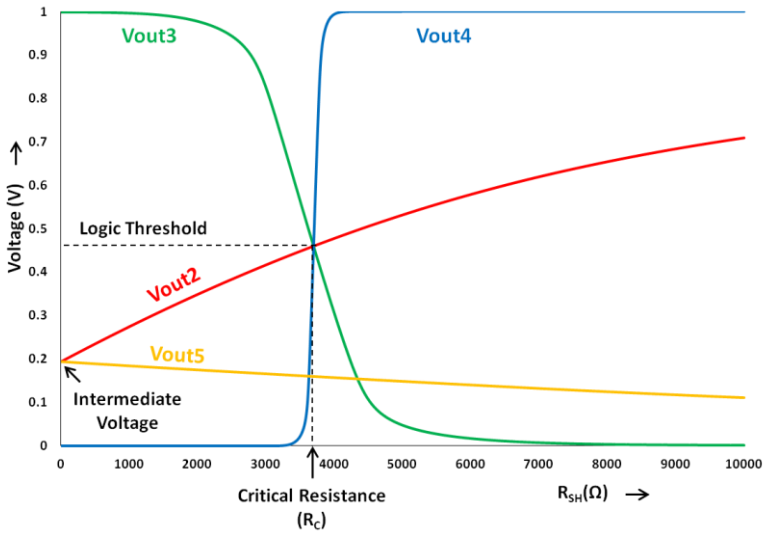
As explained in Chapter 2, in order to evaluate the impact of a resistive bridging defect, two chains of inverters are taken into consideration as shown in Figure 3.3 (A). The upper chain or the victim line consists of a series of four identical inverters (INV-1 to INV-4) while the lower chain or aggressor consists of two identical inverters (INV-5 and INV-6). The defect is inserted in the middle of the two chains by

connecting a variable bridge resistor $R_{SH}$ between the outputs of INV-2 (Vout2) and INV-5 (Vout5).

The sensitization of the defect requires opposite logic values at the two terminals of the bridge resistor; the inputs of the upper and lower chains are therefore both set to a high logic level. When the circuit is fault-free ($R_{SH}=\infty$), both the upper and the lower chain are independent of each other which results in a high logic level at the output of INV-2 (Vout2) and a low logic level at the output of INV-5 (Vout5).




**(A)**




**(B)**

**Figure 3.3: (A) Circuit under test for inter-gate resistive bridging short (B) Voltage at different nodes as a function of $R_{SH}$.**

In presence of the defect, there exists a connection between both chains and a conducting path from $V_{DD}$ to GND is established at the location of the defect through the conducting PMOS transistor of INV-2 and the conducting NMOS transistor of INV-5. When the short resistance is null ($R_{SH}=0$), Vout2 and Vout5 have the same value; this

value is denoted by Intermediate Voltage ($V_i$) and just depends on the competition between the PMOS pull-up resistance of INV-2 and the NMOS pull-down resistance of INV-5. In the didactic circuit under study, this value is relatively low ($V_i$=0.17V for RVT and $V_i$=0.3V for LVT), and more specifically below the logic threshold of the standard elementary inverter ($V_{TH}$=0.46V for RVT and $V_{TH}$=0.49V for LVT). The voltage at the output of INV-2 and INV-5 is therefore interpreted as a low logic level by the downstream gates, which corresponds to a fault-free value for the lower inverter chain, but to a faulty value for the upper one. When $R_{SH}$ increases, Vout5 gradually decreases towards ground while Vout2 gradually increase towards $V_{DD}$. When Vout2 reaches the logic threshold of INV-3, it is interpreted as a high logic level and the defect is no longer detectable. The "Critical Resistance" or $R_C$ therefore corresponds to the value of $R_{SH}$ at which the voltage at the output of INV2 intersects with the logic threshold of its downstream gate as shown in Figure 3.3 (B). Note that in our didactic example, there is no value of critical resistance for the lower chain of inverters since Vout5 never intersects with the logic threshold of INV-6 and is always interpreted as a fault-free value whatever the value of the short resistance.

## 3.3 Analytical Analysis

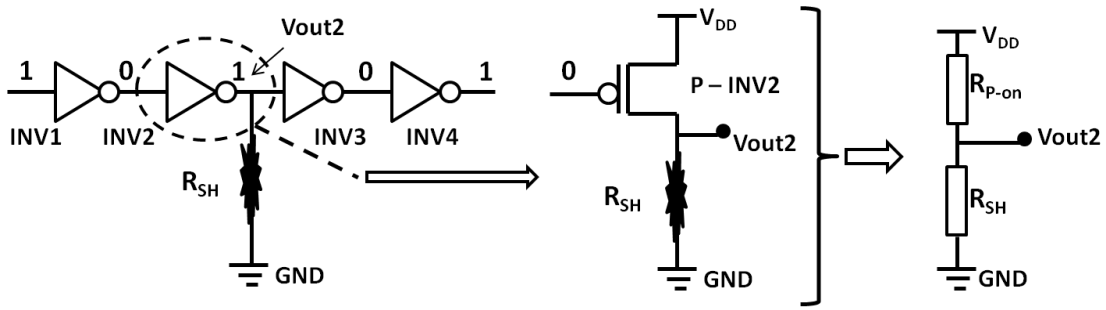
An analytical analysis is carried out in order to define a simple model for the value of the critical resistance. This analysis is based on the fact that the presence of the defect establishes an unintentional conducting path between $V_{DD}$ and GND; simple voltage relations can then be expressed by replacing conducting P or N-transistor networks by their corresponding ON-resistance model.

In case of a resistive short-to-GND as shown in Figure 3.4 (A), the inverter gate INV-2 is driven by a low logic level, which means that its P-network establishes a connection to $V_{DD}$ while its N-network is disabled. The circuit can be thus reduced to a conducting path created from $V_{DD}$ to GND through a P-network and the short resistance $R_{SH}$ as shown in Figure 3.4 (B). The involved P-transistor of INV-2 can also be represented in terms of its equivalent ON-resistance, $R_{P\text{-}on}$ as shown in Figure 3.4 (C). This forms a resistive divider and the voltage Vout2 can be simply expressed as shown in Equation 3.1.

$$Vout2 = \frac{R_{SH} \, . V_{DD}}{(R_{SH} + R_{P-on})} \qquad 3.1$$

As discussed in the previous section, the critical resistance $R_C$ corresponds to the value of the short resistance $R_{SH}$ when the voltage Vout2 at the output of the INV-2 is equal to the logic threshold $V_{TH}$ of INV-3. The expression of the critical resistance $R_C$ can therefore be derived from Equation 3.1 using Vout2 = $V_{TH}$ when $R_{SH} = R_C$:

$$R_C = \frac{R_{P-on}}{(\frac{V_{DD}}{V_{TH}} - 1)} \qquad 3.2$$




**(A)** **(B)** **(C)**

**Figure 3.4: (A) Circuit under test for resistive short-to-GND (B) Conducting path from $V_{DD}$ to GND through $R_{SH}$ (C) Voltage divider using ON -resistance model of P-network.**

This expression reveals that the critical resistance associated with a short-to-GND defect mainly depends on the ON-resistance of the P-transistor ($R_{P\text{-}on}$) of the driving gate at the location of the defect and on the ratio between the supply voltage ($V_{DD}$) and the logic threshold of the driven gate ($V_{TH}$).

In the same way, we can derive a simple expression of the critical resistance associated with a short-to-$V_{DD}$ defect. In this case, the conducting path created by the presence of the defect is established through the N-transistor of INV-2 as illustrated in Figure 3.5. The voltage Vout2 can therefore be expressed by:

$$Vout2 = \frac{R_{N-on} \, . V_{DD}}{(R_{SH} + R_{N-0n})} \qquad 3.3$$

where $R_{N\text{-}on}$ corresponds to the equivalent ON-resistance of the N-network.

The expression of the critical resistance $R_C$ is then derived from this equation by replacing Vout2 by the downstream gate logic threshold $V_{TH}$ when $R_{SH} = R_C$

$$R_C = R_{N-on} \cdot \left(\frac{V_{DD}}{V_{TH}} - 1\right) \quad 3.4$$

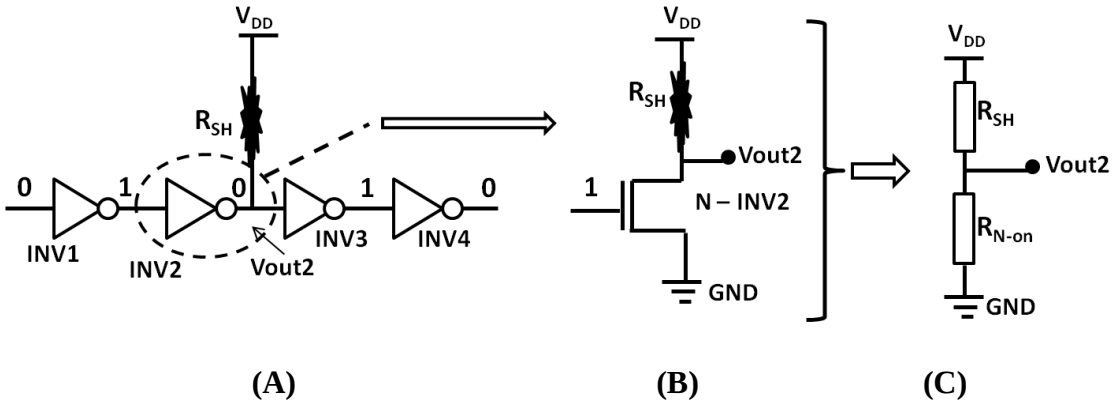


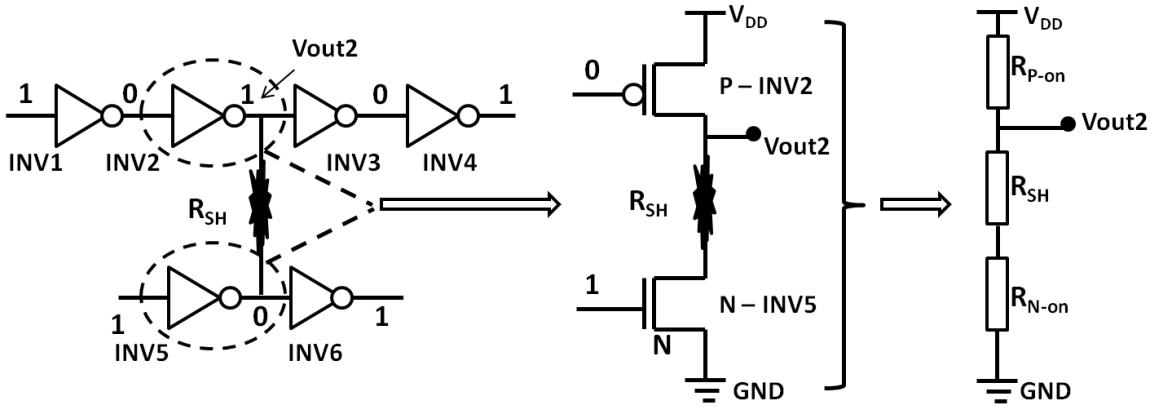

**Figure 3.5: (A) Circuit under test for resistive short-to-$V_{DD}$ (B) Conducting path from $V_{DD}$ to GND through $R_{SH}$ (C) Voltage divider using ON-resistance model of N-network.**

Finally, the same analysis can be applied for an inter-gate resistive bridging defect. In this case, the P-network of INV-2 establishes a connection to $V_{DD}$ while its N-network is disabled; the N-network of INV-5 establishes a connection to GND while its P-network is disabled. The conducting path created by the presence of the defect therefore involves both the P and N-networks of inverters INV2 and INV-5, as shown in Figure 3.6. The voltage Vout2 at the output of INV-2 can be expressed by:

$$Vout2 = \frac{(R_{SH} + R_{N-on}).V_{DD}}{(R_{P-on} + R_{SH} + R_{N-on})} \quad 3.5$$

and the expression of the critical resistance $R_C$ is obtained by replacing Vout2 by the gate logic threshold $V_{TH}$:

$$R_C = \frac{R_{P-on}}{\left(\frac{V_{DD}}{V_{TH}} - 1\right)} - R_{N-on} \quad 3.6$$




**(A)** **(B)** **(C)**

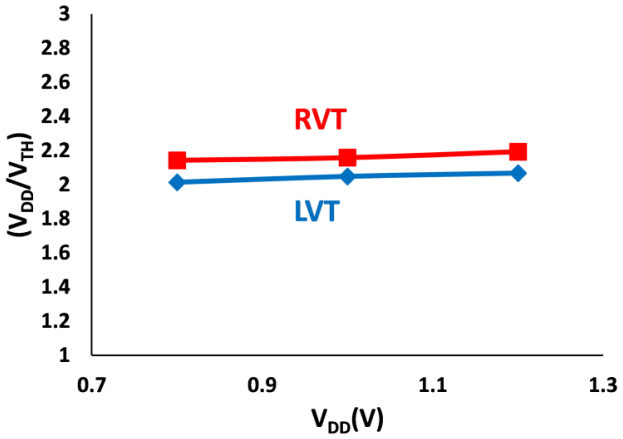
**Figure 3.6: (A) Circuit under test for inter-gate resistive bridging defect (B) Conducting path from $V_{DD}$ to GND through $R_{SH}$ (C) Voltage divider using ON-resistance model of P and N-networks.**

This simple analysis indicates that, whatever the short defect type, the critical resistance depends, on the one hand, on the ON-resistance of the transistors involved in the conducting path and on the other hand, on the ratio $V_{DD}/V_{TH}$ between the supply voltage and the gate logic threshold.

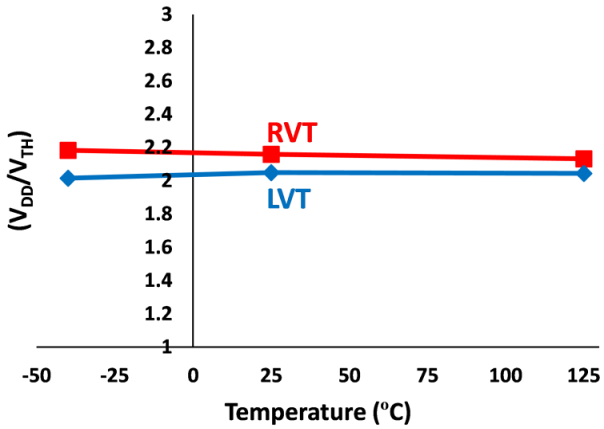
This is an interesting point because, although it is clear that the logic threshold voltage $V_{TH}$ is impacted by the operating conditions, the ratio $V_{DD}/V_{TH}$ remains almost constant with respect to variations of $V_{DD,}$ temperature and body-biasing as shown in Figure 3.7 (A), (B) and (C) respectively. It can be thus deduced that the major impact on the critical resistance $R_C$ will be brought by the variations of the ON-resistance of involved P and N networks under the different operating conditions of $V_{DD}$, temperature and body-biasing.

A more generalized expression can be given by considering the ratio $V_{DD}/V_{TH}$ as a constant α and defining β as shown in Equation 3.7.

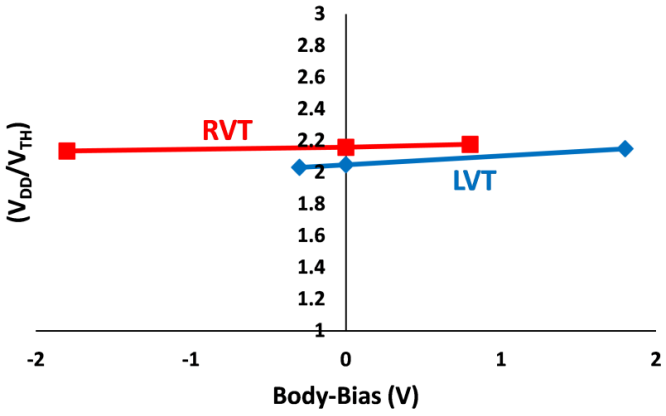
$$\beta = \frac{1}{(\frac{V_{DD}}{V_{TH}} - 1)} = \frac{1}{(\alpha - 1)} \qquad 3.7$$




**(A)**




**(B)**




**(C)**

**Figure 3.7: Simulated variations of $V_{DD}/V_{TH}$ as a function of (A) $V_{DD}$, (B) Temperature and (C) Body-biasing, for both RVT and LVT implementations.**

The critical resistance associated with resistive short-to-GND, resistive short-to-$V_{DD}$ and inter-gate resistive bridging defect can then be expressed as shown in Table 3.1, with β a constant that only depends on the implementation type (i.e. RVT or LVT configuration). The value of β can be simply determined from simulation under nominal conditions ($V_{DD}$ = 1V, Temp = 25ºC and No Body-Biasing). It comes out to be 0.8622 and 0.9531 for RVT and LVT devices respectively, so slightly lower for RVT.

**Table 3.1: Analytical expression of the critical resistance for the different types of short defect.**

| Defect Type | Expression of Critical Resistance |
|---|---|
| Resistive short-to-GND | $R_C = \beta.R_{P\text{-}on}$ |
| Resistive short-to-$V_{DD}$ | $R_C = R_{N\text{-}on} / \beta$ |
| Inter-gate resistive bridging defect | $R_C = \beta.R_{P\text{-}on} - R_{N\text{-}on}$ |

To evaluate the inaccuracy introduced by the assumption of a constant β, we have compared the value of $V_{TH}$ determined by simulation under different power supply voltages to the value of $V_{TH}$ computed with:

$$V_{TH} = \frac{V_{DD}.\beta}{(1+\beta)} \qquad 3.8$$

where β is the constant value determined under nominal conditions.

**Table 3.2: Simulated vs. computed values of $V_{TH}$ for different supply voltage values $V_{DD}$, for both RVT and LVT configurations.**

| $V_{DD}$ (V) | $V_{TH}$ (mV) | | | |
|---|---|---|---|---|
| | RVT | | LVT | |
| | Simulated | Computed (β=0.8622) | Simulated | Computed (β=0.9531) |
| 0.8 | 373 | 370 | 397 | 390 |
| 1 | 463 | 463 | 488 | 488 |
| 1.2 | 547 | 556 | 580 | 586 |

Results are summarized in Table 3.2, both for RVT and LVT implementations. A very good agreement can be observed between computed values and exact values derived from simulation, with a maximum error lower than 2%. A further exploration of the operational conditions varying altogether $V_{DD}$ from 0.8V to 1.2V, the temperature from -40°C to 125°C and body-biasing within the possible range of the corresponding implementation leads to a maximal error of 4.12% for RVT and 4.95% for LVT. Obviously, the assumption that the factor β is almost constant is reasonable, its actual variations under the combined effects of $V_{DD}$, temperature and body-biasing being inferior to 5%.

From this analysis, it can be deduced that the critical resistance $R_C$ actually just depends on the ON-resistance of the involved P and N networks. This is an important point because it means that, independently of the resistive short defect, the value of the critical resistance can be evaluated without performing any fault simulation. Indeed, it is sufficient to know the value of the ON-resistance for the different gates of the library, under the various operating conditions. This can be accomplished with a pre-characterization of the gate library using the electrical setup shown in Figure 3.8.

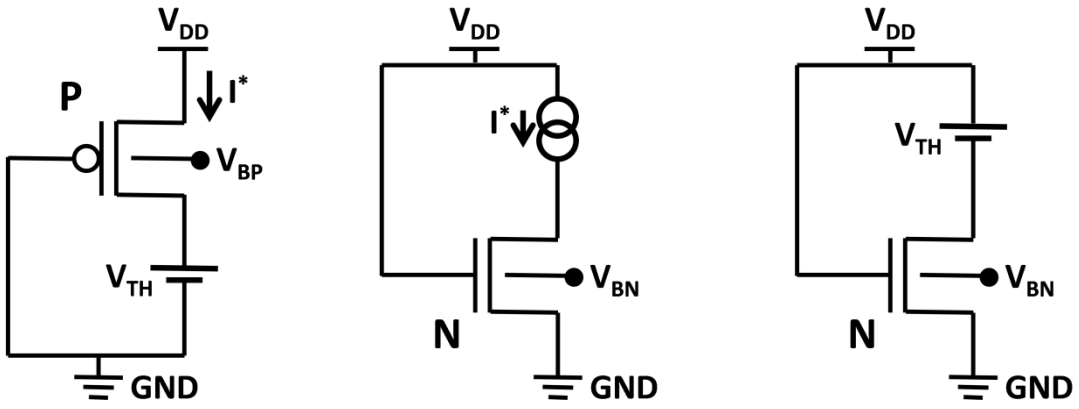



**Figure 3.8: Electrical setup to evaluate (A) $R_{P\text{-}on}$ for short-to-GND and inter-gate bridging defect, (B) $R_{N\text{-}on}$ for inter-gate bridging defect, (C) $R_{N\text{-}on}$ for short-to-$V_{DD}$.**

Figure 3.8 (A) shows a P-type transistor with its gate connected to GND, its source connected to $V_{DD}$ and its drain connected to a constant voltage source $V_{TH}$, where the value of $V_{TH}$ is considered from the computed values in Table 3.2. This transistor operates in the same conditions as the P-transistor involved in the conducting path in case of a short-to-GND (cf. Figure 3.4) or an inter-gate bridging defect (cf.

Figure 3.6). Indeed, the transistor is controlled by a low logic level and the constant voltage source $V_{TH}$ corresponds to the situation where the defect resistance is equal to the critical resistance $R_{SH}=R_C$. The ON-resistance can then be simply determined as the ratio between the drain-to-source voltage and the current flowing through the transistor with $R_{P\text{-}on}=V_{DS}/I_{DS}$. Note that the current flowing through the transistor is recorded as I* and will be used to determine the ON-resistance of the N-transistor involved in the conducting path in case of an inter-gate bridging defect.

More precisely, Figure 3.8 (B) shows the corresponding electrical setup that comprises the N-transistor with its gate connected to $V_{DD}$, its source connected to GND and its drain connected to the constant current source I*. Here again the ON-resistance is determined as the ratio between the drain-to-source voltage and the current flowing through the transistor $R_{N\text{-}on}=V_{DS}/I_{DS}$.

Finally, the ON-resistance of the N-transistor involved in the conducting path in case of a short-to-$V_{DD}$ (cf. Figure 3.5) is determined using the electrical setup shown in Figure 3.8 (C). This setup is the symmetric of the short-to-GND case, with the gate of the N-transistor controlled by a high logic level, the source connected to GND and the drain connected to the constant voltage source $V_{TH}$.

Based on this experimental setup, we have performed the characterization of the standard elementary inverter considering three different supply voltage values corresponding to Nom-$V_{DD}$=1V, Low-$V_{DD}$=0.8V and High-$V_{DD}$=1.2V, three different temperature values corresponding to Nom-T=25°C, Low-T=-40°C and High-T=125°C and three different conditions of body-biasing corresponding to No-Body-Biasing (NBB), Reverse-Body-Biasing (RBB) and Forward-Body-Biasing (FBB). This characterization has been done for both types of implementation, i.e. RVT and LVT devices. Note that as mentioned in Chapter 1, the range of reverse and forward body biasing is different for RVT and LVT devices: $V_{BB}$=-1.8V for RBB and $V_{BB}$=0.8V for FBB in case of RVT devices, while $V_{BB}$=-0.3V for RBB and $V_{BB}$=1.8V for FBB in case of LVT devices. Also note that the ON-resistance of the P-transistor determined in case of a short-to-GND is the same as the one determined in case of an inter-gate bridging defect as shown in Table 3.3 and 3.4, while the ON-resistance of the N-transistor determined in case of a short-to-$V_{DD}$ (as shown in Table 3.5 and 3.6) differs from the one determined in case of an inter-gate bridging defect (as shown in Table 3.7 and 3.8).

Such a pre-characterization can be achieved in a reasonable simulation time with standard computing equipment (in the order of some minutes of computation).

**Table 3.3: Variations of $R_{P\text{-}on}$ as a function of Body-Biasing and Temperature at different $V_{DD}$ for FDSOI-RVT under the influence of resistive short-to-GND and inter-gate bridging defect.**

| RVT | $R_{P\text{-}on}$ (kΩ) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$=0.8V | | | $V_{DD}$=1V | | | $V_{DD}$=1.2V | | |
| TEMP (°C) | -40 | 25 | 125 | -40 | 25 | 125 | -40 | 25 | 125 |
| RBB=-1.8V | 28.4 | 19.4 | 12.9 | 9.7 | 8.5 | 7.4 | 6.1 | 5.7 | 5.4 |
| NBB=0 | 12.5 | 10 | 7.8 | 6.8 | 6.0 | 5.4 | 5.2 | 4.7 | 4.5 |
| FBB=+0.8V | 9.6 | 7.9 | 6.5 | 6.0 | 5.3 | 4.9 | 5.1 | 4.4 | 4.1 |

**Table 3.4: Variations of $R_{P\text{-}on}$ as a function of Body-Biasing and Temperature at different $V_{DD}$ for FDSOI-LVT under the influence of resistive short-to-GND and inter-gate bridging defect.**

| LVT | $R_{P\text{-}on}$ (kΩ) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$=0.8V | | | $V_{DD}$=1V | | | $V_{DD}$=1.2V | | |
| TEMP (°C) | -40 | 25 | 125 | -40 | 25 | 125 | -40 | 25 | 125 |
| RBB=-0.3V | 6.6 | 6.5 | 6.1 | 3.9 | 4.0 | 4.0 | 3.0 | 3.1 | 3.2 |
| NBB=0 | 6.0 | 5.9 | 5.7 | 3.7 | 3.8 | 3.8 | 2.9 | 2.9 | 3.0 |
| FBB=+1.8V | 3.8 | 3.8 | 3.7 | 2.7 | 2.8 | 2.9 | 2.3 | 2.3 | 2.5 |

**Table 3.5: Variations of $R_{N\text{-}on}$ as a function of Body-Biasing and Temperature at different $V_{DD}$ for FDSOI-RVT under the influence of resistive short-to-$V_{DD}$ defect.**

| RVT | $R_{N\text{-}on}$ (kΩ) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$=0.8V | | | $V_{DD}$=1V | | | $V_{DD}$=1.2V | | |
| TEMP (°C) | -40 | 25 | 125 | -40 | 25 | 125 | -40 | 25 | 125 |
| RBB=-1.8V | 6.2 | 6.1 | 5.7 | 3.3 | 3.6 | 3.8 | 2.8 | 3.0 | 3.2 |
| NBB=0 | 3.8 | 3.9 | 4.0 | 2.7 | 2.8 | 3.0 | 2.3 | 2.4 | 2.6 |
| FBB=+0.8V | 3.3 | 3.4 | 3.5 | 2.5 | 2.6 | 2.8 | 2.2 | 2.3 | 2.4 |

**Table 3.6: Variations of $R_{N\text{-}on}$ as a function of Body-Biasing and Temperature at different $V_{DD}$ for FDSOI-LVT under the influence of resistive short-to-$V_{DD}$ defect.**

| LVT | $R_{N\text{-}on}$ (kΩ) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$=0.8V | | | $V_{DD}$=1V | | | $V_{DD}$=1.2V | | |
| TEMP (°C) | -40 | 25 | 125 | -40 | 25 | 125 | -40 | 25 | 125 |
| RBB=-0.3V | 4.1 | 4.2 | 4.6 | 2.8 | 3.0 | 3.2 | 2.4 | 2.5 | 2.7 |
| NBB=0 | 3.8 | 3.9 | 4.2 | 2.7 | 2.8 | 3.1 | 2.3 | 2.4 | 2.6 |
| FBB=+1.8V | 2.5 | 2.6 | 2.9 | 2.1 | 2.2 | 2.3 | 2.0 | 2.0 | 2.1 |

**Table 3.7: Variations of $R_{N\text{-}on}$ as a function of Body-Biasing and Temperature at different $V_{DD}$ for FDSOI-RVT under the influence of inter-gate bridging defect.**

| RVT | $R_{N\text{-}on}$ (kΩ) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$=0.8V | | | $V_{DD}$=1V | | | $V_{DD}$=1.2V | | |
| TEMP (°C) | -40 | 25 | 125 | -40 | 25 | 125 | -40 | 25 | 125 |
| RBB=-1.8V | 2.5 | 2.6 | 2.8 | 1.5 | 1.7 | 2.0 | 1.2 | 1.4 | 1.7 |
| NBB=0 | 1.8 | 2.0 | 2.3 | 1.3 | 1.5 | 1.8 | 1.1 | 1.3 | 1.6 |
| FBB=+0.8V | 1.7 | 1.9 | 2.1 | 1.3 | 1.5 | 1.7 | 1.1 | 1.3 | 1.5 |

**Table 3.8: Variations of $R_{N\text{-}on}$ as a function of Body-Biasing and Temperature at different $V_{DD}$ for FDSOI-LVT under the influence of inter-gate bridging defect.**

| LVT | $R_{N\text{-}on}$ (kΩ) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$=0.8V | | | $V_{DD}$=1V | | | $V_{DD}$=1.2V | | |
| TEMP (°C) | -40 | 25 | 125 | -40 | 25 | 125 | -40 | 25 | 125 |
| RBB=-0.3V | 2.4 | 2.5 | 3.1 | 1.7 | 1.9 | 2.4 | 1.6 | 1.8 | 2.1 |
| NBB=0 | 2.2 | 2.3 | 2.9 | 1.6 | 1.9 | 2.3 | 1.6 | 1.8 | 2.1 |
| FBB=+1.8V | 1.6 | 1.7 | 2.1 | 1.4 | 1.5 | 1.9 | 1.6 | 1.6 | 1.7 |

With this pre-characterization, the value of the critical resistance $R_C$ associated with each type of defect can be easily computed using the simple expressions reported

in Table 3.1, for different conditions of supply voltage, temperature and body-biasing. To validate this methodology, we have compared the values of the critical resistance computed using the compact model to the values of the critical resistance extracted from extensive fault simulation. In terms of simulation time, extensive fault simulation implies several hours of computation with standard equipment, so the proposed compact model offers a significant reduction of computational time.

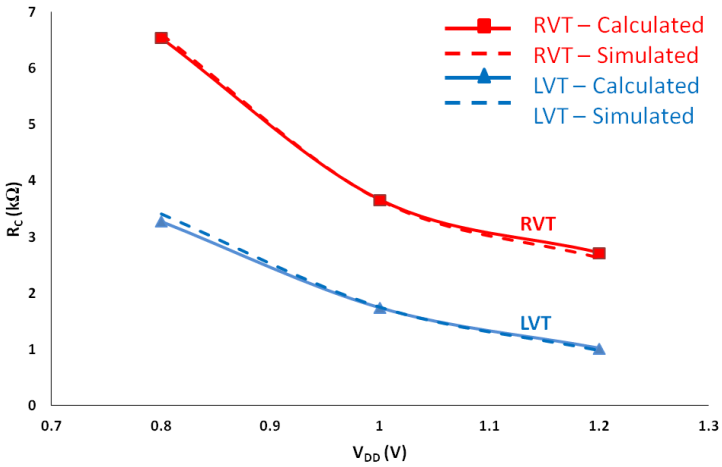
Figure 3.9 shows the variations of $R_C$ obtained either from simple calculation or extensive fault simulation as a function of (A) $V_{DD}$, (B) temperature and (C) body-biasing for an inter-gate bridging defect. A very good agreement can be observed both for RVT and LVT implementations. The same quality of matching between our compact model and extensive simulation can be observed for the other two types of defects: short-to-GND and short-to-$V_{DD}$. Results are summarized in Tables 3.9 and 3.10 which report the maximum error observed in the computed values of $R_C$ with respect to the ones obtained from extensive fault simulation under different operating conditions, for the different defect types.

**Table 3.9: Maximum error in $R_C$ obtained from the model – RVT.**

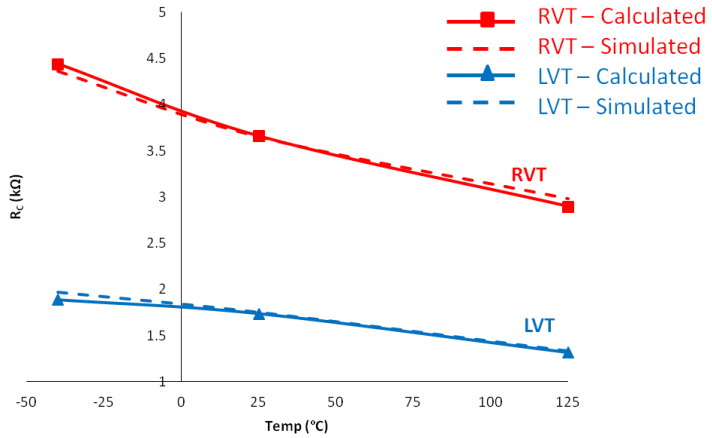
| RVT | Inter-gate bridging defect | Short-to-GND | Short-to-$V_{DD}$ |
|---|---|---|---|
| **$V_{DD}$** | 3.42% | 2.0% | 3.04% |
| **Temperature** | 2.68% | 1.66% | 1.44% |
| **Body-Biasing** | 2.10% | 1.61% | 1.61% |

**Table 3.10: Maximum error in $R_C$ obtained from the model – LVT.**

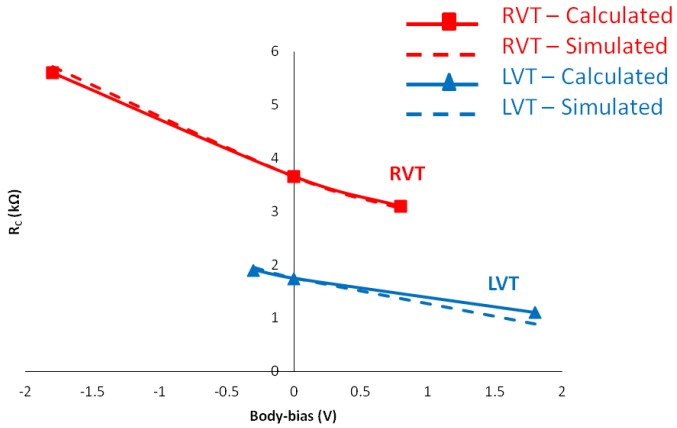
| LVT | Inter-gate bridging defect | Short-to-GND | Short-to-$V_{DD}$ |
|---|---|---|---|
| **$V_{DD}$** | 3.81% | 2.08% | 3.26% |
| **Temperature** | 4.06% | 1.92% | 1.81% |
| **Body-Biasing** | 24.58% | 7.57% | 5.69% |




**(A)**




**(B)**




**(C)**

**Figure 3.9: Variations of $R_C$ as a function of (A) $V_{DD}$ (B) temperature and (C) body-biasing, obtained from calculation or simulation, for an inter-gate bridging defect**

In case of RVT implementation, the maximum error remains below 5% whatever the conditions of power supply, temperature and body-biasing, demonstrating the validity of the proposed approach. In case of LVT implementation, the maximum error remains below 5% for the different conditions of power supply and temperature, but is slightly higher with respect to variations of the body-biasing voltage. In particular, a maximum error of 24% is observed in case of the inter-gate bridging defect under body-biasing variation. This error is observed under FBB condition, which actually induces a reduction of the critical resistance compared to nominal operating conditions. From a defect detection point of view, a reduction of the critical resistance is not a favorable condition since it reduces the defect detectability range. Excluding the FBB condition, the maximum error remains below 7%, which validates the proposed methodology to have an accurate computation of the critical resistance under favorable operating conditions for defect detection.

The analytical model proposed in this section in order to compute the critical resistance $R_C$ is tractable. It relies on the fast pre-characterization of the equivalent ON-resistance for P and N-type transistors used in the design. Note that this characterization of the cell library has to be done only once for a given technology. Once realized, the proposed model enables the computation of $R_C$ in various conditions of supply voltage, temperature and body-biasing without performing any fault simulation.

## 3.4 Simulation Results

In this section, we analyze through HSPICE simulation the impact of operating conditions on the detection of the different short defect types. More precisely, we perform simulations over an entire space within the specified ranges of body-biasing and temperature for three different values of $V_{DD}$ and we analyze the variation of the critical resistance $R_C$. For each defect type, we then identify the most favorable conditions and we quantify the enhancement in detectability brought by the individual and combined effects of supply voltage, temperature and body-biasing.

### 3.4.1 Resistive short-to-Ground Terminal (GND)

Let us first consider the case of resistive short-to-GND defect. Figures 3.10 and 3.11 depict the variations of $R_C$ over the investigated space of body-biasing voltage and temperature with each surface corresponding to a different value of $V_{DD}$, for RVT and LVT implementations respectively.

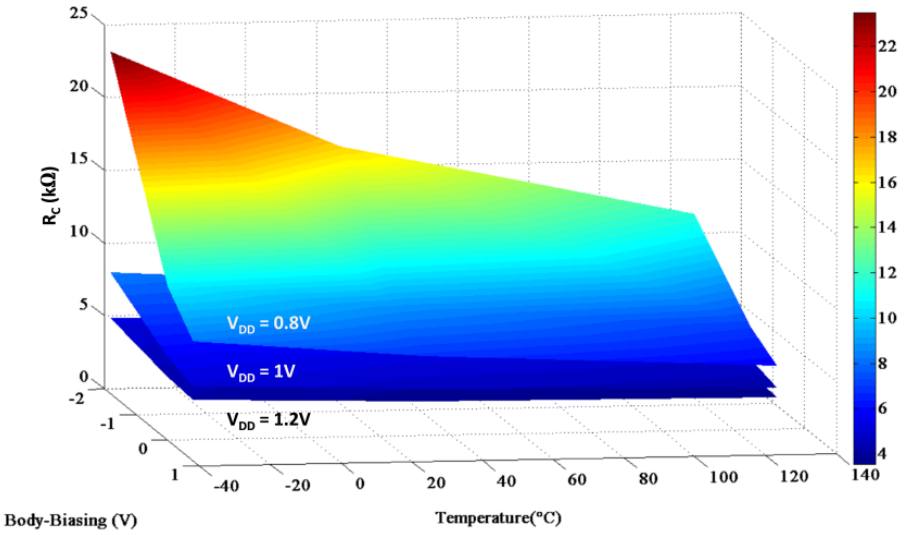



**Figure 3.10: Variations of $R_C$ as a function of Body-Biasing and Temperature at different $V_{DD}$ for FDSOI-RVT under the influence of resistive short-to-GND.**

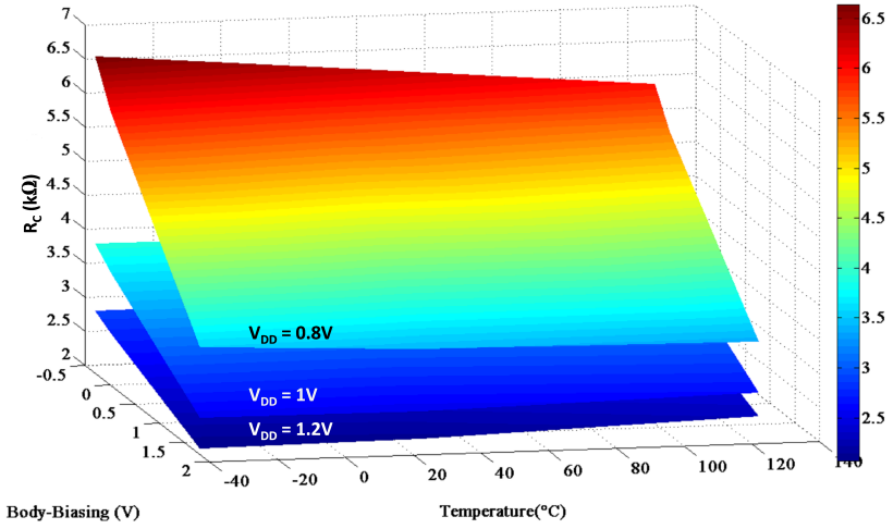



**Figure 3.11: Variations of $R_C$ as a function of Body-Biasing and Temperature at different $V_{DD}$ for FDSOI-LVT under the influence of resistive short-to-GND.**

For the sake of readability, some key values of the critical resistance $R_C$ have been extracted in Tables 3.11 and 3.12 for RVT and LVT implementations respectively.

**Table 3.11: Key values of $R_C$ varying operating conditions for FDSOI-RVT in presence of resistive short-to-GND.**

| RVT | $R_C$ (kΩ) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$=0.8V | | | $V_{DD}$=1V | | | $V_{DD}$=1.2V | | |
| TEMP (°C) | -40 | 25 | 125 | -40 | 25 | 125 | -40 | 25 | 125 |
| RBB=-1.8V | 23.5 | 16.7 | 11.6 | 8.3 | 7.4 | 6.6 | 5.2 | 4.9 | 4.7 |
| NBB=0 | 10.6 | 8.6 | 6.9 | 5.7 | 5.2 | 4.8 | 4.3 | 4.0 | 3.8 |
| FBB=+0.8V | 8.1 | 6.8 | 5.7 | 5.0 | 4.5 | 4.2 | 4.1 | 3.7 | 3.5 |

**Table 3.12: Key values of $R_C$ varying operating conditions for FDSOI-LVT in presence of resistive short-to-GND.**

| LVT | $R_C$ (kΩ) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$=0.8V | | | $V_{DD}$=1V | | | $V_{DD}$=1.2V | | |
| TEMP (°C) | -40 | 25 | 125 | -40 | 25 | 125 | -40 | 25 | 125 |
| RBB=-0.3V | 6.6 | 6.3 | 5.9 | 3.9 | 3.8 | 3.9 | 2.9 | 2.9 | 3.0 |
| NBB=0 | 6.0 | 5.7 | 5.4 | 3.6 | 3.6 | 3.6 | 2.7 | 2.7 | 2.9 |
| FBB=+1.8V | 3.5 | 3.4 | 3.3 | 2.5 | 2.5 | 2.6 | 2.0 | 2.1 | 2.2 |

In each Table, the nominal operating conditions ($V_{DD}$=1V, Temp=25°C, NBB) lie in the central cell and the corresponding $R_C$ value is presented in bold font. The central group of columns considers extreme variations of body-biasing and temperature conditions for nominal supply voltage (extractions from the central surface), while the first and third groups of columns consider the same body-biasing and temperature conditions for low and high values of $V_{DD}$ (extractions from the upper and lower surfaces), respectively. In each group of columns, the first column corresponds to low temperature conditions (Temp=-40°C, extractions from the left vertical plane of Figures 3.10 and 3.11), while the central column is obtained at nominal temperature (extractions from the vertical plane at Temp=25°C) and the last column refers to high temperature conditions (Temp=125°C, extractions from the right vertical plane of Figures 3.10 and 3.11). The first line of results shows the values of $R_C$ for the maximal Reverse Body-Biasing (RBB=-1.8V for RVT configuration or RBB=-0.3V for LVT configuration,

extractions from the back vertical plane of Figures 3.11 and 3.12), while the second line presents extractions of $R_C$ values without body-biasing (from the vertical plane at $V_{BB}$=0) and the third line gives the values extracted from the front vertical plane with maximal Forward Body-Biasing (FBB=0.8V and FBB=1.8V for RVT and LVT configurations respectively).

Results show that lower supply voltage, lower temperature and Reverse Body-Biasing (RBB) tend to increase the value of the critical resistance, i.e. improve the detectability of the resistive short defects, both for RVT and LVT implementations. However, it can be noticed that the detectability range is substantially different for RVT and LVT implementations. The critical resistance $R_C$ under nominal operating conditions ($V_{DD}$=1V, Temp=25°C, NBB, in bold font in the Tables 3.11 and 3.12) is equal to 5.2kΩ for RVT and 3.6kΩ for LVT. This difference comes from the fact that the equivalent ON-resistance is significantly higher for PMOS-RVT transistors than PMOS-LVT ones. For instance under nominal conditions, $R_{P\text{-}on}$ is equal to 6.1kΩ for RVT and 3.8kΩ for LVT, so more than 1.5 times higher for RVT. In agreement with the analytical model $R_C=\beta.R_{P\text{-}on}$ and even if the β factor is slightly lower for RVT, this does not compensate the difference in the ON-resistance; the critical resistance is therefore higher for RVT devices than LVT ones. This difference is even amplified when switching to the most favorable conditions ($V_{DD}$=0.8V, Temp=-40°C, RBB, upper left cell in Tables 3.11 and 3.12). In this case, the critical resistance $R_C$ is equal to 23.5kΩ for RVT and 6.6kΩ for LVT, which corresponds to an improvement in detectability by a factor of 4.5 for RVT and 1.7 for LVT. The difference in the improvement factor mainly comes from the fact that RVT devices can support large body-bias voltage in RBB mode ($V_{BB}$=-1.8V) while LVT devices have a very limited range ($V_{BB}$=-0.3V).

Our key observations with respect to short-to-GND defect are therefore: **(i) RVT implementation has intrinsically better detectability properties than LVT one, (ii) considerable improvement of the detectability range can be achieved by switching to low $V_{DD}$, low temperature and RBB, and (iii) this improvement is stronger for RVT implementation than LVT one.**

### 3.4.2 Resistive short-to-Power Supply ($V_{DD}$)

Let us now consider the case of short-to-$V_{DD}$ defect. Figures 3.12 and 3.13 depict the variation of $R_C$ over the investigated space of body-biasing voltage and

temperature with each surface corresponding to a different value of $V_{DD}$, for RVT and LVT implementations respectively. Tables 3.13 and 3.14 present some key values of $R_C$ varying operating conditions to their extreme dynamic ranges, extracted from Figures 3.12 and 3.13 as in the previous defect type study.

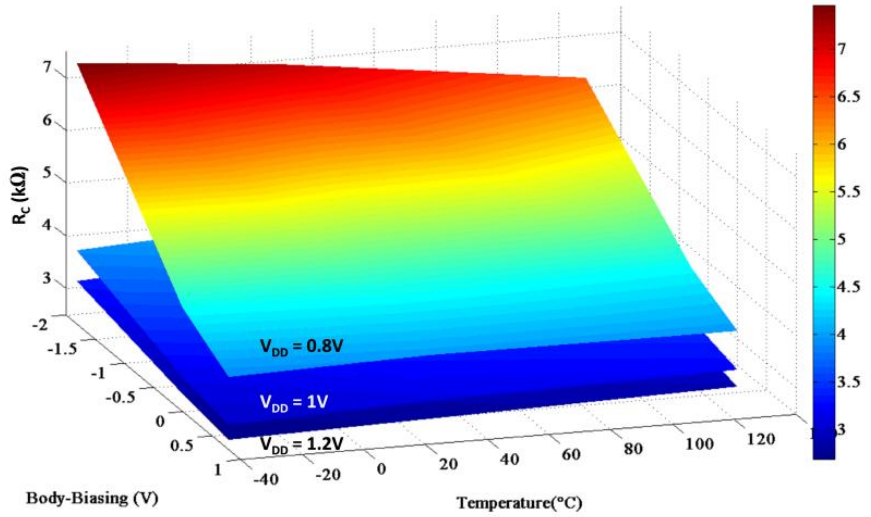



**Figure 3.12: Variations of $R_C$ as a function of Body-Biasing and Temperature at different $V_{DD}$ for FDSOI-RVT under the influence of resistive short-to-$V_{DD}$.**

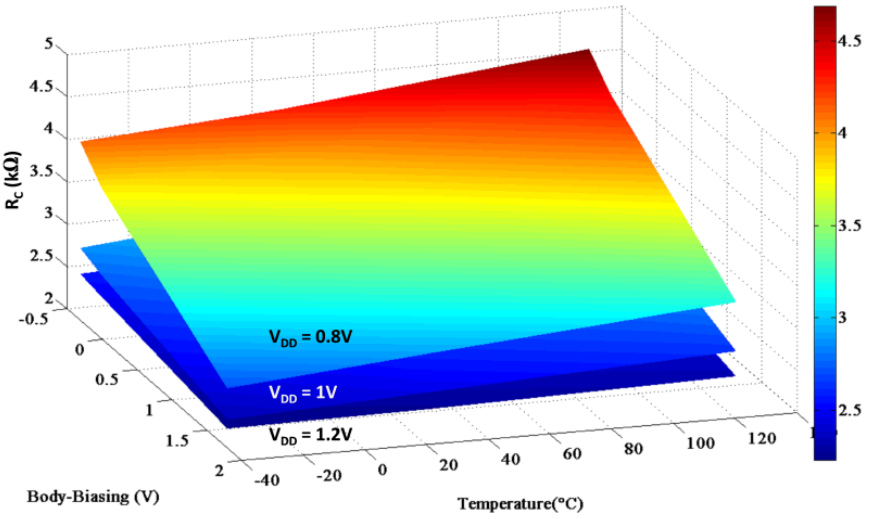



**Figure 3.13: Variations of $R_C$ as a function of Body-Biasing and Temperature at different $V_{DD}$ for FDSOI-LVT under the influence of resistive short-to-$V_{DD}$.**

**Table 3.13: Key values of $R_C$ varying operating conditions for FDSOI-RVT in presence of resistive short-to-$V_{DD}$.**

| RVT | $R_C$ (kΩ) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$=0.8V | | | $V_{DD}$=1V | | | $V_{DD}$=1.2V | | |
| TEMP (°C) | -40 | 25 | 125 | -40 | 25 | 125 | -40 | 25 | 125 |
| RBB=-1.8V | 7.5 | 7.1 | 6.3 | 3.9 | 4.1 | 4.2 | 3.3 | 3.5 | 3.7 |
| NBB=0 | 4.4 | 4.5 | 4.4 | 3.1 | 3.3 | 3.4 | 2.8 | 2.9 | 3.1 |
| FBB=+0.8V | 3.8 | 3.9 | 3.9 | 2.9 | 3.1 | 3.2 | 2.6 | 2.7 | 2.9 |

**Table 3.14:Key values of $R_C$ varying operating conditions for FDSOI-LVT in presence of resistive short-to-$V_{DD}$.**

| LVT | $R_C$ (kΩ) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$=0.8V | | | $V_{DD}$=1V | | | $V_{DD}$=1.2V | | |
| TEMP (°C) | -40 | 25 | 125 | -40 | 25 | 125 | -40 | 25 | 125 |
| RBB=-0.3V | 4.1 | 4.2 | 4.7 | 2.8 | 3.1 | 3.4 | 2.5 | 2.6 | 2.8 |
| NBB=0 | 3.7 | 3.9 | 4.3 | 2.7 | 3.0 | 3.2 | 2.5 | 2.6 | 2.7 |
| FBB=+1.8V | 2.7 | 2.9 | 3.2 | 2.3 | 2.4 | 2.6 | 2.2 | 2.2 | 2.3 |

Results show that lower supply voltage and Reverse Body-Biasing (RBB) tend to increase the value of the critical resistance and hence improve the defect detectability both for RVT and LVT implementations. However, the effect of temperature is more complex and differs depending of the device type. For LVT implementation, higher temperature tends to increase the value of the critical resistance whatever $V_{DD}$ and body-biasing conditions. However for RVT implementation, although higher temperature also results in an increase of the critical resistance in most cases, there is an exception where it induces a decrease or very small non-monotonic variation of $R_C$ in case of low $V_{DD}$ and no or reverse body-biasing (three first columns of the first two rows of the $R_C$ values presented in Table 3.7, or alternatively back vertical plane and vertical plane at $V_{BB}$=0V for the upper surface in Figure 3.13). Globally, the most favorable conditions for the detection of a short-to-$V_{DD}$ defect correspond to low supply voltage, RBB and low temperature for RVT and low supply voltage, RBB and high

temperature for LVT (leading to the highest value of $R_C$ in Tables 3.7 and 3.8 or Figures 3.13 and 3.14 respectively). The critical resistance actually increases from to 3.3kΩ under nominal conditions up to 7.5kΩ under the most favorable conditions for RVT, and from 3.0kΩ up to 4.7kΩ for LVT. This corresponds to an improvement in detectability of defect by a factor of 2.2 for RVT and 1.6 for LVT. Here again the improvement in detectability is more pronounced for RVT than LVT thanks to the wide possibility of reverse body-biasing for RVT devices. Note that on the contrary of short-to-GND defect, RVT and LVT implementations have almost the same detectability range under nominal operating conditions. Indeed the equivalent ON-resistance under nominal operating conditions is similar with $R_{N\text{-}on}$ equal to 2.87kΩ for RVT and 2.84kΩ for LVT. In agreement with the analytical model $R_C=R_{N\text{-}on}/\beta$, the critical resistance is therefore in the same range for RVT and LVT implementations. Finally it is worth noting that the equivalent ON-resistance of NMOS transistors is much smaller than the equivalent ON-resistance of PMOS transistors, both for RVT and LVT implementations. The detectability range of short-to-$V_{DD}$ defect is therefore restricted compared to the detectability range of short-to-GND defect.

Key observations with respect to short-to-$V_{DD}$ defect are therefore: **(i) RVT and LVT implementations have intrinsically similar detectability properties under nominal operating conditions, (ii) improvement of the detectability range can be achieved by switching to more favorable operating conditions, which depends on the implementation type (low $V_{DD}$, low temperature and RBB for RVT and low $V_{DD}$, high temperature and RBB for LVT), and (iii) the improvement brought by the most favorable conditions is larger for RVT implementation than LVT one.**

### 3.4.3 Inter-Gate Resistive Bridging Defect

Finally let us consider the case of inter-gate bridging defect. Figures 3.14 and 3.15 depict the variation of $R_C$ over the investigated space of body-biasing voltage and temperature with each surface corresponding to a different value of $V_{DD}$, for RVT and LVT implementations respectively. Tables 3.15 and 3.16 extract extreme values of $R_C$ varying operating conditions from nominal to their maximum values, extracted from Figures 3.14 and 3.15 according to the corresponding vertical planes or surfaces of interest. These results show that lower voltage, lower temperature and Reverse Body-Biasing (RBB) tend to increase the value of the critical resistance both for RVT and LVT implementations. These results are actually very similar to the case of a short-to-

GND defect, but with a slightly reduced detectability range. This is in agreement with the analytical model $R_C=\beta.R_{P\text{-}on}-R_{N\text{-}on}$.

Indeed, as previously mentioned the equivalent ON-resistance of PMOS transistors is much higher than the equivalent resistance of NMOS transistors. The predominant effect thus comes from the variation of the term '$\beta.R_{P\text{-}on}$', which are the same in case of an inter-gate bridging defect and a short-to-GND defect. The same trends are therefore observed but with a detectability range reduced by the term '$R_{N\text{-}on}$'.

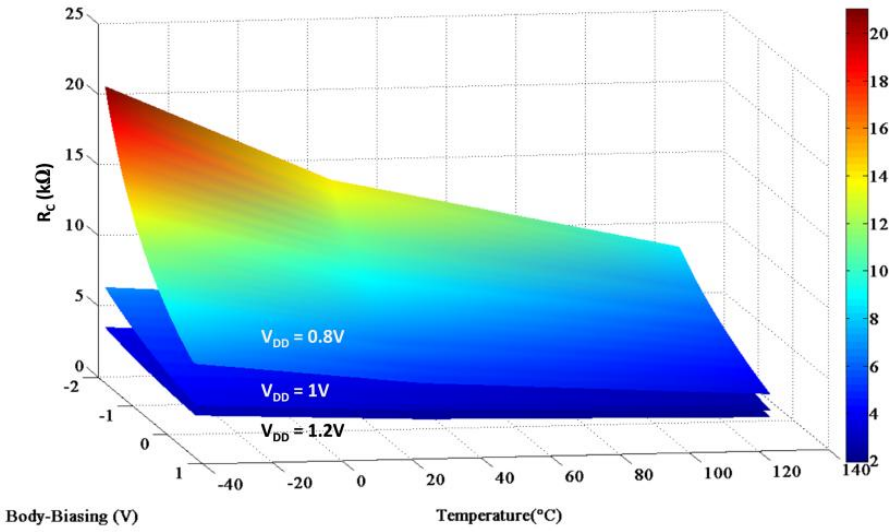



**Figure 3.14: Variations of $R_C$ as a function of Body-Biasing and Temperature at different $V_{DD}$ for FDSOI-RVT under the influence of inter-gate bridging defect.**

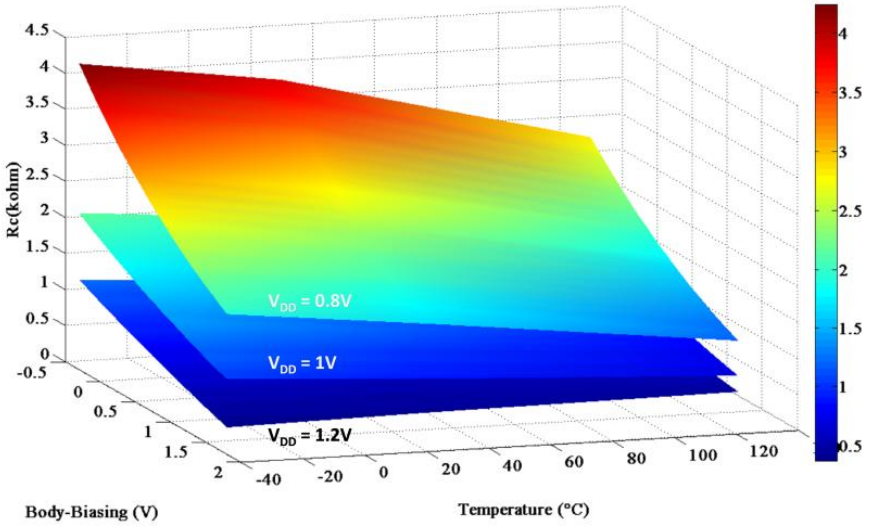



**Figure 3.15: Variations of $R_C$ as a function of Body-Biasing and Temperature at different $V_{DD}$ for FDSOI-LVT under the influence of inter-gate bridging defect.**

**Table 3.15: Key values of $R_C$ varying operating conditions for FDSOI-RVT in presence of inter-gate bridging defect.**

| RVT | $R_C$ (kΩ) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$=0.8V | | | $V_{DD}$=1V | | | $V_{DD}$=1.2V | | |
| TEMP (°C) | -40 | 25 | 125 | -40 | 25 | 125 | -40 | 25 | 125 |
| RBB=-1.8V | 21 | 14 | 8.7 | 6.7 | 5.7 | 4.5 | 3.9 | 3.4 | 3.0 |
| NBB=0 | 8.7 | 6.6 | 4.6 | 4.3 | 3.7 | 2.9 | 3.1 | 2.6 | 2.2 |
| FBB=+0.8V | 6.4 | 4.9 | 3.5 | 3.8 | 3.0 | 2.4 | 3.0 | 2.3 | 1.9 |

**Table 3.16: Key values of $R_C$ varying operating conditions for FDSOI-LVT in presence of inter-gate bridging defect.**

| LVT | $R_C$ (kΩ) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$=0.8V | | | $V_{DD}$=1V | | | $V_{DD}$=1.2V | | |
| TEMP (°C) | -40 | 25 | 125 | -40 | 25 | 125 | -40 | 25 | 125 |
| RBB=-0.3V | 4.2 | 3.9 | 2.8 | 2.1 | 1.9 | 1.4 | 1.2 | 1.1 | 0.9 |
| NBB=0 | 3.7 | 3.4 | 2.4 | 1.9 | 1.8 | 1.3 | 1.1 | 0.9 | 0.8 |
| FBB=+1.8V | 1.9 | 1.6 | 1.1 | 1.0 | 0.8 | 0.6 | 0.3 | 0.4 | 0.4 |

This study has permitted to identify the most favorable conditions for the different defect types and the different implementations. To further develop the work, it is also interesting to analyze the individual as well as combined impact of supply voltage, temperature and body-biasing on defect detectability. To this aim, a set of study cases is taken into consideration as shown in Table 3.17.

**Table 3.17: Different cases of study to evaluate the individual and combined impact of $V_{DD}$, temperature and BB on defect detection.**

| CASE | Temperature | Body-biasing | $V_{DD}$ |
|---|---|---|---|
| I | X | | |
| II | | X | |
| III | | | X |
| IV | X | X | |
| V | X | | X |
| VI | | X | X |
| VII | X | X | X |

In these different cases, one or several parameters are varied from the nominal operating conditions ($V_{DD}$=1V, T=25°C, NBB), as indicated by the 'X' mark in the Table. The individual impact of each parameter is considered in Cases I to III, the combined impact of two parameters in Cases IV to VI, and Case VII corresponds to the optimal conditions where the three parameters are varied altogether. According to previous results, optimized conditions regarding power supply and body-biasing correspond to low $V_{DD}$ ($V_{DD}$=0.8V) and reverse body-biasing (RBB) whatever the defect type and whatever the implementation type. Regarding temperature, optimized condition differs depending on the defect type and the implementation type. In case of short-to-GND and inter-gate bridging defect, optimized condition corresponds to low temperature (T=-40°C) for both RVT and LVT implementations. In case of short-to-$V_{DD}$, optimized condition corresponds to high temperature (T=125°C) for LVT implementation. The situation is more complex for RVT implementation, where optimized condition corresponds to high temperature if only one or two parameters are varied, and low temperature if the three parameters are varied altogether.

To analyze the individual and combined impact of the different parameters, we have quantified the detection improvement associated to cases I to VII, expressed as the percentage increase in the value of the critical resistance $R_C$ with respect to the reference nominal operating mode. Results are summarized in Figures 3.16 to 3.18 for the three different defect types.

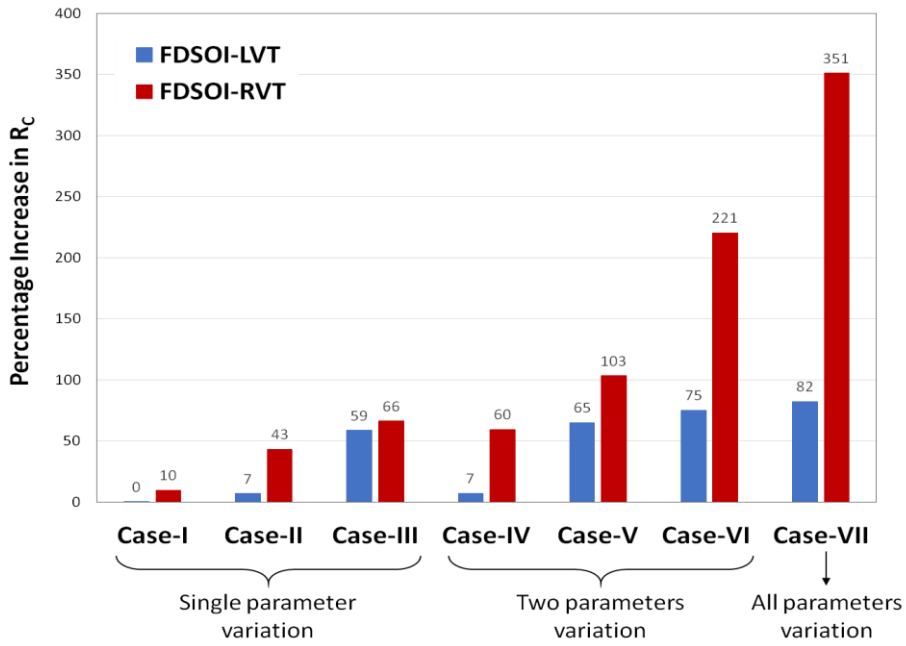



**Figure 3.16: Improvement in detection of resistive short-to-GND achieved by $V_{DD}$, temperature and body-biasing variations for the cases presented in Table 3.17.**

In case of short-to-GND defect (cf. Figure 3.16), the strongest improvement is obtained both for RVT and LVT by combining low $V_{DD}$, low temperature and RBB (Case VII) as already established. However, it is important to remark that the relative contribution of each one of these parameters is not equivalent and differs depending on the implementation type. For RVT implementation, we observe a minor improvement when using only low temperature (Case I: 10%) while we observe a significant improvement when using only either RBB (Case II: 43%) or low $V_{DD}$ (Case III: 66%). When combining two parameters, the best improvement is observed with low $V_{DD}$ and RBB (Case VI: 221%), which is more than twice higher than the improvement observed with the combination of low $V_{DD}$ and low temperature (Case V: 103%) and more than three times higher than the improvement observed with the combination of RBB and low temperature (Case IV: 60%). Finally, it is worth noting that the use of the three parameters altogether introduces a substantial benefit with an additional gain of more than +100 % (Case VII: 351%). In summary, the three parameters have a notable impact, with priority to low $V_{DD}$ and RBB conditions. For LVT implementation, results reveal that $V_{DD}$ is the most influential parameter. Indeed, negligible improvement is observed when using only low temperature (Case I: 0.2%) or RBB (Case II: 7%) while significant improvement is observed with low $V_{DD}$ (Case III: 59%). A benefit is obtained by combining several parameters, but in a limited range. A gain of +16% can

be achieved by combining two parameters, i.e. low $V_{DD}$ and RBB (Case VI: 75%), and an additional gain of +7% by combining the three parameters (Case VII: 82%).

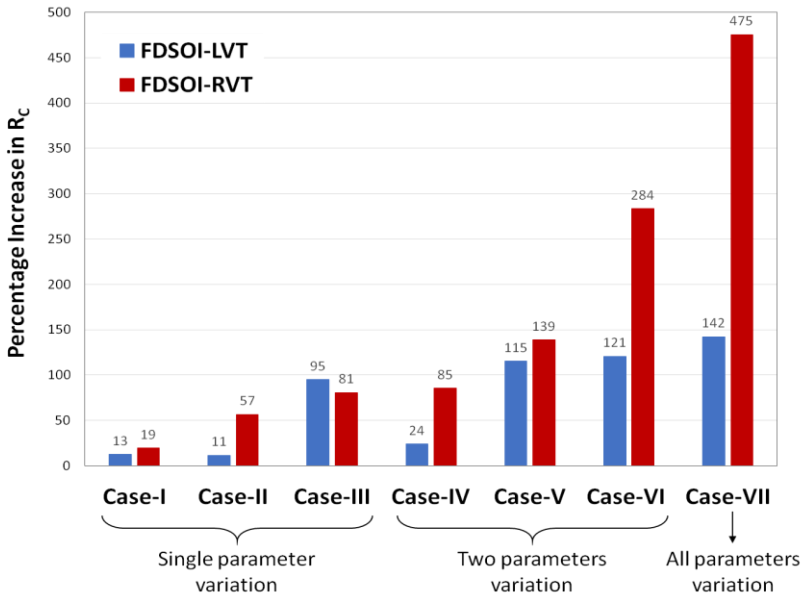



**Figure 3.17: Improvement in detection of inter-gate bridging defect achieved by $V_{DD}$, temperature and body-biasing variations for the cases presented in Table 3.17.**

In case of inter-gate bridging defect, we have already commented that observed trends are similar to the case of short-to-GND defect. Results of Figure 3.17 confirm this observation. In particular for RVT implementation, we observe a significant improvement by using low $V_{DD}$ (Case III: 81%), then low $V_{DD}$ and RBB (Case VI: 284%), then low $V_{DD}$, RBB and low temperature (Case VII: 475%). For LVT implementation, there is also a significant improvement by using low $V_{DD}$ (Case III: 95%), but then a more contained improvement by using low $V_{DD}$ and RBB (Case VI: 121%) and low $V_{DD}$, RBB and low temperature (Case VII: 142%). Globally, there is a strong benefit of combining several parameters for RVT while it is more limited for LVT.

Finally in case of short-to-$V_{DD}$ defect, results are presented in Figure 3.18. As far as individual contribution is considered, the major impact is brought by switching to low $V_{DD}$, with almost a similar improvement around 35% for both RVT and LVT implementations (Case III). Again, RBB provides notable improvement for RVT (Case II: 23%) but has a minor impact for LVT (Case II: 4%); temperature has a minor impact for RVT (Case I: 5%) and limited impact for LVT (Case II: 10%). Regarding the combined impact of two parameters, the most significant improvement is obtained using

low $V_{DD}$ and RBB for RVT (Case VI: 114%) and using low $V_{DD}$ and high temperature for LVT (Case V: 48%). Finally, it should be pointed out that the combination of all parameters induces minor improvement with an additional gain of only +10% both for RVT (Case VII: 124%) and LVT (Case VII: 58%).

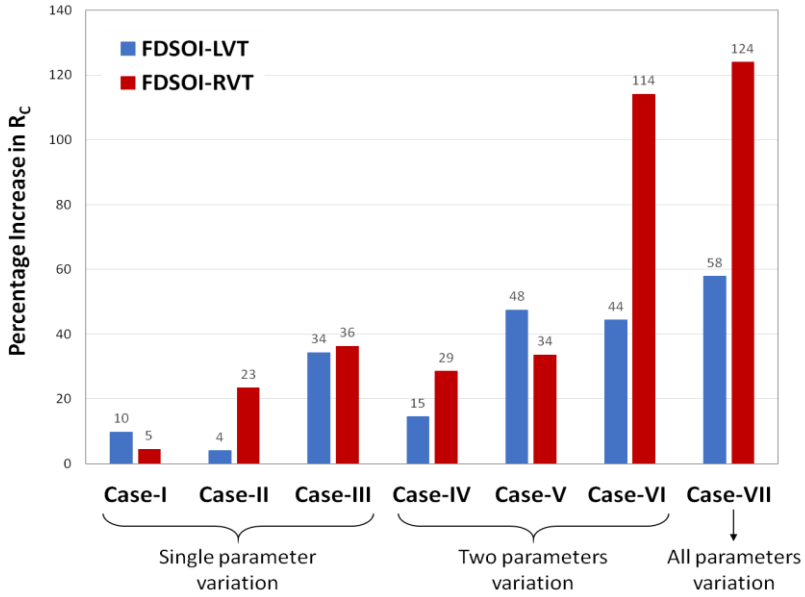



**Figure 3.18: Improvement in detection of resistive short-to-$V_{DD}$ achieved by $V_{DD}$, temperature and body-biasing variations for the cases presented in Table 3.17.**

An important outcome of this study is that power supply and body-biasing are preponderant parameters compared to temperature. Indeed, whatever the defect type and the implementation, low $V_{DD}$ condition brings the most significant improvement if only one parameter is used. Regarding the combination of two parameters, low $V_{DD}$ and RBB is the best combination in almost all cases; temperature is part of the best combination only in one case, i.e. short-to-$V_{DD}$ defect with LVT implementation. Moreover, the benefit of combining temperature with low $V_{DD}$ and RBB condition is significant only for short-to-GND and inter-gate bridging defect with RVT implementation, but leads to minor improvement in all other cases.

It should be pointed out that in an industrial test context, applying low supply voltage and dedicated body-biasing conditions does not require any specific equipment and can be easily implemented in a standard ATE. In contrast, achieving very low (–40°C) or very high (+125°C) temperature induces severe practical difficulties and might engender unaffordable supplementary cost with regard to the additional detection improvement benefit. To illustrate this point, Figures 3.19 and 3.20 summarize the detectability range that can be achieved using only electrical parameters (power supply

and body-biasing voltages) or using electrical parameters combined with temperature, for RVT and LVT implementations respectively. The detectability range under standard nominal operating mode is also given as reference.

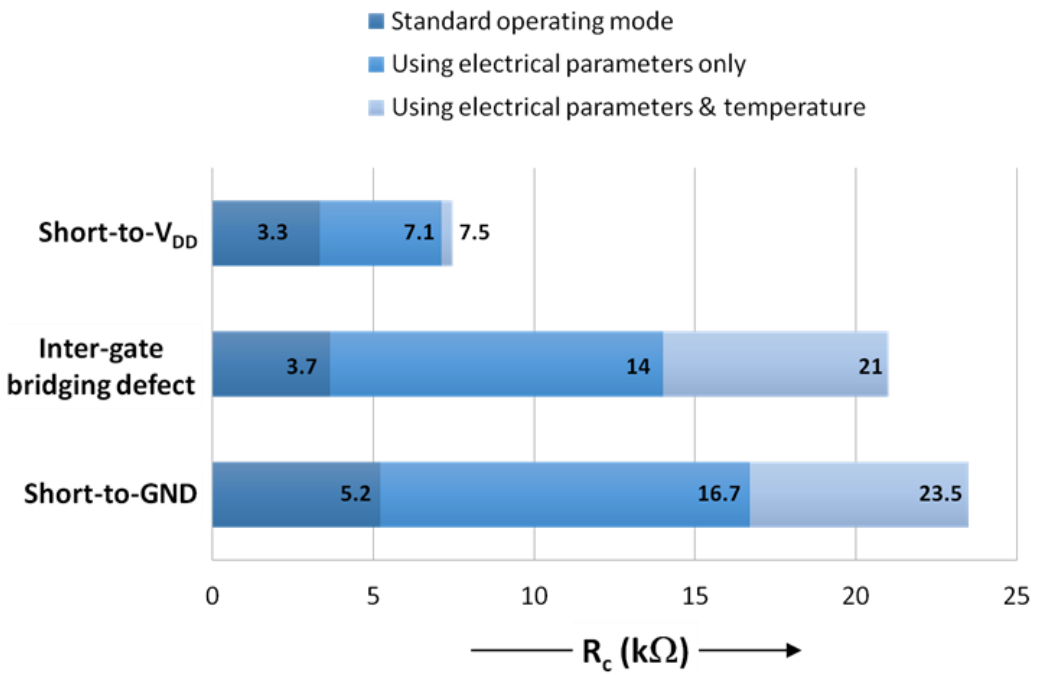



**Figure 3.19: Detectability range of the different defect types for RVT implementation.**

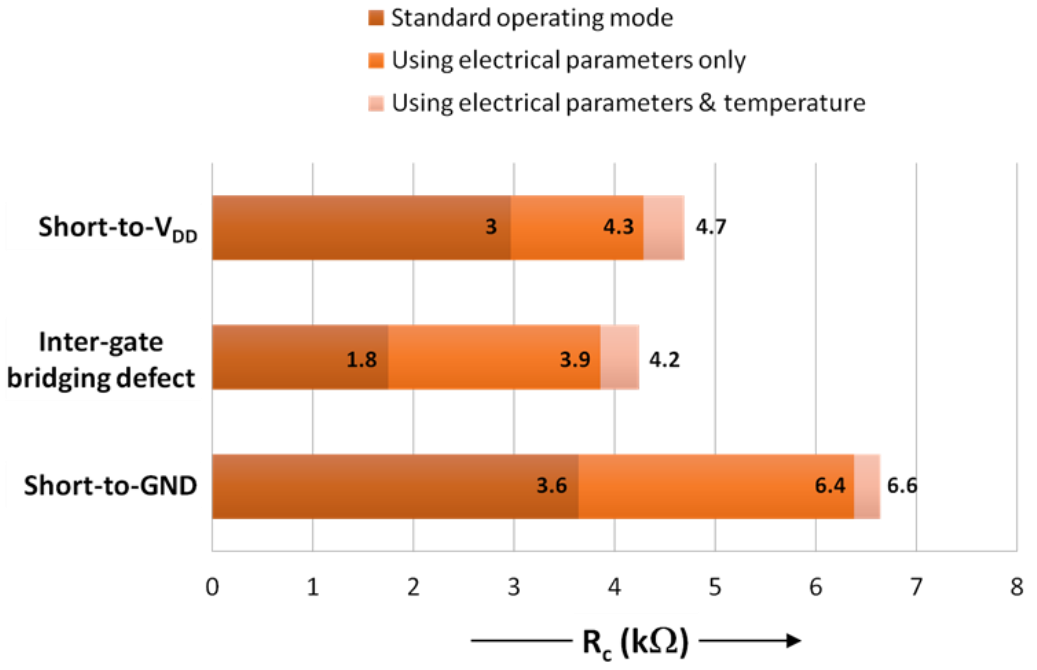


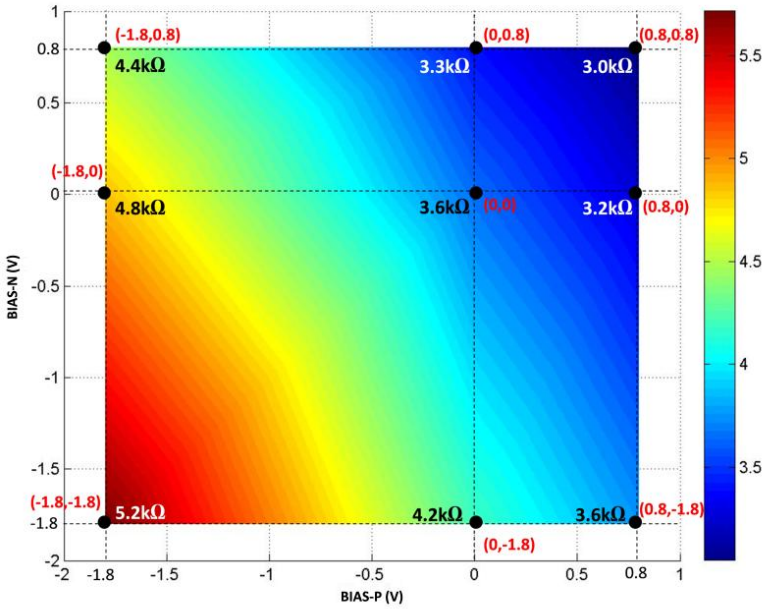

**Figure 3.20: Detectability range of the different defect types for LVT implementation.**

This figure clearly highlights the extension of the detectability range that can be achieved using appropriate electrical setting (low $V_{DD}$ and RBB) compared to the standard nominal operating mode. It also shows that the additional improvement introduced by temperature is significant only for RVT implementation in case of short-to-GND or inter-gate bridging defect. However in these cases, the defect detectability range achieved with appropriate electrical setting only is already large, with a critical resistance higher than 14kΩ for inter-gate bridging defect and higher than 16kΩ for short-to-GND. In all other cases, the use of temperature introduces only an incremental enlargement of the detectability range.

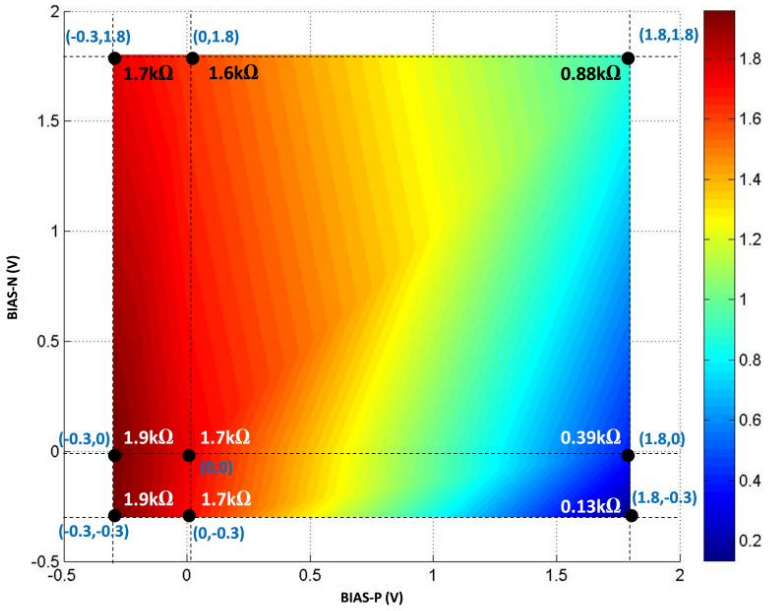
## 3.5 Exploring Body-Biasing

The study in the previous sections was restricted to the same body-biasing condition applied to both P and N transistors (NBB, FBB or RBB), which is the regular use of the body-biasing feature recommended by the manufacturer. In this section, we extend the study by performing a deeper exploration of the use of body-biasing feature. In particular, we investigate whether independent body-biasing of P and N transistors (e.g. forward for one type of transistor while reverse for the other and vice-versa) would permit to gain additional improvement in term of resistive short defect detection.

In this objective, widespread simulations have been performed with an independent variation of the voltages at the body terminal of P transistors (Bias-P) and N transistors (Bias-N) considering all possible combinations of NBB, RBB and FBB. In case of RVT implementation, the variation range for Bias-P and Bias-N is comprised between [-1.8V; 0.8V] while on case of LVT implementation, it is comprised between [-0.3; 1.8V]. For all combinations of Bias-P/Bias-N values within the possible range, the value of the critical resistance $R_C$ has been determined. Figure 3.21 presents the variation of the critical resistance $R_C$ as a function of the voltage at the body terminal of P transistors (Bias-P) and N transistors (Bias-N) in case of an inter-gate resistive bridging defect, both for (A) RVT and (B) LVT implementations.




**(A)**




**(B)**

**Figure 3.21: Variation in $R_C$ with body-biasing P and N transistors for circuit affected by inter-gate resistive bridging defect (A) RVT (B) LVT.**

As shown in Figure 3.21 (A), the value of the critical resistance under nominal operating conditions (i.e. NBB for both P and N transistors) is equal to 3.6kΩ for RVT implementation. Starting from this nominal point, a decrease of the critical resistance is

observed when implementing FBB on either type of transistors: $R_C$=3.2kΩ with Bias-P=0.8V and Bias-N=0V, $R_C$=3.3kΩ with Bias-P=0V and Bias-N=0.8V. Conversely, an increase of the critical resistance is observed when implementing RBB on either type of transistors: $R_C$=4.8kΩ with Bias-P=-1.8V and Bias-N=0V, and $R_C$=4.2kΩ with Bias-P=0V and Bias-N=-1.8V. Globally, with respect to nominal conditions, there is no impact when applying FBB on P-type transistors and RBB on N-type transistors ($R_C$=3.6kΩ with Bias-P=0.8V and Bias-N=-1.8V), and a positive impact when applying RBB on P-type transistors and FBB on N-type transistors ($R_C$=4.4kΩ with Bias-P=-1.8V and Bias-N=0.8V). Yet, the best situation is obtained when full RBB voltage is applied on both types of transistors ($R_C$=5.2kΩ with Bias-P= Bias-N=-1.8V). There is therefore no interest of using independent body-biasing for P and N transistors. Similar observations can be derived for LVT implementation, as illustrated in Figure 3.21 (B).

This study of critical resistance variations over the entire space of body-biasing has been also carried out for short-to-ground and short-to-$V_{DD}$ defects. The results obtained are in line with the results of resistive bridging defect, i.e. there is no interest of using independent body-biasing for P and N transistors since the optimal case for the detection of these defects is achieved by using full RBB voltage on both P and N transistors, whatever the implementation type.

## 3.6 Summary

This chapter has presented a detailed analysis for the detection of resistive short-to-ground, short-to-power supply and inter-gate bridging defects in FDSOI in the context of logic based test, considering the individual and combined improvements brought by supply voltage, body-biasing and temperature test conditions. Simulations of simple didactic circuits implemented with standard elementary inverters from the 28nm UTBB FDSOI gate library have been carried out using HSPICE, considering the two implementation options offered by the technology, i.e. Low $V_T$ (LVT) and Regular $V_T$ (RVT) devices. Defect detectability has been evaluated using the concept of critical resistance. A simple analytical model has been proposed that enables the computation of the critical resistance ($R_C$) in various conditions of supply voltage, body-biasing and temperature without performing any fault simulation. Results have shown that this

model enables accurate estimation of the critical resistance for all defect types and leads to a better understanding of the favorable operating conditions to improve defect detectability.

Optimal conditions for the detection of the different defect types have been established. Results have shown that the best situation for RVT implementation is obtained with low $V_{DD}$, RBB and low temperature, whatever the defect type. In case of LVT implementation, the detectability of short-to-GND and inter-gate resistive bridging defects is also optimized by low $V_{DD}$, RBB and low temperature. However, for resistive short-to-$V_{DD}$, high temperature favors the detection.

The relative contribution of the three parameters has also been analyzed. Results have pointed out that power supply and body-biasing are preponderant parameters compared to temperature, whatever the defect type. Significant enlargement of the detectability range can be achieved using only these electrical parameters, which is an important point when the test cost is taken into consideration.

Finally in the last section, a deeper exploration of the use of body-biasing feature has been realized. In particular, independent body-biasing of P and N type transistors have been investigated. Results have shown that such independent biasing does not offer any benefit compared to the situation where reverse body-biasing is applied on both P and N-type transistors.

# 4 COMPREHENSIVE STUDY FOR DETECTION OF WEAK RESISTIVE OPEN AND SHORT DEFECTS BY DELAY TESTING IN FDSOI TECHNOLOGY

# 4.1 INTRODUCTION

This chapter presents a detailed analysis for the detection of weak resistive open and resistive short defects using delay test for a didactic circuit implemented in 28nm UTBB FDSOI technology. The two different $V_T$ options offered by the technology, i.e. Regular-$V_T$ (RVT) and Low-$V_T$ (LVT), are explored. Based on HSPICE simulations, this work determines the most suitable operating conditions in terms of power supply and body-biasing to achieve maximum coverage of weak resistive short and resistive open defects in the context of delay test.

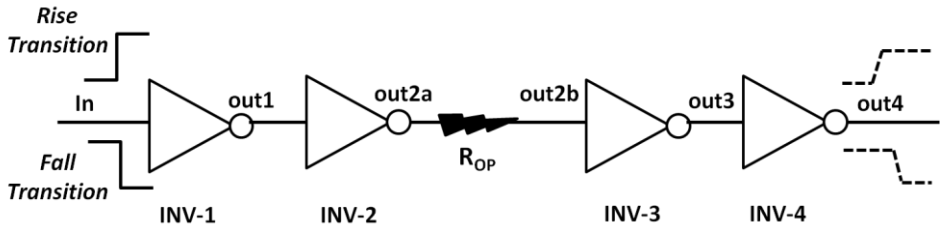
The work described in this chapter is organized as follows. An overview of the circuit under test is presented in Section 4.2. Section 4.3 focuses on the methodology for determining the detectability range of resistive open and short defects by delay testing. Section 4.4 presents the simulation results along with the analysis of the individual and combined impact of body biasing and supply voltage on defect detection. Finally concluding remarks are given in Section 4.5.

# 4.2 CIRCUIT UNDER TEST

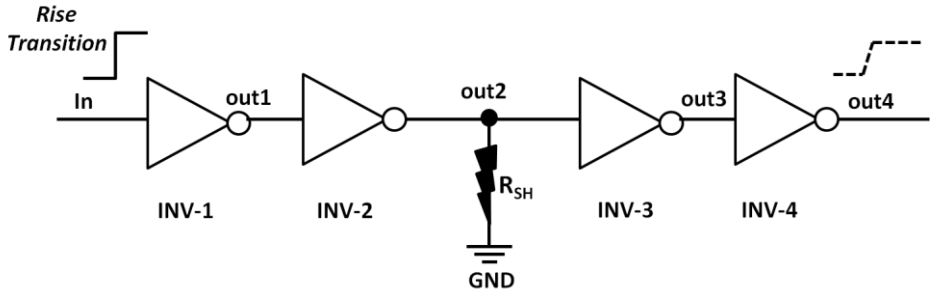
In order to study the detection of weak resistive open and short defects, we consider a simple didactic circuit composed of a chain of four inverters (INV-1 to INV-4). This circuit is implemented in 28nm UTBB FDSOI technology using standard elementary inverters from the library. The two $V_T$ options offered by the technology are considered, i.e. using either RVT or LVT devices.

Three different defects are studied, which consist of a resistive open, a resistive short to ground and a resistive short to $V_{DD}$. In each case, the defect is inserted in the middle of the inverter chain. The different setups associated to the study of the different defects are illustrated in Figure 4.1.

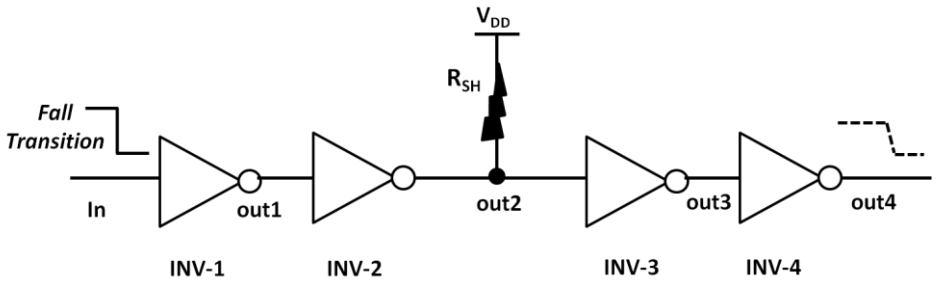
In case of the open defect, a variable resistance $R_{OP}$ is inserted between the output of INV-2 and the input of INV-3, as shown in Figure 4.1(A). Electrical transient simulations are performed varying the value of the open resistance $R_{OP}$ from 0 (fault-free circuit) towards infinity (full open) and defect detection is analyzed by looking at the total delay of the chain. This analysis is performed for both rising and falling transitions applied on the input of the chain.




**(A)**




**(B)**




**(C)**

**Figure 4.1: Circuit under test (A) Resistive open defect (B) Resistive short-to-GND (C) Resistive short-to-$V_{DD}$.**

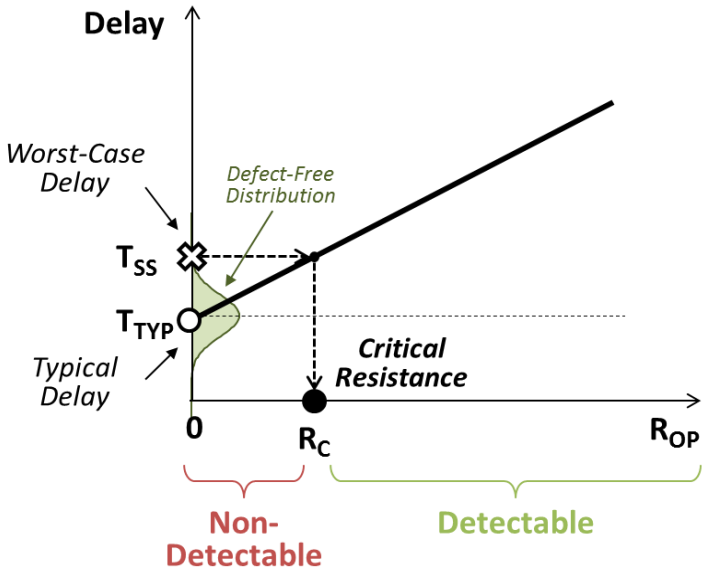
In case of a short defect, a variable resistance $R_{SH}$ is inserted between the output of INV-2 and either the ground terminal (GND) or the power supply terminal ($V_{DD}$), as shown in Figures 4.1(B) and 4.1(C) respectively. Here again, electrical transient simulations are performed varying the value of the short resistance $R_{SH}$ from 0 (frank short-circuit) towards infinity (fault-free circuit) and defect detection is analyzed by looking at the total delay of the chain. This analysis is performed for a rising transition applied at the input of the chain in case of short-to-ground defect, and a falling transition in case of short-to-$V_{DD}$ defect, given that these cases lead to an increasing of the chain delay, while opposite transitions lead to a speed-up which is not favorable towards delay testing.

## 4.3 DEFECT DETECTION

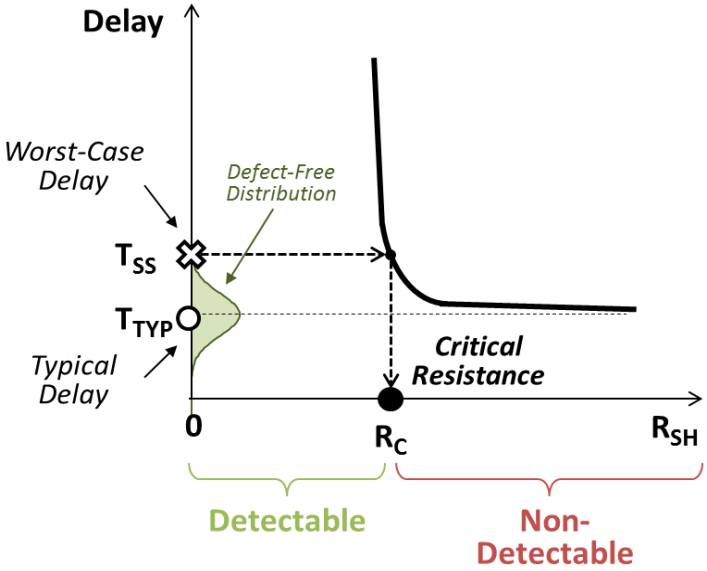
As it has been extensively shown in the literature, the presence of resistive defects may cause a malfunctioning of the circuit behavior in case of strong defects or just affect the circuit timing in case of weak defects. In this latter case, defects cannot be detected with a simple logic test but might be detected by delay-based test. In this chapter, we focus on weak resistive defects that might be detected through delay testing and our objective is to determine $V_{DD}$ and body biasing conditions that permit to optimize the defect detectability range.

In order to quantify the defect detectability range, we use the concept of critical resistance first introduced in [33] with respect to Boolean test, and then extended in [74] with respect to delay testing. In particular in [74], the Dynamic Critical Resistance (DCR) is defined as the value of the defect resistance for which the delay of a given circuit path increases up to the value of the 3σ distribution of the fault-free circuit due to process variations. This dynamic critical resistance actually defines the detectability range of the defect. More specifically for an open defect, a defect with an open resistance below this value is non-detectable since it cannot be distinguished from a fault-free circuit while a defect with an open resistance higher than this value can be detected by a delay test. On the contrary for a short defect, a defect with a short resistance higher than this value is non-detectable since it cannot be distinguished from a fault-free circuit while a defect with a short resistance smaller than this value can be detected by a delay test.

We adopt a similar approach but instead of performing time-consuming Monte-Carlo simulations in order to determine the 3σ distribution of the fault-free circuit, we simply perform a single corner simulation using the Slow-Slow process corner in order to determine the worst-case delay $T_{SS}$ of the fault-free circuit. We then define the critical resistance $R_C$ as the value of the defect resistance for which the delay of a given circuit path increases up to the value of the worst-case delay for the fault-free circuit. Note that this simplification is justified by the fact that the goal of this chapter is not to guarantee the detection of a given defect by using delay testing, but to identify the operating conditions that permits to improve the detectability range of the defect.




**(A)**




**(B)**

**Figure 4.2: Defect detectability in the context of delay-based test (A) Resistive open defect (B) Resistive short defect.**

This approach is illustrated in Figures 4.2(A) and 4.2(B) which show the delay variation according to the value of the defect resistance, for a resistive open and a resistive short respectively. In case of an open defect, the extra delay due to the presence of the defect linearly increases with the value of the defect resistance, as observed in [74]. Indeed in first approximation, we can consider that the defect mainly impacts the delay of the driving gate at the location of the defect by adding an additional

resistance to the PMOS pull-up resistance of INV-2; the delay of this gate therefore linearly increases with the value of the defect resistance. In case of a short defect, the situation is more complex since the presence of the defect creates a resistor divider formed by the resistance of the driving transistor of INV-2 (PMOS pull-up resistance in case of short-to-ground and rise transition, and NMOS pull-down resistance in case of short-to-$V_{DD}$ and fall transition) and the defect resistance $R_{SH}$. The impact of the defect therefore depends on the competition between these two resistors. The extra delay due to the presence of the defect is actually dependent on the inverse of the defect resistance and therefore exhibits strong increase as the defect resistance decreases, as expressed in [74] and [76].

Despite this different behavior, the same concept of critical resistance can be used to define the detectability range. However, note that the detectability region is opposite in case of an open or a short defect. In case of an open defect, the smaller the value of the critical resistance, the larger the detectability range. Optimal conditions that improve the detectability range of an open defect are therefore operating conditions that minimize the value of the critical resistance. On the contrary in case of a short defect, the higher the critical resistance, the larger the detectability range. Optimal conditions that improve the detectability range of a short defect are therefore operating conditions that maximize the value of the critical resistance.

## 4.4 SIMULATION RESULTS

A number of electrical transient simulations of the circuit under test have been performed considering various operating conditions. In particular, we have considered 3 different values of the power supply voltage, corresponding to nominal power supply (Nom-$V_{DD}$=1V), low power supply (Low-$V_{DD}$=0.8V) and high power supply (High-$V_{DD}$=1.2V). For each value of the power supply voltage, the circuit has been simulated with no body-biasing (NBB) and using either reverse or forward body biasing (RBB or FBB). On the total, we therefore have 9 different operating conditions. We recall that the range of reverse and forward body biasing is different for RVT and LVT devices: $V_{BB}$=-1.8V for RBB and $V_{BB}$=0.8V for FBB in case of RVT devices, while $V_{BB}$=-0.3V for RBB and $V_{BB}$=1.8V for FBB in case of LVT devices.

**Table 4.1: Typical and worst-case delay of the fault-free circuit under various operating conditions – RVT implementation (A) Rise Transition (B) Fall Transition.**

| Delay | Low – $V_{DD}$ | | | Nom – $V_{DD}$ | | | High – $V_{DD}$ | | |
|---|---|---|---|---|---|---|---|---|---|
| | RBB | NBB | FBB | RBB | NBB | FBB | RBB | NBB | FBB |
| $T_{TYP}$ (ps) | 48.5 | 26.8 | 21.9 | 23.8 | 16.9 | 14.9 | 16.4 | 13.1 | 12.0 |
| $T_{SS}$ (ps) | 59.2 | 31.0 | 24.9 | 26.6 | 18.8 | 16.4 | 18.3 | 14.3 | 13.1 |

**(A)**

| Delay | Low – $V_{DD}$ | | | Nom – $V_{DD}$ | | | High – $V_{DD}$ | | |
|---|---|---|---|---|---|---|---|---|---|
| | RBB | NBB | FBB | RBB | NBB | FBB | RBB | NBB | FBB |
| $T_{TYP}$ (ps) | 51.5 | 27.6 | 22.5 | 24.4 | 17.5 | 15.5 | 17.3 | 13.8 | 12.7 |
| $T_{SS}$ (ps) | 62.3 | 31.6 | 25.3 | 27.5 | 19.4 | 17.0 | 18.9 | 15.0 | 13.7 |

**(B)**

**Table 4.2: Typical and worst-case delay of the fault-free circuit under various operating conditions – LVT implementation (A) Rise Transition (B) Fall Transition.**

| Delay | Low – $V_{DD}$ | | | Nom – $V_{DD}$ | | | High – $V_{DD}$ | | |
|---|---|---|---|---|---|---|---|---|---|
| | RBB | NBB | FBB | RBB | NBB | FBB | RBB | NBB | FBB |
| $T_{TYP}$ (ps) | 21.9 | 20.1 | 12.7 | 14.3 | 13.5 | 9.5 | 11.1 | 10.5 | 8.1 |
| $T_{SS}$ (ps) | 24.0 | 21.9 | 13.8 | 15.5 | 14.6 | 10.3 | 11.9 | 11.3 | 8.6 |

**(A)**

| Delay | Low – $V_{DD}$ | | | Nom – $V_{DD}$ | | | High – $V_{DD}$ | | |
|---|---|---|---|---|---|---|---|---|---|
| | RBB | NBB | FBB | RBB | NBB | FBB | RBB | NBB | FBB |
| $T_{TYP}$ (ps) | 22.4 | 20.5 | 13.3 | 14.8 | 14.0 | 10.2 | 11.6 | 11.1 | 8.7 |
| $T_{SS}$ (ps) | 24.5 | 22.4 | 14.3 | 16.0 | 15.0 | 11.0 | 12.4 | 11.9 | 9.3 |

**(B)**

First, we have simulated the fault-free circuit under the different operating conditions, using either the Typical (TT) or Slow-Slow (SS) process corner and considering both rising and falling transitions. Results are summarized in Tables 4.1 and

4.2 that report the typical delay ($T_{TYP}$) and worst-case delay ($T_{SS}$) of the inverter chain, for RVT and LVT implementations respectively.

These results are in agreement with expected trends, i.e. an increase of the typical delay for lower $V_{DD}$ and a decrease for higher $V_{DD}$. The degradation in delay is more pronounced than the speedup since a 20% reduction of $V_{DD}$ induces a delay degradation of about 50% while a 20% increase of $V_{DD}$ induces a delay improvement of about 20%. Regarding the influence of body biasing, RBB induces an increase of the typical delay while FBB results in a speed-up. The influence of RBB is more pronounced in case of RVT implementation because the applied RBB voltage is higher for RVT devices than LVT ones. In the same way, the influence of FBB is more pronounced in case of LVT implementation because the applied FBB voltage is higher for LVT devices than RVT ones. The maximum reduction in delay compared to nominal supply voltage without body-biasing conditions (Nom-$V_{DD}$ and NBB) is obtained by combining High-$V_{DD}$ and FBB, with a reduction of around 30% for RVT implementation and 40% for LVT. On the other hand, the maximum increase in delay with respect to Nom-$V_{DD}$ and NBB is observed for Low-$V_{DD}$ combined with RBB, with an increase around 190% for RVT implementation and 60% for LVT. Regarding the impact of process variations under the different operating conditions, it can be observed that the difference between the worst-case delay and the typical one actually follows the same trends, i.e. the higher the typical delay, the higher this difference. Finally note that as expected, LVT implementation exhibits better speed performance than RVT implementation, with a reduction of about 3.5ps of the typical delay under nominal operating conditions (i.e. 20%), more than 20ps (55%) for the slowest operating conditions (Low-$V_{DD}$ combined with RBB) and 3ps (30%) for the fastest case (High-$V_{DD}$ combined with FBB).

Then for each defect type, we have simulated the defective circuit varying the value of the defect resistance and we have determined the values of the corresponding critical resistance under the different operating conditions. Results are reported in Tables 4.3 and 4.4 for RVT and LVT implementations respectively.

**Table 4.3: Critical Resistance $R_C$ (in kΩ) of the defective circuit under various operating conditions – RVT implementation.**

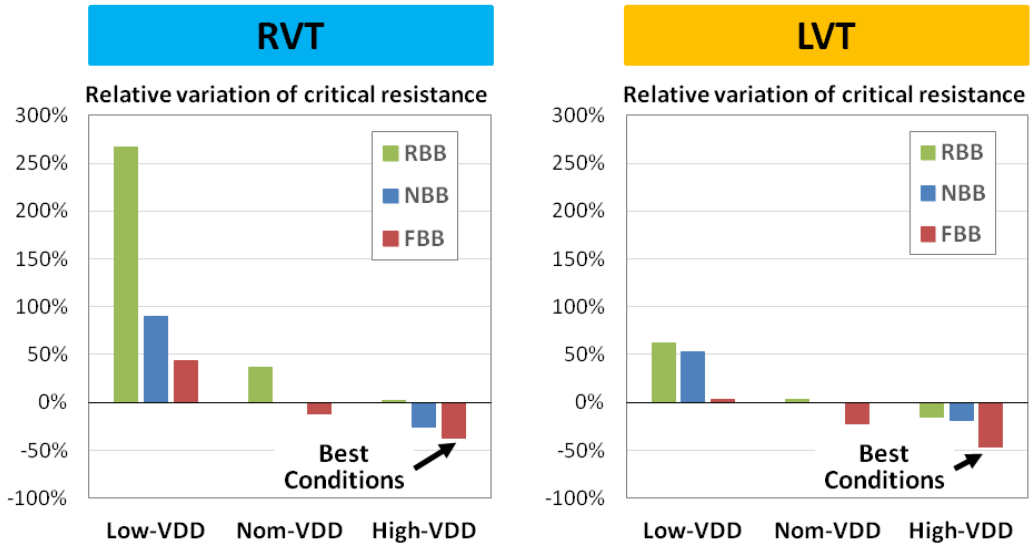
| Defect Type | Low – $V_{DD}$ | | | Nom – $V_{DD}$ | | | High – $V_{DD}$ | | |
|---|---|---|---|---|---|---|---|---|---|
| | RBB | NBB | FBB | RBB | NBB | FBB | RBB | NBB | FBB |
| Open (Rise T) | 20.9 | 10.8 | 8.2 | 7.8 | 5.7 | 5.0 | 5.8 | 4.2 | 3.6 |
| Open (Fall T) | 14.5 | 7.7 | 6.1 | 6.2 | 4.7 | 4.3 | 4.4 | 3.7 | 3.4 |
| Short-to-GND | 73.0 | 34.0 | 26.0 | 32.0 | 19.5 | 17.0 | 18.0 | 15.0 | 14.0 |
| Short-to-$V_{DD}$ | 33.5 | 20.5 | 17.5 | 18.5 | 13.0 | 11.5 | 13.5 | 10.5 | 10.0 |

**Table 4.4: Critical Resistance $R_C$ (in kΩ) of the defective circuit under various operating conditions – LVT implementation.**

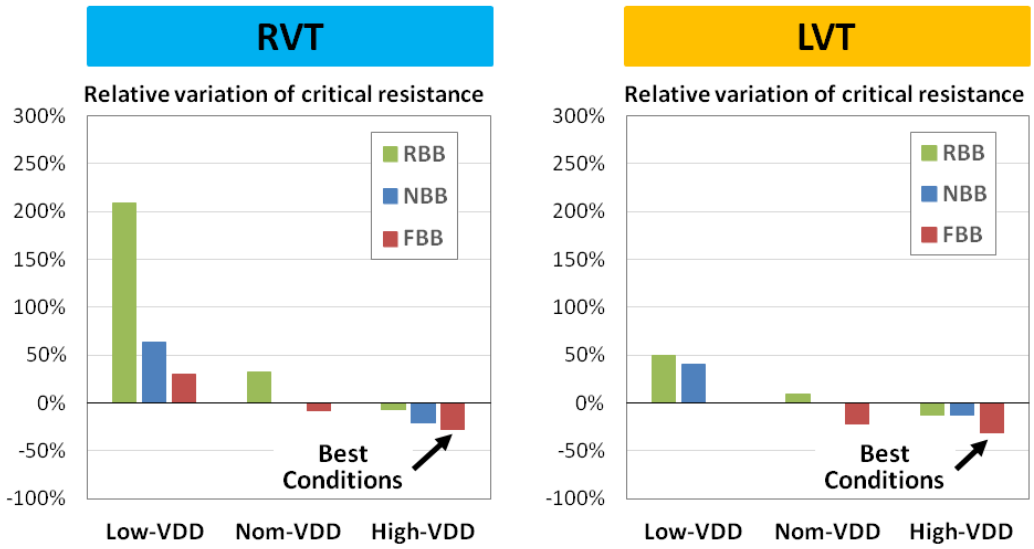
| Defect Type | Low – $V_{DD}$ | | | Nom – $V_{DD}$ | | | High – $V_{DD}$ | | |
|---|---|---|---|---|---|---|---|---|---|
| | RBB | NBB | FBB | RBB | NBB | FBB | RBB | NBB | FBB |
| Open (Rise T) | 5.2 | 4.9 | 3.3 | 3.3 | 3.2 | 2.5 | 2.7 | 2.6 | 1.7 |
| Open (Fall T) | 4.8 | 4.5 | 3.2 | 3.5 | 3.2 | 2.5 | 2.8 | 2.8 | 2.2 |
| Short-to-GND | 32.0 | 29.0 | 16.0 | 18.0 | 17.0 | 11.5 | 13.4 | 13.0 | 11.0 |
| Short-to-$V_{DD}$ | 23.5 | 21.0 | 13.3 | 14.0 | 13.5 | 10.5 | 11.3 | 10.8 | 10.0 |

From these results, we can identify the operating conditions that optimize defect detection, by looking at the minimum value of the critical resistance for an open defect and the maximum value of the critical resistance for a short defect. Whatever the implementation, i.e. RVT or LVT, it clearly appears that the best operating conditions for the detection of an open defect are High-$V_{DD}$ combined with FBB while the best operating conditions for the detection of a short defect are Low-$V_{DD}$ combined with RBB. Moreover for an open defect, even if both a rising or falling transition permits to sensitize the defect, slightly improved results are observed with a falling transition in case of RVT implementation and with a rising transition in case of LVT implementation. A refined analysis of these results can be performed by looking more in detail at the influence of $V_{DD}$ and body biasing on the value of the critical resistance. Towards this aim, Figures 4.3 to 4.5 show, for each type of defect, the relative variation of the critical resistance for the three different conditions of power supply, considering

in each case the use of RBB, NBB and FBB. These graphs clearly show that whatever the defect type and whatever the implementation, low power supply results in an increase of the critical resistance (positive relative variation) whereas high power supply results in a decrease of the critical resistance (negative relative variation). In the same way, it clearly appears that compared to the case without body biasing, RBB tends to increase the critical resistance whereas FBB tends to reduce it. However, the relative contribution of these parameters depends on the defect type and the implementation type.




**(A)**




**(B)**

**Figure 4.3: Variations of the critical resistance for the different operating conditions - Resistive open defect (A) Rise Transition (B) Fall Transition.**

For an open defect, improvement of the detectability range implies a reduction of the critical resistance. High-$V_{DD}$ and FBB are therefore the most favorable conditions. However, it can be seen in Figure 4.3 that FBB has a moderate impact and that most of the improvement comes from High-$V_{DD}$ in case of RVT implementation. In contrast, the individual influence of High-$V_{DD}$ and FBB are in the same range in case of LVT implementation (around 20%) and substantial improvement is achieved by combining both parameters. This difference can be explained by the fact that RVT devices have a limited FBB range to prevent the conduction of the P-well/N-well diode while LVT devices can support large FBB voltage.

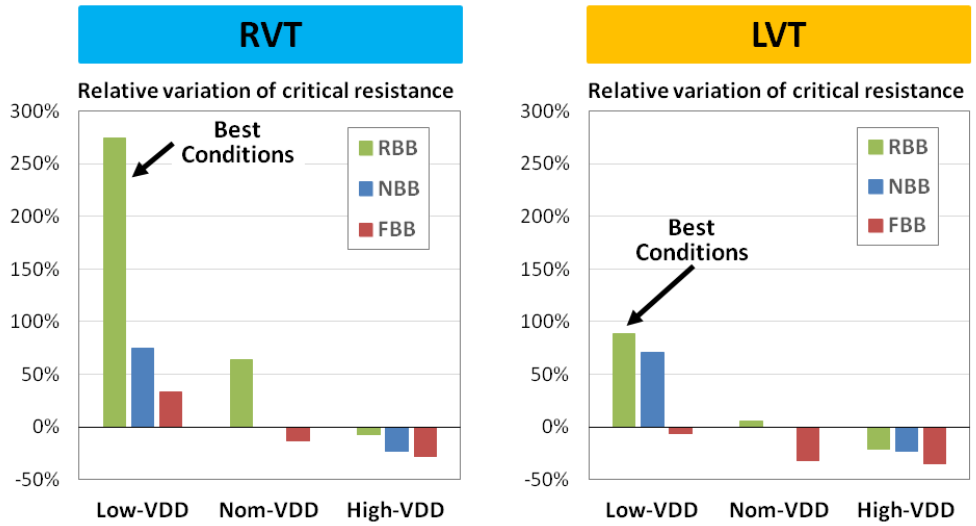



**Figure 4.4: Variations of the critical resistance for the different operating conditions - Resistive short-to-GND defect**

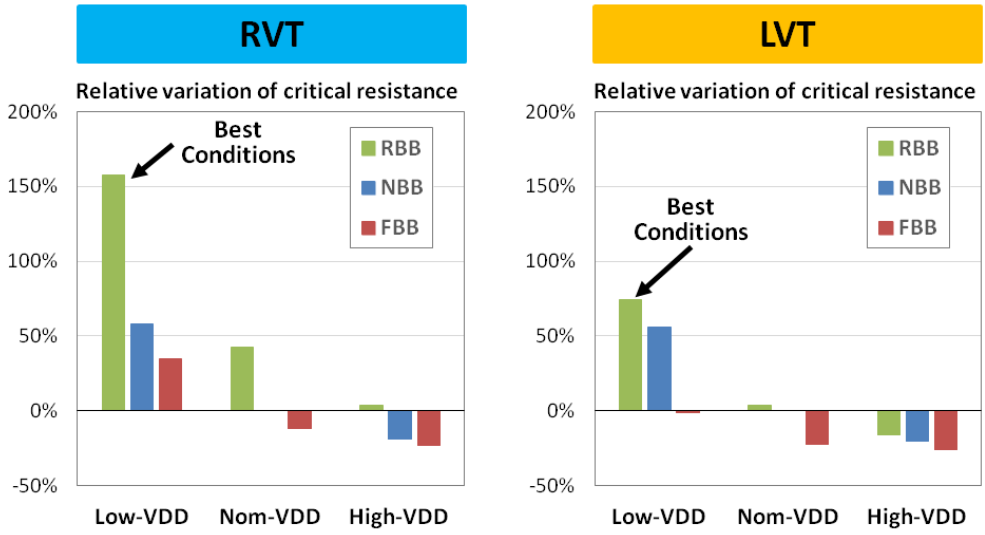



**Figure 4.5: Variations of the critical resistance for the different operating conditions - Resistive short-to-$V_{DD}$ defect.**

For a short defect, improvement of the detectability range implies an increase of the critical resistance. Low-$V_{DD}$ and RBB are therefore the most favorable conditions. Still, it can be observed that the contribution of these parameters differs depending on the implementation type. In case of RVT implementation, the individual influence of Low-$V_{DD}$ and RBB are in the same range and an extremely large improvement is achieved by combining both parameters.

In case of LVT implementation, RBB by itself has a minor influence compared to Low-$V_{DD}$ and the improvement obtained by combining both parameters is less significant. Here again, this difference comes from the fact that the RBB range is limited for LVT devices to avoid the conduction of the P-well/N-well diode while RVT devices can support large RBB voltage.

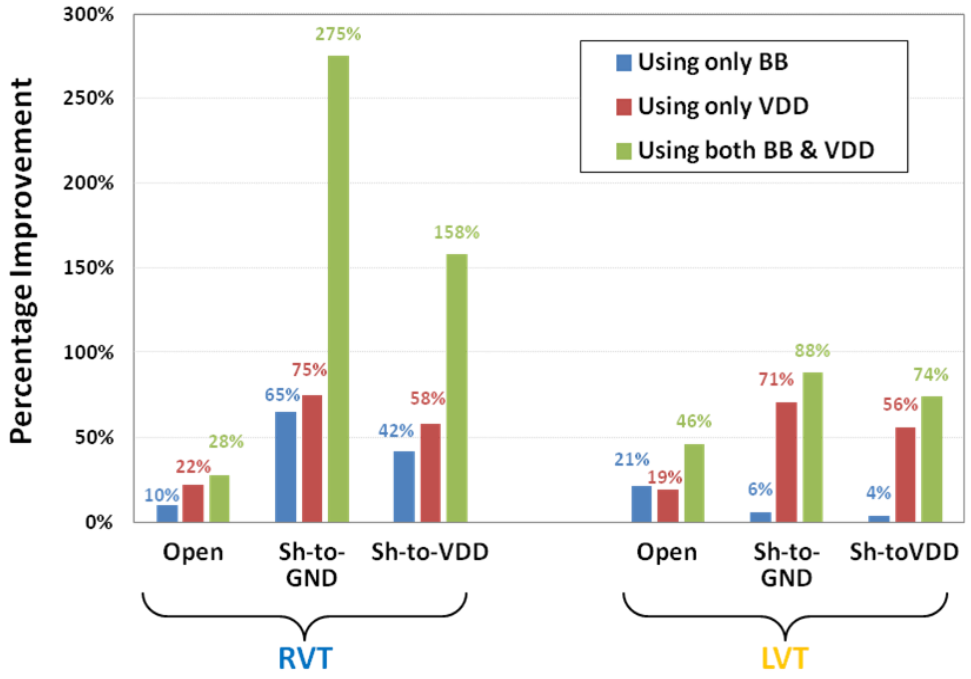



**Figure 4.6: Improvement in detection brought by $V_{DD}$ and body biasing conditions.**

Figure 4.6 summarizes all these results by showing the percentage of improvement in detection achieved by using only body biasing, only power supply or the combination of both for the different defect types in case of RVT and LVT implementations. This figure clearly highlights that the combination of $V_{DD}$ and body biasing is particularly interesting for the detection of short defects in case of RVT implementation and open defects in case of LVT implementation, with a major improvement compared to the situation where only $V_{DD}$ or body biasing are used. It also shows that the percentage improvement in detection achieved under the best conditions

is more significant for short defects than open ones. Indeed, the improvement for short defects is higher than 150% in RVT and 70% in LVT while the improvement for open defects is around 30% in RVT and 40% in LVT.

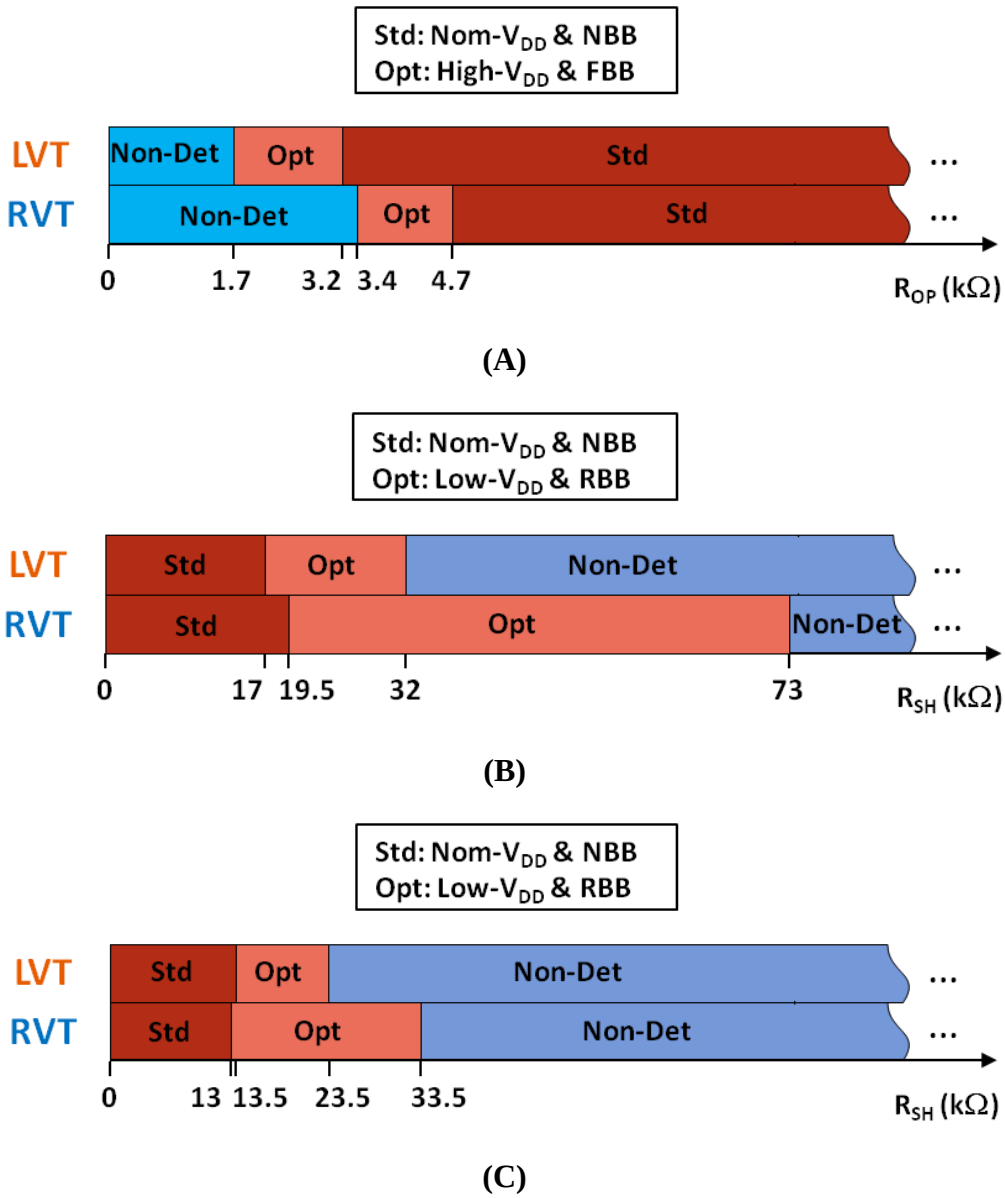



**Figure 4.7: Defect detectability range under standard and optimized operating conditions (A) Resistive open defect (B) Resistive short-to-GND (C) Resistive short-to-$V_{DD}$.**

To conclude this study, Figure 4.7 compares the detectability range achieved under standard and optimized conditions for the three investigated defects and the two types of implementations. The main outcome is that substantial improvement of the detectability range can be achieved by using appropriate conditions, and that these conditions depend on the defect type, i.e. High-$V_{DD}$ and FBB for resistive opens and

Low-$V_{DD}$ and RBB for resistive shorts. Then for a given defect, differences can be pointed out depending on the implementation.

In case of open defect, LVT implementation offers better detectability properties than RVT implementation, with a value of the critical resistance 1.5 time lower under standard conditions and twice lower under optimized conditions. In case of short defect, RVT and LVT implementations have similar detectability properties under standard conditions with a value of the critical resistance in the same range, i.e. around 18kΩ for short-to-ground and 13kΩ for short-to-$V_{DD}$. However, there is a clear advantage for RVT implementation over LVT one under optimized conditions with a detectability range more than twice larger in case of short-to-ground defect and around 1.5 times larger in case of short-to-$V_{DD}$ defect. Finally, it can be noticed that short-to-ground defects exhibit a twice larger detectability range than short-to-$V_{DD}$ defects.

## 4.5 SUMMARY

This chapter has presented a thorough analysis for the detection of weak resistive open and short defects in the context of delay test, considering the individual and combined improvement in detection brought by Body Biasing (BB) and supply voltage ($V_{DD}$). Simulations have been carried out using HSPICE with 28nm FDSOI-RVT and FDSOI-LVT gate libraries. Estimation of the critical resistance is based on the difference in the values of the delays using *Slow* and *Typical* process corners. Results show that higher supply voltage and FBB improves detectability of resistive opens while lower supply voltage and RBB improves the detectability of resistive shorts. It has also been demonstrated that circuits implemented with FDSOI-LVT transistors facilitates the detection of weak resistive opens while the circuits implemented with FDSOI-RVT transistors facilitates the detection of weak resistive shorts, with a higher detectability for resistive short-to-ground than short-to-$V_{DD}$ defects.

# 5 Impact of Process Variation on the Detectability of Resistive Short Defects: 28nm Bulk Vs. FDSOI Technologies

# 5.1 INTRODUCTION

The study of resistive defects in presence of process variations stands as an important issue for the emerging nanometer technologies. Such defects have been largely studied in the literature in case of the traditional Bulk technology. Using 45nm and 65nm gate libraries, the impact of process, voltage and temperature variations on delay test of resistive open and resistive bridge defects was shown in [77]. The influence of $V_{DD}$ and body biasing has also been investigated in [75], [76]. In [78], a comparative analysis of bulk, FDSOI and FinFET technologies in presence of a resistive short defect is performed, but without considering process variations. In [79], a more detailed analysis of resistive short in FDSOI is realized, in particular regarding the influence of $V_{DD}$, temperature and body biasing, but again the impact of process variations was not included. The comparative studies of 28nm Bulk and FDSOI in terms of ultra-low power design, self-heating etc. have already been published [80], [81]. However to the best of our knowledge, the studies have not yet focused on their comparative testability properties in presence of process variations.

In this chapter, we focus on the detectability of resistive short to ground (GND) and resistive short to power supply ($V_{DD}$) for 28nm Bulk and FDSOI technologies under the presence of process variations, in the context of a logic-based test. This study is performed based on Cadence SPECTRE simulations using 28nm Bulk and FDSOI gate libraries. The testability properties are established for the two types of devices available in each technology, namely LP (Low Power) thin oxide Regular-$V_T$ (LR) and LP thin oxide Low-$V_T$ (LL) in Bulk, and Regular-$V_T$ (RVT) and Low-$V_T$ (LVT) in UTBB (Ultra Thin Body and Buried oxide) FDSOI. In order to deduce a reasonable comparison, FDSOI-RVT is compared with Bulk-LR and FDSOI-LVT is compared with Bulk-LL. The defect detectability range is analyzed under nominal operating conditions, i.e. nominal-$V_{DD}$ and No Body-Biasing (NBB), but also under low-$V_{DD}$ and Reverse Body-Biasing (RBB) as these conditions are favorable conditions for the detection of resistive short defects [79].

The chapter is organized as follows: Section 5.2 focuses on the simulation setup and extends the concept of critical resistance in order to define robust detectability range. Section 5.3 presents a first analysis of the impact of process variations on the distribution of the critical resistance, based only on Monte-Carlo simulations of the

standard elementary inverter performed with Cadence SPECTRE and simple analytical models. Defect detectability ranges are then quantified in Section 5.4, and the impact of process variations on the achieved detectability ranges is commented for each implementation type and each operation condition. Finally, some conclusions and perspectives are drawn in Section 5.5.

## 5.2 CIRCUIT UNDER TEST AND DEFECT DETECTION IN PRESENCE OF PROCESS VARIATIONS

In order to study the detection of resistive short defects, we consider a simple didactic circuit composed of a chain of four inverters (INV-1 to INV-4) as explained in Chapter 3 and 4. Two different defects are studied, which consist of a resistive short to ground (GND) and resistive short to power supply ($V_{DD}$). The defect is inserted in the middle of the inverter chain and the setups associated to the study are as shown in Figure 5.1 (A) and (B).

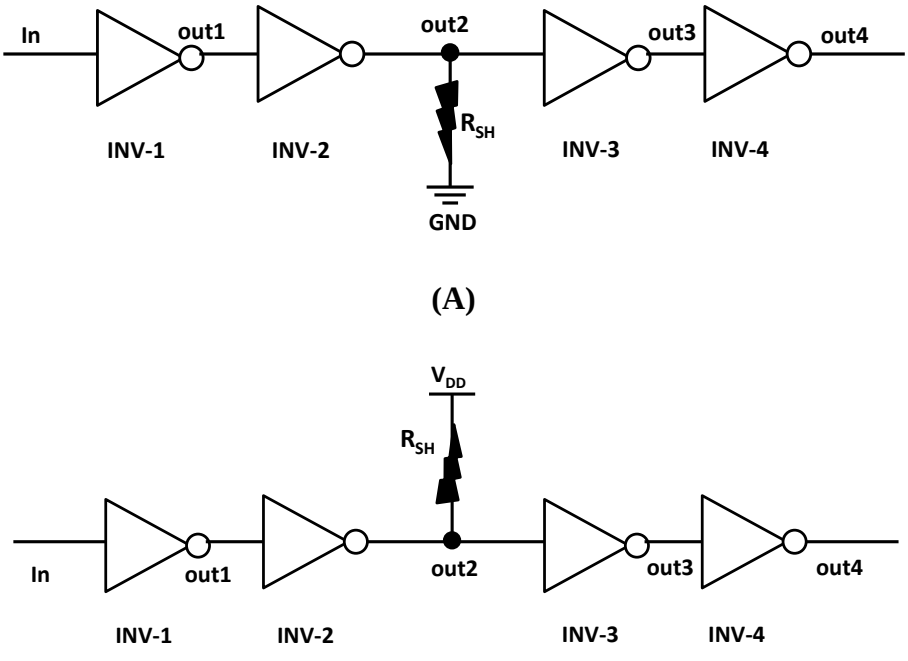



**Figure 5.1: Circuit under test**
**(A) Resistive short-to-GND and (B) Resistive short-to-$V_{DD}$.**

In case of a resistive short-to-GND, a variable resistance $R_{SH}$ is inserted between the output of INV-2 (out2) and the ground terminal (GND); a high logic level is applied to the inverter chain input (In) in order to sensitize the defect. In case of a resistive short-to-$V_{DD}$, a variable resistance $R_{SH}$ is inserted between the output of INV-2 (out2) and the power supply terminal ($V_{DD}$); a low logic level is applied to the inverter chain input (In) in order to sensitize the defect.

To infer on the comparative study of defect detectability in Bulk and FDSOI, four versions of the simple didactic circuit are implemented considering Bulk-LR, FDSOI-RVT, Bulk-LL, and FDSOI-LVT devices. In all cases, standard elementary inverters from the 28nm gate library are used.

As in Chapter 2 and 3, the concept of critical resistance is used to quantify the defect detectability range. However up to now, the value of the critical resistance $R_C$ has been determined from electrical simulations performed under typical process conditions. This actually leads to an optimistic measure of the defect detectability range. To illustrate this point, we have simulated the defective circuit in presence of process variations. More precisely, we have generated 1000 instances of the circuit under test using Monte-Carlo simulation and we have simulated these 1000 instances varying the value of the short resistance $R_{SH}$ between 0kΩ and 20kΩ with a step of 100Ω. For each circuit instance, we have then recorded the value of the critical resistance, i.e. the maximum value of the short resistance that creates a logic fault. From this, we can obtain the distribution of the critical resistance induced by process variations, as depicted in Figure 5.2 in case of short-to-GND defect and Bulk-LR implementation. We have also recorded for each simulated value of the short resistance, the number of instances that present a logic fault. Results are reported in Figure 5.3 for short-to-GND defect and Bulk-LR implementation.

These figures clearly illustrate that the critical resistance determined under typical process conditions leads to an optimistic measure of the defect detectability range. Indeed, the detectability range established under typical process conditions is the interval $[0, R_C]$, where $R_C$ corresponds to the mean value of the distribution. However in presence of process variations, only 50% of the circuits affected by a defect with a short resistance $R_{SH}$ equal to $R_C$ actually exhibit a logic fault. Furthermore, it exists some with a short resistance $R_{SH}$ lower than $R_C$ that does not exhibit a logic fault. Defect

detection is therefore not truly guaranteed in the full range, in presence of process variations.

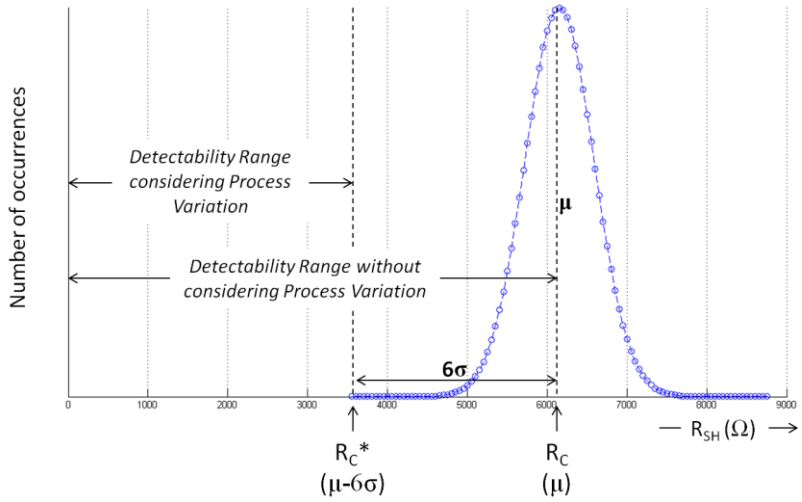



**Figure 5.2: Distribution of critical resistance in presence of process variations.**

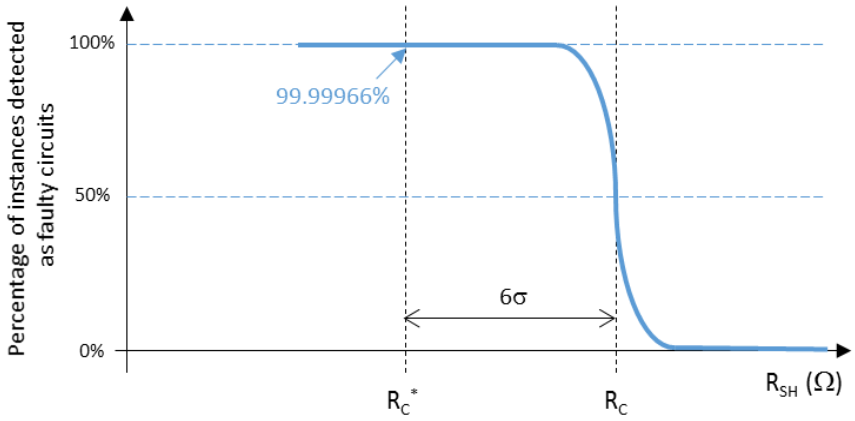



**Figure 5.3: Percentage of instances detected as faulty circuits vs. value of the short resistance.**

In this context, a more robust measure of the detectability range can be defined by considering the interval $[0, R_C{}^*]$, with $R_C{}^*$ expressed as:

$$R_C{}^* = R_C - \alpha\sigma_{R_C} \qquad 5.1$$

Where $\sigma_{R_C}$ corresponds to the standard deviation of the critical resistance distribution, and $\alpha$ is a custom parameter that can be adjusted to specify the confidence level of defect defection guarantee. In this chapter, we use $\alpha = 6$, which means that

more than 99.99966% of the defects with a short resistance lower than $R_C{}^*$ will definitely produce a logic fault.

This new definition permits to assure defect detection in the full detectability range by incorporating the impact of process variations. Obviously, the detectability range determined considering process variations is smaller than the detectability range determined using only typical process conditions. The larger the spread of the distribution induced by process variations, the stronger the reduction in the detectability range.

## 5.3 IMPACT OF PROCESS VARIATIONS ON CRITICAL RESISTANCE DISTRIBUTION

In this section, we focus on the comparative analysis of Bulk and FDSOI technologies, with respect to the impact of process variations on the distribution of the critical resistance associated to short-to-GND and short-to-$V_{DD}$ defects.

This analysis is conducted using the analytical models proposed in [82] for the estimation of the critical resistance:

$$R_{C-GND} = \beta \cdot R_{P-ON} \quad 5.2$$

$$R_{C-VDD} = R_{N-ON}/\beta \quad 5.3$$

$$\beta = \frac{1}{\left(\frac{V_{DD}}{V_{TH}} - 1\right)} \quad 5.4$$

Where, $R_{P-ON}$ corresponds to the ON-resistance of the conducting P-transistor of INV-2, $R_{N-ON}$ to the ON-resistance of the conducting N-transistor of INV-2, and $V_{TH}$ is the logic threshold of INV-3. These expressions reveal that the critical resistance depends, on the one hand, on the ON-resistance of the conducting transistor of the driving gate, and on the other hand, on the ratio between the supply voltage and the logic threshold of the driven gate. A key interest of these expressions is that they give an estimation of the critical resistance independently of the defect, based only on fault-free simulation of elementary devices. Hence, these expressions can be utilized to analyze the impact of process variations on the detectability of resistive short defects without performing any fault simulation.

For this, we need to determine the dispersion in the distribution of $R_C$ induced by process variations. A classical measure of this dispersion is the Coefficient of Variation $CV$, which is defined as the ratio of the standard deviation $\sigma$ to the mean $\mu$:

$$\mathrm{CV} = \sigma/\mu \qquad 5.5$$

This coefficient is a dimensionless number (often expressed in percentage) that quantifies the extent of variability in relation to the mean of the population. This coefficient is particularly useful to compare the variability of distributions with different means, which is the case in our study for the different implementations in Bulk and FDSOI.

In first approximation, assuming that $R_{ON}$ and $\beta$ are independent variables and based on combined standard uncertainty calculations, we can use the following equation for an estimation of the coefficient of variation of the critical resistance [83]:

$$\widehat{\mathrm{CV}}_{R_C} \approx \sqrt{{\mathrm{CV}_\beta}^2 + {\mathrm{CV}_{R_{ON}}}^2} = \sqrt{\left(\frac{\sigma_\beta}{\mu_\beta}\right)^2 + \left(\frac{\sigma_{R_{ON}}}{\mu_{R_{ON}}}\right)^2} \qquad 5.6$$

Where, $R_{ON} = R_{P-ON}$ in case of a short-to-GND defect and $R_{ON} = R_{N-ON}$ in case of a short-to-$V_{DD}$ defect.

Practically, to determine the coefficient of variation of the critical resistance associated with the two types of defect, we have performed Monte-Carlo simulations of the standard elementary inverter (cf. simulation setup defined in Chapter 3), using a population of 1000 instances for each implementation type (Bulk-LR, Bulk-LL, FDSOI-RVT and FDSOI-LVT). The study has been performed for two values of power supply corresponding to Nom-$V_{DD}$=1V and Low-$V_{DD}$=0.8V, since it has been shown that detectability of resistive short defects is enhanced by low-$V_{DD}$ condition [75], [79]. Moreover for FDSOI, the use of Reverse Body-Biasing (RBB) has been considered since it has been shown that this condition also improves the detectability of resistive short defects [79], [82]. For each implementation type and each operating condition, we have recorded the mean and standard deviation of the parameters $R_{P-ON}$ , $R_{N-ON}$ and $\beta$ as shown in Tables 5.1 to 5.4.

**Table 5.1: Mean and Standard Deviation of $R_{P-ON}$ , $R_{N-ON}$ and $\beta$ under different operating conditions for BULK-LR.**

| Bulk–LR | | | | | | |
|---|---|---|---|---|---|---|
| Operating Condition | $R_{P\text{-}ON}$ (kΩ) | | $R_{N\text{-}ON}$ (kΩ) | | β | |
| | μ | σ | μ | σ | μ | σ |
| Nom-$V_{DD}$ | 6.03 | 0.37 | 5.20 | 0.43 | 1.02 | 0.05 |
| Low-$V_{DD}$ | 10.80 | 1.06 | 9.52 | 1.32 | 1.03 | 0.07 |

**Table 5.2: Mean and Standard Deviation of $R_{P-ON}$ , $R_{N-ON}$ and $\beta$ under different operating conditions for FDSOI-RVT.**

| F**DSOI–**RVT | | | | | | |
|---|---|---|---|---|---|---|
| Operating Condition | $R_{P\text{-}ON}$ (kΩ) | | $R_{N\text{-}ON}$ (kΩ) | | β | |
| | μ | σ | μ | σ | μ | σ |
| Nom-$V_{DD}$ | 6.41 | 0.28 | 3.61 | 0.17 | 0.84 | 0.03 |
| Nom-$V_{DD}$ + RBB | 8.82 | 0.50 | 4.47 | 0.22 | 0.86 | 0.03 |
| Low-$V_{DD}$ | 10.19 | 0.72 | 4.81 | 0.31 | 0.85 | 0.05 |
| Low-$V_{DD}$ + RBB | 19.27 | 2.00 | 7.20 | 0.66 | 0.84 | 0.04 |

**Table 5.3: Mean and Standard Deviation of $R_{P-ON}$ , $R_{N-ON}$ and $\beta$ under different operating conditions for BULK-LL.**

| B**ulk–**LL | | | | | | |
|---|---|---|---|---|---|---|
| Operating Condition | $R_{P\text{-}ON}$ (kΩ) | | $R_{N\text{-}ON}$ (kΩ) | | β | |
| | μ | σ | μ | σ | μ | σ |
| Nom-$V_{DD}$ | 5.03 | 0.26 | 4.21 | 0.30 | 1.02 | 0.05 |
| Low-$V_{DD}$ | 7.71 | 0.58 | 6.71 | 0.71 | 1.03 | 0.06 |

**Table 5.4: Mean and Standard Deviation of $R_{P-ON}$ , $R_{N-ON}$ and $\beta$ under different operating conditions for FDSOI-LVT.**

| FDSOI–LVT | | | | | | |
|---|---|---|---|---|---|---|
| Operating Condition | $R_{P\text{-}ON}$ (kΩ) | | $R_{N\text{-}ON}$ (kΩ) | | β | |
| | μ | σ | μ | σ | μ | σ |
| Nom-$V_{DD}$ | 4.22 | 0.178 | 3.37 | 0.20 | 0.93 | 0.04 |
| Nom-$V_{DD}$ + RBB | 4.45 | 0.19 | 3.51 | 0.21 | 0.95 | 0.04 |
| Low-$V_{DD}$ | 6.52 | 0.42 | 4.53 | 0.34 | 0.96 | 0.05 |
| Low-$V_{DD}$ + RBB | 7.10 | 0.48 | 4.88 | 0.38 | 0.97 | 0.05 |

Once the mean and standard deviation of the parameters $R_{P-ON}$ , $R_{N-ON}$ and $\beta$ are known, we can then compute their coefficient of variation according to Eq. (5.5) and the estimated coefficient of variation of the critical resistance $\widehat{CV}_{R_C}$ according to Eq. (5.6). To assess the validity of Eq. (5.6), we have performed additional Monte-Carlo simulations of the defective circuit. In particular for the two types of defect, for the four different implementations and for the various operating conditions, 1000 instances of the defective circuit have been simulated with Cadence SPECTRE varying the value of the short defect from 0kΩ and 20kΩ. From this, we can obtain the distribution of the critical resistance and compute the coefficient of variation $CV_{R_C}$ associated with this distribution. Results are summarized in Tables 5.5 to 5.8 for the different implementations.

**Table 5.5: Coefficient of Variation of $\beta$, $R_{P-ON}$, $R_{N-ON}$, $R_{C-GND}$ and $R_{C-VDD}$ under different operating conditions for BULK-LR.**

| | Bulk–LR | |
|---|---|---|
| | Nom – $V_{DD}$ | Low - $V_{DD}$ |
| $CV_{\beta}$ | 5.70% | 7.03% |
| $CV_{R_{P-ON}}$ | 6.08% | 9.77% |
| $CV_{R_{N-ON}}$ | 8.21% | 13.86% |
| $\widehat{CV}_{R_{C-GND}}$(Estimation) | 8.34% | 12.04% |
| $CV_{R_{C-GND}}$(Simulation) | 7.05% | 10.86% |
| $\widehat{CV}_{R_{C-VDD}}$(Estimation) | 9.99% | 15.54% |
| $CV_{R_{C-VDD}}$(Simulation) | 9.13% | 14.82% |

**Table 5.6: Coefficient of Variation of $\beta$, $R_{P-ON}$, $R_{N-ON}$, $R_{C-GND}$ and $R_{C-VDD}$ under different operating conditions for FDSOI-RVT.**

| | FDSOI–RVT | | | |
|---|---|---|---|---|
| | Nom – $V_{DD}$ | | Low - $V_{DD}$ | |
| | NBB | RBB | NBB | RBB |
| $CV_{\beta}$ | 4.57% | 4.45% | 5.86% | 5.54% |
| $CV_{R_{P-ON}}$ | 4.40% | 5.72% | 7.05% | 10.39% |
| $CV_{R_{N-ON}}$ | 4.58% | 4.98% | 6.48% | 9.16% |
| $\widehat{CV}_{R_{C-GND}}$(Estimation) | 6.35% | 7.25% | 9.17% | 11.77% |
| $CV_{R_{C-GND}}$(Simulation) | 5.56% | 6.62% | 8.21% | 11.32% |
| $\widehat{CV}_{R_{C-VDD}}$(Estimation) | 6.47% | 6.68% | 8.73% | 10.70% |
| $CV_{R_{C-VDD}}$(Simulation) | 5.66% | 6.06% | 7.84% | 10.15% |

**Table 5.7: Coefficient of Variation of $\beta$, $R_{P-ON}$, $R_{N-ON}$, $R_{C-GND}$ and $R_{C-VDD}$ under different operating conditions for BULK-LL.**

| | Bulk–LL | |
|---|---|---|
| | Nom – $V_{DD}$ | Low - $V_{DD}$ |
| $CV_{\beta}$ | 5.17% | 6.36% |
| $CV_{R_{P-ON}}$ | 5.18% | 7.48% |
| $CV_{R_{N-ON}}$ | 7.22% | 10.55% |
| $\widehat{CV}_{R_{C-GND}}$(Estimation) | 7.32% | 9.82% |
| $CV_{R_{C-GND}}$(Simulation) | 6.24% | 8.53% |
| $\widehat{CV}_{R_{C-VDD}}$(Estimation) | 8.89% | 12.32% |
| $CV_{R_{C-VDD}}$(Simulation) | 8.00% | 11.66% |

**Table 5.8: Coefficient of Variation of $\beta$, $R_{P-ON}$, $R_{N-ON}$, $R_{C-GND}$ and $R_{C-VDD}$ under different operating conditions for FDSOI-LVT.**

| | FDSOI–LVT | | | |
|---|---|---|---|---|
| | Nom – $V_{DD}$ | | Low - $V_{DD}$ | |
| | NBB | RBB | NBB | RBB |
| $CV_{\beta}$ | 4.39% | 4.37% | 5.36% | 5.34% |
| $CV_{R_{P-ON}}$ | 4.15% | 4.32% | 6.44% | 6.77% |
| $CV_{R_{N-ON}}$ | 5.86% | 5.97% | 7.50% | 7.87% |
| $\widehat{CV}_{R_{C-GND}}$(Estimation) | 6.04% | 6.15% | 8.38% | 8.62% |
| $CV_{R_{C-GND}}$(Simulation) | 5.29% | 5.39% | 7.50% | 7.78% |
| $\widehat{CV}_{R_{C-VDD}}$(Estimation) | 7.32% | 7.40% | 9.22% | 9.51% |
| $CV_{R_{C-VDD}}$(Simulation) | 6.55% | 6.66% | 8.36% | 8.71% |

Several comments arise from these tables. First, as expected, it can be observed that the impact of process variations is stronger in Bulk than FDSOI. Indeed under nominal operating conditions (i.e. Nom-$V_{DD}$ & NBB), the coefficient of variation of $\beta$ is higher by +1.1% for regular-$V_T$ implementation and +0.8% for low-$V_T$ one. In the same way, the coefficient of variation of $R_{P-ON}$ is higher by +1.7% for regular-$V_T$

implementation and +1.0% for low-$V_T$ one, and the coefficient of variation of $R_{N-ON}$ is higher by +3.6% for regular-$V_T$ implementation and +1.4% for low-$V_T$ one. Consequently, the coefficient of variation of the critical resistance is higher for Bulk than FDSOI: +1.5% for regular-$V_T$ implementation and +1% for low-$V_T$ one in case of short-to-GND defect, and +3.5% for regular-$V_T$ implementation and +1.5% for low-$V_T$ one in case of short-to-$V_{DD}$ defect. It can also be observed that this trend of higher coefficient of variation in Bulk compared to FDSOI is amplified when reducing the supply voltage. Indeed, the coefficient of variation of the critical resistance is higher by +2.7% for regular-$V_T$ implementation and +1.0% for low-$V_T$ one in case of short-to-GND defect, and +7.0% for regular-$V_T$ implementation and +3.3% for low-$V_T$ one in case of short-to-$V_{DD}$ defect. Globally from these results, we can infer that process variations will induce a stronger reduction of the Bulk detectability range compared to that of FDSOI, especially when using a reduced supply voltage.

Regarding the comparison between different implementation types, it appears that the ON-resistance of low-$V_T$ transistors is less sensitive to process variations than the one of regular-$V_T$ transistors, both in Bulk and FDSOI. Consequently, the coefficient of variation of the critical resistance is smaller for low-$V_T$ implementations than regular-$V_T$ ones, which means that we can infer a lower impact of process variations on the reduction of the defect detectability range.

Regarding the impact of process variations under different body-biasing conditions in FDSOI, the use of RBB has a minor influence on the coefficient of variation of the critical resistance under nominal supply voltage conditions, both for RVT and LVT implementations. However under reduced supply voltage conditions, the use of RBB introduces a substantial increase in the coefficient of variation of the critical resistance for RVT implementation. We therefore expect a significant impact of process variations on the detectability range in this situation. Note that when process variations are not taken into account, it has been shown in [82] that the use of low-$V_{DD}$ and RBB conditions generates a significant improvement in the detection of resistive short defects for RVT implementations, with an enlargement of the detectability range by a factor 3x in case of short-to-GND and 2x in case of short-to-$V_{DD}$. The strong impact of process variations observed in this situation might attenuate this benefit.

Finally regarding the estimation of the coefficient of variation of the critical resistance using Eq. (5.6), there is a good agreement between estimated values and the

ones determined from simulation, with a difference that remains below 1.3% whatever the implementation type and whatever the operating conditions. This is interesting because it means that the impact of process variations on the distribution of the critical resistance for resistive short defects can be accurately estimated based only on fault-free simulation of elementary devices. Still, it should be pointed out that Eq. (5.6) leads to a minor overestimation of the coefficient of variation of the critical resistance: estimated values are always slightly higher than the ones obtained from simulation (+0.8% in average). This might come from the fact that the assumption of independence between $R_{ON}$ and $\beta$ is not fully exact and that there is a kind of compensation that operates between the influences of process variations on these parameters.

## 5.4 DETECTABILITY RANGE RESULTS

In this section, we perform the comparative analysis between Bulk and FDSOI regarding the impact of process variations on the detection of resistive short defects. More precisely, we quantify the detectability range with and without considering process variations for the two types of defect (short-to-GND & short-to-$V_{DD}$), for the different implementations (regular-$V_T$ & low-$V_T$), and under different power supply and body-biasing conditions.

Detectability ranges are established on one hand, using Monte-Carlo simulation of a single standard elementary inverter and on the other hand, using Monte-Carlo simulation of the complete defective circuit with 200 different values of the short defect resistance. In the first case, estimated detectability ranges are derived from the analytical expressions of Section 5.2 with:

$$\hat{R}_{C-GND} = \mu_\beta \cdot \mu_{R_{P-ON}} \tag{5.7}$$

$$\hat{R}_{C-GND}{}^{*} = \mu_\beta \cdot \mu_{R_{P-ON}}\left(1 - \alpha \cdot \sqrt{\left(\frac{\sigma_\beta}{\mu_\beta}\right)^2 + \left(\frac{\sigma_{R_{P-ON}}}{\mu_{R_{P-ON}}}\right)^2}\right) \tag{5.8}$$

$$\hat{R}_{C-VDD} = \frac{\mu_{R_{N-ON}}}{\mu_\beta} \tag{5.9}$$

$$\hat{R}_{C-VDD}{}^{*} = \frac{\mu_{R_{N-ON}}}{\mu_{\beta}}\left(1 - \alpha \cdot \sqrt{\left(\frac{\sigma_{\beta}}{\mu_{\beta}}\right)^{2} + \left(\frac{\sigma_{R_{N-ON}}}{\mu_{R_{N-ON}}}\right)^{2}}\right) \quad 5.10$$

In the second case, detectability ranges are directly computed from the mean and standard deviation of the simulated critical resistance distribution.

$$R_{C-GND} = \mu_{R_{C-GND}} \quad 5.11$$

$$R_{C-GND}{}^{*} = \mu_{R_{C-GND}} - \alpha \cdot \sigma_{R_{C-GND}} \quad 5.12$$

$$R_{C-VDD} = \mu_{R_{C-VDD}} \quad 5.13$$

$$R_{C-VDD}{}^{*} = \mu_{R_{C-VDD}} - \alpha \cdot \sigma_{R_{C-VDD}} \quad 5.14$$

Results are commented first for regular-$V_T$ implementation, and then for low-$V_T$ implementation.

### 5.4.1 FDSOI Vs. Bulk – Regular -$V_T$ Implementations

Tables 5.9 and 5.10 report the estimated and simulated values of critical resistance (both the classical critical resistance $R_C$ established under typical process variations and the "robust" critical resistance $R_C{}^{*}$ that incorporates the impact of process variations) under different operating conditions for FDSOI-RVT and Bulk-LR implementations in case of short-to-GND defect, from these tables, we can observe:

- a very good agreement between estimated and simulated values of $R_C$ for both FDSOI and Bulk implementations with an average error below 0.1%,
- a correct agreement between estimated and simulated values of $R_C{}^{*}$ for FDSOI implementation with an average error around -8%,
- a reasonable agreement between estimated and simulated values of $R_C{}^{*}$ for Bulk implementation with an average error around -16%, so an error significantly than for FDSOI implementation.

**Table 5.9: Estimated and simulated values of critical resistance associated with short-to-GND defect under different operating conditions for FDSOI-RVT**

| FDSOI-RVT | | | | | | | |
|---|---|---|---|---|---|---|---|
| Operating Conditions | | Estim. | Simul. | *Error* | Estim. | Simul. | *Error* |
| | | $\hat{R}_{C-GND}$ (kΩ) | $R_{C-GND}$ (kΩ) | $\boldsymbol{\varepsilon_{R_{C-GND}}}$ | $\hat{R}_{C-GND}{}^{*}$ (kΩ) | $R_{C-GND}{}^{*}$ (kΩ) | $\boldsymbol{\varepsilon_{R_{C-GND}{}^{*}}}$ |
| Nom-$V_{DD}$ | NBB | 5.44 | 5.45 | *-0.14%* | 3.37 | 3.63 | *-7.23%* |
| | RBB | 7.68 | 7.68 | *-0.06%* | 4.34 | 4.63 | *-6.32%* |
| Low-$V_{DD}$ | NBB | 8.75 | 8.75 | *0.00%* | 3.94 | 4.44 | *-11.33%* |
| | RBB | 16.31 | 16.34 | *-0.16%* | 4.79 | 5.24 | *-8.68%* |

**Table 5.10: Estimated and simulated values of critical resistance associated with short-to-GND defect under different operating conditions for Bulk-LR.**

| Bulk-LR | | | | | | |
|---|---|---|---|---|---|---|
| Operating Conditions | Estim. | Simul. | *Error* | Estim. | Simul. | *Error* |
| | $\hat{R}_{C-GND}$ (kΩ) | $R_{C-GND}$ (kΩ) | $\boldsymbol{\varepsilon_{R_{C-GND}}}$ | $\hat{R}_{C-GND}{}^{*}$ (kΩ) | $R_{C-GND}{}^{*}$ (kΩ) | $\boldsymbol{\varepsilon_{R_{C-GND}{}^{*}}}$ |
| Nom-$V_{DD}$ | 6.16 | 6.15 | *0.03%* | 3.08 | 3.55 | *-13.38%* |
| Low-$V_{DD}$ | 11.20 | 11.19 | *0.10%* | 3.11 | 3.90 | *-20.29%* |

In the same way, Tables 5.11 and 5.12 report the estimated and simulated values of critical resistance under different operating conditions for FDSOI-RVT and Bulk-LR implementations in case of short-to-$V_{DD}$ defect. This time, we observe:

- a correct agreement between estimated and simulated values of $R_C$ for FDSOI implementation with an average error around 11%,
- a good agreement between estimated and simulated values of $R_C$ for Bulk implementation with an average error around -1.6%,
- a good agreement between estimated and simulated values of $R_C{}^{*}$ for FDSOI implementation with an average error around 2.6%,
- a moderate agreement between estimated and simulated values of $R_C{}^{*}$ for Bulk implementation, in particular for Low-$V_{DD}$ condition with an error that reaches -40%.

**Table 5.11: Estimated and simulated values of critical resistance associated with short-to-$V_{DD}$ defect under different operating conditions for FDSOI-RVT.**

| FDSOI-RVT | | | | | | | |
|---|---|---|---|---|---|---|---|
| Operating Conditions | | Estim. | Simul. | *Error* | Estim. | Simul. | *Error* |
| | | $\hat{R}_{C-VDD}$ (kΩ) | $R_{C-VDD}$ (kΩ) | $\boldsymbol{\varepsilon_{R_{C-VDD}}}$ | $\hat{R}_{C-VDD}{}^{*}$ (kΩ) | $R_{C-VDD}{}^{*}$ (kΩ) | $\boldsymbol{\varepsilon_{R_{C-VDD}{}^{*}}}$ |
| Nom-$V_{DD}$ | NBB | 4.26 | 3.78 | *12.60%* | 2.61 | 2.50 | *4.32%* |
| | RBB | 5.15 | 4.65 | *10.86%* | 3.08 | 2.96 | *4.35%* |
| Low-$V_{DD}$ | NBB | 5.61 | 5.07 | *10.63%* | 2.67 | 2.68 | *-0.50%* |
| | RBB | 8.52 | 7.62 | *11.70%* | 3.05 | 2.98 | *2.25%* |

**Table 5.12: Estimated and simulated values of critical resistance associated with short-to-$V_{DD}$ defect under different operating conditions for Bulk-LR.**

| Bulk-LR | | | | | | |
|---|---|---|---|---|---|---|
| Operating Conditions | Estim. | Simul. | *Error* | Estim. | Simul. | *Error* |
| | $\hat{R}_{C-VDD}$ (kΩ) | $R_{C-VDD}$ (kΩ) | $\boldsymbol{\varepsilon_{R_{C-VDD}}}$ | $\hat{R}_{C-VDD}{}^{*}$ (kΩ) | $R_{C-VDD}{}^{*}$ (kΩ) | $\boldsymbol{\varepsilon_{R_{C-VDD}{}^{*}}}$ |
| Nom-$V_{DD}$ | 5.10 | 5.16 | *-1.03%* | 2.04 | 2.33 | *-12.39%* |
| Low-$V_{DD}$ | 9.19 | 9.39 | *-2.12%* | 0.62 | 1.04 | *-40.5%* |

Globally, these results show that fairly good estimation of the critical resistance can be obtained using the proposed expressions, with better accuracy for FDSOI than Bulk especially regarding the "robust" critical resistance.

Regarding the comparison between Bulk and FDSOI in terms of detectability range, results are graphically summarized in Figures 5.4 and 5.5 (simulated values) for short-to-GND and short-to-$V_{DD}$ defect, respectively. The analysis of these figures draws several comments detailed hereafter.

Under nominal operating conditions (Nom-$V_{DD}$ & NBB), Bulk implementation exhibits slightly larger detectability ranges than FDSOI implementation when process variations are not considered. Indeed for both types of defect, we observe a higher value of the critical resistance for Bulk than FDSOI ($R_C$=6.2Ω vs. $R_C$=5.4kΩ for short-to-GND and $R_C$=5.2kΩ vs. $R_C$=3.8kΩ for short-to-$V_{DD}$). However when process variations

are incorporated in the simulation, the detectability range in Bulk is reduced by 42% for short-to-GND and 55% for short-to-$V_{DD}$, while the detectability range in FDSOI is only reduced by 33% for short-to-GND and 34% for short-to-$V_{DD}$. As a consequence, the robust detectability range is actually similar in FDSOI and Bulk for short-to-GND defect ($R_C^*$=3.6kΩ) and even slightly larger for short-to-$V_{DD}$ defect ($R_C^*$=2.5kΩ vs. $R_C^*$=2.3kΩ).

Regarding the benefit that can be achieved by using favorable operating conditions, distinction should be made between the two types of defect:

- In case of short-to-GND, the most favorable conditions are Low-$V_{DD}$ for Bulk and Low-$V_{DD}$ combined with RBB for FDSOI. This observation is valid irrespective of process variations. However, the improvement brought by these conditions significantly differs depending whether process variations are taken into account or not. Without considering process variations, the critical resistance $R_C$ increases from 6.2kΩ under standard operating conditions to 11.2kΩ under optimal operating conditions in Bulk and 5.4kΩ to 16.3kΩ in FDSOI, which corresponds to a detectability improvement of 81% and 202%. In contrast when process variations are considered, the critical resistance $R_C^*$ increases from 3.6kΩ to 3.9kΩ in Bulk and 3.6kΩ to 5.2kΩ in FDSOI, which corresponds only to a detectability improvement of 8% and 44%.
- In case of short-to-$V_{DD}$, the most favorable conditions determined without considering process variations are Low-$V_{DD}$ for Bulk and Low-$V_{DD}$ combined with RBB for FDSOI, whereas the most favorable conditions determined when considering process variations are Nom-$V_{DD}$ for Bulk and either Nom-$V_{DD}$ and RBB or Low-$V_{DD}$ combined with RBB for FDSOI. Indeed in this case, the impact of process variations is so strong for Bulk at reduced supply voltage that the value of the critical resistance at Low-$V_{DD}$ is lower than the one at Nom-$V_{DD}$ ($R_C^*$=1.0kΩ vs. $R_C^*$=2.3kΩ). In contrast because process variations are lower in FDSOI, there is still a benefit of using Low-$V_{DD}$ or/and RBB. However the detectability improvement is reduced, with only 8% improvement when using Low-$V_{DD}$ and 20% when using RBB or the combination of both.

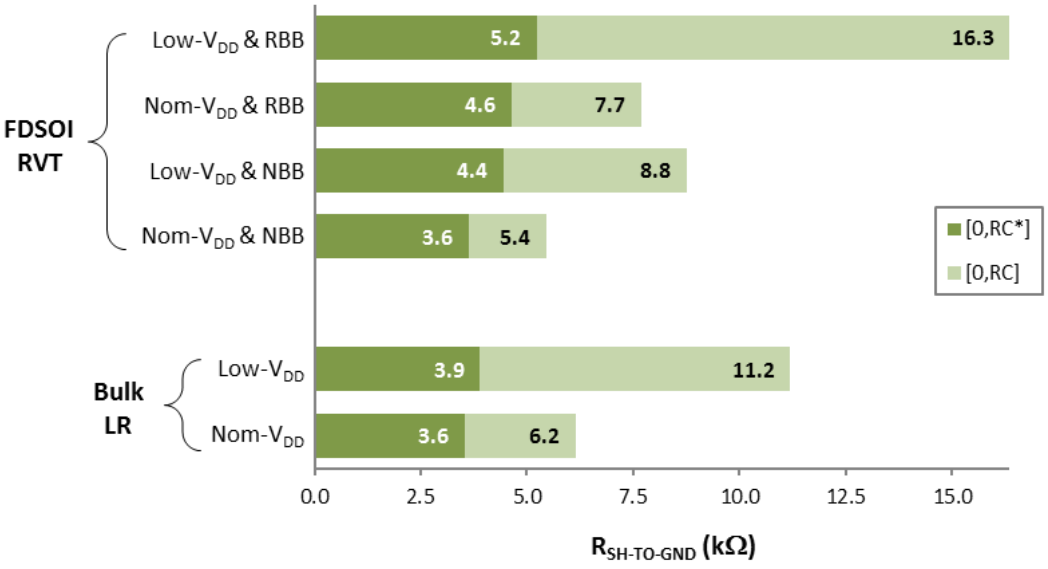



**Figure 5.4: Comparison of short-to-GND detectability range in Bulk-LR & FDSOI-RVT (with and without the impact of process variations).**

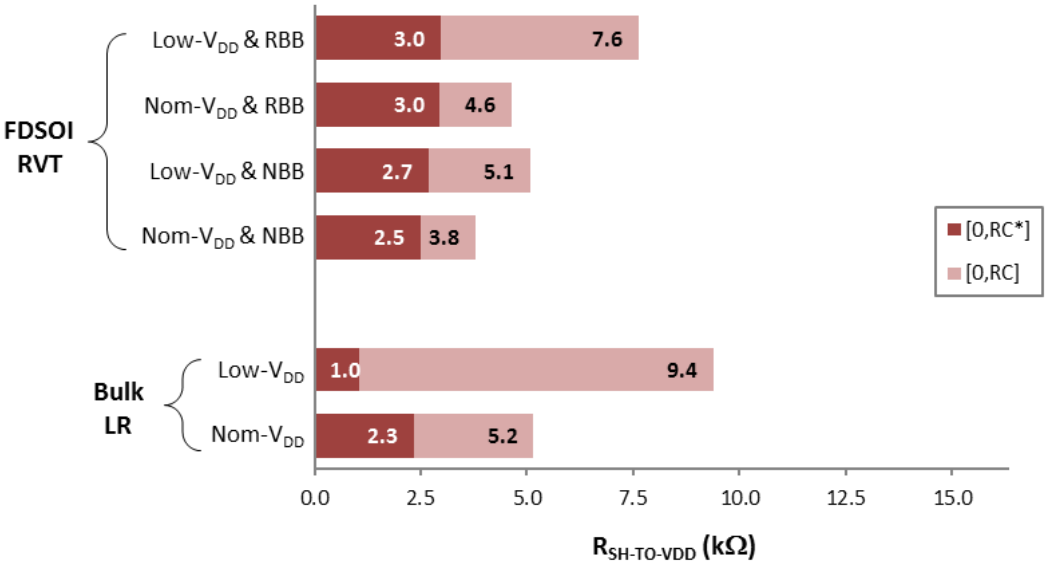



**Figure 5.5: Comparison of short-to-$V_{DD}$ detectability range in Bulk-LR & FDSOI-RVT (with and without the impact of process variations).**

More generally, these results illustrate the importance of considering process variations. Indeed, they show that the theoretical detectability range established under typical process conditions may be considerably overestimated. Moreover, the conclusions on the most favorable operating conditions with respect to robust detectability range might be erroneous when process variations are not taken into account.

To summarize, this study reveals that thanks to a lower impact of process variations, regular-$V_T$ implementations present better testability properties in FDSOI than Bulk regarding robust detection of resistive short defects. Indeed detection of short-to-GND defects can be guaranteed up to 5.2kΩ in FDSOI (using Low-$V_{DD}$ & RBB) but only up to 3.9kΩ in Bulk (using Low-$V_{DD}$). Similarly, detection of short-to-$V_{DD}$ defects can be guaranteed up to 3.0kΩ in FDSOI (using RBB or Low-$V_{DD}$ & RBB) but only up to 2.3kΩ in Bulk (using Nom-$V_{DD}$). Finally, it is worth noting that in both technologies, the detectability range of short-to-GND defects is higher than the one of short-to-$V_{DD}$ defects. This observation is valid with and without considering process variations, and just comes from the fact that P-transistors have a higher ON-resistance at the switching point than N-transistors.

### 5.4.2 FDSOI Vs. Bulk – Low -$V_T$ Implementations

Tables 5.13 and 5.14 report the estimated and simulated values of critical resistance (both the classical critical resistance $R_C$ established under typical process variations and the "robust" critical resistance $R_C{}^*$ that incorporates the impact of process variations) under different operating conditions for FDSOI-RVT and Bulk-LR implementations in case of short-to-GND defect, and Tables 5.15 and 5.16 in case of short-to-$V_{DD}$ defect. Similar conclusions than for Regular-VT implementations can be drawn, i.e. globally a fairly good estimation of the critical resistance but a higher error for Bulk than FDSOI, especially regarding the "robust" critical resistance.

**Table 5.13: Estimated and simulated values of critical resistance associated with short-to-GND defect under different operating conditions for FDSOI-LVT.**

| FDSOI-LVT | | | | | | | |
|---|---|---|---|---|---|---|---|
| Operating Conditions | | Estim. | Simul. | *Error* | Estim. | Simul. | *Error* |
| | | $\hat{R}_{C-GND}$ (kΩ) | $R_{C-GND}$ (kΩ) | $\varepsilon_{R_{C-GND}}$ | $\hat{R}_{C-GND}{}^*$ (kΩ) | $R_{C-GND}{}^*$ (kΩ) | $\varepsilon_{R_{C-GND}{}^*}$ |
| Nom-$V_{DD}$ | NBB | 3.96 | 3.95 | *0.19%* | 2.53 | 2.70 | *-6.45%* |
| | RBB | 4.24 | 4.23 | *0.17%* | 2.68 | 2.86 | *-6.53%* |
| Low-$V_{DD}$ | NBB | 6.27 | 6.25 | *0.41%* | 3.12 | 3.43 | *-9.16%* |
| | RBB | 6.93 | 6.90 | *0.47%* | 3.34 | 3.68 | *-9.09%* |

**Table 5.14: Estimated and simulated values of critical resistance associated with short-to-GND defect under different operating conditions for Bulk-LL**

| Bulk-LL | | | | | | |
|---|---|---|---|---|---|---|
| Operating Conditions | Estim. | Simul. | *Error* | Estim. | Simul. | *Error* |
| | $\hat{R}_{C-GND}$ (kΩ) | $R_{C-GND}$ (kΩ) | $\boldsymbol{\varepsilon_{R_{C-GND}}}$ | $\hat{R}_{C-GND}{}^{*}$ (kΩ) | $R_{C-GND}{}^{*}$ (kΩ) | $\boldsymbol{\varepsilon_{R_{C-GND}}{}^{*}}$ |
| Nom-$V_{DD}$ | 5.13 | 5.12 | *0.24%* | 2.88 | 3.20 | *-10.19%* |
| Low-$V_{DD}$ | 7.95 | 7.94 | *0.20%* | 3.27 | 3.87 | *-15.66%* |

**Table 5.15: Estimated and simulated values of critical resistance associated with short-to-$V_{DD}$ defect under different operating conditions for FDSOI-LVT.**

| FDSOI-LVT | | | | | | | |
|---|---|---|---|---|---|---|---|
| Operating Conditions | | Estim. | Simul. | *Error* | Estim. | Simul. | *Error* |
| | | $\hat{R}_{C-VDD}$ (kΩ) | $R_{C-VDD}$ (kΩ) | $\boldsymbol{\varepsilon_{R_{C-VDD}}}$ | $\hat{R}_{C-VDD}{}^{*}$ (kΩ) | $R_{C-VDD}{}^{*}$ (kΩ) | $\boldsymbol{\varepsilon_{R_{C-VDD}}{}^{*}}$ |
| Nom-$V_{DD}$ | NBB | 3.59 | 3.41 | *5.33%* | 2.01 | 2.07 | *-2.73%* |
| | RBB | 3.69 | 3.54 | *4.26%* | 2.05 | 2.13 | *-3.51%* |
| Low-$V_{DD}$ | NBB | 4.72 | 4.56 | *3.48%* | 2.11 | 2.27 | *-7.16%* |
| | RBB | 5.01 | 4.89 | *2.43%* | 2.15 | 2.33 | *-7.93%* |

**Table 5.16: Estimated and simulated values of critical resistance associated with short-to-$V_{DD}$ defect under different operating conditions for Bulk-LL.**

| Bulk-LL | | | | | | |
|---|---|---|---|---|---|---|
| Operating Conditions | Estim. | Simul. | *Error* | Estim. | Simul. | *Error* |
| | $\hat{R}_{C-VDD}$ (kΩ) | $R_{C-VDD}$ (kΩ) | $\boldsymbol{\varepsilon_{R_{C-VDD}}}$ | $\hat{R}_{C-VDD}{}^{*}$ (kΩ) | $R_{C-VDD}{}^{*}$ (kΩ) | $\boldsymbol{\varepsilon_{R_{C-VDD}}{}^{*}}$ |
| Nom-$V_{DD}$ | 4.14 | 4.19 | *-1.30%* | 1.93 | 2.17 | *-11.33%* |
| Low-$V_{DD}$ | 6.52 | 6.64 | *-1.84%* | 1.70 | 1.99 | *-14.90%* |

The detectability range achieved under different operating conditions for Bulk-LL and FDSOI-LVT implementations are graphically summarized in Figures 5.6 and 5.7 (simulated values), in case of short-to-GND and short-to-$V_{DD}$ defects respectively.

Here again, these results are globally in accordance with results obtained on regular-$V_T$ devices.

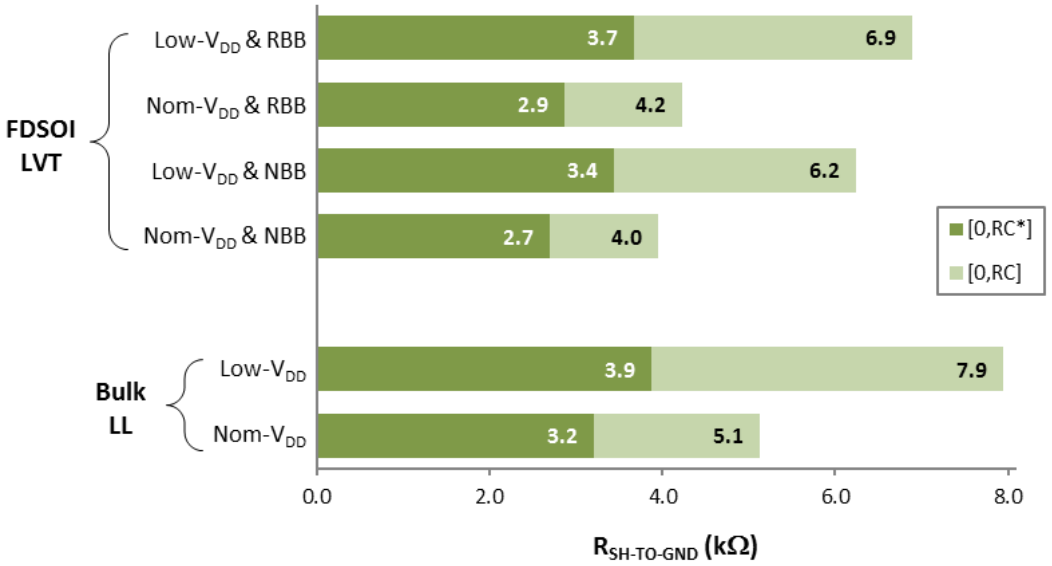



**Figure 5.6: Comparison of short-to-GND detectability range in Bulk-LL & FDSOI-LVT (with and without the impact of process variations).**

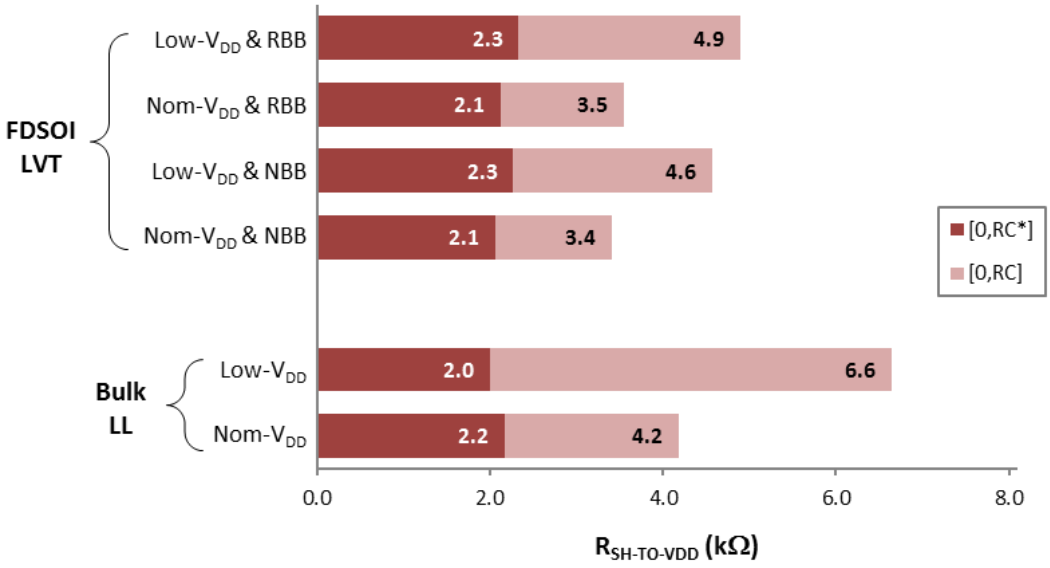



**Figure 5.7: Comparison of short-to-$V_{DD}$ detectability range in Bulk-LL & FDSOI-LVT (with and without the impact of process variations).**

Under nominal operating conditions (Nom-$V_{DD}$ & NBB), Bulk implementation exhibits slightly larger detectability ranges than FDSOI implementation when process variations are not considered. Indeed for both types of defect, we observe a higher value of the critical resistance for Bulk than FDSOI ($R_C$=5.1Ω vs. $R_C$=4.0kΩ for short-to-

GND and $R_C$=4.2kΩ vs. $R_C$=3.4kΩ for short-to-$V_{DD}$). However, when process variations are taken into account in the simulation, the detectability range in Bulk is reduced by 37% for short-to-GND and 48% for short-to-VDD, while the detectability range in FDSOI is only reduced by 32% for short-to-GND and 38% for short-to-$V_{DD}$. In particular, it can be observed that there is a significant overestimation of the detectability range established with typical process condition. However because of a smaller impact of process variations on the ON-resistance of low-$V_T$ transistors, the reduction in the detectability range is lessened compared to regular-$V_T$ implementations.

We hereafter discuss the benefit that can be achieved by using favorable operating conditions separately for both the defect types:

- In case of short-to-GND, the most favorable conditions that improve short defect detectability are Low-$V_{DD}$ for Bulk and Low-$V_{DD}$ combined with RBB for FDSOI. This observation is valid irrespective of process variations. In case of Bulk, without considering process variations, the critical resistance $R_C$ increases from 5.1kΩ under standard operating conditions to 7.9kΩ under optimal operating conditions. A similar improvement is noticed in FDSOI, $R_C$ increases from 4.0kΩ under standard operating conditions to 6.9kΩ under optimal operating conditions. Hence, an overall detectability improvement of 54% and 72% can be achieved for Bulk and FDSOI respectively. Regarding testability properties, low-$V_T$ implementations actually present comparable detectability ranges in Bulk and FDSOI, with minor advantage to Bulk in case of short-to-GND ($R_C^*$=3.9kΩ vs. $R_C^*$=3.7kΩ).
- In case of short-to-$V_{DD}$, the most favorable conditions determined without considering process variations are Low-$V_{DD}$ for Bulk and Low-$V_{DD}$ combined with RBB for FDSOI, whereas the most favorable conditions determined when considering process variations are Nom-$V_{DD}$ in Bulk and Low-$V_{DD}$ combined with NBB in FDSOI. Again, a comparable detectability ranges in Bulk and FDSOI in presence of process variation is achieved with a minor advantage to FDSOI ($R_C^*$=2.3kΩ vs. $R_C^*$=2.2kΩ).

Finally here again, the detectability range of short-to-GND defects is higher than the one of short-to-VDD defects.

## 5.5 SUMMARY

This chapter has presented a comparative study of the impact of process variations on the detectability of resistive short defects in 28nm Bulk and FDSOI technologies. Two types of short defect have been investigated, i.e. short-to-GND and short-to-$V_{DD}$. Defect detectability has been analyzed based on the concept of critical resistance, which has been extended in this chapter to ensure robust defect detection in presence of process variations.

Detectability ranges obtained with and without considering process variations have then been determined for different implementations and different operating conditions. Results have shown that, under the most favorable operating conditions, defect detection can be guaranteed in slightly larger ranges in FDSOI with respect to Bulk in case of regular-$V_T$ implementations, and similar ranges in case of low-$V_T$ implementations. Results have also highlighted the importance of taking into account process variations since the conclusions on the most favorable operating conditions derived from the theoretical detectability range established under typical process conditions range might be erroneous.

The development of analytical models allow to evaluate the impact of process variations on the critical resistance has also been investigated. Based on the assumption of independence between the gate threshold voltage and the ON-resistance of conducting transistors, very simple expressions have been established. Results have shown that fairly good estimation of the critical resistance can be achieved. However, it is clear that the hypothesis of independence between the threshold voltage and the ON-resistance is not fully valid and introduces some errors. Still, the proposed expressions have the merit to permit the estimation of the detectability range associated with a given defect without performing any fault simulation but based only on a pre-characterization of the gate library. Future work will focus on the development of more refined expressions in order to improve the accuracy.

# 6 Conclusion and Future Works

## 6.1 Thesis Summary

With continually shrinking nanoscale technologies, the increase in short channel effects, process variations and susceptibility to manufacturing defects causes difficulties in developing reliable semiconductor devices. At 28nm and beyond, the traditional planar Bulk transistor has failed to offer the expected higher performances with lower power consumption. Firstly, manufacturing structures much smaller than the wavelength of light used in modern lithography are difficult to fabricate and can be practically done only with certain coarse limits. Similarly, it is difficult to control the doping concentration for transistors in the nanometer range. Further, the structures are located closer to each other with every technology node, resulting in even the smallest of impurities or metal silvers being able to create shorts or other defects. Lastly, as the number of transistors, wires, contacts and vias on a single chip increase, the probability of one or more of being faulty increases. These limitations have resulted in increasing the probability of defects in advanced technology nodes.

Taking into account these issues that affect semiconductor devices in deep sub-micron technologies, the wide-ranging work of this thesis addresses the challenges impacting advanced technology nodes from a defect testability perspective. FDSOI and FinFET transistor technologies with a much better electrostatic integrity are considered as the most likely alternatives to the traditional Bulk transistor. The major work of this thesis is focused on comparing these emerging transistor technologies on the basis of their manufacturing defect testability.

To conclude, the major contributions of this work are as follows:

- We presented an overview of the emerging FDSOI and FinFET transistor technologies with respect to the conventional Bulk transistor. We also discussed the classical manufacturing defects such as short and open defects affecting the traditional CMOS technologies followed by the new defects specific to the emerging FDSOI and FinFET technologies. An analysis of the state-of-the-art of most common test techniques for detecting resistive short and open defects is also presented.
- A comparative study of Bulk, FDSOI and FinFET transistor technologies in presence of a resistive bridging defect has been presented. In order to compare a planar Bulk and FDSOI transistor with a vertical FinFET transistor, a particular

care has been taken to design the elementary gates so that the comparative analysis in these different technologies is meaningful. Similar designs are implemented in each technology and defect detectability is analysed with the same inter-gate resistive bridging defect in each implementation. We performed the HSPICE simulation and used the concept of critical resistance to present the static and dynamic impact of the bridging defect. Our results show that Bulk, FDSOI-LVT and FinFET exhibit similar detectability, both for the static and dynamic behavior. However, FDSOI-RVT offers a wider detectability range, which can be further extended by the appropriate use of reverse body-biasing (RBB). It should also be pointed out that for Bulk and FDSOI technologies, the simulation results are based on "industrial" models thoroughly validated through silicon measurements. In contrast for FinFET technology, simulation results might not be fully representative of industrial manufactured devices as they are based on an "academic" model.

- We presented an in-depth analysis of the impact of body-biasing, supply voltage and temperature on the detection of resistive short-to-GND, short-to-$V_{DD}$ and inter-gate bridging defects in 28nm FDSOI technology. We targeted the Low-$V_T$ (LVT) and Regular-$V_T$ (RVT) implementations offered by the FDSOI technology. The concept of critical resistance is used to evaluate the defect detectability in the context of logic based test. Simulations of simple didactic circuits implemented with standard elementary inverters from the 28nm FDSOI gate library have been carried out using HSPICE for both the implemenattions. Our results show that in case of RVT implementation, the detectability of short defects can be optimized by Low $V_{DD}$, RBB and Low temperature. Similarly, in case of LVT implementation, the detectability of short-to-GND and inter-gate resistive bridging defects is also optimized by Low $V_{DD}$, RBB and Low temperature. However, for resistive short-to-$V_{DD}$ High temperature favors the detection.

- We proposed a simple analytical model for resistive short defects based on the ON-resistance of the P and N-networks , which enables the computation of the critical resistance in various conditions of supply voltage, body-biasing and temperature without performing any fault simulations. A pre characterization of the value of the ON-resistance for different gates of the library, under various operating conditions can be achieved in reasonable simulation time with

standard computing equipment and this is sufficient to deduce the value of the critical resistance. Our results show that the proposed model enables an accurate estimation of the critical resistance and leads to a better understanding of the favorable operating conditions to improve defect detectability.

- We have also shown that for the detection of short defects in FDSOI, significant enlargement of the detectability range can be achieved by using only the electrical parameters like supply voltage and body-biasing. Temperature introduces only an incremental improvement in the detectability range, this is an important point as achieving low or high temperature induces severe practical difficulties and might engender unaffordable supplementary cost.
- The wide an effective range of body-biasing in FDSOI can be an asset from the testing point of view. We carried out a deeper exploration of the feature of body-biasing in FDSOI by independently body-biasing the P and N-type transistors. However, the results show that such an independent biasing does not offer any benefits for the detection of short defect compared to the situation where RBB is applied on both P and N-type transistor.
- A comprehensive study for the detection of weak resistive open and short defects using delay test for a didactic circuit implemented in 28nm FDSOI – RVT and LVT implementations has been presented. The value of the critical resistance is estimated based on the difference in the values of the delay using *slow* and *typical* process corners. Our results show that High $V_{DD}$ and FBB improves the detectability of weak resistive opens while Low $V_{DD}$ and RBB enhances the detectability of weak resistive shorts. We also demonstrated that circuits implemented with FDSOI-LVT transistors facilitates the detection of weak resistive opens while the circuits implemented with FDSOI-RVT transistors facilitates the detection of weak resistive shorts, with a higher detectability for resistive short-to-ground than short-to-$V_{DD}$ defects.
- A comparative study of the impact of process variations on the detectability of resistive short-to-GND and short-to-$V_{DD}$ in 28nm Bulk and FDSOI technologies has been presented. Based on Cadence SPECTRE simulations the testability properties are established for regular and low-$V_T$ devices in both Bulk and FDSOI. We have also extended the analytical models introduced in Chapter 3 in order to incorporate the impact of process variations on the critical resistance.

We determined the defect detectability ranges under different operating conditions with and without considering process variations. Our results show that a slightly larger detectability range can be achieved in FDSOI with respect to Bulk in case of regular-$V_T$ implementations, and similar detectability ranges are obtained in case of low-$V_T$ implementations.

## 6.2 Future Works

This thesis can form the basis for various possible future works in the area of manufacturing defect testability for emerging transistor technologies for resolving the wide-ranging challenges that confront the semiconductor industry. They are briefly listed below:

- The presented simulation results for the comparative study of Bulk, FDSOI and FinFET can be more reliable if the study for FinFET transistors can be carried out with an "industrial" model.
- The study has been focused on defect detection using logic or delay-based test. The study should be extended to investigate defect detection using IddX-based test.
- Apart from the inter-gate defects, the study can also be performed for intra-cell defects. The study can also be extended to other standard gates like NAND, NOR etc.
- In our study we have targeted FinFETs with a common or shorted gate. However, the study can be extended for FinFETs with independent gates.
- New defects specific to the emerging FDSOI and FinFET transistor technologies can also be targeted.

# SCIENTIFIC CONTRIBUTIONS

- **Journals**

[JETTA'17] A. Karel, M. Comte, J. M. Galliere, F. Azais and M. Renovell, "Resistive Bridging Defect Detection in Bulk, FDSOI and FinFET Technologies," in Journal of Electronic Testing (JETTA), vol. 33, no. 4, pp. 515-527, August 2017.

[TNANO'17] A. Karel, M. Comte, J. M. Galliere, F. Azais and M. Renovell, "Influence of Body-Biasing, Supply Voltage, and Temperature on the Detection of Resistive Short Defects in FDSOI Technology," in *IEEE Transactions on Nanotechnology*, vol. 16, no. 3, pp. 417-430, May 2017.

- **International Conferences**

[DATE'18] A. Karel, F. Azais, M. Comte, J. M. Galliere and M. Renovell, "Impact of Process Variation on the Detectability of Resistive Short Defects: 28nm Bulk Vs. FDSOI Technologies," *Design Automation and Test in Europe, 2018* (Submitted).

[ISVLSI'17] A. Karel, F. Azais, M. Comte, J. M. Galliere, M. Renovell and K. Singh, "Comprehensive Study for Detection of Weak Resistive Open and Short Defects in FDSOI Technology," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Bochum, Germany, 2017, pp. 320-325.

[ETS'17] A. Karel, F. Azais, M. Comte, J. M. Galliere, M. Renovell and K. Singh, "Detection of resistive open and short defects in FDSOI under delay-based test: Optimal VDD and body biasing conditions," *22nd IEEE European Test Symposium (ETS)*, Limassol, 2017, pp. 1-2.

[ISVLSI'16] A. Karel, M. Comte, J. M. Galliere, F. Azais and M. Renovell, "Impact of VT and Body-Biasing on Resistive Short Detection in 28nm UTBB

FDSOI -- LVT and RVT Configurations," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Pittsburgh, PA, 2016, pp. 164-169.

[LATS'16] A. Karel, M. Comte, J. M. Galliere, F. Azais and M. Renovell, "Comparative study of Bulk, FDSOI and FinFET technologies in presence of a resistive short defect," *17th Latin-American Test Symposium (LATS)*, Foz do Iguacu, 2016, pp. 129-134.

- **National Conference**

[GDR'16] A. Karel, M. Comte, J. M. Galliere, F. Azais and M. Renovell, "Comparative study of FinFET and FDSOI nanometric technologies based on manufacturing defect testability," *GdR: Groupement de Recherche Soc-SiP*, Nantes, France, 2016.

- **International Seminar**

[SETS'15] A. Karel, M. Comte, J. M. Galliere, F. Azais and M. Renovell, "Emerging Technologies and Test," *South European Test Seminar (SETS)*, Montafon, Austria, 2015.

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