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Alexandre Louis Bosser

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DEPARTMENT OF PHYSICS, UNIVERSITY OF JYVÄSKYLÄ  
LIRMM, UNIVERSITY OF MONTPELLIER/CNRS  
RESEARCH REPORT No. 10/2017

# SINGLE-EVENT EFFECTS OF SPACE AND ATMOSPHERIC RADIATION ON MEMORY COMPONENTS

by

**Alexandre Louis BOSSER**

Academic Dissertation for the Degree of  
Doctor of Philosophy

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and the President of the University of Montpellier, for public examination in Auditorium FYS 1 of the  
University of Jyväskylä on December 20th, 2017 at 12 noon.*



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## Preface

I would like to express my deepest gratitude to my supervisors, Prof. Ari Virtanen, Dr Luigi Dilillo and Dr Arto Javanainen, who showed great dedication at their task and were always available for fruitful discussions, useful advice and support; I know that adequate supervision and good morale are key to the success of doctoral studies. I was also fortunate to be given every possible opportunity to present my research in international conferences, which greatly improved my visibility and my expertise. I am very thankful for the exceptional work environment you have provided for me.

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I'm also grateful to my reviewers, Prof. Simone Gerardin and Prof. Ronald Schrimpf, and to my Opponent Prof. Fernanda Lima Kastensmidt, for the work they have accomplished and the useful comments they provided on my thesis on short notice. I would like to give special thanks to Prof. Lima Kastensmidt for travelling all the way to Finland for my defense.

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Finally, I would like to thank my family, my friends, and most importantly my fiancée Anni Herranen, who were always there to support me and cheer me up when I needed it. Thank you for carrying me through five long, cold, dark Finnish winters!

Alexandre

## Abstract

Electronic memories are ubiquitous components in electronic systems: they are used to store data, and can be found in all manner of industrial, automotive, aerospace, telecommunication and entertainment systems. Memory technology has seen a constant evolution since the first practical dynamic Random-Access Memories (dynamic RAMs) were created in the late 60's. The demand for ever-increasing performance and capacity and decrease in power consumption was met thanks to a steady miniaturization of the component features: modern memory devices include elements barely a few tens of atomic layers thick and a few hundred of atomic layers wide.

The side effect of this constant miniaturization was an increase in the sensitivity of these devices to radiation. Since the first radiation-induced single-event effects (SEEs) were identified in satellites in the late 70's [1] and particle-induced memory upsets were replicated in laboratory tests [2], radiation hardness has been a concern for computer memory manufacturers and for systems designers as well. In the early days, the need for data storage in radiation-rich environments, e.g. nuclear facilities, particle accelerators and space, primarily for military use, created a market for radiation-hardened memory components, capable of withstanding the effects of radiation ; however, this market dwindled with the end of the Cold War and the loss of government interest [3]. In a matter of years, the shortage of available radiation-hard components led system designers to turn to so-called Commercial Off-The-Shelf (COTS) components, with the added benefit of higher performance at a lower cost.

Since COTS devices are not designed with radiation hardness in mind, each COTS component must be assessed before it can be included in a system where reliability is important – a process known as Radiation Hardness Assurance (RHA) [4]. This has led to the emergence of radiation testing as a standard practice in the industry (and in the space industry in particular). Irradiation tests with particle accelerators and radioactive sources are performed to estimate a component's radiation-induced failure rate in a given radiation environment, and thus its suitability for a given mission.

The present work focuses on SEE testing of memory components. It presents the requirements, difficulties and shortcomings of radiation testing, and proposes methods for radiation test data processing; the detection and study of failure modes is used to gain insight on the tested components. This study is based on data obtained over four years on several irradiation campaigns, where memory devices of different technologies (static RAMs, ferroelectric RAM, magnetoresistive RAM, and flash) were irradiated with proton, heavy-ion, neutron and muon beams. The yielded data also supported the development of MTCube, a CubeSat picosatellite developed jointly by the Centre Spatial Universitaire (CSU) and LIRMM in Montpellier, whose mission is to carry out in-flight testing on the same memory devices. The underlying concepts regarding radiation, radiation environments, radiation-matter interactions, memory component architecture and radiation testing are introduced in the first chapters.

**Keywords:** Radiation effects, memory, COTS, RAM, SRAM, FRAM, MRAM, flash, single-event effect, radiation testing

## Résumé

Les composants mémoires sont omniprésents en électronique : ils sont utilisés pour stocker des données, et sont présents dans tous les champs d'application - industriel, automobile, aérospatial, grand public et télécommunications, entre autres. Les technologies mémoires ont connu une évolution continue depuis la création de la première mémoire vive statique (Static Random-Access Memory, SRAM) à la fin des années 60. Les besoins toujours plus importants en termes de performance, de capacité et d'économie d'énergie poussent à une miniaturisation constante de ces composants : les mémoires modernes contiennent des circuits dont certaines dimensions sont de l'ordre du nanomètre.

L'un des inconvénients de cette miniaturisation fut un accroissement de la sensibilité de ces composants aux radiations. Depuis la détection des premiers effets singuliers (Single-Event Effects, SEE) sur un satellite à la fin des années 70 [1], et la reproduction du phénomène en laboratoire [2], les fabricants de composants mémoires et les ingénieurs en électronique se sont intéressés au durcissement aux radiations. Au début, les besoins en stockage pour applications civiles et militaires – comme le développement d'accélérateurs de particules, de réacteurs nucléaires et d'engins spatiaux – créèrent un marché pour les composants durcis aux radiations ; cependant, ce marché s'est considérablement réduit avec la fin de la Guerre Froide et la perte d'intérêt des gouvernements [3]. En quelques années, les ingénieurs durent se tourner vers des composants commerciaux (Commercial Off-The-Shelf Components, COTS), ce qui permit au passage des gains en performance et une réduction des coûts.

Les composants COTS n'étant pas conçus pour résister aux radiations, chaque composant doit être évalué avant d'être utilisé dans des systèmes dont la fiabilité est critique. Ce processus d'évaluation est appelé Radiation Hardness Assurance (RHA) [4]. Les tests aux radiations des composants commerciaux sont devenus une pratique standardisée (en particulier dans l'industrie aérospatiale). Ces composants sont irradiés à l'aide d'accélérateurs de particules et de sources radioactives, afin d'évaluer leur sensibilité, de prédire leur taux d'erreur dans un environnement radiatif donné, et ainsi de déterminer leur adéquation pour une mission donnée.

Cette étude porte sur le test de composants mémoires aux effets singuliers. Les objectifs, difficultés et limitations des tests aux radiations sont présentés, et des méthodes d'analyse de données sont proposées ; l'identification et l'étude des modes de défaillance sont utilisées pour approfondir les connaissances sur les composants testés. Cette étude est basée sur de nombreuses campagnes de test aux radiations, effectuées sur une période de quatre ans, pendant lesquelles des mémoires de différentes technologies – mémoires vives statiques (SRAM), ferroélectriques (FRAM), magnétorésistives (MRAM) et mémoires flash – furent irradiées avec des faisceaux de muons, neutrons, protons et ions lourds. Les données générées ont également servi au développement d'un CubeSat développé conjointement par le LIRMM et le Centre Spatial Universitaire de Montpellier, MTCube, dont la mission est l'irradiation de ces mêmes composants en milieu spatial. Les concepts sous-jacents liés aux radiations, aux environnements radiatifs, à l'architecture des composants mémoires et aux tests aux radiations sont introduits dans les premiers chapitres.

**Mots-clés:** Radiation effects, memory, COTS, RAM, SRAM, FRAM, MRAM, flash, single-event effect, radiation testing



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## List of peer-reviewed publications

This doctoral thesis is based in part on the following peer-reviewed publications:

- I. **A. L. Bosser**, V. Gupta, A. Javanainen, G. Tsiligiannis, S. D. LaLumondiere, D. Brewes, V. Ferlet-Cavrois, H. Puchner, H. Kettunen, T. Gil, F. Wrobel, F. Saigné, A. Virtanen and L. Dilillo, "Single-Event Effects in the Peripheral Circuitry of a Commercial Ferroelectric Random-Access Memory" (*presented at RADECS 2017, submitted for publication in IEEE Transactions on Nuclear Science*)  
*Contribution: the author had a major role in the experiment's software and hardware development, took part in the test campaigns, and did most of the data processing and writing.*
- II. **A. Bosser**, V. Gupta, G. Tsiligiannis, A. Javanainen, H. Kettunen, H. Puchner, F. Saigné, A. Virtanen, F. Wrobel and L. Dilillo, "Investigation on MCU Clustering Methodologies for Cross-Section Estimation of RAMs", in *IEEE Transactions on Nuclear Science*, Vol. 62, no. 6, pp.2620-2626, 2015.  
*Contribution: the author had a major role in the experiment's software and hardware development, took part in the test campaigns, and did most of the data processing and writing.*
- III. **A. L. Bosser**, V. Gupta, G. Tsiligiannis, C. Frost, A. Zadeh, J. Jaatinen, A. Javanainen, H. Puchner, F. Saigné, A. Virtanen, F. Wrobel, and L. Dilillo, "Methodologies for the Statistical Analysis of Memory Response to Radiation", in *IEEE Transactions on Nuclear Science*, Vol. 63, no. 4, pp.2122-2128, 2016.  
*Contribution: the author had a major role in the experiment's software and hardware development, took part in the test campaigns, and did most of the data processing and writing.*
- IV. L. Dilillo, G. Tsiligiannis, V. Gupta, **A. Bosser**, F. Saigné and F. Wrobel, "Soft errors in commercial off-the-shelf static random-access memories", in *Semiconductor Science and Technology*, vol. 32, no.1, 2016  
*Contribution: the author had a major role in the experiment's software and hardware development, and took part in the test campaigns, data processing and writing.*
- V. V. Gupta, **A. Bosser**, G. Tsiligiannis, M. Rousselet, A. Zadeh, A. Javanainen, A. Virtanen, H. Puchner, F. Saigné, F. Wrobel and L. Dilillo, "SEE on Different Layers of Stacked-SRAMs", in *IEEE Transactions on Nuclear Science*, vol. 62, no. 6, pp. 2673-2678, 2015.  
*Contribution: the author had a major role in the experiment's software and hardware development, and took part in the test campaigns and writing.*
- VI. V. Gupta, **A. Bosser**, G. Tsiligiannis, A. Zadeh, A. Javanainen, A. Virtanen, H. Puchner, F. Saigné, F. Wrobel and L. Dilillo, "Heavy-Ion Radiation Impact on a 4 Mb FRAM Under Different Test Modes and Conditions," in *IEEE Transactions on Nuclear Science*, vol. 63, no. 4, pp. 2010-2015, Aug. 2016.  
*Contribution: the author had a major role in the experiment's software and hardware development, and took part in the test campaigns.*
- VII. G. Tsiligiannis, L. Dilillo, V. Gupta, A. Bosio, P. Girard, A. Virazel, H. Puchner, **A. Bosser**, A. Javanainen, A. Virtanen, C. Frost, F. Wrobel, L. Dusseau, and F. Saigné, "Dynamic Test Methods for COTS SRAMs," in *IEEE Transactions on Nuclear Science*, vol. 61, no. 6, pp. 3095-3102, 2014.  
*Contribution: the author took part in the test campaigns.*



## Table of Contents

Preface .....	5
Abstract.....	6
List of peer-reviewed publications.....	9
Chapter I – Radiation Environments .....	12
A. Space radiation .....	12
B. Atmospheric radiation .....	15
C. Artificial radiation sources.....	17
Chapter II – Radiation-matter interactions.....	19
A. Photon-matter interactions.....	19
B. Particle-matter interactions .....	20
C. Consequences of irradiation.....	22
D. Useful concepts for radiation testing .....	24
Chapter III – Memory devices .....	27
A. General principles.....	27
B. Memory cell technologies .....	30
C. Device manufacturing.....	32
Chapter IV – Radiation effects on memory components .....	35
A. Total Ionizing Dose (TID) effects.....	35
B. Single-Event Effects (SEEs).....	37
Chapter V – Radiation testing of memory components .....	45
A. Radiation Hardness Assurance .....	45
B. Testing standards and methodologies .....	46
C. Concepts and metrics for radiation testing.....	47
D. Algorithms for memory testing .....	48
Chapter VI – Experimental setup .....	51
A. Test setups.....	51
B. Data processing .....	56
Chapter VII – Test results and discoveries .....	59
A. Clustering of bit errors in a 90 nm SRAM .....	59
B. Statistical analysis of the radiation response of a 65 nm SRAM .....	62
C. Muon-induced Single-Event Upsets in a 65 nm SRAM.....	69
D. Failure mode analysis of an FRAM.....	74
E. Effects of heavy-ion radiation on a Single-Level Cell NAND flash memory.....	85
F. Single-Event Latch-ups in an MRAM.....	90
Chapter VIII – Summary .....	94
References .....	95
Annexes.....	104

## Chapter I – Radiation Environments

Radiation is a term used to designate the emission or transmission of energy, in the form of waves or particles. Although it can sometimes be used to designate acoustic radiation (the propagation of sound waves) or even gravitational radiation (the propagation of gravitational waves), its most commonly accepted meaning (and the one which will be retained in the present thesis) restricts it to electromagnetic radiation and particle radiation.

Electromagnetic radiation is the propagation of electromagnetic waves: this includes radio waves and microwaves, infrared, visible and UV light, X-rays and  $\gamma$ -rays. Particle radiation designates the propagation of energetic (ie. high-speed) particles, which includes (among other particles) electrons, neutrons, protons and heavier ions. These particles may or may not carry electric charge.

A distinction can be made between non-ionizing radiation and ionizing radiation, which has the power to ionize matter (remove electrons from target atoms). However, the boundary between the two is not sharply defined, because different target materials ionize at different energies.

The type, energy and flux of radiation which can be encountered at a given place is referred to as a radiation environment. In the following sections, various typical radiation environments will be described.

### A. Space radiation

#### 1) Interplanetary radiation environment

The main source of interplanetary radiation is the Sun, with the higher-energy tail of the spectrum coming from distant stars and supernovae.

The Sun emits electromagnetic radiation across most of the electromagnetic spectrum; while it does emit gamma rays, X-rays, microwaves and radio waves, most of its power output is emitted at wavelengths between 100 nm and 1 mm (which includes ultraviolet, visible and infrared light).

The Sun also emits (among other particles) a continuous stream of electrons, protons, and a few heavier particle species; this stream is known as the solar wind, and can be divided into two main components. The “slow” solar wind is composed almost entirely of electrons and protons, with particle speeds of about  $400 \text{ km.s}^{-1}$ , while the “high speed” solar wind, which originates from the coronal holes (which are concentrated around the poles, but can be found throughout the Sun’s surface) has particle speeds of 500 to  $800 \text{ km.s}^{-1}$  and is slightly richer in heavier elements. Since the Sun’s equator rotates every 27 days, the faster streams emanating from coronal holes form a spiral of expanding high-density plasma traveling outwards into the Solar system (see Figure 1) [5].



Figure 1: Illustration of the structure of the solar wind.

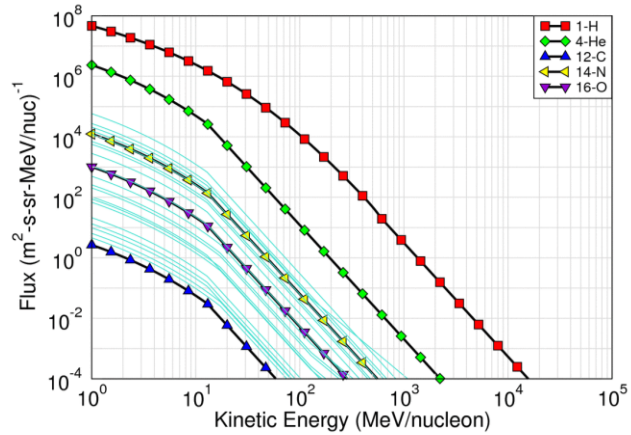


Figure 2: Maximal differential SEP flux vs kinetic energy per nucleon as a function of atomic number (in near-Earth interplanetary space). The curves for some of the most common ion species are identified. Source: CREME-MC [8], using the CREME 96 SEP model.

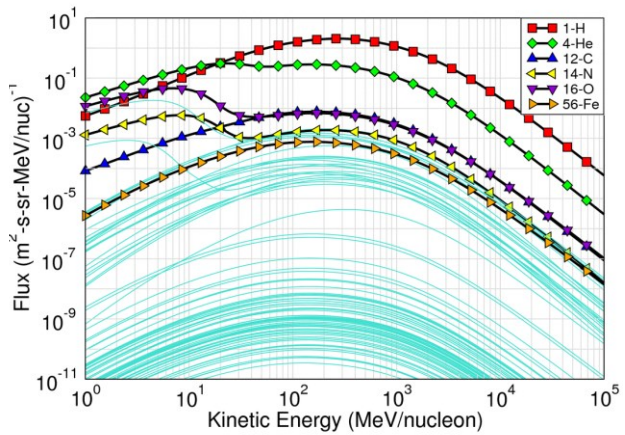


Figure 3: Maximal differential GCR flux vs. kinetic energy per nucleon as a function of atomic number (in near-Earth interplanetary space). The curves for some of the most common ion species are identified. Source: CREME-MC [8], using the CREME 96 GCR model.

In addition to the continuous solar wind, the Sun occasionally emits massive bursts of plasma, in events known as solar flares and Coronal Mass Ejections (CME). These events originate in regions where the Sun’s magnetic field lines bundle up in to helical structures known as flux ropes [6]. The ejected plasma is mostly made up of protons and electrons, with a small fraction of helium ions (alpha particles) and trace amounts of heavier nuclei, and travels at speeds around  $100 \text{ km}\cdot\text{s}^{-1}$  to around  $3000 \text{ km}\cdot\text{s}^{-1}$  [7]. As it travels through interplanetary space, it interacts with the slower solar wind plasma, creating high-density particle “shockwaves”. Altogether, these high-energy particles coming from the Sun are called Solar Energetic Particles (SEP). Figure 2 illustrates the SEP spectrum obtained during the “worst week” starting on 19th October 1989 (a week of unusually high solar activity) [8].

Another source of radiation in interplanetary space are the Galactic Cosmic Rays (GCRs), which are high-energy nuclei, ranging from hydrogen (most common, 89% of the flux) to uranium (traces only). While their origin is being debated, they are known to come from outside of the Solar System, with distant supernovae thought to be a major contributor to the GCR flux. These nuclei have been stripped of all their electrons because of their high energy, hence they carry a high electric charge and can be deflected by magnetic fields [9]. Several models have been developed, which allow the computation of the GCR spectrum and flux near the Earth, outside of the Earth’s magnetosphere [10]–[12]. Figure 3 illustrates the GCR energetic spectrum for some of the most common ion species.

The Sun goes through phases of high and low activity, with a period of around 11 years, called solar cycles. The activity of the Sun influences its radiated power, as well as the number of active regions and coronal holes on its surface, which in turn affect the frequency and magnitude of solar flares and CMEs, and ultimately the SEP spectrum and flux. The GCR spectrum is also affected: during high solar activity, the larger quantity of solar plasma diffusing through the Solar System increases the magnitude of the Heliospheric Magnetic Field (HMF). This means that lower-rigidity (lower-energy) GCR particles (which are coming from outside the Solar System) undergo more deflection by interacting with the HMF when the Sun is at its peak activity: the periods of high solar activity lead to periods of low GCR fluxes, and periods of low solar activity allow for higher GCR fluxes [13].

## 2) Near-Earth radiation environment

The Earth generates a dipole-like magnetic field, with its centre slightly offset from the Earth's centre, and tilted about  $11^\circ$  with respect to its rotational axis. The origin of this magnetic field is thought to be the motion of electrically conductive liquid iron alloys in the Earth's outer core, driven by thermal convection and Coriolis forces caused by the rotation of the Earth – an origin theory known as the “dynamo theory” [14]. As they encounter the Earth's magnetic field, charged particles (such as solar wind plasma, SEPs and GCRs) are deflected by a force known as the Lorentz force, which is proportional to their speed and to the magnitude of the magnetic field. This phenomenon has a two-fold impact on the near-Earth radiation environment.

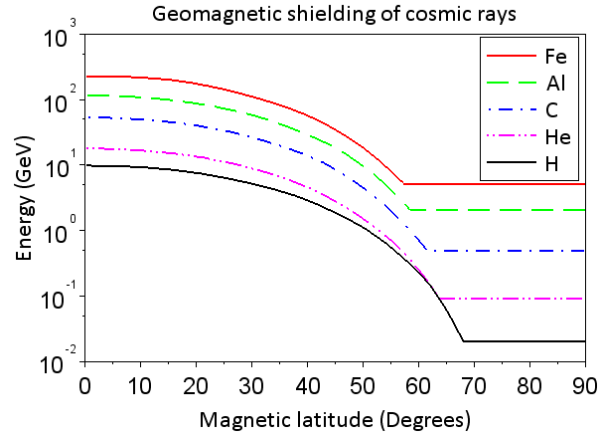


Figure 4: Effect of the geomagnetic shielding on the cosmic ray spectrum as a function of magnetic latitude and ion species. The spectrum is calculated behind 2,54 mm of aluminium. Data source: Petersen et al. [15]-p.35

The particles of low magnetic rigidity<sup>1</sup> (i.e. GCRs and high-energy SEP) can be deflected away from the Earth: this geomagnetic shielding effect prevents them from reaching areas where the geomagnetic field is stronger (at low altitudes and high latitudes). Figure 4 illustrates the effect of the geomagnetic shielding on the particle spectrum as a function of magnetic latitude and ion species (which, for fully-stripped GCRs, determines their rigidity).

The trajectories of the lowest-energy, least rigid particles (protons and electrons) are bent so much that they can be trapped in a broad region, extending from a few hundred kilometres to about 60.000 km of altitude, called the Van Allen radiation belts (Figure 5). The belts have a roughly toroidal shape, centered around the Earth's magnetic centre and aligned with its magnetic equator. Inside the belts, individual trapped particles drift around the Earth, depending on their electrical charge (eastward for electrons, and westward for protons); additionally, they move along a helicoidal path around the Earth's magnetic field lines, “bouncing” back and forth between the two magnetic poles [15]-p.22. As the magnetic field lines get closer to the Earth near the poles, these trapped particles may interact with atoms in the upper atmosphere, resulting in the generation of low-energy, “cold” plasma. This phenomenon is also the source of auroral displays.

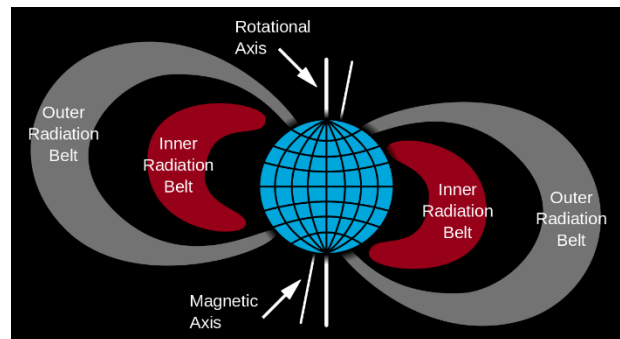


Figure 5: Illustration of the structure of the Van Allen radiation belts. Image from the public domain (credit: NASA)

The particles trapped in the Earth's magnetic field tend to concentrate at different altitudes depending on their mass and velocity. Traditionally, the Van Allen belts are considered to consist of a smaller inner belt, and a larger outer belt. The inner belt is made of protons (at energies up to 400 MeV) and electrons (at energies up to 5 MeV), while the outer belt is exclusively made up of electrons (at energies up to 7

<sup>1</sup> Magnetic rigidity is a quantity amounting to a particle's momentum divided by its electrical charge, which specifies its curvature radius when subjected to a given magnetic field.

MeV) [16]. However, the structure and particle fluxes of these radiation belts are influenced by solar activity, and can change dramatically when plasma from a solar flare or CME encounters the Earth [17]. Several models have been developed over the years to describe the characteristics of the Earth’s trapped radiation field, a recent example being the AE9/AP9/SPM model [18].

Because the centre of the Earth’s magnetosphere is slightly offset with the centre of the Earth, the lower boundary of the inner belt comes closer to the upper atmosphere (from 1000 km down to about 200 km of altitude) in a region roughly located above South America and the southern Atlantic Ocean. This region of higher radiation levels at low altitudes, called the South Atlantic Anomaly (SAA), represents a threat to electronic devices; in Low Earth Orbit (LEO), the SAA accounts for virtually all of the proton fluence (at energies above 30 MeV) received by a spacecraft [15]-p.44.

Other planets than the Earth (most notably Jupiter and Saturn) possess a magnetic field strong enough to interact significantly with charged energetic particles; phenomena and structures similar to these described in this section can be found around these planets.

## B. Atmospheric radiation

As mentioned in the previous section, the geomagnetic field can deflect low-rigidity Earth-bound charged particles. However, with the right angle of incidence and high enough rigidity (high enough energy), charged particles may penetrate the Earth’s magnetic field and enter the upper atmosphere. These high-energy ions eventually undergo nuclear interactions with the atmosphere, generating high-energy reaction products (e.g. muons, pions, gamma photons, lighter nuclei...) which in turn trigger nuclear reactions with the atmosphere (or decay into other products). After several steps, a cascade of secondary particles has taken form, called a “cosmic ray shower”. These cosmic ray showers are more abundant at higher magnetic latitudes, because the geomagnetic shielding effect is weaker near the poles.

Nuclear interactions degrade the cosmic ray spectrum until about 15 km of altitude, at which point virtually all primary cosmic rays have interacted and turned into secondary particles (although the proton spectrum remains significant) [19]. These secondary particles, which carry part of the original cosmic ray momentum, generally follow a downwards trajectory, losing energy through nuclear scattering, electronic stopping and light emission, until they decay into other particles, are captured, or come to a rest in matter. Figure 6 illustrates the vertical flux of cosmic ray

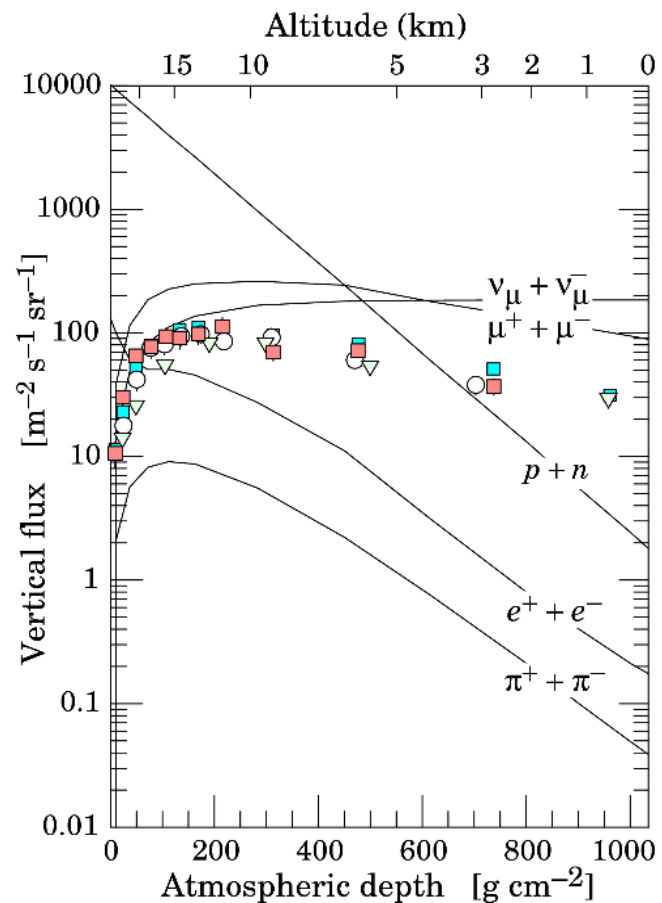


Figure 6: Vertical fluxes of atmospheric cosmic ray shower particles with  $E > 1$  GeV. The data points represent different measurements for negative muon flux. Source: Patrignani et al. [20].



shower particles in the atmosphere [20]. Among these secondary particles, neutrons and muons/antimuons are the most numerous below 20 km of altitude; indeed, their lifetime spans more than a few microseconds, and they are not easily stopped by air. This makes them the most significant threat to electronic component reliability.

### 1) Atmospheric neutrons

Atmospheric neutrons are one of the types of secondary particles which are produced in cosmic ray showers. Neutron production starts at very high altitudes (> 150 km), and as the atmosphere gets denser and the cosmic ray interactions increase, so does the neutron flux, until it reaches a peak called the Pfozter maximum around 20 km of altitude. Considering only neutrons with an energy > 1 MeV, the flux at the Pfozter maximum is at least  $3.5 \cdot 10^{-1}$  neutrons.cm<sup>-2</sup>.s<sup>-1</sup> at 42° magnetic latitude [21]. Below 20 km, the thickening of the atmosphere effectively reduces the flux: at ground level, it is two to three orders of magnitude lower than its peak value. Since the atmospheric neutron flux is a consequence of the incident high-energy cosmic ray flux, it is strongly influenced by geomagnetic shielding: the neutron flux can be six times higher at the poles than at the equator [22].

Eventually, after several collisions causing gradual energy loss, if they are not captured by encountered nuclei, these neutrons reach thermal equilibrium. Their kinetic energy stabilizes around an energy of about 0.025 eV, which is the most probable energy for a free particle at room temperature. These thermal neutrons generally interact more easily with matter [23], in particular with elements such as cadmium-113 and boron-10; hence, electronic parts containing these elements (for example, boron-10 in borophosphosilicate glass insulating layers) are more likely to be disturbed by thermalized neutrons.

### 2) Atmospheric muons and antimuons

Muons are one of the decay product of pions, which are very short-lived subatomic particles released in high-energy nuclear collisions such as those taking place in a cosmic ray shower. Muons (and their antiparticles, antimuons) are unstable elementary particles, with a half-life of 1.52 μs. They eventually decay in an electron (or positron) and two neutrinos. They carry one negative elementary charge (or, in the case of antimuons, one positive charge) and have a mass about 207 times greater than that of an electron (or about 1/9<sup>th</sup> the mass of a proton).

Cosmic ray showers release large amounts of relativistic muons: they undergo a significant time dilation effect because of their high velocities, which allows them to live long enough to travel for several kilometres. Additionally, at these high energies (atmospheric muons generally have energies > 1 GeV) muons only lose energy at a very low rate (as low as  $2 \cdot 10^{-3}$  MeV.cm<sup>-2</sup>.mg<sup>-1</sup> [24]), which gives them a high penetration capacity. Muons can go through the atmosphere, and may even travel several kilometres underground before decaying or stopping.

### 3) Naturally-occurring radionuclides

Part of the natural radiation background at ground level originates from naturally occurring radionuclides. Among these elements, radon-222 is a major contributor. It is a short-lived radioactive noble gas, which is continually produced as one of elements in the radium, uranium and thorium decay chains. Being a very dense gas, it tends to accumulate in caves, and poorly-ventilated buildings and cellars near bedrock. It decays into polonium-218 by emitting a 5.59 MeV alpha particle; the range of these particles in common plastics and ceramics doesn't exceed a few micrometres, hence these are not a concern for most packaged electronics. However, in some specific cases where electronics operate with bare dies, the alpha radiation from naturally-occurring radon can cause malfunctions and must be considered.

Naturally-occurring radionuclides can also contaminate the materials used in component manufacturing (e.g. silicon, lead...) and packaging at part-per-trillion to part-per-million levels. When such contaminants decay, they release radiation which can be detrimental to the component's reliability. The presence of alpha-emitting contaminants, such as uranium-238, thorium-232, and their decay products, was already a concern in the late 70's [25] and is still a reliability issue to this day [26].

### C. Artificial radiation sources

A wide range of technical scenarios require electronic components to operate in radiative environment where the main radiation source is artificial. These radiation sources can be antennae, lasers, man-made radioactive sources (radionuclides), particle accelerators, nuclear reactors, and nuclear weapons. These artificial sources cover a very wide range of particle species, energy and flux levels, with a wide range of possible consequences on electronic systems.

#### 1) Man-made radioactive sources

Certain industrial applications require the use of radiation sources. One good example is the use of gamma-ray sterilization units, where the gamma rays produced by the decay of a mass of cobalt-60 are used to sterilize a wide variety of pharmaceutical, agricultural and food products, for the purpose of disinfection, shelf life extension, or sprout inhibition [27]. Another example is the use of gamma-ray, x-ray and, more rarely, neutron imagers for cargo, luggage, and passenger inspection at transit centres, harbours and airports [28].

In the electronics industry, automated X-ray inspection (AXI) of printed circuit boards (PCBs) has become a standard procedure for quality control, in particular to inspect the quality of solder connections. AXI techniques allow the observation of solder joints which are not directly visible, such as those under ball grid array (BGA) packages [29]. This raises the concern of the sensitivity of these components to accumulated dose.

#### 2) Particle accelerators and nuclear power plants

Particle accelerators are facilities where charged particles are accelerated using electric and magnetic fields. The resulting particle beams are valuable tools to perform fundamental and applied research in many scientific disciplines. They represent a serious radiation hazard: the largest particle accelerators are generally designed to reach high particle fluxes and energies, and generate particle beams which can activate (generate radioactivity in) the materials they touch. High-energy ions straying away from the beam will generate so-called "hadronic cascades" of secondary particles such as protons, neutrons, pions and kaons akin to cosmic ray showers. Since such extremely complex machines require complex electronic control systems to operate, the effects of stray radiation on these systems are a major concern and a subject of investigation [30]. Small accelerators are also used for medical applications: x-rays are used in radiology to image internal organs, and x-rays, gamma rays, and proton or carbon beams are used to treat cancer (radiation oncology). The devices used for these applications may generate high enough fluxes of secondary radiation [31] to pose a threat to surrounding electronic devices.

Nuclear power plant operation also generates a considerable amount of radiation – gamma rays, X-rays, protons, neutrons, alpha particles and electrons. One of the main challenges of nuclear power plant

radiation safety is to shield equipment (and personnel) from gamma and neutron radiation, because they are highly penetrating.

### 3) Nuclear weapons

Upon detonation, nuclear weapons release heavy radioactive particles known as nuclear fallout, as well as a burst of high-energy gamma rays and neutrons. This gamma-ray burst generates a wave of scattered Compton electrons as the gamma rays interact with the air; these energetic electrons are deflected by the geomagnetic field, which leads to the emission of synchrotron radiation in the general direction of the electrons' trajectories. Since the initial gamma burst propagates at the speed of light, the synchrotron radiation from the secondary Compton electrons adds coherently, leading to the formation of an electromagnetic pulse (EMP). These pulses are capable of inducing very high voltages in ground-level conductors [32], which makes EMPs a major concern for military electronics designers [33].

## Chapter II – Radiation-matter interactions

When radiation encounters matter, several different interaction processes may ensue, which depend on the encountered material, and on the energy and type of the incoming radiation. Two broad categories can be defined: ionizing and non-ionizing radiation. In this chapter, the physical processes which are the most relevant for the study of radiation effects on electronics will be introduced. In the following chapter, the material encountered by the radiation will be designed as the “target material” or “target”.

The concept of cross-section is commonly used to quantify the probability of a certain type of radiation-matter interaction to occur. The cross-section of a reaction represents the area (as measured on a plane orthogonal to their relative motion) within which these particles must meet for the reaction to occur: the larger the cross-section, the more likely the reaction is.

### A. Photon-matter interactions

Photons can interact with matter via several physical processes. In the scope of this study, we will only consider the processes by which the interaction leads to an energy loss for the photon:

- the photoelectric effect, where an electron captures a photon with an energy higher than its own binding energy, and as a result is ejected from its atom;
- Compton scattering, the inelastic interaction between a photon and an electron of a target atom – part of the energy of the photon being transferred to the ejected electron;
- pair production, a process whereby a high-energy photon interacts with the nucleus of a target atom, and is converted into an electron-positron pair [34];
- triplet production, a process whereby a high-energy photon interacts with an electron of a target atom and is converted into an electron-positron pair, knocking off the target electron in the process [34].

For these processes to take place, the incident photon must carry an energy higher or equal to the first ionization energy of the target atom. The photoelectric effect is the dominant interaction mechanism for low-energy photons (a few eV up to a few keV), while pair and triplet production must involve photons carrying an energy superior to the rest mass of an electron and a positron (1.022 MeV). The predominance of these mechanisms in photon absorption in a lead target is plotted on Figure 7 [35].

As a result of these interactions, part or all of the initial photon energy is transferred to a recoiling electron (or positron) which then deposits this energy in the surrounding material. This is done via other physical processes, which are described in the following section.

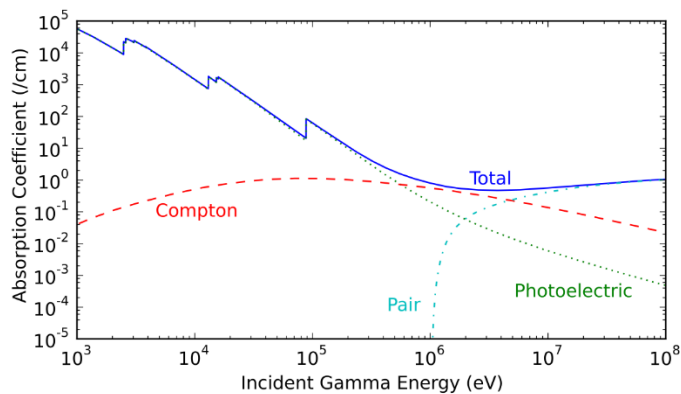


Figure 7: Predominance of photoelectric, Compton and pair production interactions in a lead target as a function of incident photon energy. Source: Joshua Hikes, using the ENDF/B-VII.0 database, under CC BY-SA 3.0 license.

## B. Particle-matter interactions

Particle radiation can interact with matter via several physical processes, depending on the type of particle. The most relevant for the scope of this study are electronic stopping, elastic and inelastic nuclear interactions, and capture. This excludes radiative losses, which are the dominant energy loss mechanism for very high-energy particles.

### 1) Electronic stopping

Coulomb's law states that charged particles exert a force on each other, which is proportional to the magnitude of their charges and inversely proportional to the square of the distance between them. Particles carrying charges of the same sign will repel each other, while opposite charges will attract each other. As a charged particle travels through matter, the electrons of the surrounding atoms exert an electrostatic force on the travelling particle and slow it down. This phenomenon is called electronic stopping. In return, the charged particle will exert an electrostatic force on the surrounding electrons, which can be sufficient to remove them from their atoms – thus leaving an ionized track along its trajectory.

The maximum amount of energy which can be transferred to an electron in a single non-relativistic collision,  $W_{max}$ , is given by the following formula:

$$W_{max} = \frac{2m_e v^2}{1 + \left(\frac{m_e}{M}\right)^2} \quad \text{Equation 1}$$

In this formula,  $m_e$  is the mass of an electron,  $c$  is the speed of light,  $v$  the velocity of the incident particle, and  $M$  the mass of the incident particle. In the case of low-energy charged ions,  $m_e \ll M$ , so we can make the approximation  $W_{max} = 2m_e v^2$ .

The average rate of energy loss through electronic stopping for the incident particle is given by the following formula [36]:

$$\frac{-dE}{dx}_{elec} = \frac{1}{4\pi\epsilon_0^2} \frac{Z_1^2 e^4}{m_e v^2} N Z_2 L \quad \text{Equation 2}$$

with  $Z_1$  the charge number of the incident particle,  $Z_2$  the atomic number of the target atoms,  $N$  the atomic density of the target material,  $\epsilon_0$  the vacuum permittivity,  $e$  the elementary charge, and  $L$  is a dimensionless quantity called the stopping number. Different theories give different expressions for the value of  $L$ . Bohr's stopping theory gives the following expression:

$$L_{Bohr} = \frac{1}{2} \ln \left[ 1 + \left( C \frac{m_e v^3}{Z_1 I \alpha c} \right)^2 \right] \quad \text{Equation 3}$$

In this equation,  $I = \hbar\omega_0$  is the material-dependent mean excitation energy, with  $\hbar$  the Planck constant and  $\omega_0$  the associated photon angular frequency, and  $\alpha$  is the fine-structure constant. This equation has been introduced in Ref. [37], and is based on Ref. [38].

Bethe's stopping theory gives a different expression for the stopping number:

$$L_{Bethe} = \ln \frac{2m_e v^2}{I} \quad \text{Equation 4}$$

This formula, which was introduced in Refs. [37] and [39], is only valid when  $2m_e v^2 \gg I$ .

These formulae demonstrate the dependency of the electronic stopping force on the charge number of the incoming particle (i.e. its atomic number if it is an ion), its velocity, and the atomic number and mass of the target material. The equation shows that heavy particles ( $M \gg m_e$ ) travelling at the same velocity and with a similar charge  $Z_1$  (e.g. an antimuon and a proton) will experience the same electronic stopping power.

## 2) Nuclear stopping

In addition to interacting with the electrons of the target atoms, incoming ions may also pass near and interact with the nuclei of the target atoms (see Figure 8). If the incident particle energy is below the energy necessary to overcome the Coulomb barrier<sup>2</sup>, the two particles will undergo elastic nuclear scattering (also called Rutherford scattering). The incoming particle will be deflected of an angle  $\theta$  (which depends on the impact parameter  $b$ , the electric charges of the incoming particle and target nucleus, and their relative velocity) and transfer part of its kinetic energy to the target atom; if this energy transfer is larger than its lattice binding energy, the target atom will be knocked free and will recoil. The differential cross-section  $d\sigma$  for an incident particle to be deflected into a solid angle  $d\Omega = 2\pi \sin\theta d\theta$  through nuclear scattering is given by the following equation (Ref. [40]):

$$\frac{d\sigma}{d\Omega} = \left(\frac{zZ\hbar c}{4}\right)^2 \left(\frac{\alpha}{E}\right)^2 \frac{1}{\sin^4 \frac{\theta}{2}} \quad \text{Equation 2}$$

where  $z$  and  $Z$  are the respective atomic numbers of the incident ion and target atom,  $\hbar$  is the Planck constant and  $\alpha$  is the fine-structure constant. This cross-section increases with decreasing incident particle energy  $E$ ; this means that the scattering events are more common, hence that the average nuclear stopping force is higher for lower-energy incident particles.

## 3) Nuclear reactions

If the energy of an incident ion is equal to - or higher than - the Coulomb barrier (or if the incident particle carries no charge, in the case of a neutron) and its trajectory brings it close enough to the nucleus of a target atom, then nuclear reactions may take place. An ion may exchange energy, momentum, even nucleons with the target nucleus; a neutron may scatter elastically or inelastically off the target nucleus, or be captured. Inelastic reactions and neutron captures leave one or both nuclei in an excited state, which

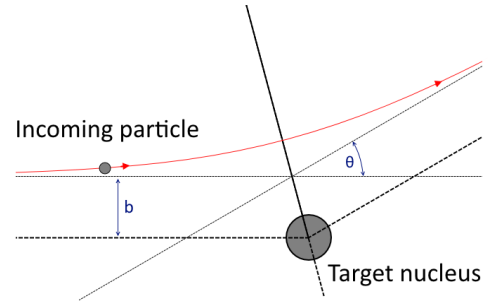


Figure 8: Illustration of the elastic nuclear scattering at an angle  $\theta$  of a positively-charged incoming particle.  $b$  is the impact parameter.

<sup>2</sup> The Coulomb barrier is the energy necessary to bring two nuclei from infinity to a distance  $r$  of each other, which is small enough for the nuclei to undergo a nuclear reaction. Its formula is  $U_{coul} = \frac{1}{4\pi\epsilon_0} \frac{q_1 q_2}{r}$ , with  $\epsilon_0$  the vacuum permittivity, and  $q_1$  and  $q_2$  their respective charges.

eventually undergo de-excitation via one or several possible modes, including gamma-ray emission, and alpha and beta decay. The interaction can also lead to the release of reaction products (lighter nuclei and neutrons) via nuclear fission, neutron evaporation and neutron spallation, or radioactive decay (if the reaction products are unstable); these daughter particles can in turn generate follow-up nuclear reactions and ionization in the target [41].

For charged ions, these processes are much more likely to take place at high incident particle energies, because of the electrostatic forces which tend to separate the two nuclei. Conversely, for nuclear reactions involving neutrons, the cross-section is heavily dependent on the target isotope and on the energy of the incident neutron: at certain energies (called “resonant energies”) the cross-section may exhibit narrow peaks of several orders of magnitude in amplitude [42]. Certain isotopes, such as boron-10 and cadmium-113, have remarkably high low-energy (so-called “thermal”) neutron capture cross-sections, which means that their presence in a target material, even in small quantities, can drastically influence the amount of nuclear reactions which will take place in the target if it is exposed to thermal neutrons. This can have consequences for electronic components, as will be discussed in the next chapters.

#### 4) Coming to rest, capture, annihilation

After they have lost their kinetic energy to the surrounding material, ions come to a stop within the target. Light ions (protons, alpha particles) may escape solid targets in gaseous form [43], but heavier ions will remain in the target.

When they reach a sufficiently low velocity (comparable to that of the target atoms’ electrons), light particles such as electrons and muons ( $\mu^-$ ) may end up being captured by a nearby atom. Captured muons rapidly decay to the lowest muonic orbital state, where they may either decay into an electron, neutrino and antineutrino, or be captured by the nucleus. The nuclear capture leads to the fragmentation of the nucleus, releasing recoiling heavy ions and light particles (neutrons, protons,  $\alpha$ -particles, etc...) [44], [45].

Conversely, antimuons ( $\mu^+$ ) may capture an electron from the target material and form an unstable pseudoatom called muonium [46]. Eventually, antimuons, being unstable particles, undergo decay into a positron, a neutrino and an antineutrino.

Positrons eventually encounter an electron, and the electron-positron pair annihilates, releasing a pair of 511 keV gamma ray photons.

### C. Consequences of irradiation

#### 1) Consequences of ionization

As discussed previously, through different physical processes, much of the energy lost by the incident particle eventually goes to ionizing (ripping electrons off) the atoms of the target material, either directly via electronic stopping, or indirectly from electronic stopping of recoiling nuclei or nuclear reaction products. The most energetic electrons set free in this manner, which can travel over significant distances, are commonly referred to as “delta rays” in the literature.

##### *Electrons and holes*

The electrons which are ripped from their original atoms leave a hole behind – a position where an electron could exist in a bound state. Since the ripped electrons do not participate in screening the charge

of the nuclei of their original atom, the holes they leave behind appear to carry a positive charge. Holes can be filled by bound electrons from the nearby atoms, which in turn leave a hole behind; this displacement of positively-charged electron holes can be studied by assimilating each hole to a virtual particle, carrying one positive elemental electric charge. Free electrons (electrons present in the material, which are not bound to an atom) and holes can annihilate each other in a process known as recombination [47]. Ionizing radiation thus has the effect of creating electron-hole pairs, in excess of the naturally-occurring equilibrium concentrations. Depending on the target material, this ionization may have different consequences.

#### *Effects of ionization on different materials*

Electrical conductors naturally present large concentrations of “free” conduction electrons, so ionization has virtually no impact; however, if a conductor is insulated from its surroundings, delta rays escaping the conductor can lead to positive charge buildup.

In electrical insulators, free charge carrier concentrations are naturally extremely low, and so are charge carrier mobilities (in particular hole mobility [48]). In the absence of an electric field, electron-hole pairs created by ionizing radiation are likely to recombine. However, if an electric field is present in the insulator, the electrons will be able to drift (and eventually be collected by a conductor) much faster than the holes; additionally, holes are easily trapped in defects in oxides [49]. Over time, this leads to a buildup of positive charge in the insulator, which will modify the electric field across the insulator and may disturb nearby circuits. This category of effects, called Total Ionizing Dose (TID) effects, will be discussed in further detail in a following chapter. With increasing temperature, the carrier mobility increases; trapped holes are more likely to escape their trapping sites and drift out of the insulator, thereby partly neutralizing TID effects – a phenomenon known as annealing.

In semiconductors, the creation of electron-hole pairs by radiation can have a wide range of consequences, depending on the function of the target material. In off-state transistors and reverse-biased diodes, the applied bias concentrates across a region of the semiconductor crystal, known as the depletion region, which is devoid of free charge carriers. When a single particle strikes the depletion region and generates charge carriers, the intense electric field separates the electron-hole pairs; the holes are collected at the negative electrode while the electrons are collected at the positive electrode, which results in the generation of a current pulse. The occurrence of these current pulses through off-state components can lead to a category of errors called Single-Event Effects (SEE) [50], which will be discussed in further detail in a following chapter.

#### 2) Consequences of atomic displacement

Bombardment of a target by heavy ions, protons, neutrons, high-energy electrons, and even gamma rays (which can produce high-energy secondary electrons) will create displacement damage [51]. Some of the target atoms will be displaced from their original locations through nuclear scattering (and depending on the type and energy of the incoming radiation, some of the target atoms may even undergo fission or decay due to nuclear reactions). This displacement damage may have consequences on the properties of the target material. In semiconductors, displacement damage to the crystal lattice will create defects which will increase charge carrier recombination and trapping, which degrades the performance of the component [52]. In insulators, displacement damage by incident particles may create low-resistivity paths of defects; under high bias (e.g. in transistors and capacitors), this can lead to leakage currents and catastrophic dielectric breakdowns [53]. Displacement damage tends to increase the transmission losses



through common optical materials, which is a concern for electro-optical components, fibre optics, and protective glass covers such as those found on solar panels.

The present study focuses mostly on SEEs caused by ionizing radiation on memory components, hence effects related to displacement damage will not be discussed in detail. However, one must keep in mind the effects of displacement damage on the characteristics of electronic components, because component failure can arise as a result of synergistic degradation due to displacement damage and total ionizing dose.

#### D. Useful concepts for radiation testing

##### 1) Linear Energy Transfer

To describe the deposition of energy by a particle in a target, the community (studying the effects of radiation on electronics) frequently uses a metric known as the Linear Energy Transfer (LET) [50]:

$$LET = -\frac{1}{\rho} \left\langle \frac{dE}{dx} \right\rangle_{elec} \quad \text{Equation 2}$$

where  $\rho$  is the target material density, and  $\left\langle \frac{dE}{dx} \right\rangle_{elec}$  is the energy lost per unit path length via electronic stopping. The units are in  $\text{MeV}\cdot\text{cm}^{-2}\cdot\text{mg}^{-1}$ ; this is useful to correlate energy deposition in targets of similar composition but different densities, or made of different materials (with different densities). The stopping force can be multiplied by the density of the target material to find the energy loss per unit path length.

The LET of a particle varies as it travels within a target and loses energy. Typically, high-energy particles have a low LET, which increases as they decelerate. At a very low energy, the LET reaches a maximum value called the Bragg peak, after which the particle quickly comes to a standstill. As an example, Figure 9 exhibits the LET vs. energy curve of a proton and a helium nucleus (alpha particle) in a silicon target [54].

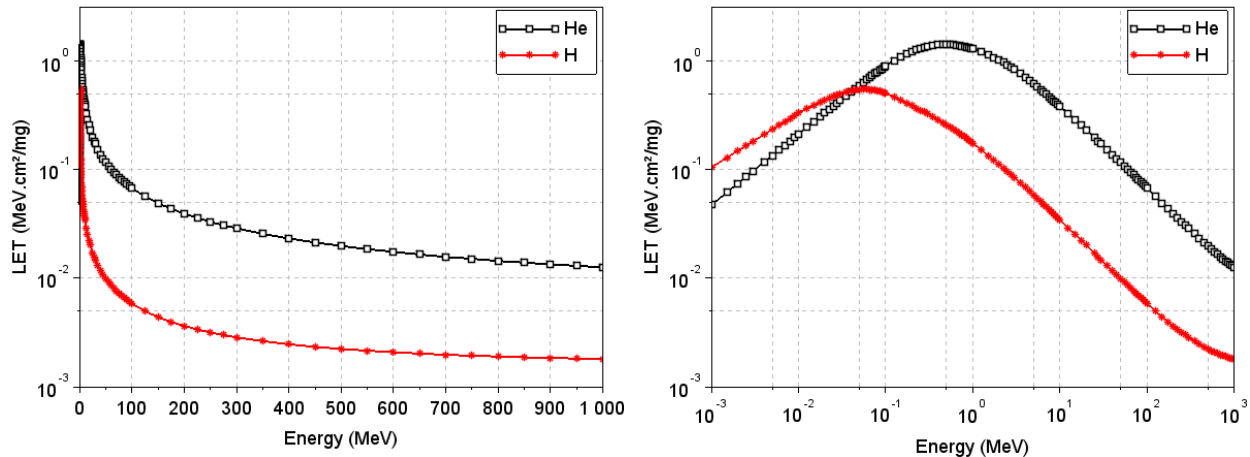


Figure 9: LET vs Energy plot for a proton (red curve) and an alpha particle (black curve) in a silicon target. The two plots present the same data in semilog and log/log format. Source: ASTAR – PSTAR.

The concept of LET is useful to simplify the study of SEEs, by associating a particle's potential for ionization with a single figure. However, the LET is only an average value; it does not account for the discrete nature of electronic stopping, nor does it reflect the small-scale variations of the electronic stopping force. Additionally, care has to be taken when applying the concept of LET to targets with very small charge

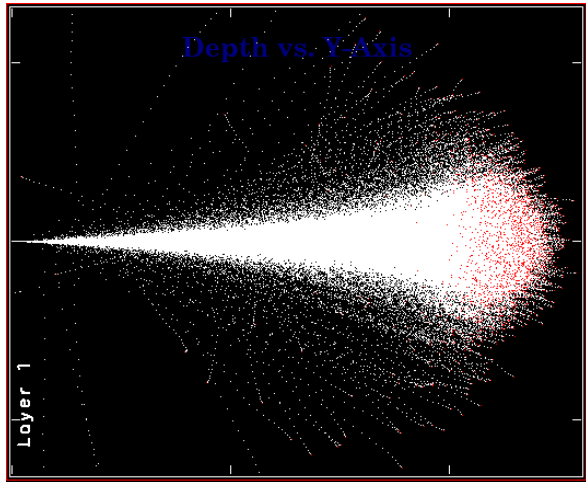


Figure 10: Illustration of the lateral and longitudinal dispersion of a 2 MeV antimuon beam inside a silicon target. The beam enters the target from the left edge; trails of white dots indicate the paths of individual muons, and red dots indicate their final resting positions. The target is 260  $\mu\text{m}$  deep. Source: SRIM.

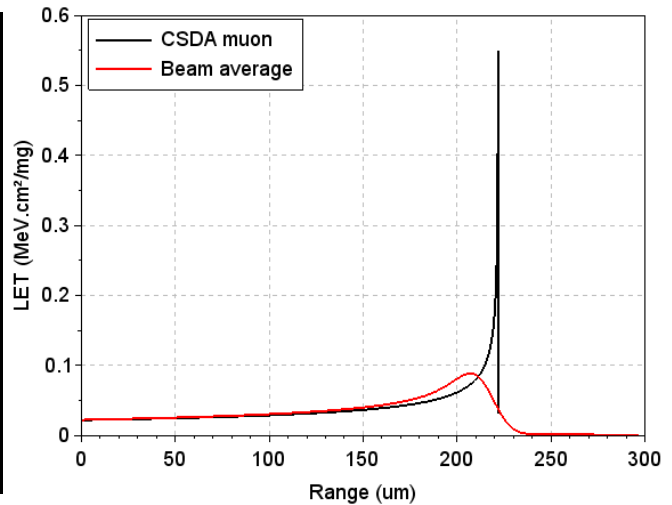


Figure 11: Ionization generated / stopping force experienced by a CSDA antimuon (black curve), and average ionization generated by an antimuon beam (red curve). The CSDA antimuon curve illustrates that while individual particles may have a narrow Bragg peak, a beam has a smooth Bragg curve because of straggling. Source: Geant4, using the MRED code.

collection volumes (of dimensions comparable to, or smaller than the ionization track). Too small volumes cannot efficiently collect the charges generated along a wide track; in this case, the LET metric does not adequately reflect the maximum amount of charge which can be collected by a circuit.

A variety of software tools have been developed by the community to simulate the transport and stopping of ions in various targets. Among these is the SRIM & TRIM suite [55], which uses a semi-empirical model for simulation. TRIM allows easy energy deposition simulations in simple volumes (layered targets) via a user-friendly graphical interface. The University of Jyväskylä developed its own semi-empirical tool for heavy-ion LET estimation in silicon targets, called the European Component Irradiation Facilities Cocktail Calculator [56], to assist beam users planning their experiments. Simulations involving more complex volumes can be made using custom scripts for the Geant4 physics toolkit [57], or specialized software based on Geant4, such as Vanderbilt University's Monte-Carlo Radiative Energy Deposition tool (MRED) [58].

## 2) Range straggling and Bragg curve

Radiation-matter interactions are stochastic in nature; two charged particles from the same accelerated beam, at the same initial energy and hitting the same target, will be affected differently by the target atoms. In particular, at low energy, nuclear scattering with different impact parameters (or off target atoms of different species) leads to a significant dispersion in the path of the incident particles. This dispersion in the particle paths creates a dispersion in their range (the depth at which a particle will stop in a target) called range straggling, which particularly affects light particles such as protons, muons and electrons. This means that different individual particles from a monoenergetic beam will likely experience their Bragg peak at different depths; the result is that the mean ionization created by a particle beam follows a curve with a smoother peak, called the Bragg curve [50]. Figure 10 shows the dispersion of a monoenergetic 2 MeV antimuon beam in a silicon target. Figure 11 compares the average ionization generated by a 2 MeV antimuon beam to the ionization generated by an antimuon which would behave according to the Continuous Slowing-Down Approximation (CSDA). This model assumes that the particle

always experiences the average stopping force theoretically matching its energy, and travels along a straight path. Figure 11 illustrates the fact that the LET of a particle can vary by more than an order of magnitude over distances of a few micrometres, as it decelerates in a target.

Knowing the Bragg curve of a particle beam and its range dispersion in the target as a function of the beam energy is important when planning an irradiation campaign, to ensure an appropriate interpretation of the test results.

## Chapter III – Memory devices

### A. General principles

#### 1) History

Memory components are ubiquitous in computer systems, where their function is to store data. Several different technologies may be used to manufacture memory components; in the early days of the computer, data storage was implemented with macroscopic devices which sometimes relied on mechanical action for their operation, such as core memories, delay line memories, magnetic tapes and hard drives. While the latter two technologies are still in use nowadays, the use of fragile mechanical parts creates reliability and performance issues, and for this reason they are progressively coming to obsolescence.

In the late 1960's, new types of memory devices were developed, which do not rely on any mechanical parts for their operation, but instead are implemented on a single integrated circuit. These are called solid-state memories. Depending on their storage mechanism, solid-state memories can be divided into two categories:

- Volatile memories, which do not retain information if their power supply is disconnected. Volatile memory technologies generally produce fast and low-latency data storage, which makes them ideal as data caches and buffers in fast computer systems. However, this comes at the expense of high power consumption, and sometimes more complex operation and lower storage density/capacity. Examples of volatile memory technologies are Static Random-Access Memory<sup>3</sup> (SRAM) and Dynamic Random-Access Memory (DRAM).
- Non-volatile memories, which retain the data if their power supply is disconnected. If the environmental conditions are right (temperature, electric and magnetic fields, etc.), the data can be retained over at least several decades; for this reason, they are often included in computer designs to be used as storage memory. Non-volatile memory technologies generally offer low (or zero) standby power consumption, high storage density and capacity at low costs per bit, while their common drawbacks are slow operation, high latency and relatively poor read/write endurance. Examples of non-volatile memory technologies are Electrically-Erasable Programmable Read-Only Memory (EEPROM) and flash memory.

The present study aims at studying the effects of radiation on solid-state memories exclusively. For convenience, in the rest of this document, the expressions “memory component”, “memory device” or “memory” will be used to refer to solid-state memories.

#### 2) Memory architecture

Most solid-state memories share a similar architecture: they present a series of external connectors (called “leads”, “pins” or “pads” depending on their shape) which are used to operate it – typically an address bus, a data bus, control signals for read/write signalling, and sometimes a clock signal. At the heart of the component, connected to the external pins via bonding wires, is a piece of silicon called the

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<sup>3</sup> In Random-Access Memories (RAMs), the access latency does not depend on the order in which data are accessed. This is the case for most solid-state memories, and is in contrast with electromechanical storage technologies such as hard disk drives or magnetic tapes, where a reading head must be positioned at the correct physical position on the storage medium to read the data.

memory die, which is cut in a single silicon crystal. The connectors, bonding wires and memory die are encapsulated in a plastic or ceramic package. Embedded in the memory die is an integrated circuit, on which two regions can be defined:

- The memory array, in which the data is stored in a multitude of simple individual circuits called memory cells (generally only one bit is stored per cell). Each memory cell is made of one or more transistors, and sometimes other elements (e.g. a capacitor) depending on the technology. The cells are organized in rows and columns, along which run power supply, ground, control and data lines which connect the cells in parallel.

Traditionally, the term “word line” is used to designate the control lines running “horizontally” along the rows of the array, which are used to “select” the cells, while “bit line” is used to designate the control/data lines running “vertically” along the columns and connected to the cells’ inputs and outputs. However, these terms may vary from one technology to the other.

- The peripheral circuitry (or more simply, “the periphery”), which is located around the memory array and is used to access, write to and read from it. The periphery also regulates the memory array’s supply voltage. It is always implemented using CMOS technology<sup>4</sup>.

Depending on the technology, the output of a memory cell may be either a voltage level or a current level, which amplitude will depend on the cell’s logic state. To correctly evaluate this logic state, the output must be compared to a reference value. One possible solution is to embed reference voltage (or current) sources in the chip; this has the advantage of minimising the silicon area, but makes the system vulnerable to possible drifts in the output of the reference source (caused e.g. by temperature variations, accumulated dose, etc...). The system robustness to parametric shifts can be greatly enhanced by adopting a differential architecture, at the expense of doubling the area required by the memory array. In differential architectures, each single bit is stored in two separate half-cells, with one holding the actual bit and the other holding its complement; to read one bit, the two half-cells are read and their outputs are compared.

The physical storage location of a bit within the memory array depends on two factors:

- The **address scrambling** scheme, which attributes an address bit to each stage of the address decoder. There is no “standard” address scrambling scheme, and the information is typically not readily released by the manufacturer. This means that two words whose addresses are related (differ only by a few bits) might effectively be stored in very different regions of the die.
- The **bit interleaving** scheme. It is common for several words to be stored on the same row, in such a way that each word’s bits are distant from each other. Figure 12 illustrates how the bits (weights 7 to 0) of words A, B, C, D, E, F, G and H could be interleaved on a single row. Bit interleaving allows bits of similar weight to be placed next to each

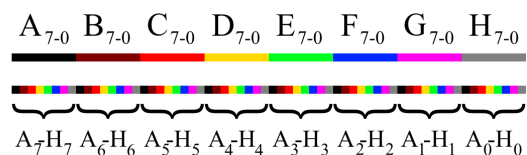


Figure 12: Illustration of an arbitrary bit interleaving scheme (bottom row) involving eight words A to H (color code on the top row).

<sup>4</sup> Complementary Metal-Oxide-Semiconductor technology, or CMOS, refers to the practice of implementing logical functions using both P-type and N-type field-effect transistors (MOSFETs), to form logically complementary structures. CMOS technology is the most popular technology for integrated circuit design, mainly because of its low static power consumption.

other; this makes it easier to multiplex their associated bit lines into a single sense amplifier. Interleaving also brings a higher immunity to Multiple-Bit Upsets (MBU, see next chapter); a single particle is less likely to affect several bits of the same word if their memory cells are distant from each other.

### 3) Operation

To perform an operation on the memory, a command must be sent by setting its control inputs at specific values according to a pre-established timing. An access is made to the memory location designated on the component's address bus: the periphery sets several transmission gates<sup>5</sup> to electrically connect the control and data lines of the relevant memory cells to the periphery's. The periphery decodes the command (typically "read" or "write") and accordingly readies subsystems for the operation to come:

- for a "read" operation, the states of the accessed memory cells are determined. For example, in SRAMs, this is done by pre-charging all bit lines to a certain voltage, then selecting the row containing the relevant cells. The cells containing e.g. a logic '0' will discharge their bit lines faster than the cells containing a logic '1'; after a short period, the voltages of the bit lines are evaluated by very sensitive analog circuits called sense amplifiers. This evaluation gives the information stored in the memory cells; this information is stored in an output buffer, and output on the memory's data bus.
- for a "write" operation, the bit lines are each set at '1' or '0' depending on the data to be written; then, the word containing the relevant memory cells is selected, and the data in these cells will be overwritten by the information stored on their bit lines.

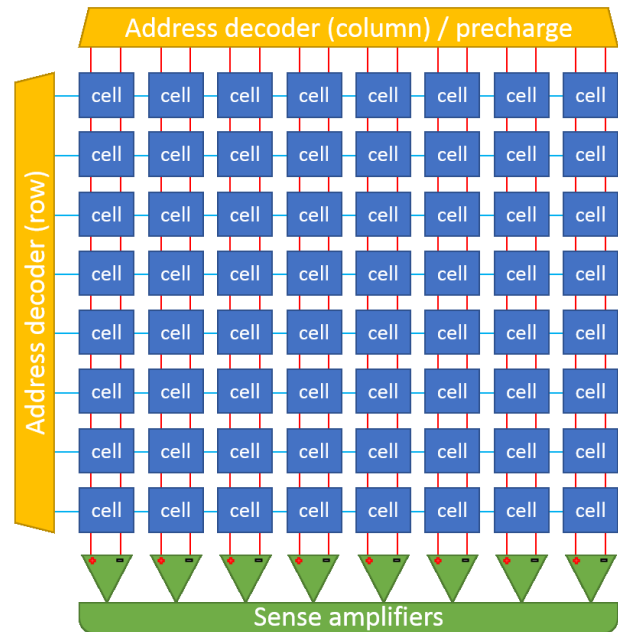


Figure 13: Organization of an SRAM memory block's cells and peripheral circuitry. The same principles apply to most other memory technologies, although the number of bit lines and control lines may differ. Power supply and ground lines are omitted for clarity.

The exact sequence of operations carried out on the control lines depends on the technology used to manufacture the memory cells, some of which will be reviewed in the next section.

<sup>5</sup> A transmission gate is a CMOS circuit used to electrically connect or disconnect two signal lines. The transmission gate has one control input, one data input and one data output. It is made of two transistors (one NMOS and one PMOS) connected in parallel to the two data terminals; both of their gates are connected to the control input, but one (e.g. the PMOS' gate) is complemented by an inverter. When the control gate is at '1', the PMOS can transmit high voltage levels to from the data input to the output, while the NMOS can transmit low voltage levels. If the control gate is at '0', no voltage transmission can occur through either the PMOS or the NMOS, so the input and output are effectively disconnected.

## B. Memory cell technologies

The following subsections introduce various memory cell technologies. This section is not intended to be an exhaustive list, but rather a quick overview of the state-of-the-art. SRAM, DRAM and flash technology are well-established and by far dominate the market. FRAM and MRAM memories are two emerging technologies which offer performances comparable to SRAM and DRAM cells while achieving non-volatility.

### 1) Static Random-Access Memory (SRAM)

First released to the market by Intel in 1969, Static Random-Access Memories (or SRAMs) have since then been the choice devices for high-performance applications. Typical SRAM cells (Figure 14) are made up of six transistors; two of them are used as access transistors, while the other four form two interconnected inverters. The outputs of the inverters are connected to each other's inputs, so that their configurations are always stable and complementary. The two possible inverter configurations are used to represent the data stored in the cell; this configuration disappears if power supply is disconnected, so SRAM memory is volatile.

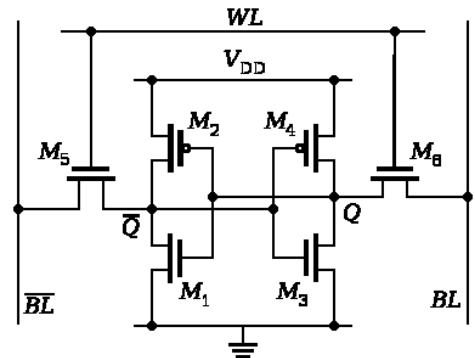


Figure 14: Schematic of an SRAM memory cell. Figure from the public domain. WL = word line, BL = bit line.

SRAM cells allow extremely fast read/write performance (as low as 10 ns), low power consumption (particularly when idle), excellent endurance and easy manufacture (complete compatibility with standard CMOS manufacturing processes). However, since they contain many transistors, SRAM cells require a large die area; this means that they cannot reach very high densities, and makes them expensive to manufacture. Another drawback of SRAM memories is their vulnerability to radiation (as detailed in Chapter 4). Their typical usage is in high-performance standalone memories, or as embedded memory within a more complex chip (e.g. processors and field-programmable gate arrays, FPGAs) where they are used to implement registers and caches.

Two different models of SRAM were used to provide data for this study; the main results are presented in Chapter 7.

### 2) Dynamic Random-Access Memory (DRAM)

Dynamic Random-Access Memory (DRAM) cells are made of one access transistor (sometimes two) and one capacitor (Figure 15). The capacitor may or may not be charged, which is used to represent '0' or '1' logic states. Leakage current through the access transistor(s) and/or the capacitor lead to capacitor discharge; this means that DRAM cells are volatile and must be periodically "refreshed" (rewritten) to retain their information (hence the "dynamic" name). Reading the cell also discharges the capacitor, which means that the cell must be rewritten after each read.

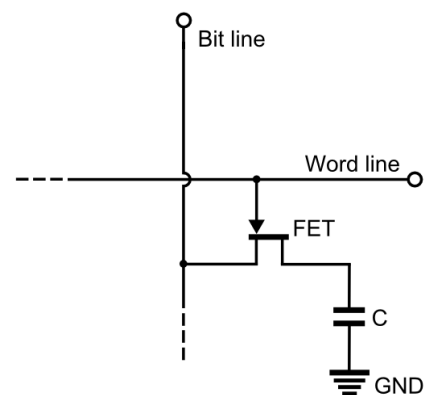


Figure 15: Schematic of a DRAM memory cell. Figure from the public domain.

DRAM cells allow fast read/write performance (down to a few tens of nanoseconds) and do not require much area for

implementation (in particular since the advent of stacked-capacitor and trench-capacitor technology). This makes DRAM an ideal technology in applications where large quantities of high-performance memory are required at a reasonable cost (e.g. computers' general-purpose working memory). One drawback of DRAM technology is its need for complex driving circuits, due to the need to perform periodic refresh operations. DRAM memory cells are also sensitive to radiation.

DRAM technology's sensitivity to radiation was not surveyed in this study; the present section is included for information only, as DRAM is a well-established technology.

### 3) Flash memory

Flash memories consist of a structure called a floating-gate metal-oxide-semiconductor field-effect transistor (MOSFET). Floating-gate MOSFETs have an additional gate between the control gate and the channel, which can be charged or discharged by hot carrier injection and tunnelling through the thin surrounding dielectrics. The quantity of charge stored in the gate allows the MOSFET to reach two (or more, in the case of multi-level cells) levels of conductivity, which is used to determine the cell's logic state. Figure 16 exhibits a schematic cross-section view of a flash memory cell.

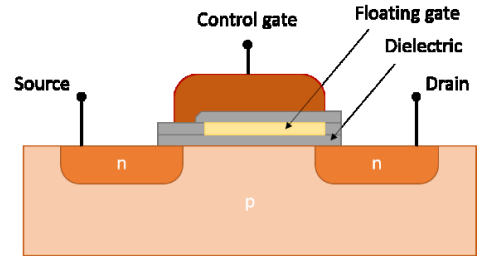


Figure 16: Cross-section schematic of a flash memory cell.

Flash memory cells are non-volatile, which means that they will remain in their logic state (and hence preserve the data) if the power supply is discontinued. Since they only consist of one transistor, they can achieve extremely high packing density, which makes their cost per bit very competitive. However, they require high operating voltages, do not achieve high read/write performance, and have poor endurance (generally thousands up to hundreds of thousands of erase cycles). These characteristics make flash memories most suitable for long-term and/or mobile data storage applications.

The interested reader can turn to Ref [59]. for more information on flash technology. Flash memories are sensitive to radiation, as detailed in Chapter 4, and some of the results gathered on flash memories during this study's irradiation campaigns are available in Chapter 7.

### 4) Ferroelectric Random-Access Memory (FRAM)

In a similar fashion to DRAM cells, FRAM cells are made of one access transistor and one ferroelectric capacitor (Figure 17). In place of the traditional dielectric layer, this component uses a ferroelectric material to separate the two capacitor electrodes, which can be set in one of two possible electric polarizations by applying strong external electric fields. The built-in potential allows the ferroelectric capacitor to retain its charge over periods ranging from at least one year to virtually unlimited, depending on the device's operating temperature [60]. Reading the cell information is done by discharging the capacitor to the bit line; this operation effectively destroys the information. Hence, like DRAM cells, FRAM cells must be restored (re-written) after readout. [61]

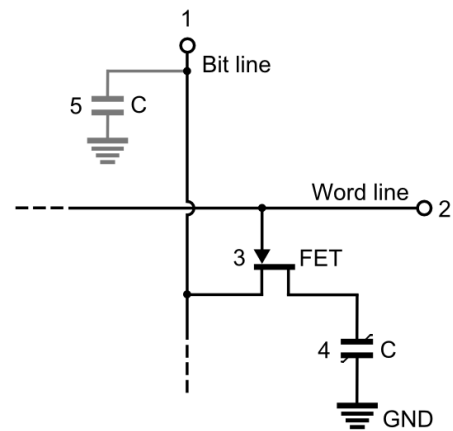


Figure 17: Schematic of an FRAM cell. Figure from the public domain.



FRAM memories allow fast access and read/write times (a few tens of nanoseconds), have excellent endurance, low power consumption and are non-volatile, which means that FRAMs could take on some of the roles traditionally taken on by fast volatile memories and slow non-volatile memories. FRAM memory cells have the additional advantage to be immune to radiation; however, the peripheral circuitry of FRAM devices is implemented with traditional CMOS technology, so FRAM devices as a whole are not immune to radiation. The results of this study’s irradiation campaigns on FRAM devices are available in Chapter 7.

### 5) Magnetoresistive Random-Access Memory (MRAM)

MRAM cells consist of a magnetoresistive element, called a magnetic tunnel junction (MTJ), which is sometimes associated to an access transistor (Figure 18). The MTJ consists in one layer of material with a fixed magnetic polarization, and one or more layers with a variable magnetic polarization (or “free layers”), which can be oriented by the application of external magnetic fields. The resistance of the MTJ is low when the layers are polarized in the same direction, and its resistance is high when their polarizations differ. The logic state of the cell can be sensed by applying a certain voltage and sensing the output current. Writing data to the cell is done by passing carefully-timed current pulses through the bit and word lines, with the induced magnetic fields coercing the free layer(s) into a new polarization.

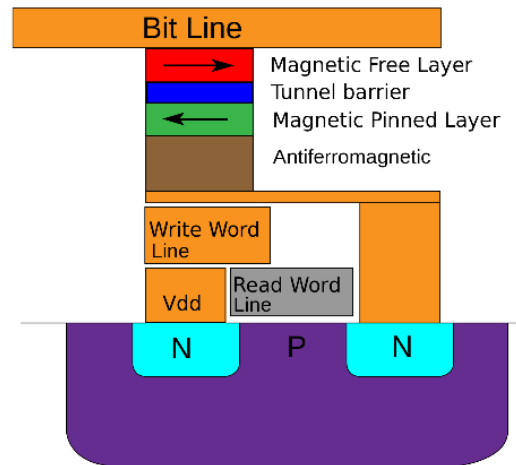


Figure 18: Cross-section schematic of an MRAM cell. Figure from the public domain.

Several variations of the MRAM technology have been developed – namely, toggle MRAM, spin-torque-transfer MRAM (STT-MRAM) and thermal-assisted switching MRAM (TAS-MRAM). The latter two are a refinement of the toggle MRAM technology, and all three rely on MTJs. The technical differences are beyond the scope of this thesis, but the interested reader can turn to Ref. [62] for an extensive review of the state of the art of MRAM technology. These memories are vulnerable to strong magnetic fields and tend to have a large active power consumption, but they have short access and read/write times (a few tens of nanoseconds), excellent endurance, can be scaled easily (in the case of STT-MRAM) and are non-volatile, which means that much like FRAMs, they could take on some of the roles traditionally taken on by fast volatile memories and slow non-volatile memories.

### C. Device manufacturing

The manufacturing of complex devices such as memory components, which can incorporate several billion transistors, is an automated process taking place in ultra-clean rooms, requiring a sequence of hundreds of separate, carefully tuned processing steps.

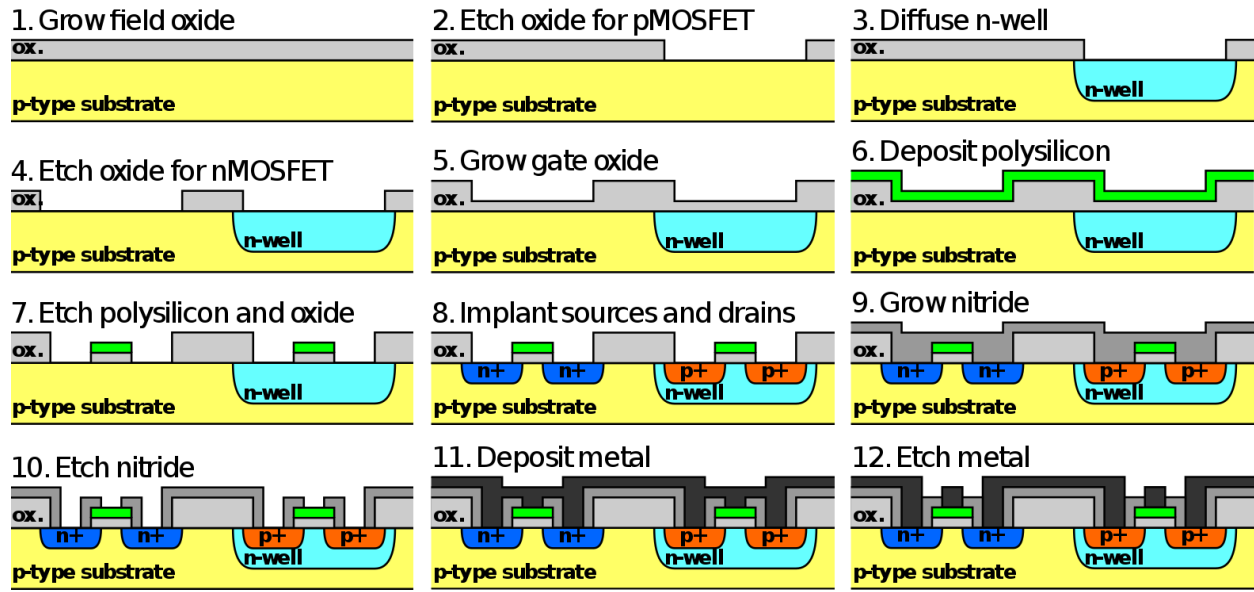


Figure 19: Illustration of the major steps in the fabrication of a PMOS and an NMOS transistor on a P-type wafer. Figure from the public domain.

The process starts by slowly growing a large semiconductor crystal - generally silicon, sometimes specialty materials such as germanium or gallium arsenide. (The largest crystals can be up to 300 mm in diameter as of 2017.) The crystal is then cut in slices a few hundreds of micrometres in thickness called wafers<sup>6</sup>.

The wafers are then subjected to several steps of chemical-mechanical polishing, oxidation, etching, ion implantation, and photolithography to form the active regions of the future transistors within the wafer; these steps constitute the so-called Front-End of Line processes (FEOL). The latter step, photolithography, consists in the deposition of a layer of light-sensitive compound called a photoresist on the surface of the wafer. The photoresist is then covered by a light-blocking mask reproducing the features to be implemented in the wafer, and irradiated with UV light. The mask is then removed and the photoresist is chemically developed, leaving behind a patterned layer of photoresist which can be used to selectively expose the wafer to various treatments (e.g. ion implantation, material deposition...). The photoresist layer can then be removed chemically or mechanically. After the completion of FEOL processes, the transistors are formed on the wafer, but they are still isolated from each other.

The Back-End of Line processes (BEOL), which consist of additional steps of oxide deposition, chemical-mechanical polishing, etching, photolithography and metal deposition, are used to create several layers of interconnecting wires and vias (connections from layer to layer) which are required to connect the transistors together. Modern devices may contain over 10 of these interconnect layers above the active silicon. At the surface of the chip, a thick dielectric layer (sometimes referred to as a “passivation layer” is deposited to insulate and protect the fragile active layers. Bonding pads are also created on the sides of the chip, which will be used as connection points for input and output signals. After the end of the BEOL processes, the wafer contains a mosaic of chips.

<sup>6</sup> This process is true for all “bulk” technologies, where the wafer is a simple slice of a large semiconductor crystal. For other technologies, such as Silicon-on-Insulator, extra steps are needed to produce a wafer.

Finally, the wafer is tested (the individual chips each undergo functional testing, which is done by applying contact probes to the bonding pads and test pads) and thinned from the back (backgrinding). The individual chips are separated from each other (generally by cutting the wafer with a diamond saw), tested again, packaged, and tested one final time.

## Chapter IV – Radiation effects on memory components

In Chapter 2, the basic mechanisms of radiation-matter interaction were introduced. This chapter will focus on the effect of radiation on complex structures, made of materials with different properties and sometimes subjected to electric fields, such as transistors and other components found inside integrated circuits.

### A. Total Ionizing Dose (TID) effects

TID effects take place when devices containing dielectrics (or “insulators”) are exposed to ionizing radiation. Insulators are materials allowing very little electrical conduction to take place, because of their high electrical resistance. This is a consequence of their electronic band structure: their valence band is completely filled, their conduction band is completely empty, and the two bands are separated by a large band gap. This means that electrical insulators have extremely low concentrations of free charge carriers (free electrons and holes), which are necessary for electrical conduction to take place. A detailed exposition of electronic band theory would be beyond the scope of this work – but the reader can turn to the first chapters of Ref. [47] for further explanations.

As discussed in the previous chapters, when ionizing radiation interacts with a target material, free charge carriers (electrons and holes) are generated. When the target material is an insulator, the resulting free carriers have very low mobility (holes particularly so) [48]. In the absence of an applied electric field, the free carriers will not be separated and are likely to recombine (one free electron and one hole can annihilate each other). However, if the irradiated insulator is subjected to an electric field, the carriers can drift; the electrons will be swept towards the higher potential while the holes will remain in place in the material, due to their lower mobility. Over time, the bulk of an electrical insulator subjected to ionizing radiation will accumulate positive charge, because of the trapping of holes. Additionally, the generation and transport of holes in the oxide can have the effect of liberating otherwise static impurities forming neutral impurity complexes (such as  $H^+$  and  $OH^-$  ions introduced during oxide growth). Under the right bias conditions, these ions can drift until they reach the Si-SiO<sub>2</sub> interface, where they can react with Si-H bonds (forming H<sub>2</sub>), Si-OH bonds (forming H<sub>2</sub>O) and leaving behind dangling Si bonds [63]. This results in the presence of trapping centres at the interface, which can trap either positive or negative charge carriers, depending on the conditions. This accumulation of charge will affect electric fields within and surrounding the insulator. When this occurs within an integrated circuit, its operation can be affected; the consequences of the generation and subsequent accumulation of positive charge carriers (holes) in insulating materials within an electronic device are designated as Total Ionizing Dose (TID) effects.

Several factors impact this charge trapping mechanism, with some of the most important being the presence and magnitude of an electric field in the insulator (component bias voltage), the insulator’s temperature and thickness, and the presence of defects in its structure which can act as hole traps. Discussing these factors would be beyond the scope of this work, but the interested reader can turn to Ref. [64] for a review of the mechanisms behind TID effects.

Two typical examples of TID effects will be given in this section. One is the creation of parasitic conducting paths along the edges of transistor channels. On Figure 20, a three-quarters schematic view of an accumulation-type N-type Metal-Oxide-Semiconductor Field-Effect Transistor (N-MOSFET) is given. Along the edges of the transistor are two large blocks of silicon dioxide; these are insulation trenches (commonly

referred to as Shallow Trench Isolation, or STI, in the literature), and their purpose is to electrically isolate each transistor from its neighbours. If the transistor is exposed to ionizing radiation, and these oxide trenches build up positive charge, then free electrons from the p-type substrate will naturally tend to accumulate near the boundary between the channel and the insulation trench, which runs between the drain and the source. This means that even when no bias is applied to the gate, a conductive path exists between the two transistor electrodes. This effect can be seen as an increase in leakage current, or as a shift in gate threshold voltage for narrow-channel transistors [65].

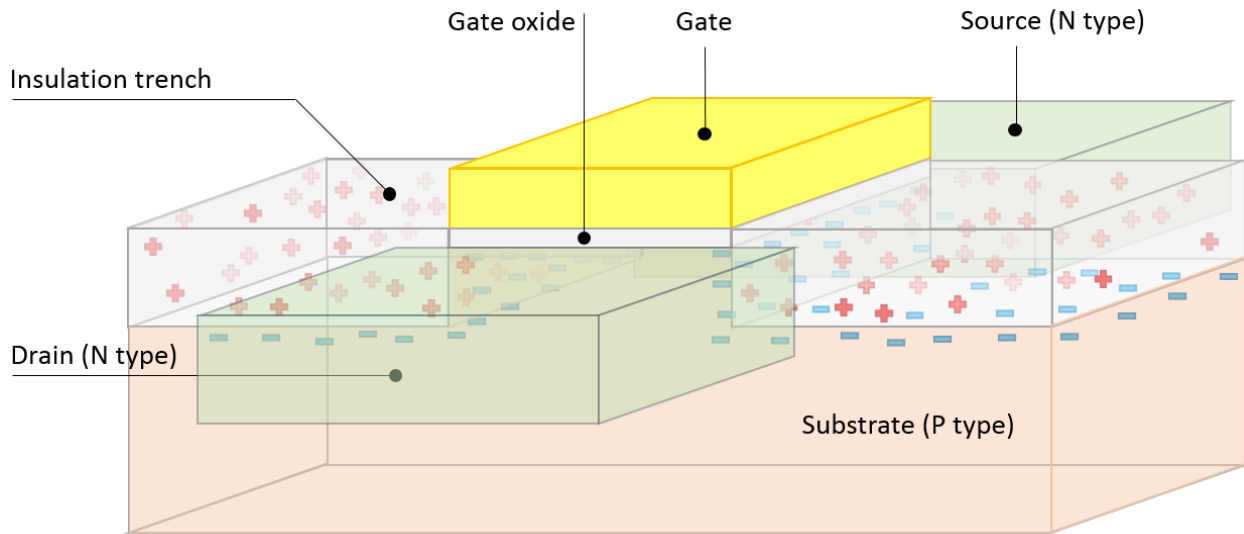


Figure 20: Transparency view of a field-effect transistor surrounded by two thick oxide insulation trenches (grey structures). The oxide's accumulated positive charge (red crosses) attracts electrons (blue bars) from the P-type substrate, which form an inversion layer of electrons at the boundary region. This creates a conductive path between the N-type drain and source regions (green boxes in the front and back), which allows leakage currents to flow through the transistor, even when no positive bias is applied to the gate (yellow plate).

A solution to this type of TID effect is to design edgeless transistors (see Figure 21). Since the channel completely surrounds the source, and since there is no insulation trench running between the source and drain, no radiation-induced parasitic path can exist between them.

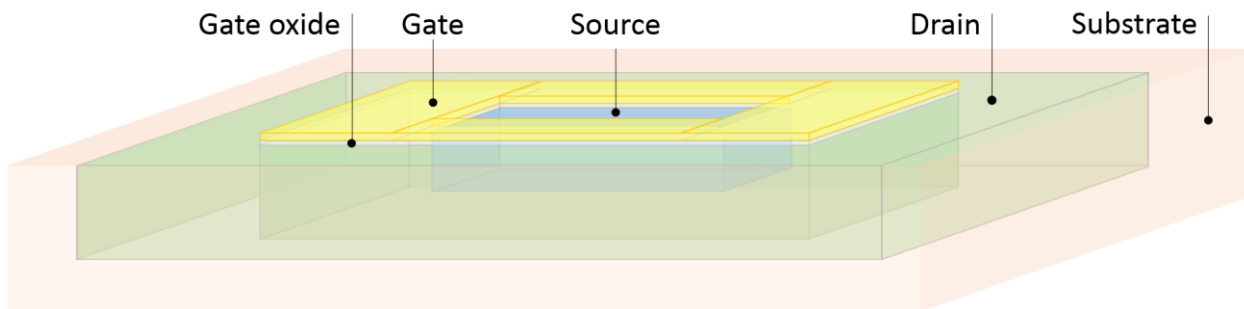


Figure 21: Transparency view of an edgeless transistor design. The transistor source (blue box) is surrounded by the gate (yellow ring plate) and the drain (green ring). The transistor channel, below the gate, has the shape of a ring surrounding the source, and hence has no "edge". The transistors are insulated from each other by insulation trenches which run between their drains (not shown here); there is no insulator near the channel or source. This means that even if oxide charging occurs, there will be no parasitic conductive channel between the drain and source.

The floating-gate MOSFETs at the heart of flash memory cells also suffer from TID effects. Charge-generated holes accumulating in the insulators surrounding the floating gate can drift, be collected by the gate and recombine with the trapped electrons, thereby neutralizing part of the stored charge. Additionally, the accumulation of positive charge around the gate partially masks the eventual negative charge stored in the gate. These two mechanisms lead to a drift in the floating-gate MOSFET threshold voltage with increasing TID [66]; beyond a certain point, this drift will prevent a correct evaluation of the cell's logic state, causing data corruption.

## B. Single-Event Effects (SEEs)

Single-Event Effects are events where the operation of an electronic component is affected by the strike of a single energetic particle. Unlike TID effects, which appear after extended periods of radiation exposure and require charge build-up, SEEs are prompt phenomena which take place on a timescale generally measured in nanoseconds, and can occur in pristine devices. There are several subcategories of SEE [67]:

- Single-Event Transients, or SETs. These can be momentary voltage excursions in the output of an analog circuit, or a transient change in the output value or in an internal node of a logic circuit;
- Single-Event Upsets, or SEUs. These cause the disruption (upset) of the logic state of one or more memory cells. SEEs resulting in only one upset are called Single-Bit Upsets, or SBUs, while those resulting in several upsets are called Multiple-Cell Upsets, or MCUs. If several of the upset cells belong to the same logic word, then the event is referred to as a Multiple-Bit Upset, or MBU.
- Single-Event Functional Interrupts, or SEFIs. During a SEFI, an electronic component loses some or all functionality. These events are generally caused when a device's control circuitry is affected by radiation, which places it in an unpredicted logic state. They may be either transient or stable; in the latter case, cycling power to the device is required to recover functionality. SEFIs may also be permanent if an internal component is damaged.
- Single-Event Latch-up, or SEL. These events occur in bulk semiconductor<sup>7</sup> devices, when the current induced by the collection of charge generated by an ion strike turns on a parasitic thyristor structure (PNPN or NPNP) under bias inside the component. SELs do not occur in Silicon-on-Insulator (SOI) devices [68], which do not contain PNPN parasitic structures [69].
- Single-Event Burn-out, or SEB. These occur when an ion strikes a semiconductor junction under very high reverse electrical bias (as is the case in power devices). In power diodes, the radiation-induced charge carriers (and eventual secondary avalanche-generated carriers) locally raise the temperature of the semiconductor; this allows a transition between a stable low-current bias point to a stable high-current bias point on the device's I-V curve, generating additional heating and inducing positive feedback [70]. In power MOSFETs, the collection of radiation-induced charge carriers may cause a voltage drop in the body potential; this may turn on a parasitic transistor (NPN structure) between the source and drain [71]. In either case, the ensuing high current leads to device destruction by thermal runaway (burn-out).

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<sup>7</sup> "Bulk" refers to manufacturing technologies where the component is implemented on a monocrystalline silicon substrate. This is in opposition to Silicon-on-Insulator technologies, where the substrate contains layers of insulating material (typically silicon dioxide or sapphire).

- Single-Event Gate Rupture, or SEGR, where a single energetic particle strike results in the breakdown of the gate oxide. This leads to an increase in gate leakage current, and can lead to device failure [72].

The present work deals mainly with the first four categories, with a focus on SEUs and SEFIs.

To understand the root causes behind SEUs and SEFIs, it is necessary to understand the mechanisms by which the charge deposited in a semiconductor during an ion strike can be collected. As was discussed in Chapter 2, charged particles passing through a semiconductor generate a “cloud” of free charge carriers along their path. In the absence of an electric field, there will be no carrier drift; the electrons and holes will remain close to each other and are likely to recombine, and only a minor fraction of the deposited charge may reach a conductor via diffusion and be collected. Conversely, if an electric field is present (as is the case across PN junctions<sup>8</sup>), the generated holes will drift towards the lowest potential, while the free electrons will drift towards the highest potential. This charge separation prevents recombination and leads to a high collected charge yield. As the charge carriers get collected at the semiconductor-metal interface, a current pulse occurs at the component’s terminals – which will translate into a voltage pulse depending on the capacitance of the connected nodes. This pulse can disrupt the circuit, and create events such as SETs, SEUs and SEFIs. The following subsections will illustrate these possibilities.

### 1) Single-Event Transients (SETs)

Figure 22 represents a logic circuit made up of two OR gates and one AND gate connected in series, which will be used to illustrate SETs and the conditions. Let us consider a situation where input terminals A, B and C are at a low voltage (logic ‘0’) and input D is at a high voltage (logic ‘1’). In this situation, the output terminal S is at ‘0’.

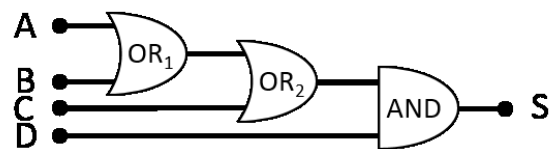


Figure 22: Schematic of logic circuit made of two OR gates and one AND gate connected in series.

If one of the output transistors of OR<sub>1</sub> is struck by an ion, a voltage pulse may appear at the output of OR<sub>1</sub> – and so at one of the inputs of OR<sub>2</sub>. If this pulse is high and long enough, it will affect the output of OR<sub>2</sub>, which will briefly output ‘1’. In turn, the transient at the end of OR<sub>2</sub> will be captured by the AND gate, and the output of the whole circuit S will briefly register ‘1’. This temporary change in the value of the circuit caused by a single ion strike is caused a Single-Event Transient.

For an SET to produce an error, certain conditions on the ion strike position and generated pulse characteristics must be met, notably [73]:

<sup>8</sup> A PN junction is the boundary between a P-doped and an N-doped region of a semiconductor. This structure possesses unique electrical characteristics; in particular, under neutral or reverse bias (N side at a higher potential than the P side), the electrons close to the boundary on the N side will recombine with the holes closer to the boundary on the P side. In this case, around the PN junction, the semiconductor will be depleted of its free charge carriers, and the charge coming from the dopant atoms will produce an electric field spanning across the depletion region.

PN junctions are the elementary building blocks of many electronic components, such as PN diodes, bipolar junction transistors and field-effect transistors.

- the pulse must be high and long enough to affect the following gate(s); otherwise it will fade out through electrical masking. Indeed, all logic gates have a limited bandwidth, and will not respond to small enough perturbations in their inputs.
- the following gate or memory element must be able to latch the pulse; indeed, a transient voltage pulse occurring at the input of a synchronous (clocked) gate outside of its temporal latching window will not be propagated at the output. This is called temporal masking.
- the ion must strike a critical node – that is, a node which, if upset, will impact the logic nodes downwards. For example, let us consider another situation where A, B, C and D are at '0'; in this case, the occurrence of an SET at the output of OR<sub>1</sub> or OR<sub>2</sub> will not be able to propagate until the output node S, because the second input D of the AND gate is '0'. This is an example of logical masking.

Single-Event Transients can also occur in analog circuits – for example, voltage pulses at the output of a voltage amplifier or charge pump.

## 2) Single-Event Upsets (SEUs)

An SEU is the corruption of the data contained in one or more memory cells following a particle strike. Typically, SEUs occur after an ion strike located directly on the memory cell (or in its vicinity), with the ensuing charge collection disrupting the cell's state. They can also result from an SET occurring in the peripheral logic during a write operation. The mechanisms at play behind SEUs differ depending on the memory cell technology.

Figure 23 illustrates the series of events by which an SRAM cell is upset by an ion strike:

- The left-hand schematic represents the cell in its initial state: red lines are at a high potential and blue lines at a low potential, green transistors are in on-state and black transistors are in off-state.
- The central schematic illustrates the effect of an ion strike on an off-state MOSFET: the transistor is effectively turned on as the charge collection generates a current pulse. Its inverter is disturbed, and its output temporarily raised to an intermediary potential between the ground and  $V_{DD}$ . Since this output is connected to the input of the second inverter, the second inverter may in turn be disturbed and its output lowered to an intermediary potential, inducing a positive feedback on the first inverter.
- The two unstable inverters may either recover their original states, or stabilise in opposite states (right-hand schematic); in the latter case, the cell has effectively been upset and its data corrupted.

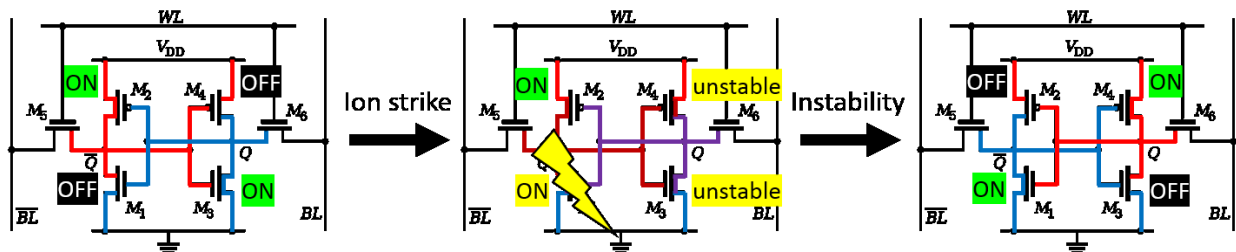


Figure 23:: Illustration of an SRAM cell being struck by an ion and suffering an SEU.

Flash memory cells can also suffer from SEUs. As discussed in Chapter 3, flash memory cells are made of a floating-gate MOSFET. The cell can be written to by emptying or storing electrons in the floating gate,



which is located between the channel and the control gate. The presence or absence of charge in the floating gate modifies the threshold voltage of the transistor (by “screening the control gate”), and determines whether the cell will be read as containing a ‘0’ or a ‘1’. In a flash memory array holding random data, the threshold voltages  $V_{th}$  of the cell population follow a statistical distribution, such as seen on Figure 24 (black curves).

Heavy ions striking a flash memory cell affect its threshold voltage. The phenomenon is reviewed in [74]. The underlying mechanisms are not yet perfectly understood, but the most likely explanations are:

- the formation of a transient conductive path through the gate oxide, allowing the discharge of the floating gate [75];
- a transient carrier flux: the excitation of the trapped carriers by the impinging particle gives them enough energy to tunnel out of the floating gate [76];
- positive charge trapping around the floating gate [77].

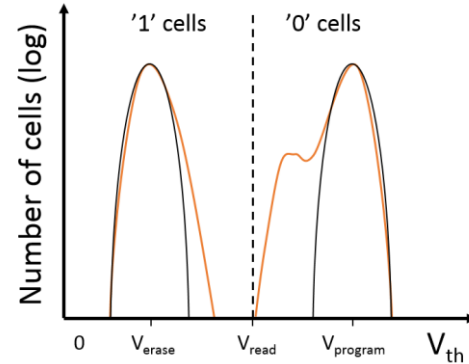


Figure 24: Distribution of the threshold voltages of the memory cells in a flash array after arbitrary data writing (black curves), and after subsequent heavy-ion irradiation (orange curves).

Regardless of the mechanism (or combination of mechanisms) at play, the consequence of heavy-ion irradiation is a modification in the threshold voltage distribution of the irradiated cell population (orange curve in Figure 24). The threshold voltages of the cells hit by heavy ions shift towards an “intrinsic” value, while the threshold voltages of the rest of the cells are unaffected. This gives rise to secondary peaks in the distribution of threshold voltages; the height of these peaks is determined by the ion fluence, and their distance to the main peaks by the ion LET and the electric field in the gate oxide [74]. Cells whose threshold voltage come to cross the limit voltage  $V_{read}$  will, upon reading, be interpreted as holding the wrong data – which constitutes an SEU.

Some memory cell technologies are inherently resilient to SEUs, because they rely on other physical mechanisms than charge storage to store information. For instance, FRAM memory cells have demonstrated invulnerability to direct upset by heavy ions up to xenon between 0° and 60° (effective LETs<sup>9</sup> of 64 MeV.cm<sup>2</sup>.mg<sup>-1</sup> and 128 MeV.cm<sup>2</sup>.mg<sup>-1</sup> respectively) at fluences of 1.5\*10<sup>7</sup> cm<sup>-2</sup> and 1.0\*10<sup>6</sup> cm<sup>-2</sup> respectively [78]. MRAMs also exhibit heavy-ion SEU invulnerability up to xenon at 60° (effective LET 112 MeV.cm<sup>2</sup>.mg<sup>-1</sup>) at a fluence of 1.0\*10<sup>7</sup> cm<sup>-2</sup> [79]. The main radiation hardness concern for these memory cell technologies is the formation of crystalline defects via displacement damage. However, since the CMOS peripheral circuits used to drive the memory cells are typically much more sensitive to radiation, the sensitivity of the memory cells is not a limiting factor. In Chapter 7, the results of radiation test

<sup>9</sup> The “effective LET” is a metric used to compare the effects of irradiation with particle beams striking the target at different incidence angles. The effective LET is equal to the normal ion LET divided by the cosine of the angle of incidence (this means that the effective LET is always superior or equal to the normal LET). This model allows for a simplified comparison of results obtained with different beams, but shows its limits when the dimensions of the charge collection volume are small.

campaigns carried out on FRAMs for the needs of this study show that the CMOS periphery is the sole contributor to the devices' failures.

### 3) Single-Event Functional Interrupts (SEFIs)

When ion strikes produce SETs or SEUs in critical locations of a memory's periphery, these circuits may accidentally enter a state where they cannot perform their designed function. This causes a category of events known as Single-Event Functional Interrupts, or SEFIs. By nature, SEFI scenarios can broadly differ from one device model to another, since SEFIs are heavily dependent on the design of the device's peripheral circuitry.

To illustrate SEFIs, let us consider the following, simplified memory array block in Figure 25. Even though the block is only meant to contain four 8-bit words, it is common practice to implement the block with redundant columns (and lines, not shown here). This is done to improve manufacturing yield: when a defective column is detected during factory testing, the manufacturer can reassign the faulty column to a spare, thereby "saving" the memory block. Without this redundancy mechanism, defective elements (which are a very common occurrence in complex integrated circuits) would compromise device operation, and the compromised devices would need to be discarded.

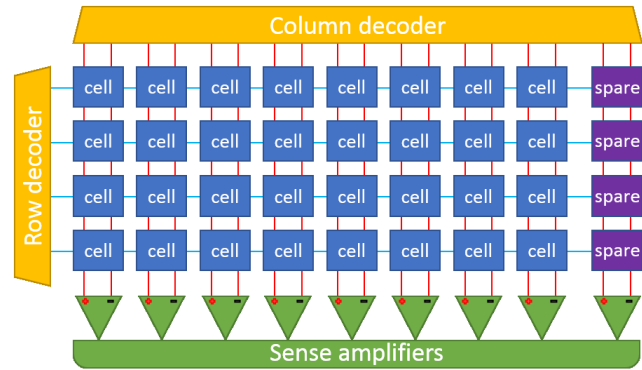


Figure 25: Schematic representation of a memory block containing four 8-bit words and one spare column.

The column reallocation operation can be done during factory testing via several methods, such as using sets of electrically-set or laser-set fuses and antifuses to connect and disconnect signal lines. Some devices, however, are reorganized programmatically; this is done by rewriting internal non-volatile memory (distinct from the general-purpose memory array) dedicated to redundancy information storage. When the device is powered up, this information is fetched from the non-volatile redundancy memory and loaded into redundancy registers<sup>10</sup>, which in turn drive transmission gates and other circuits, leading to the desired array reorganization.

If an SEU occurs in a redundancy register controlling spare column reallocation for our considered memory block, the spare will be used to replace the original column, so that the data contained in the spare will be fetched during subsequent memory accesses. However, since the spare contains arbitrary data, which likely does not match the data of the original column, subsequent accesses to this memory block will return erroneous data as long as the SEU in the hardware register is not corrected.

This is only one example of numerous possible SEFI scenarios. Further examples of SEFIs, identified in test data gathered throughout the course of this work, will be presented in Chapter 7.

<sup>10</sup> Hardware registers are circuits which are closely related to memory cells. They can store data, and they are typically implemented using latches – bistable circuits whose operation principle is similar to that of SRAM cells. However, they also have special hardware-related functions beyond those of ordinary memory. The information stored in register cells – their logical state – can be used to directly impact the configuration of other logical circuits in the device.

#### 4) Single-Event Latch-ups (SELs)

Single-Event Latch-ups, or SELs, occur when the passage of a charge particle and subsequent charge carrier collection triggers a parasitic PNPN structure (thyristor) within the component, thereby creating a self-sustaining conducting path between two conductors at different potentials. A high current may flow through the semiconductor, which can have detrimental consequences on the component's performance: higher power consumption, high IR drops<sup>11</sup> in internal lines, stuck signals, and possibly device destruction via thermal runaway.

Figure 26 illustrates a typical configuration of N-type and P-type regions inside a CMOS circuit (in this case, implemented in a P-type substrate). Two parasitic bipolar junction transistors (BJTs) can be identified: an NPN between the NFET's source (as an emitter) and the N-well, with the P-type substrate as a base; and a PNP between the PFET's source (as an emitter) and the P-type substrate, with the N-well as a base. The base of the parasitic NPN is connected to the GND tap<sup>12</sup>, but the silicon substrate and semiconductor-metal junction have a relatively high resistance; the same can be said of the PNP's base, loosely connected to the  $V_{DD}$  well tap through the N-well.

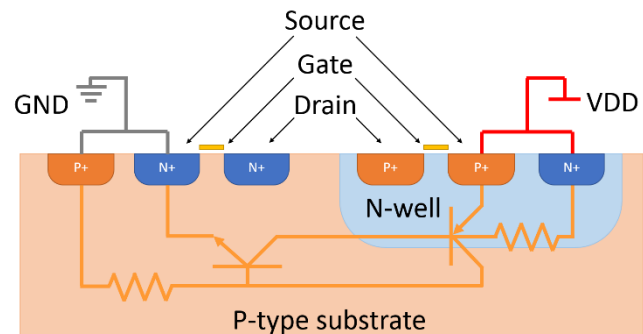


Figure 26: cross-section schematic view of a P-type substrate containing an N-type MOSFET, and a P-type MOSFET in an N-well (a typical structure in CMOS circuits). The parasitic thyristor's NPNN structure is indicated by the orange circuit diagram.

If an ion strikes through the N-well, the generated charge carriers will be separated by the electric field; the holes will recombine with the majority carriers in the N-well, while the electrons will drift towards the N+ well tap at  $V_{DD}$ . If enough electrons are collected, their motion through the low-doping, resistive N-well will create a temporary voltage drop in the well. If this voltage drop is sufficiently high, the P+ source of the PFET will start to emit holes through the N-well and into the P substrate, thereby turning on the parasitic PNP. The injected holes will travel through the substrate to the P+ electrode contact at GND. If enough holes are injected, their motion through the low-doped silicon will induce such a rise in substrate voltage that the N+ source of the NFET will start to emit electrons through the P-type substrate and into the N-well. These electrons will be collected by the N+ electrode at  $V_{DD}$ ; at this point, each BJT is injecting minority carriers into the other BJT's base, creating a positive feedback loop which allows a sustained flow of current from the  $V_{DD}$  to the GND supply rails. The current flows through the bulk of the silicon and bypasses the gates of the MOSFETs entirely, which means that the latch-up current cannot be influenced via the MOSFET gates; the only way to recover from this situation is to lower the potential of the  $V_{DD}$  supply rail (or switch power off entirely) until the parasitic BJTs turn off.

It is sometimes possible to design components in a way which minimizes the risks of SEL onset. SOI components, for example, are immune to SELs, because their architecture does not contain the PNPN

<sup>11</sup> IR drops are voltage drops in a signal or power line caused by the resistance of the line itself.

<sup>12</sup> Well taps, also called well ties, are used to set (or "tie") the potential of a semiconductor to a reference potential. In Fig. 7, the leftmost P+ contact is a well tap setting the substrate at the GND potential, and the rightmost N+ electrode is a well tap tying the N-well to  $V_{DD}$ .

structures necessary to SEL onset; each transistor is isolated from its neighbours by the buried oxide and the field oxide [69]. It is also possible to harden bulk devices against SELs by using lower bias voltages, higher substrate doping concentrations (to lower substrate resistivity), additional well taps (to lower the substrate-reference junction resistivity) and careful geometry (to minimize the gain of the parasitic BJTs). SELs are more likely to occur at high temperatures and at high impinging ion LETs.

SELs are serious failures, because of the potential for component damage via thermal runaway. It is possible to mitigate the effects of SELs by protecting components with delatcher circuits; these act as switches placed in series with the power source of the component to be protected, turning off when the supply current exceeds a threshold value. This solution has its limits, though, as SELs can produce parasitic current flows of various intensities, which may not necessarily produce an appreciable change in the component's main current consumption. What's more, some devices (e.g. memories, processors, FPGAs) have naturally varying power consumption profiles (depending on their activity), so finding an appropriate current consumption threshold is not always possible.



## Chapter V – Radiation testing of memory components

When trying to assess the radiation sensitivity of a component, it is common practice to obtain experimental data via radiation testing. This chapter will introduce the standard procedures and methodologies for Radiation Hardness Assurance (RHA) testing in general, and for radiation testing of memory components in particular.

### A. Radiation Hardness Assurance

As discussed in the previous chapters, radiation can have detrimental effects on electronic components. The build-up of ionizing dose can lead to TID effects; displacement damage can degrade material properties and component performance; finally, individual particle strikes can trigger non-destructive (SET, SEU, SEFI) and destructive failure events (SEFI, SEL, SEB, SEGR). The high level of system reliability required in some applications (typically space, aeronautics and automotive engineering) makes Radiation Hardness Assurance (RHA) a key process in achieving mission success. RHA typically involves the following steps:

- At the mission proposal/feasibility phase: definition of the radiation specifications
  - Preliminary radiation environment specification (particle spectra and flux, peak and average)
  - RHA specification (at system level): mission duration, technical performance goals, availability, required design margins, test requirements...
- At the Preliminary Design Review (PDR):
  - Final radiation environment definition
  - Preliminary shielding analysis using preliminary spacecraft layout
  - Final RHA specification (at equipment level). This will allow adequate parts selection.
- At the Critical Design Review (CDR):
  - Evaluation of radiation data of the parts selected after PDR. (Engineers tend to favour parts with existing radiation data and a favourable operational history. When no such parts are available, or when existing parts do not meet requirements, then new parts must be identified, procured and tested.)
  - Final shielding analysis
  - Circuit design analysis: failure rates computed from radiation testing data and predicted shielded radiation environment
- After CDR:
  - Radiation Lot Acceptance tests. Since devices can differ from lot to lot without notice, it is important to ensure that the most critical parts used on the mission hardware behave as expected under radiation. To this effect, other devices from the same production lot are tested.
- After Launch:
  - Failure analysis. This generates feedback on the RHA process, allowing eventual mistakes to be avoided in the future, and consolidating the operational history of the selected parts.

N.B.: This process is not rigid by nature; during a project's development, several iterations of a design may be submitted for radiation hardness evaluation, fall short of specifications, be revised and submitted again. Part selection is not the only means of ensuring equipment reliability: specific circuit-level design techniques may be used to make up for component-level shortcomings - for example, the use of Triple

Modular Redundancy (TMR) and Error-Correcting Codes (ECC). The equipment may also be positioned in another, less exposed region of the spacecraft.

The RHA process depends on the radiation data available to system designers. This data measures a component's resilience to disturbance by radiation: for example, its parametric shifts as a function of accumulated dose, or its failure rate in a given environment. This data comes partly from the feedback of previous missions, but the main means of acquiring radiation data on a component is via radiation testing. The data's accuracy and associated uncertainty are crucial for the reliability of the final system; hence radiation testing has been standardized by the main actors in the industry.

## B. Testing standards and methodologies

To accurately predict a component's degradation during its mission, it is necessary that the irradiation represents the mission's radiative environment. As discussed in Chapter 1, space radiation environments may include very high energy particles (above one GeV per nucleon). What's more, the particle fluence accumulated by a spacecraft during its mission (which can last over two decades) can reach extremely high values. Recreating these conditions in a reasonable amount of time requires facilities capable of generating high-intensity, high-energy radiation: this is why SEE tests are typically carried out at particle accelerators, while TID tests are done using cobalt-60 irradiators. These facilities have high operating costs and limited beam time availability; this explains why component test campaigns are expensive, and sometimes lengthy operations.

All major space agencies (ESA, NASA, JAXA...) have created series of testing standards for Electrical, Electronic and Electro-mechanical (EEE) components to assist system designers and facilitate RHA processes. Among the main series of standards are those published by the European Space Components Coordination (ESCC) [80] and the Joint Electron Device Engineering Council (JEDEC) [81]. These standards help ensure that the generated radiation data meets high enough levels of confidence and repeatability for critical applications. For example, the ESCC Basic Specification No. 25100 [82], entitled "Single-Event Effects Test Method and Guidelines", gives directions for SEU testing, notably on the following points:

- Particle beam characteristics: energy (for protons) or LET in silicon (for heavy ions), flux, energy and dosimetry error...
- Condition of the device under test (DUT): closed or delidded, in air or in vacuum, temperature monitoring, number of samples to be tested, standards for traceability...
- Electrical parameters for testing: bias voltages, operating frequencies, data patterns...
- Test plan requirements: total fluence to be deposited, minimum number of energy/LET steps to be carried out, recommendations regarding TID effects during SEE testing...

Radiation test data generated according to the specifications of this ESCC standard may be submitted to the ESCC for inclusion in an online radiation data repository, the ESA Radiation Reports [83]. An equivalent US repository is the NASA Goddard Space Flight Center's Radiation Database [84]. These structures have been created to facilitate data exchange, speed up RHA processes, and avoid redundant radiation testing.

Typically, memory components undergo a TID test, a proton SEE test and a heavy-ion SEE test. The reason for carrying out separate proton tests is that protons represent the largest share of the ion fluence received by a spacecraft. However, heavier ions can have much higher LETs and are more likely to trigger failures, hence the need for heavy-ion SEE testing. Obtaining separate heavy-ion and proton response

data for a component also allows failure rate predictions in environments with different proton and heavy-ion spectra (e.g. GEO and LEO orbits).

### C. Concepts and metrics for radiation testing

To effectively assess a component's response to radiation, it is important to have appropriate metrics and to measure the relevant variables. These depend on the component type; the ECSS Basic Specifications (e.g. [82] for SEE and [85] for TID) and ECSS Detail Specifications (e.g. [86] for certain types of asynchronous SRAMs) provide guidelines as to which parameters are relevant for monitoring during a test campaign.

During SEE testing of memory components, three types of failure events may occur: SEU, SEFI and SEL. An SEE radiation testing campaign shall determine:

- The device's SEU cross-section (as a function of LET for heavy ions, and as a function of particle energy for protons). This represents the sum of all sensitive areas on the die surface which if hit by an impinging ion, and if enough energy is deposited, will produce an SEU. Its formula is:  $\sigma_{SEU} = \frac{\#errors}{fluence}$

The SEU cross-section is typically zero at low particle energy/LET, then increases sharply past a certain energy/LET threshold, and eventually tends towards an asymptotic maximum value at high energy/LET. Two important values reflect this behaviour:

- The SEU threshold LET/energy, below which the device is effectively insensitive to SEU.
- The saturation SEU cross-section, which is the asymptotic value towards which the SEU curve tends at high LET/energy.

It is common to create a Weibull fit of the SEU cross-section curve; this Weibull curve is simply defined by the threshold SEU/energy, the saturation cross-section, a scale and a shape parameters, which makes it a convenient input for further standardized single-event rate calculations.

It is also interesting to consider the device's SEU cross-section per bit; this metric allows a comparison of the radiation sensitivity of memory components of different capacity. Its formula is:

$$\sigma_{SEU\ bit} = \frac{\#errors}{fluence \times \#bits}$$

- The device's LET threshold for SEL occurrence (if possible, as a function of supply voltage; otherwise, at the nominal operating voltage).
  - The minimum bias voltage for SEL occurrence (if different bias voltages can be tested)
- The device's SEFI cross-section (as a function of particle LET/energy).

TID testing campaigns, on the other hand, shall determine the drift of the component's electrical parameters (e.g. main supply current, input/output pin current, memory access delays...) and eventual failures as a function of accumulated dose. The parameters to be monitored depend on the component type, and are defined in a series of ECSS Detailed Specifications.



## D. Algorithms for memory testing

To adequately detect faults occurring in a memory device, the choice of testing algorithm is important. A variety of memory test algorithms have been developed, which are routinely used by manufacturers to check the functionality of their devices. Among these test algorithms, “March tests” are the most commonly used at production level because of their high effectiveness and their low complexity (linear with the size of the memory). March tests consist in one or more “elements” (sequences of read and write operations) to be applied to every memory address in a given order. Manufacturing defects can induce several types of faults in memories, including (not exclusively) [87]:

- Stuck-at fault (SAF), where the state of a memory cell is stuck to either ‘0’ or ‘1’, and cannot be changed;
- Transition fault (TF), where a memory cell is incapable of switching from one state to the other;
- Coupling fault (CF), where the state of a cell (victim) is influenced by the state or operations carried out on another cell (aggressor);
- Neighbourhood pattern sensitive fault (NPSF), where the state of a cell is determined by the state of a set of neighbouring cells;
- Address decoder faults (AF), where either:
  - with a certain address, no cell will be accessed;
  - a certain cell will not be accessible;
  - with a certain address, multiple cells are accessed simultaneously;
  - a certain cell can be accessed with multiple addresses.

and various combinations of these basic faults.

Without going in too much detail – the interested reader can turn to [87] and [88], which are comprehensive reviews of chip testing techniques – each of these types of basic faults requires a specific sequence of operations to be sensitized and observed. This implies that algorithms may be incapable of detecting all types of faults; for example, the March C algorithm [89] can detect SAFs, TFs, and unlinked CFs (CFs which involve cells not involved in other faults), while the MATS+ algorithm [90] can only detect SAFs. Testing algorithms also differ in the time (i.e. the number of operations) they require to be completed. A shorter testing algorithm will allow faster testing, which represents a gain in productivity for manufacturers.

March algorithms can effectively be applied to the detection of radiation-induced upsets. Since the DUTs used in irradiation campaigns have successfully passed factory checks, and are *a priori* entirely functional, the algorithms used in radiation testing campaigns focus on other specifications:

- **Minimization of error masking.** The point of a radiation testing campaign is to detect radiation-induced upsets. Memory cells are typically upset between the last operation performed during element N and the first operation performed during element N+1, because in this relatively long interval, the algorithm is performed on the rest of the array, leaving the cell idle. SEUs are only observed when the affected cells are accessed and read; this means that most SEUs are detected by the first read operation of an element. This also means that algorithms with elements starting with a write operation will, at some point, destroy information related to upset cells by overwriting all the cells without reading them first. Hence, using an algorithm with little or no

masking effect (i.e. few or zero elements starting with a write operation) will ensure an efficient data collection.

- **Stimulation of the peripheral circuitry.** Different testing algorithms will put different levels of stress on different parts of the periphery. For example, it is possible to use algorithms with very short elements (down to a single operation) and scanning the memory array in an order that maximizes switching activity in the address decoders; conversely, it is also possible to minimize the switching activity. Such algorithms have been used in this study, and are described in Chapter 6.
- **Maximal sensitization of the memory cells.** Certain algorithms can create conditions that maximize the sensitivity of the memory cells. An example is the Dynamic Stress Test developed in [91], which relies on two key effects:
  - When an SRAM cell is read, it is selected by pulling its word line up (see Chapter 4, Figure 14); this has the effect of discharging the bit line connected to the low node of the cell (the inverter with the NMOS transistor ON). The current passing through the open NMOS raises the potential of the low node, making the cell less stable during the duration of the read operation – and more vulnerable to SEU. In the meanwhile, all the other SRAM cells on the row are also selected by the word line, and discharge the bit lines connected to their low nodes (all bit lines are generally left at a high voltage as long as their block is accessed, to speed up operation). All the cells on the same row suffer the same destabilization as the accessed cell, an effect known as Read Equivalent Stress (RES) [92].
  - Carrying out several successive read operations on an SRAM cell (“read hammering”) improves the chances of detecting resistive-open defects [92].

By performing successive read operations on each memory cell, the Dynamic Stress Test combines these two effects to increase the sensitivity of all the memory cells in a given row of a memory block at any given time. This can result in a non-negligible increase in the overall cross-section of SRAM devices [93].



## Chapter VI – Experimental setup

This chapter will present the test benches used to gather radiation data, and the software tools created for data processing.

### A. Test setups

#### 1) Selected devices

- **Cypress CY62177EV30 MoBL**, a 90-nm technology, 32-Mibit<sup>13</sup> SRAM in a 48-pin TSOP type I package. This device has the particularity of embedding two 16-Mibit memory dies stacked vertically within a single package.

Each die is divided into 2 planes, each plane has 64 blocks, each block has 2048 rows, and each row contains 8 words of 8 bits. The 64 bits of each row are positioned according to an 8-bit interleaving scheme.

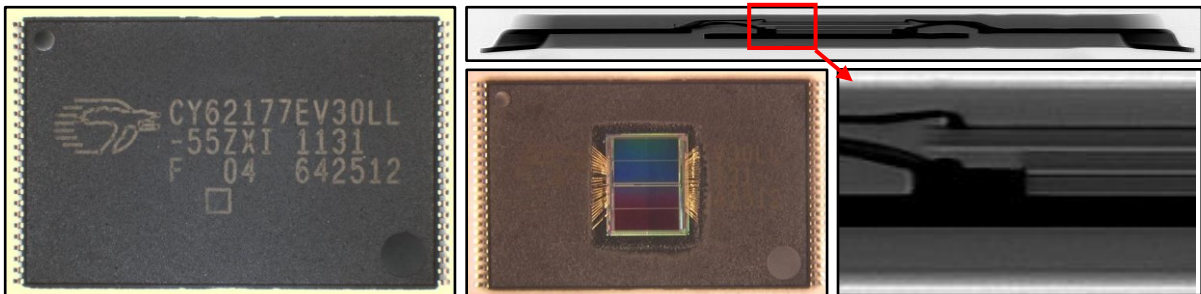


Figure 27: Top views of one closed and one delidded Cypress CY62177EV30 devices, and side X-ray view of the device. The side X-ray view zoom-in highlights the stacked-dies architecture, with bonding wires appearing on two levels.

- **Cypress CY62167GE MoBL**, a 65-nm technology, 16-Mibit SRAM in a 48-pin TSOP type I package. This device embeds an Error-Correcting Code (ECC) functionality, which enables the correction of single-bit errors, and can be activated or inhibited at device startup using a specific sequence of inputs. The device is pin-to-pin compatible with the SRAM90.

The memory array is divided into 2 halves, each divided into 2 quads, each divided into 2 octants; each of the eight octants is divided into 8 blocks. Each block holds 32768 words of 8 bits.

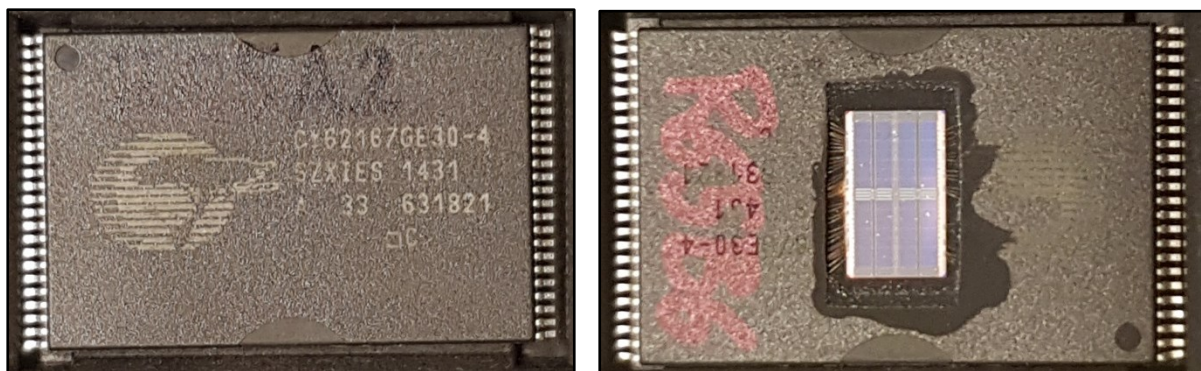


Figure 28: Top views of one closed and one delidded Cypress CY62167GE devices.

<sup>13</sup> One mebibit (symbol: Mibit) is a binary multiple of the bit. 1 Mibit =  $2^{20}$  bit =  $2^{10} \cdot 2^{10}$  bits = 1,048,576 bits.

- Cypress FM22L16**, a 130-nm technology, 4-Mibit FRAM in a 44-pin TSOP type II package. This part was originally manufactured by Ramtron International, and is now manufactured by Cypress Semiconductor after it acquired Ramtron in 2012. Devices from both manufacturers were used during this study. This component has the largest memory capacity available on the FRAM market. The memory array is divided into 8 blocks, each divided into 8192 pages; each of these holds 4 words of 16 bits. The device has a special page-wise operation mode which allows faster access times.

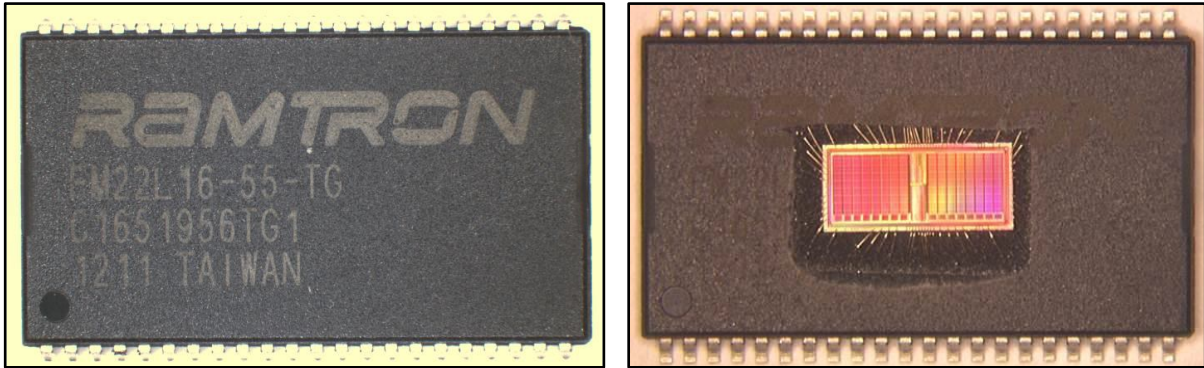


Figure 29: Top views of one closed and one delidded Ramtron/Cypress FM22L16 devices.

- Everspin MR4A08B**, a 16-Mibit toggle MRAM in a 44-pin TSOP type II package. This is the largest toggle MRAM capacity available from Everspin, which is currently the only manufacturer of standalone MRAM devices. The MRAM is pin-to-pin compatible with the FRAM. Each word contains 8 bits.

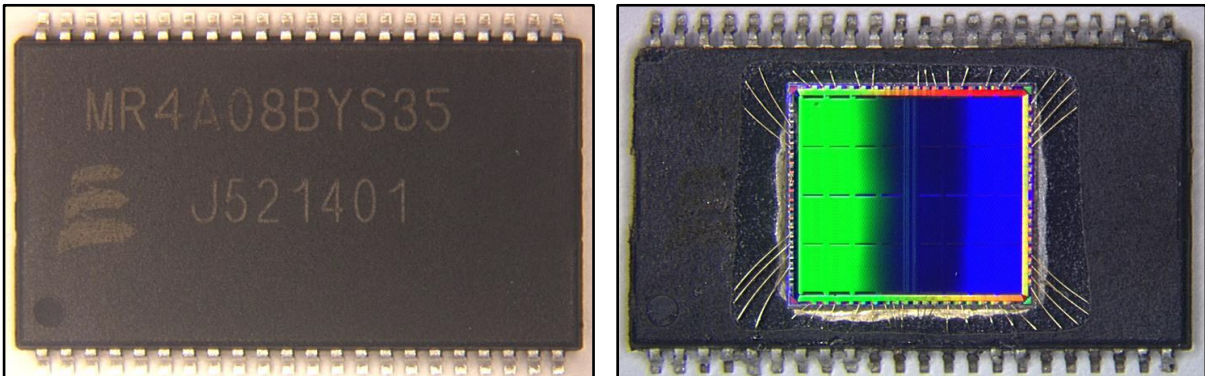


Figure 30: Top views of one closed and one delidded Everspin MR4A08B devices.

- Micron 29F32G08ABAAA**, a 32-Gibit flash memory in a TSOP type I package. The device is not pin-to-pin compatible with the SRAM65 and SRAM90. The memory array is divided into 2 planes, each divided in 2048 blocks, each divided into 128 pages of 8192 columns. Each column holds one 8-bit word.

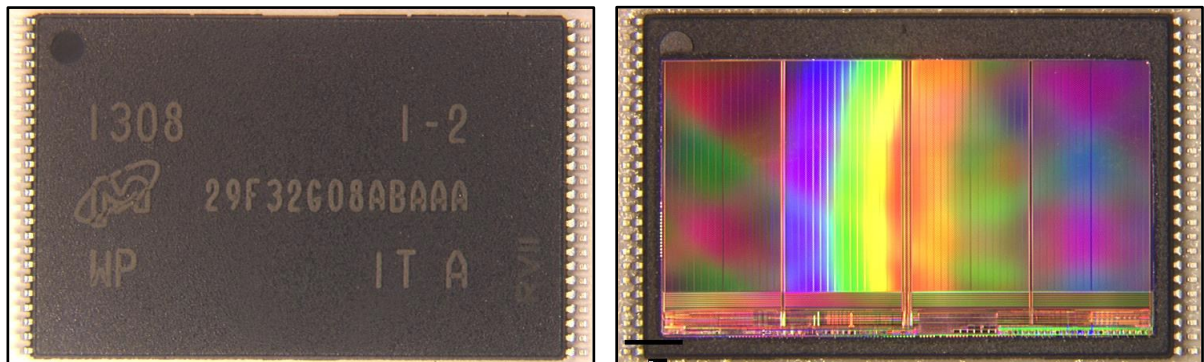


Figure 31: Top views of one closed and one delidded Micron 29F32G08ABAAA devices.

For convenience, future references to these devices will be made as **SRAM90**, **SRAM65**, **FRAM**, **MRAM** and **flash** respectively.

These devices are all COTS. They were procured in several steps, either directly from the manufacturer or from retailers. The delidding operations, when not carried out by the manufacturer (SRAM65), were done in several batches by SERMA Technologies (SRAM90, FRAM, MRAM, flash) and ESA-ESTEC (flash).

## 2) Standalone memory test bench

The several standalone memory test benches which were used to gather experimental data during this study are successive iterations of a design developed at LIRMM. At the core of the design is a Digilent Spartan-3 Starter Board Rev. E (which will be referred to as **DSSB**; see Figure 32), which embeds a Xilinx Spartan-3 XC3S200 FPGA. The DSSB has three 2\*20 pin expansion connectors, which can be used to connect expansion boards, either directly or indirectly using ribbon cables.



Figure 32: Top view of the Digilent Spartan-3 Starter Board (DSSB).

Several expansion boards were designed to interface the standalone memory devices with the DSSB. These expansion boards include Zero Insertion Force (ZIF) open-top sockets mounted on a mezzanine board. The SRAM90 and SRAM65 devices, sharing the same package and being pin-to-pin compatible (including power pins), were interfaced via the same expansion board; another board was used for the MRAM and FRAM, similarly compatible. A set of jumpers on the expansion boards was used to connect and disconnect signal lines when necessary. The flash memory was tested using a separate board, because of its different pin layout. The use of open-top ZIF sockets and mezzanine boards allowed a direct exposition of the delidded DUTs to the ion beams, while facilitating the replacement of DUTs during testing campaigns and disassembly of the test bench for easy transportation. Figure 33 illustrates these three types of expansion boards.

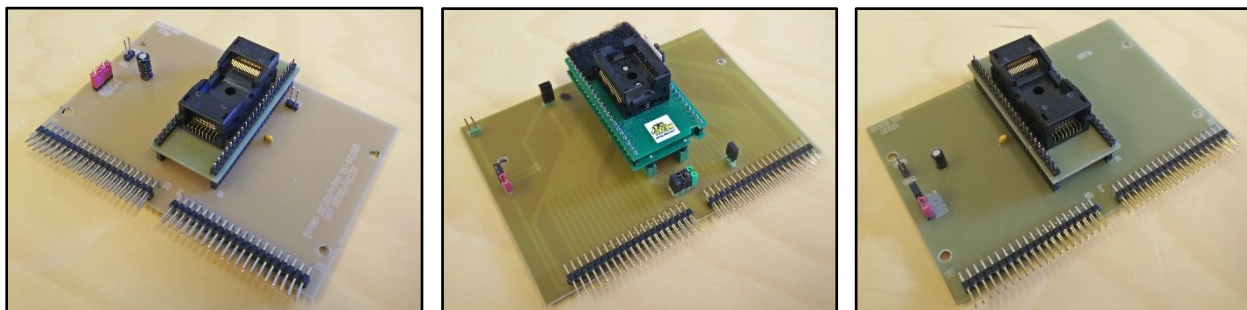


Figure 33: Expansion boards and ZIF sockets for SRAM90 and SRAM65 (left), MRAM and FRAM (centre), and flash devices (right). The top left pair of pin headers are used to connect power for the DUT; the 4-in-line pin headers on the left can be used to connect an optional delatcher mezzanine board; all other jumpers are used to connect and disconnect signal lines.

The expansion boards are equipped with a set of four pin headers, which can be used to insert an optional mezzanine delatcher<sup>14</sup> board in series with the DUT’s power supply (Figure 34). This component senses the voltage drop created by the DUT’s supply current passing through a weak resistor, and disconnects the DUT (via an NPN transistor) if the voltage drop exceeds 50 mV for over 10  $\mu$ s. In such an event, a pulse signal is sent to the DSSB via the expansion board for notification. By choosing the value of the sensing resistor, the user can adapt the delatcher to accommodate different DUT supply current levels. The delatcher restores power to the DUT after 200 ms.

The FPGA was configured with a testing program which was developed in-house, and was continually upgraded over the years. It provides many options for functional testing:

- **Static testing** – the whole memory array is written with either “all 0”, “all 1”, “logical checkerboard” or “data=address” patterns. The “data=address” pattern writes the lower 8 bits of its address vector in every word. The DUT can be read back after irradiation and the data compared with the template to check for SEE-induced errors. Periodic readback operations can be programmed with an adjustable timer; static testing can also be controlled manually with “write X” and “read X” commands.
- **Dynamic testing** – all memory addresses in the array, one by one, undergo a series of read and/or write operations (called an element). Once all addresses have been visited, the cycle repeats with a new element, until the user puts a halt to the test. All the while, the DUT undergoes irradiation. Different dynamic stressing algorithms can be used, as described below<sup>15</sup>:

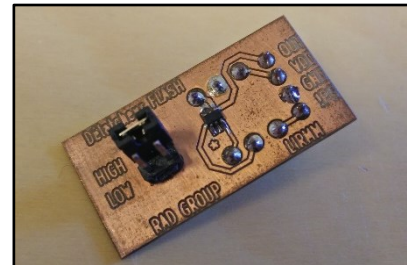


Figure 34: Mezzanine delatcher board. The jumper is used to select one of two different sense resistors.

- **Dynamic stress** [93], [94]:  $\{ \uparrow (r1, w0, r0, r0, r0, r0) ; \uparrow (r0, w1, r1, r1, r1, r1) ; \uparrow (r1, w0, r0, r0, r0, r0) ; \downarrow (r0, w1, r1, r1, r1, r1) ; \downarrow (r1, w0, r0, r0, r0, r0) ; \uparrow (r0, w1, r1, r1, r1, r1) \}$
- **March C-** [95]:  $\{ \uparrow (w0) ; \uparrow (r0, w1) ; \uparrow (r1, w0) ; \downarrow (r0, w1) ; \downarrow (r1, w0) ; \uparrow (r0) \}$
- **MATS +** [90]:  $\{ \uparrow (w0) ; \uparrow (r0, w1) ; \downarrow (r1, w0) \}$
- **mMATS+**:  $\{ \uparrow (r0, w1) ; \uparrow (r1, w0) \}$
- **Dynamic Classic** [93]:  $\{ \uparrow (w0) ; \uparrow (r0) ; \uparrow (w1) ; \uparrow (r1) \}$

<sup>14</sup> Delatchers are circuits used to protect devices in the event of a latch-up occurrence. They are typically connected in series with the device’s power supply, and disconnect them if their supply current exceeds a certain value for a certain period.

<sup>15</sup> Operations are separated by commas, while elements are in parenthesis and separated by semicolons. The arrows in the algorithm descriptions above indicate the direction of address scanning; if the arrow is up, the element will be applied to all addresses from the first to the last, and vice versa.

For all dynamic tests, the order in which memory locations were visited during a cycle could be determined in a number of possible ways:

- **Natural:** the address vector is simply incremented or decremented at each step, so that any addresses  $N$  and  $N\pm 1$  are visited consecutively
- **Fast row:** the address vector is changed so as to scan the memory array row after row\*
- **Fast column:** the address vector is changed so as to scan the memory array column after column\*
- **LFSR:** the address vector is controlled by a linear-feedback shift register (LFSR) configured so that every address is visited exactly once per cycle, in pseudo-random fashion
- **Gray:** the address vector is incremented/decremented as a Gray binary vector (instead of being treated as a natural binary vector). This ensures that only one address bit toggles between two consecutive steps, reducing the activity of the DUT's address decoders
- **Anti-Gray:** the address vector is incremented/decremented as a Gray binary vector (instead of being treated as a natural binary vector), and is complemented every other step. This ensures that all but one address bit toggle between two consecutive steps, maximizing the activity of the DUT's address decoders

\*N.B.: Using the fast row or fast column addressing schemes requires a knowledge of the DUT's address scrambling scheme. This was only available for the SRAM90 and SRAM65 devices.

- **Latch-up testing** – when a delatcher board is connected to the expansion board, the test bench is capable of detecting high DUT power current consumption. Latch-up conditions drawing sufficient current to cause the device to exceed its specifications can be detected using this functionality.

The test bench, comprising the DSSB, expansion board, eventual delatcher, and the DUT, was connected to a computer using the DSSB's RS-232 serial link. A desktop power supply was used to bias the DSSB at 5V and the DUTs at 3.3V.

### 3) Test bench monitoring and control

Both types of memory test benches were linked via an UART to a remote computer. An amateur terminal program, ComTools [96], was used for setup control and data logging. The benches were controlled using 2-byte commands, and sent data and status updates back to the control computer using 6 or 7-byte messages. Messages were sent back to acknowledge command reception, task completion, signal latch-up conditions, and erroneous outputs from the DUT. When reporting errors, a message would contain the error's address, its data, and (for dynamic tests only) mention at which step of the stress algorithm (operation and element) the error was detected.

The typical test run would unfold as follows:

- At first, commands would be used to manually put the test bench in the proper state (write a certain data pattern, or start the desired dynamic stress algorithm).
- The beam would then be started manually; the team conducting the experiment monitors the messages sent from the test bench appearing in real time on the control terminal, as well as the current delivered to the DUT by the power supply. Depending on the situation:
  - If the test run unfolds as planned, the beam would be shut down manually or automatically after reaching a predefined deposited fluence goal.



- If the DUT or test setup enters a critical failure condition (permanent SEFI, severe latch-up, monitoring software crash, etc...), the test would be aborted.
- The test data would be summarily analysed on the spot to determine the DUT response: number of errors, presence or absence of large SEFI, etc... This preliminary information could be used to alter the campaign's test plan if necessary (e.g. adding additional measurement points).
- Later on, extensive data post-processing would be carried out to extract all possible information.

Figure 35 exhibits a sample from a test log obtained during heavy-ion irradiation of an SRAM65.

```

2014/11/07 19:39:00 64 03 41 0D 08 11 64 04 70 8D 10 11 64 04 7B 69 40 11 64 07 3B E9 40 11
2014/11/07 19:39:00 64 08 05 71 20 11
2014/11/07 19:39:00 64 0C BE 46 10 11
2014/11/07 19:39:00 64 16 54 29 20 11 64 16 9F A9 01 11
2014/11/07 19:39:00 64 1C D6 4B 40 11 64 1F 96 CB 40 11
2014/11/07 19:39:01 64 12 14 DF BF 19
2014/11/07 19:39:01 64 0C 06 30 BF 19 64 0A 0D 31 DF 19 64 08 0D B1 DF 19
2014/11/07 19:39:01 64 07 72 D5 BF 19 64 05 CC 8E FE 19 64 05 CC 0E FE 19 64 04 BD 06 FB 19
2014/11/07 19:39:01 64 02 23 EF BF 19 64 02 23 6F BF 19
2014/11/07 19:39:02 64 05 19 98 02 11
2014/11/07 19:39:02 64 0F 65 15 40 11 64 10 A8 EC 02 11
2014/11/07 19:39:02 64 13 D9 98 10 11

```

Figure 35: Excerpt from an SRAM65 heavy-ion test log. The test bench sends 6-byte error messages starting with a header byte (“64” for error notifications), followed by three address bytes, one data byte and one metadata byte. The monitoring terminal groups the messages arriving within 100 ms of each other on a single line, and inserts a timestamp at the beginning of each line.

## B. Data processing

An experimented operator can identify many distinctive features in the error messages appearing on the monitoring console (based on the timing of their arrival, the similarity of their address and data vectors, and the metadata), which can be very useful to monitor the DUT response in real-time during a test run. However, automated tools are necessary to process the vast amount of data generated during a test campaign and to perform complex operations. Two software tools have been developed for this purpose, one in C/C++, the other in Scilab [97].

### 1) C processing

A C/C++ software, the Test log Interpreter and Generator of Extensive Reports (TIGER), was developed in-house to process the test data.

The test logs are read and parsed, and every message is used to generate a pointer to a structure (\*SEU) whose fields contain the error address, data and metadata of the message. The “SEU” structs are then manipulated by a series of sorting and clustering functions (the clustering functions will be discussed further in the next section). A list of “cluster” structures are created; each cluster contains a chain of \*SEU pointers (representing the errors constituting the cluster), the coordinates of its outer boundaries ( $x_{min}$ ,  $x_{max}$ ,  $y_{min}$ ,  $y_{max}$ ,  $t_{min}$  and  $t_{max}$ ), and a pointer to the next cluster.

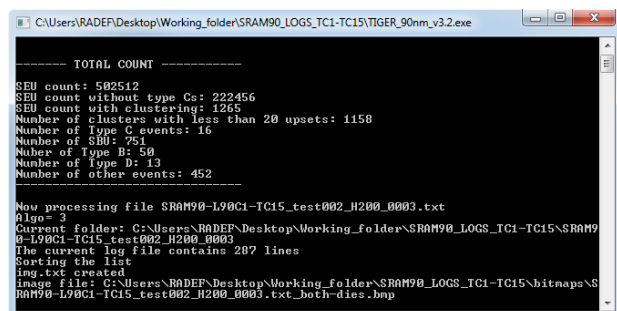


Figure 36: Screenshot of the TIGER tool processing a batch of SRAM90 test logs

Once the errors have been clustered, TIGER can output text files containing the formatted list of clusters and their list of errors. It can also generate **bitmaps**, which are a graphical representation of the data contained in the memory array. On a bitmap, every pixel represents a bit; the pixels can be coloured to indicate whether a bit has suffered an upset or not. Depending on the information available on the device, it is possible to generate several types of bitmaps:

- **Logical bitmaps**, where the words are placed one next to another, line by line, according to their logic address. All the bits of each word are placed consecutively to each other, always in the same order.

0 <sub>0</sub>	0 <sub>1</sub>	0 <sub>2</sub>	0 <sub>3</sub>	0 <sub>4</sub>	0 <sub>5</sub>	0 <sub>6</sub>	0 <sub>7</sub>	1 <sub>0</sub>	1 <sub>1</sub>	1 <sub>2</sub>	1 <sub>3</sub>	1 <sub>4</sub>	1 <sub>5</sub>	1 <sub>6</sub>	1 <sub>7</sub>	2 <sub>0</sub>	2 <sub>1</sub>	2 <sub>2</sub>	2 <sub>3</sub>	2 <sub>4</sub>	2 <sub>5</sub>	2 <sub>6</sub>	2 <sub>7</sub>	3 <sub>0</sub>	3 <sub>1</sub>	3 <sub>2</sub>	3 <sub>3</sub>	3 <sub>4</sub>	3 <sub>5</sub>	3 <sub>6</sub>	3 <sub>7</sub>
4 <sub>0</sub>	4 <sub>1</sub>	4 <sub>2</sub>	4 <sub>3</sub>	4 <sub>4</sub>	4 <sub>5</sub>	4 <sub>6</sub>	4 <sub>7</sub>	5 <sub>0</sub>	5 <sub>1</sub>	5 <sub>2</sub>	5 <sub>3</sub>	5 <sub>4</sub>	5 <sub>5</sub>	5 <sub>6</sub>	5 <sub>7</sub>	6 <sub>0</sub>	6 <sub>1</sub>	6 <sub>2</sub>	6 <sub>3</sub>	6 <sub>4</sub>	6 <sub>5</sub>	6 <sub>6</sub>	6 <sub>7</sub>	7 <sub>0</sub>	7 <sub>1</sub>	7 <sub>2</sub>	7 <sub>3</sub>	7 <sub>4</sub>	7 <sub>5</sub>	7 <sub>6</sub>	7 <sub>7</sub>
8 <sub>0</sub>	8 <sub>1</sub>	8 <sub>2</sub>	8 <sub>3</sub>	8 <sub>4</sub>	8 <sub>5</sub>	8 <sub>6</sub>	8 <sub>7</sub>	9 <sub>0</sub>	9 <sub>1</sub>	9 <sub>2</sub>	9 <sub>3</sub>	9 <sub>4</sub>	9 <sub>5</sub>	9 <sub>6</sub>	9 <sub>7</sub>	10 <sub>0</sub>	10 <sub>1</sub>	10 <sub>2</sub>	10 <sub>3</sub>	10 <sub>4</sub>	10 <sub>5</sub>	10 <sub>6</sub>	10 <sub>7</sub>	11 <sub>0</sub>	11 <sub>1</sub>	11 <sub>2</sub>	11 <sub>3</sub>	11 <sub>4</sub>	11 <sub>5</sub>	11 <sub>6</sub>	11 <sub>7</sub>
12 <sub>0</sub>	12 <sub>1</sub>	12 <sub>2</sub>	12 <sub>3</sub>	12 <sub>4</sub>	12 <sub>5</sub>	12 <sub>6</sub>	12 <sub>7</sub>	13 <sub>0</sub>	13 <sub>1</sub>	13 <sub>2</sub>	13 <sub>3</sub>	13 <sub>4</sub>	13 <sub>5</sub>	13 <sub>6</sub>	13 <sub>7</sub>	14 <sub>0</sub>	14 <sub>1</sub>	14 <sub>2</sub>	14 <sub>3</sub>	14 <sub>4</sub>	14 <sub>5</sub>	14 <sub>6</sub>	14 <sub>7</sub>	15 <sub>0</sub>	15 <sub>1</sub>	15 <sub>2</sub>	15 <sub>3</sub>	15 <sub>4</sub>	15 <sub>5</sub>	15 <sub>6</sub>	15 <sub>7</sub>

Figure 37: Illustration of the bit/pixel placement on a logical bitmap. The subscript digits indicate the bit weight within the word; words are identified by their logic address (indicated by the normal-case numbers). The words are laid out contiguously, by increasing address, left to right, line by line.

- **Chronological bitmaps**, where the words are placed according to the order in which they were accessed during the test. For all static tests, and for dynamic tests carried out with natural addressing, the chronological bitmap is equivalent to the logical bitmap. For dynamic tests carried out with non-natural addressing schemes, however, the chronological bitmap can be substantially different. Table 1 illustrates the order in which words would be accessed using four different addressing schemes.

Natural	Gray	Anti-Gray	LFSR
0000 (0)	0000 (0)	0000 (0)	0000 (0)
0001 (1)	0001 (1)	1110 (14)	0001 (1)
0010 (2)	0011 (3)	0011 (3)	0011 (3)
0011 (3)	0010 (2)	1101 (13)	0111 (7)
0100 (4)	0110 (6)	0110 (6)	1110 (14)
0101 (5)	0111 (7)	1000 (8)	1101 (13)
0110 (6)	0101 (5)	0101 (5)	1011 (11)
0111 (7)	0100 (4)	1011 (11)	0110 (6)
1000 (8)	1100 (12)	1100 (12)	1100 (12)
1001 (9)	1101 (13)	0010 (2)	1001 (9)
1010 (10)	1111 (15)	1111 (15)	0010 (2)
1011 (11)	1110 (14)	0001 (1)	0101 (5)
1100 (12)	1010 (10)	1010 (10)	1010 (19)
1101 (13)	1011 (11)	0100 (4)	0100 (4)
1110 (14)	1001 (9)	1001 (9)	1000 (8)
1111 (15)	1000 (8)	0111 (7)	0000 (0)

Table 1: Order of visit of a 16-word address space using four different addressing schemes. Note that the XOR-based LFSR addressing used to generate the LFSR sequence cannot visit an address with all bits at '1', which would otherwise result in a deadlock.

Chronological bitmaps generated from dynamic tests using the non-natural addressing schemes would be mapped as follows:

0 <sub>7</sub>	0 <sub>6</sub>	0 <sub>5</sub>	0 <sub>4</sub>	0 <sub>3</sub>	0 <sub>2</sub>	0 <sub>1</sub>	0 <sub>0</sub>	1 <sub>7</sub>	1 <sub>6</sub>	1 <sub>5</sub>	1 <sub>4</sub>	1 <sub>3</sub>	1 <sub>2</sub>	1 <sub>1</sub>	1 <sub>0</sub>	3 <sub>7</sub>	3 <sub>6</sub>	3 <sub>5</sub>	3 <sub>4</sub>	3 <sub>3</sub>	3 <sub>2</sub>	3 <sub>1</sub>	3 <sub>0</sub>	2 <sub>7</sub>	2 <sub>6</sub>	2 <sub>5</sub>	2 <sub>4</sub>	2 <sub>3</sub>	2 <sub>2</sub>	2 <sub>1</sub>	2 <sub>0</sub>
6 <sub>7</sub>	6 <sub>6</sub>	6 <sub>5</sub>	6 <sub>4</sub>	6 <sub>3</sub>	6 <sub>2</sub>	6 <sub>1</sub>	6 <sub>0</sub>	7 <sub>7</sub>	7 <sub>6</sub>	7 <sub>5</sub>	7 <sub>4</sub>	7 <sub>3</sub>	7 <sub>2</sub>	7 <sub>1</sub>	7 <sub>0</sub>	5 <sub>7</sub>	5 <sub>6</sub>	5 <sub>5</sub>	5 <sub>4</sub>	5 <sub>3</sub>	5 <sub>2</sub>	5 <sub>1</sub>	5 <sub>0</sub>	4 <sub>7</sub>	4 <sub>6</sub>	4 <sub>5</sub>	4 <sub>4</sub>	4 <sub>3</sub>	4 <sub>2</sub>	4 <sub>1</sub>	4 <sub>0</sub>
12 <sub>7</sub>	12 <sub>6</sub>	12 <sub>5</sub>	12 <sub>4</sub>	12 <sub>3</sub>	12 <sub>2</sub>	12 <sub>1</sub>	12 <sub>0</sub>	13 <sub>7</sub>	13 <sub>6</sub>	13 <sub>5</sub>	13 <sub>4</sub>	13 <sub>3</sub>	13 <sub>2</sub>	13 <sub>1</sub>	13 <sub>0</sub>	15 <sub>7</sub>	15 <sub>6</sub>	15 <sub>5</sub>	15 <sub>4</sub>	15 <sub>3</sub>	15 <sub>2</sub>	15 <sub>1</sub>	15 <sub>0</sub>	14 <sub>7</sub>	14 <sub>6</sub>	14 <sub>5</sub>	14 <sub>4</sub>	14 <sub>3</sub>	14 <sub>2</sub>	14 <sub>1</sub>	14 <sub>0</sub>
10 <sub>7</sub>	10 <sub>6</sub>	10 <sub>5</sub>	10 <sub>4</sub>	10 <sub>3</sub>	10 <sub>2</sub>	10 <sub>1</sub>	10 <sub>0</sub>	11 <sub>7</sub>	11 <sub>6</sub>	11 <sub>5</sub>	11 <sub>4</sub>	11 <sub>3</sub>	11 <sub>2</sub>	11 <sub>1</sub>	11 <sub>0</sub>	9 <sub>7</sub>	9 <sub>6</sub>	9 <sub>5</sub>	9 <sub>4</sub>	9 <sub>3</sub>	9 <sub>2</sub>	9 <sub>1</sub>	9 <sub>0</sub>	8 <sub>7</sub>	8 <sub>6</sub>	8 <sub>5</sub>	8 <sub>4</sub>	8 <sub>3</sub>	8 <sub>2</sub>	8 <sub>1</sub>	8 <sub>0</sub>

Figure 38: Chronological Gray bitmap.

0 <sub>7</sub>	0 <sub>6</sub>	0 <sub>5</sub>	0 <sub>4</sub>	0 <sub>3</sub>	0 <sub>2</sub>	0 <sub>1</sub>	0 <sub>0</sub>	14 <sub>7</sub>	14 <sub>6</sub>	14 <sub>5</sub>	14 <sub>4</sub>	14 <sub>3</sub>	14 <sub>2</sub>	14 <sub>1</sub>	14 <sub>0</sub>	3 <sub>7</sub>	3 <sub>6</sub>	3 <sub>5</sub>	3 <sub>4</sub>	3 <sub>3</sub>	3 <sub>2</sub>	3 <sub>1</sub>	3 <sub>0</sub>	13 <sub>7</sub>	13 <sub>6</sub>	13 <sub>5</sub>	13 <sub>4</sub>	13 <sub>3</sub>	13 <sub>2</sub>	13 <sub>1</sub>	13 <sub>0</sub>
6 <sub>7</sub>	6 <sub>6</sub>	6 <sub>5</sub>	6 <sub>4</sub>	6 <sub>3</sub>	6 <sub>2</sub>	6 <sub>1</sub>	6 <sub>0</sub>	8 <sub>7</sub>	8 <sub>6</sub>	8 <sub>5</sub>	8 <sub>4</sub>	8 <sub>3</sub>	8 <sub>2</sub>	8 <sub>1</sub>	8 <sub>0</sub>	5 <sub>7</sub>	5 <sub>6</sub>	5 <sub>5</sub>	5 <sub>4</sub>	5 <sub>3</sub>	5 <sub>2</sub>	5 <sub>1</sub>	5 <sub>0</sub>	11 <sub>7</sub>	11 <sub>6</sub>	11 <sub>5</sub>	11 <sub>4</sub>	11 <sub>3</sub>	11 <sub>2</sub>	11 <sub>1</sub>	11 <sub>0</sub>
12 <sub>7</sub>	12 <sub>6</sub>	12 <sub>5</sub>	12 <sub>4</sub>	12 <sub>3</sub>	12 <sub>2</sub>	12 <sub>1</sub>	12 <sub>0</sub>	2 <sub>7</sub>	2 <sub>6</sub>	2 <sub>5</sub>	2 <sub>4</sub>	2 <sub>3</sub>	2 <sub>2</sub>	2 <sub>1</sub>	2 <sub>0</sub>	15 <sub>7</sub>	15 <sub>6</sub>	15 <sub>5</sub>	15 <sub>4</sub>	15 <sub>3</sub>	15 <sub>2</sub>	15 <sub>1</sub>	15 <sub>0</sub>	1 <sub>7</sub>	1 <sub>6</sub>	1 <sub>5</sub>	1 <sub>4</sub>	1 <sub>3</sub>	1 <sub>2</sub>	1 <sub>1</sub>	1 <sub>0</sub>
10 <sub>7</sub>	10 <sub>6</sub>	10 <sub>5</sub>	10 <sub>4</sub>	10 <sub>3</sub>	10 <sub>2</sub>	10 <sub>1</sub>	10 <sub>0</sub>	4 <sub>7</sub>	4 <sub>6</sub>	4 <sub>5</sub>	4 <sub>4</sub>	4 <sub>3</sub>	4 <sub>2</sub>	4 <sub>1</sub>	4 <sub>0</sub>	9 <sub>7</sub>	9 <sub>6</sub>	9 <sub>5</sub>	9 <sub>4</sub>	9 <sub>3</sub>	9 <sub>2</sub>	9 <sub>1</sub>	9 <sub>0</sub>	7 <sub>7</sub>	7 <sub>6</sub>	7 <sub>5</sub>	7 <sub>4</sub>	7 <sub>3</sub>	7 <sub>2</sub>	7 <sub>1</sub>	7 <sub>0</sub>

Figure 39: Chronological anti-Gray bitmap.

0 <sub>7</sub>	0 <sub>6</sub>	0 <sub>5</sub>	0 <sub>4</sub>	0 <sub>3</sub>	0 <sub>2</sub>	0 <sub>1</sub>	0 <sub>0</sub>	1 <sub>7</sub>	1 <sub>6</sub>	1 <sub>5</sub>	1 <sub>4</sub>	1 <sub>3</sub>	1 <sub>2</sub>	1 <sub>1</sub>	1 <sub>0</sub>	3 <sub>7</sub>	3 <sub>6</sub>	3 <sub>5</sub>	3 <sub>4</sub>	3 <sub>3</sub>	3 <sub>2</sub>	3 <sub>1</sub>	3 <sub>0</sub>	7 <sub>7</sub>	7 <sub>6</sub>	7 <sub>5</sub>	7 <sub>4</sub>	7 <sub>3</sub>	7 <sub>2</sub>	7 <sub>1</sub>	7 <sub>0</sub>
14 <sub>7</sub>	14 <sub>6</sub>	14 <sub>5</sub>	14 <sub>4</sub>	14 <sub>3</sub>	14 <sub>2</sub>	14 <sub>1</sub>	14 <sub>0</sub>	13 <sub>7</sub>	13 <sub>6</sub>	13 <sub>5</sub>	13 <sub>4</sub>	13 <sub>3</sub>	13 <sub>2</sub>	13 <sub>1</sub>	13 <sub>0</sub>	11 <sub>7</sub>	11 <sub>6</sub>	11 <sub>5</sub>	11 <sub>4</sub>	11 <sub>3</sub>	11 <sub>2</sub>	11 <sub>1</sub>	11 <sub>0</sub>	6 <sub>7</sub>	6 <sub>6</sub>	6 <sub>5</sub>	6 <sub>4</sub>	6 <sub>3</sub>	6 <sub>2</sub>	6 <sub>1</sub>	6 <sub>0</sub>
12 <sub>7</sub>	12 <sub>6</sub>	12 <sub>5</sub>	12 <sub>4</sub>	12 <sub>3</sub>	12 <sub>2</sub>	12 <sub>1</sub>	12 <sub>0</sub>	9 <sub>7</sub>	9 <sub>6</sub>	9 <sub>5</sub>	9 <sub>4</sub>	9 <sub>3</sub>	9 <sub>2</sub>	9 <sub>1</sub>	9 <sub>0</sub>	2 <sub>7</sub>	2 <sub>6</sub>	2 <sub>5</sub>	2 <sub>4</sub>	2 <sub>3</sub>	2 <sub>2</sub>	2 <sub>1</sub>	2 <sub>0</sub>	5 <sub>7</sub>	5 <sub>6</sub>	5 <sub>5</sub>	5 <sub>4</sub>	5 <sub>3</sub>	5 <sub>2</sub>	5 <sub>1</sub>	5 <sub>0</sub>
10 <sub>7</sub>	10 <sub>6</sub>	10 <sub>5</sub>	10 <sub>4</sub>	10 <sub>3</sub>	10 <sub>2</sub>	10 <sub>1</sub>	10 <sub>0</sub>	4 <sub>7</sub>	4 <sub>6</sub>	4 <sub>5</sub>	4 <sub>4</sub>	4 <sub>3</sub>	4 <sub>2</sub>	4 <sub>1</sub>	4 <sub>0</sub>	8 <sub>7</sub>	8 <sub>6</sub>	8 <sub>5</sub>	8 <sub>4</sub>	8 <sub>3</sub>	8 <sub>2</sub>	8 <sub>1</sub>	8 <sub>0</sub>	X	X	X	X	X	X	X	X

Figure 40: Chronological LFSR bitmap. Since the address “1111” cannot be visited, one word will be coloured by default.

- **Physical bitmaps**, where every pixel is positioned according to its corresponding bit’s actual physical storage position of in the memory array. Producing such a bitmap requires precise information on the organization of the memory array – its address scrambling and bit interleaving schemes. On a physical bitmap, data could be positioned according to the following, arbitrary pattern:

0 <sub>7</sub>	8 <sub>7</sub>	4 <sub>7</sub>	12 <sub>7</sub>	0 <sub>6</sub>	8 <sub>6</sub>	4 <sub>6</sub>	12 <sub>6</sub>	0 <sub>5</sub>	8 <sub>5</sub>	4 <sub>5</sub>	12 <sub>5</sub>	0 <sub>4</sub>	8 <sub>4</sub>	4 <sub>4</sub>	12 <sub>4</sub>	0 <sub>3</sub>	8 <sub>3</sub>	4 <sub>3</sub>	12 <sub>3</sub>	0 <sub>2</sub>	8 <sub>2</sub>	4 <sub>2</sub>	12 <sub>2</sub>	0 <sub>1</sub>	8 <sub>1</sub>	4 <sub>1</sub>	12 <sub>1</sub>	0 <sub>0</sub>	8 <sub>0</sub>	4 <sub>0</sub>	12 <sub>0</sub>
2 <sub>7</sub>	10 <sub>7</sub>	6 <sub>7</sub>	14 <sub>7</sub>	2 <sub>6</sub>	10 <sub>6</sub>	6 <sub>6</sub>	14 <sub>6</sub>	2 <sub>5</sub>	10 <sub>5</sub>	6 <sub>5</sub>	14 <sub>5</sub>	2 <sub>4</sub>	10 <sub>4</sub>	6 <sub>4</sub>	14 <sub>4</sub>	2 <sub>3</sub>	10 <sub>3</sub>	6 <sub>3</sub>	14 <sub>3</sub>	2 <sub>2</sub>	10 <sub>2</sub>	6 <sub>2</sub>	14 <sub>2</sub>	2 <sub>1</sub>	10 <sub>1</sub>	6 <sub>1</sub>	14 <sub>1</sub>	2 <sub>0</sub>	10 <sub>0</sub>	6 <sub>0</sub>	14 <sub>0</sub>
1 <sub>7</sub>	9 <sub>7</sub>	5 <sub>7</sub>	13 <sub>7</sub>	1 <sub>6</sub>	9 <sub>6</sub>	5 <sub>6</sub>	13 <sub>6</sub>	1 <sub>5</sub>	9 <sub>5</sub>	5 <sub>5</sub>	13 <sub>5</sub>	1 <sub>4</sub>	9 <sub>4</sub>	5 <sub>4</sub>	13 <sub>4</sub>	1 <sub>3</sub>	9 <sub>3</sub>	5 <sub>3</sub>	13 <sub>3</sub>	1 <sub>2</sub>	9 <sub>2</sub>	5 <sub>2</sub>	13 <sub>2</sub>	1 <sub>1</sub>	9 <sub>1</sub>	5 <sub>1</sub>	13 <sub>1</sub>	1 <sub>0</sub>	9 <sub>0</sub>	5 <sub>0</sub>	13 <sub>0</sub>
3 <sub>7</sub>	11 <sub>7</sub>	7 <sub>7</sub>	15 <sub>7</sub>	3 <sub>6</sub>	11 <sub>6</sub>	7 <sub>6</sub>	15 <sub>6</sub>	3 <sub>5</sub>	11 <sub>5</sub>	7 <sub>5</sub>	15 <sub>5</sub>	3 <sub>4</sub>	11 <sub>4</sub>	7 <sub>4</sub>	15 <sub>4</sub>	3 <sub>3</sub>	11 <sub>3</sub>	7 <sub>3</sub>	15 <sub>3</sub>	3 <sub>2</sub>	11 <sub>2</sub>	7 <sub>2</sub>	15 <sub>2</sub>	3 <sub>1</sub>	11 <sub>1</sub>	7 <sub>1</sub>	15 <sub>1</sub>	3 <sub>0</sub>	11 <sub>0</sub>	7 <sub>0</sub>	15 <sub>0</sub>

Figure 41: Physical bitmap generated using 4-bit interleaving and an arbitrary address scrambling scheme.

All bitmaps only display one entry per word (n pixels per n-bit word). This means that on bitmaps from dynamic test data, each pixel contains the information from all the successive read operations performed on the corresponding cell. If a pixel is coloured, it means that it suffered at least one upset during the test, but it is not possible to tell how many upsets occurred from the bitmap.

## 2) Scilab processing software

A series of Scilab scripts were written to perform more complex operations on the test data. These scripts were used to generate certain types of bitmaps, histograms, and test summaries which were deemed too difficult to generate with C/C++. The Scilab scripts were particularly useful to study the statistical distribution of errors over the memory array.

## Chapter VII – Test results and discoveries

This chapter presents some of the most interesting test results, and the discoveries which were made over the course of this study. Most of these points have been discussed in *IEEE Transactions on Nuclear Science* (Refs. [98]–[101]).

The test data is presented in the form of bitmaps. Every bitmap is accompanied by a small table summarizing the test conditions: test facility, beam species, energy, LET in silicon at the DUT surface, flux and deposited fluence, beam tilt angle relative to the normal to the DUT surface, test type and pattern (also addressing scheme and algorithm for dynamic tests).

### A. Clustering of bit errors in a 90 nm SRAM

The failure modes of the SRAM90 (see Chapter 6) are heavily influenced by the state of the device (static or dynamic mode). Figure 42 presents a bitmap generated from heavy-ion (krypton) dynamic test data, which exhibits several radically different error patterns. These patterns (recorded on the same device model) have been classified into four categories by Tsiligiannis *et al.* in [98]:

- **Type A**, which include isolated Single-Bit Upsets (SBUs) and small, coherent clusters of errors (Multiple-Cell Upsets, MCUs) numbering up to a few tens of upsets. These upsets are caused by direct ionization by a particle strike;
- **Type B**, which include up to several hundred upsets forming an elongated pattern on the bitmap. Similar error patterns have been reported in the literature to be caused by micro-latchups [102], and Tsiligiannis *et al.* point out that these patterns are topologically confined to areas enclosed by well taps;
- **Type C**, which can include tens of thousands of upset cells. On a physical bitmap, their appearance is directly influenced by the addressing scheme which was used during the test. As can be seen on Figure 42, these patterns are highly convoluted when using natural addressing (series of vertical stripes). However, type C errors appear as contiguous bands on a chronological bitmap (Figure 43); this is an indication that these errors correspond to words which were accessed sequentially. This is characteristic of a group of errors caused by a Single-Event Functional Interrupt (SEFI);
- **Type D**, which include several tens of thousands of upsets in large, densely corrupted bands 64 bits wide, and up to 4096 bits high, generally located on the sides of the die. Often, these patterns are made of a series of blocks of 64x64 errors. These patterns have been suggested in [98] to be the result of a combination of delays in the word line signals and micro-latchups occurring in the array's power switches.

An algorithm was developed to aggregate the errors caused by SEE into clusters, which was presented in [99]. The goal of this clustering process is to extract as much information as possible from test data. As mentioned in Chapter 5, radiation test campaigns on memory devices typically aim at determining, among other things, the **SEU cross-section per bit**,  $\sigma_{SEU_{bit}}$ . This metric is useful to compare a device's radiation sensitivity to that of another device, by allowing a system designer to estimate how many errors will be generated in a given quantity of memory, after exposure to a given radiation fluence at a given energy or

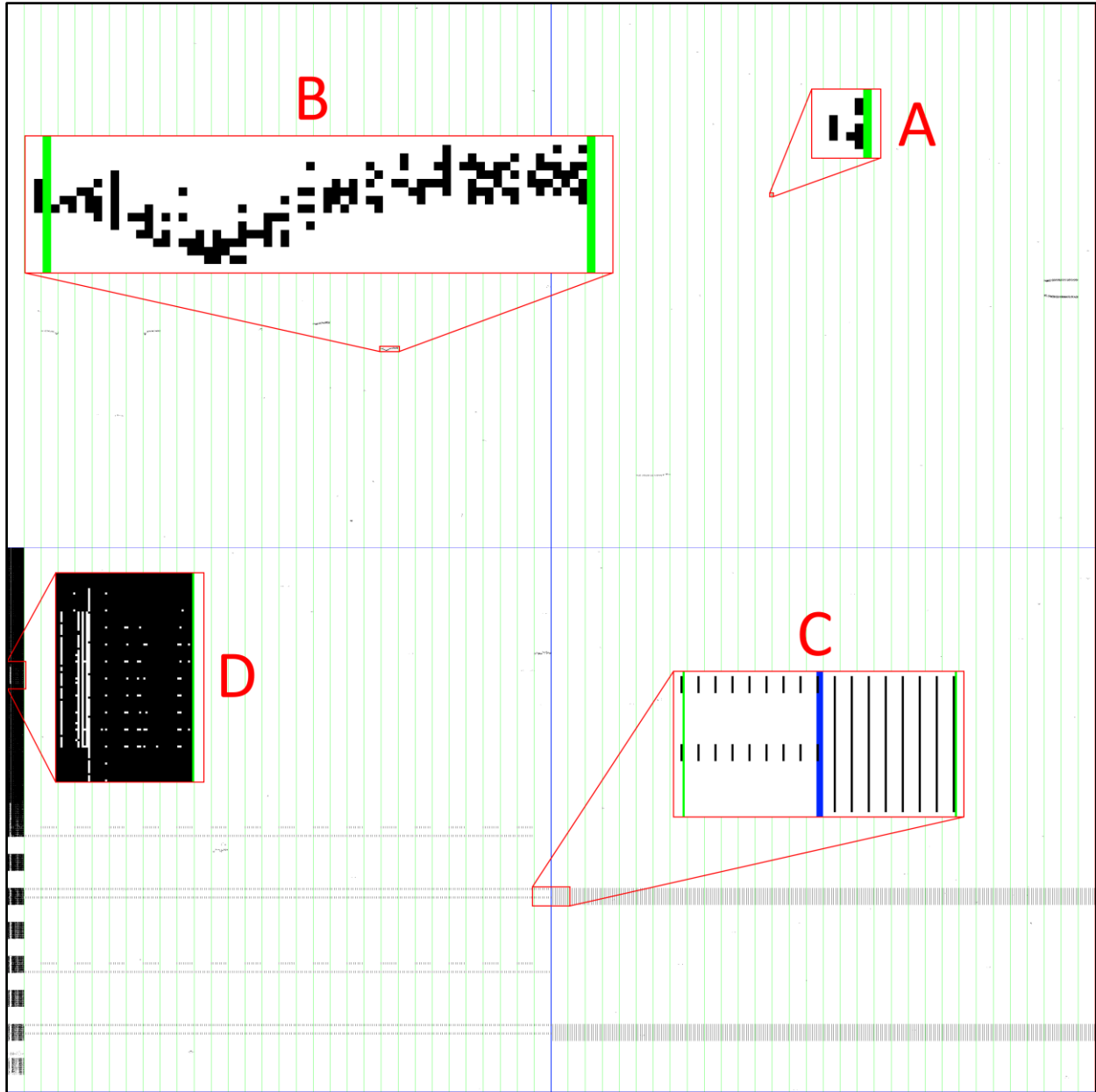


Figure 42: Physical bitmap generated with data from a heavy-ion dynamic test. The zoom-ins exhibit examples of error pattern types A and B, and close-ups on arbitrary regions of pattern types C and D. Blue and green lines are just a visual aid to separate logic blocks.

Facility	Device/lot	Ion	Energy (MeV)	LET@surface (MeV.cm <sup>2</sup> .mg <sup>-1</sup> )	Tilt angle (degrees)	Flux (counts.s <sup>-1</sup> .cm <sup>-2</sup> )	Fluence (counts.cm <sup>-2</sup> )	Test type	Addressing
RADEF	SRAM90/A	Kr	768	32.1	0	100	700	March C-	Natural

LET. However, the metric is only relevant when the error generation process is relatively consistent and repeatable – that is, when particles of similar energy or LET generate similar amounts of cell upsets. In the case of devices such as the SRAM90, when one type of ions (e.g. krypton ions, which were used to generate Figure 42 and Figure 43) at the same energy can generate anywhere between a couple errors in a type A MCU, to several hundred thousand errors in a type D failure, the metric loses its relevance. The SEU cross-section per bit cannot account for the great dispersion in the average number of errors

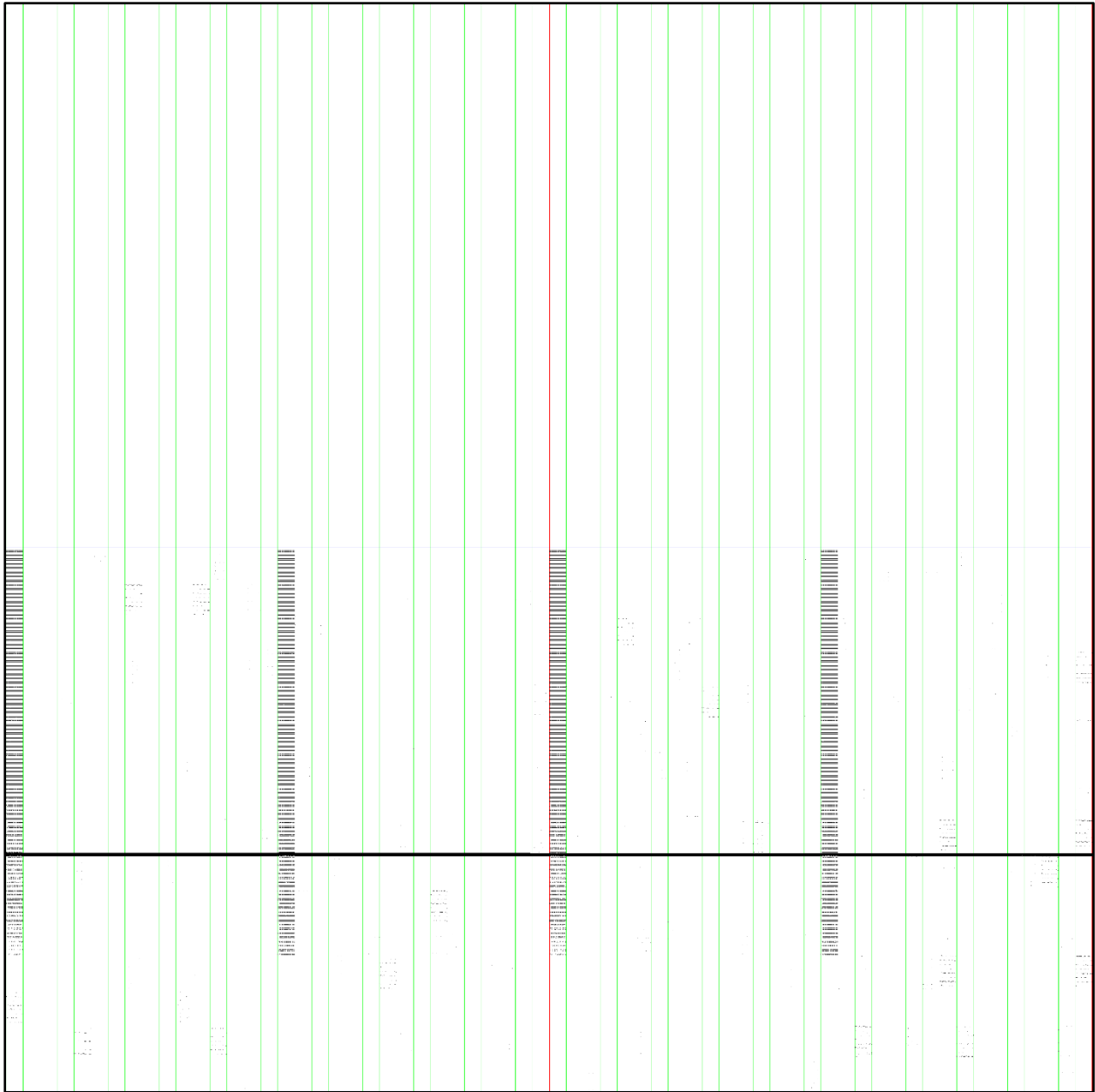


Figure 43: Chronological bitmap generated with the same data as Figure 42. With this layout, the type D pattern appears spread out in four distinct columns, and the type A and B patterns are similarly scattered. However, the complicated type C pattern appearing on the physical bitmap now appears as a coherent set of horizontal lines, denoting that it contains only words which were accessed consecutively, and were entirely corrupted. Blue and green lines are just a visual aid to separate logic blocks.

Facility	Device/lot	Ion	Energy (MeV)	LET@surface (MeV.cm <sup>2</sup> .mg <sup>-1</sup> )	Tilt angle (degrees)	Flux (counts.s <sup>-1</sup> .cm <sup>-2</sup> )	Fluence (counts.cm <sup>-2</sup> )	Test type	Addressing
RADEF	SRAM90/A	Kr	768	32.1	0	100	700	March C-	Natural

generated by an SEE. Additionally, the SEU cross-section per bit is not well suited to quantify events caused by particle strikes in the periphery (and thus not directly related to the size of the memory array). Another metric is needed assess the device's response to radiation: its **single-event cross-section**,  $\sigma_{event}$ , which

gives an estimate of the average number of SEE experienced during exposure to a given fluence at a given energy or LET.

The clustering algorithm operates by iterating on a list of bit errors, and grouping them according to temporal and physical proximity criteria (time of detection and physical distance on the array). The sequential errors caused by type C events are taken off the list first, to avoid interfering with the detection of other patterns. Then, clusters are formed by accretion of errors meeting the proximity criteria; once an error is added to an existing cluster, the cluster's physical and temporal dimensions are updated to include the new error, and the clustering process continues. In the end, the clusters are classified into types A, B and D based on their dimensions and population. Once the errors have been clustered, it becomes possible to calculate  $\sigma_{event}$ . Indeed, each cluster of errors is caused by a single event, so  $\sigma_{event}$  is simply the total ion fluence divided by the number of clusters.

Let us illustrate this clustering process with the data used to generate Figure 42 and Figure 43. In total, after a fluence of 700 ions.cm<sup>-2</sup> were deposited, 137272 bit errors were recorded, which indicates a very high SEU cross-section:

$$\sigma_{SEU} = \frac{\#SEU}{fluence} = \frac{137272}{700} = 196 \text{ cm}^2$$

This figure is aberrant, because the device's die area is only about 0.4 cm x 0.55 cm = 0.22 cm<sup>2</sup>; a deeper analysis is needed to interpret the test results. Using the method described in [99], with a physical proximity criterion of 10 horizontally and 67 vertically, and a temporal criterion of 2 seconds, the algorithm grouped these bit errors into 131 clusters: 117 of type A (including 15 SBUs), 11 of type B, one type C event and two type D clusters (on the physical bitmap, Figure 42, it is obvious that only one type D cluster is present; the second count is actually a false positive due to the aggregation of two large type B events in the upper right corner). Considering that these 131 separate clusters were caused by 131 different ion strikes, we get the following single-event cross-section:

$$\sigma_{event} = \frac{\#events}{fluence} = \frac{131}{700} = 0.18 \text{ cm}^2$$

This figure, which is very close to the die's total area, indicates that almost all the krypton ions striking the die triggered an SEE. Most importantly, it allows the prediction of the component's single-event rate in a given environment – a critical data when designing a system.

## B. Statistical analysis of the radiation response of a 65 nm SRAM

A large quantity of radiation data was acquired over four years by LIRMM and RADEF on the Cypress 65 nm SRAM (see Chapter 6); this large data pool served as a basis for a statistical analysis of the 65 nm SRAM's response to radiation. The underlying idea for this study, reported in [101], is that significant trends and patterns in the error distribution across the memory die can be revealing of the mechanisms at play during SEE.

Several devices originating from different lots were irradiated under different test modes (static and dynamic) with different beams: protons and heavy ions at RADEF (University of Jyväskylä), heavy ions at

Name	Facility	Test particle	Energy	Flux per run (cm <sup>-2</sup> )	Total fluence (cm <sup>-2</sup> )	DUT
TC0	Vesuvio	Neutrons	Atmospheric-like	1.6·10 <sup>7</sup> to 5.3·10 <sup>8</sup>	4.83·10 <sup>9</sup>	SRAM A
TC2 LEP	RADEF	Low-Energy Protons (LEP)	600 keV to 4.7 MeV	3.6·10 <sup>6</sup> to 3.6·10 <sup>7</sup>	7.18·10 <sup>8</sup>	SRAM B
TC2 HEP	RADEF	High-Energy Protons (HEP)	9.5 MeV to 50 MeV	3.6·10 <sup>8</sup> to 1.6·10 <sup>9</sup>	5.04·10 <sup>10</sup>	SRAM C
TC3	RADEF	Heavy ions (N, Fe, Kr, Xe)	9.3 MeV/u	8.4·10 <sup>2</sup> to 3.1·10 <sup>4</sup>	1.07·10 <sup>6</sup>	SRAM D
TC5	HIF	Heavy ions (C, N, Ne, Ar, Ni, Kr, Xe)	3.9 MeV, 9.3 MeV/u	1.0·10 <sup>3</sup> to 1.3·10 <sup>4</sup>	8.15·10 <sup>5</sup>	SRAM E
TC6	RADEF	High-Energy Protons (HEP)	10 MeV to 45 MeV	1.0·10 <sup>9</sup> to 1.2·10 <sup>9</sup>	8.16·10 <sup>10</sup>	SRAM F

Table 2: Summary of the test campaigns used as a data pool for this statistical study

HIF (Université Catholique de Louvain) and neutrons at Vesuvio (ISIS, Rutherford Appleton Laboratory). A summary of these test campaigns is presented in Table 2. A schematic of the organization of the memory die is present in Figure 44: the memory array is divided in four quadrants by two spines. Each quadrant is divided into four octants by a horizontal spine, which contains the sense amplifiers.

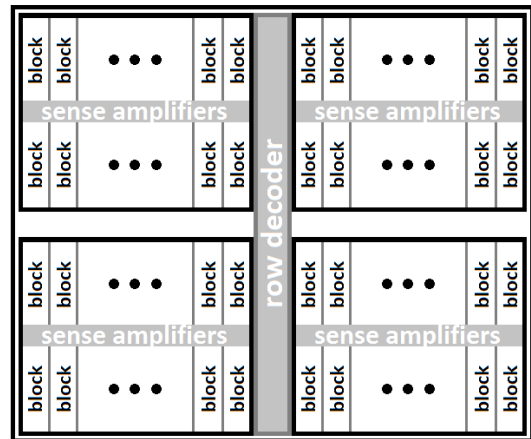


Figure 44: Schematic layout of the SRAM65's die.

Two different methods were used to study the error distributions. The first one involved creating a physical bitmap for every test run, and adding these bitmaps to create *composite bitmaps* depending on various criteria: test campaign/device, test type, particle... Visual inspection of these bitmaps allowed the detection of potential large-scale trends in the error distributions.

Indeed, one such tendency appeared on a composite bitmap from all the dynamic test runs carried out on SRAM E, which was irradiated with heavy ions. As can be seen on Figure 45, a single column of 1024 cells exhibits an unusually high concentration of errors: 47% of the column's cells have suffered at least one upset during this test campaign, whereas this figure drops to 0.57% when considering the whole array. However, no single dynamic bitmap (data from a single dynamic test run) exhibits this particular feature, nor does it appear on the combined bitmap from all static tests carried out on SRAM E. The device was tested before, during and after the test campaign, and never failed when not being irradiated. These elements indicate that this high concentration of errors on the composite bitmap is not the result of an SEE, but instead of a higher sensitivity of these cells under the combined effects of radiation exposure and dynamic stress. The extent and position of this anomaly (one cell wide, 1024 cells high, spanning exactly one quarter of the die's height) hint that this higher sensitivity stems from a latent defect in a control element – probably a bit line, or a bit line precharge circuit. No other SRAM exhibited this type of defect.

The second method consisted in a finer software analysis of the spatial distribution of the errors over the die. The TIGER C++ program and Scilab scripts were adapted to compare the bit error counts in different regions of the memory die. Several partition schemes were considered to divide the memory array, grouping the cells according to different criteria:

#### 1) Proximity of a memory cell to its sense amplifier

The array was partitioned into two groups of equal size, one containing the cells which were located the closest to the sense amplifiers, and those located the furthest away. The motivation for this partition scheme was to investigate whether potential systematic manufacturing defects in the bit lines could



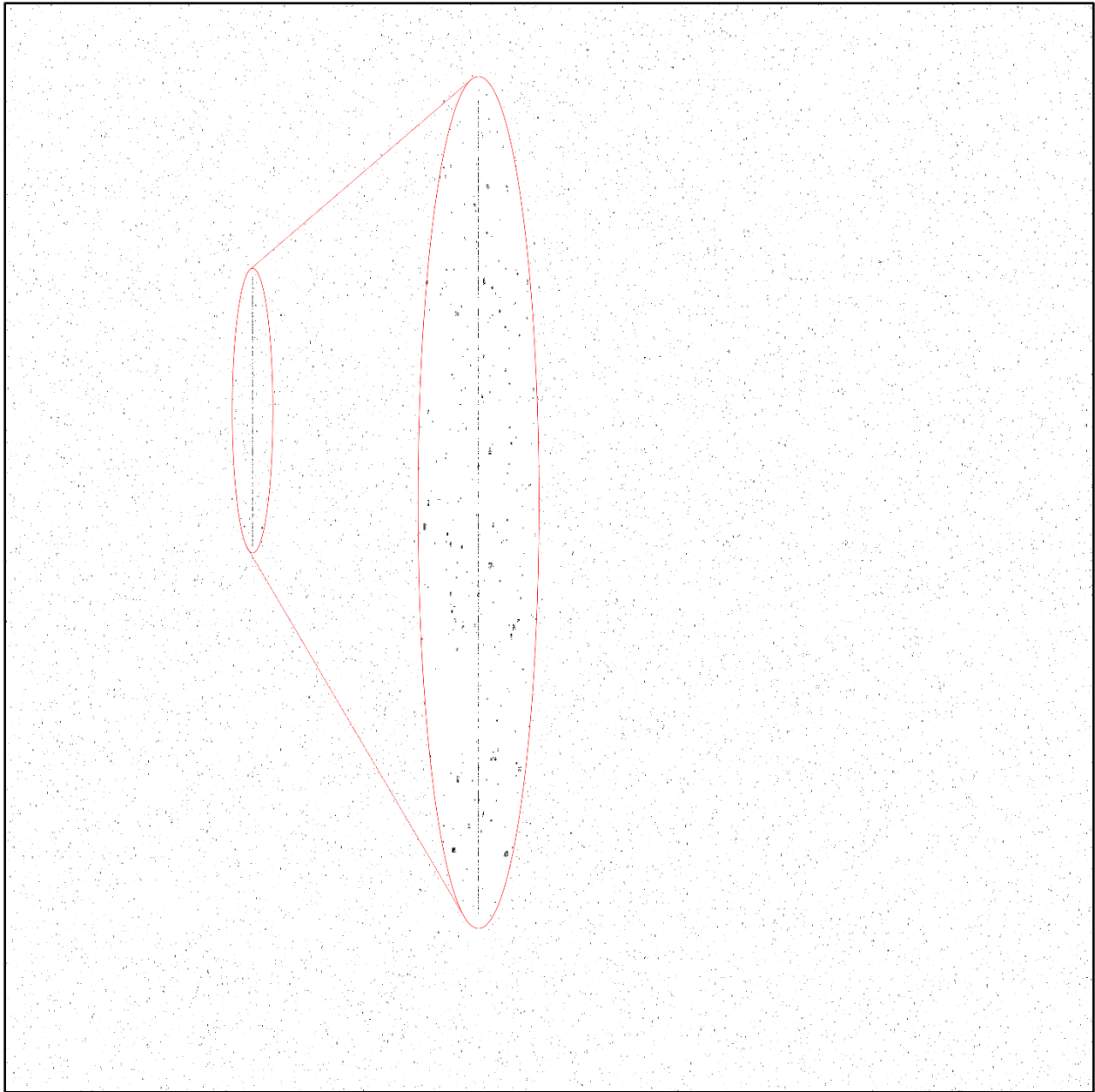


Figure 45: Composite bitmap of all dynamic tests carried out on device E (TC5, heavy-ions). The zoom-in focuses on a region of the die exhibiting abnormal error concentrations.

Facility	Device/lot	Ion	Energy (MeV)	Tilt angle (degrees)	LET@surface (MeV.cm <sup>2</sup> .mg <sup>-1</sup> )	Fluence (counts.cm <sup>-2</sup> )	Test type	Addressing
UCL	SRAM65/E	C	292	0	1.1	3.9·10 <sup>4</sup>	Various (dynamic): Dynamic stress, March C-, MATS+	Various: natural, fast row, fast column, LFSR, Gray, anti-Gray
		N	60	0 to 30	3.3 to 3.8	7.7·10 <sup>5</sup>		
		Ne	78, 235	0 to 30	3.0 to 7.4	3.0·10 <sup>5</sup>		
		Ar	151	0	15.9	5.9·10 <sup>4</sup>		
		Kr	305	0	40.4	1.4·10 <sup>4</sup>		
		Xe	420	0	67.7	1.9·10 <sup>4</sup>		

induce a correlation between a cell's distance to its sense amplifier and its sensitivity. No significant difference in SEU susceptibility was found between the cells of the two groups, regardless of the device, particle type, and electrical stimulus.

## 2) Transversal gradients in sensitivity

Two different partition schemes were used to investigate possible transversal variations in cell sensitivity, one dividing the array in sixteen horizontal columns, and the other in sixteen vertical columns, all being of equal dimensions and containing the same number of cells. Most results did not exhibit any special trend, as the recorded error count variations remained within the beam homogeneity uncertainty and statistical uncertainty, hence they are not reported here. However, a few combinations of device specimen and electrical stimulus yielded results exhibiting significant trends, of magnitudes much higher than the combined statistical uncertainty and beam homogeneity uncertainty. These results are displayed on Figures 46-50.

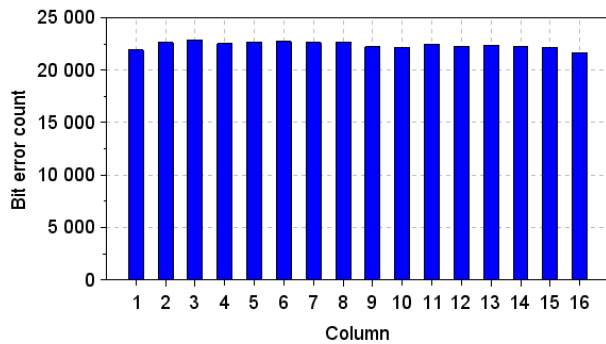


Figure 46: Error count per vertical band during SRAM B static LEP tests.

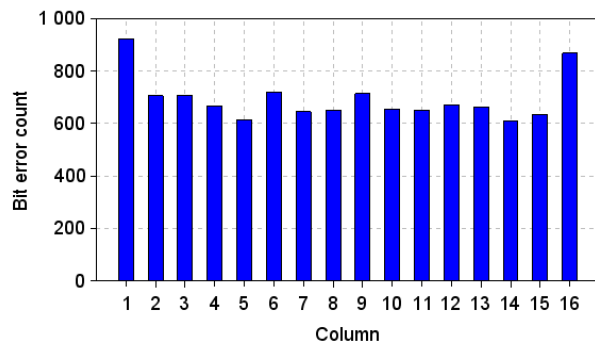


Figure 47: Error count per vertical band during SRAM B dynamic LEP tests.

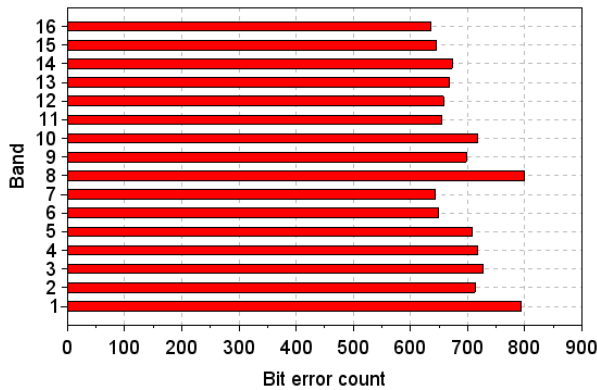


Figure 48: Error count per horizontal band during SRAM B dynamic LEP tests.

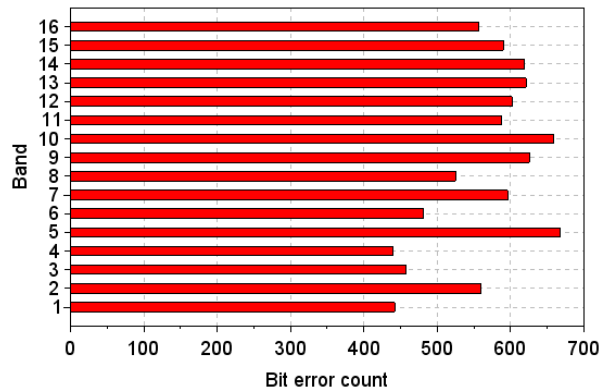


Figure 49: Error count per horizontal band during SRAM A dynamic neutron tests.

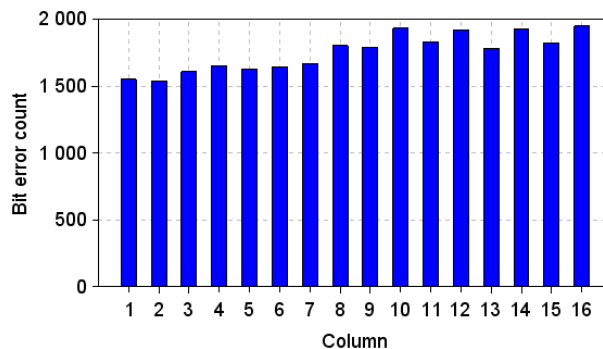


Figure 50: Error count per vertical band during SRAM C static HEP tests.

During dynamic testing of SRAM B under low-energy proton (LEP) irradiation (see Figure 47), a noticeably higher number of SEUs occurred in the bands located on the left and right edges than in the rest of the array (+40% and +33%, respectively). Importantly, these statistics are not the product of discrete, large-scale failure events affecting the edges of the die, but rather a result of a higher number of independent events in these regions. However, this trend did not appear during static tests carried out on the same device with the same beam (Figure 46).

This could be caused by voltage drops along the word lines, which run from the central vertical spine to the left and right edges of the array. The word line signal is used to drive the two NMOS access transistors of the SRAM cell, connecting each cell node to its bit line. If the word line signal is weak, the equivalent resistance between the cell node and its bitline will be higher, which will lower the read current of the cell [103]. The effect is illustrated in Figure 51 (borrowed from [103]), with data gathered from a test SRAM chip. This reduction in cell read current, which comes in conjunction with radiation-induced transients in dynamic mode, can make the cells located at the end of the word lines more prone to read errors. This conjunction of effects does not occur in static mode, which could explain the difference observed between Figure 46 and Figure 47.

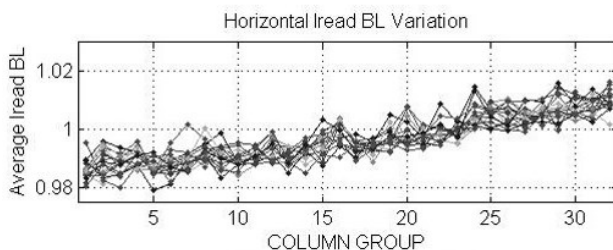


Figure 51: Effect of the cell position on the cell read current  $I_{read\_BL}$ , due to the voltage drop in the word lines. This data was acquired on a test SRAM chip. The abscissa axis indicates the distance of the cells to the word line drivers (located closest to the cells in group 32). Source: [103]

SRAM A, B and C top-to-bottom and left-to-right variations in sensitivity (Figure 48, 49 and 50) cannot be explained by the layout of the memory; the eight octants of the array share a common (mirrored) architecture, and should indicate the same trends if the variations in their sensitivity were caused by their design. This disparity is probably caused by fluctuations in the doping concentrations throughout the memory array during the manufacturing process of SRAM A, B and C, impacting in different ways the static and read noise margin characteristics of cells that are placed in different regions of the die, and ultimately leading to different SEU susceptibilities [104].

### 3) Effect of the proximity of tap cells

Tap cells (also called well taps) are connections between the memory substrate (or diffusion well) and a ground line (or supply line). They are used to lower the resistance between the substrate/well and the associated power grid, tying its potential to its reference point and effectively preventing the triggering of the parasitic thyristor responsible for latch-ups [105]. In the SRAM65, tap cells are disposed at regular intervals vertically and horizontally, forming rectangular "tap rings" enclosing a few thousand cells.

To investigate the effect of the proximity of tap cells on the SEU sensitivity of memory cells, the memory array was divided into four groups A, B, C and D of equal area and memory size. Fig. 10 represents the distribution of memory cells between groups A, B, C and D within one of the regions enclosed by tap cell

Figure 52: Distribution of the memory cells (squares) between groups A (blue), B (green), C (yellow) and D (red). Black squares represent tap cells. The length and width of the features in this figure are arbitrary and do not necessarily correspond to the actual dimensions of tap rings and cell group bands.



rows and columns (black squares). Each group was made of a collection of horizontal bands, each a few cells high and spanning the whole width of the memory array; group A contained only the memory cells which were the closest to the taps, whereas group D contained the memory cells which were the furthest away from them. Due to the simplicity of this partition scheme and to the layout of the taps, as illustrated by Figure 52, groups B, C and D contain a small percentage of cells which are as close to a tap as the cells in the A group, which are located next to the vertical boundaries of the tap ring. However, since the tap rings are much wider than they are high, these cells are so few that they have a negligible impact on the following statistics.

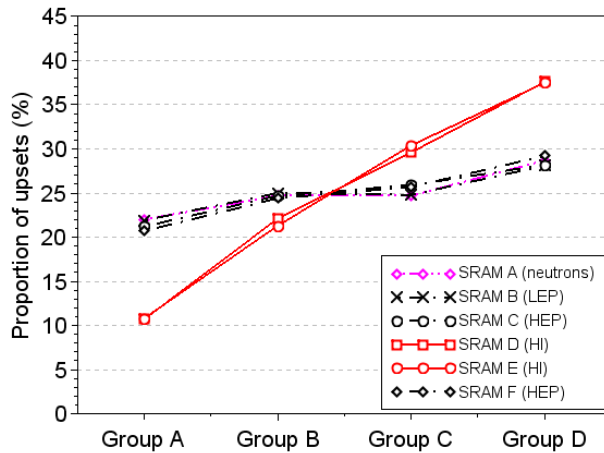


Figure 53: Effect of the proximity of the tap cells on the relative SEU sensitivity of memory cells (static test data). Heavy-ion data is shown in red, proton data in black, and neutron data in magenta.

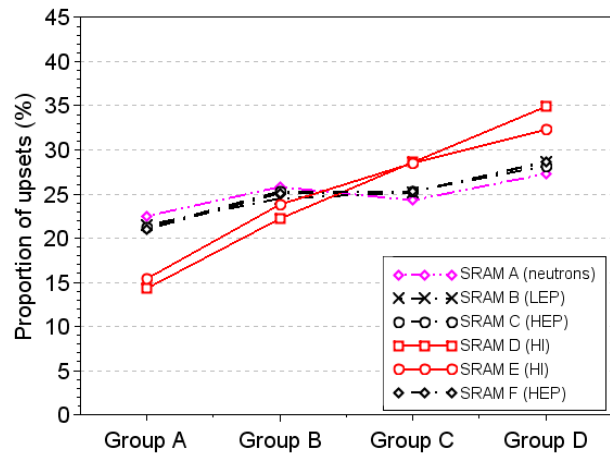


Figure 54: Effect of the proximity of the tap cells on the relative SEU sensitivity of memory cells (dynamic test data). Heavy-ion data is shown in red, proton data in black, and neutron data in magenta.

This partition scheme revealed that the distance of a memory cell to its closest tap cell had a clear impact on its radiation sensitivity; the proportion of upsets occurring in each cell group is visible on Figure 53 for static tests, and on Figure 54 for dynamic tests. These figures reveal that the positive correlation between tap cell distance and memory cell sensitivity exists in the data from all test campaigns, but is significantly stronger in heavy-ion data than in proton and neutron test data.

Figure 55 investigates further the impact of the heavy-ion LET (or, in this case, species) on the correlation between tap cell distance and memory cell sensitivity. The correlation is found to be much stronger when the device is irradiated with high-LET ions: the difference in error count between groups A and D is only 38% when considering tests with nitrogen (LET 1.8 MeV.cm<sup>2</sup>.mg<sup>-1</sup>), but reaches 360% during tests with xenon (LET 60 MeV.cm<sup>2</sup>.mg<sup>-1</sup>). These results take into consideration both static and dynamic test data.

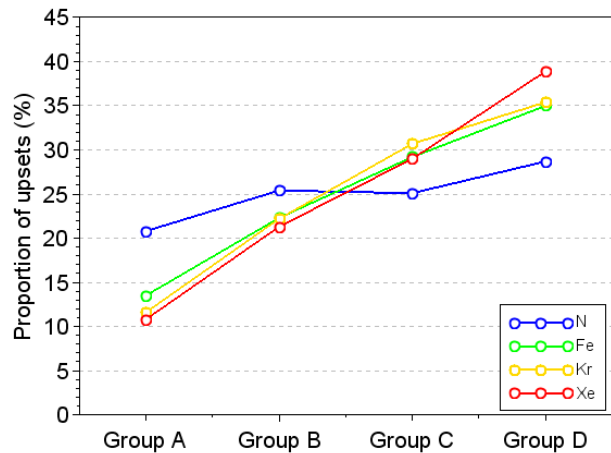


Figure 55: Effect of the heavy-ion species on the relative sensitivity of the memory cell groups (mixed static and dynamic test data).

ion's electric charge and velocity. Figure 56 gives the density of generated free charge carriers as a function of radial distance to the ion's path, for ions of varying atomic number and energy (figure borrowed from [36]). The figure shows that heavier ions generate a higher density of free carriers, and that higher-energy ions (ions with higher velocity) generate less dense, but more expansive charge clouds. This means that for a given free carrier density, the "clouds" of free carriers generated by protons and low-Z ions (such as the recoils created during neutron irradiation) is much smaller than the charge clouds generated by very heavy ions (such as xenon). These large charge clouds are then more likely to encompass tap cells, in which case the large concentration of free carriers around them facilitates the drift and collection of the generated charge at the tap. Conversely, small carrier clouds generated by protons and low-Z ions are less likely to encompass tap cells; their charge is more likely to be collected by cell transistors, and thus to trigger a cell upset.

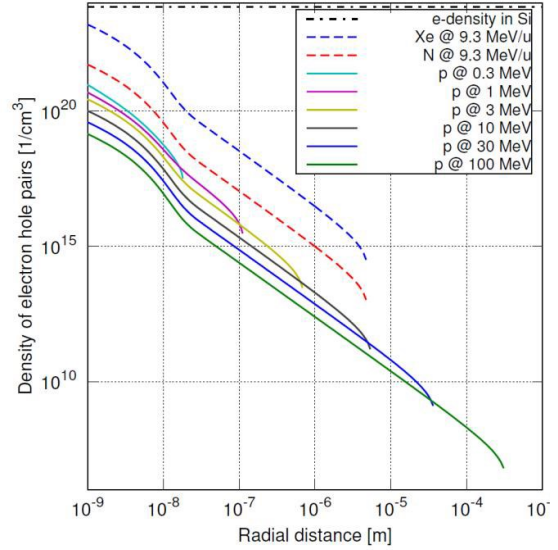


Figure 56: average density of generated charge carriers in silicon as a function of radial distance from particle trajectory for different incoming particle species and energies (figure borrowed from [36]). The dash-dotted line represents the density of all electrons in silicon.

#### 4) Block-to-block variability

The last partition scheme divided the array in regions matching its logic blocks. The variability in block sensitivity as a function of test type, particle type and memory specimen was investigated. Table 3 summarises the results, indicating for each combination of parameters, the ratio of maximum to minimum error and cluster counts among the array regions.

Particle	SRAM	Max/min error cluster count per block			Max/min error count per block			Standard error colour code
		Global	Static	Dynamic	Global	Static	Dynamic	
Neutrons	A	151%	152%	185%	148%	160%	191%	
LEP	B	111%	111%	201%	110%	111%	202%	
HEP	C	134%	141%	152%	134%	147%	147%	
HEP	D	118%	131%	125%	126%	142%	131%	
Heavy ions	E	153%	176%	155%	149%	222%	153%	
Heavy ions	F	194%	224%	202%	194%	297%	194%	

Table 3: Effect of the particle and test types on the disparity in error and cluster counts between memory blocks. The colour code indicates the statistical uncertainty, and is calculated from the number of events (clusters).

These results indicate that the disparity in sensitivity between memory blocks is maximized during heavy-ion irradiation. The testing mode (static or dynamic irradiation) has no apparent impact on this disparity, and little correlation appears between a specimen's sensitivity in static and dynamic test modes. This is evidence that by modifying the activity of various parts of the peripheral circuitry, and affecting the condition of the memory cells (e.g. supply voltage), static and dynamic testing can reveal different failure mechanisms in the memory's subsystems.

## 5) Summary

A methodology for the investigation of radiation effects on memories was introduced, which is based on error referencing, direct bitmap observation and database manipulation. When applied to the pool of data acquired on the SRAM65, this method brought out further information from the radiation test data than the typical SEE cross-section values, at no additional cost. Specifically, it highlighted specimen-to-specimen variability due to manufacturing variations or silent defects, and topological trends in the devices' SEU sensitivity due to their architectural features. The proposed methodology can be applied to other types of memories than SRAMs.

The results from this study accentuate the need to systematically perform memory testing on several specimens at once, to eliminate eventual device-specific biases in the test results. They also underline the benefits of carrying out dynamic tests along with static tests during memory irradiation campaigns, as the two test types bring out different failure mechanisms.

### C. Muon-induced Single-Event Upsets in a 65 nm SRAM

In recent years, a few studies have shown that data corruption in SRAMs may occur from ionisation by muons [106]; the abundance of these particles in the atmosphere raises the question of their impact on the reliability of future devices built with further integrated technology. As discussed in Chapter 2, muons have the same theoretical maximum electronic stopping power (or Linear Energy Transfer, LET) at the Bragg peak as protons [107], [108], which means that they can induce a comparable amount of charge per unit distance inside a memory component. The experimental static and dynamic SEU cross-sections of the SRAM65 under low-energy proton and muon irradiation are discussed in a previously unpublished study, the results of which were presented in [109].

#### 1) Experimental setup

Three devices from the same manufacturing lot were exposed to an antimuon ( $\mu^+$ ) beam from the RIKEN-RAL Port4 instrument at ISIS-RAL. The particle fluence for each test was chosen in accordance to the memories' sensitivity, depending on the type of test and muon energy, from  $2.5 \cdot 10^7$  up to  $3 \cdot 10^8 \text{ cm}^{-2}$ . The beam energies varied from 1.99 MeV to 3.15 MeV. The irradiation time varied from a few tens of minutes (when the memory was the most sensitive) to a few hours per run. A

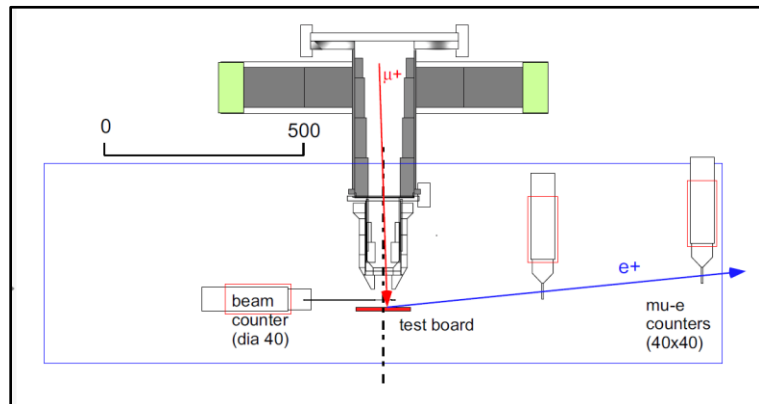


Figure 57: Schematic of the Port4 antimuon beam line setup at ISIS.

schematic of the beam line setup is available on Figure 57. The beam dosimetry was obtained with a scintillator positioned in front of the beam, while another pair of scintillators was used in line with the target area to count the positrons emitted by the decaying antimuons after they stopped in DUT. The uncertainty for the fluence in the beam dosimetry was given at  $\pm 25\%$ . The antimuon beam went through a  $50 \mu\text{m}$  mylar exit window,  $20 \mu\text{m}$  of aluminium foil, a  $300 \mu\text{m}$  polymer (polyvinyltoluene) scintillator, and about 10 cm of air before reaching the chip.

Facility (beam)	Beam energy (MeV)	Total fluence, static	Total static upsets	Total fluence, dynamic	Total dynamic upsets
ISIS (antimuons)	1.99	5,75E+07	0	-	-
	2.19	9,27E+07	1500	1,28E+08	52
	2.27	8,54E+07	1872	2,52E+07	24
	2.35	4,68E+08	13200	6,53E+08	713
	2.43	1,10E+08	2000	1,75E+08	123
	2.48	1,57E+08	1788	6,89E+07	34
	2.56	7,48E+07	162	2,76E+08	18
	2.65	5,46E+07	50	-	-
	3.15	1,52E+08	13	-	-
RADEF (protons)	0.6	3,63E+06	1461	2,89E+07	2886
	0.98	7,22E+07	356415	2,53E+08	7835
	2.2	3,61E+07	3993	1,44E+08	334
	4.7	3,61E+07	238	1,44E+08	59

Table 4: Summary of the results of the test campaigns used in this study.

The same SRAM device type was tested with low-energy protons at the RADEF facility (University of Jyväskylä). The beam energies ranged from 0.6 MeV to 4.7 MeV. The particle fluence per test run varied from  $3.6 \cdot 10^6$  to  $3.6 \cdot 10^7 \text{ cm}^{-2}$  and the typical test duration was in the order of few minutes. The uncertainty for the proton fluences in the beam dosimetry was given at  $\pm 10\%$ . These irradiations were carried out in vacuum.

Details about the combined deposited fluence and recorded upsets for each energy in the two test campaigns are given in Table 4. Dynamic tests were not carried out for each energy.

## 2) Experimental results

The response of the devices to antimuon and low-energy proton irradiations share similar characteristics. Their sensitivity was much higher during the static tests than during the dynamic tests. This difference is due to a power-saving measure, which consists in lowering the supply voltage of the memory array when the memory is idle, and thus making the SRAM cell more sensitive to SEUs. Each proton test induced from a few hundred to a few thousand upsets. This was also the case for the antimuon tests at which the initial antimuon energy translated to peak ionization at transistor depth. The three devices tested at ISIS

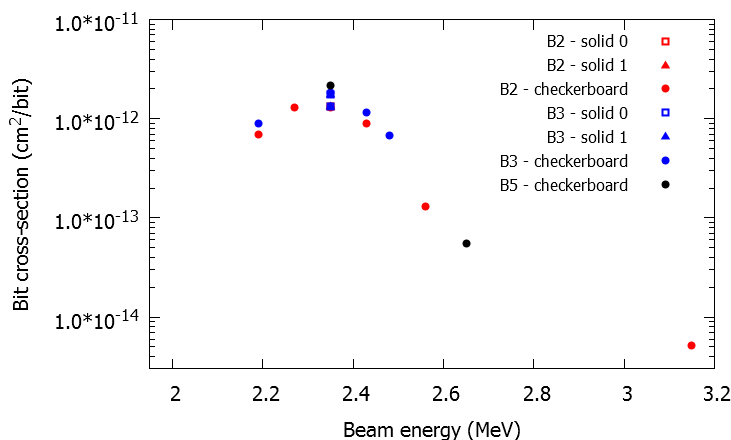


Figure 58: SEU cross-section per bit as a function of antimuon energy, for static tests. The colours differentiate the three test specimens, and the marker shapes differentiate the data pattern.

exhibited very closely matching cross-sections, which strongly depended on the initial antimuon beam energy (which we define as the energy of the particles before they pass the beam exit window). Figure 58 presents the devices' SEU cross-section data, obtained during static tests, as a function of antimuon energy and data pattern.

The graph in Figure 60 presents the devices' SEU cross-section during dynamic tests, as a function of antimuon energy and dynamic test type. The response of the device tested at RADEF with low-energy protons is given in Figure 59.

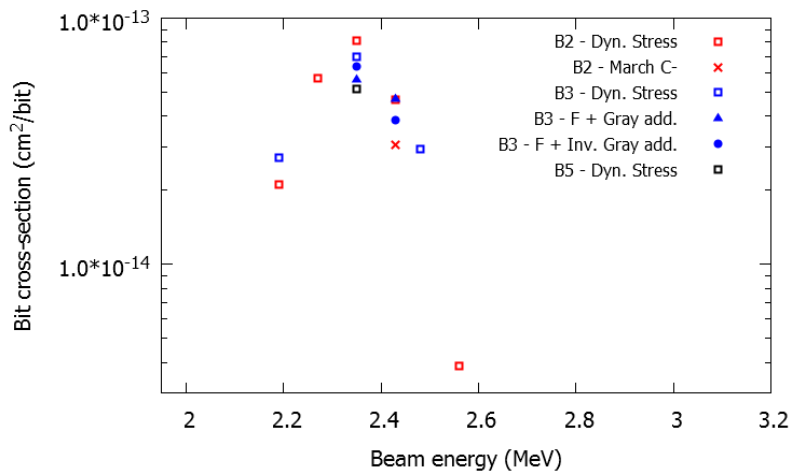


Figure 60: SEU cross-section per bit as a function of antimuon energy, for dynamic tests. The colours differentiate the three test specimens, and the marker shapes differentiate the type of dynamic test.

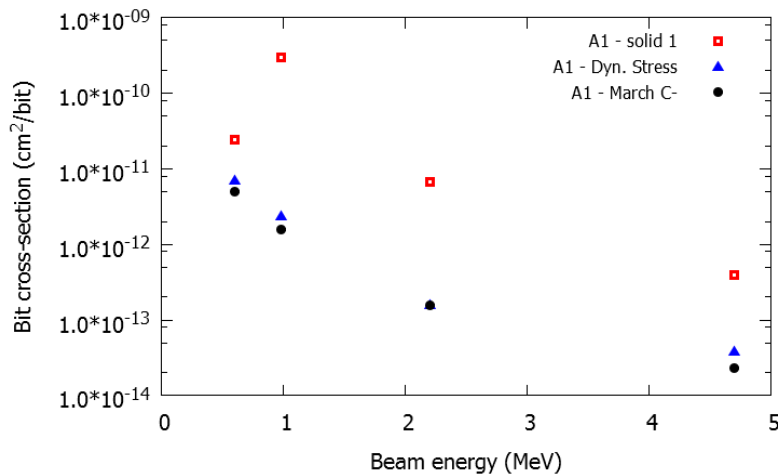


Figure 59: SEU cross-section per bit vs. proton energy. The square markers indicate static tests while the other markers dynamic tests.

For the sake of clarity, the error bars are not displayed in the previous plots, but the uncertainty on the cross-sections varied between  $\pm 27\%$  and  $\pm 37\%$  for antimuons. The uncertainty for proton cross-sections ranged between  $\pm 12\%$  and  $\pm 15\%$ , except at 4.7 MeV where it ranges from  $\pm 30\%$  to  $\pm 50\%$ .

From a rough analysis of results, the maximum antimuon SEU cross-section is about two orders of magnitude lower than the maximum proton SEU cross-section. Theoretically, the maximum electronic stopping force of a given impinging particle is then given by its charge and its velocity, as discussed in Chapter 2. All these parameters being equal for an antimuon and a proton, these particles should theoretically have the same maximum electronic stopping force, although this would occur at different energies because of their mass difference. However, in practice, this does not seem to translate



experimentally into similar maximum SEU cross-sections. In the following section, this discrepancy will be investigated with the help of Monte Carlo simulations.

### 3) Simulation results

The interaction of antimuons and protons with the tested device structures was simulated with the help of the Monte-Carlo Radiative Energy Deposition (MRED) code [110]. The geometry of the beam lines and devices was modelled, which included the bulk silicon, and the oxide and metal layers of the DUT. In the case of the antimuon simulations, the geometry also included the air, scintillator and various materials placed in front of the DUT. A detector region was set to simulate the sensitive volume (SV), which comprised the topmost 1  $\mu\text{m}$ -thick layer from the active silicon substrate. Complementary cumulative distribution functions (CCDF) of the particles' LET in the SV were computed, for antimuons and protons, with different initial particle energies (Figure 61 and Figure 62).

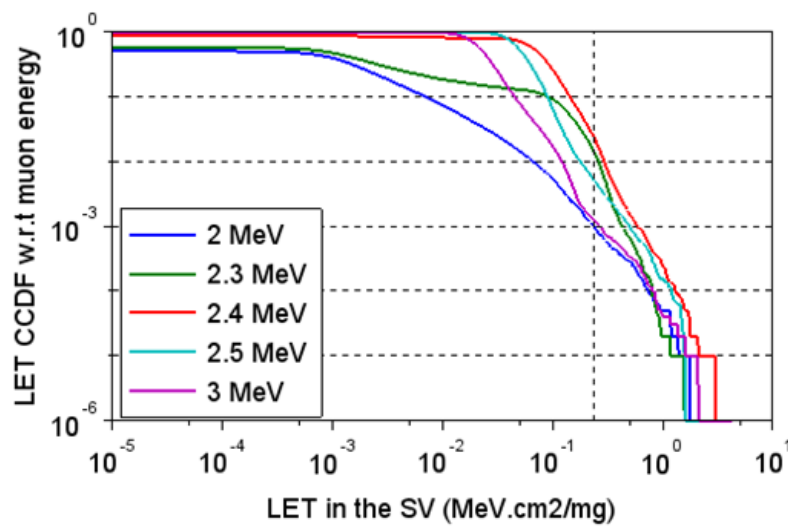


Figure 61: CCDF of the antimuon LET within the detector volume, for various initial beam energies. The dashed vertical line marks the critical LET used in the following analysis.

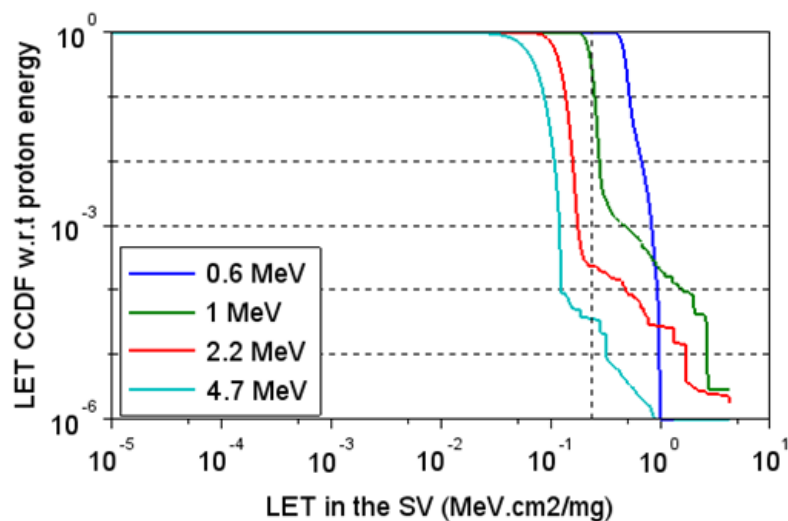


Figure 62: CCDF of the proton energy deposition within the detector volume, for various initial beam energies. The dashed vertical line marks the critical LET used in the following analysis.

The CCDF plots indicate the probability (vertical axis) that an impinging particle has an LET (i.e. induces a certain amount of charge carriers per unit length) equal or superior to a given threshold within the sensitive volume (horizontal axis). These plots have been normalized to the proportion of particles which effectively reach the DUT surface.

Comparing these curves provides an insight on the different behaviour of antimuon and protons. Proton LET CCDF curves start at a probability of 1, and then exhibit a clear elbow at an LET which depends on the original proton energy. Beyond this point, the probability abruptly decreases. Because protons are heavier than muons, there is less scattering in their trajectories due to interactions with the target electrons. Results obtained with SRIM [55] simulations indicate that for the concerned energies, the proton range longitudinal and lateral standard deviation is only about 5% of the average proton range.

Conversely, for low energies, the antimuon CCDF curves start at a probability lower than 1. This means that at low energies, some of the antimuons which reach the surface of the DUT are stopped or backscattered before reaching the sensitive volume. The antimuon CCDF curves also exhibit elbows, which occur at a lower LET than for protons, but the following decrease in probability is not as sharp as for the protons. For muon energies between 2 and 3 MeV, part of the CCDF curves extends into the region of high energy deposition. This shows that, on average, within the SV, antimuons deposit much less energy than protons, even though individual antimuons might deposit similar amounts.

The position of the elbow region of the CCDF curve is a good indicator of the probability to trigger an SEU with a given particle at a given energy: the farther up and right the elbow is, the higher is the probability of the particles having a high LET in the SV. According to this principle, the combined CCDF curves indicate that the maximum SEU rate should appear around 2.4 MeV for antimuons and 0.6 MeV for protons, which corresponds to the experimental observations (respectively 2.35 MeV and 600 keV).

The following analysis assumes that a memory cell's SV is identical in the case of antimuon and proton irradiation. If the occurrence of an SEU is determined by a particle depositing a critical charge in a SV, and the cell sensitive volumes are identical in both cases, then it is possible to compare the SEU rates obtained with antimuons and protons, as a function of this threshold LET value, by comparing the CCDF plots. By varying the SEU threshold LET, and plotting the corresponding deposition probabilities from the LET CCDF curves as a function of the incident particle energy, it is possible to study their effect on the predicted relative SEU rate, as shown in the plot presented on Figure 63, for protons.

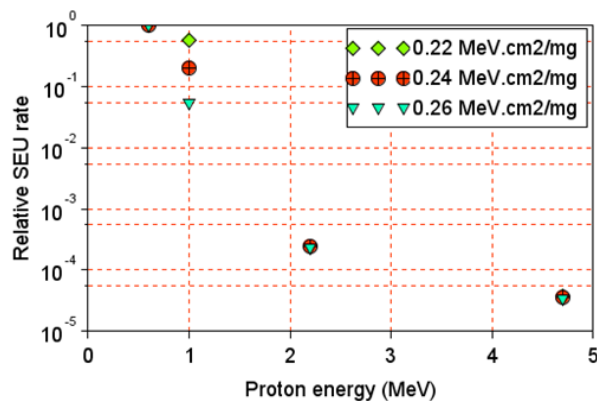


Figure 63: Effect of the SEU threshold LET and proton energy on the predicted SEU rate. Different curves are used for different values of SEU threshold LET.

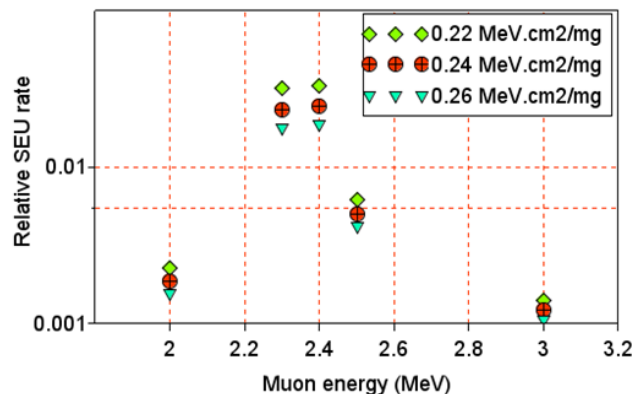


Figure 64: Effect of the SEU threshold LET and antimuon energy on the predicted SEU rate. Different curves are used for different values of SEU threshold LET.

The simulated evolution of the SER as a function of proton energy best matches the evolution of the experimental cross-section for an SEU threshold LET of about 0.24 MeV.cm<sup>2</sup>.mg<sup>-1</sup>. In Figure 64, a similar plot is given for the antimuon experimental data. Figure 63 shows that at the peak proton cross-section (600 keV), every particle which hits the SV releases enough energy to trigger an SEU, while (as seen on

Figure 64) at the peak antimuon cross-section, only about 2.5% of the particles which hit the SV do trigger an upset. This explains the two orders of magnitude difference which has been observed between the experimental proton and antimuon cross-sections.

#### 4) Summary

This study compared the response of the SRAM65 to low-energy proton and antimuon irradiation. A difference of two orders of magnitude was found between the maximum experimental antimuon and proton SEU cross-sections, despite the theoretically similar maximal particle LETs. Simulation results performed with MRED clarified the experimental results: the lighter mass of antimuons (compared to protons) results in stronger beam energy and range straggling, which leads to a lower effective SEU cross-section at low energies. This means that proton testing methods may not be directly applicable to SEU testing with muons; the strong energy straggling undergone by antimuons before reaching the DUT sensitive volume should be carefully considered when designing an experiment, in particular on devices with thick overlayers.

#### D. Failure mode analysis of an FRAM

As was mentioned in Chapter 3, Ferroelectric Random-Access Memories (FRAMs) store information as the electric polarisation of ferroelectric capacitors. FRAM memory cells have shown extreme resilience to TID [111] and SEE [112], and a high resilience to DD [113]. However, the memory array is controlled by elements implemented in CMOS technology, which are vulnerable to radiation and may be the cause of different types of failures. This section presents the results of an investigation into the failure modes of the Cypress FM22L16 FRAM [114].

##### 1) Experimental setup

The FRAM device (see Chapter 6) was irradiated in several test campaigns, with heavy ions at RADEF (Radiation Effects Facility, Univ. Jyväskylä, Finland) and GANIL (Grand Accélérateur National d'Ions Lourds, Caen, France), and pulsed, focused X-rays at APS (Advanced Photon Source, Argonne National Laboratory, Chicago, USA). The main characteristics of the beams are summarized in Table 5.

Facility	DUT	Test particle	Energy	Flux per run ( $\text{cm}^{-2}\cdot\text{s}^{-1}$ )	Total fluence ( $\text{cm}^{-2}$ )
GANIL	#1	Heavy ions (Xe)	3.4 MeV/u, 13.2 MeV/u	$4.0\cdot 10^2$ to $7.0\cdot 10^4$	$1.7\cdot 10^6$
RADEF	#2	Heavy ions (Fe, Kr, Xe)	9.3 MeV/u	$1.0\cdot 10^3$ to $5.0\cdot 10^4$	$5.91\cdot 10^7$
RADEF	#3	Heavy ions (Kr, Xe)	9.3 MeV/u	$1.0\cdot 10^3$ to $4.0\cdot 10^5$	$7.7\cdot 10^6$
RADEF	#4	Heavy ions (Ne, Ar)	9.3 MeV/u	$1.0\cdot 10^4$ to $1.8\cdot 10^4$	$1.01\cdot 10^8$
APS	#5	Pulsed, focused X-rays	8 keV, 87pJ/pulse, 37 MeV. $\text{cm}^2\cdot\text{mg}^{-1}$ equ. LET [115]	0.91	$3.0\cdot 10^8$

Table 5: Summary of the test campaigns used as a data source for this study.

DUT #5 was irradiated using beamline 20-ID-B at APS. The X-ray pulses delivered by the beam have a full width at half maximum (FWHM) duration of 100 ps, and a FWHM spot size of  $1.77\ \mu\text{m} * 1.81\ \mu\text{m}$ . The X-ray energy was set at 8 keV; the attenuation lengths for the most common materials used in IC manufacturing at this photon energy are presented in Table 6 (calculated with [116]).

The open-top DUT has about 5  $\mu\text{m}$  of interconnecting and passivation layers above the active silicon region [117]. We can estimate the attenuation caused by these layers to be minor, since they are mainly composed of  $\text{SiO}_2$ , Al and Cu. Denser materials such as Sn and W are typically used only for the lowest, thinnest interconnect layers and connecting plugs, in small amounts, while TaN is used only as a thin barrier layer between Cu and insulators.

Throughout this campaign, the total pulse energy at the DUT surface was 87 pJ. In [115], a method has been developed to correlate the transients resulting from the collection of charge carriers generated by pulsed X-rays (using the same APS beam line) and heavy ions. Using the coefficients and equivalence model described in [115], we can calculate the equivalent LET of the X-ray pulses,  $\text{LET}_{eq}$ :

$$\text{LET}_{eq} = \frac{1}{a} E_{pulse} (b E_{pulse} + c) \quad \text{Equation 1}$$

$$\text{LET}_{eq} = \frac{1}{0.172} \times 87 \times (1.16 \cdot 10^{-4} \times 87 + 7.4 \cdot 10^{-2}) \quad \text{Equation 2}$$

$$\text{LET}_{eq} = 43 \text{ MeV} \cdot \text{cm}^2 \cdot \text{mg}^{-1} \quad \text{Equation 3}$$

i.e. an X-ray equivalent LET of  $43 \text{ MeV} \cdot \text{cm}^2 \cdot \text{mg}^{-1}$  at the DUT surface. In the following discussion, we assume an overlayer profile of 1.5  $\mu\text{m}$  of Al, 1.5  $\mu\text{m}$  of Cu and 3  $\mu\text{m}$  of  $\text{SiO}_2$ ; this results in about 11% pulse energy absorption between the DUT surface and the active silicon region [116]. The formula from [115] then predicts a  $37 \text{ MeV} \cdot \text{cm}^2 \cdot \text{mg}^{-1}$  equivalent LET at the sensitive volume depth. The attenuation length in silicon is so large (69.6  $\mu\text{m}$ ) compared to the typical dimensions of logic gates and register cells (a few square micrometers) that for our purposes, we can consider the beam unattenuated once it reaches the silicon, generating charge carriers in a long vertical column.

Several regions of the die have been selectively irradiated, to identify the failure modes triggered by specific circuits. These included either memory cells or parts of the central spine (a region of the die containing peripheral circuitry, running across the memory array).

## 2) Bitmap generation

The failure modes of the device were analysed with the use of bitmaps. The bitmaps generated from the FRAM data are slightly different than those generated for the SRAM devices. FRAM bitmaps are originally 64 pixels wide and 65536 pixels high; the resulting image is divided into 32 bands of equal lengths, which are laid out next to each other, to form a square image. This means that FRAM bitmaps are read in a specific manner, as indicated on Figure 65. These bitmaps have a black background, and errors are indicated by coloured pixels; similar colours identify errors which were detected on the same element and operation of the algorithm. For ease of reading, the bitmaps are divided into sectors by grey horizontal and vertical lines, which match the height of some error cluster types (e.g. type 4, see Figure 67).

Material	Density ( $\text{g} \cdot \text{cm}^{-3}$ )	$\alpha$ ( $\mu\text{m}$ )
Si	2.33	69.6
$\text{Si}_3\text{N}_4$	3.44	72.9
$\text{SiO}_2$	2.2	130.4
Al	2.7	77.6
Sn	7.3	5.5
Cu	9.0	21.9
W	19.3	3.1
TaN	14.3	4.67

Table 6: Attenuation lengths  $\alpha$  for 8 keV photons in materials commonly used in IC manufacturing.

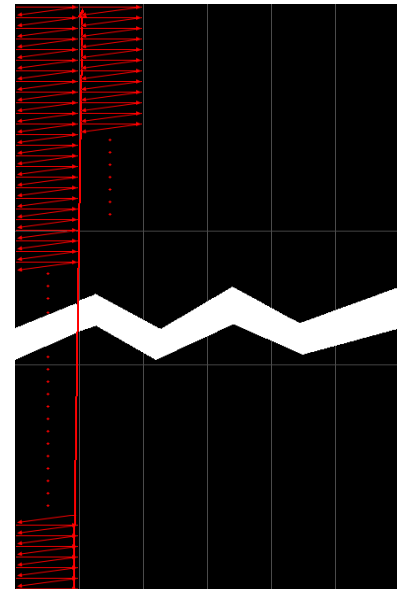


Figure 65: Reading direction for FRAM bitmaps.

### 3) Experimental results

The bitmaps revealed at least eight different failure modes:

- Type 1 events are 1-bit failures, which can be isolated errors (type 1a), or isolated errors occurring at addresses related to (sharing many bits with) previous errors (type 1b). Type 1 events were observed on all test campaigns, during both static and dynamic tests. (Figure 66)
- Type 2 events consist in several bits in one word being upset at once. The word may be either partially corrupted (type 2a) or completely corrupted (type 2b). Type 2 events were observed on all test campaigns, during both static and dynamic tests. (Figure 66)



Figure 66: Logical bitmap from an anti-Gray dynamic stress test with krypton ( $LET\ 32\ MeV.cm^2.mg^{-1}$ ).

Facility	Device/DUT	Ion	Energy (MeV)	LET@surface ( $MeV.cm^2.mg^{-1}$ )	Tilt angle (degrees)	Flux ( $counts.s^{-1}.cm^{-2}$ )	Fluence ( $counts.cm^{-2}$ )	Test type	Addressing
RADEF	FRAM/3	Kr	768	32.1	0	$5.0 \cdot 10^3$	$3.0 \cdot 10^5$	Dynamic stress	Anti-Gray

- Type 3 events consist in several pages with the same page number (appear at the same height within their logical bitmap sectors) showing large numbers of upsets affecting several words. Type 3 errors were only observed on heavy-ion campaigns, and only on dynamic tests. (Figure 67)
- Type 4 events consist in one particular bit of every page within a logic sector suffering either intermittent errors (type 4a) or continuous errors (type 4b), resulting in an interrupted or continuous vertical line on the chronological bitmap. In addition, sparse single-bit upsets (SBUs) may occur randomly within the affected sector. Type 4 events were observed on all test campaigns, mostly on dynamic tests. (Figure 67)

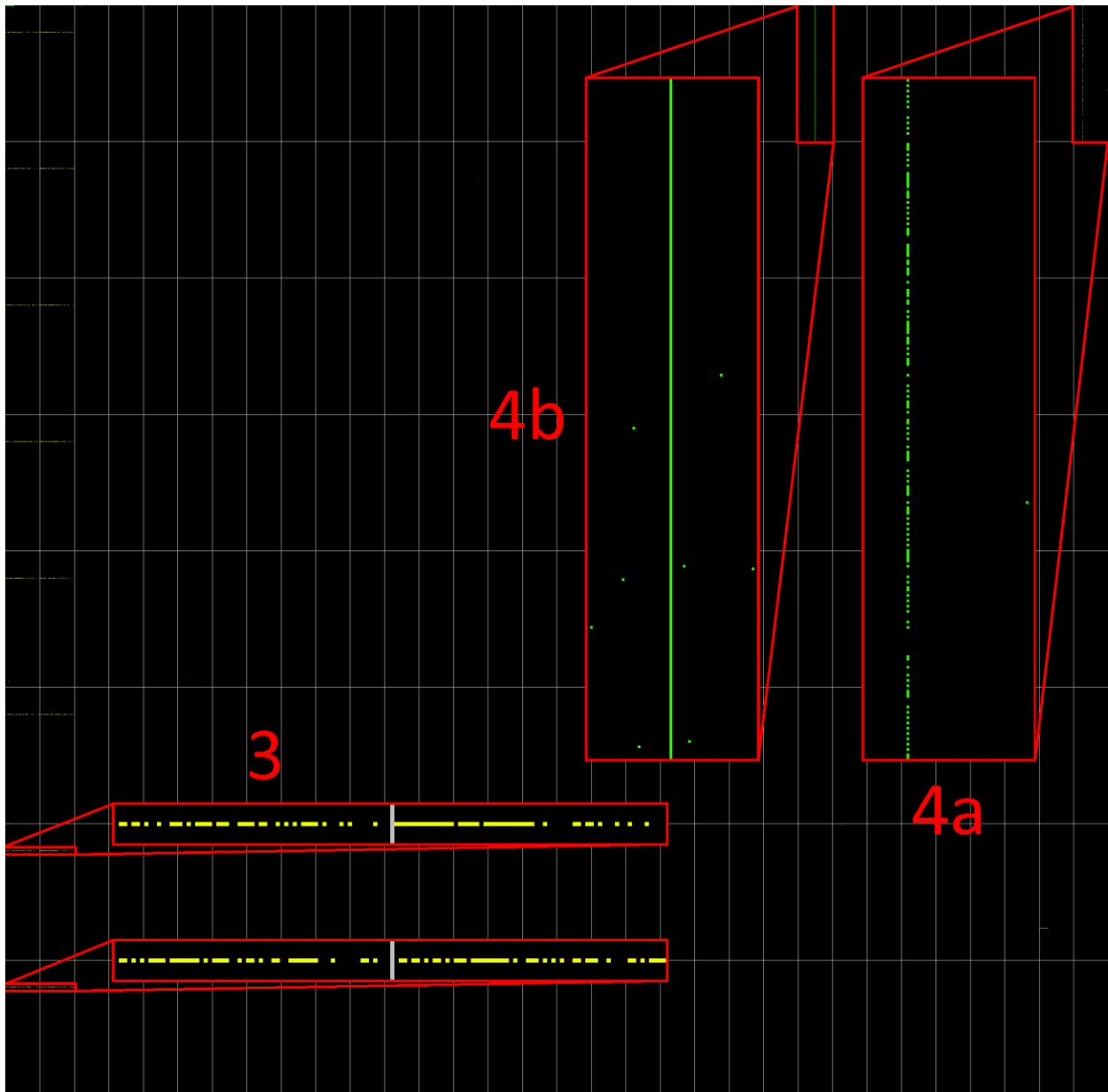


Figure 67: Logical/chronological of a natural addressing mMATS+ test with nitrogen ( $LET\ 1.8\ MeV.cm^2.mg^{-1}$ ).

Facility	Device/DUT	Ion	Energy (MeV)	LET@surface ( $MeV.cm^2.mg^{-1}$ )	Tilt angle (degrees)	Flux ( $counts.s^{-1}.cm^{-2}$ )	Fluence ( $counts.cm^{-2}$ )	Test type	Addressing
RADEF	FRAM/3	N	139	1.8	0	$3.0 \cdot 10^5$	$1.2 \cdot 10^7$	mMATS+	Natural

- Type 5: the chronological bitmap on display on Figure 68 was gathered during an anti-Gray dynamic stress test on DUT #4. It exhibits, among type 1 and 2 events, two small blocks of errors in the top left corner; each block is made of 38 completely upset words. A closer examination of the data logs reveals that each of these 76 addresses actually returned errors on several occasions, during two consecutive element scans of the Dynamic stress algorithm. During the first element scan, after the w0 operation, the five consecutive r0 operations all failed on each of these addresses; then, on the next element scan, the first operation, r0, failed on all these addresses. Subsequent accesses to these memory locations returned no errors for the rest of the test.

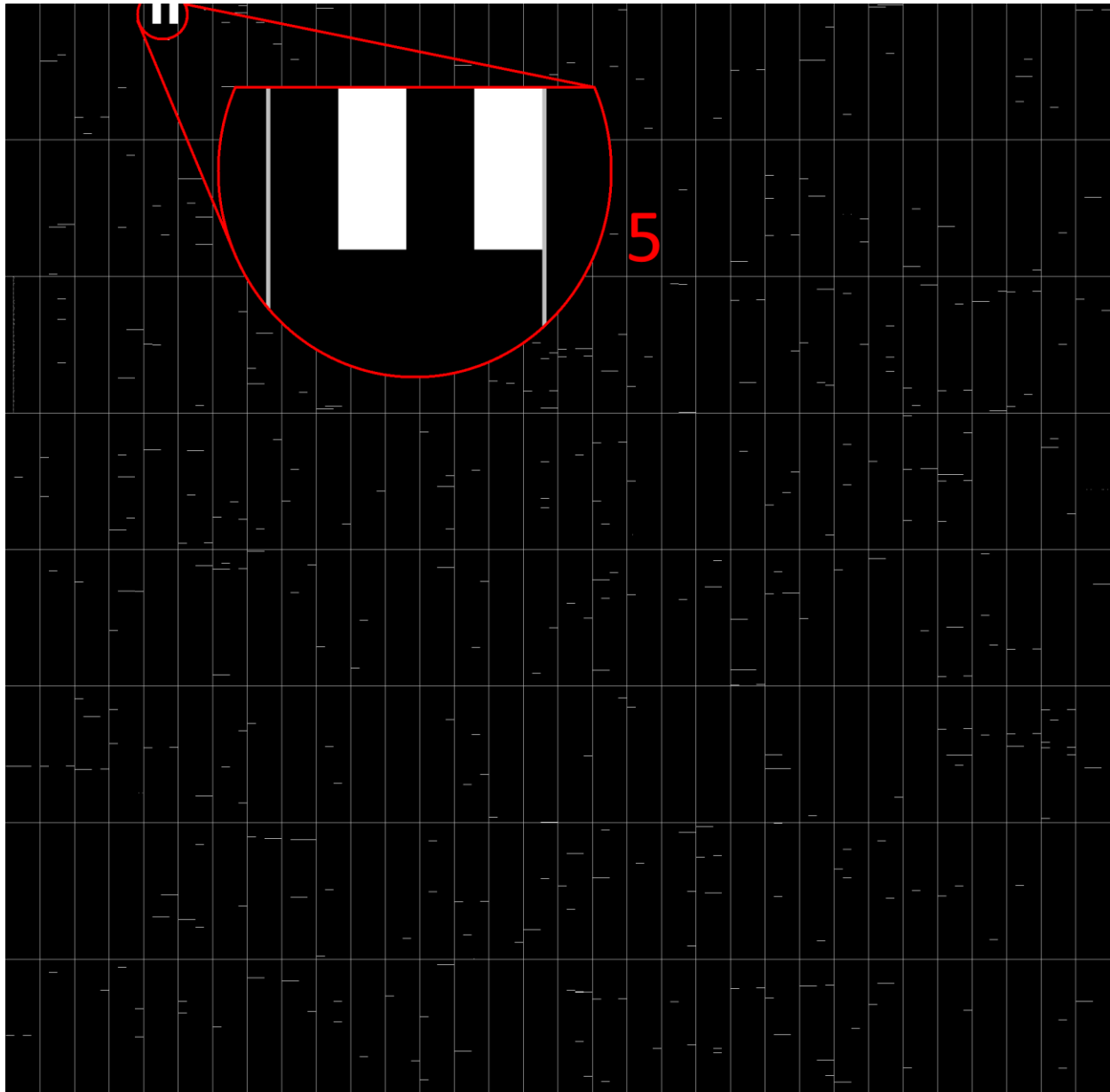


Figure 68: Chronological bitmap of an anti-Gray dynamic stress test with argon at 30° (LET 11.7 MeV.cm<sup>2</sup>.mg<sup>-1</sup>).

Facility	Device/DUT	Ion	Energy (MeV)	LET@surface (MeV.cm <sup>2</sup> .mg <sup>-1</sup> )	Tilt angle (degrees)	Flux (counts.s <sup>-1</sup> .cm <sup>-2</sup> )	Fluence (counts.cm <sup>-2</sup> )	Test type	Addressing
RADEF	FRAM/4	Ar	372	1.17	30	1.3·10 <sup>4</sup>	1.0·10 <sup>6</sup>	Dynamic stress	Anti-Gray

The logical bitmap for this test run is available on Figure 69. This figure shows how all the errors visible on the chronological bitmap in Figure 4 have closely related addresses (they are close to each other on the logical bitmap). Type 5 failures are rare: they were only reported once, during this heavy-ion test on DUT #4.

- Type 6 events consist in several hundred consecutively-accessed words being either completely upset (type 6a), or completely upset except for a few occasional bits (type 6b). The colored blocks appearing on Figure 70 are type 6a events. The number of words affected by type 6 failures seems

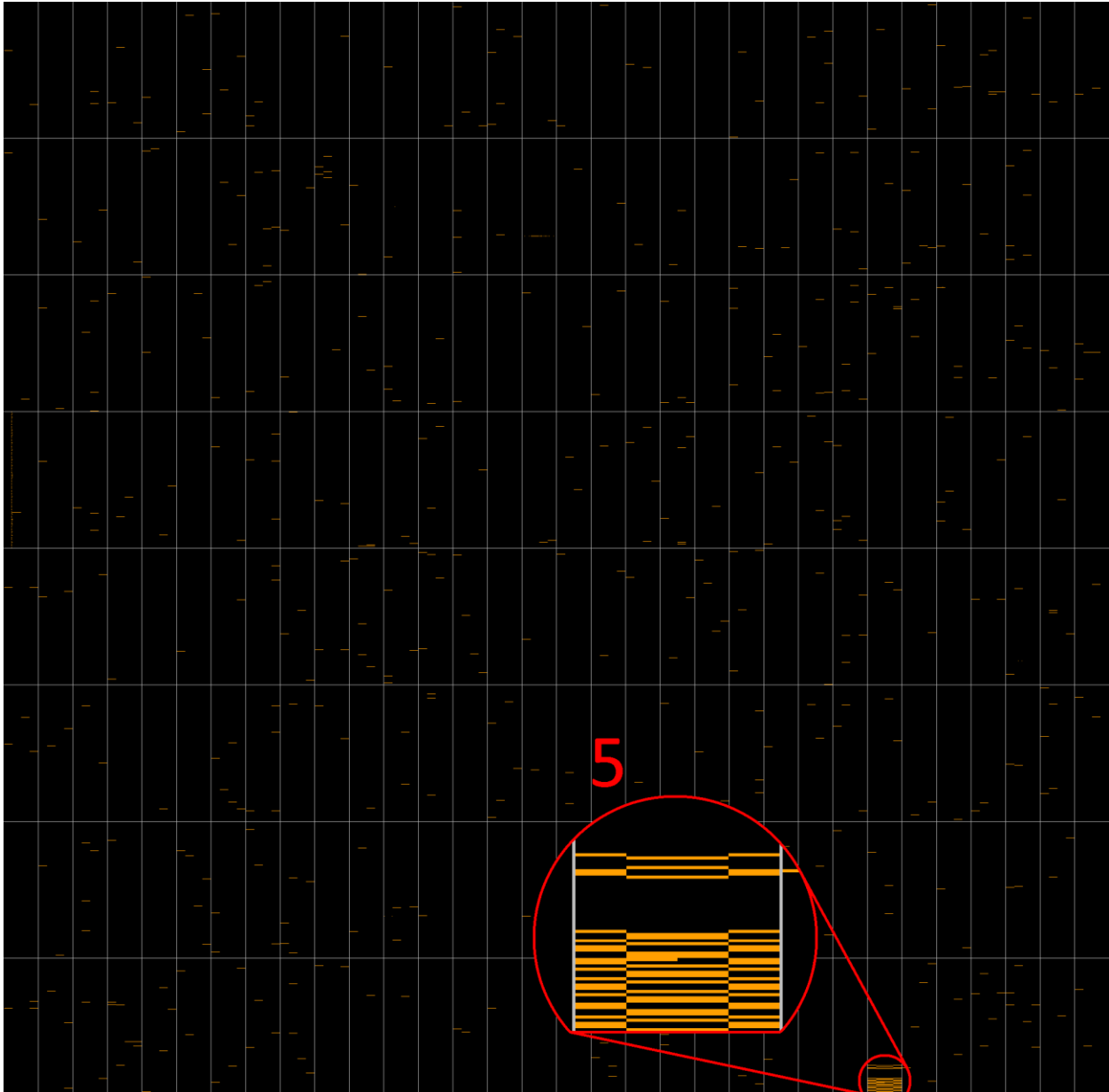


Figure 69: Logical bitmap of an anti-Gray dynamic stress test with argon at 30° (LET 11.7 MeV.cm<sup>2</sup>.mg<sup>-1</sup>). This bitmap contains the same data as that visible on Fig. 68, and the zoom-in identifies the errors highlighted in the zoom-in of Fig. 68. The complex pattern is caused by the complex anti-Gray addressing used for this test.

Facility	Device/DUT	Ion	Energy (MeV)	LET@surface (MeV.cm <sup>2</sup> .mg <sup>-1</sup> )	Tilt angle (degrees)	Flux (counts.s <sup>-1</sup> .cm <sup>-2</sup> )	Fluence (counts.cm <sup>-2</sup> )	Test type	Addressing
RADEF	FRAM/4	Ar	372	1.17	30	1.3·10 <sup>4</sup>	1.0·10 <sup>6</sup>	Dynamic stress	Anti-Gray



to be directly influenced by the type of dynamic test, and more precisely, by the speed at which the algorithm scans across the address space. Figure 70 exhibits several type 6a events, each affecting about 350 words. The data for this figure was gathered during an mMATs+ test; the elements of this algorithm contain two operations each. The data used for Figure 71 was gathered on the same DUT in exactly similar conditions, except that the test algorithm was Dynamic Classic, whose elements only contain one operation – meaning that the Dynamic Classic algorithm scans addresses faster. Figure 71 also exhibits several type 6a events, but in this case each event affects about 770 words. This correlation between algorithm scanning speed and type 6 event severity was verified on tens of different test runs; it indicates that type 6 events last for a constant amount of time (or a constant amount of I/O operations).

Type 6 events were observed only on heavy-ion campaigns, dynamic tests only.

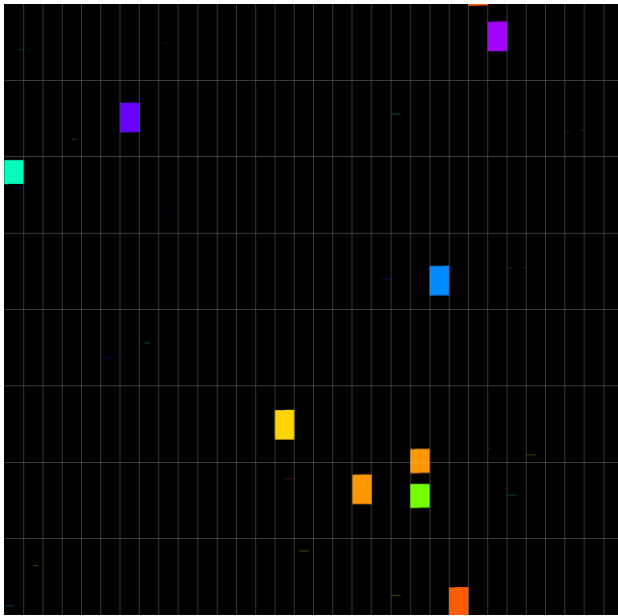


Figure 70: Logical/chronological bitmap obtained from an mMATs+ test with xenon (LET 64.3 MeV.cm<sup>2</sup>.mg<sup>-1</sup>).

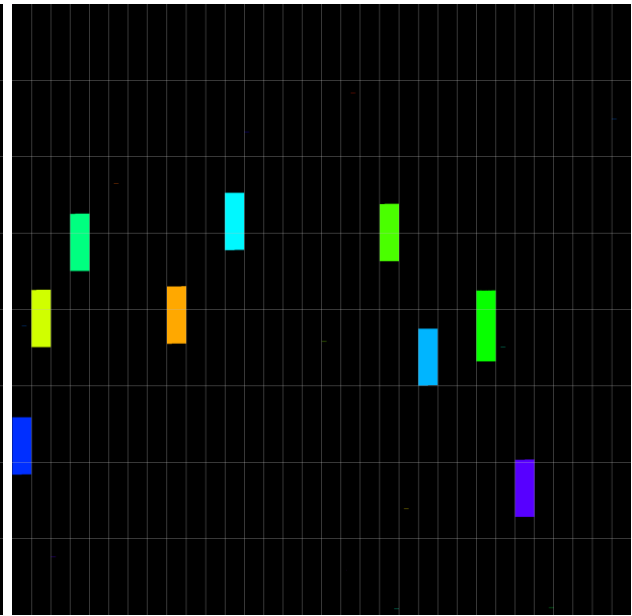


Figure 71: Logical/chronological bitmap obtained from a dynamic classic test with xenon (LET 64.3 MeV.cm<sup>2</sup>.mg<sup>-1</sup>).

Facility	Device/DUT	Ion	Energy (MeV/u)	LET@surface (MeV.cm <sup>2</sup> .mg <sup>-1</sup> )	Tilt angle (degrees)	Flux (counts.s <sup>-1</sup> .cm <sup>-2</sup> )	Fluence (counts.cm <sup>-2</sup> )	Test type	Addressing
GANIL	FRAM/1	Xe	3.43	64.3	0	5.0·10 <sup>2</sup>	1.0·10 <sup>5</sup>	mMATs+ Dynamic classic	Natural

- Type 7 events involve several thousands to tens of thousands of consecutively-accessed words, which exhibit a high density of random upsets, generating hundreds of thousands to millions of upsets. The device may eventually recover from the condition spontaneously. The type 7 event visible on Figure 72 is the logical/chronological bitmap from a pulsed X-ray test on DUT #5 at APS. The beam scanned a region of the central peripheral spine, while a natural-order mMATs+ dynamic test was performed. This type of SEFI also occurred during heavy-ion dynamic testing.

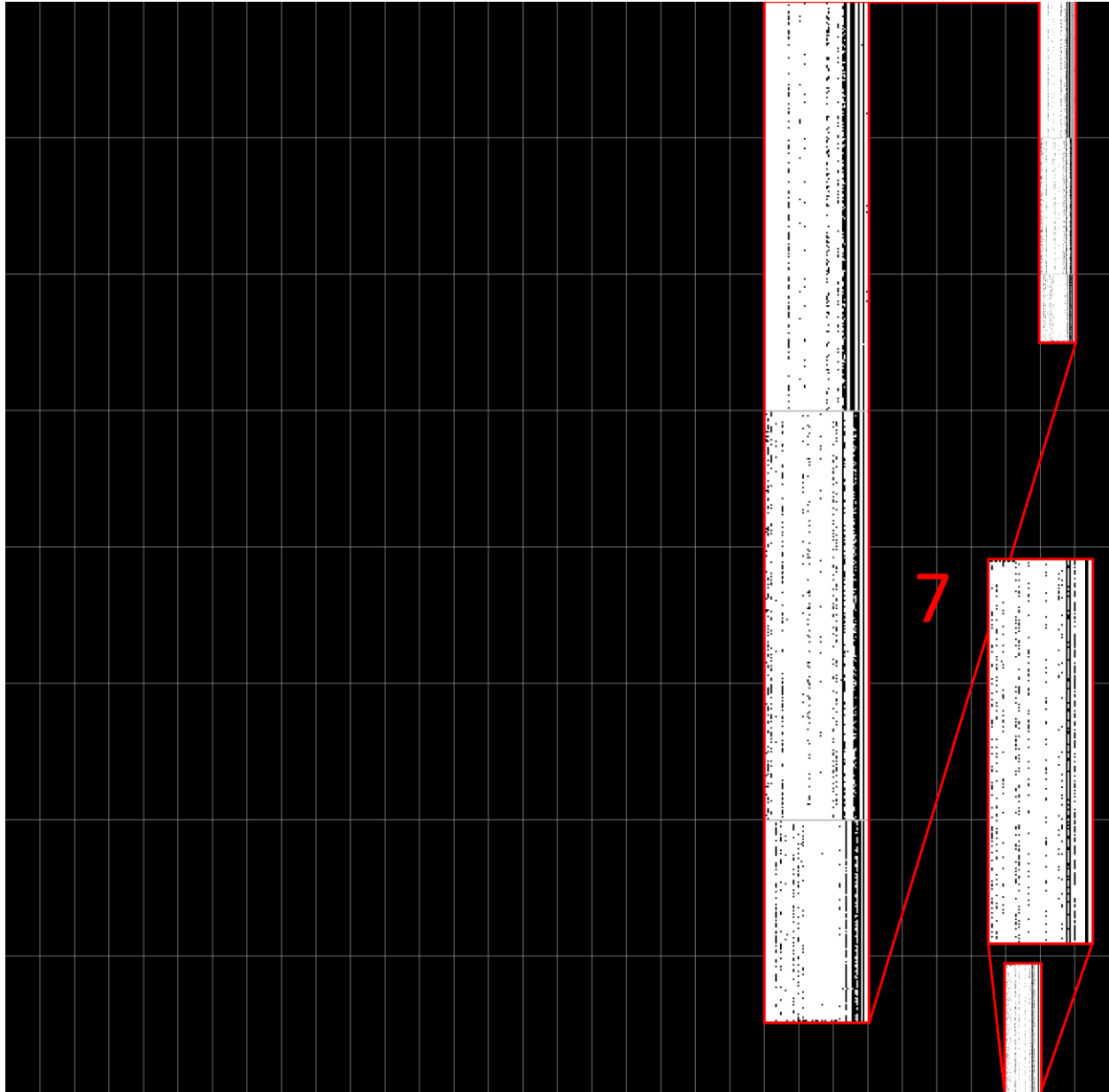


Figure 72: Logical/chronological bitmap obtained from an mMATS+ test with pulsed X-rays aimed at the central peripheral spine of DUT #5 (equivalent LET 37 MeV.cm<sup>2</sup>.mg<sup>-1</sup>).

Facility	Device/DUT	Ion	Energy (MeV)	LET@surface (MeV.cm <sup>2</sup> .mg <sup>-1</sup> )	Tilt angle (degrees)	Flux (counts.s <sup>-1</sup> .cm <sup>-2</sup> )	Fluence (counts.cm <sup>-2</sup> )	Test type	Addressing
RADEF	FRAM/4	Ar	372	1.17	30	1.3·10 <sup>4</sup>	1.0·10 <sup>6</sup>	Dynamic stress	Anti-Gray

- Type 8: several thousands to tens of thousands of words are either entirely, or almost entirely corrupted; these words all have a few address bits in common. This is evidenced by the fact that on a logical bitmap, the errors generated by type 8 events fill up entire binary subdivisions of the bitmap – either the whole bitmap, or one half, or one or more quarters or eighths, etc. This is evident on Figure 73, where a type 8 event takes up a whole eighth of the bitmap. Since this is a logical bitmap from a natural-addressing test, it means that the type 8 event started as the third

most-significant address bit toggled from 0 to 1, and ended as soon as it toggled back to 0. This type of event was recorded on all heavy-ion test campaigns, but on dynamic tests only. Type 8 events were also detected on dynamic tests where the addressing was not natural – for example, anti-Gray. This means that the errors which appear during a type 8 event are not necessarily accessed consecutively.

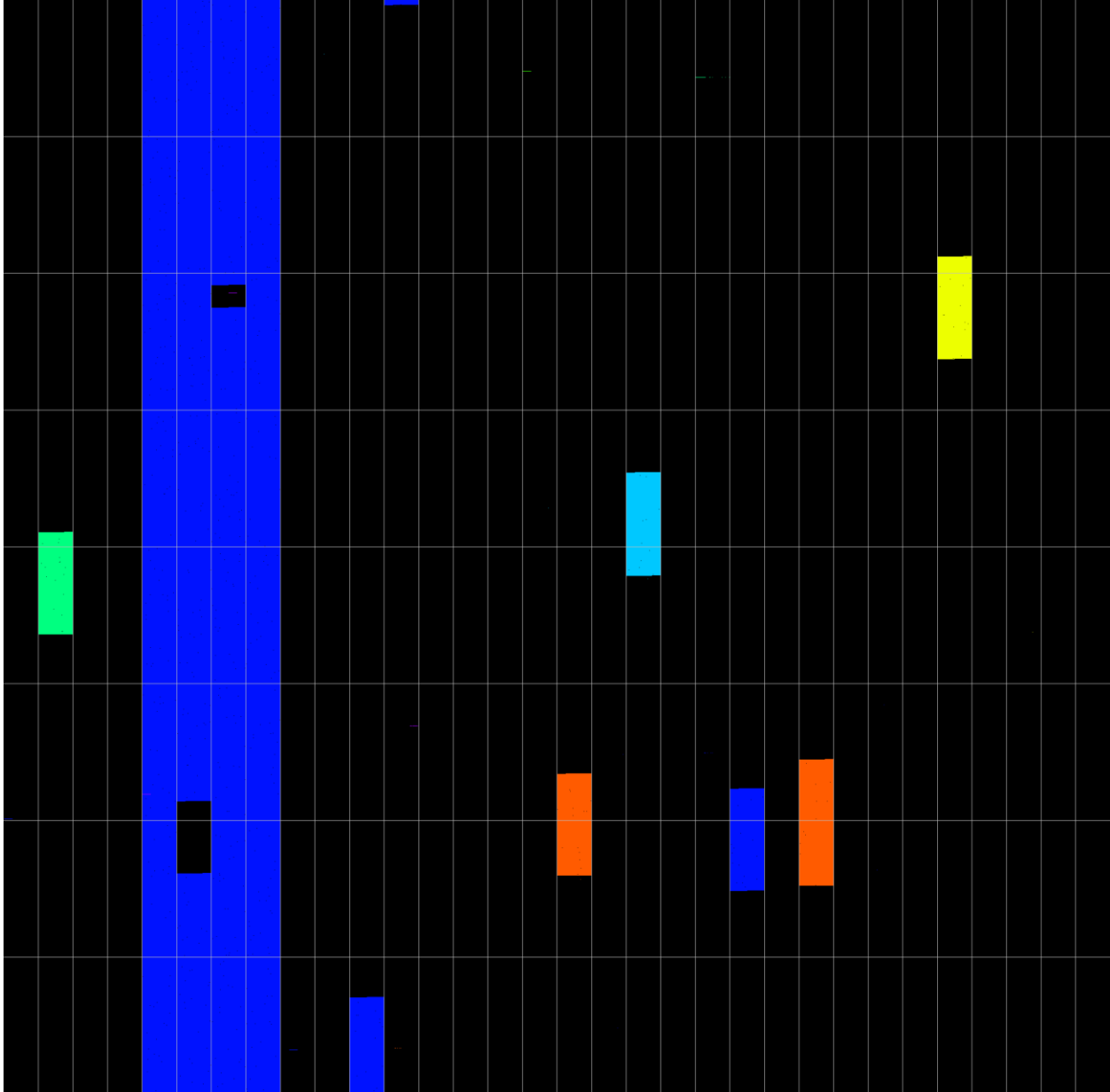


Figure 73: Logical bitmap from a natural Dynamic Classic test with krypton ( $LET\ 32.1\ MeV.cm^2.mg^{-1}$ ).

Facility	Device/DUT	Ion	Energy (MeV)	LET@surface ( $MeV.cm^2.mg^{-1}$ )	Tilt angle (degrees)	Flux ( $counts.s^{-1}.cm^{-2}$ )	Fluence ( $counts.cm^{-2}$ )	Test type	Addressing
RADEF	FRAM/3	Kr	768	32.1	0	$5.0 \cdot 10^3$	$3.0 \cdot 10^5$	Dynamic stress	Anti-Gray

Several noteworthy events occurred during static heavy-ion tests on DUT #2. The memory was written with a known data pattern (every word contains the lower 16 bits of its address vector) and irradiated under bias, then read back. On a few occasions, with iron, krypton and xenon beams, the readback data contained a few words with erroneous data (type 2a errors). These errors can be considered permanent, since subsequent readbacks returned the same errors. However, they disappeared after power cycling the DUT.

Similar events occurred during a static test on DUT #5, with the X-ray beam aimed at the central spine. The device was written with a known data pattern, then irradiated. When read back after the irradiation, two type 2a events were detected at unrelated addresses. These two words were marked by overwriting a specific data pattern (0xABCD), after which the device was power cycled, and read back again: the readback data were correct at all addresses, except from the two words, which previously underwent a type 2a event (they did not contain 0xABCD anymore). These two words were written with 0xABCD again, the DUT was power cycled again, after which the memory performed as expected.

#### 4) Discussion

These different failure modes suggest the occurrence of faults in several different elements of the peripheral circuitry.

Type 1 and 2 SEEs were detected both in static and dynamic modes, both during heavy-ion testing and X-ray periphery attacks, but never during X-ray FRAM cell attacks, thus their origin must lie in the peripheral circuitry. These events never occurred when the memory was irradiated in a powered-off state. Errors disappear after a power cycle; however, if new data are written to a corrupted word before cycling power, these data will change after the power cycling. This indicates that the element of the periphery which is upset by radiation is restored in its correct state during device power-on boot. One potential cause of these SEE could be upsets occurring in SRAM-based redundancy registers, whose purpose is the reallocation of faulty memory elements (rows, columns, blocks) to spare elements within the memory array. Upsets in such registers will be latched and trigger errors until they are reinitialized to their correct value. These registers are always reloaded with correct values at device power-on.

Type 4 SEE: the facts that this type of event occurred during X-ray periphery testing, and that most of the errors generated occur at the same bit of the same word within their page suggest two possible fault mechanisms. The first hypothesis is an upset of a redundancy register, with the consequence of either reallocating a functional column to a spare column (thus not correctly initialized), creating a continuous 4b event; or the re-allocation of a spare column to a malfunctioning column (not supposed to be used), or the allocation of a functioning column to a malfunctioning spare (not supposed to be used), resulting in an intermittent 4a error. The second hypothesis is the occurrence of a micro-latchup event or a stuck bit in a page buffer. Such events induce metastability in the buffer cells, explaining the occurrence of seemingly random errors occurring concurrently to the “vertical lines” in the rest of the page buffer positions during type 4 events (see Figure 67).

Type 3 SEE: these events could have similar origins to those of type 4 events. Since the affected pages share similar page numbers, they could all be part of a single memory row which was reallocated to a spare row. Another possibility would be that an element common to these pages (e.g. a low-level address decoder) was disturbed during the test.

Type 5 SEE: the addresses involved in this event started returning all-corrupted words after a w0 operation. For each of these addresses, several read operations spread over two scanning cycles returned the same result, until their cells were eventually rewritten. This failure can be explained by a temporary stuck address bit. Typically, during an access to the memory, the value input on the memory's address pins is loaded into an address buffer. If, under the effect of radiation, one or more bits from the buffer get stuck, then the requested operation will be performed at the wrong memory location. This hypothesis is supported by the chronological bitmap on Figure 68, which indicates that during the event, in chronological order, every other address accessed failed. This is consistent with the fact that all address bits -but one- toggle from one access to the next in anti-Gray addressing mode: the stuck bit fault can only trigger errors on every other position accessed.

Another explanation for this event could be a failure of the write operation of the first element of the algorithm. As indicated by Figure 69, all the words involved in this event have related addresses, which means that there is a high probability that they share common read/write control circuits. It is possible that locally, the peripheral elements required for write operations were temporarily disabled by an ion strike. This hypothesis is supported by the fact that no other large group of errors is visible on the logical bitmap.

Type 7 events are large-scale functional interrupts, which do not affect an "even" amount of words (a power of 2), seemingly start and stop at random address positions, and trigger a pseudorandom output, could originate in an upset of device configuration registers, or in a micro-latch-up affecting peripheral elements. Micro-latch-up conditions have been shown to disappear spontaneously in CMOS devices, when the high voltage lines sustaining them are switched off as part of normal device activity [98].

Type 8 events are large-scale failures which affect an "even" amount of words (a power of 2). They begin and end when certain address bits toggle; since each address bit controls one level of address decoding, type 8 events must be "mapped" on the memory array. For example, the type 8 event visible on Figure 73 affected exactly one eighth of the memory array; since the memory array is organized in eight blocks, one possibility is that a radiation-induced upset in a configuration register disabled a critical element in one of the eight memory blocks – and that subsequent accesses to this memory block returned an erroneous value. Since three address bits are used to select blocks, the type 8 event started when the lowest-level block-selecting bit toggled, and ended when another block was selected at the next toggle. Possible origins for these events could be upsets in configuration registers (e.g. controlling power switches feeding memory blocks).

This study shows that the SEE occurring in the FM22L16 come in several types, with different root causes, of different magnitudes and severity. All these SEEs can be considered to originate in the peripheral circuitry, as also suggested by previous studies [117][118]. However, experimental data show that at least some categories of SEE (notably type 2 errors) can be avoided by forcing a reset of the involved peripheral elements via power cycling the DUT before access (and possibly via putting the device out of sleep mode). This has major implications regarding the device's radiation sensitivity, since type 2 events are by far the most frequently encountered. Many applications using the device as a storage memory could easily implement systematic power cycling before device access as an error mitigation technique.

The results of this study suggest that hardening key elements of the peripheral circuitry of a memory device (e.g. implementing the registers with additional transistors [119] or a dual-interlocked cell architecture [120]) could effectively mitigate the most common failure modes. This would dramatically

improve the failure rate of the device, at the expense of a small increase in the area of the peripheral circuitry.

### E. Effects of heavy-ion radiation on a Single-Level Cell NAND flash memory

The study presented in this section was driven by the MTCube project [21][22], which calls for a 1-Unit CubeSat to expose several types of memories fabricated with both legacy and emerging technologies to space radiation, including the Micron flash memory. These results were also published in V. Gupta's 2017 doctoral thesis dissertation [123]. Several different failure modes were observed after static heavy-ion irradiation.

#### 1) Experimental setup

Two test campaigns were conducted, as summarized in Table 7. All tests were carried at normal beam incidence angle with respect to the die surface.

The first test campaign was carried out at GANIL [124] in Caen, France on two specimens. The primary xenon beam was degraded to reach a LET of  $26.75 \text{ MeV.cm}^2.\text{mg}^{-1}$  at the surface of the DUT. The tests were performed in air. The second test campaign took place at the RADEF facility [125] at the University of Jyväskylä, Finland. Tests were carried out on two specimens in vacuum, with beams yielding LETs of 1.8 to  $60 \text{ MeV.cm}^2.\text{mg}^{-1}$ .

The fluence ranged from  $1.0 \times 10^4$  to  $1.5 \times 10^5 \text{ cm}^{-2}$  for each individual test, during both irradiation campaigns. As for static buffer testing (at RADEF only), the fluence ranged between  $6.2 \times 10^2$  and  $1.0 \times 10^5 \text{ cm}^{-2}$  per test. At both facilities, the beam homogeneity was estimated to be +/- 10% or better over the device area.

Test campaign	Ion	Energy (MeV)	Effective LET (@ surface) (MeV/(mg/cm <sup>2</sup> ))	Range (μm)
GANIL	Xe	46.55	26.8	700
RADEF	N	139	1.8	202
	Fe	523	18.5	97
	Kr	768	32.1	94
	Xe	1217	60.0	89

Table 7: Heavy-ion cocktails used at the different facilities. The values were provided by the facilities.

The memory devices were tested under two different test modes: the static (or retention) mode, and the static buffer mode. The DUTs were biased during irradiation. Due to the very large capacity of the memory, only 512 Mib (64 blocks) out of 32 Gib were considered for the static tests.

In static buffer mode, instead of reading the memory normally, one page (64 kib) was loaded, so that its contents were stored on the memory data buffer; then the sequence of commands to carry out a reading operation was interrupted, and the DUT was irradiated; finally, the reading operation was completed to check the contents of the buffer.

Several operations (Erase, Write, Read) were performed in between runs, before and after Power Cycles (PC), to observe the errors occurring during the test runs and to ensure that the device was error-free prior to the next run.

## 2) Experimental results and discussion

### Static mode tests

Static tests performed with nitrogen resulted in respectively 1 and 2 SBU (Single-Bit Upset within a word) when using the solid '0' pattern at a respective fluence of  $3.0 \cdot 10^4$  and  $1.510^5$   $\text{cm}^{-2}$ . At those levels of fluence, no errors were recorded when using the solid '1' pattern. An erase operation was sufficient to correct the SBUs without the need of a PC.

Irradiation results with the other heavy-ion particles resulted in widely varying numbers of erroneous words per test, requiring a deeper analysis. Besides counting the number of erroneous words, the number of upset bits was evaluated for each word presenting error(s), and logical bitmaps were generated. The bitmaps of the Flash memory are built as follows: the left half of the bitmap contains the even blocks, while the right half contains the odd blocks (accordingly with the manufacturer datasheet). Each block is made of 128 horizontal lines, which each corresponds to a page. Each line is made of 8192 pixels, one per column – each column holding one memory word. The individual bits of each word are not represented on the bitmap. The two planes of the memory (halves of the bitmap) have their own data buffer. Due to the very large size of the generated bitmaps (over 64 million pixels each), it is not possible to clearly display them entirely, hence only their most relevant sections will be exhibited to support the test results analysis. Regular patterns of errors were observed such as Vertical Lines (VLs) of errors, as well as small clusters of words or isolated words with errors.

For each run, histograms were plotted, displaying the total count of word errors for each column on the 64 memory blocks which were tested. An example of a histogram is shown in Figure 74. The leftmost plots

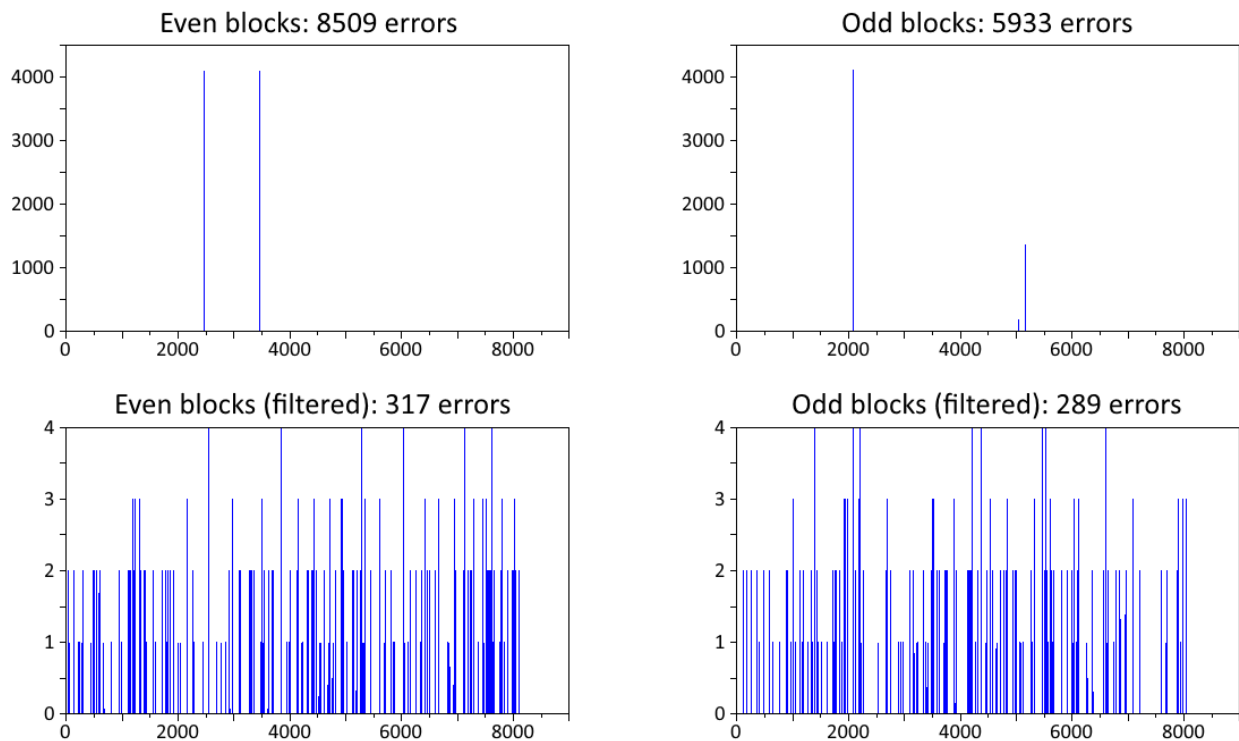


Figure 74: Histogram of a static test bitmap, where the number of word errors (ordinates) is plotted for each column (abscissa). The two leftmost (resp. rightmost) plots represent the plane containing the even (resp. odd) blocks. The lower histograms represent the error counts after removing the VLs. Each plane contains  $4096 \times 8192$  words.

represent one plane (odd blocks), the rightmost plots represent the second plane (even blocks). The top plots represent the total number of word errors per column while the bottom plots are similar the previous ones, but they do not display the columns which suffered too many word errors (the threshold was arbitrarily set to 64), allowing filtering the vertical lines of errors from smaller clusters. Thanks to this filtering, it was possible to plot the memory cross-section while only considering the small clusters of errors.

Two categories of failures could be identified on the bitmaps:

**Vertical Lines (VL)** - For a large majority of plotted bitmaps, the most significant error types that appeared were VL of errors, running from the top to the bottom of the bitmap and crossing all blocks either in the left plane (even blocks) and/or in the right plane (odd blocks) ( ).

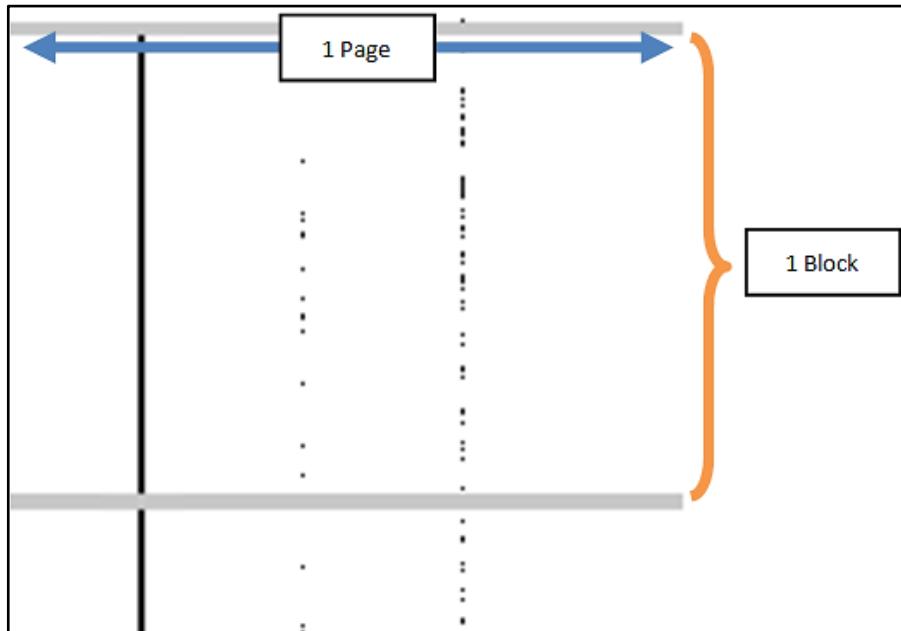


Figure 75: Close-up on a small region of a bitmap generated after static mode tests, where two types of VLs are visible (continuous and intermittent). Words are shown as black pixels if they exhibit bit errors, and as white pixels otherwise. The grey horizontal lines are used to highlight the boundaries between blocks and do not represent errors.

Several VLs may occur during one test, at any position in the planes. The threshold LET for the appearance of VLs is between 1.8 MeV.cm<sup>2</sup>/mg (N ions) and 18.5 MeV.cm<sup>2</sup>/mg (Fe ions). The vertical lines are sometimes continuous, with all words of the column exhibiting bit errors, and sometimes discontinuous, with sparse word errors along the column, as shown on Figure 75: Close-up on a small region of a bitmap generated after static mode tests, where two types of VLs are visible (continuous and intermittent). Words are shown as black pixels if they exhibit bit errors, and as white pixels otherwise. The grey horizontal lines are used to highlight the boundaries between blocks and do not represent errors. Figure 75. They were observed on every test run in static mode (solid '1', solid '0', checkerboard and anti-checkerboard data background patterns), on three specimens tested in two different test facilities (except when tested with nitrogen, 1.8 MeV.cm<sup>2</sup>/mg).

Erase operations do not suppress VLs, neither does power cycling (PC) the device - only the combination of a PC followed by an erase operation removed the errors. The VLs appeared to be dependent on the data background pattern: after beam exposition, writing and reading 'all 0' always gives VLs at the same positions, while writing and reading 'all 1' always returns another, separate set of VLs.



Two failure mechanisms are proposed to explain the occurrence of these VLs of errors:

- A stuck bit in the data buffer. During a block read operation, pages are loaded in the data buffer, one at a time, to be serially transmitted out of the memory. If one bit of the data buffer is stuck to a given value, which is the opposite of the value stored in the memory (e.g. stuck to '1' when 'all 0' is stored in the memory), at each page read, the same error will appear at the same position in the data buffer. Since the pages are represented by horizontal lines of pixels, the errors appear at the same position on each horizontal line of the bitmap, creating a VL of errors. This failure mechanism can explain the shape and extent of the VLs, but it cannot explain the fact that to stop this behavior, an erase cycle is necessary, as the erase action does not affect the data buffer.
- The control electronics of the failing bit line. If the failure is not due to the data buffer, it must be caused by a fault in the bit line control logic, since particles cannot directly upset hundreds of cells at once, in this specific arrangement. Specifically, it must involve one of the elements involved in the sensing action of the read operation. For example, in the event of a particle hit which would generate a large amount of charge, the concurrent effects of a triggered micro-latchup and charges trapped in the bit line access transistor [126] result in partial or total inhibition of the access to the bit line. All accesses to the column will be affected, generating a VL. To stop the failure condition, it is necessary to carry out both a PC, removing the micro-latchup, and the erase operation that restores the access transistor.

**Isolated MBUs and clusters of MBUs** - Besides the VLs, isolated MBUs (Multiple Bit Upsets within the same word) were also observed along with small clusters of MBUs (two to five) lined up vertically (i.e. along the same bit lines), at contiguous line addresses. No diagonal nor horizontal cluster of errors was detected. These errors occur randomly across the entire bitmap. Examples of such error types are depicted in Figure 76. An interesting characteristic of these clusters of MBUs is that the failing bits are generally the same among the words of a single cluster. After a PC, the number of erroneous bits in each word was reduced to one (SBU). This is an important point for applications, since power cycling the device before reading sensitive data could be a means to mitigate errors. These PCs do not accelerate the aging of the cell like erase actions do, and reducing to one the number of faulty bits allows the use of efficient error detection and correction techniques.



Figure 76: Close-up on error clusters taken from a bitmap generated after static mode tests, showing the shape and size of single word errors or small cluster of errors.

Isolated MBUs and clusters of MBUs occurred only for solid '0' data background tests and never for solid '1' tests. This is in line with previous results, such as those reported in [127], stating that during beam irradiation, floating gate cells are more resilient to bit flips when storing a '1' (floating gate with no charge) than when storing a '0' (charged floating gate). These errors can all be removed by an erase operation, which discharges the floating gate, whereas a PC does not; reading the device after a PC returns about the same number of word errors, with a small fluctuation. These fluctuations are due to borderline cells, i.e. cells with their floating gates at an intermediate potential after irradiation, which makes the result of a read access uncertain (intermittent errors) [126]. These small error clusters occurring along the bit line with similar error patterns can be explained by the action of a single particle hitting the memory plan. Charge sharing can also possibly occur, leading to several bits being upset in a single word. Secondary particles generated at angles may also be the cause of these vertical clusters, considering that spacers separate the columns and mitigate horizontal clusters.

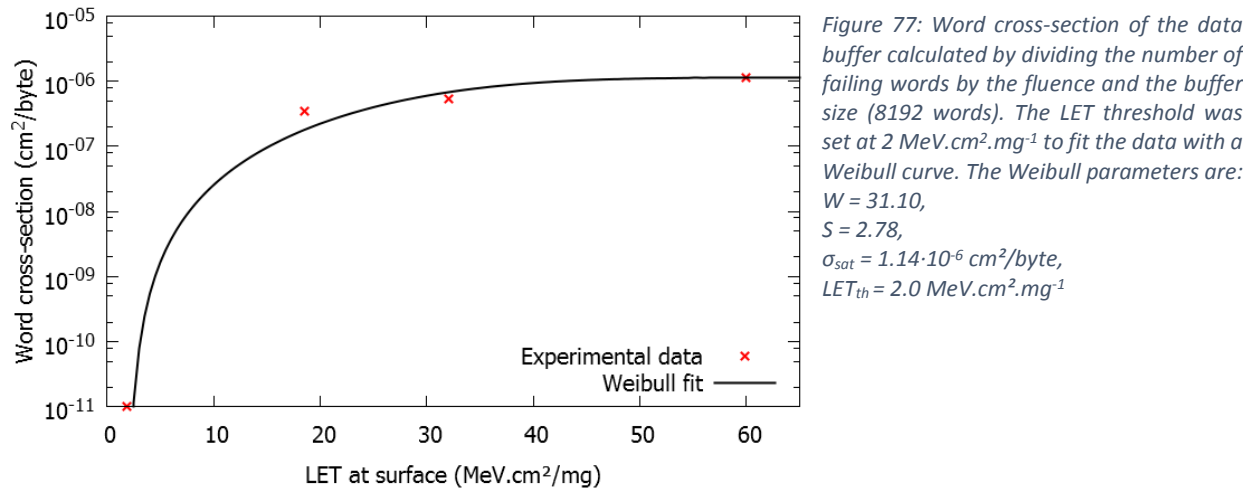
### Static buffer mode tests

Irradiation at a LET of  $1.8 \text{ MeV.cm}^2.\text{mg}^{-1}$  resulted in no buffer errors, whether using the checkerboard or solid '1' pattern. Conversely, using ions with a surface LET of  $18.5 \text{ MeV.cm}^2.\text{mg}^{-1}$  or higher, all runs returned in errors. The SEU LET threshold of the data register is somewhere between these two values.

The results from these runs can be classified into two groups:

- For some runs, few errors were detected (between 12 and 40 failing words). Generally, the failing words had only one single bit upset, although a few MBUs occurred;
- Other runs resulted in the entire data buffer (8192 words) failing. These events occurred twice out of three runs at a LET of  $18.5 \text{ MeV.cm}^2.\text{mg}^{-1}$ , and once out of three runs at  $60 \text{ MeV.cm}^2.\text{mg}^{-1}$ . When all words failed, and the buffer was loaded with a checkerboard, each word tended to have 4 bit failures, whereas when it was loaded with a solid '1' pattern, every bit of every word failed.

When considering the tests of the first group only, the word cross-section follows a Weibull curve, as depicted in Figure 77.



Similar experiments testing the data register were made by [126] on another NAND Flash component, which gave a cross-section an order of magnitude lower than evidenced by our tests.

Regarding the runs with a fully faulty buffer, the fact that most words have 4 bit errors using the checkerboard pattern, or 8 bit errors using a solid '1' pattern, suggests that during the irradiation, the control logic ruling the reset function of the data buffer produced unwanted resets and all bits were set to '0'. The datasheet of the memory indicates that a reset command to clear the data register exists, supporting this assumption. In these cases, the few words containing odd number of bit upsets are simply the result of direct SEUs occurring in the buffer after the reset; the closer the faulty reset is to the end of the irradiation, the more regular the error pattern is, with 8 bit flips for solid '1' data background and 4 bit flips for checkerboard background.

### 3) Conclusion

This study investigated the heavy-ion response of an SLC NAND flash memory in static mode. The observed errors can be classified into three groups: vertical lines (VLs) of errors (continuous or discontinuous), small vertical clusters of word errors, and single word errors. The VLs most likely occur in the bit line control

circuitry due to latch-up or stuck bit phenomena, while the other two types of errors are due to direct ionization of the memory cells. Static tests of the data buffers allowed the determination of their sensitivity, as well as the detection of unwanted reset events. The identification of these different failure modes permitted to optimize the test program of the MTCube payload.

#### F. Single-Event Latch-ups in an MRAM

Similarly to FRAMs, Magnetoresistive Random-Access Memories, or MRAMs, are an emerging type of non-volatile memory devices. This technology has the potential to bring together the endurance, performance and low power consumption of SRAMs with the low cost and high density of flash memories. MRAM cells are based on magnetic tunnel junctions, which are immune to SEEs and TID effects (see Chapter 3). However, as is the case with the FRAM previously discussed in Section D, the periphery of these circuits is implemented in CMOS and is sensitive to radiation.

A 3D component (several devices stacked in a single package) based on a toggle-MRAM device from Everspin Technologies (see Chapter 6) was selected to be flown on the RES experiment. The standalone MRAM device was the subject of multiple radiation test campaigns during the development of the payload, and was found to be prone to suffering from Single-Event Latch-ups (SELS, see Chap 5). The findings of these test campaigns have not yet been published, and will be briefly summarized in this section.

Seven devices from three different manufacturing lots were irradiated over the course of five campaigns at RADEF and GANIL, with ions ranging from nitrogen to xenon, in static and dynamic modes. A summary of the beams used in this study is available in Table 8. According to the MRAM datasheet, the maximum supply current at  $V_{DD}=3.6$  V is 68 mA during read mode, and 180 mA in write mode. These values are influenced by the operating conditions, though, and at the frequency used during our tests (7 FPGA clock cycles at 50 MHz, or 140 ns per read cycle) and with a bias voltage of 3.3 V, the typical supply current level was 4.3 mA in standby, and 11 mA in dynamic stress tests. However, at power-up, the device briefly sinks several tens of mA; to ensure proper device operation, the compliance level of the delatcher board was set at 180 mA during the MRAM SEL tests.

While none of the DUTs were sensitive to nitrogen (at any angle) or to neon at normal incidence (LET 3.6 MeV.cm<sup>2</sup>.mg<sup>-1</sup>), SELs were observed with neon at 45° (LET 5.1 MeV.cm<sup>2</sup>.mg<sup>-1</sup>) and with all ions yielding a greater LET. The MRAM's threshold LET for SEL occurrence is somewhere between these two values.

Test campaign	Ion	Energy (MeV)	Angles (degrees)	Effective LET (@ surface) (MeV/(mg/cm2))	Range (μm)
GANIL	Xe	3.4 to 46.6	0	64.3 to 26.8	37 to 700
RADEF	N	139	0 to 45	1.8 to 2.5	202
	Ne	186	0 to 45	3.6 to 5.1	146
	Ar	372	0 to 50	10.1 to 1.6	118
	Fe	523	0 to 45	18.5 to 26.2	97
	Kr	768	0	32.1	94
	Xe	1217	0	60.0	89

Table 8: Summary of the beams used for MRAM SEL characterization.

The MRAM's supply current was affected by events of two types:

- “Current excursions”, which were only observed in static mode. During these events, the DUT’s supply current abruptly increases a few milliamps above its typical idle value (4.3 mA) and remains constant. After a few seconds to a few minutes, the DUT recovers spontaneously (sometimes while still under irradiation) and the supply current returns to its initial value (Figure 78).

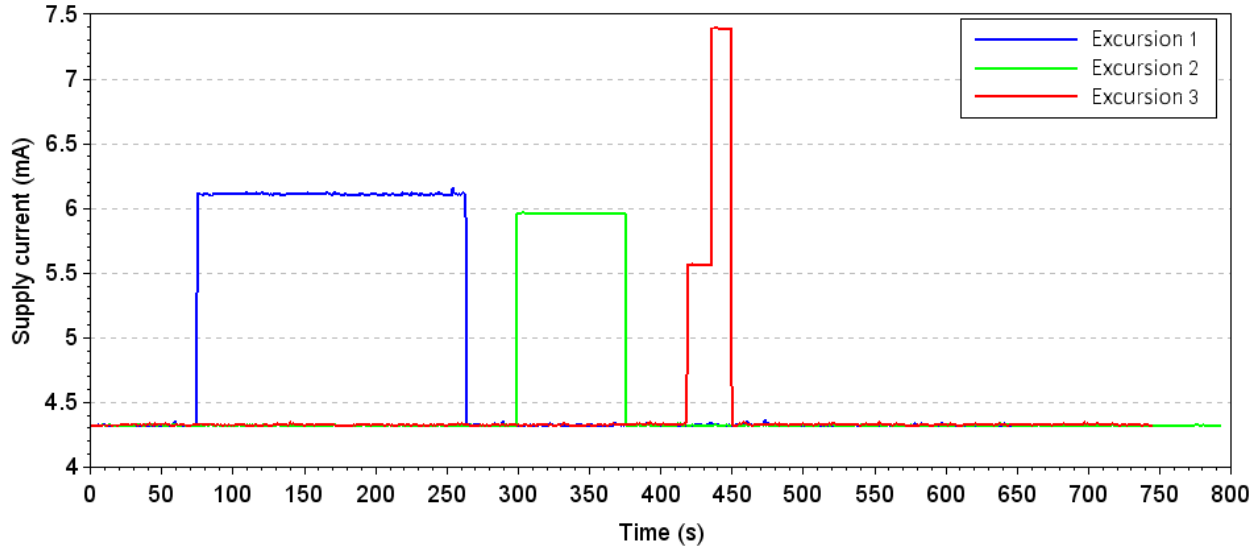


Figure 78: Examples of supply current fluctuations during current excursions. All the data was gathered on the same DUT, during static irradiation with argon ions at an angle of 0° (curve #1) and 45° (curves #2 and #3). The beam flux was about  $10^4$  counts.s<sup>-1</sup> at the DUT surface.

- SELs, which were observed in both static and dynamic modes. During SELs, the current increases abruptly by a few tens to a few hundreds of milliamps; from then on, the DUT never recovers from the condition until power is cut off. Very often, the supply current keeps increasing in successive steps of a few tens to a few hundred milliamps, until the DUT is destroyed by thermal runaway, or the power supply reaches its compliance value (see Figure 79).

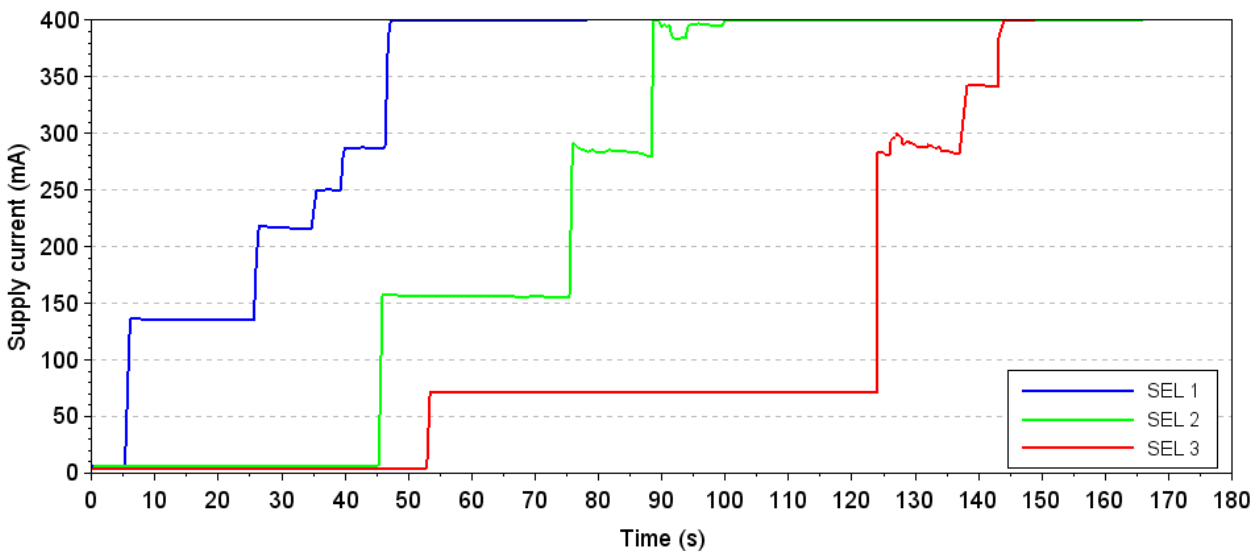


Figure 79: Examples of supply current fluctuations during SELs. The data was gathered on the same DUT for curves #1 and #2, and on a second DUT for curve #3, during static irradiation with iron ions at a normal incidence. The beam flux at the DUT surface was about  $1.5 \cdot 10^4$  counts.s<sup>-1</sup> for curves #1 and #2, and about  $10^3$  counts.s<sup>-1</sup> for curve #3. The compliance level of the power supply used to power the DUTs was always set at 400 mA.

The cause for the observed current excursions could be logic conflicts (e.g. bus contention).

MRAM SEL currents have been observed above 800 mA for 60 s, and up to 1 A for 10s, without causing any noticeable damage, idle current increase or data corruption in the DUT. (It must be noted that at these current levels, the voltage drop across the DUT power cables was very significant, but was not measured. Hence, the bias voltage of the DUT during these SEL events is not known.)

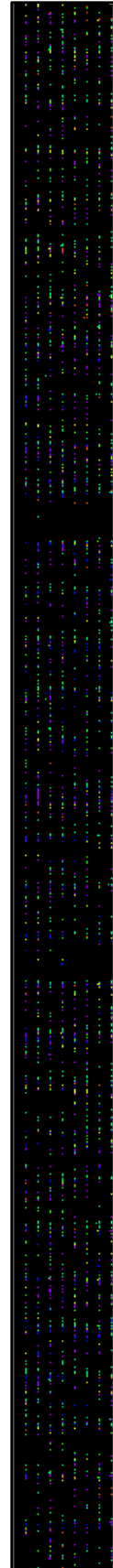
Conversely, one 400 mA SEL event has been found to cause permanent damage in one of the DUTs irradiated with iron at normal incidence. A zoom-in of a logical bitmap from a blank test (no irradiation) carried out just after this hard SEL is available on Figure 80 (MRAM bitmaps are read like an FRAM bitmap; see Section D). Two such regions were visible on the whole bitmap (which cannot be clearly displayed entirely, at 16 million pixels), which means that a region of the array containing 16,384 words, representing 131,072 bits, suffered permanent damage because of the SEL. All these words suffer from intermittent failures on their most significant bit.

Some memory devices – mostly SRAMs - store bits of similar weight together, in dedicated regions of the die; this architecture helps mitigate MBUs [128]. The failure visible on Figure 80 could be explained by e.g. an SEL damaging a read element common to all the cells of a 16,384-bit memory block containing the MSBs of 16,384 words. However, the author does not know whether the MRAM uses this architecture, and this could not be determined from photographs of the die.

Another possible explanation could be the depolarization of the free layer of the MTJ [129] and/or other elements of the affected cells by the magnetic fields generated by the SEL currents. The intense SEL currents (up to several hundred milliamps), which are generated within the die, close to the memory cells, can generate considerable magnetic fields. Theoretically, a pristine MRAM device – benefitting from its built-in magnetic shield – can be upset by a magnetic field of 8000 A/m [130], which corresponds to the field generated by a 400 mA current at a distance of 8  $\mu\text{m}$  [131]. In the present case, however, the devices were delidded, which means that their magnetic shielding layer was removed. Without magnetic shielding, it is probable that a 400 mA current would generate a magnetic field high enough to upset the configuration of the surrounding cells up to a much greater distance.

If the free layer loses its polarization, the information stored in the cell is lost, but the cell can retain functionality. If the fixed layer loses its reference magnetic polarization, the resistivity of the MTJ changes, and subsequent read operations can return either permanent or intermittent errors, depending on the degraded resistivity. The architecture of the MTJ, and the sequence of current pulses to be sent in the bit and word lines during write operations are optimized to change the magnetic polarization of the free layer, not that of the fixed layer. Finally, if the properties of the mu-metal cladding of the bit and word lines are affected by exposure to strong magnetic fields, the fields generated by current pulses passing in these lines will be modified, and the associated cells can lose functionality [132]. These last two

*Figure 80: Zoom-in on a portion of an MRAM bitmap. The data was collected during a blank dynamic stress test (no irradiation) performed after the DUT suffered from a 400 mA hard SEL. The MRAM is operated in 8-bit mode: each line of this bitmap represents 8 words of 8 bits each (64 pixels total).*



hypotheses could explain why subsequent write operations cannot restore the functionality of the affected cells.

In multiple instances, during SELs, as the supply current of the DUT reached new steps (see examples on Figure 79), simultaneous increasing steps were observed on the supply current of the DSSB driving the MRAM. The DSSB is biased at 5 V, and its supply current increased from 145 mA before the test, up to 244 mA during the SEL. This is an indication that in this condition, the MRAM can sink high currents from the peripherals connected to its address, data and control pins (the DSSB was not connected to the DUT's power supply pins). This may be a side effect of the lower bias voltage of the DUT during SELs, due to the high voltage drop across the power cables.

The supply current levels that this device is capable of sustaining during SELs, and the fact that it can sink high currents from its I/O and control pins, raise the question of the survivability of the surrounding electronics. Electronics boards using RAMs are not typically designed with the requirement to safely deliver ampere-level supply currents to this type of component. Hence, designs using the MRAM in a radiation environment including particles with LETs greater than  $3.6 \text{ MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ , neutrons, or high-energy protons, must implement latch-up protection solutions, to protect both the MRAM and the surrounding components.

## Chapter VIII – Summary

This thesis presented the main findings of a four-year investigation into the single-event effects (SEEs) of atmospheric and space radiation on memory components. Several different memory technologies were considered in this study, including Static Random-Access Memory (SRAM), Ferroelectric Random-Access Memory (FRAM), Magnetoresistive Random-Access Memory (MRAM) and flash. The devices were irradiated with a wide variety of particle beams, in static and dynamic mode, using several different testing algorithms, and their main failure modes were identified.

For some devices, such as the SRAM65, the main failure mode is memory cell upset through direct ionization (Single-Event Upset). When exposed to particle radiation, these devices quickly accumulate numerous, relatively small clusters of errors scattered across their memory array [101]. The size of the error clusters is a function of the LET of the incoming particle. These characteristics make SRAM devices suitable for use as radiation monitors [133], and they have already been used in dosimetry applications [134]–[136]. Such errors can be effectively mitigated at the component level, using software techniques such as error-correcting codes [137], [138], or design-level solutions such as adding elements to the base 6-transistor SRAM cell [119] or using dual-interlocked memory cells (DICE) [139].

In other devices, such as the MRAM and FRAM, the memory cells are implemented using inherently radiation-hard technology. The main single-event failure modes of these memories are caused by either Single-Event Latch-ups (SELs) or upsets and transients in the CMOS peripheral circuitry, which lead to a variety of single-event functional interrupts (SEFIs) and cause indirect data corruption. These fault conditions may disappear spontaneously, and can be mitigated by power cycling [114]. While these components are generally very resilient to SEEs while off-power and in standby mode, the large-scale data corruption generated by SEFIs cannot be efficiently mitigated at the component level. For critical applications in radiative environments, these components require the implementation of additional mitigation solutions, such as circuit-level triple modular redundancy (TMR) [140].

Finally, some components – such as the SRAM90 and the flash memory - can suffer both from direct cell upsets, and from indirect data corruption by fault conditions in the periphery [99]. For these devices, the large-scale failures induced by SEFIs represent the most serious failure modes, hence their use in critical applications also requires robust fault mitigation techniques such as TMR.

This study underlined the importance of using appropriate data processing and visualization tools to understand the effects of radiation on memory components. Even when the address scrambling and bit scrambling schemes of the devices were unknown (FRAM, MRAM, flash), logical bitmaps were a key resource in understanding the failure mechanisms at play.

The failure mode analysis of these devices (SRAM 90, SRAM65, FRAM, MRAM and flash) supported the development of the Radiation Effects Study experiment (RES), a CubeSat payload developed by LIRMM for on-orbit irradiation and validation of ground testing data [121]. RES is scheduled to launch in 2018 aboard MTCube (Memory Test CubeSat), a picosatellite developed by the University of Montpellier. The radiation test data and failure mode analysis allowed the prediction of on-orbit failure rates [122], and the optimization of the payload’s test program – ensuring that the devices are exposed to the space environment in the most interesting conditions, that appropriate algorithms are used for dynamic testing, that large-scale failures are handled appropriately, and that the devices do not accumulate errors uncontrollably.

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## Annex I

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# Single-Event Effects in the Peripheral Circuitry of a Commercial Ferroelectric Random-Access Memory

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**Abstract** – This study identifies the failure modes of a commercial 130 nm ferroelectric random-access memory (FRAM). The devices were irradiated with heavy-ion and pulsed focused X-ray beams. Various failure modes are observed, which generate characteristic error patterns, affecting isolated bits, words, groups of pages, and sometimes entire regions of the memory array. The underlying mechanisms are discussed.

**Index Terms**— Single-Event Effect, Single-Event Upset, SEFI, FRAM, X-ray, heavy ion, static test, dynamic test

## I. INTRODUCTION

**F**ERROELECTRIC Random-Access Memories (FRAMs) are a type of memory device, where the binary

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information is stored in the electric polarity of minute ferroelectric capacitors. When subjected to a sufficient electric field, the ferroelectric material retains electric polarization, until a sufficiently high reverse electric bias is applied. This bistable characteristic makes FRAM memory cells capable of retaining information for extended periods of time, even at high temperatures [1], [2]. This property makes FRAM interesting as an all-purpose technology, in some instances capable of replacing both traditional non-volatile storage memory (i.e. flash) as well as fast, volatile working memories such as static and dynamic random-access memories (SRAMs and DRAMs). Another advantage of this technology is its resilience to radiation. FRAM memory cells exhibit resilience up to total ionizing dose (TID) levels in the Mrad range (limited by the TID response of the access transistor) [3], [4], and are immune to single-event effects (SEEs) [5], [6].

Nevertheless, besides the memory array, the peripheral circuitry of FRAMs is implemented with traditional complementary metal-oxide-semiconductor (CMOS) technology, and hence it can potentially suffer the same kind of radiation-induced effects that are known to affect CMOS circuits. In particular, CMOS buffers and registers can suffer from single-event upsets (SEUs), which in turn can lead to temporary read/write errors, and even to single-event functional interrupts (SEFIs) of the device. FRAM devices are thus not necessarily radiation-hard, and their radiation sensitivity must be studied before they can be considered safe for use in a radiative environment.

The present study aims at further investigating the radiation-related faults that are due to failures in the peripheral circuits of an FRAM. The chosen device is the FM22L16, a 4 Mbit parallel FRAM from Cypress Semiconductor (previously manufactured by Ramtron Intl.). This component has the largest memory capacity available on the FRAM market. It has been the object of several test campaigns focusing on dose effects as well as SEEs, when exposed to heavy-ion irradiation. Different types of SEEs have been identified from the test data, and their fault mechanisms have been investigated using a pulsed focused X-ray beam. Lastly, the impact of these faults on the device's failure rate is discussed.

## II. EXPERIMENTAL SETUP

The FM22L16 is organized following a two-transistor, two-capacitors per bit architecture (2T2C), and was set in a 16-bit configuration. The FRAM array is organized in 8 blocks, each having 8192 pages, each holding 4 words of 16 bits. Data from five specimens have been used for these

Facility	DUT	Test particle	Angle (Degrees)	Energy	Linear Energy Transfer (MeV.cm <sup>2</sup> .mg <sup>-1</sup> )	Flux (cm <sup>2</sup> .s <sup>-1</sup> )	Total fluence (cm <sup>-2</sup> )
GANIL	#1	Heavy ions (Xe)	0	3.4 MeV/u, 13.2 MeV/u	64.3, 50.2	4.0·10 <sup>2</sup> to 7.0·10 <sup>4</sup>	1.70·10 <sup>6</sup>
RADEF	#2	Heavy ions (Kr, Xe)	0	9.3 MeV/u	32.1, 60.0	1.0·10 <sup>3</sup> to 6.5·10 <sup>3</sup>	1.37·10 <sup>7</sup>
RADEF	#3	Heavy ions (N, Fe, Xe)	0 to 30	9.3 MeV/u	1.8 to 69.3	5.0·10 <sup>3</sup> to 3.8·10 <sup>4</sup>	2.44·10 <sup>8</sup>
RADEF	#4	Heavy ions (Ne, Ar)	0 to 50	9.3 MeV/u	3.6 to 15.7	1.0·10 <sup>4</sup> to 1.8·10 <sup>4</sup>	1.01·10 <sup>8</sup>
APS	#5	Pulsed, focused X-rays	0	8 keV, 87pJ/pulse	37 (equivalent LET)	0.91	3.00·10 <sup>8</sup>

Table 2: Summary of the irradiations performed on the DUTs.

experiments; DUTs #1, 2 and 3 are from the same lot, while DUT #4 and DUT #5 come from a second and third lot.

DUT #1 was irradiated with a xenon beam at the Grand Accélérateur National d'Ions Lourds (GANIL, Caen, France), and DUT #2, #3 and #4 were irradiated with several heavy ion species at the Radiation Effects Facility (RADEF, University of Jyväskylä, Finland). In these tests, the DUTs were irradiated as a whole, as the beam profile was wider than the die.

Finally, DUT #5 was irradiated with pulsed focused X-rays, using beamline 20-ID-B at the Advanced Photon Source (APS) (Argonne National Laboratory, Chicago, IL, USA). The X-ray pulses delivered by the beam have a 100 ps full width at half maximum (FWHM) duration and a 1.77 μm \* 1.81 μm FWHM spot size. The X-ray energy was set at 8 keV; the attenuation lengths for the most common materials used in IC manufacturing at this photon energy are presented in Table 1. The open-top DUT has about 5 μm of interconnecting and passivation layers above the active silicon region [7]. We can estimate the attenuation caused by these layers to be minor, since they are mainly composed of SiO<sub>2</sub>, Al and Cu. Denser materials such as Sn and W are typically used only for the lowest, thinnest interconnect

Material	Density (g.cm <sup>-3</sup> )	α (μm)
Si	2.33	69.6
Si <sub>3</sub> N <sub>4</sub>	3.44	72.9
SiO <sub>2</sub>	2.2	130.4
Al	2.7	77.6
Sn	7.3	5.5
Cu	9.0	21.9
W	19.3	3.1
TaN	14.3	4.67

layers and connecting plugs, in small amounts, while TaN is used only as a thin barrier layer between Cu and insulators.

Table 1: Attenuation lengths for 8 keV photons in materials commonly used in IC manufacturing [8].

Throughout this campaign, the total pulse energy at the DUT surface was 87 pJ. In [9], a method has been developed to correlate the transients resulting from the collection of charge carriers generated by pulsed X-rays (using the same APS beam line) and heavy ions.

Using the equivalence model described in [9], we obtain:

$$LET_{eq} = \frac{1}{\alpha} E_{pulse} (bE_{pulse} + c)$$

$$LET_{eq} = \frac{1}{0.172} \times 87 \times (1.16 \times 10^{-4} \times 87 + 7.40 \times 10^{-2})$$

$$LET_{eq} = 43 \text{ MeV} \cdot \text{cm}^2 \cdot \text{mg}^{-1}$$

i.e. an X-ray equivalent LET of 43 MeV.cm<sup>2</sup>.mg<sup>-1</sup> at the DUT surface. In the following discussion, we assume an overlayer profile of 1.5 μm of Al, 1.5 μm of Cu and 3 μm of SiO<sub>2</sub>; this results in about 11% pulse energy absorption between the DUT surface and the active silicon region [8]. The formula from [9] then predicts a 37 MeV.cm<sup>2</sup>.mg<sup>-1</sup> equivalent LET at the sensitive volume depth.

The attenuation length in silicon is so large (69.6 μm) compared to the typical dimensions of logic gates and register cells (a few square micrometers) that for our purposes, we can consider the beam unattenuated once it reaches the silicon, generating charge carriers in a long vertical column.

Several regions of the die have been selectively irradiated, to identify the failure modes triggered by specific circuits. these regions included either memory cells or parts of the central spine (a region of the die containing peripheral circuitry, running across the memory array).

The irradiations performed on the DUTs are summarized in Table 2.

All five DUTs were tested in both *static* and *dynamic* modes, with an FPGA-based memory controller developed in-house. In static mode, data is written to the memory, which is subsequently irradiated; during irradiation, the peripheral circuits are idle. The data is read back after the irradiation and checked for errors. In dynamic mode, the memory controller continuously performs March test algorithms on the DUT. A March algorithm includes several elements, and each element consists in one or more read and/or write operation(s). During execution, the first element is applied to each address in the array, one after the other. Then, the next element is performed on each address as well, and so on, until all elements have been applied. The whole process repeats indefinitely until the user stops the test run. Table 3 summarizes the March algorithms most commonly used during our tests; parentheses separate elements, commas

Name	Elements and operations
<b>Dynamic Stress</b>	{↑(r1,w0,r0,r0,r0,r0); ↑(r0,w1,r1,r1,r1,r1); ↑(r1,w0,r0,r0,r0,r0); ↓(r0,w1,r1,r1,r1,r1); ↓(r1,w0,r0,r0,r0,r0); ↑(r0,w1,r1,r1,r1,r1)}
<b>March C-</b>	{↑(w0);↑(r0,w1);(r1,w0); ↓(r0,w1);↓(r1,w0);↑(r0)}
<b>Mats+</b>	{↑(w0);↑(r0w1);↓(r1w0)}
<b>mMats+</b>	{↑(r0w1);↑(r1w0)}
<b>Dynamic Classic</b>	{↑(w0);↑(r0);↑(w1);↑(r1)}

Table 3: details of the dynamic March test algorithms.

separate operations, and arrows indicate the direction in which the address space is scanned by the element (increasing or decreasing addresses). Ref. [10] discusses some of these test algorithms in detail.

Dynamic tests were sometimes carried out in a *natural order* (the algorithm moved from address to address by simply increasing or decreasing the address vector), and sometimes in other, more complex modes. The addressing order can be determined in a pseudorandom mode with a Linear Feedback Shift Register (LFSR), or using a Gray code (one bit toggling at every address change) or an anti-Gray code (every other address is complemented so that all bits but one toggle at every address change). This allowed different levels of stress to be induced on the device's periphery (in particular on the address decoders and registers).

### III. DATA PROCESSING

The readback data was processed to generate *logical bitmaps*, which are images where every pixel represents a memory cell. If the cell has suffered no upset during the test, the pixel is black; otherwise it is colored. On the logical bitmaps, the words are arranged as a function of their logical address: the four words of the first page (addresses 0x0000 to 0x0003) are displayed next to each other (1x64 pixels), then the next four words (next page) below, and so on. The resulting 64\*262,144 pixels image is rearranged as a square image for ease of display, with the first band on the left edge and the last band on the right edge. These logical bitmaps help the identification of the fault mechanisms: neighboring words have closely related addresses (their addresses share many identical bits), and so are likely to share peripheral resources (higher-level address decoders, buffers, bit/word lines, etc.).

When the tests were not carried out in a natural order, the data were also arranged as *chronological bitmaps*, on which the words are placed in the order of access during the test. On chronological bitmaps, it is easy to identify SEFIs, which generate bursts of errors, because they appear as coherent colored blocks.

For static tests and dynamic tests carried out in a natural order, the logical and chronological bitmaps are equivalent.

All bitmaps only display one entry per word (16 pixels per 16-bit word). This means that on bitmaps from dynamic test data, each pixel contains the information from all the successive read operations performed on the corresponding cell. If a pixel is colored, it means that it suffered at least one upset during the test, but it is not possible to tell how many upsets occurred from the bitmap.

Horizontal divisions (every 256 lines) and vertical divisions (64 columns/1 page wide) are displayed on the bitmaps to ease their interpretation. Separation lines divide a bitmap in 256 bitmap *sectors*; the height of these sectors matches the height of some error cluster types (e.g. type 4; see Figure 3).

The color code used on the bitmaps is used to visually associate errors which were detected on the same read cycle.

## IV. EXPERIMENTAL RESULTS

The data presented in this section originates exclusively from test runs where no Single-Event Latch-up (SEL) occurred.

When irradiated with xenon ions (LET of 60 MeV.cm<sup>2</sup>.mg<sup>-1</sup>) while not being powered, DUT#2 suffered no data corruption, which confirms that the FRAM memory cell itself is immune to SEE when not biased. The memory cells of DUT #5 did not suffer any upset, either in static or dynamic mode, when irradiated under bias with pulsed X-rays. Using this data and the conclusions of study [6], which was done on a closely related device from the same manufacturer, we can assume that the FRAM cells are immune to SEE. For the rest of this study, we will then assume that the observed SEE originate from the device's peripheral circuitry.

Figures 1 and 2 exhibit logical/chronological bitmaps from the results of two dynamic heavy-ion irradiation tests, on which different failure types can be observed. They can be classified into several categories, which have been numbered by increasing order of importance:

-Type 1 (Figure 1): 1-bit failures. These events can be isolated (type 1a), but sometimes several 1-bit failures can occur at different times at *related* addresses (sharing many bits) or within the same page (type 1b). Type 1 events were observed on all test campaigns, during both static and dynamic tests.

-Type 2 (Figure 1): several bits in one word are upset at once. The word is either partially corrupted (type 2a) or completely corrupted (type 2b). Type 2 events were observed on all test campaigns, during both static and dynamic tests.

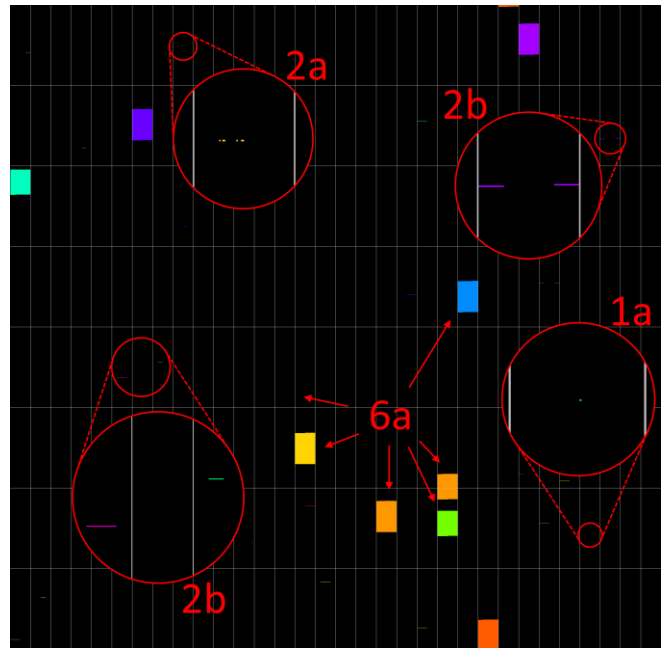


Figure 1: Logical/chronological bitmap obtained from an mMats+ test with xenon (LET 64.3 MeV.cm<sup>2</sup>.mg<sup>-1</sup>) on DUT #1, exhibiting SEE types 1a, 2a, 2b and 6a.

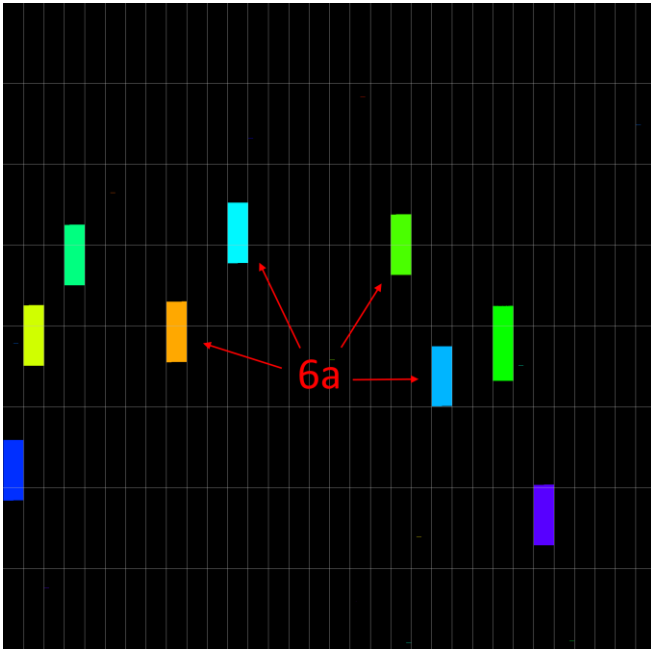


Figure 2: Logical/chronological bitmap obtained from a Dynamic Classic test with xenon (LET 60 MeV.cm<sup>2</sup>.mg<sup>-1</sup>) on DUT #1, showing SEE type 6a for comparison with Fig.1.

-Type 3 (Figure 3): several pages, which have the same *page number* (appear at the same height within their logical bitmap sectors) exhibit large numbers of upsets affecting several words. Type 3 errors were only observed on heavy-ion campaigns, and only on dynamic tests.

-Type 4 (Figure 3): one particular bit of every page within a logic sector suffers either intermittent errors (type 4a) or continuous errors (type 4b), resulting in an interrupted or continuous vertical line on the logical bitmap, respectively. In addition, sparse single-bit upsets (SBUs) may occur randomly within the affected sector. Type 4 events were observed on all test campaigns, mostly on dynamic tests.

-Type 5: the chronological bitmap on display on Figure 4 was gathered during an anti-Gray Dynamic Stress test on DUT #4. It exhibits, among type 1 and 2 events, two small blocks of errors in the top left corner; each block is made of 37 completely upset words. A closer examination of the data logs reveals that each of these 76 addresses actually returned errors on several occasions, during two consecutive element scans of the Dynamic stress algorithm. During the first element scan, after the w0 operation, the five consecutive r0 operations all failed on each of these addresses; then, on the next element scan, the first operation, r0, failed on all these addresses. Subsequent accesses to these memory locations returned no errors for the rest of the test.

The logical bitmap for this test run is available on Figure 5. This figure shows how all the errors visible on the chronological bitmap in Figure 4 have closely related addresses (they are close to each other on the logical bitmap).

Type 5 failures are rare: they were only reported once, during this heavy-ion test on DUT #4.

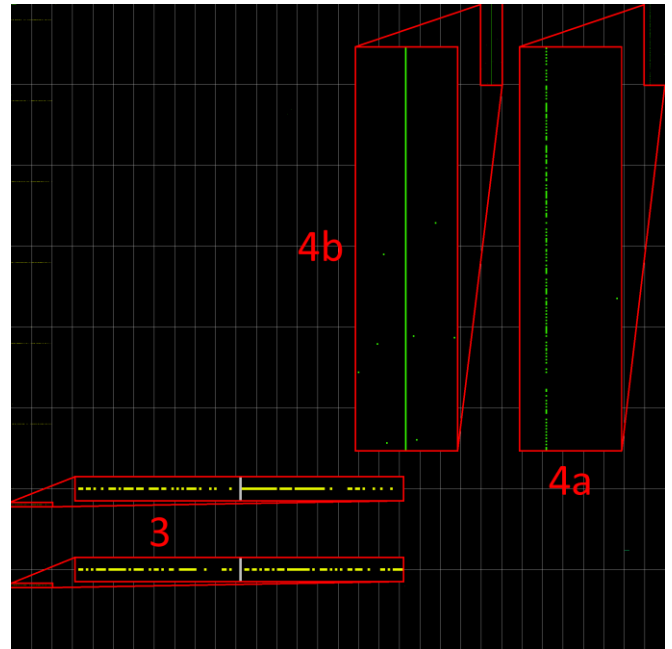


Figure 3: Logical/chronological bitmap obtained from an mMats+ test with nitrogen (LET 1.8 MeV.cm<sup>2</sup>.mg<sup>-1</sup>) on DUT #3, exhibiting SEE types 3, 4a and 4b.

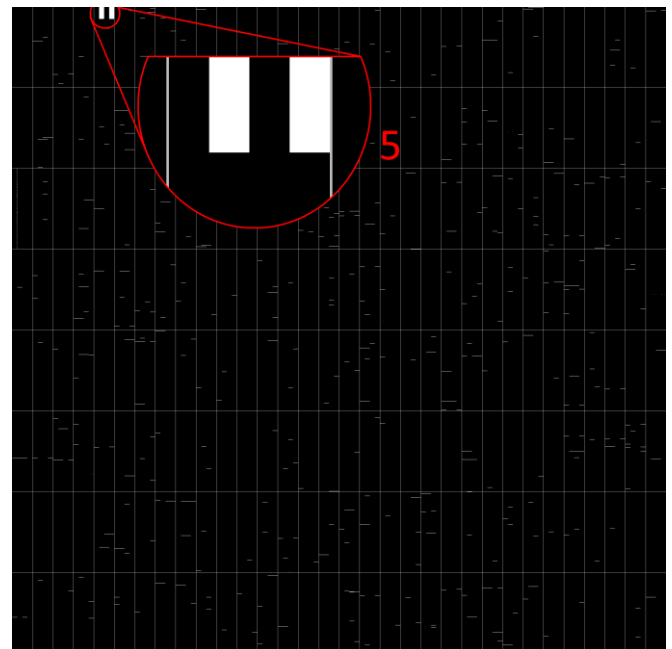


Figure 4: chronological bitmap obtained from a Dynamic Stress test with argon at 30° on DUT #4, with SEE type 5.

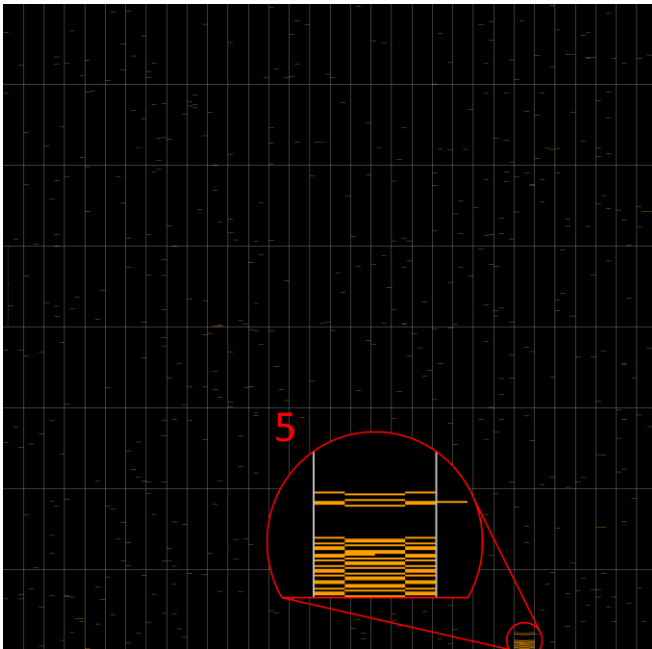


Figure 5: logical bitmap generated from the same data as that used in Figure 4; the zoom-in identifies the errors highlighted in the zoom-in of Figure 4. The complex pattern is caused by the anti-Gray addressing used in this test.

-Type 6 (Figures 1, 2 and 7): several hundred consecutively-accessed words are either completely upset (type 6a), or completely upset except for a few occasional bits (type 6b). The colored blocks appearing on Figures 1 and 2 are type 6a events. The number of words affected by type 6 failures seems to be directly influenced by the type of dynamic test, and more precisely, by the speed at which the algorithm scans across the address space. Figure 1 exhibits several type 6a events, each affecting about 350 words. The data for this figure was gathered during an mMats+ test; the elements of this algorithm contain two operations each. The data used for Figure 2 was gathered on the same DUT in exactly similar conditions, except that the test algorithm was Dynamic Classic, whose elements only contain one operation – meaning that the Dynamic Classic algorithm scans addresses faster. Figure 2 also exhibits several type 6a events, but in this case each event affects about 770 words. This correlation between algorithm scanning speed and type 6 event severity was verified on tens of different test runs; it indicates that type 6 events last for a constant amount of time (or a constant amount of I/O operations). Type 6 events were observed only on heavy-ion campaigns, dynamic tests only.

-Type 7 (Figure 6): several thousands to tens of thousands of consecutively-accessed words are affected with a high density of random upsets, generating hundreds of thousands to millions of upsets. The device may eventually recover from the condition spontaneously. The type 7 event visible on Figure 6 is the logical/chronological bitmap from a pulsed X-ray test on DUT #5 at APS. The beam scanned a region of the central peripheral spine, while a natural-order mMats+ dynamic test was performed. This type of SEFI also occurred during heavy-ion dynamic testing.

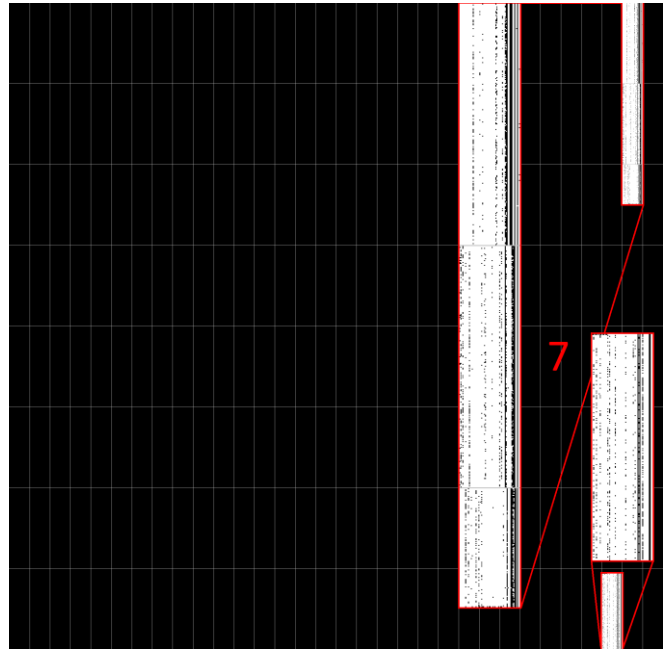


Figure 6: Logical/chronological bitmap obtained from an mMats+ pulsed X-ray test aimed at the central peripheral spine of DUT #5, exhibiting a type 7 SEE (the two bands visible in the zoom-ins belong to the same event).

-Type 8 (Figure 7): several thousands to tens of thousands of words are either entirely, or almost entirely corrupted; these words all have a few address bits in common. This is evidenced by the fact that on a logical bitmap, the errors generated by type 8 events fill up entire binary subdivisions of the bitmap – either the whole bitmap, or one half, or one or more quarters or eighths, etc. This is evident on Figure 7, where a type 8 event takes up a whole eighth of the bitmap. Since this is a logical bitmap from a natural-addressing test, it means that the type 8 event started as the third most-significant address bit toggled from 0 to 1, and ended as soon as it toggled back to 0. This type of event was recorded on all heavy-ion test campaigns, but only on dynamic tests. Type 8 events were also detected on dynamic tests where the addressing was not natural – for example, anti-Gray. This means that the errors which appear during a type 8 event are not necessarily accessed consecutively.

Several noteworthy events occurred during static heavy-ion tests on DUT #2. The memory was written with a known data pattern (every word contains the lower 16 bits of its address vector) and irradiated under bias, then read back. On a few occasions, with iron, krypton and xenon beams, the readback data contained a few words with erroneous data (type 2a errors). These errors can be considered permanent, since subsequent readbacks returned the same errors. However, they disappeared after power cycling the DUT.

Similar events occurred during a static test on DUT #5, with the X-ray beam aimed at the central spine. The device was written with a known data pattern, then irradiated. When read back after the irradiation, two type 2a events were detected at unrelated addresses. These two words were

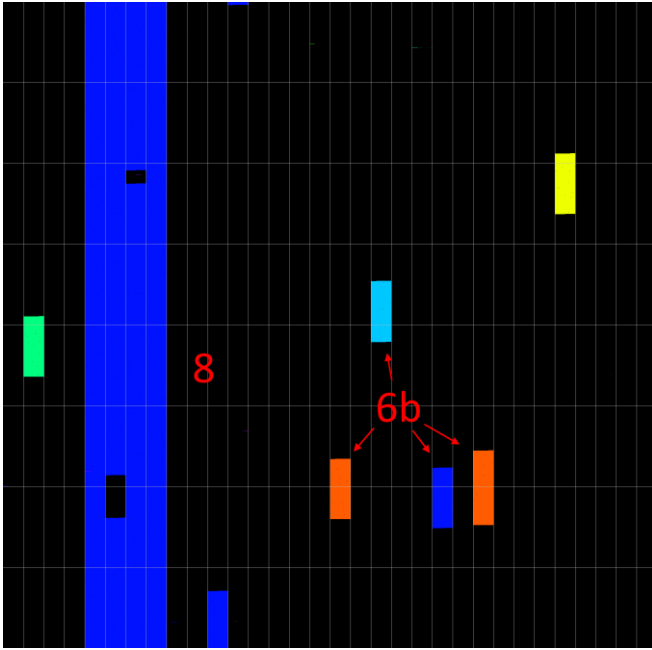


Figure 7: logical bitmap from a natural Dynamic Classic test with krypton ( $\text{LET } 32.1 \text{ MeV.cm}^2.\text{mg}^{-1}$ ) on DUT #2, exhibiting a type 8 and several type 6b events.

marked by overwriting a specific data pattern (0xABCD), after which the device was power cycled, and read back again: the readback data were correct at all addresses, except from the two words, which previously underwent a type 2a event (they did not contain 0xABCD anymore). These two words were written with 0xABCD again, the DUT was power cycled again, after which the memory performed as expected.

Table 4 gives the threshold equivalent LET and observed maximum device cross-section for each failure category, for dynamic mode and for static mode. Dashes indicate the failure category types which were not encountered in static tests.

SEFI type	Static $\text{LET}_{\text{th}}$ ( $\text{MeV.cm}^2.\text{mg}^{-1}$ )	Static max. XS ( $\text{cm}^2$ )	Dynamic $\text{LET}_{\text{th}}$ ( $\text{MeV.cm}^2.\text{mg}^{-1}$ )	Dynamic max. XS ( $\text{cm}^2$ )
1	$\leq 1.8$	$5.9 \cdot 10^{-6}$	$\leq 1.8$	$1.4 \cdot 10^{-4}$
2	$\leq 1.8$	$8.2 \cdot 10^{-6}$	$\leq 1.8$	$4 \cdot 10^{-4}$
3	-	-	$\leq 1.8$	$6 \cdot 10^{-8}$
4	$2.5 < \text{LET}_{\text{th}} \leq 3.6$	$1 \cdot 10^{-7}$	$\leq 1.8$	$1 \cdot 10^{-5}$
5	-	-	$10.1 < \text{LET}_{\text{th}} \leq 11.7$	$2 \cdot 10^{-7}$
6	-	-	$\leq 1.8$	$6.3 \cdot 10^{-5}$
7	-	-	$\leq 1.8$	$3 \cdot 10^{-7}$
8	-	-	$11.7 < \text{LET}_{\text{th}} \leq 18.5$	$2 \cdot 10^{-6}$

Table 4: Threshold equivalent LET and maximum measured cross-sections for each type of failure category, in static and in dynamic mode.

## V. DISCUSSION

These different failure modes suggest the occurrence of faults in several different elements of the peripheral circuitry.

Type 1 and 2 SEEs were detected both in static and dynamic modes, both during heavy-ion testing and X-ray periphery attacks, but never during X-ray FRAM cell attacks, thus their origin must lie in the peripheral circuitry. These events never occurred when the memory was irradiated in a powered-off state. Errors disappear after a power cycle; however, if new data are written to a corrupted word before cycling power, these data will change after the power cycling. This indicates that the element of the periphery which is upset by radiation is restored in its correct state during device power-on boot. The authors identified one potential cause of these SEE to be upsets occurring in SRAM-based redundancy registers, whose purpose is the reallocation of faulty memory elements (rows, columns, blocks) to spare elements within the memory array. Upsets in such registers will be latched and trigger errors until they are reinitialized to their correct value. These registers are always reloaded with correct values at device power-on.

Type 4 SEE: the facts that this type of event occurred during X-ray periphery testing, and that most of the errors generated occur at the same bit of the same word within their page suggest two possible fault mechanisms. The first hypothesis is an upset of a redundancy register, with the consequence of either reallocating a functional column to a spare column (thus not correctly initialized), creating a continuous 4b event; or the re-allocation of a spare column to a malfunctioning column (not supposed to be used), or the allocation of a functioning column to a malfunctioning spare (not supposed to be used), resulting in an intermittent 4a error. The second hypothesis is the occurrence of a micro-latchup event or a stuck bit in a page buffer. Such events induce metastability in the buffer cells, explaining the occurrence of seemingly random errors occurring concurrently to the “vertical lines” in the rest of the page buffer positions during type 4 events (see Figure 3).

SEE type 3: these events could have similar origins to those of type 4 events. Since the affected pages share similar page numbers, they could all be part of a single memory row which was reallocated to a spare row. Another possibility would be that an element common to these pages (e.g. a low-level address decoder) was disturbed during the test.

SEE type 5: the addresses involved in this event started returning all-corrupted words after a w0 operation. For each of these addresses, several read operations spread over two scanning cycles returned the same result, until their cells were eventually rewritten. This failure can be explained by a temporary stuck address bit. Typically, during an access to the memory, the value input on the memory’s address pins is loaded into an address buffer. If, under the effect of radiation, one or more bits from the buffer get stuck, then the requested operation will be performed at the wrong memory location. This hypothesis is supported by the chronological bitmap, which indicates that during the event, in chronological order, every other address accessed failed. This is consistent with the fact that all address bits -but one- toggle from one access to the next in anti-Gray addressing

mode: the stuck bit fault can only trigger errors on every other position accessed.

Another explanation for this event could be a failure of the write operation of the first element of the algorithm. As indicated by Figure 5, all the words involved in this event have related addresses, which means that there is a high probability that they share common read/write control circuits. It is possible that locally, the peripheral elements required for write operations were temporarily disabled by an ion strike. This hypothesis is supported by the fact that no other large group of errors is visible on the logical bitmap.

Type 7 events are large-scale functional interrupts, which do not affect an “even” amount of words (a power of 2), seemingly start and stop at random address positions, and trigger a pseudorandom output, could originate in an upset of device configuration registers, or in a micro-latch-up affecting peripheral elements. Micro-latch-up conditions have been shown to disappear spontaneously in CMOS devices, when the high voltage lines sustaining them are switched off as part of normal device activity [11].

Type 8 events are large-scale failures which affect an “even” amount of words (a power of 2). They begin and end when certain address bits toggle; since each address bit controls one level of address decoding, type 8 events must be “mapped” on the memory array. For example, the type 8 event visible on Figure 7 affected exactly one eighth of the memory array; since the memory array is organized in eight blocks, one possibility is that a radiation-induced upset in a configuration register disabled a critical element in one of the eight memory blocks – and that subsequent accesses to this memory block returned an erroneous value. Since three address bits are used to select blocks, the type 8 event started when the lowest-level block-selecting bit toggled, and ended when another block was selected at the next toggle. Possible origins for these events could be upsets in configuration registers (e.g. controlling power switches feeding memory blocks).

#### CONCLUSION

This study shows that the SEE occurring in the FM22L16 FRAM device come in several types, with different root causes, of different magnitudes and severity. The detected failure types may involve either individual bits, isolated words, groups of pages, 1-bit-wide columns, entire regions of the memory array, or a variety of SEFIs generating errors for an arbitrary duration. All these SEEs can be considered to originate in the peripheral circuitry, as also suggested by previous studies [7], [12]; possible origins for some of these failures include internal redundancy and control registers. However, experimental data show that at least some categories of SEE - notably single-word (type 2) errors - can be avoided by forcing a reset of the involved peripheral elements via power cycling the DUT before access (and possibly via putting the device out of sleep mode). This has major implications regarding the device’s radiation sensitivity, since type 2 events are by far the most frequently encountered. Many applications using the device as a storage

memory could easily implement systematic power cycling before device access as an error mitigation technique.

The results of this study suggest that hardening key elements of the peripheral circuitry of a memory device (e.g. implementing the registers with additional transistors [13] or a dual-interlocked cell architecture [14]) could effectively mitigate the most common failure modes. This would dramatically improve the failure rate of the device, at the expense of a small increase in the area of the peripheral circuitry.

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## Annex II

**A. Bosser**, V. Gupta, G. Tsiligiannis, A. Javanainen, H. Kettunen, H. Puchner, F. Saigné, A. Virtanen, F. Wrobel and L. Dilillo, "Investigation on MCU Clustering Methodologies for Cross-Section Estimation of RAMs", in *IEEE Transactions on Nuclear Science*, Vol. 62, no. 6, pp.2620-2626, 2015.

*Contribution: the author had a major role in the experiment's software and hardware development, took part in the test campaigns, and did most of the data processing and writing.*

# Investigation on MCU Clustering Methodologies for Cross-Section Estimation of RAMs

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**Abstract**—During irradiation testing of RAMs, various failure scenarios may occur which may generate different characteristic Multiple Cell Upset (MCU) error patterns. This work proposes a method based on spatial and temporal criteria to identify them.

**Index Terms**—Cluster of bit flips, dynamic test, multiple cell upset (MCU), radiation testing, RAM, SEFI, single event upset (SEU), static test.

## I. INTRODUCTION

**S**INGLE-EVENT UPSETS (SEU) are well-documented and common phenomena affecting memories of various technologies, and in particular static random-access memories

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(SRAMs), as a result of incoming radiation interacting with the component material. When an ion strikes an SRAM cell, it generates free charge carriers along its path. When collected by transistors, these carriers give rise to parasitic currents which may alter the state of the cell's inverters, and thus flip the stored bit. Several techniques have been proposed to mitigate the effect of SEUs. Error-correcting codes (ECC) [1] and dual-interlocked memory cells (DICE) [2] are among the most well-known and applied ones. These techniques have been proven to be efficient, however they present some limitations. ECC solutions make memory operation more complex by adding extra steps in the read and write processes, and both ECC and DICE solutions lead to area overhead and increase memory design complexity, which reduces their relevance for commercial purpose, especially in the latter case.

Moreover, in modern technologies, with transistor dimensions following a steady decrease, the cell density in memory arrays is increasing. This makes it more likely that the free carriers generated by impinging particles affect different neighbouring memory cells or gates at once and trigger several errors. When this phenomenon impacts the memory cell array, it is referred to as a multiple-cell upset (MCU) and introduces a significant challenge in mitigating data corruption. Current ECC solutions are capable of recovering from more than a single bit error per word (still generally no more than 2), but they are costly in terms of chip area, complexity of implementation, and may also increase the read access times [3]. For these reasons, most ECC implementations can only recover from one single upset per word, with limitations on the amount of affected words. If several bits within the same word are upset (which is referred to as a multiple-bit upset, or MBU), the error cannot be corrected and the data integrity is compromised. Further techniques have been introduced to mitigate the occurrence of MBUs, such as bit interleaving [4], which is described in the next section.

One strong motivation to acquire detailed information on the characteristics and statistics of MCUs during irradiation tests of memories is the occurrence of single-event functional interrupts (SEFIs) and single-event latch-ups (SELs) that, although caused by single particles, commonly generate large-scale events, with hundreds or thousands of bit flips per event. This means that simply calculating the memory cross-section with a raw count of bit flips may lead to misinterpreting the actual radiation response of the component, and in particular the radiation sensitivity of the memory cell array against that of the peripheral circuitry. To get a better understanding of the failure mechanisms

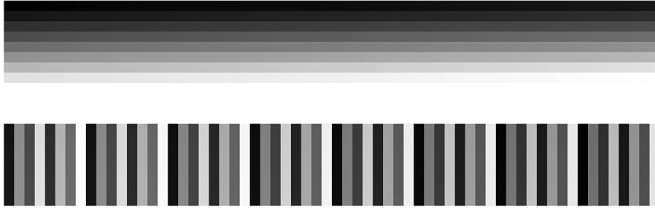


Fig. 1. On the top image is a representation of 512 consecutively-read words as they would appear on a logical bitmap: darkest words are read first. The lower image represents the same consecutively-read words, being written in scattered locations in the memory array according to the memory's address scrambling scheme. One square represents one word.

underlying the occurrence of memory errors under radiation, it is then crucial to apply effective techniques to accurately define MCUs as clusters of bit flips due to single events, as well as to calculate meaningful “clustered” single-event cross-sections. In this direction, as a follow-up to the classification of clusters made in [4], this present work proposes and evaluates clustering methodologies based on spatial and temporal criteria, for application in the post-processing of irradiation test data of actual industrial SRAMs. This methodology can also be transposed to other memory technologies, for example DRAM. To the best of our knowledge, at present there is no industry standard tool or methodology for memory radiation test data processing and cell upset clustering.

The rest of the paper is organised as follows: Section II describes the experimental setup which was used in this study. Section III reviews the experimental data and gives a description of the different categories of MCUs encountered during the tests. Section IV proposes an algorithm to automatically process test data and extract MCU statistics. Section V presents the results of this algorithm in a case study. Section VI concludes the paper.

## II. EXPERIMENTAL SETUP

The device that was chosen for this study is a commercial memory device, the CY62177EV30LL-55ZXI SRAM from Cypress Semiconductor. This memory is made of two stacked dice, and no ECC is implemented. The two-stacked dice structure has a direct impact on the distribution of errors within the memory. The physical placement of the data written to the memory array obeys an address-scrambling scheme. As can be seen on Fig. 1, a block of data being written at adjacent logical addresses in the memory will actually be written at several, separate physical locations in the memory array.

In addition, bit interleaving schemes are used to physically separate the bits belonging to the same word. This is done by placing the eight bits of a word in the same row of the memory array, keeping a constant distance of 8 bit cells between two consecutive bits (see Fig. 2).

Each irradiated memory was mounted in an open-top testing socket and driven at an operational frequency of about 15 MHz (close to the maximum frequency of 18 MHz) by a Diligent Spartan-3 field-programmable gate array (FPGA) board, on which a memory controller, based on a finite-state machine, was implemented. The FPGA was then connected via a serial

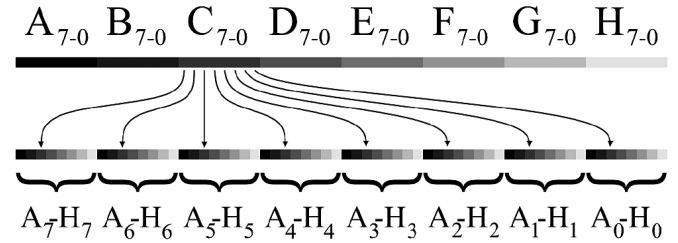


Fig. 2. Eight consecutive logical 8-bit words (top) and their physical locations according to the 8-bit interleaving scheme; each word's bits are scattered on the memory array. One square represents one bit.

link to a computer, for data storage and experiment control. In several test campaigns, the devices were exposed to proton and heavy-ion beams at the RADEF (Finland) and UCL (Belgium) facilities. The proton energies ranged from 600 keV to 55 MeV, and the heavy-ion linear energy transfer (LET) values ranged from 1.1 to 67.7 MeV · cm<sup>2</sup> · mg<sup>-1</sup>, with heavy-ion energies ranging from 3.6 to 10 MeV per nucleon. Particle fluxes and fluences were chosen in accordance to the memories' sensitivity: fluence ranged from 3.5 · 10<sup>7</sup> up to 1.5 · 10<sup>9</sup> cm<sup>-2</sup> for protons, and from 5 · 10<sup>2</sup> to 10<sup>4</sup> cm<sup>-2</sup> for the various types of heavy ions. Irradiation time varied from several seconds (when the memory was the most sensitive) to a few minutes; typically, the fluence rate was adjusted so that the tests could last a few tens of seconds.

The memories were tested both in *static* and *dynamic modes*. For the static mode testing the memories were initialised with a known data background, then irradiated for a certain time window with no access (read/write), and finally read back to detect the occurrence of bit flips. For the dynamic mode testing several algorithmic stimuli, with specific sequences of read and write accesses, were performed with the purpose of exerting specific stresses on the memory. Details of these algorithms are given in [5].

## III. EXPERIMENTAL RESULTS

To automatically generate statistics on the type and number of failure events that occurred during a test, our group has developed a C language program. It is meant to be used in data post-processing, and takes the test logs resulting from memory tests as an input. With the knowledge of the address scrambling scheme, which has been obtained from the manufacturer, the program can post-process the test logs to create images representing the locations of errors on a physical map of the memory arrays (physical bitmaps). Logical bitmaps may also be created, where the data are not sorted according to its position on the memory array, but according to its accessing order: addresses that are accessed consecutively are contiguous on the logical bitmap.

The physical bitmaps exhibit error patterns, which can be classified in different categories. Fig. 3 shows an example bitmap from a dynamic test, which gives a sense of the relative scales of these error patterns. In [4] and its references the authors identified four different types of MCU, and gave some physical and electrical explanations to their origins: type A MCUs, the most common ones, are isolated clusters of at most

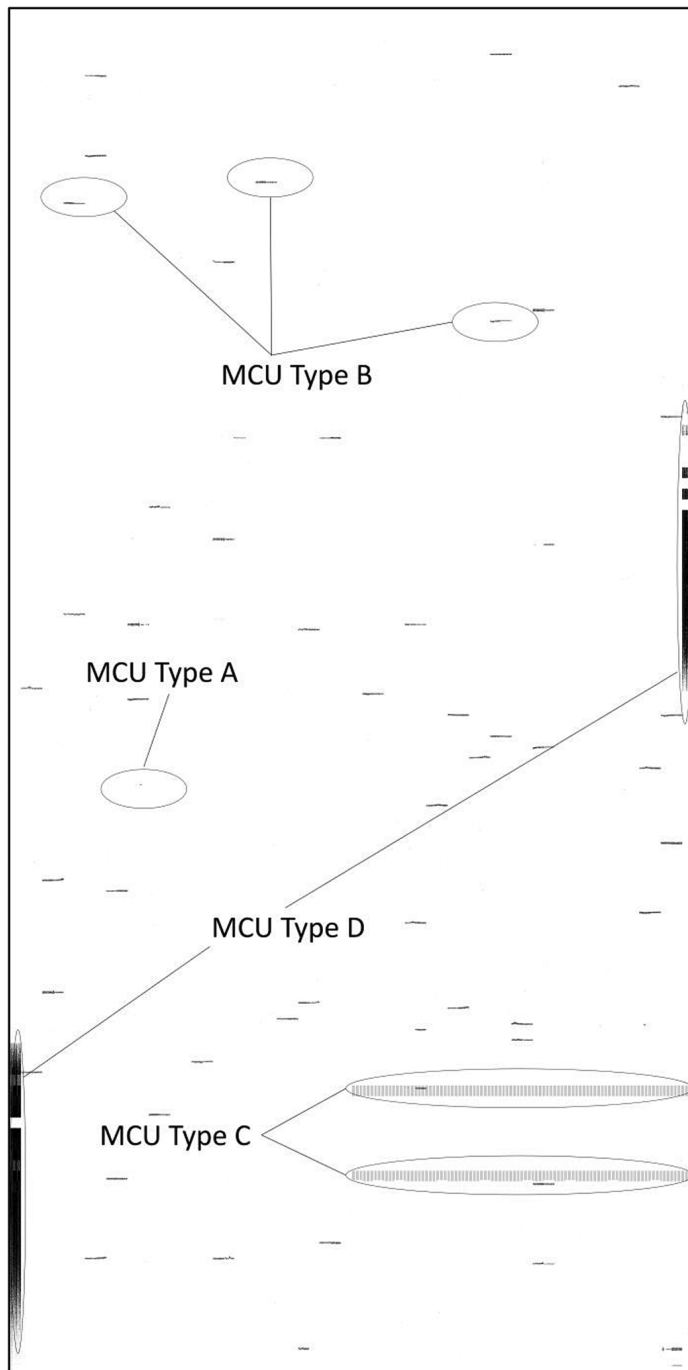


Fig. 3. example bitmap from a dynamic test, exhibiting the different kinds of MCU patterns. Type A MCUs and SEUs did occur during the test, but being relatively small they are not visible on the bitmap at this resolution. This figure has been borrowed from reference [4].

a few tens of bit flips, and they are the result of cell-inverters' instability induced by the collected charge [6][7].

Type B MCUs, also rather common, are long "horizontal" blocks of errors composed of few tens up to several hundred errors, and they are caused by micro-latch-ups limited to one or two electrical blocks delimited by tap cells within the memory cell array [8][9]. Type C MCUs comprise several possible kinds of patterns on the physical bitmaps, which depend strongly on the addressing order during the memory access. They display a sharp regularity, and comprise from thousands to tens of thousands of bit flips. However, type C events appear as contiguous

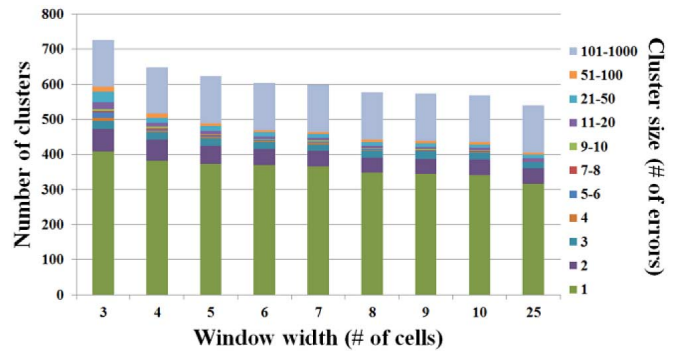


Fig. 4. Influence of the horizontal span of the physical detection window on the number of clusters and their size. The data was obtained from a dynamic test. The height of the window has a far smaller impact; hence it is not shown here.

regions on logical bitmaps. These are likely to be the result of a temporary failure (milliseconds) of the memory's I/O data buffers or synchronisation circuitry. Finally, type D MCUs are large vertical rectangles, usually located on the edges of the memory array, counting up to hundreds of thousands of errors, in a quasi-repetitive pattern of generally high error density. This last type may be the result of failures in the memory array's power switches, output buffers or synchronisation circuitry (or a combination thereof).

Bitmaps generated from dynamic test data exhibited a combination of SEU and type A, B, C and D patterns, while bitmaps generated from static test data only exhibited SEU and type A events.

As explained in [4], the data processing software used by our group has historically been based on the following algorithm: the physical bitmap was scanned across, until an upset bit was detected. Then, errors that were located within a "detection window" covering 3 bit cells in every direction (centred on the upset bit) and had been detected within 2 seconds were considered as being part of the same cluster. The process would be applied to all bits added to the cluster, until it could not be extended any further. The memory scan would then resume, ignoring previously treated errors. Lastly, a few more clustering passes were carried out to eventually merge previously generated clusters, which ought to be grouped but were left out by the first pass. This algorithm, based on empirical threshold values (3 bit cells, 2 seconds), had the advantage of being fast and easy to implement; however, with such differences in the error patterns of the A, B, C and D MCU types, it was difficult to obtain acceptable clustering results by using a single value of cell distance. As shown in Fig. 4, increasing the width parameter (horizontal distance in number of cells on the bitmap) of the detection window from 3 to 25 induced a decrease of 26% in the total number of clusters at the end of a scan, the smaller clusters being the most affected (-32% in the number of clusters of less than 100 errors).

Furthermore, this algorithm failed to sort out interweaved vertical type D and horizontal type C clusters. Because of this, direct bitmap observation of large-scale events (only a few cases w.r.t. the total amount of upsets) was so far necessary to accurately recognise the types of MCU that occurred during a test. Hence, we chose to adopt a new approach to MCU clustering in

several steps, as detailed in the next section. The software implementing the algorithm has been developed in-house and is written in the C language.

#### IV. OPTIMISING THE DETECTION ALGORITHM

In order to optimize the clustering procedure, we divided the clustering process in several steps. The focus is first set on detecting type C clusters (SEFIs), then on the remaining error clusters. This order allows a better identification of the different event types. A major component of this new clustering algorithm is the use of logical (as opposed to physical) criteria to detect SEFI events (leading to type C error clusters), which greatly improves clustering accuracy. In this present study, the authors provide specific values for the physical and temporal clustering criteria. These values have been determined to best match direct observations made on a large number of test logs and bitmaps, which have been obtained with a few different memory models which are familiar to the authors. These values may vary for other technology nodes or manufacturers, as the shape and dimensions of SEU error clusters are strongly correlated to the design of the memory and the conditions in which it is being operated. However, once identified, new criteria values can be easily introduced in the algorithm settings. What's more, by design, this algorithm can discern and isolate SEFIs-related memory upsets from general SEUs among test data from any type of memory. It has to be kept in mind that pattern recognition and interpretation is a complex problem, and that no simple algorithm can match the performance of human judgment; here, the algorithm is tuned for best accuracy in large-scale event detection, because these events are the most severe and their detection is much more important than the accurate clustering of isolated SEUs.

Our algorithm starts by reading the results of radiation tests. A database is created, containing for each corrupted word: its data value, its logical address (the relative order in which it was accessed during the test) and its physical address (its actual position on the memory array. The knowledge of the memory scrambling and interleaving schemes is necessary for this.). Then the clustering process is started, focusing first on type C clusters, and then on type D, B and A MCUs and SEUs.

*1. Detection of type C Clusters:* As previously mentioned, on physical bitmaps, type C error clusters (which only occur during dynamic testing) exhibit very regular, often complex patterns, where every bit (or almost) of every affected word displays the wrong value. Their distinctive segmented aspect is due to the bit-interleaving scheme (see Fig. 2), while their general disposition on the memory array is a function of the device's address scrambling scheme (see Fig. 1) and the addressing order used during the test. This makes the detection of these polymorphic events very difficult when using clustering algorithms based solely on physical distance criteria. However, logical bitmaps display the errors that belong to the type C cluster category as contiguous and homogeneous blocks of errors (a few small gaps, up to 7 bits wide, may occur due to bit interleaving at the ends of the cluster). An example of such a cluster is given in Fig. 5.

The reason for the two different aspects (logical and physical) of type C clusters is that they are due to SEFIs affecting the memory's I/O buffers or the address decoders. The result is



Fig. 5. Zoomed-in example of a single type C cluster, as it appears on physical (top) and logical (bottom) bitmaps.

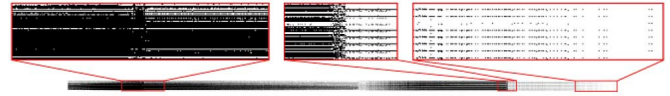


Fig. 6. Example of a type D cluster (rotated clockwise), with zoom-ins on regions of various error densities.



Fig. 7. Two examples of a type B cluster. The top example illustrates the need for a wide detection window.



Fig. 8. Several examples of type A clusters.

that for the duration of the SEFI, the memory output is set to an arbitrary and fixed value, regardless of the actual data that is actually stored in the accessed locations of the memory. This particularity makes it easier to distinguish type C errors on a logical bitmap rather than on a physical one. It is important to note that, on the logical bitmap, there is very little chance that type D MCUs (introduced above) would form large-scale coherent patterns, since they are limited to a certain physical area of the die and are not determined by the accessing order of the memory (as type C MCUs are).

Hence, a logical bitmap is created from the error database, which is then scanned in a left-to-right, line-by-line fashion. If completely upset words are detected at over 500 consecutively accessed addresses, and with gaps of only three or less addresses between them, they can be considered as forming a type C cluster. The algorithm then removes all the flipped bits corresponding to type C clusters from the error database and proceeds to the next step.

*2. Detection of Type D, B and A Clusters:* Type D clusters, which only appear during dynamic testing, are comprised of several tens of thousands of errors distributed in one column of no more than 64 bits in width, and which can span the whole height of a memory die (4096 rows). However, the error density within a type D cluster can vary tremendously (as is shown in

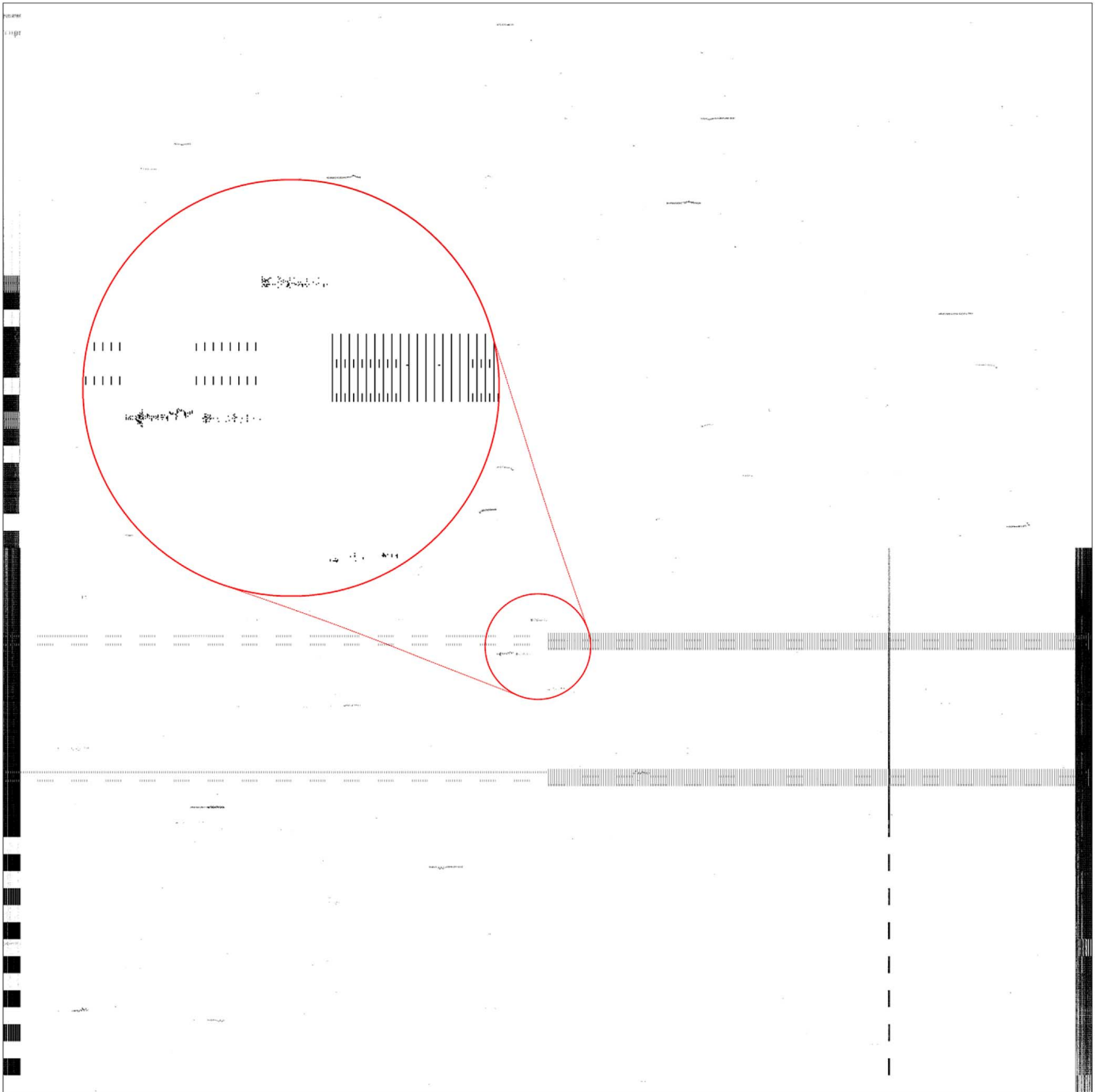


Fig. 9. dynamic test bitmap used in the present case study. A zoom-in on a region comprising type A, B and C events is provided.

Fig. 6). A major hindrance in their accurate detection is the frequent presence of very large “error-free gaps” within the clusters: entire regions 64 bits wide and sometimes over 64 bits high appear devoid of errors. This last characteristic led the first version of our algorithm to interpret the separate regions of a single type D event as separate clusters. This has so far necessitated further visual checks, which is not acceptable when processing a large amount of data.

Type B clusters are another cluster type which is exclusive to dynamic tests. Although sharing a very wide aspect ratio (up to 256 bits wide and up to 25 bits high), these clusters can differ greatly in their longitudinal distribution (see Fig. 7); while some areas may exhibit error densities close to 50%, others may

present error-free gaps extending frequently up to 10 bits. These might extend to over twenty bits, but these cases are marginal.

Type A clusters, lastly, share a generally small size and number of errors, with maximal dimensions not exceeding a couple of tens of bits in either direction; still, their shapes can vary greatly (see Fig. 8). They are the most common MCU pattern type and can be found in any type of test, either static or dynamic.

To find a compromise between processing time and clustering accuracy, the following procedure is proposed. To ensure type D events are entirely processed and detected, the detection window of this second step is set to a horizontal value of 10, and a vertical value of 67, to increase the odds of overlapping

hypothetic separate regions. Among the detected potential candidate clusters, only the ones with an error count higher than 500, and whose dimensions are comprised between 10 and 128 in width, and 30 and 4096 in height are considered as type D. On the one hand, this method has the downside of being prone to incorporate bit flips in the cluster that are not part of a type D event; on the other hand, it has the advantage of being conservative and efficiently detecting the type D MCUs in the common case where they incorporate error-free gaps. This approach is favoured because, although type D events are relatively rare, they have serious consequences in terms of error generation, which sharply increases the device's "raw" cross-section; this is why it is crucial to recognize them when they occur.

From the remaining clusters, the ones whose width is comprised between 32 and 150 cells are considered as type B. All the other clusters of at least two errors are considered as type A. Finally the detection of Single Bit Upsets (SBUs) is rather simple since they are defined as clusters that contain one single bit.

## V. CASE STUDY

To illustrate the function of our algorithm, a case study of one particular dynamic memory test result is provided. The corresponding bitmap is shown on Fig. 9. The parameters which were used were 2 seconds for the temporal criterion, and  $67 \times 10$  cells for the clustering window.

*Observations.* When the only data available from this test was the raw count of errors appearing on the test log (259620), one could only calculate the memory's error cross-section

$$\sigma_{\text{error}} = \frac{\text{error count}}{N_{\text{bits}} \cdot \text{fluence}} = \frac{259620}{16777216 \cdot 1053} = 1,5 \cdot 10^{-5} \text{ cm}^2$$

which is very high. However, the algorithm determined that the 259620 errors that occurred during the test actually originated from only 204 separate events; there were 28 isolated SEUs, 137 type A clusters, 29 type B events, 5 type C events and 3 type D events. The process of cluster recognition allows us to draw different conclusions regarding the memory's sensitivity to radiation. The memory's single-event cross-section is now

$$\sigma_{\text{event}} = \frac{\text{event count}}{N_{\text{bits}} \cdot \text{fluence}} = \frac{176}{16777216 \cdot 1053} = 1.10^{-8} \text{ cm}^2.$$

If trying to assess the failure rate of the memory, one would have assumed an average value more than three orders of magnitude too high without the clustering data. What's more important, is that almost 80% of these events have generated only one SBU or a type A cluster, which may be recovered from through software correction mechanisms. Hence, the memory's radiation sensitivity is not what it may appear at first sight. Although large-scale, critical failures might happen, these are very rare; the device failure rate is orders of magnitude lower than estimates made solely with raw bit flip counts, and in most cases, solutions can be implemented to recover from errors.

The authors of [10], who carried out studies on the single-event rates of SDRAMs, came to the same conclusion after analysing the results of laser and heavy-ion testing campaigns, as well as on-orbit SEFI rates and other on-orbit SEU rates.

TABLE I  
EFFECT OF THE ALGORITHM PARAMETERS ON THE RESULTING STATISTICS.  
IN BOLD ARE THE PARAMETERS CHOSEN IN THE PREVIOUS EXAMPLE

Detection window size	Temporal criterion	SBU	Type A	Type B	Type D
10x10	10 s	34	147	34	8
67x3	10 s	46	243	21	3
67x3	2 s	47	248	21	3
<b>67x10</b>	<b>2 s</b>	<b>29</b>	<b>137</b>	<b>30</b>	<b>3</b>
67x10	10 s	28	133	29	3
67x20	10 s	22	122	32	3

*Note.* This case study provides an opportunity to demonstrate the importance of selecting an appropriate size for the second step detection window. In the following Table I, figures are given regarding the number of SBU and type A, B and D clusters detected by the algorithm as a function of the second step detection window size and temporal criterion.

The results shown in Table I illustrate the fact that too small values for the detection window height lead to misdetecting type D events. Increasing the window width beyond 10 cells has little impact in this case, but using too small values (e.g., 3 cells) leads sparsely populated type B clusters to be improperly considered as several type A MCUs.

## VI. CONCLUSION

This paper presents a new post-processing methodology to automatically detect MCU occurrences in memory component irradiation test data and classify them in different categories. This approach utilises several steps in the analysis flow, which takes into account the different characteristics of these MCUs and provides more meaningful statistics than raw bit flip figures. It can be used to quickly pinpoint possible causes of failure when unusually high error counts are registered, and to calculate accurate on-orbit single-event rate values. As technology scaling continues, and MCUs become more and more common phenomena, such tools will be useful to scientists and engineers in radiation testing.

This methodology does not come without a few limitations. The accuracy of the clustering process may be affected if the particle fluence rate (and thereby the SEU rate) is too high or if the memory refresh rate is too low: in these cases, too many errors clusters could accumulate in the memory array in a short time interval for the algorithm to be able to sort them out. Also, the complexity of the current clustering algorithm evolves in  $n^2$ , with  $n$  being the number of errors; this means that tests having logged several hundred thousands of individual upsets may take several hours to process. This methodology may be applied to many types and models of memory components, but the values of key parameters of the algorithms have to be empirically determined to match the behaviour of the test subject. Lastly, although this algorithm allows an otherwise tedious and considerably long task to be automated, it has to be kept in mind that



due to the nature of this task, its results cannot be expected to match the reliability of “manual” clustering carried out by an experimented person on a bitmap.

#### ACKNOWLEDGMENT

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## Annex III

**A. L. Bosser**, V. Gupta, G. Tsiligiannis, C. Frost, A. Zadeh, J. Jaatinen, A. Javanainen, H. Puchner, F. Saigné, A. Virtanen, F. Wrobel, and L. Dilillo, "Methodologies for the Statistical Analysis of Memory Response to Radiation", in *IEEE Transactions on Nuclear Science*, Vol. 63, no. 4, pp.2122-2128, 2016.

*Contribution: the author had a major role in the experiment's software and hardware development, took part in the test campaigns, and did most of the data processing and writing.*

# Methodologies for the Statistical Analysis of Memory Response to Radiation

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**Abstract**—Methodologies are proposed for in-depth statistical analysis of Single Event Upset data. The motivation for using these methodologies is to obtain precise information on the intrinsic defects and weaknesses of the tested devices, and to gain insight on their failure mechanisms, at no additional cost. The case study is a 65 nm SRAM irradiated with neutrons, protons and heavy ions. This publication is an extended version of a previous study [1].

**Index Terms**—Cluster of bit flips, dynamic test, multiple cell upset (MCU), radiation effects, single event upset (SEU), SRAM, static test.

## I. INTRODUCTION

MEMORIES are ubiquitous components in today's electronic devices, with applications in about every field of the industry, from daily consumer goods to critical military, aerospace or civil nuclear systems. The technology behind

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Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

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memory components progressed continuously over the last four decades, with large improvements regarding device size, I/O performance, power consumption and capacity. However, these advances (in particular, the reduction in device feature size and operating voltages) have led to the side effect of increasing the radiation sensitivity of memories. Single-Event Upsets (SEUs), such as Single-Bit Upsets (SBUs) and Multiple-Bit Upsets (MBUs), phenomena whereby one (SBU) or several (MBU) memory bits are upset due to a single particle strike, are becoming ever more common in advanced memories.

The aim of this work is to improve the methodologies in use to characterize the behaviour of memories in a radiative environment: statistical trends may appear in their response, which may offer insight on the failure mechanisms and suggest ways to improve the radiation hardness of the device.

In this study, a set of methods is proposed to perform effective in-depth statistical analysis of test data, which rely on organising the detected errors in databases. This technique can reveal process variations and silent defects in devices, as well as topological gradients in the memory array sensitivity. In the following sections, the main points of the method are first described and then its application to the case study of a 65 nm SRAM memory from Cypress Semiconductor is discussed.

## II. TEST SETUP AND DATA COLLECTION

Our research team has conducted several test campaigns at the RADEF (University of Jyväskylä, Finland), Vesuvio (ISIS, Rutherford Appleton Laboratory, UK), and HIF (Université Catholique de Louvain, Belgium) test facilities. Table I summarises the key points of these Test Campaigns (TC).

The same types of ions were used during tests at HIF and RADEF, although with a slight difference in particle energy. These different sets of data allowed to cross-compare test results. The energy spectrum of the Vesuvio neutron beam is atmospheric-like [2]. The proton energies used at RADEF ranged from 100 keV to 6 MeV for LEP tests [3], and from 6 MeV to 55 MeV for HEP. The LET of the heavy ions used at HIF ranged from 3.3 to 67.7 MeV · cm<sup>2</sup> · mg<sup>-1</sup> [4], whereas the LET of the heavy ions used at RADEF ranged from 1.9 to 60 MeV · cm<sup>2</sup> · mg<sup>-1</sup>. Particle fluxes and fluences varied widely in accordance to the memories' sensitivity: fluence ranged from to cm<sup>-2</sup> for neutrons, from up to cm<sup>-2</sup> for protons, and from to cm<sup>-2</sup> for the various types of heavy ions.

TABLE I

LIST OF THE TEST CAMPAIGNS USED AS A SOURCE OF DATA FOR THIS STUDY. ONLY SRAM B AND C ORIGINATE FROM THE SAME LOT

Name	Facility	Test particle	Energy	DUT
TC0	Vesuvio	Neutrons	Atmospheric	SRAM A
TC2 LEP	RADEF	Low-energy protons (LEP)	600 keV to 4.7 MeV	SRAM B
TC2 HEP	RADEF	High-energy protons (HEP)	9.5 to 50 MeV	SRAM C
TC3	RADEF	Heavy-ions (N, Fe, Kr, Xe)	9.3 MeV/u	SRAM D
TC5	HIF	Heavy-ions (C, N, Ne, Ar, Ni, Kr, Xe)	3.9 MeV/u, 9.3 MeV/u	SRAM E
TC6	RADEF	High-energy protons (HEP)	10 to 45 MeV	SRAM F

Irradiation time varied from several seconds to a few minutes for ions, and from a few minutes to a few hours for neutrons.

Each irradiated memory was mounted in an open-top testing socket (for protons and heavy-ions) or directly soldered on a PCB (for neutrons) and driven by a Digilent Spartan-3 FPGA board, on which a memory controller, based on a finite-state machine, was implemented. The FPGA was then connected via a serial link to a computer, for data storage and experiment control. The test data were archived in the form of text logs, containing the timestamp, the logic address and the signature (data) of the corrupted words.

During the irradiation campaigns, the memories were tested both in *static* and *dynamic modes*. In the static mode, the memories were initialised with a known data background, then exposed to predetermined particle fluences while in retention, and finally read back to detect the occurrence of bit flips. In dynamic mode, several algorithmic stimuli, with specific sequences of read and write accesses, were performed during the whole particle exposure with the purpose of exerting specific stresses on the memory, in both the cell array and control circuitry. Details of these algorithms are given in [5].

### III. MEMORY ARCHITECTURE

In order to explore our methodologies, a commercial 65 nm SRAM memory from Cypress Semiconductor (CY62167GE) is used as a case study. A simplified view of the architecture of this memory is presented in Fig. 1.

The memory array, whose effective capacity is 16Mib (one mebibyte = 1024\*1024 bytes), is divided in four 4Mib “quads”. Each quad is in turn divided in two 2Mib “octants” by a central horizontal spine, which contains (among other functional blocks) the sense amplifiers. These sense amplifiers will be shared by the two octants of the quad.

Each octant is then further divided into blocks. In our case, where the memory was operated in 8-bit word length mode, the eight bits of each single word are all located within the same

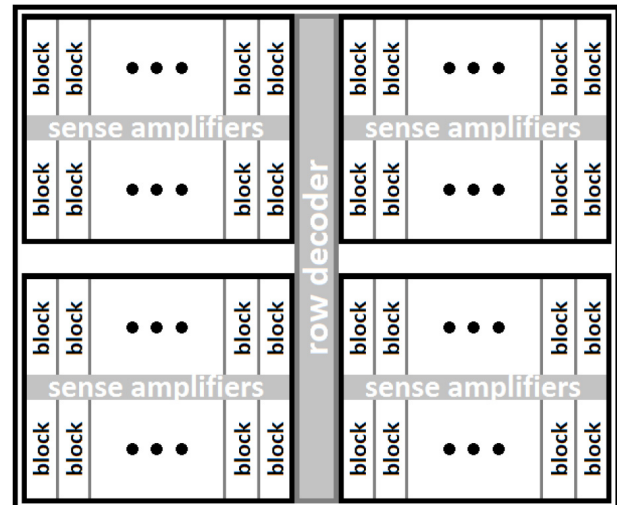


Fig. 1. Simplified floorplan of the SRAM memory used in this study.

logic block, on the same row, separated from each other by other memory cells (a technique called *interleaving*). The bit lines run vertically across each logic block from the quad’s central spine to the other edge, with bit line equalizers located at both ends.

This memory embeds Error-Correcting Code circuitry that may be used to automatically detect and correct isolated SEUs during read operations. However, this feature was disabled for the purpose of this study.

### IV. METHODOLOGY

The raw text logs containing the data from the test campaigns were processed with an in-house C++ program and Scilab [6] scripts, and the knowledge of the memory’s scrambling and interleaving schemes (provided by the manufacturer). From the test logs, databases were constructed, which referenced the location and timestamp of recorded errors, and associated them into clusters. It is then possible to manipulate these databases and extract statistics from them.

The Scilab program can generate *bitmaps*, which are images representing the memory array, generated from one or several test logs, where every pixel corresponds to a single bit cell. Every cell that suffered a radiation-induced upset during the test appears as a black pixel, whereas all the other cells appear white. In some cases, the study of bitmaps allowed identifying topological error trends with the naked eye.

The next step was to seek for less recognisable trends in this pool of data. For this purpose, we implemented in our Scilab program the capability to calculate various statistics on the number of bit flips and clusters of bit flips that had occurred throughout the die, or within specific regions of the die. By defining these regions of interest to match architectural features of the memory (logic block boundaries, proximity to key elements like the sense amplifiers or power switches, etc. . .) we managed to highlight interesting tendencies in the localisation of the cell upsets.

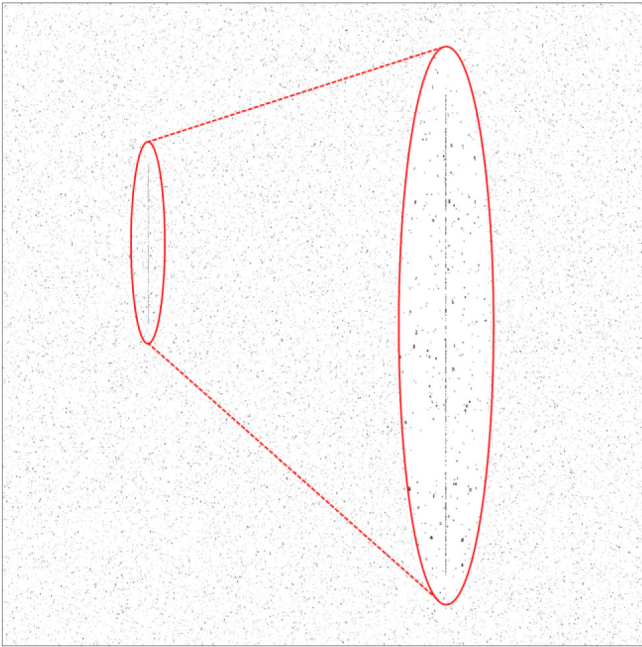


Fig. 2. Composite image of all TC5 bitmaps, with a zoom-in on the column with high rate of failure (SRAM E).

## V. CASE STUDY: A STATISTICAL SURVEY OF A 65 NM SRAM

### A. Bitmap Observation

The first step in our approach was to create a bitmap for each test campaign, displaying all the cells that suffered an upset at some point during the campaign. At first sight, the resulting bitmaps exhibited homogeneously scattered clusters of errors. Moreover, the bitmaps did not display any very large-scale error cluster, which are often seen on bitmaps obtained from other devices tested in similar conditions [7]. This last observation, made on an extensive amount of test data, indicates that this particular model of SRAM memory is not prone to large-scale failures.

However, unlike the bitmaps obtained from other test campaigns and test specimens, the bitmap generated from all the heavy-ion test data on SRAM E displayed a peculiar feature, as shown in Fig. 2: a single one-cell-wide column, running from the top to the bottom of a single memory block exhibited a far larger concentration of errors than the rest of the memory array.

When averaged over the whole memory die, only 0.53% of the cells suffered an upset during these tests. However, when only considering the cells of this particular column, the proportion of cells which suffered at least one upset increases to 47%, two orders of magnitude above the rest of the die.

After this feature was noticed, individual bitmaps were created for each test carried out on SRAM E; however, the feature did not appear on any of these. This means that this vertical set of cell upsets has not been caused by a Single Event Functional Interrupt (SEFI), but is instead purely the product of a higher vulnerability of this region (column section) of the die. Additionally, after creating two separate bitmaps from the SRAM E test data—one from the static tests, and one from the dynamic tests—the faults only appeared on the latter one. This

proves a reduced reliability of a sensitive element for the read access within the column, such as the pre-charge circuit or one of the two bit lines. Elements like the sense amplifier and the power switch are not likely to be responsible, since they are shared by more than one column, whereas the faults are statistically more present in a single column.

From this part of the study, it can be deduced that some specimens exhibit latent defects, which are only revealed when under stress from both a radiative environment and continuous read/write operations, and which can induce a local increase in SEU susceptibility of several orders of magnitude.

### B. Statistical Analyses

In this part of the study, possible large-scale statistical biases in the spatial distribution of cell upsets on the memory dies are investigated. Our mode of operation was the following:

1. The pool of data was divided into smaller, more specific data subsets. Three data subsets were created for each of our six test campaigns: one set comprised all of the tests in the campaign, the second comprised only the static tests, and the third only the dynamic tests.
2. Several partition schemes were designed for the memory array. Each partition scheme was chosen to group the cells according to a different specific criterion (for example, their proximity to a particular functional element of the memory, the memory blocks, etc.). For a given partition scheme, each region covered an equal number of memory cells.
3. For every possible combination of data subset and partition scheme, the number of cell upsets (or clusters of cell upsets) occurring in each region was counted. The results were compared to identify the effect of different parameters (test mode, particle species, etc.) on the memory sensitivity, with respect to the device topology.

The most significant results from this part of the study are detailed in the four following subsections, each of them dedicated to a different partition scheme.

1) *Effect of the Cell Position Along the Bit Line:* Bit lines are core elements in the operation of an SRAM memory cell. Each cell is connected to a pair of complementary bit lines, which are shared with all the other cells in the same column. At both ends of the bit line are pre-charge circuits, which are used during read and write operations to set the bit line to predetermined potentials. One end of each bit line may be connected to another important component: a sense amplifier. The sense amplifiers are used to read the value stored in a given cell by comparing the electric voltage difference between its two bit lines. However, since the bit lines are not perfect conductors, they may suffer from systematic manufacturing defects, which can have an impact on their capacity and conductivity. To investigate whether the distance along the bit line between a cell and its sense amplifier could have an impact on the success of a read access, a partition was used which divided the memory array into two groups of equal population of cells. One group comprises all the cells located the closest to their sense amplifier, and the other group comprises all the cells located the furthest away from their sense amplifier.

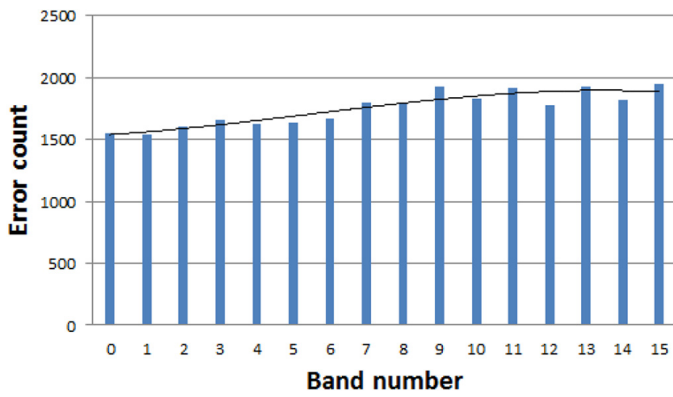


Fig. 3. Error count per vertical band during SRAM C static HEP tests.

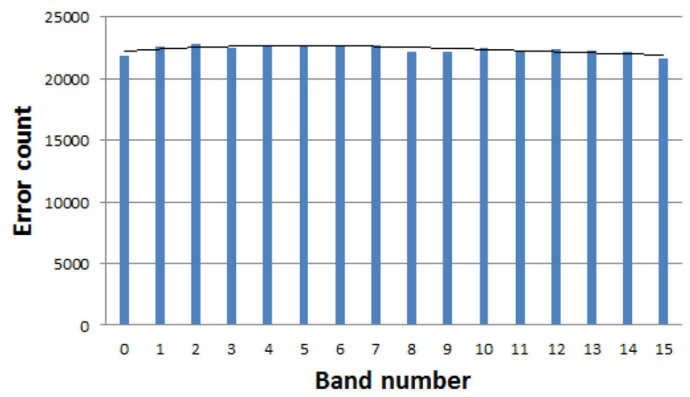


Fig. 5. Error count per vertical band during SRAM B static LEP tests.

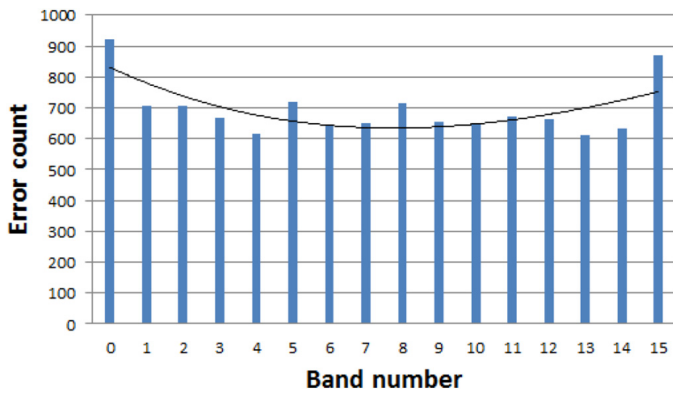


Fig. 4. Error count per vertical band during SRAM B dynamic LEP tests.

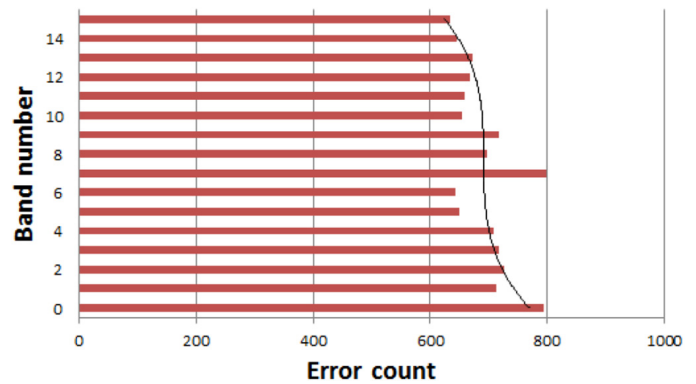


Fig. 6. Error count per horizontal band during SRAM B dynamic LEP tests.

The results were very clear: in all of the considered tests, the error counts in both groups were always very close, with the difference never exceeding 4%. This showed that the position of a cell along its bit lines has no impact on its probability to suffer an SEU; it can be seen as a beneficial impact of this memory’s array layout, whose division in eight octants minimises the issues related to the bit line length.

2) *Transversal Gradients in Sensitivity*: Other partitions that were investigated divide the array into small bands. One partition scheme splits the array in sixteen equal vertical bands running from the top to the bottom. The most remarkable results arising from this partition are represented in Figs. 3–5 by blue vertical histograms. Another partition divides the array in sixteen horizontal bands running from one edge of the array to the other, and the results obtained using this partition are plotted in Figs. 6–7 as red horizontal histograms. The large majority of the results did not exhibit any special trend, and most of the recorded error rate variations remained within the beam homogeneity uncertainty and statistical uncertainty, hence they are not reported here. In the reported cases, the magnitude of the trend was significantly larger than the combined uncertainties (standard error the bit flip count, particle fluence homogeneity, etc.). Third-degree polynomial fitting curves have been added to the histograms to highlight these trends.

In Fig. 3, the errors yielded by all HEP static tests on SRAM C show a clear bias, with a progressive increase in sensitivity from the left to the right side of the memory array, leading to a 25% increased error count in the vertical band 15 over vertical band 0. When subjected to dynamic stress tests, the

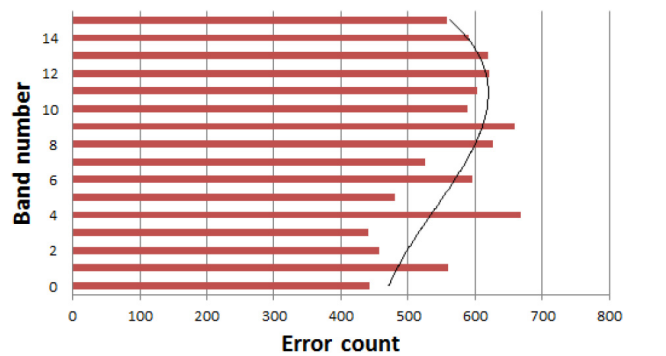


Fig. 7. Error count per horizontal band during SRAM A dynamic neutron tests.

same device exhibited a similar, though slighter (7%) sensitivity gradient. This trend was absent from the data gathered on SRAM F, obtained with similar testing patterns and similar proton energies.

Another device (SRAM B) exhibited a very sharp increase in the dynamic error rate in its leftmost and rightmost vertical areas (+40% and +33% when compared to the error rate at the centre of the die, respectively) (see Fig. 4). Interestingly, a very slight opposite trend appeared when this device was tested in static mode (see Fig. 5).

This same specimen (SRAM B) also presented a progressive 25% sensitivity increase from the top to the bottom of the die during dynamic testing (see Fig. 6). When subjected to static tests, it exhibited a similar, although slighter (5%) sensitivity increase.

Conversely, SRAM A exhibited the opposite behavior during dynamic neutron tests and not during static tests, with an error rate almost 40% higher in the bottom regions with regards to the topmost one (Fig. 7).

In the case of SRAM B's increased sensitivity on the left and right edges (Fig. 4), it could be caused by propagation delays affecting the signals from the address row decoder. This component is located at the centre of the memory die, laid out in a column that runs from the bottom to the top in a butterfly configuration that separates the die into two parts. The word line selection signals driven by the decoder undergo a larger delay to reach the outer cells than the ones located nearest to the decoder. This may reduce the time available for these cells to complete read/write operations, enhancing the device sensitivity in dynamic mode during irradiation. Conversely, the address row decoder is idle during static tests, which would explain why this tendency does not appear during static testing (Fig. 5).

SRAM A, B and C top-to-bottom and left-to-right variations in sensitivity (Figs. 3, 6 and 7) cannot find an explanation in the layout of the memory. Indeed, the eight octants of the memory array share a common (mirrored) architecture, and should indicate the same trends if the variations in their sensitivity were caused by their design. This disparity is probably caused by random doping fluctuations throughout the memory array during the manufacturing process of SRAM A, B and C, impacting in different ways the static and read noise margin characteristics of cells that are placed in different regions of the die, and ultimately leading to different SEU susceptibilities [8]–[10].

3) *Effect of the Proximity of Tap Cells:* A latch-up occurs when an ion-induced voltage transient in the substrate or diffusion well triggers a parasitic thyristor, leading to the sudden establishment of an intense and potentially destructive current flow between Vdd and the ground [11]. Tap cells are connections between the memory substrate (or a diffusion well) and the ground (or Vdd), which are used to lower the resistance between the substrate/well and the associated power grid, tying its potential to its reference point and effectively preventing the triggering of the parasitic thyristor [12]. In the memory used in our case study, tap cells are disposed at regular intervals vertically and horizontally, forming rectangular "tap rings" enclosing a few thousand cells.

To investigate the effect of the proximity of tap cells on the SEU sensitivity of memory cells, the memory array was divided into four groups A, B, C and D of equal area and memory size. Each group was made of a collection of horizontal bands, each a few cells high and spanning the whole width of the memory array; group A contained only memory cells which were the closest to the taps, whereas group D contained the memory cells which were the furthest away from them. Due to the simplicity of this partition scheme and to the layout of the taps, as illustrated by Fig. 8, groups B, C and D contain a small percentage of cells which are as close to a tap as the cells in the A group, which are located next to the vertical boundaries of the tap ring. However, since the tap rings are much wider than they are high, these cells are so few that they have very little effect on the following statistics.

The proportion of bit flips accumulated in each group during each test campaign is plotted in Fig. 9 (static test data) and

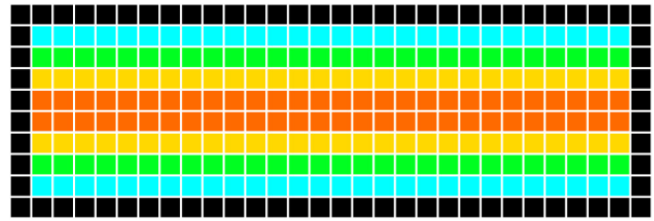


Fig. 8. Illustration of the partition scheme used to study the impact of the proximity to tap cells on cell SEU susceptibility. A single ring of tap cells is shown in black, and the rows corresponding to group A, B, C and D cells are shown blue, green, yellow and orange respectively. The length and width of the features in this figure are arbitrary and do not necessarily correspond to the actual dimensions of tap rings and cell group bands.

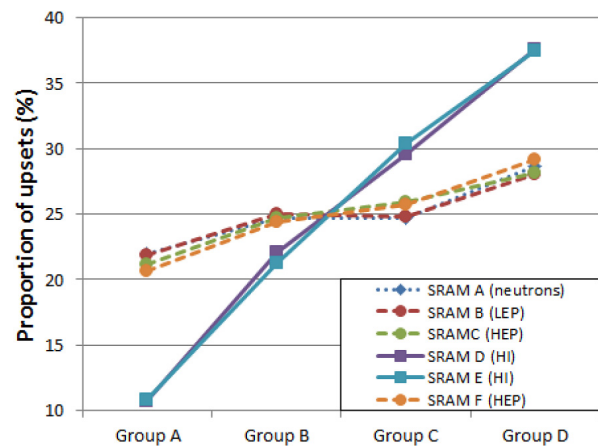


Fig. 9. Effect of the proximity of the tap cells on the relative SEU sensitivity of memory cells (static test data).

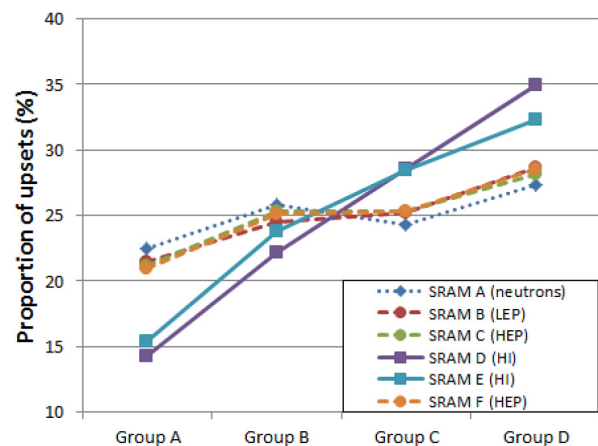


Fig. 10. Effect of the proximity of the tap cells on the relative SEU sensitivity of memory cells (dynamic test data).

Fig. 10 (dynamic test data); the ordinate axis gives the proportion of bit flips occurring in the corresponding group when compared to the whole memory array. In every test campaign, the same trend was clearly repeated: the group A cells (closest to the taps) were the least affected, while the group D cells (furthest away from the taps) suffered a sharply higher number of upsets. This suggests that the taps prevent the occurrence of SEU by collecting part of the diffusing charge, lowering the quantity of charge collected by the memory cell inverters. This behaviour was evidenced by Gasiot et al. [13], who proved that

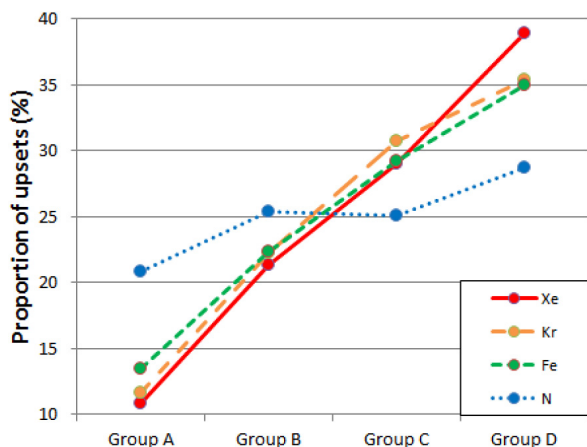


Fig. 11. Effect of the heavy-ion species on the relative sensitivity of the memory cell groups (mixed static and dynamic test data from TC3).

increasing the frequency of well tap rows was an efficient way to mitigate MCUs. Yamaguchi *et al.* [14] also explained that during an SEU, the carriers generated in a well are evacuated through the resistance between the hit point and the tap. This resistance increases with the distance between these points. This means that in the event of a particle hit, the further the hit point is away from a well tap, the higher parasitic voltage transients will be created at the hit point by the evacuation of the SEU-generated carriers, which makes the occurrence of a cell upset more likely. The mitigating effect of the taps is more pronounced during static irradiation than during dynamic irradiation; this is probably due to a lower cell supply voltage when the memory is not accessed, leading to a higher cell upset sensitivity. In this situation, eventual charge collection by the taps is more likely to make a difference between the occurrence and the non-occurrence of a cell upset.

Interestingly, while this trend was present in the data from every test campaign, it was much stronger during heavy-ion test campaigns than during neutron and proton irradiations. This can be seen in Fig. 9 and Fig. 10. Fig. 11 differentiates the data obtained at the HIF facility (TC5) by ion species and reveals that the heaviest ions led to the largest difference in sensitivity between groups A, B, C and D, whereas the results obtained with nitrogen are close to those obtained with protons and neutrons (Figs. 8 and 9).

Fig. 12 (sourced from Fig. 3.5 in reference [15], which uses semi-empirical formulae from [16]) provides an estimate for the density of ion-induced excess charge as a function of radial distance from the trajectory of the impinging particle, for different ion species (proton, nitrogen and xenon) at different energies. From this figure, we can notice that for a given free carrier density, the “cloud” of free carriers generated by protons and low-Z ions (such as the recoils created during neutron irradiation) is much smaller than the charge clouds generated by very heavy ions (such as xenon).

These large charge clouds are then more likely to encompass tap cells, in which case the large concentration of free carriers around them facilitates the drift and collection of the generated charge at the tap. Conversely, small carrier clouds generated by protons and low-Z ions are less likely to encompass tap cells;

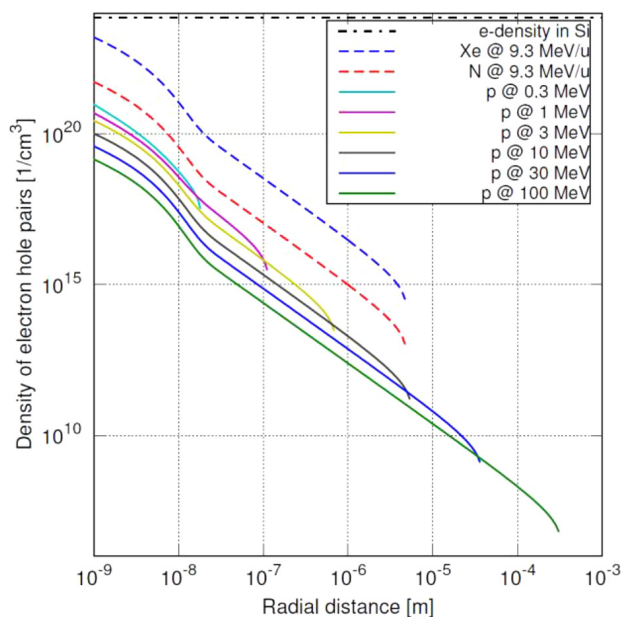


Fig. 12. An average density of generated charge carriers in silicon as a function of radial distance from particle trajectory for different incoming particle species and energies (retrieved from [15]). The dash-dotted line represent the density of all electrons in silicon.

TABLE II

EFFECT OF THE PARTICLE SPECIES AND TEST TYPE ON BLOCK SENSITIVITY DISPARITY. THE CELL COLOUR INDICATES THE STANDARD ERROR FOR THE CELL VALUE (SEE LEGEND ON THE RIGHT), WHICH WAS CALCULATED ON THE BASIS OF THE AVERAGE NUMBER OF EVENTS (CLUSTERS) PER BLOCK RECORDED IN THE CORRESPONDING SITUATION

Particle	SRAM	Max/min error cluster count per block			Max/min error count per block			Standard error colour code
		Global	Static	Dynamic	Global	Static	Dynamic	
Neutrons	A	151%	152%	185%	148%	160%	191%	<2%
LEP	B	111%	111%	201%	110%	111%	202%	<5%
HEP	C	134%	141%	152%	134%	147%	147%	<5%
HEP	D	118%	131%	125%	126%	142%	131%	<5%
Heavy ions	E	153%	176%	155%	149%	222%	153%	5%<e<10%
Heavy ions	F	194%	224%	202%	194%	297%	194%	10%<e<16%

their charge is more likely to be collected by cell transistors, and thus to trigger a cell upset.

4) *Block-to-block Variability*: The last partition scheme divided the array in similar rectangles (matching the memory’s logic blocks). In this last part of the study, the variation in cell sensitivity from block to block depending on particle type and memory specimen was investigated.

Once again, a distinction was made between the results obtained from test campaigns as a whole, and those obtained from separate static and dynamic tests. For each case, the highest and lowest values of two variables were considered: the amount of cell upsets per block, and the amount of cell upset clusters per block. Both of these variables’ max/min ratio are displayed on Table II, for each possible case.

The results of this analysis suggest that heavy-ion tests tend to induce a higher variability in the SEU susceptibility of different memory blocks. The testing mode, however, has no definite impact on this parameter. Interestingly, for a given test campaign/memory specimen, we observed little correlation between a block’s relative sensitivity during static testing, and



its relative sensitivity during dynamic testing. An important factor in this observed static/dynamic discrepancy is the fact that when idle (not being accessed), the internal control circuitry of the device lowers the supply voltage of the memory cells to a level which does not allow read or write operations (which is not a concern in idle mode) while still ensuring data retention. This low-power state of the memory array has a direct impact on the electric fields in the memory substrate, which in turns has a direct effect on free carrier generation, recombination, drift and collection in the event of a particle strike. What's more, in this low-power state, the memory cell is inherently less stable than under "active" operating bias, and is more vulnerable to access failures caused by potential random dopant fluctuations between its transistors [9]. On the other hand, during static testing, the memory control circuitry cannot induce any error, unlike during dynamic testing. These are examples how different testing conditions can reveal different failure mechanisms in the memory's subsystems.

## VI. CONCLUSION

A method for the investigation of radiation effects on memories was introduced, which is based on error referencing, direct bitmap observation and database manipulation. In the presented case study, the use of this method brought out further information from the irradiation test data than the typical cross-section values, at no additional cost. In particular, it highlighted specimen-to-specimen variability due to manufacturing variations or silent defects, and topological trends in the devices' SEU sensitivity due to their architectural features. Beside this case study, the proposed methodology can be applied to investigate other types of memories.

The results from this study accentuate the need to systematically perform memory testing on several specimens at once, to eliminate eventual device-specific biases in the test results. They also underline the benefits of carrying out dynamic tests along with static tests during memory irradiation campaigns, as they bring out different failure mechanisms.

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## Annex IV

L. Dillo, G. Tsiligiannis, V. Gupta, **A. Bosser**, F. Sagné and F. Wrobel, “Soft errors in commercial off-the-shelf static random-access memories”, in *Semiconductor Science and Technology*, vol. 32, no.1, 2016

*Contribution: the author had a major role in the experiment’s software and hardware development, and took part in the test campaigns, data processing and writing.*

## Topical Review

# Soft errors in commercial off-the-shelf static random access memories

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## Abstract

This article reviews state-of-the-art techniques for the evaluation of the effect of radiation on static random access memory (SRAM). We detailed irradiation test techniques and results from irradiation experiments with several types of particles. Two commercial SRAMs, in 90 and 65 nm technology nodes, were considered as case studies. Besides the basic static and dynamic test modes, advanced stimuli for the irradiation tests were introduced, as well as statistical post-processing techniques allowing for deeper analysis of the correlations between bit-flip cross-sections and design/architectural characteristics of the memory device. Further insight is provided on the response of irradiated stacked layer devices and on the use of characterized SRAM devices as particle detectors.

Keywords: SRAMs, radiation particles, static mode test, dynamic mode test, March test, stacked dies, bitmapping

(Some figures may appear in colour only in the online journal)

## 1. Introduction

Soft errors are the result of interaction between ionizing particles and the matter composing electronic devices. In recent years, soft errors have become a major concern for the electronics community. Malfunctions can occur in electronic devices through ionizing radiation and may affect the correct operation of both analog and digital circuitry, with detrimental outcomes on the overall system. Historically, the main applications affected by soft errors are regarding space (satellites and spacecraft), military, avionics, medical, and nuclear technology; more recently, the automotive sector is becoming increasingly concerned. All these applications do not tolerate large failure rates due to operational criticality and human safety. Concurrently, technological advances brought a considerable reduction in transistor size, worsening the

robustness of electronic devices against ionizing radiation, and bringing soft errors to the attention of commercial applications that usually integrate the latest technology nodes. The complexity of this radiation effects topic is large due to its interdisciplinary nature combining nuclear physics, with digital and analog electronics.

Electronic devices may be exposed to different types of radiation depending on their target application. Radiation environments can be divided into two main categories: natural environments such as those of space (mostly populated by heavy ions and protons) and the atmosphere (populated by many types of particles, with neutrons being the most important), or artificial environments such as those inside particle accelerators and nuclear reactors. Each environment is composed of a variety of particles with different energy spectra, making them more or less harsh for electronic

devices. The production of radiation-hardened by design (RHBD) and reliable commercial off-the-shelf (COTS) electronic components is a very challenging practice, and the testing of such devices is strongly connected to this procedure. Studying the effects of ionizing radiation on electronic devices not only reveals the weaknesses related to a given technology, but may also be extremely useful for interpreting failure mechanisms within the scope of developing efficient mitigation techniques.

Even though ionizing radiation may affect different types of components, memory devices are often the most affected by soft errors. According to [1], electronic memories, and more specifically static random access memories (SRAMs), represent the dominant type of devices in embedded systems, occupying the largest portion of system on chip (SoC) areas. Thanks to their simple architecture, compatibility with standard processes and high access performances, SRAMs are present in the majority of computing systems. On the other hand, the inner characteristics of this type of device, such as the large area needed in the die, and typical cell structure based on the inverter loop, makes SRAMs one of the main sources of errors in SoCs [2]. Additionally, the nature of all memory devices makes them capable of storing radiation-induced errors. This is in contrast to combinational circuits, where soft errors are rarer and more difficult to detect. These facts prove that memories, and more specifically SRAMs, are the perfect candidate for studying soft errors.

This article is dedicated to the exploration of state-of-the-art methods for testing memory devices under ionizing radiation by considering the different parameters that may influence this type of study and that originate from the environment (e.g. type of particle, temperature, etc), the inner characteristics of the device (e.g. design/architecture, number of stacked dies, technology node, etc) and electrical stimuli (supply voltage, switching activity, type of access, etc). We introduced accelerated testing methods combined with the most efficient techniques that permit device sensitization and expose behaviors that may not be revealed with conventional testing approaches. Furthermore, we exposed advanced data processing techniques to perform a deeper analysis of the results of irradiation campaigns combining bit-flip logs with other parameters like topological error concentration. Finally, by combining the knowledge acquired from studies of memory devices and the principles of radiation testing, SRAM-based instruments are proposed for monitoring radiation levels in artificial mixed fields and atmospheric environments through real-time testing techniques.

Section 2 will introduce the basics of state-of-the-art methods that test the effects of radiation on SRAMs. Section 3 will provide fundamentals on the SRAM architecture that are useful for understanding the following sections. The rest of the article focuses on the most meaningful studies made by the authors in recent years on this topic.

## 2. State-of-the-art methods

SRAM sensitivity to ionizing particles varies when different operation conditions are applied, such as access modes or temperature variations. To verify these results and explore realistic responses of SRAMs, the same conditions must be replicated during accelerated radiation tests in irradiation facilities. Although accelerated testing is considered to be among the most effective methods of evaluating the performance of electronic devices under ionizing radiation, its elevated cost makes extensive campaigns difficult to organize. Thus, it is fundamental to carefully plan the type of tests to apply on the device in order to reproduce those stimuli that could reveal all potential radiation-induced errors.

Electronics for space applications are generally produced using hardening techniques against radiation, and often the small demand for such devices does not permit fast evolution and custom development. Consequently, these technologies usually do not perform as well not as their commercial counterparts in terms of speed, silicon area, and power consumption. For this reason, in recent years, COTS devices started to be considered for use in harsh environment applications granted they met fixed reliability constraints [3]. On the other hand, applications that commonly utilize COTS components, such as for medical and automotive use, became more demanding in terms of soft error resilience and ensuring a minimum level of reliability. Testing memories under ionizing radiation, and more specifically SRAMs, has been practiced for many years because memories are considered good test vehicles to represent new technology nodes for terrestrial and space applications. Several guidelines exist for testing devices under different types of ionizing radiation. Although these guidelines propose numerous testing methods [4, 5], in common practice, the static mode testing (retention mode; more details given in section 4) is the most applied for memories, such as in [6, 7]. In the following sections, it will be demonstrated that static mode testing is unable to reveal the full range of effects that may occur in SRAMs when exposed to ionizing radiation. Some studies have shown that dynamic mode testing (memory accessed with read/write actions; more details given in section 4) can lead to different levels of sensitivity for SRAMs by employing functional algorithms that are generally used at production level.

For exploring the various operational conditions in which devices should be tested under radiation, temperature must be considered. Temperature variations are crucial, especially for space, military, nuclear, and avionics applications, i.e., applications that are usually affected by soft errors. At the experimental level, several works investigate the impact of temperature on device sensitivity, such as in [8–10], where the high temperature effect was studied when irradiating SRAMs with protons. However, very few of these studies involved irradiating SRAMs with neutrons. As a critical part of the testing procedures, the effect of high and low temperature will be demonstrated in section 5 using SRAM devices irradiated with neutrons and by applying different test stimuli.

Testing SRAMs under ionizing radiation may reveal several types of single event upsets (SEUs) besides the simple bit-flip, which is usually referred to as single bit upset (SBU). One of the most common events that have been observed and tend to become a major threat for memory robustness due to their increased appearance frequency is the multiple cell upset (MCU), which is a typical result of technology downscaling. Due to transistor shrinking, the distances between the sensitive nodes of cells are reduced (for example, the drain of the NMOS transistor of the two-inverter loop in SRAM cells described in section 3). Meanwhile, the charge induced by the impinging particles remains relatively stable. The importance of MCUs comes from the possibility of them resulting in multiple bit upsets (MBUs; two or more bits belonging to the same word and being corrupted). When an MBU occurs, error detection and error correction codes (ECC) cannot guarantee data integrity. Memories that integrate ECCs are usually able to correct one (rarely two) corrupted bits per byte. Of course, these techniques come with an area overhead cost due to redundancies, especially for the case of two corrected bits.

Many studies investigating particle-induced MCUs exist in the literature, most of which are focused on MCUs appearing in SRAMs at both the simulation and experimental level. At the simulation level, in [11], the relation between the increased frequency of MCUs and the device downscaling was shown for SRAM cells. The study in [12] explored the SEU and MCU cross-sections of SRAM cells as a function of the deposited charge in their sensitive nodes. Complementing the work done at the simulation level, several studies have confirmed the existence of MCUs at the experimental level. An extensive study that analyzed the sizes and shapes of MCUs appearing in an SRAM is presented in [13]. MCUs were observed while the SRAM device was irradiated with neutrons of different energies and operating in retention mode. While MCUs are the most diffuse event involving more than one corrupted bit, single event latch-ups (SELs) can induce a rather large number of corrupted bits. Another study investigated micro-SELs recorded during radiation testing and that appeared as large clusters of upsets [14]. Such events are confined thanks to memory segmentation in blocks surrounded by well taps.

In the following sections, some of the most common MCUs and large-scale events, such as micro-SELs and SEFIs, will be analyzed and investigated using results from extensive experimental campaigns performed by the authors. More generally, the state-of-the-art method introduced here will be integrated with those made in recent years by the authors.

### 3. SRAM architecture

As depicted in figure 1, SRAM memories are mainly composed of the memory cell array, where the information is physically stored and peripheral circuitry allows correct cell selection, data reading/writing, buffering, and synchronization. The main peripheral circuits are the address decoders, address and data buffers, write drivers, and sense amplifiers.

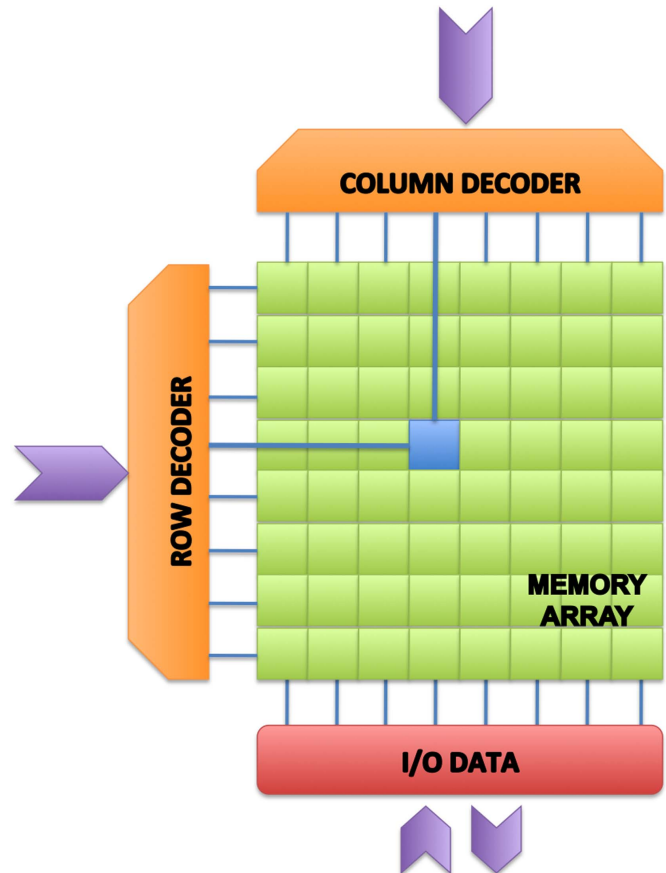


Figure 1. Basic structure of SRAMs.

The memory array can be composed of a single rectangular cell matrix, like in figure 1, or present a more complex configuration, such as the butterfly, with two cell arrays divided by a single row decoder [2]. Simple or multiple arrays can be further organized in blocks, reducing the size of bit lines and word lines, and making cell accesses more efficient with less delay as a result of shorter wiring. Furthermore, a memory word may be, generally, between 8 and 64 bits long, and the cells corresponding to these bits are often not close topologically since interleaving schemes are applied. Similarly, contiguous address values are generally not physically adjacent since scrambling schemes are employed.

To facilitate understanding of the interaction between ionizing particles and SRAMs, it is useful to introduce the core-cell structure that most commonly follows the six transistors (6 T) architecture, as shown in the scheme in figure 2. The bit to be stored in the cell is set into the latch structure composed by four transistors (PU\_BLB, PD\_BLB, PU\_BL, and PD\_BL in figure 2) that generate a two-inverter loop. The remaining two transistors are used for cell access to the bit lines (pass gates; PG\_BL and PG\_BLB) for read/write action under the command of the word line (WL) selection signal.

The storage latch presents two nodes (S and SB) that are always set to an opposite value. When the cell is accessed for a write operation, the two bit lines are set to wanted values ('1' and '0', or '0' and '1') and, when the word line signal is activated, the cell nodes are set with the values of the bit lines. This is possible because the equivalent capacitance of the bit

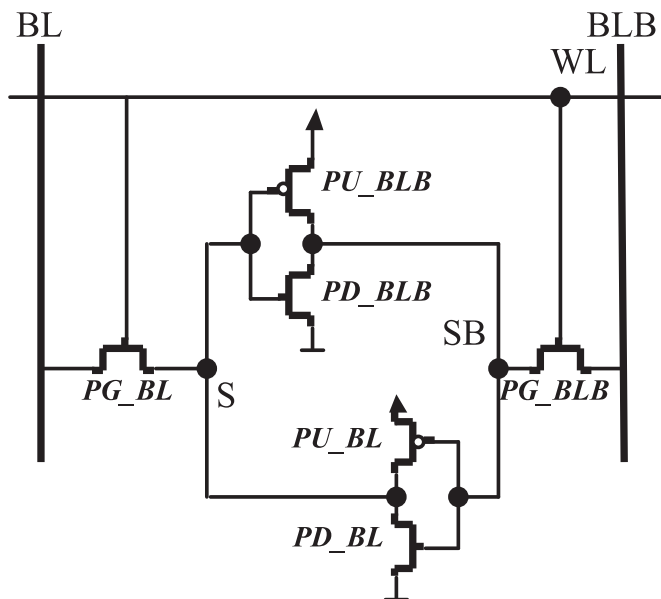


Figure 2. Scheme of the 6 T SRAM memory core-cell.

lines is two orders of magnitude higher than those of the cell nodes. For this reason, during the read access the two bit lines are pre-charged at an equalized potential (generally '1', VDD) to prevent any unwanted cell swap. When the word line signal is active, the cell node at '0' reduces the voltage level of the corresponding bit line. Afterwards, the cell is disconnected and a sense amplifier amplifies the voltage difference between the two bit lines and transmits the read value to the data buffer.

Functional and radiation-induced faults in an SRAM are either generated in the memory cell array or are mapped in it. In other words, the error can be either generated in the core-cell(s) and be observable with the cell read access, or be generated in the peripheral circuits and result in read/write failures or access to wrong memory locations. These failures are then observed with read accesses that only apparently reveal cell bit-flips. For example, if during a read access, the synchronization circuitry is affected by a particle and the sensing time can be reduced. Consequently, the voltage difference between the two cell nodes to be sensed is reduced, and the value returned by the read operation is random, and thus potentially faulty. For an external observer, although the cell still stores the correct value, the error appears like a cell bit-flip. In this case, a second read access might be operated to verify if the error is due to an actual bit-flip or to a failure in the access circuitry.

## 4. Test methods

Testing, as the main process behind the qualification of electronic components for applications affected by radiation, is a very complex procedure that involves several parameters related to the device under test (DUT) and the exposure environment. When it comes to evaluating a component's radiation sensitivity, the most important metrics are its cross-

section (the area of the device that is sensitive to particle hits) and the linear energy transfer (LET) threshold for impinging particles to cause an error. Although SRAMs are relatively simple components compared to SoCs or micro-processors, their testing can hide several aspects that can affect their sensitivity estimation and must be taken into consideration. Directives in the form of standards, such as the Joint Electron Device Engineering Council (JEDEC) [3–5], provide fundamental guidelines for the testing of electronic devices. For SRAMs, these guidelines are mainly focused on static mode testing while displaying some complementary notes on dynamic mode testing. In the following paragraphs, the details and importance of each testing mode are analyzed, and various methods related to the dynamic mode test are presented. Although there are different methods to evaluate the sensitivity of electronic devices to ionizing radiation, such as accelerated testing, simulation testing, and real-time testing, the main focus of the current study is accelerated testing.

### 4.1. Static and dynamic mode tests

Considering a simple level of abstraction, SRAM operation can be classified into two distinct modes: **static mode** (retention) and **dynamic mode** (read/write access). This abstraction is based on the major differences of the behavior of SRAM cells and controlling logic under these two modes. In figure 2, the transistor model of a 6 T SRAM cell is depicted. In static mode, SRAM cells perform data storage: the access transistors of the cell (PG\_BL and PG\_BLB) are OFF, and the inverter loop is in a state of equilibrium with respect to the stored information (e.g. one node at logic '1', the other at logic '0'). As introduced in section 3, when the cell is accessed for a read operation, the access transistors are activated and the differential voltage between the two bit lines is sensed by the differential sense amplifier, which returns either a logic '0', or a logic '1'. During a write operation, the bit lines are charged accordingly, and with the opening of the access transistors, they force either the preservation or the flipping of the stored information on the inverter loop. The activation of the peripheral circuitry of the SRAM (address decoders, write drivers, pre-charge circuitry, etc), the weakening of the inverter cell loop (read operation), and other phenomena typical of the dynamic operation mode, do not occur in the static operation mode. Conversely, when in static mode, the cell is in retention, which for many cases (especially for low-power SRAMs) means that the voltage in the memory array approaches its threshold limit, reducing the static noise margin of the cell. These differences make the cells more or less susceptible to SEUs such as SBUs, MCUs, MBUs, and SEFIs. Consequently, it is essential to differentiate the modes of testing depending on the level of SEU sensitivity of the memory in static and dynamic modes.

**4.1.1. Static mode.** Static mode testing is one of the most fundamental testing methods for the vast majority of memories, especially SRAMs. Static mode testing is described as the key test method by various standards, and requires the writing of memory with a known data pattern

prior to exposure to the radiation source (natural/real-time, accelerated, etc). Following radiation exposure, the memory is read back to check for possible bit-flips. It is important that the data background is stored on the memory prior irradiation to avoid ‘dynamic’ errors during the writing process.

Static mode testing has a rather stable memory response in terms of sensitivity. Since the only part of the memory affected is the cell array and not the periphery, all errors are classified into two major categories, which are easy to distinguish and define error probability, as opposed to dynamic mode testing, which has several different sources and types of errors. The two major categories of errors in static mode testing are SBUs and MCUs. An SBU occurs when a particle impinging the SRAM induces a parasitic charge either through direct ionization (heavy ions, alphas, low-energy protons) or indirect ionization (neutrons, protons), and this charge flips the bit stored inside the SRAM cell. On the other hand, an MCU results from the same phenomenon but the parasitic charge affects multiple cells that are topologically adjacent in the memory array.

During static mode testing, the choice of the data pattern depends on the type of test and the depth of analysis that must be achieved. Typical sets of data backgrounds are as follows: **solid 1** (all ‘1’s), **solid 0** (all ‘0’s), **checkerboard**, and **inverse checkerboard**. Comparison between the solid 1 and solid 0 data patterns reveal relations of stored information (logic ‘1’ or ‘0’) with the sensitivity of the cell using intra-die variations, or resistive/bridging defects within the cells or the memory array. Checkerboard and inverse checkerboards may reveal differences in the overall response of the memory array, but also differences regarding the shapes and sizes of MCUs, as shown in [13].

**4.1.2. Dynamic mode.** Although a basic methodology is provided for the dynamic mode testing of memory devices in the various standards describing radiation testing, no detailed guidelines are given, and moreover, no special cases are considered regarding the memory under study and its respective technology. Such guidelines cannot cover all types of memory devices when operating in dynamic mode because each type of device has its own sensitivity that also depends on the access pattern (sequence of read/write operations). A certain access pattern may stimulate (stress) one device and leave another without any stress effect. As mentioned earlier in this article, when the memory operates under static mode, only the cell array is susceptible to SEEs; when in dynamic mode, other types of SEUs may occur besides typical SBUs and MCUs, such as SEFIs and SELs. This is because additional regions of the memory are activated, and thus become vulnerable to impinging particles. For example, the injection of a parasitic current in the address decoder during a write operation may result in storing data in wrong memory locations.

#### 4.2. March tests

Finding the proper testing scheme to stimulate a memory device under its typical, best-case, or worst-case scenarios, is

**Table 1.** Marching test algorithms.

Name	Test
March C-	{ $\uparrow(w0); \uparrow(r0, w1); \uparrow(r1, w0); \downarrow(r0, w1); \downarrow(r1, w0); \uparrow(r0)$ }
Mats+	{ $\uparrow(w0); \uparrow(r0w1); \downarrow(r1w0)$ }
mMats+	{ $\uparrow(r0w1); \uparrow(r1w0)$ }
Dynamic Stress	{ $\uparrow(r1, w0, r0, r0, r0, r0, r0); \uparrow(r0, w1, r1, r1, r1, r1, r1); \uparrow(r1, w0, r0, r0, r0, r0, r0); \downarrow(r0, w1, r1, r1, r1, r1, r1); \downarrow(r1, w0, r0, r0, r0, r0, r0); \uparrow(r0, w1, r1, r1, r1, r1, r1)$ }
Dynamic Classic	{ $\uparrow(w0); \uparrow(r0); \uparrow(w1); \downarrow(r1)$ }

not evident when operating in dynamic mode. March algorithms are currently used in the manufacturing process because they are capable of detecting faults in memory devices, such as bridging faults, stuck-at faults, and coupling faults. They are preferred for their efficiency and low complexity. Depending on the type of memory, different algorithms are preferred based on their efficacy, and thus, some algorithms are expected to be applied in SRAMs while others in different types of memories, such as dynamic random-access memory (DRAM) and flash memory. Since March algorithms stimulate memory devices to reveal manufacturing defects, provide a suitable functional test, and can be tuned to operate both the typical and worst-case scenarios of the memory’s operation, they are the perfect candidate for radiation dynamic testing.

Table 1 shows a list of the March algorithms introduced in various works by the authors, such as the Dynamic Stress (March DS), the March C- and the Dynamic Classic algorithms.

Each March algorithm is constituted by several elements, each of which entails a series of operations (read or write). Each element has a given addressing order of execution: the arrow at the beginning of each element indicates the addressing order, i.e., from the highest memory address to the lowest ( $\downarrow$ ), and vice versa ( $\uparrow$ ). The operations of each element are applied to each address location (word) before proceeding the next. This means that all operations of the element are applied to a single word before the address counter of the tester is increased, or decreased, depending on the direction ( $\downarrow$  or  $\uparrow$ ) of the element. A semicolon separates the elements of the algorithms and each element has its operations enclosed in brackets. For example, the fourth element of March C-  $\downarrow(r0, w1)$ , has an addressing scheme starting from the uppermost address and applies a ‘read ‘0’’ followed by a ‘write ‘1’’ operation to all memory locations. This means that the tester reads a single word and expects to receive a zero pattern, after which it writes all the bits of the same word with logic ‘1’. Once these two operations are finished, the tester proceeds to the next word and applies the same pattern.

For all algorithms in table 1, the data background stored and read from the memory is either a solid '0' or a solid '1', and the swapping from '0' to '1' (or the opposite) stresses (by increasing the switching activity) some peripheral circuitry of the memory, such as I/O buffers. Other parts of the memory can be stressed as well, such as the address decoders. For example, the address decoder can be stressed by applying an addressing sequence in which most of the bits change at each access, strongly enhancing the switching activity of the address buffer and decoders [2]. Depending on the given March algorithm, a strong stress factor can be induced to the memory, such as with March DS, while others, like Dynamic Classic algorithm are less stressful when not properly modified. As demonstrated in [18], the algorithm March DS, induces stress to the SRAM cell by applying sequences of read operations in the same locations. When made sequentially, the read operations progressively reduce the static noise margin of the cell by degrading the voltage level of the nodes. This is due to the connection, during access, of both cell nodes (one at '0' and the other at '1') to the bit lines that are pre-charged to VDD. Furthermore, a similar effect is obtained by applying a proper addressing sequence when the memory architecture is known. During a read/write access, all the cells belonging to the same word line are indirectly selected (sharing the same word line command) and undergo to a stress similar to an actual read action. This phenomenon is known as read equivalent stress (RES) and is described in [19]. Now, by using the 'word line after word line' (fast row) addressing order in a common March test (e.g. March Classic or March C-) sequence of multiple RES actions, we created an effect similar to that seen with March DS. If the architecture of the memory is unknown, the actual address order is also clearly unknown due to address scrambling schemes and word line segmentation.

Besides the stress induced at the cell level and at the periphery of the SRAM when applying March algorithms, additional stresses can result from the activation of several memory electrical regions. By applying several March algorithms, it has been observed that some devices are sensitive to micro-SEs. More specifically, in [20], it was demonstrated that the application of dynamic tests results in biasing of the SRAM array under a certain voltage that makes it sensitive to SEs. Many SRAM memories have specific powering schemes that keep the entire array in low power mode (low voltage) when in retention mode. The COTS SRAM memories considered in next sections use this type of power scheme: during retention, the cells are fed at low voltage to prevent the triggering of latch-up phenomena, and the access of a word for a read or a write operation biases an electric sub-block of the memory to the nominal voltage, making it vulnerable to SEs. SEs appear above a certain threshold voltage that allows a parasitic PNP structure to be activated when an impinging particle induces a current. This results in the loss of all information of the cells belonging to this block since they enter into a meta-stability state. Since the remaining part of the array is biased at low voltage, the SE cannot propagate to the full array, and thus this phenomenon is called micro-SEL. Such a phenomenon would not have

been observed if a standard static mode test was chosen for the qualification of this component.

#### 4.3. Advanced address and data background stimuli

We have demonstrated the main principles behind dynamic mode testing using March algorithms. While some of the algorithms, such as March C- or DS, are rather stressful for the memory and can result in a maximized cross-section, other elements, such as Dynamic Classic, are less stressful and can lead to smaller sensitivity. These differences result from the combination of operations and the switching activity each one induces to the periphery and cell array. To further enhance or reduce the stress of the SRAM array and periphery, we propose some additional tests in the following paragraphs. These tests complement the existing March algorithms and affect the stress induced to the address decoders, the data buffers, and other peripheral circuitry. Before continuing the presentation of each complementary dynamic technique, it is important to recall that SRAM memories, except bit interleaving, usually entail a scrambling scheme of their addresses, and thus the bits of the  $x$  and  $y$  axes of the SRAM memory array are mixed to form a single sequence of bits that construct the address. To apply the following stimuli, it is necessary to be aware of the function implementing the scrambling so that the breaking of the address to  $x$  and  $y$  values of the physical location of cells is feasible. Below, some stimulation techniques for the dynamic test mode are exposed [21]:

**4.3.1. Fast row.** The fast row technique implies addresses being accessed during a March algorithm in an increasing order following a horizontal direction with respect to the physical location of the cells. More specifically, the cells are accessed from the leftmost to the rightmost on the same line, and once the line is fully accessed, the counter proceeds to the upper line. The described scheme is applied when the address of the March element under execution is in ascending order ( $\uparrow$ ), while the inverse is applied when the addressing order is descending. This scheme is expected to further enhance RES occurrence because the cells belonging to the same word line will be indirectly accessed (and stressed) multiple times.

**4.3.2. Fast column.** Following the same principle in a vertical manner, the fast column technique is implemented. With fast column, cells sharing the same bit lines are accessed consecutively from bottom to top and from left to right in the memory array when the addressing order of the March element is ascending ( $\uparrow$ ); the inverse is applied when the addressing order is descending. Although this scheme is not expected to add large stress on the cells of the array, it is expected to induce stress on the power grid of the memory. This stress is induced because of the power lines that are often placed vertically, and as a result, the access transistors of the



power lines are constantly activated, stressing them electrically.

**4.3.3. Random addressing.** The scrambled addresses of the memory devices have a certain level of randomness due to the application of scrambling techniques. However, additional random addressing schemes can be applied to further increase the switching activity of the address decoders or enhance the activation of different regions of the memory power grid. In addition to the stress factor induced by random addressing schemes, an important parameter is the representativeness of a normal operation of the memory, where words are not accessed in a consecutive manner. The random addressing scheme can be implemented using different random number generators. A linear feedback shift register (LFSR) has been used in the case studies presented in the following section.

**4.3.4. Adjacent (Gray) addressing.** So far, many of the presented algorithms act as SRAM stressing mechanisms to obtain the worst-case scenario of the device when tested for radiation effects. Although it is imperative to obtain a worst-case scenario for the operation of a device, it is also important to have a minimum case of errors, under which a low barrier on the device cross-section will be set. The development of an algorithm that can stimulate and sensitize the memory as little as possible cannot only be used to consider the best-case scenario, but can also be used as a mitigation methodology when the memory under study is used in a system. Working in that direction, we proposed the usage of the Gray coding scheme for the address extraction. This is translated in consecutive addresses that differ in only one bit (Hamming distance = 1) when the March algorithm is executed. The change of only one bit each time the address is increased or decreased results in minimum stress (switching activity) to the address buffer and decoder. This principle, combined with the Dynamic Classic test (which has the lowest data buffer activity since all elements have a single operation), results in the least possible stressful scenario for dynamic mode testing.

**4.3.5. Inverse Gray addressing.** This addressing technique inverts the effect of the Gray scheme seen above by maximizing the number of bits that switch at each access. To achieve the maximum stress that can be applied in the SRAM device in terms of switching activity, the combination of data background and address stress is considered. More specifically, the combination of the mMats+ March algorithm combined with an Inverse Gray addressing scheme induces maximum stress to the memory periphery (address buffer and decoders, data buffers). The elements of the mMats+ algorithm have a read operation followed by an inverse data write operation. For example, a 'r0' followed by a 'w1' operation. This maximizes the data buffer switching activity, as seen in many algorithms such as March C-. By simultaneously applying an addressing scheme such as the Inverse Gray, where all the bits of the address except one are inverted every time the address is increased, the switching

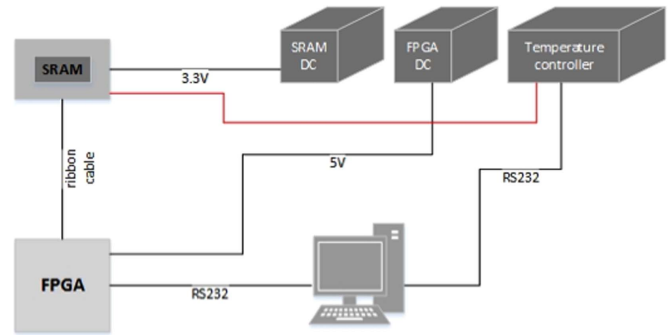


Figure 3. General scheme of irradiation test setup for SRAMs.

activity of the address buffer and decoder is brought to its maximum.

## 5. Experimental results

In the following paragraphs, experimental results are given and analyzed with radiation test campaigns using different types of particle accelerators. Before presenting these results, we describe several details of the setup used for testing SRAM devices.

### 5.1. Experimental setup

SRAM device testing is conducted by driving a standalone chip of the DUT, which is mounted on a dedicated board. This card is controlled by the tester board via cables long enough to keep the tester outside of the beam line. Such a setup assures correct functionality of the tester during irradiation. Figure 3 depicts an example of a generic test setup used for different particle accelerators and different configurations of the setup. The tester board has a field-programmable gate array (FPGA) as the main processing and communication unit, inside which the test firmware is implemented. FPGAs are chosen as testers because of their reliability in the operation flow and the possibility of complete control over the timing of operation execution, among other benefits. Both the tester board and the DUT board are powered with power supplies located in the control room (or at least driven from it), allowing them to power off in the case of a persisting SEL.

For static mode testing, the test firmware writes the data background sequence to the SRAM device prior to irradiation. After the beam exposure is completed, it reads back the data and compares them to the initial data pattern. In the case of an error, the tester sends all the necessary information for data processing to the control computer. More specifically, the message is composed by an initiating sequence that indicates the DUT code, the address of the erroneous word, the erroneous word itself, and finally, the information regarding the applied test. In static mode tests, the expected data background is sent, while in dynamic mode tests, made through March algorithms, the element and operation at which the error was located is given (e.g., the third element and first operation of the March C- algorithm, 'r1'), as well as

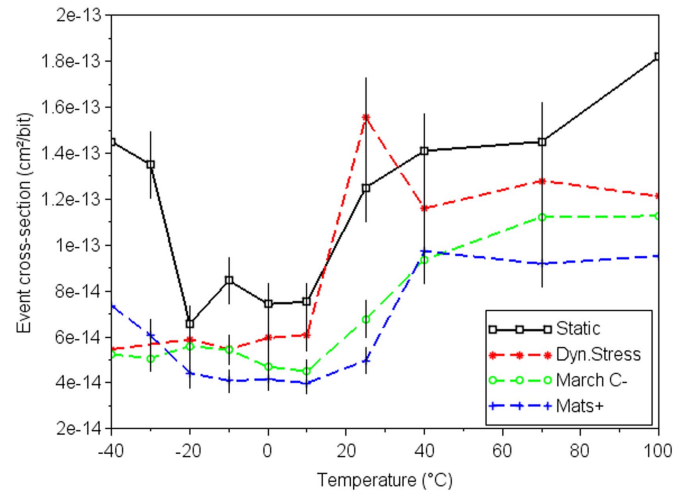
the timestamp of the error. An essential parameter of observed SEU data processing is the knowledge of the DUT scrambling algorithm. Without knowing the actual physical location of the SRAM cells in the memory array, it is very difficult to distinguish between SBUs and MCUs, and also difficult to understand the origins of larger events (which we will later demonstrate as occurring during dynamic mode testing), such as SELs and SEFIs.

Adapting the March algorithms for radiation testing is a straightforward process. The tester must implement a finite-state machine (FSM) which, depending on the algorithm, applies the required operations and elements to the SRAM under test. Since the read pattern is compared with the expected pattern, the read operations of the March algorithm (except for stimulus actions) also work as verification elements of the test. For example, for a March element like  $\downarrow(r0, w1)$ , the read '0' operation will read the contents of an SRAM word and compare them to a 'golden reference' word with all its bits being '0's. In the case of an upset, a message described earlier is transmitted to the control computer. For both static and dynamic mode tests, it is imperative to record all addresses and contents of the failing words, and not use an internal counter when testing SRAMs for detecting and identifying MCUs, SEFIs, SELs, and other large-scale events.

Although stimulating SRAMs using various testing techniques is important to consider when performing radiation testing, it is not the only factor that can affect device sensitivity. For example, temperature variations can have an effect on SRAM device performance. We used a temperature controller to control temperature variations when placing SRAM devices under the beam. A feedback loop composed of a foil heater, a thermocouple as a temperature sensor, and a controlling instrument, were used to achieve high temperature variations. The sensor relayed the current temperature to the controlling instrument, which would increase or decrease the input current to the foil heater to achieve the target temperature. Low temperature variations can be achieved by inserting the DUT along with the tester FPGA in a cryogenic chamber filled with argon gas (permitting temperature decreases below 0 °C), preventing the condensation of water vapor on the electronic devices. Due to the small size of the chamber, for our experiments, a dedicated board embedded the SRAM DUT and the tester FPGA. The tester was always kept far away from the beam line.

The exposure of the device's die depends on the type of particles used to test the DUT. For heavy ions or low-energy protons, the DUT is inserted into a vacuum chamber, and it is necessary that the top part is delidded. The linear energy transfer (LET) of these particles is not sufficient to achieve high effective ranges, and thus cannot reach the sensitive region of the SRAM under study if the package is not removed. To change the DUT in a relatively easy manner when dose levels are high, chip sockets are used to hold the DUT.

To demonstrate the advanced test methods presented above in real experimental conditions, results from different irradiation campaigns are presented in the following paragraphs. The DUTs were a 32 Mbit 90 nm asynchronous



**Figure 4.** Atmospheric neutron 90 nm SRAM event cross-section (XS) as a function of temperature. The applied tests are the Dynamic Stress, Mats+, C- and a checkerboard static mode test. The  $1\text{-}\sigma$  standard deviation is indicated by error bars, and was always lower than 15 %.

COTS SRAM (CY62177EV30 MoBL) and a 16 Mbit 65 nm asynchronous COTS SRAM (CY62167GE MoBL), both from Cypress Semiconductor. During all tests, the DUTs were powered at their nominal supply voltage (3.3 V). It is important to note that the 90 nm device is a stack of two dies. When heavy ions and low-energy protons are considered, it is essential to not consider the errors coming from the bottom die (or to properly account for energy loss in the overlayers). This is due to the fact that very few heavy ions can actually reach the bottom die since for most of them have a significantly smaller effective range than the width of the die. This topic will be detailed in section 6. Thus, the particles that cause upsets in the lower die cannot be considered for study because they will have different LETs than expected. This is not the case for high-energy proton and neutron irradiation since the cut-off factor for the particles is rather small and they are not affected by the upper layer. In the next subsections, we will introduce and analyze experimental data obtained through irradiation made with neutrons, heavy ions, and protons, respectively.

**5.1.1. Neutron irradiation.** The first set of results presented comes from experimental campaigns using neutron-induced radiation. These experiments were conducted at the ISIS facilities of the Rutherford Appleton Laboratory in Didcot, UK [22], using the VESUVIO instrument. Neutrons have energies ranging from 10–800 MeV that are very close to the atmospheric spectrum. The SRAMs under study are the aforementioned 90 nm and 65 nm COTS SRAMs. Figure 4 shows the results obtained when testing the 90 nm SRAM under temperature variations.

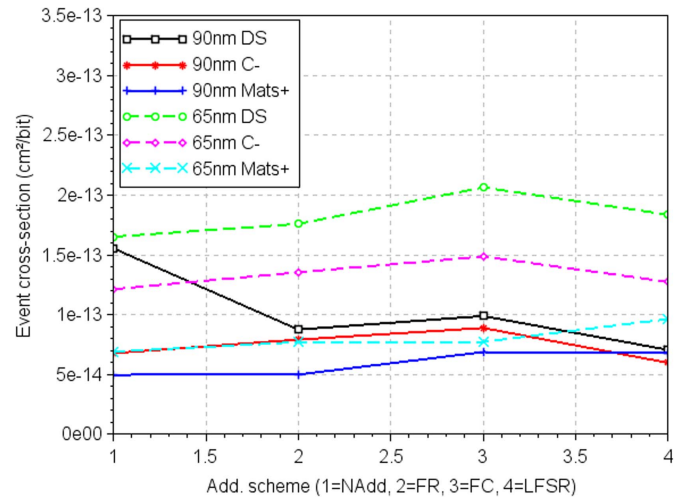
The calculated event cross-section (XS) of the 90 nm SRAM is depicted for different tests under study (static mode, March DS, March Mats+, and March C-). Before proceeding to result analysis, it is essential to describe the event cross-section calculation. As aforementioned, during irradiation,

several different types of single events can occur in an SRAM, such as SBUs, MCUs, SEFIs, or SELs. Each time such an event occurs, it must be recorded. By processing the record of all events occurring during a beam run (address, bits failing, timestamp, etc.), we can distinguish all large-scaled events that affect a large population of bit-flips. This topic will be detailed in section 7. When referring to the probability of having a failure event (be it either an SBU, MCU, micro-SEL, or SEFI) per incident particle, we call it an event XS. When referring to the probability of having a cell upset per incident particle, we call it an SEU XS.

The equation for the event XS per bit is given below.

$$\sigma_{event} = \frac{\#events}{fluence \times nb\_bits\_memory} \quad (1)$$

Analyzing the obtained results, we can see that the March DS algorithm shows a higher cross-section with respect to the other March algorithms, while the March C- remains relatively high. As explained earlier, the DS algorithm is expected to significantly sensitize the array as a result of RES action. Another observation made from the results is that the static mode cross-section seems to be higher than that in the dynamic mode. This can be explained by two main reasons. When the cells are in static mode (retention), they are operating in low-power mode, and thus, the voltage applied to the memory array is decreased, increasing the cells' sensitivity. Additionally, when the March algorithms are applied, a certain level of masking during the write operations is expected. However, this is minimized because of the order of operations in the elements (first read, then write). The memories under study, and more specifically the 90 nm SRAM, have a very unique powering scheme that makes them sensitive to localized SELs (micro-SEL). These events, along with certain types of SEFIs, have resulted in massive bit failures during radiation testing. These large clusters of upsets have been treated with an in-house developed software tool that permits grouping of all bit-flips related to the same event. The grouping of bit-flips is based on their physical location in the array and on their time of occurrence. Large events (up to 100 000 bit-flips) have been observed only during dynamic mode testing, and thus, it is to be expected that the grouping might be unable to correctly cluster all failing bits. Thus, large differences between dynamic mode tests are to be expected depending on beam intensity and the occurrence of certain large-scale events. On the contrary, the 65 nm memory does not show such large-scale events, making data processing more simple and showing that the device is significantly more robust. This is expected since it is the updated version of the 90 nm device, and thus, several major improvements have been introduced to its architecture. The increase of the XS during the  $-40$  °C test results from fast neutron flux calculation errors due to concurrent experiments. The setup for low temperature testing was one of the first installed in the ISIS facilities for SRAM testing, and thus some errors were to be expected in fluence calculations. The results from temperature variation show an overall increase in the cross-section as temperature increases, but is not of significant



**Figure 5.** Atmospheric neutron testing of 90 nm and 65 nm SRAMs with various addressing scheme and Marching algorithm combinations. Marching algorithms are the March Dynamic Stress (Stress), March C- (C-), and Matc+. Addressing schemes are the normal addressing-scrambled (NA), fast row (FR), fast column (FC), and random addressing (LFSR).

**Table 2.** Heavy ions and their energies, ranges, and LET.

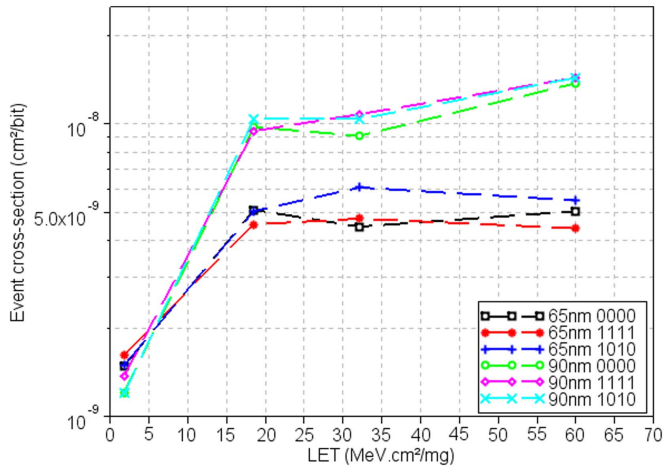
B. Ion	Energy (MeV)	LET (Surface) (MeV/(mg/cm <sup>2</sup> ))	LET (Bragg Peak) (MeV/(mg/cm <sup>2</sup> ))
N	139	1.87	5.92 (191 $\mu$ m)
Fe	523	18.5	29.7 (75 $\mu$ m)
Kr	768	32.2	41.7 (68 $\mu$ m)
Xe	1217	60.0	67.9 (57 $\mu$ m)

importance. Continuing our analysis, figure 5 shows results from testing the 65 nm and 90 nm SRAMs under atmospheric neutrons while several addressing schemes are applied in combination with the March algorithms.

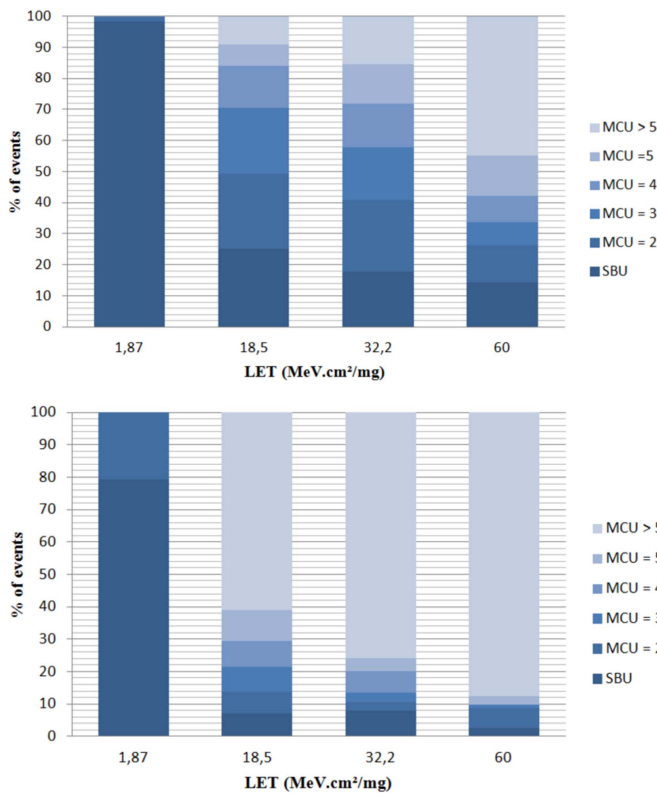
Results reiterate that the March DS algorithm is the most stressful for the memory, and this applies to both the 90 nm and 65 nm SRAMs. The Fast Column scheme has the highest stress factor, while the rest remain at similar levels. Interestingly, the normal addressing-scrambled scheme seems to have a low stress factor with respect to the other addressing techniques.

**5.1.2. Heavy ion irradiation.** As mentioned earlier, heavy ion testing requires chip decapsulation so that the heavy ions reach the sensitive region of the SRAM with a known energy. Test campaigns have been performed at the RADEF facility in Jyväskylä, Finland, with heavy ions at energies ranging from 1.87 MeV mg<sup>-1</sup> cm<sup>-2</sup> to 60 MeV mg<sup>-1</sup> cm<sup>-2</sup>, as detailed in table 2.

Both the 65 nm and 90 nm COTS SRAMs have been tested using static and dynamic mode testing. Figure 6 shows the results on the event cross-section from the 90 nm and 65 nm SRAMs for different data background patterns. From data processing and different static mode tests using different particles, two types of events appear: SBUs and MCUs.



**Figure 6.** Event cross-section for static mode testing of the 65 nm and 90 nm SRAMs under heavy ions.

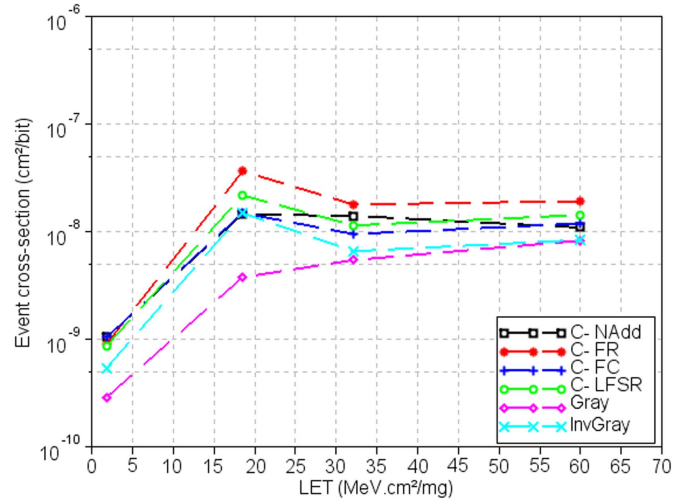


**Figure 7.** Distribution of MCUs with respect to different ions for the 90 nm and 65 nm SRAMs.

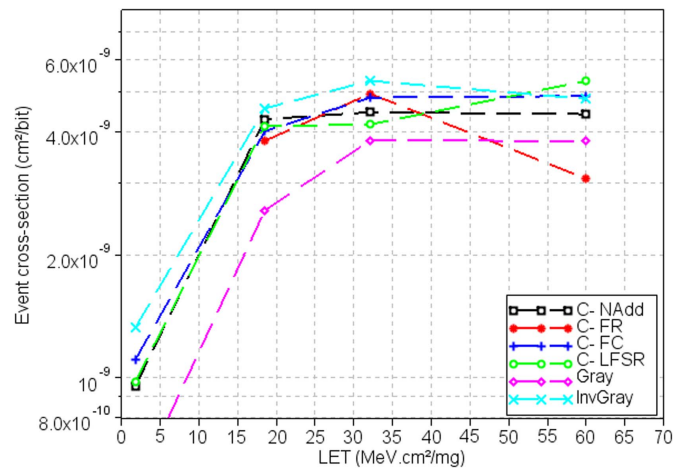
Figure 7 shows the distribution of MCUs with respect to different ions.

MCUs appear and eventually dominate the distribution of events for higher values of LET for the 65 nm SRAM, but not for the 90 nm SRAM. Similar results have been found in [23]. This results from the shrinking of sensitive node distances while the area at which the parasitic charge is distributed remains the same. As a result, a higher number of cells is affected by the same particle.

Dynamic mode testing has also been applied for both SRAMs under heavy ions. Focusing the analysis on the addressing and data background schemes introduced above,



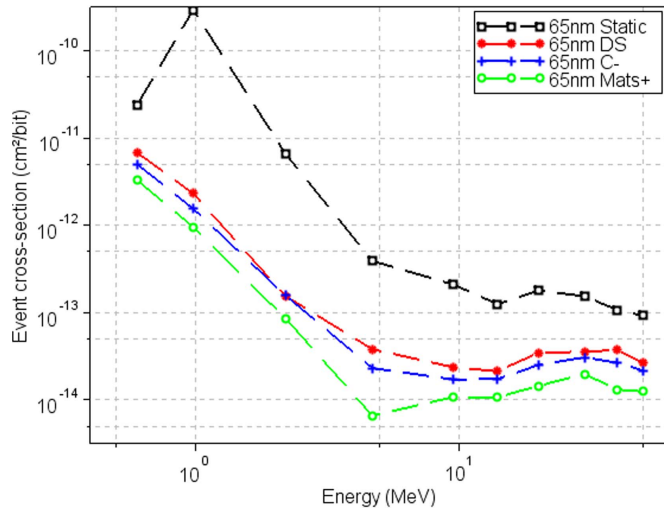
**Figure 8.** Heavy ion testing of 90 nm SRAM under various addressing schemes while applying the March C- algorithm. Addressing schemes are the Fast Row (FR), Normal Addressing (NA), Fast Column (FC), random scheme (LFSR), Gray addressing combined with the March Classic test, and inverted Gray (InvGray) addressing combined with the mMats+ March test.



**Figure 9.** Heavy ion testing of 65 nm SRAM under various addressing schemes while applying the March C- algorithm. Addressing schemes are the Fast Row (FR), Normal Addressing (NA), Fast Column (FC), random scheme (LFSR), Gray addressing combined with the March Classic March test, and inverted Gray (InvGray) addressing combined with the mMats+ March test.

application results are given in figure 8 for the 90 nm SRAM and figure 9 for the 65 nm SRAM.

Results from the different addressing schemes show a small differentiation in the sensitivity of the cross-section, similar to what has been observed during atmospheric-like neutron irradiation. During heavy ion dynamic testing, the 90 nm suffers from an increased rate of large-scale events, such as SELs and SEFIs, that make result processing and the clustering of upset bits a complicated process. This then results in many errors due to overlapping of corrupted bits at high particle fluxes. While most of the addressing schemes show similar cross-sections, two can be clearly distinguished. The March Dynamic Classic combined with the Gray addressing scheme, exhibit the lowest possible stress (lowest

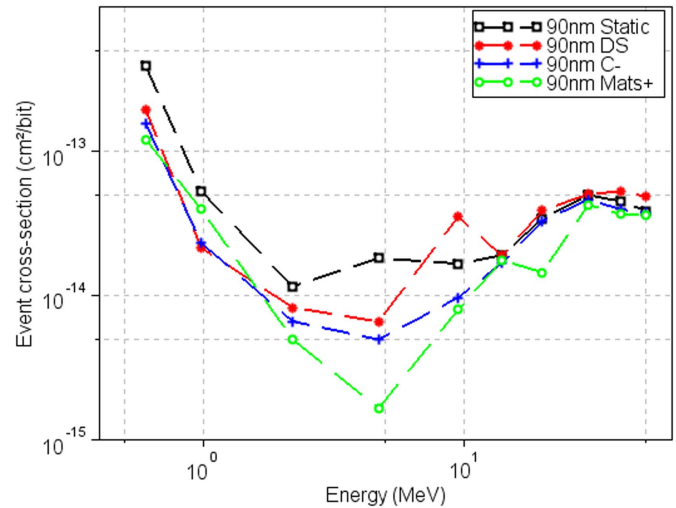


**Figure 10.** Proton irradiation results for the 65 nm SRAM under different March algorithms and static mode testing.

XS) in both devices. This result is in accordance with assumptions made when describing the differences between the applied algorithms. On the other hand, the inverse Gray addressing scheme combined with the March mMats+ algorithm induces increased sensitivity, especially for the 65 nm SRAM. Although the 90 nm SRAM with same combination of algorithms does not show the same trend, we consider that the 65 nm device shows a more stable behavior. Thus, at least for the 65 nm SRAM, this combination of March algorithm and addressing scheme results in the worst-case scenario.

**5.1.3. Proton irradiation.** We also applied our testing methods under proton irradiation because these particles are the major contributor of SEEs in space and particle accelerator applications. Our study includes high-energy protons that are responsible for indirect ionization mechanisms, but also low-energy protons responsible for indirect ionization mechanisms, as demonstrated in [16, 17]. These experiments are based on the theory that low-energy protons contribute to the sensitivity of submicron devices when the nodes start to scale below 65 nm. Experiments have been conducted at the RADEF irradiation facilities, using protons of energies ranging from 0.6 MeV to 50 MeV.

Results obtained from the two SRAM memories (65 nm and 90 nm) are given in figures 10 and 11, respectively. In both cases, static mode tests have been conducted using the checkerboard pattern to consider an average case of memory data background. The 65 nm SRAM shows greater sensitivity to low-energy protons, whereas the 90 nm SRAM shows more robust behavior. According to [15], at the simulation level, the interactions of protons with silicon pass from direct (low energy) to indirect when between 2 MeV and 10 MeV. We observed this, especially during static mode testing. Both memories show higher sensitivity at low energies, and the 65 nm SRAM has a peak at 0.98 MeV. Rising for up to three orders of magnitude, this peak indicates the passage between indirect and direct ionization. Previously, we have seen that



**Figure 11.** Proton irradiation results for the 90 nm SRAM under different March algorithms and static mode testing.

the neutron-induced cross-section for the 65 nm SRAM is in the order of  $10^{-13}$  cm<sup>2</sup>, and escalates up to  $10^{-9}$  cm<sup>2</sup> for heavy ions. For low-energy protons, the 65 nm energy peak reaches that of the heavy ion cross-sections, denoting the transition between indirect and direct ionization, the latter of which has a significantly higher probability of inducing an upset than the former. Considering the applied algorithms, results support that the March DS induces the highest sensitivity to both SRAM devices. Additionally, the statement that static mode tests show larger event sensitivity than dynamic mode tests is confirmed for protons. This illustrated the validity of static mode tests, regardless of the type of particles used for the test.

## 5.2. Differences concerning technology node/architecture

The testing techniques analyzed in this paper cover the vast majority of the events that can be observed as a result of ionizing radiation on SRAM devices. Several phenomena have been revealed thanks to dynamic mode testing and its ability to stress the periphery of the memory. SELs and SEFIs are among the major revelations of the 90 nm SRAM when tested under dynamic mode. This phenomenon is extremely critical as it impacts thousands of cells, and thus must be considered when developing a system. So far, results analysis has focused on the efficiency of each algorithm to increase or decrease device stimulation, and therefore increase or decrease its sensitivity. We can also observe the differences between the technology nodes of the studied memories. The 90 nm SRAM suffers from large-scale events, such as SELs and SEFIs, when tested under dynamic mode. Part of this problem is due to its powering scheme that divides the memory array into large blocks, which are biased at nominal voltage when accessed for a read/write operation. Conversely, the 65 nm version of the same memory, does not suffer from such events. This is related to the fact that several improvements have been made, especially related to the time window that each electric 'block' is powered at nominal voltage. This window has been significantly decreased,

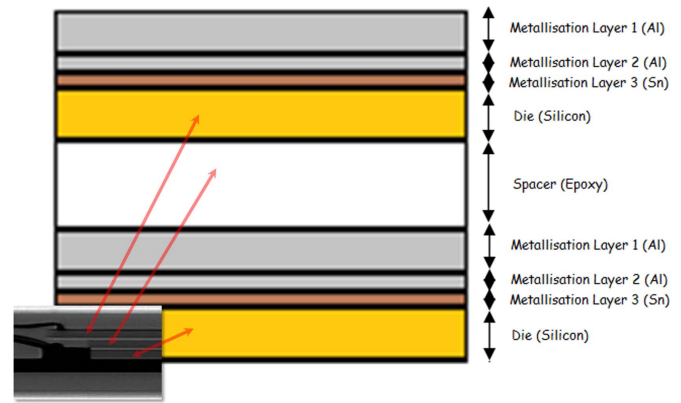
resulting in a significantly lower probability of an SEL occurrence.

As explained in the heavy ion results section, the MCUs of the 65 nm SRAM have a larger number of participating bits w.r.t. the ones of the 90 nm SRAM. The main reason behind this phenomenon is the distribution of charge among more sensitive nodes in the 65 nm device. To study this, it is imperative that the devices are tested under static mode test, which eliminates the probability of having other types of events that could mislead results, and keep only the SBUs and MCUs that occur on the cell array. An interesting observation is that although the node changes between the two devices, for most cases, and especially during static mode testing, the cross-section remains at the same levels. As the node shrinks, two opposite phenomena occur. One is the reduction of the sensitive node size—the PN junction, which reduces the funneling phenomenon and carrier drift. This mechanism works toward strengthening the cell against parasitic currents. On the other hand, a smaller node means a smaller critical charge, more defects on the transistors, and a smaller distance between sensitive nodes. For the above reasons, a smaller node also has a larger sensitivity to parasitic currents. These two phenomena work against each other, resulting in a cross-section of the smaller node (65 nm) that becomes similar to that of the larger node (90 nm).

The above testing methods have been tailored for the evaluation of SRAM devices under ionizing radiation. The March algorithms, and addressing and data background techniques have been designed while considering the weaknesses of SRAM devices, bit cells, and the periphery. The same test techniques might not be as stimulating in other types of memory devices as they are for the SRAMs and, potentially, might even mask failure. As explained in [24], ferroelectric RAMs (FRAM) are more sensitive when a write operation occurs, especially with a write operation that changes the stored information ('1' to '0' transition). As a result, the DS March algorithm, which was proved to be amongst the most stressing algorithms for SRAM devices, has the opposite impact on FRAMs. Considering this example, it becomes clear that each type of memory has its own particularities that must be thoroughly studied before structuring a test methodology.

## 6. Impact of stacked layer structure

SRAM devices, like in system in package (SiP), may be fabricated with several layers of dies [25]. This is the case of the 90 nm Cypress 32 Mbit SRAM (CY62177EV30 MoBL) that the authors have often used as test vehicle [26]. This memory is composed of two identical 16 Mbit SRAM dies stacked on top of each other, as can be seen in figure 12 (an x-ray picture and the related scheme). Taking x-ray photos and considering internal structural configuration was essential to better understanding our test results, as will be shown later in this section. This x-ray picture was made to prepare the delidding of the chip packaging (chemically performed) before heavy ion and low-energy proton irradiation. The



**Figure 12.** 90 nm SRAM x-ray image showing that the memory is constituted of two layers vertically stacked with an additional spacer between the two dies.

**Table 3.** Heavy ions cocktail and their energies and ranges in Silicon.

Ion	Energy (MeV)	LET (MeV. $\text{cm}^2\text{mg}^{-1}$ )	Range @ Bragg Peak ( $\mu\text{m}$ )
C	131	1.1	292
Ne	235	3	216
Ar	372	10.2	117
Ni	567	20.4	100
Kr	756	32.6	92
N	60	3.3	59
Ne	78	6.4	45

delidding operation is important because in accelerated test facilities for this kind of particles the range of penetration of the impinging particles is otherwise too small to penetrate and reach the sensitive area of the memory plan. Another peculiarity of this memory is its power scheme, which consists of only powering up specific blocks of the memory die when accessed for an operation. This reduces power consumption. The nominal voltage supplied to the memory is 3.3 V, whereas the core voltage varies from 1.65 V to 0.8 V, depending on whether the specific region is active or in standby mode.

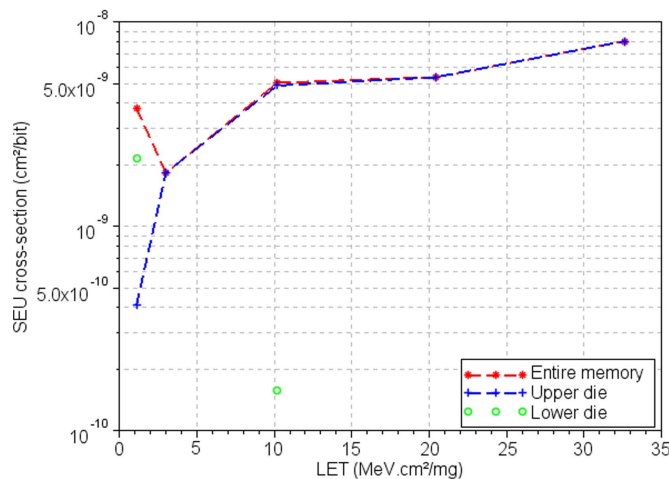
The DUT was tested at two different facilities:

- RADEF [27] in Jyväskylä (Finland) for the proton testing at energies below 50 MeV, which are considered low energies (tests being usually carried up to 200 MeV for SEE characterization of components for space applications).
- Heavy Ion Facility (HIF) [28] in Louvain-La-Neuve (Belgium) for heavy ion tests.

The heavy ion cocktail used in our experiments allowed for testing from an LET of  $1.1 \text{ MeV}\cdot\text{cm}^2\text{mg}^{-1}$  to  $32.6 \text{ MeV}\cdot\text{cm}^2\text{mg}^{-1}$ . In this case, the LET is the ionizing energy deposited by the incident particle per unit length and per material density. As shown in table 3, the range of those heavy ion particles at which the ionizing energy is maximum (Bragg peak) ranges from  $45 \mu\text{m}$  to  $292 \mu\text{m}$ . Similarly, in table 4, the DUT was tested under monoenergetic protons

**Table 4.** Proton energies and their ranges in silicon.

Energy (MeV)	Range
0.6	8.0 $\mu\text{m}$
0.98	16.0 $\mu\text{m}$
2.2	55.5 $\mu\text{m}$
4.7	194.5 $\mu\text{m}$
9.5	649.0 $\mu\text{m}$
14	1.0 mm
20	2.0 mm
30	5.0 mm
40	8.0 mm
50	12.0 mm

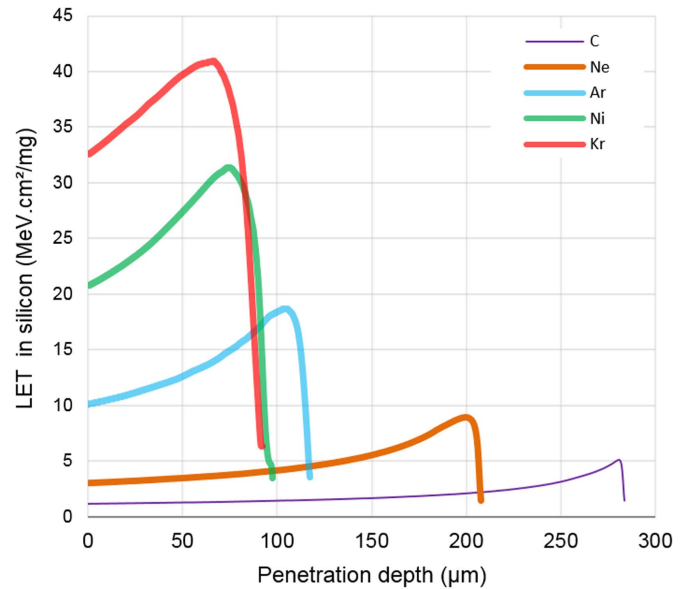
**Figure 13.** SRAM cross-section under heavy ions and static mode test calculated while considering: the entire memory (black box); bit-flips in the upper and lower die but matched to the whole memory. The 1- $\sigma$  standard deviation is always under 15 %.

ranging in energy from 0.6 MeV to 50 MeV. Protons had a range increasing with the energy from 8  $\mu\text{m}$  to 12 mm, well beyond the thickness of the DUT.

For these test campaigns, various test methods presented in the previous section were used to test the current SRAM memory. However, for the scope of this paper, we will only consider results from the static test mode since it does not trigger large-scale events such as SEFIs and SELs that could mislead the study, and thus make it the best choice for exploring the impact of a stacked layer under heavy ion and low-energy proton testing.

### 6.1. Test results

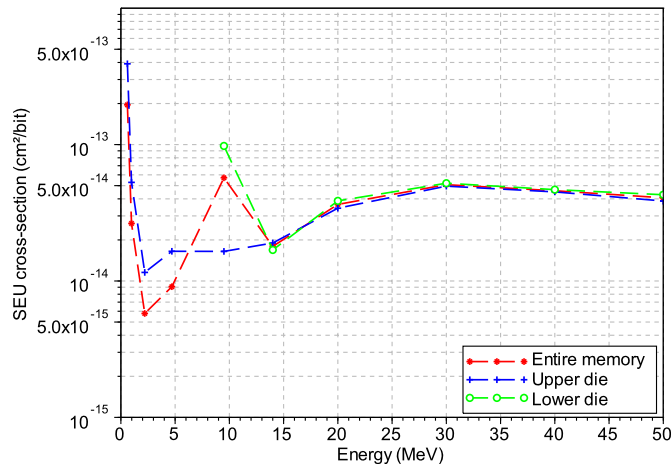
Typical cross-sections, as presented in the previous section, depend on energy (for protons) and LET (for heavy ions). In general, component cross-sections increase with energy (or LET) until it reaches a saturation point with no further substantial increase. Results for the dual-layer 90 nm SRAM were different from this trend. As shown in figure 13, the cross-section considering the entire memory (32 Mbit of memory cells on the same plane (red dashed line)) shows an unexpectedly higher cross-section at the lowest LET of the heavy ion cocktail.

**Figure 14.** High penetration ion Bragg curves in silicon.

Thanks to information provided by the manufacturer of the memory device, it was possible to discriminate between detector error belonging to log upper and lower dies. Considering only the upper die (blue dashed line), the cross-section curve shows a more typical cross-section tendency. In fact, for the lowest LET value corresponding with the carbon ion (C), most bit errors were recorded on the lower die, as shown by the green circle at a LET of 1.1  $\text{MeV}\cdot\text{cm}^2\text{mg}^{-1}$ . For the sake of precision, error was also recorded on the lower die at 10  $\text{MeV}\cdot\text{cm}^2\text{mg}^{-1}$  (second green circle), but this may be explained by the longitudinal straggling of the heavy ion (due to statistical variations in particle ranges). For the remaining LETs, no errors were recorded on the lower die.

It may be counter-intuitive to realize that errors are recorded on the lower die with only the lowest value of LET (C). The explanation comes after having a closer look at the physical particle/matter radiation interaction mechanisms. The incident particle along its path within the crossed material does not interact evenly: depending on several parameters, such as particle momentum, its charge, and the charge of the target material, the particle can transmit more or less of its energy to the target material in the form of ionized energy. Figure 14 shows the LET profile of the different particles in the heavy ion cocktail. It can be clearly seen (and this is especially true for the lowest LET particle, C) that the initial ionizing energy deposited in the target material is lower, with an increase to the maximum LET, after which there is a steep decrease until the particle has lost all of its incident energy to the target material. For C, the LET is low enough to penetrate the first memory die without being able to trigger single events; but as the LET increases, the particle interacts more, and when a threshold value of LET is passed, it triggers single events in the lower die.

Hence, the peculiarity of the carbon particle (primarily its energy and charge) produced unexpected results that have been correctly decoded using knowledge of the internal configuration of the memory and understanding basic



**Figure 15.** SRAM cross-section under proton irradiation with static test calculated while considering: the entire memory (so-called ‘black box’ SEU cross-section); upper die only; lower die only. The  $1\text{-}\sigma$  standard deviation is always under 15 %.

radiation particle/matter interaction. In space, the heavy ion particle energy can be several tens of orders of magnitude (or even hundreds of orders) higher, resulting in similar interactions on both dies (more constant LET profile along the path of the particle within the component). Therefore, the current test results should be corrected before estimating error rates for space applications.

Low-energy proton tests produced similar results, as can be seen in figure 15.

Two peaks can be seen when considering the entire memory (red line). The first (at the lowest energy) is due to the direct ionization of protons at those low energies, such as presented in [17]. Nevertheless, the second peak around 9.5 MeV is not usual for a typical SRAM memory cross-section. This unexpected event was seen again after separating the effects on the upper and lower die. In fact, there were no errors at all on the lower die at energies lower than 9.5 MeV, and the peak at 9.5 MeV was present only in the lower die. This appears to be because direct ionization interaction is occurring around this energy on the lower die due higher energy requirements for protons to penetrate deeper into the material.

## 7. Test data processing techniques

### 7.1. Creating bitmaps and clustering upsets

The various memory test setups used in this study produced data in the form of text logs. During irradiation tests, the memory controller detects upsets and sends a message containing, among other information, the logic address and the read value of the corrupted word to the computer. This raw data is not straightforward to analyze, and thus specific software tools process the data and generate various statistics, such as those proposed in [29] and [30].

Creating bitmaps is a good starting point when analyzing memory test data. A bitmap is a graphical representation of the data contained on the memory array, with every pixel

corresponding to a single word or a single bit (for example, a pixel may be colored black if it suffered an upset, and white otherwise). A physical bitmap has its pixels organized in a similar way as the memory cells on the array; to create a physical bitmap, it is required to know how the memory cells are organized, i.e., which address pins correspond to which part of the memory array (line or column).

Typical memory designs are symmetrical and create repetitive patterns, e.g. with all bit lines running vertically, while all word lines run horizontally across the die. In the event of a large-scale data corruption caused by the failure of an internal subsystem (power switches, address decoders, I/O buffers, etc.), the data corruption will appear as a repetitive pattern on the bitmap. By analyzing this pattern, one can deduce what particular subsystems have failed. For example, in [29], the authors generated a bitmap using all test data gathered during several dynamic test runs on the same single memory specimen; the bitmap exhibited a homogeneous distribution of isolated SBUs, except from a single, one-pixel-wide column running vertically over one-fourth of the bitmap. This feature was absent from similar bitmaps generated from static test data, or from dynamic data from other specimens. This indicated that this particular memory had a silent defect affecting one of its columns (bit lines, pre-charge circuit, selection multiplexer, or power switch), which caused the related cells to fail much more often than the rest of the bitmap when accessed under irradiation.

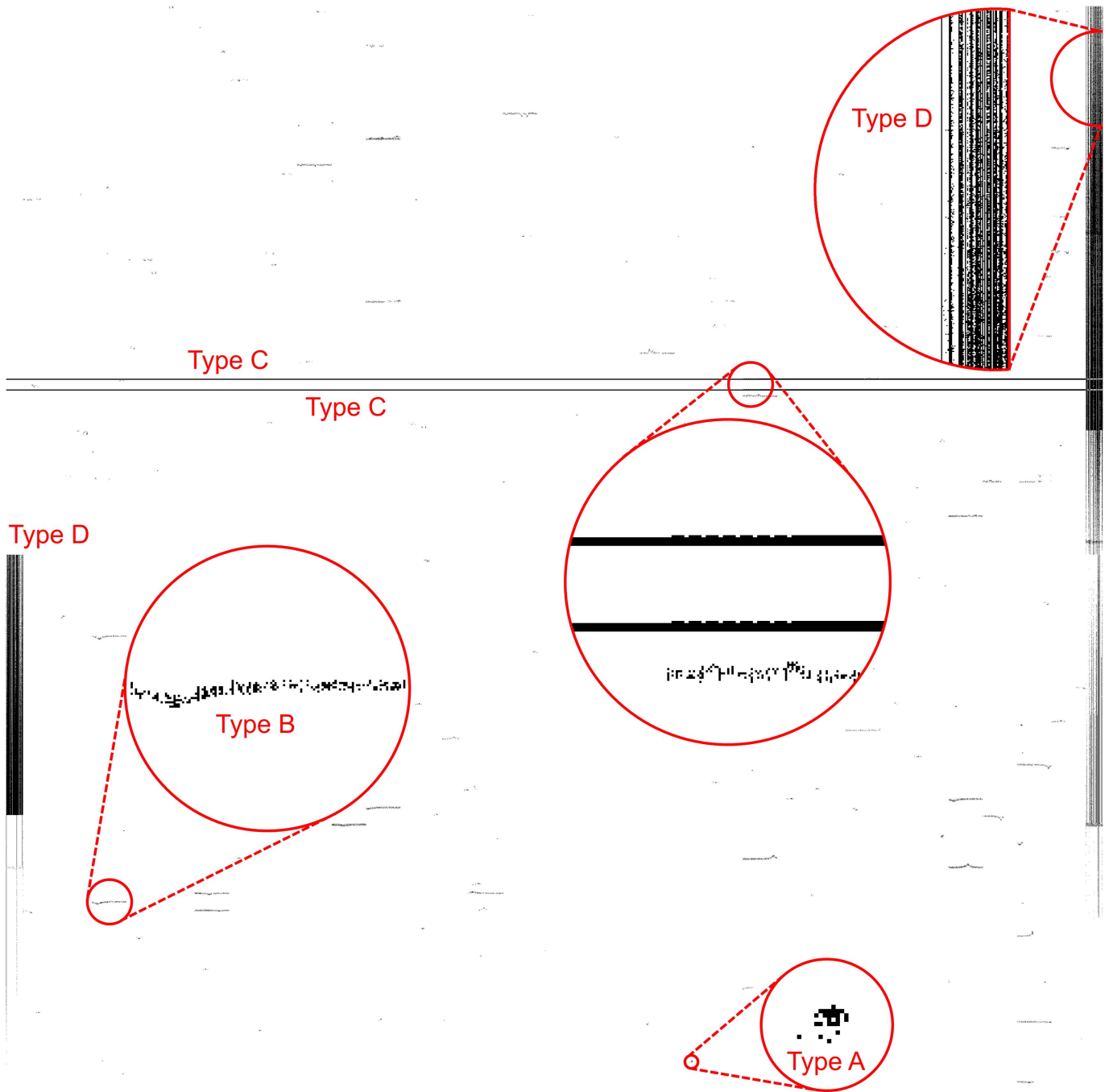
Figure 16 exhibits an example bitmap generated from heavy ion dynamic test data on a 90 nm SRAM. Several small patches and a few large bands are visible where the data has been severely corrupted. A detailed analysis of these different types of error clusters is available in [20], which will be briefly reported here. The smallest patches, barely visible, have been caused by direct heavy ion ionization (type A). The small horizontal patches were caused by limited micro-latch-ups (type B). The wide horizontal bands were very likely caused by a failure of the I/O data buffers (type C), and the wide vertical bands on the edges of the die were probably caused by power switch failure (type D).

Provided that the memory has not suffered too many upsets during a test (that is, that the physical bitmap does not exhibit too many sparse black pixels), it is possible to systematically group together neighboring upsets in clusters. Counting the clusters provides an accurate estimate of the number of SEE that occurred during irradiation.

To achieve this automatic clustering, one has to define a set of clustering criteria. To obtain the best results, these criteria must be tuned while considering the characteristic failure pattern(s) of the memory when subjected to radiation and the type of test (ion species and memory stimulus) that was conducted. Using this set of criteria, the algorithm will identify the cluster SEUs that occurred within the determined physical distance and time frame from each other.

By considering their size and shape, it is possible to automatically label the detected clusters as belonging to a different category of error clusters. For example, if applied to the test data exhibited in figure 16, this clustering algorithm automatically groups the approximately 40 000 SEU as two





**Figure 16.** Example of bitmap obtained by the irradiation of a 90 nm SRAM with heavy ions. Each pixel corresponds to a bit in the memory array, and every black pixel represents a corrupted bit. The image is  $4096 \times 4096$  pixels.

types of D, two types of C, several tens of type B, and a few hundred of type A clusters, while the rest are SBUs.

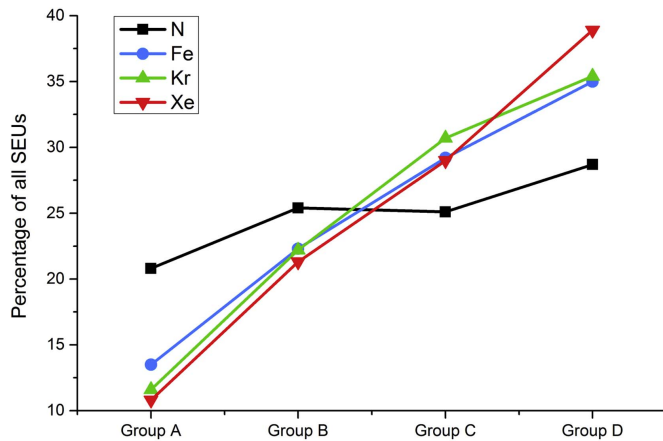
This automatic process can extract information from test data, goes far beyond the information given by a simple upset count, and can be precious to assessing the reliability (in terms of failure rate) of a memory component. A more detailed explanation of the process, with additional examples, is available in [29].

### 7.2. Statistical analysis

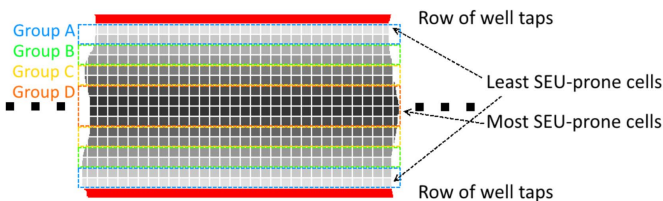
Once the bitmap and the clustering procedure have been applied to the test log, other useful data processing procedures

can be applied to these to achieve a deeper analysis. For example, the tool proposed in [30], which is based on Scilab [31], indexes errors occurring during a test, creates an error database, and generates statistics on the distribution of the corrupted data across arbitrary regions of the memory array. By adequately defining these array regions and comparing their statistics, it is possible to get insight on eventual vulnerabilities of the component that do not generate directly observable large-scale patterns on bitmaps, but nevertheless increase SEE susceptibility of some regions in the memory array.

By using this method, we investigated the eventual impact of the proximity of an SRAM cell to a well tap on its



**Figure 17.** Effect of the distance to the nearest well tap on a cell's likelihood to suffer an SEU, depending on ion species. Group A represents 25 % of the cells that are the closest to a well tap, groups B and C are intermediate groups, and group D cells are the farthest.



**Figure 18.** Representation of a portion of a memory array electric block, showing how the memory cells were divided into four equal groups based on their distance to the well taps.

SEU susceptibility. Well taps are elements of memory design that tie diffusion wells to a reference voltage; the assumption was that nearby well taps could participate in charge collection and limit the disruption of a memory cell in the event of a particle strike. By dividing the memory cells into several groups based on their distance to a well tap, we were able to detect a strong correlation between ion species, the distance from a given memory cell to the nearest well tap, and its susceptibility to suffer from a heavy ion upset. This phenomenon is illustrated in figure 17, which shows, for several ions, the percentage of SEUs detected in zones A, B, C and D, where A is the closest to the well tap and D is the farthest (see figure 18). The fact that the number of upsets decreases with proximity to the well taps suggests that increasing the number of well taps may be a simple and efficient way of increasing a memory component's tolerance to radiation. On the other hand, given an SRAM device, an easy way to increase system reliability is by setting the memory controller to automatically store sensitive data (e.g. command stack, boot info, etc.) in the region closest to the well taps.

Similar analyzes exist in the literature, and further studies can investigate the influence of other functional or architectural parameters on SEU occurrence; for example, positioning the power grid within the memory array, changing the distance of the cells from the power switches, or using different sense amplifiers.

## 8. SRAMs as radiation monitors

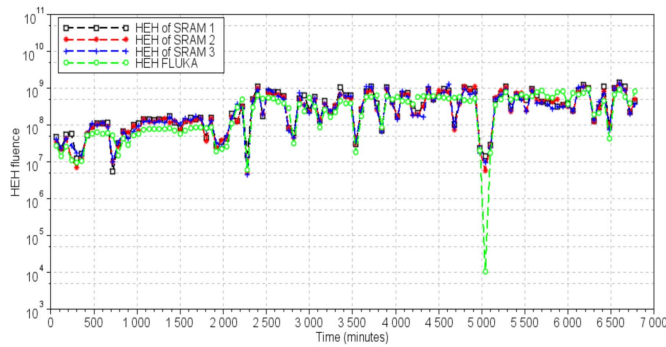
Particle accelerators and colliders produce radiation environments composed of different types of particles with different energies. One of the most important operations that these facilities must ensure is monitoring radiation levels throughout the different zones. This allows for necessary precautions not only with respect to human safety, but also with respect to the reliability of the instrumentation and used electronics. The same principle can be inducted for any environment (space, terrestrial, etc.), in which radiation (natural or artificial) is present.

Systems designed to monitor radiation levels are realized in various manners and integrate several instruments depending on the type of ionizing radiation they measure. When it comes to the effect of radiation on electronics, the metrics considered are usually the particle fluence, the Total Ionizing Dose (TID), the Displacement Damage (DD), and Soft Error Rate (SER). Several detectors can be used to measure the effects of ionizing radiation over electronic devices, with each one usually dedicated to a single metric. Moreover, once characterized under several types of particles and different energy levels, electronic devices like SRAMs can be used as radiation monitors. This is the case for the examples given in the next two sections. The first is related to a particle monitor tested the Large Hadron Collider (CERN), while the second has been used as an atmospheric neutron detector in a natural environment (Antarctica).

### 8.1. High-energy hadron monitor (CERN)

Many environments employ different types of radiation, with various intensity and conditions (e.g., space, high altitude, and accelerator environments). One example of a mixed environment is that at the Large Hadron Collider (LHC) of the Conseil Européen de la Recherche Nucléaire (CERN). The LHC environment is a mixed field composed of several particles such as hadrons (protons, pions, kaons, and neutrons), photons, electrons, and muons, with energies ranging from thermal levels (< 1 MeV) to the GeV scale. The research in [32] integrated SRAM devices as SEU collectors in a LHC-like environment. These SEUs were then used to estimate the intensity of High-Energy Hadrons (HEH) fluence. To achieve an acceleration factor allowing for radiation testing within a reasonable time, the experiment was conducted at the H4IRRAD test area [33], which emulates the internal and shielded areas of the LHC.

H4IRRAD reproduces a radiation environment that approaches atmospheric in terms of particles and energy distributions. At the H4IRRAD irradiation facility, a 20 cm thick concrete wall separates the internal and external zones that mimic the particle spectra of the LHC tunnel and its shielded areas, respectively. The particles composing HEH flux are protons, neutrons, pions, and kaons, which have energies above 20 MeV. Radiation levels inside the H4IRRAD zones were measured using the LHC radiation monitoring system (RadMon) [34] and simulated using the FLUKA code [35, 36]. Below, we briefly present the results from the characterization and testing of the monitor proposed in [32].



**Figure 19.** HEH fluence of a position at the internal zone based on recorded SEUs of the proposed monitors and FLUKA simulations.

The monitors are made of boards embedding three identical 90 nm SRAMs. To minimize large-scale effects (multi-cell upsets) that may make real-time data processing problematic, the SRAMs were tested in static (retention) mode. The use of multiple memory devices within the same monitor accelerates SEU collection and permits cross-checking of data. For example, the graph in figure 19 shows the correlation between the HEH fluence extracted by the three SRAMs in the monitor, and the HEH fluence calculated with FLUKA simulations in the internal zone of H4IRRAD.

These results prove SRAM capability to predict HEH fluence with very good accuracy. The function of the monitor is based on SEU accumulation and their correlation to impinging particles. Although these results are based on the SRAM monitor response in the H4IRRAD environment, the same principles may be applied to various radiation environments with the proper modifications and setup recalibration.

### 8.2. Atmospheric neutron monitor (Antarctica)

The same principles of radiation monitoring-based SRAM devices were used for real-time testing. Although atmospheric-like particle beams are available and provide a good approximation of the natural ground level radiation environment like at ISIS [22] and TSL [37], the spectra variations with altitude, latitude, and location, make this task complicated. In the past, many works have been conducted for the characterization of memory devices using real-time testing methods. For example, in [38] a few Gb of 40 nm SRAMs have been tested, cumulating more than 7000 h of operation at the high-altitude desert Plateau de Bure (2552 m,  $\times 6.3$  acceleration). The collected experimental data permitted the computation of SBU, MCU occurrence, SER extraction, and the study of correlation with simulation level tests. Similarly, experiments using two platforms embedded with 90 nm and 130 nm SRAMs were installed at the Midi-Pyrénées Observatory (OMP, 2885 m,  $\times 8.5$  acceleration) and the city of Puno in Peru (3889 m,  $\times 9$  acceleration) [39].

Here, we present the final part of the work conducted on an SRAM-based platform designed and developed at the Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier (LIRMM) with the support of Institut d'Électronique du Sud (IES) and the Center National

d'Études Spatiales (CNES). This platform was the result of many years of development and study, and it was installed at the Concordia scientific station in Antarctica [40] in 2013. The architectural details of the platform, embedding hundreds of 90 nm SRAMs in a modular scheme, are given in [41]. The experimental results presented a rough estimation of the atmospheric neutron flux at instrument locations, resulting in measuring an acceleration factor of about  $\times 10$  ( $\times 9.81$  expected according to JEDEC standard), with respect to the NYC measurements [42]. Furthermore, the setup of the test benches, with memory chips laid on orthogonal planes, proved that the particle flux can be considered isotropic, with differences in error counts lower than 10 % between the vertical and horizontal axes.

Finally, during exposure, the platforms experienced aurora australis (southern light) phenomena, which occurs several times every year. Aurora australis is the light emitted when charged particles, mainly electrons and protons, enter the terrestrial atmosphere and collide with its atoms. During the experiments, several aurora australis occurred at Concordia, and in particular, one episode lasted for many hours between July 14 and 15, 2013. During these events, the SEU sensing platforms were operational. The fact that the recorded data did not show any difference in error rate w.r.t. the normal conditions reveals that the particle showers, or their products observed during these phenomena, do not reach the ground level with energies large enough to induce any upsets.

## 9. Conclusions

Throughout this paper, the problems of soft error occurrence in SRAM memories devices has been presented. Results from test data obtained during extensive irradiation campaigns (heavy ions, protons, and neutrons) based on state-of-the-art test methods have been rated. It has been demonstrated that SRAM sensitivity is directly linked to the method of testing and more specifically, the operational mode: static (retention) or dynamic (memory continuously accessed). To consider the effect of the inner architecture of the memory, the case study of dual-stacked layer SRAM has been introduced, as well as bitmapping and statistical data processing methodologies. Finally, once the SRAM device has been characterized, it is proved an efficient particle detector for radiation level monitoring in various environments like LHC (CERN) and terrestrial atmospheres.

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## Annex V

V. Gupta, **A. Bosser**, G. Tsiligiannis, M. Rousselet, A. Zadeh, A. Javanainen, A. Virtanen, H. Puchner, F. Saigné, F. Wrobel and L. Dilillo, "SEE on Different Layers of Stacked-SRAMs", in *IEEE Transactions on Nuclear Science*, vol. 62, no. 6, pp. 2673-2678, 2015.

*Contribution: the author had a major role in the experiment's software and hardware development, and took part in the test campaigns and writing.*

# SEE on Different Layers of Stacked-SRAMs

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**Abstract**—This paper presents heavy-ion and proton radiation test results of a 90 nm COTS SRAM with stacked structure. Radiation tests were made using high penetration heavy-ion cocktails at the HIF (Belgium) and at RADEF (Finland) as well as low energy protons at RADEF. The heavy-ion SEU cross-section showed an unusual profile with a peak at the lowest LET (heavy-ion with the highest penetration range). The discrepancy is due to the fact that the SRAM is constituted of two vertically stacked dice. The impact of proton testing on the response of both stacked dice is presented. The results are discussed and the SEU cross-sections of the upper and lower layers are compared. The impact of the stacked structure on the proton SEE rate is investigated.

**Index Terms**—90 nm, multiple cell upset (MCU), radiation testing, SEE rate, single event upset (SEU), SRAM, stacked dice, static and dynamic mode testing.

## I. INTRODUCTION

**I**N EMBEDDED electronic systems, the largest part of the die area is generally allocated to memories, which are a key devices that directly impact the performance of the system.

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Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

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Hence, in order to dispose of more memory storage space with the same footprint area, the technique of stacking dice has become an interesting option as shown for example in [1] for Static Random Access Memory (SRAM) memories. Different types of memories can be stacked together (e.g. SRAM and FLASH memories [2]), as well as different types of components (e.g. Dynamic Random Access Memory - DRAM and microcontroller) in 3D integrated circuits that target not only area gain but also reduction of interconnections, latency and energy consumption. These kinds of structure need more complex setup and preparation for their radiation hardness assurance testing. Also the analysis of the experimental data obtained in radiation testing requires particular attention.

This study is part of the work carried in the frame of the MTCube project. MTCube (Memory Test CubeSat) is a nano-satellite of type CubeSat, which will test the radiation sensitivity of several types of memories (SRAMs, Ferroelectric Random Access Memory or FRAM, Magnetic Random Access Memory or MRAM and FLASH). One of the SRAM memories selected for flying, has the particularity of being composed of two stacked dice, thus the impact of the stacked structure on the soft error rate is investigated. This type of study has wider impact than the only MTCube mission, since stacked architectures are present not only in the form of 3D devices, which represent an emerging technology for space applications, but more commonly in Systems in Packaging (SiP) chips. The latter are composed of different silicon devices bonded together in a single packaging and they are widely used, despite the fact that the final user is aware or not of their combined architecture.

Previous studies regarding 3D integrated circuits are present in literature. For example, in [3] the authors focus on the impact of the process allowing 3D integration with respect to Total Ionizing Dose (TID) (up to 10 Mrad) of a 130 nm transistor and a CMOS (Complementary Metal Oxide Semiconductor) sensor. In [4], the authors studied the total ionizing dose and Single Event Effect (SEE) impact of protons (4.8 to 500 MeV) and neutrons on vertically stacked SOI (Silicon On Insulator) SRAMs.

The present paper focuses on the study of the effects of heavy-ion and proton particle irradiation on a two-layer stacked bulk SRAM memory. To the best knowledge of the authors, no previous studies were performed on bulk vertically stacked SRAMs. In particular, the impact of layering on the soft error rate recorded on the different dice is discussed.

The rest of the paper is organized as follows. The second section describes the experimental test set-up and test conditions. The third section covers the analysis of the heavy-ion and proton test result. Finally, in Section IV, the impact of memory stacking on the proton SEE rate in orbit is evaluated.

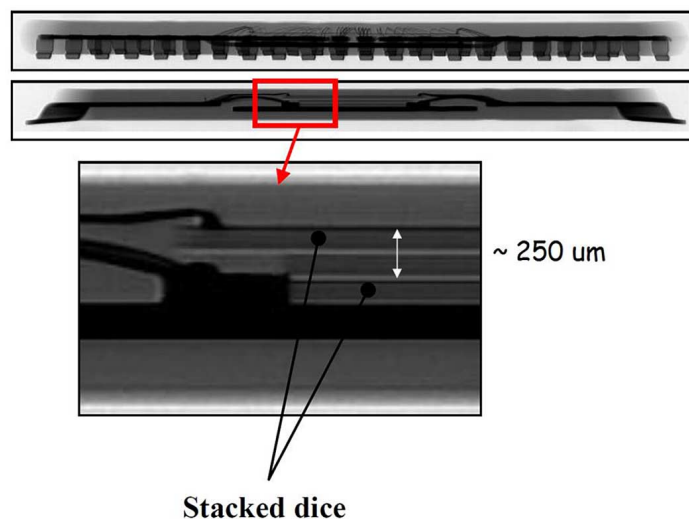


Fig. 1. X-ray performed on the SRAM CY62177EV30, where two stacked dice can be clearly distinguished separated by a spacer.

## II. EXPERIMENTAL SETUP

For the purpose of this study, an open-top asynchronous 32 Mbit SRAM with bulk technology was used (Cypress - CY62177EV30 MoBL). The nominal supply voltage to the memory is 3.3 V, the core voltage is 1.65 V in active mode and 0.8 V in standby mode. An x-ray photograph of the chip was performed and revealed the presence of two superposed dice with an epoxy spacer in between (Fig. 1). The distance between the sensitive parts (top surface) of the two dice was evaluated to about  $250 \mu\text{m}$  on the base of the photograph. Both dies have the same orientation, as confirmed by the memory manufacturer. The total BEOL (Back End Of Line) thickness is of  $1.41 \mu\text{m}$  constituted of three metal layers, two of aluminum and one of tin.

This device was irradiated at the Heavy-Ion Facility (HIF) in Louvain-La-Neuve, Belgium [5] and at the Radiation Effects Facility (RADEF) in Jyväskylä [6], [7], Finland.

Irradiations at HIF were carried out using the heavy-ion cocktail presented in Table I. The last two heavy-ion runs are part of another cocktail provided by HIF that was used solely on the upper die as the range of those ions does not allow penetration down to the lower die (see Section III-C). Irradiations at RADEF were performed with protons. In both cases the beam operator rated the beam homogeneity at better than  $\pm 10\%$  over the chip area. Several test runs were carried out during each test campaign, with ion species, energy and electrical stimuli varying from run to run. Particle fluence was adapted for each run depending on the memory sensitivity, from  $5 \times 10^2$  to  $1 \times 10^4 \text{ cm}^{-2}$  for heavy-ions, and from  $3 \times 10^6$  to  $1.5 \times 10^9 \text{ cm}^{-2}$  for protons in order to reach a sufficient number of induced errors per run to reduce the statistical uncertainty. Table I gives the main characteristics of the heavy-ion beam cocktails used for this study. RADEF provided low-energy proton beams at energies provided in Table II. One memory chip was used for tests at HIF and two chips at RADEF (one for proton tests below and up to 4.7 MeV, and one for higher proton energies).

Each device under test (DUT) was mounted on a printed circuit board (PCB) and connected to a controller implemented

TABLE I  
HEAVY-IONS AND THEIR ENERGIES AND RANGES IN SILICON

Ion	Energy (MeV)	LET (@ Top of BEOL) ( $\text{MeV}\cdot\text{cm}^2/\text{mg}$ )	Range @ Bragg Peak ( $\mu\text{m}$ )
C	131	1.1	292
Ne	235	3	216
Ar	372	10.2	117
Ni	567	20.4	100
Kr	756	32.6	92
N	60	3.3	59
Ne	78	6.4	45

TABLE II  
PROTONS ENERGIES AND THEIR RANGES IN SILICON

	Energy (MeV)	Range
Protons	0.6	$8.0 \mu\text{m}$
	0.98	$16.0 \mu\text{m}$
	2.2	$55.5 \mu\text{m}$
	4.7	$194.5 \mu\text{m}$
	9.5	$649.0 \mu\text{m}$
	14	$1.0 \text{ mm}$
	20	$2.0 \text{ mm}$
	30	$5.0 \text{ mm}$
	40	$8.0 \text{ mm}$
50	$12.0 \text{ mm}$	

through a Field-Programmable Gate Array (FPGA). For heavy-ion and low-energy proton tests (including 9.5 MeV and below 9.5 MeV), the DUT was located in a vacuum chamber directly exposed to the beam while the FPGA was placed outside the beam line to ensure reliable operation, although also located in the chamber. For proton energies above 9.5 MeV, tests were conducted in air. The data collection and experiment tuning were made through a computer that was placed outside the experimental chamber.

During each test run, in case a bit flip was detected the erroneous word along with other information such as the failing address and the timestamp was transmitted to the computer, for storage and data processing.

The memory devices were tested under two different test modes: the *static* and the *dynamic modes*. During the static mode a known data pattern is stored in the memory, which is then irradiated. Subsequently, a comparison is performed between the initial and post-irradiation data. During dynamic mode testing, specific sequences of write and read operations (algorithms) were repeatedly acted during the irradiation. Read operations, which are performed in the test algorithms, accomplish both the dynamic stimulation and the error check in the selected word.

During the static test, the data background scheme was a checkerboard pattern (10101010). For the dynamic test, several March algorithms (commonly used for memory functional tests [8]) were employed: March Dynamic Stress, March C- and Mats+. Furthermore, in order to stimulate the memory in

different manners, various addressing schemes have been applied during dynamic mode testing [9]: Fast Row, Fast Column, pseudorandom addressing, adjacent (Gray) addressing and inverse adjacent (inverse Gray) addressing.

### III. RESULTS AND DISCUSSION

Throughout all the test runs, the  $1\sigma$  standard deviation on the SEU cross-section did not exceed 15%, with most of the runs being below 11%, according to the log files provided by the facilities and the number of bit-flipped events that occurred for each run. Due to the relatively small statistical uncertainty, the error bars would be the same size or smaller than the experimental points in the graphs, thus they are not reported for sake of readability.

#### A. Two-Die Stack Memory Tested With Heavy-Ions

The graph in Fig. 2 shows the SEU cross-section of the memory during static tests. We first consider the SEU cross-section of the memory that takes into account all detected bit flips over the entire address span. The analysis of the full memory SEU cross-section shows an unexpected peak for the lowest values of Linear Energy Transfer (LET). This increase in SEU cross-section is due to the presence of a stacked structure within the chip as it will be shown hereafter. To further investigate this phenomenon, we analysed the SEU cross-section considering the errors occurring on the upper die (thanks to information provided by the manufacturer) but still referred to nominal memory size, as plotted in Fig. 2. Similarly, the SEU cross-section of the upper die is plotted in Fig. 2 (dotted line). It can be clearly observed that, while the “black-box” and the upper die SEU cross-section curves perfectly match for values of LET above  $3 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ , they show a clear discrepancy for the test performed at  $1.1 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ , which corresponds to the particle with the highest penetration. The difference between the two measured SEU cross-sections is about one order of magnitude. This is in fact due to errors occurring on the lower die. This discrepancy has been observed for three similar static test runs and for all dynamic tests performed in the same range of energies.

These results show that for low values of LET around  $1 \text{ MeV} \cdot \text{cm}^2/\text{mg}$  (corresponding to the highest particle range), the recorded errors mostly occur in one half of the memory, while for higher values of LET (lowest particle range) solely the other half of the memory is affected.

These observations are in concordance with the presence of a two-layer structure within the memory chip. Fig. 3 depicts some physical bitmaps of the memory, in which the occurring errors are represented as black dots in the memory cell array. These bitmaps allow visually observing how both dice are affected at the different values of LET. On these bitmaps, for most particles, the bit flips appear only on the upper part (referring to the upper die), while for carbon ion irradiations (having particle with the longest range), the lower part of the bitmap (lower die) displays most of the errors.

The graph in Fig. 4 gives the Bragg curves in silicon of the employed heavy-ions. With these curves and the above observations, we can estimate the depth of the sensitive volume of the lower die (its surface) from the surface of the upper layer

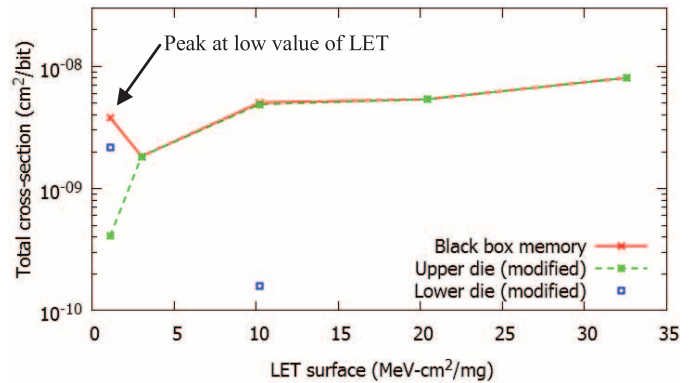


Fig. 2. Total heavy-ion SEU cross-section of the SRAM under static test calculated while considering: the entire memory (referred to as black box); the bit flips in the upper and lower die but matched to the whole memory.

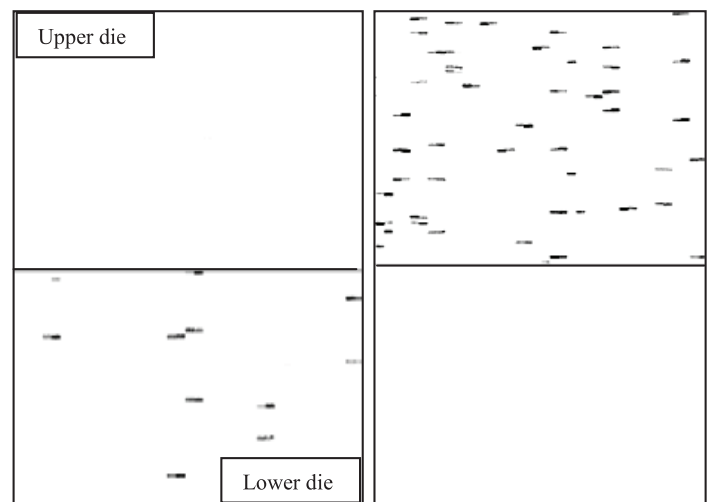


Fig. 3. Physical bitmap of the memory for carbon ion (left) and neon ion (right). On the left picture, the top die is solely affected by SEUs while there are SEUs and MCUs on the bottom die. On the right picture, the top die is affected by SEUs and MCUs while the bottom die is not affected by any SEUs nor MCUs. Note: The size of the picture does not allow to clearly see SEUs.

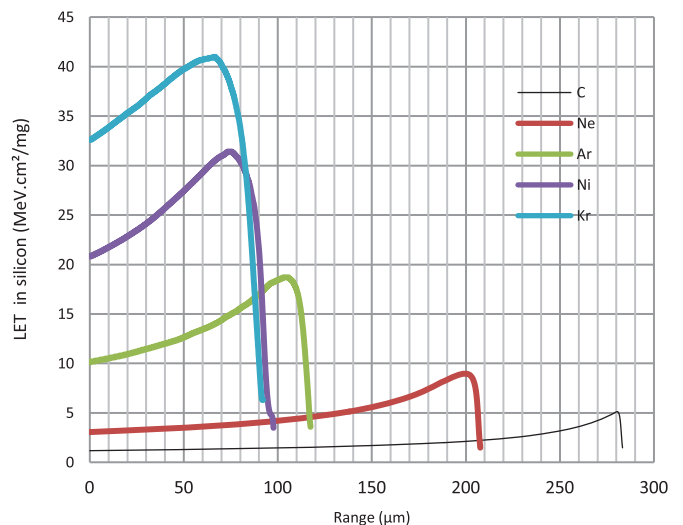


Fig. 4. High penetration ions Bragg curves in Silicon.

that includes the upper BEOL (Back End Of Line), which was exposed to the beam.



TABLE III  
ESTIMATED LET VALUES OF PARTICLES REACHING THE LOWER DIE

Run #	Flux (#/(cm <sup>2</sup> .s))	Fluence (#/cm <sup>2</sup> )	Estimated LET (MeV.cm <sup>2</sup> /mg)
1	5.0 x 10 <sup>1</sup>	1.1 x 10 <sup>3</sup>	5.1
2	5.0 x 10 <sup>1</sup>	6.0 x 10 <sup>3</sup>	1.9
3	5.0 x 10 <sup>1</sup>	4.5 x 10 <sup>3</sup>	3.1
4	1.6 x 10 <sup>2</sup>	6.2 x 10 <sup>3</sup>	3.3

Since the lower die is exhibiting errors for the carbon ions, but not for the high-penetration neon ions (as well as all the other ions), we can deduce that the sensitive volume of the lower die has to be located between the maximum penetration value of the neon ion and the maximum penetration value of the carbon ion. Thus, we can state that the surface of the lower die is located between 216 and 292  $\mu\text{m}$  from the surface of the upper die. This result is approximate since the range of the ions have been calculated by considering silicon as the only crossed material, and by neglecting any other material such as metallic connection pads and the epoxy material between the stacked layers (spacer). Since the Bragg curve of the high penetration ions have been plotted solely assuming a silicon material, the distance unit will be given in micrometer “equivalent silicon” hereafter referred to as  $\mu\text{m}(\text{Si})$  similarly to TID units in rad (Si).

In order to estimate the depth of the second layer with higher precision on the basis of the irradiation results, we performed a Weibull fit of the SEU cross-section of the static test considering, at first, only the upper die. Several identical runs were performed (same ion LET, and algorithmic stimuli), from which we then considered the averaged SEU cross-section for each value of LET. The SEU cross-section points were then fitted by a Weibull curve, which was then used together with the number of errors detected in the lower die, to estimate the LET on the lower die, assuming the sensitivity of the lower die to be identical to the upper one. This simplified approach implied neglecting the possible interaction between the ion and the upper layers (upper die and epoxy spacer) before reaching the lower die. In this simplified calculation, it was again assumed that the entire structure was made of silicon.

Concerning the count of errors, the analysis of the bitmaps revealed that errors on the lower die are also affected by large-scale events similarly to the upper die. These events are characterized by a large number of bit flips that are generally caused by Single Event Functional Interrupts (SEFIs) and micro-latchups [9]. It is thus opportune to proceed with the count of individual particle induced events by performing clustering techniques, i.e. considering all the bit flipped occurring temporally and spatially close to each other as a single event generated by the same particle. The used in-house clustering technique [10] (not detailed in this present paper) allows obtaining a precise SEU cross-section based on the actual number of SEUs rather than on raw count of the number of flipped bits, which can considerably vary the estimation of SEE. For the four static runs performed with the carbon ion, the estimated LET values of the particles reaching the lower die are presented in Table III. The standard deviation of this clustered SEU cross-section is below 12.5%.

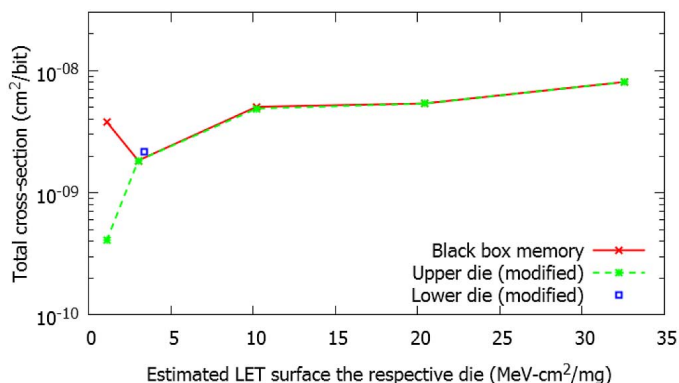


Fig. 5. Total heavy-ion SEU cross-section of the SRAM under static test as shown in Fig. 2 but for the estimated LET at the surface of the respective die. It can be noted that the lower die SEU cross-section point now fits the upper die SEU cross-section curve.

A first rough analysis of this data shows that the average estimated value of LET, at the depth where the sensitive area of the lower die is located, reaches a value of approximately 3  $\text{MeV} \cdot \text{cm}^2/\text{mg}$ . Considering the Bragg curve for the carbon ion, this value of LET is reached at a depth of about 250  $\mu\text{m}(\text{Si})$ . This value is in good agreement with the measured distance, on the basis of the X-ray photograph, between the two layers which was found to be 250  $\mu\text{m}(\text{Si})$ .

Besides, by plotting the upper and lower die SEU cross-section (Fig. 5) with respect to the LET at the surface of the respective die, the SEU cross-section of the lower die fits the SEU cross-section curve of the upper die confirming similar sensitivity of the dice. Although the approximation due to the taken assumption, this calculation method provides another mean to check the distance between two stacked dice.

### B. Two-Die Stack Memory Tested With Protons

Proton testing was performed at the RADEF facility in Jyväskylä [7] for a memory device belonging to the same production lot and by using a similar setup, with proton energies ranging from 0.6 MeV up to 50 MeV. The range of penetration of proton in Silicon ranges between 7.75  $\mu\text{m}$  (@0.6 MeV) and 12 mm (@50 MeV). The background data for the static tests was *solid '1'* (all bits set to 1).

Fig. 6 illustrates the SEU cross-sections of the upper and lower dice during proton testing. Fig. 6 also shows the overall SEU cross-section, considering the memory as a “black box” (blue curve in the graph). Two peaks are visible at 0.6 MeV (higher peak) and 9.5 MeV (lower peak). The first observation to be done is that for proton energies below 4.7 MeV, no events occurred on the lower layer except for one SEU on the lower layer at 4.7 MeV. For energies above 9.5 MeV, events occurred on both layers. The explanation may come from the direct ionization process occurring on both dice at different proton energies. The location (energy < 1 MeV) of the SEU cross-section peak and the general shape of the SEU cross-sections at very low proton energies seems in agreement with results presented in [11] where a commercial 90 nm SRAM was tested under low energy protons. Below 2.2 MeV the upper layer SEU cross-section reaches a peak due to direct ionization processes occurring on that layer. Around 10 MeV the lower die SEU cross-section

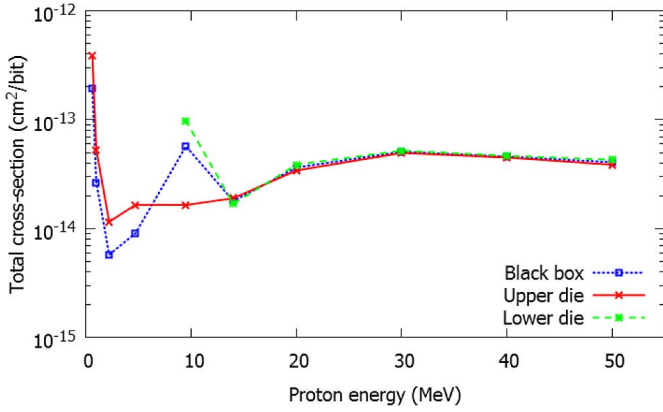


Fig. 6. Total proton SEU cross-section of the stacked SRAM under static test calculated while considering: the entire memory (so-called “black box” SEU cross-section); upper die only, lower die only.

reaches a peak since direct ionization processes are dominant on the lower die as for this energy the proton Bragg peak is close to the lower die. The proton beam energy at which the second peak SEU cross-section occurs depends on the materials that are crossed by the proton particles before reaching the lower layer, since they affect the depth at which the Bragg peak is achieved.

C. Clustered Events

In order to complete the study on the lower die, we compare the total and event SEU cross-section under static tests of the lower layer for Carbon ions (which was estimated to reach a LET at the surface of the lower layer around  $3.3 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ ) and the SEU cross-section during static tests of the upper layer for Nitrogen and Neon ions (reaching a LET at the surface of the upper layer respectively at  $3.3$  and  $3 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ ). Those particles belong to a cocktail provided by the HIF facility (see last two ion runs in Table I).

For this purpose, two specific test runs were performed and the results are summarized in the graph of Fig. 7. The event SEU cross-section shown in the graph is obtained by applying the clustering technique mentioned above (all bit flips belonging to the same particle interaction counts as one event). This was possible thanks to the knowledge of the event timestamp and scrambling scheme provided by the manufacturer of the memory, allowing creating the actual physical bitmap of the memory cell array. The good matching of results in terms of SEU cross-section (raw count and clustered) between the upper and lower dice proves that our previous measures and calculations (used to estimate the LET of  $3.3 \text{ MeV} \cdot \text{cm}^2/\text{mg}$  on the sensible area of the lower die) are correct. Fig. 8 shows the total (raw) and event proton SEU cross-sections of both dice of the memory for static mode testing. Both SEU cross-section peaks (at  $0.6 \text{ MeV}$  for the top die and at  $9.5 \text{ MeV}$  for the lower die) the total and event SEU cross-section are similar, highlighting the fact that there are mainly single bit flips occurring on both dies.

Furthermore, for energies above  $14 \text{ MeV}$ , both dies event and total SEU cross-sections have similar values, showing that the sensitivity of both dies is similar at energies above  $14 \text{ MeV}$ .

Finally, from  $20 \text{ MeV}$  up to  $50 \text{ MeV}$ , the event SEU cross-section of both dies shows an almost constant  $20$  to  $30\%$  decrease

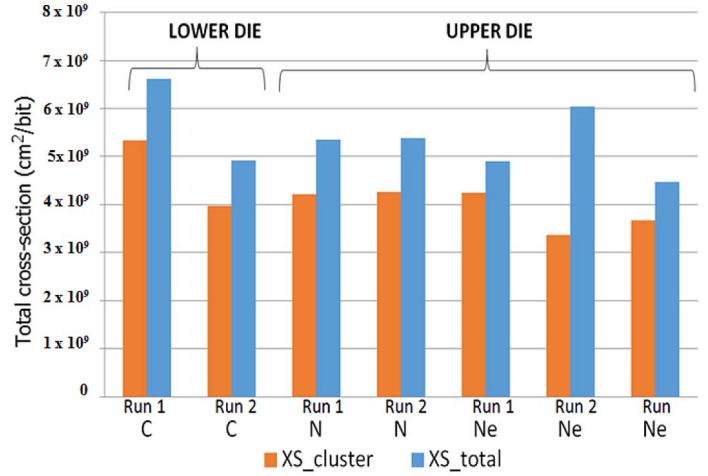


Fig. 7. Total and event SEU cross-sections (XS) for various runs: the run with carbon (C) are calculated for the lower layer (surface LET  $\sim 3.3 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ , the run with nitrogen (N) or neon (Ne) are calculated for the upper die with surface LET respectively of  $3.3$  and  $3 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ .

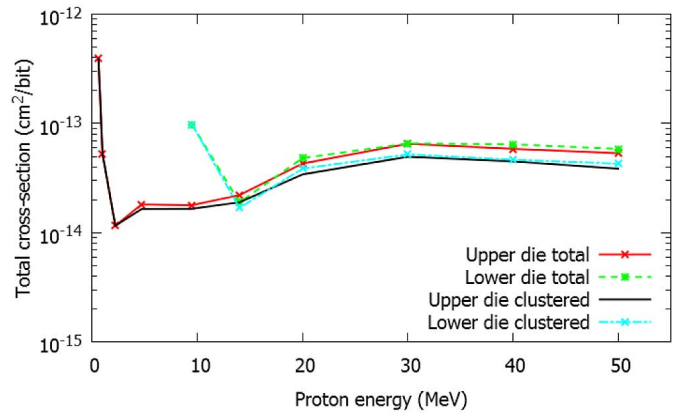


Fig. 8. Total and event proton SEU cross-sections of the SRAM under static test for both upper and lower dies.

compared to the total SEU cross-section. This highlights the fact that no big cluster events were recorded during static testing at those energies.

D. Angle Considerations Under Heavy-Ion Irradiations

Just considering the total flipped bits SEU cross-section of static test of the upper layer, we made a comparison between the results obtained with high values of LET and those with high penetration cocktail. The results are presented in the form of SEU cross-section plots in Fig. 9. It can be seen that the SEU cross-sections obtained with both ion cocktails appear coherent. Nevertheless, at least two SEU cross-section points are lower than expected. In fact, three SEU cross-section points were obtained while having the memory placed at  $45^\circ$  for N, Ne and Ar ions providing values of effective LET of  $4.7$ ,  $9.0$ ,  $22.5 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ , respectively.

The SEU cross-section for a LET of  $4.7 \text{ MeV} \cdot \text{cm}^2/\text{mg}$  and  $9.0 \text{ MeV} \cdot \text{cm}^2/\text{mg}$  does not follow the trend and present values lower than expected at these values of LET. A possible explanation is that the sensitive volume of each memory cell seems to be smaller in width compared to its vertical length.

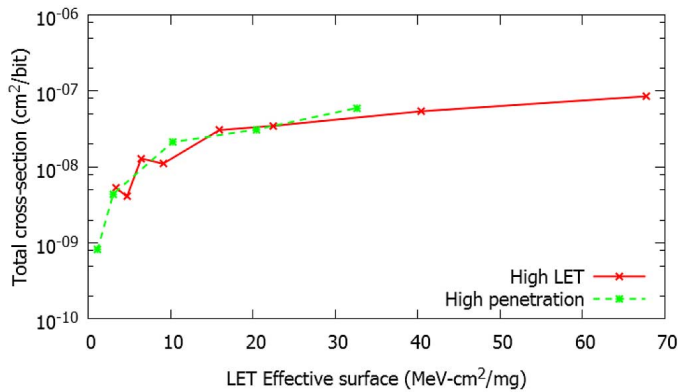


Fig. 9. Total flipped bits heavy-ion SEU static cross-section of the upper layer for the high LET and high penetration cocktail. Data was obtained for  $0^\circ$  and in some cases  $45^\circ$ .

TABLE IV  
PROTON SEU RATE IN 630 KM HIGH INCLINATION ORBIT FOR A STACKED LAYER AND SINGLE LAYER MEMORY

Memory configuration	Proton SEE rate $((s \cdot \text{bit})^{-1})$
Stacked layer	$5.36 \cdot 10^{-12}$
Single layer	$5.12 \cdot 10^{-12}$

#### IV. IMPACT OF STACKED DICE ON THE SEE RATE IN ORBIT

Based on the static SEU cross-section obtained during proton testing, the impact of stacked-dice structure is investigated on the SEE event rate. For this calculation, we consider a Low Earth Orbit (LEO) at an altitude of 630 km and an inclination of  $98^\circ$  as case study. The proton radiation environment model used was AP8 min [12] for trapped protons and ESP [13] for solar generated protons. Protons originating from Galactic Cosmic Rays were not considered. Simulations of the radiation environment were made using the OMERE software [14]. The environment was transported through a radiation shielding of 3.7 mm of aluminium simulating the equivalent material to be crossed by external particles to reach the upper memory die (i.e. external satellite shielding and plastic material of the component's packaging). In this part of the study, we compare the results of the current dual-dice SRAM with an equivalent SRAM having the same die sensitivity (i.e SEU cross-section) and storage capacity of the studied SRAM but with single-layer structure. Results are presented in Table IV.

The analysis of the results shows that the stacked memory undergoes an SEE rate increase of approximately 4.5% compared to an equivalent single layer memory.

#### V. CONCLUSION

This work presents heavy-ion and proton test results for dual-layer stacked commercial SRAM. High penetrating heavy-ion cocktails and protons enabled to clearly show the effect of a stacked-dice configuration on the radiation response of this memory. With low-energy protons, sensitivity of a component must be carefully considered in order to assess the

effects of direct ionization as this process may occur at different values of energy, corresponding to the proton Bragg peak reaching each layer. The study was completed by an analysis resulting from the clustering of the flipped bits and showed a very similar type of response on both dies as expected. Based on the experimentally calculated SEU cross-section, it was then possible to estimate the SEE rate in LEO. Considering solely protons, a negligible increase in the proton induced SEE rate is revealed for two stacked dice w.r.t. a single layer device ( $\sim 5\%$ ).

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## Annex VI

V. Gupta, **A. Bosser**, G. Tsiligiannis, A. Zadeh, A. Javanainen, A. Virtanen, H. Puchner, F. Saigné, F. Wrobel and L. Dilillo, "Heavy-Ion Radiation Impact on a 4 Mb FRAM Under Different Test Modes and Conditions," in *IEEE Transactions on Nuclear Science*, vol. 63, no. 4, pp. 2010-2015, Aug. 2016.

*Contribution: the author had a major role in the experiment's software and hardware development, and took part in the test campaigns.*

# Heavy-Ion Radiation Impact on a 4 Mb FRAM Under Different Test Modes and Conditions

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**Abstract**—The impact of heavy-ions on commercial Ferroelectric Memories (FRAMs) is analyzed. The influence of dynamic and static test modes as well as several stimuli on the error rate of this memory is investigated. Static test results show that the memory is prone to temporary effects occurring in the peripheral circuitry, with a possible effect due to fluence. Dynamic tests results show a high sensitivity of this memory to switching activity of this peripheral circuitry.

**Index Terms**—130 nm, FRAM, multiple cell upset (MCU), radiation testing, single event upset (SEU), static and dynamic mode testing.

## I. INTRODUCTION

HIGH density ferroelectric memory (FRAM) is based on metal-organic chemical vapor deposition (MOCVD) process of lead zirconium/titanate (PZT) thin films. This device represents a promising candidate for applications requiring low power consumption, fast write access, high cycling endurance, non-volatile data storage [1] and good

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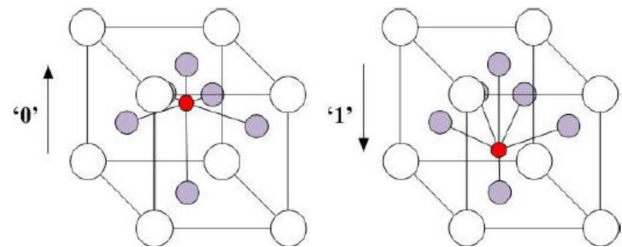


Fig. 1. PZT crystal with an oxygen atom in the center. The two stable states of the crystal correspond to the two possible polarization configurations, which in turn correspond to the two possible states of a bit ('0' or '1').

resilience to radiation. An FRAM memory cell relies on the electrical polarization of the PZT film. The PZT material can be switched between two stable states across the center of the oxygen octahedron with the application of an electric field, as depicted in Fig. 1. Depending on whether the polarization is opposite or aligned with an applied electric field, different levels of displacement current are induced during a cell read operation. A current-sensing circuit determines whether the ferroelectric capacitor is in a '0' or '1' state prior to the read operation. The cell loses its configuration during a read operation, and as a result the memory circuitry has to restore the cell to its original value after each read action. Read and write endurance greater than  $10^{12}$  cycles [2] and automotive-grade data retention reliability has been demonstrated with FRAM memory cells.

Since this non-volatile storage element is based on polarization and responds only to applied electrical fields, the FRAM memory cell is much less sensitive to soft errors from injected energetic particles compared to SRAM memory cells (charged based) [2], [3]. Considering that particle-induced parasitic currents cannot alter the polarization of the storage element, the susceptibility of the device to radiation effects is mostly due to failures in the control logic circuitry and peripheral circuit components such as the address decoders, I/O buffers, power switch, or sense amplifiers. Besides, 2 Transistors-2 Capacitors (2T-2C) architecture, as presented in Fig. 2, allows reducing even further the sensitivity of FRAM memory cells.

Previous works that studied the behaviour of FRAM under total ionizing dose [3] showed that failure did not occur because of the ferroelectric thin film, but rather due to the control circuitry using non rad-hard CMOS processes. In [5], other studies have pointed out a weakness in the sensing and

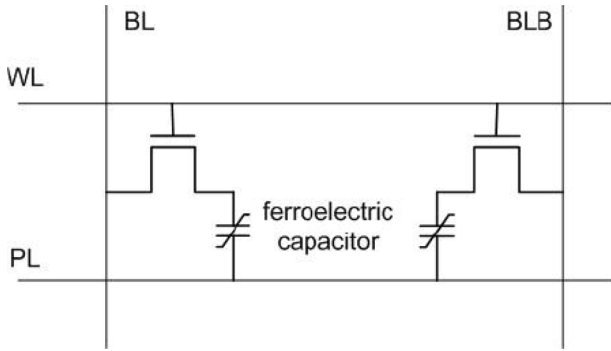


Fig. 2. two Transistors/two Capacitors (2T-2C) FRAM cell architecture [8]. WL represents the Word Line, BL the Bit Line, BLB the opposite of BL and PL the Place Line. The presence of a PZT capacitor in opposite state in the same memory cell allows increasing the reliability of the memory cell at the cost of reducing the memory cell density [9].

reference circuitry for previous generation devices with respect to the ones considered in this study. In other works, heavy-ion or proton tests have been reported such as in [6] or [3] providing similar types of results pointing as well towards peripheral logic or access state machine within the chip but also towards the hidden write operation that is performed after a read operation. For this reason these FRAM devices were not qualified for space applications. However, some more recent memories showed to withstand 50 or even 100 krad(SiO<sub>2</sub>) when the memory is unbiased as its sensitivity is reduced when compared with a biased device [5]. Therefore, Single Event Latchup (SEL) and Single Event Upset (SEU) rates are the dominant barriers to expand the use of commercial terrestrial FRAM products to the space environment.

In this study based on the results presented in [7], the vulnerability of a COTS FRAM device under heavy-ion radiation is further investigated. The purpose is to explore their applicability within the MTCube project, in which a CubeSat (cubic nano-satellite) will embed several types of memories made with emerging technologies. The effect of heavy-ions in correlation with the test modes, static (data retention) and dynamic (with continuous read/write accesses), as well as several different stimuli, are investigated.

The rest of the paper is organized as follows: Section II describes the experimental test set-up and test conditions while Section III presents the results as well as an analysis focused on the sensitivity of the tested FRAM in dynamic mode; Section IV concludes the paper.

## II. EXPERIMENTAL SETUP

The Device Under Test (DUT) is a 4Mbit asynchronous FRAM manufactured by Cypress Semiconductor (\FM 22L16) used in 16-bit word mode. The cell structure is 2T-2C and the control circuitry is built using a 130 nm CMOS process. Fig. 2 briefly shows the architecture of a 2T-2C FRAM cell.

All memories were delidded prior irradiation tests. Five Test Campaigns (TC1 to TC5) were conducted at 2 different heavy-ion radiation test facility: the RADEF facility [8] in Jyväskylä hosted TC1, TC2 and TC3; the GANIL facility [10] in Caen was used for TC4. During each TC, a different FRAM was used, except during TC3 where two different components

TABLE I  
HEAVY-ION COCKTAILS USED AT THE DIFFERENT FACILITIES. TC STANDS FOR TEST CAMPAIGN. INCLINATION ANGLE IS DEFINED AS THE ANGLE BETWEEN THE AXIS NORMAL TO THE DIE PLAN AND THE BEAM

	Ion	Incl.	Energy (MeV)	Effective LET (@ Top of BEOL) (MeV/(mg/cm <sup>2</sup> ))	Range @ Bragg Peak (μm)
TC1 (RADEF)	N	0°	139	1.8	202
	Fe	0°	523	18.5	97
	Kr	0°	768	32.1	94
	Kr	45°	768	45.4	-
TC2 (RADEF)	Ne	0°	186	3.6	146
	Ne	30°	-	4.2	-
	Ne	45°	-	5.1	-
	Ar	0°	372	10.1	118
	Ar	30°	-	11.7	-
	Ar	50°	-	15.7	-
TC3 (RADEF)	N	0°	139	1.8	202
	Fe	0°	523	18.5	97
	Kr	0°	768	32.1	94
	Xe	0°	1217	60.0	89
TC4 (GANIL)	Xe	0°	466	64.3	37
	Xe	0°	1790	50.2	137
TC5 (RADEF)	Xe	0°	1217	60.0	89
	Kr	0°	768	32.1	94
	Kr	45°	768	45.4	-

were used. Heavy-ion cocktails applied for each test campaign are detailed in Table I. During TC1, mainly static tests were performed together with two types of dynamic tests on a single DUT. The heavy-ion induced dose level reached on the DUT was estimated, based on the recommended dose estimation formula from the ESCC 25100 standard, to approximately 7 krad(SiO<sub>2</sub>) with an additional run during the same test campaign adding an extra 5 krad(SiO<sub>2</sub>). Static and dynamic tests were carried out during TC2 on another single DUT using several angles with two different types of particles. The estimated dose level was below 7 krad(SiO<sub>2</sub>). For TC3, two DUTs were tested under static and dynamic stress conditions reaching respectively 9 krad(SiO<sub>2</sub>) and 33 krad(SiO<sub>2</sub>). Static and dynamic tests were conducted on one DUT in TC4, with estimated dose level of 1.4 krad(SiO<sub>2</sub>). Finally, one DUT was used to perform unbiased tests during a small test campaign (TC5).

At both facilities the beam homogeneity is determined to be ±10% or better over the chip area. Several test runs were carried out during each test campaign, with ion species, energy and electrical stimuli varying from run to run. Particle fluence varied from  $5 \times 10^3$  to  $1.22 \times 10^7$  cm<sup>-2</sup>.

The DUTs were mounted on PCB cards and connected to controllers implemented through FPGAs. Except for TC4 where the DUT was tested in air, for all test campaigns, the DUT was located in a vacuum chamber, directly exposed to the beam while the FPGA, although located in the chamber, was placed

**March C-:**  
 $\{\uparrow (w0); \uparrow (r0, w1); \uparrow (r1, w0); \downarrow (r0, w1); \downarrow (r1, w0); \uparrow (r0)\}$

**Dynamic Stress:**  
 $\{\uparrow (r1, w0, r0, r0, r0, r0, r0);$   
 $\uparrow (r0, w1, r1, r1, r1, r1, r1);$   
 $\uparrow (r1, w0, r0, r0, r0, r0, r0);$   
 $\downarrow (r0, w1, r1, r1, r1, r1, r1);$   
 $\downarrow (r1, w0, r0, r0, r0, r0, r0);$   
 $\uparrow (r0, w1, r1, r1, r1, r1, r1)\}$

**Mats+:**  
 $\{\uparrow (w0);$   
 $\uparrow (r0, w1);$   
 $\downarrow (r1, w0)\}$

Fig. 3. March C- (above), Dynamic Stress (middle), and Mats+ (bottom) algorithms.

outside the beam line to ensure reliable operation. During each test run, in case a bit flip was detected the erroneous word along with other information such as the address and the timestamp was transmitted to a computer, for storage and data processing.

As mentioned above, the memory devices were tested under two different test modes: the *static* and the *dynamic mode*. During the static mode a known data pattern is stored in the memory, which is then irradiated. Subsequently, a comparison is performed between the pre-irradiation and post-irradiation data to detect the bit flips. During dynamic mode testing, specific sequences of write and read operations are repeatedly performed during irradiation exposure. Read operations are fundamental in dynamic mode, since they stimulate the control circuitry, while also providing the stored value of the memory cells.

For the dynamic tests, we employed March algorithms that have previously been used on SRAM devices: March C-, Mats+ and March Dynamic Stress [10], [11]. These algorithms are composed of several elements, and each element is composed of several read/write operations such as those presented in Fig. 3. Each element is applied to each memory address (word) of the memory, by advancing in the address space either in an ascending or descending order. The operations of each element are enclosed in parenthesis, while the marching direction is indicated by the arrows as can be seen in the example for the March C-, Dynamic Stress and Mats+ test algorithm [11].

Furthermore, in order to stimulate the memory in different ways, various addressing schemes have been applied during dynamic mode testing: normal logical addressing, pseudo-random addressing, adjacent (Gray) addressing and inverse adjacent (inverse Gray) addressing. More details on these test schemes are given in [13]. As the scrambling of the memory was unknown no other addressing scheme could be used.

### III. RESULTS AND DISCUSSION

#### A. Unbiased Mode Test

During TC5, a FRAM specimen was tested in unbiased mode after storing a checkerboard pattern in the core memory cells. Due to time constraints, it was only possible to test the

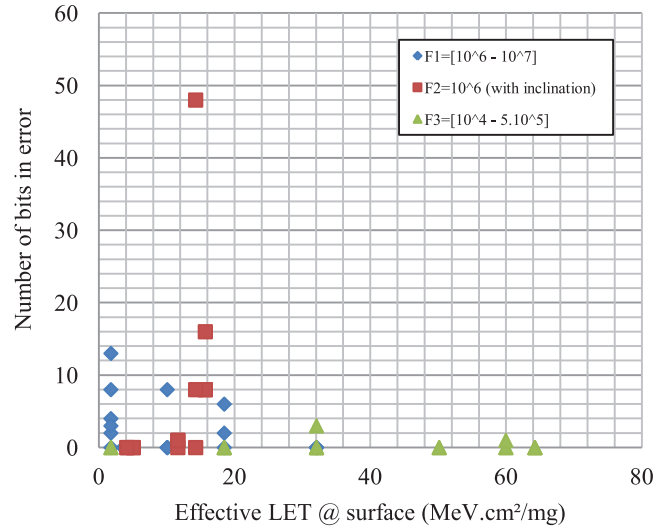


Fig. 4. Number of bit flips during heavy-ion tests (TC1, TC2, TC3 and TC4) in *static mode*. Static tests were performed at different inclinations. Errors are grouped with respect to the fluence.

memory against the two highest ions available in the RADEF cocktail. Hence the memory was tested against Xe and Kr ions at normal incidence and 45° incidence with an effective surface LET spanning from 32.1 to 84.8 MeV.cm<sup>2</sup>/mg. Various fluences were achieved from 1.1 × 10<sup>5</sup> cm<sup>-2</sup> to 1.0 × 10<sup>7</sup> cm<sup>-2</sup>. These tests resulted in no error found when reading back the memory after irradiation. A few biased tests were performed in order to ensure the good functionality of the set-up after irradiation.

#### B. Static Mode Test (Biased)

In this section, the results of *static mode* tests performed during all test campaigns with LET ranging from 1.8 up to 69.3 MeV.cm<sup>2</sup>/mg are presented. The memory was biased. During static tests, the applied patterns were solid '0' (00000000), solid '1' (11111111) and the common checkerboard pattern (10101010). The obtained results are presented in Fig. 4. The radiation sensitivity of the FRAM did not show any dependency on the data background pattern. On the other hand, the FRAM sensitivity showed an apparent relation to the fluence during each run. In order to highlight this aspect, the number of bit flips in static mode from all test campaigns are classified in three groups in Fig. 4: the group F1 gathers tests that were conducted with fluence ranging from 10<sup>6</sup> to 10<sup>7</sup> particles/cm<sup>2</sup>; the group F2 collects tests conducted with fluence of 10<sup>6</sup> particles/cm<sup>2</sup> but for inclination angles up to 50°; the group F3 gathers tests conducted with fluence ranging from 10<sup>4</sup> to 5 × 10<sup>5</sup> particles/cm<sup>2</sup>. Out of the 17 runs performed in the low-fluence group F3, 15 did not present any errors. The other two runs showed 3 errors and 1 error at respective LETs of 32 and 60 MeV.cm<sup>2</sup>/mg. It shall be remarked that none of the static runs resulted in a high number of bit flips for the F1 or F2 group: in some cases errors occurred, while in the next run, under similar conditions, no errors were recorded. The previous remark may imply that the FRAM is subjected to temporary effects,

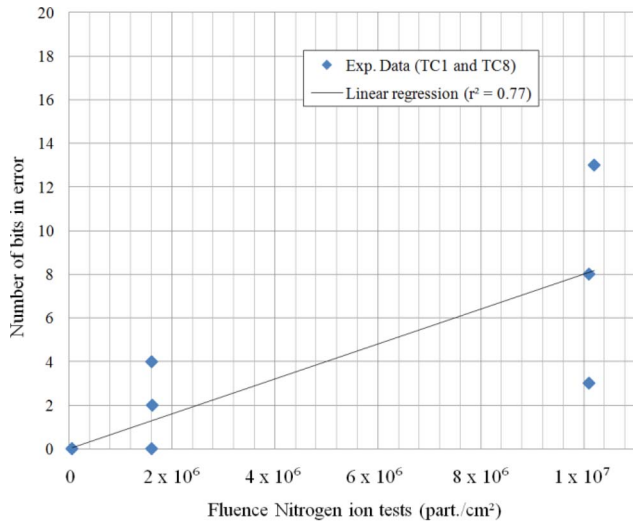


Fig. 5. Number of bit flips against fluence for the N ion (surface LET = 1.8 MeV.cm<sup>2</sup>/mg). The data was fitted using, as a first approximation, a linear regression method with a constant value equal to 0. The r-squared value is  $r^2 = 0.77$  for this fit.

able to anneal in between 2 runs (as no error were found in between 2 runs). Indeed, before starting a new run, a power cycle was performed on the memory which was sufficient to erase the recorded errors. In [4], the authors tested an FRAM memory (\FM 20L08) and noticed that, during static tests, no errors were recorded if a power cycle was performed prior to reading the memory whereas without a power cycle bitflips could appear. Those results appear to lead to the same conclusion of temporary effects. Besides, a deeper analysis of the test data by using the log files shows that the large numbers of bit flips obtained in certain runs are due not to isolated SEUs, but rather to Multiple Bit Upsets (MBUs) within the same word. This is especially true for the F2 group which relates to the runs made at high inclination. For example 48 bit flips that occurred during a run in TC2 are actually due to 7 faulty words (thus not all the 16 bit of the words were faulty). The lowest fluence at which an MBU was recorded was during TC3 at normal incidence with the Kr ion resulting in 1 word having 2 bits flipped. MBUs did not appear during unbiased mode tests even under Kr ion. Thus, we conclude that MBUs are likely to be the consequence of errors occurring in the peripheral circuitry, such as the sense amplifiers and I/O buffers that are mapped as errors in the memory cell array.”

In Fig. 5, in order to emphasis the apparent effect of fluence on the number of errors, the number of bit flipped was plotted against the fluence for the ion for which we tested at the largest fluence values. Two DUT test data was used to plot the figure below (one tested during TC1 for the fluence value of  $1.6 \times 10^5$  particles/cm<sup>2</sup> and one tested during TC3 for the 2 other fluence values). It shall be bear in mind that, initially, tests conducted on the FRAM were not focused on the effect of fluence but on the type of dynamic mode test effects and hence the non negligible impact of the fluence was found only during the post-treatment of several test campaigns. Hence due to the low number of data it is difficult to say on Fig. 5 whether a linear fit is better than a power law fit (for example).

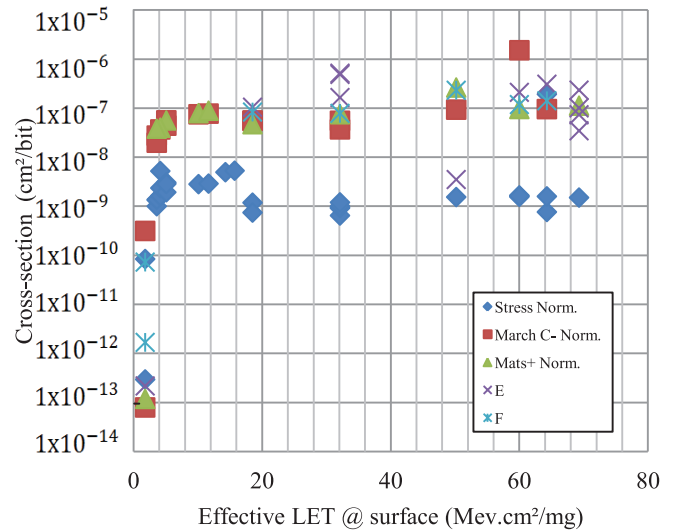


Fig. 6. Heavy-ion SEU cross-section per bit during *dynamic mode* testing. Different markers are used for different testing algorithms. Norm. means that the addressing scheme is a logical increasing addressing scheme. The  $1\sigma$  standard deviation (due to the number of counted errors and facility dosimetry) on the SEU cross-section did not exceed 15% except for the Nitrogen particle.

Nevertheless, a linear fit was calculated using the linear regression method and assuming a constant value of 0, as the number of errors for a fluence of 0 is supposed to be 0. The r-squared value for this fit was  $r^2 = 0.77$ .

In summary, Fig. 4 demonstrates that this particular FRAM has a good heavy-ion SEU resilience in static mode at low levels of fluence such as those expected for the MTCube mission being in LEO polar orbit. Conversely, at higher fluence values (even at low LETs, see Fig. 5), errors (and particularly SEUs) were detected that disappeared after a power cycle. Non-normal inclination values (30°, 45° and 50°) induced an increase in the number of flipped bits. Those results suggest that errors caused by temporary effects may occur on the CMOS part of the memory, which is not affected at lower fluence levels, as the ferroelectric part of the memory is immune to SEUs as suggested by the results from unbiased mode tests. Further tests shall be carried aiming at improving the characterization of the effect of fluence for different LET values as well as understanding the impact of inclination on the type and number of errors.

### C. Dynamic Mode Test

Dynamic mode tests were conducted during the four test campaigns and the related results are presented in Fig. 6. Since the scrambling scheme of the device is not known, the March algorithms could only be performed on logical (not physical) schemes. No Single Event Latchup (SEL) events were detected during the test campaign performed at room temperature (20°C), up to a LET of 69.3 MeV.cm<sup>2</sup>/mg. On the other hand, for all applied March algorithms, the number of collected errors has been sensibly larger compared to static mode. The high failure rate can be associated to Single Event Transients occurring in the control logic during read/write access operations.



Fig. 6 illustrates that, for each test algorithm, the radiation sensitivity of the memory follows a typical SEU cross-section curve with a LET threshold below  $1.8 \text{ MeV}\cdot\text{cm}^2/\text{mg}$  (lowest LET at which the memory was tested). The calculated SEU cross-section takes into account the total number of bits flipped. This might explain, for example, why at  $60 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ , the March C– dynamic SEU cross-section is higher than expected due to possible larger clusters of events (as the scrambling of the memory is currently unknown, it was not possible to clusterize the events). The saturation for all curves occurs very rapidly with increasing LET values. It is interesting to notice that there is a clear difference between the Dynamic Stress algorithm saturation SEU cross-section and all the other algorithms utilized during the test campaigns. This difference is of almost two orders of magnitude. Consequently, it is observed that the Dynamic Stress test has an opposite behavior than what has been observed for SRAMs [12]: among the various March algorithms applied on a 90 nm SRAM, the Dynamic Stress was the one that returned the highest SEU cross-section. The opposite behavior of the two types of memories may be explained by their structural differences. The March Stress has been created specifically to generate a ‘hammering’ effect on SRAM cells through multiple sequential read accesses to each memory location. In [14] and [15], the hammering effect has been proven to reduce significantly and progressively the Read Noise Margin (RNM) of the CMOS-based cells of SRAMs, which makes it more prone to be upset if disturbed by radiation-induced transients. In the case of the tested FRAM device, the storage elements are ferroelectric cells that do not exhibit to any RNM reduction, since a restoring write is applied after each read access, as explained above. Besides, as the cell structure of this memory is 2T-2C it is more immune to parasitic noise [16]. Moreover, in FRAMs, the most sensitive part is the CMOS control logic (address decoders, address/data registers, etc.) which is less affected by the March Stress test, that presents the lowest switching activity w.r.t. the other algorithms, since the change of address is made every 7 cycles (number of operations per element, see Fig. 3), and data up to 6 cycles (5 consecutive read operations in one element + the first one of the next element).

Similarly to reference [3], it was also noted that most of the first errors occurring during dynamic mode testing occurred on consecutive addresses. Moreover, several bit errors were MBUs, highlighting the sensitivity of the memory to the switching activity. Those few consecutive errors were then followed by large clusters of block errors. Additionally, other types of dynamic tests (namely E and F in Fig. 5) were used with high switching activity and resulted in SEU cross-section values similar to March C– of Mats+ dynamic tests. The worst case SEU cross-section value in static mode ( $10^{-11} \text{ cm}^2/\text{bit}$ ) is up to four orders of magnitude lower than the dynamic test SEU cross-section. All the previous remarks favor the increase of sensitivity of the CMOS part of the peripheral circuitry, which is only solicited in dynamic mode testing.

In Fig. 7, the effect of different types of addressing scheme during dynamic test is presented (Normal addressing, LSF, R

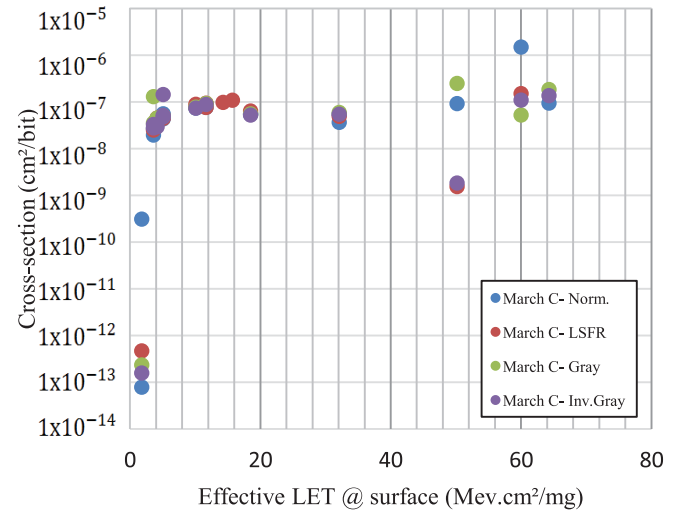


Fig. 7. Heavy-ions SEU cross-section during *dynamic mode* testing on TC1, TC2, TC3 and TC4 focusing on the different addressing scheme of one type of dynamic mode test performed (here March C–). The  $1\sigma$  standard deviation (due to the number of counted errors and facility dosimetry) on the SEU cross-section did not exceed 15% except for the Nitrogen particle.

gray and anti-gray as described in [13]) for the March C– test. It appears that the order at which the memory cells are accessed does not impact the sensitivity of the memory, which was the case, on the contrary, for SRAMs memories [13]. Similarly, no impact of the addressing scheme was observed on the Dynamic Stress and Mats+ tests.

#### IV. CONCLUSION

Heavy-ion testing confirmed that the static SEU cross-section in FRAM devices is very low due to the intrinsic radiation hardness of the storage cell based on ferroelectric layer. Unbiased tests between an effective surface LET of  $32.1$  and  $84.8 \text{ MeV}\cdot\text{cm}^2/\text{mg}$  resulted in no error. Nevertheless, when the memory is biased, errors caused by temporary effects may occur during high-fluence runs in static mode tests, leading to a non-negligible number of bits flips in static mode. Those errors disappeared after a power cycle. On the other hand, upset rates during dynamic mode testing are much higher due to errors in the control logic and require additional mitigation techniques to improve their radiation behaviour. The dynamic SEU cross-section values are in the same order of magnitude as those of commercial 90 nm SRAM dynamic test SEU cross-sections measured in [13]. Further tests are required to understand the impact of the fluence on the cross-section, to confirm latchup immunity at elevated temperatures as well as studying the sensitivity to high energy protons. Additional knowledge on the scrambling may allow a better understanding of the impact of the peripheral circuitry by the analysis of the physical bitmaps.

#### ACKNOWLEDGMENT

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## Annex VII

G. Tsiligiannis, L. Dilillo, V. Gupta, A. Bosio, P. Girard, A. Virazel, H. Puchner, **A. Bossler**, A. Javanainen, A. Virtanen, C. Frost, F. Wrobel, L. Dusseau, and F. Saigné, "Dynamic Test Methods for COTS SRAMs," in *IEEE Transactions on Nuclear Science*, vol. 61, no. 6, pp. 3095-3102, 2014.

*Contribution: the author took part in the test campaigns.*

# Dynamic Test Methods for COTS SRAMs

G. Tsiligiannis, L. Dilillo, V. Gupta, A. Bosio, P. Girard, A. Virazel, H. Puchner, A. Bosser, A. Javanainen, A. Virtanen, C. Frost, F. Wrobel, L. Dusseau, and F. Saigné

**Abstract**—In previous works, we have demonstrated the importance of dynamic mode testing of SRAM components under ionizing radiation. Several types of failures are difficult to expose when the device is tested under static (retention) mode. With the purpose of exploring and defining the most complete testing procedures and reveal the potential hazardous behaviors of SRAM devices, we present novel methods for the dynamic mode radiation testing of SRAMs. The proposed methods are based on different word address accessing schemes and data background: Fast Row, Fast Column, Pseudorandom, Adjacent (Gray) and Inverse Adjacent (Gray). These methods are evaluated by heavy ion and atmospheric-like neutron irradiation of two COTS SRAMs of 90 nm and 65 nm technology.

**Index Terms**—65 nm, 90 nm, COTS, dynamic test, heavy ions, multiple cell upset (MCU), neutrons, single event upset (SEU), SRAMs.

## I. INTRODUCTION

THE use of electronic devices in space applications requires their proper qualification according to certain guidelines such as the ones presented in [1]. Until the very recent years, specifications for such devices have been quite conservative. Most of the electronic components used in space are fabricated with radiation-hardened technologies. Such technologies are usually not as performing as the commercial ones in terms of speed, die area and power consumption. For this reason, since a few years, Commercial Off The Shelf devices (COTS) are considered for use in space applications, as long as they meet certain reliability constraints [2]. Meanwhile, taking

into account that Static Random Access Memories (SRAMs) are among the most commonly used storage devices in Systems on Chip (SoCs), and also the most performing ones, it becomes essential the exploration of the potentials of such commercial devices for use in space.

Qualification of electronic parts for use in space applications imposes their test under particle radiation to study Single Event Effects (SEEs), but also requires investigating their response to Total Ionizing Dose (TID). Several studies explore the response of COTS devices to these types of radiation effects. In [3] the response of two high performance 65 nm and 90 nm synchronous SRAMs is explored under high and low energy protons. The study presented in [4] reports the sensitivity of SRAM devices to protons with technologies from 65 nm down to 28 nm. Similarly, several heavy ion testing studies exist e.g. in [5], where the dependence of the SEE susceptibility of commercial SRAMs on the different ion energies has been explored. Additionally, the effect of the incident angle on the Multiple Bit Upset (MBU) in a commercial 65 nm SRAM under heavy-ion exposure has been studied in [6].

With the target of contributing to the effort of evaluating the usability of COTS devices in space, but also applying more efficient radiation testing techniques, in this paper, we explore novel approaches for testing SRAM memories under radiation, while operating in dynamic test mode. In the past, we have shown that dynamic mode testing can reveal certain faulty behaviors of SRAMs that are not easily detected while applying static mode testing. For example, in [7] it is shown that Single Event Functional Interrupts (SEFIs) and Single Event Latchups (SEL) can be revealed by testing SRAMs in dynamic mode. Additionally, in [8] it is shown that static mode testing may underestimate the failure rates of memory devices, while different dynamic tests are evaluated for their sensitization of an SRAM device when subjected to mono-energetic neutrons. Depending on the applied algorithm in dynamic test, the SRAM devices show different levels of sensitivity to ionizing radiation. Here, we introduce new test methods related to dynamic mode testing. In particular, we investigate the impact on the sensitivity of specific addressing sequences and data background when the devices are exposed to heavy ion and atmospheric-like neutron irradiation. These new methods are based on Fast Row (row after row addressing order), Fast Column (column after column addressing order), Pseudo-Random, Adjacent (Gray) and Inverse Adjacent (Inverse-Gray) access schemes, each one stimulating a different mechanism for the sensitization of the memory towards soft errors. We first experimentally tested one 90 nm and one 65 nm (with and without Error Correcting Codes respectively) asynchronous SRAM from Cypress Semiconductor using heavy ions with LET ranging from 1.8 MeV/(mg/cm<sup>2</sup>)

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TABLE I  
HEAVY IONS AND THEIR ENERGIES AND RANGES AND LET

Ion	Energy (MeV)	LET (Surface) (MeV/(mg/cm <sup>2</sup> ))	LET (Bragg Peak) (MeV/(mg/cm <sup>2</sup> ))
N	139	1.87	5.92 (191 $\mu$ m)
Fe	523	18.5	29.7 (75 $\mu$ m)
Kr	768	32.2	41.7 (68 $\mu$ m)
Xe	1217	60.0	67.9 (57 $\mu$ m)

up to 60 MeV/(mg/cm<sup>2</sup>) at RADEF (Jyväskylä, Finland [9]). To complement the study with additional results, the same components were irradiated also under atmospheric-like neutrons at ISIS (Didcot, UK [10]). Results show that for certain technologies, the addressing scheme may change the sensitivity of the memory over SEEs, and especially for large scale events such as SELs or SEFIs. The rest of the paper is structured as follows: Section II presents the experimental setup and analyzes the novel addressing schemes; Section III analyzes the results occurring from heavy ion and neutron irradiation while Section IV concludes the work.

## II. EXPERIMENTAL SETUP

### A. Devices and Facilities

The evaluation of the novel testing methods was performed utilizing different sources of ionizing radiation under which SRAM devices were exposed such as heavy ions and atmospheric-like neutrons. Heavy ion irradiation of the two SRAMs took place at the RADEF facility in the University of Jyväskylä in Finland [9] while atmospheric like neutron irradiation took place at the ISIS facilities in UK [10]. At the RADEF facility, Nitrogen, Iron, Krypton and Xenon-ions were used at the energy of 9.3 MeV/amu. The Linear Energy Transfer values (LET) for these ions were ranging from 1.8 MeV/(mg/cm<sup>2</sup>) for N up to 60 MeV/(mg/cm<sup>2</sup>) for Xe, as exposed in Table I. The atmospheric-like neutron beam of the ISIS facilities provides neutrons of energies of 10 MeV up to 800 MeV that follow the distribution of the atmospheric neutrons spectra. It is important to note that the fluence during both heavy ions and neutrons experiments was high enough to always provide more than 100 upsets per run.

Two open-top COTS asynchronous Cypress SRAMs of 65 nm and 90 nm bulk technology (CY62167GE MoBL and CY62177EV30 MoBL, respectively) were irradiated. In the RADEF facility, the devices had the top packaging chemically removed and they were inserted inside a vacuum chamber. Conversely, at ISIS, the devices were exposed directly to the beam without having to remove their lid. A built-in Error Correction Code (ECC) scheme is employed in the 65 nm SRAM, which was enabled or disabled during the test application. The ECC scheme allows a single bit correction per 32 bit data. The effective size of the two devices was 16 Mbit for the 65 nm SRAM and 32 Mbit for the 90 nm SRAM. While the 65 nm SRAM was composed of a single 16 Mbit die, the 90 nm device was a stacked device of two 16 Mbit monolithic dies. In order to consider only consistent data, for the 90 nm memory, only the top die (the one directly exposed) is taken into account when irradiated under heavy ions, because only a part of them

is able to penetrate to the bottom die. Conversely, when the 90 nm SRAM was exposed under atmospheric neutrons, both dies were considered since the dispersion of particles was very low from the first die to the second. The devices were placed in a socket mounted on a PCB and were driven by a Finite State Machine (FSM), implemented through FPGAs. The controlling FPGA was operating at a frequency of 50 MHz, which allowed accessing the device under test with a speed close to the maximum operational one. The test sink, comparison between expected data and actual read data, was made by the FSM. The detected errors were transmitted with a serial protocol to a computer located outside the vacuum chamber and the irradiation room. The powering of the memory and FPGA-based control cards was operated from distance as well. During the test application, the FPGA was placed at a certain distance from the beam center to avoid FPGA upsets, allowing the reliable execution of the experiments.

### B. Testing Modes

Two major categories of tests were applied to both SRAM devices: with the memories in *static mode* (retention) and in *dynamic mode* (continuously accessed). Static mode testing follows the typical guidelines, where a known data background sequence is written (*solid '0'* and *solid '1'* with all cells at '0' and '1' respectively, or with a *checkerboard* pattern like "10101010"), and after a certain time window the entire memory is read back. In case of an upset, the corrupted word is transmitted, along with the address and the timestamp. On the other hand, the dynamic mode testing requires that, during the irradiation time, the memory is accessed by read and write operations. To achieve that, we applied two different March algorithms: the "C-" [11] and the March "Dynamic Stress" (hereafter referred to as DS) [12]. These algorithms were repetitively executed during the whole irradiation time. A March algorithm is composed of several elements, and each element is composed of several operations. In Fig. 1 the elements and operations composing the March C- and March DS algorithm are displayed. The operations composing each element are applied to the entire address space of the memory either in an ascending order, or in a descending order according to the given indication for each element (arrows in Fig. 1). Similar tests have been applied to SRAM devices under ionizing radiation in previous studies such as [7].

### C. Novel Testing Methods

Up to now, during radiation testing, March algorithms made use of the standard logical addressing scheme when advancing through the memory address space, which very often employs scrambling techniques. The methods proposed in this work exploit different addressing schemes to enhance or reduce the sensitivity of the device. Five new addressing schemes for the dynamic mode testing are here introduced, and they stress the SRAM device at the cell level and at the peripheral level by sensitizing the I/O buffers and the power distribution grid among others. In these new schemes, the March elements are applied by accessing the cells in the following manners: fast row, fast column, pseudorandom, adjacent and inverse adjacent.

$$\begin{aligned}
& \{\uparrow (w0) \uparrow (r0, w1); \uparrow (r1, w0); \\
& \downarrow (r0, w1); \downarrow (r1, w0); \uparrow (r0)\} \\
& \quad (a) \\
& \{\uparrow (r1, w0, r0, r0, r0, r0, r0); \\
& \uparrow (r0, w1, r1, r1, r1, r1, r1); \\
& \uparrow (r1, w0, r0, r0, r0, r0, r0); \\
& \downarrow (r0, w1, r1, r1, r1, r1, r1); \\
& \downarrow (r1, w0, r0, r0, r0, r0, r0); \\
& \uparrow (r0, w1, r1, r1, r1, r1, r1)\} \\
& \quad (b)
\end{aligned}$$

Fig. 1. (a) March C- algorithm. This algorithm is composed of six elements and each element is composed of one or two operations (read/write). Each element (and thus the operations composing the element) is applied to the entire address space, before proceeding to the following one either in an ascending or descending order, indicated by the arrow prior the parenthesis. (b) Dynamic Stress (DS) March algorithm. This algorithm is based on the Read Equivalent Stress (RES) by applying multiple read operations to the accessed words. RES results to the weakening not only of the accessed words but also of the cells belonging to the same word line [12].

**Fast Row Addressing:** in this scheme, consecutive words are accessed horizontally considering the physical bitmap of the memory when the March elements are applied. More specifically, words are accessed on the same row starting from the leftmost part to the rightmost part before proceeding to the lower row. The Fast Row scheme sensitizes the memory by means of cell stress. The main sensitization mechanism is the action of Read Equivalent Stress (RES) [13], during which cells belonging to the same row are stressed multiple times (one for each read/write access to a cell belonging to the same row). When the word line is activated the RES is induced to the cells belonging to the same row because they share the same word line signal and are indirectly selected. During this indirect selection, the access transistors of the cells are activated, and the cells are connected to their bit lines that are both set at max voltage through the precharge circuits. Consequently, the voltage at the cell node set at '0' will undergo an increase of a few hundreds of millivolts, making the indirectly selected cell more prone to fault since the self-refreshing loop of the cell is weakened. The same principle lies behind the conception of DS algorithm that uses actual multiple read operations as described in [12].

**Fast Column Addressing:** following a similar principle with the *fast row* addressing scheme, *fast column* addressing scheme accesses consecutive words in a vertical order, following the columns of the memory. Thus, when a March element is applied, all the words of the leftmost column of the memory array will be accessed, prior continuing to the following column, until the entire address space is covered. Working in a different direction than Fast Row, Fast Column addressing scheme has the purpose to explore the impact of the design of the power lines that feed the memory array. In these devices (but also for many other memories), the power lines are vertically distributed in the cell array. By establishing a vertical addressing scheme such as Fast Column, it is expected that a certain electric stress to be induced to the power line, by grouped multiple accesses.

**Pseudorandom Addressing:** although the employed memories make use of an address scrambling scheme, the words are accessed in large consecutive regions of the array before transitioning to a different region. By using a Linear Feedback Shift

Register (LFSR) to select the address, a more efficient pseudorandom addressing scheme can be achieved. The Pseudo-Random address accessing scheme, is not meant to induce a stress in the memory cell array, but rather in the peripheral circuitry. Such a scheme is expected to stress significantly the periphery and in particular the address buffer and the address decoders. This is related to the fact that the bits of the address buffers will have to toggle much more frequently than for usual schemes in which a certain locality is met (either at the system level, or at the memory level thanks to the address scrambling of the memory). These changes in addressing bits induce also a high switching activity (thus stress) in the address decoder.

**Adjacent (Gray) Addressing:** while the proposed methods of addressing so far target the stressing of the memory, now we explore an addressing scheme that could reduce the device sensitivity to ionizing radiation. More specifically, an adjacent addressing scheme is considered which is implemented by making use of a Gray code. When applying a Gray code with consecutive words accessed by the March algorithms, consecutive addresses differ by only one bit, while the remaining bits remain the same. This addressing scheme is expected to stress as less as possible the address buffers and the address decoders of the memory. By applying at the same time the March Dynamic Classic algorithm, where each element is a single read or write operation with solid data background, the switching activity of I/O data buffers is minimized, thus further minimizing the overall switching activity. In (1), the Dynamic Classic algorithm is displayed

$$\{\uparrow (w0); \uparrow (r0); \uparrow (w1); \downarrow (r1)\}. \quad (1)$$

**Inverse Adjacent (Gray) Addressing:** while the application of a Gray code in the addressing scheme is expected to reduce to the minimum the switching activity of the periphery of the memory, the application of an exact opposite scheme works for the opposite target. By applying an Inverse Gray code, where the addresses of two consecutively accessed words differ in all their bits besides one, combined with a modified version of the Mats+March algorithm [16] displayed in Eq. (2), the switching activity of both the data I/O and the address buffers as well as the address decoders are maximized

$$\{\uparrow (r0w1); \uparrow (r1w0)\}. \quad (2)$$

While during dynamic mode testing the proposed addressing schemes may affect the final result of the test by modifying the sensitivity to the SRAM device, during static mode testing the addressing scheme does not affect the memory sensitivity. Thus, the addressing schemes will be explored in the following section only on dynamic mode testing. Static mode testing data will be also provided as reference.

### III. RESULTS AND DISCUSSION

As described above, tests have been applied to both SRAMs in static and dynamic mode. When it comes to asynchronous SRAMs, usually static mode testing allows the definition of the error rate of the memory devices in terms of Single Bit Upsets (SBUs) and Multiple Cell Upsets (MCUs). However, dynamic mode testing can reveal additional phenomena such as SEFIs

and SELs [8], [12]. Initially the results from the heavy ion irradiation will be exposed, and following some additional experiments with neutron irradiation will complement the obtained results. It has to be mentioned that in all the cross section calculations, the statistical error did not exceed 16% during heavy ions measurements and 10% during neutron experiments according to the log files provided by the facilities.

#### A. Static Mode Experiments

The graph in Fig. 2 shows the cross section as a function of the LET obtained when the memories were irradiated in static mode and with the ECC circuitry deactivated. The bit cross section was calculated while considering the total count of corrupted bits. In other words, corrupted bits participating to SBUs and MCUs were not distinguished, and thus an elevated cross section is expected. Eq. (3) describes this relation:

$$\sigma_{raw}(\text{cm}^2/\text{bit}) = \frac{\#\text{corrupted bits}}{\text{fluence} \times \text{size of memory}} \quad (3)$$

Making use of in-house developed software, we were able to group bit flips such as those concerned in a single MCU (few bit flips), but also take in account larger events such as SELs (hundreds of bit flips) and SEFIs (thousands of bit flips). As already presented in [7], large-scale events involving thousands of corrupted bits may occur at the devices under study. The types and origins of these events have been analyzed thoroughly in the aforementioned study. More specifically, it has been shown that thanks to the powering scheme implemented in these devices, only SBUs and MCUs may occur in static mode. However, during dynamic mode testing, larger events may be triggered such as micro-SELs or SEFIs as a result of the powering of the device at nominal voltage in the selected blocks. The fact that no power reset was required after the occurrence of such phenomena, resulted in the calculation of the devices' cross section by considering SBUs, MCUs, SEFIs and micro-SELs as single events. The clustering procedure has been performed by considering two criteria. The first criterion was the temporal locality of the corrupted bits, i.e. corrupted bits with a timestamp with a timing distance larger than a certain time span may not belong to the same event (the time window varies depending on the fluence and error rate). The second criterion was the spatial locality of corrupted bits, i.e. bits that had a topological distance larger than 3 bits on the physical bitmap were not considered to belong to the same event. These limits have been extracted during the processing of experimental data coming from extensive past irradiation experiments. By clustering the corrupted bits to events, we were able to observe a sensible difference in MCU and SBU distribution for the two technology nodes, when the devices operated in static mode. Eq. (4) expresses the event cross section, while Fig. 3 shows the event cross section of the results presented in Fig. 2. Finally, Fig. 4 gives an outlook of the MCU evolution as recorded for the different ions in both SRAM devices

$$\sigma_{event} = \frac{\#\text{clusters}}{\text{fluence} \times \text{size of memory}} \quad (4)$$

These histograms clearly show that MCUs in the 65 nm SRAM appear for lower LETs than for the 90 nm SRAM

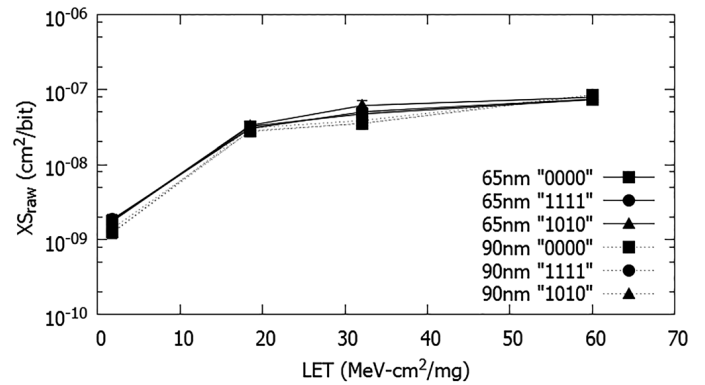


Fig. 2. Bit cross section evolution of the 65 nm and 90 nm SRAM for different LET values and data background. In this graph, the raw data are presented without classifying upsets as SBUs or MCUs, but considering the total count of the corrupted bits.

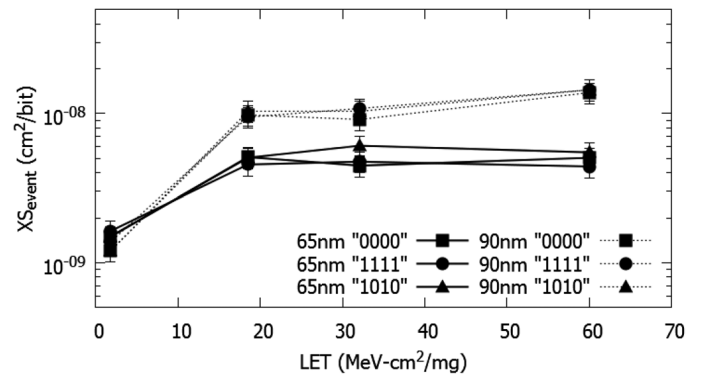


Fig. 3. Event cross section evolution of the 65 nm and 90 nm SRAM for different LET values. In this graph, the clustered data are presented according to the neighboring scheme described in the data processing subsection.

and their size (number of affected cells) is also considerably larger. Similar MCU distributions have been observed in the past, as in study [17]. This is the result of the shrinking of the sensitive node distance, while at the same time the area at which the charge is distributed remains the same, resulting to higher number of bits participating in MCUs for more scaled technologies.

#### B. New Addressing Schemes in Dynamic Mode Experiments

Continuing the results analysis, we present the data generated during the dynamic mode testing. When SRAMs are tested in static mode, they only perform data retention and the heavy ions affect mostly the cell array, which in this particular memory's case is kept in low power mode (low voltage sufficient to retain the cell contents), while the periphery is not operational. Conversely, when the memory is in dynamic mode, the array (more specifically according to the power scheme described, certain parts of it) is powered to the nominal voltage, thus latchup phenomena can be triggered. At the same time, the periphery is operational, and additional failures may occur such as SEFIs that are not likely to appear in static mode. Additionally, during the application of certain March algorithms such as DS, many consecutive read "stresses" are applied to the cells. Similarly, the *fast row* addressing scheme induces multiple Read Equivalent Stresses (RESS) to the cells that belong to the same word line

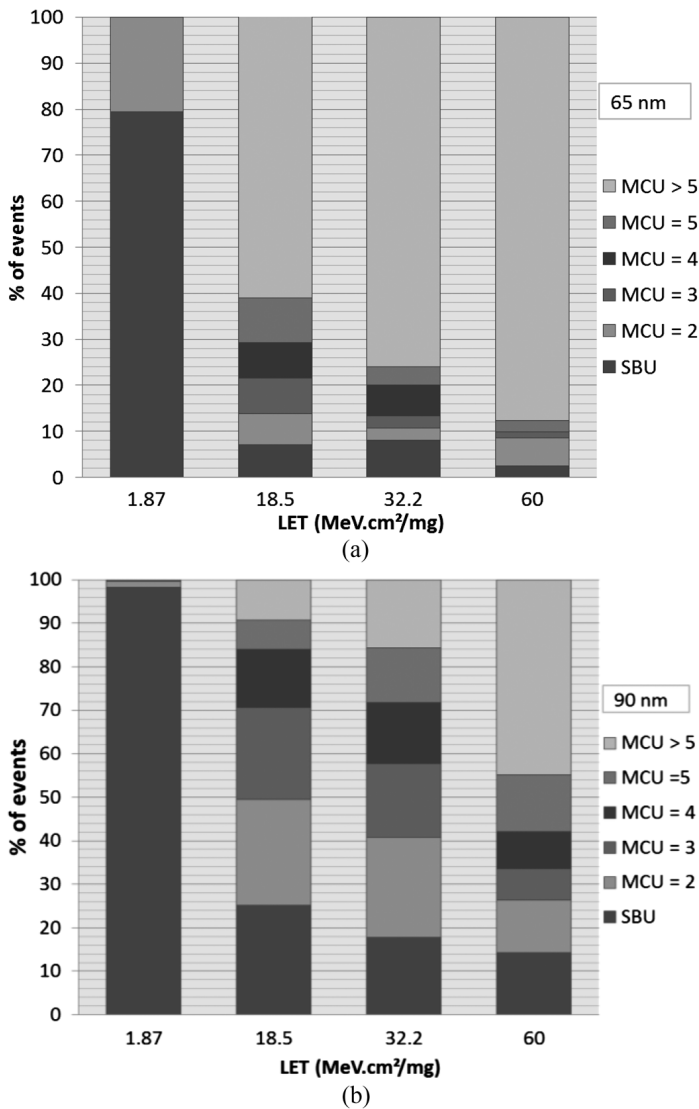


Fig. 4. SBU and MCU percentage as a function of LET: (a) for 65 nm SRAM and (b) for 90 nm SRAM.

[13], making them more sensitive to soft errors. In Fig. 5 the evolution of the event cross section is presented for the tests in dynamic mode, by using only the normal logical addressing scheme. Results from static mode testing are also depicted that serve as a reference. The results from Fig. 5 show that the algorithm sensitizing the most the 90 nm memory is the DS, while for the 65 nm memory most of the algorithms remain at similar levels. Due to the lack of experimental time, we did not concentrate data for all the available energies for the Dynamic Classic tests. However, results seem promising with respect to its low stress factor. Although the DS March test sensitizes the most the SRAMs, the inherent application of RES with the normal addressing may overlap other features that are meant to be exposed in this study during the application of the addressing schemes. For this reason, the March C- algorithm is applied by utilizing the mentioned addressing schemes. Fig. 6 exposes the retrieved results for the 90 nm and the 65 nm SRAMs.

In Fig. 6(a), we can observe that for the 90 nm “March C-” algorithm, the “Fast Row” scheme is the one leading to the highest cross section. This result is attributed to the action of

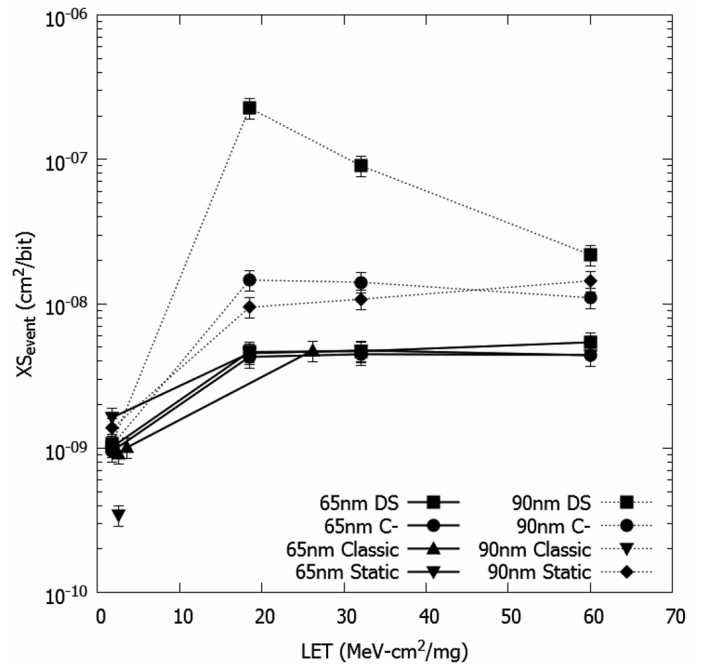


Fig. 5. Event cross section evolution of the 65 nm and 90 nm SRAM for different LET values while in dynamic mode. The data presented here are the clustered data, as they were recorded, including SBUs, MCUs but also SEFIs and SELs in which the device continued to operate. The applied tests were *Dynamic Stress* (DS) and *C-*, employing their normal addressing scheme.

RESs that are induced when the Fast Row scheme is applied. Similarly, comparing results obtained when applying the DS algorithm with the Fast Row scheme, and the normal addressing [observed in Fig. 6(c)], the latest was the one providing the highest cross section. This can be attributed to the saturation of the stress factor in a way where additional consecutive read accesses do not induce further stress to the cells belonging to the same row. The peak observed when the DS test is applied with normal addressing at the 18.51 MeV – cm<sup>2</sup>/mg, is the result of a SEFI corrupting several thousands of cells, thus inducing errors during the clustering process. Although most of the remaining algorithms seem to stress the memory in similar levels, it is evident that the combination of Dynamic Classic March test with the Gray addressing scheme is able to minimize the sensitivity of the memory. This result proves the hypothesis previously made that the switching activity of address, I/O buffers and address decoders has an actual impact on the device cross section. This observation can be utilized at the system level in order to add certain robustness, by exploiting for example the spatial locality of accessed words in a cache memory, thus reducing the stress induced in the peripheral circuitry. Considering the stress induced by the mMats+ algorithm combined with the inverse Gray addressing scheme, it seems that the 90 nm SRAM is not particularly affected with respect to the rest of the addressing schemes, and, in general, it does not overcome the stress induced by the Fast Row and the Fast Column schemes. However, further experiments with other particle sources may reveal different behaviors.

By observing the cross section evolution of the 65 nm memory in Fig. 6(b), it becomes apparent that the response of the device to all the applied algorithms remains at the same



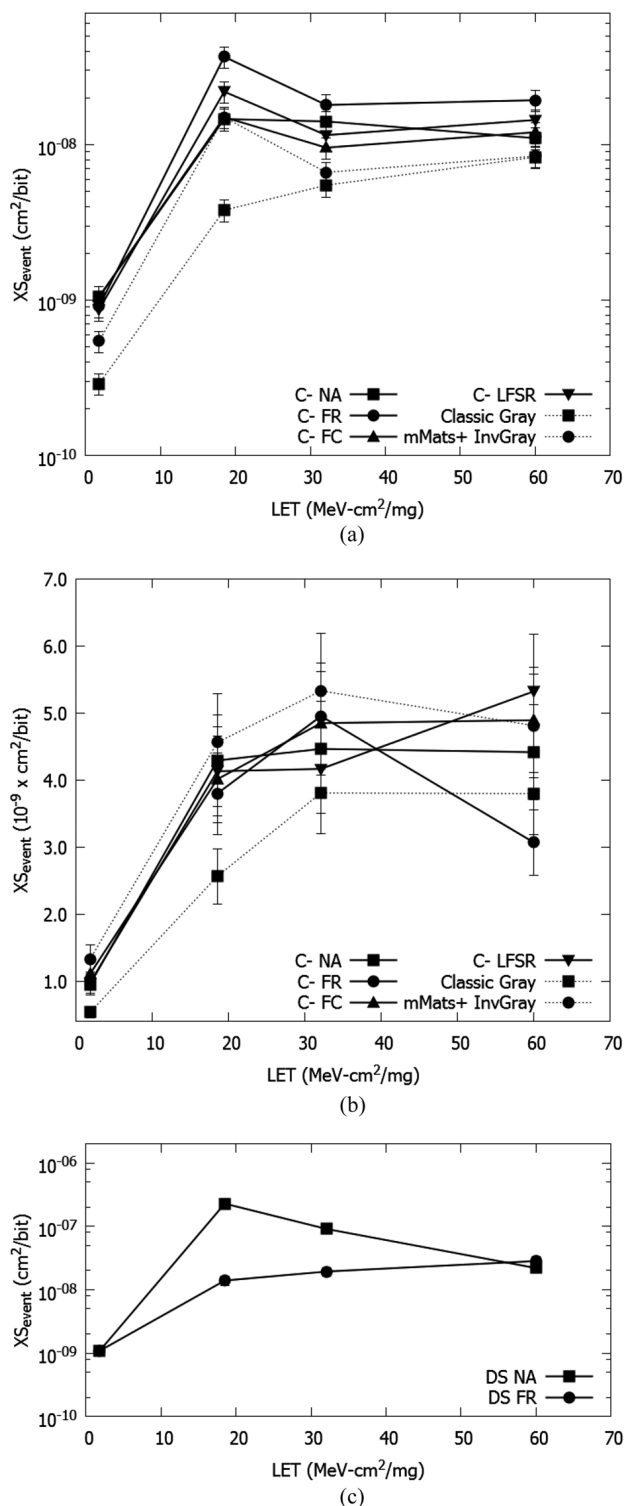


Fig. 6. (a) 90 nm SRAM response under heavy ion irradiation. (b) 65 nm SRAM response under heavy ion irradiation. The results from the March *C*-, the Gray Dynamic Classic and Inverse Gray mMats+ algorithms are shown. NA corresponds to the Normal Addressing Scheme, FR to the Fast Row, FC to the Fast Column, LFSR to the pseudo-random addressing scheme and Gray and InvGray to the Gray code and Inverse Gray code addressing schemes, respectively. (c) Dynamic Stress (DS) with normal addressing and Fast Row applied to the 90 nm SRAM.

levels with very small differences that may be due to statistical errors (max of 27% variation between the cross sections). This can be explained by the fact that several architectural improvements have been introduced in this device (65 nm) with

respect to its precursor (90 nm). An important improvement has been the minimization of the time window when an electric block is powered up during its selection for the application of read/write access. This also explains why no micro-SEs have been observed in the 65 nm memory, while they were numerous in the 90 nm device. Additionally, 65 nm devices are often manufactured to be more robust in terms of defects (resistive open for example [13]) w.r.t. 90 nm devices, thus making them less sensible to the stress induced by the RES mechanism or the multiple read accesses made by the DS algorithm. An interesting observation is that the Fast row and the pseudo-random addressing schemes display a different impact on sensitivity for different LET values. The lack of further information on the architecture details makes the explanation of such a trend rather difficult, considering also the low difference on their cross sections response that could occur simply due to a statistical error. The cross section fluctuations for ions with different LET and the various addressing schemes applied to the same test may be the result of a dependence of the sensitivity of the peripheral circuitry to the LET. Nevertheless, the trend of reduced sensitivity obtained with the application of the Gray code addressing scheme seems to be effective for both for 65 nm and 90 nm SRAMs. The connection, revealed in this study, between Gray code addressing scheme and sensitivity is very significant, as it relates the device sensitivity to the I/O buffer and address decoder stressing. The observation of similar results for two different technologies nodes strengthens this observation. Additionally, the Inverse Gray code combined with the mMats+ algorithm (maximization of switching activity) seems to sensitize the 65 nm SRAM more than the other combinations of addressing schemes and algorithms.

With respect to the novel addressing schemes here introduced for both SRAMs, it is worth mentioning that due to the large occurrence of micro-SEs and SEFIs, their masking effect on other events such as SBUs and MCUs makes the statistical study difficult, especially for the 90 nm SRAM (more prone to large scale event). Furthermore, due to the high ion flux combined with the high sensitivity of SRAM devices to direct ionization and the low speed of the serial protocol used for the communication, saturation of the test FSM might have occurred during certain tests. More specifically, the high error rate occurring to the SRAMs does not always allow the proper execution of the tests, stalling the application of the March elements due to delays induced by the communication. This may result to the continuous occupation of the test FSM with the transmission of the detected upsets, and thus the stress that each algorithm is meant to induce, will not be practically induced. The massive amount of data to be transmitted will result to the application of operations with large delays between them (thousands of corrupted bits to be transmitted in a few tens of seconds, along with the timestamp and the algorithm information), thus not exposing the intended stress factor that each addressing and operation is meant to induce. As a result, all the different algorithms will apply the same level of stress. This phenomenon has occurred mostly for the cases of Heavy Ions with the highest energy (above 32.1 MeV – cm<sup>2</sup>/mg), for which the sensitivity of the memories was highly increased. Nevertheless, even with some cases of saturation, results show that different addressing

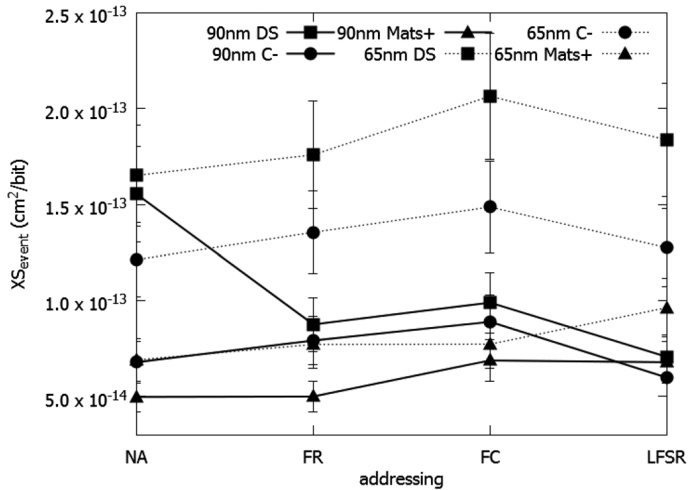


Fig. 7. 65 nm and 90 nm SRAM response under atmospheric like neutron irradiation. The NA corresponds to the Normal Addressing Scheme, FR to the Fast Row, FC to the Fast Column, LFSR to the Random addressing scheme, while the Dynamic Stress (DS), the March C- and the Mats+ algorithms were applied.

schemes can play an important role in the sensitization or robustness of the SRAM device.

In order to perform complementary measurements, and to avoid the saturation problem observed during heavy ion irradiation, the same devices were exposed to atmospheric-like neutron irradiation with the same algorithms (besides the adjacent Gray addressing and inverse Gray, due to reasons of limited experimental time). Fig. 7 displays the results obtained by applying different addressing schemes with different March algorithms.

In Fig. 7 the effect of the different March algorithms and their combination with addressing schemes becomes more apparent. With the neutron soft error rate being significantly lower (indirect ionization mechanism) than the one of heavy ions (direct ionization mechanism) and also a low flux ( $\approx 4 \cdot 10^4$  n/cm<sup>2</sup> flux of neutrons), previous saturation problems are overcome. Both the 65 nm and the 90 nm SRAMs show the same response under the three March algorithms, with the DS being the most sensitizing, while the Mats+ being the less sensitizing of them. Conversely to what has been observed during heavy ion irradiation, the addressing scheme showing the highest sensitization is the Fast Column, while the normal addressing, the pseudorandom and the Fast Row show to have a similar sensitizing action. The larger number of events during Fast Column may prove a dependence on the power lines stress, which are vertically positioned in both memories. The domination in terms of events of the DS March test shows that the hammering of the words with multiple read operations and the inducing RES to the word line prevails among other stress factors. One additional observation that was made comparing the heavy ion data with neutron data is a change of the overall sensitivity of the 65 nm SRAM with respect to the 90 nm SRAM. While during heavy ion irradiation the 65 nm SRAM shows to be significantly more robust than the 90 nm device, during neutron radiation this trend is reversed.

A possible explanation is the susceptibility of the 65 nm component to thermal neutrons. In fact, the study of the spectra of the ISIS neutron beam revealed that the thermal neutrons have almost the same distribution with fast neutrons.

### C. ECC Activation

The ECC scheme that is implemented in this memory allows the correction of 1 bit per 32 stored bits. These 32 bits can be divided either in two words of 16 bits or four words of 8 bits. When the ECC was activated during heavy ion irradiation, we observed that in static mode several bits were not corrected, leading to a cross section of  $\approx 10^{-10}$  cm<sup>2</sup>. Conversely, in dynamic mode, no failure of the ECC scheme has been observed. The achieved fluence for both static and dynamic mode test was of the order of 10,000 Fe ions for the tests concerning the ECC application. During static mode testing and when a certain value of fluence is achieved, an accumulation of events occurs and Multiple Bit Upsets (MBUs) start to appear. This means that more than one bits belonging to the same word can be corrupted, thus they cannot be corrected since the applied ECC can correct only one error at a time. This accumulation effect does not appear in dynamic mode testing, since the memory is accessed constantly under read/write operations. In particular, the time span between two write accesses is short enough to erase any single error, thus preventing error accumulation in the same word.

## IV. CONCLUSION

Novel addressing schemes have been presented for the testing of bulk SRAMs. It has been shown that Fast Row and Fast Column addressing schemes induce a significant stress to the memory, which can increase the device cross section up to 50%. Pseudo-Random schemes seem to stress the periphery of the memory by inducing SEFIs. The Adjacent (Gray) addressing scheme combined with the Dynamic Classic March test showed to minimize the memory cross section during dynamic mode. This result revealed that the switching activity (stress) of the address and I/O buffers and the address decoders affects the sensitivity of the memory. Consequently, reducing this stress factor may mitigate SEE phenomena. Finally, it was shown that DS test is the most effective to maximize the sensitivity of both SRAMs at the device level, proving the importance of the ‘hammering’ and Read Equivalent Stress factors. This observation combined with the addressing schemes results, showed that although static testing is important to reveal the sensitivity of an SRAM at the cell level, dynamic testing exposes the overall sensitivity of the device as a system. Error correction can significantly lower the failure rate to make COTS components suitable for space applications, unless retention mode is predominant.

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