# Development of an Efficient Methodology for Modeling Parasitic Effects within a Broadband Test Circuit

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Normandie Université

# THÈSE

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# Development of an Efficient Methodology for Modeling Parasitic Effects within a Broadband Test Circuit


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# GLOSSARY

| | |
|---|---|
| ENSICAEN | **E**cole **N**ationale **S**upérieure d'**I**ngénieurs de **CAEN** |
| RF | **R**adio **F**requency |
| mm | **M**illimeter-**W**ave |
| PCB | **P**rinted **C**ircuit **B**oard |
| VNA | **V**ector **N**etwork **A**nalyzer |
| DUT | **D**evice **U**nder **T**est |
| SOLT | **S**hort-**O**pen-**L**oad-**T**hru |
| ADC | **A**nalogue **D**igital **C**onverter |
| CW | **C**ontinuous **W**ave |
| CPW | **C**oplanar **W**ave **G**uide |
| TRL | **T**hru-**R**eflect-**L**ine |
| SOLR | **S**hort-**O**pen-**L**oad-**R**eciprocal |
| LRM | **L**ine-**R**eflect-**M**atch |
| TSD | **T**hru-**S**hort-**D**elay |
| HFSS | **H**igh **F**requency **S**tructure **S**timulator |
| 3D | **3 D**imensions |
| 2.5D | **2.5 D**imensions |
| ADS | **A**dvanced **D**esign **S**ystem |
| GS | **G**round-**S**ignal |
| GSG | **G**round-**S**ignal-**G**round |

| | |
|---|---|
| e.m | **E**lectromagnetic-**S**imulation |
| HBT | **H**eterojunction **b**ipolar **T**ransistor |
| MMIC | **M**onolithic **M**icrowave **I**ntegrated **C**ircuit |
| WLAN | **W**ide **L**ocal **A**rea **N**etwork |
| LNA | **L**ow **N**oise **A**mplifier |
| TX | **T**ransmitter **M**ode |
| RX | **R**eceiver **M**ode |
| PA | **P**ower **A**mplifier |
| ANT | **A**ntenna |
| GND | **G**round |
| TAR | **T**hru-**A**ntenna-**R**eceiver |
| TAT | **T**hru-**A**ntenna-**T**ransmitter |
| LAR | **L**ine-**A**ntenna-**R**eceiver |
| LAT | **L**ine-**A**ntenna-**T**ransmitter |
| RAR | **R**eflect-**A**ntenna-**R**eceiver |
| RAT | **R**eflect-**A**ntenna-**T**ransmitter |
| EVB | **E**valuation **B**oard |
| Cal-Kit | **C**alibration **Kit** |

# GENERAL INTRODUCTION

## 1. Thesis frame

The thesis subject is "Development of an Efficient Methodology for Modelling Parasitic effects within a Broadband Circuit". The thesis has been prepared in a common laboratory among Ecole Nationale Supérieure d'Ingénieurs de CAEN (ENSICAEN), Crismat laboratory, Presto Engineering Europe and NXP Caen.

The thesis subject was found, when engineers from the industrial environment start to complain form the difference in behavior between the test board and the final end product for the customers. The study begun by measuring an active device within a load board and to compare it with the same device soldered on the final application board. Many difficulties found during the characterization and modeling in order to locate the critical sources of errors which have lead to the next studies. Some works in this thesis are not only to resolve the error issues within the test board, but also to support our partners in industrial society to de-embed the errors from the final end product device and then be able to optimize the production yield.

## 2. Organization of thesis manuscript

The manuscript is organized in 5 chapters.

- ✓ Chapter 1 presents the context and state of the art for the evolution of network analyzer and calibration methods. The purpose of chapter 1 is to give a global background of the different calibration methods that have been used during measurements and our new approach for a TRL technique. The state of art of the method developed in this thesis will be presented in details in the next chapters.
- ✓ Chapter 2 presents the new approach for the TRL technique and de-embedding method with analytical equations. The different calibration steps and de-embedding have been described and an overview scheme for a full two-port board setup has been shown with the placement of standards and reference planes. At the end of this chapter an example has been studied for the first validation.

- ✓ Chapter 3 concentrates on the measurement methodology and extraction of results. The device to be tested has been described and the design model and fabrication for the TRL standards have been shown. Then an evaluation and verification of the measurements have been done using an evaluation board by a comparison the measurement results with calculated ones.
- ✓ Chapter 4 presents a multi-port TRL calibration method for a differential device. It shows a mixed-mode TRL de-embedding method and a four-port measurement method using a two-port Vector Analyzer Network (VNA). This chapter introduces also a double TRL calibration methodology for a DUT with differential input and single output.
- ✓ Chapter 5 concludes the thesis with a summary of the obtained results. The perspectives and technical challenges are presented.

# CHAPTER I

# CONTEXT AND STATE OF THE ART

## I.1 Introduction

Chapter I presents the objectives and motivation of the thesis in the background of the RF, mm-waves and the history of vector analyzers and calibration methods. This chapter is organized as follows. Paragraph I.2 shows the history of RF/microwave network analyzers. Then, paragraph I.3 presents an evolution of network analyzers. Paragraph I.4 shows a description of vector network analyzer with its measurement S-parameters and SOLT calibration errors. Furthermore, paragraph I.5 presents the self-calibration procedures and a de-embedding technique. Paragraph I.6 shows an overview scheme of a device embedded within a test socket in a load board, the place of reference planes where the measurements takes place and our new approach for TRL calibration. Finally, paragraph I.7 concludes chapter I.

## I.2 Context and motivation

The RF/microwave network analyzer has enabled the evolution of high frequency components and how they are designed. The basic ability to measure transmission, reflection, and impedance properties of circuits and devices enables engineers to optimize the performance of amplifiers, frequency converters, signal separation and altering devices, and other components. The performance of communications and defense systems depends heavily on the capabilities of these components and their test systems [1-3].

Network analyzers — being vector measuring instruments — have the unique ability to apply error correction techniques to improve their accuracy. Initially, short circuits were used to establish the maximum level of reflection magnitude. Precision transmission lines, sliding loads, and sliding shorts were used as impedance standards. Precision attenuators, such as piston and rotary vane variable attenuators, were used to establish transmission loss reference levels. Such calibration methods were able to remove some of the measurement scalar errors [4-6]. The 8407 and 8410 swept frequency vector network analyzers made it possible to correct some of the vector errors. The 8542 made full vector error correction possible for the first time [7]. It also allowed imperfect standards, such as the open-standard, to be denied by a device model. The short-open-load through calibration method was fully enabled.

A surge in research on VNA calibration methods brought us the through-reflect-line family of calibrations, which was implemented in the 8510 [8]. Measurement accuracy became limited by

the accuracy of the calibration standards. Thus, ultra-precision reference transmission lines and slotless female contacts were introduced. Electronic calibration was invented to simplify calibration; a single connection and a software controlled sequence completed the process. Multi-port, differential, and non-linear calibration methods and standards are the current challenges [9].

## I.3 Evolution of network Analyzer

Network Analyzer Architectures Historically, scalar network analyzers were a common tool used to characterize a network using only the magnitude of the signal. However, as network analysis technology matured, the development of digital components, such as analog-to-digital converters (ADCs), greatly simplified the design of vector network analyzers [10-12]. As a result, most modern VNAs are capable of measuring both scalar (magnitude) and vector (magnitude and phase) information about a signal.

### I.3.1 Scalar network analyzer

Scalar network analyzers typically capture a broadband signal and convert it to DC or low frequency AC in order to measure the power of the signal. Examples of the hardware used to accomplish this include diodes and thermoelectric devices. The main advantage of scalar network analyzers is that the hardware required for down conversion and power detection is relatively simple and inexpensive. In addition, because the detectors are broadband devices, it is unnecessary to re-tune the receiver to measure power at a different frequency.

Thus, performing a frequency sweep is as simple as re-tuning the frequency of the microwave source and measuring the power at each frequency step [13]. Due to their relatively simple architecture, scalar network analyzers are capable of relatively fast frequency sweeps. Note that some scalar network analyzers simplify the hardware even further by removing the reference sensor. In these designs, however, a slightly more complicated measurement sequence is required. A simplified block diagram of a scalar network analyzer is shown in Fig. I-1.

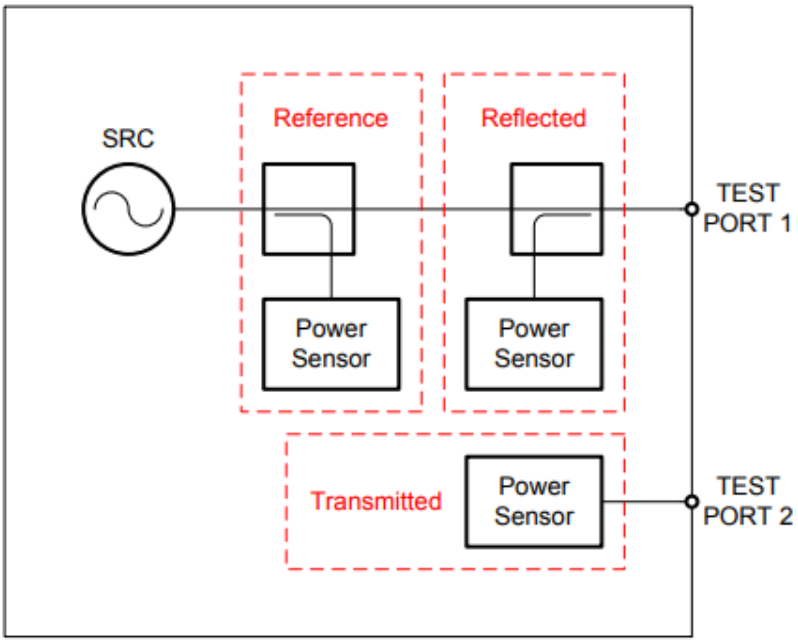



Figure I-1: Simplified Scalar network analyzer block diagram

Scalar analyzers make transmission or insertion loss measurements by using a signal source that sweeps repetitively over the frequency range of interest. If the reference detector is not available, you can calculate the transmission coefficient as the power ratio of the transmitted signal with and without the device under test (DUT) in the signal path.

While scalar network analyzers have the benefit of simplicity of design, they are also prone to inherent challenges. For example, broadband detectors are susceptible to spurious tones and broadband noise. In addition, because the calibration is scalar in nature, it is not as accurate as full vector calibration. Due to their lack of selectivity, scalar network analyzers tend to have limited dynamic range compared to vector network analyzers.

## I.4 Vector network analyzers

Vector network analyzers generally use full heterodyne receivers to measure both the phase and magnitude of signals and are often significantly more complex than scalar network analyzers. Measurements made with vector network analyzers are often more accurate, and the narrowband nature of the receivers provides better rejection of broadband noise and spurious tones, allowing for improved dynamic range. Furthermore, calibration can use more complex error models, which provide greater accuracy [15]. Due to the complexity of the heterodyne receiver architectures of

vector network analyzers, these instruments generally perform frequency sweeps more slowly than broadband scalar network analyzers. In addition, the added complexity often makes them more expensive.

The fundamental principle of a vector network analyzer is to measure the amplitude and phase of both incident and reflected waves at the various ports of the DUT. The general design of a VNA is to stimulate an RF network at a given port with a stepped or swept continuous wave (CW) signal and to measure the travelling waves, not only at the stimulus port but at all the ports of the network terminated with specific load impedances, typically 50 Ohms or 75 Ohms. Often, the device under test (DUT) is fabricated in a noncoaxial or waveguide medium and thus requires fixtures and additional cabling to enable an electrical connection to the VNA [16]. A typical but simplified VNA architecture is illustrated in Fig. I-5.

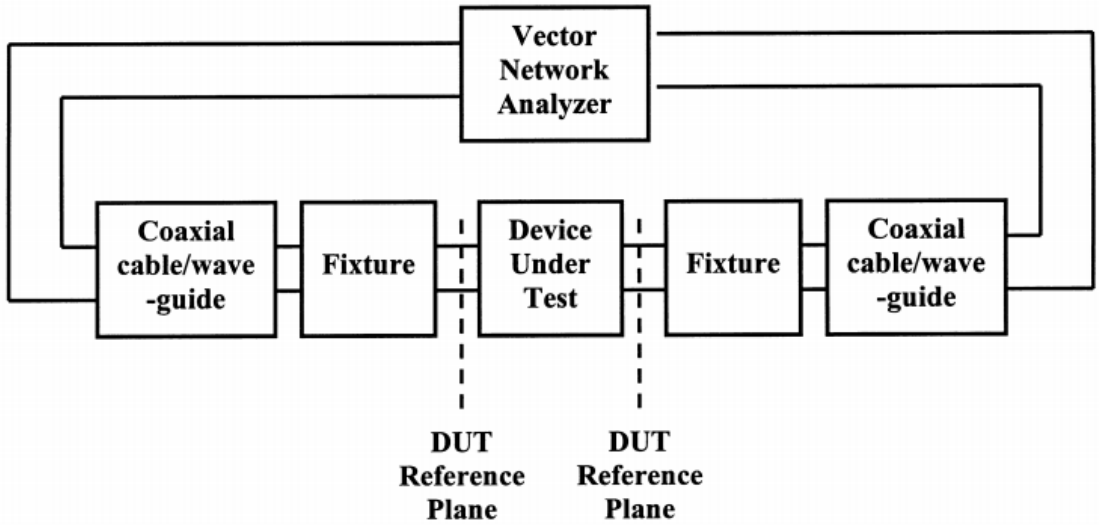



Figure I-2: Overall scheme for vector network analyzer

### I.4.1 Measuring of S-parameters

The measurement of S parameters assumes a generator making it possible to send a signal on the device and to measure the signal reflected. This assumes that we are working with a reference impedance $Z_0$ to determine the reflection coefficient. In most applications, this reference impedance, also called access impedance, is equal to 50 Ω.

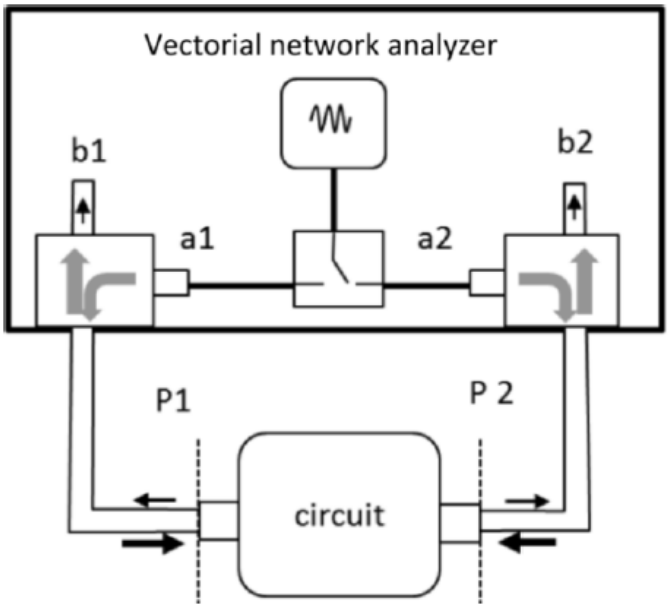



Figure I-3: Simplified operating principle of a vector network analyzer

The device is connected to the analyzer by high-quality radiofrequency cables over which the incident signal and the reflected signal propagate at the same time as shown in Fig. I-6. The measurement of $S_1$ parameters is based on the alternating application of signals $a_1$ and $a_2$ and the separation of the reflected signal from the incident signal at the coupler from the active access side, and the measurement of the signal transmitted from the other side [17]. The impedances of the different access points being equal to the reference impedance $Z_0$, we measure the S parameters.

These measurements allow us to take losses and dispersal in the cables into account, as well as directivity defects in the couplers [18-19]. These corrections are made via stages of calibration prior to any measurement. Calibration of a vector network analyzer enables us to correct the various systematic errors due to the test system: losses and directivity defects in couplers and conversion losses in detectors.

### I.4.2 SOLT calibration

The Short-Open-Load-Thru is the oldest, most used and widely adopted calibration technique. It has been developed for simple reflectometer VNAs assuming that forward and reverse measurements are made by independent setups [20-21]. The simplest form of calibration uses three loads: short circuit, open circuit, and 50 Ω load (SOLT: short, open, load, thru).

Standard calibrations are used to correct the effects of cables and vector network analyzer components in order to place reference planes in $P_1$ and $P_2$.

In a vector analysis bench, we must correct the following various types of errors:

- Systematic errors: losses and directivity defects in couplers, detector conversion losses, signal frequency variations, etc.
- Random errors: component noise, switcher and connection repetitiveness.
- Characteristic derivatives: thermal derivatives, contact aging, physical modification of cables, etc.

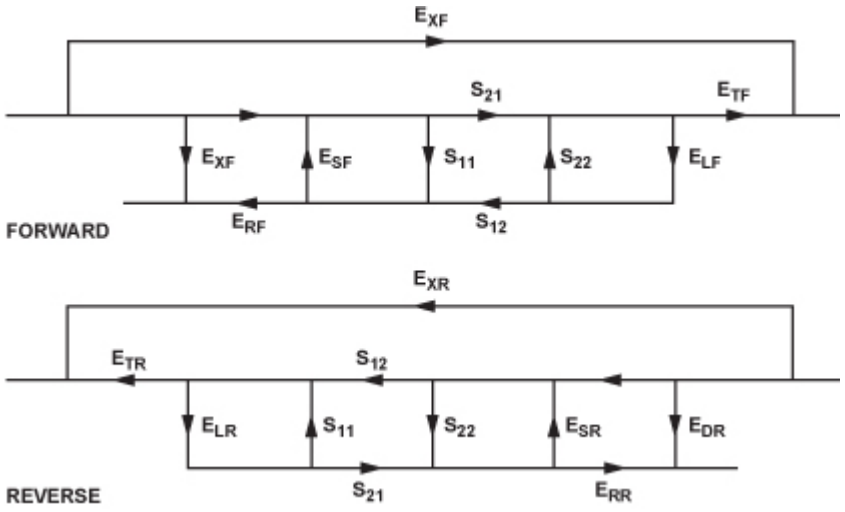



Figure I-4: Systematic errors in vector network analyzer

Although the location of the reference plane on VNA measurements is one factor that affects measurement results, VNAs are also subject to a range of inherent instrument impairments that can also be accounted for through calibration. In general, there are four main contributions to this imperfection.

The various errors in Fig. I-7 correspond to:

- $E_{DF}$, $E_{DR}$: directivity;
- $E_{RF}$, $E_{RR}$: reflection tracking;
- $E_{XF}$, $E_{XR}$: isolation;

- $E_{LF}$, $E_{LR}$: Load match;

F & R: forward and reverse respectively.

The sources of error listed above are often referred to as systematic sources of error because they systematically affect the measurement at all times [22]. The effects of systematic errors on a measurement result, shown in Fig. I-4, can largely be removed through calibration.

## I.5 Self calibration methods

Network analyzer self-calibration procedures for the eight-term error model have been available for over 20 years [23-24]. The self calibration methods have been developed for double reflectometer VNAs as shown in Fig. I-3. As far as only one setup is considered, the model can be described by a unique flow chart where some terms in Fig. I-4 are equal (e.g $E_{SF} = E_{LR}$). A correction procedure is sometimes used to eliminate the switching errors due to a non-ideal source and load match. This, together with the isolation measurement, extends the eight-term model essentially to the 12-term error model.

The accuracy of network analyzers is enhanced by calibrating the setup at its measurement ports. Usually this is performed by applying the well-known 12-term procedure, employing the standards thru, match, short and open [25-26]. While the 12-term procedure depends only on fully known standards, there are some other methods in use allowing for partly unknown standards.

There are many self calibration techniques which differ by the kind of standards and the math adopted. They were introduced in as TSD (thru, short, delay), in as LRM (line, reflect, match) [27-28] and in as TRL (thru, reflect, line) [29]. They can be implemented in a double reflectometer as shown in as well as in other configurations.

Here the more common ones are presented and in particular those called:

- **T**hru-**R**eflect-**L**ine
- **L**ine-**R**eflect-**M**atch
- **T**hru-**S**hort-**D**elay

LRM is a particular case of TRL which has many characteristics as broad band performances and where the VNA reference impedance is set by the load.

### I.5.1 TRL procedure

This technique uses a Thru which is typically either a direct connection between the ports, a longer Line and an unknown reflection standard [30-32].

The main characteristics of the TRL calibration are:

1. The propagation constant of the line is obtained as a by-product of the calibration.

2. The characteristic impedance of the line sets the reference impedance of the VNA.

3. The length difference between the line and the thru does not have to be a multiple of the wavelength.

This calibration makes it possible to place reference planes on a printed circuit using calibration components created by the user, compatible with the device being tested [33-36]. Calibration devices are shown in Fig. I-5.

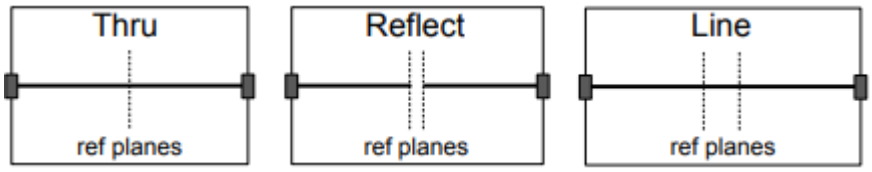



Figure I-5: TRL calibration standards

The creation of the calibration components in Fig. I-5 must comply with the following rules:

- Thru: the two access points are connected to one another by a line of length $La_1 + La_2$.
- Reflect: a printed circuit is created in which the lines are open at the level of the reference planes.
- Line: we need a line with an excess length $\Delta L$ on a frequency band. We can show that it must introduce a phase difference, different from $k\pi$, between the low frequency and the high frequency of the band. The minimum measurable phase difference is estimated at 15°, and the phase introduced by the line between access points between 15° and 165°, for a band ratio $F_{max}/F_{min} = 11$.

For all devices, the access points must be as reproducible as possible in order to minimize errors.

## I.6 Industrial context

The development of interconnected devices and communication technologies has put on the market billions of RF semiconductor units. The modulation scheme complexity, always increasing to improve the data rate pushes the RF technology towards its limits in term of noise level or signal quality. Testing such parameters with the right accuracy is then becoming really challenging. Previous methods, only based on simple rules to design a clean RF load boards are not enough to keep the expected yield level. It is now required to have an accurate picture of all losses and distortions brought by the test fixture to the measurement. The challenge is here to be able to set the test limits with more accuracy, in order to clearly isolate the device performance from the test fixture influence.

### I.6.1 Load board

For its measurement, a device under test (DUT) is embedded into a socket which is embedded in a measurement board. The measurement is performed using a vector network analyzer (VNA) at the outer accesses of the board after an appropriate calibration [37-38]. The de-embedding is a method which consists of removing the unwanted elements (the board and the socket) in order to reach the characteristics of the circuit itself as shown in Fig. I-6 below.

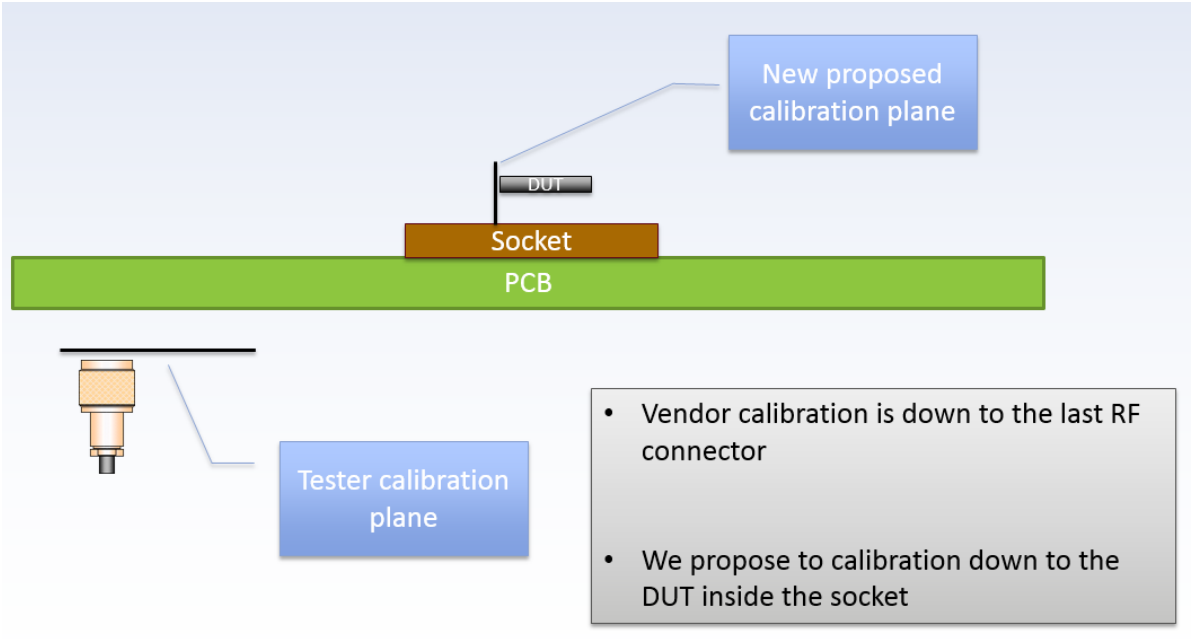



Figure I-6: Overview Scheme

To make the de-embedding possible, a calibration is necessary. It consists of finding the right method to extract the parameters of the input and output accesses. We propose to define convenient elements that will be placed instead of the circuit. Many methods exist, but they use calibration circuits that are not compatible with the geometry of our equipment.

One of the most accurate and efficient method is TRL (Thru-Reflect-Line). The detailed analytical calculation is shown in **Appendix 1**. But the characteristic impedance of the line must be known. That means that we need to design the line on a well-known substrate with well-known geometry [39].

De-Embedding is a process that removes the effects of unwanted portions of the structure that are embedded in the measured data by subtracting their contribution. However, just as in an RF measurement, understanding of the inner workings of the process can sometimes allow you to design our circuits in such a way as to produce more accurate results or analyze our circuit more efficiently.

### I.6.2 Device under test (DUT)

For control, DUTs are placed inside a test board. Measurement setups can collect the information between the input and output ports of the board. We must remove by calculation the parts of the board situated between the board ports and the DUT ports. This operation is called "de-embedding". It uses vector network analyzer measurements.

The measurement test board is described in Fig. I-7. It appears three two-ports: the input access (between $P_0$ and $P_1$), the output accesses (between $P_2$ and $P_3$) and the device under test itself (between $P_1$ and $P_2$). They can be described by their S-parameters (or other parameters).

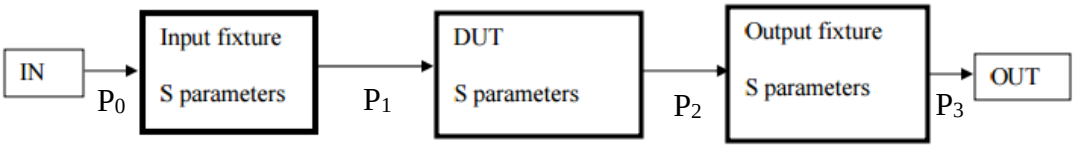



Figure I-7: Overview two-port board

In order to get the total response of the system we will have to handle the S- parameters matrices. In order to simplify the task somewhat, it is convenient to use the T-parameters representation of the block. Therefore:

$$\mathbf{T_{measured} = T_{IN} * T_{DUT} * T_{OUT}} \quad [I\text{-}1]$$

## I.7 Conclusion

The calibration of two-port VNAs has greatly enhanced the measurement accuracy of microwave devices. In the following chapter we will show the analytical calculation of TRL calibration methodology and de-embedding technique, based on the eight-term error model of a two port vector network analyzer measurement system. Then eight error terms of fixtures are derived directly from the S parameters of the fabricated calibration standards measured from the coaxial reference plane.

To test our algorithm, first we use a load board with a socket be measured which is used normally in production to test thousands of devices between reference PCB board plane ( RF coaxial connectors) within short period of time and an evaluation board with a soldered device and without socket to measure the device's behavior.

# CHAPTER II

# TRL CALIBRATION TECHNIQUE AND DE-EMBEDDING METHOD

## II.1 Introduction

In measuring circuits at microwave frequencies, it is essential to access the DUT (Device Under Test) at a known reference plane, particularly when measuring devices whose characteristics are affected simultaneously by input and output impedances. A major problem encountered when using vector network analyzer to obtain the S-parameters of a DUT is the need to separate the errors of the fixtures, transmission lines etc... The S- parameters of those errors are consequently introduced into the measurement results as errors. To get the S parameters of DUTs, the effect of the errors should be removed [40-41].

Various calibration techniques are used to measure devices at microwave frequencies. One of those techniques using standards of a "thru" line, "reflect". TRL is one type in a family of two-port self-calibrations that better support on-wafer measurements and test fixtures.

The chapter is built around four main sections:

- The first section describes the methodology used to perform our new approach for TRL calibration.
- The second section presents in details the analytical calculations for achieving calibration and de-embedding for a single input/output device.
- The third section shows an extraction of device's behavior by our study.
- The final section discusses the final results of an applied example which by comparison with simulations confirm the studied done.

## II.2 Methodology description for TRL calibration

We plan to use the TRL calculations in an original manner. As the TRL standards are not available in our technology, we design and fabricate specific standards that are inspired from TRL [42]. Each standard is previously characterized, either with an electromagnetic simulation or an on-wafer measurement.

The Thru-Reflect-Line (TRL) calibration algorithm and several of its' variants are frequently described as providing the best opportunity for the most accurate VNA measurements [43]. Foundations for this perspective are partially driven from the fact that, unlike with some calibration

algorithms (Short-Open-Load-Thru for example) the response of the calibration standards need not be known a priori. This allows the standards to be patterned in the same substrate and with the same launch transition behavior as the device under test (DUT).

### II.2.1 Standards definition

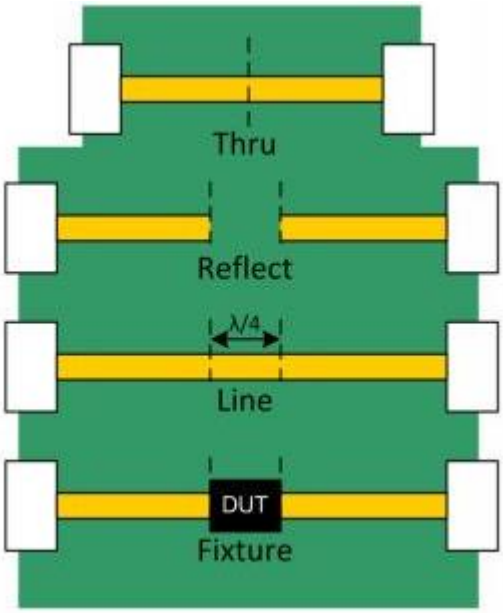



Figure II-1: TRL calibration model

The creation of the calibration standards in Fig. II-1 must comply with the following rules:

- **Thru:** Ideally, a zero length through line where the measurement ports are directly connected.

  The S-matrix of thru is:

$$S = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \qquad \text{[II-1]}$$

- **Reflect:** A highly reflective device (most often a short or open). The absolute reflection coefficient is derived from the additional standard measurement information, but knowledge of the electrical length must be within one-fourth wavelength to ensure proper identification of the standard.

It is important to use the identical reflection standards to calibrate both ports. If the phases of the reflection coefficients are equal, the reference planes are situated in the middle of the thru. A printed circuit can be created in which the lines are open at the level of the reference planes. For on-wafer measurement, the reflect may be obtained by lifted probes.

The S-matrix of reflect is:

$$\mathbf{S} = \begin{pmatrix} \Gamma & T \\ T & \Gamma \end{pmatrix} \qquad \text{[II-2]}$$

Where |T|<<|**Γ**|

- **Line:** A nonzero length through line with the same intrinsic impedance as the through standard. The difference between the phase shifts of the line and thru standards require a minimum of 15 degrees to 165 degrees. It is not necessary to know the propagation constant because it is calculated from the extra measurement information. But the reference impedance is equal to the characteristic impedance of the line. It must be known before measurement (when it exists for TEM and quasi-TEM modes) if necessary by the use of an electromagnetic simulator.

  The required phase relationship between the thru and line standards creates restrictions on the frequency span that can be measured with a given though and line combination. If a larger frequency span is needed, use multiple lines must be used.

  The S-matrix of line is:

$$S = \begin{pmatrix} 0 & X \\ X & 0 \end{pmatrix} \qquad \text{[II-3]}$$

For an actual line $X = e^{-\gamma l}$

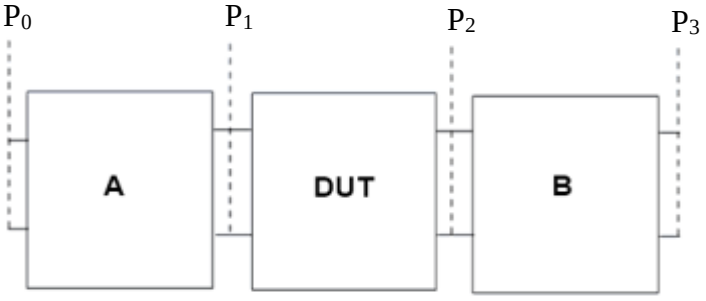



Figure II-2: Two-port measurement setup

Fig. II-2, describes the measurement setup. Planes $P_0$ and $P_3$ are the input and output ports of the board. A first full-two-port calibration is made between these planes (e.g. SOLT between SMA connectors). The two-port A and B represent respectively the input and output accesses of the board. $P_1$ and $P_2$ are the reference planes of the DUT. The DUT and the calibration elements are placed between $P_1$ and $P_2$.

### II.2.2 Calculation of the error terms

For a full analytical calculation about the TRL calibration and de-embedding method please refers to **appendix 1** at the end of manuscript. Generally, the calculation is presented with matrices handling [44]. The proposed calculation is completely analytical and can be easily introduced into a measurement software for fast quick operations.

The flow chart on the left handed side shows the system of errors terms distributed within the setup of two-port measurement. It is the 8-term error model which should have been described in chapter 1. While the right handed one corresponds to the S-parameters measured by the VNA between planes $P_0$ and $P_3$.

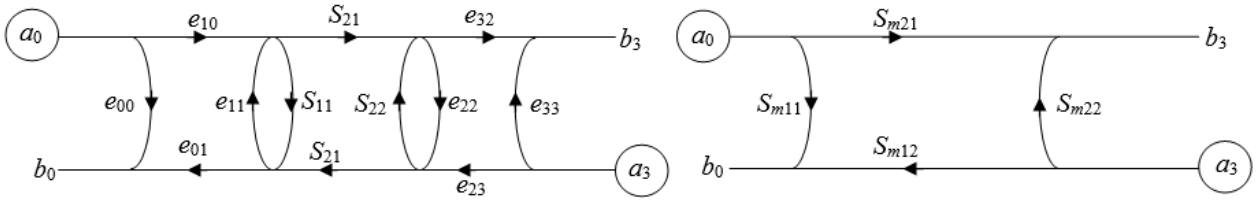



Figure II-3: Distribution of system of errors within two-port network

## II.3 DUT embedded within a PCB

For a TRL calibration between VNA reference ports, the input impedance of a planes $P_1$ and $P_2$ of the VNA are not matched. In our case we deal with corrected measurements after the SOLT calculation between the RF coaxial input/output connectors. The "corrected VNA" ports are matched.

In our case, we cannot have exact TRL standards. We must find a new method compatible with our facilities [45-47]. The De-embedding technique that we propose in our project, must extract the input and output error terms at the level of DUT i.e RF feed transmission lines effects, fixture

effects etc... and to shift the reference test planes from RF coaxial connectors till the position of pins where the device under test lies.

Fig. II-4& II-5 show the load board setup. The DUT is put in the middle of the test socket which is embedded into a board. $P_1$ and $P_2$ are defined in the middle of the socket, $P_0$ and $P_3$ are defined in the SMA connector reference planes.

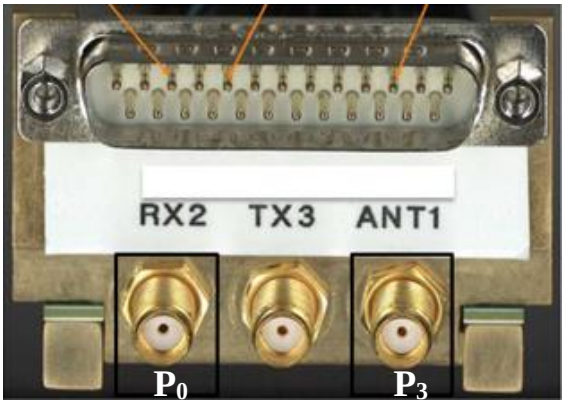



Figure II-4: RF coaxial input/output ports

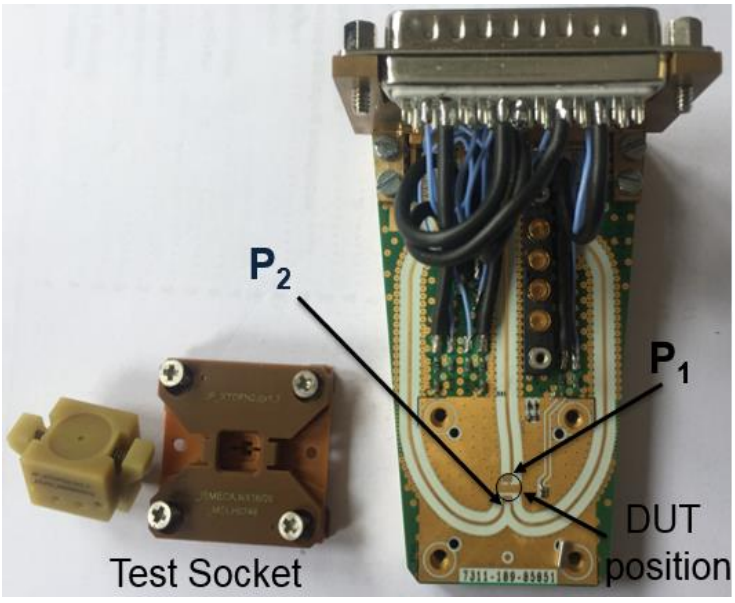
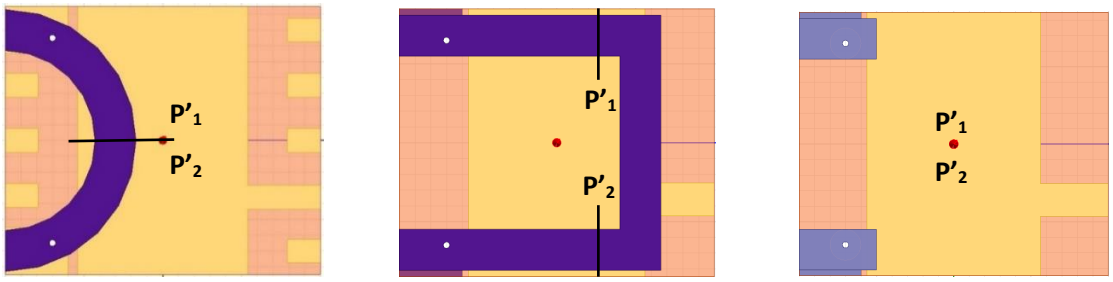



Figure II-5: Load board setup

We will design and fabricate standards that are not exactly TRL standards as shown in Fig. II-6.




Thru Line Reflect

Figure II-6: Examples of fabricated standards

The calibration standards have been chosen not too far from the TRL (thru-reflect-line) standards. But for our method, their S-parameters must be known. In a first approach, they have measured by on-wafer GS probes or simulated with an E.M simulator (e.g HFSS, CST). So, we know exactly what we put between planes $P_1$ and $P_2$ during the calibration.

## II.4 Two-port board setup

The calibration standards placed between $P_1$ and $P_2$ are virtually split into three two-ports. In the middle, between the fictitious planes $P'_1$ and $P'_2$, the theoretical TRL standards are placed as shown in Fig. II-7. That means that the two-ports A' and B' transform the actual calibration elements into TRL virtual standards.

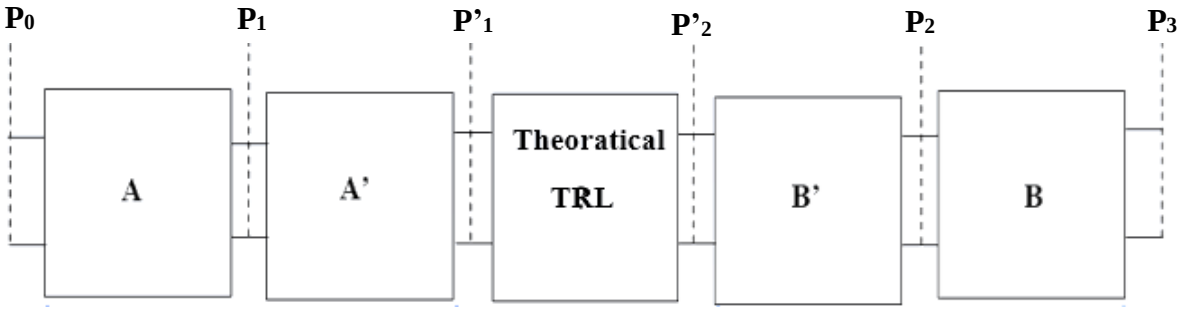



Figure II-7: Reference plane's distribution for two-port board

We assume that each standard consists of an ideal TRL standard (between $P'_1$ and $P'_2$ in Fig. II.2) embedded into fictitious two-ports A' (between $P_1$ and $P'_1$) and B' (between $P'_2$ and $P_2$). That means that the two-ports A' and B' transform the actual calibration elements into TRL virtual standards.

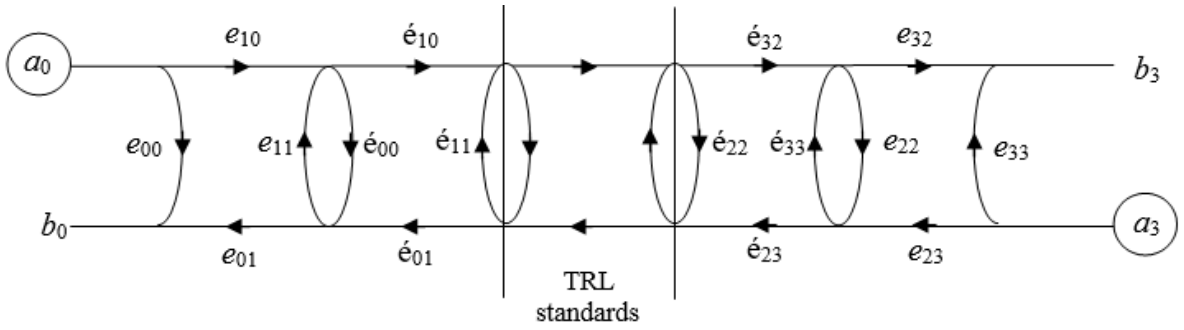



Figure II-8: Identification of errors for a two-port board

Once the three calibration standards have been measured between $P_1$ and $P_2$, the board including the elements is measured using the SOLT calibration between $P_0$ and $P_3$. A TRL calculation gives the characteristics of A' and B'. The board including the elements is measured between $P_3$ and $P_4$. Another TRL calculation gives the characteristic of AA' and B'B.

The characteristics of two-port A and B will be useful for the de-embedding. During the measurement itself, the DUT is placed between planes $P_1$ and $P_2$. The measurement is made between $P_0$ and $P_3$. Using transfer matrices, we have to remove A and B to reach the DUT parameters [48].

In the following, the "TRL" calibrations are simplified by:

- They use calibrated measurement. After correction, the situation is like if $a_3$=0 for the forward measurements and $a_0$=0 for the reverse measurement.
- All the two-ports are physically reciprocal passive. So, in the calculation of the error terms $e_{10}$=$e_{01}$ and $e_{32}$=$e_{23}$.

### II.4.1 Calibration steps

**Step 1:**

On-wafer GS calibration between $P_1$ and $P_2$ when necessary.

**Step 2**

On-wafer measurement between $P_1$ and $P_2$ with the three circuits between $P_1$ and $P_2$.

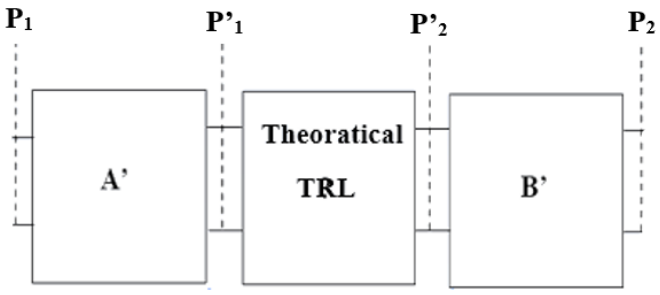



Figure II-9: Planes configuration for a standard

TRL calculation giving $e'_{ij}$ or electromagnetic simulation.

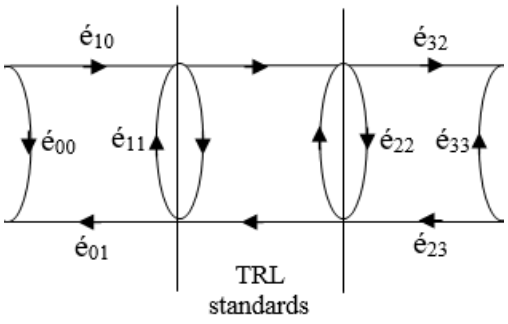



Figure II-10: Error terms in a standard

$$\mathbf{S}_{\mathbf{A}'} = \begin{pmatrix} e'_{00} & e'_{10} \\ e'_{10} & e'_{11} \end{pmatrix} \qquad \mathbf{S}_{\mathbf{B}'} = \begin{pmatrix} e'_{22} & e'_{32} \\ e'_{32} & e'_{33} \end{pmatrix} \qquad \text{[II-4]}$$

$$\mathbf{T}_{\mathbf{A}'} = \begin{pmatrix} -\dfrac{e'_{00}e'_{11} - e'^{2}_{10}}{e'_{10}} & \dfrac{e'_{00}}{e'_{10}} \\ -\dfrac{e'_{11}}{e'_{10}} & \dfrac{1}{e'_{10}} \end{pmatrix} \qquad \mathbf{T}_{\mathbf{B}'} = \begin{pmatrix} -\dfrac{e'_{22}e'_{33} - e'^{2}_{32}}{e'_{32}} & \dfrac{e'_{22}}{e'_{32}} \\ -\dfrac{e'_{33}}{e'_{32}} & \dfrac{1}{e'_{32}} \end{pmatrix} \qquad \text{[II-5]}$$

- **Step 3**

Coaxial SOLT calibration between $P_0$ and $P_3$

- **Step 4**

Measurement between $P_0$ and $P_3$ with the three circuits between $P_1$ and $P_2$.

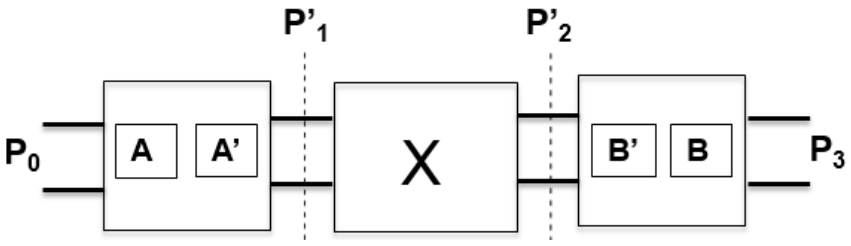



Figure II-11: Planes configuration for a measurement setup

TRL calculation giving $e''_{ij}$.

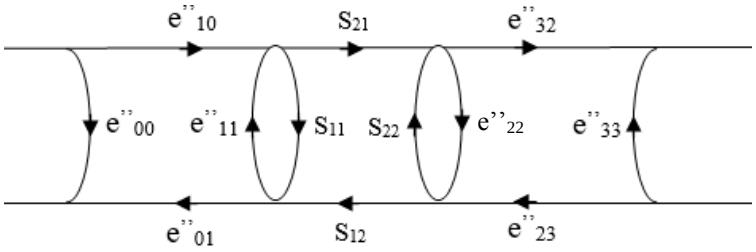



Figure II-12: Distribution of error terms between RF coaxial connectors

$$\mathbf{S_{AA'}} = \begin{pmatrix} e''_{00} & e''_{10} \\ e''_{10} & e''_{11} \end{pmatrix} \qquad \mathbf{S_{B'B}} = \begin{pmatrix} e''_{22} & e''_{32} \\ e''_{32} & e''_{33} \end{pmatrix} \qquad \text{[II-6]}$$

$$\mathbf{T_{AA'}} = \begin{pmatrix} -\frac{e''_{00}e''_{11}-e''^{2}_{10}}{e''_{10}} & \frac{e''_{00}}{e''_{10}} \\ -\frac{e''_{11}}{e''_{10}} & \frac{1}{e''_{10}} \end{pmatrix} \qquad \mathbf{T_{B'B}} = \begin{pmatrix} -\frac{e''_{22}e''_{33}-e''^{2}_{32}}{e''_{32}} & \frac{e''_{22}}{e''_{32}} \\ -\frac{e''_{33}}{e''_{32}} & \frac{1}{e''_{32}} \end{pmatrix} \qquad \text{[II-7]}$$

### Step 5

Extraction of the error model

$$\mathbf{T_A} = \mathbf{T_{AA'}}\,\mathbf{T_{A'}}^{-1} \quad ; \quad \mathbf{T_B} = \mathbf{T_{B'}}^{-1}\,\mathbf{T_{B'B}} \qquad \text{[II-8]}$$

### II.4.2 DUT measurements

Measurement between $P_0$ and $P_3$ with the DUT between $P_1$ and $P_2$.

Measured S-parameters:

$$\mathbf{S_m} = \begin{pmatrix} S_{m11} & S_{m12} \\ S_{m21} & S_{m22} \end{pmatrix} \quad \text{[II-9]}$$

$$\mathbf{T_m} = \begin{pmatrix} -\frac{S_{m11}S_{m22} - S_{m12}S_{m21}}{S_{m21}} & \frac{S_{m11}}{S_{m21}} \\ -\frac{S_{m22}}{S_{m21}} & \frac{1}{S_{m21}} \end{pmatrix} \quad \text{[II-10]}$$

Extraction of device's parameters by de-embedding:

$$\mathbf{T} = \mathbf{T_A^{-1}} \mathbf{T_m} \mathbf{T_B^{-1}} \quad \text{[II-11]}$$

$$\mathbf{S} = \begin{pmatrix} \frac{T_{12}}{T_{22}} & \frac{T_{11}T_{22} - T_{12}T_{21}}{T_{22}} \\ \frac{1}{T_{22}} & -\frac{T_{21}}{T_{22}} \end{pmatrix} \quad \text{[II-12]}$$

## II.5 First validation of the method

The measurements have been simulated using Keysight's ADS as shown in the configuration setup of Fig. II-13. The calibration standards are described in Fig. II-14.

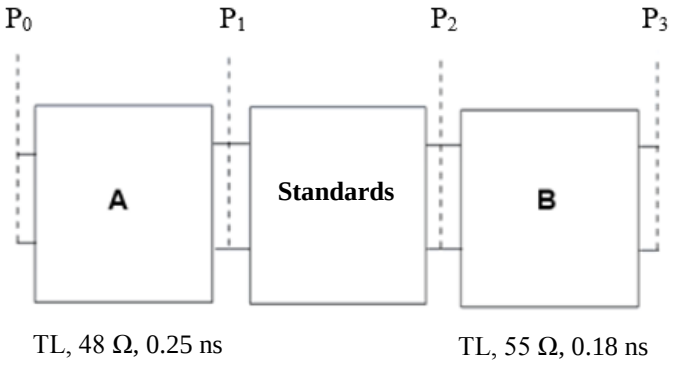



Figure II-13: Simulated calibration setup

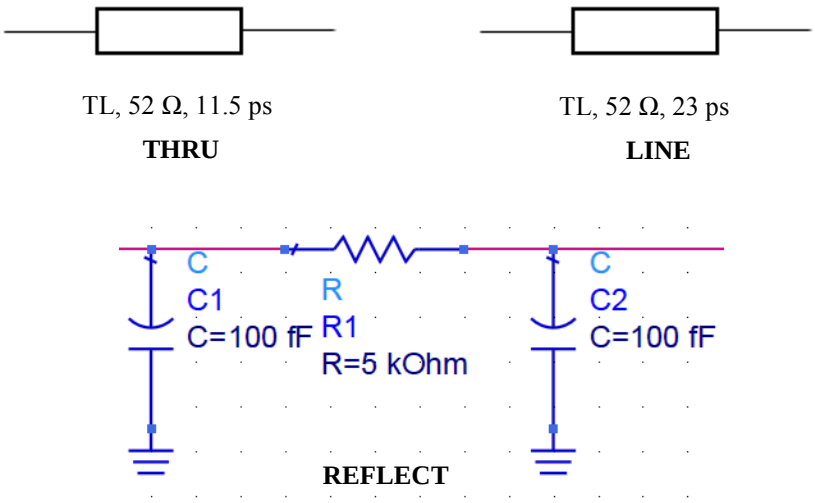



Figure II-14: Simulated standards

The steps of de-embedding that were described in previous section will be used to extract the system of errors again and compare it to the introduced or calculated ones.

- Step 1: calculate the virtual errors A' & B' from three calibrated elements.
- Step 2: calculate AA' & B'B from the measurements of three elements.
- Step 3: extract the error model A & B from previous system of errors (AA', B'B, A' & B').

$$\mathbf{T_A} = \mathbf{T_{AA'}}\,\mathbf{T_{A'}}^{-1} \quad ; \quad \mathbf{T_B} = \mathbf{T_{B'}}^{-1}\,\mathbf{T_{B'B}} \qquad \text{[II-13]}$$

Fig. II-15, compares the introduced S-parameters A (in red) to the simulated ones (in blue).

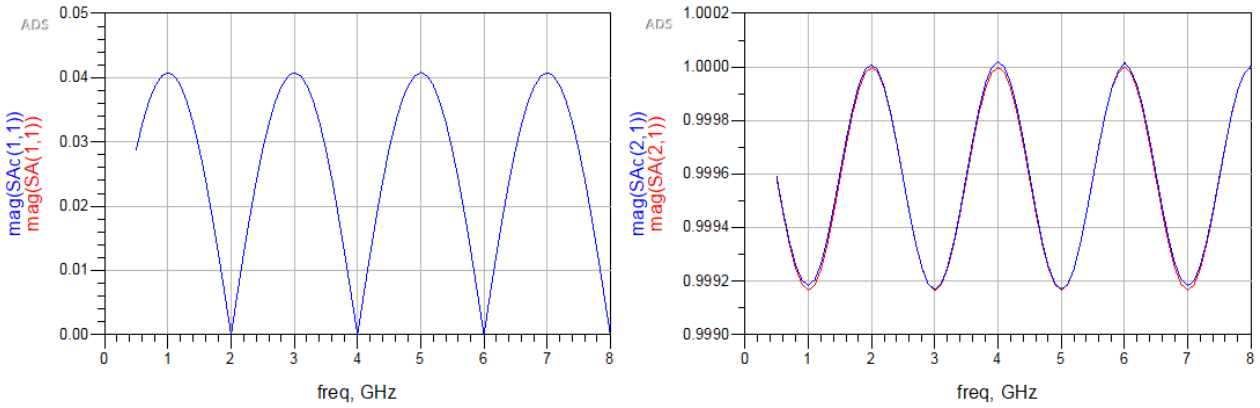



Figure II-15: Simulated vs. Introduced S parameters of input board

Fig. II-16 till II-18 show the simulated vs. introduced for the three calibration standards (Thru, line and Reflect) respectively.

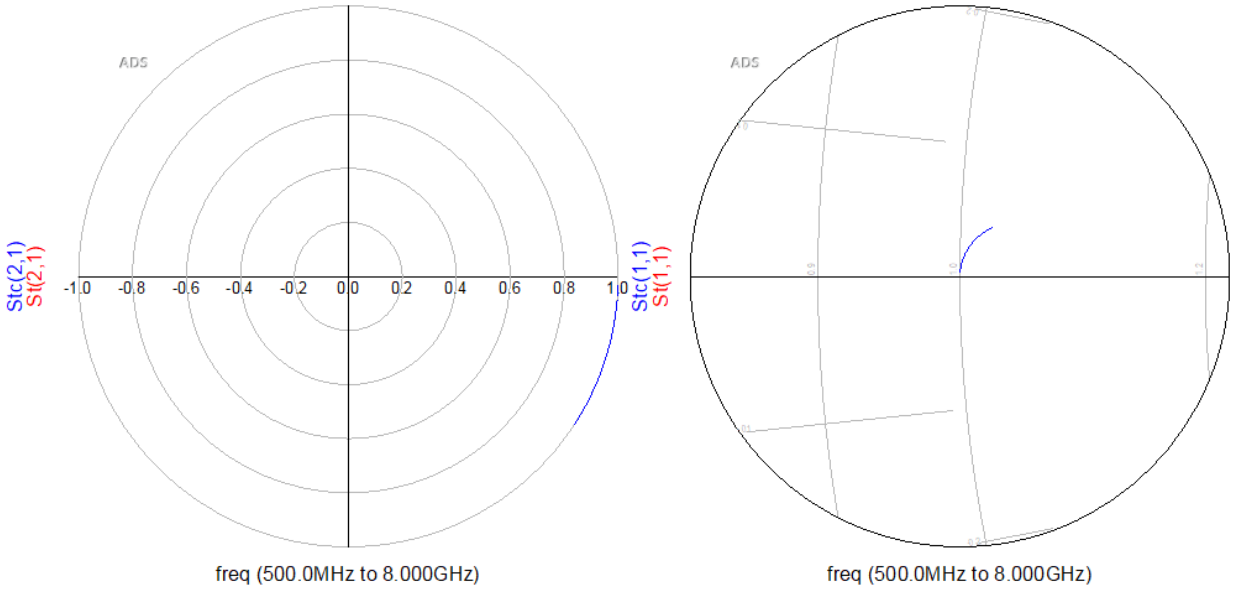



Figure II-16: Simulated vs. Introduced S parameters for Thru standard

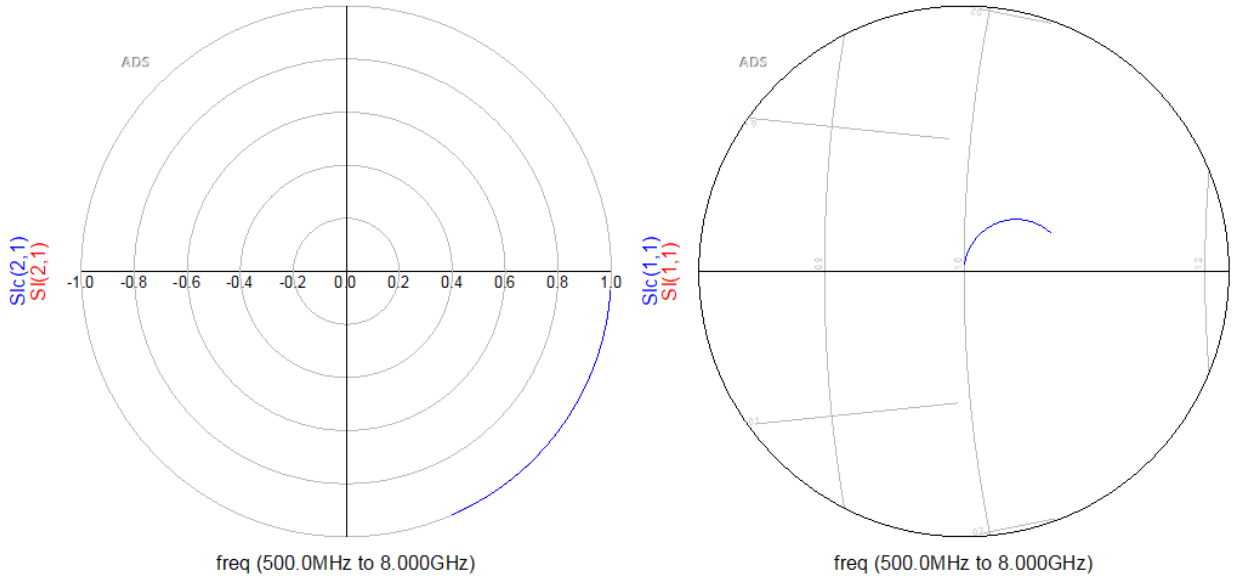



Figure II-17: Simulated vs. Introduced S parameters for Line standard

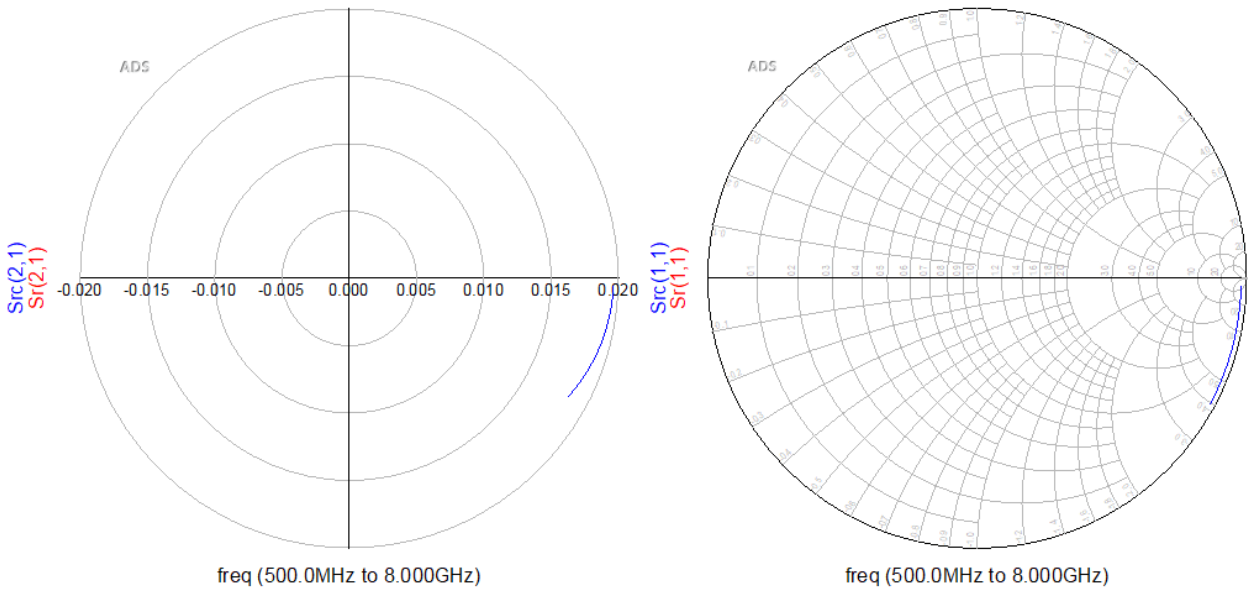



Figure II-18: Simulated vs. Introduced S parameters for Reflect standard

By comparison we find that there is no differences during all over the band of frequency. The other parameters are in a very good agreement as far as the parasitic resonance does not appear for higher frequencies. Their differences are null and this confirms the validity of our analytical calculations for calibration technique and de-embedding method and also it shows that the method is applicable. This study will be applied on different devices as we will see in the following chapter.

## II.6 Conclusion and Perspectives

In this Chapter, we have used a new approach for a TRL calibration technique and de-embedding method. The way that we use the technique show the validity of our approach. All the analytical calculations needed to apply to new approach have been shown.

An overview scheme for a full two-port board setup with the different steps needed to perform the calibration has been described. At the end of this chapter, an example has been studied to show the validation of the proposed study. Simulated vs. Introduced S-parameters for different calibration standards were compared and the results confirm the validity of this technique.

In the next chapters, this study will be applied on different types of devices. First on the following chapter where we are going to test an active MMIC device used for WLAN with different modes. Then on chapter 4 where we will give a further applications to this study where the device that we will investigate is a differential device.

# CHAPTER III

# MEASUREMENT METHODOLOGY AND EXTRACTION RESULTS

## III.1 Introduction

The design of passive circuits that are used in calibration step is a complex and very precise procedure in which many steps have to be carefully taken into account for a successful and efficient implementation in order to be fit within the test socket of a load board. In past years, a great number of substrate integrated circuits have been developed [49]. Our aim is to present a TRL calibration kit for device measurements, and to verify its validity for de-embedding the effect of the SMA connectors, transmission feeding lines, mismatch etc... An additional advantage of this calibration kit is that any designer or researcher can fabricate their own calibration kit with standard machinery for manufacturing planar circuits, so it is much cheaper than any other standard commercial calibration kits, which besides they can correct better the deviations due to the measurement circuit between the network analyzer itself and the SMA connectors [50].

To perform a TRL calibration, three standards have to be manufactured (so called TRL). These standards must help de-embed the errors from the measurements and shift the reference planes down to the pins of DUT. Once the standards have been manufactured, the procedure that has to be followed is that usual in TRL calibration. First, we define the calibration kit on a chip mechanically and electrically compatible with the device to measure. Then we measure the three standards of the calibration kit in their reference planes with a vector network analyzer.

Alternatively, when the on-wafer measurement facilities are not available, the standards may be simulated with a 2.5D or 3D electromagnetic simulator. The device is measured between the outer ports of the board after a coaxial calibration (e.g. an SOLT calibration between SMA ports). The calibration process itself consists of replacing the device by the three standards and calculating the figures useful for our de-embedding method calculation [51].

Chapter III is organized as follows. Paragraph III.2 presents a description about the device that undergoes test. Then, paragraph III.3 shows the design model of the calibration standards using a 3D e.m simulator HFSS and later on the fabricated ones. A fully e-m simulated experiment is proposed in paragraph III.4 and an example of HBT that had been measured. Then in paragraph 5, a measurements for the different calibration standards. Paragraph III.6 shows the measurements validation of a device with LNA and bypass mode. Paragraph III-7 shows the application for power measurements and finally, paragraph III.8 concludes chapter III.

## III.2 Characteristics of a device that undergoes test

The device under test (DUT), is a manufactured product undergoing testing, either at first manufacture or later during its life cycle as part of ongoing functional testing and calibration checks. But during its life time, the DUT is soldered and cannot be included into the board. This can include a test after repair to establish that the product is performing in accordance with the original product specification.

Our device that undergoes test is a fully integrated RF front-end MMIC for WLAN. It includes a Low-Noise Amplifier, a TX Power Amplifier and an integrated power detector covering the entire ISM band. It has RX by-pass mode for high signal handling and low-power TX mode to optimize power efficiency of the PA for low-power levels.

Fig. III-1 below shows a pin configuration of the device to be tested.

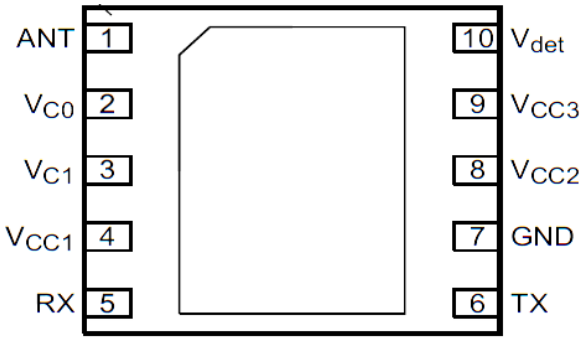



Figure III-1: Pin's configuration of the tested device

| Symbol | Pin | Description |
|---|---|---|
| ANT | 1 | Antenna in/out pin |
| $V_{CO}$ | 2 | $C_0$ control pin |
| $V_{C1}$ | 3 | $C_1$ control pin |
| $V_{CC1}$ | 4 | Supply voltage (LNA) |
| RX | 5 | RX output |
| TX | 6 | TX input |
| GND | 7 | Ground |
| $V_{CC2}$ | 8 | Supply voltage (PA) |
| $V_{CC3}$ | 9 | Supply voltage (PA) |
| $V_{det}$ | 10 | Detection voltage |
| GND | Exposed die pad | Ground |

Table III-1: Pin's description of DUT

Table III-1 shows a pin description of the device under test. It contains 10 pins numbered from one to ten and an exposed die pad for ground centered at the middle of the device. This device of body 2.0 mm x 1.7 mm x 0.35 mm must be introduced inside test socket of a test board as shown in Fig. III-2.

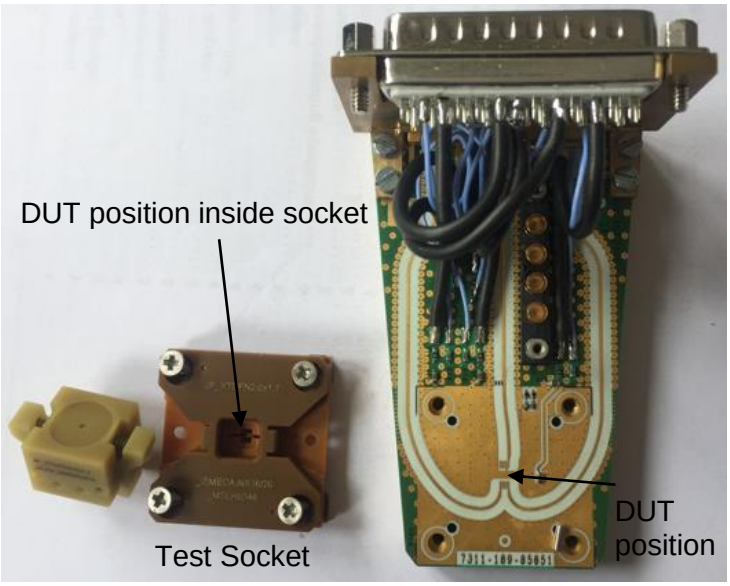



Figure III-2: Schema of the test board

## III.3 Calibration standards: design model and fabrication

### III.3.1 Design model

We have design the layouts of the calibration standards under the same restrictions as the device above and respecting all the tolerances given by the manufacturer. These designs are studied under two situations.

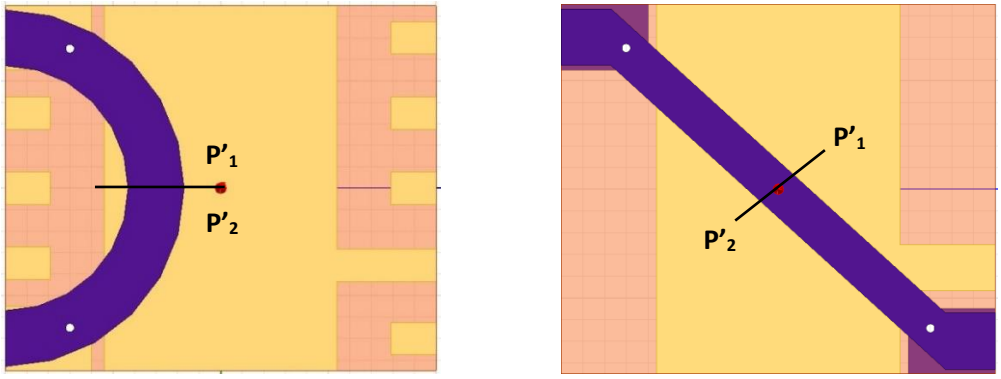
- First situation: three models of calibration standards which correspond to thru, line and reflect are situated between A (antenna) and R (receiver).
- Second situation: Another three models of calibration standards which correspond to thru, line and reflect are situated between T (transmitter) and A (antenna).

The name of each element has been chosen as follows:

- First letter **T** for thru**, L** for line**, R** for reflect.
- Second letter **A** for antenna.

- Third letter **R** for receiver and **T** for transmitter.

Fig. III-3 till III-5, show the layout of different calibration elements.

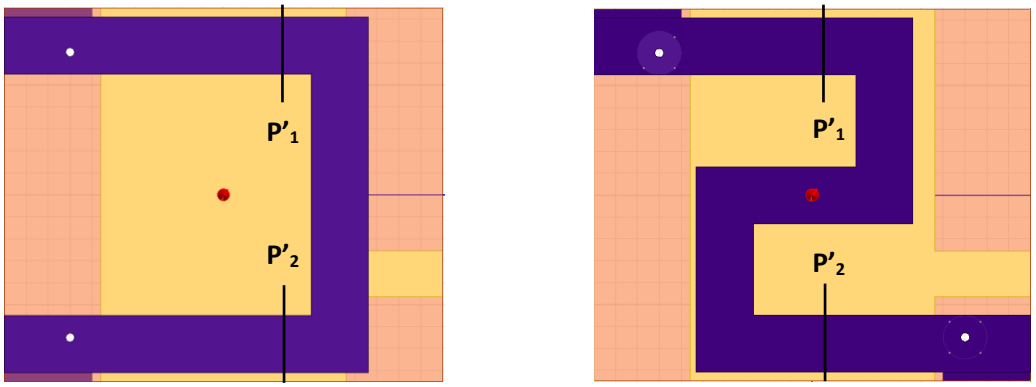



(a) TAR (b) TAT

Figure III-3: Layout of a "Thru" calibration element

When we put the TAR or TAT between $P_1$ and $P_2$, we consider that a thru is placed between $P'_1$ and $P'_2$.

$$\mathbf{S} = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \qquad \text{[III-1]}$$




(c) LAR (d) LAT

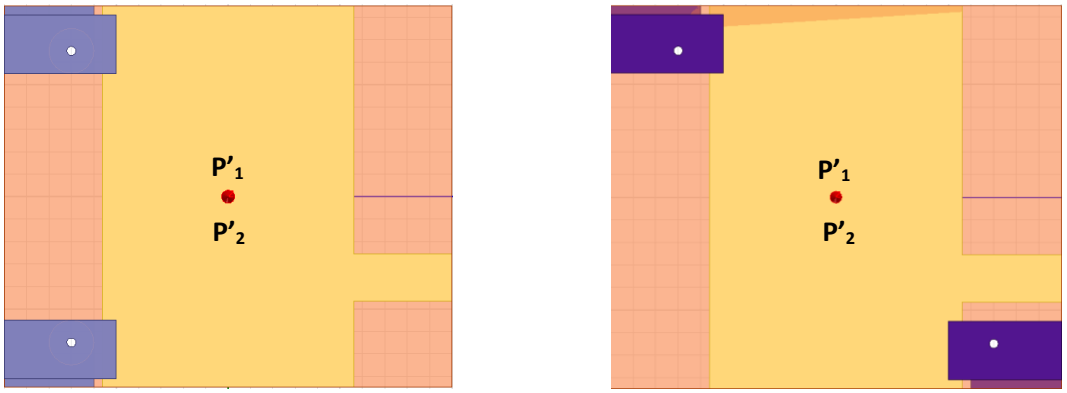
Figure III-4: Layout of a "Line" calibration element

When we put LAT or LAR between $P_1$ and $P_2$, we consider that a line is placed between $P'_1$ and $P'_2$.

$$\mathbf{S} = \begin{pmatrix} 0 & X \\ X & 0 \end{pmatrix} \qquad \text{[III-2]}$$

The zeros for the reflection coefficients mean that the reference impedance between planes $P_1$ and $P_2$ is the characteristic impedance of the line standard.

In our case, the reference impedance is the reference impedance of the GS measurement (i.e. the load for SOLT or the characteristic impedance of the line for TRL). Here, the VNA was calibrated in TRL with an alumina calibration substrate [52]. That means that the reference impedance is 50 Ω.




(e) RAR (d) RAT

Figure III-5: Layout of a "Reflect" calibration element

When we put RAT or RAR between $P_1$ and $P_2$, we consider that reflects are placed in $P'_1$ and $P'_2$.

$$\mathbf{S} = \begin{pmatrix} \Gamma & 0 \\ 0 & \Gamma \end{pmatrix} \qquad \text{[III-3]}$$

The common value for Γ means that the reference planes between $P'_1$ and $P'_2$ is placed in the middle of thru.

These circuits have been optimized using Keysight's HFSS 3D electromagnetic simulator. The shape and place of the ground has been carefully designed in order to allow GS probe measurements.

### III.3.2 Calibration standards under fabrication

Fig. III-6 and III-7, show some photos under microscopic level for the fabricated calibration standards that will be used to perform TRL calibration.

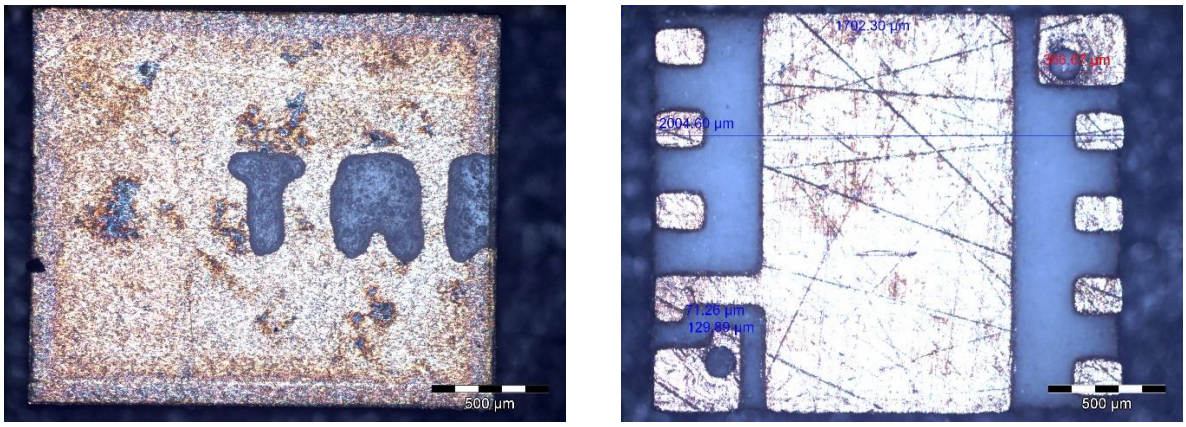



Figure III-6: Top and Bottom view of "TAT" fabricated standard

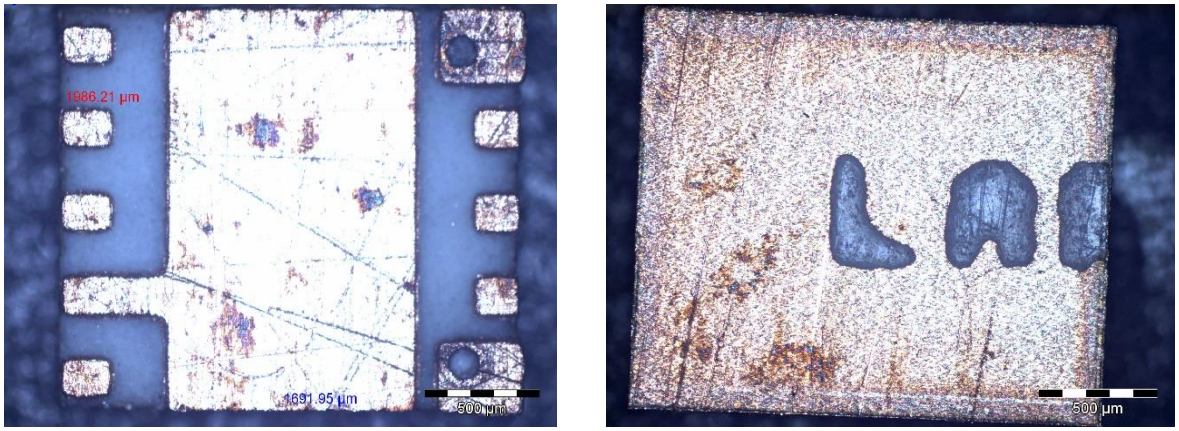



Figure III-7: Top and Bottom view of "LAR" fabricated standard

The design of these standards has been done under some restrictions. One of these is the capability of testing those standards by GS probes and by replacing these standards by DUT under VNA tester. This double function enables us to extract the measurements of circuits alone in order to introduce their results in calibration process. The transmission of signal will be at the upper part of circuits which is shown by different transmission lines and the measurements using GS probes are done at the lower part which contains the signal and ground needed for such test [53].

## III.4 E.M simulation validation

In this part we will use an on-wafer measured HBT transistor as a DUT and we cascade the two half parts of PCB that we have modeled using HFSS as input/output parts. The three design standards Thru, Line and reflect shown before from Fig. III-3 to III-5, will be used to perform the calibration process.

### III.4.1 PCB model

The following figures show a PCB and three standards (Thru, Line and Reflect) which have been modeled and simulated by HFSS 3D electromagnetic software. Using ADS (Advanced Design System) we cascade the two halves of PCB by each standard and later HBT.

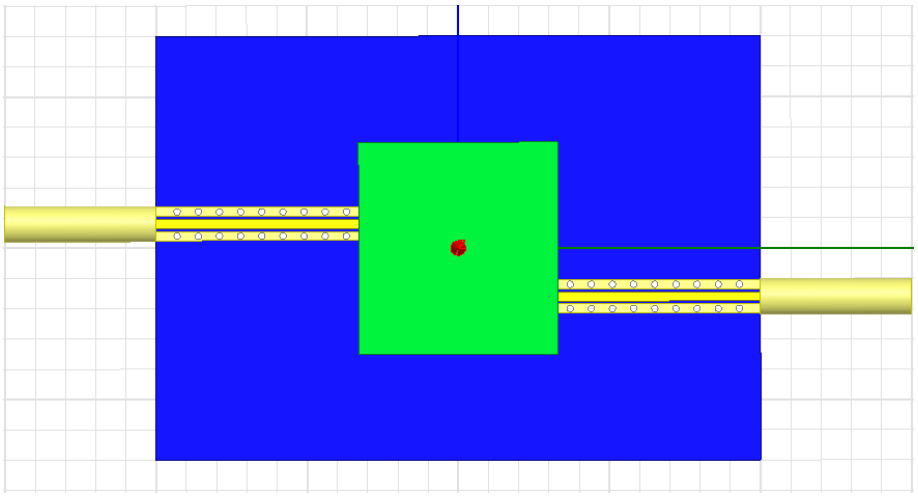


Figure III-8: HFSS PCB model

### III.4.2 Use of E.M simulations for the calibration standards

It is not always possible to have a VNA equipment with a probe station and GS probes. In that case, it is necessary to be confident in electromagnetic simulation to know exactly what is put between planes $P_1$ and $P_2$ during the calibration process. Fig. III-9, compares the results for some standards using E.M simulation and GS probe measurements [54].

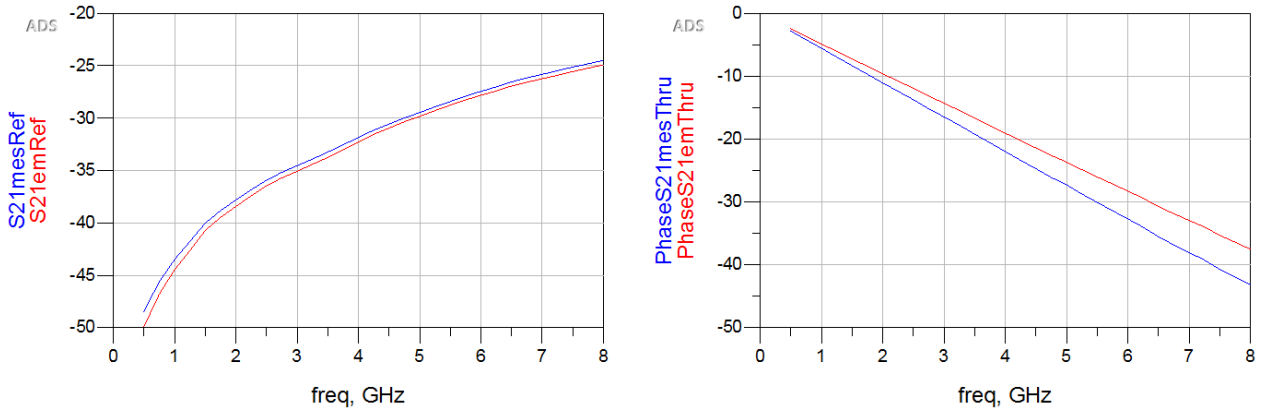



Figure III-9: S parameters of a "Thru" and "Ref" calibration standards

Red curves referred to the electromagnetic simulation results and the blue ones are for the GS probes measurement. The comparison of transmission coefficient $S_{21\ dB}$ for a reference standard doesn't show any difference between the e.m simulated standard using HFSS and under GS probes.

While the slight difference shown in the phase study, is referred mainly to the position of the probes on the circuit, where our GS probes are lied on the tested circuit within two positions: 45 and 180 degrees according to the type of standard under test e.g (TAT, TAR etc...) which explains clearly the difference in phase.

### III.4.3 Simulated measurements with an active two-port device

The simulation measurements are done between the RF coaxial connectors planes which they represent the input and output of the board $P_3$ and $P_4$ respectively.

The DUT (device under test) in our case here is HBT (heterojunction bipolar transistor) where it's placed at the level of pins of the socket $P_1$ and $P_2$.

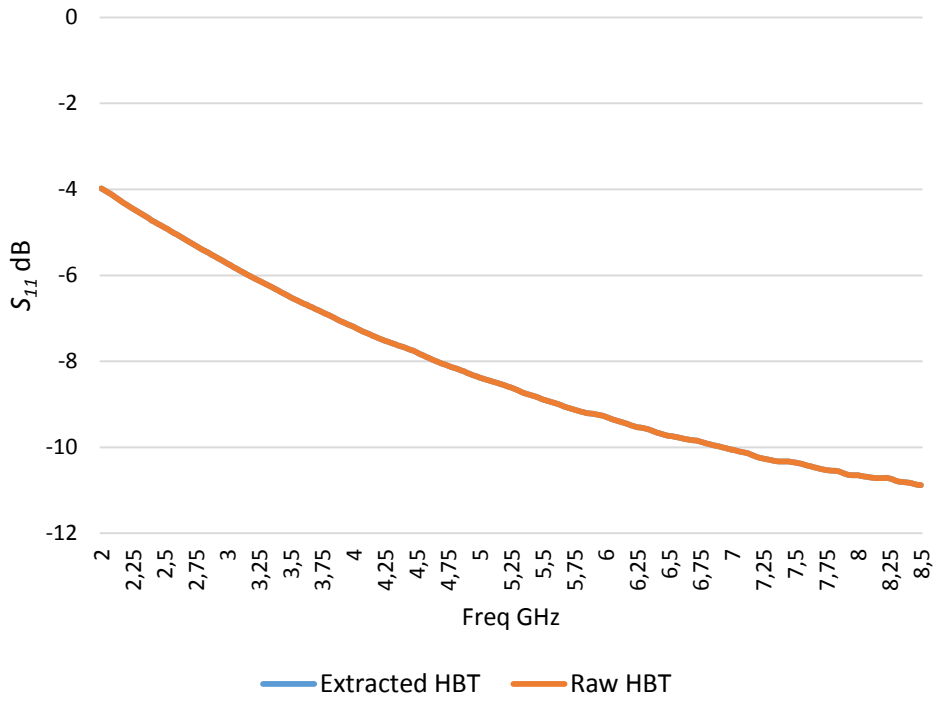



Figure III-10: Measured and calculated $S_{11\ dB}$ of HBT

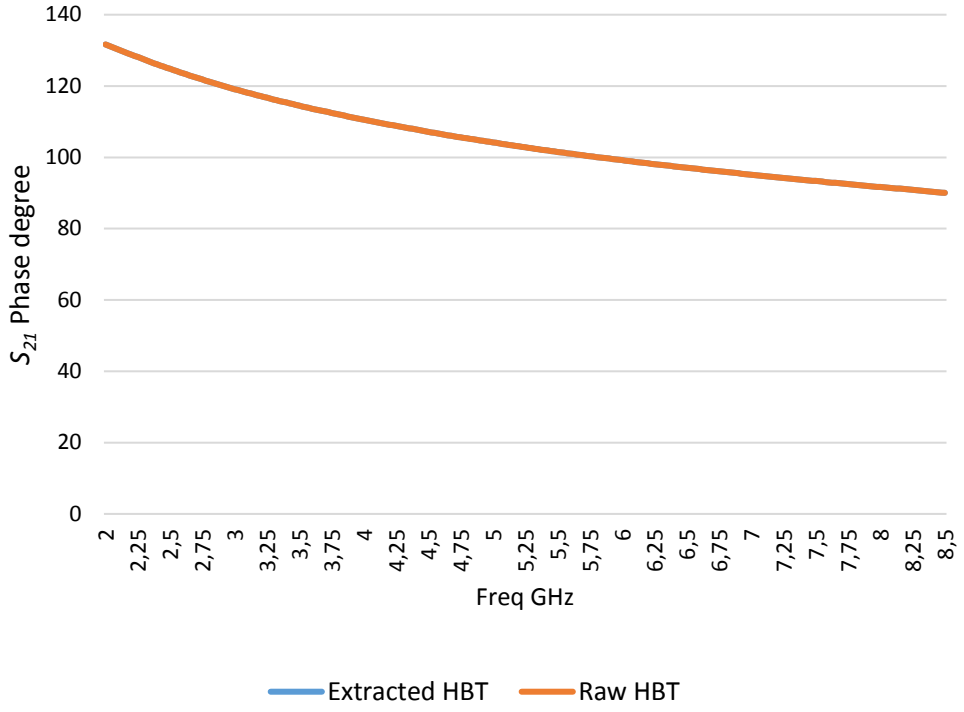



Figure III-11: Measured and calculated phase $S_{21\ degree}$ of HBT

Fig. III-10 and Fig. III-11, show the results of extracted and raw HBT for $S_{11}$ in dB and $S_{21}$ in phase respectively.

The results don't show any difference at the level of transmission and reflection coefficients. The measurements evaluate clearly the validity of our technique and its efficiency.

This technique will be applied on the device that had been described in paragraph III-2.

## III.5 Calibration standards behavior

Different standards were modeled and tested as shown in section III.1. These standards will be measured first by GS probes and later they will be placed respectively inside socket of a test board (Fig. III-2) to be tested by a vector network analyzer between the outer coaxial planes.

### III.5.1 Measuring of standards by GS probes

Fig. III-12, shows some photos for the standards under GS probes measurement. These photos were taken under macro and microscopic levels in order to show clearly the placement of probes at the right locations.

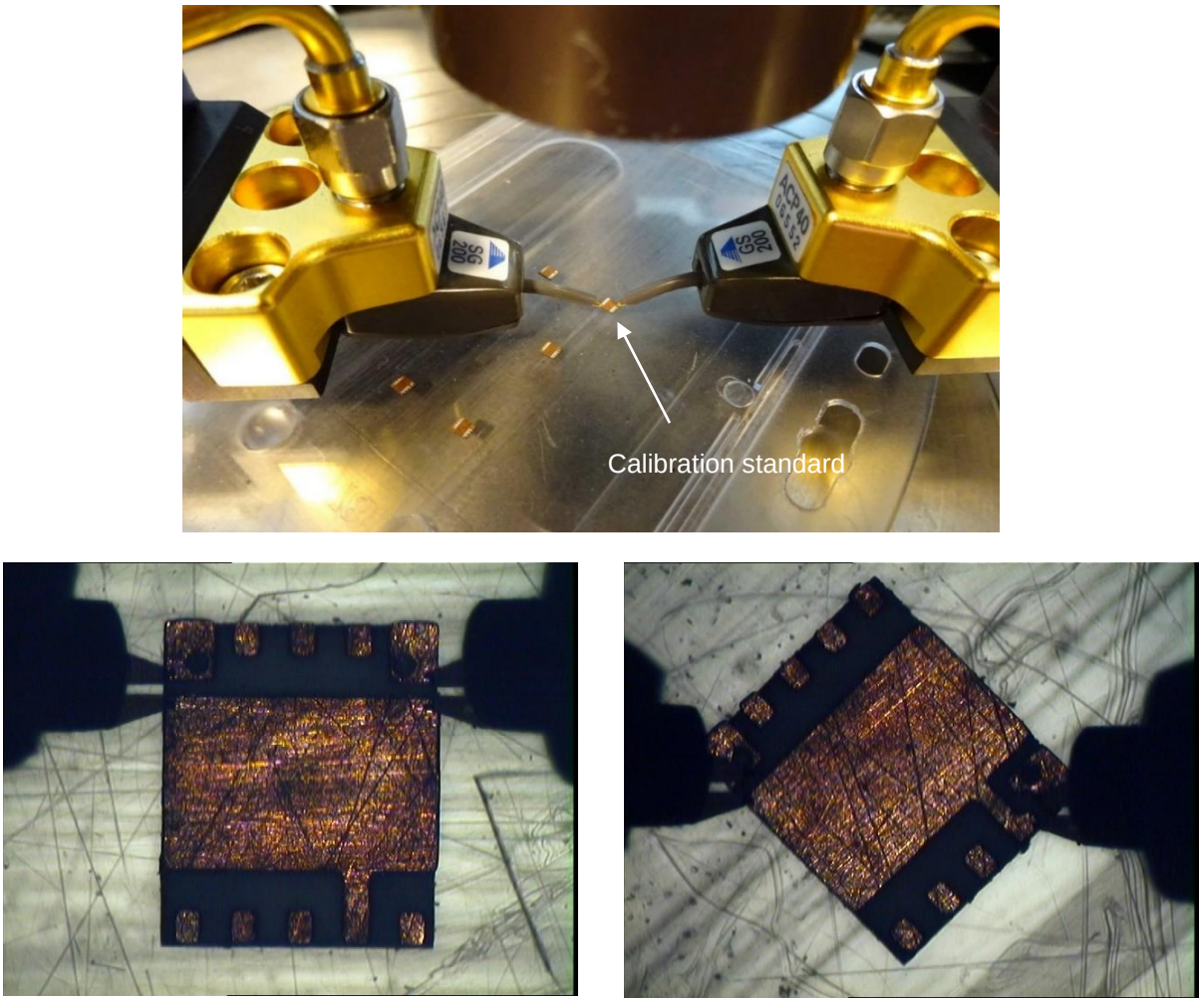



Figure III-12: Standards calibration under GS probes

The standards above are showing the probes in 180˚ & 45˚ face to face. These constraints are essential in order to meet the requirements of calibration of such DUT.

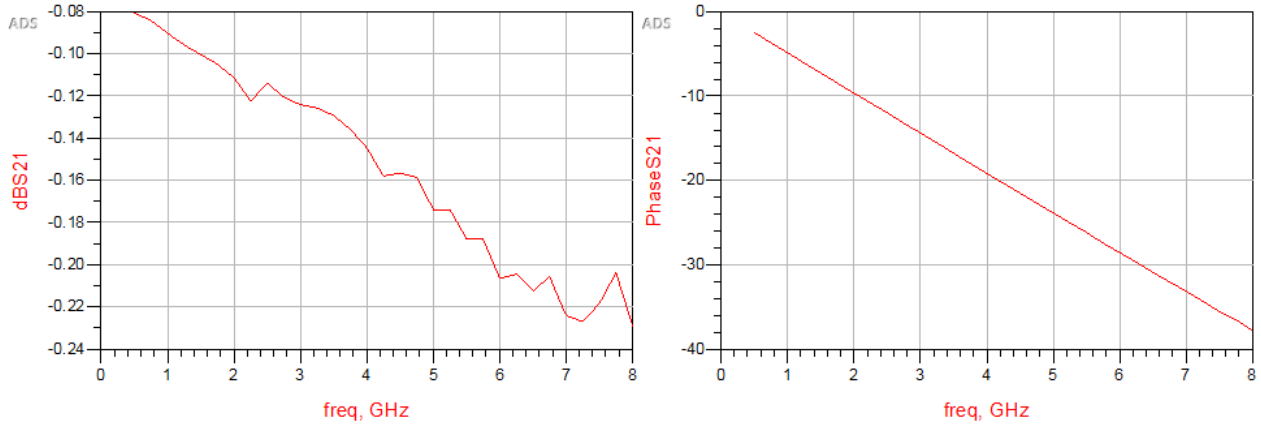



Figure III-13: S parameters of a “Thru” standard

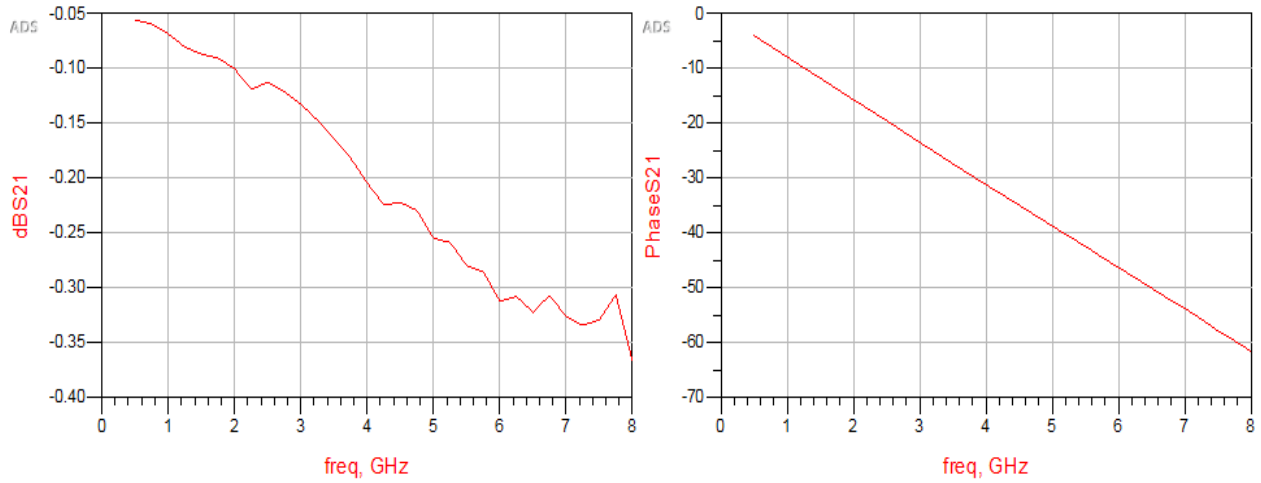



Figure III-14: S parameters of a "Line" standard

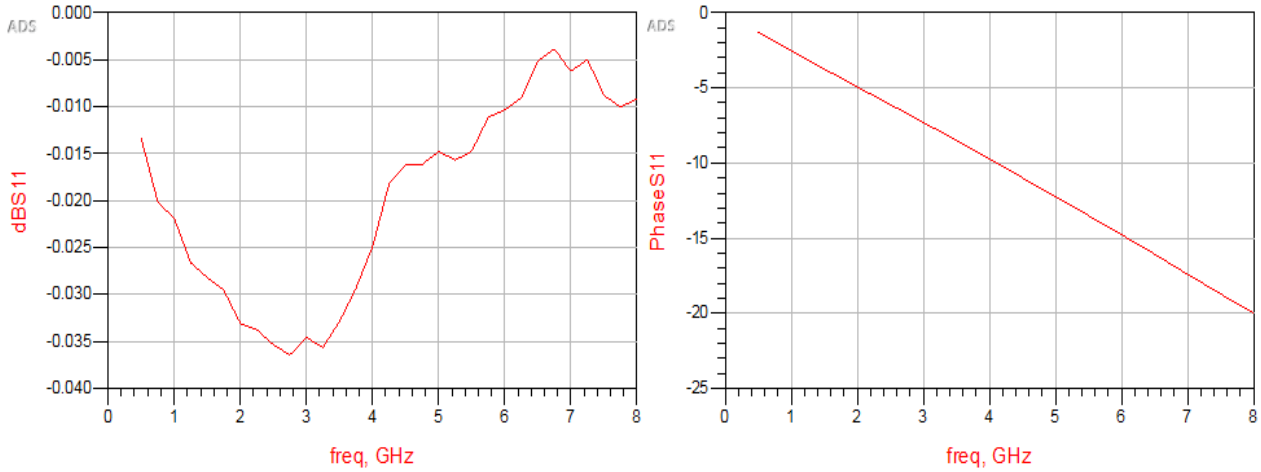



Figure III-15: S parameters of a "Reflect" standard

Fig. III-13 to III-15, show the measurement results of the three fabricated calibration standards: Thru, Line and reflect respectively.

### III.5.2 Verification of the calibration using standards

The calibration standards will be placed respectively inside the socket of the test board which shown in Fig. III-16.

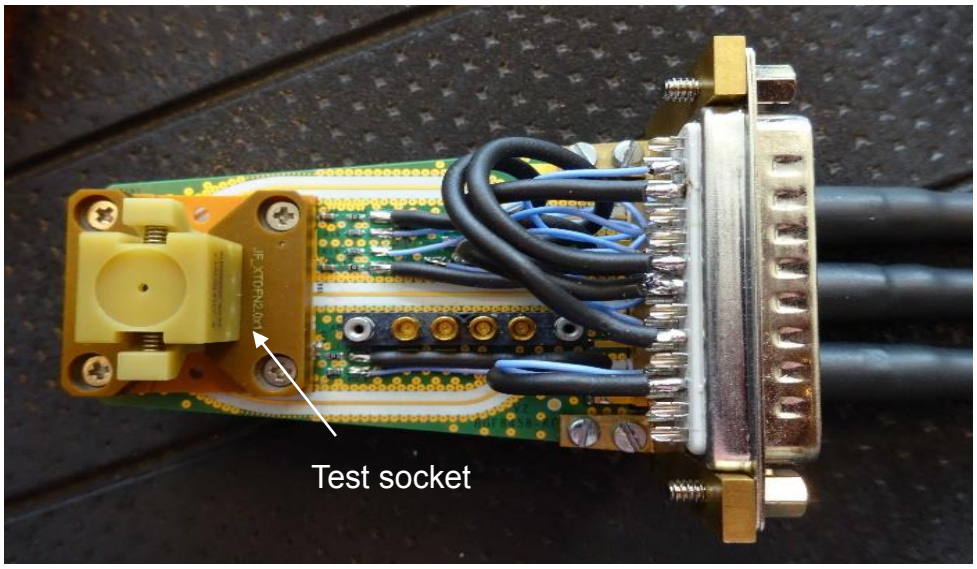



Figure III-16: Test board with a socket

Fig. III-17 and III-18 show the comparison results between under three cases of study:

- Calibration standards under GS probes (blue curves).
- Calibration standards within test board (gray curves).
- Extraction results of the standards after de-embedding (orange curves).

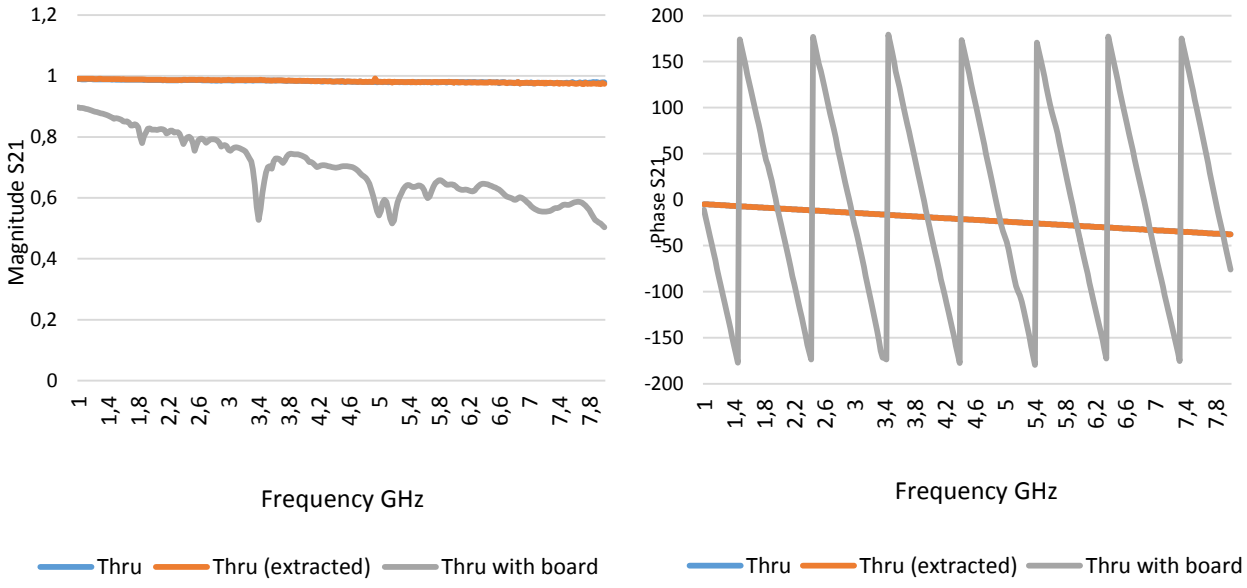



Figure III-17: "Thru" standard behavior in three cases

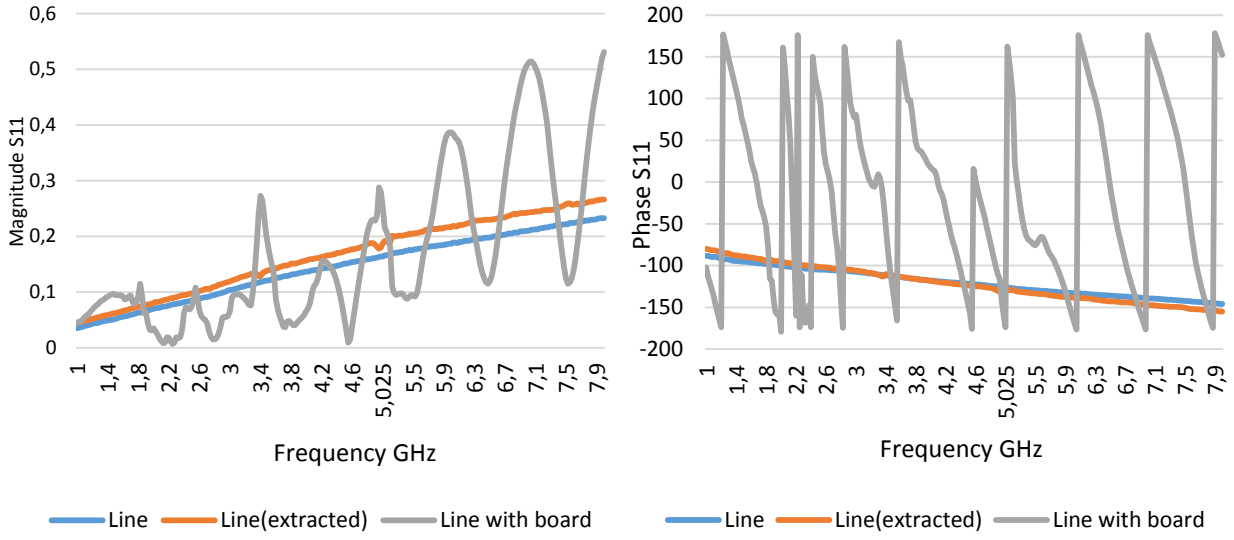



Figure III-18: "line" standard behavior in three cases

By comparing the standards with and without board (Gray and blue respectively), we could see clearly the difference at the level of magnitude and phase. The difference between the magnitudes correspond mainly to the losses which exist in the board. These losses have several origins (mismatch, coupling, resistance etc.). The phase due to the length of the PCB lines is compensated by the calibration. The remaining difference are due to the position of the pins on the chip.

De-embedding described in previous sections aim to reduce these errors or losses at the input and output of DUT after set of measurements which are used for calibration. Standard extracted (thru & Line) which are shown in Fig. III-10 & Fig. III-11, were deducted from the measurement of standards with board after controlled by de-embedding. By comparing those results to the ones with samples under GS probes, we can clarify easily that the importance of this technique is essential for extracting the behavior of samples within complex board. The confirmation of this technique has been proved clearly by comparing samples extracted with samples only (under probes). The difference is null and this confirms the importance of using this technique in extracting error terms in calibration.

## III.6 Measurement: evaluation and validation

The de-embedding method developed in chapter 2 gives the S-parameters of a DUT between $P_1$ and $P_2$ when the actual measurements were made between $P_0$ and $P_3$.

### III.6.1 Board specification

To validate the measurement results and de-embedding technique, we must compare the result with direct measurement between $P_1$ and $P_2$. For this purpose, we have used an evaluation board (EVB) as shown in Fig. III-20, this board contains a TRL calibration kit consisting of two microstrip lines 1A3 and E19 which corresponds to thru and line. The chip has been soldered on the board. That means that it cannot be used for a production test with tens of components every minute (see chapter 1).

The device that we will use in our measurements is the device described in paragraph III-2. This device will be tested and measured within two boards:

Load Board: where the device is laying inside the socket of the test board shown in Fig. III-13.

Evaluation Board: where the device is soldered in an evaluation board (EVB) shown in Fig. III-19.

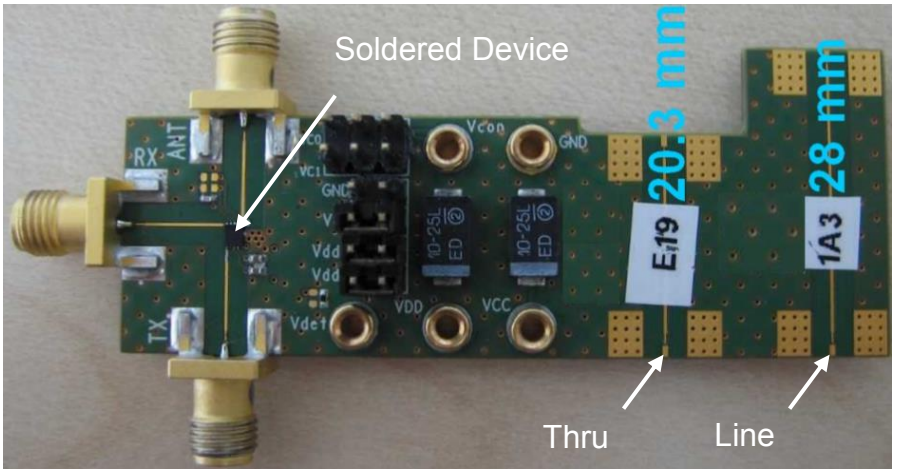



Figure III-19: Evaluation board (EVB)

### III.6.2 Measurements validation

Figures III-20 till III-22 below illustrate the behavior of a device under test in two modes: LNA (Low noise amplifier) and Bypass modes. The measurement study has been done under three cases:

- Blue curves correspond to the DUT in evaluation board.
- Orange curves correspond to the extracted DUT by de-embedding
- Green curves correspond to the DUT in test board

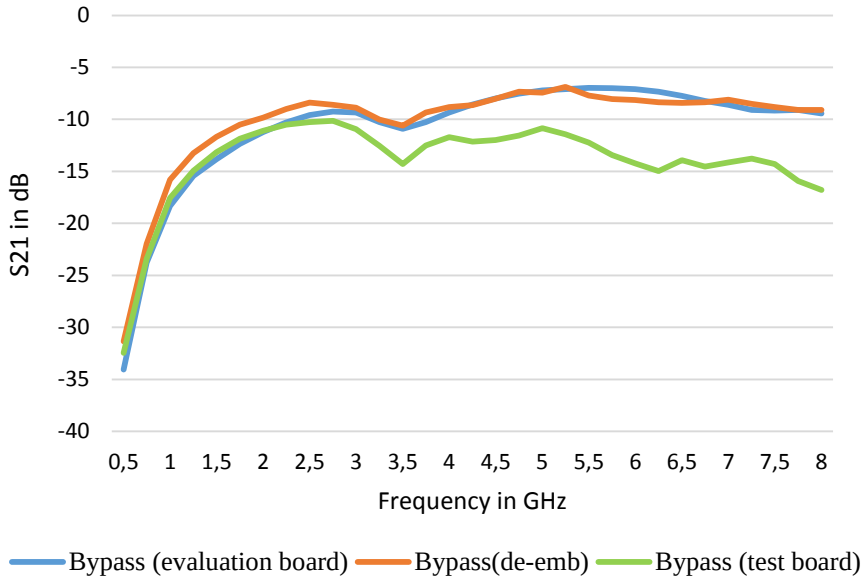



Figure III-20: $S_{21}$ dB for DUT in ByPass mode

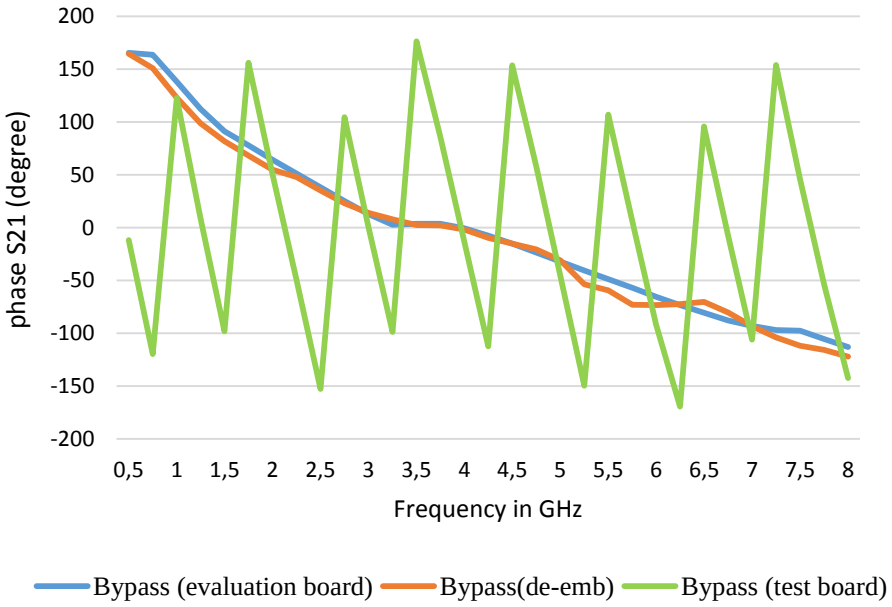



Figure III-21: $S_{21}$ phase for DUT in ByPass mode

The calibration and de-embedding technique described in chapter II is applied on the measurements of the device with a test board in order to remove the errors within the board. The result of this extraction is presented in the figures above under the name de-emb in orange curves.

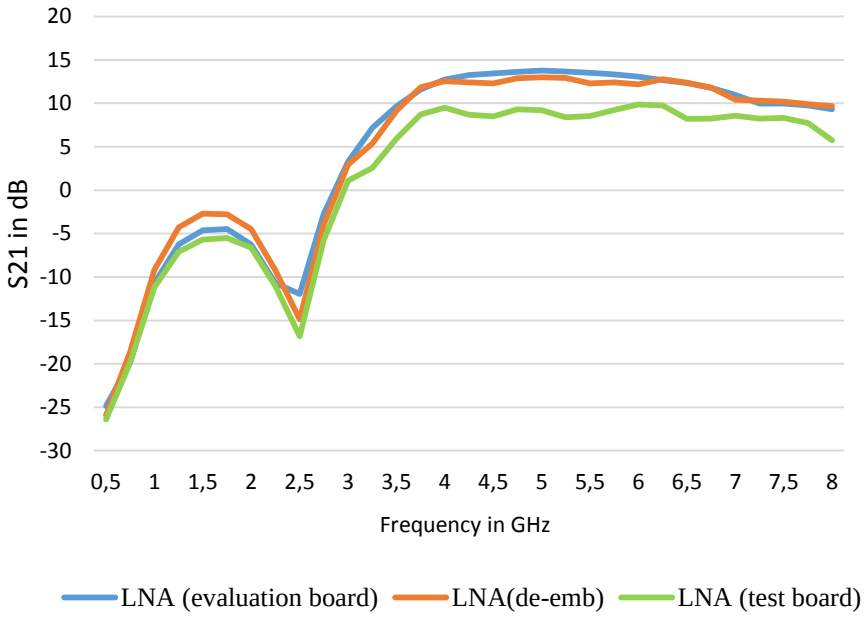



Figure III-22: $S_{21}$ dB for DUT in LNA mode

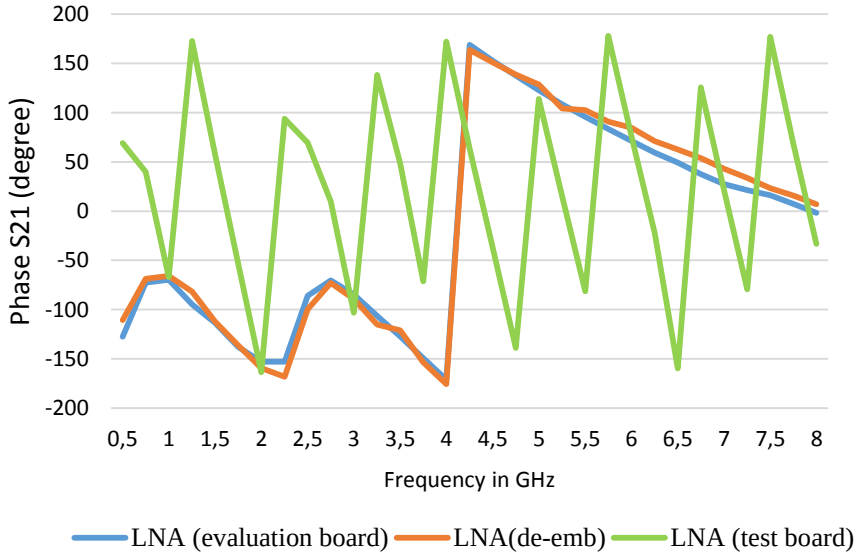



Figure III-23: $S_{21}$ phase for DUT in LNA mode

The comparison between the de-embedded DUT (orange curves) and the measured one in a test board (green curves) shows a clear difference in the transmission level (dB and phase) for the two studied modes. The difference in the two curves corresponds mainly to the losses which are embedded within the test board. These losses have several origins (mismatch, coupling, resistance etc.) and they have been compensated well by calibration and de-embedding.

To confirm the validity of the technique used, a result of measurements of an evaluation board (blue curves) for the same device will be compared with the de-embedded ones (orange curves). By comparison these two curves, we could see clearly that the results are quite the same. This validates that the study that had been done is sufficient for compensating the losses.

We can see on the $S_{21}$ transmission in dB and phase that the correction of the access point, transmission lines and mismatch losses is corrected for all frequencies. Note that this technique is fairly general and makes it possible to correct the losses embedded within a PCB.

### III.6.3 Parasitic coupling effects

Parasitic effects are becoming more critical with increasing requirements on performance, density, complexity, and levels of integration in RFIC designs. For radio frequency (RF) designs, parasitic effects such as IC package pin leakage and substrate coupling are now widely seen [55]. This leads to the need to model the parasitic networks in the areas of chip-package and substrate. The parasitic couplings are the effect of the pins and the leakage in the substrate. The coupling between the pins has been measured by removing the DUT from the board [56].

The measured parameters allow to calculate the admittance matrix $\mathbf{Y_P}$ which represents a pi-circuit describing the parasitic coupling between the pins (Fig. III-24).

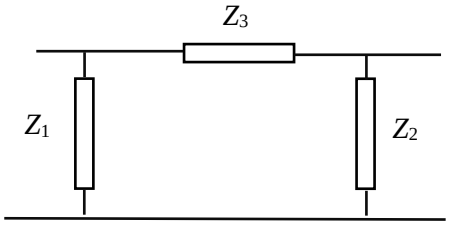



Figure III-24: Pi-circuit model

An RLCG equivalent circuit is derived from Z or Y-parameters. Y-parameters are convenient if we want to model our circuit under test with elements in a pi topology (one component across, and two in shunt). Z-parameters are convenient when we want to model the circuit with a T type of topology (two components in series with a shunt element between them) [57].

Each branch of the $\pi$ or T equivalent topology is represented by an admittance or by an impedance, noted in $Yparameters$ or $Zparameters$ respectively. Each impedance in the pi-circuit can be considered as a resistance in parallel with a capacitance [58].

The value of each is described below:

$$R_1 = \frac{1}{\mathrm{Re}(Y_{11} + Y_{21})} \quad ; \quad R_2 = \frac{1}{\mathrm{Re}(Y_{22} + Y_{21})} \quad ; \quad R_3 = \frac{-1}{\mathrm{Re}(Y_{21})} \qquad \text{[III-4]}$$

$$C_1 = \frac{\mathrm{Im}(Y_{11} + Y_{21})}{\omega} \quad ; \quad C_2 = \frac{\mathrm{Im}(Y_{22} + Y_{21})}{\omega} \quad ; \quad C_3 = \frac{-\mathrm{Im}(Y_{21})}{\omega} \qquad \text{[III-5]}$$

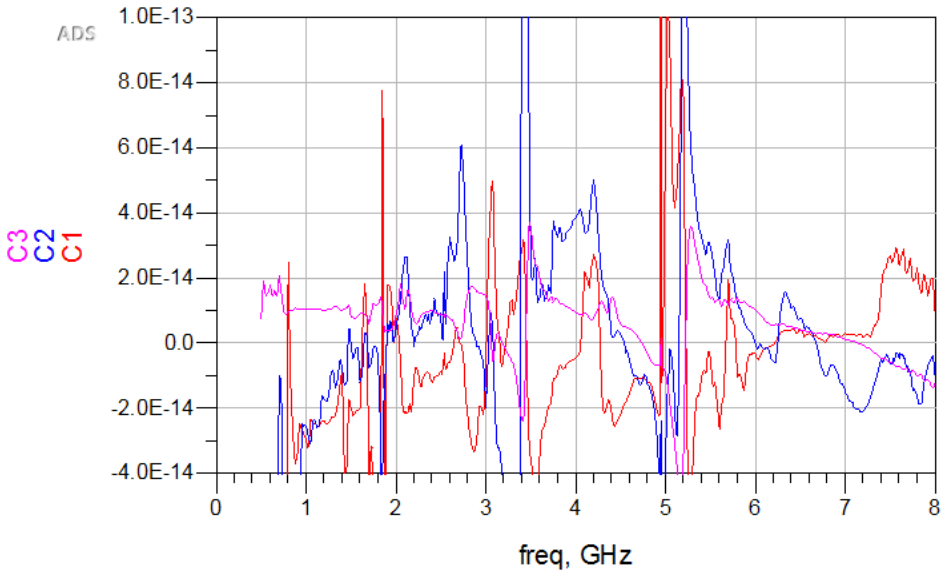



Figure III-25: Capacitance

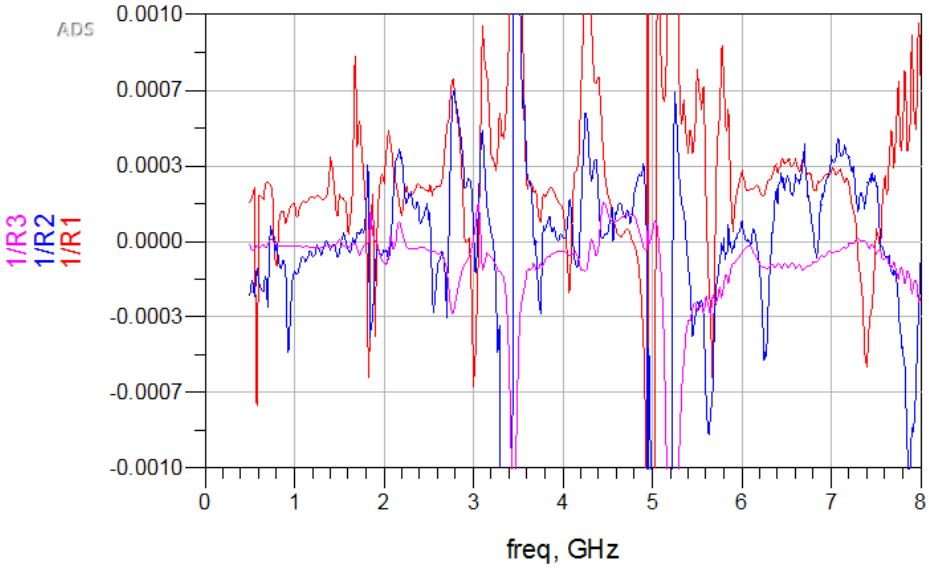



Figure III-26: Conductance

As we could see in Fig. III-25 and III-26, the capacitance and conductance is very small which show that reflect is almost unilateral and also that the coupling between the input and output parts of the board is negligible.

## III.7 Applications to power measurements

The power gain of an electrical network is the ratio of an output power to an input power. Unlike other signal gains, such as voltage and current gain, "power gain" may be ambiguous as the meaning of terms "input power" and "output power" is not always clear. Three important power gains are operating power gain, transducer power gain and available power gain [59].

Note that all these definitions of power gains employ the use of average (as opposed to instantaneous) power quantities and therefore the term "average" is often suppressed, which can be confusing at occasions.

### III.7.1 Available power gain

The available power that the two-port could transfer to the conjugate of its output impedance ($\Gamma_{OUT}$) divided by the available power that the source could transfer to the conjugate of its Thevenin impedance.

It's useful for noise measurement study [60].

$$G_a = \frac{|S_{21}|^2\left(1-|\Gamma_S|^2\right)}{\left(1-|\Gamma_{OUT}|^2\right)|1-S_{11}\Gamma_S|^2} \qquad \text{[III-6]}$$

With:

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1-S_{11}\Gamma_S} \quad \text{and} \quad \Gamma_S = 0 \qquad \text{[III-7]}$$

In Fig. III-27, the available power gain at input and output parts correspond to pink and light blue color respectively.

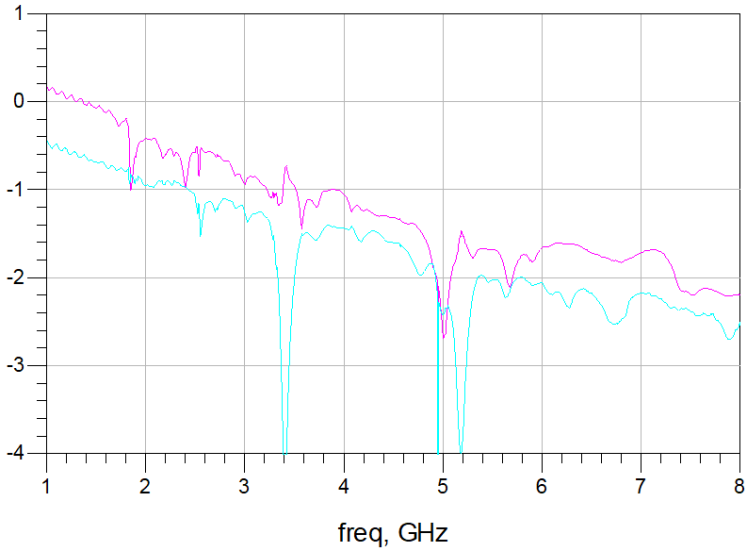



Figure III-27: Available power gain

### III.7.2 Insertion power gain

It's defined as the signal power loss introduced by the RF switch between the input port and the output port in its on-state. It's measured by inserting the DUT between a generator and a load. The numerator of the ratio is the power delivered to the load while the DUT is inserted. The denominator, or reference power, is the power delivered to the load while the source is directly connected.

$$\text{IL (dB)} = -20 \log_{10} |S_{21}| \qquad \text{[III-8]}$$

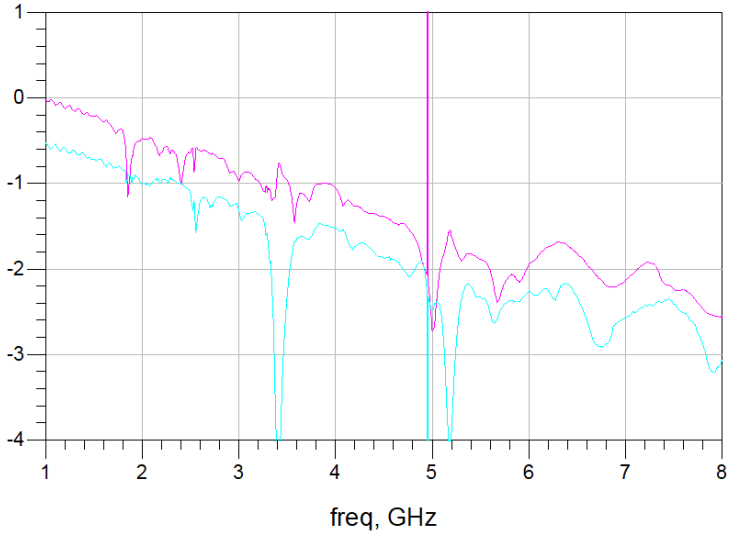



Figure III-28: Insertion power gain

In Fig. III-28, the insertion power gain at input and output parts correspond to pink and light blue color respectively.

### III.7.3 Operating power gain

The power that is transferred from the two-port output to the load $\Gamma_L$ divided by the power that is transferred from the source to the two-port input. It can be written in terms of the two-port s-parameters and the load reflection coefficient.

$$G = \frac{|S_{21}|^2\left(1-|\Gamma_L|^2\right)}{\left(1-|\Gamma_{IN}|^2\right)|1-S_{22}\Gamma_L|^2} \qquad \text{[III-9]}$$

With:

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} \quad \text{and} \quad \Gamma_L = 0 \qquad \text{[III-10]}$$

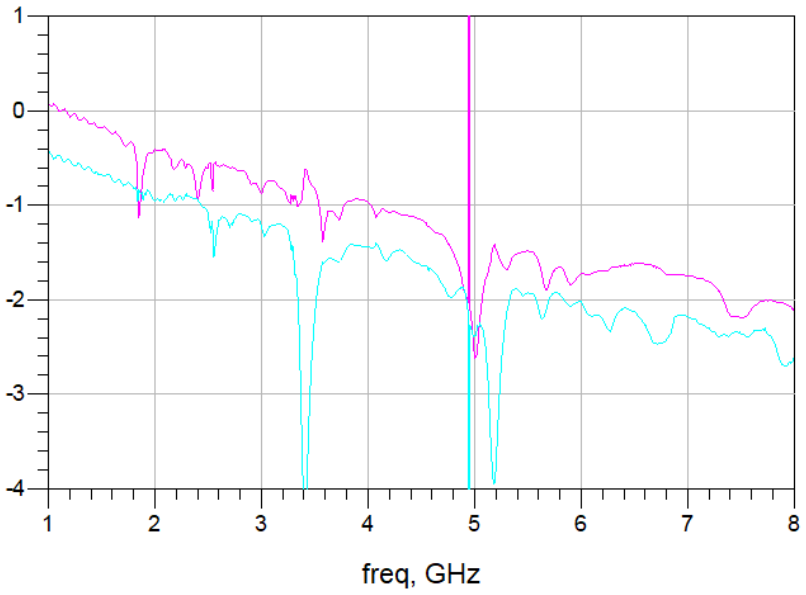



Figure III-29: Operating power gain

In Fig. III-29, the operating power gain at input and output parts correspond to pink and light blue color respectively.

### III.7.4 Transducer gain

The power that is transferred from the two-port output to the load $\Gamma_L$ divided by the available power that the source could transfer to the conjugate of its Thevenin impedance (reflection coefficient $\Gamma_{IN}$).

$$G_T = \frac{|S_{21}|^2 \left(1-|\Gamma_L|^2\right)\left(1-|\Gamma_S|^2\right)}{|1-\Gamma_{IN}\Gamma_S|^2 |1-S_{22}\Gamma_L|^2} \quad \text{[III-11]}$$

With

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} \quad \text{[III-12]}$$

And $\Gamma_S$ =0 and $\Gamma_L$ =0, the result is the same like the insertion gain because we take into consideration that the input and output of DUT are matched.

## III.8 Conclusion and Perspectives

The measurement of S parameters enable characterization in terms of the reflection and transmission of a signal in a printed circuits board (PCB), however, requires calibration and de-embedding techniques that must be put in place in order to correct defects related to the device and measurement cabling.

Our method is fully compatible with on-wafer and a device within a board. It provides directly the S-parameters in the device reference planes. In some cases, where a calibration is not directly possible in the DUT reference planes, the device accesses need to be characterized and modeled. In many applications, components are mounted on a PCB that holds power supply circuits, control circuits and lines for RF or high-speed signals. To measure these components, specific techniques make it possible to correct the effects of connection lines (losses, mismatching, etc.).

The purpose of de-embedding is to calculate the S parameters of a component based on measurements of an overall measurement of the component mounted on PCB with access lines of and on knowledge of the equivalent access line propagation parameters. This requires either a prior measurement of the S parameters of the access lines, or a measurement of the overall access line (without the component).

# CHAPTER IV

# MULTI-PORT TRL CALIBRATION FOR DIFFERENTIAL DEVICES

## IV.1 Introduction

More and more circuits in telecommunication technologies are differential structures. This simplifies the design of RF functions and helps to the parasitic frequencies rejection. Measurement methods developed particularly for these differential circuits will reduce characterization time and increase accuracy. A differential circuit with at least three ports (two inputs and one output) demands multi-port tests. In addition, multi-port measurement is also required to determine mutual coupling between differential interconnections which influences significantly package performance due to the trend of increasing operation frequency, and signal density. Before an RF measurement, a calibration must be done. The algorithm developed in the recent publications such as [61] allows rigorous mixed modes measurement. However their main drawback is so complex and often with many assumptions.

TRL (Thru-Reflect-Line) is one of the most popular methods because it places the reference planes at the input and output of the DUT directly on the wafer. It assumes that the characteristic impedance is clearly defined for each line standard. When the accesses are constituted by coupled lines, the propagation constants and the characteristic impedances of the quasi-TEM $c$ and $\pi$ modes are defined [62]. For symmetric access lines, that means that the propagation constants and the characteristic impedances are related to the odd and even modes, so called mixed modes. When the waveguides are not homogeneous (e.g. micro-strip or coplanar waveguide) these propagation constants and characteristic impedances are different each from the other. Actually, the TRL calibration allow S-parameters measurement [63]. We must keep in mind that S-parameters are defined for propagation modes and not for voltages and currents. This means that the classical 4 port TRL de-embedding is not valid. The mixed mode de-embedding process is more rigorous. When there is no coupling between the access lines or when the mixed modes are quasi-TEM, the propagation constants and the characteristic impedances are equal. In that case, it is possible to consider the natural "modes" for the description of the DUT.

This is organized as follows. Paragraph IV.2 presents the TRL mixed-mode de-embedding method. Paragraph IV.3 describes the transformation matrix calculations for differential input and single output device. In paragraph IV.4, a full study for double TRL calibration process for a differential device and later in paragraph IV.5, the circuit simulation schemes and the extraction results. Finally in paragraph IV.6, a general conclusion and perspectives.

## IV.2 TRL mixed mode de-embedding method

In this paragraph, we describe a mixed mode TRL de-embedding method. The first part reminds the essential notions on natural and mixed modes, and the transformation between them. Then in the second part, the error model is proposed and the calculation of the error terms is detailed [64]. The third part will present the experiment to verify the method with some line structures realized based on glass substrate. The final part will conclude the method.

### IV.2.1 Natural modes

The natural "modes" are defined from voltages and currents. There are not real modes because they do not correspond to eigen solution of the propagation equation [65].

For Port *i*, the power waves $a_i$ and $b_i$ are defined by:

$$a_i = \frac{1}{2}\left(\frac{V_i}{\sqrt{Z_i}} + I_i\sqrt{Z_i}\right) \qquad \text{[IV-1]}$$

$$b_i = \frac{1}{2}\left(\frac{V_i}{\sqrt{Z_i}} - I_i\sqrt{Z_i}\right) \qquad \text{[IV-2]}$$

The corresponding natural *S* and *T* parameters of a four-port structure shown in Figure IV-1 are defined by Eq. (IV-1) and (IV-2).

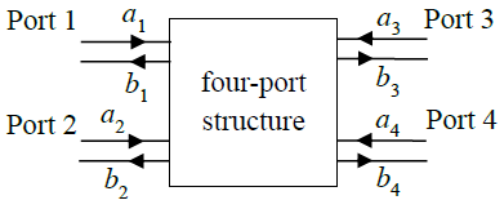



Figure IV-1: four-port structure

S parameters represent the relation between reflected and incident power waves.

$$\begin{pmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{pmatrix} = (\mathbf{Sm}) \begin{pmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{pmatrix} \qquad \text{[IV-3]}$$

T parameters describe the relation between input and output power waves.

$$\begin{pmatrix} b_1 \\ b_2 \\ a_1 \\ a_2 \end{pmatrix} = \mathbf{T} \begin{pmatrix} a_3 \\ a_4 \\ b_3 \\ b_4 \end{pmatrix} \qquad \text{[IV-4]}$$

Where $a_i$, $b_i$ are the incident and reflected power waves for port $i$ ($i$ = 1, 2, 3, 4) respectively [66].

The natural $S$ parameters can be determined from measurement or EM simulation. If we put together 4 measurement results in matrix form, we have:

$$\begin{pmatrix} b_1^{(1)} & b_1^{(2)} & b_1^{(3)} & b_1^{(4)} \\ b_2^{(1)} & b_2^{(2)} & b_2^{(3)} & b_2^{(4)} \\ b_3^{(1)} & b_3^{(2)} & b_3^{(3)} & b_3^{4)} \\ b_4^{(1)} & b_4^{(2)} & b_4^{(3)} & b_4^{(4)} \end{pmatrix} = \mathbf{S_m} \begin{pmatrix} a_1^{(1)} & a_1^{(2)} & a_1^{(3)} & a_1^{(4)} \\ a_2^{(1)} & a_2^{(2)} & a_2^{(3)} & a_2^{(4)} \\ a_3^{(1)} & a_3^{(2)} & a_3^{(3)} & a_3^{4)} \\ a_4^{(1)} & a_4^{(2)} & a_4^{(3)} & a_4^{(4)} \end{pmatrix} \qquad \text{[IV-5]}$$

Where the superscript $^{(i)}$ means the $i^{\text{th}}$ measurement configuration ($i$ = 1, 2, 3, 4) in which the source generates $ai^{(i)}$ ; the others $aj^{(i)}$ ($j \neq i$ and $j$= 1, 2, 3, 4) being very weak.

$$\begin{pmatrix} b_1^{(i)} \\ b_2^{(i)} \\ b_3^{(i)} \\ b_4^{(i)} \end{pmatrix} = \mathbf{S_m} \begin{pmatrix} a_1^{(i)} \\ a_2^{(i)} \\ a_3^{(i)} \\ a_4^{(i)} \end{pmatrix} \qquad \text{[IV-6]}$$

Thus:

$$\mathbf{S_m} = \begin{pmatrix} b_1^{(1)} & b_1^{(2)} & b_1^{(3)} & b_1^{(4)} \\ b_2^{(1)} & b_2^{(2)} & b_2^{(3)} & b_2^{(4)} \\ b_3^{(1)} & b_3^{(2)} & b_3^{(3)} & b_3^{4)} \\ b_4^{(1)} & b_4^{(2)} & b_4^{(3)} & b_4^{(4)} \end{pmatrix} \begin{pmatrix} a_1^{(1)} & a_1^{(2)} & a_1^{(3)} & a_1^{(4)} \\ a_2^{(1)} & a_2^{(2)} & a_2^{(3)} & a_2^{(4)} \\ a_3^{(1)} & a_3^{(2)} & a_3^{(3)} & a_3^{4)} \\ a_4^{(1)} & a_4^{(2)} & a_4^{(3)} & a_4^{(4)} \end{pmatrix}^{-1} \qquad \text{[IV-7]}$$

### IV.2.2 Mixed modes

Let us take a symmetrical tee as an example:

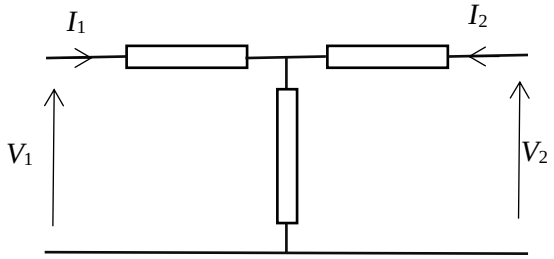



Figure IV-2: Symmetrical tee

- The differential mode is defined as:

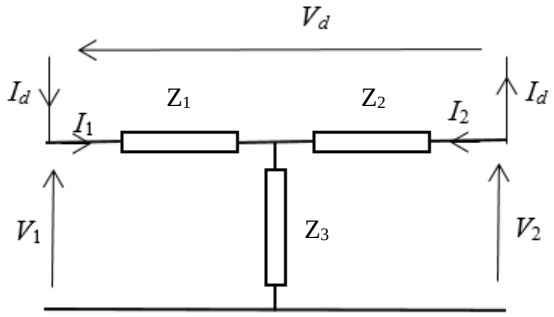



Figure IV-3: Differential mode

$$V_d = V_1 - V_2 \qquad I_d = I_1 = -I_2 \qquad \text{[IV-8]}$$

The input impedance for the differential mode is:

$$Z_d = \frac{V_d}{I_d} = Z_1 + Z_2 = Z_{11} + Z_{22} - 2Z_{12} \qquad \text{[IV-9]}$$

- The common mode is defined as:

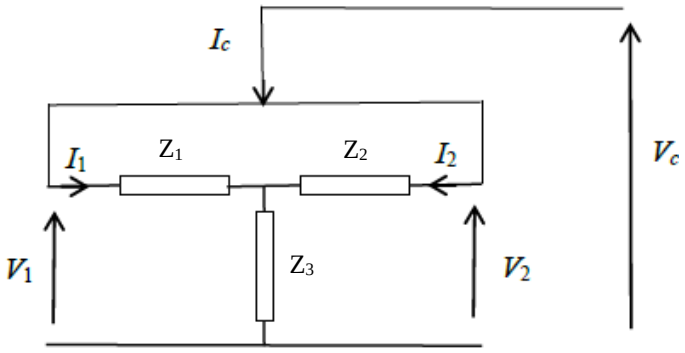



Figure IV-4: Common mode

$$V_c = V_1 = V_2 \qquad I_c = I_1 + I_2 \qquad \text{[IV-10]}$$

The input impedance for the common mode is: $Z_c = \frac{V_c}{I_c} = (Z_1 // Z_2) + Z_3$ [IV-11]

$$Z_c = \frac{(Z_{11} - Z_{12})(Z_{22} - Z_{12})}{Z_{11} + Z_{22} - 2Z_{12}} + Z_{12} \qquad \text{[IV-12]}$$

In general:

$$V_d = V_1 - V_2 \;;\quad I_d = \frac{I_1 - I_2}{2} \;;\quad V_c = \frac{V_1 + V_2}{2} \;;\quad I_c = I_1 + I_2 \qquad \text{[IV-13]}$$

Reciprocally:

$$V_1 = \frac{2V_c + V_d}{2} \;;\; V_2 = \frac{2V_c - V_d}{2} \;;\; I_1 = \frac{I_c + 2I_d}{2} \;;\; I_2 = \frac{I_c - 2I_d}{2} \qquad \text{[IV-14]}$$

### IV.2.3 In terms of power waves

Let us consider symmetrical a propagation structure in a TEM mode. A forward wave can be represented by the voltage and the current in each conductor ($V_1$, $V_2$, $I_1$, $I_2$). If there is no coupling:

$$\frac{V_1}{I_1} = \frac{V_2}{I_2} = Z_0 \qquad \text{[IV-15]}$$

In terms of power waves:

$$V_1 = a_1\sqrt{Z_0} \;;\quad I_1 = \frac{a_1}{\sqrt{Z_0}} \;;\quad V_2 = a_2\sqrt{Z_0} \;;\quad I_2 = \frac{a_2}{\sqrt{Z_0}} \qquad \text{[IV-16]}$$

The travelling power for the differential mode if $Z_0$ is real is:

$$P_d = \frac{1}{2}\mathrm{Re}\left(V_d I_d^*\right) = \frac{1}{2}\mathrm{Re}\left(\frac{(V_1 - V_2)(I_1 - I_2)^*}{2}\right) = \frac{1}{2}\frac{|a_1 - a_2|^2}{2} = \frac{1}{2}|a_d|^2 \qquad \text{[IV-17]}$$

So: $$a_d = \frac{a_1 - a_2}{\sqrt{2}} \qquad \text{[IV-18]}$$

The travelling power for the common mode if $Z_0$ is real is:

$$P_c = \frac{1}{2}\mathrm{Re}\left(V_c I_c^*\right) = \frac{1}{2}\mathrm{Re}\left(\frac{\left(V_1+V_2\right)\left(I_1+I_2\right)^*}{2}\right) = \frac{1}{2}\frac{\left|a_1+a_2\right|^2}{2} = \frac{1}{2}\left|a_c\right|^2 \qquad \text{[IV-19]}$$

So: $$a_c = \frac{a_1+a_2}{\sqrt{2}} \qquad \text{[IV-20]}$$

Reciprocally:

$$a_1 = \frac{a_c+a_d}{\sqrt{2}} \quad ; \quad a_2 = \frac{a_c-a_d}{\sqrt{2}} \qquad \text{[IV-21]}$$

### IV.2.4 Characteristic Impedance for non-coupled lines

- Differential mode:

$$V_d = V_1 - V_2 = \left(a_1-a_2\right)\sqrt{Z_0} = a_d\sqrt{Z_d} \qquad \text{[IV-22]}$$

$$a_d\sqrt{2}\sqrt{Z_0} = a_d\sqrt{Z_d} \qquad \text{[IV-23]}$$

$$Z_d = 2Z_0 \qquad \text{[IV-24]}$$

- Common mode:

$$V_c = \frac{V_1+V_2}{2} = \frac{a_1+a_2}{2}\sqrt{Z_0} = a_c\sqrt{Z_c} \qquad \text{[IV-25]}$$

$$\frac{a_c\sqrt{2}}{2}\sqrt{Z_0} = a_c\sqrt{Z_c} \qquad \text{[IV-26]}$$

$$Z_c = \frac{Z_0}{2} \qquad \text{[IV-27]}$$

### IV.2.5 S-matrix transformation between natural and mixed modes

For natural mode:

$$\begin{pmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{pmatrix} = \left(\mathbf{S_{nat}}\right)\begin{pmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{pmatrix} \quad \text{or :} \quad \frac{1}{\sqrt{2}}\begin{pmatrix} 1 & 0 & 1 & 0 \\ 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & -1 \end{pmatrix}\begin{pmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{pmatrix} = \frac{1}{\sqrt{2}}\left(\mathbf{S_{nat}}\right)\begin{pmatrix} 1 & 0 & 1 & 0 \\ 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & -1 \end{pmatrix}\begin{pmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{pmatrix} \qquad \text{[IV-28]}$$

The transformation matrix is:

$$(\mathbf{S_{mix}}) = \begin{pmatrix} 1 & 0 & 1 & 0 \\ 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & -1 \end{pmatrix}^{-1} (\mathbf{S_{nat}}) \begin{pmatrix} 1 & 0 & 1 & 0 \\ 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & -1 \end{pmatrix} = \frac{1}{2} \begin{pmatrix} 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \\ 1 & -1 & 0 & 1 \\ 0 & 0 & 1 & -1 \end{pmatrix} (\mathbf{S_{nat}}) \begin{pmatrix} 1 & 0 & 1 & 0 \\ 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & -1 \end{pmatrix} \quad \text{[IV-29]}$$

## IV.3 Differential input and single output device

The input part of the board has a single input and a differential output by the use of Balun [67].

### IV.3.1 S-matrix transformation

- Single Input/ Differential Output

$$\begin{pmatrix} b_1 \\ b_2 \\ b_3 \end{pmatrix} = (\mathbf{S_{nat}}) \begin{pmatrix} a_1 \\ a_2 \\ a_3 \end{pmatrix} \text{ or } \begin{pmatrix} 1 & 0 & 0 \\ 0 & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 0 & -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} \begin{pmatrix} b_1 \\ b_d \\ b_c \end{pmatrix} = (\mathbf{S_{nat}}) \begin{pmatrix} 1 & 0 & 0 \\ 0 & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 0 & -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} \begin{pmatrix} a_1 \\ a_d \\ a_c \end{pmatrix} \quad \text{[IV-30]}$$

$$(\mathbf{S_{mix}}) = \begin{pmatrix} 1 & 0 & 0 \\ 0 & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 0 & -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix}^{-1} (\mathbf{S_{nat}}) \begin{pmatrix} 1 & 0 & 0 \\ 0 & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 0 & -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \\ 0 & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} (\mathbf{S_{nat}}) \begin{pmatrix} 1 & 0 & 0 \\ 0 & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 0 & -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} \quad \text{[IV-31]}$$

$$(\mathbf{S_{mix}}) = \begin{pmatrix} S_{11} & \frac{S_{12} - S_{13}}{\sqrt{2}} & \frac{S_{12} + S_{13}}{\sqrt{2}} \\ \frac{S_{21} - S_{31}}{\sqrt{2}} & \frac{S_{22} - S_{32} - S_{23} + S_{33}}{2} & \frac{S_{22} - S_{32} + S_{23} - S_{33}}{2} \\ \frac{S_{21} + S_{31}}{\sqrt{2}} & \frac{S_{22} + S_{32} - S_{23} - S_{33}}{2} & \frac{S_{22} + S_{32} + S_{23} + S_{33}}{2} \end{pmatrix} \quad \text{[IV-32]}$$

❖ Differential Input/ Single Output

$$(\mathbf{S_{mix}}) = \begin{pmatrix} \frac{S_{11}-S_{21}-S_{12}+S_{22}}{2} & \frac{S_{11}-S_{21}+S_{12}-S_{22}}{2} & \frac{S_{13}-S_{23}}{\sqrt{2}} \\ \frac{S_{11}+S_{21}-S_{12}-S_{22}}{2} & \frac{S_{11}+S_{21}+S_{12}+S_{22}}{2} & \frac{S_{13}+S_{23}}{\sqrt{2}} \\ \frac{S_{31}-S_{32}}{2} & \frac{S_{31}+S_{32}}{2} & S_{33} \end{pmatrix} \quad \text{[IV-33]}$$

### IV.3.2 Z-matrix transformation for a single input and differential output

Single input $P_0$. Differential output $P_1$ and $P_2$ or $P_d$ and $P_c$

$$V_1 = \tfrac{1}{2}V_d + V_c\ ;\ V_2 = -\tfrac{1}{2}V_d + V_c\ ; I_1 = I_d + \tfrac{1}{2}I_c\ ;\ I_2 = -I_d + \tfrac{1}{2}I_c \quad \text{[IV-34]}$$

$$\begin{pmatrix} 1 & 0 & 0 \\ 0 & \frac{1}{2} & 1 \\ 0 & -\frac{1}{2} & 1 \end{pmatrix} \begin{pmatrix} V_0 \\ V_d \\ V_c \end{pmatrix} = (\mathbf{Z_{nat}}) \begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & \frac{1}{2} \\ 0 & -1 & \frac{1}{2} \end{pmatrix} \begin{pmatrix} I_0 \\ I_d \\ I_c \end{pmatrix} \quad \text{[IV-35]}$$

$$(\mathbf{Z_{mix}}) = \begin{pmatrix} 1 & 0 & 0 \\ 0 & \frac{1}{2} & 1 \\ 0 & -\frac{1}{2} & 1 \end{pmatrix}^{-1} (\mathbf{Z_{nat}}) \begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & \frac{1}{2} \\ 0 & -1 & \frac{1}{2} \end{pmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & -1 \\ 0 & \frac{1}{2} & \frac{1}{2} \end{pmatrix} (\mathbf{Z_{nat}}) \begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & \frac{1}{2} \\ 0 & -1 & \frac{1}{2} \end{pmatrix} \quad \text{[IV-36]}$$

$$(\mathbf{Z_{mix}}) = \begin{pmatrix} Z_{00} & Z_{01}-Z_{02} & \frac{Z_{01}+Z_{02}}{2} \\ Z_{10}-Z_{20} & Z_{11}-Z_{21}-Z_{12}+Z_{22} & \frac{Z_{11}-Z_{21}+Z_{12}-Z_{22}}{2} \\ \frac{Z_{10}+Z_{20}}{2} & \frac{Z_{11}+Z_{21}-Z_{12}-Z_{22}}{2} & \frac{Z_{11}+Z_{21}+Z_{12}+Z_{22}}{4} \end{pmatrix} \quad \text{[IV-37]}$$

The normalized matrix with regard to $Z_0$ for Port 1, $Z_d$ for differential and $Z_c$ for common is

$$(\mathbf{z_{mix}}) = \begin{pmatrix} \frac{Z_{00}}{Z_0} & \frac{Z_{01}-Z_{02}}{\sqrt{Z_0 Z_d}} & \frac{Z_{01}+Z_{02}}{2\sqrt{Z_0 Z_c}} \\ \frac{Z_{10}-Z_{20}}{\sqrt{Z_0 Z_d}} & \frac{Z_{11}-Z_{21}-Z_{12}+Z_{22}}{Z_d} & \frac{Z_{11}-Z_{21}+Z_{12}-Z_{22}}{2\sqrt{Z_d Z_c}} \\ \frac{Z_{10}+Z_{20}}{2\sqrt{Z_0 Z_c}} & \frac{Z_{11}+Z_{21}-Z_{12}-Z_{22}}{2\sqrt{Z_d Z_c}} & \frac{Z_{11}+Z_{21}+Z_{12}+Z_{22}}{4Z_c} \end{pmatrix} \quad \text{[IV-39]}$$

With non-coupled lines:

$$Z_d = 2Z_0 \quad \text{and} \quad Z_c = \frac{1}{2}Z_0 \quad \text{[IV-38]}$$

## IV.4 TRL calibration process

### IV.4.1 First TRL between $P_1$ and $P_3$ using Thru1, Line1 and Reflect

Accesses 0 and 4 are the accesses we have performed a calibration. It could be an SOLT calibration between coaxial connectors. For the e-m simulation, it is the plane where the S-parameters are calculated, e.g. the end of the CPW on the board. [68]

The input three-port consists of the CPW on the board, the balun and the pins. The output two-port consists of the CPW on the board and the pins.

The first TRL calibration applies to the figure above. The thru is THRU1. This means that the reference plane is situated in the middle of the thru. The line is LINE 1. The REFLECT consists of leaving pins of access 1 open. That means that a reflection coefficient Γ is presented at access 1. Γ is a line ended by the capacitance of the pins.

The length of the line is the distance between the pins and the reference plane. It must be the reflection coefficient that is presented to access 2. The three-port with its access 2 terminated by Γ is considered as the input two-port by the TRL process. Where the standards were measured under 50 ohm GS probes.

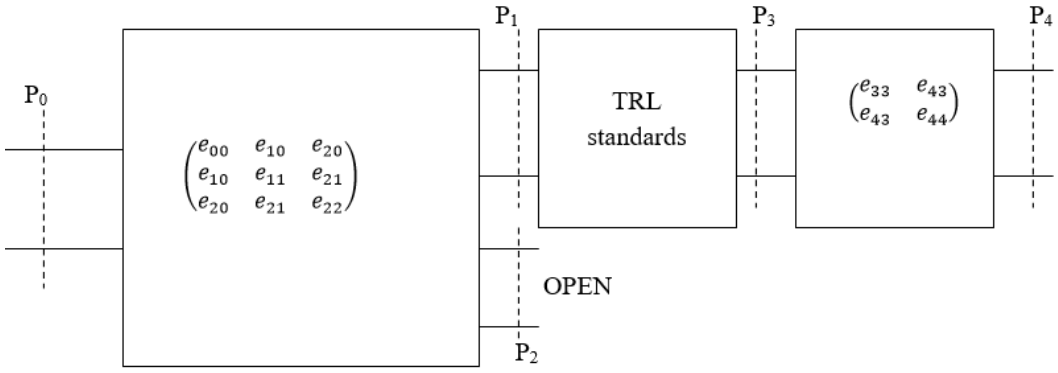



Figure IV-5: First step of TRL process

The TRL calculation gives:

For A: $$\begin{pmatrix} e_{00}^{(1)} & e_{10}^{(1)} \\ e_{10}^{(1)} & e_{11}^{(1)} \end{pmatrix}$$ [IV-40]

For B: $$\begin{pmatrix} e_{33} & e_{43} \\ e_{43} & e_{44} \end{pmatrix}$$ [IV-41]

They can be transformed into de-normalized Z-matrices.

As Port 2 is open, we obtain the corresponding Z-parameters de-normalized of the input three-port:

$$\begin{pmatrix} Z_{00} & Z_{10} \\ Z_{10} & Z_{11} \end{pmatrix}$$ [IV-42]

### IV.4.2 Second TRL between $P_2$ and $P_3$ using Thru2, Line2 and Reflect

The second TRL calibration is based upon the same idea.

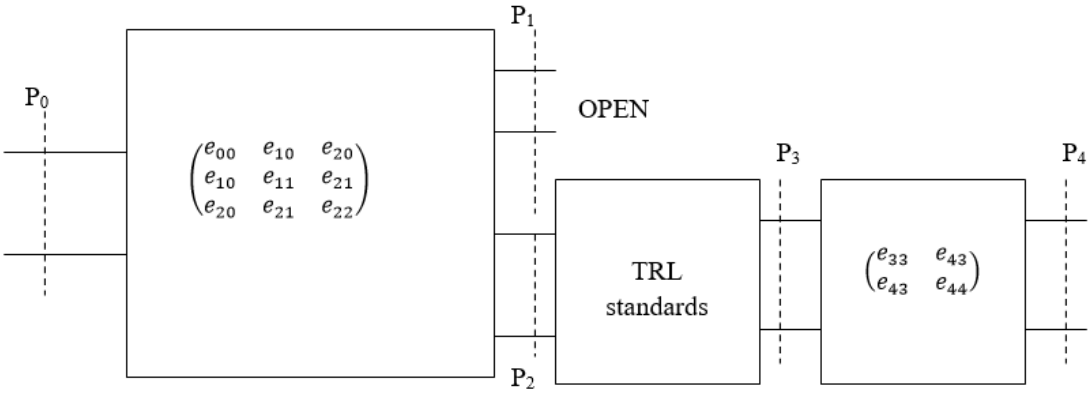



Figure IV-6: Second step of TRL process

The TRL calculation gives:

For A: $$\begin{pmatrix} e_{00}^{(2)} & e_{20}^{(2)} \\ e_{20}^{(2)} & e_{22}^{(2)} \end{pmatrix}$$ [IV-43]

For B: $$\begin{pmatrix} e_{33} & e_{43} \\ e_{43} & e_{44} \end{pmatrix}$$ [IV-44]

They can be transformed into de-normalized Z-matrices.

As Port 1 is open, we obtain the corresponding Z-parameters de-normalized of the input three-port:

$$\begin{pmatrix} Z_{00} & Z_{20} \\ Z_{20} & Z_{22} \end{pmatrix}$$ [IV-45]

Only $Z_{21}$ is missing:

$$(\mathbf{Z_A}) = \begin{pmatrix} Z_{00} & Z_{10} & Z_{20} \\ Z_{10} & Z_{11} & ? \\ Z_{20} & ? & Z_{22} \end{pmatrix}$$ [IV-46]

### IV.4.3 Determination of $Z_{21}$

It is not possible to reach $Z_{21}$ with the two TRL operations. So, we need another one. We propose to connect Ports 1 and 2 and measure the impedance at Port 0.

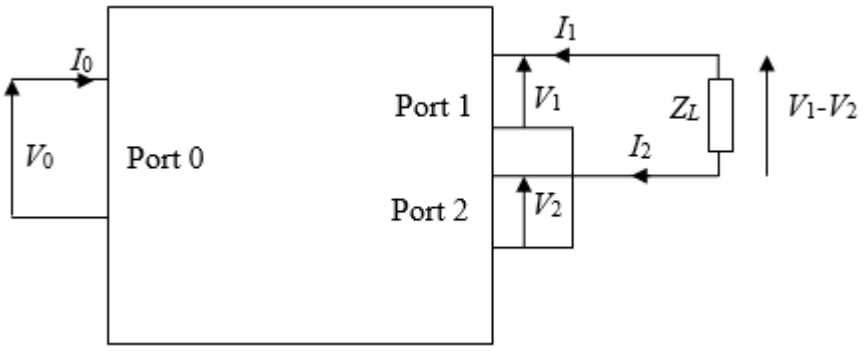



Figure IV-7: Third step of TRL process

The matrix development for a reciprocal three-port is

$$\begin{cases} V_0 = Z_{00}I_0 + Z_{10}I_1 + Z_{20}I_2 \\ V_1 = Z_{10}I_0 + Z_{11}I_1 + Z_{21}I_2 \\ V_2 = Z_{20}I_0 + Z_{21}I_1 + Z_{22}I_2 \end{cases} \quad \text{[IV-47]}$$

The conditions of the circuit are:

$$I_1 = -I_2 \quad ; \quad V_1 - V_2 = \Gamma_L I_2 \quad \text{[IV-48]}$$

From the last two lines of the matrix:

$$I_2 = \frac{Z_{10} - Z_{20}}{Z_{11} - 2Z_{21} - Z_{22} - Z_L} I_0 \quad \text{[IV-49]}$$

$$I_1 = \frac{Z_{20} - Z_{10}}{Z_{11} - 2Z_{21} - Z_{22} - Z_L} I_0 \quad \text{[IV-50]}$$

Reporting into the first line:

$$Z_{IN} = \frac{V_0}{I_0} = Z_{00} - \frac{(Z_{20} - Z_{10})^2}{Z_{11} - 2Z_{21} - Z_{22} - Z_L} \quad \text{[IV-51]}$$

With:

$$Z_{IN} = Z_0 \frac{1 + S_{00}}{1 - S_{00}} \quad \text{[IV-52]}$$

$S_{00}$ is the reflection coefficient measured at the input of the three-port A.

$$Z_{21} = \frac{Z_{11} - Z_{22} - Z_L}{2} - \frac{(Z_{20} - Z_{10})^2}{2(Z_{00} - Z_{IN})} \quad \text{[IV-53]}$$

For the simulation, we can describe the connection between Port 1 and Port 2 by a resistance in series with an inductance.

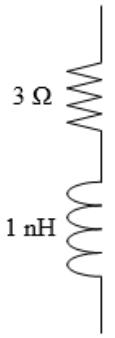



Figure IV-8: Ports behavior

## IV.5 Circuit simulation using ADS

For the simulated calibration, we can use the following ideal balun. The frequency for the phase shift is the central frequency of the operating bandwidth and the differential impedance is equal to 50Ω [69].

### IV.5.1 Input/Output parts of PCB

Fig. IV-9 and IV-10, show the input and output parts of PCB respectively. The input A with a single input and differential output is a three-port network consists of the CPW on the board, the balun and the pins. The output B with a single input and output is a two-port network consists of the CPW on the board and the pins.

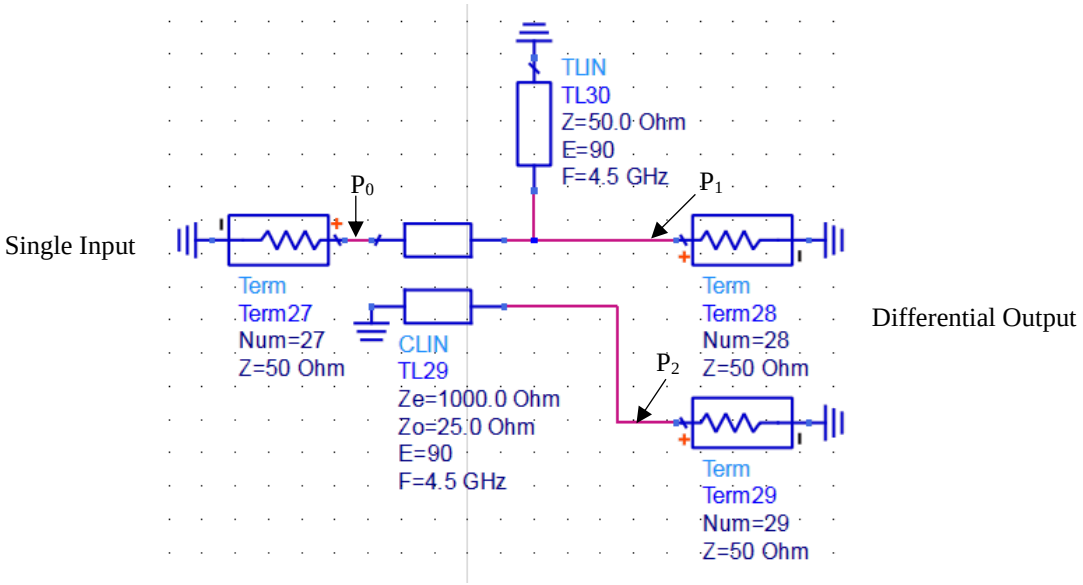



Figure IV-9: Input part A of the PCB

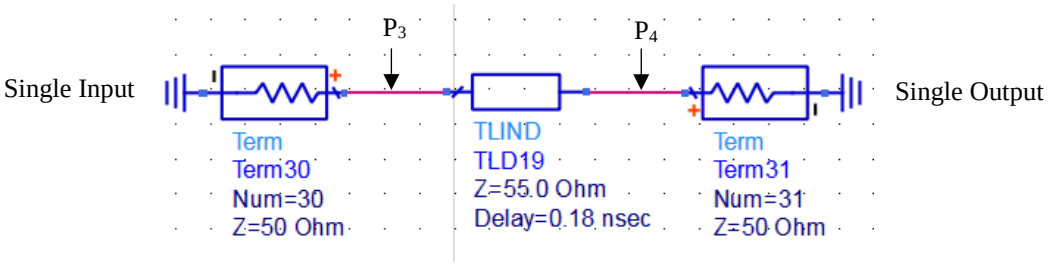



Figure IV-10: Output part B of the PCB

Fig. IV-11 and IV-12, correspond to the initial simulated parameters of the input A ($S_{inA}$ in red) and to the output part B ($S_{inB}$ in blue) respectively.

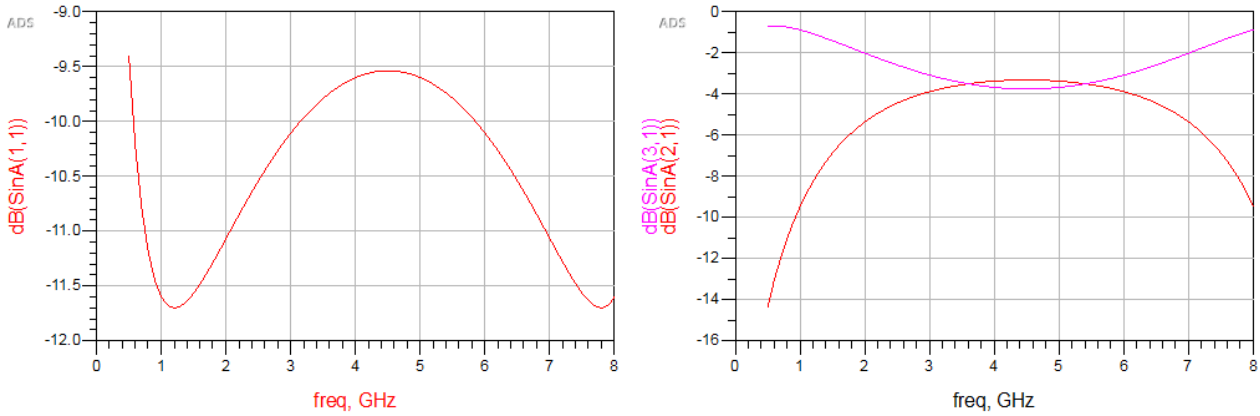



Figure IV-11: Simulation results of initial parameters of the input part of the board A

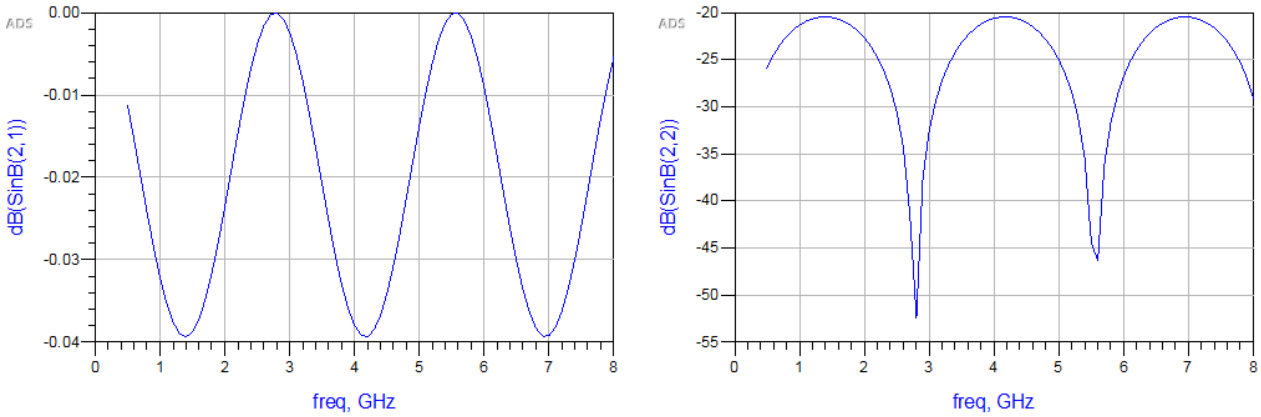



Figure IV-12: Simulation results of initial parameters of the output part of the board B

### IV.5.2 Standards description with ADS elements

In this subparagraph, the three calibration standards (Thru, Line and Reflect) will be simulated by ADS respectively. The standards were measured under 50 ohm GS probes.

For the calibration process, it's important to know the behavior of the standards, because there measurement results will be used to perform the TRL. Here below are the circuit simulation schemes which correspond to the three calibration standards.

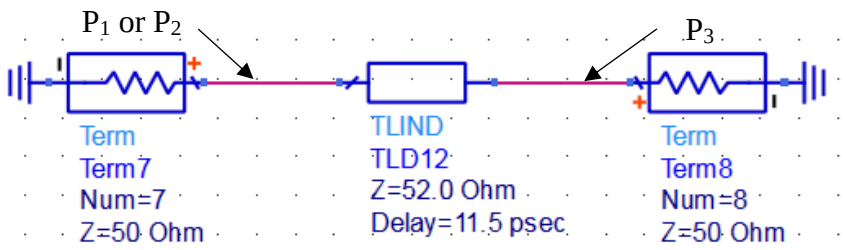



Figure IV-13: "Thru" standard

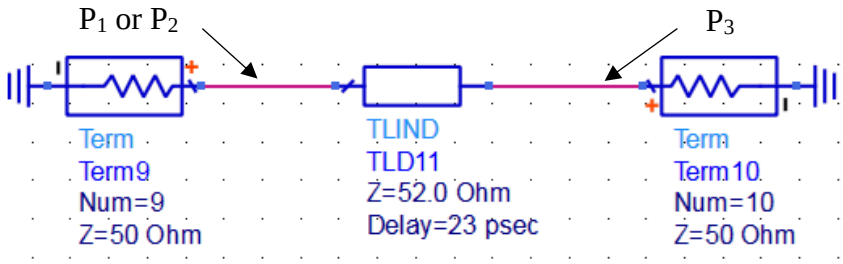



Figure IV-14: "Line" standard

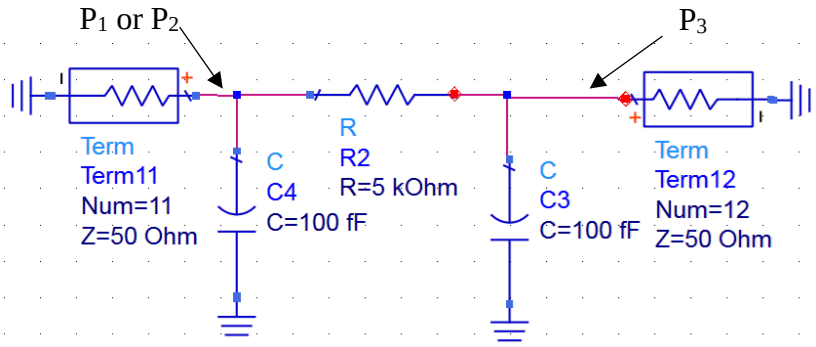



Figure IV-15: "Reflect" standard

### IV.5.3 Double TRL calibration and determination of $Z_{21}$

For a differential device, a double TRL calibration process is needed. All the steps to perform this study were described and illustrated in IV.4. The following three figures refer to the first TRL process which consists of Thru1, Line 1 and reflect 1.

In the first TRL process, accesses 1 and 3 are connected and access 2 leaves open. Whereas the second one is based upon same idea, but a connection is established between accesses 2 and 3 and leaves access 1 open.

From figures IV-16,17 and 18, where they correspond to first TRL process. We extract the S matrix of B and $Z_{00}$, $Z_{10}$, $Z_{11}$ of A.

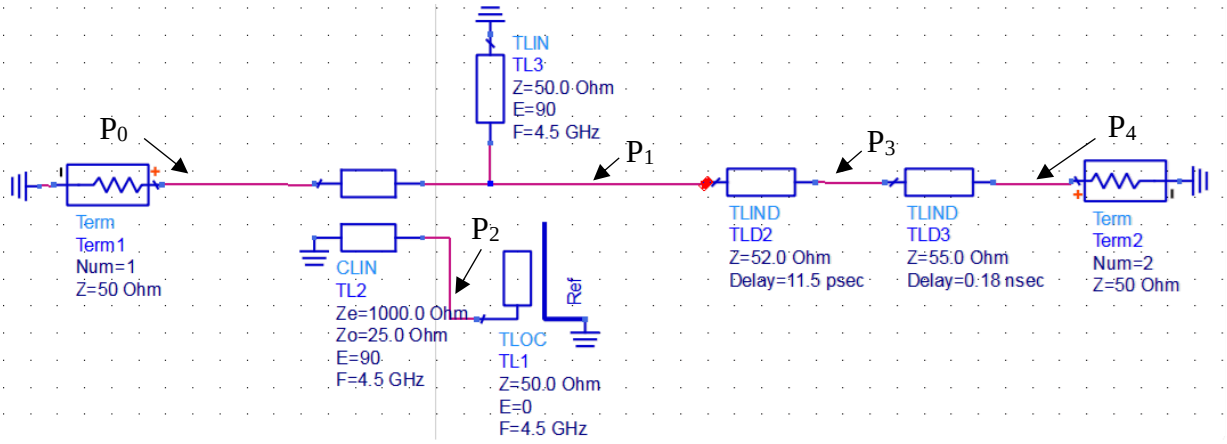



Figure IV-16: PCB model with Thru 1

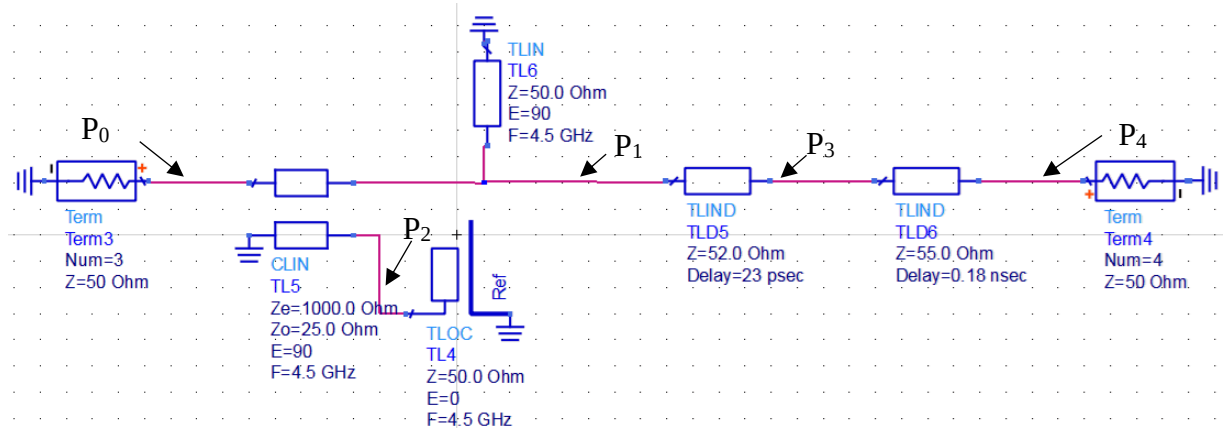



Figure IV-17: PCB model with Line 1

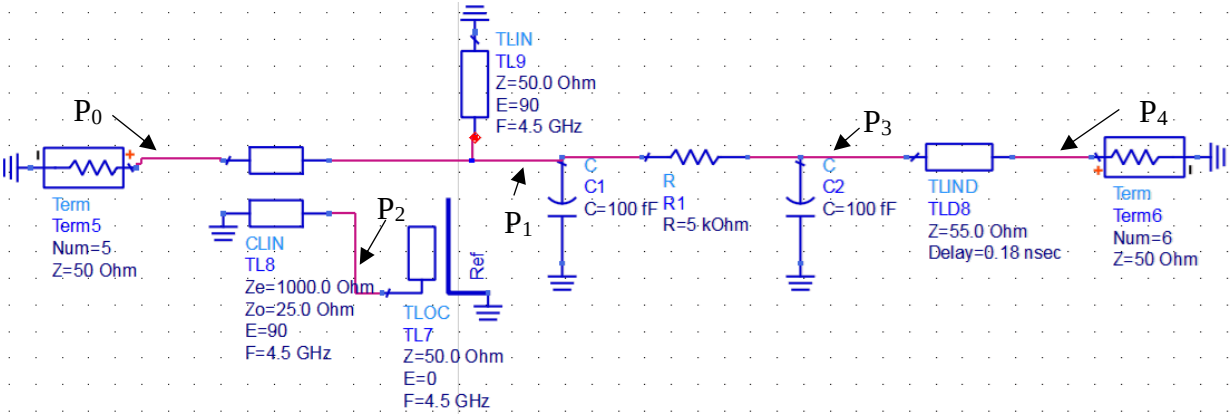



Figure IV-18: PCB model with Reflect 1

From the second TRL process, where the calculations are based upon the same idea, we extract the S matrix of B and $Z_{00}$, $Z_{20}$, $Z_{22}$ of A.

The Third step of TRL process is used to determine $Z_{21}$. Fig. IV-19 below refers to the ADS schematic where the last unknown parameter is to be determined. The determination is based on connecting accesses 1 and 2 with their ports behavior. This behvaior has been descibed in IV-4 and shows in a series connection of a resistor with 3**Ω** to a coil with 3nH.

All the elements of $Z_A$ matrix are obtained and then a normalizion is done by 50**Ω**. The initial parameters A and B will be compared to the calculated one in the next part.

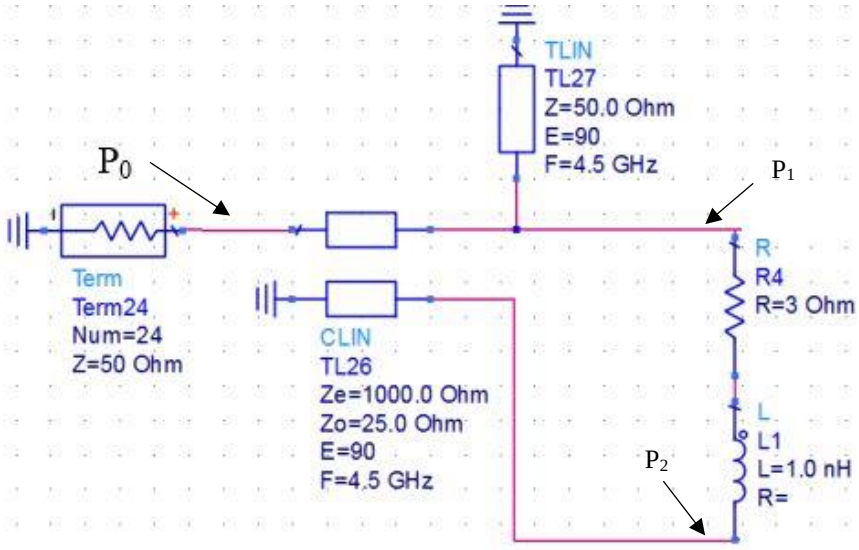



Figure IV-19: ADS schematic to determine $Z_{21}$ parameter

### IV.5.4 Initial vs. Calculated A and B parameters

In this chapter, we introduce a multi TRL process to perform a calibration for a differential device. The study is based on the same idea of the TRL analytical calculations, that we have already dicussed in chapter 2 and validated by measuring an active device in chapter 3.

But for the differential device, it's not sufficient to perform TRL once, that's why we need a double step process for TRL and then a third step to calculate $Z_{21}$. In paragrpagh IV.4, we have illustrated all the calibartion steps needed and later in this parahrapgh IV.5, we have shown all the calibration simulation schematics. Now, in this part we will show the calculated A and B parameters in comparison with the intial ones.

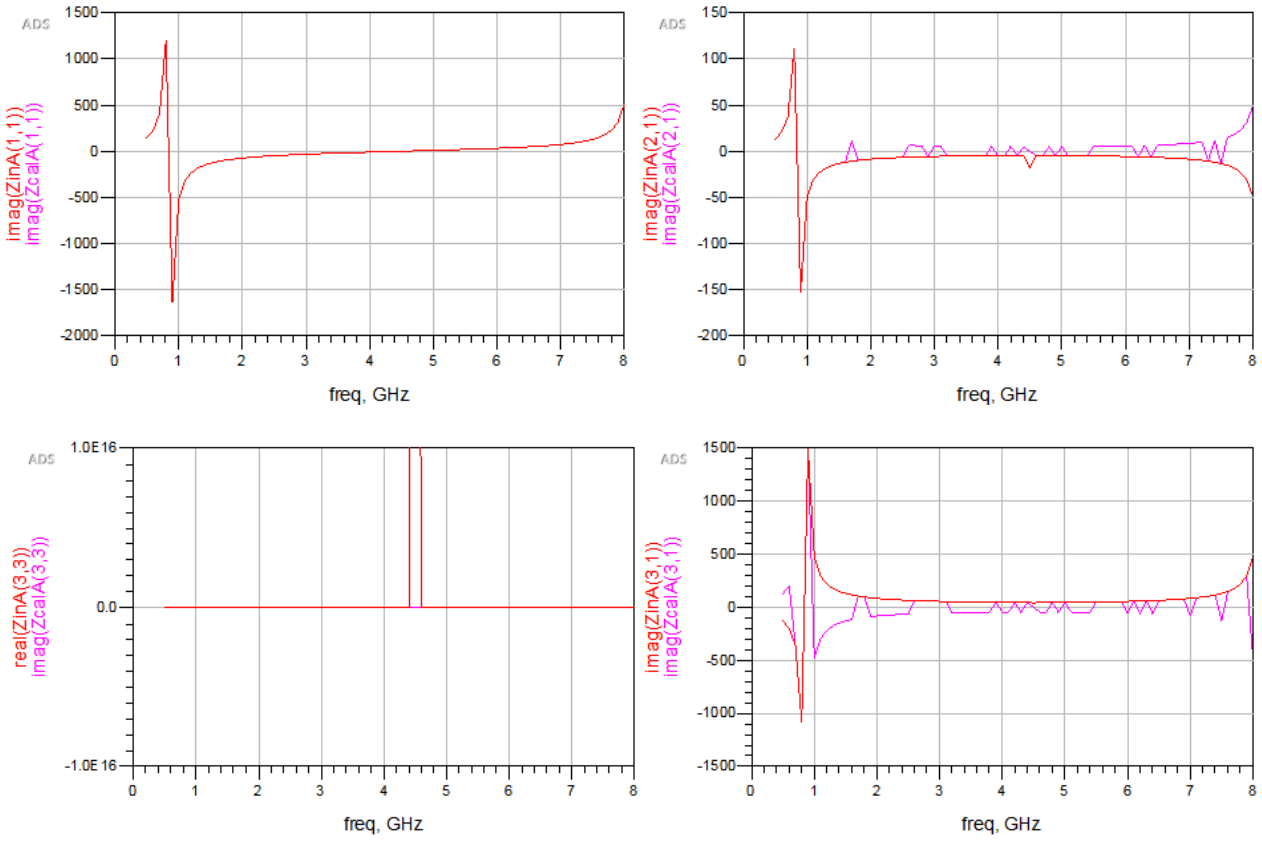



Figure IV-20: Initial vs. Calculated parameters of the input part A

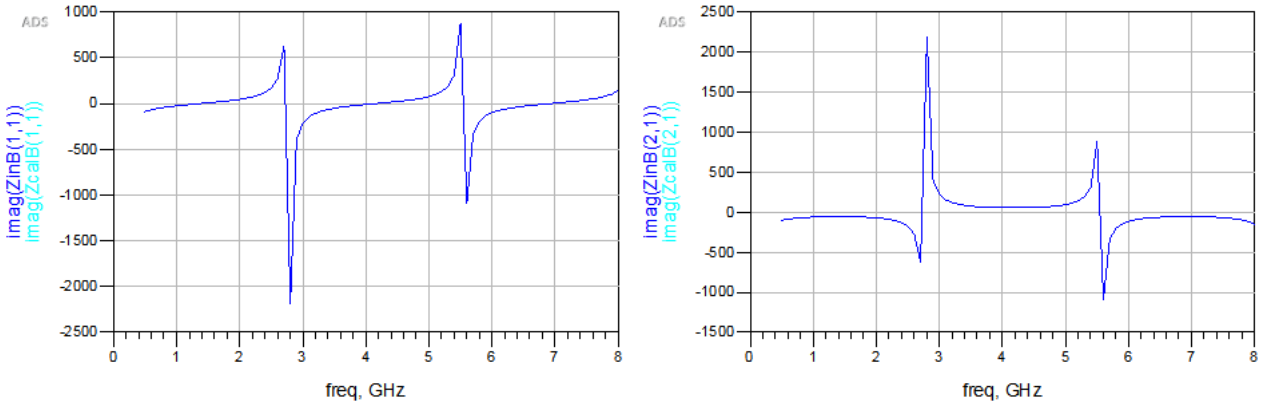



Figure IV-21: Initial vs. Calculated parameters of the output part B

Fig. IV-18, refers to the Z parameters of the calculated and initial parameters A of the input part of the board, which is a three port network and contains the balun. The results show a coincidence within a wide band of frequency where the red and pink colors correspond to the initial and calculated Z parameters of A respectively.

Fig. IV-19, refers to the Z parameters of the calculated and initial parameters B of the output part of the board, which is a two port network. The dark and light blue colors which correspond to the initial and calculated Z parameters of B respectively, show a coincidence over all the frequency band of study. This comparison confirms the importance of multi TRL process which is essential to perform calibration for a differential device. This approach with Z parameters study is a starting point for characterization and modeling the errors embedded with any differential board.

## IV.6 Conclusion and Perspectives

The four-port VNA are now familiar and many calibration procedures developed for two-port analyzers have been extended to four-port. Before an RF measurement, a calibration must be done on an external calibration kit (Cal-kit) provided by manufacturer to eliminate the influence of VNA, cables and RF connectors. The calibration algorithms programmed in most of modern VNAs are applicable for all circuit types. After RF measurements, input and output accesses must be de-embedded from measurement results.

A simple technique has been described to measure the S-parameters of an N-port device at its reference planes using a two-port VNA. For each measurement, the unused N-2 ports are left open. The proposed method has been successfully verified with a branch-line coupler measured with a four-port VNA. On the one hand, this technique allows an accurate characterization of multi-port passive and stable devices. On the other hand, it allows a characterization cost saving in terms of test set equipment and used wafer area.

Nonetheless, due to the high reflection coefficient at non-connected ports, the device must be stable at this measurement configuration. The method applies well to passive circuits, but the stability for active circuits must be checked, even outside the measurement bandwidth. This method could be applied for some device's characterization in which a two-port VNA will be used to measure multi-port circuits.

# CHAPTER V

# GENERAL CONCLUSION AND PERSPECTIVES

## V.1 General Conclusion

This thesis focuses on measurement for characterizing electromagnetic interactions in a board (PCB) using modeling and electromagnetic simulation. This is a potential package for industrial environment in test measurements and for customers for their final end product device. In the context that the complexity and interactions within the board increase, the characterization and calibration of the board are more complicated, and take much time.

The objectives of this thesis aim to establish measurement methodologies in order to reduce the errors embedded with the load board and to reduce time to market for measured devices. To evaluate the developed methodologies, a fully integrated RF front-end MMIC device for WLAN is used.

The device is supported by Presto Engineering Inc. It includes a Low-Noise Amplifier, a TX Power Amplifier and an integrated power detector covering the entire ISM band. It has RX by-pass mode for high signal handling and low-power TX mode to optimize power efficiency of the PA for low-power levels. The tools and software used for measuring, characterizing and testing were found by Presto Engineering and NXP Semiconductors Caen.

The measurement calibration and de-embedding techniques were developed to meet the requirements of industry taking into account the errors embedded within the load board. Firstly, a new approach for calibration and de-embedding method was studied by analytical calculations and then a first validation example has been applied to confirm the proposed study.

The next part of the thesis focuses on modeling and measuring methodologies. Different calibration standards with two port PCB were modeled and simulated by HFSS 3D electromagnetic software. The calibration standards were fabricated by Accurate Circuit Engineering (ACE) in United States of America. The fabricated calibration standards have been characterized and evaluated by electromagnetic simulations. When it is technically possible, these standards can be measured with on-wafer probes.

The study has been realized up to 8.5 GHz by using an experimental single input and single output device which described before. The extraction results of the device within a test board has been compared with an evaluation board that includes a TRL calibration-kit. Our new approach for

TRL calibration and de-embedding technique have been evaluated by measurement and shows a very well agreement. This technique will be extended for complex system e.g 5G devices.

The third part of the thesis talks about the simulation methodology for differential device. The calibration in mixed modes is highly demanded not only for differential devices which are progressively used for high-speed circuit, but also for the mutual coupling between interconnections. Because the drawback of the mixed-mode calibrations in the recent publication is very complex, a double TRL process combined with calibration algorithm is simpler to apply. The mutual coupling between the differential ports has been evaluated by a resistance in series with an inductance.

The method has been applied for the characterization of error terms and has been evaluated by simulations up to 8GHz. All the experimental setup with the calibration steps had allowed to extract the error terms that have been coincide with the initial introduced parameters. Due to time constraints and technological complexity, it hasn't been possible to validate experimentally the method.

The method will be definitely validated when an error calculation is done, allowing the evaluation of the global accuracy of the method.

## V.2 Perspectives

This thesis opens to many potential perspectives:

- To validate the accuracy of the method, an error calculation is necessary.
- RF calibration and de-embedding procedure can be quickly performed by using our approach in an automatic system. For this purpose a specific software based upon National Instrument's LabVIEW, Keysight's VEE or other could allow an automatic environment.
- The design of the calibration standards allowing probe measurements could be very difficult so, a 3D electromagnetic simulation can be a sufficient alternative.
- Development of dedicated calibration and de-embedding solutions for a differential devices with a more complex geometry and number of ports greater than 4.
- New studies must be extended to follow the new trends for complex system e.g 5G devices.

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# LIST OF FIGURES

# LIST OF PUBLICATIONS

## Journals

[1] **K. Hamze**; D. Pasquet; P. Descamps; E. De Ledinghen; " Extraction of Device S-Parameters within Board by using a TRL De-Embedding Technique, " *Microwave and Optical Technology Letters (MOTL), WILEY*, MOP-18-0371, 18 **June 2018.**

[2] **K. Hamze**; D. Pasquet; P. Descamps; E. De Ledinghen; "Analytical calculations for TRL Calibration Method**,"** *Microwave Journal (MWJ), HORIZON HOUSE PUBLICATIONS, INC.* Ref. no. 8348, 24 **July 2018.**

## International IEEE Conferences

[3] **K. Hamze**; D. Pasquet; P. Descamps; E. De Ledinghen; "Applied TRL Calibration Method to Differential Devices Embedded in a Test Board," *Radio and Wireless Week (RWW), Orlando*, Florida, 20-23 **January 2019**.

[4] **K. Hamze**; P. Descamps; D. Pasquet; C. Mayor; C. Gautier; " Evaluation of Substrate's Characteristics from the Relation between Wave and Characteristic Impedances for a CPW," *Microwave and Radar Week (MRW)*, 8th International MRW Conference, Poznan, Poland, 14-17 **May 2018**.

[5] **K. Hamze**; P. Descamps; D. Pasquet; E. De Ledinghen; " Evaluation of the Error due to Bended CPW Lines used in a Calibration Process," *Mediterranean Microwave Symposium,* 17th International MMS Conference, Marseille, France, 28-30 **November 2017**.

[6] **K. Hamze**; D. Pasquet; P. Descamps; E. De Ledinghen; " Theoretical Comparison Between Calibration Standards using Straight and Bended CPWs," *International Conference on Advanced Technologies, Systems and Services in Telecommunications*, 13th International Telsiks Conference, Nis, Serbia, 18-20 **October 2017 .**

# National Conference

[7] **K. Hamze**; P. Descamps; D. Pasquet; E. De Ledinghen; " Parasitic Effects of Coplanar and Slot modes in Waveguides," *Circuits et systèmes intégrés RF/millimétriques du GDR Ondes*, Grenoble, France, **March 2017**.

# APPENDIX 1

## 1.1 Single Input/Output Terminated Ports:

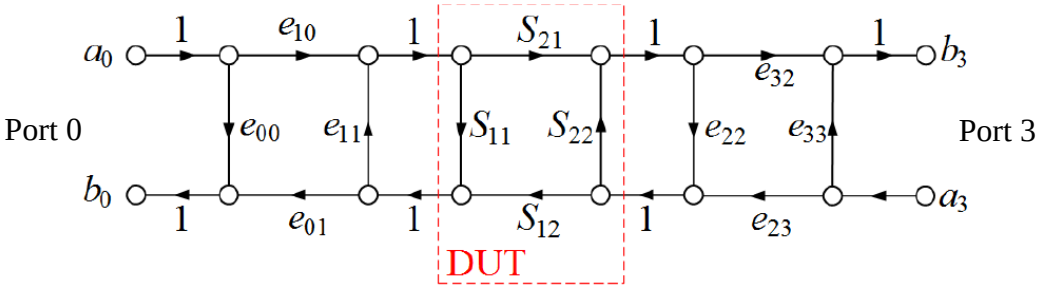


Figure 1.1: Distribution of error terms in two-port network

### 1.1.1 Forward: Three ratios are measured:

$$A_F = \frac{b_0}{a_0} \;;\; B_F = \frac{b_3}{a_0} \;;\; C_F = \frac{a_3}{a_0} \tag{1.1}$$

For a TRL calibration between VNA reference ports, the input impedance of a plane $P_3$ of the VNA is not matched. It means that the ratios $A_F$, $B_F$ depend on port 3 mismatch described by $C_F$.

$$A_F = S_{m11} + C_F S_{m12} \tag{1.2}$$

$$B_F = S_{m21} + C_F S_{m22} \tag{1.3}$$

### 1.1.2 Reverse: Three ratios are measured:

$$A_R = \frac{b_3}{a_3} \;;\; B_R = \frac{b_0}{a_3} \;;\; C_R = \frac{a_0}{a_3} \tag{1.4}$$

For a TRL calibration between VNA reference ports, the input impedance of a plane $P_0$ of the VNA is not matched. It means that the ratios $A_R$, $B_R$ depend on port 0 mismatch described by $C_R$.

$$A_R = S_{m22} + C_R S_{m21} \tag{1.5}$$

$$B_R = S_{m12} + C_R S_{m11} \tag{1.6}$$

$$S_{m11} = \frac{A_F - C_F B_R}{1 - C_F C_R} \tag{1.7}$$

$$S_{m21} = \frac{B_F - C_F A_R}{1 - C_F C_R} \tag{1.8}$$

$$S_{m22} = \frac{A_R - C_R B_F}{1 - C_F C_R} \tag{1.9}$$

$$S_{m12} = \frac{B_R - C_R A_F}{1 - C_F C_R} \tag{1.10}$$

In our case we deal with corrected measurements after the SOLT calculation between the RF coaxial input/output connectors. The "corrected VNA" ports are matched and $C_F = C_R = 0$

### 1.1.3 Calibration standards

*a) Thru* :

$$S = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \tag{1.11}$$

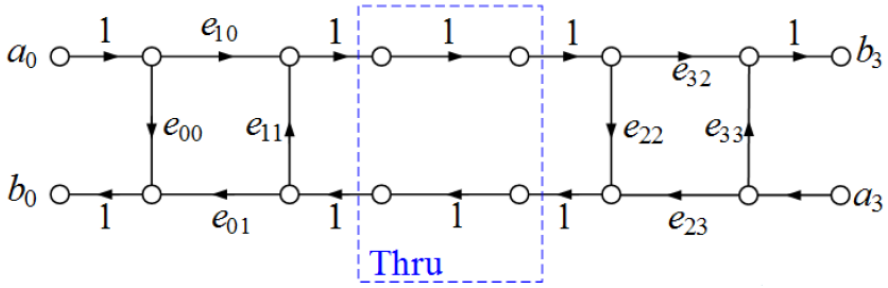


Figure 1.2: Distribution of error terms in Thru standard

$$S_{m11} = e_{00} + e_{10}e_{01}\frac{e_{22}}{1 - e_{11}e_{22}} = R_{F1} \tag{1.12}$$

$$S_{m12} = \frac{e_{01}e_{23}}{1-e_{11}e_{22}} = T_{R1} \tag{1.13}$$

$$S_{m21} = \frac{e_{10}e_{32}}{1-e_{11}e_{22}} = T_{F1} \tag{1.14}$$

$$S_{m22} = e_{33} + e_{32}e_{23}\frac{e_{11}}{1-e_{11}e_{22}} = R_{R1} \tag{1.15}$$

*b) Line where* $S_{11}$=$S_{22}$=0 :

$$S = \begin{pmatrix} 0 & X \\ X & 0 \end{pmatrix} \tag{1.16}$$

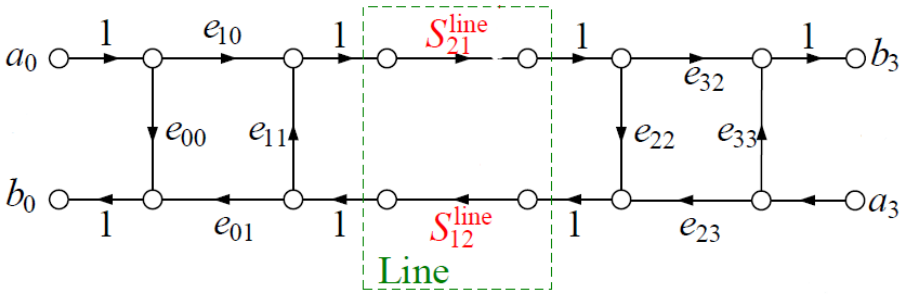


Figure 1.3: Distribution of error terms in Line standard

$$S_{m11} = e_{00} + e_{10}e_{01}\frac{e_{22}X^2}{1-e_{11}e_{22}X^2} = R_{F2} \tag{1.17}$$

$$S_{m12} = \frac{e_{01}e_{23}X}{1-e_{11}e_{22}X^2} = T_{R2} \tag{1.18}$$

$$S_{m21} = \frac{e_{10}e_{32}X}{1-e_{11}e_{22}X^2} = T_{F2} \tag{1.19}$$

$$S_{m22} = e_{33} + e_{32}e_{23}\frac{e_{11}X^2}{1-e_{11}e_{22}X^2} = R_{R2} \tag{1.20}$$

For an actual line $X = e^{-\gamma l}$

*c) Reflect*

$$\mathbf{S} = \begin{pmatrix} \Gamma & T \\ T & \Gamma \end{pmatrix} \tag{1.21}$$

Where |T|<<|**Γ**|

In our case, as $a_3$=0, the reflection coefficient at the input of the reflect.

$$\Gamma_B = \Gamma + \frac{T^2\Gamma}{1 - e_{22}\Gamma} \tag{1.22}$$

The reflect for the calculation can, be considered as a unilateral two-port whose S matrix is:

$$S = \begin{pmatrix} \Gamma_B & 0 \\ 0 & \Gamma_B \end{pmatrix} \tag{1.23}$$

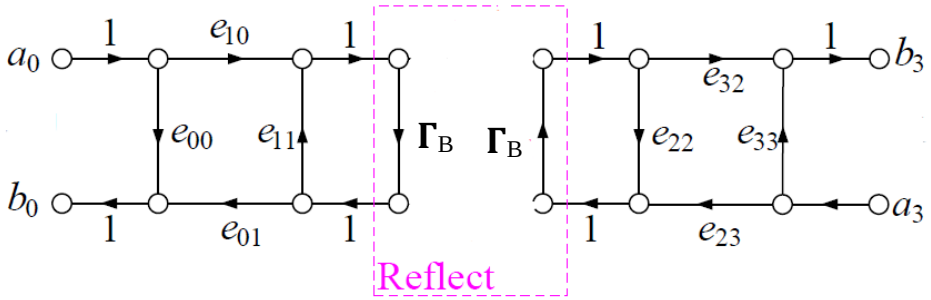


Figure 1.4: Distribution of error terms in reflect standard

$$S_{m11} = e_{00} + \frac{e_{10}e_{01}\Gamma_B}{1 - e_{11}\Gamma_B} = R_{F3} \tag{1.24}$$

$$S_{m22} = e_{33} + \frac{e_{32}e_{23}\Gamma_B}{1 - e_{22}\Gamma_B} = R_{R3} \tag{1.25}$$

## 1.1.4 Solution

From (1.12) and (1.17) and from (1.15) and (1.20):

(1.26)

$$R_{F1} - R_{F2} = \frac{e_{10}e_{22}}{e_{32}}\left(T_{F1} - T_{F2}X\right)$$

$$R_{R1} - R_{R2} = \frac{e_{32}e_{11}}{e_{01}}\left(T_{R1} - T_{R2}X\right) \tag{1.27}$$

Let:

$$\alpha = e_{11}e_{22} \text{ and } \beta = \left(R_{F1} - R_{F2}\right)\left(R_{R1} - R_{R2}\right) \tag{1.28}$$

$$\begin{cases} \beta = \alpha\left(T_{F1} - XT_{F2}\right)\left(T_{R1} - XT_{R2}\right) \\ \dfrac{T_{F1}}{T_{F2}} = \dfrac{1-\alpha X^2}{(1-\alpha)X} \end{cases} \tag{1.29}$$

We obtain two expressions for $\alpha$:

$$\begin{cases} \alpha = \dfrac{\beta}{\left(T_{F1} - XT_{F2}\right)\left(T_{R1} - XT_{R2}\right)} \\ \alpha = \dfrac{T_{F2} - XT_{F1}}{X\left(XT_{F2} - T_{F1}\right)} \end{cases} \tag{1.30}$$

That gives a second degree equation in $X$:

$$X^2 + \frac{\beta - T_{F1}T_{R1} - T_{F2}T_{R2}}{T_{F1}T_{R2}}X + \frac{T_{R1}T_{F2}}{T_{F1}T_{R2}} = 0 \tag{1.31}$$

There are two solutions for this equation, but both values for $|X|$ are close to unity for a line with small losses. It is difficult to choose the right solution. It is safer to choose $|\alpha| << 1$:

$$\alpha = \frac{\beta}{\left(T_{F1} - XT_{F2}\right)\left(T_{R1} - XT_{R2}\right)} \tag{1.32}$$

From (12) and (17):

$$e_{00} = \frac{R_{F1}(1-\alpha)X^2 - R_{F2}\left(1-\alpha X^2\right)}{X^2 - 1} \tag{1.33}$$

$$e_{33} = \frac{R_{R1}(1-\alpha)X^2 - R_{R2}\left(1-\alpha X^2\right)}{X^2 - 1} \tag{1.34}$$

Let:

$$R'_{Fi} = R_{Fi} - e_{00} \text{ and } R'_{Ri} = R_{Ri} - e_{33} \tag{1.35}$$

From (22) and (12):

$$\frac{\Gamma_B}{e_{22}} = \frac{R'_{F3}}{R'_{F1} + \alpha\left(R'_{F3} - R'_{F1}\right)} \tag{1.36}$$

From (23) and (15):

$$\Gamma_B e_{22} = \frac{R'_{R3}\alpha}{R'_{R1} + \alpha\left(R'_{R3} - R'_{R1}\right)} \tag{1.37}$$

So:

$$\Gamma_B = \left( \frac{R'_{F3}R'_{R3}\alpha}{\left(R'_{F1} + \alpha\left(R'_{F3} - R'_{F1}\right)\right)\left(R'_{R1} + \alpha\left(R'_{R3} - R'_{R1}\right)\right)} \right)^{1/2} \tag{1.38}$$

We have choose the right determination of $\Gamma_B$ by comparing its argument to the phase calculated from group delay.

For the remaining elements:

$$e_{22} = \frac{R'_{F1} + \alpha\left(R'_{F3} - R'_{F1}\right)}{R'_{F3}}\Gamma_B \tag{1.39}$$

$$e_{11} = \frac{\alpha}{e_{22}} \tag{1.40}$$

$$e_{10}e_{32} = T_{F1}\left(1-\alpha\right) \tag{1.41}$$

$$e_{01}e_{23} = T_{R1}\left(1-\alpha\right) \tag{1.42}$$

$$e_{10}e_{01} = \frac{R'_{F3}\left(1-e_{11}\Gamma_B\right)}{\Gamma_B} \tag{1.43}$$

$$e_{23}e_{32} = \frac{R'_{R3}\left(1-e_{22}\Gamma_B\right)}{\Gamma_B} \tag{1.44}$$

### 1.1.5 De-Embedding

From the calculated error terms $e_{ij}$ and the $S_{mij}$ parameters measured between $P_0$ and $P_3$, it is possible to calculate the DUT S-parameters:

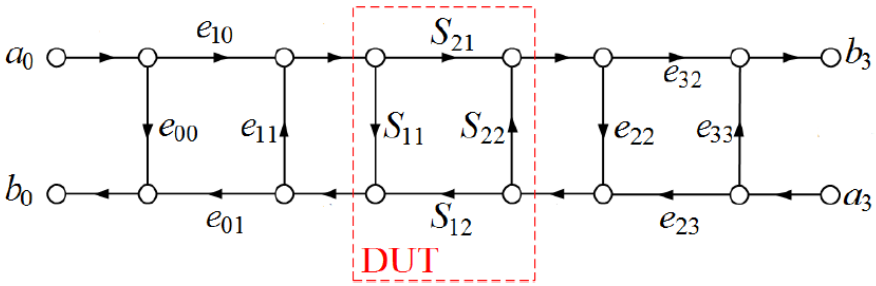


Figure 1.5: Two-port network model

$$S_{11} = \frac{A_{11}\left(1 + A_{22}e_{22}\right) - A_{12}A_{21}e_{22}}{\left(1 + A_{11}e_{11}\right)\left(1 + A_{22}e_{22}\right) - A_{12}A_{21}e_{11}e_{22}} \tag{1.45}$$

$$S_{12} = \frac{A_{12}\left(1 + A_{11}\left(e_{22} - e_{11}\right)\right)}{\left(1 + A_{11}e_{11}\right)\left(1 + A_{22}e_{22}\right) - A_{12}A_{21}e_{11}e_{22}} \tag{1.46}$$

$$S_{21} = \frac{A_{21}\left(1 + A_{22}\left(e_{22} - e_{11}\right)\right)}{\left(1 + A_{11}e_{11}\right)\left(1 + A_{22}e_{22}\right) - A_{12}A_{21}e_{11}e_{22}} \tag{1.47}$$

$$S_{22} = \frac{A_{22}\left(1 + A_{11}e_{11}\right) - A_{12}A_{21}e_{11}}{\left(1 + A_{11}e_{11}\right)\left(1 + A_{22}e_{22}\right) - A_{12}A_{21}e_{11}e_{22}} \tag{1.48}$$

With :

$$A_{11} = \frac{S_{m11} - e_{00}}{e_{10}e_{01}} \tag{1.49}$$

$$A_{12} = \frac{S_{m12}}{e_{01}e_{23}} \tag{1.50}$$

$$A_{21} = \frac{S_{m21}}{e_{10}e_{32}} \tag{1.51}$$

$$A_{22} = \frac{S_{m22} - e_{33}}{e_{32}e_{23}} \tag{1.52}$$

# APPENDIX 2

## 2.1 Multi-ports input/output termination

A differential circuit with at least three ports (two inputs and one output) demands multi-port tests. In addition, multi-port measurement is also required to determine mutual coupling between differential interconnections which influences significantly package performance due to the trend of increasing operation frequency, and signal density.

### 2.1.1 Two-port terminated by $\Gamma_L$ at access 2

$$\begin{cases} b_1 = S_{11}a_1 + S_{12}\Gamma_L b_2 \\ b_2 = S_{21}a_1 + S_{22}\Gamma_L b_2 \end{cases} \tag{2.1}$$

$$S_{22}\Gamma_L b_2 = b_2 - S_{21}a_1 \;\; ; \;\; b_2 - S_{22}\Gamma_L b_2 = S_{21}a_1 \;\; ; \;\; b_2 = S_{21}a_1\left(1 - S_{22}\Gamma_L\right)^{-1} \tag{2.2}$$

$$\frac{b_1}{a_1} = S_{11} + S_{12}\Gamma_L S_{21}\left(1 - S_{22}\Gamma_L\right)^{-1} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2.3}$$

### 2.1.2 Three-port terminated by $\Gamma_L$ at access 3

$$\left(\mathbf{S^H}\right) = \begin{pmatrix} \left(\mathbf{S_{11}^H}\right) & \left(\mathbf{S_{12}^H}\right) \\ \left(\mathbf{S_{21}^H}\right) & S_{22}^H \end{pmatrix} \tag{2.4}$$

$$\left(\mathbf{S_{11}^H}\right) = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \;\; ; \;\; \left(\mathbf{S_{12}^H}\right) = \begin{pmatrix} S_{13} \\ S_{23} \end{pmatrix} \;\; ; \;\; \left(\mathbf{S_{21}^H}\right) = \begin{pmatrix} S_{31} & S_{32} \end{pmatrix} \;\; ; \;\; S_{22}^H = S_{33} \tag{2.5}$$

$$\begin{cases} \begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \left(\mathbf{S_{11}^H}\right)\begin{pmatrix} a_1 \\ a_2 \end{pmatrix} + \left(\mathbf{S_{12}^H}\right)\Gamma_L b_3 \\ b_3 = \left(\mathbf{S_{21}^H}\right)\begin{pmatrix} a_1 \\ a_2 \end{pmatrix} + S_{22}^H\Gamma_L b_3 \end{cases} \tag{2.6}$$

$$b_3 = \left(\mathbf{S_{21}^H}\right)\begin{pmatrix} a_1 \\ a_2 \end{pmatrix}\left(1 - S_{22}^H\Gamma_L\right)^{-1} \tag{2.7}$$

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \left( \left(\mathbf{S_{11}^H}\right) + \left(\mathbf{S_{12}^H}\right)\Gamma_L \left(\mathbf{S_{21}^H}\right) \left(1 - S_{22}^H \Gamma_L\right)^{-1} \right) \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{2.8}$$

### 2.1.3 *M*-port terminated on *N* accesses

Four-port VNA are not always available. In that case, a two-port VNA must be used. For the moment, we have considered the error model as two two-ports.


Figure 2.1: Two-port error models

Instead, we could consider the error model as a four-port

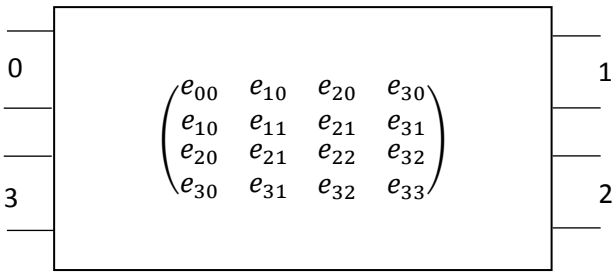


Figure 2.2: Four-port error model

0 and 3 are the planes where we measure with the VNA between SMAs. 1 and 2 are the DUT reference planes.

$$\left(\mathbf{S^M}\right) = \begin{pmatrix} \left(\mathbf{S_{11}^M}\right) & \left(\mathbf{S_{12}^M}\right) \\ \left(\mathbf{S_{21}^M}\right) & \left(\mathbf{S_{22}^M}\right) \end{pmatrix} \tag{2.9}$$

$$\left(\mathbf{S_{11}^M}\right) = \begin{pmatrix} S_{11}^M & \cdots & S_{1,M-N}^M \\ \cdots & \cdots & \cdots \\ S_{M-N,1}^M & \cdots & S_{M-N,M-N}^M \end{pmatrix} \; ; \left(\mathbf{S_{22}^M}\right) = \begin{pmatrix} S_{M-N+1,M-N+1}^M & \cdots & S_{M-N+1,M}^M \\ \cdots & \cdots & \cdots \\ S_{M,M-N+1}^M & \cdots & S_{M,M}^M \end{pmatrix} \tag{2.10}$$

$$\left(\mathbf{S}_{\mathbf{12}}^{\mathbf{M}}\right)=\begin{pmatrix} S_{1,M-N+1}^{M} & \cdots & S_{1,M}^{M} \\ \cdots & \cdots & \cdots \\ S_{M-N,M-N+1}^{M} & \cdots & S_{M-N,M}^{M} \end{pmatrix} ; \left(\mathbf{S}_{\mathbf{21}}^{\mathbf{M}}\right)=\begin{pmatrix} S_{M-N+1,1}^{M} & \cdots & S_{M-N+1,M-N}^{M} \\ \cdots & \cdots & \cdots \\ S_{M,1}^{M} & \cdots & S_{M,M-N}^{M} \end{pmatrix} \qquad (2.11)$$

# ABSTRACT

The work of this thesis deals with the developing of an efficient methodology for modeling parasitic effects within a broadband board. Reducing "Time to Market" for the design of RF and microwave products necessitates the development of an efficient characterization and modeling methodologies for better calibrating the errors embedded within the test board.

Main results concern the following contributions:

- Development of an innovative calibration standards to characterize and model the parasitic effects embedded within the model.
- Elaboration of a new approach based on a TRL calibration technique and de-embedding method effective to de-embed these effects.
- Application on differential devices upon using multi-port TRL calibration.

The new proposed approach for calibration and de-embedding is applied to an active device which is being in use in industry nowadays. The measurement result of the device within a load board has been compared to a calibrated measurement using an evaluation board that include TRL standards. This study has been extended with multi-port TRL calibration to be used for large variety of devices like the differential ones.

***Key-words:*** TRL calibration, De-embedding, DUT, Multi-Port, Load board, Differential device.

# RESUME

Les travaux de cette thèse traitent de l'élaboration d'une méthodologie efficace pour la modélisation des effets parasites dans une carte en large bande de fréquence. La réduction du «Time to Market» pour la conception des produits RF et hyperfréquences nécessite le développement d'une méthode efficace de caractérisation et de modélisation pour mieux prendre en compte les erreurs incluses dans la carte de test.

Les principaux résultats concernent les contributions suivantes :

- Mise au point des standards de calibrage innovateur pour caractériser et modéliser les effets parasites inhérent au modèle.
- Élaboration d'une nouvelle approche basée sur une technique de calibrage TRL et une méthode d'élimination efficace de ces effets.
- Application aux dispositifs différentiels lors de l'utilisation du calibrage TRL dans le cas de plusieurs ports.

La nouvelle approche proposée pour le calibrage et le de-embedding est appliquée à un dispositif actif qui est actuellement utilisé dans l'industrie. Les résultats de mesure d'un dispositif inclus dans une carte de test ont été comparés à des mesures calibrées à l'aide d'une carte d'évaluation comportant des standards TRL. Cette étude a été prolongée avec le calibrage TRL multi-port pour être utilisé pour la bande large des dispositifs comme les dispositifs différentiels.

***Mots-clés**:* TRL, de-embedding, DUT, multi-port, carte de test, dispositif différentiel.