



# Axial GaAs/InAs nanowire heterostructures for photonic applications on Si

Daria Vyacheslavovna Beznasyuk

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## THÈSE

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Présentée par

**Daria Vyacheslavovna BEZNASYUK**

Thèse dirigée par **Julien CLAUDON**, Chercheur CEA, CEA Grenoble  
et codirigée par **Moira HOCEVAR**

préparée au sein du **Laboratoire Institut Néel**  
et de l'**Ecole Doctorale de Physique**

**Nanofils à hétérostructures axiales  
GaAs/InAs pour applications photoniques  
sur Si**  
**Axial GaAs/InAs nanowire heterostructures  
for photonic applications on Si**

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devant le jury composé de :

**Monsieur MICHEL GENDRY**

DIRECTEUR DE RECHERCHE, CNRS DELEGATION RHONE AUVERGNE,  
Président

**Monsieur GILLES PATRIARCHE**

DIRECTEUR DE RECHERCHE, CNRS DELEGATION ILE-DE-FRANCE SUD,  
Rapporteur

**Madame LUCIA SORBA**

PROFESSEUR, ECOLE NORMALE SUPERIEURE DE PISE ITALIE, Rapporteur

**Monsieur JEAN-LUC ROUVIERE**

INGENIEUR CHERCHEUR, CEA GRENOBLE, Examineur

**Monsieur PETER KROGSTROP**

PROFESSEUR, UNIVERSITE DE COPENHAGUE - DANEMARK, Examineur



*I don't know anything, but I do know that everything is interesting  
if you go into it deeply enough.*

Richard Feynman

# Résumé

Un objectif technologique important de l'industrie des semiconducteurs concerne l'intégration sur silicium de semiconducteurs III-V à bande interdite directe tels que InAs et GaAs, pour réaliser des émetteurs et détecteurs de lumière aux longueurs d'onde de télécommunication. L'épitaxie de couches minces d'InAs et de GaAs sur silicium est cependant difficile en raison de la grande différence de paramètre de maille entre ces matériaux. Ces films minces épitaxiés présentent une interface de mauvaise qualité limitant les performances de futurs dispositifs. Pour surmonter le défi de l'épitaxie de matériaux à fort désaccord de maille, il a été proposé d'utiliser des nanofils en raison de leur dimension latérale réduite et de leur rapport hauteur/largeur élevé. Ainsi, les nanofils relâchent la contrainte par relaxation élastique sur la paroi latérale des nanofils. Cela se produit non seulement à l'interface nanofils/substrat, mais aussi à l'interface entre matériaux différents le long de l'axe des nanofils.

Dans ce contexte, ma thèse visait à faire croître des hétérostructures axiales de nanofils GaAs/InAs sur des substrats silicium pour réaliser des émetteurs à photons uniques. Lors de ce travail expérimental, j'ai fait croître des nanofils par le mécanisme vapeur-solide-liquide assisté par catalyseurs d'or dans un réacteur d'épitaxie par jet moléculaire. Les nanofils ont ensuite été caractérisés en utilisant la spectroscopie à rayons X par dispersion d'énergie et la microscopie électronique à transmission pour évaluer leur composition et leur structure cristalline. La distribution de la contrainte a été étudiée expérimentalement par analyse de phase géométrique, puis comparée à des simulations par éléments finis. Au cours de cette thèse, j'ai abordé différents défis inhérents aux hétérostructures axiales de nanofils, tels que la formation de nanofils tordus, la composition graduelle de l'interface et la croissance radiale parasite.

J'ai d'abord optimisé le protocole de croissance pour éviter la formation de nanofils tordus. Les nanofils changent habituellement de direction de croissance lorsque le catalyseur d'or à l'extrémité du nanofil a été déstabilisé. En gardant une forte sursaturation dans la gouttelette d'or pendant toute la procédure de croissance, j'ai obtenu des nanofils droits d'InAs/GaAs avec un rendement de 90%. J'ai alors optimisé les flux de matériaux pour réduire la composition graduelle de l'interface entre les segments d'InAs et de GaAs. L'utilisation d'un flux d'indium élevé pendant la croissance du segment InAs a permis d'obtenir une interface abrupte de 5 nm.

Grâce à l'analyse de la composition chimique des nanofils, j'ai observé que le segment nom-

inalement pur d'InAs est en fait un alliage ternaire  $\text{In}_x\text{Ga}_{1-x}\text{As}$ . J'ai découvert que l'incorporation de Ga dans le segment nominal InAs est due à la diffusion d'adatoms Ga créés thermiquement sur les nanofils GaAs et sur la couche de GaAs bidimensionnelle développée sur le substrat de silicium. L'utilisation de diamètres larges de nanofils supprime la diffusion de Ga le long des parois latérales des nanofils, permettant ainsi la croissance d'un segment d'InAs pur au-dessus de celui de GaAs.

Enfin, j'ai étudié la distribution de la contrainte de 7% à l'interface InAs/GaAs. Celle-ci est répartie le long du nanofil et dépend du diamètre du nanofil et de la composition de l'interface. J'ai observé que les nanofils de diamètre inférieur à 40 nm sont exempts de dislocations: la contrainte est relaxée élastiquement via la courbure des plans cristallins proches des parois latérales du nanofil. D'autre part, les nanofils avec des diamètres supérieurs à 95 nm relaxent à la fois élastiquement et plastiquement, par une courbure des plans et la formation de dislocations.

En conclusion, j'ai fabriqué des hétérostructures de matériaux à fort désaccord de maille. J'ai pu confirmer que les interfaces axiales GaAs/InAs sont pseudomorphiques en dessous d'un certain diamètre critique. Ces résultats constituent une première étape vers la réalisation de boîtes quantiques InAs dans des nanofils de GaAs intégrés sur silicium: un système prometteur pour l'émission de photons uniques sur puce.

# Abstract

Combining direct bandgap III-V compound semiconductors, such as InAs and GaAs, with silicon to realize on-chip optical light emitters and detectors at telecommunication wavelengths is an important technological objective. However, traditional thin film epitaxy of InAs and GaAs on silicon is challenging because of the high lattice mismatch between these materials. These epitaxial thin films exhibit a poor quality at the interface with silicon, limiting the performance of future devices. Nanowires can overcome the challenge of combining high lattice mismatched materials owing to their small lateral size and high aspect ratio. Thanks to their free, unconstrained surfaces, nanowires release the mismatch strain via elastic lateral relaxation. This occurs not only at the nanowire/substrate interface, but also at materials' interfaces along the nanowire axis.

In this context, my thesis aimed at growing axial GaAs/InAs nanowire heterostructures on silicon substrates to realize on-chip, integrated, single-photon emitters. In this experimental work, I grew nanowires by gold-assisted vapor liquid solid mechanism in a molecular beam epitaxy reactor. The nanowires were then characterized using energy dispersive x-ray spectroscopy and transmission electron microscopy to evaluate their composition and crystalline structure. Strain distribution was studied experimentally using geometrical phase analysis and compared theoretically with the finite element simulations. During this thesis, I tackled different challenges inherent to axial nanowire heterostructures, such as kinking during material exchange, compositionally graded interfaces, and radial overgrowth.

First, I developed an optimized a growth protocol to prevent the formation of kinks. Kinks usually appear when the gold catalyst at the nanowire tip has been destabilized. By keeping a high supersaturation in the gold droplet during the entire growth procedure, straight InAs-on-GaAs nanowires were achieved with a yield exceeding 90%. By a careful tuning of the material fluxes supplied during growth, I significantly improved the interface sharpness between the InAs and GaAs nanowire segments: the use of a high In flux during the growth of the InAs segment resulted in a 5 nm composition gradient at the InAs/GaAs interface.

Through the careful analysis of the nanowires' chemical composition, I observed that the nominally pure InAs segments grown on top of GaAs are in fact ternary  $\text{In}_x\text{Ga}_{1-x}\text{As}$  alloys. I found out that Ga incorporation in the nominal InAs segment is due to the diffusion of Ga adatoms thermally created on the GaAs nanowire sidewalls and on the two-dimensional GaAs layer grown

on silicon substrate. I demonstrated that the use of large nanowire diameters prevents Ga diffusion along the nanowire sidewalls, resulting in the growth of pure InAs segments on top of GaAs.

Finally, I studied how 7% mismatch strain at the InAs/GaAs interface is distributed along the nanowire, depending on the nanowire diameter and interface sharpness. I observed that nanowires with diameters below 40 nm are free of misfit dislocations regardless of the interface sharpness: strain is fully, elastically released via crystalline planes bending close to the nanowire sidewalls. On the other hand, nanowires with diameters above 95 nm at the interface exhibit strain relaxation, both elastically and plastically, via plane bending and the formation of misfit dislocations, respectively.

In conclusion, I have successfully fabricated highly mismatched heterostructures, confirming the prediction that axial GaAs/InAs interfaces are pseudomorphic below a certain critical diameter. These findings establish a first step toward the realization of high quality InAs quantum dots in GaAs nanowires on silicon: a promising system for on-chip single photon emission.

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# Chapter 1

## Introduction

### 1.1 Quantum dot-based single photon sources

In the last few decades single-photon sources have gained an immense popularity in quantum-information science. Such sources emit a light pulse containing exactly one photon in response to an excitation signal. They could find applications in quantum-secure communication [1] and photonic quantum information processing [2]. Furthermore, a device which emits a perfectly regulated stream of photons (i.e. without noise) could also be used in optical metrology, as a standard of light flux.

While a single atom can be employed to generate single-photon light pulses, a practical source should preferentially be a solid-state one. In this context, semiconductor quantum dots have emerged as a promising candidate. Quantum dots are optically-active nanostructures which typical size is in the order of 10 nanometers. Such a nanostructure confines charge carriers in the three directions of space. As a result, their electronic energy spectrum features discrete states, very similar to the one of a real atom. In particular, the radiative recombination of a single electron-hole pair (or an exciton) trapped in the quantum dot leads to the emission of a single-photon pulse. Experimentally, the single-photon nature of the light pulse is revealed by intensity correlation measurements, which display antibunching at short delays, proving that the photons are indeed emitted one by one.

Up to recently, most semiconductor quantum dots, investigated in quantum optics, have been obtained via a self-assembly process<sup>1</sup> over a two-dimensional substrate. To preserve optical properties, these quantum dots are usually capped by a top semiconductor layer. At cryogenic temperature, these zero-dimensional emitters have demonstrated remarkable performance: individual quantum dots offer a perfect antibunching, associated with a quantum yield very close to one [3, 4, 5]. In addition, light emission is stable, without short-term blinking nor long-term intensity

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<sup>1</sup>Stranski-Krastanow growth mode.

loss due to aging processes. However, the collection of light from these structures is very low, because of two issues. First, the quantum dot is much smaller than the optical wavelength. As a result, it emits light in all the directions of space. Furthermore, because of the large refractive index of the two-dimensional matrix which surrounds the quantum dot, only a very small fraction (typically 1%) of the emitted photons can be collected with free-space optics.

A successful strategy to improve collection efficiency consists in inserting the quantum dot into a photonic structure, such as a photonic-crystal microcavity [6], a pillar microcavity [7, 8], a nanowire waveguide [9]. Quantum dots inserted into a photonic-crystal microcavity achieve a brightness of around 50%. Significantly higher brightness of 80%, combined with clean antibunching properties, are achieved both with pillar cavities and top-down tapered nanowires [10, 9]. Yet such devices are obtained with a complex, multi-stage top-down fabrication process. Despite the recent development of deterministic fabrication techniques, the control over the quantum dot position remains difficult. Finally, state-of-the-art devices often employ InAs/GaAs self-assembled quantum dots, with an emission wavelength in the 900-950 nm range. For the distribution of single photons over long distances, it would be very desirable to operate a quantum dot which emits light around 1.3  $\mu\text{m}$  or 1.5  $\mu\text{m}$ , the low-loss transmission windows of optical fibers.

A promising, alternative fabrication strategy is to grow directly a semiconductor nanowire, and to define the quantum dot as an axial heterostructure (see Figure 1.1) [11, 12, 13]. Importantly, this quantum dot fabrication strategy offers a great freedom for the definition of the quantum dot geometry and alloy composition. Moreover, nanowires can host material combinations of different lattice parameters and different nature since the crystal lattice can relax laterally and elastically by releasing the strain caused by the lattice mismatch [14]. Combination of different materials with dislocation-free interfaces, therefore, can be realized in nanowire heterostructures with no equivalent in traditional two dimensional thin film epitaxy. Furthermore, the strain arising at the interface between mismatched materials can serve as an additional tuning parameter for band-gap engineering. Last but not least, nanowire heterostructures can be epitaxially grown on various substrates, including silicon wafers, and therefore open up a fascinating opportunity to efficiently couple electronics and optics. Finally, one can easily define a waveguide around this nanowire quantum dot by performing a lateral overgrowth. With this technique, the quantum dot is naturally localized on the wire axis, which optimizes the photonic performance.

As previously mentioned, single photon sources based on quantum dots emitting at 1.5  $\mu\text{m}$  are particularly interesting thanks to the reduced losses of telecom fibers at this wavelength. InAs is a semiconductor with a very narrow band gap (0.35 eV), high electron mobility ( $4 \times 10^4 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ ) and is considered to be one of the most attracting material to realize so. Despite the fact that pure InAs has its emission wavelength at approximately 3.5  $\mu\text{m}$  one can engineer the band gap by tuning the height of the quantum dot, exploiting material strain generated at the heterointerface, or

by creating a ternary InGaAs alloy [15].

The present thesis is dedicated to the growth of GaAs/InAs nanowire heterostructures on Si substrates with the main idea to realize single photon emitters and detectors at the telecommunication wavelength. Before proceeding to the presentation of the work, we first discuss the state-of-the art for InAs/InGaAs nanowire quantum dots.

## 1.2 InAs/GaAs nanowire quantum dots: state-of-the-art

As for today, many groups have demonstrated the formation and investigated optical properties of quantum dots in nanowire axial heterostructures. Various material combinations were investigated, such as AlGaAs/GaAs [16, 17], GaAsP/GaAs [18], GaP/GaAsP [11], InP/InAsP [19], InAs/InP [20, 21], Si/GaP/GaAs [22], ZnSe/CdSe [23], GaN/AlN [24]. Yet only a few works have explored the growth and optical properties of InAs quantum dots inserted axially in GaAs nanowires [25, 15]. This can be explained by the difficulties in the growth of InAs-on-GaAs nanowire heterostructures, such as strain, kinking and graded composition at the interface as well as radial overgrowth. These growth challenges will be considered in detail in Chapter 2.

The first successful report on the optical properties of InAs quantum dots inserted into a GaAs nanowire heterostructure was demonstrated by Panev and coauthors in 2003 [25]. In this work, heterostructures were grown by chemical beam epitaxy technique. The embedded quantum dots were about 40 nanometers in diameter and not more than 50 nanometers in height. At low excitation power a single sharp exciton photoluminescence peak was observed, which confirmed the presence of a quantum dot. The emission peak (around 880 nm) is characteristic for a quantum dot made of a ternary In(Ga)As alloy with a large Ga content. Moreover, photoluminescence results were obtained at liquid helium temperatures, which potentially limits the practical use of such heterostructures. More recently another promising work was performed by Tatebayashi and coworkers [15]. The samples were grown by means of metalorganic chemical vapor deposition technique. The authors grew two types of samples: a first one with  $\text{In}_{0.3}\text{Ga}_{0.7}\text{As}$  quantum dots and a second one with nominally pure InAs quantum dots. In addition, the quantum dots were different in height (from 1.5 to 16 nanometers) in order to tune the emission wavelength. For the both types of quantum dots, single sharp emission peaks were obtained at liquid helium temperatures. It was observed that the emission peak is redshifted with height of the quantum dot (from 870 nanometers to 1000 nanometers). Moreover, the emission peaks remained stable even at room temperature, demonstrating the high quality of the grown quantum dots. Again, the nominally pure InAs quantum dots were found to be made of ternary In(Ga)As quantum dots, which did not allow to reach the desirable low-loss window of 1.3-1.6  $\mu\text{m}$  wavelengths. Therefore, despite these pioneering works, achieving emission from InAs quantum dots inserted into GaAs nanowires at telecommunication wavelengths is still a challenge.

## 1.3 Thesis objectives and content

### *Objectives:*

The prime motivation of this thesis has been to develop and realize on-chip highly sensitive optical light emitters and detectors at telecommunication wavelengths. We aim to grow optically active low band-gap InAs quantum dots inside nanowire heterostructures. These structures will be grown by molecular beam epitaxy using a gold droplet catalyst.

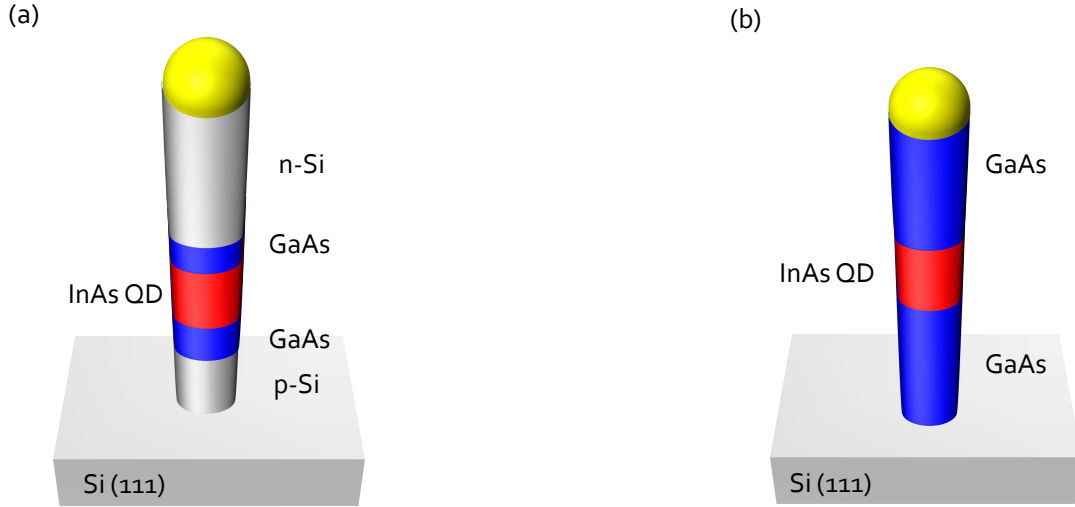
We consider two key nanowire-based configurations to realize the devices, where an InAs quantum dot is inserted in a Si nanowire (Figure 1.1 a) or in a GaAs nanowire (Figure 1.1 a). The first configuration is of great importance for the realization of highly-sensitive photodetectors. Indeed, a single-photon can be absorbed by the InAs quantum dot, generating an electron-hole pair. Under proper voltage biasing, an avalanche amplification takes place in the Si segment leading to a detectable signal. However, InAs and Si have an extremely high lattice-mismatch (more than 11%), which is likely to lead to a deterioration of a crystalline quality at the interface even in a nanowire heterostructure [14]. In contrast, the mismatch between Si and GaAs is only 4%. Therefore, we propose to use thin GaAs barriers between the Si and InAs segments in order to reduce the mismatch strain and produce dislocations-free heterointerfaces. Thus the final nanowire heterostructure is very sophisticated and contains materials from different semiconductor families, namely GaAs and InAs (III-V group) and Si (IV group). The second configuration is a simplified version of the first one: a low band-gap InAs quantum dot is inserted into a larger band-gap GaAs nanowire. Therefore, our main focus is to growth GaAs/InAs nanowire heterostructures on Si substrates with the main idea to implement on-chip, integrated, single-photon emitters.

### *Organization of the manuscript:*

This thesis is organized as follows. In Chapter 2 I present general physical concepts, understanding of which is required before proceeding to the results. The concepts are discussed from an experimental point of view based on significant examples from literature. The growth of InAs quantum dots in GaAs nanowires poses significant challenges, such as kinking, interface grading and shell overgrowth. They are discussed at the end of the Chapter.

In Chapter 3, I describe the experimental techniques used throughout the project. I discuss the basic components and working principles of molecular-beam epitaxy reactor, scanning electron microscope, transmission electron microscope and image processing technique such as Geometrical Phase Analysis.

In Chapter 4, I present results on the molecular-beam epitaxy growth of GaAs segments on top of Si nanowires. I use Si nanowires which are grown by chemical vapor deposition, as template stems. I demonstrate the possibility to re-grow GaAs segments on top of Si stems by recycling the gold catalyst present at the Si nanowire tips. I discuss in details the challenges which arise from such a growth method, namely kinking of GaAs segment, attributed to the initial position of Au



**Figure 1.1:** Schematic representation of two nanowire-based devices configurations, proposed and considered in this thesis.

droplets at the tips of Si nanowires, gold diffusion on the nanowire sidewalls and the resulting growth of GaAs nanoneedles catalyzed by the gold clusters, and parasitic GaAs overgrowth on faceted sidewalls of Si nanowires. In order to overcome these problems, I propose alternative way to combine GaAs and Si, where Si stems are etched out of bulk silicon with gold droplets used as mask. Preliminary results using etched Si nanowires are demonstrated.

I focus on the growth of pure wurtzite GaAs nanowires grown by Au-assisted vapor–liquid–solid mechanism on Si substrates in Chapter 5. I first study the nucleation process of GaAs nanowires on Si. By a set of growth experiments, I observe that GaAs nanowires are formed only after 3 minutes of GaAs deposition. Before that time, in-plane GaAs traces form, grow horizontally and eventually cover the entire substrate surface. I show that the growth of Au-assisted GaAs nanowires on Si substrates is possible in a wide temperature window, yet the best morphology is achieved at 610 °C. I further study the influence of material fluxes on the nanowires growth. I find that an increase in the Ga flux at a constant As flux leads to radial overgrowth. On the contrary, increasing the As flux at a constant Ga flux increases the nanowires growth rate. Finally, I demonstrate the growth of pure wurtzite GaAs nanowires on silicon using a high V/III ratio.

Chapter 6 discusses the Au-assisted growth of straight InAs-on-GaAs nanowire heterostructures on Si. I tackle different challenges inherent to axial nanowire heterostructures, such as kinking during material exchange, compositionally graded interfaces, and radial overgrowth. First, I develop an optimized growth protocol to prevent the formation of kinks. By keeping a high supersaturation in the gold droplet during the entire growth procedure, straight InAs-on-GaAs nanowires were achieved with a yield exceeding 90%. By a careful tuning of the material fluxes



supplied during growth, I significantly improve the interface sharpness between the InAs and GaAs nanowire segments: the use of a high In flux during the growth of the InAs segment resulted in a 5 nanometers composition gradient at the InAs/GaAs interface. Through the careful analysis of the nanowires' chemical composition, I observed that the nominally pure InAs segments grown on top of GaAs are in fact ternary  $\text{In}_x\text{Ga}_{1-x}\text{As}$  alloys. By a set of experiments I establish that Ga incorporation in the nominal InAs segment is due to the diffusion of Ga adatoms thermally created on the GaAs nanowire sidewalls and on the two-dimensional GaAs layer grown on silicon substrate. I demonstrate that the use of large nanowire diameters prevents Ga diffusion along the nanowire sidewalls, resulting in the growth of pure InAs segments on top of GaAs.

Finally, in Chapter 7 I investigate how the mismatch strain distributes along the  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}/\text{GaAs}$  and InAs/GaAs nanowire interfaces, depending on the nanowire diameter and interface sharpness. To do so I use transmission electron microscopy coupled with geometrical phase analysis. It was observed that  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}/\text{GaAs}$  nanowires with diameters below 46 nanometers are free of misfit dislocations, regardless of the interface sharpness: the 6% strain is fully, elastically released within a strained region in the vicinity of the interface via crystalline planes bending close to the nanowire sidewalls. The results come in good agreement with the finite element simulations. These experimental findings confirm the prediction that heterointerfaces with a 6% lattice mismatch are pseudomorphic in axial nanowires with diameters below 50 nanometers. On the other hand, I find that 7% mismatched InAs/GaAs nanowires with diameters above 95 nanometers at the interface exhibit strain relaxation, both elastically and plastically, via plane bending and the formation of misfit dislocations, respectively. I observe an asymmetric distribution of the misfit dislocations across the interface and link it with the possible gliding of edge dislocations along the (0001) plane. I find moreover that misfit dislocations produce threading dislocations which exist on the nanowire sidewalls.

In conclusion, the experimental findings of my thesis establish a first step toward the realization of high quality InAs quantum dots in GaAs nanowires on silicon: a promising system for on-chip single photon emission. The last chapter also discusses future research directions and the perspectives opened by this work.

# Chapter 2

## General concepts

In the pioneering paper from 1964, silicon nanowires were called whiskers and had a diameter in a micrometer range. They were first realized by Wagner and Ellis [26] and have been studied by the scientific community for more than 50 years. The real increase in the number of publications on nanowire-related topics yet has occurred in the late 1990s with the development of size-selective single crystal nanowire synthesis along with advanced in-situ and ex-situ diagnostic methods. The diagnostic methods, particularly an ultrahigh-vacuum transmission electron microscope, allowed for a direct observation of fundamental processes during nanowire growth as well as a post-growth analysis of synthesized nanostructures.

Today, the field of nanowire application is extensive and includes nanowire electronics and optoelectronics [27, 28], nanowire biosensing [29], nanowire photonics [30, 31, 32], nanowire thermoelectricity [33] and nanowire quantum physics [34].

### 2.1 Nanowire growth methods

There are two categories of methods which are used to create nanowires: the top-down and the bottom-up approach. In the top-down approach, objects with desirable dimensions are obtained from bulk materials. For this, one defines a hard mask via lithography or nanoimprinting techniques before selective etching. One of the main advantages of this method is the ability to precisely control the size and position of nanowires on the substrate. However, the control over the position of quantum dots in such structures remains difficult. Indeed, nanowires are etched out of planar layers with spontaneously distributed, self-assembled quantum dots (these dots are formed due to strain, which arises from the difference in lattice parameters of the quantum dot material and the substrate material) and thus, the radial position of a single quantum dot is random in the final structure. In addition, multistage etching procedures make the top-down fabrication process very complex. Finally, the etching might introduce defects on the surface of nanowire heterostructures.

In the bottom-up approach, nanowire heterostructures are built from atoms and molecules. In this case, the position of a single monolayer can be precisely regulated allowing thus a full control over the imbedded quantum dots. Moreover, this approach opens up a world of possibilities for the creation of totally new structures, which cannot be obtained in a planar form (for example, direct band-gap GaP semiconductor materials [35], dislocation free, highly mismatched, GaAs/InAs heterostructures [36]). In the current manuscript, we concentrate our attention on the bottom-up nanowire heterostructures.

There are several methods to induce nanowire growth, which can be divided into particle-assisted and particle-free mechanisms. Among particle assisted methods of current importance is the vapor-liquid-solid mechanism, where liquid metal particles deposited onto a substrate act as catalyst of the nanowire growth. For example, when gold is involved in the growth process, the vapor-liquid-solid mechanism will be referred to as Au-assisted, when silver is involved - Ag-assisted and so on. For III-V materials the same group-III metal is often used to catalyze the growth (Ga for GaAs nanowires, for example). In this case, the metal droplets are formed on a substrate in the beginning of the growth process. In order to underline this fact, the mechanism is often referred to as self-assisted vapor-liquid-solid mechanism. This technique suppresses possible contamination by a foreign catalyst. Yet, the growth of self-catalyzed III-V nanowire heterostructures, in which the group III material is changed, is tricky. Indeed, different group-III elements have different growth conditions, which can lead to the consumption of the catalyst. Therefore, the Au-assisted vapor-liquid-solid mechanism remains as the most relevant process to date, owing to the versatility of materials which can be grown by this technique.

Particle-free mechanisms, such as selective area growth, are used as an alternative way to grow nanowires. No catalysts are needed in this case: nanowires are grown selectively on patterned substrates and thus are free from any kind of impurities from the catalyst. Yet complex procedures, namely lithography and wet chemical etching involved to pattern the substrate make this method very costly.

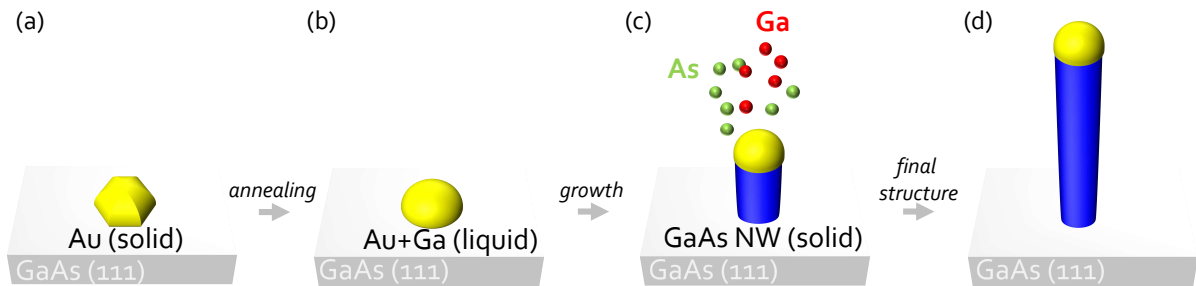
### **Au-assisted Vapor-Liquid-Solid mechanism**

Most nanowires and nanowire heterostructures grow by the vapor-liquid-solid mechanism by using gold (Au) nanoparticle catalysts distributed on a substrate. The growth of nanowires takes place below the liquid Au droplets but not on the bare substrate. The growth direction of nanowires is usually  $\langle 111 \rangle$ , which means that the crystal axis is perpendicular to the (111) substrate. The final diameter of the nanowires depends on the initial Au particle diameter. There are several ways to obtain Au on the substrate: electron-beam lithography patterning, in-situ Au thin film deposition and dewetting, and ex-situ Au colloids deposition from a solution. Each of the methods has its own advantages and drawbacks. The electron-beam lithography patterning allows to achieve ordered arrays of nanowires with uniform diameters and adjustable density. However, such substrate

## 2.1 Nanowire growth methods

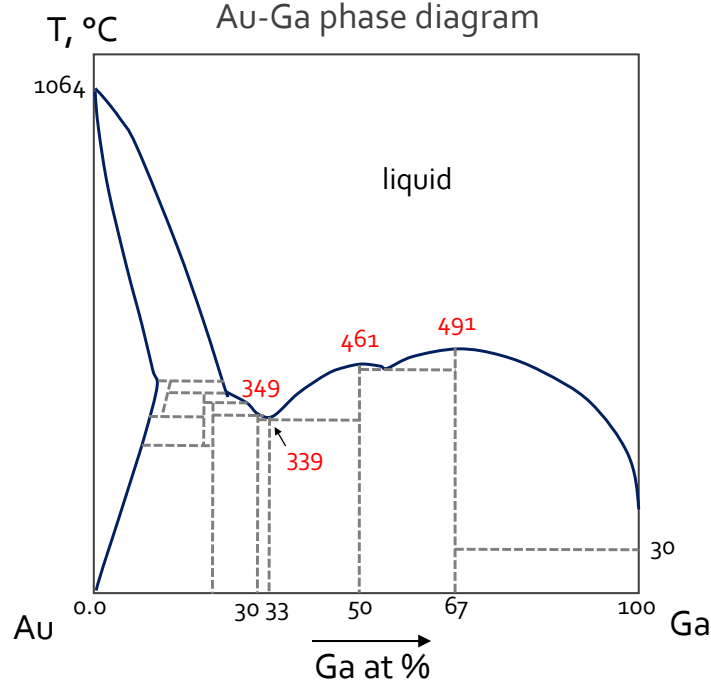
preparation procedures are time-consuming and costly. Therefore, the vast majority of research works, dedicated to the Au-assisted growth, use the other two methods, which are relatively simple and cost-effective. With in-situ Au thin film preparation, nanowires usually exhibit uniform density on the substrate, however a large variation in the nanowire diameter (20%-40%) is often observed. In the current project we dwell upon the ex-situ Au colloids deposition. With this method, the deviation in the diameters of nanowires is usually 3 times smaller than that for in-situ Au deposition [37].

Figure 2.1 shows a schematic of GaAs nanowire growth on a GaAs substrate by the Au-assisted vapor–liquid–solid mechanism. The growth can be roughly divided into four steps: 1) Au deposition, 2) substrate annealing, 3) material supply with subsequent crystal growth and 4) termination of the growth by cutting off supplied material fluxes. Once Au droplets are deposited onto the GaAs substrate, the substrate is annealed at the temperatures above the Au-Ga melting temperature. In this stage Ga from the substrate diffuses into the Au droplet and forms an Au+Ga alloy. For 30% of Ga in the Au-Ga solution, the melting temperature is  $\sim 349\text{ }^{\circ}\text{C}$  (see Figure 2.2). It is important to understand that the melting temperature of the Au+Ga alloy is much lower than that of Au (see phase diagram Figure 2.2). Therefore, at the typical growth temperatures which are  $560\text{--}610\text{ }^{\circ}\text{C}$ , the Au+Ga alloy is liquid.



**Figure 2.1:** Schematic representation of GaAs nanowire growth by the Au-assisted vapor–liquid–solid mechanism. a) Creation of Au droplets on a GaAs(111) substrate. b) Annealing of the substrate. c) Supply of Ga and As fluxes and initiation of the nanowire growth. d) Supplied materials are cut-off to terminate the nanowire growth process.

In the next step, the growth species (Ga and As) supplied in the vapor phase enter the liquid droplet. The supplied materials arrive into the droplet either by direct impingement from the vapor phase or by surface diffusion from the nearby surfaces. After a certain time, the droplet becomes supersaturated: the concentration of Ga and As in the droplet exceeds equilibrium concentration, and a GaAs crystal precipitates at the liquid–solid interface below the droplet. Thus, the lateral nanowire size is predefined by the Au droplet. Yet, several processes can modify the nanowire diameter during the growth (this will be discussed below). In summation, during nanowire formation three different phases are involved: a vapor phase (supplied materials), a liquid phase (droplet) and a solid phase (growing nanowire).



**Figure 2.2:** Au-Ga phase diagram adapted from [38]. Below 30 °C both Au and Ga are solid and are immiscible. The melting temperature of the Au-Ga alloy is 349 °C at a Ga concentration of 30%.

## Growth thermodynamics

During nanowire growth, the system, from a thermodynamic point of view, is far from its equilibrium state. In order to understand what promotes the phase transformation during nanowire precipitation, we first will define an "equilibrium state" for the system.

The system, which consists of vapor, liquid and solid phases, adopts its *equilibrium state* when the chemical potentials  $\mu$  of the three involved phases at a given pressure  $P$  and temperature  $T$  are equal to each other:

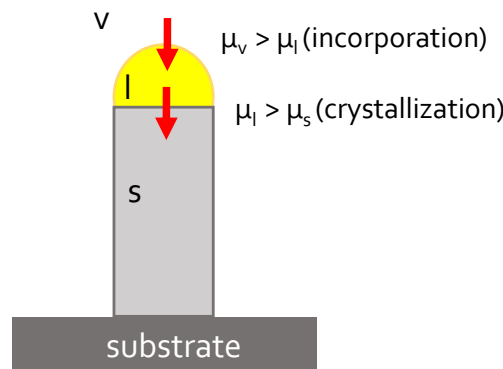
$$\mu_v(P,T) = \mu_l(P,T) = \mu_s(P,T). \quad (2.1)$$

The *chemical potential* of a phase represents changes in the Gibbs free energy  $G$  when the number of atoms in the phase is changed "by one":  $\mu = \frac{\partial G}{\partial n}$ .

During the growth, as we saw in the previous section, the semiconductor material undergoes two phase transformations, namely the vapor-liquid and the liquid-solid. This means that the chemical potentials of the three involved phases are no longer the same but follow the relation:

$$\mu_v(P,T) > \mu_l(P,T) > \mu_s(P,T). \quad (2.2)$$

The difference of the chemical potentials is the main driving force for the transfer of atoms between the phases and the consequent phase transformation (see Figure 2.3). Particularly, the first inequality  $\mu_v(P,T) > \mu_l(P,T)$  leads to the transfer of atoms from the vapor phase to the liquid droplet and thus is proportional to the incorporation rate. The second inequality  $\mu_l(P,T) > \mu_s(P,T)$  leads to the transfer of atoms from the liquid droplet to the solid nanowire and thus is generally proportional to the crystallization rate.



**Figure 2.3:** Schematic representation of the relationship between the chemical potentials of vapor, liquid and solid phases during the nanowire growth process. Adapted from [39].

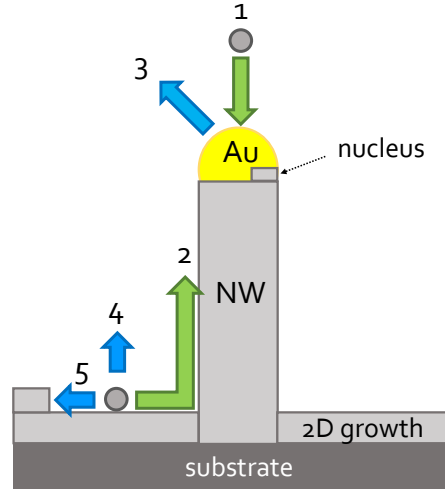
### Kinetic growth processes

In most cases, nanowires grow layer-by-layer and the growth is mediated by the formation of a two-dimensional nucleus. This was confirmed experimentally in-situ during the formation of GaAs nanowires grown by the vapor–liquid–solid mechanism in ultra-high vacuum transmission electron microscope [40].

Let us now consider in detail what kinetic processes govern nanowire growth (see Figure 2.4). The supplied materials arrive onto the growth substrate in vapor phase. For nucleus formation and the subsequent nanowire precipitation, the droplet has to be supersaturated with the supplied material. There are two ways for the material to reach the liquid droplet: the direct capture by the droplet surface and the diffusion of material from nearby surfaces to the droplet (green arrows on Figure 2.4). The supplied material can also be desorbed from the surfaces (processes 3, 4 Figure 2.4) or result in a two-dimensional growth on the substrate (process 5 Figure 2.4).

If the direct impingement of material into the droplet depends mostly on the supplied flux, the diffusion of adatoms<sup>1</sup> into the droplet strongly depends on the growth parameters. When the diffusion length of adatoms  $\lambda_f$  is much larger than the nanowire length  $L$ , all adatoms arrive into

<sup>1</sup>adsorbed atoms



**Figure 2.4:** Schematic illustration of kinetic processes occurring during nanowire growth. Adapted from [41]. The green arrows represent fluxes involved in the elongation of the nanowire and the blue arrows correspond to the desorption and two-dimensional nucleation on the substrate.

the nanowire tip and contribute to the axial growth. Conversely, when  $\lambda_f \ll L$  adatoms desorb from the surface or create a conformal layer on the sidewalls of the nanowire. Usually, high growth temperatures promote the desorption of adatoms. Moreover, vapor deposition growth techniques such as chemical vapor deposition result in very low diffusion lengths of adatoms. Therefore, depending on the growth conditions, we can distinguish two different growth mechanisms, namely the *adsorption-induced* mechanism (governed by process 1 Figure 2.4) and the *diffusion-induced* mechanism (governed by processes 1 and 2 Figure 2.4).

For the adsorption-induced growth mechanism, the nanowire growth rate generally increases with the nanowire radius. Moreover, the nanowire growth rate becomes zero at some minimum nanowire radius  $R_{min}$ . This phenomenon is attributed to the Gibbs-Thomson effect: the chemical potential of a droplet increases with its surface curvature. The smaller the droplet radius, the greater its chemical potential. At a certain droplet radius  $R_{min}$  the chemical potential of the droplet becomes comparable to the chemical potential of the substrate and the vapor. This leads to the disappearance of the transfer of atoms between phases and the nanowire growth is stopped.

In contrast, for the diffusion-induced growth mechanism, the nanowire growth rate decreases with the nanowire radius. In this case, the diffusion of adatoms from the substrate plays a major role. This regime is generally observed for nanowires with diameters at least below 100 nanometers [41]. The decreasing dependence can be derived from a simple consideration [42]. The direct flux of supplied material arrives directly to the droplet and thus is proportional to the droplet surface area ( $\propto R^2$ ). The diffusion flux of adatoms arrives to the nanowire top from the nanowire sidewalls and thus is proportional to the nanowire perimeter ( $\propto R$ ). The material is then incorporated into

the nanowire via the nanowire-particle interface ( $\propto R^2$ ). The nanowire growth rate is therefore given by:

$$\frac{dL}{dt} = c_1 + \frac{c_2}{R}, \quad (2.3)$$

where  $L$  is the nanowire length,  $t$  is the growth time,  $c_1$  and  $c_2$  are coefficients. The first term on the right side of the equation 2.3 is the contribution from the direct flux, while the second term is the contribution from the diffusion flux. The second term of the equation 2.3 is inversely proportional to the nanowire radius. Therefore, thin nanowires grow faster than the thick ones for the diffusion-induced growth mechanism.

The current manuscript is dedicated to Au-assisted III-V nanowire heterostructures grown by the high vacuum molecular beam epitaxy technique. In contrast to chemical vapor deposition, the molecular beam epitaxy growth provides very high values of the diffusion length of adatoms (a few micrometers, which is in the order of the typical nanowire length). This means that growth of nanowires will be driven by the diffusion-induced growth mechanism.

## 2.2 Crystal structure of III-V semiconductor nanowires

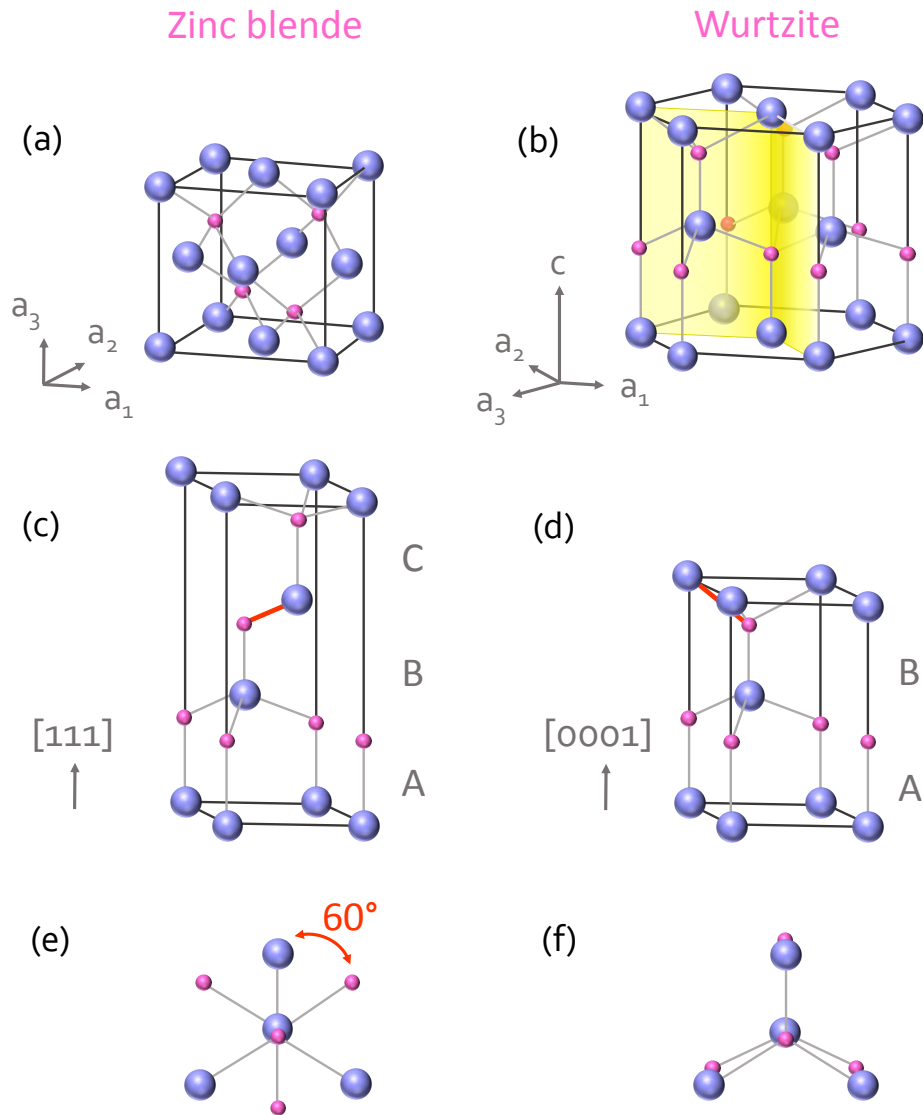
All III-V bulk semiconductor materials under ambient conditions, except for the group III nitrides, have a stable zinc blende crystal structure. In order to observe wurtzite crystal phase in III-V bulk materials one would have to apply an enormous pressure of several gigapascals (GPa) on the crystal [43]. Interestingly, in the case of semiconductor nanowires, pure zinc blende (see, for example, [44]), pure wurtzite (see, for example, [36]) and a mixture of the both crystal phases (see, for example, [40]) can be achieved.

### Zinc blende and wurtzite phases

Most III-V nanowires (with an exception for III-antimonide [45]) tend to adopt a wurtzite crystal structure. Yet, neither wurtzite nor zinc blende phase are unstable and often a disordered mixture of both crystal structures can be found along a nanowire length.

Since nanowires grow preferentially in the  $\langle 111 \rangle$  growth direction, the crystal phase mixing occurs in the same direction. Let us now consider in details the principal stacking differences of the wurtzite and the zinc blende phases. Figure 2.5 depicts cubic zinc blende and hexagonal wurtzite crystal phases. For the zinc blende crystal structure the unit cell is a face-centered cube (see Figure 2.5 a). Since all sides in the cube are equal, the zinc blende phase has only one lattice constant which is usually denoted as  $a$ . The wurtzite crystal structure forms a hexagon (see Figure 2.5 b) constructed by three unit cells. The unit cell of wurtzite is a straight parallelepiped with





**Figure 2.5:** Schematic illustration of zinc blende and wurtzite crystal structures. Two different colors (violet and pink) correspond to two different types of atoms (group III and group V). a) Cubic zinc blende unit cell. b) Hexagonal wurtzite crystal structure constructed by three unit cells. The yellow planes indicate boundaries for one of the three unit cells. Equivalent close-packed directions:  $\langle 111 \rangle$  for zinc blende (c) and  $\langle 0001 \rangle$  wurtzite (d). The difference in the fourth interatomic bond is marked with red color. Top view of the difference in the interatomic bond configuration for zinc blende (e) and wurtzite (f).

an equilateral rhombus at a base. Two lattice constants are thus necessary to define the wurtzite unit cell. In addition to  $a$  (which describes the rhombus sides), the lattice parameter  $c$  is used to describe the height of the unit cell.

The stacking sequence of wurtzite and zinc blende crystal structures along the close-packed

$\langle 111 \rangle$  direction<sup>2</sup> differs only in the position of the fourth interatomic bond (see Figure 2.5 c,d). The fourth interatomic bond of the zinc blende crystal phase is rotated by  $60^\circ$  compared to the second interatomic bond, whereas in the hexagonal wurtzite crystal phase the both bonds are aligned with each other (see Figure 2.5 e,f). This provides two types of layer stacking, being *..ABCABCA..* for the zinc blende phase and *..ABABABA..* for the wurtzite phase. Each letter A, B or C indicates one of the three possible lateral positions of the monolayer (ML). Any change in the position of the fourth interatomic bond during nanowire formation thus will lead to a switch between the crystal structures.

### Control of the nanowire crystal phase

Understanding the control of nanowire crystal phases during growth opens up great prospects for future devices. For example, stacking defects can act as scattering centers for carriers and hence lead to the degradation of the electronic properties of the final device. Indeed, Parkinson and co-authors demonstrated [46] that the carrier mobility of GaAs nanowires is strongly influenced by the density of stacking defects. Another work, demonstrating the influence of phase mixture on electronic properties of nanowires was performed by Thelander and coworkers [47]. The authors reported that long wurtzite segments in zinc blende InAs nanowires block the transport of carriers and the final nanowire resistivity is increased by two orders of magnitude. Therefore, the control over the phase purity in nanowires is of great importance for electron transport performances.

One additional motivation to control the crystal phase in nanowires is to access properties of a given material, that are not available in the bulk. For example, bulk GaP material has a zinc blende crystal structure and an indirect band gap. Assali with colleagues [35] demonstrated, however, that by growing GaP nanowires in wurtzite crystal structure the band gap becomes direct and a strong photoluminescence is observed.

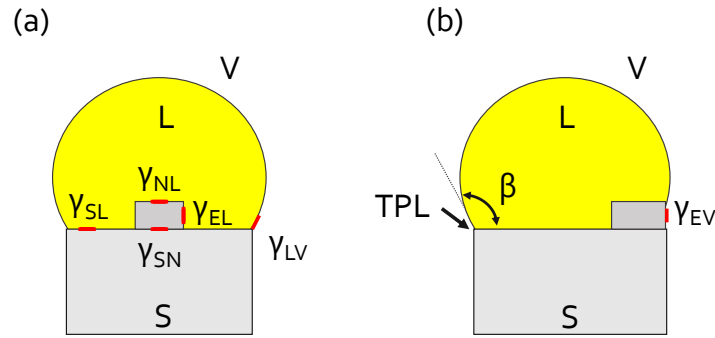
Moreover, changing on purpose the crystal phase, one can engineer crystal phase heterostructures in a single material nanowire. Indeed, wurtzite and zinc blende phases have different band structures [48] and usually exhibit type-II band alignment once combined [48]. This enables the realization of, for example, zinc blende quantum dots in a wurtzite InP nanowire [49]. Since only one semiconductor material is used, these quantum dots feature atomically abrupt interfaces. Therefore, the ability to tune the crystal structure of a nanowire in a reproducible way offers a great prospect for band structure engineering.

The driving force of phase selection during the nanowire growth is strongly correlated to the nucleation process at the droplet-nanowire interface [50]. For typical nanowire diameters ( $\sim 10$ -100 nanometers), the nucleation process is assumed to be mononuclear [51]: a nascent nucleus rapidly spreads at the nanowire growth front and fully covers it much before the second nucleation

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<sup>2</sup>direction having the minimum distance between atoms.

event can occur. Theoretically, the nucleus can form at the droplet-nanowire interface either somewhere away from the triple-phase line<sup>3</sup> (Figure 2.6 a) or at the triple-phase line (Figure 2.6 b). In the first case the nucleus is totally surrounded by the liquid phase, while for the second case the nucleus has an edge exposed to the vapor phase. It was demonstrated [50] that nucleation in the center will lead to the zinc blende phase formation while the wurtzite phase is more favorable when nucleation occurs at the triple-phase line. Let us now examine the parameters which are responsible for the wurtzite formation in nanowires, which make them different from their bulk counterparts.



**Figure 2.6:** Two different nucleation configurations. a) Nucleation in the center of the droplet-nanowire interface. b) Nucleation at the triple-phase line. Big letters V, L, S and N represent vapor, liquid, solid and nucleus, respectively. Surface energies nucleus-liquid  $\gamma_{NL}$ , solid-liquid  $\gamma_{SL}$ , solid-nucleus  $\gamma_{SN}$ , edge-liquid  $\gamma_{EL}$ , liquid-vapor  $\gamma_{LV}$ , edge-vapor  $\gamma_{EV}$  are indicated. Triple-phase line is denoted as TPL.  $\beta$  is the contact angle of the droplet.

The total surface energy  $\Gamma$  of the nucleus which is formed at the droplet-nanowire interface away from the triple-phase line (see Figure 2.6 a) can be expressed as:

$$\Gamma = \gamma_{EL}, \quad (2.4)$$

where  $\gamma_{EL}$  is the surface energy associated with the interfaces between the nucleus edge (E from edge) and the liquid droplet (L from liquid). For the nucleation at the triple-phase line (see Figure 2.6 b), however, the nucleus has to be shifted from the center to the droplet edge. This means that a fraction  $x$  of the nucleus surface will be replaced by the nucleus-vapor interface. The latter will eliminate part of the liquid-vapor interface. The total surface energy  $\Gamma$  of the nucleus, therefore, will be given as:

$$\Gamma = \gamma_{EL}(1 - x) + x(\gamma_{EV} - \gamma_{LV} \sin \beta), \quad (2.5)$$

<sup>3</sup>where vapor, liquid and solid phases coexist.

where  $\beta$  is the contact angle of the droplet. By comparing 2.4 and 2.5 the triple-phase nucleation (and thus, the wurtzite phase) is favorable when:

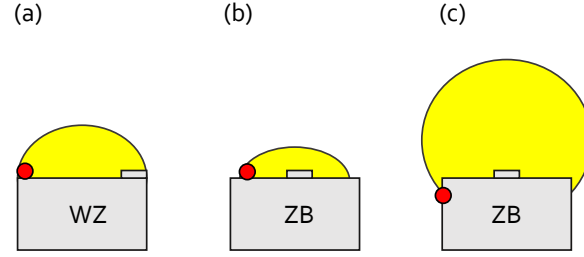
$$\gamma_{EV} - \gamma_{EL} - \gamma_{LV} \sin \beta < 0, \quad (2.6)$$

Conversely, when the left side of the equation 2.6 is larger than zero, nucleation occurs at the center of the droplet-nanowire interface and zinc blende phase is favorable. By examining the equation 2.6 it becomes clear that the contact angle of the droplet  $\beta$  plays an important role in the phase selection.

It was estimated in [50] that for Au-assisted GaAs nanowires  $\gamma_{EV} \sim \gamma_{EL}$ ,  $0.72 \leq \gamma_{LV} \leq 1.14 \text{ Jm}^{-2}$  and, therefore, the left side of the equation 2.6 will have its minimum value at  $\beta = 90^\circ$ . At this angle the triple-phase nucleation and, thus, the wurtzite phase, is the most probable. On the other hand, when  $\beta$  is very different from  $90^\circ$ ,  $\sin \beta$  is small and the zinc blend phase is more favorable. Similar results were reported in [52, 53, 54, 55]. For example, Rieger and his colleagues observed that the wurtzite segment can be created in zinc blende Ga-assisted GaAs nanowires when the contact angle of Ga droplets is decreased from  $137^\circ$  down to  $90^\circ$  [52]. The authors used a Ga interruption technique in order to partially consume the liquid Ga droplet and therefore decrease its contact angle on top of GaAs nanowires. Similar results were obtained in the work of Munshi and coauthors [53], where Ga-assisted GaAs nanowires were grown by means of molecular beam epitaxy. The authors noted that the insertion of a GaAsSb segment on top of zinc blende GaAs nanowires decreases the contact angle of the Ga droplet from  $130^\circ$  to  $90^\circ$ . If the GaAs segment is regrown again on top of GaAsSb, the GaAs segment has wurtzite crystal structure and the contact angle of the droplet remains in the range between  $90^\circ$  and  $115^\circ$ .

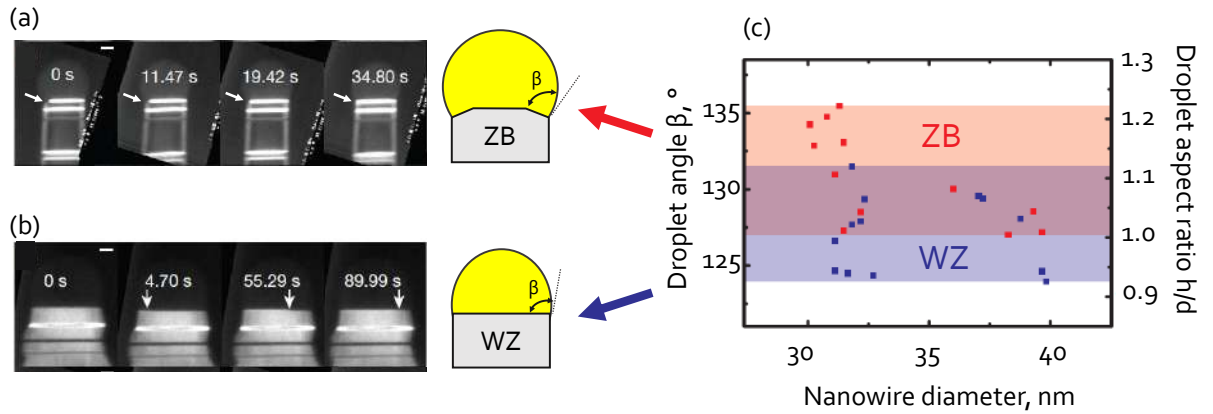
Krogstrup et al. [55] also proposed that the nanowire phase selection directly correlates with the volume and contact angle of the catalyst droplet and, hence, with its shape. For a small droplet, the triple phase line will withdraw along the nanowires top facet (Figure 2.7 b). For a large droplet, it will shift to the nanowire sidewall (Figure 2.7 c). This will lead to the formation of a nucleus at the center of the droplet/nanowire interface (away from the triple phase line) promoting zinc blende crystal structure. By varying the Ga droplet size, Yu and coworkers [56] managed to demonstrate the controlled growth of zinc blende/defect-section and wurtzite/defect-section Ga-assisted nanowire superlattices.

Moreover, recently it has been experimentally confirmed in-situ that the droplet geometry is responsible for the nanowire crystal phase selection [40]. The V/III flux ratio was found to be the main parameter that controls the droplet geometry. The growth of Au-GaAs NWs was performed in ultra-high vacuum transmission electron microscope (UHVTEM). It was observed that the wurtzite phase forms when the droplet contact angle does not exceed a certain value ( $< 132^\circ$ ). Moreover, the droplet/nanowire interface is always planar for wurtzite and the layer-by-layer



**Figure 2.7:** Schematic representation of the effect of the droplet shape on the crystal structure of the nanowire. The position of the triple phase line in each case is marked with a red dot.

growth proceeds slowly (see Figure 2.8 b). Conversely, for the zinc blende phase formation, the droplet contact angle is large ( $> 127^\circ$ ). Besides, theoretical calculations given in the paper, predict that zinc blende crystal structure will be favorable when the contact angles are extremely small ( $< 60^\circ$ ). However, such contact angles are not achievable experimentally in UHVTEM. The droplet/nanowire interface is no longer planar, but has a truncated facet during zinc blende formation (see Figure 2.8 a). The size of truncation depends on the droplet supersaturation and is increased at low supersaturations. The growth of zinc blende crystals happens more rapidly than in the wurtzite case.

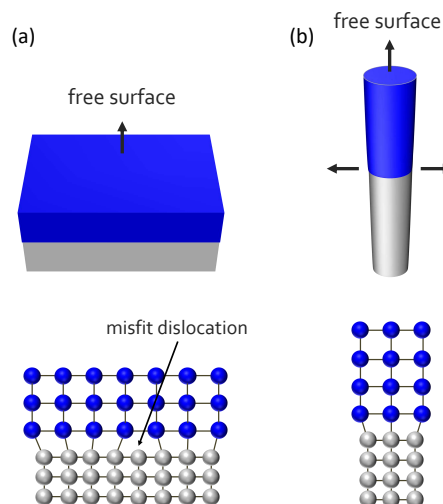


**Figure 2.8:** Dynamics of the crystal phase selection in Au-GaAs nanowires grown in UHVTEM. Adapted from [40]. Set of dark-field images (10 nm scale bar), extracted from a recorded in situ movie, which reveal the formation of zinc blende (a) and wurtzite (b) crystal phases. White arrows indicate the droplet/nanowire interface, which is truncated for (a) and is planar for (b). Once nucleus is formed at the interface, it takes about 0.5 min (a) and 1.5 min (b) to complete it. c) Experimental results on phase selection at different droplet geometry. Points indicate switch from wurtzite to zinc blende (red) and from zinc blende to wurtzite (blue). Distinct areas where only wurtzite (blue shading,  $\beta < 127^\circ$ ) and only zinc blende (pink shading,  $\beta > 132^\circ$ ) are visible. Aspect ratio  $h/d$  is a ratio of droplet height  $h$  to the nanowire diameter at the interface  $d$ .

The theoretical considerations and experimental examples discussed above show that the catalyst droplet geometry (namely, its volume and contact angle) plays a significant role in crystal structure selection for particle-assisted nanowires. By adjusting carefully the growth parameters such as V/III beam equivalent pressure ratio, it is possible to engineer the crystal phases in a nanowire.

## 2.3 Nanowire heterostructures

For the fabrication of advanced electronic and optoelectronic devices it is often necessary to assemble different semiconductor materials with different band gaps and, thus, to create heterostructures. In most cases lattice parameters of the involved semiconductor materials differ from each other, thus causing strain at the interface where materials are joined. In thin film epitaxy, the combination of mismatched materials results in extremely poor quality of heterointerfaces with high density of misfit dislocations (Figure 2.9). The dislocations act as non-radiative recombination centers and thus must be avoided. Nanowires can overcome the strain issue owing to their small lateral size and high aspect ratio. Indeed, nanowires have free (not constrained) surfaces on their sidewalls where the strain caused by the mismatch can be elastically released by lateral expansion (Figure 2.9). For example, dislocation free interfaces were achieved in various nanowire heterostructures such as Si/SiGe with lattice mismatch of 0.17% [57], GaP/GaAs<sub>0.75</sub>P<sub>0.25</sub> with lattice mismatch of 0.9% [58], InAs/InP with lattice mismatch of 3% [59], InAs/GaAs with lattice mismatch of about 7% [60], InP/InAs with lattice mismatch of 10.5% [61].

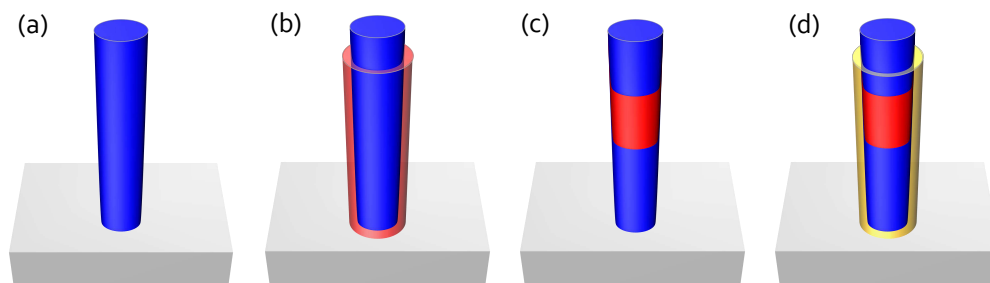


**Figure 2.9:** Schematic illustration of the principal difference between two-dimensional (a) and nanowire (b) geometries for epitaxy of mismatched materials.

## Growth of axial and radial heterostructures

Two kinds of nanowire heterostructures can be formed: axial heterojunctions along the nanowire growth direction, and radial or core/shell heterojunctions where semiconductor materials are grown around a core nanowire. Anisotropic growth of axial heterostructures is promoted by the catalyst droplet (see 2.1). Conversely, to create radial heterostructures, conformal two dimensional growth on the nanowire sidewalls must be fostered at the expense of the axial growth. For the metal-organic chemical vapor deposition, axial nanowire growth is inhibited at higher growth temperatures and/or increased reactant concentration in the vapor phase. In the molecular beam epitaxy, this regime is usually achieved at low growth temperatures and a low V/III beam equivalent pressure ratio is necessary for that.

Figure 2.10 shows examples of different nanowire heterostructures. Probably, the most common nanowire heterostructure is obtained when the substrate material differs from that of the nanowire (2.10 a). Often III-V nanowires are grown on silicon substrates to potentially reduce production costs. Another motivation to use silicon wafers is the possibility to integrate future III-V nanowire-based devices with standardized CMOS process. Radial nanowire heterostructures are called core-shell (Figure (2.10 b). The inner material is referred to as the core, and the surrounding layers are referred to as the shell. This configuration allows, for example, to passivate the nanowire core [62], to grow radial p-n junctions for photovoltaic applications [63], to form nanowire waveguide by growing tailored shells [13]. Yet the growth of high quality, lattice mismatched, epitaxial layers in the radial direction is not an easy task since nanowires have a large surface area. Theoretical calculations [64] predict that the critical thickness of an InAs shell grown around a GaAs core with more than 10 nm diameter is 0.6 nm (the same as in the planar two dimensional epitaxy). An example of axial nanowire heterostructures is shown in Figure 2.10 c. In such structures, materials are placed along the nanowire axis. The interface between the two mismatched materials is thereby minimized compared to core-shell heterostructures. Figure 2.10 d shows a hybrid axial-radial structure.



**Figure 2.10:** Schematic illustration of different nanowire heterostructure configurations. a) Nanowire-substrate, b) radial (core/shell), c) axial and d) axial-radial nanowire heterostructure.

## Elastic properties

As we already discussed, strain originated at the interface between mismatched materials in nanowire heterostructures can be elastically released on the nanowire sidewalls. The lattice mismatch between the materials is given, by<sup>4</sup>:

$$\frac{\Delta a}{a} = \frac{a_L - a_S}{a_S}, \quad (2.7)$$

where  $a_S$  and  $a_L$  are lattice parameters of the substrate and the grown layer, respectively. If the lattice parameter of the substrate is smaller than the lattice parameter of the grown layer, a compressive strain ( $\varepsilon < 0$ ) will be observed in the layer. If, on the contrary, the lattice parameter of the substrate is greater than the lattice parameter of the grown layer, a tensile strain ( $\varepsilon > 0$ ) will be present in the layer.

In order to describe the strain effects in nanowire heterostructures, elastic continuum theory is used [65]. The displacement of a lattice cell at the heterointerface can be described by a local displacement vector  $\vec{u}(r)$ :

$$\vec{u}(r) = \vec{R} - \vec{r}, \quad (2.8)$$

where  $\vec{r}$  is the vector which describes the initial position of the lattice cell with coordinates  $x_i$  and  $\vec{R}$  is the final vector of the displaced body with coordinates  $x'_i$ . The resulting strain caused by the deformation is described by a strain tensor  $\varepsilon_{ij}$ :

$$\varepsilon_{ij} = \frac{1}{2} \left[ \frac{\partial u_i}{\partial x_j} + \frac{\partial u_j}{\partial x_i} \right], \quad (2.9)$$

where quadratic terms are ignored in the case of small deformations.  $\varepsilon_{xx}$ ,  $\varepsilon_{yy}$  and  $\varepsilon_{zz}$  components of strain tensor represent uniaxial strain along the axes x, y and z, respectively. The sum of  $\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}$  gives the relative change in volume of the deformed cell and is called the hydrostatic strain  $\varepsilon_{hy}$ . Components  $\varepsilon_{ij}$  with  $i \neq j$  denote a shear strain which acts tangentially. Note that the strain tensor  $\varepsilon_{ij}$  is symmetric and has only 6 out of 9 independent components. This allows a shortened representation of the strain tensor in form of a  $6 \times 1$  matrix (Voigt notation, see Appendix A).

The deformation gives rise to internal forces which tend to return the deformed body to its equilibrium state. These internal forces are described by a stress tensor  $\sigma_{ij}$ :

$$\sigma_{ij} = C_{ijkl} \varepsilon_{kl}, \quad (2.10)$$

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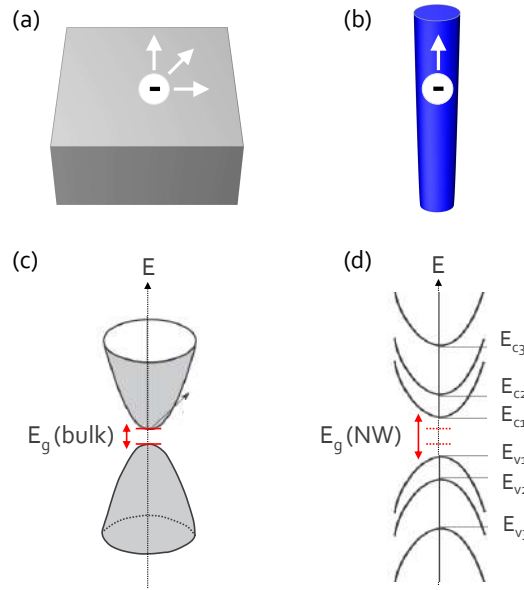
<sup>4</sup>Most often in the literature, the mismatch  $\Delta a/a$  is given in percentage



where  $C_{ijkl}$  is the stiffness tensor composed of elastic constants. The equation 2.10 is a Hooke's law for the three dimensional case. The symmetric, third-order stress tensor  $\sigma_{ij}$  is often represented in form of a  $6 \times 1$  matrix, similarly to the strain tensor (see Appendix A). The values of elastic constants for wurtzite GaAs and wurtzite InAs materials, which were used for this thesis, are also listed in the Appendix A.

## Electronic band structure

The band structure of nanowires differs from that of the bulk materials (see Figure 2.11). Indeed, thanks to the one-dimensional geometry of nanowires, carriers are free to travel only along the nanowire axis and are spatially confined across the nanowire (Figure 2.11 b). The lateral confinement widens up the energy band gap compared to the unconfined three-dimensional case (Figure 2.11 c,d). If a nanowire heterostructure is considered, the strain which is generated at the interface between mismatched materials, affects the energy of the electronic bands as well.



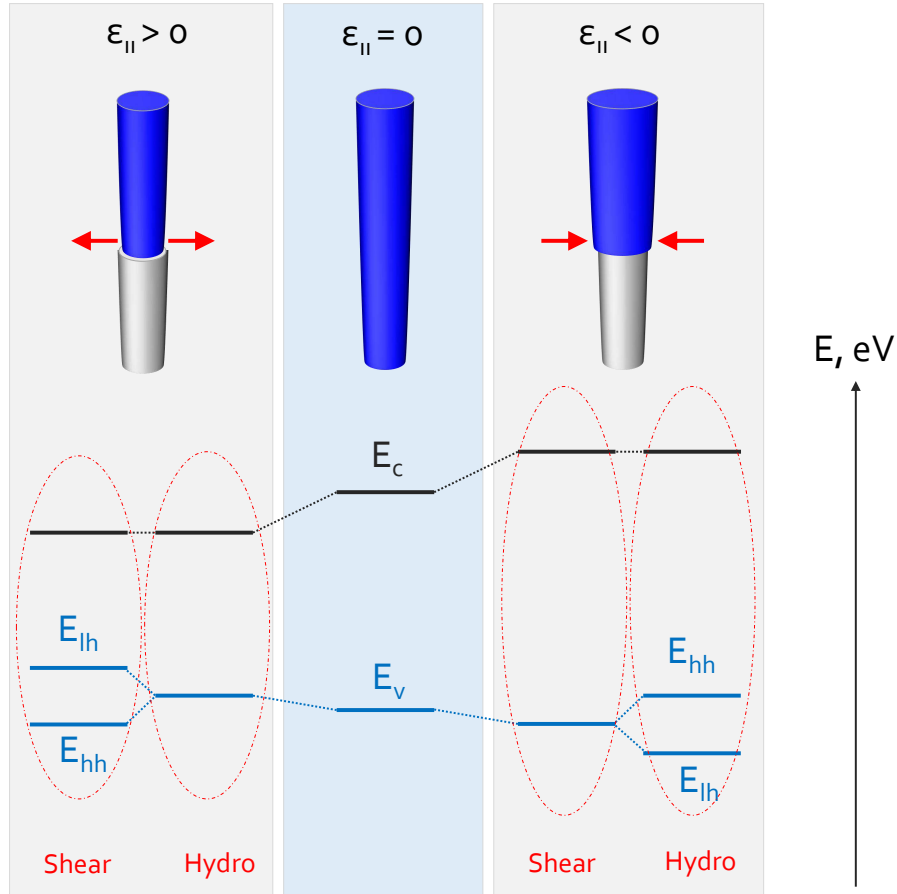
**Figure 2.11:** The main difference in the band gap structure for a bulk material (a,c) and a nanowire (b,d) in zinc blende. The band gap energy of bulk and nanowire is  $E_g(bulk)$  and  $E_g(NW)$ , respectively. Quantized levels formed in a nanowire due to spatial confinement are denoted as  $E_{c1}$ ,  $E_{c2}$ .. for the conduction band and  $E_{v1}$ ,  $E_{v2}$ .. for the valence band.

The band gap energy of a nanowire  $E_g(NW)$  can be expressed, as:

$$E_g(NW) = E_g(bulk) + E_{conf} - E_{coulomb}. \quad (2.11)$$

### 2.3 Nanowire heterostructures

The first term in the right hand side of Equation 2.11,  $E_g(bulk)$ , represents the band gap energy of bulk materials, which is characteristic of the material. The second term of the equation,  $E_{conf}$ , describes the additional energy due to quantum confinement. It scales with the radius of the nanowire as  $R^{-2}$  and hence increases with the nanowire radius decrease. The last subtractive term,  $E_{coulomb}$ , represents the energy of an exciton, which is formed due to the electrostatic attractive force between electron and hole in a nanowire.



**Figure 2.12:** Difference in the band gap structure for the strained nanowire heterostructures as compared to the unstrained nanowire.  $E_c$  and  $E_v$  represent conduction and valence bands,  $E_{hh}$  and  $E_{lh}$  denote heavy-hole and light-hole valence bands.

In a nanowire heterostructure, the material strain which is caused by the mismatch at the heterointerface induces further modification of the bandgap energy. To illustrate this effect, we consider as an example the impact of a bi-axial strain field on a zinc blende semiconductor. We note  $\perp$  the 111 direction, which corresponds to the wire axis, and  $\parallel$  an in-plane direction. This strain field features an hydrostatic component  $\varepsilon_h = \varepsilon_{\perp} + 2\varepsilon_{\parallel}$  and a bi-axial shear strain component given by  $\varepsilon_{sh} = 2(\varepsilon_{\perp} - \varepsilon_{\parallel})$ . The conduction band is only affected by the hydrostatic component,

and the associated energy shift reads:

$$\Delta E_c = a_c \varepsilon_h, \quad (2.12)$$

with  $a_c < 0$  the hydrostatic deformation potential of the conduction band. The case of the valence band is more complex. We restrict the discussion to the heavy-hole ( $hh$ ) and light-hole ( $lh$ ) bands. For simplicity, we also neglect the coupling between the light-hole and split-off bands. In these conditions, the energy shifts of the  $hh$  and  $lh$  bands induced by strain read:

$$\begin{aligned} \Delta E_{v,hh} &= a_v \varepsilon_h - \frac{d}{2\sqrt{3}} \varepsilon_{sh} \\ \Delta E_{v,lh} &= a_v \varepsilon_h + \frac{d}{2\sqrt{3}} \varepsilon_{sh}. \end{aligned} \quad (2.13)$$

Here,  $a_v > 0$  is the hydrostatic deformation potential of the valence band. Note that the deformation potential  $d < 0$  corresponds to one defined in the usual cubic deformation basis spanned by the crystal directions  $\{(100), (010), (001)\}$ .

Changes in the band structure alignment due to strain are presented in Figure 2.12. In case of compressive strain in the layer ( $\varepsilon_{||} < 0$ ), the hydrostatic component of strain will shift the conduction band edge upward and the valence band downward along the energy axis, leading to an increase in the band gap. The shear component of strain shifts the heavy holes upward and the light holes downward along the energy axis. For the case of tensile strain ( $\varepsilon_{||} > 0$ ), the hydrostatic component of strain will shift the conduction band edge downward and the valence band upward along the energy axis, leading thus to a decrease in the band gap. It is important to note that the valence band ground state is changed from heavy hole in case of compressive strain to the light hole in the other case.

## Challenges

Axial nanowire heterostructures are ideal building blocks for the realization of quantum dots. However, several important issues still limit the full implementation of nanowires. Despite the fact that nanowire geometry allows strain, caused by the mismatch, to more easily accommodate on the free side surfaces compared to thin film epitaxy, misfit dislocations can still be found at the material interfaces, if the diameter of the nanowire heterostructure exceeds a critical value. Moreover, problems such as kinking in one of the two interface directions, graded and asymmetric interfaces, and radial overgrowth arise during particle-assisted axial nanowire growth. The listed problems are crucial, especially when thin barriers or optically efficient quantum dots have to be produced. Let us focus on each of these problems in detail.

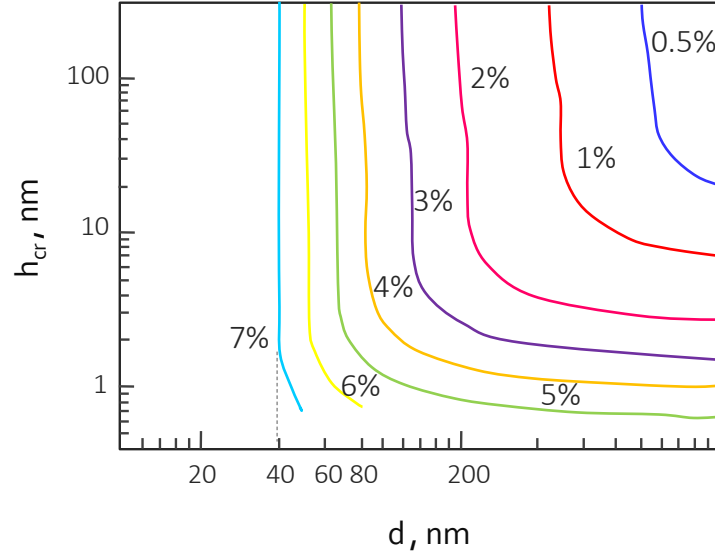
### *Dislocations:*

Usually materials which have to be combined in a nanowire heterostructure have different lattice parameters. The lattice mismatch causes strain at the interface where materials are joined together. If the final nanowire heterostructure has continuous change in the lattice spacing across the interface, the strain is released *elastically*. Conversely, strain is released *plastically* if networks of misfit dislocations are formed at the interface. The dislocations permit discontinuities of the lattice spacing. The strain in this case is accumulated around dislocation cores.

Larsson and coworkers demonstrated that strain is effectively elastically released in the vicinity of the interface in InAs/InP nanowire heterostructures with lattice mismatch of 3% [59]. The length of the strained area at the interface was found to be 10 nanometers for nanowires with diameters of 20 nanometers. Another example of elastic strain relaxation in nanowire heterostructures was reported by Ercolani and his colleagues [66]. The authors grew and investigated InAs/InSb axial nanowires with 7% lattice mismatch. It was observed, that the strain is fully elastically relaxed within 20-30 nanometers of the interface for nanowires with diameters of about 50 nanometers. On the other hand, de la Mata and coauthors [67] reported that InAs/InSb nanowire heterostructures exhibit relaxation of strain both elastically and plastically via partial formation of misfit dislocations. The diameter of studied nanowires is 35 nanometers at the interface, the final strain is found to be 5.5% and is released within 4 nanometers. Moreover, the authors presented strain studies for GaAs/GaSb nanowire heterostructures with 7.8% lattice mismatch. Again it is observed that the strain is released both elastically (by plane bending at one side of the studied nanowire) and plastically via formation of networks of dislocations at the interface. The nanowire is about 55 nanometers in diameter. Partially plastic relaxation of strain was also observed by Frigeri and coworkers in 65 nanometers in diameter GaAs/InAs nanowire heterostructures with 7.1% lattice mismatch [68]. The authors noted that the average distance between misfit dislocations increases from the center of the interface to the nanowire sidewalls. The latter revealed that the strain was partially relaxed via lateral expansion of the nanowire. The listed works represent experimental evidences of strain relaxation in nanowire heterostructures. However, in order to understand which factors influence the mode of strain relaxation (whether elastic or plastic) a theoretical model has to be formulated.

Theoretical calculation of the critical thickness  $h_{cr}$  for misfit dislocation formation depending on the nanowire diameter  $d$  and the lattice mismatch  $\Delta a/a$  was done by Frank Glas in [14]. An adapted graph of the critical thickness as a function of nanowire diameter is presented in Figure 2.13. For a given lattice mismatch there is a critical diameter  $d_{cr}$  below which infinitely long nanowires with dislocation free interfaces can be grown (to the left from the vertical asymptotes). For example, the growth of dislocations free highly mismatched GaAs/InAs nanowire heterostructures with  $\Delta a/a \sim 7\%$  is theoretically possible for diameters below 40 nanometers. Conversely, if the nanowire diameter exceeds the critical value (to the right from the vertical asymptotes), strain will relax plastically via formation of misfit dislocations. Obviously, the larger the lattice mismatch,

the smaller the critical diameter. The horizontal asymptotes show the critical thickness which would correspond to the growth of dislocations free two-dimensional layers ( $d$  tends to infinity).

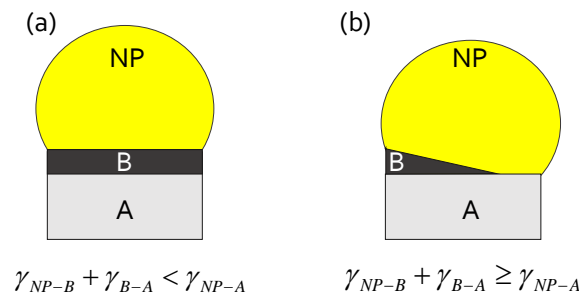


**Figure 2.13:** Dependence of the critical thickness  $h_{cr}$  on the nanowire diameter  $d$  for different lattice mismatch  $\Delta a/a$  given in %. Adapted from [14]. Vertical asymptotes correspond to the critical diameter  $d_{cr}$ , horizontal asymptotes correspond to the critical thickness for two-dimensional layers. For the GaAs/InAs materials with  $\Delta a/a \sim 7\%$   $d_{cr} \sim 40$  nm.

It is expected that the value of the critical diameter for the heterointerface nanowire/substrate is smaller than for the same material combination within a nanowire. Indeed, the substrate does not have free surfaces and thus there is no possible lateral relaxation. It is especially important when III-V nanowire compound semiconductors are integrated on Si(111) substrates. Several experimental works on the growth of III-V nanowires on different mismatched substrates have been done. In the work of Cirilín and coworkers [69] for GaAs nanowires grown on Si with 4.1% lattice mismatch the critical diameter is found to be 110 nanometers. The authors state that above the critical diameter nanowires do not grow at all or bend due to dislocations. On the other hand, Tomioka and his colleagues [70] observed dislocation centers at the interface between GaAs nanowires with diameters of 103 nanometers and a Si substrate. In this work, high resolution transmission electron microscopy analysis was used to determine the quality of the interfaces. GaAs nanowires with dislocations free interfaces on Si substrates were found for 20 nanometer diameters. However, the information about interface quality of GaAs nanowires with diameters between 20 and 103 nanometers is missing in this paper. Given that the critical diameter for the Si/GaAs axial nanowire interface is approximately 80 nanometers (calculations of Glas [14], Figure 2.13), this value should be even smaller for the nanowire/substrate interface.

### Kinking:

Axial growth of particle-seeded nanowires is determined by the position of the catalyst on top of a nanowire. However, the droplet position is very sensitive to the growth conditions. Any instabilities in the latter will lead to the kinking of the droplet and hence the final nanowire will not be straight. Moreover, differences in surface energies of the semiconductor materials has been shown to play an important role in the droplet position. It has been demonstrated that the growth of straight, Au-assisted, axial nanowire heterostructures is usually observed for one of the two interface directions [71]. For example, nanowires are straight for the growth of GaAs on top of InAs (GaAs-on-InAs) while InAs-on-GaAs nanowires kink [72, 73, 74]. The discrepancy of the two interfaces was explained in [71]. A schematic of the proposed model is shown in Figure 2.14. Two different semiconductor materials have different surface energies<sup>5</sup>. If the surface energy of the layer B/droplet interface is greater than the one associated with the layer A/droplet interface, the system will tend to minimize the surface area of the layer B. The clustering of the layer B will occur (Figure 2.14 b). At the same time the liquid droplet will prefer to stay in contact with layer A. Eventually, the position of the liquid droplet will be shifted from the top nanowire facet to the nanowire sidewall thus leading to kinking. This surface energy difference is a major obstacle for the growth of multilayer nanowire heterostructures.



**Figure 2.14:** Schematic illustration of the model proposed in [71]. The model explains the kinked morphology for one of the two interface directions in axial Au-assisted nanowire heterostructures. Inequalities below each figure correspond to the (a) layer-by-layer growth and straight nanowires and (b) island growth and kinked nanowires. Letters A, B and NP represent layer A, layer B and the liquid nanoparticle, respectively. The surface energies are: layer A at the interface with liquid nanoparticle  $\gamma_{A-NP}$ , layer A at the interface with layer B  $\gamma_{A-B}$ , layer B with the interface with liquid nanoparticle  $\gamma_{B-NP}$ .

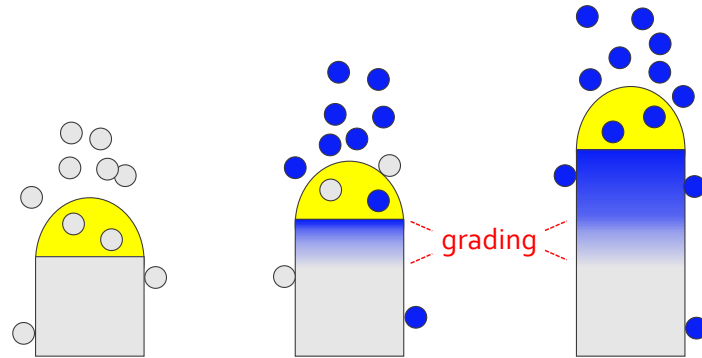
Yet, the surface energies of the involved materials at the interface with the liquid droplet are not constant during nanowire growth and may be changed by careful tuning of growth parameters. Therefore, the straight axial growth of nanowire heterostructures can be potentially achieved in the both interface directions. For example, Messing and coworkers demonstrated that the

<sup>5</sup>energy which is needed to break intermolecular bonds to create a new surface

surface energies of the nanowire layers with the liquid droplet can be changed by tuning the crystal structure of the segments [74]. The authors achieved straight "energetically unfavorable" InAs-on-GaAs nanowire heterostructures with a vertical yield of 65% when the InAs segment was crystallized in wurtzite. Another way to modify the surface energies and to promote the straight growth of Au-assisted nanowire heterostructures was reported by Zannier and her colleagues both for InAs-on-GaAs [75] and InP-on-InAs [76] interfaces. It was found that straight axial nanowire heterostructures are promoted at high III-to-Au ratios. This leads to the large contact angles of the liquid droplet and maintains its stability.

### ***Interface grading:***

Another challenge unique to the particle-seeded nanowire systems, especially important for Au-assisted nanowire growth, is interface grading. This effect is also known as the "reservoir effect" and is attributed to the solubility of growth species in the liquid droplet [77]. A simple schematic of the effect is shown in Figure 2.15. During vapor-liquid-solid growth of nanowires there is always some amount of semiconductor material stored in the liquid droplet. Therefore, even if the supplied materials are abruptly switched to grow a heterostructure, the material, accumulated in the liquid droplet from the growth of the first layer, will still continue to incorporate in the new segment leading to a graded interface. Additionally, different materials have different affinities for the liquid droplet. Therefore, the interface grading is often not symmetric and is more pronounced for one of the two interface directions.



**Figure 2.15:** Schematic illustration of interface grading for particle-seeded nanowire heterostructures. Adapted from [78]. The liquid droplet and the two different semiconductor materials are depicted in yellow, gray and blue, respectively.

Generally, the length of the graded interface  $L$  depends on the nanowire radius  $R$ . It is expected that the smaller the diameter, the sharper the interface [79]. Indeed, the amount of residual material accumulated in the Au droplet is proportional to its volume ( $\propto R^3$ ). This material enters

the nanowire through the nanowire-droplet interface ( $\propto R^2$ ). The length of the graded interface, thus, will scale linearly with the nanowire radius:  $L \propto R$ .

Several strategies to improve the abruptness of the interface have been proposed. For example, growth interrupts were implemented in [80], where self-catalyzed GaP/GaAs nanowire heterostructures were grown by means of molecular beam epitaxy technique. It was demonstrated that the length of the interface between GaP and GaAs segments is decreased from 15 to 2 monolayers when small diameters and the 60 second interruption of all fluxes are used. Similar growth interrupts procedure can be implemented in Au-catalyzed nanowires where the group-III elements are switched [25, 81]. In this case, the interruption of the group-III flux takes place while the group-V flux is maintained. As such, the group-V flux promotes the precipitation of the group-III material accumulated in the liquid droplet. Yet it should be noted that the interruption time is limited since a prolonged group-V exposure destabilizes the liquid droplet at the nanowire top [40].

Another way to increase the interface abruptness was proposed by Dick and coauthors [60] for the Au-assisted GaAs-on-InAs nanowire heterostructures. It was observed that the solubility of In in the Au droplet can be decreased by the introduction of short Ga pulses. The interface sharpness, moreover, can be further improved by increasing the number of Ga pulses (5 and 20 pulses were tested). The amount of Ga, introduced to the droplet by pulses, should be small enough to not initiate the GaAs growth before all the accumulated In is expelled.

Another solution to avoid interface grading was demonstrated in the work [82] for the self-catalyzed GaAs/InAs nanowire heterostructures. For this first Ga-assisted GaAs nanowires were grown and then the Ga-droplet was fully consumed under an appropriate growth conditions. This led to a flat top facet free of Ga. Afterward, InAs segments on top of GaAs stems were created by a separate supply of In and As fluxes. This technique allowed of the creation of atomically sharp interfaces for axial InAs-on-GaAs nanowires. Moreover, the radial overgrowth of InAs around GaAs (another common problem for axial InAs/GaAs nanowires) is avoided with this approach. However, it still remains unclear whether the formation of long InAs segments (longer than 20 nm) with dislocation-free interfaces is possible with this technique.

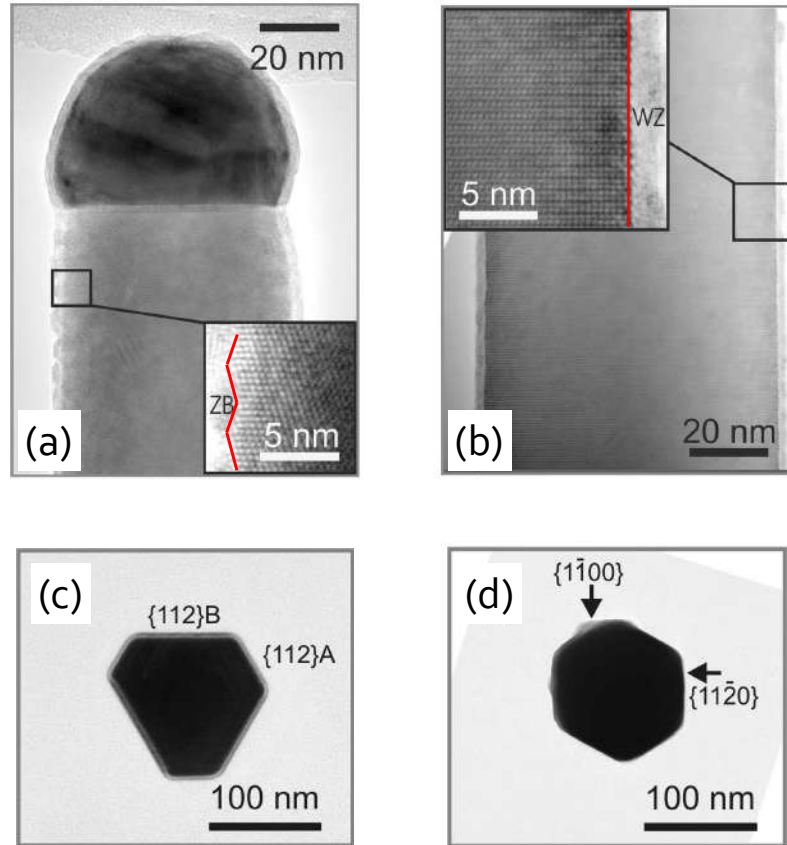
#### ***Radial overgrowth:***

An additional problem, which is often observed for axial nanowire heterostructures, is parasitic conformal growth on the nanowire sidewalls. Since the vapor-liquid-solid growth of nanowires is promoted simultaneously by direct flux of supplied materials and diffusion flux of adatoms from the substrate, there is always a possibility that an adatom will be trapped on the nanowire sidewall leading to an unintentional radial overgrowth. Such radial layers are source of additional strain, carrier instabilities and leakage in axial nanowire heterostructures.

A careful tuning of the available growth parameters has been shown to efficiently inhibit the



radial overgrowth for GaN/AlN nanowire superlattices [83]. An increase of the growth temperature from 765 °C up to 780 °C led to the complete suppression of the parasitic AlN overgrowth. Yet such high growth temperatures are not applicable for the growth of III-As nanowires. One of the possible solutions to suppress the parasitic radial growth can be seen in the crystal structure tuning. It was reported that InAs overgrowth for InAs-on-GaAs nanowire heterostructures is more pronounced when the GaAs segment exhibits zinc blende crystal structure [74]. Another example of significant InAs lateral overgrowth around zinc blende GaAs nanowires was observed by Huang and his colleagues [84]. Indeed, the zinc blende crystal phase has  $\{112\}$ -like side facets which usually promote tilted  $\{111\}$  microfacets (Figure 2.16) [50, 85]. The microfacets act as additional traps for the diffusion of adatoms. On the contrary, nanowires in the wurtzite crystal phase have straight  $\{1010\}$  type side facets and thus are more likely to promote the axial selectivity.



**Figure 2.16:** Different nature of side facets for wurtzite and zinc blende crystal structures. Adapted from [85]. InAs nanowires with pure zinc blende a) and pure wurtzite b) crystal structures. Microfacets are clearly visible on zinc blende nanowire side walls. TEM images of cross sections taken along the growth axis for zinc blende c) and wurtzite d) crystal phases, depicting difference in nanowire sidewalls.

In this work, we are going to study the growth of highly-mismatched InAs-on-GaAs nanowire

heterostructures. We develop a growth strategy aimed at achieving straight nanowires. We demonstrate that with an optimized growth protocol and growth parameters the yield of straight axial InAs-on-GaAs nanowire heterostructures on silicon is as high as 92%. We propose and discuss possible ways to increase the interface sharpness between InAs and GaAs segments. We find parameters for which the InAs shell formation around GaAs nanowires is inhibited. Furthermore, detailed investigations of the interface crystalline quality of thin (below 50 nanometers) and thick (above 95 nanometers) nanowires is presented.



# Chapter 3

## Experimental methods

### 3.1 Molecular beam epitaxy

#### A history of molecular beam epitaxy

At the end of the fifties, together with the progress in production of vacuum-deposited films, there was a growing need for compound semiconductors. By that time it was already known that most of III-V compounds show strong dissociation during evaporation stage. Moreover, individual components of III-V compounds (like, for example, Ga and As) have significantly different vapor pressures. As a consequence, the evaporated III-V compound films were not homogeneous in composition and did not exhibit good crystalline quality. A great progress was achieved with the development of so called “three-temperature method” (3T-method) by Gunther in 1958 [86]. In this method, a more volatile element (such as As, Sb etc.) was present in a growth chamber in excess, creating gaseous ambient while a less volatile element (such as Ga, In etc.) was evaporated directly onto a substrate. This technique allowed for the first time a stoichiometric deposition of semiconductor compounds such as InAs, InSb, GaAs. It was however not clear how to grow ternary compounds with two different group-V elements such as, for example,  $\text{GaAs}_x\text{P}_{1-x}$  by this method because of different vapor pressures of As and P. Even though the films grown by 3T-method were not single-crystal and the vacuum was far from ultra-high, it was this technique which became a prototype of well-known now molecular beam epitaxy (MBE).

It took more than a decade for the scientists to extend 3T-method in order to be able to grow high-quality single-crystal epitaxial films of III-V compounds. In 1969, J. R. Arthur and A. Y. Cho proposed to use molecular beams of group-V elements aimed directly onto a substrate instead of using their gaseous ambient for the growth [87, 88]. The vacuum conditions for the growth were significantly improved ( $1 \times 10^{-9}$  Torr instead of  $1 \times 10^{-7}$  Torr [89]). Furthermore, with time polished monocrystalline substrates instead of borosilicate glass were employed. By adding these

last two conditions to the stoichiometric deposition provided by 3-T method, the MBE technique was born.

All existing epitaxial techniques have one thing in common: the growth of one material on top of another happens epitaxially. In other words the orientation of grown crystalline material will be defined by the underlying crystal. Speaking about reagent carriers, epitaxial techniques can be roughly divided into three groups:

1. Liquid phase epitaxy (reagent carrier is a liquid phase).
2. Vapor phase epitaxy (reagent carrier is a vapor phase).
3. Molecular beam epitaxy (reagent carrier is a molecular beam).

The liquid phase epitaxy (LPE) is the oldest technique and was used for the growth of different compounds. With the miniaturization of electronic devices, however, where high-quality submicrometer structures are required, more advanced techniques (such as metalorganic vapor phase epitaxy (MOVPE) and MBE) were invented. The use of LPE now can be found in industry due to its economical reason, especially for a large-scale production (LPE is still the main way to obtain monocrystalline silicon by Czochralski process, for example).

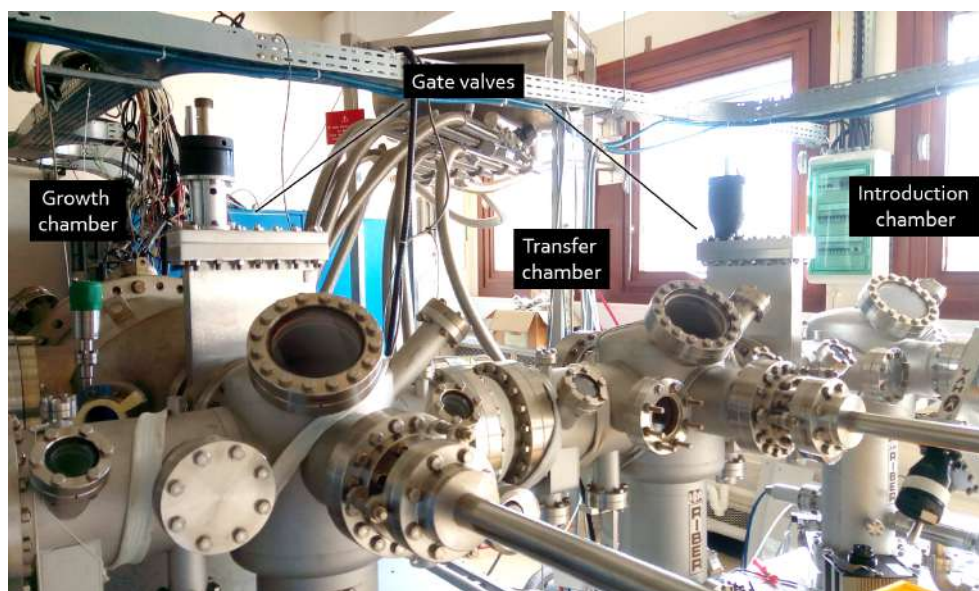
MOVPE process involves chemical reactions, which take place near substrate. Vapor-phase chemical precursors (such as, for example, Trimethylgallium and Arsine for the growth of GaAs) are used for the growth of different materials. Continuous supply of reagents, simplicity in controlling the reagents consumption (and hence, the growth rate) in a wide range and possibility to use high growth temperatures made MOVPE the most common epitaxial technique.

In a MBE reactor, the growth is carried in an ultra high vacuum environment by means of physical deposition of molecules and/or atoms on the surface. This technique allows to control the composition of the epitaxial layers with atomic monolayer precision. It is possible to monitor the growth of the crystal layers in real time using reflection high energy electron diffraction (RHEED). MBE is an important technique to realize nanostructures in both fundamental and applied research [90].

All samples considered in the present manuscript, are grown in a Riber-32 MBE reactor which is discussed hereinafter.

#### Riber-32 MBE reactor

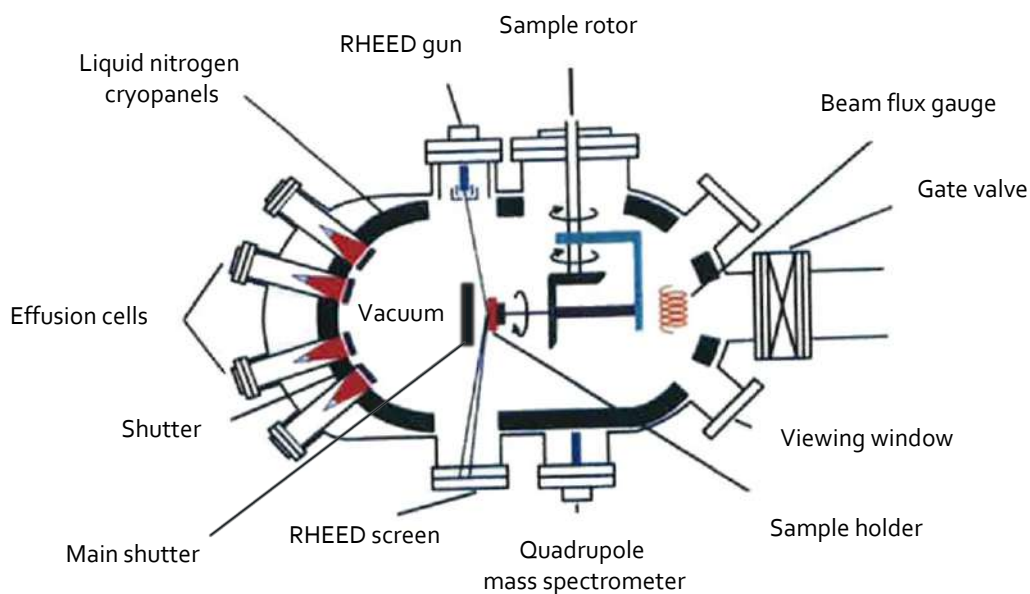
The Riber-32 MBE reactor is composed of three main parts: an introduction chamber, a transfer chamber and a growth chamber (see Figure 3.1).



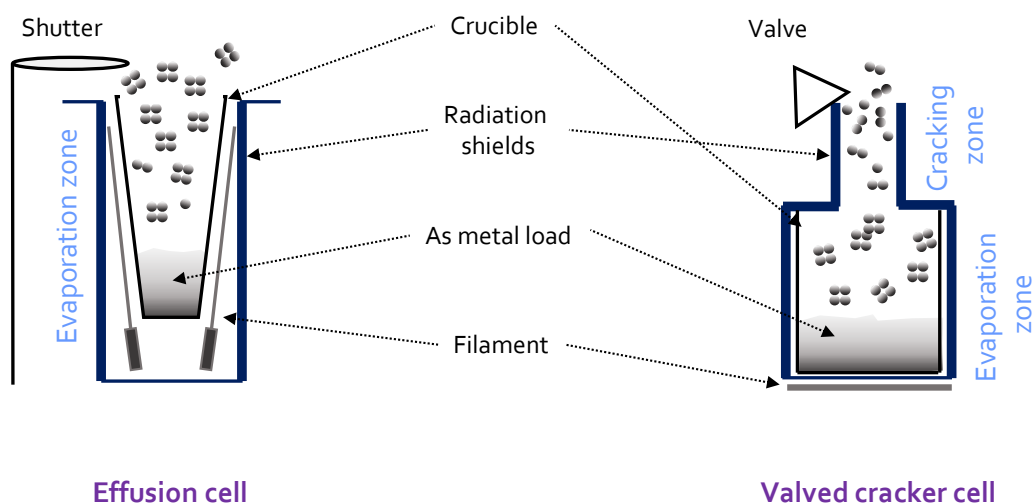
**Figure 3.1:** A picture of the Riber-32 MBE equipment at NPSC. Three chambers with corresponding gate valves are indicated.

Each chamber is isolated by a gate valve and has its own pumping system. The introduction chamber allows sample loading from the outside and, thanks to the gate valve system between the chambers, the ultra high vacuum (UHV) of the growth chamber is not affected by the loading at the atmospheric pressure. Samples are usually glued with In on a molybdenum holder prior loading into the introduction chamber. The transfer chamber connects the growth chamber with the introduction chamber. Samples are preliminarily degassed on a heater up to 250 °C in the transfer chamber in order to eliminate possible contamination and to remove water from the surface. The samples are then transferred into the growth chamber. A sketch of the growth chamber is shown in Figure 3.2.

The MBE growth chamber is made of UHV-compatible stainless steel. UHV conditions in the growth chamber are achieved by two different pumps: a turbomolecular pump and a titanium sublimation pump. We obtain a pressure of  $10^{-10}$  Torr in the growth chamber. A quadrupole mass spectrometer located in the chamber allows to monitor the background composition and to determine the level of water, oxygen, nitrogen and other contaminants by measuring the atomic weights of the chemical elements.



**Figure 3.2:** Schematic representation of the Riber-32 MBE growth chamber.



**Figure 3.3:** Sketch of an effusion cell and of a cracker cell. Both cells have an evaporation zone, where a metal load turns into vapor. However, the cracker cell has an additional zone where poly-atoms (tetramers of As in our case) are decomposed into dimers and monomers (cracking zone on the picture).

Liquid nitrogen cryopanel surround the inner surface of the growth chamber. Their cold

surface traps contaminations and residual gas species on the walls, improving the vacuum in the chamber. In addition, the cryopanel helps minimizing cross-contamination between effusion cells of different materials.

There are six effusion cells (In, Al, C, Si and two sources of Ga) and one valved cracker cell filled with As. The crucible of the effusion cells is truncated increasing the uniformity of deposited molten sources. Yet to achieve maximum uniformity rotation of the sample during each growth is still necessary. A simple sketch of the As effusion cell and the As cracker cell is shown on Figure 3.3. In the present work, the valved As cracker cell was used for all grown samples. The main advantages of the valved cracker cell compared to the normal effusion cell are: more directive flux of As, the flux is highly reproducible and precise. Moreover the higher loading capacity of the valved cracker cell leads to a longer operating life (no need to break the vacuum and open the growth chamber to refill As for a long time!).

In front of each effusion cell a shutter allows rapid interruption and resumption of material fluxes. The cracker cell has a valve, which controls the flux of supplied As. An additional general shutter is placed between the sample holder and the cells to interrupt all material fluxes simultaneously. A small hole located right opposite of the As cracker cell helps to maintain As flux while all fluxes are off (it is necessary, for example, at a cooling stage of As-like nanowire heterostructures to avoid the surface damaging 5).

## **Flux monitoring**

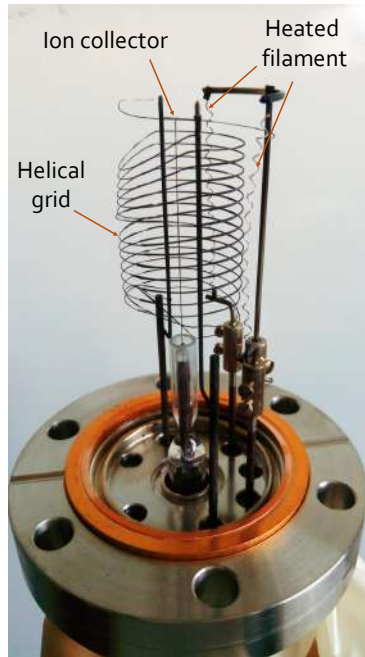
Accurate control over fluxes is necessary especially when complex heterostructures are grown in MBE. Flux monitoring is usually carried out with an ionization gauge (see Figure 3.4) which works in the range of  $10^{-3}$  to  $10^{-10}$  Torr.

The working principle of flux monitoring by the ionization gauge is simple: a heated filament emits electrons which are accelerated by the potential difference between the filament and a helical grid. These fast electrons bombard molecules of measured material and ionize them. The gas ions are attracted by the negatively charged ion collector, and the resulting current is amplified and converted into the beam equivalent pressure (BEP). Often BEP ratio is used to indicate a relation of a more volatile to the one of a less volatile element (V/III BEP ratio, for example).

The ionization gauge is positioned on the back side of the sample manipulator (see Figure 3.1). Such a configuration allows gauge shielding while samples are grown.

Measuring fluxes should be treated with caution, especially when one considers more volatile elements (As for our case). The molecules of such elements do not have high sticking coefficient compared to, for example, Ga or In, and can have a second pass through the gauge influencing the measured signal. This problem, however, can be bypassed by first measuring the flux of Ga (or the





**Figure 3.4:** The picture of ionization gauge which is composed of three main parts: a heated filament, a helical grid and an ion collector.

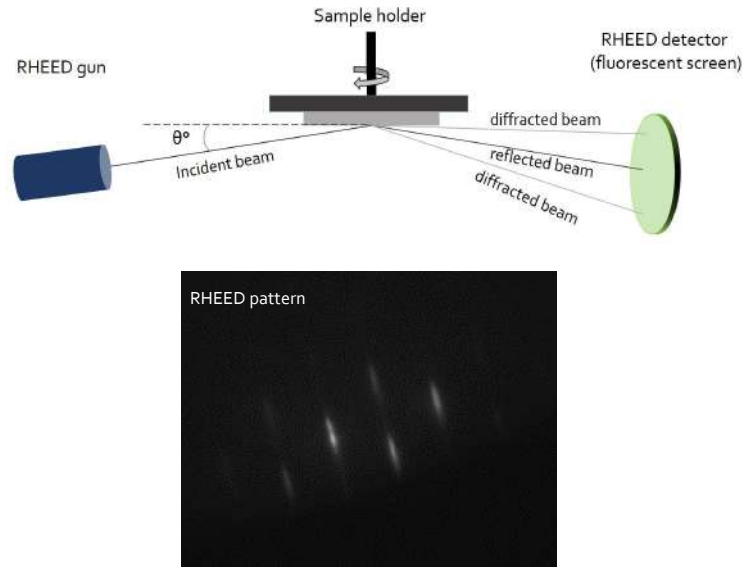
one of any group III-element). By doing so, As will be absorbed on the surface behind the gauge after its first pass, as the sticking coefficient of As is nearly one on group-III covered surfaces.

### Reflection high energy electron diffraction (RHEED)

As mentioned in introduction, to monitor the crystal growth of samples (its quality, growth rate, surface structure and temperature), we employ reflection high energy electron diffraction (RHEED). A beam of electrons in the energy range of 3-30 keV and with an incident angle  $\theta = 2^\circ$  is sent to the surface of the grown sample (see Figure 3.5). Since the incident angle is very small, electrons do not penetrate the crystal and are scattered from the upper layer of the sample. These scattered electrons which carry the necessary information about the surface hit the fluorescent screen. As a result, a pattern is visible on the RHEED screen (see RHEED pattern of a GaAs substrate after de-oxidation on Figure 3.5).

In analyzing the RHEED pattern, one needs to understand its formation. Since the incident angle of the electron beam is just  $2^\circ$  (grazing incidence), the investigated three-dimensional sample can be considered as a two-dimensional grating. The reciprocal lattice of such a grating presents rods perpendicular to the sample surface (Figure 3.6a,b). Taking into account energy and momentum conservation, constructive interferences will only occur when the Ewald sphere crosses the reciprocal rods. If the analyzed surface is atomically flat, the reciprocal rods will be

### 3.1 Molecular beam epitaxy



**Figure 3.5:** Simple sketch of RHEED system and a pattern image obtained from the fluorescent screen after de-oxidation of a GaAs substrate.

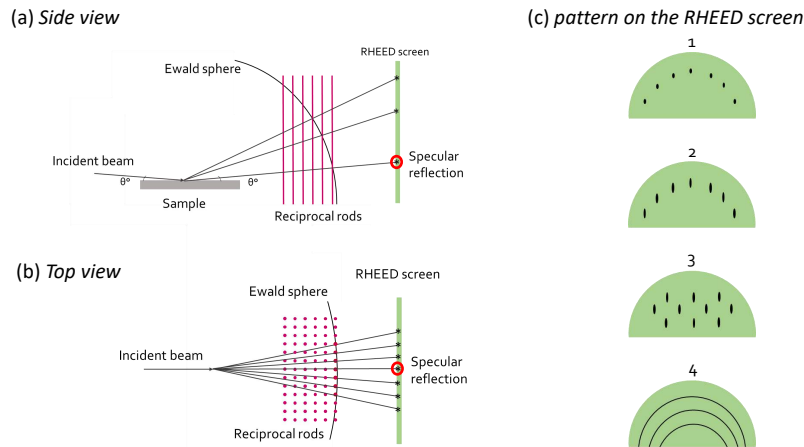
very narrow and the intersection with the Ewald sphere will result in "dots-like" pattern on the RHEED screen (see Figure 3.6 d,1). In practice, however, streaked pattern is observed (see Figure 3.6 d,2). This happens due to the broadening of the reciprocal rods caused by crystal imperfections. It worths distinguishing two additional cases: Figure 3.6 d,3 shows the RHEED pattern from the surface with small surface steps and Figure 3.6 d,4 shows the RHEED pattern from polycrystalline surfaces. Now we can decipher the RHEED pattern obtained from the de-oxidized GaAs substrate on Figure 3.5: the surface is smooth, yet with a high density of atomic steps.

The distance between streaks on the RHEED pattern brings information on the plane spacing. Indeed, after performing simple math with the Bragg scattering condition, the distance between planes can be expressed as [91]:

$$d = \frac{\lambda L}{D}, \quad (3.1)$$

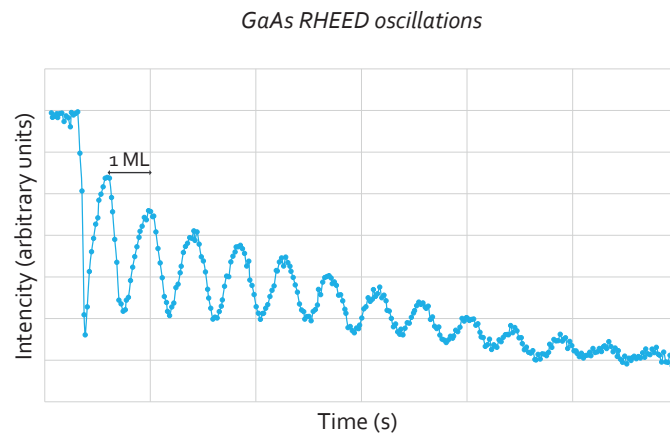
where  $\lambda$  is the electron beam wavelength,  $L$  is the distance between the sample and the RHEED screen and  $D$  is the distance between diffraction streaks.

In addition, the spot associated with the specular reflection of the beam on the sample brings very useful information. Indeed, the intensity of the specular RHEED spot oscillates during the growth and this provides us a quick and precise method for determining growth rates (see Figure 3.7). Indeed, the intensity varies depending on the surface coverage. The maximum brightness of the specular spot is achieved when the surface is fully covered and thus is smooth. Conversely,



**Figure 3.6:** Simple sketch of the RHEED pattern origin: (a)-side view and (b) - top view. The schema shows the intersection of the Ewald sphere with the reciprocal rods. (c) Schematic illustration of RHEED pattern for four different cases: 1 - ideal smooth surface, 2 - real smooth surface, 3 - smooth surface with a high density of atomic steps, 4 - polycrystalline surface.

when the surface is only half covered and thus has its maximum roughness, diffuse reflection leads to a minimal brightness. The entire amplitude cycle, therefore, corresponds to the growth of a single monolayer (ML). It is also worth noting that the RHEED oscillations dump with time as each successive ML is always more rough than the previous one.



**Figure 3.7:** RHEED oscillations taken for the GaAs growth rate. The distance between two maxima indicates the time corresponding to the growth of one monolayer.

#### **Sample temperature calibration using RHEED**

The sample temperature is measured with a thermocouple which is connected to the back side of the holder. Achieving reproducible and accurate substrate temperature is essential for MBE. Since the thermocouple wires are connected to the holder and not directly to the sample substrate, there is a discrepancy between the real substrate temperature and the one that is measured by thermocouple. Moreover, nominally identical substrate holders may provide different substrate temperatures due to the indirect measurements. Therefore, in order to have a reliable growth temperature from one growth run to the other, we performed a RHEED temperature calibration. In the current work, we used the desorption temperature of  $\text{GaO}_x$  as a reference point.

It is a well known fact that the protective oxide desorbs from GaAs at 580 °C under an As flux. The desorption will lead to the subsequent surface reconstruction: from an amorphous RHEED haze (with only one streak corresponding to the reflected beam) to a smooth crystalline RHEED pattern.

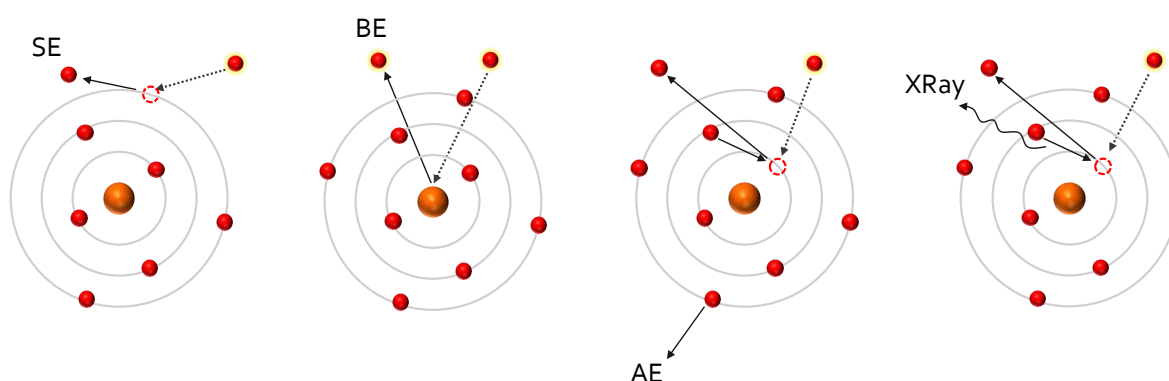
A small  $5 \times 5 \text{ mm}^2$  piece of a GaAs wafer is glued to the center of the holder. After an outgassing in the introduction chamber at 200 °C the sample is introduced into the growth chamber. The sample temperature is firstly raised to 400 °C in the absence of As flux. Once 400 °C is reached, the As valved cracker cell is opened. This step is necessary to prevent As desorption from the GaAs substrate at high temperatures. In the temperature range between 400 °C and 550 °C RHEED amorphous "haze", attributed to the oxide, along with a weak specular streak is visible. From 550 °C to approximately 580-590 °C the streak becomes more apparent owing to the weakening of the RHEED amorphous "haze". RHEED pattern in the form of bright broken streaks, attributed to the smooth crystalline surface is observed in the range between 610-640 °C in this work.

## **3.2 Electron microscopy**

The first optical microscope has been invented back in the 17th century. This was a great development which allowed people to view objects which are invisible for the naked eye (such as red blood cells or bacterias, for example). However diffraction imposes a limit on the resolution of this imaging system: any object (or details of an object) which is less than half the wavelength of the microscope's illumination source ( $< \lambda/2$ ) is not visible. Since an optical microscope uses visible light (wavelength range is 390-700 nm) as the illumination source, the estimated resolution does not exceed a few hundreds of nanometers. One way to overcome this limitation is to use high-speed electrons which have a shorter wavelength than visible photons.

## Scanning electron microscopy

In the scanning electron microscopy (SEM), a focused electron beam in the energy range of 1 to 30 kV is used to image the sample. Such an acceleration voltage is sufficient to minimize the wavelength of electrons down to 0.04 nm (for the highest energy). Each point of the sample surface is sequentially irradiated by the electron beam, which is scanning the sample. An interaction of electrons with the sample surface results in different types of signals such as secondary and back-scattered electrons, Auger electrons, X-rays and cathodoluminescence. A simple sketch of the physical nature of these signals is depicted in Figure 3.8.



**Figure 3.8:** Interaction between electrons of the scanning electron microscope and the sample. From left to right: secondary electrons (SE); backscattered electrons (BE); Auger electrons (AE); X-rays. Adapted from [92].

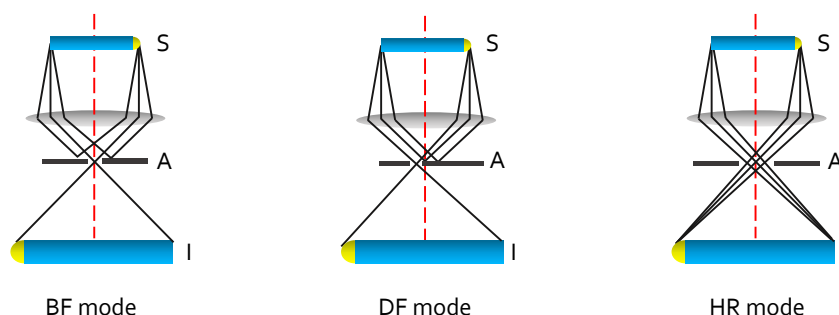
The SEM uses signals produced by electrons to observe and analyze the sample nature. Depending on the type of the signals, collected by a suitable detector, we can get an information on the surface topography (secondary electrons), the distribution of different elements (backscattered electrons), or the chemical composition (X-Rays).

SEM analysis is fast, accurate and allows to observe the sample from all possible directions through x-y-z rotation of the sample stage. In the present work, a SEM Zeiss Ultra-55 operated at 5 kV and with a spacial resolution of about 1 nm was used. All samples were cleaved in parts before the SEM studies. The freshly cleaved surface was used to image the side view of the sample and to measure the growth direction, the length, the diameter and the actual morphology of grown nanowires, as well as to investigate a 2-dimensional (2D) growth on the surface. Top-view imaging was performed in order to estimate the nanowire density, the direction of possible nanowire kinking and the ratio of kinked over straight nanowires. Some samples were mechanically transferred on a carbon grid and imaged from the top before composition analysis by energy-dispersive x-ray

spectroscopy. Observation of the sample with a  $30^\circ$  tilt was used to obtain an overview of the morphology of the sample, the surface of the 2D growth, the nanowire kinking and its angle and, again, the ratio of kinked over straight nanowires. The SEM Zeiss Ultra-55 offers the possibility to work in the scanning-transmission electron microscopy (STEM) mode thanks to an additional sample holder with build-in detector which is located right below the sample. This holder can be placed inside the SEM chamber. We used this detector from time to time to have a quick information on a structure and composition of the samples. However, when detailed information on the structural properties of nanowires was necessary, high-resolution transmission electron microscopy (TEM) was used.

## Transmission electron microscopy

TEM is a powerful tool which enables a direct imaging of the crystalline lattice. It thus provides information on the crystal structure, the crystallographic orientation, and on possible structural defects and dislocations. All of this is possible thanks to high accelerating voltages of irradiated electrons (typical range is 100-300 kV), which is much higher than in case of SEM. The high voltage together with the specially prepared thin sample (thickness  $< 100$  nm) allows penetration of electrons through the sample. An image is formed due to the electrons which pass through the sample and interact with it. The image plane is then magnified by a system of lenses and displayed on a fluorescent screen.



**Figure 3.9:** Three main image modes of TEM depending on the position of the objective aperture. From left to right: bright field (BF); dark field (DF); high-resolution (HR). Capital letters S, A and I represent Sample, Aperture and Image respectively.

In TEM, the sample is illuminated with a parallel beam of electrons. The image interpretation depends on the operation mode of the TEM. There are several image modes: bright field (BF) TEM, dark field (DF) TEM and high-resolution (HR) TEM (see Figure 3.9). In all cases a selective aperture situated at or near the focal plane is inserted. In BF mode, the image is formed from the direct beam only. The aperture is placed in such a way that only transmitted beam which has not been scattered and diffracted is selected. In this case the image contrast is due to the weakening of

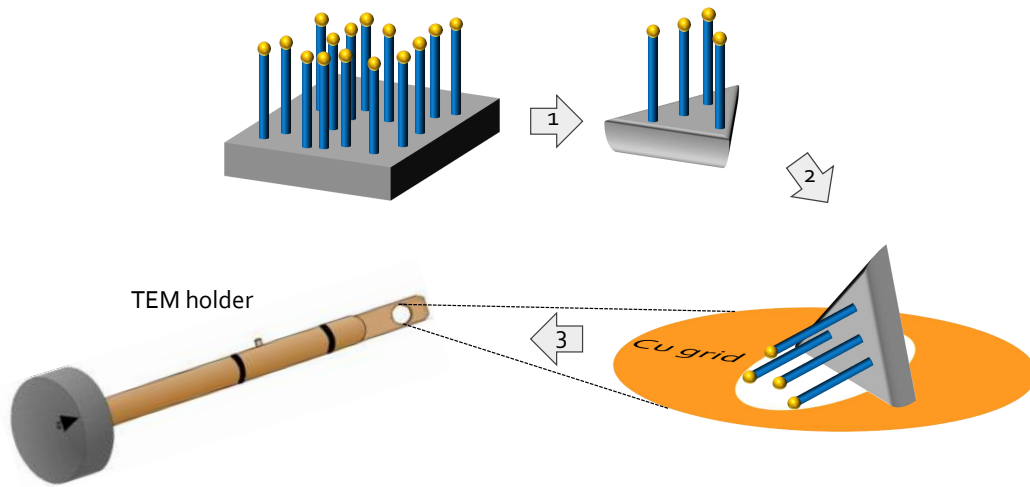
the direct beam: objects with higher density of electrons, made of heavier elements will result in darker contrast (Au nanoparticle appears darker than GaAs or InAs, for example). In the DF mode, the aperture blocks the direct beam while the diffracted beams are selected. Since the diffracted beams have strongly interacted with the sample, a very useful information can be collected in the DF TEM (information on dislocations, stacking defects). In HR mode, this aperture can be inserted in order to select both the direct beam and a few diffracted beams. This use of the objective aperture can increase the contrast and smooth some details of the HRTEM images, but it also limits the resolution of the HR-TEM image. Consequently in practice, the objective aperture is not inserted in HR-mode.

One additional high-resolution functionality of a modern TEM is a scanning transmission electron microscopy (STEM) mode. In this case, the electron beam is focused on a narrow spot on the sample (instead of a parallel beam of electrons like in TEM) and like in SEM this spot scans the sample. Similar to TEM, STEM uses the transmitted beam to build up the final images. However, instead of the objective lens and the selective aperture special detectors are employed: a BF detector is placed on-axis below the sample and collects the direct beam, an annular DF (ADF) detector gathers electrons, scattered through small angles and a high angle ADF (HAADF) detector collects electrons scattered out to higher angles. HAADF images are sometimes referred to as Z-contrast images because the contrast depends on the atomic number  $Z$  of the chemical element (roughly as  $Z^2$ ).

Contrary to HR-TEM images, whose contrast critically depends on many parameters such as a sample thickness, beam tilt, defocus, HR-STEM images are generally much easier to interpret. In HR-TEM atomic columns can be white or black depending on the experimental parameters. In HR-STEM images, atomic columns are always white

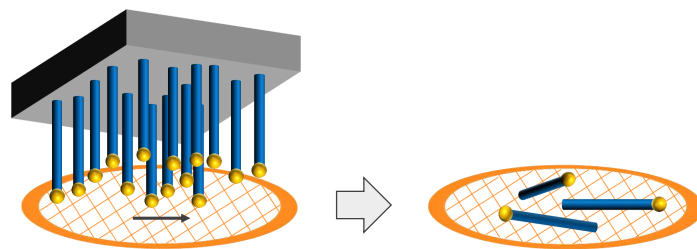
Another advantage of the STEM mode is the possibility to obtain a spatially resolved chemical composition of the sample with energy dispersive X-ray spectroscopy (EDX). A simple sketch explaining its working principle is presented on the right diagram of the Figure 3.8. The sample is illuminated with the focused electron beam and the X-ray spectrum is collected by an energy-dispersive spectrometer. This spectrum is characteristic of each chemical element. Its analysis therefore yields the sample composition.

In the present work, a CM300 TEM equipped with a LaB6 thermionic emitter operated at 300 kV was used for crystalline structure investigations (and to investigate an epitaxial relationship between grown NWs and the substrate) in the TEM mode. The detailed chemical composition and the crystalline structure of the nanowires were investigated by EDX and HAADF STEM on a probe corrected FEI Titan Themis working at 200 kV, equipped with four silicon drift detectors for EDX. As mentioned earlier, the TEM samples should be very small and especially *extremely thin* (less than 100 nm in thickness) for the correct investigation. We discuss below sample preparation for TEM, HAADF STEM and EDX.



**Figure 3.10:** Schematic representation of the TEM sample preparation. The sizes of the cleaved sample and the Cu grid are intentionally exaggerated.

For TEM measurements, the samples were first cleaved in small "pie-like" pieces (see Figure 3.10). Then, the cleaved sample was glued to a copper (Cu) grid, as shown on the second step of the Figure 3.10. Finally, the Cu grid was placed on a TEM holder. Individual nanowires can be easily studied on the sharp corners of such cleaved sample. Moreover, the nanowires are not removed from the original substrate and the epitaxial relationship between the substrate and the grown crystals can be studied. However, samples prepared using this technique are not well suited for EDX analysis. Indeed, the substrate will give an additional X-ray signal. For this reason, for the STEM and EDX measurements the nanowires were mechanically transferred on a carbon membrane by simply sliding the membrane across the NW sample (see Figure 3.11).



**Figure 3.11:** Schematic representation of the sample preparation for the HAADF STEM and EDX studies.

One way to extract a quantitative information from HRTEM and HRSTEM images is to use a Geometrical Phase Analysis (GPA) [93], a technique based on a Fourier space algorithm. This technique is discussed hereafter.



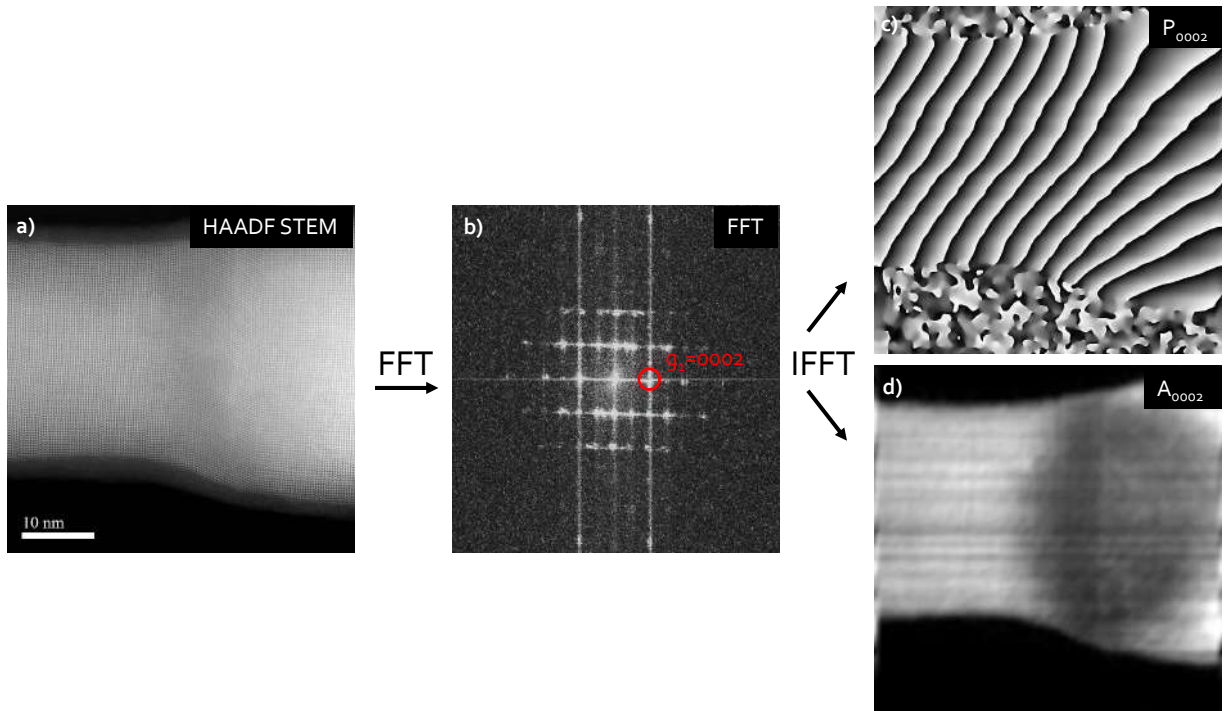
### 3.3 Geometrical Phase Analysis

Geometrical Phase Analysis (GPA) is a powerful image processing tool which is extremely helpful to extract local lattice displacement and strain fields from HRTEM images [93]. Moreover, the technique allows to visualize the obtained local distortions in 2D color map format. The method is based on a double fast Fourier transform (FFT): the first FFT, applied to the original HRTEM image, yields Bragg peaks and the second one (so called inverse FFT (IFFT)) is performed on one of the peaks, providing an access to the local lattice variations from the phase component of the resulting complex image.

Indeed, any HRTEM image of a crystal structure can be represented as a Fourier transform:

$$I(\mathbf{r}) = A_0 + \sum_{g>0} 2A_g \cos(2\pi \mathbf{g}\mathbf{r} + P_g), \quad (3.2)$$

where  $I(\mathbf{r})$  is the image intensity at the position  $\mathbf{r}$ ,  $\mathbf{g}$  is the reciprocal lattice vector,  $A_g$  and  $P_g$  are the amplitude and the phase, respectively, corresponding to the particular reciprocal lattice vector. The GPA plots an image equivalent to this equation (see the FFT image on Figure 3.12 b).



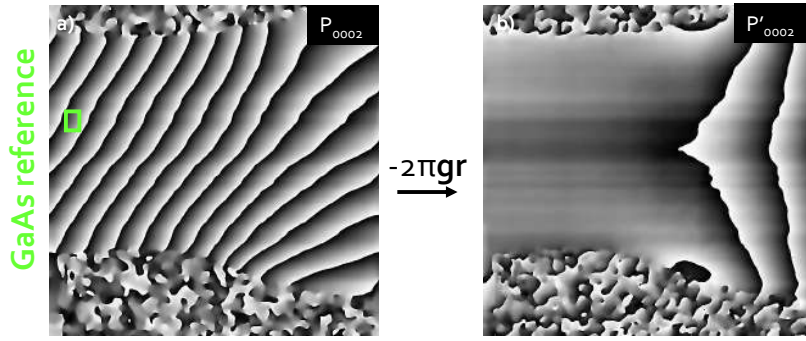
**Figure 3.12:** GaAs/InGaAs nanowire heterointerface. a) HAADF STEM image taken along the [2-1-10] viewing direction; b) FFT image obtained by GPA with the selected Bragg peak  $g = 0002$ ; c) phase  $P_{0002}$  and d) amplitude  $A_{0002}$  images obtained by IFFT applied to the  $g = 0002$  of the FFT image b).

### 3.3 Geometrical Phase Analysis

The image corresponding to a particular set of  $\mathbf{g}$  (we will call it  $B_g(\mathbf{r})$ ) can be therefore written as:

$$B(\mathbf{r}) = 2A_g \cos(2\pi \mathbf{g} \mathbf{r} + P_g). \quad (3.3)$$

To obtain this equation in the image format by GPA, we filter only one of the Bragg peaks from the FFT image (3.12 b)) and perform the IFFT. The final complex image will consist of phase (3.12 c)) and amplitude (3.12 d)) components. The gradient of the phase indicates the deviation in the lattice vector [93]. In order to observe this deviation more clearly, it is necessary to choose on the phase image a phase-reference-area, where the software will calculate its average phase value, and subtract the averaged value from the original phase image. An example of this procedure can be found in Figure (3.13): the a) image is a raw phase component  $P_{0002}$  obtained from the HAADF STEM 3.12 a). We take undistorted GaAs lattice far from the interface as a reference, and subtract this value out of the raw phase image. The resulting phase (we will call it  $P'_{0002}$ ) is shown in Figure 3.13 b): the phase is nearly zero in the GaAs segment before the interface (since this part has been chosen as a reference and the lattice vector has not undergone any significant changes). A noticeable color gradient can be seen on the right side from the interface which corresponds to the ternary InGaAs segment. The abrupt black and white color variation is caused by phase renormalization between  $\pm\pi$ .



**Figure 3.13:** GaAs/InGaAs nanowire heterointerface. From left to right: [2-1-10] HAADF STEM image; FFT image obtained by GPA with the selected Bragg peak  $g_1 = 0002$ ; phase  $P_{0002}$  and amplitude  $A_{0002}$  images obtained by IFFT applied to the  $g_1 = 0002$  on FFT image.

The local deformation can be found out of the gradient of the displacement field of two non collinear lattice vectors:

$$e = \begin{bmatrix} e_{xx} & e_{xy} \\ e_{yx} & e_{yy} \end{bmatrix} = \begin{bmatrix} \frac{dU_x}{dx} & \frac{dU_x}{dy} \\ \frac{dU_y}{dx} & \frac{dU_y}{dy} \end{bmatrix}. \quad (3.4)$$

The symmetric part of this matrix represents the strain (we will call it  $\varepsilon$ ):

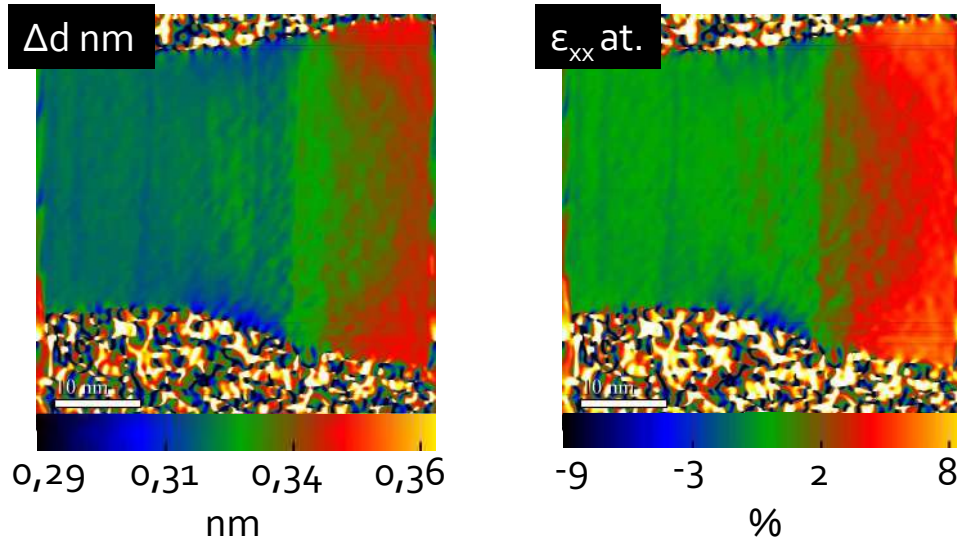
$$\varepsilon = \frac{1}{2}(e + e^T), \quad (3.5)$$

and the antisymmetric part represents the local rigid rotation  $\omega$ :

$$\omega = \frac{1}{2}(e - e^T), \quad (3.6)$$

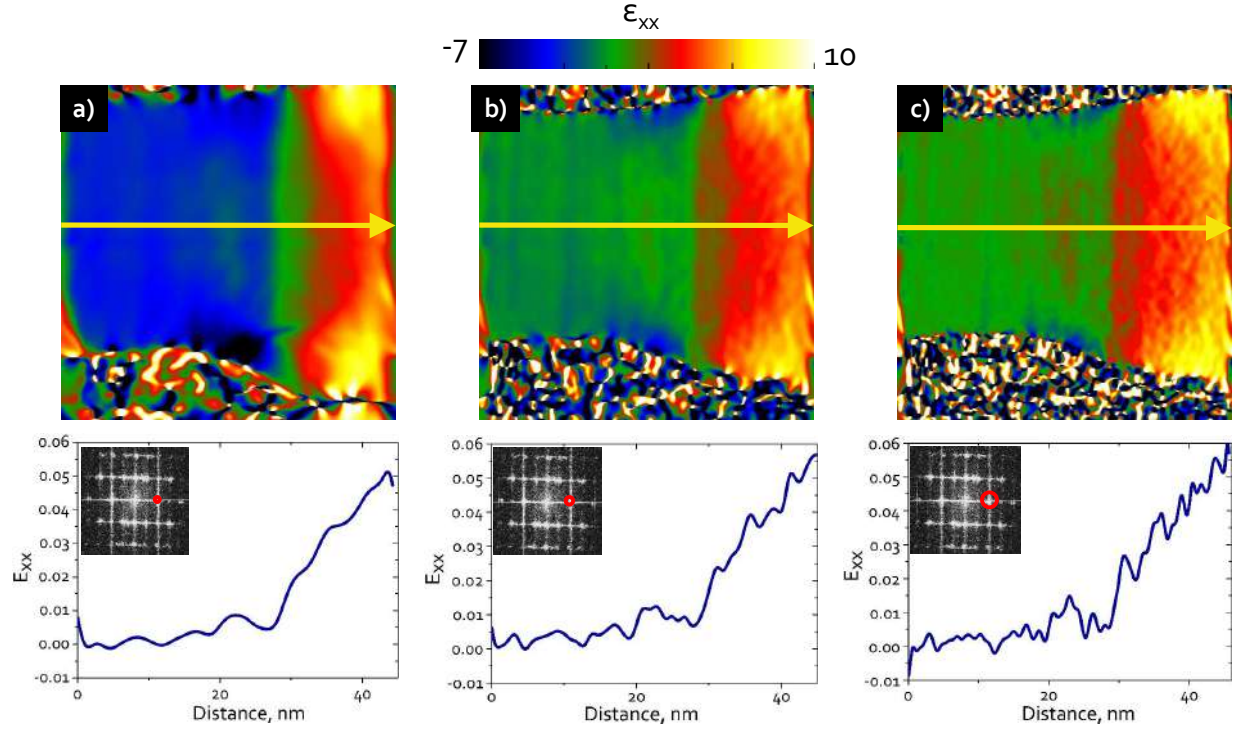
here  $e^T$  is the transpose deformation matrix.

Figure 3.14 shows 2D color maps obtained by GPA for a GaAs/InGaAs nanowire: a local lattice variation  $\Delta d$  and the  $\varepsilon_{xx}$  component of the strain tensor.



**Figure 3.14:** 2D color maps of the GaAs/InGaAs nanowire heterointerface corresponding to the  $g=0002$ . From left to right: local lattice variation  $\Delta d$  (corresponds to  $c/2$  in wurtzite) and  $\varepsilon_{xx}$  component of the strain tensor.

When analyzing GPA results it is important to keep in mind that the spatial resolution of the final image depends on the size of the mask which is applied to the particular Bragg peak. Since the reciprocal space has an inverse relation to the direct space, the bigger the mask size we use in FFT the smaller the mask size in the real space and the better the spatial resolution of the final image. To demonstrate this effect, three different mask sizes were chosen. Figure 3.15 shows the  $\varepsilon_{xx}$  strain color maps and corresponding line profiles obtained from 3.12 (a) for three mask sizes: (a)  $20 \text{ nm}^{-1}$ , (b)  $45 \text{ nm}^{-1}$  and (c)  $97 \text{ nm}^{-1}$  (numbers correspond to the radius of the mask in the reciprocal space, masks are visible in red on the FFT images). The  $97 \text{ nm}^{-1}$  radius was chosen as the largest mask which does not include additional Bragg peaks.



**Figure 3.15:**  $\epsilon_{xx}$  strain maps and corresponding line profiles of the GaAs/InGaAs nanowire heterointerface ( $g=0002$ ) for three different mask sizes: (a)  $20 \text{ nm}^{-1}$ , (b)  $45 \text{ nm}^{-1}$  and (c)  $97 \text{ nm}^{-1}$ . Masks are indicated in red on FFT images.

The maps and profiles are qualitatively the same for all cases: a compressed InGaAs layer is visible on top of a GaAs segment. However, increasing the mask size improves the spatial resolution, and essentially leads to larger values of  $\epsilon_{xx}$ . Yet, the increase in spatial resolution comes with an increase in the noise. It becomes extremely pronounced for the largest mask (see Figure 3.15 (c)).

All the image processing performed in the current work was carried out using GEM GPA v7 software written by Jean-Luc Rouviere [94]. We used the mask size of  $\sim 45 \text{ nm}^{-1}$  in order to preserve a balance between a good spatial resolution and a high signal-to-noise ratio.



## Chapter 4

# Growth of GaAs-on-Si nanowire heterostructures

Today, highly sensitive single-photon detectors with the ability to amplify weak input signals are required in fiber-optic communication systems. Silicon-based avalanche photodetectors are widely used for these purposes owing to both high gain (up to 1000) and low noise, high sensitivity, low cost and a direct compatibility with the silicon-based technology [95, 96]. Moreover, Si photodetectors in a nanowire geometry have the potential for higher sensitivity thanks to their reduced cross section [97]. Yet, the band gap of silicon is 1.12 eV and is too high to detect light at the telecom wavelength. Thus, the insertion of an optically active, low band-gap InAs segment in a Si nanowire seems a natural strategy to realize highly-sensitive single-photon detectors at telecommunication wavelengths. However, the extremely high lattice-mismatch between InAs and Si (more than 11%) makes it challenging to realize such heterointerfaces [14] with the last being crucial for the device performances. In contrast, the mismatch between Si and GaAs is only 4%. Therefore, the use of a thin GaAs barrier between Si and InAs segments contributes to reduce strain and to produce dislocations free heterointerfaces. Thus, the final nanowire heterostructure should contain four heterointerfaces, namely: Si/GaAs, GaAs/InAs, InAs/GaAs, GaAs/Si.

In this chapter, we will focus on the first heterointerface, namely Si/GaAs. The growth of hybrid IV/III-V nanowire heterostructures is more difficult and much less studied than the growth of materials from the same semiconductor family. Only very recently impressive results on the growth of axial Si/III-V [22, 98] and Ge/III-V [98] nanowires were demonstrated. In particular, it was shown that the combination of GaAs and Si in a nanowire heterostructure is possible if a thin GaP [22] or a thin Ge [98] barrier is introduced between GaAs and Si. In both cases, the growth of such complex heterostructures was performed by means of metalorganic vapor phase epitaxy. Another way to directly combine GaAs and Si in nanowires was proposed by Sonia Conesa-Boj and co-authors [99]: Ga-assisted GaAs nanowires were grown in a molecular beam



epitaxy reactor while Si segments were grown at low growth temperatures in a plasma enhanced chemical vapor deposition reactor. By a careful tuning of the Ga droplet supersaturation and the growth temperature, a Si axial segment grew on top of GaAs stems. However, the Ga droplet at the top of the final structure was damaged, preventing the growth of additional axial segments.

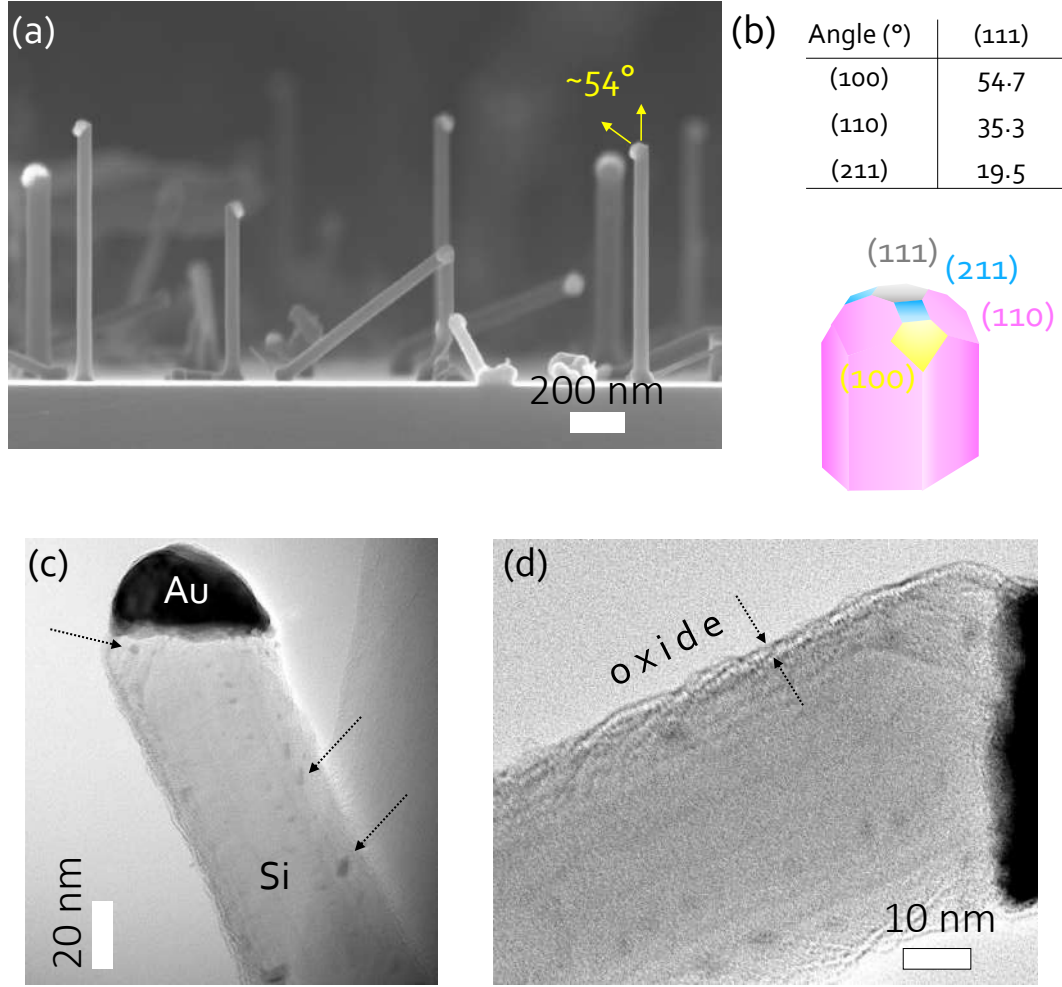
In this chapter, we present studies on the molecular-beam epitaxy growth of GaAs segments on top of Si nanowires, that were grown by chemical vapor deposition. We recycle the gold catalyst present at the Si nanowire tips to grow GaAs segments. We first analyze the effect of different chemical treatments, used to remove the native oxide formed both on the Si nanowires and on the substrate, on the morphology and chemistry of Si nanowires. The chemical treatments are performed prior to loading the samples to the molecular beam epitaxy reactor. We then study how the morphology of Si/GaAs nanowires is affected by the growth temperature. Finally, we propose alternative ways of combining GaAs and Si in nanowire heterostructures.

## **4.1 Analysis of the silicon nanowires**

The most common way to synthesize Si nanowires is the vapor-liquid-solid method with Au as a catalyst [26, 100, 101, 102]. The advantages of using an Au catalyst are: availability, chemical stability (does not oxidize in air) and low eutectic temperature with Si. On the other hand, Au is known to diffuse on the Si nanowire sidewalls. This problem is particularly present when Si nanowires are grown by low-pressure chemical vapor deposition [100, 102]. The Au clusters, in turn, can promote the growth of branches on the nanowire sidewalls [103, 104] and increase its roughness. More dramatically, Au forms deep levels in the band gap of Si. Therefore, it is important to keep the Au droplet far from critical surfaces.

In this work, Si nanowires were grown in the vapor-liquid-solid mode on Si(111) substrates in a low pressure chemical vapor deposition reactor by Pascal Gentile at CEA/INAC [105, 103]. Silane ( $\text{SiH}_4$ ) was used as the source of Si and hydrogen ( $\text{H}_2$ ) was used as a carrier gas. Gold colloids with 50 nanometers diameter were deposited on Si(111) substrates before the growth. The growth temperature was 620 °C and the Si nanowires were grown for 1 hour. We first analyzed the morphology of the Si nanowires by scanning electron microscope (SEM) imaging and then with a transmission electron microscope (TEM).

A side-view SEM image of the nanowires is presented in Figure 4.1 a. Most Si nanowires are perpendicular to the Si(111) substrate. After analyzing several SEM images, we estimate that, on average, the length and diameter of the nanowires are  $828 \pm 118$  nm and  $68 \pm 21$  nm, respectively. The Au droplets, which are visible at the tips of nanowires, sit on a top facet forming an angle with the {111} growth direction. We measured this angle on a series of nanowires and it is equal to  $53.80^\circ \pm 3^\circ$ . Within the margin of error, it corresponds to the angle formed between the {100}-oriented facets and the (111)-top facet ( $54.7^\circ$ , see Figure 4.1 b). Therefore, the Au



**Figure 4.1:** Au-assisted Si nanowires on a Si(111) substrate. a) Side-view SEM image of the Si nanowires. The angle between the top (111) facet and the gold droplet is indicated in yellow. b) Schematic illustration of the facets and the corresponding angles they make with the (111) top facet in zinc blende Si nanowires. Bright-field TEM image c) and close up view d) of a typical Si nanowire. In this mode, the gold particle appears in dark contrast and is visible at the top of the nanowire. Moreover additional small gold clusters are present on the nanowire sidewalls (some of them are indicated by arrows on c) ). A 2 nm thick silicon oxide layer is visible on c).

droplet sits on a {100}-oriented facet. During the vapor-liquid-solid growth of Si nanowires on (111) substrates, the nanowire/droplet growth interface is not planar but has periodically occurring truncated facets. Moreover, it was demonstrated that the size of the truncated facet depends on the supersaturation of the catalyst droplet [106]: the smaller the supersaturation the bigger the truncated facet. We suppose that {100}-oriented facets are formed at the end of the growth process, after closing the silane valve and cooling down the substrate to room temperature. At this stage,



nanowire growth proceeds via the consumption of Si remaining in the liquid gold droplet. This quickly reduces the droplet supersaturation provoking thus an enlargement of the truncated facet. As the Au droplet continuously shrinks, it becomes unstable and can slide down to one of the formed truncated facets [107].

We then take a close-up view of the Si nanowires using bright field TEM imaging. A typical nanowire is shown in Figure 4.1 b. The gold droplet can be clearly identified at the top of the Si nanowire. Moreover, small Au clusters are visible on the nanowire sidewalls and are consistently observed for all studied Si nanowires. We also observe a few nanometer thick silicon oxide layer, surrounding each Si nanowire (Figure 4.1 c). The oxide forms when samples are removed from the reactor and exposed to air. Thus, before loading the Si nanowire samples into the molecular beam epitaxy reactor to grow GaAs segments, it is necessary to perform a series of chemical treatments to deoxidize the nanowires and the surfaces of silicon substrates.

## 4.2 Si nanowire surface preparation prior to GaAs growth

Chemical cleaning methods can be divided into two groups, namely hydrophilic and hydrophobic. The hydrophilic strategy aims at simultaneously removing the naturally formed silicon oxide layer and at forming an intentional ultrathin protective oxide layer which is then removed in a growth chamber at 800 °C. The main advantage of this method is that the protective layer is inert with air. However, it was demonstrated that hydrophilic cleaning results in the contamination of silicon surfaces by boron atoms dissolved from glasswares [108, 109]. Moreover, it was suggested that boron contamination is responsible for roughening the silicon surface [109].

The hydrophobic methods consist in dissolution of the silicon oxide using, for example, hydrofluoric acid (HF) or ammonium fluoride (NH<sub>4</sub>F). The use of such chemicals leads to hydrogen-terminated surfaces, preventing re-oxidation of the sample. Hydrogen can be then thermally desorbed at temperatures around 500 °C in the growth chamber. Yet, it is important to remember, that silicon surfaces terminated with hydrogen are not stable in air and slowly transform into silicon oxide. This means that the time between deoxidation and the loading of silicon substrates into the growth chamber must be kept to a minimum.

Given a vast literature on chemical treatments of silicon oxide, the most common ones are: 1) pure HF; 2) a mixture of HF and NH<sub>4</sub>F; 3) Piranha solution (H<sub>2</sub>SO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub>, hydrophilic method) followed by HF or NH<sub>4</sub>F cleaning to decrease boron contamination [110, 111, 109]. It was experimentally demonstrated that a surface treated with HF is rougher than a surface treated with NH<sub>4</sub>F [112]. Yet, the authors emphasize that any roughness obtained with HF can be then decreased by dipping the sample in a NH<sub>4</sub>F solution. Taking into account all considerations above, we tested two different recipes to de-oxidize our Si nanowires sample. The sample was cut into

## 4.2 Si nanowire surface preparation prior to GaAs growth

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three pieces. The first part was left as it is. The remaining pieces were cleaned with one of the following chemical procedures:

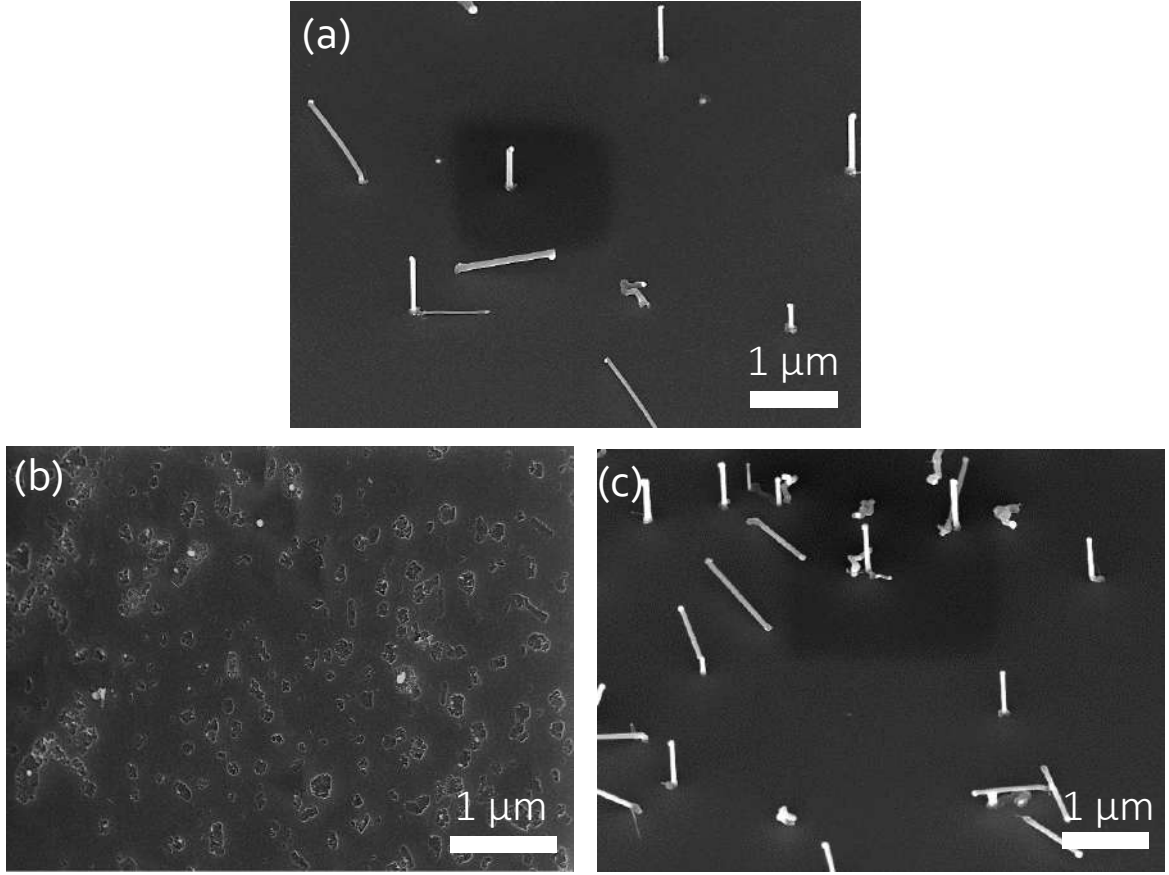
- **Method 1:**  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$  3:1 followed by  $\text{NH}_4\text{F}$  (20 minutes, 10 minutes);
- **Method 2:** 1% HF followed by  $\text{NH}_4\text{F}$  (1 minute, 40 seconds).

Note that all substrates were rinsed thoroughly in deionized water after each chemical step. After the final water rinse the substrates were blown dry with nitrogen. We analyzed the three pieces of the sample by scanning electron microscopy and the results are presented in Figure 4.2. The nanowire surface density before chemical treatments is found to be  $7 \times 10^9 \text{ cm}^{-2}$ .

**Method 1:** no nanowires are observed at the surface and only gold droplets can be seen on the sample (Figure 4.2 b). The substrate surface is noticeably rough with nanometer size grooves. Since we did not find any Si nanowires, we suspect, that either the nanowires were etched away or they were detached from the substrate. Taking into account, that  $\text{NH}_4\text{F}$  etches silicon at approximately 0.5 nanometers per minute [113] at room temperature, 10 minutes is obviously not enough to etch nanowires with 60 nanometer diameter. On the other hand, the Piranha solution is a strong oxidizer and Si nanowires will probably oxidize after the  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$  step.  $\text{NH}_4\text{F}$  etches silicon oxide much faster than silicon (7.2 nanometers per minute) and it is likely that the oxidized Si nanowires were etched away from the Si substrates during the 10 minutes  $\text{NH}_4\text{F}$  etching step in the Piranha-treatment procedure.

**Method 2:** in contrast to Method 1, the density of nanowires remains unchanged (see Figure 4.2 c). Moreover, no visible roughness is observed at the surface. In order to estimate whether the silicon oxide was successfully removed, we performed transmission electron microscopy studies of the sample. Figure 4.3 b shows the Si nanowires before chemical treatment. We observe a rough, 2 nanometers thick, silicon oxide layer on the nanowire surface. Moreover, a large number of gold clusters is observed at the nanowire sidewalls. On average, we find 32 gold clusters per 120 nanometers length. The gold clusters diameter ranges from 1 to 5 nanometers. In contrast, we did not find any traces of silicon oxide after the HF-treatment (Figure 4.3 b) and the sidewalls of the nanowires are much smoother than before the treatment. Interestingly, the amount of gold clusters is notably reduced. We find approximately 7 gold clusters per 120 nanometer length. The gold clusters density is reduced by 4.5 times after chemical treatment.

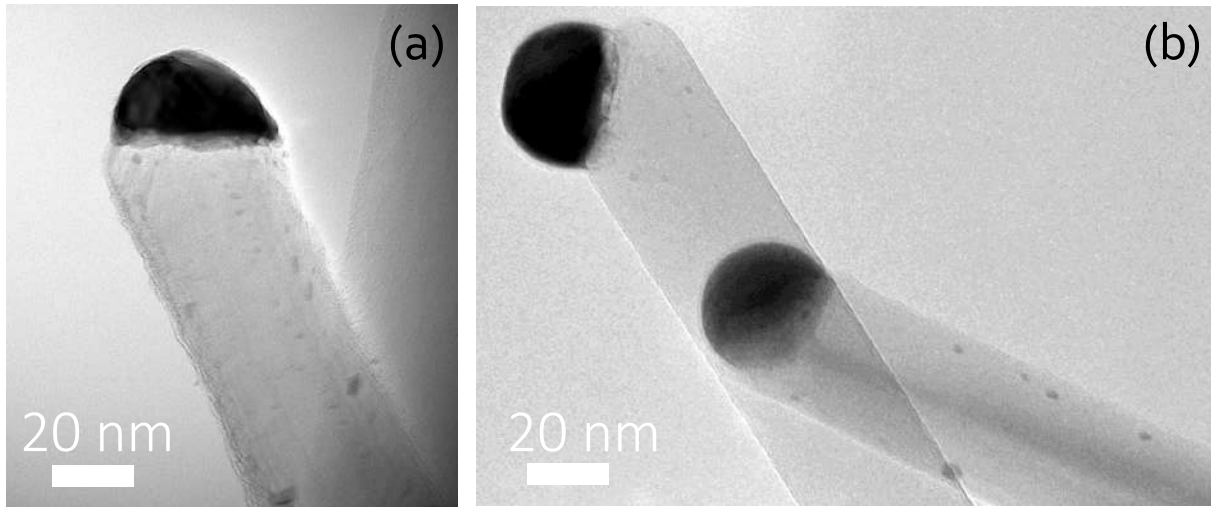
Gold is a noble metal and is known to be very stable. Chemical etching of gold requires a strong oxidizer and, thus, there are only a few chemical solutions which can etch gold at room temperature, namely a mixture of nitric acid ( $\text{HNO}_3$ ) and hydrochloric acid ( $\text{HCl}$ ), also known as Aqua Regia, and a mixture of potassium iodide ( $\text{KI}$ ) with iodine ( $\text{I}$ ). Method 2 consists in using HF and  $\text{NH}_4\text{F}$  solutions. Those solutions do not etch the gold clusters, present on the nanowire sidewalls. However, during its contact with air, the Si nanowires oxidize. The layer of silicon oxide



**Figure 4.2:** Au-assisted Si nanowires on Si(111) substrate before (a) and after chemical treatments (c, d). All the images are taken with a 30° tilt. a) SEM image of as-grown Si nanowires. b) SEM image of the sample surface after the Piranha treatment. No nanowires are found and only gold droplets are present at the surface (the droplets are indicated with arrows). The surface is rough which is visible even with the naked eye. c) SEM image of the sample after the HF-treatment.

can be also formed below the nanometer-sized gold clusters. During the HF/NH<sub>4</sub>F procedure of Method 2, the silicon oxide is removed, leading to the lift-off of gold clusters from the nanowire surface.

To conclude, we successfully removed silicon oxide from Si nanowires with the Method 2 chemical treatment. The density of the nanowires remained the same as before the treatment. Moreover, we observed a significant reduction of the parasitic gold clusters decorating the nanowire sidewalls. We thus used this procedure for all samples grown in this chapter. The transport of clean samples from the chemical bench to the molecular beam epitaxy reactor was done in closed beakers filled with nitrogen in order to avoid re-oxidation of the silicon surface. Before reaching



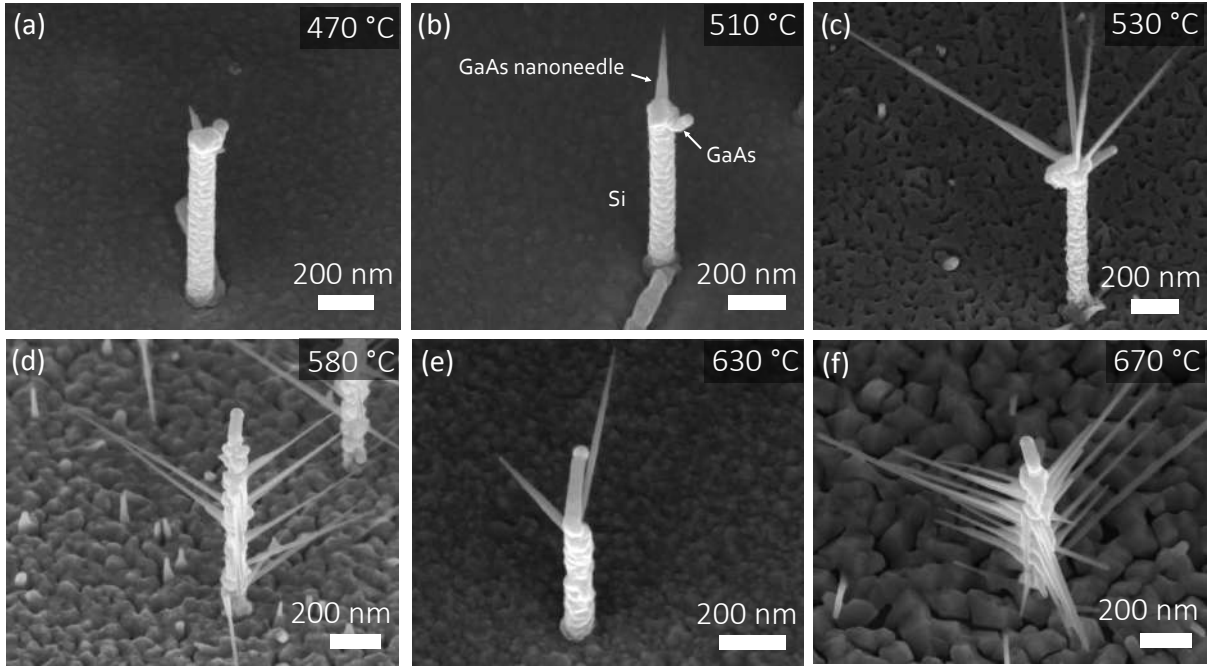
**Figure 4.3:** Au-assisted Si nanowires on Si(111) substrate before and after HF-treatment. a) Bright-filed TEM image of a typical as grown Si nanowire. A 2 nm thick silicon oxide layer and a large number of gold clusters are visible on the surface of the nanowire. b) Bright-filed TEM image of a typical Si nanowire after the HF-treatment. No silicon oxide can be seen on the nanowire surfaces. The number of gold clusters is significantly reduced and the surface is visibly smooth.

the growth chamber, the substrates were degassed at 200 °C in a high vacuum transfer module until the pressure dropped below  $2 \times 10^{-8}$  Torr.

### 4.3 Growth of GaAs segments on top of Si nanowires

We started our experiments with growth temperature studies by investigating the effect of the growth temperature on the morphology of GaAs segments on Si nanowires. Following the experimental findings reported in the work of Tchernycheva and coauthors [114] for Au-GaAs nanowires grown by means of molecular beam epitaxy on GaAs(111)B substrates, we grew a set of samples with growth temperature ranging between 470 °C and 670 °C (see Figure 4.4). We used fixed Ga and As fluxes of  $0.28 \text{ nm s}^{-1}$  and  $1 \times 10^{-5}$  Torr, respectively. The corresponding Ga flux was found from a two-dimensional equivalent growth rate on a GaAs(001) surface. The corresponding V/III beam equivalent pressure ratio equals to 30. To grow GaAs segments, the samples were heated to the desired growth temperature with a ramp of  $40 \text{ °C min}^{-1}$ . After one minute of stabilization, we opened simultaneously the As cracker cell valve and the gallium shutter. The growth of GaAs segments was performed during 8 minutes. After growth, the gallium shutter was closed and the substrate was cooled down under an arsenic flux.

Figure 4.4 presents the evolution of Si/GaAs nanowire heterostructures as a function of the growth temperature. Importantly all nanowires feature lateral GaAs nanoneedles grown on the

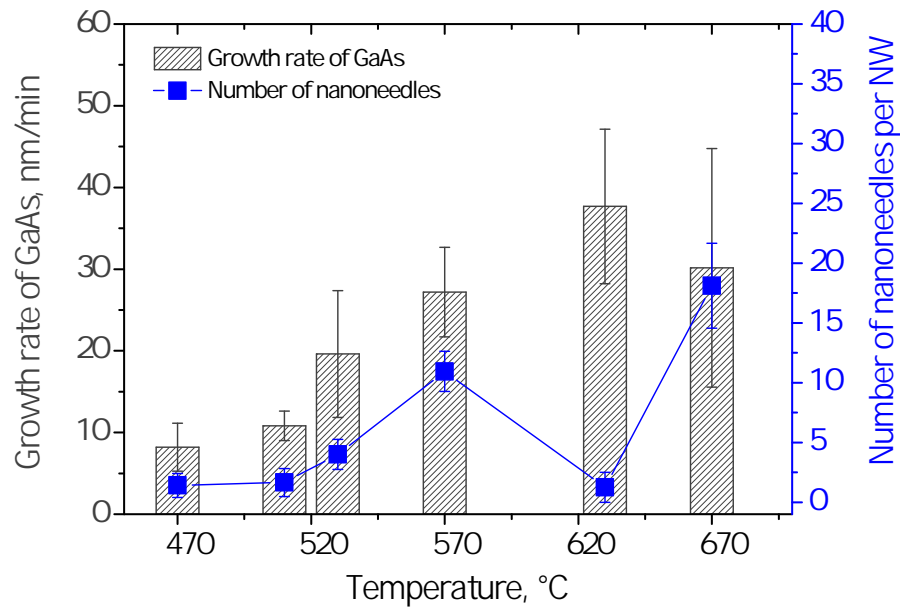


**Figure 4.4:** Au-assisted Si/GaAs nanowires on Si(111) substrate. a)-f) Evolution of the Si/GaAs nanowire morphology with respect to the growth temperature (SEM images, 30° tilt).

nanowire sidewalls. The growth is catalyzed by parasitic tiny Au clusters which were detected on Si nanowire surfaces before growth (Figure 4.3). We observe that an axial GaAs segment grows on Si in the temperature window from 470 °C to 670 °C (see Figure 4.4). The GaAs segments grow at an angle with the Si stems. We attribute the GaAs kinking to the initial position of the gold droplet (see 4.1 a,b), which sits on a tilted facet at the top of the Si nanowire.

In order to estimate the evolution of growth, we measured and plotted the average growth rate of axial GaAs segments and the average number of GaAs nanoneedles per nanowire depending on the growth temperature (see Figure 4.5). We find that the GaAs growth rate increases with temperature until 630 °C (see the chart bar in Figure 4.5). This tendency can be explained by a reduction of the Ga diffusion at low temperatures, similar to the results obtained for Au-assisted GaAs nanowires [115] and for self-assisted GaAs nanowires [116]. Adatom diffusion from the substrate is the major contribution to the elongation of nanowires grown by molecular beam epitaxy [115]. For higher growth temperatures more Ga adatoms diffuse toward the gold catalyst and promote the growth of GaAs segments. Yet, when the growth temperature is too high (more than 630 °C in our case), Ga desorption from the substrate and from the nanowire sidewalls reduces the number of Ga adatoms reaching the droplet, limiting the nanowire growth rate (see the results for 670 °C in the chart of Figure 4.5).

For temperatures below 530 °C the growth of axial GaAs is irregular: not all Si nanowires



**Figure 4.5:** SEM analysis of Si/GaAs nanowire heterostructures. Plot of the average growth rate of axial GaAs segments and the average number of nanoneedles per nanowire (per NW) versus growth temperature.

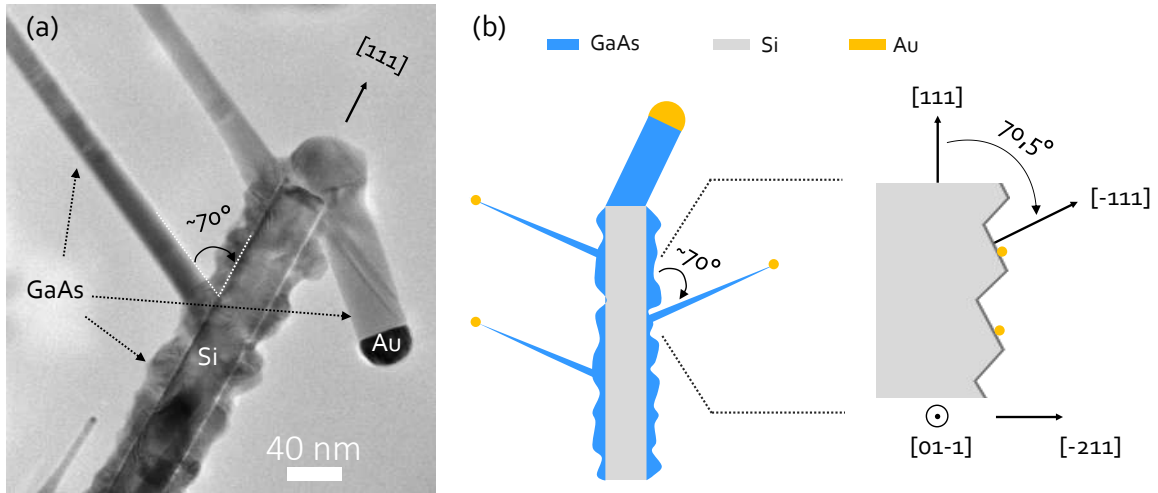
have a GaAs segment on top. Furthermore, not all nanowires have nanoneedles on their sides. On average we find no more than 2 nanoneedles per nanowire for temperatures below 530 °C (see the bar chart in Figure 4.5). As the average number of gold clusters on the Si nanowire surfaces before GaAs growth is 7 per 120 nanometers length, we assume that not all gold clusters give rise to the nanoneedles formation. Apparently, 8 minutes of growth is not enough to initiate the formation of Au-assisted GaAs segments at low temperatures, most likely due to the low diffusivity of Ga adatoms. In order to verify this assumption, another set of samples should be grown for a longer time. We also detect a thick conformal GaAs layer around the Si stems (see Figure 4.4 a,b,c), which further confirms the low diffusivity of Ga adatoms at low temperatures [117, 118].

In contrast, for temperatures above 530 °C, the Ga adatom diffusion is high enough and all nanowires feature an axial GaAs segment after 8 minutes of growth (see Figure 4.4 d,e,f). Furthermore, the number of nanoneedles as well as their length increases significantly at high temperatures (Figure 4.5). In addition, we find that high growth temperatures assist the kinetics of GaAs islands formation on the surface of Si substrates and around Si nanowires due to the high mobility of Ga adatoms. This is in good agreement with the epitaxial growth of GaAs on Si reported in [117].



## 4.4 Structural characterization of Si/GaAs nanowires

We now study the structural properties of our best sample by TEM. We chose the sample grown at 630 °C because it exhibits the smallest number of nanoneedles per nanowire and the highest axial growth rate for GaAs (see Figure 4.6). We aim at better understanding the Si/GaAs interface. Moreover, we want to gain some information about the quality of the GaAs shell covering the Si nanowire surfaces.



**Figure 4.6:** TEM analysis of Si/GaAs nanowire heterostructures grown at 630 °C. a) Bright-field TEM image of a typical Si/GaAs nanowire heterostructure. GaAs nanoneedles grown at an angle of  $\sim 70^\circ$  to the  $[111]$  nanowire growth axis. One of the angles is indicated on the image. b) Schematic illustration of a typical Si/GaAs nanowire (on the left) and an expected faceted sidewall (on the right). The sidewall consists in an upward oriented facet and a downward oriented one. We suppose that the gold parasitic clusters are only anchored on the upward  $\{111\}$ -like facets. The angle between the upward facet and the  $[111]$  growth direction is  $70.5^\circ$ .

Figure 4.6 shows a typical Si/GaAs nanowire heterostructure. We observe a Si stem with a homogeneous diameter, which is surrounded by a rough and thick GaAs shell. The Si stem measures 37 nanometers in diameter. The thickness of the parasitic shell is 17 nm. We find an axial GaAs segment on top of the Si stem with the gold droplet at the tip. The diameter of the GaAs segment is the same as the one of the Si nanowire. Evidently, GaAs is grown from the same gold droplet. Yet, the GaAs segment is kinked and features planar defects (twins). Two nanoneedles are present on the nanowire sidewall with a total length of 780 nm each. The needles are tapered with 25 nm and 5 nm diameters on the bottom and at the tip, respectively. Interestingly, all nanoneedles we found are grown at a  $70^\circ$  angle to the  $[111]$  growth direction (see Figure 4.6). Moreover, we observe a three-fold symmetry in the distribution of nanoneedles on the sides of nanowires: three sidewalls are covered with nanoneedles and alternate with three empty sidewalls (this is particularly noticeable in Figure 4.4 d,f).

It was firstly observed and described by Ross and coauthors [119] that Au-catalyzed Si nanowire sidewalls exhibit so called "sawtooth" faceting. Yet, only three out of the six possible  $\{112\}$ -oriented sidewalls are faceted. In addition, more recently it was found [120] that gold parasitic nanoclusters are present only on the faceted sidewalls (to be more precise: (11-2), (1-21) and (-211) planes), while the other three sidewalls are flat and gold-free. The authors identified that the facets consist of two alternating types: the upward-oriented one ( $\{111\}$ -like facet) and the downward-oriented one (may include several inclinations, namely  $\{115\}$ ,  $\{116\}$ ,  $\{117\}$ ,  $\{113\}$  and  $\{100\}$ ). Moreover, in this work high-resolution scanning transmission electron microscope analysis revealed that the gold clusters are only present on the upward facets.

In our experiments, the GaAs nanoneedles follow a three-fold symmetry: they are only observed on three out of six nanowire sidewalls. Therefore, we speculate that our Si nanowires have a saw-tooth faceting. We measured the angle between the nanowire growth direction and GaAs nanoneedles on a series of nanowires. The angle is always positive and equals to  $70^\circ \pm 2^\circ$ . Within margin of error, it corresponds to the angle between  $[111]$  nanowire growth direction and  $\{111\}$ -upward-oriented facets ( $70,5^\circ$ ). In conclusion, the nanoneedles are most likely grown on the upward  $\{111\}$ -oriented facets thanks to the anchored there gold nanoclusters.

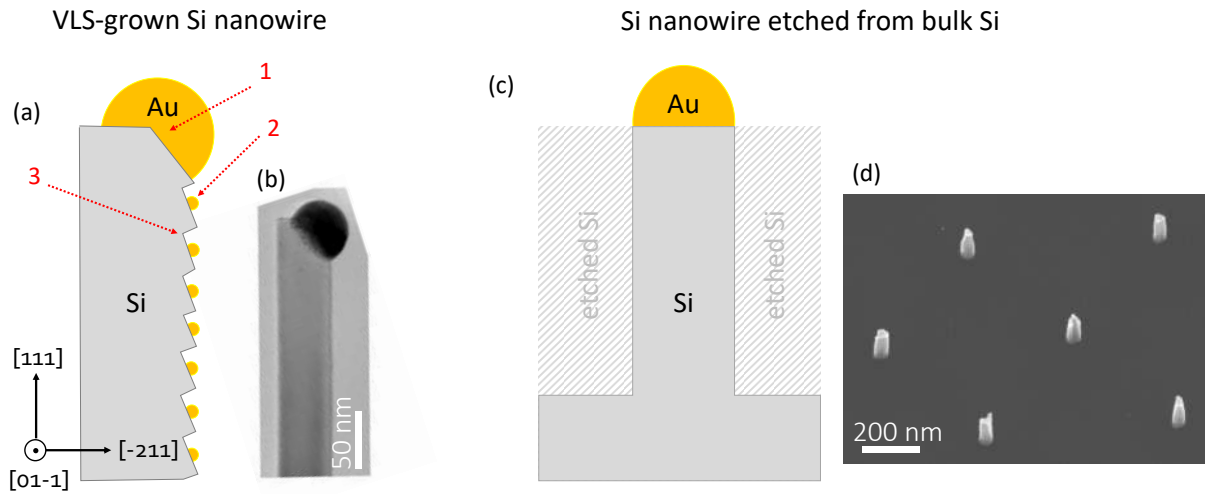
## 4.5 Conclusions and outlook

Prior to the growth of GaAs segments we investigated the efficiency of different chemical treatments to remove the native oxide present on Si nanowire surfaces and on Si substrates. We achieved oxide-free surfaces and showed that the number of parasitic gold clusters present on the Si nanowire sidewalls is decreased significantly after the proposed  $\text{HF}/\text{NH}_4\text{F}$  chemical treatment.

Moreover, we have successfully demonstrated the possibility to grow GaAs segments on top of Si by re-using the gold catalyst present at the Si nanowire tips. We investigated the range of growth temperatures for the GaAs segments and found that it corresponds to the one used for Au-assisted GaAs nanowires grown by molecular beam epitaxy. The growth of GaAs segments was observed in the whole temperature range from  $470^\circ\text{C}$  up to  $670^\circ\text{C}$ . The longest segments were achieved at  $630^\circ\text{C}$ .

Transmission electron microscopy studies of the Si/GaAs nanowire heterostructures revealed that the GaAs segments at the tips of Si nanowires are kinked and have crystalline defects. Moreover, a radial GaAs shell grows around the Si nanowires. In addition, GaAs nanoneedles form at the nanowire sidewalls due to the presence of parasitic gold clusters. By a careful examination of the angle between the nanoneedles growth direction and the Si nanowire growth axis, as well as their presence only on the three facets (the three-fold symmetry), we determined that the sidewalls of Si nanowires are most likely faceted. Furthermore, gold clusters are probably anchored to  $\{111\}$ -upward-oriented facets, promoting the growth of nanoneedles with a constant angle.





**Figure 4.7:** Comparison of Si nanowires obtained by two different methods. a) Schematic illustration and b) bright-field TEM image of a Si nanowire, grown in a low pressure chemical vapor deposition reactor by the vapor-liquid-solid (VLS) method with gold as catalyst. These nanowires are used in the current work. Several issues are indicated: 1) the gold droplet seats at an angle to the top facet which promotes the formation of kinked GaAs segments; 2) diffusion of gold droplets on the nanowire sidewalls and resulting growth of GaAs nanoneedles; 3) enhanced parasitic GaAs shell growth on the sidewalls of the Si nanowires. c) Schematic illustration and d) SEM image (30° tilt) of Si nanowires obtained by etching. The gold colloids are used as a mask to prevent the etch of material underneath and thus to form Si nanowires.

The transmission electron microscopy analysis provided insight into the challenges that we face (Figure 4.7 a):

1. kinking of GaAs segments, attributed to the initial position of Au droplets at the tips of Si nanowires;
2. gold diffusion along the nanowire sidewalls and resulting growth of GaAs nanoneedles catalyzed by gold clusters;
3. parasitic GaAs shell on the sidewalls of Si nanowires.

Taking into account that the challenges are a direct consequence of the vapor-liquid-solid growth of Si nanowires in a low pressure chemical vapor deposition reactor, we expect that the use of a top-down approach, where Si nanowires are etched out of bulk silicon with gold droplets used as a mask (Figure 4.7 c), could help to avoid the listed problems. In order to check our speculation, we performed preliminary studies on reactive-ion etching of Si substrates to obtain Si nanowires (see Figure 4.7 d). The position of gold droplets, which are deposited on the surface of bulk silicon, is unchanged during the entire etching process. Moreover the etching process is

#### 4.5 *Conclusions and outlook*

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performed at relatively low temperatures ( $\sim 50$  °C), which prevents the migration of gold from the droplet to the sidewalls of etched Si nanowires. In addition, we avoid faceting, which is the result of self-assembling in the vapor-liquid-solid growth of nanowires. Yet, the etching process is not straightforward and requires further adjustments to obtain homogeneous Si nanowires that will be used for the growth of GaAs nanowire segments.



## Chapter 5

# Growth of wurtzite GaAs nanowires on Si (111) substrates

In the present work we aim to achieve Au-assisted axial GaAs/InAs nanowire heterostructures for photonic applications at telecommunication wavelengths. We already saw in Chapter 2, that the crystal phase purity of nanowires is crucial for the performance of nanowire-based devices, since defects in crystal stacking act as traps and scattering centers for the charge carriers. Thereby, it is important to minimize the occurrence of the stacking faults during nanowire growth. Moreover, it is important to consider the particular case of InAs-on-GaAs nanowire heterostructures, where "energetically unfavorable" InAs segment has to be grown straight on top of GaAs nanowires. In this case, a GaAs segment with the wurtzite crystal structure may help to stabilize the gold droplet and increase the yield of vertical InAs-on-GaAs nanowires. Indeed, during Au-assisted vapor-liquid-solid growth, wurtzite nanowires only nucleate when the droplet/nanowire interface is planar, whereas truncated facets at the interface produce zinc-blende nanowires [40]. The size of the truncated edge varies during nanowire growth and increases at low supersaturation of the growth species in the gold droplet [106]. Thus, the gold droplet can be destabilized more easily during the group III element switch (when the supersaturation changes drastically) in the zinc blende crystal phase and can slide to the truncated facet, producing kinked nanowires. Thus, constraining the GaAs segment to the wurtzite crystal phase will help to stabilize the droplet on the top, flat facet and increase the yield of vertical InAs-on-GaAs nanowires.

In this chapter, we focus on the growth of pure wurtzite GaAs nanowires grown by Au-assisted vapor–liquid–solid mechanism on Si substrates. Au-assisted GaAs nanowires were previously grown on Si substrates, both by molecular beam epitaxy (MBE) [121, 122, 123, 69, 118] and by metal-organic chemical vapor deposition (MOCVD) [124, 125, 98]. However, non of these works reported pure wurtzite GaAs nanowires. For example, Soshnikov and coworkers [121] observed a mixture of wurtzite and zinc blende crystal phases in Au-assisted GaAs nanowires

grown on Si(111) substrates by MBE. The authors used in-situ reflection high-energy electron diffraction. Similar results were revealed in the work of Ihn and coauthors [122], where the crystal structure analysis of MBE GaAs nanowires was performed by high-resolution transmission electron microscopy (TEM). The authors also observed a pure zinc blende crystal phase for GaAs nanowires grown in the [001] growth direction on Si(111) substrates. Breuer et al. [118] demonstrated that GaAs nanowires grown by MBE on Si substrates nucleate in pure wurtzite phase only upon reaching a certain height caused by defects in the base of GaAs nanowires with a high density of stacking faults. The authors attribute the defective region to the incubation delay: the growth of GaAs nanowires is delayed on Si(111) substrates. This happens due to the lower surface energy of the Au/Si relative to the Au/GaAs system. For the MOCVD growth of GaAs nanowires, high crystalline quality, zinc blende, crystal phase was achieved at relatively low growth temperatures (417 °C) and a high V/III ratio (25) in the work of Bao and his colleagues [125]. The crystal quality of nanowires was studied by high-resolution TEM.

Here, we focus on the growth of pure wurtzite, Au-assisted, GaAs nanowires on Si (111) substrates by MBE. We first study the nucleation process of GaAs nanowires on Si. We then optimize the nanowire morphology and crystal structure purity by varying both the growth temperature and the V/III beam equivalent pressure ratio. The crystal structure characterization analysis is performed by high-resolution TEM.

## 5.1 Substrates preparation

In our experiments, we used  $n^{++}$ -type As doped 2 inch Si substrates. The cleaning treatment of the native silicon oxide prior to nanowire growth was performed by **Method 2**, described in the Chapter 4. For this Si substrates were etched in 1% HF for 1 minute followed by 40 seconds immersion in 40%  $\text{NH}_4\text{F}$  to remove the native oxide and to create atomically flat terraces on the Si surface [112]. After each chemical step, all substrates were rinsed thoroughly in deionized water. The efficiency of the cleaning treatment was determined at the final water rinsing step: a clean silicon surface is hydrophobic and repels water. If drops of water were still sticking to the surface after the chemical procedure, the last chemical step was repeated. After the final water rinsing step, substrates were blown dry with nitrogen.

20 nanometers diameter Au nanoparticles were then deposited onto the substrates using colloidal Au. The typical nanoparticle deposition time was 1 minute. In order to avoid re-oxidation of the surface upon exposure to air during this step, we introduced a drop of 1% HF to the colloidal Au solution on the substrate. Then, the substrates were rinsed thoroughly in high quality deionized water, blown dry with nitrogen, and immediately loaded into the introduction module of the MBE setup. We carried the clean samples from the chemical bench to the MBE reactor using closed beakers filled with nitrogen in order to minimize the contact of silicon surface with air. Before

reaching the growth chamber, the samples were degassed at 200 °C in a high vacuum transfer module until the pressure dropped below  $2 \times 10^{-8}$  Torr.

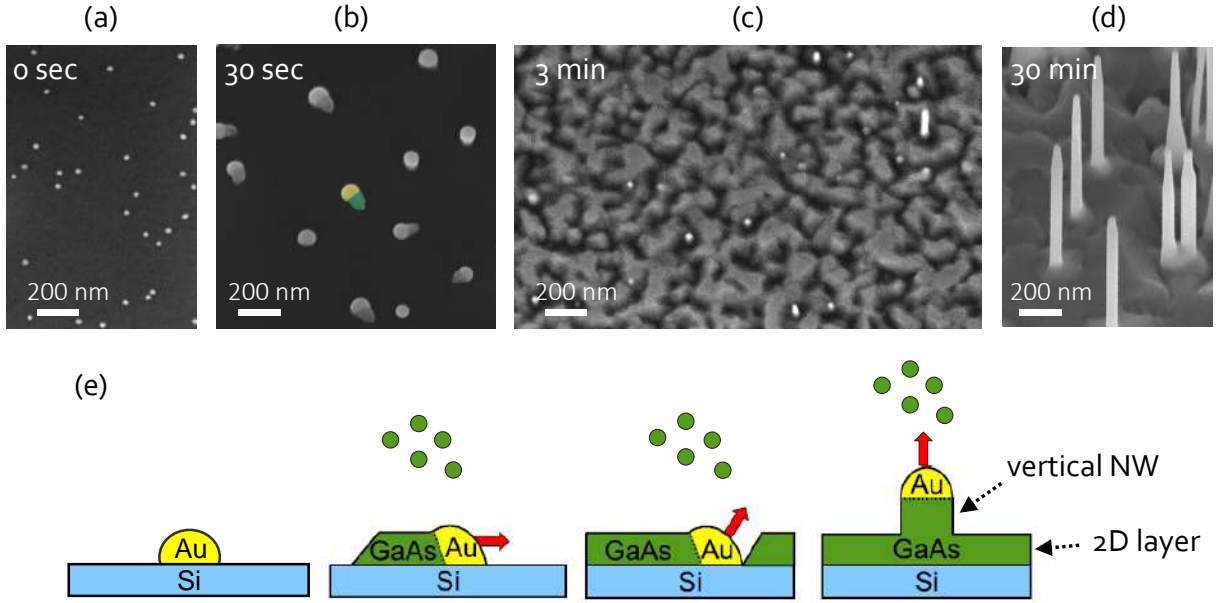
## 5.2 Nucleation of GaAs nanowires on Si substrates

We first studied the nucleation of Au-assisted GaAs nanowires on Si (111) substrates to understand the first stages of the growth at the GaAs/Si heterointerface [118, 126].

We prepared a series of four samples with the same growth parameters, but with different growth time, to study the evolution of the GaAs nanowire growth. The samples were cut from the same, de-oxidized, 2-inch Si wafer. We used fixed Ga and As fluxes of  $0.085 \text{ nm s}^{-1}$  and  $6 \times 10^{-6}$  Torr, respectively. The corresponding Ga flux was found from two-dimensional equivalent growth rate on a GaAs(001) surface. The corresponding V/III beam equivalent pressure ratio is 30. The samples were heated to a growth temperature of 610 °C with a ramp of  $40 \text{ °C min}^{-1}$ . The first sample was left with Au droplets and without any GaAs deposition. The growth of GaAs segments was performed during 30 seconds, 3 minutes and 30 minutes for the remaining samples. After growth, both the gallium shutter and the arsenic valve were closed and the substrate was cooled down to the room temperature. The morphology of grown samples was analyzed by scanning electron microscopy (SEM).

Figure 5.1 a)-d) shows the evolution of surface/nanowire morphology as a function of growth time. Before the deposition of GaAs, Au droplets are homogeneously dispersed on the substrate (Figure 5.1 a). The 30 seconds GaAs growth yielded no nanowires or crystal islands on the substrate (Figure 5.1 b). Instead we see large gold droplets which are larger than the diameter of the colloid. Some droplets show a notable GaAs "trace" laying on the substrate surface. After 3 minutes of growth, the Si substrate is almost fully covered by the GaAs traces which coalesce and form a partial, two-dimensional, layer (Figure 5.1 c). Small gold droplets can be detected on top of GaAs traces thanks to their brighter contrast. Only few vertical, thin nanowires are formed in this stage. Finally, after 30 minutes of growth, thin GaAs nanowires and a thick closed two-dimensional layer of GaAs are present (Figure 5.1 d).

From our observations, we conclude that the GaAs nanowire formation on Si (111) substrate is delayed in time. Such growth behavior was first observed and explained in the work of Breuer and coauthors [118]. Particularly, they report that vertical growth of GaAs nanowires takes place only after the whole Si surface is covered by Au-assisted GaAs in-plane traces (Figure 5.1 d). The traces appear due to lower interface energy of Au-Ga droplet on Si (111) substrate ( $\gamma \leq 35 \text{ meV \AA}^{-2}$ ) compared to Au-Ga droplet on GaAs (111)B substrate ( $\gamma \geq 43 \text{ meV \AA}^{-2}$ ). Therefore, the Au-Ga droplet remains in contact with the Si surface in order to minimize the surface energy. Our results are consistent with those reported by Breuer et al. First, in-plane GaAs traces form,



**Figure 5.1:** Evolution of Au-assisted GaAs nanowire growth on Si (111) substrate. SEM images (30° tilt) of GaAs nanowires before growth (a) and after 30 seconds (b), 3 minutes (c), 30 minutes (d) of growth. e) Schematic of the growth model proposed in [118]. GaAs is shown in green, Au droplet - in yellow, Si substrate - in blue.

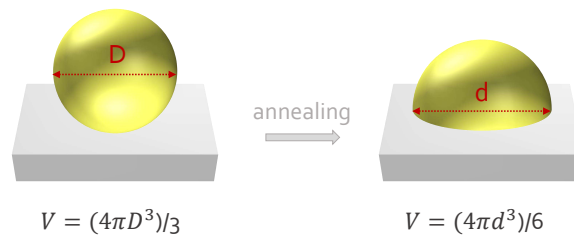
elongate and enlarge, eventually covering the whole Si surface. Then, vertical GaAs nanowires appear after 3 minutes of growth.

Interestingly, an increase in the gold droplets diameter can be seen after 30 seconds (Figure 5.1 b). To estimate the magnitude of the change, we measured the droplets diameter for each of the four samples. Recently deposited Au colloids have  $20 \pm 2$  nanometers diameter. After 30 seconds of GaAs deposition time, two types of gold droplets can be distinguished: relatively small and motionless droplets on the Si surface and bigger droplets which move in plane, followed by GaAs traces. The diameter of the droplets is  $37 \pm 7$  and  $67 \pm 9$  nanometers, respectively, and far exceeds the diameter of the initially deposited nanoparticles. After 3 minutes of growth, however, the diameter of the Au droplets at the tip of the GaAs nanowires is  $20 \pm 4$  nanometers recovering its initial value. After 30 minutes of growth, the droplet diameter remains constant at  $22 \pm 3$  nanometers.

To understand the diameter enlargement of the Au droplets after 30 seconds of growth, we first evaluate the shape of the droplet before and after thermal annealing on the Si substrate (Figure 7.8). When Au droplets are deposited from the colloidal solution they have a spherical shape and a diameter  $D$ . Once the substrate temperature increases to  $610^\circ\text{C}$  under vacuum, however, the liquid Au droplet alloys with silicon from the substrate (Si atoms diffuse to the liquid droplet,

## 5.2 Nucleation of GaAs nanowires on Si substrates

while Au atoms diffuse to the Si substrate) and adopts a hemispherical shape with diameter  $d$ . Assuming the volume of the droplet  $V$  remains unchanged, the diameter will increase by  $2^{1/3}$  for the hemisphere liquid droplet. The final diameter of the Au droplet at the growth temperature before GaAs deposition should be about 25 nanometers.



**Figure 5.2:** Modification of the Au droplet diameter after thermal annealing: the shape changes from sphere with diameter  $D$  to hemisphere with diameter  $d$ . Droplet volume  $V$  remains unchanged.

Secondly, Ga solubility in the liquid Au droplet must be taken into account after the growth begins. It was demonstrated experimentally by high-resolution TEM analysis, that Au droplet accumulates up to 50% of Ga during growth of Au-assisted GaAs nanowires on GaAs (111)B substrates [127]. Moreover, according to the Au-Ga phase diagram (Figure 2.2), there exists an even more Ga-rich Au-Ga phase with 67 atomic % of Ga.

In our experiment, after 30 seconds of growth (which is equivalent to two-dimensional layer with 2.55 nanometers thickness) the diameter of Au droplets increases by 32% and 63% for the motionless droplets and the droplets with GaAs traces, respectively. The Si substrate does not show any sign of additional GaAs islands. We assume that the increase in the droplet diameter during GaAs deposition occurs due to high Ga accumulation in the liquid Au droplet. It was experimentally observed [127] that a pure Au droplet has a face centered cubic lattice ( $a_{Au} = 0.408$  nm), while an Au-Ga 50%-50% alloy has an orthorhombic lattice ( $a_{Au/Ga} = 0.640$  nm,  $b_{Au/Ga} = 0.627$  nm and  $c_{Au/Ga} = 0.345$  nm). The crystal structure change leads to the change in the volume of a unit cell and in the volume of the droplet finally. Indeed, the unit cell volume of pure Au is  $V_{Au} = a_{Au}^3 = 0.069$  nm<sup>3</sup>, while the unit cell volume of Au-Ga alloy is  $V_{Au} = a_{Au-Ga} \times b_{Au-Ga} \times c_{Au-Ga} = 0.138$  nm<sup>3</sup>, making the final droplet volume increase by a factor of two. Taking into account that Au droplet diameter is 25 nanometers before the growth, we estimate the diameter of Au-Ga 50%-50% droplet to be 33 nanometers. Within the margin of error, it corresponds to the diameter of motionless droplets (Figure 5.1 b). Since droplets with a GaAs trace have an even bigger diameter, we speculate that concentration of Ga in the liquid droplet exceeds 50% at the time of GaAs nucleation at the droplet/trace interface. Indeed, according to the phase diagram, an Au-Ga-As alloy with 40% of Ga is liquid at growth temperatures above 550 °C. Moreover, the Ga solubility in the liquid alloy is no more limited.



After 3 minutes of growth, when the entire Si surface is covered by GaAs traces and droplets are located on top of GaAs, the diameter of Au droplets decreases and equals  $\sim 20$  nanometers. This phenomenon can be explained by energetic considerations at the Au/Si and Au/GaAs interfaces. The interface energy of a Au-Ga droplet on a Si (111) surface is lower than the interface energy of the same droplet on a GaAs surface [118]. This means that Au-Ga droplet will tend to minimize its surface contact with GaAs compared to Si. To do so, it can either i) increase contact angle to wet less the surface and/or ii) expel Ga (decrease Ga concentration) in order to shrink. Based upon the first assumption, additional TEM analysis has to be performed to measure the contact angle of the Au droplet on Si after 30 seconds of growth and on GaAs after 3 minutes of growth. Yet, results reported in the literature indeed demonstrate clear trend for the Au droplet to wet less the GaAs surface: the contact angle of Au droplet on a Si (111) substrate is found to be  $\sim 43^\circ$  [128, 118], while on a GaAs (111) substrate the contact angle equals or exceeds  $90^\circ$  [50, 129]. The second assumption seems to be satisfied for our experiments. However, additional investigation of samples by energy dispersive x-ray spectroscopy would help to estimate the Ga concentration after 30 seconds and 3 minutes of growth.

In conclusion, we observed an incubation delay of Au-assisted GaAs nanowires grown on Si (111) substrates in good agreement with the results reported by Breuer et al [118]. First, few nanowires were found on the substrate after only 3 minutes of GaAs deposition. After 30 minutes of growth the number and length of nanowires was increased. The delay in nanowires growth is due to the formation of horizontal Au-assisted GaAs traces. Only after the traces cover the entire Si surface, nanowires growth begins.

### 5.3 Influence of the growth temperature

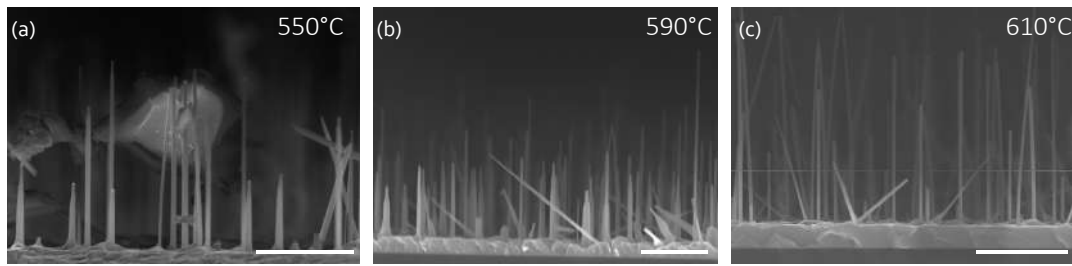
We performed the growth of three samples at different growth temperatures to study thermal influence on the morphology of GaAs nanowires. We chose the following three temperature points: 550, 590 and 610  $^\circ\text{C}$ . The nanowire growth rate as a function of temperature reaches a maximum and rapidly decreases after that due to adatom desorption at high temperatures [115, 116]. For the current experiment, taking into account results from Chapter 4, we intentionally chose the upper temperature of 610  $^\circ\text{C}$  to be below the Ga desorption range.

Si substrates were prepared as described in section 5.1. We used fixed Ga and As fluxes of  $0.085 \text{ nm s}^{-1}$  and  $6 \times 10^{-6} \text{ Torr}$ , respectively. The corresponding Ga flux was found from a two-dimensional equivalent growth rate on GaAs(001) surface. The corresponding V/III beam equivalent pressure ratio is 30. We heated the samples to the desired growth temperature with a ramp of  $40 \text{ }^\circ\text{C min}^{-1}$ . After one minute of stabilization, both the arsenic cracker cell valve and the gallium shutter were opened simultaneously. We performed the growth of GaAs nanowires in 30

### 5.3 Influence of the growth temperature

minutes. After growth, the gallium shutter was closed and the samples were cooled down under an arsenic flux.

Figure 5.3 shows side view SEM images of nanowires grown at 550, 590 and 610 °C. Essentially all the nanowires grow perpendicular to the substrate surface. At 550 °C (5.3 a) nanowires exhibit high variation in length: thick nanowires are short while the thinner ones are significantly longer. We observed that nanowires are tapered with a large diameter variation along the growth axis. Raising the growth temperature to 590 °C generally did not improve the nanowire morphology (5.3 b). These nanowires feature an inhomogeneous distribution in length and tapering along the growth direction similar to those grown at 550 °C. A significant improvement in the nanowire morphology is achieved at 610 °C (Figure 5.3 c). The GaAs nanowires grown at this temperature are thin and homogeneous in diameter along the entire length.



**Figure 5.3:** Evolution of GaAs nanowire morphology with growth temperature. SEM images (side view, scale bar 1  $\mu\text{m}$ ) of Au-assisted GaAs nanowires grown at (a) 550 °C, (b) 590 °C and (c) 610 °C.

Around 12 nanowires per sample were measured for their length  $L$  and diameters at the bottom  $d_b$  and on the top  $d_t$ . From these measurements we calculated fluctuations in length  $\delta L$  and diameter  $\delta d$  and growth rate  $\frac{dL}{dt}$ . The results are summarized in Table 5.1.

T, °C	$\langle L \rangle$ , nm	$\delta L$ , %	$\frac{dL}{dt}$ , nm/sec	$d_b$ , nm	$d_t$ , nm	$\delta d$ , %
550	$1260 \pm 526$	42	$0.7 \pm 0.3$	$66 \pm 15$	$26 \pm 6$	60
590	$1136 \pm 333$	29	$0.6 \pm 0.2$	$84 \pm 35$	$29 \pm 6$	65
610	$1897 \pm 429$	23	$1.0 \pm 0.2$	$30 \pm 6$	$26 \pm 4$	13

**Table 5.1:** Influence of the growth temperature on the morphology of Au-assisted GaAs nanowires on Si(111) substrates.

The maximum nanowire growth rate is achieved at 610 °C ( $\sim 1.0 \text{ nm s}^{-1}$ ). Furthermore, we see from the Table 5.1 that the nanowires grown at 610 °C feature the smallest fluctuations in length  $\delta L$  and diameter  $\delta d$ . Increase in growth rate and decrease in tapering with growth temperature correlates with the results of GaAs/Si nanowire growth (Chapter 4).

We notice that the average growth rate of nanowires is always significantly higher than the deposition growth rate ( $0.085 \text{ nm s}^{-1}$ ) in the chosen interval of growth temperatures. This is

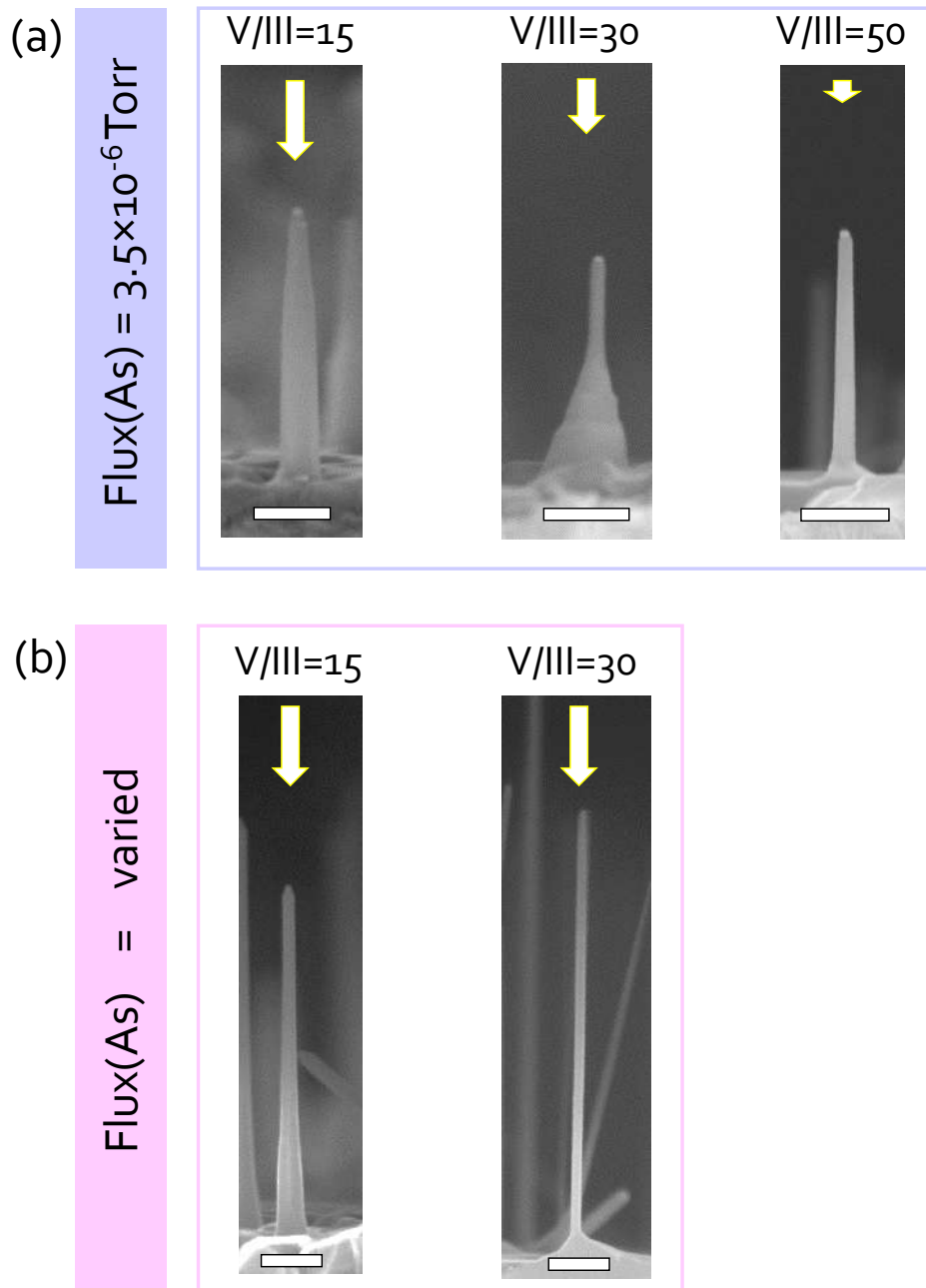
typical for the diffusion-induced growth mechanism when the nanowire growth is controlled by the adatom surface diffusion [115]. In addition, we observe that the nanowire length decreases with the nanowire diameter for all samples what confirms the diffusion-induced nature of the growth. At the chosen growth temperature window the desorption of Ga from the nanowire sidewalls can be neglected. This means that the nanowire growth rate is limited only by adatom surface diffusion: at high growth temperatures the diffusion of Ga adatoms is increased, what promotes high axial growth.

Given that the best nanowire aspect ratio was found at 610 °C, we kept this growth temperature for further experiments. We then performed a series of studies on the influence of Ga and As fluxes and the V/III flux ratio on the morphology of nanowires.

## 5.4 Influence of the As, Ga fluxes and the overall V/III flux ratio

In this section, we study the influence of both the As and Ga fluxes on the nanowire growth rate and morphology. For the first set of samples, we kept a constant As flux of  $3.5 \times 10^{-6}$  Torr and varied Ga flux to obtain V/III beam equivalent pressure ratios of 15, 30 and 50. The corresponding Ga flux is  $2.3 \times 10^{-7}$ ,  $1.2 \times 10^{-7}$  and  $0.7 \times 10^{-7}$  Torr, respectively. For the second set of samples, we fixed Ga flux at  $2.0 \times 10^{-7}$  Torr and varied As flux to obtain the same V/III beam equivalent pressure ratios of 15, 30 and 50. The growth temperature and growth time for all experiments were fixed at 610 °C and 30 minutes. The sample grown in the second set of samples at V/III ratio 50 was lost during the annealing step and, thus, is not considered hereafter. Figure 5.4 summarizes the results.

We now focus on the results obtained for the first set of samples. Figure 5.4 a) shows the evolution of the nanowires morphology with decreasing Ga flux (increasing V/III ratio). At a V/III ratio of 15, the nanowires are tapered with a large diameter variation along the growth axis (see Table 5.2). We measured an average length of  $690 \pm 60$  nanometers. At a V/III ratio of 30, the tapering is localized along the first half of the nanowire. We find the nanowire total length of  $831 \pm 286$  nanometers with large fluctuations. Nanowires with significantly improved morphology were found for V/III ratio of 50 (the lowest Ga deposition rate). The nanowires length slightly decreases compared to the lower V/III ratio samples and is found to be of  $562 \pm 207$  nanometers with large fluctuations. Importantly, for all the samples the growth rate is higher than the nominal two-dimensional deposition rate, and the nanowire length is increased with decreased nanowire diameter, indicating the diffusion-induced growth mechanism. This means that the growth rate of the nanowires depends on the diffusion flux of Ga adatoms. The desorption of Ga adatoms is negligible at the chosen growth temperatures.



**Figure 5.4:** Evolution of the GaAs nanowire morphology versus the As and Ga fluxes. SEM images (side view, scale bar 200 nm) of nanowires grown at a fixed As flux of  $3.5 \times 10^{-6} \text{ Torr}$  for different Ga fluxes (a), and at a fixed Ga flux of  $2.0 \times 10^{-7} \text{ Torr}$  for different As fluxes (b). The corresponding V/III beam equivalent pressure ratio is specified on the top of each image. The size of the white arrows indicates the relative changes in Ga flux.

V/III ratio	Ga flux, Torr	$\langle L \rangle$ , nm	$\frac{dL}{dt}$ , nm/sec	$d_b$ , nm	$d_t$ , nm
15	$2.3 \times 10^{-7}$	$690 \pm 61$	$0.38 \pm 0.03$	$118 \pm 23$	$24 \pm 4$
30	$1.2 \times 10^{-7}$	$831 \pm 286$	$0.46 \pm 0.16$	$162 \pm 60$	$22 \pm 4$
50	$0.7 \times 10^{-7}$	$562 \pm 207$	$0.31 \pm 0.11$	$61 \pm 10$	$22 \pm 3$

**Table 5.2:** Influence of Ga flux on the morphology of Au-assisted GaAs nanowires on Si(111) substrates. As flux is fixed at  $3.5 \times 10^{-6}$  Torr for all samples.

V/III ratio	As flux, Torr	$\langle L \rangle$ , nm	$\frac{dL}{dt}$ , nm/sec	$d_b$ , nm	$d_t$ , nm
15	$3.0 \times 10^{-6}$	$1402 \pm 312$	$0.78 \pm 0.17$	$107 \pm 32$	$22 \pm 4$
30	$6.0 \times 10^{-6}$	$1488 \pm 355$	$0.8 \pm 0.2$	$25 \pm 5$	$25 \pm 3$

**Table 5.3:** Influence of As flux on the morphology of Au-assisted GaAs nanowires on Si(111) substrates. Ga flux is fixed at  $2.0 \times 10^{-7}$  Torr for all samples.

Notice that the nanowire length does not increase proportionally to the Ga flux (decreasing V/III ratio): the higher Ga flux has no (or very little) effect on the axial growth rate. On the other hand, the radial growth around the GaAs stems is increased with increased Ga flux. This means, that at the chosen growth parameters the axial growth rate is limited by group-V species and the local V/III flux ratio in the droplet is smaller than unity [130, 131]. Since the As flux is kept constant, increase in Ga flux (decrease in V/III flux ratio) leads to the radial overgrowth and, consequently, tapered nanowires are formed.

The second set of samples was grown at a constant Ga flux of  $2.0 \times 10^{-7}$  Torr ( $\sim 0.085$  nm s<sup>-1</sup>) and As flux was varied instead. Figure 5.4 b) along with Table 5.3 summarizes the results. Essentially, all the nanowires feature longer segments in comparison with the first set of samples. Nanowires grown at a lower As flux (V/III ratio of 15) still feature a noticeable tapering with large diameter variation along the nanowire axis. Doubling the As flux to obtain V/III ratio of 30 resulted in long thin nanowires with an homogeneous diameter throughout the entire length. We find a short tapered base at the bottom of nanowires.

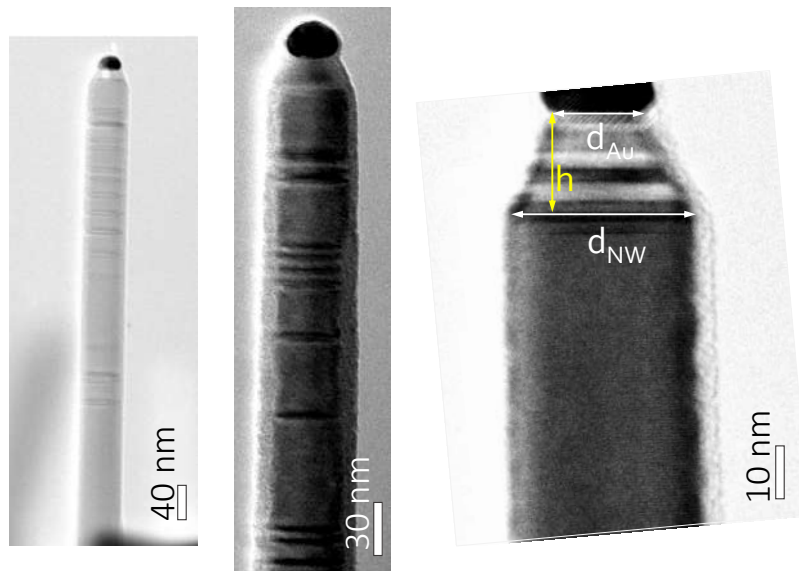
We notice that the nanowire length is increased with increased As flux (increased V/III flux ratio). This observation confirms that the axial growth rate is group-V dependent. At lower As flux (V/III=15) the nanowires feature visible tapering, while at higher As flux (V/III=30) only a small tapered base close to the substrate surface is found. It has been well documented, that the diffusion length of Ga adatoms depends on the V/III overall pressure ratio [132] and is decreased at high As fluxes. The decreased diffusion length of Ga adatoms from the substrate to the nanowire sidewalls leads to a small tapered base, which we observe for the V/III ratio of 30.

Based on our experimental findings, we conclude that the axial growth rate is group-V limited and is increased with increased As flux. Higher Ga flux at a constant As flux has almost no influence on the nanowire growth rate but provokes radial overgrowth instead. To grow thin, long

and homogeneous in diameter nanowires high V/III ratios and a moderate Ga flux are required.

### 5.5 Structural characterization of GaAs nanowires

Figure 5.5 shows TEM images of Au-assisted GaAs nanowires grown at a V/III ratio of 15 from Figure 5.4 b. We find that the major part of the nanowire has wurtzite crystal structure but exhibits a high density of stacking faults. The distribution of stacking faults is not homogeneous along the nanowire axis. Moreover, the number of stacking faults varies from nanowire to nanowire. The nanowires have tapered tips with a catalyst droplet diameter being smaller than the nanowire diameter. The nanowire diameter  $d_{NW}$ , the droplet diameter  $d_{Au}$  and the length of tapering  $h$  analyzed from TEM images are summarized in Table 5.2. In addition, taking into account the length of the tapered segment and the cooling rate ( $40\text{ }^{\circ}\text{C min}^{-1}$ ), we calculated the growth rate of the tapered segment  $\frac{dL_t}{dt}$ .



**Figure 5.5:** Bright-field TEM images of typical Au-assisted GaAs nanowires grown at a Ga flux of  $2.0 \times 10^{-7}$  Torr, a V/III flux ratio of 15 and a growth temperature of  $610\text{ }^{\circ}\text{C}$ . Many stacking faults are visible along the growth axis. The diameter of the nanowire  $d_{NW}$ , the diameter of the Au droplet  $d_{Au}$  and the length of the tapered section  $h$  are indicated.

At a higher V/III flux ratio of 30 (Figure 5.6), the nanowires grow with a pure wurtzite crystal phase, as observed on the selected area diffraction pattern. The nanowires have less than four stacking faults per micrometer. We observe a slight tapering at the tips of the nanowires, similar to the nanowires grown at low V/III ratio. The crystal structure switches from wurtzite to zinc blende in the tapered section right below the gold droplet. The average values of nanowire diameter  $d_{NW}$ ,

droplet diameter  $d_{Au}$ , the length of tapering  $h$  and the growth rate  $\frac{dL_t}{dt}$  of the tapered segment are shown in Table 5.4.

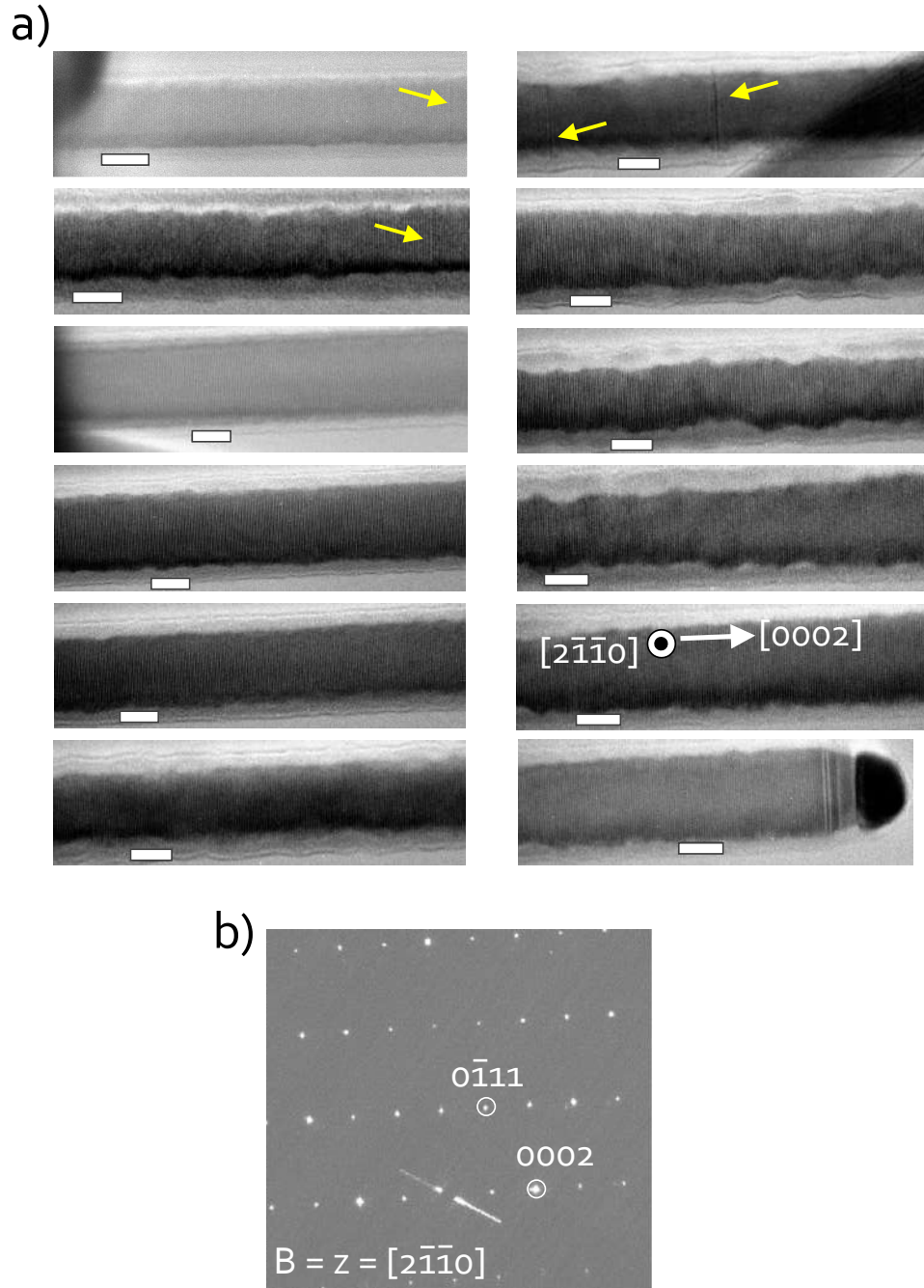
Sample	$d_{NW}$ , nm	$d_{Au}$ , nm	$h$ , nm	$\frac{dL_t}{dt}$ , nm min <sup>-1</sup>
V/III = 15	$37 \pm 10$	$19 \pm 3$	$14 \pm 3$	$2.7 \pm 0.57$
V/III = 30	$23 \pm 3$	$19 \pm 3$	$6 \pm 2$	$1.14 \pm 0.38$

**Table 5.4:** Influence of the V/III flux ratio on the constriction of nanowire tips.

Interestingly, we notice that nanowires grown at the V/III ratio of 15 have larger diameters than the ones at the V/III ratio of 30. Moreover, while nanowires from both samples exhibit characteristic narrowing in diameter right below the catalyst droplet (Figure 5.5 and 5.6), the length of this narrow segment varies (see Table 5.4). We find, that this segment is approximately two times shorter for nanowires grown at a higher V/III flux ratio. The origin of this tapered segment is related to the growth termination procedure. It is well documented, that nanowires cooled under As flux while Ga flux is switched off feature a so-called "cooling neck" [133, 127]. The neck is formed by precipitation of Ga accumulated during growth in the catalyst droplet and usually features a zinc blende crystal phase due to decreased supersaturation. The nanowire growth is possible owing to the ambient As which is supplied during the cooling step, yet the growth is group-III limited. The higher the concentration of available Ga in the catalyst droplet, the faster the GaAs segment is formed below the droplet. We find that the cooling neck at V/III flux ratio of 30 is formed at the growth rate of  $1.14 \pm 0.38$  nm min<sup>-1</sup>, which is 2.4 times slower than at the lower V/III flux ratio of 15. This observation confirms that at a V/III flux ratio of 15, the catalyst droplet contains more Ga compared to the droplet at a V/III flux ratio of 30. A similar trend was reported in the work of Zhang and coworkers for Au-assisted InAs nanowires grown with MBE [134].

We now try to understand why the purity of the crystal structure is significantly improved at higher V/III flux ratio (higher As flux). One possible explanation is that the wurtzite crystal structure requires a high group-V supersaturation at the particle as suggested by Glas [50]. On the other hand, we saw in Chapter 2 that the catalyst droplet geometry (more precisely - its contact angle) is responsible for the crystal structure phase selection in III-V nanowires. The catalyst contact angle is, in turn, dependent on the V/III flux ratio. For molecular beam epitaxy growth, low V/III flux ratios assist formation of Ga-rich catalyst droplets with large contact angles and zinc blende nanowires. Conversely, at high V/III flux ratios the catalyst droplet has a moderate size with a decreased contact angle compared to those with low V/III ratios: wurtzite nanowires are favorable in this case (see, for example, [135]). A decrease in the V/III flux ratio from 30 to 15 increases the droplet size and contact angle and provokes the formation of thicker nanowires with stacking faults.





**Figure 5.6:** a) Bright-field TEM images (scale bar 10 nm) of an individual Au-assisted GaAs nanowire grown at a Ga flux of  $2.0 \times 10^{-7}$  Torr, a V/III flux ratio of 30 and a growth temperature of 610 °C. The wire has a wurtzite crystal structure as shown on the electron diffraction pattern (b) with four stacking faults per entire length (marked by the yellow arrows). The region directly below the gold particle features a ‘cooling neck’ with a zinc blende crystal phase.



## **5.6 Conclusions**

In this chapter, we investigated the nucleation process of Au-assisted GaAs nanowires on Si (111) substrates. We observed that the nucleation is delayed and first nanowires are grown only after 3 minutes of GaAs deposition. Before that time, in-plane GaAs traces form, grow horizontally and eventually cover the entire substrate surface.

Moreover, we studied the influence of the growth parameters on the GaAs nanowire morphology and crystal structure. We found that GaAs nanowires grow for all chosen substrate temperatures (550, 590 and 610 °C). Yet, nanowires feature the smallest fluctuations in height and diameter and grow with the highest growth rate at 610 °C. An increase in Ga flux at a constant As flux has little effect on the axial growth rate but provokes radial overgrowth. In contrast, increasing As flux at a constant Ga flux, we observed an increase in the nanowire growth rate. This observation confirmed that the nanowire growth is group-V determined. In general, we established that high V/III flux ratios are necessary to obtain GaAs nanowires with uniform diameters and minimized tapering. Moreover, a high V/III ratio significantly suppresses the formation of stacking faults in wurtzite Au-GaAs nanowires grown on Si (111) substrates.

## Chapter 6

# Growth of InAs-on-GaAs nanowire heterostructures

The present chapter is devoted to the step by step optimization of the growth parameters to achieve high crystalline quality, straight InAs-on-GaAs nanowire heterostructures. We already know from Chapter 2, that growth of nanowire heterostructures is challenging. Problems such as kinking in one of the two interface directions, graded and asymmetric interfaces and parasitic radial overgrowth arise during particle-assisted axial nanowire growth. Moreover, crystalline quality at the interface is strongly affected by strain caused by the lattice mismatch, which imposes severe conditions on the choice of the nanowire diameter. In theory, dislocations free InAs/GaAs interfaces (7% lattice mismatch) can be produced in nanowires with diameters below 40 nanometers. Yet, only few articles have reported the growth of InAs-on-GaAs axial nanowire heterostructures, reflecting how challenging it is.

Straight nanowire segments are observed when GaAs is grown on top of an InAs stem. The reverse case is found to be energetically unfavorable: InAs kinks when grown on top of a GaAs stem. The first growth of GaAs-on-InAs nanowire heterostructures was achieved already in 1996 by Hiruma and his colleagues [136]. The authors used a MOCVD reactor to synthesize nanowires. The growth was catalyzed by Au droplets prepared on InAs substrates. However, the nanowires exhibited a poor crystalline quality at the interface due to the presence of misfit dislocations despite an interface of 20 nanometers in diameter. Other examples of straight GaAs-on-InAs nanowires can be found in the works of Paladugu and coworkers [72, 73] as well as Dick and coauthors [71, 60]. All authors observe that growth in the reverse direction (InAs-on-GaAs), however, is difficult and that the InAs segments kink or wrap around the GaAs stems due to a higher interface energy between Au and InAs than between Au and GaAs.

One way to prevent kinking at the GaAs/InAs interface is to use graded InGaAs buffer layers between GaAs and InAs [84, 137]. However, the method severely limits the use of such structures

since sharply defined thin barriers or ultra-thin quantum dots cannot be realized in this case. Another interesting way to avoid kinking was demonstrated by Scarpellini and his colleagues [82]. They performed MBE growth of self-assisted InAs-on-GaAs nanowires. Liquid Ga droplets assisted the growth of the GaAs nanowires, while solid In droplets assisted the growth of the InAs segments. Such method, furthermore, helped to avoid interface grading and parasitic radial growth of InAs around GaAs. However, a network of misfit dislocations was observed at the interface between the segments. It remains unclear whether the formation of thin nanowires (and therefore dislocation-free interfaces) is possible with this technique.

Messing and coauthors demonstrated that the probability of kinked InAs segments can be decreased down to 40% if the diameter of the nanowires increases to 100 nanometers and if the nanowires grow in the wurtzite crystal structure [74]. Nanowire heterostructures were grown in a MOCVD reactor on GaAs(111)B substrates. Diameters of 100 nanometers are yet undesirable in heterostructures with  $\sim 7\%$  lattice mismatch due to a higher probability of forming misfit dislocations at the interface. A different approach on the growth of straight InAs-on-GaAs nanowires was proposed recently by Zannier and her colleagues [75]. The nanowires were grown in a chemical beam epitaxy reactor on GaAs(111) B substrates. The authors showed that the yield of straight InAs segments on top of the GaAs stems increases significantly at high III-to-Au ratios. They pre-deposited In before the growth of GaAs nanowires. This led to an increase of the Ga solubility in the Au droplet from 33% to 45% and to an increase of the vertical yield of InAs-on-GaAs nanowires. Unfortunately, the crystalline quality of the interfaces was not studied and there is no available information on whether the misfit dislocations are formed at the interface in this case.

In this chapter we successfully grew straight Au-assisted InAs-on-GaAs nanowire heterostructures on Si (111) substrates by MBE. First, we developed a two-step growth procedure to enhance the yield of vertical InAs-on-GaAs nanowires. In addition, we investigated the influence of the growth temperature on the yield of vertical InAs segments. We then optimized the nanowire morphology and the crystal structure purity using different In fluxes. We investigated the composition of the interface by energy dispersive x-ray spectroscopy (EDX) and the nanowire crystal structure by transmission electron microscopy (TEM). Finally, we propose different strategies to control the chemical composition of the InAs segment.

EDX measurements presented in Figures 6.6, 6.7, 6.15 and 6.16 were performed by Eric Robin at CEA. I took high resolution TEM measurements at NEEL institute. High resolution HAADF STEM measurements were done by Martien den Hertog at CEA and by Marcel Verheijen at Philips Research Eindhoven.

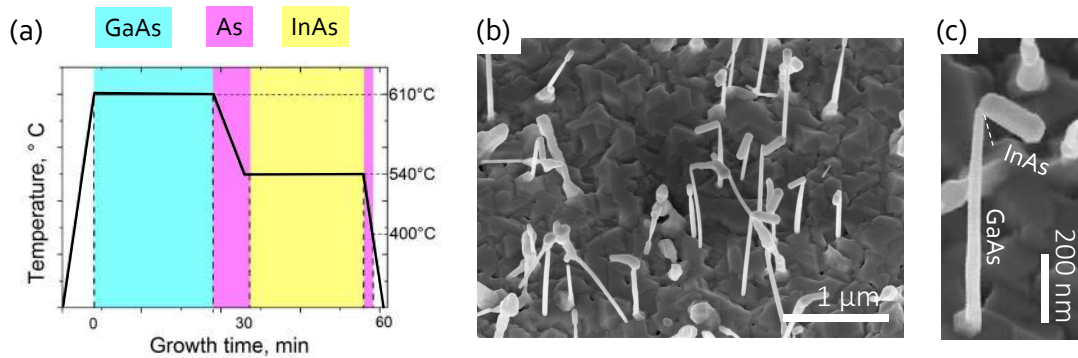
## 6.1 Optimization of the growth protocol

All samples discussed hereinafter were prepared in the same way as described in chapter 5.1. We used 20 nanometers gold colloids and the GaAs segments were grown in the wurtzite crystal structure. To do so, we used Ga and As fluxes of  $0.085 \text{ nm s}^{-1}$  and  $6 \times 10^{-6} \text{ Torr}$ , respectively. The growth temperature was set to  $610^\circ\text{C}$ . More details about the growth of wurtzite GaAs nanowires can be found in Chapter 5.

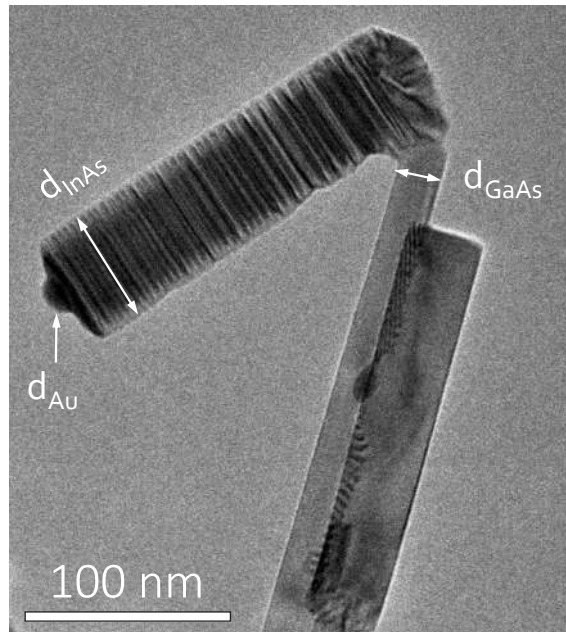
The growth temperature of InAs nanowires by MBE is significantly lower than that of GaAs nanowires. Moreover, the growth temperature window is much narrower. Tchernycheva and coauthors established experimentally, that MBE InAs nanowires grow only at temperatures between  $380^\circ\text{C}$  and  $430^\circ\text{C}$  with a maximum growth rate at  $410^\circ\text{C}$  [138]. Similar results can be found in the work by Martelli et al [139]. Interestingly, the growth temperature of InAs segments grown on top of GaAs stems is usually higher. For example, Messing and her colleagues carried out the growth of InAs segments at  $500^\circ\text{C}$  [74]. Growth temperatures as high as  $530^\circ\text{C}$  were used in the work of Zannier et al [75].

The most straightforward way to grow of semiconductor segments at different temperatures is to use a growth interruption while changing the temperature. Indeed, growth interruptions are known to improve the abruptness of nanowire heterointerfaces [25, 81] and are widely implemented for different semiconductor combinations (see, for example, ref. [71]). Therefore, we interrupted the growth of GaAs during the cooling procedure between the GaAs segment grown at high temperature ( $610^\circ\text{C}$ ) and the InAs grown at lower temperature ( $540^\circ\text{C}$ ). The interruption took place by closing the gallium shutter and maintaining the arsenic flux (pink stage in Figure 6.1 a). We set a growth time of 25 minutes for GaAs, a cooling down process of 5 minutes plus 2 minutes of temperature stabilization. The growth time for the InAs part was 25 minutes, resulting in a total growth time of 57 minutes. We fixed the In and As fluxes to  $0.05 \text{ nm s}^{-1}$  and  $8.4 \times 10^{-7} \text{ Torr}$ , respectively. The In flux corresponds to two-dimensional equivalent growth rate on an InAs(001) surface. The corresponding V/III beam equivalent pressure ratio is 7. The results of InAs-on-GaAs nanowires are shown in Figure 6.1.

We find that approximately 40% of all InAs segments grow kinked with respect to the GaAs nanowire stem. Moreover, the InAs segments have a significantly larger diameter as compared to the GaAs stems (Figure 6.1 b,c). On average, the diameter of the GaAs, InAs segments and Au droplets are  $19 \pm 2 \text{ nm}$ ,  $55 \pm 12 \text{ nm}$  and  $22 \pm 5 \text{ nm}$  respectively. Within the margin of error, the diameter of GaAs nanowires and Au droplets corresponds to the initial size of the deposited Au colloids. The GaAs nanowires diameter is homogeneous along the entire growth axis revealing no or a very limited shell overgrowth (Figure 6.1 c). The diameter of the InAs segments is homogeneous as well. Yet, it exceeds significantly the diameter of the GaAs stems and the one of the Au droplets. A high density of stacking faults can be seen in the InAs segment (Figure 6.2).



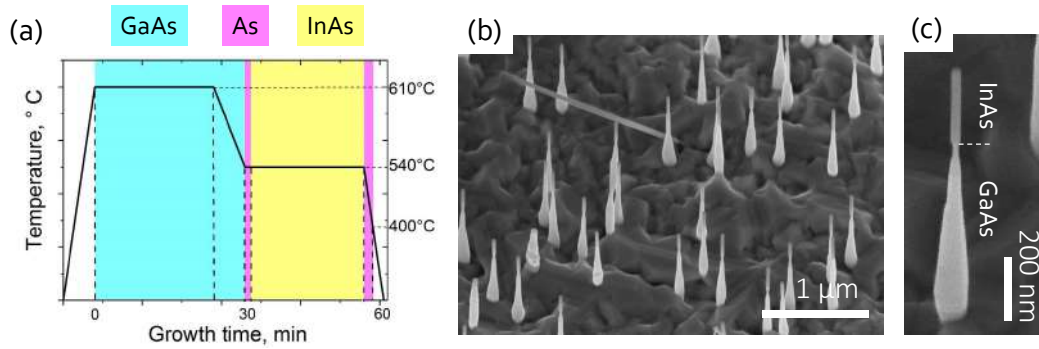
**Figure 6.1:** a) Scheme of the InAs-on-GaAs nanowire growth sequence with an intermediate cooling down step under As flux only. b) SEM image (30° tilt) of InAs-on-GaAs nanowires corresponding to the growth sequence. c) Magnified SEM image (30° tilt) of a single InAs-on-GaAs nanowire from image (b).



**Figure 6.2:** Bright-field TEM image of a kinked InAs-on-GaAs nanowire from the sample shown in Figure 6.1 (b). The nanowire kinks at the InAs/GaAs interface. The InAs segment presents randomly distributed stacking faults along the entire growth axis. The arrows indicate the positions where the diameters of GaAs, InAs and Au were measured.

## 6.1 Optimization of the growth protocol

One possible hypothesis for the InAs segment kinking is as follows. During the cooling step under As (pink stage on Figure 6.1 a), Ga is purged from the droplet and forms a GaAs nanowire section (see the cooling neck appearance for GaAs nanowires cooled under As in Chapter 5.5). Since the Ga source is switched off, the concentration of Ga atoms in the liquid droplet decreases, resulting in the supersaturation decrease in the Au droplet. This favors the formation of a zinc blende GaAs section with truncated facets at the droplet/nanowire interface. The facets, moreover, increase in size with the supersaturation decrease in the droplet. InAs growth starts, when we open the In shutter. A large amount of In dissolves into the depleted droplet both from direct impingement and from adatom surface diffusion to the nanowire tip. Such abrupt volume expansion destabilizes the droplet. It has a high probability to slide on the truncated facets, leading to the growth of a kinked InAs segment. Therefore, a special precaution should be taken during the cooling procedure in order to keep the Au droplets stable.



**Figure 6.3:** a) Scheme of the InAs-on-GaAs nanowire growth sequence with an intermediate cooling step under continuous growth of GaAs. b) SEM image (30° tilt) of InAs-on-GaAs nanowires corresponding to the growth sequence. c) Magnified SEM image (30° tilt) of a single InAs-on-GaAs nanowire from image (b).

We developed an optimized growth protocol, where the Ga flux is switched off after the cooling procedure and only for 2 minutes (see Figure 6.3 a). We grow the GaAs nanowires during 25 minutes at 610 °C and extend the growth for 5 minutes while cooling down to 540 °C compared to the previously discussed case. We use fixed In and As fluxes of  $0.126 \text{ nm s}^{-1}$  and  $6.0 \times 10^{-6}$  Torr, respectively. The corresponding V/III beam equivalent pressure ratio is 20. Essentially, all InAs segments grow straight on top of the GaAs stems (Figure 6.3 b,c). Only 8% of nanowires do not exhibit InAs segment at all or have a kinked geometry. We observe that the diameter of the structure evolves along the growth axis: the GaAs nanowire segments have a bottle-shaped morphology, where the basis of each nanowire has a larger diameter than the tip (Figure 6.3 c). It

is an indication of GaAs and/or InAs radial overgrowth. The diameter of the InAs segments is homogeneous along the entire growth axis.

We now discuss what is the mechanism resulting in the formation of straight InAs segments. During the cooling step under Ga and As, the droplet is constantly fed with Ga. This leads to a stable level of supersaturation in the liquid droplet. The GaAs nanowires keep growing in the wurtzite crystal structure, forming planar droplet/nanowire interface as opposed to the zinc blende crystal structure with truncated facets. We believe that InAs nucleates from a mechanically stable Au droplet on a flat top facet, favoring straight growth.

## Discussion

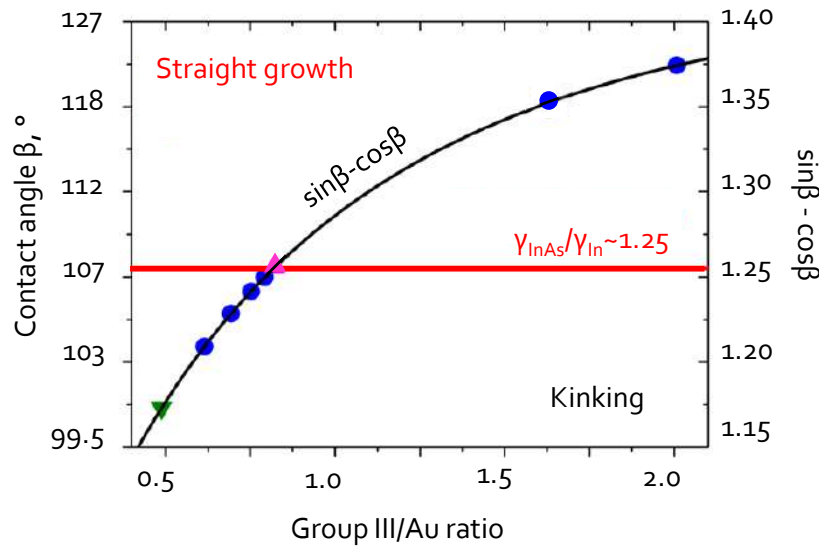
It is difficult to deduce whether the concentration of Ga (group-III) in the liquid droplet or the crystal structure itself (and thus a flat top facets at the liquid/solid interface) is responsible for the droplet stability. A clear dependence of the crystal structure of InAs segments on the growth of straight InAs-on-GaAs nanowires was demonstrated in the work of Messing and coworkers [74]. Only InAs with a wurtzite phase led to straight InAs-on-GaAs heterostructures. In the present thesis, straight InAs segments have a wurtzite crystal structure containing stacking faults. We collected information about the crystal structure of InAs and GaAs segments from the recent literature on the growth of Au-assisted InAs-on-GaAs axial nanowire heterostructures (see Table 6.1). Remarkably, a straight morphology of InAs-on-GaAs nanowires is always accompanied by the presence of the wurtzite crystal structure for InAs segments.

NW heterostructure	InAs morpho-logy	GaAs crys-tal structure	InAs crystal structure
InAs-GaAs-InAs [136]	straight	zinc blende	wurtzite
InAs-on-GaAs [71]	kinked	?	?
InAs-on-GaAs [72, 73]	kinked	zinc blende	zinc blende
InAs-on-GaAs [74]	straight	zinc blende	wurtzite
	kinked	zinc blende	zinc blende
	straight	wurtzite	wurtzite
	kinked	wurtzite	zinc blende
InAs-on-GaAs [75]	straight	wurtzite	wurtzite
InAs-on-GaAs [36]	straight	wurtzite	wurtzite

**Table 6.1:** A summary of works on InAs-on-GaAs nanowires morphology versus the crystal structure of the segments. Question marks correspond to the case where the crystal structure is unknown.

On the other hand, Zannier et al. [75] considered solely the geometry of the droplet. High group III concentrations in the liquid droplet and thus large contact angles (larger than  $107^\circ$ ,





**Figure 6.4:** Graph of  $\sin \beta - \cos \beta$  (or the droplet contact angle  $\beta$ ) as a function of group III-to-Au ratio. Adapted from [75]. The red straight line represents the ratio of InAs over In surface energies and separates areas of straight (above) and kinked (below) growth of InAs-on-GaAs axial nanowires. Straight growth of InAs segments on top of GaAs is possible when the droplet contact angle is above  $107^\circ$ . The experimental points correspond to different nanowire samples, namely InAs-GaAs-InAs (blue circles), GaAs-InAs with In pre-deposition (pink triangle), GaAs-InAs without In pre-deposition (green triangle).

see Figure 6.4) contribute to a higher droplet stability at the nanowire tip and thus facilitate the formation of straight nanowire heterostructures. The authors pre-deposited In before the growth of their GaAs nanowires, which led to an increase of the Ga solubility in the Au droplet from 33% to 45% and to an increase of the vertical yield of InAs-on-GaAs nanowires. To explain the results, the authors used the Nebol'shin-Shchetinin model, which considers the nanoparticles stability at the nanowire tip. Straight growth occurs if  $\frac{\gamma_{sv}}{\gamma_{lv}} < \sin \beta - \cos \beta$ , where  $\gamma_{sv}$  is the solid-vapor surface energy of the nanowire sidewalls ( $\gamma_{\text{InAs}}$  for the experiment),  $\gamma_{lv}$  is the liquid-vapor surface energy of the catalyst droplet at the nanowire tip ( $\gamma_{\text{In}}$  considering a gold droplet with a high concentration of In) and  $\beta$  is the contact angle of the droplet. The model is plotted in Figure 6.4. The experimental results of the authors (points in the Figure) come in great agreement with the model.

Here, we aim at linking both interpretations, i.e the droplet geometry and the crystal structure. Interestingly, we notice, that the experimental points attributed to the straight growth correspond to contact angles limited to  $127^\circ$  (Figure 6.4.). Such angles are known to promote the formation of the wurtzite crystal phase in Au-assisted nanowires (see, for example, [40]). Yet, experimental data for nanowires having an Au droplet with an angle greater than  $127^\circ$  are missing. Such angles correspond to the presence/formation of the zinc blende crystal structure. We propose to grow



nanowires with large droplet contact angles (more than  $130^\circ$ ). Such contact angles correspond to the zinc blende crystal phase and a high group III-to-V ratio at the same time. This experiment would clarify whether the crystal phase and/or the droplet angle are responsible for the formation of straight InAs-on-GaAs nanowires.

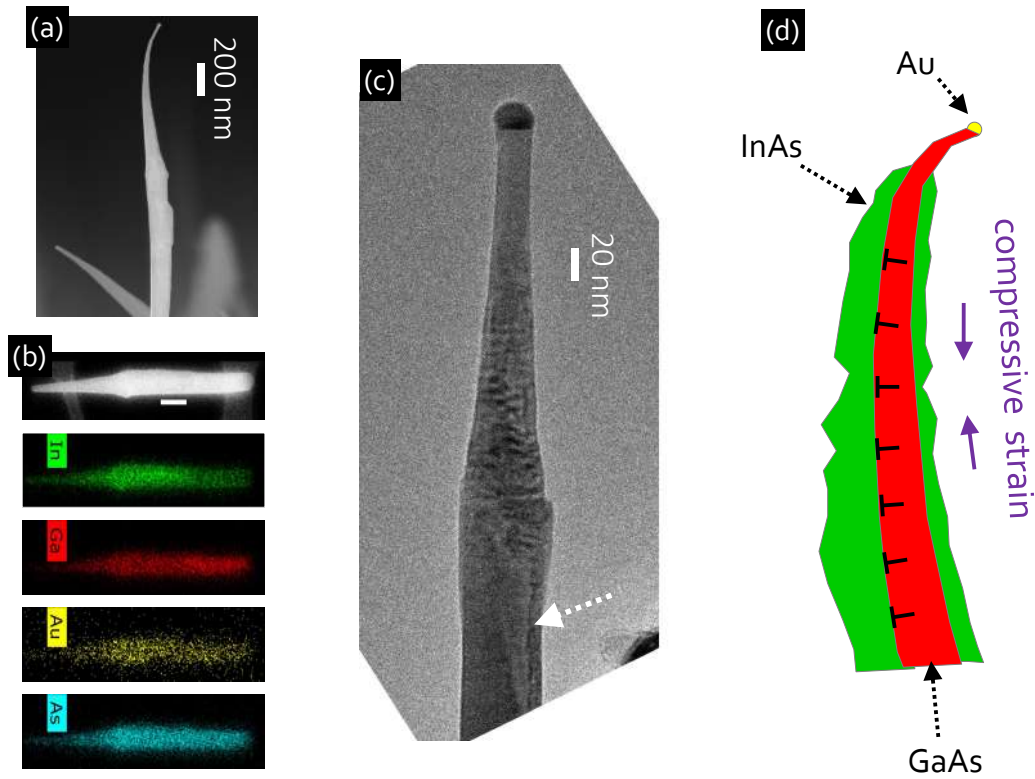
## 6.2 Influence of the growth temperature on the yield of vertical InAs segments

We now study the influence of the growth temperature on the yield of vertical InAs segments. Two set of samples were prepared using the same growth protocol as depicted in Figure 6.3. For the first set of samples (four samples) we use the following material fluxes:  $0.126 \text{ nm s}^{-1}$  for In and  $6.0 \times 10^{-6}$  Torr for As. The corresponding V/III beam equivalent pressure ratio is 30. We varied the growth temperature between  $420^\circ\text{C}$  and  $540^\circ\text{C}$  by steps of  $40^\circ\text{C}$ . For the second set of samples (four samples) we decreased the In flux to obtain an equivalent growth rate of  $0.05 \text{ nm s}^{-1}$ , while keeping the As flux constant ( $6.0 \times 10^{-6}$  Torr). The resulting V/III beam equivalent pressure ratio is 50. For the second set of samples the growth temperatures are  $510^\circ\text{C}$ ,  $540^\circ\text{C}$ ,  $570^\circ\text{C}$  and  $610^\circ\text{C}$ .

### Low growth temperatures

The SEM observations of samples grown at  $420^\circ\text{C}$  and  $460^\circ\text{C}$  reveal no axial InAs growth on top of GaAs stems. Nanowires grown at  $420^\circ\text{C}$  are significantly tapered (Figure 6.5) with diameters of  $130 \pm 24 \text{ nm}$  and  $21 \pm 9 \text{ nm}$  at the basis and at the top, respectively. The droplet at the nanowires top is usually smaller than 20 nanometers, reaching a minimum of 12 nanometers. Moreover, we find that some of the nanowires do not preserve their Au droplets at the tips. Such nanowires are slightly shorter than the other nanowires.

Strong tapering can be explained by the reduction of Ga diffusion during the cooling growth step from  $610^\circ\text{C}$  to  $420^\circ\text{C}$ . The Ga adatoms contribute to radial growth instead of diffusing to the nanowire tip. Therefore, the Ga concentration in the liquid droplet decreases continuously with the temperature leading to the decrease in the droplet volume: nanowires grow tapered (Figure 6.3 a). Similar tapering phenomenon has been explained in the work of Harmand et al. for Au-assisted GaAs nanowires [127]. The authors state that the diminution of the nanowire diameter is a direct consequence of the Ga depletion from the catalyst droplet at the nanowire tip. Once the substrate temperature reaches  $420^\circ\text{C}$  we open the In flux. The incoming In atoms diffuse along the GaAs side walls. Yet, due to a large and most likely a rough GaAs shell formed around the GaAs stems during the cooling growth step, the In adatoms have a high chance to be trapped on the nanowire sidewalls, forming an InAs shell. The final nanowires thus have a core/shell geometry. Post growth

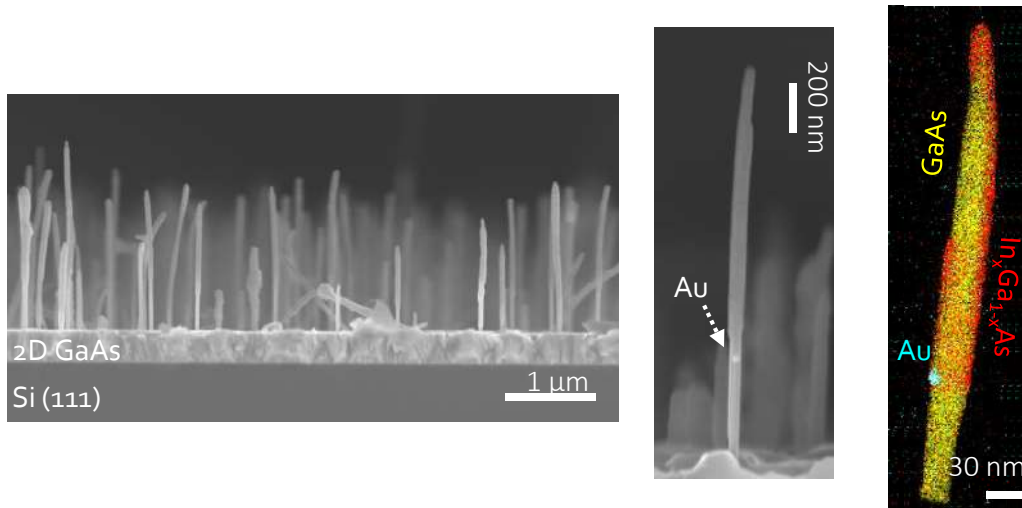


**Figure 6.5:** InAs-on-GaAs nanowire heterostructures grown at 420 °C. a) SEM image (side view) of a typical nanowire. b) SEM image of an individual nanowire and its EDX elemental maps. It is clearly visible that an InGaAs shell surrounds the GaAs segment. c) Bright-field TEM image of an individual nanowire. The arrow indicates a misfit dislocation formed in the shell due to strain. d) Schematic of the nanowire from (a) with the curvature. The growth of an heterogeneous shell results in residual compressive strain on the thinner shell side. The strain at the thicker shell side is released by network of misfit dislocations (black intersections).

energy-dispersive x-ray spectroscopy (EDX) analysis confirms this growth behavior (Figure 6.5 b). We observe that the InAs shell (In in green) covers the GaAs core (Ga in red). We find moreover that some catalyst droplets are not preserved at the nanowires tips at low growth temperatures. A similar phenomenon was reported for Au-assisted GaAs nanowires grown in the temperature range between 340 °C and 420 °C by Tchernycheva and coworkers [114]. They establish experimentally that the Au-Ga droplet can be both in a liquid and a solid state in this temperature window, leading to an unstable droplet. Such a droplet can easily fall from the top of the nanowire.

We notice that some GaAs/InAs core/shell nanowires curve along their length (Figure 6.5 a). As the lattice mismatch between GaAs and InAs materials is 7%, we suspect that the InAs shell heavily strains the GaAs core. According to Raychaudhuri et al. [64], the critical diameter of the GaAs core lays below 10 nanometers to grow a dislocations-free interfaces in core/shell

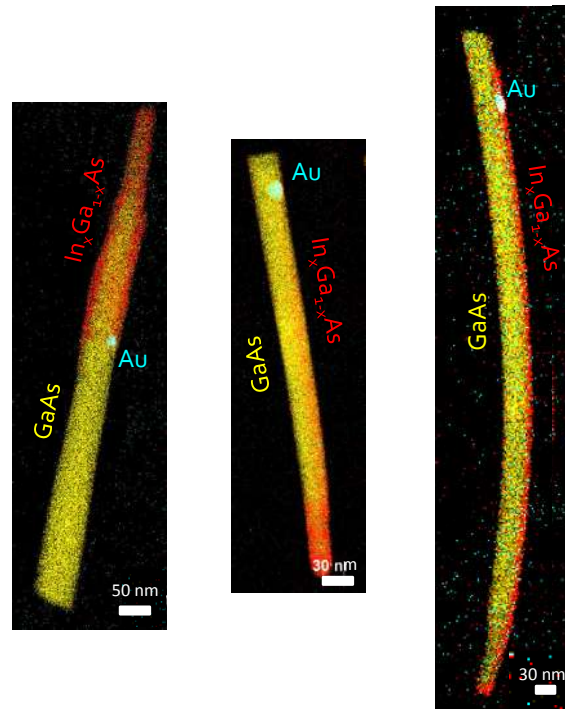
GaAs/InAs nanowires. Our GaAs nanowires exceed 20 nanometers, therefore, it is energetically favorable to form misfit dislocations. TEM analysis reveal the presence of heavy strain at the nanowire sidewalls (Figure 6.5 c), similar to the work reported for InAs/GaAs core/shell nanowires, in which the presence of misfit dislocations was confirmed using HRTEM [140]. In this work, the authors observed the curvature of nanowires which is the result of a non symmetric shell growth around the core. The side where thick shell is formed (thickness about 30 nanometers) is fully plastically relaxed via the formation of misfit dislocations. On the contrary, on the thinner shell side (about 10 nanometers thickness) the relaxation happens both plastically and elastically, leading to the bending of the nanowire. In conclusion, one potential explanation for the bending of our GaAs/InAs nanowires is the formation of an inhomogeneous InAs shell around the GaAs core at low growth temperatures (Figure 6.5 d). We explain the inhomogeneous shell formation by the shadowing of the In flux.



**Figure 6.6:** InAs-on-GaAs nanowire heterostructures grown at 460 °C. a) SEM image (side view) of the nanowires. b) Close-up SEM image (side view) of an individual nanowire. The position of the gold droplet is indicated by an arrow. c) An overlay image of Ga, In, As and Au EDX elemental maps revealing the position of the gold droplet and the InGaAs shell.

Nanowires grown at 460 °C (Figure 6.6 a) exhibit a slight inverse tapering. We find no catalyst droplets at the tips. Figure 6.6 b shows the Au droplet on the sidewall of the nanowires. Post growth EDX analysis confirms that the Au droplets do not preserve at the nanowire tips. Moreover, InGaAs regions around the GaAs stems are visible on the overlay of EDX elemental maps. Interestingly, these InGaAs regions always "start" from the tip and "end" at the gold droplet (Figure 6.7). We suppose that the Au droplet catalyzes the growth of these regions: InGaAs segment wraps around the tip of the GaAs stem and continues to grow in the opposite direction.

A similar geometry was found in other works related to the growth of energetically unfavorable Au-assisted axial nanowire heterostructures (see, for example, [71, 72]) and is usually referred to as "kinked morphology". Zannier et al. observed similar growth behavior for InAs-on-GaAs nanowire heterostructures for low group III concentration in the Au droplet [75]. We cannot evaluate the actual gold droplet composition during growth to confirm their hypothesis. First of all, the droplet diameter is small (only 20 nm) and the droplet is located on the nanowire sidewall leading to a weak EDX signal coming from the droplet combined with the background signal. Finally, after the growth is terminated and the sample is cooled down under As flux, a certain amount of group III material is purged out of the droplet, modifying the initial composition of the droplet.

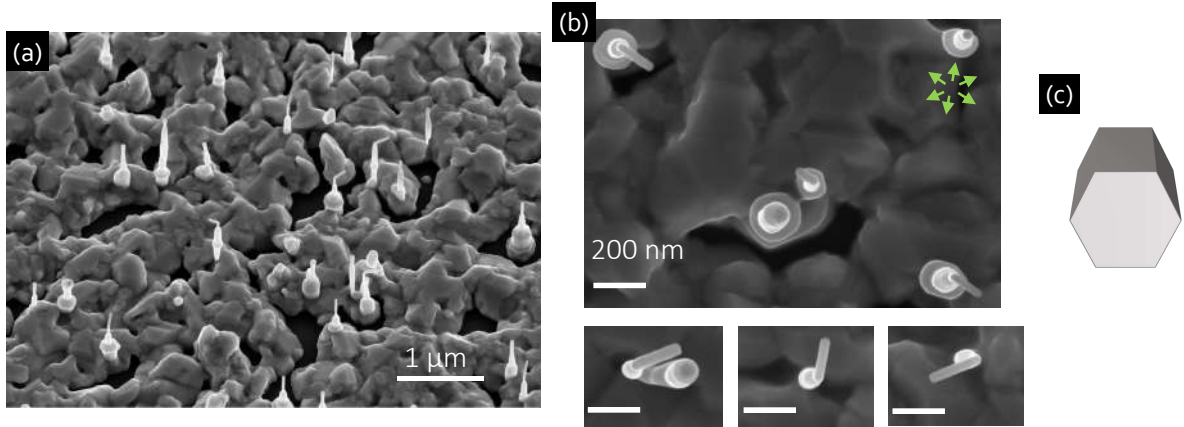


**Figure 6.7:** Additional EDX data for InAs-on-GaAs nanowire heterostructures grown at 460 °C. An overlay image of Ga, In, As and Au EDX elemental maps revealing the position of the gold droplet and the InGaAs regions.

### High growth temperatures

Above 570 °C, we observe InAs segments grown on top of the GaAs nanowires, in contrast to the samples grown at low temperatures. However, the segments kink at given angles to the nanowire growth direction. Figure 6.8 shows a sample grown at a constant growth temperature of 610 °C. We observe that GaAs stems feature a significant diameter variation along the growth axis. It is

an indication of InAs radial overgrowth. Indeed, GaAs nanowires grown at 610 °C are thin and homogeneous in diameter (see Chapter 5), which means that the diameter evolution happens only once the In source is supplied. Top-view SEM images (Figure 6.8 b) reveal a systematic kinking along one of the six available in hexagonal wurtzite GaAs stems directions. A similar kinking distribution was recently reported for wurtzite InP nanoflags [141].



**Figure 6.8:** InAs-on-GaAs nanowires grown at 610 °C. a) SEM image (30° tilt) of the nanowires. b) SEM images (top view, scale bar 200 nm) of the kinked nanowires. The nanowires kink along one of the six GaAs nanowire directions (directions indicated by arrows in the upper right corner). c) Schematic representation of six wurtzite side facets and corners along the [0002] growth direction.

We notice that kinked InAs-on-GaAs nanowires grown at high temperatures ( $\geq 570$  °C) have a similar morphology to those grown with non-optimized growth protocol, where nanowires kink due to a drop in supersaturation (Figure 6.1). According to experimental findings reported by Hertenberger and coworkers [142] for self-assisted InAs nanowires grown in MBE, the desorption rate of In stays approximately constant between 480 °C and 540 °C temperatures and increases by a factor of two at temperatures above 540 °C. The growth parameters used for InAs nanowires (namely, In and As fluxes) overlap with the ones used in the current manuscript. Due to a high desorption rate, less In enters the liquid droplet, resulting in the supersaturation decrease. As discussed earlier, such decrease favors long truncated edges at the solid/liquid interface. The droplets become unstable and the nanowires have a higher probability to kink.

### Optimum growth temperature: 540 °C

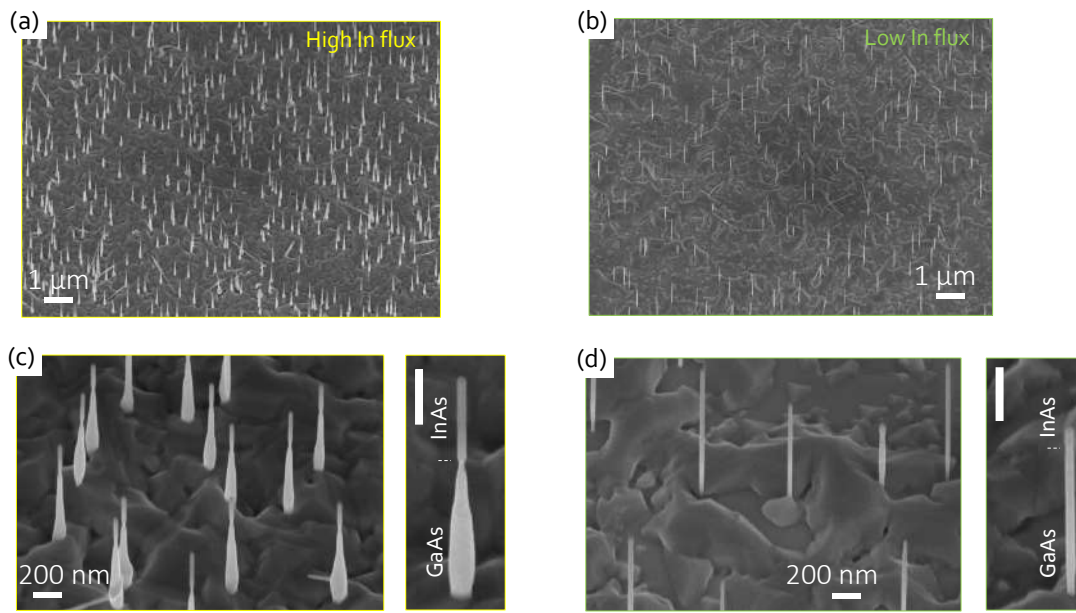
When InAs grows at 540 °C, we find that essentially all InAs segments grow straight on top of GaAs stems regardless of the In flux (Figure 6.9). At this optimum temperature, In adatoms surface diffusion to the liquid droplet is enhanced compared to the low growth temperatures. Moreover, the desorption of In is still negligible at 540 °C [142]. Therefore, the supersaturation



### 6.3 Influence of the In flux on the nanowires morphology and InAs-GaAs interface composition

of Au remains high during the whole growth sequence, resulting in the formation of a planar droplet/nanowire interface and, consequently a stable position of the droplet at the nanowire tip.

While straight growth of InAs-on-GaAs nanowires was achieved for both low and high In fluxes, we note significant difference in nanowire morphology (see Figure 6.9 c,d). At high In flux, GaAs stems exhibit significant diameter variation along the growth axis. On the contrary, at low In flux, nanowires are thin and exhibit a homogeneous diameter. We perform a detailed investigation of the samples morphology in the following section.

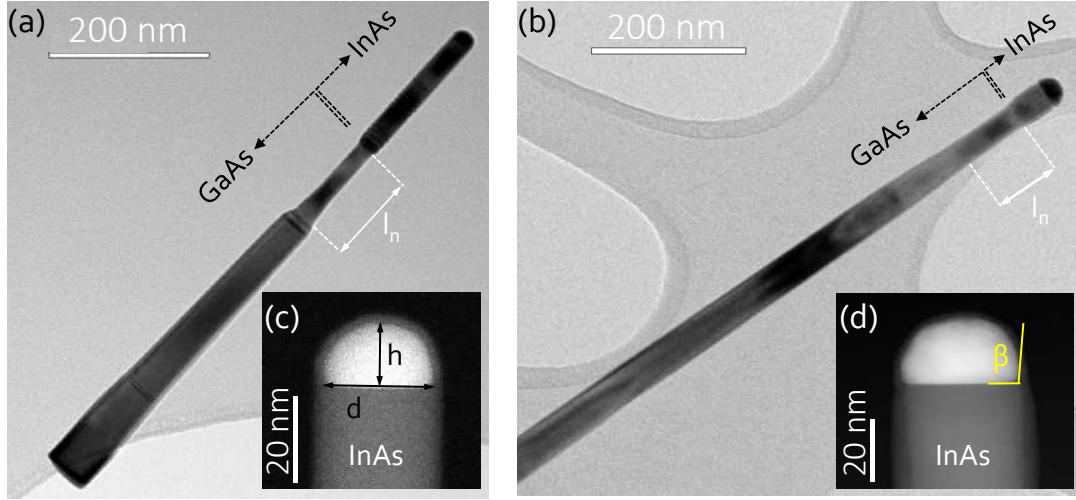


**Figure 6.9:** InAs-on-GaAs nanowires grown at low and high In fluxes at 540 °C. SEM images (30° tilt) of the nanowires grown at (a) high ( $0.126 \text{ nm s}^{-1}$ ) and (b) low ( $0.05 \text{ nm s}^{-1}$ ) In fluxes. c) Close-up view of the nanowires from (a); d) close-up view of the nanowires from (b). Note that parasitic 2D growth on the substrate is 380 nanometers for high In flux and 330 nanometers for low In flux: it is the reason why the GaAs segment looks longer in (d) than in (c).

## 6.3 Influence of the In flux on the nanowires morphology and InAs-GaAs interface composition

### Nanowire morphology

We now examine by TEM the morphology of the nanowires grown at 540 °C for two different In fluxes (6.10). Table 6.2 summarizes the morphological parameters of the nanowires grown at low and high In fluxes: the diameter  $d_{\text{InAs}}$  and the length  $l_{\text{InAs}}$  of the InAs segment, the diameter at the interface  $d_i$  (the thinnest part of the nanowire), the shell thickness around the GaAs segment



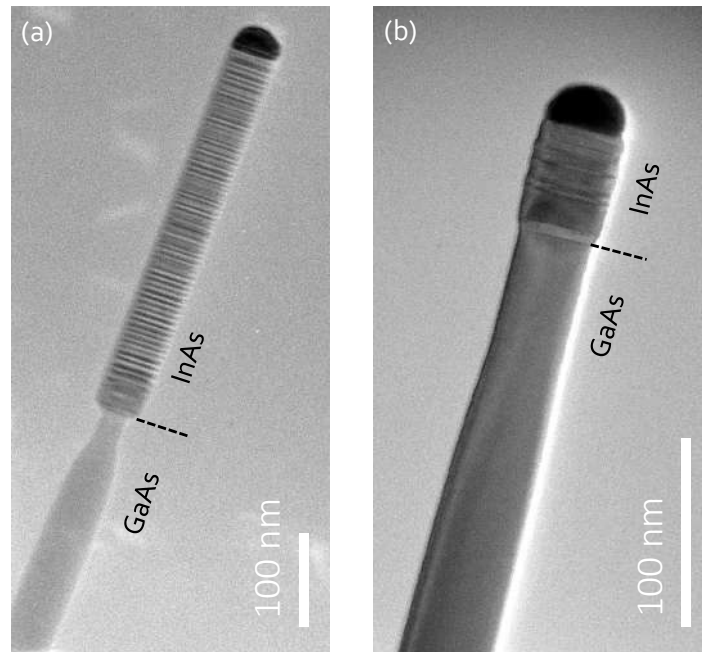
**Figure 6.10:** Morphology of InAs-on-GaAs nanowires grown at 540 °C for two different In fluxes observed by TEM. Bright-field TEM image of a typical InAs-on-GaAs nanowire grown at a high In flux ( $0.126 \text{ nm s}^{-1}$ ) (a) and at a low In flux ( $0.05 \text{ nm s}^{-1}$ ) (b). The interface is indicated by a dashed black arrow. The length of the GaAs neck is denoted by a white arrow. The insets (c) and (d) are the dark field TEM close-up views of the nanowire tips. The droplet height  $h$ , the nanowire diameter  $d$  and the droplet contact angle  $\beta$  are indicated on the images.

$d_{sh}$  (the thickest part minus the GaAs core), the length of the GaAs neck  $l_n$ , the axial  $V_{ax}$  and the radial  $V_r$  InAs growth rates. Moreover, we also measured the aspect ratio of the gold droplets  $h/d$  (height divided by the InAs nanowire diameter) and the droplet contact angle  $\beta$ .

In flux, nm/s	$d_{InAs}$ , nm	$d_i$ , nm	$d_{sh}$ , nm	$l_{InAs}$ , nm	$l_n$ , nm	$V_{ax}$ , nm/s	$V_r$ , nm/s	$h/d$	$\beta$ , °
0.126	$28 \pm 5$	$22 \pm 2$	$12 \pm 6$	$423 \pm 85$	$113 \pm 5$	$0.47 \pm 0.09$	$0.013 \pm 0.007$	$0.6 \pm 0.004$	$95 \pm 4$
0.05	$37 \pm 9$	$30 \pm 8$	$4 \pm 2$	$70 \pm 51$	$94 \pm 16$	$0.05 \pm 0.03$	$0.003 \pm 0.0013$	$0.57 \pm 0.05$	$105 \pm 16$

**Table 6.2:** Morphological parameters of the InAs-on-GaAs nanowires grown at 540 °C. The  $d_{sh}$  was deterimed using EDX, the  $h/d$  was determined by TEM.

As already observed by SEM in Figure 6.9 c), a high In flux of  $0.126 \text{ nm s}^{-1}$  leads to a bottle-shape nanowire morphology. The InAs segments grow on top of GaAs with an axial growth rate of  $0.47 \pm 0.09 \text{ nm s}^{-1}$ . The axial growth rate is 4 times larger than the equivalent two-dimensional growth rate. This is a signature of a diffusion-induced growth mechanism. An InAs shell surrounds the bottom of the GaAs segment. This shell has a lateral growth rate of  $0.013 \pm 0.007 \text{ nm s}^{-1}$  (10% of the two-dimensional growth rate). All nanowires feature a thin neck before the interface. We measure a length of the neck segment of  $113 \pm 5$  nanometers.



**Figure 6.11:** Crystal structure of InAs-on-GaAs nanowires grown at 540 °C for two different In fluxes. (a) Bright-field TEM image of a typical InAs-on-GaAs nanowire grown at high In flux of  $0.126 \text{ nm s}^{-1}$ . (b) Bright-field TEM image of a typical InAs-on-GaAs nanowire grown at low In flux of  $0.05 \text{ nm s}^{-1}$ .

This neck is formed during the cooling step when Ga and As fluxes are still supplied during 5 minutes. According to Chapter 5, we estimate that the growth rate of GaAs nanowires at 540 °C is approximately  $0.4 \text{ nm s}^{-1}$ . Then the 113 nanometers segment will be grown in 4.7 minutes which corresponds to the cooling time.

By decreasing the In flux down to  $0.05 \text{ nm s}^{-1}$  under a constant As flux (thus increasing the V/III flux ratio from 20 to 50), we observe that the nanowire diameter along the entire growth axis is more uniform. However, we notice an increase in the fluctuation of the InAs segment length compared to segments grown with a high In flux. The axial growth rate is  $0.05 \pm 0.03 \text{ nm s}^{-1}$  (the same as two-dimensional growth rate). We find a thin shell, surrounding the bottom of the wire, which is formed at a radial growth rate of  $0.003 \pm 0.0013 \text{ nm s}^{-1}$  (17% of the two-dimensional growth rate). All nanowires feature a GaAs cooling neck (Figure 6.10 b).

Finally, we observed by TEM that the InAs segments grown at high In flux exhibit a high density of stacking faults and the crystal phase switches along the entire growth axis (Figure 6.11 a). At low In flux, the density of stacking faults decreases noticeably (Figure 6.11 b). A lower In flux and consequently higher V/III flux ratio improved the crystalline quality of InAs segments, as observed for GaAs nanowires in Chapter (5), where pure wurtzite GaAs nanowires were achieved with high V/III flux ratio.



The local V/III flux ratio affects the liquid droplet geometry and the contact angle during nanowire growth [40] and is responsible for the crystal structure selection. The lower the local V/III flux ratio, the larger the liquid droplet. Therefore, there is a higher probability that the liquid/solid interface has a truncated facet, provoking the zinc blende crystal switch. This leads to the formation of stacking faults in the wurtzite crystal sequence that arises naturally in III-As nanowires grown by Au-assisted vapor-liquid-solid mechanism. For example, Plante and La Pierre observed that the density of stacking faults in wurtzite Au-assisted GaAs nanowires is decreased when the Ga flux is decreased from 0.28 to 0.07 nm s<sup>-1</sup> at a constant As flux[130]. Moreover, radial growth is suppressed at the lowest Ga flux. Our results are thus in agreement with the experimental findings reported in [130].

## InAs-GaAs interface composition

Here we study the chemical composition of the nanowires grown at low and high In fluxes. We performed EDX measurements along and across the nanowire axis. We use In L-lines, Ga K-lines, As K-lines and Au L-lines for the quantification analysis.

Figure 6.12 shows the EDX results for a typical InAs-on-GaAs nanowire grown at a low In flux. On the axial EDX line profile we clearly see three zones (Figure 6.12 b): the long bottom segment is pure GaAs, the upper segment with a larger diameter is InAs and the droplet is Au. Surprisingly, we find that the composition of the nominal InAs segment is an In<sub>x</sub>Ga<sub>1-x</sub>As ternary alloy with  $x$  varying from 0.9 at the GaAs interface to 0.8 near the top. A pure 5 nanometers InAs segment is visible below the Au catalyst. The post-growth droplet contains 70% of Au and 30% of In. No detectable Ga is found in the droplet. We measure a GaAs/In<sub>0.85</sub>Ga<sub>0.15</sub>As interface length of 20 nanometers. The interface sharpness ranges between 15 and 30 nanometers for this sample, depending on the studied nanowire. The EDX line profiles taken perpendicular to the growth axis of the same InAs-on-GaAs nanowire are presented in Figures 6.12 c and d. We find that the In<sub>0.85</sub>Ga<sub>0.15</sub>As segment is surrounded by a thin Ga-rich In<sub>x</sub>Ga<sub>1-x</sub>O shell (Figure 6.12 c). The GaAs stem features a few nanometers thick In<sub>0.05</sub>Ga<sub>0.95</sub>As shell, which is covered by gallium oxide (Figure 6.12 d).

We then performed EDX on nanowires grown at a higher In flux (Figure 6.13). From the axial EDX line profile 6.13 b, we determine an interface of 10 nanometers for the presented nanowire, which is significantly sharper than the interface of nanowires grown at low In flux. Yet, the nanowire seems bended and the interface length may thus be potentially overestimated. EDX measurements performed on additional nanowires from the same sample revealed that the interface sharpness reaches 5-8 nanometers. We find similar compositions of the nanowire as for the low In flux: the upper nominal InAs segment contains Ga and hence is an In<sub>x</sub>Ga<sub>1-x</sub>As ternary alloy. The concentration of In reaches 95% right after the GaAs interface, and decreases down to 80% at the nanowire top. Similarly to the sample grown at low In flux, we observe a

pure InAs segment before the Au droplet on several nanowires (yet the segment is not present for the nanowire in Figure 6.13). A Ga-rich  $\text{In}_x\text{Ga}_{1-x}\text{O}$  shell is visible on the EDX line profile taken across the InGaAs segment (6.13 c). The thin  $\text{In}_{0.05}\text{Ga}_{0.95}\text{As}$  shell, surrounding the GaAs stems (Figure 6.13 d) is covered with indium oxide but not with Ga oxide as it was for the low In flux sample. It is a signature of an In-rich layer below the oxide. Interestingly, we do not find a pure InAs shell around the GaAs segments neither for low nor for high In fluxes.

In conclusion, the interface length is significantly reduced at higher In flux. It even approaches the values of the interface length obtained for self-catalyzed InAs-on-GaAs nanowires [82]. We suppose that the introduction of In in the gold droplet leads to the rapid decrease of the Ga solubility in the droplet. An increase in the In incorporation rate in the droplet leads to faster depletion of Ga, and thus to a sharper interface. However, a question remains: why the expected InAs segment is in fact an InGaAs ternary alloy?

## 6.4 Study on anomalous formation of a ternary $\text{In}_x\text{Ga}_{1-x}\text{As}$ segment

Here, we discuss why the expected pure InAs segment is an InGaAs ternary alloy. We propose possible strategies to realize a pure InAs segment.

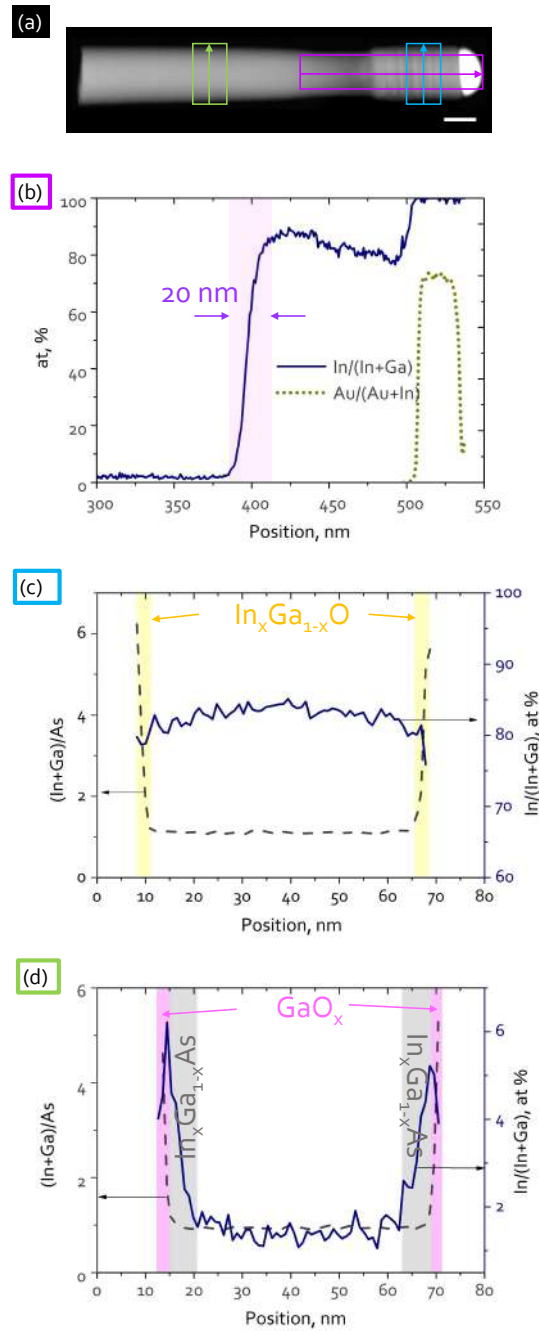
As we see in Figures 6.12 c and 6.13, the InGaAs segment has a constant composition in the radial direction, confirming that Ga adatoms are incorporated into the volume via the catalyst droplet. Moreover, we observe that the amount of Ga increases along the growth axis: the longer the InGaAs segment the higher the Ga concentration at the top. This means that there is a source of Ga in the system regardless of the growth time (within the 25 minutes during which the In shutter is open). We speculate that the possible sources of Ga in our experiment are: **i)** the presence of residual Ga adatoms on the substrate surface and the nanowire sidewalls; **ii)** Ga accumulated in the catalyst droplet during the growth of GaAs segments; **iii)** thermally created Ga atoms from the GaAs nanowire sidewalls; **iv)** thermally created Ga atoms from the two-dimensional GaAs on the Si substrate. We examine below these four possibilities.

*i) residual Ga adatoms on the substrate surface and the nanowire sidewalls:*

As the lifetime of Ga adatoms before incorporation or adsorption is in the order of several tens of milliseconds [143], this possible Ga source dries up immediately after switching off the Ga flux.

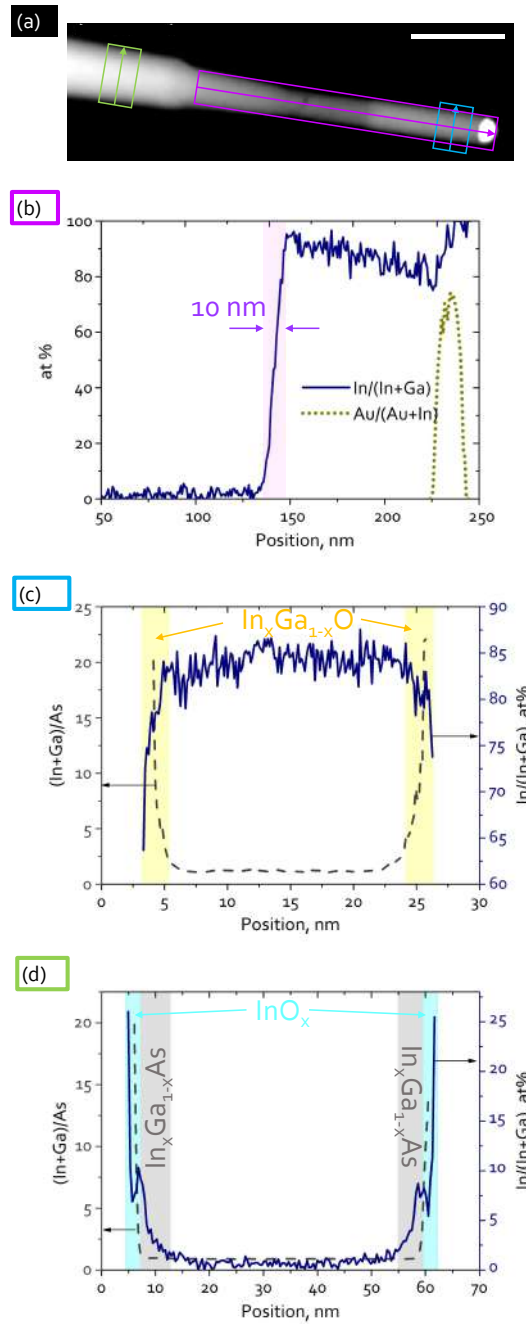
*ii) Ga accumulated in the catalyst droplet:*

The amount of Ga in the droplet is proportional to the droplet volume  $\propto R^3$  (where  $R$  is the droplet radius) and hence is limited in time. By considering that the Ga atoms incorporate into the nanowire via the droplet/nanowire interface ( $\propto R^2$ ), we find a transitional InGaAs region of 10-20



**Figure 6.12:** Determination of the chemical composition of an InAs-on-GaAs nanowire grown at a low In flux ( $0.05 \text{ nm s}^{-1}$ ) on Si. (a) HAADF-STEM image (scale bar 30 nm) of the nanowire. EDX line profile of In and Au composition along the growth axis (b). EDX line profiles of In and As across the InAs nanowire segment (c) and across the GaAs stem (d).

#### 6.4 Study on anomalous formation of a ternary $\text{In}_x\text{Ga}_{1-x}\text{As}$ segment



**Figure 6.13:** Determination of the chemical composition of an InAs-on-GaAs nanowire grown at a high In flux ( $0.126 \text{ nm s}^{-1}$ ) on Si. (a) HAADF-STEM image (scale bar 60 nm) of the nanowire. EDX line profile of In and Au composition along the growth axis (b). EDX line profiles of In and As across the InAs nanowire segment (c) and across the GaAs stem (d).

nanometers, affected by the residual Ga atoms stored in the liquid droplet, which corresponds to the interface length (Figure 6.12 b and 6.13 b).

This means that the Ga present in the InAs segment after the interface originates probably from thermally created Ga atoms, which are formed either on the GaAs nanowire sidewalls (iii) and/or on the substrate surface (iv) and diffuse toward the nanowire tip. Under our experimental conditions ( $T=540^\circ\text{C}$  and  $6.0 \times 10^{-6}$  Torr arsenic flux) the diffusion length of Ga and In adatoms is on the order of several micrometers [132] and exceeds the length of the nanowires ( $\sim 1.5\ \mu\text{m}$ ).

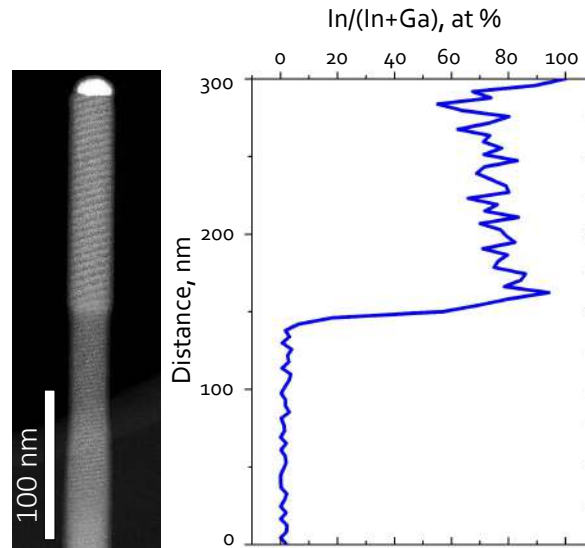
*iii) Ga source from the nanowire sidewalls:*

Generally, low-dimensional systems have lower cohesive energy per atom pair compared to bulk materials due to an increased surface-to-volume ratio. In other words, it is more energetically favorable to create an isolated atom out of a nanowire surface than out of the two-dimensional layer by breaking all the bonds [144]. After having analyzed HRSTEM images of our nanowires, we notice that both the GaAs and InAs-on-GaAs nanowire sidewalls feature similar geometry and are always from the same  $\{-2110\}$  family. We do not find any visible damage at the InAs-on-GaAs nanowire sidewalls. Yet, a damaged GaAs nanowire surface can efficiently trap In adatoms during InAs segment growth in order to minimize its surface energy. In this case the nanowire sidewalls will remain visibly smooth with the formation of an InGaAs shell (and not a pure InAs shell). This would explain, why the shell formed around the GaAs segments is an  $\text{In}_{0.05}\text{Ga}_{0.95}\text{As}$  ternary alloy (Figure 6.13 d).

*iv) Ga source from the two-dimensional GaAs layer:*

We now suppose, that the population of Ga atoms is formed on the substrate surface out of the two-dimensional GaAs layer. In order to verify this idea, we grew an additional InAs-on-GaAs nanowire sample on GaAs (111)B instead of Si (111). We kept the same growth parameters as for the sample with low In flux. As shown in Figure 6.14 , EDX analysis revealed that the amount of Ga incorporated into the InAs segment is higher when growing on GaAs rather than on Si. We find a ternary  $\text{In}_x\text{Ga}_{1-x}\text{As}$  alloy with  $x$  varying from 0.8 at the GaAs interface to 0.6 near the top. The Ga concentration in the InAs segment is almost twice as high as in the InGaAs segment grown on the Si substrate (Figure 6.13). A pure 5 nanometers InAs region before the gold droplet is visible once again.

Gonzalez and coworkers reported on the incorporation of Ga atoms from GaAs substrates into nominally pure Au-assisted InAs nanowires grown by MBE [145, 146]. The authors state that Ga is supplied from the first monolayers of the GaAs substrate. The Ga adatoms migrate toward the liquid droplet and incorporate into the nanowire via the liquid/solid interface. Depending on the growth parameters, the Ga content in their nominally pure InAs nanowires reaches values between 3% and 19%. Yet, the Ga composition along the nanowire axis remains constant. We notice, however, that the concentration of Ga in our nominally pure InAs segments is not constant



**Figure 6.14:** Investigation of the chemical composition of a typical InAs-on-GaAs nanowire grown with a low In flux of  $0.05 \text{ nm s}^{-1}$  on GaAs (111)B substrate. (a) HAADF-STEM image of the nanowire. (b) EDX line profile of In composition along the growth axis of the nanowire from image (a).

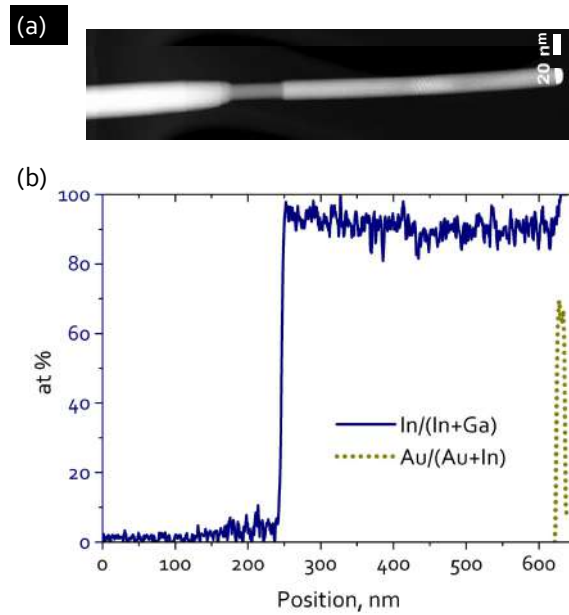
and increases toward the nanowire tip. This is a signature of a more complex process happening during the growth of our nanowires.

To explain the Ga increase, we propose that both the **iii)** and the **iv)** source supply Ga. As already discussed, the **iii)** source damages the nanowire sidewalls, creating traps for In adatoms. The longer the growth time, the rougher the nanowire sidewalls and the more In adatoms are trapped at their surfaces. This leads to a reduced In incorporation and hence increased Ga proportion along the InAs nanowire segment.

*Strategies to realize a pure InAs segment:*

Given the importance of growing In(Ga)As quantum dots with a precise composition, we now investigate how to control/decrease the Ga concentration in the nominally pure InAs segments. We know from Chapter 5, that the Ga diffusion length decreases at low growth temperatures and high As fluxes. We first investigate how the increase in As flux will influence the Ga concentration. For this, we kept all growth parameters identical to the sample with high In flux (In flux of  $0.126 \text{ nm s}^{-1}$ ) but increased the As flux from  $6.0 \times 10^{-6} \text{ Torr}$  to  $1.0 \times 10^{-5} \text{ Torr}$ . The EDX line scan, taken along the nanowire axis (Figure 6.15), reveals that the InAs segment is still an  $\text{In}_x\text{Ga}_{1-x}\text{As}$  ternary alloy. Nevertheless, the Ga content is notably decreased compared to the lower As flux (Figure 6.13 b) and does not exceed 10%.

To completely eliminate Ga in the InGaAs segment, Ga diffusion from the substrate and the nanowire surfaces should be restrained. One way to do so is to decrease the growth temperature.



**Figure 6.15:** Investigation of the chemical composition of a typical InAs-on-GaAs nanowire grown with a high In flux of  $0.126 \text{ nm s}^{-1}$  and a high As flux of  $1.0 \times 10^{-5}$  Torr on Si (111) substrate. (a) HAADF-STEM image of the nanowire. (b) EDX line profile of In and Au composition along the growth axis of the nanowire from image (a).

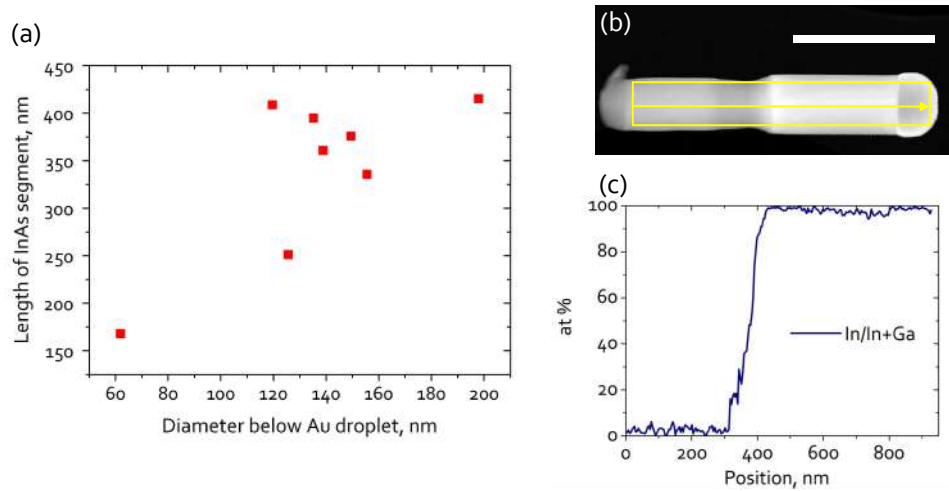
Indeed, we observe systematically a pure InAs segment right below the catalyst droplet with a length of few nanometers (Figure 6.12 d). This segment is formed at the end of the growth procedure, when the temperature decreases from  $540^\circ\text{C}$  to  $400^\circ\text{C}$  under As flux (see Figure 6.12). At low growth temperatures (below  $530^\circ\text{C}$ ) the diffusivity of Ga adatoms is very low, and there is no Ga migration toward the Au droplet [41]. Therefore, only In remains in the liquid droplet, which is purged out of it, forming a pure InAs segment. However, even though the pure InAs segment is found at low growth temperatures, we cannot grow InAs-on-GaAs nanowires at temperatures below  $540^\circ\text{C}$  as the yield of straight InAs segments decreases dramatically in this temperature range (see Figure 6.18). We thus search another solution to achieve a pure InAs segment.

Another way to avoid Ga in InGaAs is to completely suppress adatoms diffusion. It is possible by growing InAs using the *adsorption-induced* growth mechanism, where only direct impingement of the supplied material contributes to the nanowire formation (2). The *adsorption-induced* growth mechanism takes place when the nanowire diameter exceeds a critical value. The critical diameter for the *adsorption-induced* growth mechanism generally increases for the same material system, when the supersaturation of the gaseous phase is increased [41]. For example, Plante and LaPierre observed that for Au-assisted GaAs nanowires grown by MBE, the critical diameter above which the *adsorption-induced* mechanism begins to dominate over the *diffusion-induced* mechanism, is



in the range of 100-180 nanometers.

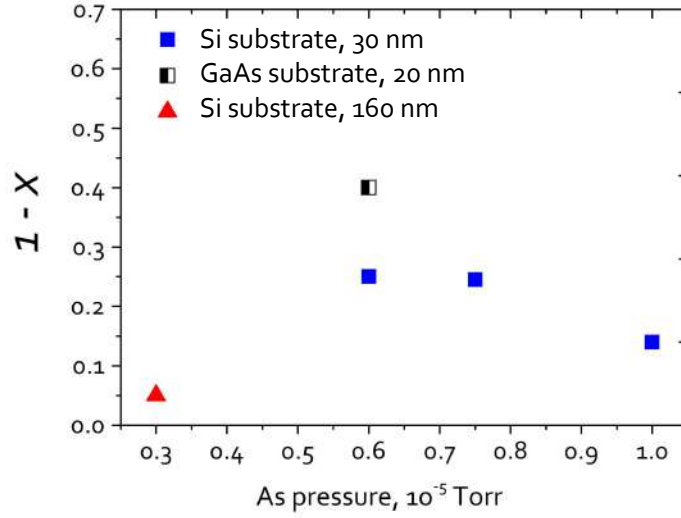
We studied an InAs-on-GaAs nanowire sample grown with intentionally increased diameters to verify if the nanowire length increases with the nanowire diameter ( $L(d)$  dependence, which is characteristic to nanowires grown via the *adsorption-induced* growth mechanism, see Chapter 2). We used 50 nanometers Au colloids. As the gold colloids can coalesce some nanowires can have a diameter larger than the gold droplet catalyst. The growth parameters were set as  $0.05 \text{ nm s}^{-1}$  and  $3.0 \times 10^{-6}$  Torr for In and As fluxes, respectively. After growth, we dispersed nanowires on a carbon grid and used SEM to measure the InAs segment length  $L$  and the nanowire diameter  $d$  at the droplet/nanowire interface. The results are presented in Figure 6.16 a. We observe that the InAs nanowire length increases with diameter, in the range between 60 and 200 nanometers diameter, consistent with the theory for *adsorption-induced* growth mechanism. Yet, several data points do not follow the  $L(d)$  dependence and are most probably related to a measurements error. Indeed, the length is measured on SEM images of nanowires, which are randomly dispersed on a grid. The nanowires axis is not necessarily oriented in a direction perpendicular to the electron beam, and the error on the InAs length measurements can increase significantly depending on the angle between the nanowire axis and the electron beam.



**Figure 6.16:** InAs-on-GaAs nanowires grown with 50 nanometers gold colloids at low In flux of  $0.05 \text{ nm s}^{-1}$ . (a) InAs segment length as a function of the nanowire droplet diameter. Each data point represents a measurement taken from a single nanowire. (b) HAADF-STEM image (scale bar 500 nm) of a typical InAs-on-GaAs nanowire. (c) EDX line profile of In composition along the growth axis of the nanowire from image (b).

We then performed an EDX analysis of the nanowires along the growth axis. The composition profile (Figure 6.16 c) revealed that the InGaAs segment contains less than 5 % of Ga, which is 4 times less than for 20 nm diameter nanowire grown on a Si substrate with higher V/III ratio





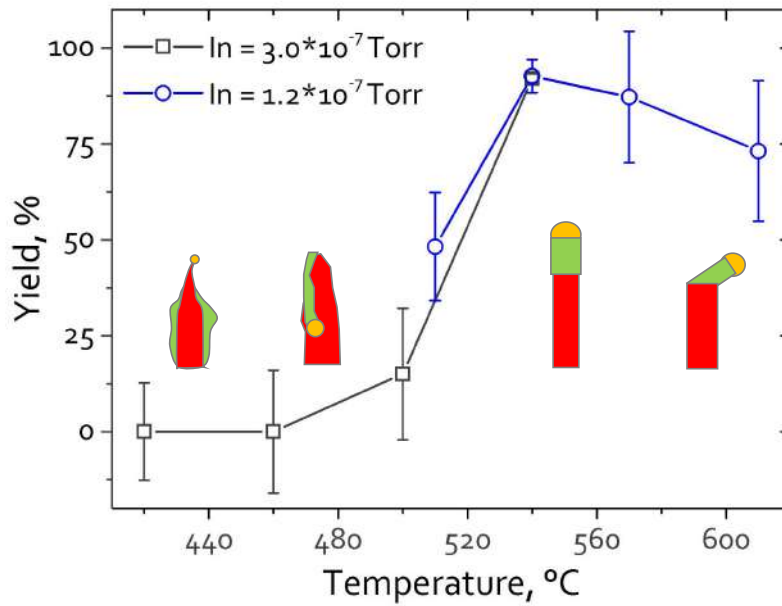
**Figure 6.17:** Summary on the Ga molar fraction in nominally pure InAs segments vs the As flux for different diameters (diameter at the Au/InAs interface is indicated) and substrates.

(Figure 6.12). Finally, the use of large diameter nanowires brought to light that the only use of the *adsorption-induced* growth mechanism can prevent Ga diffusion from the substrate.

By a set of experiments, we established that Ga found in the nominally pure InAs segment, is most likely formed due to the diffusion of Ga adatoms thermally created on the substrate and on the nanowire sidewalls. We defined several strategies to improve the purity of the InAs segment: a) high As flux; b) Si substrate; c) large diameters. By increasing the As flux, the Ga concentration in the InGaAs segment decreases from 25 % to 15 % (blue square points, Figure 6.17). The use of a Si (111) substrate instead of a GaAs (111)B, reduces the amount of Ga in the InGaAs by a factor of 2 (black square, Figure 6.17). The Ga concentration in the InGaAs segment becomes negligible (less than 5 %) for nanowires with large diameters (red triangle, Figure 6.17) owing to the transition from the *diffusion-induced* to the *adsorption-induced* growth mechanism. Unfortunately, an increase in the nanowire diameter can cause deterioration of the crystal quality of the GaAs/InAs interfaces as we will see in the following Chapter 7.

## 6.5 Conclusions

In conclusion, we demonstrated the successful growth of Au-assisted straight InAs-on-GaAs nanowire heterostructures on Si by MBE with a yield up of 92%. We found out that the key ingredient to obtain straight InAs on GaAs segments is to keep the Au droplet stable. To this end, we proposed a two-step growth procedure enabling to maintain a high supersaturation in the Au catalyst during the group III element interchange.



**Figure 6.18:** Yield of straight InAs-on-GaAs nanowires plotted as a function of InAs growth temperature with In fluxes of  $3.0 \times 10^{-7}$  Torr ( $0.126 \text{ nm s}^{-1}$ ) and  $1.2 \times 10^{-7}$  Torr ( $0.05 \text{ nm s}^{-1}$ ).

We investigated the influence of the InAs growth temperature on the yield of vertical InAs segments (Figure 6.18). We find that at 540 °C, the yield of straight nanowire heterostructures reaches its maximum regardless of the In flux. Low growth temperatures below 500 °C led to the formation of a thick and irregular shell around the GaAs nanowires with no axial InAs growth. On the contrary, axial InAs segments form at growth temperatures above 570 °C. However, the segments kink.

We evaluated the influence of the In flux on the interface sharpness. We observed that the samples grown with higher In flux feature sharp interfaces with a length down to 5 nanometers. Yet, high In flux led to an increase in the density of stacking faults in the InAs segment. Through accurate study of the chemical composition across the GaAs segments, we found that  $\text{In}_{0.05}\text{Ga}_{0.95}\text{As}$  shell is formed around GaAs segments for both In fluxes.

Our study surprisingly revealed, that nominally pure InAs segments contain a high concentration of Ga. Moreover, the Ga concentration is not constant along the growth axis and increases toward the nanowire tip. Through detailed analysis of potential Ga sources, we concluded that Ga is most likely supplied from the diffusion of thermally created Ga atoms, formed on the GaAs nanowire sidewalls and on the two-dimensional GaAs layer grown on Si substrates. We found that increasing the As beam flux contributes to reduce the Ga concentration in the  $\text{In}_x\text{Ga}_{1-x}\text{As}$

segments. We proposed a strategy to completely eliminate the influence of Ga diffusion from the substrate surface and the nanowire sidewalls based on the only use of *adsorption-induced* growth mechanism. Experimentally, we observe that InAs-on-GaAs nanowires with large diameters between 60 and 200 nanometers are almost free of Ga in the InGaAs segment (less than 5%) even at low As flux, owing to the suppression of the *diffusion-induced* growth mechanism.

## Chapter 7

# Strain distribution in axial InAs-on-GaAs nanowire heterostructures

As we already discussed in Chapter 2, strained and defect-free heterointerfaces are much easier to obtain in nanowires than in planar thin films owing to the nanowires geometry. For a given lattice mismatch there is a critical diameter below which infinitely long nanowires with dislocations free interfaces can be grown. Yet, strain affects the band structure of the nanowire heterostructure and thus its electronic and optical properties. In this regard, it is important to understand how the strain distributes in the vicinity of the interface in axial nanowire heterostructures.

The characterization techniques, which allow to evaluate strain in nanowires can be divided into two groups. The first group measures the average strain in nanowires as, for example, photoluminescence (PL) [147] or x-ray diffraction [148, 149]. The second group allows to directly access the strain distribution in an individual nanowire with atomic resolution. It is based on high resolution transmission electron microscopy (HRTEM) imaging and is widely used to study strain effects in nanowire heterostructures. One way to quantitatively extract the strain field from HRTEM images is to use a Geometrical Phase Analysis (GPA) [93], a technique based on a Fourier space algorithm (see Chapter 3).

Taraci and his colleagues were the first ones to map strain in an individual Ge nanowire grown on a Si (111) substrate using HRTEM and GPA [150]. They observed that strain fields were present not only in the vicinity of the substrate/nanowire heterointerface but also along the nanowire sidewalls. The latter strain was unintentionally induced during TEM sample preparation. A year later, Larsson et al. reported strained and dislocations free atomically sharp interfaces in axial InAs/InP nanowire heterostructures [59]. The authors performed strain measurements of the nanowire heterointerfaces using HRTEM. The results were compared with finite element simulations of the same heterostructure and showed good agreement with it. Importantly, GPA strain mapping allows to visualize missing atomic planes such as misfit dislocations at the nanowire

heterointerfaces. Frigeri et al. [68] studied the strain distribution along axial GaAs/InAs nanowire heterostructures with diameters exceeding the critical diameter for misfit dislocations formation. It was found that at the nanowire heterointerfaces the GaAs segment features additional planes of atoms in comparison with the upper InAs segment. The average distance between the extra-half planes increases from the center of the interface to the nanowire sidewalls. This is an indication that the strain is not only relaxed plastically via the formation of dislocations but is also relaxed elastically via lateral expansion of the nanowire. As for today, a large number of works has been published on the determination of strain by HRTEM and GPA in axial [66, 67, 151] and radial nanowire heterostructures [152] and nanowire superlattices [153, 154]. Yet, nanowire heterostructures considered in those works feature sharp compositional interfaces in the range of 1.5-5 nanometers, which is very different from our InAs-on-GaAs nanowires with graded interfaces in the range of 5-90 nanometers.

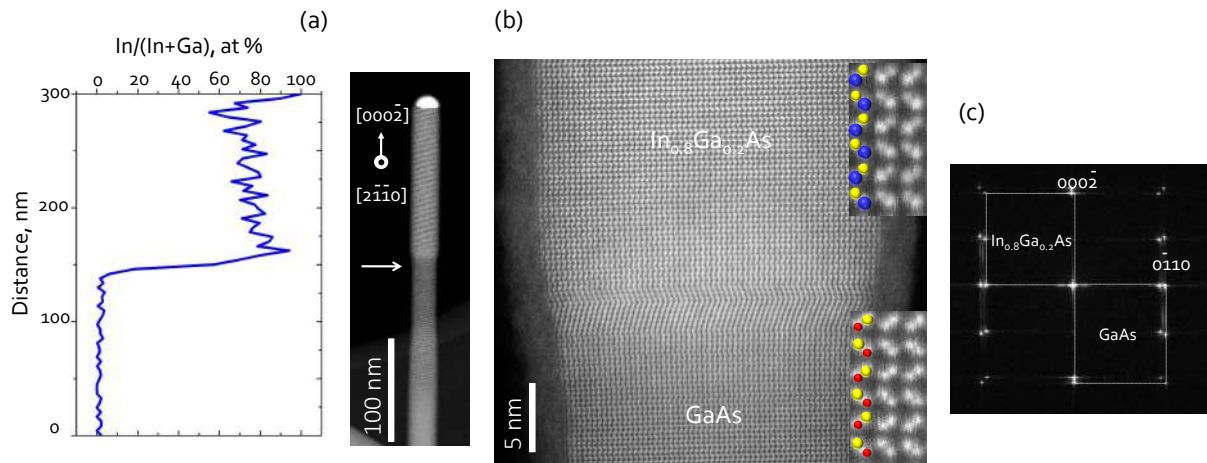
In this chapter, we investigate the strain distribution in our  $\text{In}_x\text{Ga}_{1-x}\text{As-on-GaAs}$  ( $x$  varying between 0.6 and 1.0) nanowire heterostructures. We study nanowires with different interface sharpnesses and with diameters below and above the theoretical critical diameter for the formation of misfit dislocations [14]. We combine HRSTEM with GPA and the resulting data are compared with theoretical simulations performed using the finite element method. The simulations have been performed by Petr Stepanov at NEEL institute.

## 7.1 Nanowires with diameters below the critical diameter

### Crystalline quality

#### *Crystal structure:*

Dislocations free GaAs/InAs nanowire heterointerfaces, with a lattice mismatch of 7%, are expected for nanowire diameters below 40 nanometers [14] (see Chapter 2). We first investigated the interfaces of nanowires grown with 20 nanometers gold colloids (Table 7.1). Nine nanowires were analyzed from three different samples (namely: NW256, NW483 and NW348). Figure 7.1 a) shows a high angle annular dark field scanning TEM (HAADF STEM) image and an EDX line scan along the nanowire obtained from nanowire X3 (sample NW348). The nanowire features two segments: the lower is composed of GaAs and the upper one is the nominally pure InAs segment (Figure 7.1 a). Yet we saw in Chapter 6 that the upper segment is in fact composed of an  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  ternary alloy (Figure 7.1 a). Moreover, note that the bottom segment of the nanowire features a thin InGaAs shell, whose origin has been discussed in the previous Chapter 6. The high resolution HAADF STEM image of the nanowire interface (Figure 7.1 b) reveals that both segments have a wurtzite crystal structure as further confirmed by FFT (Figure 7.1 c). In Figure 7.1 b we can also see a small zinc blende region right at the interface (due to its small fraction it is



**Figure 7.1:** Crystal structure of an InAs-on-GaAs nanowire from sample NW348 (NW X3). (a) Dark-field TEM image of the InAs-on-GaAs nanowire taken along the  $[2\bar{1}\bar{1}0]$  viewing direction and EDX composition profile measured along the nanowire growth axis. The position of the interface is indicated with the arrow. (b) High resolution HAADF-STEM image of the nanowire interface shown in (a). Two insets present magnified HAADF-STEM images of the GaAs (bottom) and In<sub>0.8</sub>Ga<sub>0.2</sub>As (top) crystal structure. Ga, In and As columns positions are marked by red, blue and yellow, respectively. Most of the wire has a wurtzite crystal structure as confirmed by Fast Fourier Transform (c).

not observed in the Fourier transform). In order to determine the polarity of the nanowire, we used magnified HAADF STEM images (insets in Figure 7.1 b) to access the atomic contrast between group III (Ga or In) and V (As) columns arranged in dumbbell pairs. The heavier the element the brighter the contrast in the HAADF STEM image. We determined that in both segments the As column is always facing the tip of the nanowire in a dumbbell pair whereas In and Ga always face the bottom. This indicates that the nanowire growth direction is As polar or  $[000\bar{2}]$  [155].

We calculated the in-plane ( $a = 4.212 \text{ \AA}$ ) and out-of-plane ( $c = 7.0 \text{ \AA}$ ) lattice constants of In<sub>0.8</sub>Ga<sub>0.2</sub>As. They are larger than those of GaAs ( $a = 3.9845 \text{ \AA}$ ,  $c = 6.52 \text{ \AA}$ ). Therefore, two sets of patterns are present on the FFT image (Figure 7.1 c): the inner pattern belongs to In<sub>0.8</sub>Ga<sub>0.2</sub>As and the external one to GaAs.

#### Interface quality

The visual inspection of the high-resolution HAADF STEM image (Figure 7.1 b) did not reveal any misfit dislocations at the interface between the GaAs and In<sub>0.8</sub>Ga<sub>0.2</sub>As segments. The nanowire has a diameter of 22 nanometers at the interface which is far below the critical diameter for plastic relaxation of GaAs/InAs interfaces. Identical TEM analysis was performed on all the nanowires presented in Table 7.1 with interface diameters  $d_i$  between 21 and 45.8 nanometers. We did not observe any misfit dislocations in good agreement with the theoretical work by F. Glas [14]. Interestingly, the crystal phase switches from wurtzite to zinc blende in the transition region between GaAs and In<sub>0.8</sub>Ga<sub>0.2</sub>As for all the investigated nanowire heterostructures. The

Sample	Substrate	$d_{Au}$ , nm	In rate, $\text{nm s}^{-1}$	V/III ratio	NW	$d_i$ , nm	interface sharpness, nm	MF dislocations
NW256	Si	20	0.05	50	1	31.5	25	no
					2	23	24	no
					3	23.4	19	no
					4	45.8	26	no
					7	21		no
NW483	Si	20	0.126	30	11	24.7	5	no
					12	25	10.5	no
NW348	GaAs (111)B	20	0.05	50	X2	26	10	no
					X3	22	14	no
NW498	Si	50	0.05	25	1	96.2	80	yes
					3	110	-	yes
					6	168.5	90	yes

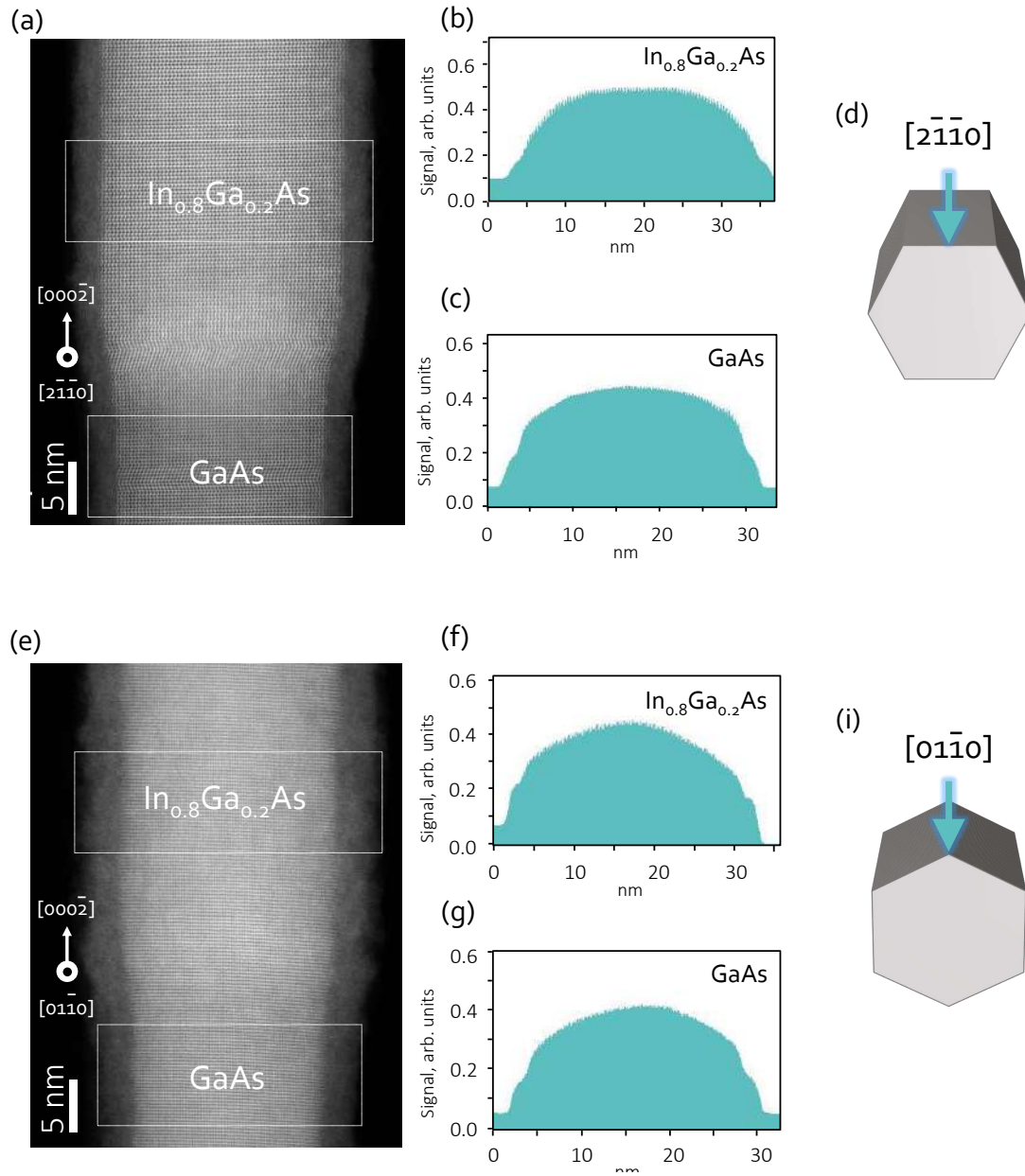
**Table 7.1:** Database of the nanowire samples studied in this chapter. MF is an abbreviation of misfit.

length of the zinc blende segment reaches values between 1.6 and 9.8 nanometers. The segment appears once In is introduced in the system. A possible explanation of its origin is given below. We observe that the nanowire becomes thicker after the interface. We attribute it to an increase in the size of the catalyst droplet due to uptake of In [156, 67]. The change in volume and contact angles, as we saw in Chapter 2, can be responsible for the crystal structure change.

#### Nanowire facets:

Generally, a nanowire cross section is hexagonal and the six facets are oriented normal to the growth direction. Yet their crystallographic orientation is has to be determined. We now study the crystal orientation of the nanowire sidewalls using HAADF STEM images along  $[2\bar{1}\bar{1}0]$  (Figure 7.2 a) and  $[01\bar{1}0]$  (Figure 7.2 e) viewing directions. To this end, we perform intensity line scans across the  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  and GaAs segments. The intensity is directly related to the nanowire thickness and thus allows to scan the profile of the nanowire sidewalls along the beam direction. Figure 7.2 a) is an HAADF STEM image taken along the  $\langle 2\bar{1}\bar{1}0 \rangle$  zone axis. The intensity profiles taken across the  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  (Figure 7.2 b) and GaAs (Figure 7.2 c) have a similar shape and feature a flat central region. This is a signature that the nanowire heterostructure is terminated by  $\{\bar{2}110\}$  facets (Figure 7.2 d). When the nanowire is rotated by  $30^\circ$  and viewed along the  $\langle 01\bar{1}0 \rangle$  zone axis (Figure 7.2 e), the profiles from both segments (Figure 7.2 f,g) exhibit maximum intensity in the central region, which corresponds to the facets edge (Figure 7.2 h). This observation confirms that the orientation of the nanowire side facets is  $\{\bar{2}110\}$ .





**Figure 7.2:** Nanowire facets orientation (nanowire X3 from sample NW348). HAADF STEM images of the  $\text{InAs}$ -on- $\text{GaAs}$  nanowire taken along the  $[2\bar{1}\bar{1}]_0$  (a) and  $[01\bar{1}]_0$  (e) viewing directions. Signal intensity across  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  (b) and GaAs (c) obtained from (a). Signal intensity across  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  (f) and GaAs (g) obtained from (e). The line profiles are averaged over a width of 9 nanometers. d),h) Scheme of the nanowire orientation with respect to the electron beam.



The most common orientation of the nanowire side facets in wurtzite nanowires is  $\{10\bar{1}0\}$  [59, 157, 158]. On the other hand, Plante and LaPierre [159, 130] observed that the facet orientation of Au-assisted GaAs nanowires grown by MBE changes from  $\{10\bar{1}0\}$  to  $\{\bar{2}110\}$  when the nanowires undergo significant radial growth. The authors showed that the nanowire tip is free of radial shell and features  $\{10\bar{1}0\}$  side facets, while the nanowire bottom is covered by a thick radial shell and features  $\{\bar{2}110\}$  facets. They authors were able to control the orientation of nanowire facets by varying the Ga flux, with V/III flux ratio ranging between 1.1 and 4.6. Similar results were later published by Czaban et al. for core-shell GaAs/AlGaAs nanowires grown by MBE [160]. Interestingly, Li et al. [131] reported contradictory results for Au-assisted GaAs nanowires grown by MBE. Their nanowires grown at high As fluxes ( $>5.0 \times 10^{-6}$  Torr) feature  $\{\bar{2}110\}$  facets regardless of the Ga flux and radial growth. The authors used much higher V/III flux ratios (30-300) than Plante and LaPierre. Their observations suggest that the orientation of the nanowire side facets depends mainly on the As flux. In the current manuscript, all GaAs nanowires and InAs-on-GaAs nanowire heterostructures exhibit  $\{\bar{2}110\}$  side facets. Since our growth conditions (As flux and V/III flux ratio) are similar to the ones used in [131], we conclude that high As fluxes may promote the  $\{\bar{2}110\}$  nanowire side facets.

From the results of HAADF-STEM image analysis, which revealed a complete absence of misfit dislocations, we conclude that a large strain exists at the interface between GaAs and  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  segments. In the following, we perform strain mapping using GPA to investigate the strain distribution in the nanowire heterostructure.

## Strain mapping

We mapped the strain distribution at the nanowire heterointerface between the GaAs and  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  segments of nanowire X3 (sample NW348), using GPA applied to the HAADF-STEM images (Figure 7.3). In GPA, strain is calculated using a reference region without crystalline defects and with undistorted lattice parameters. We chose here a GaAs region away from the interface. In the GaAs section, the GPA strain, noted E, corresponds to the conventional mechanical strain  $\varepsilon$ . However, E is different from  $\varepsilon$  in the InGaAs segment. Far from the interface, E still have a non-zero value, due to the difference of lattice parameters between GaAs and  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  (6%).

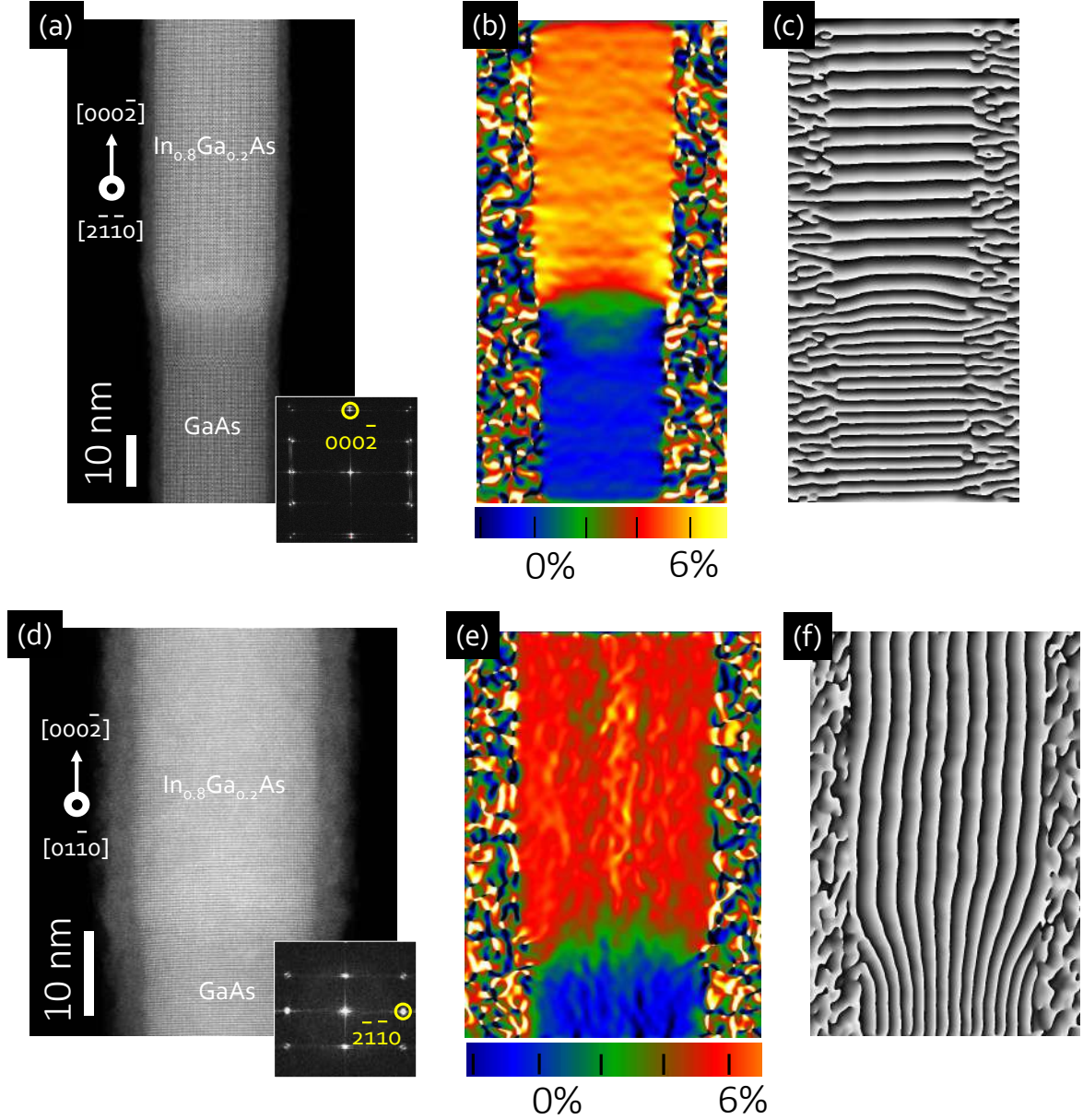
Figure 7.3 a) shows the HAADF-STEM image of the nanowire heterointerface taken along the  $[2\bar{1}\bar{1}0]$  viewing direction. We use the (0002) Bragg peak as indicated in the FFT image (inset Figure 7.3 a) to plot the two-dimensional field of the out-of-plane component of strain  $E_{\perp}$  (Figure 7.3 b). The blue color at the bottom of the image corresponds to unstrained GaAs ( $E_{\perp}=0$ ). The orange color at the top corresponds to unstrained  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$ , yet shifted by 6% compared to the GaAs reference. The region on both sides of the interface has different colors due to the presence of strain. The interface border is sharp and curved. The size of the strained region is

not homogeneous across the interface and is significantly larger at the center of the nanowire. We observe a tendency toward compressive strain on the GaAs side of the interface and toward tensile strain on the  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  side of the interface only along the nanowire sidewalls. As discussed later, quantitative analysis requires a knowledge of the interface composition profile. Importantly, the strain distribution in the interface region does not present any sign of discontinuity: this indicates the absence of misfit dislocations. In order to visualize the elastic deformation of crystalline planes caused by the lattice mismatch, we plot the numerical Moiré pattern (Figure 7.3 c). The Moiré pattern is obtained from the phase image of Figure 7.3 a) using Fourier filtering of  $(000\bar{2})$  Bragg peak, which corresponds to the group of c-planes. The Moiré image acts as a lens magnifying the lattice spacing and allows to see deformations in the crystal. We observe that the crystalline planes bend in the vicinity of the interface close to the side walls. Yet, no extra planes are inserted indicating fully elastic relaxation of the mismatch strain.

The nanowire features both wurtzite and zinc blende segments. In order to access in-plane component of strain  $E_{\parallel}$ , we rotated the nanowire by  $30^\circ$  around its growth axis and took the HAADF-STEM image along the  $[0\ 1\ \bar{1}\ 0]$  viewing direction (Figure 7.3 d). The  $(2\bar{1}\bar{1}0)$  Bragg peak from FFT (inset in Figure 7.3 d) was filtered to plot the  $E_{\parallel}$  strain field (Figure 7.3 e). On the image 7.3 e) blue and the red correspond to unstrained GaAs and  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$ , respectively. We see green flames at the interface. The Moiré pattern, obtained from the phase image of Figure 7.3 d) by Fourier filtering of the  $(2\bar{1}\bar{1}0)$  Bragg peak corresponds to the group of a-planes (Figure 7.3 f). We find that a-planes deform significantly in the vicinity of the interface close to the side walls and that no misfit dislocations are present at the interface similar to the c-planes.

Now we discuss why strain builds at the interface between GaAs and  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  and how it accommodates there. The in-plane lattice constant  $a$  of  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  is  $\sim 6\%$  larger than that of GaAs, however layers form an interface without misfit dislocations. This leads to a large in-plane strain in the vicinity of the interface: the GaAs layer is stretched and the  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  layer is compressed across the nanowire. The in-plane lattice distance (Figure 7.3 f) slowly but continuously increases when moving from GaAs to  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$ . The continuous change in the lattice spacing is possible owing to free nanowire sidewalls where planes bend in order to accommodate the lattice mismatch. Far from the interface, lattice planes become parallel to each other and recover the spacing that is characteristic of unstrained GaAs (below the interface) and of unstrained  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  (above the interface).

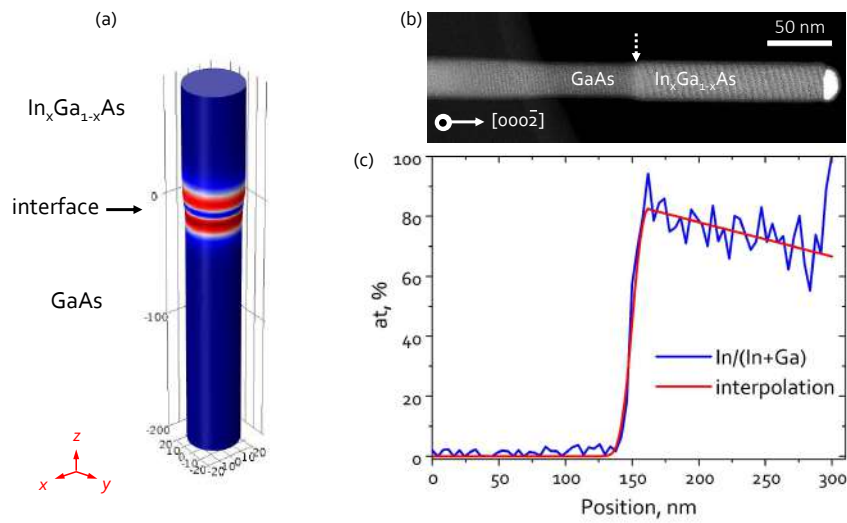
Close to the interface, the out-of-plane lattice constant  $c$  is modified due to the Poisson effect, which tends to limit the variation of the unit cell volume. We find that the c-planes bend at the GaAs/ $\text{InGaAs}$  interface (Figure 7.3 c). Importantly, the spacing between c-planes across the nanowire becomes inhomogeneous and decreases close to the nanowire sidewalls on the GaAs side and increases toward the nanowire sidewalls on the  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  side. This causes compressive and tensile regions along the nanowire sidewalls observed in Figure 7.3 b).



**Figure 7.3:** Strain and deformation in nanowire X3 (sample NW348). a) HAADF STEM image of the InAs-on-GaAs nanowire taken along the  $[2\bar{1}\bar{1}0]$  viewing direction. The inset shows the corresponding Fast Fourier Transform (FFT). The  $(000\bar{2})$  Bragg peak is used to extract  $E_{\perp}$  (b). c) Numerical Moiré pattern obtained from the phase image of (a) after Fourier filtering of the  $(000\bar{2})$  Bragg peak. d) HAADF STEM image of the InAs-on-GaAs nanowire taken along the  $[01\bar{1}0]$  viewing direction and its FFT on the inset. The  $(2\bar{1}\bar{1}0)$  Bragg peak is used to extract  $E_{\parallel}$  (e). f) Numerical Moiré pattern obtained from the phase image of (d) after Fourier filtering of the  $(2\bar{1}\bar{1}0)$  Bragg peak.

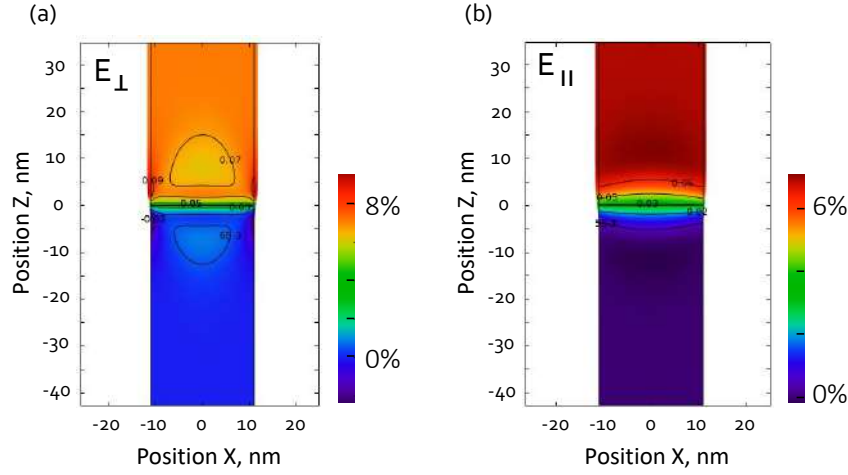
## Comparison with numerical simulations

In order to better understand our experimental findings, we perform numerical simulations of the strain distribution in a nanowire heterostructure using the finite element method. We consider a cylindrical  $\text{In}_x\text{Ga}_{1-x}\text{As}$ -on-GaAs nanowire heterostructure with a wurtzite crystal structure (Figure 7.4 a). The nanowire axis is  $z=[000\bar{2}]$ . The nanowire diameter is set to 20 nanometers and corresponds to that of the nanowire interface in Figure 7.4 b. The length of the GaAs section is 200 nanometers, the length of the InAs section is 60 nanometers. We impose that the nanowire sidewalls and its upper surface are free from any forces and let the nanowire to deform elastically. We assume that the nanowire interface is free from dislocations owing to its small cross section [14]. To determine the lattice mismatch between the segments, we take into account that the In composition varies over a distance of about 15 nanometers along the growth direction (Figure 7.4 c). We thus interpolate the EDX line profile with an error function, which is then used to determine the lattice parameter of the  $\text{In}_x\text{Ga}_{1-x}\text{As}$  segment, assuming Vegard's law. Finally, we compute the resulting strain fields relative to the GaAs lattice parameter to be consistent with the GPA experimental data.



**Figure 7.4:** Geometry and composition of the nanowire designed for numerical simulations. a) Simulated cylindrical  $\text{In}_x\text{Ga}_{1-x}\text{As}$ -on-GaAs nanowire heterostructure which mimics the nanowire interface from image (b). b) HAADF STEM image of the InAs-on-GaAs nanowire taken along the  $[2\bar{1}\bar{1}0]$  viewing direction (nanowire X3, sample NW348). c) EDX line profile of the In composition along the growth axis of the nanowire from image (b). The red curve is the interpolation used in the simulations.

Both components of the simulated strain field,  $E_{\perp}$  (Figure 7.5 a) and  $E_{\parallel}$  (Figure 7.5 b) are in good agreement with the experimental results (Figure 7.3 b,e).



**Figure 7.5:** Strain maps from the simulated nanowire in Figure 7.4. a) Out-of-plane strain component  $E_{\perp}$ . b) In-plane strain component  $E_{\parallel}$ .

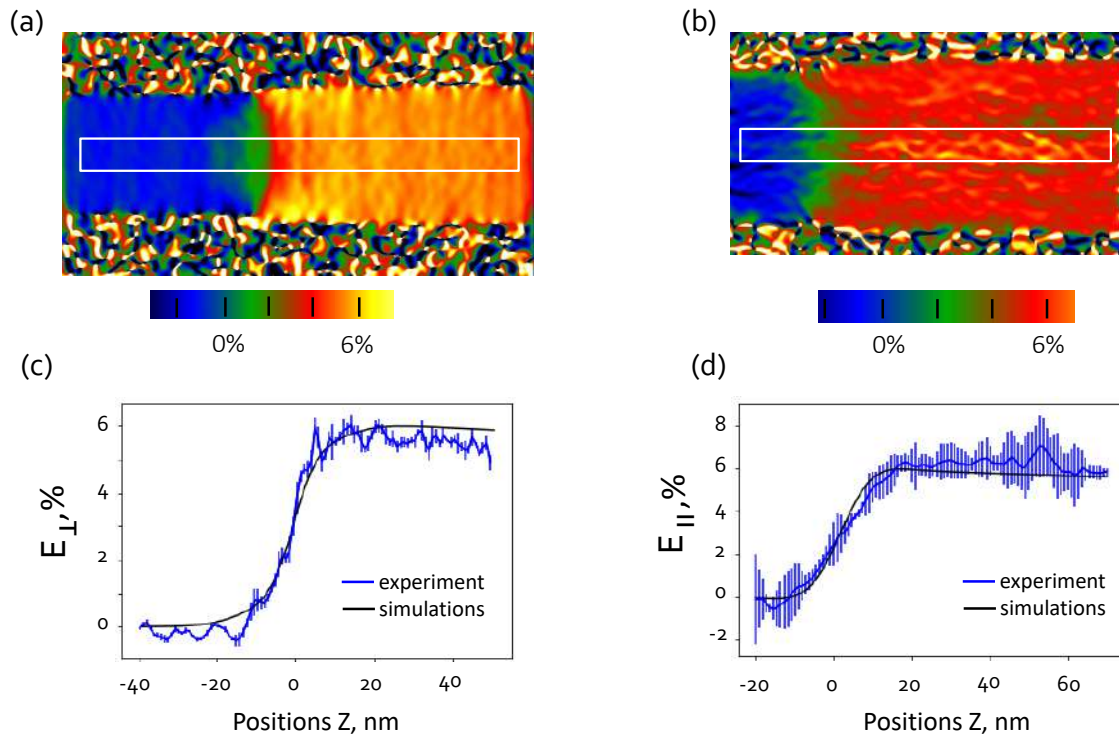
In the simulated  $E_{\perp}$  map, the blue and the orange segment represent unstrained GaAs (0%) and unstrained  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  (6% as relative to the GaAs), respectively. The color gradient at the interface corresponds to the strained region. Along the axis of the nanowire,  $E_{\perp}$  remains positive and increases when moving from GaAs to  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$ . On the nanowire sidewalls in the vicinity of the interface however,  $E_{\perp}$  changes sign from negative on the GaAs side to positive on the  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  side. This strain behavior is in good agreement with the GPA analysis (Figure 7.3 b).

In the simulated  $E_{\parallel}$  map, the violet color corresponds to the unstrained GaAs layer and the red color to the unstrained  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  layer. The strained region in the vicinity of the interface shows good agreement with the green flames observed in the GPA map (Figure 7.3 e).

To quantitatively compare the experimental and simulated results, we extract line profiles of  $E_{\perp}$  and  $E_{\parallel}$  along the nanowire axis, as shown in Figure 7.6. The experimental line profiles are averaged over a box of 8 nanometers as indicated in Figure 7.6 a,b. We use standard deviation as error bars for the experimental line profiles. The simulated data is extracted directly from the simulated strain maps as the line profile along the center of the nanowire (position  $x = 0$  in Figures 7.5 a,b). We find that despite a small discrepancy between experimental and simulated values ( $\leq 0.5\%$ ) the results show good agreement. A slow change takes place from 0% (GaAs reference) to about 6% ( $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  segment) which is consistent with the theoretical lattice mismatch of 6% between the segments. The change occurs over a distance of 30-40 nanometers and exceeds by far the compositional gradient of 14 nanometers (7.5 c,d). Given that the line profiles are taken along the nanowire core, where surface relaxation effects are negligible, the 30-40 nm corresponds to the region which is strained.

We observe that the experimental profile of  $E_{\perp}$  gives slightly lower values of strain compared to the simulated results. In contrast, the experimental  $E_{\parallel}$  values are 0.5% higher in the  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$





**Figure 7.6:** Quantitative comparison of the experimental and simulated strain fields.  $E_{\perp}$  (a) and  $E_{\parallel}$  (b) strain maps of the  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$ -on-GaAs nanowire from Figure 7.4 b (nanowire X3, sample NW348). c) Line profile of the boxed area in (a) taken from left to right (in blue, with error bars) and the simulated line profile (in black). d) Line profile of the boxed area in (b) taken from left to right (in blue, with error bars) and the simulated line profile (in black).

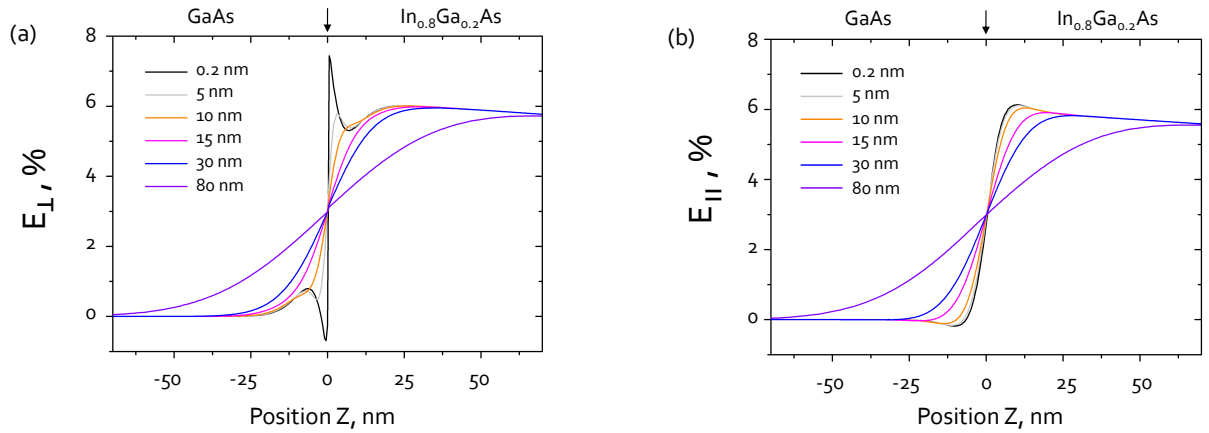
segment compared to the finite element results. Different reasons can cause the discrepancy between the experimental and simulated values. First of all, the experimental results are strongly influenced by STEM scanning errors (such as a shift which can happen between scanning lines). In addition, distortions induced by sample drift or environmental vibrations introduce errors in strain measurements [161]. While the first type of scanning errors is eliminated by choosing a proper scan direction (parallel to the strain direction), the other distortions will still introduce noise (especially noticeable in Figure 7.6 c). For example, Chung et al [161] observed strain fluctuations of 0.25% within sample areas with theoretical  $E_{\perp} = E_{\parallel} = 0\%$ . Moreover, GPA strain measurements are partly limited by the size of the mask applied to the selected Bragg peaks in the Fourier space. The bigger the mask size in the reciprocal space, the better the spatial resolution yet the lower the signal-to-noise ratio (see Chapter 3). Here we use a medium-sized mask in order to preserve a balance between a good spatial resolution and a high signal-to-noise ratio. In consequence, the strain level is slightly averaged. This could explain why the experimental profile of  $E_{\perp}$  gives slightly lower values of strain compared to the simulated results. Finally, the EDX interpolation used to extract  $a_{\text{InGaAs}}$  and  $c_{\text{InGaAs}}$  lattice parameters introduces an error in the simulations and

therefore causes some additional discrepancies between the theory and experiment.

In conclusion, GPA is an accurate tool to measure experimentally the strain distribution in nanowire heterostructures with only an introduction of some noise. We found that 6% strain is present at the  $\text{GaAs}/\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  interface in good agreement with the simulations. The strain relaxation occurs along a region of 30-40 nanometers via elastic relaxation: planes bend close to the nanowire sidewalls.

### Influence of the interface sharpness on the strain field

As we saw above, an  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As-on-GaAs}$  nanowire with 20 nanometers diameter and interface sharpness of 15 nanometers has the possibility to relax 6% lattice mismatch in the vicinity of the interface without the introduction of misfit dislocations. The length of the strained region was found to depend on strain-relaxation effects and the interface sharpness. We now simulate how the interface sharpness influences both the size and the shape of the strained region along the interface. We consider the nanowire from Figure 7.4 a) and vary the interface length between 0.2 and 80 nanometers. The results are presented in Figure 7.7.



**Figure 7.7:** Influence of the interface sharpness on the strain field.  $E_{\perp}$  (a) and  $E_{\parallel}$  (b) profiles calculated for the  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As-on-GaAs}$  nanowire from Figure 7.4 assuming different sharpness of the interface (between 0.2 and 80 nanometers). The interface is indicated with the arrow.

Both the shape and the size of  $E_{\perp}$  (Figure 7.7 a) and  $E_{\parallel}$  (Figure 7.7 b) strain profiles along the nanowire axis vary significantly with the interface sharpness. Yet, the profile of  $E_{\perp}$  undergoes the highest change. We find that when the interface is atomically abrupt (interface length of 0.2 nanometers) a compressive strain on the GaAs side and an even more pronounced tensile strain on the  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  side exists. The compressive strain reaches -0.7% and the tensile strain reaches 7.4% over a distance of a few nanometers from the interface. This is a signature of an abrupt shift in  $c$  lattice parameter. Strain relaxation takes place over a total distance of 20 nanometers on each

side of the interface and corresponds to the nanowire diameter. A qualitatively similar profile is observed, yet with smaller values of the compressive and tensile strain, when the interface length increases to 5 nanometers. When the interface length exceeds 10 nanometers, however, the compressive strain on the GaAs side and the tensile strain on the  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  side near the interface disappear and residual strain features are detected only far from the interface along the profile. The lattice parameter is observed to slowly but continuously change while crossing the interface. Strain-relaxation effects vanish completely when the interface length exceeds 30 nanometers.

The profile of  $E_{\parallel}$  (Figure 7.7 b) shows variations of the  $a$  lattice parameter when passing from GaAs to  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  even for atomically sharp interface (0.2 nanometers). We observe a  $\sim 7$  nm tensile strained region in GaAs and a  $\sim 7$  nm compressive strained region in  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$ . The length of the strained regions increases while the magnitude of the strain value decreases with increasing interface lengths. Similar to the  $E_{\perp}$ , strain relaxation totally disappears when the interface length becomes larger than 30 nanometers.

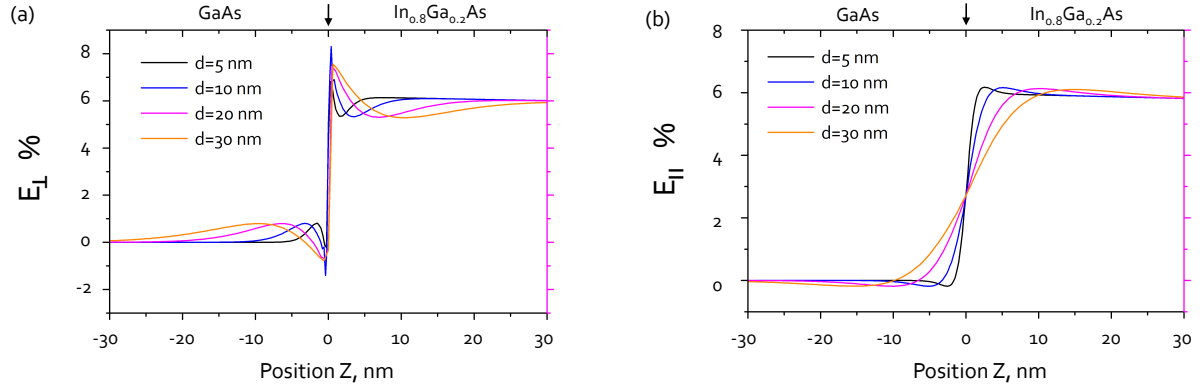
In conclusion, our simulations demonstrate that the interface sharpness strongly influences the strain distribution at the GaAs/InGaAs interface. The sharper the interface between the involved materials the higher the mechanical strain. These results suggest that dislocations free interfaces are easier to achieve when the chemical composition varies smoothly from one material to the other one.

### Influence of the nanowire diameter on the strain field

We are now interested in how the nanowire diameter influences the strain distribution along the heterointerface. We consider the nanowire from Figure 7.4 a) with an abrupt interface of 0.2 nanometers and vary its diameter between 5 and 30 nanometers, such that we are always below the theoretical critical diameter for misfit dislocation formation [14]. The results are presented in Figure 7.8.

Looking at  $E_{\perp}$  (Figure 7.8 a), we always observe a compressive region on the GaAs side and a tensile region on the  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  side for all simulated profiles. Yet, the amplitude of both the strained region and its length evolve with the nanowire diameter. The smallest amplitude and length were found for the smallest nanowire diameter ( $d = 5$  nanometers): the lattice parameter abruptly changes over a short distance from the interface. When the nanowire diameter increases to 10 nanometers, the strain amplitude jumps significantly and reaches a maximum value amongst all profiles. The length of the strained regions becomes slightly broader than for the nanowire with 5 nanometers diameter, indicating that strain relaxation spreads over a longer distance when increasing the diameter.





**Figure 7.8:** Influence of the nanowire diameter on the strain field.  $E_{\perp}$  (a) and  $E_{\parallel}$  (b) strain profiles calculated for the  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As-on-GaAs}$  nanowire from Figure 7.4 assuming an abrupt interface and different diameters between 5 and 30 nanometers. The interface is indicated with the arrow.

The  $E_{\parallel}$  strain profile (Figure 7.8 b) exhibits a tensile strain on the GaAs side and a compressive strain on the  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  side for all simulated diameters. The amplitude of the strain decreases for larger diameters and the length of the strained region is larger on both sides of the interface.

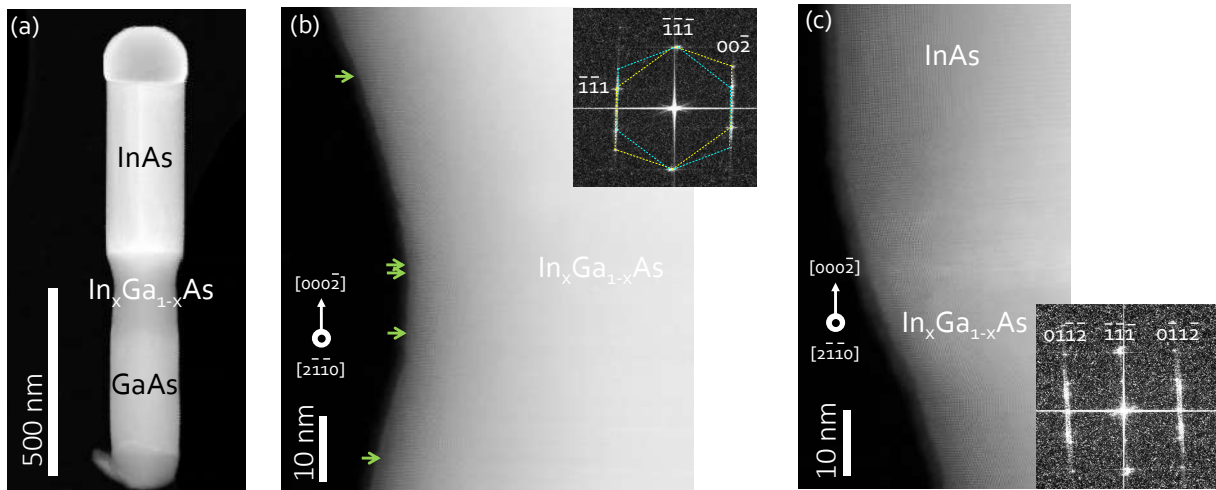
Our simulations demonstrate that the most efficient relaxation of the misfit strain happens for narrow nanowires due to close proximity of the nanowire sidewalls.

## 7.2 Nanowires with diameters above the critical diameter

### Crystalline quality

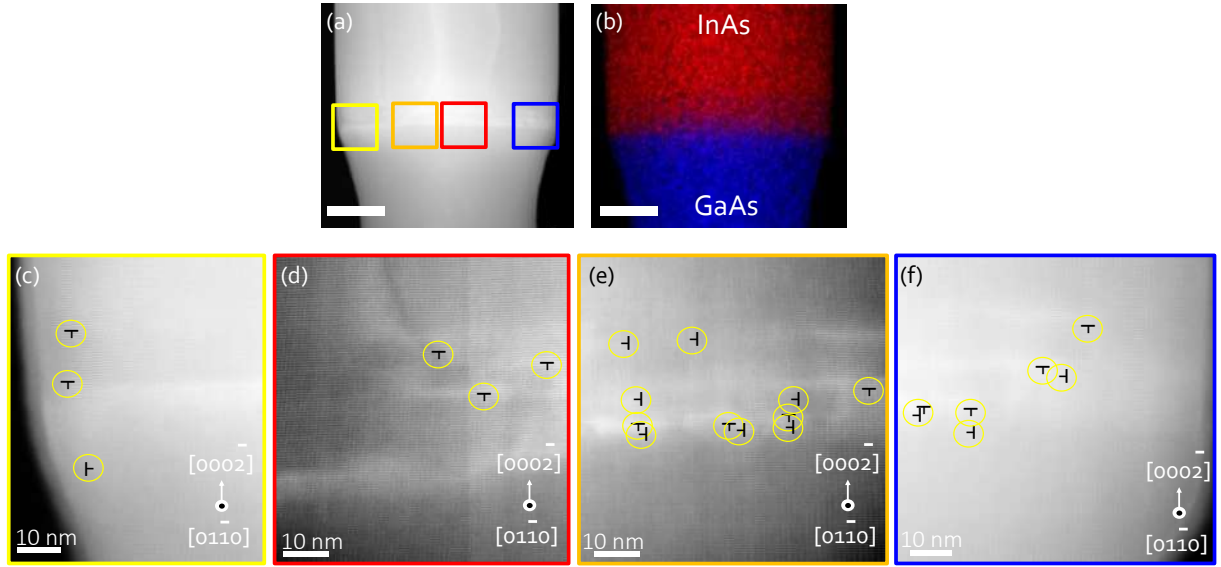
#### *Crystal structure:*

As discussed previously, the theoretical calculations of Frank Glas [14] predicted the formation of misfit dislocations in axial nanowire heterostructures with 7% lattice mismatch for diameters above 40 nanometers. We investigate InAs-on-GaAs axial nanowires grown with 50 nanometers gold colloids (Table 7.1) in order to verify calculations of Frank Glas. Three nanowires from the same sample were analyzed by TEM and GPA. We present here a complete study of nanowire 6 (sample NW498, see table 7.1), whose diameter at the interface is 168.5 nanometers and is largely above the critical diameter.



**Figure 7.9:** Crystal structure of an InAs-on-GaAs nanowire from sample NW498 (nanowire 6, Table 7.1). (a) Dark-field TEM image taken along the  $[2\bar{1}\bar{1}0]$  viewing direction. (b) High resolution HAADF-STEM image of the GaAs/InGaAs transition region from (a). The region has a highly defective zinc blende crystal structure with twins as confirmed by the Fast Fourier Transformation, shown as an inset. The arrows point on twin planes. (c) High resolution HAADF-STEM image of the GaAs/InGaAs transition region together with first layers of InAs. The crystal structure changes from defective zinc blende to wurtzite as seen in the FFT.

The nanowire structure and its crystalline quality were analyzed by TEM. Similar to the thin nanowires investigated before, we observe a characteristic broadening of the nanowire diameter at the interface between GaAs (bottom segment) and InAs (top segment) (Figure 7.9 a). From EDX measurements of this nanowire (presented in Chapter 6) we know that the In<sub>x</sub>Ga<sub>1-x</sub>As interface length is  $\sim 90$  nanometers with  $x$  varying from 0.0 to 1.0. HAADF STEM images of the In<sub>x</sub>Ga<sub>1-x</sub>As transition region viewed along the  $[2\bar{1}\bar{1}0]$  zone axis are shown in Figure 7.9 b and c.



**Figure 7.10:** Crystal quality of the InAs-on-GaAs nanowire from Figure 7.9. (a) STEM image of the nanowire interface taken along the  $[0\ 1\ \bar{1}\ 0]$  zone axis. (b) Overlay image of In and Ga EDX elemental maps of the nanowire from a) showing the interface border. The scale bar is 50 nanometers. (c)-(f) Four successive high resolution HAADF-STEM images viewed along the  $[0\ 1\ \bar{1}\ 0]$  zone axis, acquired across the nanowire interface from left to right, as indicated by the square boxes in a). Positions of misfit dislocations are indicated with the  $\perp$ .

We find that the  $\text{In}_x\text{Ga}_{1-x}\text{As}$  segment exhibits a zinc blende crystal structure with a high density of twin planes as confirmed by the associated FFT (Figure 7.9 b). After the transition region, the InAs segment grows with a wurtzite crystal phase. This is evidenced by the appearance of additional Bragg peaks in the FFT (Figure 7.9 b). We find that the nanowire growth direction is As polar or  $[000\bar{2}]$  similar to the thin nanowires.

#### Interface quality:

We then carefully investigated HAADF STEM images of the nanowire interface taken along the  $[0\ 1\ \bar{1}\ 0]$  viewing direction for the presence of misfit dislocations (Figure 7.10). It is worth noting that we were forced to divide the interface across the nanowire into four parts and acquire four successive HAADF STEM images owing to the large nanowire diameter of  $\sim 170$  nanometers (Figure 7.10 c-d)). The images have a minor vertical misalignment, yet they are all taken across the interface. The position of the interface is verified by the overlay image of In and Ga EDX elemental maps (Figure 7.10 b). By looking at the images, we notice blurred areas where a high resolution information is partly missing. By exploring these areas, we find randomly distributed misfit dislocations inserted across and along the GaAs/InAs interface (marked with the  $\perp$  symbol). It is noticeable that the right side of the nanowire interface contains more misfit dislocations than the left one. The most defective region of the nanowire interface is found in Figure 7.10 c).

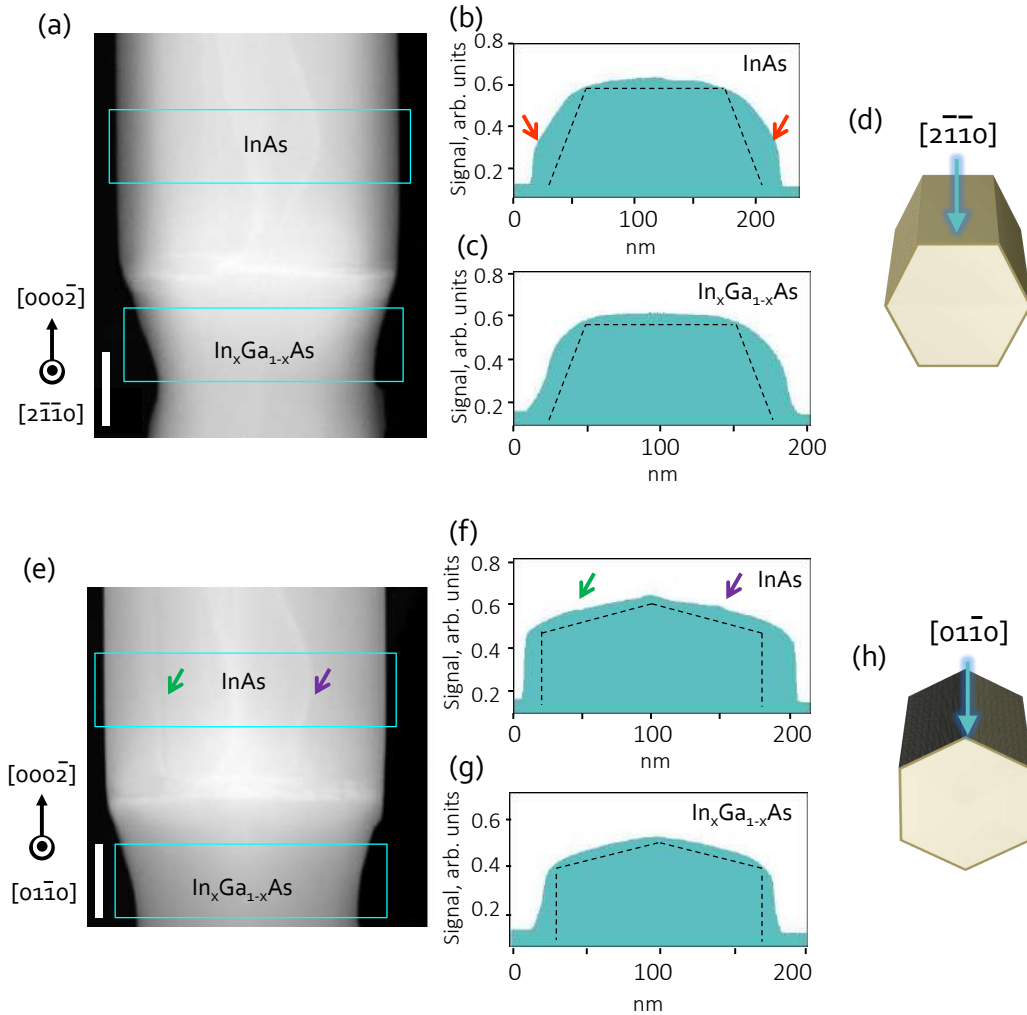
By paying special attention to the HAADF STEM images, we observe that horizontal and vertical planes of atoms are bent close to the nanowire sidewalls. We hence conclude that the strain between the layers is released both plastically (by the network of dislocations) and elastically (by planes bending). These two effects lead to a deterioration of the image resolution and blurred areas appear, making the visual inspection less accurate. For the same reason, we were not able to perform a Burgers vector analysis around the dislocation cores. Therefore, the images will be further analyzed with GPA in the next section to determine the type of misfit dislocations and their location.

### *Nanowire facets:*

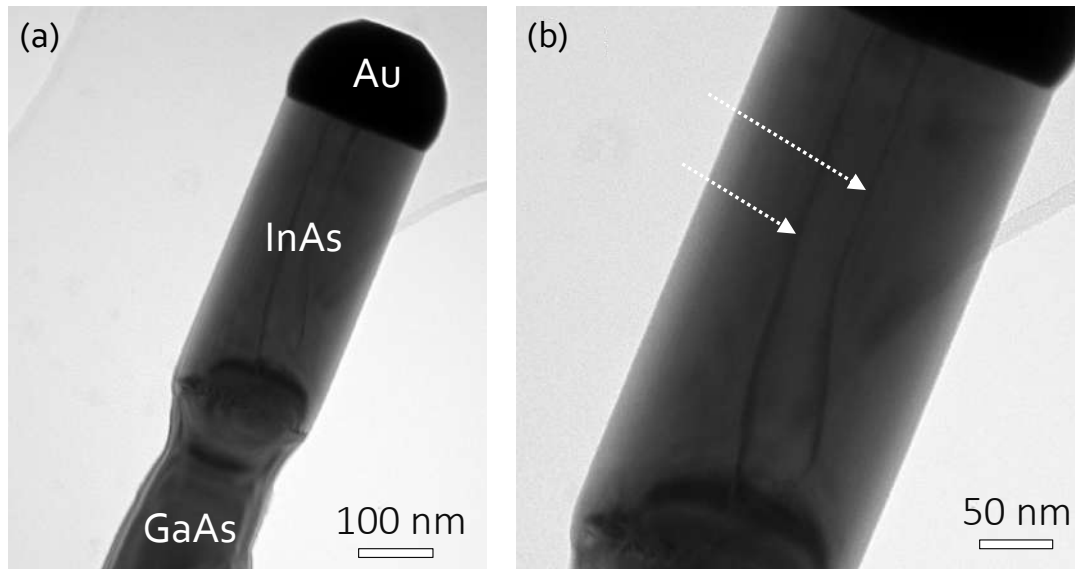
We investigated the crystal orientation of the nanowire sidewalls using HAADF STEM images taken along the  $[2\bar{1}\bar{1}0]$  (Figure 7.11 a) and the  $[01\bar{1}0]$  (Figure 7.11 e) zone axis. When the nanowire is viewed along the  $[2\bar{1}\bar{1}0]$  zone axis, intensity line scans across the InAs (Figure 7.11 b) and the  $\text{In}_x\text{Ga}_{1-x}\text{As}$  (Figure 7.11 c) segments show a flat central region, characteristic of  $\{\bar{2}110\}$  facets (Figure 7.11 d).

When the nanowire is viewed along the  $[01\bar{1}0]$  zone axis (Figure 7.11 e), profiles from InAs (Figure 7.11 f) and  $\text{In}_x\text{Ga}_{1-x}\text{As}$  (Figure 7.11 g) feature an intensity maximum in the center. This intensity peak corresponds to the nanowire edge, confirming the presence of  $\{\bar{2}110\}$  facets (Figure 7.11 h).

Paying special attention to the intensity profile across the InAs segment, one can notice additional features indicated by arrows in Figure 7.11 b and f. The left one corresponds to a thin, straight and elongated groove located at the left side of the InAs nanowire segment (Figure 7.11 f). The right feature results from an elongated bulge which has a brighter contrast than the rest of the nanowire. Similar bulges can be seen when the nanowire is viewed along the  $[2\bar{1}\bar{1}0]$  zone axis (Figure 7.11 a). Furthermore, we saw identical features on two other nanowires from the same sample. As the density of misfit dislocations is high and they are randomly distributed close to the nanowire interface, the bulges and/or the groove may be a signature of threading dislocations terminated at the nanowire sidewalls. On the other hand, large nanowires can potentially have more than six sidewall facets. For example, Vincent et al. reported that zinc blende Si nanowires with 80 nanometers diameter exhibit twelve facets [120]. Similar results can be also found in the work of Oehler et al. [162]. Therefore, the additional features we find on the intensity line scans may be a signature of  $\{0\bar{1}10\}$  facets. As a result, we took conventional TEM images on one of these thick nanowires to confirm that the additional features come from threading dislocations (Figure 7.12). We found at least two threading dislocations for the studied nanowire (NW6) which originate at the GaAs/InAs interface and continue along the InAs part.



**Figure 7.11:** Sidewall facets orientation of the InAs-on-GaAs nanowire from Figure 7.9. HAADF STEM images (scale bar 50 nanometers) of the nanowire taken along the  $[2\bar{1}\bar{1}0]$  (a) and the  $[01\bar{1}0]$  (e) viewing directions. Signal intensity across InAs (b) and  $\text{In}_x\text{Ga}_{1-x}\text{As}$  (c) obtained from (a). Signal intensity across InAs (f) and  $\text{In}_x\text{Ga}_{1-x}\text{As}$  (g) obtained from (e). The line profiles are averaged over a width of 50 nanometers. The facets in b) and f) show additional features. d),h) A reconstructed nanowire geometry with corresponding sidewall facets from (a) and (e), respectively.



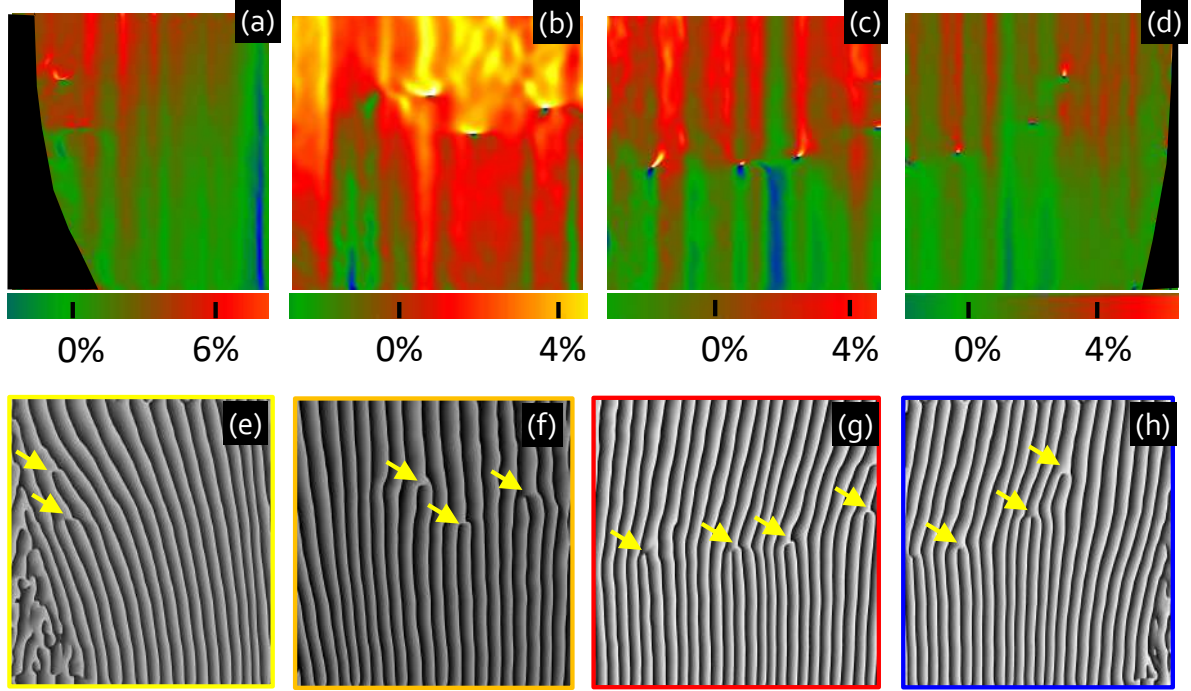
**Figure 7.12:** Conventional TEM images of the thick InAs-on-GaAs nanowire from Figure 7.9 indicating threading dislocations. (a) Bright field TEM image of the nanowire and (b) a zoomed view of its InAs part. The position of threading dislocations is indicated with the arrows.

## Strain mapping

We now investigate the interface between the InAs and GaAs segments by GPA. To do so, we use four successive HR HAADF STEM images from Figure 7.10. Figures 7.13 a-d show color maps of the in-plane component of strain  $E_{||}$ . Despite the presence of noise, visible as vertical bright stripes and caused by scanning errors, the GaAs/InAs interface is visible thanks to the gradual color change when moving from the bottom to the top of each image. We find that  $E_{||}$  changes from 0% (GaAs, used as a reference) to 4% (InAs, in reference to GaAs) in Figure 7.13 b,c and d. Given that InAs and GaAs have 7% lattice mismatch, the InAs is not relaxed yet. Interestingly, in Figure 7.13 a), which corresponds to the left side of the nanowire interface (near the nanowire sidewall), the strain surpasses larger variations from 0% in the GaAs part to 6% in the InAs part, indicating that the InAs lattice parameter  $a$  is almost recovered in this case. In all images, bright spots are visible; they correspond to misfit dislocations at the GaAs/InGaAs interface.

We then perform Moiré pattern analysis to visualize the misfit dislocations and other crystal deformations, caused by the mismatch strain. Figure 7.13 e-h shows extra half-planes which exist at the nanowire interface along the  $[2\bar{1}10]$  direction. The distribution of these extra planes is not homogeneous across the interface: the right side of the nanowire interface is more defective than the left one. This observation is in good agreement with the visual inspection of HR HAADF STEM images (Figure 7.10). In addition, we find a significant bending of the planes close to the nanowire sidewalls. The bending occurs through sidewall expansion. This means that strain relaxation for  $E_{||}$  at GaAs/InAs interfaces in nanowires with large diameters takes place both





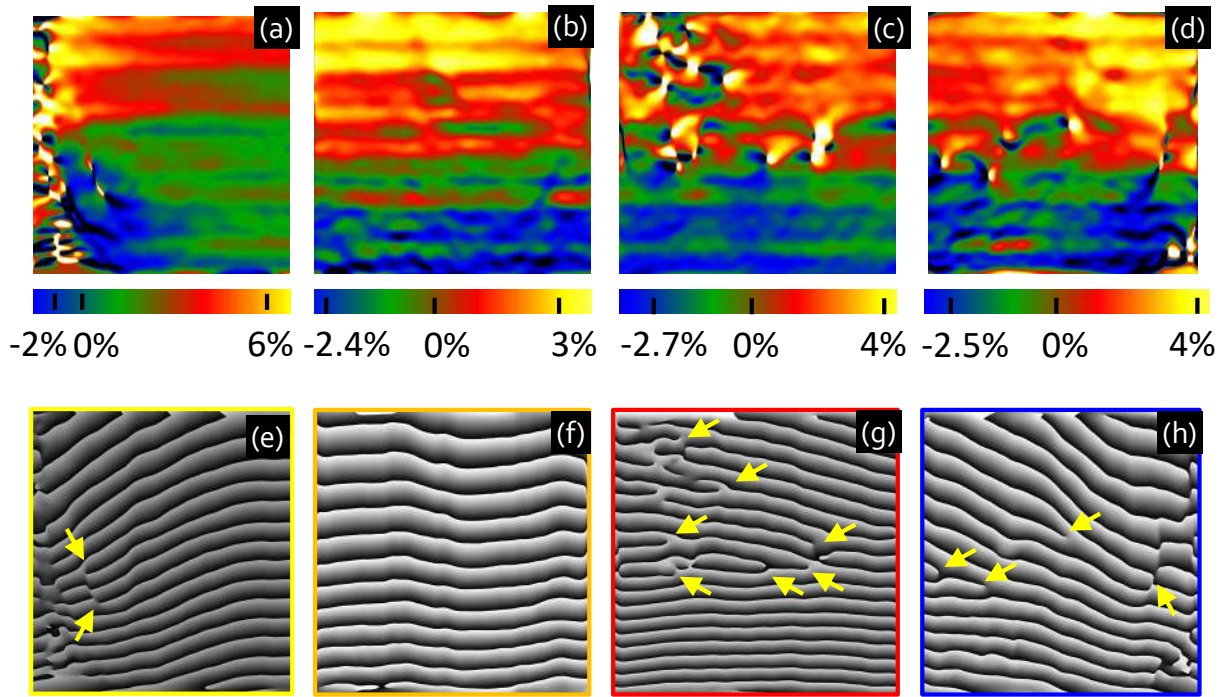
**Figure 7.13:** Strain mapping and Moiré pattern analysis of the nanowire interface from Figure 7.10 using  $(2\bar{1}\bar{1}0)$  Bragg peak a-d) The in-plane components of strain  $E_{\parallel}$ . e-f) Moiré patterns, obtained after Fourier filtering of the  $(2\bar{1}\bar{1}0)$  Bragg peak, displaying extra half-planes (marked by the arrows).

elastically and plastically, via planes bending close to the nanowire sidewalls and formation of misfit dislocations, respectively.

Note, that our GPA images are processed from HRSTEM images taken along the  $[0\ 1\ \bar{1}\ 0]$  zone axis. Generally, dislocations lines have  $\langle 2\bar{1}\bar{1}0 \rangle$  direction in wurtzite (or equivalent  $\langle 110 \rangle$  direction in zinc blende). To correctly visualize the dislocation nature, images have to be taken in the direction parallel to the dislocation line (i.e. the nanowire has to be viewed along the  $[2\bar{1}\bar{1}0]$  direction in wurtzite notation). This means, that Moiré images displayed in Figure 7.13 e-h can only help us to estimate the position of dislocations. Yet, information about their nature is missing since dislocation lines are inclined relative to the  $[0\ 1\ \bar{1}\ 0]$  zone axis. Therefore, to estimate the nature of the dislocations (their type), we performed GPA analysis on HRSTEM images taken along the  $[2\bar{1}\bar{1}0]$  viewing direction (see Chapter A).

We then investigate the out-of-plane strain distribution  $E_{\perp}$  and the behavior of planes along the  $[000\bar{2}]$  direction. Figure 7.14 a-d presents color maps of  $E_{\perp}$ . It shows that different strain fields are present in GaAs (bottom, blue) and InAs (top, orange). A compressive strain of about -2.5% on the GaAs side is easily observed. The expected tensile strain on the InAs side is hard to distinguish: we observe a strain of 4% (Figure 7.14). It is worth noting that  $E_{\perp}$  obtained from the





**Figure 7.14:** Strain mapping and Moiré pattern analysis of the nanowire interface from Figure 7.10 using the  $(000\bar{2})$  Bragg peak. a)-d) The out-of-plane components of strain  $E_{\perp}$ . e)-f) Moiré patterns of the images, obtained after Fourier filtering of the  $(000\bar{2})$  Bragg peak, displaying extra planes (marked by the arrows).

left side of the nanowire (close to the nanowire sidewall, Figure 7.14 a) varies from -2% to 6%, indicating asymmetry across the nanowire interface, similar to the  $E_{\parallel}$ . Moreover, we find bright spots only in three out of four regions of the nanowire interface (Figure 7.14 a,c and d). The strain centers represent dislocations cores. To further investigate the dislocation distribution, we use Moiré pattern analysis (Figure 7.14 e-h).

The first thing we notice is that the right side of the nanowire interface is highly defective (Figure 7.14 g,h) while the left side is almost free of misfit dislocations (Figure 7.14 e,f). These dislocations are unfinished planes which exist along the  $[000\bar{1}]$  direction with a Burgers vector of  $\frac{1}{2}[000\bar{1}]$ . At the same time, we also notice a large bending of the  $c$  planes close to the nanowire sidewalls. This confirms that strain relaxation occurs through elastic deformation of planes and partially through the formation of misfit dislocations (as observed for the  $a$  planes before).

We now discuss why the InAs-on-GaAs nanowires with large diameters exhibit elastic and plastic relaxation of misfit strain. We demonstrated that when the nanowire diameter exceeds the critical diameter value, there still exists an elastic relaxation near the nanowire sidewalls, which partially reduces the mismatch strain. This results in an increased spacing between misfit dislocations from the nanowire axis to the nanowire sidewalls. For example, Frigeri et al. reported that the average spacing between dislocations increases from 4 nanometers (at the center of the

interface) to 6.5 nanometers (near the sidewalls) in InAs-on-GaAs nanowires with diameters above the critical one [68]. We indeed observe that the density of misfit dislocations is increased near the center of the nanowire interface (Figure 7.13) coupled with the planes bending near the nanowire sidewalls. Yet, there is no periodicity between the dislocations spacing even near the nanowire center. Interestingly, while the interface is less defective near the nanowire sidewalls (Figure 7.13 e,h), we find two closely positioned misfit dislocations right at the sidewalls (Figure 7.13 e). Moreover, we constantly observe an asymmetry in the density of misfit dislocations between the left and the right side of the nanowire interface. In wurtzite crystals, edge dislocations along the  $[2\bar{1}10]$  direction glide along the (0001) plane, meaning that the dislocation line can move along the (0001) plane through the entire nanowire. The gliding of dislocations results in their non-periodic distribution and hence some parts of the nanowire interface are more defective than the others.

### 7.3 Conclusions

To conclude, we performed strain measurements along GaAs/ $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  and GaAs/InAs nanowire interfaces, with different nanowire diameter and interface sharpness.  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As-on-GaAs}$  nanowires with diameters below 46 nanometers are free of misfit dislocations regardless of the interface sharpness (5-26): the 6% strain is completely elastically relaxed within the strained region in the vicinity of the interface. Elastic relaxation occurs via crystalline planes bending close to the nanowire sidewalls. The experimental results are in good agreement with finite element simulations. They confirm that strain in our nanowires arises from the mismatched interface and not from external forces. Our experimental findings confirm that heterointerfaces with 6% lattice mismatch are pseudomorphic in axial nanowires for diameters below 50 nanometers.

On the other hand, we find that 7% mismatched InAs-on-GaAs nanowires with diameters above 95 nanometers at the interface exhibit strain relaxation, both elastically and plastically, via planes bending and the formation of misfit dislocations, respectively. These results are unexpected, because the theoretical calculations reported by Glas predict complete plastic relaxation of the strain at the GaAs/InAs interface for nanowires with diameters above 100 nanometers [14]. The asymmetric distribution of the misfit dislocations across the interface could find an explanation through the gliding of edge dislocations along the (0001) plane. Furthermore, the misfit dislocations produce threading dislocations ending at the nanowire sidewalls.

In summary, this study illustrates different strain relaxation mechanisms that occur in nanowire heterostructures and strongly depend on the nanowire diameter. Elastic relaxation allows epitaxial growth of materials with large lattice mismatch as long as the wire diameter is smaller than a critical value.

# Chapter 8

## General conclusions and perspectives

### 8.1 General conclusions

The long term objective of this thesis is to grow optically active low band-gap InAs quantum dots inside nanowire heterostructures for the implementation of on-chip optical light emitters and highly sensitive detectors at telecommunication wavelengths. In order to reach this ambitious goal, we have set the following objectives:

1. to demonstrate the possibility of combining III-V and Si in nanowire heterostructures;
2. to grow pure wurtzite Au-assisted GaAs nanowires on Si (111) substrates;
3. to grow dislocation-free and straight InAs-on-GaAs nanowire heterostructures on Si (111) substrates;
4. to understand the strain distribution at the InAs/GaAs interface.

#### *1) Combining III-V and Si in nanowire heterostructures*

In the first part of this thesis, we demonstrated the possibility of combining III-V and Si in nanowire heterostructures. We grew GaAs segments on top of Si nanowire stems by re-using the gold catalyst present at the Si tips. We found that the GaAs segments grow between 470 °C and 670 °C, in good agreement with previous works on the Au-assisted growth of GaAs nanowires on Si and GaAs substrates. The Si/GaAs nanowire heterostructures were studied by transmission electron microscope and scanning electron microscope. We found that the GaAs segment at the Si tip is kinked and exhibit a poor crystalline quality. Kinks are a direct consequence of the initial position of the Au droplets on the Si nanowire before GaAs growth: we find that the Au droplets do not sit on the upper planar facet, but on a {100} facet oriented at 54° angle of the nanowire growth direction.

Another challenge is GaAs nanoneedles, which grow unintentionally on the Si nanowire sidewalls because of parasitic gold clusters. The parasitic clusters form during the Si nanowire growth process. The angle between nanoneedles and the Si nanowire growth direction as well as their presence only on three facets suggest that the sidewalls of Si nanowires have a saw-tooth faceting with a characteristic three-fold symmetry. We also speculate that the gold clusters are anchored only on the  $\{111\}$ -upward-oriented saw-tooth facets, promoting the growth of nanoneedles with a constant angle. Finally, we find a parasitic GaAs overgrowth on the sidewalls of the Si nanowires. These issues are a direct consequence of the vapor-liquid-solid growth of Si nanowires in a low pressure chemical vapor deposition reactor and can be potentially avoided if the Si stems would be prepared by some other way. We therefore propose to form the Si stems by a top-down approach, where Si nanowires are etched out of bulk silicon with the gold droplets used as a mask. In order to test our idea, we performed preliminary studies using reactive-ion etching of Si (111) substrates to obtain Si nanowires. Importantly, we observed that the position of the gold droplets, which are deposited on the surface of bulk silicon, is unchanged during the whole etching process. Moreover the etching process is performed at relatively low temperatures ( $\sim 50$  °C), which prevents the migration of gold from the droplet to the sidewalls of etched Si nanowires. In addition, we avoid faceting, which is the result of self-assembling in the vapor-liquid-solid growth of nanowires. We therefore demonstrate an alternative way to create Si nanowires in order to combine Si and GaAs in nanowire heterostructures.

## *2) Growth of pure wurtzite GaAs nanowires on Si (111) substrates*

The crystal phase purity of nanowires is crucial for the performances of nanowire-based devices, because crystal defects act as traps and scattering centers for the charge carriers. Thereby it is important to minimize the occurrence of stacking faults during nanowire growth. Here, we focused on the Au-assisted growth of pure wurtzite GaAs nanowires on Si (111) substrates by molecular beam epitaxy.

We first investigated the nucleation process of the GaAs nanowires on Si (111) substrates. We observed a delay in the nucleation: the first vertical GaAs nanowires appear on the substrate only after 3 minutes of materials deposition. Before that, in-plane GaAs traces form and grow horizontally until they cover the entire Si substrate surface. Our results are in good agreement with the work reported by Breuer et al. [118]. The traces are formed owing to a lower interface energy of Au-Ga droplets on Si ( $\gamma \leq 35 \text{ meV}\text{\AA}^{-2}$ ) compared to the surface energy of Au-Ga droplets on GaAs (111)B ( $\gamma \geq 43 \text{ meV}\text{\AA}^{-2}$ ). We then studied the influence of the growth temperature and material fluxes on the GaAs nanowire morphology and crystal structure. We found that the GaAs nanowires grow for all chosen substrate temperatures (550, 590 and 610 °C). Yet, nanowires feature homogeneity in height and diameter and grow with the highest growth rate at 610 °C, owing to the enhanced Ga diffusion from the substrate. We also demonstrated that the axial growth of nanowires is controlled by the group-V flux.

We then studied the GaAs nanowires crystal structure by transmission electron microscopy. We observed that at a V/III beam equivalent pressure ratio of 15, most of the nanowires have a wurtzite crystal structure with a high density of stacking faults. When the V/III beam equivalent pressure ratio increases up to 30, the nanowires grow with a pure wurtzite crystal phase. The nanowires exhibit less than four stacking faults per micrometer. We established that high V/III flux ratios are also necessary to obtain GaAs nanowires with uniform diameters and minimized tapering.

### *3) Growth of dislocation-free straight InAs-on-GaAs nanowire heterostructures on Si (111) substrates*

The growth of axial nanowire heterostructures is challenging when switching group III elements. The problems that potentially arise are: a kinking in one of the two interface directions, graded and asymmetric interfaces and a parasitic radial growth. Moreover, the crystalline quality of the interface is strongly affected by the strain caused by the materials lattice mismatch. The mismatch imposes severe conditions on the choice of the nanowire diameter. For example, dislocation-free InAs/GaAs interfaces (7% lattice mismatch) require in theory diameters smaller than 40 nanometers.

In this work, we successfully fabricated dislocation-free axial InAs-on-GaAs nanowire heterostructures on silicon with a yield of 92% using 20 nanometers gold colloids. We studied extensively the nanowire growth protocol and established that the key ingredient to obtain straight InAs-on-GaAs nanowires is to keep the Au droplet stable. In order to achieve this, we developed a two-step growth procedure enabling to maintain a high supersaturation in the Au catalyst during the materials switch from Ga to In.

We observed that the growth temperature plays an important role in the morphology of the InAs-on-GaAs nanowire heterostructures. We identified three temperature regimes. At low growth temperatures (below 500 °C) there is no InAs axial growth. A thick and irregular InAs shell surrounds the GaAs nanowires. At high growth temperatures (above 570 °C), we find axial InAs segments on top of GaAs stems, but the segments kink most of the time. Finally, at the optimum growth temperature of 540 °C, the yield of straight InAs segments reaches a maximum regardless of the In flux.

By tuning carefully the material fluxes supplied during growth, we significantly improved the interface sharpness between InAs and GaAs. Using a low In flux during the growth of InAs resulted in a 20 nm composition gradient at the InAs/GaAs interface. When the In flux is increased by a factor of 2, the interface gradient is as low as 5 nm thanks to faster Ga depletion from the Au droplet. Yet, high In flux led to an increase in the density of staking faults in the InAs segment, similarly to our wurtzite GaAs nanowires. It is thus necessary to find a compromise between improving the interface sharpness and preserving the nanowire crystal quality.

A detailed EDX analysis revealed that our nominally pure InAs segments contain a high concentration of Ga. Moreover, the Ga concentration is not constant along the nanowire growth axis and increases toward the nanowire tip. Through a careful analysis of all possible Ga sources, we established that Ga is most likely supplied from the diffusion of thermally created Ga atoms, formed on the GaAs nanowire sidewalls and on the two-dimensional GaAs layer grown on the Si substrate. We proposed several strategies to reduce the Ga concentration in the segment. Increasing the As flux, the Ga concentration in the InGaAs segment decreases from 25% to 15%. The Ga concentration in the InGaAs segment becomes negligible (less than 5%) for nanowires with large diameters (larger than 60 nanometers), owing to the transition from diffusion-induced to adsorption-induced growth mechanism. At large diameters, nanowire growth is governed by the adsorption-induced growth mechanism: only a direct impingement of material contributes to the nanowire elongation, eliminating thus the influence of Ga diffusion from the substrate surface and the nanowire sidewalls. Yet, the increase in the nanowire diameter above 40 nm deteriorates the crystal quality of the GaAs/InAs interface.

#### *4) Strain distribution along axial InAs-on-GaAs nanowires*

Finally, we performed strain measurements along  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}/\text{GaAs}$  (thin diameters) and  $\text{InAs}/\text{GaAs}$  (thick diameters) nanowire interfaces. To do so, we combined high-resolution scanning transmission electron microscopy with Geometrical Phase Analysis. We demonstrated that  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}/\text{GaAs}$  nanowires with diameters below 46 nanometers are free of misfit dislocations, regardless of the interface sharpness (between 5 and 26 nanometers). The 6% strain is fully elastically released within a strained region on both sides of the interface: elastic relaxation takes place via the bending of crystal planes close to the nanowire sidewalls. The length of the strained region depends on both the interface sharpness and the nanowire diameter. Our experimental results come in good agreement with the finite element simulations. Our findings confirm the prediction that interfaces with 6% lattice mismatch are pseudomorphic in axial nanowires with diameters below 50 nanometers [14].

On the other hand, we find that 7% mismatched  $\text{InAs}/\text{GaAs}$  nanowires with diameters above 95 nanometers at the interface relax strain both elastically and plastically, via plane bending and formation of misfit dislocations, respectively. These results were unexpected because theoretical calculations by Frank Glas predict complete plastic relaxation for nanowires with diameters above 100 nanometers [14]. We also observed an asymmetric distribution of the misfit dislocations across the interface. This asymmetry could be explained by the gliding of edge dislocations along the (0001) plane. We observed finally that the misfit dislocations produce threading dislocations ending at the nanowire sidewalls.

Our results are of significance for any nanowire heterostructures, especially if high quality thin tunnel barriers or quantum dots have to be produced in the final structure. For an efficient nanowire-based single-photon emitter, the quantum dot height is typically in the range 5–40

nm. We found that the strained region for the 20 nm in diameter  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}/\text{GaAs}$  nanowire heterostructure reaches 40 nanometers at the interface, meaning that the entire InAs quantum dot, inserted into a GaAs nanowire will be strongly strained. Strain deeply influences the band structure of semiconductors, and consequently the electronic and optical properties of final devices.

## 8.2 Perspectives

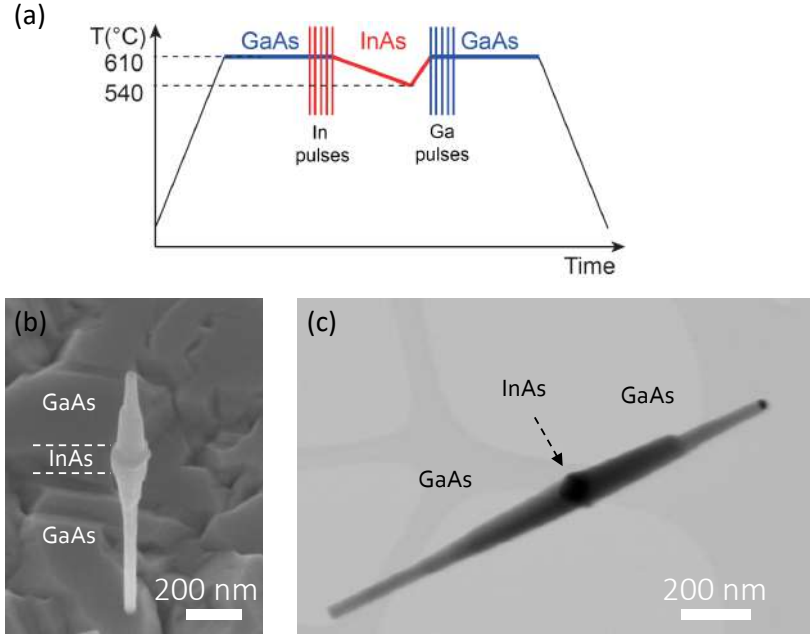
Our results establish a first step toward the realization of high quality InAs quantum dots in GaAs nanowires on silicon. We now have the experimental proof that InAs quantum dots can be realized in GaAs nanowires without dislocations for diameters below 46 nanometers. For our long term goals, it is important i) to grow InAs-on-GaAs nanowires with an homogeneous composition and a reproducible crystal quality, ii) to create a complete GaAs/InAs/GaAs structure, iii) to evaluate the emission properties of the grown structures. First of all, both the InAs crystalline phase purity and the GaAs/InAs interface sharpness have to be better controlled. For example, the interface sharpness can be improved with short pulses of In flux used after the Ga flux is switched off. The In pulses will decrease the equilibrium concentration of Ga in the gold droplet, resulting in abrupt GaAs/InAs interfaces [60]. The amount of In introduced to the droplet by pulses should be small enough to not initiate InAs growth before all the accumulated Ga is expelled. Similarly, the abruptness of the InAs/GaAs interface can be improved with short Ga pulses. We used this technique to grow a GaAs/InAs/GaAs nanowire heterostructure (see below). On the other hand, an homogeneous reproducible and controlled segment composition can be probably achieved if nanowires are grown on patterned Si substrates [163]. For this growth procedure, Si (111) substrates are typically covered with a silicon oxide mask, which has nano-openings. With appropriate Ga flux and growth temperature, GaAs nanowires grow selectively inside of the nano-openings while the oxide mask remains free from parasitic GaAs growth. We now briefly discuss preliminary work on the growth of GaAs/InAs/GaAs nanowire heterostructures, and on the numerical modeling of nanowire quantum dots.

### Growth of GaAs/InAs/GaAs nanowire heterostructures

We grew a complete GaAs/InAs/GaAs nanowire heterostructure as a preliminary test (Figure 8.1). We used 5 short pulses of In and Ga fluxes aimed to improve the interface sharpness on both sides of the InAs quantum dot (Figure 8.1 a). We observed a significant enlargement in the diameter of the structure along the growth axis (Figure 8.1 b). We attribute this diameter enlargement to the InAs region. Moreover, we find a characteristic dark contrast in bright-field scanning transmission electron microscopy (STEM) images at the expected position of the InAs segment (Figure 8.1 c). Further EDX measurements are required to determine the sharpness of the interfaces and



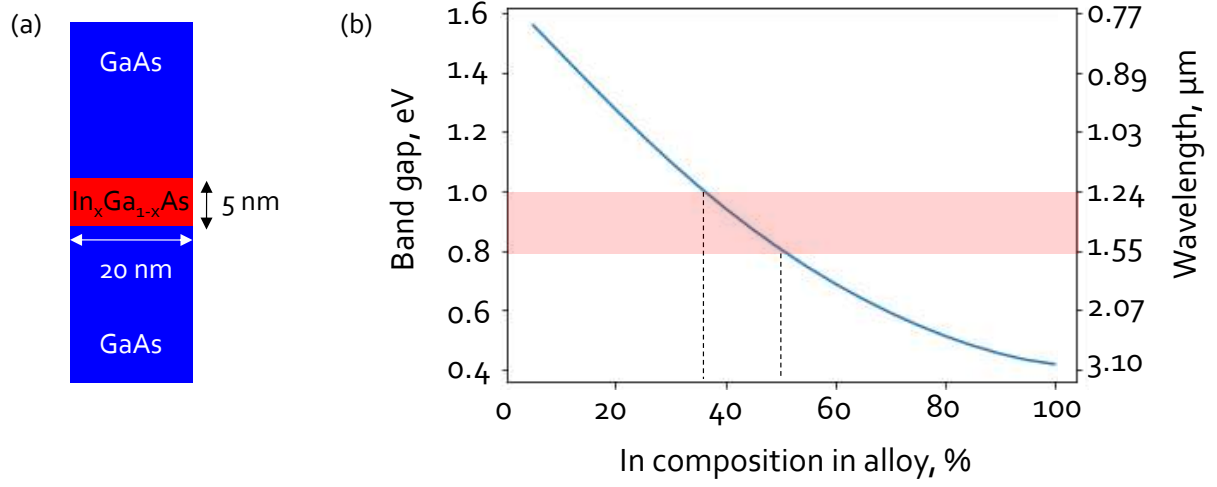
the chemical composition of the quantum segment. Photoluminescence measurements are also planned to investigate the optical properties of the structure.



**Figure 8.1:** GaAs/InAs/GaAs nanowire heterostructures grown on a Si(111) substrate. a) Scheme of the growth protocol. b) SEM image (30° tilt) of a typical GaAs/InAs/GaAs heterostructure from the sample. c) STEM image of a typical GaAs/InAs/GaAs heterostructure from the sample.

## Modeling of nanowire quantum dots

Finally, we evaluated the geometry and composition of the quantum dot required to reach the desired emission at telecommunication wavelengths. We developed a model of wurtzite-phase GaAs/InGaAs/GaAs nanowire quantum dot using the Nextnano3 software [164]. The complete structure is simulated in three dimensions. In a first step, the 3D strain distribution is calculated by minimization of the elastic energy, assuming zero stress at the nanowire surface. Then, the band profile is calculated by solving the Poisson-Schrodinger equation self-consistently, using the effective mass approximation. We focus on an  $\text{In}_x\text{Ga}_{1-x}\text{As}$  quantum dot, with a 5 nm height and a diameter of 20 nm. In Figure 8.2, the band gap is plotted as a function of In composition for the quantum dot. This  $\text{In}_x\text{Ga}_{1-x}\text{As}$  quantum dot will potentially emit light in the telecommunication wavelength window for an In concentration between 35% and 50%.



**Figure 8.2:** a) Scheme of the modelled InGaAs/GaAs single-quantum-dot nanowire. (b) Nextnano simulations of the  $\text{In}_x\text{Ga}_{1-x}\text{As}$  quantum dot band gap as a function of In composition of the alloy.

For efficient light emission, the wavefunctions of the electron and hole must overlap radially and axially to ensure a fast radiative recombination. We found that the wavefunction overlap of the modelled quantum dot is low due to strain. However, the addition of a thin  $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$  shell can significantly mitigate this issue.



## List of associated publications

- *Dislocation-free axial InAs-on-GaAs nanowires on silicon*  
Beznasyuk, D.V., Robin, E., Den Hertog, M., Claudon, J. and Hocevar, M.  
Nanotechnology, 2017, 28(36), p.365602.
- *Full interface characterization in highly-mismatched dislocation-free axial nanowire heterostructures*  
Daria V Beznasyuk, Petr Stepanov, Marcel Verheijen, Jean-Luc Rouvière, Julien Claudon, Moïra Hocevar  
In preparation



# Appendix A

## Appendix

### A.1 Voigt notation

Three-dimensional strain tensor:

$$\varepsilon = \begin{bmatrix} e_{11} & \frac{1}{2}(e_{12} + e_{21}) & \frac{1}{2}(e_{13} + e_{31}) \\ \frac{1}{2}(e_{12} + e_{21}) & e_{22} & \frac{1}{2}(e_{23} + e_{32}) \\ \frac{1}{2}(e_{13} + e_{31}) & \frac{1}{2}(e_{23} + e_{32}) & e_{33} \end{bmatrix} \quad (\text{A.1})$$

Strain tensor is symmetric and only 6 out of 9 components are independent:

$$\varepsilon = \begin{bmatrix} \varepsilon_{11} & \varepsilon_{12} & \varepsilon_{13} \\ \varepsilon_{12} & \varepsilon_{22} & \varepsilon_{23} \\ \varepsilon_{13} & \varepsilon_{23} & \varepsilon_{33} \end{bmatrix} \quad (\text{A.2})$$

By substituting indexes in the way:  $11 \rightarrow 1$ ,  $22 \rightarrow 2$ ,  $33 \rightarrow 3$ ,  $23$  and  $32 \rightarrow 4$ ,  $13$  and  $31 \rightarrow 5$ ,  $12$  and  $21 \rightarrow 6$ , the six independent components of the strain tensor are often represented in Voigt notation:

$$\varepsilon = \begin{bmatrix} \varepsilon_1 \\ \varepsilon_2 \\ \varepsilon_3 \\ \varepsilon_4 \\ \varepsilon_5 \\ \varepsilon_6 \end{bmatrix} \quad (\text{A.3})$$

Elasticity stiffness tensor  $\mathbf{C}$  is comprised of 81 components, yet only 36 of them are independent. Following the Voigt notation, the stiffness tensor can be represented in form of a  $6 \times 6$  matrix:

$$\mathbf{C} = \begin{bmatrix} C_{11} & C_{12} & C_{13} & C_{14} & C_{15} & C_{16} \\ C_{21} & C_{22} & C_{23} & C_{24} & C_{25} & C_{26} \\ C_{31} & C_{32} & C_{33} & C_{34} & C_{35} & C_{36} \\ C_{41} & C_{42} & C_{43} & C_{44} & C_{45} & C_{46} \\ C_{51} & C_{52} & C_{53} & C_{54} & C_{55} & C_{56} \\ C_{61} & C_{62} & C_{63} & C_{64} & C_{65} & C_{66} \end{bmatrix} \quad (\text{A.4})$$

The Hook's law:

$$\begin{bmatrix} \sigma_{11} \\ \sigma_{22} \\ \sigma_{33} \\ \sigma_{32} \\ \sigma_{31} \\ \sigma_{21} \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & C_{13} & C_{14} & C_{15} & C_{16} \\ C_{21} & C_{22} & C_{23} & C_{24} & C_{25} & C_{26} \\ C_{31} & C_{32} & C_{33} & C_{34} & C_{35} & C_{36} \\ C_{41} & C_{42} & C_{43} & C_{44} & C_{45} & C_{46} \\ C_{51} & C_{52} & C_{53} & C_{54} & C_{55} & C_{56} \\ C_{61} & C_{62} & C_{63} & C_{64} & C_{65} & C_{66} \end{bmatrix} \begin{bmatrix} \varepsilon_{11} \\ \varepsilon_{22} \\ \varepsilon_{33} \\ \tilde{\varepsilon}_{32} \\ \tilde{\varepsilon}_{31} \\ \tilde{\varepsilon}_{21} \end{bmatrix} \quad (\text{A.5})$$

where  $\tilde{\varepsilon}_{ij} = 2\varepsilon_{ij}$  ( $i \neq j$ ).

To build stiffness tensor for nanowires with zinc blende crystal structure, only 3 independent coefficients are required:  $C_{11}$ ,  $C_{12}$  and  $C_{44}$ . This happens due to equality of the three axis in the cubic crystal cell. For nanowires with wurtzite crystal phase, the stiffness tensor contains 5 independent coefficients:  $C_{11}$ ,  $C_{12}$ ,  $C_{13}$ ,  $C_{44}$  and  $C_{55}$ , since only two out of the three axis are equivalent in hexagonal crystal cell.

The values of elastic constants for wurtzite GaAs and wurtzite InAs materials, used in this thesis are indicated below.

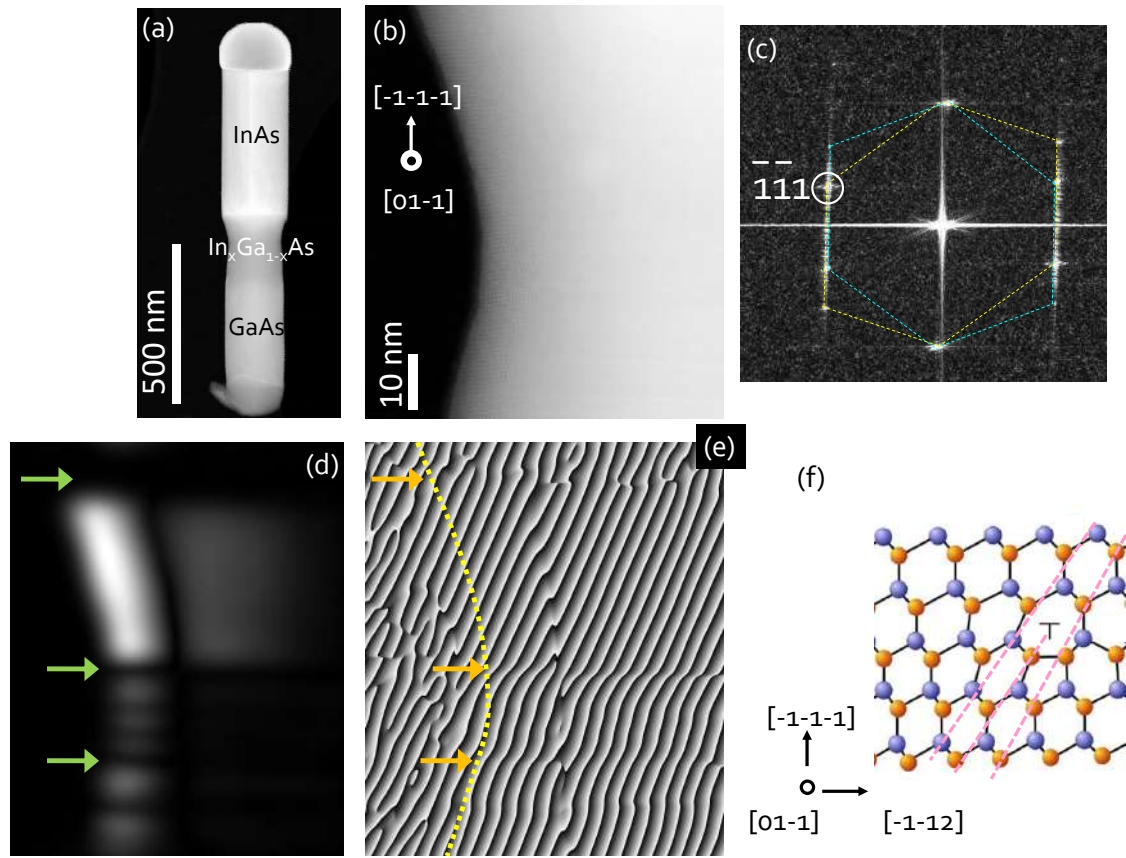
	$C_{11}$	$C_{12}$	$C_{13}$	$C_{33}$	$C_{44}$
GaAs	147.6	46.0	33.4	160.2	42.4
InAs	110.3	42.8	32.1	120.9	27.3

**Table A.1:** Table of elastic constants for GaAs and InAs in wurtzite crystal phase [165]. Values are given in GPa.

## A.2 The nature of dislocations in thick nanowires

Generally, dislocation lines have  $\langle 110 \rangle$  direction in zinc blende notation. To correctly visualize the dislocation nature, images have to be taken in the direction parallel to the dislocation line (i.e. the nanowire has to be viewed along the  $\langle 110 \rangle$  direction). To estimate the nature of dislocations





**Figure A.1:** (a) Dark-field TEM image taken along the  $[0\ 1\ \bar{1}]$  viewing direction. (b) High resolution HAADF-STEM image of the GaAs/InGaAs transition region from (a). The region has a highly defective zinc blende crystal structure with twins as confirmed by the Fast Fourier Transformation (FFT) in (c). (d) The image amplitude obtained from the FFT by filtering the  $(-1,-1,1)$  Bragg peak. Black zones along the nanowire axis (marked by the arrows) appear due to the twin planes. There the information about image amplitude is missing. (e) Moiré pattern, obtained after Fourier filtering of the  $(-1,-1,1)$  Bragg peak. The Moiré pattern is violated at the position of twin planes. The nanowire border is marked with the yellow dashed line. (f) Perfect  $60^\circ$ -mixed dislocation in zinc blende stacking sequence viewed along the  $[0\ 1\ \bar{1}]$  direction.

(their type), found in thick nanowires, we analyzed HRSTEM images taken along the  $[0\ 1\ \bar{1}]$  viewing direction (see Figure A.1).

Figure A.1 e) shows the Moiré pattern obtained by Fourier filtering of the  $(-1,-1,1)$  Bragg peak. We observe  $(-1-11)$  planes inclined with respect to the nanowire axis. It is difficult to identify the expected  $60^\circ$ -mixed dislocations (unfinished  $(-1-11)$  planes, see Figure A.1 f) among the noise introduced by twin planes (marked by the arrows). The similar "noise violation" effect is found in all studied images.



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