Theoretical Study of In-plane Heterojunctions of Transition-metal Dichalcogenides and their Applications for Low-power Transistors

Jean Choukroun

NNT : 2018SACLS557

Thèse de doctorat

Theoretical Study of In-plane Heterojunctions of transition-metal Dichalcogenides and their Applications for Low-power Transistors

Thèse de doctorat de l'Université Paris-Saclay
préparée à Université Paris-Sud

École doctorale n°575 : Electrical, Optical, Bio : Physics and Engineering (EOBE)
Spécialité : Electronique et optoélectronique, nano et microtechnologies

Thèse présentée et soutenue à Orsay, le **14 décembre 2018** par

Jean CHOUKROUN

Composition du Jury :

M. Yann-Michel NIQUET Ingénieur-chercheur, CEA, INAC, Grenoble	Rapporteur
M. Raphaël CLERC Professeur, CNRS, Laboratoire Hubert Curien, St Etienne	Rapporteur
M. Philippe DOLLFUS Directeur de recherche, CNRS, C2N, Orsay	Directeur de thèse
M. Marco PALA Chargé de recherche, CNRS, C2N, Orsay	Co-encadrant
M. Frédéric ANIEL Professeur, CNRS, C2N, Orsay	Président
M. Bernard PLAÇAIS Directeur de Recherche, CNRS, ENS-LPA, Paris	Examinateur

Acknowledgements

First, I would like to express my sincere gratitude to my supervisors, Dr. Philippe DOLLFUS and Dr. Marco PALA. Philippe took me in as an intern in March 2015 and, during that time, motivated me to pursue a PhD thesis with him. Although the first two years of this PhD work were arduous to say the least, he was always kind, patient, motivated, and there for me whenever I needed advice. Marco joined the team and my PhD project as a co-supervisor near the end of 2017 and, thanks to his expertise on TFETs and his NEGF quantum transport software, brought fresh ideas and breathed new life into my PhD work.
Although radically pivoting with less than year left was daunting and no easy task, it worked out and allowed us to produce the entirety of the work presented in this thesis. Their constant guidance and encouragement were instrumental to this work, and for that, I thank them again.

Besides my supervisors, I also would like to thank all of my colleagues from the COMICS group, both present (Dr. Jérôme Saint-Martin, Prof. Arnaud Bournel, Mr. Christophe Chassat, Dr Demetrio Logoteta and Mr Brice Davier) and past (Dr. Michele Amato, Dr. Damien Querlioz, Dr. MaiChung Nguyen, Dr. Viet Hung Nguyen, Ms. Jiaqi Zhou and Dr. Jerôme Larroque) for a friendly work atmosphere and for offering help whenever it was needed.

I also want to thank my family. My parents, of course, for their unending love and support, for the trust they put in me, for cheering me on and allowing me to get this far. My brothers and sister, as well as my cousins and grand-parents, for the much needed respite they offered whenever we had the chance of being together. Finally, I want to thank my girlfriend Elodie for the joy she brings me every single day, for allowing me to get out of my own head and think of something else than work even during the extremely busy and arduous year that was 2018, and for keeping me sane especially over the course of the last few months and the writing of this manuscript.

Bures-sur-Yvette, December 14th 2018

Jean Choukroun

Abstract

The invention of the transistor in 1947 is arguably one of the most important advances in technology in the history of mankind. From single transistors came integrated circuits, and finally microprocessors in 1971 based on the traditional MOSFET architecture.
The number of transistors per microprocessor increased following Moore's law, nowadays reaching the tens of billions. However, this scaling of traditional, silicon-based MOSFET seems to be reaching its conclusion: with billions of transistors crammed into a single chip, the dissipated heat actually impedes device performance and a scaling of the power supply is therefore badly needed to remedy this issue. However, due to the working mechanism at the very core of MOSFETs, which prevents further decrease of the supply voltage of these transistors without affecting performance, this power supply scaling won't come.
New architectures such as the TFET could bring a solution to this issue: thanks to their reliance on band-to-band tunneling, TFETs can perform at very low supply voltages and are amongst the most promising avenues for transistor technology beyond the age of the silicon-based MOSFET.
New materials could also take part in this transistor revolution: since the experimental isolation of graphene in 2004 by Geim and Novoselov, research interest in 2D materials has soared, motivated by the incredible electronic and mechanical properties of the single-layer carbon material. Dozens of 2D materials were since discovered and fabricated, and among them, transition metal dichalcogenide monolayers (TMDs) are some of the most commonly studied to this day. Thanks to their semiconducting nature and direct band gaps ranging from 1 to 2 eV, they hold potential in electronics and photonics.
Moreover, when under appropriate strains, their band alignment can result in broken-gap configurations which could be used in the case of TFETs to circumvent the traditionally low currents observed due to the tunneling mechanism they rely upon.

In this work, TMDs based in-plane heterojunctions are investigated thanks to an atomistic tight-binding approach, some of which are observed to lead to a broken-gap configuration (namely $MoTe_2/MoS_2$ and WTe_2/MoS_2). Their potential for use in tunnel field-effect transistors is subsequently evaluated via quantum transport computations based on this atomistic tight-binding model as well as the non-equilibrium Green's function theory. N-type TFETs based on these in-plane heterojunctions are shown to yield high ON currents ($I_{ON} > 10^3$ µA/µm) and extremely low subthreshold swings ($SS < 5$ mV/dec) at low supply voltages ($V_{DD} = 0.3$ V). Innovative device architectures allowed by the 2D nature of these materials are also proposed, and shown to enhance performance even further.

Résumé

A - Introduction

L'invention du transistor en 1947 est sans aucun doute l'une des plus grandes avancées technologiques de l'histoire de l'humanité. Vinrent ensuite les circuits intégrés, puis les microprocesseurs, (basés sur des transistors de type MOSFET) et pouvant contenir aujourd'hui des dizaines de milliards de transistors.
Néanmoins, la miniaturisation des MOSFETs lancée dans les années 70 semble à bout de souffle: le mécanisme de fonctionnement au cœur même des MOSFET empêche aujourd'hui la diminution de leur tension d'alimentation pourtant nécessaire pour réduire la consommation (voir Figure R 1), entraînant un échauffement pouvant fortement dégrader les performances des composants.

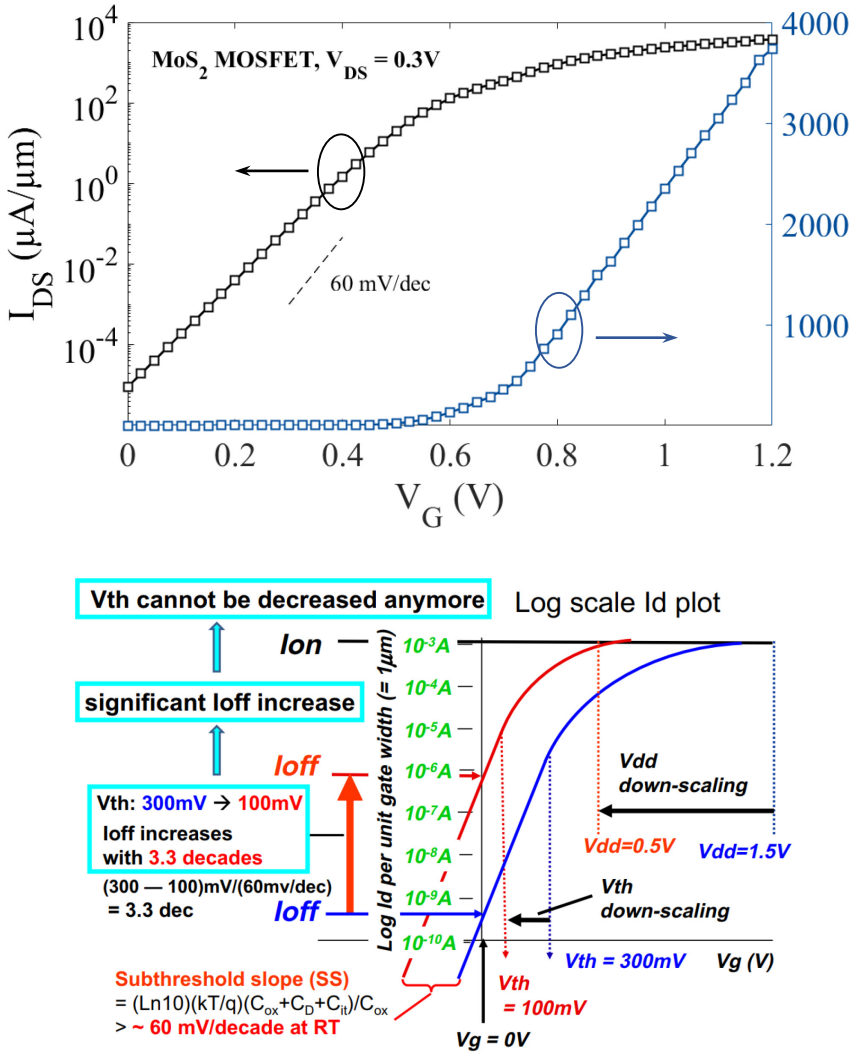


Figure R 1. (haut) Caractéristique I_D-V_G d'un MOSFET à inversion type-n à $V_{DS} = 0.3$ V et (bas) augmentation de I_{OFF} induite par une diminution de la tension d'alimentation.

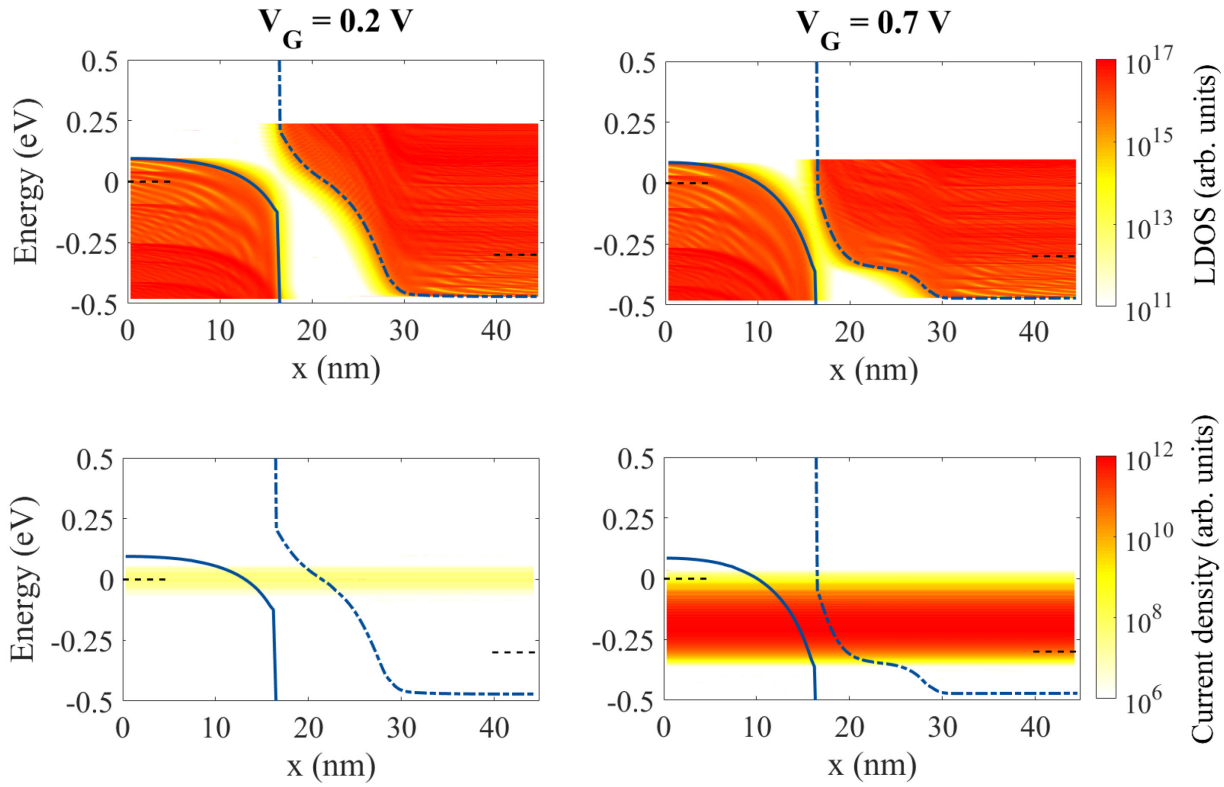


Figure R 2. (haut) LDOS dans un TFET WSe_2-MoS_2 (contraint) à l'état OFF (gauche) et ON (droite). La courbe bleue pleine (pointillée) représente la CB la plus basse (VB la plus haute), et les lignes noires pointillées le niveau de Fermi dans les contacts. (bas) Densité de courant dans le même dispositif.

De nouvelles architectures telles que le TFET pourraient donc apporter une alternative au MOSFET silicium. Grâce à son mode de fonctionnement (effet tunnel bande-à-bande, voir Figure R 2), le TFET peut présenter une pente sous-seuil bien plus raide, et donc un *SS* (augmentation de V_G nécessaire pour augmenter le courant d'un facteur 10) plus faible que le MOSFET (dont la limite théorique est de 60 mV/dec) : une très légère augmentation de V_G peut suffire pour passer de l'état OFF à l'état ON.
Ainsi, le TFET peut en principe fonctionner à des tensions d'alimentation bien plus faibles que les MOSFETs traditionnels, ce qui en fait un candidat de choix pour succéder au MOSFET silicium. Néanmoins, du fait que leur fonctionnement repose sur l'effet tunnel bande à bad, les TFETs présentent un inconvénient de taille : de faibles courants ON, limitant leurs applications possibles.
Du point de vue des matériaux, les matériaux 2D dont la notoriété est en constante augmentation depuis l'observation expérimentale du graphène en 2004, pourraient également être une alternative viable au silicium. De par leur épaisseur monoatomique, la plupart de ces matériaux présentent des propriétés novatrices, qu'elles soient électroniques ou mécaniques. Des applications variées en nanoélectronique, optoélectronique, spintronique, science des matériaux mais aussi conversion et stockage d'énergie par exemple, leur sont promises. Parmi ces matériaux 2D, les monocouches de dichalcogènures de métaux de transitions (TMDs) -des semiconducteurs à bande interdite directe d'environ 1 à 2 eV- possèdent un fort potentiel pour l'électronique et la photonique.

De plus, dans le cas de contraintes appropriées, les hétérojonctions de TMDs peuvent conduire un alignement de bandes présentant un « broken-gap ». Cette configuration ($E_{VB\text{-source}} > E_{CB\text{-drain}}$ pour un TFET type n) permettrait de surpasser les limites habituelles du TFET, à savoir de faibles courants, limités par l'effet tunnel sur lequel ces dispositifs reposent.
Dans ce travail de thèse, le potentiel de diverses hétérojonctions planaires de TMDs dans le cadre de TFETs est donc étudié en détail, au moyen d'une approche liaisons fortes couplée à des simulations de transport balistique quantique basées sur la théorie des fonctions de Green hors-équilibre.

B - Modèles et méthodes

Les TMDs étudiés sont les suivants : MoS_2, $MoSe_2$, $MoTe_2$, WS_2, WSe_2 et WTe_2. Leur agencement atomique respecte une maille hexagonale séparée en trois niveaux (chalcogène, métal, chalcogène – voir Figure R 3).
Ils sont modélisés via un modèle liaisons fortes basé sur le modèle développé par Fang et al. [1]. Ce modèle prend en compte les contributions de 11 orbitales atomiques : les 5 orbitales d du métal de transition, et les 3 orbitales p du chalcogène (3×2 puisque deux atomes de chalcogène dans la cellule unitaire des TMDs). La réponse des matériaux à une contrainte mécanique, et l'évolution de leurs propriétés en résultant, est également modélisée. Les couplages aux premiers et seconds voisins sont pris en compte, ainsi que le couplage partiel aux troisièmes voisins pour plus de précision.

Afin d'utiliser ce modèle dans le cadre de notre étude de transport électronique, un changement de base était nécessaire. Le modèle fut donc reconstruit pour s'accommoder à nos besoins : en résulte le modèle schématisé en Figure R 5.
La cellule unitaire considérée est représentée en rouge (jaune pour celle du modèle initial), et les Hamiltoniens $\mathbf{H_{n,m}}$ et $\mathbf{T_{i,j}}$ résultant des couplages considérés y sont également représentés. A partir de ces Hamiltoniens 22×22, les propriétés électroniques du TMD peuvent être calculées, comme le montre la structure de bandes présentée en Figure R 4.

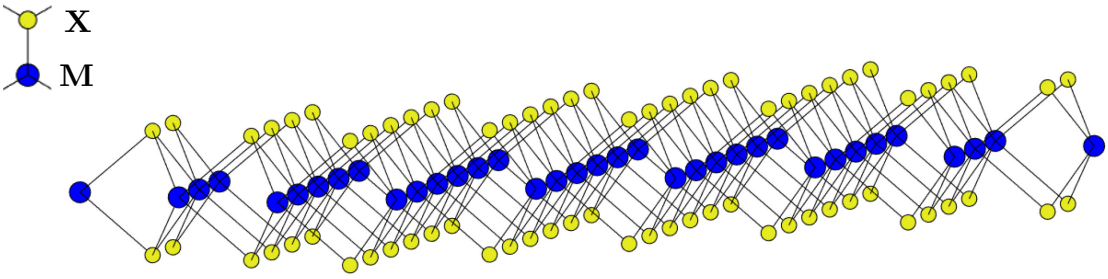


Figure R 3. Représentation « de côté » d'un TMD, mettant en avant la structure de ces matériaux, composée de trois couches distinctes.

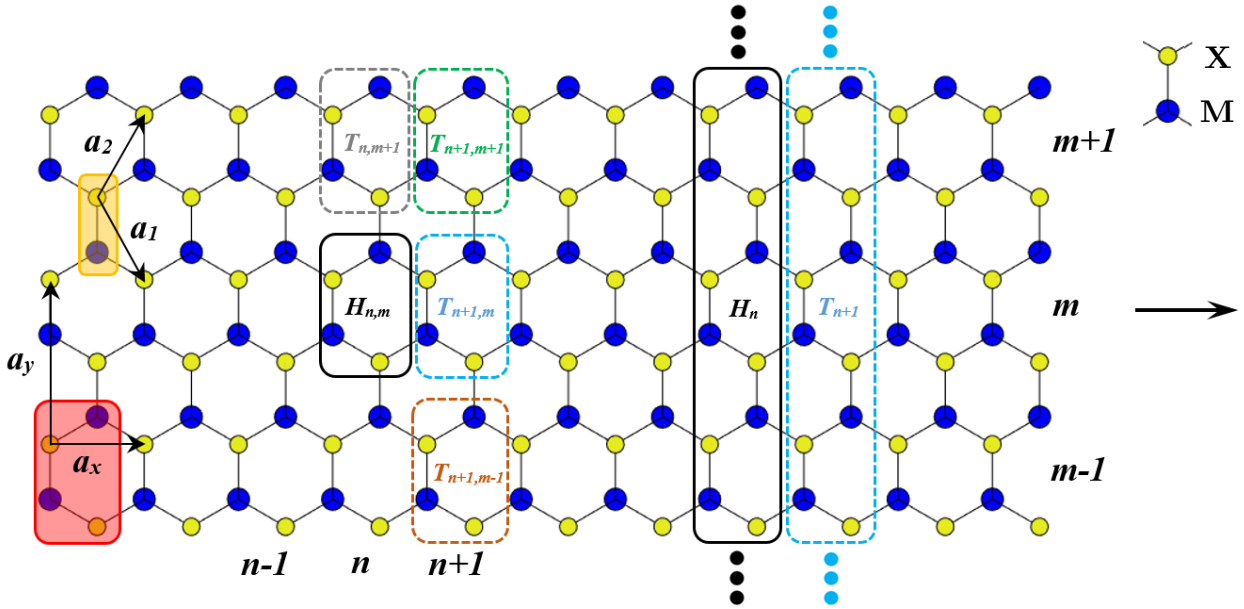


Figure R 5. Représentation de la structure des TMDs (vue de dessus) ainsi que du modèle TB utilisé. La zone rouge (jaune) représente la cellule unitaire (celle du modèle original), $H_{n,m}$ est l'Hamiltonien d'une cellule unitaire, et $T_{i,j}$ est l'Hamiltonien représentant le couplage de la maille (i,j) avec la maille (n,m). Les Hamiltoniens de couche H_n et T_{n+1} seront utilisés dans le modèle de transport basé sur les NEGF.

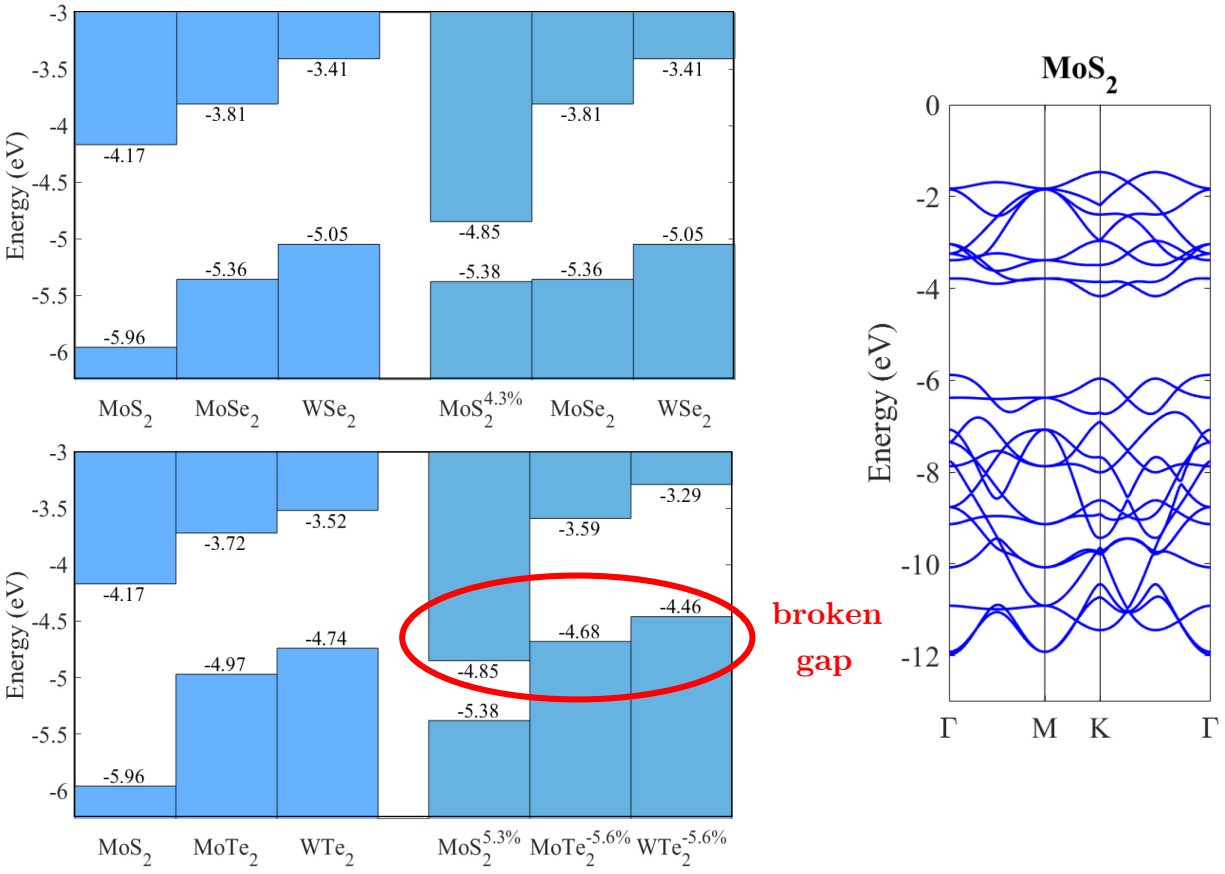


Figure R 4. (gauche) Alignement de bandes des TMDs considérés dans leur forme relaxée et contrainte (les contraintes appliquées sont celles nécessaires à l'obtention d'un accord de maille entre les TMDs considérés). L'existence d'un broken-gap dans les hétérojonctions $MoS_2/MoTe_2$ et MoS_2/WTe_2 est mise en évidence. Le niveau du vide est de 0 eV. (droite) Structure de bandes du MoS_2 obtenue via le modèle TB.

Les TMDs considérés n'ayant pas tous le même paramètre de maille, les matériaux de part et d'autre d'une hétérojonction seront soumis à des contraintes mécaniques.
Les alignements de bandes des TMDs sous leur forme relaxée et contrainte (auquel cas les contraintes appliquées sont celles nécessaires à l'obtention d'un accord de maille entre les TMDs considérés) sont présentées en Figure R 4, et mettent en exergue l'existence d'un broken-gap dans le cas des hétérojonctions $MoTe_2/MoS_2$ et WTe_2/MoS_2.

Une approche basée sur la théorie des fonctions de Green hors-équilibre est utilisée pour modéliser le transport électronique dans des dispositifs basés sur ces hétérostructures.
Cette approche consiste à séparer le dispositif en trois zones distinctes : deux contacts semi-infinis (source et drain), et une zone « device ». La fonction de Green du dispositif peut ensuite être déterminée à partir du Hamiltonien de la zone device ainsi que de son couplage avec les contacts source et drain.

$$G(E) = \left((E + i0^+)I - H_D - \Sigma_L - \Sigma_R\right)^{-1} \qquad (R1)$$

Pour ce faire, il est néanmoins nécessaire de décrire la zone device comme une succession de couches identiques suivant la direction du transport, ce qui justifie le changement de base opéré dans le cadre du modèle TB. Les matrices H_n et T_{n+1} (voir Figure R 5) sont donc créées à partir des $H_{n,m}$ et $T_{i,j}$ présentés précédemment comme suit

$$H_n(k_y) = H_{n,m} + T_{n,m+1}.e^{i.k_y.a_y} + T_{n,m-1}.e^{-i.k_y.a_y} \qquad (R2)$$

$$T_{n+1}(k_y) = T_{n+1,m} + T_{n+1,m-1}.e^{-i.k_y.a_y} + T_{n+1,m+1}.e^{i.k_y.a_y} \qquad (R3)$$

A partir de cette fonction de Green, les paramètres liés au transport dans le dispositif (telles que la charge, le courant, la densité d'états ...) peuvent ensuite être calculés. Afin d'assurer une résolution optimale, cette approche NEGF est couplée de façon auto-cohérente avec la résolution de l'équation de Poisson.

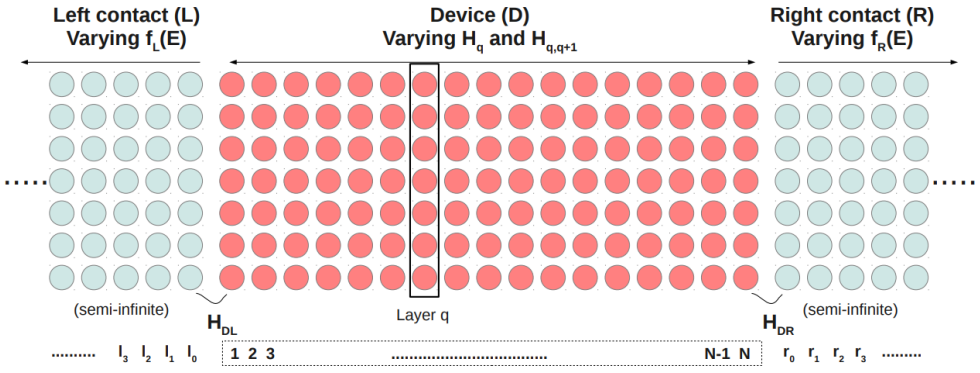


Figure R 6. Division du système en trois zones, chacune subdivisée en couches successives identiques

C - Résultats

Les dispositifs étudiés sont composés d'une couche de SiO_2 de 3.35 nm d'épaisseur sur laquelle l'hétérojonction de TMD repose. Cette hétérojonction est séparée de la top-gate par une couche d'oxide de forte permittivité (high-κ) d'EOT = 1.34 nm. Les contacts sont dopés de manière électrostatique par des « backgates » (possibilité offerte par la nature 2D des matériaux utilisés), plutôt que par un dopage chimique traditionnel et invasif. La source et le drain sont de longueurs respectives $L_S =$ 16.8 nm et $L_D =$ 10.05 nm, et la longueur du canal est variable selon les dispositifs. Une différence de potentiel V_{DS} est appliquée entre les contacts source et drain, fixant ainsi les énergies de Fermi dans les contacts à $\mu_S = 0$ et $\mu_S = -eV_{DS}$. Les performances visées par les dispositifs sont un rapport ON/OFF élevé ($> 10^7$) et un SS faible (< 30 mV/dec), assurant une transition OFF-ON ne nécessitant qu'une faible augmentation de V_G. La source est composée d'un TMD (autre que MoS_2 et WS_2), et MoS_2 est utilisé dans le canal comme dans le drain.

C.1 - TFET standard

Le potentiel des hétérojonctions de TMDs présentées en Figure R 4 dans le cadre de TFETs standard est étudiée. Leurs caractéristiques I_D-V_G sont comparées en Figure R 7, et l'importance de l'alignement de bandes résultant de l'hétérojonction est mise en exergue. Les hétérojonctions présentant une configuration broken-gap ($MoTe_2/MoS_2$ et WTe_2/MoS_2) présentent des performances bien plus élevées que les autres dispositifs ($SS < 8$ mV/dec et $I_{ON} > 10^3$ µA/µm).

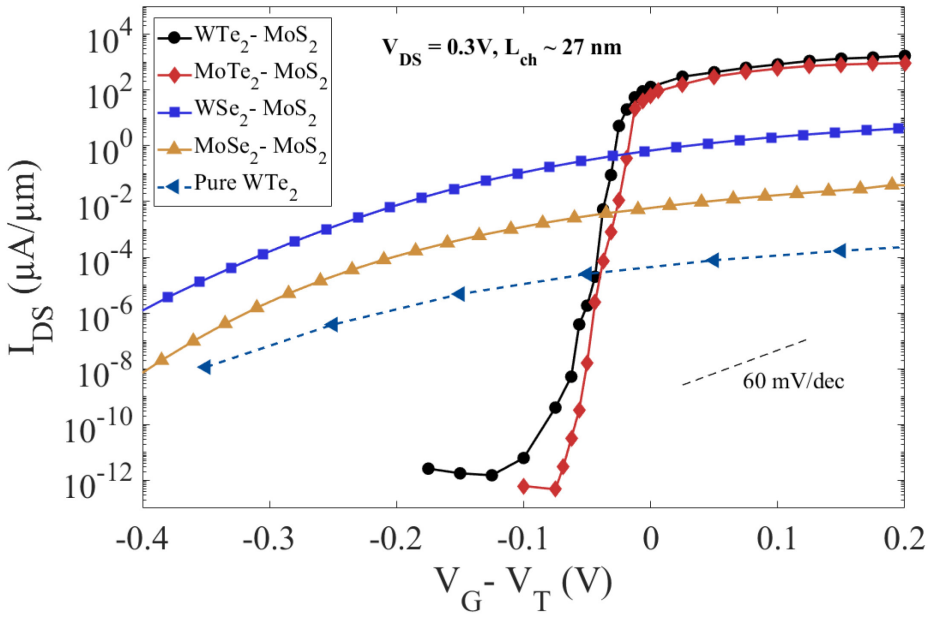


Figure R 7. Caractéristiques I_D-V_G des quatre hétérojonctions considérées, ainsi que d'un TFET homojonction WTe_2 à $V_{DS} = 0.3$ V et $L_{ch} = 27$ nm. L'influence de l'alignement de bandes résultant de l'hétérojonction sur les performances (aussi bien SS que I_{ON}) est mise en évidence.

Les dispositifs basés sur ces hétérojonctions sont donc étudiés plus en détail (influence de la longueur des contacts, du canal, des tensions appliquées aux « backgates ») afin d'optimiser leurs performances. Il en ressort notamment qu'une longueur de canal > 20 nm est nécessaire afin de minimiser *SS* et de maximiser le courant ON, comme le montre Figure R 8, mais aussi que les tensions appliquées aux backgates influencent I_{ON} ainsi que *SS*.

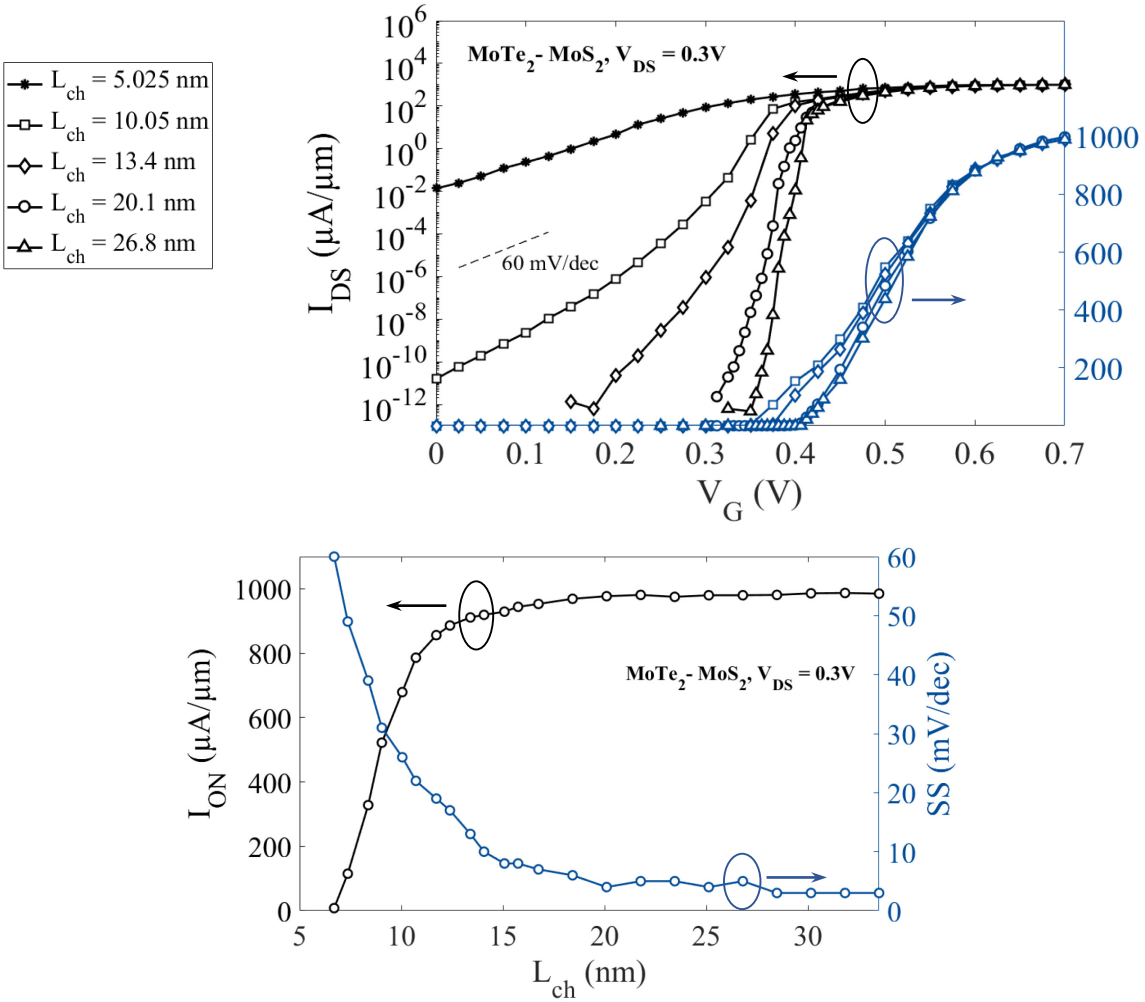


Figure R 8. (haut) I_D-V_G du TFET $MoTe_2/MoS_2$ à $V_{DS} = 0.3$ V pour L_{ch} allant de 5 nm à 27 nm. (bas) Influence directe de L_{ch} sur *SS* et I_{ON} pour le même dispositif.

C.2 - DBE-TFET

A partir de l'étude de l'influence des tensions appliquées aux « backgates » sur les performances des dispositifs présentés en C.1, l'idée d'une nouvelle architecture nous est venue : le DBE-TFET (Drain-backgate-enhanced TFET).

Dans ces dispositifs, la backgate drain est polarisée par rapport à la « top-gate » et un métal présentant une fonction de travail différente est utilisée, afin que $V_{BG\text{-}D} = V_G$ et $W_{BG\text{-}D} = W_{CG} - \Delta W$. En fixant ΔW à une valeur appropriée, les performances des dispositifs peuvent être fortement améliorées (voir Figure R 9).

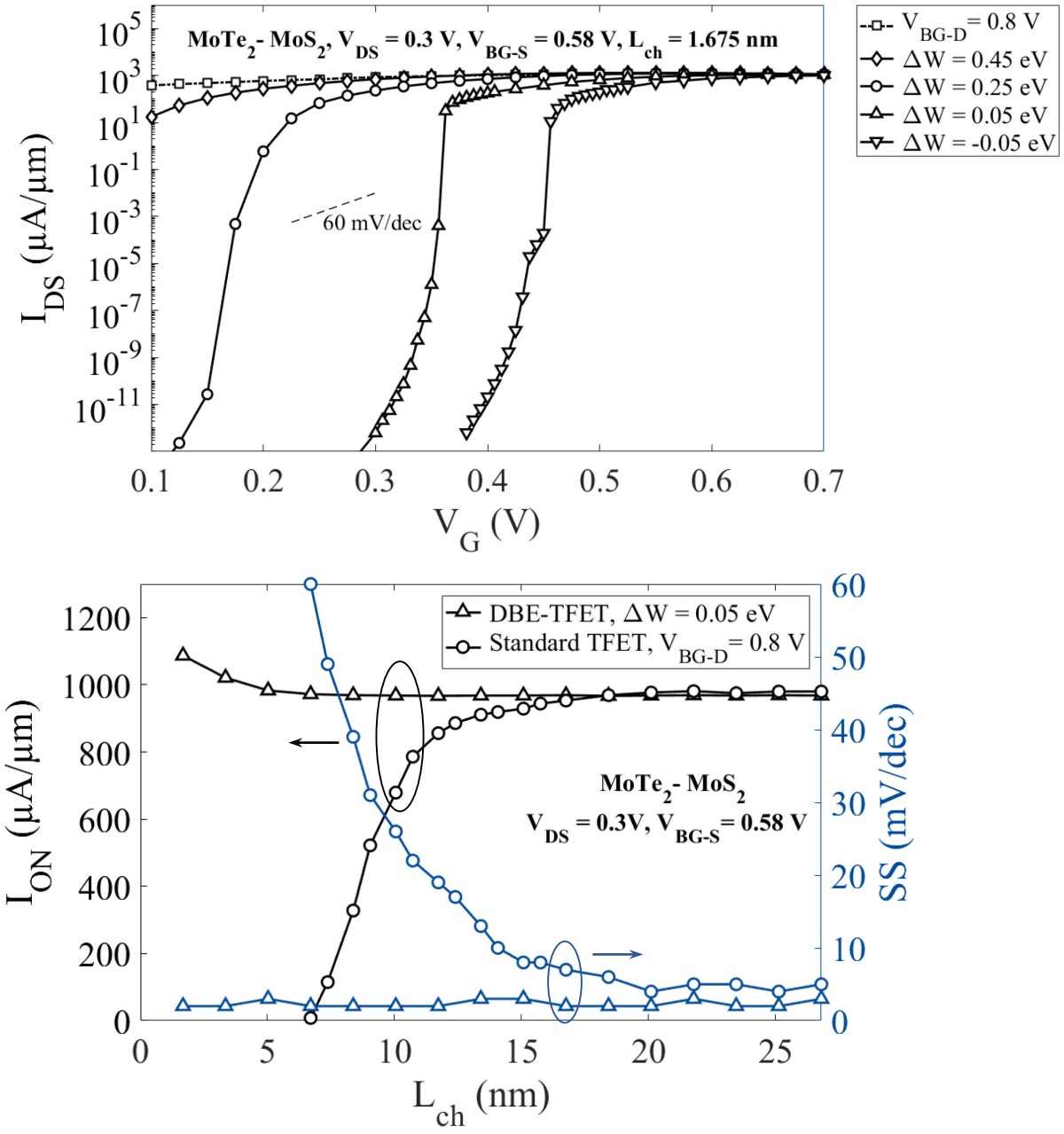


Figure R 9. (haut) I_D-V_G d'un DBE-TFET $MoTe_2/MoS_2$ à différents ΔW à $V_{DS} = 0.3$ V et $L_{ch} = 1.675$ nm. L' I_D-V_G d'un TFET $MoTe_2/MoS_2$ standard est aussi représentée pour comparaison. (bas) Influence directe de L_{ch} sur SS et I_{ON} dans un DBE-TFET $MoTe_2/MoS_2$ et un TFET standard.

Grâce à ce mécanisme, même des dispositifs comportant des canaux très courts ($L_{ch} < 2$ nm) peuvent être réalisés, chose rendue impossible par l'effet tunnel direct source-drain présent dans les TFETs standards. Les DBE-TFETs permettent d'éliminer l'influence de la longueur de canal sur les performances du dispositif, et ont donc un avantage important par rapport aux TFETs standards.

C.3 - UC-TFETs

Une autre architecture novatrice, basée sur les DBE-TFETs, est présentée et étudiée dans ce travail : le UC-TFET (ungated-channel TFET).
Puisque la CB du drain est contrôlée par $V_{BG\text{-}D}$ avec précision (comme montré dans le cas des DBE-TFETs), une « top-gate » n'est pas nécessaire pour contrôler le courant. Dans un UC-TFET, $V_{BG\text{-}D}$ est donc utilisé comme V_G le serait dans un dispositif classique.

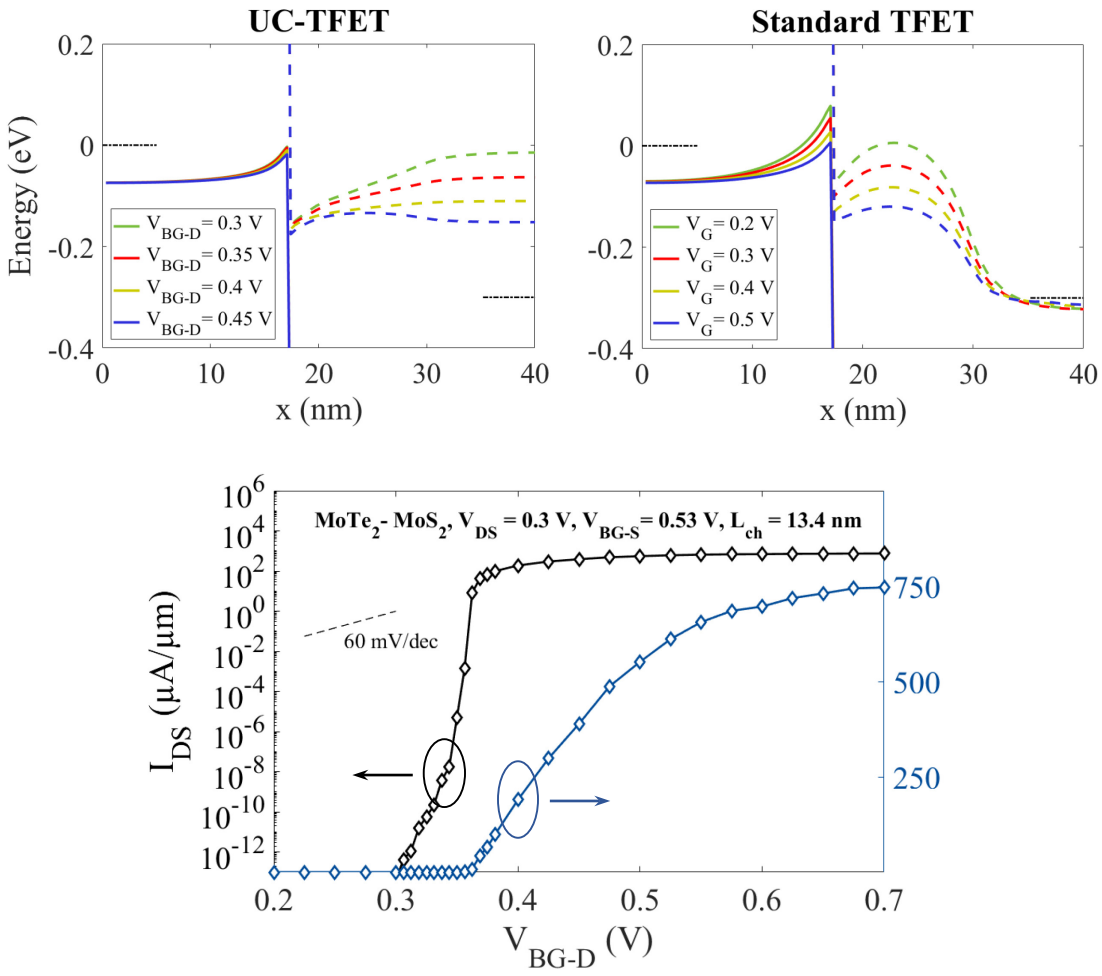


Figure R 10. (haut) Plus haute VB (lignes pleines) et plus basse CB (lignes pointillées) dans un UC-TFET et un TFET-standard lors de la transition OFF-ON.
(bas) I_D- $V_{BG\text{-}D}$ d'un UC-TFET $MoTe_2/MoS_2$ à $V_{DS} = 0.3$ V et $L_{ch} = 13.4$ nm

Comme le montre Figure R 10, le niveau de la CB dans le drain est utilisé pour contrôler le flux de porteurs dans le dispositif. Ainsi, des performances du même ordre que celles des DBE-TFET sont obtenues, tout en éliminant la top-gate (ce qui simplifierait le processus de fabrication des transistors).

D - Conclusion

Ce travail a mis en avant le fort potentiel des hétérojonctions planaires de TMDs dans le cadre de TFETs. En effet, sous certaines contraintes, ces hétérojonctions peuvent conduire à un broken-gap, configuration optimale pour le fonctionnement d'un TFET. Ainsi, les dispositifs basés sur ces hétérojonctions présentent des performances extrêmement élevées ($SS < 5$ mV/dec et ON/OFF $> 10^8$). De plus, deux architectures novatrices, le DBE-TFET et le UC-TFET ont été étudiées, et présentent des performances tout aussi impressionnantes. Elles permettent notamment de réaliser des dispositifs comportant un canal d'une longueur de moins de 5 nm, tout en préservant ces performances élevées.
Il est néanmoins important de rappeler que les interactions électron-phonon ne sont pas prises en compte dans ce travail, et que les performances sont donc observées dans le cas d'un transport parfait et balistique.

Table of contents

List of figures

List of abbreviations

AFM	Atomic force microscopy
BTBT	Band-to-band tunneling
CB	Conduction band
CMOS	Complementary metal oxide semiconductor
CVD	Chemical vapor deposition
DBE-TFET	Drain-backgate-enhanced TFET
DFT	Density functional theory
DIBL	Drain-induced barrier lowering
DITL	Drain-induced threshold lowering
DOS	Density of states
FET	Field effect transistor
ITRS	International technology roadmap for semiconductors
LDOS	Local density of states
LPE	Liquid phase exfoliation
MBE	Molecular beam epitaxy
MOSFET	Metal oxide semiconductor field effect transistor
NEGF	Non-equilibrium Green's function
TFET	Tunnel field effect transistor
TMD	Transition metal dichalcogenide
TMC	Transition metal chalcogenide
TMH	Transition metal halide
UC-TFET	Ungated-channel TFET
VB	Valence band
vdW	van der Waals
SCE	Short-channel effects
SS	Sub-threshold swing

Outline

At the onset, the goal of my PhD work was to study electronic transport in nanoelectronic devices based on 2D materials and 2D material heterostructures. Important notions on nanoelectric devices and so-called 2D materials therefore need to be introduced and boiled down before delving into the actual research work I performed during the past three years.

In Chapter 1, a comprehensive history of the MOSFET, arguably the most important device in nanoelectrics, as well as its shortcomings and the limits of its scaling will be presented. One of the most promising contenders for the future of transistors -the TFET- will be discussed in detail, and the solutions it could bring to the transistor scaling issue will be outlined.
In Chapter 2, the aforementioned 2D materials will be presented, and the electronic and structural properties of a few of them will be detailed. Potential applications for these materials, as well as the main synthesis techniques used to grow and deposit them will then be discussed.
In Chapter 3, the models and methods used during my PhD work will be presented. More specifically, the tight-binding approach used to model the materials as well as the non-equilibrium Green's function formalism used to compute electronic transport through the devices and its implementation will be detailed.
Then, in Chapters 4-7, simulation results obtained for a variety of devices based on 2D materials will be presented and discussed. Among these devices are MOSFETs and TFETs, but also new device designs based on the standard TFET architecture that yield extremely promising results. In all cases, the influence of device parameters such as the materials used, channel length and more will be investigated.

Finally, a conclusion will summarize the main takeaways of this thesis work, and highlight the promising devices and results obtained. An outlook will also describe potential avenues to pursue this work further.

Chapter 1

Introduction to nanoelectronics

Nowadays, microprocessors are everywhere: from smartphones to traditional computers, from cars to rockets, from weighing scales to stoplights -among many other things-, they truly enable the creation of anything we consider to be "technological". A case can therefore be made that the invention of the very building block of the microprocessor, the transistor, is one of the most important and impacting breakthroughs in human history.

1.1 History of transistors and nanoelectronics

In 1947 John Bardeen, William Schockley and Walter Brattain, three scientists working at Bell Telephone Laboratories, were studying the potential of germanium crystals as a replacement for the large, energy hungry, and unreliable vacuum tubes[2], [3] that were used in telecommunications to amplify voice and music. As the culmination of years of research, they finally succeeded[4]–[6] in creating the very first "point-contact" transistor, in which gold foils were deposited on a germanium crystal and successfully amplified an input signal, without the need for a lengthy heat-up time as was the case for vacuum tubes. This transistor was used in commercial products such as telephone exchanges and hearing aids as soon as 1952[2], but sensitivity to moisture and overall fragility would prevent it from being widely adopted[3], [4].

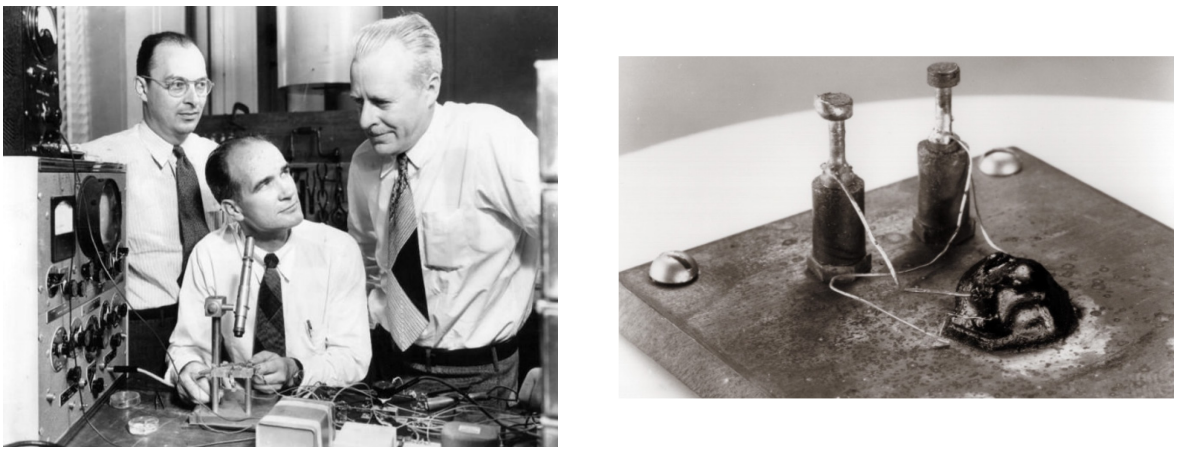


Figure 1. Left: John Bardeen, William Schockley and Walter Brattain.
Right: the first point-contact transistor

During this time however, Schockley came up with an updated design for a transistor: the "bipolar junction" transistor. It relied on a "sandwich" NPN design and therefore on germanium doping to control current flow, and was far more robust than its point-contact counterpart[2]. This "sandwich" design was used in 1958 in the IBM 7070, the first computer based on transistors rather than vacuum tubes[4]. For their work and the invention of the transistor, Bardeen, Schockley and Brattain were awarded the Nobel Prize in 1956.

Around this time, an important shift happened in the transistor industry: instead of relying on germanium, transistor research and manufacture switched to silicon[2], [7]. Although germanium had several advantages[5], such as being less reactive than silicon, having a lower melting point which is helpful for manufacturing, as well as having superior carrier mobility, its drawbacks were too great. Its low band gap (0.67 eV compared to 1.12 eV for silicon) lead to high leakage currents, and the transistors simply did not work beyond 75°C. Another strong advantage of silicon that would be implemented later on is that its oxide (SiO_2) can be easily grown to form an insulating layer with a high quality Si/SiO_2 interface.
The first silicon transistor was reported by Texas Instruments, although Bell Telephone Laboratories had been working on similar technology for several years[5]. Silicon based electronics were thus born, and remain the dominating market force to this day. For several years, transistors were manufactured as individual components, before being assembled with other parts of the end circuit, such as resistors, capacitors diodes[2] ... However, this technique led to sprawling circuits that were challenging to assemble and increasingly unreliable[2], [5]. In 1958 Jack Kilby, an engineer at Texas Instruments, came up with a solution for this issue: create several transistors and other devices such as resistors from a single piece of semiconductor, therefore drastically reducing the size of the overall resulting circuit. The integrated circuit was born[2], [4], and Kilby was subsequently awarded the Nobel Prize in 2000 for this work.
The advent of the integrated circuit based on silicon transistors truly was the beginning of the computer revolution and, more broadly, of an electronics revolution. Since the late 1950s, radios, TVs and other consumer electronics devices based on transistors were commercialized, which only accelerated the growing interest in this technology.
In 1960, John Atalla and Dawon Khang, researchers at Bell Telephone Laboratories, fabricated the first Field Effect Transistor[8] (FET), in which current flow is controlled by the electric field created by the gate. More precisely, these devices are referred to as Metal Oxide Semiconductor FETs (MOSFET), due to the materials used (metal for the gate, oxide for the insulating layer and semiconductor for the channel). Schockley and others had long anticipated[9] and worked on this transistor architecture, but never managed to fabricate it due to surface states preventing the electric fields from penetrating the semiconductor. This MOSFET architecture is the most commonly used in transistors to this day, and will be described in more detail in the next section.

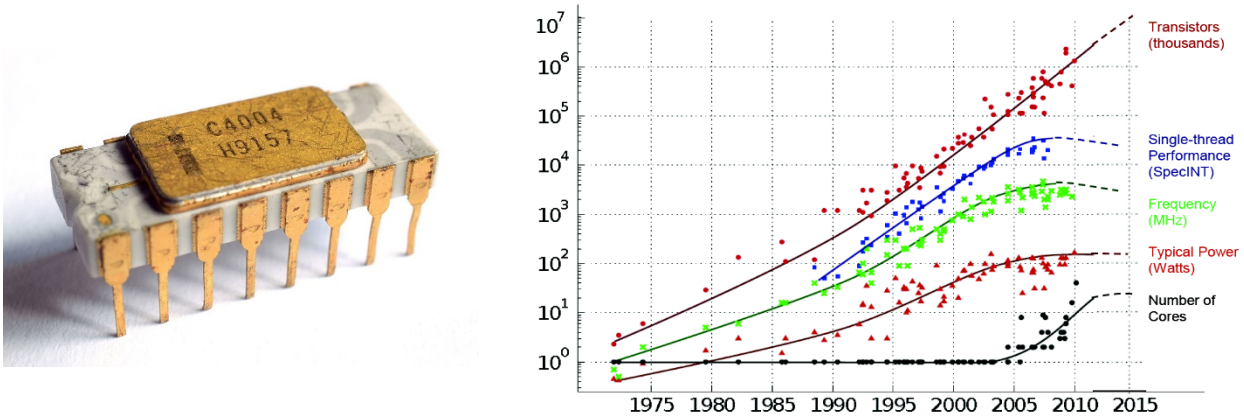


Figure 2. Left: Intel's 4004 microprocessor, composed of 2300 transistors. Right: evolution of performance indexes of microprocessors from 1971 to 2012 [10]

In 1965, Gordon Moore, then Director of R&D at Fairchild Semiconductors, published an article[11] predicting the amount of transistors in an integrated circuit would double every two years for the foreseeable future; this statement is now famously known as Moore's Law (although it has recently been slightly adapted) and ruled the industry ever since. Shortly thereafter, in 1968, Moore left Fairchild Semiconductors to form Intel Corporation, which would go on to invent the microprocessor in 1971 with its 4004 chip[12]. It was composed of 2300 transistors, had a clock speed of 108 kHz, and was as powerful as the 30-ton ENIAC computer from 1946 that filled an entire room. From there, Intel introduced new processors every couple of years which include[13] the 8086 chip in 1978 with 29 000 transistors, the 486 chip in 1989 with 1 200 000 transistors (the first generation with over 1 million transistors), or the Itanium 2 series 9000 in 2006 with 1.7 billion transistors. Since then, Intel has become the world's leading microprocessor manufacturer; however, AMD's Epyc microprocessor boasts the highest transistor count to date, with over 19.2 billion transistors[14].

So, in roughly 70 years, we have gone from large, single transistors, to packing over 19 billion transistors in areas below 800 mm^2. As far as microprocessors go, since 1971 and Intel's 4004 chip, clock speed has increased from 108 kHz in single core architecture to over 3 GHz in 32 core architectures, and the process size was reduced from 10 µm to less than 15 nm.

The next section will focus on the device architecture that made it all possible, and that is at the core of every microprocessor used today: the MOSFET.

1.2 Metal Oxide Semiconductor Field-Effect Transistor (MOSFET)

As mentioned in the previous section, MOSFETs are the prevailing type of transistors used in electronics, and they have been for roughly 60 years since their initial fabrication by Bell Telephone Laboratories in 1960[8]. As its name suggests, a MOSFET is mainly composed of a metal gate, separated from a semiconductor body by a thin, insulating oxide layer, and as is the case for all FETs, the electric field created by the gate controls current flow in the device.

1.2.1 Working principle of a MOSFET

The working principle of an inversion mode, n-type MOSFET is shown in Figure 3 a). A semiconductor (usually silicon) makes up the body of the device, and is doped in a specific way: the source and drain region, where the electrical contacts are located, are n-doped (which means they carry excess electrons), whereas the rest of the device -and therefore the channel region, located in between the source and drain- is p-doped (which means it is lacking electrons, or has excess holes).
A constant, positive voltage V_{DS} is applied between the source and the drain, while a varying voltage V_G is applied to the gate.
In the OFF state (when no or very low voltage is applied to the gate) no current flows from source to drain due to the p character of the channel.
In the ON state however (when a high enough voltage is applied to the gate) the electric field it generates in the semiconductor, through the oxide, creates an n-type inversion channel through which electrons can flow freely from the source to the drain.

Depletion mode n-type MOSFETs have a similar working principle, with a key difference: the channel is n-doped, like the contacts. Therefore, current flows freely from the source to the drain when no gate voltage is applied, and a negative gate voltage is necessary to stop current flow through the channel.

In p-type MOSFETs, V_{DS} is negative and all doping is reversed: the contacts are p-type, the body n-type, and a negative (positive) voltage has to be applied to the gate to allow current flow in inversion (depletion) mode. In this case, the current carriers are not electrons, but holes.
When an n-type MOSFET and a p-type MOSFET operate in a complementary way, a CMOS (Complementary MOS) device is created; CMOS can be used to create inverters or NAND (Not AND) and NOR (which are the basic functions of logic operations in a circuit) and is therefore extremely useful.

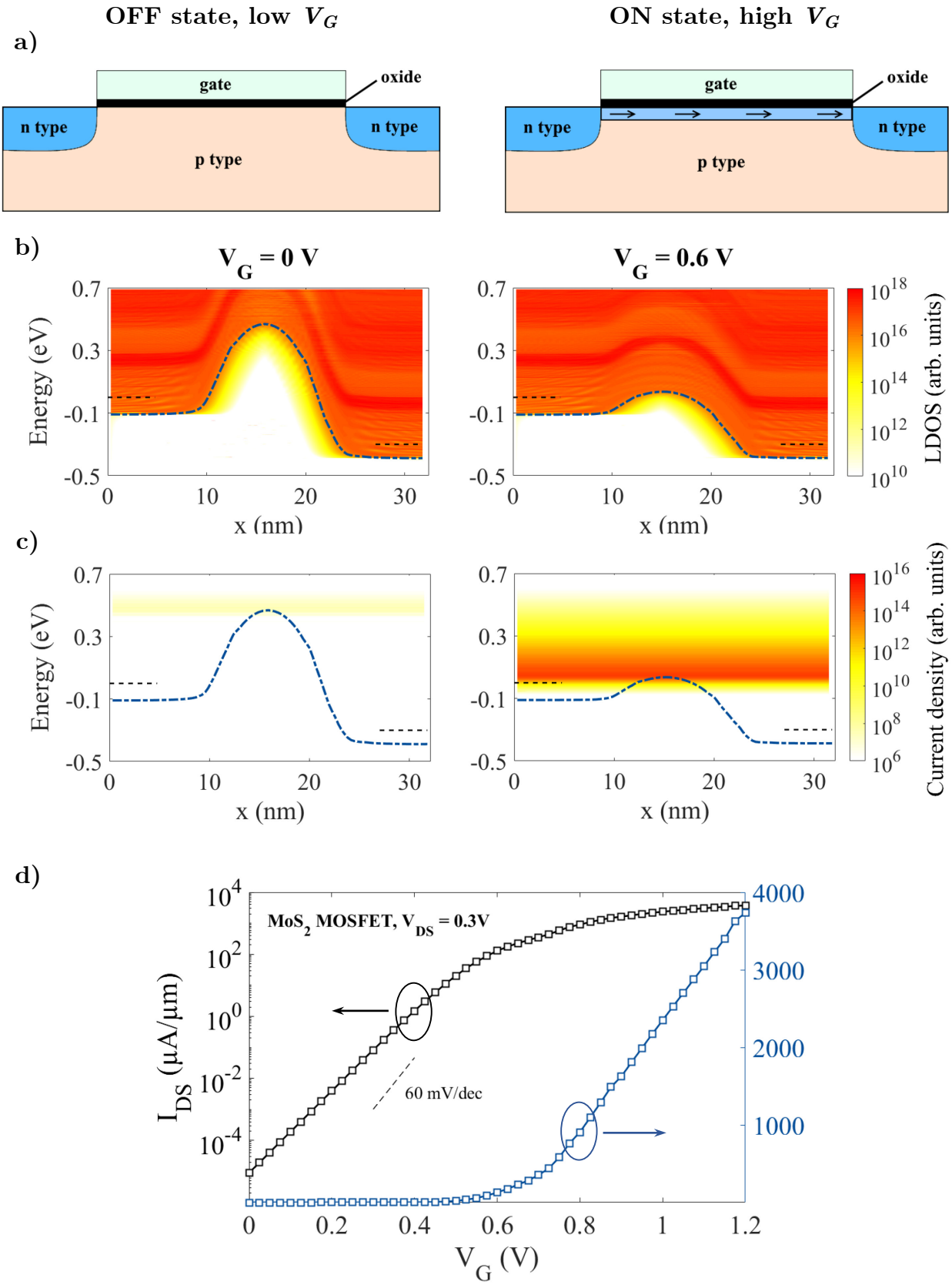


Figure 3. a) Sketch of an n-type, inversion mode MOSFET in the OFF (left) and ON state (right). b) Local density of states in a MoS_2 MOSFET in the OFF (left) and ON state (right). The dotted blue line represents the lowest conduction band, and the dotted black lines the Fermi levels in the source and drain. c) Current density in the same device. d) Current characteristics of the device at $V_{DS} = 0.3$ V.

Because electrons are Fermions, their distribution along the available energy states is controlled by the Fermi-Dirac distribution given in Eq.(1)

$$n(E) = \frac{1}{e^{E-\mu/k_B T} + 1} \tag{1}$$

where *n(E)* is the probability that the level at energy E is occupied, μ is the Fermi level in the device, k_B is the Boltzmann constant (k_B = 1,3806 × 10^{-23} J.K^{-1}) and T is the temperature in Kelvin.
As is shown in Figure 4, temperature has a high impact on the energy states that might be populated. At $T = 0$ K, all states below the Fermi level are occupied, and all states above it are empty; as the temperature increases however, electrons gain thermal energy ($k_B T$) and might leave states below μ to populate states above it. At $T = 500$ K for instance, electrons might populate states up to 0.25 eV above the Fermi level. However, no matter the temperature, the occupation probability at $E = \mu$ is always 0.5.

In MOSFETs, as is the case in all other transistors, the Fermi level in the contacts in eV is dictated by the drain voltage.

$$\mu_S = 0 \qquad \mu_D = -eV_{DS} \tag{2}$$

The level of the conduction band in the source and drain, while influenced by V_{DS}, also depends on the level of doping in the contacts. The height of the energy barrier imposed by the gate when $V_G = 0$ V depends on the Fermi energy of the metal and the affinity (the bottom of the lowest conduction band compared to the vacuum level) of the material used. Therefore, only by carefully selecting the doping applied to the semiconductor, the material to use as a gate, and the drain current can a functioning MOSFET be achieved.

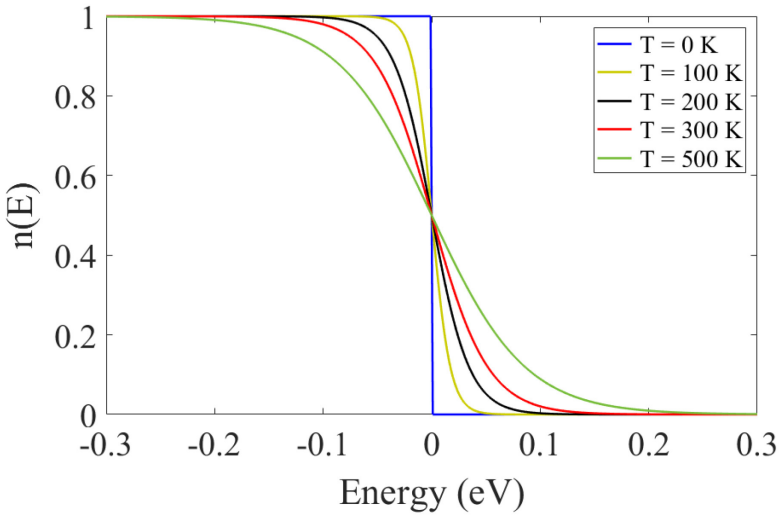


Figure 4. Fermi-Dirac distribution for $\mu = 0$ eV at temperatures ranging from 0 to 500 K.

To characterize the performance of a transistor, several metrics are often used. The current ratio (ON/OFF) is the most prevalent. I_{OFF} is calculated either at $V_G = V_{OFF} = 0$ V, or given a fixed value (10^{-5} µA/µm for instance), in which case $V_{OFF} = V_G(I_{OFF})$.
The ON current, I_{ON}, is then calculated at $V_{ON} = V_{OFF} + V_{DD}$ with $V_{DS} = V_{DD}$. The goal is to maximize I_{ON} while minimizing I_{OFF}, and therefore to yield a high I_{ON}/I_{OFF} ratio. The sub-threshold swing (SS) is another important figure of merit. It describes the steepness of the current slope in the sub-threshold regime in log scale (from $V_G = 0$ V to 0.4 V in Figure 3 d) for instance) and is calculated[15] as

$$SS = \left(\frac{\partial \log(I_{DS})}{\partial V_G}\right)^{-1} \tag{3}$$

between two fixed I_{DS} values (such as 10^{-5} and 10^{-2} µA/µm). SS is given in mV/dec, because it describes the increase in gate voltage necessary to increase the current ten-fold. Due to the aforementioned Fermi-Dirac distribution electrons are bound to, the thermionic effect occurring in MOSFETs entails a hard lower limit of 60 mV/dec at 300 K, as is detailed in Eq.(4)

$$SS_{MOSFET-min} = \ln(10) \times \frac{k_B T}{e} = 60\ mV/dec \tag{4}$$

Switching frequency, drain-induced barrier lowering (DIBL) and other electric characteristics have to be taken into account when designing MOSFETs, as some applications will result in strict guidelines to be followed[16]–[21].

1.2.2 Moore's Law and initial MOSFET scaling

As mentioned earlier, Moore's Law (stated in 1965 but slightly revised since) predicted that the amount of transistors in an integrated circuit would double roughly every two years. In order to abide by this prediction, all of the dimensions of a MOSFET had to be scaled down aggressively along the years. For instance, oxide thickness was reduced[22] from over 250 nm to roughly 15 nm between 1975 and 1990, and gate length was reduced from over 20 µm to 1 µm in the same timeframe, all the while making MOSFETs faster and less power-consuming. However, with such aggressive scaling, issues related to gate length and oxide thickness such as source to drain tunneling and leakage currents arose and were in part solved via the evolution of the structure of MOSFETs: first, Silicon On Insulator (SOI) MOSFETs were introduced[23], [24]. Silicon dioxide (SiO_2, same as the gate oxide) is buried in between the silicon substrate and the Si channel, and only a very thin channel of silicon is deposited above it, between the contacts.

This new structure (shown in Figure 5 a)) allowed for far lower leakage currents (and therefore lower I_{OFF}), higher performance than regular MOSFETs at similar supply voltages[25], and for the elimination of latch-up (a specific type of short-circuit). However, the thick, buried silicon dioxide layer hampers the evacuation of the heat created by transistor operation. Nonetheless, SOI technology allowed MOSFET scaling to continue, and oxide thicknesses and channel length to be reduced even further.
In the late 1990s[26], double-gate MOSFETs (and beyond) were introduced[27], [28], as a way to enhance the electrostatic control in the channel and remedy most short-channel effects (SCE), such as carrier velocity saturation, high DIBL and others[29], [30] ... Thanks to this new structure, carriers in the whole channel could be controlled by the gates, mainly allowing for I_{OFF} reductions as well as overcoming most SCE. The FinFET[27], [28], [31], a device in which the channel is composed of a thin silicon "fin" and surrounded by several gates (shown in Figure 5 b) and c)) is the most common type of multiple-gate MOSFET. It is still currently used in the 10 nm processes of chip manufacturers such as Intel or Samsung, as it allows for shorter channels and lower SS than regular MOSFETs. In this case, specific parameters to this design such as the fin height, fin width and fin pitch in the case of multi-finger FinFETs (see Figure 5 c)), impact FinFET performance.

Another technological breakthrough that allowed the continued scaling of MOSFETs was the advent of the high-κ dielectric[32]. Until then, only SiO_2 had been used as a gate oxide, due to its inherent compatibility with silicon. However, as gate oxide thickness decreased, gate tunneling leakage currents increased and hampered device performance.

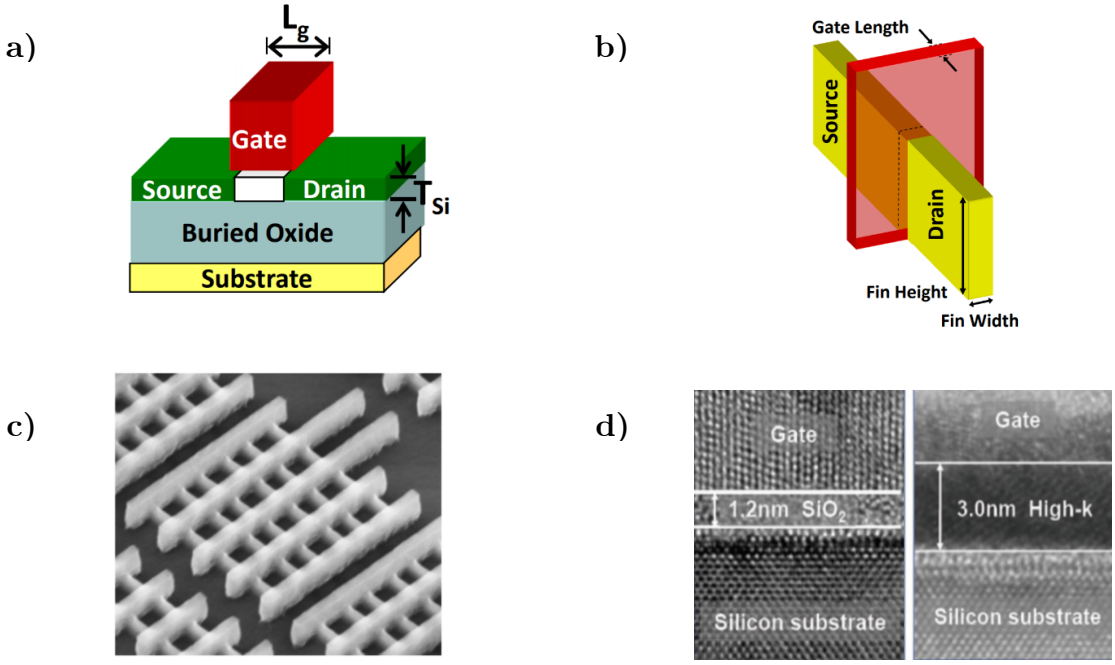


Figure 5. a) Sketch of a SOI MOSFET. b) Sketch of a FinFET. c) SEM image of a multiple-finger FinFET d) Comparison between SiO_2 and a high- dielectric as a gate oxide [31], [33].

So called "high-κ materials" have a higher dielectric constant than SiO_2 ($\kappa_{SiO_2} = 3.9$[34], [35]) and can therefore provide more capacitance for the same thickness. Thicker high-κ dielectric layers can therefore be used to prevent gate leakage, while increasing gate control over the channel; the thickness of most oxide layers is therefore now referred to as their Equivalent Oxide Thickness (EOT), calculated as

$$EOT = t_{high-\kappa} \times \frac{\kappa_{SiO_2}}{\kappa_{high-\kappa}} \tag{5}$$

Hafnium oxide, for instance, is one of the most commonly used high-κ dielectrics and has a $\kappa = 20$ [33] ; a 5 nm HfO_2 layer is therefore as efficient as a 1 nm SiO_2 layer in terms of gate capacitance, but reduces gate leakage currents up to a factor of 10^4 thanks to a thicker insulating stack.
Several other techniques and designs (such as the use of strained silicon[36], [36]–[38], or a silicon-germanium alloy[39], [40] in the channel for instance) were theorized and put into use over the years, but are not detailed here for concision purposes.

Through the years and the technological nodes, from 1971 and 20 µm processes to 2018 and 7 nm processes, these various adjustments and modifications to MOSFET design allowed the industry to more or less abide by Moore's Law.
However, as we look into the future of nanoelectronics, several fundamental issues and challenges related to the MOSFET's mode of operation and the properties of silicon cast doubt on the possibility for this aggressive scaling trend to continue unabated. That is, unless a truly industry-changing paradigm shift occurs.

1.3 The power scaling challenge

The techniques mentioned in the previous section allowed for a mitigation of the negative effects that come with MOSFET scaling (SCE such as DIBL, gate leakage ...), but these effects remain an issue and a strong hindrance to further scaling[41]–[43].
The main limiting factor currently faced by the transistor industry is power scaling: thanks to the downsizing of MOSFETs, more transistors can be crammed into a smaller area with each generation, which allows for higher performing microprocessors for instance. However, in doing so, the power dissipated by unit area vastly increases and can prevent the transistors from operating properly. A scaling in dissipated power per transistor is therefore badly needed, but has eluded the industry for over a decade[44], [45].
In a MOSFET, the power consumption is evaluated as shown in Eq.(6), and can be broken down in two parts: dynamic power consumption (when the device is ON) and static power consumption (when the device is OFF).

$$P = \underbrace{C_L \cdot f_c \cdot V_{DD}{}^2}_{\textbf{Dynamic}} + \underbrace{I_{OFF} \cdot V_{DD}}_{\textbf{Static}} \tag{6}$$

Where V_{DD} is the supply voltage, C_L is the load capacitance and f_C the operating clock frequency of the device. It is plain to see that both dynamic and static power consumption are highly dependent on the supply voltage, and V_{DD} scaling is therefore the most effective way to decrease the power consumed by a CMOS circuit. However, V_{DD} scaling is easier said than done, because both the supply voltage and the threshold voltage (V_T) are intrinsically tied to each other and to the performance of the transistor.

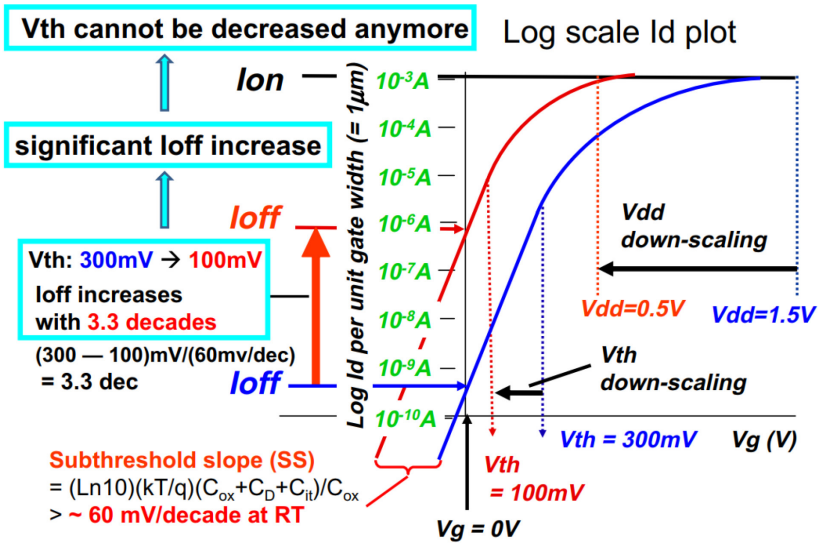


Figure 6. Increase in I_{OFF} due to a reduction of V_{DD} and V_T[43].

In order to decrease V_{DD} and maintain I_{ON}, V_T has to be reduced. However, by decreasing V_T, the OFF current (current at $V_G = 0$ V) is strongly increased, as shown in Figure 6. Because this is due to the high SS (> 60 mV/dec) of MOSFETs, it cannot be circumvented and has kept V_{DD} scaling from keeping up with other aspects of MOSFET scaling such as channel length, oxide thickness... What's more, this inability to scale the supply voltage at the same rate as the other characteristics of the device actively hampers performance[42], [44]: the strong electric fields generated by the high supply voltage cannot be dealt with properly by the shorter channels for instance, which increases DIBL and can cause barrier breakdown.

In an effort to limit power consumption, V_{DD} has nonetheless been scaled down as much as possible, down to approximately 1 V since the mid-2000s[46]. As a result, static power consumption has accounted for over 50%[47] of the dissipated power since the 45 nm node; the bulk of the power consumed by today's transistors therefore occurs when they are turned off.

This trend obviously cannot continue, and new approaches are therefore required to pursue transistor scaling further.
Two main types of approaches are possible:

- MOSFET based on new materials: most transistors manufactured and used today are based on silicon. The use of higher mobility materials in the channel could increase device performance and allow for the use of lower supply voltages without degrading I_{ON}. Silicon-germanium alloys[39], [40], as well as III-V semiconductors[48]–[51] (such as InAs, InGaAs, GaAs...) and their heterostructures hold some potential in this regard. Another possibility is the use of 2D materials[41], [52], [53] (only one atom thick) such as graphene for instance, to take advantage of their properties and the vastly different physics their 2D structure allows. These materials and their possible applications will be detailed in Chapter 2.

- New device architectures: other kinds of FETs hold potential for power supply scaling beyond the limits of regular MOSFETs. The inability to scale V_{DD} any lower in MOSFETs originates from their gradual current increase in the sub-threshold regime; therefore, devices presenting a much steeper turn-on transition (and therefore a far lower SS) hold potential for ultra-low power operation. While some architectures such as the piezoelectrical FET[54], [55] the electro-mechanical FET[55], [56] and the negative capacitance MOSFET based on ferroelectric gate stacks[57]–[59] have shown promise for specific applications, the Tunnel FET (TFET) has by far been the most investigated and developed concept in the last fifteen years[46], [55], [60], [61] thanks to its versatility compared to other steep-slope devices.

In the next section, the core concepts and working principle of TFETs will be discussed, as well as the advantages (and shortcomings) of this transistor design compared to traditional MOSFETs.
A quick review of the state-of-the-art in TFET technology will also be presented.

1.4 Tunnel Field Effect Transistor (TFET)

While MOSFETs are the prevailing types of transistor, Si-based MOSFET scaling is slowing down and seems to be reaching its limits, due to increasingly high dissipated power per unit area and the inability to provide satisfactory performance at low supply voltages. TFETs are one of the most promising avenues for ultra-low power operation identified by the international technology roadmap for semiconductors (ITRS)[16].

1.4.1 Working principle of a TFET

From a structural standpoint, TFETs are no different from MOSFETs. A TFET is made up of source and drain contacts separated by a channel area, over which are deposited a thin insulating layer and a gate that will control current flow. The source and drain are doped differently, unlike in the case of MOSFETs.
From an operating principle standpoint however, TFETs are vastly different from MOSFETs. They don't rely on an energy barrier to overcome, but, as their name suggests, on band-to-band-tunneling (BTBT), which frees them from the 60 mV/dec SS lower limit that constrains MOSFET technology.

The sketch of an n-type TFET and its operating principle are shown in Figure 7 (a). In an n-type TFET, the source is p-doped and the drain n-doped, while the channel is not doped (pristine material).
Just like in a MOSFET, a constant, positive supply voltage V_{DS} is applied to the source and drain and sets the Fermi energies μ_{S} and μ_{D}, while a varying gate voltage V_G controls current flow in the device.
In the OFF state (as shown in Figure 7 (b) and (c)) -when no or low V_G is applied-, carriers in the source valence band (VB) are contained to the source because no energy states are available to them in the channel, and because the distance to tunnel straight from the source VB to drain conduction band (CB) is too high.
In the ON state (as shown in Figure 7 (b) and (c)), the electric field generated by the high V_G brings the channel CB down into the same energy range as the source VB. Carriers are therefore able to tunnel from the source VB to the channel CB, and current can flow between the source and the drain.
In a p-type TFET, the doping is reversed: the source is n-doped while the drain is p-doped. A constant, negative V_{DS} is therefore applied to the contacts, and a highly negative gate voltage V_G is necessary to bring VB states in the channel up into the energy range of the source CB states. In this case, carriers tunnel from the source CB to the channel VB. Only lateral TFETs are discussed in this work, but vertical TFETs (in which the channel is composed of overlapping layers) are also being heavily investigated.

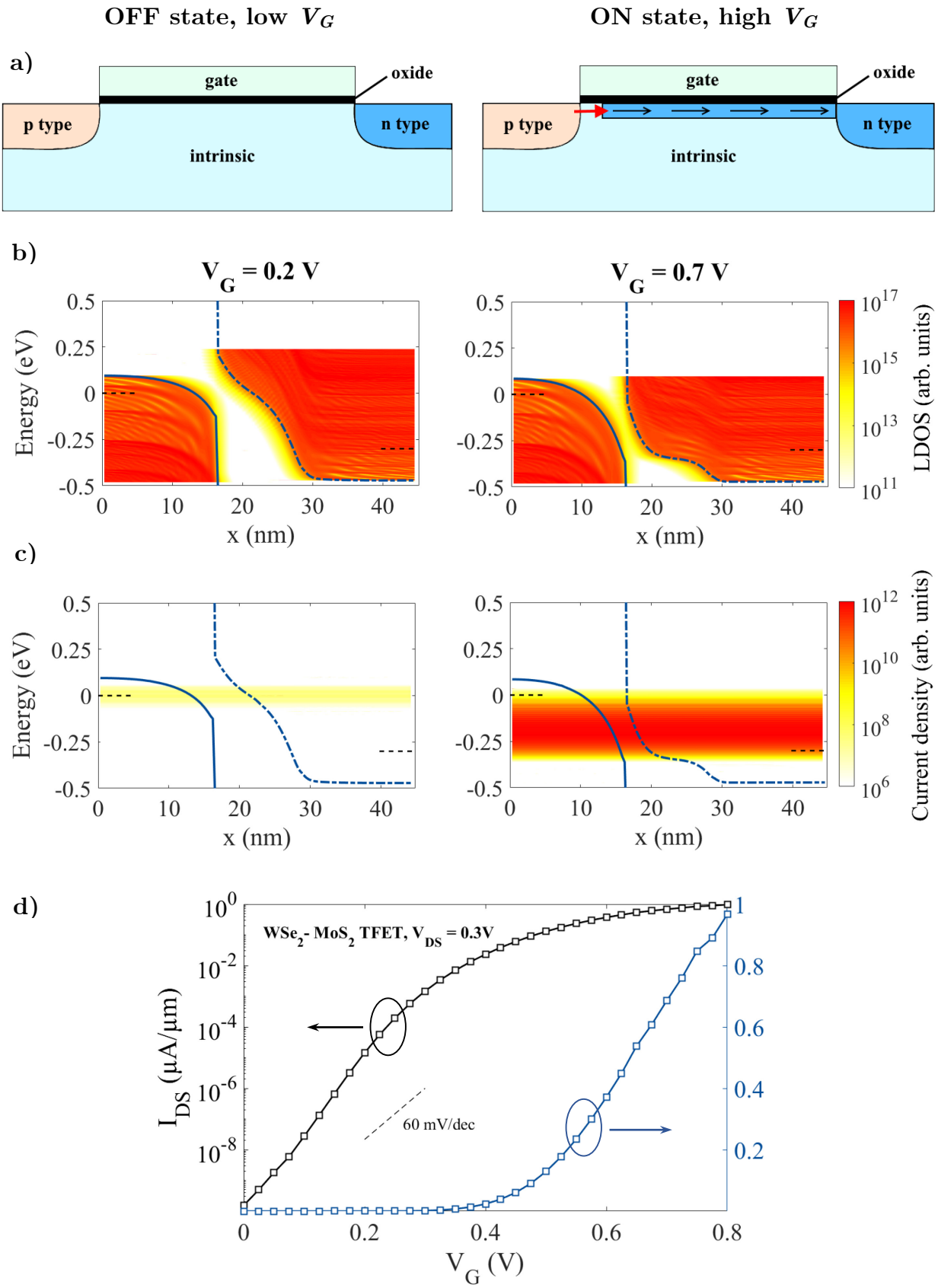


Figure 7. a) Sketch of an n-type TFET in the OFF (left) and ON state (right). b) Local density of states in a WSe_2-MoS_2 (strained) TFET in the OFF (left) and ON state (right). The dotted (full) blue line represents the lowest CB (highest VB), and the dotted black lines the Fermi levels in the source and drain. c) Current density in the same device. d) Current characteristics of the device at $V_{DD} = 0.3$ V.

Much like in a CMOS device, a p-type TFET and an n-type TFET can operate in a complementary way in order to create inverters and NAND gates for instance, which are the basic functions for logic operations.
Two types of lateral TFETs can be distinguished: homojunction TFETs and heterojunction TFETs.

- In a homojunction TFET the source, channel and drain are all composed of the same material (see Figure 8 (b)). A low band gap is therefore needed, as it is directly correlated to the length of the depletion region (the length through which the carriers will tunnel). If the band gap is too low however, a true OFF state will never be reached; finding the appropriate material is therefore very challenging.

- In a heterojunction TFET, at least two different materials are used. Most often, one material is used in the source, and the other in the channel and drain, thus creating an interface where the tunneling will occur. With this heterojunction approach, each material's individual band gap does not matter anymore; rather, the band alignment of those materials compared to one another is the most important parameter. For instance, in the case of an n-type TFET, using a material with a high VB in the source and another with a low CB in the channel and drain will be highly beneficial, as this favorable band alignment (known as a staggered gap) will reduce the length of the depletion region to be tunneled. These heterojunction devices are however more challenging to simulate and produce, due to the strains and lattice reconstructions imposed by the interface.

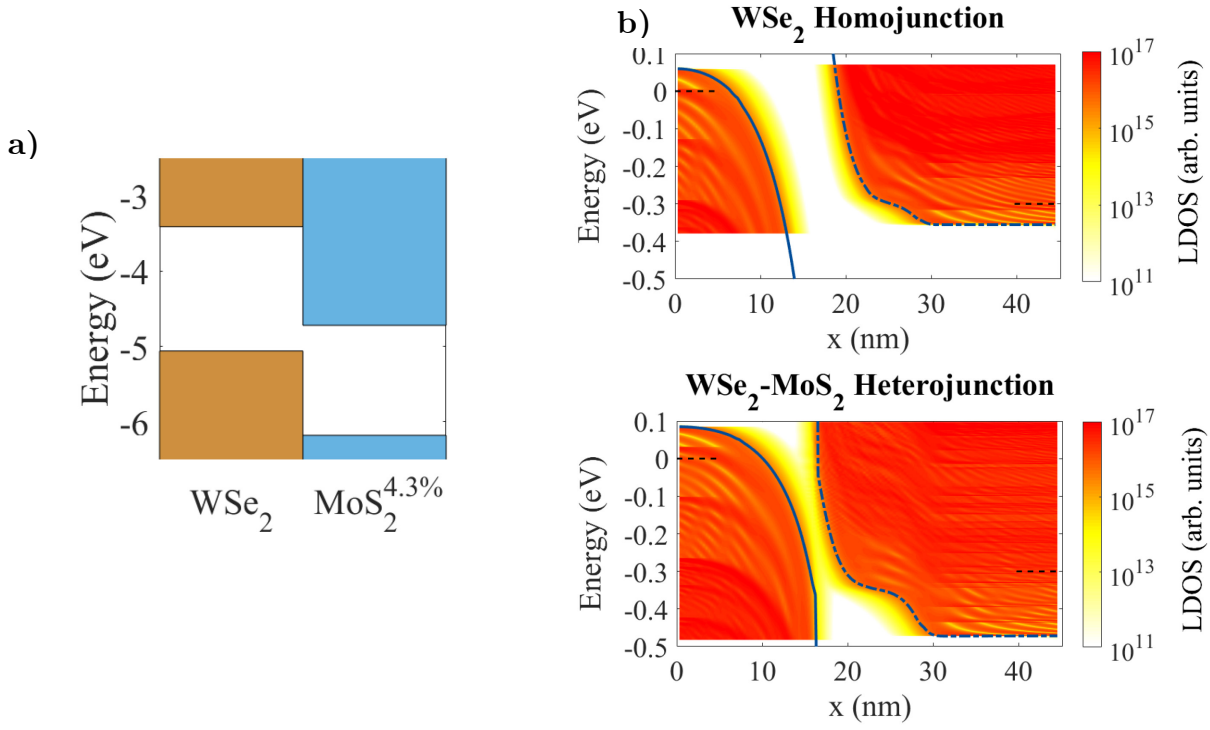


Figure 8. a) Band alignment for WSe_2 and MoS_2 (under a 4.3% tensile strain). b) LDOS of a WSe_2 homojunction TFET in the ON state; the depletion region is roughly 10 nm long. c) LDOS of a WSe_2-MoS_2 (strained) heterojunction TFET in the ON state; the depletion region is less than 5 nm long.

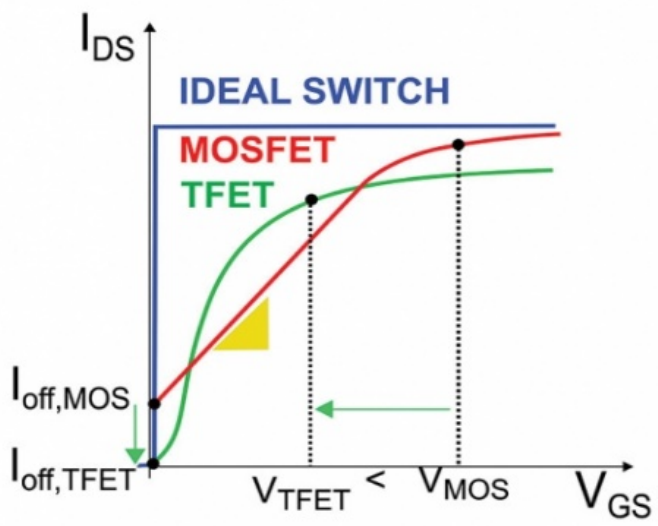


Figure 9. Typical current characteristic for a TFET (green), a MOSFET (red), and an ideal switch (blue).

Thanks to their BTBT injection mechanism (rather than the thermionic injection found in MOSFETs), TFETs have no lower limit for *SS*: because the carriers come from the top of the source VB, the band gap of the source material acts as an energy filtering mechanism and cuts the tail of the Fermi-Dirac distribution.

Theoretically, a properly designed TFET could therefore go from a fully OFF state ($I_{DS} \leq 10^{-5}$ µA/µm) to a fully ON state ($I_{DS} \geq 10^{3}$ µA/µm) with less than a 0.1 V increase in gate voltage; to perform the same transition, a perfect 60 mV/dec MOSFET would require at least a 0.5 V increase. However, because TFETs rely on tunneling through a bandgap of finite (real space) thickness, the maximum currents they can yield are often lower than that of similar MOSFETs.
Typical current characteristics for a MOSFET and a TFET are shown in Figure 9 and exemplify the typical behavior of each device: MOSFETs switch gradually from the OFF to the ON state but yield high ON current, while TFETs present a much steeper slope in the sub-threshold regime and yield lower current, but reach saturation at lower gate voltages. Finally, an ideal switch would go from a fully OFF state to a fully ON state with only an infinitesimal increase in V_G, and would yield extremely high I_{ON}.

Now that the operating principle and main characteristics of the TFET have been introduced, I will briefly discuss the history the device, and its current state-of-the-art.

1.4.2 History and current state of the TFET

The origin of the TFET can be traced back to 1978, when Quinn *et al.* [62] proposed to modify a MOSFET with a highly degenerate p-doped source. Later, in 1992[63], this design was realized based on GaAs, and named the surface tunnel transistor (STT) and was reported to exhibit transistor characteristics at room temperature. In the following years, TFETs based on silicon, SOI substrates, and InGaAs on InP substrates were reported[64]–[66]; however, in those early days the focus of TFETs wasn't their potentially low *SS*, but the possibility to control negative differential resistance (NDR) via the gate.

It was not until 2004 that discussion about the low-*SS* potential of TFETs started to gain traction[67]–[70] and ushered new interest in these devices. Since then, and due to the foreshadowing of the end of Si MOSFET scaling due to power consumption issues, interest in TFETs (along other steep-slope devices) has been growing rapidly.
By 2010, sub-60 mV/dec TFETs based on Si[71]–[73], Ge[74] and carbon nanotubes (CNT)[67], [75] had been reported.
Since its invention, the TFET structure has, much like the MOSFET structure before it, been tuned and modified to enhance device performance. Multiple-gate TFETs such as double-gate TFETs[76]–[78] and gate-all-around (GAA) TFETs[78], [79] have been reported to strongly enhance performance, namely increasing I_{ON} while decreasing I_{OFF} and V_T. In order to more precisely control the bands along the devices, structures such as dual material gates[80] (the gate material changes depending on the position along transport direction) and dual gate oxides[81] (the gate oxide changes depending on the position along transport direction) have been investigated.

In the last ten years, homojunction TFETs based on a wide variety of materials have been investigated: from Si[71], [72], [82], [83], Ge[74], GeSn[84], strained SiGe[85] to III-V semiconductors such as InGaAs[86], [87] and InAs[88], [89], some of which yielded relatively high ON currents and sub-thermal *SS*. The same cannot be said of heterojunction TFETs based on III-V semi-conductors such as AlGaSb/InAs[90], InAsSb/GaSb[91], InAs/GaSb[92], and others; these tend to achieve very high ON currents in exchange for *SS* far beyond 60 mV/dec.
More recently, theoretical studies of TFETs based on 2D materials have multiplied, due to the high interest garnered by those materials since the isolation of graphene in 2004[93]. Due to their one-atom thick structure, 2D materials have a host of advantages compared to their bulk counterparts; they are for instance free of dangling bonds and have a lower concentration of traps and roughness at the interface, which favor *SS*[94]–[96].
Vertical TFETs based on 2D materials such as graphene[97], [98] and transition metal dichalcogenides have been reported[99]–[101], some of which have shown potential for extremely low-power operation ($V_{DD} < 0.1$ V) thanks to sub-20 mV/dec *SS* and high I_{ON}.

Many lateral TFETs based on 2D materials have also been reported. Transition metal dichalcogenides, thanks to their direct band gap, are the most commonly used materials, and have shown great promise via low SS and relatively high I_{ON} both in homojunction[102], [103] and heterojunction TFETs[104]–[106]. Promising performance has also been reported for TFETs based on few-layer phosphorene[107], Bi_2Se_3 [108], and carbon nanotubes[109], [110] for instance.

Thanks to the unique advantages they offer compared to Si-based MOSFETs, for which the end of scaling is rapidly approaching, TFETs are uniquely positioned to take up the mantle and enable ultra-low power operation in nanoelectronics.
For this reason, TFETs are one of the hottest topics in transistor research today, and are at the center of this work.

Chapter 2

Introduction to 2D materials

2.1 History and characteristics of 2D materials

The first experimental isolation of graphene (by Geim and Novoselov in 2004[93]) and the subsequent demonstration of its extremely attractive properties ushered the golden age of 2D material research in all areas of physics; from condensed matter research to material science, mechanical engineering and nanoelectronics just to name a few.
Graphene suddenly became of extremely high interest, as can attest the exponential growth of the number of studies about graphene (shown in Figure 10), and even though the initial excitement over graphene has somewhat steadied over the past couple of years, it will most likely find its way into industrial use. However, the excitement ignited by graphene extended to all 2D materials, of which many were discovered and isolated in the following years.
While hexagonal boron nitride (h-BN) and transition metal dichalcogenides (TMDs) are the most commonly studied of those materials, research focused on many others such as silicene, germanene, black phosphorus and group-III mono-chalcogenides for instance, is being pursued in order to report and classify their properties.
The term "2D material" is quite vague considering the breadth of the properties of the materials classified as such. Some of them are semi-metals, some are insulators, some are semiconductors (with narrow to wide band gaps), some exhibit in-plane anisotropy[111]–[113] while others do not ... The one thing all 2D materials have in common is weak interlayer bonding due to van der Waals interactions, and strong intralayer covalent bonding. This weak interlayer bonding allows (in most cases) for mechanical exfoliation of a few layers or even a single layer -via the scotch tape method used to isolate graphene in 2004 for instance-; many research teams are therefore able to access 2D materials and study their properties.

From their atomic thickness also come several traits found across many 2D materials:

- Flexibility and elastic properties: most 2D materials exhibit exceptionally high mechanical properties. In 2008, a Young's modulus of 1 TPa and a breaking strength of 130 GPa were reported for graphene[114], while a similar study on MoS2 reported a Young's modulus above 200 GPa and a breaking strength of 27 GPa[115] which remains remarkable.

In-plane strains exceeding 20% are required to break those materials, making them extremely promising for potential use in flexible electronics for instance.

- Possibility of creating heterostructures with clean interfaces: their atomic thickness allows 2D materials to be either combined in-plane or stacked out-of plane in order to create heterostructures. By doing so, it is possible to drastically modify the properties of the structure, or protect it from its environment; for instance, the encapsulation of an air-sensitive material between two h-BN layers helps prevent degradation. In the case of in-plane heterojunctions, the absence of the out-of-plane dangling bonds[46] found in bulk materials allows for a much cleaner interface with far fewer traps and defects.

Due to the breadth of those properties, applications spaces for 2D materials are extremely broad and the main areas of focus of current academic research are therefore to classify those materials, determine the limits of their performance, and develop the growth and deposition techniques needed to integrate them in future devices. For instance, although the electron mobility is extremely high in graphene, the absence of a band gap prevents its use for logic applications, and the relatively low mobility in TMDs make them poor candidates for MOSFET technology. There is therefore a necessity to study those materials and determine the best possible use of their properties, while avoiding their inherent setbacks; once the appropriate application will have been determined, the tall order of scaling up and maturing the resulting technology will remain.

In this chapter, I will present the crystal structure and electronic properties of several 2D materials, before briefly outlining some of their potential applications in nanoelectronics and optoelectronics and the state of the art deposition and growth techniques related to them.

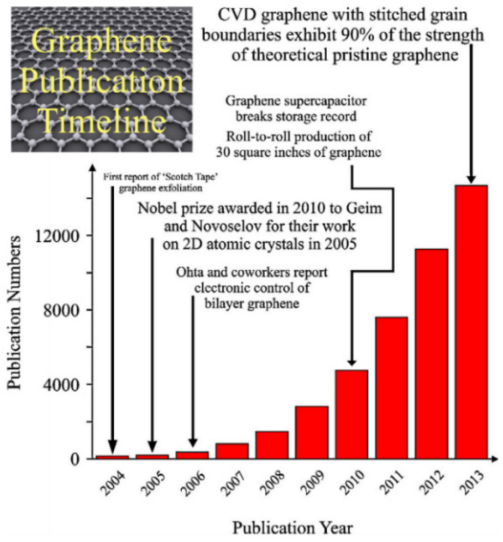


Figure 10. Number of publications about graphene per year, from 2004 to 2013, from [116].

2.2 Properties of 2D materials

2.2.1 Graphene

As mentioned above, graphene is the origin of today's interest in 2D materials. This can be attributed to the fact that many of its properties are best in class: unparalleled mechanical stiffness, strength and elasticity, as well as supreme electrical and thermal conduction[52]. However, some of its inherent drawbacks, such as the absence of a band gap, will force technology to adapt to graphene and complicate its integration.

2.2.1.1 Crystal structure

Graphene is a one-atom-thick sheet of honeycomb arranged sp^2 hybridized carbon atoms with a lattice constant of $a_G = 2.46$ Å, which itself can be divided in two sublattices. The C-C bonds are separated by an angle of 120° , and have a length of $d_{C\text{-}C} = 1.42$ Å[117].

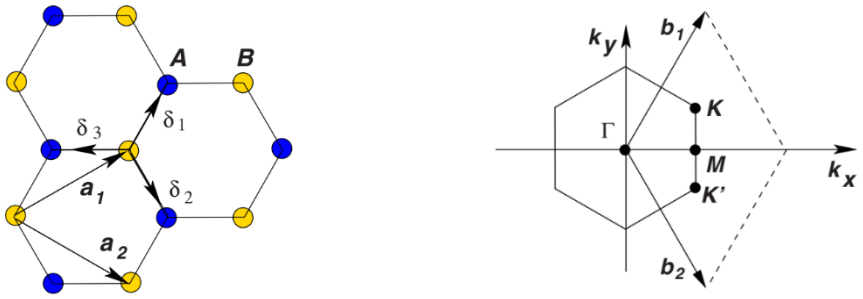


Figure 11. Left : Lattice arrangement of graphene in which $a_{1,2}$ are the lattice unit vectors and $\delta_{1,2,3}$ are the nearest neighbor vectors. Right : first Brillouin zone of graphene[118].

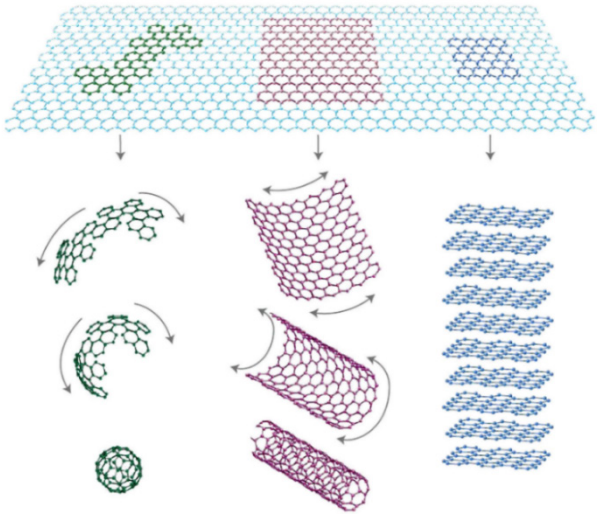


Figure 12. Graphene (top) and related structures: fullerene (left), carbon nanotube (center) and graphite (right) [119].

As presented in Figure 12, graphene is the basis for many carbon allotropes such as graphite (stack of graphene sheets), fullerenes (graphene sheet rolled up into a ball) and carbon nanotubes (graphene sheet rolled up into a tube).
Now that I have briefly described the crystal structure of graphene, I will present its electronic properties which, along with its mechanical and optical properties, make it one of the most interesting materials currently available.

2.2.1.2 Electronic and transport properties

Due to its atomic arrangement, the electronic dispersion of graphene presents cones at the K and K' points of the first Brillouin zone, where the valence and conduction bands meet (see Figure 13). At those wave vectors, the dispersion increases linearly with the energy, which mimics the physics of quantum electrodynamics for massless fermions. Although they move with a velocity approximately 300 times smaller than the speed of light, those electrons are therefore referred to as "massless Dirac fermions". This behavior allows for specific rare phenomena to occur in graphene, such as the integer quantum Hall effect that was observed experimentally[120], and the possibility for Klein tunneling, a non-relativistic process in which the transmission through a potential barrier may be almost perfect and non-dependent on barrier height or length[118].
This linear dispersion allows graphene to present extremely high carrier mobility, beyond 200 000 $cm^2.V^{-1}.s^{-1}$[121] -compared to 1400 $cm^2.V^{-1}.s^{-1}$ in silicon- and a large critical current density of 10^8 $A.cm^{-2}$[93]. However, the absence of a band gap induced by those Dirac cones greatly limits the potential of graphene for logic operation; without a band gap, a graphene transistor cannot be properly switched off and the resulting I_{ON}/I_{OFF} ratios are very low. With that said, high transconductance has been observed in large area graphene field effect transistors[122], which suggests they could be used for radio frequency and analog applications.
There are, however, several techniques to open up a bandgap in graphene, some of which are presented below:

- Bilayer graphene: by applying a transverse electric field to bilayer graphene (stack of two graphene layers), a band gap of width dependent on the applied voltage can be opened near the K-point [123], [124]. This band gap can span up to 250 meV, which is too low for most electronic applications.
- Graphene nanoribbons: by nanostructuring graphene into ribbons of a specific width, a band gap can be opened in graphene[118]. However, this is only possible in perfect armchair type nanoribbons for which the number of carbon dimers along the width is $M = 3n$ or $3n + 1$, $\forall n \in \mathbb{N}$. In this case, the width of the band gap is inversely proportional to the nanoribbon width, and extremely narrow GNRs are therefore required to obtain usable band gaps[125]. In the case of zigzag type nanoribbons, edge states prevent the opening of a band gap (see Figure 14).

However, while this behavior is observed in theory and perfect nanoribbons, edge disorder in experimental setups have shown a universal electronic behavior in graphene nanoribbons, no matter the ribbon orientation[126].

- Graphene nanomesh : by creating periodic defects in a graphene sheet, a band gap of up to 500 meV can also be opened [127]–[129]. However, controlling the exact shape and periodicity of the defects can prove challenging in an experimental setup.

Although graphene is the reason for today's tremendous interest in 2D materials, many other 2D materials exhibit interesting properties and could potentially find their use in future devices. TMDs -which I will now present- are, apart from graphene, one of the most studied class of 2D materials.

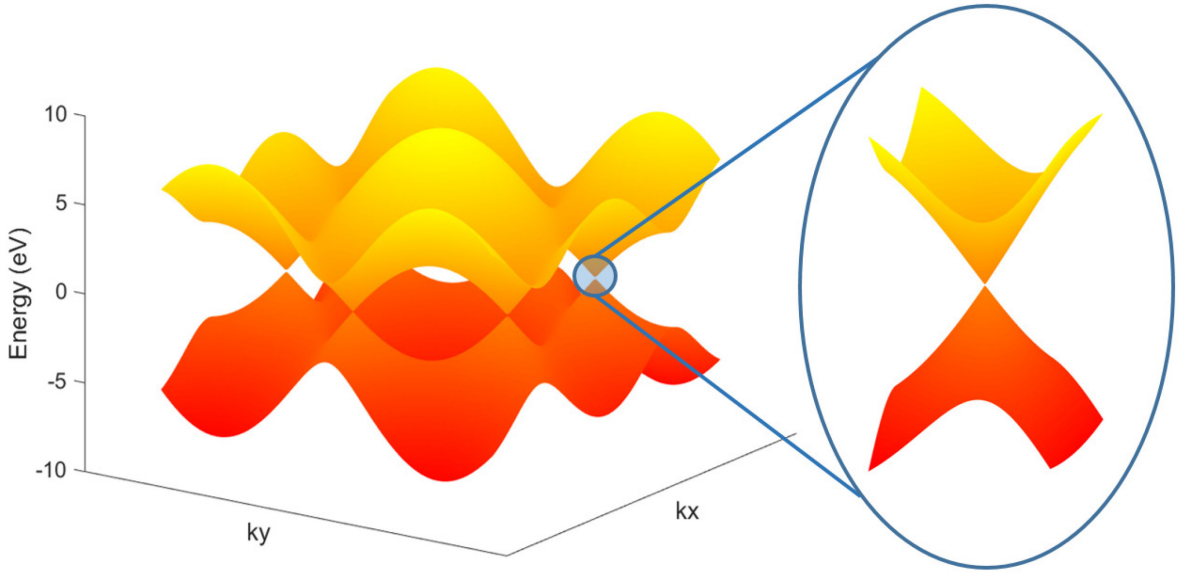


Figure 13. Electronic band structure of graphene, and zoom on one of the Dirac points.

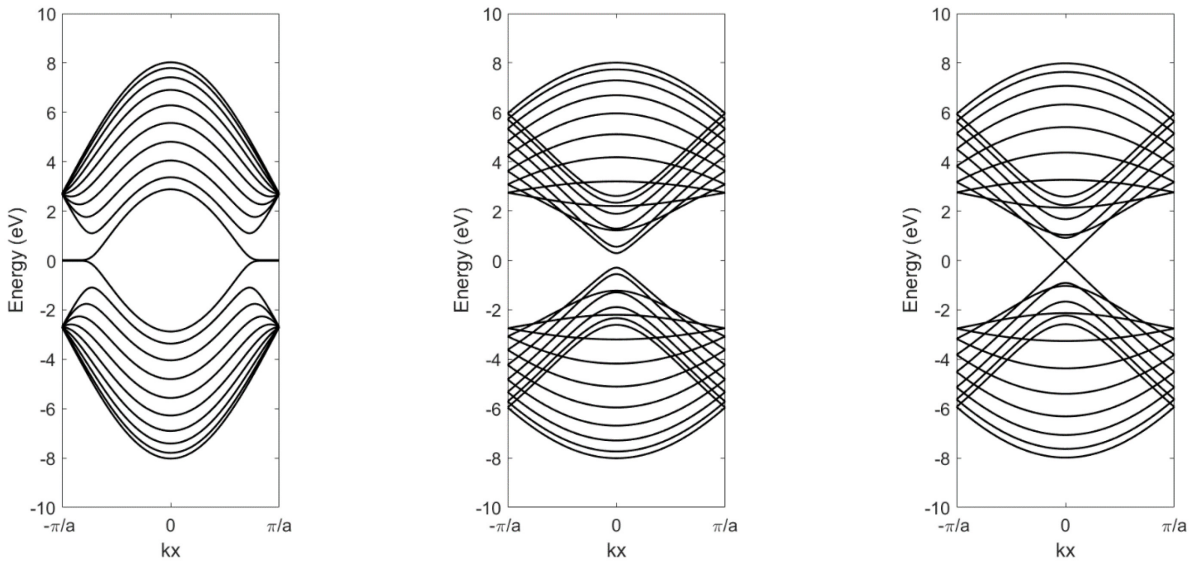


Figure 14. Electronic dispersion diagrams in $ky = 0$ for several types of perfect graphene nanoribbons.
Left : zigzag nanoribbon, Center : armchair nanoribbon of width $M = 3n$ or $3n + 1$.
Right : armchair nanoribbon of width $M = 3n + 2$.

2.2.2 Transition Metal Dichalchogenides

TMDs are a class of materials composed of one transition metal atom for every two chalcogen atoms. Although the metal can be from groups IV, V, VI, VII or X, the TMDs garnering the most research interest are those bearing a group VI transition metal. They are of the type MX_2, and are more specifically MoS_2, $MoSe_2$, $MoTe_2$, WS_2, WSe_2 and WTe_2. Although they exist in bulk form, I am solely interested in their monolayer form; I will therefore refer to group-6 monolayer TMDs as "TMDs" from this point on.

2.2.2.1 Crystal structure

A TMD monolayer is actually composed of 3 separate layers : a top X layer, a middle M layer, and a bottom X layer (see Figure 15). They can exhibit three phases: hexagonal (2H), octahedral (1T), and distorted octahedral (1T'). In both octahedral phases, TMDs are semi-metallic, whereas they are semiconducting in the hexagonal phase; since the goals of my PhD project are focused on nanoelectronics applications, I will describe only the hexagonal phase of those materials. In this phase, the coordination is trigonal prismatic[130] and the chalcogen atom determines the lattice parameter of the structure -which I report in Table 1.

2.2.2.2 Electronic and transport properties

2H-TMDs are semiconductors with direct bands gaps ranging from 1.2 to 2 eV (as calculated by the TB model used throughout this work, which will be presented in detail later) and effective electron masses ranging from $0.45 \times m_e$ to $0.65 \times m_e$[132]. Although their theoretical mobilities range from 350 $cm^2.V^{-1}.s^{-1}$ for MoS_2 to more than 2500 $cm^2.V^{-1}.s^{-1}$ for $MoTe_2$ [133], the measured experimental mobilities are far lower, in part due to the creation of a substantial Schottky barrier at the contact. For instance, a mobility of $0.5 - 3$ $cm^2.V^{-1}.s^{-1}$ has been measured in MoS_2, and can be improved up to 160 $cm^2.V^{-1}.s^{-1}$ by encapsulating the monolayer in a high-κ dielectric or a polymer electrolyte[134], [135], and mobilities up to 50 $cm^2.V^{-1}.s^{-1}$ were reported in WS_2[136].

$\mathbf{MX_2}$	MoS_2	WS_2	$MoSe_2$	WSe_2	$MoTe_2$	WTe_2
a (Å)	3.18	3.18	3.32	3.32	3.55	3.55
E_{gap} (eV)	1.79	1.95	1.55	1.65	1.25	1.23

Table 1. Lattice parameter (as reported in [131]) and band gap (as calculated in the DFT-validated TB model used) of the considered TMDs.

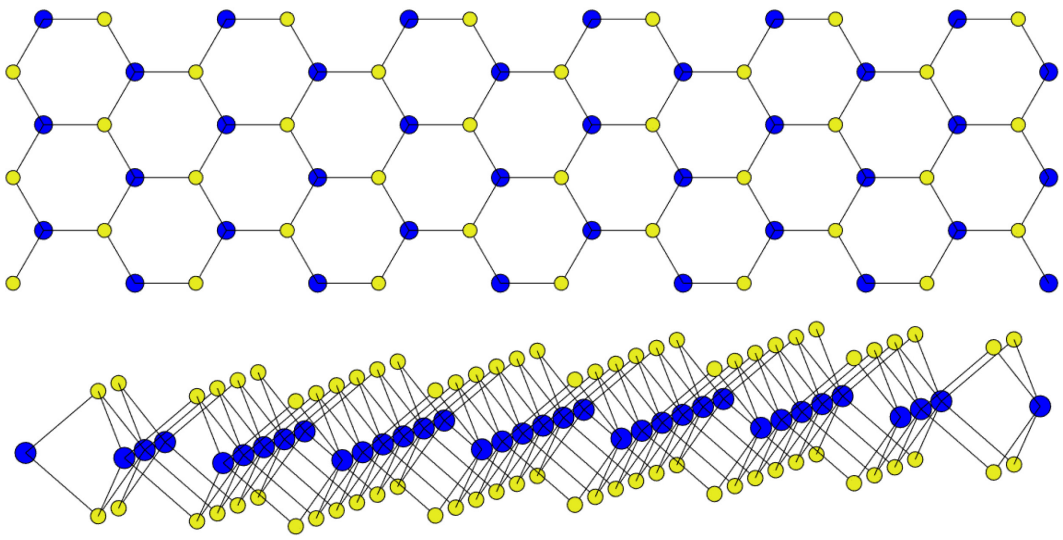


Figure 15. (top) Overhead view of a TMD monolayer in its hexagonal phase, in which yellow markers represent the chalcogen atoms and the blue markers represent the transition metal atoms. (bottom) Side view of the same TMD.

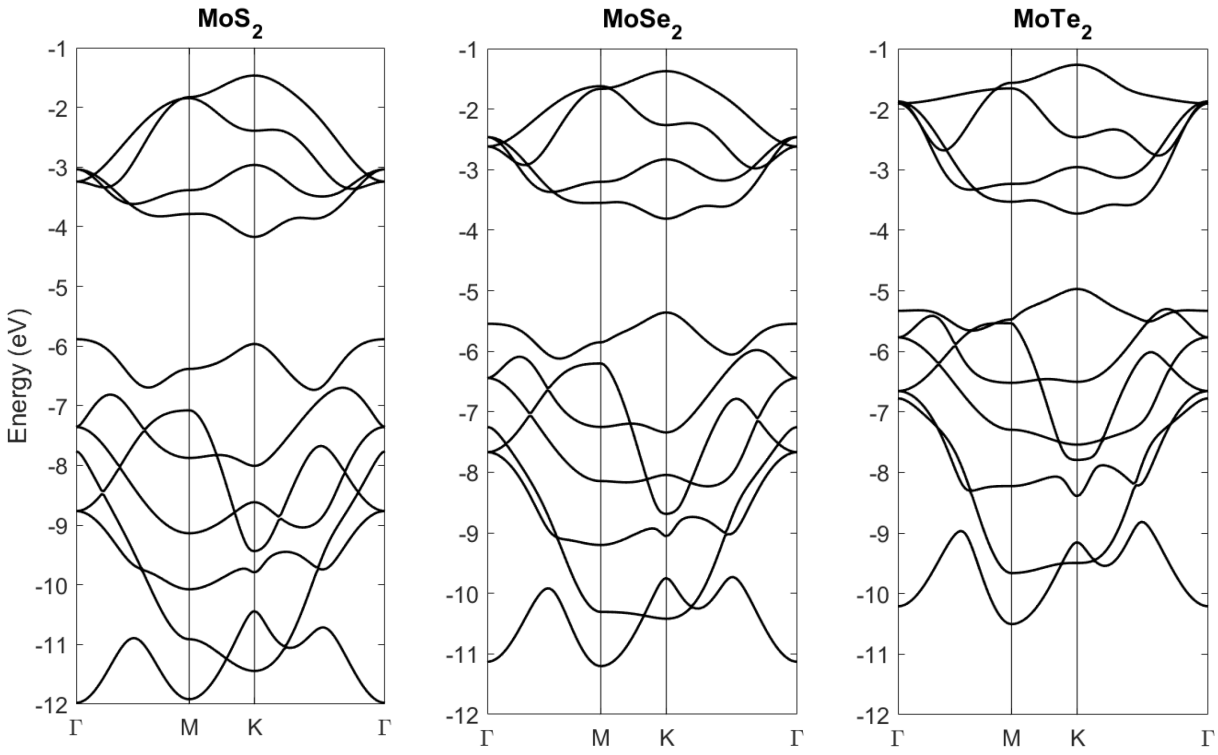


Figure 16. Electronic dispersion along the high symmetry directions of the first Brillouin zone for three of the six considered TMDs.

TMDs are the materials on which I mainly focused for this work, and ultimately, the ones used in the devices presented in the "results" section of this manuscript. However, studying other 2D materials and their properties remains interesting and can lead to novel ideas and uses. In this next part, I will therefore present a few other 2D materials.

2.2.3 Other 2D materials

As I mentioned in the introduction to this part, 2D materials have an incredibly broad range of properties and therefore of potential applications. Even though I did not study the following materials during my PhD work, they remain interesting and worth quickly presenting in order to present a more complete view of 2D materials. The materials discussed here are hexagonal boron nitride, silicene, germanene and phosphorene.

2.2.3.1 2D hexagonal boron nitride

2D Hexagonal boron nitride (hBN) is an isomorph of graphene in which the 2 sublattices are occupied with boron and nitrogen atoms arranged in honeycomb formation. It has a lattice parameter of $a_{h-BN} = 2.5$ Å [137], which is therefore very close to that of graphene ($a_G = 2.46$ Å). Just as is the case for graphene, h-BN layers can be stacked. hBN is an insulator, with a band gap of approximately 6 eV[137] and presents a piezoelectric effect, which enables applications in sensing and actuating. Its high thermal stability (1000 °C in air [138]), thermal conductivity ($\kappa \sim 484\ W.m^{-1}.K^{-1}$) and mechanical strength (Young's modulus ~ 1 TPa) [139] also benefit h-BN in other applications. For instance, its layered nature makes it viable for use as a lubricant both in sintered body or in powder form[140], another example is its use for the last 30 years in the metallizing industry, where it is used as an evaporation boat for aluminum[140] Thanks to its very small lattice mismatch with graphene, h-BN has the potential to be an ideal platform for graphene electronics, but also an efficient capping layer thanks to its inert nature, protecting the structural and chemical integrity of the active layer. Many studies have investigated graphene-hBN heterostructures, whether vertical (van der Waals) or horizontal (in-plane). Several vertical graphene–hBN transistors exhibiting a strong negative differential resistance (NDR) effect[141] that can be partially controlled via the twist applied to the layers [142] have been reported for example. However, the low I_{ON}/I_{OFF} ratios and high sub-threshold swings of such devices[97], [143] present a fundamental barrier to an integrated circuit application.

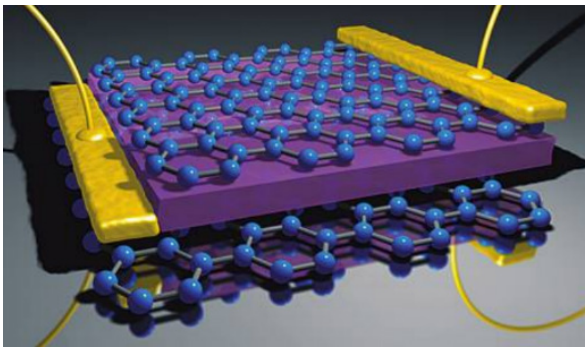


Figure 17. Vertical transistor made up of stacked hBN monolayers encapsulated between graphene contacts [97].

2.2.3.2 Silicene and germanene

Silicene and germanene are quasi-2D materials made up of sp^2 hybridized silicon atoms arranged in a hexagonal lattice. However, contrary to graphene, this hybridization is unstable and leads to a "buckling" of the structure: the silicon/germanium atoms are shifted slightly out of plane (see Figure 18), hence the quasi-2D term.
Much like graphene, they both present a linear electronic dispersion around the K and K' points of the Brillouin zone[144]–[147] -which leads to the existence of massless Dirac Fermions along those directions-, but do not present a band gap. However, due to their buckled nature, a small tunable band gap of several tens of meV can be opened by applying a transverse electric field on the structure[148] -as is the case in graphene bilayers- or by surface adsorption[149], [150]. This ability to open a band gap, coupled with their extremely high calculated electron mobilities (2.57×10^5 $cm^2.V^{-1}.s^{-1}$ for silicene [151] and 6×10^5 $cm^2.V^{-1}.s^{-1}$ for germanene [152]) makes them highly interesting for logic applications. Silicene especially, thanks to its natural compatibility with current silicon-based electronics, is being investigated for nanoelectronic applications[153], [154]. In both silicene and germanene, this band gap opening can also give rise to novel physical properties such as the quantum Hall effect due to a high spin-orbit coupling [155], which only increases their attractiveness for various applications.
Silicene and germanene have been experimentally demonstrated in 2012 and 2014 respectively, but the techniques related to their deposition are being improved upon. Silicene has for now been grown on several specific metallic substrates such as Ag(111) [156]–[160], ZrB_2(0001) and Ir(111), but its deposition remains a challenge due to its high instability in air. Germanene growth was also a challenge because of its tendency to favor sp^3 hybridization rather than sp^2, and therefore give way to its hydrogenated cousin, germanane. In spite of this challenge, germanene was successfully deposited on a variety of materials ranging from metals such as Al(111)[161]–[163], Au(111)[164], [165] or Pt(111)[166], but also MoS_2, [167] or Sb[168].
Silicene and germanene, much like graphene, can also be used to create nanoribbons, either armchair or zigzag (depending on the edge type). Ab-initio studies of those nanoribbons have shown that half-metallicity[169] and giant magnetoresistance[170] can arise in those ribbons, paving the way for possible applications in spintronics.

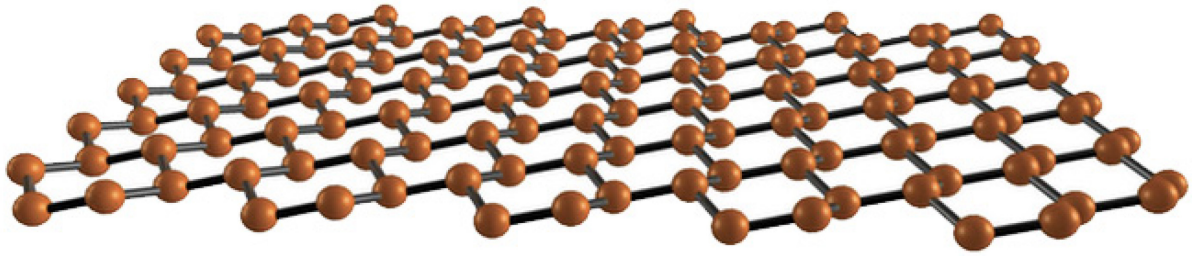


Figure 18. Lattice arrangement of silicene and germanene.

2.2.3.3 Phosphorene

Phosphorene is the 2D form of black phosphorus, the most stable phosphorus allotrope at room temperature, and was first isolated in 2014. Just like graphite, the layered structure of black phosphorus is held together by van der Waals forces, and allows phosphorene to be mechanically exfoliated, much like graphene[171]. Phosphorene layers share a hexagonal lattice arrangement with the other 2D materials previously mentioned, but present a high non-planarity referred to as "puckering" (shown in Figure 10) that differs from the buckling found in silicene and germanene. It has been shown[172] that black phosphorus has a direct band gap of 0.36 eV, which increases exponentially as the number of phosphorene layers decreases, reaching an appreciable value of 1 eV for a single phosphorene layer. This high dependence of the band gap on the number of layers is extremely interesting, as it would allow to tune the band gap depending on the desired application. Another interesting aspect is its reaction to electric fields: under a transverse electric field, the material turns from a semiconductor into a Dirac semi-metal with linear dispersion along the armchair direction[173], in part similar to the dispersion found in graphene for instance. Phosphorene is highly flexible and can resist stresses of up to 30% [174], [175], even though its Young modulus is one order of magnitude smaller than that of graphene. Its reaction to strain is peculiar, as the band gap experiences a direct-indirect-direct transition under axial strain before closing completely at a strain of roughly 13% [174]. Effective masses are also highly impacted by strain, allowing for yet another tuning mechanism to obtain the desired properties. Overall, significantly lower effective masses were reported in the armchair direction than in the zigzag direction, indicating that it is favored for carrier transport[174].

Due to these many interesting properties arising from its puckered structure, phosphorene is an exciting and promising candidate for electronic and optical applications [176]–[181]. Several p-type FETs based on few layer phosphorene have been studied, yielding ON currents of a few hundred mA/mm, and hole mobilities in the order of several hundred $cm^2.V^{-1}.s^{-1}$ [171], [172], [176]. In a particular instance[171], it was used in conjunction with an MoS_2 n-type FET to create the first CMOS inverter based on 2D materials.

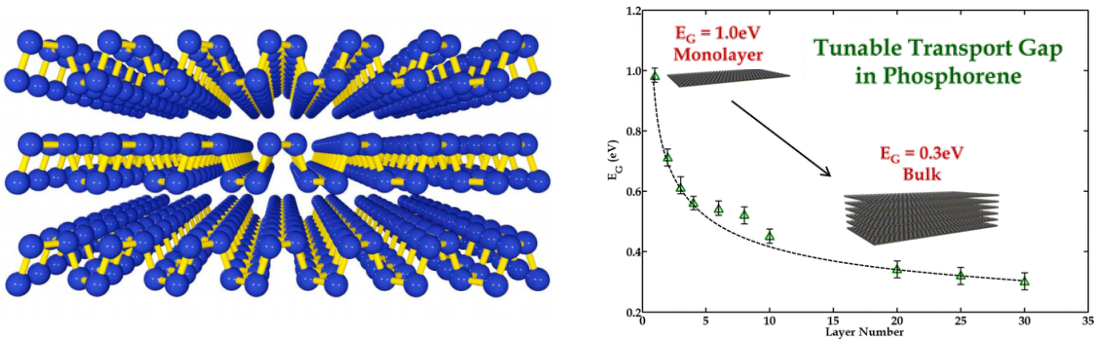


Figure 19. Left : Atomic arrangement of few layer phosphorene.
Right: Evolution of its band gap with respect to the number of layers [172].

2.3 Atlas of 2D materials

In this part, I will present tables categorizing many known and theorized 2D materials. However, note that this list is not intended to be exhaustive, and that its goal is solely to highlight the breadth of materials being actively researched.
For each listed material, information on the band gap (its value and whether it is direct or indirect), and whether the material has been isolated experimentally (yes/no) is given. As most of these materials are still relatively new, band gap values are highly dependent on the method used to obtain them; therefore, the values mentioned here give a general indication, but **are not to be considered absolutely accurate**. Several references are given for each material, should the reader be interested in getting more information on a particular material.
Please note that neither oxides based on mentioned 2D materials (such as graphene oxide), nor layered covalent organic frameworks are listed here.

For page layout considerations, the first table starts on the next page.

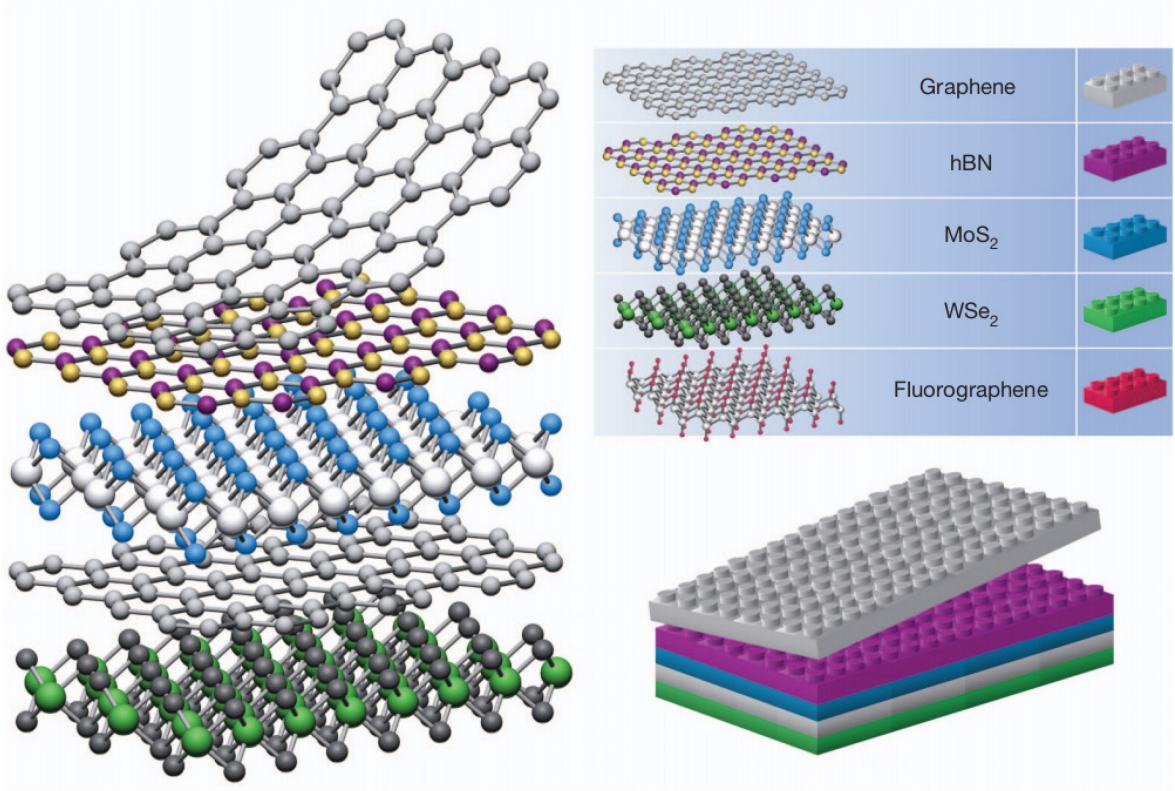


Figure 20. The "lego-like" possibilites of van der Waals heterostructures allowed by the breadth of 2D materials [182].

		Material	E_G (eV)	Exp	References
Graphene-like	-ene	Graphene	---	Y	[119]–[121]
		hBN	4.70 (D)	Y	[137], [140], [183]
		Silicene	---	Y	[144], [157], [160]
		Germanene	0.02 (D)	Y	[163]–[165]
		Silicon carbide	2.55 (D)	Y	[184], [185]
		Stanene	0.10 (D)	Y	[186]–[188]
		Phosphorene	1.88 (D)	Y	[178], [179], [187]
		Borophene	---	Y	[189]–[191]
		Gallenene	---	Y	[186], [192]
		Antimonene	2.28 (I)	Y	[193], [194]
		Arsenene	2.49 (I)	Y	[193], [194]
		Bismuthene	0.55 (D)	Y	[193], [195], [196]
		Selenene	0.13 (D)	Y	[186], [197]
		Tellurene	0.16 (D)	Y	[186], [197]
	hydrogenated (-ane)	Graphane	3.56 (D)	Y	[198], [199]
		Silicane	2.26 (I)	Y	[186], [200]
		Germanane	1.16 (D)	Y	[200], [201]
	halogenated	Fluorographene	3.29 (D)	Y	[199], [202], [203]
		Chlorographene	2.80 (D)	Y	[204]–[206]
		Bromographene	0.08 (D)	Y	[205], [206]
		Iodographene	unknown	Y	[205], [206]
		Fluorophosphorene	---	N	[207]
		Chlorophosphorene	---	N	[207]
		Bromophosphorene	---	N	[207]
		Iodophosphorene	---	N	[207]
		Fluorosilicene	1.47 (D)	N	[186], [208], [209]
		Chlorosilicene	1.97 (D)	N	[186], [208], [209]
		Bromosilicene	1.95 (D)	N	[186], [208], [209]
		Iodosilicene	1.19 (D)	N	[186], [208], [209]
		Fluorogermanene	0.20 (D)	N	[210]–[212]
		Chlorogermanene	0.08 (D)	N	[210]–[212]
		Bromogermanene	0.23 (D)	N	[210]–[212]
		Iodogermanene	0.16 (D)	N	[210]–[212]
	-yne	Graphyne	0.50 (D)	Y	[199], [213], [214]
		Graphdiyne	0.46 (D)	Y	[199], [213], [214]
		Silicyne	0.73 (D)	N	[215], [216]
		Silicdiyne	0.43 (D)	N	[217]

	Material		Gap (eV)	Exp	References
Transition Metal Dichalcogenides (TMDs)	MoS_2	T	---	Y	[132], [135]
		H	2.02 (D)	Y	[132]
	$MoSe_2$	T	---	Y	[132], [218]
		H	1.72 (D)	Y	[132], [185]
	$MoTe_2$	T	---	Y	[132], [219]
		H	1.28 (D)	Y	[132], [185]
	WS_2	T	---	Y	[136], [136]
		H	1.98 (D)	Y	[115], [185]
	WSe_2	T	---	Y	[185], [220]
		H	1.63 (D)	Y	[220]
	WTe_2	T	---	Y	[113]
		H	1.03 (D)	Y	[113], [221]
	ZrS_2	T	1.10 (I)	Y	[222], [223]
		H	0.92 (I)	Y	[222], [223]
	NbS_2	T	---	Y	[224], [225]
		H	---	Y	[224], [225]
	PdS_2	T	1.17 (I)	Y	[226]
		O	1.11 (I)	Y	[226]
	TiS_2	T	1.65 (I)	Y	[227]
		H	1.25 (I)	Y	[227]
	NiS_2	T	---	Y	[226]
		O	0.52 (I)	Y	[226]
	PtS_2	T	---	Y	[226], [228]
		O	1.75 (I)	Y	[226], [228]
	HfS_2	T	1.27 (I)	Y	[222]
	$HfSe_2$	T	0.61 (I)	Y	[222]
Transition Metal Chalcogenides (TMCs)	ZnS	α	2.58 (D)	Y	[229], [230]
		β	2.57 (D)	Y	[229], [230]
	ZnSe	α	1.91 (I)	Y	[231]
		β	2.01 (D)	Y	[231]
	CdS	α	1.72 (D)	Y	[232]
		β	1.65 (D)	Y	[232]
	CdSe	α	1.20 (I)	Y	[232], [233]
		β	1.30 (D)	Y	[233], [234]

T, H, and O refer to the tetrahedral, hexagonal and orthorhombic phases of the considered TMDs, while α and β refer to the flat and corrugated phases of the considered TMCs.

		Material	Gap (eV)	Exp	References
Transition Metal Halides (TMHs)	MY_2	$CaCl_2$	5.97 (I)	N	[185]
		$CaBr_2$	5.13 (I)	N	[185]
		$MnCl_2$	0.37 (D)	N	[185]
		$MnBr_2$	0.18 (I)	N	[185]
		$FeCl_2$	---	N	[185]
		$FeBrI_2$	---	N	[185]
		$NiCl_2$	1.06 (I)	N	[185]
		$NiBr_2$	0.64 (I)	N	[185]
	MY_3	$FeCl_3$	---	N	[185]
		$FeBr_3$	---	N	[185]
		$MoCl_3$	0.80 (I)	N	[235]
		$MoBr_3$	0.56 (I)	N	[235]
		$TiCl_3$	0.60**	N	[236]
		VCl_3	1.10**	N	[236]
Semimetal Chalcogenides (SMCs)		GaS	2.57 (I)	Y	[237], [238]
		GaSe	2.05 (I)	Y	[237], [238]
		GaTe	2.02 (I)	Y	[185], [237]
		InS	2.09 (I)	Y	[239], [240]
		InSe	1.70 (I)	Y	[239], [240]
		InTe	1.60 (I)	Y	[239], [240]

** $TiCl_3$ and VCl_3 are half-metals, so the gaps mentioned only apply to one spin direction.

2.4 Applications of 2D materials

Thanks to their often impressive suite of mechanical, optical, thermal and electronic properties, 2D materials are being regarded as a potential paradigm shift for many industries. In this section, I will go over some of the applications for which 2D materials might be best suited. Among those technological fields are, for instance, high-frequency electronic devices, data storage, photonic and optoelectronic devices, wearable and flexible devices, sensors, and bioelectronics, just to name a few. I will try to touch on most application spaces of 2D materials, in order to highlight the breadth of possibilities and uses they offer, but this section is by no means meant to be all-encompassing.

2.4.1 Electronics

Electronics is one of the main areas that could be revolutionized by graphene. Indeed, the ITRS considers graphene to be among the top candidates for post-Si electronics[16]. As mentioned earlier in this manuscript, current III-V and silicon based transistor are not able to keep up with Moore's law, due to the increase in heat dissipated per unit area caused by miniaturization. Furthermore, the miniaturization of bulk devices severely impacts performance such as reducing carrier mobility in silicon when decreasing the body thickness, or causing shifts in the band gaps of semiconductors due to quantum confinement. Circumventing this issue will require a drastic change in either the materials used in nanoelectronic devices, or in the types of devices used (or even both). With its incredibly high mobility, flexibility and virtually limitless quantity, graphene could be the material that revolutionizes the nanoelectronics industry.
However, its lack of band gap severely limits the potential of simple, pure graphene to be used in nanoelectronics. This zero band-gap is responsible for low I_{ON}/I_{OFF} ratio, and high static power dissipation. For instance, a typical static drain current of roughly 280 µA/µm at $V_{DD} = 2.5$V is observed in graphene inverters[241], against approximately 100 nA/µm at $V_{DD} = 0.75$V for Si based logic transistors[242]. Band gap opening is therefore heavily investigated, with techniques ranging from quantum confinement in 2D (graphene nanoribbons) and 1D (graphene quantum dot), selective chemical functionalization[198] to applying a transvers electric field to bilayer graphene[243], [244], or even via substrate-induced effects; a band gap of up to 0.5 eV was reported[245] in graphene on h-BN and h-BN/Ni(111) for instance.
Despite this drawback, the prospect that graphene devices could be scaled to extremely short channel lengths and high-frequencies while managing heat dissipation thanks to its astounding thermal properties[246] ensure an ever-growing number of studies on GFETs (Graphene Field Effect Transistors). The first GFET was reported in 2007 [247], and many have followed since, with increasingly promising characteristics[248]–[251].

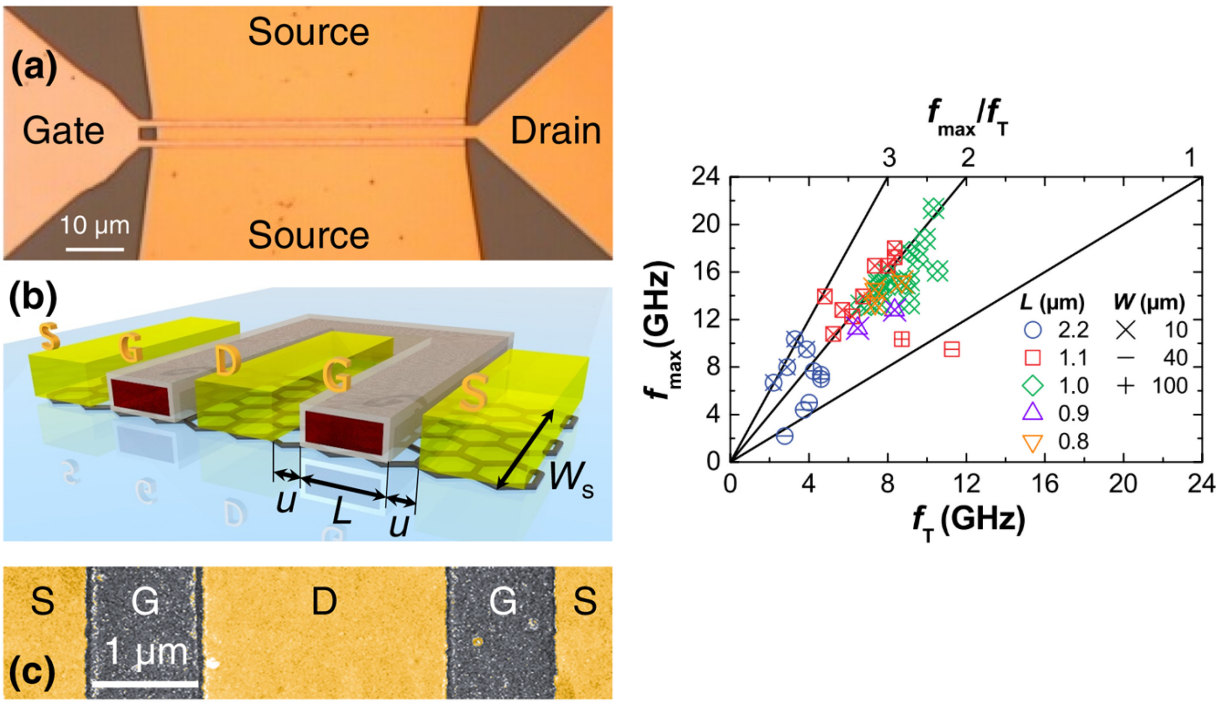


Figure 21. Left: High frequency GFET (a)Optical image of the GFET (b)Schematic of the central part of the GFET (c)SEM image of the central part of the GFET. Right: Maximum oscillation frequency as a function of the cutoff frequency of GFETs with varying gate lengths and channel widths [252].

A recent, encouraging GFET[252] provided high gain, frequency and transconductance, while outlining that several technological challenges such as improving the quality of CVD graphene and lowering both contact and gate resistance remain. While many challenges they face are as of now unresolved, GFETs remain a very promising avenue for post-Si electronics[253]–[255].

TMDs have also been considered and studied for use in FETs. Their semiconducting behavior and direct band-gaps ranging from roughly 1 to 2 eV especially MoS_2 being very attractive for logic uses. One of the first TMD-based FET was reported in 2004[256] and was based on WSe_2; it showed high p-type mobility, but a low I_{ON}/I_{OFF} of 10^4 and therefore was not suited for the intended logic applications. In 2011 however, a similar WSe_2 p-type device that was top-gated by a high-κ dielectric yielded far more promising performances, notably an I_{ON}/I_{OFF} of 10^6[257]. During the same year, an MoS_2 based device was also reported and showed great promise for n-type operation[258], yielding a an I_{ON}/I_{OFF} of 10^8 and high electron mobilities. Shortly thereafter, bilayer MoS_2 was used to great effect in the creation of several logic building blocks[135]: an inverter, a NAND gate, static RAM and a five-stage ring oscillator, although the ON currents yielded were lower than that of the aforementioned single-layer MoS_2 FET. In contrast, several issues relating to MoS_2 FETs are yet to be addressed: namely, control over material doping and the quality of electrical contacts need to be drastically overhauled, while p-type operation and ambipolar behavior would be desirable[53].

Beyond MOSFETs, 2D materials could also find their use in both vertical and in-plane TFET architectures. In the case of in-plane TFETs for instance, the quality of the interface is paramount and the absence of dangling bonds and drastically reduced concentration of traps found in 2D materials give them a strong advantage compared to bulk materials. As mentioned in the introduction to this manuscript, TFETs are one of the main avenues outlined by the ITRS for power scaling in transistors. They have the benefit of relying on BTBT and therefore not having any theoretical lower limit for *SS*, unlike MOSFETs, which physically cannot yield *SS* below 60 mV/dec at RT.
Several in-plane TFETs based on TMDs have been simulated[102], [104], and focused on comparing the viability of the different TMDs for TFET operation. Due to its lower band gap and effective mass, WTe_2 was identified in both cases as the most promising material, and yielded ON currents in the hundreds of µA/µm and *SS* around 20 to 30mV/dec[102]. In one of those reports, the viability of in-plane heterojunction between TMDs bearing the same chalcogen atom (WS_2-MoS_2 for instance) was investigated, and it was concluded that the WTe_2-MoS_2 heterojunction, once again due to the lower band gaps and effective masses, was the most promising; it was however unable to outperform the simulated WTe_2 homojunction device[104].
Vertical TFETs based on TMDs have also been simulated[99], [259]. In this case, device geometry parameters such as the overlap length between the stacked materials and extension of the gate over the contacts severely impact performance and therefore have to be carefully selected. MoS_2-WTe_2 is the most commonly used pair of materials, due to its favorable band aligment for TFET operation. Low *SS* figures of 20 to 30 mV/dec and I_{ON} as high as 10^3 µA/µm were reported[99], [259], which is very encouraging. It is worth noting, however, that phonon scattering and the effect of defects and impurities were not taken into account in those reports.

The works mentioned here are only a small portion of the active research happening on the integration of 2D materials in nanoelectronic devices, but they highlight the extremely high interest garnered by this class of materials for potential application in this field.

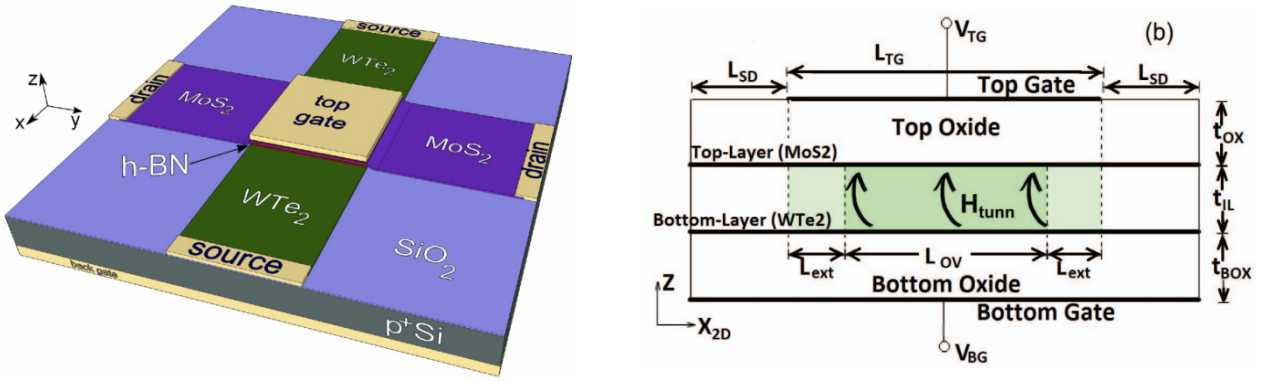


Figure 22. Left:3D sketch of the MoS_2-WTe_2 vertical TFET studied by *Cao et al.* Right: Sketch of the 2D structure simulated [99].

2.4.2 Spintronics

Spintronics is another research field that could benefit greatly from the advent of 2D materials. Unlike traditional electronics, that exploit the transport of electrical charges, spintronics's interest lies with the transport of spin. To this day, spintronics-based logic has been hampered by the need to achieve not only a high degree of control over spin, but also a long spin lifetime. This conflict and duality arises from the fact that a strong spin-orbit coupling character is usually needed to have a high degree of control over spin[260], but that such a strong spin-orbit coupling most often leads to fast spin decoherence[261].
Graphene, in its pristine form, exhibits negligible spin-orbit coupling[262] which leads to long coherence and spin relaxation times; it could therefore be a good candidate for use as a non-magnetic channel through which spin is transported. However, spin relaxation times in the order of nanoseconds (ns) have been reported in graphene[263] and the spin relaxation mechanism is not yet completely clear. Several relaxation mechanisms related to phonon and impurity scattering[260], [264]–[266] as well as the influence of the substrate and contact resistance between graphene and the magnetic electrodes[53] are at play here; further research is therefore needed to quantify and identify the contribution of each mechanism and tune the devices accordingly.
In addition to logic applications, graphene spintronic devices could potentially be used for sensing applications; thanks to its long spin diffusion length (beyond 30µm in single layer graphene[267] and up to 100µm in few layer graphene[268]), it could be used to develop magnetic sensors in the pT to nT range. Such spintronic sensors could find use in medicine, for instance to assist in tumour reduction or onsite drug delivery[53].

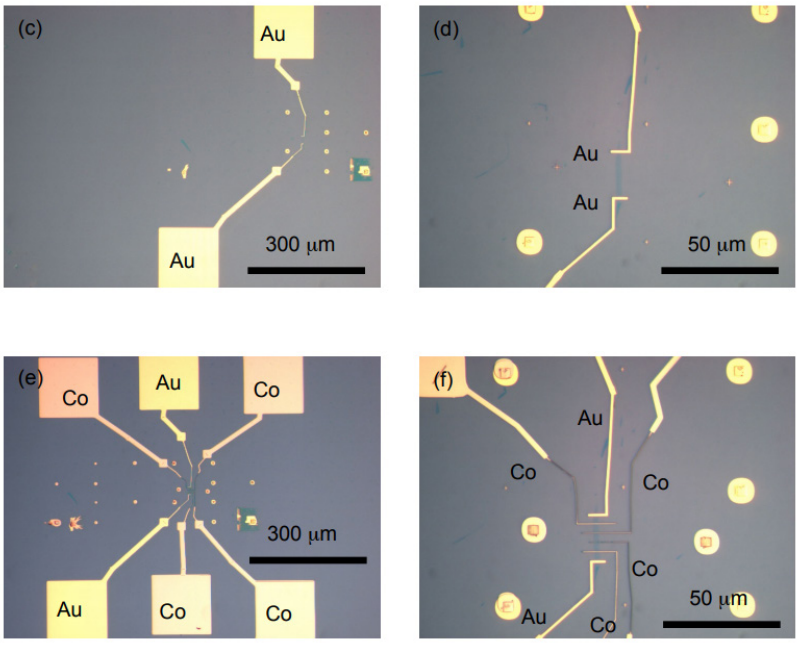


Figure 23. Graphene spin-valves on gold contacts (c,d) and with copper electrodes (e,f) [269]

As is often the case for other applications, graphene is the most prominently studied 2D material in the field of spintronics. However, it is by no means the only 2D material with possible use in this field. It has been theorized[270] and later shown[271], that MoS_2, non-magnetic in its pristine form, can acquire a magnetic moment by adsorption of other transition metal atoms (Mn, Fe, Co, Ni) on a Mo site, allowing for MoS_2 based spintronics applications[53], [272], [273].
Due to their generated valley in the K and K' point of the Brillouin zone, TMDs also show great promise[274], [275] in the field of valleytronics[276], [277], in which an optical excitation can be used to finely control carrier momentum, therefore using different valleys to store information separately.

2.4.3 Optoelectronics and photonics

Photonics and optoelectronics are among the research fields that are heavily impacted by the advent of 2D materials, and only a small sliver of the many possible applications are mentioned here. Graphene, especially, has a slew of advantages compared to usually used materials: it has very large carrier concentrations[278], wavelength-independent absorption[279], low dissipation rates[280] and its optical properties can be tuned by electrostatic doping, just to name a few. For instance, thanks to its high compatibility with CMOS processes, graphene is a promising candidate for optical interconnects operating at high data rates[281]–[283], and its flexibility would allow for integration on a flexible substrate[284]. Another example would be the detection of wavelengths outside the limit set by the band gaps of semiconductors currently used; thanks to its wide absorption spectrum, detection in the far infra-red (THz range), as well as short-wave infra-red would be possible with graphene. This property could also be used[285] to create optical limiters (devices with a low transmittance for high intensity light) across a broad spectrum; such limiters garner great interest for eye protection and sensing applications since, in their current form, no limiter can cover both the visible and the near-infra-red range[285]. Indeed, broad optical limiting capabilities were reported for LPE graphene in the case of ns pulses[286]. Photodetectors can also benefit from the wide range of absorption[287], [288] and ultrafast response found in graphene[289]; many photodetectors with varying designs based on graphene have been realized[290]–[292] and yielded impressive performance, such as in a communications link at 10 $Gbit.s^{-1}$[289] for instance.
Laser technology based on graphene has been studied since the late 2000s, and yielded promising results. An ultrafast LASER, mode-locked by a graphene saturable absorber was first reported in 2009[293] with a low output power of 1 mW, but following reports[294]–[296] have improved upon this work and reached output powers beyond 3 W[294], for discrete pulses ranging from 1 to 2µm depending on the report. The widest range reported yet is found in ref [296] and extends from 1525 to 1559nm, for picosecond (ps) pulses.

TMDs can also find use[297] in optoelectronics thanks to their transparency and flexibility. Among other applications, photodetectors based on MoS_2 have shown stable switching times of 50 ms[298] and high photoresponsitivity[299] (880 $A.W^{-1}$ at 561 nm), and the ability to tune their gap depending on the number of layers allows for the detection of several wavelengths[300]. Overall, while graphene is suited for ultrafast, broadband technologies, TMDs are geared towards applications where strong light absorption[301] and electroluminescence[302] are required.

Although it is not expanded upon in this thesis for obvious concision purposes, graphene and other 2D materials hold strong potential for applications in plasmonics[303]–[306], antennas[307]–[310], light emitting devices[233], [234], [311] and more, and we refer the reader to the mentioned references for information and insight on these topics.

2.4.4 Sensors

Thanks to their one-atom thickness (or almost, in the case of TMDs) and their high flexibility, 2D materials are perfect for sensing applications. They could revolutionize this field and allow for cheap, reliable and flexible devices to be used in sensor arrays or as individual on-chip sensors. Because of their ultimate surface to body ratio, each atom that composes a 2D material is in direct contact with the environment of the sensor, which leads to an incredible degree of sensitivity[312] that is beneficial for all manner of sensing: mass[313], [314], electrochemical[315], [316], magnetic[312], radiation[317] and many more. For instance, nano-electro-mechanical sensors (NEMs) based on pristine graphene resonators, which measure the shift in resonance frequency depending on particle adsorption on the device, have been developed and an astonishing detection limit at 158 parts-per-quadrillion for gas molecules at room temperature was reported[318].

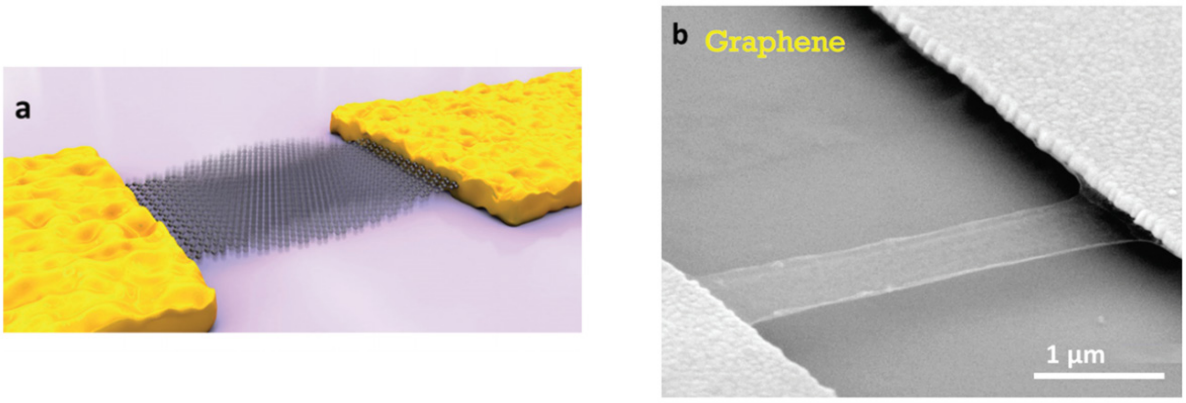


Figure 24. (a) Sketch of a resonating graphene sheet in action. (b) Actual graphene micro-resonator fabricated by SiO_2 etching[319].

Such technology could of course be used to monitor aerosol content in the atmosphere for instance. However, several challenges remain unsolved: while suspended graphene yields the most promising results, it is more difficult and far less stable than graphene on substrate, in which substrate interactions can diminish the sensing capabilities[53]; contamination by hydrocarbons is another issue that can drastically impact performance, and while it can be easily solved by UV light cleaning or annealing in a lab, it is a very real issue in real-world conditions. To remedy this, functionalization or passivation[320] may be required, but such techniques run the risk of undermining the sensing capabilities of the resonator. These types of challenges must therefore be addressed before graphene NEMs can become ubiquitous.

The use of graphene for magnetic sensing is also extremely promising. Current technologies are based on tunneling magnetoresistance and giant magnetoresistance, but are limited by spin-torque instabilities and thermal magnetic noise[321], and their use in the µT to the nT range is therefore severely limited. Graphene-based Hall sensors yielding a similar sensitivity to that of existing sensors have been reported[322], but sensors based on a combination of extraordinary magnetoresistance and spintronics were able to reach a sensitivity of 10mV/Oe [321], [323], which is larger than state of the art InAs 2DEG sensors of similar dimensions.

Once again, although graphene spearheads research into 2D materials for sensing applications, other materials, most notably TMDs are promising in this regard. Gas sensors based on MoS_2 have been reported as early as 1996[324], and, more recently, nitrous oxide sensors based both on single-layer MoS_2 and multi-layer MoS_2 have been realized[325]. These showed extremely high sensitivity, detecting nitrous oxide down to 0.8 parts-per-million; it is worth noting that, in this study, sensors based on 2, 3 and 4 layer MoS_2 were more stable and reliable than their single layer counterpart. Another MoS_2 based sensor using reduced graphene oxide as contacts was reported[326] to yield a sensitivity as low as 2 parts-per-billion, and its performance could be increased further by platinum functionalization. Even more recently, an MoS_2 sensor was used to detect DNA particles[327]; in this instance, the sensor has been modified with Au particles, which greatly enhances DNA absorption on MoS_2.

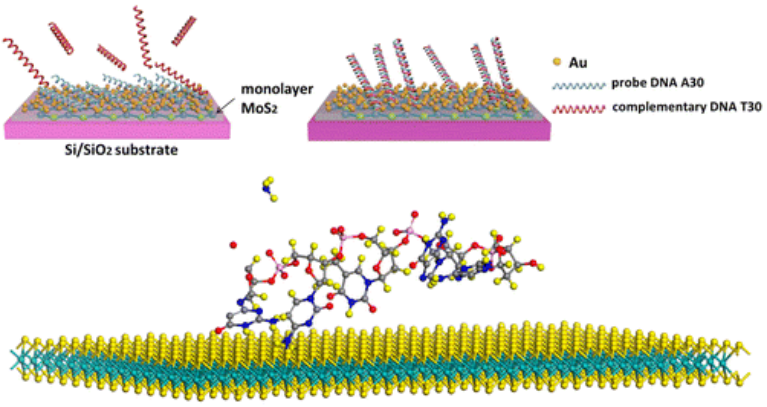


Figure 25. Au modified MoS_2 monolayer for DNA sensing [327].

2.4.5 Energy storage

Energy storage, as well as energy conversion, is yet another technological field in which the potential applications of 2D materials are plentiful. In the specific case of batteries, the biggest challenge is to find the best possible materials to be used as anode and cathode. Li-ion batteries are widely regarded as the most promising technology to be used in future utilities and electric vehicles for instance, and they are made up of an $LiCoO_2$ cathode and a graphite anode[328]–[330]. Due to its relatively low specific capacity (ampere-hours available at a given discharge value per unit weight) of 372 $mAh.g^{-1}$[331], graphite does not seem to be the ideal material for this use, but most other materials bearing a higher capacity (4200 $mAh.g^{-1}$ for Si for instance [332]) can only sustain a low number of charge/discharge cycles before their performance starts declining rapidly. Identifying the right materials is therefore a balancing act between several performance indicators, and 2D materials as well as nanostructures such as nanoporous materials[331], [333] could be of extremely high interest. Graphene has shown potential as a conductive additive to nanostructured electrodes[334], [335], while reduced graphene oxide sheets have shown great promise as electrodes, whether in their pristine form[336] or by creating composites with SnO_2[337], reaching capacities up to 780 $mAh.g^{-1}$ for instance[337]. Once again, TMDs are also very promising in this respect, the weak VdW forces binding the layers allowing for ion diffusion without a significant increase in volume[53]. Exfoliated then restacked MoS_2 has for example led to a specific capacity of over 800 $mAh.g^{-1}$[338], while layered G/MoS_2 composites material in which Li ions can be intercalated, leading to a high specific capacity of 1100 $mAh.g^{-1}$[339].

Supercapacitors could also benefit greatly from the advent of 2D materials. Their performance can be improved by increasing the surface area of the electrode while reducing its thickness, and one-atom thick, all-surface materials are a natural fit; strong electrochemical performance in graphene-based supercapacitors has been reported[340]–[343]. Other than pristine graphene, the use of several varieties of graphene oxide in supercapacitors, such as aerosol spray dried graphene oxide[344], microwave expanded graphite oxide[343], [345] and reduced graphene oxide[346] have been investigated and yielded promising results.

Graphene and other 2D materials have also found great interest hydrogen storage and fuel cells, which convert electrochemical energy into electrical energy as long as fuel and oxygen are available, and are used in vehicles, smart phones, and power backup systems for instance. 2D materials have been used to replace the costly noble metal alloys (Pt, Au ...) used in the cathode for the oxygen reduction reaction, and produced promising results [347], [348]. MoS_2 and WS_2, thanks to their edges acting as catalytic sites, could also replace those noble metals and have been studied for these purposes[349]. Graphene also holds potential for hydrogen storage thanks to its robustness and flexibility, allowing for the control of hydrogen intake via its curvature[350], [351], but also the production of hydrogen in a more renewable process than the one currently used[352], [353].

2.4.6 Flexible electronics

Through their ultimate thinness, their flexibility and incredibly high resistance to strain, 2D materials will enable the advent of flexible electronics, widely considered to be the next ubiquitous platform for the electronics industry[354]; the ultimate goal being to create devices with performance equal to or higher than regular current electronic devices, but in a foldable, transparent and lightweight format by which many new applications would be made possible. Important technological challenges remain however, such as ensuring that all components yield acceptable performance under high deformation and are environmentally sound. A complete revolution of the current low-cost, high output manufacturing processes used will also be necessary before "printable" flexible electronics reach ubiquity, which is a tall order.

As is the case for most applications, graphene is the most promising 2D material for such applications. Its one-atom thickness, high flexibility, transparency and extremely high conductivity[118] make it an ideal candidate to be used in the core components of devices such as antennas, interconnects, RF transistors, and LEDs; many other applications are envisioned, such as flexible displays[355]–[357], flexible chemical sensors[358]–[360], flexible batteries and other energy storage devices[361]–[364].

Before that, however, the properties of graphene will need to be properly tuned depending on the intended application: for instance, a very low resistivity of $< 5\ \Omega/m$ is required for high frequency applications in antennas[365], while a resistivity of a couple hundred Ω/m would be sufficient for capacitive touch panels[366]. Graphene resistivity is highly dependent on the deposition technique used though[53], which will be a major challenge to be overcome in order to reach the easily "printable" flexible electronics that would revolutionize the industry.

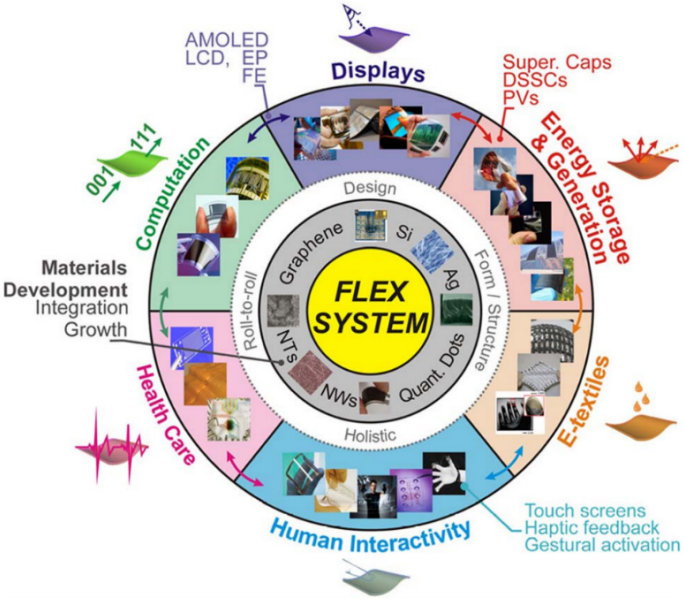


Figure 26. Possible applications of flexible electronics, and the 2D materials and techniques that enable them [354].

However, the prospects offered by graphene are extremely enticing and will without a doubt motivate the industry to develop the necessary techniques and processes to usher society in a world of flexible electronics. Due to its over 90% transmittance in the 200 to 900nm range, graphene has incredible potential as a transparent conductive material; this property could be put to use in solar cells for instance, which exhibit a 10 to 25% power loss originating from the currently used transparent conductive layer[367]. In a similar fashion, graphene has strong potential as anode material in flexible OLED panels[368], solving many issues related to the currently used indium tin oxide (ITO is brittle, indium diffusion impacts performance over time ...). Human-computer interaction is another field that could benefit greatly from 2D materials: experimentally realized transparent and flexible graphene actuators[369] indicate that graphene could enable precise haptic feedback in capacitive touch screens, which are arguably the main way we interact with computers nowadays.
Other 2D materials, such as h-BN or TMDs (namely MoS_2) hold potential for flexible electronics applications. Graphene/h-BN heterostructures have been shown[370] to enhance GFET performance, and could therefore be used to create flexible GFETs; in a similar way, using h-BN instead of Al_2O_3 as a top gate oxide in MoS_2 devices could allow for flexible, TMD based FETs. Thanks to their direct band-gap, TMDs such as MoS_2 and WS_2 are very promising for optoelectronics and photovoltaics, and could therefore be used to create novel, flexible optoelectronic devices[53].

While not intended to be all-encompassing, this section provided comprehensive examples of current and future potential applications for various 2D materials. The techniques used to deposit and grow these materials will now be briefly presented, as they are a fundamental part in realizing the full potential of these materials and bringing the aforementioned applications to life.

2.5 Brief overview of 2D materials synthesis

Growth and deposition techniques, more specifically at an extremely large scale, are the cornerstone of the previously outlined applications for 2D materials. The development of scalable processes that would allow for the specific tuning of electronic, mechanical and structural properties of those materials would obviously be a huge step towards the realization of those applications. In this section, I will briefly present the main techniques used to synthesize 2D materials, in order to give an overview of this technological side of the field. Once again, the reader is referred to the mentioned references for more precise and detailed information on the mentioned techniques.
Two main classes of synthesis techniques can be distinguished: top-down deposition (via mechanical or liquid-phase exfoliation for instance) and bottom-up growth (via chemical vapor deposition or molecular beam epitaxy).

2.5.1 Mechanical and Liquid-Phase Exfoliation

Mechanical exfoliation, also known as the "scotch-tape" method, was the very first technique used to obtain monolayer graphene in 2004 by Geim and Novoselov[93]. Due to the weakness of the van der Waals forces than bind the individual layers of 2D materials in their bulk/3D form, a strong enough force can cleave either a single or several layers of the considered material. Thanks to its simplicity and flexibility, mechanical exfoliation has been used extensively to produce single and multi-layers for a variety of materials ranging from graphene[371]–[375] to TMDs[372], [375]–[377], but also h-BN[375], [378], [379]. As a well-established technique, mechanical exfoliation can provide high quality layers of high purity and of which the size is only limited by that of the starting material[380]. Mechanical exfoliation has for instance been used to produce extremely high quality single layer graphene which was reported to yield a 10^7 $cm^2.V^{-1}.s^{-1}$ carrier mobility at 25 K[381]. However, by its very nature, mechanical exfoliation is not a scalable method and its use is therefore mostly limited to the production of laboratory samples.

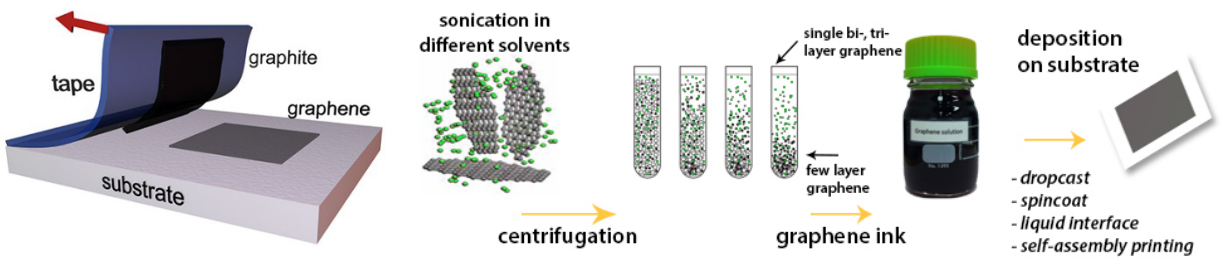


Figure 27. Left: Mechanical Exfoliation. Right: Liquid-Phase Exfoliation [382].

Liquid Phase Exfoliation (LPE) is another widely used method to produce single or multi-layers of 2D materials. First, the bulk material is dispersed in a solvent (N-methyl-2-pyrrodilone is frequently used) using sonication, then the mixture undergoes centrifugation in order to disperse the layers and arrange them in the solvent (single layers at the top, many-layers at the bottom). The concentration of single and few layer compounds depend on the solvent used and can be increased[383], [384] via the use of a surfactant prior to sonication, but chemical treatments are then needed to remove it.
From the resulting solution, 2d material "inks" can be produced, and can then be deposited via drop and dip casting[385], [386], spray-coating, ink-jet printing[387] and other techniques. Graphene inks with carrier mobilities up to 90 $cm^2.V^{-1}.s^{-1}$ have for instance been reported[387].
LPE is cheap and relatively scalable, and, contrary to some other techniques, does not rely on growth substrates. However, the size of LPE flakes is limited by the intense exfoliation and purification processes: the area of LPE-produced, single layer graphene flakes rarely exceeds $1\mu m^2$ [383], [384], [387] for instance.
LPE has been used to produce graphene[383], [384], [388], [389], TMDs such as MoS_2, WS_2, $MoSe_2$ and $MoTe_2$[390]–[392] as well as h-BN[390]–[392].

2.5.2 Molecular Beam Epitaxy

Molecular beam epitaxy (MBE) is an epitaxy technique performed in ultra-high vacuum (10^{-8} to 10^{-12} Torr). It has been widely used to create epitaxial layers of semiconductors, metals and insulators, and allows for a high degree of control over both doping profile and chemical composition[393], [394]. Due to the high vacuum required and the long deposition times, MBE is more suited for deposition on 2 to 6 inch wafers than on 30-inch ones for instance [395]. This technique allows for precise control over the number of layers deposited, and has been used to deposit graphene on a wide range of subtrates including but not limited to h-BN[396], Si(111)[397], SiC[398] or dielectric substrates[399]. MBE-grown TMDs, mainly $MoSe_2$[400]–[402], WSe_2[220], [403], $MoTe_2$[404] and WTe_2 [405] have also been reported, as well as MBE grown h-BN[406], [407].

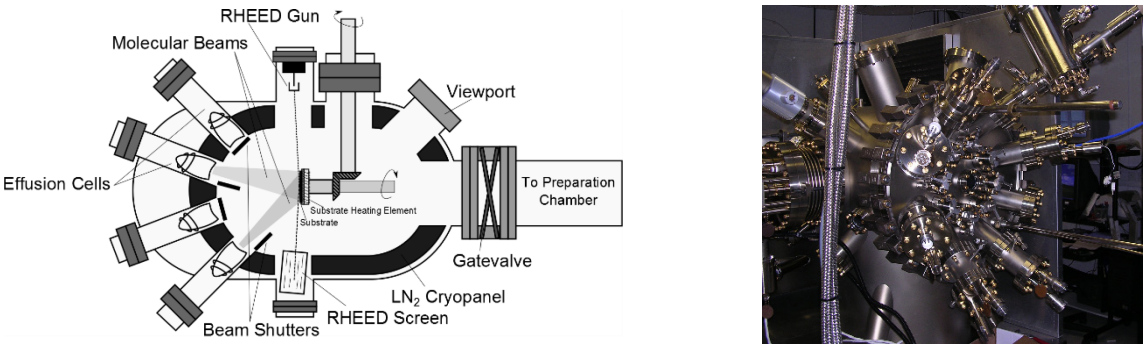


Figure 28. Left: MBE operation sketch. Right: MBE experimental setup[408].

MBE-growth of both silicene[159], [160], [409]–[411] and germanene[168], [412] on specific metallic substrates has been reported, and allows for further investigation of the properties of these relatively new 2D materials.

2.5.3 Chemical Vapor Deposition

Chemical Vapor Deposition (CVD) is the most widely used technique to deposit thin films, and has been the cornerstone for semiconductor based devices for decades[413]. It is extremely versatile, as it allows for the deposition of either crystalline or amorphous films from gaseous, solid or liquid precursors. Many specific types of CVD exist, such as plasma-enhanced CVD (PECVD), cold/hot wall CVD and many more, and the selection of the type to be used is dictated by the deposited material.
Graphene CVD is versatile and can be performed by many techniques (thermal-CVD, PECVD ...), and from a variety of precursors (liquid, gaseous or solid), and the first report of the deposition of large area graphene (cm^2) dates back to 2009[414]. Many other reports have followed since[415]–[418], and high quality graphene films were deposited on a wide variety of substrates with carrier mobilities up to 30 000 $cm^2.V^{-1}.s^{-1}$. Another advantage of CVD is that it allows for the deposition of extremely large quantities of high quality material; deposition of 50 cm graphene films with carrier mobilities around 10^4 $cm^2.V^{-1}.s^{-1}$ has been reported[395]. CVD has also been used to deposit other 2D materials, namely TMDs: deposition of MoS_2 [390], [419], $MoSe_2$ [218], $MoTe_2$[219], [420], WS_2[421], WSe_2[421], [422] and WTe_2[221], [423] on various substrates has been reported.

Due to its extreme versatility and its ability to deposit large surfaces, CVD is the most prominently used deposition technique for large scale production of thin films and 2D materials.

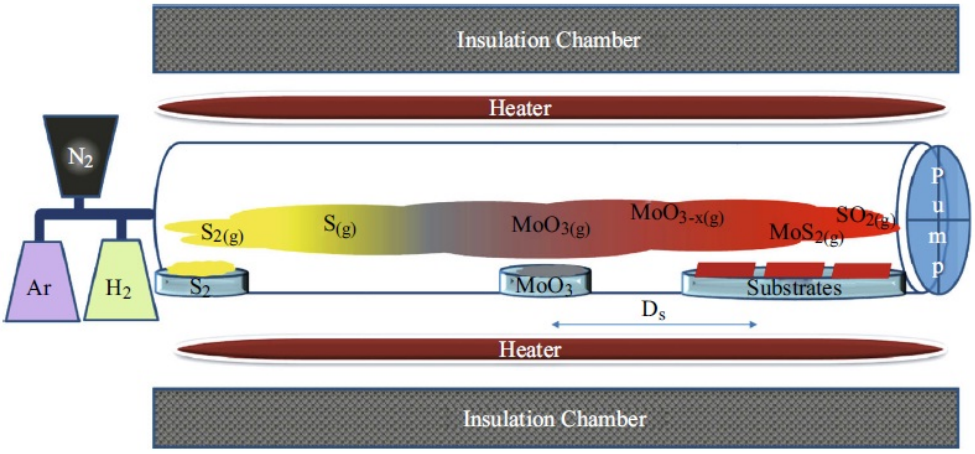


Figure 29. Deposition of MoS_2 flakes via CVD[424].

2.5.4 Thermal decomposition of SiC

Graphene growth by thermal decomposition of silicon carbide is another technique that holds potential and attracts a lot of interest. By annealing either the Si-face (0001) or the C face $(000\bar{1})$ of hexagonal SiC the silicon atoms evaporate, leaving behind a reconstructed graphene layer on top of a semiconducting SiC substrate. The resulting graphene is therefore ready for electronic applications and does not need to be transferred onto another substrate, as is the case with several other techniques.
The thermal decomposition of bulk SiC at extremely high temperatures (>2000°C) was originally reported in 1965[425], and was expanded upon and enhanced (800°C in UHV) roughly a decade later[426]. Although the graphene produced by this method yielded satisfactory electronic properties[427], it was composed of small grains (from 30 to 200 nm) of varying thickness[428], [429] and was therefore not usable for industrial applications. Since then however, the process has been refined[430]–[432]: by annealing SiC at specific temperatures and in an argon or hydrogen environment, the evaporation rate of silicon is reduced, favoring more precise graphene reconstruction. Graphene samples obtained by similar techniques have shown domains as large as 50×50 µm[433], and in some cases, extremely high electronic mobilities (>11 000 $cm^2.V^{-1}.s^{-1}$)[431].
However, the use of bulk, hexagonal SiC limits wafer sizes and cost and hinders wide machining processes. The use of cubic silicon carbide (3C-SiC) (which can be grown on top or regular silicon vie MBE) as a substrate for graphene growth could help overcome these limitations[434]–[436], and has been widely investigated for several years[437]–[439].

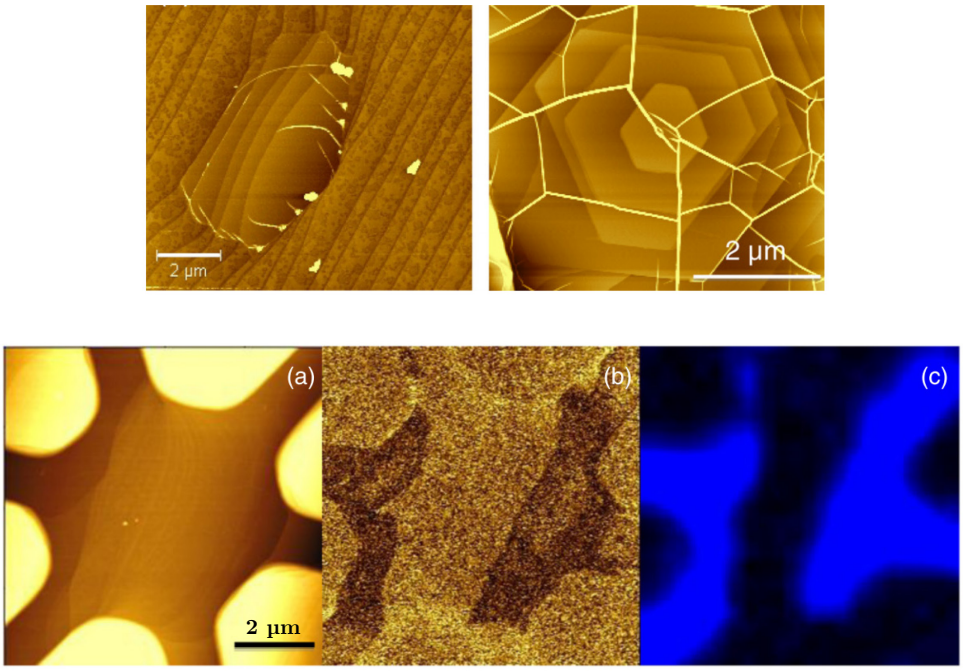


Figure 30. Top: AFM images of graphene on the $(000\bar{1})$ face of SiC. Bottom: (a)AFM topology map, (b)EFM amplitude scan and (c)Raman 2D band intensity map of monolayer graphene growth on a pre-patterned $(000\bar{1})$ face of SiC [440].

Several other graphene production techniques have been developed, such as growth on metals by precipitation[441] for instance, but are not detailed here as this short rundown focused on the main deposition techniques for graphene and other 2D materials.

Now that general nanoelectronics and the scaling issues they face as well as some 2D materials that could potentially bring part of a solution have been introduced, I will present the models and methods used to perform my PhD work.

Chapter 3

Physical models used

In this section, I will introduce the theoretical models and approaches I used to investigate the potential TMDs hold for nanoelectronic applications.
First, I will present the Tight-Binding (TB) method, which is the approach used in this work to model the materials themselves as well as their electronic properties. A short introduction on the theory of the TB method will be given, before delving into the actual TB model I used to simulate the considered TMDs, as well as the modifications and adaptations I made upon this model for our quantum transport computation needs.

I will then give some insight on the non-equilibrium Green's function (NEGF) method that was used to model electronic transport through the nanodevices investigated. A short introduction on this method will be presented, followed by information on the implementation of this theoretical framework in our transport code.

3.1 Tight-binding formalism

3.1.1 Theoretical overview

Many different approaches can be used to model materials and their electronic properties, and the selection of the correct approach based on the system studied is paramount. Density Function Theory (DFT) for instance, as a true ab-initio method, is well-suited for investigating and predicting features such as the band structure of a small set of atoms; it however cannot be used for larger structures containing thousands of atoms such as transistors and other devices. For such systems, simplified and approximated methods referred to as semi-empirical methods are required. These include the tight-binding approach, empirical pseudo-potential approaches, or the use of k.p Hamiltonians for instance.

Based on the LCAO (linear combination of atomic orbitals) method introduced in 1928 by Finklestein and Horowitz[442], the tight-binding method was introduced by Slater and Koster in 1954[443] as a tool to calculate the band structure of solids.

In this theoretical overview, I will very briefly introduce the theory and the concepts necessary to the understanding of the TB model used and developed over the course of my PhD. Far more in-depth and complete information, as well as examples, can be found in the following references[444]–[449].
As its name suggests, the TB approach considers the electrons to be tightly-bound to their respective atoms. As such, a general set of wave functions can be deduced from the superposition of the wave functions located on each atom, assuming they interact in a limited capacity with surrounding atoms and potentials. The overall Hamiltonian of the structure at position $\vec{r}$ can therefore be approximated by the sum of all atomic Hamiltonians H_{at} of the n atoms located at $\overrightarrow{R_n}$, along with the interaction potential between the atoms ΔU. (In order to improve notation readability, only one orbital per atom is considered in this example)

$$H(\vec{r}) = \sum_n H_{at}\left(\vec{r} - \overrightarrow{R_n}\right) + \Delta U(\vec{r}) \tag{7}$$

The eigenfunction $\psi(\vec{r})$ to this Hamiltonian is the solution to the time-independent Schrödinger's equation

$$H(\vec{r})\psi(\vec{r}) = E\psi(\vec{r}) \tag{8}$$

and can therefore be expressed as a superposition of individual atomic wave functions $\varphi(\vec{r} - \overrightarrow{R_n})$, and calculated as a linear combination of the atomic orbitals.

$$\psi(\vec{r}) = \sum_n d\left(\overrightarrow{R_n}\right)\varphi\left(\vec{r} - \overrightarrow{R_n}\right) \tag{9}$$

By combining Eqs.(9) and (8) we can obtain Eq.(10) which, when multiplied by $\varphi^*\left(\vec{r} - \overrightarrow{R_m}\right)$ and integrated over real space, leads to eqs(11) and (12).

$$H(\vec{r}) \sum_n d\left(\overrightarrow{R_n}\right)\varphi\left(\vec{r} - \overrightarrow{R_n}\right) = E \sum_n d_l\left(\overrightarrow{R_n}\right)\varphi\left(\vec{r} - \overrightarrow{R_n}\right) \tag{10}$$

$$\sum_n \int d\vec{r}\left(\varphi^*\left(\vec{r} - \overrightarrow{R_m}\right)H(\vec{r})\varphi\left(\vec{r} - \overrightarrow{R_n}\right)\right) d\left(\overrightarrow{R_n}\right) = E \sum_n \int d\vec{r}\left(\varphi^*\left(\vec{r} - \overrightarrow{R_m}\right)\varphi\left(\vec{r} - \overrightarrow{R_n}\right)\right) d\left(\overrightarrow{R_n}\right) \tag{11}$$

$$\sum_n h_{mn}\, d\left(\overrightarrow{R_n}\right) = E \sum_n s_{mn}\, d\left(\overrightarrow{R_n}\right) \tag{12}$$

In Eq.(12), h_{mn} is an element of the Hamiltonian matrix, and s_{mn} is the overlap between the m and n atomic orbitals.

By replacing $H(\vec{r})$ by Eq.(8) in h_{mn}, this matrix element can be decomposed as

$$h_{mn} = \int d\vec{r}\varphi^*\left(\vec{r} - \overrightarrow{R_m}\right)\left[\sum_k H_{at}\left(\vec{r} - \overrightarrow{R_k}\right) + \Delta U(\vec{r})\right]\varphi\left(\vec{r} - \overrightarrow{R_n}\right) \tag{13}$$

$$\leftrightarrow \sum_k \int d\vec{r}\varphi^*\left(\vec{r} - \overrightarrow{R_m}\right)H_{at}\left(\vec{r} - \overrightarrow{R_k}\right)\varphi\left(\vec{r} - \overrightarrow{R_n}\right) + \int d\vec{r}\varphi^*\left(\vec{r} - \overrightarrow{R_m}\right)\Delta U(\vec{r})\varphi\left(\vec{r} - \overrightarrow{R_n}\right) \tag{14}$$

$$\leftrightarrow \sum_k \int d\vec{r}\varphi^*\left(\vec{r} - \overrightarrow{R_m}\right)\varepsilon_k\delta_{kn}\varphi\left(\vec{r} - \overrightarrow{R_n}\right) + \int d\vec{r}\varphi^*\left(\vec{r} - \overrightarrow{R_m}\right)\Delta U(\vec{r})\varphi\left(\vec{r} - \overrightarrow{R_n}\right) \tag{15}$$

in which δ_{kn} is the Kronecker delta, i.e $\delta_{kn} = 1$ if $k = n$ and 0 otherwise.
Therefore, the h_{mn} Hamiltonian matrix element is finally

$$h_{mn} = \varepsilon_n \int d\vec{r}\varphi^*\left(\vec{r} - \overrightarrow{R_m}\right)\varphi\left(\vec{r} - \overrightarrow{R_n}\right) + \int d\vec{r}\varphi^*\left(\vec{r} - \overrightarrow{R_m}\right)\Delta U(\vec{r})\varphi\left(\vec{r} - \overrightarrow{R_n}\right) \tag{16}$$

$$h_{mn} = \varepsilon_n . s_{mn} + t_{mn} \tag{17}$$

In this expression of the matrix element, ε_n is called the on-site energy and represents the energy of the atomic orbital of the n-th atom in vacuum, without taking the neighboring orbitals into account; on the contrary, t_{mn} represents the coupling between the atomic orbitals found on the m-th and n-th atom and is often referred to as the hopping integral. In the case where several orbitals are considered on each atom, each orbital is categorized by an on-site energy as well as couplings to every other orbital, including those located on the same atom.

In practice, a tight-binding Hamiltonian is an N×N matrix, where N is the number of orbitals in the considered system (in the case of a periodic system, N is the number of orbitals in the unit cell to be repeated). Diagonal elements of this matrix contain the on-site energies, while off-diagonal elements contain the hopping elements between the corresponding orbitals.
As an example, the creation of the TB Hamiltonian for a 2D infinite graphene sheet is shown over the next few pages, and used to calculate the band structure of the system.

3.1.2 Building a TB Hamiltonian for graphene

For this example, we will investigate a 2D infinite graphene sheet as shown in Figure 31 a) (periodic along the x and y axes), and apply a very simple tight-binding model in which we consider a single orbital per atom, and only first-neighbor coupling. Many different unit cells can be used to reduce the size of this system, and we chose the one shown in Figure 31 b) that contains 4 atoms, and therefore 4 orbitals.

The resulting tight-binding Hamiltonian is therefore the following 4×4 matrix

$$H_0 = \begin{bmatrix} \varepsilon_A & t_{AB} & t_{AC} & t_{AD} \\ t_{BA} & \varepsilon_B & t_{BC} & t_{BD} \\ t_{CA} & t_{CB} & \varepsilon_C & t_{CD} \\ t_{DA} & t_{DB} & t_{DC} & \varepsilon_D \end{bmatrix}$$

Since we only consider first-neighbor coupling, it can be simplified to

$$H_0 = \begin{bmatrix} \varepsilon_A & t_{AB} & 0 & 0 \\ t_{BA} & \varepsilon_B & t_{BC} & 0 \\ 0 & t_{CB} & \varepsilon_C & t_{CD} \\ 0 & 0 & t_{DC} & \varepsilon_D \end{bmatrix}$$

This matrix describes all orbital interactions in the unit cell of the system, but is not sufficient to fully describe the material.

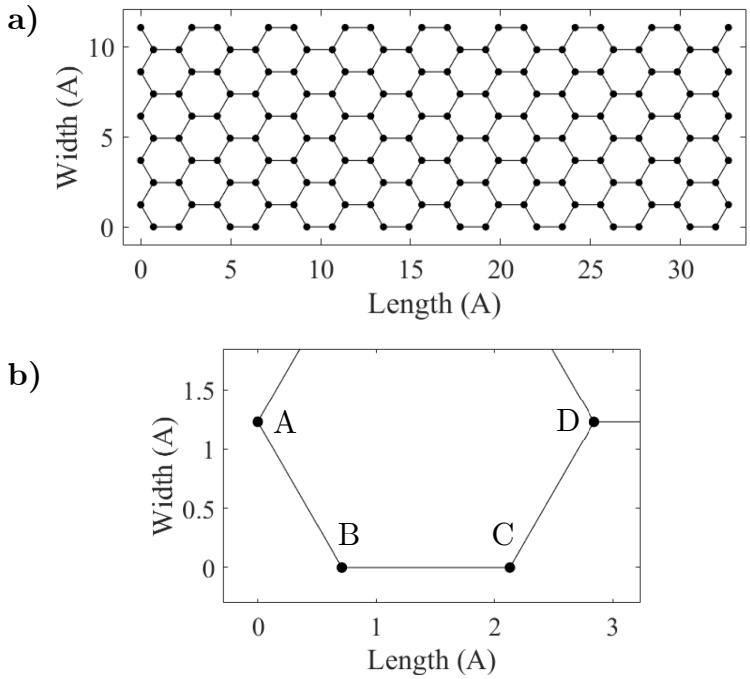


Figure 31. a) 2D infinite graphene sheet (periodic along x and y).
b) Unit cell used in this example, and naming convention for the atoms.

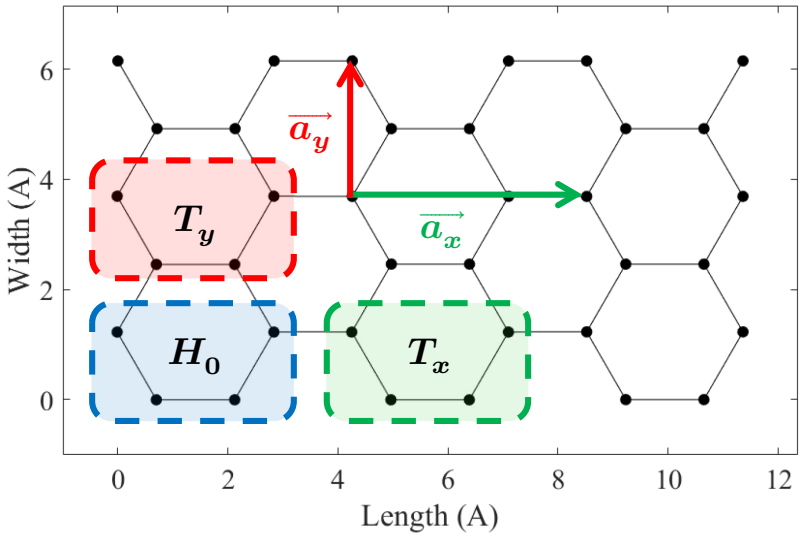


Figure 32. Representation of the unit vectors and neighboring unit cells

In order to compute the bandstructure of a 2D infinite graphene sheet, we have to take periodicity into account. The unit vectors used to reproduce a 2D infinite sheet from the chosen unit cell are $\overrightarrow{a_x}$ and $\overrightarrow{a_y}$ as shown in Figure 32 ($a_c = 2.46$ Å is the graphene lattice constant)

$$\overrightarrow{a_x} = \begin{pmatrix} \sqrt{3}a_c \\ 0 \end{pmatrix} \qquad \overrightarrow{a_y} = \begin{pmatrix} 0 \\ a_c \end{pmatrix}$$

We must now create Hamiltonians describing the coupling of the unit cell with the neighboring cells, as shown in Figure 32:

- T_x describes the coupling between the blue unit cell and the green one, which are connected by $\overrightarrow{a_x}$
- T_y describes the coupling between the blue unit cell and the red one, which are connected by $\overrightarrow{a_y}$

These coupling Hamiltonians will therefore be the following 4×4 matrices

$$T_x = \begin{bmatrix} t_{A_0A_x} & t_{A_0B_x} & t_{A_0C_x} & t_{A_0D_x} \\ t_{B_0A_x} & t_{B_0B_x} & t_{B_0C_x} & t_{B_0D_x} \\ t_{C_0A_x} & t_{C_0B_x} & t_{C_0C_x} & t_{C_0D_x} \\ t_{D_0A_x} & t_{D_0B_x} & t_{D_0C_x} & t_{D_0D_x} \end{bmatrix} \qquad T_y = \begin{bmatrix} t_{A_0A_y} & t_{A_0B_y} & t_{A_0C_y} & t_{A_0D_y} \\ t_{B_0A_y} & t_{B_0B_y} & t_{B_0C_y} & t_{B_0D_y} \\ t_{C_0A_y} & t_{C_0B_y} & t_{C_0C_y} & t_{C_0D_y} \\ t_{D_0A_y} & t_{D_0B_y} & t_{D_0C_y} & t_{D_0D_y} \end{bmatrix}$$

in which $t_{M_0N_x}$ ($t_{M_0N_y}$)is the coupling between the M atom of the blue unit cell and the N atom of the green (red) unit cell.

By looking at the atomic arrangement of the structure(Figure 32), we can easily eliminate all couplings beyond the first neighbor

$$T_x = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ t_{D_0A_x} & 0 & 0 & 0 \end{bmatrix} \qquad T_y = \begin{bmatrix} 0 & t_{A_0B_y} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & t_{D_0C_y} & 0 \end{bmatrix}$$

In the end, we therefore have 3 tight-binding Hamiltonians that describe the whole system. In most simple graphene TB models, the on-site energies are set to 0 eV and the first neighbor hopping parameters t_G to -2.7 eV.

$$H_0 = \begin{bmatrix} 0 & t_G & 0 & 0 \\ t_G & 0 & t_G & 0 \\ 0 & t_G & 0 & t_G \\ 0 & 0 & t_G & 0 \end{bmatrix} \qquad T_x = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ t_G & 0 & 0 & 0 \end{bmatrix} \qquad T_y = \begin{bmatrix} 0 & t_G & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & t_G & 0 \end{bmatrix}$$

The bandstructure at a given wave vector (k_x, k_y) can now be calculated as the eigenvalues of the following H_{tot} matrix

$$H_{tot} = H_0 + T_x . e^{ik_x . |\overrightarrow{a_x}|} + {T_x}^\dagger . e^{-ik_x . |\overrightarrow{a_x}|} + T_y . e^{ik_y . |\overrightarrow{a_y}|} + {T_y}^\dagger . e^{-ik_y . |\overrightarrow{a_y}|}$$

$$H_{tot} = t_G \begin{bmatrix} 0 & 1 + e^{ik_y . |\overrightarrow{a_y}|} & 0 & e^{-ik_x . |\overrightarrow{a_x}|} \\ 1 + e^{-ik_y . |\overrightarrow{a_y}|} & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 + e^{-ik_y . |\overrightarrow{a_y}|} \\ e^{ik_x . |\overrightarrow{a_x}|} & 0 & 1 + e^{ik_y . |\overrightarrow{a_y}|} & 0 \end{bmatrix}$$

Because the unit cell chosen contains 4 atoms, the basis contains 4 orbitals and therefore 4 eigenvalues will be obtained for each given wave vector (k_x, k_y).
The resulting bandstructure projected along k_x, k_y as well as in 3D is shown in Figure 33.

As this simple example has shown, building a TB Hamiltonian is a matter of carefully selecting the unit cell and therefore the unit vectors that come with it. Then, we simply need to fill out the Hamiltonian matrices depending on the position of the considered orbitals, and calculate the total Hamiltonian for sets of wave vectors (k_x, k_y).

Evidently, as the investigated system gets more complicated and the basis gets bigger (considering several orbitals per atom for instance, as well as second or even third neighbor coupling), the creation of the matrices gets more complicated and requires careful consideration and observation.

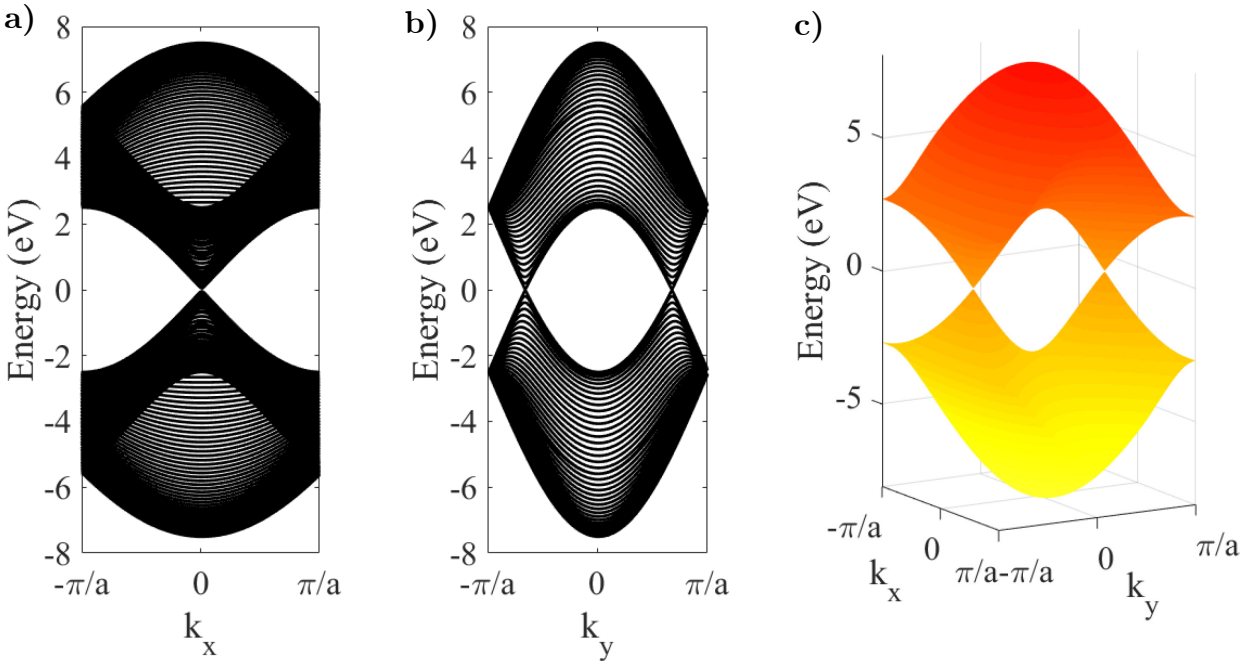


Figure 33. Bandstructure of a 2D infinite graphene sheet projected along k_x (a), k_y (b) and in 3D (c).

Finding and selecting a TB model in the literature with information on the on-site energies and coupling parameters in the desired material is of course required. Most TB models are fitted onto DFT bandstructures and aim for accuracy around the band gap.

Now that I have quickly introduced the underlying theory of the tight-binding formalism and shown how to build tight-binding Hamiltonians, I will present the TB model I used for TMDs.
Although I had to modify it in order to use it in our transport calculations, it is important to introduce the model in its original form to present a clear picture of the theoretical approach to material modelling used in this work.

3.1.3 Base TB model used for TMDs

The TB model used was developed by Fang et al. and is detailed in [1]. I will briefly introduce its features and parameters here, but I refer the reader to the original paper for much more in-depth information and insight about this model. Some paragraphs are cited directly from the original paper, and will be clearly marked as quotations.

This tight-binding model is based on the Wannier transformation of ab-initio DFT calculations, and takes into account the effect of strain in the limit of a slowly varying in-plane strain field. Although the model is applicable to graphene and hBN as well as TMDs, our interest lies solely with the latter.

Before we get to the TMD model itself, I will cite the article to convey some general information about the construction of the model and the way strain is handled.

As a summary of the work presented, the original paper states:

Here we generalize the Wannier method to monolayers with in-plane strain and derive the relevant models, compatible with the underlying crystal symmetry. In increasing order of complexity with the underlying orbital content, we construct such tight-binding models for graphene, hexagonal boron nitride (hBN) and four TMDCs. These models are valid in the presence of slowly-varying in-plane strain field, providing the electronic coupling to long-wavelength in-plane acoustic phonon modes. We also derive the corresponding effective low-energy theories coupled with the strain field, consistent with the effective models derived from the principles of symmetry group representations, which by itself can identify all symmetry-allowed terms but is insufficient to provide estimates for the values of the coupling constants involved. Our ab initio Wannier tight binding approach thus complements the powerful symmetry group analysis, gives accurate values of the parameters in the model, and empowers calculations of large-scale structures of strained materials.

Detailing the way strain is modelled, Fang et. al state

The slowly varying in-plane strain field can be described by the displacement deformation vector field $u = (u_x(x,y), u_y(x,y)$. *The coordinates* x *and* y *denote the undistorted crystal coordinate, which is mapped to the new position* $(x + u_x(x,y), y + u_y(x,y))$ *in space. Since a constant displacement field introduces no physical changes to the layers, the strain field is characterized by the derivative of* u, *defined in tensor form*

$$u_{ij} = (\partial_i u_j + \partial_j u_i)/2$$

where $i, j = x, y$ *. This second rank tensor can be decomposed in the trace scalar part* $(u_{xx} + u_{yy})$, *and the doublet* $(u_{xx} - u_{yy}, -2u_{xy})$ *which forms a two-dimensional irreducible representation of the* C_{3v} *symmetry group of the crystal. There is also a rotational piece,* $\omega_{xy}, = \partial_x u_y - \partial_y u_x$ *which we take* $\omega_{xy} = 0$ *by choosing the proper set of coordinates.*
We can further simplify the modeling by applying the local density approximation to the strain effects, that is, by assuming locally the tight-binding parameters are approximated by the strained periodic crystal with constant u_{ij}. *In the following, these strain model parameters are extracted from the Wannier transformation of DFT calculations with periodic unit cells for the uniformly strained crystals. A structure with non-uniform strain can be modeled by combining these local-strain tight-binding parameters which have only long-wavelength variations compared to the lattice constants. The key steps in constructing these microscopic Hamiltonians are:*

(i) In linear elastic theory, the deformed microscopic displacement vector $v' = (v_x', v_y', v_z')$ *between atomic sites is*

$$\begin{aligned} v_x' &= v_x + v_x \partial_x u_x + v_y \partial_y u_x \\ v_y' &= v_y + v_x \partial_x u_y + v_y \partial_y u_y \\ v_z' &= v_z \end{aligned} \tag{A1}$$

with $v = (v_x, v_y, v_z)$ *the unstrained vector.*

Though these relations hold for the primitive lattice vectors, strictly speaking this approximation, the Cauchy-Born rule, is only valid for a Bravais lattice with a single atom basis. For a strained primitive unit cell with multiple basis atoms, the relative position or orientation of these atoms varies, in addition to the relations prescribed by Eq.(A1). For example, in layered materials such as phosphorene, TMDCs and puckered graphene-like materials, there is a height variation in the position of individual atoms under strain./.../We include the height corrections for the chalcogen atoms in TMDCs by generalizing the above Cauchy-Born approximation.

(ii) To incorporate the strain effects in the tight-binding Hamiltonians, the hopping integral between orbitals on different sites is assumed to scale with the pair distance, known as the central force approximation. Up to leading order linear response, the strained hopping integral can be approximated as

$$t'_{\alpha\beta} = t^0_{\alpha\beta} + \mu\delta_{\alpha\beta}.(\delta_{\alpha\beta}.\Delta).u \qquad \mu = \frac{1}{|\delta_{\alpha\beta}|}\frac{dt_{\alpha\beta}}{d|\delta_{\alpha\beta}|} \tag{A2}$$

Some empirical models go beyond the linear order by proposing a functional form which depends on the pair distance, such as exponential functions or algebraic functions of $|r|$. For the orbitals that are not s-like, the hopping integrals within the two-center Slater-Koster approximation can be decomposed into various channels related to the angular momentum projection, such as the σ and π bonds in p-p orbital coupling. The scaling can be applied to each channel as a function of pair distance. In general, the scaling of the hopping integral reflects the shapes of the orbitals and the changes in the crystal field potential. These translate into more involved forms of scaling beyond merely the pair distance dependence. For example, if the crystal is stretched along a direction that is perpendicular to the bond, the central force approximation would dictate no change for the hopping, which is not accurate. Here, we derive the models up to linear order in the strain and beyond the central force approximation. All the terms that couple $(u_{xx}+u_{yy})$, $(u_{xx}-u_{yy})$ and u_{xy} are retained in the Hamiltonian, and their forms are constrained by the underlying crystal symmetry. Thus, the hoppings along a bond acquire corrections when the crystal is stretched along the perpendicular direction to the bond, which captures the local environment change. Many layered materials involve orbitals beyond s-like ones, and have a more complicated geometry for atomic configurations and relative orientations.

(iii) Treatments of strain effects on tight-binding Hamiltonians typically involve only the scaling of hopping terms and neglect the variations for on-site energy terms. The on-site energy variations will be relevant for a layer with non-uniform strain field, also called the deformation potential. We extract the relevant potential information and work function from DFT calculations and define the energy reference point to be zero at the vacuum level outside the layer. In experiments, the presence of a substrate or encapsulating layers, and the charge redistribution in the layer with non-uniform strain result in further modification of the electrostatic environment, the screening for interactions and hence of the onsite terms.

In practice, the displacements $(u_{xx}+u_{yy})$, $(u_{xx}-u_{yy})$ and $(-2u_{xy})$ act as modifiers when properly building the tight-binding Hamiltonian matrices.

The TMD model takes into account the five d orbitals of the metal atoms and the three p orbitals of the chalcogen atoms. Since the TMD unit cell is MX_2, this results in a $5+3\times 2=11$ orbital basis, which in turn results in seven valence bands and four conduction bands in the obtained band structure.

In this 11 orbital basis, the orbitals are grouped in four sectors (A, B, C, D) and classified as odd (o) or even (e) with respect to an xy mirror plane symmetry as follows

$$\Psi_A{}^{(o)} = \begin{pmatrix} \phi_x = d_{xz} \\ \phi_y = d_{yz} \end{pmatrix} \qquad \Psi_B{}^{(o)} = \begin{pmatrix} \phi_x = p_x \\ \phi_y = p_y \\ \phi_z = p_z \end{pmatrix}$$

$$\Psi_C{}^{(e)} = \begin{pmatrix} \phi_x = d_{xy} \\ \phi_y = d_{x^2-y^2} \\ \phi_z = d_{z^2} \end{pmatrix} \qquad \Psi_D{}^{(e)} = \begin{pmatrix} \phi_x = p_x \\ \phi_y = p_y \\ \phi_z = p_z \end{pmatrix}$$

The coupling matrices that will be used to create the total Hamiltonian couple these sectors, and are therefore 3×3, 2×3, 3×2 or 2×2 matrices (depending on whether the A sector is involved) and are

$$\langle \Psi_i | H | \Psi_j \rangle = \begin{bmatrix} H_{xx} & H_{xy} & H_{xz} \\ H_{yx} & H_{yy} & H_{yz} \\ H_{zx} & H_{zy} & H_{zz} \end{bmatrix}$$

where $H_{mn} = \langle \phi_m{}^i | H | \phi_n{}^j \rangle$.

Thanks to the three-fold symmetry of the hexagonal lattice of TMDs (see Figure 34), the number of necessary parameters is greatly reduced and only a third of the matrices are given here (from which the rest can be derived through a rotation operation).

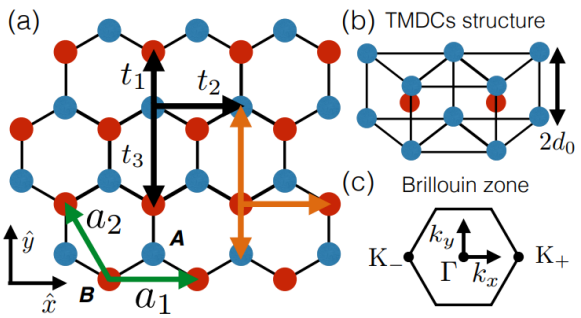


Figure 34. a) Top view of the TMD lattice in which the orange arrows represent the couplings for which matrices are given here (black arrows relate to hBN and graphene). b) Side view of a TMD. c) First Brillouin zone in the momentum space [1]

The model takes into account first (M-X), second (M-M or X-X) and third (M-X) neighbor coupling, and the corresponding coupling Hamiltonians matrices contain parameters given in Appendix A. These matrices are of the type ${H_{IJ}}^{(n)}$ where $I, J = [A, B, C, D]$ and n indicates the order of coupling (same atom, first/second/third neighbor).

The on-site couplings ${H_{JJ}}^{(0)}$ include the on-site energy as well as the hybridization between orbitals located on the same atom. ${H_{AA}}^{(0)}$, ${H_{BB}}^{(0)}$, ${H_{CC}}^{(0)}$ and ${H_{DD}}^{(0)}$ are calculated as

$$
\begin{aligned}
{H_{JJ}}^{(0)} = &\begin{bmatrix} \epsilon_1 & 0 & 0 \\ 0 & \epsilon_1 & 0 \\ 0 & 0 & \epsilon_0 \end{bmatrix} + (u_{xx} + u_{yy}) \begin{bmatrix} \alpha_1^{(0)} & \alpha_1^{(0)} & 0 \\ 0 & \alpha_1^{(0)} & 0 \\ 0 & 0 & \alpha_1^{(0)} \end{bmatrix} \\
&+ (u_{xx} - u_{yy}) \begin{bmatrix} \beta_0^{(0)} & 0 & 0 \\ 0 & -\beta_0^{(0)} & \beta_1^{(0)} \\ 0 & \beta_1^{(0)} & 0 \end{bmatrix} + 2u_{xy} \begin{bmatrix} 0 & \beta_0^{(0)} & \beta_1^{(0)} \\ \beta_0^{(0)} & 0 & 0 \\ \beta_1^{(0)} & 0 & 0 \end{bmatrix}
\end{aligned}
$$

The first and third neighbor couplings both follow the same pattern and occur between the A/B and C/D sectors. Third neighbor coupling between the A/B sectors is neglected. Therefore, ${H_{BA}}^{(1)}$, ${H_{DC}}^{(1)}$ and ${H_{DC}}^{(3)}$ are calculated as

$$
\begin{aligned}
{H_{IJ}}^{(n)} = &\begin{bmatrix} t_0^{(n)} & 0 & 0 \\ 0 & t_1^{(n)} & t_2^{(n)} \\ 0 & t_3^{(n)} & t_4^{(n)} \end{bmatrix} + (u_{xx} + u_{yy}) \begin{bmatrix} \alpha_0^{(n)} & 0 & 0 \\ 0 & \alpha_1^{(n)} & \alpha_2^{(n)} \\ 0 & \alpha_3^{(n)} & \alpha_4^{(n)} \end{bmatrix} \\
&+ (u_{xx} - u_{yy}) \begin{bmatrix} \beta_0^{(n)} & 0 & 0 \\ 0 & \beta_1^{(n)} & \beta_2^{(n)} \\ 0 & \beta_3^{(n)} & \beta_4^{(n)} \end{bmatrix} + 2u_{xy} \begin{bmatrix} 0 & \beta_5^{(n)} & \beta_6^{(n)} \\ \beta_7^{(n)} & 0 & 0 \\ \beta_8^{(n)} & 0 & 0 \end{bmatrix}
\end{aligned}
$$

The second neighbor couplings ${H_{AA}}^{(2)}$, ${H_{BB}}^{(2)}$, ${H_{CC}}^{(2)}$ and ${H_{DD}}^{(2)}$ are calculated as

$$
\begin{aligned}
{H_{JJ}}^{(2)} = &\begin{bmatrix} t_0^{(2)} & t_3^{(2)} & t_4^{(2)} \\ -t_3^{(2)} & t_1^{(2)} & t_5^{(2)} \\ -t_4^{(2)} & t_5^{(2)} & t_2^{(2)} \end{bmatrix} + (u_{xx} + u_{yy}) \begin{bmatrix} \alpha_0^{(2)} & \alpha_3^{(2)} & \alpha_4^{(2)} \\ -\alpha_3^{(2)} & \alpha_1^{(2)} & \alpha_5^{(2)} \\ -\alpha_4^{(2)} & \alpha_5^{(2)} & \alpha_2^{(2)} \end{bmatrix} \\
&+ (u_{xx} - u_{yy}) \begin{bmatrix} \beta_0^{(2)} & \beta_3^{(2)} & \beta_4^{(2)} \\ -\beta_3^{(2)} & \beta_1^{(2)} & \beta_5^{(2)} \\ -\beta_4^{(2)} & \beta_5^{(2)} & \beta_2^{(2)} \end{bmatrix} + 2u_{xy} \begin{bmatrix} 0 & \beta_6^{(2)} & \beta_7^{(2)} \\ \beta_6^{(2)} & 0 & \beta_8^{(2)} \\ \beta_7^{(2)} & -\beta_8^{(2)} & 0 \end{bmatrix}
\end{aligned}
$$

As mentioned above, these are only a third of the coupling matrices (those referring to atoms connected by the δ bonds shown in orange in Figure 34). The other couplings can be obtained by a three-fold rotation of these δ bonds, so the corresponding Hamiltonians can be determined as such

$$H_{\delta'}(u_{xx}, u_{yy}, 2u_{xy}) = \mathcal{U}_R^{\dagger}.\, H_{\delta}(u_{xx}', u_{yy}', 2u_{xy}')\mathcal{U}_R$$

where δ' is a $\frac{2\pi}{3}$ counter-clockwise rotation of the original δ bond, in which the updated displacements u_{xx}', u_{yy}' and $2u_{xy}'$ are calculated as

$$u'_{xx} = \frac{u_{xx}}{4} + \frac{3u_{yy}}{4} - \frac{\sqrt{3}u_{xy}}{2} \qquad u'_{yy} = \frac{3u_{xx}}{4} + \frac{u_{yy}}{4} + \frac{\sqrt{3}u_{xy}}{2}$$

$$2u'_{xy} = \frac{\sqrt{3}u_{xx}}{2} - \frac{\sqrt{3}u_{yy}}{2} - u_{xy}$$

and $\mathcal{U}_R$, the 3×3 matrix describing the rotation operation, is as follows

$$\mathcal{U}_R = \begin{bmatrix} -\frac{1}{2} & \frac{\sqrt{3}}{2} & 0 \\ -\frac{\sqrt{3}}{2} & -\frac{1}{2} & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

By applying this rotation operation twice (to obtain δ' and δ''), all couplings in the material will be taken into account. The bandstructure of the considered TMDs can therefore be calculated.

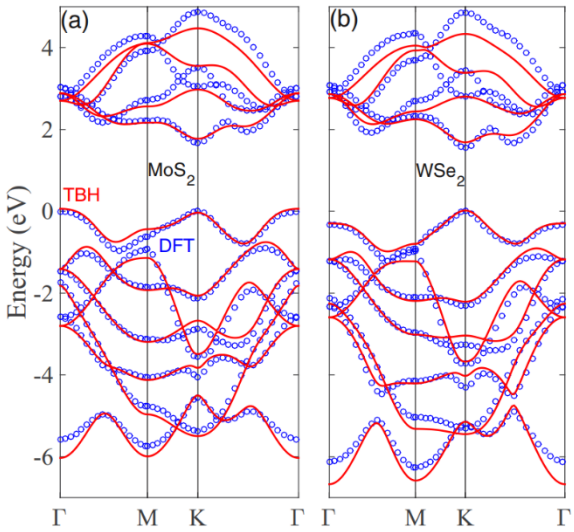


Figure 35. Comparison of the TB bandstructure against DFT results for MoS_2 and WSe_2 [450]

Figure 35, which is pulled from the original article[450] about the TB model that did not yet include the effect of strain, compares the bandstructures obtained with this TB Hamiltonian for MoS_2 and WSe_2 against DFT calculations in which the interaction between ionic cores and valence electrons is described by pseudopotentials of the projector augmented wave (PAW) type, and the exchange-correlation energy of electrons is treated within the generalized gradient approximation (GGA) as parametrized by Perdew, Burke, and Ernzerhof (PBE). As we can see, the TB model yields very good results close to the band gap. As we get further away from the gap however, the accuracy of the model falters because it was calibrated to accurately reproduce the highest VB and lowest CB, which is where our interests lie. The model is therefore well suited for our needs.

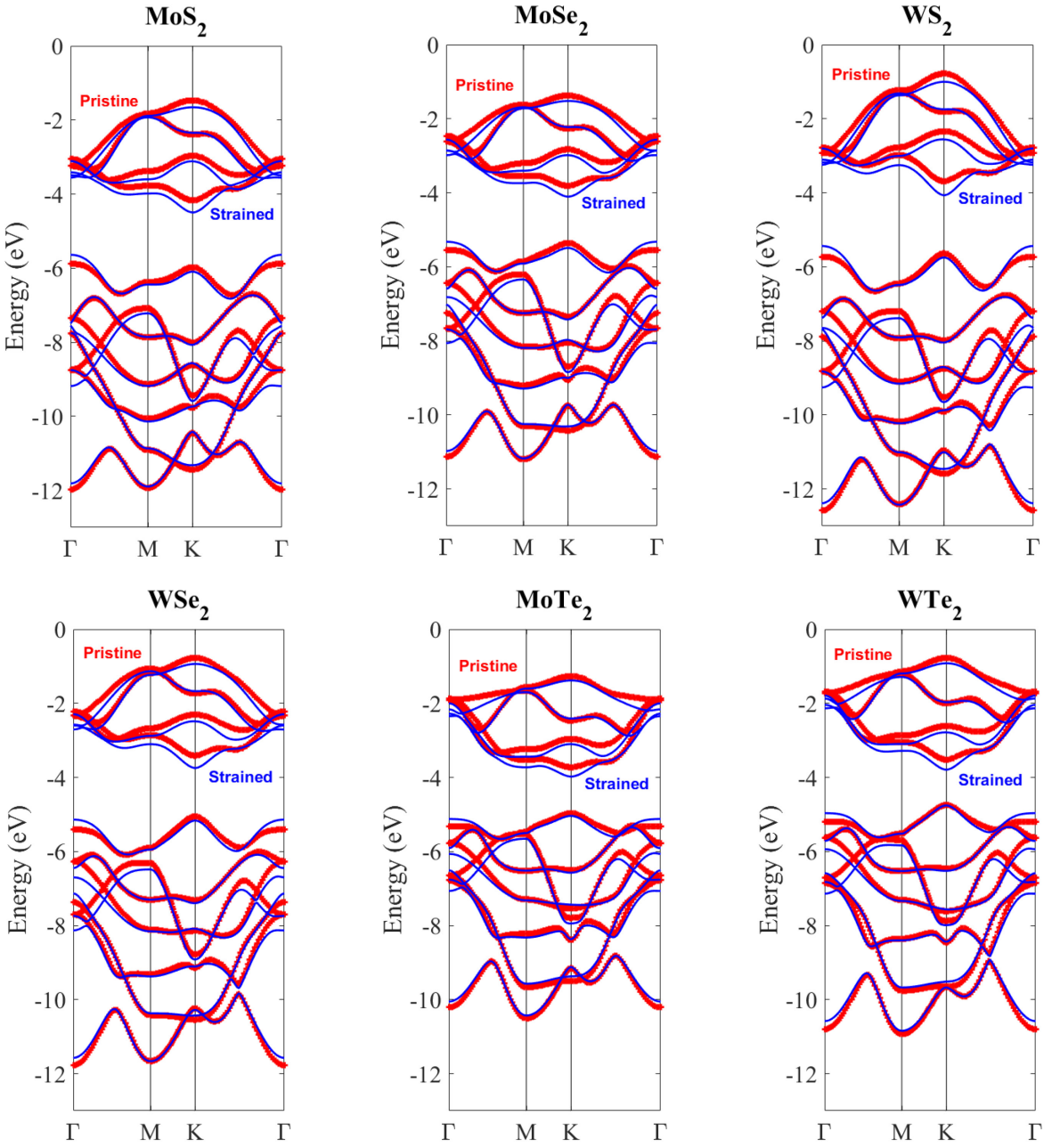


Figure 36. Bandstructures for the six considered TMD in their pristine form (red crosses) and under a 2.5% tensile strain (blue lines)

Figure 36 shows the impact of a 2.5% tensile strain on the bandstructures of all six considered TMDs along high symmetry points in the first Brillouin zone. The bandstructure is modified mainly around the K and Γ high symmetry points, namely the bottom of the CB is pulled towards lower energies at the K point, while the VB is pulled towards higher energies at the Γ point. The band gap is therefore reduced.

This tendency is highlighted in Figure 37, which shows the impact of compressive and tensile strains on the band alignment and band gap in all six considered TMDs. Compressive strains tend to pull both VB and CB towards higher energies, although at different rates, only slightly impacting the band gap. Tensile strains however, as evidenced above, pull the VB up and the CB down, resulting in a dramatic decrease in band gap. Note that while these band gaps are direct in pristine TMDs, these become indirect under any strain roughly $<-1\%$ or $>2\%$.

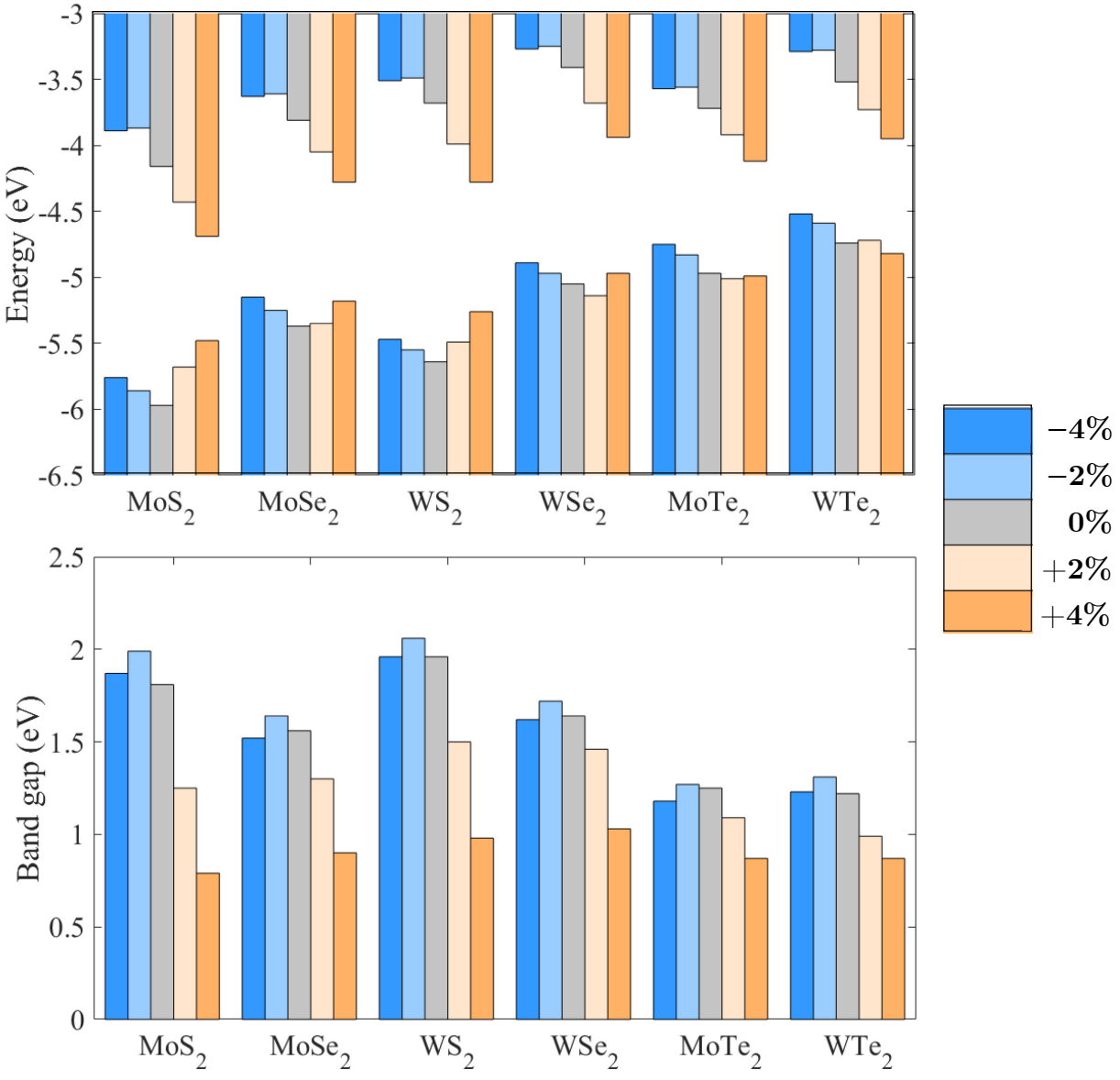


Figure 37. Influence of compressive (<0) and tensile (>0) strains of the highest VB and lowest CB (a) and on the band gap (b) of all six considered TMDs. In a), the vacuum level is set to 0 eV

The goal of this section was solely to properly describe the TB model used and to show the examples of materials modelled with it, therefore I will get further into the detail of band alignment and the possibilities strain offers in this regard in later sections.

Tables containing the TB parameters are given in Appendix A. Please note that in the original article, only 4 TMDs are modelled (MoS_2, WS_2, $MoSe_2$ and WSe_2). Due to the interest WTe_2 and $MoTe_2$ had for use in TFETs (mainly low band gap and interesting band alignment with other TMDs), I contacted Shiang Fang, the author of the original article, to inquire about the availability of such parameters for WTe_2 and $MoTe_2$. Although the work needed to derive those TB parameters had not yet been undertaken, he accepted due to my request, which was the starting point of a fruitful collaboration.

The tables presented in Appendix A contain the TB parameters for all six TMDs.

3.1.4 Basis modification

Now that the base TB model and its features have been introduced, I will present the modifications I made upon this model so that it would suit our computing needs.
As will be shown later, due to the NEGF formalism we use for transport calculations, the unit cell we use must be reproducible along the transport direction; this is not the case of the base, 11-orbital MX_2 unit cell (yellow area in Figure 38). A change in the basis was therefore necessary.

We elected to use a $(MX_2)_2$ unit cell (red area in Figure 38) that can be easily reproduced along the transport direction, resulting in a 22-orbital basis. However, the original TB model was not built for this change in unit cell, mainly due to the way it describes coupling between sectors in discrete matrices.
In order to facilitate this basis modification and the creation of the 22×22 Hamiltonians that will follow, a reworking of the model was necessary.
My goal was to create 11×11 matrices that describe the coupling of orbitals based solely on the positions of the atoms on which they are located; this way, building the final 22×22 Hamiltonians would only be a matter of adding up the correct matrices based on the atomic bonds considered.

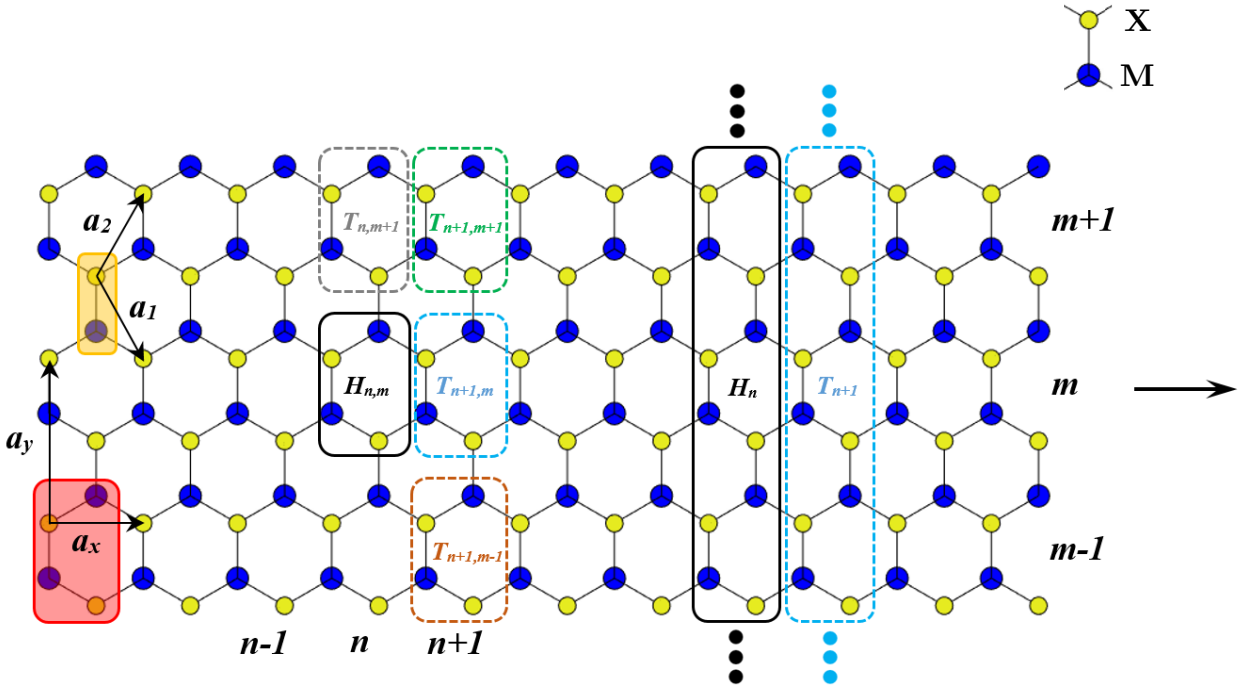


Figure 38. Atomic arrangement of TMDs. The yellow area represents the base, 11-orbital unit cell with the corresponding unit vectors a_1 and a_2, while the red area represents the 22-orbital unit cell used in our work, with its unit vectors a_x and a_y. $H_{n,m}$ and H_n are the Hamiltonians of a single unit cell and a single material "layer", respectively. Finally, $T_{i,j}$ and T_i represent the coupling of the (n,m) cell with the (i,j) unit cell, and the coupling of the (i) layer with the (n) layer, respectively. Transport direction is indicated by the arrow.

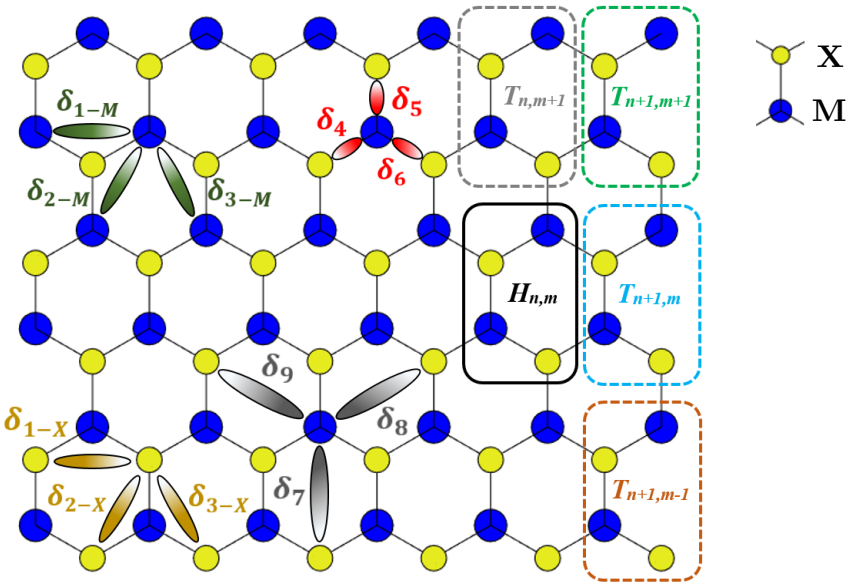


Figure 39. Lattice arrangement of a TMD. The highlighted δ_1 through δ_9 areas represent the coupling matrices between various orbitals on the considered atoms.

There are nine "position pairs" that lead to coupling in this TMD arrangement, referred to as δ_1 to δ_9 in Figure 39. In this figure, coupling direction follows the color gradient (for instance, δ_4 to δ_9 represent the coupling from X to the M atom)

- δ_1, δ_2 and δ_3 represent the coupling between orbitals located on atoms of the same type (either M-M or X-X coupling); they are split into separate δ_{i-X} and δ_{i-M} matrices to simplify Hamiltonian construction later on.

- δ_4, δ_5 and δ_6 represent the first-neighbor coupling between orbitals located on atoms of a different type (X-M coupling).

- δ_7, δ_8 and δ_9 represent the third-neighbor coupling between orbitals located on atoms of a different type (X-M coupling).

In the original model, only a third of the coupling Hamiltonians are given, from which the rest can be calculated due to the rotational symmetry of the structure. The same approach is used here: only δ_1, δ_5 and δ_7 are given, and the rest can be determined from those thanks to $\mathcal{A}_R$, an 11×11 version of the $\mathcal{U}_R$ matrix which describes the rotation operation.

The full, 11×11 matrices for δ_1, δ_5, δ_7 and $\mathcal{U}_R$ are given on the next page, where $H^{(n)}_{XY\,ij}$ is the (i,j) element of the $H^{(n)}_{XY}$ matrix.

$$\delta_{1-X} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & H^{(2)}_{BB_{11}} & H^{(2)}_{BB_{21}} & H^{(2)}_{BB_{31}} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & H^{(2)}_{BB_{12}} & H^{(2)}_{BB_{22}} & H^{(2)}_{BB_{32}} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & H^{(2)}_{BB_{13}} & H^{(2)}_{BB_{23}} & H^{(2)}_{BB_{33}} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & H^{(2)}_{DD_{11}} & H^{(2)}_{DD_{21}} & H^{(2)}_{DD_{31}} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & H^{(2)}_{DD_{12}} & H^{(2)}_{DD_{22}} & H^{(2)}_{DD_{32}} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & H^{(2)}_{DD_{13}} & H^{(2)}_{DD_{23}} & H^{(2)}_{DD_{33}} \end{bmatrix}$$

$$\delta_{1-M} = \begin{bmatrix} H^{AA^{(2)}}_{11} & H^{AA^{(2)}}_{21} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ H^{AA^{(2)}}_{12} & H^{AA^{(2)}}_{22} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & H^{CC^{(2)}}_{11} & H^{CC^{(2)}}_{21} & H^{CC^{(2)}}_{31} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & H^{CC^{(2)}}_{12} & H^{CC^{(2)}}_{22} & H^{CC^{(2)}}_{32} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & H^{CC^{(2)}}_{13} & H^{CC^{(2)}}_{23} & H^{CC^{(2)}}_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$\delta_5 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ H^{BA}_{11} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & H^{BA}_{22} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & H^{BA}_{32} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & H^{DC^{(1)}}_{11} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & H^{DC^{(1)}}_{22} & H^{DC^{(1)}}_{23} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & H^{DC^{(1)}}_{32} & H^{DC^{(1)}}_{33} & 0 & 0 & 0 \end{bmatrix}$$

$$\delta_7 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & H^{(3)}_{DC\,11} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & H^{(3)}_{22}{}^{DC} & H^{(3)}_{23}{}^{DC} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & H^{(3)}_{32}{}^{DC} & H^{(3)}_{33}{}^{DC} & 0 & 0 & 0 \end{bmatrix}$$

As for the 11×11 matrix describing the rotation operation, $\mathcal{A}_R$, it can be calculated from the 3×3 rotation matrix $\mathcal{U}_R$ as follows

$$\mathcal{A}_R = \begin{bmatrix} -1/2 & -\sqrt{3}/2 & 0 & 0 & 0 \\ -\sqrt{3}/2 & -1/2 & 0 & 0 & 0 \\ 0 & 0 & \mathcal{U}_R & 0 & 0 \\ 0 & 0 & 0 & \mathcal{U}_R & 0 \\ 0 & 0 & 0 & 0 & \mathcal{U}_R \end{bmatrix}$$

$$\mathcal{A}_R = \begin{bmatrix} -1/2 & -\sqrt{3}/2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\sqrt{3}/2 & -1/2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1/2 & -\sqrt{3}/2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\sqrt{3}/2 & -1/2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1/2 & -\sqrt{3}/2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -\sqrt{3}/2 & -1/2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1/2 & -\sqrt{3}/2 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\sqrt{3}/2 & -1/2 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

Thanks to this matrix, δ_3 can be determined from δ_1, δ_4 from δ_5, and δ_8 from δ_7 as follows:

$$\delta_3 = {\mathcal{A}_R}^\dagger \delta_1 \mathcal{A}_R \qquad \delta_4 = {\mathcal{A}_R}^\dagger \delta_5 \mathcal{A}_R \qquad \delta_8 = {\mathcal{A}_R}^\dagger \delta_7 \mathcal{A}_R$$

From these newly calculated matrices, δ_2, δ_6 and δ_8 can be calculated by applying the same rotation operation

$${\delta_2}^\dagger = {\mathcal{A}_R}^\dagger \delta_3 \mathcal{A}_R \qquad \delta_6 = {\mathcal{A}_R}^\dagger \delta_4 \mathcal{A}_R \qquad \delta_9 = {\mathcal{A}_R}^\dagger \delta_8 \mathcal{A}_R$$

It is worth noting that by applying $\mathcal{A}_R$ on δ_3, we obtain ${\delta_2}^\dagger$ and not δ_2 because, due to the way the vectors were defined (see Figure 39), $\overrightarrow{\delta_3}$ becomes $-\overrightarrow{\delta_2}$ via this $\frac{2\pi}{3}$ counter-clockwise rotation.

Finally, an 11×11 matrix containing the on-site energies has to be created before we can construct the 22×22 Hamiltonians based on the new, expanded unit cell

$$E_i = \begin{bmatrix}
H^{(0)}_{AA_{11}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & H^{(0)}_{AA_{22}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & H^{(0)}_{BB_{11}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & H^{(0)}_{BB_{22}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & H^{(0)}_{BB_{33}} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & H^{(0)}_{CC_{11}} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & H^{(0)}_{CC_{22}} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & H^{(0)}_{CC_{33}} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & H^{(0)}_{DD_{11}} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & H^{(0)}_{DD_{22}} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & H^{(0)}_{DD_{33}}
\end{bmatrix}$$

Now that we have all 11×11 matrices describing the on-site energies and all possible couplings in the material, they can be used to create the 22×22 Hamiltonians that will describe the material in the new basis.

As is shown in Figure 40, five unique 22×22 Hamiltonians are necessary to fully describe the material

- $H_{n,m}$: the Hamiltonian of the new unit cell
- $T_{n+1,m}, T_{n,m+1}, T_{n+1,m-1}$ and $T_{n+1,m+1}$: the coupling Hamiltonian of the (n, m) unit cell with the (i, j) cell.

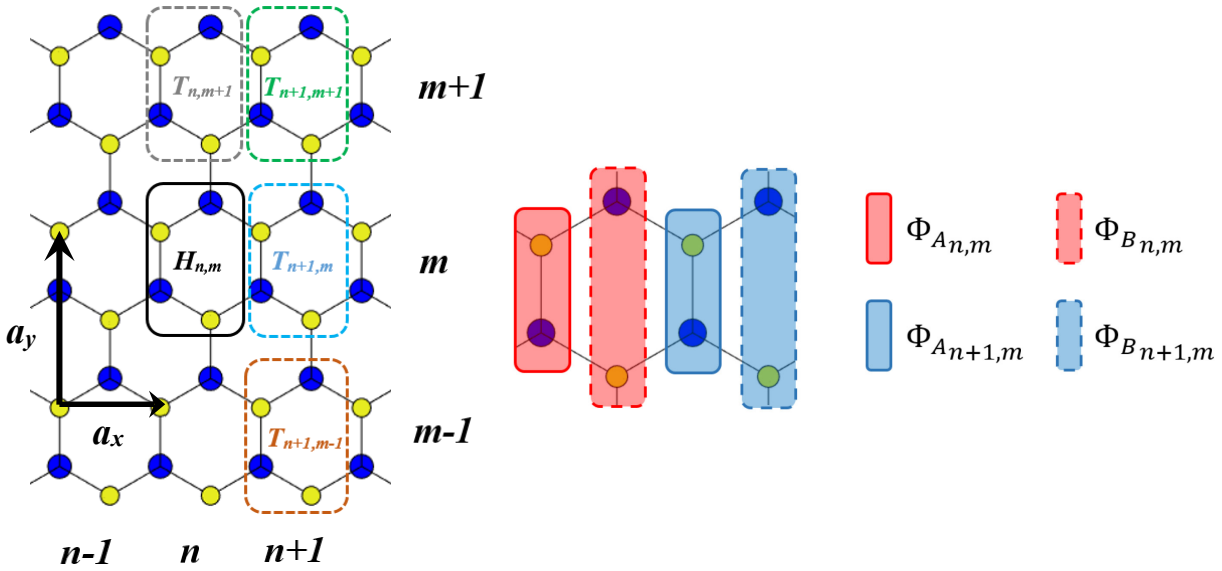


Figure 40. Left: 22×22 Hamiltonians that will have to be created to take all couplings (up to third neighbor) into account: $H_{n,m}$ is the Hamiltonian of a single unit cell, and $T_{i,j}$ represents the coupling of the (n,m) cell with the (i,j) unit cell. Right: Visualisation of the A and B sublattices in two adjacent unit cells. Full (dashed) lines represent the A (B) sublattice, and their color indicates the unit cell to which they belong (red for the (n,m) unit cell, blue for the (n+1,m) unit cell.

The new $(MX_2)_2$ unit cell is twice the size of the original one, and can be decomposed into 2 sublattices A and B as shown in Figure 40. Each of them is associated with the original 11×11 basis

$$\Phi_A = |d_{xz}\rangle, |d_{yz}\rangle, |p_x\rangle, |p_y\rangle, |p_z\rangle, |d_{xy}\rangle, |d_{x^2-y^2}\rangle, |d_{z^2}\rangle, |p_x\rangle, |p_y\rangle, |p_z\rangle$$

$$\Phi_B = |d_{xz}\rangle, |d_{yz}\rangle, |p_x\rangle, |p_y\rangle, |p_z\rangle, |d_{xy}\rangle, |d_{x^2-y^2}\rangle, |d_{z^2}\rangle, |p_x\rangle, |p_y\rangle, |p_z\rangle$$

Each 22×22 Hamiltonian is therefore composed of four 11×11 matrices $\Psi_{X_{i,j}.Y_{k,l}}$. Those matrices are linear combinations of the δ_i and E_i matrices, and describe the coupling between the X sub-lattice of the (i,j) unit cell and the Y sublattice of the (k,l) unit cell. They can be constructed by carefully observing Figure 39 and selecting the couplings that apply to the case considered, just as we did in the example TB for graphene.

$H_{n,m}$ (the Hamiltonian of the unit cell) and $T_{i,j}$ (the Hamiltonians describing the coupling between the unit cell and adjacent cells), can be constructed as

$$H_{n,m} = \begin{pmatrix} \Psi_{A_{n,m}.A_{n,m}} & \Psi_{B_{n,m}.A_{n,m}} \\ \Psi_{A_{n,m}.B_{n,m}} & \Psi_{B_{n,m}.B_{n,m}} \end{pmatrix} \qquad T_{i,j} = \begin{pmatrix} \Psi_{A_{n,m}.A_{i,j}} & \Psi_{B_{n,m}.A_{i,j}} \\ \Psi_{A_{n,m}.B_{i,j}} & \Psi_{B_{n,m}.B_{i,j}} \end{pmatrix}$$

with $i = [n-1, n, n+1]$ and $j = [m-1, m, m+1]$.

Finally, we obtain

$$H_{n,m} = \begin{pmatrix} E_i + \delta_5 + {\delta_5}^\dagger & {\delta_6}^\dagger + \delta_4 + \delta_{3-X} + {\delta_{2-M}}^\dagger \\ \delta_6 + {\delta_4}^\dagger + {\delta_{3-X}}^\dagger + \delta_{2-M} & E_i + \delta_7 + {\delta_7}^\dagger \end{pmatrix}$$

$$T_{n+1,m} = \begin{pmatrix} {\delta_{1-X}}^\dagger + {\delta_{1-M}}^\dagger + {\delta_8}^\dagger + \delta_9 & 0 \\ \delta_{3-M} + {\delta_{2-X}}^\dagger + {\delta_6}^\dagger + \delta_4 & {\delta_{1-X}}^\dagger + {\delta_{1-M}}^\dagger \end{pmatrix} \qquad T_{n,m+1} = \begin{pmatrix} \delta_7 & {\delta_{2-X}}^\dagger \\ {\delta_{3-M}}^\dagger & {\delta_5}^\dagger \end{pmatrix}$$

$$T_{n+1,m-1} = \begin{pmatrix} 0 & 0 \\ \delta_{3-X} & \delta_9 \end{pmatrix} \qquad T_{n+1,m+1} = \begin{pmatrix} 0 & 0 \\ {\delta_{2-M}}^\dagger & {\delta_8}^\dagger \end{pmatrix}$$

as the five unique Hamiltonians needed to fully describe the material.
Those couplings are symmetrical with respect to the original (n, m) unit cell, so that

$$T_{n-k,m-l} = {T_{n+k,m+l}}^\dagger$$

From these Hamiltonian, the bandstructure at a given wave vector $\vec{k}$ can be calculated as we did in the example about graphene. As they are 22×22 matrices, we obtain twice as many bands as with the original MX_2 unit cell and its 11-orbital basis

$$\begin{aligned} H_{tot} = H_{n,m} &+ T_{n+1,m} . e^{i\vec{k}\cdot\overrightarrow{a_{n+1,m}}} + {T_{n+1,m}}^\dagger . e^{-i\vec{k}\cdot\overrightarrow{a_{n+1,m}}} \\ &+ T_{n,m+1} . e^{i\vec{k}\cdot\overrightarrow{a_{n,m+1}}} + {T_{n,m+1}}^\dagger . e^{-i\vec{k}\cdot\overrightarrow{a_{n,m+1}}} \\ &+ T_{n+1,m+1} . e^{i\vec{k}\cdot\overrightarrow{a_{n+1,m+1}}} + {T_{n+1,m+1}}^\dagger . e^{-i\vec{k}\cdot\overrightarrow{a_{n+1,m+1}}} \\ &+ T_{n+1,m-1} . e^{i\vec{k}\cdot\overrightarrow{a_{n+1,m-1}}} + {T_{n+1,m-1}}^\dagger . e^{-i\vec{k}\cdot\overrightarrow{a_{n+1,m-1}}} \end{aligned}$$

in which

$$\overrightarrow{a_{n+1,m}} = \overrightarrow{a_x} = \begin{pmatrix} a_{MX_2} \\ 0 \end{pmatrix} \qquad \overrightarrow{a_{n,m+1}} = \overrightarrow{a_y} = \begin{pmatrix} 0 \\ \sqrt{3} a_{MX_2} \end{pmatrix}$$

$$\overrightarrow{a_{n+1,m+1}} = \overrightarrow{a_x} + \overrightarrow{a_y} = \begin{pmatrix} a_{MX_2} \\ \sqrt{3} a_{MX_2} \end{pmatrix} \qquad \overrightarrow{a_{n+1,m-1}} = \overrightarrow{a_x} - \overrightarrow{a_y} = \begin{pmatrix} a_{MX_2} \\ -\sqrt{3} a_{MX_2} \end{pmatrix}$$

where a_{MX_2} = 3.18 Å for MoS_2 and WS_2.
3.31 Å for $MoSe_2$ and WSe_2.
3.55 Å for $MoTe_2$ and WTe_2.

The bandstructure of all 6 TMDs along high symmetry points in the first Brillouin zone is shown in Figure 41. Due to the basis modification resulting in the 22×22 Hamiltonians, 22 bands are obtained. As expected for all six materials, this bandstructure is in agreement with the one obtained in the original basis: the additional bands originate from the band folding that occurs due to the doubling of the unit cell along the k_x direction, and is highlighted in Appendix B.

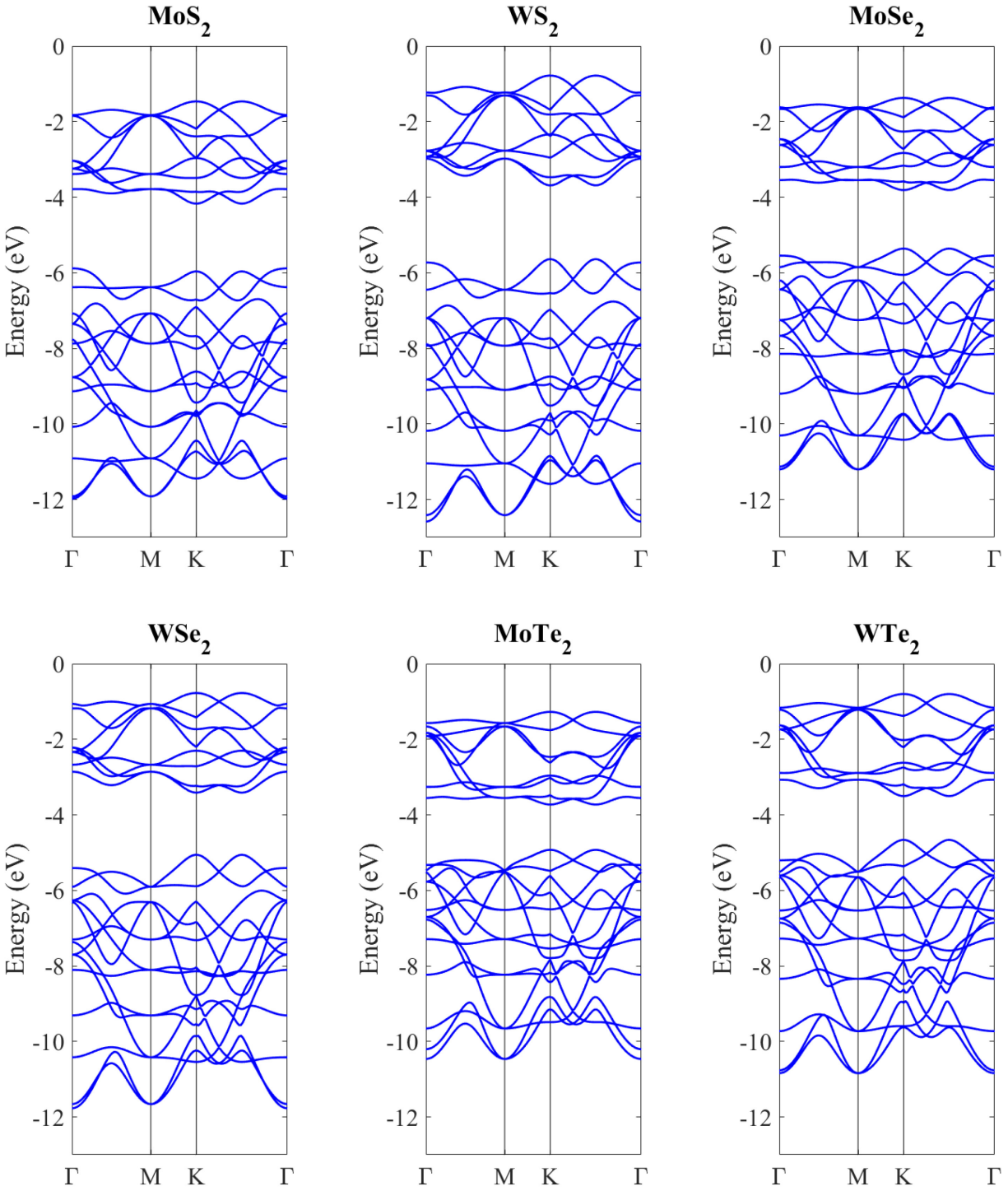


Figure 41. Bandstructure for all six TMDs as obtained with the 22×22 Hamiltonians resulting from the expanded unit cell.

3.1.5 Band alignment in TMDs

As mentioned in Section 1.4, band alignment is paramount in TFETs due to their reliance on band-to-band-tunneling.

The band alignment obtained between the TMDs considered in this TB model will therefore strongly dictate TFET performance and impact the heterostructures we choose to investigate. As a reminder, carriers tunnel from the source VB to the channel CB in an n-type TFET, therefore in the case of heterostructure-based TFETs, optimal operation requires a high VB and a low CB.
Pristine TMDs obtained with this TB model yield the band alignment shown in Figure 42 (the vacuum level is set to 0 eV). MoS_2 has by far the lowest CB at -4.17 eV, and is therefore a great candidate for use as the channel/drain material. As for the source material, we can see that WTe_2 yields the highest VB at -4.74 eV, followed by $MoTe_2$ and WSe_2 around -5.0 eV. These TMDs could therefore be used as a source material in the heterojunction TFETs envisioned.

However, this band alignment is only valid for TMDs in their pristine form, therefore when no strain is applied. As mentioned in Section 2.2.2, the lattice parameter in TMDs is dictated by the chalcogen atom and ranges from 3.18 Å for MoS_2 and WS_2 to 3.55 Å for $MoTe_2$ and WTe_2, and 3.31 Å for $MoSe_2$ and WSe_2.
In the case of a heterojunction between two TMDs with different chalcogen atoms, the lattice parameter will not be the same on either side of the interface, and the material will experience strain so that lattice matching can be reached.

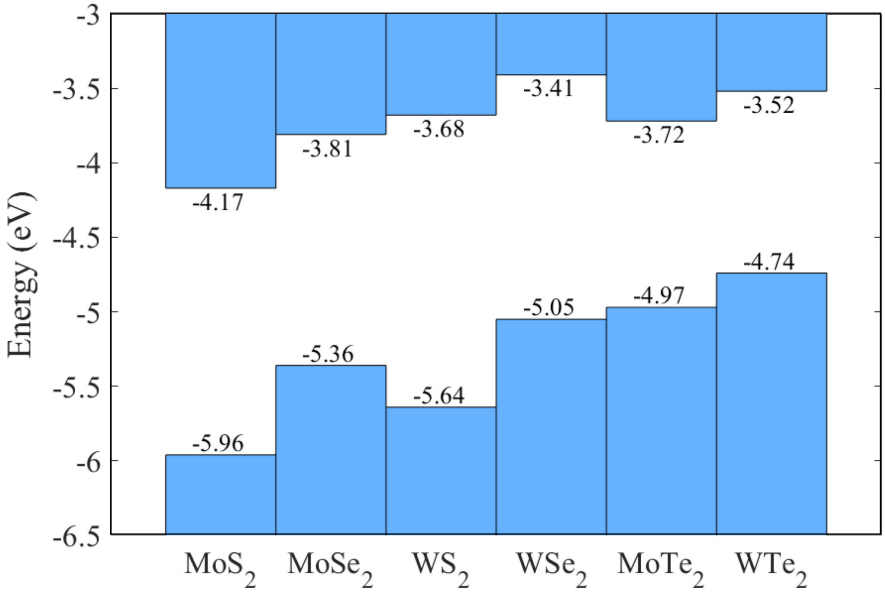


Figure 42. Band alignment in pristine TMDs obtained by using this TB model. The vacuum level is set to 0 eV.

In the case of the $MoSe_2/MoS_2$ and WSe_2/MoS_2 heterojunctions, we approximate that only MoS_2 will experience strain. Therefore, a tensile strain of roughly 4.3% will be applied onto MoS_2 to reach $a_{ASe_2} = 3.31$ Å (as mentioned in Chapter 2., TMDs can withstand strains of up to 20% before breaking). Under this strain, the bandstructure of MoS_2 is heavily modified, as shown in Figure 43 (left): the CB is substantially lowered, but its minimum remains at the K point, while the VB is also modified, its maximum shifting to the Γ point.
Figure 43 (right) shows the lowest CB and highest VB of both pristine and strained MoS_2, and of $MoSe_2$ (top) and WSe_2 (bottom). It highlights the impact of strain on the band alignment of these materials, and on the benefits this strain has for TFET operation. Band offset is reduced by 680 meV in both cases, resulting in a 510 meV band offset for $MoSe_2/MoS_2$ and 200 meV for WSe_2/MoS_2.

In this case, the strain caused by the lattice mismatch will probably benefit TFET performance of the $MoSe_2/MoS_2$ and WSe_2/MoS_2 heterojunctions.

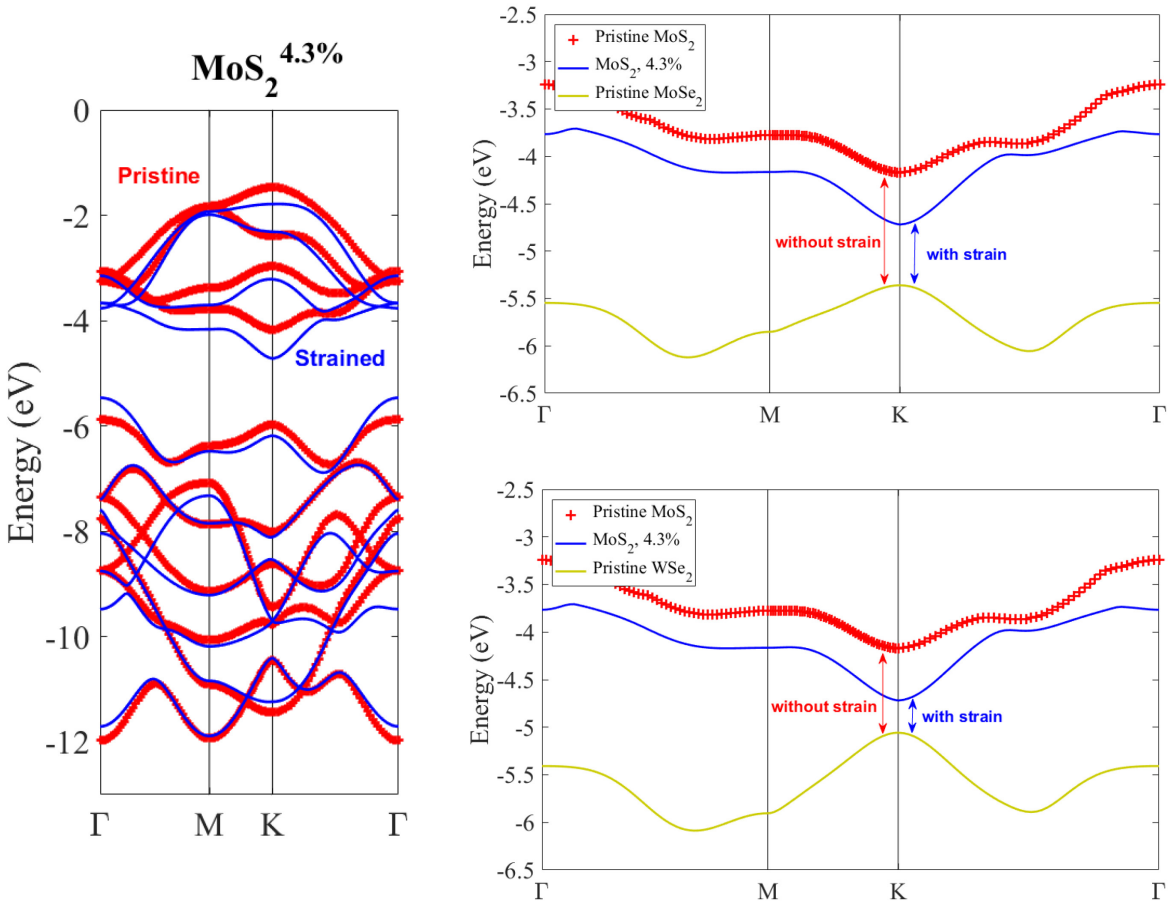


Figure 43. Left: Banstructure of MoS_2 in pristine form (red crosses) and under a 4.3% tensile strain (blue curves). Right: Highest VB of $MoSe_2$ (top), WSe_2 (bottom) (gold curve) and lowest CB of both pristine and strained MoS_2 (resp. red crosses and blue curve)

In the case of the $MoTe_2/MoS_2$ and WTe_2/MoS_2 heterojunctions, the lattice mismatch is much greater (0.37 Å). Therefore, we approximate that both materials will experience strain so that a common lattice parameter of $a = 3.35$ Å is reached. Therefore, a tensile strain of roughly 5.3% will be applied onto MoS_2, while a compressive strain of roughly 5.6% will be applied onto $MoTe_2$ and WTe_2. Under this strain, the bandstructure of all three materials are heavily modified, as shown in Figure 44: in MoS_2 the changes are the same as those mentioned before, while in $MoTe_2$ and WTe_2 the minimum of the CB shifts outside of the K point, while the VB is heavily pulled towards higher energies, its maximum remaining in the K point.

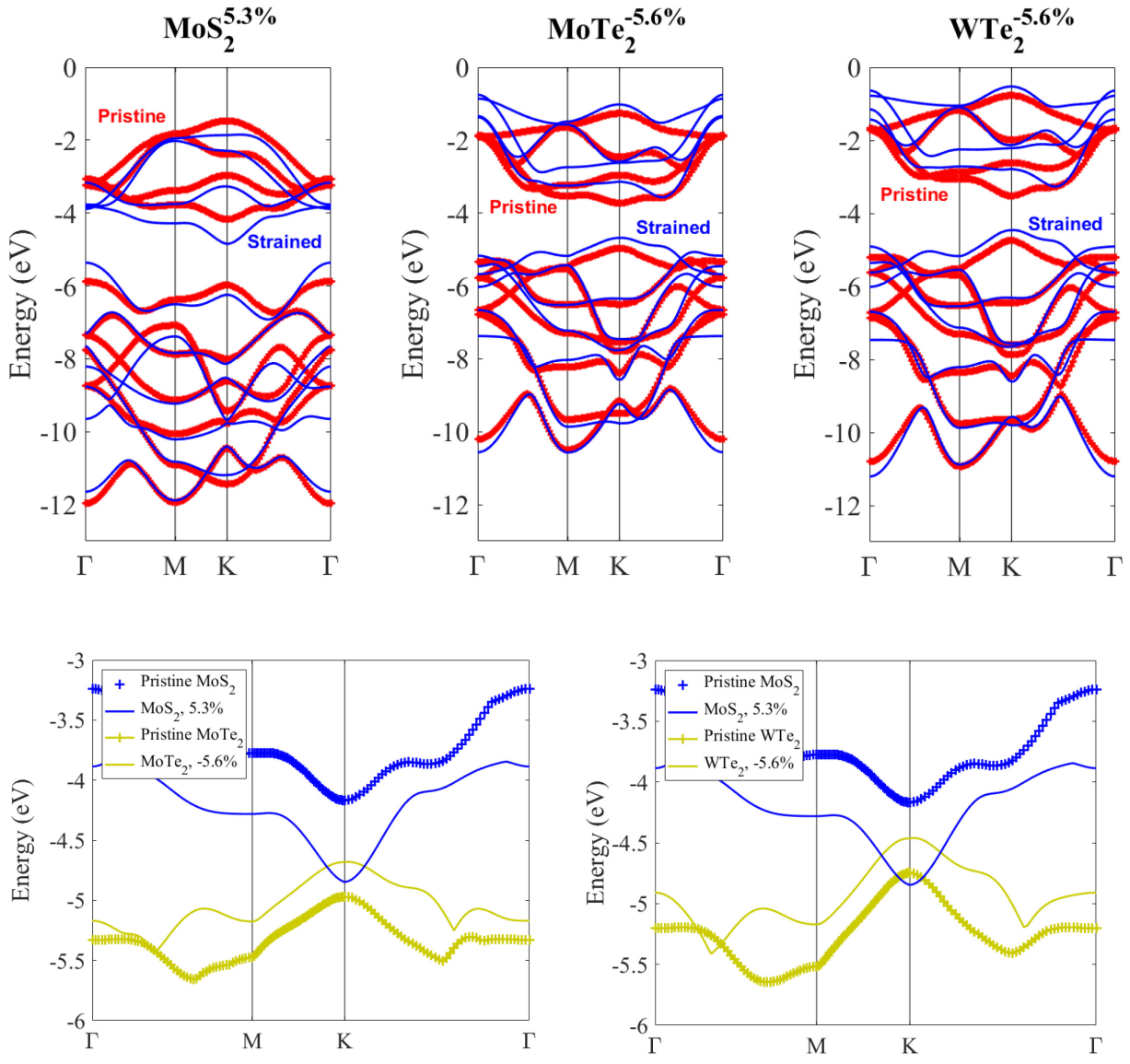


Figure 44. Top: Bandstructures of MoS_2, $MoTe_2$ and WTe_2 both in their pristine form (red crosses) and under the necessary strains to reach lattice matching (blue curves). Bottom: Highest VB of $MoTe_2$ and WTe_2 in their pristine form and under strain (resp. gold crosses and gold curve), and lowest CB of MoS_2 both in its pristine form and under strain (resp. blue crosses and blue curve)

Figure 44 (bottom) once again highlights the benefits of this strain on the band alignment. In the case of the $MoTe_2/MoS_2$ heterojunction, the band offset goes from roughly 800 meV without strain to −170 meV under strain: the $MoTe_2$ VB maximum is actually higher than the bottom of the MoS_2 CB. This configuration is known as a "broken gap", and is expected to be extremely beneficial to TFET performance.
The WTe_2/MoS_2 heterojunction yields similar results: the band offset goes from roughly 570 meV without strain to −390 meV under strain.
Figure 45 shows the band alignment that occurs in all heterojunction TFETs when the proper strain is applied, and highlights the broken gap configuration of the $MoTe_2/MoS_2$ and WTe_2/MoS_2 heterojunctions.

As will be shown in Chapter 6, this strain-induced "broken gap" allows the $MoTe_2/MoS_2$ and WTe_2/MoS_2 heterojunction TFETs to yield extremely promising results

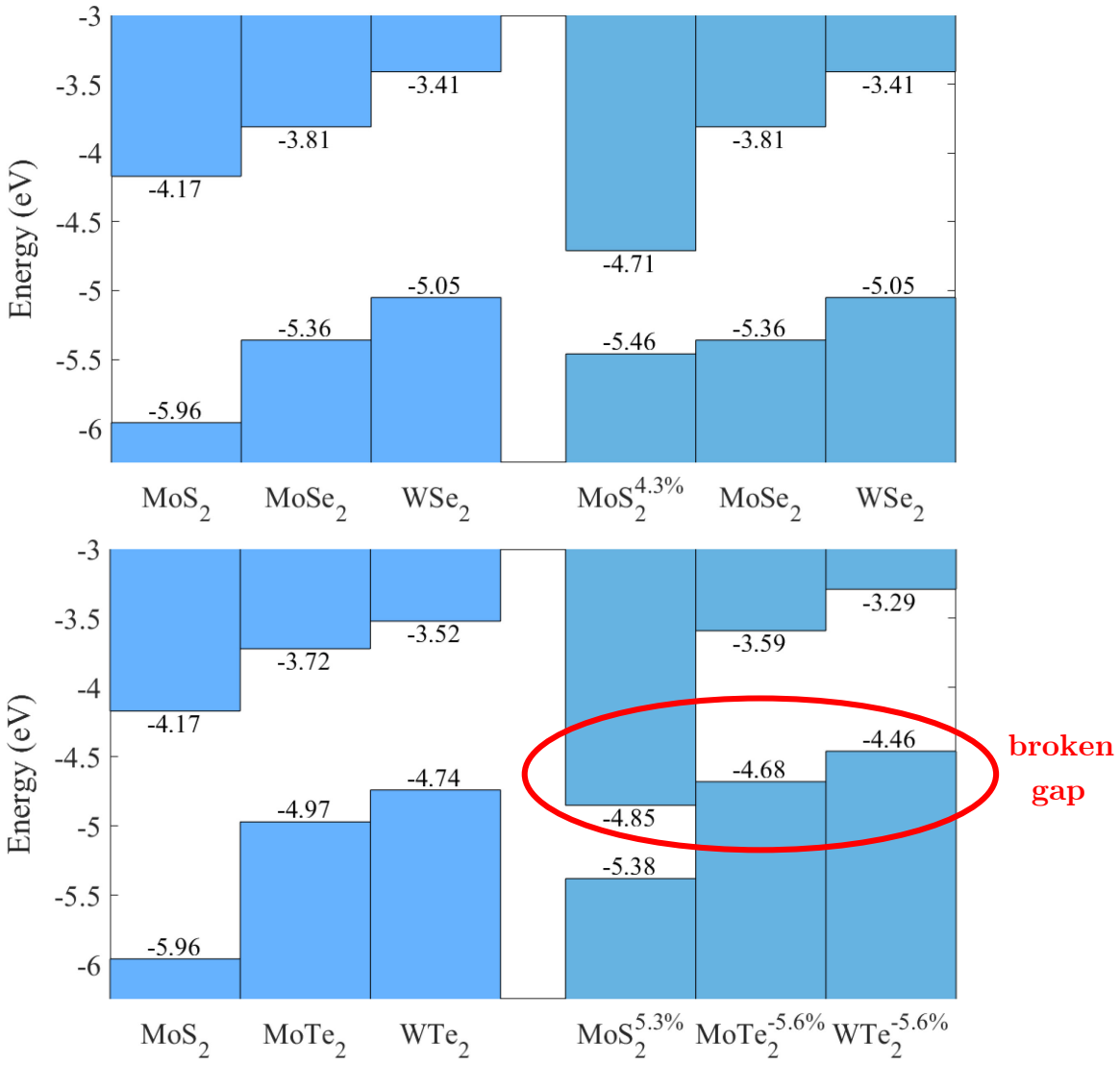


Figure 45. Top: CB and VB of MoS_2, $MoSe_2$ and WSe_2 in their pristine form and under the strain applied in the ASe_2/MoS_2 heterojunctions. Bottom: CB and VB of MoS_2, $MoTe_2$ and WTe_2 in their pristine form and under the strain applied in the ATe_2/MoS_2 heterojunctions.

This section introduced the most important aspect of the tight-binding approach and model used in this thesis. The TB theory was briefly explained, before highlighting and showing in detail the creation of the fully atomistic tight-binding Hamiltonians that will be used in the electronic transport simulation.

The next section will briefly introduce the NEGF formalism, before focusing on its implementation in the transport code.

3.2 Non-Equilibrium Green's Function (NEGF) formalism

In this section, I will very briefly describe the main aspects of the NEGF formalism, and its use in transport calculations.
For much more detailed information about this technique, the reader is referred to dedicated handbooks [451]–[454].

3.2.1 Definition of Green's function

The Green's function method is a technique that can strongly simplify the solving of linear differential equations.

For instance, consider

$$Dy(x) = f(x) \tag{18}$$

where D is an operator.
The Green's function associated to D is defined as

$$DG(x, x') = \delta(x - x') \tag{19}$$

in which δ is the delta function.
The solution $y(x)$ can therefore be calculated as

$$y(x) = \int G(x, x')f(x')dx' \tag{20}$$

Solving Eq.(19) is easier than Eq.(18) because it does not include $f(x)$ and $y(x)$ and only depends on the operator D. Plus, this technique is extremely versatile as $G(x, x')$ can be used to solve all equations of the type Eq.(18), no matter $y(x)$.

Thanks to this versatility, the Green's function method is often used to solve linear differential equations in a wide range of applications.
Obviously, its use in the computation of electronic transport is the aspect we are focused on, and I will introduce it in further detail.

3.2.2 Use in quantum transport calculations

Green's functions are commonly used to solve Schrödinger's or Poisson's equation in the case of quantum transport.

From Schrödinger's equation

$$H|\varphi\rangle = E|\varphi\rangle \tag{21}$$

which can be rewritten as a function of the $(E - H)$ operator as follows

$$(E - H)|\varphi\rangle = 0 \tag{22}$$

we can define Green's function as

$$(E - H)G(r, r'; E) = \delta(r - r') \tag{23}$$

Once a specific basis has been defined, the previous operators can be written in matrix form

$$(EI - H)G(E) = \mathrm{I} \qquad\qquad G(E) = (EI - H)^{-1} \tag{24}$$

However, this simple approach would only work for isolated systems with no coupling to their surroundings, which is obviously not the case in transport problems.

In most transport problems, the considered system can be divided into three distinct regions (see Figure 46): the left and right semi-infinite contacts, and the device region, connecting the two.

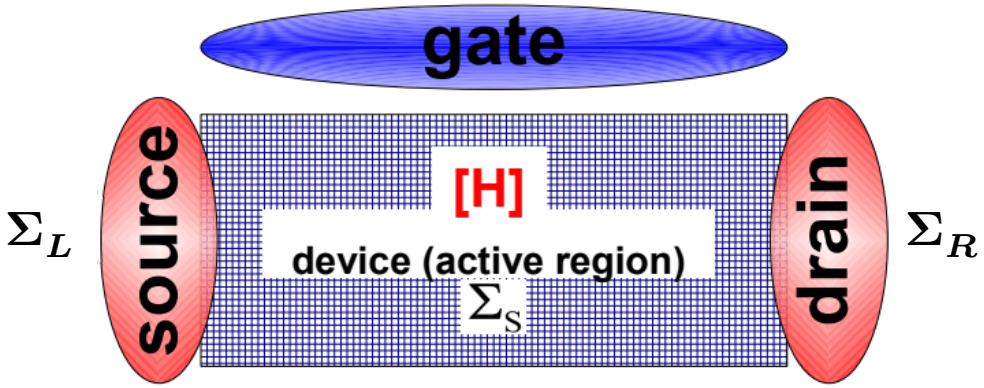


Figure 46. Schematic representation of a transistor highlighting the three regions (source, device and drain) [455]

In this case, the coupling between the active region (device) and the left and right contacts has to be considered. This is done via the so-called "self-energies" Σ_L and Σ_R.

The Green's function equation then becomes

$$G(E) = \left((E + i0^+)I - H_D - \Sigma_L - \Sigma_R\right)^{-1} \tag{25}$$

in which H_D is the Hamiltonian of the device region, $\Sigma_{L(R)}$ is the self-energy of the left (right) semi-infinite contact and 0^+ is an infinitesimal element added to prevent divergence. If phonon scattering is considered, the self-energy due to scattering processes in the device (Σ_S) has to be included.

3.2.2.1 Calculation of the self-energies

In order to help with the calculation of the self-energies, the system is subdivided into layers, perpendicular to transport direction (see Figure 47).
The device region is composed of N identical layers and its Hamiltonian H_D is therefore

$$H_D = \begin{bmatrix} H_1 & H_{1,2} & 0 & & & & \\ H_{2,1} & H_2 & H_{3,2} & & & & \\ 0 & H_{3,2} & H_3 & \ddots & & & \\ & & \ddots & \ddots & \ddots & & \\ & & & \ddots & H_{N-2} & H_{N-2,N-1} & 0 \\ & & & & H_{N-1,N-2} & H_{N-1} & H_{N-1,N} \\ & & & & 0 & H_{N,N-1} & H_N \end{bmatrix}$$

where H_K is the Hamiltonian of the K layer and $H_{I,J}$ the coupling Hamiltonian between layers I and J.

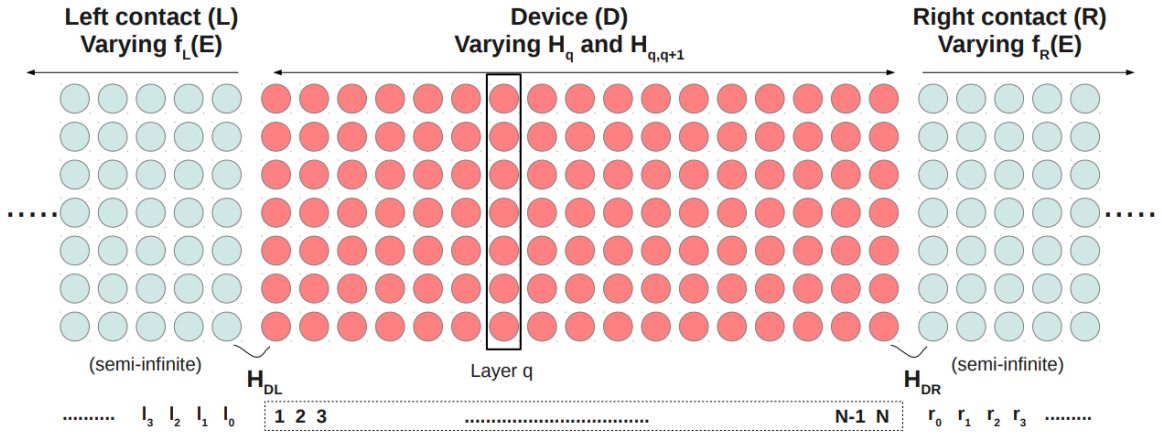


Figure 47. Subdivision of the system into individual layers [456]

The matrices describing the self-energies are therefore N×N matrices as well

$$\Sigma_L = \begin{bmatrix} \Sigma_L^S & 0 & & & \\ 0 & 0 & & & \\ & & \ddots & & \\ & & & 0 & 0 \\ & & & 0 & 0 \end{bmatrix} \qquad \Sigma_R = \begin{bmatrix} 0 & 0 & & & \\ 0 & 0 & & & \\ & & \ddots & & \\ & & & 0 & 0 \\ & & & 0 & \Sigma_R^S \end{bmatrix}$$

Σ_L^S and Σ_R^S can be obtained [457] by solving

$$\Sigma_L^S = H_{DL} . g_0^L . H_{LD} \qquad \Sigma_R^S = H_{DR} . g_0^R . H_{RD} \tag{26}$$

where H_{DL} is the coupling between the first layer of the device region and the first layer of the source region ($H_{LD} = {H_{DL}}^\dagger$), H_{DR} is the coupling between the N-th layer of the device region and the first layer of the drain region ($H_{RD} = {H_{DR}}^\dagger$), and $g_0^{L(R)}$ is the surface Green's function at the left (right) contact.

These surface Green's functions are defined[457] by the recursive relation

$$g_n^{L(R)} = \left(E + i0^+ - H_n^{L(R)} - H_{n,n+1}^{L(R)} . g_{n+1}^{L(R)} . H_{n+1,n}^{L(R)}\right)^{-1} \tag{27}$$

While this equation can technically be solved, it proves extremely challenging from a convergence standpoint. I will not detail it here since it is widely available elsewhere[456], [456], [457], but a so-called "quick-iterative scheme" was introduced by Sancho et al. in 1984[458]. It uses an enhanced solving method that allows for the consideration of 2^n layers after n iterations, compared to simply solving Eq.(27), which solves one layer per iteration.

3.2.2.2 Recursive Green's function algorithm

Transmission and Density of States (DOS) are the most important characteristics for transport and device analysis, mainly because most other characteristics such as electrical ones can be derived from them.

Due to the often very large size of the device Hamiltonian H_D, it can be computationally impossible to obtain the device's Green's function matrix by direct inversion. It has been shown[457], [459] that to reduce the computational burden of this method, one can compute only specific elements of the Green's function matrix which are those needed to calculate DOS and ballistic transmission.

These elements are G_{11} or G_{NN} for the transmission, and G_{i1}, ${G_{1i}}^{\dagger}$, G_{iN} and ${G_{Ni}}^{\dagger}$ for the calculation of DOS at the i-th layer.

G_{11} and G_{NN} can be calculated using a recursive algorithm based on the Dyson's equations (G_{11} is shown here but G_{NN} can be calculated in a similar manner; more detail available in [457], [459])

$$\text{Calculate } G_{NN}^{S} = (E + i0^{+} - H_N - \Sigma_R)^{-1}$$

$$\text{for } j = N, N-1, \ldots, 3, 2 \;\rightarrow\; G_{jj}^{S} = (E + i0^{+} - H_j - H_{j,j+1}.\, G_{j+1,j+1}^{S}.\, H_{j+1,j})^{-1}$$

$$G_{11} = G_{11}^{S} = (E + i0^{+} - H_1 - \Sigma_L - H_{12}.\, G_{22}^{S}.\, H_{21})^{-1} \tag{28}$$

As for G_{i1}, ${G_{1i}}^{\dagger}$, G_{iN} and ${G_{Ni}}^{\dagger}$, they can be calculated as follows (in which $A = E + i0^{+} - H - \Sigma_L - \Sigma_R$)

for G_{i1}:

$$A_{11}G_{11} + A_{12}G_{21} = 1$$

$$A_{21}G_{11} + A_{22}G_{21} + A_{23}G_{31} = 0$$

$$\vdots$$

$$A_{i,i-1}G_{i-1,1} + A_{i,i}G_{i,1} + A_{i,i+1}G_{i+1,1} = 0 \tag{29}$$

for G_{iN}:

$$A_{NN}G_{NN} + A_{N,N-1}G_{N-1,N} = 1$$

$$A_{N-1,N}G_{NN} + A_{N-1,N-1}G_{N-1,N} + A_{N-1,N-2}G_{N-2,N} = 0$$

$$\vdots$$

$$A_{i,i-1}G_{i-1,N} + A_{i,i}G_{i,N} + A_{i,i+1}G_{i+1,N} = 0 \tag{30}$$

Using these techniques allows for a drastic reduction of the computing resources required compared to the traditional, "brute-force" inversion of the large device Hamiltonian.

3.2.3 Calculation of transport properties from NEGF

Now that the matrix form (or at least the necessary elements) of the Green's function of the device has been calculated, it can be used to access electrical and transport characteristics in the device such as transmission, DOS, LDOS and current.

3.2.3.1 Transmission

When considering ballistic transport, the transmission through the system can be calculated as [451], [457], [460]

$$T = \text{trace}[\Gamma_L G \Gamma_D G^\dagger] \tag{31}$$

where $\Gamma_{L(R)} = i[\Sigma_{L(R)} - {\Sigma_{L(R)}}^\dagger]$ corresponds to the energy level broadening due to the coupling with the source (drain).

However, if we used the recursive approach to calculate only specific elements of the Green's matrix as detailed in the previous section, the transmission can be obtained in two distinct ways

$$T(E) = trace\big[\hat{\Gamma}_L\big(i\big(\mathrm{G}_{11} - {\mathrm{G}_{11}}^\dagger\big) - \mathrm{G}_{11}\hat{\Gamma}_L{\mathrm{G}_{11}}^\dagger\big)\big] \tag{32}$$

$$T(E) = trace\big[\hat{\Gamma}_R\big(i\big(\mathrm{G}_{NN} - {\mathrm{G}_{NN}}^\dagger\big) - {\mathrm{G}_{NN}}^\dagger\hat{\Gamma}_L\mathrm{G}_{NN}\big)\big] \tag{33}$$

where $\hat{\Gamma}_{L(R)} = i[\widehat{\Sigma}_{L(R)} - {\widehat{\Sigma}_{L(R)}}^\dagger]$ (as a reminder, $\widehat{\Sigma}_{L(R)} = H_{DL(R)} . g_0^{L(R)} . H_{L(R)D}$)

3.2.3.2 DOS and LDOS

The density of states corresponds to the number of states per unit volume within a given energy interval $[E, E + dE]$ and is therefore given as

$$D(E) = \frac{dN(E)}{dE} \tag{34}$$

which can be rewritten using the delta function

$$D(E) = \sum_n \delta(E - E_n) \tag{35}$$

It has been shown[451], [457], [460] that the Lorentz form of the delta function

$$\sum_n \delta(E - E_n) = \lim_{n\to 0} \sum_n \frac{\eta}{\pi(E - E_n)^2 + \eta^2} \tag{36}$$

where $\eta = 0^+$ can be used to obtain the DOS when using the Green's function method. By defining the spectral function $A = i[G - G^\dagger]$, the DOS can be calculated as

$$D(E) = \frac{\text{trace}(A)}{2\pi} = \frac{i \times \text{trace}(G - G^\dagger)}{2\pi} \tag{37}$$

The local density of states corresponds to the density of states at a specific point in real-space. Therefore, it can simply be calculated for the i-th layer from the G_{ii} element of the Green's matrix as

$$D_{ii}(E) = \frac{\text{trace}(A_{ii})}{2\pi} = \frac{i \times \text{trace}\big(G_{ii} - {G_{ii}}^\dagger\big)}{2\pi} \tag{38}$$

Because $A_{ii} = i\big[G_{ii} - {G_{ii}}^\dagger\big] = -2Im(G_{ii})$, it can also be obtained as follows

$$D_{ii}(E) = -\text{trace}\left[\frac{Im(G_{ii})}{\pi}\right] \tag{39}$$

LDOS is an important analysis tool in nanoelectronic transport because it can reveal quantum effects such as resonances that arise due to confinement.

3.2.3.3 Electrical current and conductance

The ballistic electrical current flowing through the device when a voltage bias is applied can be calculated from the transmission via the standard Landauer's formula[451], [457], [460]

$$I = \frac{2e}{h} \int [f_L(E - \mu_L) - f_R(E - \mu_R)]\, T(E) dE \tag{40}$$

where $f_{L(R)}(E - \mu_{L(R)})$ is the Fermi function (see Chapter 1.2.1) of the left (right) contact, in which $\mu_{L(R)} = E_{F_{L(R)}} + U_{L(R)}$, $E_{F_{L(R)}}$being the Fermi energy in the left (right) contact and $U_L - U_R = eV_{DS}$

In a similar manner, ballistic conductance can be calculated as

$$G_e(\mu, T_0) = \lim_{V_{DS}\to 0} \frac{I}{V_{DS}} = \frac{2e^2}{h} \int \frac{\partial f(E, \mu, T_0)}{\partial E} T(E) dE \tag{41}$$

In this section, the basic theory of the NEGF method and its use in the computation of nanoelectronic transport have been detailed.
I will now focus on its implementation with the TB model, and their implementation in the transport code.

3.3 Implementation of TB and NEGF models

Now that the TB theory and model used as well as the NEGF method have been introduced, this section aims to present their interaction with one another as well as their implementation in the electronic transport code.

3.3.1 Creation of the layer Hamiltonians

As shown in the previous section, in NEGF theory the device region has to be divided into repeating layers along the transport direction, which results in the change in basis of the TB model detailed in Section 3.1.4.
The 22×22 Hamiltonians $H_{n,m}, T_{n+1,m}, T_{n,m+1}, T_{n+1,m-1}$ must therefore be used to create the layer Hamiltonians H_n and T_{n+1} shown in Figure 48.

Since they regroup the influence of a whole layer into a single Hamiltonian, H_n will be calculated solely from $H_{n,m}$ and $T_{n,m+1}$, while T_{n+1} will be calculated using $T_{n+1,m}, T_{n+1,m-1}$ and $T_{n+1,m+1}$.

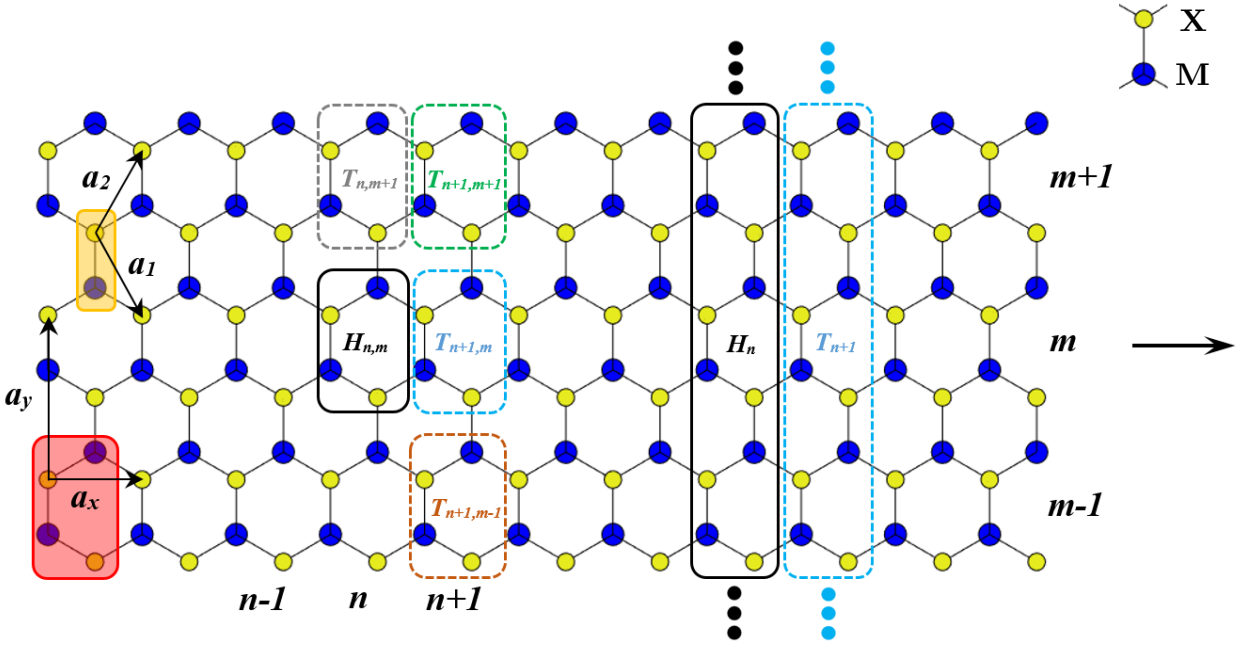


Figure 48. Atomic arrangement of TMDs. The yellow area represents the base, 11-orbital unit cell with the corresponding unit vectors a_1 and a_2, while the red area represents the 22-orbital unit cell used in our work, with its unit vectors a_x and a_y. $H_{n,m}$ and H_n are the Hamiltonians of a single unit cell and a single material "layer", respectively. Finally, $T_{i,j}$ and T_i represent the coupling of the (n,m) cell with the (i,j) unit cell, and the coupling of the (i) layer with the (n) layer, respectively. Transport direction is indicated by the arrow

At a given y component of the wave vector k_y, these matrices can be calculated as follows

$$H_n(k_y) = H_{n,m} + T_{n,m+1}.e^{i.k_y.a_y} + T_{n,m-1}.e^{-i.k_y.a_y} \tag{42}$$

$$T_{n+1}(k_y) = T_{n+1,m} + T_{n+1,m-1}.e^{-i.k_y.a_y} + T_{n+1,m+1}.e^{i.k_y.a_y} \tag{43}$$

$$T_{n-1}(k_y) = T_{n+1}(k_y)^{\dagger} = {T_{n+1,m}}^{\dagger} + {T_{n+1,m-1}}^{\dagger}.e^{i.k_y.a_y} + {T_{n+1,m+1}}^{\dagger}.e^{-i.k_y.a_y} \tag{44}$$

They are therefore 22×22 matrices as well.

With those layer Hamiltonians now calculated, the total Hamiltonian at a given wave vector (k_x, k_y) can be calculated as

$$H_{tot}(k_x, k_y) = H_n(k_y) + T_{n+1}(k_y).e^{i.k_x.a_x} + T_{n-1}(k_y).e^{-i.k_x.a_x} \tag{45}$$

This Hamiltonian fully describes a single layer of the 2D infinite TMD and its coupling to the surrounding layers at a given wave vector.

In the case of an in-plane heterojunction as shown in Figure 49, the appropriate orbital couplings are used in each material, and the coupling at the interface is calculated as the average of the coupling parameters of the materials on either side of the interface.

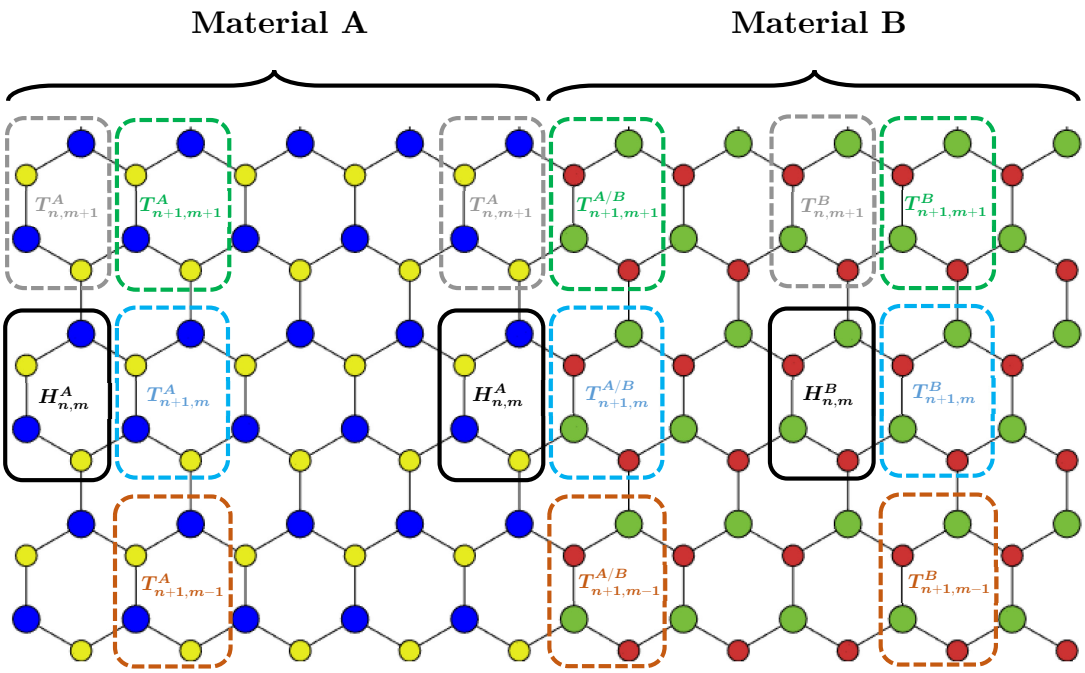


Figure 49. Heterojunction between TMDs A (left) and B (right), and the couplings considered

The coupling matrices at the interface are therefore calculated as

$$T^{A/B}_{n+1,m} = \frac{T^{A}_{n+1,m} + T^{B}_{n+1,m}}{2} \tag{46}$$

$$T^{A/B}_{n+1,m-1} = \frac{T^{A}_{n+1,m-1} + T^{B}_{n+1,m-1}}{2} \tag{47}$$

$$T^{A/B}_{n+1,m+1} = \frac{T^{A}_{n+1,m+1} + T^{B}_{n+1,m+1}}{2} \tag{48}$$

where A(B) is the TMD on the left (right) side of the interface as shown in Figure 49. In the end, the layer coupling Hamiltonians $T^{A/B}_{n+1}$ and $T^{A/B}_{n-1}$ are therefore

$$T^{A/B}_{n+1}(k_y) = T^{A/B}_{n+1,m} + T^{A/B}_{n+1,m-1} \cdot e^{-i.k_y.a_y} + T^{A/B}_{n+1,m+1} \cdot e^{i.k_y.a_y} \tag{49}$$

$$T^{A/B}_{n+1}(k_y) = \frac{T^{A}_{n+1} + T^{B}_{n+1}}{2} \qquad T^{A/B}_{n-1}(k_y) = T^{A/B^{\dagger}}_{n+1}(k_y) \tag{50}$$

Now that all of the necessary layer Hamiltonians have been created, they can be used to determine the device's Green's function which will in turn be used to compute electronic transport through the device.

3.3.2 Integration of the Hamiltonians into NEGF theory

In order to obtain the device's Green's function, the full device Hamiltonian, and the self-energies associated with the contacts must first be calculated since, as a reminder, the device's Green function is calculated as $G(E) = (E + i0^{+} - H_D - \Sigma_L - \Sigma_R)^{-1}$.

From the H_n, T_{n+1} and T_{n-1} matrices, the device Hamiltonian matrix H_D can be constructed as

$$\mathrm{H}_D = \begin{bmatrix} \mathrm{H}_n & \mathrm{T}_{n+1} & 0 & & & & \\ \mathrm{T}_{n-1} & \mathrm{H}_n & \mathrm{T}_{n+1} & 0 & & & \\ 0 & \mathrm{T}_{n-1} & \mathrm{H}_n & \ddots & & & \\ & 0 & \ddots & \ddots & \ddots & 0 & \\ & & & \ddots & \mathrm{H}_n & \mathrm{T}_{n+1} & 0 \\ & & & 0 & \mathrm{T}_{n-1} & \mathrm{H}_n & \mathrm{T}_{n+1} \\ & & & & 0 & \mathrm{T}_{n-1} & \mathrm{H}_n \end{bmatrix}$$

In the case of a heterojunction, H_D can be detailed as

$$\mathrm{H}_D = \begin{bmatrix} H_n^A & T_{n+1}^A & 0 & & & & & \\ T_{n-1}^A & H_n^A & \ddots & & & & & \\ 0 & \ddots & \ddots & T_{n+1}^A & 0 & & & \\ & & T_{n-1}^A & H_n^A & T_{n+1}^{A/B} & 0 & & \\ & & 0 & T_{n-1}^{A/B} & H_n^B & T_{n+1}^B & & \\ & & & 0 & T_{n-1}^B & \ddots & \ddots & 0 \\ & & & & & \ddots & H_n^B & T_{n+1}^B \\ & & & & & 0 & T_{n-1}^B & H_n^B \end{bmatrix}$$

As mentioned in Section 3.2.2.1, the self-energies due to the coupling of the device region with the contacts are calculated as

$$\Sigma_L = \begin{bmatrix} H_{DL}.g_0^L.H_{LD} & 0 & & \\ 0 & 0 & & \\ & & \ddots & \\ & & 0 & 0 \\ & & 0 & 0 \end{bmatrix} \qquad \Sigma_R = \begin{bmatrix} 0 & 0 & & \\ 0 & 0 & & \\ & \ddots & & \\ & & 0 & 0 \\ & & 0 & H_{DR}.g_0^R.H_{RD} \end{bmatrix}$$

which, in our case, becomes

$$\Sigma_L = \begin{bmatrix} T_{n-1}^A.g_0^L.T_{n+1}^A & 0 & & \\ 0 & 0 & & \\ & & \ddots & \\ & & 0 & 0 \\ & & 0 & 0 \end{bmatrix} \qquad \Sigma_R = \begin{bmatrix} 0 & 0 & & \\ 0 & 0 & & \\ & \ddots & & \\ & & 0 & 0 \\ & & 0 & T_{n+1}^B.g_0^R.T_{n-1}^B \end{bmatrix}$$

As a reminder, the left and right surface Green's functions g_0^L and g_0^R are as follows

$$g_0^L = (E + i0^+ - H_n^A - T_{n-1}^A.g_1^L.T_{n+1}^A)^{-1} \quad g_0^R = (E + i0^+ - H_n^A - T_{n+1}^B.g_1^R.T_{n-1}^B)^{-1} \quad (51)$$

and are calculated using the quick iterative scheme mentioned in Section 3.2.2.1.

With both the device Hamiltonian and the self-energies obtained, the device's Green's function matrix could be calculated as

$$G(E) = (E + i0^+ - H_D - \Sigma_L - \Sigma_R)^{-1}$$

However, rather than performing a brute-force inversion of the huge resulting matrix, we use the recursive algorithm presented in Section 3.2.2.2 to compute only the elements of the matrix necessary to obtain the transmission and DOS which helps to drastically reduce computation times.

In order to resolve spatial information such as LDOS, charge, potential etc, a simple 2D mesh adapted to each simulated device is created using the Gmsh software. The lattice parameter of the considered material is used as mesh size, so that each unit cell corresponds to a single mesh element.

3.3.3 Validity of the approximations used

Several approximations are made in this work, mainly that transport is fully ballistic (no phonon scattering is considered), and that the strain is applied uniformly across the device and the contact regions.
This section will provide insight into why these approximations were made, and present supporting material.

- Ballistic approximation: Mean free paths around 20 nm have been reported [461] in MoS_2 so, in the case of short devices, this ballistic approximation is expected to provide reliable results.
  While the deformation potentials reported for TMDs are rather small [462]–[464], phonon scattering would undoubtedly impact performance, namely by reducing ON current and increasing *SS*, depending on the device channel length.

- Uniform strain: in the case of the heterojunctions that give rise in a lattice mismatch, the appropriate strain is applied uniformly to each material, including the contacts, to recover lattice matching across the full device. A more realistic approach to strain modelling would have been to gradually relax the strain away from the interface and consider pristine contacts. However, from a computational standpoint, we would have needed as many different layer Hamiltonians and coupling Hamiltonians as there are layers in the considered system which is extremely taxing, not to mention scaling the mesh size accordingly.
  What's more, in similar heterostructures (WSe_2-MoS_2) strain has been shown to relax over several tens of nanometers[465] (see Figure 50). Considering the length of most of the devices investigated is < 40 nm, the uniformly applied strain approximation is not outlandish.

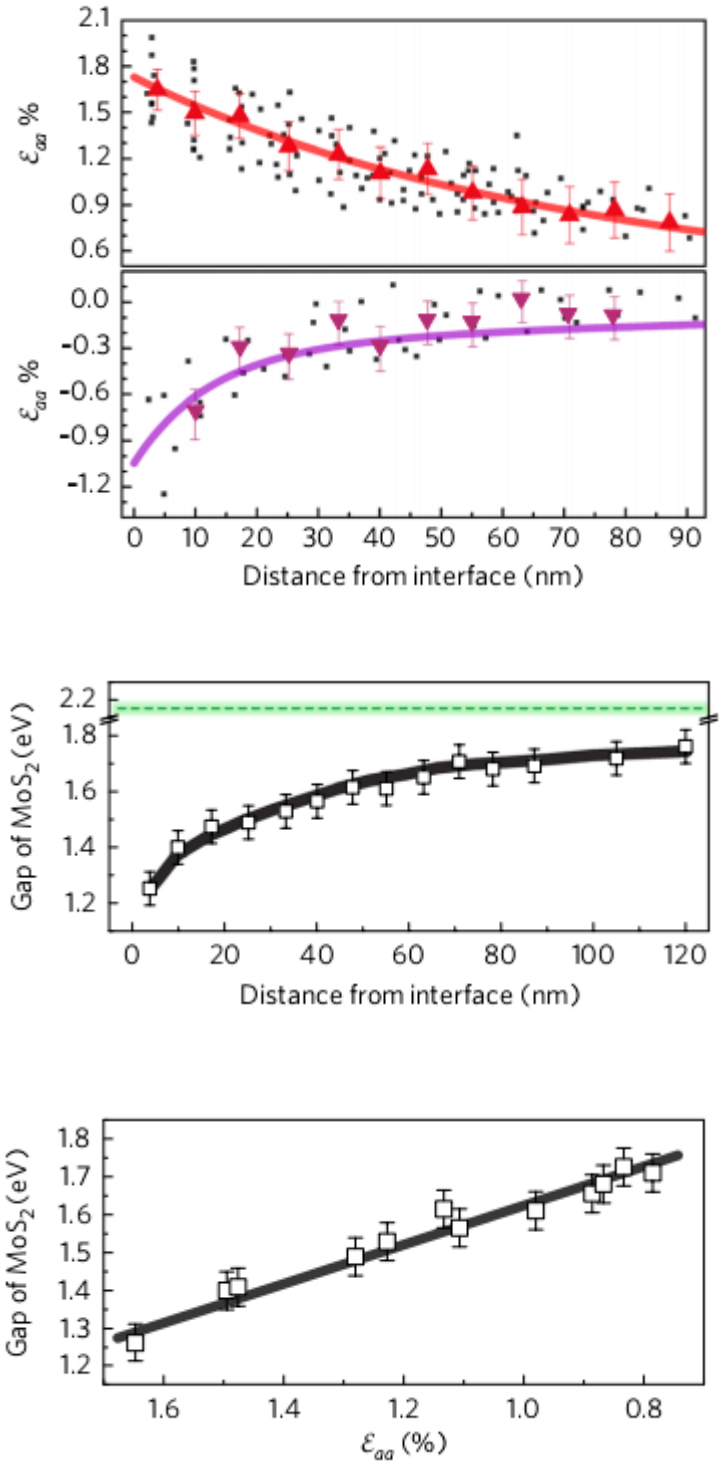


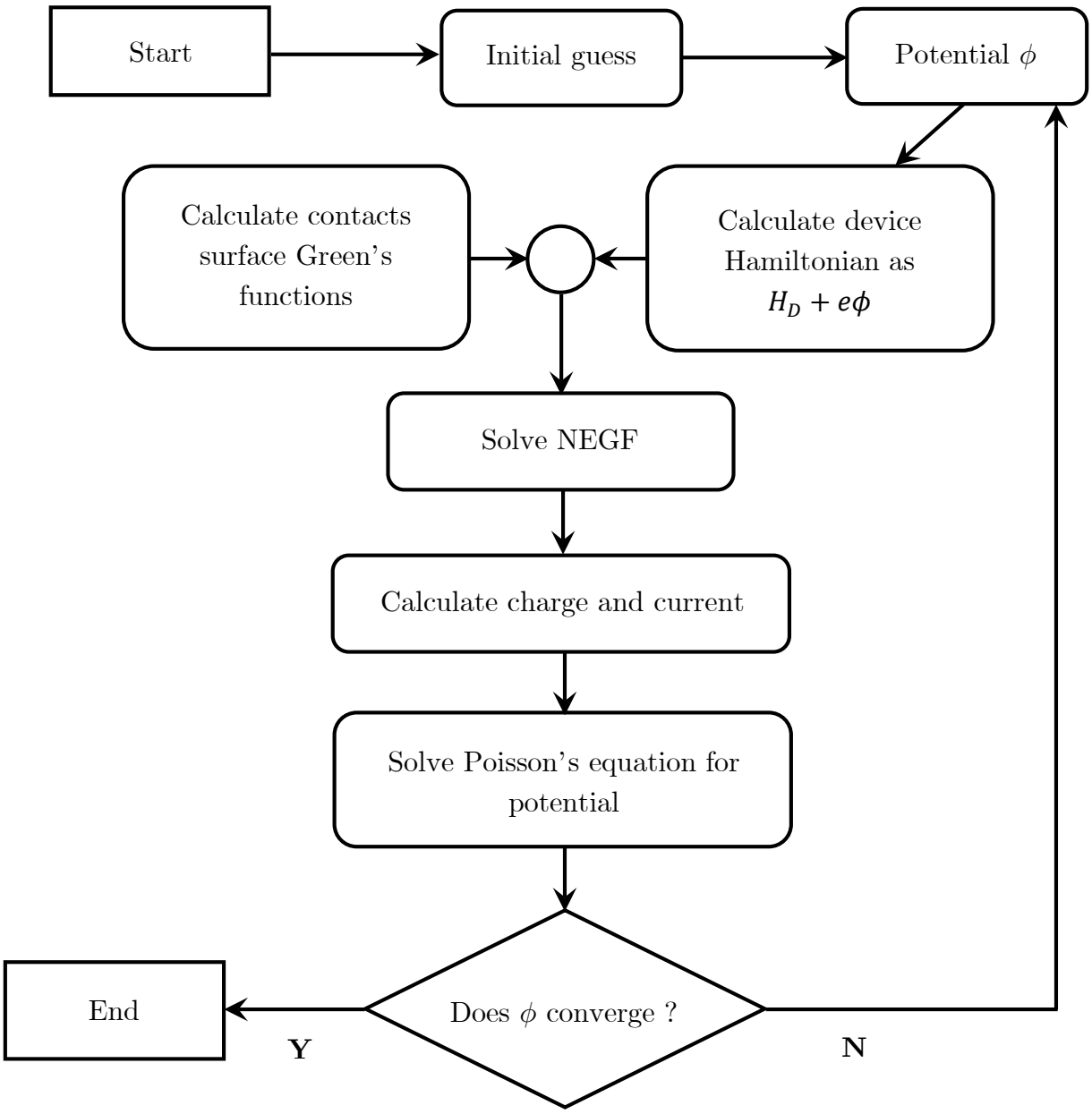
Figure 50. (top) Evolution of tensile and compressive uniaxial strains observed in an experimental MoS_2/WSe_2 in-plane heterojunction as distance to the interface increases. (middle) Evolution of the MoS_2 band gap observed in the same heterojunction as distance to the interface increases (bottom) Evolution of the MoS_2 band gap observed in the same heterojunction as the tensile strain decreases.

3.3.4 Self-consistent transport simulation flowchart

The flowchart for the transport simulation is presented here.
In simplified terms, an initial guess based on the bias voltage is used to compute the initial Green's function of the device, from which the charge and current are extracted.
This charge distribution is then used to calculate the potential via Poisson's equation

$$\nabla.(\varepsilon\nabla.\phi) = -\frac{\rho}{\varepsilon_0} \tag{52}$$

where ϕ is the electrostatic potential and ρ is the charge density. This updated potential profile is used to calculate an updated Green's function for the device, from which a new potential profile is obtained. This loop is repeated until convergence is reached.



Now that the theory behind the TB model and the NEGF method used for transport has been detailed, I will present and analyze the first devices I investigated over the course of my PhD work: homojunction TMD transistors.

Chapter 4

Homojunction TMD transistors

In this chapter, I will quickly present simulation results pertaining to homojunction TMD based transistors (both MOSFET and TFET).
The unremarkable performance of the devices considered in this chapter will be used to highlight and contrast with the outstanding performance of heterojunction-based TFETs. As such, these devices and their performance will not be analyzed in as much detail as those presented in later chapters.

However, this chapter will also be used to introduce important concepts that will also apply to heterojunction TFETs, such as the effect and significance of backgate voltages for instance.

4.1 Homojunction TMD MOSFETs

The first type of devices I investigated were basic, n-type inversion MOSFETs based on a single TMD monolayer. Those devices will give us insight about the limited capabilities of TMDs in traditional MOSFETs.

4.1.1 Device architecture

The MOSFETs presented here all share the same architecture, shown in Figure 51:

- SiO_2 buried oxide with thickness $t_{BOX} = 10 \times a_{MX_2}$ (3.18 nm for MoS_2/WS_2, 3.31 nm for $MoSe_2/WSe_2$ and 3.55 nm for $MoTe_2/WTe_2$).

- High-κ top gate oxide with equivalent oxide thickness $EOT = 4 \times a_{MX_2}$ (1.272 nm for MoS_2/WS_2, 1.324 nm for $MoSe_2/WSe_2$ and 1.42 nm for $MoTe_2/WTe_2$).

- TMD source, channel and drain of lengths L_S, L_{ch} and L_D with $L_S = L_D = 30 \times a_{MX_2}$ (roughly 10 nm) and L_{ch} ranging from $30 \times a_{MX_2}$ to $80 \times a_{MX_2}$ (roughly 26 nm).

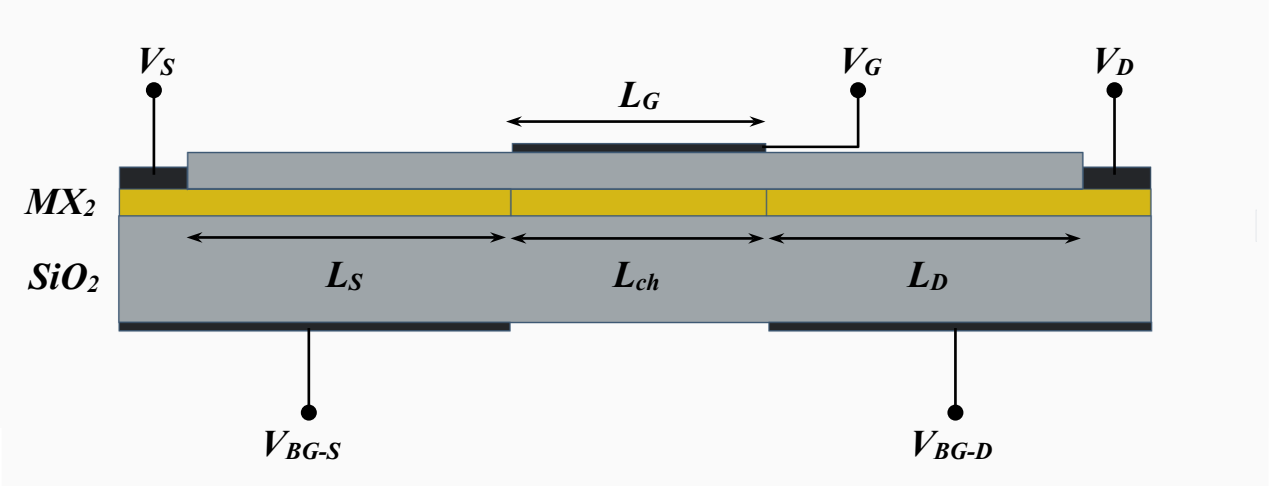


Figure 51. Device architecture for the considered MOSFETs. A single TMD acts as the source, channel and drain, while SiO_2 is used as a buried oxide, and a high-κ dielectric as the top gate oxide.

- Source and drain contacts to which voltages $V_S = 0$ and $V_D = V_{DS}$ are applied which will control the Fermi energies in the contacts.
- A top gate of length $L_G = L_{ch}$, to which a voltage V_G is applied. This gate will control current flow through the device.
- Source and drain backgates to which voltages $V_{BG\text{-}S}$ and $V_{BG\text{-}D}$ are applied. Since the active layer is purely 2D, we can use backgates rather than chemical doping to control charge densities in the contacts.
- The workfunction of the top gate as well as the source and drain backgates in each device is the following: 5.07 eV for MoS_2, 4.71 eV for $MoSe_2$, 4.58 eV for WS_2, 4.31 eV for WSe_2, 4.62 eV for $MoTe_2$ and 4.42 eV for WTe_2.

4.1.2 Electronic transport simulations

Electronic transport simulations across MOSFETs based on MoS_2, $MoSe_2$, WS_2, WSe_2, $MoTe_2$ and WTe_2 were carried out using the self-consistent transport code outlined in Section 3.3.4.
The response of these transistors was studied for gate voltages ranging from 0 to 1.5 V, at a supply voltage $V_{DD} = 0.3$ V, and at backgate voltages $V_{BG\text{-}D} = V_{BG\text{-}S} = 1.9$ V. The gate length L_{ch} is $40\times$ a_{MX_2} so it ranges from 12.72 nm to 14.2 nm depending on the TMD considered. The resulting I_D-V_G characteristics are shown both in log scale and in linear scale in Figure 52.

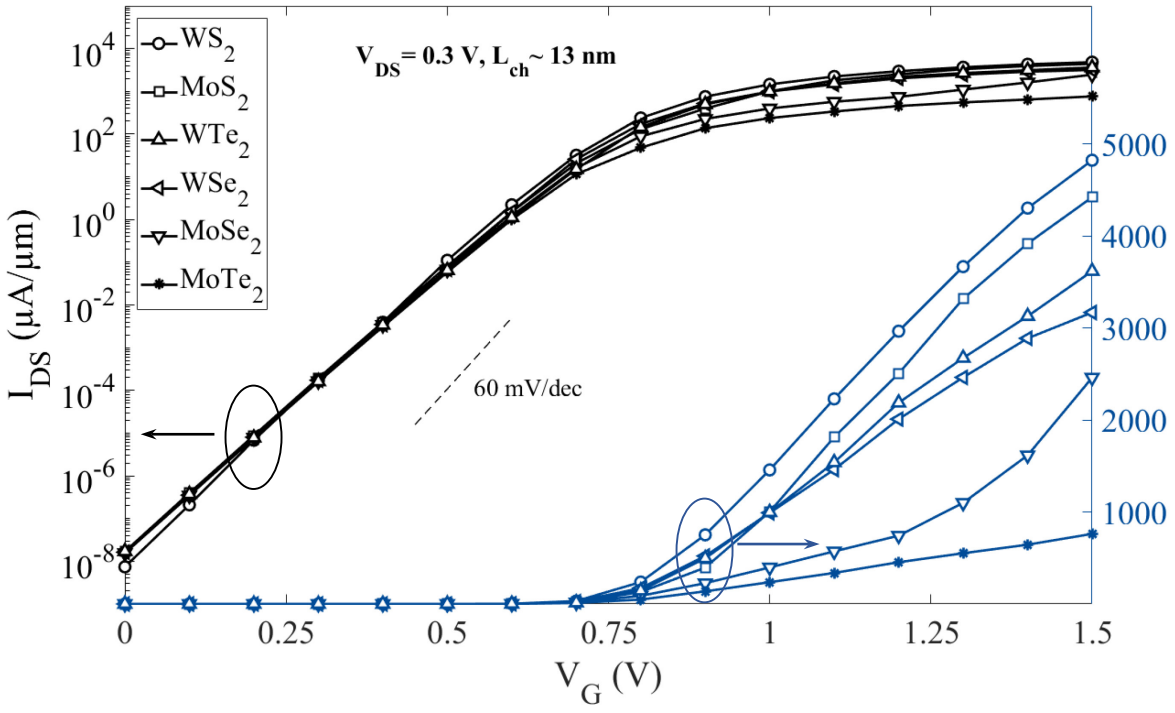


Figure 52. I_D-V_G characteristics of all six TMD-based n-type inversion MOSFETs at V_{DS} = 0.3 V, $V_{BG\text{-}D}$ = $V_{BG\text{-}S}$ = 1.9 V and L_{ch} = 40× a_{MX_2} ~ 13 nm. The dotted line indicates a 60 mV/dec sub-threshold swing, the theoretical lower limit for MOSFETs.

The workfunction of the top gate as well as the source and drain backgates in each device is the following: 5.07 eV for MoS_2, 4.71 eV for $MoSe_2$, 4.58 eV for WS_2, 4.31 eV for WSe_2, 4.62 eV for $MoTe_2$ and 4.42 eV for WTe_2.

The simulated MOSFETs behave as expected, which is to say they are in the OFF state (no current flow) when no gate voltage is applied, and slowly switch to the ON state (current flows from the source to the drain) as V_G increases.
The six transistors share a common threshold voltage V_T ~ 0.75 V, and a sub-threshold swing of roughly 75 mV/dec. As a reminder, SS is evaluated as shown in Eq.(3), between I_{DS} = 10^{-5} and 10^{-2} µA/µm in this case.

Out of all six transistors, the WS_2 and MoS_2 MOSFETs yield the highest ON currents, beyond 4000 µA/µm at V_G = 1.5 V. The WTe_2 and WSe_2 follow closely, yielding ON currents > 3000 µA/µm, while $MoSe_2$ and $MoTe_2$ yield far lower currents.

Figure 53. shows the lowest CB in the MoS_2 MOSFET during the transition from the OFF (V_G = 0 V) to the ON state (V_G = 0.8 V) and highlights the working mechanism of MOSFETs: as V_G increases, the electric field generated by the gate lowers the energy barrier between the source and channel until carriers are able to flow freely across the device.

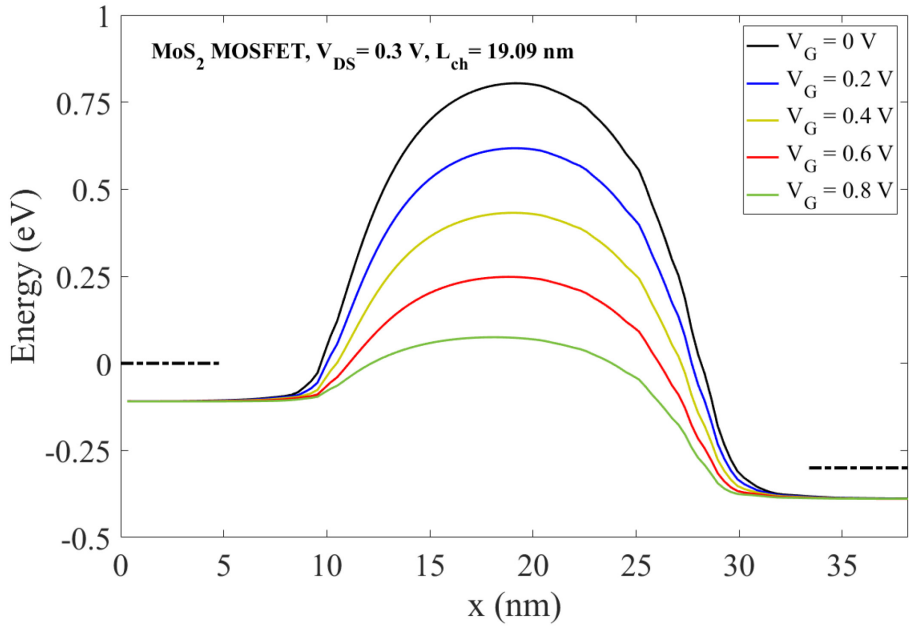


Figure 53. Lowest CB in the MoS_2 MOSFET highlighting the OFF/ON transition at $V_{DS} = 0.3$ V, $L_{ch} = 19$ nm and V_G ranging from 0 to 0.8 V. The black dotted lines indicate the Fermi energies in the source and drain (resp. 0 eV and −0.3 eV).

The influence of design parameters such as channel length and backgate voltages will now be highlighted and briefly investigated.

4.1.2.1 Influence of backgate voltages

As mentioned earlier, we use backgates rather than chemical doping to control charge densities in the contacts because the active layer of the devices is fully 2D. Chemical doping consists of introducing atoms bearing either more or fewer electrons than the base material atoms, therefore increasing the number of electrons or holes available for transport. However, the appearance of defects and atomic reconstruction are a common side-effect of chemical doping, which degrades the transport properties. The use of electrostatic doping via backgates as shown here is therefore preferable whenever possible.

Physically, the backgates are used to force the potential to a certain value ($V_{BG\text{-}S/D}$) and therefore to control the energy level of the bands in the contacts, as well as their relationship with the Fermi energy.
The voltages applied to the backgates must therefore be carefully selected to obtain a functioning device. For instance, by applying an excessively low $V_{BG\text{-}S}$, the lowest CB in the source would be forced at higher energies than μ_S and be partially (or completely) devoid of carriers (see the Fermi-Dirac distribution in Section 1.2.1), which would result in the absence of current. Similarly, applying backgate voltages resulting in the CB being at higher energies in the drain than in the source would prevent current flow.

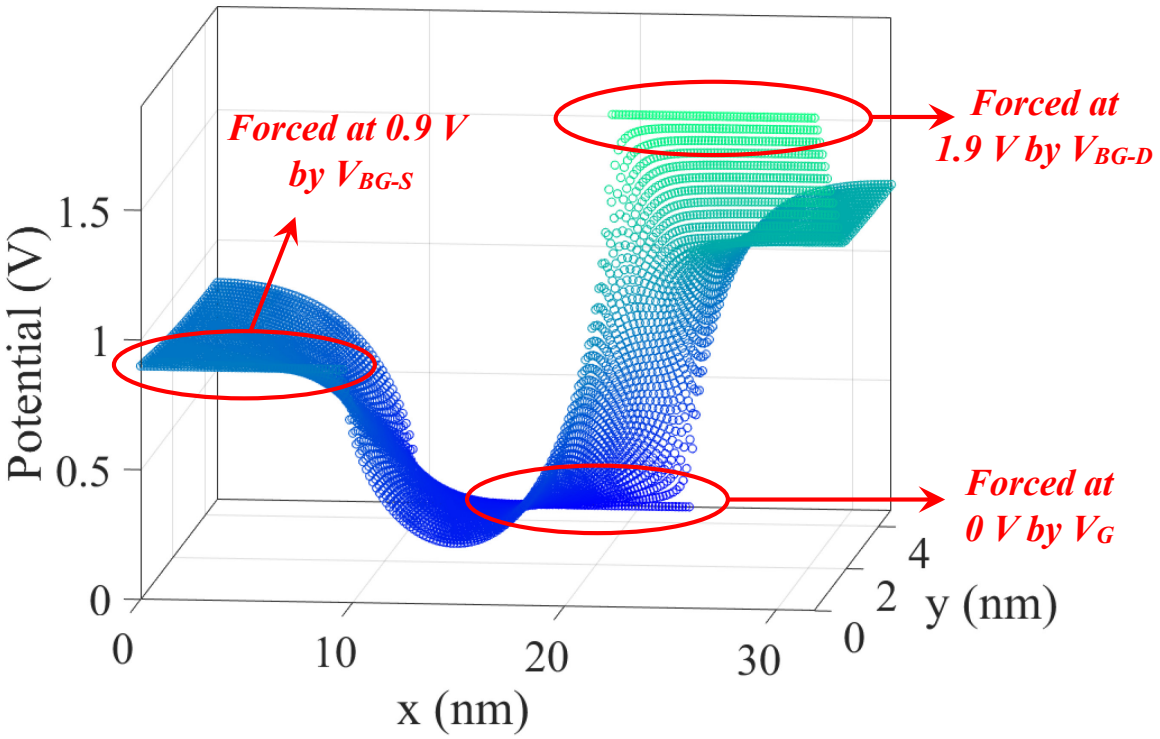


Figure 54. Potential profile in the WS_2 MOSFET at $V_G = 0$ V, $V_{BG-S} = 0.9$V and $V_{BG-D} = 1.9$ V. The active layer (TMD) is located at y = 3.2 nm.

Figure 54 shows the potential profile in the WS_2 MOSFET for $L_{ch} = 12.72$ nm, $V_G = 0$ V, $V_{BG-S} = 0.9$V and $V_{BG-D} = 1.9$ V. The red ellipses highlight the areas where the potential is forced by the gates (left: source backgate, right: drain backgate, bottom: top-gate). The potential profile in the active layer (located at y = 3.2 nm) is therefore highly impacted by all three voltages and will dictate whether current flows or not.

The current characteristics of the WS_2 device were investigated for several backgate voltages ranging from 1.15 V to 2.9 V, and are shown in Figure 55.

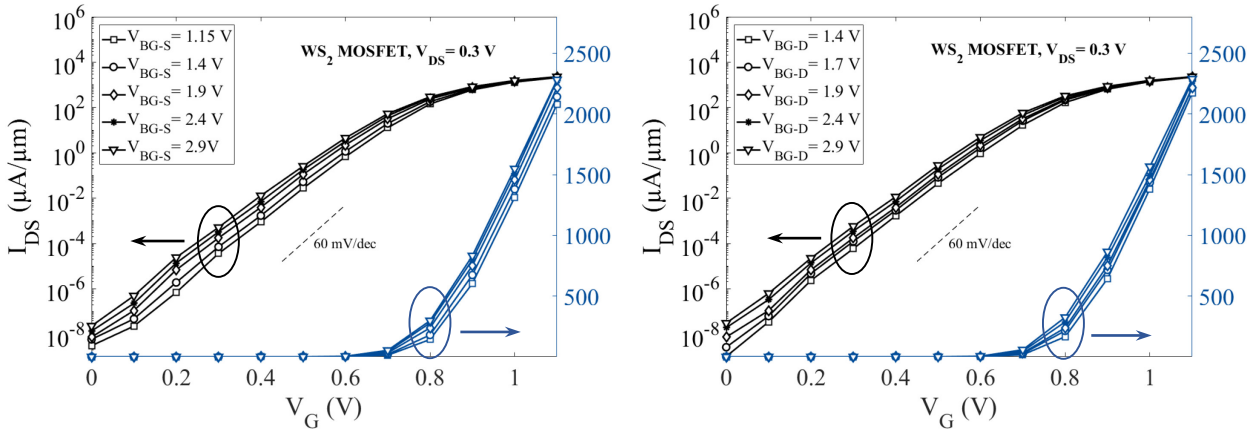


Figure 55. I_D-V_G characteristics for the WS_2 device at $L_{ch} = 12.72$ nm and $V_{DS} = 0.3$ V.
Left: $V_{BG-D} = 1.9$ V and V_{BG-S} ranges from 1.15 V to 2.9 V.
Right: $V_{BG-S} = 1.9$ V and V_{BG-D} ranges from 1.4 V to 2.9 V.

The I_D-V_G characteristics show the mild impact of such changes to both $V_{BG\text{-}S}$ and $V_{BG\text{-}D}$ to device operation. The overall behavior remains the same, but the OFF state is more impacted than the ON state: by applying low backgate voltages, the OFF current can be reduced ten-fold (compared to $V_{BG\text{-}S/D} = 2.9$ V) while only marginally impacting ON current.
While only the WS_2 device is investigated here, the influence of $V_{BG\text{-}S/D}$ is observed to be the same across all six devices.

In the case of these MOSFETs, the backgate voltages act as a fine-tuning tool to slightly enhance performance as long as they are kept in the appropriate range.

4.1.2.2 Influence of channel length

Channel length is another important design parameter in FETs. As channel length decreases, short-channel effects (SCE) such as carrier velocity saturation, high DIBL, source-to-drain tunneling and more can arise and degrade device performance.

The performance of the TMD-based MOSFETs was therefore investigated for gate lengths ranging from $30 \times a_{MX_2}$ (roughly 12 nm) to $80 \times a_{MX_2}$ (roughly 26 nm).

The lowest CB of these two MoS_2 MOSFETs for V_G ranging from 0 V to 0.8 V is shown in Figure 56 and gives strong indications on the behavior of these devices.
At $V_G = 0$ V, the top of the CB barely reaches 0.45 eV in the short-channel device while it exceeds 0.75 eV in the long-channel device; we can therefore expect an increase in OFF current (both by thermionic injection and by tunneling through the shorter energy barrier) as channel length is reduced.

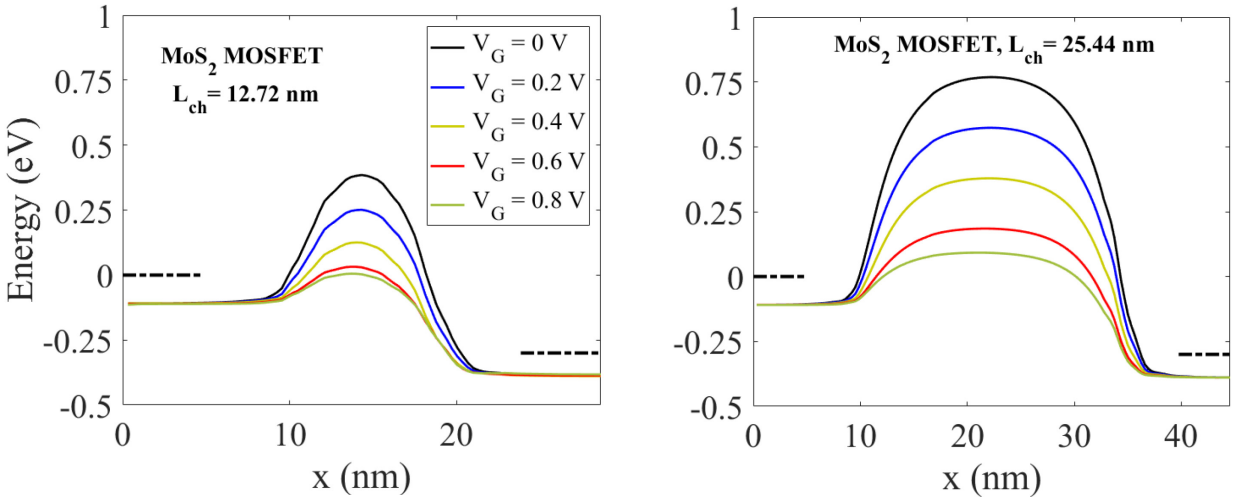


Figure 56. Lowest CB in the MoS_2 MOSFET for V_G ranging from 0 V to 0.8 V, $V_{DS} = 0.3$ V, $V_{BG\text{-}S} = V_{BG\text{-}D} = 1.9$ V, and (left) $L_{ch} = 12.72$ nm (right) 25.44 nm.

This lower energy barrier is due to the fact that the drain backgate (which forces the potential and the level of the CB in the drain) is much closer to the source when the channel is short, and therefore prevents the CB from reaching high energies in the channel.

The I_D-V_G characteristics of all six MOSFETs are shown at $L_{ch} = 30 \times a_{MX_2}$, $40 \times a_{MX_2}$, $60 \times a_{MX_2}$ and $80 \times a_{MX_2}$, $V_{DS} = 0.3$ V and $V_{BG\text{-}S/D} = 1.9$ V are shown in Figure 57.

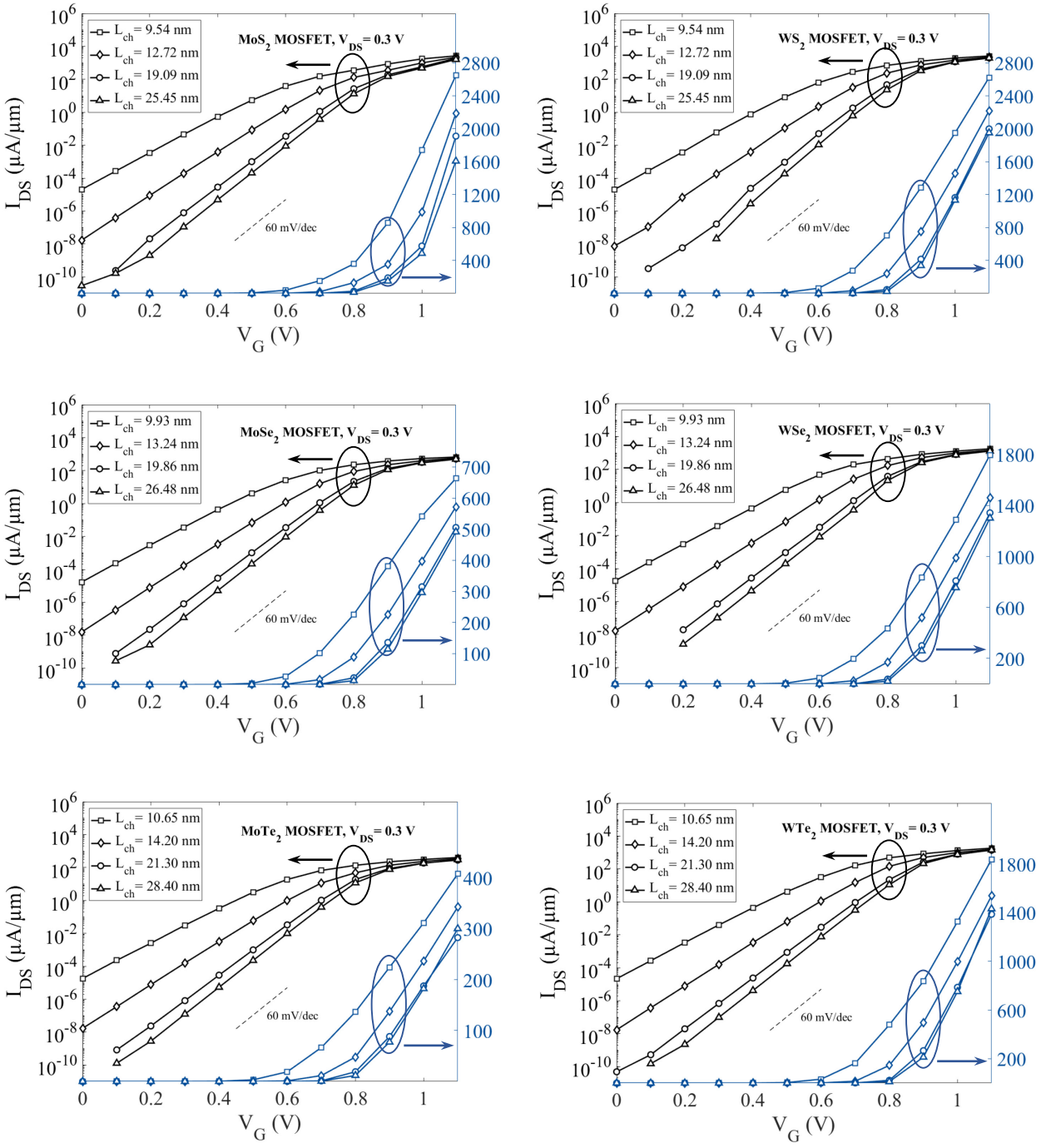


Figure 57. I_D-V_G characteristics for all six devices, with L_{ch} ranging from 10 to 28 nm, $V_{DS} = 0.3$ V and $V_{BG\text{-}S/D} = 1.9$ V.

The same behavior is observed in all devices and is the one expected from investigating the CB profiles in Figure 56.

In the case of the shortest channel, the device can hardly be fully turned OFF, yielding currents around $I_{DS} = 2.10^{-5}$ µA/µm at $V_G = 0$ V due to the low energy barrier and carrier tunneling straight from source to drain as evidenced by the LDOS and current density shown in Figure 58.

However, as channel length increases, the OFF current strongly decreases, and can even be reduced by a factor of up to 10^6 at low V_G due to the increased barrier height and electrostatic integrity of the channel.

Sub-threshold swing is also impacted by L_{ch}: a high 85 mV/dec SS is observed in the case of the shortest channel, while the theoretical lower limit of 60 mV/dec is reached by the devices bearing the 28 nm channel; this highlights the fact that in the case of the longest channel, current in the OFF state is purely due to the thermionic injection of carriers above the barrier, while tunneling strongly contributes to the OFF current observed in the short-channel devices (see the current densities shown in Figure 58).

Finally, L_{ch} also influences the threshold voltage V_T of these devices, which can once again be explained by the increased proximity of the drain backgate voltage and its influence on the CB in the channel. As a result, $V_T \sim 0.65$ V in the short-channel devices compared to ~ 0.85 V in the case of the longer-channels. Even though V_T increases with channel length, the ON current at a given $V_G = V_T + V_1$ remains unchanged.

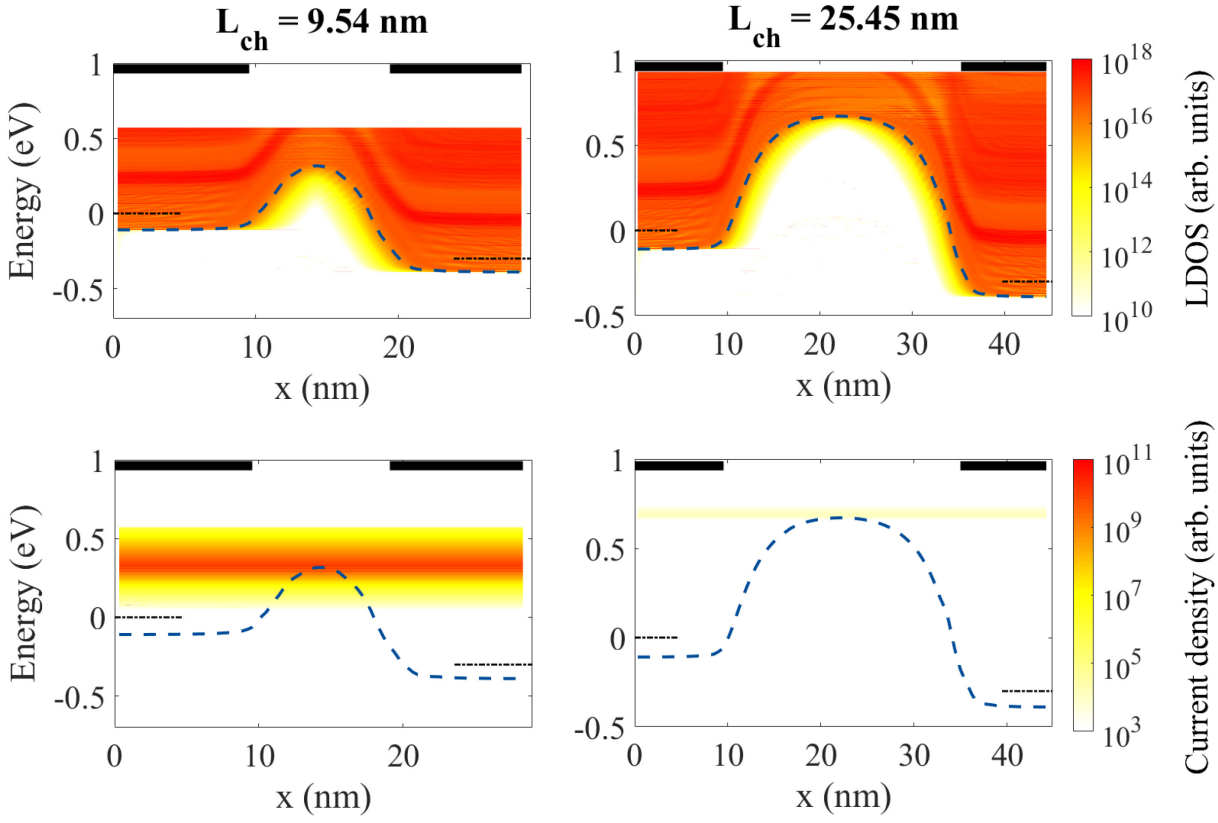


Figure 58. LDOS (top) and current density (bottom) in the MoS_2 MOSFET in the OFF state ($V_G = 0.2$ V), at $V_{DS} = 0.3$ V and $V_{BG\text{-}S/D} = 1.9$ V for (left) $L_{ch} = 9.54$ nm and (right) $L_{ch} = 25.45$ nm.

Channel length is therefore identified as an important parameter in the case of these MOSFETs. A short channel (<15 nm) will strongly impact device performance, increasing both the OFF state current and *SS*. However, if the channel length is beyond approximately 20 nm, the device can yield its peak performance both in the OFF and the ON state without any significant drawbacks, in the ballistic approximation.

In the end, these MOSFETs yield somewhat unremarkable performances: their ON currents are respectable, ranging from a couple hundred to several thousand µA/µm (in the ballistic regime), but are no match for today's top of the line Si-based technology. These results are in-line with recent experimental work on such devices: due to their relatively low mobility, TMDs have been all but abandoned in the quest to find a successor to silicon in MOSFET technology.

4.2 Homojunction TMD TFETs

The second type of device investigated in this work is the n-type homojunction TFET. These devices will be presented and investigated even more briefly than the MOSFETs previously mentioned, for reasons that will quickly become obvious.

They will however be useful as they will present the working mechanism of a TFET and, by being used as comparison, highlight the importance of material selection and band alignment in heterojunction-based TFETs.

4.2.1 Device architecture

The device architecture for homojunction TFETs is the same as that of the MOSFETs presented previously (see Figure 51), except that $L_S = 50 \times a_{MX_2}$ (roughly 16.5 nm).
The main difference when it comes to operating the device will be the voltages applied to the source and drain backgates. In an n-type TFET, carriers tunnel from the source VB to the channel CB. The backgates, which control the profile of the electronic bands, must therefore be set to appropriate voltages (allowing for an energy interval to be both below the top of the source VB and above the bottom of the channel/drain CB). Therefore, the source backgate voltage will be strongly negative, so that the source VB will be pushed upwards towards μ_F, while the drain backgate voltage will remain positive, as was the case in the studied MOSFETs.

4.2.2 Considered TMDs

As TFETs rely on BTBT as a working mechanism, the band gap of the material used will be directly related to the length of the depletion region (the region through which carriers will tunnel from the source VB to the channel CB).
If the band gap is too wide, no amount of gate voltage will allow carriers to tunnel through the resulting depletion region.

In the TB model used, MoS_2, $MoSe_2$, WS_2 and WSe_2 all have band gaps wider than 1.6 eV. These wide band gaps induce a long depletion region (>10 nm), no matter the gate and source/drain backgate voltages applied, which prevents the tunneling of carriers and therefore current flow through the device. As such, these materials cannot be used for homojunction TFET operation.
$MoTe_2$ and WTe_2, however, have narrower band gaps at around 1.2 eV and therefore seem more suited for use in homojunction TFETs. The only devices presented in this section are therefore $MoTe_2$ and WTe_2 homojunction TFETs.

4.2.3 Electronic transport simulations

The same transport code was used to simulate electronic transport simulations in the $MoTe_2$ and WTe_2 homojunction TFETs.

Their behavior was studied for gate voltages ranging from $V_G = 0$ V to 1.5 V, at $V_{DS} = 0.3$ V, $L_{ch} = 28.4$ nm and backgate voltages of $V_{BG\text{-}S} = -1.75$ V and $V_{BG\text{-}D} = 0.75$ V.
The corresponding current characteristics are shown in Figure 59.

A few things are immediately obvious from looking at these current characteristics:

- Both transistors yield very low currents: while both homojunction TFETs present "transistor-like" characteristics (clear transition from an OFF to an ON state followed by a current saturation), the resulting ON-state currents are in the nA/µm range for WTe_2 and in the tens of pA/µm for $MoTe_2$. While small, the ON-state current in the WTe_2 device is larger than that of the $MoTe_2$ device by a factor of approximately 10^2, which can be attributed to its slighty narrower band gap.

- In both devices, the sub-threshold swing exceeds 60 mV/dec even though, contrary to MOSFETs, TFETs can in principle yield *SS* below this theoretical limit as detailed in Chapter 1.

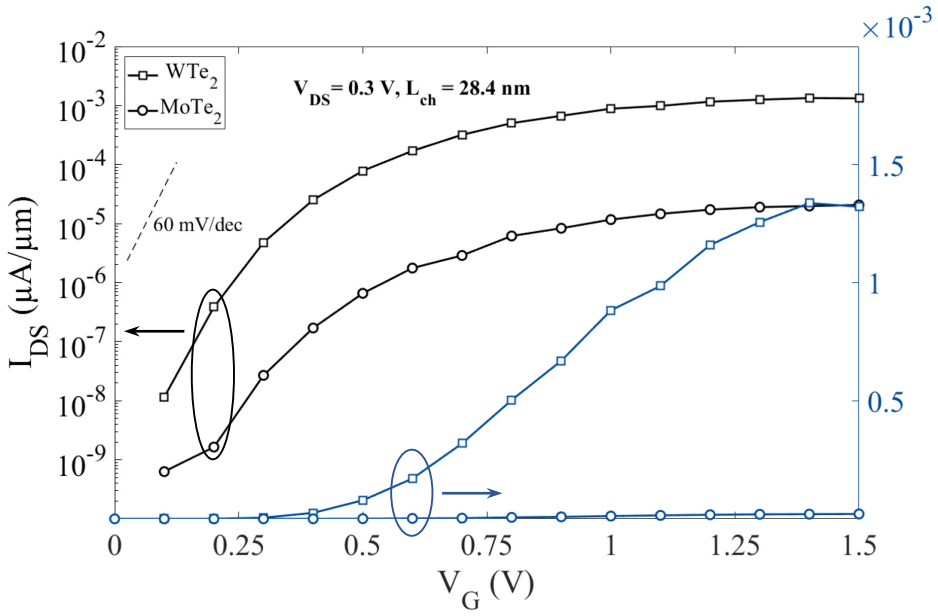


Figure 59. I_D-V_G characteristics of the $MoTe_2$ and WTe_2 homojunction TFETs at $V_{DS} = 0.3$ V, $L_{ch} = 28.4$ nm and backgate voltages of $V_{BG\text{-}S} = -1.75$ V and $V_{BG\text{-}D} = 0.75$ V. The dotted line indicates a 60 mV/dec sub-threshold swing, the theoretical lower limit for MOSFETs.

The overall performance of these devices is therefore extremely poor, and they cannot be used as transistors for CMOS circuits due to their extremely low ON-state currents.

However, they provide a good example and valuable insight into the workings of a TFET as is evidenced by Figure 60 and Figure 61.

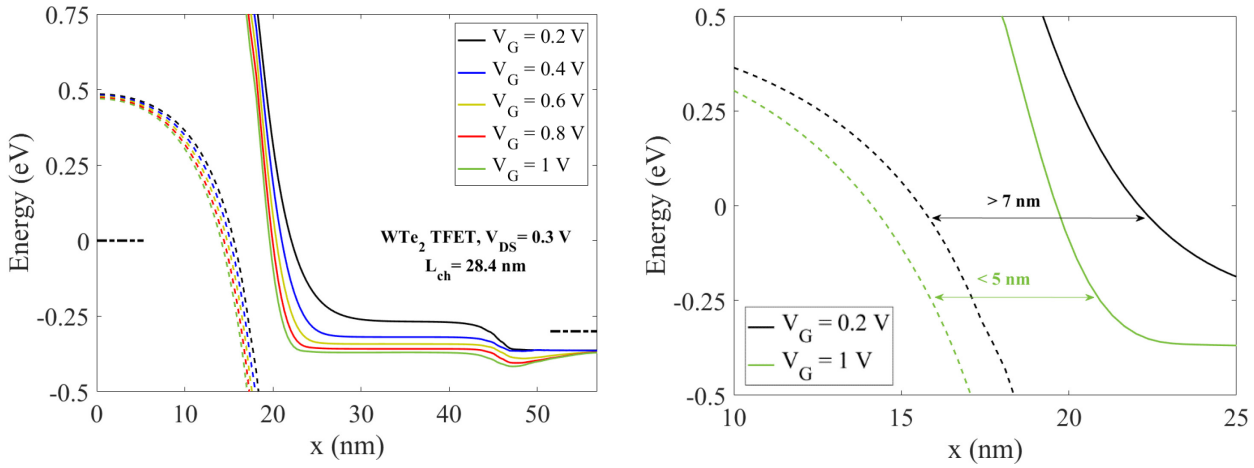


Figure 60. Left: Highest VB (dotted lines) and lowest CB (full lines) in the WTe_2 device at $V_{DS} = 0.3$ V, $L_{ch} = 28.4$ nm and for V_G ranging from 0 V to 0.8 V. Right: Highest VB (dotted lines) and lowest CB (full lines) in the same device, highlighting the length of the depletion region through which carriers must tunnel in the OFF ($V_G = 0$ V) and ON state ($V_G = 0.8$ V).

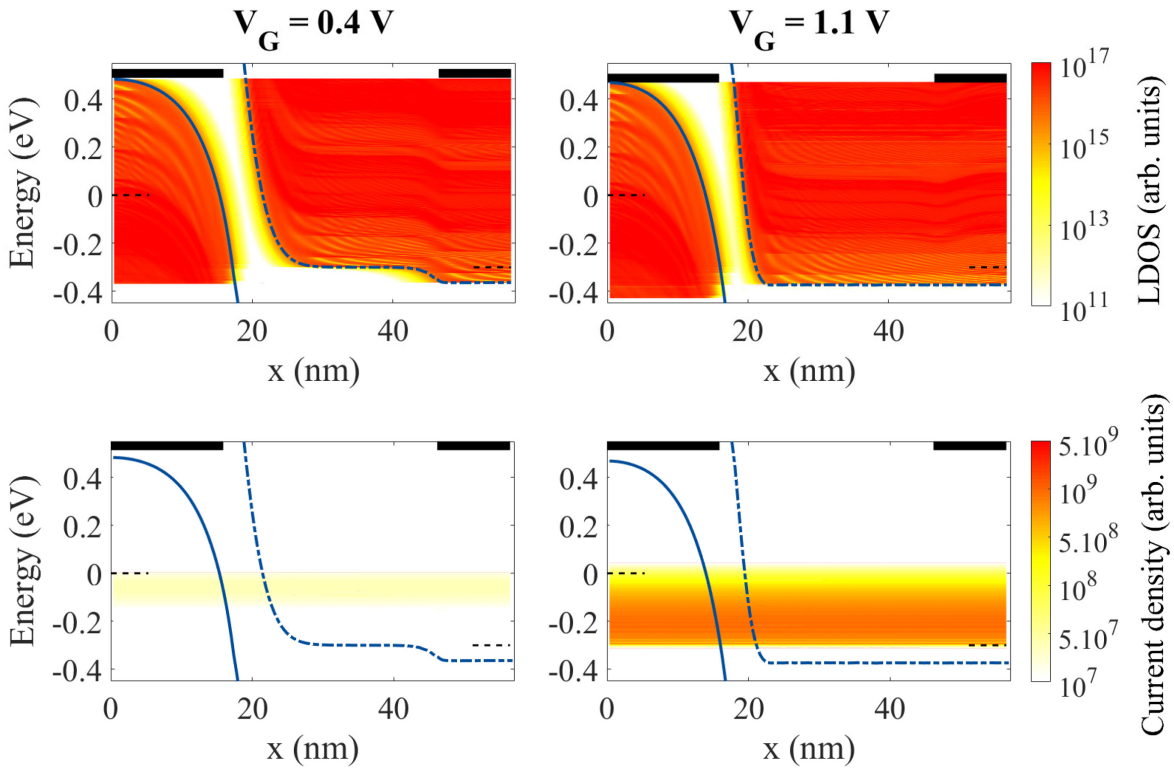


Figure 61. (top) LDOS and (bottom) current density figures in the same WTe_2 device in the (left) OFF and (right) ON state, as well as highest VB (full line) and lowest CB (dashed line). The black bars represent the backgates. The effect of the gate voltage is obvious: as it increases, the length of the depletion region between the source VB and channel CB is reduced and carriers can tunnel through.

Figure 60 shows the highest VB and lowest CB of the WTe_2 device when transitioning from the OFF state ($V_G = 0$ V) to the ON state ($V_G = 0.8$ V), and Figure 61 shows LDOS and current density figures for the same device.
Both figures highlight the effect of the gate voltage on the bands: as V_G is increased, the CB in the channel is pushed towards lower energies, and gets closer to the source VB. As such, the length of the depletion region (the region through which the carriers will have to tunnel) is reduced from over 7 nm in the OFF state, to less than 5 nm in the ON state. This seemingly small change is enough to allow carriers to tunnel from one band to the other, and therefore establish current.

Even though these devices do not yield satisfactory results, the influence of channel length and backgate voltages will now be briefly discussed.

4.2.3.1 Influence of backgate voltages

As explained in Section 4.1.2.1, backgate voltages force the potential to a given value, and therefore control the profile of the bands in the contacts.
In the case of an n-type TFET, the source backgate voltage must be strongly negative, so that the source VB is pushed upwards towards μ_S ($\mu_S = 0$) and in the same energy range as the channel CB.

Figure 62 shows the influence of the source and drain backgate voltages on the current characteristics of the WTe_2 device. $V_{BG\text{-}S}$, which controls the level of the VB in the source, has a strong impact on the behavior of the transistor: as expected, if it is not negative enough only the very top of the VB will be available for tunneling and current will drop significantly. $V_{BG\text{-}D}$, however, has little to no impact on device performance, only slightly impacting ON-state current.

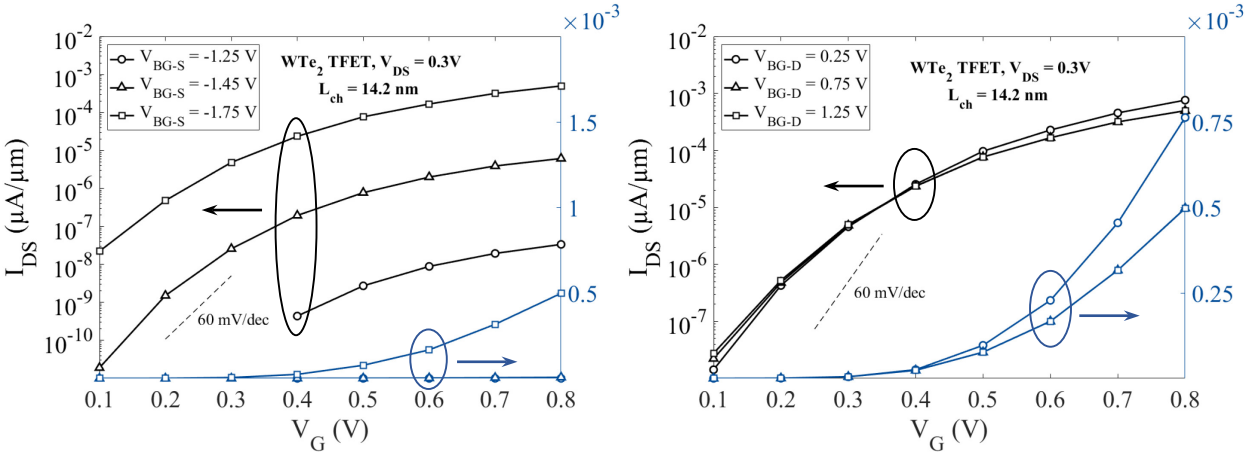


Figure 62. I_D-V_G characteristics for the WTe_2 TFET at $L_{ch} = 14.2$ nm and $V_{DS} = 0.3$ V.
Left: $V_{BG\text{-}D} = 0.75$ V and $V_{BG\text{-}S}$ ranges from -1.25 V to -1.75 V.
Right: $V_{BG\text{-}S} = -1.75$ V and $V_{BG\text{-}D}$ ranges from 0.25 V to 1.25 V.

4.2.3.2 Influence of channel length

As was the case for the MOSFETs presented in Section 4.1, the impact of channel length on the performance of the $MoTe_2$ and WTe_2 homojunction TFETs is briefly investigated here.

I_D-V_G characteristics for both devices with L_{ch} ranging from 5.4 nm to 28 nm are shown in Figure 63.

It is clear that, for channel lengths exceeding roughly 14 nm, the behavior of the transistor is unchanged by L_{ch}, whether in the OFF state or in the ON state.

However, as the channel length approaches 10 nm, the current at extremely low gate voltages increases by a factor of ~10.

Finally, as channel length decreases further (down to 5.3 nm as shown in Figure 63), the OFF state current keeps increasing until the device cannot be properly turned off. This behavior is expected and is due to uncontrolled source-to-drain tunneling, a common short-channel effect which was already observed it in the case of MOSFETs (see Figure 57).

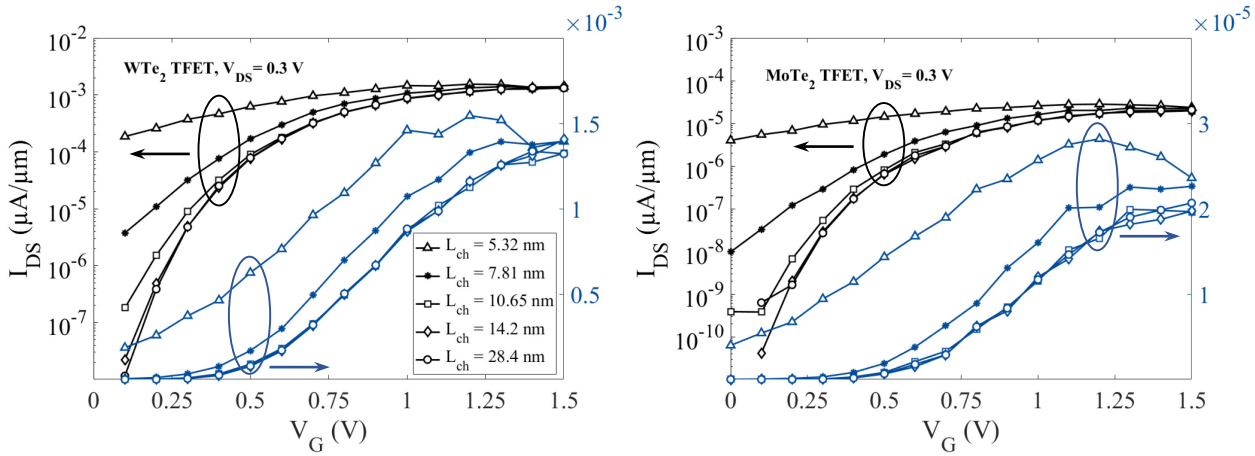


Figure 63. I_D - V_G characteristics of the WTe_2 and $MoTe_2$ devices for L_{ch} ranging from 5 nm to 28 nm at V_{DS} = 0.3 V, $V_{BG\text{-}S}$ = −1.75 V and $V_{BG\text{-}D}$ = 0.75 V; the legend applies to both figures. Source-to-drain tunneling is observed and strongly degrades OFF-state current for channel lengths below.

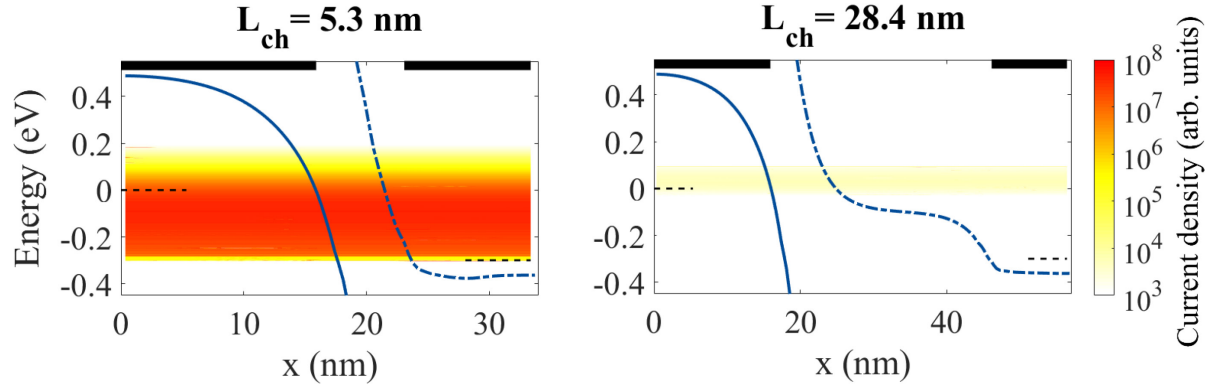


Figure 64. Current density, highest VB (full line) and lowest CB (dashed line) in the WTe_2 device at V_G = 0.1 V for L_{ch} = 5.3 nm (left) and L_{ch} = 28.4 nm. The black bars at the top represent the backgates. In the case of the short channel, the proximity of the drain backgate pulls the CB down in the channel despite the low gate voltage, leading to the tunneling of carriers from the source VB to the channel CB.

The origin of this tunneling at very low gate voltage in the case of extremely short channels is highlighted by Figure 64, which shows current densities for the WTe_2 at $V_G = 0.1$ V for $L_{ch} = 5.3$ nm and $L_{ch} = 28.4$ nm. In the case of the short channel, the increased proximity of the drain backgate, which forces the CB around -0.35 eV in the drain, pulls the channel CB down despite the low gate voltage. The available carriers in the source VB can therefore tunnel and establish current.

While these TMD-based homojunction TFETs yield very weak performance (extremely low ON current and high *SS*) and therefore cannot be used as efficient CMOS transistors, they provided an interesting framework to investigate the overall operation of a TFET, as well as the influence of design parameters such as channel length and backgate voltages, which will be useful when studying the TMD-based in-plane heterojunction TFETs that constitute the main part of my PhD work.
Furthermore, their weak performance will be used as a reference for comparison and will highlight the importance of band alignment in TFETs, as well as the vast potential of the in-plane TMD heterojunctions studied in the coming chapters.

Chapter 5

In-plane heterojunction TFETs

In this Chapter, TFETs based on in-plane heterojunctions of TMDs will be investigated. As was detailed in Section 1.4.1, the band alignment between the source and the drain is paramount in TFETs to achieve high performance.
Using TMD heterojunctions should therefore allow us to "mix-and-match" VB and CB from all six TMDs to obtain the most favorable band alignment.

5.1 Device architecture

The devices presented here all follow the same design, which is very close to that of the homojunction TFETs presented in Section 4.2.1, the only difference being that two different TMDs are used in the active layer: one in the source and another in the channel and drain.
As a reminder, the device architecture (shown in Figure 65) is as follows:

- SiO_2 buried oxide with thickness $t_{BOX} = 10 \times a_{device}$ (will depend on the considered heterojunction).

- High-κ top gate oxide with equivalent oxide thickness $EOT = 4 \times a_{device}$.

- TMD_1 source of length L_S.

- TMD_2 channel and drain of lengths L_{ch} and L_D.

- Source and drain contacts to which voltages $V_S = 0$ and $V_D = -e\,V_{DS}$ are applied and will control the Fermi energies in the contacts.

- A top gate of length $L_G = L_{ch}$, to which a voltage V_G is applied. This gate will control current flow through the device.

- Source and drain backgates to which voltages $V_{BG\text{-}S}$ and $V_{BG\text{-}D}$ are applied. Since the active layer is purely 2D, we can use backgates rather than chemical doping to control charge densities in the contacts.

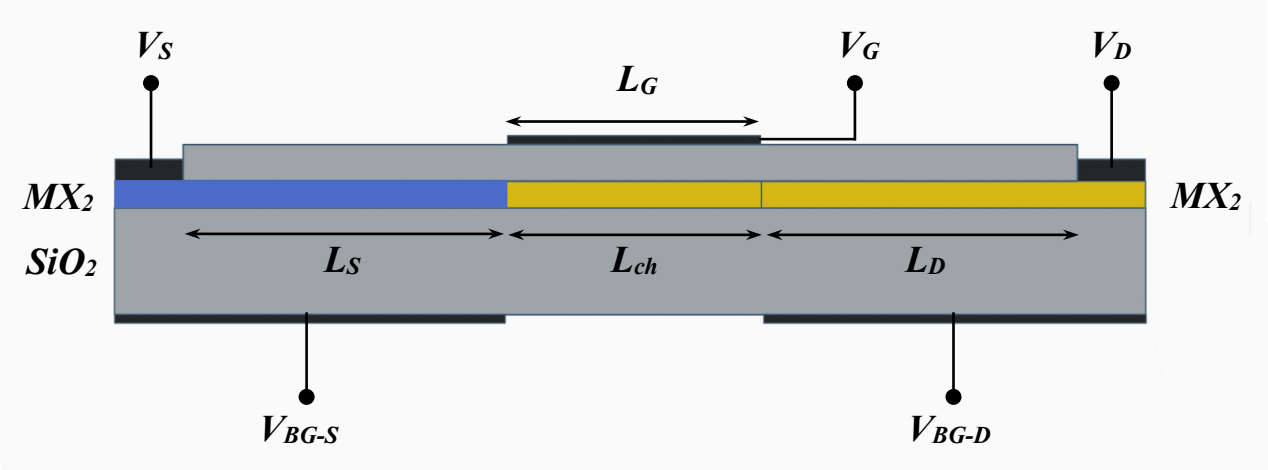


Figure 65. Device architecture for the considered heterojunction TFETs. One TMD acts as the source, and another as the channel/drain. SiO_2 is used as a buried oxide, and a high-κ dielectric as the top gate oxide.

The selection of the TMDs to be used in the source and in the channel/drain region will now be detailed.

5.2 Selection of the TMD heterojunctions

As shown in Section 1.4.1, the band alignment in TFETs is a paramount feature, and selecting the correct TMD pair to be used as a heterojunction is therefore extremely important and will strongly impact device performance.

As a reminder, the band alignment of pristine TMDs, as obtained with the TB model used in this work, is shown in Figure 66.

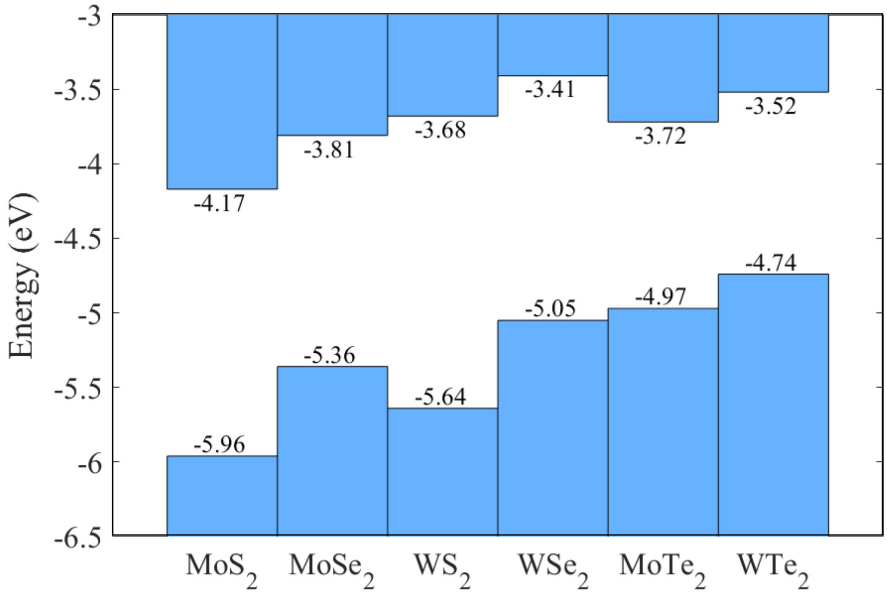


Figure 66. Band alignment in pristine TMDs obtained by using our TB model. The vacuum level is set to 0 eV.

To minimize the length of the depletion region in the considered TFETs, the VB must be as high as possible, while the CB must be as low as possible.
As a result, MoS_2, which yields the lowest CB, will be used as a channel/drain material in all heterojunction TFETs. The resulting heterojunctions and the strains applied to reach lattice matching at the interface are therefore the following:

- $MoSe_2/MoS_2$ and WSe_2/MoS_2: in these heterojunctions, ASe_2 is in its pristine form, while a 4.3% tensile strain is applied onto MoS_2 so that a common lattice parameter is reached at $a_{ASe_2} = 3.31$ Å. The effects of this strain are detailed in 3.1.5, highlighted in Figure 43 and summed up in Figure 67.

- $MoTe_2/MoS_2$ and WTe_2/MoS_2: in these heterojunctions, ATe_2 is under a 5.6% compressive strain, while a 5.3% tensile strain is applied onto MoS_2 so that a common lattice parameter is reached at $a = 3.35$ Å. The effects of this strain are detailed in 3.1.5, highlighted in Figure 44 and summed up in Figure 67.

- The WS2/MoS2 heterojunction is not considered because it results in a roughly 1.5 eV gap between the source VB and channel CB, which is far too high for TFET operation.

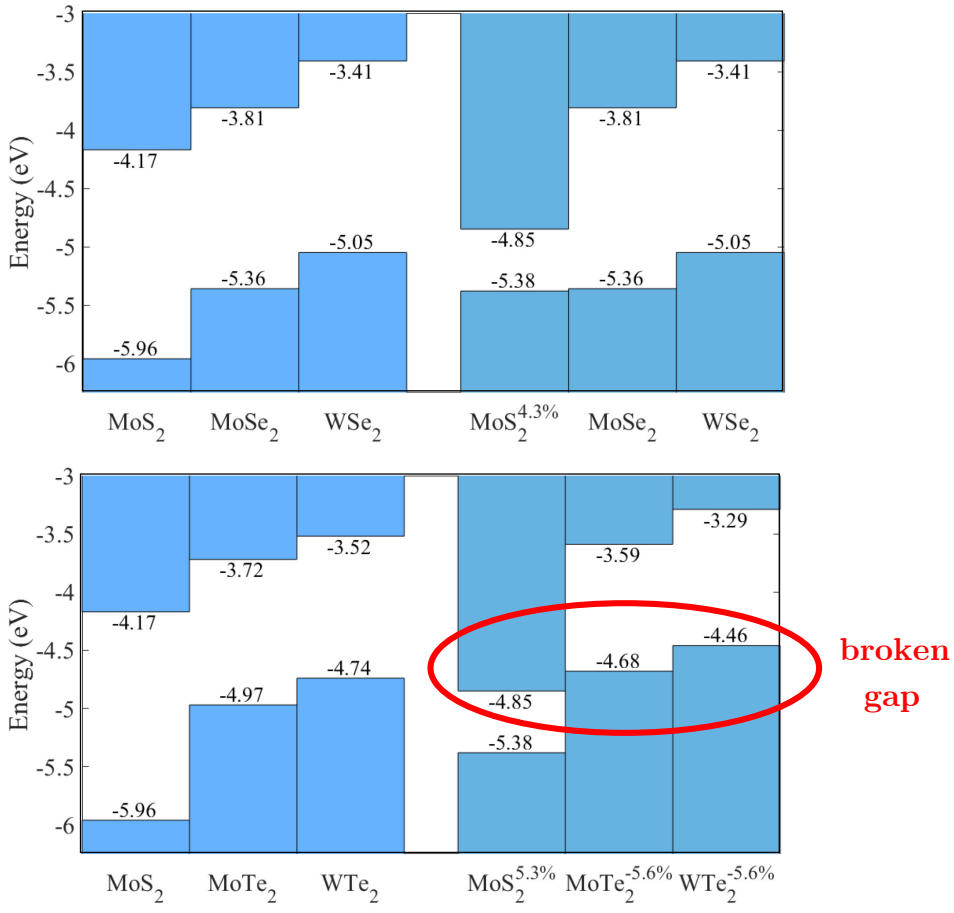


Figure 67. Top: CB and VB of MoS_2, $MoSe_2$ and WSe_2 in their pristine form and under the strain applied in the ASe_2/MoS_2 heterojunctions. Bottom: CB and VB of MoS_2, $MoTe_2$ and WTe_2 in their pristine form and under the strain applied in the ATe_2/MoS_2 heterojunctions.

5.3 Electronic transport simulations

The transport code used previously was slightly adapted to accommodate several materials in the active layer, but the transport calculation and overall flowchart remain unchanged.

5.3.1 Comparison of all four heterojunctions

Before delving deeper into the influence of design parameters such as contact or channel length, or backgate voltages for instance, let us compare the performance of all four considered TMD heterojunction TFETs.

Their performance was studied for gate voltages ranging from $V_G = 0$ V to 0.6 V, at $V_{DS} = 0.3$ V, $L_{ch} = 80 \times a_{device} \sim 27$ nm, $L_S = L_D = 50 \times a_{device} \sim 16.5$ nm and backgate voltages depending on the heterojunction considered (the work-function W_G of the metal used as top-gate and both backgates is also given):
- $MoSe_2/MoS_2$: $V_{BG\text{-}S} = -1$ V, $V_{BG\text{-}D} = 0.5$ V, $W_G = 4.81$ eV.
- WSe_2/MoS_2: $V_{BG\text{-}S} = -0.5$ V, $V_{BG\text{-}D} = 1$ V, $W_G = 4.91$ eV.
- $MoTe_2/MoS_2$: $V_{BG\text{-}S} = 0.58$ V, $V_{BG\text{-}D} = 0.8$ V, $W_G = 5.19$ eV.
- WTe_2/MoS_2: $V_{BG\text{-}S} = 0.85$ V, $V_{BG\text{-}D} = 1.1$ V, $W_G = 5.19$ eV.

The resulting current characteristics are shown in Figure 68.

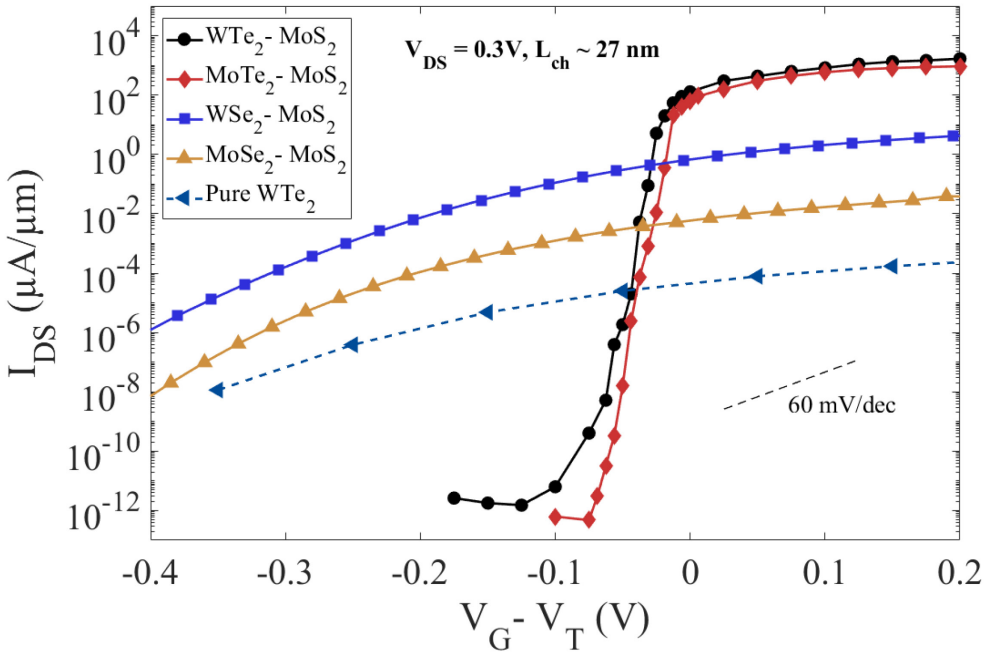


Figure 68. I_D-V_G characteristics for all four heterojunction TFETs as well as the homojunction WTe_2 TFET at $L_{ch} \sim 27$ nm, $V_{DS} = 0.3$ V. The dotted line represents a 60 mV/dec *SS*.

Due to the band alignment of these TMDs, different ranges of gate voltages have to be applied to observe the OFF-ON transition. Therefore, the current characteristics are plotted against V_G - V_T, where V_T is the threshold voltage obtained by the linear approximation of the ON current so that they appear in the same range.

A few things are obvious from the observation of Figure 68:

- In all cases, the heterojunction is beneficial: all heterojunction-based devices yield superior performance compared to the homojunction WTe_2 TFET, which was by far the highest performing homojunction device.
  Most notably, WSe_2 and $MoSe_2$, which could not even function as homojunction TFETs due to their wide band gaps, perform as transistors when used in conjunction with MoS_2.

- $MoTe_2/MoS_2$ and WTe_2/MoS_2 yield by far the best performance: while the two other devices benefited greatly from the heterojunction and now show transistor-like characteristics, the $MoTe_2/MoS_2$ and WTe_2/MoS_2 heterojunctions yield incredibly steep transitions from the OFF to the ON state, and far higher ON currents -in the thousands of µA/µm-.

The large difference in performance between the $MoSe_2/MoS_2//WSe_2/MoS_2$ and the $MoTe_2/MoS_2//WTe_2/MoS_2$ devices can be directly explained by the alignment of the bands in those devices.

The band offset (calculated as $CB_{min} - VB_{max}$, see Figure 67) in each of these heterojunctions is given in Table 2 alongside figures of merit such as the length of the depletion region in the ON state, I_{ON}/I_{OFF}, and sub-threshold swing (I_{ON} is calculated at $V_G = V_{OFF} + V_{DD}$, where $V_{DD} = 0.3$ V and V_{OFF} is V_G for which $I_{DS} = 10^{-5}$ µA/µm and SS is estimated between $I_{DS} = 10^{-5}$ µA/µm and $I_{DS} = 10^{-2}$ µA/µm). This table highlights the strong correlation between the band offset in the considered heterojunction and the performance of the corresponding TFET.

	$MoSe_2/MoS_2$	**WSe_2/MoS_2**	**$MoTe_2/MoS_2$**	**WTe_2/MoS_2**
Band offset (eV)	0.51	0.2	−0.17	−0.39
$L_{depletion}$ (nm)	5.3	4.4	~0	~0
I_{ON}/I_{OFF}	8.7×10^2	2.5×10^4	9.8×10^7	2.0×10^8
SS (mV/dec)	106	55	4	3

Table 2. Band offset and transport performance (depletion region length in ON state, I_{ON}/I_{OFF} and SS) in the four in-plane heterojunction TFETs at $V_{DD} = 0.3$ V.

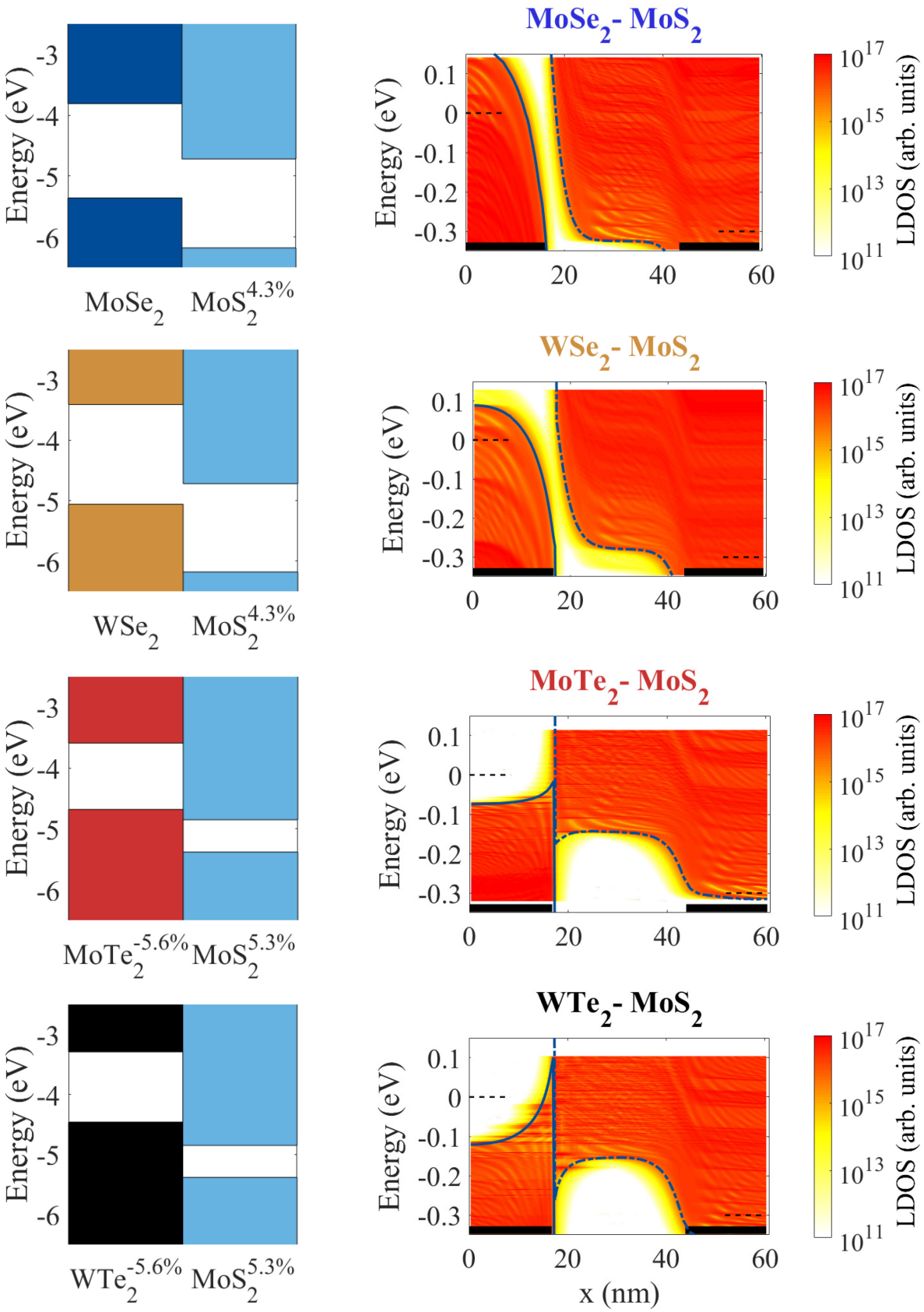


Figure 69. Left: Source VB and channel CB in each heterojunction, highlighting their band alignment. Right: LDOS in the ON state ($V_G = 0.5$ V) for each heterojunction, highlighting the depletion region through which carriers must tunnel. Full (dotted) blue lines indicate the VB (CB), dotted black lines indicate the Fermi levels in the contacts, and black bars represent the source and drain backgates.

The band alignments and LDOS maps shown in Figure 69 highlight the influence of the band offset on the length of the depletion region, and therefore on the performance of the device. In the case of a broken gap ($MoTe_2/MoS_2$ and WTe_2/MoS_2) the depletion region is almost non-existent, which allows the TFET to yield an extremely steep OFF-ON transition as well as high ON currents in the thousands of µA/µm, even at a low supply voltage of 0.3 V.

It is worth noting that the performances shown for the $MoSe_2/MoS_2$ and WSe_2/MoS_2 devices in Figure 68 were obtained by optimizing contact length, channel length and backgate voltages, and therefore represent the peak performances registered for these devices, both in terms of *SS* and ON current. Still, those performances are weak at best, with *SS* around or beyond 60 mV/dec and I_{ON}/I_{OFF} ratios below 10^5.

For this reason, the rest of this chapter and manuscript, will focus solely on the $MoTe_2/MoS_2$ and WTe_2/MoS_2 heterojunctions, which yield far more promising performances with *SS* below 5 mV/dec and I_{ON}/I_{OFF} around 10^8.

5.3.2 Influence of contact length

The length of the source and drain contacts may have a strong influence on the potential in the device and therefore the profile of the bands due to the corresponding backgates. If the contact is too short, the potential cannot adapt as it should, which modifies the profile of the bands in the contacts and possibly even in the channel. As a result, the computed current will be impacted, mainly in the OFF state.
The goal is therefore to identify the shortest contact lengths that do not impact the profile of the bands and the performance of the device. The results presented thereafter were obtained in the $MoTe_2/MoS_2$ heterojunction device with $V_{DS} = 0.3$ V, $L_{ch} = 20.1$ nm, $V_{BG\text{-}S} = 0.58$ V and $V_{BG\text{-}D} = 0.8$ V. While the results presented in this section pertain to the $MoTe_2/MoS_2$ device, the same observations were made for the WTe_2/MoS_2 device.

We first investigate the influence of the source contact, by modulating its length from 10 nm to 23.5 nm. The resulting I_D-V_G characteristics, as well as the profile of the highest VB and lowest CB, are shown (for $L_D = 10.05$ nm) in Figure 70.

It is clear that a 10 nm source is too short:

- Currents in the OFF state increase by a factor of approx. 10^3 compared to the devices with longer source contacts.
- The highest VB in the source is not forced at the same energy at x = 0 as in the case of longer contacts.

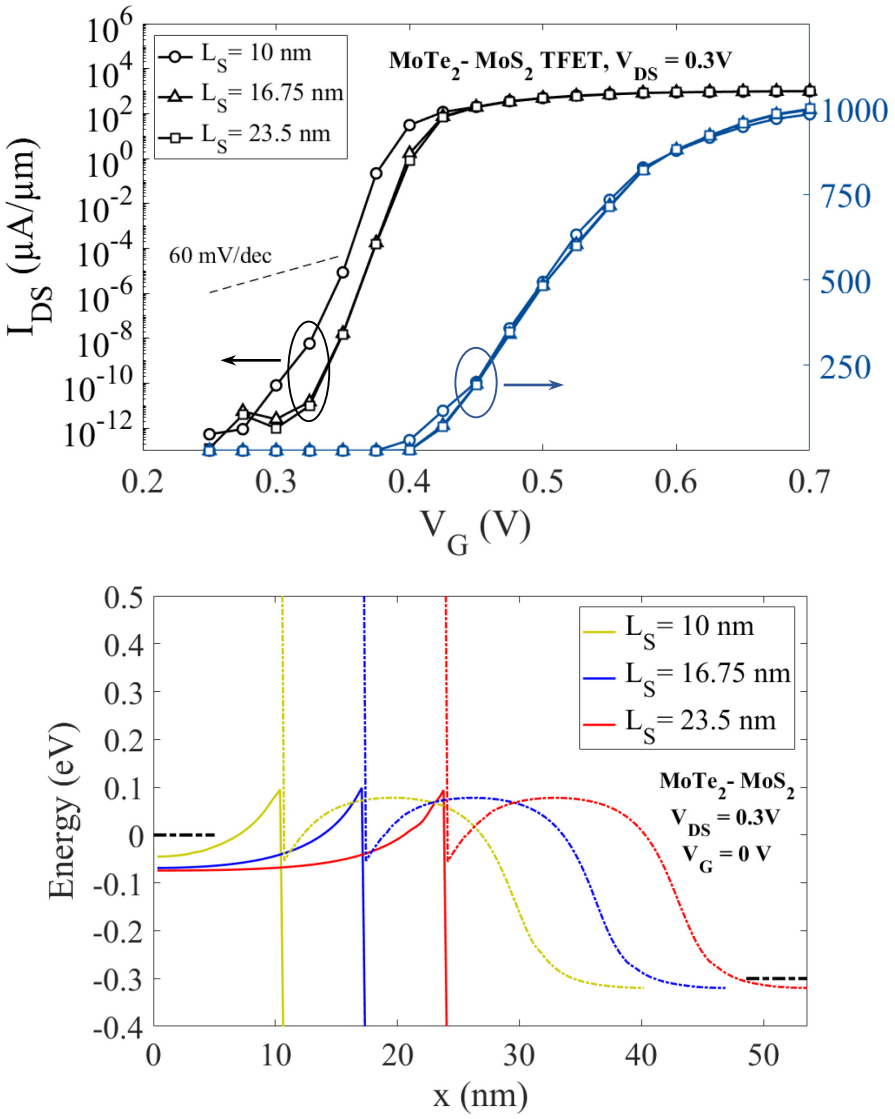


Figure 70. Influence of L_S on the $MoTe_2/MoS_2$ device. Top: I_D-V_G characteristics at $V_{DS} = 0.3$V, $L_{ch} = 20.1$ nm, $V_{BG\text{-}S} = 0.58$ V and $V_{BG\text{-}D} = 0.8$ V. Bottom: Highest VB (full lines) and lowest CB (dashed lines) for the same device, at $V_G = 0$ V.

A 16.75 nm source however, seems to be ideal. Compared to the device bearing an even longer source, the currents are not impacted whether in the OFF or the ON state, and the highest VB is also forced at the same energy at x = 0 although barely; this indicates that an even shorter source contact would likely be too short and impact the performance of the device.

As a result, a source length of $L_S = 16.75$ nm will be used in all of the devices investigated. A similar study was performed to identify the appropriate drain contact length.

I_D-V_G characteristics and the profile of the highest VB and lowest CB, are shown for $L_S = 16.75$ nm and L_D ranging from 6.7 nm to 16.75 nm in Figure 71.

While a drain contact of 6.7 nm does not impact current, the lowest CB in the drain is not forced at the same energy as the devices with longer contacts and, which can be an issue at higher drain backgate voltages.

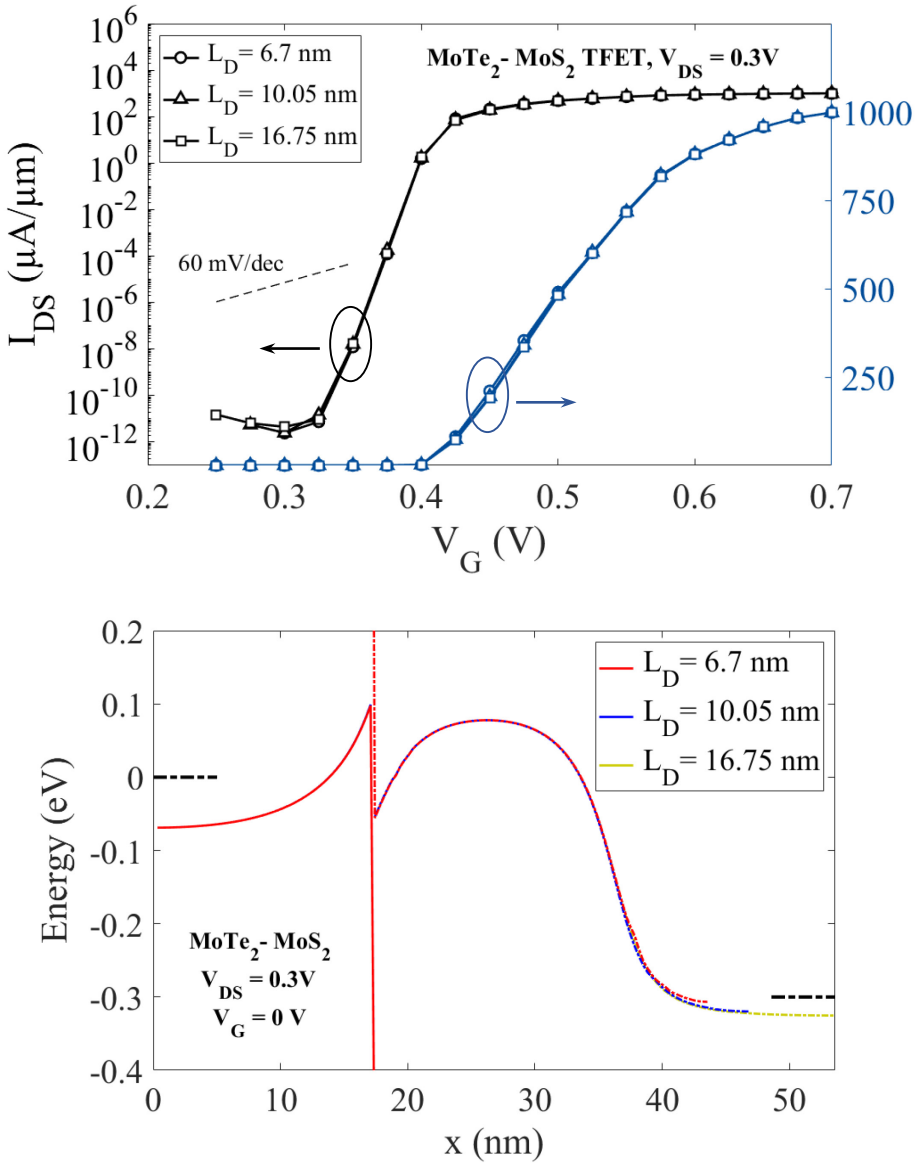


Figure 71. Influence of L_D on the $MoTe_2/MoS_2$ device. Top: I_D-V_G characteristics for the at $V_{DS} = 0.3$V, $L_{ch} = 20.1$ nm, $V_{BG\text{-}S} = 0.58$ V and $V_{BG\text{-}D} = 0.8$ V. Bottom: Highest VB (full lines) and lowest CB (dashed lines) for the same device, at $V_G = 0$ V.

Therefore, to make sure the drain will be of an appropriate length no matter the device investigated, I will use a drain contact length of 10.05 nm in all of the devices investigated. Thanks to this quick study of device performance and band profile, I was able to determine contact lengths that ensure a proper resolution of the potential while remaining short nonetheless, so that the need in computational resources is kept at a minimum; while it is not studied here, the negative impact of electron-phonon interactions on device performance will therefore be reduced thanks to this short contact length.
As a reminder, $L_S = 16.75$ nm and $L_D = 10.05$ nm will now be used for all devices. The influence of channel length on device performance will now be studied.

5.3.3 Influence of channel length

In Chapter 4, gate length was identified to strongly impact performance both in the case of the TMD MOSFETs and homojunction TMD TFETs. It is therefore expected to influence device performance in these TMD heterojunction devices.

I_D-V_G characteristics for the $MoTe_2/MoS_2$ and WTe_2/MoS_2 devices at $V_{DS} = 0.3$ V, L_{ch} ranging from 5.025 nm to 26.8 nm, and the following backgate voltages:
- $MoTe_2/MoS_2$: $V_{BG\text{-}S} = 0.58$ V, $V_{BG\text{-}D} = 0.8$ V
- WTe_2/MoS_2: $V_{BG\text{-}S} = 0.85$ V, $V_{BG\text{-}D} = 1.1$ V

are presented in Figure 72.

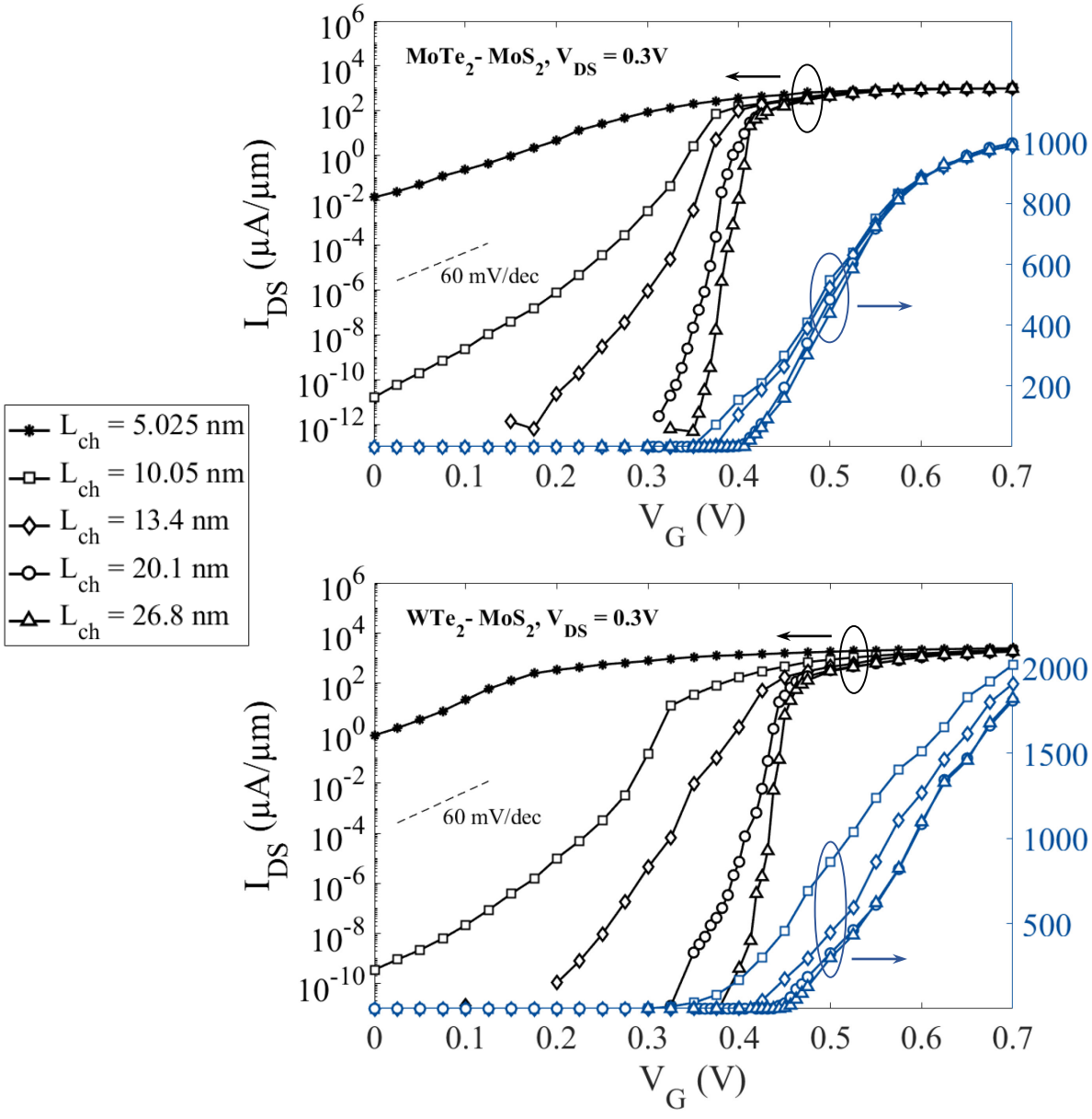


Figure 72. I_D-V_G characteristics for the heterojunction devices at $V_{DS} = 0.3$ V, L_{ch} ranging from 5 nm to 27 nm, $V_{BG\text{-}S} = 0.58$ V and $V_{BG\text{-}D} = 0.8$ V (note that the current at $L_{ch} = 5.025$ nm is only shown in log scale for clarity purposes).

As expected, channel length has a strong impact on the performance of both heterojunction TFETs. In both devices, increasing L_{ch} has several major beneficial effects (in the ballistic limit):

- Strong reduction of the OFF-state current: the log scale plots highlight the huge impact of channel length on OFF-state performance. First, if the channel is too short (5.025 nm), the device cannot be switched off due to source-to-drain tunneling and does not behave like a transistor; a 10 nm-channel, however, is sufficient to observe transistor behavior with a clear OFF-ON transition.
  As the channel length keeps increasing, device performance in the OFF state can be strongly increased: for instance, a 3.35 nm increase of channel length leads to a reduction of the OFF-current by a factor of approximately 10^5 for the WTe_2/MoS_2 device at low gate voltages ($V_G = 0.2$ V). Even more impressively, an increase in channel length from 10.05 nm to 26.8 nm allows the $MoTe_2/MoS_2$ device to be in a fully OFF state at $V_G = 0.35$ V, resulting in a reduction of current by a factor beyond 10^{10} (due to both a decrease in leakage current and a slight increase in threshold voltage).
  These effects can be explained by the band profiles and current density figures shown in Figure 73 and Figure 74. Much like in Section 4.1.2.2 for MOSFETs, the increased proximity of the drain backgate that comes with a short channel pulls the CB down in the channel region, lowering the barrier to be overcome at a given V_G. This effect is compounded by the tunneling of carriers through the top of this barrier (see current density figures), further increasing OFF-state leakage currents.
- Strong decrease in sub-threshold swing: along with this strong decrease in OFF state current comes a dramatic increase of the steepness of the slope in the sub-threshold regime. Figure 75 shows the evolution of SS as a function of channel length in both heterojunction devices. For instance, both devices yield $SS \sim 60$ mV/dec for $L_{ch} \sim 7$ nm, compared to $SS < 5$ mV/dec for $L_{ch} > 25$ nm.
  Once again, this is due to the source-to-drain tunneling that occurs in the case of short channels, which increases OFF-state current and therefore "flattens" the transition from a fully OFF to fully ON state.
  This effect is highlighted by the current density figures mentioned earlier (Figure 74). In the case of a short channel, an increasing number of carriers can tunnel through the top of the channel CB as V_G increases, leading to this steady increase in current. In the case of a long channel however, no such tunneling occurs and the device goes from fully OFF to fully ON state when the threshold voltage is reached.
- Strong increase in I_{ON} (see Figure 75): I_{ON} is calculated at $V_{ON} = V_{OFF} + V_{DD}$ where V_{OFF} is V_G for which $I_{DS} = I_{OFF} = 10^{-5}$ µA/µm. Due to the strong decrease in OFF-state leakage current, V_{OFF} strongly increases with channel length (from 0.2 V at $L_{ch} = 10.05$ nm to 0.425 V at $L_{ch} = 26.8$ nm in the WTe_2/MoS_2 device) and therefore so does V_{ON}. Much like SS, I_{ON} saturates for long channels.

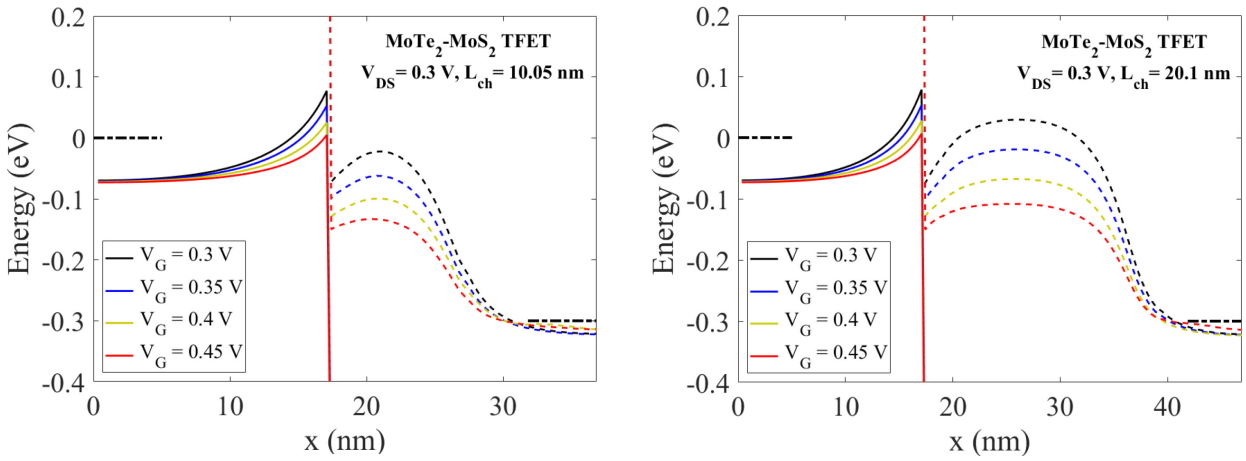


Figure 73. Highest VB (full lines) and lowest CB (dotted lines) during the OFF-ON transition in the $MoTe_2/MoS_2$ device at $V_{DS} = 0.3$ V and (left) $L_{ch} = 10.05$ nm (right) $L_{ch} = 20.1$ nm.

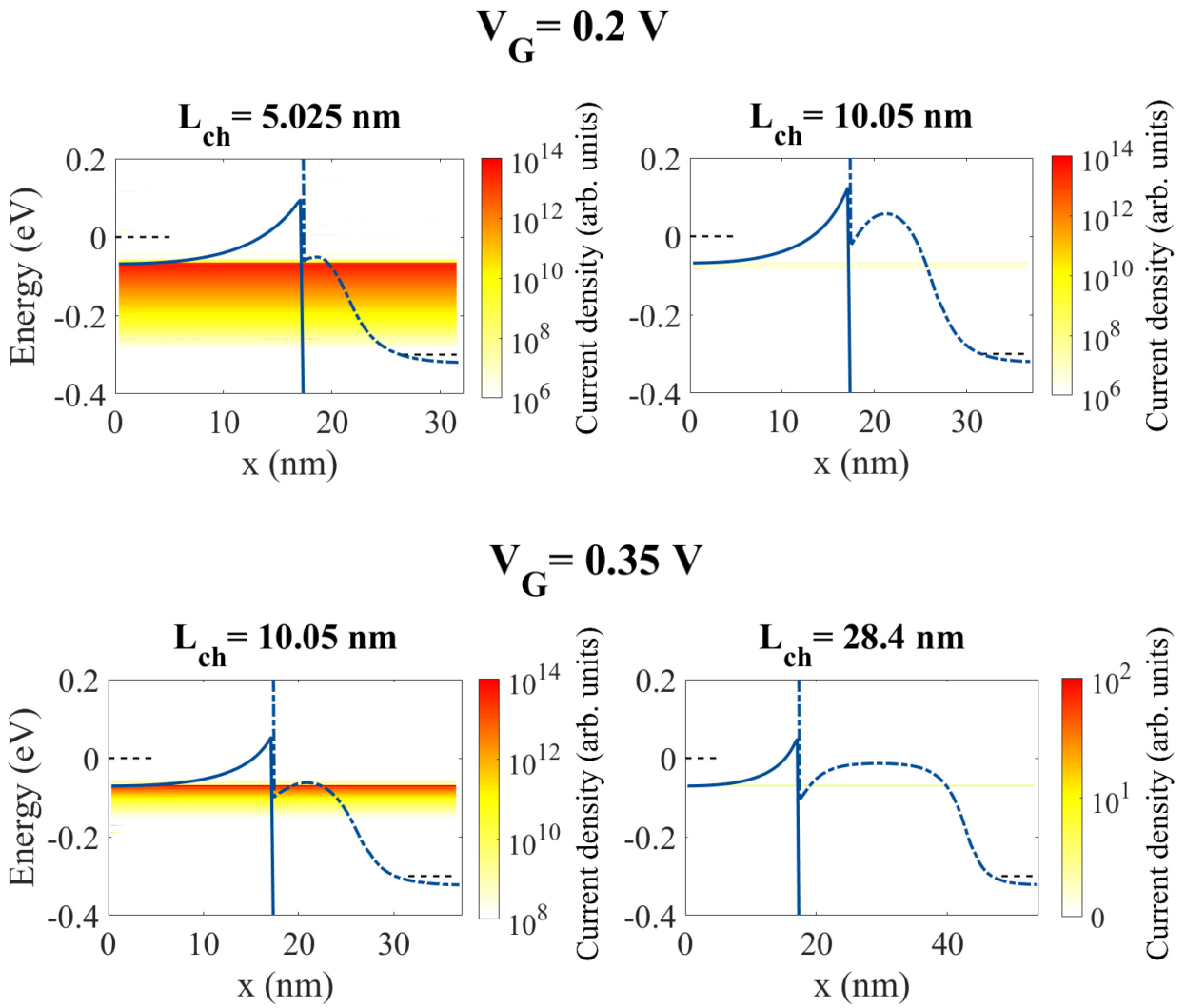


Figure 74. Highest VB (full line) and lowest CB (dotted line) and current density in the $MoTe_2/MoS_2$ device at various L_{ch} and V_G, and for $V_{DS} = V_{DD} = 0.3$ V. The top left plot highlights the direct source-to-drain tunneling preventing an actual OFF state to be reached in the device with $L_{ch} = 5.025$ nm. The bottom left plot highlights the tunneling through the top of the barrier which degrades SS in the case of short channels.

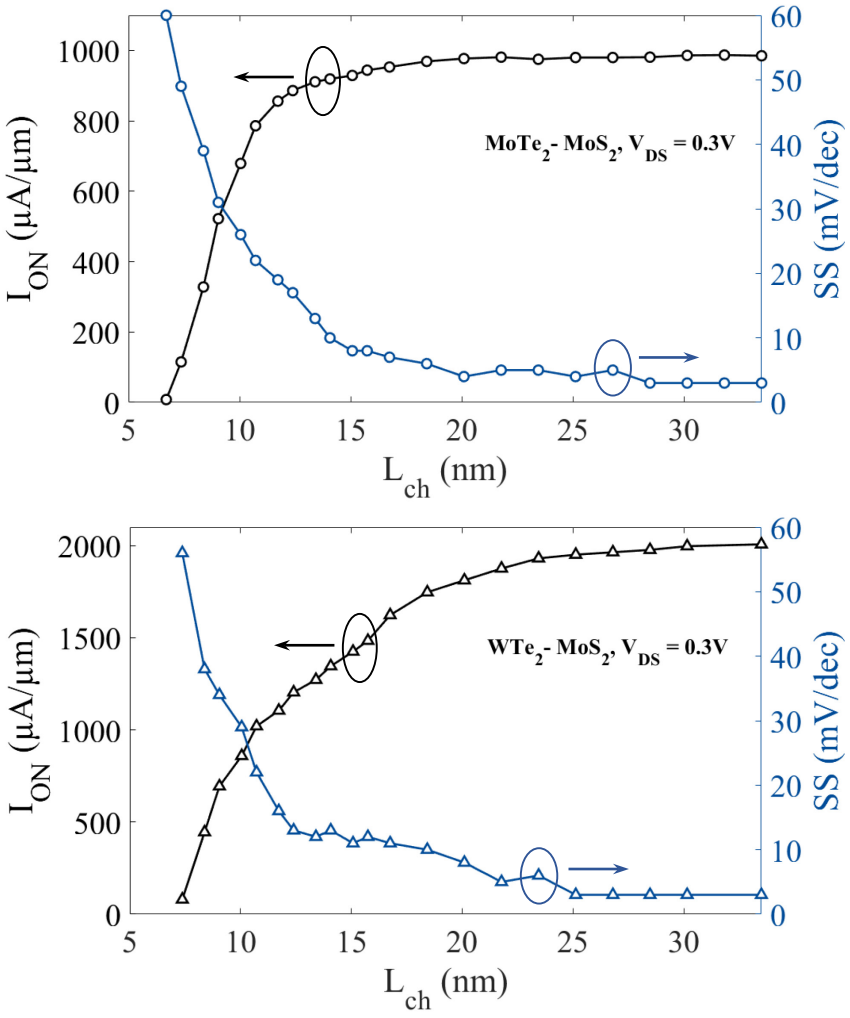


Figure 75. Influence of L_{ch} on ON current and SS in (top) the $MoTe_2/MoS_2$ device and (bottom) the WTe_2/MoS_2 device. In both devices, an increase in channel length allows for better performance (lower SS and higher ON current) up until a certain L_{ch}, beyond which device performance reaches saturation (20 nm for the $MoTe_2/MoS_2$ device and 30 nm for the WTe_2/MoS_2 device).

From this study, it is clear that the performance of these heterojunction TFETs is intrinsically tied to the length of the channel.

From OFF-state leakage current to SS, and even ON current, all aspects of device performance are strongly impacted by a change in channel length. In the case of the $MoTe_2/MoS_2$ device, a channel length $>$ 20 nm is sufficient to reach peak performance, while a channel length $>$ 30 nm is necessary in the case of the WTe_2/MoS_2 device.

Nonetheless, promising performance (sub-5 mV/dec SS and $I_{ON}/I_{OFF} > 10^8$) is observed in both of these devices.

However, electron-phonon interactions (which are not taken into account here) are expected to impact performance more and more as channel length increases: a compromise would therefore need to be found to obtain peak performance in those devices. The influence of the source and drain backgate voltages will now be investigated, as they could allow for further optimization.

5.3.4 Influence of backgate voltages

As was shown in Sections 4.1.2.1 and 4.2.2.1, the voltages applied to the source and drain backgates control the potential and band profile in the device, and can therefore strongly impact device performance.
The effect of the backgate voltages on the performance of the $MoTe_2/MoS_2$ and WTe_2/MoS_2 devices with $V_{DS} = 0.3$ V and $L_{ch} = 13.4$ nm is studied and analyzed in this section.

Figure 76 shows the influence of $V_{BG\text{-}S}$ and $V_{BG\text{-}D}$ on the I_D-V_G characteristics and the ON current in $MoTe_2/MoS_2$ device at $L_{ch} = 13.4$ nm.

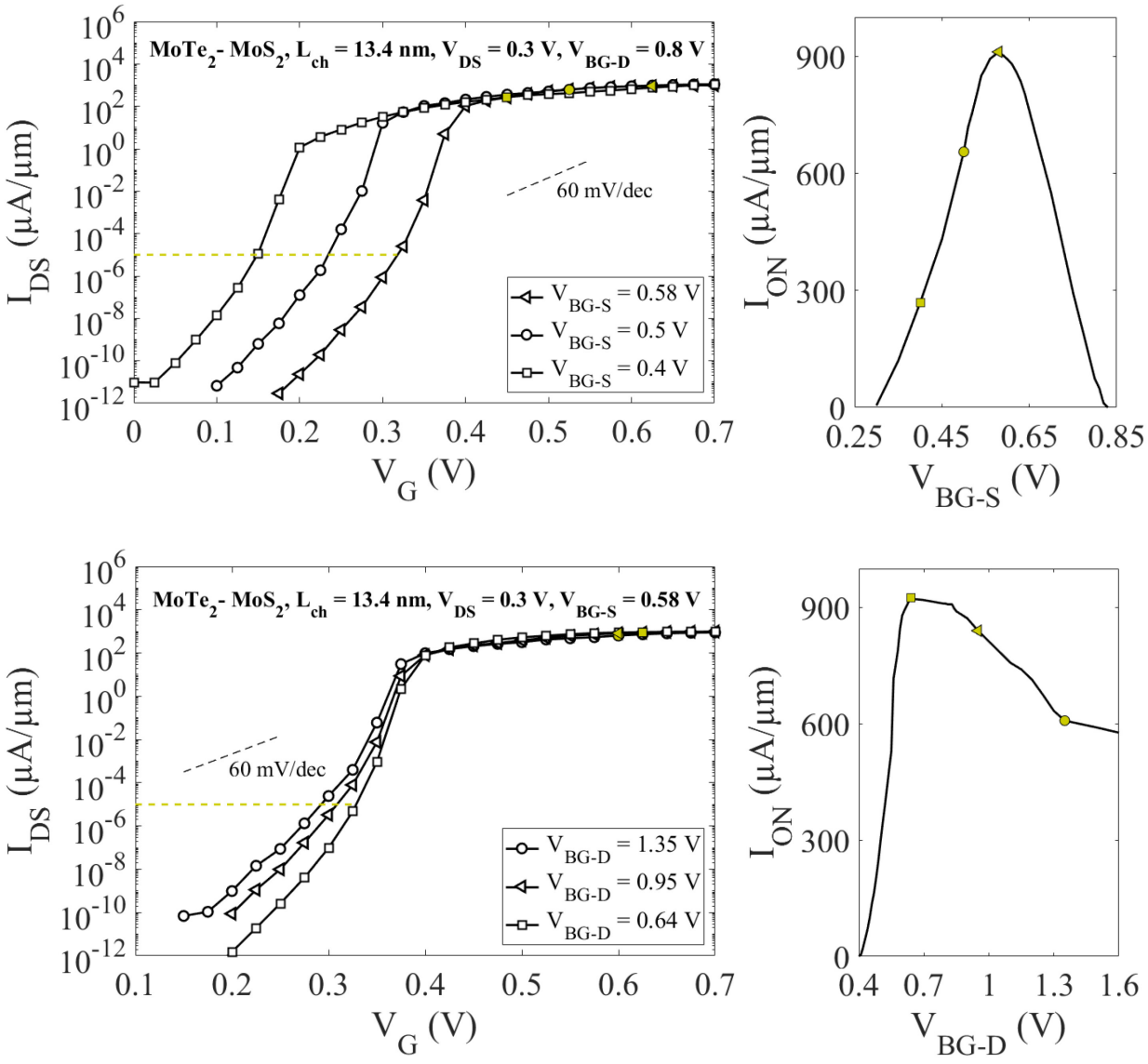


Figure 76. Influence of (top) the source and (bottom) drain backgate voltages on the I_D-V_G characteristics and the ON current in the $MoTe_2/MoS_2$ device at $L_{ch} = 13.4$ nm, at $V_{DS} = V_{DD} = 0.3$ V. The gold dotted line represents the $I_{OFF} = 10^{-5}$ µA/µm and therefore identifies the corresponding V_{OFF} for each characteristics. I_{ON} is then obtained at $V_{ON} = V_{OFF} + V_{DD}$, which is highlighted with a gold marker for each characteristic.

Let us now analyze the influence of the backgate voltages:

- Source backgate voltage: $V_{BG\text{-}S}$ strongly impacts both the current characteristics and the ON current of the device. Namely, the threshold voltage is highly affected, dropping from 0.4 V for $V_{BG\text{-}S} = 0.58$ V to 0.25 V for $V_{BG\text{-}S} = 0.4$ V.
  As is shown in Figure 76, the ON current is highly impacted by the source backgate voltage, and has a somewhat Lorentzian aspect when represented as a function of $V_{BG\text{-}S}$. The explanations for this behavior differ for either side of the peak.
  - For $V_{BG\text{-}S} < 0.58$ V, I_{ON} increases with $V_{BG\text{-}S}$: this behavior is due to the Fermi-Dirac distribution of the carriers in the bands. When $V_{BG\text{-}S}$ is too low, the source VB is forced at energies $> \mu_S$, and therefore fewer carriers are available for transport until very high gate voltages are reached. At higher $V_{BG\text{-}S}$ however, the source VB is forced at energies $< \mu_S$, and the band is therefore filled with carriers ready for transport. The slope of the current in the ON regime is therefore far steeper (see Figure 77 (left)), and more current flows in the device.
  - For $V_{BG\text{-}S} > 0.58$ V, I_{ON} decreases with $V_{BG\text{-}S}$: by increasing $V_{BG\text{-}S}$ further, the source VB is pulled towards even lower energies, gradually narrowing the energy interval between the top of the source VB and the bottom of the channel/drain CB. The band profile shown in Figure 77 for $V_{BG\text{-}S} = 0.75$ V exemplifies this behavior and highlights the narrow energy interval in which current can flow.

  From this analysis, $V_{BG\text{-}S} = 0.58$ V is identified as the source backgate voltage for which the $MoTe_2/MoS_2$ heterojunction TFET at $L_{ch} = 13.4$ nm yields peak performance. A similar study is now performed for $V_{BG\text{-}D}$.

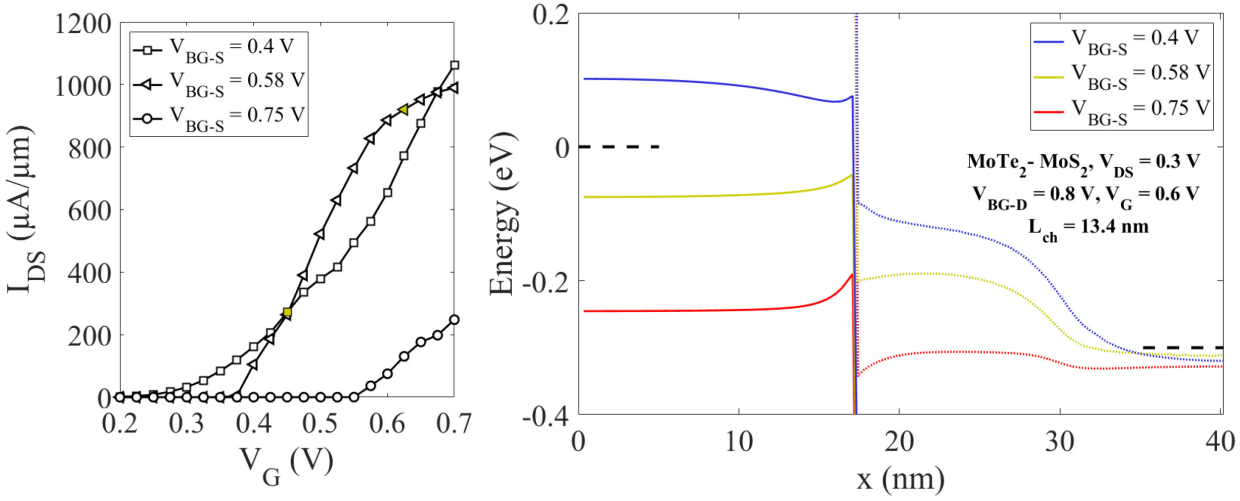


Figure 77. (left) I_D-V_G characteristics and (right) band profile at $V_G = 0.6$ V in the $MoTe_2/MoS_2$ device at various source backgate voltages ranging from 0.4 V to 0.75 V. The influence of $V_{BG\text{-}S}$ on the threshold voltage V_T and the steepness of the current in the ON regime is highlighted by the I_D-V_G characteristics. The band profiles highlight the impact of $V_{BG\text{-}S}$ on both the position of the source VB with respect to μ_S, and the width of the energy interval through which current can flow.

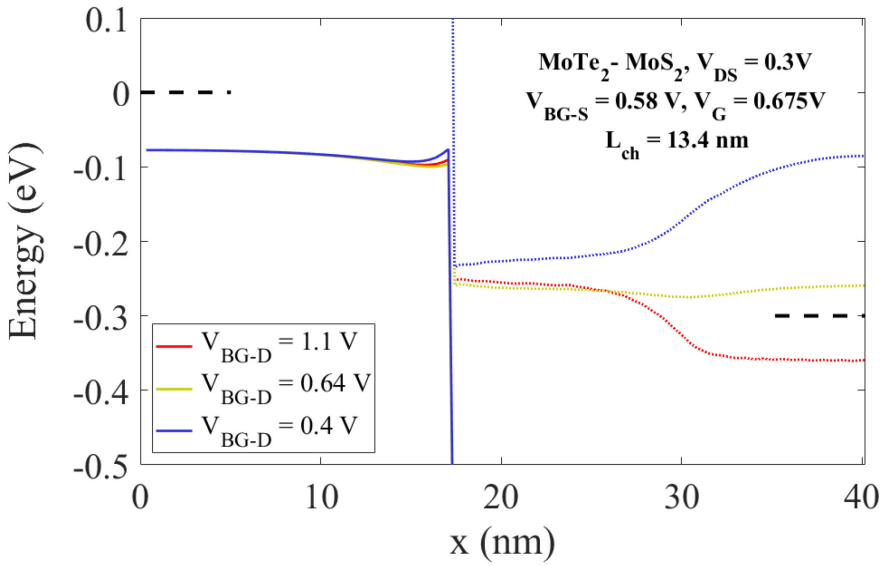


Figure 78. Highest VB (full lines) and lowest CB (dotted lines) in the $MoTe_2/MoS_2$ device in the ON state (V_G = 0.675 V) at V_{DS} = 0.3 V, L_{ch} = 13.4 nm, $V_{BG\text{-}S}$ = 0.58 V and $V_{BG\text{-}D}$ ranging from 0.4 V to 1.1 V. When the drain backgate voltage is too low (0.4 V here), the CB is forced at higher energies in the drain than the VB in the source and ON current drops dramatically (see Figure 76)

- Drain backgate voltage: much like $V_{BG\text{-}S}$, $V_{BG\text{-}D}$ also has an influence on both the current characteristics and the ON current (see Figure 76). As $V_{BG\text{-}D}$ decreases, the steepness of the slope in the sub-threshold regime increases: SS goes from 16 mV/dec for $V_{BG\text{-}D}$ = 1.35 V to 8 mV/dec $V_{BG\text{-}D}$ = 0.64 V for instance.
  The effects of $V_{BG\text{-}D}$ on I_{ON} can once again be explained by two separate mechanisms:
  - For $V_{BG\text{-}D} > 0.64$ V: as $V_{BG\text{-}D}$ decreases, the steepness of the slope in the sub-threshold regime increases while V_T remains unchanged. Therefore, V_{OFF} (V_G for which $I_{DS} = I_{OFF} = 10^{-5}$ µA/µm) increases, and so does V_{ON}. Finally, since I_{ON} is calculated at V_{ON}, I_{ON} increases as $V_{BG\text{-}D}$ decreases.
  - For $V_{BG\text{-}D} < 0.64$ V: as $V_{BG\text{-}D}$ decreases, I_{ON} plummets, before finally reaching 0 around $V_{BG\text{-}D}$ = 0.4 V. The band profiles shown in Figure 78 highlight the explanation for this phenomenon: at $V_{BG\text{-}D}$ = 0.64 V, the CB in the channel and drain is relatively flat (at high V_G, where I_{ON} is obtained). By decreasing $V_{BG\text{-}D}$ further, the CB in the drain is pushed towards higher energies, narrowing the energy window in which current can flow. Finally, at $V_{BG\text{-}D}$ = 0.4 V, the CB in the drain is forced at the same energy than the VB in the source, closing the aforementioned energy window and preventing current flow.

In the end, thanks to this analysis of the influence of source and drain backgate voltages, an optimal set of backgate voltages $V_{BG\text{-}S}$ = 0.58 V and $V_{BG\text{-}D}$ = 0.64 V was identified for this $MoTe_2/MoS_2$ device at V_{DS} = 0.3 V and L_{ch} = 13.4 nm.

A similar study was performed on the WTe_2/MoS_2 device at L_{ch} = 13.4 nm (Figure 79), for which optimal backgate voltages of $V_{BG\text{-}S}$ = 0.85 V and $V_{BG\text{-}D}$ = 0.62 V were identified.

Since some of the mechanisms highlighted here depend on the energy window between the source VB and drain CB, several other optimal sets of $V_{BG\text{-}S}$ and $V_{BG\text{-}D}$ can be found in the same range for both devices. While this study was performed on devices with L_{ch} = 13.4 nm, the backgate voltages identified remain optimal for most channel lengths in the same range. A shift is expected in the case of long channels due to the different profile of the CB in the channel (induced by the decreased proximity of the drain backgate).

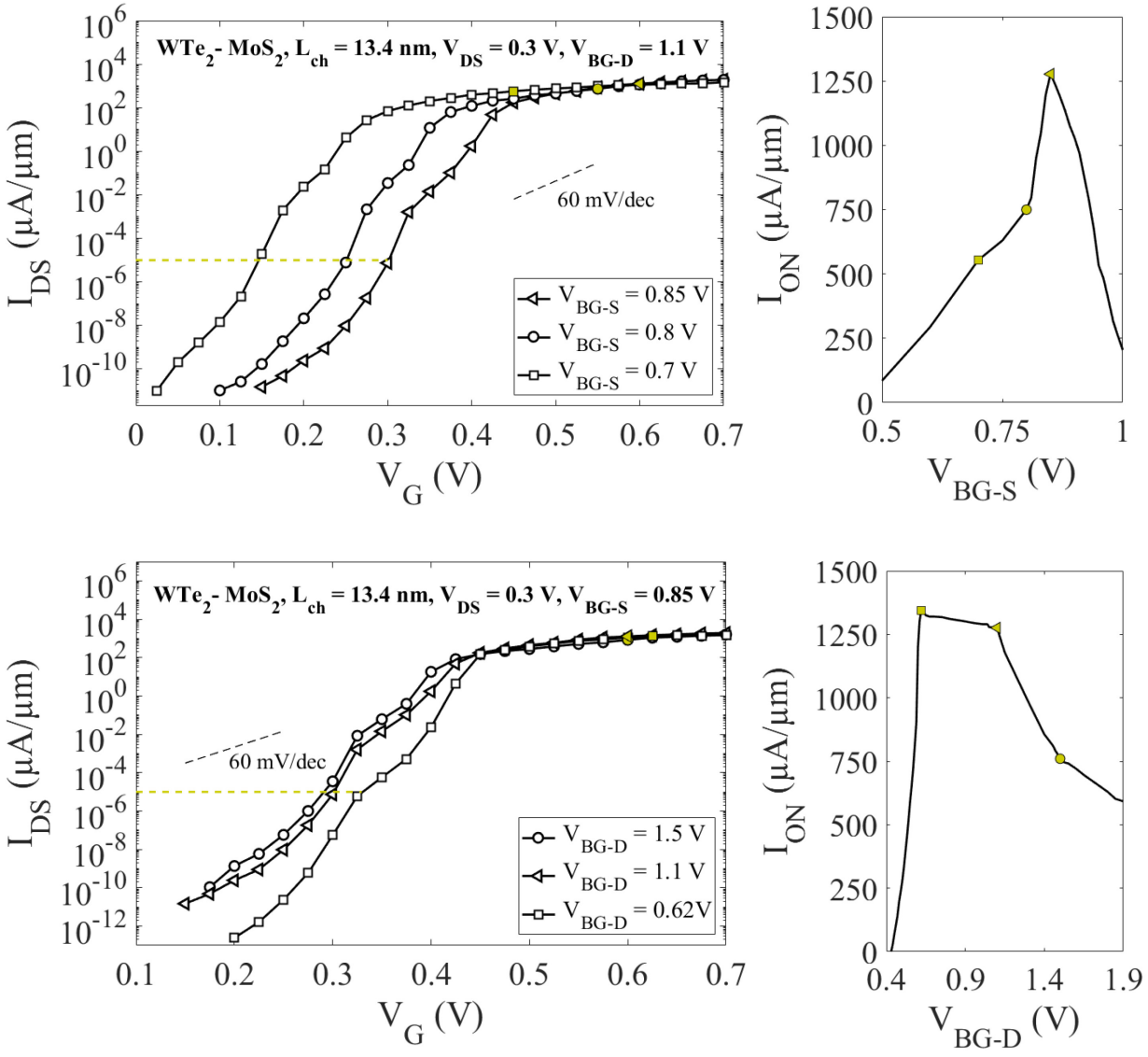


Figure 79. Influence of (top) the source and (bottom) drain backgate voltages on the I_D-V_G characteristics and the ON current in the WTe_2/MoS_2 device at L_{ch} = 13.4 nm and V_{DS} = V_{DD} = 0.3 V. The gold dotted line represents the I_{OFF} = 10^{-5} µA/µm and therefore identifies the corresponding V_{OFF} for each characteristics. I_{ON} is then obtained at V_{ON} = V_{OFF} + V_{DD}, which is highlighted with a gold marker for each characteristic.

5.3.5 Drain voltage characteristics and DITL

In this short section, I will present drain voltage characteristics for the $MoTe_2/MoS_2$ and WTe_2/MoS_2 devices, as well as highlight their robustness against a common short-channel effect that traditionally impedes MOSFETs: drain induced barrier lowering (DIBL).

The I_D-V_{DS} characteristics for the $MoTe_2/MoS_2$ device are shown in Figure 80 at L_{ch} = 13.4 nm, V_G ranging from 0.45 V to 0.6 V, and various $V_{BG\text{-}S/D}$ sets, to highlight the impact the backgate voltages have on these characteristics.

At $V_{BG\text{-}S}$ = 0.4 V and $V_{BG\text{-}D}$ = 2.85 V, the characteristics exhibit the behavior expected of a transistor for all V_G: linear increase in current at low V_{DS}, followed by a saturation for $V_{DS} > 0.15$ V. This indicates that this device can operate at full capacity even at very low supply voltages, making its potential for ultra-low power operation even greater.

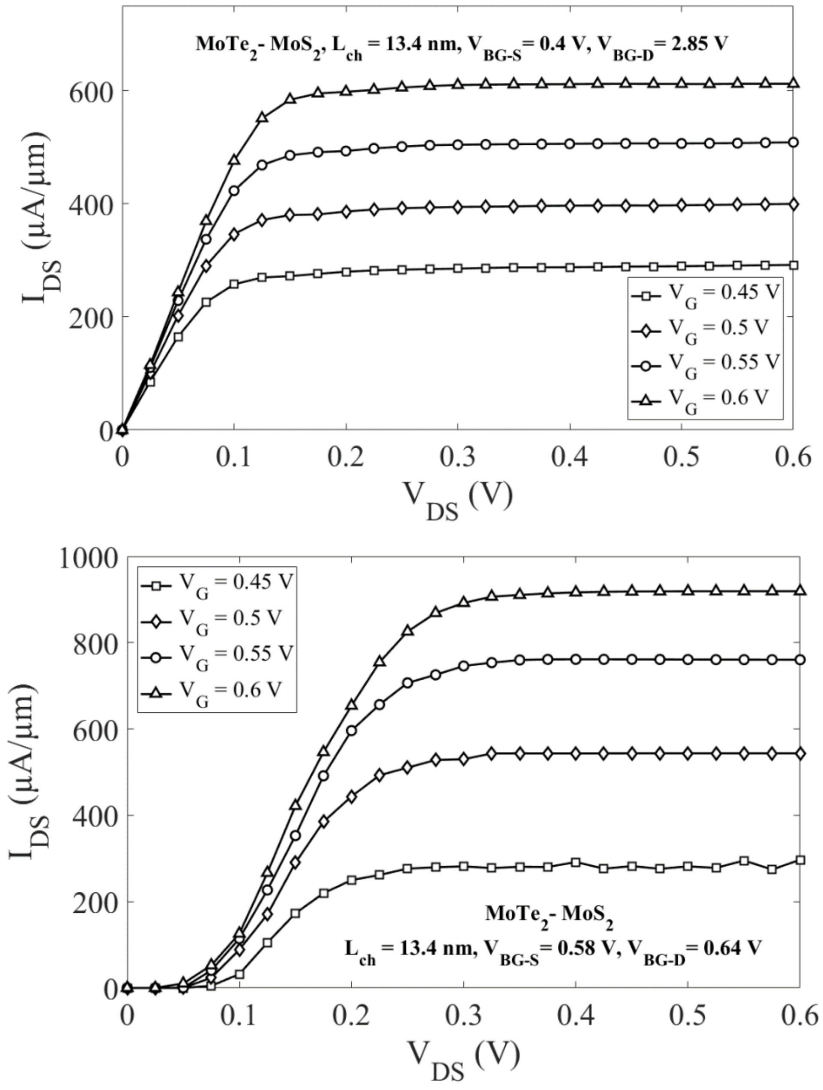


Figure 80. I_D-V_{DS} characteristics of the $MoTe_2/MoS_2$ device for V_G ranging from 0.45 V to 0.6 V, L_{ch} = 13.4 nm, and two sets of backgates voltages, including the optimal set identified in Section 5.3.4.

At $V_{BG\text{-}S} = 0.58$ V and $V_{BG\text{-}D} = 0.64$ V (the optimal set of backgate voltages for which I_{ON} is at its peak at $L_{ch} = 13.4$ nm), the I_D-V_{DS} characteristics exhibit a different behavior. Instead of a linear increase in current at low V_{DS}, the current remains around 0 until $V_{DS} = 0.075$ V, then increases until $V_{DS} = 0.3$ V after which it saturates.
The origin of this behavior can be understood by investigating the energy levels of the source VB and drain CB presented in Figure 81, which shows the band profile for both of the devices shown above at $V_G = 0.6$ V and V_{DS} ranging from 0 V to 0.2 V.

- In the device at $V_{BG\text{-}S} = 0.4$ V and $V_{BG\text{-}D} = 2.85$ V, the drain CB sits at lower energies than the source VB even at $V_{DS} = 0$ V, and the only factor preventing current flow is that $\mu_D = \mu_S$. As soon as V_{DS} increases, $\mu_D < \mu_S$ and current flows freely from the source to the drain.

- In the device at $V_{BG\text{-}S} = 0.58$ V and $V_{BG\text{-}D} = 0.64$ V however, the drain CB sits at higher energies than the source VB for all $V_{DS} < 0.5$ V, and therefore no current flows even though $\mu_D < \mu_S$. When V_{DS} is high enough, the drain CB is forced at lower energies than the source CB and current flows from the source to the drain.

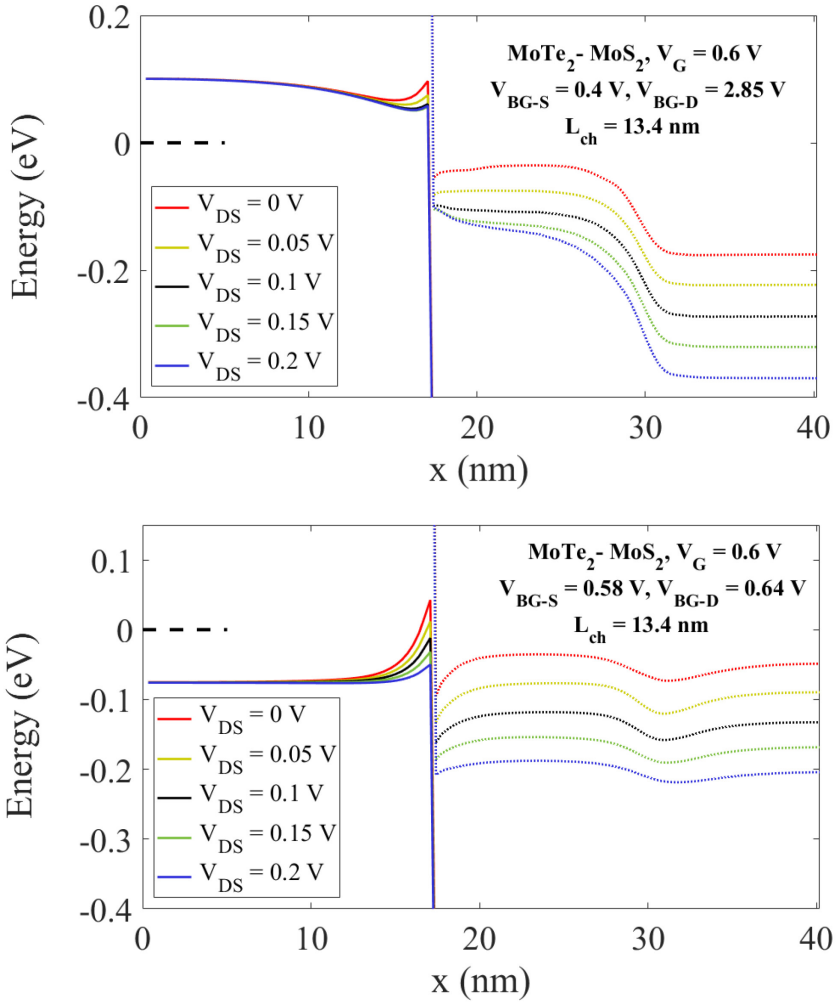


Figure 81. Highest VB (full lines) and lowest CB (dotted lines) in the $MoTe_2/MoS_2$ devices studied in Figure 80 at $V_G = 0.6$ V and V_{DS} ranging from 0 V to 0.2 V.

However, using this optimal set of backgate voltages allows the device to yield much higher currents (50% higher at high V_G) and may therefore be preferable if high I_{ON} is of prime importance for the targeted application.
Moreover, even though the characteristic may not resemble that of a "classic" transistor, the current saturates nicely at $V_{DS} > 0.3$ V nonetheless, which is once again extremely promising for ultra-low power operation.

Similar observations can be made for the WTe_2/MoS_2 device, of which the I_D-V_{DS} characteristics are shown in Figure 82.

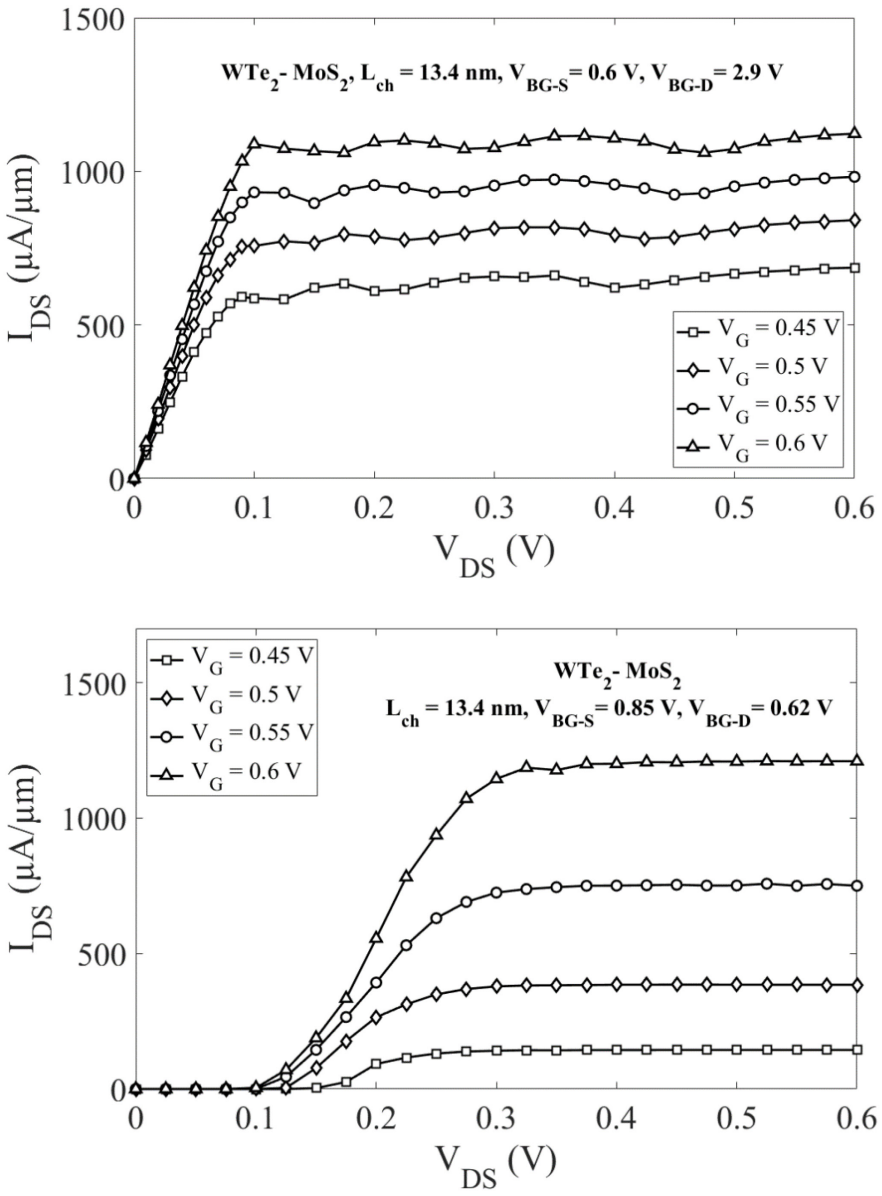


Figure 82. I_D-V_{DS} characteristics of the WTe_2/MoS_2 device for V_G ranging from 0.45 V to 0.6 V, L_{ch} = 13.4 nm, and two sets of backgate voltages, including the optimal set identified in Section 5.3.4.

Drain-induced barrier lowering (DIBL) is an SCE commonly found in MOSFETs, and, as its name suggests, describes the influence of the applied supply voltage on the height of the potential barrier. As an SCE, it is increasingly reinforced as channel length is shortened, and is measured in mV/V (shift in V_T per 1 V increase in V_{DS}).

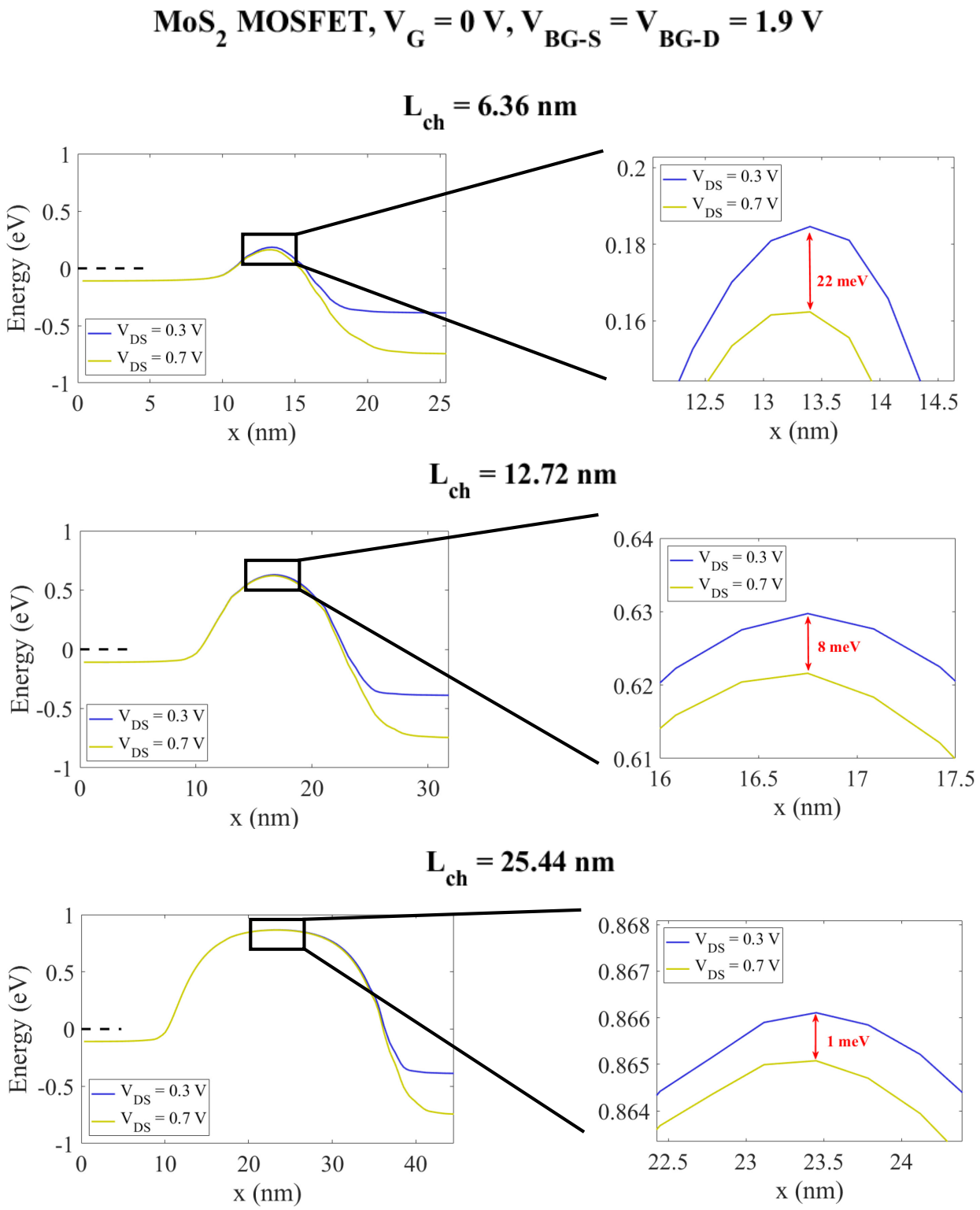


Figure 83. Highest VB in the MoS_2 MOSFET at $V_G = 0$ V and $V_{DS} = 0.3$ V and 0.7 V for several channel lengths, highlighting the DIBL in each case (right).

Figure 83 highlights the effects of the DIBL occurring in the MoS_2 MOSFET studied in Section 4.1, and its dependence on channel length. DIBL is often used as a measurement of the susceptibility of a MOSFET to short-channel effects in general.

TFETs, on the other hand, generally do not suffer from this effect since they rely on BTBT rather than thermionic injection over a potential barrier. They can however suffer drain induced threshold lowering (DITL).
Figure 84 highlights the robustness of the $MoTe_2/MoS_2$ and WTe_2/MoS_2 devices against this effect: for V_{DS} varying from 0.1 to 0.8 V, V_T remains unchanged. Currents reported at $V_{DS} = 0.1$ V are lower for all gate voltages due to the position of the energy levels of the bands in the contacts at these backgate voltages (see Figure 81 which highlighted the same issue).

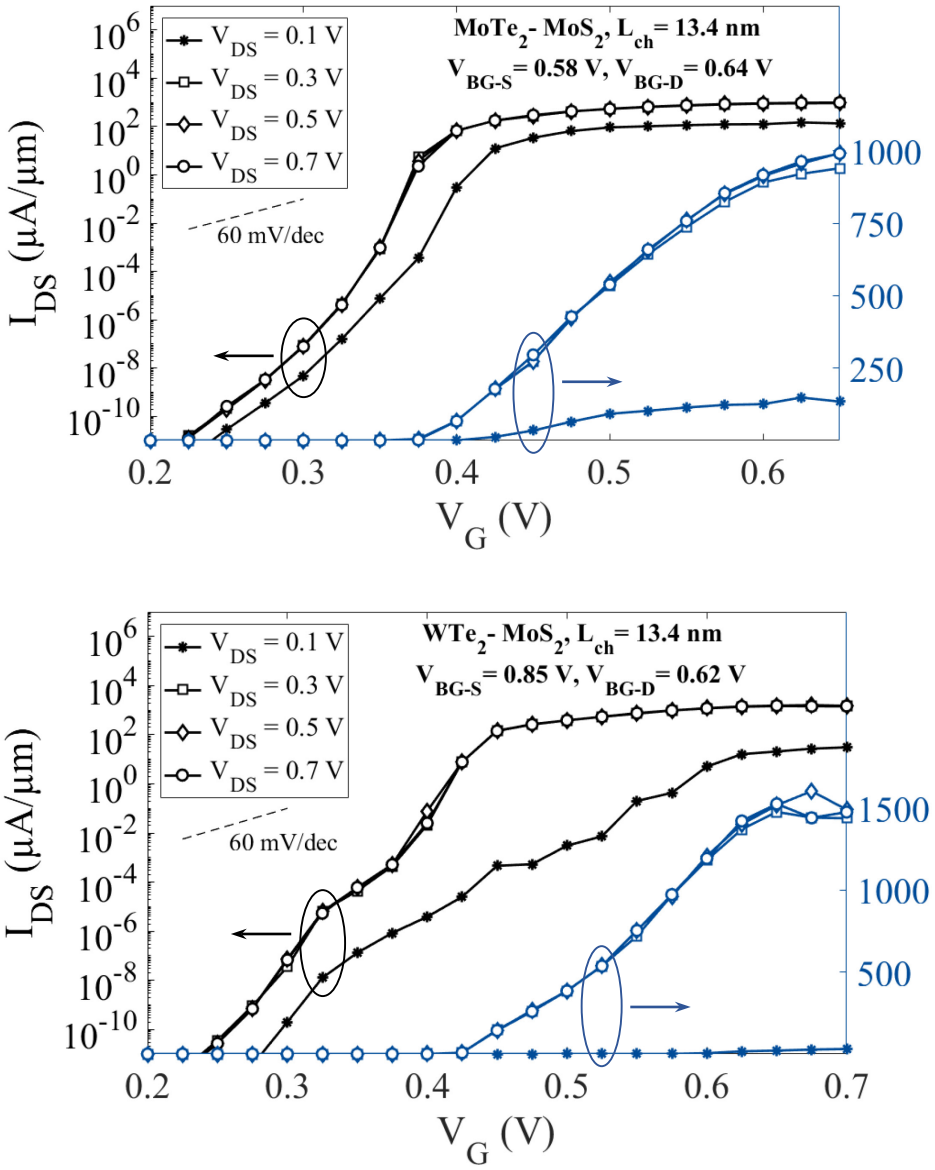


Figure 84. I_D-V_G characteristics of the $MoTe_2/MoS_2$ and the WTe_2/MoS_2 devices for $L_{ch} = 13.4$ nm, V_{DS} ranging from 0.1 V to 0.7 V and the optimal backgate voltages for each device as identified in Section 5.3.4.

Indeed, by using the optimal sets of $V_{BG\text{-}S}$ and $V_{BG\text{-}D}$ identified in Section 5.3.4, the CB in the drain is forced at energy levels higher than the VB in the source at very low V_{DS} (see Figure 81). Therefore, much like for the I_D-V_{DS} characteristics shown in Figure 80 and Figure 82, a certain threshold has to be reached by the supply voltage so that the drain CB is forced below the source VB and current can flow. However, at V_{DS} close to this threshold, the energy window in which current can flow remains narrow compared to higher V_{DS}, which explains the lower currents reported at low V_{DS}.
Figure 85 highlights the width of the energy window in which current can flow for V_{DS} = 0.1 V and 0.7 V in the $MoTe_2/MoS_2$ device.

In the end, the study of these devices under varied supply voltages highlighted their robustness when it comes to DITL as well as their capacity to saturate at low V_{DS}, which reinforces their strong potential for ultra-low power operation.

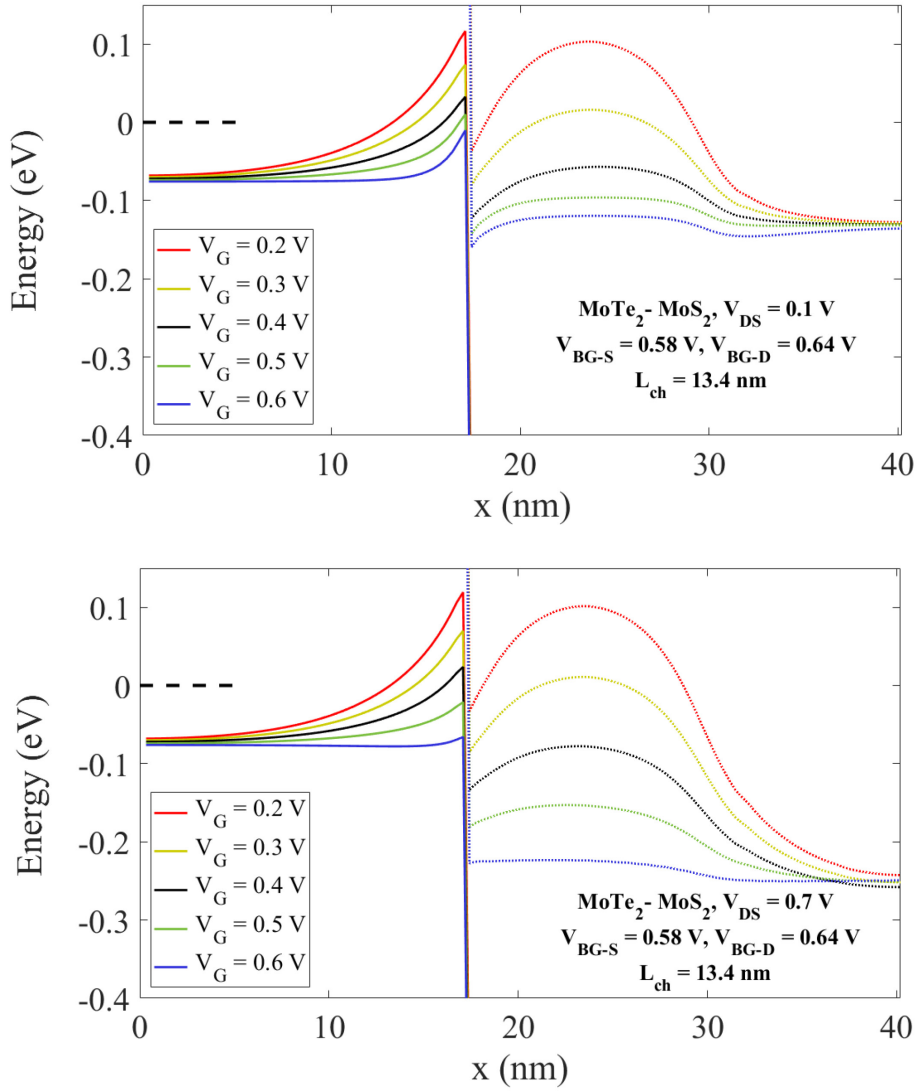


Figure 85. Highest VB (full lines) and lowest CB (dotted lines) in the $MoTe_2/MoS_2$ device at L_{ch} = 13.4 nm, $V_{BG\text{-}S}$ = 0.58 V, $V_{BG\text{-}D}$ = 0.64 V and (top) V_{DS} = 0.1 V (top) V_{DS} = 0.7 V. At V_{DS} = 0.1 V, the drain CB is at comparable energies than the source VB (see Figure 81), leading to lower currents.

5.4 Conclusion on standard in-plane heterojunction TFETs

The $MoTe_2/MoS_2$ and WTe_2/MoS_2 devices studied in this chapter show great promise for ultra-low power operation thanks to several key points:

- **Extremely low SS:** depending on the length of the channel, the devices yield ballistic SS ranging from 30 mV/dec in the case of short channels, down to below 5 mV/dec for $L_{ch} > 20$ nm.

- **High ON/OFF ratio:** depending on the backgate voltages applied to the contacts, ballistic ON/OFF ratios up to 10^8 for the $MoTe_2/MoS_2$ device and 2×10^8 for WTe_2/MoS_2 device have been reported.

- **Good saturation even at low V_{DS}:** both devices saturate nicely at low drain voltages (as low as $V_{DS} = 0.2$ V) when the optimal backgate voltages are applied. They therefore yield peak performance while remaining energy-efficient, which only strengthens their appeal as ultra-low power electronic switches.

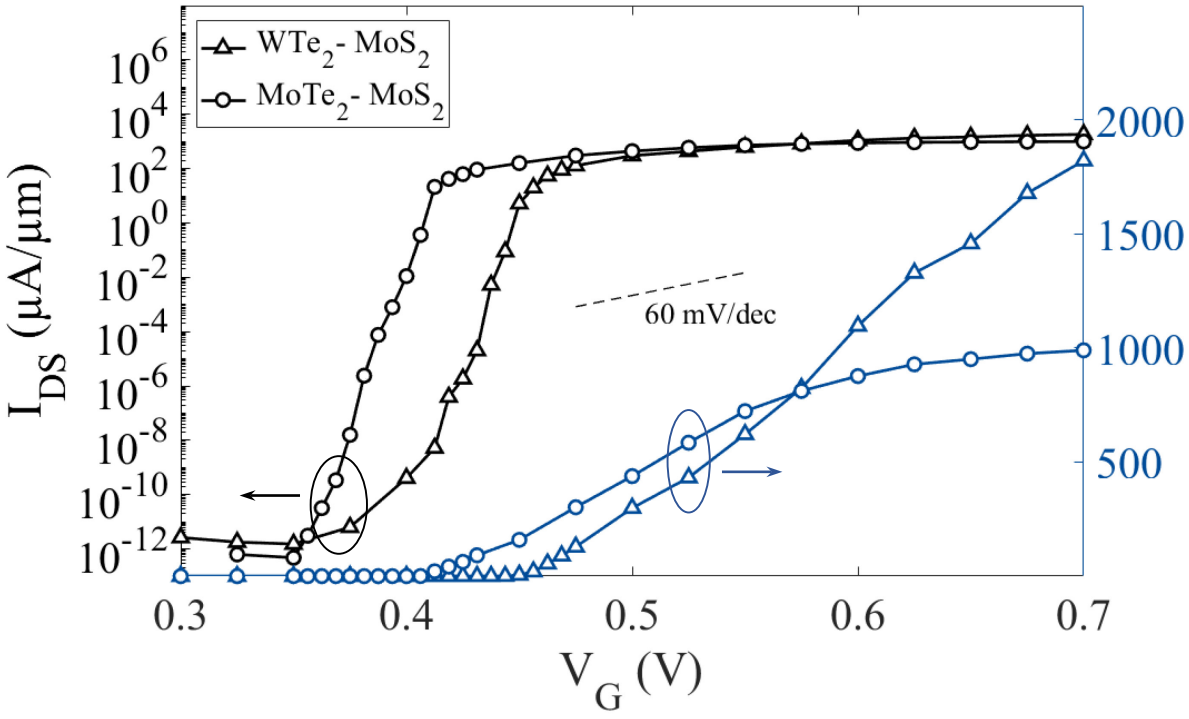


Figure 86. I_D-V_G characteristics for both devices at $V_{DS} = 0.3$ V, $L_{ch} = 26.8$ nm, $V_{BG\text{-}S/D} = 0.58$ V and 0.64 V for $MoTe_2/MoS_2$ and $V_{BG\text{-}S/D} = 0.85$ V and 0.62 V for WTe_2/MoS_2.

Chapter 6

Drain-backgate-enhanced heterojunction TFETs

6.1 Origin and definition

When studying the influence of the source and drain backgate voltages on the performance of the $MoTe_2/MoS_2$ and WTe_2/MoS_2 devices, an idea for a new device derived from the standard in-plane heterojunction based TFET came to us.
By analyzing the impact of the drain backgate voltage on the current in the sub-threshold regime, we observed an interesting phenomenon that could be exploited to our advantage. As $V_{BG\text{-}D}$ increases, the current in the sub-threshold regime also increases (see Figure 87). This is expected and is due to the impact of $V_{BG\text{-}D}$ on the drain CB: the drain CB is pulled down towards lower energies, allowing for more electrons to flow from the source to the drain (see the bands profiles and LDOS shown in Figure 88).
It thus seems relevant to check if this property can be used to improve the device performance: we anticipate that the steepness of the slope in the sub-threshold regime may be dramatically increased by carefully selecting the workfunctions of the various gates and applying the same voltage to the drain backgate and channel gate, so that

$$V_{BG-D} = V_G \qquad W_{BG-D} = W_{CG} - \Delta W \tag{53}$$

where ΔW is the offset between the work-functions of the metals used as drain-backgate ($W_{BG\text{-}D}$) and channel gate/source backgate (W_{CG}).
By carefully selecting ΔW, the drain CB can be forced at energies higher than the source CB at low V_G, preventing all current flow in the OFF state. The workfunctions of the metals used as gates in both DBE devices are therefore:

- 5.19 eV for the channel-gate and the source backgate.
- $(5.19 - \Delta W)$ eV for the drain backgate.

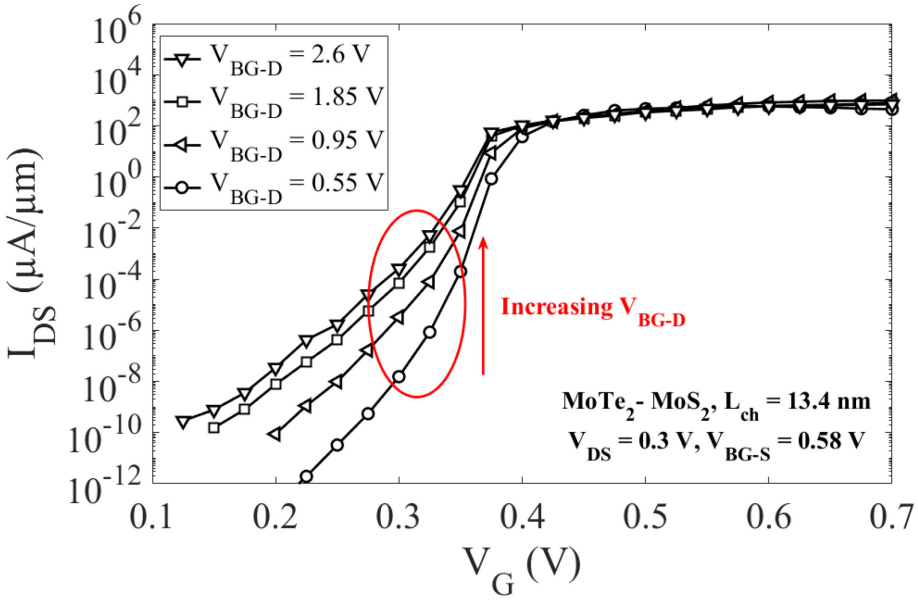


Figure 87. I_D-V_G characteristics for the $MoTe_2/MoS_2$ device at $V_{DS} = 0.3$ V, $L_{ch} = 13.4$ nm, $V_{BG\text{-}S} = 0.58$ V and $V_{BG\text{-}D}$ ranging from 0.55 V to 2.6 V. This figure highlights the increase in OFF current with $V_{BG\text{-}D}$ used in these DBE devices.

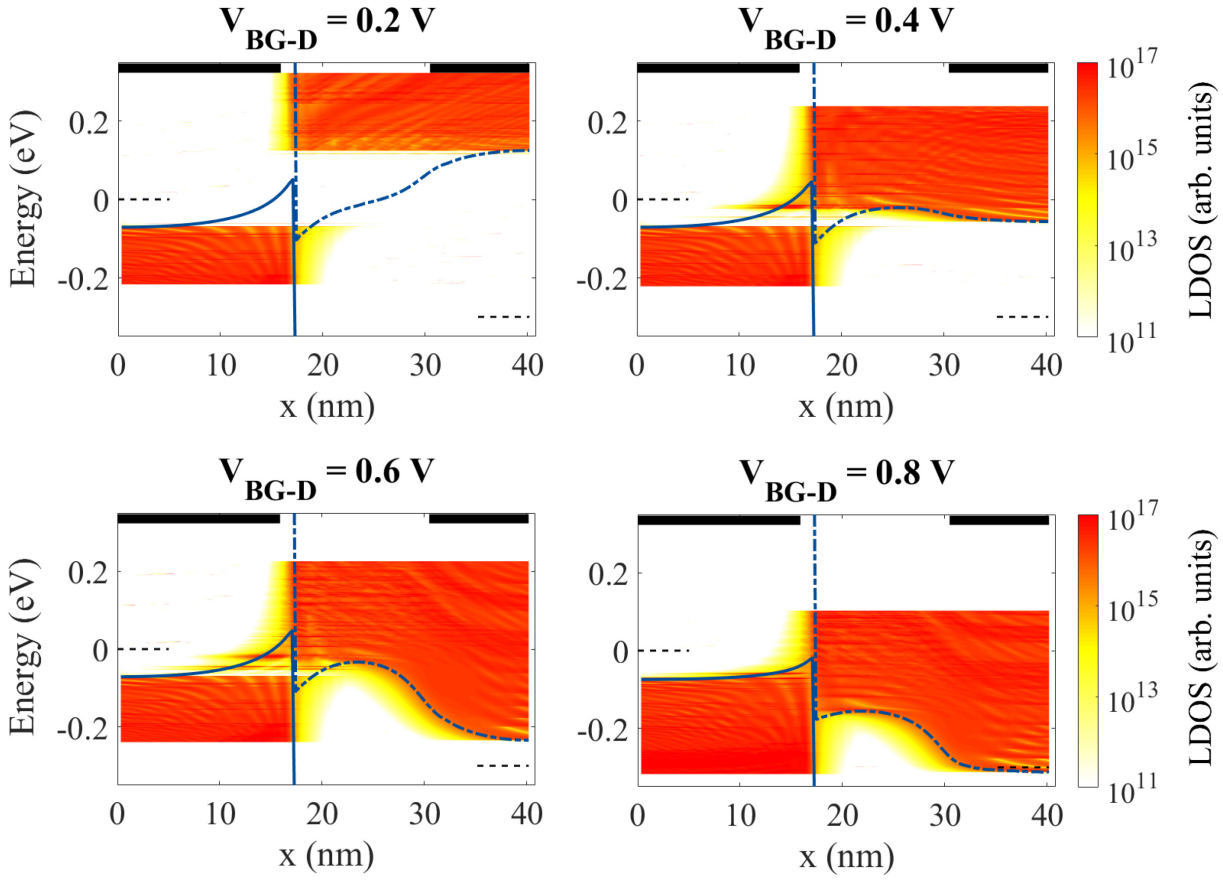


Figure 88. LDOS, highest VB (full lines) and lowest CB (dotted line) at $V_G = 0.35$ V in the $MoTe_2/MoS_2$ device detailed in Figure 89 for $V_{BG\text{-}D}$ increasing from 0.2 V to 0.8 V. This figure highlights the absence of states in the channel/drain to tunnel to at low $V_{BG\text{-}D}$. As $V_{BG\text{-}D}$ increases, the drain CB is pulled down towards lower energies, and current can start flowing from the source VB to the channel/drain.

6.2 Device architecture

The architecture of the drain-backgate-enhanced (DBE) devices investigated is the same as that of the standard TFETs presented in Section 5.1. The only difference is that, as detailed in the previous section, the voltage applied to the drain backgate will be V_G, the same voltage as the channel-gate.
The source backgate voltage is not modified and behaves as it did in the standard in-plane heterojunction TFETs.

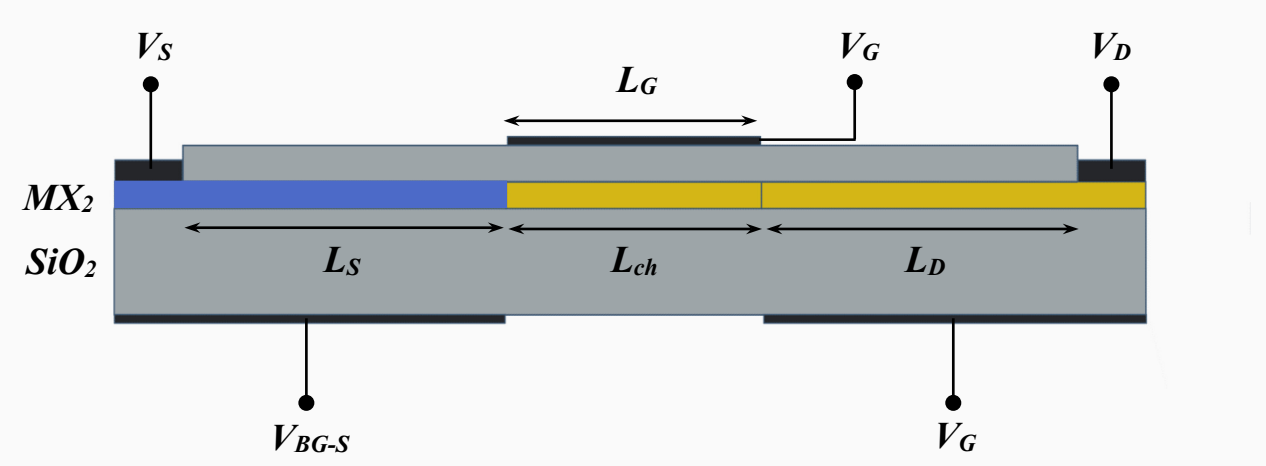


Figure 89. Device architecture for the considered DBE in-plane heterojunction TFETs.
One TMD acts as the source, and another as the channel/drain. SiO_2 is used as a buried oxide, and a high-κ dielectric as the top gate oxide. The same voltage is applied to the drain backgate and the top-gate so that $V_{BG\text{-}D} = V_G$, while $W_{BG\text{-}D} = W_{CG} - \Delta W$ is the workfunction of the metal used as drain backgate.

6.3 Electronic transport simulations

6.3.1 Influence of backgate metal workfunction

The first parameter to study in these new devices is of course the backgate work-function difference with respect to the channel gate, ΔW, and its influence on device performance. In some of the I_D-V_G characteristics shown in this section, the behavior of these drain backgate enhanced devices will be shown for several ΔW (as full lines), but also compared to that of a standard in-plane heterojunction TFET with a static $V_{BG\text{-}D}$ (which will be shown as dotted lines) in which case $W_{BG\text{-}D} = W_{CG}$.
I_D-V_G characteristics for both the DBE $MoTe_2/MoS_2$ and the WTe_2/MoS_2 devices at $V_{DS} = 0.3$ V, $L_{ch} = 10.05$ nm and $V_{BG\text{-}S} = 0.58$ V and 0.85 V (resp.) and various workfunction offsets are shown in Figure 90.

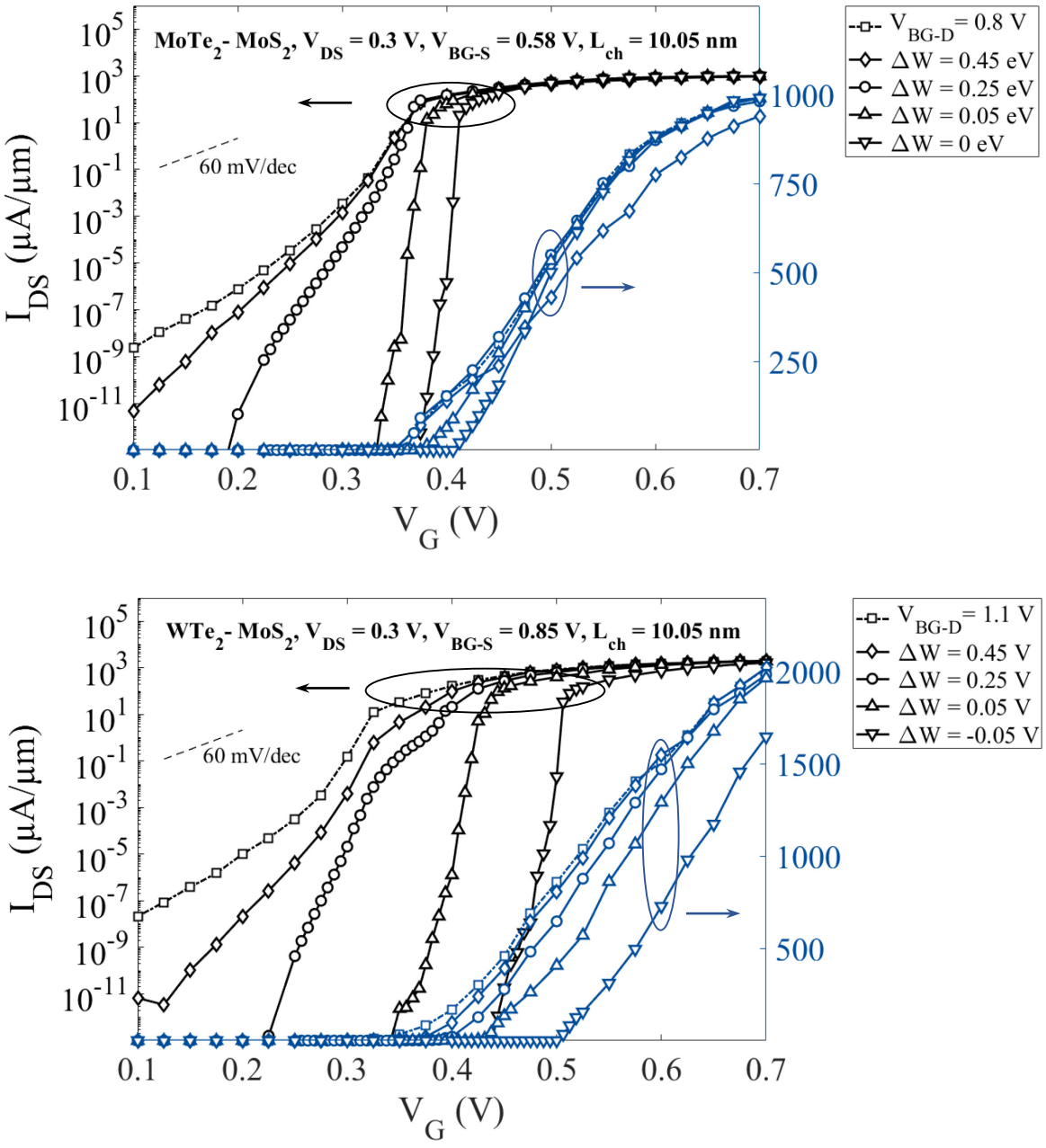


Figure 90. I_D-V_G characteristics for the $MoTe_2/MoS_2$ and the WTe_2/MoS_2 devices at $V_{DS} = 0.3$ V, $L_{ch} = 10.05$ nm and $V_{BG\text{-}S} = 0.58$ V and 0.85 V (resp.). ΔW ranges from -0.05 eV to 0.45 eV for the DBE heterojunction TFETs.

A similar behavior can be observed across both devices: as ΔW decreases, the steepness of the slope in the sub-threshold regime strongly increases due to the absence of source-to-drain tunneling (because the CB in the drain is at higher energies than the source VB). SS is therefore tremendously reduced as ΔW decreases: it is for instance reduced from 30 mV/dec in the standard $MoTe_2/MoS_2$ device to less than 5 mV/dec in the DBE device for $\Delta W = 0.05$ V. At this workfunction offset however, minimal SS has been reached and will not change if ΔW is decreased further.

ON current is also strongly affected by ΔW: since V_{OFF} is strongly increased (from 0.25 V in the standard $MoTe_2/MoS_2$ device to 0.35 V in the DBE device for $\Delta W = 0.05$ eV), so is V_{ON} and therefore I_{ON}.

Due to the joint influence of ΔW and V_G on the CB in the drain (see Figure 88) and the resulting ability of these devices to completely inhibit source-to-drain tunneling at low V_G, the limits of channel scaling are completely removed.
As highlighted in Figure 91, DBE devices with channels as short as 1.675 nm (which, in the case of standard TFETs cannot be switched OFF due to source-to-drain tunneling) are shown to reach SS as low as the 10 nm devices shown previously, and marginally higher ON currents at high V_G thanks to source-to-drain tunneling.

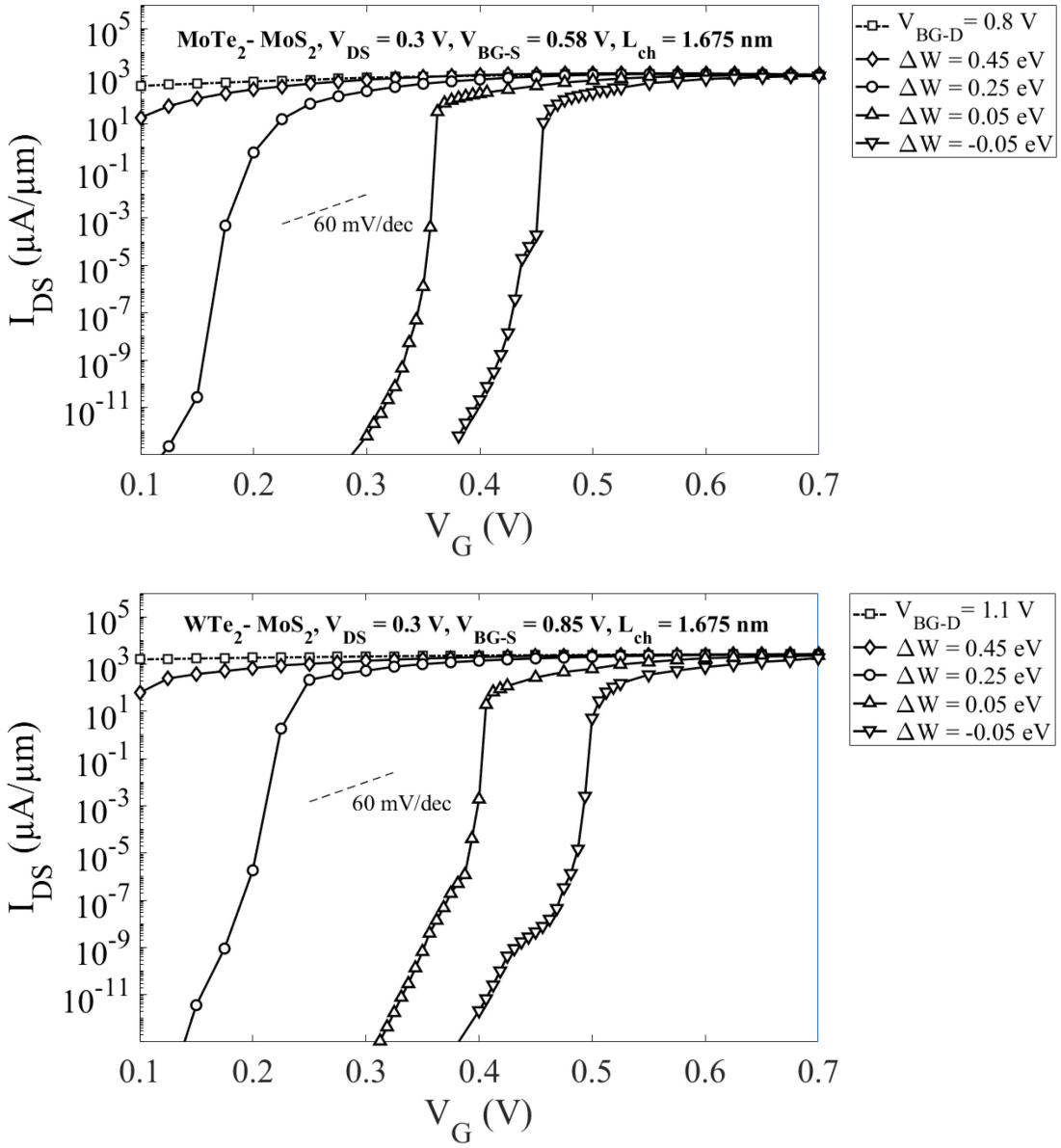


Figure 91. I_D-V_G characteristics for the DBE $MoTe_2/MoS_2$ and the WTe_2/MoS_2 devices at $V_{DS} = 0.3$ V, $L_{ch} = 1.675$ nm and $V_{BG\text{-}S} = 0.58$ V and 0.85 V (resp.). ΔW ranges from −0.05 eV to 0.45 eV for the DBE-TFETs. The current is only shown in log scale to improve readability.

The potential of this DBE devices cannot be understated: the traditional limits of channel scaling are removed, and, in short-channel devices, source-to-drain tunneling actually becomes an advantage at high V_G, increasing I_{ON} further. This will be highlighted in Section 6.4, which will investigate the effect of channel length on these DBE devices.

It is now clear that these new devices present tremendous advantages compared to standard TFETs; and their optimal workfunction offset will now be identified.

Figure 92 shows the I_D-V_G characteristics for the DBE $MoTe_2/MoS_2$ device at $V_{DS} = 0.3$ V, $L_{ch} = 10.05$ nm, $V_{BG\text{-}S} = 0.58$ V, and ΔW ranging from -0.20 eV to 0.05 eV. As mentioned before, it is clear that the maximum steepness is reached at $\Delta W = 0.05$ eV, and therefore SS is not modified by decreasing the work-function offset further. Both the threshold voltage and the steepness of the slope in the ON regime are however impacted as ΔW decreases further, and the ON current is therefore expected to be modified as well.
Although it is not shown here, similar observations can be made for the DBE WTe_2/MoS_2 device.

The direct influence of the work-function offset on SS and I_{ON} in both the DBE $MoTe_2/MoS_2$ and WTe_2/MoS_2 devices at $L_{ch} = 10.05$ nm, $V_{DS} = 0.3$ V and $V_{BG\text{-}S} = 0.58$ V and 0.85 V (resp.) is shown in Figure 93.

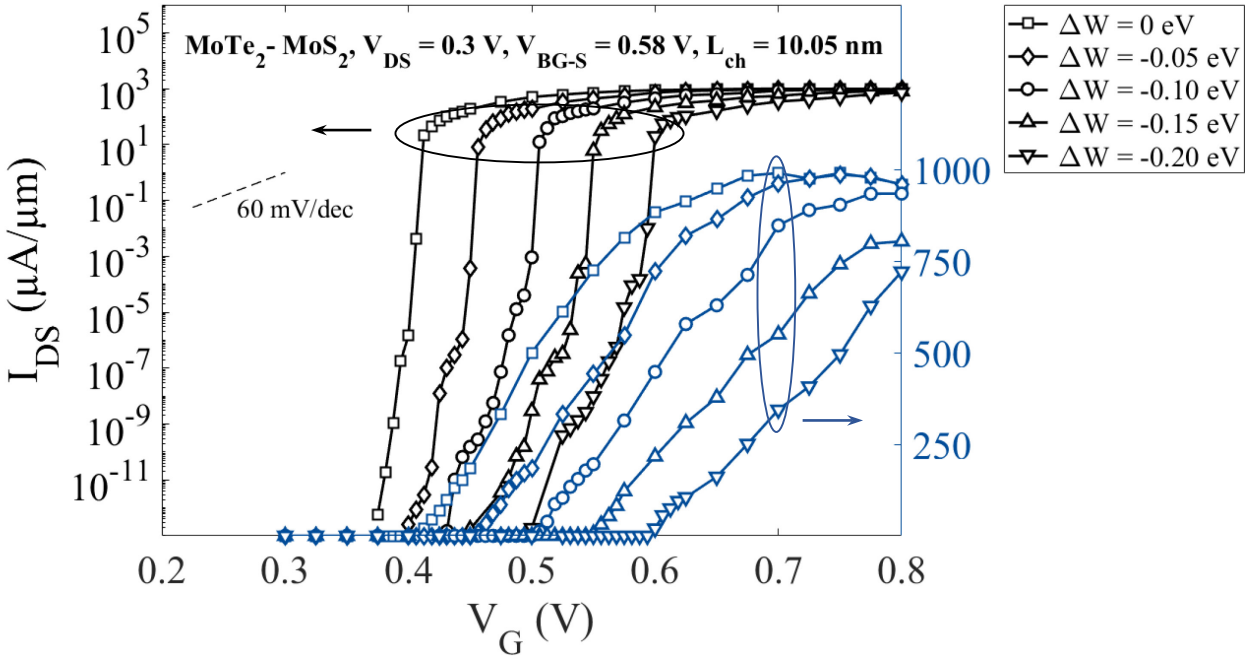


Figure 92. I_D-V_G characteristics for the backgate-enhanced $MoTe_2/MoS_2$ device at $V_{DS} = 0.3$ V, $L_{ch} = 10.05$ nm, $V_{BG\text{-}S} = 0.58$ V, and ΔW ranging from -0.20 eV to -0.05 eV.

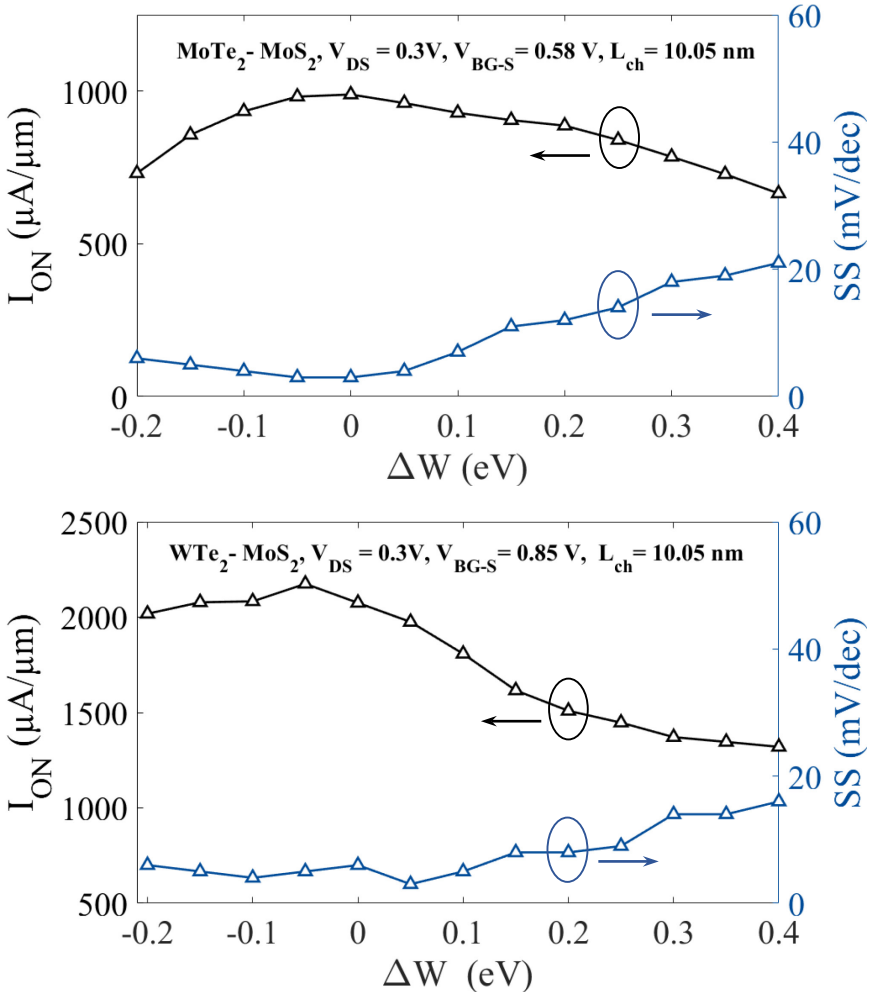


Figure 93. Influence of the workfunction offset on device performance in the DBE (top) $MoTe_2/MoS_2$ and (bottom) WTe_2/MoS_2 devices. In both cases, an optimal range from -0.05 eV to 0.05 eV allowing for peak performance (minimum *SS* and maximum I_{ON}) can be identified.

The work-function offset has a similar impact in both devices:

- I_{ON}: As ΔW decreases, the ON current increases until it reaches a maximum around $\Delta W = 0$ eV (980 µA/µm for $MoTe_2/MoS_2$ and 2175 µA/µm for WTe_2/MoS_2) and slightly decreases for $\Delta W <$ -0.05 eV
- *SS*: As ΔW decreases, *SS* decreases and stabilizes around 5 mV/dec for $\Delta W < 0.1$ eV

In both DBE devices, the optimal work-function offset is identified to be $\Delta W = -0.05$ eV. This is expected since, at this ΔW, $V_{OFF} \sim 0.415$ V (see Figure 92), therefore $V_{ON} = V_{OFF} + V_{DS} \sim 0.715$ V.
At this V_G, the equivalent drain backgate voltage in the standard devices (where $W_{BG\text{-}D} = W_{CG}$) is $V_{BG\text{-}D} = \frac{\Delta W}{e} + 0.715 \sim 0.665$ V, which is close to the optimal drain backgate voltages identified in Section 5.3.4 for both devices (0.64 V for $MoTe_2/MoS_2$ and 0.62 V for WTe_2/MoS_2).

By using the same metal in all gates ($\Delta W = 0$ eV), great performance can therefore be reached. Note that these observations pertain to the devices with short channels (10.05 nm shown here). In the case of longer channel where standard TFETs already yield peak I_{ON} and minimum SS (see Figure 75), ΔW has almost no influence on device performance.

6.3.2 Influence of channel length

In Section 5.3.3, it was shown that the performance of the standard heterojunction TFETs was strongly influenced by channel length, and that $L_{ch} > 20$ nm (30 nm) was necessary for the $MoTe_2/MoS_2$ (the WTe_2/MoS_2 device) to yield its peak performance both in terms of SS as well is I_{ON}.

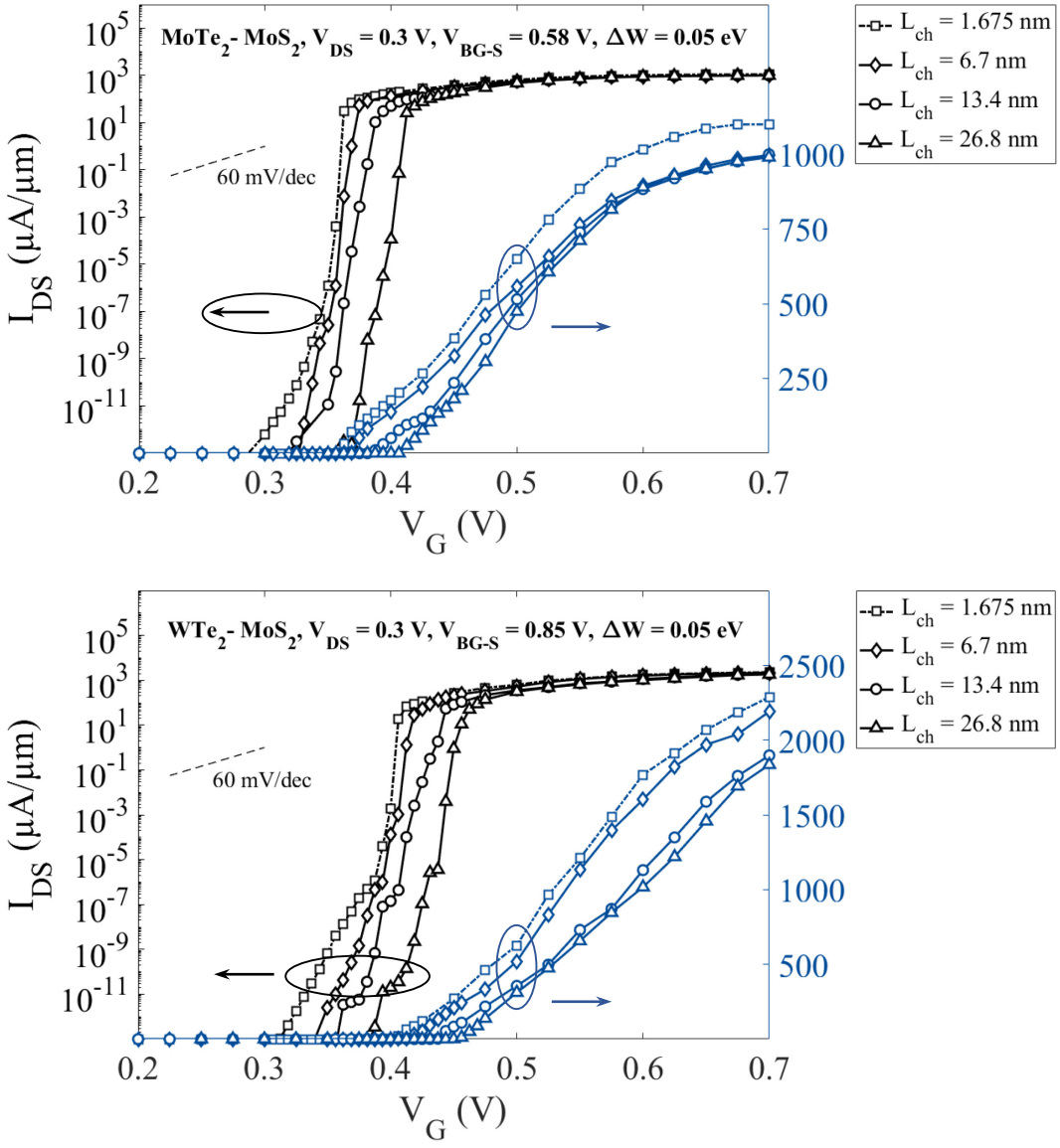


Figure 94. I_D-V_G characteristics for the DBE $MoTe_2/MoS_2$ and the WTe_2/MoS_2 devices at $V_{DS} = 0.3$ V, $V_{BG\text{-}S} = 0.58$ V and 0.85 V (resp.), $\Delta W = 0.05$ eV and for channel lengths between 1.675 nm and 27 nm.

Figure 94 shows the I_D-V_G characteristics for the DBE $MoTe_2/MoS_2$ and the WTe_2/MoS_2 devices at $V_{DS} = 0.3$ V, $V_{BG\text{-}S} = 0.58$ V and 0.85 V (resp.), $\Delta W = 0.05$ eV and channel lengths ranging from 1.675 nm to 26.8 nm.
In both devices, it is obvious that channel length does not impact *SS* (as a reminder, we estimate *SS* between $I_{DS} = 10^{-5}$ µA/µm and 10^{-2} µA/µm): no matter the channel length, the transition from a fully OFF to a fully ON state requires only a small increase in V_G of at most 0.03 V.

The direct influence of channel length on *SS* and I_{ON} in the DBE devices is shown in Figure 95. Its impact on the performance of the standard TFETs as studied in Section 5.3.3 is also shown for comparison purposes.

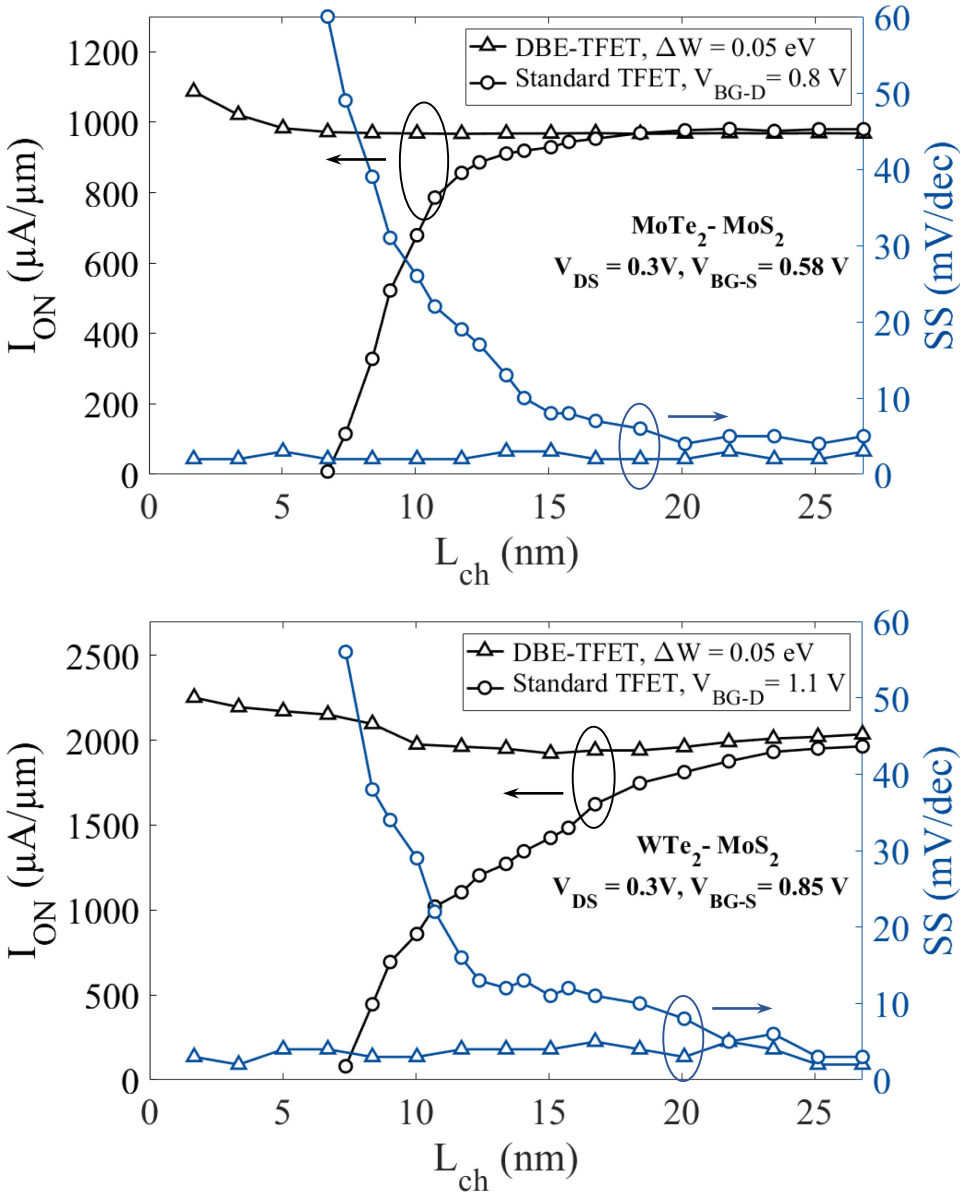


Figure 95. Influence of channel length on both *SS* and I_{ON} in the DBE $MoTe_2/MoS_2$ and WTe_2/MoS_2 devices at $V_{DS} = 0.3$ V and $V_{BG\text{-}S} = 0.58$ V and 0.85 V (resp.), as well as the standard TFETs as studied in Section 5.3.3 and shown in Figure 75.

As expected, *SS* is not impacted by L_{ch} in either device and remains < 5 mV/dec for all channel lengths. The ON current at this ΔW is slightly impacted in both devices: it peaks for the shortest channel, then decreases until $L_{ch} > 7$ nm at which point it stabilizes. This evolution can be explained by two factors highlighted in Figure 96 and Figure 97:

- in short-channel devices, the proximity of the drain backgate pulls the CB down in the channel, widening the energy window in which current can flow.
- in very short-channel devices, carriers can tunnel directly from the source VB to the drain CB, effectively widening the aforementioned energy window even further.

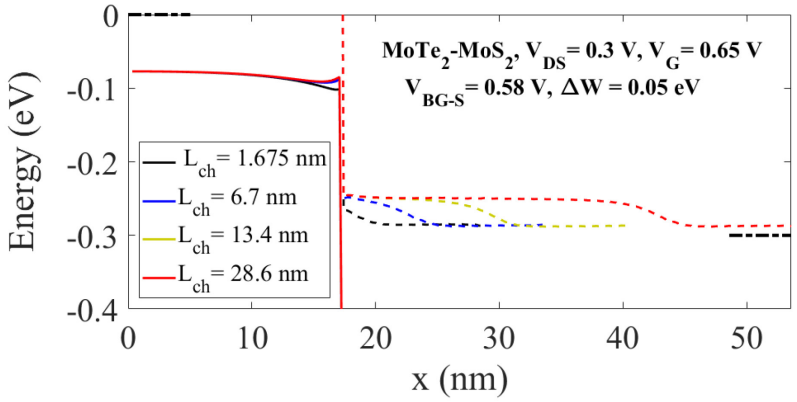


Figure 96. Highest VB (full lines) and lowest CB (dotted lines) in the DBE $MoTe_2/MoS_2$ device at $V_{DS} = 0.3$ V, $V_G = 0.65$ V, $V_{BG\text{-}S} = 0.58$ V, $\Delta W = 0.05$ eV and L_{ch} ranging from 1.675 nm to 26.8 nm, highlighting the impact of L_{ch} on the CB in the channel.

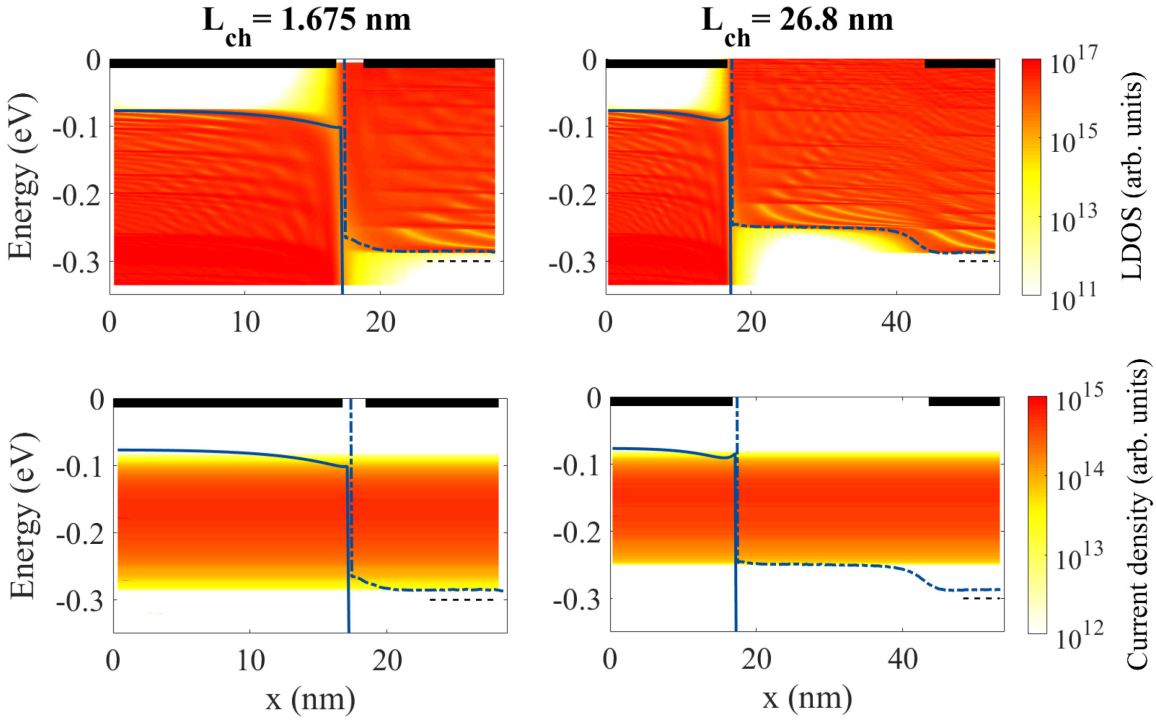


Figure 97. (top) LDOS and (bottom) current density as well as highest VB (full lines) and lowest CB (dotted lines) in the DBE $MoTe_2/MoS_2$ device at $V_{DS} = 0.3$ V, $V_G = 0.65$ V, $V_{BG\text{-}S} = 0.58$ V, $\Delta W = 0.05$ eV and (left) L_{ch} =1.675 nm and (right) 26.8 nm, highlighting the impact of L_{ch} on source-to-drain tunneling.

However, the main takeaway from Figure 95 is the striking comparison with the standard TFETs, because virtually any dependence on channel length is removed in the DBE devices:

- The performance of standard heterojunction TFETs increases with L_{ch}, and channel lengths beyond at least 8 nm are necessary for these devices to even be functional. Channel lengths beyond at least 20 nm are necessary for them to yield the promising performances detailed in Chapter 4.

- The performance of the DBE TFETs, no matter the channel length, is always superior to or equal to the peak performance of the standard TFETs. There are no limits to channel scaling, and extremely short channels actually yield marginally higher ON currents (maximum I_{ON} requires $L_{ch} < 5$ nm) at the considered ΔW (at a lower ΔW, L_{ch} would not influence I_{ON}). Moreover, the negative impact of electron-phonon interactions increases with device length, so keeping the channel short would alleviate these effects.

While they share the same materials, architecture and general principle of operation, the DBE devices allow us to access the peak performance of the already very promising heterojunction TFETs at any channel length.

6.3.3 Influence of source backgate voltage

Much like in the standards TFETs studied in Chapter 4, the source backgate voltage is another important tuning parameter, as it controls the potential profile as well as the energy level of the VB in the source contact.
However, since the analysis is very close to that of the standard TFETs performed in Section 5.3.4, this section will be brief and will solely focus on identifying the optimal $V_{BG\text{-}S}$ for each device at $\Delta W = 0.05$ eV.
The effect of the backgate voltages on the performance of the DBE $MoTe_2/MoS_2$ and WTe_2/MoS_2 devices at $V_{DS} = 0.3$ V, $L_{ch} = 10.05$ nm and $\Delta W = 0.05$ eV and analyzed in this section.
The corresponding I_D-V_G characteristics for both devices are shown in Figure 98 at several source backgate voltages:

- DBE $MoTe_2/MoS_2$ device: $V_{BG\text{-}S} = 0.4$ V, 0.52 V and 0.6 V
- DBE WTe_2/MoS_2 device: $V_{BG\text{-}S} = 0.7$ V, 0.8 V and 0.85 V

Overall, the impact of the source backgate voltage in these DBE devices is very close to its influence on the performance of the standard TFETS described in Section 5.3.4.

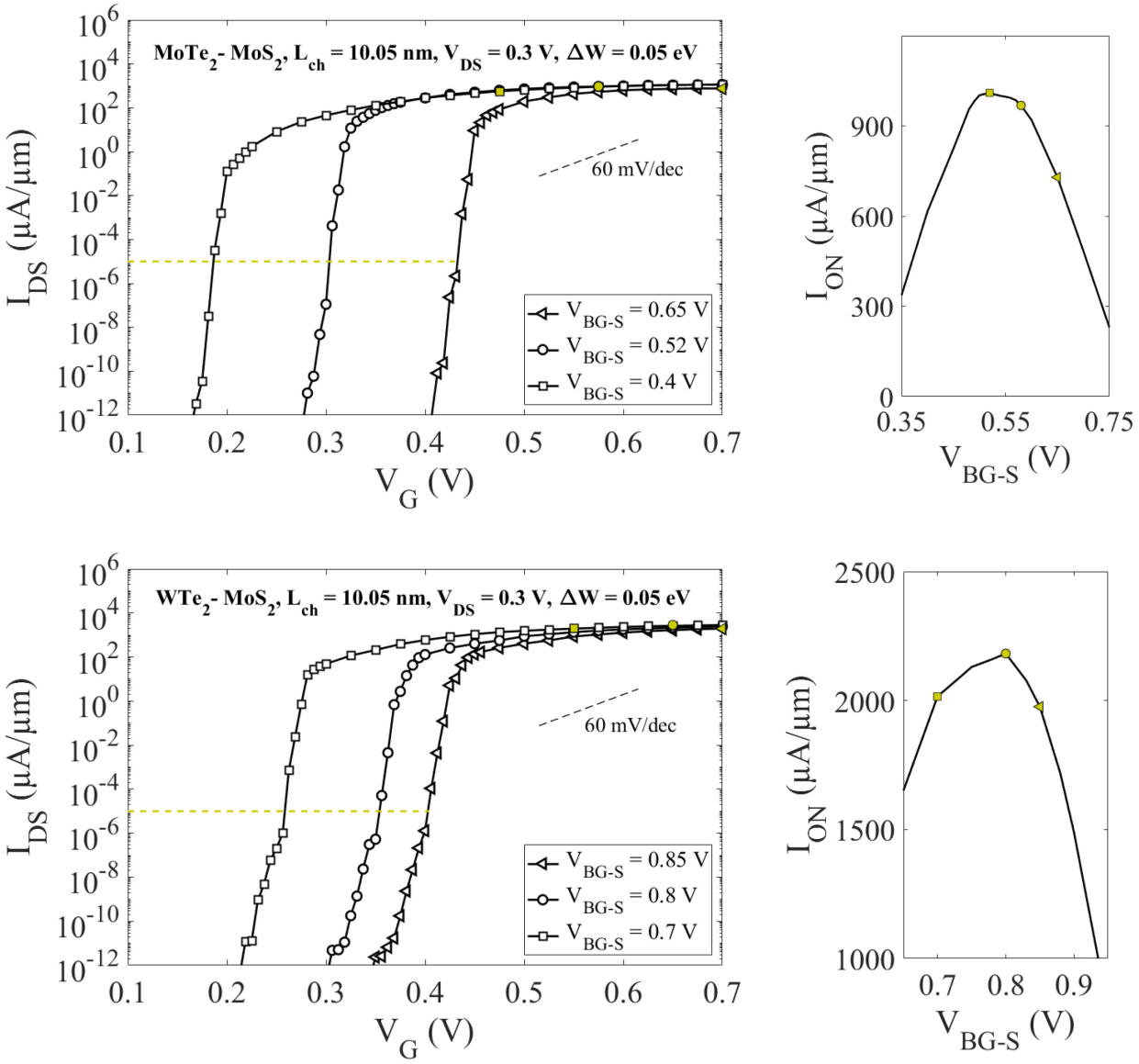


Figure 98. (left) I_D-V_G characteristics at various $V_{BG\text{-}S}$ and (right) influence of the source backgate voltage on I_{ON} in the DBE (top) $MoTe_2/MoS_2$ and (bottom) WTe_2/MoS_2 devices at $V_{DS} = V_{DD} = 0.3$ V, $L_{ch} = 10.05$ nm and $\Delta W = 0.05$ eV.

As was the case in the standard heterojunction TFETs, the source backgate voltage does not impact SS in either device, as evidenced by the slope in the sub-threshold regime of the I_D-V_G characteristics.

The ON current of both devices however, is strongly impacted by $V_{BG\text{-}S}$ as highlighted by in Figure 98 (right). In both cases, a somewhat parabolic evolution of I_{ON} can be observed, around a peak value of 1011 µA/µm at $V_{BG\text{-}S} = 0.52$ V for the $MoTe_2/MoS_2$ device, and 2182 µA/µm at $V_{BG\text{-}S} = 0.8$ V for the WTe_2/MoS_2 device (at $L_{ch} = 10.05$ nm).

These optimal backgate voltages remain close to those identified for the standard TFETs in Section 5.3.4, which is expected ($V_{BG\text{-}S} = 0.58$ V for the $MoTe_2/MoS_2$ device and $V_{BG\text{-}S} = 0.85$ V for the WTe_2/MoS_2 device).

6.3.4 Drain voltage characteristics and DITL

Another strong feature of the heterojunction TFETs presented in Chapter 4 is the saturation reached at supply voltages as low as 0.2 V. Since these DBE-TFETs rely on the same materials and general principle of operation, they are expected to yield similar performance.

The I_D-V_{DS} characteristics of the DBE $MoTe_2/MoS_2$ device at L_{ch} = 13.4 nm, V_G ranging from 0.4 V to 0.6 V and $V_{BG\text{-}S}$ = 0.4 V and 0.52 V are shown in Figure 99.

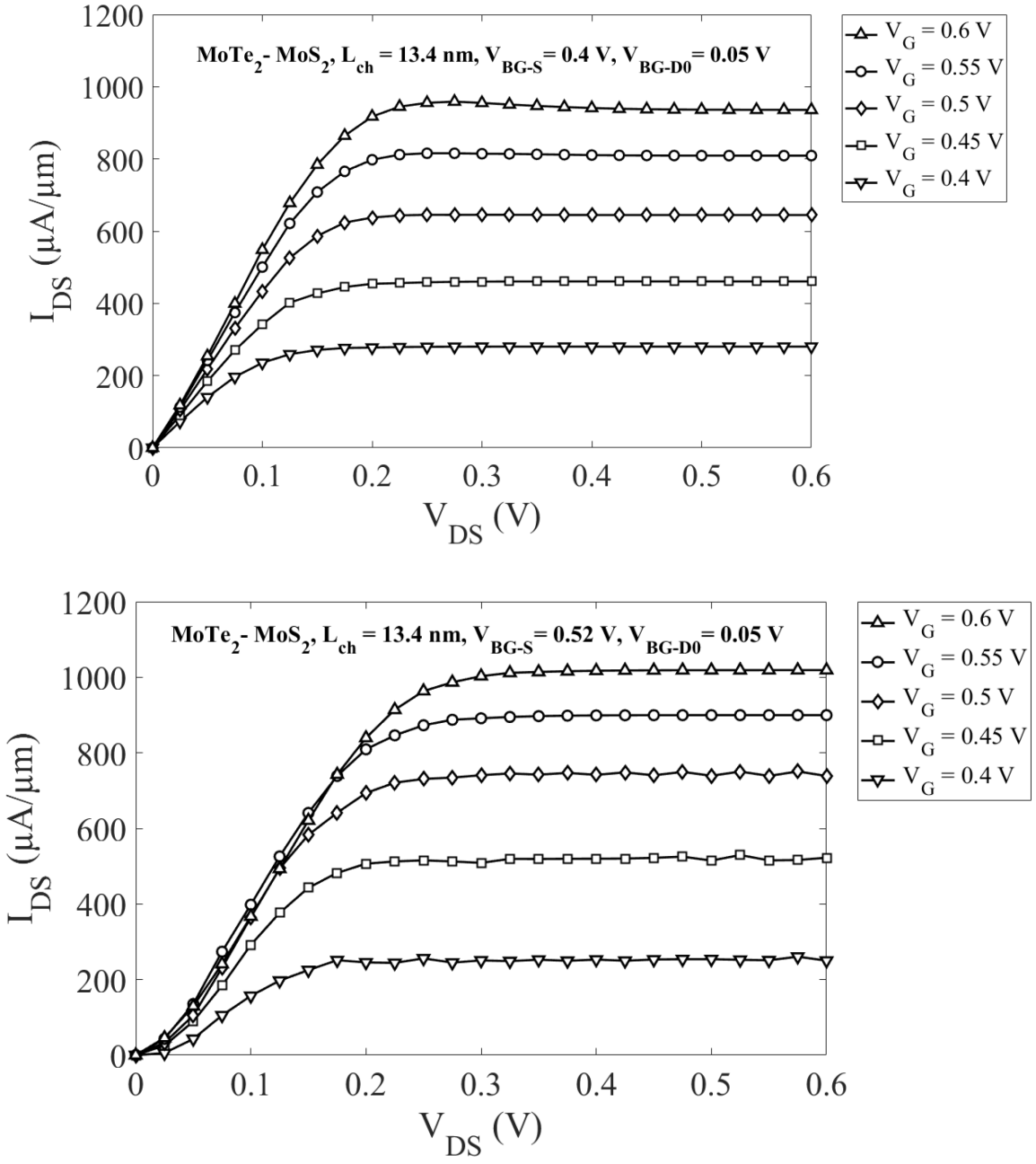


Figure 99. I_D-V_{DS} characteristics of the DBE $MoTe_2/MoS_2$ device at L_{ch} = 13.4 nm, ΔW = 0.05 eV and (top) $V_{BG\text{-}S}$ = 0.4 V (bottom) $V_{BG\text{-}S}$ = 0.52 V.

The characteristics are, as expected, similar to those of the standard in-plane heterojunction TFETs:

- at the optimal $V_{BG\text{-}S} = 0.52$ V, the drain CB is forced at energies higher than the source CB for $V_{DS} < 0.015$ V (see Figure 81), therefore the current is established only once this threshold drain voltage is reached. The current then follows a linear increase until saturation is reached around $V_{DS} = 0.25$ V
- at $V_{BG\text{-}S} = 0.4$ V, the characteristic is that of a standard transistor. The current increases linearly from $V_{DS} = 0$, and reaches saturation around $V_{DS} = 0.2$ V.

Although $V_{BG\text{-}S} = 0.52$ V has been identified as yielding the maximum I_{ON} for the DBE $MoTe_2/MoS_2$ device, the currents reported in Figure 99 at a given V_G are in the same range as those obtained at $V_{BG\text{-}S} = 0.4$ V.
This can be explained by the strong shift in threshold voltage (from 0.3 V to 0.35 V) and V_{OFF} (from 0.19 V to 0.3 V) which are both highlighted by the I_D-V_G characteristics shown in Figure 100.
Even though the current at any given V_G is comparable between the two considered source backgate voltages, the ON current is calculated at

- $V_{ON} = V_{OFF} + V_{DD} = 0.19 + 0.3 = 0.49$ V for $V_{BG\text{-}S} = 0.4$ V.
- $V_{ON} = V_{OFF} + V_{DD} = 0.3 + 0.3 = 0.6$ V for $V_{BG\text{-}S} = 0.58$ V.

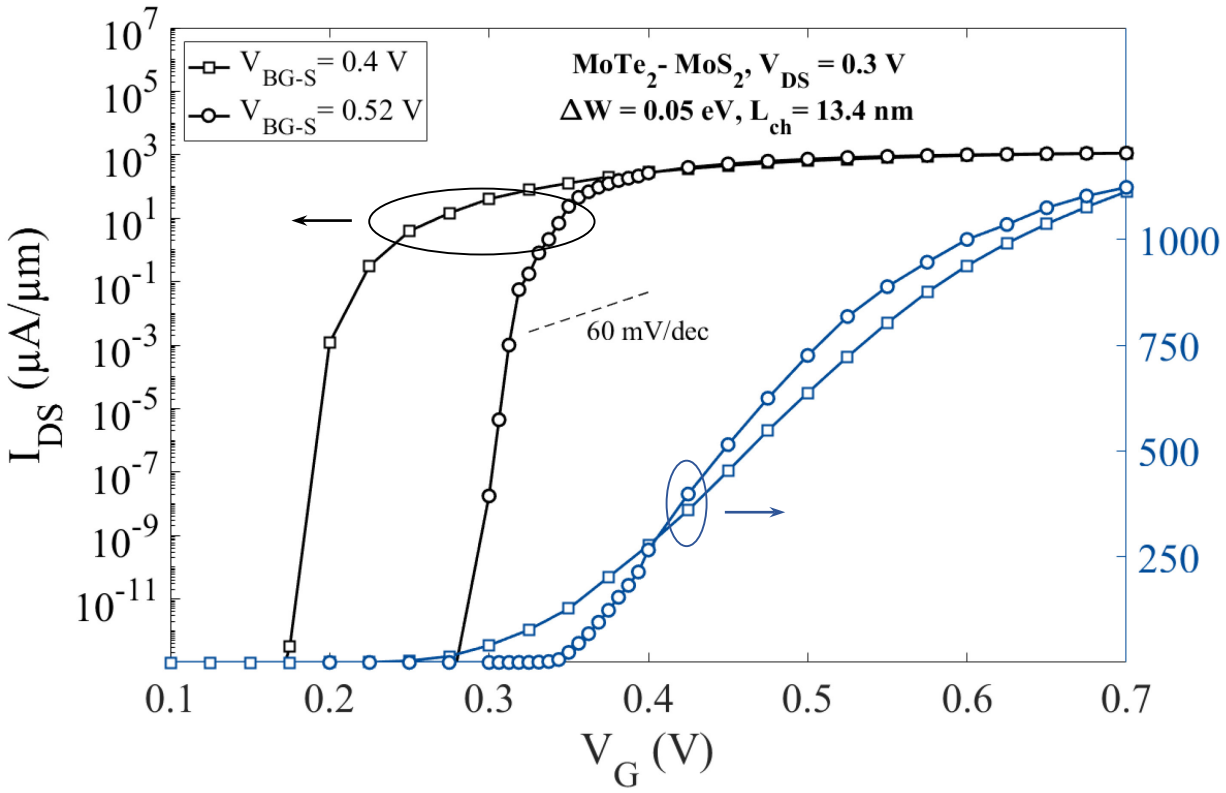


Figure 100. I_D-V_G characteristics of the DBE $MoTe_2/MoS_2$ device at $V_{DS} = 0.3$ V, $L_{ch} = 13.4$ nm, $\Delta W = 0.05$ eV and $V_{BG\text{-}S} = 0.4$ V and 0.52 V. The strong shift in both V_{OFF} and V_T is highlighted here.

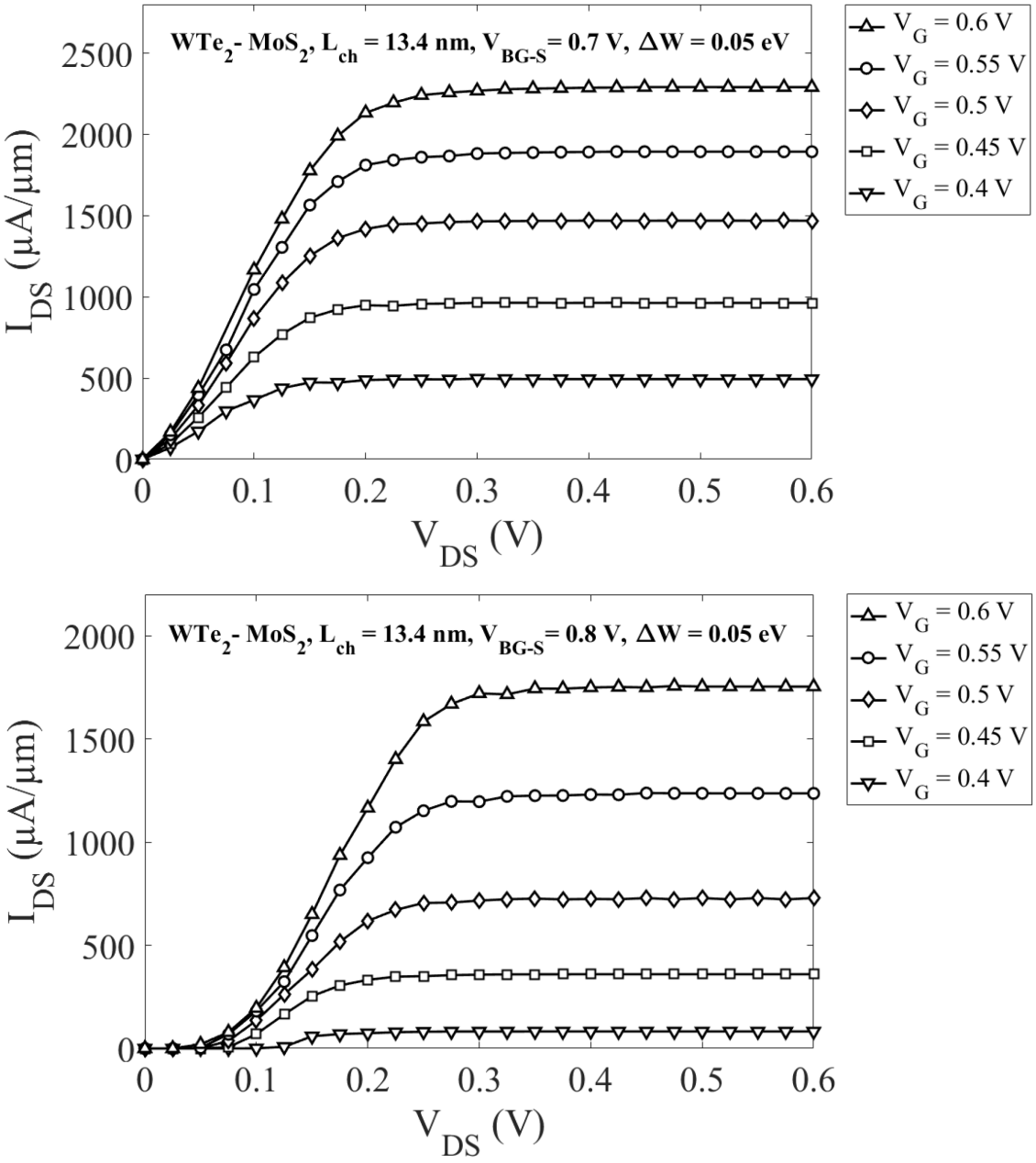


Figure 101. I_D-V_{DS} characteristics of the DBE WTe_2/MoS_2 device at L_{ch} = 13.4 nm, ΔW = 0.05 V and (top) $V_{BG\text{-}S}$ = 0.7 V (bottom) $V_{BG\text{-}S}$ = 0.8 V.

Similar observations can be made about the I_D-V_{DS} characteristics for the WTe_2/MoS_2 device shown in Figure 101.

In both the DBE $MoTe_2/MoS_2$ and WTe_2/MoS_2 devices, much like in the standard heterojunction TFETs, current saturation is reached at drain voltages as low as V_{DS} = 0.2 V; this peak performance reached at low V_{DS} highlights the potential of these DBE in-plane heterojunctions TFETs for ultra-low power operation.

Figure 102 shows the I_D-V_G characteristics of the $MoTe_2/MoS_2$ and the WTe_2/MoS_2 devices for L_{ch} = 13.4 nm, V_{DS} ranging from 0.1 V to 0.7 V and the optimal $V_{BG\text{-}S}$ and ΔW identified for each device, and highlights the absence of DITL in these devices.

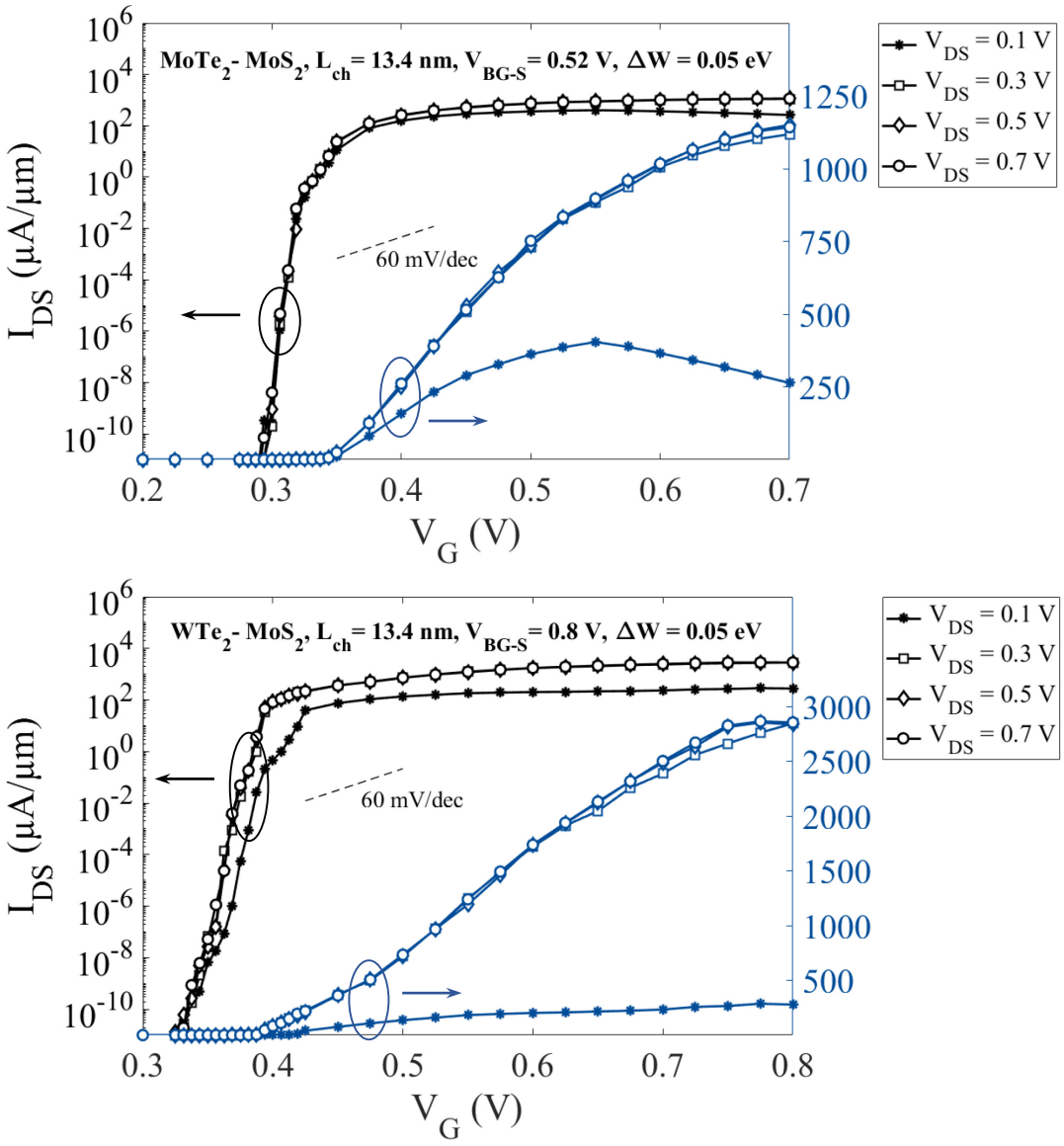


Figure 102. I_D-V_G characteristics of the DBE $MoTe_2/MoS_2$ and the WTe_2/MoS_2 devices for L_{ch} = 13.4 nm, V_{DS} ranging from 0.1 V to 0.7 V, and the optimal $V_{BG\text{-}S}$ and ΔW for each device as identified in Sections 6.3.1 and 6.3.3.

Once again, the behavior of these DBE devices is close to that of the standard TFETs: at very low V_{DS}, the drain CB lies at energies close to the source CB, and less current can flow; at higher V_{DS} however, both OFF and ON-state behaviors are unaffected by the drain voltage.

The current decrease observed at $V_G > 0.55$ V at $V_{DS} = 0.1$ V in the $MoTe_2/MoS_2$ device is due to the effect of the gate voltage on the source VB: at high V_G, the source VB at the source channel/interface is pulled down towards lower energies, narrowing the energy window in which current can flow. At higher V_{DS}, the drain CB lies at far lower energies, allowing for a wider energy interval in which the current saturates and therefore is not impacted by the marginal lowering of the source VB due to the gate voltage.

6.4 Conclusion on DBE in-plane heterojunction TFETs

The DBE $MoTe_2/MoS_2$ and WTe_2/MoS_2 devices studied in this chapter, while being only a minor variation from the standard TFETs studied in Chapter 4, show even greater promise for ultra-low power operation and device scaling. By using the same metal in all gates and applying $V_{BG\text{-}D} = V_G$, performance far superior to that of the standard TFETs can be reached.

- **Gate length scaling does not impact:** *SS* is unaffected by channel length, and the ON current only slightly increases in the case of very short channels (down to < 2 nm) for the considered workfunction offset. Such short channels would strongly alleviate most negative effects due to electron-phonon scattering.
- **Extremely low SS:** no matter the length of the channel, the devices yield ballistic *SS* below 7 mV/dec when the optimal workfunction offset is applied, and ballistic *SS* as low as 3 mV/dec were observed in some short channel devices
- **High ON/OFF ratio:** depending on the source backgate voltage applied to the device, ballistic ON/OFF ratios beyond 10^7 for the $MoTe_2/MoS_2$ device and 2×10^8 for WTe_2/MoS_2 device have been reported, no matter the channel length.
  For channel lengths below 10 nm, ballistic ON currents of 1.2×10^3 for the $MoTe_2/MoS_2$ device and 2.4×10^3 for WTe_2/MoS_2 device can be reached.
- **Good saturation even at low V_{DS}:** both devices saturate at drain voltages as low as $V_{DS} = 0.3$ V when the optimal backgate voltages are applied. Once again, this only strengthens their appeal as ultra-low power electronic switches.

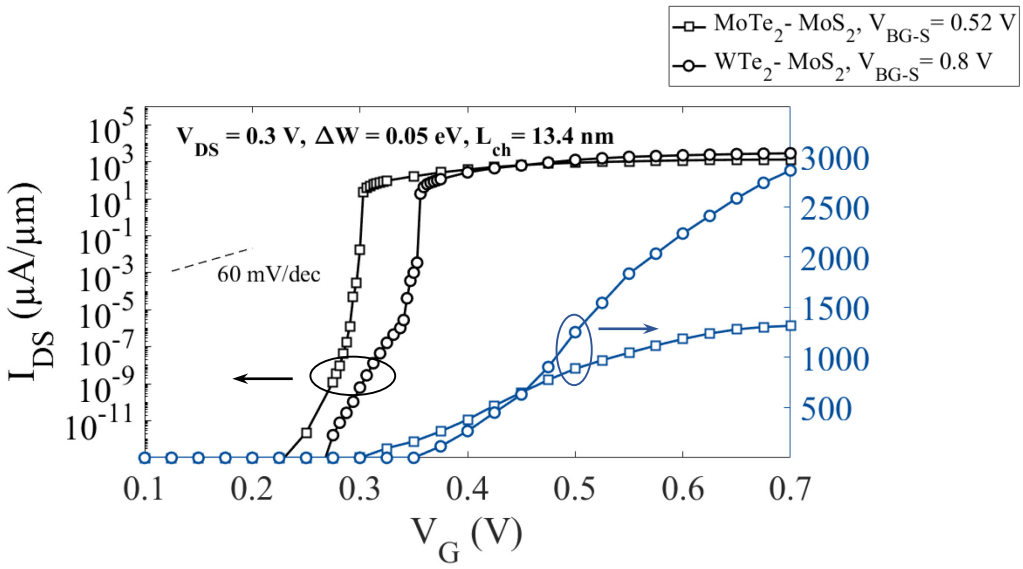


Figure 103. I_D-V_G characteristics of the backgate-enhanced $MoTe_2/MoS_2$ and the WTe_2/MoS_2 devices for $L_{ch} = 1.675$ nm, $V_{DS} = 0.3$ V, and the optimal $V_{BG\text{-}S}$ and ΔW for each device.

Chapter 7

Ungated-channel in-plane heterojunction TFETs

7.1 Introduction

The DBE devices investigated in Chapter 6 relied on the influence of the drain backgate on the CB in the drain contact to increase the performance of the standard $MoTe_2/MoS_2$ and WTe_2/MoS_2 heterojunction TFETs.
However, in those devices, a top-gate was still used to control the potential in the channel and, in conjunction with the drain backgate, control current flow in the device.
From the study of these devices came an idea for yet another device design based on these in-plane heterojunction TFETs: **since the drain backgate is used to force the energy level of the CB in the drain, is a channel gate truly necessary for these devices to operate well and achieve good performance ?**

As the results presented and analyzed in this chapter will show, these devices are fully able to operate without a channel gate. Current flow is therefore only controlled by the drain backgate voltage $V_{BG\text{-}D}$.
From an experimental standpoint, foregoing the top-gate would be extremely beneficial and streamline the material deposition and fabrication processes.

Much like the DBE devices presented in Chapter 6, this innovative device design is made possible by the 2D nature of the materials used in the active layer.
If traditional, bulk materials were used instead, standard chemical doping would have to be used instead of the electrostatic doping used in this work; this electrostatic doping via backgates affords us the active control of the band profile and potential in the contacts necessary for the DBE and "ungated-channel" (UC) devices to function.

These DBE and UC devices therefore make full use of the 2D nature of the materials considered in this work.

7.2 Device architecture

The architecture of the UC devices (as shown in Figure 104) is extremely close to that of the DBE devices presented previously.
The only difference is that these devices operate without a top-gate and that current flow is therefore controlled solely via the drain backgate voltage $V_{BG\text{-}D}$. In these devices, the workfunction of both backgates is 5.13 eV for both the $MoTe_2/MoS_2$ and WTe_2/MoS_2 devices.

The overall structure of the device is unchanged, with either $MoTe_2$ or WTe_2 being used as source material, and MoS_2 being used in the channel and drain. The channel, usually defined by the top-gate, is instead defined here as the region separating the source and drain backgates.

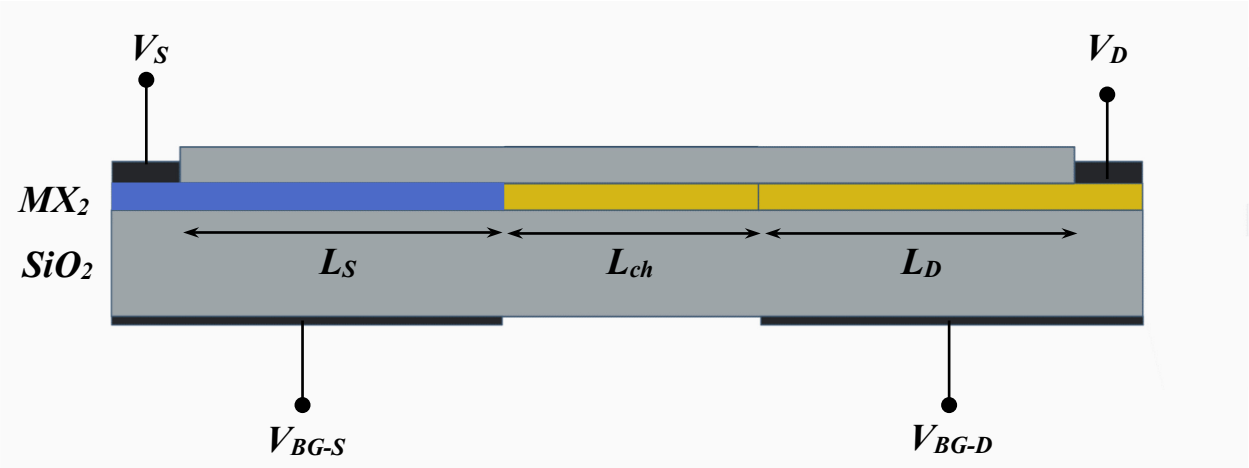


Figure 104. Device architecture for the considered ungated-channel in-plane heterojunction TFETs. One TMD acts as the source, and another as the channel/drain. SiO_2 is used as a buried oxide, and a high-κ dielectric as the top gate oxide. The voltage applied to the drain backgate is used to control current flow in the device, while the source backgate voltage remains constant.

7.3 Electronic transport simulations

As was the case for the TFETs studied in the previous chapters, overall performance as well as the influence of design parameters will be analyzed. Namely, the impact of the channel length and the source backgate voltage on figures of merit such as SS and I_{ON} will be investigated.

Since the drain backgate voltage is used to control current flow in lieu of a traditional top-gate, I_D-$V_{BG\text{-}D}$ characteristics will be shown instead of I_D-V_G characteristics.

7.3.1 Principle of operation

In this short section, I will highlight the principle of operation of these UC devices. While the examples presented here pertain to the $MoTe_2/MoS_2$ device, the mode of operation is the same in the WTe_2/MoS_2 device.

The I_D-$V_{BG\text{-}D}$ characteristic of a UC $MoTe_2/MoS_2$ device at $V_{DS} = 0.3$ V, $L_{ch} = 13.4$ nm and $V_{BG\text{-}S} = 0.53$ V is shown in Figure 105.
The first observation to make is that the device indeed behaves as a transistor: at low $V_{BG\text{-}D}$ the device is in the OFF state where no current flows; once a threshold $V_{BG\text{-}D}$ is reached however, the device goes to the ON state and current flows in the device. The transition from the OFF state to the ON state is extremely steep, requiring only a small increase in $V_{BG\text{-}D}$ below 0.02 V, which leads to a sub-threshold swing of roughly 3 mV/dec.
In this device, V_{OFF} (at which $I_{DS} = 10^{-5}$ µA/µm) ~ 0.35 V, therefore V_{ON} ~ 0.65 V, which leads to an ON current of roughly 750 µA/µm.
The performances of this initial transistor are already very promising, rivaling those of the DBE devices and of the very best standard TFETs analyzed in Chapters 5 and 6.

In order to highlight the principle of operation of these UC devices, Figure 106 shows the evolution of the highest VB and lowest CB in an UC device and a standard device during the OFF/ON transition, while Figure 107 shows the LDOS in the device at $V_G = 0.3$ V, 0.35 V, 0.3625 V and 0.5 V (red ellipses in Figure 105).

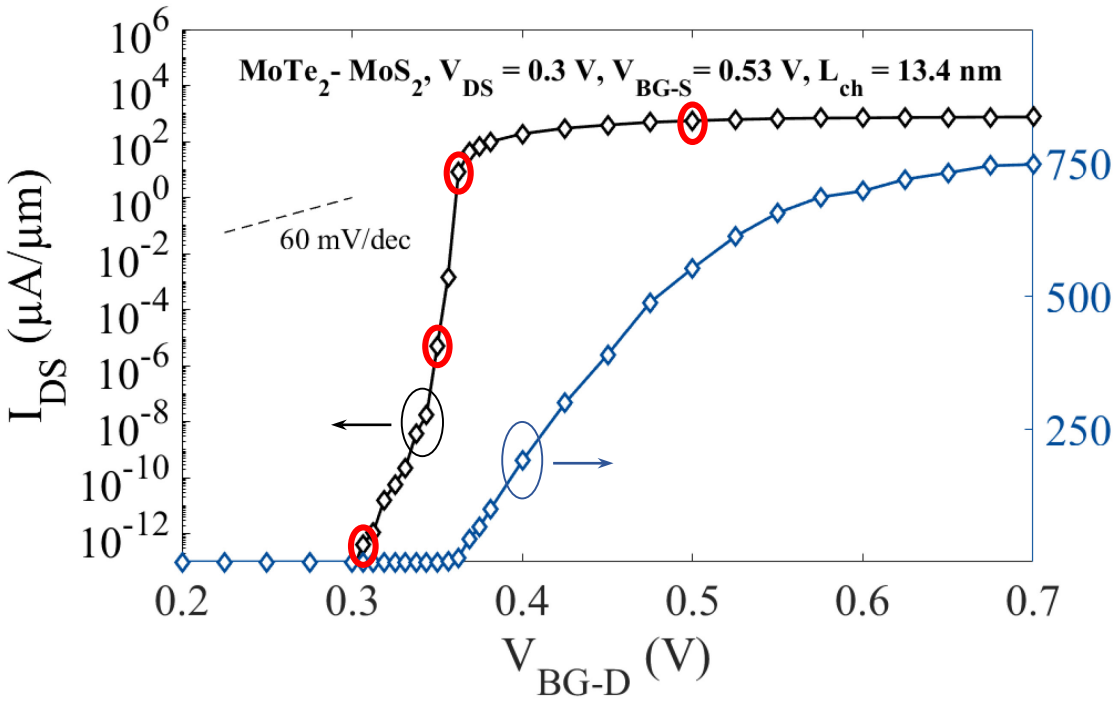


Figure 105. I_D-$V_{BG\text{-}D}$ characteristic of a UC $MoTe_2/MoS_2$ device at $V_{DS} = 0.3$ V, $L_{ch} = 13.4$ nm and $V_{BG\text{-}S} = 0.53$ V.

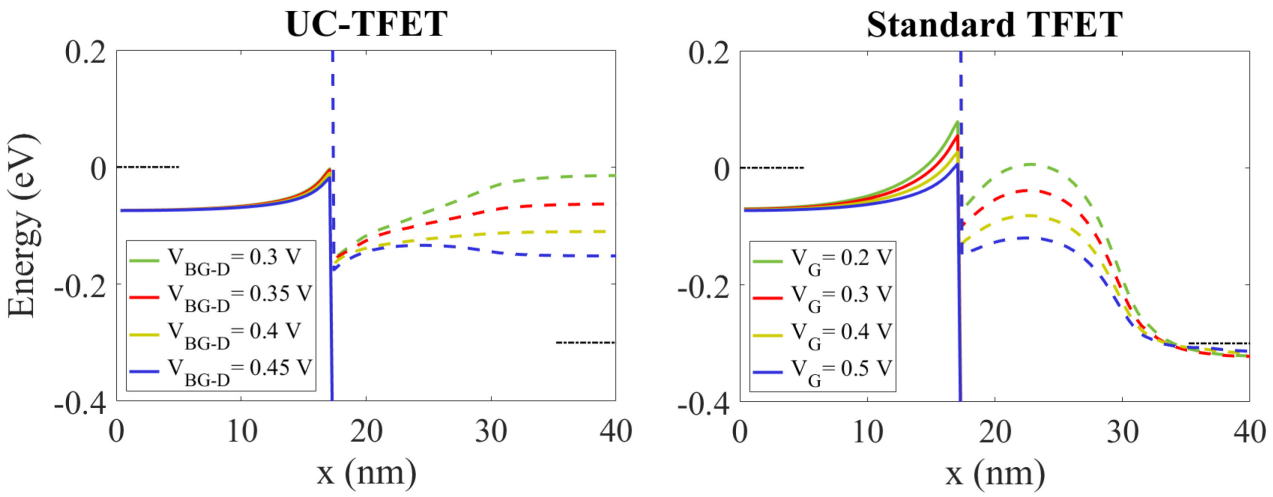


Figure 106. Highest VB (full lines) and lowest CB (dotted lines) highlighting the OFF/ON transition in (left) a UC-TFET and (right) a classic TFET. The black dashed lines represent the Fermi energies in the contacts.

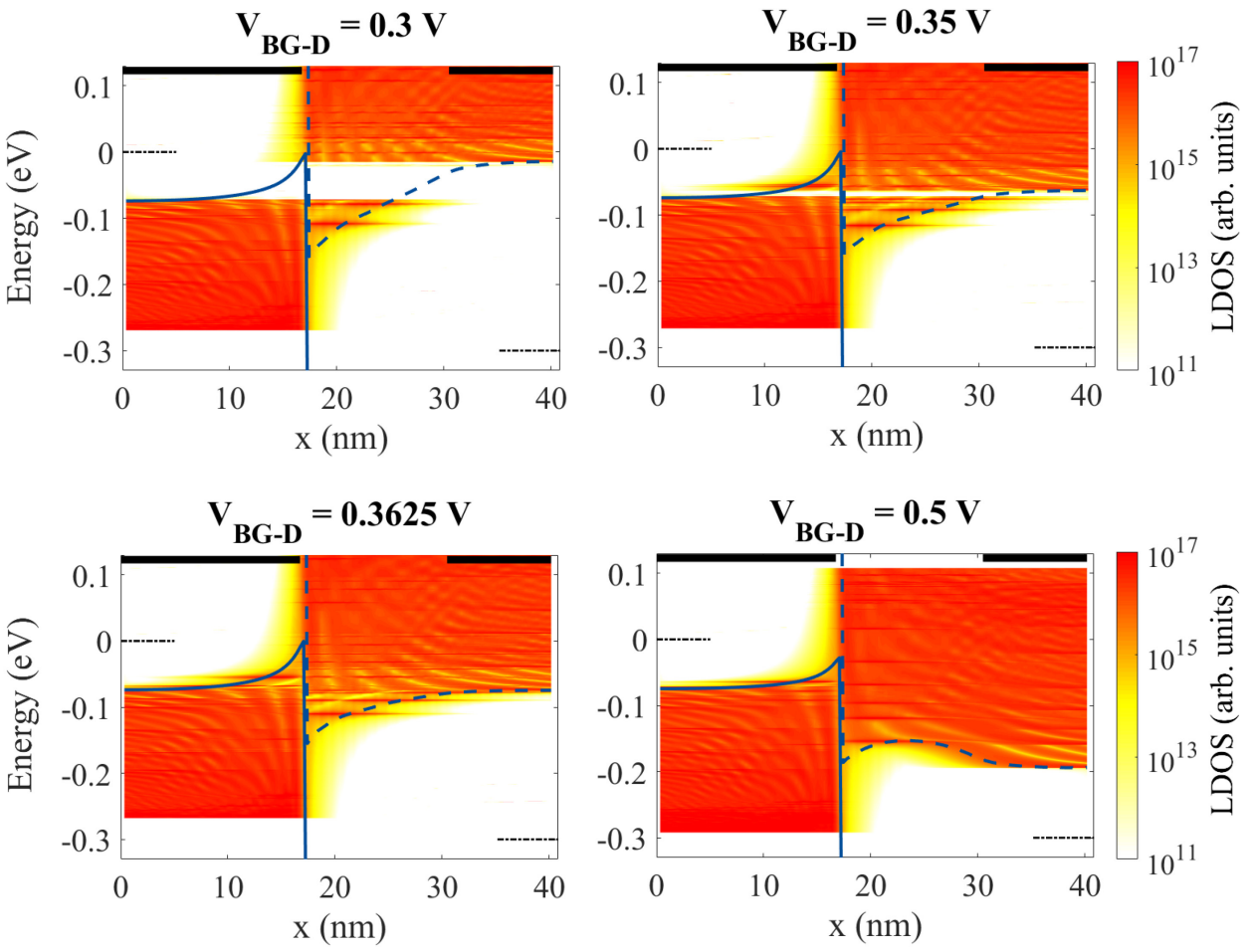


Figure 107. LDOS in the UC $MoTe_2/MoS_2$ device at the drain backgate voltages highlighted with red ellipses shown in Figure 105. The highest VB (full lines), lowest CB (dotted lines), and Fermi levels in the source and drain contacts (dashed black lines) are also represented. These LDOS figures highlight that the UC devices operate solely by modulating the energy of the CB in the drain contact.

The band profiles represented in Figure 106 highlight how the working principle of these UC devices differs from that of a standard TFET:

- Standard TFET: the static source and drain backgate voltages force the potential and the energy level of the bands in the contacts. The top-gate voltage is used to control the profile of the bands in the channel: as V_G increases, the channel CB is pushed towards lower energies, allowing carriers to flow from source to drain.

- UC TFET: only the source backgate voltage is static, and it forces the energy level of the band in the source contact. The drain backgate voltage dynamically controls the energy level of the band in the drain: as it increases, the drain CB is pushed down towards lower energies. As soon as $E_{CB\text{-}drain} < E_{VB\text{-}source}$, current flows freely from the source to the drain, and the transistor turns ON (see the current densities shown in Figure 108).

As was the case for the DBE devices, this radically different working principle frees the UC devices from traditional FET shortcomings such as source-to-drain tunneling and other short-channel effects: since no states are available to tunnel to at low $V_{BG\text{-}D}$, the device is in a true OFF state where no current can occur, no matter L_{ch}.
As soon as a high enough $V_{BG\text{-}D}$ is reached however, the broken gap heterojunction formed by the carefully selected strained TMDs ensures that carriers can flow from the source VB to the channel/drain CB unabated.

The influence of the length of the channel on the performance of these UC devices will now be investigated.

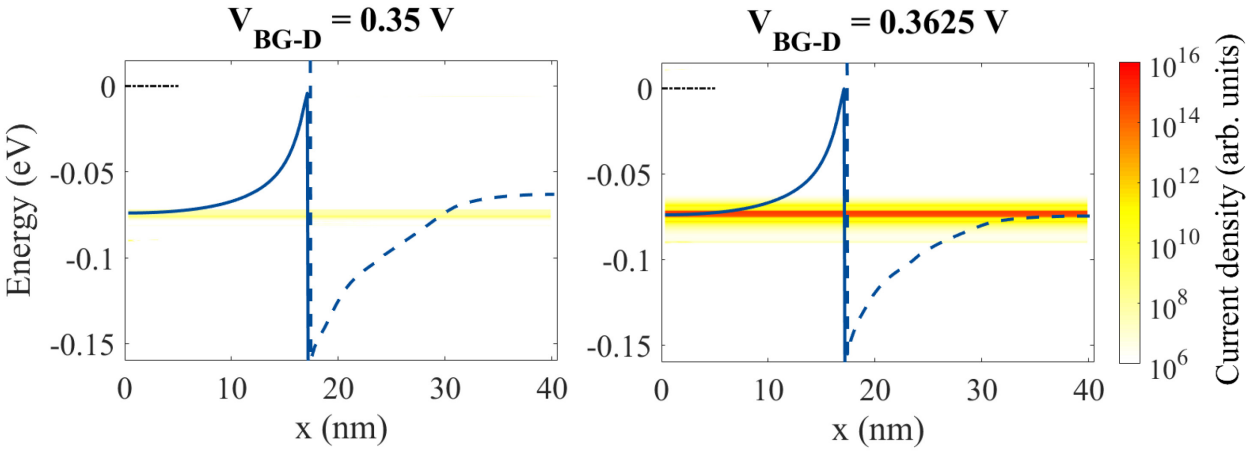


Figure 108. Current density in the UC $MoTe_2/MoS_2$ device at $V_{BG\text{-}D} = 0.35$ V and $V_{BG\text{-}D} = 0.3625$ V. The highest VB (full lines), lowest CB (dotted lines), and Fermi levels in the source and drain contacts (dashed black lines) are also represented. These current density figures highlight the infinitesimal increase in $V_{BG\text{-}D}$ (0.0125 V) required to transition from the OFF to the ON state.

7.3.2 Influence of channel length

While channel length had a strong impact on the performance of the standard TFETs studied in Chapters 5, the DBE devices studied in Chapter 6 were largely impervious to the influence of L_{ch} (except in the case of very short channels).
In this section, the influence of channel length in these UC devices will be analyzed in discussed.

I_D-$V_{BG\text{-}D}$ characteristics for both the UC $MoTe_2/MoS_2$ and WTe_2/MoS_2 devices at $V_{DS} = 0.3$ V, $V_{BG\text{-}S} = 0.53$ V and 0.8 V (resp.) and channel lengths ranging from 1.675 nm to 26.8 nm are shown in Figure 109.

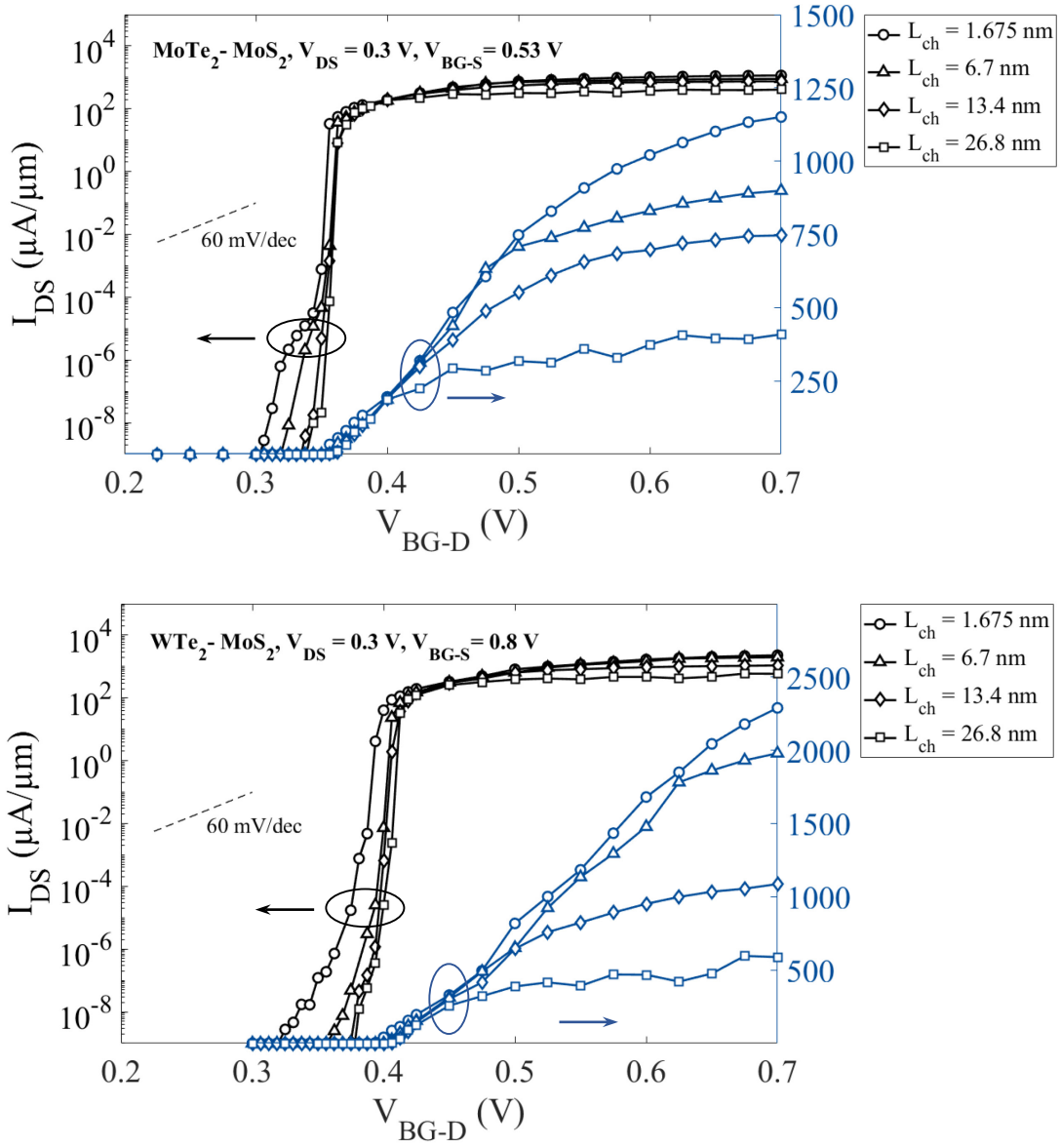


Figure 109. I_D-$V_{BG\text{-}D}$ characteristics for both the UC (top) $MoTe_2/MoS_2$ and (bottom) WTe_2/MoS_2 devices at $V_{DS} = 0.3$ V, $V_{BG\text{-}S} = 0.53$ V and 0.8 V (resp.) and channel lengths ranging from 1.675 nm to 26.8 nm. Although it has no effect on SS and V_T, channel length strongly impacts the behavior at high $V_{BG\text{-}D}$ and therefore I_{ON}.

From these I_D-$V_{BG\text{-}D}$ characteristics, two main observations applying to both devices can be made:

- *SS* is not influenced by channel length: whether L_{ch} = 1.675 nm or 26.8 nm, the steepness of the slope in the sub-threshold regime remains constant. Both devices yield $SS \sim 3$ mV/dec across all channel lengths.
- The ON-state is strongly impacted by channel length: for $V_{BG\text{-}D} > 0.45$ V, the current in the ON-state decreases as L_{ch} increases. For instance, in the $MoTe_2/MoS_2$ device, current at $V_{BG\text{-}D} = 0.6$ V drops from 1030 µA/µm for a 1.675 nm channel to 450 µA/µm for a 26.8 nm; I_{ON} is therefore strongly impacted.

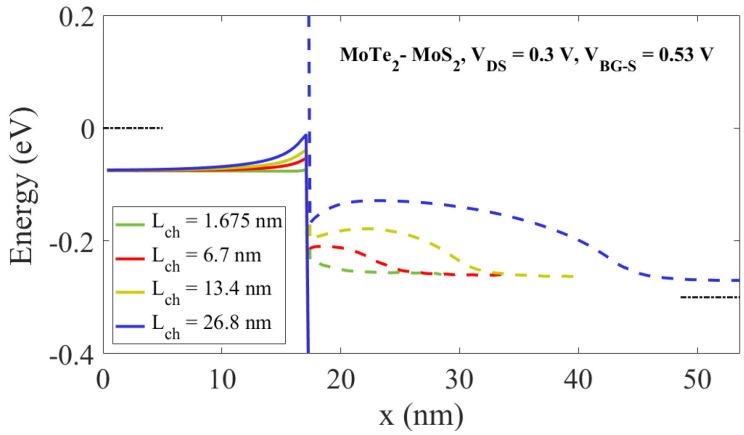


Figure 110. Highest VB (full lines) and lowest CB (dotted lines) in the UC $MoTe_2$ device in the ON state for channel lengths ranging from 1.675 nm to 26.8 nm. As L_{ch} increases, the impact of the drain backgate voltage on the CB in the channel is reduced, and the band can reach higher energies.

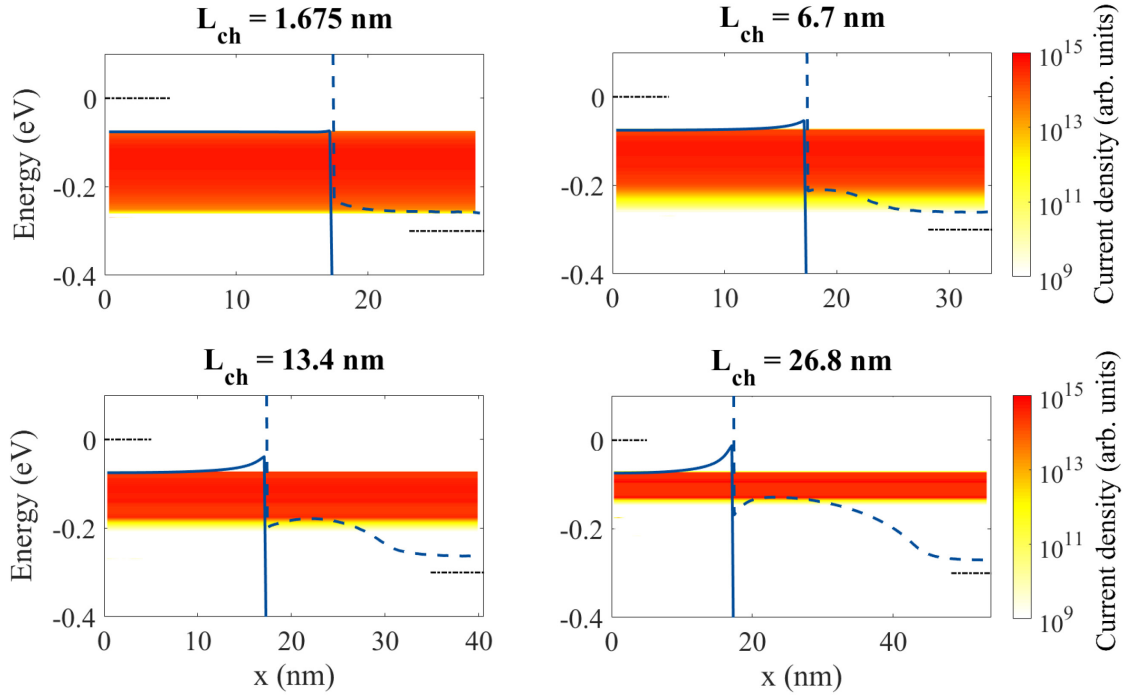


Figure 111. Current density, highest VB (full line) and lowest CB (dotted line) in the UC $MoTe_2$ device in the ON state for channel lengths ranging from 1.675 nm to 26.8 nm. As L_{ch} increases, the width of the energy window in which current can flow is drastically reduced, impacting the ON current.

These figures confirm the observations made from the I_D-$V_{BG\text{-}D}$ characteristics shown in Figure 109: *SS* is not affected by L_{ch} and remains < 5 mV/dec in both devices; I_{ON} however is strongly affected by channel length, and is reduced by over 50% (75%) when L_{ch} increases from 2 nm to 26.8 nm in the $MoTe_2/MoS_2$ (WTe_2/MoS_2) device; finally, due to the absence of a top-gate, the threshold voltage V_T is not influenced by L_{ch}, unlike in the standard and DBE devices. As soon as $V_{BG\text{-}D}$ induces $E_{CB\text{-}D} < E_{VB\text{-}S}$, the device switches ON, no matter the channel length.

The band profiles and current densities shown in Figure 110 and Figure 111 highlight the origin of the strong decrease of I_{ON} when the channel length increases.

As the channel length increases, the influence of the drain backgate voltage on the CB in the channel is reduced. Therefore, even though at a given $V_{BG\text{-}D}$ the energy level of the band in the drain is the same for all channel lengths, the channel CB can reach higher energies, narrowing the width of the energy window in which current flows.

This phenomenon is especially apparent in the current density figures shown for several channel lengths (see Figure 111).

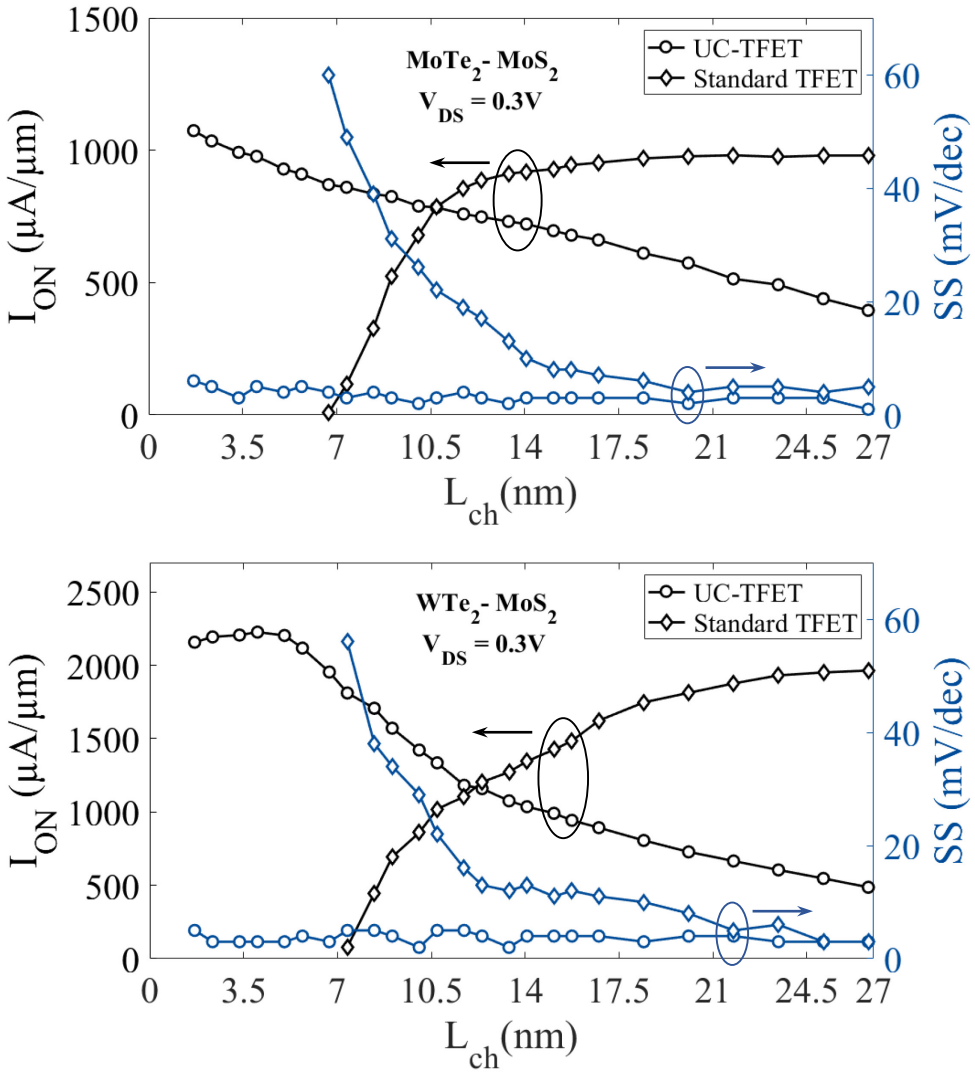


Figure 112. Influence of the channel length on *SS* and I_{ON} in the UC and standard (top) $MoTe_2/MoS_2$ and (bottom) WTe_2/MoS_2 devices.

The direct influence of channel length on I_{ON} and SS in these UC devices is shown in Figure 112, alongside its impact on the same figures of merit in the standard TFETs for comparison purposes.
Although these devices yield peak performance when the channel is kept short (preferably below 10 nm), they have a strong advantage compared the standard TFETs: they switch from the OFF to the ON state with a minimal increase in $V_{BG\text{-}D}$ thanks to their < 5 mV/dec SS no matter the channel length. The standard TFETs, on the other hand, require a channel length > 20 nm to reach this kind of performance.

However, when compared to the DBE TFETs, in which both SS and I_{ON} remain constant and optimal no matter the channel length, this strong decrease in I_{ON} puts the UC devices at a disadvantage.
In the case of extremely short channels, the devices yield similar performance; however, for channel lengths beyond 5 nm the DBE devices yield far higher ON currents as is evidenced by Figure 113.

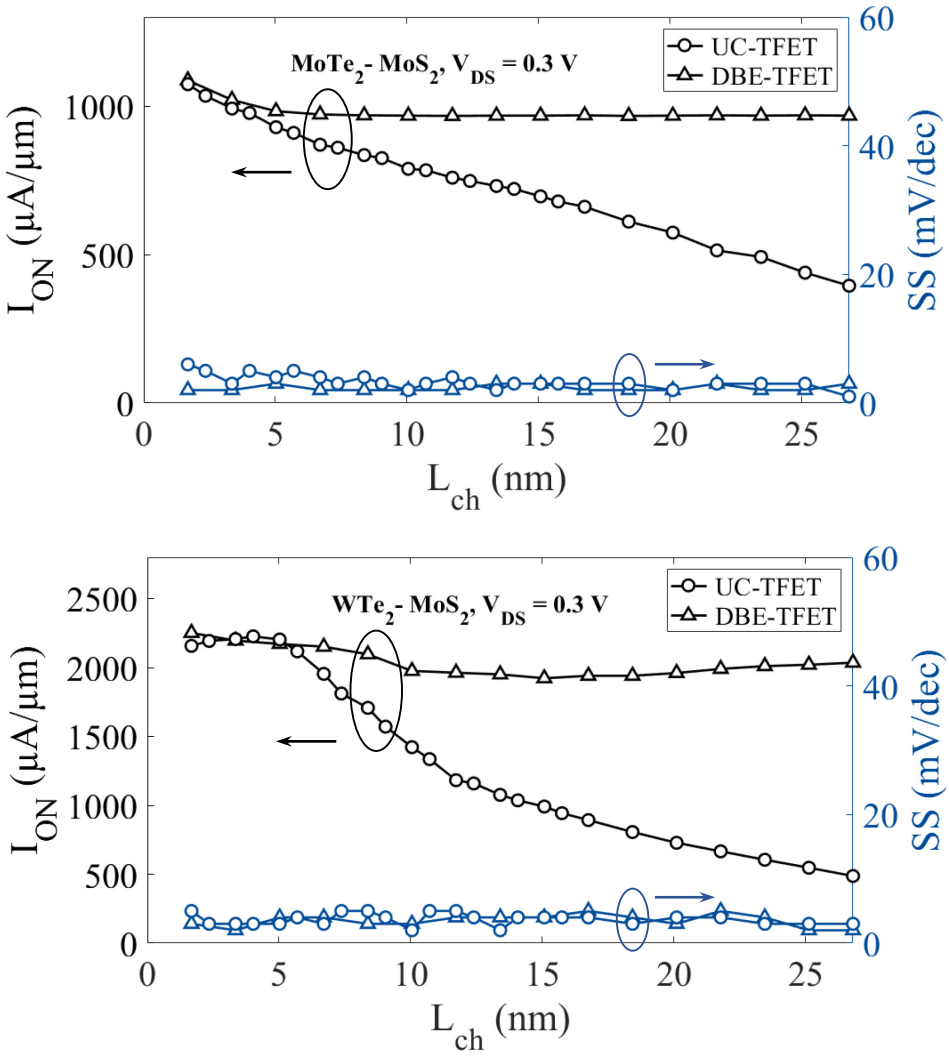


Figure 113. Influence of the channel length on SS and I_{ON} in the UC and DBE (top) $MoTe_2/MoS_2$ and (bottom) WTe_2/MoS_2 devices.

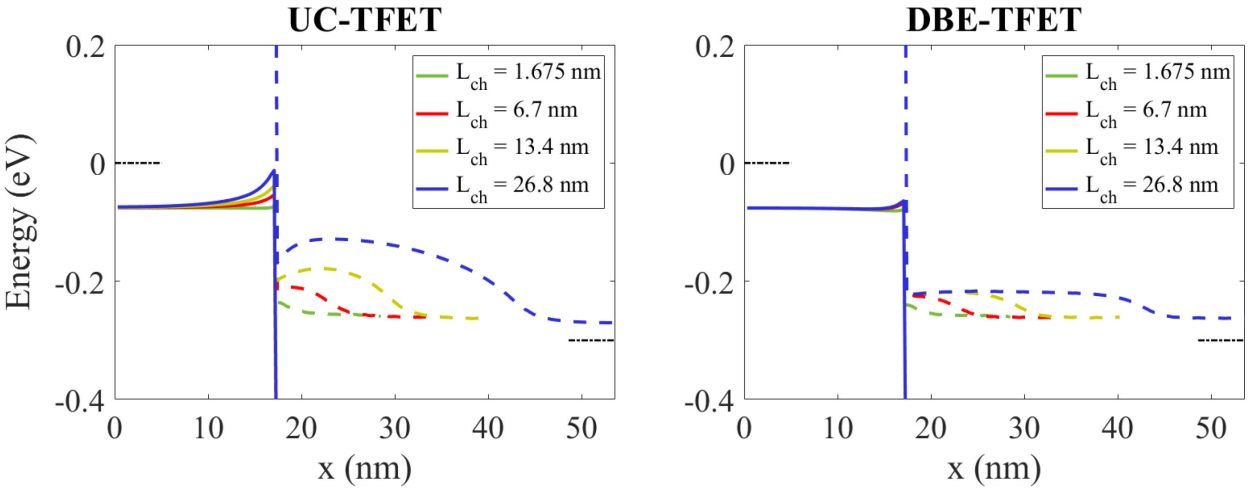


Figure 114. Highest VB (full lines) and lowest CB (dotted lines) in the (left) UC and (right) DBE $MoTe_2/MoS_2$ device in the ON state, for channel lengths ranging from 1.675 nm to 26.8 nm. In the DBE device, the voltage applied to the top-gate forces the energy level of the CB in the channel, preventing it from being modified by channel length.

The band profiles of both the UC and DBE $MoTe_2/MoS_2$ devices shown in Figure 114 highlight the origin of this difference in behavior regarding channel length:

- In the UC device, as explained earlier, the influence of $V_{BG\text{-}D}$ on the channel CB is reduced as channel length increases, and the band can therefore adapt to the potential over a longer distance, gradually narrowing the width of the energy window in which current can flow.
- In the DBE device however, the electric field generated by the top-gate forces the level of the CB in the channel at the same energy no matter the channel length, and I_{ON} is therefore not impacted (except in the case of very short channels).

These UC devices therefore have a surprising relationship with channel lengths: their performance strongly increases when L_{ch} is shortened.
In standard FETs, channel scaling tends to strongly degrade performance and, when too aggressive, prevents the device from operating as a transistor altogether. In these devices however, channel scaling is very much encouraged as it actually favors performance, even in the case of extremely short channels (< 2 nm), and would strongly reduce the impact of electron-phonon scattering on device performance.

Although very short channels are required to reach peak performance in these UC devices, high ON/OFF ratios (beyond 5×10^7) are nonetheless observed in both devices at $L_{ch} \sim 20$ nm, which remains extremely promising.

7.3.3 Influence of source backgate voltage

As was the case in both the standard and DBE TFETs, the source backgate voltage (which controls the potential profile and the energy level of the bands in the source contact) has a strong influence on the performance of these UC devices.

Figure 115 shows the I_D-$V_{BG\text{-}D}$ characteristics of the UC $MoTe_2/MoS_2$ and WTe_2/MoS_2 devices at $V_{DS} = 0.3$ V, $L_{ch} = 13.4$ nm and various $V_{BG\text{-}S}$ as well as the direct influence of the source backgate voltage on the ON current in each device.

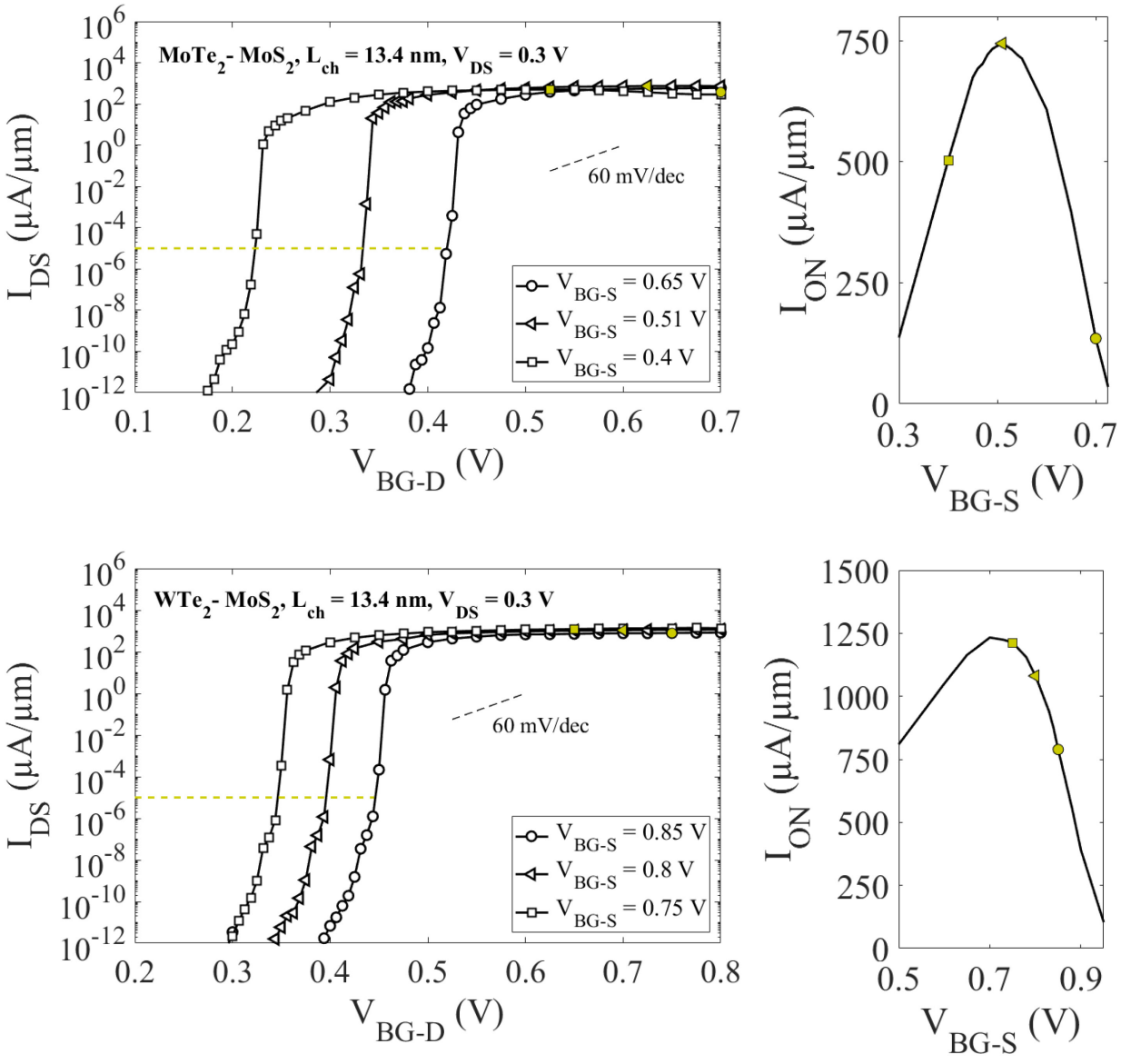


Figure 115. Left: I_D-$V_{BG\text{-}D}$ characteristics of the UC (top) $MoTe_2/MoS_2$ and (bottom) WTe_2/MoS_2 devices at $V_{DS} = V_{DD} = 0.3$ V, $L_{ch} = 13.4$ nm and various $V_{BG\text{-}S}$. The gold dotted line represents $I_{OFF} = 10^{-5}$ µA/µm, and the gold markers highlight the resulting I_{ON} measured at $V_{BG\text{-}D} = V_{ON} = V_{OFF} + V_{DD}$. Right: Influence of $V_{BG\text{-}S}$ on the ON current in the device.

The source backgate voltage has a similar influence on these devices than on both the standard and DBE TFETs shown in Sections 5.3.4 and 6.3.3: *SS* is not impacted, and I_{ON} follows a somewhat parabolic evolution around an optimal value of $V_{BG\text{-}S}$ in both devices.

The reason for this evolution is the same as in the devices previously studied, and was detailed in Section 5.3.4 in the case of the standard TFETs.

Thanks to this study, the optimal source backgate voltages (at $V_{DS} = 0.3$ V and $L_{ch} = 13.4$ nm) can be identified as:

- $V_{BG\text{-}S} = 0.51$ V for the UC $MoTe_2/MoS_2$ device.
- $V_{BG\text{-}S} = 0.73$ V for the UC WTe_2/MoS_2 device.

7.3.4 Drain voltage characteristics and DITL

Both the standard and DBE devices have exhibited current saturation for drain voltages for supply voltages as low as 0.2 V, and strong resistance to DITL; both of these features are very promising for ultra-low voltage operation. Similar behavior can be expected in the UC devices thanks to their strong resemblance to these devices.

I_D-V_{DS} characteristics for the UC $MoTe_2/MoS_2$ device at $L_{ch} = 10.05$ nm and $V_{BG\text{-}S} = 0.35$ V at various $V_{BG\text{-}D}$ are shown in Figure 116. Standard transistor behavior can be observed; the relatively low currents (which range from 200 µA/µm to 360 µA/µm) observed are due to the channel length: as shown in Section 7.3.2, even shorter channels are required for these UC devices to yield peak performance.

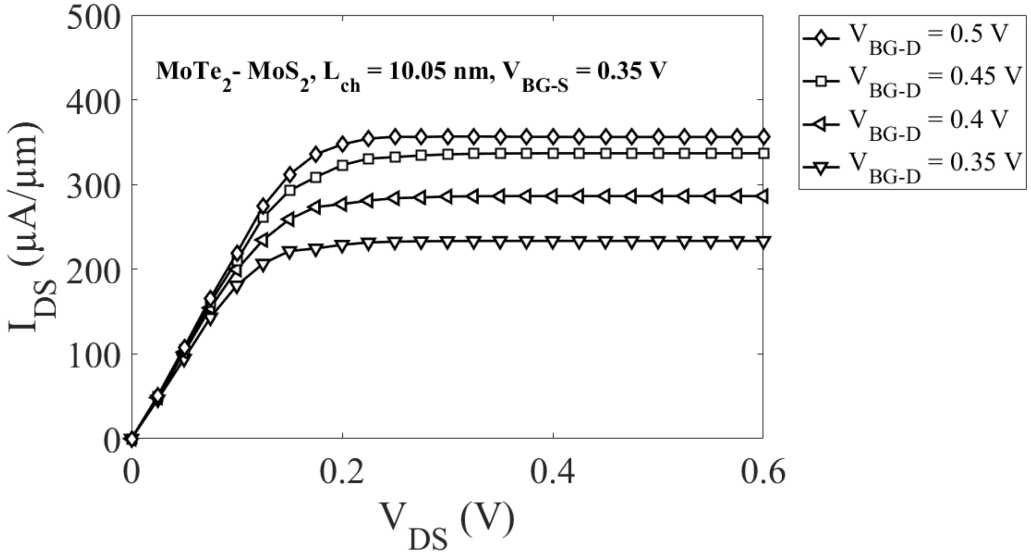


Figure 116. I_D-V_{DS} characteristics for the UC $MoTe_2/MoS_2$ device at $L_{ch} = 10.05$ nm, $V_{BG\text{-}S} = 0.35$ V and $V_{BG\text{-}D}$ ranging from 0.35 V to 0.5 V; standard transistor behavior can be observed.

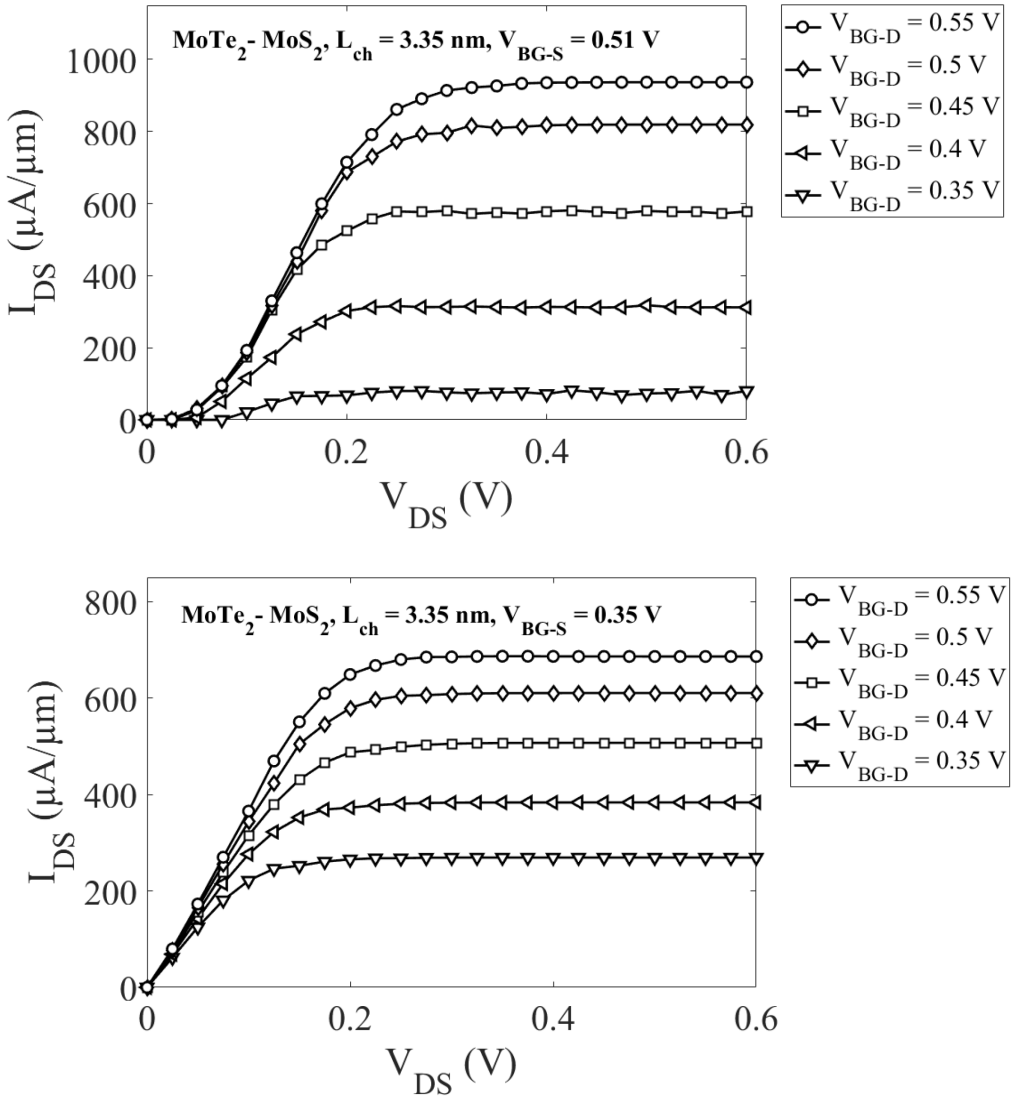


Figure 117. I_D-V_{DS} characteristics for the UC $MoTe_2/MoS_2$ device at L_{ch} = 3.35 nm, $V_{BG\text{-}D}$ ranging from 0.35 V to 0.5 V and (top) $V_{BG\text{-}S}$ = 0.51 V (bottom) $V_{BG\text{-}S}$ = 0.35 V.

I_D-V_{DS} characteristics for the UC $MoTe_2/MoS_2$ device at a shorter channel length of 3.35 nm at $V_{BG\text{-}S}$ = 0.35 V as well as $V_{BG\text{-}S}$ = 0.51 V (the optimal source backgate voltage identified in Section 7.3.3) are shown in Figure 117.

As was the case for all previous transistors, standard transistor behavior can be observed at low $V_{BG\text{-}S}$ while, at the optimal $V_{BG\text{-}S}$, a threshold V_{DS} (0.05 V in this case) has to be reached before current can be established. As explained in the previous chapters, at this source backgate voltage the drain CB is forced at higher energies than the source VB at very low V_{DS} which explains the absence of current. Much higher currents (up to 1000 µA/µm) are reached in these devices, thanks to their very short channel which favors performance in these UC devices. In all cases, the current saturates at $V_{DS} \sim 0.225$ V, much like in the DBE and standard devices. Similar observations can be made about the WTe_2/MoS_2 device, for which I_D-V_{DS} characteristics are shown in Figure 118.

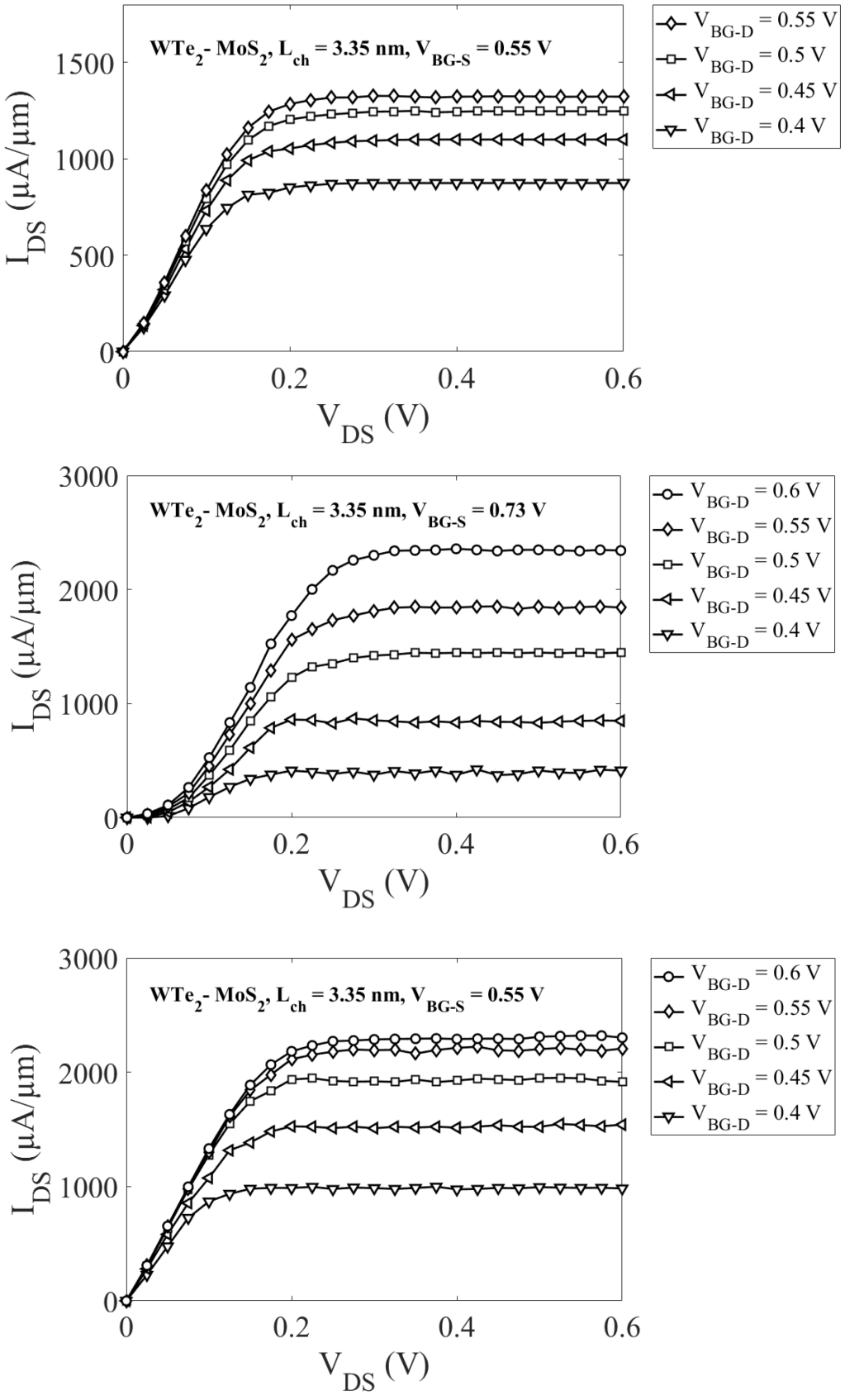


Figure 118. I_D-V_{DS} characteristics for the UC WTe_2/MoS_2 device at $V_{BG\text{-}D}$ ranging from 0.35 V to 0.5 V and (top) L_{ch} = 10.05 nm, $V_{BG\text{-}S}$ = 0.55 V, (middle) L_{ch} = 3.35 nm, $V_{BG\text{-}S}$ = 0.73 V, (bottom) L_{ch} = 3.35 nm, $V_{BG\text{-}S}$ = 0.55 V.

I_D-$V_{BG\text{-}D}$ characteristics for both UC devices at V_{DS} ranging from 0.1 V to 0.7 V, L_{ch} = 3.35 nm and the optimal source backgate voltage as identified for each device in Section 7.3.3 are shown in Figure 119.

Much like the standard and DBE TFETs presented previously, these UC devices are insensitive to DITL: threshold voltage is not impacted for supply voltages ranging from 0.1 V to 0.7 V, and behavior in both the OFF and ON state is unchanged for V_{DS} ranging from 0.3 V to 0.7 V.

As was the case in the previous devices, lower currents are observed at V_{DS} = 0.1 V due to the source backgate voltage used: the $V_{BG\text{-}S}$ identified as optimal to maximize ON current forces the source VB to energy levels higher than the drain CB at very low V_{DS} (a more detailed explanation is given in Section 5.3.5 and band profiles are shown in Figure 81).

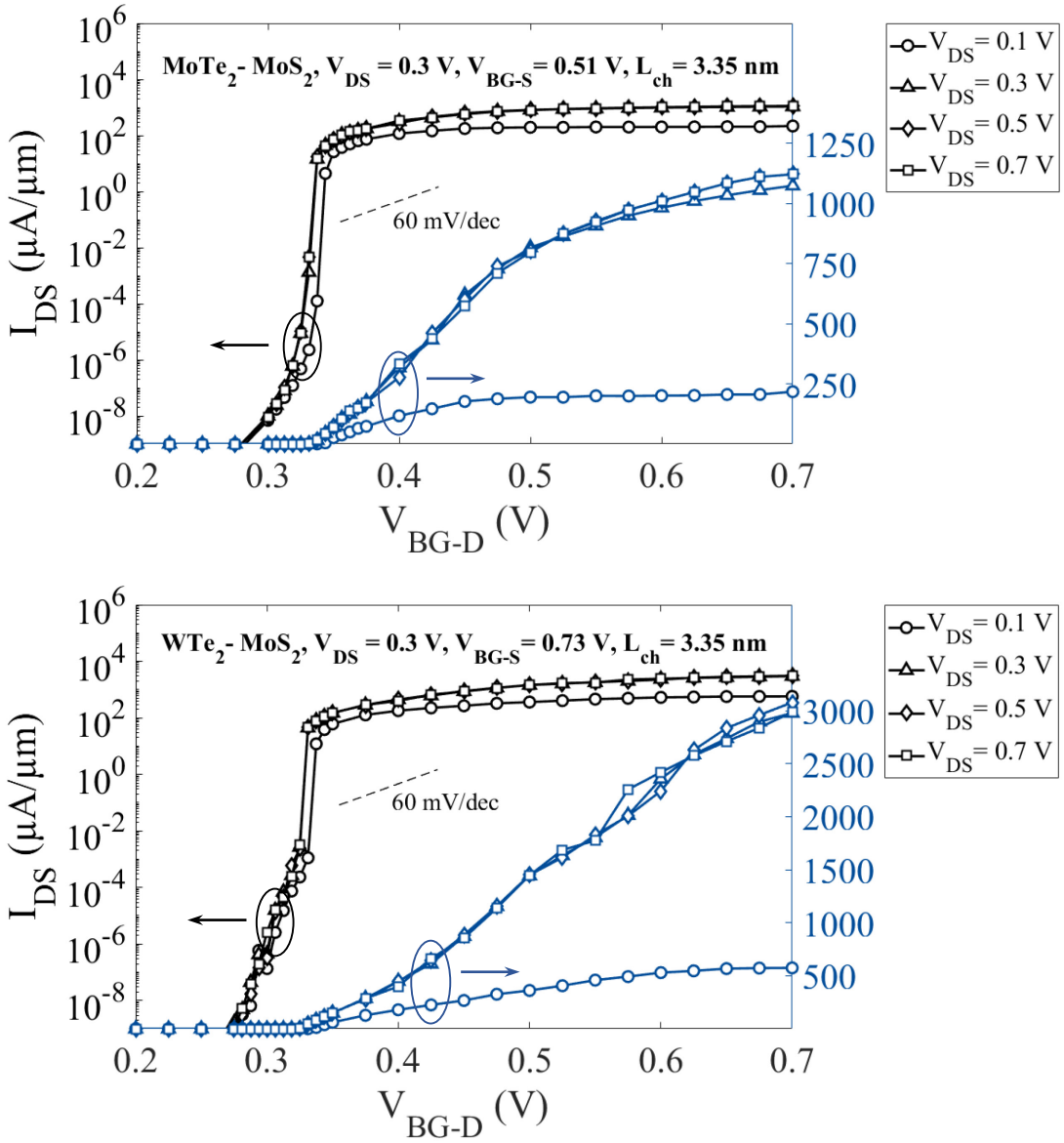


Figure 119. I_D-$V_{BG\text{-}D}$ characteristics of the UC $MoTe_2/MoS_2$ and the WTe_2/MoS_2 devices for L_{ch} = 3.35 nm, V_{DS} ranging from 0.1 V to 0.7 V, and the optimal $V_{BG\text{-}S}$ for each device.

7.4 Conclusion on ungated-channel in-plane heterojunction devices

The UC $MoTe_2/MoS_2$ and WTe_2/MoS_2 devices studied in this chapter share many of the traits exhibited in both the standard and especially the DBE devices studied in Chapters 5 and 6. They exhibit the following properties:

- **Device scaling strongly favors performance:** *SS* is unaffected by the channel length variation, and ON current strongly increases as the channel is shortened, yielding I_{ON} comparable to that of the DBE devices in very short channel devices.
- **Extremely low SS:** no matter the length of the channel and $V_{BG\text{-}S}$ applied, the devices yield $SS < 5$ mV/dec. As a result, a minuscule 0.0125 V increase in $V_{BG\text{-}D}$ is enough for the device to transition from a fully OFF to fully ON state.
- **High ON/OFF ratio:** depending on the source backgate voltage applied to the device, ballistic ON currents of 1.2×10^3 for the $MoTe_2/MoS_2$ device and 2.4×10^3 for the WTe_2/MoS_2 device can be reached in the case of very short channels (< 5 nm). Although I_{ON} decreases as channel length increases, promising ballistic ON/OFF ratios of 7×10^7 are obtained for $L_{ch} \sim 20$ nm in both devices.
- **Good saturation even at low V_{DS}:** both UC devices are shown to saturate at very low drain voltages ($V_{DS} = 0.25$ V). Peak performance can therefore be reached at minimal supply voltage, which is promising for ultra-low power operation.
- **No top-gate is required to operate these devices**, which would facilitate and streamline the fabrication process.

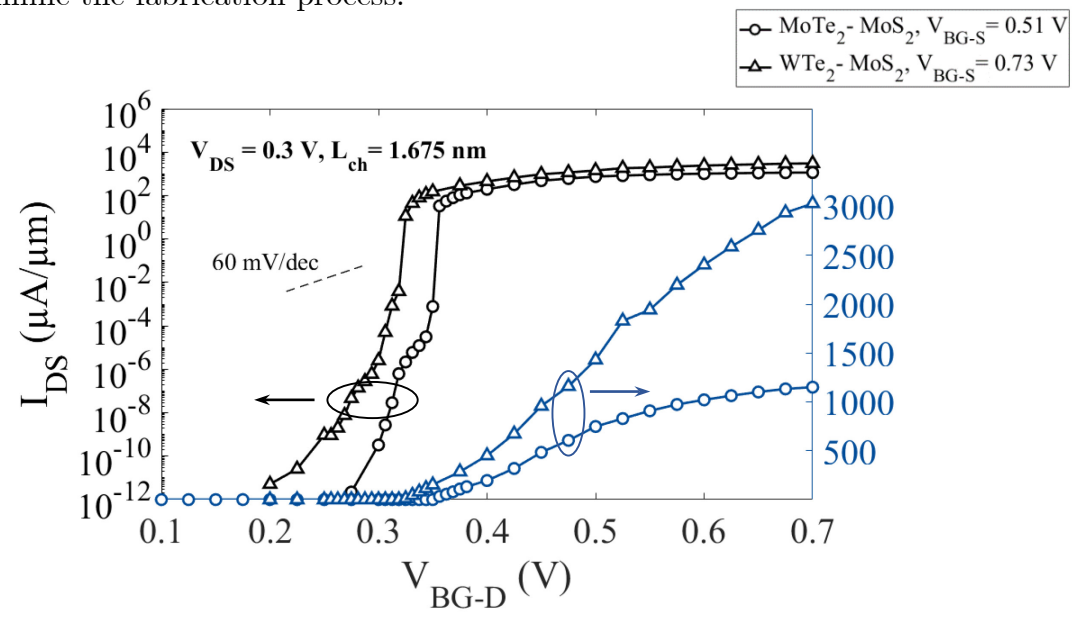


Figure 120. I_D-V_G characteristics of the UC $MoTe_2/MoS_2$ and the WTe_2/MoS_2 devices for $L_{ch} = 1.675$ nm, $V_{DS} = 0.3$ V, and the optimal $V_{BG\text{-}S}$ for each device.

Chapter 8

Summary and outlook

In this thesis, an in-depth study of in-plane heterojunctions of transition metal dichalcogenides and their potential for use in nanoelectronics (namely TFETs) was performed, and innovative device architectures taking advantage of the 2D nature of the considered materials were proposed.
Full quantum simulations showed that in the ballistic limit, the resulting devices yield high ON/OFF ratios ($> 10^8$) and extremely low sub-threshold swings (< 5 mV/dec) at low supply voltages ($V_{DD} = 0.3$ V).

In Chapter 1 a quick outline of the history of the transistor was given, before an introduction on MOSFETs outlining its working principle as well as the limits of the scaling of traditional, silicon-based MOSFETs was presented. Indeed, due to their instrinsic working mechanism (thermionic injection over a potential barrier), the power supply cannot be reduced without deteriorating device performance; nonetheless, the resulting heat dissipated by the billions of transistors found in microprocessors today prevents further miniaturization and severely hampers the future prospects of Si-MOSFET technology, which has ruled over the market for over four decades. A detailed introduction on TFETs was then given: thanks to their reliance on band-to-band tunneling and the resulting low sub-threshold swings, these devices are identified by the ITRS as amongst the best candidates to solve the supply voltage scaling issue.
In Chapter 2, the other main facet of this thesis work was brought to light: ever since 2004 and the experimental isolation of graphene by Geim and Novoselov, scientific interest in graphene and other so-called 2D materials has soared. Motivated by the unheard-of electronic and mechanical properties of graphene, dozens of other one-atom (or few-atom) thick materials were discovered and studied, in the hopes of bringing about a 2D revolution that could extend to all aspects of technology. General information as well as a rundown of their electronic properties were given for the most prominent 2D materials, ranging from graphene to hBN, transition metal dichalcogenide monolayers (TMDs) or silicene, just to name a few. Potential applications spaces for these materials (in electronics, photonics, sensing ...) as well as the current state of 2D material synthesis were quickly presented, to provide a full picture of the research field.

In Chapter 3, the physical models used in this work were detailed, along with information about the computational techniques used to investigate electronic transport in TFETs. First, the tight-binding approach was broadly presented, before the TB model used to describe the properties of the considered TMDs, along with the changes made upon it so that it would fit our needs, were detailed. A short overview of non-equlibrium Green's function theory, its use in nanoelectronics and, more specifically, quantum transport simulation was then given. Finally, a detailed explanation of the implementation of these two approaches in the code used to model ballistic quantum transport in field-effect transistors was presented.

Finally, simulation results were highlighted and analyzed in Chapters 4 through 7.
In Chapter 4, a brief study of the potential (or rather lack thereof) of TMDs for use in MOSFET technology was performed, highlighting their high SS and low ON current. TFETs based on in-plane heterojunctions of strained TMDs were studied in Chapter 5, and the paramount importance of band alignment in these devices was shown. Out of all the studied heterojunctions, the two bearing a "broken-gap" configuration ($MoTe_2/MoS_2$ and WTe_2/MoS_2) were shown to yield vastly superior performance (lower SS and higher I_{ON}) than the others. An in-depth study of these devices was then performed to identify the influence of design parameters such as contact length, channel length, as well as the voltages applied to the source and drain backgates (used instead of the traditional chemical doping, thanks to the 2D nature of the materials used). Namely, channel lengths beyond 20 nm were identified as a requirement to obtain peak performance from these devices. By optimizing the aforementioned parameters, these TFETs were shown to yield ballistic SS as low as 3 mV/dec and ballistic I_{ON} in excess of 10^3 µA/µm at a low supply voltage $V_{DD} = 0.3$ V.
Chapter 6 introduced DBE-TFETs: a device architecture derived from the classic TFET design studied in the previous chapter, based on observations made when studying the influence of the drain backgate voltage. By applying the same voltage to the drain backgate and the top-gate, the efficiency of the device was strongly improved, and all limits to channel scaling were removed: peak performance was shown to be achieved in devices with channels as short as 1.675 nm. A study of the impact of design parameters was also performed, as to identify prime conditions to operate the DBE-TFETs.
In Chapter 7 another innovative device design was introduced, the UC-TFET. In this device, the top-gate was completely removed, and the drain backgate (which determines the potential in the drain) was used to control current flow in the device. Foregoing the top-gate would be a strong advantage from a technological standpoint, as the manufacturing process could be streamlined and simplified. The influence of design parameters on the performance of the UC devices was analyzed, and similarly outstanding ballistic performance was reported ($SS < 5$ mV/dec and $I_{ON} > 10^3$ µA/µm), especially in the case of short channels (< 7 nm).

Some work remains, however: in these devices, strain is applied to the entirety of the material, including the contacts. A more accurate approach would be to model the gradual relaxation of the strain as the distance from the interface increases, and to consider pristine contacts.

From a simulation and computation standpoint, this is hardly feasible: considering a strain relaxation pattern similar to that observed in experimental works (see Section 3.3.3) would entail several key points:

- Dramatically increase the device length: as shown in Figure 50, a relatively small strain of 1.2% requires several hundreds of nanometers for the material to recover its pristine condition. The strong 5% strains applied in our case would therefore require device lengths well in the µm range to allow for the recovery of pristine behavior in the left and right semi-infinite contacts (as categorized in the NEGF method). The models and methods used in this work are in no way meant to be used to simulate such a high number of atoms, and the computational cost would therefore skyrocket.
- Consider a near-infinite amount of Hamiltonians to describe the TMDs: if such a strain relaxation pattern is to be adopted, the layer Hamiltonians and coupling Hamiltonians between successive layers would depend on their distance to the interface. For the sake of argument, let us assume a device length of 2 µm (one micron from each side of the interface, which is very conservative considering the data shown in Figure 50): in which the average distance between consecutive layers is 3.36 Å: a total number of $2000/0.336 \sim 6000$ unique layer Hamiltonians (and as many coupling Hamiltonians) would be necessary to model the system. Once again, this is simply not feasible from a computational standpoint.

While not totally accurate, the uniform strain patterns considered in this work allowed me to study these in-plane TMD heterojunctions and highlight their potential for TFET operation.

Similarly, the electron-phonon interaction was not taken into account in this work, and the ballistic results obtained therefore represent the best case scenario for each device. Both figures of merit (SS and I_{ON}) are expected to be negatively impacted by phonon scattering mechanisms to various degrees, as shown in [109], [466], [467].
SS is expected to be increased no matter the channel length, due to phonon absorption mechanisms active in the source region in the OFF-state regime and promoting inelastic tunneling of carriers from the valence to the conduction band.
Considering the mean-free-paths reported for MoS_2 [461], I_{ON} would mainly be impacted in the devices bearing channel lengths beyond 20 nm, and a compromise would therefore be necessary to maximize the performance of the standard TFETs.

In the case of both the DBE and UC-TFETS however, I_{ON} is at its peak when the channel is kept extremely short; as a result, peak ON current is not expected to be meaningfully impacted by phonon scattering.

As a final highlight of the promising potential of in-plane TMD heterojunctions for use in ultra-low power operation TFETs, the highest performances observed for all devices (at $V_{DS} = V_{DD} = 0.3$ V and with channel lengths ranging from 5 nm to 27 nm) are shown in Table 3.

		L_{ch} (nm)	SS (mV/dec)	I_{ON} (µA/µm)	ON/OFF	Impact of L_{ch} increase
$MoTe_2$-MoS_2	standard	5.025	73	0.153	1.53×10^4	↗
		13.4	10	923	9.23×10^7	
		26.8	5	970	9.7×10^7	
	DBE	5.025	3	1119	1.119×10^8	→
		13.4	2	1115	1.115×10^8	
		26.8	4	1105	1.105×10^8	
	UC	5.025	3	907	9.07×10^7	↘
		13.4	3	693	6.93×10^7	
		26.8	2	397	3.97×10^7	
WTe_2-MoS_2	standard	5.025	60	97	9.7×10^6	↗
		13.4	25	1344	1.344×10^8	
		26.8	4	1918	1.918×10^8	
	DBE	5.025	4	2550	2.550×10^8	→
		13.4	3	2512	2.512×10^8	
		26.8	3	2531	2.532×10^8	
	UC	5.025	3	2516	2.516×10^8	↘
		13.4	2	1239	1.239×10^8	
		26.8	2	586	5.86×10^7	

Table 3. Highest performance (SS, I_{ON} and ON/OFF) observed for all TFETs studied in this thesis, at $V_{DS} = V_{DD} = 0.3$ V and channel lengths ranging from 5 nm to 27 nm.

Appendix A – TB parameters

	$\mathbf{MoS_2}$				$\mathbf{MoSe_2}$				$\mathbf{WS_2}$			
	$H^{(0)}_{AA}$	$H^{(0)}_{BB}$	$H^{(0)}_{CC}$	$H^{(0)}_{DD}$	$H^{(0)}_{AA}$	$H^{(0)}_{BB}$	$H^{(0)}_{CC}$	$H^{(0)}_{DD}$	$H^{(0)}_{AA}$	$H^{(0)}_{BB}$	$H^{(0)}_{CC}$	$H^{(0)}_{DD}$
ϵ_0	-----	-6.720	-6.082	-8.839	-----	-5.986	-5.559	-8.231	-----	-6.838	-5.734	-9.078
ϵ_1	-4.873	-7.235	-5.856	-7.850	-4.547	-6.502	-5.314	-7.110	-4.327	-7.250	-5.498	-8.033
$\alpha^{(0)}_0$	-----	1.623	-1.021	-0.858	-----	1.396	-1.090	-0.742	-----	1.743	-1.212	0.158
$\alpha^{(0)}_1$	-2.498	-1.500	-1.817	-3.317	-2.498	-1.440	-2.023	-3.316	-2.631	-1.854	-1.916	-4.290
$\beta^{(0)}_0$	-0.890	-0.094	-0.370	-1.142	-0.890	-0.121	-0.296	-1.146	-0.986	0.089	-0.292	-1.390
$\beta^{(0)}_1$	-----	0.273	-0.043	0.720	-----	0.270	0.004	0.829	-----	0.487	0.036	1.586

	$\mathbf{WSe_2}$				$\mathbf{MoTe_2}$				$\mathbf{WTe_2}$			
	$H^{(0)}_{AA}$	$H^{(0)}_{BB}$	$H^{(0)}_{CC}$	$H^{(0)}_{DD}$	$H^{(0)}_{AA}$	$H^{(0)}_{BB}$	$H^{(0)}_{CC}$	$H^{(0)}_{DD}$	$H^{(0)}_{AA}$	$H^{(0)}_{BB}$	$H^{(0)}_{CC}$	$H^{(0)}_{DD}$
ϵ_0	-----	-6.066	-5.267	-8.466	-----	-5.264	-5.250	-7.601	-----	-5.305	-5.052	-7.786
ϵ_1	-4.069	-6.494	-5.001	-7.277	-4.339	-5.807	-4.945	-6.390	-3.969	-5.789	-4.716	-6.566
$\alpha^{(0)}_0$	-----	1.385	-1.012	-0.050	-----	-1.685	-0.835	-0.182	-----	1.695	-0.819	0.696
$\alpha^{(0)}_1$	-2.357	-1.724	-1.967	-4.138	-1.820	-1.235	-2.061	-3.463	-1.795	-1.536	-2.022	-4.519
$\beta^{(0)}_0$	-0.902	0.059	-0.220	-1.337	-0.829	-0.250	-0.232	-1.267	-0.935	-0.078	-0.126	-1.482
$\beta^{(0)}_1$	-----	0.482	-0.022	1.507	-----	0.333	0.063	0.954	-----	0.556	0.043	1.576

Table 4. TB parameters necessary to build the $H^{(0)}_{JJ}$ Hamiltonians for all six TMDs

	$\mathbf{MoS_2}$			$\mathbf{MoSe_2}$			$\mathbf{WS_2}$		
	$H_{BA}^{(1)}$	$H_{DC}^{(1)}$	$H_{DC}^{(3)}$	$H_{BA}^{(1)}$	$H_{DC}^{(1)}$	$H_{DC}^{(3)}$	$H_{BA}^{(1)}$	$H_{DC}^{(1)}$	$H_{DC}^{(3)}$
$t_0^{(n)}$	-0.789	1.411	0.014	-0.695	1.268	0.017	-0.884	1.558	0.010
$t_1^{(n)}$	2.158	0.652	-0.245	1.941	0.554	-0.215	2.302	0.664	-0.273
$t_2^{(n)}$	-----	-0.940	-0.150	-----	-0.874	-0.155	-----	-0.993	-0.154
$t_3^{(n)}$	-1.379	-0.954	-0.221	-1.326	-0.858	-0.223	-1.436	-0.943	-0.265
$t_4^{(n)}$	-----	-0.883	-0.069	-----	-0.772	-0.069	-----	-1.005	-0.066
$\alpha_0^{(n)}$	0.545	-0.486	0.173	0.408	-0.407	0.175	0.585	-0.609	0.537
$\alpha_1^{(n)}$	-0.605	0.843	0.204	-0.417	0.825	0.185	-0.482	1.045	0.185
$\alpha_2^{(n)}$	-----	2.178	0.567	-----	1.928	0.554	-----	2.827	0.623
$\alpha_3^{(n)}$	1.845	0.446	0.744	1.718	0.272	0.760	1.826	0.071	1.055
$\alpha_4^{(n)}$	-----	-0.208	0.035	-----	-0.298	0.062	-----	-0.241	-0.090
$\beta_0^{(n)}$	-1.076	1.724	-0.178	-0.897	1.530	-0.164	-1.128	2.402	-0.345
$\beta_1^{(n)}$	0.401	-0.353	-1.069	0.264	-0.367	-0.995	0.140	-0.900	-1.110
$\beta_2^{(n)}$	-----	-2.204	-0.070	-----	-1.995	-0.093	-----	-2.293	-0.125
$\beta_3^{(n)}$	-2.100	-0.682	-0.267	-1.874	-0.510	-0.292	-1.990	-0.306	-0.120
$\beta_4^{(n)}$	-----	-0.850	-0.281	-----	-0.727	-0.290	-----	-1.184	-0.536
$\beta_5^{(n)}$	0.859	0.899	-0.690	0.770	0.761	-0.664	0.915	0.902	-1.093
$\beta_6^{(n)}$	-----	-0.542	-0.382	-----	-0.475	-0.391	-----	-0.193	-0.644
$\beta_7^{(n)}$	-0.377	-2.093	-0.340	-0.469	-1.841	-0.299	-0.634	-2.934	-0.535
$\beta_8^{(n)}$	-0.836	1.101	0.015	-0.717	1.005	0.007	-0.944	1.427	-0.127

Table 5. TB parameters necessary to build the $H_{IJ}^{(n)}$ Hamiltonians for MoS_2, $MoSe_2$ and WS_2

	$\mathbf{WSe_2}$			$\mathbf{MoTe_2}$			$\mathbf{WTe_2}$		
	$H^{(1)}_{BA}$	$H^{(1)}_{DC}$	$H^{(3)}_{DC}$	$H^{(1)}_{BA}$	$H^{(1)}_{DC}$	$H^{(3)}_{DC}$	$H^{(1)}_{BA}$	$H^{(1)}_{DC}$	$H^{(3)}_{DC}$
$t_0^{(n)}$	-0.773	1.399	0.017	-0.557	1.117	0.038	-0.617	1.221	0.053
$t_1^{(n)}$	2.079	0.567	-0.242	1.690	0.461	-0.194	1.813	0.480	-0.218
$t_2^{(n)}$	-----	-0.905	-0.161	-----	-0.798	-0.144	-----	-0.798	-0.142
$t_3^{(n)}$	-1.401	-0.853	-0.263	-1.197	-0.678	-0.204	-1.263	-0.673	-0.225
$t_4^{(n)}$	-----	-0.896	-0.068	-----	-0.652	-0.050	-----	-0.772	-0.045
$\alpha_0^{(n)}$	0.406	-0.493	0.468	0.260	-0.364	0.217	0.286	-0.545	0.629
$\alpha_1^{(n)}$	-0.322	0.917	0.202	-0.275	0.813	0.199	-0.202	0.903	0.276
$\alpha_2^{(n)}$	-----	2.409	0.653	-----	1.850	0.545	-----	2.643	0.654
$\alpha_3^{(n)}$	1.764	0.022	1.050	1.309	-0.017	0.791	1.309	-0.393	1.123
$\alpha_4^{(n)}$	-----	-0.238	-0.021	-----	-0.438	0.021	-----	-0.456	-0.107
$\beta_0^{(n)}$	-0.929	1.973	-0.321	-0.644	1.435	-0.125	-0.665	1.828	-0.278
$\beta_1^{(n)}$	-0.029	-0.877	-1.094	0.106	-0.372	-0.985	-0.121	-0.818	-1.079
$\beta_2^{(n)}$	-----	-2.153	-0.114	-----	-1.711	-0.113	-----	-1.812	-0.180
$\beta_3^{(n)}$	-1.879	-0.276	-0.241	-1.534	-0.337	-0.219	-1.4841	-0.048	-0.160
$\beta_4^{(n)}$	-----	-0.897	-0.476	-----	-0.668	-0.297	-----	-0.824	-0.544
$\beta_5^{(n)}$	0.798	0.761	-1.022	0.482	0.633	-0.663	0.461	0.593	-0.997
$\beta_6^{(n)}$	-----	-0.300	-0.651	-----	-0.403	-0.425	-----	-0.150	-0.726
$\beta_7^{(n)}$	-0.690	-2.447	-0.423	-0.728	-1.753	-0.330	-1.001	-2.304	-0.430
$\beta_8^{(n)}$	-0.793	1.082	-0.058	-0.588	-0.877	0.018	-0.577	0.941	0.012

Table 6. TB parameters necessary to build the $H_{IJ}^{(n)}$ Hamiltonians for WSe_2, $MoTe_2$ and WTe_2

	$\mathbf{MoS_2}$				$\mathbf{MoSe_2}$				$\mathbf{WS_2}$			
	$H^{(2)}_{AA}$	$H^{(2)}_{BB}$	$H^{(2)}_{CC}$	$H^{(2)}_{DD}$	$H^{(2)}_{AA}$	$H^{(2)}_{BB}$	$H^{(2)}_{CC}$	$H^{(2)}_{DD}$	$H^{(2)}_{AA}$	$H^{(2)}_{BB}$	$H^{(2)}_{CC}$	$H^{(2)}_{DD}$
$t^{(2)}_0$	-0.206	0.865	0.275	0.912	-0.146	0.964	0.251	0.991	-0.198	0.873	0.355	0.965
$t^{(2)}_1$	0.031	-0.187	-0.558	0.006	0.017	-0.172	-0.473	-0.004	0.027	-0.218	-0.691	0.014
$t^{(2)}_2$	----	-0.174	-0.298	-0.192	----	-0.211	-0.264	-0.217	----	-0.175	-0.371	-0.212
$t^{(2)}_3$	-0.257	-0.070	-0.249	-0.038	-0.810	-0.068	-0.201	-0.039	-0.310	-0.099	-0.304	-0.101
$t^{(2)}_4$	----	0.100	0.114	-0.106	----	0.076	0.096	-0.121	----	0.110	0.145	-0.163
$t^{(2)}_5$	----	-0.068	0.410	0.008	----	-0.074	0.352	0.005	----	-0.082	0.488	-0.031
$\alpha^{(2)}_0$	-0.258	-1.841	-1.027	-1.425	-0.309	-1.979	-0.951	-1.586	-0.453	-1.844	-1.232	-1.122
$\alpha^{(2)}_1$	-0.202	-0.027	1.544	-0.057	-0.125	-0.103	1.333	-0.072	-0.213	-0.067	1.947	-0.162
$\alpha^{(2)}_2$	----	0.444	1.032	0.644	----	0.536	0.885	0.668	----	0.434	1.123	0.674
$\alpha^{(2)}_3$	0.705	-0.045	0.206	-0.170	0.514	-0.059	0.195	-0.162	0.834	-0.042	0.462	-0.314
$\alpha^{(2)}_4$	----	-0.210	0.285	-0.199	----	-0.123	0.236	-0.202	----	-0.208	0.365	-0.333
$\alpha^{(2)}_5$	----	0.141	-0.738	0.065	----	0.142	-0.596	0.050	----	0.177	-0.654	0.105
$\beta^{(2)}_0$	-0.676	-2.203	-0.910	-2.013	-0.588	-2.378	-0.793	-2.180	-0.942	-2.254	-1.068	-1.920
$\beta^{(2)}_1$	-0.192	0.768	1.337	0.828	-0.118	0.827	1.108	0.884	-0.175	0.772	1.240	1.039
$\beta^{(2)}_2$	----	0.350	0.376	0.540	----	0.445	0.333	0.576	----	0.283	0.522	-0.580
$\beta^{(2)}_3$	0.555	-0.065	-0.003	0.143	0.416	-0.016	0.008	0.155	0.649	-0.054	-0.083	0.345
$\beta^{(2)}_4$	----	-0.208	0.188	-0.056	----	-0.146	0.126	-0.026	----	-0.198	0.179	0.062
$\beta^{(2)}_5$	----	0.096	-0.779	0.082	----	0.112	-0.667	0.073	----	0.127	-0.863	0.130
$\beta^{(2)}_6$	-0.095	0.482	-0.634	0.744	-0.063	0.567	-0.565	0.777	-0.076	0.467	-0.960	0.858
$\beta^{(2)}_7$	----	-0.146	0.288	0.051	----	-0.128	0.255	0.066	----	-0.128	0.484	0.146
$\beta^{(2)}_8$	----	-0.089	-0.152	-0.099	----	-0.092	-0.110	-0.127	----	-0.117	-0.046	-0.236

Table 7. TB parameters necessary to build the $H^{(2)}_{JJ}$ Hamiltonians for MoS_2, $MoSe_2$ and WS_2

	$\mathbf{WSe_2}$				$\mathbf{MoTe_2}$				$\mathbf{WTe_2}$			
	$H^{(2)}_{AA}$	$H^{(2)}_{BB}$	$H^{(2)}_{CC}$	$H^{(2)}_{DD}$	$H^{(2)}_{AA}$	$H^{(2)}_{BB}$	$H^{(2)}_{CC}$	$H^{(2)}_{DD}$	$H^{(2)}_{AA}$	$H^{(2)}_{BB}$	$H^{(2)}_{CC}$	$H^{(2)}_{DD}$
$t^{(2)}_0$	-0.137	0.977	0.320	1.047	-0.156	-1.071	0.205	1.063	-0.158	1.079	0.255	1.112
$t^{(2)}_1$	0.013	-0.198	-0.584	0.003	0.018	-0.111	-0.372	0.038	0.015	-0.130	-0.447	0.049
$t^{(2)}_2$	----	-0.217	-0.333	-0.241	----	-0.251	-0.214	-0.232	----	-0.258	-0.270	-0.252
$t^{(2)}_3$	-0.232	-0.092	-0.245	-0.102	-0.167	-0.056	-0.163	-0.044	-0.198	-0.073	-0.189	-0.111
$t^{(2)}_4$	----	0.079	0.124	-0.185	----	-0.045	0.071	-0.092	----	-0.045	0.094	-0.155
$t^{(2)}_5$	----	-0.091	0.423	-0.038	----	-0.077	0.283	-0.007	----	-0.095	0.339	-0.056
$\alpha^{(2)}_0$	-0.490	-1.986	-1.127	-1.357	-0.262	-2.085	-0.797	-1.680	-0.414	-2.068	-0.897	-1.367
$\alpha^{(2)}_1$	-0.117	-0.152	1.617	-0.159	-0.056	-0.320	1.102	-0.251	-0.034	-0.372	1.353	-0.387
$\alpha^{(2)}_2$	----	0.557	1.013	0.718	----	0.608	0.650	0.709	----	0.621	0.665	0.777
$\alpha^{(2)}_3$	0.589	-0.074	0.325	-0.303	0.405	-0.069	0.204	-0.195	0.458	-0.086	0.327	-0.399
$\alpha^{(2)}_4$	----	-0.105	0.291	-0.287	----	-0.068	0.216	-0.278	----	-0.049	0.264	-0.392
$\alpha^{(2)}_5$	----	0.188	-0.564	0.112	----	0.148	-0.402	0.067	----	0.202	-0.340	0.157
$\beta^{(2)}_0$	-0.809	-2.427	-0.966	-2.086	-0.403	-2.633	-0.606	-2.405	-0.556	-2.658	-0.757	-2.281
$\beta^{(2)}_1$	-0.090	0.834	1.179	1.069	-0.069	0.976	0.870	1.037	-0.005	0.983	0.879	1.244
$\beta^{(2)}_2$	----	0.401	0.406	0.556	----	0.564	0.243	0.609	----	0.540	0.364	0.548
$\beta^{(2)}_3$	0.480	0.015	-0.044	0.331	0.278	0.013	-0.015	0.176	-0.319	0.034	-0.064	0.351
$\beta^{(2)}_4$	----	-0.104	0.129	0.063	----	-0.027	0.129	-0.099	----	0.035	0.089	-0.043
$\beta^{(2)}_5$	----	0.152	-0.727	0.112	----	0.118	-0.524	0.077	----	0.161	-0.614	0.117
$\beta^{(2)}_6$	-0.037	0.550	-0.776	0.873	-0.036	0.677	-0.436	0.850	-0.013	0.670	-0.607	0.928
$\beta^{(2)}_7$	----	-0.157	0.308	0.109	----	-0.112	0.174	0.108	----	-0.119	0.266	0.184
$\beta^{(2)}_8$	----	-0.129	-0.099	-0.224	----	-0.101	-0.071	-0.141	----	-0.131	-0.015	-0.251

Table 8. TB parameters necessary to build the $H^{(2)}_{JJ}$ Hamiltonians for WSe_2, $MoTe_2$ and WTe_2

Appendix B – Band folding

In this Appendix, the band folding resulting in the doubling of the unit cell along the k_x direction will be highlighted for all six TMDs. The bandstructures of all six TMDs at $k_y = 0$ and k_x ranging from $\frac{-2\pi}{a}$ to $\frac{2\pi}{a}$ are shown in Figure 121 and Figure 122.

The bands resulting from the base unit cell and the corresponding 11×11 Hamiltonians are shown as red circles, while the bands obtained in the expanded unit cell and the corresponding 22×22 Hamiltonians are shown as blue lines.

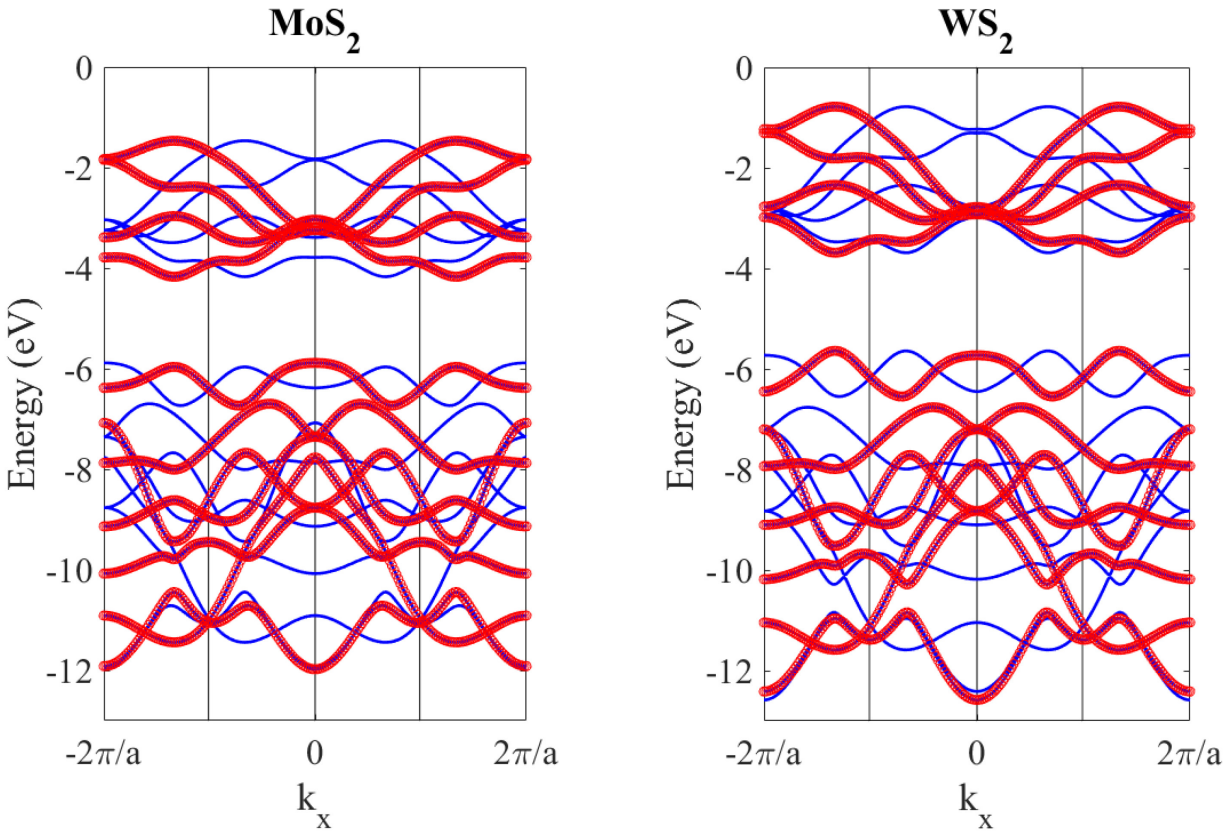


Figure 121. Bandstructure of MoS_2 and WS_2 at $k_y = 0$ and k_x ranging from $\frac{-2\pi}{a}$ to $\frac{2\pi}{a}$ as obtained with the original 11×11 Hamiltonians (red circles) and the 22×22 Hamiltonians resulting from the expanded unit cell (blue lines), highlighting the band folding induced by the basis modification.

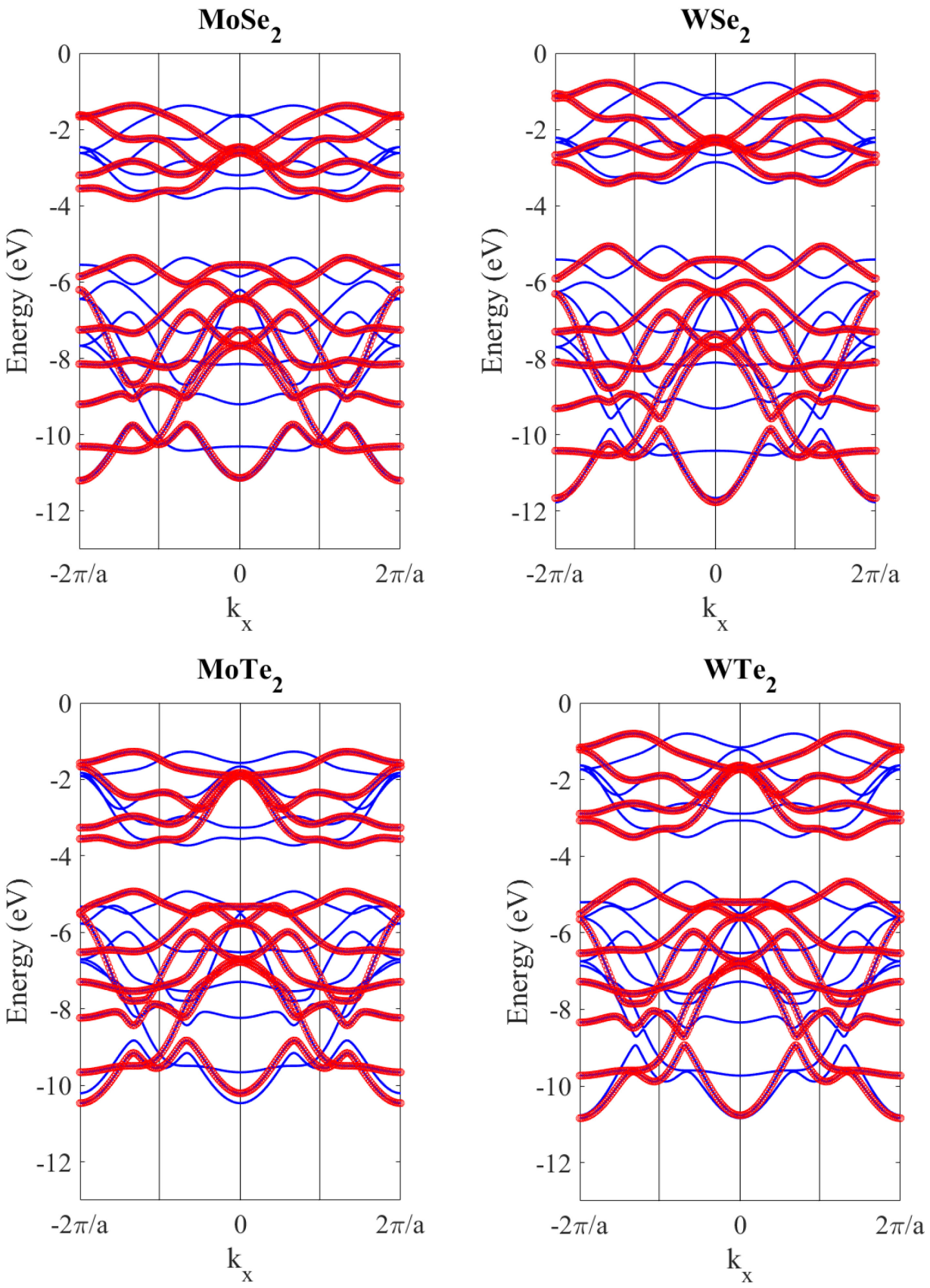


Figure 122. Bandstructure of $MoSe_2$, WSe_2, $MoSe_2$ and WTe_2 at $k_y = 0$ and k_x ranging from $\frac{-2\pi}{a}$ to $\frac{2\pi}{a}$ as obtained with the original 11×11 Hamiltonians (red circles) and the 22×22 Hamiltonians resulting from the expanded unit cell (blue lines), highlighting the band folding induced by the basis modification.

References

[1]S. Fang, S. Carr, J. Shen, M. A. Cazalilla, and E. Kaxiras, "Electronic Structure Theory of Strained Two-Dimensional Materials with hexagonal symmetry," *Phys. Rev. B*, vol. 98, no. 7, p. 075106, 2018.

[2]"The Transistor in a Century of Electronics," *Nobelprize.org*. [Online]. Available: https://www.nobelprize.org/educational/physics/transistor/history/.

[3]"The History of the Transistor," *sjsu.edu*. [Online]. Available: http://www.sjsu.edu/faculty/watkins/transist.htm.

[4]C. de Looper, "A history of the transistor," *PCmech.com*. [Online]. Available: https://www.pcmech.com/article/history-of-transistor/.

[5]M. Riordan, "The lost history of the transistor," *Spectrum.IEEE.org*. [Online]. Available: https://spectrum.ieee.org/tech-history/silicon-revolution/the-lost-history-of-the-transistor#.

[6]"History of transistors," *Rohm.com*. [Online]. Available: https://www.rohm.com/electronics-basics/transistors/history-of-transistors.

[7]"1954: Silicon Transistors Offer Superior Operating Characteristics," *ComputerHistory.org*. [Online]. Available: http://www.computerhistory.org/siliconengine/silicon-transistors-offer-superior-operating-characteristics/.

[8]"1960: Metal Oxide Semiconductor (MOS) Transistor Demonstrated," *ComputerHistory.org*. [Online]. Available: http://www.computerhistory.org/siliconengine/metal-oxide-semiconductor-mos-transistor-demonstrated/.

[9]"1926: Field Effect Semiconductor Device Concepts Patented," *ComputerHistory.org*. [Online]. Available: http://www.computerhistory.org/siliconengine/field-effect-semiconductor-device-concepts-patented/.

[10]K. Rupp *et al.*, "40 Years of Microprocessor Trend Data," *KarlRupp.net*, 2011. [Online]. Available: https://www.karlrupp.net/2015/06/40-years-of-microprocessor-trend-data/.

[11]G. E. Moore, "Cramming More Components Onto Integrated Circuits," *Electronics*, vol. 38, no. 8, Apr. 1965.

[12]"1971: Microprocessor Integrates CPU Function onto a Single Chip," *ComputerHistory.org*. [Online]. Available: http://www.computerhistory.org/siliconengine/microprocessor-integrates-cpu-function-onto-a-single-chip/.

[13]..... Intel Corp., *Transistor and microprocessor timeline*. .

[14]"AMD's Epyc Products," *AMD.com*, 2018. [Online]. Available: https://www.amd.com/en/products/epyc.

[15]E. P. Vandamme, P. Jansen, and L. Deferm, "Modeling the subthreshold swing in MOSFET's," *IEEE Electron Device Lett.*, vol. 18, no. 8, pp. 369–371, Aug. 1997.

[16]International Technology Roadmap for Semiconductors, "2015 ITRS Executive Report," 2015.

[17]A. Lidow, T. Herman, and H. W. Collins, "Power MOSFET technology," in *1979 International Electron Devices Meeting*, 1979, pp. 79–83.

[18]R.-H. Yan, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: From Bulk to SO1 to Bulk," p. 7.

[19]Yuan Taur, "An analytical solution to a double-gate MOSFET with undoped body," *IEEE Electron Device Lett.*, vol. 21, no. 5, pp. 245–247, May 2000.

[20]C. Fiegna, H. Iwai, M. Saito, E. Sangiorgi, and B. Riccb, "Scaling the MOS Transistor Below 0.1 pm: Methodology, Device Structures, and Technology Requirements," *IEEE Trans. ELECTRON DEVICES*, vol. 41, no. 6, p. 11, 1994.

[21]I. K. Budihardjo, P. O. Lauritzen, and H. A. Mantooth, "Performance requirements for power MOSFET models," *IEEE Trans. Power Electron.*, vol. 12, no. 1, pp. 36–45, Jan. 1997.

[22].....M. V. Fischetti, "History of the MOSFET," p. 55, 2009.

[23].....J.-P. Colinge, "The evolution of silicon-on-insulator MOSFETs," 2003, pp. 354–355.

[24]J.-P. Colinge, "On the Evolution of SOI Materials and Devices," in *Science and Technology of Semiconductor-On-Insulator Structures and Devices Operating in a Harsh Environment*, vol. 185, D. Flandre, A. N. Nazarov, and P. L. F. Hemment, Eds. Berlin/Heidelberg: Springer-Verlag, 2005, pp. 11–26.

[25]..... N. Murty Kodeti, "Silicon On Insulator (SOI) Implementation," 2010.

[26]D. Hisamoto *et al.*, "A folded-channel MOSFET for deep-sub-tenth micron era," 1998, pp. 1032–1034.

[27]L. GEPPERT, "Radical changes are in the offing for transistors as their dimensions shrink to a few tens of nanometers," *IEEE Spectr.*, p. 6, 2002.

[28]J.-P. Colinge, "Multiple-gate SOI MOSFETs," *Solid-State Electron.*, vol. 48, no. 6, pp. 897–905, Jun. 2004.

[29]A. Tsormpatzoglou, C. A. Dimitriadis, R. Clerc, Q. Rafhay, G. Pananakakis, and G. Ghibaudo, "Semi-Analytical Modeling of Short-Channel Effects in Si and Ge Symmetrical Double-Gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 8, pp. 1943–1952, Aug. 2007.

[30]A. Tsormpatzoglou, C. A. Dimitriadis, R. Clerc, G. Pananakakis, and G. Ghibaudo, "Semianalytical Modeling of Short-Channel Effects in Lightly Doped Silicon Trigate MOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 10, pp. 2623–2631, Oct. 2008.

[31]T.-J. King Liu, "FinFET: history, fundamentals and future," presented at the 2012 Symposium on VLSI Technology Short Course, 2012.

[32]G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-$\varkappa$ gate dielectrics: Current status and materials properties considerations," *J. Appl. Phys.*, vol. 89, no. 10, pp. 5243–5275, May 2001.

[33]J. Robertson and R. M. Wallace, "High-K materials and metal gates for CMOS applications," *Mater. Sci. Eng. R Rep.*, vol. 88, pp. 1–41, Feb. 2015.

[34]S. Mohsenifar and M. . Sharkhokhabadi, "High-$\varkappa$ Metal Gate (HKMG), MOSFET, High-$\varkappa$ oxides, Scaling down, Moore's Law, Silica, CMOS," *Microelectron. Solid State Electron.*, p. 13, 2015.

[35]"The high-k solution," *Spectrum.IEEE.org*, 2007. [Online]. Available: https://spectrum.ieee.org/semiconductors/design/the-highk-solution.

[36]..... J. L. Hoyt *et al.*, "Strained silicon MOSFET technology," 2002, pp. 23–26.

[37]S. E. Thompson *et al.*, "A Logic Nanotechnology Featuring Strained-Silicon," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 191–193, Apr. 2004.

[38]S. E. Thompson *et al.*, "A 90-nm Logic Technology Featuring Strained-Silicon," *IEEE Trans. Electron Devices*, vol. 51, no. 11, pp. 1790–1797, Nov. 2004.

[39]V. Venkataraman, S. Nawal, and M. J. Kumar, "Compact Analytical Threshold-Voltage Model of Nanoscale Fully Depleted Strained-Si on Silicon–Germanium-on-Insu lator (SGOI) MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 3, pp. 554–562, Mar. 2007.

[40]V. P. Kesan *et al.*, "High performance 0.25 mu m p-MOSFETs with silicon-germanium channels for 300 K and 77 K operation," 1991, pp. 25–28.

[41]S. Thiele, W. Kinberger, R. Granzner, G. Fiori, and F. Schwierz, "The prospects of two-dimensional materials for ultimately scaled CMOS," 2017, pp. 113–116.

[42]F. Adamu-Lema, Be. Electronics, A. Asenov, and D. S. Roy, "Scaling and Intrinsic Parameter Fluctuations in nano- CMOS Devices," p. 218.

[43]H. Iwai, "Roadmap for 22nm and beyond (Invited Paper)," *Microelectron. Eng.*, vol. 86, no. 7–9, pp. 1520–1528, Jul. 2009.

[44]Nam Sung Kim *et al.*, "Leakage current: Moore's law meets static power," *Computer*, vol. 36, no. 12, pp. 68–75, Dec. 2003.

[45]P. M. Zeitzoff and H. R. Huff, "MOSFET Scaling Trends, Challenges, and Potential Solutions Through the End of the Roadmap: A 2005 Perspective," p. 94.

[46]D. Esseni, M. Pala, P. Palestri, C. Alper, and T. Rollo, "A review of selected topics in physics based modeling for tunnel field-effect transistors," *Semicond. Sci. Technol.*, vol. 32, no. 8, p. 083005, Aug. 2017.

[47]B. Doyle *et al.*, "Transistor Elements for 30nm Physical Gate Lengths and Beyond," vol. 6, no. 2, p. 15.

[48]S. Takagi *et al.*, "High Performance III-V-on-Insulator MOSFETs on Si Realized by Direct Wafer Bonding Applicable to Large Wafer Size," *ECS Trans.*, vol. 66, no. 5, pp. 27–35, May 2015.

[49]S. C. Lee, A. Neumann, Y.-B. Jiang, K. Artyushkova, and S. R. J. Brueck, "Top-down, in-plane GaAs nanowire MOSFETs on an Al_2O_3 buffer with a trigate oxide from focused ion-beam milling and chemical oxidation," *Nanotechnology*, vol. 27, no. 37, p. 375707, Sep. 2016.

[50]A. Kumar *et al.*, "Integration of InGaAs MOSFETs and GaAs/ AlGaAs lasers on Si Substrate for advanced opto-electronic integrated circuits (OEICs)," *Opt. Express*, vol. 25, no. 25, p. 31853, Dec. 2017.

[51]M. Yokoyama, H. Yokoyama, M. Takenaka, and S. Takagi, "III-V single structure CMOS by using ultrathin body InAs/GaSb-OI channels on Si," 2014, pp. 1–2.

[52]K. S. Novoselov, V. I. Fal'ko, L. Colombo, P. R. Gellert, M. G. Schwab, and K. Kim, "A roadmap for graphene," *Nature*, vol. 490, no. 7419, pp. 192–200, Oct. 2012.

[53]A. C. Ferrari *et al.*, "Science and technology roadmap for graphene, related two-dimensional crystals, and hybrid systems," *Nanoscale*, vol. 7, no. 11, pp. 4598–4810, 2015.

[54]R. S. Dahiya, G. Metta, M. Valle, A. Adami, and L. Lorenzelli, "Piezoelectric oxide semiconductor field effect transistor touch sensing devices," *Appl. Phys. Lett.*, vol. 95, no. 3, p. 034105, Jul. 2009.

[55]L. Zhang, J. Huang, and M. Chan, "Steep Slope Devices and TFETs," in *Tunneling Field Effect Transistor Technology*, L. Zhang and M. Chan, Eds. Cham: Springer International Publishing, 2016, pp. 1–31.

[56]D. Grogg, C. Meinen, D. Tsamados, H. C. Tekin, M. Kayal, and A. M. Ionescu, "Double gate movable body Micro-Electro-Mechanical FET as hysteretic switch: Application to data transmission systems," 2008, pp. 302–305.

[57]S. Salahuddin and S. Datta, "Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices," *Nano Lett.*, vol. 8, no. 2, pp. 405–410, Feb. 2008.

[58]K.-S. Li *et al.*, "Sub-60mV-swing negative-capacitance FinFET without hysteresis," in *2015 IEEE International Electron Devices Meeting (IEDM)*, Washington, DC, USA, 2015, pp. 22.6.1-22.6.4.

[59]A. Islam Khan *et al.*, "Experimental evidence of ferroelectric negative capacitance in nanoscale heterostructures," *Appl. Phys. Lett.*, vol. 99, no. 11, p. 113501, Sep. 2011.

[60]H. Lu and A. Seabaugh, "Tunnel Field-Effect Transistors: State-of-the-Art," *IEEE J. Electron Devices Soc.*, vol. 2, no. 4, pp. 44–49, Jul. 2014.

[61]A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, Nov. 2011.

[62]J. J. Quinn, G. Kawamoto, and B. D. McCombe, "Subband spectroscopy by surface channel tunneling," *Surf. Sci.*, vol. 73, pp. 190–196, May 1978.

[63]T. Baba, "Proposal for Surface Tunnel Transistors," *Jpn. J. Appl. Phys.*, vol. 31, no. Part 2, No. 4B, pp. L455–L457, Apr. 1992.

[64]Y. Omura, "Negative Conductance Properties in Extremely Thin Silicon-on-Insulator (SOI) Insulated-Gate pn-Junction Devices (SOI Surface Tunnel Transistors)," *Jpn. J. Appl. Phys.*, vol. 35, no. Part 2, No. 11A, pp. L1401–L1403, Nov. 1996.

[65]T. Uemura and T. Baba, "First demonstration of a planar-type surface tunnel transistor (STT): Lateral interband tunnel device," *Solid-State Electron.*, vol. 40, no. 1–8, pp. 519–522, Jan. 1996.

[66]T. Uemura and T. Baba, "Large enhancement of interband tunneling current densities of over 10/sup 5/ A/cm/sup 2/ in In/sub 0.53/Ga/sub 0.47/As-based surface tunnel transistors," *IEEE Electron Device Lett.*, vol. 18, no. 5, pp. 225–227, May 1997.

[67]J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors," *Phys. Rev. Lett.*, vol. 93, no. 19, Nov. 2004.

[68]P.-F. Wang *et al.*, "Complementary tunneling transistor for low power application," *Solid-State Electron.*, vol. 48, no. 12, pp. 2281–2286, Dec. 2004.

[69]Qin Zhang, Wei Zhao, and A. Seabaugh, "Analytic expression and approach for low subthreshold-swing tunnel transistors," 2005, vol. 1, pp. 161–162.

[70]K. K. Bhuwalka, J. Schulze, and I. Eisele, "Performance Enhancement of Vertical Tunnel Field-Effect Transistor with SiGe in the δp^+ Layer," *Jpn. J. Appl. Phys.*, vol. 43, no. 7A, pp. 4073–4078, Jul. 2004.

[71]F. Mayer *et al.*, "Impact of SOI, Si1-xGexOI and GeOI substrates on CMOS compatible Tunnel FET performance," 2008, pp. 1–5.

[72]K. Jeon *et al.*, "Si tunnel transistors with a novel silicided source and 46mV/dec swing," 2010, pp. 121–122.

[73]Woo Young Choi, Byung-Gook Park, Jong Duk Lee, and Tsu-Jae King Liu, "Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, Aug. 2007.

[74]T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, "Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With record high drive currents and <60mV/dec subthreshold slope," 2008, pp. 1–3.

[75]Y. Lu, S. Bangsaruntip, X. Wang, L. Zhang, Y. Nishi, and H. Dai, "DNA Functionalization of Carbon Nanotubes for Ultrathin Atomic Layer Deposition of High $\varkappa$ Dielectrics for Nanotube Transistors with 60 mV/Decade Switching," *J. Am. Chem. Soc.*, vol. 128, no. 11, pp. 3518–3519, Mar. 2006.

[76]K.-F. Lee *et al.*, "Characteristic Optimization of Single- and Double-Gate Tunneling Field Effect Transistors," vol. 2, p. 4, 2010.

[77]S. Poorvasha, School of Electronics Engineering, VIT University, Chennai â€“ 600127, Tamil Nadu, India, M. Pown, School of Electronics Engineering, VIT University, Chennai â€“ 600127, Tamil Nadu, India, B. Lakshmi, and School of Electronics Engineering, VIT University, Chennai â€“ 600127, Tamil Nadu, India, "Tunnel Field Effect Transistors for Digital and Analog Applications: A Review," *Indian J. Sci. Technol.*, vol. 10, no. 13, pp. 1–7, Apr. 2017.

[78]S. Saurabh and M. J. Kumar, "Impact of Strain on Drain Current and Threshold Voltage of Nanoscale Double Gate Tunnel Field Effect Transistor: Theoretical Investigation and Analysis," *Jpn. J. Appl. Phys.*, vol. 48, no. 6, p. 064503, Jun. 2009.

[79]J. Madan and R. Chaujar, "Gate Drain Underlapped-PNIN-GAA-TFET for Comprehensively Upgraded Analog/RF Performance," *Superlattices Microstruct.*, vol. 102, pp. 17–26, Feb. 2017.

[80]T. P. Amrutha, I. Flavia Princess Nesamani, and V. Laskhmi Prabha, "Design of Si/SiGe Heterojunction Line Tunnel Field Effect Transistor (TFET) with High-K Dielectric," *ARPN J. Eng. Appl. Sci.*, vol. 10, no. 4, pp. 1879–1882, 2015.

[81]R. Narang, M. Saxena, R. S. Gupta, and M. Gupta, "Asymmetric gate oxide Tunnel Field Effect Transistor for improved circuit performance," 2012, pp. 284–287.

[82]D. Leonelli *et al.*, "Performance Enhancement in Multi Gate Tunneling Field Effect Transistors by Scaling the Fin-Width," *Jpn. J. Appl. Phys.*, vol. 49, no. 4, p. 04DC10, Apr. 2010.

[83]R. Gandhi, Z. Chen, N. Singh, K. Banerjee, and S. Lee, "Vertical Si-Nanowire n-Type Tunneling FETs With Low Subthreshold Swing ($\leq \hbox{50}\ \hbox{mV/decade}$) at Room Temperature," *IEEE Electron Device Lett.*, vol. 32, no. 4, pp. 437–439, Apr. 2011.

[84]Y. Yang *et al.*, "Towards direct band-to-band tunneling in P-channel tunneling field effect transistor (TFET): Technology enablement by Germanium-tin (GeSn)," 2012, pp. 16.3.1-16.3.4.

[85]A. Villalon *et al.*, "Strained tunnel FETs with record ION: first demonstration of ETSOI TFETs with SiGe channel and RSD," 2012, pp. 49–50.

[86]G. Dewey *et al.*, "Fabrication, characterization, and physics of III-V heterojunction tunneling Field Effect Transistors (H-TFET) for steep sub-threshold swing," 2011, pp. 33.6.1-33.6.4.

[87]A. Alian *et al.*, "Record performance InGaAs homo-junction TFET with superior SS reliability over MOSFET," 2015, pp. 31.7.1-31.7.4.

[88]K. Ganapathi, Y. Yoon, and S. Salahuddin, "Analysis of InAs vertical and lateral band-to-band tunneling transistors: Leveraging vertical tunneling for improved performance," *Appl. Phys. Lett.*, vol. 97, no. 3, p. 033504, Jul. 2010.

[89]A. C. Ford *et al.*, "Ultrathin body InAs tunneling field-effect transistors on Si substrates," *Appl. Phys. Lett.*, vol. 98, no. 11, p. 113105, Mar. 2011.

[90]R. Li *et al.*, "AlGaSb/InAs Tunnel Field-Effect Transistor With On-Current of 78 µA/µm at 0.5 V," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 363–365, Mar. 2012.

[91]A. W. Dey *et al.*, "High-Current GaSb/InAs(Sb) Nanowire Tunnel Field-Effect Transistors," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 211–213, Feb. 2013.

[92]Guangle Zhou *et al.*, "Novel gate-recessed vertical InAs/GaSb TFETs with record high ION of 180μA/μm at VDS 0.5 V," 2012, pp. 32.6.1-32.6.4.

[93]K. S. Novoselov *et al.*, "Electric Field Effect in Atomically Thin Carbon Films," *Science*, vol. 306, no. 5696, pp. 666–669, Oct. 2004.

[94]M. G. Pala and D. Esseni, "Interface Traps in InAs Nanowire Tunnel-FETs and MOSFETs—Part I: Model Description and Single Trap Analysis in Tunnel-FETs," *IEEE Trans. Electron Devices*, vol. 60, no. 9, pp. 2795–2801, Sep. 2013.

[95]D. Esseni and M. G. Pala, "Interface Traps in InAs Nanowire Tunnel FETs and MOSFETs—Part II: Comparative Analysis and Trap-Induced Variability," *IEEE Trans. Electron Devices*, vol. 60, no. 9, pp. 2802–2807, Sep. 2013.

[96]F. Conzatti, M. G. Pala, and D. Esseni, "Surface-Roughness-Induced Variability in Nanowire InAs Tunnel FETs," *IEEE Electron Device Lett.*, vol. 33, no. 6, pp. 806–808, Jun. 2012.

[97]L. Britnell *et al.*, "Field-Effect Tunneling Transistor Based on Vertical Graphene Heterostructures," *Science*, vol. 335, no. 6071, pp. 947–950, Feb. 2012.

[98]N. Myoung, K. Seo, S. J. Lee, and G. Ihm, "Large Current Modulation and Spin-Dependent Tunneling of Vertical Graphene/MoS2 Heterostructures," *ACS Nano*, vol. 7, no. 8, pp. 7021–7027, Aug. 2013.

[99]J. Cao, A. Cresti, D. Esseni, and M. Pala, "Quantum simulation of a heterojunction vertical tunnel FET based on 2D transition metal dichalcogenides," *Solid-State Electron.*, vol. 116, pp. 1–7, Feb. 2016.

[100]D. Sarkar *et al.*, "A subthermionic tunnel field-effect transistor with an atomically thin channel," *Nature*, vol. 526, no. 7571, pp. 91–95, Oct. 2015.

[101]J. Cao *et al.*, "Operation and Design of van der Waals Tunnel Transistors: A 3-D Quantum Transport Study," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4388–4394, Nov. 2016.

[102]H. Ilatikhameneh, Y. Tan, B. Novakovic, G. Klimeck, R. Rahman, and J. Appenzeller, "Tunnel Field-Effect Transistors in 2-D Transition Metal Dichalcogenide Materials," *IEEE J. Explor. Solid-State Comput. Devices Circuits*, vol. 1, pp. 12–18, Dec. 2015.

[103]R. K. Ghosh and S. Mahapatra, "Monolayer Transition Metal Dichalcogenide Channel-Based Tunnel Transistor," *IEEE J. Electron Devices Soc.*, vol. 1, no. 10, pp. 175–180, Oct. 2013.

[104]K.-T. Lam, X. Cao, and J. Guo, "Device Performance of Heterojunction Tunneling Field-Effect Transistors Based on Transition Metal Dichalcogenide Monolayer," *IEEE Electron Device Lett.*, vol. 34, no. 10, pp. 1331–1333, Oct. 2013.

[105]T. Roy, M. Tosun, M. Hettick, G. H. Ahn, C. Hu, and A. Javey, "2D-2D tunneling field-effect transistors using WSe2/SnSe2 heterostructures," *Appl. Phys. Lett.*, vol. 108, no. 8, p. 083111, Feb. 2016.

[106]H. Ilatikhameneh, G. Klimeck, and R. Rahman, "2D tunnel transistors for ultra-low power applications: Promises and challenges," 2015, pp. 1–3.

[107]T. A. Ameen, H. Ilatikhameneh, G. Klimeck, and R. Rahman, "Few-layer Phosphorene: An Ideal 2D Material For Tunnel Transistors," *Sci. Rep.*, vol. 6, no. 1, Sep. 2016.

[108]Q. Zhang, G. Iannaccone, and G. Fiori, "Two-Dimensional Tunnel Transistors Based on Bi2Se3 Thin Film," *IEEE Electron Device Lett.*, vol. 35, no. 1, pp. 129–131, Jan. 2014.

[109]S. O. Koswatta, S. J. Koester, and W. Haensch, "On the Possibility of Obtaining MOSFET-Like Performance and Sub-60-mV/dec Swing in 1-D Broken-Gap Tunnel Transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 12, pp. 3222–3230, Dec. 2010.

[110]P. B. Pillai, P. Umari, and M. M. De Souza, "Are carbon nanotubes still a viable option for ITRS 2024?," 2013, pp. 32.2.1-32.2.4.

[111]D. A. Chenet *et al.*, "In-Plane Anisotropy in Mono- and Few-Layer ReS2 Probed by Raman Spectroscopy and Scanning Transmission Electron Microscopy," *Nano Lett.*, vol. 15, no. 9, pp. 5667–5672, Sep. 2015.

[112]J. Wu, N. Mao, L. Xie, H. Xu, and J. Zhang, "Identifying the Crystalline Orientation of Black Phosphorus Using Angle-Resolved Polarized Raman Spectroscopy," *Angew. Chem.*, vol. 127, no. 8, pp. 2396–2399, Feb. 2015.

[113]E. Torun, H. Sahin, S. Cahangirov, A. Rubio, and F. M. Peeters, "Anisotropic electronic, mechanical, and optical properties of monolayer WTe2," *J. Appl. Phys.*, vol. 119, no. 7, p. 074307, 2016.

[114]C. Lee, X. Wei, J. W. Kysar, and J. Hone, "Measurement of the Elastic Properties and Intrinsic Strength of Monolayer Graphene," *Science*, vol. 321, no. 5887, pp. 385–388, Jul. 2008.

[115]K. Liu *et al.*, "Elastic Properties of Chemical-Vapor-Deposited Monolayer MoS2 , WS2 , and Their Bilayer Heterostructures," *Nano Lett.*, vol. 14, no. 9, pp. 5097–5103, Sep. 2014.

[116]E. P. Randviir, D. A. C. Brownson, and C. E. Banks, "A decade of graphene research: production, applications and outlook," *Mater. Today*, vol. 17, no. 9, pp. 426–432, Nov. 2014.

[117]L. E. F. Foa Torres, S. Roche, and J.-C. Charlier, *Introduction to Graphene-Based Nanomaterials: From Electronic Structure to Quantum Transport*. Cambridge: Cambridge University Press, 2013.

[118]A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," *Rev. Mod. Phys.*, vol. 81, no. 1, pp. 109–162, Jan. 2009.

[119].....A. K. Geim and K. S. Novoselov, "THE RISE OF GRAPHENE," p. 14.

[120]K. S. Novoselov *et al.*, "Two-dimensional gas of massless Dirac fermions in graphene," *Nature*, vol. 438, no. 7065, pp. 197–200, Nov. 2005.

[121]K. I. Bolotin *et al.*, "Ultrahigh electron mobility in suspended graphene," *Solid State Commun.*, vol. 146, no. 9–10, pp. 351–355, Jun. 2008.

[122]I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors," *Nat. Nanotechnol.*, vol. 3, no. 11, pp. 654–659, Nov. 2008.

[123]E. McCann and V. I. Fal'ko, "Landau-Level Degeneracy and Quantum Hall Effect in a Graphite Bilayer," *Phys. Rev. Lett.*, p. 4, 2006.

[124]E. McCann, "Asymmetry gap in the electronic band structure of bilayer graphene," *Phys. Rev. B*, p. 4.

[125]M. Y. Han, B. Özyilmaz, Y. Zhang, and P. Kim, "Energy Band-Gap Engineering of Graphene Nanoribbons," *Phys. Rev. Lett.*, vol. 98, no. 20, May 2007.

[126]D. Querlioz *et al.*, "Suppression of the orientation effects on bandgap in graphene nanoribbons in the presence of edge disorder," *Appl. Phys. Lett.*, vol. 92, no. 4, p. 042108, Jan. 2008.

[127]S. Berrada *et al.*, "Graphene nanomesh transistor with high on/off ratio and good saturation behavior," *Appl. Phys. Lett.*, vol. 103, no. 18, p. 183509, Oct. 2013.

[128]N. V. Hung, F. Mazzamuto, J. Saint-Martin, A. Bournel, and P. Dollfus, "Graphene nanomesh-based devices exhibiting a strong negative differential conductance effect," *Nanotechnology*, vol. 23, no. 065201, 2012.

[129]J. Yang, M. Ma, L. Li, Y. Zhang, W. Huang, and X. Dong, "Graphene nanomesh: new versatile materials," *Nanoscale*, vol. 6, no. 22, pp. 13301–13313, Oct. 2014.

[130]D. Voiry, A. Mohite, and M. Chhowalla, "Phase engineering of transition metal dichalcogenides," *Chem. Soc. Rev.*, vol. 44, no. 9, pp. 2702–2712, 2015.

[131]J. Kang, S. Tongay, J. Zhou, J. Li, and J. Wu, "Band offsets and heterostructures of two-dimensional semiconductors," *Appl. Phys. Lett.*, vol. 102, no. 1, p. 012111, 2013.

[132]F. A. Rasmussen and K. S. Thygesen, "Computational 2D Materials Database: Electronic Structure of Transition-Metal Dichalcogenides and Oxides," *J. Phys. Chem. C*, vol. 119, no. 23, pp. 13169–13183, Jun. 2015.

[133]W. Zhang, Z. Huang, W. Zhang, and Y. Li, "Two-dimensional semiconductors with possible high room temperature mobility," *Nano Res.*, vol. 7, no. 12, pp. 1731–1737, Dec. 2014.

[134]G. Wang *et al.*, "Vertically Aligned MoS2 Nanosheets Patterned on Electrochemically Exfoliated Graphene for High-Performance Lithium and Sodium Storage," *Adv. Energy Mater.*, p. 1702254, Nov. 2017.

[135]H. Wang *et al.*, "Integrated Circuits Based on Bilayer MoS2 Transistors," *Nano Lett.*, vol. 12, no. 9, pp. 4674–4680, Sep. 2012.

[136]D. Ovchinnikov, A. Allain, Y.-S. Huang, D. Dumcenco, and A. Kis, "Electrical Transport Properties of Single-Layer WS2," *ACS Nano*, vol. 8, no. 8, pp. 8174–8181, Aug. 2014.

[137]K. Zhang, Y. Feng, F. Wang, Z. Yang, and J. Wang, "Two dimensional hexagonal boron nitride (2D-hBN): synthesis, properties and applications," *J. Mater. Chem. C*, vol. 5, no. 46, pp. 11992–12022, 2017.

[138]L. H. Li, J. Cervenka, K. Watanabe, T. Taniguchi, and Y. Chen, "Strong Oxidation Resistance of Atomically Thin Boron Nitride Nanosheets," *ACS Nano*, vol. 8, no. 2, pp. 1457–1462, Feb. 2014.

[139]R. Kumar, G. Rajasekaran, and A. Parashar, "Optimised cut-off function for Tersoff-like potentials for a BN nanosheet: a molecular dynamics study," *Nanotechnology*, vol. 27, no. 8, p. 085706, Feb. 2016.

[140]J. Eichler and C. Lesniak, "Boron nitride (BN) and BN composites for high-temperature applications," *J. Eur. Ceram. Soc.*, vol. 28, no. 5, pp. 1105–1109, Jan. 2008.

[141]Y. Zhao, Z. Wan, X. Xu, S. R. Patil, U. Hetmaniuk, and M. P. Anantram, "Negative Differential Resistance in Boron Nitride Graphene Heterostructures: Physical Mechanisms and Size Scaling Analysis," *Sci. Rep.*, vol. 5, p. 10712, May 2015.

[142]A. Mishchenko *et al.*, "Twist-controlled resonant tunnelling in graphene/boron nitride/graphene heterostructures," *Nat. Nanotechnol.*, vol. 9, no. 10, pp. 808–813, Sep. 2014.

[143]G. Fiori, S. Bruzzone, and G. Iannaccone, "Very Large Current Modulation in Vertical Heterostructure Graphene/hBN Transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 268–273, Jan. 2013.

[144]J. Zhuang, X. Xu, H. Feng, Z. Li, X. Wang, and Y. Du, "Honeycomb silicon: a review of silicene," *Sci. Bull.*, vol. 60, no. 18, pp. 1551–1562, Sep. 2015.

[145]A. V. Gert, M. O. Nestoklon, and I. N. Yassievich, "Band structure of silicene in the tight binding approximation," *J. Exp. Theor. Phys.*, vol. 121, no. 1, pp. 115–121, Aug. 2015.

[146]A. Nijamudheen, R. Bhattacharjee, S. Choudhury, and A. Datta, "Electronic and Chemical Properties of Germanene: The Crucial Role of Buckling," *J. Phys. Chem. C*, vol. 119, no. 7, pp. 3802–3809, Feb. 2015.

[147]H. Behera and G. Mukhopadhyay, "First-Principles Study of Structural and Electronic Properties of Germanene," *ArXiv11116333 Cond-Mat*, pp. 823–824, 2011.

[148]M. Houssa, A. Dimoulas, and A. Molle, "Silicene: a review of recent experimental and theoretical investigations," *J. Phys. Condens. Matter*, vol. 27, no. 25, p. 253002, Jun. 2015.

[149]R. Quhe *et al.*, "Tunable and sizable band gap in silicene by surface adsorption," *Sci. Rep.*, vol. 2, no. 1, Dec. 2012.

[150]M. Ye *et al.*, "Tunable band gap in germanene by surface adsorption," *Phys. E Low-Dimens. Syst. Nanostructures*, vol. 59, pp. 60–65, May 2014.

[151]Z.-G. Shao, X.-S. Ye, L. Yang, and C.-L. Wang, "First-principles calculation of intrinsic carrier mobility of silicene," *J. Appl. Phys.*, vol. 114, no. 9, p. 093712, Sep. 2013.

[152]X.-S. Ye, Z.-G. Shao, H. Zhao, L. Yang, and C.-L. Wang, "Intrinsic carrier mobility of germanene is larger than graphene's: first-principle calculations," *RSC Adv*, vol. 4, no. 41, pp. 21216–21220, 2014.

[153]N. D. Drummond, V. Zólyomi, and V. I. Fal'ko, "Electrically tunable band gap in silicene," *Phys. Rev. B*, vol. 85, no. 7, Feb. 2012.

[154]L. Tao *et al.*, "Silicene field-effect transistors operating at room temperature," *Nat. Nanotechnol.*, vol. 10, no. 3, pp. 227–231, Mar. 2015.

[155]C.-C. Liu, W. Feng, and Y. Yao, "Quantum Spin Hall Effect in Silicene and Two-Dimensional Germanium," *Phys. Rev. Lett.*, vol. 107, no. 7, Aug. 2011.

[156]P. Vogt *et al.*, "Silicene: Compelling Experimental Evidence for Graphenelike Two-Dimensional Silicon," *Phys. Rev. Lett.*, vol. 108, no. 15, Apr. 2012.

[157]B. Feng *et al.*, "Evidence of Silicene in Honeycomb Structures of Silicon on Ag(111)," *Nano Lett.*, vol. 12, no. 7, pp. 3507–3511, Jul. 2012.

[158]A. Fleurence, R. Friedlein, T. Ozaki, H. Kawai, Y. Wang, and Y. Yamada-Takamura, "Experimental Evidence for Epitaxial Silicene on Diboride Thin Films," *Phys. Rev. Lett.*, vol. 108, no. 24, Jun. 2012.

[159]D. Chiappe, C. Grazianetti, G. Tallarida, M. Fanciulli, and A. Molle, "Local Electronic Properties of Corrugated Silicene Phases," *Adv. Mater.*, vol. 24, no. 37, pp. 5088–5093, Sep. 2012.

[160]L. Meng *et al.*, "Buckled Silicene Formation on Ir(111)," *Nano Lett.*, vol. 13, no. 2, pp. 685–690, Feb. 2013.

[161]M. Derivaz *et al.*, "Continuous Germanene Layer on Al(111)," *Nano Lett.*, vol. 15, no. 4, pp. 2510–2516, Apr. 2015.

[162]G. Liu *et al.*, "Multiple Dirac Points and Hydrogenation-Induced Magnetism of Germanene Layer on Al (111) Surface," *J. Phys. Chem. Lett.*, vol. 6, no. 24, pp. 4936–4942, Dec. 2015.

[163]R. Stephan *et al.*, "Germanene on Al(111): Interface Electronic States and Charge Transfer," *J. Phys. Chem. C*, vol. 120, no. 3, pp. 1580–1585, Jan. 2016.

[164]M. E. Dávila, L. Xian, S. Cahangirov, A. Rubio, and G. Le Lay, "Germanene: a novel two-dimensional germanium allotrope akin to graphene and silicene," *New J. Phys.*, vol. 16, no. 9, p. 095002, Sep. 2014.

[165]M. E. Dávila and G. Le Lay, "Few layer epitaxial germanene: a novel two-dimensional Dirac material," *Sci. Rep.*, vol. 6, no. 1, Aug. 2016.

[166]L. Li *et al.*, "Buckled Germanene Formation on Pt(111)," *Adv. Mater.*, vol. 26, no. 28, pp. 4820–4824, Jul. 2014.

[167]L. Zhang *et al.*, "Structural and Electronic Properties of Germanene on MoS 2," *Phys. Rev. Lett.*, vol. 116, no. 25, Jun. 2016.

[168]J. Gou *et al.*, "Strained monolayer germanene with 1 × 1 lattice on Sb(111)," *2D Mater.*, vol. 3, no. 4, p. 045005, Sep. 2016.

[169]Y. Wang *et al.*, "HALF-METALLIC SILICENE AND GERMANENE NANORIBBONS: TOWARDS HIGH-PERFORMANCE SPINTRONICS DEVICE," *Nano*, vol. 07, no. 05, p. 1250037, Oct. 2012.

[170]C. Xu *et al.*, "Giant magnetoresistance in silicene nanoribbons," *Nanoscale*, vol. 4, no. 10, p. 3111, 2012.

[171]H. Liu *et al.*, "Phosphorene: An Unexplored 2D Semiconductor with a High Hole Mobility," *ACS Nano*, vol. 8, no. 4, pp. 4033–4041, Apr. 2014.

[172]S. Das, W. Zhang, M. Demarteau, A. Hoffmann, M. Dubey, and A. Roelofs, "Tunable Transport Gap in Phosphorene," *Nano Lett.*, vol. 14, no. 10, pp. 5733–5739, Oct. 2014.

[173]J. Kim *et al.*, "Observation of tunable band gap and anisotropic Dirac semimetal state in black phosphorus," *Science*, vol. 349, no. 6249, pp. 723–726, Aug. 2015.

[174]X. Peng, Q. Wei, and A. Copple, "Strain-engineered direct-indirect band gap transition and its mechanism in two-dimensional phosphorene," *Phys. Rev. B*, vol. 90, no. 8, Aug. 2014.

[175]Q. Wei and X. Peng, "Superior mechanical flexibility of phosphorene and few-layer black phosphorus," *Appl. Phys. Lett.*, vol. 104, no. 25, p. 251915, Jun. 2014.

[176]M. Buscema, D. J. Groenendijk, S. I. Blanter, G. A. Steele, H. S. J. van der Zant, and A. Castellanos-Gomez, "Fast and Broadband Photoresponse of Few-Layer Black Phosphorus Field-Effect Transistors," *Nano Lett.*, vol. 14, no. 6, pp. 3347–3352, Jun. 2014.

[177]F. Xia, H. Wang, and Y. Jia, "Rediscovering black phosphorus as an anisotropic layered material for optoelectronics and electronics," *Nat. Commun.*, vol. 5, no. 1, Dec. 2014.

[178]V. Tran, R. Soklaski, Y. Liang, and L. Yang, "Layer-controlled band gap and anisotropic excitons in few-layer black phosphorus," *Phys. Rev. B*, vol. 89, no. 23, Jun. 2014.

[179]L. Kou, C. Chen, and S. C. Smith, "Phosphorene: Fabrication, Properties, and Applications," *J. Phys. Chem. Lett.*, vol. 6, no. 14, pp. 2794–2805, Jul. 2015.

[180]R. Fei, A. Faghaninia, R. Soklaski, J.-A. Yan, C. Lo, and L. Yang, "Enhanced Thermoelectric Efficiency via Orthogonal Electrical and Thermal Conductances in Phosphorene," *Nano Lett.*, vol. 14, no. 11, pp. 6393–6399, Nov. 2014.

[181]Y. Jing, Q. Tang, P. He, Z. Zhou, and P. Shen, "Small molecules make big differences: molecular doping effects on electronic and optical properties of phosphorene," *Nanotechnology*, vol. 26, no. 9, p. 095201, Mar. 2015.

[182]I. V. Grigorieva, "Van der Waals heterostructures," *Nature*, vol. 499, no. 7459, pp. 419–425, Jul. 2013.

[183]A. Lipp, K. A. Schwetz, and K. Hunold, "Hexagonal boron nitride: Fabrication, properties and applications," *J. Eur. Ceram. Soc.*, vol. 5, no. 1, pp. 3–9, 1989.

[184]H. Hibino, H. Kageshima, and M. Nagase, "Graphene Growth on Silicon Carbide," vol. 8, no. 8, p. 6, 2010.

[185]P. Miró, M. Audiffred, and T. Heine, "An atlas of two-dimensional materials," *Chem. Soc. Rev.*, vol. 43, no. 18, pp. 6537–6554, Aug. 2014.

[186]A. Molle, C. Grazianetti, L. Tao, D. Taneja, M. H. Alam, and D. Akinwande, "Silicene, silicene derivatives, and their device applications," *Chem. Soc. Rev.*, vol. 47, no. 16, pp. 6370–6387, 2018.

[187]S. Balendhran, S. Walia, H. Nili, S. Sriram, and M. Bhaskaran, "Elemental Analogues of Graphene: Silicene, Germanene, Stanene, and Phosphorene," *Small*, vol. 11, no. 6, pp. 640–652, Feb. 2015.

[188]F. Zhu *et al.*, "Epitaxial growth of two-dimensional stanene," *Nat. Mater.*, vol. 14, no. 10, pp. 1020–1025, Oct. 2015.

[189]H. R. Jiang, Z. Lu, M. C. Wu, F. Ciucci, and T. S. Zhao, "Borophene: A promising anode material offering high specific capacity and high rate capability for lithium-ion batteries," *Nano Energy*, vol. 23, pp. 97–104, May 2016.

[190]A. A. Kistanov, Y. Cai, K. Zhou, N. Srikanth, S. V. Dmitriev, and Y.-W. Zhang, "Exploring the charge localization and band gap opening of borophene: a first-principles study," *Nanoscale*, vol. 10, no. 3, pp. 1403–1410, 2018.

[191]A. J. Mannix *et al.*, "Synthesis of borophenes: Anisotropic, two-dimensional boron polymorphs," *Science*, vol. 350, no. 6267, pp. 1513–1516, Dec. 2015.

[192]V. Kochat *et al.*, "Atomically thin gallium layers from solid-melt exfoliation," *Sci. Adv.*, vol. 4, no. 3, p. e1701373, Mar. 2018.

[193]M. Pumera and Z. Sofer, "2D Monoelemental Arsenene, Antimonene, and Bismuthene: Beyond Black Phosphorus," *Adv. Mater.*, vol. 29, no. 21, p. 1605299, Jun. 2017.

[194]S. Zhang, Z. Yan, Y. Li, Z. Chen, and H. Zeng, "Atomically Thin Arsenene and Antimonene: Semimetal-Semiconductor and Indirect-Direct Band-Gap Transitions," *Angew. Chem.*, vol. 127, no. 10, pp. 3155–3158, Mar. 2015.

[195]E. Aktürk, O. Ü. Aktürk, and S. Ciraci, "Single and bilayer bismuthene: Stability at high temperature and mechanical and electronic properties," *Phys. Rev. B*, vol. 94, no. 1, Jul. 2016.

[196]F. Reis *et al.*, "Bismuthene on a SiC substrate: A candidate for a high-temperature quantum spin Hall material," *Science*, vol. 357, no. 6348, pp. 287–290, Jul. 2017.

[197]L. Xian, A. Pérez Paz, E. Bianco, P. M. Ajayan, and A. Rubio, "Square selenene and tellurene: novel group VI elemental 2D materials with nontrivial topological properties," *2D Mater.*, vol. 4, no. 4, p. 041003, Aug. 2017.

[198]D. C. Elias *et al.*, "Control of Graphene's Properties by Reversible Hydrogenation: Evidence for Graphane," *Science*, vol. 323, no. 5914, pp. 610–613, Jan. 2009.

[199]M. Inagaki and F. Kang, "Graphene derivatives: graphane, fluorographene, graphene oxide, graphyne and graphdiyne," *J Mater Chem A*, vol. 2, no. 33, pp. 13193–13206, 2014.

[200]V. Zólyomi, J. R. Wallbank, and V. I. Fal'ko, "Silicane and germanane: tight-binding and first-principles studies," *2D Mater.*, vol. 1, no. 1, p. 011005, Apr. 2014.

[201]M. Ali, X. Pi, Y. Liu, and D. Yang, "Electronic and magnetic properties of graphene, silicene and germanene with varying vacancy concentration," *AIP Adv.*, vol. 7, no. 4, p. 045308, Apr. 2017.

[202]K.-J. Jeon *et al.*, "Fluorographene: A Wide Bandgap Semiconductor with Ultraviolet Luminescence," *ACS Nano*, vol. 5, no. 2, pp. 1042–1046, Feb. 2011.

[203]D. K. Samarakoon, Z. Chen, C. Nicolas, and X.-Q. Wang, "Structural and Electronic Properties of Fluorographene," *Small*, vol. 7, no. 7, pp. 965–969, Apr. 2011.

[204]H. Şahin and S. Ciraci, "Chlorine Adsorption on Graphene: Chlorographene," *J. Phys. Chem. C*, vol. 116, no. 45, pp. 24075–24083, Nov. 2012.

[205]F. Karlický, K. Kumara Ramanatha Datta, M. Otyepka, and R. Zbořil, "Halogenated Graphenes: Rapidly Growing Family of Graphene Derivatives," *ACS Nano*, vol. 7, no. 8, pp. 6434–6464, Aug. 2013.

[206]Y. Munaiah, P. Ragupathy, and V. K. Pillai, "Single-Step Synthesis of Halogenated Graphene through Electrochemical Exfoliation and Its Utilization as Electrodes for Zinc Bromine Redox Flow Battery," *J. Electrochem. Soc.*, vol. 163, no. 14, pp. A2899–A2910, 2016.

[207]M. Sun, S. Wang, J. Yu, and W. Tang, "Hydrogenated and halogenated blue phosphorene as Dirac materials: A first principles study," *Appl. Surf. Sci.*, vol. 392, pp. 46–50, Jan. 2017.

[208]N. Gao, W. T. Zheng, and Q. Jiang, "Density functional theory calculations for two-dimensional silicene with halogen functionalization," *Phys Chem Chem Phys*, vol. 14, no. 1, pp. 257–261, 2012.

[209]W.-B. Zhang, Z.-B. Song, and L.-M. Dou, "The tunable electronic structure and mechanical properties of halogenated silicene: a first-principles study," *J. Mater. Chem. C*, vol. 3, no. 13, pp. 3087–3094, 2015.

[210]P. Liang, Y. Liu, S. Xing, H. Shu, and B. Tai, "Electronic and magnetic properties of germanene: Surface functionalization and strain effects," *Solid State Commun.*, vol. 226, pp. 19–24, Jan. 2016.

[211]Q. Pang, Y. Zhang, J.-M. Zhang, V. Ji, and K.-W. Xu, "Electronic and magnetic properties of pristine and chemically functionalized germanene nanoribbons," *Nanoscale*, vol. 3, no. 10, p. 4330, 2011.

[212]C. Si, J. Liu, Y. Xu, J. Wu, B.-L. Gu, and W. Duan, "Functionalized germanene as a prototype of large-gap two-dimensional topological insulators," *Phys. Rev. B*, vol. 89, no. 11, Mar. 2014.

[213]B. G. Kim and H. J. Choi, "Graphyne: Hexagonal network of carbon with versatile Dirac cones," *Phys. Rev. B*, vol. 86, no. 11, Sep. 2012.

[214]L. D. Pan, L. Z. Zhang, B. Q. Song, S. X. Du, and H.-J. Gao, "Graphyne- and graphdiyne-based nanoribbons: Density functional theory calculations of electronic structures," *Appl. Phys. Lett.*, vol. 98, no. 17, p. 173102, Apr. 2011.

[215]Y. Pei and H.-B. Wu, "Optimized geometry and electronic structure of graphyne-like silicyne nanoribbons," *Chin. Phys. B*, vol. 22, no. 5, p. 057303, May 2013.

[216]E. Aktürk and G. Gökoğlu, "Silicon-based counterpart of alpha-graphyne," *Phys. Lett. A*, vol. 378, no. 18–19, pp. 1313–1315, Mar. 2014.

[217]Y. Zhu, H. Bai, and Y. Huang, "Crystal orbital studies on the 1D silic-diyne nanoribbons and nanotubes," *J. Phys. Condens. Matter*, vol. 28, no. 4, p. 045303, Feb. 2016.

[218]J. Xia *et al.*, "CVD synthesis of large-area, highly crystalline MoSe2 atomic layers on diverse substrates and application to photodetectors," *Nanoscale*, vol. 6, no. 15, p. 8949, Jun. 2014.

[219]L. Zhou *et al.*, "Large-Area Synthesis of High-Quality Uniform Few-Layer MoTe2," *J. Am. Chem. Soc.*, vol. 137, no. 37, pp. 11892–11895, Sep. 2015.

[220]H. J. Liu *et al.*, "Molecular-beam epitaxy of monolayer and bilayer WSe2 : a scanning tunneling microscopy/spectroscopy study and deduction of exciton binding energy," *2D Mater.*, vol. 2, no. 3, p. 034004, Jun. 2015.

[221]C. H. Naylor *et al.*, "Large-area synthesis of high-quality monolayer 1T'-WTe2 flakes," *2D Mater.*, vol. 4, no. 2, p. 021008, Feb. 2017.

[222]H. Guo, N. Lu, L. Wang, X. Wu, and X. C. Zeng, "Tuning Electronic and Magnetic Properties of Early Transition-Metal Dichalcogenides via Tensile Strain," *J. Phys. Chem. C*, vol. 118, no. 13, pp. 7242–7249, Apr. 2014.

[223]Y. Li, J. Kang, and J. Li, "Indirect-to-direct band gap transition of the ZrS2 monolayer by strain: first-principles calculations," *RSC Adv.*, vol. 4, no. 15, p. 7396, 2014.

[224]G. Seifert, H. Terrones, M. Terrones, and T. Frauenheim, "Novel NbS2 metallic nanotubes," *Solid State Commun.*, vol. 115, no. 12, pp. 635–638, Aug. 2000.

[225]A. Kuc, N. Zibouche, and T. Heine, "Influence of quantum confinement on the electronic structure of the transition metal sulfide T S 2," *Phys. Rev. B*, vol. 83, no. 24, Jun. 2011.

[226]P. Miró, M. Ghorbani-Asl, and T. Heine, "Two Dimensional Materials Beyond MoS2: Noble-Transition-Metal Dichalcogenides," *Angew. Chem. Int. Ed.*, vol. 53, no. 11, pp. 3015–3018, Mar. 2014.

[227]V. V. Ivanovskaya, "Electronic Structure of Titanium Disulfide Nanostructures: Monolayers, Nanostripes, and Nanotubes," *Semiconductors*, vol. 39, no. 9, p. 1058, 2005.

[228]Y. Zhao *et al.*, "Extraordinarily Strong Interlayer Interaction in 2D Layered PtS2," *Adv. Mater.*, vol. 28, no. 12, pp. 2399–2407, Mar. 2016.

[229]Q. Peng *et al.*, "Mechanical properties and stabilities of g-ZnS monolayers," *RSC Adv.*, vol. 5, no. 15, pp. 11240–11247, 2015.

[230]M. Shahrokhi, "Quasi-particle energies and optical excitations of ZnS monolayer honeycomb structure," *Appl. Surf. Sci.*, vol. 390, pp. 377–384, Dec. 2016.

[231]L. Li, P. Li, N. Lu, J. Dai, and X. C. Zeng, "Simulation Evidence of Hexagonal-to-Tetragonal ZnSe Structure Transition: A Monolayer Material with a Wide-Range Tunable Direct Bandgap," *Adv. Sci.*, vol. 2, no. 12, p. 1500290, Dec. 2015.

[232]J. Zhou, J. Huang, B. G. Sumpter, P. R. C. Kent, H. Terrones, and S. C. Smith, "Structures, Energetics, and Electronic Properties of Layered Materials and Nanotubes of Cadmium Chalcogenides," *J. Phys. Chem. C*, vol. 117, no. 48, pp. 25817–25825, Dec. 2013.

[233]D. V. Talapin, A. L. Rogach, A. Kornowski, M. Haase, and H. Weller, "Highly Luminescent Monodisperse CdSe and CdSe/ZnS Nanocrystals Synthesized in a Hexadecylamine−Trioctylphosphine Oxide−Trioctylphospine Mixture," *Nano Lett.*, vol. 1, no. 4, pp. 207–211, Apr. 2001.

[234]B. O. Dabbousi *et al.*, "(CdSe)ZnS Core−Shell Quantum Dots: Synthesis and Characterization of a Size Series of Highly Luminescent Nanocrystallites," *J. Phys. Chem. B*, vol. 101, no. 46, pp. 9463–9475, Nov. 1997.

[235]H. Hillebrecht *et al.*, "Structural and scanning microscopy studies of layered compounds MCl3 (M = Mo, Ru, Cr) and MOCl2 (M = V, Nb, Mo, Ru, Os)," *J. Alloys Compd.*, vol. 246, no. 1–2, pp. 70–79, Jan. 1997.

[236]Y. Zhou, H. Lu, X. Zu, and F. Gao, "Evidencing the existence of exciting half-metallicity in two-dimensional TiCl3 and VCl3 sheets," *Sci. Rep.*, vol. 6, no. 1, May 2016.

[237]L. Huang, Z. Chen, and J. Li, "Effects of strain on the band gap and effective mass in two-dimensional monolayer GaX (X = S, Se, Te)," *RSC Adv.*, vol. 5, no. 8, pp. 5788–5794, 2015.

[238]Y. Ma, Y. Dai, M. Guo, L. Yu, and B. Huang, "Tunable electronic and dielectric behavior of GaS and GaSe monolayers," *Phys. Chem. Chem. Phys.*, vol. 15, no. 19, p. 7098, 2013.

[239]J. Jalilian and M. Safari, "Electronic and optical properties of α -InX (X = S, Se and Te) monolayer: Under strain conditions," *Phys. Lett. A*, vol. 381, no. 15, pp. 1313–1320, Apr. 2017.

[240]H. Jin, J. Li, Y. Dai, and Y. Wei, "Engineering the electronic and optoelectronic properties of InX (X = S, Se, Te) monolayers via strain," *Phys. Chem. Chem. Phys.*, vol. 19, no. 6, pp. 4855–4860, 2017.

[241]E. Guerriero *et al.*, "Gigahertz Integrated Graphene Ring Oscillators," *ACS Nano*, vol. 7, no. 6, pp. 5588–5594, Jun. 2013.

[242]C.-H. Jan *et al.*, "A 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications," 2012, pp. 3.1.1-3.1.4.

[243]T. Ohta, "Controlling the Electronic Structure of Bilayer Graphene," 07-Nov-2016. [Online]. Available: http://pubman.mpdl.mpg.de/pubman/item/escidoc:737967/component/escidoc:737966/280856.pdf. [Accessed: 07-Nov-2016].

[244]J. B. Oostinga, H. B. Heersche, X. Liu, A. F. Morpurgo, and L. M. K. Vandersypen, "Gate-induced insulating state in bilayer graphene devices," *Nat. Mater.*, vol. 7, no. 2, pp. 151–157, Feb. 2008.

[245]T. Kawasaki, T. Ichimura, H. Kishimoto, A. A. Akbar, T. Ogawa, and C. Oshima, "DOUBLE ATOMIC LAYERS OF GRAPHENE/MONOLAYER h-BN ON Ni(111) STUDIED BY SCANNING TUNNELING MICROSCOPY AND SCANNING TUNNELING SPECTROSCOPY," *Surf. Rev. Lett.*, vol. 09, no. 03n04, pp. 1459–1464, Jun. 2002.

[246]A. A. Balandin, "Thermal properties of graphene and nanostructured carbon materials," *Nat. Mater.*, vol. 10, no. 8, pp. 569–581, Aug. 2011.

[247]M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, "A Graphene Field-Effect Device," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 282–284, Apr. 2007.

[248]L. Liao *et al.*, "Scalable Fabrication of Self-Aligned Graphene Transistors and Circuits on Glass," *Nano Lett.*, vol. 12, no. 6, pp. 2653–2657, Jun. 2012.

[249]L. Liao *et al.*, "High- oxide nanoribbons as gate dielectrics for high mobility top-gated graphene transistors," *Proc. Natl. Acad. Sci.*, vol. 107, no. 15, pp. 6711–6715, Apr. 2010.

[250]D. B. Farmer, H.-Y. Chiu, Y.-M. Lin, K. A. Jenkins, F. Xia, and P. Avouris, "Utilization of a Buffered Dielectric to Achieve High Field-Effect Carrier Mobility in Graphene Transistors," *Nano Lett.*, vol. 9, no. 12, pp. 4474–4478, Dec. 2009.

[251]L. G. Rizzi *et al.*, "Cascading Wafer-Scale Integrated Graphene Complementary Inverters under Ambient Conditions," *Nano Lett.*, vol. 12, no. 8, pp. 3948–3953, Aug. 2012.

[252]E. Guerriero *et al.*, "High-Gain Graphene Transistors with a Thin AlOx Top-Gate Oxide," *Sci. Rep.*, vol. 7, no. 1, Dec. 2017.

[253]Q. Wilmart *et al.*, "A Klein-tunneling transistor with ballistic graphene," *2D Mater.*, vol. 1, no. 1, p. 011006, Apr. 2014.

[254]Q. Wilmart *et al.*, "Contact gating at GHz frequency in graphene," *Sci. Rep.*, vol. 6, no. 1, Aug. 2016.

[255]E. Pallecchi *et al.*, "Graphene nanotransistors for RF charge detection," *J. Phys. Appl. Phys.*, vol. 47, no. 9, p. 094004, Mar. 2014.

[256]V. Podzorov, M. E. Gershenson, C. Kloc, R. Zeis, and E. Bucher, "High-mobility field-effect transistors based on transition metal dichalcogenides," *Appl. Phys. Lett.*, vol. 84, no. 17, pp. 3301–3303, Apr. 2004.

[257]H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, and A. Javey, "High-Performance Single Layered WSe2 p-FETs with Chemically Doped Contacts," *Nano Lett.*, vol. 12, no. 7, pp. 3788–3792, Jul. 2012.

[258]B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS2 transistors," *Nat. Nanotechnol.*, vol. 6, no. 3, pp. 147–150, Mar. 2011.

[259]F. Chen, H. Ilatikhameneh, Y. Tan, D. Valencia, G. Klimeck, and R. Rahman, "Transport in vertically stacked hetero-structures from 2D materials," *J. Phys. Conf. Ser.*, vol. 864, p. 012053, Jun. 2017.

[260]S. Roche and S. O. Valenzuela, "Graphene spintronics: puzzling controversies and challenges for spin manipulation," *J. Phys. Appl. Phys.*, vol. 47, no. 9, p. 094011, Mar. 2014.

[261]M. B. Lundeberg, R. Yang, J. Renard, and J. A. Folk, "Defect-Mediated Spin Relaxation and Dephasing in Graphene," *Phys. Rev. Lett.*, vol. 110, no. 15, Apr. 2013.

[262]M. I. Katsnelson, *Graphene: Carbon in Two Dimensions*. Cambridge: Cambridge University Press, 2012.

[263]W. Han, R. K. Kawakami, M. Gmitra, and J. Fabian, "Graphene spintronics," *Nat. Nanotechnol.*, vol. 9, no. 10, pp. 794–807, Oct. 2014.

[264]F. Seitz, H. Ehrenreich, and y Yafet, Eds., *Solid state physics: advances in research and applications. Vol. 14: ...* New York, NY: Academic Press, 1963.

[265]R. J. Elliott, "Theory of the Effect of Spin-Orbit Coupling on Magnetic Resonance in Some Semiconductors," *Phys. Rev.*, vol. 96, no. 2, pp. 266–279, Oct. 1954.

[266]D. V. Tuan, F. Ortmann, D. Soriano, S. O. Valenzuela, and S. Roche, "Pseudospin-driven spin relaxation mechanism in graphene," *Nat. Phys.*, vol. 10, no. 11, pp. 857–863, Nov. 2014.

[267]M. Drögeler *et al.*, "Spin Lifetimes Exceeding 12 ns in Graphene Nonlocal Spin Valve Devices," *Nano Lett.*, vol. 16, no. 6, pp. 3533–3539, Jun. 2016.

[268]W. Yan *et al.*, "Long Spin Diffusion Length in Few-Layer Graphene Flakes," *Phys. Rev. Lett.*, vol. 117, no. 14, Sep. 2016.

[269]W. Han and R. K. Kawakami, "Spin Relaxation in Single Layer and Bilayer Graphene," p. 22.

[270]A. Ramasubramaniam and D. Naveh, "Mn-doped monolayer MoS 2 : An atomically thin dilute magnetic semiconductor," *Phys. Rev. B*, vol. 87, no. 19, May 2013.

[271]Y. Wang *et al.*, "Defects engineering induced room temperature ferromagnetism in transition metal doped MoS 2," *Mater. Des.*, vol. 121, pp. 77–84, May 2017.

[272]T. Garandel, R. Arras, X. Marie, P. Renucci, and L. Calmels, "Charge transfer and magnetization of a MoS2 monolayer at the Co(0001)/MoS2 interface," *J. Phys. Conf. Ser.*, vol. 903, p. 012017, Oct. 2017.

[273]J. Klinovaja and D. Loss, "Spintronics in MoS 2 monolayer quantum wires," *Phys. Rev. B*, vol. 88, no. 7, Aug. 2013.

[274]C. Mai *et al.*, "Many-Body Effects in Valleytronics: Direct Measurement of Valley Lifetimes in Single-Layer MoS2," *Nano Lett.*, vol. 14, no. 1, pp. 202–206, Jan. 2014.

[275]Y. K. Luo *et al.*, "Opto-Valleytronic Spin Injection in Monolayer MoS2/Few-Layer Graphene Hybrid Spin Valves," *Nano Lett.*, vol. 17, no. 6, pp. 3877–3883, Jun. 2017.

[276]J. R. Schaibley *et al.*, "Valleytronics in 2D materials," *Nat. Rev. Mater.*, vol. 1, no. 11, Nov. 2016.

[277]C. Robert *et al.*, "Spin and valley polarization in MoS2, MoSe2, and WSe2 monolayers (Conference Presentation)," 2016, p. 99313C.

[278]I. Khrapach *et al.*, "Novel Highly Conductive and Transparent Graphene-Based Conductors," *Adv. Mater.*, vol. 24, no. 21, pp. 2844–2849, Jun. 2012.

[279]C.-Y. Teng, T.-F. Yeh, K.-I. Lin, S.-J. Chen, M. Yoshimura, and H. Teng, "Synthesis of graphene oxide dots for excitation-wavelength independent photoluminescence at high quantum yields," *J. Mater. Chem. C*, vol. 3, no. 17, pp. 4553–4562, 2015.

[280]A. S. Mayorov *et al.*, "Micrometer-Scale Ballistic Transport in Encapsulated Graphene at Room Temperature," *Nano Lett.*, vol. 11, no. 6, pp. 2396–2399, Jun. 2011.

[281]D. Englund, R.-J. Shiue, and Xuetao Gan, "On-chip graphene optoelectronic devices for optical interconnects," 2014, pp. 348–349.

[282]K. J. A. Ooi, P. C. Leong, L. K. Ang, and D. T. H. Tan, "All-optical control on a graphene-on-silicon waveguide modulator," *Sci. Rep.*, vol. 7, no. 1, Dec. 2017.

[283]R. Chowdri, N. M. Hossain, and M. H. Chowdhury, "High-speed graphene based quantum-optical interconnect design," 2015, pp. 1–4.

[284]W. Zhu *et al.*, "Graphene radio frequency devices on flexible substrate," *Appl. Phys. Lett.*, vol. 102, no. 23, p. 233102, Jun. 2013.

[285]M. Bass, V. N. Mahajan, and Optical Society of America, Eds., *Handbook of optics*, 3rd ed. New York: McGraw-Hill, 2010.

[286]J. Wang, Y. Hernandez, M. Lotya, J. N. Coleman, and W. J. Blau, "Broadband Nonlinear Optical Response of Graphene Dispersions," *Adv. Mater.*, vol. 21, no. 23, pp. 2430–2435, Jun. 2009.

[287]A. R. Wright, X. G. Xu, J. C. Cao, and C. Zhang, "Strong nonlinear optical response of graphene in the terahertz regime," *Appl. Phys. Lett.*, vol. 95, no. 7, p. 072101, Aug. 2009.

[288]J. M. Dawlaty *et al.*, "Measurement of the optical absorption spectra of epitaxial graphene from terahertz to visible," *Appl. Phys. Lett.*, vol. 93, no. 13, p. 131905, Sep. 2008.

[289]T. Mueller, F. Xia, and P. Avouris, "Graphene photodetectors for high-speed optical communications," *Nat. Photonics*, vol. 4, no. 5, pp. 297–301, May 2010.

[290]J. Park, Y. H. Ahn, and C. Ruiz-Vargas, "Imaging of Photocurrent Generation and Collection in Single-Layer Graphene," *Nano Lett.*, vol. 9, no. 5, pp. 1742–1746, May 2009.

[291]M. C. Lemme *et al.*, "Gate-Activated Photoresponse in a Graphene p–n Junction," *Nano Lett.*, vol. 11, no. 10, pp. 4134–4137, Oct. 2011.

[292]N. M. Gabor *et al.*, "Hot Carrier-Assisted Intrinsic Photoresponse in Graphene," *Science*, vol. 334, no. 6056, pp. 648–652, Nov. 2011.

[293]T. Hasan *et al.*, "Nanotube–Polymer Composites for Ultrafast Photonics," *Adv. Mater.*, vol. 21, no. 38–39, pp. 3874–3899, Oct. 2009.

[294]C. Feng, Y. Wang, J. Liu, Y. H. Tsang, Y. Song, and Z. Yu, "3W high-power laser passively mode-locked by graphene oxide saturable absorber," *Opt. Commun.*, vol. 298–299, pp. 168–170, Jul. 2013.

[295]Z. Sun *et al.*, "Graphene Mode-Locked Ultrafast Laser," *ACS Nano*, vol. 4, no. 2, pp. 803–810, Feb. 2010.

[296]Z. Sun *et al.*, "A stable, wideband tunable, near transform-limited, graphene-mode-locked, ultrafast laser," *Nano Res.*, vol. 3, no. 9, pp. 653–660, Sep. 2010.

[297]Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, "Electronics and optoelectronics of two-dimensional transition metal dichalcogenides," *Nat. Nanotechnol.*, vol. 7, no. 11, pp. 699–712, Nov. 2012.

[298]Z. Yin *et al.*, "Single-Layer MoS2 Phototransistors," *ACS Nano*, vol. 6, no. 1, pp. 74–80, Jan. 2012.

[299]O. Lopez-Sanchez, D. Lembke, M. Kayci, A. Radenovic, and A. Kis, "Ultrasensitive photodetectors based on monolayer MoS2," *Nat. Nanotechnol.*, vol. 8, no. 7, pp. 497–501, Jul. 2013.

[300]H. S. Lee *et al.*, "MoS2 Nanosheet Phototransistors with Thickness-Modulated Optical Energy Gap," *Nano Lett.*, vol. 12, no. 7, pp. 3695–3700, Jul. 2012.

[301]L. Britnell *et al.*, "Strong Light-Matter Interactions in Heterostructures of Atomically Thin Films," *Science*, vol. 340, no. 6138, pp. 1311–1314, Jun. 2013.

[302]R. S. Sundaram *et al.*, "Electroluminescence in Single Layer MoS2," *Nano Lett.*, vol. 13, no. 4, pp. 1416–1421, Apr. 2013.

[303]F. Schedin *et al.*, "Surface-Enhanced Raman Spectroscopy of Graphene," *ACS Nano*, vol. 4, no. 10, pp. 5617–5626, Oct. 2010.

[304]T. J. Echtermeyer *et al.*, "Strong plasmonic enhancement of photovoltage in graphene," *Nat. Commun.*, vol. 2, no. 1, Sep. 2011.

[305]F. H. L. Koppens, D. E. Chang, and F. J. García de Abajo, "Graphene Plasmonics: A Platform for Strong Light–Matter Interactions," *Nano Lett.*, vol. 11, no. 8, pp. 3370–3377, Aug. 2011.

[306]M. Jablan, H. Buljan, and M. Soljačić, "Plasmonics in graphene at infrared frequencies," *Phys. Rev. B*, vol. 80, no. 24, Dec. 2009.

[307]S. L. Cunningham, A. A. Maradudin, and R. F. Wallis, "Effect of a charge layer on the surface-plasmon-polariton dispersion curve," *Phys. Rev. B*, vol. 10, no. 8, pp. 3342–3355, Oct. 1974.

[308]V. Ryzhii, "Terahertz Plasma Waves in Gated Graphene Heterostructures," *Jpn. J. Appl. Phys.*, vol. 45, no. No. 35, pp. L923–L925, Sep. 2006.

[309]V. Ryzhii, M. Ryzhii, V. Mitin, and T. Otsuji, "Toward the creation of terahertz graphene injection laser," *J. Appl. Phys.*, vol. 110, no. 9, p. 094503, Nov. 2011.

[310]T. Holmgaard and S. I. Bozhevolnyi, "Theoretical analysis of dielectric-loaded surface plasmon-polariton waveguides," *Phys. Rev. B*, vol. 75, no. 24, Jun. 2007.

[311]S. A. Maier and H. A. Atwater, "Plasmonics: Localization and guiding of electromagnetic energy in metal/dielectric structures," *J. Appl. Phys.*, vol. 98, no. 1, p. 011101, Jul. 2005.

[312]E. W. Hill, A. Vijayaragahvan, and K. Novoselov, "Graphene Sensors," *IEEE Sens. J.*, vol. 11, no. 12, pp. 3161–3170, Dec. 2011.

[313]S. M. Avdoshenko, C. Gomes da Rocha, and G. Cuniberti, "Nanoscale ear drum: Graphene based nanoscale sensors," *Nanoscale*, vol. 4, no. 10, p. 3168, 2012.

[314]C.-L. Wong, M. Annamalai, Z.-Q. Wang, and M. Palaniapan, "Characterization of nanomechanical graphene drum structures," *J. Micromechanics Microengineering*, vol. 20, no. 11, p. 115029, Nov. 2010.

[315]Q. He, S. Wu, Z. Yin, and H. Zhang, "Graphene-based electronic sensors," *Chem. Sci.*, vol. 3, no. 6, p. 1764, 2012.

[316]Y. Liu, X. Dong, and P. Chen, "Biological and chemical sensors based on graphene materials," *Chem Soc Rev*, vol. 41, no. 6, pp. 2283–2307, 2012.

[317]..... A. Patil *et al.*, "Graphene field effect transistor as radiation sensor," 2011, pp. 455–459.

[318]G. Chen, T. M. Paronyan, and A. R. Harutyunyan, "Sub-ppt gas detection with pristine graphene," *Appl. Phys. Lett.*, vol. 101, no. 5, p. 053119, Jul. 2012.

[319]A. Eichler, J. Moser, J. Chaste, M. Zdrojek, I. Wilson-Rae, and A. Bachtold, "Nonlinear damping in mechanical resonators made from carbon nanotubes and graphene," *Nat. Nanotechnol.*, vol. 6, no. 6, pp. 339–342, Jun. 2011.

[320]J. Lin, J. Zhong, J. Reiber Kyle, M. Penchev, M. Ozkan, and C. S. Ozkan, "Molecular absorption and photodesorption in pristine and functionalized large-area graphene layers," *Nanotechnology*, vol. 22, no. 35, p. 355701, Sep. 2011.

[321]S. Pisana, P. M. Braganca, E. E. Marinero, and B. A. Gurney, "Tunable Nanoscale Graphene Magnetometers," *Nano Lett.*, vol. 10, no. 1, pp. 341–346, Jan. 2010.

[322]C.-C. Tang, M.-Y. Li, L. J. Li, C. C. Chi, and J. C. Chen, "Characteristics of a sensitive micro-Hall probe fabricated on chemical vapor deposited graphene over the temperature range from liquid-helium to room temperature," *Appl. Phys. Lett.*, vol. 99, no. 11, p. 112107, Sep. 2011.

[323]S. Pisana, P. M. Braganca, E. E. Marinero, and B. A. Gurney, "Graphene Magnetic Field Sensors," *IEEE Trans. Magn.*, vol. 46, no. 6, pp. 1910–1913, Jun. 2010.

[324]B. K. Miremadi, R. C. Singh, S. R. Morrison, and K. Colbow, "A highly sensitive and selective hydrogen gas sensor from thick oriented films of MoS2," p. 2.

[325]H. Li *et al.*, "Fabrication of Single- and Multilayer MoS2 Film-Based Field-Effect Transistors for Sensing NO at Room Temperature," *Small*, vol. 8, no. 1, pp. 63–67, Jan. 2012.

[326]Q. He *et al.*, "Fabrication of Flexible MoS2 Thin-Film Transistor Arrays for Practical Gas-Sensing Applications," *Small*, vol. 8, no. 19, pp. 2994–2999, Oct. 2012.

[327]K. Jin, L. Xie, Y. Tian, and D. Liu, "Au-Modified Monolayer MoS2 Sensor for DNA Detection," *J. Phys. Chem. C*, vol. 120, no. 20, pp. 11204–11209, May 2016.

[328]M. Winter and R. J. Brodd, "What Are Batteries, Fuel Cells, and Supercapacitors?," *Chem. Rev.*, vol. 104, no. 10, pp. 4245–4270, Oct. 2004.

[329]P. G. Bruce, B. Scrosati, and J.-M. Tarascon, "Nanomaterials for Rechargeable Lithium Batteries," *Angew. Chem. Int. Ed.*, vol. 47, no. 16, pp. 2930–2946, Apr. 2008.

[330]J. Maier, "Nanoionics: ion transport and electrochemical storage in confined systems," *Nat. Mater.*, vol. 4, no. 11, pp. 805–815, Nov. 2005.

[331]Y. Yu, L. Gu, A. Dhanabalan, C.-H. Chen, and C. Wang, "Three-dimensional porous amorphous SnO2 thin films as anodes for Li-ion batteries," *Electrochimica Acta*, vol. 54, no. 28, pp. 7227–7230, Dec. 2009.

[332]A. M. Wilson, B. M. Way, J. R. Dahn, and T. van Buuren, "Nanodispersed silicon in pregraphitic carbons," *J. Appl. Phys.*, vol. 77, no. 6, pp. 2363–2369, Mar. 1995.

[333]P. Milani *et al.*, "Synthesis and characterization of cluster-assembled carbon thin films," *J. Appl. Phys.*, vol. 82, no. 11, pp. 5793–5798, Dec. 1997.

[334]B. Lung-Hao Hu, F.-Y. Wu, C.-T. Lin, A. N. Khlobystov, and L.-J. Li, "Graphene-modified LiFePO4 cathode for lithium ion battery beyond theoretical capacity," *Nat. Commun.*, vol. 4, no. 1, Dec. 2013.

[335]S. Yang, X. Feng, S. Ivanovici, and K. Müllen, "Fabrication of Graphene-Encapsulated Oxide Nanoparticles: Towards High-Performance Anode Materials for Lithium Storage," *Angew. Chem. Int. Ed.*, vol. 49, no. 45, pp. 8408–8411, Nov. 2010.

[336]E. Yoo, J. Kim, E. Hosono, H. Zhou, T. Kudo, and I. Honma, "Large Reversible Li Storage of Graphene Nanosheet Families for Use in Rechargeable Lithium Ion Batteries," *Nano Lett.*, vol. 8, no. 8, pp. 2277–2282, Aug. 2008.

[337]S.-M. Paek, E. Yoo, and I. Honma, "Enhanced Cyclic Performance and Lithium Storage Capacity of SnO2/Graphene Nanoporous Electrodes with Three-Dimensionally Delaminated Flexible Structure," *Nano Lett.*, vol. 9, no. 1, pp. 72–75, Jan. 2009.

[338]G. Du, Z. Guo, S. Wang, R. Zeng, Z. Chen, and H. Liu, "Superior stability and high capacity of restacked molybdenum disulfide as anode material for lithium ion batteries," *Chem Commun*, vol. 46, no. 7, pp. 1106–1108, 2010.

[339]K. Chang and W. Chen, "Cysteine-Assisted Synthesis of Layered MoS2/Graphene Composites with Excellent Electrochemical Performances for Lithium Ion Batteries," *ACS Nano*, vol. 5, no. 6, pp. 4720–4728, Jun. 2011.

[340]M. D. Stoller *et al.*, "Interfacial capacitance of single layer graphene," *Energy Environ. Sci.*, vol. 4, no. 11, p. 4685, 2011.

[341]L. Yuan *et al.*, "Flexible Solid-State Supercapacitors Based on Carbon Nanoparticles/MnO2 Nanorods Hybrid Structure," *ACS Nano*, vol. 6, no. 1, pp. 656–661, Jan. 2012.

[342]T. Y. Kim *et al.*, "High-Performance Supercapacitors Based on Poly(ionic liquid)-Modified Graphene Electrodes," *ACS Nano*, vol. 5, no. 1, pp. 436–442, Jan. 2011.

[343]Y. Zhu *et al.*, "Carbon-Based Supercapacitors Produced by Activation of Graphene," *Science*, vol. 332, no. 6037, pp. 1537–1541, Jun. 2011.

[344]T. Kim, G. Jung, S. Yoo, K. S. Suh, and R. S. Ruoff, "Activated Graphene-Based Carbons as Supercapacitor Electrodes with Macro- and Mesopores," *ACS Nano*, vol. 7, no. 8, pp. 6899–6905, Aug. 2013.

[345]L. L. Zhang *et al.*, "Highly Conductive and Porous Activated Reduced Graphene Oxide Films for High-Power Supercapacitors," *Nano Lett.*, vol. 12, no. 4, pp. 1806–1812, Apr. 2012.

[346]X. Yang, C. Cheng, Y. Wang, L. Qiu, and D. Li, "Liquid-Mediated Dense Integration of Graphene Materials for Compact Capacitive Energy Storage," *Science*, vol. 341, no. 6145, pp. 534–537, Aug. 2013.

[347]I.-Y. Jeon *et al.*, "Facile, scalable synthesis of edge-halogenated graphene nanoplatelets as efficient metal-free eletrocatalysts for oxygen reduction reaction," *Sci. Rep.*, vol. 3, no. 1, Dec. 2013.

[348]H.-J. Choi, S.-M. Jung, J.-M. Seo, D. W. Chang, L. Dai, and J.-B. Baek, "Graphene for energy conversion and storage in fuel cells and supercapacitors," *Nano Energy*, vol. 1, no. 4, pp. 534–551, Jul. 2012.

[349]J. Yang and H. S. Shin, "Recent advances in layered transition metal dichalcogenides for hydrogen evolution reaction," *J Mater Chem A*, vol. 2, no. 17, pp. 5979–5985, 2014.

[350]F. Bonaccorso *et al.*, "Graphene, related two-dimensional crystals, and hybrid systems for energy conversion and storage," *Science*, vol. 347, no. 6217, pp. 1246501–1246501, Jan. 2015.

[351]V. Tozzini and V. Pellegrini, "Prospects for hydrogen storage in graphene," *Phys Chem Chem Phys*, vol. 15, no. 1, pp. 80–89, 2013.

[352]M. Ni, M. K. H. Leung, D. Y. C. Leung, and K. Sumathy, "A review and recent developments in photocatalytic water-splitting using TiO2 for hydrogen production," *Renew. Sustain. Energy Rev.*, vol. 11, no. 3, pp. 401–425, Apr. 2007.

[353]Z. Zou, J. Ye, K. Sayama, and H. Arakawa, "Direct splitting of water under visible light irradiation with an oxide semiconductor photocatalyst," *Nature*, vol. 414, no. 6864, pp. 625–627, Dec. 2001.

[354]A. Nathan *et al.*, "Flexible Electronics: The Next Ubiquitous Platform," *Proc. IEEE*, vol. 100, no. Special Centennial Issue, pp. 1486–1517, May 2012.

[355]K.-Y. Shin, J.-Y. Hong, and J. Jang, "Flexible and transparent graphene films as acoustic actuator electrodes using inkjet printing," *Chem. Commun.*, vol. 47, no. 30, p. 8527, 2011.

[356]I. Lahiri, V. P. Verma, and W. Choi, "An all-graphene based transparent and flexible field emission device," *Carbon*, vol. 49, no. 5, pp. 1614–1619, Apr. 2011.

[357]S. Kim *et al.*, "Low-Power Flexible Organic Light-Emitting Diode Display Device," *Adv. Mater.*, vol. 23, no. 31, pp. 3511–3516, Aug. 2011.

[358]L. Huang, Y. Huang, J. Liang, X. Wan, and Y. Chen, "Graphene-based conducting inks for direct inkjet printing of flexible conductive patterns and their applications in electric circuits and chemical sensors," *Nano Res.*, vol. 4, no. 7, pp. 675–684, Jul. 2011.

[359]J. Yi, J. M. Lee, and W. I. Park, "Vertically aligned ZnO nanorods and graphene hybrid architectures for high-sensitive flexible gas sensors," *Sens. Actuators B Chem.*, vol. 155, no. 1, pp. 264–269, Jul. 2011.

[360]Y. Wang *et al.*, "Super-Elastic Graphene Ripples for Flexible Strain Sensors," *ACS Nano*, vol. 5, no. 5, pp. 3645–3650, May 2011.

[361]D. Wei *et al.*, "Flexible solid state lithium batteries based on graphene inks," *J. Mater. Chem.*, vol. 21, no. 26, p. 9762, 2011.

[362]G. Zhou, F. Li, and H.-M. Cheng, "Progress in flexible lithium batteries and future prospects," *Energy Env. Sci*, vol. 7, no. 4, pp. 1307–1338, 2014.

[363]Y. Hu and X. Sun, "Flexible rechargeable lithium ion batteries: advances and challenges in materials and process technologies," *J Mater Chem A*, vol. 2, no. 28, pp. 10712–10738, 2014.

[364]X. Wang and G. Shi, "Flexible graphene devices related to energy conversion and storage," *Energy Environ. Sci.*, vol. 8, no. 3, pp. 790–823, 2015.

[365]I. Surjati and Y. KN, "Increasing Bandwidth Dual Frequency Triangular Microstrip Antenna For WiMAX Application," vol. 10, no. 06, p. 5, 2010.

[366]S. Bae, S. J. Kim, D. Shin, J.-H. Ahn, and B. H. Hong, "Towards industrial applications of graphene electrodes," *Phys. Scr.*, vol. T146, p. 014024, Jan. 2012.

[367]M. W. Rowell and M. D. McGehee, "Transparent electrode requirements for thin film solar cell modules," *Energy Env. Sci*, vol. 4, no. 1, pp. 131–134, 2011.

[368]F. Bonaccorso, Z. Sun, T. Hasan, and A. C. Ferrari, "Graphene photonics and optoelectronics," *Nat. Photonics*, vol. 4, no. 9, pp. 611–622, Sep. 2010.

[369]U. Kim *et al.*, "A transparent and stretchable graphene-based actuator for tactile display," *Nanotechnology*, vol. 24, no. 14, p. 145501, Apr. 2013.

[370]J. Lee *et al.*, "High-Performance Current Saturating Graphene Field-Effect Transistor With Hexagonal Boron Nitride Dielectric on Flexible Polymeric Substrates," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 172–174, Feb. 2013.

[371]K. S. Novoselov *et al.*, "Two-dimensional atomic crystals," *Proc. Natl. Acad. Sci. U. S. A.*, vol. 102, no. 30, pp. 10451–10453, 2005.

[372]E. Gao, S.-Z. Lin, Z. Qin, M. J. Buehler, X.-Q. Feng, and Z. Xu, "Mechanical exfoliation of two-dimensional materials," *J. Mech. Phys. Solids*, vol. 115, pp. 248–262, Jun. 2018.

[373]M. Yi and Z. Shen, "A review on mechanical exfoliation for the scalable production of graphene," *J. Mater. Chem. A*, vol. 3, no. 22, pp. 11700–11715, 2015.

[374]A. Martinez, K. Fuse, and S. Yamashita, "Mechanical exfoliation of graphene for the passive mode-locking of fiber lasers," *Appl. Phys. Lett.*, vol. 99, no. 12, p. 121107, Sep. 2011.

[375]A. J. Mannix, B. Kiraly, M. C. Hersam, and N. P. Guisinger, "Synthesis and chemistry of elemental 2D materials," *Nat. Rev. Chem.*, vol. 1, no. 2, p. 0014, Jan. 2017.

[376]A. Kis and A. Ferrari, "Deliverable 1.4 'Report on growth and modelling of TMDs,'" p. 14, 2016.

[377]S. A. Ansari, H. Fouad, S. G. Ansari, M. P. Sk, and M. H. Cho, "Mechanically exfoliated MoS 2 sheet coupled with conductive polyaniline as a superior supercapacitor electrode material," *J. Colloid Interface Sci.*, vol. 504, pp. 276–282, Oct. 2017.

[378]C. R. Dean *et al.*, "Boron nitride substrates for high-quality graphene electronics," *Nat. Nanotechnol.*, vol. 5, no. 10, pp. 722–726, Oct. 2010.

[379]L. H. Li, Y. Chen, G. Behan, H. Zhang, M. Petravic, and A. M. Glushenkov, "Large-scale mechanical peeling of boron nitride nanosheets by low-energy ball milling," *J. Mater. Chem.*, vol. 21, no. 32, p. 11862, 2011.

[380]A. K. Geim, "Graphene: Status and Prospects," *Science*, vol. 324, no. 5934, pp. 1530–1534, Jun. 2009.

[381]P. Neugebauer, M. Orlita, C. Faugeras, A.-L. Barra, and M. Potemski, "How Perfect Can Graphene Be?," *Phys. Rev. Lett.*, vol. 103, no. 13, Sep. 2009.

[382]GLAB, *Laboratory for Graphene, other 2D materials and ordered nanostructures*. [Online]. Available: http://www.graphene.ac.rs.

[383]M. Lotya *et al.*, "Liquid Phase Production of Graphene by Exfoliation of Graphite in Surfactant/Water Solutions," *J. Am. Chem. Soc.*, vol. 131, no. 10, pp. 3611–3620, Mar. 2009.

[384]M. Lotya, P. J. King, U. Khan, S. De, and J. N. Coleman, "High-Concentration, Surfactant-Stabilized Graphene Dispersions," *ACS Nano*, vol. 4, no. 6, pp. 3155–3162, Jun. 2010.

[385]H. Choi, H. Kim, S. Hwang, W. Choi, and M. Jeon, "Dye-sensitized solar cells using graphene-based carbon nano composite as counter electrode," *Sol. Energy Mater. Sol. Cells*, vol. 95, no. 1, pp. 323–325, Jan. 2011.

[386]D. Li, M. B. Müller, S. Gilje, R. B. Kaner, and G. G. Wallace, "Processable aqueous dispersions of graphene nanosheets," *Nat. Nanotechnol.*, vol. 3, no. 2, pp. 101–105, Feb. 2008.

[387]F. Torrisi *et al.*, "Inkjet-Printed Graphene Electronics," *ACS Nano*, vol. 6, no. 4, pp. 2992–3006, Apr. 2012.

[388]U. Khan, A. O'Neill, M. Lotya, S. De, and J. N. Coleman, "High-Concentration Solvent Exfoliation of Graphene," *Small*, vol. 6, no. 7, pp. 864–871, Apr. 2010.

[389]T. Hasan *et al.*, "Solution-phase exfoliation of graphite for ultrafast photonics," *Phys. Status Solidi B*, vol. 247, no. 11–12, pp. 2953–2957, Dec. 2010.

[390]M. Chhowalla, H. S. Shin, G. Eda, L.-J. Li, K. P. Loh, and H. Zhang, "The chemistry of two-dimensional layered transition metal dichalcogenide nanosheets," *Nat. Chem.*, vol. 5, no. 4, pp. 263–275, Apr. 2013.

[391]J. Shen *et al.*, "Liquid Phase Exfoliation of Two-Dimensional Materials by Directly Probing and Matching Surface Tension Components," *Nano Lett.*, vol. 15, no. 8, pp. 5449–5454, Aug. 2015.

[392]J. N. Coleman *et al.*, "Two-Dimensional Nanosheets Produced by Liquid Exfoliation of Layered Materials," *Science*, vol. 331, no. 6017, pp. 568–571, Feb. 2011.

[393]V. Umansky, M. Heiblum, Y. Levinson, J. Smet, J. Nübler, and M. Dolev, "MBE growth of ultra-low disorder 2DEG with mobility exceeding 35×106cm2/Vs," *J. Cryst. Growth*, vol. 311, no. 7, pp. 1658–1661, Mar. 2009.

[394]M. Jungo, F. M. di Sopra, D. Erni, and W. Baechtold, "Scaling effects on vertical-cavity surface-emitting lasers static and dynamic behavior," *J. Appl. Phys.*, vol. 91, no. 9, pp. 5550–5557, May 2002.

[395]S. Bae *et al.*, "Roll-to-roll production of 30-inch graphene films for transparent electrodes," *Nat. Nanotechnol.*, vol. 5, no. 8, pp. 574–578, Aug. 2010.

[396]J. M. Garcia *et al.*, "Graphene growth on h-BN by molecular beam epitaxy," *Solid State Commun.*, vol. 152, no. 12, pp. 975–978, Jun. 2012.

[397]J. Hackley, D. Ali, J. DiPasquale, J. D. Demaree, and C. J. K. Richardson, "Graphitic carbon growth on Si(111) using solid source molecular beam epitaxy," *Appl. Phys. Lett.*, vol. 95, no. 13, p. 133114, Sep. 2009.

[398]E. Moreau *et al.*, "Graphene growth by molecular beam epitaxy on the carbon-face of SiC," *Appl. Phys. Lett.*, vol. 97, no. 24, p. 241907, Dec. 2010.

[399]U. Wurstbauer *et al.*, "Molecular beam growth of graphene nanocrystals on dielectric substrates," *Carbon*, vol. 50, no. 13, pp. 4822–4829, Nov. 2012.

[400]M. K. Cheng *et al.*, "Large-area epitaxial growth of MoSe2 via an incandescent molybdenum source," *Nanotechnology*, vol. 28, no. 45, p. 455601, Nov. 2017.

[401]L. Jiao *et al.*, "Molecular-beam epitaxy of monolayer MoSe2 : growth characteristics and domain boundary formation," *New J. Phys.*, vol. 17, no. 5, p. 053023, May 2015.

[402]S. Vishwanath *et al.*, "Comprehensive structural and optical characterization of MBE grown MoSe2 on graphite, CaF2 and graphene," *2D Mater.*, vol. 2, no. 2, p. 024007, May 2015.

[403]R. Yue *et al.*, "Nucleation and growth of WSe2 : enabling large grain transition metal dichalcogenides," *2D Mater.*, vol. 4, no. 4, p. 045019, Sep. 2017.

[404]H. C. Diaz, R. Chaghi, Y. Ma, and M. Batzill, "Molecular beam epitaxy of the van der Waals heterostructure MoTe2 on MoS2 : phase, thermal, and chemical stability," *2D Mater.*, vol. 2, no. 4, p. 044010, Nov. 2015.

[405]L. A. Walsh *et al.*, "WTe2 thin films grown by beam-interrupted molecular beam epitaxy," *2D Mater.*, vol. 4, no. 2, p. 025044, Mar. 2017.

[406]A. Summerfield *et al.*, "Moiré-Modulated Conductance of Hexagonal Boron Nitride Tunnel Barriers," *Nano Lett.*, vol. 18, no. 7, pp. 4241–4246, Jul. 2018.

[407]S. Novikov *et al.*, "High-temperature molecular beam epitaxy of hexagonal boron nitride layers (Conference Presentation)," 2018, p. 17.

[408]Univ. Cambridge, "University of Cambridge, MBE setup in the Department of Physics." [Online]. Available: https://www.phy.cam.ac.uk/research/research-groups/sp/facilities/mbe.

[409]J. Zhuang, X. Xu, G. Peleckis, W. Hao, S. X. Dou, and Y. Du, "Silicene: A Promising Anode for Lithium-Ion Batteries," *Adv. Mater.*, vol. 29, no. 48, p. 1606716, Dec. 2017.

[410]C. Grazianetti, D. Chiappe, E. Cinquanta, G. Tallarida, M. Fanciulli, and A. Molle, "Exploring the morphological and electronic properties of silicene superstructures," *Appl. Surf. Sci.*, vol. 291, pp. 109–112, Feb. 2014.

[411]A. Molle *et al.*, "Hindering the Oxidation of Silicene with Non-Reactive Encapsulation," *Adv. Funct. Mater.*, vol. 23, no. 35, pp. 4340–4344, Sep. 2013.

[412]F. d'Acapito *et al.*, "Evidence for Germanene growth on epitaxial hexagonal (h)-AlN on Ag(1 1 1)," *J. Phys. Condens. Matter*, vol. 28, no. 4, p. 045002, Feb. 2016.

[413]W. Kern and G. L. Schnable, "Low-pressure chemical vapor deposition for very large-scale integration processing—A review," *IEEE Trans. Electron Devices*, vol. 26, no. 4, pp. 647–657, Apr. 1979.

[414]X. Li *et al.*, "Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils," *Science*, vol. 324, no. 5932, pp. 1312–1314, Jun. 2009.

[415]X. Li *et al.*, "Graphene Films with Large Domain Size by a Two-Step Chemical Vapor Deposition Process," *Nano Lett.*, vol. 10, no. 11, pp. 4328–4334, Nov. 2010.

[416]N. Petrone *et al.*, "Chemical Vapor Deposition-Derived Graphene with Electrical Performance of Exfoliated Graphene," *Nano Lett.*, vol. 12, no. 6, pp. 2751–2756, Jun. 2012.

[417]Z. Yan *et al.*, "Toward the Synthesis of Wafer-Scale Single-Crystal Graphene on Copper Foils," *ACS Nano*, vol. 6, no. 10, pp. 9110–9117, Oct. 2012.

[418]Y. Hao *et al.*, "The Role of Surface Oxygen in the Growth of Large Single-Crystal Graphene on Copper," *Science*, vol. 342, no. 6159, pp. 720–723, Nov. 2013.

[419]K.-K. Liu *et al.*, "Growth of Large-Area and Highly Crystalline MoS2 Thin Layers on Insulating Substrates," *Nano Lett.*, vol. 12, no. 3, pp. 1538–1544, Mar. 2012.

[420]L. Zhou *et al.*, "Role of Molecular Sieves in the CVD Synthesis of Large-Area 2D MoTe2," *Adv. Funct. Mater.*, vol. 27, no. 3, p. 1603491, Jan. 2017.

[421]S. Li *et al.*, "Halide-assisted atmospheric pressure growth of large WSe2 and WS2 monolayer crystals," *Appl. Mater. Today*, vol. 1, no. 1, pp. 60–66, Nov. 2015.

[422]N. D. Boscher, C. J. Carmalt, and I. P. Parkin, "Atmospheric pressure chemical vapor deposition of WSe2 thin films on glass—highly hydrophobic sticky surfaces," *J Mater Chem*, vol. 16, no. 1, pp. 122–127, 2006.

[423]E. Zhang *et al.*, "Tunable Positive to Negative Magnetoresistance in Atomically Thin WTe2," *Nano Lett.*, vol. 17, no. 2, pp. 878–885, Feb. 2017.

[424]N. K. Perkgoz and M. Bay, "Investigation of Single-Wall MoS2 Monolayer Flakes Grown by Chemical Vapor Deposition," *Nano-Micro Lett.*, vol. 8, no. 1, pp. 70–79, Jan. 2016.

[425]D. V. Badami, "X-Ray studies of graphite formed by decomposing silicon carbide," *Carbon*, vol. 3, no. 1, pp. 53–57, Jul. 1965.

[426]A. J. Van Bommel, J. E. Crombeen, and A. Van Tooren, "LEED and Auger electron observations of the SiC(0001) surface," *Surf. Sci.*, vol. 48, no. 2, pp. 463–472, Mar. 1975.

[427]C. Berger *et al.*, "Ultrathin Epitaxial Graphite: 2D Electron Gas Properties and a Route toward Graphene-based Nanoelectronics," *J. Phys. Chem. B*, vol. 108, no. 52, pp. 19912–19916, Dec. 2004.

[428]H. Hibino, H. Kageshima, F. Maeda, M. Nagase, Y. Kobayashi, and H. Yamaguchi, "Microscopic thickness determination of thin graphite films formed on SiC from quantized oscillation in reflectivity of low-energy electrons," *Phys. Rev. B*, vol. 77, no. 7, Feb. 2008.

[429]J. Hass *et al.*, "Highly ordered graphene for two dimensional electronics," *Appl. Phys. Lett.*, vol. 89, no. 14, p. 143106, Oct. 2006.

[430]K. V. Emtsev *et al.*, "Towards wafer-size graphene layers by atmospheric pressure graphitization of silicon carbide," *Nat. Mater.*, vol. 8, no. 3, pp. 203–207, Mar. 2009.

[431]E. Pallecchi *et al.*, "High Electron Mobility in Epitaxial Graphene on 4H-SiC(0001) via post-growth annealing under hydrogen," *Sci. Rep.*, vol. 4, no. 1, May 2015.

[432]D. Pierucci *et al.*, "Atomic and electronic structure of trilayer graphene/SiC(0001): Evidence of Strong Dependence on Stacking Sequence and charge transfer," *Sci. Rep.*, vol. 6, no. 1, Dec. 2016.

[433]G. R. Yazdi, R. Vasiliauskas, T. Iakimov, A. Zakharov, M. Syväjärvi, and R. Yakimova, "Growth of large area monolayer graphene on 3C-SiC and a comparison with other SiC polytypes," *Carbon*, vol. 57, pp. 477–484, Jun. 2013.

[434]N. Mishra, J. Boeckl, N. Motta, and F. Iacopi, "Graphene growth on silicon carbide: A review: Graphene growth on silicon carbide," *Phys. Status Solidi A*, vol. 213, no. 9, pp. 2277–2289, Sep. 2016.

[435]M. Suemitsu, Y. Miyamoto, H. Handa, and A. Konno, "Graphene Formation on a 3C-SiC(111) Thin Film Grown on Si(110) Substrate," *E-J. Surf. Sci. Nanotechnol.*, vol. 7, pp. 311–313, 2009.

[436]A. Ouerghi *et al.*, "Epitaxial graphene on 3C-SiC(111) pseudosubstrate: Structural and electronic properties," *Phys. Rev. B*, vol. 82, no. 12, Sep. 2010.

[437]B. Gupta *et al.*, "Effect of substrate polishing on the growth of graphene on 3C–SiC(111)/Si(111) by high temperature annealing," *Nanotechnology*, vol. 27, no. 18, p. 185601, May 2016.

[438]A. Ouerghi *et al.*, "Epitaxial graphene on cubic SiC(111)/Si(111) substrate," *Appl. Phys. Lett.*, vol. 96, no. 19, p. 191910, May 2010.

[439]M. Suemitsu and H. Fukidome, "Epitaxial graphene on silicon substrates," *J. Phys. Appl. Phys.*, vol. 43, no. 37, p. 374012, Sep. 2010.

[440]Y. Hu *et al.*, "Structured epitaxial graphene: growth and properties," *J. Phys. Appl. Phys.*, vol. 45, no. 15, p. 154010, Apr. 2012.

[441]Z. Peng, Z. Yan, Z. Sun, and J. M. Tour, "Direct Growth of Bilayer Graphene on SiO2 Substrates by Carbon Diffusion through Nickel," *ACS Nano*, vol. 5, no. 10, pp. 8241–8247, Oct. 2011.

[442]B. N. Finkelstein and G. E. Horowitz, "Uber die Energie des He-Atoms und des positiven H2-Ions im Normalzustande," *Z. Phys.*, vol. 48, no. 1–2, pp. 118–122, Jan. 1928.

[443]J. C. Slater and G. F. Koster, "Simplified LCAO method for the periodic potential problem," *Phys. Rev.*, vol. 94, no. 6, p. 1498, 1954.

[444]O. K. Andersen and O. Jepsen, "Explicit, first-principles tight-binding theory," *Phys. Rev. Lett.*, vol. 53, no. 27, p. 2571, 1984.

[445]C. M. Goringe, C. R. Bowler, and E. Hernandez, "Tight-binding modelling of materials," *Rep. Prog. Phys.*, no. 60, pp. 1447–1512, 1997.

[446]D. A. Papaconstantopoulos and M. J. Mehl, "The Slater–Koster tight-binding method: a computationally efficient and accurate approach," *J. Phys. Condens. Matter*, no. 15, pp. 413–440, 2003.

[447]..... W. A. Harrison, "Tight-binding methods," *Surf. Sci.*, vol. 299, pp. 298–310, 1994.

[448]Y. M. Niquet, D. Rideau, C. Tavernier, H. Jaouen, and X. Blase, "Onsite matrix elements of the tight-binding Hamiltonian of a strained crystal: Application to silicon, germanium, and their alloys," *Phys. Rev. B*, vol. 79, no. 24, Jun. 2009.

[449]N. H. Quang, N. T. Truc, and Y.-M. Niquet, "Tight-binding versus effective mass approximation calculation of electronic structures of semiconductor nanocrystals and nanowires," *Comput. Mater. Sci.*, vol. 44, no. 1, pp. 21–25, Nov. 2008.

[450]S. Fang, R. Kuate Defo, S. N. Shirodkar, S. Lieu, G. A. Tritsaris, and E. Kaxiras, "Ab initio tight-binding Hamiltonian for transition metal dichalcogenides," *Phys. Rev. B*, vol. 92, no. 20, p. 205108, Nov. 2015.

[451]S. Datta, "The non-equilibrium Green's function (NEGF) formalism: An elementary introduction," in *Electron Devices Meeting, 2002. IEDM'02. International*, 2002, pp. 703–706.

[452]S. Datta, *Quantum Transport Atom to Transistor*. Cambridge: Cambridge University Press, 2013.

[453]S. Datta, *Electronic transport in mesoscopic systems*, 1. paperback ed. (with corr.), 8. print. Cambridge: Cambridge Univ. Press, 2009.

[454]D. K. Ferry, S. M. Goodnick, and J. P. Bird, *Transport in nanostructures*, 2nd ed. Cambridge, UK ; New York: Cambridge University Press, 2009.

[455]V. H. Nguyen, "Transport electronic et effets de spins dans les nanostructures de graphene," Universite Paris-Sud XI, IEF, 2010.

[456]M. C. Nguyen, "Theoretical study of electronic and thermoelectric nanodevicesbased on strained graphene junctions," Universite Paris-Sud XI, IEF, 2016.

[457]M. P. Anantram, M. S. Lundstrom, and D. E. Nikonov, "Modeling of Nanoscale Devices," *Proc. IEEE*, vol. 96, no. 9, pp. 1511–1550, Sep. 2008.

[458]M. P. Lopez Sancho, J. M. Lopez Sancho, and J. Rubio, "Quick iterative scheme for the calculation of transfer matrices: application to MO(100)," *J. Phys. F*, no. 14, pp. 1205–1215, 1984.

[459]R. Lake, G. Klimeck, R. C. Bowen, and D. Jovanovic, "Single and multiband modeling of quantum electron transport through layered semiconductor devices," *J. Appl. Phys.*, vol. 81, no. 12, pp. 7845–7869, Jun. 1997.

[460]..... J. Schueler, "Green's Functions and Their Applications to Quantum Mechanics," 2011.

[461]Y. Yoon, K. Ganapathi, and S. Salahuddin, "How Good Can Monolayer MoS2 Transistors Be?," *Nano Lett.*, vol. 11, no. 9, pp. 3768–3773, Sep. 2011.

[462]Z. Jin, X. Li, J. T. Mullen, and K. W. Kim, "Intrinsic transport properties of electrons and holes in monolayer transition-metal dichalcogenides," *Phys. Rev. B*, vol. 90, no. 4, p. 045422, Jul. 2014.

[463]K. Kaasbjerg, K. S. Thygesen, and K. W. Jacobsen, "Phonon-limited mobility in n -type single-layer MoS 2 from first principles," *Phys. Rev. B*, vol. 85, no. 11, p. 115317, Mar. 2012.

[464]K. Kaasbjerg, K. S. Thygesen, and A.-P. Jauho, "Acoustic phonon limited mobility in two-dimensional semiconductors: Deformation potential and piezoelectric scattering in monolayer MoS 2 from first principles," *Phys. Rev. B*, vol. 87, no. 23, p. 235312, Jun. 2013.

[465]C. Zhang *et al.*, "Strain distributions and their influence on electronic structures of WSe2–MoS2 laterally strained heterojunctions," *Nat. Nanotechnol.*, vol. 13, no. 2, pp. 152–158, Feb. 2018.

[466]H. Carrillo-Nunez, R. Rhyner, M. Luisier, and A. Schenk, "Effect of surface roughness and phonon scattering on extremely narrow InAs-Si Nanowire TFETs," in *2016 46th European Solid-State Device Research Conference (ESSDERC)*, Lausanne, Switzerland, 2016, pp. 188–191.

[467]M. G. Pala, C. Grillet, J. Cao, D. Logoteta, A. Cresti, and D. Esseni, "Impact of inelastic phonon scattering in the OFF state of Tunnel-field-effect transistors," *J. Comput. Electron.*, vol. 15, no. 4, pp. 1240–1247, Dec. 2016.

List of publications and conferences

Publications

J. Choukroun, M. Pala, S. Fang, E. Kaxiras, and P. Dollfus *"High performance WTe_2-MoS_2 in-plane heterojunction Tunnel Field Effect Transistors"*, 2018 48th European Solid-State Device Research Conference, 10.1109/ESSDERC.2018.8486869 *IEEE Proceedings* ***(2018)***

J. Choukroun, M. Pala, S. Fang, E. Kaxiras, and P. Dollfus *"High performance Tunnel Field Effect Transistors based on in-plane transition metal dichalcogenide heterojunctions"*, 10.1088/1361-6528/aae7df, *to appear in Nanotechnology* ***(2018)***

J. Choukroun, M. Pala and P. Dollfus *"Ungated-channel architecture for high performance Tunnel Field Effect Transistors based on 2D material heterostructures"*, ***to be submitted***

International conferences

J. Choukroun, M. Pala, J. Saint-Martin, and P. Dollfus *"Atomistic simulation of electronic transport in planar graphene-MoS_2 heterostructure devices"*, GDR Graphene and co 2017 - Aussois, France **(2017)**

J. Choukroun, M. Pala, S. Fang, E. Kaxiras, and P. Dollfus *"High performance WTe_2-MoS_2 in-plane heterojunction Tunnel Field Effect Transistors"*, ESSDERC 2018 - Dresden, Germany **(2018)**

J. Choukroun, M. Pala, S. Fang, E. Kaxiras, and P. Dollfus *"Quantum simulation of high performance Tunnel Field Effect Transistors based on 2D material in-plane heterojunctions"*, 6th International Symposium on Graphene Devices, ISGD-6 - St Petersburg, Russia **(2018)**

université PARIS-SACLAY
ÉCOLE DOCTORALE
Physique et ingénierie : électrons, photons, sciences du vivant (EOBE)

Titre : Etude théorique d'hétérojonctions planaires de dichalcogénures de métaux de transition et de leurs applications dans le cadre de transistors ultra-basse consommation

Mots clés : TFET, transistor, matériaux 2D, TMD, simulation quantique

La miniaturisation des MOSFET a permis une forte diminution des transistors et des puces, ainsi qu'une augmentation exponentielle des capacités de calcul. Cette miniaturisation ne peut néanmoins continuer ainsi: de nos jours, un microprocesseur peut contenir des dizaines de milliards de transistors et la chaleur dégagée par ces composants peut fortement détériorer ses performances. De plus, du fait de leur principe même de fonctionnement, la tension d'alimentation des MOSFET ne peut être réduite sans en impacter les performances. De nouvelles architectures telles que le TFET -basé sur l'effet tunnel bande-à-bande et pouvant fonctionner à des tensions d'alimentation très basses- ainsi que de nouveaux matériaux pourraient donc apporter une alternative au MOSFET silicium. Les monocouches de dichalcogènures de métaux de transitions (TMDs) -des semiconducteurs à bande interdite directe d'environ 1 à 2 eV- possèdent un fort potentiel pour l'électronique et la photonique. De plus, dans le cas de contraintes appropriées, ils peuvent conduire un alignement de bandes présentant un broken-gap; cette configuration permet de surpasser les limites habituelles du TFETs, à savoir de faibles courants dus à l'effet tunnel sur lequel ces dispositifs reposent.

Dans ce travail de thèse, des hétérojonctions planaires de TMD sont modélisées via une approche atomistique de liaisons fortes, et une configuration broken-gap est observée dans deux d'entre elles ($MoTe_2/MoS_2$ et WTe_2/MoS_2). Leur potentiel dans le cadre de transistors à effet tunnel (TFETs) est évalué au moyen de simulations de transport quantique basées sur un modèle TB atomistique ainsi que la théorie des fonctions de Green hors-équilibre. Des TFETs type-n basés sur ces hétérojonctions sont simulés et présentent des courants ON élevés ($I_{ON} > 10^3$ µA/µm) ainsi que des pentes sous-seuil extrêmement raides ($SS < 5$ mV/dec) à des tensions d'alimentation très faibles ($V_{DD} = 0.3$ V). Plusieurs architectures novatrices basées sur ces TFETs et découlant de la nature 2D des matériaux utilisés sont également présentées, et permettent d'atteindre des performances encore plus élevées.

université PARIS-SACLAY
ÉCOLE DOCTORALE
Physique et ingénierie : électrons, photons, sciences du vivant (EOBE)

Title : Theoretical study of in-plane heterojunctions of transition metal dichalcogenides and their applications for low-power transistors.

Keywords : TFET, transistor, 2D materials, TMDs, quantum simulation

Abstract : Nowadays, microprocessors can contain tens of billions of transistors and as a result, heat dissipation and its impact on device performance has increasingly become a hindrance to further scaling. Due to their working mechanism, the power supply of MOSFETs cannot be reduced without deteriorating overall performance, and Si-MOSFETs scaling therefore seems to be reaching its end. New architectures such as the TFET, which can perform at low supply voltages thanks to its reliance on band-to-band tunneling, and new materials could solve this issue. Transition metal dichalcogenide monolayers (TMDs) are 2D semiconductors with direct band gaps ranging from 1 to 2 eV, and therefore hold potential in electronics and photonics. Moreover, when under appropriate strains, their band alignment can result in broken-gap configurations which can circumvent the traditionally low currents observed in TFETs due to the tunneling mechanism they rely upon.

In this work, in-plane TMD heterojunctions are investigated using an atomistic tight-binding approach, two of which lead to a broken-gap configuration ($MoTe_2/MoS_2$ and WTe_2/MoS_2). The potential of these heterojunctions for use in tunnel field-effect transistors (TFETs) is evaluated via quantum transport computations based on an atomistic tight-binding model and the non-equilibrium Green's function theory.

N-type TFETs based on these in-plane TMD heterojunctions are shown to yield high ON currents ($I_{ON} > 10^3$ µA/µm) and extremely low subthreshold swings ($SS < 5$ mV/dec) at low supply voltages ($V_{DD} = 0.3$ V). Innovative device architectures allowed by the 2D nature of these materials are also proposed, and shown to enhance performance even further.

Université Paris-Saclay
Espace Technologique / Immeuble Discovery
Route de l'Orme aux Merisiers RD 128 / 91190 Saint-Aubin, France