



HAL
open science

Design of embedded sinusoidal signal generators for mixed signal Built-in Self-Test

Hani Malloug

► **To cite this version:**

Hani Malloug. Design of embedded sinusoidal signal generators for mixed signal Built-in Self-Test. Micro and nanotechnologies/Microelectronics. Université Grenoble Alpes, 2018. English. NNT : 2018GREAT069 . tel-01997892

HAL Id: tel-01997892

<https://theses.hal.science/tel-01997892>

Submitted on 29 Jan 2019

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

THÈSE

Pour obtenir le grade de

DOCTEUR DE LA COMMUNAUTÉ UNIVERSITÉ GRENOBLE ALPES

Spécialité : NANO ELECTRONIQUE ET NANO TECHNOLOGIES

Arrêté ministériel : 25 mai 2016

Présentée par

Hani MALLOUG

Thèse dirigée par **Salvador MIR**, Directeur de recherche
et codirigée par **Manuel J. BARRAGAN**

préparée au sein du **Laboratoire Techniques de l'Informatique
et de la Microélectronique pour l'Architecture des systèmes
intégrés**

dans l'**École Doctorale Electronique, Electrotechnique,
Automatique, Traitement du Signal (EEATS)**

Conception de générateurs sinusoïdaux embarqués pour l'auto-test des circuits mixtes

Design of embedded sinusoidal signal generators for mixed signal Built-in Self-Test

Thèse soutenue publiquement le **28 septembre 2018**,
devant le jury composé de :

Monsieur Dominique DALLET

Professeur, Bordeaux INP, Président du jury

Madame Marie-Minerve LOUËRAT

Chargé de Recherche, CNRS délégation Paris, Rapporteur

Monsieur Serge BERNARD

Directeur de Recherche, CNRS délégation Languedoc-Roussillon,
Rapporteur

Monsieur Florian CACHO

Ingénieur senior, STMicroelectronics Crolles, Examineur

Monsieur Salvador MIR

Directeur de Recherche, CNRS délégation Alpes, Directeur de thèse

Monsieur Manuel J. BARRAGAN

Chargé de Recherche, CNRS - TIMA, Co-Encadrant



To my family...

Acknowledgments

I wish to express my sincere appreciation to those who have contributed to this thesis and supported me in one way or the other during this amazing journey.

First of all, I would like to express my sincere gratitude to my advisors Salvador MIR and Manuel J. BARRAGAN for the continuous support during my PhD study, for their patience, motivation, and immense knowledge. I could not have imagined having better advisors and mentors for my PhD study.

Besides my advisors, I would like to thank all the members of the jury for their participation in this thesis committee: Prof. Dominique DALLET from Bordeaux INP-IMS, Dr. Marie-Minerve LOUËRAT from CNRS-LIP6, Dr. Serge BERNARD from CNRS-LIRMM and Mr. Florian CACHO senior engineer at STMicroelectronics-Crolles.

Special thanks should be also directed to the Reliable Mixed-signal Systems (RMS) team leader Prof. Emmanuel SIMEU, my office colleagues and close friends Rshdee ALHAKIM and Ghislan Takam TCHANDOU and all RMS team students (Renato, Athanasios, Martin, Guillaume, Marc, Florent, Chadi, Halim, and Brice) for the good times we spent together.

Furthermore, I would also like to acknowledge with much appreciation Alejandro CHAGOYA, From CIME, who was always available to solve any technical problem and Mamadou DIALLO from TIMA laboratory for his valuable support during the prototype layout phase.

My sincere thanks also goes to the staff of TIMA laboratory for their efficient help (Anne-Laure, Laurence, Youness, Frédéric, Ahmed and Nicolas).

Moreover, thanks to all our STMicroelectronics collaborators: Hervé LEGALL, Florian CACHO, Laurent BASTÈRES and Dimitri GOGUET for all their help and my friends from STMicroelectronics analog design division (Reda, Hanae, Louise, Hani, Sotiris, Nassim, Florian and Thomas).

Last but not the least, I would like to thank my family: my parents and my brothers for supporting me spiritually.

Contents

Contents	v
List of Figures	ix
List of Tables	xvii
1 Introduction	1
1.1 Analog and mixed-signal circuits market	1
1.2 AMS testing challenges	2
1.3 Built-In Self-Test	4
1.4 Motivations	7
1.5 Thesis outline	7
2 State-of-the-art of sinusoidal signal generators	9
2.1 Introduction	9
2.2 Closed-loop oscillators	10
2.2.1 Oscillators with two-level hard limiter feedback	11
2.2.2 Oscillators with multi-level hard limiter feedback	13
2.3 Open-loop sinusoidal signal generators	14
2.3.1 DDFS-based generators	14
2.3.2 $\Sigma\Delta$ -Based generators	16
2.3.3 SC-based generators	17
2.3.3.1 VGA-based generators	19
2.3.3.2 SC-filter-based generators	19
2.4 Generators based on harmonic cancellation techniques	20
2.4.1 SC-filter-based generators with harmonic cancellation	21
2.4.2 Ring oscillator-based generators with harmonic cancellation	22
2.4.3 DAC-based generator with harmonic cancellation	25
2.5 Distortion shaping technique	25
2.6 Spectral manipulation techniques for on-chip signal generators: Harmonic cancellation versus distortion shaping	27

3	Harmonic cancellation techniques using digital resources	35
3.1	Introduction	35
3.2	Theoretical basis	36
3.3	Practical implementation	37
3.3.1	Digital shift register	38
3.3.2	Weighting stage	39
3.3.3	Filtering stage	41
3.4	Harmonic cancellation with unitary scale weight ratios using odd number of signals	42
3.5	Harmonic cancellation with unitary scale weight ratios using even number of signals	46
3.6	Harmonic cancellation strategy with integer scale weight ratios . . .	50
3.7	Harmonic cancellation strategy with irrational scale weight ratios .	54
3.8	Comparison of different harmonic cancellation techniques	60
3.8.1	Limitations of harmonic cancellation implementation	60
3.8.2	Analysis of performances limitations	60
4	Circuit design and simulations	69
4.1	Introduction	69
4.2	Hardware architecture of the sinusoidal signal generator	69
4.2.1	Circular shift-register	71
4.2.2	Double-ended buffer	73
4.2.3	Non-overlapping buffer	77
4.2.4	D/A conversion	81
4.2.5	Bias circuit and harmonic cancellation calibration	84
4.2.6	Output filter	90
4.3	System-level electrical simulation results	92
4.4	Physical implementation of a proof-of-concept sinusoidal signal generator	99
4.4.1	Layout of the sinusoidal signal generator	101
4.4.2	Post-layout simulation results	105
5	Experimental results	107
5.1	Introduction	107
5.2	Prototype fabrication	107
5.3	Test setup	107
5.4	Test procedure	110
5.5	Experimental results	112
5.5.1	Oscilloscope acquisition	112
5.5.2	Linearity measurements	112
5.5.3	Experimental results at different operating frequencies . . .	115

5.5.4	Results discussion	117
6	Conclusions and future works	125
6.1	Thesis contributions	125
6.2	Future works	126
A	Résumé en français	129
A.1	Introduction	129
A.1.1	Contexte	129
A.1.2	Auto-test intégré	131
A.1.3	Motivations	131
A.2	État de l'art des générateur de signaux sinusoïdaux	132
A.2.1	Oscillateurs en boucle fermé	132
A.2.2	Générateurs en boucle ouvertes	133
A.2.3	Générateurs basés sur des techniques d'annulation d'harmoniques	135
A.3	Techniques d'annulation harmonique utilisant des ressources numériques	137
A.3.1	Base théorique	138
A.3.2	Implémentation pratique	138
A.3.3	Annulation d'harmonique avec les rapports de poids unitaire utilisant un nombre impair de signaux	139
A.3.4	Annulation d'harmonique avec les rapports de poids unitaire utilisant un nombre pair de signaux	141
A.3.5	Annulation d'harmonique avec les rapports de poids entier	143
A.3.6	Annulation d'harmonique avec les rapports de poids entier irrationnels	145
A.3.7	Comparaison de différentes techniques d'annulation d'harmoniques	147
A.4	Conception de circuit et simulations	149
A.4.1	Architecture du générateur de signal sinusoïdal	151
A.4.2	Résultats de la simulation électrique au niveau du système	153
A.4.3	Implémentation physique du générateur de signaux sinusoïdal	157
A.4.4	Résultats des simulations post-layout	158
A.5	Résultats expérimentaux	160
A.5.1	Configuration de test	160
A.5.2	Procédure de test	161
A.5.3	Acquisition par oscilloscope	162
A.5.4	Mesures de linéarité	162
A.5.5	Résultats expérimentaux à différentes fréquences d'opération	164

CONTENTS

A.5.6 Discussion des résultats	165
A.6 Conclusion	167
List of publications	171
Bibliography	173

List of Figures

1.1	Global Semiconductor Market.	2
1.2	Manufacturing cost and test cost per transistor [1].	3
1.3	Diagram of test setup with automated test equipment.	4
1.4	ATE cost evolution estimation [1].	5
1.5	Test time distribution: Mobile phone SoC (Courtesy of Infineon Technologies) [2].	5
1.6	General block diagram of analog and mixed-signal BIST.	6
2.1	Closed-loop oscillator.	10
2.2	Two-level limiter feedback oscillator: (a) block diagram; (b) feedback characteristic.	11
2.3	HD3 versus Q-factor value of a second-order band-pass filter.	12
2.4	Multi-level limiter feedback oscillator: (a) block diagram; (b) feedback characteristic.	13
2.5	Open-loop sinusoidal signal generator.	14
2.6	Block diagram of the conventional DDFS-based generator.	15
2.7	$\Sigma\Delta$ -based sinusoidal signal generator.	17
2.8	$\Sigma\Delta$ -based generators: (a) memory-based implementation; (b) $\Sigma\Delta$ -oscillator implementation.	18
2.9	SC-based generator: (a) block diagram, (b) timing diagram.	18
2.10	Programmable SC-VGA.	19
2.11	SC low-pass filter-based generator.	20
2.12	Harmonic cancellation-based generator using analog signals.	21
2.13	Ring oscillator-based generator with harmonic cancellation block diagram.	22
2.14	Subtraction harmonic cancellation strategy.	23
2.15	Harmonic cancellation-based generator using digital signals.	24
2.16	DAC-based generator with harmonic cancellation bloc diagram.	26
2.17	Conceptual block diagram of the distortion shaping technique.	27

LIST OF FIGURES

2.18	Switched-capacitor implementation of the sinusoidal signal generator: (a) Schematic view of the SC generator, (b) Programmable array of input elements.	29
2.19	Average THD of the output sine-wave versus maximum error level in the input elements for the generation techniques with and without spectral manipulation, with $\alpha_1 = 1$ and $\alpha_3 = 10^{-4}$	31
2.20	Average THD of the output sine-wave versus third-order non-linearity coefficient in the output filter for the generation techniques with and without spectral manipulation, with $\alpha_1 = 1$ and maximum error in step level at 1%.	33
2.21	(a) Obtained THD for the 1000 generator instances, with and without harmonic cancellation; (b) THD improvement due to the harmonic cancellation.	34
3.1	Temporal forms and spectra of periodic signals	37
3.2	Harmonic cancellation based generator.	38
3.3	Block diagram of the proposed sinusoidal signal generator.	39
3.4	Chronogram of the digital shift-register outputs.	40
3.5	Implementation based on weighted resistor network.	40
3.6	Implementation based on current sources.	41
3.7	Low-pass filter response.	41
3.8	Conceptual block diagram of the harmonic cancellation strategy using integer scale weight ratios and even number of signals to cancel the 3 rd and 5 th order harmonic components.	43
3.9	Phase vector diagram of the harmonic cancellation strategy using integer scale weight ratios and even number of signals to cancel the 3 rd and 5 th order harmonic components.	44
3.10	Block diagram of the proposed sinusoidal signal generator using 9 signal phases and unitary scale weights to cancel the third-, and fifth-order harmonic components.	45
3.11	(a) Waveform of the step-level sinusoidal signal; (b) waveform of the generated sine-wave (c) spectrum of the generated sine-wave.	45
3.12	Conceptual block diagram of the harmonic cancellation strategy using integer scale weight ratios and even number of signals to cancel the 3 rd and 5 th order harmonic components.	47
3.13	Phase vector diagram of the harmonic cancellation strategy using integer scale weight ratios and even number of signals to cancel the 3 rd and 5 th order harmonic components.	48
3.14	Block diagram of the proposed sinusoidal signal generator using four signal phases and unitary scale weights to cancel the third-, and fifth-order harmonic components.	48

3.15	(a) Waveform of the step-level sinusoidal signal; (b) waveform of the generated sine-wave; (c) spectrum of the generated sine-wave.	49
3.16	Conceptual block diagram of the harmonic cancellation strategy using integer scale weight ratios to cancel the 3 rd and 5 th order harmonic components.	51
3.17	Phase vector diagram of the harmonic cancellation strategy using integer scale weight ratios to cancel the 3 rd and 5 th order harmonic components.	52
3.18	Block diagram of the proposed sinusoidal signal generator using nine signal phases and integer scale weights to cancel the third- and fifth-order harmonic components.	52
3.19	(a) Waveform of the step-level sinusoidal signal; (b) waveform of the generated sine-wave; (c) spectrum of the generated sine-wave.	53
3.20	Conceptual block diagram of the harmonic cancellation strategy using irrational scale weight ratios to cancel the 3 rd , 5 th , 7 th and 9 th order harmonic components.	55
3.21	Phase vector diagram of the harmonic cancellation strategy using irrational scale weight ratios to cancel the 3 rd , 5 th , 7 th and 9 th order harmonic components.	56
3.22	Block diagram of the proposed sinusoidal signal generator using five signal phases to cancel the third-, fifth-, seventh- and ninth-order harmonic components.	57
3.23	(a) Waveform of the step-level sinusoidal signal; (b) waveform of the generated sine-wave; (c) spectrum of the generated sine-wave.	57
3.24	Correlation between third- and ninth-order harmonic component.	59
3.25	Generated step-level sine-wave with errors: (a) time domain; (b) frequency domain.	61
3.26	Generated output THD variation as function of the maximum delay error.	62
3.27	Generated output THD variation as function of the maximum weight mismatch.	64
3.28	Generated output THD histograms before and after calibration.	66
3.29	Comparison of the proposed harmonic cancellation strategies.	67
4.1	Block diagram of a practical implementation of the proposed sinusoidal signal generator.	71
4.2	D-scan flip-flop.	71
4.3	Circular shift-register architecture.	72
4.4	Chronogram circular shift-register.	73
4.5	Histograms of phase-shifts of five shift-register outputs, across 100 Monte Carlo iterations.	74

LIST OF FIGURES

4.6	Histograms of duty-cycles of five shift-register outputs, across 100 Monte Carlo iterations.	75
4.7	Double-ended buffer.	76
4.8	Double-ended buffer input/output wave-forms.	76
4.9	Classical non-overlapping signals generator.	77
4.10	Outputs of non-overlapping buffer.	78
4.11	Histograms of phase-shifts of complementary outputs provided by the digital part, across 100 Monte Carlo iterations.	79
4.12	Histograms of duty-cycles of complementary outputs provided by the digital part, across 100 Monte Carlo iterations.	80
4.13	Histograms of skews of complementary outputs provided by the digital part, across 100 Monte Carlo iterations.	82
4.14	Basic current-steering digital-to-analog conversion branch.	83
4.15	Output current waveform of the (a) positive path. (b) negative path. (c) differential output current.	84
4.16	Histograms of output currents provided by the current branches, across 100 Monte Carlo iterations.	85
4.17	Histograms of current ratios provided by the current branches, across 100 Monte Carlo iterations.	86
4.18	(a) Transistor-level schematic of the basic bias circuit. (b) Evolution of output voltage (V_{bias}) and control signal (Set).	87
4.19	Evolution of output currents and bias voltages.	88
4.20	Transient current evolution of 100 μ A current branch.	89
4.21	Second-order passive low-pass filter.	91
4.22	Output filter diagram.	91
4.23	Configuration time diagram of the sinusoidal signal generator.	92
4.24	Generated sinusoidal output signal under nominal conditions.	93
4.25	Spectrum of the generated sinusoidal output signal under nominal conditions.	94
4.26	Histograms of (a) THD and (b) SFDR of the generated sinusoidal signal across 100 Monte Carlo simulations.	95
4.27	Histogram of the magnitude of: (a) second harmonic component; (b) third harmonic component, across 100 Monte Carlo iterations without calibration.	96
4.28	Spectrum of the generated sinusoidal output signal under worst-case process and mismatch variations, before calibration.	97
4.29	Spectrum of the generated sinusoidal output signal under worst-case process and mismatch variations, after calibration.	98
4.30	Clock tree circuit.	100

4.31	Output current waveform of the proof-of-concept version: (a) positive path; (b) negative path; (c) differential output current.	101
4.32	Output sinusoidal signal of the implemented circuit.	102
4.33	Spectrum of the output sinusoidal signal of the implemented circuit.	102
4.34	Layout of the core of the sinusoidal signal generator.	103
4.35	Pad frame constraint.	104
4.36	Layout of the sinusoidal signal generator with pads.	104
4.37	Spectrum of the output sinusoidal signal resulted from post-layout simulation.	105
4.38	Spectrum of the output sinusoidal signal obtained from post-layout simulation after calibration.	106
5.1	Micro-photograph of the sinusoidal signal generator.	108
5.2	Pads diagram of the prototype.	108
5.3	Probes photo: (a) probes connection; (b) micro-photograph.	108
5.4	Block diagram of the experimental setup.	110
5.5	Setup photos.	111
5.6	Oscilloscope acquisition of the generated sinusoidal signal.	113
5.7	Photo of the spectrum of the generated sinusoidal signal before calibration at 166.67 MHz.	113
5.8	Photo of the power of the harmonic components of the circuit before calibration at 166 MHz.	114
5.9	Photo of the spectrum of the calibrated generator at 166.67 MHz.	116
5.10	Power of the harmonic components of the calibrated circuit at 166.67 MHz.	116
5.11	Spectra of the generated signals in different frequencies: from 1 MHz to 80 MHz.	118
5.12	Spectra of the generated signals in different frequencies: from 125 MHz to 333 MHz.	119
5.13	Variation of the fundamental tone power Vs signal frequency.	120
5.14	(a) SFDR; (b) THD; variation Vs frequency.	121
5.15	Variation of harmonic power.	122
5.16	Impact of odd- and even-order harmonics on the: (a) SFDR; (b) THD.	123
A.1	Diagramme de test avec des équipements de test externe.	130
A.2	Estimation de l'évolution du coût des ATEs.	130
A.3	Distribution du temps de test dans un SoC (Infenion technology).	131
A.4	Schéma bloc d'un BIST.	132
A.5	Oscillateur en boucle fermé.	133
A.6	Générateur en boucle ouverte.	134

LIST OF FIGURES

A.7	Générateur basé sur la technique de DDFS.	134
A.8	Générateur à capacité commuté avec annulation des harmoniques.	136
A.9	Générateur basé sur un oscillateur à anneaux avec annulation d'harmonique.	137
A.10	Schéma du générateur de signaux sinusoïdal proposé.	139
A.11	Schéma de la stratégie d'annulation des harmoniques utilisant des rapports de pondération unitaires et un nombre impair de signaux pour annuler la 3ème et la 5ème composantes harmonique.	141
A.12	Schéma de la stratégie d'annulation des harmoniques utilisant des rapports de pondération unitaires et un nombre pair de signaux pour annuler la 3ème et la 5ème composantes harmonique.	142
A.13	Schéma de la stratégie d'annulation des harmoniques utilisant des rapports de pondération entier pour annuler la 3ème et la 5ème composantes harmonique.	144
A.14	Schéma de la stratégie d'annulation des harmoniques utilisant des rapports irrationnelles.	146
A.15	Schéma bloc du générateur de signal sinusoïdal proposé.	146
A.16	Variation THD de sortie générée en fonction de l'erreur de retard maximum.	148
A.17	Variation de THD de sortie générée en fonction du décalage de poids maximal.	150
A.18	Schéma bloc d'une implémentation pratique du générateur de signal sinusoïdal proposé.	151
A.19	Branche de courant de base de conversion numérique-analogique.	152
A.20	Schéma au niveau de transistor du circuit de polarisation de base.	153
A.21	Algorithme de calibration d'une branche de courant.	154
A.22	Signal de sortie sinusoïdal généré dans des conditions nominales.	155
A.23	Spectre du signal de sortie sinusoïdal généré dans des conditions nominales.	155
A.24	Histogrammes de (a) THD et (b) SFDR du signal sinusoïdal généré sur 100 simulations de Monte Carlo.	156
A.25	Spectre du signal de sortie sinusoïdal généré sous des variations de processus et de mésappariement dans le pire des cas, avant calibration.	157
A.26	Spectre du signal de sortie sinusoïdal généré sous des variations de processus et de mésappariement dans le pire des cas, après calibration.	158
A.27	Layout du générateur de signal sinusoïdal.	158
A.28	Le spectre du signal sinusoïdal de sortie résultait d'une simulation post-layout.	159

A.29	Le spectre du signal sinusoïdal de sortie résultait d'une simulation post-layout, après calibration.	160
A.30	Micro-photographie du générateur de signal sinusoïdal.	161
A.31	Schéma du montage expérimental.	162
A.32	Acquisition par oscilloscope du signal sinusoïdal généré.	163
A.33	Photo du spectre du signal sinusoïdal généré avant calibration à 166,67 MHz.	163
A.34	Photo du spectre du générateur calibré à 166,67 MHz.	164
A.35	(a) SFDR; (b) THD; variation Vs fréquence.	166
A.36	Variation de la puissance des harmoniques.	167
A.37	Impact des harmoniques impaires et paires sur : (a) le SFDR; (b) THD.	168

List of Tables

3.1	Coefficients of harmonic cancellation technique.	54
3.2	Comparison of harmonic cancellation strategies.	67
4.1	Truth table of D-scan flip-flop.	72
4.2	Transistor sizes for basic current branch.	81
4.3	Bias voltages of the current branches.	81
4.4	Charge time for the bias circuits.	87
4.5	Passive low-pass filter.	90
4.6	Comparison to the state of the art.	98
4.7	Bias voltages of implemented current sources.	100
4.8	Bias voltages of calibrated current sources.	106
5.1	Pads table.	109
5.2	List of equipment.	112
5.3	Bias voltages, current ratios and current ratios variation percentage before and after calibration.	115

List of Algorithms

4.1	One current branch calibration algorithm.	90
-----	---	----

Liste des symboles

ADC	Analog-to-Digital Converter
ATE	Automated Test Equipement
AWG	Arbitrary Waveform Generator
CAGR	Compound Annual Growth Rate
CORDIC	COordinate Rotation DIgital Computer
CUT	Circuit Under Test
DAC	Digital-to-Analog Converter
DDFS	Direct Digital Frequency Synthesizer
DEM	Dynamic Elements Matching
DNL	Differential Non-Linearity
DPG	Digital Pattern Generator
DUT	Device Under Test
FCW	Frequency Control Word
FFT	Fast Fourier Transform
I/O	Input/Output
INL	Integral Non-Linearity
ITRS	International Technology Roadmap for Semiconductors
LFSR	Linear Feed-back Shift Register
MEMS	Micro-Electro-Mechanical System

PMU Power Management Unit

Q-factor Quality factor

RAM Random Access Memory

ROM Read-Only Memory

SEMI Semiconductor Equipment and Materials International

SFDR Spurious-Free Dynamic Range

SINAD Signal-to-Noise-and-Distortion

SNR Signal-to-Noise Ratio

SoC System on Chip

Te Test enable

THD Total Harmonic Distortion

Ti Test input

VGA Variable Gain Amplifier

$\Sigma\Delta$ Sigma-Delta

Chapter 1

Introduction

1.1 Analog and mixed-signal circuits market

Nowadays the quality of our daily life rests without any doubt on the huge growth of electronics in the last decades. The SEMI (formerly Semiconductor Equipment and Materials International) [3] predicts a continuation of the expansion of the semiconductor market from \$342.7B in 2015 to \$655.6B in 2025 with a CAGR of 6.7%, as shown in Fig. 1.1. This global growth includes an increase of the market of analog and mixed-signal circuits with a CAGR of 7.2% with \$380B in 2025. Analog and mixed-signal (AMS) circuits include a number of devices such as operational amplifiers, active or passive filters, analog mixers, D/A and A/D converters, PLL, etc. which are widely used in very large volume applications such as cellular telephones, hard disk drives, modems, motor controllers, multimedia players, etc.

The expansion of the AMS circuits market is driven by three main factors: First, the fast development of design and fabrication technologies for digital circuits creates new operation ranges (higher frequencies, lower voltages, lower currents, etc.) which require the development of new AMS devices that match the same operation conditions in terms of timing and power consumption. The second factor driving the rise of the AMS market is the growth of the telecommunication market (mobile, 5G, IoT) involving essentially AMS devices, notably converters and transceivers. The third factor is the wide use of systems combining sensors and integrated circuits in several applications such as medical, automotive, imaging and consumer electronics where A/D and D/A converters are unavoidable to interface between the sensor and the rest of the system.

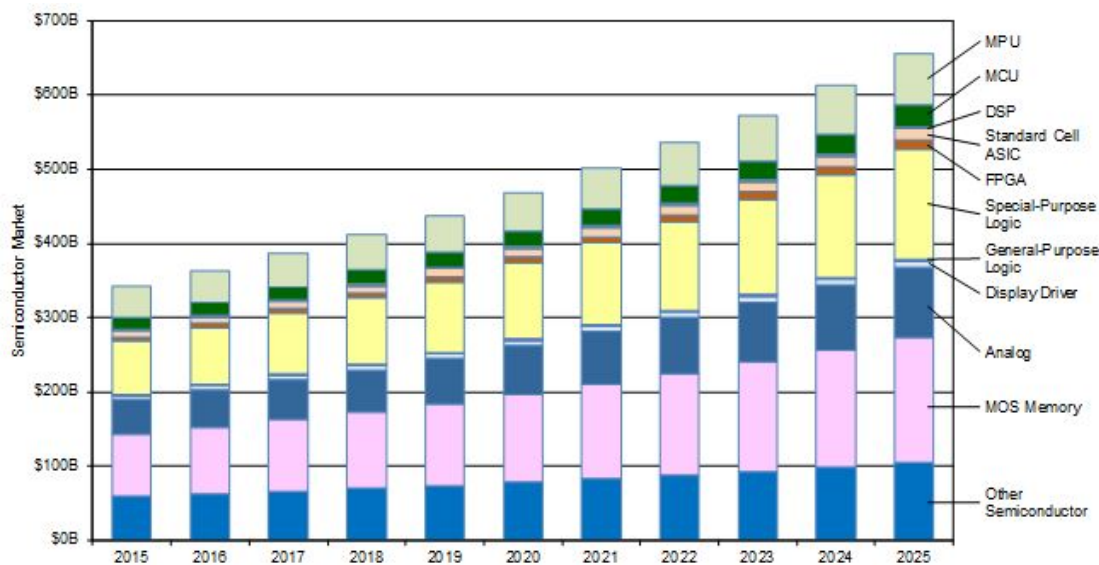


Figure 1.1: Global Semiconductor Market.

1.2 AMS testing challenges

The fabrication process of an integrated circuit include several steps of printing, masking, etching, implanting, and chemical vapor deposition. Like any industrial process, these steps are not perfect and some imperfections may introduce failures in the behave of the fabricated device. Unlike digital circuits, AMS circuits are very sensitive to the minor variations in the fabrication process.

In order to improve the quality value of their product, it is very important for semiconductor industries to test the individual circuit to guarantee that the delivered devices are not defective and meet all the required specifications. However, testing integrated circuits is a very expensive process comparable to the cost of the fabrication process. In fact, analysts in ITRS (International Technology Roadmap for Semiconductors) [1] indicate that the manufacturing cost has been dropping in a continuous way during the last 30 years, with a reduction amount around 30% per years. However, test cost of digital, analog and mixed-signal circuits tends to rise, or at least remains constant, with an increase of AMS test cost, as it can be seen in Fig. 1.2 extracted from the ITRS reports [1].

The high cost of AMS testing can be explained by the fact that post-fabrication validation process is usually based on functional specification tests using automated test equipment (ATE). It consists in the direct measurements of all performances of the device under test (DUT), in different operation conditions, and comparing the results to the expected specifications, listed in the circuit datasheet.

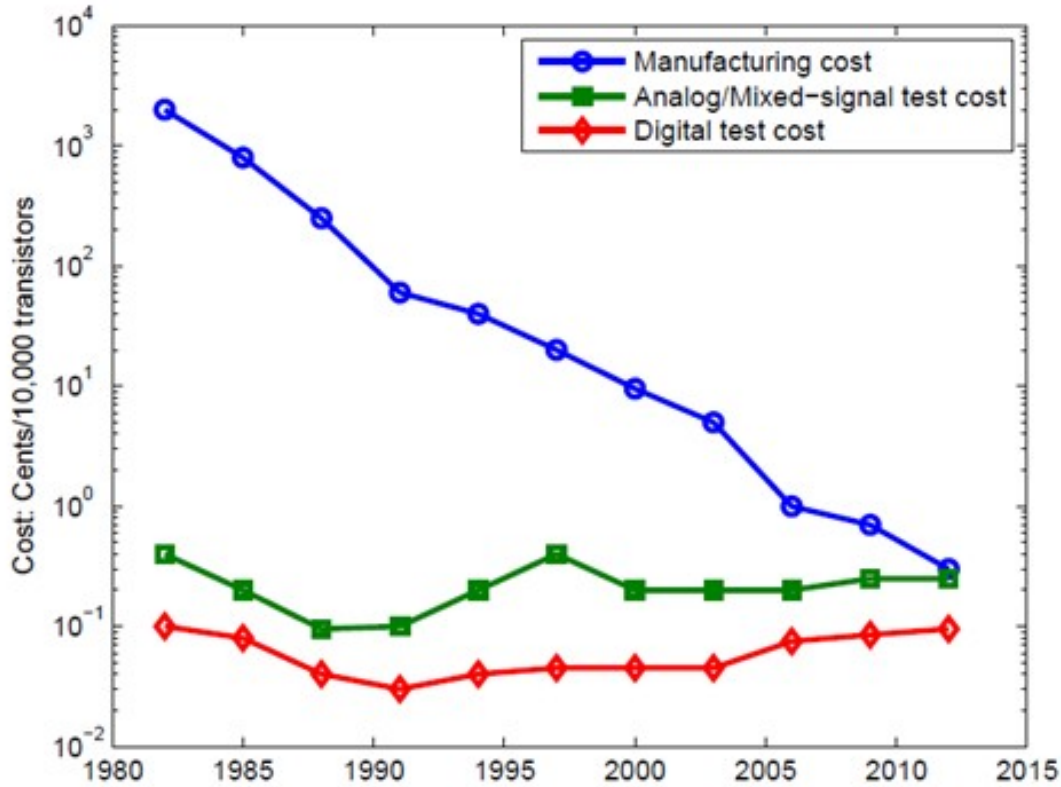


Figure 1.2: Manufacturing cost and test cost per transistor [1].

To manage this kind of functional tests, test equipment may include test stimulus generators to stimulate the DUT, acquisition instruments to receive and process the output of the DUT, power supplies and loads to activate the DUT under normal conditions, as schematically shown in Fig. 1.3. Some A/D and D/A conversion stages are often needed to configure the stimulation devices and to convert the DUT response to the digital domain to be computed and evaluated. The ATE-based test system require also the use of I/O circuitry, usually build into dedicated test board, to adapt the ATE inputs and outputs to communicate with the DUT, and interface devices to access to the DUT and establish all connections.

The complexity of external tester systems is necessarily increasing because of the evolution of DUT specifications, requiring accurate stimulus, high performance evaluation instruments and large memories for data acquisition. The increase of ATE complexity leads, in turn, to the increase of its cost, as estimated by the ITRS in Fig. 1.4. In addition, the growth of the integration rate in system-on-chip (SoC), involving digital systems, analog circuits, mixed-signal circuits, optical, RF and MEMS, complicates the access to the internal blocks of the system and requires

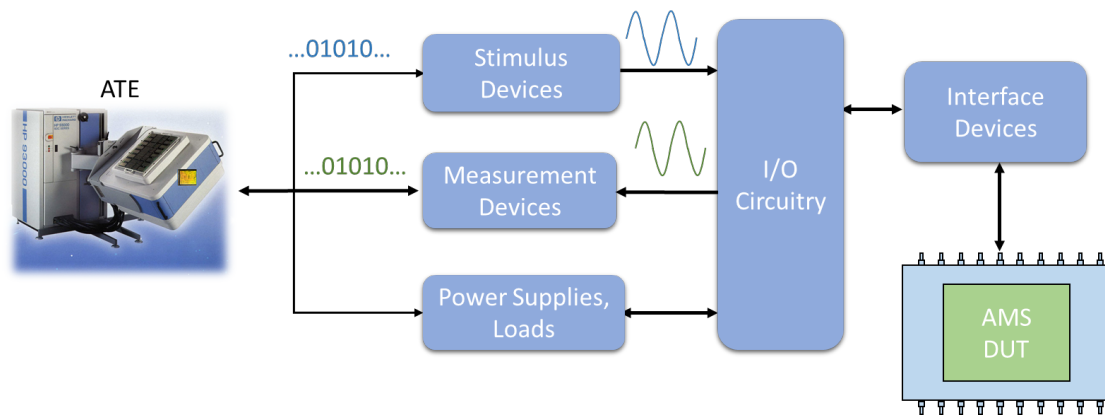


Figure 1.3: Diagram of test setup with automated test equipment.

dedicated test access. The ITRS analysts recommend to make efforts on reducing the cost of test interfaces in order to reduce the global test cost and compensate the rise of ATE cost, as shown in Fig. 1.4.

In order to give an idea of the complexity of AMS production test, Fig. 1.5 shows an example of the test time distribution per circuitry of a mobile phone SoC, the pie chart depicts that mixed-signal tests, RF tests and power management unit tests (PMU) consume the majority of the test time with 34%, 23% and 20%, respectively, of the totality of required test time.

AMS circuitry typically occupies 20% of the area of a SoC, but incurs 70% of the test cost and 45% of the test effort [4]. This may be explained by the fact that AMS test are not fully automated, and hence require the input of test engineers.

1.3 Built-In Self-Test

A promising solution to the issues of testing AMS circuits is the development of mixed-signal Built-In Self-Test (BIST) strategies. BIST techniques, first developed for testing digital blocks, are aimed at moving some of the ATE functionalities to the DUT and hence reduce the complexity of the external tester and test protocol.

In general, the use of BIST structures for AMS on-chip test is aimed to reduce test cost while keeping a high test quality by:

- **minimizing test time and effort:** in a full BIST scheme, the totality of test instruments are embedded in the DUT and test methodologies are programmed on-chip which reduce the time needed to setup and configure the external test equipment.
- **improving the self-testability of the DUT:** a full BIST circuit allows

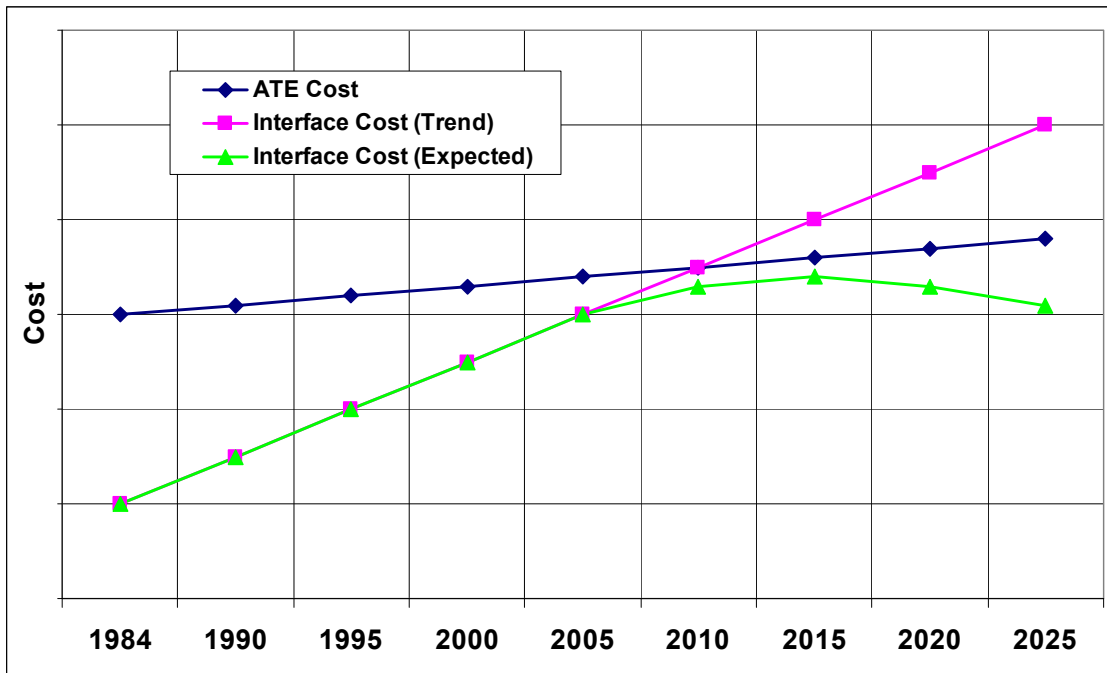


Figure 1.4: ATE cost evolution estimation [1].

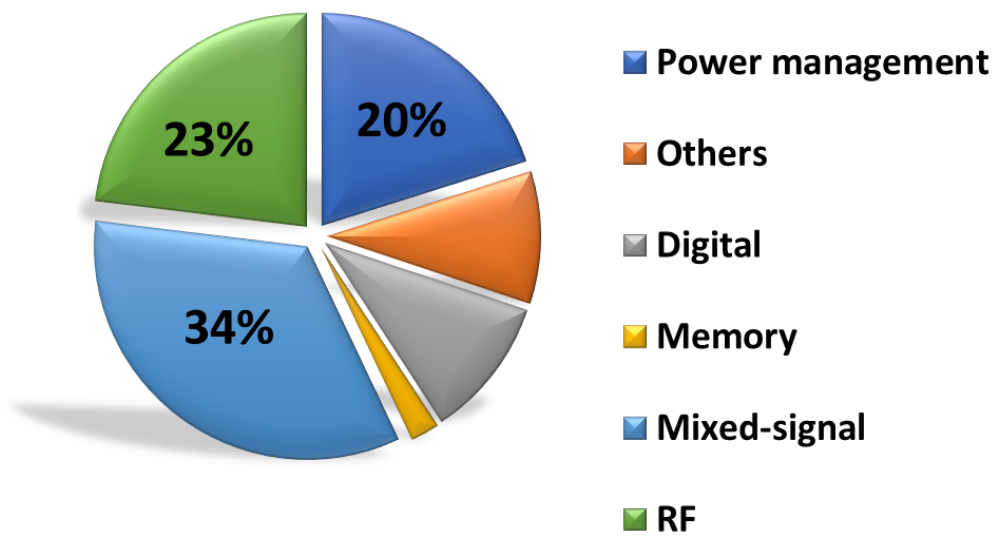


Figure 1.5: Test time distribution: Mobile phone SoC (Courtesy of Infineon Technologies) [2].

the DUT to evaluate its own performances in its real operating environment without external test equipment support.

- **reducing access complexity:** by including BIST in a complex SoC, test instruments would be embedded in the DUT which minimizes significantly the number of pins required to connect the SoC to an external tester.
- **improving test accuracy:** using embedded BIST might allow performing more accurate measurements without suffering from the ATE limitations and noise generated from different test support such as the load board.

However, the development of mixed-signal full BIST is still an open research topic. Unlike its digital counterpart, based on fault-based structural tests, mixed-signal test techniques are usually based on functional specification-based tests. Enabling on-chip specification-based test requires the development of built-in test instruments for providing, acquiring and analyzing the appropriate test signals required by each particular DUT.

Figure 1.6 depicts a conceptual block diagram of a full BIST required for testing AMS devices: a test stimulus generator is required to provide the appropriate stimulus. The test stimulus may correspond to a sine-wave, pulse, square-wave or arbitrary waveform depending on the type of test to be performed. The response of the DUT to the test stimulus is captured for processing by a response analyzer block. The test operation is controlled by a BIST controller that is driven from a low cost digital ATE.

BIST circuits should meet some requirements such as robustness to fabrication process variations, low power consumption, low area overhead, low design effort, and testability to ensure the accuracy of measurements.

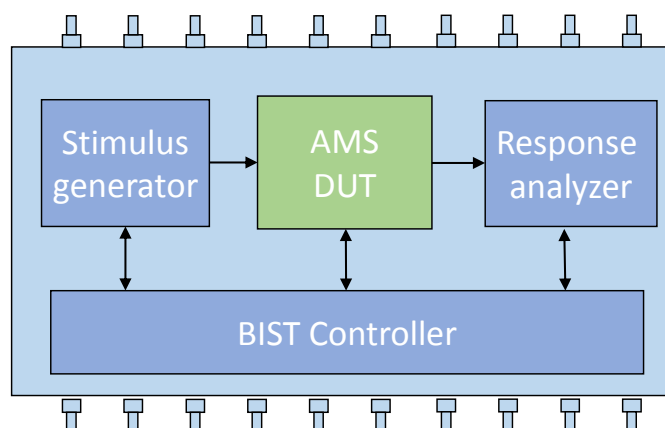


Figure 1.6: General block diagram of analog and mixed-signal BIST.

1.4 Motivations

One of the most critical blocks in an AMS BIST system is the stimulus generator. For many critical AMS circuits, such as A/D converters, amplifiers, filters, etc. the test stimulus must be an analog signal. Depending on the type of the target performance measurement, several types of analog stimulus may be used. Let us take the test of an ADC as an example: measuring the static performances of an ADC (INL and DNL) requires usually the use of a ramp signal or a slow sine-wave as test input. However, in order to measure its dynamic performances (SNR, SFDR, SINAD), a sinusoidal signal is usually required to drive the ADC under test.

In this thesis we focus on designing an embedded stimulus generator to provide a sinusoidal signal test stimulus. The design of an efficient and accurate sinusoidal signal generator may enable a wide variety of on-chip test applications for AMS circuits. Indeed, the vast majority of AMS circuits may be fully characterized by applying appropriate sinusoidal signal stimuli and analyzing the output response. As an example, we can cite the IEEE standard for ADC measurements [5], where a wide variety of test methods based on sinusoidal stimuli are described.

1.5 Thesis outline

The main goal of this thesis is to propose a novel sinusoidal signal generator for AMS BIST applications that:

- a) Improves the performances, in terms of linearity and operation frequency, of previously presented solutions.
- b) Reduces the design effort: the target sinusoidal signal generator should consist in mostly digital circuitry, which would allow us to easily migrate the design among different technological nodes.

This thesis is organized as follows:

Chapter 2 presents a review of the state-of-the-art of different sine-wave generators used for BIST applications, classified by their architectures and their signal generation strategies. Several works are detailed on the generation of a high-linear test stimulus for ADC testing and BIST purposes.

Chapter 3 introduces the principle of harmonic cancellation technique, which is a signal processing technique that may be adapted in signal generators to improve performance and simplify the design. In this chapter, we propose 4 different harmonic cancellation strategies that could be applied in a generic hardware architecture. The performance of each generation method is shown through simulation results of accurate behavior models and a comparison of all harmonic cancellation

techniques is provided as a guideline for test designer to select the appropriate sine-wave generation strategy for their design.

In chapter 4, we select one of the presented harmonic cancellation strategies, presented in chapter 3, and we detail the design of the sine-wave generator at transistor level. Electrical simulation in nominal operation, statistical simulations (Monte Carlo) and post layout simulation of the designed generator are provided to show its performances.

Chapter 5 presents the experimental results of the physical characterization of the fabricated prototype, where we evaluate the linearity of the implemented sine-wave generator.

Finally, chapter 6 concludes this thesis and discusses the directions for our future research on this topic.

Chapter 2

State-of-the-art of sinusoidal signal generators

2.1 Introduction

A key element for enabling analog and mixed-signal BIST is the design of a high-quality embedded analog signal generator in order to stimulate the DUT. Analog and mixed signal circuits testing requires most of the time the application of analog stimulus such as sine-waves, triangular waves, ramps, etc. depending on the test purposes. In this line, sinusoidal test stimulus are particularly interesting, since they are used in the characterization of a wide variety of analog and mixed signal circuits. As an example, there are a number of standard test techniques for ADC testing based on applying precise sinusoidal test stimuli [5].

In this chapter, we provide a comprehensive revision of different signal generation techniques that have been presented in the last years. In this line, we will focus the discussion on generation techniques that are suitable for on-chip implementation aimed at BIST applications.

Some constraints should be respected when designing analog stimulus generator for analog and mixed signal BIST applications :

- The generator must be capable of generating high-precision test signals with linearity exceeding that of the DUT.
- The generator should be programmable (amplitude, frequency) to accommodate the test stimulus to the desired test.
- The area occupied by the generator should be minimal.
- Low design effort.

The state-of-the-art shows a number of works aimed at implementing highly linear sine-wave generators. These generators can be classified according to their architecture into two main families: closed-loop oscillators and open-loop generators. Independently of the generator architecture, some harmonic manipulation techniques, such as harmonic cancellation and distortion shaping, may be also applied in the generation strategy in order to improve the stimulus linearity while reducing the implementation complexity of the circuit.

2.2 Closed-loop oscillators

Circuits based on LC tank and RC feedback such as Colpitts and Wien oscillators [6, 7, 8, 9] are classical approaches to design analog oscillators. However, it is usually difficult to integrate this type of generators in BIST applications for practical reasons, such as the complexity of the design and their high area and power overhead for oscillations with high spectral purity.

Astable closed-loop oscillators, conceptually shown in Fig. 2.1, are a classical solution for on-chip sinusoidal signal generation. They consist in a filtering stage with a non-linear feedback.

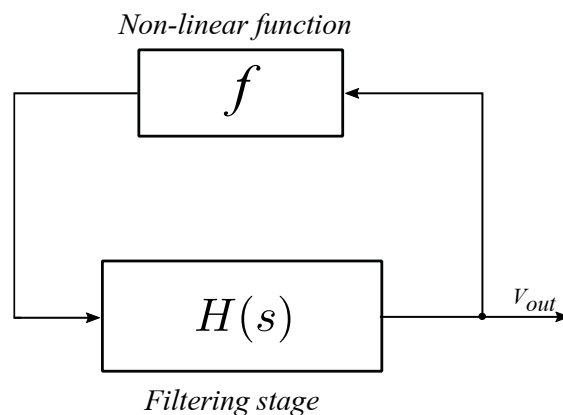


Figure 2.1: Closed-loop oscillator.

In practical implementations, a closed-loop oscillator usually consists of a band-pass filter and a hard limiter in the non-linear feedback loop. Different implementations have been presented in the literature. Some of them use two-level hard limiters, while others use multilevel hard limiter in the feedback loop.

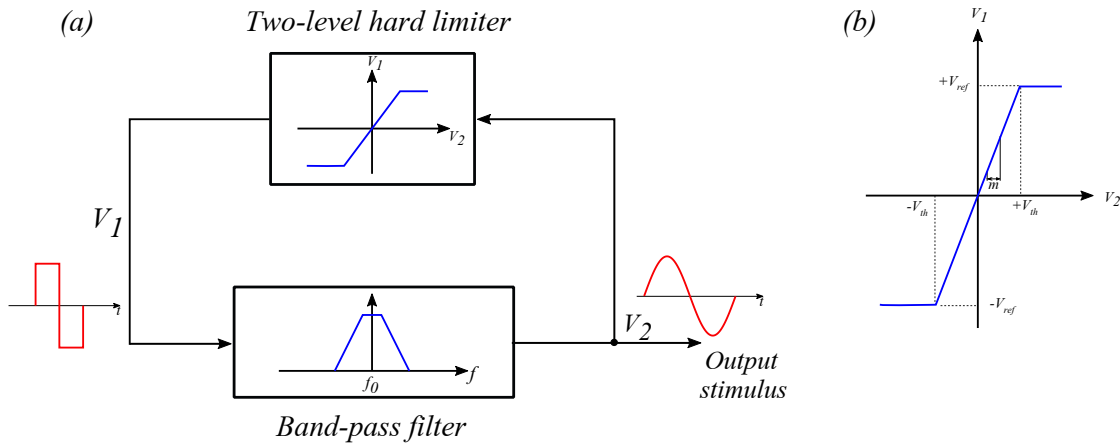


Figure 2.2: Two-level limiter feedback oscillator: (a) block diagram; (b) feedback characteristic.

2.2.1 Oscillators with two-level hard limiter feedback

A generic oscillator based on band-pass filter and using a simple comparator as a two-level hard limiter is shown in Fig. 2.2.a. The characteristic of the two-level comparator, as shown in Fig. 2.2.b, is given by the following equations

$$\begin{cases} V_1 = m \times V_2 & \text{for } |V_2| < V_{th} \\ V_1 = \text{sign}(V_2) \times V_{ref} & \text{for } |V_2| > V_{th} \end{cases} \quad (2.1)$$

where V_{th} is the threshold voltage of the input and V_{ref} is the clamping amplitude of the comparator.

The main advantages of this type of oscillator are the possibility of tuning the oscillation frequency by changing the center frequency f_0 of the band-pass filter [10], and the indirect control of the oscillation amplitude with the help of the two levels $\pm V_{ref}$ of the comparator [11] (for a given $\pm V_{ref}$, the amplitude of the output is controlled by the gain of the band-pass filter). The feedback loop behaves like a sinus-to-square wave converter when its gain is larger than the unity. Assume that the output of the filter V_2 is a sinusoidal signal, it will be converted into a symmetric square-wave V_1 . This square-wave will have a fundamental tone at the center frequency of the band-pass filter, as well as an infinite number of odd harmonics. When feeding the band-pass filter, only the fundamental tone is passed while all the other harmonics are filtered, hence the output signal should be a highly-linear sinusoidal signal.

However, a high Q -factor is required for the band-pass filter in order to reject all unwanted harmonics adjacent to the fundamental frequency. The work in [12] shows the evolution of the third harmonic component with respect to the quality-

factor of the filter. For reference, we reproduce the results in Fig. 2.3. Results show that a band-pass filter with $Q = 100$ is required to attenuate the third harmonic components below -60 dB.

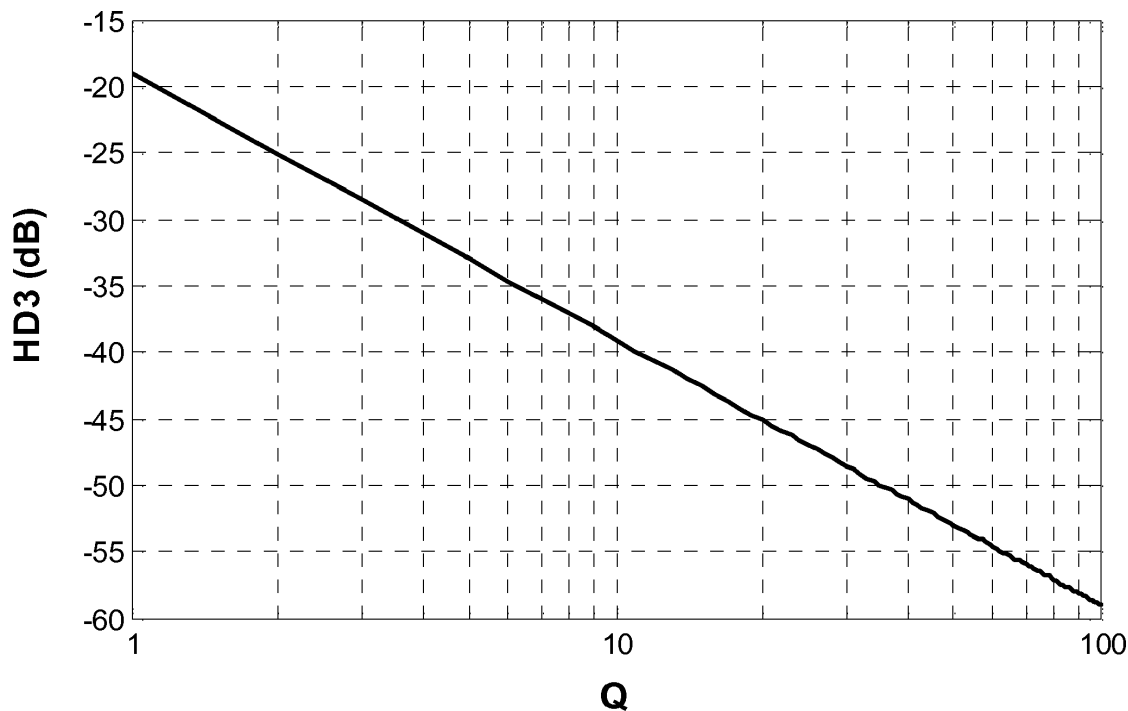


Figure 2.3: HD3 versus Q -factor value of a second-order band-pass filter.

Switched-capacitor design techniques are very convenient for implementing a band-pass filter with a large Q -factor because of many features such as the simplicity of the design and the reduced sensitivity to mismatch and temperature variations. A classical implementation of a filter-based oscillator is proposed in [12] and [13] using a two-level limiter, with a switched-capacitor band-pass filter. Experimental results demonstrate a Total Harmonic Distortion (THD) of -58 dB for 1 MHz output signal frequency. The implemented band-pass filter has a quality-factor $Q = 50$ to keep the third-order harmonic component below -50 dB, which increases the design complexity of the oscillator. The proposed generator is suitable for relatively low-frequency applications because the operation frequency of SC circuits is limited by RC behavior. Increasing the operation frequency of SC circuits also inverses the design complexity. This family of oscillators is also limited by the silicon area mostly consumed by the capacitors which increase the cost factor.

2.2.2 Oscillators with multi-level hard limiter feedback

Band-pass filter based-oscillators using multi-level hard limiter have been proposed to enhance the performances of the previous oscillator-family without increasing the Q -factor of the filter. The improvement factor in this class of oscillators is the use of non-linear harmonic shaping techniques allowing the suppression of unwanted harmonic components not filtered by the band-pass filter, mainly the third- and fifth-order harmonic components. It consists in using a multi-level comparator with multiple clamping voltages V_{ref_i} and multiple threshold voltages V_{th_i} in the feedback loop as it is schematically shown in Fig. 2.4.

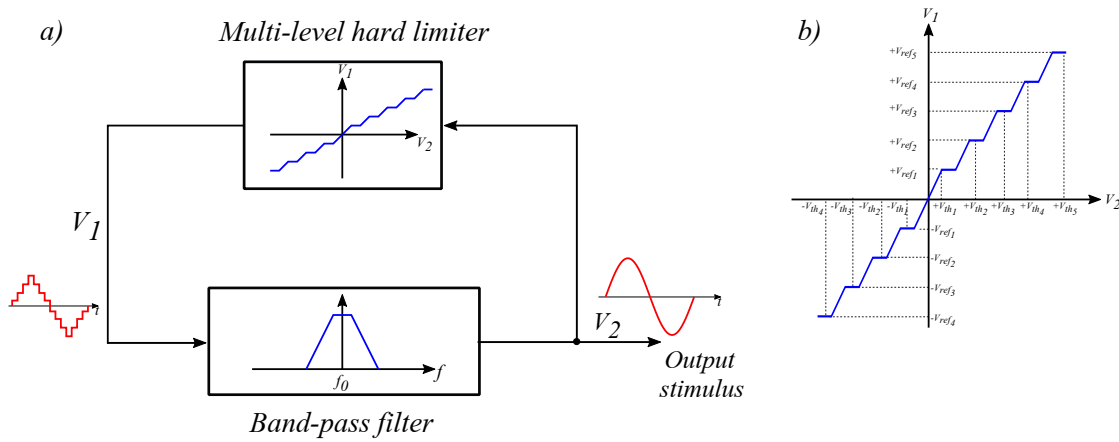


Figure 2.4: Multi-level limiter feedback oscillator: (a) block diagram; (b) feedback characteristic.

The introduction of the multi-level comparator in the band-pass filter based-oscillator will convert the sinusoidal signal V_2 to a step-wise sine-wave instead of a square-wave. By selecting properly the clamping levels and the threshold voltages of the comparator, a set of unwanted harmonic components can be suppressed in the spectrum of V_1 . Some proposals [12, 14] use a four-level comparator, with a fix clamping ratio equal to $\frac{1}{\sqrt{2}}$ and results show that 3^{rd} and 5^{th} harmonics can be fully canceled in the step step-wise sine-wave. A band-pass filter with a small quality-factor ($Q = 10$) is used to attenuate higher-order harmonic components. Experimental results demonstrate an improvement of the linearity of the generated sinusoidal signal with a THD of -53 dB for a generated sinusoidal signal at 10 MHz. However, the design still require a large Q -factor and also suffers from the linearity output swing and power consumption problems. In general, the linearity of oscillator-based generator depends strongly on the linearity and the selectivity of the employed band-pass filter and the smoothness of the non-linear feedback which make the implementation of these circuits quite challenging.

2.3 Open-loop sinusoidal signal generators

Open-loop sinusoidal signal generators usually take advantage of the digital signal processing techniques for analog signal generation. The signal generation strategy, conceptually shown in Fig. 2.5, usually contains a digital pattern generator that encodes a digitized high-resolution sinusoidal signal, a D/A converter to translate the signal to the analog domain and an analog filter on the output to reject all unwanted harmonic components.

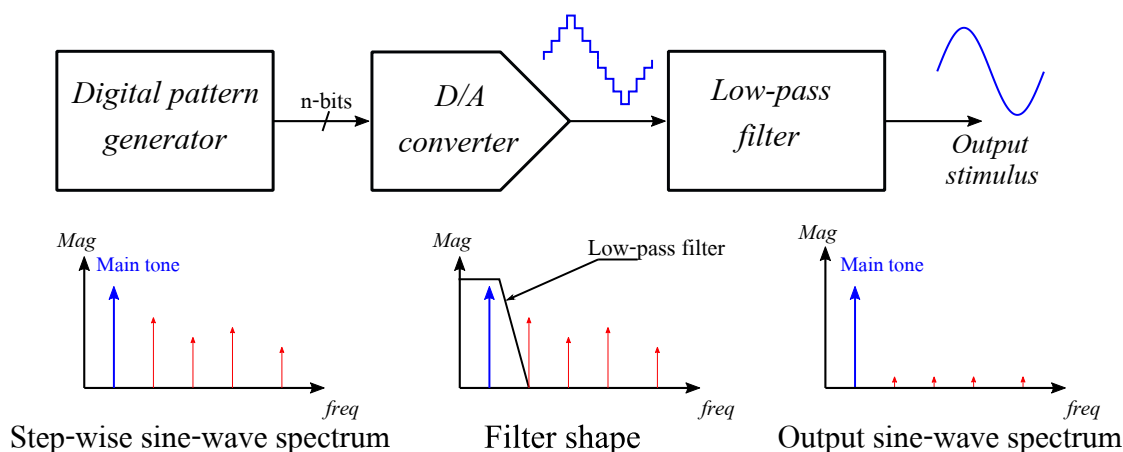


Figure 2.5: Open-loop sinusoidal signal generator.

Unlike closed-loop oscillators, this family of generators does not rely on an oscillation condition. The frequency and the amplitude of the generated signal are easily controlled digitally by configuring the digital pattern generator and the D/A converter contrary to the feedback-based oscillators where the signal features are controlled by the time-constant and the gain of the band-pass filter. The requirements of the filter will be also largely reduced and a basic passive filter is sufficient for the design.

2.3.1 DDFS-based generators

Due to the digital input stage of the open-loop generators, several possible approaches had been explored in order to implement this category of generators. A classical implementation is based on DDFS (Direct Digital Frequency Synthesizer) techniques. It was presented for the first time back in the 70's [15]. The conventional schema of a DDFS-based generator is conceptually shown in Fig. 2.6. It consists on a phase accumulator followed by a ROM, a D/A converter and a filter in the output. The phase accumulator serves as a digital phase generator, driven by a clock f_{clk} to generate a phase value sequence. The input of the phase

accumulator is a m -bits FCW (Frequency Control Word) which determines the periodicity of the phase accumulator. The output of the phase accumulator is a saw-tooth waveform that represents the linearly changing phase of a sinusoid. The ROM table, addressed by the output of the phase accumulator, contains the digital amplitude coefficients corresponding to the phase values of a single cycle of a sampled sine-wave. The digital samples provided by the ROM are then converted to the analog domain using a D/A converter to generate an analog step-wise sinusoidal waveform which will be filtered with the help of a low-pass filter in order to produce a linear sine-wave by attenuating unwanted harmonics. The frequency of the output signal is a function of the frequency control word FCW , the phase accumulator bit resolution n and the clock frequency f_{clk} as:

$$f_{out} = \frac{FCW}{2^n} f_{clk} \quad (2.2)$$

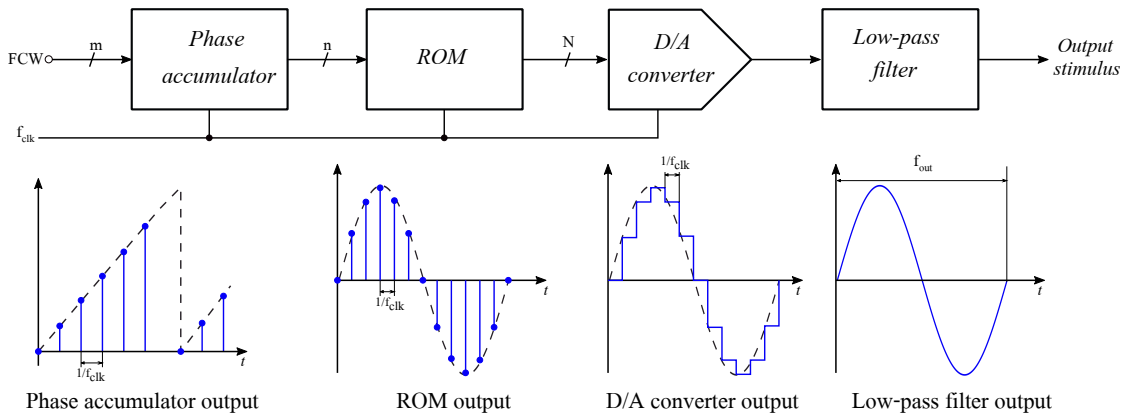


Figure 2.6: Block diagram of the conventional DDS-based generator.

The spectral purity of the conventional DDS-based generator is determined by ROM resolution. Unfortunately, a large resolution means a large ROM size and consequently higher area and slower access time. For this reason, some optimization approaches had been developed to reduce the ROM size, some of these techniques take advantage of the symmetric characteristic of the sinusoidal signal and propose to store the quarter of a single period, from 0 to $\pi/2$, to reconstruct the full signal from 0 to 2π , this way the number of sample is reduced and the ROM size will be divided by 4 compared to the conventional approach [16, 17]. A second ROM optimization method aims at reducing the number of phase-points used in the phase-accumulator to decrease the number of ROM samples, without degrading the linearity of the output signal, by applying the *Sunderland* sine-wave approximation techniques [18]. The application of this approximation method was

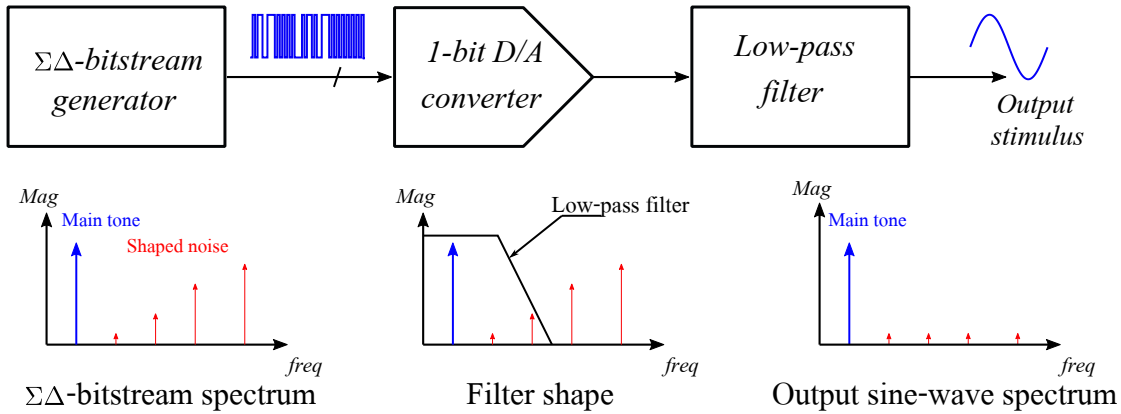
the subject of many works [18, 19, 20] showing that the *ROM* size can be compressed with a compression ratio between 51 [18] and 165 [20] compared to the conventional generation technique.

Another *ROM* compression technique is based on the *Taylor* approximation technique that relies on a linear interpolation between the sine samples [21]. This approach was applied in [21] and [22] resulting a compression ratio of 157 and 64, respectively. The CORDIC (COordinate Rotation DIgital Computer) algorithm [23] was also used to reduce the *ROM* size and some researches [24, 25, 26] had shown the effectiveness of this technique.

Despite all presented efforts to reduce the *ROM* size, *DDFS*-based generators are still costly in terms of area which implies an important area overhead for a BIST application. Moreover, the linearity of the generated sinusoidal signal is significantly influenced by the linearity of the D/A converter and the output filter that could be degraded because of mismatch and technological variations. For this reason several works propose to compensate the non-idealities of the physical implementation of the D/A converter and to increase the output signal linearity by minimizing the harmonic components close to the main tone. Some of the presented solutions [27, 28] rely on pre-distorting the original input sequence, to have a noise shape matched with the shape of the D/A converter, based on an estimation procedure. Another work [29] proposes a pre-distortion technique based on on-chip measurement instruments to measure the magnitudes and phases of unwanted harmonics with a feedback correction mechanism. However, this approach requires measurement equipment with higher accuracy and linearity than the D/A converter to be compensated. Otherwise, the estimation procedure may erroneously attribute to the D/A converter a component produced by the measuring equipment itself and, therefore, worsen the D/A performances when attempting to correct it by introducing an unneeded term.

2.3.2 $\Sigma\Delta$ -Based generators

The architecture of the $\Sigma\Delta$ -based generator, depicted in Fig. 2.7, is derived from the *DDFS*-based generator and it focuses on reducing the D/A converter requirements by using a single-bit optimized bitstream. The generation strategy is based on the noise-shaping of the characteristics of the $\Sigma\Delta$ encoding technique. It consists of generating a 1-bit $\Sigma\Delta$ -encoded version of an N -bit digital signal which will be converted to the analog domain using a 1-bit D/A converter. An analog low-pass filter is used at the output in order to reconstitute the sinusoidal signal. The shape of the output filter should match the noise shaping of the $\Sigma\Delta$ -bitstream to attenuate the shaped quantization noise and conserve only the fundamental tone in the frequency of the output. The quality of the output signal depends strongly on the spectral content of the optimized $\Sigma\Delta$ -bitstream [30, 31].

Figure 2.7: $\Sigma\Delta$ -based sinusoidal signal generator.

Previous works show that the $\Sigma\Delta$ -bitstream generator may be implemented with two different approaches. The first approach, schematically presented in Fig. 2.8.a, is based on using a memory module where a portion of the $\Sigma\Delta$ -encoded signal is stored and reproduced periodically. The memory-based $\Sigma\Delta$ -generator relies in general on a *LFSR* (Linear Feed-back Shift Register) with the output fed to the input and a 1-bit D/A converter which can be a simple digital buffer [32, 33]. This approach has several nice advantages such as the modulator speed and the reduced area of the circuit. Some solutions were explored in order to improve the precision of the output signal by increasing the resolution of the $\Sigma\Delta$ -bitstream by using *LFSR* with increased length or by replacing the *LFSR* by a *RAM* memory [33, 34]. On the other hand, the second approach, shown in Fig. 2.8.b, is actually a closed-loop oscillator approach. It is based on implementing a $\Sigma\Delta$ -modulator in a gain loop configuration with a digital resonator which generates an N -bit sinusoidal signal with amplitude and phase determined by the initial conditions in the multi-bit registers [35]. This implementation has a high precision and high frequency resolution. However both implementations are limited by the linearity of the filter and require the design of a filter with high selectivity, for instance in [35] a 6th-order filter was required to implement a $\Sigma\Delta$ -oscillator-based generator to attenuate the shaped quantization noise.

2.3.3 SC-based generators

SC-based generators use a programmable gain element with a DC input as a simple DAC to generate a step-wise sinusoidal waveform, as it is shown in Fig. 2.9.a. The linearity of the sinusoidal output depends essentially on the number and the accuracy of the step-levels used to construct the signal, however increasing the number of step-levels implies the increase of signal paths and hence the design

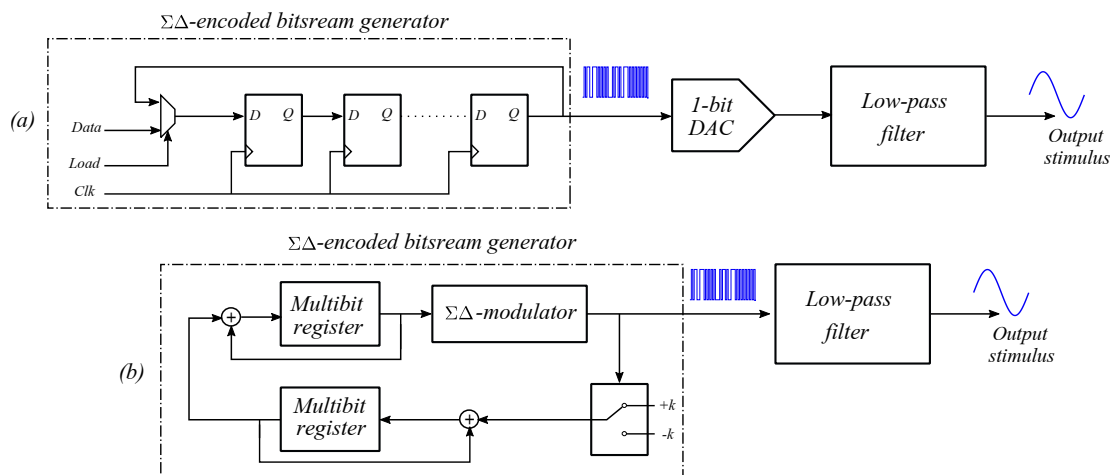


Figure 2.8: $\Sigma\Delta$ -based generators: (a) memory-based implementation; (b) $\Sigma\Delta$ -oscillator implementation.

complexity of the circuit.

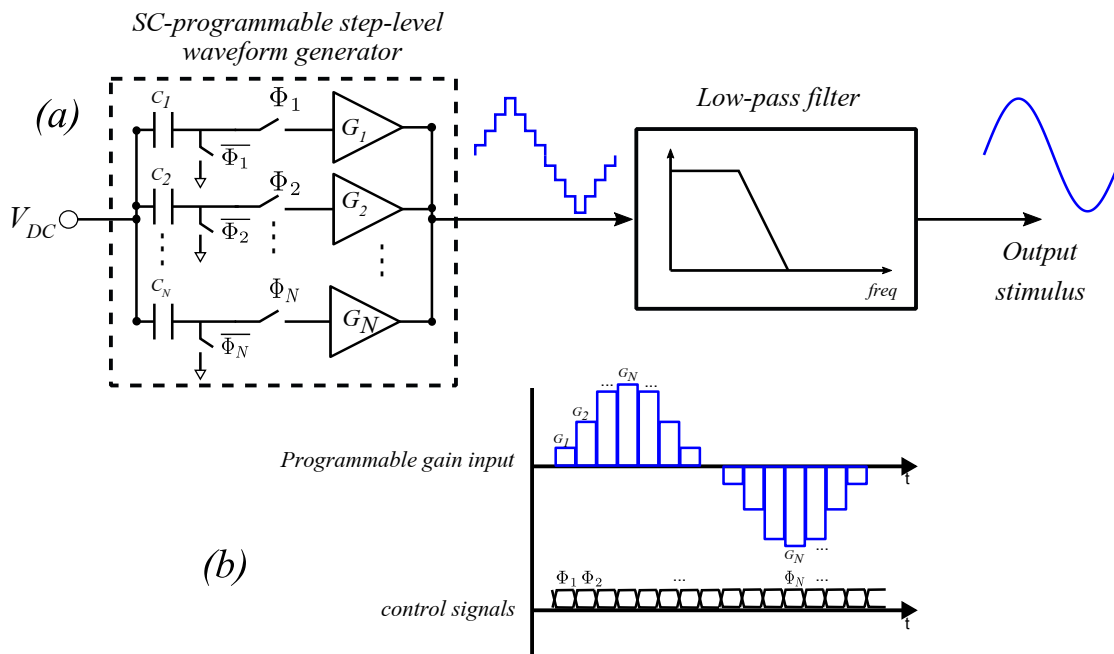


Figure 2.9: SC-based generator: (a) block diagram, (b) timing diagram.

2.3.3.1 VGA-based generators

Several implementations of SC-based generators rely on a programmable SC-VGA, as depicted in Fig. 2.10, to generate the step-wise sinusoidal signal [36, 37, 38]. Each gain step represents a value of an ideally sampled sine-wave. For an amplifier with N -gain steps, a step-wise sine-wave with maximum $4N$ samples can be generated. The Φ_z signal set the zero of the sinusoid and the signal Φ_i serves to select the appropriate gain. The step gain of the signal is controlled by the sequences of Φ_{in} and $\overline{\Phi_{in}}$ and the signal amplitude is fixed by the value of the reference input voltages $+V_{DC}$ and $-V_{DC}$

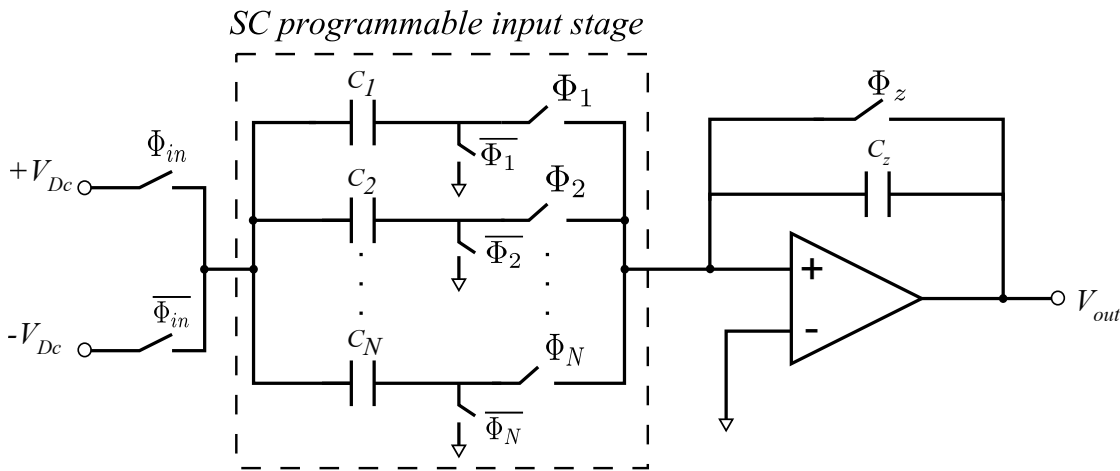


Figure 2.10: Programmable SC-VGA.

The main advantages of this implementation are the simplicity, the compact implementation and the simple control of the frequency and the amplitude of the generated signal through the input voltage V_{DC} and the clock frequency of the control signals Φ_i . However, in terms of the linearity of the output signal, the performance of this approach is limited by the accuracy and the number of step-levels and by the selectivity of the output filter. Thus the improvement of the spectral purity of the output will require the implementation of more signal paths and the use of a very smooth high-selective filter which implies increasing the design complexity and the area overhead.

2.3.3.2 SC-filter-based generators

The main idea of the generators based on SC-filter consists on merging the generation and the filtering stages to reduce the area overhead. The work in [39] and [40] present a second-order low-filter whose input capacitors had been modified

to include a number of programmable capacitors that can be connected and disconnected to the signal path according to the state of the control signals Φ_i , as it schematically shown in Fig. 2.11. A DC input reference provides control on the amplitude of the generated signal. The linearity of the output sinusoidal signal depends strongly on the linearity of the filter and the number and accuracy of the generated step-levels.

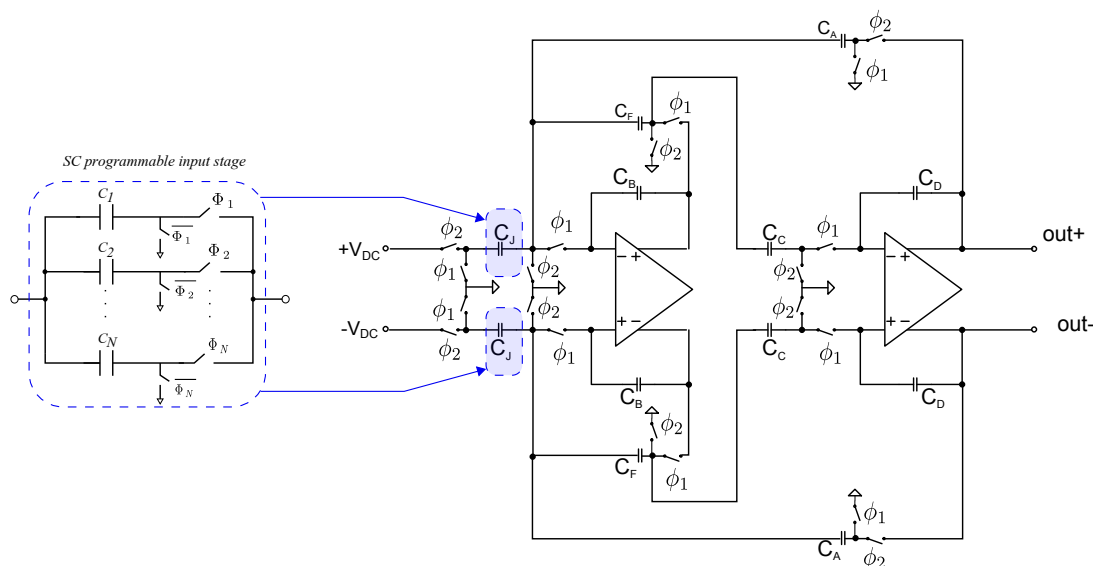


Figure 2.11: SC low-pass filter-based generator.

2.4 Generators based on harmonic cancellation techniques

Harmonic cancellation is a signal processing technique aimed at generating an analog signal with a high spectral quality by combining a set of scaled and time-shifted versions of an arbitrary periodic signal. This technique allows removing a set of unwanted harmonic distortion components from the spectrum of a generic periodical signal, without additional resources for measuring and pre-distortion as used in [27, 28, 29]. Hence, harmonic cancellation can be used in a practical sinusoidal signal generation scenario to cancel harmonic components close to the fundamental frequency of the desired signal, while a lenient low-pass filter attenuates higher-order harmonics. The first practical implementation of a sinusoidal signal generator based on harmonic cancellation principles was presented in the 60's [41], although this proposal has not been fully developed until recent years.

Thus, in the last few years, several sinusoidal signal generators have been presented that take advantage of harmonic cancellation to reduce the complexity of the required circuitry based on circuit architectures presented previously.

2.4.1 SC-filter-based generators with harmonic cancellation

In general harmonic cancellation is based on combining a set of analog periodical signals with appropriate phase-shifts and scale weights, as it is schematically shown in Fig. 2.12, in order to cancel a set of low-order harmonic components in the resulting combined signal. A simple low-pass filter is then used to cancel higher-order harmonics. This approach has the potential of simplifying the design of the output filter while providing a high-quality output sinusoid.

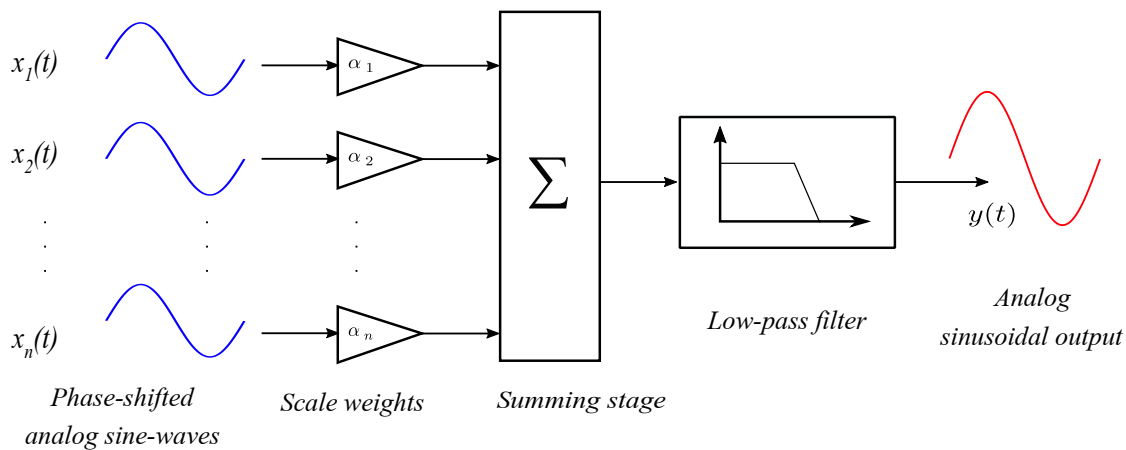


Figure 2.12: Harmonic cancellation-based generator using analog signals.

However, the direct implementation of the conceptual block diagram in Fig. 2.12 is challenging. In fact, using different sine-wave generators to provide a set of phase-shifted outputs requires a perfect matching between the generators to avoid degrading the performance of harmonic cancellation. Furthermore, implementing such architecture implies a considerable additional cost in terms of area and power consumption. Instead of that, the generator proposed in [42] implements the harmonic cancellation at the input of a modified switched-capacitor second-order low-pass filter. The generator takes the advantage of the programmable input stage of the basic generator presented previously in Fig. 2.11 to provide the phase-shifted versions of the sinusoidal signal simultaneously, using the same elements. Given that there is a trade off between the number of harmonics to be canceled, the number of constructing signals, the complexity of the implementation and the control of the input stage [43], the authors in [42] propose to combine simultaneously three sinusoidal signals phase-shifted by $2\pi/9$. The main goal of

this generation scenario is to remove the third-order harmonic component, which is the most significant harmonic distortion component, in the spectrum of the generated sine-wave before getting to the filtering stage. Results in [42] demonstrate that this generator is able to provide a linear sinusoidal signal in the output with a THD of -77 dB at 1 MHz.

2.4.2 Ring oscillator-based generators with harmonic cancellation

Another widely explored approach for generating phase-shifted periodic signals in the context of signal generation with harmonic cancellation is the use of ring oscillators [43, 44, 45, 46, 47]. The generators use a N -stage phase-shift ring oscillator as shown in Fig. 2.13 to provide a set of phase-shifted signals. The output of two consecutive stages of the ring-oscillator will have a phase-shift of $\frac{2\pi}{N}$, this way any selected phase-shift can be implemented by choosing properly the number of the stages of the oscillator. Following the general harmonic cancellation schema in Fig. 2.12, the selected phase-shifted signals are then fed to a weighting stage and are summed to cancel a set of undesired harmonics.

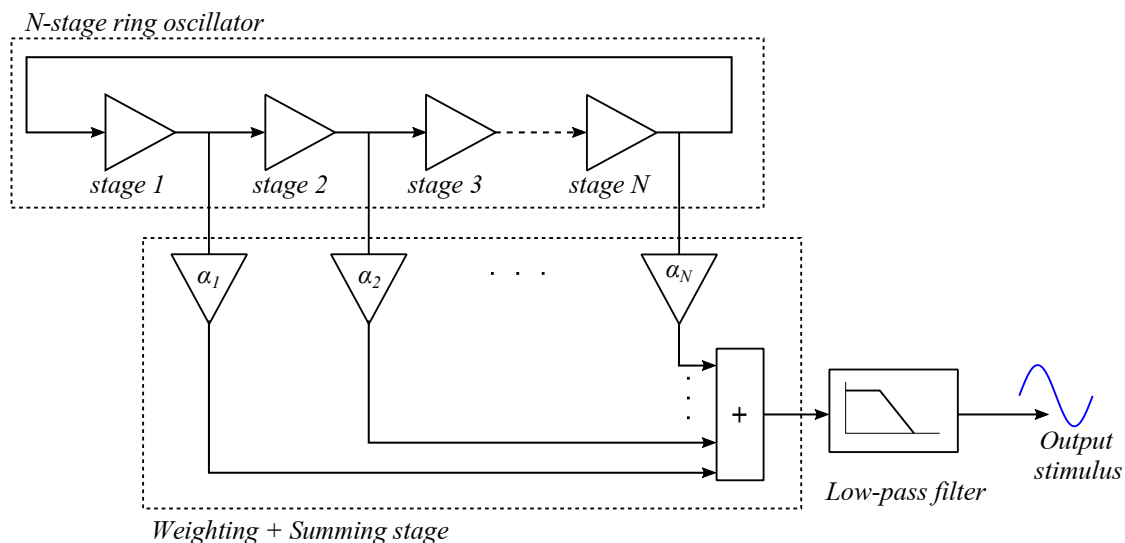


Figure 2.13: Ring oscillator-based generator with harmonic cancellation block diagram.

The work in [43, 44] details the implementation of a sinusoidal signal generator based on this harmonic cancellation strategy using a ring-oscillator. Authors propose to combine time-delayed and scaled versions of a periodical signal $x_0(t)$ to obtain a signal $y(t)$ in which only a set of low-order harmonics are not cancelled.

The amplitudes of the signals are scaled with the help of a programmable amplifier in such a way that the magnitudes of the non-canceled harmonic components in $y(t)$ will be equal to the magnitudes of those of the original signal $x_0(t)$, so by subtracting the two signals $x_0(t)$ and $y(t)$, all harmonic components non-canceled in $y(t)$ will be compensated and removed in the resulting signal $z(t)$. A low-pass filter is used at the output to attenuate the remaining harmonic components.

Figure 2.14 shows an example of this harmonic cancellation strategy using a 3-stages phase-shift ring oscillator to provide three signals phase-shifted by $\frac{2\pi}{3}$. These three signals are weighted by a coefficient of $\frac{1}{3}$ and summed to provide the signal $y(t)$. Figure 2.14.a and Fig. 2.14.b show the spectrum of the original signal $x_0(t)$ and the resulting combining signal $y(t)$, respectively, in which all harmonics components are removed, except the third harmonic and its multiples. The non-canceled harmonics have the same magnitudes and phases as the harmonics in the original signal. The spectrum of the differential combination between $x_0(t)$ and $y(t)$ provides signal $z(t)$ whose spectrum is shown in Fig. 2.14.c. It is clear to see that all harmonics with order multiple of three are canceled. Figure 2.14.d shows the spectrum of the output signal after a third-order low-pass filter to remove the remaining non-cancelled harmonics.

Good linearity figures are demonstrated using discrete on-board prototypes, with a THD of -67 dB at 10 KHz. However, moving this technique to an on-chip implementation may be problematic due to the extensive use of analog processing.

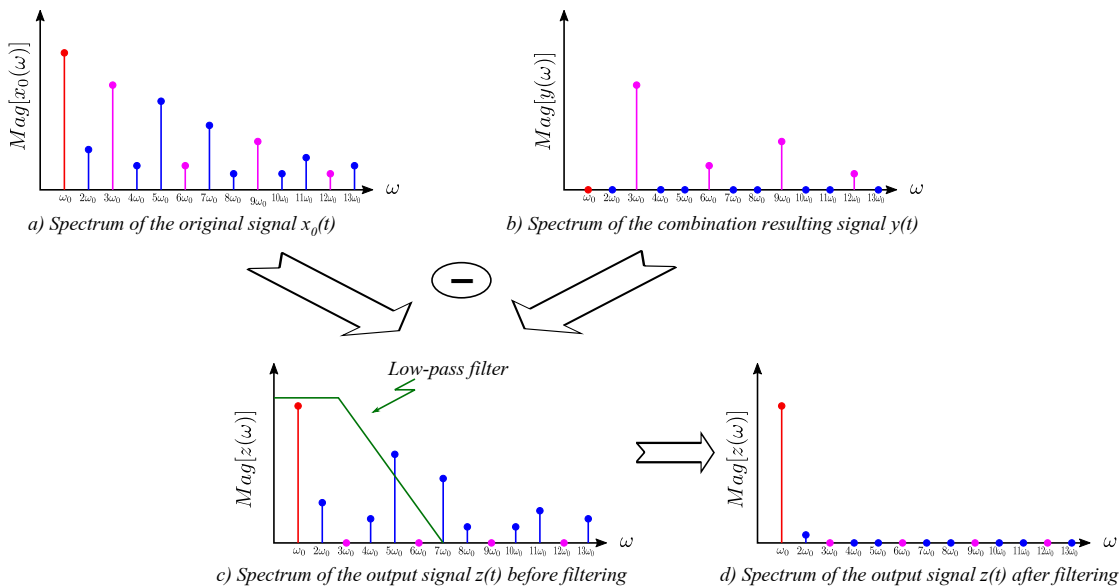


Figure 2.14: Subtraction harmonic cancellation strategy.

A fully on-chip implementation of the harmonic cancellation technique, based

on digital resources, has been presented in [45]. The proposed circuit consists of a digital ring oscillator to provide time-delayed square-waves, a resistor network to scale and sum the time-delayed signals and a passive low-pass filter to attenuate high-frequency harmonics. Experimental results demonstrate a THD of -72 dB for a sinusoidal signal generated at 10 MHz. The linearity is limited by the impact of mismatch and process variations on the summing resistors and the ring oscillator, that reduces the effectiveness of the harmonic cancellation.

The main drawback of harmonic cancellation techniques applied by the previous generators is their focus on canceling only one harmonic at a time without being able to suppress other harmonics simultaneously. Moreover, the problem increases while migrating from old technology to newer ones because of the analog structures of the generators.

Recently, harmonic cancellation techniques, using a more efficient harmonic cancellation strategy giving the possibility to attenuate more than one distortion harmonic component, have been exploited to design efficient sinusoidal signal generators based on mostly digital circuitry, which makes this generation strategy very appealing for integration in a complex mixed-signal SoC [46, 47, 48, 49]. These on-chip sinusoidal signal generators combine a set of digital square-waves with appropriate phase-shifts and amplitude scaling to generate an analog sinusoidal signal with high spectral quality, as shown in the block diagram in Fig. 3.2.

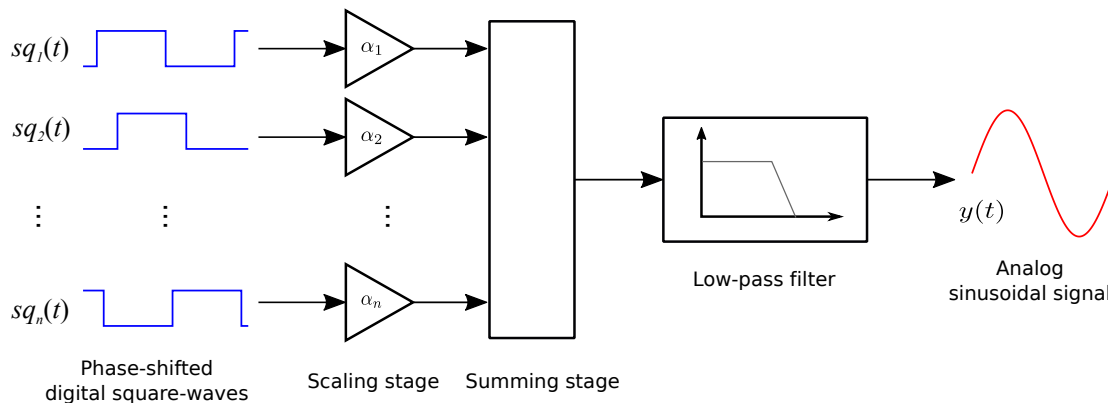


Figure 2.15: Harmonic cancellation-based generator using digital signals.

A generator based on a digital ring oscillator and a resistor network is proposed in [46]. The proposed generator combines five digital square-waves with three different amplitudes in order to cancel the 3^{rd} -, 5^{th} -, 7^{th} - and 9^{th} -order harmonic components. The feasibility of this strategy was demonstrated experimentally and the THD of the resulted signal is -70 dB at 850 MHz. However, given that circuit is very sensitive to delay errors introduced by the ring oscillator, an external calibration loop is used. Based on this work, a second generator combining two

stages of harmonic cancellation to attenuate a larger number of harmonics was designed in [47]. The number of canceled harmonic components was extended until the 21th-order components. The weighting stages were designed as a network of current mirrors to scale the phase-shifted square-waves with scales of $\frac{1}{2}$, $\frac{\sqrt{2}}{2}$, $\frac{\sqrt{3}}{2}$ and 1 using the DEM (Dynamic Elements Matching) technique to improve the matching between the current mirrors and reduce the impact of fabrication process variation.

2.4.3 DAC-based generator with harmonic cancellation

This approach, introduced in [50] and [51], derives from the DFFS-based generator presented previously in 2.3.1 with an additional harmonic cancellation strategy built into the DAC. The general architecture of the DAC-based generator with harmonic cancellation is schematically depicted in Fig. 2.16 where, similarly to the DFFS-based generator, a DPG (Digital Pattern Generator) is used to provide a set of square-waves with selected phase-shifts. These digital signals are fed to the DAC to be scaled and summed. In this level, the selection of the proper weights is very critical to apply perfectly the harmonic cancellation strategy. The DAC provides an analog step-wise sinusoidal signal in which a number of low-order harmonic components is canceled. A low-order low-pass filter is then introduced to attenuate the higher-order harmonics and generates a sinusoidal signal with a high spectral linearity.

The current-steering DAC is designed with unit current mirrors to ensure a good matching and [51] is performing the DEM technique to improve linearity of the DAC and reduce the scaling error which may dramatically reduce the performances of the harmonic cancellation. Each set of current-unit is controlled by the synchronized digital signals provided by the DPG to reach the required scale of the selected square-wave. Experimental implementation had been developed to demonstrate the performance of this approach and the result shows a SFDR of 43 dB for the generator without the DEM [50] and a SFDR of 70 dB at 100 MHz for the generator with the DEM technique which show the sensitivity of this type of approach to the linearity of the DAC.

2.5 Distortion shaping technique

The so-called distortion-shaping algorithm, originally proposed for improving the linearity of external low cost AWGs [52, 53], is aimed at pre-compensating, in the digital domain, the non-linearity of analog and mixed-signal blocks in the generator signal chain. In particular, this technique proposes to interleave time-shifted versions of the target sinusoidal signal in such a way that the intermodulation

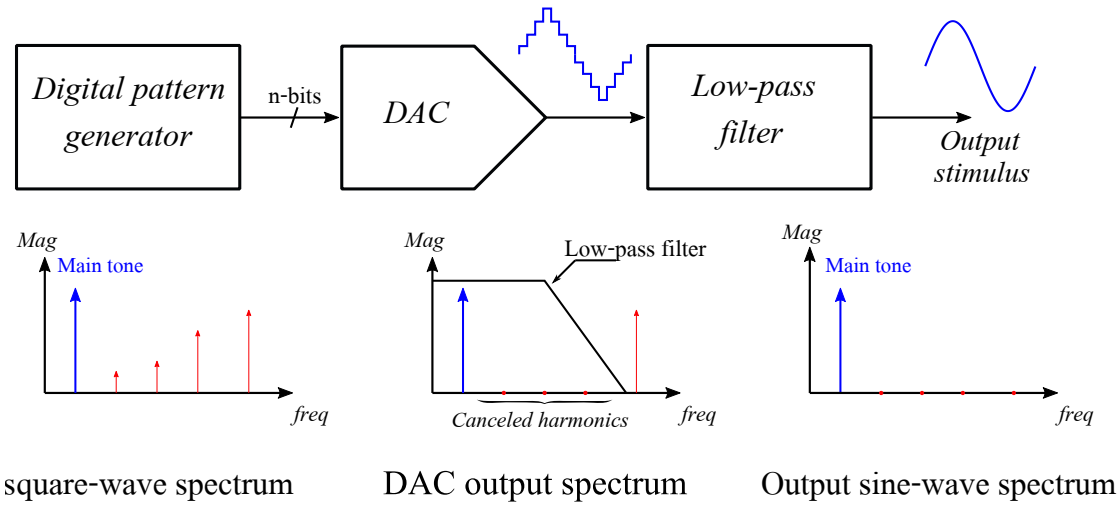


Figure 2.16: DAC-based generator with harmonic cancellation bloc diagram.

products produced by subsequent non-linear blocks in the signal chain will move low-order harmonics to higher frequencies far from the main tone, relaxing this way the design of the generator output filter.

As an example to show the functionality of this technique, let us consider the case of an open-loop sinusoidal generator as described in previous section 2.4.1 featuring a weakly non-linear output filter. Let us assume for the sake of the example that the non-linearity of the filter can be approximated as a third-order polynomial. If the filter is driven by a pure sinusoidal signal, this non-linear filter will limit the spectral quality of the generated output by introducing third-order harmonic distortion. In order to compensate the non-linearity of the output filter, the distortion shaping algorithm, as it is conceptually presented in Fig. 2.17, proposes to modify the generator to feed the filter with a signal composed of samples of two time-interleaved sinusoids as,

$$D_{in}(nT_s) = \begin{cases} x_0(nT_s) & n \text{ is even} \\ x_1(nT_s) & n \text{ is odd} \end{cases} \quad (2.3)$$

where

$$\begin{cases} x_0(nT_s) = A \sin\left(2\pi f_0 nT_s + \frac{\pi}{6}\right) \\ x_1(nT_s) = A \sin\left(2\pi f_0 nT_s - \frac{\pi}{6}\right) \end{cases} \quad (2.4)$$

A and f_0 are the amplitude and frequency of the original sinusoid, respectively, and $T_s = 1/f_s$ is the sampling period. If the non-linearity of the output filter can be modeled by a third-order polynomial as $y = \alpha_1 x + \alpha_3 x^3$, where x and y are

the input and output of the filter, respectively, α_1 is its linear gain and α_3 is the third-order non-linear coefficient, then the output response to signal 2.3 can be expressed as:

$$\begin{aligned}
 y(nT_s) = & \frac{\sqrt{3}}{2} \left(\alpha_1 A + \frac{3}{4} \alpha_3 A^3 \right) \sin(2\pi f_0 nT_s) \\
 & \frac{1}{2} \left(\alpha_1 A + \frac{3}{4} \alpha_3 A^3 \right) \cos \left(2\pi \left(\frac{f_s}{2} - f_0 \right) nT_s \right) \\
 & - \frac{1}{4} \alpha_3 A^3 \cos \left(2\pi \left(\frac{f_s}{2} - 3f_0 \right) nT_s \right)
 \end{aligned} \tag{2.5}$$

According to (2.5), the output signal does not present third-order harmonic distortion, but two additional tones appear at frequencies $\frac{f_s}{2} - f_0$ and $\frac{f_s}{2} - 3f_0$. Roughly speaking, the third-order distortion component is shifted to higher frequencies, far from the main tone, where it can be easily attenuated by the output filtering. The presented algorithm can be generalized to cancel sets of harmonic components by time-interleaving appropriate time-shifted versions of the original sinusoid [53, 52].

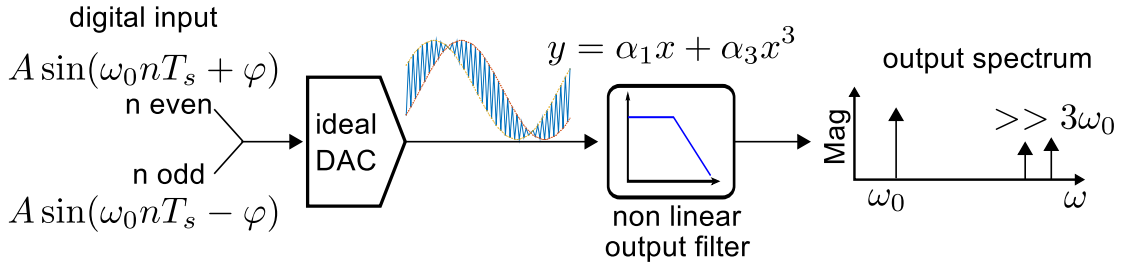


Figure 2.17: Conceptual block diagram of the distortion shaping technique.

Although experimental results on AWGs have been presented in [53, 52], featuring an attenuation of 85 dBc of the third order harmonic components at 1 MHz, implementing this technique on-chip may be challenging, as it rely on a complete DAC for signal generation.

2.6 Spectral manipulation techniques for on-chip signal generators: Harmonic cancellation versus distortion shaping

In the contest of this thesis, it is particularly interesting to explore the performance of the state-of-the-art spectral manipulation techniques for the implementation of

efficient and accurate on-chip sinusoidal signal generators. In this section, we present and discuss a direct comparison between the two previously presented spectral manipulation techniques, i.e, harmonic cancellation and distortion shaping. For the sake of the discussion, and in order to provide a fair comparison, in this section we explore the implementation of these techniques to the efficient open-loop generator described in [39], as a basic generator, able to generate a high quality sinusoidal stimulus with reduced circuitry resources while relaxing its design constraints. As it was described in the previous section 2.3.3.2, the basic generator is mainly a low-order filter whose gain has been made programmable by connecting and disconnecting carefully weighted devices to its input path. Applying the proposed harmonic cancellation techniques to this generator only requires to modify the input array of programmable devices at the generator input. As a practical example of the described generator, Fig. 2.18 shows a practical implementation based on a switched-capacitor second-order low-pass filter whose input capacitor has been replaced by an array of nine programmable capacitors that can be connected or disconnected to the signal path according to the set of digital control signals c_x . The nine input capacitors have been matched to generate the steps of a 36-level step-wise sinusoid. An input DC reference provides control on the amplitude of the generated signal.

It is worth to notice that by carefully selecting the number of elements in the array of programmable input capacitors, the basic generator and the two proposed harmonic cancellation techniques can be implemented simply by modifying the digital control signals. Thus, the basic generator is achieved by programming the input array to connect to the signal path the sequence of capacitors C_n^{basic} given by

$$C_n^{basic} = C_I \sin\left(n \frac{2\pi}{36}\right) \quad n = 0, 1, 2, \dots \quad (2.6)$$

where negative values are achieved by inverting the input DC reference, and the zero is achieved by connecting both positive and negative signal paths to the common mode. In the same way, harmonic cancellation for the third harmonic component can be achieved by connecting the sequence of capacitors C_n^{HC} given by

$$C_n^{HC} = C_I \sin\left(n \frac{2\pi}{36}\right) + C_I \sin\left((n-4) \frac{2\pi}{36}\right) + C_I \sin\left((n+4) \frac{2\pi}{36}\right) \quad n = 0, 1, 2, \dots \quad (2.7)$$

which is analogous to the harmonic cancellation strategy with phase-shifts of $\pm 2\pi/9$. This phase-shift cancels the third harmonic component.

Equivalently, distortion-shaping for the third-order harmonic component can be easily achieved by connecting to the signal path the sequence C_n^{DS} given by

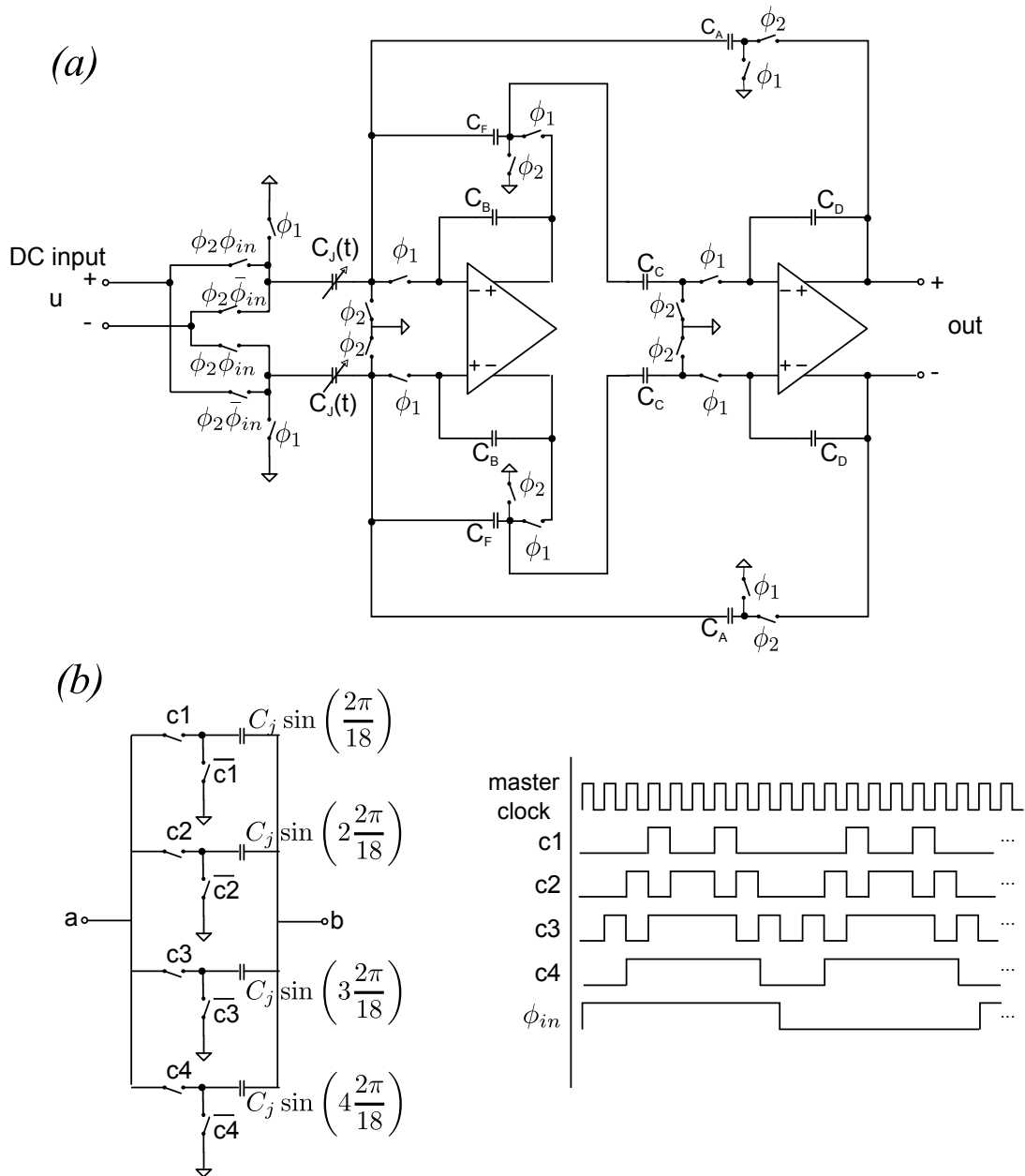


Figure 2.18: Switched-capacitor implementation of the sinusoidal signal generator: (a) Schematic view of the SC generator, (b) Programmable array of input elements.

$$C_n^{DS} = \begin{cases} C_I \sin\left(\left(n+3\right)\frac{2\pi}{36}\right) & n \text{ is even} \\ C_I \sin\left(\left(n-3\right)\frac{2\pi}{36}\right) & n \text{ is odd} \end{cases} \quad (2.8)$$

which is analogous to (2.3) with two time-interleaved signals with phase-shifts of $\pm\pi/6$.

In order to analyze the performance and design trade-offs of the considered generator with harmonic cancellation techniques, we have developed a behavioral model of the proposed generator to explore the effects of the main non-idealities affecting the spectral purity of the generated signal. It should be clear that in any practical implementation, the main performance limitations are given by the realization of precise step-levels at the input array of programmable elements, the spectral response of the filter, the non-linearity of the filter and the effectiveness of the harmonic cancellation techniques. In this work we evaluate the performance of the proposed generator and harmonic cancellation techniques in terms of THD. Our analysis considers a generator based on a second-order low-pass filter whose input element has been replaced by an array of 9 sine-weighted elements, similar as the one depicted in Fig. 2.18. The corner frequency of the filter has been designed to be coincident with the frequency of the generated sinusoid, so harmonic components are placed in the rejection band and are attenuated by the filtering. The quality factor of the filter has been set to $Q = 5$, which is a relatively low value that can be efficiently implemented. Finally, assuming a fully-differential implementation and weak non-linearity conditions, the non-linearity of the filter has been modeled as a third-order polynomial in the form:

$$x_{out}(n) = \alpha_1 x_{in}(n) + \alpha_3 x_{in}^3(n) \quad (2.9)$$

In order to compare the performance of the basic generator and the proposed harmonic cancellation schemes, we have performed statistical behavioral simulations considering random errors affecting the sine-weighted input elements. In a particular implementation, these errors will emerge from mismatches between devices, process variations, etc. Figure. 2.19 and Fig. 2.20 show the average performance of the generators under study obtained after 1000 runs of the experiment for two different experiments. Figure 2.19 shows the average THD as a function of the error level in the input elements when the coefficients are fixed to $\alpha_1 = 1$ and $\alpha_3 = 10^{-4}$ (in normalized amplitude units). Error bars in the figure show the obtained $\pm 1\sigma$ variation interval for each point. As it can be seen, in this weak non-linearity scenario, the generator with harmonic cancellation offers a consistently better performance in terms of THD than the basic generator, in line with the findings published in [42], while the generator with distortion shaping yields a higher and fairly constant THD in the whole considered variation range.

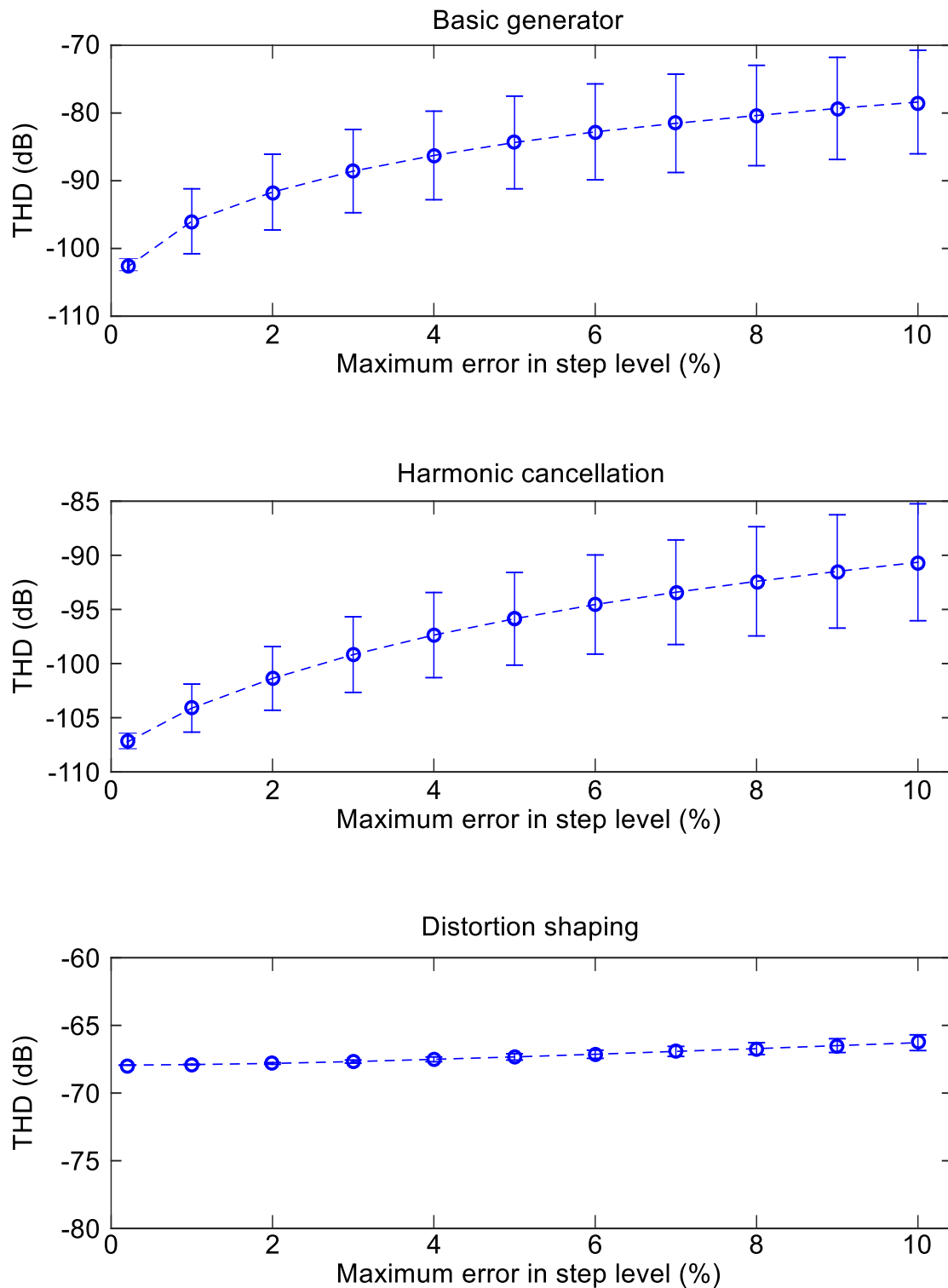


Figure 2.19: Average THD of the output sine-wave versus maximum error level in the input elements for the generation techniques with and without spectral manipulation, with $\alpha_1 = 1$ and $\alpha_3 = 10^{-4}$.

On the other hand, Fig. 2.20 shows the obtained average THD performance as a function of the non-linearity coefficient α_3 , when the maximum random error in the levels is fixed to 1% and $\alpha_1 = 1$. As it can be observed, again the generator with harmonic cancellation shows a performance advantage over the basic generator. Strikingly, the generator with distortion shaping shows a higher and constant THD in the whole explored range. The apparently limited performance of the distortion shaping algorithm applied to the proposed generation scheme can be explained by evaluating the spectral components in the output signal. According to equation 2.5, the distortion shaping algorithm cancels the third-order harmonic distortion component in the output signal, but it also produces two tones at frequencies $17f_o$ and $15f_o$, where f_o is the fundamental frequency of the generated sinusoid, with magnitudes around -5 dB and -11 dB with respect to the magnitude of the fundamental, respectively. These two tones are subsequently attenuated by the -40 dB/dec roll-off of the second-order low-pass filter rejection band. However, in our case study, these two high-frequency tones are still too close to the fundamental to be significantly attenuated by the low-pass filter. Increasing the number of steps in the input array will move these tones to higher frequencies where they will be effectively attenuated, but that increases the complexity of the design. There is a clear design trade-off for distortion shaping generators between the number of steps, that is, the number of samples per period in the input step-wise signal, and the order of the output filter.

The dispersion on the THD values in Fig. 2.19 and 2.20 is relatively high for the basic and harmonic cancellation generators. To get more insight into this issue, Fig. 2.21.a shows the histograms of the obtained THD for these generation schemes when the maximum error in the steps is set to 1%, $\alpha_1 = 1$ and $\alpha_3 = 10^{-4}$ (again, α_1 and α_3 are expressed in normalized amplitude units). As it can be observed, the THD histograms for the basic and harmonic cancellation generators have a significant overlap. However, it should be expected that the THD of the generators with and without cancellation are highly correlated. To get more insight into this issue, Fig. 2.21.b shows the histogram of the THD improvement obtained by harmonic cancellation for the 1000 simulated instances. It is observed that the THD improvement is always positive, while its median value is around 12 dB. It is also interesting to notice that the inclusion of weak non-linearity in the filter yields a different behavior for the THD improvement due to harmonic cancellation than the one reported in [42], obtained for linear filtering conditions. Although the average THD improvement is similar in both cases, the inclusion of non-linear filtering reduces the minimum improvement that we can expect.

2.6 Spectral manipulation techniques for on-chip signal generators: Harmonic cancellation versus distortion shaping

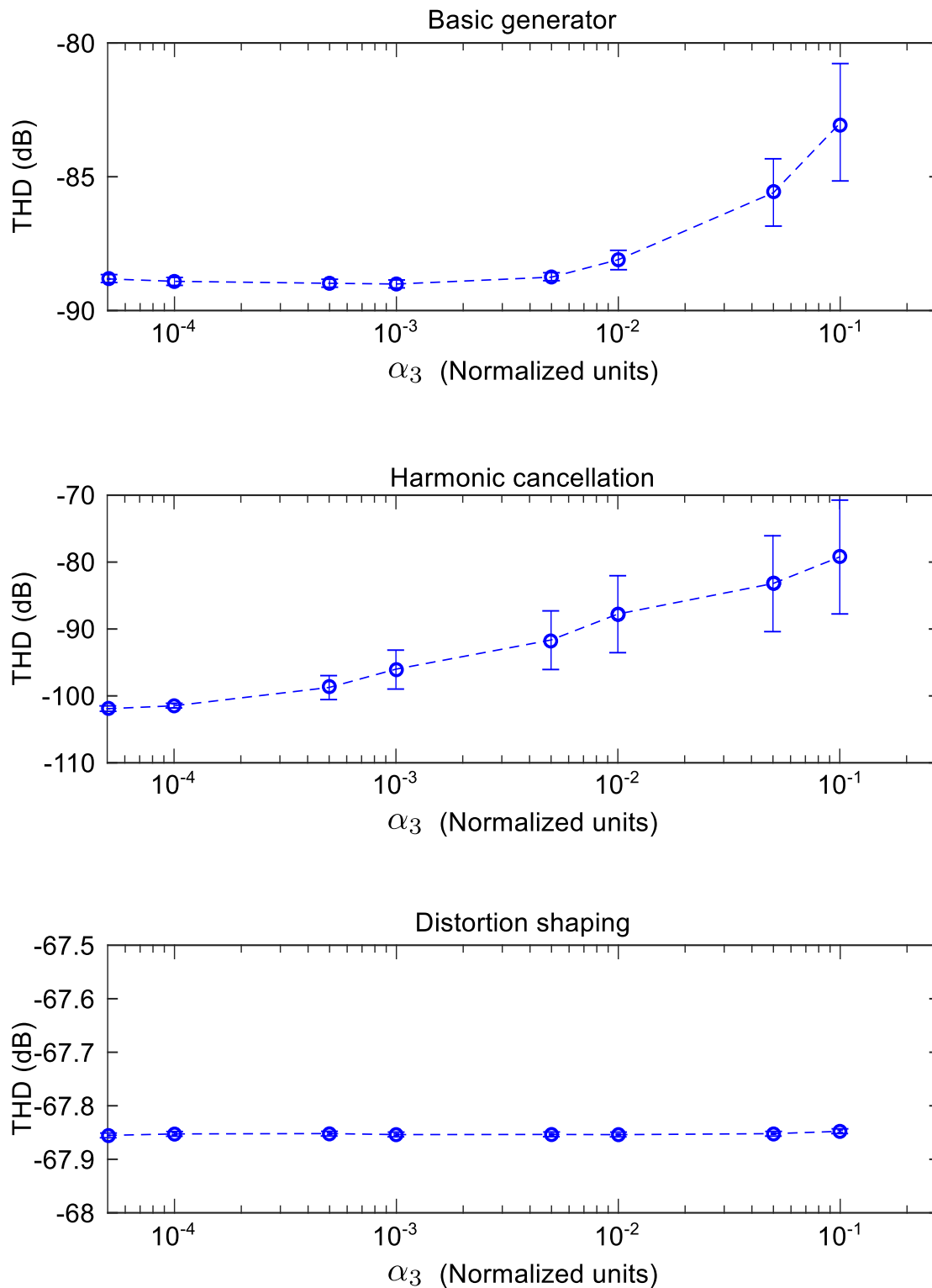


Figure 2.20: Average THD of the output sine-wave versus third-order non-linearity coefficient in the output filter for the generation techniques with and without spectral manipulation, with $\alpha_1 = 1$ and maximum error in step level at 1%.

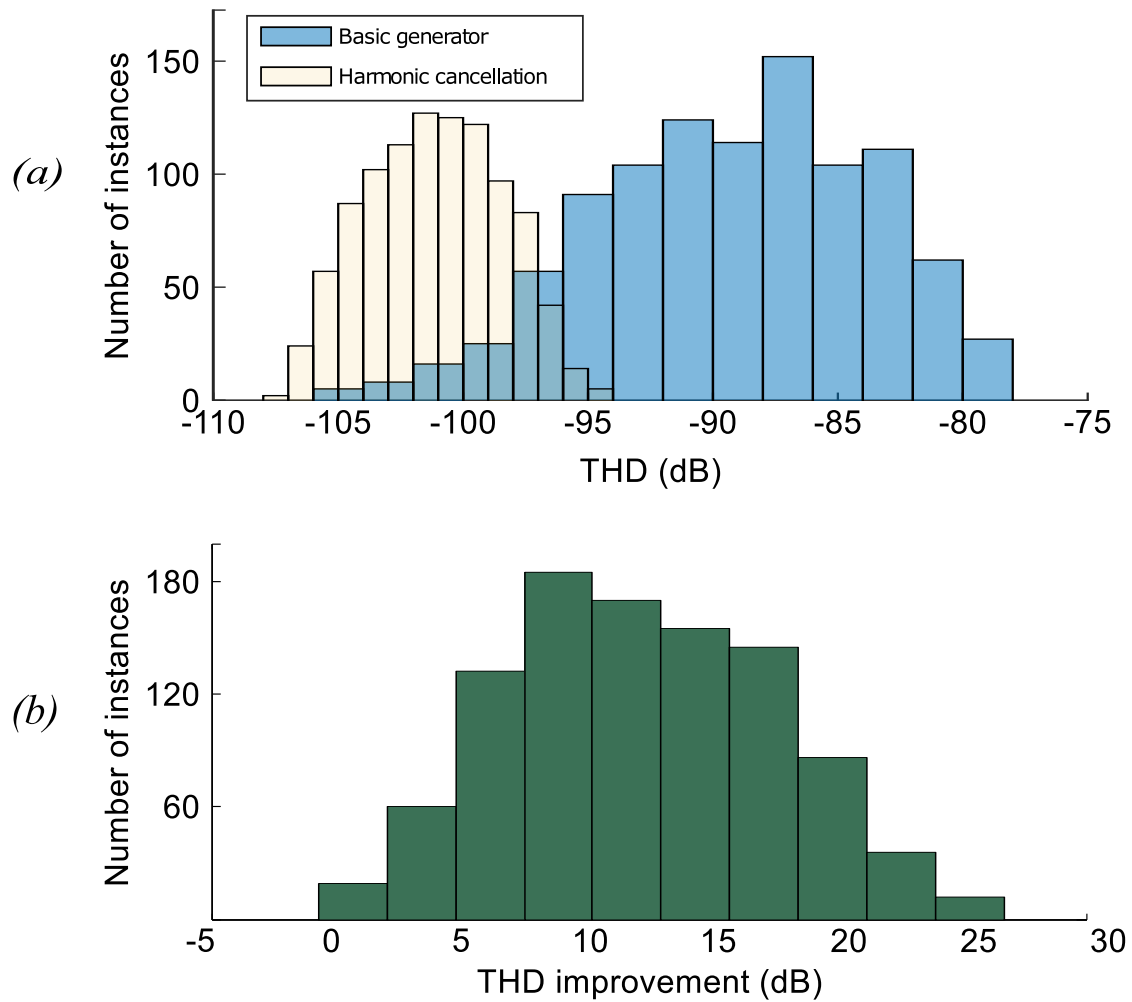


Figure 2.21: (a) Obtained THD for the 1000 generator instances, with and without harmonic cancellation; (b) THD improvement due to the harmonic cancellation.

Chapter 3

Harmonic cancellation techniques using digital resources

3.1 Introduction

The strong trade-off between the spectral purity of the generated analog stimulus and the design complexity of the analog signal generators has been always the most critical key element for the design of on-chip sine-wave generators for analog and mixed signal BIST, specially when high performances are required such as high frequency operation, high resolution of the stimulus and low THD. A common challenge of the previously proposed analog signal generator designs, as presented in the previous chapter, is the design of the output filter. Designers are always aimed at integrating highly linear filters with low cut-off frequencies in order to attenuate all unwanted harmonic components, which is a time and effort consuming task. For this reason, some advanced works explore novel strategies, based on harmonic cancellation techniques, able to build analog signals that do not contain a number of low order harmonic components before feeding the output filter. Thus the specifications of the output filter will be relaxed because it will be used to filter only high-order distortion harmonic components.

In this chapter, we are going to detail the theoretical basis of harmonic cancellation. We will present four harmonic cancellation techniques able to suppress a number of low-order unwanted harmonic components at the same time, using different types of scale weights to build robust sinusoidal signal synthesizers. The feasibility of our proposals will be shown through an example of implementation that can be generalized for all techniques, based on digital resources. Finally the efficiency of the different harmonic cancellation strategies will be demonstrated by simulations of behavioral models.

3.2 Theoretical basis

Harmonic cancellation is based on manipulating and linearly combining a number of periodic signals, with different amplitudes and phase-shifts, to provide a periodic signal in which a number of selected harmonic components are attenuated or completely canceled in the frequency domain.

Let us consider a generic periodic signal $x(t)$ expressed as a Fourier series expansion as:

$$x(t) = \sum_{k=1}^{\infty} A_k \cos(k\omega_0 t + \varphi_k) \quad (3.1)$$

where A_k and φ_k are the amplitude and phase of harmonic component k in signal $x(t)$, respectively, and ω_0 is the fundamental frequency of $x(t)$.

Without loss of generality, let us define signal $y(t)$ as the linear combination of signal $x(t)$ scaled by a factor α_0 and p pairs of scaled and shifted signals with opposite time-shifts Δt_i and $-\Delta t_i$ with respect to signal $x(t)$ and scaled by a factor α_i ,

$$y(t) = \alpha_0 x(t) + \sum_{i=1}^p \alpha_i [x(t + \Delta t_i) + x(t - \Delta t_i)] \quad (3.2)$$

From equations (A.1) and (A.2) it can be derived,

$$y(t) = \sum_{k=1}^{\infty} A_k \left[\alpha_0 + 2 \sum_{i=1}^p \alpha_i \cos(k\phi_i) \right] \cos(k\omega_0 t + \varphi_k) \quad (3.3)$$

where $\phi_i = \omega_0 \Delta t_i$.

Thus, the combination of a periodical signal and its scaled and phase-shifted versions has a spectral content which is that of the original periodic signal but scaled by coefficients $[\alpha_0 + 2 \sum_{i=1}^p \alpha_i \cos(k\phi_i)]$. In other words, by selecting an appropriate set of phase shifts ϕ_i and scale weights α_0 and α_i such as these coefficients are small for given values of k , unwanted harmonic components in $y(t)$ can be attenuated or completely canceled.

Several types of periodic signals can be exploited by the harmonic cancellation technique for building highly-linear sinusoidal signal such as sawtooth, triangular signal and square-waves. The selected signal, for a practical implementation of the harmonic cancellation technique, should satisfy a trade-off between the simplicity of implementation and its spectral response. Moreover, in this thesis we will also focus on the feasibility of the implementation using digital resources. The spectrum response of the sawtooth wave, as shown in Fig. 3.1.a contains both odd- and even-order harmonic components which make it not preferable to use for

harmonic cancellation. The triangular wave, as shown in Fig. 3.1.b, has a spectrum including only odd-order harmonic components and their magnitudes are inversely proportional to square of harmonic order. However from a practically point of view, this type of signals can not be easily implemented with digital resources. The square-wave signal with a duty-cycle of 50%, presented in Fig. 3.1, is very convenient for harmonic cancellation not only because its spectrum contains only odd-order harmonic components whose magnitude decreases as their frequency increases, but also because this signal may be easily generated digitally with a simple digital synthesizer.

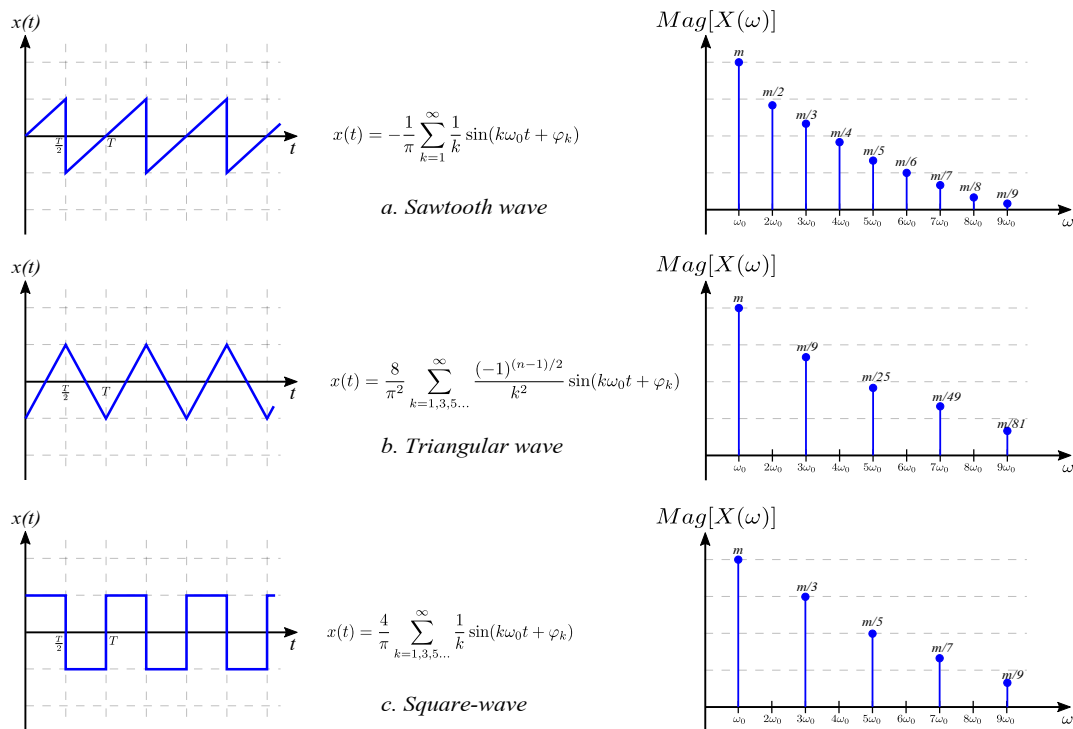


Figure 3.1: Temporal forms and spectra of periodic signals

3.3 Practical implementation

Similarly to [50, 54, 46], we propose to apply the described harmonic cancellation technique to a set of digital square-waves to produce a high-quality analog sinusoidal signal, as it is conceptually shown in Fig. 3.2. Thus, we have to combine p pairs of scaled and delayed versions of a square-wave, as defined in (A.3). And according to (A.3), in order to cancel the k -th harmonic component, we have to

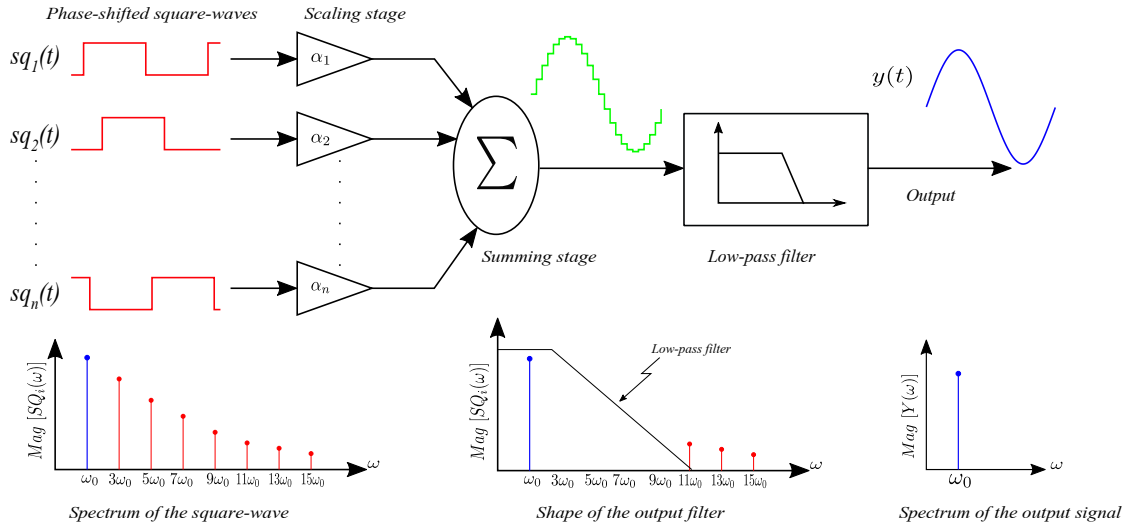


Figure 3.2: Harmonic cancellation based generator.

find the phase-shifts ϕ_i and weights α_0 and α_i that verify the harmonic cancellation condition:

$$\alpha_0 + 2 \sum_{i=1}^p \alpha_i \cos(k\phi_i) = 0 \quad (3.4)$$

Based on the analytical results presented in the previous section, we propose a simple hardware architecture in order to implement an efficient sinusoidal signal generator using digital square-wave signals and the described harmonic cancellation technique. The proposed architecture was presented in [54, 55] and it is illustrated in Fig. 3.3. It features a digital generator that provides a set of time delayed digital square-waves, a weighting stage to scale and combine the different square-wave phases, and a simple low-pass filter to filter high-order harmonic components in the output. The selected generator should be designed to provide two fully differential outputs in such a way that all even-harmonic components will be absent and the harmonic cancellation technique will be used to suppress only odd-order harmonics.

3.3.1 Digital shift register

The core of the generator is a circular shift-register with N flip-flops that provides delayed versions of a binary waveform where the delay can be modified directly by adjusting the number of flip-flops. The frequency of the output signal may be tuned by varying the frequency of the clock pulse applied to the register. The shift-register is loaded at the beginning of the operation by $N/2$ consecutive logic

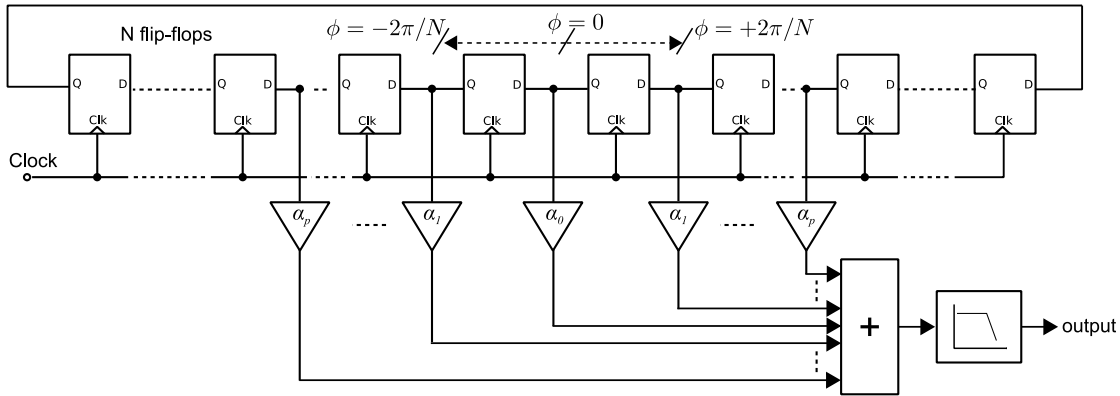


Figure 3.3: Block diagram of the proposed sinusoidal signal generator.

zeros followed by $N/2$ consecutive logic ones as shown in Fig. 3.4. When the circular shift-register is driven by a clock signal at frequency f_{clk} , the output of each flip-flop is a square-wave signal with a 50% duty-cycle and frequency f_{clk}/N . By construction, the phase-shift between two consecutive outputs in the circular shift-register is $2\pi/N$, which allows an easy implementation of the required phase-shifts just by properly adjusting the number of flip-flops N in the register and selecting the appropriate flip-flop output in the shift-register.

3.3.2 Weighting stage

The set of selected phase-shifted square-waves from the shift-register are conveniently scaled and summed to generate a sinusoidal output. The scaling technique should be selected carefully in order to provide the ideal ratios defined by the harmonic cancellation condition according to (A.4). Different practical implementations of the scaling and summing node have been proposed in the literature, including weighted resistor networks [45, 46, 54] as shown in Fig. 3.5, weighted current sources [55], as depicted in Fig. 3.6, and complete current-steering DACs [50].

Mismatch and process variations can impact the scale weight factors in the weighting stage which causes the degradation of the performances of harmonic cancellation, as it will be demonstrated later in this chapter. For this reason, some scale weight compensation techniques can be used such as the compensation resistor network as presented in [54] when the scaling stage is based on resistor network. In the case when the scaling stage is designed as weighted current sources, we introduced in [55] a calibration technique which consist of using compensation capacitors to control the amount of current provided by the current sources. The current-steering DAC used in [50] to scale the weight ratios also uses the Dynamic

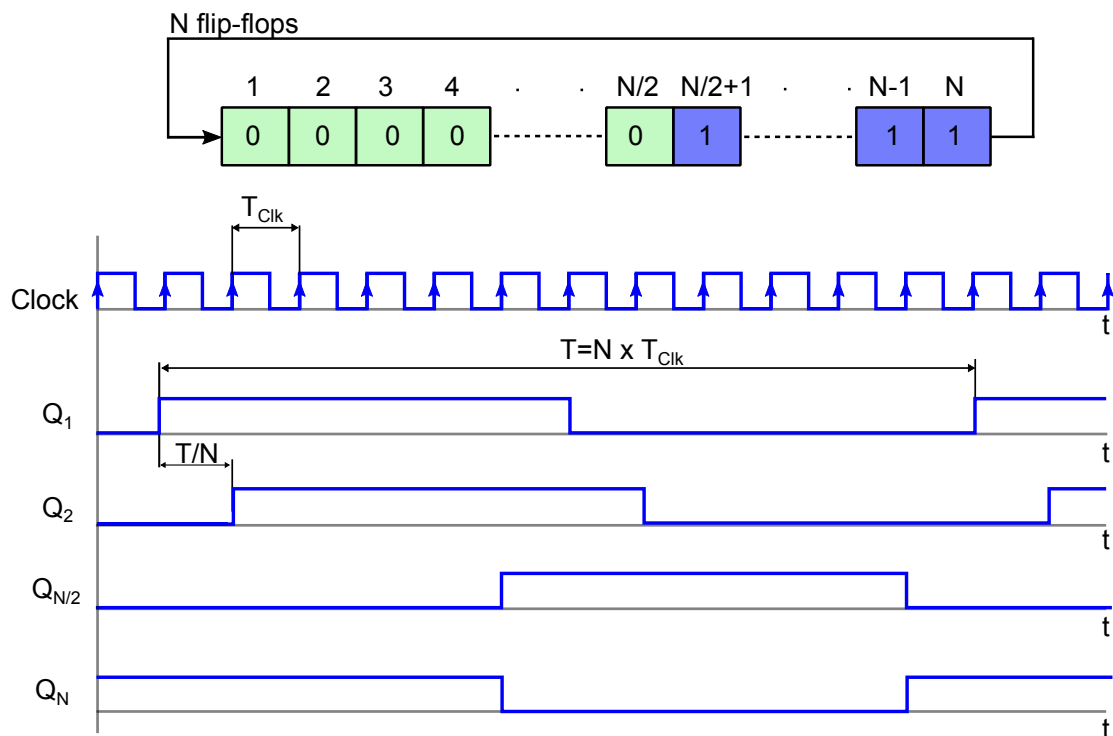


Figure 3.4: Chronogram of the digital shift-register outputs.

Element Matching (DEM) technique in order to increase its linearity impacted by mismatch and process variations.

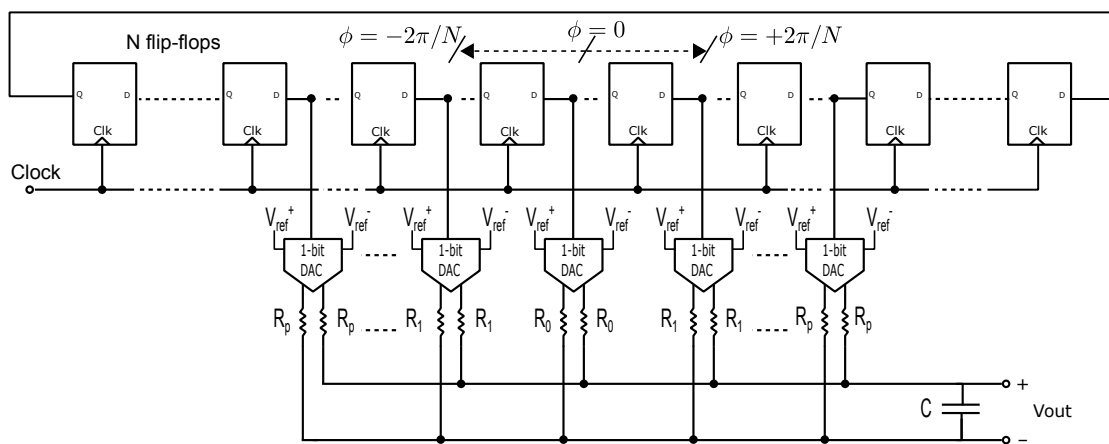


Figure 3.5: Implementation based on weighted resistor network.

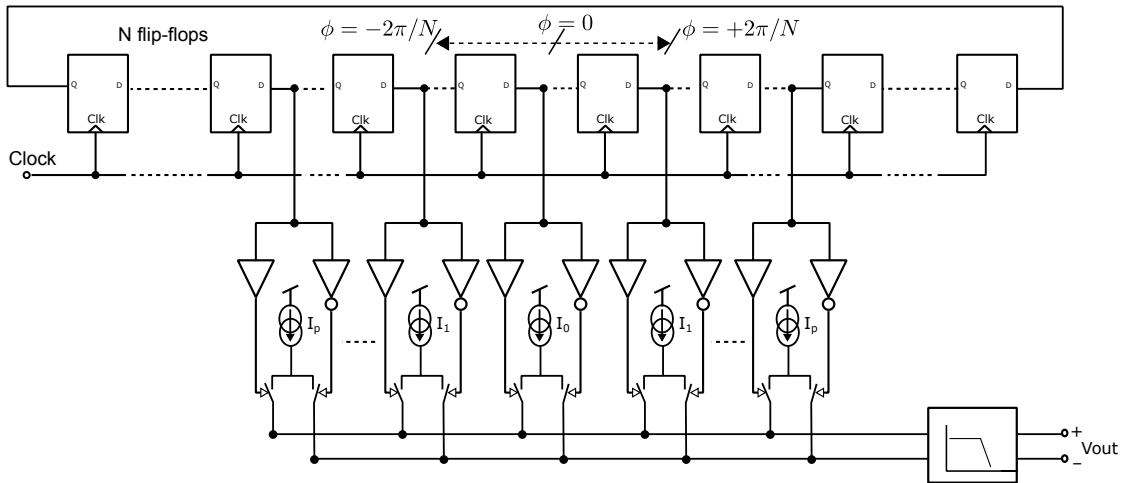


Figure 3.6: Implementation based on current sources.

3.3.3 Filtering stage

The combination of the delayed and scaled square-waves, with the appropriate harmonic cancellation coefficients, produces a sinusoidal signal in which a set of low-order harmonic components is suppressed. This signal will be fed to a simple passive low-pass filter with low-order to attenuate higher-order harmonic components not affected by the harmonic cancellation strategy, as shown in Fig 3.7. The linearity of the filter is critical in order to not introduce any unwanted distortion harmonics.

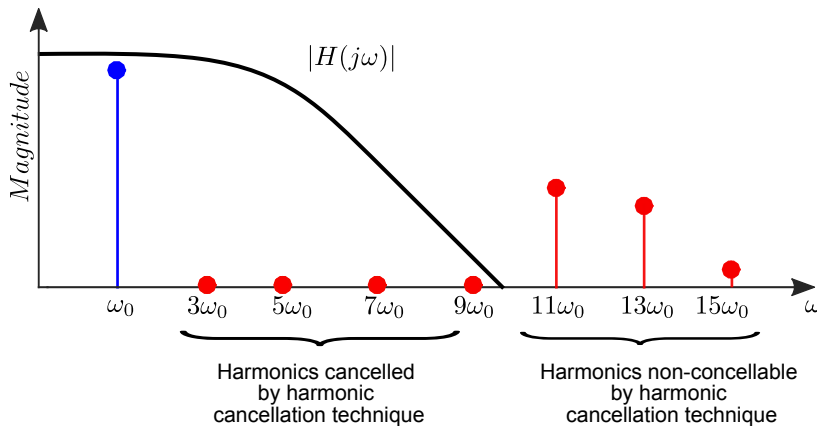


Figure 3.7: Low-pass filter response.

In this chapter we explore multiple solutions for the practical implementation of the harmonic cancellation condition (A.4), leading to different harmonic cancellation techniques. The selection of the harmonic cancellation coefficients α_i and ϕ_i

is a critical step to define the appropriate harmonic cancellation technique with regard to three main features:

- The satisfaction of the harmonic cancellation condition in (A.4)
- The simplicity of the implementation of the scale weight ratios α_i
- The simplicity of the implementation of the phase-shift ϕ_i

Thus, we analyze in the following sections four harmonic cancellation techniques that may be applied for designing on-chip sinusoidal signal generators for BIST applications. The described techniques are classified based on the nature of the necessary scale-weight ratios and the number of signals to be used.

3.4 Harmonic cancellation with unitary scale weight ratios using odd number of signals

Let us consider signal $y_1(t)$ defined as signal $y(t)$ in A.2 but with weights $\alpha_0 = 1$, $\alpha_1 = 1$, and $p = 1$ as:

$$\begin{aligned} y_1(t) &= x(t) + x(t + \Delta t_1) + x(t - \Delta t_1) \\ &= \sum_{k=1}^{\infty} A_k [1 + 2 \cos(k\phi_1)] \cos(k\omega_0 t + \varphi_k) \end{aligned} \quad (3.5)$$

with the same notation defined in section (3.2). In this configuration, it is easy to demonstrate that the third-harmonic component of the original signal $x(t)$ can be easily canceled by setting $\phi_1 = 2\pi/9$ as:

$$\begin{cases} 1 + 2\cos(k\frac{2\pi}{9}) = 0 & k = 3 \\ 1 + 2\cos(k\frac{2\pi}{9}) \neq 0 & k = 1 \end{cases} \quad (3.6)$$

Let us iterate the same process and define now signal $y_2(t)$ as the linear combination of the signal $y_1(t)$ and two phase-shifted versions of $y_1(t)$ with opposite delays $\pm\Delta t_2$ as:

$$\begin{aligned} y_2(t) &= y_1(t) + y_1(t + \Delta t_2) + y_1(t - \Delta t_2) \\ &= \sum_{k=1}^{\infty} A_k [1 + 2 \cos(k\phi_1)] [1 + 2 \cos(k\phi_2)] \cos(k\omega_0 t + \varphi_k) \end{aligned} \quad (3.7)$$

3.4 Harmonic cancellation with unitary scale weight ratios using odd number of signals

Again, as it can be observed, a new harmonic cancellation condition appears $[1 + 2\cos(k\phi_1)] \times [1 + 2\cos(k\phi_2)] = 0$ and two harmonic components can be canceled by carefully selecting variables ϕ_1 and ϕ_2 . For instance, the third- and fifth-order harmonic components can be canceled by setting $\phi_1 = 2\pi/9$ and $\phi_2 = 2\pi/15$ as:

$$\begin{cases} [1 + 2\cos(k\frac{2\pi}{9})] [1 + 2\cos(k\frac{2\pi}{15})] = 0 & k = 3 \text{ and } 5 \\ [1 + 2\cos(k\frac{2\pi}{9})] [1 + 2\cos(k\frac{2\pi}{15})] \neq 0 & k = 1 \end{cases} \quad (3.8)$$

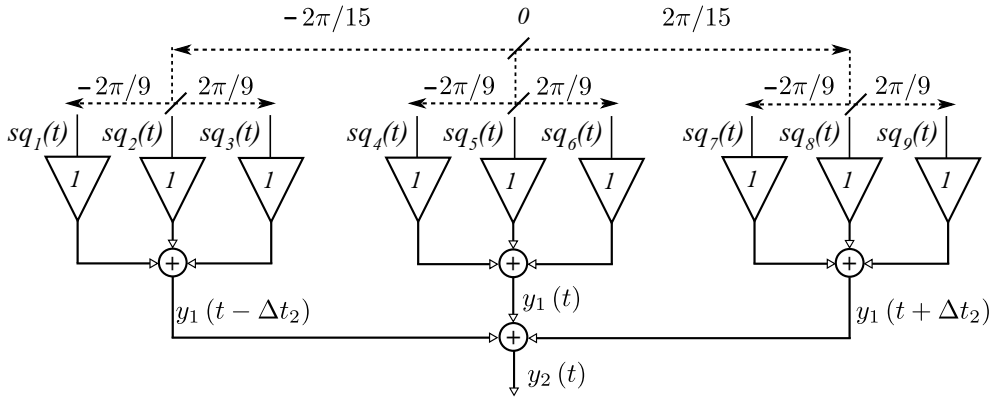


Figure 3.8: Conceptual block diagram of the harmonic cancellation strategy using integer scale weight ratios and even number of signals to cancel the 3rd and 5th order harmonic components.

This operation requires the use of 9 square-waves $sq_1(t)$ to $sq_9(t)$ distributed in three sets of three signals, where the relative phase-shift between signals from the same set $\phi_1 = 2\pi/9$ and the phase-shift between the sets $\phi_2 = 2\pi/15$, as it is schematically presented in Fig. 3.8. The suppression of the third- and fifth-order harmonic components in the spectrum of the output signal $y_2(t)$ is illustrated by the vector phase diagrams shown in Fig. 3.9. These polar diagrams show the phase and magnitude of the third- and fifth-order harmonic component vectors, plotted in blue and red respectively, of the original square-waves used to build the intermediate signals $y_1(t - \Delta t_2)$, $y_1(t)$ and $y_1(t + \Delta t_2)$, with the notation in Fig. 3.8. Again, it can be observed that the combination of third-order harmonic vectors (in blue) in each set results in a null vector, while for the fifth-order harmonic the combination of the three sets also results in a null vector (for clarity, the resultant fifth-order harmonic vector is represented in green for each of the sets).

Figure.3.10 shows a block diagram of a signal generator based on this harmonic cancellation strategy with built-in cancellation of the third and fifth harmonic

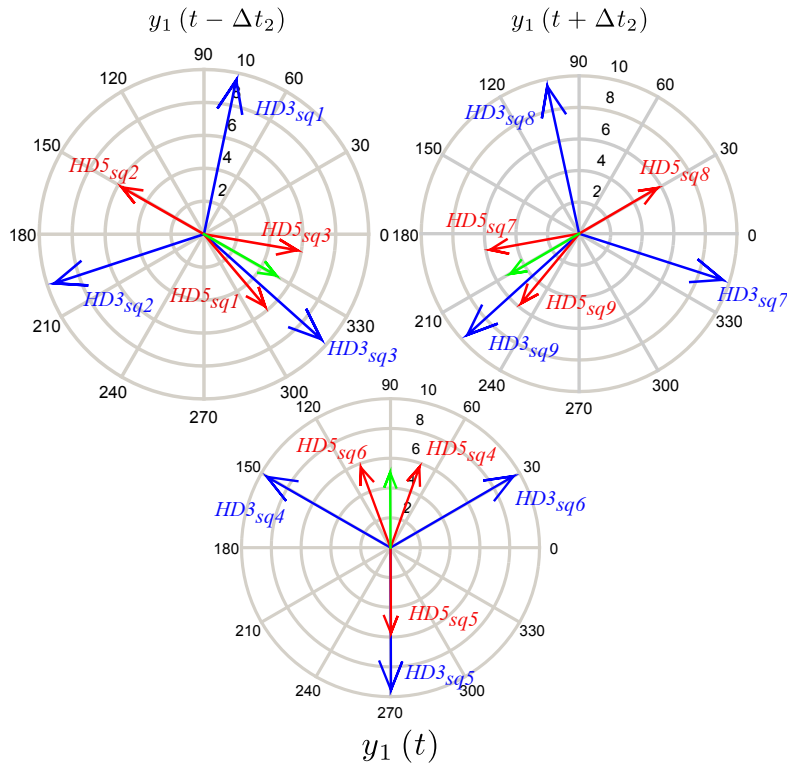


Figure 3.9: Phase vector diagram of the harmonic cancellation strategy using integer scale weight ratios and even number of signals to cancel the 3^{rd} and 5^{th} order harmonic components.

components. The required phase-shifts can be achieved using a shift-register with 90 flip-flops, initially loaded to 45 consecutive logic ones and 45 consecutive logic zeros. The scale factors in all signal paths are made equal (i.e., unitary ratios), which further relaxes the design effort for improving the matching of the different signal paths. As an example, Fig. 3.11 shows the waveform of the step-level sine-wave provided by combination of the delayed and square-waves with unitary amplitude, the final signal in the output of the first-order filter and the spectrum of the final signal where the cancellation of the third- and fifth-harmonic components is clearly depicted. Results were obtained by behavioral simulations in MATLAB of the generator in Fig. 3.10 under ideal conditions.

This harmonic cancellation strategy can be generalized to cancel any number of harmonics. If we iterate the process p times, the resulting signal $y_p(t)$ can be written as:

3.4 Harmonic cancellation with unitary scale weight ratios using odd number of signals

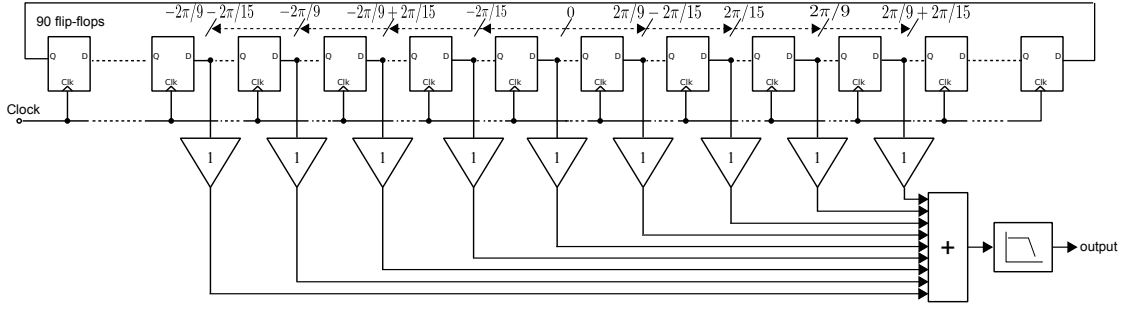


Figure 3.10: Block diagram of the proposed sinusoidal signal generator using 9 signal phases and unitary scale weights to cancel the third-, and fifth-order harmonic components.

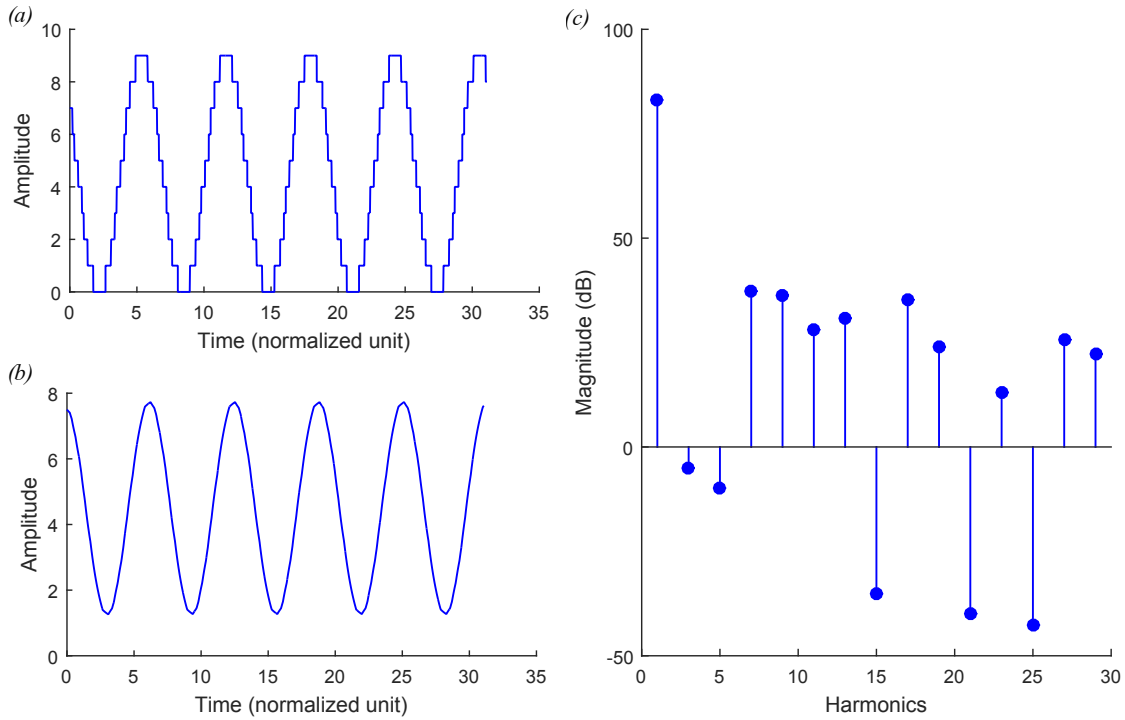


Figure 3.11: (a) Waveform of the step-level sinusoidal signal; (b) waveform of the generated sine-wave (c) spectrum of the generated sine-wave.

$$\begin{aligned}
 y_p(t) &= y_{p-1} + y_{p-1}(t + \Delta t_p) + y_{p-1}(t - \Delta t_p) \\
 &= \sum_{k=1}^{\infty} A_k \prod_{i=1}^p [1 + 2 \cos(k\phi_i)] \cos(k\omega_0 t + \varphi_k)
 \end{aligned} \tag{3.9}$$

And the resulting cancellation condition for a given harmonic k lower than $2p+1$

can be expressed as:

$$\prod_{i=1}^p [1 + 2 \cos(k\phi_i)] = 0 \quad (3.10)$$

This harmonic cancellation strategy simplifies the implementation of scale weights by making them equal, however it requires a longer shift-register to provide the appropriate phase-shifts.

3.5 Harmonic cancellation with unitary scale weight ratios using even number of signals

In order to reduce the complexity of the digital phase-shifted square-waves synthesizer in the generator presented above, we present a similar harmonic cancellation strategy using unitary weight ratios with a reduced number of square-waves. Let us consider signal $y_1(t)$ defined as signal $y(t)$ in (A.2) but with weights $\alpha_0 = 0$, $\alpha_1 = 1$ and $p = 1$ as:

$$\begin{aligned} y_1(t) &= x(t + \Delta t_1) + x(t - \Delta t_1) \\ &= \sum_{k=1}^{\infty} 2A_k \cos(k\phi_1) \cos(k\omega_0 t + \varphi_k) \end{aligned} \quad (3.11)$$

with the same notation previously defined. In this configuration, a given harmonic component can be canceled by choosing an appropriate value of ϕ_1 . For instance, the third harmonic component can be canceled by setting $\phi_1 = \pi/6$ as:

$$\begin{cases} \cos(k\frac{\pi}{6}) = 0 & k = 3 \\ \cos(k\frac{\pi}{6}) \neq 0 & k = 1 \end{cases} \quad (3.12)$$

Similarly to the previous case, the process can be iterated. Let us define signal $y_2(t)$ as:

$$\begin{aligned} y_2(t) &= y_1(t + \Delta t_2) + y_1(t - \Delta t_2) \\ &= \sum_{k=1}^{\infty} 2^2 A_k \cos(k\phi_1) \cos(k\phi_2) \cos(k\omega_0 t + \varphi_k) \end{aligned} \quad (3.13)$$

In the resulting signal $y_2(t)$, the fifth-order harmonic component can be easily canceled by setting $\phi_2 = \pi/10$ and a new harmonic cancellation condition appears to cancel the third- and fifth- order harmonic components as:

$$\begin{cases} \left[\cos(k\frac{\pi}{6}) \right] \left[\cos(k\frac{\pi}{10}) \right] = 0 & k = 3 \text{ and } 5 \\ \left[\cos(k\frac{\pi}{6}) \right] \left[\cos(k\frac{\pi}{10}) \right] \neq 0 & k = 1 \end{cases} \quad (3.14)$$

This harmonic cancellation strategy can be implemented by combining four square-waves $sq_1(t)$ to $sq_4(t)$, as schematically shown in Fig. 3.12. These 4 square-waves are distributed into two sets of two square-waves with relative phase-shifts of $\pi/3$, while the phase-shift between the two sets is of $\pi/5$.

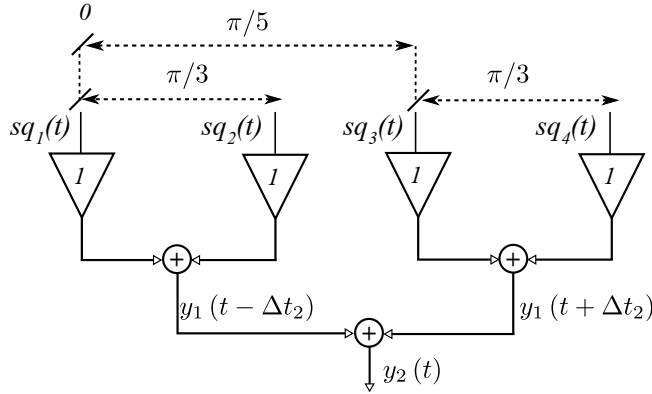


Figure 3.12: Conceptual block diagram of the harmonic cancellation strategy using integer scale weight ratios and even number of signals to cancel the 3rd and 5th order harmonic components.

The cancellation of the third- and fifth-order harmonic components is shown in the vector phase diagram in Fig. 3.13. These polar diagrams show the phase and magnitude of the third- and fifth-order harmonic component vectors, plotted in blue and red respectively, of the original square-waves used to build the intermediate signals $y_1(t - \Delta t_2)$, and $y_1(t + \Delta t_2)$, with the notation in Fig. 3.12. Again, it can be observed that the combination of third-order harmonic vectors (in blue) in each set results in a null vector, while for the fifth-order harmonic the combination of the two sets also results in a null vector (for clarity, the resultant fifth-order harmonic vector is represented in green for each of the sets).

Figure 3.14 shows a block diagram of a signal generator based on this harmonic cancellation strategy with built-in cancellation of the third- and fifth-order harmonic components. As in the previous strategy, the required phase-shifts can be easily achieved using a shift-register with 30 flip-flops, initially loaded to 15 consecutive logic ones and 15 consecutive logic zeros. The scale factors in all signal paths are made equal (i.e., unitary ratios), which further relaxes the design effort for improving the matching of the different signal paths. As an example, Fig. 3.15

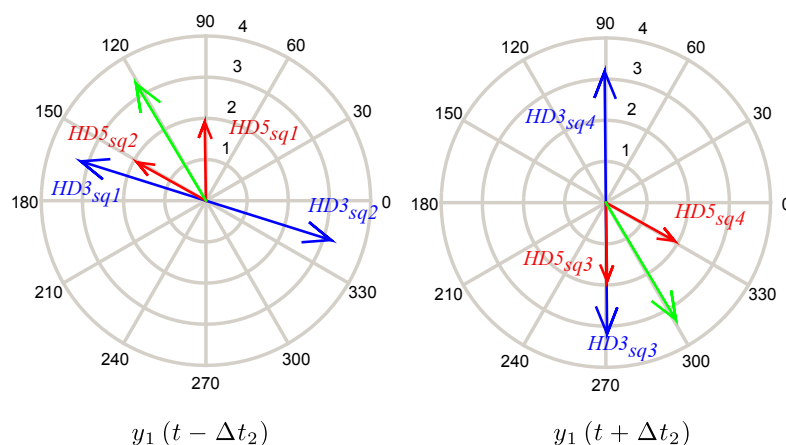


Figure 3.13: Phase vector diagram of the harmonic cancellation strategy using integer scale weight ratios and even number of signals to cancel the 3rd and 5th order harmonic components.

shows the waveform of the step-level sine-wave provided by combination of the delayed and scaled square-waves, the final signal in the output of the first-order filter and the spectrum of the final signal where the cancellation of the third- and fifth-harmonic components is clearly depicted. Results were obtained by behavioral simulations in MATLAB of the generator in Fig. 3.14 under ideal conditions.

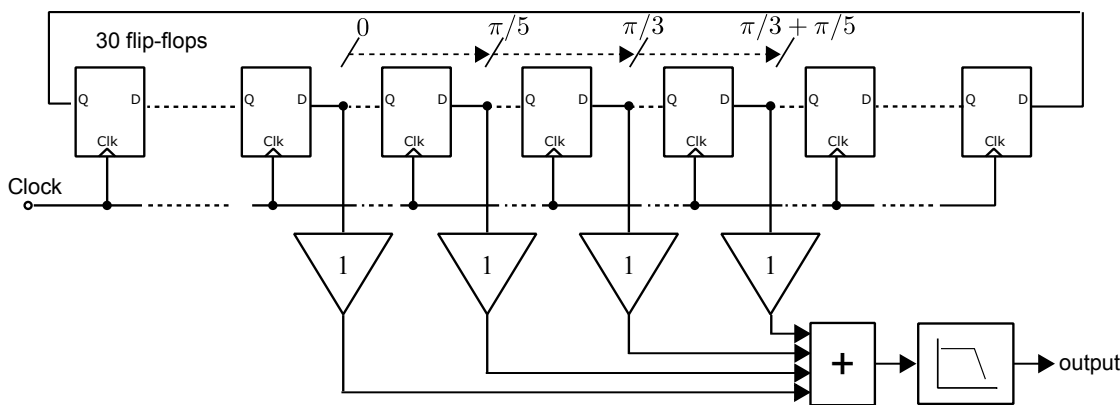


Figure 3.14: Block diagram of the proposed sinusoidal signal generator using four signal phases and unitary scale weights to cancel the third-, and fifth-order harmonic components.

Again, this harmonic cancellation strategy can be also generalized to cancel any number of harmonics. If we iterate the process p times, the resulting signal $y_p(t)$ can be written as:

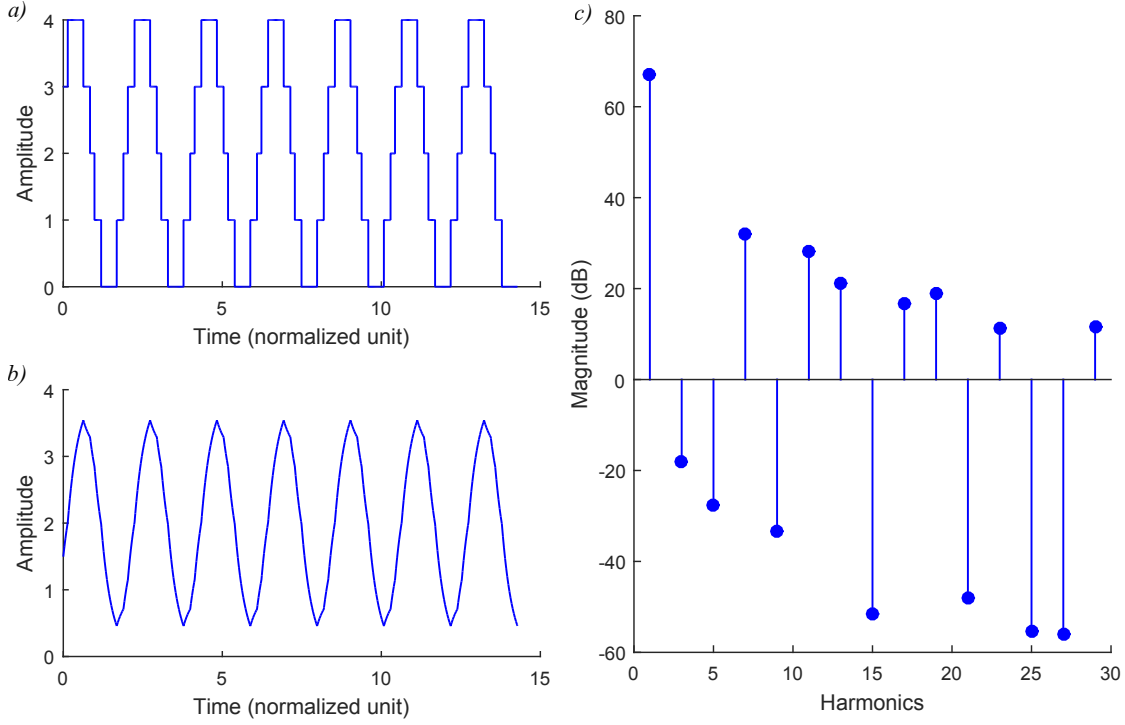


Figure 3.15: (a) Waveform of the step-level sinusoidal signal; (b) waveform of the generated sine-wave; (c) spectrum of the generated sine-wave.

$$\begin{aligned}
 y_p(t) &= y_{p-1}(t + \Delta t_p) + y_{p-1}(t - \Delta t_p) \\
 &= \sum_{k=1}^{\infty} 2^p A_k \prod_{i=1}^p \cos(k\phi_i) \cos(k\omega_0 t + \varphi_k)
 \end{aligned} \tag{3.15}$$

And the resulting cancellation condition for a given harmonic k can be expressed as:

$$\prod_{i=1}^p \cos(k\phi_i) = 0 \tag{3.16}$$

Similarly to the previous harmonic cancellation strategy, multiple harmonic components can be canceled using this design equation, at the cost of increasing the design complexity. However, it has to be noted that for this solution there is a risk of attenuating strongly the fundamental component if a high number of square-waves are combined, since the limit of the cancellation condition in (A.15) tends to zero as p increases.

3.6 Harmonic cancellation strategy with integer scale weight ratios

A similar strategy can be devised to achieve harmonic cancellation conditions using integer weight ratios for all the signal phases. Let us consider signal $y_1(t)$ defined as signal $y(t)$ in (A.2) but with weights $\alpha_0 = 2$, $\alpha_1 = 1$, and $p = 1$ as:

$$\begin{aligned} y_1(t) &= 2x(t) + x(t + \Delta t_1) + x(t - \Delta t_1) \\ &= \sum_{k=1}^{\infty} 2A_k [1 + \cos(k\phi_1)] \cos(k\omega_0 t + \varphi_k) \end{aligned} \quad (3.17)$$

In this configuration, the third harmonic component can be canceled by setting $\phi_1 = \pi/3$ as:

$$\begin{cases} 1 + \cos(k\frac{\pi}{3}) = 0 & k = 3 \\ 1 + \cos(k\frac{\pi}{3}) \neq 0 & k = 1 \end{cases} \quad (3.18)$$

Similarly to the previous case, the process can be iterated. Let us define signal $y_2(t)$ as:

$$\begin{aligned} y_2(t) &= 2y_1(t) + y_1(t + \Delta t_2) + y_1(t - \Delta t_2) \\ &= \sum_{k=1}^{\infty} 2^2 A_k [1 + \cos(k\phi_1)] [1 + \cos(k\phi_2)] \cos(k\omega_0 t + \varphi_k) \end{aligned} \quad (3.19)$$

In the resulting signal $y_2(t)$, the fifth-order harmonic component can be easily canceled by setting $\phi_2 = \pi/6$, and a new harmonic cancellation condition appears which is the product of the third-order harmonic cancellation condition and the fifth-order harmonic cancellation condition as

$$\begin{cases} [1 + \cos(k\frac{\pi}{3})] [1 + \cos(k\frac{\pi}{6})] = 0 & k = 3 \text{ and } 5 \\ [1 + \cos(k\frac{\pi}{3})] [1 + \cos(k\frac{\pi}{6})] \neq 0 & k = 1 \end{cases} \quad (3.20)$$

As it can be observed, by adding a new pair of delayed signals we can cancel two harmonic components of the original signal $x(t)$.

Similarly to the harmonic cancellation strategy with integer scale ratios presented in the previous section, we propose to implement the harmonic cancellation strategy with unitary scale ratios in the same way to cancel the third- and fifth-order harmonic components by setting $\phi_1 = \pi/3$ and $\phi_2 = \pi/5$. This solution

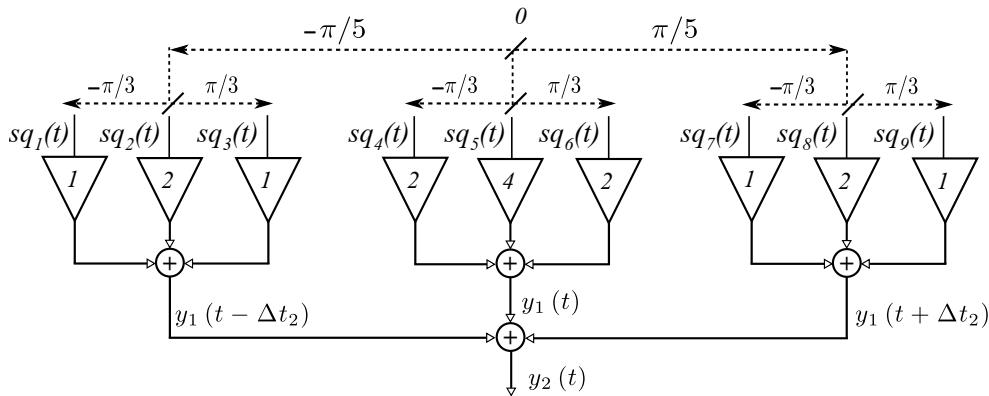


Figure 3.16: Conceptual block diagram of the harmonic cancellation strategy using integer scale weight ratios to cancel the 3rd and 5th order harmonic components.

employs a combination of 9 square-waves $sq_1(t)$ to $sq_9(t)$, as it is schematically shown in Fig. 3.16. These 9 square-waves are distributed into three sets of square-waves, each set contains three square-waves with a relative phase-shift or $\pm\pi/3$, and the sets are phase shifted by $\pm\pi/5$. The suppression of the third- and fifth-order harmonic components in the spectrum of the output signal $y_2(t)$ is illustrated by the vector phase diagrams shown in Fig. 3.17. These polar diagrams show the phase and magnitude of the third- and fifth-order harmonic component vectors, plotted in blue and red respectively, of the original square-waves used to build the intermediate signals $y_1(t - \Delta t_2)$, $y_1(t)$ and $y_1(t + \Delta t_2)$, with the notation in Fig. 3.16. It is clearly observed that the combination of third-order harmonic vectors (in blue) in each set results in a null vector, while for the fifth-order harmonic the combination of the three sets also results in a null vector (for clarity, the resultant fifth-order harmonic vector is represented in green for each of the sets).

Figure 3.18 shows a block diagram of a sinusoidal signal generator based on this harmonic cancellation strategy for canceling the third- and fifth-order harmonic components. The required phase-shifts can be easily achieved using a shift-register with 30 flip-flops, initially loaded to 15 consecutive logic ones and 15 consecutive logic zeros to generate a 50% duty-cycle square-wave. In this case, scale factors ratios are integer –and powers of 2– which simplifies matching of the different signal branches in a practical implementation and relaxes its design effort.

The waveform of the step-level signal provided by combination of the delayed and scaled square-waves shown in Fig. 3.19.a is nearly close to a step-wise sine-wave and it will have the form of a typical sinusoidal signal after filtering as depicted in Fig. 3.19.b. The cancellation of the third- and fifth-harmonic components due to the harmonic cancellation is illustrated by the spectrum of the final signal in

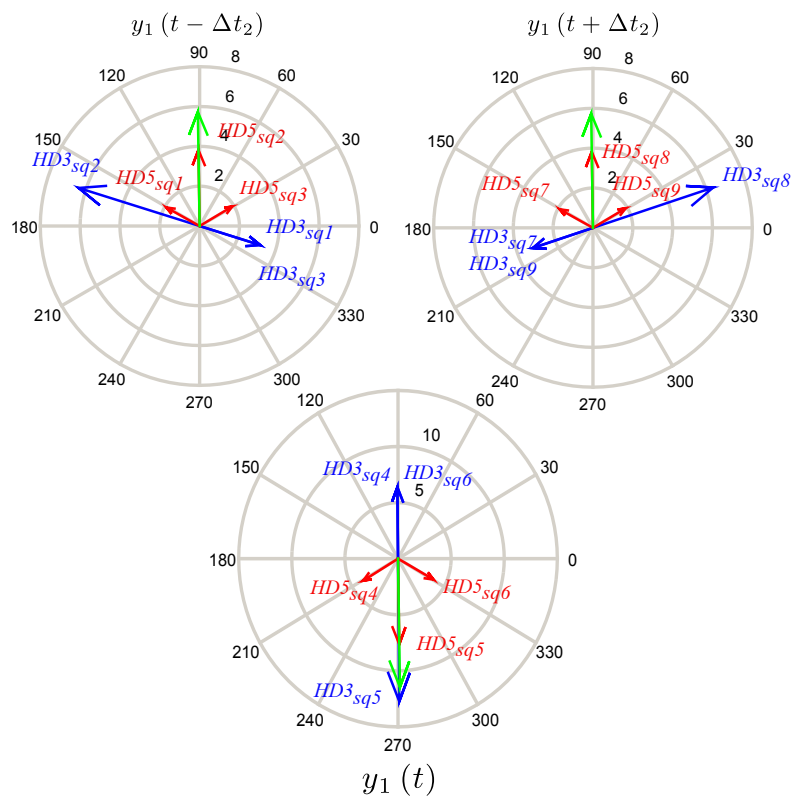


Figure 3.17: Phase vector diagram of the harmonic cancellation strategy using integer scale weight ratios to cancel the 3rd and 5th order harmonic components.

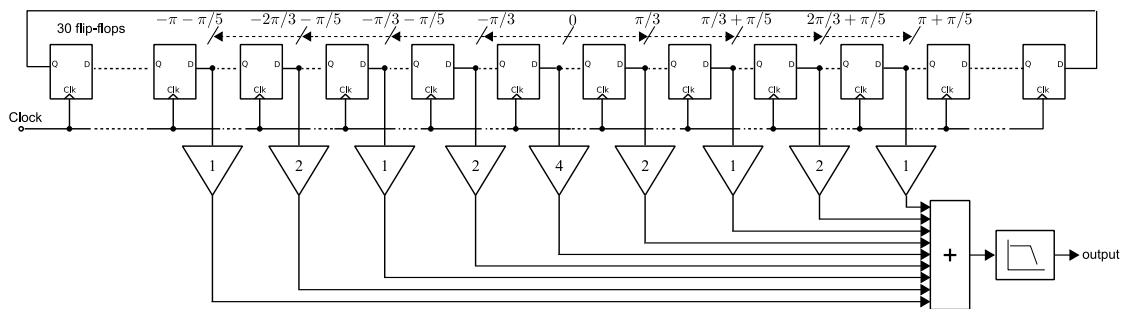


Figure 3.18: Block diagram of the proposed sinusoidal signal generator using nine signal phases and integer scale weights to cancel the third- and fifth-order harmonic components.

3.19.c.

This harmonic cancellation strategy can be easily generalized for canceling any number of harmonics. Thus, if we iterate the process p times, the resulting signal

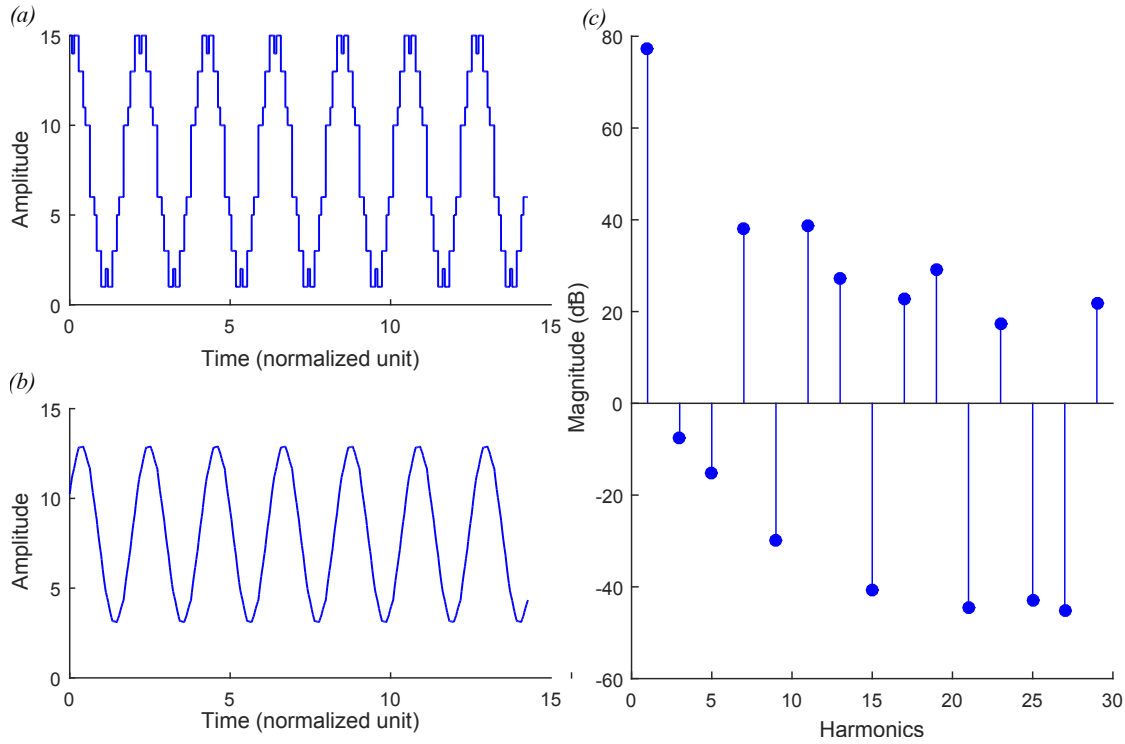


Figure 3.19: (a) Waveform of the step-level sinusoidal signal; (b) waveform of the generated sine-wave; (c) spectrum of the generated sine-wave.

$y_p(t)$ can be written as:

$$\begin{aligned}
 y_p(t) &= 2y_{p-1}(t) + y_{p-1}(t + \Delta t_p) + y_{p-1}(t - \Delta t_p) & (3.21) \\
 &= \sum_{k=1}^{\infty} 2^p A_k \prod_{i=1}^p [1 + \cos(k\phi_i)] \cos(k\omega_0 t + \varphi_k)
 \end{aligned}$$

And the resulting cancellation condition for a given harmonic k can be expressed as equation A.22 to cancel all odd harmonic components lower than $2p + 1$.

$$\prod_{i=1}^p [1 + \cos(k\phi_i)] = 0 \quad (3.22)$$

However, cancelling multiple harmonic components requires longer shift-registers to be able to generate the required signal phases and increases the number of required signal phases, hence increasing the complexity of the design.

3.7 Harmonic cancellation strategy with irrational scale weight ratios

A possible solution to solve the harmonic cancellation condition in A.4 is to set $\alpha_0 = 1$, and to compute the phase-shifts ϕ_i and the weights α_i as:

$$\begin{cases} \phi_i = i \frac{2\pi}{4(p+1)} & 1 \leq i \leq p \\ \alpha_i = \cos(i \frac{2\pi}{4(p+1)}) & 1 \leq i \leq p \end{cases} \quad (3.23)$$

These design equations allow canceling a given set of low-order odd harmonic components in the original square-wave signal $sq(t)$, lower than the $2(2p + 1)$ -th order, while a lenient low-pass filter can be used to attenuate high-frequency harmonic components.

This harmonic cancellation strategy has been thoroughly explored by a number of groups [50, 41, 46, 48] and it based on a direct application of the coefficient formula given in (A.23) to calculate the scale factors α_i and the phase-shifts ϕ_i . Table 3.1 summarizes the phase-shifts and the weight ratios required for a given number of signal pairs, p , and the number of harmonics to be suppressed.

Table 3.1: Coefficients of harmonic cancellation technique.

p	N	Phase-shifts (ϕ_i)				Scale weight (α_i)					$1^{st}nch^*$
		ϕ_1	ϕ_2	ϕ_3	ϕ_4	α_0	α_1	α_2	α_3	α_4	
1	3	$\frac{\pi}{4}$	-	-	-	1	$\frac{\sqrt{2}}{2}$ $\simeq 0.707$	-	-	-	7
2	5	$\frac{\pi}{6}$	$\frac{\pi}{3}$	-	-	1	$\frac{\sqrt{3}}{2}$ $\simeq 0.866$	$\frac{1}{2}$	-	-	11
3	7	$\frac{\pi}{8}$	$\frac{\pi}{4}$	$\frac{3\pi}{8}$	-	1	$\sqrt{\frac{2+\sqrt{2}}{4}}$ $\simeq 0.923$	$\frac{\sqrt{2}}{2}$ $\simeq 0.707$	$\sqrt{\frac{2-\sqrt{2}}{4}}$ $\simeq 0.382$	-	15
4	9	$\frac{\pi}{10}$	$\frac{\pi}{5}$	$\frac{3\pi}{10}$	$\frac{2\pi}{5}$	1	$\sqrt{\frac{5+\sqrt{5}}{8}}$ $\simeq 0.951$	$\frac{\sqrt{5}+1}{4}$ $\simeq 0.809$	$\sqrt{\frac{5-\sqrt{5}}{8}}$ $\simeq 0.587$	$\frac{\sqrt{5}-1}{4}$ $\simeq 0.309$	19

* nch = non – cancellable harmonic

In a practical implementation, there is a clear trade-off between the number of harmonics that can be canceled and the complexity of the generator, since the necessary number of delayed versions of the original square-wave increases if harmonic cancellation is extended to high-order harmonics. A good trade-off is explored in

previous works [50, 48, 46] using $p = 2$ pairs versions of the original square-wave, which cancels odd-order harmonics up to the ninth harmonic components. .

This solution employs a combination of 5 square-waves $sq_1(t)$ to $sq_5(t)$, as it is conceptually depicted in Fig. 3.20 with opposite phase-shifts $\phi_1 = \frac{\pi}{6}$, and $\phi_2 = \frac{\pi}{3}$ and scale weights $\alpha_0 = 1$, $\alpha_1 = \frac{\sqrt{3}}{2}$, and $\alpha_2 = \frac{1}{2}$, using the notation in (A.3). According to the analytical results in (A.23), this configuration cancels the third-, fifth-, seventh-, and ninth-order harmonic components in the original square-wave $x(t)$, while keeping a reduced design complexity.

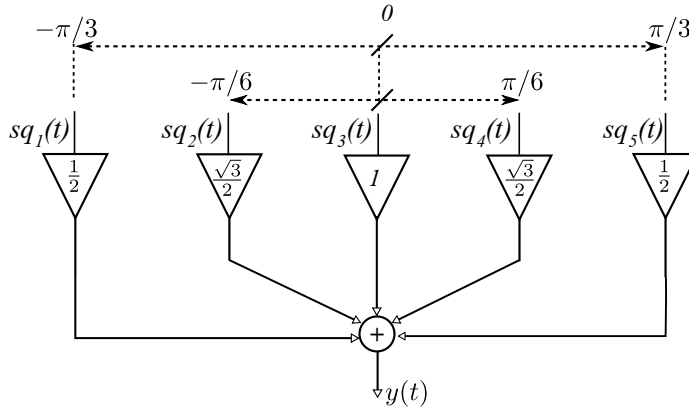


Figure 3.20: Conceptual block diagram of the harmonic cancellation strategy using irrational scale weight ratios to cancel the 3rd, 5th, 7th and 9th order harmonic components.

The suppression of the unwanted harmonic components in the spectrum of the output signal $y(t)$ is illustrated by the vector phase diagrams shown in Fig. 3.21. These polar diagrams show the phase and magnitude of the third-, fifth-, seventh-, and ninth-order harmonic component vectors of the original square-waves $sq_1(t)$ to $sq_5(t)$, with the notation in Fig. 3.20. It is clearly observed that the combination of harmonic vectors with the same order results in a null vector.

Figure 3.22 shows a block diagram of a sinusoidal signal generator based on this harmonic cancellation strategy for canceling the third-, fifth-, seventh- and ninth-order harmonic components. The required phase-shifts can be easily achieved using a shift-register with 12 flip-flops, initially loaded to 6 consecutive logic ones and 6 consecutive logic zeros to generate a 50% duty-cycle square-wave.

As an example, Fig. 3.23 shows the waveform of the step-level sine-wave provided by combination of the delayed and scaled square-waves, the final signal in the output of the first order filter and the spectrum of the final signal where the cancellation of the third-, fifth-, seventh- and ninth-harmonic components is clearly depicted. The spectrum in Fig. 3.23.c shows also a reproduction of the suppression of harmonics in higher-order and only the 1st, 11th, 13th, 23th, 25th... are retained.

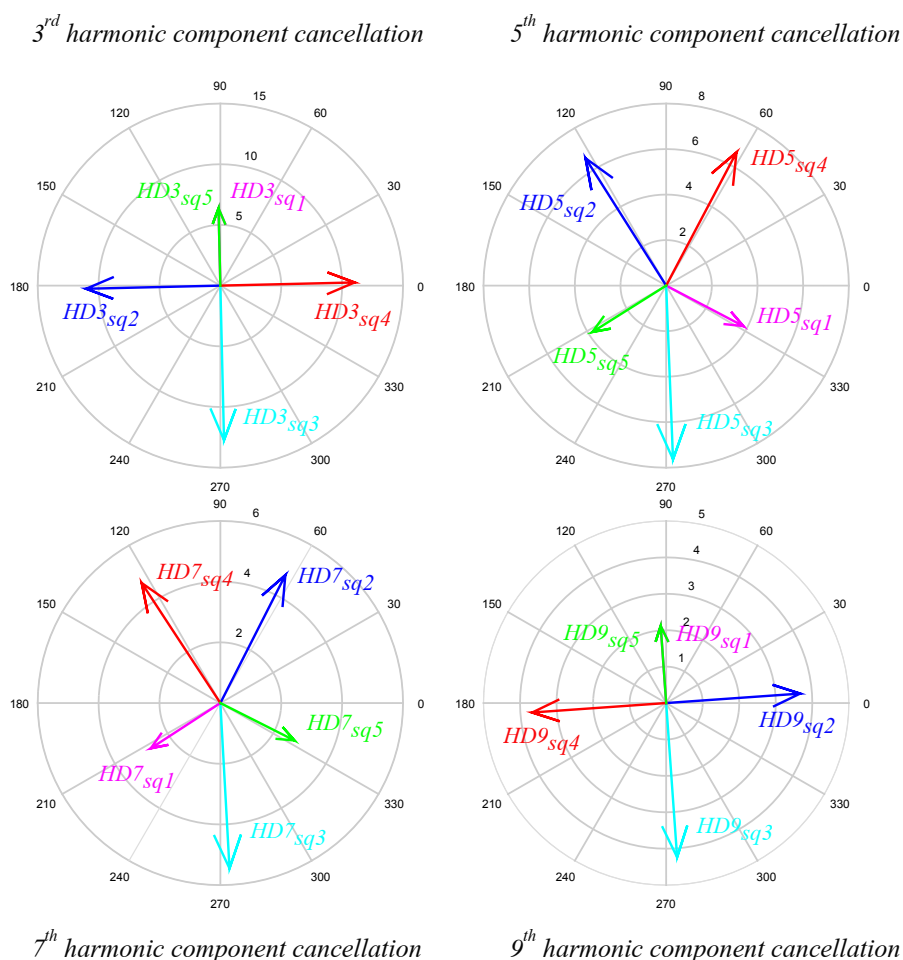


Figure 3.21: Phase vector diagram of the harmonic cancellation strategy using irrational scale weight ratios to cancel the 3^{rd} , 5^{th} , 7^{th} and 9^{th} order harmonic components.

Results were obtained by behavioral simulations in MATLAB of the generator in Fig. 3.22 under ideal conditions.

Multiple practical implementations of the irrational weights have been explored, for instance by using weight resistors [46, 47, 54] or weighted current sources [49, 51, 55]. The performances of the harmonic cancellation are very sensitive to mismatch which requires a careful layout of the elements and, usually, a dedicated calibration [46, 54] or mismatch compensation techniques like Dynamic Element Matching [50]. The calibration technique of the weighting ratios depends on the hardware implementation of the scaling stage. The generator in [54] is using a weighting resistor network in the scaling stage and the author introduces an efficient calibration technique based on implementing compensation resistors to

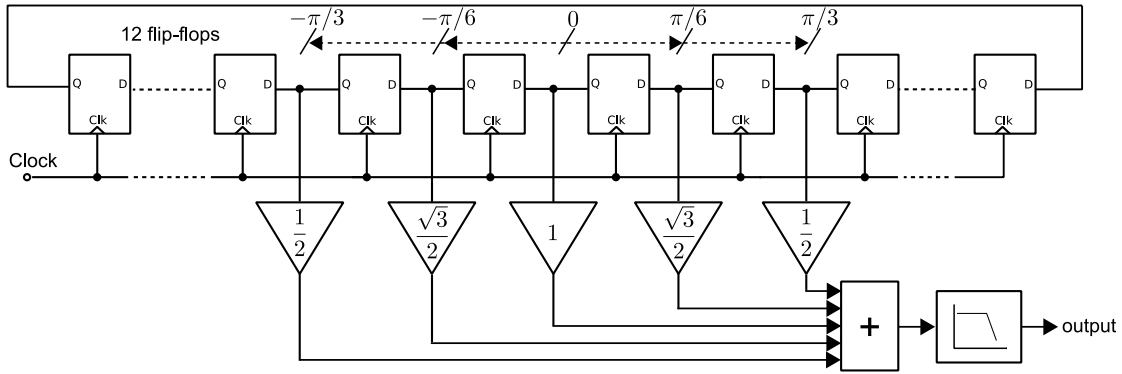


Figure 3.22: Block diagram of the proposed sinusoidal signal generator using five signal phases to cancel the third-, fifth-, seventh- and ninth-order harmonic components.

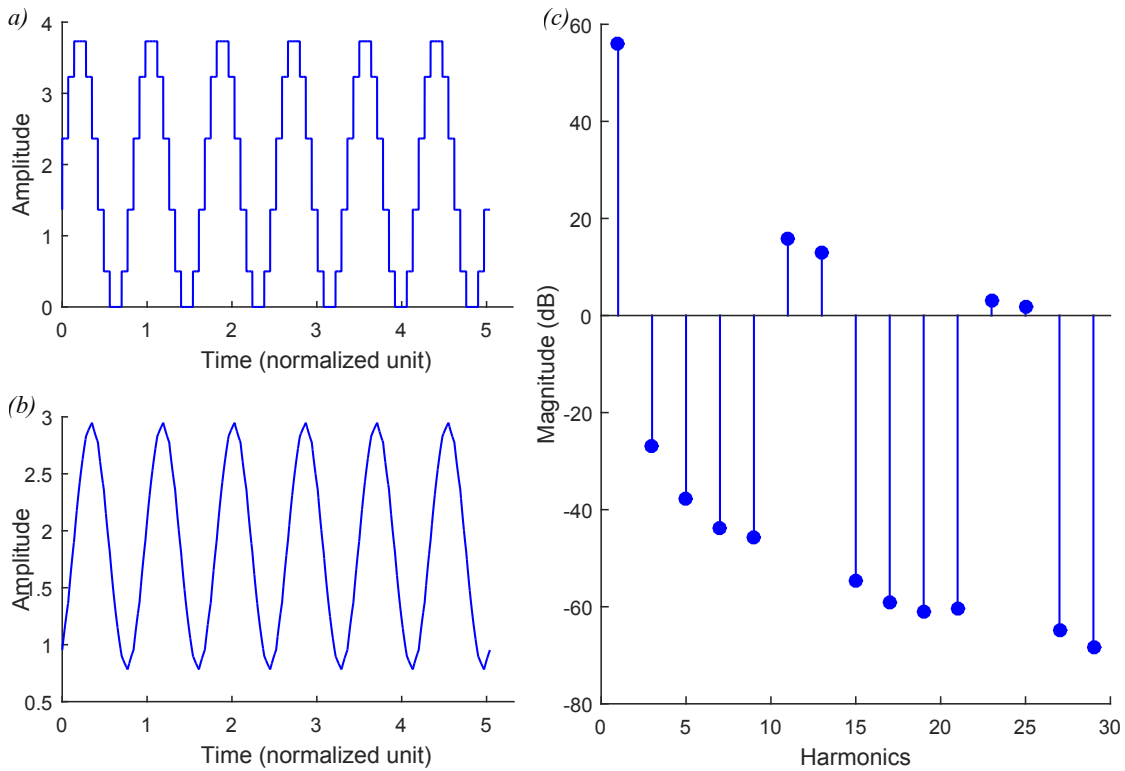


Figure 3.23: (a) Waveform of the step-level sinusoidal signal; (b) waveform of the generated sine-wave; (c) spectrum of the generated sine-wave.

correct the resistors values and compensate the weighting factor variation.

This harmonic cancellation strategy has also an interesting characteristic: there is a correlation between the cancellation of different harmonic components. That

is, ensuring the cancellation condition for some components, assures cancellation conditions for other components. This can be seen by observing the phase vector diagram in Fig. 3.21 where the distributions of the third- and ninth-order harmonic components are the same and the cancellation of the harmonics is done and similarly for the fifth- and seventh- harmonic components. To further explore this correlation, let us develop the harmonic cancellation conditions A.4 for the 3rd-, 5th-, 7th- and 9th-order harmonic components as

for $k = 3$

$$1 + \sqrt{3}\cos\left(3\frac{\pi}{6}\right) + \cos\left(3\frac{\pi}{3}\right) = 1 + \sqrt{3}\cos\left(\frac{\pi}{2}\right) + \cos(\pi) = 0 \quad (3.24)$$

for $k = 5$

$$1 + \sqrt{3}\cos\left(5\frac{\pi}{6}\right) + \cos\left(5\frac{\pi}{3}\right) = 1 + \sqrt{3}\cos\left(\frac{5\pi}{6}\right) + \cos\left(\frac{5\pi}{3}\right) = 0 \quad (3.25)$$

for $k = 7$

$$1 + \sqrt{3}\cos\left(7\frac{\pi}{6}\right) + \cos\left(7\frac{\pi}{3}\right) = 1 + \sqrt{3}\cos\left(\frac{7\pi}{6}\right) + \cos\left(\frac{7\pi}{3}\right) = 0 \quad (3.26)$$

for $k = 9$

$$1 + \sqrt{3}\cos\left(9\frac{\pi}{6}\right) + \cos\left(9\frac{\pi}{3}\right) = 1 + \sqrt{3}\cos\left(\frac{\pi}{2}\right) + \cos(\pi) = 0 \quad (3.27)$$

From eq. (3.24) and (3.27) it is clear that the harmonic cancellation condition third- and ninth-harmonic components have the same form and the cancellation of the components is done using the same cancellation coefficients. The same condition can be found for the fifth- and seventh-harmonic components when observing (3.25) and (3.26).

This correlation between the cancelled harmonics can be very useful when a calibration based on spectrum measurements is expected to compensate the effect of mismatch and process variations. Indeed, this type of calibration tends to compensate the timing or/and scaling error introduced in the circuit, by trimming techniques, and the correction is based on minimizing the magnitudes of the unwanted harmonics. Due to this correlation, each couple of harmonics will progress in the same way, in other words, the calibration can be simplified by focusing only on measuring the third- and fifth-order harmonics instead of measuring all unwanted harmonic components. Figure 3.24 presents the simulations results that confirm this correlation in two operation scenarios. 100 generator instances are simulated when medium imperfections of 0.1 ps and 1% are introduced on the flip-flop delays and the scale weight ratios, respectively, and when high imperfections are introduced such as 1 ps and 10% for the delay of the flip-flops and the scale

3.7 Harmonic cancellation strategy with irrational scale weight ratios

weight ratios, respectively. The results show a correlation of at least 98% between the considered couples of harmonics for both imperfections scenarios.

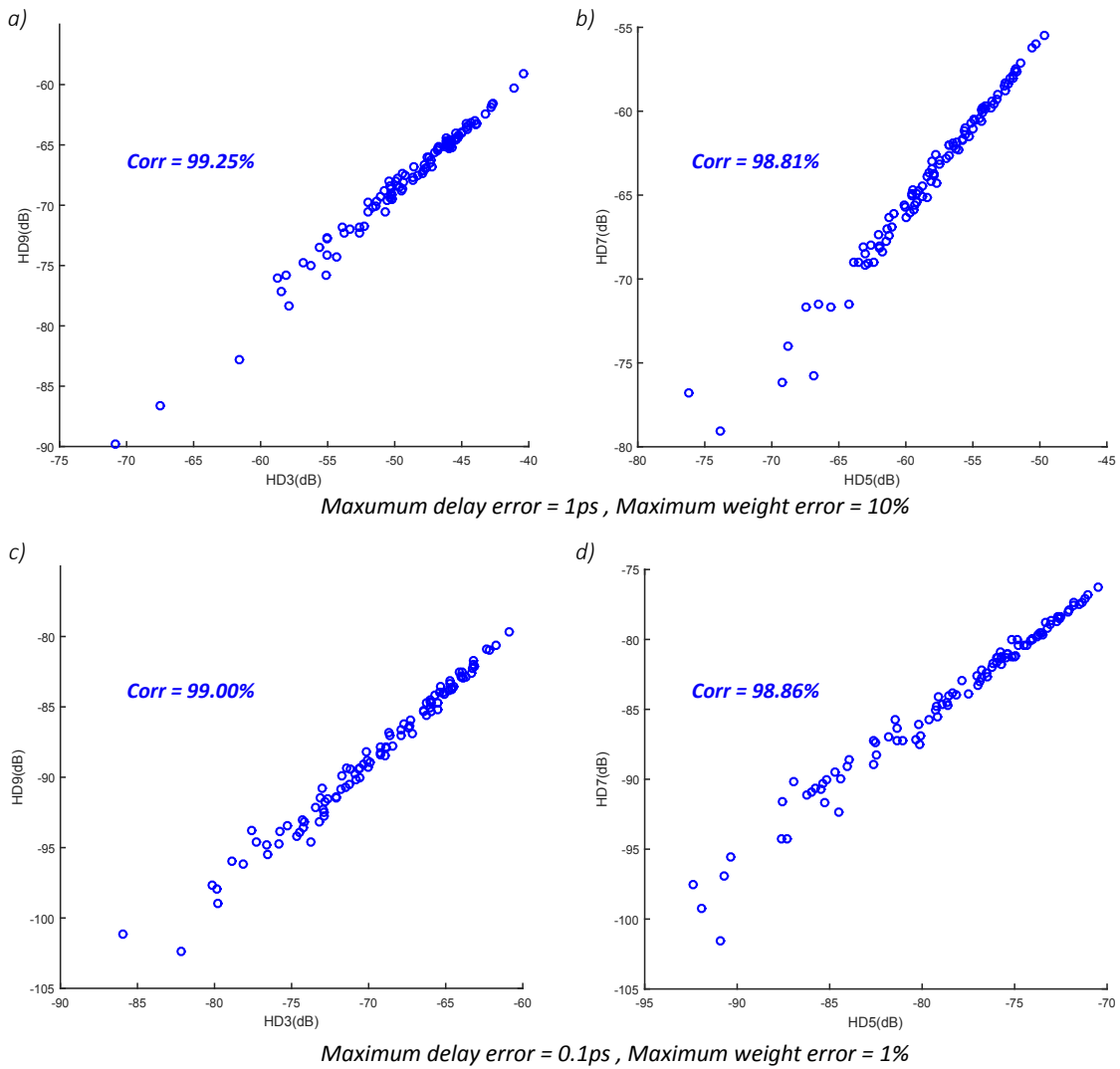


Figure 3.24: Correlation between third- and ninth-order harmonic component.

3.8 Comparison of different harmonic cancellation techniques

3.8.1 Limitations of harmonic cancellation implementation

The main limitations of the proposed on-chip implementation of the sine-wave generation strategies presented above are the random variations of the scale-weight ratios and the phase-shift of the combined square-waves. The deviation of the scale-weight coefficients are caused essentially by the mismatch between the weighting elements which may affect the step-levels of the step-wise sine-wave, as shown in Fig. 3.25.a. The variations of the fabrication process parameters may also affect the phase-shifted square-wave generator by introducing additional random delays to the flip-flops propagation delay, which will introduce a random additional phase-shift between the square-waves. In the frequency domain, the additional level errors ε_α and timing errors ε_t impact the phases and the amplitudes of the distortion harmonic vectors of the square-waves and it will be moved from their nominal positions shown in Fig. 3.9, 3.13, 3.17 and 3.21. In this case the combination of the distortion harmonics will not be a null vector, but distortion harmonic components may appear in the spectrum of the generated sinusoidal signal as shown in Fig. 3.25.b. which may limit strongly the performance of the harmonic cancellation technique.

3.8.2 Analysis of performances limitations

In order to demonstrate the feasibility of the proposed harmonic cancellation strategies, we have developed realistic behavioral models for the described generators in Fig. 3.10, 3.14, 3.18 and 3.22. The goal of these simulations is to analyze the effectiveness of the cancellation in the presence of fabrication imperfections that may introduce deviations in the phase-shifts and scale weight ratios required for the considered harmonic cancellation techniques. A set of statistical behavioral simulations were performed in MATLAB considering mismatch between the scale weights and between the propagation delays of the flip-flops. Scale weight mismatch was modeled as random variable with a Gaussian distribution. It has to be noted that this simple mismatch model is aimed at providing an upper performance bound, independently of the practical realization of the weights, with the goal of guiding the exploration of the design trade-offs for the proposed generator. Delay errors in the flip-flops include the contribution of propagation delay variation and clock jitters, modeled as independent random variables.

Two different operation scenarios were considered for all the proposed generators: a high-frequency scenario with clock frequencies $f_{clk} = 2$ GHz, and a moderate-

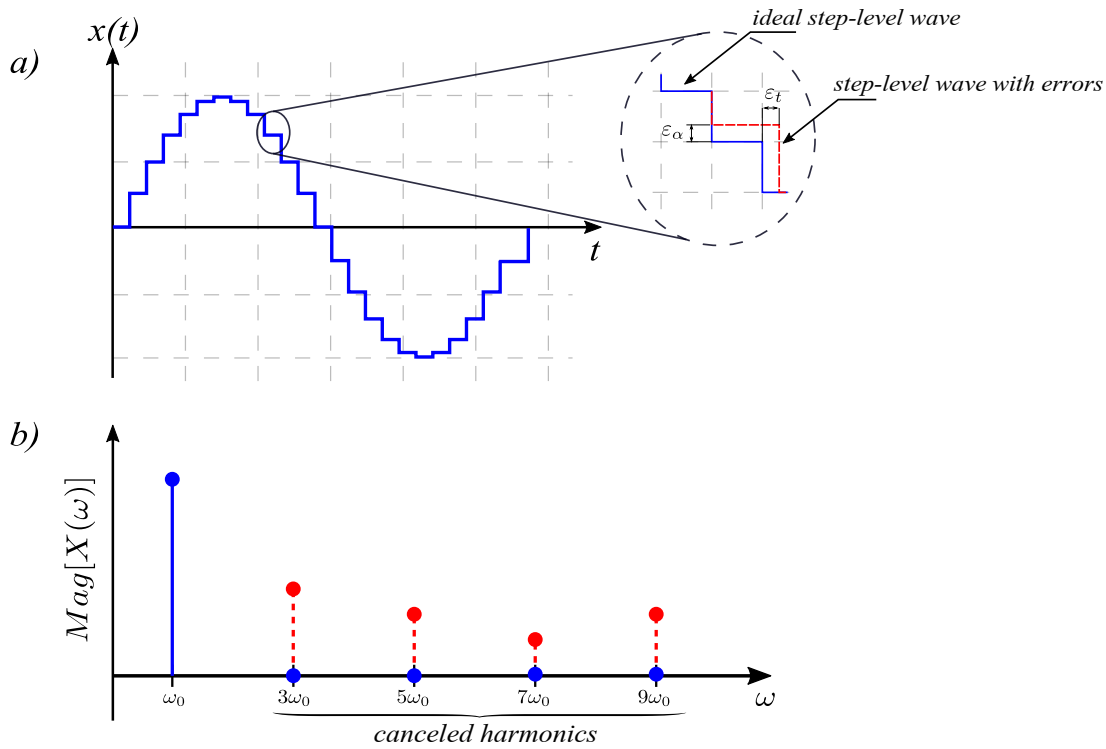


Figure 3.25: Generated step-level sine-wave with errors: (a) time domain; (b) frequency domain.

frequency scenario with $f_{clk} = 200$ MHz. Notice that the frequency of the output sinusoidal signal for each generator will be equal to the clock frequency divided by the number of flip-flops used in the digital shift-register, that is, $f_{wave} = \frac{f_{clk}}{N}$. Our analysis considers a system level perspective in which the master clock frequency is given by the system. Given that the generated output frequency is a fraction of the master clock frequency, the design trade-offs for the different generator architectures have to include the output frequency as a variable.

The performance of each generator in the two considered operation scenarios is evaluated in terms of the THD of the generated sinusoidal signal. It is important to remark that, in order to provide a fair comparison between the proposed harmonic cancellation strategies, the THD is evaluated until the highest-order non-cancellable harmonic component, i.e. the THD will be computed until the 10th harmonic component in the case of the generator with irrational scale weight ratios and until the 6th harmonic component for the other generators, since higher harmonic components are not affected by the cancellation strategy.

In order to assess the influence of timing errors in the proposed harmonic cancellation strategies, Fig. 3.26 shows boxplots of the THD obtained for the four

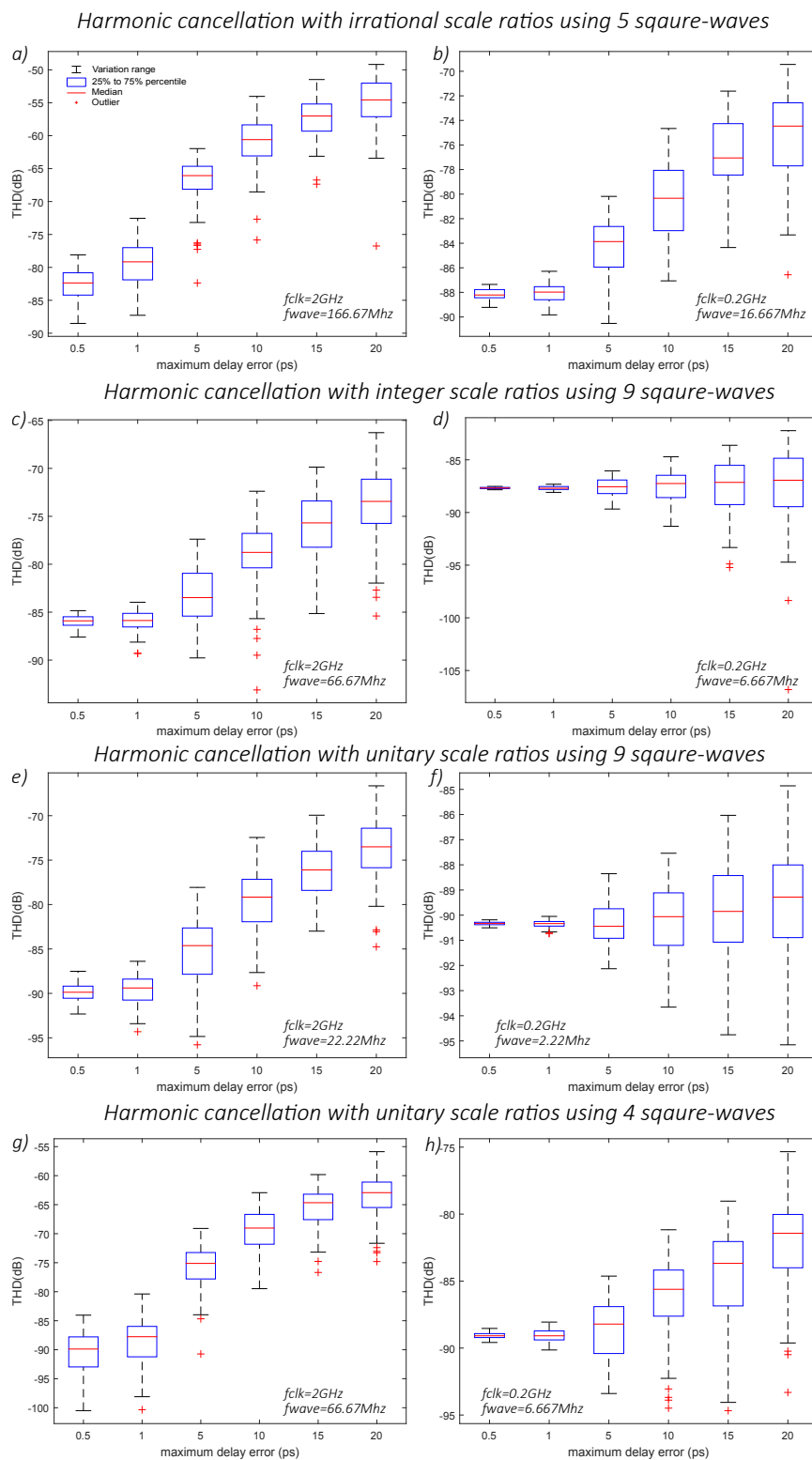


Figure 3.26: Generated output THD variation as function of the maximum delay error.

considered harmonic cancellation strategies, for the two different operation frequencies considered, as a function of the maximum delay error of the flip-flops in the shift-registers, obtained by behavioral level statistical simulations. A total of 100 generator instances were randomly generated for each combination of operation conditions. Scale-weight mismatch and delay errors were modeled as random variables. In this set of simulations, the scale-weight mismatch is set to a maximum of 0.1% for all simulations.

As it is clearly shown in Fig. 3.26, for all the considered sinusoidal signal generators and operation scenarios, the obtained THD is very low (around -90 dB) when the delay errors are negligible, which points to a good performance of the harmonic cancellation strategies close to the ideal conditions.

In the high-frequency scenario, i.e., $f_{clk} = 2$ GHz, it is clear that there is a degradation of the THD due to the delay mismatch between the flip-flops. However, it is interesting to notice that this degradation is less important for generators using 9 square-waves than for generators using fewer square-waves.

This observation is also confirmed in the low operation frequency scenario, i.e. $f_{clk} = 200$ MHz, where the linearity of generators using 9 square-waves have almost no variation as function of the delay errors, as shown in 3.26.d and Fig. 3.26.f. The reason for this different behavior comes for the different cancellation strategies: as it can be seen in the polar vector diagrams in Fig. 3.17, 3.9, and 3.13, for generators with 9 square-waves the cancellation of the undesired harmonic components is the result of combining three different vectors, while the cancellation for generation strategies using fewer square-waves comes from combining only two vectors. It can be easily proved that the resultant vector (and hence, the effectiveness of the cancellation strategy) is more sensitive to variations when it comes from the combination of two vectors than when it is the resultant of three vectors.

In order to evaluate the impact of scale-weight mismatch in the proposed harmonic cancellation strategies, Fig. 3.27 shows boxplots of the THD obtained for the four considered harmonic cancellation strategies, for the two different operation frequencies considered, as a function of the maximum scale-weight mismatch in the summing network, obtained by behavioral level statistical simulations. A total of 100 generator instances were randomly generated for each combination of operation conditions. Scale-weight mismatch and delay errors were modeled as random variables. In this set of simulations, the time delay mismatch is set to a maximum of 0.1ps for all simulations.

As it can be observed, the impact of scale weight mismatch is practically identical for the four considered harmonic cancellation strategies. However, it is clear that the degradation of the signal linearity due to scale weight mismatch is more significant than the degradation due to the time delay errors. The linearity of the generated signal for the considered generation strategies depends strongly on the

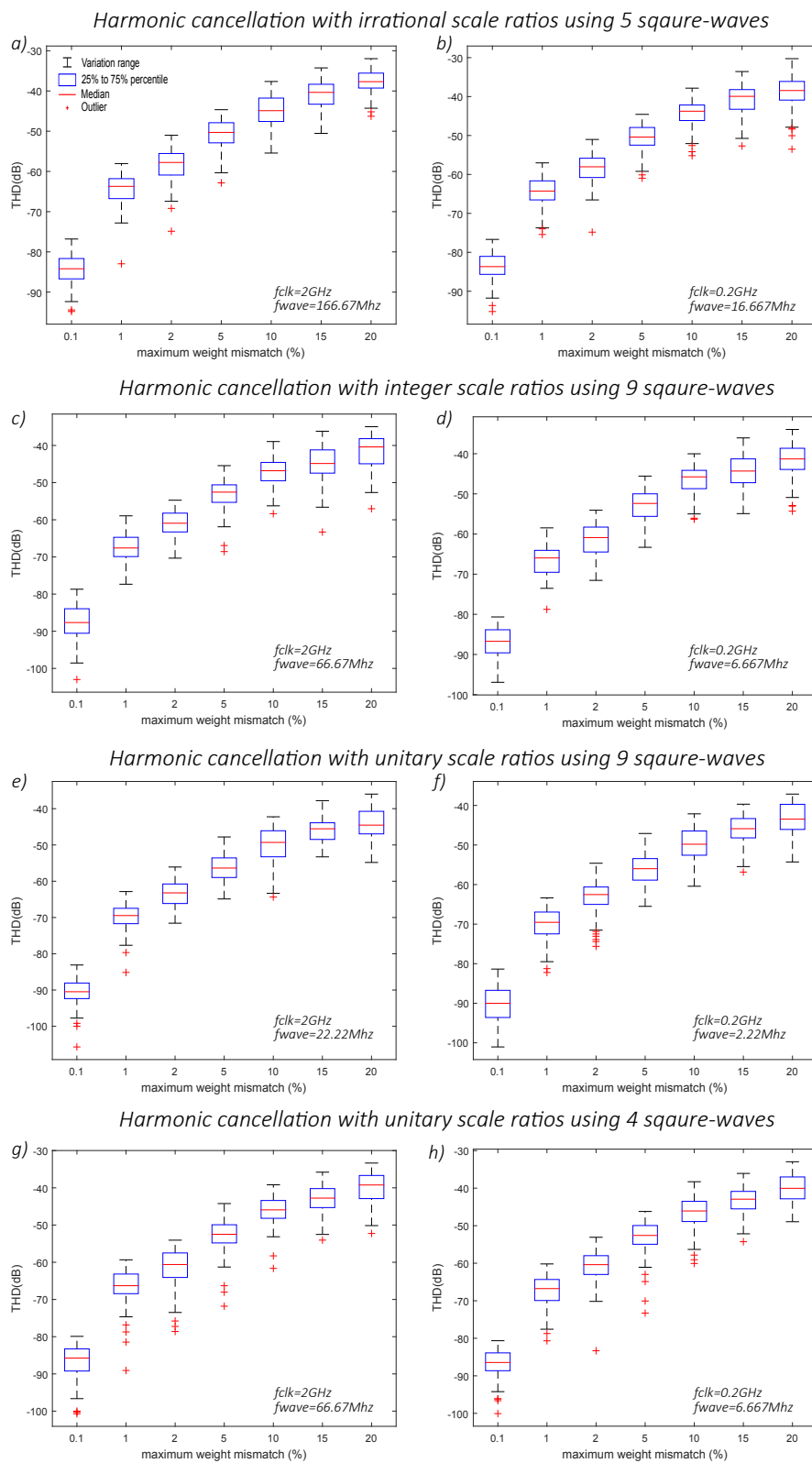


Figure 3.27: Generated output THD variation as function of the maximum weight mismatch.

precision of the scale weighting stage, while the linearity degradation due to time delay mismatch is only dominant for high-frequency operation.

Based on the THD variation results presented above, a scale weight calibration technique can be an efficient solution to compensate the linearity degradation of the proposed harmonic cancellation strategies. Two practical calibration techniques were discussed in [54] and [55]. The work in [54] proposes a one-shot calibration technique for a summing resistor network, while the work in [55] proposes simple calibrated current sources for implementing the scale weights in the summing network.

Statistical simulations were performed with the goal of evaluating the gain of a scale weight calibration for the four considered harmonic cancellation strategies. Figure 3.28 shows histograms of the obtained linearity in terms of THD for sinusoidal signal generators based on the four considered harmonic cancellation techniques before and after scale-weight calibration. A total of 100 instances of each generator were generated considering random time delay errors in the flip-flops and random scale weight mismatch, set to maximum deviations of 10 ps and 10%, respectively. In addition, the analysis was performed in both the high-frequency and the moderate-frequency scenarios.

As it can be seen in Fig. 3.28, scale-weight calibration offers a significant improvement in the THD of the generated signal for both considered operation frequency scenarios. This THD improvement is more noticeable in the moderate-frequency scenario, even though the impact of the time delay error is not corrected. For the high-frequency scenario, the effect of scale weight calibration is still significant, but uncorrected delay errors limit the linearity of the generated signal.

In the view of the obtained analytical and simulation results, it can be stated that there is a trade-off between the complexity of the scaling and summing network, the number of distortion harmonic components that can be canceled, the number of necessary phase-shifted square-waves, and the frequency of the generated sinusoidal signal. Table 3.2 summarizes the main characteristics of the four considered cancellation techniques in this line. Thus, harmonic cancellation using irrational scale weight ratios in Fig. 3.22 is interesting in terms of the frequency of the generated signal, the reduced number of square-waves and the number of harmonic components that can be canceled. However the implementation of this strategy may be complex and prone to scale weight mismatch because of the irrational scale weight ratios. The harmonic cancellation technique with unitary scale ratios and four signal paths in Fig. 3.14 reduces the necessary hardware resources, but the frequency of the provided signal is decreased with respect to the previous technique. In addition, the sensitivity of the implementation to delay errors is significant even in moderate-frequency operation. The unitary harmonic cancellation with 9 signal paths in Fig. 3.10 reduces the sensitivity to delay errors, but it re-

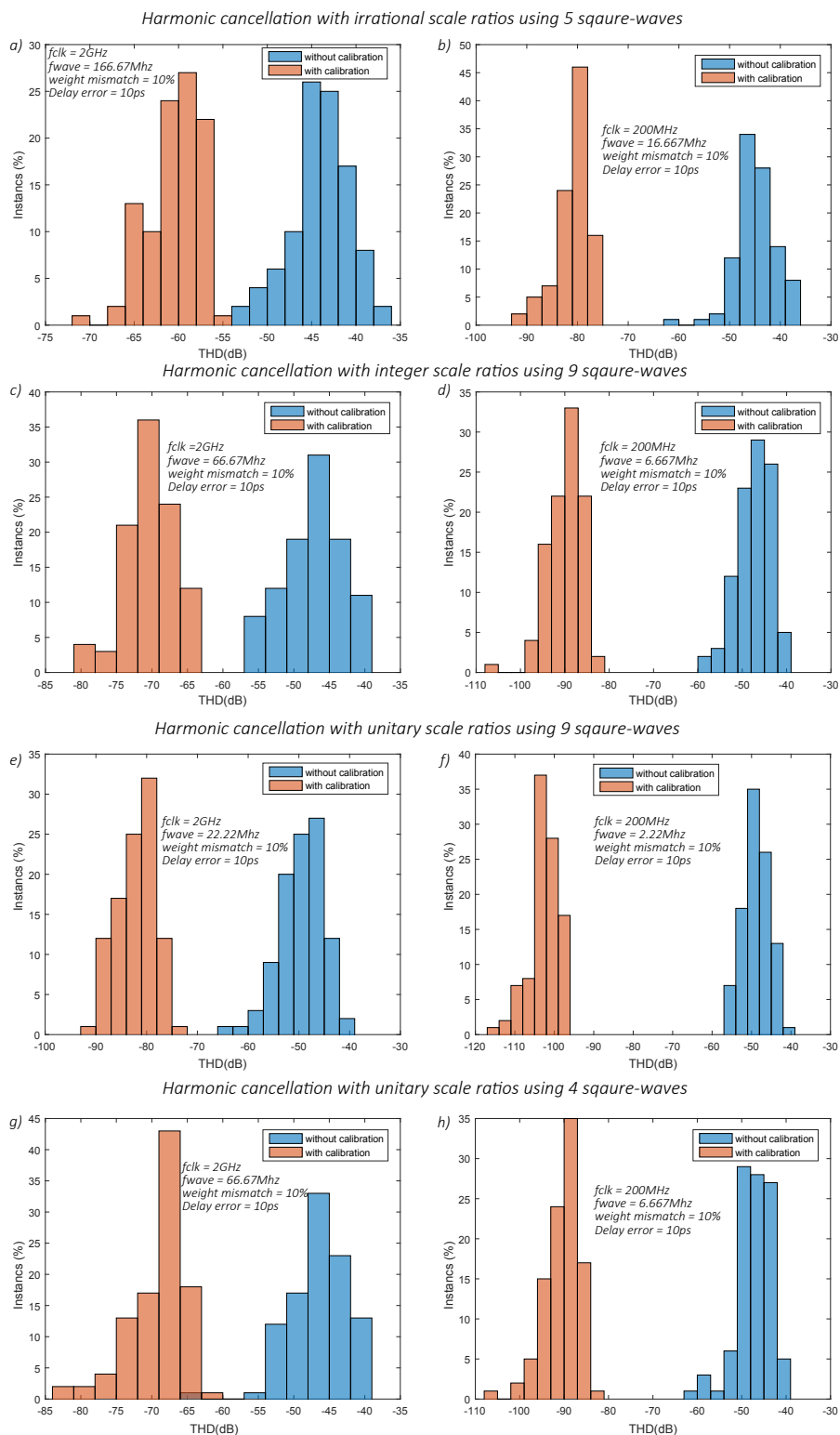


Figure 3.28: Generated output THD histograms before and after calibration.

quires a longer shift-register which decreases the frequency of the generated signal. On the other hand, the harmonic cancellation technique using integer scale ratios with 9 square waves in Fig. 3.18 uses the same number of square-wave signals with a shorter shift-register, which increase the frequency of the final output, but it requires different scale ratios between each signal path.

Table 3.2: Comparison of harmonic cancellation strategies.

Type of Scale ratios	Irrational	Integer	Unitary	
Number of square-waves	5	9	9	4
Length of shift-register	12	30	90	30
Frequency of the generated sine-wave	$f_{clk}/12$	$f_{clk}/30$	$f_{clk}/90$	$f_{clk}/30$
Relative phase-shift	$\pi/6$	$\pi/15$	$\pi/45$	$\pi/15$
Harmonic components to be canceled	$3^{rd}, 5^{th}, 7^{th}, 9^{th}$	$3^{rd}, 5^{th}$	$3^{rd}, 5^{th}$	$3^{rd}, 5^{th}$
Design complexity of the weighting stage	High	Low	Low	Low

Figure 17 further clarifies this trade-off. This figure represents the order of the first non-canceled harmonic as a function of the number of necessary phase-shifted square-waves for each of the presented sinusoidal signal generation techniques. Additionally, we indicate, for each data point, the set of different weights required for implementing each generator (for the generators with non-unitary weights).

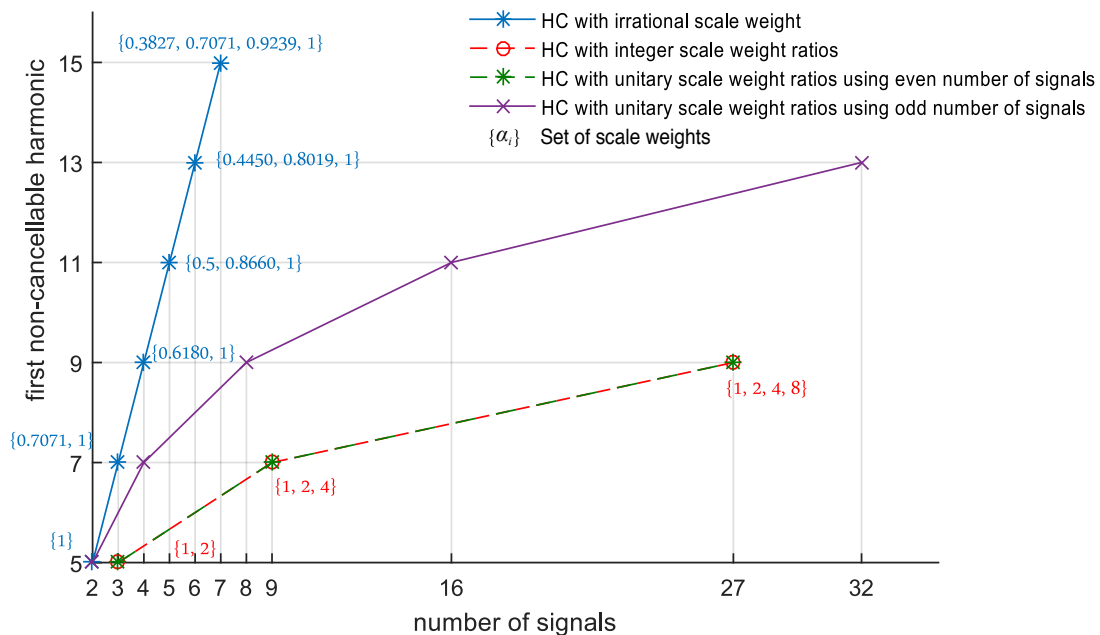


Figure 3.29: Comparison of the proposed harmonic cancellation strategies.

Chapter 4

Circuit design and simulations

4.1 Introduction

In view of the analytical results presented in the previous chapter, it is clear that the proposed harmonic cancellation technique using irrational weight ratios leads to more efficient implementations than the other proposed techniques, when we consider the trade-off between the number of harmonic components that may be cancelled and the necessary number of phase-shifted square-waves.

In this chapter, as a methodological design example, we present the complete design flow for such a sinusoidal signal generator, together with simulation results to validate the feasibility and performances of the proposed circuitry. The generator has been designed using STMicroelectronics 28 nm FDSOI technology, and our design goals are set to generate a sinusoidal signal with a THD better than -70 dB at a frequency above 100 MHz, which are design targets in the state of the art.

4.2 Hardware architecture of the sinusoidal signal generator

If we consider the proposed harmonic cancellation technique with irrational scale weight presented in section 3.7, it is clear that there is a trade-off between the number of harmonics that can be canceled and the complexity of the generator, since the necessary number of delayed versions of the original square-wave increases if harmonic cancellation is extended to high-order harmonics. Similarly, a trade-off exists between the number of canceled harmonics, the complexity of implementing irrational scale weights and the selectivity of the output filter. Taking these trade-offs into account, we propose to consider five time-delayed square-waves with

opposite phase-shifts $\Phi_1 = \frac{\pi}{6}$ and $\Phi_2 = \frac{\pi}{3}$ and scale weights $\alpha_0 = 1$, $\alpha_1 = \frac{\sqrt{3}}{2}$ and $\alpha_2 = \frac{1}{2}$, as shown in Fig. 3.20, using the notation in (3.2). According to the analytical results in previous chapter, this configuration cancels the third-, fifth-, seventh-, and ninth-order harmonic components in the original square-wave.

The proposed hardware architecture for our sinusoidal signal generator is derived from the block diagram depicted in Fig. 3.22. We choose to implement the weighting stage with the current steering technique, widely used in high frequency designs, and a simple passive RC filter in the output to filter higher-order non-cancellable harmonic components. A calibration circuitry is introduced in the design to compensate the weighting stage errors based on the analytical results shown in section 3.8. The target circuit should be ideally differential to avoid the apparition of even harmonic components. For this reason, digital blocks are designed to convert the single-ended signals provided by the square-wave generator to low-skew complementary square-waves while keeping a duty-cycle close to 50%.

The architecture of the circuit is shown in Fig.4.1 where the generator design features a circular shift-register that provides a set of five time-delayed digital square-waves. The generated signals are fed to double-ended buffers that output two complementary square-waves without modifying the relative phase-shift and duty cycles. These complementary digital square-waves are aimed to drive five fully-differential current-steering branches, whose reference currents have been properly weighted to the ratios $\frac{I_1}{I_0} = \alpha_1 = \frac{\sqrt{3}}{2}$ and $\frac{I_2}{I_0} = \alpha_2 = \frac{1}{2}$, to ensure harmonic cancellation as it was discussed above. However, to ensure a good switching of current-sources, it is very important to avoid opening the differential current switches at the same time, for this reason a non-overlapping buffer was introduced in the input of the current switches. The differential output currents of the five branches are summed using an on-chip passive network that provides additional filtering and translates the generated signal to an output voltage signal. The use of current-steering sources is more convenient than using the resistors network for scaling the square-waves, as it was proposed in [46], [47] and [54], because it simplifies the implementation of the irrational scale factor $\frac{\sqrt{3}}{2}$. Also, current sources are easier to calibrate for process and mismatch variations. The calibration of the current branches will be done with the help of the bias capacitors block and the calibration strategy will be shown in the following sections.

In order to satisfy the design goals of the desired generator -provide a sinusoidal signal with a THD better than -70 dB at a frequency above 100 MHz- both digital and mixed-signal parts of the circuit should respect a set of timing and weighting constraints obtained by behavioral simulations and presented in section 3.8 in the previous chapter. That means that digital signals controlling the current branches should have a timing accuracy, including duty-cycle and signal delays, lower than 5 ps and the current steering DAC should have a weight accuracy better than 1%,

according to Fig. 3.26 and Fig. 3.27.

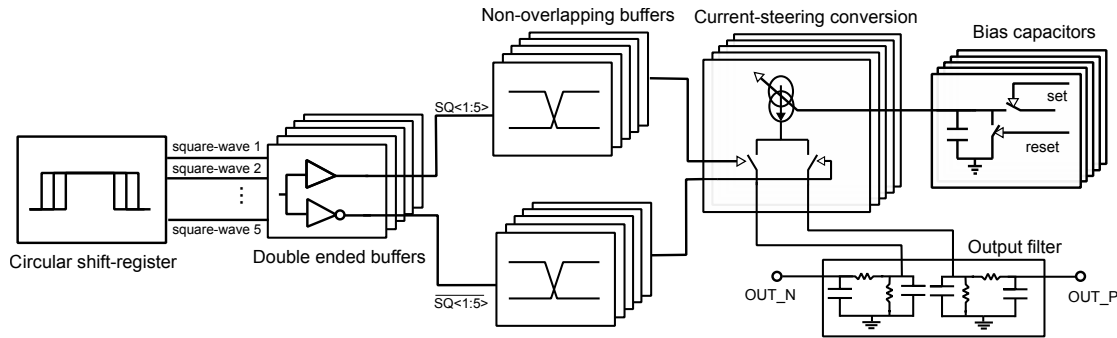


Figure 4.1: Block diagram of a practical implementation of the proposed sinusoidal signal generator.

4.2.1 Circular shift-register

A circular shift-register of twelve flip-flops provides the five square-waves with a 50% duty-cycle and phase-shifts $\Phi_1 = \frac{\pi}{6}$ and $\Phi_2 = \frac{\pi}{3}$ that are used for harmonic cancellation. The square-wave generator is driven by a master clock $f_{clk} = 2$ GHz in such a way that the frequency of the provided square-wave will be $f_{sq} = \frac{f_{clk}}{12} = 166.67$ MHz.

In order to reduce the design effort, the employed flip-flops are standard scan D-flip-flops, as shown in Fig.4.2, provided by the standard-cell library of the 28 nm FDSOI technology, with a two-input multiplexer (test enable, T_e , and test input, T_i) on the D input. The scan flip-flop behaves as a normal D-flip-flop when T_e is at a logic '0', i.e., the output Q follows the input D at the clock rising edge. On the other hand when T_e is set to a logic '1', the output Q is set to T_i , independent of D , as depicted in the truth table.4.1.

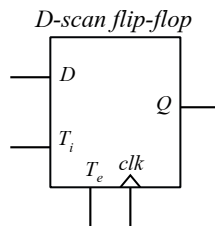


Figure 4.2: D-scan flip-flop.

The scan inputs, T_i and T_e , are used for loading in parallel the initial digital square-wave into the circular register, which correspond to six consecutive logic '1'

followed by six consecutive logic '0'. The initial six logic '1' sequence is reconfigured internally in the circular shift-register by connecting the T_i inputs of six consecutive flip-flops to vdd, as schematically shown in Fig.4.3. To load the six consecutive logic '0' sequence, the remained six flip-flop must be configured by setting their T_i to gnd. However, in our design, the flip-flops whose outputs are in the sine-wave generation path, have their T_i inputs controlled externally by signals T_{i0} to T_{i4} . These signals will be used for calibration purposes, as it will be described later in this chapter.

Table 4.1: Truth table of D-scan flip-flop.

D	clk	T_i	T_e	Q	\bar{Q}
D	\uparrow	-	0	-	D
-	\uparrow	T_i	1	-	T_i
-	-	-	0	Q	\bar{Q}

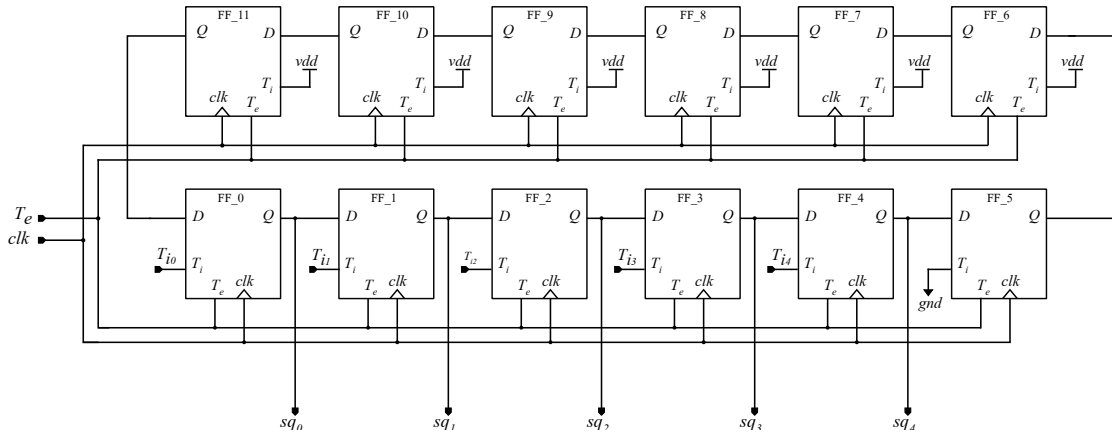


Figure 4.3: Circular shift-register architecture.

Figure 4.4 shows the chronogram of signals controlling the circular-shift register and its outputs. The initial sequence is loaded within a pulse of the T_e signal, which is common for all flip-flops. During this pulse-width, T_{i0} to T_{i4} are set to logic '0'. After the loading step, the circular shift-register enters in the generation mode of the configured square-wave by setting T_e to logic '0'. The generated square-waves sq_0 to sq_4 are time-delayed by a clock cycle which corresponds to a relative phase-shift of $\frac{\pi}{6}$.

Two key points for the functionality of the proposed system are the duty-cycle of the five square-wave outputs of the circular shift-register, that has to be kept at 50% (otherwise even harmonics will appear at the output), and the relative phase-shifts between the outputs that have to comply to the design values $\Phi_1 = \frac{\pi}{6}$ and

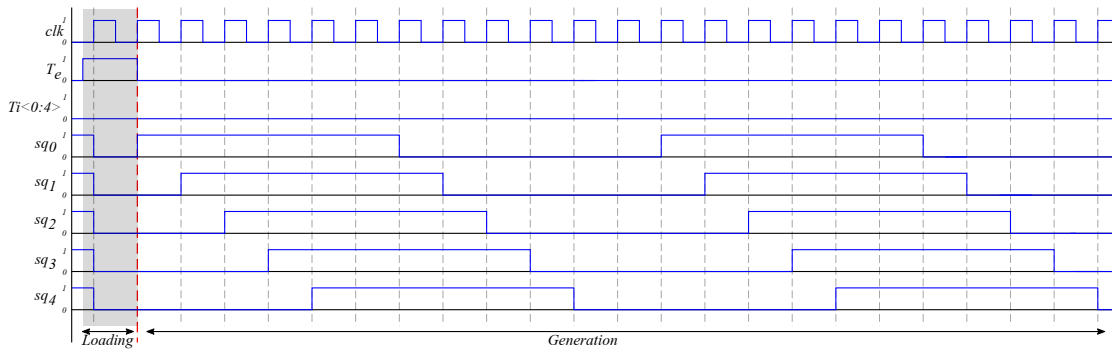


Figure 4.4: Chronogram circular shift-register.

$\Phi_2 = \frac{\pi}{3}$ (otherwise the effectiveness of the harmonic cancellation is compromised). Ideally, the synchronous operation of the circular shift-register guarantees these two conditions. However, non-idealities such as mismatch between the delays of the individual flip-flops or clock skew in the distribution of the clock signal to the flip-flops could jeopardize these conditions, specially for high clock frequencies. Moreover, clock jitter has to be minimized as it would increase the noise floor of the generated signal.

In order to evaluate the timing performances of the circular shift-register, we analyzed the statistical variation of the phase-shifts and the duty-cycles of the five outputs delivered by this block, when it is driven by a 2 GHz clock signal, against mismatch and fabrication process variations. Figures 4.5 and 4.6 show the distributions of the relative phase-shifts and the duty-cycles, respectively, of the different outputs provided by 100 iterations of Monte Carlo simulation. Histograms in Fig. 4.5 show that the different phase-shifts are centered around 30° and 60° , equivalent to $\frac{\pi}{6}$ and $\frac{\pi}{3}$, respectively, as required for the harmonic cancellation condition. The maximum $\pm 1\sigma$ variation range of the different phase-shifts is around $\pm 0.094^\circ$, equivalent to a $\pm 1\sigma$ delay error variation of ± 1.5 ps at 166.667 MHz, which complies with the requirements set by the behavioral simulation presented in Fig. 3.26.a to generate a sinusoidal signal with a THD below than -70 dB.

However, when examining the distribution of the duty-cycles of the square-waves generated by the digital shift register, depicted in histograms in Fig. 4.6, it is clear that the different duty-cycles are centered around 49.9%. These small deviations from the nominal duty-cycle of 50% will be corrected in the following blocks.

4.2.2 Double-ended buffer

In order to provide differential control signals for the current steering DAC, we propose a double ended buffer design that provides a single-to-differential con-

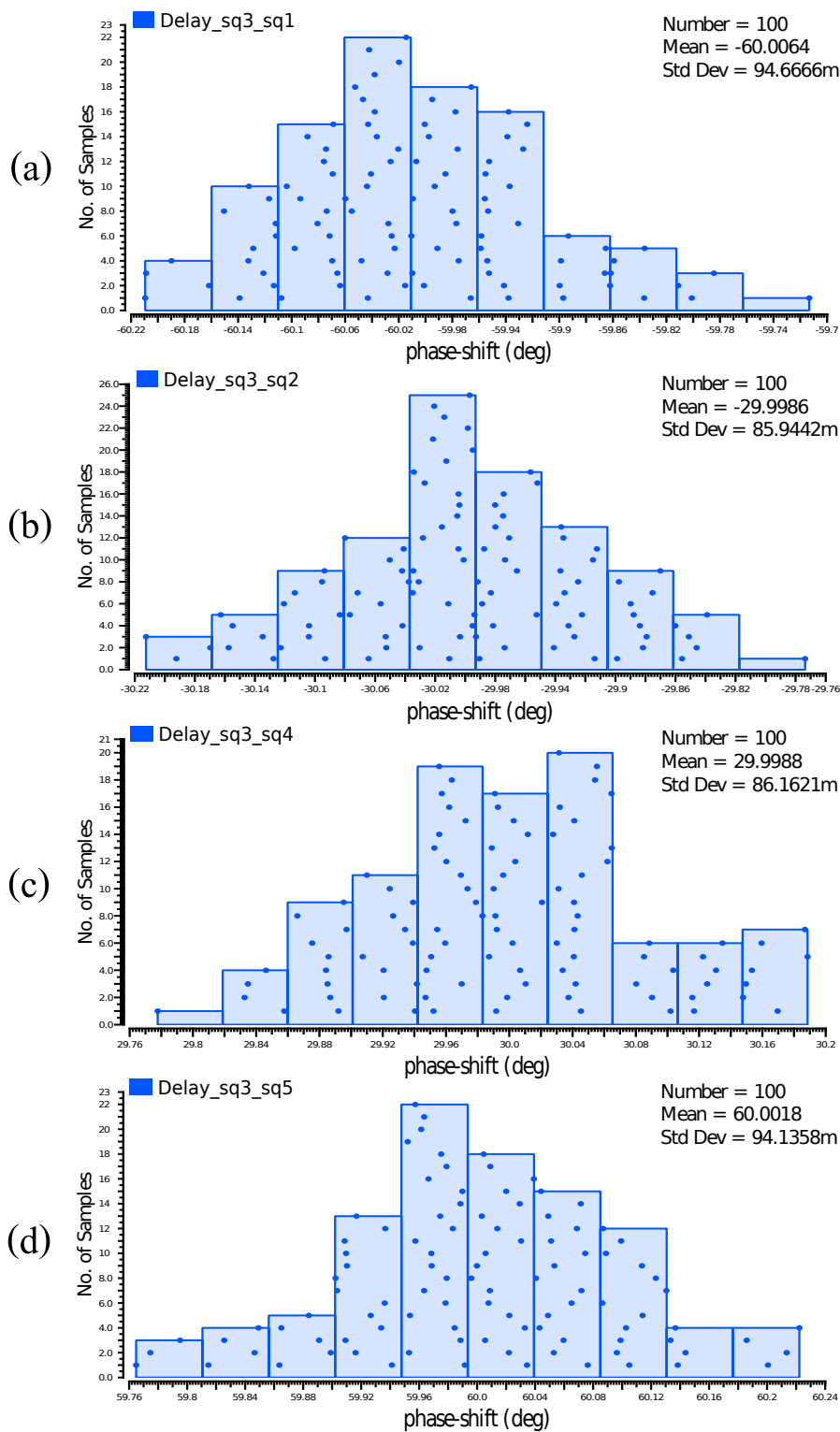


Figure 4.5: Histograms of phase-shifts of five shift-register outputs, across 100 Monte Carlo iterations.

4.2 Hardware architecture of the sinusoidal signal generator

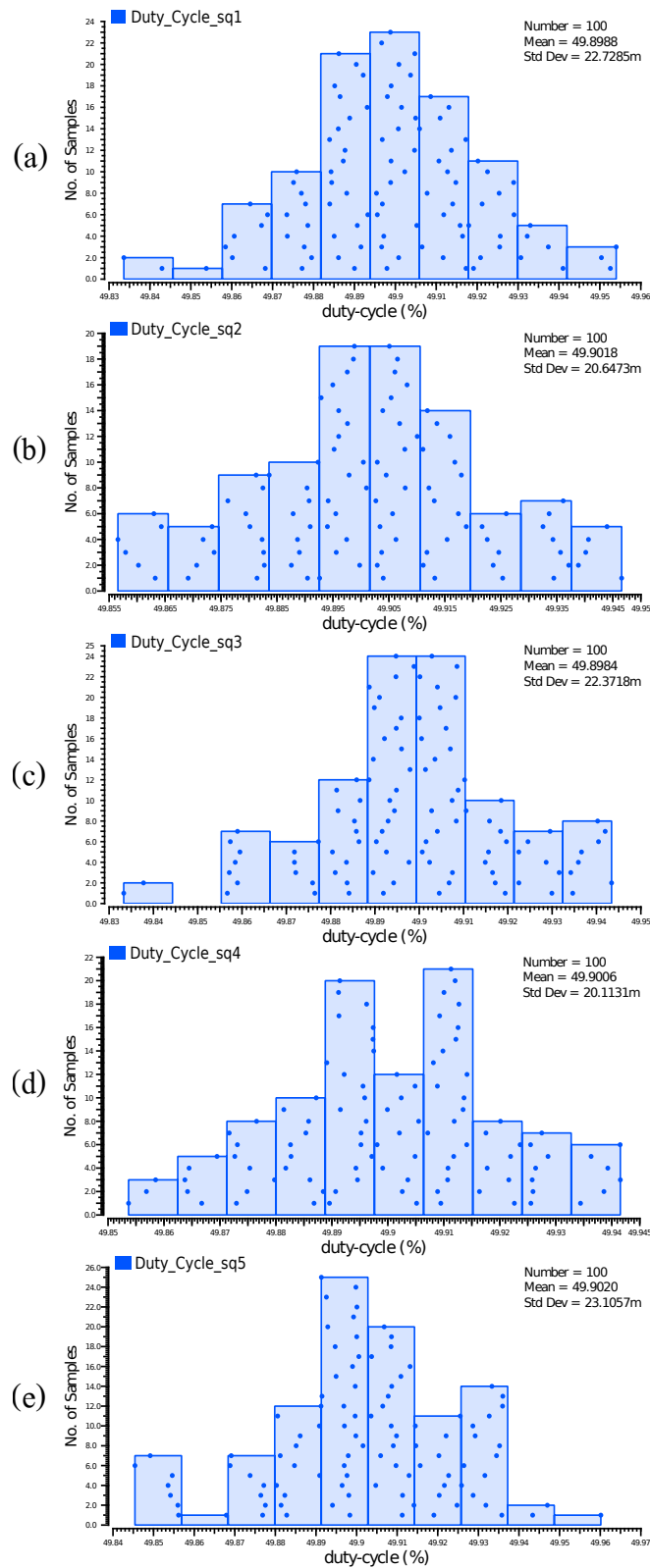


Figure 4.6: Histograms of duty-cycles of five shift-register outputs, across 100 Monte Carlo iterations.

version of the square-wave signals generated by the circular shift register. This double-ended buffer is designed in order to ensure a low skew between the complementary outputs. As illustrated in Fig. 4.7, the input stage of the buffer has two branches, the input of the positive branch includes a transmission gate followed by two inverters (*INV2* and *INV4*) to generate a buffered version of the input, while the input of the negative branch has a chain of three inverters (*INV1*, *INV2* and *INV3*) to generate the complement of the input signal. The transmission gate in the positive branch is used to compensate the propagation delay of *INV1* in the negative branch, and it is designed to be continuously enabled. A cross-coupled latch (*INV6* and *INV7*) is used to reduce the rise and fall times of the buffer and to reduce the skew between the differential signals. A buffering output stage (*INV8* to *INV11*) is used to provide appropriate fan-out to drive the following stage.

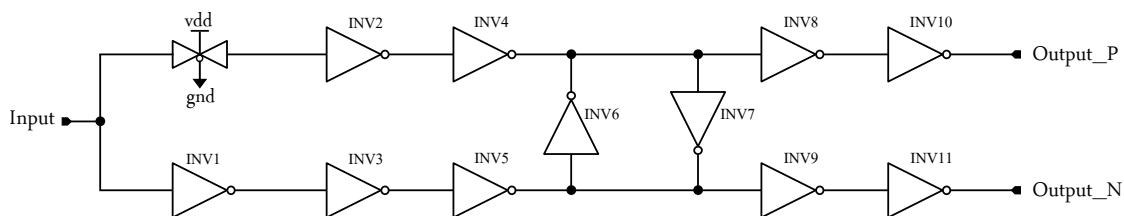


Figure 4.7: Double-ended buffer.

Figure 4.8 shows an electrical simulation of the designed double-ended buffer to show the functionality of the circuitry under nominal conditions.

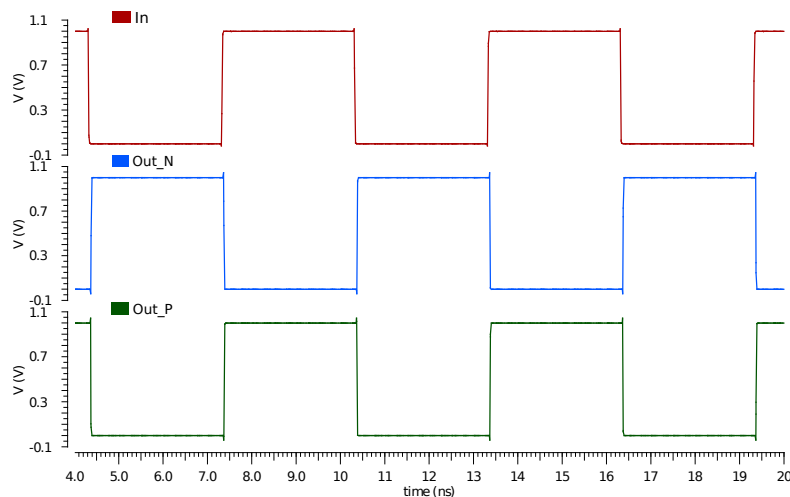


Figure 4.8: Double-ended buffer input/output wave-forms.

4.2.3 Non-overlapping buffer

Ideally, the outputs of the double-ended buffer may drive the *PMOS* current switches in the differential current-steering branches, as shown in the conceptual block diagram in Fig. 4.1. However, to ensure a good switching of current-sources, it is very important to avoid opening the differential switches at the same time. For this reason, we designed a non-overlapping buffer as shown schematically in Fig. 4.9, similar to the classical non-overlapping phase generators for switched-capacitor circuits [56, 57, 58]. The non-overlapping buffer is designed to provide complementary signals which intersect close to the low state, to avoid opening the differential switches simultaneously, while keeping the same duty-cycle between the square-waves to avoid even-order harmonics in the generated sinusoid.

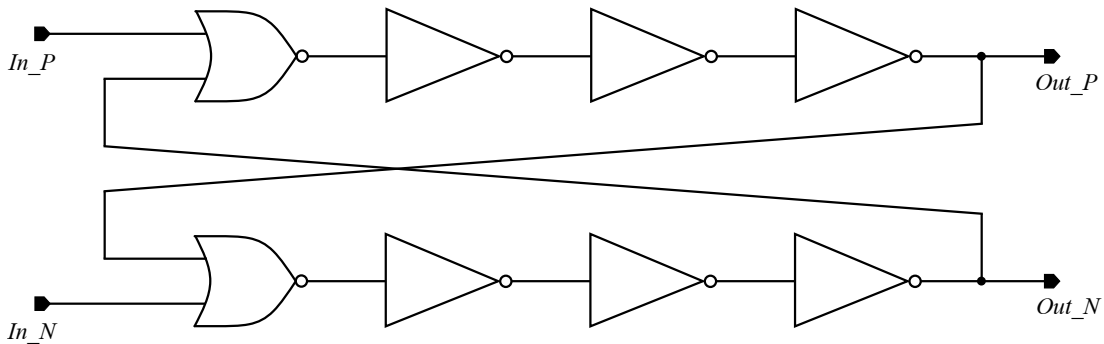


Figure 4.9: Classical non-overlapping signals generator.

In order to show the functionality of the non-overlapping buffer, transistor level electrical simulation of the designed block are performed under nominal conditions. Results are depicted in Fig. 4.10 where it is clear that differential signals intersect in a low voltage state.

As discussed in subsection 4.2, it is very crucial to reduce the skew between the complementary signals provided by the digital part of the generator, to conserve a 50% duty-cycle of the square-waves, and to respect the phase-shifts of $\frac{\pi}{3}$ and $\frac{\pi}{6}$ between signals, in order to avoid the apparition of even order harmonic components and to respect the harmonic cancellation conditions. Figures 4.11, 4.12 and 4.13 show the distributions of the relative phase-shifts, the duty-cycles, and the skews, respectively, of the different outputs provided by 100 iterations of Monte Carlo simulation of the digital part. Histograms in Fig. 4.11 show that the different phase-shifts are still centered around 30° and 60° , equivalent to $\frac{\pi}{6}$ and $\frac{\pi}{3}$, respectively, as provided by the circular shift-register in Fig. 4.5.

In addition to its principal role, providing differential signals with low voltage intersect, the non-overlapping buffer was designed to improve also the duty-cycles of

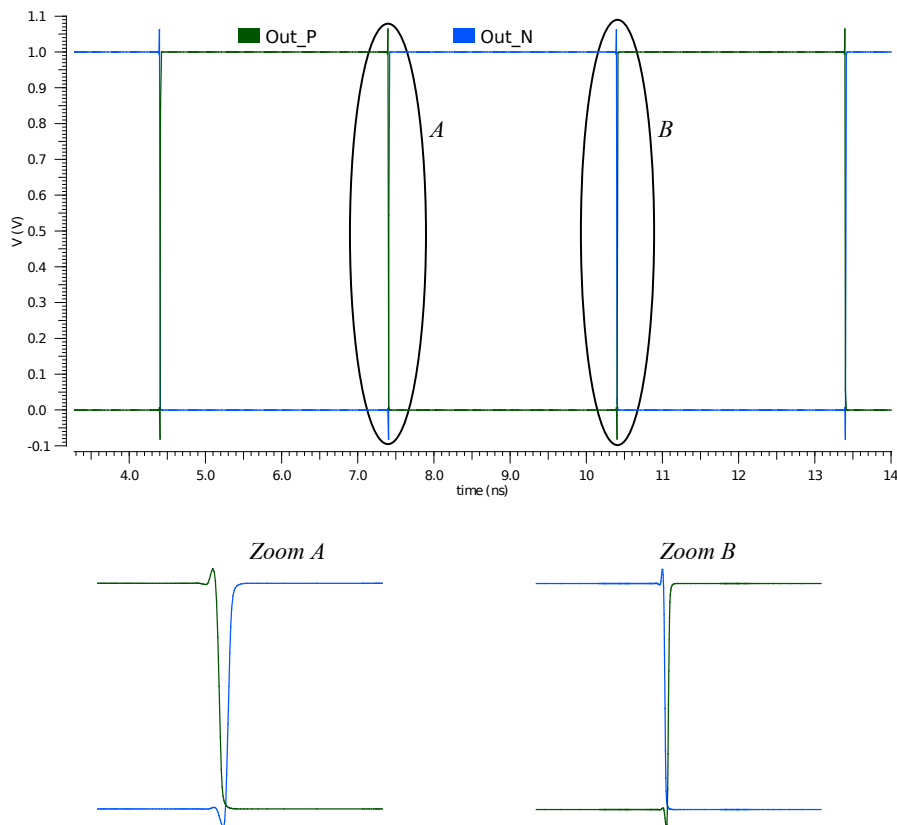


Figure 4.10: Outputs of non-overlapping buffer.

the square-waves generated originally from the circular shift-register. Histograms in Fig. 4.12 show the distributions of the duty-cycles of all square-waves provided by the digital part, including the circular shift-register, the double-ended buffer and the non-overlapping buffer, under Monte Carlo simulations involving 100 samples, in transistor level, against mismatch and fabrication process variations. Simulation results show the improvement of the duty-cycles which are around 49.98% with a maximum $\pm 1\sigma$ standard variation of 32.5m%, which complies with the design requirement of the digital bloc.

Another important key element to reach the desired performances of the designed sine-wave generator is the skew between the complementary square-waves. In fact, the square waves controlling the current steering DAC should be perfectly differential, with a low skew between the differential paths, in order to avoid even harmonic components in the spectrum of the generated signal. Histograms in Fig. 4.13 show the phase-shifts between complementary signals in both signal paths on the output of the digital part. Statistical simulation results show that phase-shifts

4.2 Hardware architecture of the sinusoidal signal generator

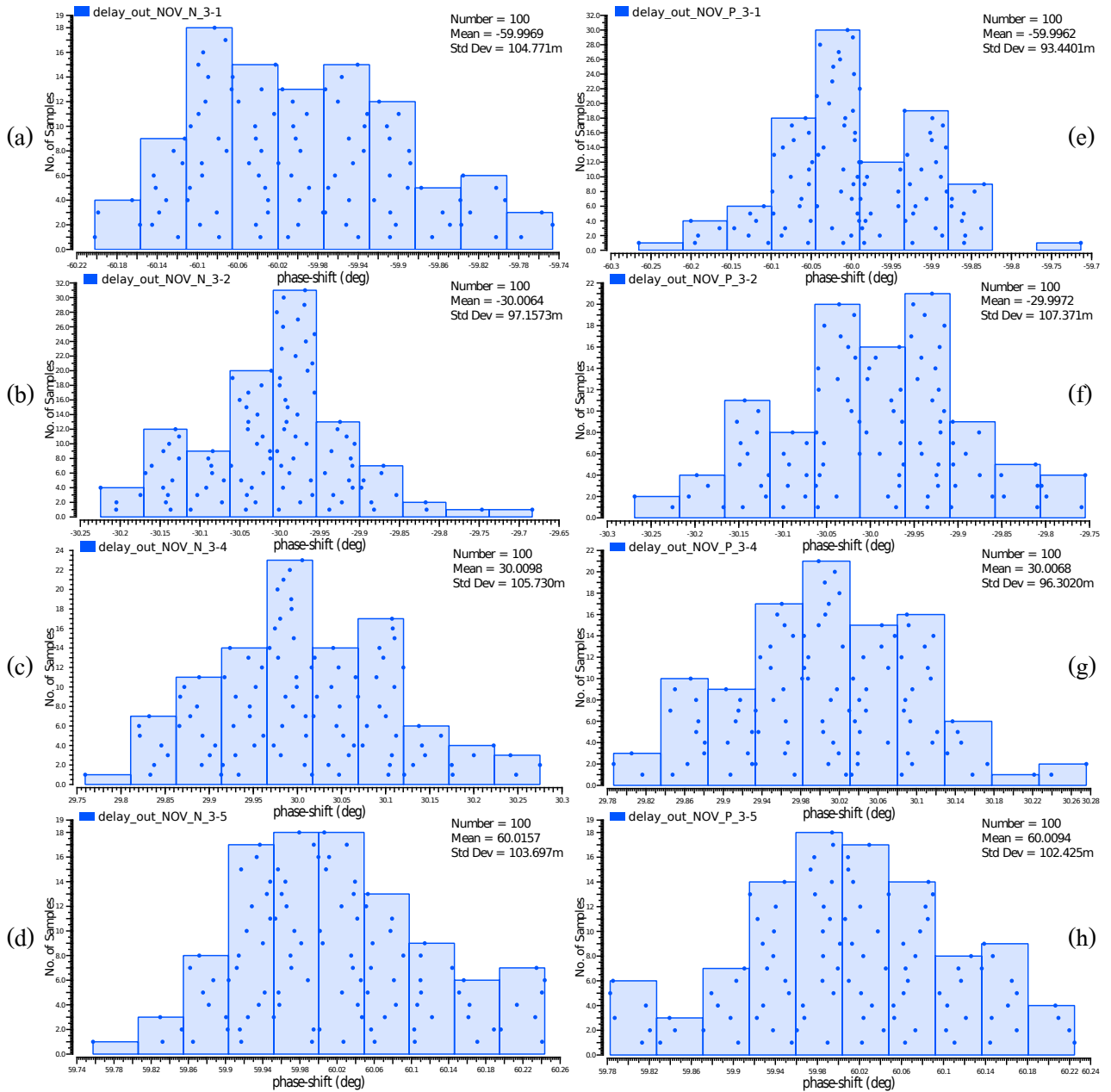


Figure 4.11: Histograms of phase-shifts of complementary outputs provided by the digital part, across 100 Monte Carlo iterations.

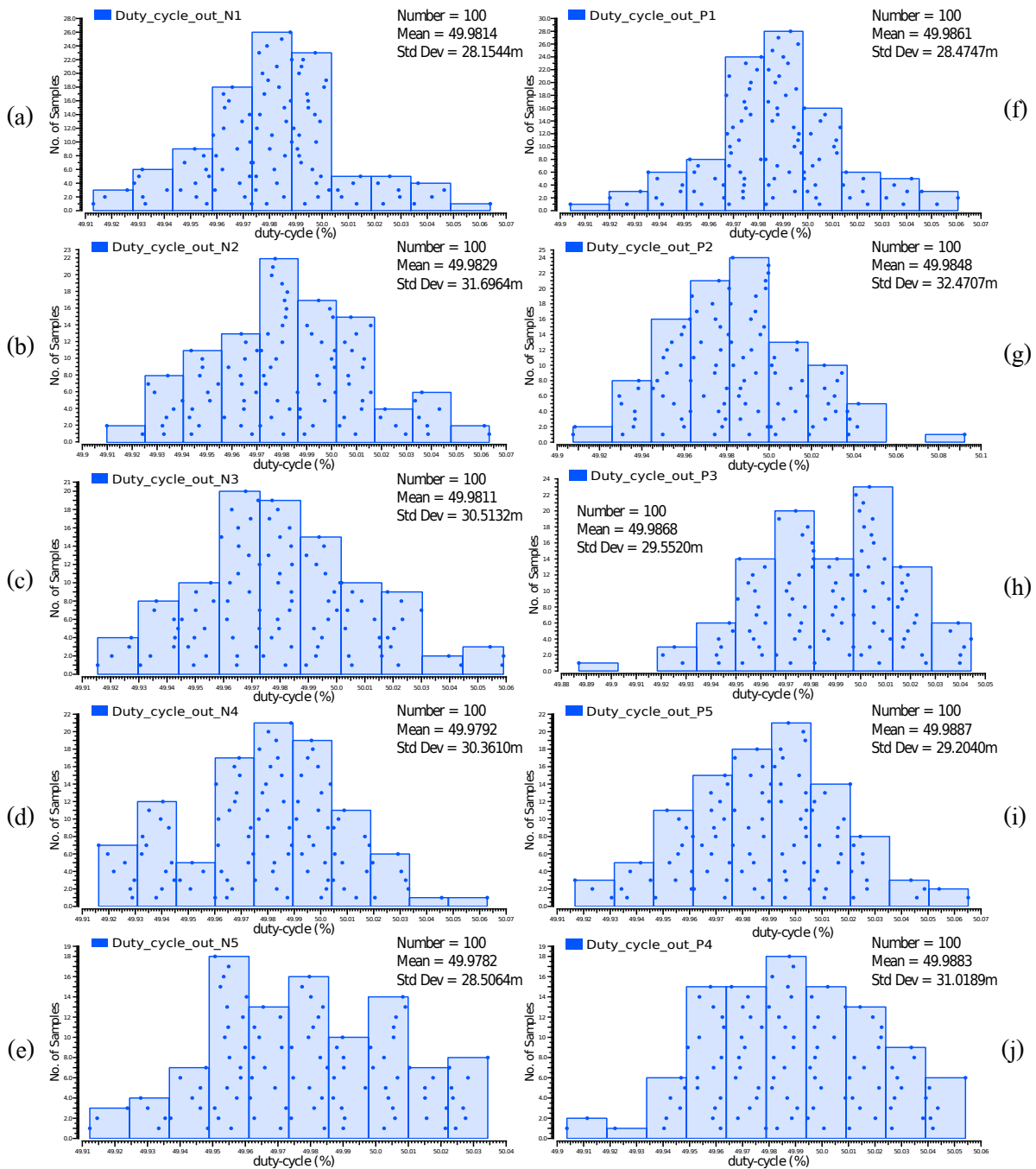


Figure 4.12: Histograms of duty-cycles of complementary outputs provided by the digital part, across 100 Monte Carlo iterations.

between all differential signals are centered around 180° with a weak variation.

4.2.4 D/A conversion

The set of time-delayed square-waves provided by the non-overlapping buffers drive a simplified current-steering *DAC* with five branches. Each branch is designed to generate a weighted current with weight ratios equal to $\alpha_1 = \frac{\sqrt{3}}{2}$ and $\alpha_2 = \frac{1}{2}$ as it was described in section 4.2. Figure 4.14 shows the transistor-level schematic of the basic current-source employed in the design. Transistor M1 is biased at a controlled voltage V_{bias} to generate a current that is then replicated by two current mirrors (M2 to M5). Transistor M6 is a cascode transistor to increase the output impedance of the current source. The output current is switched in a differential mode by switches M7 and M8 which are controlled by the time-delayed square-wave signals provided from the digital part of the circuit.

Table 4.2 lists the sizes of transistors used to design the basic current branch as in Fig. 4.14. The current mirrors have been sized and biased to provide three currents (100 μA , 86.67 μA and 50 μA), that correspond to the target weights ratios 1, $\frac{\sqrt{3}}{2}$ and $\frac{1}{2}$, respectively. The bias voltages used to generate the required currents are listed in Table. 4.3. The switches have been sized to reduce the parasitic capacitors at the transistor gates.

Table 4.2: Transistor sizes for basic current branch.

	M1=M4=M5	M2=M3	M6	M7=M8
W	150 μm	150 μm	500 nm	1 μm
L	150 nm	150 nm	32 nm	32 nm

The current provided by different current branches are summed at the input of the output filter. The combined currents provide a step-wise sinusoidal signal with five steps and the difference between two consecutive current steps is determined by the enabled branches of the current steering DAC. Figure 4.15 shows the transient electrical simulation of the designed 5-branches current steering DAC under nominal conditions, where the shift-register is clocked at 2 GHz.

Table 4.3: Bias voltages of the current branches.

V_{bias}	584 mV	593 mV	617 mV
I	100 μA	86.67 μA	50 μA

It is clear that the designed current ratios (that define the scale weights necessary for harmonic cancellation) are sensitive to mismatch and process variations.

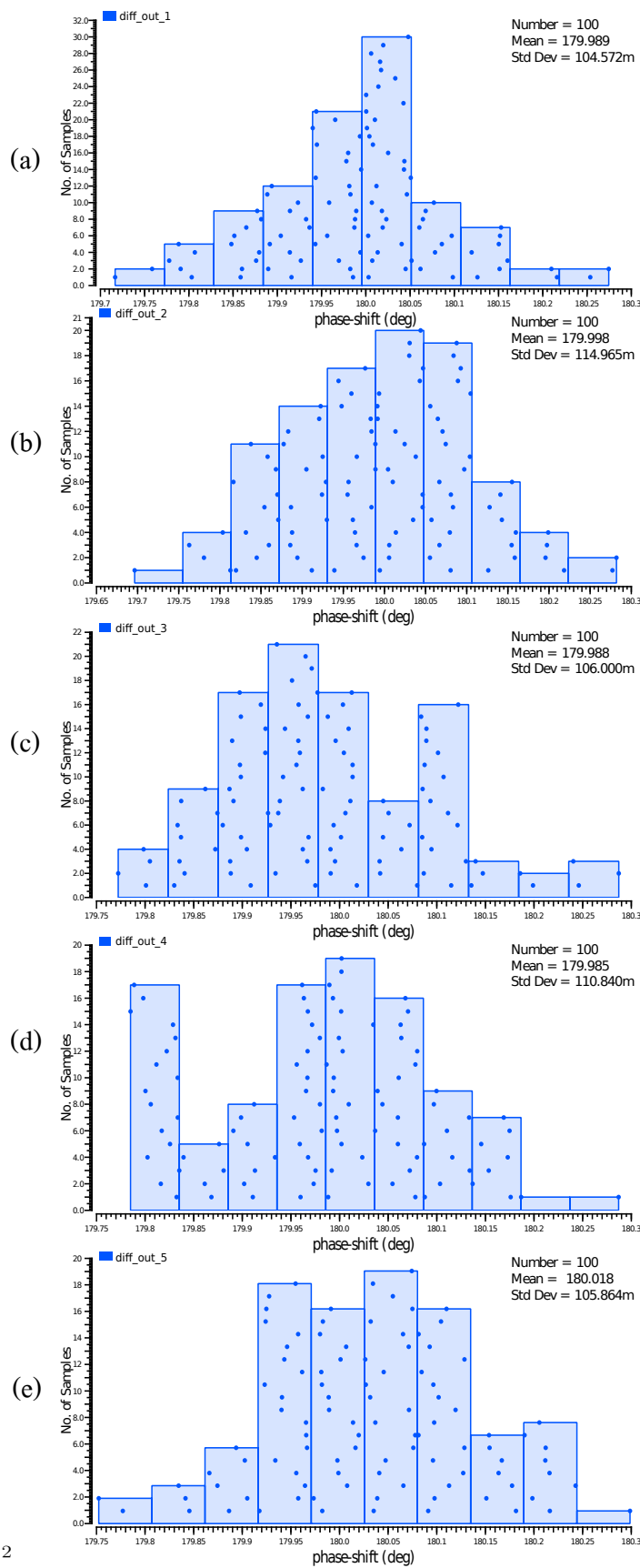


Figure 4.13: Histograms of skews of complementary outputs provided by the digital part, across 100 Monte Carlo iterations.

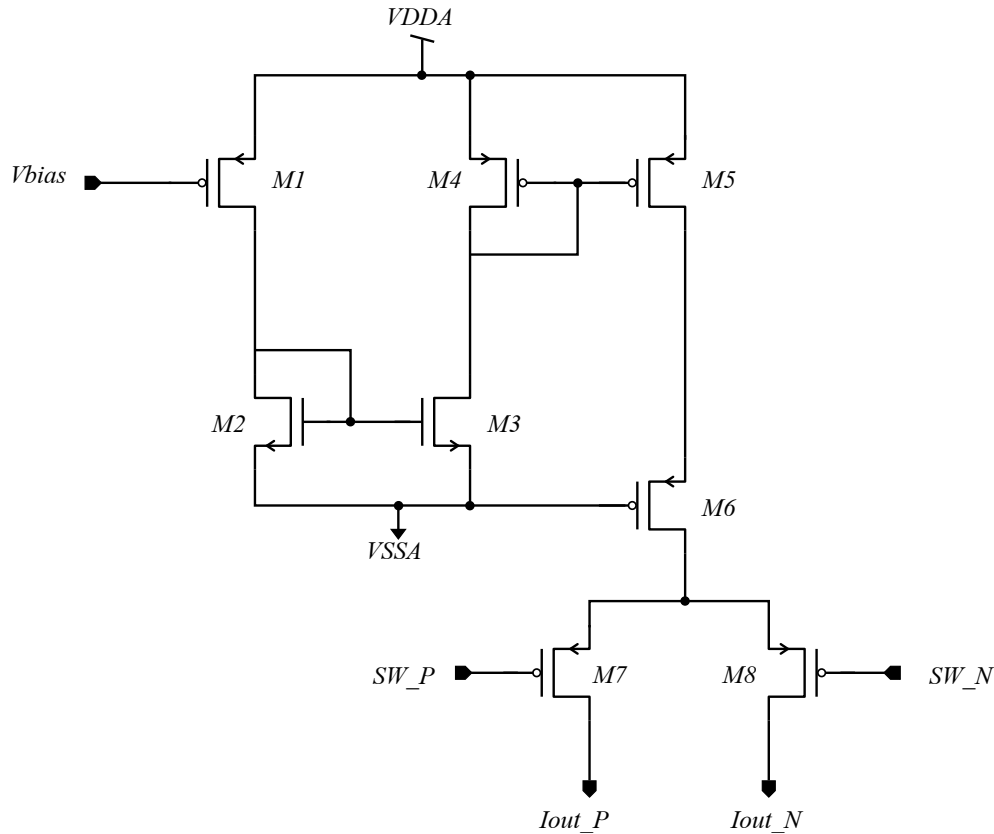


Figure 4.14: Basic current-steering digital-to-analog conversion branch.

These deviations from the target scale weights may have a significant impact in the performance of the harmonic cancellation strategy. In order to analyze the robustness of the current branches, Fig. 4.16 shows the histograms of the currents I_0 , I_1 and I_2 provided by Monte Carlo simulations of 100 samples regarding mismatch and process variations. Statistical distributions of currents show that all current branches provide current values centered around the nominal values required for this design ($I_0 = 100 \mu\text{A}$, $I_1 = 86.67 \mu\text{A}$ and $I_2 = 50 \mu\text{A}$) with a maximum variation below $1.8 \mu\text{A}$.

However the variation of the current branches impact directly the ratios between currents α_1 and α_2 (defined as $\frac{I_1}{I_0}$ and $\frac{I_2}{I_0}$, respectively) whose values are the most critical condition of the applied harmonic cancellation strategy. In order to analyze this effect, Fig. 4.17 shows the histograms of the generated ratios α_1 and α_2 obtained by process and mismatch Monte Carlo simulations across 100 samples. It is clear that the variation range of the scale weight ratios is above the target of 1% obtained in our analytical study in Fig. 3.27.a. For this reason, a simple calibration stage has been added in order to compensate the variation of

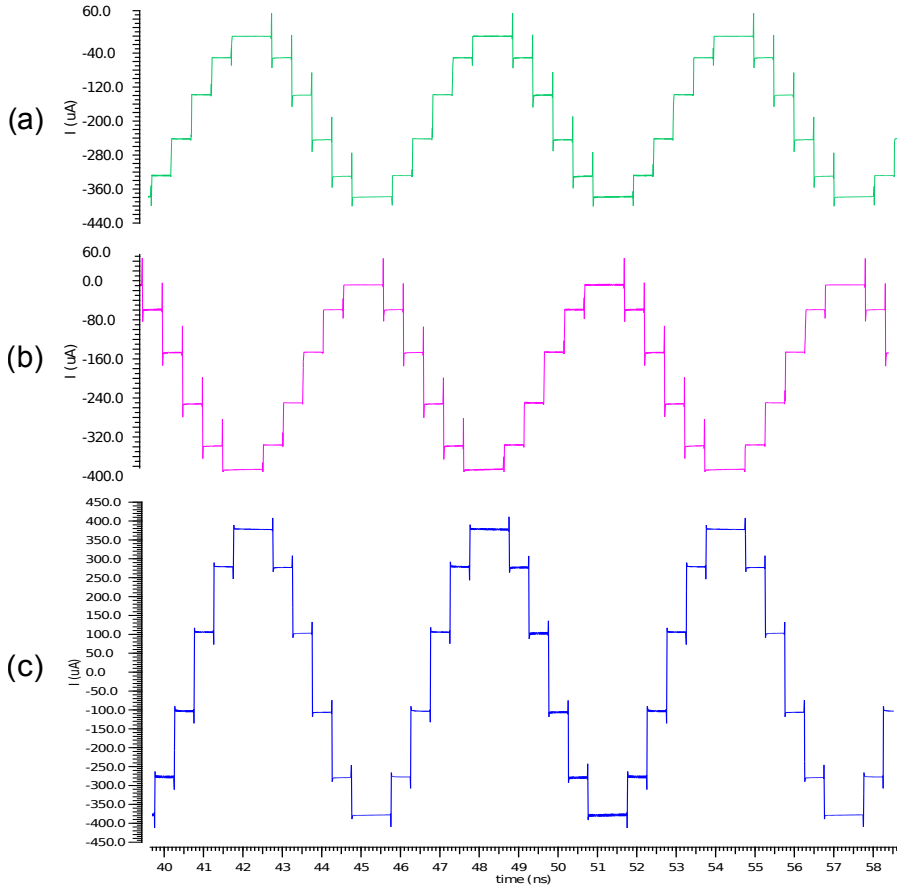


Figure 4.15: Output current waveform of the (a) positive path. (b) negative path. (c) differential output current.

the scale-weight ratios.

4.2.5 Bias circuit and harmonic cancellation calibration

The current supplied by each current source in the current-steering DAC is directly controlled by the set of bias voltages V_{bias_i} , $i = 1..5$. Given that the proposed harmonic cancellation relies on precise scale weights implemented as current ratios in the current-steering DAC, a precise control on these bias voltages is necessary to account for current variations due to process and mismatch. Figure 4.18 shows the transistor level schematic of the proposed bias circuit. It consists of a capacitor that can be charged and reset through NMOS switches. The capacitor is connected to a DC reference voltage V_{ref} via switch M_{1b} controlled by digital signal Set . Switch M_{2b} is connected to the ground to reset the capacitor. The voltage at node V_{bias} follows the exponential curve $V_{bias} = V_{ref}(1 - e^{-\frac{T_c}{R_{on}C}})$ where R_{on} is

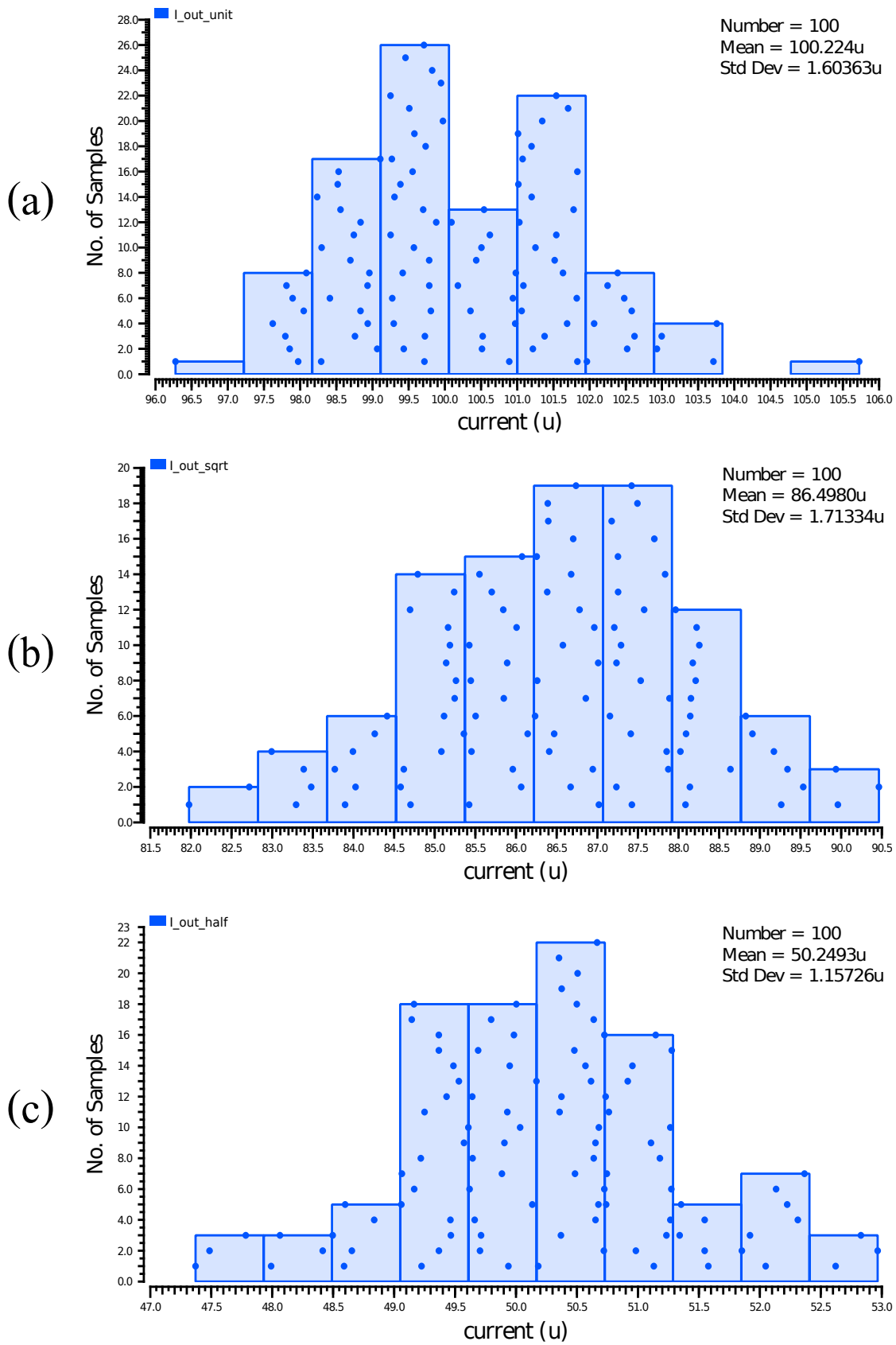


Figure 4.16: Histograms of output currents provided by the current branches, across 100 Monte Carlo iterations. 85

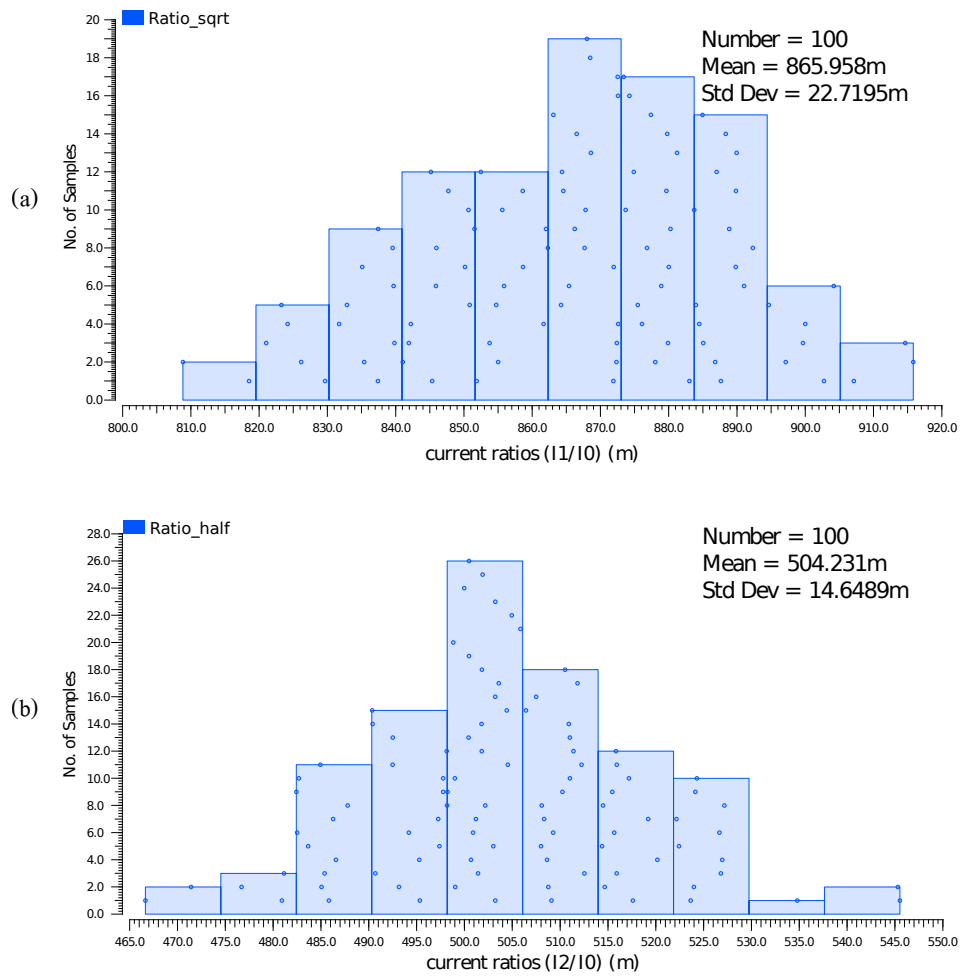


Figure 4.17: Histograms of current ratios provided by the current branches, across 100 Monte Carlo iterations.

the ON resistance of transistor M_{1b} , C is the value of the capacitor, and T_c is the charge time. This simple circuit allows controlling the bias voltage of each current-steering branch by programming the value of T_c .

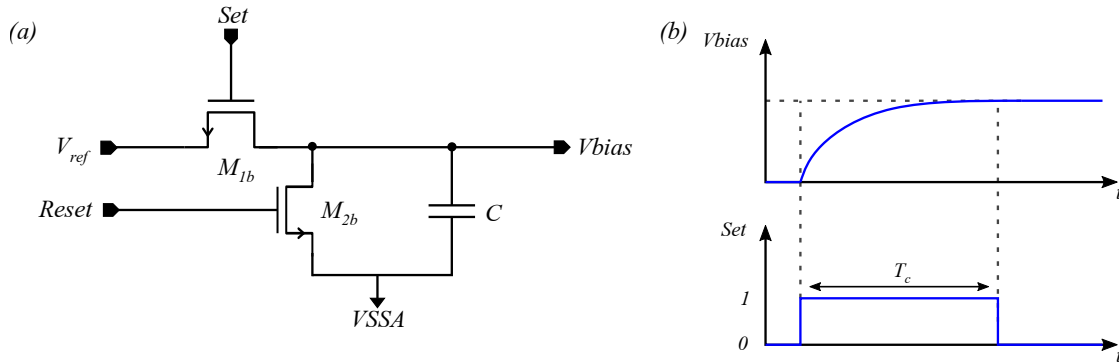


Figure 4.18: (a) Transistor-level schematic of the basic bias circuit. (b) Evolution of output voltage (V_{bias}) and control signal (Set).

In this design we use 5 bias circuits with 5 MOM capacitors of 1.7 pF. Under nominal conditions, the charge times T_{ci} providing the different bias voltages of the currents branches are fixed as in table 4.4. The NMOS switches were sized as minimum $\frac{W}{L} = \frac{80}{30}$ nm.

Table 4.4: Charge time for the bias circuits.

I_{out1}	I_{out2}	I_{out3}	I_{out4}	I_{out5}
50 μ A	86.67 μ A	100 μ A	86.67 μ A	50 μ A
T_{c1}	T_{c2}	T_{c3}	T_{c4}	T_{c5}
203 ns	136 ns	120 ns	136 ns	203 ns

The transient evolution of the bias voltages V_{bias_i} , $i = 1..5$, obtained by electrical simulations is shown in Fig. 4.19. It has to be noted that once transistors M_{1b} and M_{2b} are open, the capacitors start discharging through the parasitic resistors, so these values have to be refreshed if the generator has to run continuously. According to electrical simulation results, we show in Fig. 4.20, as an example, the transient evolution of the $I_0 = 100\mu$ A current branch. It is clear that the current remains within 0.1% of accuracy for 8 μ s, that correspond to 1333 periods of the generated sinusoidal signal for a 2 GHz master clock.

Several calibration algorithms of harmonic cancellation had been proposed in previous works such as the SFDR optimization algorithm presented in [46] based on measuring the harmonics of the output signal and tuning the phases of the square-waves to compensate the timing errors of the generators using a battery

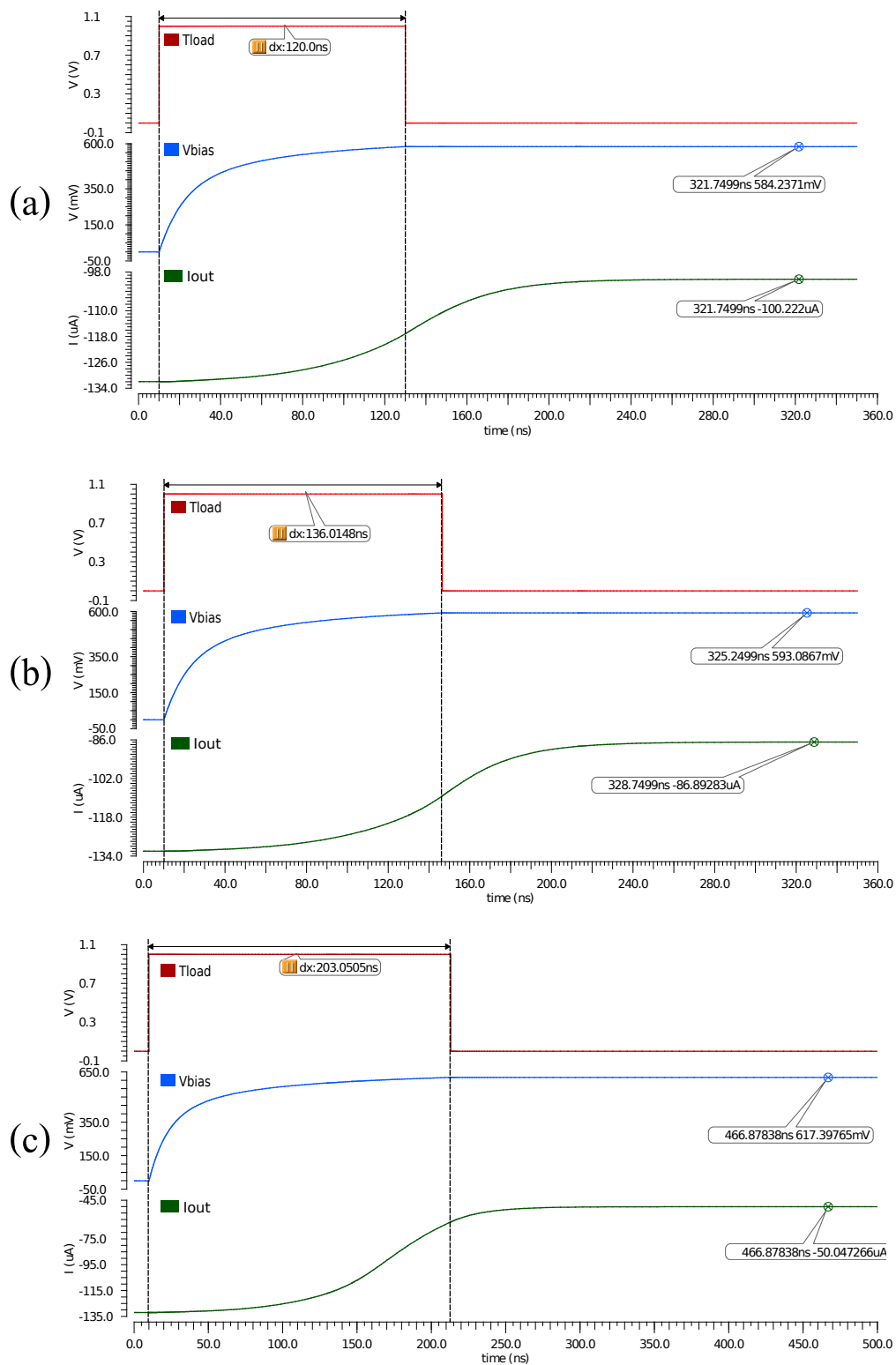


Figure 4.19: Evolution of output currents and bias voltages.

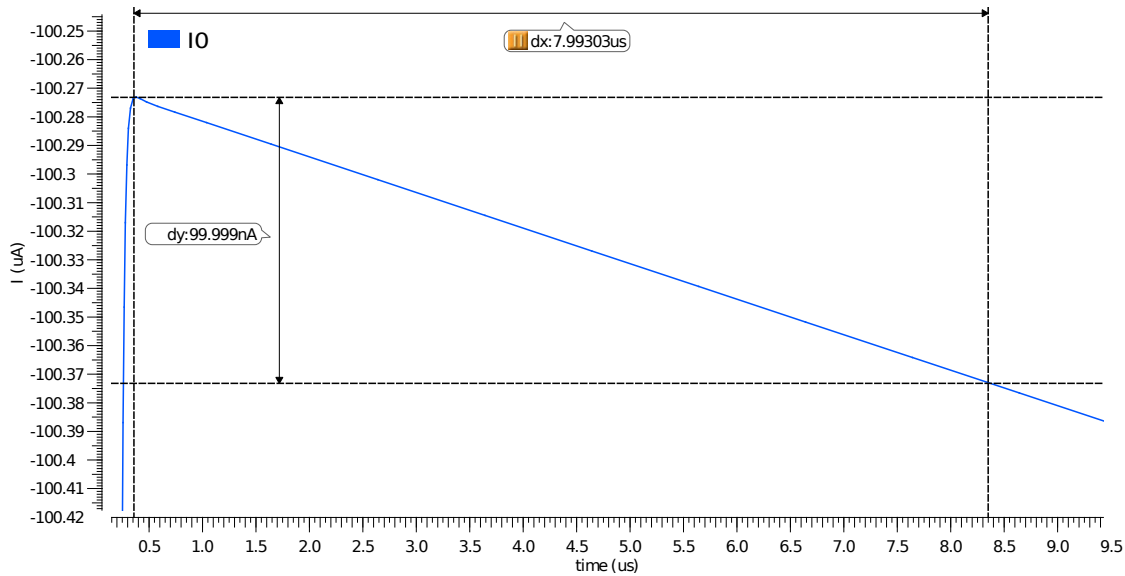


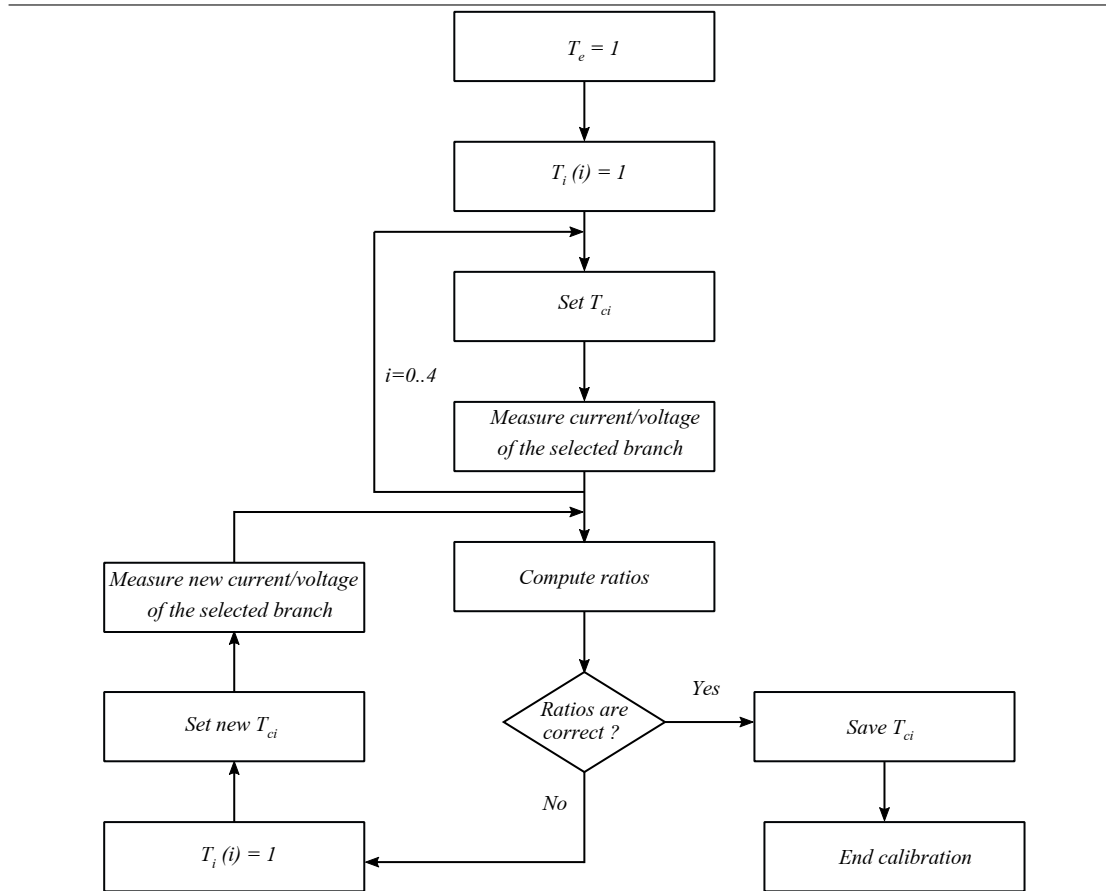
Figure 4.20: Transient current evolution of 100 μA current branch.

of capacitors. This calibration strategy requires additional on-chip equipment to implement an FFT function in order to convert the output signal to the frequency domain and to compute its SFDR.

In our work, we propose the iterative calibration algorithm in 4.1 that adjusts one current ratio at a time, using only DC measurements. The calibration technique starts by activating the calibration mode by setting signal T_e to a logic “1” in the circular shift-register, and then activating sequentially individual current-sources in a DC mode by means of the T_i signal corresponding to the selected current-path. The initial charge times T_{ci} controlling the current generated by each current branch are set to the nominal values provided by electrical simulations. Then, the actual output currents (or voltages) of all current-sources are measured, sequentially, to compute their ratios. If the resulting ratios are different from the nominal ratios fixed by the harmonic cancellation technique ($\alpha_1 = \frac{\sqrt{3}}{2}$ and $\alpha_2 = \frac{1}{2}$), charging times T_{ci} are modified and the ratios are measured and computed again. The process is iterated within a calibration loop until the measured ratios match the target scale weights within a predefined accuracy. Conventional optimization algorithms, such as a gradient-directed search [46] can be used to guide the search of the appropriate T_{ci} values within the calibration loop.

In this work the measurement of the current (or voltages) is external. However, due to the simplicity of the algorithm and the required resources, an on-chip implementation may be feasible using additional resources.

Algorithm 4.1 One current branch calibration algorithm.



4.2.6 Output filter

The output filter is used to remove higher-order harmonic components, non-affected by the harmonic cancellation. In our circuit, we propose to use a simple second-order passive low-pass filter, built as the cascade of a RC current filter ($R_1//C_1$) and a RC voltage filter (R_2C_2 series), as schematically shown in Fig. 4.21. This filter acts as summing node for the currents generated by the current-steering branches, and attenuates the magnitude of higher-order harmonics. The values of the components are listed in table. 4.5, using polysilicon resistors and MOM capacitors.

Table 4.5: Passive low-pass filter.

$R_1=R_2$	814Ω
$C_1=C_2$	1.7 pF

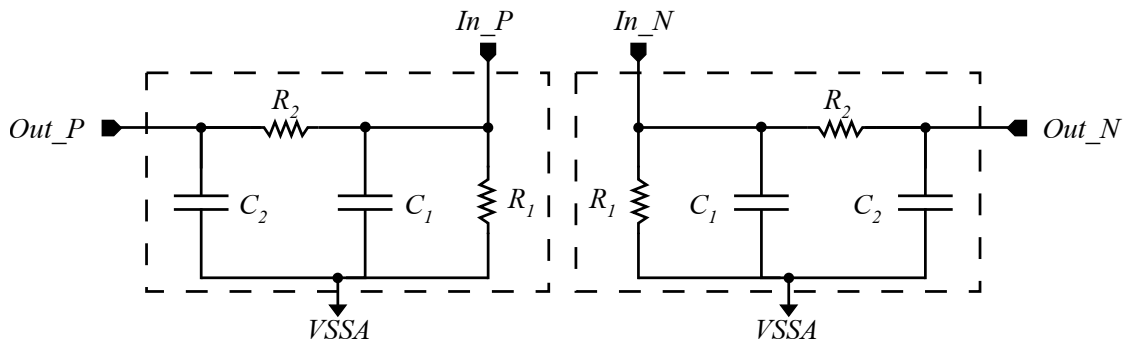


Figure 4.21: Second-order passive low-pass filter.

Figure 4.22 shows the diagram of the filter, $\frac{V_{out}}{I_{in}}$, obtained by electrical simulation. As it can be observed, the filter has been designed so that the output frequency of the generator (166.67 MHz for a 2 GHz master clock) lies on the edge of the rejection band to maximize the attenuation of higher-order harmonic components.

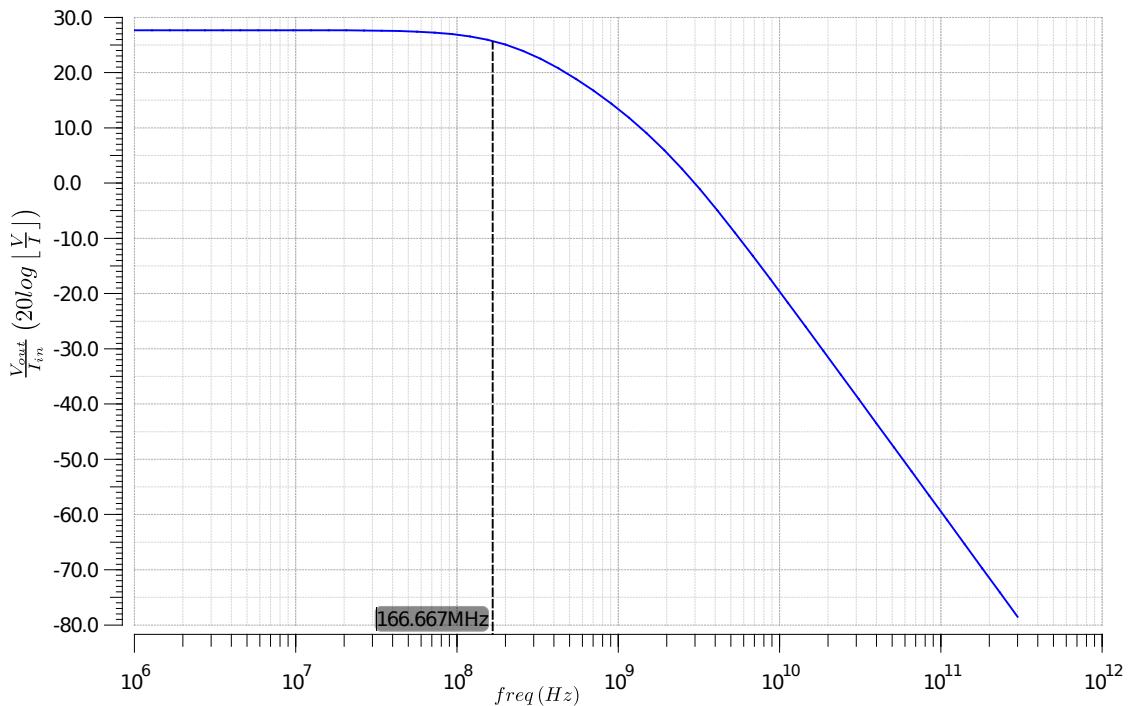


Figure 4.22: Output filter diagram.

4.3 System-level electrical simulation results

Electrical simulations of the complete system at transistor level are performed in order to show the feasibility and the performance of the proposed sinusoidal signal generator. The charge time T_{ci} of the bias capacitors used to control each current-steering branch are tuned to generate three current values: $I_0 = 100 \mu\text{A}$, $I_1 = 86.67 \mu\text{A}$ and $I_2 = 50 \mu\text{A}$ (as indicated in Table 4.4), corresponding to the scale weight ratios required for the harmonic cancellation technique: $\frac{I_1}{I_0} = \frac{\sqrt{3}}{2}$ and $\frac{I_2}{I_0} = \frac{1}{2}$. The circuit is clocked at $f_{clk} = 2 \text{ GHz}$ to generate a sinusoidal signal at a frequency equal to $\frac{f_{clk}}{12} = 166.67 \text{ MHz}$.

The initial configuration of the generator is programmed as in the timing diagram depicted in Fig.4.23. The initial load of the digital square wave into the circular-shift register is done as discussed previously in 4.2.1. The configuration of the current sources is controlled by the pulse-widths of signals Set_i defined by the charge times T_{ci} which are set as in Table 4.4.

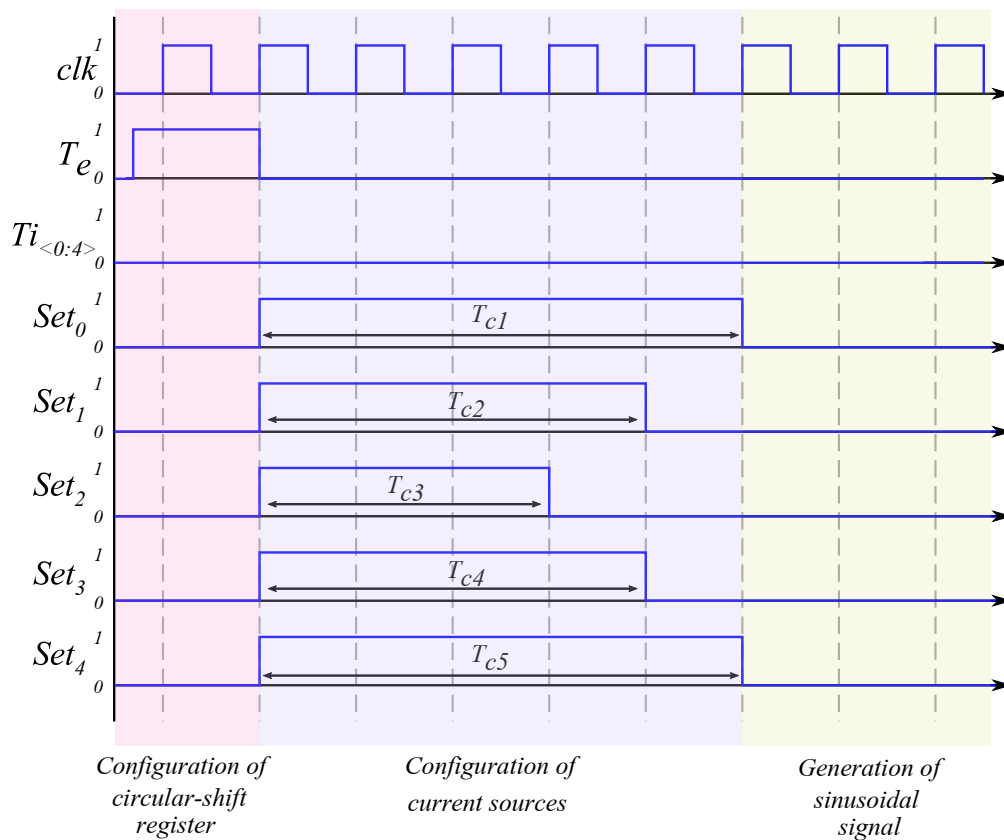


Figure 4.23: Configuration time diagram of the sinusoidal signal generator.

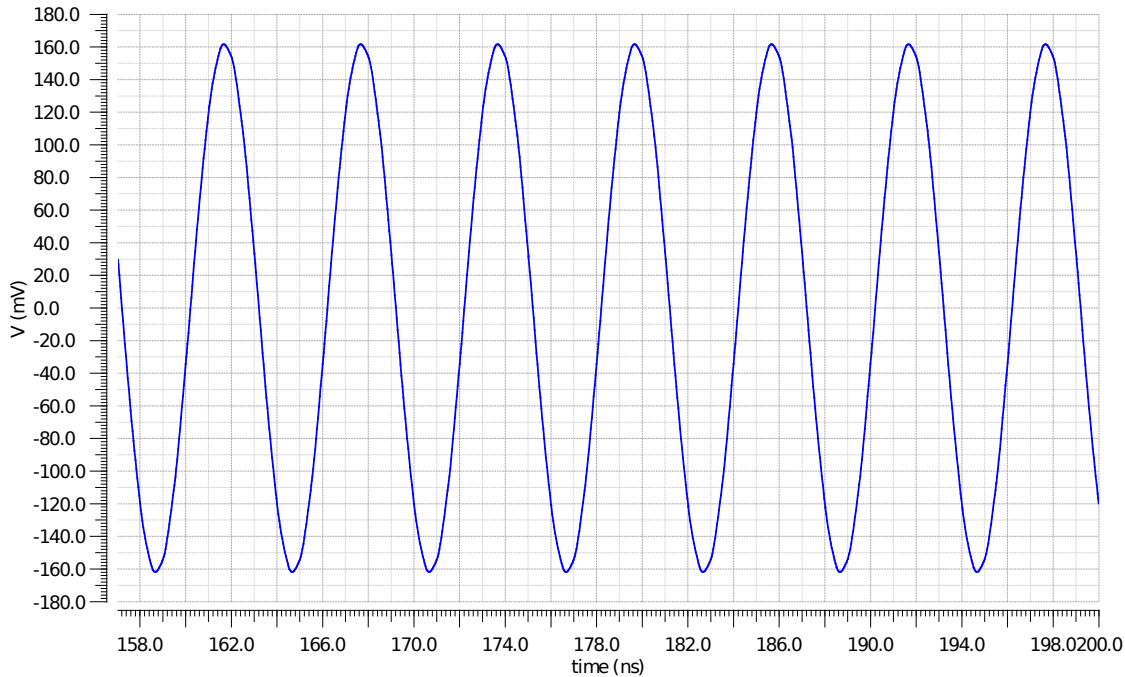


Figure 4.24: Generated sinusoidal output signal under nominal conditions.

Figure 4.24 shows the waveform of the generated sinusoidal signal with a differential amplitude of 320 mVpp. The quality of the generated output signal is evaluated in terms of its THD and its SFDR. It is important to remark that in the reported results, measurements are performed up to the tenth-order harmonic to prove the feasibility of the harmonic cancellation technique. The eleventh harmonic component is not cancelled and its magnitude—defined only by the spectral content of the square-wave and the order of the output filter—is constant for all the presented experiments. In the proposed implementation with a second-order low-pass output filter, the eleventh harmonic component has a magnitude of -56 dBc.

Figure 5.7 shows the spectrum of the generated signal at the output of the filter obtained from a transistor level simulation in the typical corner of the technology. As expected, the spectrum clearly shows that all odd harmonic components below the eleventh component are attenuated. Additionally, the absence of even order harmonics is an evidence of the low skew in the duty-cycle of the time-delayed set of square-waves. Under typical corner conditions, the generated sinusoidal signal has a THD = -78 dB and a SFDR = 81 dB. However, these nominal performance results have to be interpreted as an upper limit. Indeed, as discussed in chapter 3 and in our previous works [54] and [55], the performance of the proposed generation technique is very dependent on mismatch and process variations

which introduce additional scaling errors and timing delays. Errors in the scale weight ratios will limit the effectiveness of the cancellation for the odd harmonic components, while timing deviations of the square-waves will introduce even-order harmonic components.

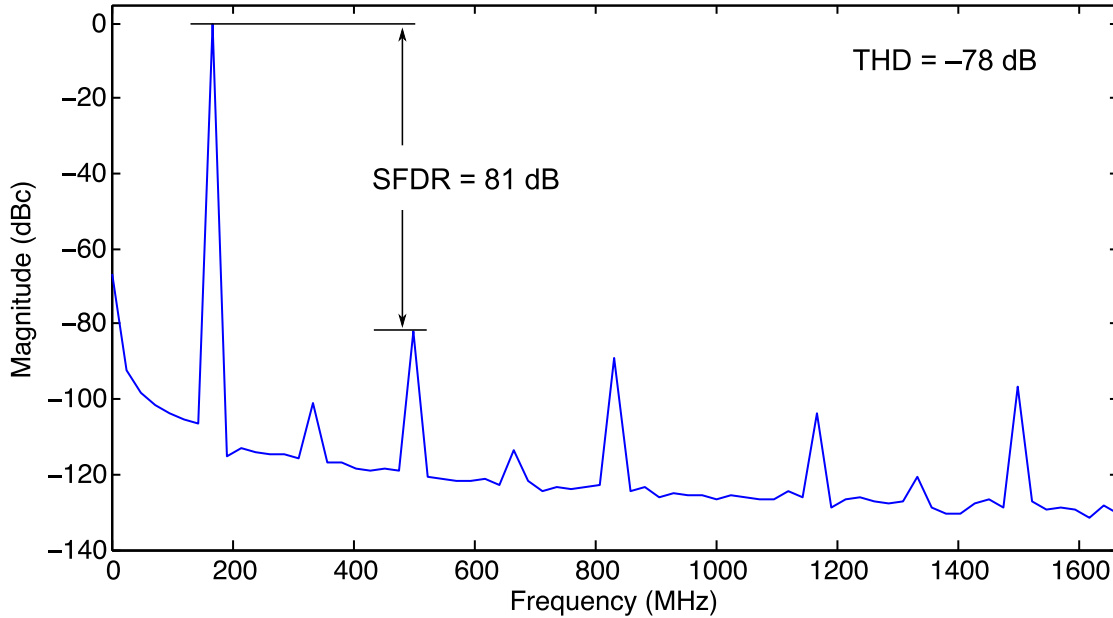


Figure 4.25: Spectrum of the generated sinusoidal output signal under nominal conditions.

In order to evaluate the performance of the proposed generator in the presence of technological variations, we perform a set of transistor level Monte Carlo simulations considering both the process and mismatch variations included in the statistical corner of the technology. Figures 4.26.a and 4.26.b show the THD and SFDR of the generated sinusoidal signal, respectively, for 100 Monte Carlo iterations. These simulations were performed without calibrating the current ratios (i.e., the charging times T_{ci} defining the currents in the current-steering branches were kept constant at nominal values). It is clear to see a significant degradation of the performance: the mean values of the linearity metrics are $\text{THD}_{mean} = -50$ dB and $\text{SFDR}_{mean} = 52$ dB. Interestingly, results also show that the main source of degradation of the harmonic cancellation is the mismatch of the current-steering sources, which deviates the current ratios from their nominal values, limits the effectiveness of the cancellation of odd-order harmonics, and introduces even-order harmonics due to mismatch between the positive and negative branches of the fully-differential signal paths. On the other hand, variations on the duty cycle of the time-delayed square-waves due to process and mismatch are very well controlled, with a worst-case variation of only 0.03% from the target 50% duty-cycle.

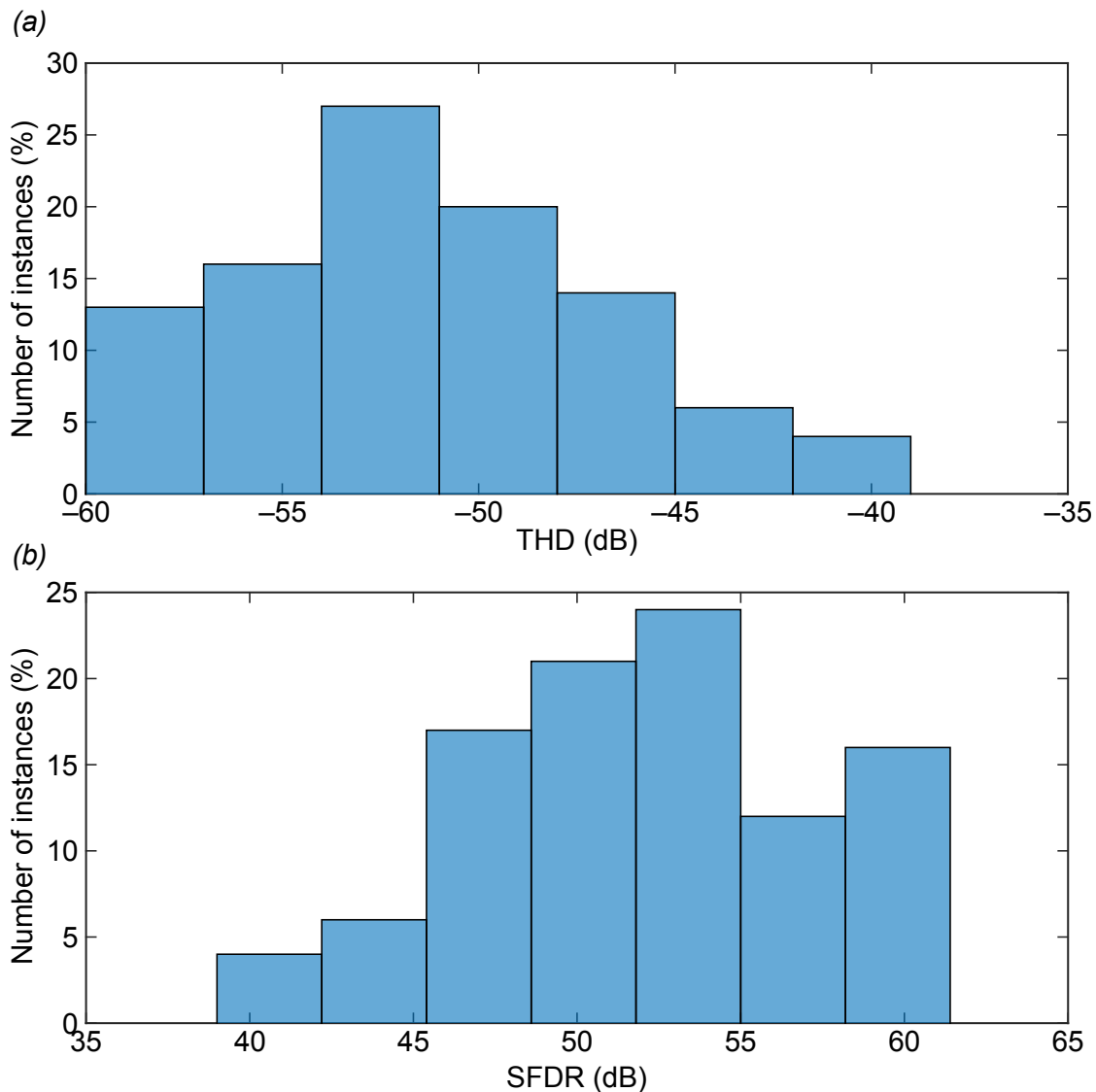


Figure 4.26: Histograms of (a) THD and (b) SFDR of the generated sinusoidal signal across 100 Monte Carlo simulations.

Additional insight can be obtained by analyzing individual spectral components. Thus, Figure 4.27.a) and 4.27.b) show histograms of the magnitude of the second and third harmonic components of the generated output, respectively, for the 100 Monte Carlo simulations. It is clear that the impact of process and mismatch on the third-order component dominates over the effect on the second. That means that the degradation of the current ratios has a larger impact in the linearity of the generator than the mismatch between the differential branches. This strongly

supports our choice of calibrating only the current scale-weights, since they are the dominant contribution to the generator non-linearity.

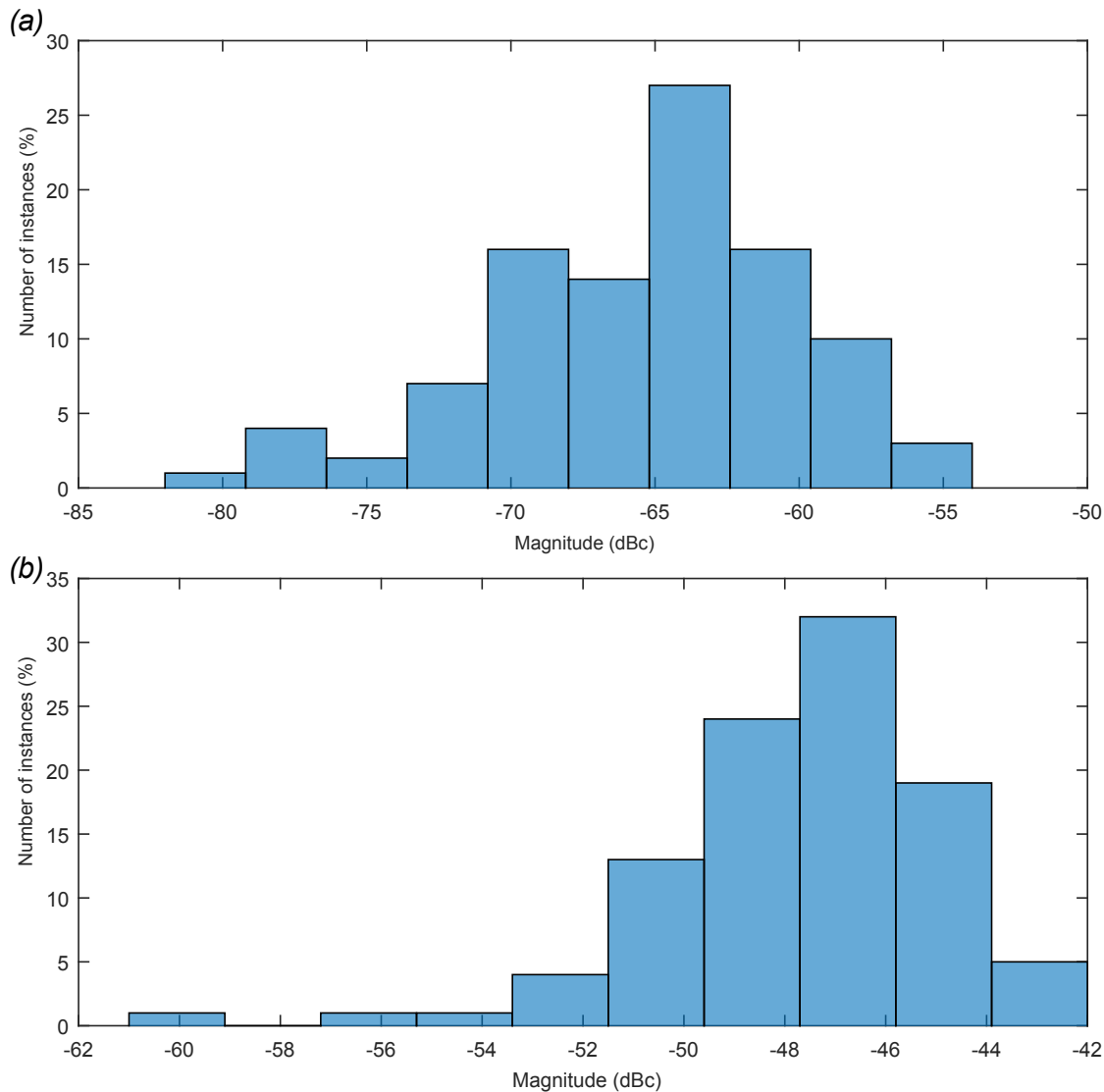


Figure 4.27: Histogram of the magnitude of: (a) second harmonic component; (b) third harmonic component, across 100 Monte Carlo iterations without calibration.

In order to show the feasibility of the proposed calibration technique, we selected the worst-case generator obtained by process and mismatch Monte Carlo simulation. The spectrum of the generated output sinusoid for this worst-case generator is plotted in Fig. 5.11 which presents a THD= -39.5 dB and a SFDR= 40 dB. As it was discussed in the previous section, the proposed calibration algorithm tunes

the currents in the current-steering branches in order to calibrate the current ratios that define the scale weights for the harmonic cancellation. The spectrum of the generated sinusoidal output after calibration is plotted in Fig. 5.12. It is clear that odd-order harmonics are greatly attenuated after the calibration. The linearity of the calibrated signal is significantly improved, with a THD= -66.7 dB and a SFDR= 70 dB, which corresponds to a 30 dB improvement with respect to the uncalibrated generator. In fact, the linearity of the calibrated generator is limited by the uncompensated even-order harmonics. These even-order harmonics are due to mismatch between the fully-differential signal paths and cannot be compensated by the proposed calibration.

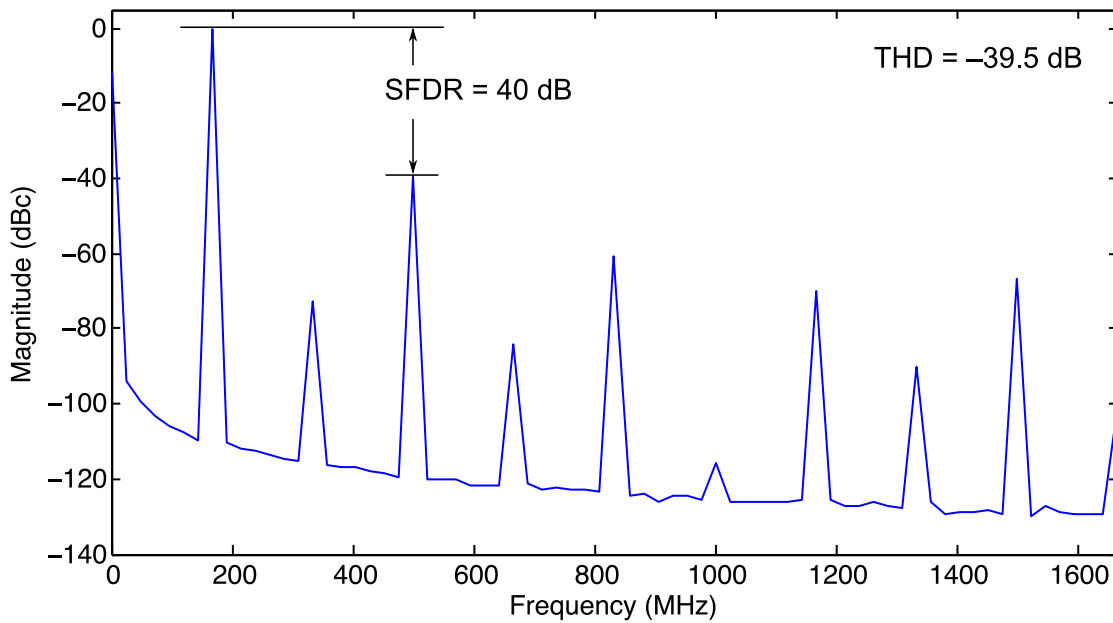


Figure 4.28: Spectrum of the generated sinusoidal output signal under worst-case process and mismatch variations, before calibration.

Table 4.6 compares the performances of the proposed sinusoidal signal generator to the state-of-the-art. The generators presented in this comparison are based on the harmonic cancellation technique and built using mostly digital circuitry. Thus, the work in [51] employs a circular shift-register for the generation of time-delayed square-waves, although a complete DAC with DEM is used for analog signal reconstruction. The generators in [45], [46], on the other hand, use digital ring oscillators and resistive summing networks. Regarding the performance of the proposed generator, in terms of generated frequency and linearity our proposal compares very well to the state-of-the-art.

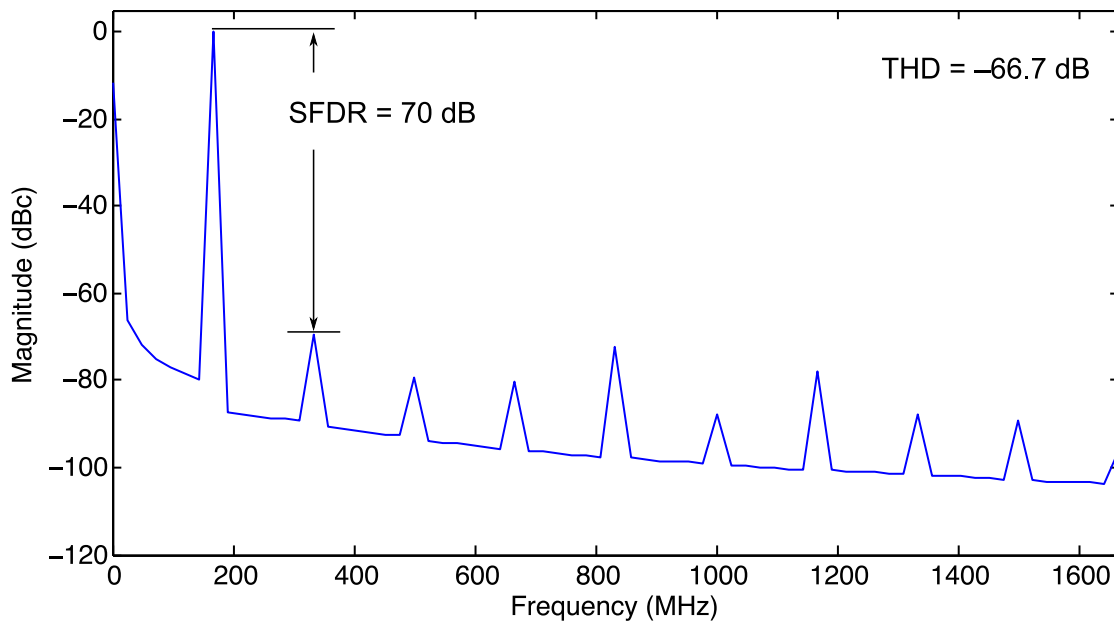


Figure 4.29: Spectrum of the generated sinusoidal output signal under worst-case process and mismatch variations, after calibration.

Table 4.6: Comparison to the state of the art.

	This work ¹	[51]	[46]	[45]
Process	FDSOI 28nm	CMOS 130nm	CMOS 180nm	CMOS 0.13 μ m
Generated frequency	166.7MHz	2MHz	150MHz–850MHz	10MHz
SFDR/THD (without calibration)	52dB/ – 51.2dB ²	68.7dB/ <i>NA</i>	50.4dB/–46dB@150MHz	<i>NA</i> / – 72dB
SFDR/THD (with calibration)	better than 70dB/ – 67dB ³	71.6dB/ <i>NA</i>	60.3dB/- 54.9dB@150MHz	no calibration

¹results obtained from MC simulations.

²Mean values from 100 MC simulations.

³Calibration of worst case MC run.

4.4 Physical implementation of a proof-of-concept sinusoidal signal generator

This PhD project has been carried out as collaboration with STMicroelectronics in the framework of the NANO2017 program. STMicroelectronics was in charge of fabrication and characterization of the sinusoidal signal generator prototype. In order to align our thesis schedule with STMicroelectronics internal tape-out schedule, we were offered to adapt the previously presented design to a simplified proof-of-concept prototype that could be characterized at wafer level using a probe station. Thus, the design was modified in order to comply with the constraints of the proposed test setup, namely:

1. Maximum 12 DC pads available for I/O and power supplies.
2. 1 RF pad GSG for external clock signal. The clock signal is provided by an external oscillator.
3. 1 RF differential pad GSGSG for the output.
4. Adapt the output impedance of the circuit to $50\ \Omega$.
5. The output power of the generated main tone has to be above $-20\ \text{dBm}$, for meaningful measurements with the available spectrum analyzer, that has a noise floor around $-100\ \text{dB}$.

In order to comply with the mentioned requirements, the previously presented design was modified:

- The bias capacitor for calibration were removed to reduce the number of DC inputs. An alternative solution for configuring and calibrating the current sources was adapted, manually, based on tuning the bias voltages directly instead of tuning the charging times as discussed in 4.2.5.
- The bias voltage of the central current-branch (I_3) is embedded on-chip by means of a voltage divider to reduce the number of DC pads. This reduces the calibration flexibility.
- The analog and digital power supply are connected together to reduce the number of DC pads. Due to this modification, there is a risk to increase the noise in the analog part coming from the digital part of the circuit.
- The $50\ \Omega$ input impedance of the probe setup reduces the output power of the generator below the $-20\ \text{dBm}$ limit imposed by the spectrum analyzer. In

order to increase the output power, the bias current of each current-steering branch was doubled. The updated bias voltages and corresponding currents are listed in table. 4.7

- A clock tree has been designed to route the external master clock to the shift-register. The developed clock tree, shown in Fig. 4.30, uses dedicated clock buffers from the standard cell library of the 28nm FDSOI technology.

Table 4.7: Bias voltages of implemented current sources.

I_{out1}	I_{out2}	I_{out3}	I_{out4}	I_{out5}
$100\mu A$	$173.34\mu A$	$200\mu A$	$173.34\mu A$	$100\mu A$
V_{bias1}	V_{bias2}	V_{bias3}^*	V_{bias4}	V_{bias5}
$593mV$	$567mV$	$560mV$	$567mV$	$593mV$

* V_{bias3} is implemented on-chip within a voltage divider

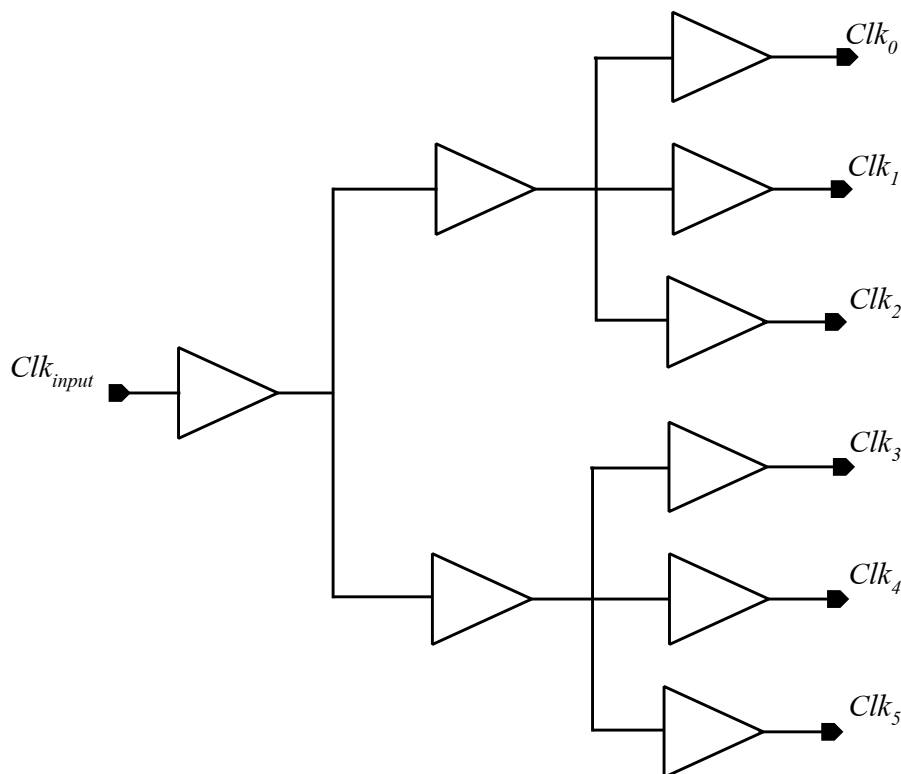


Figure 4.30: Clock tree circuit.

The proof-of-concept version of the generator was simulated in the same conditions as the previously presented generator ($f_{clk} = 2$ GHz and $f_{out} = 166.67$

MHz). Figure 4.31 shows the transient electrical simulation of the output currents of the current steering DAC under nominal conditions, where the shift-register is clocked to 2 GHz. The amplitude of the output signal, as shown in Fig. 4.32, is decreased to 60 mVpp and its power is equal to -20 dBm which is acceptable for the spectrum analyzer. In terms of linearity, the output signal still has a low THD= -79 dB and a SFDR= 82 dB, as shown in Fig. 4.33. The set of harmonic components selected to be canceled in this configuration, which are the 3^{rd} -, 5^{th} -, 7^{th} - and 9^{th} -order harmonics, are all below -90 dBc which means that they are well attenuated. However the linearity of the proof-of-concept version is limited by the second order harmonic equal to -82 dBc, due to the skew between the two differential paths.

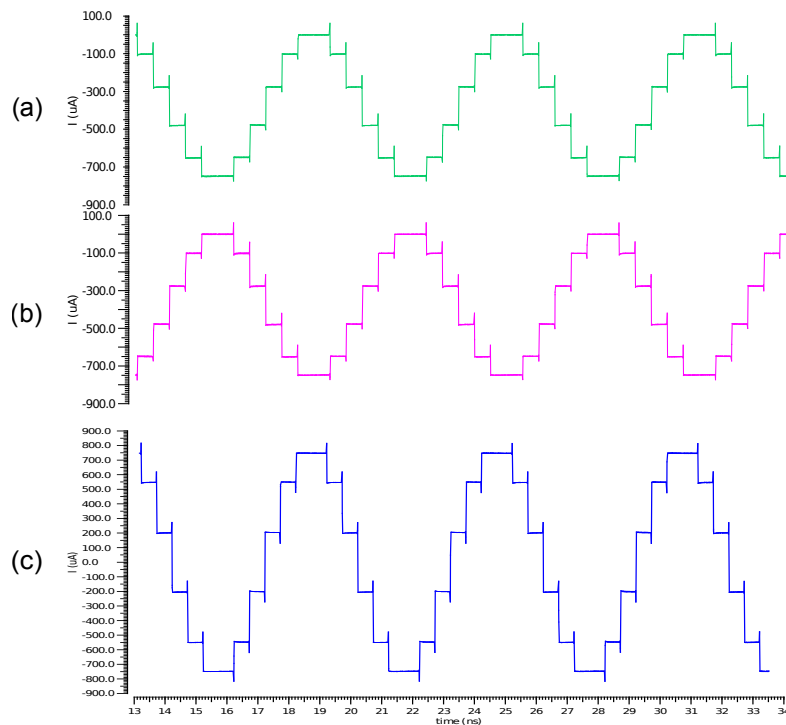


Figure 4.31: Output current waveform of the proof-of-concept version: (a) positive path; (b) negative path; (c) differential output current.

4.4.1 Layout of the sinusoidal signal generator

Figure 4.34 shows the layout of the proof-of-concept prototype. The layout was developed according to the design rules of the 28 nm FDSOI technology and following mixed-signal conventional layout practices. Thus, the analog and digital sections are clearly separated. We minimized the number of crossing analog and digital

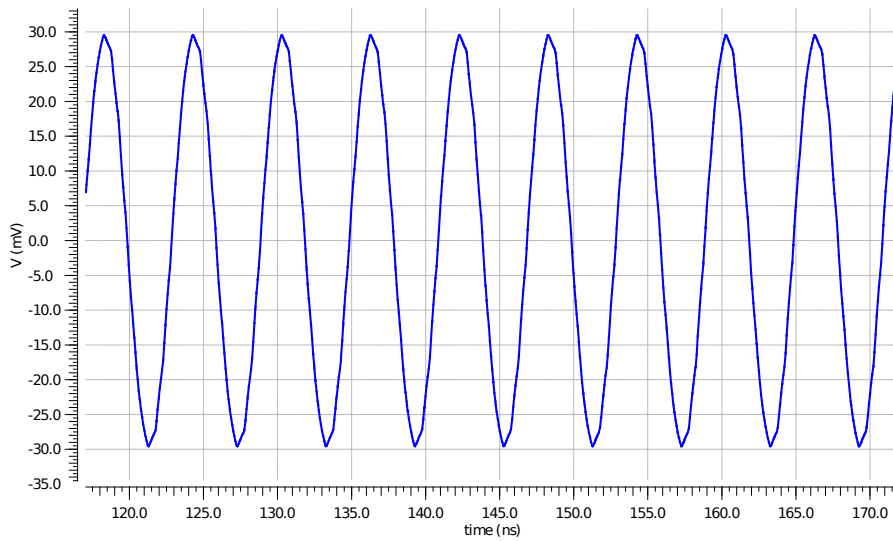


Figure 4.32: Output sinusoidal signal of the implemented circuit.

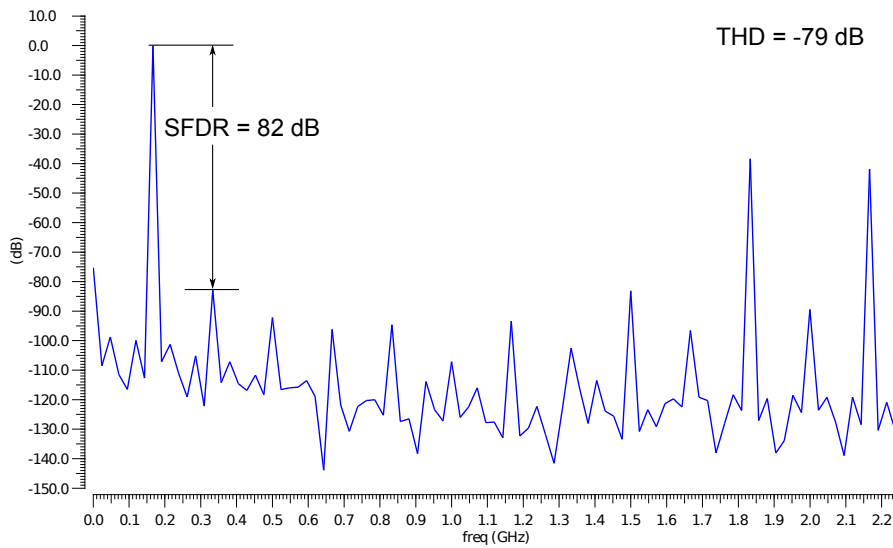


Figure 4.33: Spectrum of the output sinusoidal signal of the implemented circuit.

paths, and added appropriate shielding when necessary. The current sources have an identical layout to improve matching, while the output filter is laid out to keep a differential path to the output pads. Decoupling capacitors have been added to sensitive DC nodes.

The digital section is laid out in a symmetrical fashion with respect to the central vertical axis of the circuit, while the routing of the phase-shifted square-waves to the analog section has been carefully designed to provide the same length for the different signals in order to avoid imbalanced delays. The area of the circuit is $140\ \mu\text{m} \times 80\ \mu\text{m}$.

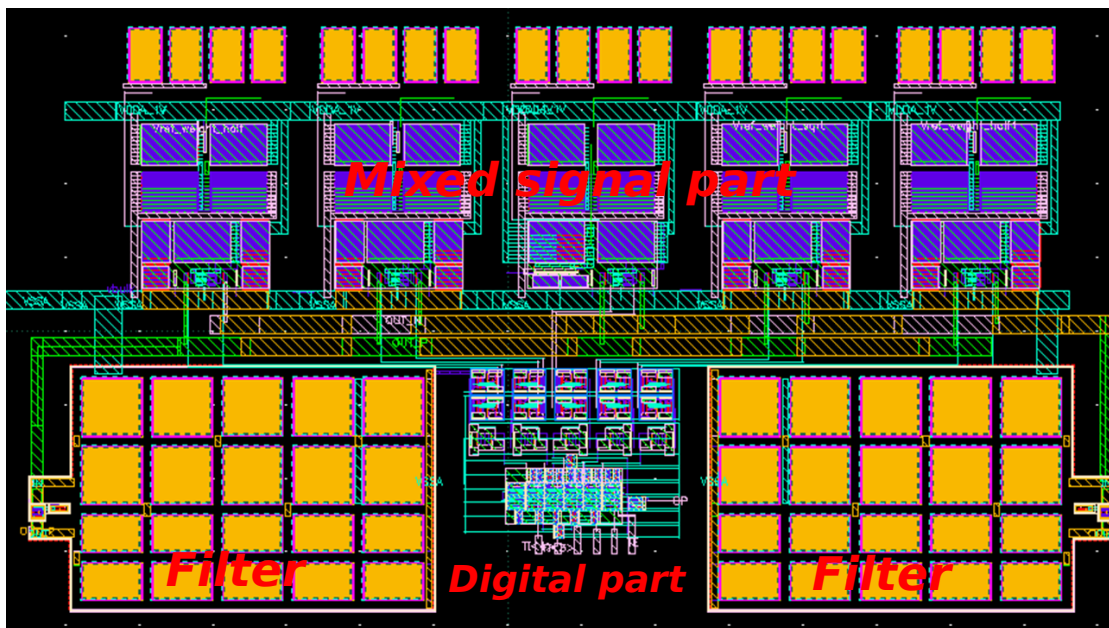


Figure 4.34: Layout of the core of the sinusoidal signal generator.

Regarding the pad frame of the prototype, it has to be carefully laid out in order to interface correctly to the probe heads in the test equipment. This imposes strict geometrical constraints to the size, position and orientation of the pads. The available tester requires $100\ \mu\text{m}$ by $75\ \mu\text{m}$ pads, with a pitch of $100\ \mu\text{m}$. Additionally, horizontal and vertical pad lines should be separated by $300\ \mu\text{m}$, as depicted in Fig. 4.35.

The layout of the prototype including the pad frame is depicted in Fig. 4.36. Clearly, the long distances between the pads and the core imposed by geometrical constraints of the pad frame, may introduce parasitic elements that may impact the performances of the circuit. In order to minimize these parasitics, routing paths to pads had been laid out as stacks of metal layers connected by matrix of vias. The area of the prototype including pads is $1.56\ \text{mm}$ by $0.9\ \text{mm}$.

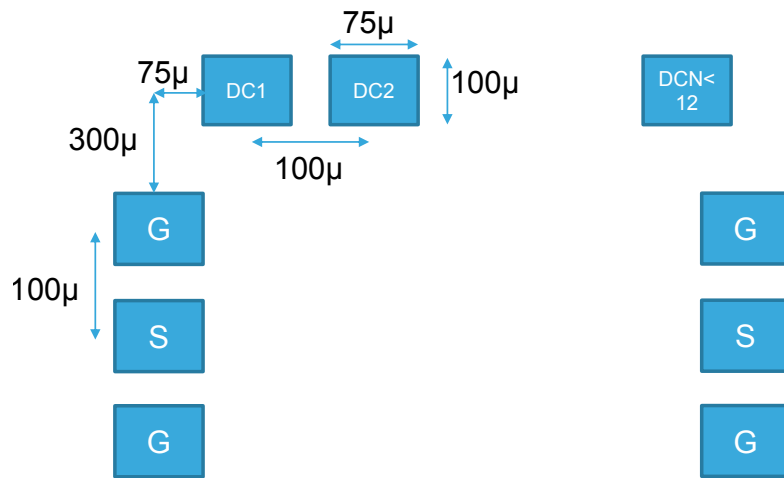


Figure 4.35: Pad frame constraint.

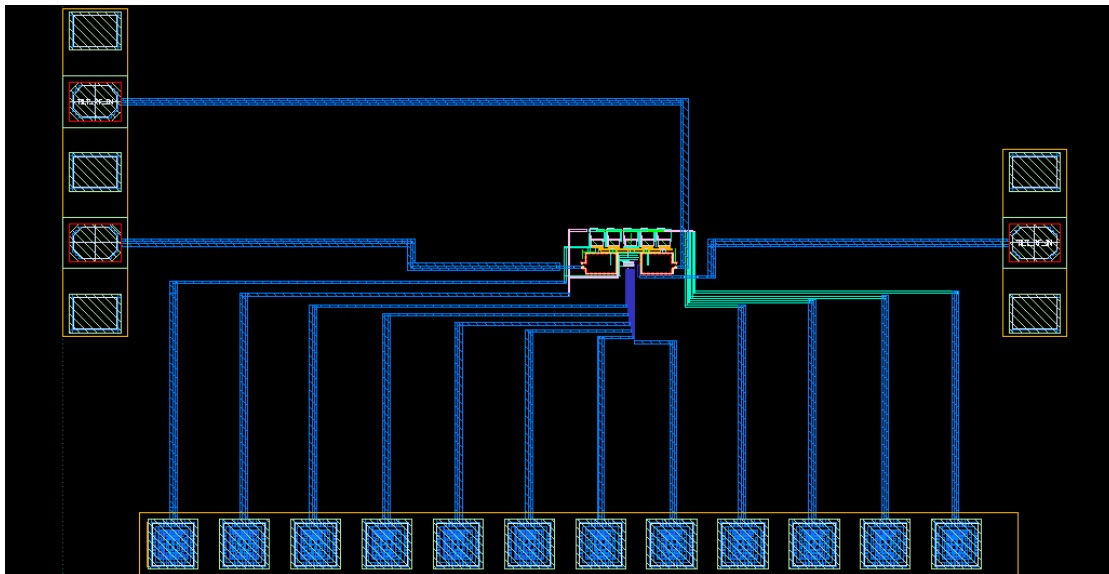


Figure 4.36: Layout of the sinusoidal signal generator with pads.

4.4.2 Post-layout simulation results

In order to validate the feasibility and performance of the designed sinusoidal signal generator, we performed electrical simulation of the extracted view. The simulation of the extracted view includes the effects of parasitic resistors and capacitors, introduced by the layout.

The extracted view was simulated in the same conditions as the previous simulations ($f_{clk} = 2$ GHz and bias voltages set as table 4.7). The spectrum of the generated output is shown in Fig. 4.37. As it can be seen, there is a clear degradation of the linearity of the generated signal. This degradation is explained by deviations of the currents in the current-steering branches due to layout parasitics, and it can be greatly mitigated by tuning the bias voltages of the current steering branches to recover the appropriate current ratios defined by the harmonic cancellation strategy ($\alpha_1 = \frac{I_2}{I_3} = \frac{I_4}{I_3} = \frac{\sqrt{3}}{2}$ and $\alpha_2 = \frac{I_1}{I_3} = \frac{I_5}{I_3} = \frac{1}{2}$).

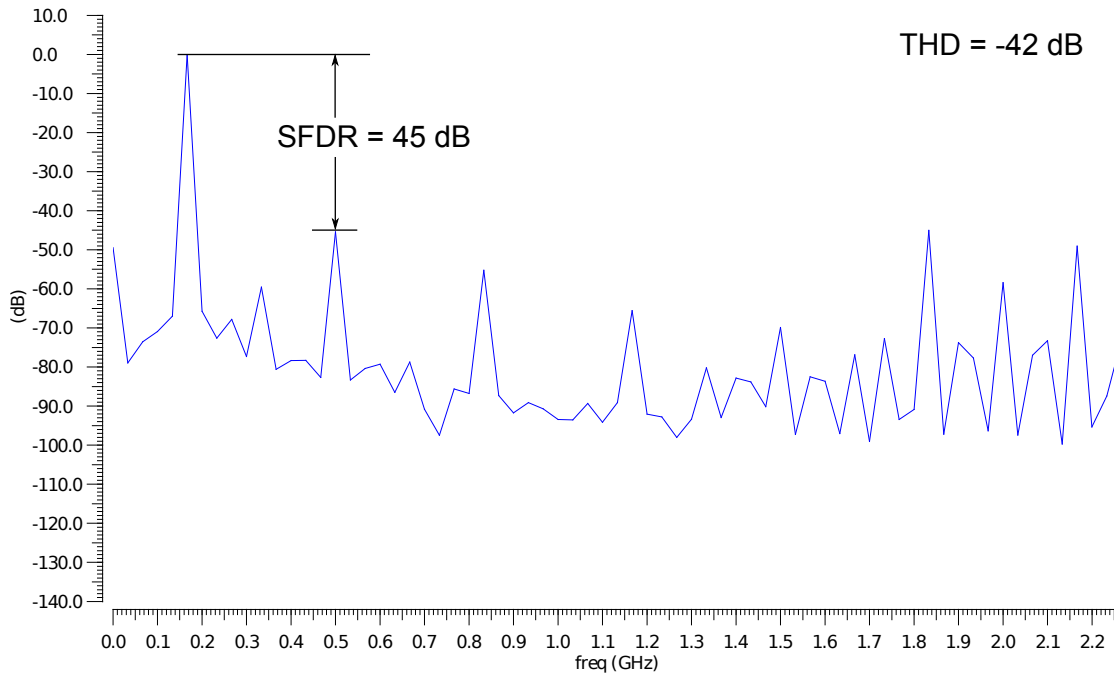


Figure 4.37: Spectrum of the output sinusoidal signal resulted from post-layout simulation.

The calibration algorithm was presented previously in 4.1. However, since the bias capacitors were removed from the final implementation, we adapted the calibration algorithm to this implementation by tuning the bias voltages of the current sources and measuring the output currents in the calibration mode. Table. 4.8 summarizes the bias voltages before and after calibration. The spectrum of the

sinusoidal signal provided by the calibrated generator is depicted in Fig. 4.38. This spectrum shows the effect of the calibration where all odd order harmonics are below -70 dBc, with an attenuation of -20 dB compared to the uncalibrated generator. However the linearity of the outputs is still limited by the second order harmonic component that comes from an imbalance between the differential signal paths due to parasitic elements and can not be calibrated by tuning the bias currents.

Table 4.8: Bias voltages of calibrated current sources.

	I_{out1}	I_{out2}	I_{out3}	I_{out4}	I_{out5}
	$100\mu A$	$173.34\mu A$	$200\mu A$	$173.34\mu A$	$100\mu A$
	V_{bias1}	V_{bias2}	V_{bias3}^*	V_{bias4}	V_{bias5}
Before calibration	$593mV$	$567mV$	—	$567mV$	$593mV$
After calibration	$600mV$	$568.4mV$	-	$562.4mV$	$587.4mV$

* V_{bias3} is implemented on-chip within a voltage divider.

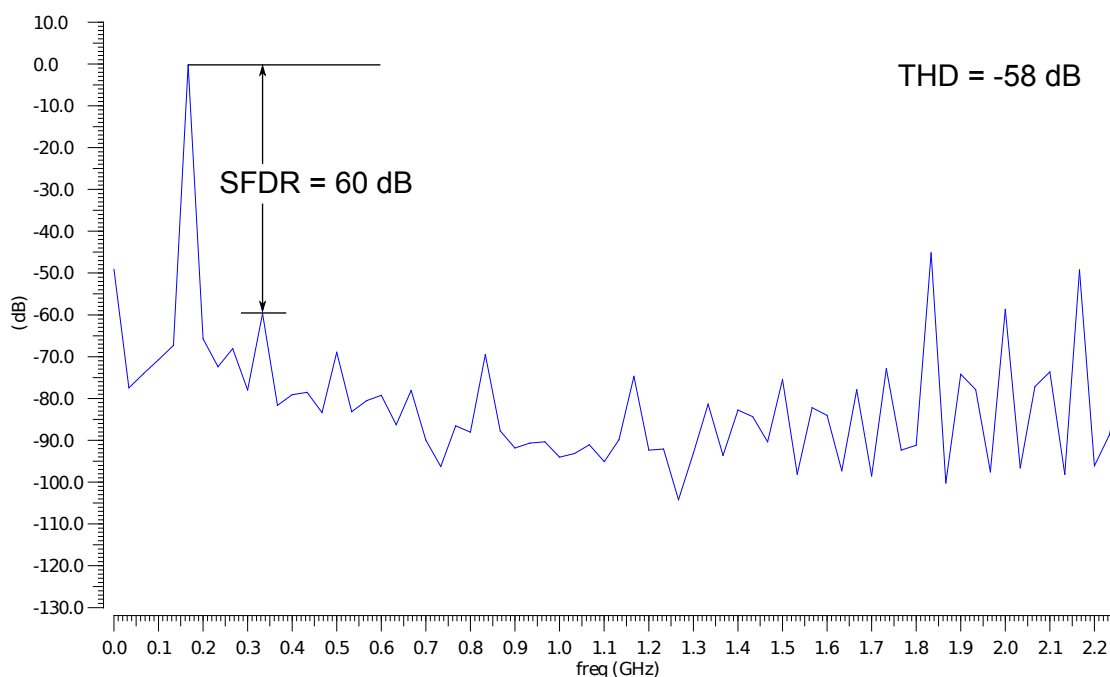


Figure 4.38: Spectrum of the output sinusoidal signal obtained from post-layout simulation after calibration.

Chapter 5

Experimental results

5.1 Introduction

The proof-of-concept prototype of the sinusoidal signal generator was fabricated and characterized in the laboratory for validating the feasibility of our proposal. In this chapter, we detail the test setup, the measurement procedure and the obtained experimental results.

5.2 Prototype fabrication

The proposed sinusoidal signal generator was fabricated in STMicroelectronics 8-metal 28 nm FDSOI technology. The characterization of the fabricated prototype was carried out in Algeco lab in STMicroelectronics-Crolles. The prototype was designed for wafer-level tests using micro-probes. Figure 5.1 shows the micro-photograph of the prototype. The circuit includes 15 pads, as schematically shown in Fig. 5.2, in order to interface with the external equipment aimed at providing the appropriate clock signal, bias voltages and digital configuration signals to the circuit under test and to properly receive the outputs of the sinusoidal signal generator to be evaluated. The different pads are listed and described in table 5.1.

5.3 Test setup

The main purpose of the experimental validation of the implemented sinusoidal signal generator is to validate the proposed harmonic cancellation strategy by evaluating the linearity of the generated sinusoidal signal in terms of its THD and SFDR. The circuit is connected to the micro-probes as show in Fig. 5.3.

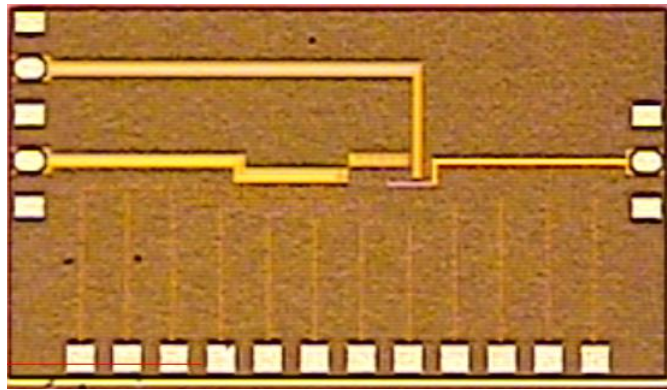


Figure 5.1: Micro-photograph of the sinusoidal signal generator.

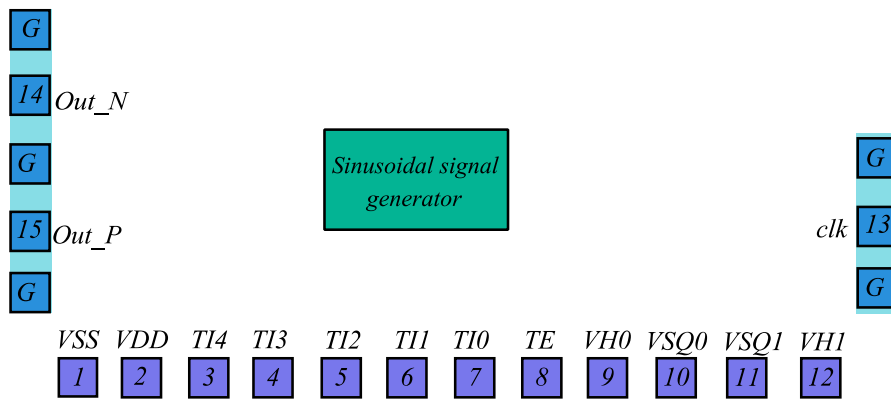


Figure 5.2: Pads diagram of the prototype.

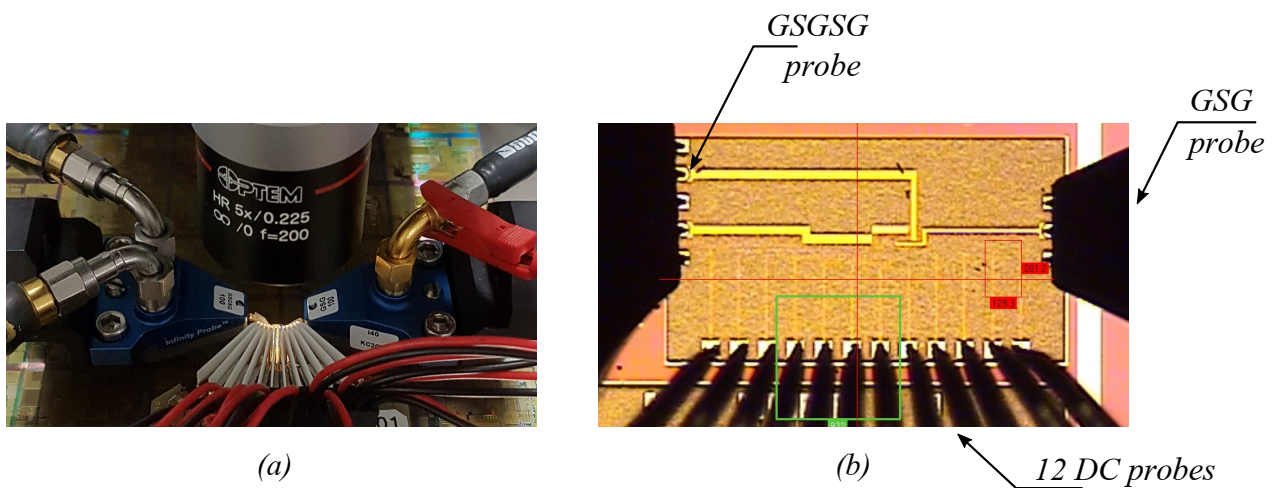


Figure 5.3: Probes photo: (a) probes connection; (b) micro-photograph.

Table 5.1: Pads table.

N°	Name	Type	Description
1	VSS	DC	Ground 0V
2	VDD	DC	Supply voltage 1V
3	TI4	DC	Configuration input signals of the digital shift-register
4	TI3	DC	
5	TI2	DC	
6	TI1	DC	
7	TI0	DC	
8	TE	DC	Digital pulse to switch between generation mode and calibration mode.
9	VH0	DC	Bias voltages of the current sources
10	VSQ0	DC	
11	VH1	DC	
12	VSQ1	DC	
13	Clk	GSG	Sinusoidal signal used as clock signal
14	Out_N	GSGSG	Differential outputs of the sinusoidal signal generator
15	Out_P		

The block diagram of the validation setup is depicted in Fig. 5.4 where a high frequency signal generator is required to drive the 2 GHz clock signal, a set of pulse generators to configure the square wave sequence in the digital shift-register and to be used to control each current source separately when the calibration mode is activated.

The DC voltage generators are used to provide the different bias voltages of the current sources. They will be set initially as the voltages obtained by simulations and they will be tuned in the calibration mode in order to regulate the current ratios of the current sources to be close enough to the nominal ratios defined by the harmonic cancellation technique. It has to be noted that the resolution of the calibration depends strongly of the resolution of the DC generators. In our experimental setup DC voltage generators are limited to a resolution of 1 mV.

The setup includes also signal acquisition instruments such as an oscilloscope to display the generated sinusoidal signal and a spectrum analyzer to compute its spectrum.

The RF cables used to connect the output of the circuit to the oscilloscope and to the spectrum analyzer are selected with equal lengths to avoid introducing additional phase-shift between the differential outputs.

A high resolution amperemeter is used in the calibration mode of the generator to measure and calibrate the current sources of the generator.

Additional instruments are used in this setup such as a hybrid coupler to combine the differential signals in the input of the spectrum analyzer, DC block modules to block the DC component of the signal and a level shifter in the output of the clock generator to generate a 0.5 V offset voltage to the clock signal. The equipment used in this setup is listed in table 5.2 and some pictures of the test setup are shown in Fig. 5.5.

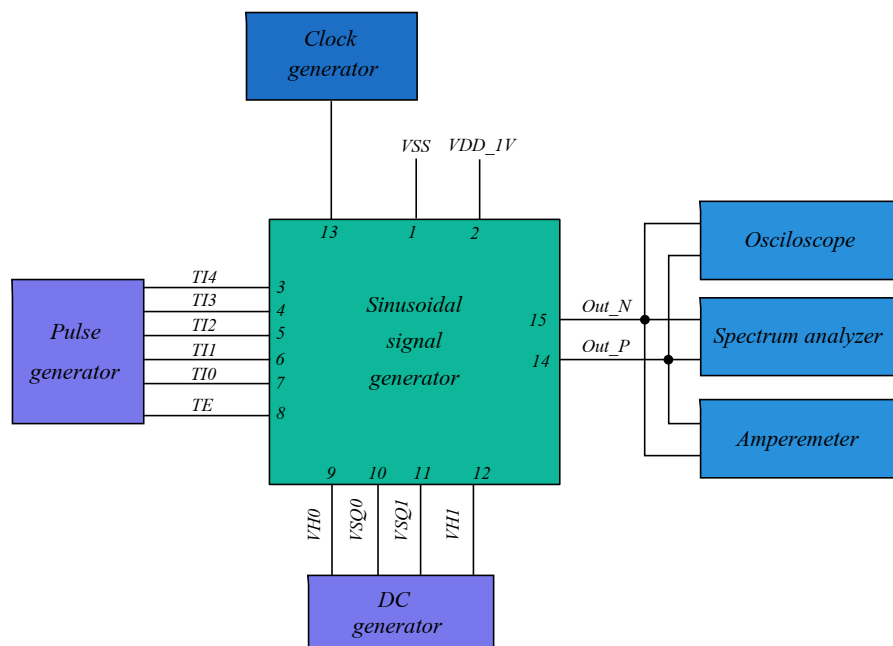


Figure 5.4: Block diagram of the experimental setup.

5.4 Test procedure

The functional test starts by setting the values of all bias voltages as in table 4.7 in chapter 4, obtained by simulations to provide currents with the nominal ratios defined by harmonic cancellations. The clock signal frequency is set to 2 GHz. The load of the initial square-wave in the circular shift register is made by the means of the pulse T_e when all T_i signal are set to 0V.

The generated output can be first acquired by the oscilloscope to verify visually the functionality of the circuit. The output is then connected to the amperemeter to measure the current delivered by each current source separately and calculate the current ratios between the different current branches. Then the calibration process will be performed as it was described in algorithm 4.1 in chapter 4. Once

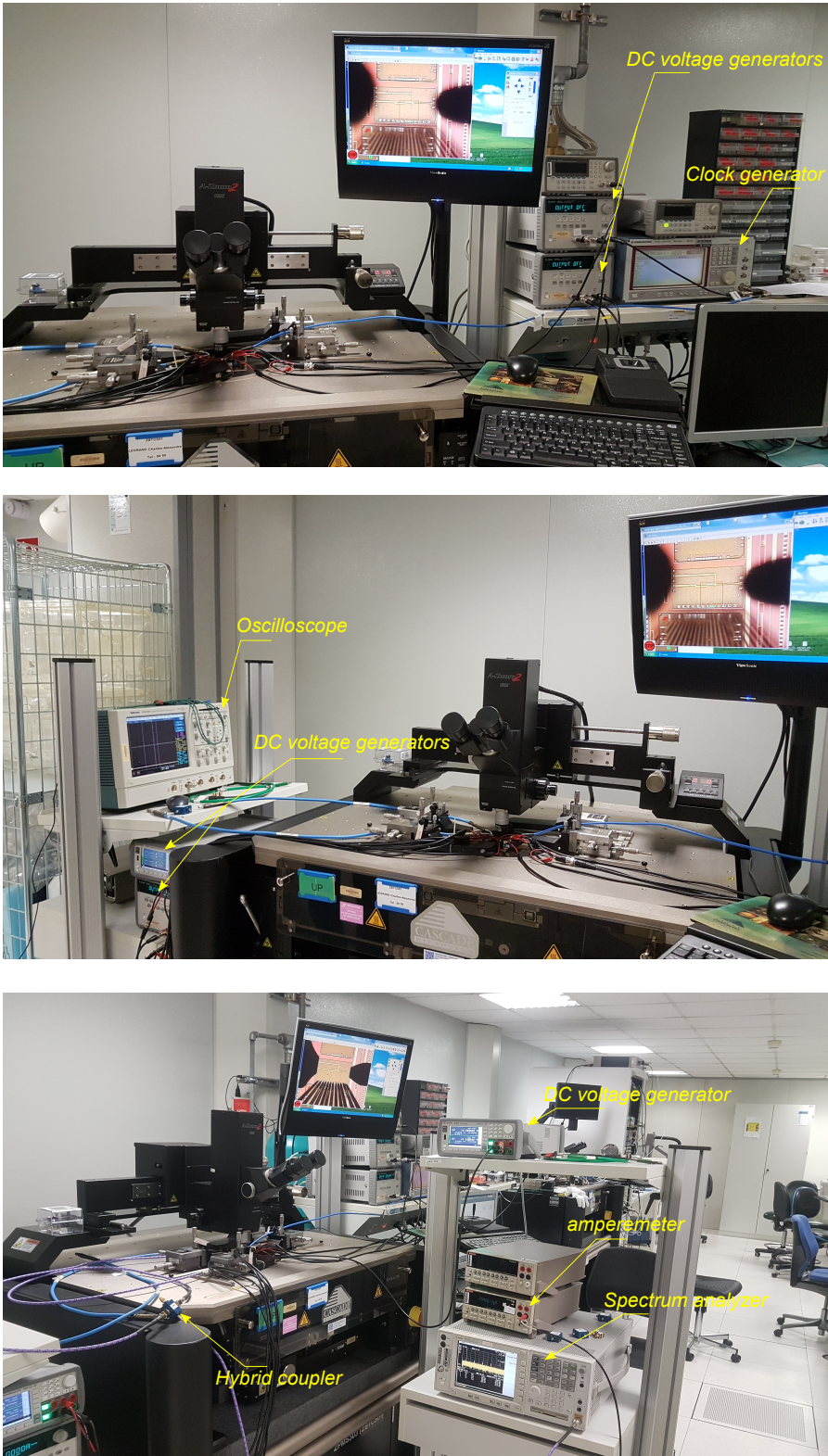


Figure 5.5: Setup photos.

Table 5.2: List of equipment.

Function	Manufacturer	Model	s/n
Prober	Cascade Microtech	CADCADE S300	615640506
Infinity probe 40Ghz	Cascade Microtech	I40 – GSG-100	KC2GV
Infinity probe 40Ghz	Cascade Microtech	I40-GSGSG-100	JT22W
WPH probe DC	Cascade Microtech	WPH-912-100	WPH-912-100 01
source x2 DC	Agilent	2962	MY52351064
source x2 DC	Agilent	2902	MY51143443
source x2 DC	Agilent	E3648A	MY53230017
source x2 DC	Agilent	E3631A	MY53120031 GAPWS34
source x2	Agilent	E3631A	MY51210020 GAPWS28
Pulse Generator	Agilent	33250	MY40009342 GAWFG09
Oscilloscope	Tektronix	TDS5054B	B022935
Multimeter	Keithley	N4876A	0887895
Spectrum Analyser	Agilent	E4443A	MY44300352
Signal Generator	Rohde & Schwarz	SMT06	848134/001

the calibration process is finished, the generation mode is reactivated and the linearity of the generated signal is evaluated using the spectrum analyzer.

5.5 Experimental results

5.5.1 Oscilloscope aquisition

Figure 5.6 shows the differential sinusoidal signal generated by one of the fabricated sinusoidal signal generators for a clock frequency of 2 GHz (output signal frequency 166.67 MHz), as it was displayed on the oscilloscope. The amplitude of the output signal is 39 mVpp for a 50 Ω load.

5.5.2 Linearity measurements

The spectrum of the generated differential signal before calibration is depicted in Fig. 5.7. It shows that the power of the main component is equal to -29 dBm and the linearity of the sinusoidal signal is limited by the 3rd and the 5th-order harmonic components with a power equal to -70 dBm and -74 dBm, respectively, while even order harmonics are below the noise floor.

We measured the power of all harmonic components until the 10th-order harmonic, using the spectrum analyzer, as shown in Fig. 5.8. These measurement

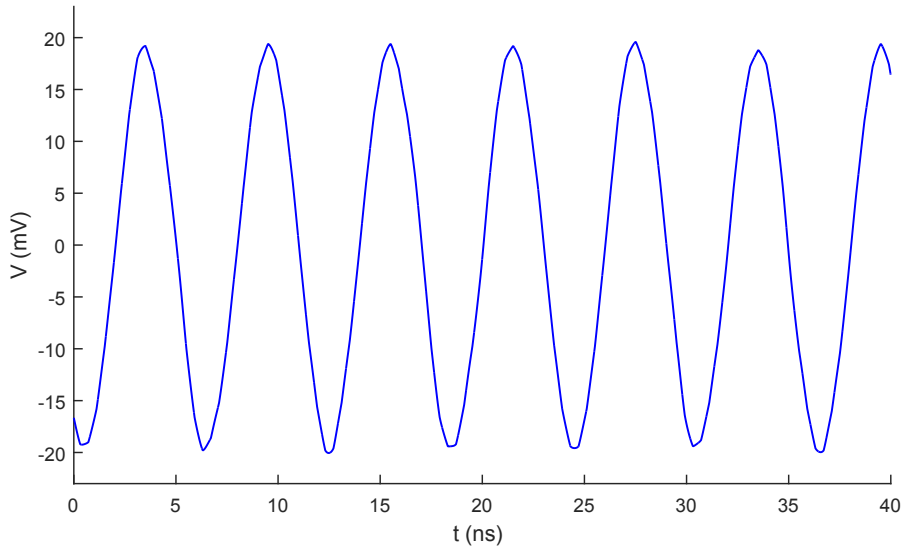


Figure 5.6: Oscilloscope acquisition of the generated sinusoidal signal.

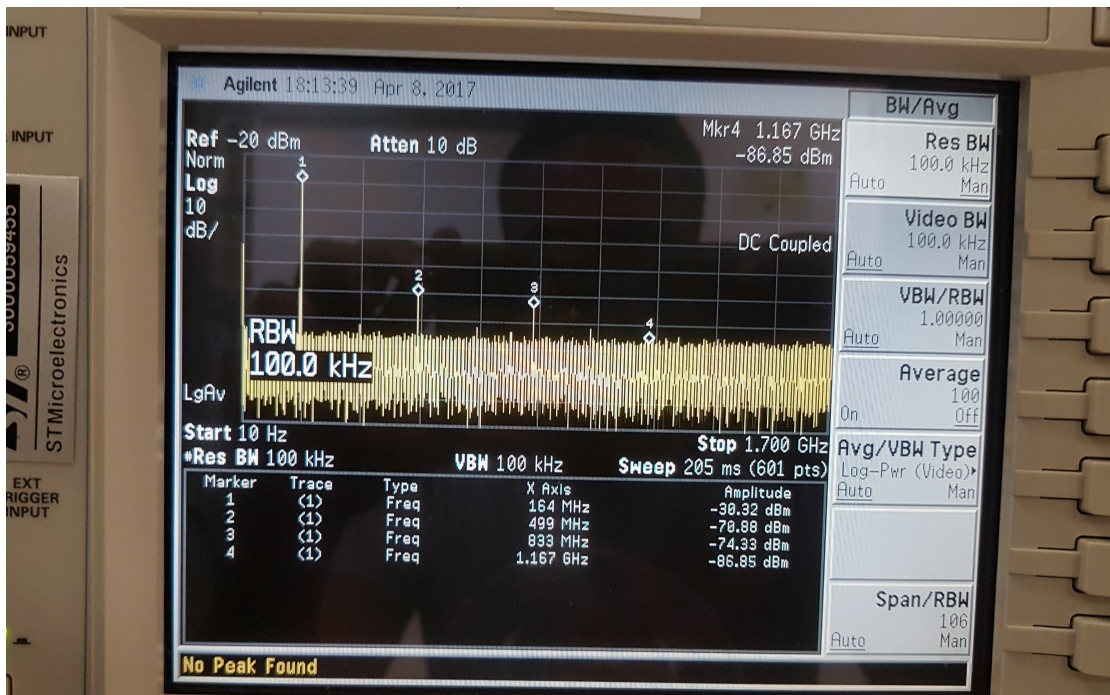


Figure 5.7: Photo of the spectrum of the generated sinusoidal signal before calibration at 166.67 MHz.

were used to calculate the THD and the SFDR of the output signal generated by the uncalibrated generator resulting in a THD of -38.9 dB and a SFDR of 41.5 dB.

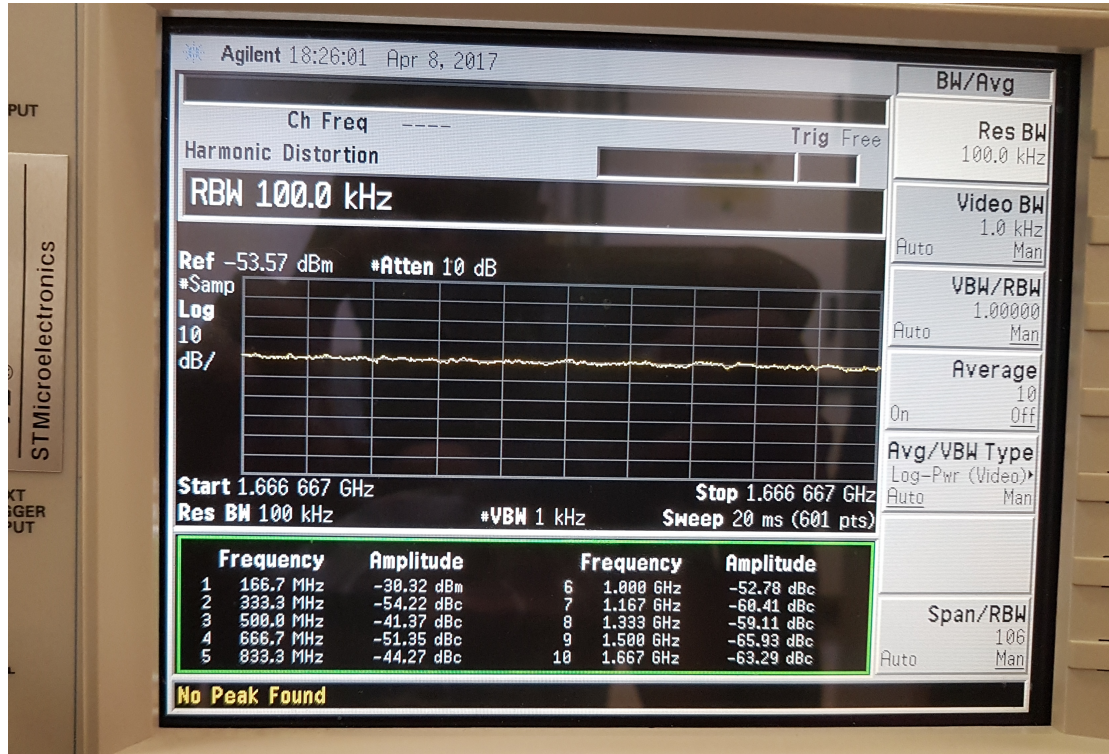


Figure 5.8: Photo of the power of the harmonic components of the circuit before calibration at 166 MHz.

As expected, the linearity of the uncalibrated generator is impacted by non-idealities. In order to calibrate the generator, the outputs of the generator under test were connected to the amperemeter and we computed the ratios between the current sources as described in algorithm 4.1. Table 5.3 shows the actual ratios between the current sources. The ratios were significantly deviated from the nominal ratios of harmonic cancellation with a maximum variation of 13.5%. In order to compensate these deviations, the currents provided by the different current sources were calibrated to produce ratios as close as possible to the nominal ratios of harmonic cancellation by tuning the bias voltages.

The new bias voltages are listed in table 5.3. The maximum variation of the new current ratios is 0.4%. The calibration step in this setup is limited by the resolution of the DC voltage generator. A second limitation of the calibration setup is that only one channel is connected to the amperemeter, and the second channel of the generator is on high impedance, which produces a difference between the

impedances seen in the output of each channel.

Table 5.3: Bias voltages, current ratios and current ratios variation percentage before and after calibration.

Before calibration	V_{bias}	V_{H0}	V_{SQ0}	V_{SQ1}	V_{H1}
		593mV	567mV	567mV	593mV
	Ratio	$\frac{I_{Out0}}{I_{Out3}}$	$\frac{I_{Out1}}{I_{Out3}}$	$\frac{I_{Out4}}{I_{Out3}}$	$\frac{I_{Out5}}{I_{Out3}}$
		0.49	0.79	0.75	0.45
Δ_{Ratio}	-2%	-8.8%	-13.5%	-10%	
After calibration	V_{bias}	V_{H0}	V_{SQ0}	V_{SQ1}	V_{H1}
		592mV	560mV	557mV	583mV
	Ratio	$\frac{I_{Out0}}{I_{Out3}}$	$\frac{I_{Out1}}{I_{Out3}}$	$\frac{I_{Out4}}{I_{Out3}}$	$\frac{I_{Out5}}{I_{Out3}}$
		0.502	0.867	0.868	0.499
Δ_{Ratio}	+0.4%	+0.03%	+0.15%	-0.2%	
Nominal ratios		$\frac{1}{2}$	$\frac{\sqrt{3}}{2}$	$\frac{\sqrt{3}}{2}$	$\frac{1}{2}$

The calibrated output signal spectrum displayed on the spectrum analyzer is shown in Fig. 5.9. The spectrum shows an improvement of the linearity of the generated signal where all odd harmonic components are attenuated and their power are very close to the noise floor of the spectrum analyzer which is approximately -93 dBm. The harmonic components above the 11th-order harmonic component are also attenuated by the low-pass filter and are below the noise floor.

The power of the first 10 harmonic components measured with the spectrum analyzer are displayed Fig. 5.10. The calibrated signal at 166.67 MHz has a THD of -46 dB and a SFDR equal to 52 dB, with an improvement of 10 dB regarding the uncalibrated generator. The linearity of the calibrated generator is limited by the even-order harmonic components, mainly the 4th and the 6th-order harmonics that can not be calibrated with the proposed strategy.

5.5.3 Experimental results at different operating frequencies

The output frequency of the generated signal can be easily programmed by modifying the clock frequency of the digital shift-register in the proposed generator. However, it has to be noted that the proposed proof-of-concept implementation has a fixed low-pass output filter with a cut-off frequency of 166.67 MHz. If the frequency has to be programmed, the cut-off frequency of the filter can be made also programmable. In our proof-of-concept, the fixed output filter means that the attenuation of the high order harmonic components will be reduced for output frequencies lower than 166 MHz, while the fundamental component will be attenuated for output frequencies above 166 MHz.

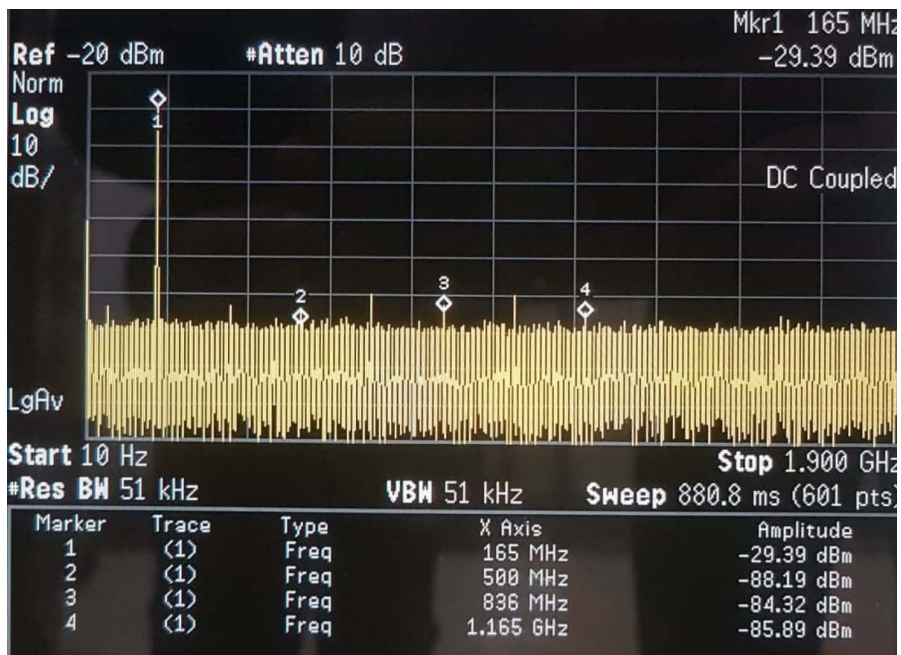


Figure 5.9: Photo of the spectrum of the calibrated generator at 166.67 MHz.

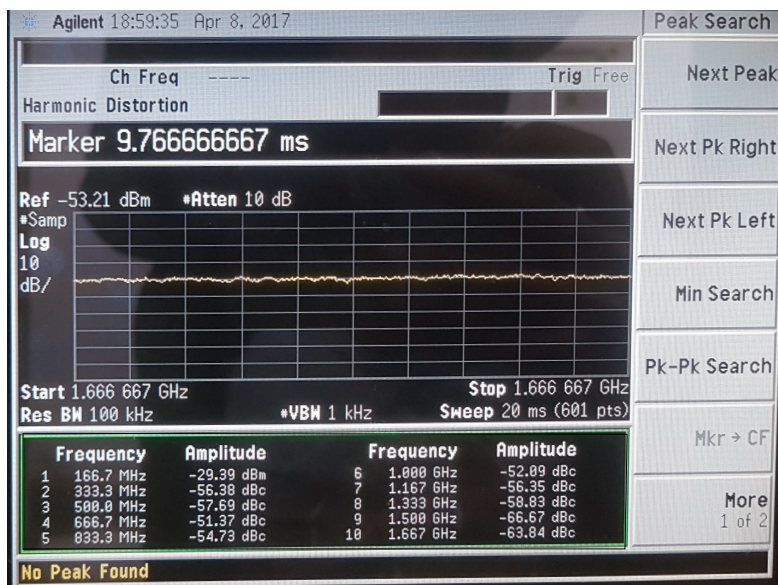


Figure 5.10: Power of the harmonic components of the calibrated circuit at 166.67 MHz.

Taking these unavoidable limitations into account, we repeated the test and calibration procedure at different clock frequencies from 20 MHz to 4 GHz to generate sinusoidal signals from 1 MHz to 333 MHz. Figure 5.11 and Fig. 5.12 show the spectra of the generated sinusoidal signals obtained for different frequencies.

5.5.4 Results discussion

For frequencies lower than 5 MHz, Fig. 5.11.a and Fig. 5.11b, we notice an attenuation of the main tone compared to the 166 MHz generator. This is due to the hybrid coupler, used in the input of the spectrum analyzer to provide the difference between the differential outputs of the generator, which has an operation band of 5 MHz-500 MHz. The fundamental tone of the generated signals is also attenuated for higher frequencies because of the filter. Figure 5.13 show the variation of the fundamental tone power as function of the output frequency.

At it was expected for low frequencies, we can notice also the presence of the 11th-order harmonic component. This harmonic component is not cancellable with the implemented harmonic cancellation strategy, and it is not attenuated by the low-pass filter because it lies in the pass-band frequency of the filter.

Figure A.35.a and Fig. A.35.b show the SFDR and THD after calibration, respectively, as function of the generated output frequency. It can be noticed that, even with the expected degradation previously mentioned, the obtained linearity figures show a fairly constant behavior across the considered frequency range, with an average SFDR of 49 dB and an average THD of -45 dB.

In order to get further insight into the linearity of the fabricated prototype, Fig. 5.15 shows a boxplot diagram of the measured power for the first ten harmonic distortion components of the generated sinusoidal signal, across the considered frequency range. It is clear that harmonic distortion components are centered around -50 dBc with respect to the fundamental, barely above the noise floor of the spectrum analyzer. It is also clear that dispersion of the seventh order harmonic component is larger than the dispersion of other components. This is a consequence of the limited resolution of the DC sources used for calibration, that do not allow us to cancel the seventh harmonic component completely.

Additional insight into the distortion mechanisms limiting the performance of the generator can be gain by analyzing the partial THD and SFDR computed alternatively with the even and odd harmonic components. Thus, in Fig.5.16.a we show the measured SFDR across the considered frequency range, together with the partial SFDR due to even components, $\text{SFDR}_{\text{even}}$, and the partial SFDR due to odd harmonic components, SFDR_{odd} .

Equivalently, Fig. 5.16.b shows the THD across the considered frequency range, together with the partial figures THD_{even} and THD_{odd} . It is clear to see that for low frequencies, below ~ 150 MHz, the observed linearity is mainly limited by

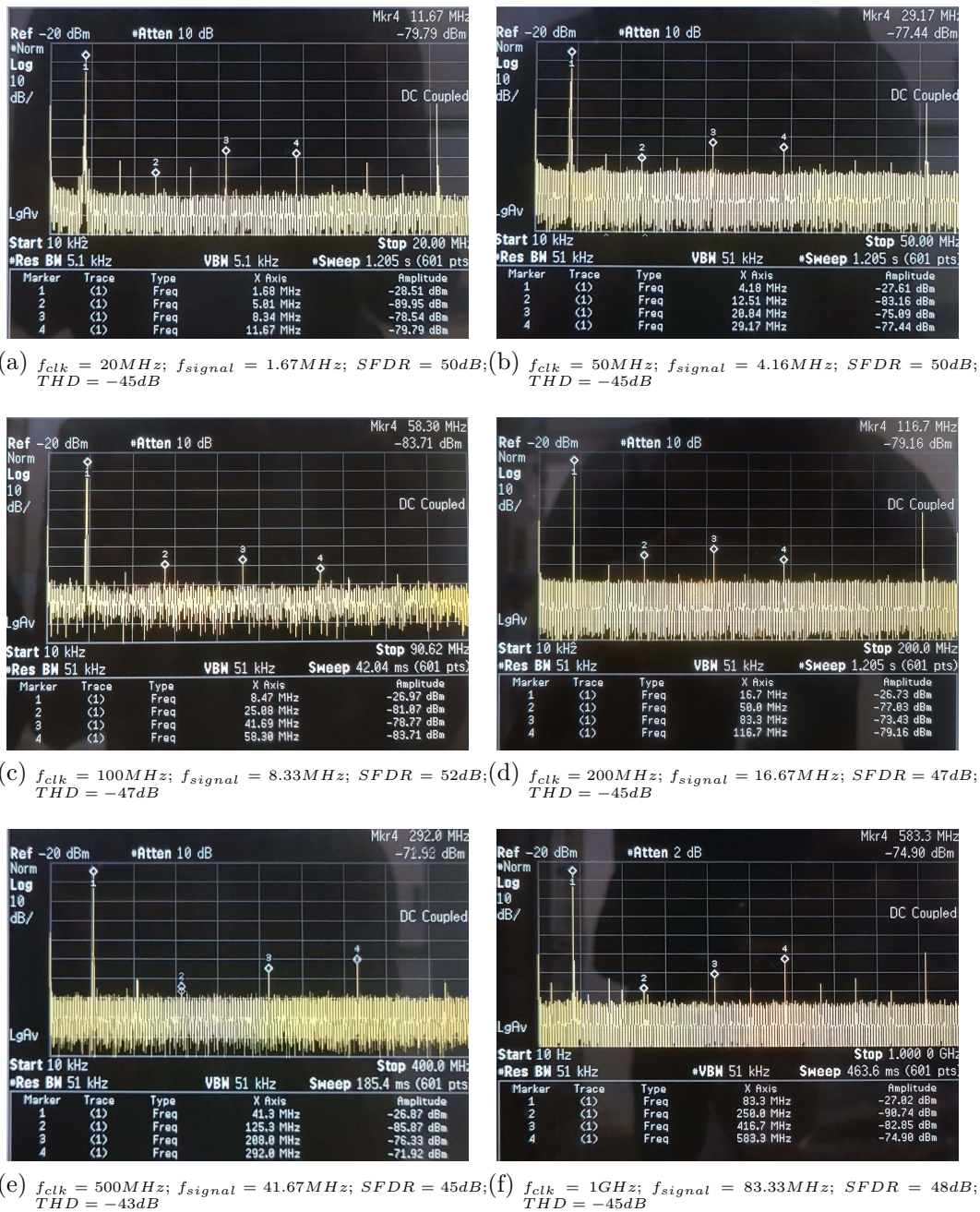


Figure 5.11: Spectra of the generated signals in different frequencies: from 1 MHz to 80 MHz.

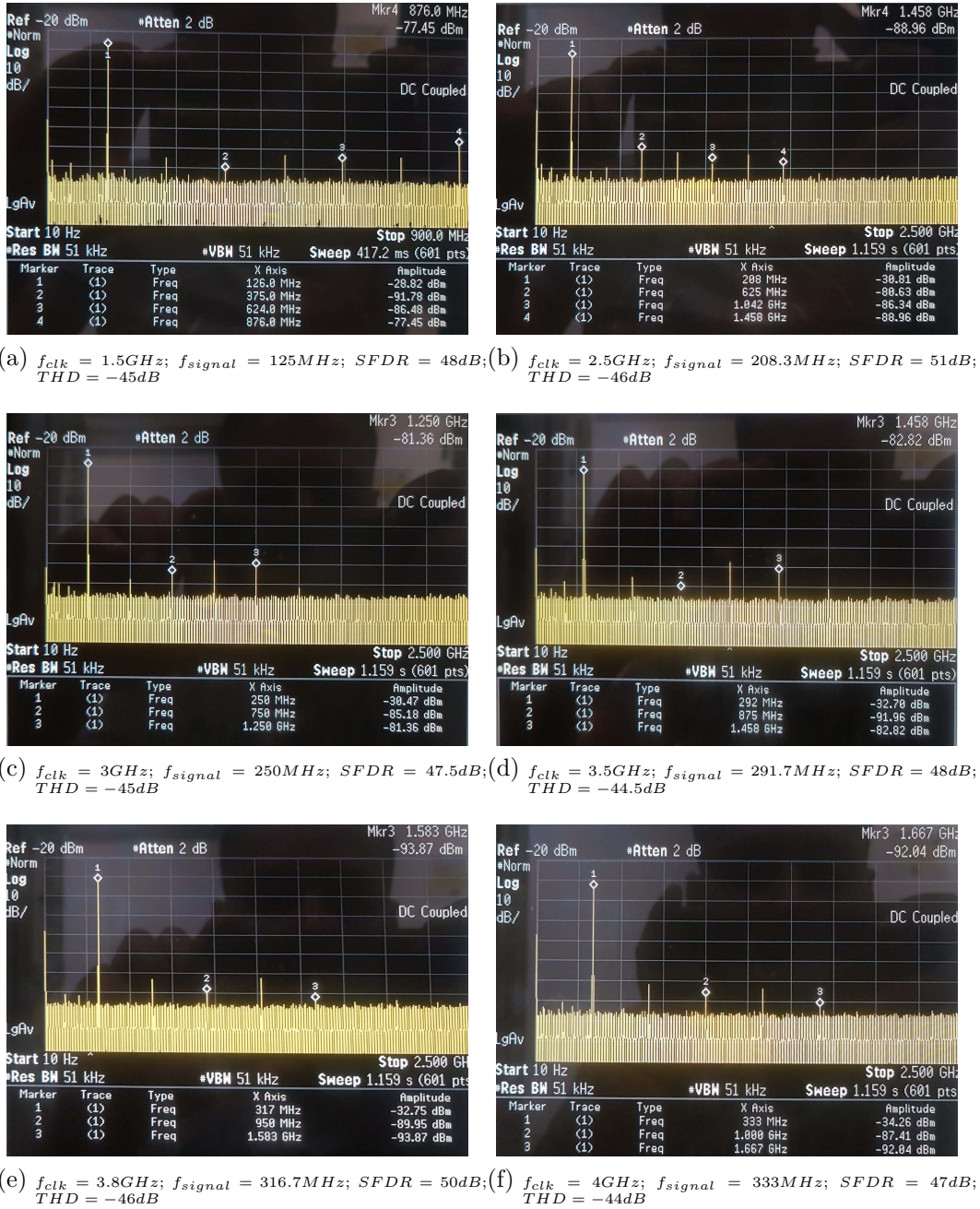


Figure 5.12: Spectra of the generated signals in different frequencies: from 125 MHz to 333 MHz.

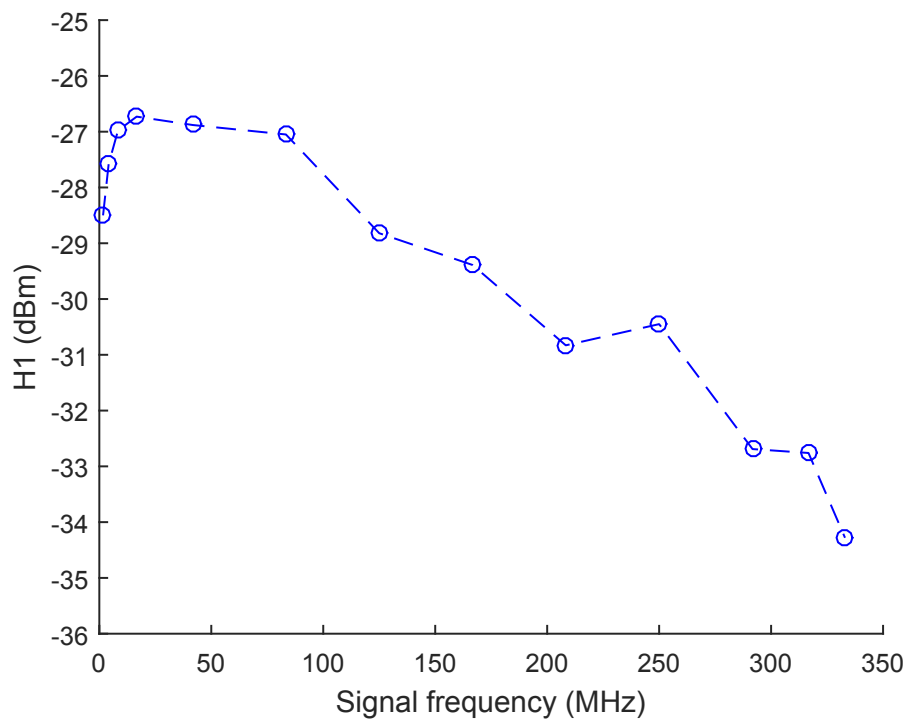
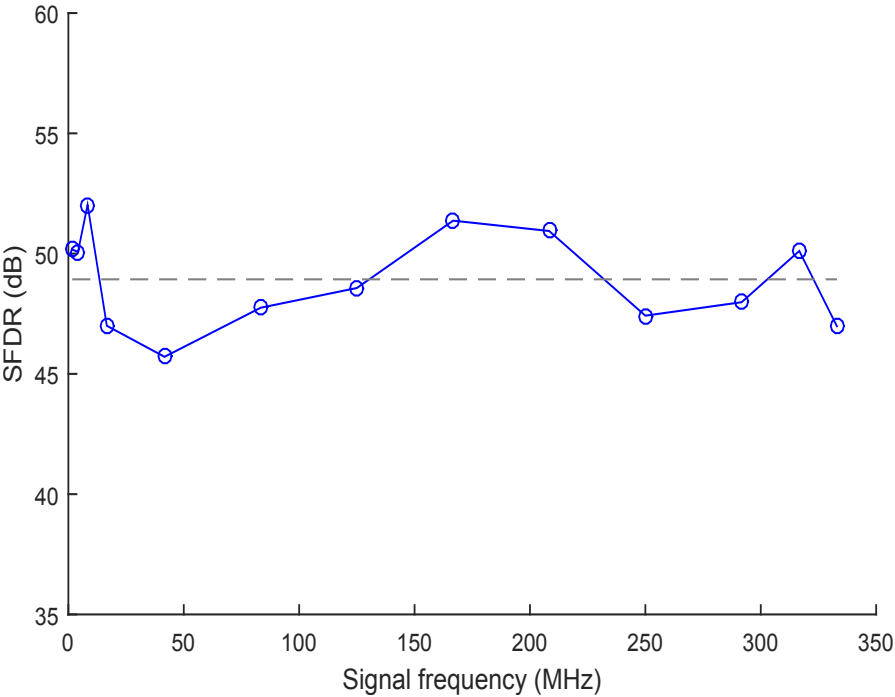
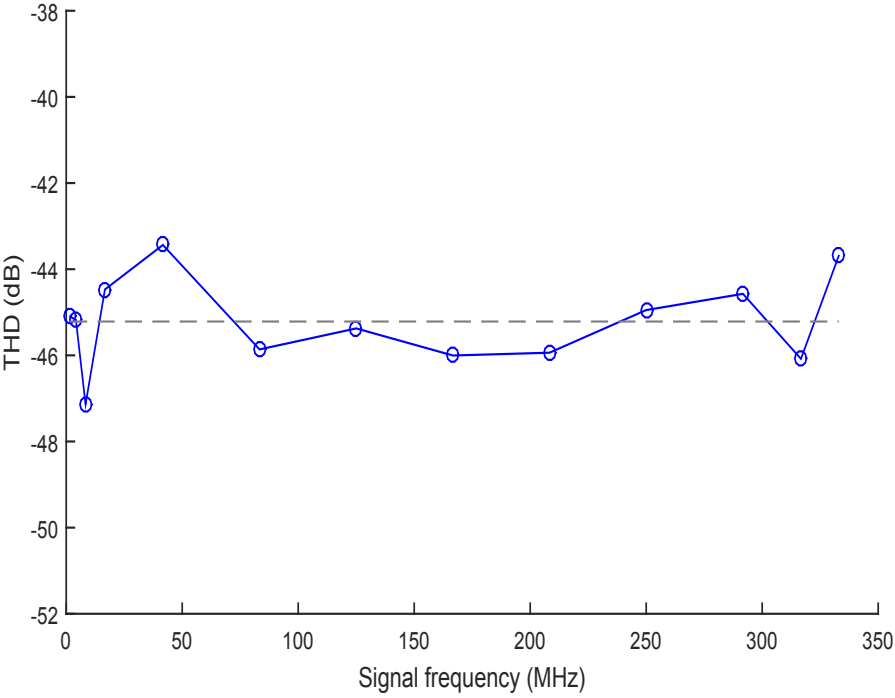


Figure 5.13: Variation of the fundamental tone power Vs signal frequency.

the odd harmonic components due to incomplete harmonic cancellation because of the limited resolution of the DC sources. For higher output frequencies, timing errors due to circuit imbalances and to non-idealities of the external clock lead to degradation of the 50% duty-cycle of the digital square-waves and may affect also the balance between the differential outputs, both effects leading to even-order harmonic distortion.



(a)



(b)

Figure 5.14: (a) SFDR; (b) THD; variation Vs frequency.

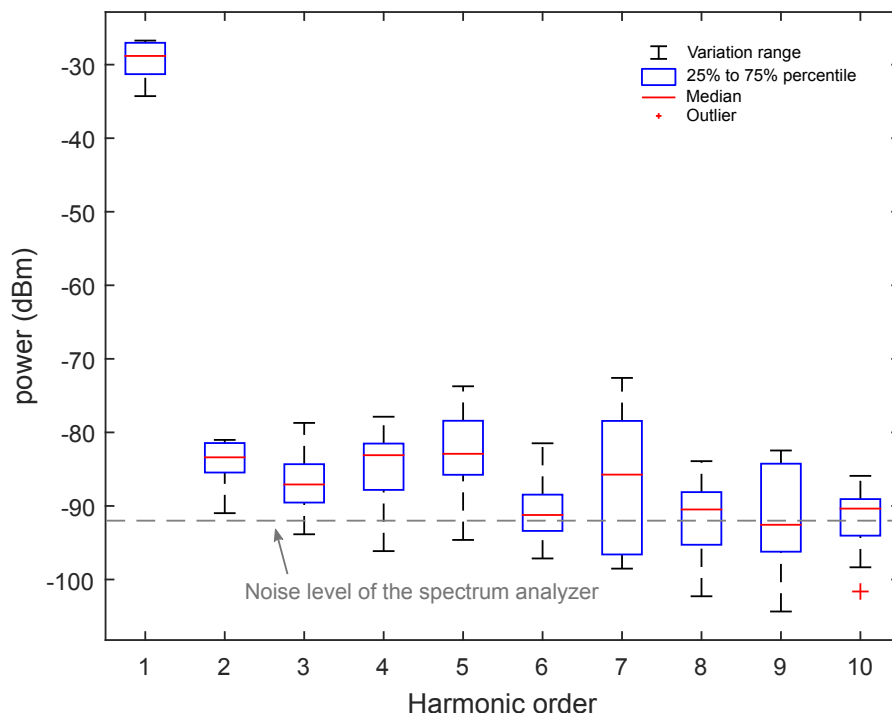
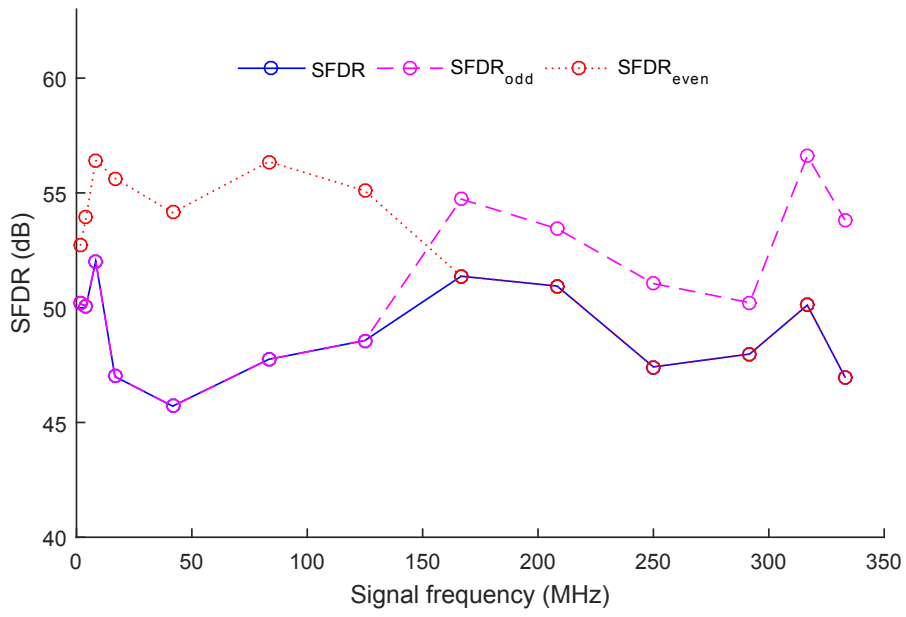
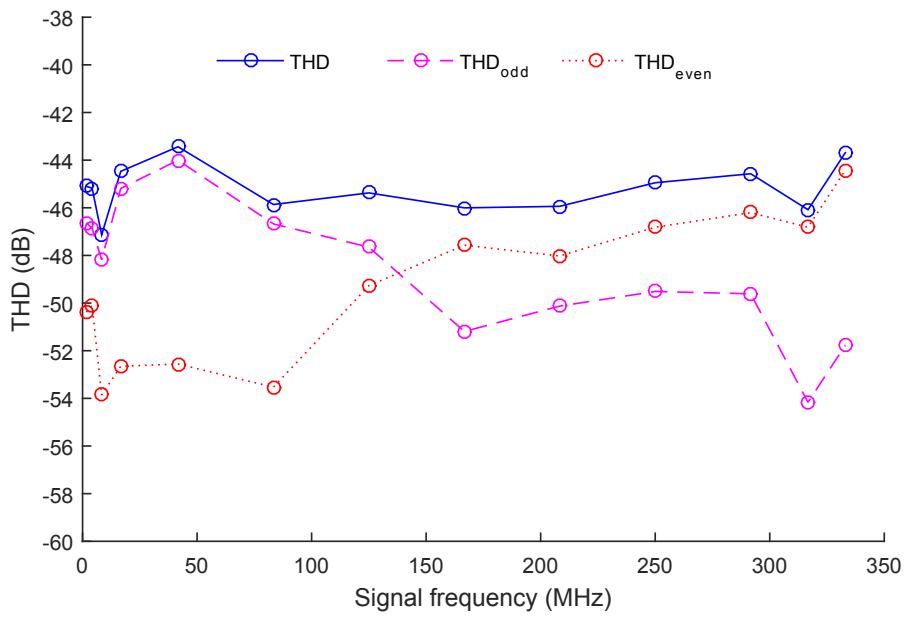


Figure 5.15: Variation of harmonic power.



(a)



(b)

Figure 5.16: Impact of odd- and even-order harmonics on the: (a) SFDR; (b) THD.

Chapter 6

Conclusions and future works

This thesis project was carried out through the NANO2017 program with the collaboration of STMicroelectronics. The main goal of this thesis is to develop novel architectures for embedded highly-linear sinusoidal signal generators for mixed signal BIST applications. In this chapter, we summarize the main conclusions that we can extract from our work and the directions of our future researches on this topic.

6.1 Thesis contributions

A. We presented a comparison between two advanced spectral manipulation techniques, namely harmonic cancellation and distortion shaping, applied to a family of efficient sinusoidal generators intended for BIST applications. The practical implementation of both techniques has been discussed, and behavioral models have been used to explore the performance limitations and design trade-offs of the considered generator with and without applying the spectral manipulation techniques. Obtained simulation results in chapter 2 clearly show a trade-off between the choice of harmonic cancellation or distortion shaping techniques, and the simplicity of the design. The use of harmonic cancellation techniques can improve the linearity of the basic generator without increasing the complexity of the design. However, the application of distortion shaping requires a greater complexity to get similar performance.

B. We have explored also four different harmonic cancellation strategies that may lead to the design of efficient and robust sinusoidal signal generators based on mostly-digital resources. The proposed harmonic cancellation solutions simplify the design of the different scale weight factors in the generator that are usually a key limiting factor for the effectiveness of the harmonic cancellation. These

harmonic cancellation techniques employ integer and unitary scale weight ratios, instead of the irrational scale weight ratios proposed by previous implementations, which may facilitate and improve matching in practical on-chip implementations. The trade-off between performance and implementation simplicity has been explored based on behavioral statistical simulations.

C. We have proposed a complete transistor-level architecture for a generator employing a harmonic cancellation technique with irrational scale weight. The generator is based on a circular shift register that provides a set of time-delayed square-waves together with a simplified current steering DAC. A simple calibration strategy has been proposed for assuring the effectiveness of the harmonic cancellation. Electrical simulation results under process and mismatch variations show a linearity of the generated stimulus better than $\text{THD} = -67$ dB and $\text{SFDR} = 70$ dB, however the post layout simulation show a THD of -58 dB and a SFDR of 60 dB at 166 MHz.

D. We have fabricated a proof-of-concept prototype in STMicroelectronics 28 nm FDSOI technology. This prototype has been characterized in the lab and results show that the sinusoidal signal generated by the calibrated generator presents a THD of -45 dB and a SFDR of 52 dB at 166.67 MHz, with an improvement of 10 dB compared to the uncalibrated generator. Experiment results show also that the calibrated generator presents fairly constant performances in an operating frequency range from 1 MHz to 333 MHz, with a clock frequency between 20 MHz and 4 GHz. The obtained average of THD is around -45 dB and the average of the SFDR is around 50 dB.

6.2 Future works

Further work in this line include three main research paths:

A. The improvement of the practical realization of the proposed sinusoidal signal generator at the design level for a quantitative exploration of the performance limits of this family of generators.

B. The practical realization of the different harmonic cancellation techniques proposed in this manuscript with integer and unitary scale ratios, as described in chapter 3, in a transistor level implementations and their experimental characterization in the laboratory.

C. The integration of a complete BIST prototype including the generation of the test stimulus, analysis of the output response and external control, into a state-of-the-art ADC for further validation of the proposed generation technique.

Annexe A

Résumé en français

A.1 Introduction

A.1.1 Contexte

De nos jours, les circuits intégrés analogiques et mixtes (AMS) tel que les amplificateurs, les filtres, les convertisseurs analogique-numérique et les convertisseurs numérique-analogique, sont largement utilisés dans plusieurs domaines d'application comme la télécommunication, l'internet des objets, l'automobile, etc. Chaque circuit AMS est caractérisé par une liste de spécifications et de performances listés dans son datasheet. Le processus de fabrication des circuits intégrés, comme tout processus industriel, peut introduire des imperfections qui peuvent avoir un impact direct sur le comportement des circuits fabriqués. Pour cette raison, il est très important pour les industriels en semi-conducteur de tester chaque circuit fabriqué afin de vérifier que les circuits livrés au clients remplissent toutes les spécifications requises dans leurs datasheet.

Cependant, le processus de test de production des circuit AMS est très couteux. Ceci est due essentiellement à l'utilisation des équipements des test automatique (ATE) qui sont très chères. Ces testeurs contiennent des blocs de génération de stimuli pour exciter le circuit sous test (CUT), des dispositifs de mesure pour évaluer la réponse du circuit, des blocs de charge et d'alimentation, des circuits d'entré/sortie et des dispositifs d'interface pour connecter le CUT, comme présenté dans la figure A.1. L'ITRS (International Technology Roadmap for semiconductors) estime que le coût des ATE et des interfaces de test va continuer à augmenter pendant les prochaines années comme on peut voire sur la figure A.2.

De plus, les tests des circuits intégrés AMS sont des tests fonctionnelles, basés sur les spécifications de chaque circuit, ce qui nécessite un temps de test important. A titre d'exemple, le camembert dans la figure A.3 montre la distribution du temps

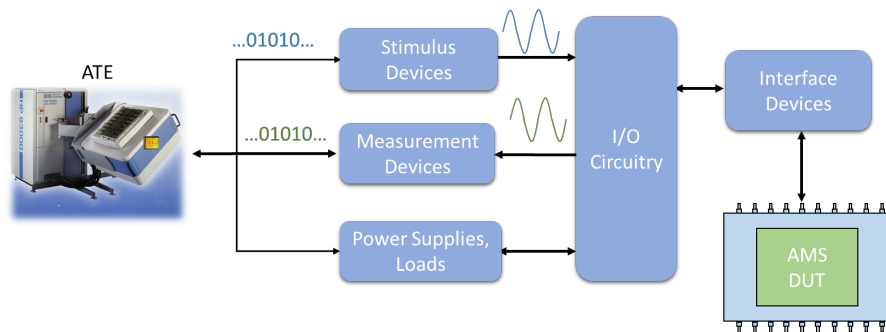


FIGURE A.1 : Diagramme de test avec des équipements de test externe.

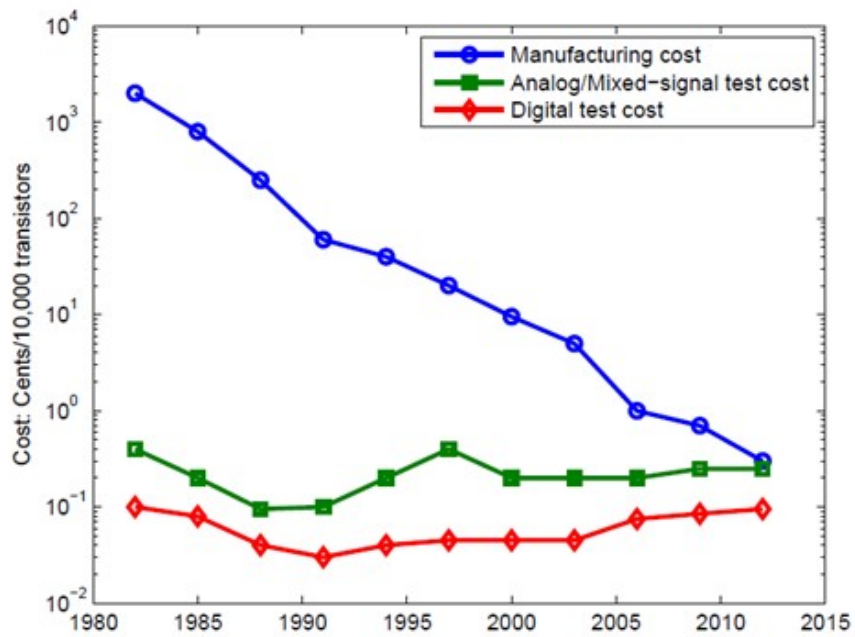


FIGURE A.2 : Estimation de l'évolution du coût des ATEs.

de test requit pour le test d'un SoC d'un téléphone mobile et c'est clair que les circuits AMS consomment 34% du temps de test global.

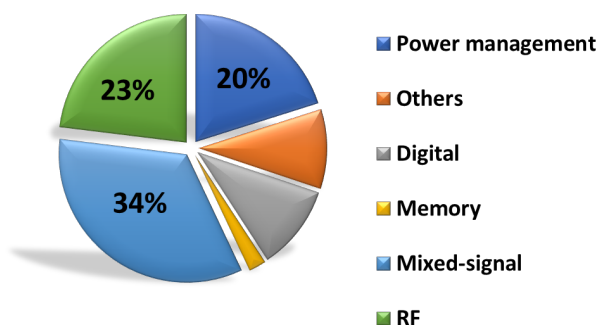


FIGURE A.3 : Distribution du temps de test dans un SoC (Infinion technology).

A.1.2 Auto-test intégré

L'auto-test intégré, dite aussi BIST (Built-In Self-Test) est apparu comme une solution pour réduire le coût de validation des circuits mixtes, énormément influencé par le coût des équipements de test utilisés. Le BIST consiste à intégrer quelques fonctionnalités des équipements de test dans le circuit sous test. Ceci permet de :

- Minimiser le temps de test : dans un BIST, la totalité des instruments de test est intégrée dans le circuit sous-test et les tests sont programmés ce qui réduit le temps nécessaire pour l'installation et la configuration des équipements de test externes.
- Améliorer l'auto-testabilité du circuit sous-test : un BIST complet permet au circuit testé d'évaluer ses propres performances.
- Réduire la complexité d'accès au circuit sous-test.

Un circuit de BIST complet, comme schématisé dans la figure A.4, contient un générateur de stimulus pour exciter le circuit sous-test, un instrument de mesure pour évaluer sa réponse, et un système de programmation et de contrôle de test.

A.1.3 Motivations

Le générateur de stimulus est un élément critique dans le BIST des circuits AMS tel que les amplificateurs, les filtres, les convertisseurs A/N, etc. Plusieurs formes

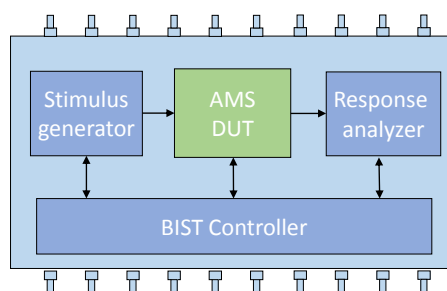


FIGURE A.4 : Schéma bloc d'un BIST.

de stimulus peuvent être appliqués suivant la nature de la performance à mesurer. Prenons par exemple le test d'un CAN : la mesure des performances statique de ce convertisseur (INL et DNL) nécessite en général l'utilisation d'une rampe ou d'un signal sinusoïdal de faible fréquence. Par contre, pour mesurer ses performances dynamiques (SNR, SFDR, SINAD), un signal sinusoïdal de haute linéarité est requis pour stimuler le CAN sous-test.

Dans cette thèse, nous présentons la conception d'un générateur de signal sinusoïdal de haute linéarité pour le BIST des circuits mixtes qui applique des techniques d'annulation d'harmonique.

A.2 État de l'art des générateur de signaux sinusoïdaux

L'état de l'art montre plusieurs types de générateur de signaux sinusoïdaux qui ont été développés pour produire des stimuli de haute linéarité. Ces générateurs peuvent être classés selon leurs architectures en deux grandes familles : les oscillateurs en boucle fermée et les générateurs en boucle ouverte. Indépendamment de leurs architectures, l'état de l'art montre aussi des techniques de manipulation des harmoniques qui ont été appliquées pour améliorer la linéarité des signaux sinusoïdaux générés, tout en réduisant la complexité de leur implémentation.

A.2.1 Oscillateurs en boucle fermée

L'oscillateur en boucle fermée (Astable), schématisé dans la figure A.5, consiste à un étage de filtrage avec un feedback non-linéaire.

Une implémentation pratique de ce type de générateur consiste généralement à utiliser un filtre passe-bande avec un comparateur en boucle de feedback. Différentes implémentations ont été présentées dans la littérature. Certaines utilisent

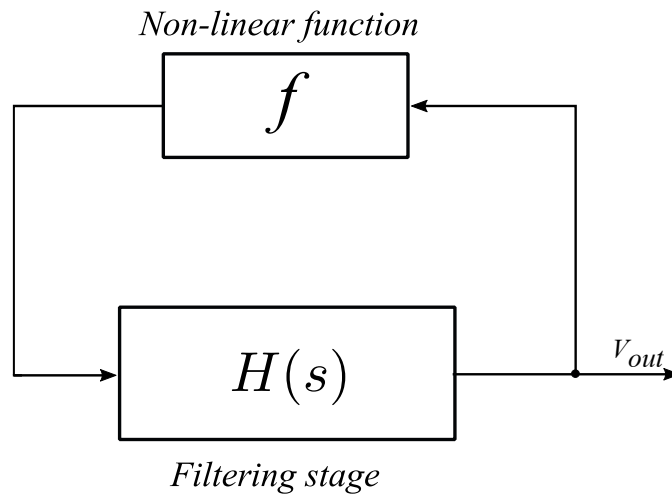


FIGURE A.5 : Oscillateur en boucle fermé.

des comparateurs à deux niveaux [11], tandis que d'autres utilisent des comparateurs à plusieurs niveaux [12, 14] dans la boucle de contre-réaction.

Cependant, un filtre passe-bande avec un facteur de qualité Q très élevé est toujours nécessaire pour rejeter toutes les harmoniques non-désirées, proche de la fondamentale. Cette famille d'oscillateur est également limitée par la surface de silicium principalement consommée par les condensateurs, ce qui augmente le facteur de coût.

A.2.2 Générateurs en boucle ouvertes

Les générateurs de signaux sinusoïdaux en boucle ouverte tirent généralement parti des techniques de traitement des signaux numériques pour la génération de signaux analogiques. La stratégie de génération de signal, illustrée de manière conceptuelle sur la figure A.6, contient généralement un générateur de vecteur numérique qui code un signal numérisé de haute résolution sinusoïdal, un convertisseur N/A permettant de traduire le signal dans le domaine analogique et un filtre sur la sortie pour rejeter toutes les composantes harmoniques indésirables.

En raison de l'entrée numérique des générateurs à boucle ouverte, plusieurs approches possibles ont été explorées afin de mettre en œuvre cette catégorie de générateurs. Une implémentation classique est basée sur les techniques DDFS (Direct Digital Frequency Synthesizer) [16, 17]. Le schéma conventionnel d'un générateur basé sur DDFS est illustré de manière conceptuelle à la figure A.7. Il consiste en un accumulateur de phase suivi d'une ROM, d'un convertisseur N/A et d'un filtre en sortie. L'accumulateur de phase sert de générateur de phase numérique, piloté par une horloge f_{clk} . L'entrée de l'accumulateur de phase est un m -bits FCW (Mot de

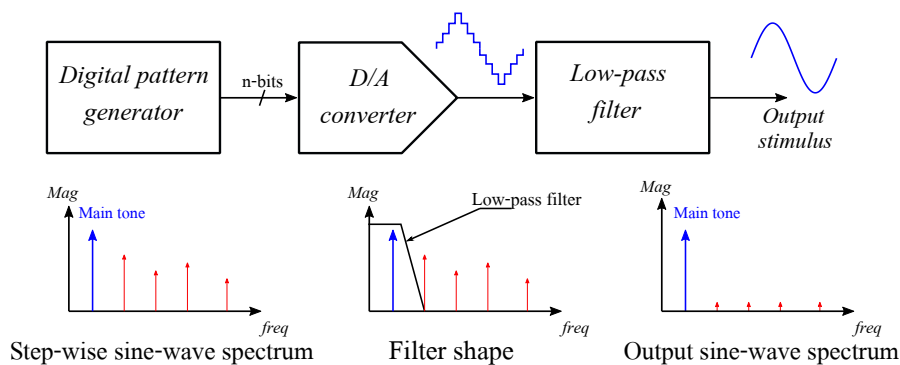


FIGURE A.6 : Générateur en boucle ouverte.

contrôle de fréquence) qui détermine la périodicité de l'accumulateur de phase. La sortie de l'accumulateur de phase est une forme d'onde en dents de scie qui représente le changement de phase. La ROM, adressée par la sortie de l'accumulateur de phase, contient les coefficients d'amplitude numériques correspondant aux valeurs de phase d'un seul cycle d'une onde sinusoïdale échantillonnée. Les échantillons numériques fournis par la ROM sont ensuite convertis dans le domaine analogique en utilisant un convertisseur N/A pour générer une forme d'onde sinusoïdale analogique pas à pas qui sera filtrée à l'aide d'un filtre passe-bas afin de produire une onde sinusoïdale linéaire en atténuant les harmoniques indésirables.

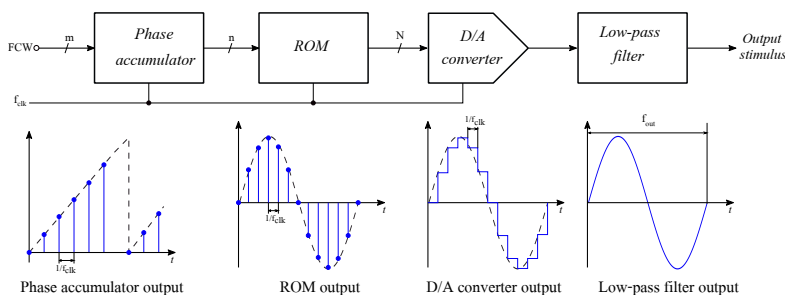


FIGURE A.7 : Générateur basé sur la technique de DDFS.

L'architecture du générateur $\Sigma\Delta$, est dérivé du générateur à base de DDFS et il se concentre sur la réduction de la complexité du convertisseur N/A. La stratégie de génération repose sur la mise en forme du bruit des caractéristiques de la technique de codage $\Sigma\Delta$. Il consiste à générer une version codée $\Sigma\Delta$ à 1 bit d'un signal numérique à N bits qui sera convertie dans le domaine analogique à l'aide d'un convertisseur N/A à 1 bit. Un filtre passe-bas analogique est utilisé en sortie afin de reconstituer le signal sinusoïdal. La forme du filtre de sortie doit correspondre à la mise en forme du bruit du train de bits $\Sigma\Delta$ afin d'atténuer le bruit de quantification mis en forme et de conserver uniquement le ton fondamental

dans la fréquence de la sortie [30, 31].

Les générateurs basés sur les capacités commutés (SC) utilisent un élément de gain programmable avec une entrée DC comme simple convertisseur N/A pour générer une forme d'onde sinusoïdale par étapes. La linéarité de la sortie sinusoïdale dépend essentiellement du nombre et de la précision des niveaux d'étape utilisés pour construire le signal. Toutefois, l'augmentation du nombre d'étapes implique l'augmentation du nombre de trajets de signal et donc de la complexité de conception du circuit.

Plusieurs implémentations de générateurs basés sur SC reposent sur un SC-VGA programmable. Chaque pas de gain représente la valeur d'une onde sinusoïdale parfaitement échantillonnée. Pour un amplificateur à pas de gain N , il est possible de générer une onde sinusoïdale par étapes avec un maximum de $4N$ échantillons. Les principaux avantages de cette mise en œuvre sont la simplicité, la mise en œuvre compacte et le contrôle simple de la fréquence et de l'amplitude du signal généré via la tension d'entrée VDC et la fréquence d'horloge des signaux de commande. Cependant, en termes de linéarité du signal de sortie, les performances de cette approche sont limitées par la précision et le nombre de niveaux de pas et par la sélectivité du filtre de sortie. Ainsi, l'amélioration de la pureté spectrale de la sortie nécessitera la mise en œuvre de davantage trajets de signaux et l'utilisation d'un filtre très sélectif très lisse, ce qui implique une augmentation de la complexité de la conception et un surcharge de la surface.

A.2.3 Générateurs basés sur des techniques d'annulation d'harmoniques

L'annulation d'harmonique est une technique de traitement de signal qui vise à générer un signal analogique avec une qualité spectrale élevée en combinant un ensemble de versions pondérées et décalées dans le temps d'un signal périodique arbitraire. Cette technique permet de supprimer un ensemble de composantes de distorsion harmonique non désirées du spectre du signal périodique généré, sans ressources supplémentaires pour la mesure et la pré-distorsion, comme dans [27, 28, 29]. Par conséquent, l'annulation des harmoniques peut être utilisée dans un scénario de génération de signal sinusoïdal pratique pour annuler les composantes harmoniques proches de la fréquence fondamentale du signal souhaité, tandis qu'un filtre passe-bas atténue les harmoniques d'ordre supérieur.

Au cours des dernières années, plusieurs générateurs de signaux sinusoïdaux ont été présentés. Ils exploitent l'annulation des harmoniques pour réduire la complexité des circuits sur la base des architectures présentées précédemment. Le générateur proposé dans [42] implémente l'annulation des harmoniques à l'entrée d'un filtre passe-bas de deuxième ordre à capacités commutées modifié. Le géné-

rateur tire parti de l'étage d'entrée programmable du générateur de base présenté précédemment sur la figure A.8 pour fournir les versions déphasées du signal sinusoïdal simultanément, en utilisant les mêmes éléments. Étant donné qu'il existe un compromis entre le nombre d'harmoniques à annuler, le nombre de signaux de construction, la complexité de l'implémentation et le contrôle de l'étape d'entrée [43], les auteurs de [42] proposent de combiner simultanément trois fonctions sinusoïdales. signaux déphasés de $2\pi/9$. L'objectif principal de ce scénario de génération est de supprimer la composante harmonique du troisième ordre, qui est la composante de distorsion harmonique la plus significative, dans le spectre de l'onde sinusoïdale générée avant d'atteindre l'étape de filtrage. Les résultats de [42] démontrent que ce générateur est capable de fournir un signal linéaire sinusoïdal en sortie avec un THD de -77 dB à 1 MHz.

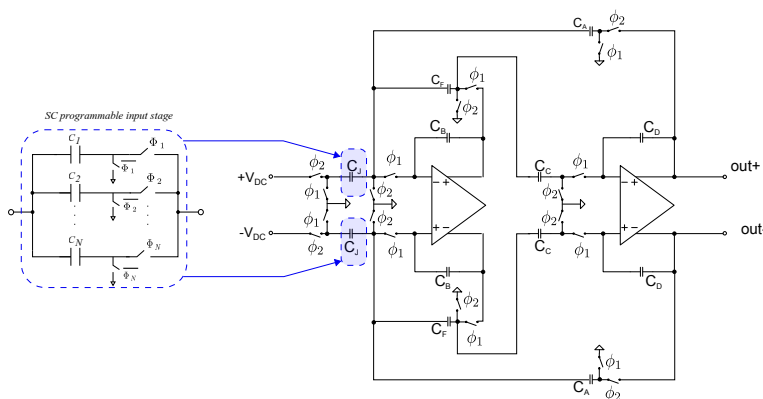


FIGURE A.8 : Générateur à capacité commuté avec annulation des harmoniques.

Une autre approche largement explorée pour générer des signaux périodiques déphasés dans le contexte de la génération de signaux avec annulation d'harmoniques est l'utilisation d'oscillateurs en anneau [43, 44, 45, 46, 47]. Les générateurs utilisent un oscillateur en anneau à décalage de phase à N étages, comme illustré à la figure A.9 pour fournir un ensemble de signaux déphasés. La sortie de deux étages consécutifs de l'oscillateur aura un déphasage de $\frac{2\pi}{N}$ de cette manière, le décalage de phase sélectionné peut être implémenté en choisissant correctement le nombre d'étages de l'oscillateur. Suivant le schéma général d'annulation d'harmoniques de la figure A.9, les signaux déphasés sélectionnés sont ensuite acheminés vers un étage de pondération et sont additionnés pour annuler un ensemble d'harmoniques non désirés.

L'algorithme de mise en forme de distorsion, initialement proposé pour améliorer la linéarité des générateurs externes à faible coût (AWG) [52, 53], vise à pré-compenser, dans le domaine numérique, la non-linéarité des blocs analogiques et mixtes dans la chaîne de génération du signal. En particulier, cette technique

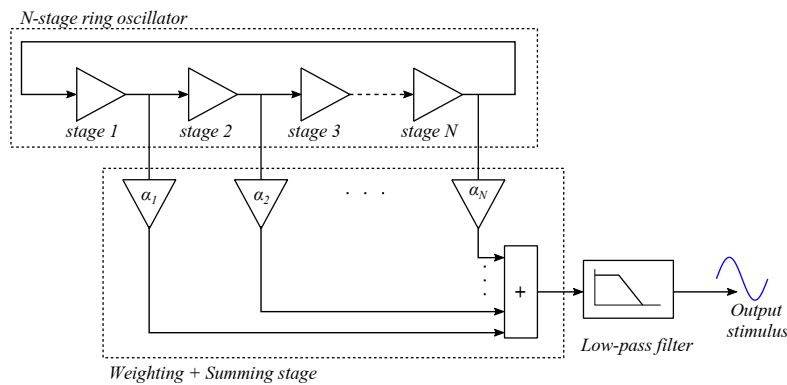


FIGURE A.9 : Générateur basé sur un oscillateur à anneaux avec annulation d'harmonique.

propose d'entrelacer des versions décalées dans le temps du signal sinusoïdal cible de manière à ce que les produits d'intermodulation produits par les blocs non linéaires suivants dans la chaîne de signaux déplacent les harmoniques d'ordre inférieur vers des fréquences plus éloignées du son principal.

A.3 Techniques d'annulation harmonique utilisant des ressources numériques

Le compromis important entre la pureté spectrale du stimulus analogique généré et la complexité de conception des générateurs de signaux analogiques a toujours été l'élément clé le plus critique pour la conception de générateurs sinusoïdaux sur puce pour les BIST analogiques et mixtes, spécialement lorsque des performances élevées sont requises, telles qu'un fonctionnement à haute fréquence, une résolution élevée du stimulus et un THD bas. Un défi commun aux conceptions de générateur de signal analogique proposées précédemment, est la conception du filtre de sortie. Les concepteurs ont toujours pour objectif d'intégrer des filtres hautement linéaires à basses fréquences de coupure afin d'atténuer toutes les composantes harmoniques indésirables, ce qui est une tâche fastidieuse et qui prend du temps. Pour cette raison, certains travaux avancés explorent de nouvelles stratégies, basées sur des techniques d'annulation harmonique, capables de générer des signaux analogiques ne contenant pas un certain nombre de composantes harmoniques d'ordre inférieur avant d'alimenter le filtre de sortie. Ainsi, les spécifications du filtre de sortie seront assouplies car il sera utilisé pour filtrer uniquement les composantes harmoniques de distorsion d'ordre élevé.

A.3.1 Base théorique

La technique d'annulation des harmoniques est basée sur la manipulation et la combinaison linéaire d'un certain nombre de signaux périodiques, d'amplitudes et de déphasages différents, afin de fournir un signal périodique dans lequel un certain nombre de composantes harmoniques sélectionnées sont atténuées ou complètement annulées dans le domaine fréquentiel. Considérons un signal périodique générique $x(t)$ exprimé comme une extension de série de Fourier comme :

$$x(t) = \sum_{k=1}^{\infty} A_k \cos(k\omega_0 t + \varphi_k) \quad (\text{A.1})$$

où A_k et φ_k sont l'amplitude et la phase de la composante harmonique k dans le signal $x(t)$, respectivement, et ω_0 est la fréquence fondamentale de $x(t)$.

Sans perte de généralité, définissons le signal $y(t)$ comme combinaison linéaire du signal $x(t)$ multiplié par un facteur α_0 et p paires de signaux pondérés par des facteurs α_i et décalés avec des décalages temporels opposés Δt_i et $-\Delta t_i$ par rapport au signal $x(t)$,

$$y(t) = \alpha_0 x(t) + \sum_{i=1}^p \alpha_i [x(t + \Delta t_i) + x(t - \Delta t_i)] \quad (\text{A.2})$$

Des équations (A.1) et A.2), il peut être dérivé,

$$y(t) = \sum_{k=1}^{\infty} A_k \left[\alpha_0 + 2 \sum_{i=1}^p \alpha_i \cos(k\phi_i) \right] \cos(k\omega_0 t + \varphi_k) \quad (\text{A.3})$$

Ainsi, la combinaison d'un signal périodique et de ses versions échelonnées et déphasées a un contenu spectral identique à celui du signal périodique original, mais échelonné par des coefficients $[\alpha_0 + 2 \sum_{i=1}^p \alpha_i \cos(k\phi_i)]$. En d'autres termes, en sélectionnant un ensemble approprié de déphasages ϕ_i et poids de pondération α_0 et α_i tels que ces coefficients sont petits pour des valeurs données de k , composants harmoniques indésirables dans $y(t)$ peut être atténué ou complètement annulé.

A.3.2 Implémentation pratique

De manière similaire à [50, 54, 46], nous proposons d'appliquer la technique d'annulation d'harmonique décrite à un ensemble de signaux carrés numériques afin de produire un signal sinusoïdal analogique de haute qualité. Nous devons donc combiner p paires de versions pondérées et déphasés d'un signal carré, telles que définies dans (A.3). Et selon (A.3), pour annuler la $k^{\text{ème}}$ composante harmonique,

nous devons trouver les déphasages ϕ_i et poids α_0 et α_i qui vérifie la condition d'annulation d'harmoniques :

$$\alpha_0 + 2 \sum_{i=1}^p \alpha_i \cos(k\phi_i) = 0 \quad (\text{A.4})$$

Sur la base des résultats analytiques présentés, nous proposons une architecture matérielle simple afin de mettre en œuvre un générateur de signal sinusoïdal efficace utilisant des signaux numériques carrée et la technique de suppression d'harmoniques décrite.

L'architecture proposée est illustrée à la figure A.10. Elle comporte un générateur numérique qui fournit un ensemble de signaux carrés numériques retardés, une étape de pondération pour mettre à l'échelle et combiner les différentes phases d'ondes carrées, ainsi qu'un simple filtre passe-bas pour filtrer les composantes harmoniques d'ordre élevé en sortie. Le générateur sélectionné doit être conçu pour fournir deux sorties entièrement différentielles de manière à ce que tous les composants à harmoniques paires soient absents et que la technique de suppression des harmoniques soit utilisée pour supprimer uniquement les harmoniques d'ordre impair.

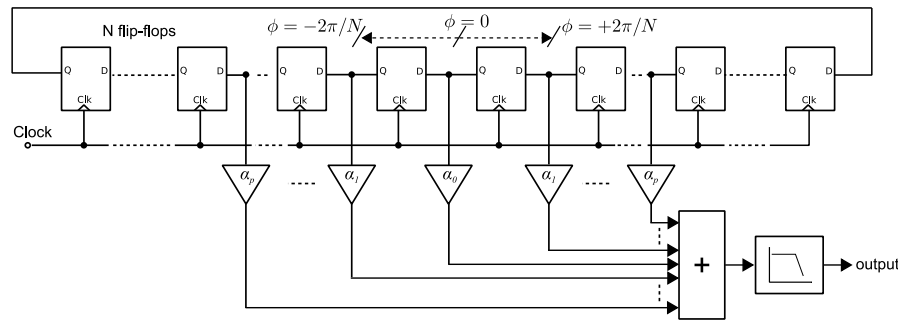


FIGURE A.10 : Schéma du générateur de signaux sinusoïdal proposé.

A.3.3 Annulation d'harmonique avec les rapports de poids unitaire utilisant un nombre impair de signaux

Considérons le signal $y_1(t)$ défini comme signal $y(t)$ dans (A.2) mais avec les poids $\alpha_0 = 1$, $\alpha_1 = 1$ et $p = 1$ tel que :

$$\begin{aligned} y_1(t) &= x(t) + x(t + \Delta t_1) + x(t - \Delta t_1) \\ &= \sum_{k=1}^{\infty} A_k [1 + 2 \cos(k\phi_1)] \cos(k\omega_0 t + \varphi_k) \end{aligned} \quad (\text{A.5})$$

Dans cette configuration, il est facile de démontrer que la composante de troisième harmonique du signal d'origine $x(t)$ peut être facilement annulée en définissant $\phi_1 = 2\pi/9$ comme :

$$\begin{cases} 1 + 2\cos(k\frac{2\pi}{9}) = 0 & k = 3 \\ 1 + 2\cos(k\frac{2\pi}{9}) \neq 0 & k = 1 \end{cases} \quad (\text{A.6})$$

Reprenons le même processus et définissons maintenant le signal $y_2(t)$ comme combinaison linéaire du signal $y_1(t)$ et deux versions déphasées de $y_1(t)$ avec des délais opposés $\pm\Delta t_2$ comme :

$$\begin{aligned} y_2(t) &= y_1(t) + y_1(t + \Delta t_2) + y_1(t - \Delta t_2) \\ &= \sum_{k=1}^{\infty} A_k [1 + 2\cos(k\phi_1)] [1 + 2\cos(k\phi_2)] \cos(k\omega_0 t + \varphi_k) \end{aligned} \quad (\text{A.7})$$

De nouveau, comme on peut le constater, une nouvelle condition d'annulation d'harmoniques apparaît $[1 + 2\cos(k\phi_1)] \times [1 + 2\cos(k\phi_2)] = 0$ et deux composantes harmoniques peuvent être annulées en sélectionnant soigneusement les variables ϕ_1 et ϕ_2 . Par exemple, les composantes harmoniques des troisième et cinquième ordres peuvent être annulées en définissant $\phi_1 = 2\pi/9$ et $\phi_2 = 2\pi/15$ comme :

$$\begin{cases} [1 + 2\cos(k\frac{2\pi}{9})] [1 + 2\cos(k\frac{2\pi}{15})] = 0 & k = 3 \text{ and } 5 \\ [1 + 2\cos(k\frac{2\pi}{9})] [1 + 2\cos(k\frac{2\pi}{15})] \neq 0 & k = 1 \end{cases} \quad (\text{A.8})$$

Cette opération nécessite l'utilisation de 9 signaux carrés $sq_1(t)$ à $sq_9(t)$ répartis en trois ensembles de trois signaux, où le déphasage relatif entre les signaux d'un même ensemble $\phi_1 = 2\pi/9$ et le déphasage entre les ensembles $\phi_2 = 2\pi/15$, tel qu'il est présenté schématiquement à la figure A.11.

Cette stratégie d'annulation d'harmoniques peut être généralisée pour annuler un nombre quelconque d'harmoniques. Si nous itérons le processus p fois, le signal résultant $y_p(t)$ peut être écrit comme :

$$\begin{aligned} y_p(t) &= y_{p-1} + y_{p-1}(t + \Delta t_p) + y_{p-1}(t - \Delta t_p) \\ &= \sum_{k=1}^{\infty} A_k \prod_{i=1}^p [1 + 2\cos(k\phi_i)] \cos(k\omega_0 t + \varphi_k) \end{aligned} \quad (\text{A.9})$$

Et la condition d'annulation résultante pour un harmonique donné k inférieur à $2p + 1$ peut être exprimé par :

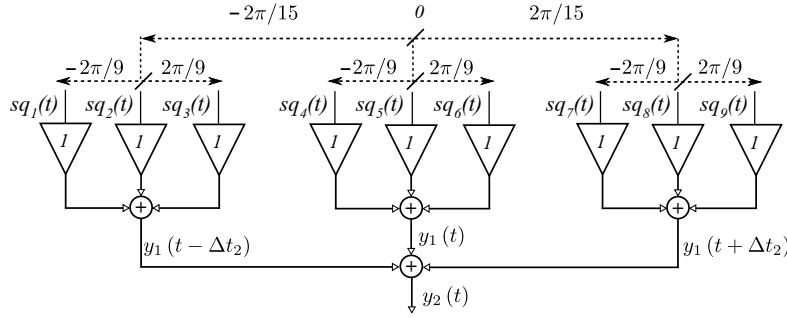


FIGURE A.11 : Schéma de la stratégie d'annulation des harmoniques utilisant des rapports de pondération unitaires et un nombre impair de signaux pour annuler la 3ème et la 5ème composantes harmonique.

$$\prod_{i=1}^p [1 + 2 \cos(k\phi_i)] = 0 \quad (\text{A.10})$$

Cette stratégie d'annulation d'harmoniques simplifie l'implémentation des poids de pondération en les rendant égales. Toutefois, un registre à décalage plus long est nécessaire pour fournir les décalages de phase appropriés.

A.3.4 Annulation d'harmonique avec les rapports de poids unitaire utilisant un nombre pair de signaux

Afin de réduire la complexité du synthétiseur numérique à ondes carrées déphasé dans le générateur présenté ci-dessus, nous présentons une stratégie similaire d'annulation de l'harmonique utilisant des rapports de poids unitaires avec un nombre réduit d'ondes carrées. Considérons le signal $y_1(t)$ défini comme signal $y(t)$ dans (A.2) mais avec les poids $\alpha_0 = 0$, $\alpha_1 = 1$ et $p = 1$ tel que :

$$\begin{aligned} y_1(t) &= x(t + \Delta t_1) + x(t - \Delta t_1) \\ &= \sum_{k=1}^{\infty} 2A_k \cos(k\phi_1) \cos(k\omega_0 t + \varphi_k) \end{aligned} \quad (\text{A.11})$$

avec la même notation précédemment définie. Dans cette configuration, une composante harmonique donnée peut être annulée en choisissant une valeur appropriée de ϕ_1 . Par exemple, le troisième composant harmonique peut être annulé en définissant $\phi_1 = \pi/6$ comme :

$$\begin{cases} \cos(k\frac{\pi}{6}) = 0 & k = 3 \\ \cos(k\frac{\pi}{6}) \neq 0 & k = 1 \end{cases} \quad (\text{A.12})$$

De la même manière que dans le cas précédent, le processus peut être itéré. Définissons le signal $y_2(t)$ comme :

$$\begin{aligned} y_2(t) &= y_1(t + \Delta t_2) + y_1(t - \Delta t_2) \\ &= \sum_{k=1}^{\infty} 2^2 A_k \cos(k\phi_1) \cos(k\phi_2) \cos(k\omega_0 t + \varphi_k) \end{aligned} \quad (\text{A.13})$$

Dans le signal résultant $y_2(t)$, la composante harmonique de cinquième ordre peut être facilement annulé en définissant $\phi_2 = \pi/10$ et une nouvelle condition d'annulation d'harmoniques semble annuler les composantes harmoniques de troisième et cinquième ordre comme suit :

$$\begin{cases} \left[\cos(k\frac{\pi}{6}) \right] \left[\cos(k\frac{\pi}{10}) \right] = 0 & k = 3 \text{ and } 5 \\ \left[\cos(k\frac{\pi}{6}) \right] \left[\cos(k\frac{\pi}{10}) \right] \neq 0 & k = 1 \end{cases} \quad (\text{A.14})$$

Cette stratégie d'annulation d'harmoniques peut être mise en œuvre en combinant quatre signaux carrés $sq_1(t)$ à $sq_4(t)$, comme illustré schématiquement à la figure A.12. Ces 4 signaux carrés sont réparties en deux ensembles de deux signaux carrés avec des déphasages relatifs de $\pi/3$, alors que le déphasage entre les deux ensembles est de $\pi/5$.

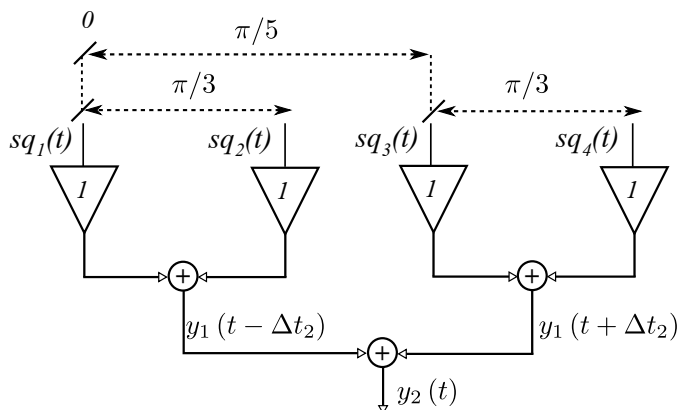


FIGURE A.12 : Schéma de la stratégie d'annulation des harmoniques utilisant des rapports de pondération unitaires et un nombre pair de signaux pour annuler la 3ème et la 5ème composantes harmonique.

Là encore, cette stratégie d'annulation d'harmoniques peut également être généralisée pour annuler un nombre quelconque d'harmoniques. Si nous itérons le processus p fois, le signal résultant $y_p(t)$ peut être écrit comme :

$$\begin{aligned}
 y_p(t) &= y_{p-1}(t + \Delta t_p) + y_{p-1}(t - \Delta t_p) \\
 &= \sum_{k=1}^{\infty} 2^p A_k \prod_{i=1}^p \cos(k\phi_i) \cos(k\omega_0 t + \varphi_k)
 \end{aligned} \tag{A.15}$$

Et la condition d'annulation résultante pour un harmonique donné k peut être exprimé par :

$$\prod_{i=1}^p \cos(k\phi_i) = 0 \tag{A.16}$$

De la même manière que la stratégie d'annulation d'harmoniques précédente, plusieurs équations harmoniques peuvent être annulées à l'aide de cette équation de conception, au prix d'une complexité accrue.

A.3.5 Annulation d'harmonique avec les rapports de poids entier

Une stratégie similaire peut être conçue pour atteindre les conditions d'annulation des harmoniques en utilisant des rapports de poids entiers pour toutes les signaux déphasés. Considérons le signal $y_1(t)$ défini comme signal $y(t)$ dans (A.2) mais avec les poids $\alpha_0 = 2$, $\alpha_1 = 1$, et $p = 1$ comme :

$$\begin{aligned}
 y_1(t) &= 2x(t) + x(t + \Delta t_1) + x(t - \Delta t_1) \\
 &= \sum_{k=1}^{\infty} 2A_k [1 + \cos(k\phi_1)] \cos(k\omega_0 t + \varphi_k)
 \end{aligned} \tag{A.17}$$

Dans cette configuration, la troisième composante harmonique peut être annulée en définissant $\phi_1 = \pi/3$:

$$\begin{cases} 1 + \cos(k\frac{\pi}{3}) = 0 & k = 3 \\ 1 + \cos(k\frac{\pi}{3}) \neq 0 & k = 1 \end{cases} \tag{A.18}$$

De la même manière que dans le cas précédent, le processus peut être itéré. Définissons le signal $y_2(t)$ comme :

$$\begin{aligned}
 y_2(t) &= 2y_1(t) + y_1(t + \Delta t_2) + y_1(t - \Delta t_2) \\
 &= \sum_{k=1}^{\infty} 2^2 A_k [1 + \cos(k\phi_1)] [1 + \cos(k\phi_2)] \cos(k\omega_0 t + \varphi_k)
 \end{aligned} \tag{A.19}$$

Dans le signal résultant $y_2(t)$, la composante harmonique de cinquième ordre peut être facilement annulé en définissant $\phi_2 = \pi/6$, et une nouvelle condition d'annulation d'harmoniques apparaît, qui est le produit de la condition d'annulation d'harmoniques du troisième ordre et du cinquième ordre tel que :

$$\begin{cases} [1 + \cos(k\frac{\pi}{3})] [1 + \cos(k\frac{\pi}{6})] = 0 & k = 3 \text{ and } 5 \\ [1 + \cos(k\frac{\pi}{3})] [1 + \cos(k\frac{\pi}{6})] \neq 0 & k = 1 \end{cases} \quad (\text{A.20})$$

De la même manière que la stratégie d'annulation harmonique avec des rapports unitaire présentée dans la section précédente, nous proposons d'implémenter la stratégie d'annulation harmonique avec des rapports binaire de la même manière pour annuler les composantes harmoniques du troisième et du cinquième ordre en définissant $\phi_1 = \pi/3$ et $\phi_2 = \pi/5$. Cette solution utilise une combinaison de 9 signaux carrés $sq_1(t)$ à $sq_9(t)$, comme il est montré schématiquement à la figure A.13. Ces 9 signaux carrés sont réparties en trois séries, chacune contenant trois signaux carrés avec un déphasage relatif de $\pm\pi/3$, et les ensembles sont déphasés de $\pm\pi/5$.

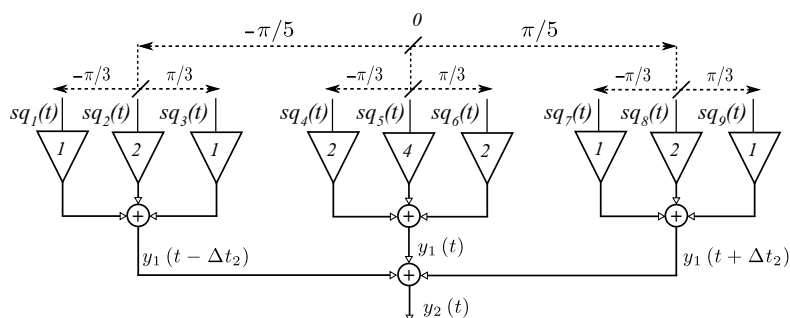


FIGURE A.13 : Schéma de la stratégie d'annulation des harmoniques utilisant des rapports de pondération entier pour annuler la 3ème et la 5ème composantes harmonique.

Cette stratégie d'annulation d'harmoniques peut être facilement généralisée pour annuler un nombre quelconque d'harmoniques. Ainsi, si nous itérons le processus p fois, le signal résultant $y_p(t)$ peut être écrit comme :

$$\begin{aligned} y_p(t) &= 2y_{p-1}(t) + y_{p-1}(t + \Delta t_p) + y_{p-1}(t - \Delta t_p) \\ &= \sum_{k=1}^{\infty} 2^p A_k \prod_{i=1}^p [1 + \cos(k\phi_i)] \cos(k\omega_0 t + \varphi_k) \end{aligned} \quad (\text{A.21})$$

Et la condition d'annulation résultante pour un harmonique donné k peut être exprimé par l'équation suivante pour annuler toutes les composantes harmoniques impaires inférieures à $2p + 1$:

$$\prod_{i=1}^p [1 + \cos(k\phi_i)] = 0 \quad (\text{A.22})$$

Cependant, l'annulation de plusieurs composants harmoniques nécessite des registres à décalage plus longs pour pouvoir générer les phases de signal requises et augmenter le nombre de phases de signal requises, augmentant ainsi la complexité de la conception.

A.3.6 Annulation d'harmonique avec les rapports de poids entier irrationnels

Une solution possible pour résoudre la condition d'annulation d'harmoniques dans A.4 est de définir $\alpha_0 = 1$ et de calculer les déphasages ϕ_i et les facteurs α_i comme :

$$\begin{cases} \phi_i = i \frac{2\pi}{4(p+1)} & 1 \leq i \leq p \\ \alpha_i = \cos(i \frac{2\pi}{4(p+1)}) & 1 \leq i \leq p \end{cases} \quad (\text{A.23})$$

Ces coefficients permettent d'annuler un ensemble donné de composantes harmoniques impaires de faible ordre dans le signal carré original $sq(t)$ inférieur au $2(2p + 1)$. Un filtre passe-bas peut être utilisé pour atténuer les composantes harmoniques haute fréquence.

Dans une implémentation pratique, il existe un compromis clair entre le nombre d'harmoniques pouvant être annulés et la complexité du générateur, car le nombre nécessaire de versions retardées du signal carré d'origine augmente si l'annulation des harmoniques est étendue à un ordre élevé d'harmoniques.

Nous proposons une solution utilise une combinaison de 5 signaux carrés $sq_1(t)$ à $sq_5(t)$, tel qu'il est représenté sur la figure A.14 avec des décalages de phase opposés $\phi_1 = \frac{\pi}{6}$ et $\phi_2 = \frac{\pi}{3}$ et poids de la balance $\alpha_0 = 1$, $\alpha_1 = \frac{\sqrt{3}}{2}$ et $\alpha_2 = \frac{1}{2}$, en utilisant la notation entre (A.3). Selon les résultats analytiques de (A.23), cette configuration annule les composantes harmoniques des troisième, cinquième, septième et neuvième ordre du signal carré d'origine $x(t)$, tout en conservant une complexité de conception réduite.

La figure A.15 montre un schéma fonctionnel d'un générateur de signal sinusoïdal basé sur cette stratégie d'annulation d'harmoniques pour annuler les composantes harmoniques des troisième, cinquième, septième et neuvième ordres. Les déphasages requis peuvent être facilement obtenus à l'aide d'un registre à décalage à 12 bascules, initialement chargé sur 6 logiques '1' consécutives et sur 6 logiques '0' consécutifs, afin de générer un signal carré avec un rapport cyclique de 50% .

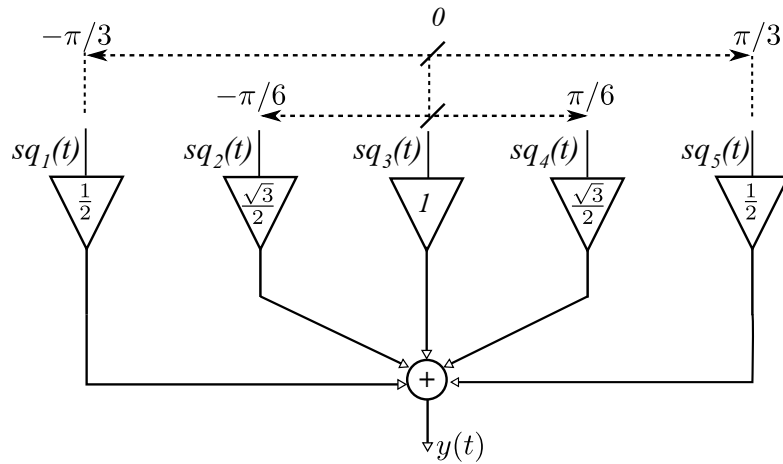


FIGURE A.14 : Schéma de la stratégie d'annulation des harmoniques utilisant des rapports irrationnelles.

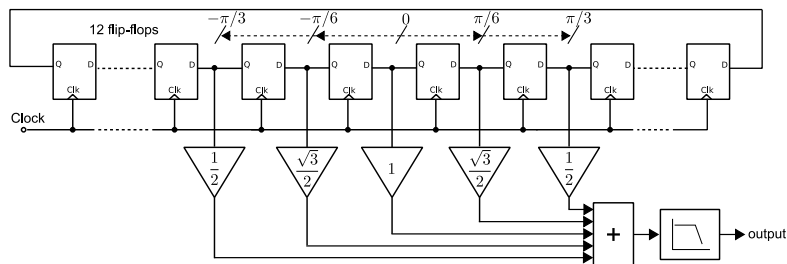


FIGURE A.15 : Schéma bloc du générateur de signal sinusoïdal proposé.

A.3.7 Comparaison de différentes techniques d'annulation d'harmoniques

Les principales limitations de l'implémentation des stratégies de génération du signal sinusoïdale présentées sont les variations aléatoires des rapports des poids de pondération et le déphasage des signaux carrés combinés. Afin de démontrer la faisabilité des stratégies d'annulation harmoniques proposées, nous avons développé des modèles comportementaux réalistes pour les générateurs décrits. Le but de ces simulations est d'analyser l'efficacité de l'annulation en présence d'imperfections de fabrication susceptibles d'introduire des écarts dans les déphasages et les rapports de pondération requis pour les techniques d'annulation harmonique considérées. Une série de simulations comportementales statistiques ont été réalisées dans MATLAB en tenant compte de la disparité entre les poids de la balance et les délais de propagation des bascules. La discordance de poids de pondération a été modélisée comme variable aléatoire avec une distribution gaussienne. Il convient de noter que ce modèle de non-concordance simple vise à fournir une limite de performance supérieure, indépendamment de la réalisation pratique des pondérations, dans le but de guider l'exploration des compromis de conception pour le générateur proposé.

Deux scénarios de fonctionnement différents ont été envisagés pour tous les générateurs proposés : un scénario haute fréquence avec des fréquences d'horloge $f_{clk} = 2 \text{ GHz}$, et un scénario à fréquence modérée avec $f_{clk} = 200 \text{ MHz}$. Noter que la fréquence du signal sinusoïdal de sortie pour chaque générateur sera égale à la fréquence d'horloge divisée par le nombre de bascules utilisées dans le registre à décalage numérique, c'est-à-dire que $f_{wave} = \frac{f_{clk}}{N}$. Notre analyse considère une perspective au niveau du système dans laquelle la fréquence d'horloge principale est donnée par le système. Étant donné que la fréquence de sortie générée est une fraction de la fréquence d'horloge principale, les compromis de conception pour les différentes architectures de générateur doivent inclure la fréquence de sortie en tant que variable.

Afin d'évaluer l'influence des erreurs de synchronisation dans les stratégies d'annulation d'harmoniques proposées, la figure A.16 montre les boîtes à moustaches du THD obtenu pour les quatre stratégies d'annulation harmoniques considérées, pour les deux fréquences d'opération différentes considérées, en fonction de l'erreur de retard maximum des bascules dans les registres à décalage, obtenue par des simulations statistiques du niveau comportemental. Un total de 100 instances de générateur ont été générées aléatoirement pour chaque combinaison de conditions de fonctionnement. Les erreurs de décalage et de décalage entre poids et pondération ont été modélisées sous forme de variables aléatoires. Dans cet ensemble de simulations, le décalage entre poids et pondération est fixé à 0,1% maximum pour toutes les simulations.

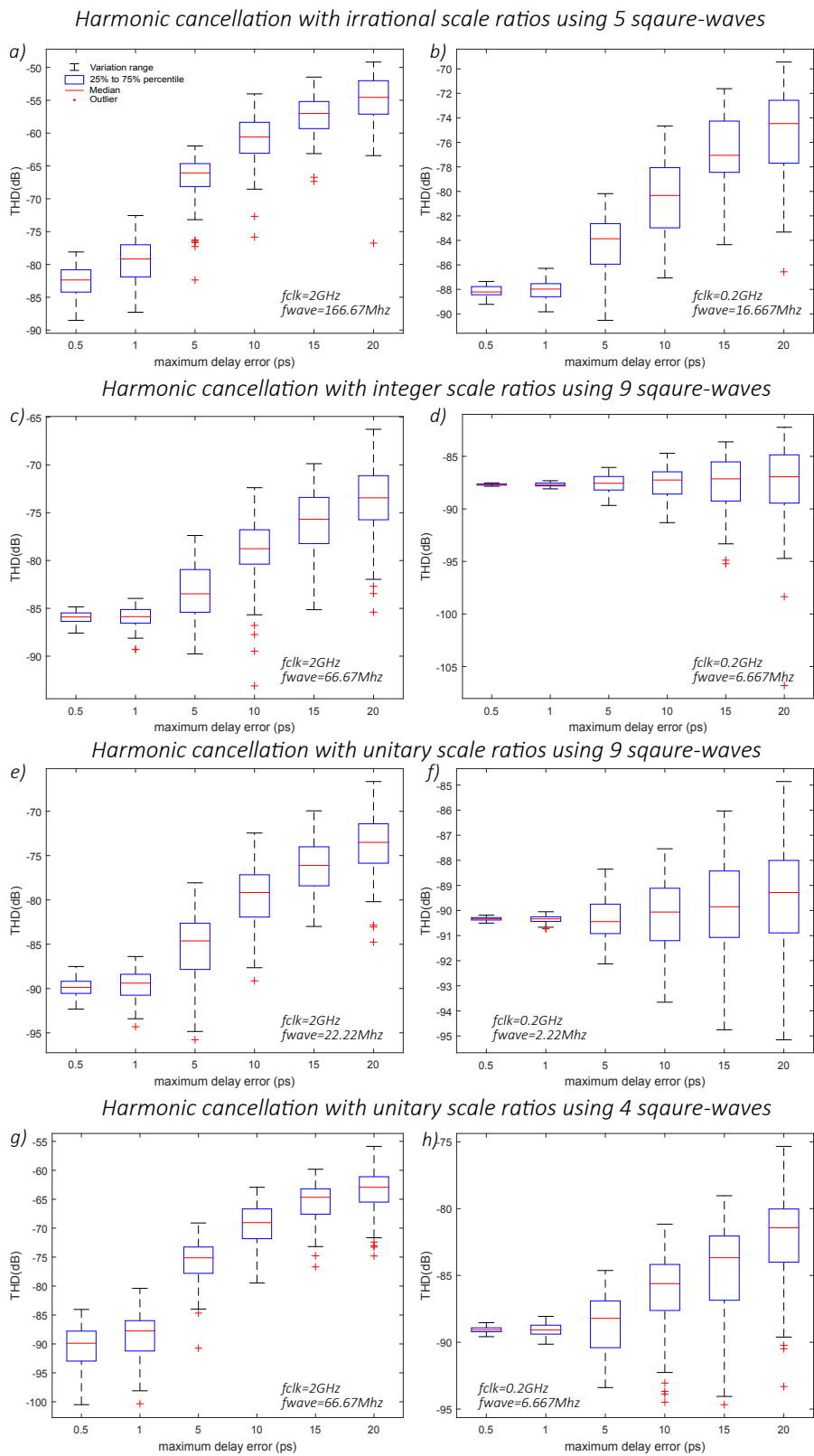


FIGURE A.16 : Variation THD de sortie générée en fonction de l'erreur de retard maximum.

Comme le montre clairement la figure A.16, pour tous les générateurs de signaux sinusoïdaux et scénarios de fonctionnement considérés, le THD obtenu est très faible (environ -90 dB) lorsque les erreurs de retard sont négligeables, ce qui indique une bonne performance des stratégies d'annulation des harmoniques proches des conditions idéales.

Dans le scénario haute fréquence, c-à-d, $F_{clk} = 2$ GHz, il est clair qu'il y a une dégradation du THD due au décalage des délais entre les bascules. Cependant, il est intéressant de noter que cette dégradation est moins importante pour les générateurs utilisant 9 signaux carrés que pour ceux utilisant moins de signaux carrés.

Afin d'évaluer l'impact de la disparité entre poids et pondération dans les stratégies d'annulation d'harmoniques proposées, la figure A.17 présente des diagrammes en boîte du THD obtenu pour les quatre stratégies d'annulation d'harmoniques considérées, en fonction de la disparité maximale entre poids et pondération dans le réseau de sommation, obtenue par des simulations statistiques du niveau de comportement. Un total de 100 des instances de générateur ont été générées aléatoirement pour chaque combinaison de conditions de fonctionnement. Les erreurs de décalage de phase et de décalage entre poids de pondération ont été modélisées sous forme de variables aléatoires. Dans cet ensemble de simulations, la non-concordance de délai est définie à 0,1 ps au maximum pour toutes les simulations.

Comme on peut le constater, l'incidence de l'inadéquation du poids de la balance est pratiquement identique pour les quatre stratégies d'annulation d'harmoniques considérées. Cependant, il est clair que la dégradation de la linéarité du signal due au déséquilibre poids-balance est plus importante que la dégradation due aux erreurs de retard. La linéarité du signal généré pour les stratégies de génération considérées dépend fortement de la précision de la phase de pondération de la balance, tandis que la dégradation de la linéarité due au décalage dans le temps n'est dominante qu'en fonctionnement à haute fréquence.

A.4 Conception de circuit et simulations

Au vu des résultats analytiques présentés dans le chapitre précédent, il est clair que la technique d'annulation harmonique proposée utilisant des ratios de poids irrationnels conduit à des implémentations plus efficaces que les autres techniques proposées, lorsque l'on considère le compromis entre le nombre de composantes harmoniques peut être annulé et le nombre nécessaire d'ondes carrées décalées déphasés.

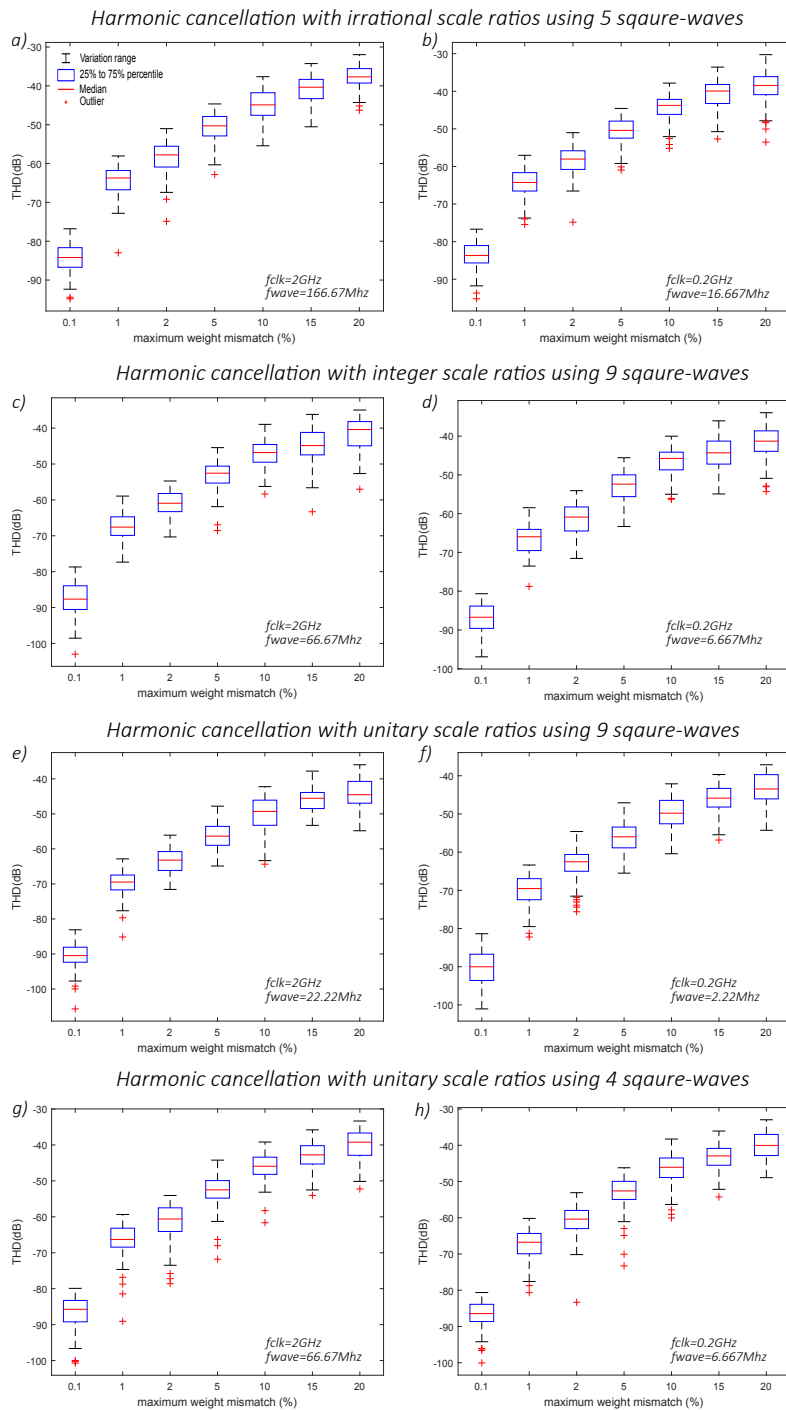


FIGURE A.17 : Variation de THD de sortie générée en fonction du décalage de poids maximal.

A.4.1 Architecture du générateur de signal sinusoïdal

Si nous considérons la technique d'annulation d'harmoniques proposée avec un poids d'échelle irrationnel présenté dans la section 1.3.7, il est clair qu'il existe un compromis entre le nombre d'harmoniques pouvant être annulés et la complexité du générateur, car le nombre nécessaire de versions retardées du signal carrée d'origine augmente si l'annulation des harmoniques est étendue aux harmoniques d'ordre élevé. De même, il existe un compromis entre le nombre d'harmoniques annulées, la complexité de l'implémentation des poids pondérations irrationnelles et la sélectivité du filtre de sortie. Compte tenu de ces compromis, nous proposons d'envisager cinq signaux carrés retardés temporellement avec des déphasages opposés $\Phi_1 = \frac{\pi}{6}$ et $\Phi_2 = \frac{\pi}{3}$ et poids de pondérations $\alpha_0 = 1$, $\alpha_1 = \frac{\sqrt{3}}{2}$ et $\alpha_2 = \frac{1}{2}$, en utilisant la notation de (1.3.2). Cette configuration annule les composantes harmoniques des troisième, cinquième, septième et neuvième ordres du signal carrée d'origine.

L'architecture du circuit est illustrée à la figure A.18, où le générateur comprend un registre à décalage circulaire qui fournit un ensemble de cinq signaux carrés numériques retardés. Les signaux générés sont acheminés vers des mémoires tampons à double extrémité qui émettent deux ondes carrées complémentaires sans modifier les cycles relatifs de déphasage et de service. Ces signaux carrés numériques complémentaires ont pour but de commander cinq branches de commande de courant totalement différentielles, dont les courants de référence ont été correctement pondérés, pour assurer l'annulation des harmoniques, comme indiqué ci-dessus. Cependant, pour assurer une bonne commutation des sources de courant, il est très important d'éviter d'ouvrir les commutateurs de courant différentiels en même temps, pour cette raison, un tampon sans chevauchement a été introduit dans l'entrée des commutateurs de courant. Les courants de sortie différentiels des cinq branches sont additionnés en utilisant un réseau passif qui fournit un filtrage supplémentaire et convertit le signal généré en un signal de tension de sortie. L'étalonnage des branches en cours sera effectué à l'aide du bloc de condensateurs de polarisation et la stratégie d'étalonnage sera présentée dans les sections suivantes.

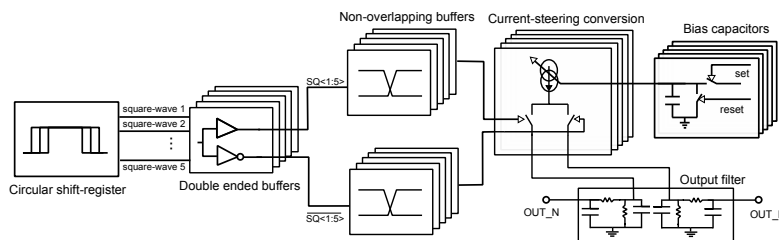


FIGURE A.18 : Schéma bloc d'une implémentation pratique du générateur de signal sinusoïdal proposé.

Chaque branche est conçue pour générer un courant pondéré avec des rapports de poids égaux à $\alpha_1 = \frac{\sqrt{3}}{2}$ et $\alpha_2 = \frac{1}{2}$. La figure A.19 montre le schéma au niveau des transistors de la source de courant de base utilisée dans la conception. Le transistor M1 est polarisé à une tension contrôlée V_{bias} pour générer un courant qui est ensuite répliqué par deux miroirs de courant (M2 à M5). Le transistor M6 est un transistor cascode pour augmenter l'impédance de sortie de la source de courant. Le courant de sortie est commuté en mode différentiel par les commutateurs M7 et M8, qui sont contrôlés par les signaux à onde carrée retardés fournis par la partie numérique du circuit.

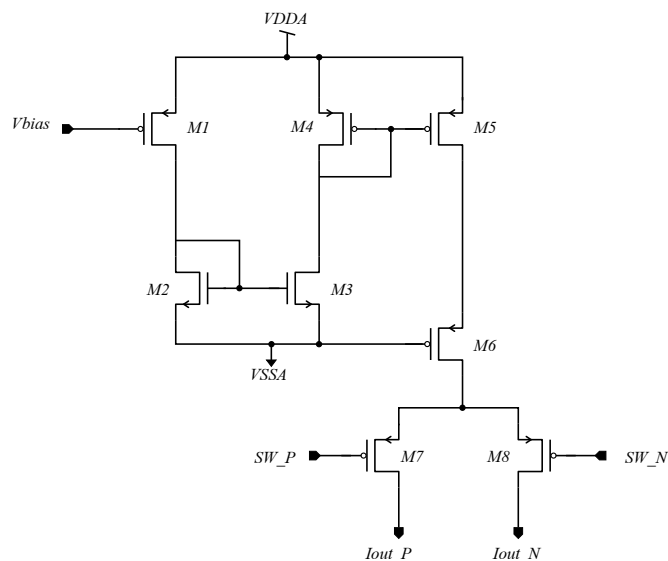


FIGURE A.19 : Branche de courant de base de conversion numérique-analogique.

Le courant fourni par chaque source de courant dans le CNA est directement contrôlé par l'ensemble des tensions de polarisation V_{bias_i} , $i = 1..5$. Étant donné que l'annulation des harmoniques proposée repose sur des poids de balance précis implémentés en tant que les rapports de courant dans le CNA, un contrôle précis de ces tensions de polarisation est nécessaire pour prendre en compte les variations de courant dues au processus et à la disparité. La figure A.20 montre le schéma de niveau de transistor du circuit de polarisation proposé. Il consiste en un condensateur pouvant être chargé et réinitialisé à l'aide de commutateurs NMOS. Le condensateur est connecté à une tension de référence continue V_{ref} via le commutateur M_{1b} contrôlé par signal numérique. Le transistor M_{2b} est connecté à la masse pour réinitialiser le condensateur. La tension au nœud V_{bias} suit la courbe exponentielle $V_{bias} = V_{ref}(1 - e^{-\frac{T_c}{R_{on}C}})$ où R_{on} est la résistance d'activation du transistor M_{1b} , C est la valeur du condensateur, et T_c est le temps de charge.

Ce circuit simple permet de contrôler la tension de polarisation de chaque branche de contrôle du courant en programmant la valeur de T_c .

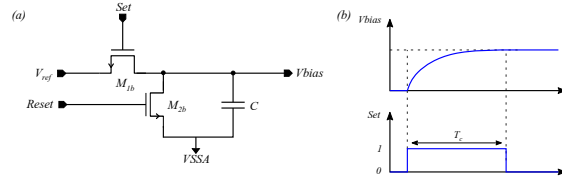


FIGURE A.20 : Schéma au niveau de transistor du circuit de polarisation de base.

Dans notre travail, nous proposons l'algorithme de calibration itératif dans A.21 qui ajuste un rapport de courant à la fois, en utilisant uniquement des mesures en courant continu. La technique de calibration commence par activer le mode de calibration en réglant le signal T_e à un "1" logique dans le registre à décalage circulaire, puis en activant séquentiellement des sources de courant individuelles en mode continu au moyen du T_i signal correspondant au trajet de courant sélectionné. Le temps de charge initial T_{ci} du contrôle des courant générés par chaque branche de courant est réglé tel que les valeurs nominales fournies par les simulations électriques. Ensuite, les courants de sortie réels (ou tensions) de toutes les sources de courant sont mesurés, séquentiellement, pour calculer leurs rapports. Si les ratios résultants sont différents des ratios nominaux fixés par la technique d'annulation d'harmoniques ($\alpha_1 = \frac{\sqrt{3}}{2}$ et $\alpha_2 = \frac{1}{2}$), temps de charge T_{ci} sont modifiés et les ratios sont mesurés et calculés à nouveau. Le processus est itéré dans une boucle d'étalonnage jusqu'à ce que les rapports mesurés correspondent aux poids de la balance cible avec une précision prédéfinie.

A.4.2 Résultats de la simulation électrique au niveau du système

Des simulations électriques du système complet au niveau des transistors sont effectuées afin de montrer la faisabilité et les performances du générateur de signaux sinusoïdal proposé. Le temps de charge T_{ci} des condensateurs de polarisation utilisés pour contrôler chaque branche de contrôle du courant sont réglés pour générer trois valeurs de courant : $I_0 = 100 \mu A$, $I_1 = 86,67 \mu A$ et $I_2 = 50 \mu A$, correspondant aux rapports pondéraux de balance requis pour la technique d'annulation d'harmoniques : $\frac{I_1}{I_0} = \frac{\sqrt{3}}{2}$ et $\frac{I_2}{I_0} = \frac{1}{2}$. Le circuit est synchronisé à $f_{clk} = 2 GHz$ pour générer un signal sinusoïdal à une fréquence égale à $\frac{f_{clk}}{12} = 166.67 MHz$.

La figure A.22 montre la forme du signal sinusoïdal généré avec une amplitude différentielle de $320 mV_{pp}$. La qualité du signal de sortie généré est évaluée en termes de THD et de SFDR. Il est important de noter que, dans les résultats

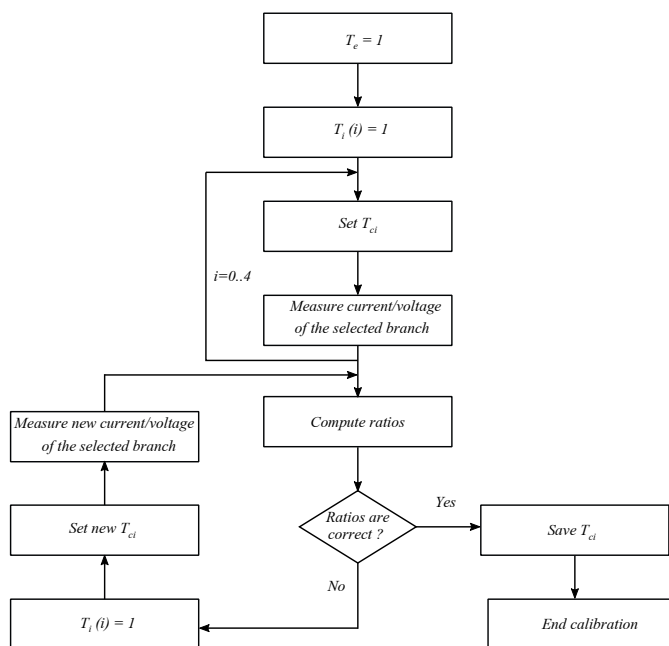


FIGURE A.21 : Algorithme de calibration d'une branche de courant.

rapportés, des mesures sont effectuées jusqu'au dixième ordre harmonique afin de prouver la faisabilité de la technique de suppression harmonique. La onzième composante harmonique n'est pas annulée et sa magnitude est constante pour toutes les expériences présentées.

La figure A.23 montre le spectre du signal généré à la sortie du filtre, obtenu à partir d'une simulation au niveau du transistor, dans les conditions typiques de la technologie. Comme prévu, le spectre montre clairement que toutes les composantes harmoniques impaires situées au-dessous de la onzième composante sont atténuées. De plus, l'absence d'harmoniques d'ordre égal est une preuve du faible biais dans le rapport cyclique de la série des signaux carrés différée dans le temps. Dans des conditions typiques, le signal sinusoïdal généré a un $THD = -78$ dB et un $SFDR = 81$ dB. Cependant, ces résultats nominaux doivent être interprétés comme une limite supérieure. En effet, comme indiqué dans nos travaux précédents, les performances de la technique de génération proposée dépendent dans une très grande mesure de l'adaptation et des variations de processus qui introduisent des erreurs d'échelle et des délais supplémentaires. Des erreurs dans les rapports pondéraux de la balance limiteront l'efficacité de l'annulation pour les composants harmoniques impairs, tandis que les écarts de synchronisation des ondes carrées introduiront des composants harmoniques d'ordre pair.

Afin d'évaluer les performances du générateur proposé en présence de variations technologiques, nous effectuons un ensemble de simulations Monte Carlo au

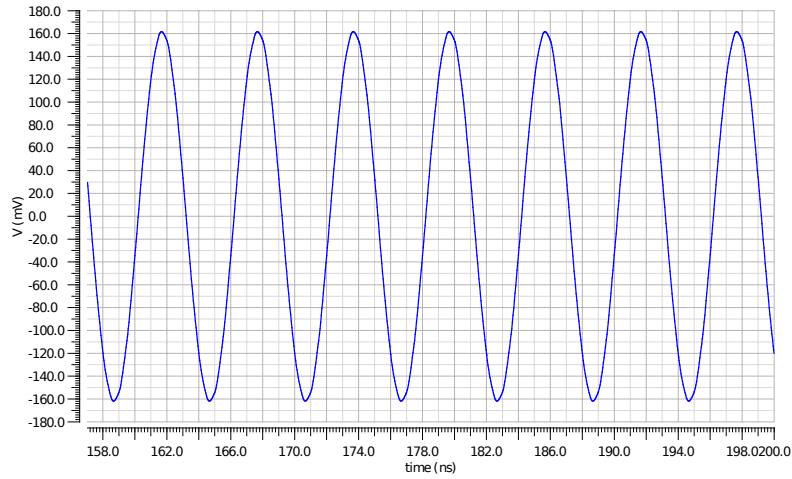


FIGURE A.22 : Signal de sortie sinusoïdal généré dans des conditions nominales.

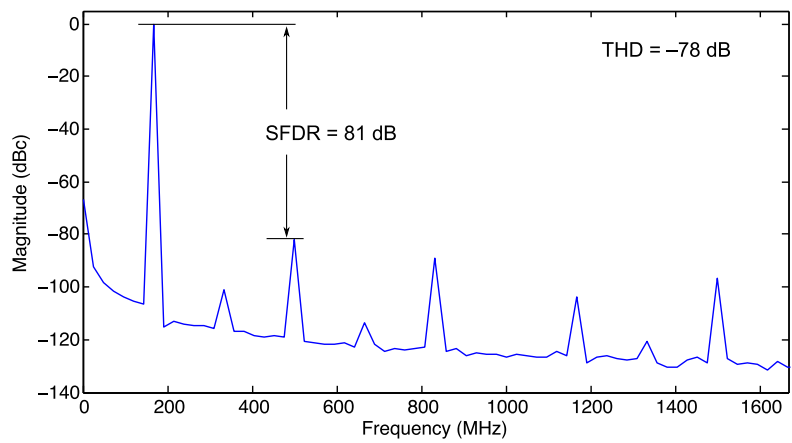


FIGURE A.23 : Spectre du signal de sortie sinusoïdal généré dans des conditions nominales.

niveau des transistors prenant en compte à la fois les variations de processus et de non-appariement incluses dans l'angle statistique de la technologie. Les figures A.24.A et A.24.B montrent les valeurs THD et SFDR du signal sinusoïdal généré, respectivement, pour 100 itérations de Monte Carlo. Ces simulations ont été effectuées sans calibrer les rapports de courant. Il est clair que nous observons une dégradation significative des performances : les valeurs moyennes des métriques de linéarité sont $THD_{mean} = -50 \text{ dB}$ et $SFDR_{mean} = 52 \text{ dB}$. Fait intéressant, les résultats montrent également que la principale source de dégradation de l'annulation des harmoniques est le déséquilibre des sources de courant, qui dévie les rapports de courant de leurs valeurs nominales, limite l'efficacité de la suppression des harmoniques d'ordre impair et introduit une discordance entre les branches positive et négative des chemins de signaux entièrement différentiels. Par ailleurs, les variations du cycle de service des ondes carrées retardées en raison du traitement et du désaccord sont très bien contrôlées, avec une variation dans le pire des cas de 0,03 % de la cible 50 % du rapport cyclique.

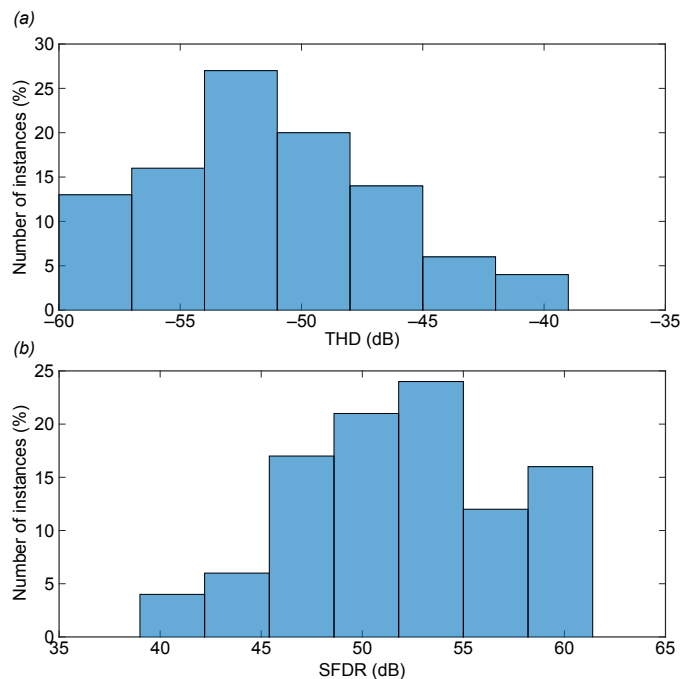


FIGURE A.24 : Histogrammes de (a) THD et (b) SFDR du signal sinusoïdal généré sur 100 simulations de Monte Carlo.

Afin de montrer la faisabilité de la technique d'étalonnage proposée, nous avons sélectionné le générateur de cas le plus défavorable obtenu par simulation Monte Carlo de processus et de mésappariement. Le spectre de la sinusoïde de sortie générée pour ce générateur de cas le plus défavorable est représenté sur la figure

A.25 qui présente un $THD = -39,5dB$ et un $SFDR = 40 dB$. Comme indiqué dans la section précédente, l'algorithme d'étalonnage proposé ajuste les courants dans les branches du courant afin d'étalonner les rapports de courant qui définissent les poids de la balance pour l'annulation des harmoniques. Le spectre de la sortie sinusoïdale générée après l'étalonnage est représenté sur la figure A.26. Il est clair que les harmoniques d'ordre impair sont grandement atténuées après l'étalonnage. La linéarité du signal calibré est considérablement améliorée, avec un $THD = -66,7 dB$ et un $SFDR = 70 dB$, ce qui correspond à $30dB$ d'amélioration par rapport au générateur non étalonné.

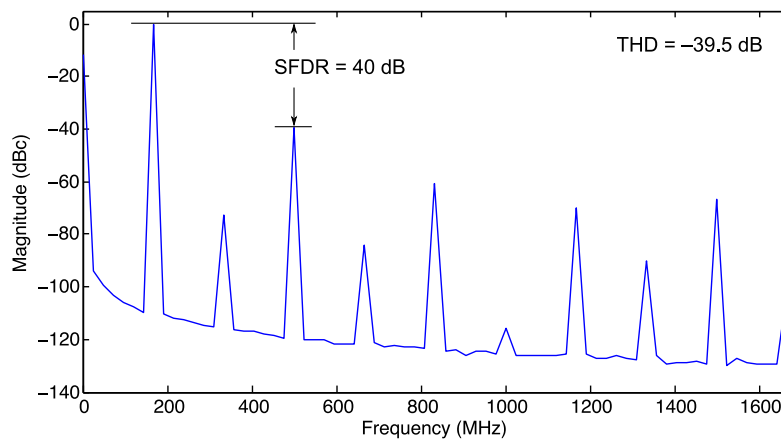


FIGURE A.25 : Spectre du signal de sortie sinusoïdal généré sous des variations de processus et de mésappariement dans le pire des cas, avant calibration.

A.4.3 Implémentation physique du générateur de signaux sinusoïdal

La figure A.27 montre le layout du prototype de preuve de concept. La structure a été développée conformément aux règles de conception de la technologie FDSOI 28 nm et aux pratiques d'implémentation conventionnelles à signaux mixtes. Ainsi, les sections analogique et numérique sont clairement séparées. Nous avons minimisé le nombre de chemins analogiques et numériques qui se croisaient et ajouté un blindage approprié si nécessaire. Les sources de courant ont une présentation identique pour améliorer la correspondance, tandis que le filtre de sortie est conçu pour conserver un chemin différentiel vers les pads de sortie. Des condensateurs de découplage ont été ajoutés aux nœuds CC sensibles.

La section numérique est agencée de manière symétrique par rapport à l'axe vertical central du circuit, tandis que l'acheminement des ondes carrées déphasées

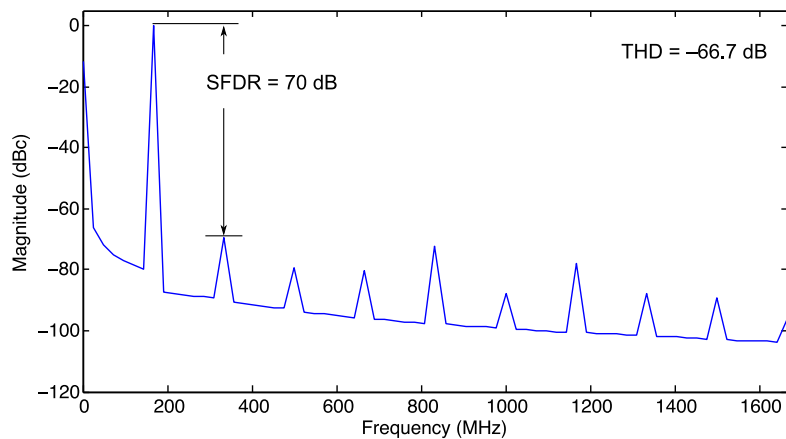


FIGURE A.26 : Spectre du signal de sortie sinusoïdal généré sous des variations de processus et de mésappariement dans le pire des cas, après calibration.

vers la section analogique a été soigneusement conçu pour fournir la même longueur aux différents signaux ordre pour éviter les retards déséquilibrés La surface du circuit est $140\mu\text{m} \times 80\mu\text{m}$.

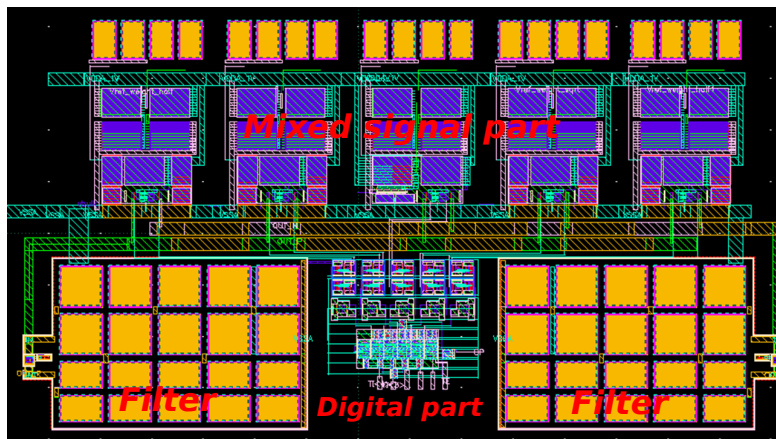


FIGURE A.27 : Layout du générateur de signal sinusoïdal.

A.4.4 Résultats des simulations post-layout

Afin de valider la faisabilité et les performances du générateur de signal sinusoïdal conçu, nous avons effectué une simulation électrique de la vue extraite. La simulation de la vue extraite inclut les effets de résistances parasites et de condensateurs introduits par le layout.

La vue extraite a été simulée dans les mêmes conditions que les simulations précédentes ($f_{clk} = 2 \text{ GHz}$). Le spectre de la sortie générée est illustré à la Fig. A.28. Comme on peut le constater, il existe une nette dégradation de la linéarité du signal généré. Cette dégradation est expliquée par les déviations des courants dans les branches sous-alimentées par des parasites d'implantation, et elle peut être considérablement atténuée en ajustant les tensions de polarisation afin de récupérer les rapports de courant appropriés définis par la stratégie de suppression des harmoniques.

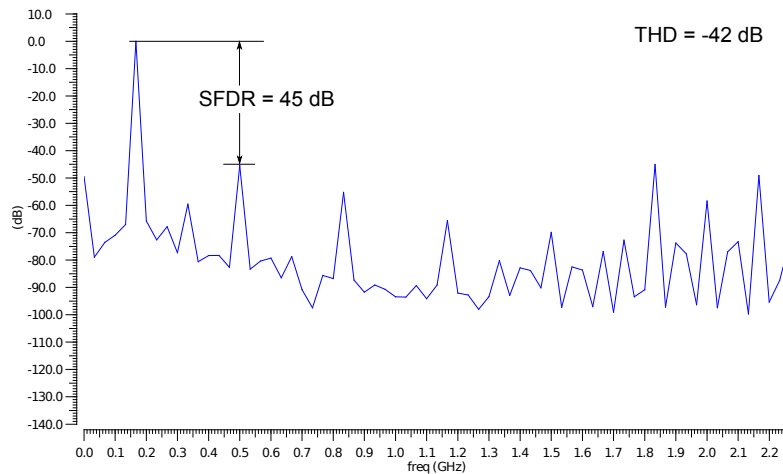


FIGURE A.28 : Le spectre du signal sinusoïdal de sortie résultait d'une simulation post-layout.

L'algorithme d'étalonnage a été présenté précédemment, cependant, puisque les condensateurs de polarisation ont été retirés de la dernière implémentation, nous avons adapté l'algorithme d'étalonnage à cette implémentation en ajustant les tensions de polarisation des sources de courant et en mesurant les courants de sortie dans le mode d'étalonnage. Le spectre du signal sinusoïdal fourni par le générateur calibré est décrit à la figure A.29. Ce spectre montre l'effet de l'étalonnage lorsque toutes les harmoniques d'ordre impair sont inférieures à -70 dBc , avec une atténuation de -20 dB par rapport au générateur non étalonné. Cependant, la linéarité des sorties est toujours limitée par la composante harmonique de second ordre qui provient d'un déséquilibre entre les chemins de signaux différentiels dû à des éléments parasites et ne peut pas être calibrée en réglant les courants de polarisation.

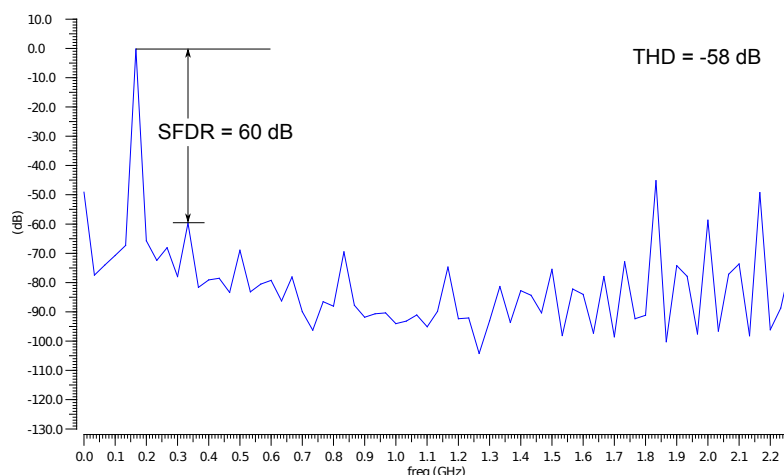


FIGURE A.29 : Le spectre du signal sinusoïdal de sortie résultait d'une simulation post-layout, après calibration.

A.5 Résultats expérimentaux

Le générateur de signal sinusoïdal proposé a été fabriqué en technologie FDSOI 28 nm à 8 métaux de STMicroelectronics. La caractérisation du prototype fabriqué a été réalisée dans le laboratoire Algeco de STMicroelectronics-Crolles. Le prototype a été conçu pour des tests au niveau des plaquettes utilisant des micro-sondes. La figure A.30 montre la microphotographie du prototype. Le circuit comprend 15 pads, afin de servir d'interface avec l'équipement externe destiné à fournir le signal d'horloge, les tensions de polarisation et les signaux de configuration numériques appropriés au circuit testé et recevoir correctement les sorties du générateur de signal sinusoïdal à évaluer.

A.5.1 Configuration de test

Le but principal de la validation expérimentale du générateur de signal sinusoïdal mis en œuvre est de valider la stratégie d'annulation des harmoniques proposée en évaluant la linéarité du signal sinusoïdal généré en termes de THD et de SFDR. Le schéma synoptique de la configuration de validation est illustré à la Fig. A.31 dans laquelle un générateur de signal haute fréquence est nécessaire pour piloter le système avec un signal d'horloge à 2 GHz, des générateurs d'impulsions permettant de configurer la séquence carrée dans le registre à décalage numérique et permettant de contrôler chaque source de courant séparément lorsque le mode de calibrage est activé.

Les générateurs de tension continue sont utilisés pour fournir les différentes

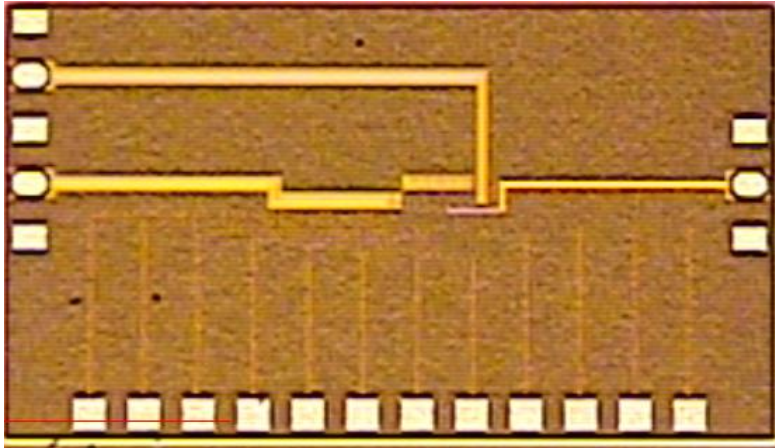


FIGURE A.30 : Micro-photographie du générateur de signal sinusoïdal.

tensions de polarisation des sources de courant. Elles seront initialement définies comme les tensions obtenues par les simulations et elles seront accordées en mode étalonnage afin de réguler les rapports de courant des sources de courant afin qu'ils soient suffisamment proches des rapports nominaux définis par la technique de suppression d'harmoniques. Il faut noter que la résolution de l'étalonnage dépend fortement de la résolution des générateurs à courant continu. Dans notre configuration expérimentale, les générateurs de tension continue sont limités à une résolution de 1 mV.

La configuration comprend également des instruments d'acquisition de signal tels qu'un oscilloscope pour afficher le signal sinusoïdal généré et un analyseur de spectre pour calculer son spectre.

Les câbles RF utilisés pour connecter la sortie du circuit à l'oscilloscope et à l'analyseur de spectre sont sélectionnés avec des longueurs égales pour éviter d'introduire un déphasage supplémentaire entre les sorties différentielles.

Un ampèremètre à haute résolution est utilisé dans le mode d'étalonnage du générateur pour mesurer et étalonner les sources de courant du générateur.

A.5.2 Procédure de test

Le test fonctionnel commence par définir les valeurs de toutes les tensions de polarisation obtenues par des simulations afin de fournir aux courants les rapports nominaux définis par les annulations d'harmoniques. La fréquence du signal d'horloge est réglée sur 2 GHz . La charge du signal carrée initiale dans le registre à décalage circulaire est réalisée au moyen de l'impulsion T_e quand tous les signaux T_i sont mis à 0V.

La sortie générée peut être d'abord acquise par l'oscilloscope pour vérifier visuel-

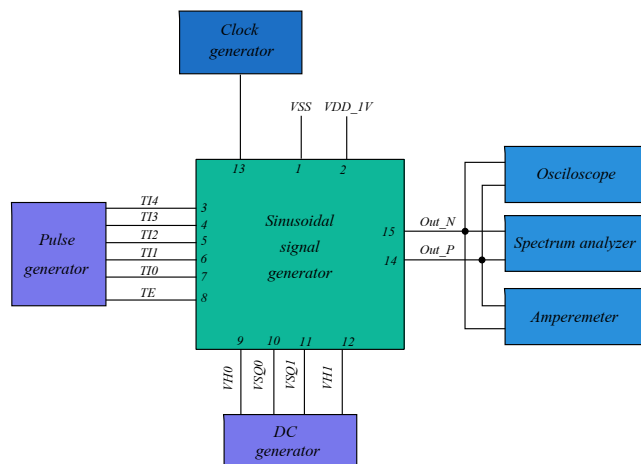


FIGURE A.31 : Schéma du montage expérimental.

lement la fonctionnalité du circuit. La sortie est ensuite connectée à l'ampèremètre pour mesurer séparément le courant délivré par chaque source de courant et calculer les rapports de courant entre les différentes branches de courant. Ensuite, le processus de calibration sera exécuté comme décrit dans l'algorithme de calibration. Une fois le processus de calibration terminé, le mode de génération est réactivé et la linéarité du signal généré est évaluée à l'aide de l'analyseur de spectre.

A.5.3 Acquisition par oscilloscope

La figure [A.32] montre le signal sinusoïdal différentiel généré par l'un des générateurs de signal sinusoïdal fabriqués pour une fréquence d'horloge de $2GHz$ (fréquence du signal de sortie $166,67 MHz$), tel qu'il était affiché sur l'oscilloscope. L'amplitude du signal de sortie est de $39 mV_{pp}$ pour une charge de 50Ω .

A.5.4 Mesures de linéarité

Le spectre du signal différentiel généré avant l'étalonnage est décrit à la Fig. A.33. Il montre que la puissance du composant principal est égale à $-29 dBm$ et la linéarité du signal sinusoïdal est limitée par la 3^{ème} et la 5^{ème} composante harmonique avec une puissance égale à $-70 dBm$ et $-74 dBm$, respectivement.

Nous avons mesuré la puissance de toutes les composantes harmoniques jusqu'au 10^{ème} en utilisant l'analyseur de spectre. Ces mesures ont été utilisées pour calculer le THD et le SFDR du signal de sortie généré par le générateur non étalonné, donnant un THD de $-38,9 dB$ et un SFDR de $41,5 dB$.

Comme prévu, la linéarité du générateur non étalonné est affectée par des non-idéalités. Afin de calibrer le générateur, les sorties du générateur testé ont été

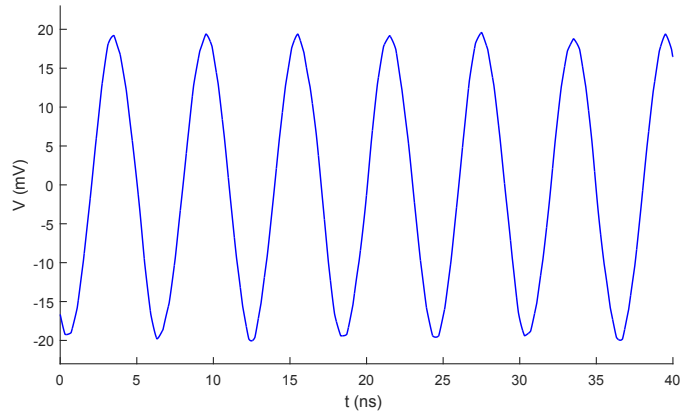


FIGURE A.32 : Acquisition par oscilloscope du signal sinusoïdal généré.

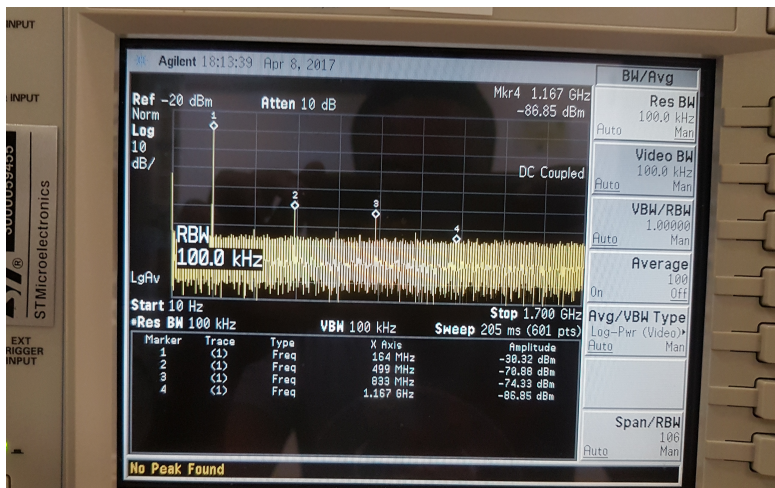


FIGURE A.33 : Photo du spectre du signal sinusoïdal généré avant calibration à 166,67 MHz.

connectées à l'ampèremètre et nous avons calculé les rapports entre les sources de courant, comme décrit dans l'algorithme de calibration. Afin de compenser les écarts, les courants fournis par les différentes sources de courant ont été étalonnés pour produire des rapports aussi proches que possible des rapports nominaux de suppression des harmoniques en réglant les tensions de polarisation. L'étape d'étalonnage dans cette configuration est limitée par la résolution du générateur de tension continue.

Le spectre du signal de sortie étalonné affiché sur l'analyseur de spectre est illustré à la Fig. A.34. Le spectre montre une amélioration de la linéarité du signal généré lorsque toutes les composantes harmoniques impaires sont atténuées et que leur puissance est très proche du bruit de fond de l'analyseur de spectre, qui est d'environ -93 dBm. Les composantes harmoniques au-dessus du 11^{ème} sont également atténuées par le filtre passe-bas et se situent sous le niveau de bruit.

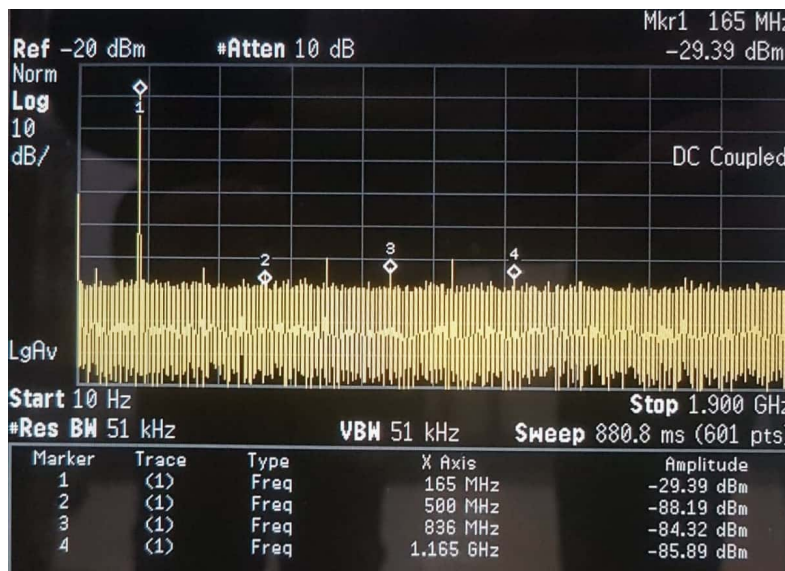


FIGURE A.34 : Photo du spectre du générateur calibré à 166,67 MHz.

A.5.5 Résultats expérimentaux à différentes fréquences d'opération

La fréquence de sortie du signal généré peut être facilement programmée en modifiant la fréquence d'horloge du registre à décalage numérique dans le générateur proposé. Toutefois, il convient de noter que la mise en œuvre de la validation de principe proposée comporte un filtre de sortie passe-bas fixe avec une fréquence de coupure de $166,67$ MHz. Si la fréquence doit être programmée, la fréquence de coupure du filtre peut également être programmée. Dans notre preuve de concept, le

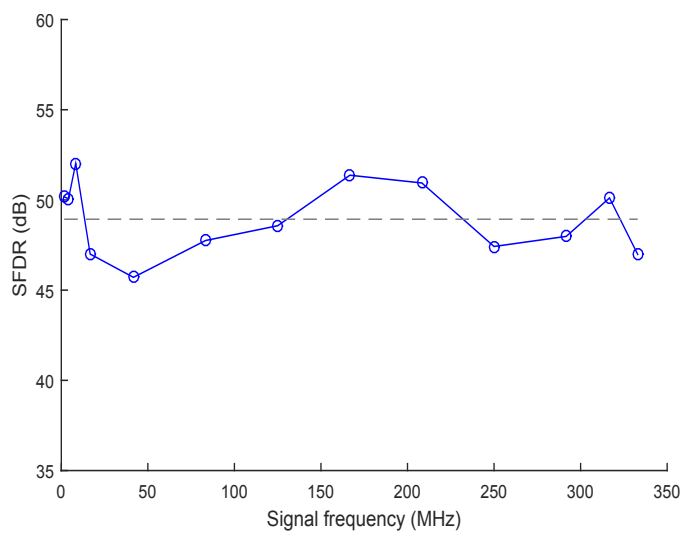
filtre de sortie fixe signifie que l'atténuation des composantes harmoniques d'ordre élevé sera réduite pour les fréquences de sortie inférieures à 166 MHz, tandis que la composante fondamentale sera atténuée pour les fréquences de sortie supérieures à 166 MHz.

En prenant en compte ces limitations inévitables, nous avons répété la procédure de test et d'étalonnage à différentes fréquences d'horloge allant de 20 MHz à 4 GHz pour générer des signaux sinusoïdaux à partir de 1 MHz à 333 MHz. Les figures ?? A et figure A.35.b montrent respectivement le SFDR et le THD après calibration, en fonction de la fréquence de sortie générée. On peut noter que les chiffres de linéarité obtenus montrent un comportement relativement constant dans la gamme de fréquences considérée, avec un SFDR moyen de 49 dB et un THD moyen de -45 dB.

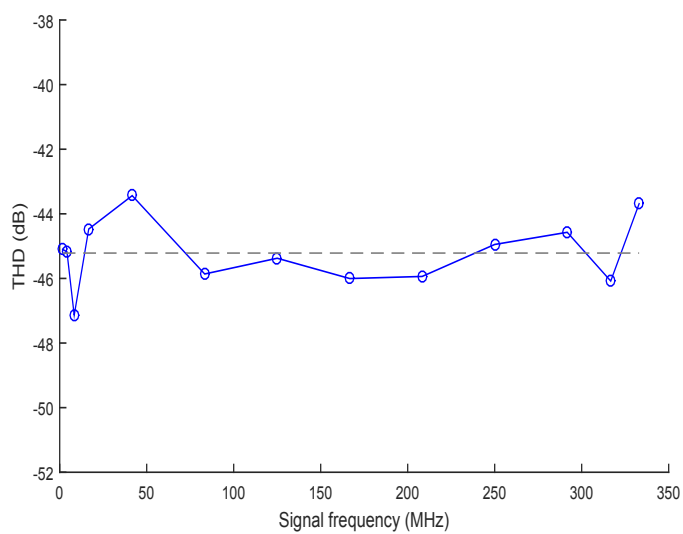
A.5.6 Discussion des résultats

Afin de mieux comprendre la linéarité du prototype fabriqué, la figure A.36 montre un diagramme en boîte à moustaches de la puissance mesurée pour les dix premières composantes de distorsion harmonique du signal sinusoïdal généré, sur la fréquence considérée intervalle. Il est clair que les composantes de distorsion harmonique sont centrées autour de -50 dBc par rapport au fondamental, à peine au-dessus du bruit de fond de l'analyseur de spectre. Il est également clair que la dispersion du composant harmonique du septième ordre est supérieure à la dispersion des autres composants. Ceci est une conséquence de la résolution limitée des sources DC utilisées pour l'étalonnage, ce qui ne nous permet pas d'annuler complètement le septième composant harmonique.

Il est possible de mieux comprendre les mécanismes de distorsion limitant les performances du générateur en analysant le THD et le SFDR partiels calculés alternativement avec les composantes harmoniques paires et impaires. Ainsi, dans la Fig. A.37. A, nous montrons le SFDR mesuré dans la plage de fréquences considérée, ainsi que le SFDR partiel dû à des composants pairs, $SFDR_{pair}$, et le SFDR partiel dû à des composants harmoniques impaires, $SFDR_{impair}$. De manière équivalente, la Fig. A.37. B montre le THD dans la plage de fréquences considérée, ainsi que les chiffres partiels THD_{pair} et THD_{impair} . Il est clair que pour les basses fréquences, en dessous de ~ 150 MHz, la linéarité observée est principalement limitée par les composantes harmoniques impaires dues à une annulation harmonique incomplète en raison de la résolution limitée des sources à courant continu. Pour les fréquences de sortie plus élevées, les erreurs de synchronisation dues à des déséquilibres de circuit et à des non-idéalités de l'horloge externe entraînent une dégradation du 50% du cycle de service des ondes carrées numériques et peut également affecter l'équilibre entre les sorties différentielles, ces deux effets entraînant une distorsion harmonique d'ordre pair.



(a)



(b)

FIGURE A.35 : (a) SFDR ; (b) THD ; variation Vs fréquence.

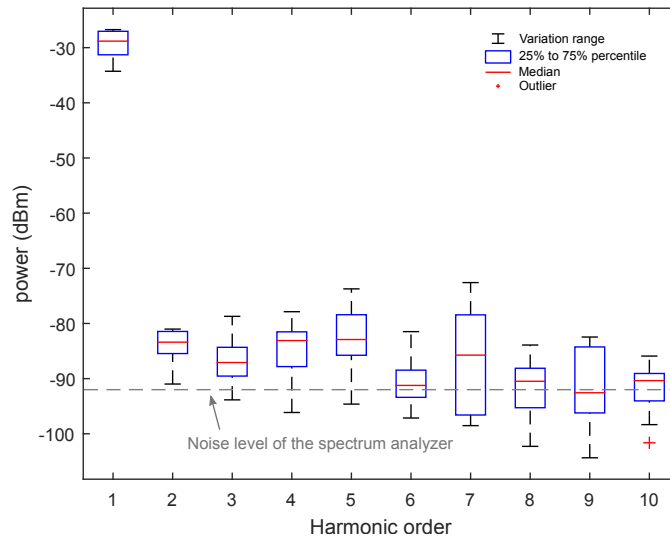


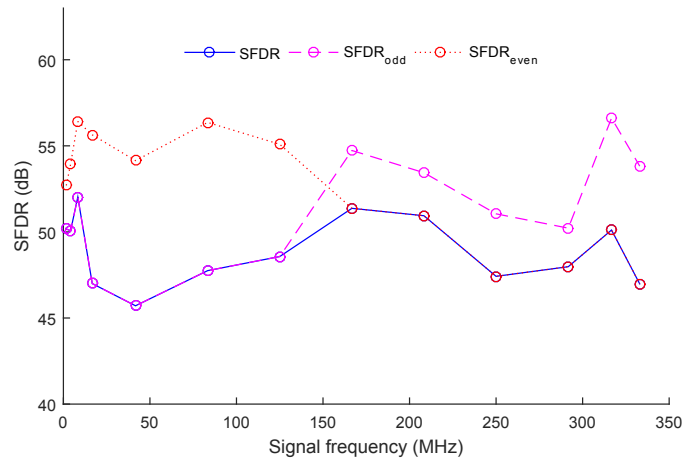
FIGURE A.36 : Variation de la puissance des harmoniques.

A.6 Conclusion

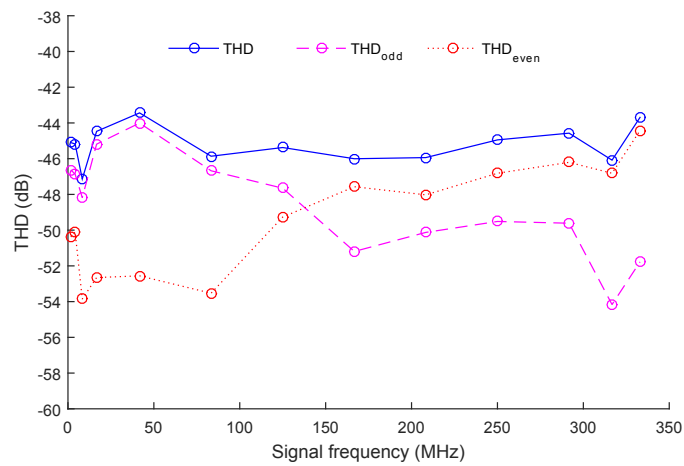
A. Nous avons exploré quatre stratégies d’annulation d’harmoniques différentes pouvant conduire à la conception de générateurs de signaux sinusoïdaux efficaces et robustes basés sur des ressources essentiellement numériques. Les solutions d’annulation d’harmoniques proposées simplifient la conception des différents facteurs de pondération de la balance dans le générateur, qui constituent généralement un facteur limitant essentiel pour l’efficacité de l’annulation des harmoniques.

B. Nous avons proposé une architecture complète au niveau des transistors pour un générateur utilisant une technique d’annulation d’harmoniques avec un poids d’échelle irrationnel. Le générateur est basé sur un registre à décalage circulaire qui fournit un ensemble d’ondes carrées à retard temporel ainsi qu’un convertisseur numérique-analogique simplifié. Une stratégie de calibrage simple a été proposée pour garantir l’efficacité de l’annulation des harmoniques. Les résultats de la simulation électrique en cours de traitement et les variations de mésappariement montrent une linéarité du stimulus généré meilleure que $THD = -67 \text{ dB}$ et $SFDR = 70 \text{ dB}$, cependant, la simulation post-layout montre un THD de -58 dB et un SFDR de 60 dB à 166 MHz .

C. Ce prototype a été caractérisé en laboratoire et les résultats montrent que le signal sinusoïdal généré par le générateur calibré présente un THD de -45 dB et un SFDR de 52 dB à 166.67 MHz , avec une amélioration de 10 dB par rapport au générateur non étalonné. Les résultats expérimentaux montrent également que le générateur calibré présente des performances assez constantes dans une plage de fréquences 1 MHz à 333 MHz , avec une fréquence d’horloge comprise entre



(a)



(b)

FIGURE A.37 : Impact des harmoniques impaires et paires sur : (a) le SFDR; (b) THD.

20 *MHz* et 4 *GHz*. La moyenne obtenue de THD est d'environ -45 *dB* et la moyenne du SFDR est d'environ 50 *dB*.

List of publications

– Journal:

[1] H. Malloug, M. J. Barragan and S. Mir, "Practical harmonic cancellation techniques for the on-chip implementation of sinusoidal signal generators for mixed-signal BIST applications," *Journal of Electronic Testing: Theory and Applications*, Springer, 2018, 34(3), 263-279.

– International conferences and workshops:

[2] H. Malloug, M. J. Barragan, S. Mir and H. L. Gall, "Harmonic cancellation strategies for on-chip sinusoidal signal generation using digital resources," 2017 International Mixed Signals Testing Workshop (IMSTW), Thessaloniki, Greece, 2017, pp. 1-6.

[3] H. Malloug, M. J. Barragan, S. Mir, L. Bastères and H. Le Gall, "Design of a sinusoidal signal generator with calibrated harmonic cancellation for mixed-signal BIST in a 28 nm FDSOI technology," 2017 22nd IEEE European Test Symposium (ETS), Limassol, Cyprus, 2017, pp. 1-6.

[4] H. Malloug, M. J. Barragan, S. Mir, E. Simeu and H. Le-Gall, "Mostly-digital design of sinusoidal signal generators for mixed-signal BIST applications using harmonic cancellation," 2016 IEEE 21st International Mixed-Signal Testing Workshop (IMSTW), Sant Feliu de Guixols, Spain, 2016, pp. 1-6.

[5] H. Malloug, M. J. Barragan and S. Mir, "Evaluation of harmonic cancellation techniques for sinusoidal signal generation in mixed-signal BIST," 2015 20th International Mixed-Signal Testing Workshop (IMSTW), Paris, France, 2015, pp. 1-6.

[6] M. Portolan, M. Barragan, H. Malloug, S. Mir. "Interactive mixed-signal testing through 1687," 2016 First International Test Standards Application Workshop (TESTA), Amsterdam, Netherlands. 2016, pp. 1-2.

– Poster

[7] H. Malloug, M. J. Barragan and S. Mir, "Conception d'un générateur de signal sinusoïdal basé sur les techniques d'annulation d'harmonique en 28nm FDSOI," 2018 13ème Colloque du GDR SoC/SiP, Paris, France, 2018, pp. 1-2.

Bibliography

- [1] The International Technology Roadmap for Semiconductors, “Test and test equipment,” <http://www.itrs2.net/>, note = Online; 2009.
- [2] F. Poehl, F. Demmerle, J. Alt, and H. Obermeir, “Production test challenges for highly integrated mobile phone SOCs—A case study,” in *Test Symposium (ETS), 2010 15th IEEE European*. IEEE, 2010, pp. 17–22.
- [3] Dr. Handel Jones, International Business Strategies (IBS), “Whitepaper: Semiconductor Industry from 2015 to 2025,” <http://www.semi.org/en/node/57416>, note = Online; August 4, 2015.
- [4] K. Arabi, “Special session 6C: New topic mixed-signal test impact to SoC commercialization,” in *VLSI Test Symposium (VTS), 2010 28th*. IEEE, 2010, pp. 212–212.
- [5] “IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters,” *IEEE Std 1241-2010 (Revision of IEEE Std 1241-2000)*, pp. 1–139, Jan 2011.
- [6] E. H. Colpitts, “Oscillation generator,” 1927, uS Patent 1,624,537.
- [7] D. Chattopadhyay, *Electronics (fundamentals and applications)*. New Age International, 2006.
- [8] C. E. Wheatley III and D. N. Punch, “High dynamic range closed loop automatic gain control circuit,” 1992, US Patent 5,107,225.
- [9] M. Wien, “Messung der Inductionsconstanten mit dem optischen Telephon,” *Annalen der Physik*, vol. 280, pp. 689–712, 1891.
- [10] D. B. Cox, L. T. Lin, and R. S. Florek, “A real-time programmable switched-capacitor filter,” *IEEE Journal of Solid-State Circuits*, vol. 15, no. 6, pp. 972–977, 1980.

- [11] P. E. Fleischer, A. Ganesan, and K. R. Laker, "A switched capacitor oscillator with precision amplitude control and guaranteed start-up," *IEEE Journal of solid-state circuits*, vol. 20, no. 2, pp. 641–647, 1985.
- [12] S. W. Park, J. L. Ausín, F. Bahmani, and E. Sánchez-Sinencio, "Nonlinear shaping sc oscillator with enhanced linearity," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 11, pp. 2421–2431, 2007.
- [13] M. A. Dominguez, J. L. Ausín, J. Duque-Carillo, and G. Torelli, "A high-quality sine-wave oscillator for analog built-in self-testing," in *Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on*. IEEE, 2006, pp. 4–pp.
- [14] F. Bahmani and E. Sánchez-Sinencio, "Low THD bandpass-based oscillator using multilevel hard limiter," *IET Circuits, Devices & Systems*, vol. 1, no. 2, pp. 151–160, 2007.
- [15] J. Tierney, C. Rader, and B. Gold, "A digital frequency synthesizer," *IEEE Transactions on Audio and Electroacoustics*, vol. 19, no. 1, pp. 48–57, 1971.
- [16] H. T. Nicholas, H. Samueli, and B. Kim, "The optimization of direct digital frequency synthesizer performance in the presence of finite word length effects," in *Frequency Control Symposium, 1988., Proceedings of the 42nd Annual*. IEEE, 1988, pp. 357–363.
- [17] D. Guest, "Simplified data-transmission channel measurements," *Hewlett-Packard J*, vol. 26, no. 3, pp. 15–24, 1974.
- [18] D. A. Sunderland, R. A. Strauch, S. S. Wharfield, H. T. Peterson, and C. R. Cole, "CMOS/SOS frequency synthesizer LSI circuit for spread spectrum communications," *IEEE Journal of Solid-State Circuits*, vol. 19, no. 4, pp. 497–506, 1984.
- [19] K. A. Essenwanger and V. S. Reinhardt, "Sine output DDSs. A survey of the state of the art," in *Frequency Control Symposium, 1998. Proceedings of the 1998 IEEE International*. IEEE, 1998, pp. 370–378.
- [20] G. W. Kent and N.-H. Sheng, "A high purity, high speed direct digital synthesizer," in *Frequency Control Symposium, 1995. 49th., Proceedings of the 1995 IEEE International*. IEEE, 1995, pp. 207–211.
- [21] A. Bellaouar, M. Obrecht, A. Fahim, and M. Elmasry, "A low-power direct digital frequency synthesizer architecture for wireless communications," in *Custom Integrated Circuits, 1999. Proceedings of the IEEE 1999*. IEEE, 1999, pp. 593–596.

- [22] A. M. Eltawil and B. Daneshrad, "Piece-wise parabolic interpolation for direct digital frequency synthesis," in *Custom Integrated Circuits Conference, 2002. Proceedings of the IEEE 2002*. IEEE, 2002, pp. 401–404.
- [23] J. E. Volder, "The CORDIC trigonometric computing technique," *IRE Transactions on electronic computers*, no. 3, pp. 330–334, 1959.
- [24] A. Madisetti, A. Y. Kwentus, and A. N. Willson, "A 100-MHz, 16-b, direct digital frequency synthesizer with a 100-dBc spurious-free dynamic range," *IEEE Journal of solid-state circuits*, vol. 34, no. 8, pp. 1034–1043, 1999.
- [25] E. Antelo, J. Villalba, and E. L. Zapata, "A low-latency pipelined 2D and 3D CORDIC processors," *IEEE Transactions on Computers*, vol. 57, no. 3, pp. 404–417, 2008.
- [26] D. R. Moran, J. G. Menoyo, and J. L. J. Martin, "Digital frequency synthesizer based on two coprime moduli DDS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 12, pp. 1388–1392, 2006.
- [27] D. Rabijns, W. Van Moer, and G. Vandersteen, "Spectrally pure excitation signals: Only a dream?" *IEEE Transactions on Instrumentation and Measurement*, vol. 53, no. 5, pp. 1433–1440, 2004.
- [28] C. H. Bae, J. H. Ryu, and K. W. Lee, "Suppression of harmonic spikes in switching converter output using dithered sigma-delta modulation," in *Industry Applications Conference, 2001. Thirty-Sixth IAS Annual Meeting. Conference Record of the 2001 IEEE*, vol. 4. IEEE, 2001, pp. 2167–2174.
- [29] D. A. Lampasi, A. Moschitta, and P. Carbone, "Accurate digital synthesis of sinewaves," *IEEE Transactions on Instrumentation and Measurement*, vol. 57, no. 3, pp. 522–529, 2008.
- [30] B. Dufort and G. W. Roberts, "Optimized periodic sigma-delta bitstreams for analog signal generation," in *Circuits and Systems, 1997. Proceedings of the 40th Midwest Symposium on*, vol. 1. IEEE, 1997, pp. 289–292.
- [31] —, "Signal generation using periodic single and multi-bit sigma-delta modulated streams," in *Test Conference, 1997. Proceedings., International*. IEEE, 1997, pp. 396–405.
- [32] E. M. Hawrysh and G. W. Roberts, "An integration of memory-based analog signal generation into current DFT architectures," *IEEE Transactions on Instrumentation and Measurement*, vol. 47, no. 3, pp. 748–759, 1998.

- [33] B. Dufort and G. W. Roberts, "On-chip analog signal generation for mixed-signal built-in self-test," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 3, pp. 318–330, 1999.
- [34] G. Prenat, S. Mir, D. Vázquez, and L. Rolíndez, "A low-cost digital frequency testing approach for mixed-signal devices using $\Sigma\Delta$ modulation," *Microelectronics journal*, vol. 36, no. 12, pp. 1080–1090, 2005.
- [35] A. K. Lu, G. W. Roberts, and D. A. Johns, "A high-quality analog oscillator using oversampling D/A conversion techniques," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 41, no. 7, pp. 437–444, 1994.
- [36] H. Patangia and B. Zenone, "A programmable switched-capacitor sinewave generator," in *Circuits and Systems, 1994., Proceedings of the 37th Midwest Symposium on*, vol. 1. IEEE, 1994, pp. 165–168.
- [37] M. Mendez-Rivera, J. Silva-Martínez, and E. Sánchez-Sinencio, "On-chip spectrum analyzer for built-in testing analog ICs," in *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*, vol. 5. IEEE, 2002, pp. V–V.
- [38] J. Silva-Martinez and E. Sánchez-Sinencio, "Excess phase jitter cancellation method for SC relaxation oscillators," *IEEE Transactions on circuits and systems*, vol. 34, no. 6, pp. 695–700, 1987.
- [39] M. J. Barragán, D. Vázquez, and A. Rueda, "Analog sinewave signal generators for mixed-signal built-in test applications," *Journal of Electronic Testing*, vol. 27, no. 3, pp. 305–320, 2011.
- [40] —, "A BIST solution for frequency domain characterization of analog circuits," *Journal of Electronic Testing*, vol. 26, no. 4, pp. 429–441, 2010.
- [41] A. C. Davies, "Digital generation of low-frequency sine waves," *IEEE Transactions on Instrumentation and Measurement*, vol. 18, no. 2, pp. 97–105, 1969.
- [42] M. J. Barragan, G. Leger, D. Vazquez, and A. Rueda, "On-chip sinusoidal signal generation with harmonic cancelation for analog and mixed-signal bist applications," *Analog Integrated Circuits and Signal Processing*, vol. 82, no. 1, pp. 67–79, 2015.
- [43] B. K. Vasan, S. K. Sudani, D. J. Chen, and R. L. Geiger, "Low-distortion sine wave generation using a novel harmonic cancellation technique," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 5, pp. 1122–1134, 2013.

- [44] —, “Sinusoidal signal generation for production testing and BIST applications,” in *Circuits and Systems (ISCAS), 2012 IEEE International Symposium on*. IEEE, 2012, pp. 2601–2604.
- [45] M. M. Elsayed and E. Sanchez-Sinencio, “A low THD, low power, high output-swing time-mode-based tunable oscillator via digital harmonic-cancellation technique,” *IEEE Journal of Solid-State Circuits*, vol. 45, no. 5, pp. 1061–1071, 2010.
- [46] C. Shi and E. Sánchez-Sinencio, “150–850 MHz high-linearity sine-wave synthesizer architecture based on FIR filter approach and SFDR optimization,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 9, pp. 2227–2237, 2015.
- [47] —, “On-Chip Two-Tone Synthesizer Based on a Mixing-FIR Architecture,” *IEEE Journal of Solid-State Circuits*, 2017.
- [48] S. David-Grignot, A. Lamlih, V. Kerzerho, F. Azais, F. Soulier, S. Bernard, T. Rouyer, and S. Bonhommeau, “Analytical study of on-chip generations of analog sine-wave based on combined digital signals,” in *Mixed Signals Testing Workshop (IMSTW), 2017 International*. IEEE, 2017, pp. 1–5.
- [49] P. Aluthwala, N. Weste, A. Adams, T. Lehmann, and S. Parameswaran, “A simple digital architecture for a harmonic-cancelling sine-wave synthesizer,” in *Circuits and Systems (ISCAS), 2014 IEEE International Symposium on*. IEEE, 2014, pp. 2113–2116.
- [50] —, “Design of a digital harmonic-cancelling sine-wave synthesizer with 100 MHz output frequency, 43.5 dB SFDR, and 2.26 mW power,” in *Circuits and Systems (ISCAS), 2015 IEEE International Symposium on*. IEEE, 2015, pp. 3052–3055.
- [51] P. D. Aluthwala, N. Weste, A. Adams, T. Lehmann, and S. Parameswaran, “Partial dynamic element matching technique for digital-to-analog converters used for digital harmonic-cancelling sine-wave synthesis,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 2, pp. 296–309, 2017.
- [52] F. Abe, Y. Kobayashi, K. Sawada, K. Kato, O. Kobayashi, and H. Kobayashi, “Low-distortion signal generation for ADC testing,” in *Test Conference (ITC), 2014 IEEE International*. IEEE, 2014, pp. 1–10.
- [53] K. Wakabayashi, K. Kato, T. Yamada, O. Kobayashi, H. Kobayashi, F. Abe, and K. Niitsu, “Low-distortion sinewave generation method using arbitrary

- waveform generator,” *Journal of Electronic Testing*, vol. 28, no. 5, pp. 641–651, 2012.
- [54] H. Malloug, M. J. Barragan, S. Mir, E. Simeu, and H. Le-Gall, “Mostly-digital design of sinusoidal signal generators for mixed-signal BIST applications using harmonic cancellation,” in *Mixed-Signal Testing Workshop (IMSTW), 2016 IEEE 21st International*. IEEE, 2016, pp. 1–6.
- [55] H. Malloug, M. J. Barragan, S. Mir, L. Bastères, and b. p. y. o. Le Gall, Hervé, “Design of a sinusoidal signal generator with calibrated harmonic cancellation for mixed-signal BIST in a 28 nm FDSOI technology.”
- [56] K. Laker and W. Sansen, “Design of analog integrated circuits and systems,” 1994.
- [57] M. Brownlow, G. Cairns, C. Dachs, Y. Kubota, H. Washio, and H. Yamashita, “6-bit multiresolution digital-to-analog converter for low-temperature polysilicon digital drivers,” in *Flat Panel Display Technology and Display Metrology II*, vol. 4295. International Society for Optics and Photonics, 2001, pp. 85–95.
- [58] H. D. Truong and C. M. Lin, “Clock generator with programmable non-overlapping clock edge capability,” Aug. 22 1995, uS Patent 5,444,405.

TITRE

CONCEPTION DE GENERATEURS SINUSOÏDAUX EMBARQUES POUR L'AUTO-TEST DES CIRCUITS MIXTES

Résumé : Développer un générateur de signal analogique efficace est un élément clés pour les BIST des circuits analogiques et mixtes afin de produire le stimulus de test approprié, et remplacer les générateurs de signaux externes coûteux dans les protocoles de standard de test fonctionnel analogique et mixte. Dans cette optique, nous présentons dans cette thèse des stratégies différentes de génération de signal sinusoïdal, basées sur les techniques d'annulation d'harmonique, pour le design d'un synthétiseur embarqué de signal sinusoïdal à haute fréquence. Les générateurs proposés utilisent des circuits numériques pour produire un ensemble de signaux carrés déphasés. Ces signaux carrés sont pondérés et combinés en appliquant différentes stratégies d'annulation d'harmonique dans un convertisseur numérique-analogique simplifié. Le générateur sélectionné permet d'annuler toutes les harmoniques en dessous de la 11^{ème}. De plus, une simple stratégie de calibration a été conçue pour compenser l'effet de mismatch et de la variation de process de fabrication sur l'efficacité de la technique d'annulation d'harmonique. La simplicité du circuit rend cette approche adaptable pour le BIST des circuits intégrés analogique et mixte. Les modèles comportementaux, les simulations électriques d'un design en 28 nm FDSOI et les résultats expérimentaux sont fournis pour valider la fonctionnalité du générateur proposé. Les résultats obtenus montrent des performances du circuit calibré autour de 52 dB de SFDR pour un signal généré à 166 MHz.

Mots clés : Générateur de signal sinusoïdal, annulation des harmoniques, test-intégré, 28 nm FDSOI

TITLE

DESIGN OF EMBEDDED SINUSOIDAL SIGNAL GENERATORS FOR MIXED SIGNAL BUILT-IN SELF-TEST

Abstract: One of the main key points to enable mixed-signal BIST solutions is the development of efficient on-chip analog signal generators that can provide appropriate test stimuli and replace costly external signal generators in standard analog and mixed-signal functional test protocols. In this line, we present in this thesis different sinewave generation strategies based on harmonic cancellation techniques to design a high-frequency on-chip sinusoidal synthesizer. The proposed generators employ digital hardware to provide a set of phase-shifted digital square-wave signals. These square-wave signals are scaled and combined using different harmonic cancellation strategies in a simplified current-steering DAC. The selected generator allows the cancellation of all harmonic components up to the eleventh. Additionally, a simple calibration strategy has been devised to compensate the impact of process variations and mismatch on the effectiveness of the harmonic cancellation. The simplicity of the circuitry makes this approach suitable for mixed-signal BIST applications. Accurate behavioral models, electrical simulations of a 28 nm FDSOI design and experimental results are provided to validate the functionality of the proposed signal generator. Obtained results show a calibrated performance around 52 dB of SFDR for a generated sinusoidal signal at 166 MHz.

Keywords: sinusoidal signal generator, harmonic cancellation, built-in self-test, 28 nm FDSOI

