



Power amplifier design for 5G applications in 28nm FD-SOI technology

Florent Torres

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THÈSE PRÉSENTÉE
POUR OBTENIR LE GRADE DE
DOCTEUR DE
L'UNIVERSITÉ DE BORDEAUX

ÉCOLE DOCTORALE DES SCIENCES PHYSIQUES ET DE L'INGÉNIEUR
SPÉCIALITÉ ÉLECTRONIQUE

Par Florent TORRES

**Power Amplifier Design for 5G Applications
in 28nm FD-SOI Technology**

Sous la direction de : Eric KERHERVE & Andreia CATHELIN

Soutenue le 18 mai 2018

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Titre : Développement d'un amplificateur de puissance pour des applications 5G en technologie 28nm FD-SOI

Résumé : Le futur réseau mobile 5G est prévu pour être déployé à partir de 2020, dans un contexte d'évolution exponentielle du marché de la téléphonie mobile et du volume de données échangées. La 5G servira de levier à des applications révolutionnaires qui permettront l'émergence du monde connecté. Dans ce but, plusieurs spécifications pour le réseau sont attendues même si aucun standard n'est encore défini et notamment une faible latence, une consommation d'énergie réduite et un haut débit de données. Les bandes de fréquences traditionnellement utilisées dans les réseaux mobiles ne permettront pas d'atteindre les performances visées et plusieurs bandes de fréquences millimétriques sont à l'étude pour créer un spectre complémentaire. Cependant, ces bandes de fréquence millimétriques souffrent d'une forte atténuation dans l'air et dans les matériaux de construction. Plusieurs techniques vont être implémentées pour outrepasser ces limitations dans les zones urbaines denses comme le backhauling, FD-MIMO et beamforming phased array. Ces techniques entraînent l'utilisation d'un grand nombre de transmetteurs dans les stations de bases et dans les dispositifs de l'utilisateur final. La technologie CMOS offre d'indéniables avantages pour ce marché de masse tandis que la technologie FD-SOI offre des performances et fonctionnalités additionnelles. L'amplificateur de puissance est le bloc le plus critique à concevoir dans un transmetteur et consomme le plus d'énergie. Afin d'adresser les challenges de la 5G, plusieurs spécifications concernant la puissance consommée, la linéarité et le rendement sont attendues. Les variations de l'environnement dans les beamforming phased array et le contexte industriel nécessitent des topologies robustes alors qu'une reconfigurabilité au niveau de l'amplificateur de puissance est bénéfique dans le cas de circuits adaptatifs. Cette thèse adresse ces challenges en explorant la conception d'un amplificateur de puissance reconfigurable et robuste pour des applications 5G en intégrant des techniques de design spécifiques et en mettant en avant les avantages de la technologie 28nm FD-SOI pour la reconfigurabilité.

Title: Design of power amplifier for 5G applications in 28nm FD-SOI technology

Abstract: The 5G future mobile network is planned to be deployed from 2020, in a context of exponential mobile market and exchanged data volume evolution. The 5G will leverage revolutionary applications for the advent of the connected world. For this purpose, several network specifications are expected notably low latency, reduced power consumption and high data-rates even if no standard is yet defined. The frequency bands traditionally used for mobile networks will not permit the needed performances and several mmW frequency bands are under study to create a complementary frequency spectrum. However, these mmW frequency bands suffer from large attenuation in building material and in free-space. Therefore, several techniques will be implemented to tackle these limitations in dense urban areas like backhauling, FD-MIMO and beamforming phased array. This is leading to a large number of transceivers for base stations and end-user devices. CMOS technology offers undeniable advantages for this mass market while FD-SOI technology offers additional features and performances. The power amplifier is the most critical block to design in a transceiver and is also the most power consuming. To address the 5G challenges, several specifications concerning power consumption, linearity and efficiency are expected. The environment variations in beamforming phased array and the industrial context drive the need for robust topologies while power amplifier reconfigurability is benefic in a context of adaptive circuits. This thesis addresses these challenges by exploring the conception of a robust and reconfigurable power amplifier targeting 5G applications while integrating specific design techniques and taking advantage of 28nm FD-SOI CMOS technology features for reconfigurability purposes.

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In memory of my Dad,

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General Introduction

We are at the dawn of a revolution in the telecommunication industry. The next generation of mobile network, the 5G, is planned to be deployed in 2020 and contrary to its predecessors it will not be a mobile-centroid network. Therefore, challenging specifications are expected to leverage new applications that will connect people, things, and the world. No standard is available before 2019 but we already know that to achieve the targeted specifications, mmW frequency bands allocation will be necessary. To overcome these high frequencies limits and leverage 5G, new design techniques will be implemented at base stations and end-user devices. The telecommunication industry is actually working on transceivers for mmW 5G and while GaAs, GaN and SiGe technologies have been used for mobile communications, the targeted mass market drives the need for high performances and low-cost integration that FD-SOI CMOS technology can offer.

In any transceiver, the power amplifier design is challenging. In deep sub-micron processes for telecommunication field at mmW frequencies, this is a critical block that has to be designed carefully. In addition, the 5G specifications impose challenging requirements at power amplifier level. This CIFRE thesis, realized in the frame of the ST-IMS common laboratory is targeting several goals:

- The specifications for power amplifier design featuring state of the art performances around 30GHz to address the 5G challenges.
- A power amplifier design solution meeting these specifications and implemented in 28nm FD-SOI technology.
- The exploration of the 28nm FD-SOI technology for RF and mmW applications, with industrial implementation margins.

This manuscript is composed of three chapters.

The first chapter is defining the context of this thesis and presents the mobile telecommunications market evolutions leading to the 5G emergence. To define the power amplifier specifications for 5G leveraged applications, we provide complete overviews of the expected frequency spectrum, potential modulations, and technological solutions to enable high-data rates in dense urban areas. In addition, important power amplifier parameters and performances are defined. The 5G mmW PA challenges are then discussed. A complete state of the art shows the PA design trends for the frequency of interest and highlights the actual limitations that this thesis target to overcome. Therefore, at the end of this first chapter, the thesis goals concerning performances are clearly exposed.

The second chapter presents a design flow for mmW 28nm FD-SOI power amplifiers. The specificities of this technology and the reconfigurability offered by the body-bias capability are discussed.

Then the possible overall PA architectures and amplification stages topologies are exposed. While general mmW impedance matching, stability, and design techniques enhancement are provided, this technology requires specific passive design approach. For this purpose, a specific model for transformer design is proposed. EM simulation tools optimization for fast and accurate prototyping is also discussed to complete a step-by-step design flow and give directions to designers. Indeed, accurate EM simulations in deep sub-micron technologies at high frequencies is mandatory and time-consuming due to the design elements small dimensions.

The third chapter describes the design and measurements of a balanced power amplifier targeting the 5G challenges in 28nm FD-SOI CMOS process and following the design flow defined in Chapter II. It exposes the design and layout choices, optimizations and margins for a robust integration with gain reconfigurability. The balanced topology choice, providing robustness to output antenna impedance variations, and its implementation are explained. The power-stage is featuring the first reconfigurable cascode implemented in 28nm FD-SOI. This reconfigurability achieves continuous wide range fine gain tuning and dynamic class switching. An output load impedance determination strategy is explored to avoid the performances degradation generally induced by dynamic class switching. On-wafer probing measurements have been conducted exhibiting state of the art level performances over a 5G frequency range. Robustness to temperature ranges up to 125°C and local process variability is also explored. A comparison with the state of the art is provided. This power amplifier has demonstrated the best in class ITRS FOM over the targeted frequency range. Finally, a novel reconfigurable and wideband design for 90° hybrid coupler is explored for future works. This manuscript is concluded by research perspectives for balanced power amplifiers architectures reducing multi-band transceivers complexity and costs by using this new coupler design.

Chapter I: The Road to 5G Power Amplifier Design

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Chapter I: The Road to 5G Power Amplifier Design

I.1 5G: Future global wireless network

I.1.1 Generalities

The mobile communication revolution started in the early 1980's with the first Motorola DynaTAC mobile phone. At that time, the communication was analogic and the mobile phone was only used to phone. This was the first generation of mobile network, the 1G, paving the way for the future of telecommunications. The next decades have seen the apparition of new usages and new mobile network generations. With the 2G, using GSM, GPRS, EDGE and CDMA standards, this is the beginning of text messages and early mobile "Internet" connection. With the 3G in the 2000's, the UMTS/HSPA/CDMA2000 standards leveraged multimedia usages. It was possible to browse the World Wide Web, send emails, stream music, send videos thanks to way higher data-rates compared to the previous generation. The first smartphones are appearing, diversifying the usages. However low data-rates around 3.1Mbps were reached in 3G. This exponential multimedia usage drove the need for higher data-rates. The phones are now smart and multitask, the 4G is birthed, leveraged by LTE and then LTE-Advanced standards. This is the current mobile network that we use in our everyday life.

The smartphone has entered our lives and from this time the mobile market presents an uninterrupted growth. In their mobility report, the analysts from Ericsson [ERI15] are making projections about the market evolutions concerning the broadband mobile subscriptions. An evolution of more than +110% in 2020 compared to 2015 is expected, with more than 7 billion broadband mobile subscriptions all over the world, leveraged by the emergence of smartphone in Asian countries. Meanwhile, the analysts from Cisco [CIS16], are expecting more than 11 billion mobile network connected objects in 2020 and more than 24 billion IP network connected objects in 2019. For both cases the part of smartphones and machine-to-machine (M2M) connections in these numbers is the highest. The evolution of the smartphone market and the democratization of high definition mobile video streaming will drive an explosion of the data traffic, with a 10 times higher monthly data-traffic level in 2020 compared to 2015. The emergence of the connected world with the Internet Of Things (IOT) explains the increasing number of M2M connections. The 5G infrastructure Public and Private Partnership [5GPPP] expects the emergence of the connected world to *"connect over 7 trillion wireless devices serving over 7 billion people"*. This mobile market evolution is illustrated in Figure I.1.1.

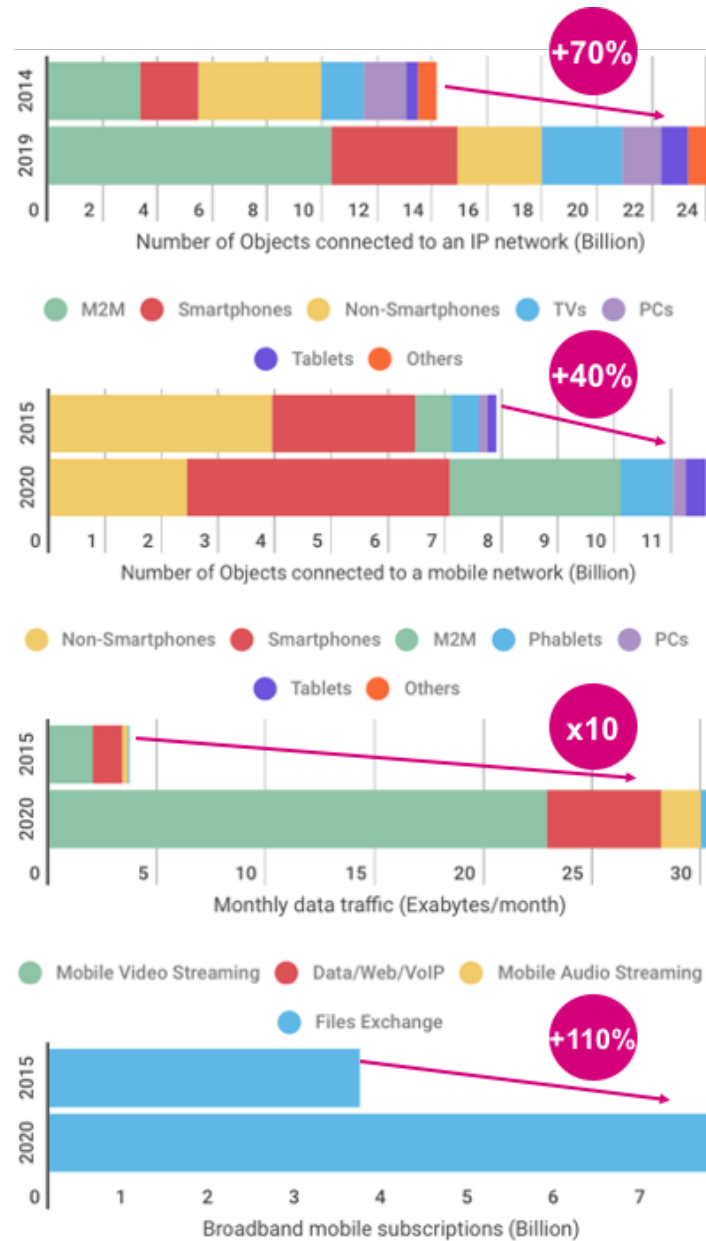


Figure I.1.1: Mobile telecommunications market 2014-2020 (data sources: [ERI15], [CIS16])

Furthermore, in the future connected world, a real revolution concerning the usages is planned. Everything and everybody will be connected, anywhere, anytime. The transportations become smart and safer with autonomous vehicles and transportation networks monitoring, optimization and security. The City becomes smart, safer. The flux and resources are monitored and managed thanks to the IOT with for example drinking water constant and automated quality check. The houses become connected too, allowing higher safety, a better resources management and is easier to use thanks to home automation. Furthermore, the industry will be connected too and the IOT will play an important role for that. Virtual and augmented reality will

open the way for new entertainment and business opportunities. These technologies will also allow the E-Health era with remote surgery, real-time remote patient monitoring. These are just some examples of the endless capabilities offered by the connected world.

The emergence of these new usages drives the need to rethink the mobile network actually centered on the smartphone usage and to propose a new network architecture, interoperable with existing networks to enable this connected world. As Nokia stated *“Driven by the enormous increase in mobile data traffic and flourishing user demands, we need to look beyond 4G”*. This is in this context that the 5G, the next generation of mobile network is emerging, with a first deployment planned for 2020.

While no standard is yet available, the expected usages are drawing the contours of needed 5G network specifications [AND14] and are discussed in the following paragraph.

In fact, with the huge increase of data usage, higher data-rates are expected with around 10Gbps downlink speed to allow ultra-HD video streaming and instant access to any content, making the Internet more tactile [FET14]. This notion of real-time tactile Internet [ITU14] is also extremely important for critical applications such as autonomous transportations and remote surgery. For these applications, a maximum system latency of 1ms is expected. The huge deployment of IOT with wireless sensors networks is driving the need for low power usages with battery lifetime of more than 10 years to be efficient. Another important point is the network ubiquity, leading to a network coverage 1000 times higher than in 2010 for constant quality [PIE15] and reliability of service for the user. Finally, while a collective awareness about environment and natural resources preservation is taking place, a decrease by 90% of the 5G network energy consumption is expected, limiting both operating costs and environmental impact. These specifications are summarized in the Figure I.1.2. It is noticeable that these specifications are not fixed and will depend on the different use-cases.

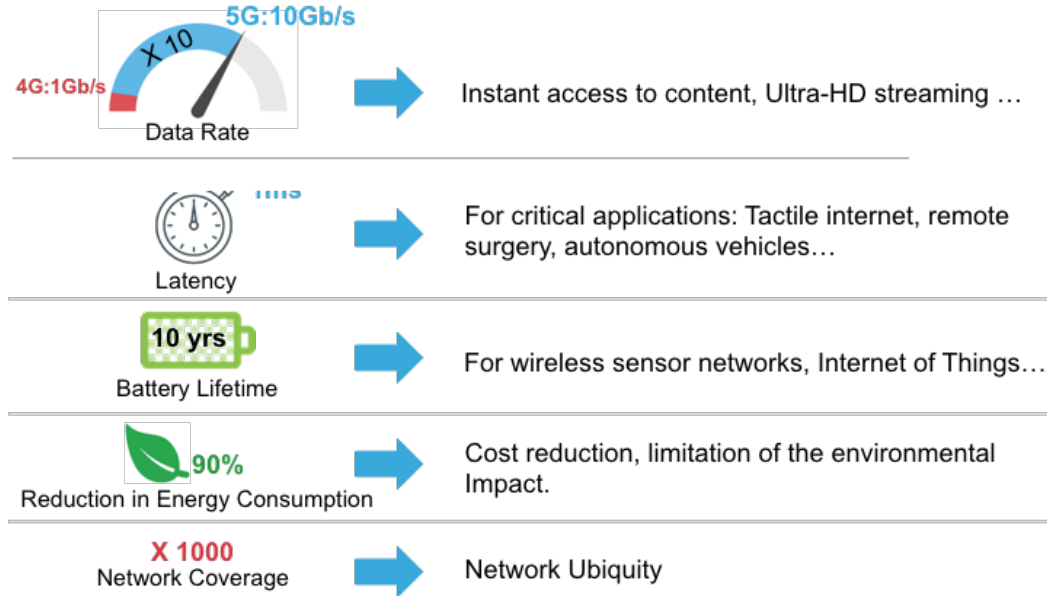


Figure I.1.2: 5G expected specifications (may vary depending on the use-case)

I.1.2 Frequency considerations

The past and actual mobile network generations are using several frequency bands depending on the region of the world, managed by the International Communications Union. Traditionally, the frequency bands allocated for mobile networks are located under 3.6GHz. These frequencies are beneficial in term of signal propagation. This is easily illustrated by the free-space path loss formula (I-1) and (I-2), derived from Friis equation [FRI46], where higher wavelength λ is leading to lower attenuation in free space.

$$Attenuation = \left(\frac{4\pi \cdot d}{\lambda} \right)^2 \quad (I-1)$$

$$Attenuation (dB) = 20 \log \left(\frac{4\pi \cdot d}{\lambda} \right) \quad (I-2)$$

These long distance achievable communications made the frequency bands under 3.6GHz very popular throughout the years for multiple applications and this is leading now to a spectral congestion. This issue is sometimes referred as “beachfront effect” and the crowded sub-3.6GHz spectrum cannot handle the needs of 5G network [AND14].

Furthermore, these frequency bands offer a limited bandwidth, incompatible with the targeted data-rates. In fact, the relation between channel capacity C (the maximum achievable data-rate) and bandwidth in a noiseless channel is given by the Nyquist formula (I-3) with M the number of signal levels and BW the bandwidth in Hz. It is noticeable that higher bandwidth is leading to higher achievable data-rate.

$$C(bps) = 2 \cdot BW \cdot \log_2(M) \quad (I-3)$$

The same assessment can be done regarding the Shannon-Hartley formula (I-4) from [SHA49], where the channel capacity C is function of the bandwidth and SNR (Signal-to-Noise Ratio) in a noisy channel.

$$C(bps) = BW \cdot \log_2(1 + SNR) \quad (I-4)$$

The conventional sub-3.6GHz spectrum is not sufficient to leverage 5G and a complementary spectrum is needed. The unlicensed frequency band around 5GHz is a solution but will not be sufficient to achieve the required high data-rates.

Therefore, a complementary spectrum in the mmW frequencies appears as a good solution to overcome these limits. In fact, wide frequency bands are available, allowing high data-rates. However, these bands suffer from strong attenuation in free space and several mmW frequency bands suffer from air attenuation as they correspond to peak absorption of O_2 (60GHz) and H_2O (23GHz) [UKT188]. The atmospheric attenuation at sea level in function of the frequency is available in Figure I.1.3 from [WEL09].

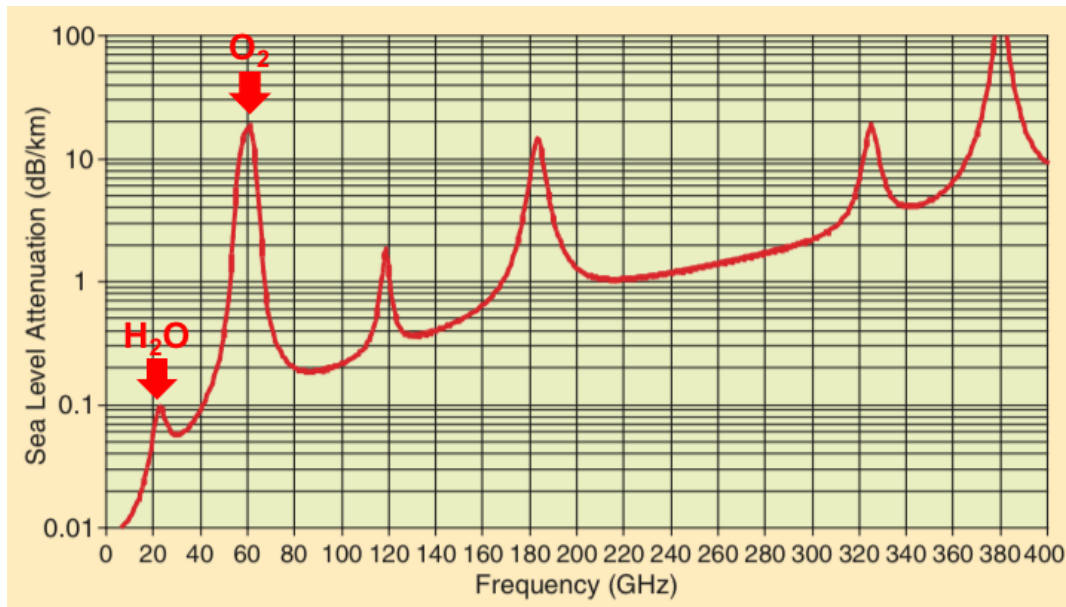


Figure I.1.3: Atmospheric attenuation versus frequency (based on [WEL09])

This strong attenuation made the mmW frequencies unsuitable for mobile communications and so these bands are free from any spectral congestion issue. They are ideal to leverage 5G as recent technology enhancements can overcome the attenuation [RAP13] and are discussed in the following section.

No standard for 5G will emerge before 2019 during the World Radiocommunication Conference (WRC-19) organized by the International Communications Union (ITU) and so no mmW frequency spectrum is yet allocated for 5G at this day. However, several mmW frequency bands are under studies by the 5G industrial actors since ITU WRC-15 conference [WRC15]. The expected 5G frequency spectrum is summarized in Figure I.1.4.

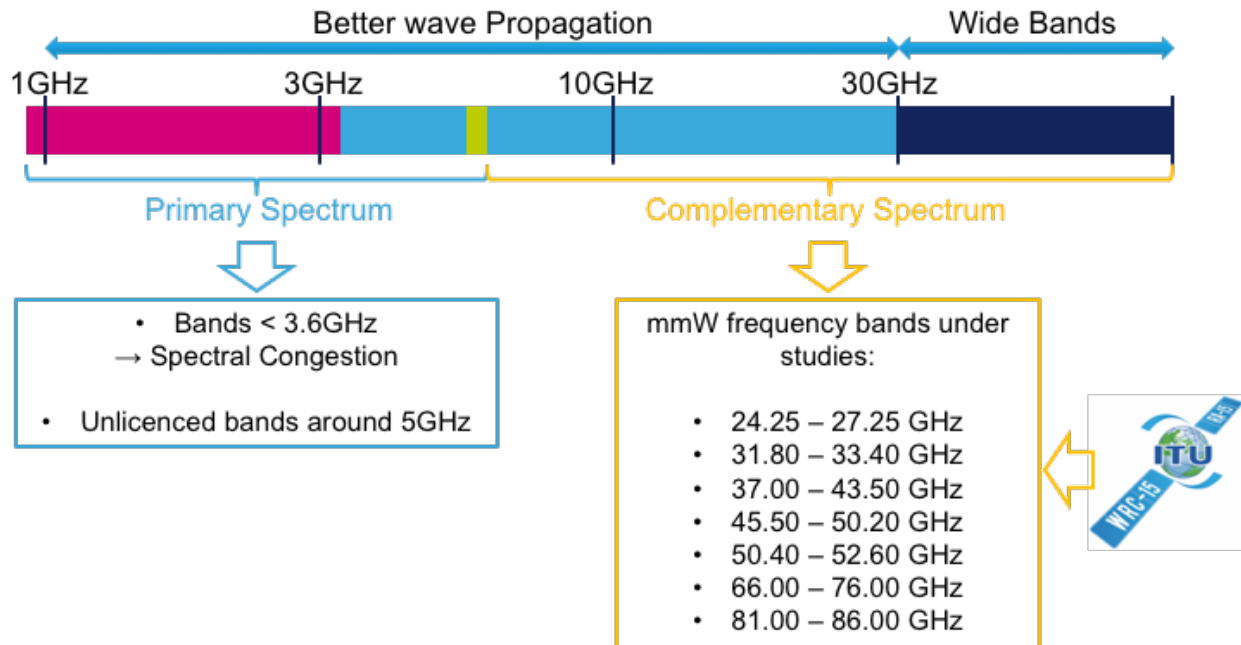


Figure I.1.4: 5G expected frequency spectrum

I.1.3 Technical solutions to leverage 5G

As we expose previously, one of the main challenges of 5G is to achieve high data-rates and network coverage even in dense urban areas.

In dense urban areas, the mmW frequencies used to achieve high data-rates are suffering from natural path-loss attenuation and atmospheric peak absorption as we stated previously but also from the attenuation in the different materials encountered in this environment. Several material attenuation values are available in Figure I.1.5 [GLO15] and Figure I.1.6 [NOK16].

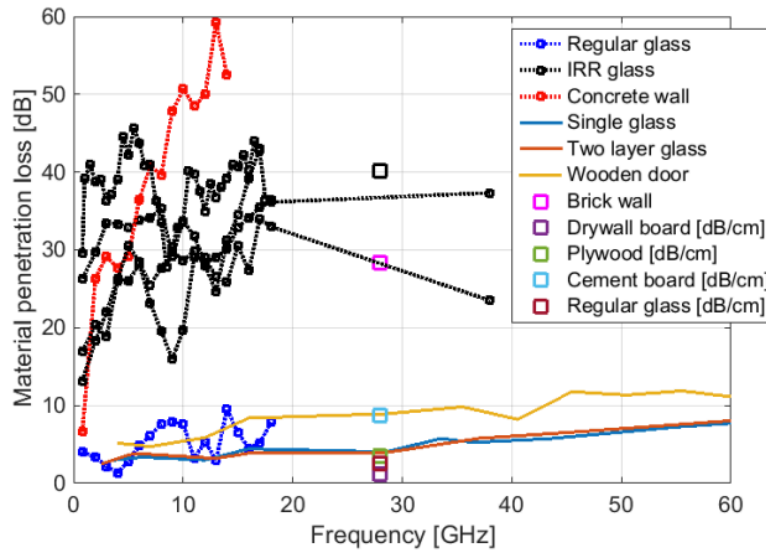


Figure I.1.5: Penetration losses in several materials depending on frequency [GLO15]

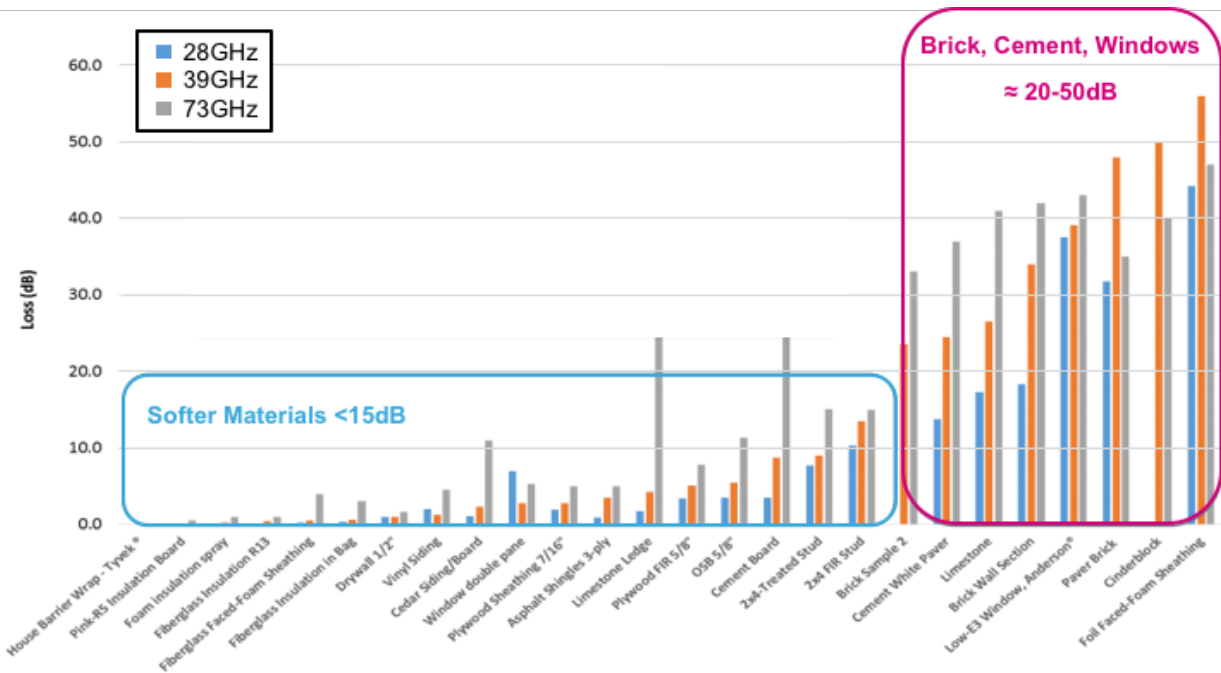


Figure I.1.6: Losses induced by material penetration at 28GHz, 39GHz and 73GHz [NOK16]

To overcome this issue and allow a higher network capability, the densification of active nodes is a solution but is not the only solution under study. Several technical solutions are studied from the use of small-cells [LAY14] and backhaul [TAO15] to massive MIMO (multiple-input multiple-output) [GAO15] and adaptive beamforming [CHE16]. This section presents a brief overview of the technical solutions that can leverage 5G.

The cell-scaling is fundamental for 5G as it allows several coexistent network layers depending on the environment. The use of small-cells architectures (micro, nano and femto cells) in addition to macro-cells will allow a significant increase in data-rates and efficiency by allowing short range communications and base station complement in dense urban areas with frequency re-use and limited power consumption. The cell dimensioning and the use-case scenario differ regarding the environment and while the small-cells will be advantageous in urban area it will have no interest in rural areas where macro-cells are more adapted. The cell dimensioning and the characteristics concerning power, parallel device number and range are available in Table I.1.1 and illustrated in Figure I.1.7. The characteristics of small-cells communication make the mmW frequencies totally suitable in this case.

	Range (radius, km)	Number of users (simultaneous)	Output power (W)	Locations
Macro-cell	8 to 30	>2000	10 to >50	Outdoor
Micro-cell	0.2 to 2	100 to 2000	1 to 10	Indoor/Outdoor
Pico-cell	0.1 to 0.2	30 to 100	0.25 to 1	Indoor/Outdoor
Femto-cell	0.01 to 0.1	1 to 30	0.001 to 0.25	Indoor

Table I.1.1: Cell dimensioning and characteristics (data source: [QOR17])

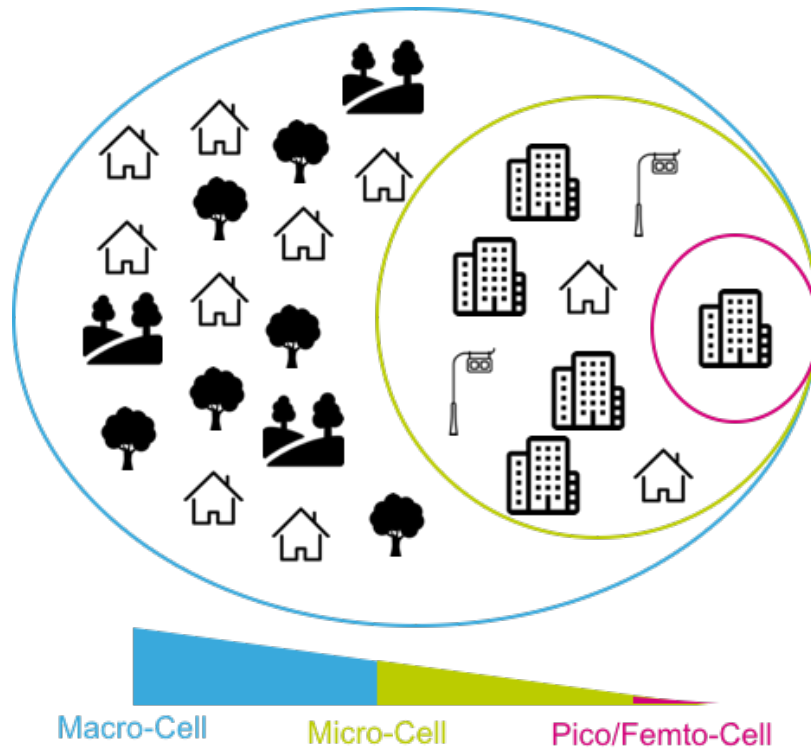


Figure I.1.7: Cell-dimensioning illustration

The connection between small-cells is the principle of backhaul. It consists of very short, high data-rates and high capacity signal bouncing in space. With a smart implementation of small-

cells using backhaul in a city (for example in traffic lights or floor lamps), the backhauling can provide high-speed data link at mmW frequencies by avoiding the losses encountered in a base-station-to-end-user direct communication through buildings and other obstacles. It allows multipath possibilities, base station decluttering and ensures a constant quality of service even in case of several nodes failures.

However, base station level optimization is also needed to address the 5G challenges. The concept of Massive MIMO consists in the implementation of large antennas arrays in base stations to allow a large number of simultaneous connections of spatially separated devices with the same quality of service. This technique allows spectral efficiency enhancement without base station densification. A better energy efficiency is also expected as large antenna arrays gain allows lower transmission power levels. The Figure I.1.8 illustrates the concept of Massive MIMO.

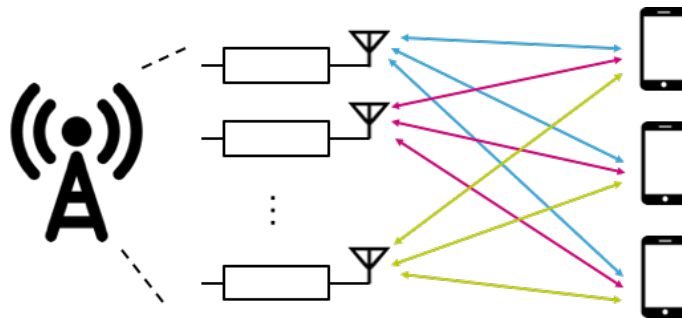


Figure I.1.8: Massive-MIMO concept

Beamforming is also a technology expected to leverage 5G conjointly with Massive MIMO. Beamforming is a technique actually used in defense and satellites applications. It consists on the combination of signal in an antenna array to electrically orient a beam without needing any antenna mechanical movement, enabling higher reliability of systems. In a beamforming array, composed by N amplification cells, a phase shift is induced by phase shifter in each amplification path, to dynamically, quasi-instantaneously and spatially control the beam orientation and so concentrate the transmitted power to a desired position. This principle is illustrated in Figure I.1.9.

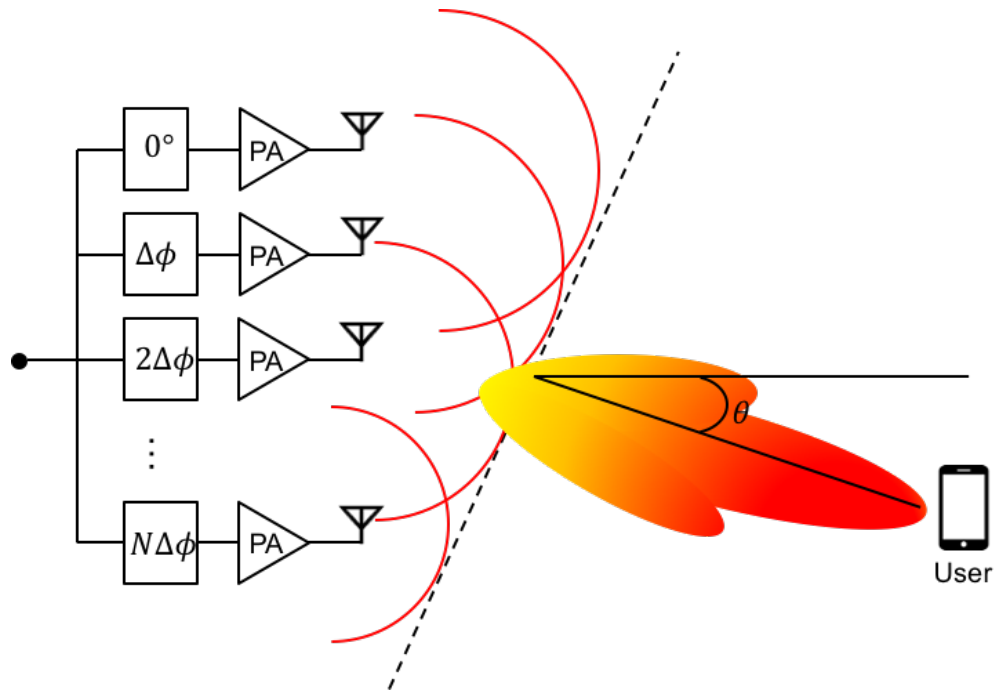


Figure I.1.9: Beamforming concept

Furthermore, the use of multiple amplification paths in base station for beamforming is interesting in term of reliability of service. If one path is under failure, the other paths can overcome this issue.

The use of beamforming technique in massive MIMO array allows an interesting spatial feature, referred as Full Dimension MIMO [NAM13], [KIM14], allowing 3D MIMO communications as illustrated in Figure I.1.10. While this technique has the advantage to provide high number of connections in urban and rural areas, large antenna and amplification system arrays present the disadvantage of being costly.

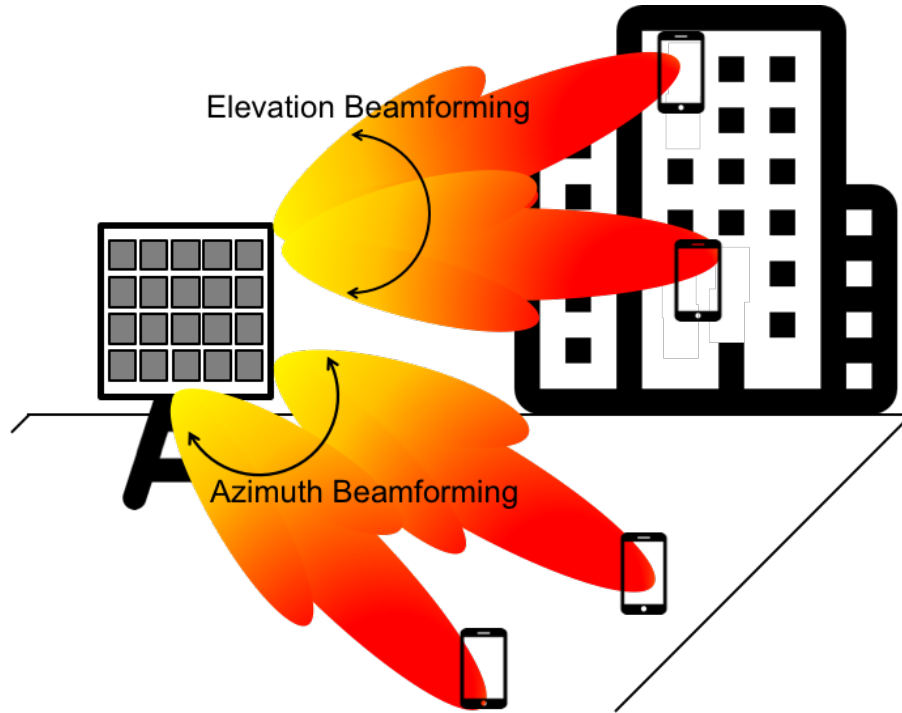


Figure I.1.10: Full dimension MIMO concept

Furthermore, it is notable that while all the antenna and amplification paths will be the same in this kind of base station, the environmental condition can differ from a circuit to another depending on its position on the array or environmental conditions. This can lead to differences into antenna impedances and can be critical at the amplification path systems output. This kind of mismatch can induce standing wave issue caused by the reflection of a wave by the load. The amplitude of the reflected wave is function of Γ_L , the reflection coefficient of the load (I-5).

$$V_{Reflected} = \Gamma_L \cdot V_{Incident} \quad (I-5)$$

It is possible to quantify the “quality” of the matching with the Voltage Standing Wave Ratio (VSWR), a low value corresponding to a poor matching. The VSWR can be estimated with the equation (I-6).

$$VSWR = \frac{1 + |\Gamma_L|}{1 - |\Gamma_L|} \quad (I-6)$$

Depending on the phase conditions of both reflected and incident waves, a destructive or constructive combination between waves can be obtained. A destructive combination reduces the voltage swing at the amplifier output and can degrade the performances of the overall amplification chain. However, constructive combination enhances the voltage swing at the amplifier output and can dramatically degrade the power amplifier, depending on the amplitude

and the duration of this phenomenon. This effect is illustrated in Figure I.1.11. Therefore, security margins are necessary over the output swing to overcome the power amplifier degradation in case of mismatch.

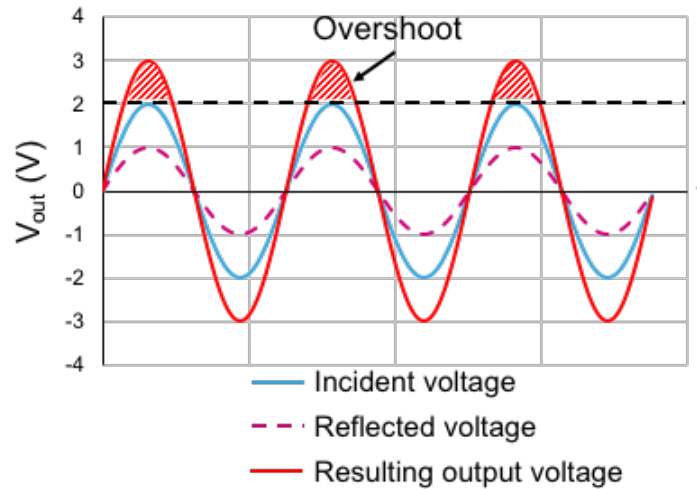


Figure I.1.11: Constructive combination of incident and reflected waves illustration

I.1.4 Overview of potential 5G modulations and waveforms

5G required specifications will not only be achieved with new network architectures. New modulations and waveforms schemes are also under study to achieve these specifications in terms of coverage, speed and multi-service abilities to meet the needs of several use-cases. In this section we provide an overview of some 5G candidate modulations and waveforms that have been identified [NEK16], [MED17], [CAI17]. The use of MIMO architectures impose a specific suitability concerning inter-cell interferences while the use of multiple frequency bands requires suitability to flexible and dynamic band allocation.

Concerning the modulation schemes, recent work shows that high-order Quadrature Amplitude Modulations (QAM) are allowing satisfying performances to fit with the 5G needs [KIM16]. However, the inter-cell interferences in dense urban areas induced by small-cells, backhauling, FD MIMO and their coexistence motivated the researches for non-conventional QAM modulations. Frequency Quadrature Amplitude Modulation (FQAM) [HON13], hybrid between Frequency Shift Keying (FSK) and QAM modulations has recently been explored for 5G applications. An example of FQAM modulation scheme can be found in Figure I.1.12, from [SAM15]. FQAM is particularly advantageous in terms of performances notably concerning frame-error-rate [GSM14] and transmission rates for edge-users [HON14]. Furthermore, these performances enhancement are achieved with no complexity increase as the architecture of an OFDM FQAM transceiver is similar to a classical OFDM architecture [NEK16]. However high peak-to-average power ratio (PAPR) is also achieved with FQAM.

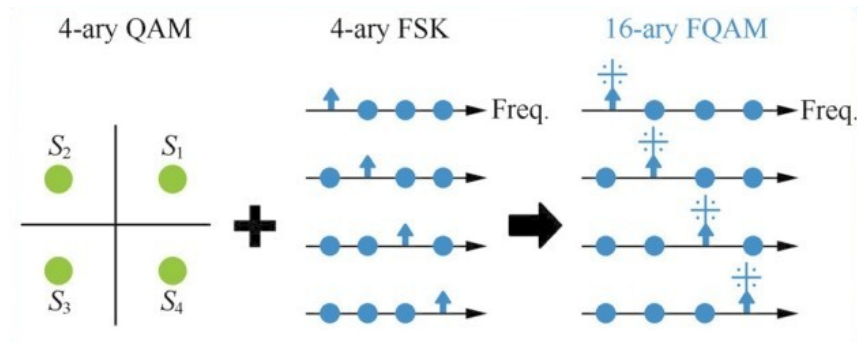


Figure I.1.12: 16-ary FQAM illustration [SAM15]

Amplitude Phase Shift Keying modulation (APSK) [MER15] is a hybrid between ASK and PSK and has recently been studied for 5G. An example of APSK constellation diagram is available in Figure I.1.13 from [LI15]. This modulation, coupled with advanced channel coding and demodulation algorithms has demonstrated interesting performances in terms of channel capacity [IMT15]. In [GAZ11] and [BAL12], it has been illustrated that APSK modulation shows a lower PAPR than conventional QAM with the power back-off benefit for power amplifiers. While complex algorithms used for this modulation are leading to higher transceiver complexity, the PAPR reduction achievable with constellation optimization makes this modulation particularly interesting for 5G.

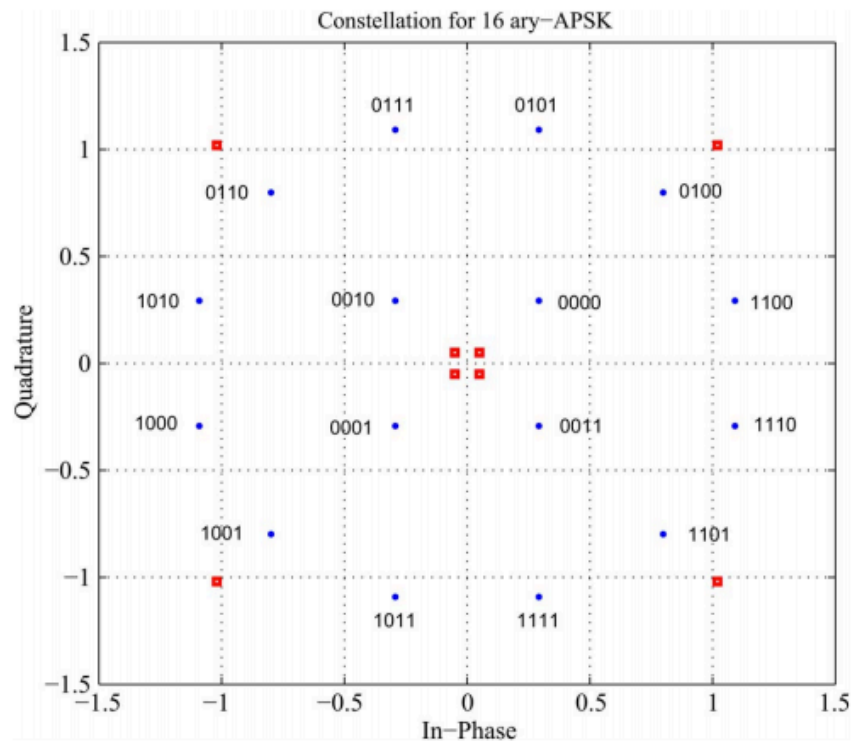


Figure I.1.13: 16-ary APSK illustration [LI15]

In addition to modulation schemes, adapted waveforms are also important. The required specifications drove the need for waveforms that are able to handle multi-frequency spectrum, multiple use-cases with enhanced spectral efficiency and lowered out-of-band emissions to avoid interferences while limiting the power consumption. For this purpose, multi-carrier modulations are being studied. Orthogonal Frequency-Division Multiplexing (OFDM) [CHA66] is actually used in LTE/LTE-Advanced standards and is a strong candidate for 5G. It offers the benefit of being easily integrated in MIMO systems with no added transceiver complexity. OFDM consists in the use of multiple subcarriers within the same channel. The subcarriers are orthogonal to each other's. Therefore, the subcarriers can overlap with no interference. However, guard intervals in the time domain are necessary to avoid multi-path delay induced inter-symbol interferences at the receiver. Cyclic prefix [BIN90] is generally used in OFDM (CP-OFDM) to reduce these inter-symbol interferences. It consists in the prefixing of each symbol by the end part of the same symbol. However, spectral efficiency and out-of-band leakage must be improved to meet the needs of 5G and avoid the use of guard-bands. Figure I.1.14 illustrates the principle of OFDM.

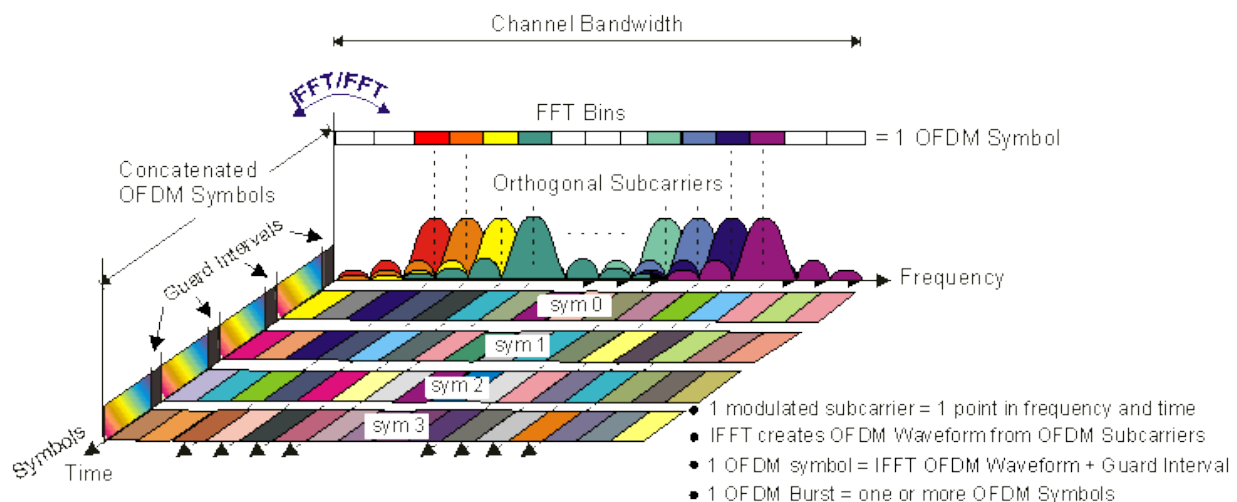


Figure I.1.14: Frequency and time domains OFDM representation [KEY17]

For this purpose, several enhancements of OFDM waveform have been recently studied:

- Filtered-OFDM [ABD15] is performing an optimization over out-of-band leakage through sub-carrier filtering in the frequency domain and is lowering the guard-band consumption. Furthermore, the need for global synchronization system can be relaxed compared to classical OFDM topology [ZHA15].
- Windowed-OFDM is very similar to Filtered-OFDM. It is performing an out-of-band leakage reduction through non-rectangular windows use in the time domain. Therefore, side-lobes reduction is achieved [LUO14] and synchronization requirements can be relaxed [NEK16].
- Unique Word-OFDM [HUE10] is a variant of OFDM that achieves improved bit-error-rate and out-of-band emission performances compared to CP-OFDM [ONI10], [RAJ13].

It consists in the use of a non-random unique-word deterministic sequence as guard-band and does not depend on the transmitted data, contrary to random cycle prefix. Therefore, the symbol duration is not extended. Furthermore, this OFDM variant can be used for synchronization and channel estimation [HOF10].

- Universal Filtered-OFDM [WIL14] allows the use of multiple signal layers with the users separated by their interleavers. This is improving cross-talk and multi-path robustness for multiple access channel. It consists in the filtering of sub-carriers blocks. Compared to CP-OFDM, inter-symbol interferences are reduced and the spectral efficiency is improved thanks to guard-band reduction.

However, maximum spectral efficiency is still not achieved and solutions like FBMC waveforms [BEL10] have been proposed for 5G but make the transceivers architectures more complex. Finally, high PAPR is still achieved with OFDM based waveforms and complex modulation schemes that could be used for future wireless networks, compared with single-carrier waveforms due to large signal envelope fluctuations [ROH99]. PAPR reduction for complex modulation schemes and waveforms is actually a trend in the literature to address the 5G challenges [LAA15], [BUL14], [BEN17].

I.1.5 CMOS technology for 5G

In the previous sections we highlighted that the future mobile network will be defined by the use of small-cells to densify the network. A huge increase of smartphone number and data use, Massive MIMO phased array for beamforming and power consumption reduction are also expected. This mass market requires production costs limitation and high integration capacities for both active network nodes, base stations and end-user devices.

The III-V semiconductors technologies like GaN or GaAs and silicon based SiGe are offering high power capabilities. However, their integration capacity is limited and the production costs are higher compared to CMOS technology. In addition, transceivers in III-V technologies suffer from high power consumption due to high supply voltage levels. At the contrary, CMOS technologies present a high capacity of integration while they are low cost in terms of production. A comparison between GaAs, SiGe and CMOS technology is available in Figure I.1.15.

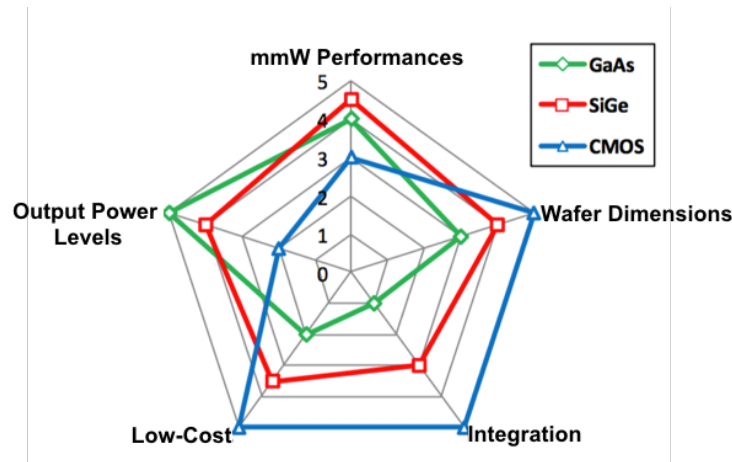


Figure I.1.15: GaAs, SiGe and CMOS technologies comparison [LAR15-2]

Nevertheless, the downscaling in CMOS technologies made them more adapted for digital circuits. This downscaling, offering lower gate-length, gate oxide thickness and supply voltages allows higher die density, faster devices and reduced power consumption. Recent progresses have been made to allow successful implementation of RF circuits and complete transceivers on CMOS technologies, offering promising performances in deep sub-micron technologies.

With advanced technologies like CMOS SOI, it is possible to integrate both high-speed digital and RF parts to leverage System On Chip (SOC) [CHA99] integration (Figure I.1.16) and so lowering the production cost of communication systems.

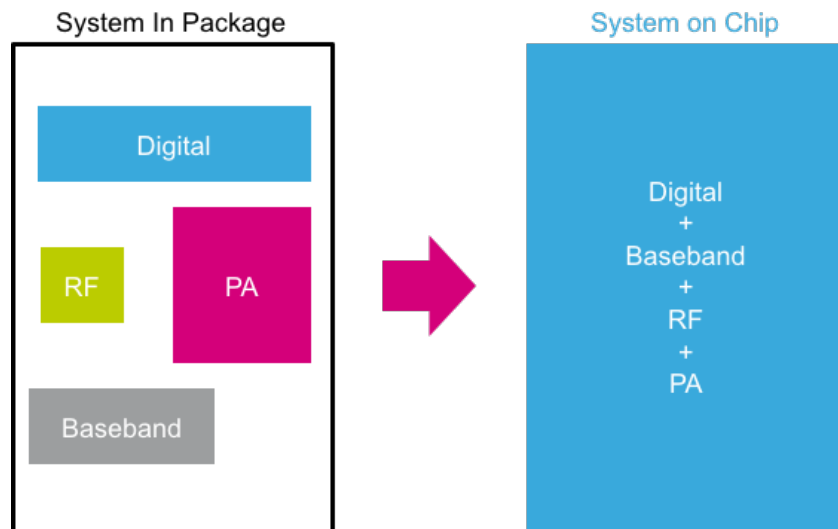


Figure I.1.16: System on Chip compared to System in Package

However, the power amplifier remains a bottleneck for SoC integration in advanced deep sub-micron technologies. In fact, the CMOS technology suffers from low transistor breakdown voltages that limit the achievable output power compared to III-V technologies. Nevertheless, the use of Massive MIMO phased-arrays reduce the need for high output power with multi-path

amplification on emitters, as the power is distributed over a wide range of systems. Therefore, the specifications over transmitted power are relaxed. Furthermore, the contribution of power amplifier to overall device power consumption, in both user-end and actual base station, is very large and has to be reduced while high linearity levels are expected. The challenges of CMOS amplifiers for 5G and SoC applications that this thesis addresses are developed in Section I.2.4.

I.2 Power Amplifier theory

I.2.1 Power amplifier generalities

In all RF transceiver architectures, the power amplifier is the last element of the transmission chain just before the antenna (Figure I.2.1) and remains challenging to design as a malfunction or degradation impacts critically the overall transmitter performances. In order to achieve power amplifier performance analyses and comparison with the state of the art, several figures of merits can be used and are depicted in the following section.

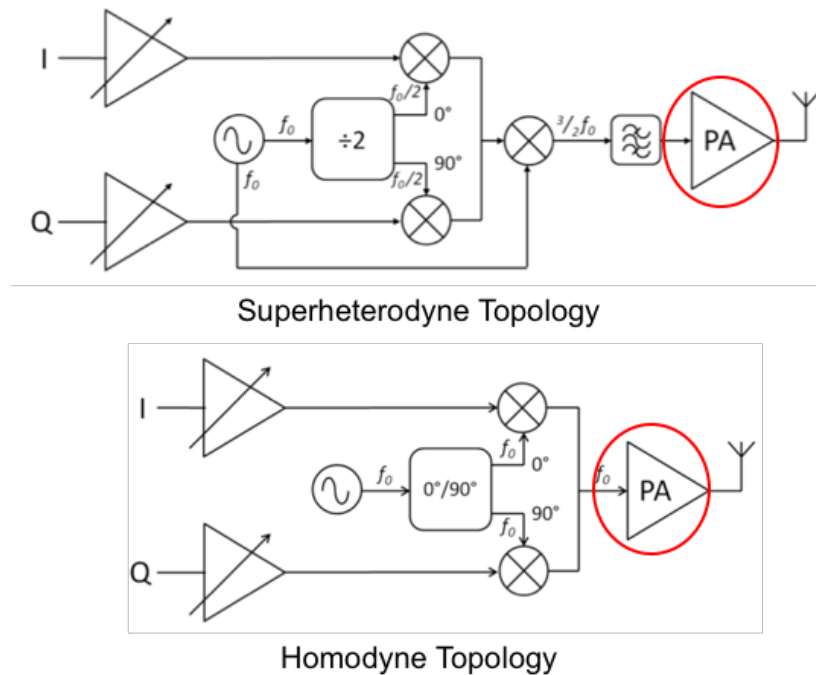


Figure I.2.1: Power amplifier in different transmitter topologies

First of all, before detailing these different PA performances, it is primordial to be familiar with the different parameters that will be used for calculations. The Figure I.2.2 summarizes these parameters while Table I.2.1 gives their definition.

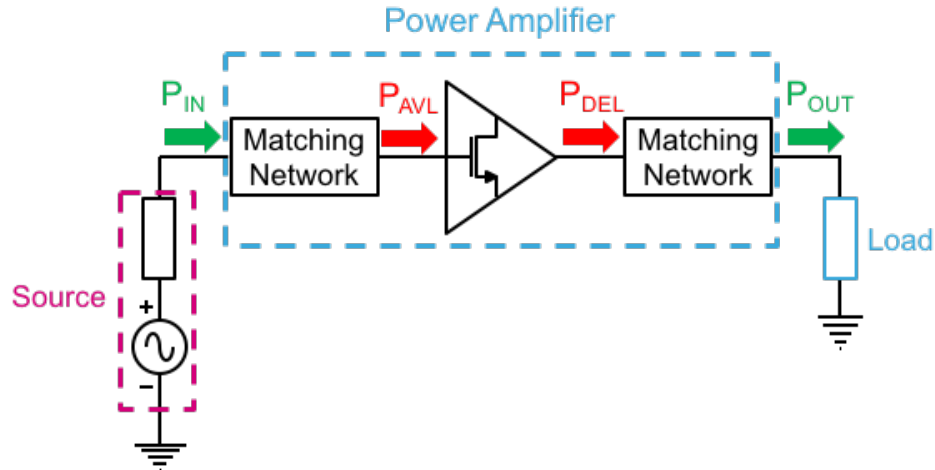


Figure 1.2.2: Different powers involved in a power amplifier

Name	Definition
P_{IN}	Power delivered by the source
P_{AVL}	Power available at the input of the power amplifier
P_{DC}	Power consumed by the power amplifier
P_{DEL}	Power delivered by the power amplifier
P_{OUT}	Power delivered to the load

Table 1.2.1: Definition of the different powers involved in a power amplifier

From these parameters it is then possible to define the following power amplifier performances.

- Power added efficiency

The power added efficiency (PAE) is a primordial parameter for power amplifier designed to target mobile networks applications. It links the device input and output power levels with the overall power consumption and so traduces the power amplifier efficiency. This parameter is calculated with (I-7).

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} \quad (I-7)$$

Several power added efficiency values are interesting to determine when it comes to power amplifier analysis. The PAE_{max} , corresponding to peak efficiency, is generally used for comparison with the state of the art. However, with complex modulation schemes, the amplifier tends to operate at a certain back-off from maximum output power. The PAE at back-off is so an interesting parameter to enhance. Furthermore, the efficiency at P_{1dB} , developed in the following section, is also an important comparison point.

Another efficiency parameter can be used, the drain efficiency η_D , but does not take the input power into account in the calculation. This parameter is not preferred for analysis of power amplifiers operating in sine classes. However, it is possible to use it to define efficiency of power amplifier showing different waveforms at the input and output. It is also an interesting parameter to characterize single transistors. Its formula is given in (I-8).

$$\eta_D = \frac{P_{OUT}}{P_{DC}} \quad (I-8)$$

- Power Gain

The power gain is the parameter that traduces the power amplifier ability to produce output power from a certain amount of power at its input. Several definitions of power gain are available and differs depending on the definition of input power. The definition of the power gain that is used in this work is the transducer gain. It offers the best definition in our case as it takes into account the losses and mismatch induced by matching networks, corresponding to the amplifier in its implementation environment. This power gain can be calculated with the equation (I-9).

$$G = G_{tr} = \frac{P_{OUT}}{P_{IN}} \quad (I-9)$$

Generally, the input and output powers are expressed in dBm, then the power gain becomes (I-10):

$$G(dB) = G_{tr}(dB) = P_{OUT}(dBm) - P_{IN}(dBm) \quad (I-10)$$

- Linearity

The linearity is a fundamental parameter for PA operating in communication networks. It traduces the power amplifier ability to amplify a signal without distortion. Several parameters evaluate the linearity of a power amplifier.

- 1dB compression point

If we consider a continuous-wave signal (CW) applied at the input of a power amplifier, the output power will be defined by (I-11) and (I-12):

$$P_{OUT} = G \times P_{IN} \quad (I-11)$$

$$P_{OUT}(dBm) = G(dB) + P_{IN}(dBm) \quad (I-12)$$

The P_{OUT} versus P_{IN} characteristic can be plotted and two zones corresponding to two distinct operations are identified:

- A linear zone.
- A non-linear zone where the power gain is decreasing and corresponding to the power amplifier compression.

The ICP1/OCP1 are corresponding to the input/output power levels respectively, where the power gain is reduced by 1dB compared to its linear characteristic. These linearity parameters are illustrated in Figure I.2.3. It is also noticeable that several notations are used in the state of the art to define the output compression point: OCP1, P_{1dB} , P_{-1dB} ... The relation between OCP1 and ICP1 is given by (I-13).

$$OCP1(dBm) = (G(dB) - 1) + ICP1(dBm) \quad (I-13)$$

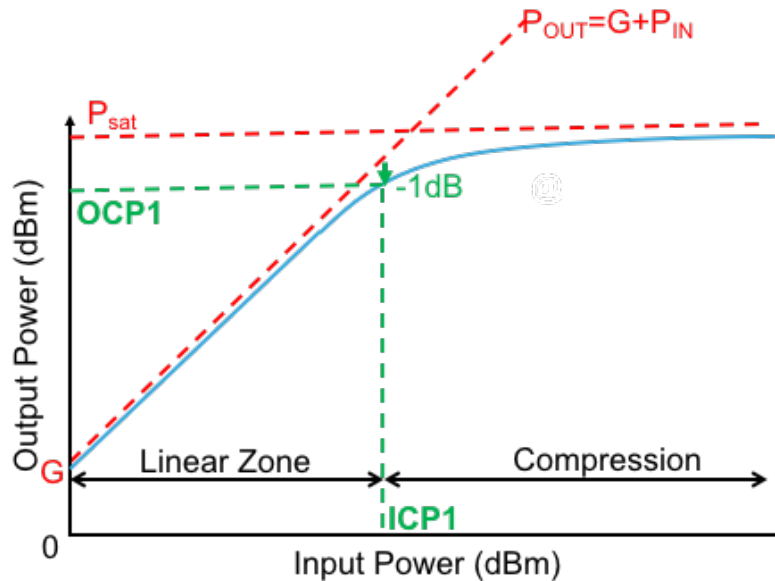


Figure I.2.3: P_{OUT} VS P_{IN} , ICP1/OCP1 illustration

- AM-AM and AM-PM conversion

Two others parameters are also evaluated to express the power amplifier linearity under CW conditions. While AM-AM represents the gain conversion, the AM-PM gives an interesting information about the phase evolution over input/output power levels. Ideally these two parameters characteristics should remain flat. AM-AM and AM-PM conversion curves are available in Figure I.2.4.

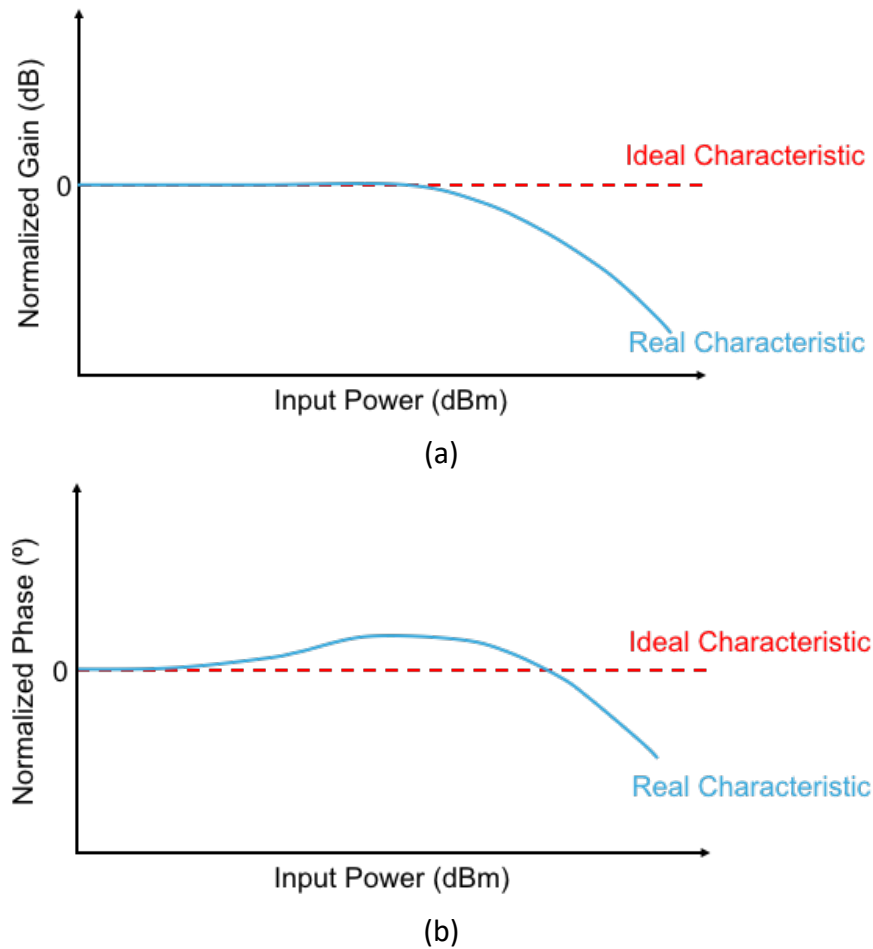


Figure I.2.4: AM-AM (a) and AM-PM (b) conversions illustration

I.2.2 PA classes of operation

The power amplifier operations are divided in several classes, corresponding to different input/output signals waveforms and transistor states. These classes are controlled by the biasing conditions and/or the harmonic matching conditions. Two main types of classes are available:

- Sine classes, grouping A, B, C and AB classes.
- Switched classes grouping D, E and F classes.

Several other switched classes variations exist. However, we only focus on the D, E and F overview as in this work only sine classes have been implemented. The maximum achievable efficiency values of these classes are estimated using drain efficiency as classes are compared without taking into account input matching conditions.

- Class A

Class A operation is defined by the transistor continuous conduction state. This class is corresponding to a biasing point located on the middle of the load line over $I_D=f(V_{DS})$ characteristic. Class A theoretically achieves the highest output power and gain levels if perfectly matched. However, the maximum drain efficiency achievable by this class of operation is limited to around 50% as it is illustrated in (I-14).

$$\eta_{MAX-Class-A} = \frac{P_{OUT}}{P_{DC}} = \frac{\frac{1}{4} \cdot (V_{DD} - V_T) \cdot I_{MAX}}{\frac{1}{2} \cdot V_{DD} \cdot I_{MAX}} \quad (I-14)$$

$$\eta_{MAX-Class-A} \approx 50\% \quad (I-15)$$

- Class B

The class B operation is defined by a biasing point located on threshold voltage V_T over $I_D=f(V_{GS})$ characteristic. This is leading to a conduction time of half a cycle. While the efficiency is improved in this class compared to class A operations and can be calculated with (I-16), while the output power, gain and linearity are lower than in class A.

$$\eta_{MAX-Class-B} = \frac{P_{OUT}}{P_{DC}} = \frac{\frac{1}{4} \cdot (V_{DD} - V_T) \cdot I_{MAX}}{\frac{V_{DD} \cdot I_{MAX}}{\pi}} \quad (I-16)$$

$$\eta_{MAX-Class-AB} \approx 78.5\% \quad (I-17)$$

- Class C

The operation in class C is defined by a biasing point located under V_T on $I_D=f(V_{GS})$ characteristic and is leading to a theoretical efficiency level over 78.5%.

- Class AB

Class AB operation is a hybrid between class A and class B. This operating class is leading to a conduction angle θ between π and 2π . This type of operation achieves efficiency levels comprised between 50% and 78.5% in theory, as it is illustrated in (I-18) - (I-20).

$$\eta_{MAX-Class-AB} = \frac{P_{OUT}}{P_{DC}} = \frac{1}{2} \cdot \frac{V_{DD} - V_T}{V_{DD}} \quad (I-18)$$

$$\eta_{MAX-Class-AB} = \frac{\theta - \sin(\theta)}{2 \sin\left(\frac{\theta}{2}\right) - \theta \cos\left(\frac{\theta}{2}\right)} \quad (I-19)$$

$$50\% < \eta_{MAX-Class-AB} < 78.5\% \quad (I-20)$$

Illustrations of operating point for sinusoidal classes are available in Figure I.2.5 while conduction zones of a transistor depending on the operating classes are available in Figure I.2.6.

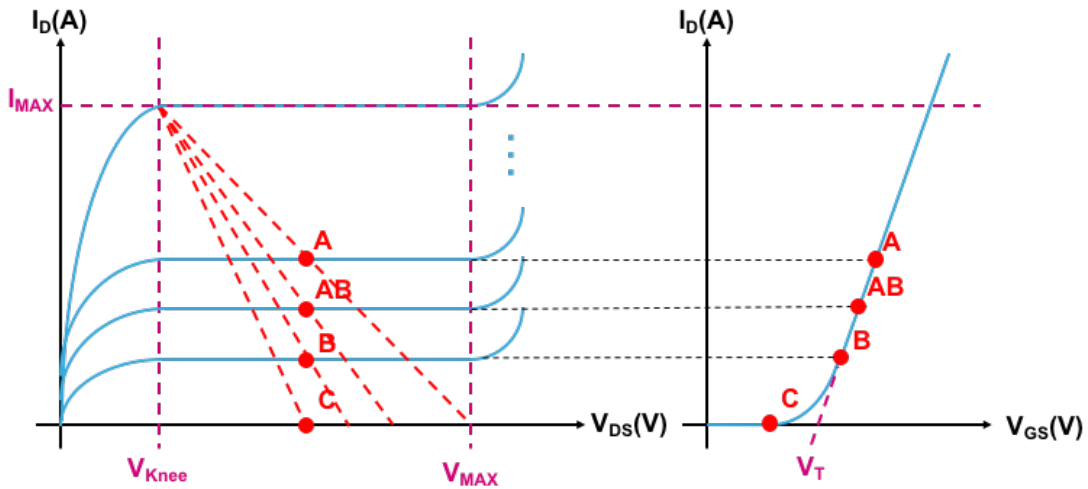


Figure I.2.5: $I_D=f(V_{DS})$ and $I_D=f(V_{GS})$ characteristics with sinusoidal operating classes

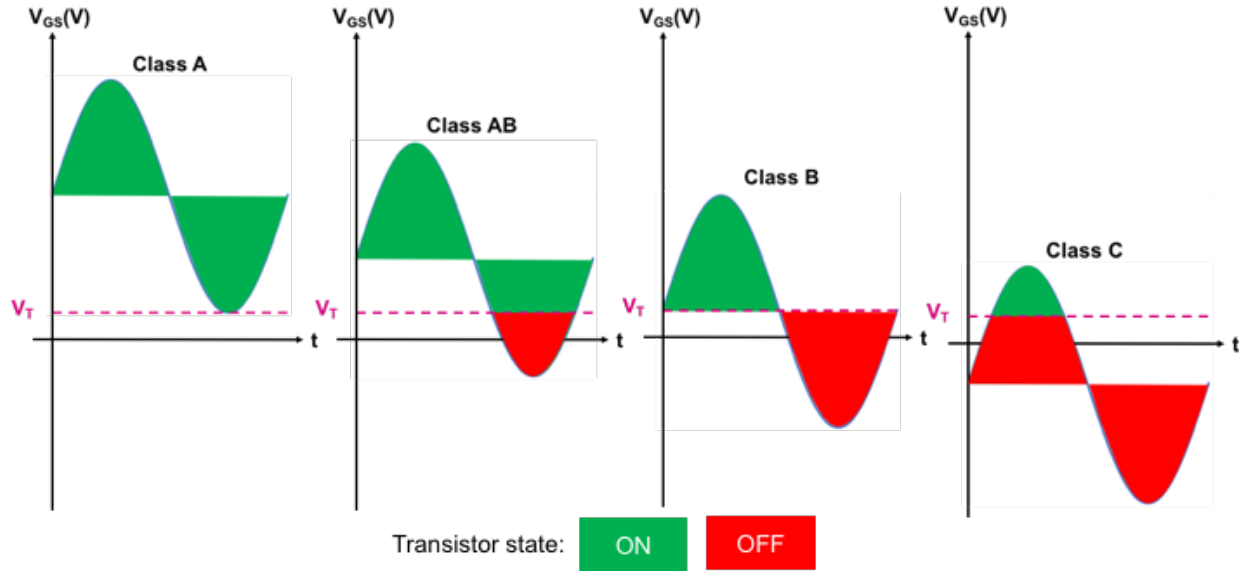


Figure I.2.6: Transistor conduction zones in different sinusoidal operating classes

While sinusoidal classes are linear but efficiency limited, it is possible to use transistors as switches to improve efficiency with conduction angles of 0° . However, linearity will be reduced with the following switched classes. Therefore, their use for wireless network applications will necessitate to implement additional linearization techniques.

- Class D

Class D amplifier allows power consumption reduction by using two transistors. The transistors are switched ON and OFF alternatively. LC resonators are associated at the output in order to eliminate the harmonics and keep the fundamental at the right frequency. The output voltages and currents waveforms do not overlap and a drain efficiency of 100% can be theoretically achieved in class D operation (I-21).

$$\eta_{MAX-Class-D} = \frac{P_{OUT}}{P_{DC}} = \frac{\frac{V_{DD} \cdot I_{MAX}}{\pi}}{\frac{V_{DD} \cdot I_{MAX}}{\pi}} \quad (I-21)$$

$$\eta_{MAX-Class-D} \approx 100\% \quad (I-22)$$

- Class E

The class E amplifier uses only one transistor that is switched. When the transistor is ON, it presents a low resistance ideally negligible that ensure an ideal null power consumption. When the transistor is OFF, it presents a very high impedance and ideally no current is flowing while the

power consumption is ideally null. Therefore, for ideal switching, the current and voltage output waveforms of the amplifier are in opposition of phase with no overlap and a theoretical drain efficiency of 100% can be achieved. In this class, the higher harmonics see an open circuit.

- Class F

The class F amplifier uses a sinusoidal input signal. Waveform engineering at transistor level is performed thanks to the output matching to form a square waveform. Series resonators absorb even harmonics while presenting an open circuit to the odd harmonics. This is leading to an output current composed only by even harmonics while the output voltage is composed only by the odd harmonics. Therefore, for an ideal infinite number of harmonics, no overlap exists between output current and voltages and then an ideal theoretical efficiency value of 100% can be obtained with a square V_{DS} curve.

Because these switched classes efficiency enhancement is based on ideal switching with no overlap between output current and voltage waveforms, the impact of parasitic elements is critical. In fact, the parasitic elements at transistor level at high frequency make the transistor switching non-ideal and reduce the benefit over efficiency of these classes. The interest of these classes for mmW operation is then limited. Figure I.2.7 summarizes the presented switched class amplifiers architectures and associated waveforms. The link between classes, I_{DS} conduction angles and theoretical maximum efficiency is summarized in Table I.2.2.

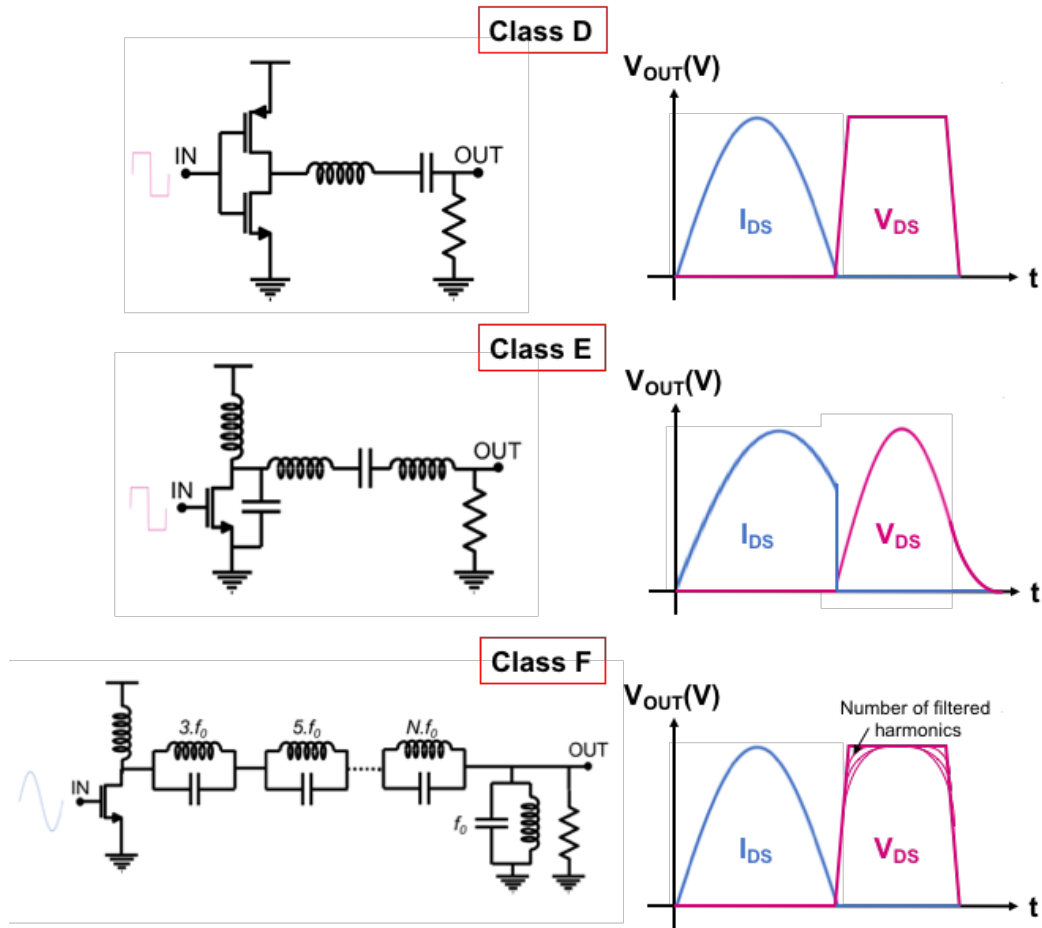


Figure I.2.7: Switched operating classes amplifiers and waveforms

Operating Class	Conduction angle θ	η_{MAX}
A	2π	50%
AB	$\pi < \theta < 2\pi$	$50\% < \eta_{MAX-Class-AB} < 78.5\%$
B	π	78.5%
C	$< \pi$	$> 78.5\%$
D, E, F	0	100%

Table I.2.2: Theoretical efficiency achievable by operating classes

I.2.3 Parameters for modulated signals

We developed previously that potential 5G modulations and waveforms could be based on OFDM. This type of multicarrier modulations implies a large input power dynamic compared to single-carrier modulations and necessitates linear amplification. Therefore, the parameters evaluated for linearity in Section I.2.1 are not sufficient to conclude over power amplifier linearity under complex modulated signal conditions.

Several additional parameters can be evaluated for this purpose and are developed in this section:

- The Adjacent Channel Leakage Ratio (ACLR), also named Adjacent Channel Power Ratio (ACPR).
- The Error-Vector Magnitude (EVM).
- The notion of Output Back-Off (OBO).
- The Peak-to-Average Power Ratio (PAPR).

- ACLR

The adjacent channel leakage ratio defines the quantity of parasitic signal generated over adjacent channels to the channel of interest. These parasitic are generated by the non-linearity of the power amplifier and more specifically by the intermodulation products. Stringent requirements over ACLR are posed by the standards emission masks for wireless communications to avoid any critical pollution of adjacent bands and allow simultaneous use of these bands. The ACLR is calculated with the equation (I-23) where $P(f)$ is the spectral power density at the output of the amplifier.

$$ACLR = \frac{2 \int_{B_0} |P(f)| df}{\int_{B_1} |P(f)| df + \int_{B_2} |P(f)| df} \quad (I-23)$$

Where B_0 , B_1 and B_2 are the power levels on the operation band and the adjacent bands respectively. This phenomenon is illustrated in Figure I.2.8.

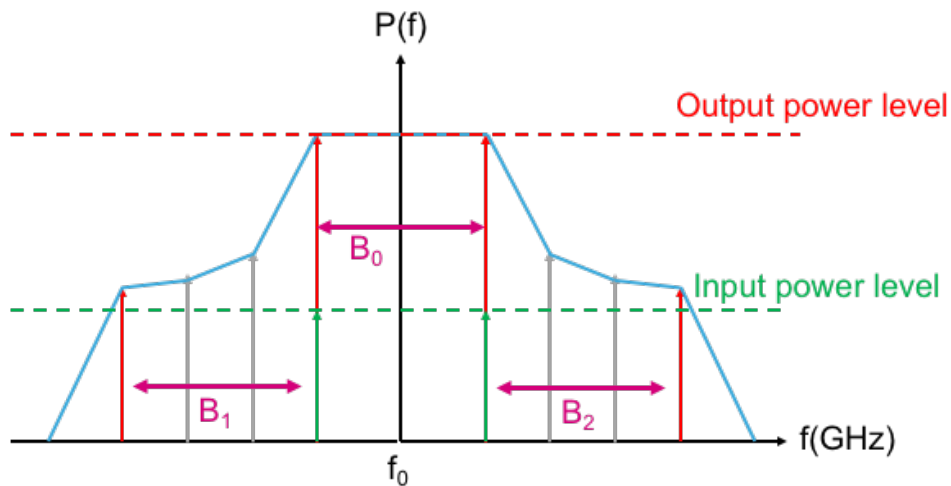


Figure I.2.8: Adjacent channel leakage ratio illustration

- EVM

The error-vector magnitude is a parameter that allows the evaluation of the transmitted symbol dispersion at the output of the power amplifier, compared to the ideally expected symbol. In practice, the power amplifier non-linearity induces a shift of these symbols that must remain limited to ensure the quality of the transmitted signal and avoid the losses of information during demodulation at the reception. The EVM is the module of the error vector between measured and ideal symbol. It can be calculated with the equation (I-24) and the Figure I.2.9 illustrates this non-desirable effect.

$$EVM_{RMS} = \sqrt{\frac{\frac{1}{N} \sum_{k=1}^N [(I_{meas,k} - I_{exp,k})^2 + (Q_{meas,k} - Q_{exp,k})^2]}{\frac{1}{N} \sum_{k=1}^N [(I_{exp,k})^2 + (Q_{exp,k})^2]}} \quad (I-24)$$

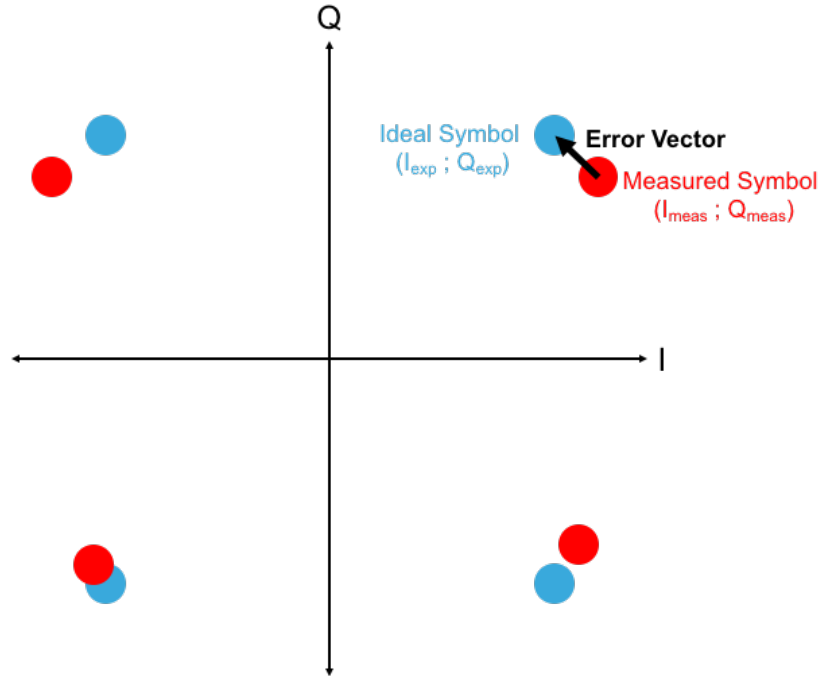


Figure I.2.9: Error vector illustration

- PAPR

The peak-to-average power ratio parameter is estimated to quantify the ratio between P_{MAX} the peak power, and P_{AVG} the average power during a time interval. This is necessary to quantify the signal envelope variations induced by complex modulations where the time-domain

signal $S(t)$ has non-constant envelop. As in OFDM waveforms multiple carriers are used, $S(t)$ is defined by the equation (I-25).

$$S(t) = A \sum_{k=-\infty}^{+\infty} \sum_{i=0}^{N-1} x_{i,k} \cdot \omega(t - kT) \cdot e^{j2\pi i \Delta f (t - kT)} \quad (I-25)$$

With:

- A : the signal amplitude
- $x_{i,k}$: the symbol of a subcarrier i at a time k
- N : the number of subcarriers
- $\omega(t - kT)$: the window function
- Δf : the frequency difference between sub-carriers

The PAPR is then defined by (I-26).

$$PAPR(dB) = \frac{P_{MAX}}{P_{AVG}} = \frac{\max_{[0,T]} |S(t)|^2}{\frac{1}{T} \int_0^T |S(t)|^2 dt} \quad (I-26)$$

- OBO/PBO

The output back-off is defined as the ratio between maximum output power achieved by the power amplifier and the average modulated signal power. It is calculated with the equation (I-27).

It is also possible to define the peak back-off, PBO, as the difference between maximum output power and instant maximal power, corresponding to the power amplifier marge of utilization from P_{SAT} . The PBO can be calculated by the equation (I-28).

$$OBO(dB) = 10 \log \left(\frac{P_{SAT}}{P_{AVG}} \right) \quad (I-27)$$

$$PBO(dB) = OBO(dB) - PAPR(dB) \quad (I-28)$$

High values of PAPR will lead to large peak back-off to ensure good linearity. The efficiency is also impacted as it generally increases with the output power. A large PBO will then lead to a reduced level of efficiency. Furthermore, as the linear power delivered by the power amplifier is limited, the transistors are over dimensioned and so consume more power. This is traducing the traditional trade-off between output power, linearity and power consumption.

I.2.4 PA for 5G: Specifications

As we stated previously, the power amplifier for SoC implementation and 5G applications is a bottleneck. In fact, power amplifier design has become a real trend in the literature throughout the years and network generations, and the study of power amplifier for 5G will be an important axis of research for the next years (Figure I.2.10).

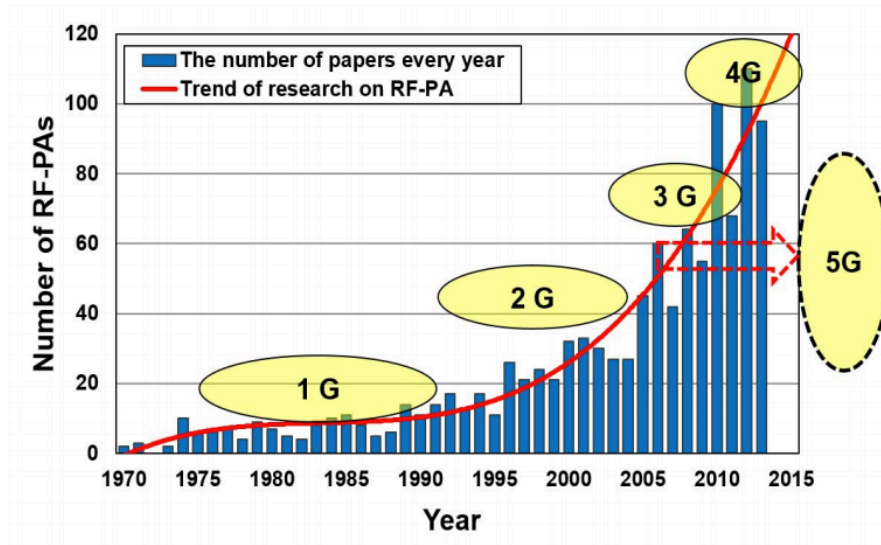


Figure I.2.10: Research of RF PA trend [CHE15]

In this section, we present the specifications relative to these applications for a deep sub-micron power amplifier implementation that is the topic of this thesis. The power amplifier is the most power-consuming block of the overall modern transceivers. This is illustrated in Figure I.2.11, where the power consumption is higher than the sum of the other parts of the transmitters.

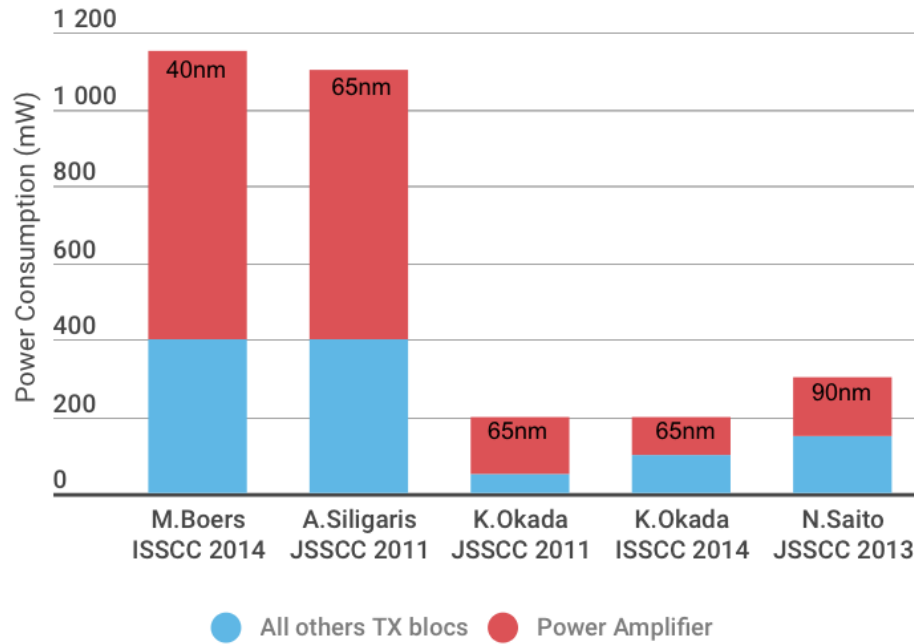


Figure I.2.11: Power consumption in 60GHz transmitters state of the art

Furthermore, in the base station the power amplifier is also the most power consuming element. This is illustrated in Figure I.2.12 from [AUE11] representing the dissipated power repartition in a 4G base station. The power amplifier consumes more than all the other elements of the station (57%), supply and cooling included.

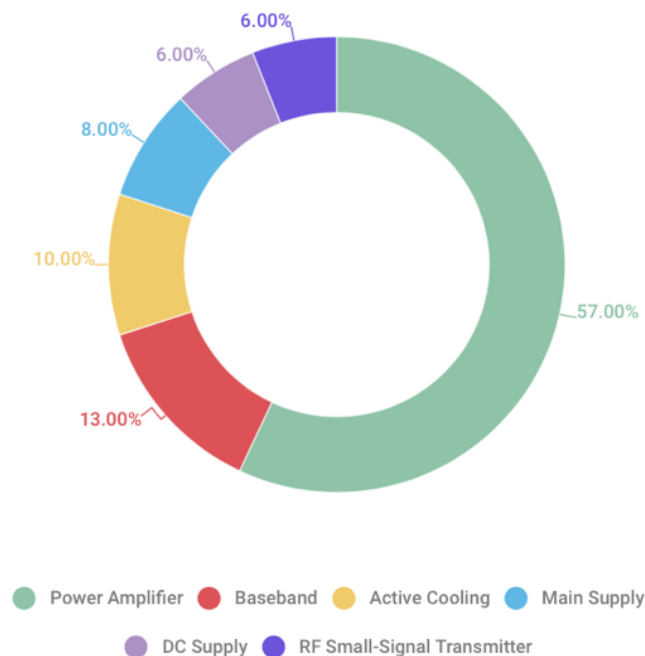


Figure I.2.12: Dissipated power repartition in 4G base station (data from [AUE11])

The network coverage through small-cells and Massive MIMO implies a densification of both network active nodes and power amplifiers per base station. Therefore, power consumption reduction in power amplifiers is needed. Furthermore, power amplifiers with high efficiency are also needed in this optic of more power efficient networks for lower operating costs and environmental impact. While output power level requirements are relaxed by the use of Massive MIMO and multiple amplification path, the need for high levels of gain has been highlighted in recent transceiver [SAD17] (32dB of gain on single path). However, simultaneously good level of efficiency and performances are challenging in any power amplifier design.

Moreover, as we saw in Section I.1.4, the complex modulations and waveforms potentially derived from OFDM are leading to high PAPR values. Power amplifiers will then operate at high peak power back-off. Therefore, high linearity is needed to ensure a good quality of transmission while linearity/consumption tradeoff is well known by power amplifier designers. Furthermore, the efficiency at back-off tends to be low in mmW power amplifiers and has to be enhanced.

We also pointed at the fact that the specifications of the network in terms of data-rate and latency will depend on the use-case. Therefore, system reconfigurability in terms of frequency and/or performances are benefit for the applications. From a power amplifier perspective, while frequency band reconfigurability and wideband design are challenging, a reconfigurability in mode is also benefit. Gain reconfigurability is interesting for system level control in SoC. In [CHE17], a digital gain control allows thermal compensation to avoid heat induced PA gain drop. Multimode dynamic operations can also leverage power consumption improvement with:

- A limited power consumption and performances mode to be used most of the time.
- A high performance “boost” mode with higher power consumption only used if necessary.

Finally, as the implementation in phased-array systems can lead to antenna mismatch due to the environment variations, it is important to propose systems that are robust to these variations to avoid any malfunction or degradation. Several solutions are available like self-healing circuits [BOW13] that are able to monitor and adapt to external variations while self-contained circuits [ZOU04] are robust to environment variations.

The design of power amplifier for SoC and 5G is then challenging as it has to address simultaneously multiple challenges while providing high performances at mmW frequencies, and is the objective of this thesis.

I.3 mmW PA state of the art

In this section, we present several power amplifier designs that have been published in the state of the art. These circuits have been chosen as they address one or several 5G identified challenges. This section is separated in two distinct parts to better highlight the context of the work presented in this thesis. The first section shows the state of the art available at the time the

realized circuit has been designed. The second section shows the state of the art after the presented power amplifier design, in order to offer an up to date state of the art to the reader and to confirm several 5G PA design trends while highlighting actual limitations.

I.3.1 State of the art before circuit design

- 10GHz/25GHz dual-band power amplifier

The power amplifier presented in [WAN15] has not been designed to target 5G but X/K-band radar. However, multi-band abilities and frequency near to 5G bands are interesting. This power amplifier is implemented in 180nm CMOS technology and is featuring a single-ended 2-stages topology as it is presented in Figure I.3.1. The power stage is a cascode architecture to maximize power gain, stability and output power. The driver stage is composed by two common-source transistors to improve the overall gain.

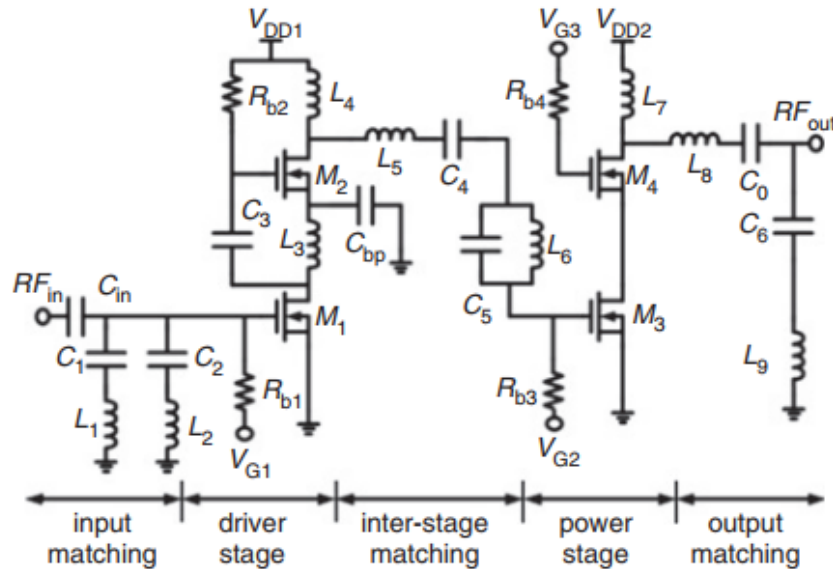
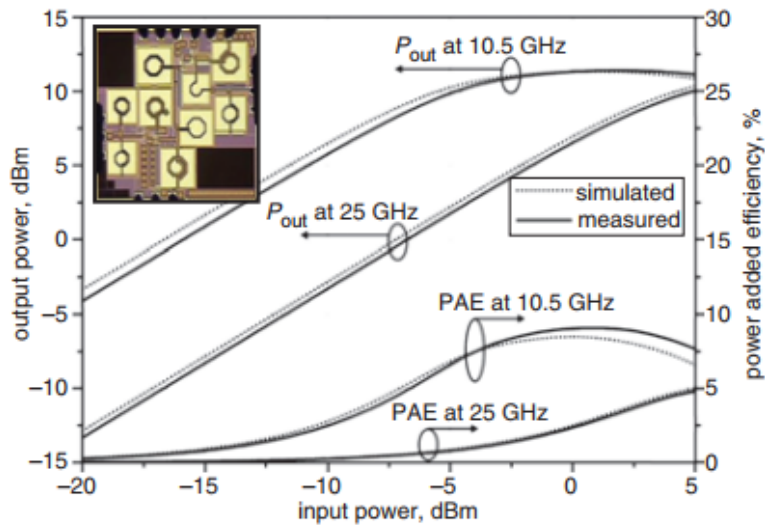
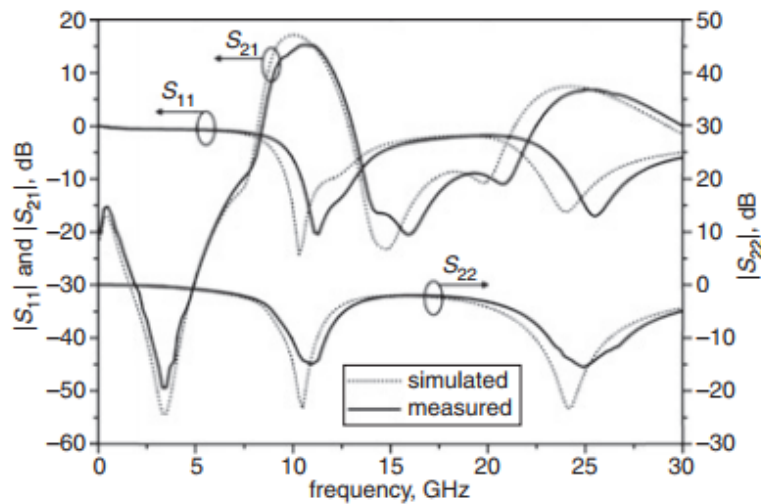


Figure I.3.1: Dual-band power amplifier scheme [WAN15]

The dual-band ability is made possible by the matching networks that are also achieving harmonics and intermodulation products suppression. However, these matching networks introduce losses and a current re-use technique is implemented on the driver stage to compensate these losses regarding power gain. Despite these interesting features, the performances achieved by this amplifier are low to address mmW 5G applications. The difference between performances at 10GHz and 25GHz regarding efficiency (PAE_{max} of 9% at 10GHz, 4.8% at 25GHz) and power gain (15.2dB at 10GHz, 6.8dB at 25GHz) illustrates the difficulty to provide same performance levels at two frequencies simultaneously. These performances are available in Figure I.3.2.



(a)



(b)

Figure 1.3.2: Bi-band power amplifier performances [WAN15]:

CW performances (a) and S-parameters (b)

- High output power and wideband power amplifiers

Two power amplifiers implemented in 45nm CMOS SOI technology are presented in [JAY16], featuring single-ended 4-stacked topologies biased in Class AB. Both of these amplifiers are using multi-gate transistor layout, in order to reduce the parasitics of each transistor and between stages compared to a conventional stacked topology. The difference between these two circuits is the sizing of the transistors. The first circuit is featuring total transistor width of 230 μ m and the second circuit is featuring a total width of 307 μ m. Transistor stacking allows high frequency bandwidth over 10GHz for both circuits. The use of single-stage topology is leading to high

efficiency levels with a PAE_{max} of 29% and 26% for first and second PA respectively but is leading to limited gain for both power amplifiers ($<14dB$). Transistor stacking allows high output power of 23dBm for both circuits without needing power combining thanks to a supply voltage up to 5.2V. However, this high supply voltage is leading to a high-power consumption over 400mW that is not compatible with the 5G requirements. Figure I.3.3 presents the power amplifier schemes and photomicrographs while Figure I.3.4 is illustrating the achieved performances under 5.2V (high-bias) and 5V (low-bias).

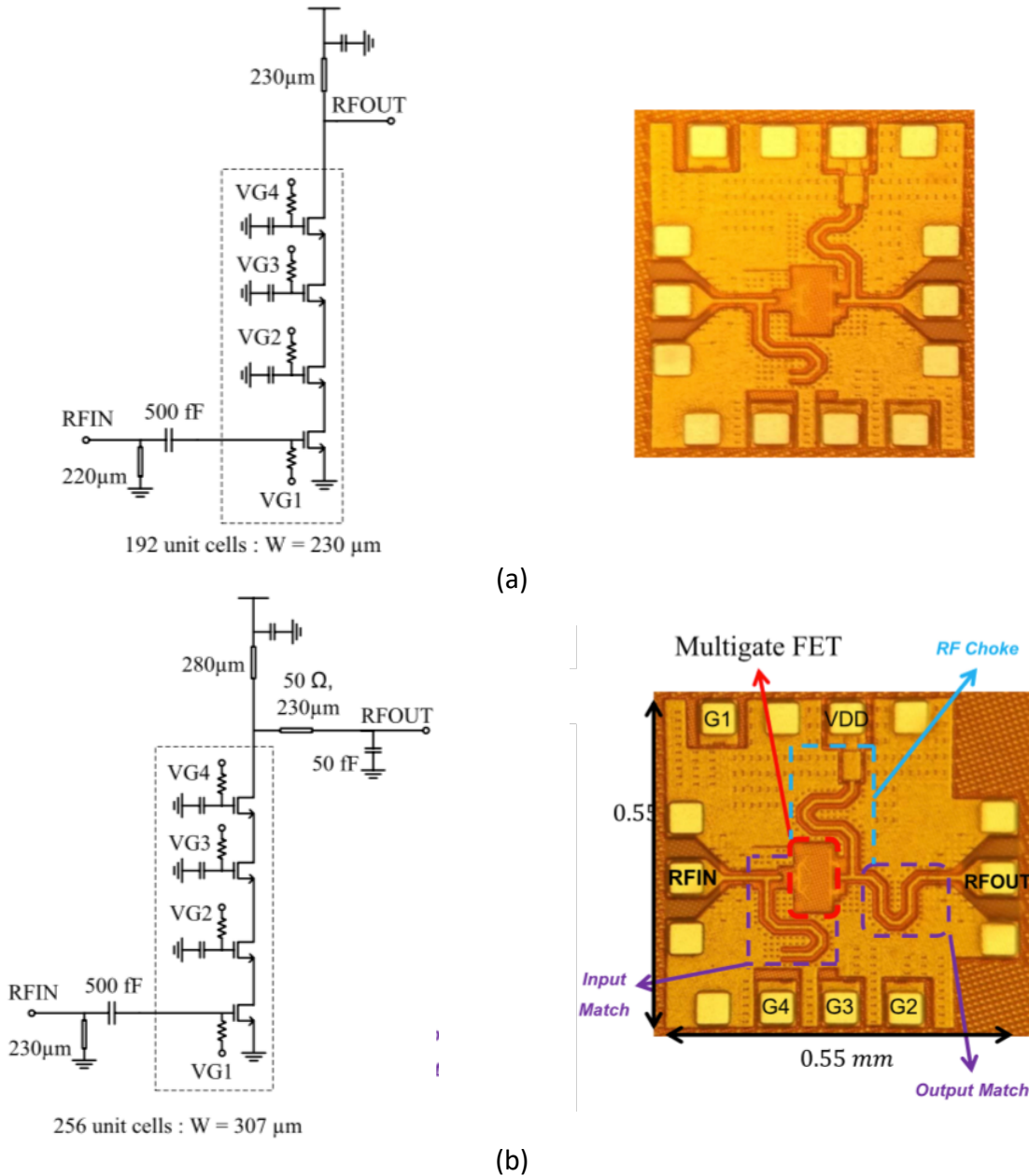


Figure I.3.3: 4-stacked PA from [JAY16], $W_{tot}=230 \mu m$ (a) and $W_{tot}=307 \mu m$ (b)

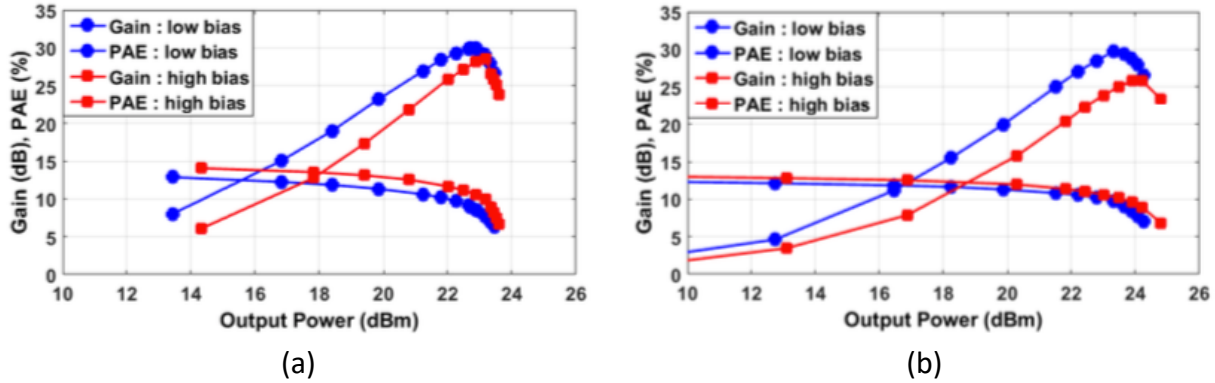


Figure I.3.4: CW performances of 4-stacked PA from [JAY16], $W_{tot}=230\mu\text{m}$ (a) and $W_{tot}=307\mu\text{m}$ (b)

- Highly linear and efficient power amplifiers

The reference [PAR16] presents two 28GHz differential single-stage power amplifiers implemented in 28nm CMOS technology. One is exhibiting a common-source topology while the other is a cascode topology (Figure I.3.5). Both power amplifiers are featuring a 2nd harmonic control circuit to provide linear operations by shorting the 2nd harmonics to the ground. Capacitive neutralization is implemented for both power amplifiers and allows common-source C_{GD} parasitic capacitance reduction to improve isolation, stability and higher the gain.

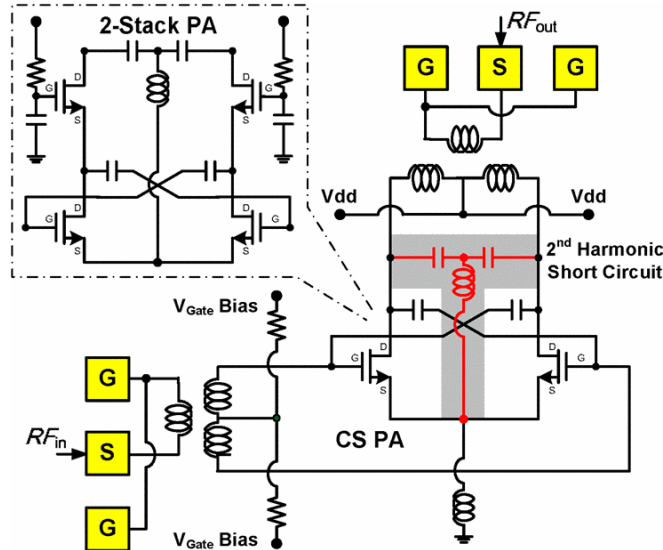


Figure I.3.5: Common-source and 2-stack PA topologies from [PAR16]

In this work, the advantage offered by cascode topology compared to common-source topology is clearly highlighted. At the same frequency of operation, a power gain of 13.6dB/10dB, a PAE of 43.3%/36.5% and an output power of 19.8dBm/14.8dBm under 2.2V/1.1V are obtained for cascode/common-source topology respectively. While good performances in terms of output power and PAE are reached with linear operation, the single-stage topology avoids excessive

losses in passives for efficiency enhancement but also provides a low level of power gain. Performances are available in Figure I.3.6.

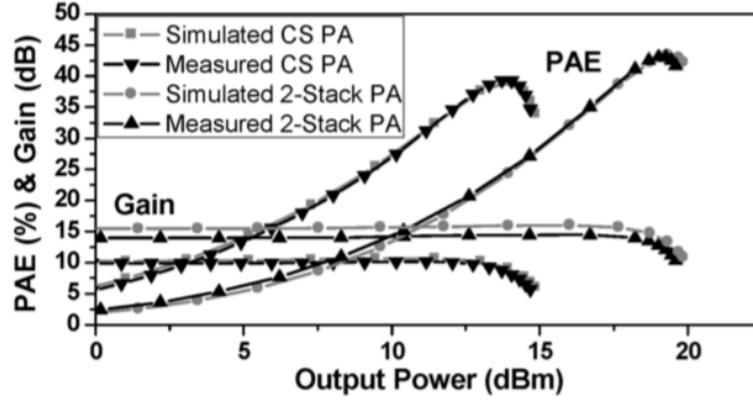


Figure I.3.6: CW performances of common-source and 2-stack PA topologies from [PAR16]

The power amplifier presented in [SHA16], also targeting highly efficient operation for 5G around 30GHz, is implemented in 28nm bulk CMOS technology. It is featuring a 2-stages differential common-source topology as illustrated in Figure I.3.7.

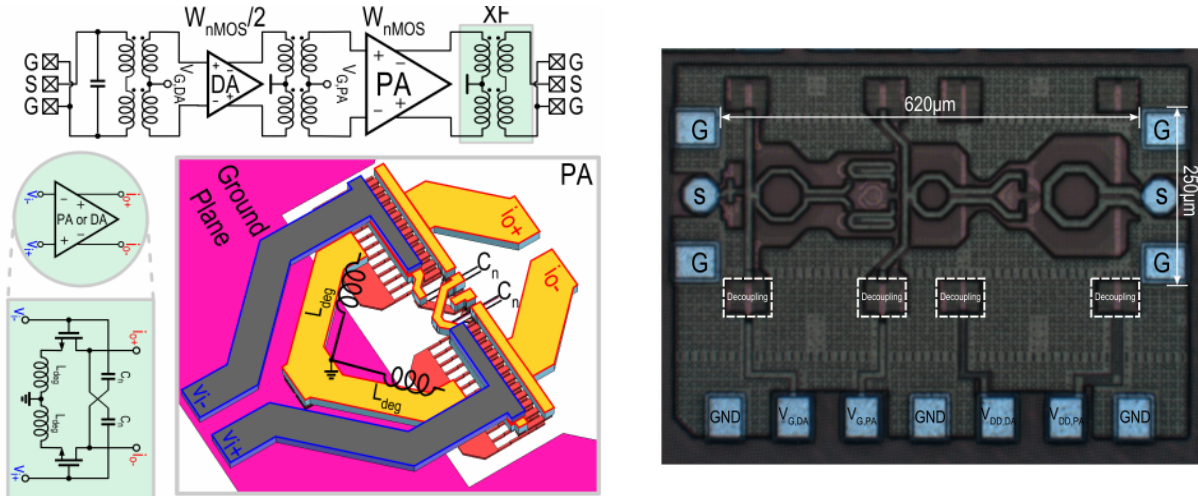


Figure I.3.7: 2-stages differential common-source PA from [SHA16]

The single-ended to differential conversion and impedance transformations at the input and output are realized by baluns while inter-stage matching is performed by a transformer. Center taps are used to apply gate biasing for the two stages. While careful transistors sizing maximizes PAE, Metal-Oxide-Metal (MOM) capacitive neutralization is implemented on both stages to higher the reverse isolation, stability and gain. Furthermore, inductive source degeneration is achieved to broaden inter-stage matching. High peak efficiency of 36.6% is achieved thanks to the design choices and the use of only one amplification path. Compared to power combining, single amplification path allows easier output impedance matching with limited losses. However, this is leading to low output power value of 15.3dBm at saturation under 1.15V

supply voltage. Furthermore, the common-source architecture of the two stages limits the achievable power gain to a maximum of 16.3dB value. The performances of this power amplifier under 1V supply voltage are available in Figure I.3.8.

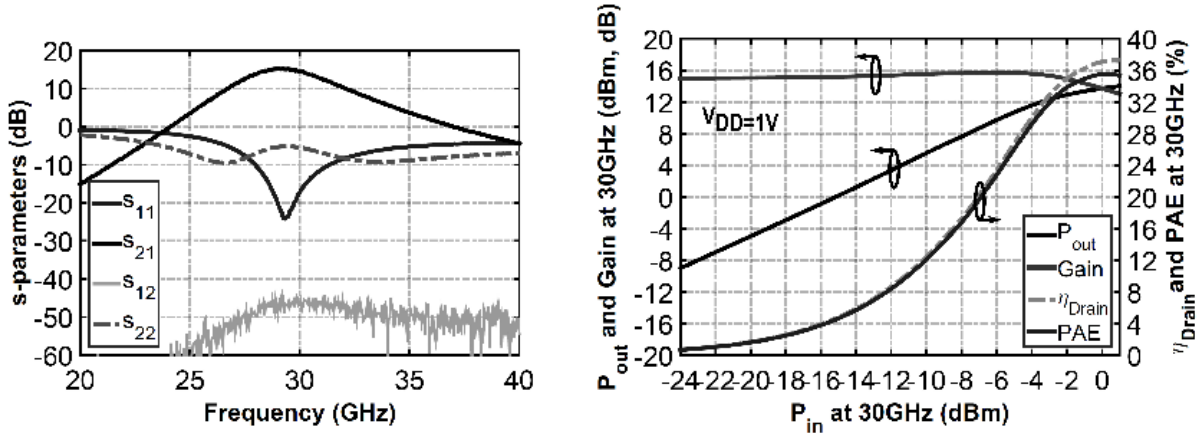
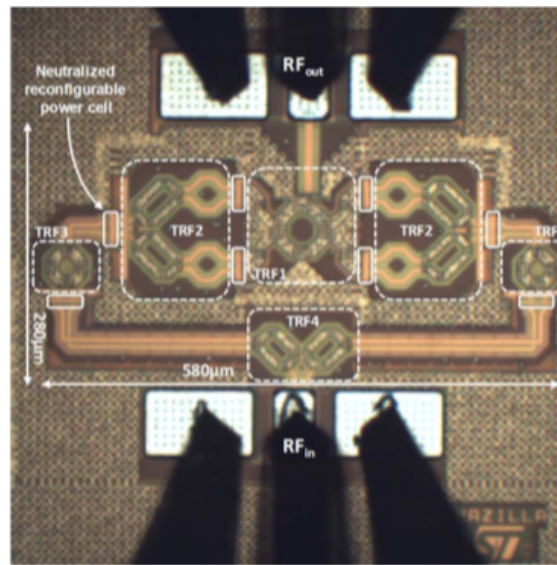


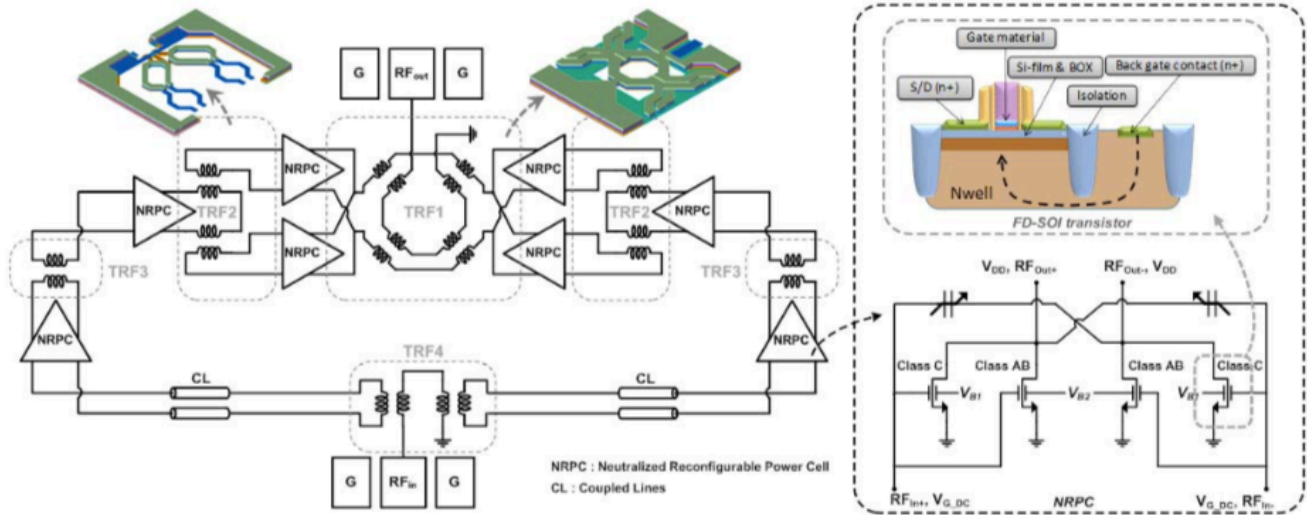
Figure I.3.8: S-parameters and CW performances of 2-stages differential common-source PA from [SHA16]

- Reconfigurable power amplifier at 60GHz

A 60GHz power amplifier designed in 28nm FD-SOI technology is presented in [LAR15]. This power amplifier is featuring a 3-stages topology and two amplification paths. The power-cell used in all stages presents a differential segmented-biased common-source topology allowing pseudo-Doherty operations thanks to transistors body biasing through back-gate contact offered by the technology. Variable neutralization capacitance to increase stability, reverse isolation and gain is also implemented and can be refined to fit any drift induced by manufacturing process. The first two stages are composed by one power-cell. The third stage is composed by two amplification paths. In fact, the inter-stage between second and third stages splits into two differential ways. Therefore, as there are two amplification paths, the output matching network performs impedance matching, differential to single-ended conversion and power combining for 4 differential amplification stages. This is achieved thanks to a DAT. A photomicrograph and a schematic of this amplifier are available in Figure I.3.9 (a) and (b).



(a)



(b)

Figure I.3.9: Power amplifier from [LAR15]: photomicrograph (a) and scheme (b)

This power combining allows high output power levels over 18dBm. The pseudo-Doherty architecture allows highly linear operations and breaks the linearity/consumption trade-off. Furthermore, it is possible to obtain a gain tuning allowing values between 15.4dB and up to 35dB thanks to body biasing with dynamic operating class shifting. However, this mode reconfigurability from a high-linearity mode to a high-gain mode is leading to a PAE_{max} decrease from 21% to 17.7%, a P_{1dB} decrease from 18.2dBm to 15dBm and a power consumption increase from 74mW to 331mW. Furthermore, the 3-stages topology and the output power combining through DAT limits the achievable efficiency at peak and back-off. It is also noticeable that a reduction of supply voltage from 1V to 0.8V allows a mode with lower power consumption in

high-linearity mode, from 74mW to 58mW with reduced RF performances. The performances of this PA are available in Figure I.3.10 for both extreme modes at 60GHz.

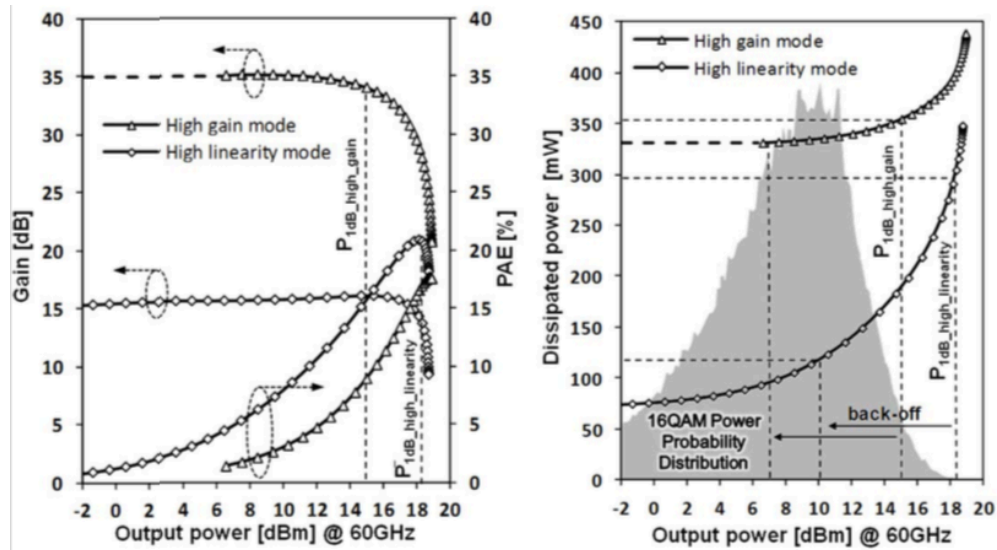


Figure I.3.10: CW performances of the reconfigurable PA presented in [LAR15]

I.3.2 State of the art after circuit design

- Multi-band reconfigurable Doherty power amplifier

The reference [HU17] presents a Doherty power amplifier implemented in 130nm SiGe BiCMOS technology and targeting 5G massive-MIMO applications at 28GHz, 37GHz and 39GHz. A schematic and a photomicrograph of this power amplifier are available in Figure I.3.11.

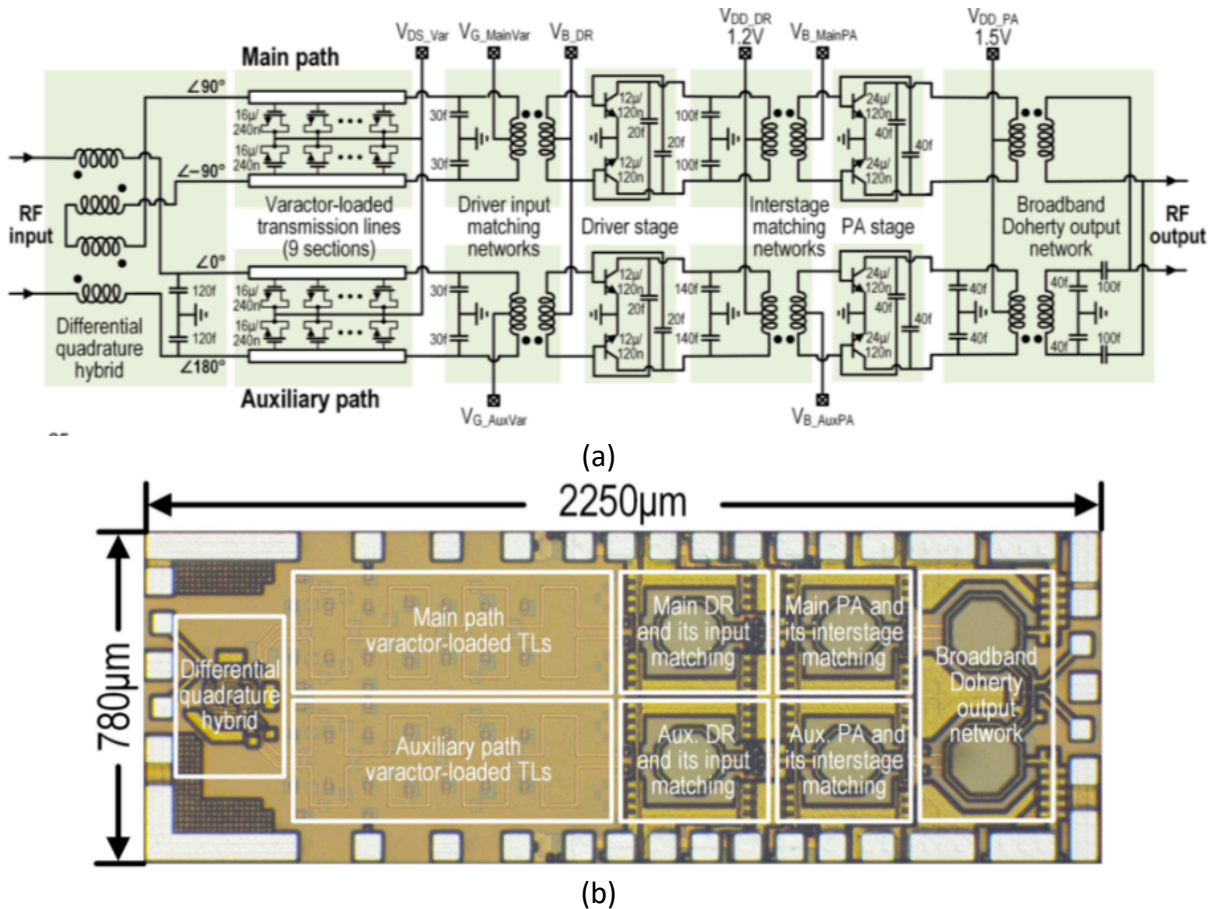


Figure I.3.11: Power amplifier from [HU17]: scheme (a) and photomicrograph (b)

The RF input is splitted by a differential quadrature hybrid, enabling two differential amplification paths (main and auxiliary) while the output combination is realized through a transformer-based Doherty combiner. Compared to a conventional Doherty combiner, the presented topology is more compact, allows an improved passive efficiency at back-off and an enhanced bandwidth due to a reduced transformation ratio. Driver and power stages for both main and auxiliary amplification paths are composed by differential common-source transistors with capacitive neutralization. An adaptive uneven-feeding scheme is implemented to improve back-off efficiency. The multi-band reconfigurability is achieved thanks to adjustable varactor-loaded transmission lines that achieve wideband input matching under different settings.

This power amplifier shows good performances in terms of P_{sat} and $P_{1\text{dB}}$ with respectively 16.8dBm/17dBm and 15.2dBm/15.4dBm at 28GHz/39GHz thanks to Doherty operation. However, the large number of passive devices limits the achievable PAE to 20.3% and 21.4% at 28GHz and 39GHz respectively. Common-source and 2-stages topologies also limit the achievable power gain with values under 18.5dB at all frequencies of operation. This is illustrating that high P_{sat} , PAE, $P_{1\text{dB}}$

and power gain performances over multi-band operations is challenging to achieve. Performances at 28GHz and 39GHz are available in Figure I.3.12.

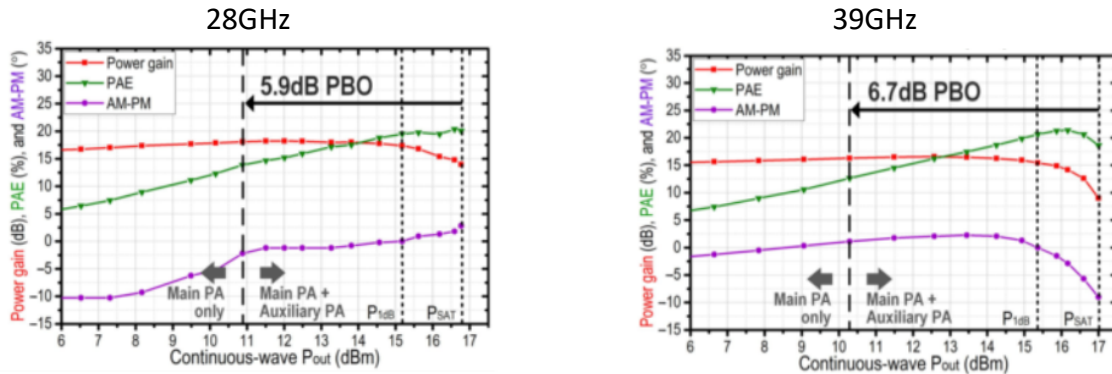


Figure I.3.12: Power amplifier from [HU17], CW performances

- High output power Doherty power amplifier

The 32GHz power amplifier presented in [IND17] and implemented in 28nm bulk CMOS technology is also featuring a transformer-based Doherty topology. In this reference, two Doherty amplifiers are combined at the output. For each single Doherty power amplifier, both main and auxiliary paths feature the following topology. A differential driver stage provides power gain, then the signal is splitted in two differential paths to the power stage composed by two PA unit cells. This PA unit cell is common for both driver and power cell in main and auxiliary paths. It is composed by a differential common-source structure with capacitive neutralization. A photomicrograph and a schematic of this power amplifier are available in Figure I.3.13.

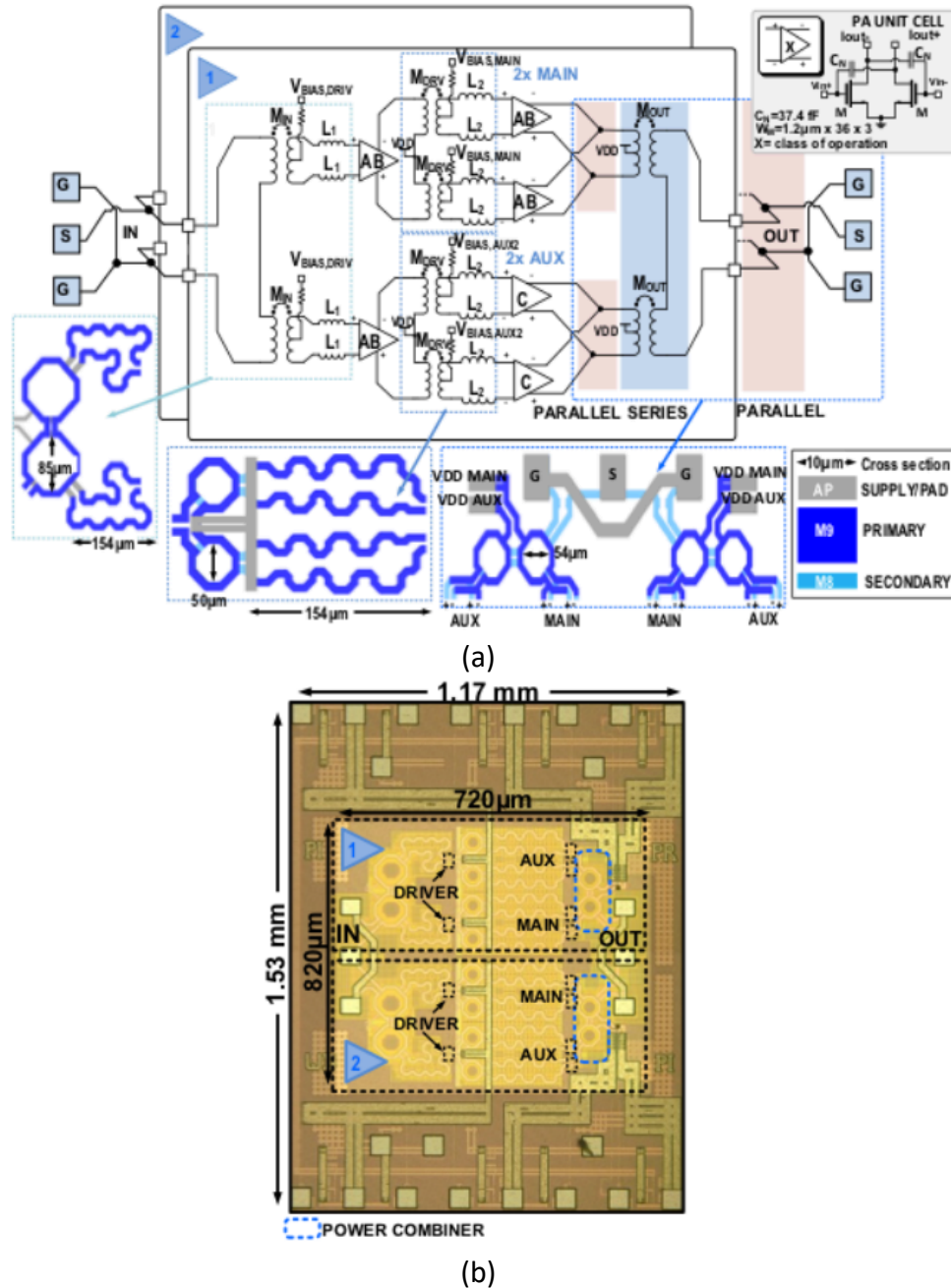


Figure I.3.13: Power amplifier from [IND17]: scheme (a) and photomicrograph (b)

The Doherty architecture of each unitary power amplifier achieves AM-PM compensation for linear operations and also improves the output power. The power combining realized at the output between the two PA provides a high output power with 19.8dBm of P_{sat} under 1V supply voltage with a $P_{1\text{dB}}$ of 16dBm at 32GHz. A good power gain of 22dB is obtained thanks to the

overall topology while the efficiency is limited by the number of passives on the RF path with a peak efficiency of 21%. However, the DC power consumption of the overall power amplifier around 250mW is high for 5G massive-MIMO or small-cells implementation. These performances are available in Figure I.3.14.

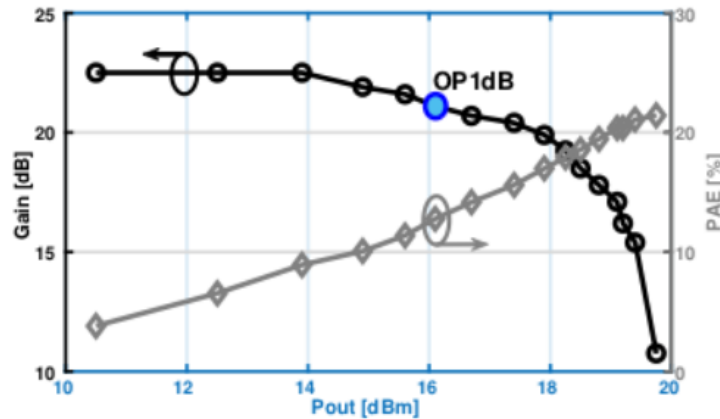


Figure I.3.14: Power amplifier from [IND17], CW performances

- Highly-efficient power amplifiers

The reference [SHA17] presents a power amplifier targeting 28GHz 5G phased-array applications and is designed in 40nm CMOS technology. This power amplifier is featuring a 3-stages differential topology. The driver and power cells differential common-source topologies with neutralization capacitances are inherited from [SHA16] with different stages sizing. A differential digitally tunable gain stage has been added at the input and allows 9 digital gain steps of 1dB, providing a maximum power gain of 22dB. Double tuned transformers are implemented to provide a dual in-band resonance and so widen the bandwidth of the amplifier for wideband linearity.

Like in [SHA16], high efficiency levels are obtained thanks to the sizing of the stages with a peak efficiency of 33.7%. A low power consumption of 30mW is observed. However, in this configuration with only one amplification path and the use of common-source topology, a limited output power P_{sat} of 15.1dBm is achieved. A schematic and a photomicrograph are available in Figure I.3.15 while performances at 28GHz with maximum achievable gain are illustrated in Figure I.3.16.

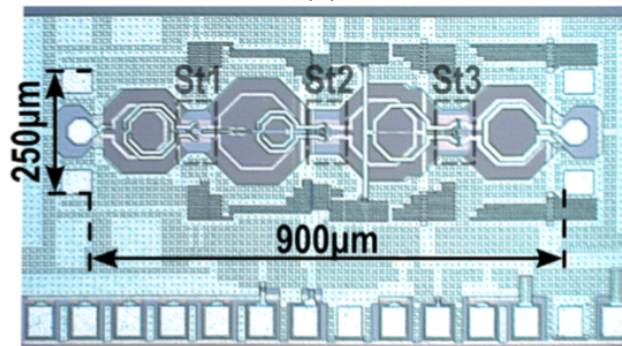
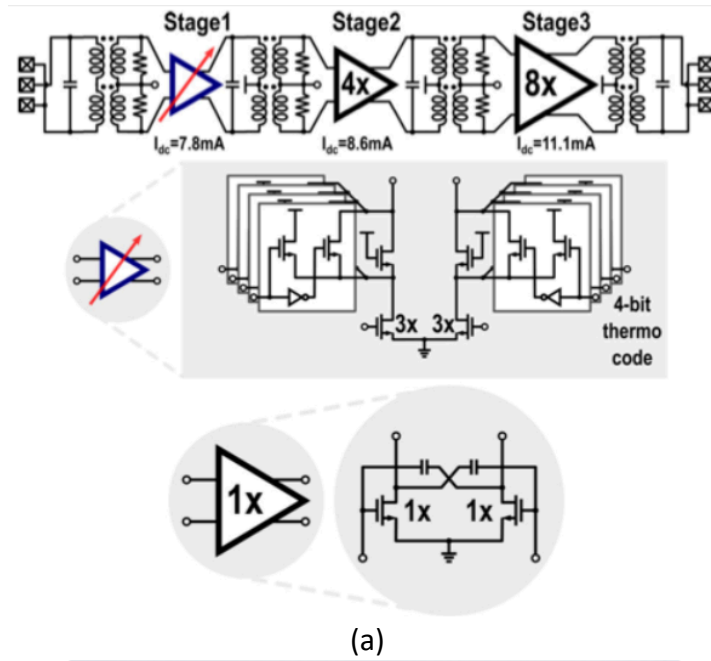


Figure I.3.15: Power amplifier from [SHA17]: scheme (a) and photomicrograph (b)

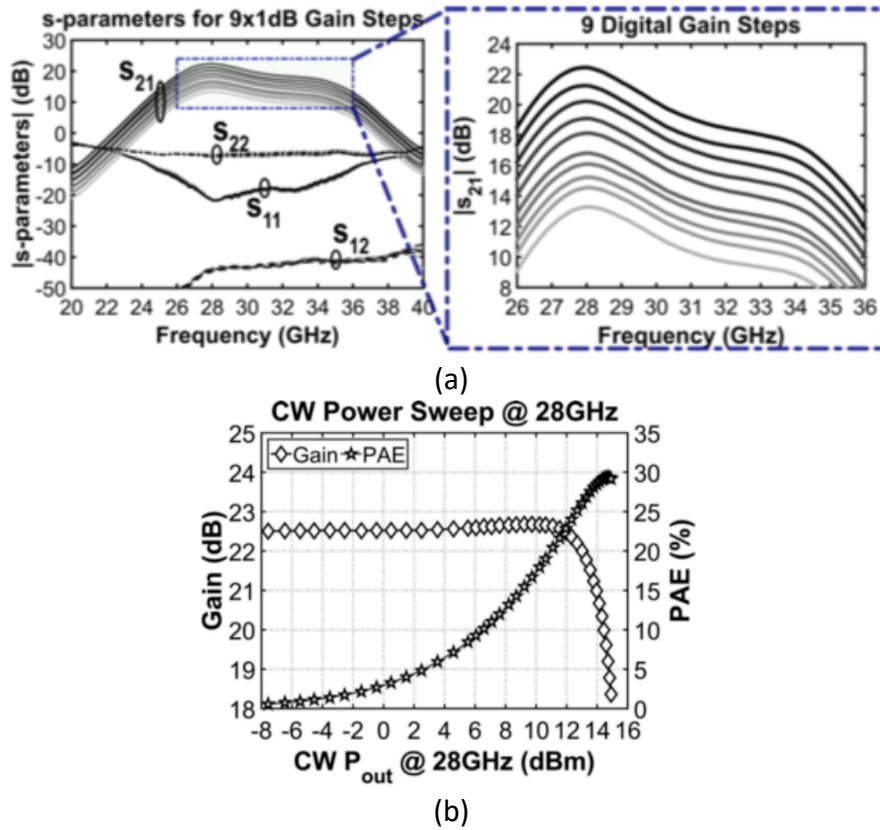


Figure I.3.16: Power amplifier from [SHA17]: S-parameters with reconfigurable gain (a) and 28GHz CW performances (b)

- Self-contained power amplifier

In [MOR17], a power amplifier targeting 28GHz beamforming phased-array applications is implemented in 28nm FD-SOI technology. This power amplifier presents a balanced topology and presents a novel design method for 90° hybrid couplers implementation. Each amplification path is composed by a differential driver stage and two differential power stages. The power stages are all using the same reconfigurable power cell while driver has different sizing and no reconfigurability. This reconfigurable power cell features a differential push-pull configuration in order to enhance AM-AM and AM-PM conversions. Segmented biasing through back gate is performed to provide pseudo-Doherty operation and ensure higher linearity and output power levels. In addition, capacitive neutralization with MOM capacitors is performed to improve reverse isolation and improve the power gain and the stability. The balanced topology also provides output power combining and achieves a P_{sat} of 18.7dBm at 28GHz under 2V supply voltage with a 15.4 dBm P_{1dB} .

Furthermore, a balanced topology is implemented to provide a good VSWR robustness, and for self-contained ability in case of antenna impedance variations. While the 2-stages

topology of each amplification path provides a satisfying gain of 17.5dB, the large number of passive devices for balanced topology implementation, impedance matching and single to differential conversion is leading to low efficiency levels with a PAE_{max} of 12.4%. The power consumption is also high with a 154mW DC value. The topology of this amplifier is available in Figure I.3.17 while the performances are illustrated in Figure I.3.18.

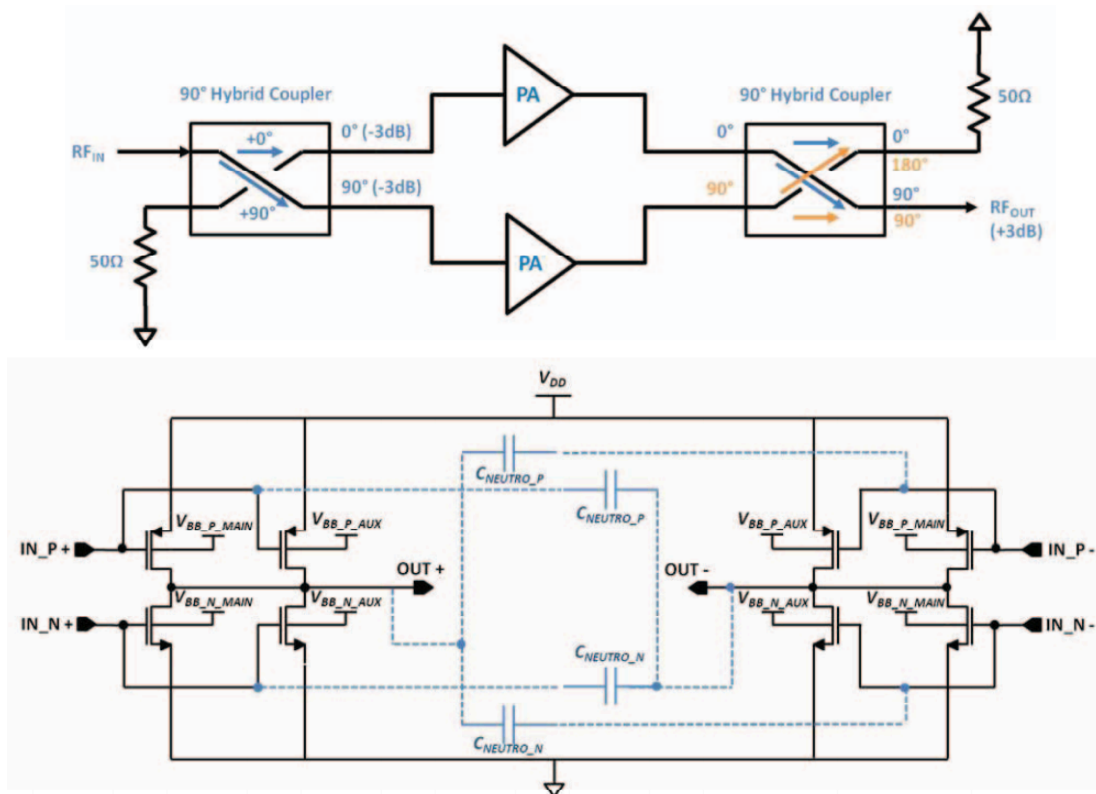


Figure I.3.17: Self-contained power amplifier from [MOR17]: overall and power-cell topology

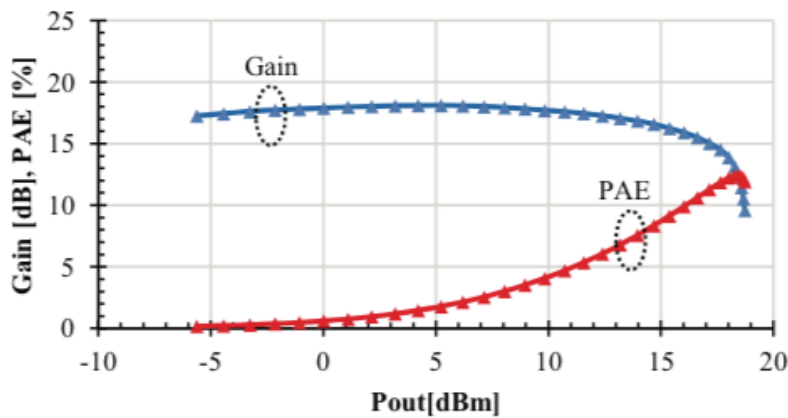


Figure I.3.18: Self-contained power amplifier from [MOR17]: CW performances

- 73GHz power amplifier in advanced 14nm technology node

The reference [CAL17] presents a power amplifier for E-band phased-array applications in 14nm FinFET CMOS technology from Intel. This power amplifier is featuring a 3-stages differential topology. Each stage is designed with differential common-source topology and capacitive neutralization is performed in order to improve reverse isolation and power gain. Each stage is operating in class AB to maximize efficiency at back-off. The matching networks are implemented using baluns and transformers. While the output impedance is matched to higher the efficiency, the others matching networks are designed to improve the power. Careful stage design has been conducted to reduce the layout induced parasitics that could lower the gain and efficiency.

Despite these design efforts, this power amplifier presents low performance levels. The 3-stages common-source topology provides a gain of only 11.9dB while the peak efficiency value is under 9%, incompatible with phased-array 5G requirements. The use of only one amplification path is leading to a maximum output power of 7.4dBm while 1.6dB P_{1dB} is achieved at 71GHz in these conditions. This reference shows that the technology is not enough mature to meet the needs of mmW 5G applications. Figure I.3.19 presents a photomicrograph and a schematic of the circuit while Figure I.3.20 presents the achieved performances.

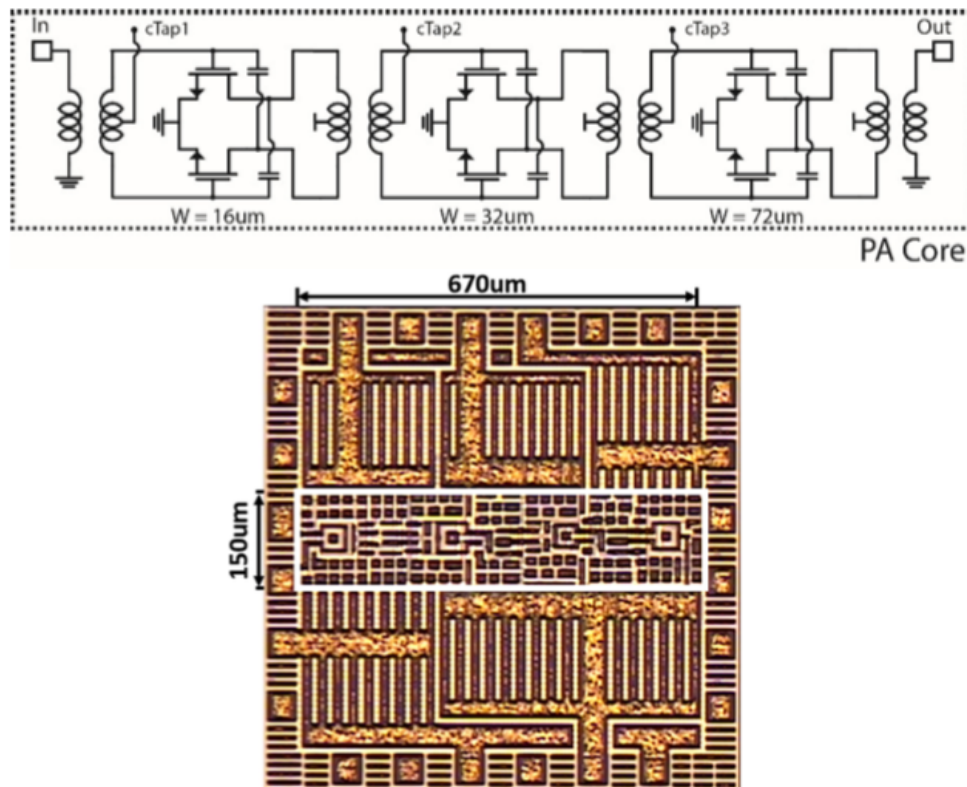


Figure I.3.19: Power amplifier from [CAL17]: scheme and photomicrograph

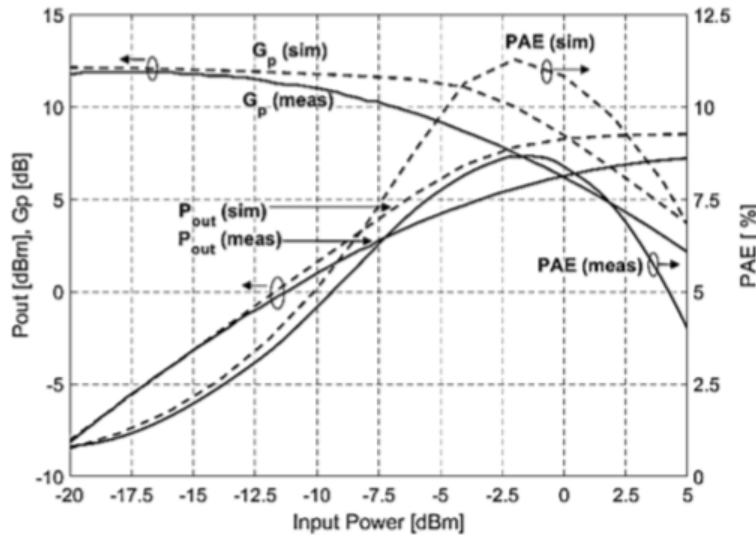


Figure I.3.20: Power amplifier from [CAL17]: CW performances at 71GHz

I.4 Conclusion

In this chapter, an overview over 5G wireless communication network is provided. It is planned for a deployment in 2020 in an exponential mobile market and data volumes growth. Contrary to actual and past wireless networks centered on mobile phone, the 5G will address and leverage new applications in various domains with several degrees of criticality. Therefore, several specifications are available and will depend on the use cases.

To leverage high data-rates, users' densification and network ubiquity, mmW frequencies will be used as a complementary spectrum and several techniques will be deployed to overcome induced limitations and address the 5G challenges. In addition, complex modulation schemes and waveforms for higher spectral efficiency are currently studied by industrials and academics and are still leading to high PAPR values. While CMOS technology allows high integration at low cost compared to III-V technologies, CMOS SOI make possible the co-integration of digital and analog/RF blocks, paving the way for SoC integration that will lower the cost of future communication systems.

An overview of the important parameters and performances of power amplifiers is also provided, including operating classes and parameters related to modulated signals.

The power amplifier remains a bottleneck for SoC integration and 5G power. While high performances are expected regarding output power, efficiency and power consumption levels, the high PAPR induced by modulations and waveforms is leading to stringent linearity requirements. In addition, reconfigurability in frequency and/or mode is also beneficial for SoC implementation. This is defining the thesis context, a power amplifier design for 5G applications in 28nm FD-SOI technology from STMicroelectronics

Finally, a complete state of the art for mmW power amplifiers operating in 5G bands of interest is provided. The state of the art before the circuit design phase of this thesis shows the performances to improve and gives several trends and limitations to overcome. Therefore, it has been possible to define several specifications to achieve with the realized design to improve the state of the art around 30GHz. These specifications are summarized in Table I.4.1 and represent the thesis circuit design goals.

	Targeted specifications at 30GHz
P_{sat} (dBm)	> 17
PAE_{max} (%)	> 30
PAE @ 6dB P_{sat} back-off (%)	> 10
Power gain (dB)	> 16
P_{1dB} (dBm)	> 15
Reconfigurability	Yes

Table I.4.1: Specifications to achieve with the power amplifier designed during the thesis

The state of the art that emerged after the circuit design phase is also important to study and mention, as it targets the same objectives and confirms several trends that we discussed: multi-band, gain reconfigurability, high efficiency, insensitivity to impedance mismatch and advanced technology nodes integration.

Chapter II: mmW PA design methodology in 28nm FD-SOI technology

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Chapter II: mmW PA design methodology in 28nm FD-SOI technology

The power amplifier is the last block of the emitter chain in a transceiver just before the antenna. It is a critical block to design as the performances of the overall transceiver can be degraded if the power amplifier is not well designed. Furthermore, as we exposed in Chapter I, the power amplifier is the most power consuming block in transmission/reception chain and real efforts to push the power consumption into lower levels are necessary for future wireless network and SoC implementation. Nevertheless, power amplifier design at mm-Wave frequencies remains challenging as several effects impacting the performances are occurring with higher frequency. A specific design methodology is needed to avoid design mistakes that could lead to critical dysfunctions. In this chapter we focus on the depiction of a specific approach into design and theory for the implementation of power amplifier targeting future wireless network and SoC implementation in 28nm FD-SOI technology node.

For this purpose, at first, the specificity of the 28nm FD-SOI technology from STMicroelectronics will be discussed. Then the different power amplifier topologies that it is possible to implement will be discussed with reconfigurability and the power cell design will be analyzed.

Impedance matching solutions, passive design and modeling at mmW will then be considered. Several design optimizations to overcome mmW induced undesired effects and stability are then depicted.

Finally, the goal of this chapter is to provide a complete design flow overview for mmW power amplifier implementation in advanced deep sub-micron CMOS technology.

II.1 28nm FD-SOI technology overview

Reconfigurability needs and digital intensive standards in future wireless networks systems drive the need for SoC integration in advanced CMOS technology nodes, as it has been discussed in section I.1.5. This section provides an overview of 28nm FD-SOI technology from STMicroelectronics that has been used in this work.

II.1.1 Active devices

Compared to classical bulk CMOS, the SOI technology is featuring an ultra-thin silicon layer over a buried oxide. In the 28nm FD-SOI technology, the implementation of the buried oxide isolates the channel from the substrate and confines the electrons that are flowing in the channel. Therefore, channel-to-substrate leakage is reduced. The presence of the buried oxide under source and drain eliminates the junction diodes from source and drain to substrate. Thus, it

reduces the parasitic capacitances source-substrate and drain-substrate compared to a bulk CMOS technology. The fully depleted channel made possible by the BOX implantation does not require dopant implementation: this is reducing the number of manufacturing masks and reduces the process variability compared to a classical 28nm bulk technology.

The FD-SOI technology is featuring an additional control by the substrate voltage, the body biasing, that has the ability to modify the threshold voltage, V_T , of the transistors. The body biasing impact is discussed in section II.1.2. A comparative scheme between Bulk and FD-SOI CMOS technology transistors is provided in Figure II.1.1.

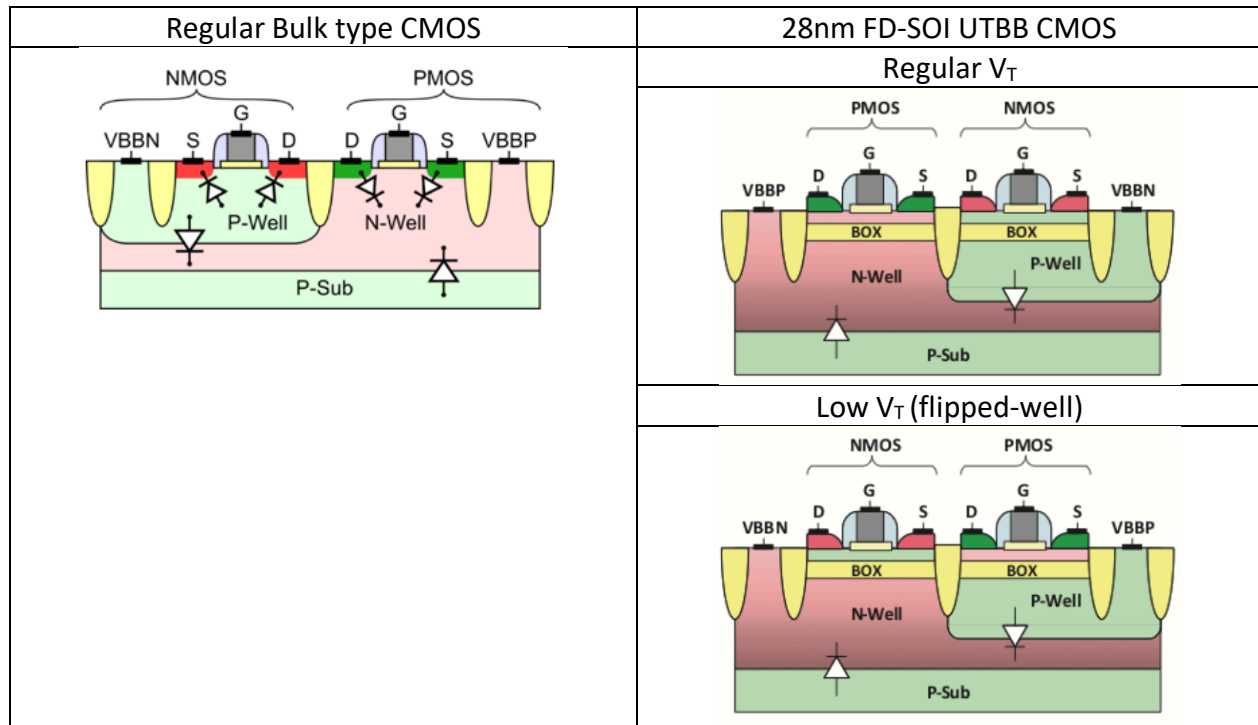


Figure II.1.1: Cross section of regular Bulk CMOS technology VS 28nm UTBB FD-SOI CMOS technology transistors [CAT17]

Two different types of transistor are available in the 28nm FD-SOI technology from STMicroelectronics: the RVT device for “regular V_T ” and the LVT device for “low V_T ”. While the RVT transistors are similar to the bulk devices, the LVT devices are flipped-well transistors. This means that the NMOS transistor is embedded in an N-well while the PMOS transistor is embedded in a P-well, resulting in a triple well implementation. The flipped-well structure is enabling lower threshold voltage values for both NMOS and PMOS devices.

28nm FD-SOI $I_D=f(V_{DS})$ characteristic measurements for several V_{GS} values are reported in Figure II.1.2 from [LAR15-2] and compared with 28nm bulk technology. It is noticeable that for a fixed V_{GS} value, the drain current achieved for all V_{DS} values is way higher in 28nm FD-SOI technology.

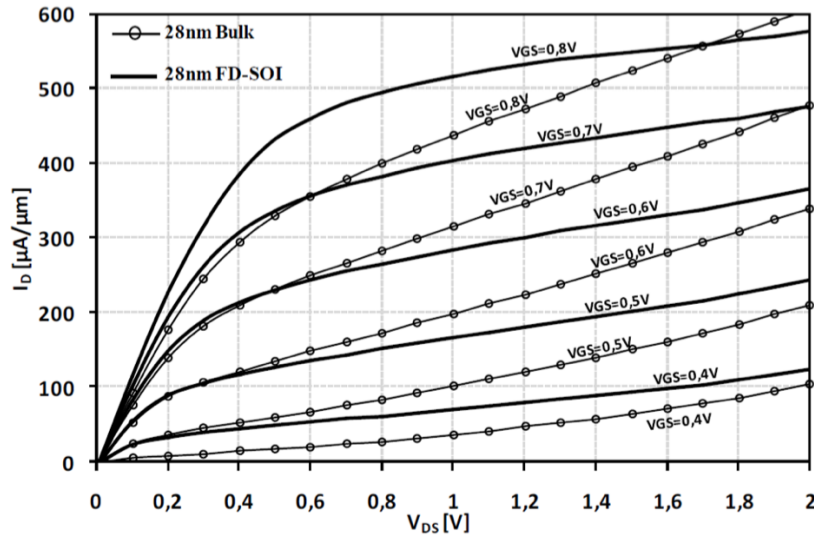


Figure II.1.2: $I_D=f(V_{DS})$ characteristic comparison between 28nm Bulk and 28nm FD-SOI technologies [LAR15-2]

In addition, high values of f_T and f_{max} are reported in 28nm FD-SOI technology with LVT NMOS transistors. For a transistor featuring a gate length of 30nm and 20 fingers of 800nm width, Metal1-Pcell model gives 295GHz of f_T and 394GHz of f_{max} . In [GUI17], f_T and f_{max} of 246GHz and 359GHz respectively have been measured with an optimized BEOL (Figure II.1.3).

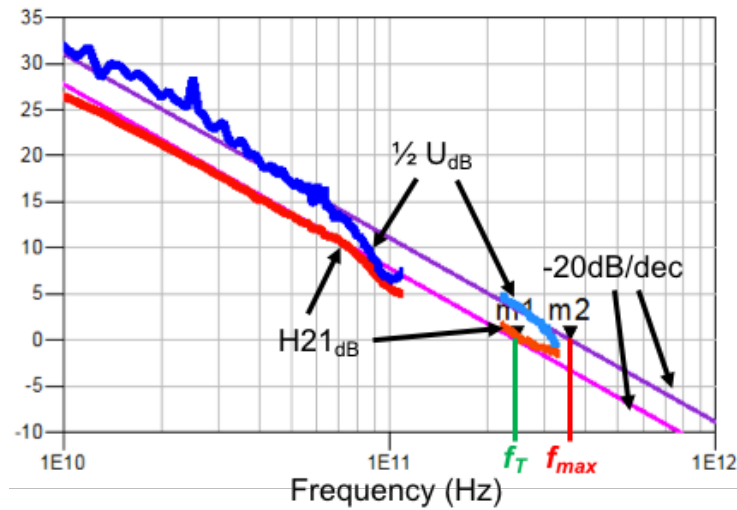


Figure II.1.3: Measured f_T and f_{max} for full BEOL LVT NMOS transistor [GUI17]

II.1.1 Body Biasing

Two types of body-biasing can be applied to the active devices. A forward body biasing, FBB, allowing to reduce the V_T and a reverse body biasing enabling higher V_T level. The maximum FBB and RBB voltage values are limited by the parasitic diodes in the well. A special care must be

taken to keep these diodes in blocked state. Indeed, while an over limit FBB can cause harmful excessive current, an excessive RBB can lead to critical breakdown.

For these reasons, FBB and RBB limits are +3V and -3V for the NMOS device, while FBB and RBB limits are -3V and +3V for PMOS devices. These limits are available in Table II.1.1.

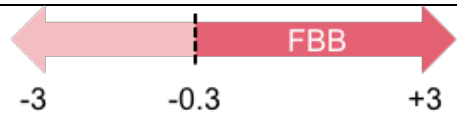
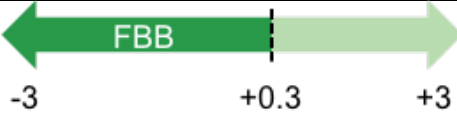
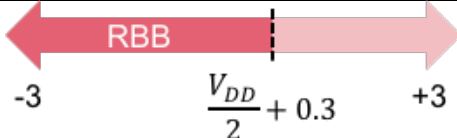
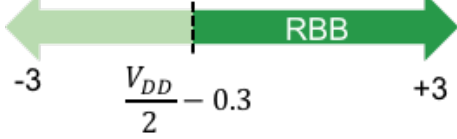
Transistor Type	Biasing mode and limits (V)	Nominal body biasing
LVT NMOS		GND
LVT PMOS		GND
RVT NMOS		GND
RVT PMOS		VDD

Table II.1.1: 28nm FD-SOI CMOS technology transistors body biasing mode, limits and nominal voltage.

While V_T variation can also be achieved in bulk technology through body biasing node, in deep sub-micron CMOS the achievable V_T range is limited to few mV. At the contrary, the 28nm FD-SOI technology can achieve a very large V_T variation over 250mV with the body biasing node. This is illustrated in Figure II.1.4, comparing V_T variations between 28nm bulk and FD-SOI technologies induced by forward body biasing for LVT transistor with minimum gate length.

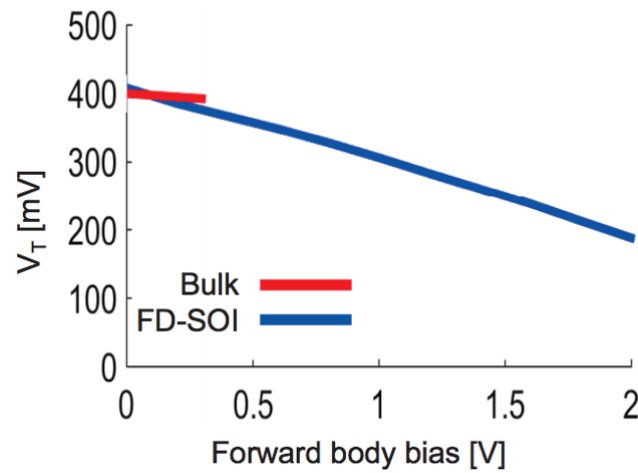


Figure II.1.4: Forward body biasing induced V_T variation comparison between Bulk and 28nm FD-SOI technologies (NMOS) [CAT17]

The Figure II.1.5 illustrates the V_T achievable range by NMOS and PMOS LVT and RVT transistors available in the technology at minimum gate length through forward and reverse body biasing.

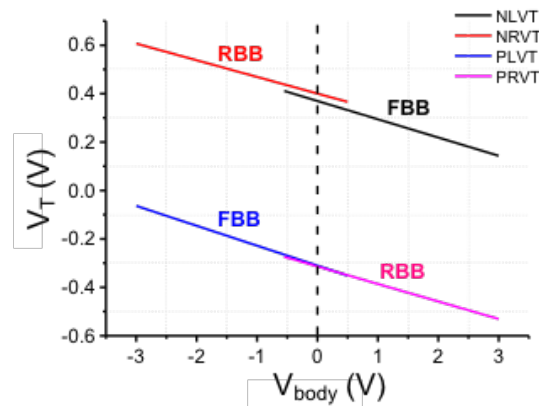


Figure II.1.5: V_T achievable range with NMOS and PMOS LVT and RVT transistors at minimum gate length in 28nm FD-SOI [CAT17]

II.1.2 Back end of line

In addition to the available active devices, the suitability of a technology for RF and mmW design can be determined by exploring the back-end-of-line (BEOL). Indeed, the number of metal layers available, their corresponding thickness and distance from the substrate are very important parameters to take into account for passive devices design and performances enhancement. Two different back-end-of-line are actually available in the 28nm FD-SOI technology. One is featuring

8 metal layers while the other is featuring 10 metal layers, they are named 8ML and 10ML respectively.

The 8 metal layers BEOL is composed by:

- 6 thin copper metal layers of the same thickness, named *M1* to *M6* for metal-1 to metal-6 respectively.
- 2 thick copper metal layers with identical thickness named *IA* and *IB*.
- A thick *AluCap* named *LB*.

The 10 ML stack is featuring two supplementary intermediary metal layers named B1 and B2 that are located between M6 and IA metal layers. The thin metal layers are particularly useful for the routing of digital applications and are not adapted for RF routing. In fact, the very small thickness of these metal levels induces a high resistivity that is not suitable for RF path implementation or passive device design. The RF routing must be designed over thick metal layers *IA/IB* and the *AluCap*. The 10ML BEOL option available in the technology is more adapted for complex RF and mmW routing layout as the intermediary metal layers offer additional levels with lower resistance than *M1* to *M6* and can be used for crossing. However, the passive devices must be designed on *IA/IB* and *AluCap* in all the cases. Another advantage of the 10ML BEOL is that thanks to added intermediary levels, the thick metal layers are more distant from the substrate, reducing the associated capacitance to substrate, and so reducing parasitic capacitances when designing passives and RF routing. For these reasons, we used a 10ML back-end-of-line option for the circuit implemented in this thesis. A scheme of the 10 metal layers stack is available in Figure II.1.6.

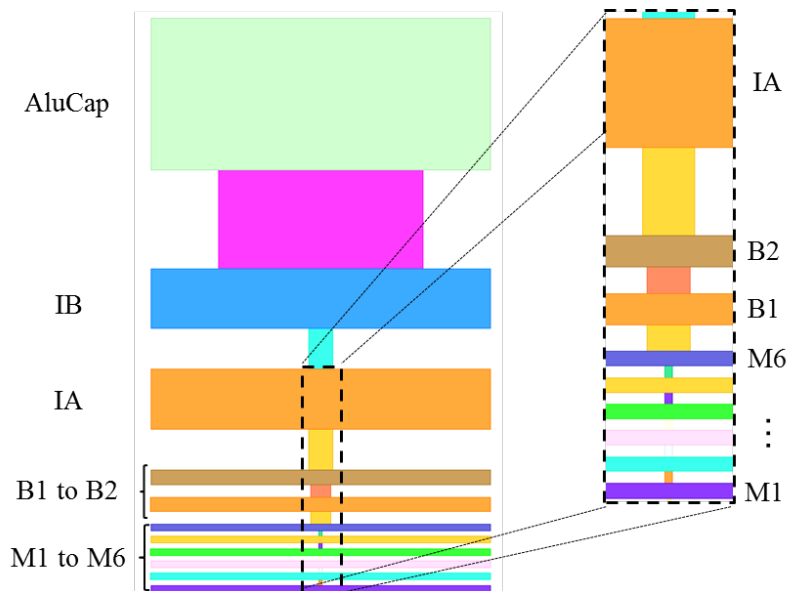


Figure II.1.6: 10 metal layers 28nm FD-SOI CMOS technology back-end-of-line

II.2 Power Amplifiers topologies at mmW frequencies

The first fundamental step in a power amplifier design is to determine its topology. In fact, this choice has to be made carefully, depending on the targeted specifications, the frequency of operation, the technology and the aimed application. These imperatives will lead to several design options for the designer and are discussed in the following sections. In this thesis, we focused on mmW PA design for 5G applications in deep sub-micron CMOS SOI technology for the specifications identified in Chapter I. Therefore, the topology determination and reconfiguration possibilities offered by the technology are discussed.

II.2.1 Choice of operating classes at mmW frequencies

In Chapter I, it has been exposed that 5G wireless communication standard at mmW frequencies will use complex modulations and waveforms. These complex advanced modulations schemes are leading to high PAPR values and necessitate stringent requirements over transceivers linearity. Therefore, the power amplifier must operate in linear operating classes. For this purpose, class A and class AB operations are preferred for this type of modulation as they provide the highest linearity among other classes.

Nevertheless, we also exposed that high efficiency levels and low power consumption are important requirements for 5G network active nodes. While the class A operation provides the highest linearity and gain levels, its efficiency is limited to a theoretical maximum value of 50%, due to the continuous conduction state of the transistors. The class AB operation, with a maximum theoretical PAE of 78.5% is then preferred in recent works [SHA16], [SHA17], [PAR16], aiming for high PAE levels, even if the linearity and gain levels are lower compared to achievable levels in class A.

Class AB is then a good compromise between linearity, efficiency, gain and output power achievable levels for mmW power amplifiers targeting 5G applications. However, the sine operating classes are defined by the biasing conditions. The choice between class A or class AB operation for each PA stage or for the overall power amplifier is then not definitive and can be adjusted during the design process to fit specific needs over performances or circuit behavior that could occur. Finally, the possibility of a dynamic sine operating class switching through body-biasing node is an interesting investigation that is developed in Section II.2.3.

Switched operating classes (class E and F) can achieve higher efficiency as we developed in Chapter I due to the power consumption diminution achieved thanks to output voltage and current waveforms overlap reduction. Therefore, they can appear as a good choice for mmW 5G power amplifiers. However, these classes are suffering from several drawbacks. Indeed, the switching mode of operation of these classes is leading to a low linearity that is not directly compatible with complex modulations and waveforms system implementation. This lack of linearity can be corrected by using external linearization techniques like digital pre-distortion

[CHE09], [LIU11]. However, they are adding design complexity and implementation cost. In addition, external linearization circuits induce a supplementary power consumption and so reduce the efficiency of the overall amplification chain. This is limiting the attractiveness of switched classes. Furthermore, specific harmonic matching through matching networks is necessary to achieve the targeted high efficiency levels. At mmW frequencies, the higher order harmonics are high in frequency and the quality factor of passive devices at high frequency tends to be lowered. Therefore, the expected efficiency levels are harder to obtain. These harmonic matching networks also limit the overall achievable bandwidth [CRI06]. The high frequency harmonic matching requires also technology with high f_T and f_{max} performances. Despite these drawbacks, switched classes remains interesting for mmW 5G applications thanks to the high efficiency achievable and further research is needed to overcome the listed issues.

Recent interest arises for class J operation investigations [CRI06] as it offers high efficiency along with linearity over a wide bandwidth. This class is based on class AB with output voltage and current waveforms engineering. While these features are interesting to achieve in the context of 5G, at the moment no mmW CMOS amplifier featuring the expected high level of performances is available in the literature.

II.2.2 Different implementation topologies available

The first step in power amplifier design is to make a choice regarding the different achievable architectures depending on the identified specification. Three main topologies for power amplifier are available with their respective advantages and drawbacks. These different topologies, single-ended, differential and balanced are discussed in the following section.

- Single-Ended:

Commonly used in the state of the art, single-ended power amplifiers present the advantage to offer an easy and fast implementation with limited area footprint. The absence of balun, transformer, splitting or combining devices prevents the overall power amplifier efficiency drop caused by the losses induced by these elements. Nevertheless, this topology is sensible to ground return path parasitics that can lead to stability issues and so have a critical impact over performances. The use of DC block capacitors over RF path and choke inductance over supply voltage path is mandatory with single-ended design. Electrostatic discharge protection devices should also be inserted in single-ended power amplifier design to prevent any degradation during the manufacturing process and circuit operations. A block scheme of the single-ended topology is provided in Figure II.2.1.

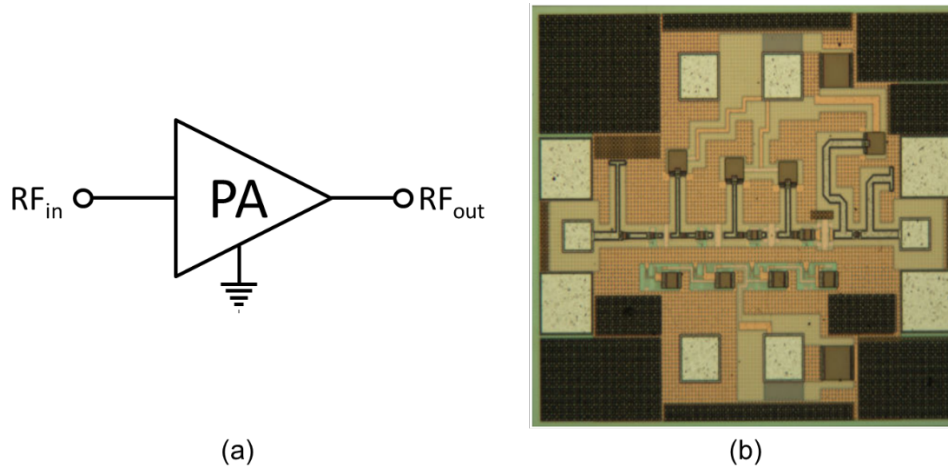


Figure II.2.1: Single-ended topology scheme (a) and implementation example [DEM10] (b)

- Differential topology:

Differential topology, is based on RF input splitting into two identical paths 180° out-of-phase and recombined at the output. Splitting and combining are realized with baluns. This topology presents the advantage of enabling a virtual dynamic ground and so to overcome ground return path induced issues that could be encountered with single-ended design. Power combining at the output provides a 3dB higher output power level. The use of baluns also provides electrostatic discharge protection as the power amplifier core is electrically isolated from input and output pads. Thus, no DC block capacitor over RF path is necessary. It is also possible to use the balun center tap to apply supply voltage or bias, choke inductance is then unnecessary. However, several disadvantages are inherent to differential topology. Losses in the input and output baluns reduce the overall PA performances, especially in terms of efficiency, and have to be limited. Furthermore, a larger area footprint than single-ended topology is reported. A block scheme of the differential structure can be found in Figure II.2.2.

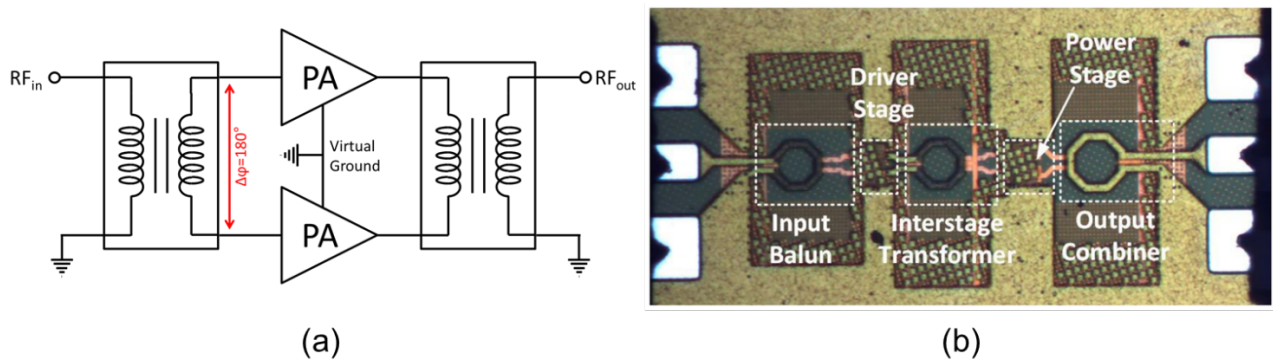


Figure II.2.2: Differential topology scheme (a) and implementation example [XIA17] (b)

Pseudo-differential topology [KER15] is also available. In differential topology, the “common” terminals (source for common-source, and so on) are connected and the corresponding reference is a neutral point. There is a feedback between both “common” terminals. In pseudo-differential topology, the same ground reference is applied over all the circuit, including on both “common” terminals. There is no direct connection or feedback between the “common” terminals and their corresponding reference is the circuit ground. Therefore, there is no virtual ground in pseudo-differential topology. In deep sub-micron CMOS technology, differential topology is preferred as it eliminates the ground path parasitics encountered in pseudo-differential topology.

- Balanced topology

Balanced topology has been used for decades and has been first introduced in [EIS65]. It is based on the use of 90° hybrid couplers to split the RF signal into two identical paths in quadrature and recombined at the output. This topology is made possible in 28nm FD-SOI technology thanks to the recent possibility to implement 3dB 90° hybrid coupler in deep sub-micron CMOS technology [MOR17], [KNO17]. A balanced structure presents several advantages. First, power combining at the output enables 3dB higher saturated output power and output compression power levels. The overall PA gain resulting from this combination is similar to the gain of standalone unitary power amplifier on each path. This structure is also robust in terms of RF input and output port impedance mismatch and make it very attractive for phased array systems implementations where the environment conditions can modify the input and/or output impedances. Reverse isolation, stability and input/output matching are also improved. Another interesting advantage is the linearity enhancement due to 90° hybrid coupler use as combiner and has been demonstrated in [MOR17-2] and that is developed in Section II.7.1. This linearity enhancement is featuring 6dB in-band 3^{rd} order intermodulation product and 9dB 2^{nd} order intermodulation product reductions and off-band 3^{rd} order intermodulation product cancellation. However, several drawbacks are noticeable with this topology. The losses introduced by the coupler can dramatically reduce the overall PA efficiency and have to be limited. Traditionally, the area footprint is larger than the two other presented topologies, single-ended and differential. However, recent improvements in 90° coupler design allow to adapt the coupler geometry to available surface for a pragmatic design approach [KNO17]. A block scheme of the balanced amplifier is available in Figure II.2.3.

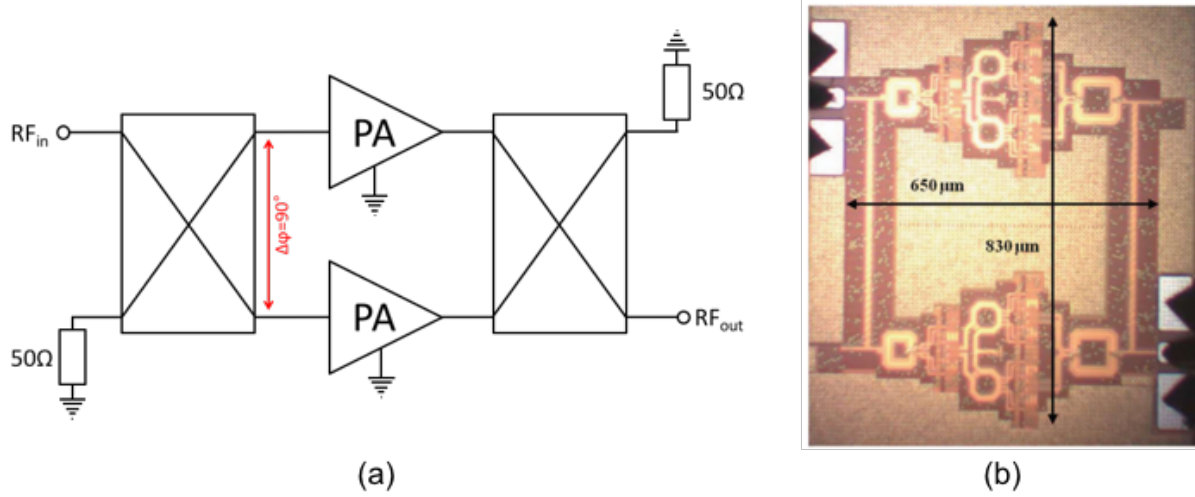


Figure II.2.3: Balanced topology scheme (a) and implementation example [MOR17] (b)

- Multi-stage topology

If the gain of the chosen amplification stage is not sufficient for the targeted application, it is possible to cascade several amplification stages. This is the principle of multi-stage amplifier design. It is possible to implement multi-stage amplifiers for all type of topology depicted previously, all amplification paths can be composed by several stages.

Ideally, the overall gain of a N -stage amplifier (Figure II.2.4) is the sum (in dB) of all the gain provided by each stage (II-1).

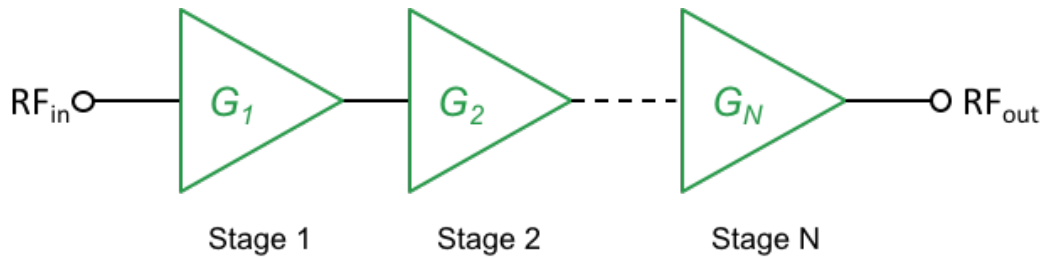


Figure II.2.4: Ideal multi-stage amplification path

$$G_{overall} (dB) = \sum_{i=1}^N G_i (dB) \quad (II-1)$$

However, the amplification stages cannot be directly connected and lossy matching networks must be inserted between stages (Figure II.2.5), as it is developed in Section II.4.1. Therefore, the losses introduced by the matching networks reduce the overall amplification path gain (II-2).

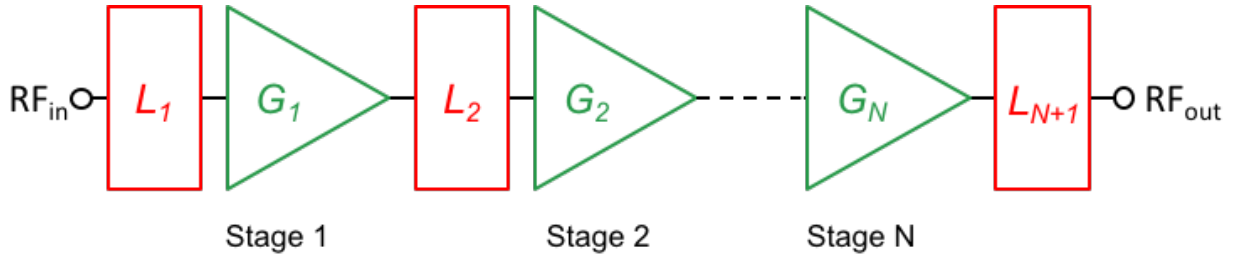


Figure II.2.5: Multi-stage amplification path with lossy matching networks

$$G_{overall} (dB) = \sum_{i=1}^N G_i (dB) - \sum_{i=1}^{N+1} L_i (dB) \quad (II-2)$$

More than a gain diminution, the losses introduced by matching networks are leading to an efficiency reduction. Therefore, a trade-off appears between the number of stages necessary to achieve the targeted gain and the overall PAE diminution caused by the matching networks.

II.2.3 Power amplifier reconfigurability discussion

In Chapter I, we pointed at the necessity and advantages of power amplifier reconfigurability for 5G applications and SoC control implementation. Several reconfigurability types are possible depending on the fixed objectives. In [HU17], varactor loaded lines allow the power amplifier reconfiguration for frequency band switching. In [LEH07], switched PA configuration allows several saturated output power modes and propose lower power consumption for lower power modes.

In this section we focus on the reconfigurability that can be implemented by using 28nm FD-SOI body biasing node. A back-gate enabled reconfigurability is interesting to explore because it does not add supplementary stage or complexity to an existing design.

Power amplifier reconfigurability through body biasing node has been explored in [LAR15]. In this reference, the body bias is used to implement pseudo-Doherty operations. In fact, this is possible because of the body biasing effect over V_T , as we exposed in section II.1.3. The V_T variation allows dynamic current density modification for a fixed gate bias condition. To illustrate the operating class choice by gate biasing, Figure II.2.6 presents $I_D=f(V_{GS})$ curves of a LVT NMOS transistor with 30nm gate length and 50 fingers of 1 μ m under 1V supply voltage, showing class A and class AB corresponding bias.

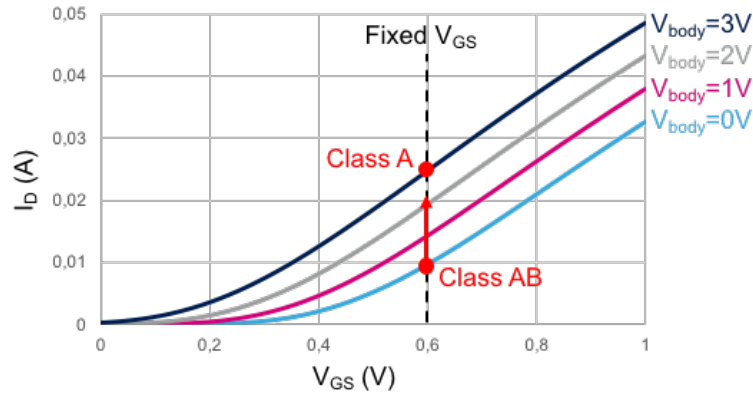


Figure II.2.6: Operating class shifting induced by body biasing

In [LAR15] and [MOR17], this ability allows to bias all the transistors for class C operations while the V_T variation through body biasing over “main” transistors enables class AB operation. Then, body biasing over “auxiliary” transistors allows a high-gain mode, enabling class A operations for all devices [LAR15]. This pseudo-Doherty operation is illustrated in Figure II.2.7.

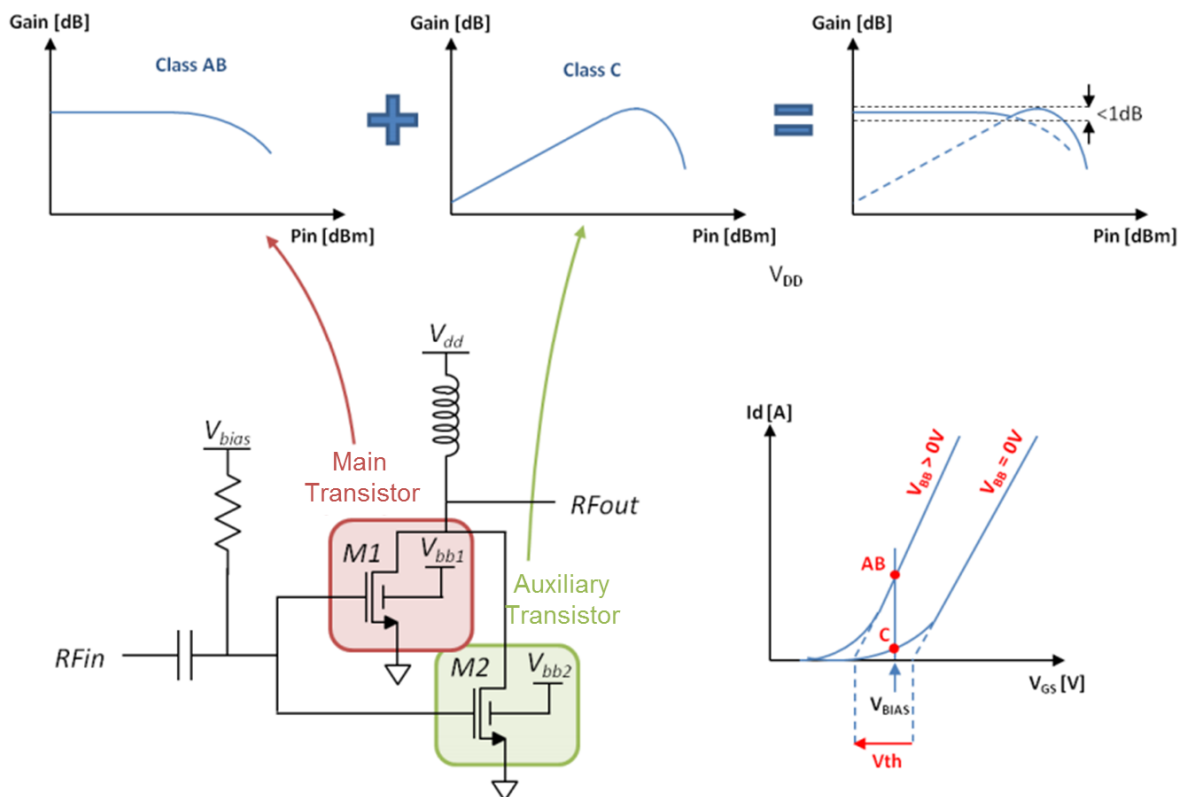


Figure II.2.7: Body-biasing enabled pseudo-Doherty operation [MOR17-2]

In other context than pseudo-Doherty implementation, the V_T variation presents advantages for reconfigurability thanks to dynamical operating class modulation.

Let's focus on a common-source topology to illustrate this behavior. For a common-source transistor in saturation loaded by R_L and fed by an ideal voltage source, the small-signal voltage gain is given by (II-3).

$$A_v = -g_m(r_o // R_L) \quad (II-3)$$

Where r_o is the MOS device output resistance, R_L the load resistance and g_m the transconductance with λ the channel length modulation parameter (II-4).

$$g_m = \frac{W}{L} \cdot \mu_n \cdot C_{ox} \cdot (V_{GS} - V_T) \cdot (1 + \lambda V_{DS}) \quad (II-4)$$

Therefore, the gain amplitude is determined by g_m parameter. Two solutions easily appear to obtain higher gain for fixed V_{DS} and transistor geometrical parameters:

- The classical solution is to use higher gate bias V_{GS} in order to reach higher gain in higher operation class.
- The body biasing enabled V_T diminution that provides dynamical operation class shifting.

As both solutions induce the same effects over g_m , it is interesting to highlight the advantage of using body-biasing for gain enhancement instead of classical V_{GS} improvement.

In Figure II.2.8, $I_D=f(V_{GS})$ curves of a LVT NMOS transistor with 30nm gate length and 50 fingers of $1\mu\text{m}$ for a V_{DS} of 1V are plotted to highlight the V_{GS} and V_{body} variations needed to achieve a fixed I_D level.

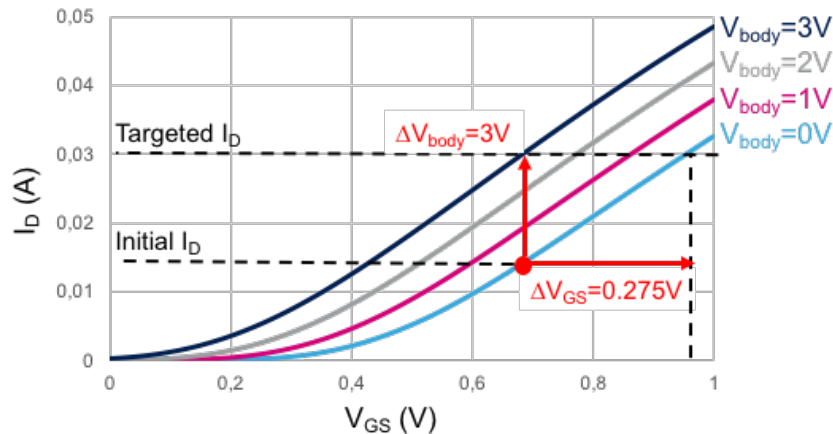


Figure II.2.8: V_{GS} and V_{body} dynamic comparison for fixed I_D level target

As it is noticeable, if we want to achieve a higher fixed I_D level from an I_D and V_{GS} reference, two solutions are possible. The V_{GS} value can be improved by 275mV while the body biasing can be set to 3V to reach the same I_D level. This means that a small variation of V_{GS} is leading to a large drain current variation while body biasing dynamic is higher. Therefore, the wide dynamic

possible through body biasing node allows a very fine tuning of operating class. This is enabling continuous class shifting with easily reachable intermediary modes. Simulations have been conducted for the power amplifier presented in Chapter III to illustrate this effect. For similar operating conditions, a 100mV V_{GS} increase is leading to a 6.7dB gain variation while 100mV increase of body biasing is leading to a 0.8dB power gain improvement. This is illustrating the fact that the body biasing node in this technology enables both dynamic fine continuous class switching and fine grain control with no additional stage or additional design complexity.

In addition, we saw in the previous section that multi-stage topology enables interesting performance enhancement possibilities. In the following paragraph, reconfigurability in multi-stage amplifier is discussed.

In multi-stage PA, for reconfigurable operation in 28nm FD-SOI technology using body biasing, a question may arise: In which stage the body-biasing should be implemented? In a multi-stage amplifier each stage must be linear enough to not degrade the linearity of the next stage. Therefore, acceptable overall linearity performances can be achieved. Practically, this means that the 1dB output compression point of each stage must be higher than the 1dB input compression point of the following stage. However, the use of body-biasing to increase the gain has a negative impact on linearity and has been observed in measurements provided in Chapter III. Thus, it is more benefic to implement the reconfigurability through body biasing on the last stage of the amplifier, generally the power stage, to limit the induced linearity deterioration caused by the saturation of previous stages.

II.3 Power cells topologies at mmW frequencies

After the determination of adequate power amplifier topology for targeted application, the next step is to make a choice between the different stage topologies and is explored in the following paragraph.

II.3.1 Common-source topology

In common-source topology, the RF input is applied on the transistor Gate and the RF output is connected to the Drain. A figure of this structure is provided in Figure II.3.1. This topology, by its apparent simplicity, allows a fast and easy implementation. A great linearity is achieved thanks to the high voltage sweep achievable at the output, up to 2 times V_{DD} in class A. Nevertheless, this topology is sensitive to the parasitic elements. C_{DS} capacitance is leading to lower gain level because of output impedance lowering. Indeed, to achieve high power gain, wider transistors are necessary, but wider transistors lead to higher C_{DS} value that is responsible of the decrease of output impedance. Low output impedance is an issue for output matching as it can be difficult to synthesize and can necessitate high impedance transformation ratio at the output. Another drawback of this structure is the effect of C_{GD} parasitic capacitance that, coupled with

Miller effect discussed in Section II.7.2, acts as a return path. This lowers the power gain and causes stability issues while reducing the bandwidth.

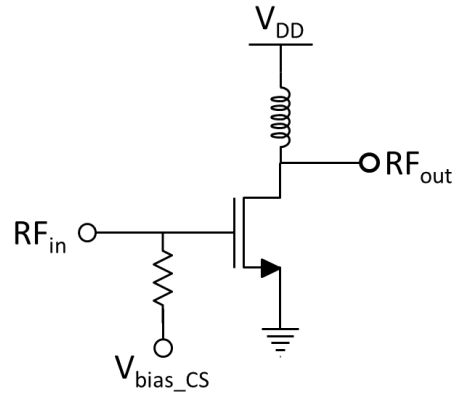


Figure II.3.1: Common-source topology scheme

To overcome the potential stability issues on common-source stages, several techniques can be used and are illustrated in Figure II.3.2:

- A RC circuit on the common-source transistor gate is lowering the gain at low frequency. The dimensioning of these elements must ensure sufficient gain at the desired frequency of operation simultaneously with low insertion losses.
- The degeneration inductance on the common-source transistor source, lowering the overall gain of the amplifier and allowing higher stability. While this technique is commonly used for low noise amplifiers design, it can also be used for power amplifiers [SHA16].

It is also possible to enhance the stability of differential common-source stages by using capacitive neutralization of Miller capacitance, this technique is depicted in Section II.7.2.

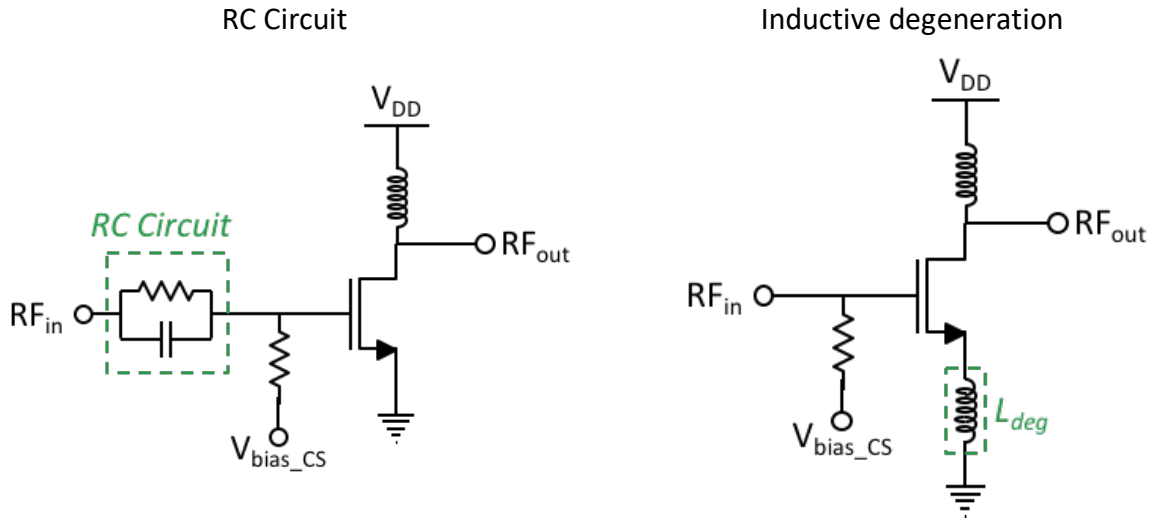


Figure II.3.2: Common-source stabilization techniques

II.3.2 Cascode topology

Cascode topology consists in introducing a transistor in common-gate configuration at the Drain terminal of a common-source transistor. With this topology, input and output are isolated. Hence, Miller effect is reduced for both transistors and so higher power gain and bandwidth are achievable with an improved stability. Higher output power level is also achievable. In fact, in cascode configuration, maximum output voltage swing is shared between the CG and CS transistors. This allows the use of higher supply voltage, leading to higher output power. A schematic view of cascode topology is presented in Figure II.3.3.

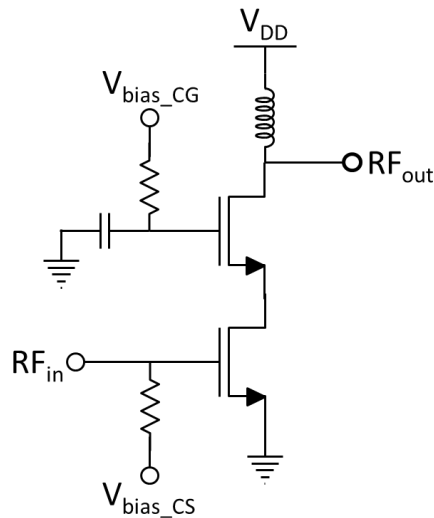


Figure II.3.3: Cascode topology scheme

However, this structure is sensible to parasitics and especially the ones introduced by the connection between the two transistors and must be minimized in layout. In classical CMOS technology, the parasitic capacitance between this node and the substrate is critical and has to be reduced as it creates signal leaking in the substrate at high frequencies and so reduces the overall gain of the structure. Generally, a matching between the two stages can be inserted [GU12], [YEH12]. However, with the 28nm FD-SOI technology, the SOI configuration shields the substrate and the high resistivity of the substrate naturally reduces the C_{sub} parasitic capacitance. Therefore, only parasitic inductance and resistance must be reduced at this node by using wide routing on top thick metal layers offered by the technology. These parasitic elements are illustrated in Figure II.3.4.

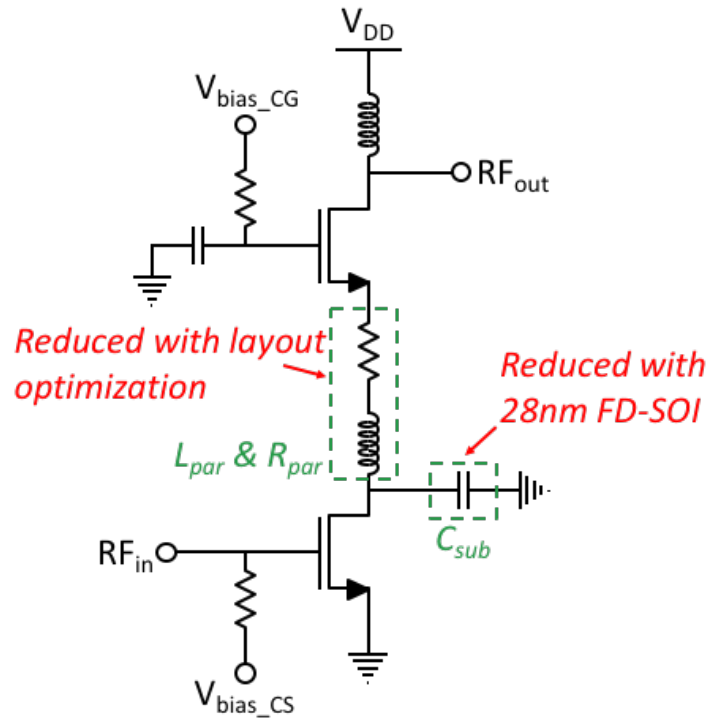


Figure II.3.4: Cascode inter-stage parasitic elements illustration

It is also possible to stack more transistors like in [JAY16]. As for the cascode configuration, the voltage swing is distributed over all stacked transistors. Therefore, it is possible to use a higher supply voltage leading to higher output power and PAE levels. Nevertheless, the high supply voltages used in stacked configuration generally result in high power consumption that is prohibitive for applications like 5G, where dissipated power must remain limited.

II.4 Impedance matching

Impedance matching is an important step in any power amplifier design flow. Indeed, the impedance must be carefully determined and designed to enhance the power amplifier performances. In this section, we provide general theoretical aspects of impedance matching. We also explain how to determine practically the optimum impedance values during design process. Finally, we provide the specific matching network topologies that it is possible to implement at mW frequencies.

II.4.1 Theoretical aspects

The main purpose of impedance matching is to determine and synthetize the impedances that maximize the power transfer between source, stages and output of a power amplifier to reach the best performances. In this section, we provide theoretical aspects of impedance matching to highlight its importance and how to determine the right impedances that make the designed stage operating at its fullest potential.

First of all, to better illustrate the role of load impedance in power transfer, let's consider a simple active source (V_S ; Z_S), loaded by a passive load Z_L .

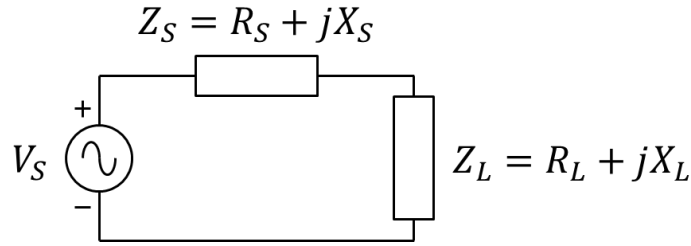


Figure II.4.1: Active source loaded by a passive load scheme

The power absorbed by the load is:

$$P_{load} = \frac{1}{2} \cdot \text{Re}(V_L \cdot I_L^*) \quad (II-5)$$

$$P_{load} = \frac{1}{2} \cdot \text{Re} \left[\left(\frac{V_S \cdot Z_L}{Z_S + Z_L} \right) \cdot \left(\frac{V_S}{Z_S + Z_L} \right)^* \right] \quad (II-6)$$

$$P_{load} = \frac{1}{2} \cdot |V_S|^2 \cdot \frac{R_L}{|Z_S + Z_L|^2} \quad (II-7)$$

$$P_{load} = \frac{1}{2} \cdot |V_S|^2 \cdot \frac{R_L}{(R_S + R_L)^2 + (X_S + X_L)^2} \quad (II-8)$$

To maximize P_{load} , the denominator $(R_S + R_L)^2 + (X_S + X_L)^2$ must be minimized. It is possible to eliminate the term $(X_S + X_L)^2$ for

$$X_L = -X_S. \quad (II-9)$$

Then the term $(R_S + R_L)^2$ has to be reduced. It can be developed and factorized by R_L to give:

$$(R_S + R_L)^2 = \frac{R_S^2}{R_L} + 2R_S + R_L \quad (II-10)$$

To find the minimum of this function, its derivative must be equal to zero,

$$\frac{d}{dR_L} \left(\frac{R_S^2}{R_L} + 2R_S + R_L \right) = 0 \quad (II-11)$$

$$R_L = \pm R_S \quad (II-12)$$

To verify if this solution corresponds to a minimum, the second derivative of (II-10) has to be calculated and its sign has to be explored.

$$\frac{d^2}{dR_L^2} \left(\frac{R_S^2}{R_L} + 2R_S + R_L \right) = \frac{2R_S^2}{R_L^3} \quad (II-13)$$

This function is always positive for any positive value of R_S or R_L corresponding to the only physical solution of (II-12). The solution $R_L = R_S$ is then a minimum of (II-11).

The power absorbed by the load is thus maximum for

$$Z_L = R_S - jX_S = Z_S^* \quad (II-14)$$

As the maximum theoretical power transfer is corresponding to the maximum delivered power by the source, we can write from (II-8)

$$P_{load_max} = P_{source_max} = \frac{1}{2} \cdot |V_S|^2 \cdot \frac{R_S}{|Z_S + Z_S^*|^2} \quad (II-15)$$

Leading to a theoretical maximum power transferred from source to load

$$P_{load_max} = \frac{1}{8} \cdot \frac{|V_S|^2}{R_S} \quad (II-16)$$

However, from a physical side in an implementation, the circuits terminations, antennas, measurement instruments impedances are rarely equal to the complex conjugate of the PA input/output. Generally, 50Ω terminations are encountered. This is also the case between two

amplification stages, where the input of the follower stage is rarely equal to the complex conjugate of the previous stage output. Thus, a direct connection could lead to critical performance degradation. Therefore, a matching network must be inserted to transform the impedances and so match the inputs and outputs to achieve the highest power transfer.

The matching network principle is illustrated in Figure II.4.2. The input impedance of the matching network, Z_{in} , is matched to the source impedance Z_S . Meanwhile, the output impedance of the matching network, Z_{out} , is matched to the load impedance Z_L .

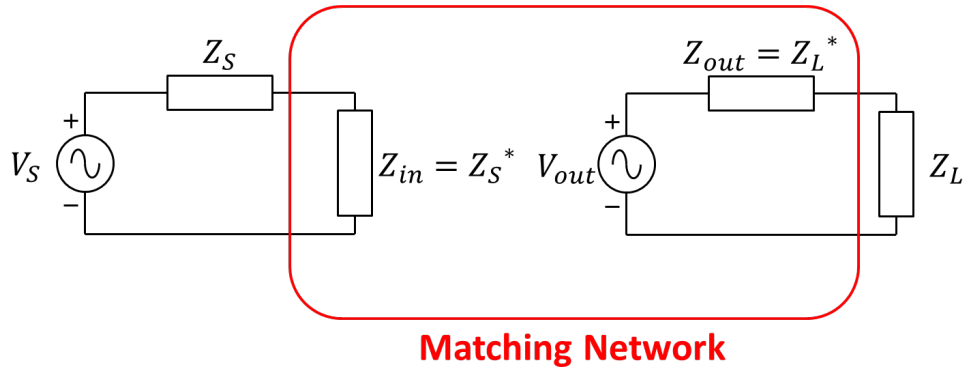


Figure II.4.2: Matching network illustration

As $Z_{in} = Z_S^*$ and $Z_{out} = Z_L^*$, both source and load are matched and a maximum power transfer is theoretically obtained. However, in practice, the introduction of a matching network generates losses and so the maximum output power achievable is:

$$P_{load_max_ach} = P_{load_max} - L_{MN} \quad (II-17)$$

Where L_{MN} the losses induced by the matching network.

Let's now consider a generic power amplifier featuring two stages as illustrated in Figure II.4.3. Matching networks must be introduced at the input and output of the power amplifier and also between power stages to ensure a maximum power transfer through the overall power amplifier.

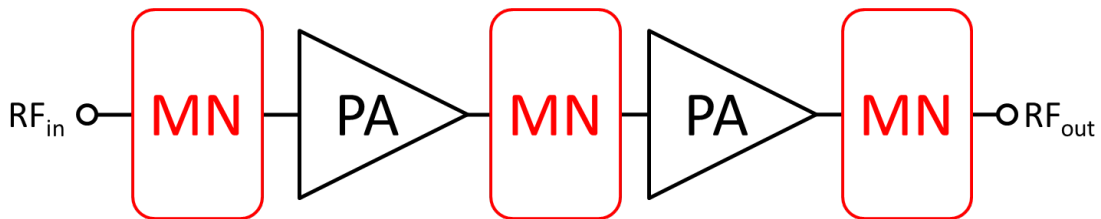


Figure II.4.3: Generic power amplifier scheme with matching networks at the input, output and inter-stage

The optimal input and output amplifier and stages impedances are essential to determine before designing corresponding matching networks. It is possible to conduct two distinct analysis through simulation software: the load-pull for optimum load determination and source impedance sweep for optimal source impedance determination. These analyses are mandatory to find the impedances leading to maximum targeted performances.

- Load-pull:

The load-pull is a nonlinear characterization method. It consists in the variation of the output termination load of the device under test, DUT, for fixed operating conditions concerning biasing, input power and frequency of operation. While the output load is varied, performances like PAE, output power and gain are calculated, depending on the desired parameter optimization. It is then possible to draw the desired performances contours into the Smith Chart: the optimal impedance regarding targeted performances can be determined. Load-pull simulation schematic and Smith Chart performance contour examples are available in Figure II.4.4.

In laboratory, load-pull measurements can be done using impedance tuner and allow characterization of power amplifiers and transistors to extract the optimal performances while varying output load impedance along with biasing and frequency conditions on a test bench.

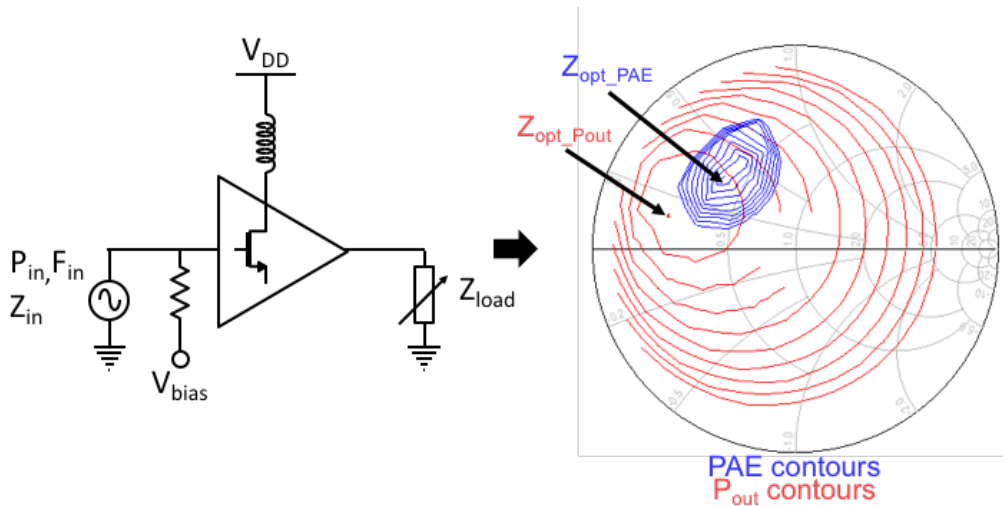


Figure II.4.4: Load-pull setup and results illustration

- Source impedance sweep:

In simulation tools, it is not possible to perform a source-pull analysis to define the optimal source impedance. Another method is used. It consists in sweeping R_s and X_s alternatively during a harmonic balance simulation, for fixed bias and frequency conditions while input power can also be swept. Gain, output power and PAE or any other targeted performance can be calculated and plotted in order to determine which $(R_s; X_s)$ couple is leading to the best aimed performances. From a practical view, on a test-bench in laboratory, it is possible to set a source-pull

measurement using impedance tuner at source determination in order to characterize a DUT in a similar way than for the load-pull.

After the determination of the necessary optimal impedances for each stage and amplifier input/output, it is possible to design the desired matching networks to maximize the power transfer from the input of the amplifier to the output termination through all gain and power stages.

II.4.2 Possible implementations at mmW frequencies

Different matching network topologies are possible to implement depending on the power amplifier topology and operating conditions.

For single-ended amplifiers, the most common matching network topologies are L, T and π matching networks, named accordingly and respectively to the form factor of these networks. These three topologies are illustrated in Table II.4.1.

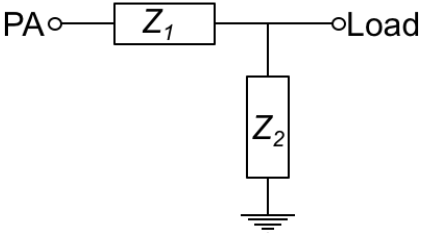
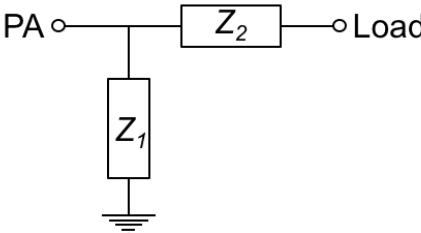
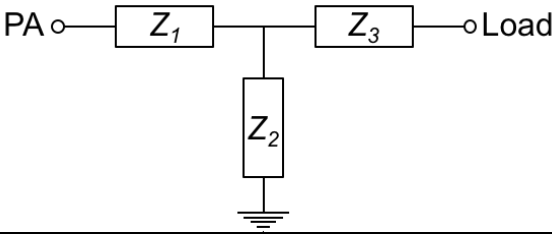
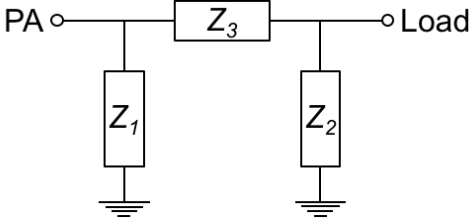
L-type		
T-type		
π -type		

Table II.4.1: L-type, T-type and π -type matching networks block schemes

Different elements can be used to synthesize these networks, like stubs, resistors, capacitors or inductors to obtain the desired impedance transformation. In simulation, it exists several tools like Smith Chart tool in ADS simulator to help with the design of these networks.

It is also possible to use lumped elements or distributed elements depending on the physical element size and the wavelength of the signal. For an element with a physical size very small compared to the wavelength, under $\lambda/100$, it is preferable to use lumped elements. At the

contrary, distributed elements are preferable to use when the dimension of the element and the wavelength present the same magnitude, corresponding to a size over $\lambda/10$. Between these two extrema, it is possible to use both distributed or lumped elements, depending on the design specifications. Generally, while at low frequencies these networks can be synthesized using lumped elements, at mmW frequencies distributed elements must be used, depending on the physical size.

In addition, impedance transformation is also achievable through integrated transformers. A transformer consists in two inductors, named primary and secondary, that are magnetically coupled.

A transformer can be seen as the simple model illustrated in Figure II.4.5 for theoretical purpose. R_p , R_s and L_p , L_s are the resistances and inductance of the primary and secondary turns respectively. A complete specific model for transformer modeling at mmW frequency in 28nm FD-SOI is available in Section II.5.1.

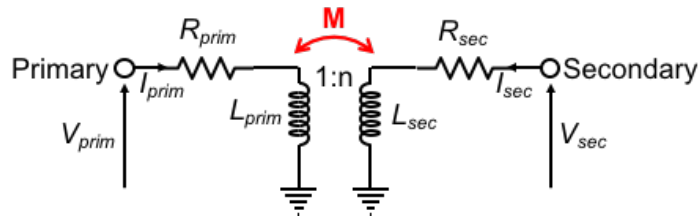


Figure II.4.5: Simplified transformer model

The impedance matrix Z of this quadrupole, linking voltage and currents of primary and secondary is defined by (II-18)-(II-19):

$$\begin{bmatrix} V_{prim} \\ V_{sec} \end{bmatrix} = \begin{bmatrix} \left. \frac{V_{prim}}{I_{prim}} \right|_{V_{sec}=0} & \left. \frac{V_{prim}}{I_{sec}} \right|_{I_{prim}=0} \\ \left. \frac{V_{sec}}{I_{prim}} \right|_{I_{sec}=0} & \left. \frac{V_{sec}}{I_{sec}} \right|_{V_{prim}=0} \end{bmatrix} \cdot \begin{bmatrix} I_{prim} \\ I_{sec} \end{bmatrix} \quad (II-18)$$

$$\begin{bmatrix} V_{prim} \\ V_{sec} \end{bmatrix} = \begin{bmatrix} j\omega \cdot L_{prim} + R_{prim} & j\omega \cdot M \\ j\omega \cdot M & j\omega \cdot L_{sec} + R_{sec} \end{bmatrix} \cdot \begin{bmatrix} I_{prim} \\ I_{sec} \end{bmatrix} \quad (II-19)$$

The impedance transformation depends on the impedance ratio between secondary and primary windings. The transformation ratio n between primary and secondary is defined by:

$$n = \sqrt{\frac{L_{prim}}{L_{sec}}} \quad (II-20)$$

The parameter M is the mutual inductance between primary and secondary. It depends on the inductances of primary and secondary and on the coupling coefficient k :

$$M = k \cdot \sqrt{L_D L_{UP}} \quad (II-21)$$

Finally, the quality factors of primary and secondary are:

$$Q_{prim} = \frac{\omega \cdot L_{prim}}{R_{prim}} \quad (II-22)$$

$$Q_{sec} = \frac{\omega \cdot L_{sec}}{R_{sec}} \quad (II-23)$$

The impedances can be adjusted thanks to geometrical parameters of the windings: diameter, surface in regard between primary and secondary, width, number of turns, metal levels. The reference [LEI11] provides an extensive study of transformers geometry for mmW applications and compared the two achievable topologies: planar and stacked. It demonstrated that stacked topology provides lower losses and enhance the coupling. Therefore, stacked topology will be used in the transformers and baluns implemented for this thesis.

Transformers can be used for single-to-single and differential-to-differential matching networks. Differential-to-single/single-to-differential conversion and power combining/splitting in a balun configuration are also achievable. These different available configurations are shown in Table II.1.1, illustrated for inter-stage matching network. Advantages are also offered with transformers and baluns, linked with circuit reliability. As a magnetic coupling is performed, there is no direct electrical connection between the stages matched by a transformer. Therefore, galvanic and electric isolation between stages is achieved, providing ESD protection and better temperature management in the circuit.

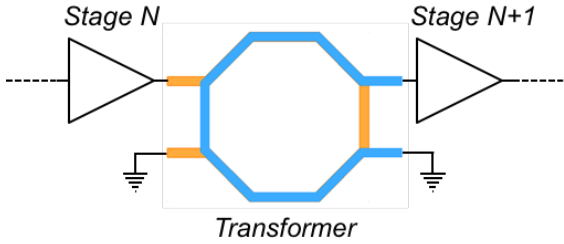
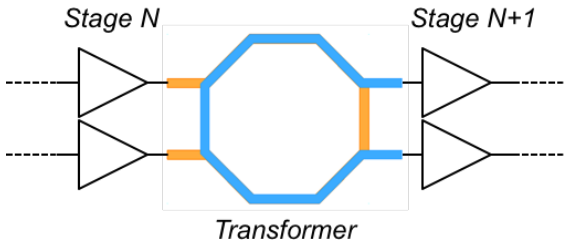
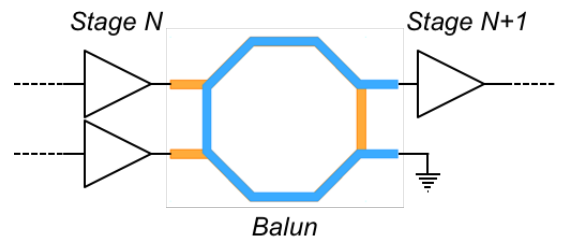
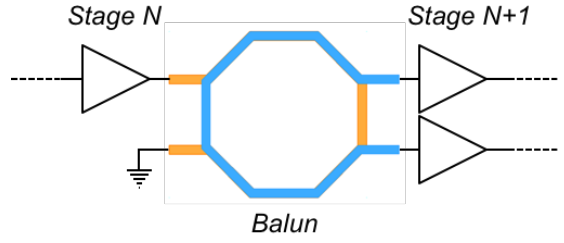
Single-ended to-single-ended	
Differential-to-differential	
Differential-to-single (combining)	
Single-to-differential (splitting)	

Table II.4.2: Different inter-stage matching networks achievable with transformers and baluns

II.5 EM CAD tools for mmW design modeling

II.5.1 Passive devices modeling

As we discussed previously, to synthesize matching networks it is possible to use lumped elements, distributed elements and transformers. While lumped elements are generally well modeled in the technologies design kits, it is necessary to provide lumped models for distributed elements using transmission lines and transformers in order to allow a fast prototyping before layout. In this section we explore the modeling of these elements and analyze the sources of losses in order to give directions for future layout.

- Microstrip transmission line modeling

It is possible to define a transmission line model by using a lumped RLCG model as it is illustrated in Figure II.5.1.

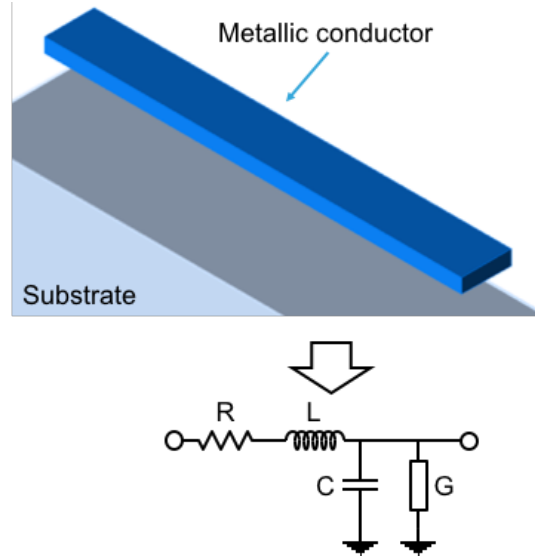


Figure II.5.1: Transmission line equivalent RLCG model illustration

These parameters can be estimated with the equations (II-24) to (II-27). R , L , C and G are the linear resistance, inductance, capacitance and conductance respectively.

$$R [\Omega.m^{-1}] = Re(Z_c \cdot \gamma) \quad (II-24)$$

$$L [H.m^{-1}] = \frac{Im(Z_c \cdot \gamma)}{2\pi f} \quad (II-25)$$

$$C [F.m^{-1}] = \frac{Im\left(\frac{\gamma}{Z_c}\right)}{2\pi f} \quad (II-26)$$

$$G [S.m^{-1}] = Re\left(\frac{\gamma}{Z_c}\right) \quad (II-27)$$

Where Z_c and γ are the line characteristic impedance and the complex propagation constant respectively. It is possible to deduct these two parameters by using ABCD matrix [FRI94], with S-parameters obtained through EM simulation tools.

$$A = \frac{1}{2} \cdot \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{S_{21}} \quad (II-28)$$

$$B = \frac{Z_c}{2} \cdot \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{S_{21}} \quad (II-29)$$

$$C = \frac{1}{2Z_c} \cdot \frac{(1 - S_{11})(1 - S_{22}) + S_{12}S_{21}}{S_{21}} \quad (II-30)$$

$$D = \frac{1}{2} \cdot \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{S_{21}} \quad (II-31)$$

Therefore,

$$Z_c = \sqrt{\frac{B}{A}} \quad (II-32)$$

$$\gamma = \frac{\cosh^{-1}(A)}{l} \quad (II-33)$$

Furthermore, the complex propagation constant γ can be expressed by (II-34) where α and β are the attenuation and phase constants respectively. From these parameters it is also possible to deduct Q , the quality factor of the transmission line with (II-35) [GOL63].

$$\gamma = \alpha + j\beta \quad (II-34)$$

$$Q = \frac{\beta}{2\alpha} \quad (II-35)$$

The phase constant can be calculated with (II-36) and depends on the relative permittivity of the material ϵ_r :

$$\beta [\text{rad.m}^{-1}] = \frac{2\pi\sqrt{\epsilon_r}}{\lambda_0} \quad (II-36)$$

The attenuation constant is the sum of several loss sources [MAR08] that depends on the frequency, the material properties and the line geometrical parameters:

- The losses in the conductor, α_c , corresponding to the skin depth effect and calculated with (II-38).
- The losses in the dielectric, α_d , calculated with (II-39).
- The losses in the substrate, α_s , calculated with (II-40).

$$\alpha [\text{dB.m}^{-1}] = \alpha_c + \alpha_d + \alpha_s \quad (II-37)$$

$$\alpha_c [\text{dB.m}^{-1}] = 8.686 \cdot \frac{\sqrt{R_{DC}^2 + R_{HF}^2}}{2Z_c} \quad (II-38)$$

$$\alpha_D [dB \cdot m^{-1}] = 8.686\pi \cdot \frac{\epsilon_r}{\sqrt{\epsilon_{eff}}} \cdot \frac{(\epsilon_{eff} - 1)}{(\epsilon_r - 1)} \cdot \frac{\tan(\delta) \cdot f}{c_0} \quad (II-39)$$

$$\alpha_S [dB \cdot m^{-1}] = 8.686 \cdot \frac{G \cdot Z_C}{2} \quad (II-40)$$

With,

$$R_{DC}^2 = \frac{l \cdot \rho}{W \cdot T} \quad (II-41)$$

$$R_{HF}^2 = \frac{l}{2W + 2T} \cdot \frac{\sqrt{\mu_0 \mu_r} \cdot \pi f}{\sigma} \quad (II-42)$$

$$G = \frac{\sqrt{\epsilon_{eff}}}{Z_C \cdot c_0} \cdot \tan(\delta) \cdot 2\pi f \quad (II-43)$$

As it is noticeable, these loss sources are all dependent from frequency and higher frequency of operation is leading to higher losses. Therefore, special care must be taken when designing distributed matching networks in order to limit the impact of losses while achieving the targeted performances.

If the transmission line length is over $\lambda/20$, the line should be divided in several parts for accurate modeling. Therefore, the RLCG lumped element is subdivided in several serial RLCG sub-cells (Figure II.5.2).

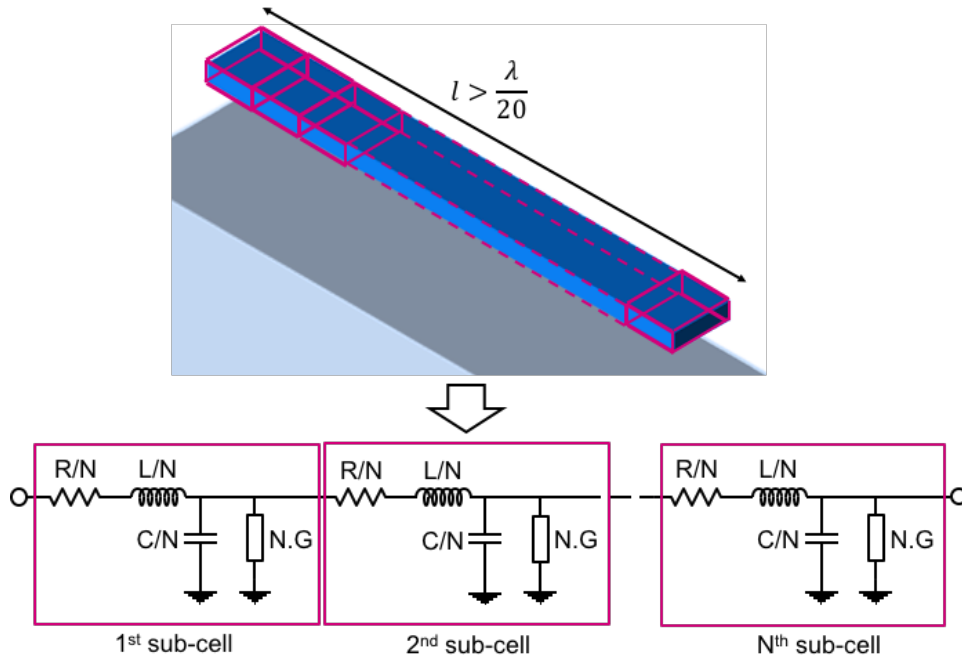


Figure II.5.2: Transmission line and RLCG model sub-division

- Transformer modeling

Transformer modeling is complex as it has to take into account multiple magnetic and electrical behaviors. [LEI11] introduced a complete lumped model independent from the technology.

This model is complex as it takes into account all the coupling and electrical behavior from DC to high frequencies and is independent from technology. Furthermore, this model is initially developed for bulk CMOS technology and has not been validated in 28nm FD-SOI technology.

In this section we propose a specific lumped model for stacked transformers prototyping in 28nm FD-SOI CMOS technology for mmW applications. It is based on the model depicted in [LEI11] and refined to fit 28nm FD-SOI technology while different method to calculate several elements are used. This model is available in Figure II.5.3.

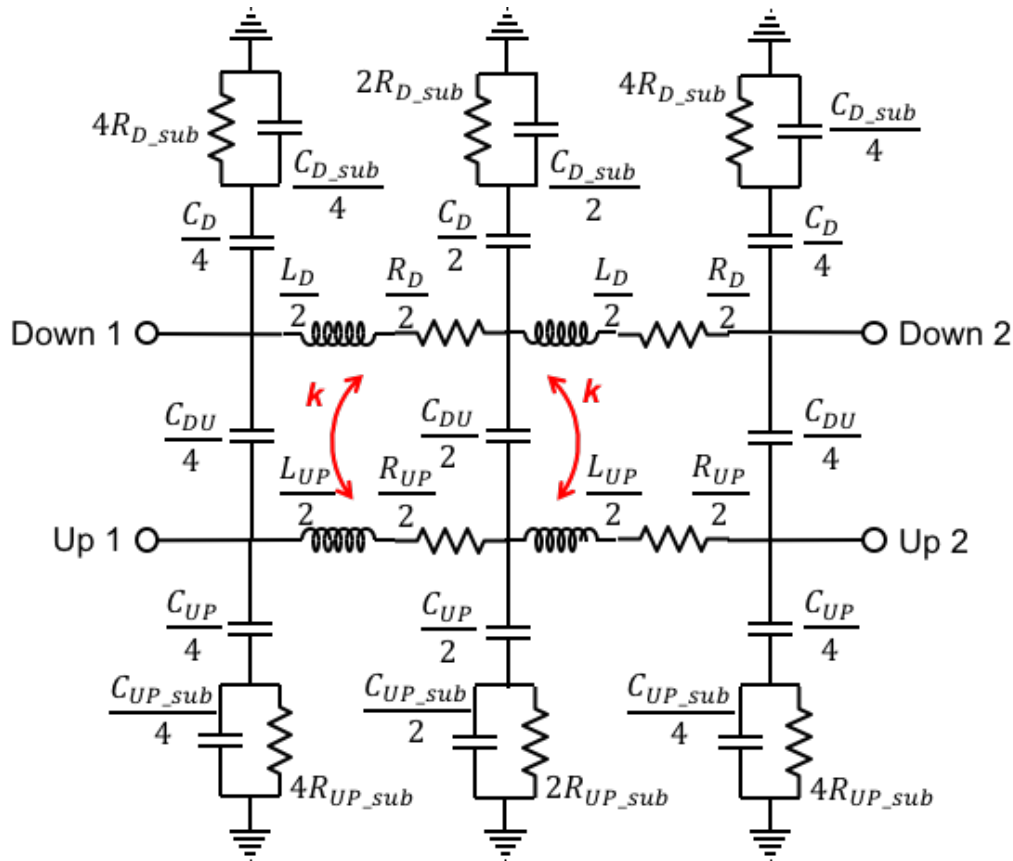


Figure II.5.3: Lumped model for 28nm FD-SOI transformer prototyping adapted from [LEI11]

Different lumped elements are used in this model:

- C_D is the capacitance between the “down” transformer winding, the nearest from the substrate, and the substrate. Its value can be calculated using parallel plate capacitor and fringe capacitance formulas.

- C_{UP} is the capacitance between the “up” transformer winding and the substrate. As in the stacked transformer topology the upper winding is placed over the down winding, it is shielded from the substrate on most parts. Therefore, this parameter is mainly composed by the fringe capacitance and by a smaller capacitance between the metal and substrate.
- C_{DU} is the capacitance between “up” and “down” transformer windings. It can be estimated with the parallel plate capacitor formulas.
- L_D , R_D and L_{UP} , R_{UP} are the inductances and resistances of “up” and “down” windings respectively.
- C_{D_sub} , C_{UP_sub} and R_{D_sub} , R_{UP_sub} are the coil-to-substrate capacitances and resistances within the substrate respectively.

Let's consider a transformer implemented in the two upper and thickest metal layers of the technology IA and IB with no substrate shielding as it has been proved in [LEI11] that it has no interest at mmW.

The technological and geometrical parameters used in this section are defined in Table II.5.1.

Parameter	Definition
W_D	Width of “down” winding
W_{UP}	Width of “up” winding
A_{D-UP}	Facing surface between “up” and “down” windings
A_{D-Sub}	Facing surface between “down” winding and substrate
A_{UP-Sub}	Facing surface between “up” winding and substrate
d_{IA-Sub}	Distance between IA metal level and substrate
d_{IB-Sub}	Distance between IB metal level and substrate
d_{IA-IB}	Distance between IA and IB metal levels
t_{IA}	Thickness of IA metal level
t_{IB}	Thickness of IB metal level
l_D	Total length of “down” winding
l_{UP}	Total length of “up” winding
n_D	Number of turn of “down” winding
n_{UP}	Number of turn of “up” winding
d_{Avg_D}	Average “down” winding diameter
d_{Avg_UP}	Average “up” winding diameter
ψ_D	Fill ratio of “down” winding diameter
ψ_{UP}	Fill ratio of “up” winding diameter
d_{in_i}	Inside diameter of “down” or “up” winding
d_{out_i}	Outside diameter of “down” or “up” winding
μ_{IA}	IA metal layer permeability
μ_{IB}	IB metal layer permeability
ρ_{IA}	IA metal layer resistivity
ρ_{IB}	IB metal layer resistivity
ϵ_{IA-Sub}	Dielectric permittivity from IA metal level to substrate
ϵ_{IB-Sub}	Dielectric permittivity from IB metal level to substrate
ϵ_{IA-IB}	Dielectric permittivity from IA and IB metal levels

Table II.5.1: Technological and geometrical parameters definitions used in the model

As we stated previously, C_D parameter is composed by C_{D_Par} parallel plate capacitance and C_{D_Fr} fringe capacitances values (II-44). Fringe capacitance can be estimated from [EO93].

$$C_D = K_C(C_{D_Par} + C_{D_Fr}) \quad (II-44)$$

With,

$$C_{D_Par} = \frac{\epsilon_0 \cdot \epsilon_{IA-Sub} \cdot A_{D-Sub}}{d_{IA-Sub}} \quad (II-45)$$

$$C_{D_Fr} = \frac{2\pi \cdot \varepsilon_0 \cdot \varepsilon_{IA-Sub} \cdot l_D}{\ln \left(1 + \frac{d_{IA-Sub}}{t_{IA}} + \sqrt{\frac{d_{IA-Sub}}{t_{IA}} \left(\frac{2d_{IA-Sub}}{t_{IA}} + 2 \right)} \right)} \quad (II-46)$$

C_{UP} is calculated with (II-47):

$$C_{UP} = K_C (C_{UP_Par} + C_{UP_Fr}) \quad (II-47)$$

Where,

$$C_{UP_Par} = \frac{\varepsilon_0 \cdot \varepsilon_{IB-Sub} \cdot A_{UP-Sub}}{d_{IB-Sub}} \quad (II-48)$$

$$C_{UP_Fr} = \frac{2\pi \cdot \varepsilon_0 \cdot \varepsilon_{IB-Sub} \cdot l_{UP}}{\ln \left(1 + \frac{d_{IB-Sub}}{t_{IB}} + \sqrt{\frac{d_{IB-Sub}}{t_{IB}} \left(\frac{2d_{IB-Sub}}{t_{IB}} + 2 \right)} \right)} \quad (II-49)$$

C_{DU} can be calculated with parallel plate capacitance formula (II-50).

$$C_{DU} = K_C \cdot \frac{\varepsilon_0 \cdot \varepsilon_{IA-IB} \cdot A_{D-UP}}{d_{IA-IB}} \quad (II-50)$$

The resistances values R_D and R_{UP} are composed by two different resistances:

- R_{D_DC} and R_{UP_DC} represent the DC resistances and are only dependent from geometrical and technological parameters (II-51), (II-52).
- R_{D_HF} and R_{UP_HF} represent the resistance at high frequencies, take into account the skin depth effect and are dependent from frequency (II-53), (II-54). These values are calculated from [LEI11].

$$R_{D_DC} = K_{R_DC} \cdot \frac{l_D \cdot \rho_{IA}}{W_D \cdot t_{IA}} \quad (II-51)$$

$$R_{UP_DC} = K_{R_DC} \cdot \frac{l_{UP} \cdot \rho_{IB}}{W_{UP} \cdot t_{IB}} \quad (II-52)$$

$$R_{D_HF} = K_{R_HF} \cdot \frac{l_D \cdot \rho_{IA}}{1 + \frac{t_{IA}}{W_D} \cdot \delta_{IA} \cdot \left[1 - e^{\left(-\frac{t_{IA}}{\delta_{IA}} \right)} \right]} \quad (II-53)$$

$$R_{UP_HF} = K_{R_HF} \cdot \frac{l_{UP} \cdot \rho_{IB}}{1 + \frac{t_{IB}}{W_{UP}} \cdot \delta_{IB} \cdot \left[1 - e^{\left(-\frac{t_{IB}}{\delta_{IB}} \right)} \right]} \quad (II-54)$$

The parameters K_{R_DC} and K_{R_HF} in (II-51)-(II-54) are resistances weighing factor. While several weighing factors are defined in [LEI11] depending on the transformer geometry, it has

been observed during this work that they are not valid for 28nm FD-SOI technology. Therefore, we defined the weighing factors available in Table II.5.2, for capacitances and resistances expressed previously, specifically for 28nm FD-SOI technology.

Geometry	K_{R_DC}	K_{R_HF}	K_C
Flipped	0.9	150.10^3	0.350

Table II.5.2: K_R HF resistances weighing factor depending on transformer topology [LEI11]

The values of ρ_{IA} and ρ_{IB} are not directly available in the DRM. However, it is possible to extract these parameters from the available sheet resistance of the corresponding metal level R_{sheet} in $\Omega.m^{-1}$ with the formula (II-55).

$$\rho_i = R_{sheet_i} \cdot W_i \cdot t_i \quad (II-55)$$

In equations (II-53) - (II-54), δ_{IA} and δ_{IB} are the IA and IB skin depths related to skin effect. They can be calculated with (II-56) and (II-57).

$$\delta_{IA} = \sqrt{\frac{\rho_{IA}}{\pi f \cdot \mu_0 \mu_{IA}}} \quad (II-56)$$

$$\delta_{IB} = \sqrt{\frac{\rho_{IB}}{\pi f \cdot \mu_0 \mu_{IB}}} \quad (II-57)$$

The skin effect is a phenomenon reflecting the alternative current distribution inside a conductor. This phenomenon is frequency-dependent. At high frequency, the current tends to circulate on the edge of the conductor. Skin depth δ represents the distance from the surface where the current density is reduced by around 37%. In other terms, 63% of the current is flowing between the surface and δ in the conductor.

To illustrate the skin depth effect, we plot the metal skin depth versus frequency for 28nm FD-SOI IA and IB levels, as they present the same thickness (Figure II.5.4). As it is noticeable, the skin depth value for IA and IB metal layers at mmW frequencies is between 420nm at 30GHz and 210nm at 100GHz.

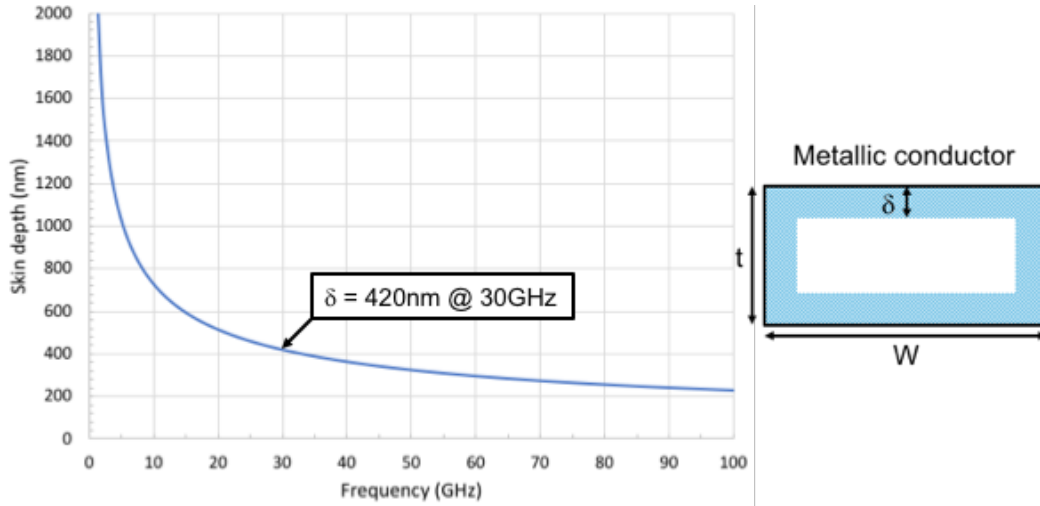


Figure II.5.4: Skin depth versus frequency of IA and IB metal layers in 28nm FD-SOI

Concerning the primary and secondary inductances values L_D and L_{UP} , they are calculated from [MOH99] that presents a modified Wheeler formula [WHE28] for integrated spiral inductors (II-58), (II-59).

$$L_D = K_1 \mu_0 \frac{n_D^2 \cdot d_{Avg_D}}{1 + K_2 \cdot \psi_D} \quad (II-58)$$

$$L_{UP} = K_1 \mu_0 \frac{n_{UP}^2 \cdot d_{Avg_UP}}{1 + K_2 \cdot \psi_{UP}} \quad (II-59)$$

In the equations (II-58) and (II-59), d_{Avg_i} and ψ_i are the average windings diameter between d_{out_i} and d_{in_i} the outside and inside diameters, and the associated fill ratio. They can be estimated with (II-60) and (II-61).

$$d_{Avg_i} = \frac{d_{out_i} + d_{in_i}}{2} \quad (II-60)$$

$$\psi_i = \frac{d_{out_i} - d_{in_i}}{d_{out_i} + d_{in_i}} \quad (II-61)$$

The constants K_1 and K_2 are defined in [MOH99] and their values depends on the transformer geometry. They are available in Table II.5.3.

Geometry	K_1	K_2
Square	2.34	2.75
Hexagonal	2.33	3.82
Octagonal	2.25	3.55

Table II.5.3: K_1 and K_2 values depending on transformer geometry [MOH99]

The substrate resistances and capacitances are calculated with expressions (II-62)-(II-65) from [LEI11]. They are based on geometrical and technological parameters for the resistances, from [CAO03]. The capacitances values take into account the substrate relaxation time constant as defined in [DIC05].

$$R_{D_sub} = \frac{3 \cdot \rho_{sub} \cdot W_D}{l_D \cdot t_{IA}} \quad (II-62)$$

$$R_{UP_sub} = \frac{3 \cdot \rho_{sub} \cdot W_{UP}}{l_{UP} \cdot t_{IB}} \quad (II-63)$$

$$C_{D_sub} = \frac{\epsilon_0 \cdot \epsilon_{Sub} \cdot \rho_{IA}}{R_{D_sub}} \quad (II-64)$$

$$C_{UP_sub} = \frac{\epsilon_0 \cdot \epsilon_{Sub} \cdot \rho_{IB}}{R_{UP_sub}} \quad (II-65)$$

In 28nm FD-SOI technology, there are several oxide layers between substrate and IA/IB metal layers. Therefore, the ϵ_{IA-Sub} , ϵ_{IB-Sub} and ϵ_{IA-IB} parameters are corresponding to equivalent oxide permittivity between the mentioned metal layers and substrate and cannot be directly found in the DRM. It is possible to estimate these parameters thanks to the Kraszerwski formula (II-66) from [KRA77] and illustrated in Figure II.5.5.

$$\epsilon_{eq} = \left[\sqrt{\epsilon_n} + \frac{d_{n-1}}{d_{n-1} + d_n} \cdot (\sqrt{\epsilon_{n-1}} - \sqrt{\epsilon_n}) \right]^2 \quad (II-66)$$

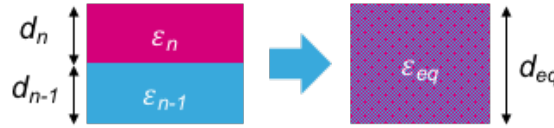


Figure II.5.5: Equivalent oxide permittivity simplification

The estimated values of ϵ_{IA-Sub} , ϵ_{IB-Sub} and ϵ_{IA-IB} parameters are available in Table II.5.4.

Parameter	Value
ϵ_{IA-Sub}	3.4
ϵ_{IB-Sub}	3.6
ϵ_{IA-IB}	3.9

Table II.5.4: ϵ_{IA-Sub} , ϵ_{IB-Sub} and ϵ_{IA-IB} parameters values

The last remaining parameter to estimate is the coupling coefficient k between the two windings that can be calculated with (II-67) where M is the mutual inductance between these windings. In practice, k is generally comprised between 0.7 and 0.9.

$$k = \frac{M}{\sqrt{L_D L_{UP}}} \quad (II-67)$$

In order to estimate the mutual inductance M , it is possible to use an analytic method as described in [LEI11]. However, for a prototyping phase, it is more convenient to extract this parameter from a 2-port electromagnetic simulation by using the equation (II-68) and the setup described in Figure II.5.6. The primary and secondary of the transformer can be implemented on “down” or “up” winding.

$$M = \frac{\text{Im}(Z_{21})}{2\pi f} \quad (\text{II-68})$$

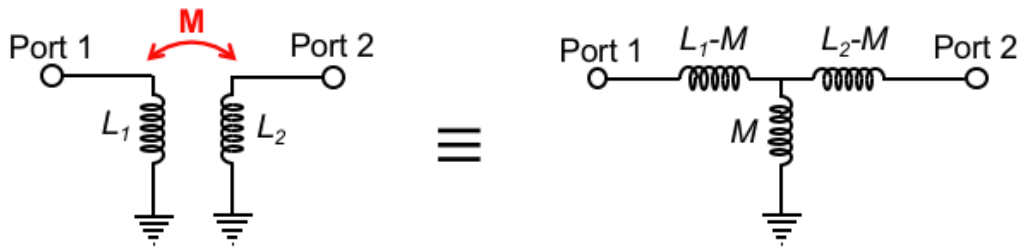


Figure II.5.6: Transformer two-ports EM simulation setup

Therefore, all the parameters have been estimated and it is possible to explore the accuracy of this model compared to EM simulations.

For this purpose, we designed a 1 turn flipped octagonal transformer (Figure II.5.7) with the geometrical parameters values available in Table II.5.5.

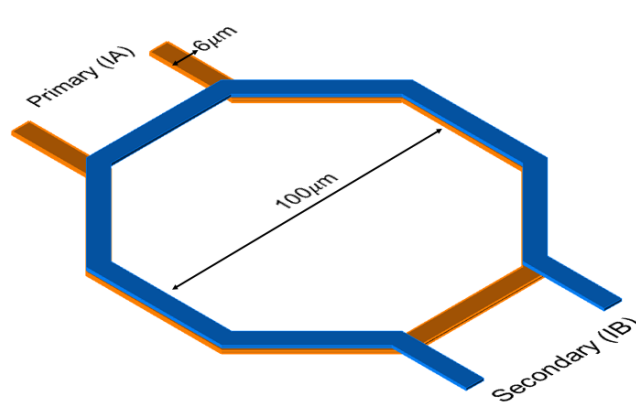


Figure II.5.7: Designed transformer for EM simulations and model comparison

Parameter	Value
W_D	$6\mu\text{m}$
W_{UP}	$6\mu\text{m}$
l_D	$355.9\mu\text{m}$
l_{UP}	$355.9\mu\text{m}$
n_D	1
n_{UP}	1
d_{in_i}	$100\mu\text{m}$
d_{out_i}	$112\mu\text{m}$

Table II.5.5: Geometrical parameters of the designed transformer

EM simulation has been performed with KEYSIGHT Momentum, and the comparison with model has been made with S-parameters analysis in Goldengate simulator up to 100GHz.

The simulation setup is available in Figure II.5.8 and the results of these simulations are available in Figure II.5.9 for S_{21} and S_{11} parameters. Figure II.5.10 shows the primary and secondary inductance values and the mutual inductance between primary and secondary.

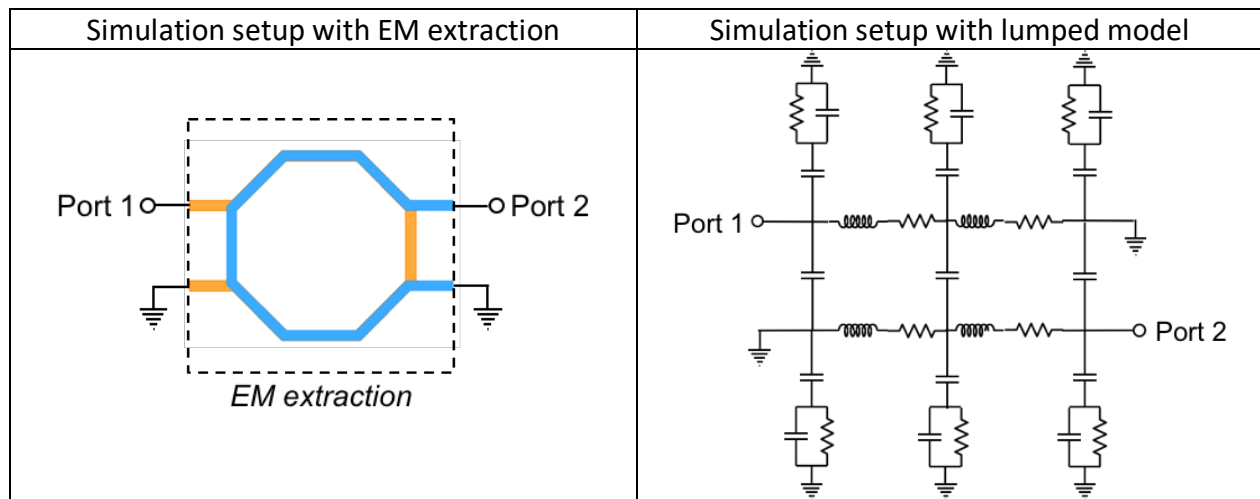


Figure II.5.8: Simulation setup for comparison between lumped model and EM simulations

The primary/secondary inductances and the mutual inductance between primary and secondary are calculated with:

$$M = \frac{\text{Im}(Z_{21})}{2\pi f} \quad (\text{II-60})$$

$$L_{\text{primary}} = \frac{\text{Im}(Z_{11})}{2\pi f} \quad (\text{II-70})$$

$$L_{Secondary} = \frac{Im(Z_{22})}{2\pi f} \quad (II-71)$$

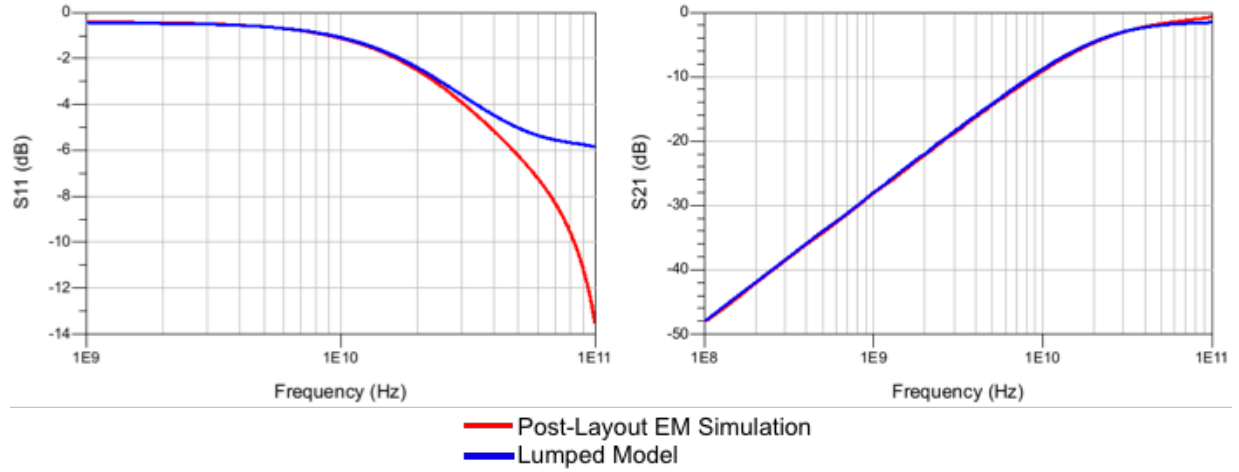


Figure II.5.9: S21 and S11 comparison between lumped model and EM simulations

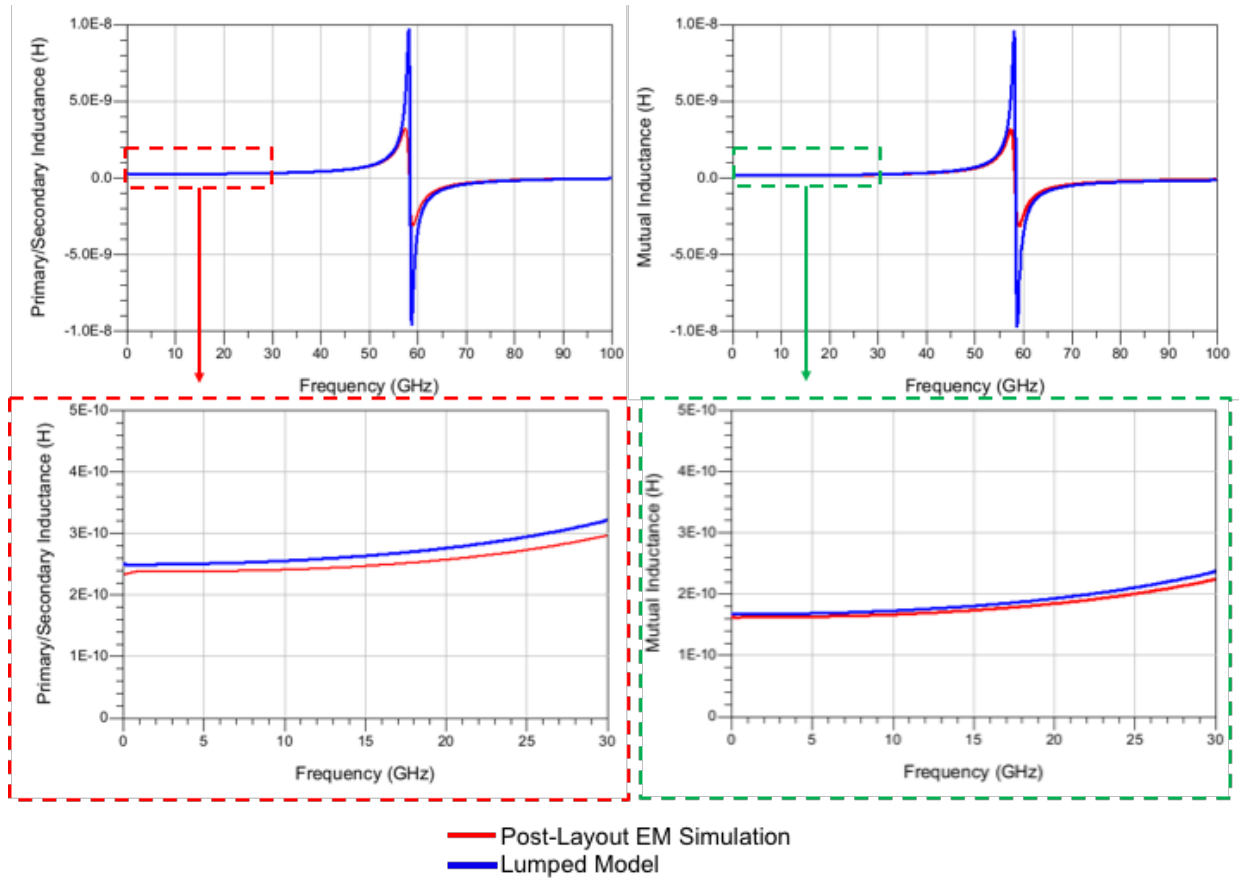


Figure II.5.10: Primary/secondary inductance and mutual inductance comparison between lumped model and EM simulations

It is noticeable that concerning the primary/secondary inductance values, the lumped model fits the EM simulation with only a small difference. The difference between the two compared curves is 20pH at 15GHz. The same remark can be done regarding mutual inductance curves. The difference between the two compared curves is even smaller than for primary/secondary inductance, with 7pH at 15GHz. Furthermore, the resonance visible on these two parameters is happening at the same frequency of 58.7GHz.

If we compare the S-parameters of the model and the EM simulation, it is noticeable that S_{21} fits perfectly up to 50GHz with after a small deviation at higher frequencies. The model is giving higher losses values than in post-layout simulations, leading to a pessimistic value. Concerning S_{11} parameter, while perfect fitting is obtained up to 25GHz, a deviation is obtained at higher frequencies. The model shows a lower 50Ω input/output matching, corresponding to a pessimistic model. Up to 60GHz, the maximum S_{11} difference between EM simulation and models is around 2dB. Therefore, we can assume that the proposed model is accurate up to 60GHz, and pessimistic for higher frequencies.

It is possible to implement this model in an algorithm to perform first dimensioning of transformers specifically in 28nm FD-SOI technology in mmW frequencies in a prototyping phase. However, refinements of transformer geometry and sizing through EM extraction and simulation tools are mandatory to fit perfectly with the targeted impedances and performances.

II.5.2 Optimization of the EM simulation tools for fast and accurate prototyping

After the passive devices modeling and the determination of the distributed elements corresponding value, the next step during the design process is the layout of these passive elements. At mmW frequencies, it is mandatory to perform electromagnetic (EM) simulations in order to extract, quantify and simulate the effect of parasitics (resistances, capacitances, inductances, coupling...) over the designed structure, as we exposed that these passive devices are critical elements in a power amplifier design. For this purpose, several EM simulation tools can be used and can be sorted in two available categories: 3D EM tools like ANSYS HFSS and KEYSIGHT EMPro and 2.5D (or 3D planar) EM simulator like KEYSIGHT Momentum. While 3D EM simulators are very accurate, it takes time to design the 3D structure and simulate it, especially in a context of passive prototyping where several versions of a passive are designed. Sometimes the time before the tape-out is limited and a first step of fast prototyping is needed in order to find the adequate dimensioning for desired passive behavior. For this purpose, 2.5D EM simulation tools are useful as it is possible to design in the same environment than classical layout in 2D. Therefore, the drawing is easy and fast. However, simulation of complex structure can be very long and resource consuming. This happens generally when the design is featuring small dimensions elements and/or vias. To accelerate the prototyping process, it is possible to perform several design and/or simulation simplifications.

In this section, we propose a new simulation fast and accurate approach for the KEYSIGHT Momentum EM simulator. This work has been presented during a technical review meeting with KEYSIGHT at STMicroelectronics Crolles.

Three different simulation setups will be exposed in the following paragraphs:

- A setup without any simplification is used as a reference. This is the most accurate simulation that is possible. (Blue trace in Figure II.5.11 and Figure II.5.12)
- A second setup where a vias simplification is performed. An array of via is replaced by one large via with the same geometrical size than the array. In this case, the EM simulator vias model is set to 2D-distributed while conductors model is set to 3D-distributed. The differences on the different vias/conductors models are explained in the following paragraph. This is the classical method used by the designers to simplify complex designs and save simulation time and resources. (Red trace in Figure II.5.11 and Figure II.5.12)
- A third setup where the simplifications are performed through EM simulator. The vias model is set to “lumped elements” while metal layers model is set to 3D-distributed. (Thick pink trace in Figure II.5.11 and Figure II.5.12)

The objective of this study is to explore the feasibility of this setup for fast and accurate passive prototyping.

Three different models are available in the Momentum EM simulation options concerning vias and metal layers and can be described as it follows. All these models are taking into account DC resistances and skin effect.

Regarding the vias modeling, three different models are provided:

- 3D-distributed: All the capacitances, mutual and self-inductances and all surface currents are estimated with a 3D mesh.
- 2D-distributed: All capacitances and inductances are estimated with a 2D mesh taking into account the currents for vertical sidewalls only.
- Lumped elements: A mesh-less equivalent circuit is used for each via, featuring self-inductor arranged in serial with a resistor.

Three models also exist for metallic conductors:

- 3D-distributed: Top, bottom and sidewall currents are estimated on any surface with a 3-dimensional mesh.
- 2D-distributed: Only top and bottom on vertical sidewalls currents are estimated.
- Sheet: The conductor is considered as a sheet. No sidewall current is available as no sidewall is meshed.

In this work we focus on accurate EM simulations for mmW passive design that is critical in a power amplifier implementation, only 3D-distributed modeling is used for metal layers. 2D-distributed and lumped elements via models are explored depending on the simulation setup previously exposed to compare simulations time, resources use and accuracy.

For this demonstration, let's consider a 90° hybrid coupler. The design is detailed in Chapter III. The direct and coupled paths are implemented in *IA* and *IB* metal layers and each unitary cell is featuring four 6x6 XA vias arrays. The three different setups have been simulated from 20GHz to 100GHz and the corresponding results are exhibited in Figure II.5.11 and Table II.5.6.

As it is observable, there is no major divergence over S_{21} and S_{31} parameters for all simulation setups. This is leading to no deviation regarding the amplitude difference between direct and coupled ports. Only a slight variation of -0.1dB is observed between the simulation where no simplification is applied and the EM engine optimization mode at 100GHz. The phase variation between the two output ports is also not affected by the simulation setup. While the simulation mode is not inducing any noticeable variation over performances, the impact over simulation time and resources consumption is important. In fact, the simulation with no simplification is more than 37 minutes long and needs 10.3GB of RAM while the simulation using EM engine optimization is only 16 seconds long and necessitates only 0.8 GB of RAM. Therefore, it has been demonstrated that with a fine and design aware EM engine optimization, it is possible to perform fast and accurate electromagnetic simulations for mmW passive design.

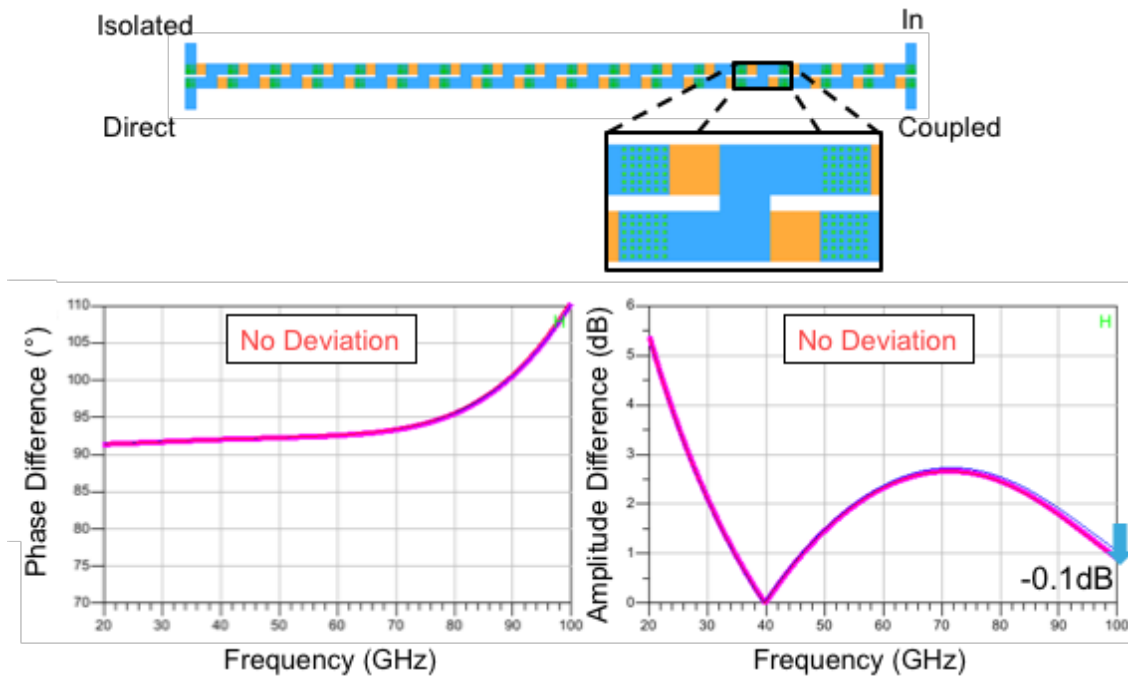


Figure II.5.11: Momentum setup comparison for standalone 90° hybrid coupler

Momentum Setup	Matrix Size	Simulation Time	Allocated RAM (Gb)
1- No Simplification	34895	37min 35sec	10.3
2- Vias Simplification	2197	54sec	1.1
3- EM engine optimization	1612	16sec	0.8

Table II.5.6: Momentum setup comparison for standalone 90° hybrid coupler: simulation resources

However, even if the structure is complex with crossings and via arrays, the environment of the simulated structure is simple. Indeed, no ground plane is simulated and there is nothing around the structure that could modify its behavior and so induces differences between the different simulation setups.

In order to verify if the EM engine optimization setup is also accurate for more complex simulations, another structure has been explored and simulated. This is a novel tunable hybrid coupler structure available in Figure II.5.12. The specific design of this coupler is developed in Chapter III. In the current section we just need to notice that this coupler presents three modes of operation:

- A first mode where all the strips around the coupler are floating, with a behavior comparable as a classical 90° hybrid coupler.
- A second mode where only one strip is grounded. This mode shows a second frequency where the amplitude difference between direct and coupled ports is equal to zero.
- A third mode where both strips are grounded and leading to a wideband operation regarding the 1dB amplitude difference band.

This structure has been extracted with Momentum with the three simulations setups, and the three modes previously depicted. The results are available in Figure II.5.12 and Table II.5.7. First, we focus on the simulation time and resources consumption. The complexity of the structure is leading to a long simulation time of 6 hours and 21 minutes when no simplification is made with 34.3GB of RAM used. The classical via array simplification into one large 2D-distributed via is leading to a simulation time reduced to around 47 minutes with 14.1GB of RAM necessary. Finally, with the EM engine optimization setup, only 6 minutes and 4.2GB of RAM are necessary! The simulation time is then 60 times faster and the RAM allocation 6.5 times lower compared to the setup where no simplification is performed.

Momentum Setup	Matrix Size	Simulation Time	Allocated RAM (Gb)
1- No Simplification	52941	6hr 21min	34.3
2- Vias Simplification	20636	47min 38sec	14.1
3- EM engine optimization	11076	6min 17sec	4.2

Table II.5.7: Momentum setup comparison for standalone 90° hybrid coupler: simulation resources

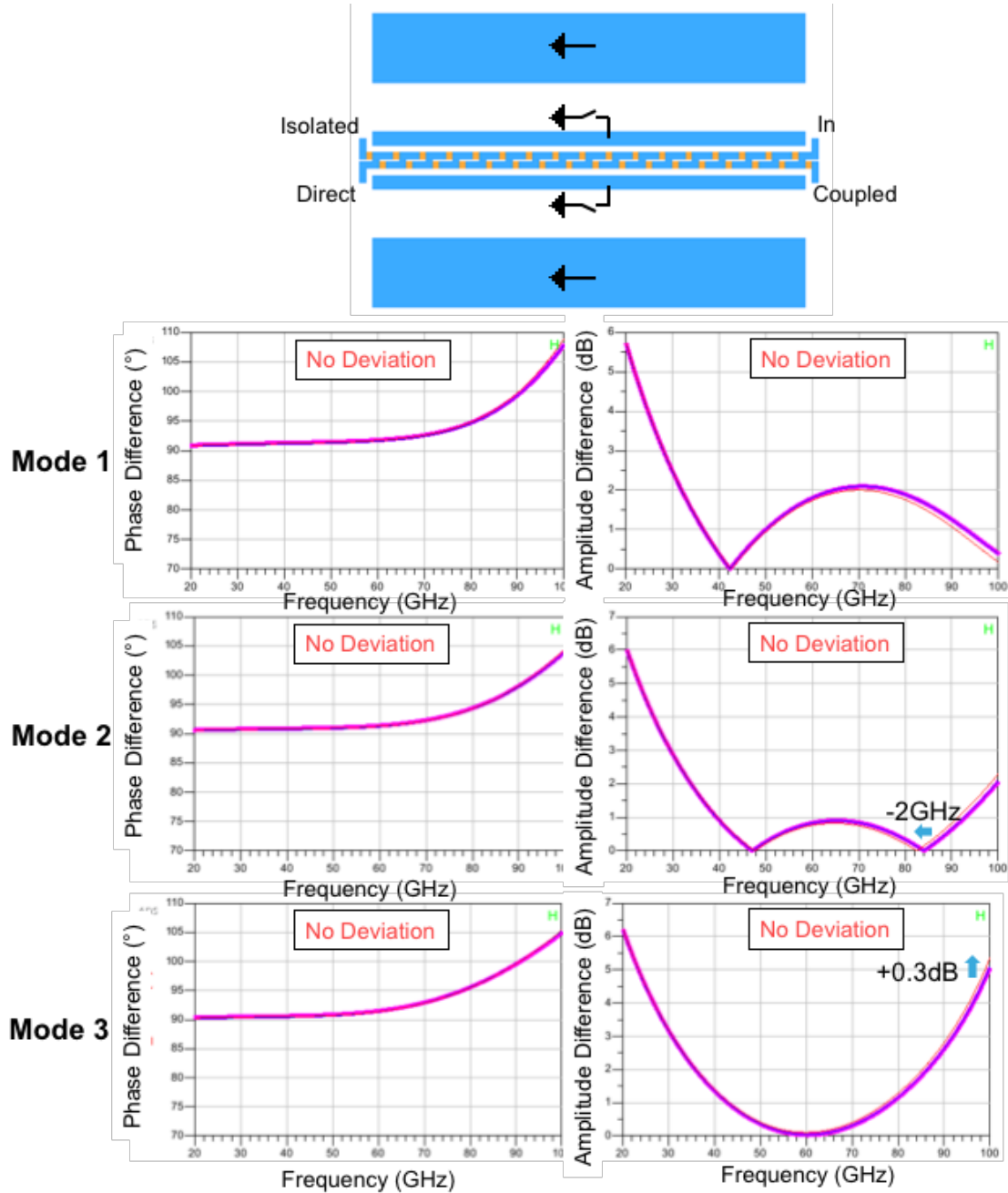


Figure II.5.12: Momentum setup comparison for tunable 90° hybrid coupler: results

While the simulation time and necessary resources are highly reduced, it is important to verify if for each operating mode of this 90° hybrid coupler and each simulation setup the same results are obtained. In the following paragraphs we are not developing the different operating mode behavior as this is available in Chapter III, we only focus on the different simulation setup results and induced deviations. For the first operating mode with both strips 1 and 2 floating, it is noticeable that no deviation is occurring whatever simulation setup is used over phase difference. The only deviation over amplitude difference is obtained from around 70GHz with a maximum of 0.2dB deviation for the via simplification setup. Concerning the second operating mode where two frequencies give an amplitude difference of 0dB, it is also remarkable that no deviation occurs on the phase difference between the different simulation setups. However, there is a slight deviation regarding the amplitude difference curves. In fact, while the first frequency peak is the same for all simulations, the via simplification setup presents a drift of -2GHz on the second frequency peak.

Finally, for the third operation mode leading to wideband operation, there is also no difference depending on the simulation setups regarding the phase difference, all the curves are superimposed. The only deviation is visible over the amplitude difference curves where via simplification curve differs from the two others, with a bandwidth reduced from around 1GHz and an amplitude difference 0.3dB higher at 100GHz.

From these results it is possible to conclude that the simulation simplifications using EM engine tool optimization regarding the models used for vias and metal layers are leading to a major reduction of simulation time and allocated resources while giving identical results compared to long and resource consuming simulations with no simplification. Compared to the classical via array simplification method classically used by designers, the simulation time with this new approach is widely reduced. The results are also more accurate for complex structures. Therefore, EM engine optimization is possible for fast and accurate prototyping even for complex passive designs in their environment. However, after the prototyping phase, full EM simulation has to be performed in order to have the most accurate EM extraction for post-layout simulations.

II.6 Stability considerations

Power amplifiers stability is a critical point that has to be taken into account during all the design process. Indeed, instability causes performances degradation and can be harmful for the circuits due to large voltage overshoot and power reachable during oscillations. It is not rare that power amplifiers operate at the limit of stability when reaching the best performances as possible. Several methods can be used by the designer to verify that stability conditions are met with its design and are separated in two parts: the linear stability analysis and the non-linear stability analysis. In this section, these two types of stability analyses are discussed in order to provide to designers the methods to verify and ensure stability of power amplifier designs.

II.6.1 Linear stability

The linear stability analysis is the first step to perform for power amplifier stability analysis and has to be conducted early in the design process for each stage independently. This analysis is conducted by using small-signal simulations for a 2-ports circuit with matched input and output ports. From the obtained S-parameters it is possible to calculate a first stability parameter, k_{Rollet} . It can be estimated with the equation (II-72):

$$k_{Rollet} = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12} \cdot S_{21}|} \quad (II-72)$$

With,

$$\Delta = S_{11} \cdot S_{22} + S_{12} \cdot S_{21} \quad (II-73)$$

Several observations over stability conditions can be formulated depending on the values of k_{Rollet} and Δ and are summarized in Table II.6.1.

$ k_{Rollet} > 1$	$k_{Rollet} > 1$	$ \Delta < 1$	Unconditionally stable
		$ \Delta > 1$	Conditionally stable
	$k_{Rollet} < -1$		Unstable
$ k_{Rollet} < 1$			Conditionally stable
$ k_{Rollet} = 1$			Unstable

Table II.6.1: Stability depending on k_{Rollet} and Δ values

Unconditional stability conditions have to be met for all stages of the design to ensure overall power amplifier linear stability. However, if these analyses are performed too early in the design process, the simulated stage can be instable. Indeed, the matching network composed by passive components introduces losses that help to the stage stabilization and parasitic interconnections have to be extracted for the same reason. Thus, linear stability analyses should be done post stage layout, after the input and output matching network implementation for each stage.

If conditional stability is obtained, it is possible to draw the stability circles for each desired frequency in the Smith Chart to determine the source or load impedances that could lead to potential instability. The stability circles can be determined as it follows.

Stable operations occur for:

$$|\Gamma_{in}| < 1 \text{ and } |\Gamma_{out}| < 1 \quad (II-74)$$

In this case, no reflection with a gain > 1 , source of instability, is obtained at the input and output of the stage of interest. Parameters $|\Gamma_{in}|$ and $|\Gamma_{out}|$ can be determined with S-parameters as it follows, with Γ_L and Γ_S the load and source reflection coefficients respectively.

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12} \cdot S_{21} \cdot \Gamma_L}{1 - S_{22} \cdot \Gamma_L} \right| \quad (II-75)$$

$$|\Gamma_{out}| = \left| S_{22} + \frac{S_{12} \cdot S_{21} \cdot \Gamma_S}{1 - S_{11} \cdot \Gamma_S} \right| \quad (II-76)$$

Instability occurs when $|\Gamma_{in}|$ and $|\Gamma_{out}|$ are equal or superior to 1. We can define the boundaries of instability in (II-77) and (II-78).

$$|\Gamma_{in}| = 1 \quad (II-77)$$

$$|\Gamma_{out}| = 1 \quad (II-78)$$

In other terms,

$$\left| S_{11} + \frac{S_{12} \cdot S_{21} \cdot \Gamma_L}{1 - S_{22} \cdot \Gamma_L} \right| = 1 \quad (II-79)$$

$$\left| S_{22} + \frac{S_{12} \cdot S_{21} \cdot \Gamma_S}{1 - S_{11} \cdot \Gamma_S} \right| = 1 \quad (II-80)$$

This can be rearranged as available in (II-81) and (II-82).

$$|S_{11} - \Delta \cdot \Gamma_L| = |1 - S_{22} \cdot \Gamma_L| \quad (II-81)$$

$$|S_{22} - \Delta \cdot \Gamma_S| = |1 - S_{11} \cdot \Gamma_S| \quad (II-82)$$

The solutions for $|\Gamma_L|$ and $|\Gamma_S|$ can be formulated to form the equations of a circle in Γ_L and Γ_S plans respectively.

$$|\Gamma_L - C_L| = R_L \quad (II-83)$$

$$|\Gamma_S - C_S| = R_S \quad (II-84)$$

With,

$$R_L = \left| \frac{S_{12} \cdot S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \quad (II-85)$$

$$C_L = \frac{(S_{22} - S_{11}^* \cdot \Delta)^*}{|S_{22}|^2 - |\Delta|^2} \quad (II-86)$$

And,

$$R_S = \left| \frac{S_{12} \cdot S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \quad (II-87)$$

$$C_S = \frac{(S_{11} - S_{22}^* \cdot \Delta)^*}{|S_{11}|^2 - |\Delta|^2} \quad (II-88)$$

C_L and C_S are the center of the load and source stability circles in Γ_L and Γ_S plans respectively while R_L and R_S are the corresponding radius.

These load and source stability circles represent the boundary of stability and instability regions. The stability regions are determined by S_{11} and S_{22} . In fact, if $|S_{11}|$ or $|S_{22}|$ are superior to 1, the stability region is inside the corresponding circle while if $|S_{11}|$ or $|S_{22}|$ are inferior to 1, the stability region is located outside the corresponding circle. The Figure II.6.1 illustrates the stability circles in the Smith Chart and the associated stability regions.

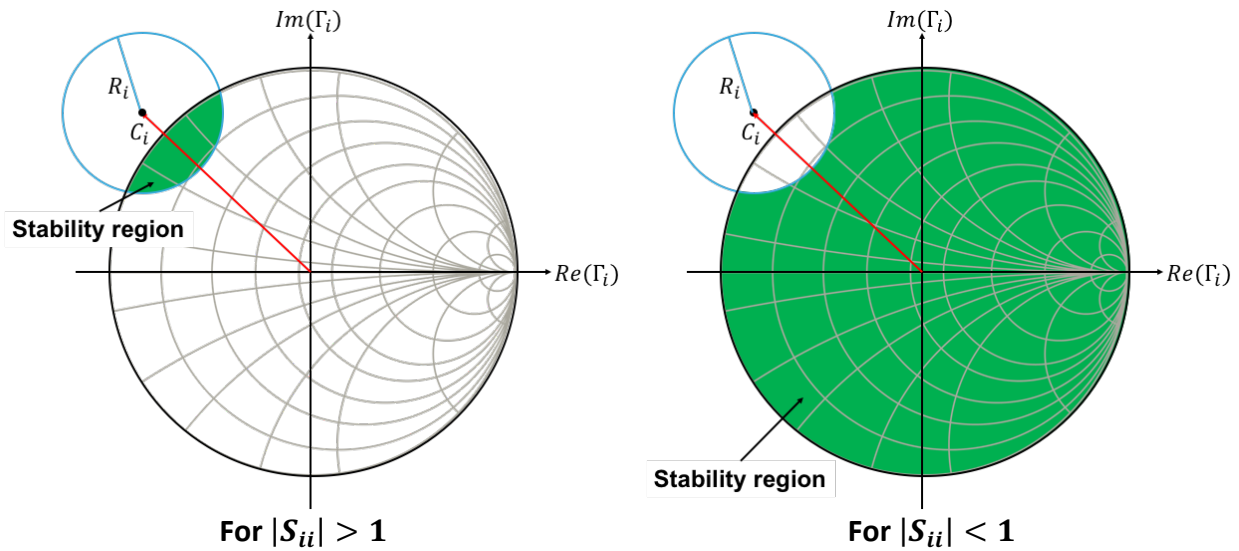


Figure II.6.1: Stability circles illustration

Another small-signal stability parameter can be used and have been theorized by Edwards and Sinsky in [EDW92] and is a geometrical parameter. Indeed, it gives the distance between Smith Chart origin center and the nearest point of the load or source stability circle. This factor is named μ and μ' for load and source stability purposes respectively and can be calculated using the following equations.

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta \cdot S_{11}^*| + |S_{12} \cdot S_{21}|} \quad (II-89)$$

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta \cdot S_{22}^*| + |S_{12} \cdot S_{21}|} \quad (II-90)$$

For an unconditional stability, μ and μ' must be superior to 1. Indeed, this condition means that the stability circles are located outside the Smith Chart and so no impedance for both load and source can lead to instable operations.

From a practical side, when designing a power amplifier, the designer conducts small-signal analysis and calculate k_{rollot} , Δ , μ and μ' to verify stability over a desired frequency range. The stability circles can be explored only when non-unconditional stability is obtained.

II.6.2 Non-Linear stability

While the small-signal analysis allows to determine linear stability, this is not sufficient to conclude on the overall stability of a power amplifier. In fact, the small-signal analysis doesn't take into account the stability at higher power levels while oscillations can occur for power levels approaching compression or saturation. Furthermore, oscillations can also be caused by sudden current or voltage pulses on the supply or bias nodes during measurements. Therefore, non-linear stability analyses are necessary to verify stable operations of the power amplifier. For this purpose, several transient simulations can be conducted.

First, a transient simulation with no RF signal applied at the input of the circuit. Normally, an output voltage V_{out} of 0V is obtained over all the simulated time range. The power amplifier is then excited with square wave current pulses, located at different nodes. In fact, this pulse must be inserted separately on each supply, bias, body bias and ground nodes of the amplifier.

Instability is characterized by pulse induced oscillations over output voltage. If these oscillations are sustained in time, the power amplifier is instable. If these oscillations are amortized, the power amplifier is then stable. An example of pulse induced amortized oscillations is available in Figure II.6.2.

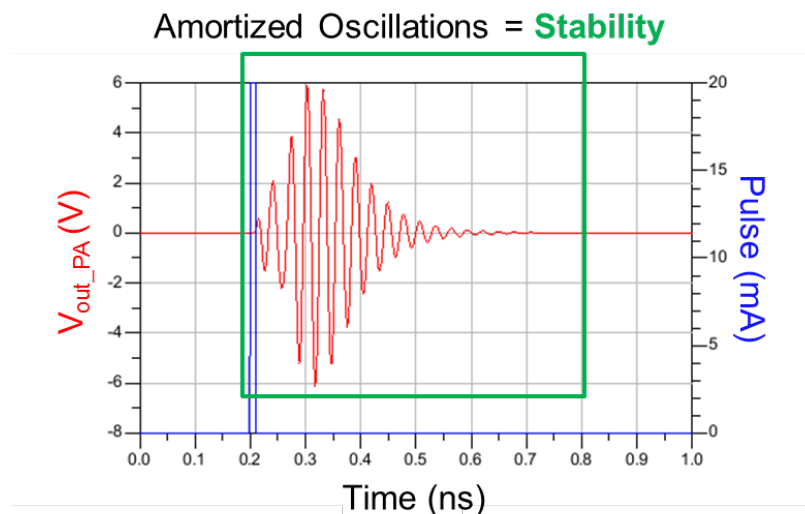


Figure II.6.2: Damped oscillations resulting from a pulse excitation

In order to characterize the stability at different input power levels, it is also possible to insert voltage pulses over all the supply, bias, body biasing and ground nodes separately while an input power at the frequency of interest for a desired operating point is applied. If the insertion of this pulse has no effect or only temporary effect over the output voltage, then the amplifier is stable at the simulated power and operating conditions. Figure II.6.3 presents a stable PA behavior to a voltage pulse insertion.

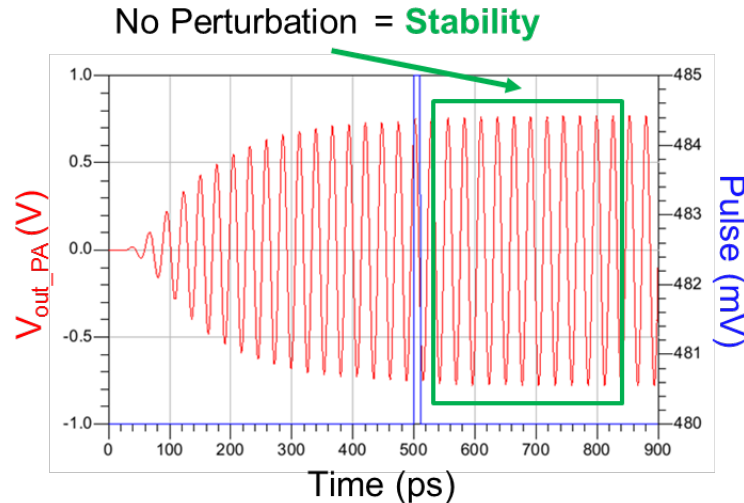


Figure II.6.3: No perturbations resulting from a pulse excitation

While the linear stability must be performed early in the design process to ensure each stage linear stability, the non-linear stability exploration depicted in this section must be performed later in the design process. In fact, this analysis must be performed in post-layout simulations, where the accesses for the different voltage nodes are routed and extracted.

If oscillations occur in simulations, it is important to correct the design, by adding losses, RC tank or other design techniques to reduce the risk of oscillation. Furthermore, stability considerations must be known early by the designer. A design oriented to robust stability using several design techniques enhancing overall amplifier stability and each stage is mandatory.

II.7 Design optimization techniques

The designer can use several design techniques optimization in order to overcome potential issues or maximize targeted performances in deep sub-micron technology at mmW frequency. In this section we detail two design optimization techniques that have been used in the power amplifier design presented in Chapter III: power combining and cross-coupling capacitive neutralization.

II.7.1 Power combining

The CMOS technology down-scaling has the effect to reduce the achievable output power of power amplifiers compared to III-V technology. This phenomenon is not new and not limited to CMOS technology. It appeared from early solid-state amplifier era, where the achievable power was way lower than the power levels obtained with vacuum tubes.

To overcome power limitation, it is possible to use power combining. The concept of power combining consists of the output combination of multiple power cells to achieve higher overall output power compared to a single amplifier.

It is possible to use transmission lines to perform integrated power combining by using Wilkinson or Zero-degree combiners (Figure II.7.1). While these structures can achieve impedance matching by adjusting the transmission lines dimensions, the use of transmission lines implies large insertion losses and size.

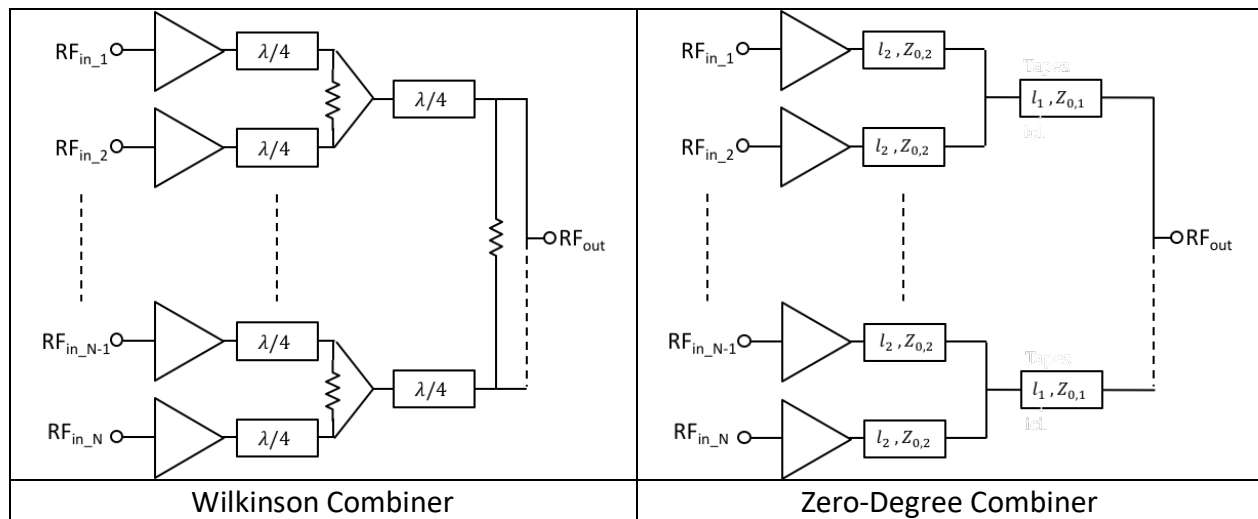


Figure II.7.1: Wilkinson and Zero-degree combiners block schemes

In this section we explore several power combining techniques for mmW deep-submicron implementation using transformers and 90° hybrid couplers. In this way, an overview of the power combining possibilities for differential, N -differential-path and balanced power amplifiers is proposed. Some of these techniques have been performed in the power amplifier design depicted in Chapter III.

- Transformer-based power combining
 - Differential power combining

Power combining of a differential amplification path can be performed through baluns. The perfect combination of identical amplification branches with 180° phase difference is leading

to an output power level enhancement by 3dB while the gain is the same than the standalone amplification branch. This is illustrated in Figure II.7.2.

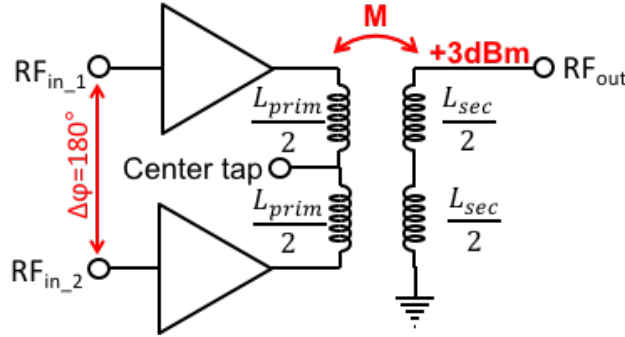


Figure II.7.2: Differential-to-single power combining through balun

- N -differential-path power combining

It is also possible to combine multiple differential amplification path by using transformers with two structures:

- Parallel power-Combining Transformer (PCT).
- Series power-Combining Transformer (SCT).

These two structures differ from the secondary winding topology, allowing different combination. A figure issued from [AN08] and presenting both topologies is available in Figure II.7.3.

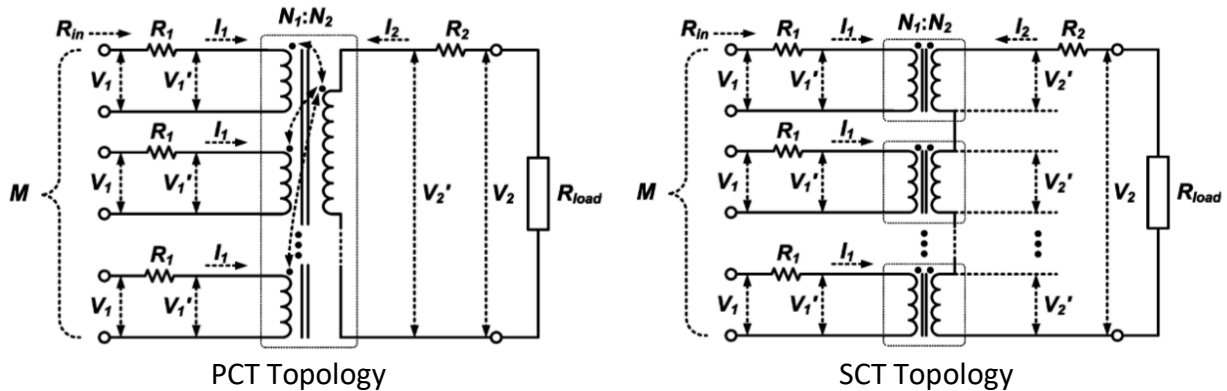


Figure II.7.3: PCT and SCT topologies block schemes [AN08]

The PCT topology consists in the combination of several independent transformers secondary winding currents and is used in [LEE07]. In [MAR10], the PCT topology is achieved thanks to transmission lines at the output.

The SCT topology consists in the serial combination of the transformer secondary winding, therefore the secondary voltages are added while they share the same current.

The principal application of SCT topology is the DAT, for “Distributed Active Transformer”, which has been introduced in the early 2000’s by [AOK02]. While the secondary turn of a transformer remains unchanged compared to a classical transformer, in a DAT multiple primary turns are implemented to combine multiple amplification path. A schematic of a DAT is available in Figure II.7.4 to illustrate this concept.

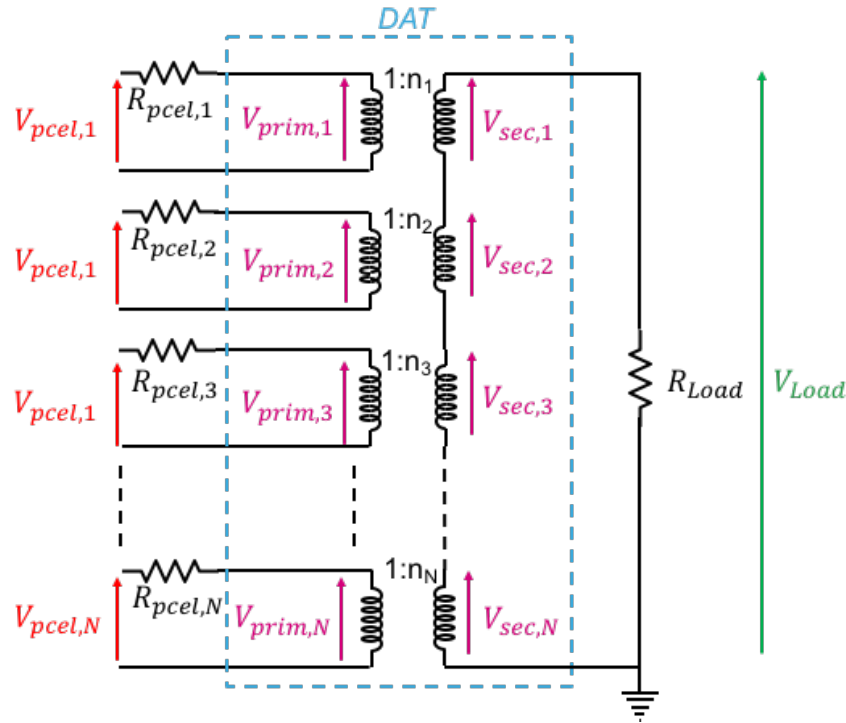


Figure II.7.4: DAT schematic

As stated previously, the voltage at the load, V_{Load} , is the sum of secondary voltages:

$$V_{Load} = V_{Sec,1} + V_{Sec,2} + \dots + V_{Sec,N} = \sum_{k=1}^N V_{Sec,k} \quad (II-91)$$

V_{Load} can then be expressed with the primary voltage:

$$V_{Load} = \sum_{k=1}^N n_k \cdot V_{Prim,k} \quad (II-92)$$

It has been exposed in [CHO10] that the impedance seen by each amplification path is only dependent from output power and impedances of the other amplification cells, as the current flowing in the secondary remains constant. This impedance is given by (II-93).

$$Z_{Load,k} = \frac{V_{prim,k} (R_{Load} + \sum_{i=1}^N n_i^2 \cdot R_{P,i})}{n_k \cdot \sum_{i=1}^N n_i \cdot V_{prim,i}} \quad (II-93)$$

Let's consider that all the amplification paths power cells deliver the same voltages and present the same impedances, corresponding to identical paths combining through the DAT, Z_{Load} can then be simplified as:

$$Z_{Load,k} = \frac{R_{Load}}{n^2 \cdot N^2} \quad (II-94)$$

The output power delivered to the load and resulting from the ideal combining of N amplification paths is then:

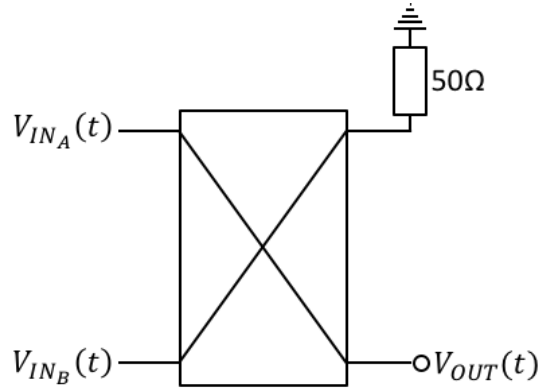
$$P_{Load} = \frac{n^2 \cdot N^2 \cdot V_P^2}{2R_{Load}} \quad (II-95)$$

While in the work presented in Chapter III, the N -paths DAT power combination has not been used, it has been implemented in 28nm FD-SOI technology in previous work [LAR15], demonstrating the feasibility of this technique.

However, it is remarkable that phase and amplitude imbalance in these combiners are critical. Therefore, several hybrid combiners using both serial and parallel combining have been implemented. This is the case for Series-Parallel power-Combining Transformer (SPCT) [ALO12] and Parallel-Series power-Combining Transformer (PSCT) [SHI13].

- 90° hybrid coupler power combining

90° power combining is notably used at the output of balanced power amplifiers. It can be performed using 90° hybrid couplers. This type of coupling improves the output power levels, P_{sat} and P_{1dB} , by 3dB by combining two 90° out-of-phase amplification paths. A schematic of a 90° hybrid coupler in combiner configuration is available in Figure II.7.5.



$$V_{OUT}(t) = \frac{1}{\sqrt{2}} (V_{INA}(t) \angle -45^\circ + V_{INB}(t) \angle +45^\circ)$$

Figure II.7.5: Combining through 90° hybrid coupler

This topology is not only beneficial in terms of output power enhancement but also improves the intermodulation products in the context of balanced amplifier. In the following section, we provide the equations illustrating these intermodulation products reductions in a balanced amplifier, resulting of 90° combination of 90° out-of-phase amplification paths and demonstrated in [MOR17-2].

For a V_{in} signal introduced at the input of a balanced amplifier and featuring two tones f_1 and f_2 with the same amplitude V_0 (II-96), it has been demonstrated that V_{INA} and V_{INB} , the output of each identical amplification and, so the inputs of the combiner, can be expressed by (II-96)-(II-98).

$$V_{in}(t) = V_0 \cdot (\cos(\omega_1 t) + \cos(\omega_2 t)) \quad (II-96)$$

$$V_{INA}(t) = \sum_n K_n \cdot \left(\frac{V_0}{\sqrt{2}}\right)^n \cdot \left(\cos\left(\omega_1 t + \frac{\pi}{4}\right) + \cos\left(\omega_2 t + \frac{\pi}{4}\right)\right)^n \quad (II-97)$$

$$V_{INB}(t) = \sum_n K_n \cdot \left(\frac{V_0}{\sqrt{2}}\right)^n \cdot \left(\cos\left(\omega_1 t - \frac{\pi}{4}\right) + \cos\left(\omega_2 t - \frac{\pi}{4}\right)\right)^n \quad (II-98)$$

Several remarks can be made regarding the intermodulations due to the 90° phase difference between both amplification paths:

- 3rd order intermodulations at $2f_1 - f_2$ and $2f_2 - f_1$ are out-of-phase by 90°. After 90° combination at the output, they are recombined in phase.
- 3rd order intermodulations at $2f_1 + f_2$, $2f_2 + f_1$, $3f_1$, $3f_2$ are out-of-phase by 270°. After 90° combination at the output, they are recombined at 180° and so are eliminated.

- 2nd order intermodulations at $f_1 + f_2$, $2f_1$, $2f_2$ are out-of-phase by 180°. After 90° combination at the output, they are recombined in quadrature.

Therefore, [MOR17-2] demonstrated that the voltages at the output of the balanced amplifier after 90° combination are:

- At the fundamental:

$$V_{OUT}(t) = K_1 \cdot V_0 \cdot (\cos(\omega_1 t) + \cos(\omega_2 t)) \quad (II-99)$$

- 2nd order intermodulation products:

$$V_{OUT}(t) = \frac{K_2 \cdot V_0^2}{2} \cdot \left[\cos((\omega_2 - \omega_1)t) + \frac{\cos(2\omega_1 t)}{2} + \frac{\cos(2\omega_2 t)}{2} + \cos((\omega_2 + \omega_1)t) \right] \quad (II-100)$$

- 3rd order intermodulation products:

$$V_{OUT}(t) = \frac{3}{4} \cdot \frac{K_3 \cdot V_0^3}{2} \cdot [\cos((2\omega_1 - \omega_2)t) + \cos((2\omega_2 - \omega_1)t)] \quad (II-101)$$

This is resulting in a reduction of the 3rd order intermodulations by -6dB, the 2nd order intermodulation products by -9dB and a rejection of the 3rd order intermodulation products. Detailed theoretical demonstration is available in [MOR17-2]. This is illustrated in Figure II.7.6, comparing classical power amplifier architecture (dotted) with balanced power amplifier topology (solid) intermodulation products.

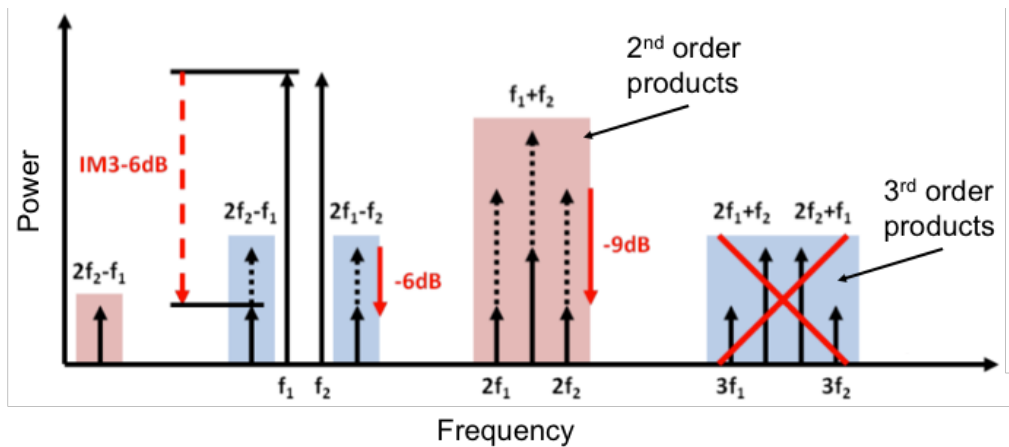


Figure II.7.6: Intermodulation products comparison between classical and balanced topology [MOR17-2]

II.7.2 Neutralization capacitance theory

The effect of C_{GD} capacitance over common-source amplification stage is well known by the IC designers. The C_{GD} capacitance is the parasitic capacitance between gate and drain of a MOS device and can't be avoided even if the transistor BEOL optimization tends to reduce its value. The presence of this parasitic capacitance reduces the reverse isolation, from output to input, as it adds a return path between gate and drain of the device. This return path also reduces the CS stage gain and enables Miller effect, theorized by Miller in 1920 [MIL20].

In fact, a capacitance introduced between the output and input ports of an inverter amplifier leads to a large input equivalent capacitance limiting the bandwidth. C_{Miller} value is given by the equation (II-102) while Figure II.7.7 presents a schematic representation of this effect.

$$C_{Miller} = C_{GD}(1 + A_V) \quad (II-102)$$

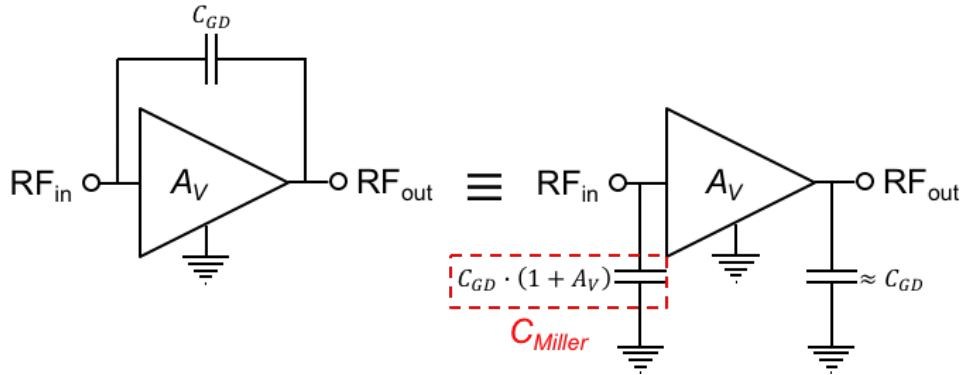


Figure II.7.7: Miller capacitance illustration

Furthermore, the C_{GD} capacitance has an impact on the f_T of the transistor. Indeed, f_T is given by the formula (II-103) for a MOS transistor. The higher the C_{GD} capacitance is, the lower the f_T is.

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \quad (II-103)$$

Therefore, the improvements resulting from C_{GD} capacitance reduction is undeniable and has been intensively discussed in the literature. In this section we focus on a C_{GD} neutralization technique that has been used during the power amplifier design presented in Chapter III.

Differential topology enables the possibility of using cross-coupling capacitive neutralization technique in the design. This technique, extensively used in PA literature, enhances stability, gain and reduce Miller effect by minimizing parasitic gate-to-drain capacitance C_{GD} .

A capacitor C_{neutro} is inserted and connected from the gate of one transistor to the drain of the other transistor. In this way, C_{GD} parasitic capacitance sees a parallel capacitor with a phase shift of 180° that acts like a negative capacitance.

A simplified schematic of a common-source stage featuring neutralization capacitors is given in Figure II.7.8.

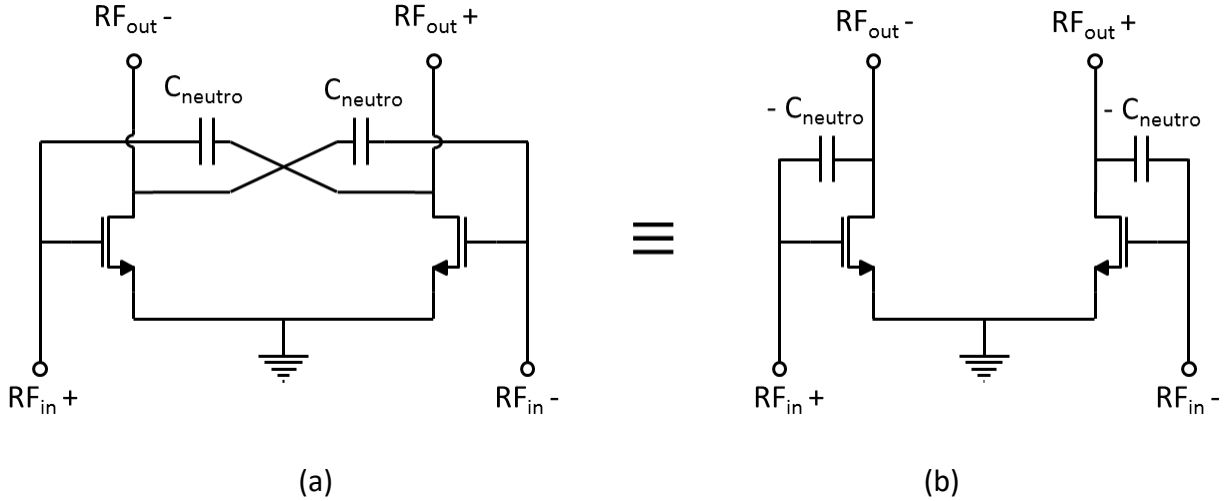


Figure II.7.8: CS stage with C_{neutro} (a) acting as negative parallel capacitance (b)

To illustrate the stability and gain enhancement provided by the use of this design technique, we can reason on the small-signal equivalent schematic of a cross-coupled differential pair provided in Figure II.7.9.

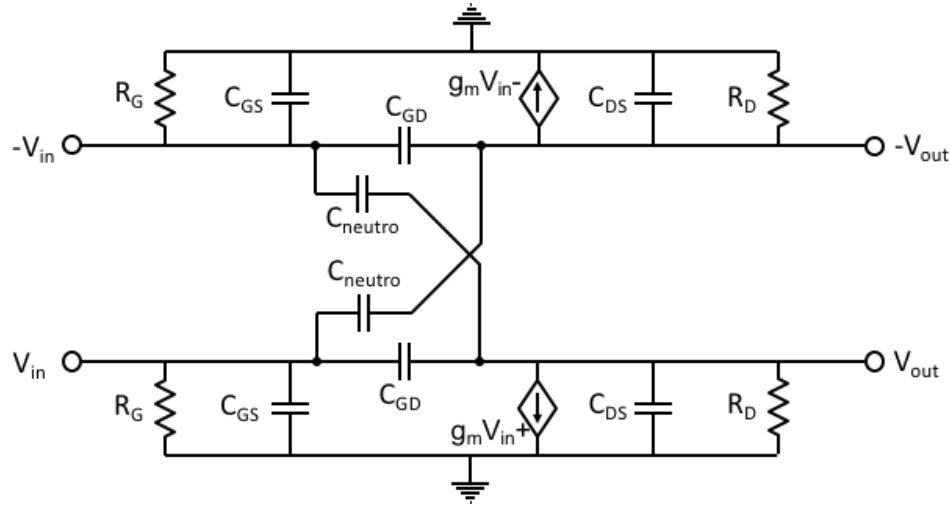


Figure II.7.9: Small-signal equivalent scheme of cross-coupled differential common-source stage

Stability factor k_{rollet} , depicted in Section II.6.1, maximum available gain MAG and maximum stable gain MSG can be expressed as it follows [ASA11]:

$$k_{rollet} = \frac{2\text{Re}(Y_{11})\text{Re}(Y_{22}) - \text{Re}(Y_{12}Y_{21})}{|Y_{12}Y_{21}|} \quad (II-104)$$

$$MAG = \left| \frac{Y_{21}}{Y_{12}} \right| \left(k_{rollet} - \sqrt{k_{rollet}^2 - 1} \right) \quad (II-105)$$

$$MSG = \left| \frac{Y_{21}}{Y_{12}} \right| \quad (II-106)$$

If we calculate the admittance matrix Y derived from Figure II.7.9:

$$Y = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \quad (II-107)$$

$$Y = \begin{bmatrix} \left. \frac{I_{in}}{V_{in}} \right|_{V_{out}=0} & \left. \frac{I_{in}}{V_{out}} \right|_{V_{in}=0} \\ \left. \frac{I_{out}}{V_{in}} \right|_{V_{out}=0} & \left. \frac{I_{out}}{V_{out}} \right|_{V_{in}=0} \end{bmatrix} \quad (II-108)$$

$$Y = \begin{bmatrix} \frac{1}{R_G} + j\omega C_{GS} + j\omega(C_{GD} + C_{neutro}) & -j\omega(C_{GD} - C_{neutro}) \\ g_m - j\omega(C_{GD} - C_{neutro}) & \frac{1}{R_D} + j\omega C_{DS} + j\omega(C_{GD} + C_{neutro}) \end{bmatrix} \quad (II-109)$$

Stability and gain parameters can be rewritten:

$$k_{rollet} = \frac{2 + R_G R_D \omega^2 (C_{GD} - C_{neutro})^2}{R_G R_D \omega |C_{GD} - C_{neutro}| \sqrt{g_m^2 \omega^2 (C_{GD} - C_{neutro})^2}} \quad (II-110)$$

$$MAG = \frac{\sqrt{g_m^2 + \omega^2 (C_{GD} - C_{neutro})^2}}{\omega |C_{GD} - C_{neutro}|} \left(k_{rollet} - \sqrt{k_{rollet}^2 - 1} \right) \quad (II-111)$$

$$MSG = \frac{\sqrt{g_m^2 + \omega^2 (C_{GD} - C_{neutro})^2}}{\omega |C_{GD} - C_{neutro}|} \quad (II-112)$$

It is remarkable that the more C_{neutro} value is near to C_{GD} value and so reducing the $(C_{GD} - C_{neutro})$ factor, the higher k_{rollet} stability factor is and MAG/MSG, leading to higher stability and gain.

During the design process, optimal C_{neutro} value can be defined using a small-signal analysis and by fine tuning the value of C_{neutro} while optimum input and output loads are presented to the circuit. For this purpose, it is mandatory to ensure that interconnections, input/output path and parasitic resistances and capacitances inherent to transistors BEOL have been properly extracted.

To define C_{neutro} value, the function $k_{rollet} = f(C_{neutro})$ can be plotted on a graph. MAG and MSG can also be plotted on the same graph. The optimal value of C_{neutro} is the one that gives the peak response of the k_{rollet} factor. A C_{neutro} acceptable values range can be defined as the range of values that are leading to $k_{rollet} > 1$, ensuring small-signal stability. This is illustrated in Figure II.7.10.

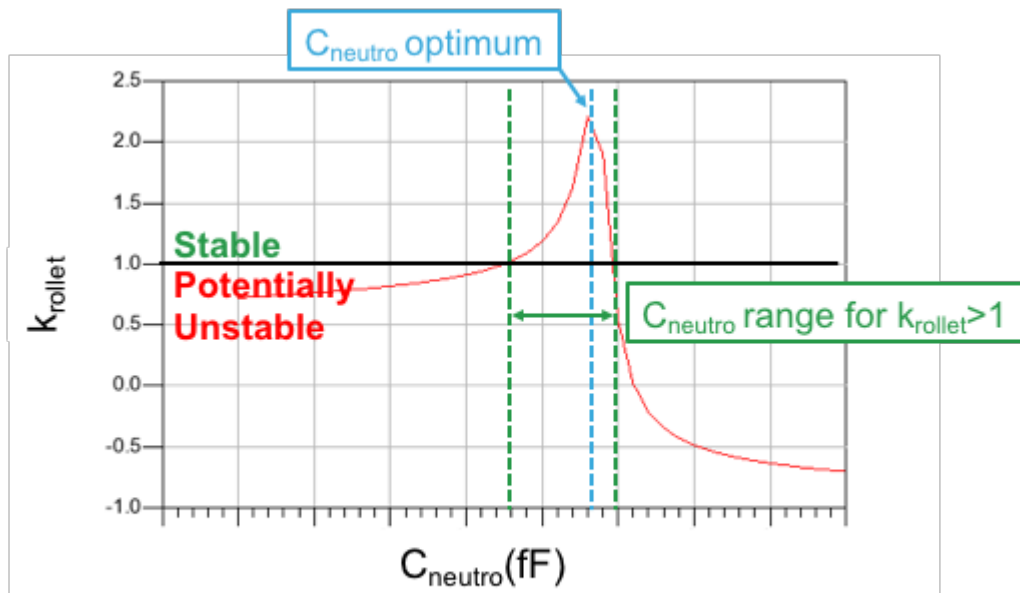


Figure II.7.10: Graphical C_{neutro} value determination based on k_{rollet} value

II.8 Conclusion - Design flow of mmW PA design

Throughout the chapter, we provided design topologies, requirements and techniques to design a complete power amplifier at mmW frequencies. As a conclusion of this chapter, it is interesting to provide the complete design flow, highlighting the sequence of essential steps necessary for a successful silicon implementation in advanced deep sub-micron technologies. Figure II.8.1 synthetizes the design flow, highlighting all the important steps in a power amplifier design. This methodology and the techniques presented in this chapter, when stated, have been used to design the power amplifier presented in Chapter III. Specific stage design steps are explored in the following chapter, targeting robust 28nm FD-SOI integration.

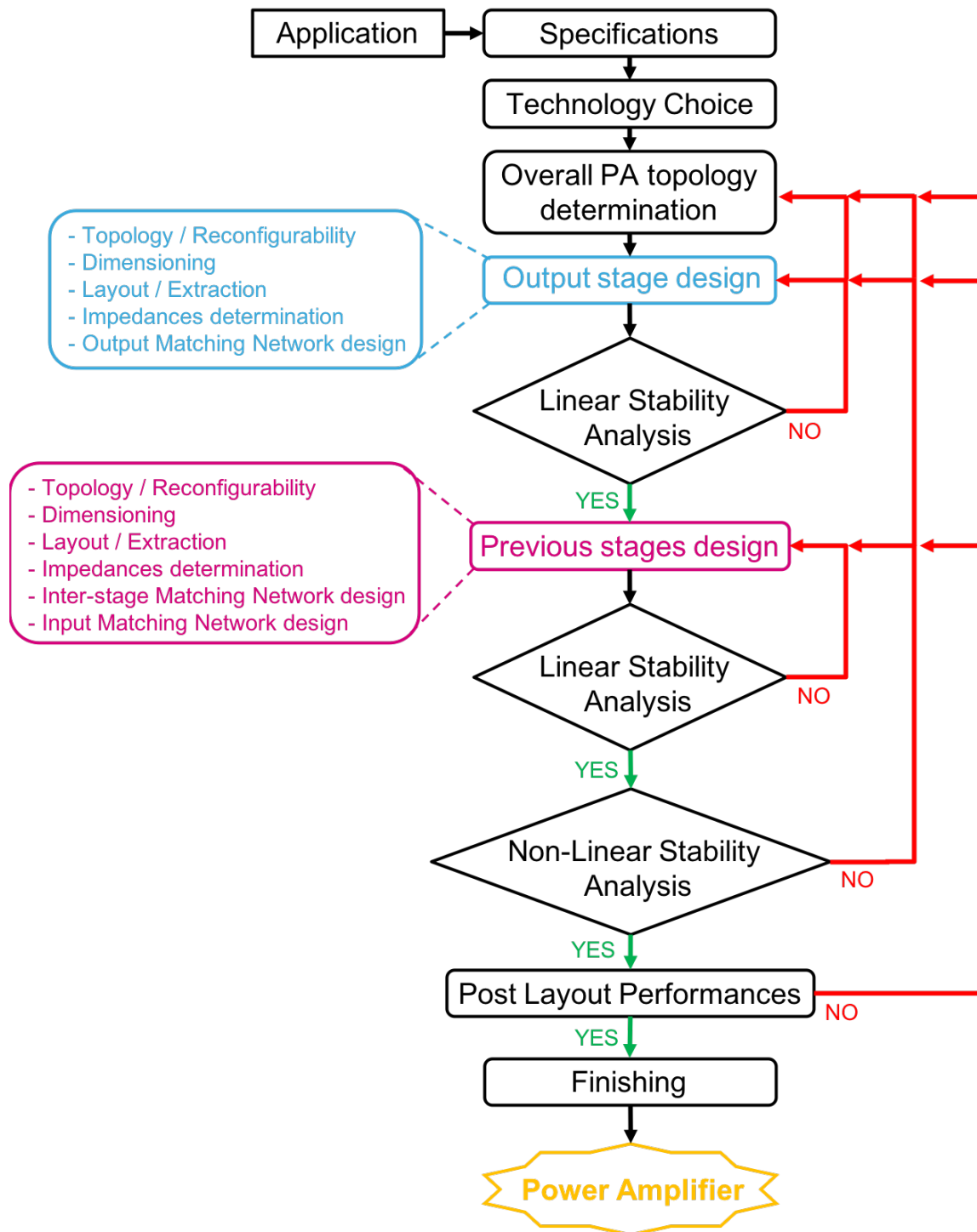


Figure II.8.1: Complete design flow of a mmW power amplifier in deep sub-micron CMOS technology

The specifications and the selected technology are the solid foundations of the design. The knowledge concerning the technology advantages and limitations is primordial to be able to select topologies and perform design choices throughout the power amplifier design process.

The first step in the design flow is then to define the overall PA topology: single or multi-stage, single-ended, differential or balanced... This has to be decided regarding the specifications and targeted applications. In deep sub-micron technology nodes, the parasitics at high frequency necessitate to choose topologies offering the best stability and reducing their impact. This differs from the classical less advanced technology nodes design flow or low frequency designs as the parasitics have a less critical impact. Expected performances at high-level can be evaluated with an early technology exploration. This will allow the designer to know the possibilities and the limits of the technology to better choose topology, dimensions and design techniques to achieve expected performances.

Then the power amplifier stages are designed successively from the output stage, that is the most critical for overall power amplifier performances, to the input stage. Each stage is designed following the quasi-similar scheme.

A topology is selected to fit the specifications and reconfigurability needs if necessary. The transistors and different elements composing the stage are then dimensioned. Several design techniques as presented in this chapter are implemented. The active part of the stage is then designed, with a special care for interconnections induced parasitic reduction. These parasitic elements must be extracted early in the process with tools like StarRCXT or QRC, in order to be taken into account during early post-layout simulations because they are critical at mmW frequencies. Optimal impedances at the output and input of the stage can then be determined using load-pull and source impedance sweep. The corresponding output matching network can be designed, with a special care for induced losses limitation. For this purpose, only thick top metal layers in 28nm FD-SOI technology should be considered for passive devices implementation. To determine the dimensioning of corresponding matching networks, it is possible to use the specific model provided in this chapter. Optimized fast and accurate EM simulations can then be conducted to design and refine the layout of matching networks.

Performances of the output stage can then be simulated and estimated while a linear stability analysis has to be performed. If the stage is unstable, the designer should reconsider the design and go back to the previous step. If the linear analysis is conclusive, the next step is to design the previous stages.

As for the output stage, the topology, dimensioning, layout and parasitics extraction have to be conducted first. The optimum impedances are then determined. Inter-stage matching network between the output of this stage and the input of the next stage is then designed.

Input matching network can also be implemented when the input stage has been designed. It corresponds to the last step of the design process before layout finishing involving ground planes, bias and supply path and pad integration. Each stage must satisfy the linear stability analysis conditions or need to be re-designed.

Then when full power amplifier is designed, post-layout simulations have to be performed. Non-linear stability has to be explored, if the conditions are satisfied, the performances under post-layout simulations can be estimated. If these stability conditions are not satisfied, the design should be modified.

Finally, if the performances obtained during post-layout simulations fit with the specifications, the power amplifier can be fully finished and is ready to be manufactured. If the performances are not sufficient, design must be corrected.

Chapter III: Reconfigurable balanced mmW PA implementation in 28nm FD-SOI technology

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Chapter III: Reconfigurable balanced mmW PA implementation in 28nm FD-SOI technology

In this chapter, we focus on a power amplifier implementation targeting the mmW 5G applications challenges highlighted in Chapter I. High performances are aimed in terms of efficiency, gain and linearity while gain reconfigurability for system level control in SoC is expected. For this purpose, the design flow depicted in Chapter II has been applied and several specific design techniques has been used in order to provide both high performances with robust integration.

First, active devices layout optimization and dimensioning are presented. Then the choice of the overall power amplifier topology and its implementation is discussed. Moreover, the design of each amplification stage and associated matching networks are depicted. We also discuss the points to check for a robust implementation targeting industrial production.

This circuit has been manufactured in 28nm FD-SOI technology. Measurement results and comparison with the state of the art are provided in the second half of this chapter.

Finally, perspectives and possible enhancement for future references are provided along with a new design for reconfigurable and wideband 90° hybrid couplers.

It is noticeable that this PA has been designed initially to operate around 37GHz. Therefore, passive elements are designed around this frequency, while the active devices have been designed for wideband operations. The provided measurements are shifted to 31GHz because of a mismatch between C_{neuro} and C_{GD} in simulation and manufacture, and is also discussed in this chapter.

III.1 Active devices

In the implemented circuit only LVT NMOS transistors from the 28nm FD-SOI are used. The design of active devices is crucial. While several parameters can be optimized directly from the Metal1-Pcell available in the design-kit with a wise dimensioning, the layout optimization is also important as it adds unneglectable parasitic elements. Both optimizations are discussed in this section.

II.1.2 Dimensioning

In order to design a transistor with a fixed total width W_{tot} from a transistor unitary cell several topologies are available. In fact, a transistor with a total width W_{tot} is composed by N_f number of unitary single-finger transistors exhibiting a width W_f (III-1)

$$W_{tot} = N_f \cdot W_f \quad (III-1)$$

Therefore, it is possible to directly implement this W_{tot} transistor with N_f fingers or it is possible to parallelize several elementary transistors cells (Figure III.1.1).

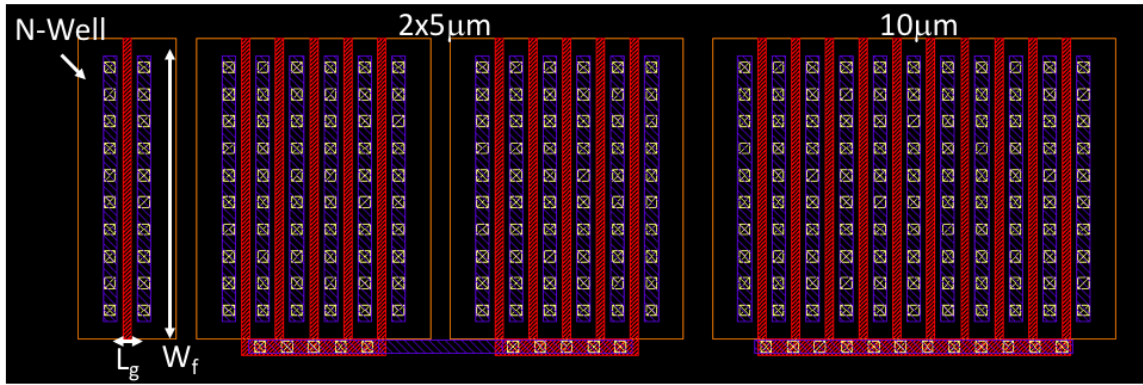


Figure III.1.1: Different transistors topologies

The sub-division advantage of a W_{tot} transistor in W_{el} elements is to multiply the gate accesses and so distribute the stress between gates. Therefore, both higher reliability and lower gate resistance are provided. The importance of low gate resistance will be discussed in the next section as it is an important part of layout optimization strategy. The use of multiple elementary transistors also allows a more compact and adaptive layout. Moreover, it limits the non-quasi-static effects that can occurs in large transistor, corresponding to a non-null difference of potential between the two extremities. Furthermore, large transistors also introduce higher intrinsic parasitic elements that make the impedance matching harder to implement.

The maximum W_{tot} of a transistor can be calculated with (III-2) from [LAR15-2]. At 30GHz the W_{tot_max} is around 330µm while at 37GHz this value is limited to 270µm. In this work we have designed an elementary transistor cell with 32µm W_{el} for easy integration (Figure III.1.2). Its optimized layout is depicted in Section III.1.1. The width of the transistors used in each stage are provided in corresponding Section III.3 sub-sections.

$$W_{tot_max}[\mu m] = \frac{10^4}{f[GHz]} \quad (III-2)$$

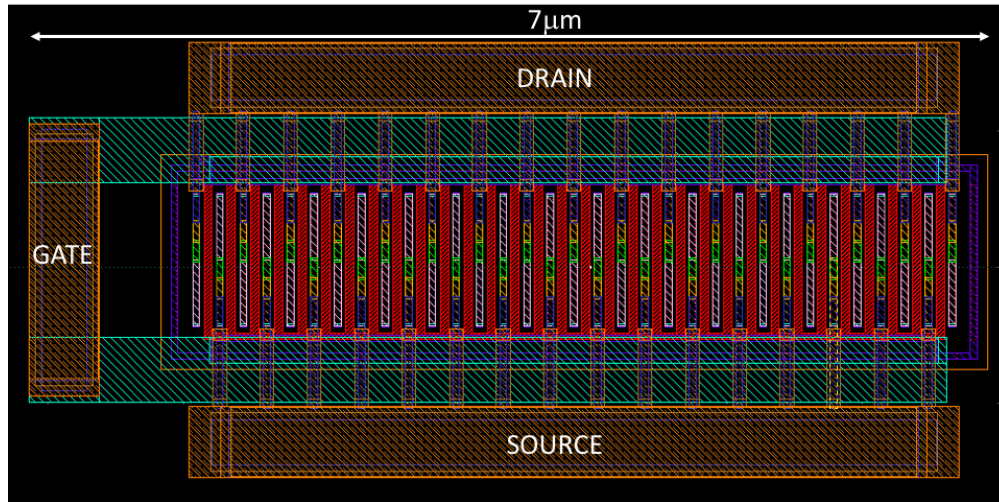


Figure III.1.2: Layout view of designed elementary cell

It is possible to define several adapted values of W_{el} because it has no significant impact over performances as long as the physical dimension remain small to avoid the non-quasi-static effects. The most important dimensions in the elementary transistor cell are the unitary transistor gate width and length.

Concerning the gate width W_f , a chart is available in [MOR99] (Figure III.1.3) to define the optimal W_f over several technology nodes for f_{max} enhancement.

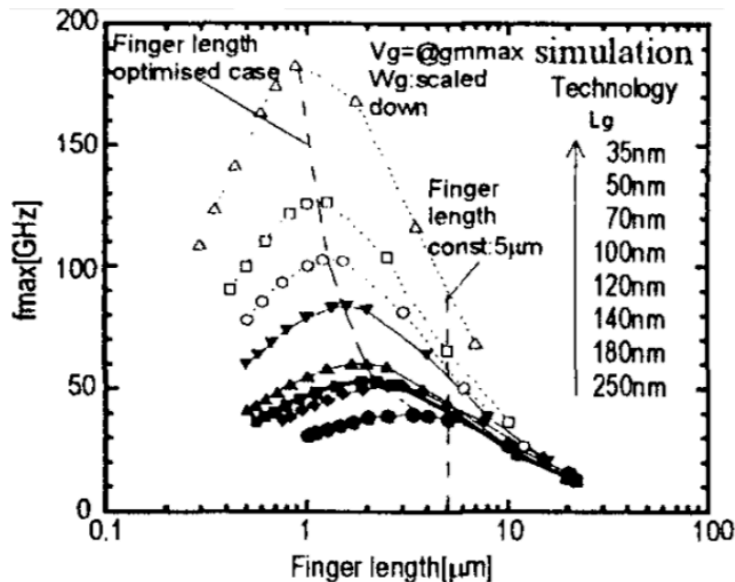


Figure III.1.3: Finger width determination depending on technology nodes [MOR99]

However, the 28nm technology node is not reported. It is possible to make the projection that the optimal gate finger width will be around $1\mu\text{m}$ if we follow the tendency provided in Figure III.1.3. In order to verify this value, we determined the f_T and f_{max} of a fixed Metal1-Pcell with a

total width of 400 μm , where the finger width is varied. The number of finger is adaptive at each iteration in order to always provide a 400 μm fixed W_{tot} . The results are reported in Figure III.1.4 and are issued from early simulations with the 28nm FD-SOI technology design kit version 2.5f.

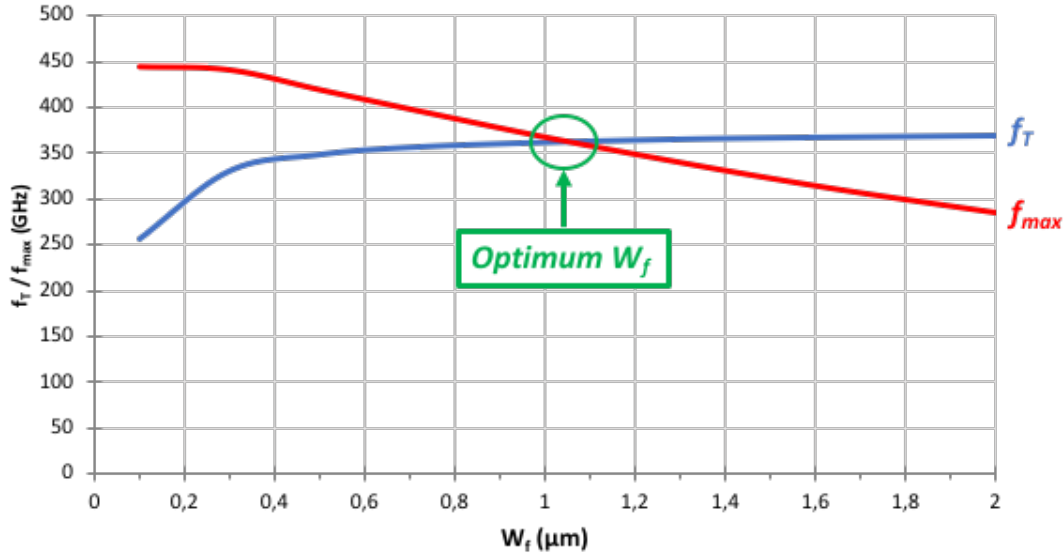


Figure III.1.4: f_T and f_{max} versus gate length for a fixed 400 μm transistor

The evolutions reported in Figure III.1.4 are linked to the intrinsic gate resistance and capacitance. Indeed, with a small value of W_f , the gate resistance is limited and higher f_{max} is achieved while lower f_T is reported due to higher gate capacitances. Therefore, it appears that the optimal finger width W_f in 28nm FD-SOI technology is around 1 μm and is in good agreement with the tendency depicted in [MOR99].

Concerning the gate length, in this design we implement a non-minimum gate length of 60nm. There are several reasons for this gate length value justification related to target both performances and robustness of integration. Indeed, a non-minimum gate length reduces the local process variability and therefore the performance dispersion between chips. Higher gate length also reduces the current per gate finger at high power and thus limits the stress in respect with electromigration. This phenomenon is developed in Section III.5.2. Furthermore, higher gate length is leading to lower C_{DS} parasitic capacitance and thus eases the output matching. Parasitic gate resistance and C_{GD}/C_{GS} ratio are also limited. In addition, 60nm gate length demonstrates great large-signal performances during early simulations. This choice is also ensuring comfortable transconductance at the desired frequency band. The Figure III.1.5 shows a comparison of f_T and f_{max} between 60nm and 30nm gate length transistors in function of the current density. For a current density under 500 $\mu\text{A}/\mu\text{m}$, a higher f_{max} is reported with 60nm gate length transistor. Furthermore, the f_T achieved by this 60nm transistor, around 200GHz, is good enough to provide great performances on the frequency band targeted in this work.

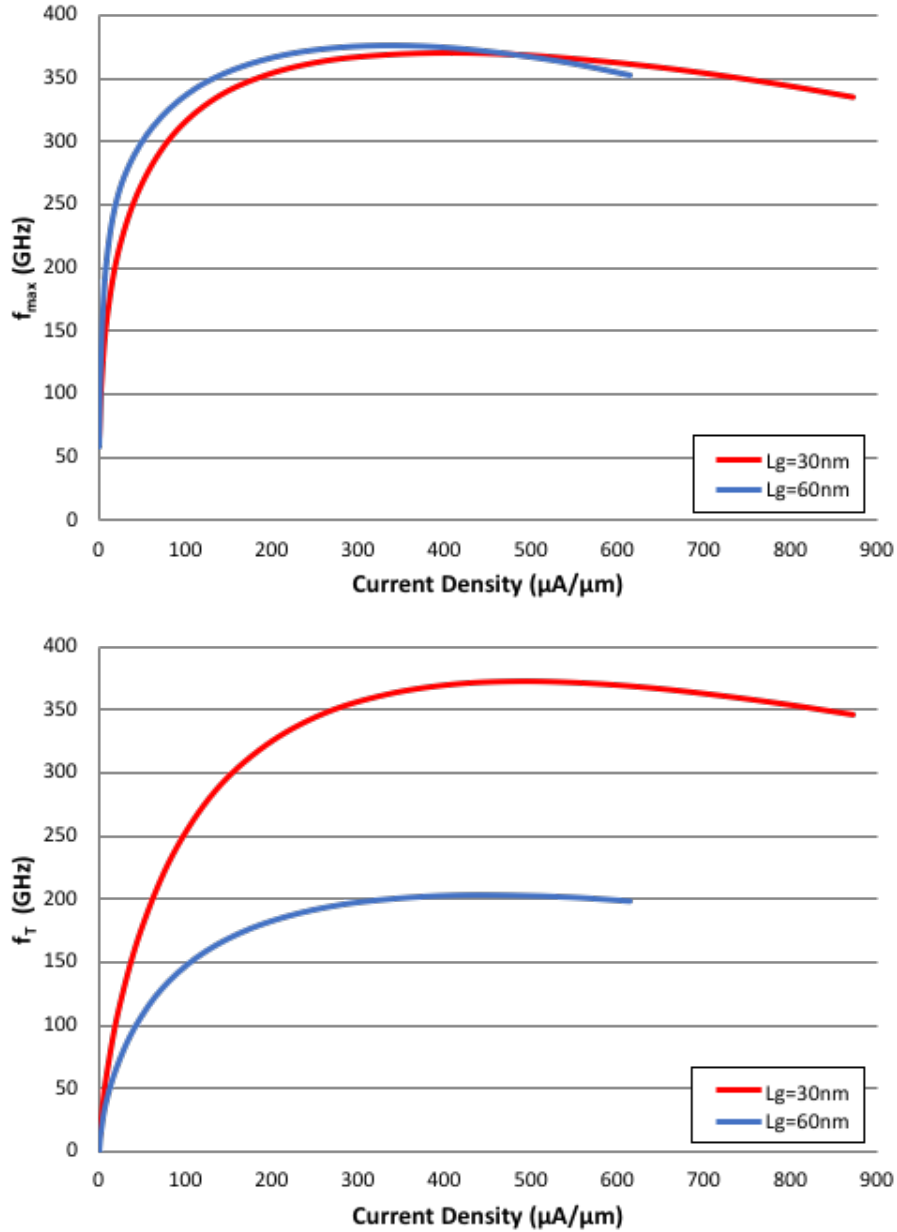


Figure III.1.5: f_T and f_{\max} comparison between gate length of 60nm and 30nm (DK 2.7)

III.1.1 Layout optimization strategy

Specific layout optimization strategy is mandatory in these frequency bands in deep sub-micron technologies, to maximize f_T and f_{\max} while reducing the parasitic interconnects. To illustrate the effect of parasitic interconnects over f_T and f_{\max} performances it is possible to estimate these parameters with (III.3) and (III.4) from the intrinsic transistor small-signal parameters with interconnects as available in Figure III.1.6.

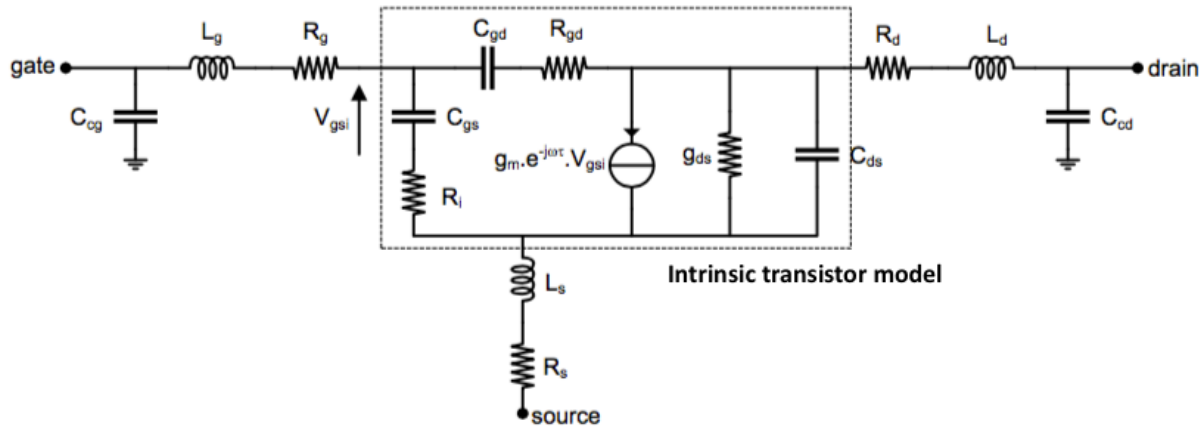


Figure III.1.6: Intrinsic transistor small-signal model with interconnections induced parasitic at high frequency [LAR15-2]

$$f_T = \frac{g_m}{2\pi \cdot C_{GS} \sqrt{1 + \frac{2 \cdot C_{GD}}{C_{GS}}}} \quad (III-3)$$

$$f_{max} = \frac{g_m}{2\pi \cdot C_{GS} \sqrt{(R_G + R_S + R_i) \cdot \left(g_{ds} + \frac{g_m \cdot C_{GD}}{C_{GS}}\right)}} \quad (III-4)$$

It is then noticeable that f_T and f_{max} performances are degraded by parasitic interconnections. These parasitics cannot be eliminated and so they have to be reduced in the transistor BEOL.

Therefore, several techniques have been used for this purpose, in order to optimize the BEOL of the elementary transistor cell that is part of the specific overall design optimization strategy.

In order to reduce the gate access resistance, a double gate access on $M2$ has been implemented and the gate access is routed from $M2$ to $1A$ thick top metal layer. In addition to f_{max} enhancement due to gate resistance reduction, this double gate access also allows to reduce the stress over gate access at high power and so provides higher robustness than a classical single gate access. As double gate access at poly-silicon level was not available in the design kit at the time this circuit has been designed, it had to be carefully implemented in order to fulfill the DRM rules. In later design kits, this option is now available directly for the RF transistors due to its inherent advantages. It is also noticeable that the poly-silicon gate access can be widened for higher resistance reduction.

Source and drain accesses can also be optimized in order to reduce the associated parasitic resistances and the C_{DS} capacitance. The classic layout method is to implement the full surface of each drain and source finger, from $M1$ to the desired top metal layer. However, while this solution allows source and drain access resistance reduction, it is leading to a large C_{DS} value due to the

fringe and parallel plate capacitance between drain and source fingers. Therefore, in this work we propose a staggered structure. From $M1$ to $M2$, the whole finger surface is implemented. Then external accesses are implemented from $M3$ to IA metal level, with iterative reduction of finger length in each metal layer. Therefore, less surfaces are in regard between interdigitated source and drain fingers while accesses resistances are reduced thanks to metal layer stacking. Corresponding fringe capacitances to the ground are also reduced for f_{max} and f_T improvements. Accesses width and the number of vias on each finger and metal layers have been optimized in respect with electromigration, that is explored in Section III.5.2. DRM and density rules have also been fulfilled. During the design optimization, all the capacitances and access resistances have been extracted with RCC extraction through StarRCXT tool.

In these conditions, effective f_T of 220GHz for the Metal1-Pcell and 190GHz for the full optimized BEOL elementary transistor cell have been simulated. A 3D view of this elementary transistor cell is available in Figure III.1.7, for better visibility only vias between IA and $B2$ are visible.

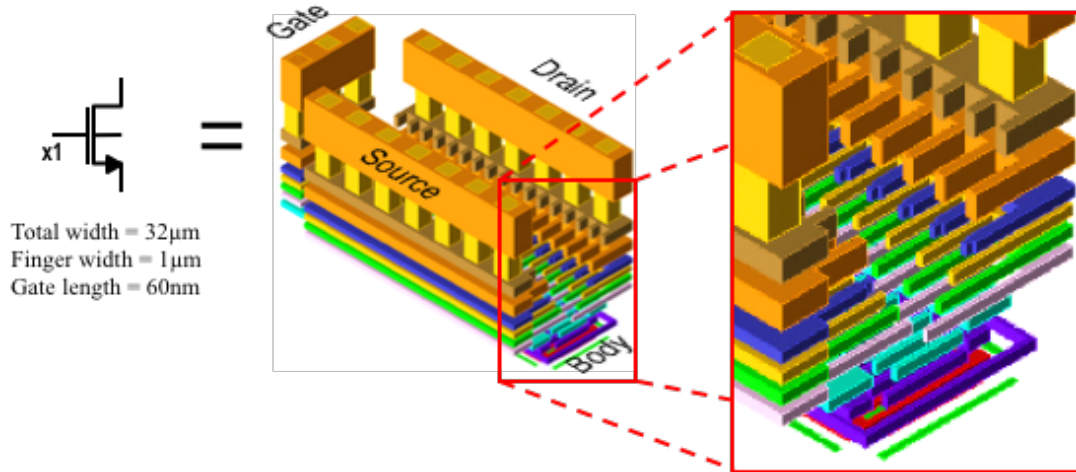


Figure III.1.7: 3D view of elementary transistor cell optimal layout

III.2 Power Amplifier topology

III.2.1 Choice of overall topology

In Chapter I, we have defined the specific needs for 5G mmW integrated power amplifiers that this work is targeting. The specifications in terms of performances can be summarized:

- Power amplifier is the most power consuming block in a transceiver. As a major 5G specification is to reduce the network power consumption, highly efficient PAs are expected with reduced power consumption.
- The complex modulations and waveforms that will be used for 5G will present high PAPR and are leading to stringent requirements concerning linearity.

- Gain reconfigurability is benefic for PA as it enhances system level control for SoC. Several modes also allow to modulate performances and power consumption depending on the use case. Large gain needs for 5G transceivers have also been identified.

Furthermore, we have developed that in beamforming phased array, the environment difference of each circuit can lead to antenna mismatch and to harmful voltage overshoot at the output of individual power amplifiers.

Therefore, the overall power amplifier structure must be chosen wisely to target robust integration in the 5G and SoC implementation context, targeting the previously depicted challenges.

In Chapter II, we exposed that balanced topology provides several advantages. Indeed, this topology offers robustness to input and output impedance mismatch and thus is ideal for beamforming phased array implementation. We have also exposed that the use of 90° hybrid couplers at the output performs power combining and so improves the P_{1dB} and maximum achievable output power by 3dB. Moreover, the 90° recombination of amplification paths with 90° phase imbalance reduces the IM3 by 6dB and achieves ACPR improvement. Therefore, impedance mismatch insensitivity, output power levels and linearity improvements are performed by balanced topology. For these reasons, we decided to choose an overall balanced topology for the power amplifier implemented in this thesis.

After the overall power amplifier topology determination, the next step is to define the amplification paths architecture. Both amplification paths of the balanced amplifier are identical. As we discussed in Chapter II, multi-stage topology allows higher gain than single-stage and is used in the designed power amplifier targeting high gain level. The number of stages is important to define as we highlight that PAE decreases and power consumption increases with the number of cascaded stage. For this purpose, as we target high PAE and low power consumption simultaneously with high gain, we decide to limit the number of stages to two.

Another choice regarding amplification paths has to be done between single-ended or differential topology. In Chapter II, we have exposed the advantages and drawbacks of both architecture. We have decided to use differential topology for both amplification stages of each amplification paths as it performs supplementary power combining and stability improvements thanks to virtual dynamic ground. The use of baluns and transformers for impedance matching and input splitting/output combining also provides advantages over robustness and reliability of the amplifier (Section III.5.1.). It also eliminates the need for DC blocking capacitors on RF paths. Furthermore, the center taps of baluns/transformers are used to apply bias and supply voltages and eliminate the need for choke inductors with large area footprint.

The overall power amplifier topology is shown in Figure III.2.1 while the specific design of each amplification stage is developed in Section III.3 and the impedance matching network

implementations are available in Section III.4. The balanced topology implementation is depicted in the following section.

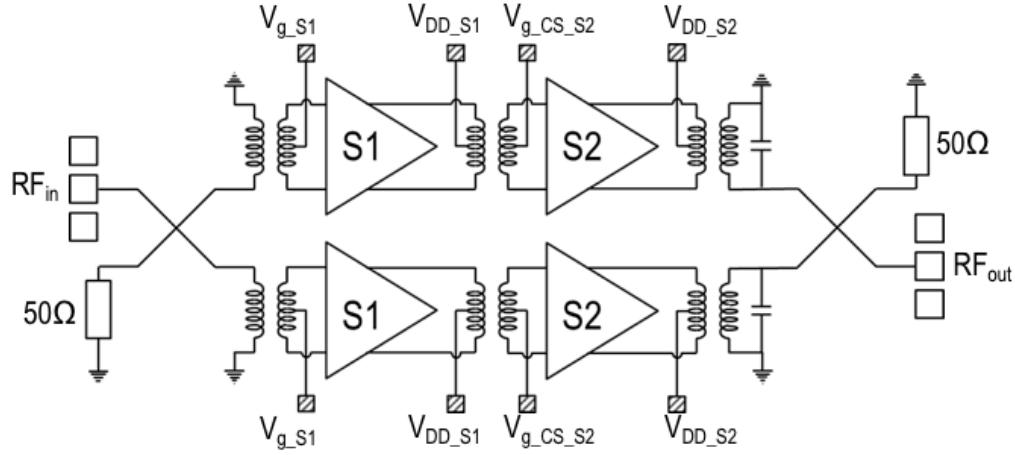


Figure III.2.1: Designed balanced power amplifier overall topology targeting 5G and SoC integration challenges

III.2.2 Balanced topology implementation

In the power amplifier designed in this thesis we decide to implement a balanced topology for its inherent advantages depicted previously. The fundamental design block necessitated for this topology is the 90° hybrid coupler and is depicted in this section.

The design of quadrature hybrid coupler is challenging as it has to be compact to limit the area footprint while limited losses are expected to avoid critical overall amplifier efficiency reduction. Several distributed 90° hybrid coupler architectures are available in the literature and have been extensively used in MMIC like branch-lines coupler or coupled-lines coupler (Figure III.2.2).

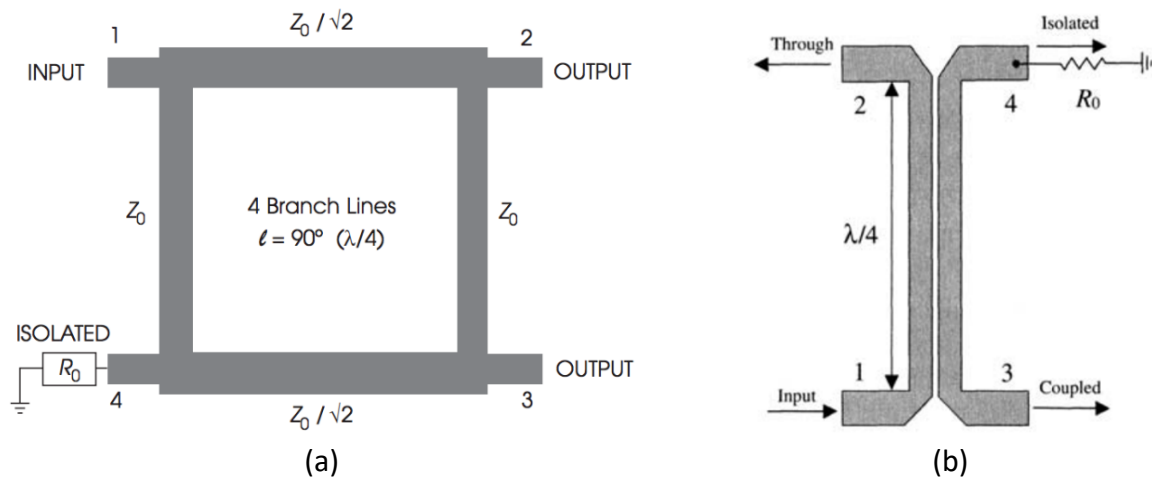


Figure III.2.2: Branch-lines (a) and coupled-lines coupler (b) illustration [BRE07]

However, integration of these couplers over expected 5G mmW frequency bands is challenging as they are based on $\lambda/4$ transmission lines that have a high area footprint around 30GHz.

Recently, a 90° hybrid coupler distributed design featuring twisted layout and compact size has been demonstrated in [KNO17], and has been validated in 28nm FD-SOI balanced design [MOR17], showing measured robustness to at least 3:1 VSWR conditions. Another advantage of this coupler that has been explored in [KNO17] is the possibility to adapt the size and design of the coupler, and therefore to propose a pragmatic design.

In this work we used this promising coupler design to perform balanced topology. We provide in this section the design procedure developed in [MOR17-2] and used in this work.

In order to design the 90° hybrid coupler, it is first possible to identify the coupler as a simple lumped elements model as presented in Figure III.2.3.

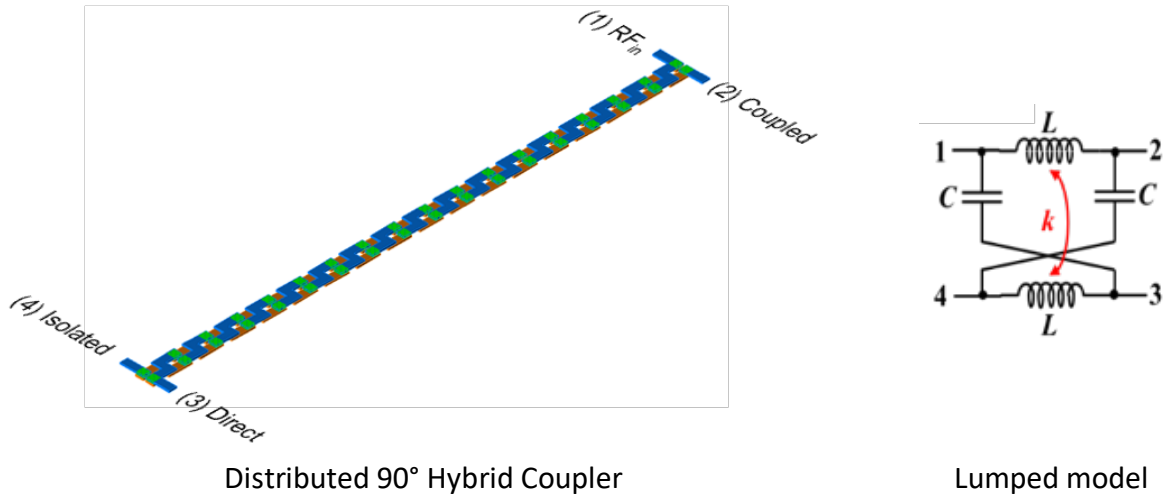


Figure III.2.3: Quadrature hybrid coupler and simplified lumped elements model

It is then possible to determine the values of L and C lumped elements from the equations (III-5) and (III-6), where f_0 is the coupler central frequency, Z_0 its characteristic impedance and k the coupling coefficient.

$$L = \frac{Z_0 \cdot (2 - k)}{2\pi \cdot f_0} \quad (III-5)$$

$$C = \frac{(2 - k)}{Z_0 \cdot 2\pi \cdot f_0} \quad (III-6)$$

Therefore, the coupler dimensioning is dependent on the frequency, targeted performances and coupling coefficient.

To synthesize these values, the starting point is a unitary twisted cell design (Figure III.2.4). The inductances and capacitances are distributed along the two tracks. This cell is implemented over *IA* and *IB* thick top metal layers in order to reduce the parasitic routing resistances. Its dimensioning is made to respect the DRC rules while showing sufficient inductance, capacitance and limited resistance on each track. The implemented geometrical values are 25μm, 5μm and 1.6μm for *L*, *W* and *S* respectively.

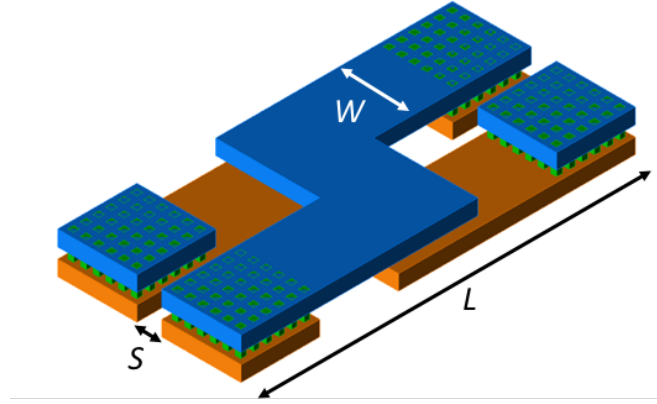


Figure III.2.4: Unitary twisted cell

The unitary inductance L_u , capacitance C_u and resistance R_u over each track can be extracted with EM tools.

Therefore, it is possible to design the hybrid coupler by cascading several unitary twisted cells in order to achieve the targeted inductance and capacitance estimated previously. The total inductance, capacitance and resistance of N cascaded unitary cells are:

$$L_{tot} = N \cdot L_u \quad (III-7)$$

$$C_{tot} = N \cdot C_u \quad (III-8)$$

$$R_{tot} = N \cdot R_u \quad (III-9)$$

Several parameters are important to verify in order to ensure optimal quadrature operation. The amplitude between both coupled and direct ports should be the same at the frequency of operation. In other words, the difference of amplitude $\Delta Amplitude$ should be 0dBm at central frequency. A phase difference, $\Delta Phase$ of 90° between outputs is also required. Losses in the coupler also have to be estimated and must be limited to maximize the efficiency from a system level. Frequency bandwidth is a key parameter to determine, 1dB $\Delta Amplitude$ bandwidth

will be taken as reference. These parameters are obtained by conducting small-signal analysis study with all the coupler terminations loaded with Z_0 .

$$\Delta Amplitude [dB] = |S_{21}[dB] - S_{31}[dB]| \quad (III-10)$$

$$\Delta Phase [^\circ] = phase(S_{21}) - phase(S_{31}) \quad (III-11)$$

In this work we implement a 50Ω 40GHz hybrid coupler based on 17 cascaded twisted elementary cells, leading to track lengths of $452\mu m$ and to total L and C value of 219pH and 43.8fF respectively for a k of 0.9. The performances of this coupler after post-layout simulations are available in Figure III.2.5. From these results it is possible to determine losses of 0.44dB at a frequency of operation of 40GHz with a $\Delta Phase$ of 92° . A 1dB $\Delta Amplitude$ bandwidth of 11.7GHz is observed, with a $\Delta Phase$ of $92^\circ \pm 0.2^\circ$ over the bandwidth.

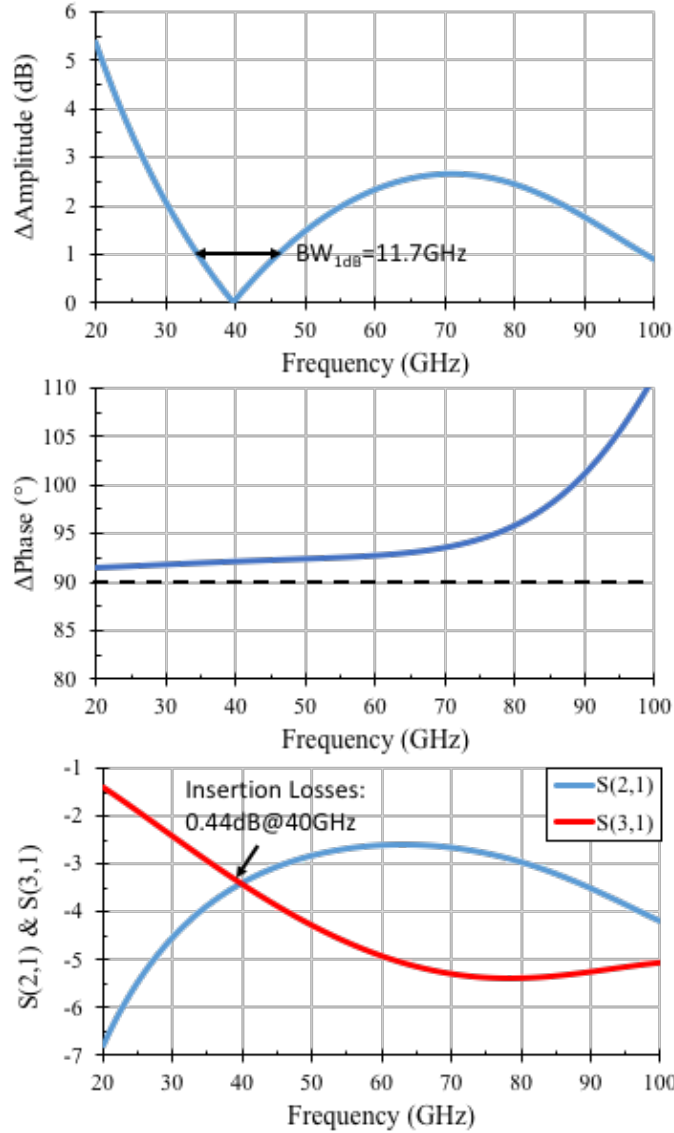


Figure III.2.5: 40GHz 90° hybrid coupler performance

In order to implement the balanced topology, ballast resistors are also needed. The role of ballast resistor is to dissipate the power induced by reflected wave in case of impedance mismatch at the input or output. Furthermore, this resistance must present the same characteristic impedance than targeted by the 90° hybrid coupler. In this case both ballast resistors at input and output are 50Ω. As this element has to dissipate reflected wave power, it cannot be implemented with a classical 50Ω poly-resistor as the temperature dissipation can lead to the thin poly-resistor destruction. For this purpose, we use the same metallic ballast resistor than the one integrated in [MOR17]. It is implemented on *B1* and *B2* intermediary metal levels. A ground ring is implemented around the metallic resistance from *M1* to *B2* while a substrate shielding ground plane is implemented under the structure from *M1* to *M2*. (Figure III.2.6).

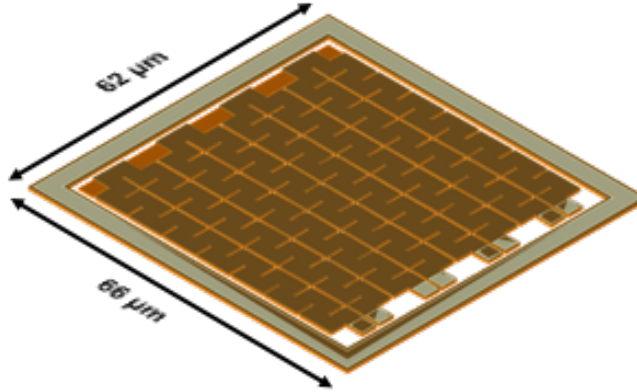


Figure III.2.6: 50Ω ballast resistor design

In addition, RF pads are important elements to design as they add parasitic capacitance to ground at mmW frequencies that must be limited and taken into account for the circuit design. For R&D oriented circuits, the pads must be designed in order to support the probe contacts while additional requirements concerning metal density or form factor are necessary for pads targeting flip-chip or wire-bonding for packaging. Passivation aperture has to be realized and must be large enough in order to permit efficient probe contact during measurements. For this work we used shielded RF pads topology in order to prevent any signal leakage through the substrate at these nodes. The shield is implemented on *M1* and *M2* lower and thinner metal layers. Pad area is implemented over *AluCap* and *IB* metal layers to ensure a low pad resistivity and a large area surface. Specific dummies are introduced between pad contact area and shield to ensure mechanical robustness for probe contact. The capacitance to ground induced by the RF pad and depending on the frequency can be calculated with EM simulation, with the equation (III-12). A layout view of the shielded capacitance is available in Figure III.2.7 while the pad capacitance value in function of frequency is exhibited in Figure III.2.8.

$$C_{Pad} = \frac{1}{Im(Z_{11}) \cdot 2\pi \cdot f} \quad (III-12)$$

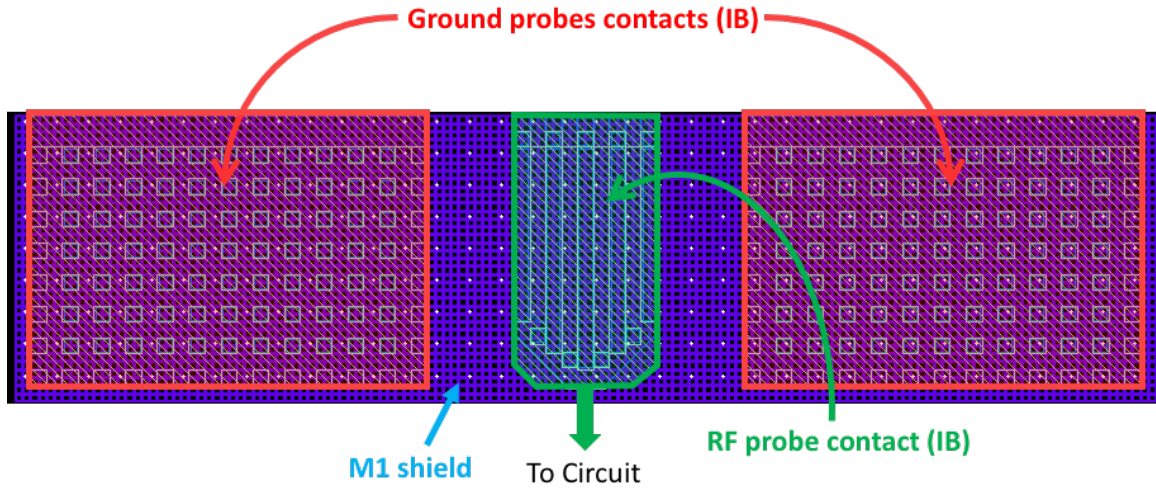


Figure III.2.7: Layout view of implemented shielded RF pad

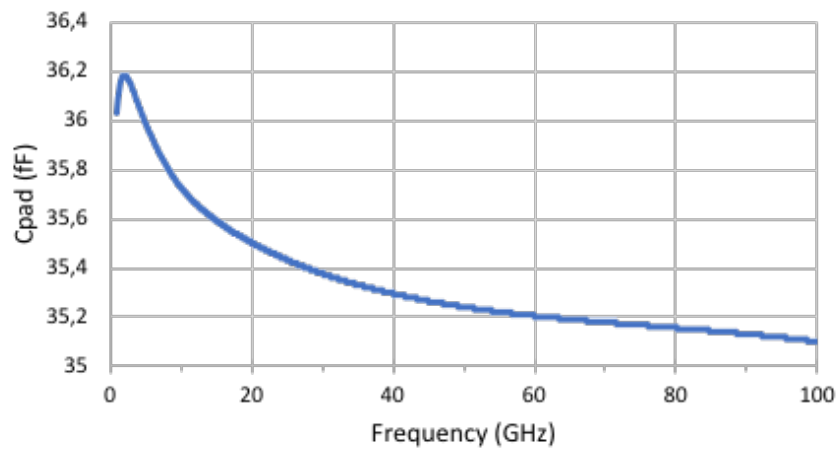


Figure III.2.8: RF pad capacitance to ground estimation (EM simulation)

III.3 Stages design

After the implementation of overall balanced topology elements targeting robust integration with enhanced performances, a specific stages design strategy is adopted to provide high performances, reconfigurability and robustness to industrial margin for SoC oriented integration. As depicted in the specific design flow provided on Chapter II, we first focus on the output power stage S2 and then on the driver stage S1 design.

III.3.1 Design and implementation of S₂ stage

In an amplification chain, the output power stage is expected to deliver power and gain. For this purpose, we decide to implement a cascode topology as it enhances gain, reverse isolation, output power and bandwidth compared to a common-source topology as developed in

Chapter II. Differential topology has been chosen in order to perform power combining and so improves P_{sat} and P_{1dB} by 3dB and enhances stability compared to a single-ended topology.

As discussed in Chapter II, the reconfigurability through body-biasing node should be implemented in the last stage of the amplification chain for linearity considerations. Therefore, we implemented body-biasing reconfigurability on S2 stage. The overall S2 topology is available in Figure III.3.1.

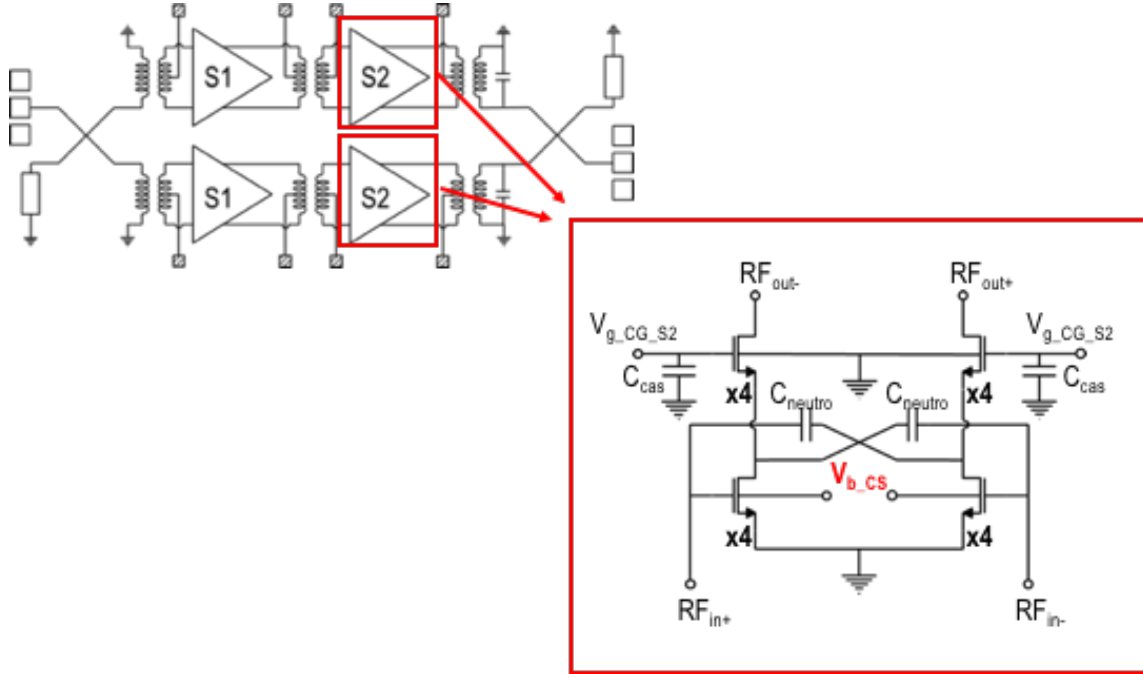


Figure III.3.1: S2 output power stage topology

In a cascode stage, the operating class of the overall structure is defined by the gate bias of the common-source stage. The common-gate stage is implemented to improve the output impedance of the structure, compared to a standalone common-source stage, in order to enhance the gain. Therefore, to implement body-biasing enabled gain reconfigurability over a cascode stage and perform dynamic and continuous operating class switching, the varying body-biasing node must be located on common-source stage. This power stage (S2) is biased in class AB under nominal conditions and can be dynamically switched to class A with body biasing. This stage is the first body-biasing enabled reconfigurable cascode structure implemented in 28nm FD-SOI technology in the literature.

Both CS and CG stages are implemented with 4x elementary transistor cells in parallel, leading to a W_{tot} of 128 μ m for both CS and CG transistors. This value W_{tot} has been determined as a compromise between gain, P_{sat} , peak PAE and power consumption performances. The W_{tot} maximum size is also limited by the input matching. Indeed, higher transistor length is leading to a lower input impedance. Therefore, input matching can be difficult to achieve if the optimal input

impedance is low as the impedance transformation ratio will be large. In this technology, the input impedance real part limit is around 10Ω , under this value the matching network will be very difficult to synthesize.

The cascode capacitance C_{cas} dimension of 200fF has been determined in order to distribute the nominal supply voltage equally between CS and CG transistors. This capacitance has been implemented with a MOM capacitor, with interdigitated fingers from $M2$ to $M6$ and is connected to the common-gate stage gate access on $M2$ metal layer.

Capacitive neutralization, as explored in Chapter II, has been realized over the common-source stage in order to improve reverse isolation, gain and stability. A C_{neutro} value of 33fF is optimal and has been estimated graphically as explained in Chapter II and illustrated in Figure III.2.3. C_{neutro} is implemented with MOM capacitor from $M2$ to $M5$.

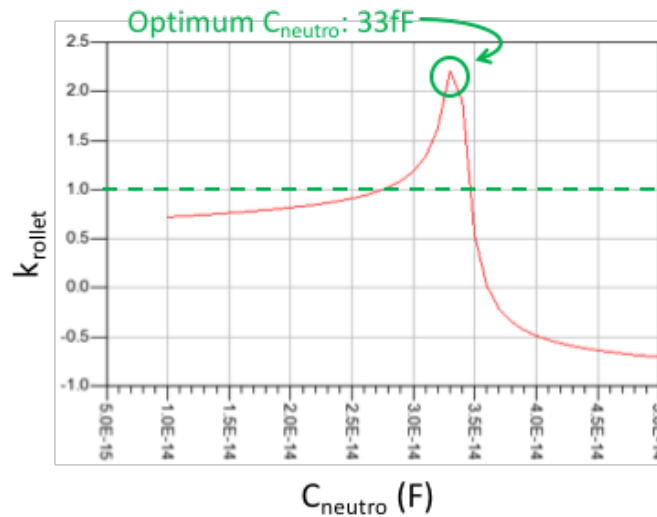


Figure III.3.2: S2 stage C_{neutro} determination

The realized layout of S2 stage is available in Figure III.3.3.

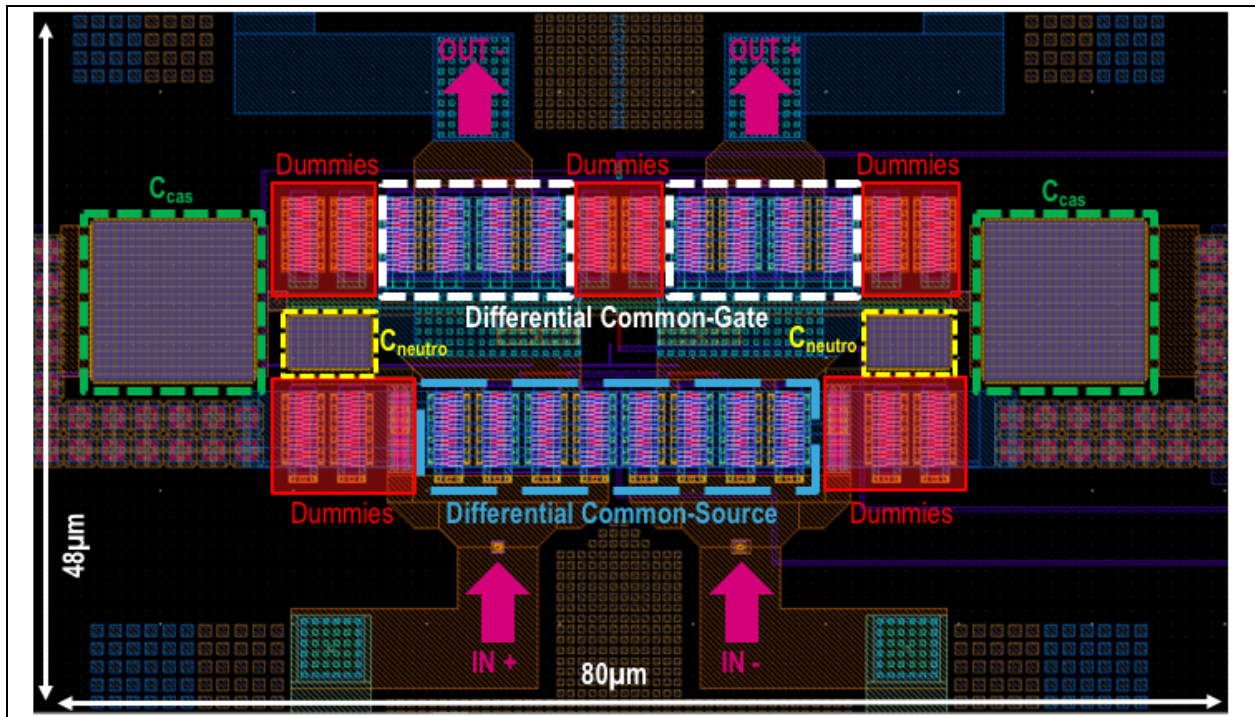


Figure III.3.3: S2 output power stage layout

Several layout optimizations have been realized in order to limit the parasitic elements induced by layout and routing and also the local variability, for a better robustness to industrial margins. Dummies transistors with full identical BEOL have been implemented aside all useful transistor stages. The role of these transistor dummies is to reduce the local process variability that could occur during manufacturing at such deep sub-micron node. In general, variations are occurring at the edge of an element array. Therefore, if a variability occurs during process, the dummies transistor will be impacted while the useful transistors in the array core will be “shielded”.

Concerning the differential common-source stage, gate access implemented on *IA* level is enlarged in order to reduce the gate access resistance at routing level. Antenna diodes have been inserted at each gate access on the differential structure and are needed due to the *AluCap* routing. Antenna diodes are necessary as a charge accumulation can occur over *AluCap* metal layer during the manufacturing. Therefore, these extra charges are flowing to the ground through the diodes instead of penetrating active devices by the gate and induce damage. The size of these diodes has been chosen to be as small as possible while fulfilling the design rules in order to limit the gate-to-ground added capacitance. An *IB* top thick metal layer rail is implemented over all the differential common-source in order to connect their source access to the lateral ground planes. The drain contacts are implemented on *IA* metal layer. The common-source stage gate bias is applied through input transformer center tap. All the distances between transistors are reduced to the minimum allowed by the design rules.

The common-gate stage design is also optimized for parasitic reduction. The gate bias of this stage is the only supply or bias applied directly to the node and not using any center tap of balun or transformer. The gate access is routed on *M2* metal layer as no RF signal is flowing through this node. Therefore, a different transistor BEOL topology has been used for common-gate transistors. It only differs from the common-source at the gate contact node, implemented only in *M2* and not routed up to *IA* metal layer. This also eases the inter-stage routing that we explain later in the section. Figure III.3.4 shows the differences between common-source and common-gate transistors. The transistors drain accesses on this stage are implemented over *IA* metal layers and are wide in order to reduce drain resistance and to offer better thermal resistance at high output power. Connections to output matching network are realized with a wide 10x7 via array between *IA* and *IB* for the same reasons.

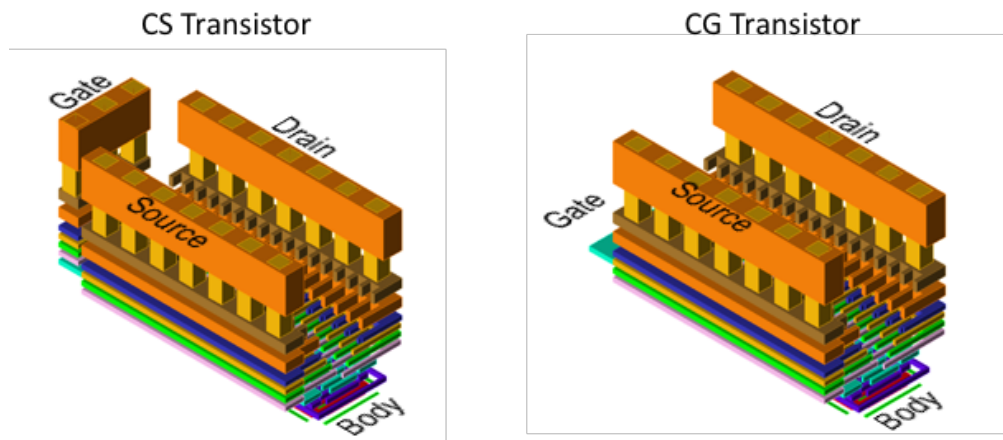


Figure III.3.4: Difference of BEOL between CS and CG elementary transistor cells

As developed in Chapter II, the inter-stage is a critical node in cascode topology. While the capacitance-to-substrate is naturally reduced by the SOI technology, parasitic resistances and inductances have to be reduced through layout. Therefore, wide inter-stage connection over *IA* and *IB* metal layers has been designed, with a large 16x5 via array. This node is also designed in respect with DRM density rules and electromigration purposes that are developed in Section III.5.2. Figure III.3.5 shows the interconnections between common-source and common-gate stages in the cascode topology.

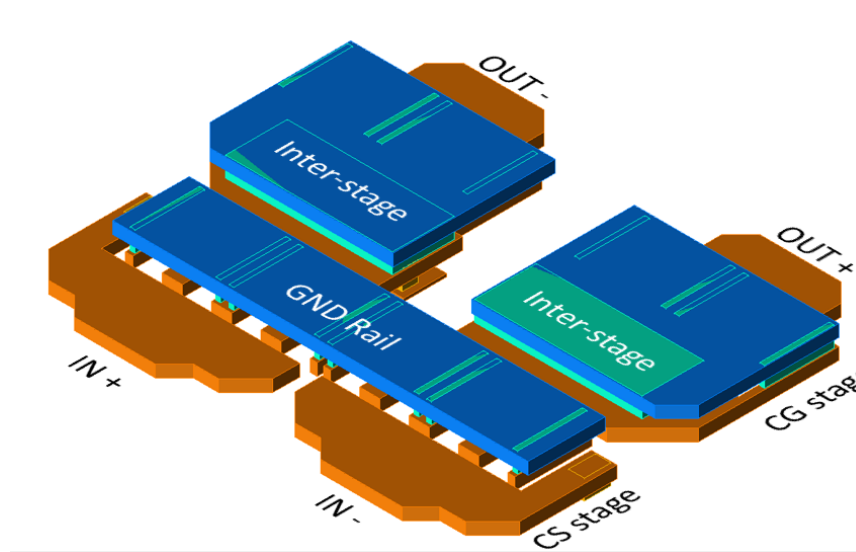


Figure III.3.5: Interconnections in the cascode stage

The C_{neutro} placement between gate and drain of the differential branches has to be integrated in design process very early as the routing induced parasitic on this node can affect the necessary C_{neutro} value. Therefore, routing should not be implemented on thin metal layers and routing length should be limited. For this purpose, we implement the C_{neutro} routing over intermediate metal layers $B1$ and $B2$ available in the technology. The accesses at gate side are connected through via array to IA . The routing is then integrated over dummy transistor (which BEOL layers differ from the others dummies), as near as possible from the stage input gate. Then the C_{neutro} MOM capacitor is placed at the interstage, as near as possible from the two stages for a compact design. Then the crossing occurs over drain accesses, one C_{neutro} is using a $B1$ routing while the other is using a $B2$ routing. They are then connected to the drain of common-source stage, at the interstage node, with a large via array. Even if the routing has been designed in order to reduce the parasitics, an EM extraction is mandatory before fixing definitely the C_{neutro} value.

Finally, the back-gate accesses for both common-source and common-gate stages are routed on $M1$ metal layer. $10k\Omega$ poly-resistors have been implemented over all body and gate bias accesses in order to avoid any RF signal leakage through these nodes. During the design optimization, all the interconnections induced parasitics have been extracted using KEYSIGHT Momentum EM simulator.

III.3.2 Design and implementation of S_1 stage

In a multi-stage amplifier, the role of the driver stage, is to provide additional gain while limiting the power consumption. For this purpose, a common-source configuration has been implemented as it provides enough gain for a limited power consumption compared with a cascode architecture. As the driver stage does not need to provide a high gain nor high power, the driver transistors width is generally chosen as half the power stage transistors width.

Therefore, we choose to use transistors with $64\mu\text{m}$ total width and composed by two elementary transistor cells depicted in Section III.1. As for the output stage, differential topology has been used to provide higher stability while performing power combining. The S1 stage topology is available in Figure III.3.6.

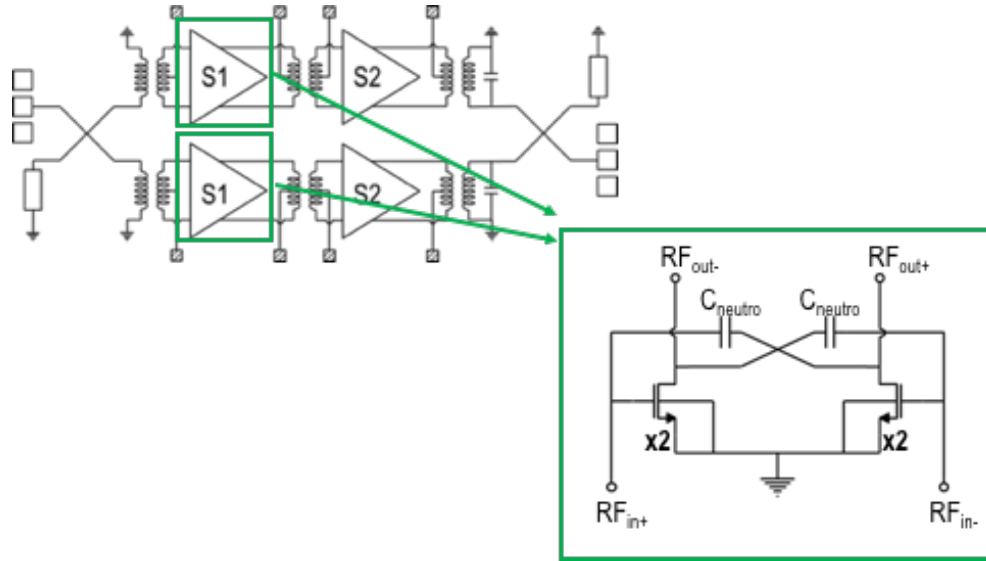


Figure III.3.6: S1 driver power stage topology

Differential topology has also been implemented in order to allow the use of neutralization capacitances to eliminate the Miller effect induced by C_{GD} over a common-source stage and so enhances stability, bandwidth and gain. In this stage, the C_{neutro} optimal value is 16fF. It has been synthesized with a MOM capacitor from M2 to M5. The realized layout of S1 stage is available in Figure III.3.7

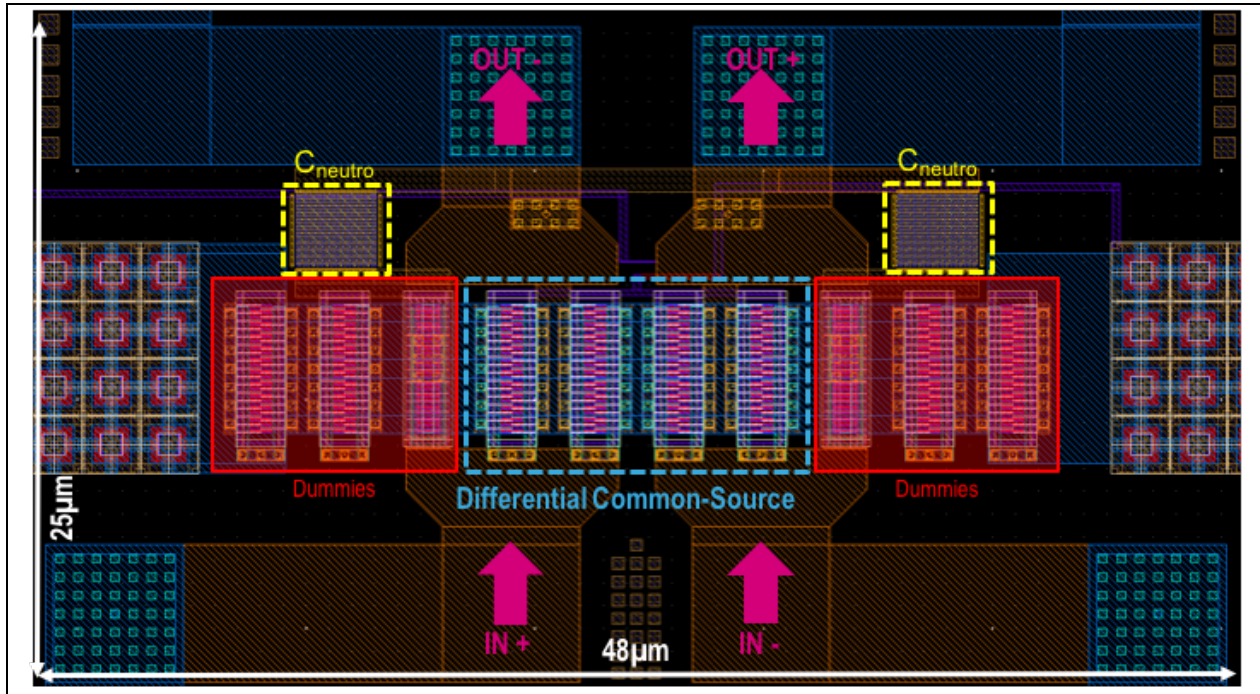


Figure III.3.7: S1 driver power stage layout

As for the output stage, the interconnections parasitics have been reduced in the design by using large gate and drain accesses over 1A thick metal level. A /B rail is implemented to connect the sources to lateral ground planes. Transistor dummies have been integrated to reduce the local process variability on this stage. The gate bias and drain supply voltage are applied through center taps of input/inter-stage matching networks. Body biasing is applied through a 10kΩ resistor to avoid any RF signal leakage. C_{neutro} routing is following the same strategy than in the previous section for the output stage. All the interconnections have been extracted with Momentum EM simulations during the design process. S1 stage is biased in class A in order to enhance the gain and linearity.

III.4 Impedance matching network implementation

While specific stage design is important to provide the best operations under robust reliability conditions for targeted applications, the design of matching networks is also very important to perform the right impedance transformations and thus enhances performances while limiting the losses to achieve a maximum of efficiency.

III.4.1 Output matching network optimization strategy

As described in the design flow at the end of Chapter II, the output matching network is the most critical matching network design of all the amplification chain and must be designed carefully to achieve the best performances for targeted applications. In this section, we propose a novel approach for output impedance matching of reconfigurable power amplifiers.

Traditionally, the ideal load impedance is determined with a load-pull simulation in nominal operating conditions. Then the matching network is designed and implemented to match the determined impedance. Even in the case of reconfigurability, the impedance is matched for the nominal operation. This is the case in reconfigurable circuits implemented in 28nm FD-SOI [LAR15] where the output load is chosen for the maximum linearity conditions.

However, with the body biasing, the intrinsic parameters of the active devices are modified. This is illustrated in Figure III.4.1, where C_{GG} , C_{DD} , C_{SS} , C_{GD} , C_{DS} and C_{GS} intrinsic capacitances are plotted versus body-biasing for several gate lengths for a 128 μ m transistor Metal1-Pcell.

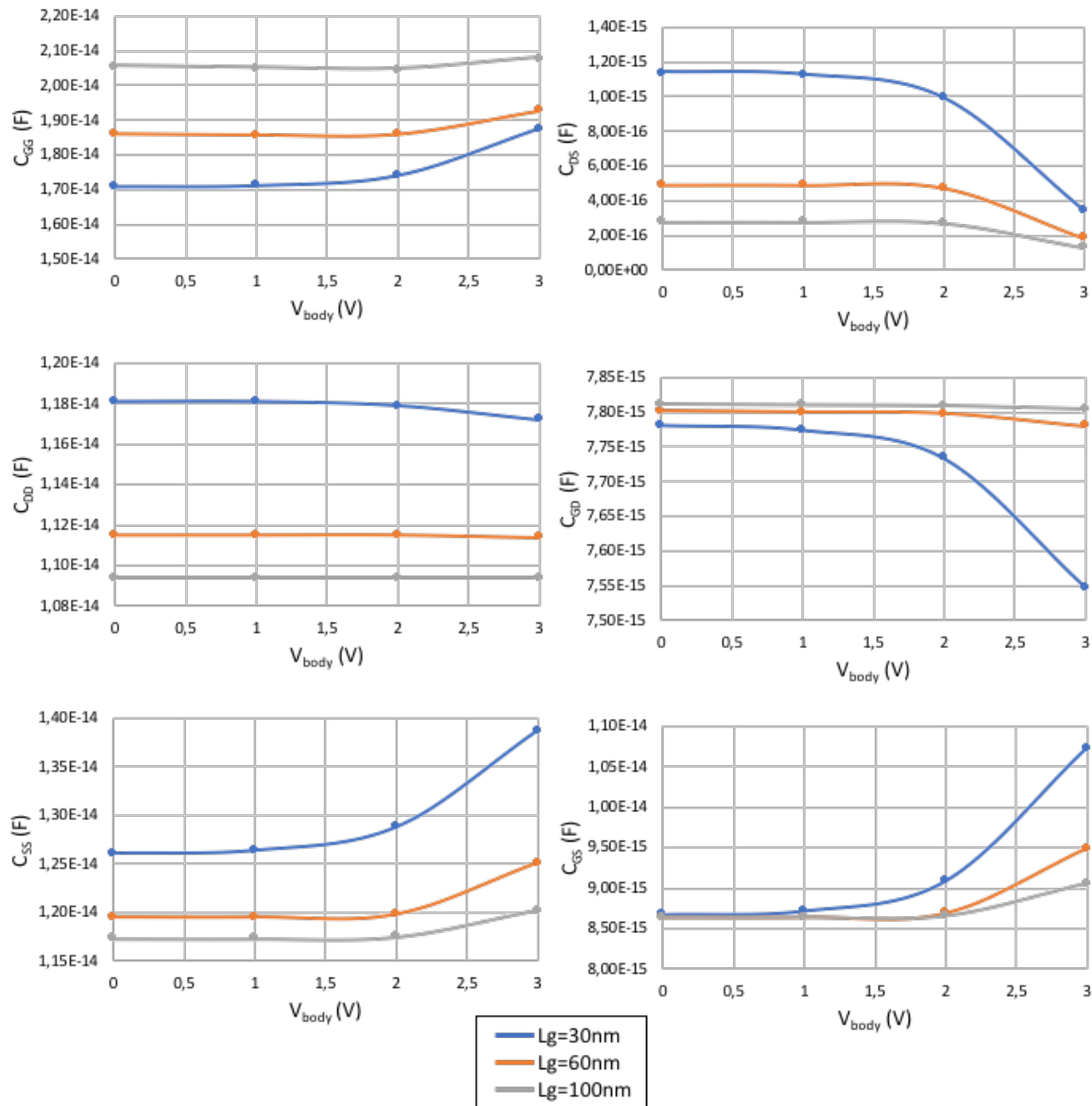


Figure III.4.1: Active device intrinsic capacitances evolution versus body biasing simulations

Therefore, the output optimal impedance of S2 stage varies depending on the body-biasing. This effect is noticeable by conducting load-pull for the extreme body-biasing conditions of 0V and 3V. The results of these simulations are available in Figure III.4.2.

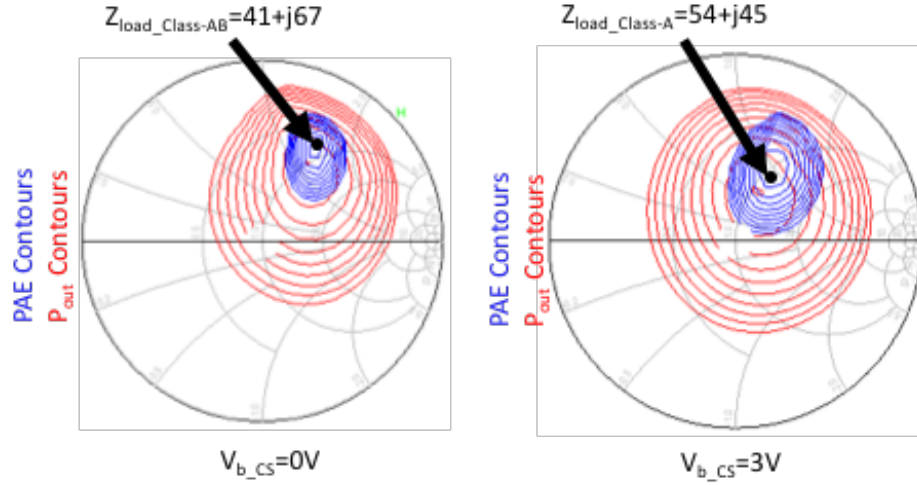


Figure III.4.2: Load-pull for extreme body-biasing conditions of 0V and 3V and associated optimal differential impedances

As it is noticeable, for a body-biasing of 0V, the differential optimal impedance to enhance both PAE and gain is $Z_{load_Class-AB} = 41 + j67$. In addition, for a 3V body-biasing, the optimal impedance is $Z_{load_Class-A} = 54 + j45$. Therefore, the choice of one or the other optimal impedance will lead to privilege an operating mode among the others. Therefore, in this work as we want an optimal matching for all operating mode, the choice of output load is made as a trade-off between both extreme body-biasing mode instead of choosing to privilege the maximum linearity mode. This choice is made to ensure quasi-constant PAE and output power among all operating classes and so avoid the efficiency decrease traditionally observed with this kind of reconfigurability [LAR15], [MOR17-2]. The chosen differential output load impedance is thus $Z_{load_optimized} = 60 + j62$. This output load impedance strategy choice is illustrated in Figure III.4.3.

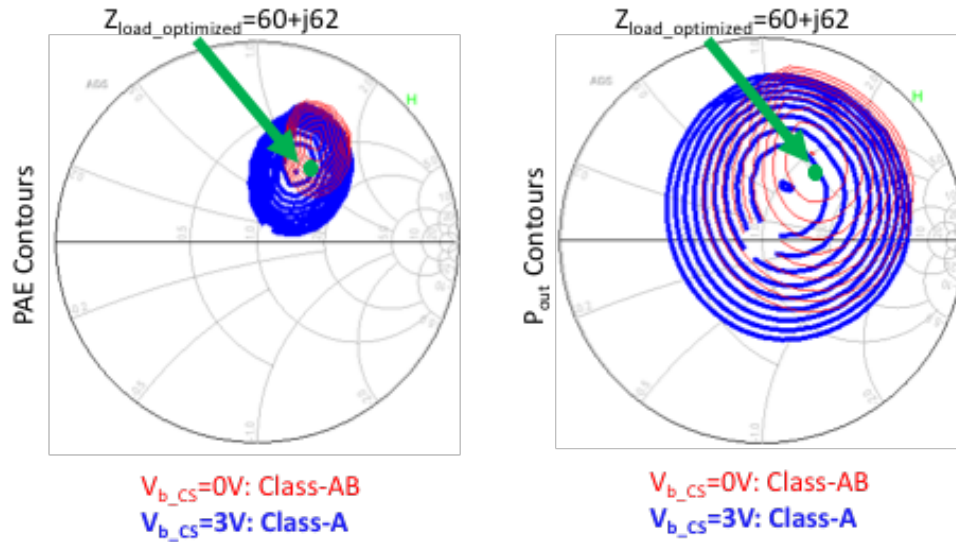


Figure III.4.3: Optimum output load determination strategy illustration

This output load matching is synthesized with a flipped balun in stacked configuration, transforming the optimum load to 50Ω and performing the output differential-to-single conversion. The primary winding is featuring two turns and is implemented over *IB* metal layer with a track width of $6\mu\text{m}$. The crossing between the two turns is made in *IA*, therefore no losses are added due to a crossing implemented in thinner metal layers. The secondary consists in a single turn implemented on *LB AluCap* with $6\mu\text{m}$ width. The secondary balun winding is positioned over the second turn of the primary in order to maximize the coupling. A 3D view and the associated dimensions are available in Figure III.4.4. A capacitance of 105fF is introduced between the two secondary terminations in order to refine the balun central frequency. This capacitance also broadens the balun bandwidth.

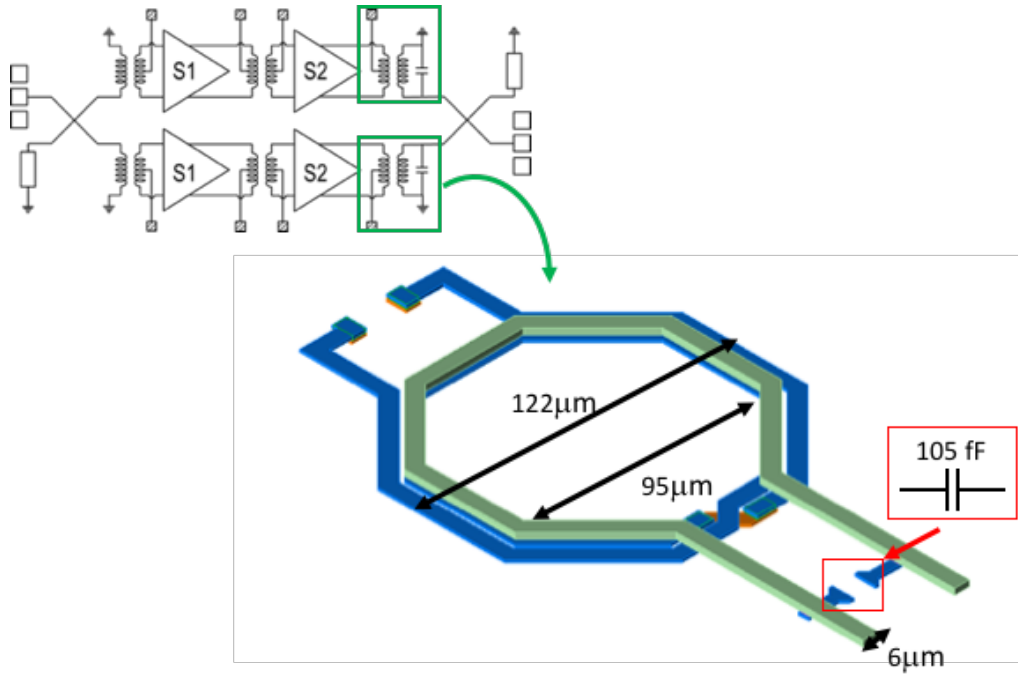


Figure III.4.4: Output matching network balun with associated dimensions

The performances of this balun are available in Figure III.4.5. A bandwidth of 28GHz is achieved from 22GHz to 50GHz. Insertion losses under 1dB are achieved from 14GHz.

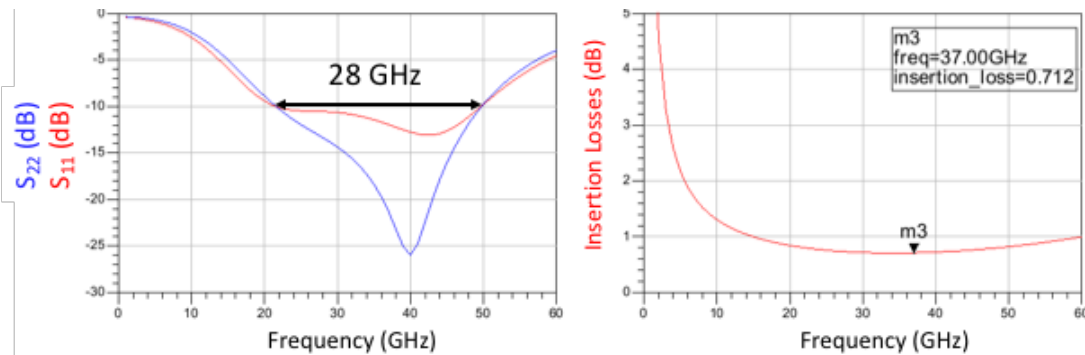


Figure III.4.5: Output balun performances

III.4.2 Inter-stage and input matching

The inter-stage and input matching networks do not need to be adapted to body-biasing conditions as the body biasing only affects the output impedance of S2 and no reconfigurability is implemented on S1. The input and output optimal impedances of S1 stage and the input optimal impedance of S2 stage have been determined with load-pull and source impedance sweep simulations. These identified differential impedance values are available in Table III.4.1

$Z_{in_opt_S2}$	$10+j52$
$Z_{out_opt_S1}$	$58+j106$
$Z_{in_opt_S1}$	$15+j102$

Table III.4.1: S1 and S2 stages optimum impedance values

As explained in the Chapter II design flow, inter-stage matching network is first designed. S1 and S2 stages are both differential. Therefore, a transformer is used to perform differential impedance transformation. Both primary and secondary windings are featuring a single-turn configuration. The primary is implemented over *IB* metal layer while the secondary is implemented over *LB AluCap*. Primary center tap is used to apply the driver supply voltage while the secondary center tap is used to apply common-source gate bias of the output stage cascode topology. A 3D view is available in Figure III.4.6 while the S-parameters issued from post-layout simulations and insertion losses are plotted in Figure III.4.7. S_{22} and S_{11} parameters are centered at 34GHz and 35GHz respectively with a 6GHz bandwidth. This transformer presents low insertion losses under 1dB from 17GHz with a value of 0.66dB at 37GHz.

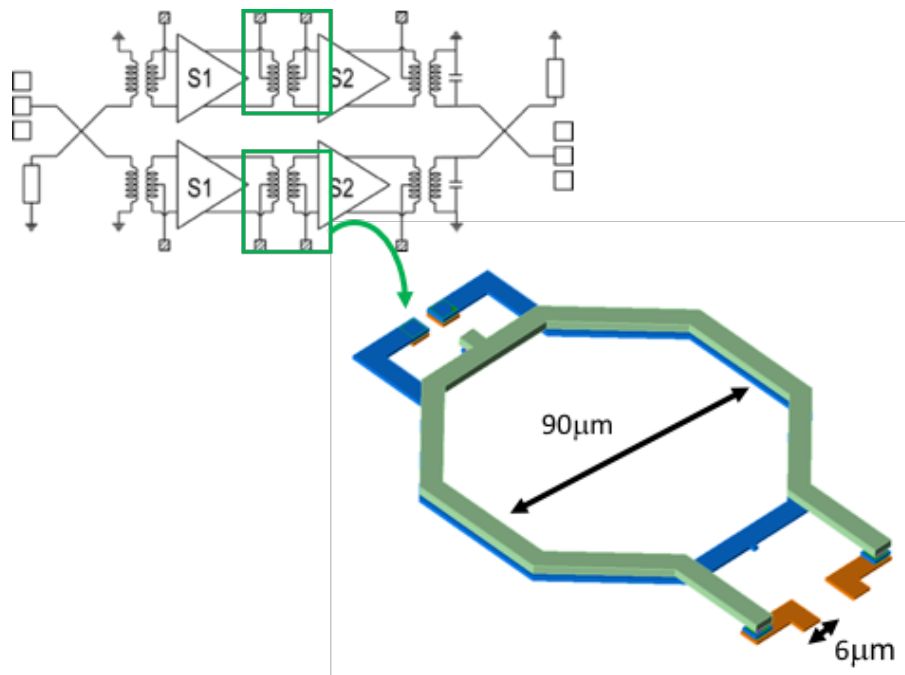


Figure III.4.6: Inter-stage matching network 3D view and dimensions

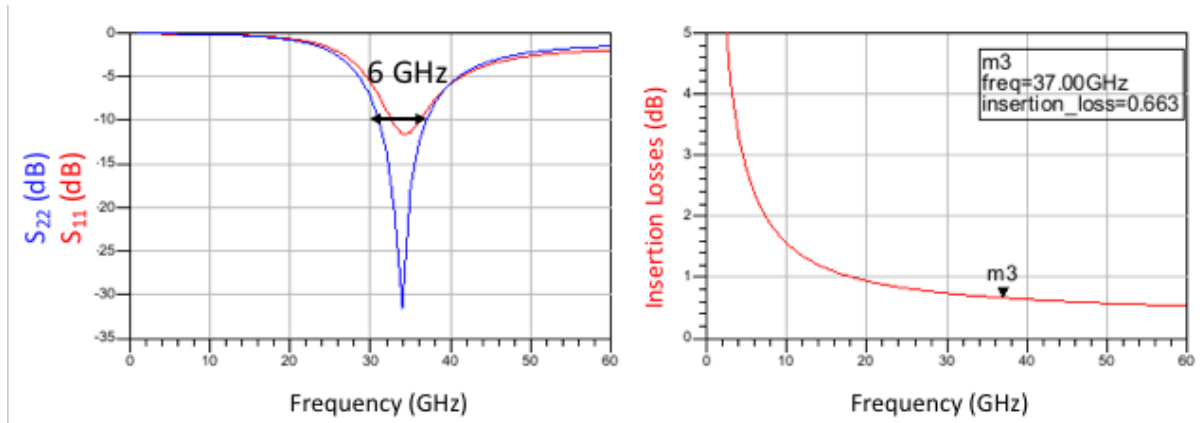


Figure III.4.7: Inter-stage matching network post-layout performances

Regarding the input matching network, it has to perform impedance transformation from 50Ω to $Z_{in_opt_S1}$ and single-to-differential conversion. Therefore, a stacked flipped balun has been integrated. The primary is featuring a one-turn configuration implemented on *AluCap*. The secondary winding presents a 3-turn topology over *IB*. The crossings between turns are implemented on *IA* in order to avoid excessive resistive losses. Part of the 2nd and 3rd turns is implemented over *IA* metal layer due to DRM design constraints. The primary winding is stacked over the secondary turn of the secondary winding in order to maximize the coupling. A 3D view is available in Figure III.4.8 while the S-parameters and insertion losses performances can be found in Figure III.4.9. The S_{11} and S_{22} present a central frequency at 34GHz and 35GHz respectively with a 7GHz bandwidth while insertion losses under 1dB are reported from 30GHz with a value of around 0.9dB at 37GHz. The center tap of the secondary is used to apply the driver stage gate bias voltage.

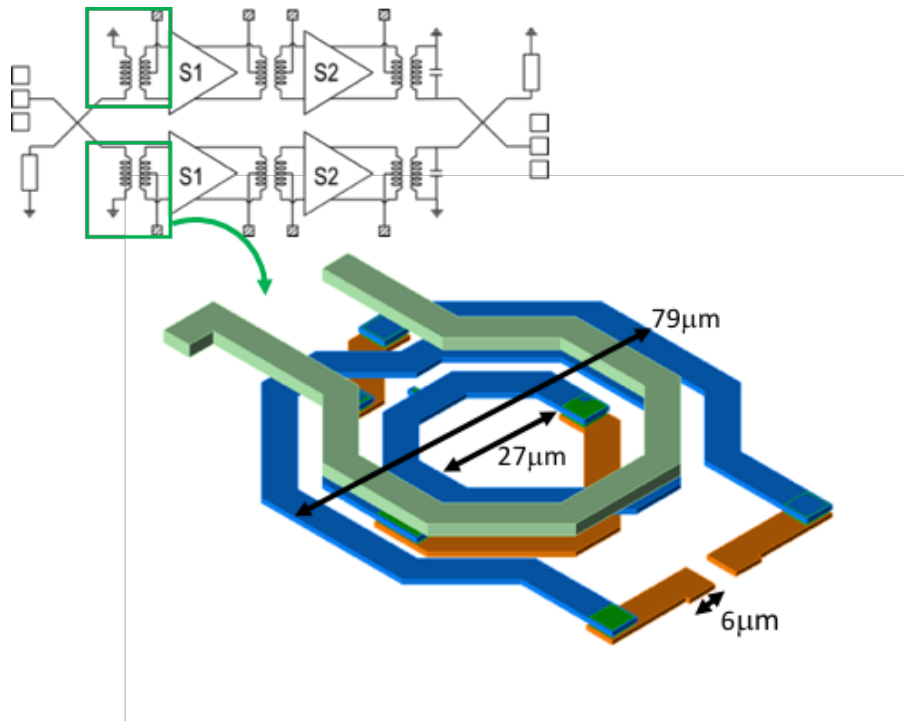


Figure III.4.8: Input matching network 3D view and dimensions

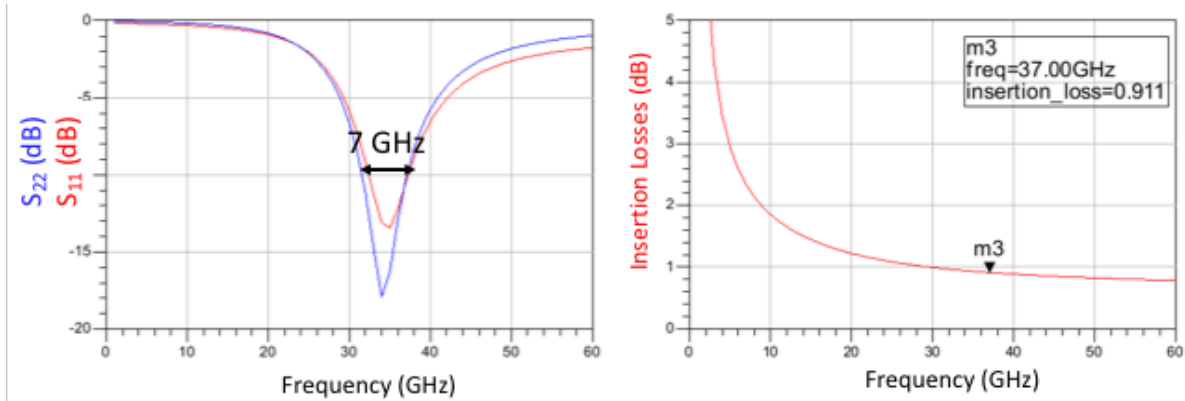


Figure III.4.9: Input matching network post-layout performances

III.5 Robust integration and reliability

In this work we targeted high performances, reconfigurability and robust integration for industrial applications. For this purpose, several reliability conditions have been checked like electromigration and safe operating area while ESD protections and optimized ground path have been implemented. These reliability purposes, mandatory for the targeted applications, are discussed in the following section.

III.5.1 ESD protection

Electrostatic discharges, ESD, can occur during manufacturing, measurement process and during circuit operation. This phenomenon is due to the environment and can be dramatic for integrated circuits as it can induce critical damages and failures.

Indeed, these discharges are critical for MOS transistors. When ESD is located on MOS gate, the gate oxide voltage is increasing and its destruction is occurring when breakdown voltage is reached. This phenomenon is amplified with CMOS technology downscaling, thinner gate oxide is leading to increased ESD sensitivity. When ESD is located on other transistor terminals, the associated PN junctions can suffer from avalanche breakdown phenomenon, increasing the device local temperature and causing permanent damages to the integrated circuit. Therefore, for a robust integration, it is mandatory to implement ESD protections in the circuit. Several ESD solutions are provided in the literature, depending on the frequency of use and the placement on the circuit nodes. At low frequency, clamping diode-based circuit protections can be implemented easily (Figure III.5.1). This avoid the excessive current penetration in the circuit core in case of ESD while diodes are in blocking state during normal operation. However, at mmW frequency, the diode parasitic capacitance presents a low impedance and can shorts the RF input/output signals. Therefore, this solution is not adapted to RF paths ESD protection at mmW frequencies.

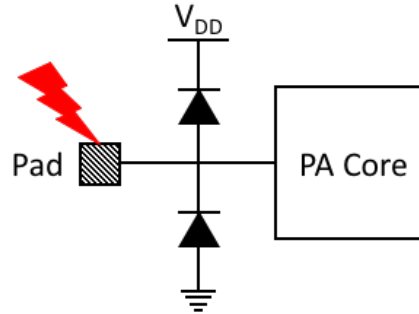


Figure III.5.1: Diode-based ESD protection

Other solutions are available to overcome this issue, based on stubs, clamping diodes with RF signal leakage blocking or transformers (Figure III.5.2). In this circuit, we decide to use baluns and transformers as input/output and inter-stage matching networks not only for impedance transformation purpose but also for the robustness they confer to the circuit. In fact, transformers primary and secondary are magnetically and electrically coupled but physically isolated, providing ESD protection for each stage of the PA on the RF paths. The use of transformers also provides galvanic isolation between stages. Therefore, the PA design is sectorized and robust to local ESD or stage temperature rise. However, it is not a sufficient condition to completely protect the circuit from ESD. Indeed, bias and supply voltages are applied on center taps of the baluns/transformers, and so are physically and electrically connected to the corresponding stages. To protect these

nodes from ESD, we integrate ESD protection on each pad as described in Figure III.5.1, as no RF signal is flowing at these nodes.

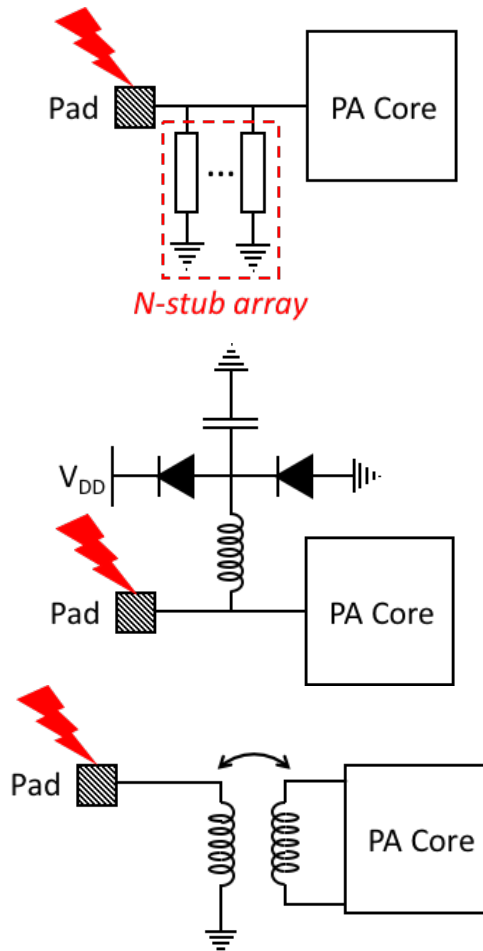


Figure III.5.2: Several ESD protection usable at mmW frequencies on RF paths

III.5.2 Electromigration

In [BLA69], the electromigration is defined as the atoms movement in a conductor, induced by the electron flow. The issue with this effect is that it can induce damages to the conductors, creating open and short-circuits. In the extreme cases it can destroy routing paths or passivity and provoke failure. Electromigration is dependent from current densities and junction temperatures. In advanced deep-submicron process nodes, this effect is a major concern for integrated circuits robustness. Indeed, both conductor width and thickness are downscaling and become more sensible to electromigration.

Therefore, in order to provide a robust integration, it is important to fulfill electromigration rules available in the DRM for several years of operation at fixed temperature depending on the targeted applications. These rules allow to calculate at which temperature the

power amplifier can operate for 10 years with no electromigration induced damages. These calculations can be done by considering the maximum current flowing at different circuit nodes.

In this design, we check carefully the electromigration conditions fulfilment. In practice, the temperature at which 10 years of operations are possible is limited by the number of vias in powercell transistor fingers due to the staggered structure presented previously. For the most extreme encountered measured conditions, corresponding to the maximum back-gate biasing mode operating at saturated output power (from the measurements available in Section III.7.2), electromigration rules are fulfilled for 10 years of operation at 100°C. By considering a lifetime derating available in the DRM, a 125°C electromigration reliability is achievable for 2 years in these extreme operating conditions.

III.5.3 Safe operating area

The safe operating area is the ensemble of voltage and current conditions and dynamics in which any circuit element can operate during a certain time without self-harm. In fact, an operation outside these conditions could lead to an instant destruction of the active device due to junction or gate oxide breakdown. In cascode topology, this check is also important as high voltage swing can occur in the inter-stage node between common-source and common-gate even if the DC voltage supply is distributed between both stages. Therefore, a SOA check is mandatory before fixing the operating conditions and can be done through Spectre simulator during a transient simulation. In this work, the SOA conditions have been carefully explored and fulfilled for all operating conditions, ensuring safe operations and a maximum of reliability even under maximum body-biasing conditions. All the measurement conditions performed and depicted later in this chapter strictly fulfill the SOA conditions.

III.5.4 Ground return path optimization

Ground path optimization is mandatory in deep sub-micron CMOS technologies as the thin metal layers available introduce parasitic resistance and inductance over the ground path. These parasitic elements impact can be critical as it can induce oscillations. This issue is critical in single-ended power amplifiers where a signal return path from the output to the input through the ground plane is possible and leading to oscillations. In this work, even if a differential architecture is used allowing higher stability, ground plane has been optimized to reduce parasitics in order to avoid unexpected performances degradation. Furthermore, it is also important to optimize the voltage supply plan for the same reasons.

For this purpose, in this work, the ground plane and supply voltage planes are composed by a large array of elementary cells. The thin and intermediary metal layers from *M1* to *B2* are stacked to create a wider ground. *IB* metal layer is also connected to the ground. The *IA* metal layer is used to implement the supply voltage plane. Therefore, the supply voltage plane is

implement between two ground planes. This creates a distributed decoupling capacitance between supply and ground planes, enhancing the stability of the overall structure.

The elementary ground and supply plane cell has been carefully designed to fulfill density rules while enhancing the number of via and the metal width to minimize parasitics. A 3D view of this structure is available in Figure III.5.3.

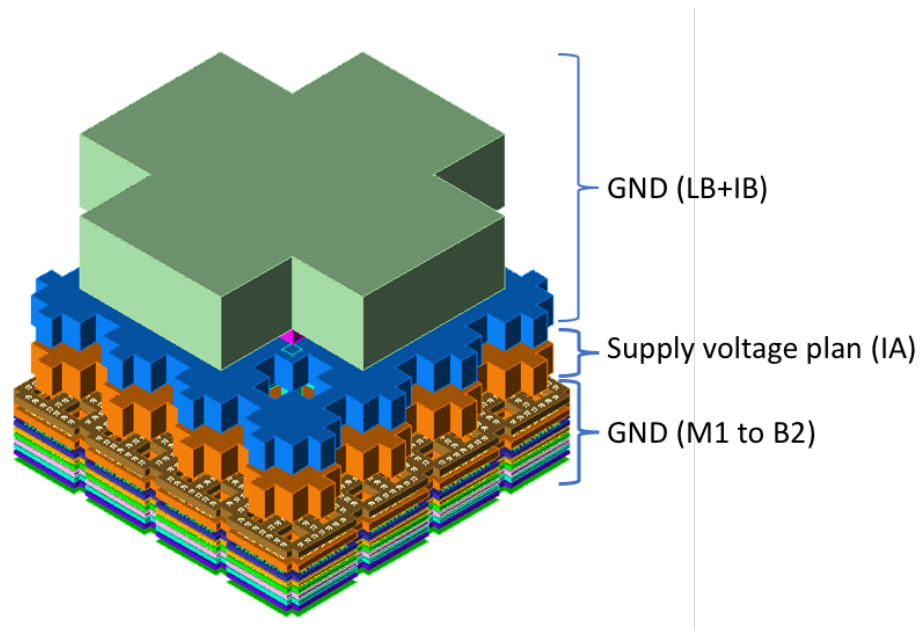


Figure III.5.3: Elementary ground and supply planes cell 3D view

It is also noticeable that two different supply planes have been implemented independently, one for the driver cell and the other for the power cell. Large MOM decoupling capacitors of 1pF are also implemented as near as it is possible from the center taps where the supply voltages are applied to the stages to enhance overall stability.

III.6 Measurements setup

The following sections focus on on-wafer measurements of the reconfigurable balanced power amplifier implemented in 28nm FD-SOI from STMicroelectronics presented previously. Figure III.6.1 shows a photomicrograph of the manufactured power amplifier.

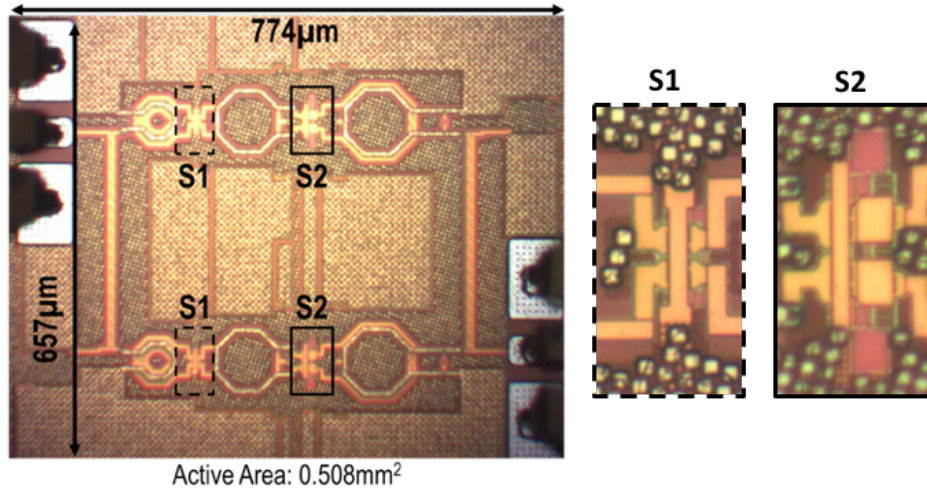


Figure III.6.1: Manufactured power amplifier photomicrograph

The mm-wave measurements have been realized at the NANOCOM platform at IMS laboratory in Bordeaux. Several test bench configurations have been used depending on the targeted measurements. These bench configurations are detailed in the next section followed by numerous small-signal and large-signal measurements. Body biasing voltage variations and the induced effects over the power amplifier performances and behavior are key points that have been explored during the measurement process. Frequency and temperature of operation variations have been performed in order to provide a complete study of the power amplifier performances and behavior under several measurements conditions. A statistical study featuring large-signal measurements over several on-wafer circuits' locations has been performed in order to quantify the process variability impact over performances. Finally, a comparison of the measured power amplifier performances with the state of the art is provided with a discussion regarding technology and topology choices impact over performances of the reported power amplifiers operating at millimeter-wave frequencies.

The following sections target to present the performances reached by the designed power amplifier. It illustrates operating conditions choices and estimate the robustness and reliability of the design. The reconfigurability abilities enabled by the extensive use of body biasing voltage tuning, a 28nm FD-SOI technology flavor described in the previous chapters, are also highlighted.

III.6.1 Small-signal analysis test bench

Small-signal measurements provide a frequency analysis around the biasing point with a linear and low power input signal. In order to estimate the S-parameters performances, small-signal measurements have to be performed and a test bench is set up for this purpose. We used

a 2-port PNA Network Analyzer, reference E8361A from Keysight, delivering -27dBm from 1GHz to 60GHz, connected to Ground-Signal-Ground, GSG, mmW probes through cables. A 2-port calibration has been made using standard SOLT calibration procedure featuring short, open, through and 50 Ω load references on impedance standard substrate. Thanks to the calibration method, losses into cables and mmW probes are estimated and de-embedded from the measurements. The device under test, in our case a circuit on a quarter of wafer, is placed on a heating chuck from ATT Systems, enabling chuck temperature sweep from ambient and up to 125°C in order to provide small-signal measurements with variable temperature conditions. Finally, supply, bias and body bias voltages are applied thanks to four Keysight E3631A DC supply sources through two GSGSGSGS probes. A scheme of this test bench is available in Figure III.6.2.

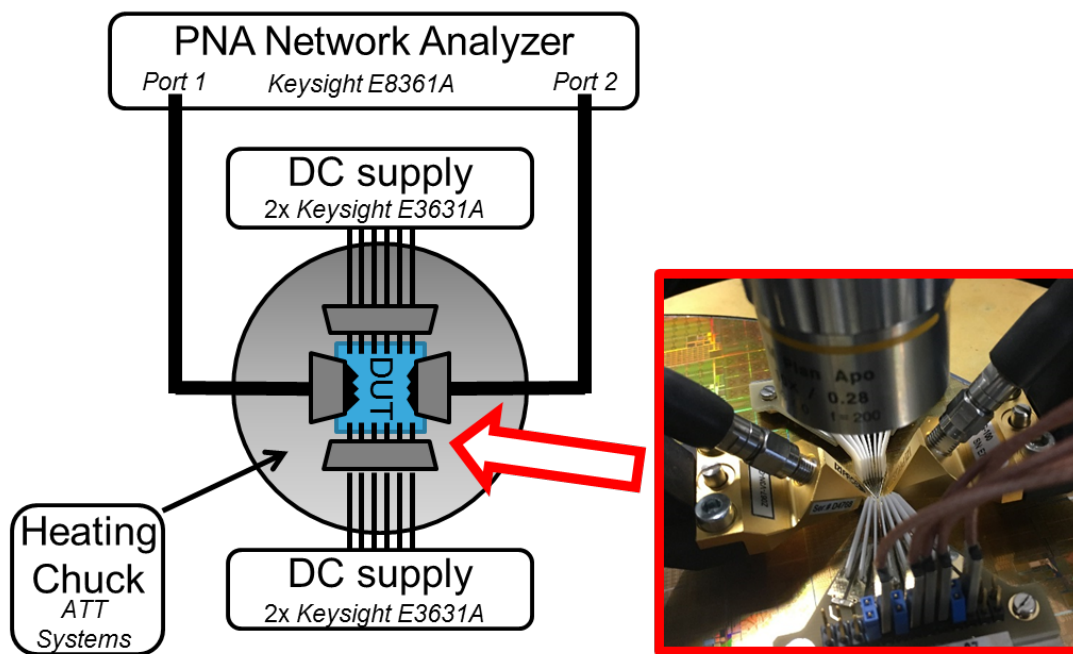


Figure III.6.2: Small-signal measurements test bench

III.6.2 Large-signal measurements test bench

Large-signal measurements illustrate the performances reached by the power amplifier under single-tone input signal with a power variation covering all the amplifier operating range to allow linearity exploration. For this purpose, a bench for continuous-wave large-signal measurements have been set up. This bench is featuring a power source SMF100A from Rohde & Schwarz at the input, delivering -20dBm to 10dBm power at desired frequencies. A power-meter E4418B from Keysight is placed at the output to measure the output power delivered by the circuit. DC voltages are applied using four DC supply sources E3631A from Keysight through two GSGSGSGS probes. As for small-signal analysis test bench, the same heating chuck is used to set temperature to desired levels. A computer controls and reads parameters like voltages, currents, input/output powers. The computer is also connected to RF source, power-meter and DC supply devices. A software from Focus is used to control the previously cited parameters, compute the

results and calculate automatically from measurements the parameters like PAE_{max} and power gain. Losses in cables and GSG mmW probes are estimated for each frequency of measurements and are de-embedded from the measurements. The power-meter is calibrated using standard procedure. A scheme of this bench is available in Figure III.6.3.

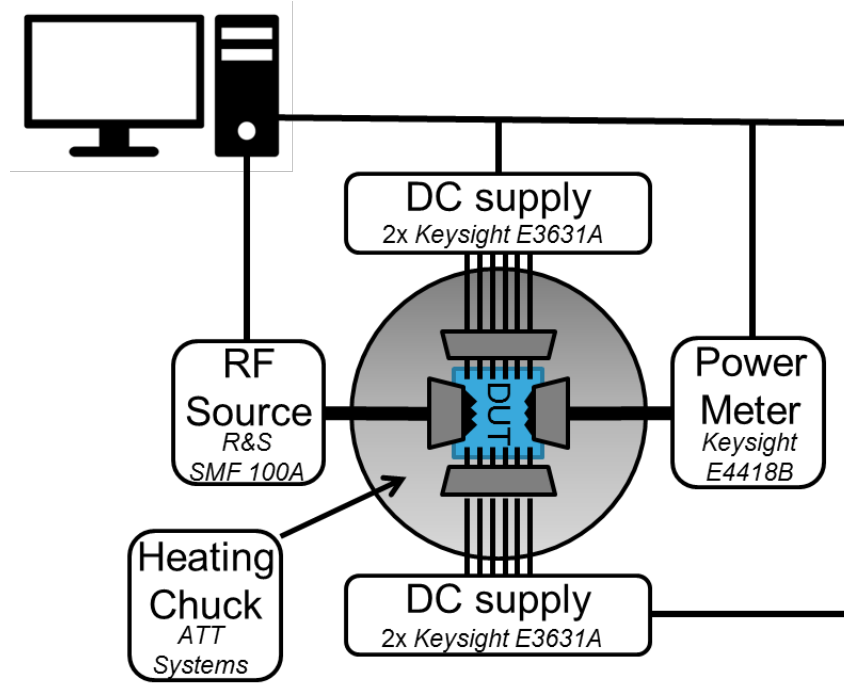


Figure III.6.3: Large-signal measurements test bench

III.7 Measurements at optimal operating point

In this work, the optimal operating point in measurements is obtained at 31GHz for a S2 supply voltage V_{DD_S2} of 1.98V, corresponding to the GO2 nominal voltage at maximum rating and made possible by the cascode architecture. S1 supply voltage V_{DD_S1} is set to 0.7V in order to enhance overall PA efficiency by limiting the power consumption. Gate bias values are 800mV, 422mV and 1.5V for V_{g_S1} , $V_{g_CS_S2}$ and $V_{g_CG_S2}$ respectively. The following results are corresponding to small-signal and large-signal measurements at this optimal operating point. In the following sections, the body biasing value V_{b_CS} is sweeping between 0V and 1.65V to illustrate the performances enhancement and the different effects enabled by the use of body-biasing node for PA reconfigurability purpose for both small-signal and large-signal measurements. This choice of operating conditions for supply, bias and body bias voltages ensures reliable and stable power amplifier behavior while maximizing reached performances and is summarized in Table III.7.1. In the following sections, if no different values are stated, the temperature of measurements is assumed to be 25°C.

	Voltage node name	Value (V)
S1 Stage	V_{DD_S1}	0.700
	V_{g_S1}	0.800
S2 Stage	V_{DD_S2}	1.98
	$V_{g_CS_S2}$	0.422
	$V_{g_CG_S2}$	1.5
	V_{b_CS}	0 to 1.65

Table III.7.1:Optimal operating point

As explained in the chapter introduction, the measurements are provided at 31GHz while the PA has been initially designed around 37GHz because of a mismatch between C_{neutro} and C_{GD} value during the manufacturing. The performances levels are thus achieved with passives which central frequency are around 37GHz. This is explored in Section III.11 with a comparison between retro-simulation and measurement. Oscillations have been observed for higher V_{b_CS} values at 35GHz due to this mismatch. However, the results depicted in the following sections are provided in totally stable conditions.

III.7.1 Small-signal measurements with body biasing tuning.

Small-signal analysis is performed for several values of V_{b_CS} between 0V and 1.65V from 20GHz to 40GHz. The graphs exhibiting plotted values of S_{11} , S_{22} , S_{21} and S_{12} are available in Figure III.7.1 (a), (b), (c) and (d) respectively. As it is noticeable on the S_{21} graph, the small-signal response in gain evolves with the body bias variation. When $V_{b_CS}=0V$, the maximum small-signal gain value is 21.9dB with a 3dB bandwidth BW_{-3dB} of 4.5GHz from 29GHz to 33.5GHz. The value of gain is incrementally improved to reach a maximum level of 32.6dB for $V_{b_CS}=1.65V$. A second gain peak is measured at 35GHz with higher V_{b_CS} values. It is residual from the high gain achievable for higher V_{b_CS} values that, with mismatched C_{neutro} and C_{GD} , is leading to oscillating conditions at driver stage. This is also corresponding to the S_{12} peak encountered at the same frequency. The gain achievable at this higher frequency allows BW_{-3dB} broadening and explains the achieved bandwidth. A maximum BW_{-3dB} of 6GHz, from 30GHz to 36GHz, is observed. These results demonstrate that the proposed power amplifier bandwidth covers the potential 5G band from 31.8GHz to 33.4GHz for all operating modes. Power amplifier S_{21} measured behavior illustrates that the body biasing allows dynamic gain level control over a >10dB wide range of values all over the targeted frequency bandwidth.

The S_{11} curve at nominal operation presents an attenuation pole at 32GHz and a lower one at 28GHz. These notches evolve with the body biasing and gradually shift the attenuation poles at 30GHz and 35GHz for $V_{b_CS}=1.65V$. For all modes S_{11} illustrates that the power amplifier is well matched at the input. S_{22} curve at nominal operation shows two attenuation poles at 31GHz and 33GHz. The curve is incrementally flattened with the V_{b_CS} improvement. This phenomenon is induced by the gain enhancement achieved through body biasing. Indeed, the output power for the same small-signal input power level is enhanced. Therefore, the output is matched in power for higher V_{b_CS} values, while at nominal operation with $V_{b_CS}=0V$ it is matched at small-signal. S_{22}

remains low enough to ensure good output matching and stable operations over all V_{b_CS} conditions.

Regarding the S_{12} , corresponding to the output-to-input isolation, the curves are very slightly affected by body biasing variations. The value remains under -35dB, demonstrating a good isolation under all body biasing conditions over all the measured frequencies. This great value of output-to-input isolation is reached thanks to the overall balanced topology, the S2 stage cascode design and the extensive use of cross-coupling C_{GD} capacitance neutralization in all stages.

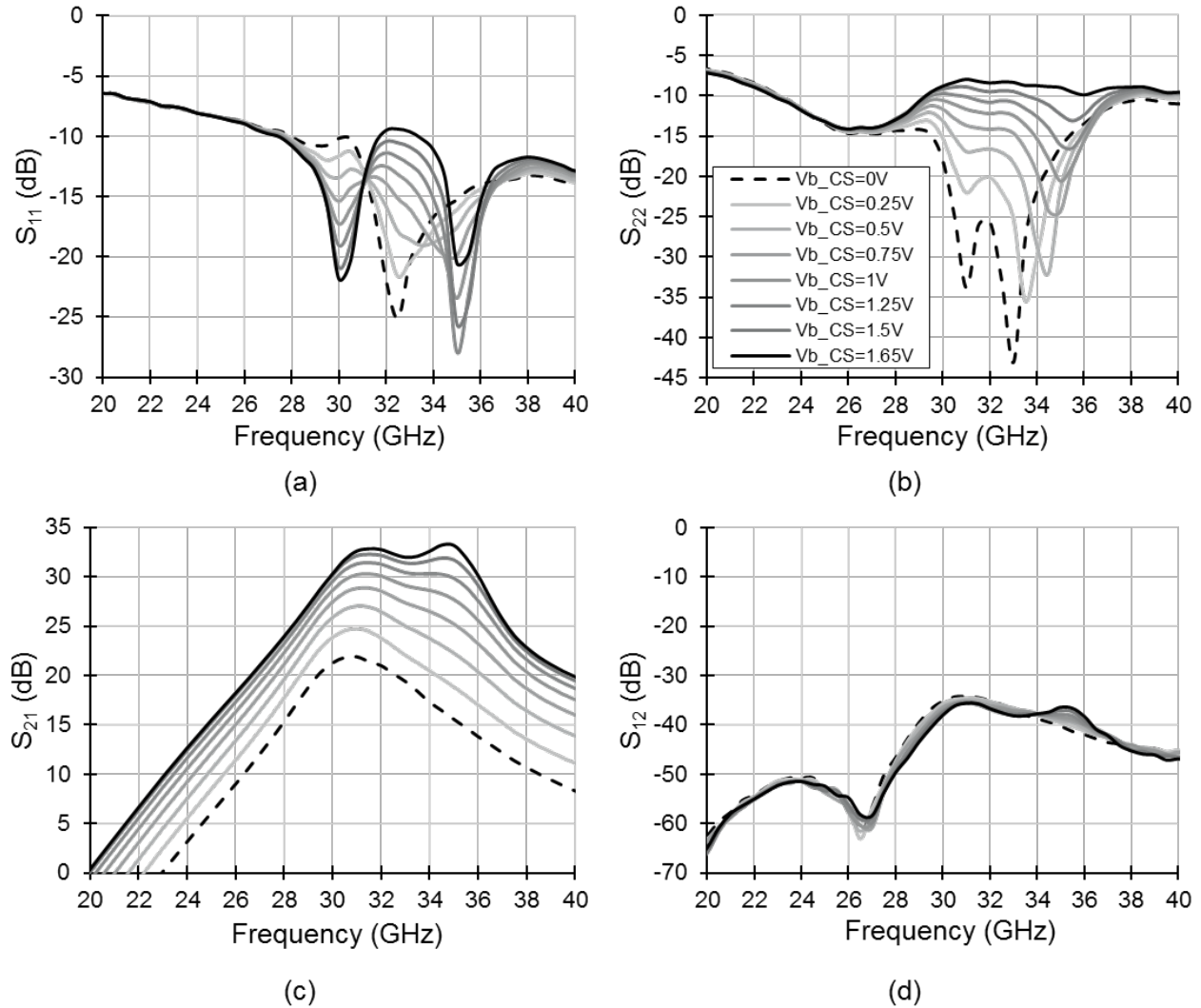


Figure III.7.1: Measured S-Parameters with body biasing continuous tuning

III.7.2 Large-signal measurements with body biasing tuning

Large-signal measurements have been performed using the test-bench presented Section III.6.2 with the same operating conditions than small-signal analysis. The power gain, PAE and power consumption results for a 31GHz frequency of operation are available in Figure III.7.2 (a), (b) and (c) respectively, with V_{b_CS} value varying from 0V to 1.65V.

The power gain graph confirms the wide gain span, from 21.9dB at $V_{b_CS}=0V$ to an extreme value of 32.6dB at $V_{b_CS}=1.65V$ with incremental levels. To the 21.9dB of power gain value is corresponding a P_{1dB} of 15.3dBm, obtained with a gain expansion of 0.9dB, typical to class-AB operation, allowing to push the 1dB output compression point P_{1dB} to higher output power level. To the 32.6dB gain curve, with typical class-A behavior, is corresponding a P_{1dB} value of 11.6dBm. Therefore, two extremes modes can be identified as it follows:

- A high-linearity mode when $V_{b_CS}=0V$.
- A high-gain mode when $V_{b_CS}=1.65V$.

A saturated output power of 17.3dBm is obtained in high-linearity mode and reaches 17.9dBm in high-gain mode. There is only a slight change in P_{sat} value regarding the operation mode. On the PAE curves, it is noticeable that for all values of V_{b_CS} , the peak efficiency is quasi-constant from 24.7% in high-linearity mode to 25.5% in high-gain mode. The PAE at 1dB output compression point, PAE_{1dB} , is reduced from 21% to 10% in high-linearity and high-gain modes respectively as P_{1dB} decreases with V_{b_CS} .

As explained in Chapter I, the PAE at back-off is an important parameter to take into account as it is in this condition that the PA likely has most chances to operate in advanced modulation schemes. The PAE at back-off is a challenging parameter to enhance for future transceivers. In this work, PAE at 6dB P_{sat} back-off is very slightly affected with only $\pm 1.7\%$ by V_{b_CS} variation and remains over 10% in all operating modes. This value is improved compared to other power amplifiers realized in the same technology at higher frequencies [LAR15]. The quasi-constant values of PAE_{max} and P_{sat} for all the body biasing conditions confirm the output load optimization strategy exposed in Section III.4.1.

As one challenging specification for future wireless network is to reduce the overall system power consumption and as we expose the fact that the power amplifier is the most power consuming block in the overall transmitter architecture, it is important to limit the power consumption of the power amplifier. Power consumption curves, for this work, are plotted in Figure III.7.2(c). It is noticeable that depending on the operating mode, the power consumption differs and justifies the performances difference. In high-linearity mode, the DC power consumption is 76.1mW while in high-gain mode the overall power consumption reaches 140.2mW. The power consumption at saturated output power is 229mW and 204mW for high-gain and high-linearity modes respectively. Indeed, it is possible to operate the power amplifier in high-linearity mode most of the time to lower the system power consumption and then to increase the gain level only when necessary to limit the overall average power consumption.

These large-signal measurements are highlighting that the body biasing tuning allows a fine grain wide range gain control. This permits to provide precisely any necessary gain level located in the achievable range for performances enhancement, contrary to classical gain control stages with fixed gain steps [SHA17]. This tuning node is also usable to compensate any manufacturing, environment or time induced performance drift in the context of robust adaptive systems. The body biasing voltage control also enables operating continuous class shifting, explained in Chapter II and measured in this section. This continuous class shifting is achieved with quasi no efficiency degradation thanks to the output impedance matching strategy and demonstrates the possibilities offered by the technology to implement efficient reconfigurable PA with no additional stage requirement.

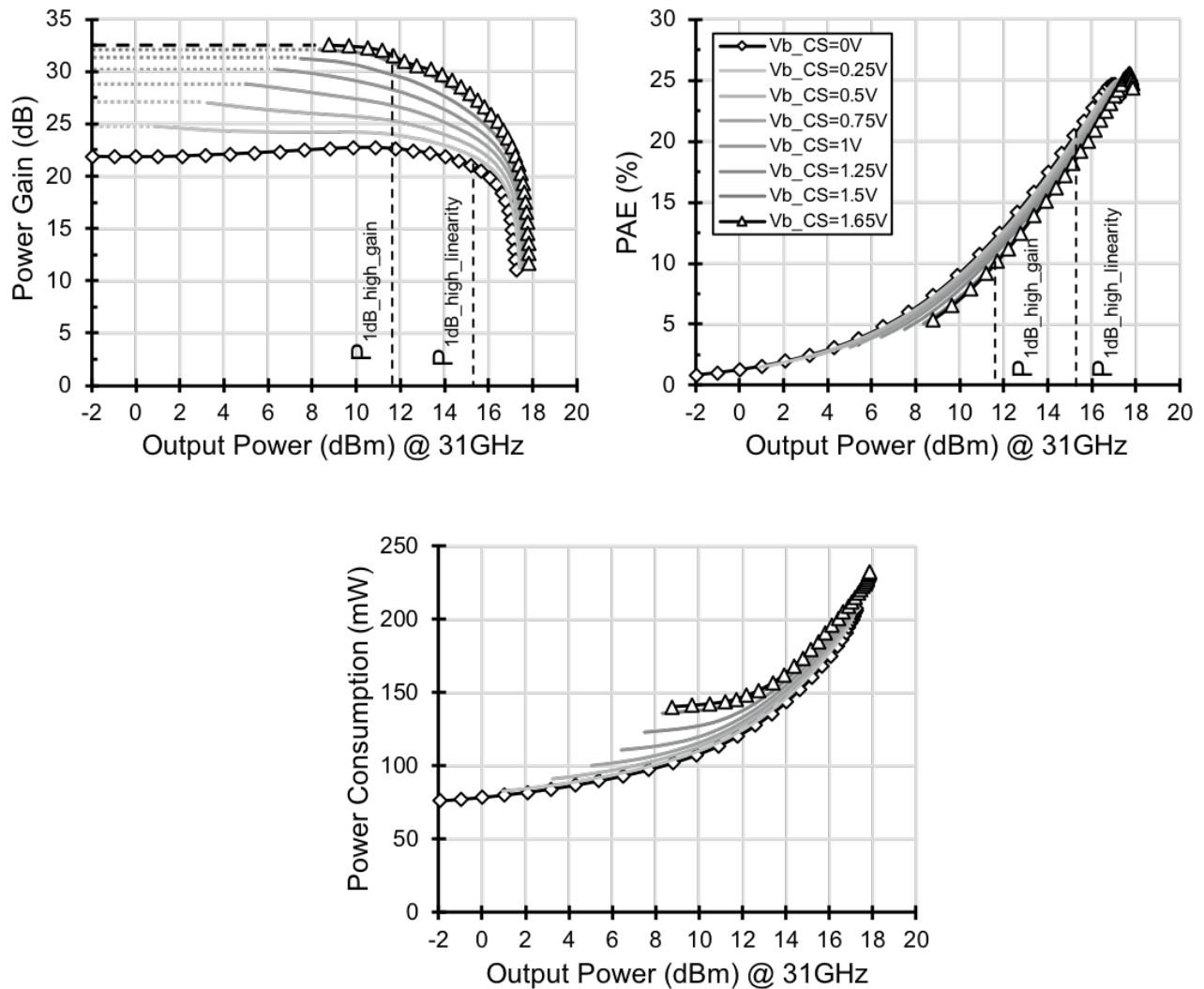


Figure III.7.2: Large-signal measurements: Gain (a), PAE (b) and Power consumption (c) with body biasing tuning variation from 0V to 1.65V

III.7.3 AM-PM measurements with body biasing tuning

Linearity is a key performance for future wireless systems as complex modulation schemes are leading to high PAPR levels. The P_{1dB} , corresponding to 1dB gain compression output power level is a parameter that describes linearity but an additional information regarding the phase is also necessary. For this purpose, it is possible to conduct AM-PM measurements. The AM-PM parameter is the output signal phase modification induced by an amplitude variation at the input of the power amplifier.

To measure this parameter, we performed large-signal S_{21} measurement with an input power sweep from -37dBm to 1dBm at 31GHz. For each input power point, the real and imaginary parts of S_{21} are measured. From these S_{21} measurements, it is possible to estimate the output power P_{out} using (III-12) to (III-15). The phase of S_{21} is calculated using (IV-4) and is then normalized.

$$P_{out}(dBm) = P_{in}(dBm) + Gain(dB) \quad (III-12)$$

$$Gain(dB) = 20 \log \left(\sqrt{Re(S_{21})^2 + Im(S_{21})^2} \right) \quad (III-13)$$

$$P_{out}(dBm) = P_{in}(dBm) + 20 \log \left(\sqrt{Re(S_{21})^2 + Im(S_{21})^2} \right) \quad (III-14)$$

$$Phase_{S_{21}}(^{\circ}) = \tan^{-1} \left(\frac{Im(S_{21})}{Re(S_{21})} \right) \times \frac{180}{\pi} \quad (III-15)$$

Finally, normalized S_{21} phase is plotted in function of P_{out} for several V_{b_CS} values from 0V to 1.65V like in previous sections. The AM-PM measurements results are available in Figure III.7.3.

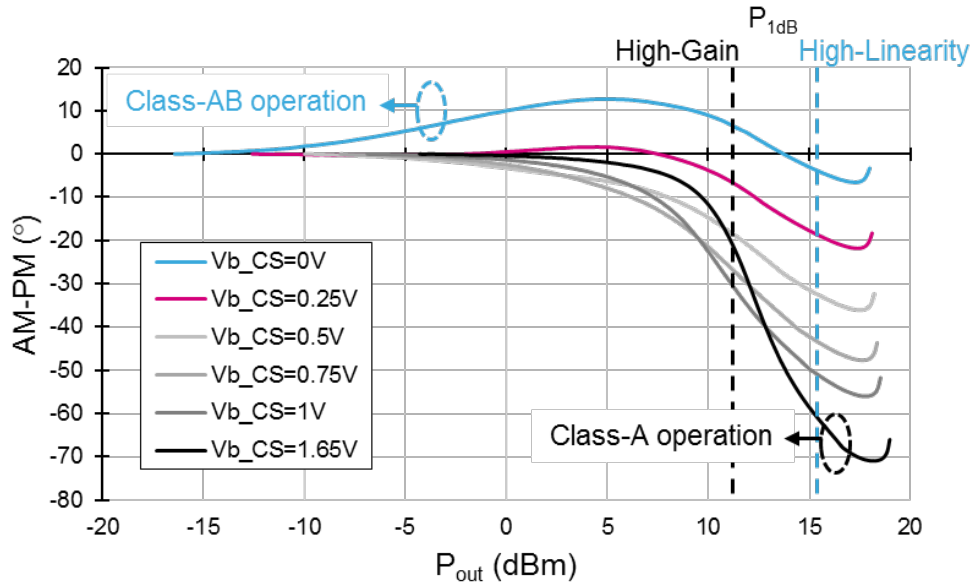


Figure III.7.3: AM-PM versus P_{out} measurements at 31GHz with body biasing tuning from 0V to 1.65V

Several remarks can be made regarding these results. The curve for $V_{b_CS}=0V$ is corresponding to typical class AB operation. Indeed, a phase expansion with a maximum of 12.7° deviation from normalized origin value is reached. This phase expansion is typical from gain expansion in class AB mode. The AM-PM value at P_{1dB} of 15.3dBm in this mode is 3.6° . The curve for $V_{b_CS}=1.65V$ shows typical class A operation. No phase variation occurs at low input power when the gain is flat and then the phase decrease when the output power approach P_{1dB} to finally present a high deviation during compression and up to saturation. In this mode, the AM-PM value at P_{1dB} of 11.6dBm is -21.6° . Intermediary modes are leading to intermediary AM-PM curves. $V_{b_CS}=0.25V$ curve is corresponding to class AB operation with a lower phase expansion of 1.6° , while V_{b_CS} from 0.5V to 1V curves shows class A type of operations. From these behaviors, it is noticeable that at high output power levels, from 11.2dBm to P_{sat} , the $V_{b_CS}=0V$ curve gives the lowest AM-PM variation. Then, in the output power interval from 4.5dBm to 11.2dBm, the curve corresponding to $V_{b_CS}=0.25V$ intermediary mode is leading to the lowest AM-PM variations compared to all other modes. Finally, under 4.5dBm output power level, both $V_{b_CS}=0.25V$ and 1.65V modes are leading to a very low phase variation depending on output power level.

Therefore, there is an optimal mode regarding phase linearity depending on the output power level. It is then possible to dynamically modulate the AM-PM value with the body biasing node voltage depending on the desired trade-off between gain, power consumption, output power level and linearity performances. This dynamic modulation could be done with an adaptive scheme implementation in the context of SoC. Linearization techniques like digital pre-distortion

could also be implemented in this context, linked to body bias and targeted performances levels to compensate the phase deviation dynamically.

III.7.4 Measurements over frequency range

As it is exposed in Section III.7.1, the gain BW_{-3dB} in high-linearity mode, corresponding to $V_{b_CS}=0V$, is covering the band from 29GHz to 33.5GHz. In high-gain mode, for $V_{b_CS}=1.65V$, it is covering the band from 30GHz to 36GHz. In this section we expose the large-signal measurements in both extreme modes at several frequencies from 28GHz to 35GHz. For this purpose, PAE_{max} and PAE_{-1dB} versus frequency are plotted in Figure III.7.4 (a) while P_{sat} and P_{1dB} versus frequency curves are presented in Figure III.7.4 (b).

It is noticeable in PAE_{max} curves that for both modes from 32GHz to 35GHz, there is no difference on the values, both curves are superimposed. This difference starts slightly at 31GHz and is higher for lower frequencies. At 28GHz, PAE_{max} is 18.7% and 22.6% at $V_{b_CS}=0V$ and $V_{b_CS}=1.65V$ respectively. This difference of PAE_{max} values can be explained by the fact that the output of the power amplifier is better matched at P_{in} corresponding to PAE_{max} value for $V_{b_CS}=1.65V$ at these frequencies. P_{sat} values are always higher for $V_{b_CS}=1.65V$ over all the measured frequency range and always above 15dBm for both modes. Maximum values are obtained at 31GHz and have been detailed in the previous section. A maximum difference of 1.4dBm between the two modes is obtained at 28GHz and can confirm the hypothesis of the non-optimal matching at 28GHz.

The 1dB output compression point curves are exhibiting several noticeable behaviors. First, P_{1dB} values are higher for $V_{b_CS}=0V$, for all frequency values for the same reason detailed in Section III.7.2 at 31GHz as P_{1dB} is reduced with V_{b_CS} tuning. Maximum value of 15.3dBm in high-linearity mode is obtained at 31GHz and 32GHz. Minimum values are obtained at 28GHz and 35GHz with 12.7dBm and 13.2dBm respectively. In high-gain mode, a maximum P_{1dB} level of 12.4dBm is reached at 30GHz while the lowest value is obtained at 35GHz with 7.5dBm. Then, we can remark that the P_{1dB} difference between both extreme modes is minimized at 30GHz with 1.9dBm of difference while at 35GHz this value is maximum with 5.7dBm.

On the PAE_{-1dB} versus frequency curves, it is noticeable that the values for $V_{b_CS}=0V$ are higher. This is naturally explained because of the higher level of P_{1dB} in this configuration, leading to higher corresponding efficiency value. Maximum values of 21% and 20.5% are reached at 31GHz and 32GHz respectively while minimum values of 14.5% and 13.5% are obtained at 28GHz and 35GHz respectively. For high-gain mode, a maximum of 15.5% is obtained at 30GHz while minimum value of 5.8% is obtained at 35GHz. These two curves exhibit the same variations than P_{1dB} curves depicted previously.

These frequency measurements for the same operating conditions confirm the PA operation and performances suitable for 5G applications on the 31.8GHz-to-33.4GHz 5G band. The large-signal measurements over frequency shows that at 35GHz second gain peak identified during S_{21} measurements for $V_{b_CS}=1.65V$, the achieved linearity and efficiency levels are low

compared to the targeted values. No further measurements have been conducted at this frequency.

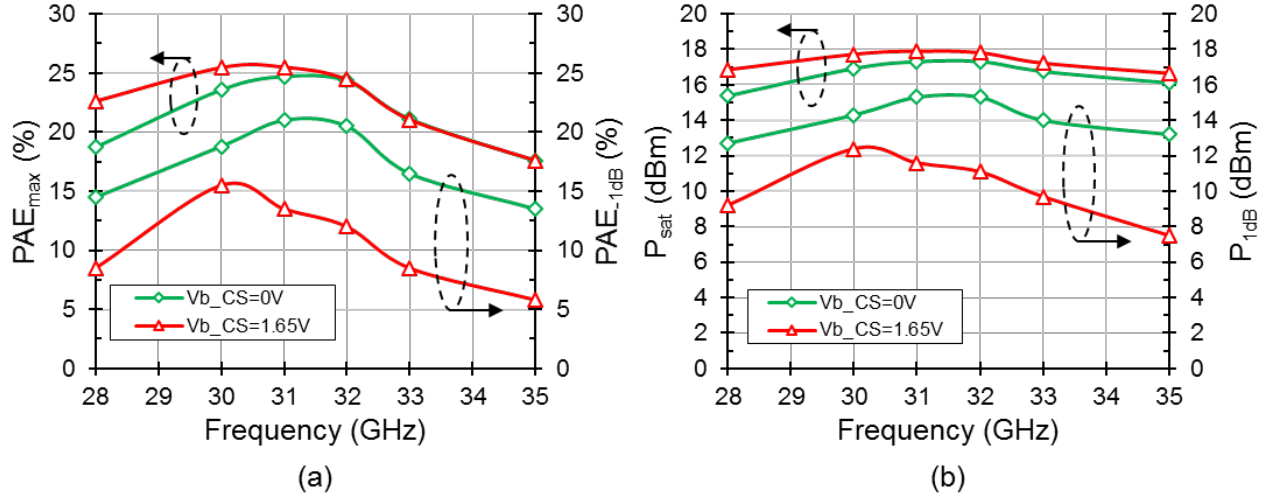


Figure III.7.4: Large-signal measurements: PAE_{max}/PAE_{1dB} (a) and P_{sat}/P_{1dB} (b) in extreme modes from 28GHz to 35GHz

III.8 Power Amplifier behavior for temperature variations

31GHz Small-signal and large-signal measurements have been performed for a temperature of operation from 25°C to 125°C, in order to evaluate the design robustness to temperature variations. These measurements are made under the same operating conditions than previously and using corresponding bench described in Section III.6 and we check carefully that the temperature is stabilized between two measurements.

III.8.1 Large-signal measurements from 25°C to 125°C with body biasing tuning

In these measurements, we report the values of the power gain, P_{sat}, PAE_{max} and P_{DC} for V_{b_CS} varying from 0 to 1.65V at temperatures comprised between 25°C and 125°C. Results are reported in Figure III.8.1.

First, we focus on P_{sat} and PAE_{max}. The effect of temperature over P_{sat} is an incremental reduction with a maximum total decrease of 1.2dBm (-0.3dB per 25°C levels) for all modes. The temperature impact on P_{sat} level for all modes is limited and the saturated output power always remains over 16dBm. The same behavior is noticeable over peak efficiency. PAE_{max} levels are decreasing when the temperature is improved. The maximum efficiency decrease is 3.3% and 4.6% in high-linearity and high-gain modes respectively. Even at 125°C, the PAE_{max} value is over 20%. We can hence conclude that temperature has a slight influence over output power and efficiency.

The power gain response is different than the two previous parameters. In fact, at V_{b_CS}=0V, the tendency is a gain improvement with temperature. From V_{b_CS}=0.4V, the trend is

reversing and the gain is decreased with the temperature. The gain dynamic range between high-linearity and high-gain mode is then reduced with the temperature. However, fine grain gain control is available at all temperature of operation and performed gain levels are still high.

Finally, P_{DC} levels depending on temperature and body biasing have been measured. It is remarkable that the P_{DC} level is minimum at ambient temperature. The highest the temperature and the V_{b_CS} are, the highest the P_{DC} levels are. In high-linearity mode, the result is a P_{DC} increase of 8.2mW while a 9.4mW maximum augmentation is achieved in high-gain mode.

It is noticeable that at 125°C, several changes compared to the general behavior tendencies are observed. This can be explained by the measurements conditions. Indeed, the temperature induced chip dilatation made the RF and DC probe contact less efficient.

The measured performances modifications induced by the temperature improvement can be explained by its physical impact over the chip. Two distinct effects are occurring.

When the temperature is improved, the internal transistor parameters are modified. This affects the V_T that is decreasing with the temperature. This induced V_T reduction is leading to a higher drain current level for a fixed V_{DS} , in the same way that it can be done with body-biasing at ambient temperature. Therefore, it induces the higher power consumption related. This V_T variation affects both stages and does not have the same impact over performances for all V_{b_CS} values. In fact, for $V_{b_CS}=0V$, the V_T variation induces higher gain as the operating class is drifting from class AB to class A. For $V_{b_CS}=1.65V$, the PA is already in class A. Therefore, the V_T shift is operating a drift from class A to over class A, in a mode of operation where the power consumption is higher for reduced gain performances.

Concerning P_{sat} variations, they are linked to the PA routing and that is why the same behavior in function of temperature is observed for all V_{b_CS} values. Indeed, the copper resistivity is improving with the temperature. Therefore, the drain access resistance (balun parasitic resistance) of the power stage is improved. This reduces the total V_{DS} value of this stage for fixed current conditions. Therefore, the saturated output power is reduced.

These large-signal measurements illustrate that a 100°C operation temperature augmentation leads to output power and efficiency levels reduction, while power consumption is improved, for all modes. The gain dynamic between the two extreme modes is also reduced. Nevertheless, these variations are limited and are not critical. Furthermore, the level of performances reached at 125°C is still high. Another noticeable point is the fact that the power amplifier is not degraded with temperature. It has been observed during the measurements process that after 125°C measurements, if the temperature is then set to 25°C, no drift over performances is observed compared to classical 25°C operation for both extremes modes, demonstrating the design and technology robustness over temperature variations during measurements.

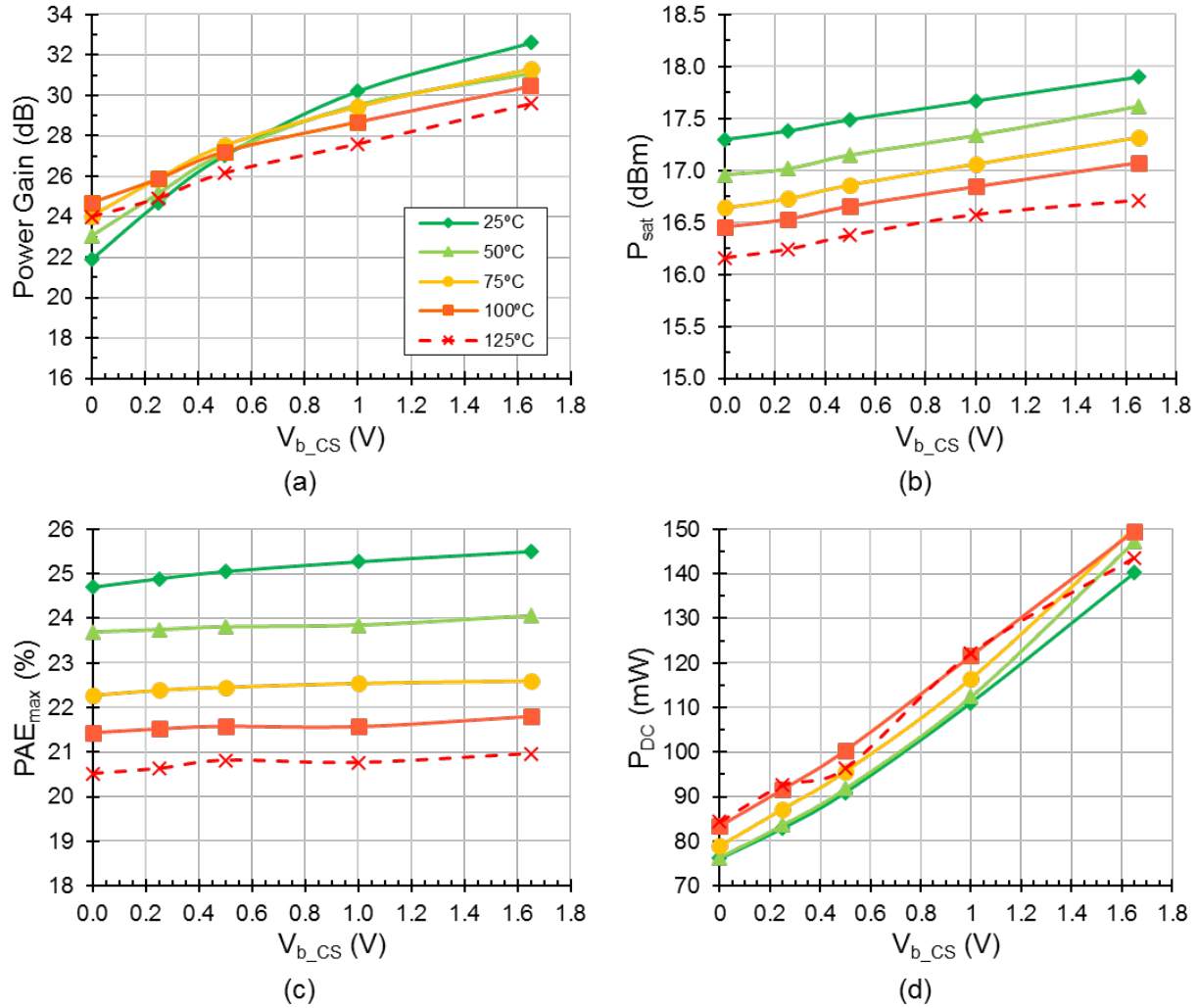


Figure III.8.1: Large-Signal measurements at 31GHz from 25°C to 125°C
with V_{b_CS} tuning from 0V to 1.65V

III.8.2 Small-signal measurements from 25°C to 125°C

Small-signal analysis for several temperature conditions has also been carried out in order to determine the induced impact over S-parameters.

S-parameters curves in high-linearity mode and high-gain mode are exhibited in Figure III.8.2 and Figure III.8.3 respectively. Each curve corresponding to a different temperature value from 25°C to 125°C. In all temperature conditions, input and output stay well matched over the frequency range of interest in all modes. Both S_{11} and S_{22} temperature behaviors can be compared to S_{11} and S_{22} variations caused by body-bias tuning. It confirms the temperature induced V_T variation behavior as explained in the previous section.

The S_{21} curves confirm this behavior and the values obtained in the previous section. As expected, higher power gain level and slightly improved BW_{-3dB} are obtained with higher

temperature levels for $V_{b_CS}=0V$ while the inverse tendency occurs for $V_{b_CS}=1.65V$. S_{12} curve illustrates that the isolation is not impacted by temperature variations and remains higher than 35dB under all temperature conditions. This is conferred by the balanced topology that provides a robust high reverse isolation.

Large-signal and small-signal temperature performances analysis have been performed. They show that the temperature impact over intrinsic transistor parameters and chip routing causes only slight output power, efficiency and gain tuning range degradation. Satisfying matching, isolation and stability conditions are achieved for a 100°C temperature span. The fine grain gain control is still achievable over all temperature conditions. We can hence conclude that the proposed power amplifier design presents robustness to industrial temperature range with good performance levels achieved at 125°C.

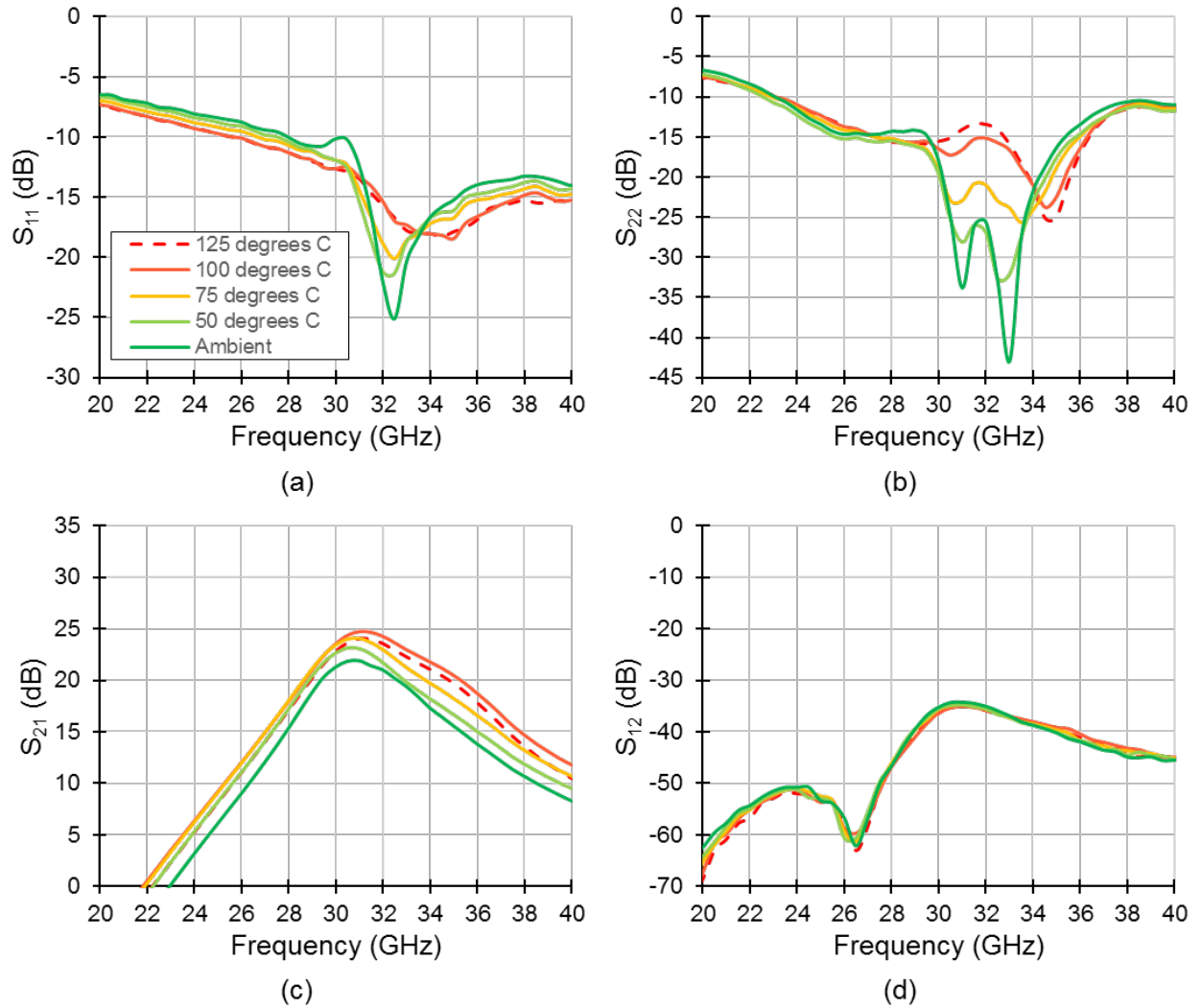


Figure III.8.2: Small-Signal measurements from 25°C to 125°C in high-linearity mode

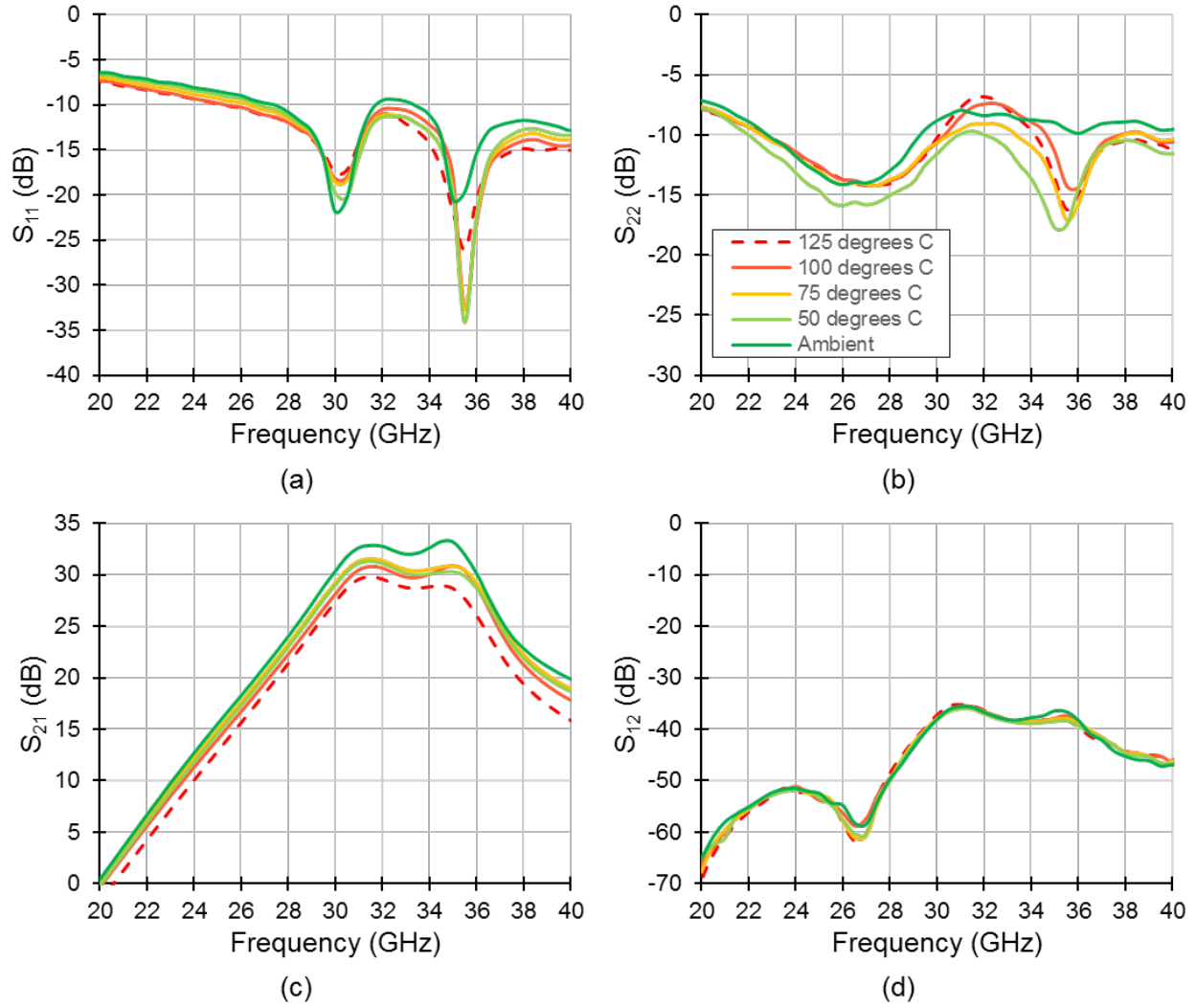


Figure III.8.3: Small-Signal measurements from 25°C to 125°C in high-gain mode

III.9 On-wafer variability statistical study

During the power amplifier design, efforts have been made in order to reduce the impact of process induced on-wafer variability. In order to estimate these variations regarding individual circuit's performances, a serial of large-signal measurements have been conducted. For this purpose, 13 on-wafer occurrences of the same circuit at different locations on one wafer have been measured under the same conditions for both high-gain and high-linearity modes. The same conditions as in the previous analysis have been used at ambient temperature. The values of peak efficiency, saturated output power and power gain have been measured for each circuit. Therefore, average and standard deviation values have been calculated for each parameter in both operating modes. Results of this study are reported in Figure III.9.1, featuring PAE_{max} , P_{sat} and power gain values range versus corresponding number of occurrences leading to these values. Corresponding average and standard deviation values are also calculated and reported.

First, let's focus on high-linearity mode. A PAE_{max} average value of 24.99% with a very low corresponding standard deviation of 0.28% is reported. Concerning power gain, an average value of 21.77dB and a standard deviation of 0.62dB has been measured. In addition, a very slight standard deviation is achieved over P_{sat} with 0.08dBm for an average value of 17.46dBm.

For the high-gain mode, a PAE_{max} average value of 24.92% and a low standard deviation of 0.35% are measured. Regarding the power gain, average power gain level of 31.94dB with a standard deviation of 0.45dB is calculated. Finally, an average P_{sat} value of 17.9dBm with a very slight standard deviation of 0.07dBm is reported.

The calculated standard deviation from measurements over 13 different on-wafer locations is very low for P_{sat} and is under 0.1dBm in both high-linearity and high-gain extreme modes. Similarly, a very low peak efficiency standard deviation under 0.5% for both modes is observed. The highest reported standard deviation is for power gain value and is under 1dB in all V_{b_CS} conditions from 0V to 1.65V.

These relatively low variations between measured performances over several chips are achieved thanks to the choices made early in the design process in order to reduce the process variability risks. Indeed, as generally the process variations are occurring over active devices arrays, the choice of dummies transistors integration around the useful transistors reduces this risk as they are more likely to be impacted because of their placement at the edge of the active devices array. The choice of a non-minimal gate length of 60nm and the subdivision of large total width transistors in elementary transistor cells reduce the chance of a process induced gate length drift in each transistor. Furthermore, the wide RF path routing reduces the impact of a small metal layers width difference that can happen during manufacturing.

It has been observed during the measurement process that the gain value variation can come to on-wafer mmW probe placement on RF pads that can slightly differ from one measurement to another, the power gain is the most sensitive parameter observed for this effect. Nevertheless, all standard deviations obtained are low, even for the power gain. These results reflect the robustness of the design and 28nm FD-SOI technology to process spread and

consolidate the choices made during the design to reduce local process variations, like the dummies transistors insertion aside each useful transistor stage.

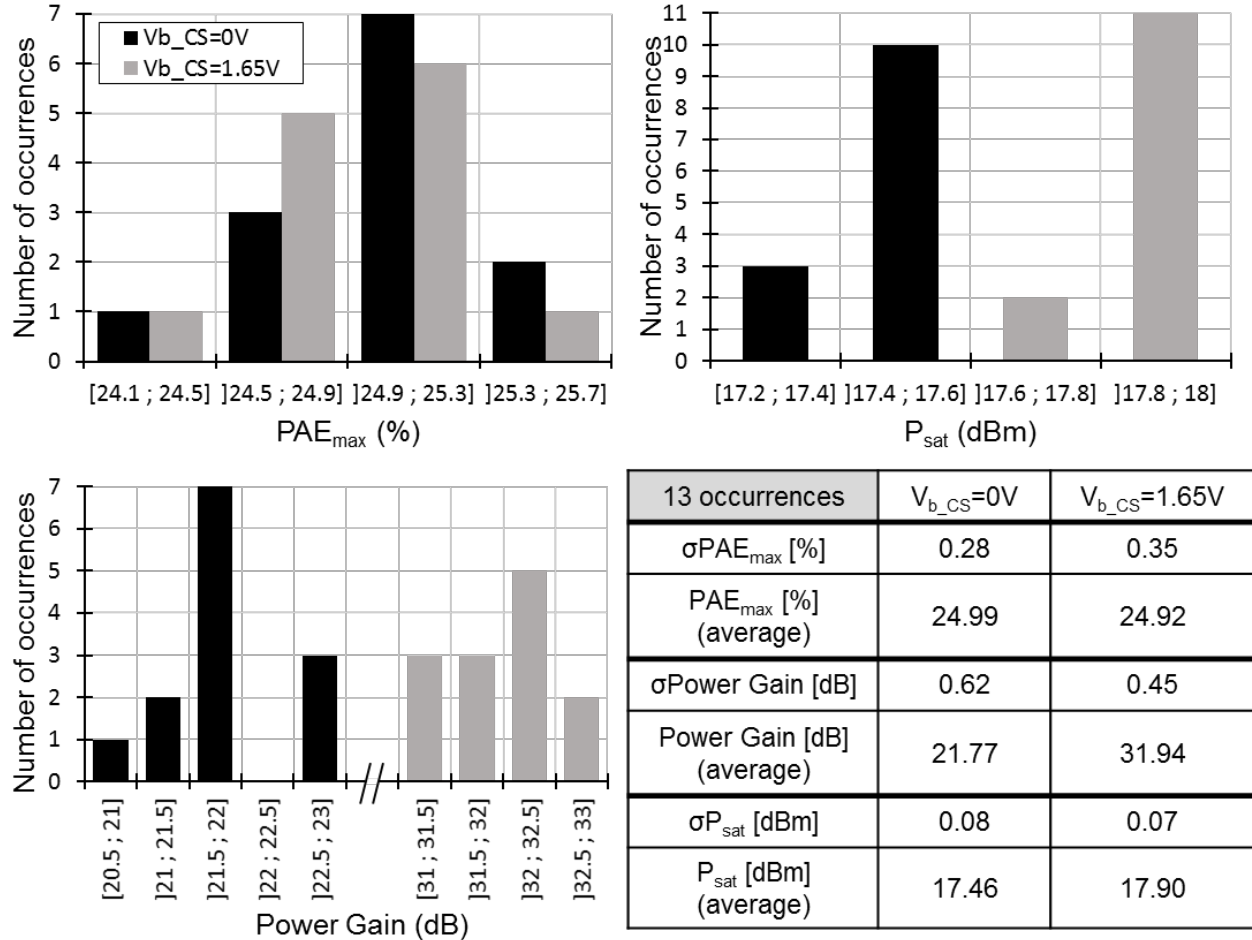


Figure III.9.1: Statistical PAE_{max} , power gain and P_{sat} measurements over 13 on-wafer occurrences at 31GHz. Identical bias and supply conditions.

III.10 Comparison and discussion regarding mmW PA state of the art

This section now compares the measured performances of the power amplifier proposed in this work with the state of the art. In Chapter I, we developed the future wireless networks requirements regarding power amplifiers. For this purpose, it has been discussed that high efficiency, reduced power consumption and good linearity are needed while frequency and/or mode reconfigurability is interesting for SoC implementation. Furthermore, good linear performances concerning power levels and gain are necessary. We first provide a state of the art overview.

[WAN15] presents a 10GHz-25GHz dual band power amplifier exhibiting a single-ended 2-stages cascode in 180nm CMOS technology. Low performances are reached in terms of output power, efficiency and gain levels. High-power consumption is caused by the higher supply voltage of the 2-stages cascode topology. It illustrates the difficulty to achieve satisfying performances over several bands and the need for advanced technology nodes for efficient and performant power amplifier implementation.

Two 29GHz power amplifiers are presented in [JAY16] and exhibit high output power and efficiency levels. However, the high supply voltage requested by the single-ended stacked multi-gate topology that permits to achieve these performances is leading to a prohibitive levels of power consumption which is not desirable in an energy saving context for future wireless networks.

A solution for 30GHz highly efficient and low power consumption power amplifier targeting 5G is presented in [SHA16]. However, the use of common-source topology ensuring the low power consumption limits the achievable output power and gain levels.

The limit of common-source topology for high output power is also illustrated in [PAR16]. In fact, two differential power amplifiers are proposed in this reference. One is exhibiting a common-source topology while the other is featuring cascode configuration. The use of transistor stacking allows to double the supply voltage level and enhance output power, gain and efficiency levels compared to the common-source. The single-stage topology limits the number of passive devices for matching and differential-to-single conversion and so the induced impact over efficiency. Both circuits are featuring a 2nd harmonic control that is enabling efficient and linear operations. However, low gain values are achieved in both PAs, due to the single-stage topology.

Furthermore, none of these power amplifier is featuring reconfigurability while it has been demonstrated in [LAR15] that high performances and power gain control are achievable at 60GHz. In fact, the realized power combining allows high output power level while the segmented biasing of the common-source transistors is leading to high linearity operations. This circuit is implemented in 28nm FD-SOI and uses the back-gate for both segmented-biasing and gain reconfigurability.

In the state of the art at that time, there were a lack of power amplifiers featuring efficiency and good performances regarding gain, output power, power consumption and

reconfigurability for frequency bands around 30GHz to leverage future wireless networks implementation. This is in this context that the presented work emerged to address these remaining challenges targeting SoC implementation. Furthermore, as we developed in previous chapters, an implementation in phased array systems is subject to environment variations that can lead to performances degradation. None of the power amplifiers available in the state of the art presents a solution to overcome this issue.

The reference [HU17] addresses the multi-band challenge. It is featuring a transformer-based Doherty topology implemented in 130nm SiGe technology. This multi-band operation is leveraged by the use of wideband passive devices and varactor loaded transmission lines at the input of both main and auxiliary paths to dynamically select the desired band of operation and covers several potential 5G bands. However, while good output power levels are achieved, the limited efficiency and gain levels illustrate that high performances are still difficult to obtain over all bands.

Another wideband power amplifier has been proposed in [ALI17]. In this reference, the continuous class F operation enabled by a tuned network and the limitation to a single-stage topology allows high efficiency performances over a wide frequency range of operation. However, this topology is leading to low output power and gain levels, illustrating that efficiency and high performances are hard to obtain simultaneously with wideband operations.

As stated previously, reconfigurability in mode is an interesting alternative solution for SoC implementation. The reference [SHA17] presents an evolution of the power amplifier referenced in [SHA16] and shares the same 2-stage differential common-source topology, implemented in 40nm CMOS technology. Digital variable gain control with 9dB dynamic range has been implemented and makes this reference the only gain power amplifier with reconfigurable gain, with our work, of the 30GHz state of the art. Excepted this ability, the power amplifier presented in [SHA17] presents the same advantages and drawbacks than [SHA16]: high efficiency, low power consumption but limited output power.

The performance trade-off between output power, gain, efficiency and power consumption is also illustrated by [IND17]. The Doherty configuration allows high power levels thanks to power combining. Good power gain and linearity levels are measured while a limited peak efficiency is achieved. Furthermore, this topology is leading to high power consumption, even if the supply voltage is limited to 1V.

While these references try to address the state of the art challenges concerning efficiency and performances enhancement and/or reconfigurability, none of these addresses the issue of environment variation for phased array implementation. This is the topic of the work presented in [MOR17]. This reference exhibits a balanced topology in 28nm FD-SOI CMOS technology, providing robustness to input and output impedance variations. The robustness is explored in order to move the biasing limits forward the actual security margins in case of VSWR to enhance global power amplifier performances. While good levels of output power and power consumption are achieved, a limited gain is measured. Furthermore, the efficiency levels are limited by the losses encountered in the passive devices on the RF path.

The reference [CAL17] presents a power amplifier implemented in 14nm FinFET technology node. This amplifier has been designed for higher 5G frequency bands around 70GHz. Two modes corresponding to different operating conditions are presented. The “normal mode” provides low power gain at 66GHz while a “high-gain mode” provides a higher but still limited power gain value. Furthermore, despite the use of design techniques such as capacitive neutralization, low efficiency, linearity and output power levels are achieved in both modes. These performances do not the 5G requirements and illustrate that further research is needed in this technology node to implement a power amplifier targeting SoC implementation for future wireless networks.

Now that we have defined the state of the art, it is necessary to compare the measured performances. For this purpose, for each circuit of the state of the art, several parameters including power gain, P_{sat} , P_{1dB} , PAE_{max} , $PAE_{@6dB}$, P_{sat} Back-off, BW_{-3dB} and P_{DC} are reported or estimated from the available data in the literature when stated. The number of stages, the technology and their area footprint are also reported. Furthermore, to compare circuits one to another, figures of merit FOM are commonly used in the literature. For power amplifiers comparisons, the ITRS FOM, for *International Technology Roadmap for Semiconductors*, is generally used. This figure of merit can be calculated using the equation (III-16) where power gain is expressed in linear form and P_{sat} is expressed in Watt. All these values for selected circuits are provided in Table III.10.1.

$$ITRS\ FOM = P_{sat}(W) \times Gain(lin) \times freq(GHz)^2 \times PAE_{max}(\%) \quad (III-16)$$

	Our Work		[RAB18] ^{\$}	[HU17]	[SHA17]	[IND17]	[ALI17]	[JAY16]	[SHA16]	[PAR16]	[WAN15]	[MOR17]	[LAR15]	[CAL17]
Technology	28nm UTBB FD-SOI CMOS		ISSCC'18 130nm SiGe	ISSCC '17 130nm SiGe	ISSCC '17 40nm CMOS	RFIC '17 28nm CMOS Bulk	RFIC '17 65nm CMOS	JSSC '16 45nm SOI CMOS	ISSCC '16 28nm CMOS Bulk	IMS '16 28nm CMOS	EL '15 180nm CMOS	LASCAS '17 28nm FD-SOI CMOS	ISSCC '15 28nm FD-SOI CMOS	RFIC '17 14nm FinFET CMOS
Number of Stages	2		1	2	3	2	1	1	2	1	2	2	3	3
Operating Mode	High Lin.	High Gain	-	28GHz Band	Max. Gain	-	-	-	-	-	-	-	High Lin.	"High Gain"
Supply Voltage [V]	0.7/1.98 ^{''}	0.7/1.98 ^{''}	4	1.5	1.1	1	1.1	5.2	1.15	1.1	3	2	1	1
Frequency [GHz]	31	31	28	28	27	32	29	29	30	28	25	28	60	66
Power Gain [dB]	21.9	32.6	14 [*]	18.2	22.4	22	10	14 [*]	16.3	10	6.8	17.5	15.4	8.3
P _{sat} [dBm]	17.3	17.9	23	16.8	15.1	19.8	14.8	23.7	15.3	14.8	10	18.4	18.8	7.4
P _{1dB} [dBm]	15.3	11.6	20 [*]	15.2	13.7	16	13.2	20	14.3	14	9	15.4	18.2	5.5
PAE _{max} [%]	24.7	25.5	41.4	20.3	33.7	21	46.4	29	36.6	36.5	4.8	12.4	21	8.6
PAE _{1dB} [%]	21	10	40 [*]	19.5	27.5 [*]	12 [*]	22 [*]	18 [*]	35.8	35.2	4 [*]	9.5 [*]	21	9
PAE _{6dB P_{sat} Backoff} [%]	11.5	10.4	34.7	14 [*]	15 [*]	8 [*]	-	11 [*]	-	24 [*]	2 [*]	6 [*]	8 [*]	4.2
BW _{3dB} [GHz]	4.5 (14%)	6 (18%)	-	16.4 (52%)	7 (24%)	6 (18%)	8 (26%)	11 (38%)	4 (13%)	-	4 [*] (16%)	4 [*] (14%)	10 (17%)	8.5 (12%)
P _{DC} [mW]	76.1	140.2	50 [*]	71 [*]	30.3	250 [*]	57 [*]	448 [*]	20.1	-	150	154	74	-
Active Area [mm ²]	0.508		0.56 ^{**}	1.76 ^{**}	0.23	0.59	0.12	0.24	0.16	0.28	0.864 ^{'''}	0.66	0.162	0.26
ITRS FOM [W/GHz ²]	1,932	26,925	1,626	503	1,381	3,255	117	1,436	476	86	1.5	405	1,988	16
														115

^{\$}Reference added after PhD defense. Not discussed in the following paragraphs.
[#]Stage 1 (S1) supply, ^{''}Stage 2 (S2) supply. ^{*}Estimated from reported figures, ^{**}With Pads.

Table III.10.1: mmW PA state of the art comparison table

In order to compare the designed circuit measurements with the state of the art, it is possible to find in Figure III.10.1 to Figure III.10.4 the reported power gain, PAE_{max} , P_{DC} and ITRS FOM respectively versus P_{sat} of each circuit referenced around 30GHz in Table III.10.1. The references are sorted by technology type and nodes in the Figure III.10.1 to Figure III.10.4, following the classification detailed in Table III.10.2.

Technology	○				△		×
	CMOS				CMOS SOI		SiGe
Node	●	●	●	●	▲	▲	✖
	28nm	40nm	65nm	180nm	28nm FD-SOI	45nm	130nm

Table III.10.2: Technology classification used in Figures IV-14 to IV-17

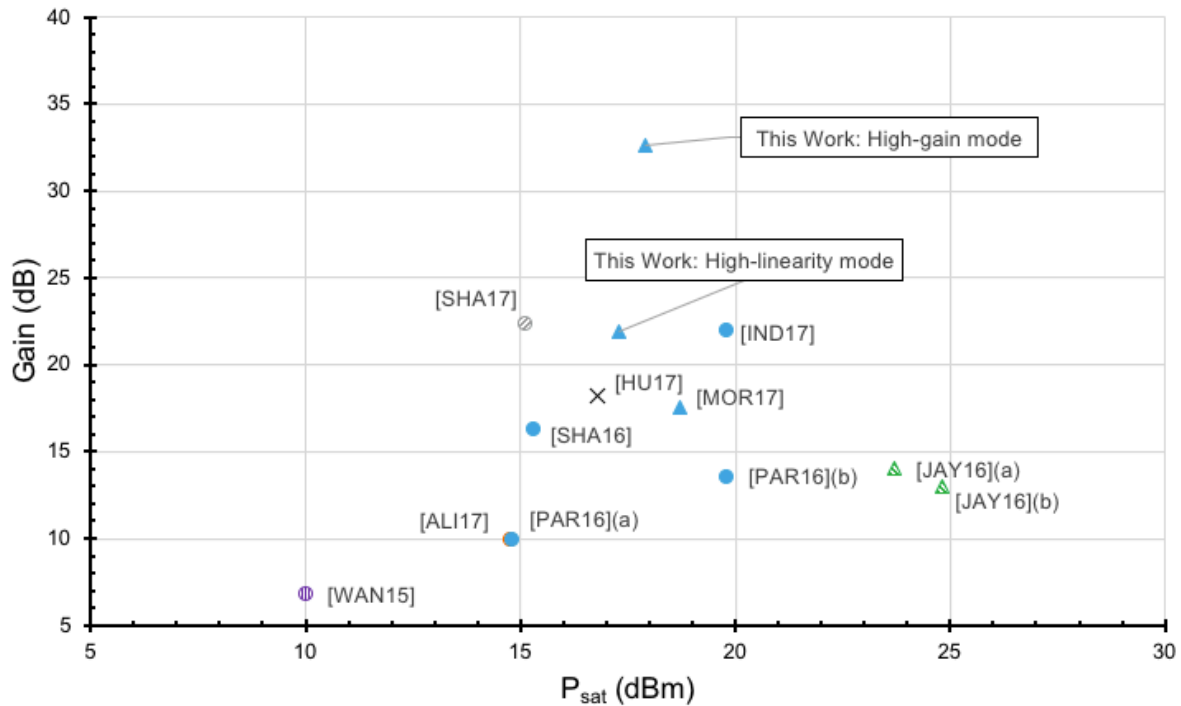


Figure III.10.1: State of the art comparison: power gain level versus P_{sat}

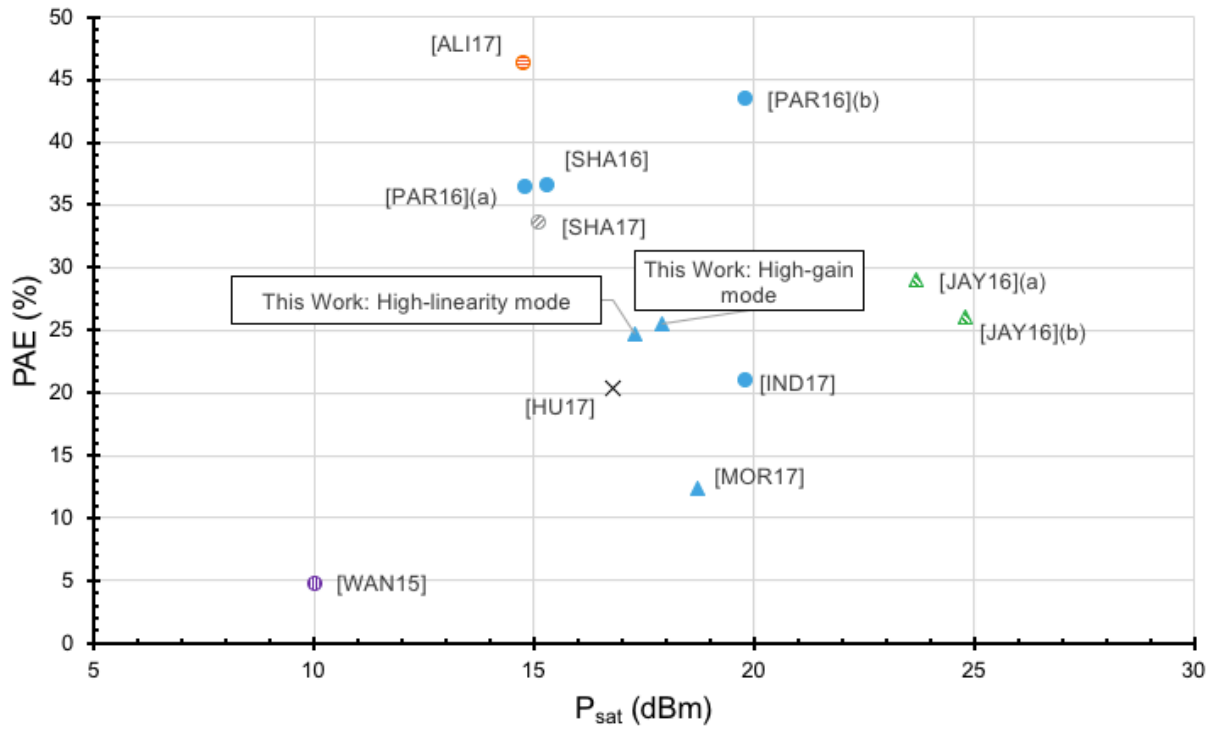


Figure III.10.2: State of the art comparison: PAE versus P_{sat}

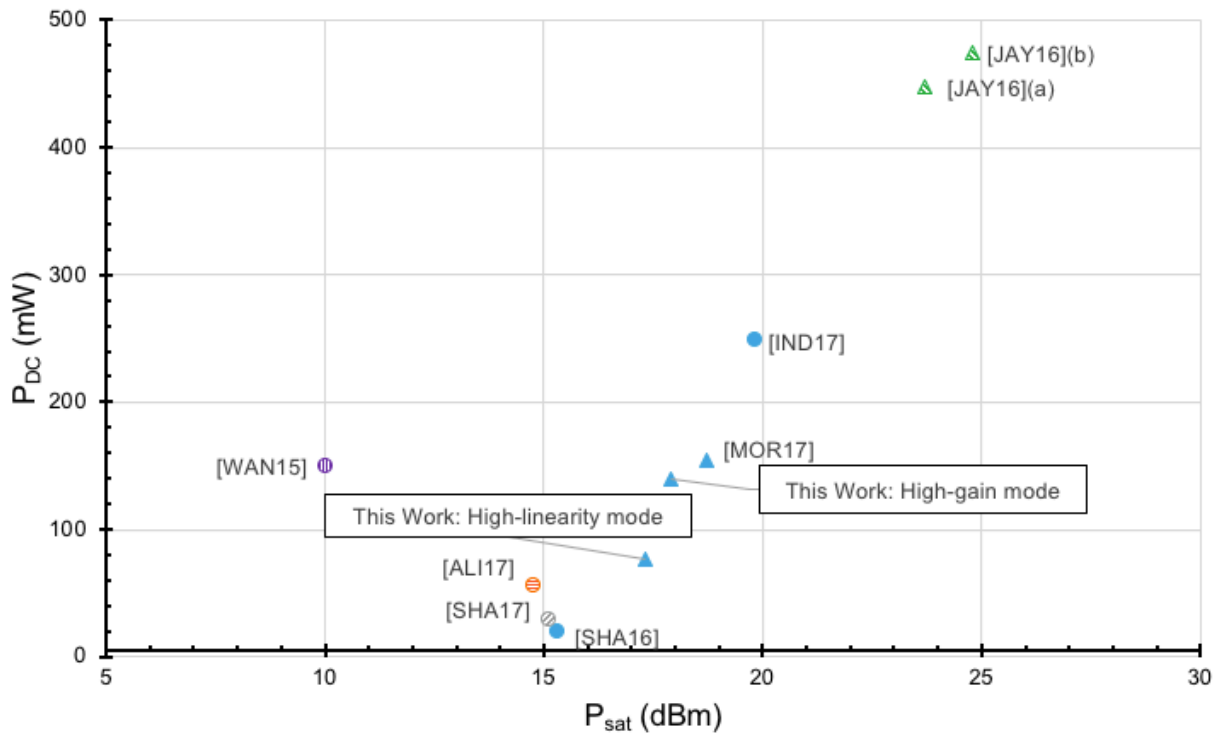


Figure III.10.3: State of the art comparison: P_{DC} versus P_{sat}

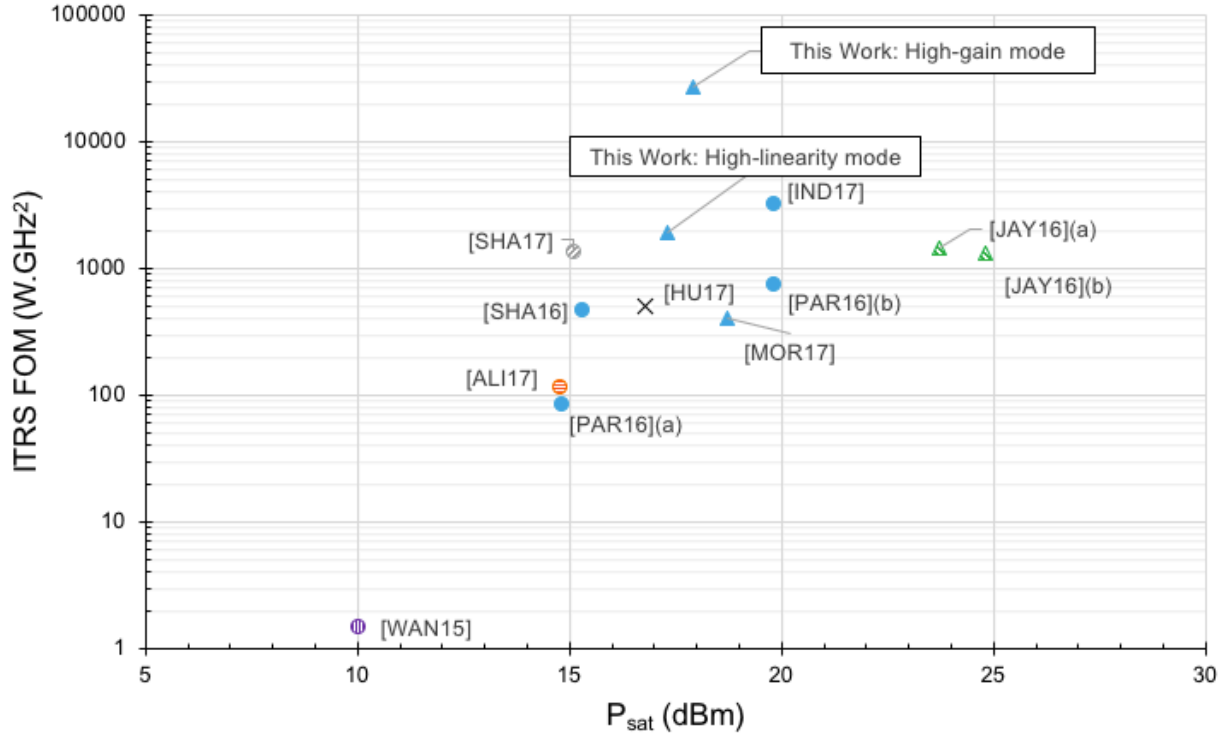


Figure III.10.4: State of the art comparison: ITRS FOM versus P_{sat}

Several remarks can be done about performance levels, targeted application and the state of the art. This is discussed in the following paragraphs.

We exposed previously the necessity of highly efficient, low consumption, linear power amplifiers to fulfill 5G applications requirements. For beamforming phased array, as multiple amplification path will be implemented at the same base-station for FD-MIMO, the output power will be distributed. Therefore, high P_{sat} performance for each amplification path is not mandatory, while high gain is expected.

The performances achieved by our designed power amplifier meets these needs. Indeed, we present a sufficient P_{sat} around 17.5dBm due to the limited achieved power consumption in all operating modes with a maximum of 140mW. High gain is achieved in high-linearity mode while the high-gain mode shows the highest reported gain value of the state of the art around 30GHz, 10dB higher than [SHA17] that is the second highest reported gain value in this frequency range. Concerning linearity, good performances regarding P1dB are achieved in high-linearity mode, with 2dBm between 1dB compression point and saturation.

Compared to previous design [LAR15] implemented in 28nm FD-SOI, the main performance improvement is higher efficiency levels in all modes and the fact that no efficiency degradation is occurring. Furthermore, the balanced topology confers additional robustness to external conditions variations. Compared to [MOR17] featuring balanced topology in the same technology, the efficiency is enhanced while additional body-biasing based gain reconfigurability is demonstrated. Higher gain is also achieved in all modes.

In the state of the art, several tendencies concerning performances can be identified. Most PAs achieving high output power levels present a limited gain [JAY16](a), [JAY16](b), [PAR16](b). They also suffer from high power consumption in order to achieve this high output power even if efficiency levels are good. The circuits with a high PAE generally suffer from low P_{sat} levels, linked with the low power consumption that they achieve [ALI17], [PAR16](a), [SHA17]. It is also noticeable that the performances reported for [SHA17] are obtained in the highest gain mode. Therefore, this reference achieves the same level of gain in its highest configuration than our design in our lowest gain configuration. This is illustrating that, a trade-off generally exists between achieved performances for the different applications targeted.

In the proposed power amplifier, this trade-off is relaxed as good levels of PAE and output power are reported, simultaneously with a limited power consumption, while high gain levels are measured. The very high gain measured in high-gain mode allows to achieve the highest ITRS FOM reported around 30GHz.

Concerning technologies, it is noticeable that CMOS SOI implemented power amplifiers permit to achieve the highest levels of gain and saturated output power, while the circuits in CMOS technology present the highest peak PAE values. The only circuit implemented in SiGe shows “middle-class” performances while no power consumption is reported. Finally, it is clearly highlighted with [WAN15] that 180nm CMOS technology node cannot offer the level of performances necessary for this kind of applications.

III.11 Power amplifier core performances extraction

As we explained along the chapter, oscillating conditions appeared in measurement around 35GHz and measurements operating conditions have been defined in order to provide stable conditions. The best performances have been obtained at 31GHz and we provide the measurements in the last section. Exploration have been conducted in order to find the origin of oscillations. It appears in simulations that a difference over the implemented C_{neutro} at common-source driver stage can lead to oscillations while it has no effect on the cascode power stage. Moreover, the driver C_{neutro} difference is leading to a gain modification between measurements and simulations at 31GHz. This is how we estimate the driver C_{neutro} difference, by modifying its value in post-layout simulation bench in order to find a good agreement between simulation and measurements at 31GHz and this is illustrated in Figure III.11.1. We estimate the driver C_{neutro} value at 20fF (4fF difference) to achieve the same levels of gain in simulation and in measurements in high-linearity mode.

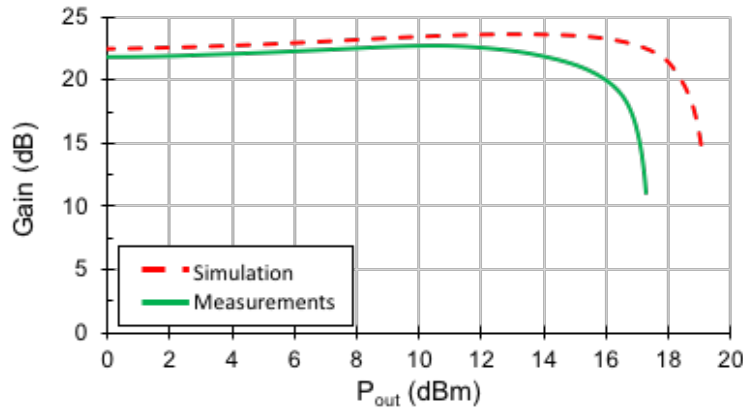


Figure III.11.1: Gain measurements versus simulations with driver $C_{neutro}=20\text{fF}$

However, while similar gain levels are achieved, we observe a P_{sat} difference between simulations and measurements. This is due to the power-cell and ground planes access resistance. We have been able to estimate the value of these resistances by defining the V_{DD_S2} and V_{b_CS} values that have to be applied in simulation to fit the measurements output power level and P_{DC} and compare them with the values applied during measurements. This is illustrated in Figure III.11.2.

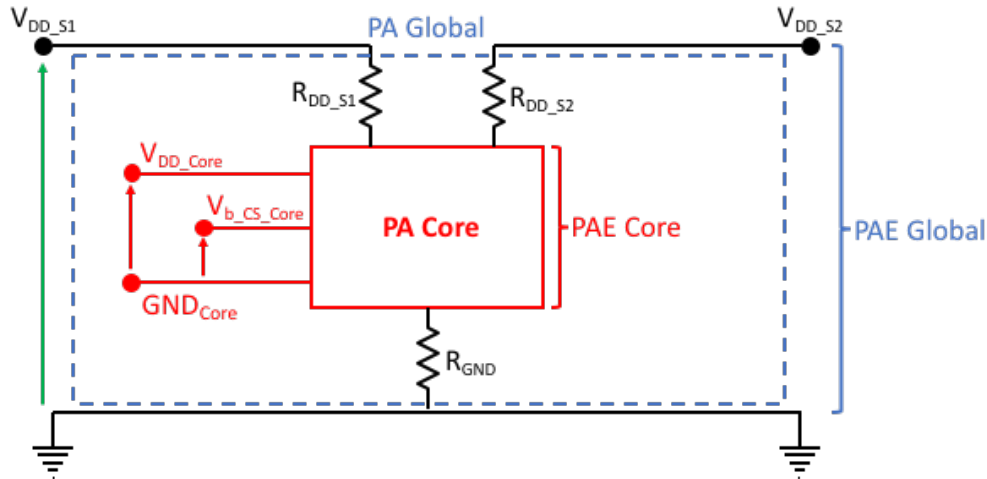


Figure III.11.2: Power amplifier core and access resistances

We estimate R_{VDD_S2} and R_{GND} values of 4Ω and 3Ω respectively. These resistances also impact the PAE by applying these access resistances in post-layout simulation, we can compare the simulated PAE with measurements in order to verify that these values are right (Figure III.13.3). As expected, P_{sat} between measurement and simulations are similar while PAE levels are accurate at 2%.

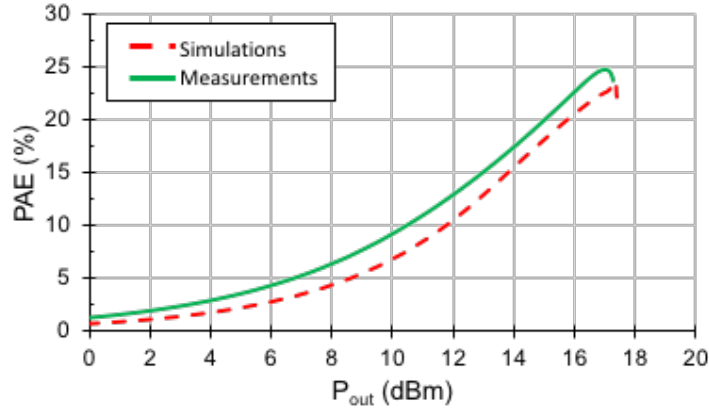


Figure III.11.3: PAE comparison between measurements and simulations featuring R_{VDD_S2} and R_{GND}

Finally, we are now able to define the core efficiency performances of this power amplifier, this performance is available in Figure III.11.4. Peak PAE of 35% is achieved at core and can be expected in future implementations with several design improvements or in a complete system.

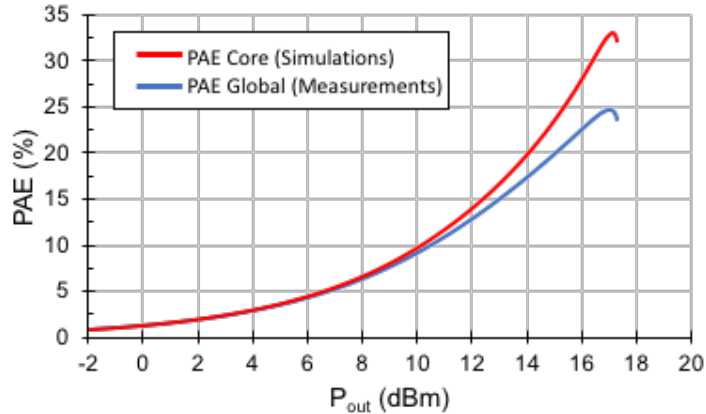


Figure III.11.4: Core efficiency performances of the designed power amplifier

Several remarks can be done on these defined values in order to improve the performances of future works. The C_{neutro} difference reported in this section corresponds to a difference between the intrinsic C_{GD} characteristic of the driver stage transistors and the associated neutralization capacitance. In order to avoid this drift that happens during manufacturing process, it is possible to use a MOS transistor in varactor configuration and sized to match the desired C_{GD} compensation [LAR15]. Concerning the access resistances, several bottlenecks have been identified in the circuit for both ground planes and that will have to be modified for future works. Furthermore, in order to reduce the supply voltage plan resistance, it would be possible to stack IB and IA metal levels to create this plan, instead of using only IA .

III.12 Conclusion

In the first half of this chapter, we present a balanced power amplifier implementation in 28nm FD-SOI for 5G applications around 30GHz that follows the design flow defined in Chapter II. Elementary transistor cell design exploration and overall balanced topology choice and implementation are first explored with the use of a promising 90° hybrid coupler design introduced in [MOR17]. The stages design topology and implementation are then discussed, the differential power stage is the first body-biasing enabled reconfigurable cascode topology implemented in 28nm FD-SOI technology while the differential first stage is featuring a common-source configuration. Layout optimization strategy for each stage is presented, targeting performance enhancement by limiting layout induced parasitics. Robust integration is also targeted notably with the implementation of dummies elements to limit process induced local variability. Impedance matching is then depicted, the choice of output load is made in order to get the best output optimal impedance compromise with respect to output power and efficiency contours during load-pull simulations for all operation classes. Robust integration and robustness are then discussed, showing the ESD protection used in this circuit, the performed ground path optimization and finally the achieved SOA and electromigration conditions.

In the second part of this chapter, small-signal and large-signal measurements have been presented for several operation and measurements conditions with all the losses induced by cables and mmW probes de-embedded from the results. A very wide and fine grain gain dynamic over 10dB is enabled thanks to body biasing variations between 0V and 1.65V. Two extreme modes have been identified and extensively explored during the measurements. The high-linearity mode is featuring a power gain of 21.9dB with a peak efficiency of 24.7% and a saturated output power of 17.3dBm while a 32.6dB power gain is reached in only two stages in high gain mode, with a PAE_{max} of 25.5% and a P_{sat} of 17.9dBm under full stable and reliable conditions at 31GHz. The quasi-constant peak efficiency and saturated output power obtained for all operation modes confirms the output load optimization strategy. Small-signal and large-signal measurements over several frequencies of operation exhibits performances compliant with an expected 5G frequency band, from 31.8GHz to 33.4GHz. Design and technology robustness to industrial temperature range have been demonstrated. Indeed, measurements with a chuck temperature up to 125°C are leading to a slight performances levels reduction at the frequency of interest for all body biasing conditions with no circuit dysfunction or degradation. Process spread robustness has also been demonstrated thanks to statistical study large-signal measurements, exhibiting very low performances standard deviations. This robustness to both temperature variations and on-wafer process variability demonstrates the possibility of mmW power amplifier robust integration in deep sub-micron CMOS technology in an industrial context thanks to a design aware of these problematics. Finally, a comparison and discussion regarding the measured performances of this circuit and the state of the art have been provided. It highlights state of the art performances and power gain reconfigurability with no required additional stage. Both peak and back-off efficiency enhancement are obtained compared with others circuits designed in the same technology with a reduced power consumption. The extreme

high gain achieved by this power amplifier in high-gain mode is leading to the best in class ITRS FOM around 30GHz, to the best of our knowledge.

III.13 Perspective: Wideband and reconfigurable 90° hybrid coupler

In this work, the overall power amplifier bandwidth is limited by the passive devices. For 5G applications, it is interesting to cover several 5G bands as frequency spectrum in mmW frequencies will be distributed in several bands. Therefore, to design wideband or frequency reconfigurable power amplifiers it is mandatory to implement wideband or reconfigurable passives. Balun bandwidth broadening techniques are available in the literature like in [SHA17] where a double tuned transformer technique is depicted. However, for balanced power amplifier design that provides high performance and robustness for 5G applications, even if wideband baluns are implemented the bandwidth will be limited by the 90° hybrid coupler. In this section, we provide a study for 90° hybrid coupler enhancement by using lateral ground planes effect generally avoided by the designers. Finally, a reconfigurable 90° hybrid coupler design featuring a wideband mode is proposed for future references.

III.13.1 Lateral ground planes placement exploration

Designers generally place the ground planes as far as possible from passive devices to avoid a negative and critical impact on overall performances. In this section, instead of making this traditional choice to limit the impact of ground planes, we want to take advantage of the coupler behavior modification induced by the presence of these ground planes to allow different operations than originally designed for. For this purpose, lateral ground planes are symmetrically inserted on both sides of the coupler, implemented on *IA* and *IB* metal layers and exhibiting a length of 325 μ m. The gap between lateral ground planes and coupler paths is noted *G*. A figure of this configuration can be found in Figure III.13.1. To ease extraction process on Momentum, full ground planes are used while in real implementation, ground planes are patterned.

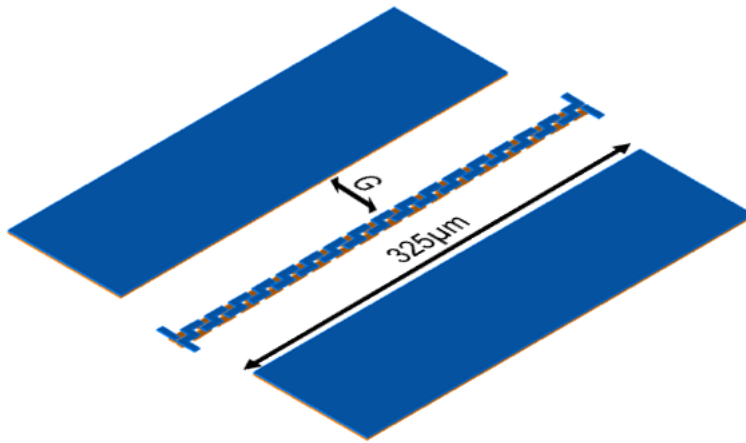


Figure III.13.1: 3D view of 90° hybrid coupler layout with lateral ground planes.

The presence of lateral ground planes on both sides adds a plate-to-plate capacitance between each path and ground as it is exhibited in Figure III.13.2.

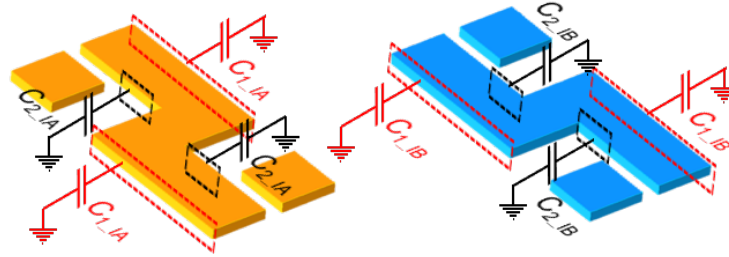


Figure III.13.2: Capacitances added on unitary cell.

Total capacitance for each IA and IB track in unitary cell C_{track_Ix} can be calculated with (III-17) where the capacitances C_{1_Ix} and C_{2_Ix} can be estimated for by using (III-18) with ϵ_0 the vacuum permittivity.

$$C_{track_Ix} = 2(C_{1_Ix} + C_{2_Ix}) \quad (III-17)$$

$$C_{n-Ix} = \frac{k_{Ix_eq} \cdot \epsilon_0 \cdot L_{Cn} \cdot t_{Ix}}{G_n} \quad (III-18)$$

To determine k_{Ix_eq} , the simplified oxide permittivity, it is possible to use (III-19) from [KRA77] where k_n and t_n are the permittivity and the thickness of a fixed oxide level n , as explained in Chapter II.

$$k_{Ix_eq} = \left[\sqrt{k_n} + \frac{t_{n-1}}{t_{n-1} + t_n} (\sqrt{k_{n-1}} - \sqrt{k_n}) \right]^2 \quad (III-19)$$

As IA and IB metal levels present same thickness and equivalent oxide permittivity, it is possible to write (III-20) to determine the overall added capacitance for each track C_{track_tot} depending on N the number of cascaded cells. In this design as the lateral ground planes are smaller than the overall coupler length, several capacitances in (III-20) do not exist. This leads to (III-21):

$$C_{track_tot} = N \cdot C_{track_Ix} \quad (III-20)$$

$$C_{track_tot} = N \cdot C_{track_Ix} - 2 \left(\frac{1}{3} C_{1_Ix} + C_{2_Ix} \right) \quad (III-21)$$

In the following study, lateral ground planes are placed at different distances G . For each G value, small-signal analysis similar than in section I is conducted. Minimal G value is fixed by technology design rules. G values and corresponding added capacitances on each track are given in Table I. Small-signal analysis results are presented in Figure III.13.3. Several remarks can be

done on the presented results. When the lateral ground planes are at a large distance of 50 μm from the coupler structure, there is no noticeable effect on performances compared to the standalone coupler presented in Section III.2.2. When ground planes are placed nearer, higher frequency of operation is reported, respectively 43.6GHz and 44.1GHz for G of 30 μm and 20 μm . For $G=10\mu\text{m}$, frequency of operation is 48.9GHz and a second frequency of 89.6GHz are obtained. Finally, when the ground planes are near the structure, for $G=4.5\mu\text{m}$, frequency of operation is significantly higher and a new operation mode appears. Instead of having one or two peak frequencies, a $\Delta\text{Amplitude}=0\text{dB}\pm 0.1\text{dB}$ is obtained over a wide band of frequency, from 62.8GHz to 69GHz. In this case, a very wide 1dB bandwidth of 39GHz, from 47GHz to 86GHz, is achieved with a ΔPhase of $92^\circ\pm 2.4$. Finally, if ground planes are placed too near, there is no frequency value where $\Delta\text{Amplitude}=0\text{dB}$ as for $G=2\mu\text{m}$, this behavior has no interest for targeted applications.

We have successfully demonstrated the possibility of taking advantage from lateral ground planes position to modify behavior of a 90° hybrid coupler to obtain a very wideband operation.

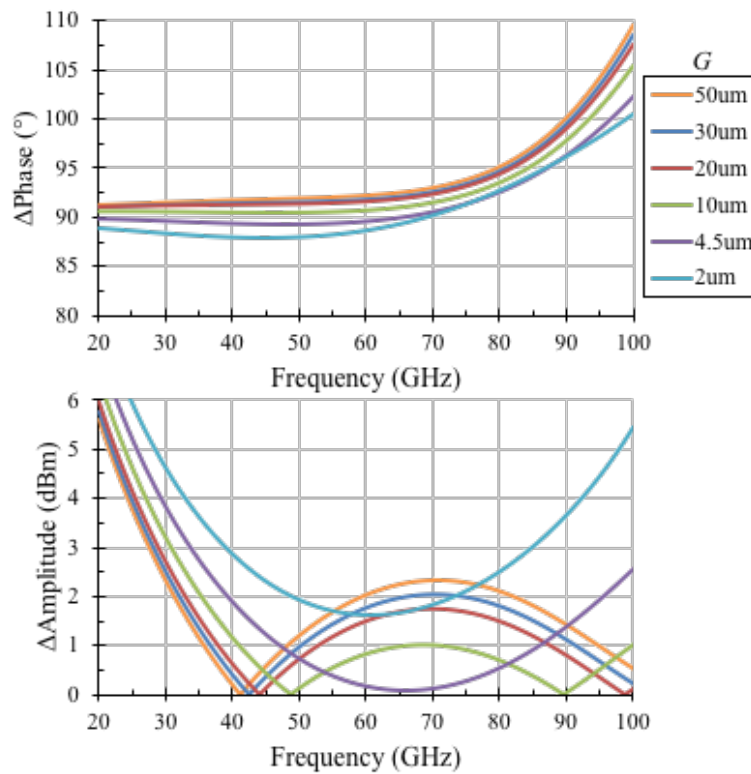


Figure III.13.3: Small-signal simulations for several ground planes distances from coupler.

Gap Distance G (μm)	Added Capacitance on one path (fF)
50	0.43
30	0.70
20	1.04
10	2
4.5	4.2
2	9

Table III.13.1: Added capacitances for several gap distances

III.13.2 Tunable and wideband 90° Hybrid coupler design

In this section a way to dynamically tune the gap value is explored, in order to allow several modes, with the same coupler and with fixed position of lateral ground planes for future silicon implementation. For this purpose, we propose a structure using metal strips with controlled states, floating or grounded. These strips are introduced between lateral ground planes and the coupler. When the strips are floating they are seen as dummies, no additional capacitance is added between coupler paths and ground. Whereas, when the strips are connected to the ground, supplementary capacitances are added like described previously. The objective is to obtain a tunable hybrid coupler featuring the 3 different modes identified in previous section and differs from [KNO17] that explores a way to refine central frequency using capacitors banks. Figure III.13.4 presents the design and dimensions. Geometrical parameters, like strips position and dimensions have been determined with Momentum extractions and parametric simulations, their optimum values are given in Table III.13.2. Several modes are possible to obtain. A first mode where both strips are set to floating state, a second mode where only one strip is grounded and the other floating and finally a third mode where both strips are set to ground. Second mode is only possible thanks to the symmetrical twisted design of the coupler that allows each path to see the same capacitance, and so no mismatch between direct or coupled path are introduced. Switches for strips state control can be easily implemented in the technology.

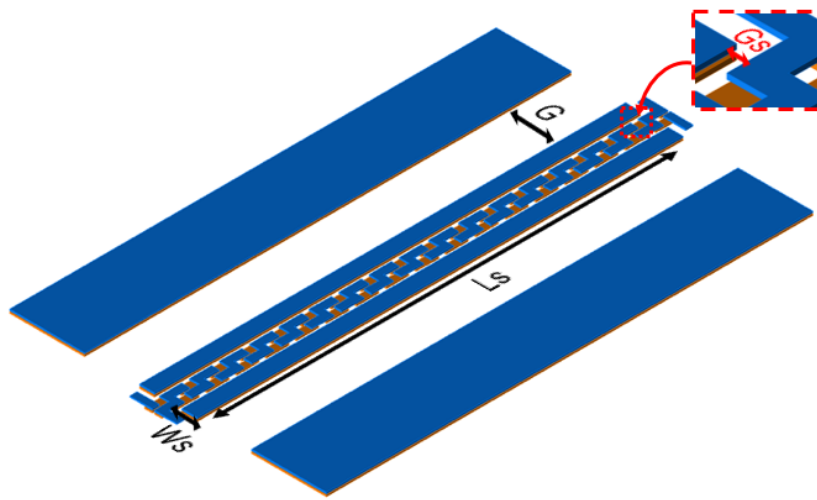


Figure III.13.4: 3D view of tunable multimode 90° hybrid coupler layout

Parameter name	Size (μm)
G	36.6
Ls	325
Ws	10
Gs	3.4

Table III.13.2: Geometrical parameters

Small-signal analysis have been performed for the three modes. The results can be found in Figure III.13.5. When both strips are floating (mode 1), the coupler exhibits an operating frequency of 42GHz with a 1dB $\Delta\text{Amplitude}$ bandwidth of 13.4GHz and ΔPhase of $91^\circ \pm 0.3^\circ$ with 0.45dB losses, a similar behavior to standalone coupler. Intermediary mode is obtained when only one of the strips is connected to the ground (mode 2), frequencies of operation are 46.4GHz and 85.1GHz. Losses of 0.44dB and 0.82dB are obtained for the two frequencies of operation respectively. Finally, when all the strips are grounded (mode 3), $\Delta\text{Amplitude} = 0\text{dB} \pm 0.1\text{dB}$ is obtained from 53.4GHz to 67.6GHz. 1dB $\Delta\text{Amplitude}$ bandwidth of 37.5GHz, from 42GHz to 79.5GHz, is achieved with a ΔPhase of $93^\circ \pm 1.7^\circ$ and losses of $0.5\text{dB} \pm 0.08\text{dB}$. This behavior is similar to Section III.13.1 case where the ground planes are near the coupler, enabling a very wide bandwidth and low phase variation in the operating frequency range. The controlled strips virtually expand lateral ground planes depending in their configuration and allow multimode reconfigurable operations. A comparison with the integrated coupler state of the art is provided in Table III.13.3. It is noticeable in Figure III.13.5 that a coupling greater than 3dB is achieved in mode 1. This is a common phenomenon known as over-coupling and can be observed in numerous commercial and academic 90° hybrid couplers.

	This Work*				[MOR17]*	[HOU13]	[HAR11]	[LIN10]
Technology	28nm FD-SOI CMOS					Standard CMOS	150μm GaAs	0.18μm CMOS
Tunability	Yes				No	No	No	No
Mode	1	2		3	/	/	/	/
Central Frequency (GHz)	42	46.4	85.1	60.5	29.5	135	84	26.5 [#]
BW @ xdB ΔAmplitude (GHz)	13.4 @1dB	25 @1dB	26.8 @1dB	37.5 @1dB	10 @1dB	50 @1dB	5 @0.3dB	11 [#] @1dB
ΔPhase on BW (°)	91 ±0.3°	91 ±0.7°	95.9 ±4.2°	93 ±1.7°	93.7 ±1°	90 ±3°	88 ±1°	97.5 [#] ±17.5°

*Simulated [#]Graphically estimated

Table III.13.3: Comparison with 90° hybrid coupler state of the art

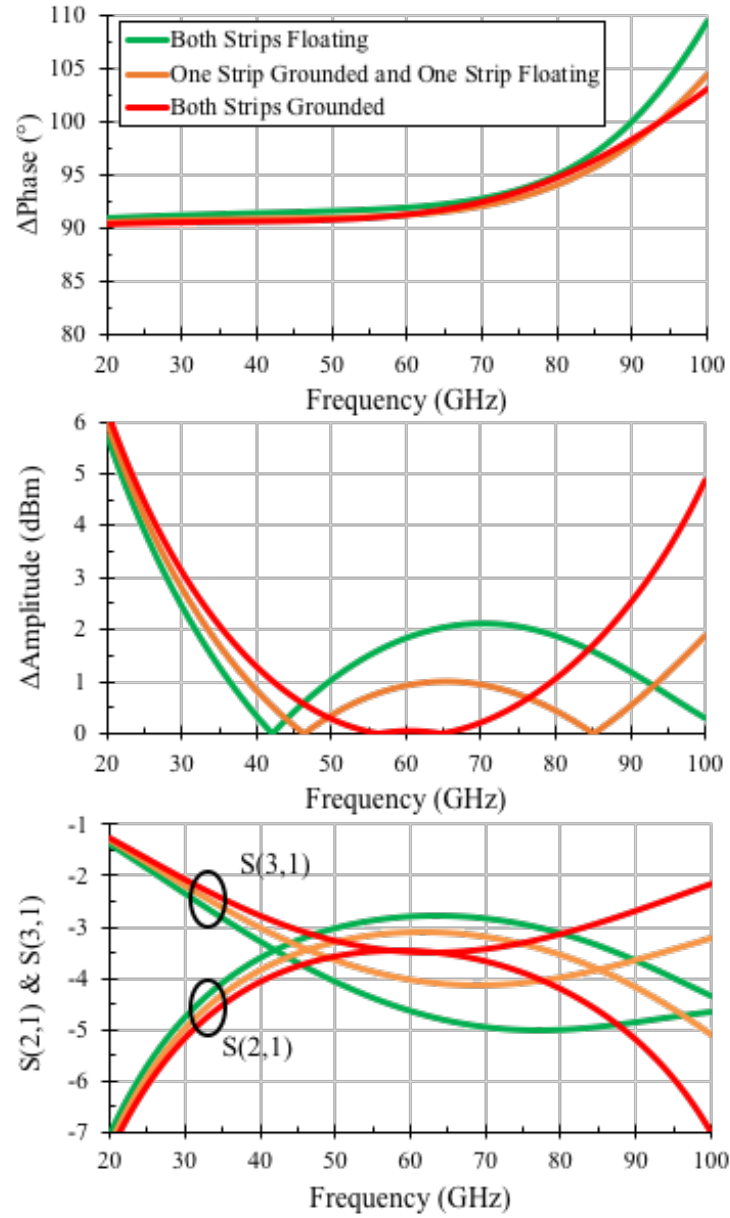


Figure III.13.5: Tunable Multimode 90° hybrid coupler simulated performances.

General Conclusion & Perspectives

Conclusion

In this thesis, the power amplifiers challenges induced by the next generation of mobile communication network have been identified and addressed. The 5G will leverage the connected world and several specifications are expected depending on the use-cases even if no standard is yet defined. The most challenging specifications are a low latency of 1ms, data-rates over 10Gb/s and a reduction of network power consumption of 90% while the network densification will enable its ubiquity.

The sub-6GHz 5G frequency bands will not be able to handle the high-data rates usages as they are offering limited bandwidth and suffer from spectral congestion. To enable these usages, a complementary spectrum at mmW frequencies is attractive as these frequency bands are offering wide bandwidth compatible with the desired high data-rates. For this purpose, several mmW frequency bands are actually under study for future standardization.

In dense urban areas, several technological techniques will be used like FD-MIMO, backhauling and beamforming phased-array to tackle the mmW frequencies transmission limitations. In this thesis, 30GHz power amplifier design solutions to target these applications have been proposed.

The power amplifier is the most power consuming bloc in transceivers. Efficiency improvement and reduced energy consumption are thus crucial for 5G. Furthermore, the complex modulations that will be used for 5G drive stringent requirements over linearity. Frequency and/or operating mode reconfigurability is expected to adapt the system performances to the required use-case operation. While CMOS technology is perfectly adapted for consumer market, the reconfigurability needs and standards drive the need for SoC integration in advanced technology nodes. The 28nm FD-SOI technology offers additional interesting characteristics and features that have been demonstrated in this thesis for RF and mmW applications.

While these specifications and challenges have been identified in Chapter I, the second chapter is dedicated to the specific design methodology for mmW 28nm FD-SOI power amplifier implementation. Several topologies for amplification stages and overall power amplifier have been discussed. The 28nm FD-SOI CMOS technology specificities and reconfigurability possibilities have also been presented. Impedance matching and possible implementations have been considered. In order to achieve fast and accurate passive devices prototyping in this technology, we proposed specific model and EM software optimization. Furthermore, stability and design optimization techniques have been explored to provide a specific step-by-step design flow for mmW power amplifier design in 28nm FD-SOI technology around 30GHz.

The final chapter is dedicated to the power amplifier design, implementation and measurements. We selected a 2-stages balanced overall topology to provide robustness to the environment variations that can occur in phased-array systems. This topology also enhances output power levels, matching, isolation, stability, reduces the IM3 and achieve ACPR improvements. The driver stage consists in a differential common-source delivering fixed gain. The power stage is featuring the first body-biasing enabled cascode topology in 28nm FD-SOI technology. It provides higher gain, isolation and output power levels. The overall design is oriented for robust integration. C_{GD} capacitive neutralization is implemented on each stage and ESD protections have been integrated. Electromigration, SOA and density rules have been carefully fulfilled. Transistor-level design optimizations have been conducted in order to reduce the process induced local variability.

On-wafer probing measurements have been realized and show good performances over the 31.8GHz-33.4GHz expected 5G frequency band. The body-biasing node voltage tuning on the power stage enables a continuous wide range ($>10\text{dB}$) gain tuning and dynamic class shifting from class AB to class A. Quasi no degradation of PAE and P_{sat} is reported over all the body-bias tuning range and is achieved thanks to the output impedance load optimization strategy. Robustness to both process variability and temperature of operation up to 125°C have been demonstrated with limited performances degradations and confirm the design choices. The comparison between measurements and targeted specifications identified in Chapter I is available in Table III.13.4. While all the aimed performances have been achieved, only peak efficiency shows lower values than expected due to passive devices induced losses.

	Targeted specifications	High-linearity mode	High-gain mode
P_{sat} (dBm)	> 17	17.3	17.9
PAE_{max} (%)	> 30	24.7	25.5
$\text{PAE @ 6dB } P_{\text{sat}} \text{ back-off}$ (%)	> 10	11.5	10.4
Power gain (dB)	> 16	21.9	32.6
$P_{1\text{dB}}$ (dBm)	> 15	15.3	11.6
Reconfigurability	Yes	Yes, power gain dynamic $> 10\text{dB}$	

Table III.13.4: Large-signal measurements versus targeted values

A comparison with the state of the art is provided in the third chapter. It highlights that this power amplifier offers good performances in terms of efficiency, output power levels and power consumption. The high-gain obtained with only two stages demonstrates the highest ITRS FOM at the frequency range of interest. Compared to previous power amplifier design in 28nm FD-SOI, efficiency levels are improved over all the tuning range. The achieved performances highlight the 28nm FD-SOI capabilities for mmW power amplifier design targeting 5G challenges. The fine grain power gain reconfigurability with no efficiency degradation allows an efficient control and response at system level for SoC implementation.

Perspectives

The complementary 5G spectrum at mmW frequencies from 30GHz will be composed of several frequency bands. At the moment, no frequency band is standardized upon 5G but several are under studies and could lead to a standardization (Table III.13.5).

Potential mmW 5G frequency bands (GHz) (WRC-15)	24.25 – 29.5
	31.8 – 33.4
	37 – 43.5
	45.5 – 50.2
	50.4 – 52.6
	66 – 76
	81 – 86

Table III.13.5: mmW frequency bands under study for 5G complementary spectrum

Therefore, it would be interesting for future 5G systems in base stations and end-user devices to be able to simultaneously cover several frequency bands from this spectrum or to be reconfigurable in frequency. This would reduce the number of implemented RF amplification chains in the systems, if we consider initially that one amplification path is covering one frequency band. Therefore, this would lead to area, cost and complexity reduction of the overall system. For this purpose, we can imagine several balanced power amplifier designs using the reconfigurable 90° hybrid coupler presented in Chapter III. Indeed, this tunable 90° hybrid coupler can address the 35GHz-95GHz frequency range, depending on the operating mode and the desired phase performances. It can thus cover several mmW 5G frequency bands. It is also noticeable that the coupler size can be refined to cover the mmW 5G frequency bands around 30GHz.

- PA with frequency switched operation:

In this topology, several amplification paths operating at different frequency bands are implemented. Each amplification path has its own input, output and inter-stage matching network in order to present single 50Ω ports at the input and output. Therefore, switches are implemented to select the desired amplification paths depending on the frequency band while the input and output 90° hybrid couplers are also configured for the desired operations. This technique can be schematically represented as Figure III.13.6. The advantage of this topology would be to enable balanced topology operation for different operating frequency ranges with limited additional complexity, and to use only one 90° hybrid coupler for splitting/combining instead of implementing 3 balanced PAs for the same covered frequency bands. Furthermore, the wideband mode of the reconfigurable 90° hybrid coupler is compatible with a wideband amplification path and therefore could cover several 5G bands simultaneously. The challenge with this topology is to cover all specifications for each targeted frequency band. Each different amplification path will have to be carefully designed to fulfill the corresponding frequency band

requirement (EVM, ACPR) and spectral mask. Furthermore, it will have to also achieve 5G required performances, notably in terms of efficiency, linearity, and low power consumption.

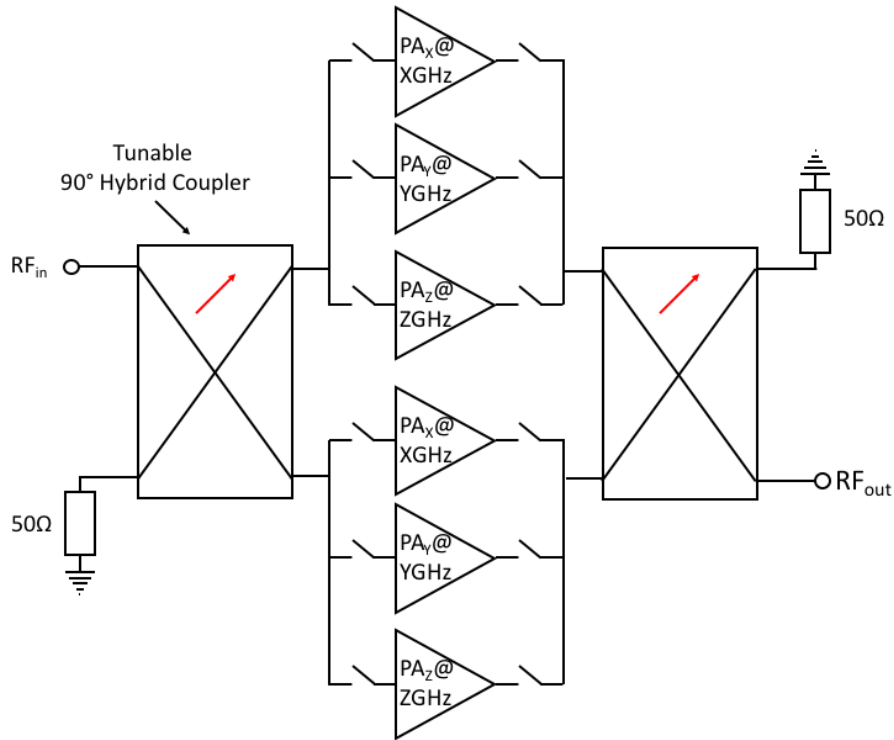


Figure III.13.6: Balanced frequency switched PA illustration

- Balanced wideband PA:

This topology is more classical than the previous one, however it also allows to cover several frequency bands depending on the bandwidth achievable by both amplification paths and 90° hybrid coupler. For this topology, no switch is necessary as it is possible to use the lateral ground planes at the right distance from the 90° hybrid coupler to enable the wideband operation as depicted in the Chapter III perspectives. The advantage of this topology is to provide wideband operation that was initially limited by the narrow band 90° hybrid coupler behavior. If we consider that the amplification paths can cover the same bandwidth than the novel 90° hybrid coupler, a 62% fractional bandwidth can be expected with a 60.5GHz central frequency. This means that the bandwidth limitations constraints have been moved from couplers to power cells and matching networks. Therefore, wideband passives like double-tuned transformers will have to be implemented, conjointly with wideband oriented power cells topologies like cascode. An illustration of this balanced wideband PA is available in Figure III.13.7, and is similar to a classical balanced topology with wideband hybrid couplers instead of classical ones.

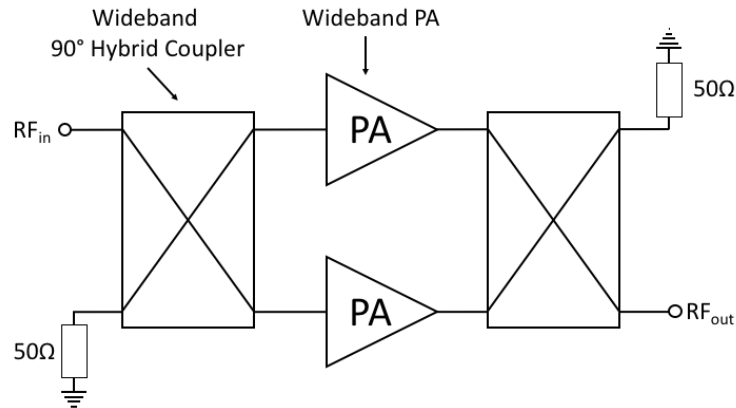


Figure III.13.7: Balanced wideband PA illustration

- Balanced multi-band PA:

In this topology, multi-band amplification paths are implemented, they can be reconfigurable or not but need to cover several frequency bands. Therefore, it is possible to implement the tunable hybrid coupler from Chapter III for balanced operations. The operating frequency band will thus be selected by the 90° hybrid coupler tuning and the amplification path frequency reconfigurability (if implemented). Wideband mode can also be available if the amplification path is able to handle it. Therefore, this is a solution even more compact than frequency switched topology for multiple band coverage. However, it will increase the complexity and constraints at amplification path level. An illustration of this concept is available in Figure III.13.8. This topology is similar to classical balanced architecture with tunable hybrid couplers instead of classical ones.

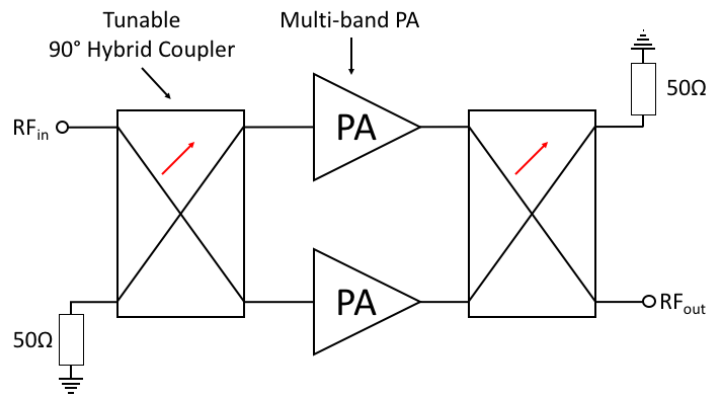


Figure III.13.8: Balanced multi-band PA illustration

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Glossary

1G:	First mobile network generation
2G:	Second mobile network generation
3G:	Third mobile network generation
4G:	Fourth mobile network generation
5G:	Fifth mobile network generation
ACLR:	Adjacent Channel Leakage Ratio
ACPR:	Adjacent Channel Power Ratio
APSK:	Amplitude and Phase-Shift keying
ASK:	Amplitude Shift Keying
BEOL:	Back-End-Of-Line
BOX:	Buried Oxide
BW:	Bandwidth
CDMA:	Code Division Multiples Access
CG:	Common-Gate
CMOS:	Complementary Metal Oxide Semiconductor
CP:	Cyclic Prefix
CS:	Common-Source
CW:	Continuous-Wave
DAT:	Distributed Active Transformer
DC:	Direct Current
DRC:	Design Rules Check
DRM:	Design Rules Manual
DUT:	Device Under Test
EDGE:	Enhanced Data rates for GSM Evolution
EM:	Electromagnetic

ESD:	Electrostatic Discharge
EVM:	Error-Vector Magnitude
FD-MIMO:	Full-Dimension MIMO
FD-SOI:	Fully-Depleted SOI
FinFET:	Fin Field-Effect Transistor
f_{\max} :	Maximum oscillation Frequency
FOM:	Figure of Merit
FQAM:	Frequency and Quadrature Amplitude Modulation
FSK:	Frequency Shift Keying
f_T :	Transition Frequency
GaAs:	Gallium Arsenide
GaN:	Gallium Nitride
GND:	Ground
GPRS:	General Packet Radio Service
GSM:	Global System for Mobile Communications
ICP1:	1dB Input Compression Point
IOT:	Internet Of Things
IP:	Internet Protocol.
ITRS:	International Technology Roadmap for Semiconductors
LTE:	Long Term Evolution
FBMC:	Filter Bank Multi-Carrier
LVT:	Low V_T
M2M:	Machine-to-Machine
MAG:	Maximum Available Gain
MIMO:	Multi-Input Multi-Output
mmW:	Millimeter-wave
MOM:	Metal-Oxide-Metal
MOS:	Metal-Oxide-Semiconductor

MSG:	Maximum Stable Gain
OBO:	Output Back-off
OCP1 / P_{1dB} :	1dB Output Compression Point
OFDM:	Orthogonal Frequency-Division Multiplexing
PA:	Power Amplifier
PAE:	Power Added Efficiency
PAPR:	Peak-to-Average Power Ratio
PBO:	Peak Back-Off
PCT:	Parallel power-Combining Transformer
PDC:	DC Power Consumption
P_{sat} :	Saturated Output power
PSCT:	Parallel-Series power-Combining Transformer
PSK:	Phase-Shift Keying
QAM:	Quadrature Amplitude Modulation
RF:	Radiofrequency
RVT:	Regular V_T
SCT:	Series power-Combining Transformer
SiGe:	Silicon-Germanium
SNR:	Signal-to-Noise Ratio
SOA:	Safe Operating Area
SoC:	System on Chip
SOI:	Silicon On Insulator
SOLT:	Short/Open/Load/Thru
SPCT:	Series-Parallel power-Combining Transformer
UMTS:	Universal Mobile Telecommunications System
UTBB:	Ultra-Thin Body and Buried oxide
VSWR:	Voltage Standing Wave Ratio