Development and validation of a predictive model to ensure the long-term electromagnetic compatibility of embedded electronic systems

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Abstract

With the technological evolution of integrated circuits (ICs) through the transistors scaling, which leads to the multiplication of the number of transistors within a chip, the requirements in terms of emission and immunity levels become more restrictive in the aeronautic, space and automotive industries. Moreover, since the evolution of Electromagnetic Compatibility (EMC) levels of electronic equipment after aging must meet the EMC long-term robustness requirements, the EMC margins defined by the manufacturers are often overestimated and the filtering systems designed by the equipment manufacturer could be oversized.

Therefore, for the integrated circuits dedicated to embedded applications, it is necessary to study the different aspects of EMC modeling as well as the reliability the modeling. These last years, several standards have been proposed for the construction of predictive EMC models such as ICEM-CE/RE (Integrated Circuit Emission Model for Conducted and Radiated Emission) and ICIM-CI (Integrated Circuit Immunity Model for Conducted Immunity). On the other hand, to integrate the effect of aging in EMC models, it is important to study the main intrinsic degradation mechanisms that accelerate the aging of ICs, such as HCI (Hot Carrier Injection), TDDB (Time Dependent Dielectric Breakdown), EM (Electromigration) and NBTI (Negative Bias Temperature Instability). For this purpose, there are existing models for the reliability prediction, such as the MIL-HDBK-217 standard and the FIDES standard. However, these models could take into account only the activation of one degradation mechanism. The combination of several degradation mechanisms could be critical for the IC performances and could contribute in the evolution of EMC level.

This dissertation introduces the different aspects of EMC and reliability modeling. This work deals with the construction of a conducted emission model of an FPGA and the proposition of new modeling methodologies. Furthermore, the reliability of the tested FPGA is described using a new predictive model, which takes into account the activation of the different degradation mechanisms. The reliability model has been combined with the EMC model for the long-term conducted emission level prediction.

Résumé

Avec l'avancement technologique des circuits intégrés à travers la miniaturisation des tailles des transistors et leur multiplication au sein d'une même puce, l'intégration des circuits dans des systèmes embarqués complexes, principalement dans l'industrie aéronautique, spatiale et automobile, rencontre de plus en plus d'exigences en termes de respect des niveaux d'émission et d'immunité. De plus, étant donné que l'évolution des niveaux de Compatibilité Electromagnétique (CEM) des équipements électroniques doit respecter ces exigences à long-terme, les marges définis par les industriels sont souvent surestimés et les systèmes de filtrages établis par les équipementiers peuvent être surdimensionnés.

De ce fait, pour les circuits intégrés dédiés aux applications embarquées, il est nécessaire d'étudier les deux aspects qui concernent la modélisation CEM ainsi que la modélisation de la fiabilité. Ces dernières années, des standards ont été proposés et permettent la construction de modèles CEM prédictifs tel que ICEM-CE/RE (Integrated Circuit Emission Model for Conducted and Radiated Emission) et ICIM-CI (Integrated Circuit Immunity Model for Conducted Immunity). De plus, pour intégrer l'effet du vieillissement dans les modèles CEM, il faut étudier les principaux mécanismes de dégradation intrinsèques aux circuits intégrés qui accélèrent leur vieillissement tels que le HCI (Hot Carrier Injection), TDDB (Time Dependent Dielectric Breakdown), EM (Electromigration) et NBTI (Negative Bias Temperature Instability). Des modèles standardisés sont utilisés dans les différents domaines industriels qui permettent la construction de modèle de fiabilité tels que le standard MIL-HDBK-217 et le standard FIDES. Cependant, ils ne permettent de prendre en compte qu'un seul mécanisme de dégradation à la fois.

Ce manuscrit de thèse introduit ces aspects de modélisation CEM et de fiabilité. Il traite également la construction d'un modèle d'émission conduite d'un FPGA avec la proposition de nouvelle méthodologie de modélisation. Ensuite, l'étude de la fiabilité du FPGA est décrite à travers l'utilisation d'un nouveau modèle permettant la prise en compte des différents mécanismes de dégradations et a été combiné au modèle CEM pour la prédiction des niveaux d'émissions conduite à long-terme.

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List of acronyms

EMC	Electromagnetic Compatibility
DSM	Deep Sub-Micron
CMOS	Complementary Metal-Oxide-Semiconductor
TSV	Through-Silicon Vias
IC	Integrated Circuit
CISPR	Comité International Spécial des Perturbations Radioélectriques
IEC	International Electrotechnical Commission
CE	Conducted Emission
RE	Radiated Emission
CI	Conducted Immunity
RI	Radiated Immunity
PCB	Printed Circuit Board
EOT	Equivalent Oxide Thickness
LSTP	Low Standby Technology for Portable applications
EMI	Electromagnetic Interference
FIT	Failure In Time
MTTF	Mean Time To Failure
AGREE	Advisory Group for Electronic Reliability of electronic Equipment
COTS	Commercial Off-The-Shelf
FPGA	Field Programmable Gate Array
CFR	Constant Failure Rate
TDDB	Time Dependent Dielectric Breakdown
EM	Electromigration
NBTI	Negative Bias Temperature Instabilities
HCI	Hot Carrier Injection
CHC	Channel Hot Carrier
DAHC	Drain Avalanche Hot Carrier
CHE	Channel Hot Electron
LEM	Lucky Electron Model
SBD	Soft Breakdown
HBD	Hard Breakdown
GIDL	Gate Induced Drain Leakage
SRAM	Static Random-Access Memory
EMR	Electromagnetic Robustness
OEM	Original Equipment Manufacturer
HTOL	High Temperature Operating Life
LTOL	Low Temperature Operating Life
PTC	Power Temperature Cycling
EME	Electromagnetic Emission

EMS	Electromagnetic Susceptibility
SMPS	Switch-Mode Power Supplies
DPI	Direct Power Injection
PLL	Phase-Locked-Loop
ICEM	Integrated Circuit Emission Model
ICIM	Integrated Circuit Immunity Model
IBIS	Input/Output Buffer Information Specification
PDN	Power Distribution Network
IA	Internal Activity
IBC	Inter-Block Coupling
PI	Power Integrity
FEM	Finite Element Method
MoM	Method of Moment
FDTD	Finite Difference Time Domain
PWL	Piece Wise Linear
VLSI	Very Large Scale Integration
CLB	Configurable Logic Blocs
ELECIS	Electronic board for Long-term Electromagnetic Compatibility Issues Simulation
SI	Signal Integrity
VNA	Vector Network Analyzer
PEEC	Partial Element Equivalent Circuit
FE FD	Finite Element Frequency Domain
RMS	Root Mean Square
XPA	Xilinx Power Analyzer
EIA	Electronic Industries Alliance
JEDEC	Joint Electron Device Engineering Council
PoF	Physics-of-Failure
HALT	Highly Accelerated Life Test
HASS	Highly Accelerated Stress Screen
ALM	Accelerated Lifetime Model
AF	Acceleration Factor
TST	Transition State Theory
IPL	Inverse Power Law
BAZ	Boltzmann Arrhenius Zhurkov
MTOL	Multiple Temperature Operational Life model
M-HTOL	Multiple High Temperature Operational Life test
MSTORM	Multi-phySics mulTi-stressOrs predictive Reliability Model
SSALT	Step-Stress Accelerated Life Test

General introduction

Thesis context

For many years, Electromagnetic Compatibility (EMC) has been a major constraint on electronic systems to ensure limited electromagnetic emission level and sufficient immunity to electromagnetic interference. This requirement is essential to guarantee safety levels in critical and long-term industrial applications. EMC does not only concern electronic systems and equipment, but also integrated circuits (ICs). Indeed, they are at the heart of EMC problems, since they are the source of electromagnetic emissions produced by an electronic system, but also the hardly disturbed element when this electronic system is subjected to electromagnetic interference. Thus, EMC has become a major challenge for integrated circuits [1].
On the other hand, the technological evolution and the improved flexibility of integrated circuits have widely increased their integration in the aeronautical, space and automotive applications. However, this technological evolution is not without consequences on the emission and immunity levels of integrated circuits, mainly related to the increase in the number of transistors and the ever growing operating functions as well as the switching frequencies. Hence, in order to predict the EMC level of ICs using simulation tools, existing IEC standards (e.g. IEC 62433 [2]) have been proposed for the anticipation of EMC issues in order to propose and test solutions. These models allow avoiding the requalification phases in case of obsolescence and second sourcing and lead to saving time and money. In addition, besides the prediction of emission and immunity level at a PCB level, these models can help to assess and improve the effect of decoupling and filtering network, the PCB design and the IC configuration.

- **ICEM-CE**: Integrated Circuit Emission Model for Conducted Emission
- **ICEM-RE**: Integrated Circuit Emission Model for Conducted Emission
- **ICIM-CI**: Integrated Circuit Emission Model for Conducted Emission

However, the presented EMC of IC models are not very much spread due to IC manufacturing confidentiality issues, and the low profit in developing such models comparing to their cost. Furthermore, the existing method for the construction of EMC of ICs models presents several limitations, such as their dependence on measurements and the need of multiple optimization phases. Thus, the present work research deals with a key question for EMC modeling: How to construct an EMC of a complex IC model using a new predictive methodology in a reduced time and set of data?

Besides the EMC aspect, the reliability of IC is also a binding subject. During their operating lifetime, integrated circuits are affected by different intrinsic degradation mechanisms, which are accelerated due the harsh environmental operating conditions (high temperature, thermal cycling, electrical stress, etc.). These degradation mechanisms do not only cause the breakdown of integrated circuits (hard failure), but also lead to the generation of drifts in the performances of

integrated circuits (soft failure). This effect is increasingly noteworthy in CMOS (Complementary Metal-Oxide-Semiconductor) circuits with deep submicron (DSM) technology (gate size less than 90 nm) [3][4]. There are existing standard models for the prediction of the reliability of ICs for the different industrial applications. The most traditional standards for reliability modeling are the MIL-HDBK-217F and FIDES, but they have been proposed considering only one dominant failure mechanism and do not take into account the possible combination of several degradation mechanisms after aging. Hence, the need of a modern reliability model for advanced ICs has been felt and recent researches dealing with their development.

On the other hand, even if the aging of ICs does not compromise the functioning of the circuit, it can present a significant impact on EMC performance, as shown in recent research works [5][6][7][8]. The acceleration of the intrinsic degradation mechanisms in integrated circuits can lead to the variations of emission and immunity levels, affecting the EMC margins required by the final application. Therefore, there is no certainty that in a given environment and after certain lifetime duration, an electronic system is still compliant from an EMC the point of view. Figure 1 describes the problem of long-term electromagnetic robustness for aeronautic applications. Today, there is no existing tool that allows the prediction of EMC variations during the life cycle of a system. The recent researches that study the aging effect on EMC level relies on measurements under specific testing conditions and do not propose any method to predict the EMC level for untested operating conditions. The objective of this project is to demonstrate the feasibility of the construction of a new predictive electromagnetic robustness model.

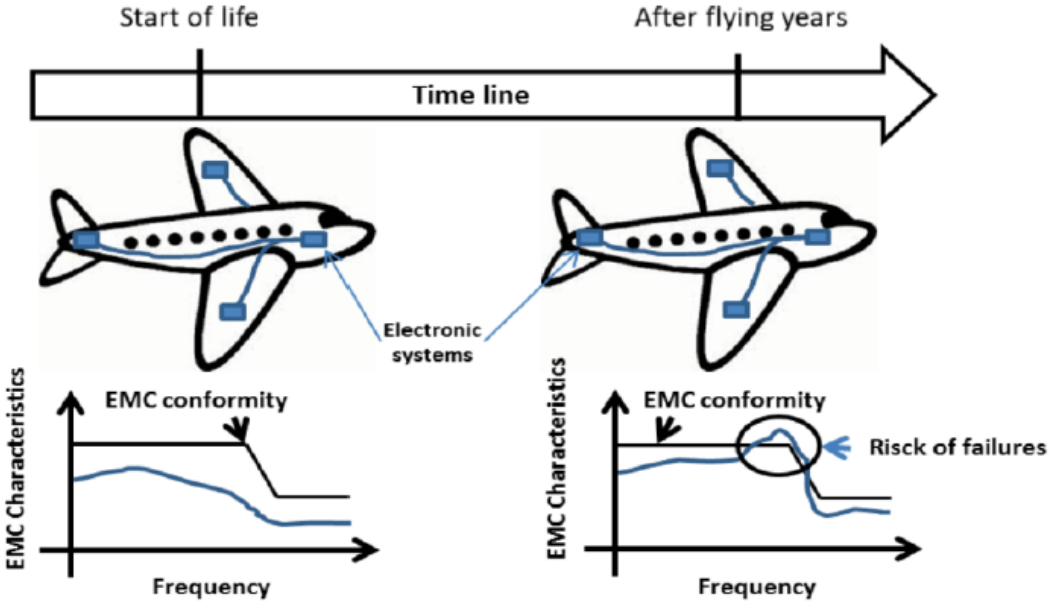

Figure 1 Long-term electromagnetic robustness

This thesis is part of the work package 3 of the “Robustesse Electronique” (Electronic Robustness) project of IRT Saint-Exupéry deals with the development of predictive models to ensure the long-term electromagnetic compatibility robustness of embedded electronic systems. The purpose of this work is to develop EMC models for integrated circuits that take into account

the environment and aging effect [9]. This project is supported by several industrials in Toulouse region (Continental, Airbus group innovation, Airbus, Nexio) and academic structures (LAAS CNRS, IMS Bordeaux).

The results of the work leaded in the work package 1 of the “Robustesse Electronique” project concern the construction of a predictive reliability model that combines the different activated degradation mechanisms with a multiple stress method. These results have been followed up for the long-term electromagnetic robustness prediction [10][11].

Compared to traditional reliability studies, the present long-term EM robustness study does not focus only on the components’ lifetime, but also on the evolution over time of electromagnetic emission levels of ICs. The long-term electromagnetic robustness research work is applied to circuits that remain functional after a given period of stress.

As presented in Figure 2, the aim of this project is the development of a generic methodology for the prediction of EMC level of an IC before and after aging under any operating conditions.

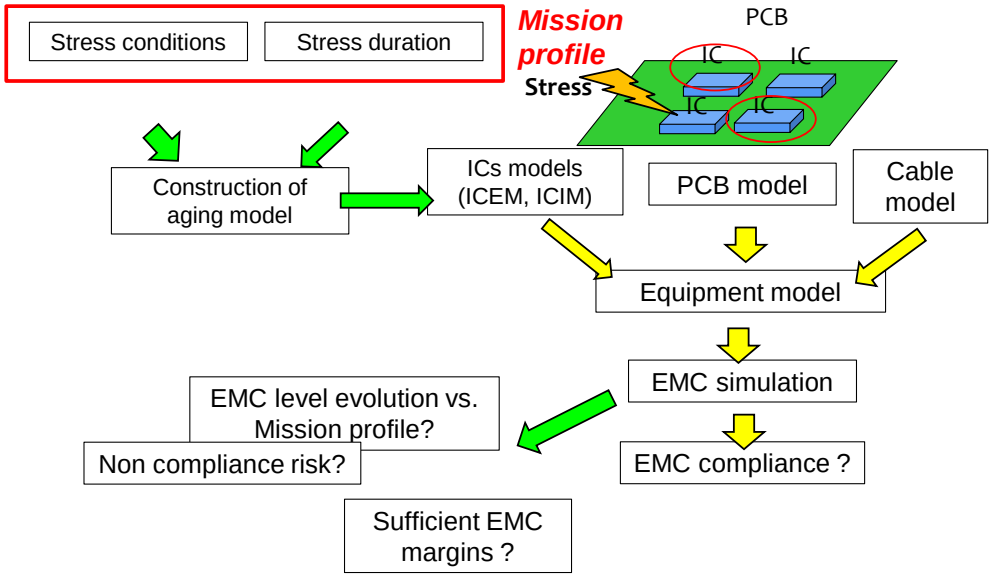

Figure 2 Workflow of long-term electromagnetic robustness prediction

Scope of this dissertation

Based on the context presented above, this thesis deals with two main subjects:

- The improvement of IC models for EMC, especially the construction of ICEM-CE model for advanced integrated circuits dedicated to embedded applications with a proposal of new construction methodology to overcome the issues of the standard methods.
- A new methodology proposal for the prediction of long-term conducted emission level based on a new reliability model. This model must be predictive, i.e. able to extrapolate the mean time required to a given EMC level drift in various stress conditions, even if there are multiple stress sources.

This manuscript is organized as follow:

The Chapter I presents a general overview on the effect of ICs reliability issues on the long-term electromagnetic robustness. This chapter introduces the technological evolution of CMOS circuits and the different aspects of EMC of ICs as it is presented in the state of the art. Furthermore, the reliability of ICs is explained with the presentation of the main activated degradation mechanisms during the operating lifetime of a CMOS IC. Finally, previous long-term electromagnetic robustness research works are briefly summarized.

The Chapter II deals with the methodology of construction of an ICEM-CE model of a complex digital circuit (in this study, a FPGA designed in 45 nm CMOS technology). The different blocks of the ICEM-CE model are constructed following the standard methods. In addition, a new methodology is proposed for the construction of the internal activity of the FPGA based on the manufacturer estimation tools and the component signal integrity models (IBIS). Compared to the standard approach, the proposed method simplifies the model extraction process and limits the influence of uncertainty. The results of this new approach will be compared to the standard method. Finally, a new developed tool for automatic extraction of the IA block is presented.

The Chapter III introduces the traditional and most recent models for reliability prediction used in the different industrial applications. To understand the reliability modeling approach, different acceleration models are presented for single and multiple stresses studies. Finally, the MSTORM model that allows the reliability prediction for combined degradation mechanisms is introduced. MSTORM will form the basis of the proposed methodology to predict the long-term electromagnetic robustness of ICs.

The Chapter IV presents the methodology of accelerated aging tests in order to construct the reliability model of the studied FPGA and compare the obtained data to the MSTORM model. Furthermore, the aging tests allow observing its effect on signal integrity and conducted emission (CE). Then the observed drift for a given time to failure is integrated into the ICEM-CE model for CE level simulation.

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Chapter I. Effect of ICs reliability issues on long-term electromagnetic robustness

With the development of the nanoscales circuits and their strong integration in the different embedded application areas, the EMC constraints raise more problems related to the evolution of the electrical characteristics of the integrated circuits. In addition, the integration of the Deep Sub-Micron (DSM) circuits in critical environments implies the appearance of degradations, which impairs the functional safety of the electronic devices. Thus, it has become crucial to study the electromagnetic compatibility compliance and the reliability of integrated circuits to characterize their electromagnetic robustness.

In this chapter, the first section is dedicated to a presentation of the technology evolution from the past to the predicted future, and the different aspects of the electromagnetic compatibility (emissions, susceptibility) of integrated circuit are presented and the transistors scaling impact on the evolution of the electromagnetic compatibility is discussed. The second section concerns the reliability of integrated circuit, the different degradation mechanism will be presented and their evolution with the new technologies. Finally, the aging effect on the electromagnetic emissions and susceptibility is presented with case studies from the “state of the art”.

1. Overview on EMC of integrated circuits

1.1. Evolution of CMOS technology

1.1.1 CMOS technology scaling theory

The birth of CMOS (Complementary Metal-Oxide-Semiconductor) technology took place in 1963; it was invented by Franck Wanlass at Fairchild semiconductor. Since then, CMOS technology is widely used for the development of integrated circuits as microprocessors, microcontrollers, memories and other digital circuits. The evolution of the economic context of electronic industry since the 1990’s implied strong requirements in terms of reducing the power density and increasing the performance of integrated circuits.

Over the last 15 years, the use of integrated circuits has evolved in the various application areas. The main purpose was to miniaturize electronic equipment to include increasingly complex electronic functions in a reduced space, which affected the transistors scaling [12]. As displayed below in the Figure I-1, the CMOS technology process has presented an important shrinkage from 180 nm in 2000 (2D technology) to reach 5 nm in 2020 involving the 3D technology from 2012. The 3D technology integration consists in manufacturing integrated circuits by stacking silicon wafer vertically using through-silicon vias (TSV) interconnections. The 3D technology allows the increase of system performance with decreasing the interconnect distance between the region of a chip and decreasing wiring parasitic [2].

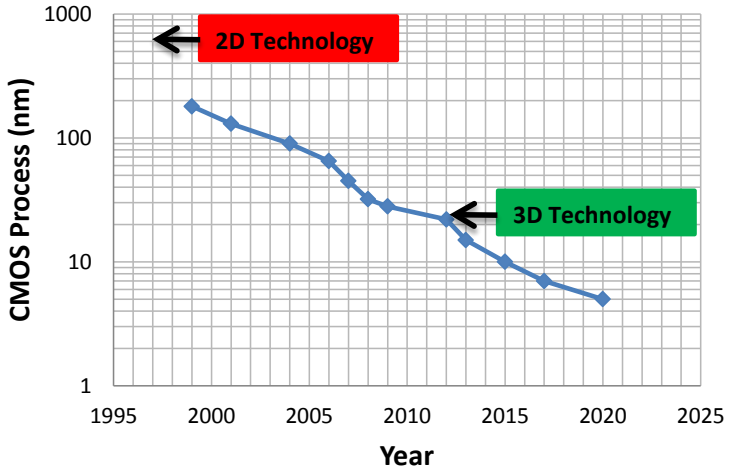

Figure I-1 Reduction of the gate length of CMOS process over the years

In 1965, Gordon Moore observed that the number of components inside a chip has doubled every 18 months [14]. He established an outstanding law called Moore's law that gave a quantitative estimation of the electronic progress. The evolution of the digital electronic industry predicted by Moore's law presented a good accuracy for the last decades and involved a major technological advance of various digital circuits as the increase of memories capacity and the development of sensors. The consequence of electronic industry progress for the last 40 years is presented in the Figure I-2 where the data was collected by [15] and completed for 2010-2015 by K. Rupp, it shows an important evolution of transistor count as predicted by Moore's law due to the reduction of the gate length which enhanced the number of logical cores. In the same Figure, as suggested by Dennard [16], the power density growth is proportional to the number of transistors; the reason of the power density increase is related to the die size and the fast frequency scaling [17].

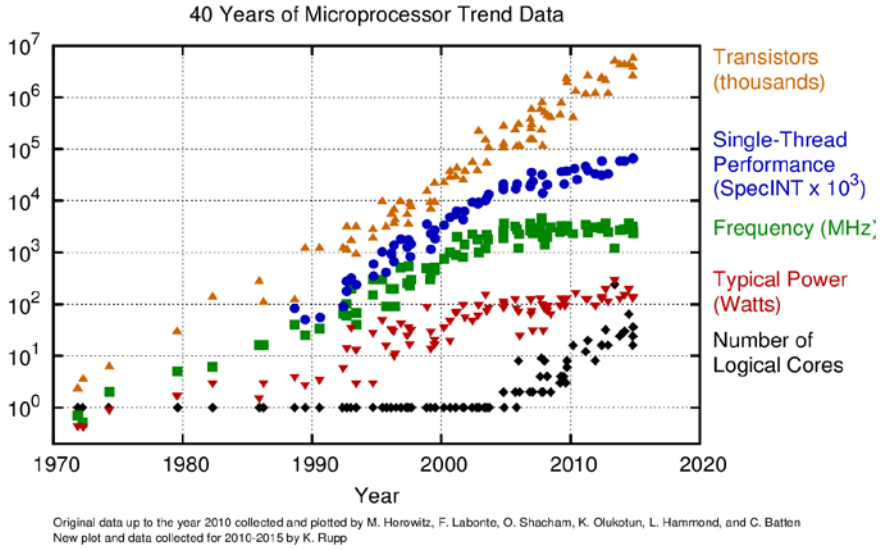

Figure I-2 Evolution of ICs characteristics with the technology scaling [15]

1.1.2 Impact of technology scaling on ICs

The evolution of the CMOS technology scaling has a major impact on the performances of the ICs. A significant decrease in performance gain is predicted below the power supply voltage of 1,5 V. This is related to the threshold voltage which decreases more slowly than the historical trend and leads to an aggressive design of MOS devices with a very high electric field in the gate oxide. Thereby, in the last six decades, manufacturers of devices for critical applications such as aeronautic, automotive, space and military have contributed to the development of the semiconductor reliability field. The main challenges that can hinder the transistors scaling can be depicted by different categories: the **physical challenge** comes from the increase of the leakage current which induce a negative leverage on the CMOS device functionalities, the **power-thermal challenge,** as mentioned in the previous paragraph, the increase of the transistors count leads to the increase of the power consumption and the need of a higher thermal dissipation, the **material challenge** is mainly related to the ability of the dielectric and the wiring materials to insure a reliable insulation and conduction, the **technological challenge** results from the lack of competence of lithography-based techniques to afford a resolution below the wavelength of light to manufacture CMOS components, and finally the **economical challenge** related to the increase of the cost of manufacturing more scaled transistors [18].

For the new scaled transistors technologies the power consumption at a single switching event has decreased, but the total on chip power consumption increased. The technology scaling impact on the power consumption concerns the dynamic power consumption and the leakage current, as presented in the Figure I-3 the dynamic power P_{act} increases linearly and the leakage power P_{leak} is increasing exponentially, due to the scaling down of the threshold voltage, and presents a higher sensitivity to the temperature [3]. In digital CMOS components, leakage power is a critical parameter that strongly affects the performance of the circuits; it induces the over-heat of the device and the decrease of the circuit lifetime. As a result the leakage power must be thoroughly controlled during the early design stages.

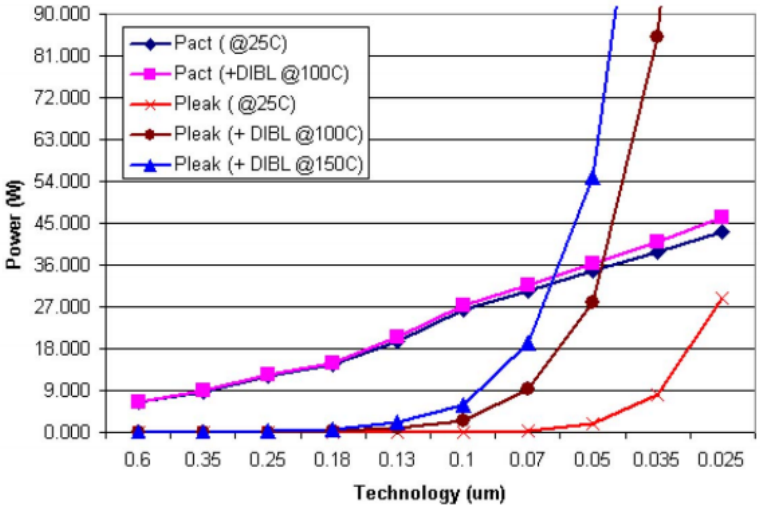

Figure I-3 Evolution of the leakage power and the dynamic power with technology scaling for different temperatures and constant die size [3]

The fast operating frequencies and the increased complexity of integrated circuits through the evolution of packaging, the transistors scaling and the wafer process are at the origin of the increase of the noise generated by internal switching events of the circuit which make the device a major source of noise. It can lead to an important dysfunction that cause critical problems as the signal integrity problems of advanced DSM (Deep Sub-Micron, refers to devices with a gate length less than 90 nm) technology in digital devices and lead to the crosstalk errors in the fast numerical busses.

Advanced researches are carried on to assess and control the increase of the noise generated by digital components and the study of long-term reliability of ICs has become an overriding qualification step for semiconductor manufacturers and component vendors. In the next paragraphs these different aspects will be discussed in detail.

1.2. Electromagnetic compatibility of integrated circuits for embedded applications

The Electromagnetic Compatibility (EMC), as defined by ISO 11451, is “the capacity of a device, equipment or a system to function satisfactorily in its electromagnetic environment, without introducing electromagnetic disturbances such as to create noise that could impair the proper functioning of the devices or systems located in its environment”.

The EMC problems can be depicted into three elements as shown in the Figure I-4:

- **Source**: the origin of the electromagnetic energy that causes the disturbances (lightning, electrostatic discharge, high speed data trace, IC…)
- **Victim**: the receptor of the disturbance that cannot function properly due to the electromagnetic interference (electronic device, IC, high speed data trace…)
- **Coupling path**: the coupling mode that drives the disturbance from the source to the victim (cables, parasitic inductance, parasitic capacitance, antenna, power rails, ground plane…). The coupling path could be as a conducted mode or a radiated mode.

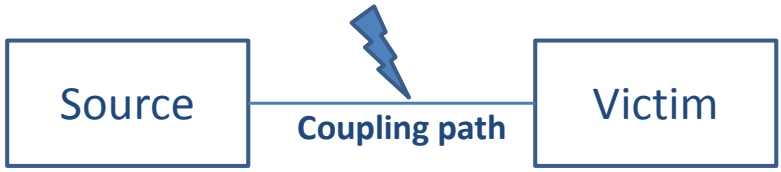

Figure I-4 Elements contributing in an EMC

If Electromagnetic laws are known since the publication in 1865 of the famous Maxwell laws, the EMC concept appeared early in the 1930’s with the emergence of radio communications and became an important concern during the second world war; when interferences between radio and air navigation systems posed several functional problems. This era saw the creation of the CISPR (Comité International Spécial des Perturbations Radioélectriques) by the IEC (International Electrotechnical Commission) which develops standards to avoid the critical effects of interference. The appearance of the new CMOS process has raised the EMC problems which have worsened with the DSM technology due to the increase of the number of logic gates inside an IC.

The two aspects dealt with by EMC studies are emission; it represents the noise generated by the component, equipment or the electronic system and the susceptibility aspect which is the noise levels that cause a malfunction of an electronic device, as presented in the Figure I-5. Both emissions and susceptibility are related to different areas of integration (aeronautic, automotive,…) [1] and could be divided into four categories:

- The **Conducted Emissions** (CE) where the noise produced by the device or an equipment is transmitted to the victim through the wires,
- The **Radiated Emissions** (RE) where the noise produced by the device or an equipment is transmitted to the victim through the air,
- The **Conducted Susceptibility** (CS) or **Conducted Immunity** (CI) where the noise produced by the aggressor is transmitted to the victim through the wires,
- The **Radiated Susceptibility** (RS) or **Radiated Immunity** (RI) where the noise produced by the aggressor is transmitted to the victim through the air.

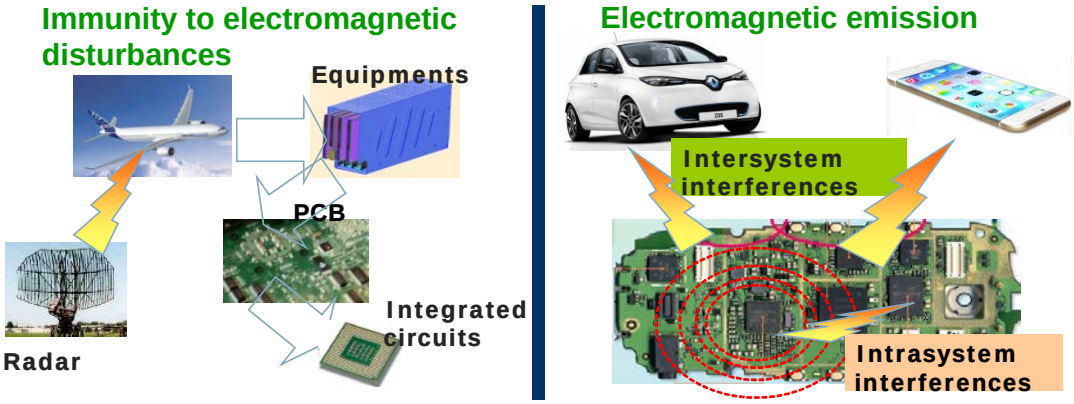

Figure I-5 EMC issues of integrated circuits [1]

To ensure sufficient compatibility of the different electronic devices it is necessary to ensure a low emission and susceptibility profile; this is the critical condition for industrials to guarantee a sufficient functional safety level. Moreover, the integrated circuits degradation can have a significant impact on EMC performances as proven by recent researches; hence, before addressing the long-term reliability aspect, it is essential to understand the origin and the consequences of both emission and susceptibility of ICs. The existing standards for EMC requirements at an electronic equipment level and IC level are detailed in Annex 1.

1.2.1 Electromagnetic emissions of ICs

1.2.1.1 General overview on electromagnetic emissions

As defined by the IEC [26], “the Electromagnetic emission is the phenomenon by which electromagnetic energy emanates from a source and is released into its environment”.

In aeronautical systems, different electronic devices can be the source of parasitic emissions. Cellular phones, laptops, televisions, signals transmitted by radars and also embedded aeronautical equipment. All these electronic systems operate in different frequency bands as

presented in the Figure I-6, and could alter the RF communications and security systems through conducted or radiated coupling.

Figure I-6 Sources of EME in an aeronautical system

The origin of the parasitic emissions is mainly due to the dynamic current consumed during the activation of each logic gate of an IC. The sudden and rapid variation of the amplitude of the current conducted through the supply rails causes large fluctuations in the supply voltage due to the parasitic inductance of the internal IC traces, the bonding wires, the package lead frames, and the printed circuit board (PCB) traces.

1.2.1.2 Impact of technology scaling on electromagnetic emissions

The miniaturization of the CMOS circuits, involving the reduction of the gate length Lg and the equivalent oxide thickness EOT, has led over the years to increase the current (I_{on}) consumed when the transistor is in the on state and also the leakage current (I_{off}) flowing when the transistor is in the off state. The Table I-1 presents the evolution of the Ion / Ioff currents and the supply voltage Vdd for two different DSM technologies: HP (High Performance) and LSTP (Low Standby Technology for Portable Applications) [27].

In an IC embedded application, a combination of hundreds of thousands logic gates are switching at the same time, it leads to a dynamic current consumption with very high amplitudes, which is at the origin of the increase of the parasitic emission of the IC.

Year of production	2004	2007	2010	2013	2016
Technology node (nm)	90	65	45	32	22
HP physical Lg (nm)	37	25	18	13	9
EOT (nm) (HP/LSTP)	1,2/2,1	0,9/1,6	0,7/1,3	0,6/1,1	0,5/1,0
Vdd (HP/LSTP)	1,2/1,2	1,1/1,1	1,1/1,0	1,0/0,9	0,9/0,8
Ion/W,HP (mA/mm)	1100	1510	1900	2050	2400
Ioff/W,HP (mA/mm)	0,05	0,07	0,1	0,3	0,5
Ion/W,LSTP (mA/mm)	440	510	760	880	860
Ioff/W,LSTP (mA/mm)	1e-5	1e-5	6e-5	8e-5	1e-4

Table I-1 Excerpt of 2003 ITRS technology scaling from 90nm to 22nm [27]

The increase use of high-performance microprocessors and microcontrollers with several clocks and different frequencies as well as the increase in the operating frequencies of the ICs create high-frequency parasitic emission spectrum that may disturb the sensitive applications [33]. The evaluation of future ICs developments is necessary to illustrate the evolution of parasitic emission to meet the requirements of both manufacturers and customers of ICs. If we do not integrate any EMC optimization strategy, parasitic emissions will tend to increase in the future with advanced technologies as shown in Figure I-7 [32].

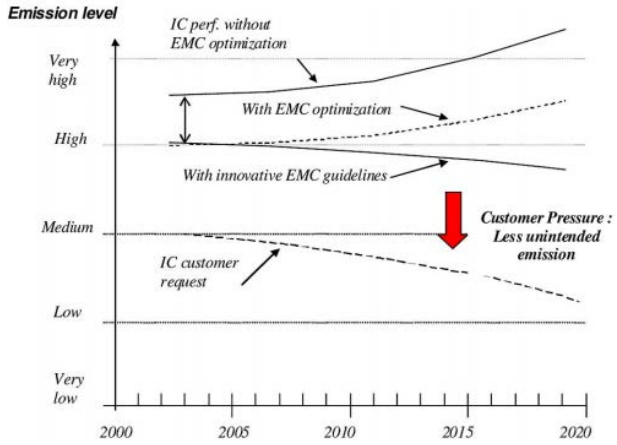

Figure I-7 Evolution of the emission level requirements with the technology evolution [32]

1.2.1.3 Measurement and modelling of electromagnetic emissions

In embedded systems, as automotive or aeronautical applications, the increasing requirement in computing power involves the use of complex and powerful processors. As an example of complex IC, the use of 32-bit microcontrollers clocked by a high-frequency signal, integrating high-speed communication protocols tend to become widespread. The increase in computing power and the communication rate is accompanied by multiple signal integrity problems. The processors, which are essentially synchronous, behave as internal current pulse sources whose peaks can reach considerable values. As a consequence, they produce broadband noise and interference may occur over some frequency bands.

To control the parasitic emission level generated by industrial electronic equipment, there are existing standards for EMC characterization dedicated to the different industrial application fields (e.g. Automotive, Aeronautical and Military) as illustrated in the Table I-2 [28]. These standards provide the necessary guidelines for testing conditions and measurements.

Application field	Standard
Automobile	ISO 7637, ISO 11451/11452, CISPR 25, SAE J1113
Aeronautical	RTCA DO-160-G, EUROCAE ED-14
Military	MIL-STD-461E

Table I-2 Examples of EMC standards for automobile, aeronautic, and military applications

However, at an IC level, manufacturers of ICs are obliged to characterize components at early design stages in order to reduce redesign cost and time-to-market. Thus, EMC compliance has to be taken into account as shown in Figure I-8. The traditional IC design flow consists in verifying EMC compliance after ICs manufacturing with standard measurements. In the IEC standard there are several methods for measuring the conducted and radiated emissions of an IC for a specific frequency band. The Table I-3 summarizes the existing standards for emission measurement. For an EMC-oriented design flow, an efficient modelling and simulation methodology is necessary to ensure a good prediction of EMC level. Also, the standard measurement methods are adapted to characterize and confirm customer EMC requirements.

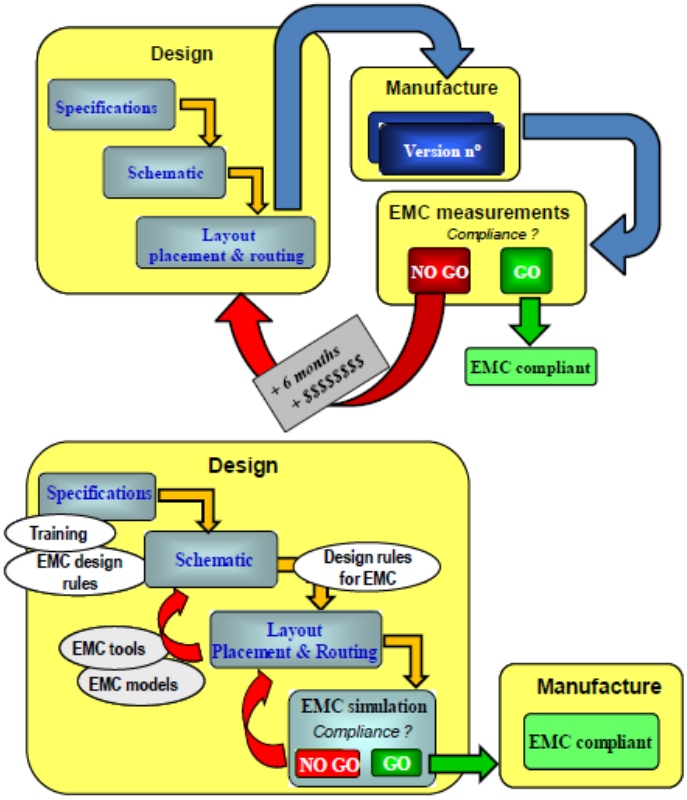

Figure I-8 IC design flow with taking into account EMC compliance in the design (top), taking EMC compliance in the design (bottom) [1]

	Measurement method	Standard
Radiated Emissions	TEM cell (150 KHz – 18 GHz)	IEC 61967-2
	GTEM cell (150 KHz – 18 GHz)	
	Surface scan (150 KHz – 3 GHz)	IEC 61967-3
	IC strip line (150 KHz – 3 GHz)	IEC 61967-8
Conducted Emissions	1Ω/150Ω direct coupling (150 KHz – 1 GHz)	IEC 61967-4
	Work Bench Faraday Cage (150 KHz – 1 GHz)	IEC 61967-5
	Magnetic probe (150 KHz – 1 GHz)	IEC 61967-6

Table I-3 Standards for conducted and radiated emissions measurements at IC level

The study of the 32-bit STXX microcontrollers following the IEC 61967-2 standard has shown that within the IC the main contributor to electromagnetic interference is the flash unit. However, the activation of IOs and the clock tree could strongly contribute to the noise generated by the IC. Following five categorization levels from no EMI risk (Electromagnetic Interference) to high EMI risk, the IC is qualified in term of radiated emissions. The Figure I-9 presents the frequency spectrum of the emissions generated by the flash unit; it shows that the radiated level exceeds the acceptable limits defined by the standard [28]. Hence, integrated circuits qualification is an important concern to manufacturers of IC, it can be complemented by EMI modelling to allow testing different components in order to predict the generated noise and minimize the EMI in an early design phase.

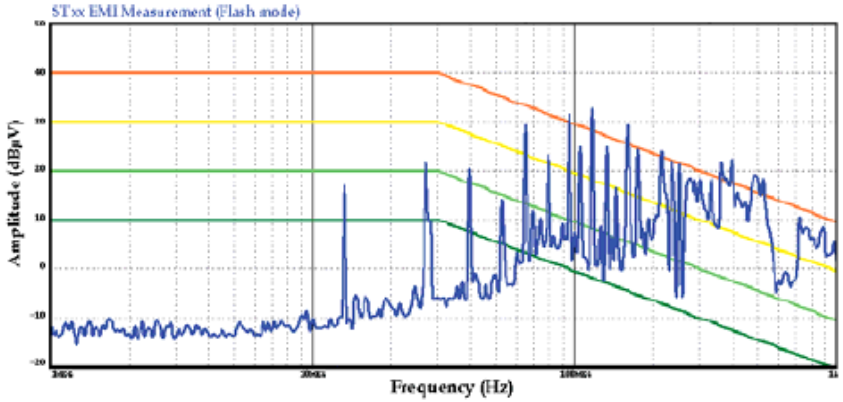

Figure I-9 Emission spectrum of the STXX microcontroller generated by the flash unit [28]

Existing standards allow the construction of electromagnetic emission model of an IC as presented by the Table I-4. The EMI models are used to evaluate the risk of electromagnetic disturbance Dedicated tools and guidelines should be able to predict EMC performance through simulation, in order to avoid the requalification phases and to save time and cost of production.

	IC Model	Standard
ICEM-RE	Integrated Circuit Emission Model – Radiated Emission	IEC 62433-3
ICEM-CE	Integrated Circuit Emission Model – Conducted Emission	IEC 62433-2

Table I-4 IEC standards for EMI modelling at IC level

1.2.2 Electromagnetic susceptibility

1.2.2.1 General overview on electromagnetic susceptibility

The Electromagnetic susceptibility as it is defined by the IEC [26] is the principle that "qualifies the sensitivity of an electrical or electronic device, equipment or system, referred to as a victim, to malfunction or fail in the presence of electromagnetic disturbance". It is important to understand the difference between susceptibility and immunity which have an opposite meaning but they study the same phenomenon. The definition of immunity in the standard [26] is "the ability of an electrical or electronic device, equipment or system to perform without error, loss of performance or degradation in the presence of an electromagnetic disturbance".

Several physical phenomena may be at the origin of the susceptibility of the IC. The continuous stress produced by RF (Radiofrequency) link and the ICs generate electromagnetic field in an environment where sensitive electronic devices are operating. The main sources of electromagnetic disturbance produced by the electronic components, cell phones, radars, and the ICs themselves can cause interference in the surrounding ICs. These electromagnetic aggressions cause functional problems which can lead to the integral deterioration of the IC or alteration of the functioning of an aeronautical system as shown in the Figure I-10.

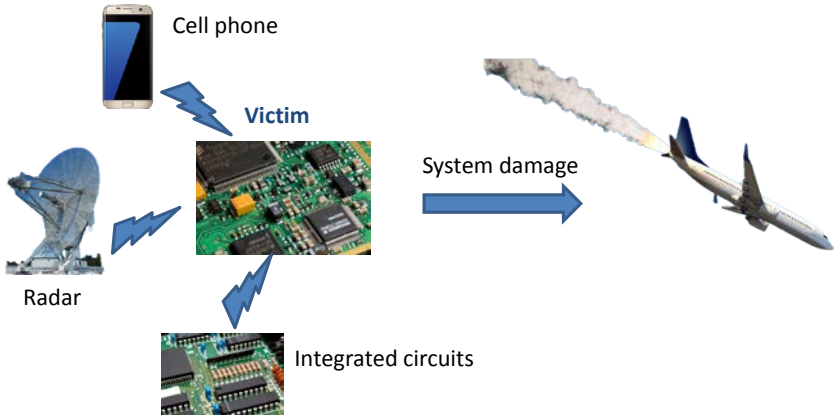

Figure I-10 Susceptibility of ICs in an aeronautical environment

Aggressions can be classified according to their energy levels and the frequency bands where they occur. In some cases, the energy of the generated noise is not sufficient to permanently modify the electrical or technological characteristics of ICs. Hence, the effect of the electromagnetic interference on the IC could be distinguished by two types of failure [28]:

- **Hard failure**: the coupled disturbance exceeds the acceptable limit so far of the IC and generates a permanent damage or the destruction of the circuit.

- **Soft failure**: the coupled disturbance exceeds the acceptable limit of the IC and generates temporary dysfunction of the circuit that is recovered when the disturbance is interrupted or after the reset of IC.

The aggressions coupled to an IC could be classified into three different types of disturbances [30]:

- **Pulse stress**: In digital ICs, the pulse aggression whose duration is at least equal to the response time of the victim circuit propagates within the logic layers and causes additional or premature switching of the internal signals. The switching that occurs from the pulse disturbance can be generated in different ways and can cause various dysfunction; errors in the reception and the transmission of data on the IOs of the IC, errors in the execution of the configuration by a disturbance of the sequencer which can lead to the interruption of the digital IC operation and the loss of the data stored in memory.
- **Continuous stress**: Continuous stress may result from exposure to a high-frequency pulse train that has small amplitude in a sinusoidal waveform and that can be modulated in amplitude. As a consequence of continuous disturbance, the IC noise level increases which can lead to an alteration of the functioning of the component in different ways, depending on the nature of the internal blocks. Since digital circuits are very sensitive to the continuous stress, this disturbance may cause a shift in the supply voltage of the digital blocks, which causes a change in the switching thresholds of the internal elementary logic blocks.
- **High energy stress**: The high energy stress which result from the overvoltage couplings can trigger specific non-linear elements of the IC such as protections against ESD Electrostatic Discharges or clamping between the supply rails. The disturbance could occur through the application of sufficient energy to cause a local heating of the chip. It can generate damage to the oxide grid, inter-metal contacts and even metal interruption by electromigration effect which can cause permanent damage to the IC. The application of a high energy perturbation on a transistor may cause an avalanche effect due to the exceeding of the operating voltage limit at the terminals of the junctions or the channel of the circuit. This phenomenon may either cause premature aging of the transistor with lead to the modification of its electrical characteristics or a destruction of the circuit [31].

1.2.2.2 Impact of technology scaling on electromagnetic susceptibility

The technological improvement of the CMOS circuits and their miniaturization through the reduction of the grid size has increased the sensitivity of the IC to the external perturbations due to the increase of the operating frequency of the digital buses and the reduction of the supply voltage. Hence, the scaling of the transistors forces the manufacturers of the ICs to respect higher immunity margins. The Figure I-11 presents the immunity level evolution with and without EMC optimization and also the IC customer requested level. IC performances without EMC optimization have a very low immunity level that decreases with the technology evolution; the

application of the EMC design rules allows the increase of the immunity margin but the IC customer requirements stay higher.

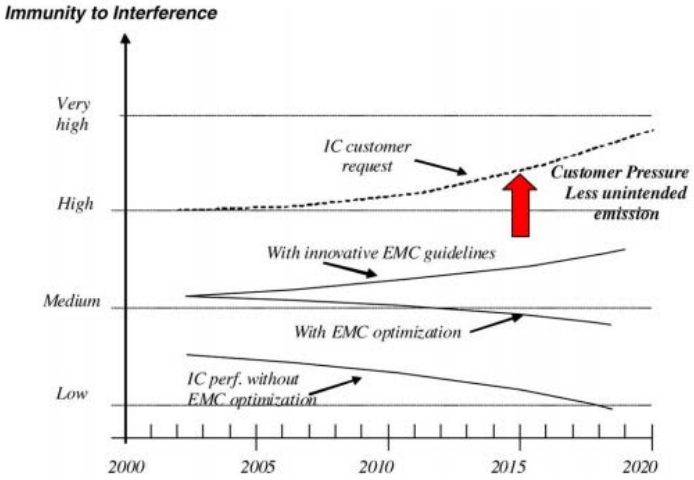

Figure I-11 Evolution of the immunity level requirements with the technology evolution [32]

The reduction of the power supply of the ICs tends to reduce the noise margins and the switching thresholds of the digital circuits, which makes the circuits very sensitive to electromagnetic interferences. When the noise margins are exceeded, static errors can be generated such as the change in the signal logic states. If the level of the disturbance is high enough and allows exceeding the switching threshold, the circuit considers it as a logical state change. It can be induced by a direct coupling of the disturbance on the IOs or on the power or ground pins. If the superimposition of the input signal and the disturbance is greater than the switching threshold, then critical changes may occur in the logic state of the output of the circuit [30].

Furthermore, the increase in operating frequencies of ICs has a very important impact on susceptibility. The digital circuits are characterized by a delay margin in order to avoid the loss of synchronization or the appearance of undesirable states (glitches). The increase of the operating frequency of the IC means the decrease of the switching period which leads to a reduction in the delay margin. This induces many design constraints for synchronous circuits. A disturbance which is not sufficient to modify the logic state can still cause a dynamic error; the conducted disturbance at the power supply rails may be at the origin of additional propagation delays on the signals. The effect of the disturbances can desynchronize these signals and the clock, by advancing or delaying the appearance of clock edges, leading to the appearance of logical errors [33].

1.2.2.3 Measurement and modelling of electromagnetic susceptibility

The manufacturers of the ICs must characterize the susceptibility level of the components before their marketing to ICs end-users in order to guarantee low susceptibility level. Hence, existing measurements techniques in the IEC 62132 standard [34] allow qualification test of ICs to avoid high sensitivity level to radiated and conducted disturbance, as shown in the Table I-5 Standards for conducted and radiated susceptibility measurements at IC.

	Measurement method	Standard
Radiated susceptibility	TEM cell (150 KHz – 1 GHz)	IEC 62132-2
	GTEM cell (150 KHz – 1 GHz)	
	Surface scan (150 KHz – 1 GHz)	IEC 62132-9
	Bulk Current Injection BCI (150 KHz – 1 GHz)	IEC 62132-3
Conducted susceptibility	Direct Power Injection DPI (150 KHz – 1 GHz)	IEC 62132-4
	Work Bench Faraday Cage (150 KHz – 1 GHz)	IEC 62132-5

Table I-5 Standards for conducted and radiated susceptibility measurements at IC

Digital circuits are very sensitive to RF interference. For example, the application of the DPI measurement method allows testing immunity level of an IC to a continuous disturbance. The method relies on a capacitive coupling principle with the injection at the component pin of necessary RF power to set off a loss of functionality at a specified frequency. The Figure I-12 presents the immunity level of two different LDOs TLE4275GV33 and NCV4275A3 on the frequency band 20 MHz – 400 MHz with NRESET < 1V as immunity criteria, and it shows that the circuit is very sensitive to the DPI around the frequencies 100 - 300 MHz . Thus, it is important to study the susceptibility of ICs in order to make the necessary improvements.

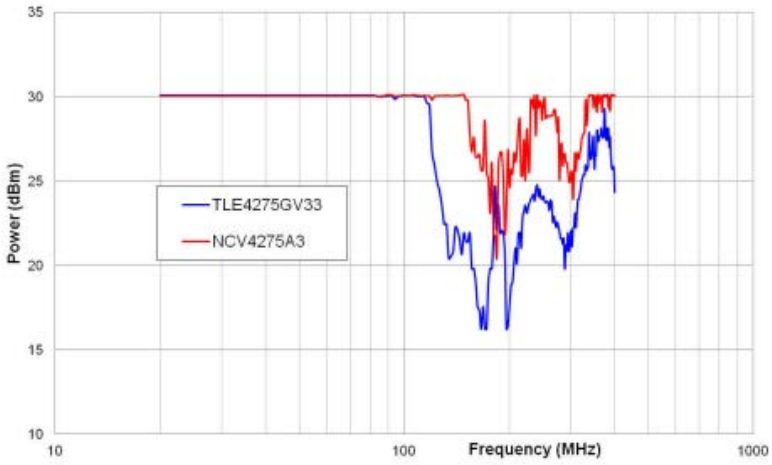

Figure I-12 Immunity level of two different LDOs [68]

These measurements methods are useful for the construction of immunity models. In the design phase of an electronic system, the integrated circuit equivalent model validates the component compliance before manufacture. The IC immunity models must be able to predict the susceptibility level to interference. Modeling approaches are discussed within the international committee IEC which has proposed models to characterize the conducted immunity as presented in the Table I-6. However, a considerable effort is needed at the research level to provide appropriate methodologies for the prediction of radiated immunity of ICs.

	IC Model	Standard
ICIM-RI	Integrated Circuit Immunity Model – Radiated Emission	IEC 62433-5
ICIM-CI	Integrated Circuit Immunity Model – Conducted Emission	IEC 62433-4

Table I-6 Standard for IC immunity modelling

2. Integrated circuits reliability issues

2.1. Introduction

As it is commonly defined, the reliability is the ability of a system or component to perform its required functions under stated conditions for a specified period of time. For several years, reliability has become a major factor influencing the development of ICs. The increasing complexity of technologies makes the susceptibility of circuits to the environmental constraints more difficult to manage in terms of robustness; thus, the required reliability levels in most applications are extremely high. Reliability is an indicator of the quality of the ICs over a defined period; for an IC, the reliability is expressed in FIT (Failure In Time) which the unit is 10^9 hours per device: The FIT expressed for a given IC population how much failures appeared during a certain time. The FIT is a statistical data and not a physical one. 1 FIT means that 1 failure occurred on one device during 10^9 hours which is senseless or that 1 failure occurred on 1 000 devices during 10^6 hours. In the AEC Q-100, electronics suppliers require from components manufacturers' results on 100 000 parts minimum.

To quantify the reliability of a component the MTBF (Mean Time To Failure) is used for most semiconductors standards and concern the irreversible failure. For a constant failure rate λ, the MTTF is given by the expression I-1:

$$MTTF = \frac{1}{\lambda} \tag{I-1}$$

In the 1950s, the Advisory Group for Electronic Reliability of Electronic Equipment (AGREE) has demonstrated that the failure rate of electronic equipment is similar to the mortality rate of people in a closed system. They noted that the failure rate of electronic components and systems follows a bathtub curve as shown in the Figure I-13.

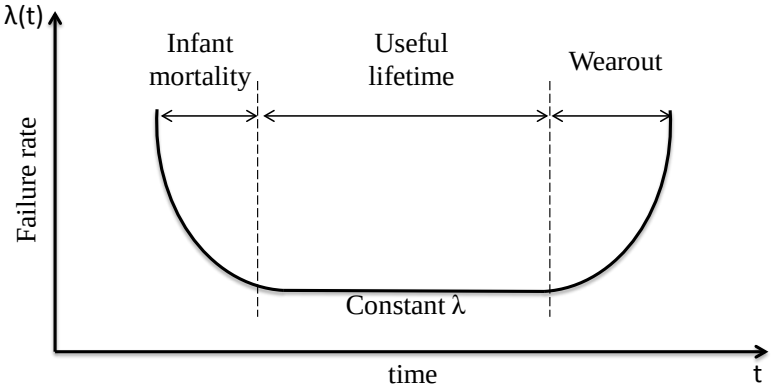

Figure I-13 Bathtub curve

The bathtub curve represents the three stages of evolution of the failure rate in time for an electronic system or component:

- **Infant mortality**: The infant defects appear in the first period of the life of an electronic system or component. They are due to defects related to the circuit design and/or the technological process. The failure rate decreases in this period until the component reaches a level of maturity which allows a constant failure rate. A method based on burn-in test is generally used required by the suppliers to the components manufacturers to eliminate these infant defects under well-defined thermal and electrical stress conditions for a very short time.
- **Useful time**: The operating life of an electronic component knows the appearance of random defects linked to random stress conditions (e.g. ESD: electrostatic discharges). In this period the appearance of the defects follows an exponential law which allows having a constant failure rate. Reliability studies have to reduce the frequency of occurrence of the operating life defects.
- **Wearout**: The failure rate increases more rapidly over time; the defects occur more frequently. This phase is due to the critical wearout of electronic components. The technological node, the manufacturing process and the temperature and voltage conditions are the main contributors to the wearout phase.

Industrial applications (aeronautics, space, automotive, military, etc.) have strong demands on the quality of the electronic systems and components. The reliability must be verified to ensure the correct functioning of the components during the operating life. The biggest advances in the technology process are made in the commercial industry such as the increase in computing power, the capacity of the memories... Thus, the industrials perform a strong integration of Commercial Off The Shelf (COTS) components. However, the limitation of the operating temperature range, as shown in the Table I-7, raises problems of reliability.

Industrial application	Temperature range
Space, Military	-55°C – 125°C
Industrial	-40°C – 85°C
Commercial	0°C – 75°C

Table I-7 Operating temperature range of COTS components in industrial application [36]

2.2. Impact of technology scaling on the long-term reliability of ICs

As a primary consequence of transistors scaling, the DSM circuits fault sensitivity increases, hence, the long-term reliability has become an important constraint for manufacturers of integrated circuits. Miniaturization can lead to the appearance of infant mortalities that are difficult to trap using the screening. The devices could have a premature impact of a degradation mechanism leading to a sharp reduction of the lifetime. Scaling impact on degradation mechanism of digital devices has been a hot topic during the last years [3]; and it has been proved in previous studies that some degradation mechanisms have their contribution on the speed degradation of digital circuits [20]. As for example, a decrease of the delay was noted for a FPGA (Field Programmable Gate Array) [21], and for the operating voltage, as the SRAM minimum

voltage shift [22]. The reliability experts states that scaling can lead to earlier failures than for older technologies as shown in the Figure I-14 where the failure constant in the bottom of the bathtub curve seems to increase with the transistors scaling. This trend results in earlier wearout failure and a very short lifetime of devices.

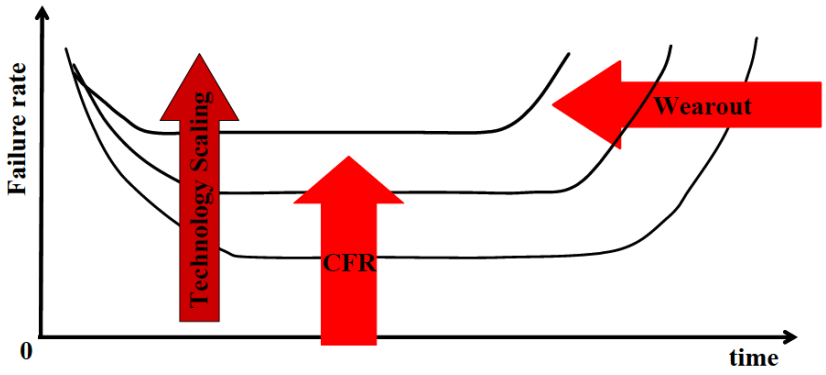

Figure I-14 Evolution of the bathtub curve with the technology scaling [3]

Figure I-15 presents the trends of power supply and threshold voltage (V_{DD} and V_{TH}) and gate oxide thickness according to the CMOS channel length evolution. The negative effect of scaling on the reliability is also related to the non-ideal scaling [38]. Indeed, the power supply does not decrease as rapidly as expected because the difference between the threshold voltage and the power supply is reduced, leading to a high sensitivity to noise. Hence, the reduction of the threshold voltage leads to the increase of the current leakage and therefore the power leakage.

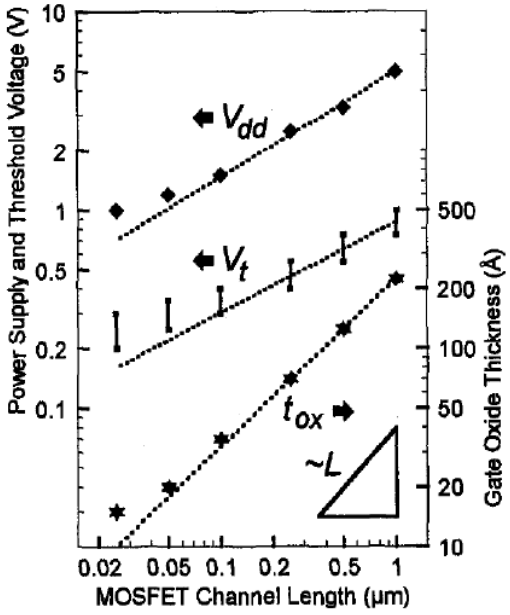

Figure I-15 Trends of power supply and threshold voltage and gate oxide thickness with the evolution of CMOS channel length [23]

The increase in power leakage depends exponentially on the temperature which leads to very high temperatures. The Figure I-16 shows the effect of miniaturization on the reliability of 180 nm processors to 65 nm. For several applications running in processors with a specified CMOS

technology, the temperature increases considerably, and in parallel the reliability decreases with transistors scaling, this is represented by the Mean Time To Failure (MTTF) calculated on the basis of the worst case of current density and temperature [39].

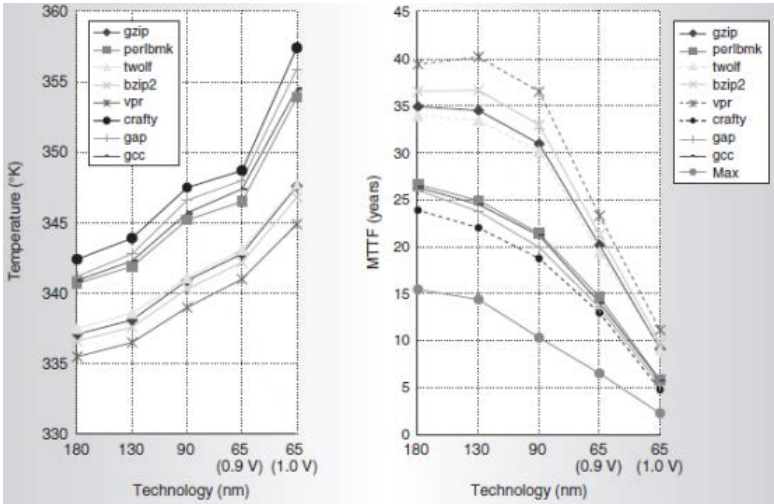

Figure I-16 Maximum temperature reached for different structure (Left), MTTF evolution with the technology scaling (right) [39]

2.3. Degradation mechanisms

During their lifetime, CMOS devices are affected by specific degradation mechanisms that lead to the wearout of electronic devices. However, it is necessary to distinguish the two primary classes of mechanisms:

- **The intrinsic mechanisms**: due to internal causes of the IC, inherent to the design and the materials used. To limit them, it is necessary to remain in areas of limited operation.
- **The extrinsic mechanisms**: due to an external cause during the manufacturing process or the operation

Only the intrinsic mechanisms will be addressed in this manuscript, a detailed presentation will concern the degradation mechanisms presented in the Figure I-17: Electromigration (EM), Time Dependent Dielectric Breakdown (TDDB), Hot Carrier Injection (HCI) and Negative Bias Temperature Instabilities (NBTI), their activation depend on the environmental conditions as the temperature and the power supply voltage and the current density. All these degradation mechanisms are described in JEDEC JEP112G « Failure Mechanisms and Models for Semiconductor Devices ».

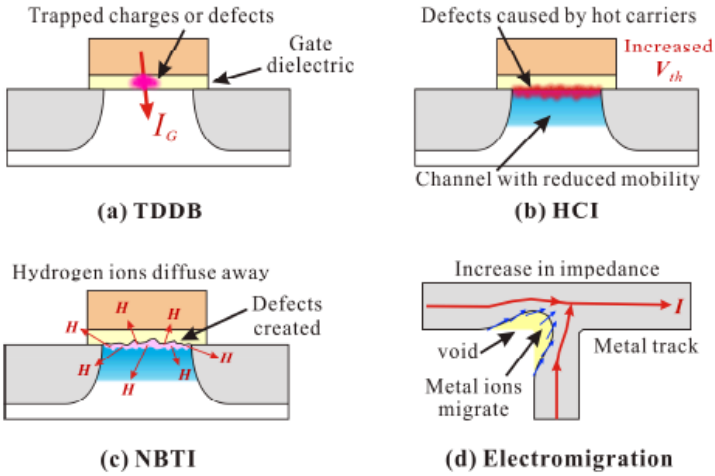

Figure I-17 Illustration of the degradation mechanisms: TDDB, HCI, EM, NBTI [24]

2.3.1 Electromigration

2.3.1.1 Overview on electromigration mechanism

Electromigration is a failure mechanism that affects the wiring on microelectronics circuit. The metallization is induced by the wiring used for the interconnections inside a circuit chip; it insures the routing of the signals, the power and the ground planes inside a circuit chip. An on chip metallization failure can be depicted by four phenomenons [40]:

- **Open-circuit and short-circuit failures**: These defects are generally due to the discontinuities in the signal lines or the leakage of power in the surrounding lines.
- **Elevated resistance failure** : The increase of the resistance leads to a delayed signal which causes timing defects
- **Leakage failure**: The current leakage can lead to the reduction of the threshold voltage needed to trigger the circuit.

The degradations generated by the electromigration mechanism are relatively related to the microstructure of the metal of tracks. Thus, the metal of the interconnection tracks of the ICs generally consists of juxtaposed grains considered as monocrystalline with random orientation. These grains themselves have dislocations which behave differently regarding to electromigration.

Electrical failure for most macroscopic applications occurs when applied currents are high enough to cause wires to overheat and burn out. The same phenomenon can also occur in microscopic environment, but because the wiring is embedded in a hard dielectric (SiO2) and attached to a thermally conductive Si substrate, the power dissipated in the wire is rapidly conducted away and the wiring is kept from burning out until much higher densities are reached. As a consequence of the higher current density in chip metallization is the phenomenon of Electromigration (EM), which is the movement of the metal atoms (Al, AlCu, Cu) in response to an applied current.

The electromigration mechanism is represented by different types of diffusion as shown in Figure I-18, it is recognized that diffusion at the upper interface dominates the transport of atoms but some researchers justify a reduction in the lifetime of large lines by a contribution of grain boundaries [41]. This lifetime reduction is confirmed by an increase in the activation energy, which is the necessary energy to go from an initial state (good device) to a final state (failed device). In general, the migration in the grain boundaries (whose crystal structure is more regular) is the slowest. The overall speed of electromigration is therefore strongly conditioned by the microstructure of the material, as well as by its surface state.

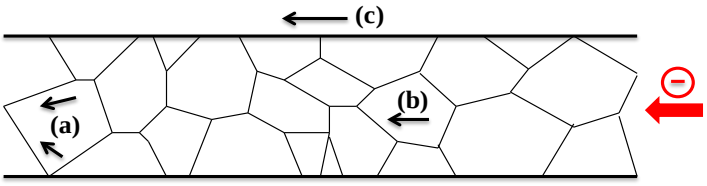

Figure I-18 Illustration of various diffusion processes within the lattice of an interconnection: (a) grain boundary diffusion, (b) bulk diffusion, and (c) surface diffusion

The first aspect of failure identified is the creation of voids [42]. The appearance of these voids is due to the shrinkage of atoms in the metal tracks. This effect is the most frequent cause of breakdowns. In fact, the local absence of metal leads to an increase in the resistance of the track or even to an open-circuit. The track loses its functionality partially or totally. The Figure I-19 shows voids created on a CMOS structure induced by electromigration at the interconnection tracks.

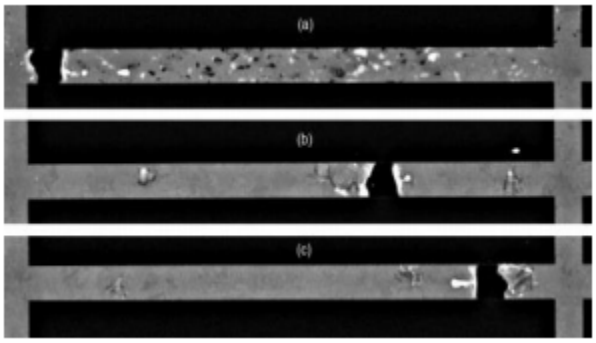

Figure I-19 Voids induced by electromigration in the metallization of interconnections and vias [43]

2.3.1.2 Physical analysis of electromigration

The general approach to Electromigration reliability involves the sampling, accelerated testing, data analysis, projection of failure rates to use conditions and specification of current densities allowed under use conditions in order to meet specified rate criteria.

An empirical relationship known as Black's law (I-2) is usually used to describe the failure induced by Electromigration:

$$t_{50} = \frac{A}{j^n} e^{\frac{\Delta h}{kT}} \qquad \text{(I-2)}$$

Where t_{50} is the MTTF (Mean Time To Failure at which 50% of the population has failed), n is the current density (j) exponent, and A is a constant. Δh is the activation energy for diffusion in eV.

The methodology of describing the electromigration reliability must be analyzed with a statistical approach. If we study a large number of samples, not all parts fail at exactly the same time; the TTF is expected to be close between the samples but a distribution will still exist. Several statistical distributions can be applicable to describe failure times, and three are most commonly used for electromigration wearout: normal distribution, lognormal distribution and Weibull distribution.

2.3.1.3 Impact of technology scaling on EM

With the scaling of the CMOS transistors, line widths will decrease over the years [41]. This has a considerable impact on the current which decreases as shown in Figure I-20 because of the decreased power supply voltage and the reduction of the gate capacitance. However, the increase in the frequency of the ICs will lead to the current density J increase. Since the maximum tolerable current density is reduced with the scaling, the ITRS [27] indicates that the minimum sized interconnections will be impacted by the mechanism of electromigration in the coming years as shown by the yellow barrier of the Figure I-20.

The increase of the interconnections resistivity caused by the scattering effect in the small wires presents more constraints regarding to electromigration. Furthermore the increase in the current density leads to the increase of the temperature gradient in interconnections caused by Joule heating [44].

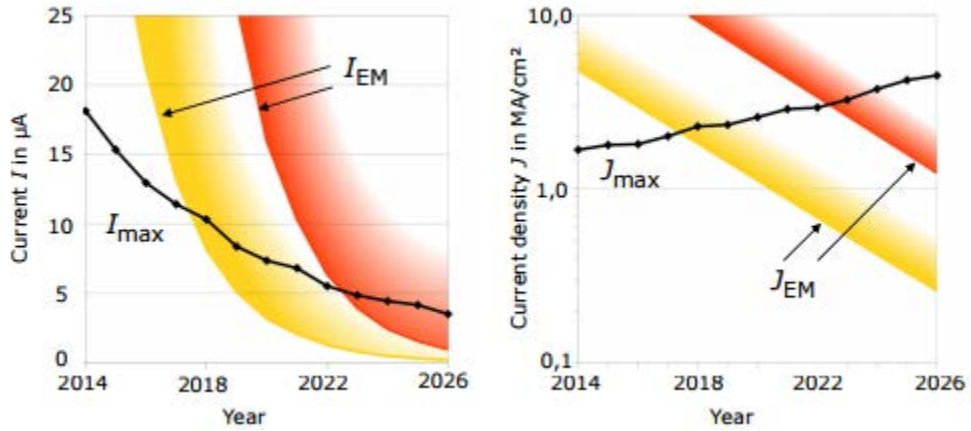

Figure I-20 Expected development of currents (left) and current densities (right) needed for driving four inverter gates, according to ITRS 2011 [27]. EM degradation needs to be considered when crossing the yellow barrier of currents (I_{EM}) and current densities (J_{EM}). The solutions are not known in the red area

2.3.2 Hot Carrier Injection

2.3.2.1 Overview on HCI mechanism

The generation of hot carriers is a phenomenon that has emerged as the size of the transistors decreases. Indeed, the ratio between the gate length size of the transistor and the power supply voltage is not constant over the technologies and the electric fields across the channel are

increasingly strong, in order to conserve ICs performance in terms of sufficient switching frequency and low static consumption.

The phenomenon of hot carrier injection exists in both the NMOS and PMOS transistors. A hot carrier refers to a carrier which has been accelerated by a strong lateral electric field. This phenomenon is the most important as the channel lengths and the oxide thicknesses are reduced. Thus, this phenomenon appears more often inside digital circuits than analog circuits, for which miniaturization is a real challenge to improve performances in terms of switching frequency.

Carriers (electrons or holes) can get large kinetic energies from transit through regions of high electric field. This energy is able to increase due to several mechanisms. The carriers are called "hot" because they were historically assumed to be thermally distributed at an effective temperature higher than that of the lattice. Hot carriers can gain enough energy to be injected into the gate oxide or cause interfacial damage introducing instabilities in the electrical characteristics of a MOSFET device, Figure I-21. HC can be generated in several ways and in different regions of the devices; in gate oxide (produced by an avalanche process induced by large gate oxide electrical fields or high energy radiation), silicon substrate (produced by optical illumination or by the substrate electrical fields assisted injection) or at Si/SiO_2 interface of the channel. These defects then lead to threshold voltage shifts and transconductance degradation of MOS devices.

Channel Hot Carrier (CHC) effects are generated in the MOSFET channel regions under channel conduction conditions similar to applications in ICs.

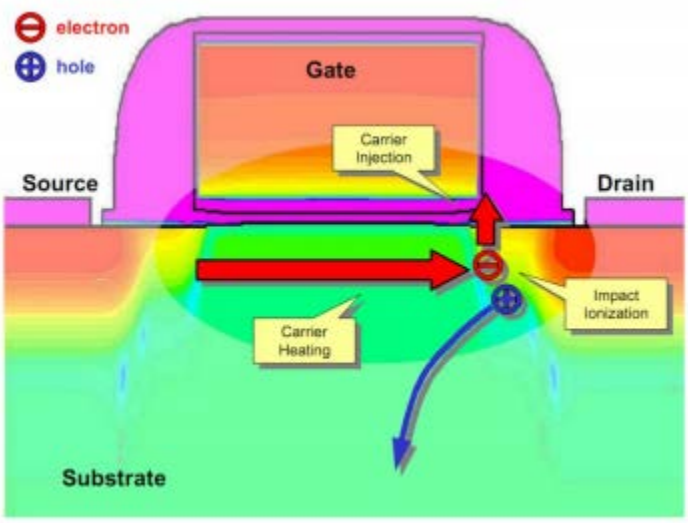

Figure I-21 Impact ionization in the vicinity of the drain caused by a hot carrier [43]

The HCI mechanism is triggered due to the phenomenon that generates and injects hot carriers:

- **Drain Avalanche Hot Carrier (DAHC)**: Due to the strong lateral electric field in MOSFET, the channel carriers generated by the source are strongly accelerated; the carriers gain energy that is yield to the atoms of the crystal lattice during the collisions, if this energy is higher than the ionization energy, then there is generation of electron-hole pairs which instantaneously dissociate. The primary ionization occurs near the drain which collects the electrons and pushes the holes towards the substrate. A number of electrons can be injected into the gate. Carrier trapping in the oxide is the cause of

degrading the oxide. If the voltage of the gate V_G is nearly equal to half the drain voltage $V_D/2$, then the maximum surge current condition arises. This phenomenon causes the most degradation for normal temperatures. The DAHC injection mechanism is presented by the Figure I-22.

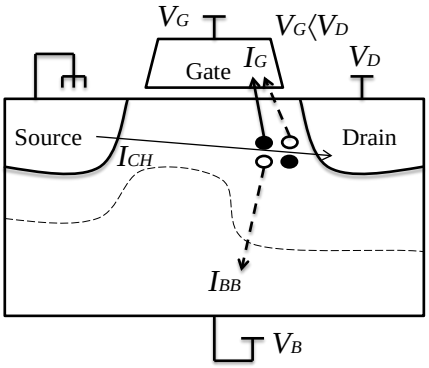

Figure I-22 Drain Avalanche Hot Carrier (DAHC) mechanism

- **Channel Hot Electron (CHE)**: in the vicinity of the drain, an area of intense transverse electric field, and provided that they have acquired sufficient energy during their passage in the channel, electrons can cross the Si/SiO_2 energy barrier and be directly injected into the front gate oxide as shown in Figure I-23. These electrons form the basis of the creation of a gate current and their action is maximum when the gate voltage V_g is equal to the drain voltage V_d.

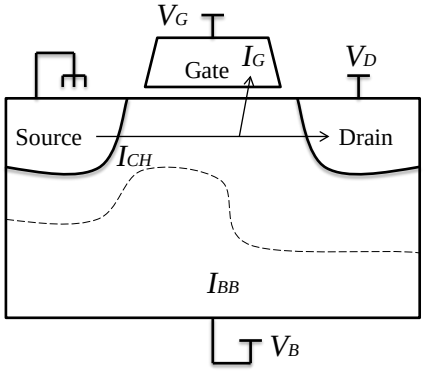

Figure I-23 Channel Hot Electron mechanism

2.3.2.2 Induced degradations by the HCI

The hot carriers injection modifies the static I(V) characteristics of the MOS transistors. The Figure I-24 shows the degradation of the electrical parameters of the NMOS transistors for different dimensions (length and width of the channel) of the stress time. In this study, the impact of HCI degradation on the drain current is manifested by a reduction in the saturation current when the stress time increases.

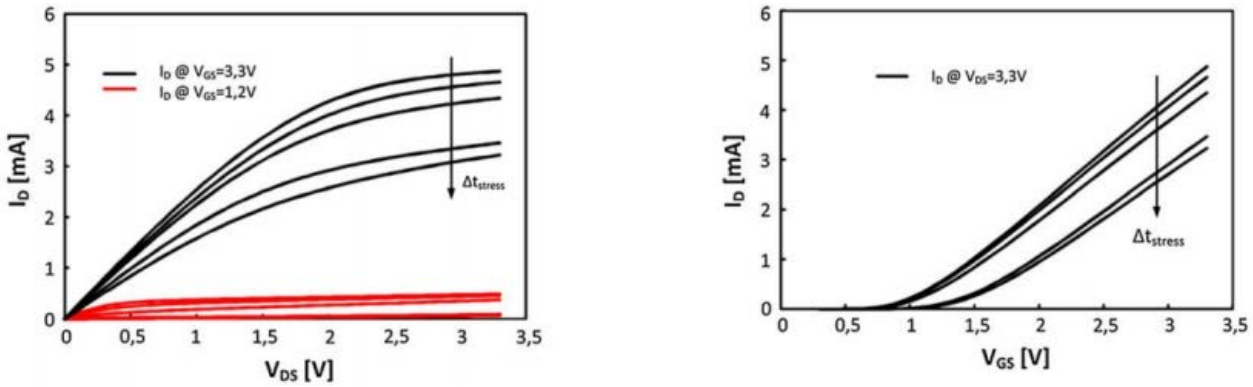

Figure I-24 Characteristics of transfers of the drain current with respect to the variation of the gate voltage (Ids / Vgs) (a), with respect to the variation of the drain voltage (Ids / Vds) (b)

These characteristics are used to extract the variation of the threshold voltage of the NMOS transistors. This threshold variation is more significant for transistors with high operating voltage and a short channel length than for other types of NMOS.

The sensitivity of the components to the effects of hot carriers varies with temperature, but it is not by increasing the temperature that the degradation is worse. The increase in temperature has rather the effect of limiting the damage due to the hot carriers. Indeed, at high temperatures, the number of hot carriers is reduced because the saturation length of their velocity is itself reduced.

In addition, the mean free path of the majority carriers is also reduced and the impact ionization process is less effective when the temperature is high.

2.3.2.3 Scaling impact on HCI

As the CMOS technology scaling allows the reduction of the geometrical dimensions of the transistors, this has a direct impact on the degradations induced by the HCI mechanism. This is related to the MTTF expression given by the Equation I-3; thus, the HCI strongly depends on the channel length at constant supply voltage.

$$MTTF_{HCI} = A \cdot L_{eff} \quad \text{(I-3)}$$

Where A is a constant, and L_{eff} the channel length. The channel length dependency can be derived from the modification in the Lucky Electron Model (LEM). The LEM states that the channel carrier has enough energy to create hole-pairs; thus, only the interface states are responsible for the degradation induced by hot carriers, the traps in the volume are not taken into account. The interface states are generated by the channel energetic electrons which are “lucky” enough not to lose all their kinetic energy due to the collisions on dopant impurities by electron-phonon diffusion that reaches a threshold energy of 1,3 eV which trigger the impact ionization. For a pinch-off potential value V_{dsat}, the drain potential V_{ds}-V_{dsat} and a gate thickness, the impact by ionization rate α is given by formula (I-4) [56].

$$\alpha = e^{\frac{-1}{V_{ds}-V_{dsat}}} \quad \text{(I-4)}$$

According to the expression of the LEM model, the rate of impact by ionization is independent of the gate length for a constant value of $\frac{-1}{V_{ds-V_{dsat}}}$. However, with the miniaturization of the transistors, the rate α increases due to the energy gain by the drain field and the channel electric field, i.e the electric field between the edge source and the pinch-off region. The drain field is independent of the channel length but the channel electric field E_{ch} increases with the decrease of the effective channel length L_{eff} II-5.

$$E_{ch} = \frac{V_{ds}-V_{dsat}}{L_{eff}} \quad \text{(I-5)}$$

The Figure I-25 shows the evolution of the impact ionization rate following the gate length and the oxide thickness.

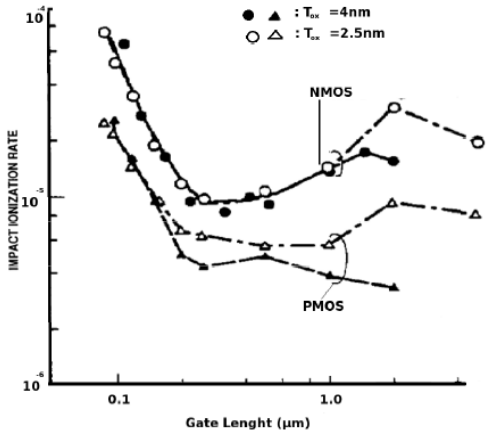

Figure I-25 Effect of the oxide thickness and the gate length on the impact ionization rate [56]

2.3.3 Time Dependent Dielectric Breakdown

2.3.3.1 Overview on TDDB mechanism

The TDDB mechanism is related to the integrity of the gate oxide. It is a phenomenon of parameter drift followed by the sudden breakdown of the gate oxide due to the creation of a conductive path through the oxide which leads to the rise of the gate conductance. The latter can then lead to the destruction of the oxide and to a failure of the circuit. The TDDB depends on the number of defects in the oxide created during manufacturing. It remains independent of the polarization conditions, but depends on the current density which will flow through the gate oxide by the tunnel effect.

When the electrons have crossed the potential barrier of the oxide they are accelerated by the vertical electric field which depends on the applied voltage and the oxide thickness. For DSM technologies, when an oxide thickness is less than 2 nm, the electric field can reach 4 to 5 MV/m. The oxide is able to support fields of more than 10 MV/m without reaching the breakdown. Nevertheless, the energy provided by these charges can locally break the chemical bond Si/SiO_2 and create interface traps. These modify the properties of the channel and help to reduce the mobility of the carriers in the channel. Moreover, the trapping of these charges can increase the electric field locally and increase even more the electron current by tunnel effect. Therefore, there

is a kind of feedback effect that accelerates the process of degradation. The destruction occurs only when a real hole has been created through the oxide and a strong current can pass, creating a short circuit at the grid and the substrate. The leakage current induced by strong electric field stresses through thin gate oxides is not really a problem for the functionality of the circuit as long as it remains low. Nevertheless this is a real problem for reliability.

The TDDB mainly concerns dielectric layers. The degradation induced by the TDDB begins when the traps are formed at the Si/SiO_2 interface. This trap formation strongly depends on the conditions of polarization and the applied stress. Firstly, traps density is relatively small; in this case no conduction path can exist as shown in Figure I-26 (a). Then, as the traps generation increases, the traps begin to overlap forming a conduction path between the substrate and the gate of the MOSFET, thus degradation of the dielectric begins. This type of degradation is commonly known as Soft Breakdown (SBD), it is represented by Figure I-26 (b). Once the conduction path formed by the new traps is created by thermal degradation, see Figure I-26 (c). Finally, the conductance increases roughly, resulting in a localized rupture on the gate dielectric of the MOSFET, this type of failure is called Hard Breakdown (HBD), it is represented in Figure I-26 (d).

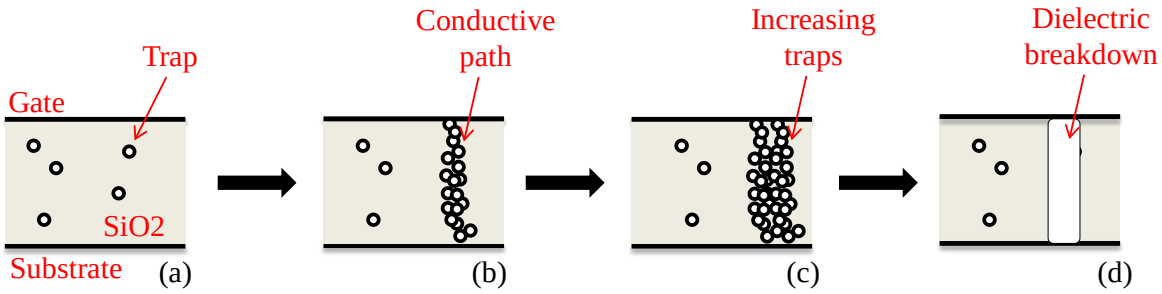

Figure I-26 Steps of creation of the degradations in the dielectric of a MOSFET generated by the TDDB mechanism

2.3.3.2 Induced degradation by the TDDB mechanism

The SBD is associated with the formation of a temporary conduction path in the dielectric. This path allows a discharge of the gate potential as well as a dissipation of the stored energy. This dissipation of energy causes the fast rise in temperature of the dielectric which can be followed by a phase of total or partial healing of the degradations suffered. Several SBDs can be observed before the HBD occurs. The SBD often appear a few microseconds after the application of the stress; the observation of this degradation requires the use of a measuring device faster than those used for HBD. Figure I-27 shows an SBD acquired by a digital oscilloscope [46].

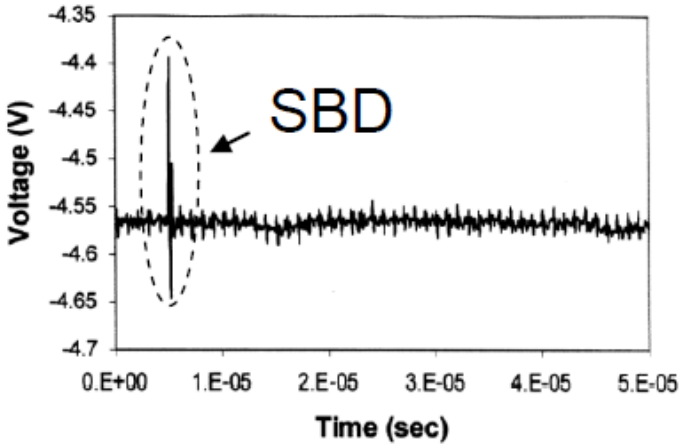

Figure I-27 Appearance of an SBD on the gate voltage [46]

These results show the rapid appearance of the failure induced by the SBD on the gate voltage. In fact, the SBD occurs with a significant variation of the gate voltage for a very short time, which recovers its initial value very quickly. The appearance of dislocations caused by the SBD varies with the surface of the dielectric. Thus, for components with a large dielectric surface, the effect of the SDB is less visible due to the leakage current magnitude. The SDB results in a slight increase in this leakage current.

The HBDs and the SBDs can be distinguished by the current that passes after the incident and the failure generated. Sometimes, an HBD does not lead to destruction of the circuit. The HBDs are characterized by a strong change in gate voltage or gate current during a stress, while the SBDs are characterized by a small offset of the DC characteristics. A HBD is characterized by a linear relationship between the current and the gate voltage (I_G and V_G), while an SBD has an exponential relationship between the same parameters. However, for small oxide thicknesses, changes on V_G or I_G are no longer very important and the noise on I_G or V_G becomes a good criterion for detecting a SBD. The Figure I-28 gives a presentation of the breakdown on the gate voltage for different oxide thickness [47].

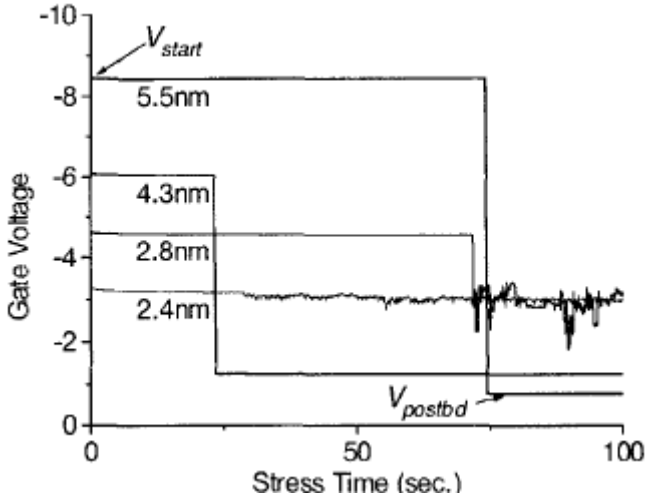

Figure I-28 Breakdown on the gate voltage for different oxide thickness [47]

HBDs are uncommon than SBDs for small oxide thicknesses and for nominal voltage and current levels. For advanced technologies, the main degradation problems concern the SBD. However, the SBDs lead to a very slight degradation or drift of parameters of a MOS transistor such as transconductance and threshold voltage.

In some cases, even if the characteristics of the transistors are impacted by the TDDB, it is possible that the SBDs do not necessarily hinder the functioning of a circuit and the HBDs may not cause a complete circuit failure. For example, in [48] a ring oscillator programmed with a 0.18 µm transistors is stressed by an overvoltage stress, after several HBDs on some logic gates, the circuit continues to function properly. Only parameters such as the quiescent current, operating current and the operating frequency change. Even if the variation is very small, researchers believe that the drift could be higher when several logic gates are impacted, generating timing issues within the circuit.

2.3.3.3 Scaling impact on TDDB

Scaling has a considerable impact on the reliability of the gate oxide. The temperature and the electric field accelerate the TDDB mechanism with the reduction of to the oxide thickness. Depending on the gate voltage and the oxide thickness, different types of current flow in the oxide and these currents have different dependencies on the electric field [49]. For reduced oxides size, the dependence is linear with the electric field. The leakage current through the Si/SiO_2 barrier that raises the gate current is due to a Fowler-Nordheim tunnel effect for strong fields, while for an applied power supply voltage less than 3V there is a direct tunnel effect. In order to reduce the leakage current in the gate without reducing the performance of the transistors in terms of operating frequency, the introduction of High-K material has been proposed. They are mainly manufacture with HfO_2 process. It is possible to increase the oxide capacitance C_{ox} while increasing the thickness of the dielectric. However, new problems appear as electron trapping in the oxide for positive grate voltages, which increases with the oxide thickness reduction because statistically the induced degradations are more numerous [50]. This trapping modifies the threshold voltage V_{th}.

The equation (I-6) allows calculating the MTTF for the TDDB mechanism [38]; it shows the drawback of the increase of the temperature and the advantage of the power supply voltage reduction. Thus, the reliability of the circuits decreases with the reduction of the gate oxide thickness due to the increase of the leakage current in the gate and the tunnel effect. Since the $MTTF_{TDDB}$ is inversely proportional to the total surface area of the gate oxide, when the oxide thickness is reduced by ε_{ox} (nm) for the new technologies, the leakage current due to a direct tunnel effect is multiplied by 10, so the MTTF is reduced by $10^{\frac{\varepsilon_{ox}}{0,22}}$ [51].

$$MTTF_{TDDB} \propto \left(\frac{1}{V}\right)^{a-bT} . e^{\frac{(X+\frac{Y}{T}+ZT)}{kT}} \quad \text{(I-6)}$$

Where T is the absolute temperature in (K), a, b, X, Y and Z are fitting parameters and V is the voltage.

1.1.1 Negative Bias Temperature Instabilities

2.3.3.4 Overview on NBTI mechanism

The Negative Bias Temperature Instabilities (NBTI) mechanism appears when the transistors gate is stressed with a negative potential and high temperature while the drain, source and the substrate are connected to the ground. As shown in Figure I-29, the NBTI phenomenon involves the breaking of the Si-H bond when applying an electrical stress. This dissociation gives rise to interface traps and hydrogenated entities which are diffused through the oxide. The applied voltage varies from 2 to 3 times the nominal power supply voltage, and the temperature ranges varies between 25 and 200°C, so as not to deteriorate the chemical structure of the device. This phenomenon mainly degrades the PMOS transistors. It is strongly related to the oxide thickness and the channel length; it causes a charge trapping at the silicon oxide interface which leads to a drift of the threshold voltage, the mobility of electrons and the reduction in the drive currents I_{on}. The drift of the threshold voltage related to the NBTI is more severe for the advanced technologies because the power supply voltage and the oxide thicknesses are reduced.

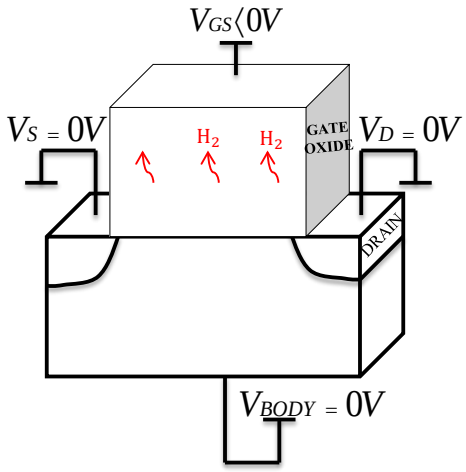

Figure I-29 Electric configuration of the NBTI mechanism activation

The NBTI degradation is generally modeled with the Reaction-Diffusion (RD) model. This model suggests that the degradation of PMOS transistors due to NBTI follows a power law. RD is accepted as one of the best models describing the defects generation mechanism at the Si/SiO_2 interface.

The RD model can be decomposed into five stages; the first stage concerns the outset of stress, this phase is dominated by the breaking of the Si-H bonds, during the second stage the dissociation and recombination reactions are balanced. The third stage is very short, it is controlled by the diffusing hydrogen, and then during the fourth stage the hydrogen reaches the oxide/poly interface of the gate. Finally, in the last stage, when the Si-H bonds are all dissociated no further degradation can occur. This saturation condition rarely occurs and requires extremely long stress or very high stress conditions that would lead to other degradation mechanisms that precede this stage (TDDB). The Figure I-30 presents the stages of the RD model depending on the number of interface states generated by Si-H bond failure at the instant t.

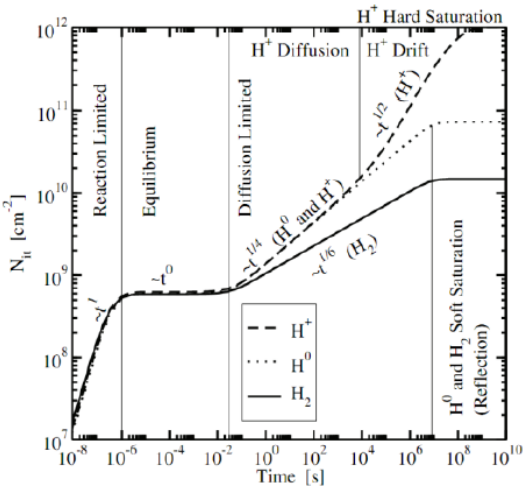

Figure I-30 Illustration of the five stages of a RD model

2.3.3.5 Induced degradation with the NBTI

The main induced effects by NBTI on PMOS transistors are the increase of the threshold voltage V_{th}, and the decrease of the drain current I_d and the transconductance g_m, and also the increase in the GIDL current (Gate Induced Drain Leakage) which is the leakage currents of the drain towards the substrate. These degradations may seem negligible for the less integrated components; particularly due to the higher threshold voltage values. On the other hand, the highly integrated CMOS produce much more heat during dynamic operations, which triggers the NBTI mechanism. Furthermore, in saturated mode, the current I_{dsat} and the voltage V_{thsat} and the transconductance derive with the same way as it is presented in the Figure I-31. Hence, the electrical characteristics of the transistor no longer correspond to the initial performance criteria, which can lead to the circuit failure.

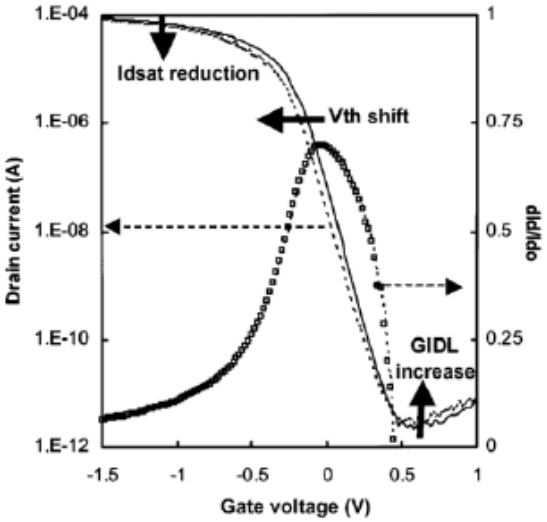

Figure I-31 Principal degradation induced by the NBTI on transistors [52]

The repercussion of the NBTI on a circuit comes more from the mismatch between PMOS and NMOS transistors because NBTI affects PMOSFET preferentially. In [53] several examples are given:

- **An inverter**: the well pairing of the V_{th} of the NMOS and the PMOS of the inverter makes it possible to ensure symmetry of the characteristic V_{out} (V_{in}), and the rise and fall times. The PMOS degradation creates a difference between the inverter's rise and fall time. The propagation time across the inverter increases, reducing the speed of the digital circuits and degrading the dynamic margins.
- **SRAM**: The static noise margin defines the ability of the memory cell to maintain steady information when there is parasitic noise or a mismatch between the different transistors of the cell.
- **RF circuit**: RF circuit design is largely based on input and output matching of components. The NBTI mechanism can degrade the scattering parameters of a transistor. The capacitance C_{gs} is strongly degraded by the NBT mechanism and is largely responsible for the variation of the S-parameters. In the inversion regime, the capacitance of the gate is reduced during an NBT constraint.

2.3.3.6 Scaling impact on the NBTI

The scaling of the CMOS transistors has a considerable impact on the degradations induced by the NBTI mechanisms. This is mainly due to the reduction of the thickness of the gate oxide. These thin oxides increase the vertical oxide field E_{ox} to a few MV/cm, which lead to more severe degradation that correspond to the increase in the threshold voltage V_{th}. The Figure I-32 presents the reduction of the NBTI lifetime with the increase of the electric field.

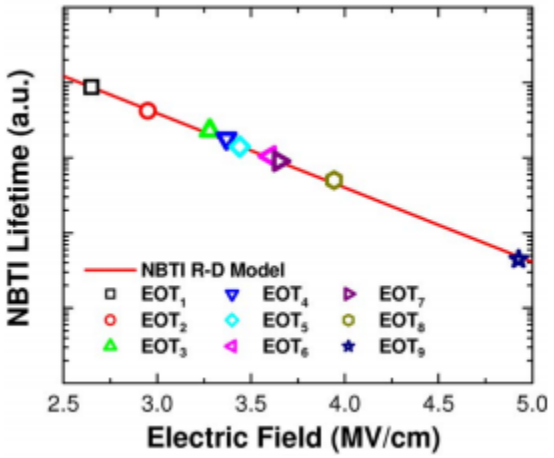

Figure I-32 NBTI lifetime evolution with the increase of the electric field [54]

To summarize, the CMOS transistors miniaturization and the evolution of advanced DSM ICs are aggravating the failure mechanisms. The increase of transistors density leads to the reduction of interconnections length. As a result, the superposition of metallic interconnections levels raises; and therefore increases the metallization density favoring electromigration mechanisms and intermetallic oxide ruptures. Moreover, the reduction of the geometrical dimensions, mainly the gate oxide thickness and the reduction of the polarization voltage do not change in the same proportions. The result is an increase in the electric fields impacting the failure mechanisms that are sensitive to electrical stress:

- The increase of the current density in the metallic interconnections favors electromigration.
- The increase of the electric field at the metallic interconnections and the gate enhances the intermetallic oxide and the gate oxide rupture.
- The increase of the electric field in the channel generally favors the HCI and NBTI mechanisms.

On the other hand, all the failure mechanisms are accelerated by the high temperatures except the HCI mechanism which is accelerated by the low temperatures. The Table I-8 summarizes the various mechanisms of degradation and the elements favoring these mechanisms as well as the stresses that accelerate them [55].

Table I-8 Scaling impact on the degradation mechanisms and stresses accelerating the mechanism

Degradation mechanism	Scaling impact	Stresses accelerating the mechanism		
		Electric stress	High temperature	Low temperature
EM	Increased density of metallization. Decrease in the width and thickness of metal lines. Increased current density in interconnections.	x	x	
HCI	Reduced length and thickness of drain. Decreased oxide thickness. Increased electric field.	x		x
TDDB	Decreased oxide thickness. Increase of the electric field	x	x	
NBTI	Decreased oxide thickness. Increase of the electric field	x	x	

3. Aging effect on EMC

3.1. Electromagnetic robustness of ICs

3.1.1.1 Overview on electromagnetic robustness

Integrated circuits lifetime has become a major problem for nanoscale technologies. In fact, on the future technology nodes, the most pessimistic predictions extend over 10 years for the integrated circuit lifetime. Thus, the degradation mechanisms appear earlier for the new technologies, causing a drift of the physical parameters which are directly related to the electromagnetic behavior of the integrated circuit. At the end of 2005, a new demand appears

from automotive manufacturers aiming to ensure the electromagnetic robustness (EMR) of embedded systems [57]. The concept of EMR is an extension of electromagnetic compatibility for the complete operating lifetime of the product. Since the reliability communities and the EMC of the components being somewhat segregated, the EMR of ICs is under-explored. However, it is fundamental to ensure the long-term functional safety of critical electronic systems. If a circuit meets EMC limits at the beginning of its life, its internal characteristics change over time, hence, compliance with the EMC limits is no longer guaranteed a few years later, as shown in the Figure I-33.

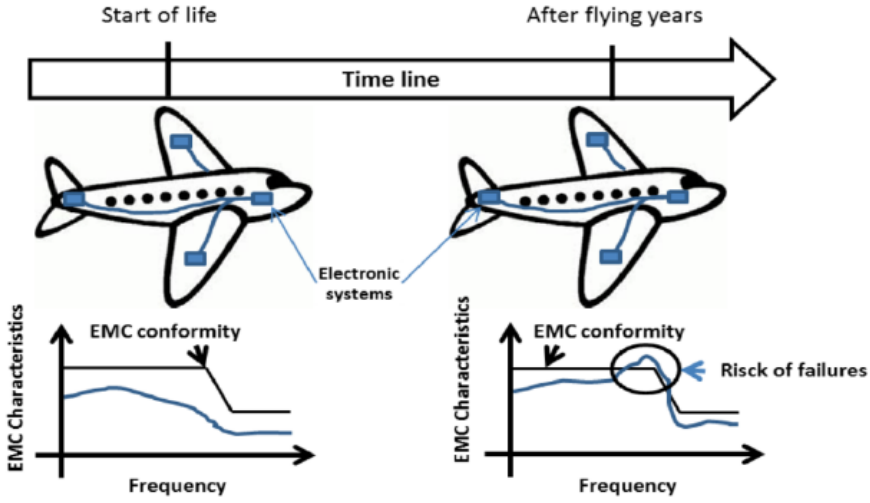

Figure I-33 Long-term electromagnetic robustness (EMR) [58]

The constraints of the space, aeronautical and terrestrial industries in terms of stringency requirements in critical environment are strong and binding for equipment manufacturers who develop and supply to the Original Equipment Manufacturer (OEM) electronic equipment. With the development of digital simulation tools, some OEMs are using the modeling to assess the risks of the EMC non-compliance of their equipment and validate the solutions. However, the requirements set out in the standards (CISP, DO160) are applied to new equipment. By following the current validation and qualification procedures, neither the manufacturer nor the OEM is satisfied that in a given environment and after a certain lifetime, a system always complies with the EMC requirements. Today, there are no existing tools to predict EMC variations during the lifetime of an electronic system.

Several studies have demonstrated that some characteristics of MOS transistors such as mobility, threshold voltage, saturation current [52], transconductance [43], and the leakage currents in the substrate or oxide capacity are drifted due to aging [3], which degrade the overall performance of the integrated circuit. In fact, the emission and the susceptibility that define the electromagnetic compatibility of an IC depend closely on the electrical and physical parameters of the circuit. Thus the aging of electronic circuits and equipment can contribute to the variation of the EMC parameters. The electronic control units of industrial equipment integrate both digital components (memories, clocks, logic gates, etc.), and analog (power electronics, input/output, amplifiers ...) and mixed electronic (power and logic). Besides the operating environment, the coexistence of

the circuits in the same system or even the same component may require additional protections because the EMC compliance of the electronic systems drifts during the lifetime.

To take into account the lifetime of the equipment imposed by the manufacturers, the manufacturers of electronic components must integrate in their design flow the aging of integrated circuits. The concept of components aging is added to the complexity of miniaturization and the reliability of integrated circuits.

3.1.1.2 Electromagnetic robustness methodology

For the characterization of the electromagnetic robustness of integrated circuits, it is necessary to define a specific methodology. The test set-up optimization is a critical step that consists in defining a number of samples for a precise evaluation of the statistical dispersion between the tested components; however the number of samples must be adapted to optimize the aging duration. It is also essential to define the EMC measurements to perform before and after aging in order to follow the drifts on the parameters which will affect the EMC levels of the integrated circuits. Stress conditions must be defined in the initial phase (temperature, vibrations, high voltage, shock, humidity, etc.) as well as the aging duration to accelerate the degradation of the components tested. In the second stage, the EMC measurement test set-up and the aging set-up must be defined and fixed throughout the aging process to ensure the reproducibility of the EMC measurements. Thus, the set-up must be validated with the measurements to make sure that only the aging is responsible of the EMC drifts. The uncertainties associated with the measurement define a limit for the consistency of the EMC drifts due to aging. At the end of the campaign, the obtained results allow comparing the EMC levels before and after aging and to extract the statistical data that concerns the EMC drifts. These data are necessary to predict the risk of non-conformity of the EMC of the integrated circuits after an operating lifetime, and readjust the margins of EMC compliance. Figure I-34 presents a methodology of characterization of the EMR proposed in [57].

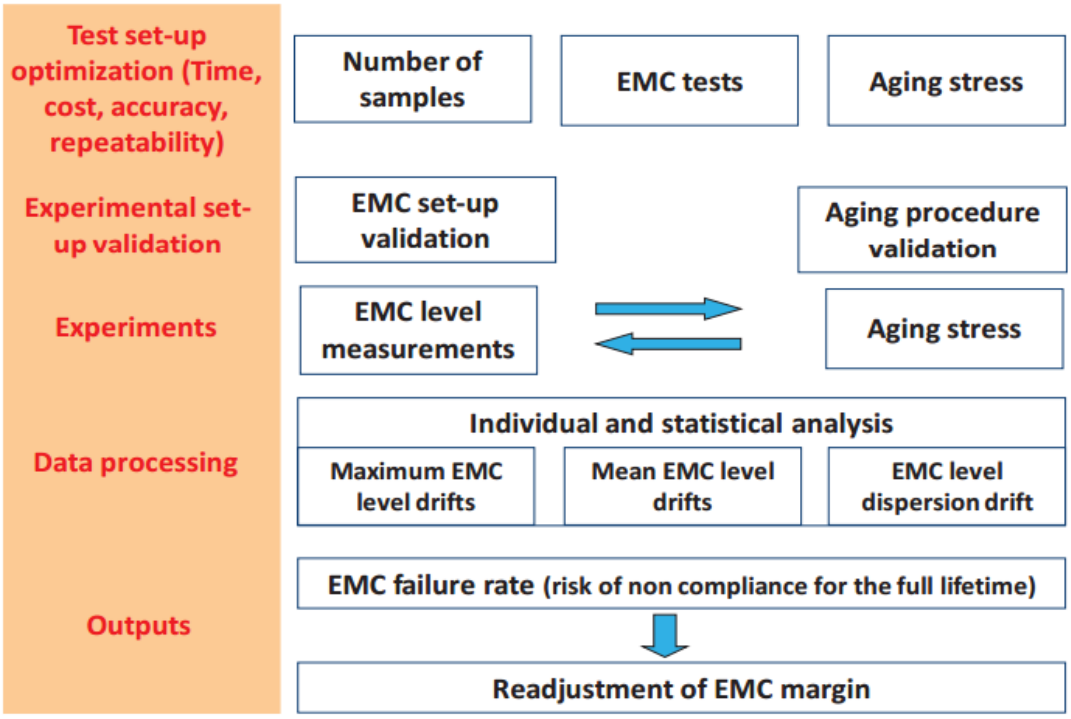

Figure I-34 Electromagnetic robustness characterization methodology [57]

Temperature stress is generally used to accelerate the aging of electronic devices. It can be combined with other type of stress (high voltage, vibration ...). It is mainly used for qualification and reliability. HTOL (High Temperature Operating Life) and LTOL (Low Temperature Operating Life) are accelerated aging tests that activate the internal degradation mechanisms of electronic components. They are used to determine the effects of the polarization conditions and the operating temperature of the semiconductors over a long period. This aging approach is based on the application in a climatic chamber of a positive temperature of 150 °C for HTOL and negative -40 °C for LTOL [59]. The components are kept in this climatic chamber for 408 h with a reading point after 96 h [60]. The supply voltage during the stress is brought to + 30 % within the maximum nominal operating range. The acceleration factors are temperature and voltage. The devices under stress can be exploited in a dynamic mode of operation. The input parameters, in particular the supply voltages, the clock frequencies, the input signals can be used outside their nominal values, but which lead to predictable and non-destructive behavior of the devices under stress.

Another methodology that allows accelerated aging of integrated circuits is based on Power Temperature Cycling (PTC). The acceleration factor is the temperature and the high voltage variation. It is equivalent to apply 1000 cycles at temperatures of -65 °C to 150 °C to stress the tested circuits. The accelerated aging TC (Temperature Cycling) is identical to the PTC but the electronic components are not powered and the acceleration factor of the TC is only the temperature. These types of accelerated aging allow passing on the behavior of electronic components' housings after years of operating life according to the requirements.

3.2. Aging effect on electromagnetic emissions (EME) of ICs

3.2.1.1 Aging effect on EME of an analog circuit

The impact of aging on the electromagnetic emissions of integrated circuits varies according to the type of the circuit (microcontroller, memory, power circuit…) and the applied stress conditions, involving the various degradation mechanisms. Studies on the impact of thermal aging on switch-mode power supplies (SMPS) have been carried out [61] since they are widely used in electronic applications of different industrial fields because of their high power efficiency. However, one of the main disadvantages is the noise produced by the switching activity which is responsible for conducted and radiated electromagnetic emission. In [61] and [62], it was demonstrated that the drifts in conducted emission of a DC-DC buck converter is related to the degradation of the passive devices that ensure filtering. The electrical schematic of the studied DC-DC converter in [62] is presented in the Figure I-35.

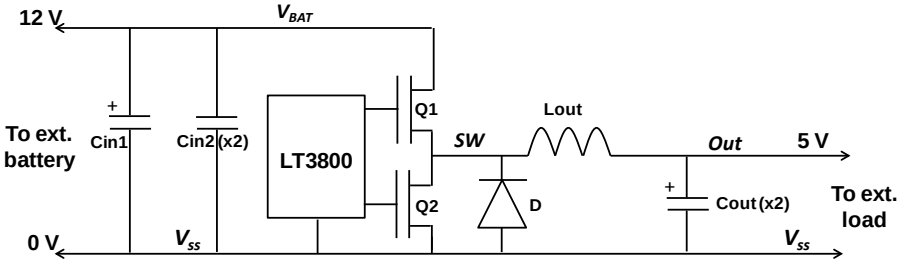

Figure I-35 Electrical diagram of the studied DC-DC converter in [62]

The studied DC-DC converter is based on a LT3800 circuit, configured in step down mode to convert the 12 V provided from an external battery into 5V. The circuit drives the gate of Q1 and Q2 NMOSFET transistors. A Schottcky diode D is mounted in parallel to Q2, and the switching frequency is set to 200 KHz. The capacitors C_{in1} and C_{in2} are used to filter the CE of the input power supply, C_{out} and L_{out} are used to filter the regulated output voltage.

The circuit was stressed in thermal chamber under the HTOL stress condition. Several measurements were performed before and after aging for the different components; impedance measurement on the passive devices, electrical measurement (I(V), C(V), Z(f)) on the transistors and the diode and a CE measurement on the DC-DC converter circuit. Figure I-36 shows the evolution of the impedance of an electrolytic capacitor and the output filtering inductor L_{out}. The degradation of capacitor mainly concerns the equivalent serial resistance (ESR) that highly increases after 336h of thermal stress. This effect is not inherent to all the capacitors, ceramic capacitors are very robust and does not defect rapidly [64]. The iron power inductor L_{out} presents a shift in the resonant frequency and a decrease of the impedance between 4 MHz and 100 MHz which can alter the filtering performance of the inductor.

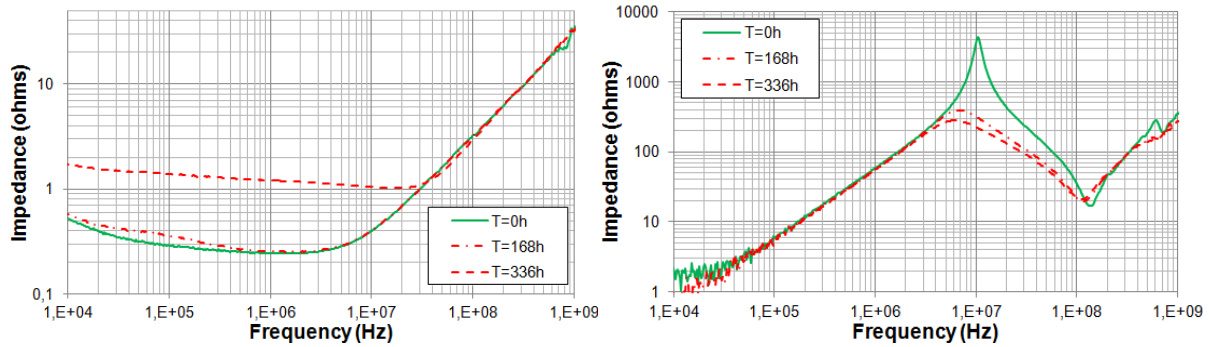

Figure I-36 Impedance evolution before and after aging on an electrolytic capacitor (left) and the output inductor (right) [62]

Figure I-37 presents the evolution of the electrical characteristic I(V) of the Schottky diode and a TVS diode. The degradation manifest with a decrease in the current which is more significant in the case of the TVS diode, this is due to the increase of the on-resistance. The degradation of Schottky diode is modest and has nearly no effect on the CE measurements, which is the same for the TVS diode. However, since its degradation is more important, this alters its efficiency to suppress the transient disturbance.

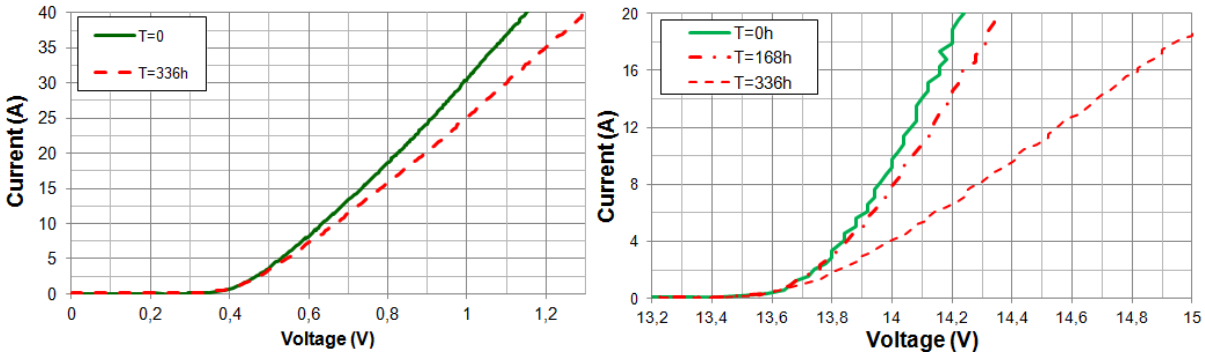

Figure I-37 Evolution of the I(V) characteristics of the Schottky diode (left) and a TVS diode (right) [62]

The conducted emission measurement was performed following the CISPR16-1-2 standard to characterize the noise on the power supply cables. In addition, a 150 Ω probe was added to characterize the conducted noise at the output of the DC-DC converter, the Figure I-38 illustrate the CE measurements before and after aging. The impact of aging in the input is too small; this is because the ceramic capacitor C_{in1} provides a sufficient ESR level that compensates the defect on the ESR of the tantalum capacitor C_{in2}. However, the measured CE at output of the converter increases significantly between 4 MHz and 100 MHz to reach up to +15 dB, because of the degradation of the inductor L_{out}.

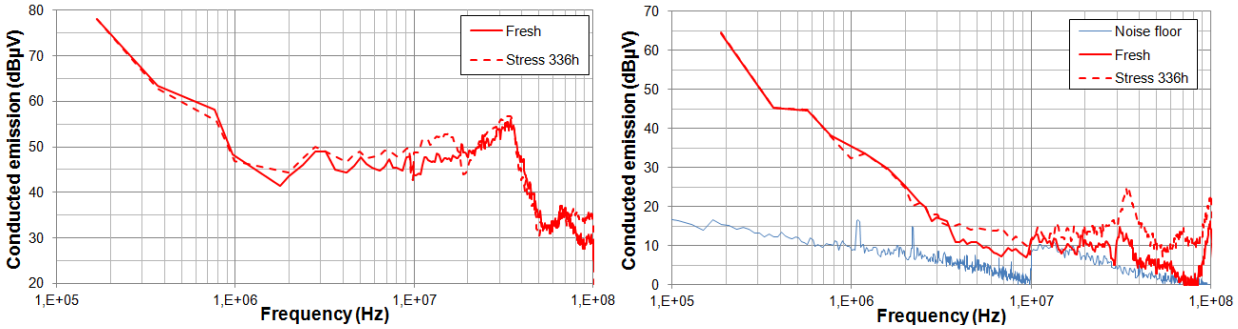

Figure I-38 Conducted emission at the input (left) and the output (right) of the DC-DC converter before and after aging [62]

The presented case study demonstrated that for power circuits the main contribution in the evolution of the CE is due to the degradation of the passive filtering circuit. This effect could have an important contribution on the increase of the emission level (until +30 dB) of electronic systems which is critical in the automotive applications [65].

3.2.1.2 Aging effect on EME of a digital circuit

For other integrated circuits as digital devices, the effect of ageing mainly concerns the involved degradation mechanism on the internal PMOS and NMOS transistors following the condition of stress. Whatever the technology is, only the sensitivity of the integrated circuit to the aging varies. Several studies have showed that the aging leads to a time dependent reduction of the power integrity issues. The study of a 90 nm digital circuit demonstrated the different stress conditions which activate the NBTI mechanism leads to the gradual increase of the threshold voltage with the stress duration following a power law. This study also shows the impact of PMOS and NMOS transistors degradation on the electromagnetic emissions of the digital circuit. Figure I-39 shows that the core power supply voltage fluctuation in the time domain and the conducted noise in the frequency domain decreases with the stress time [63].

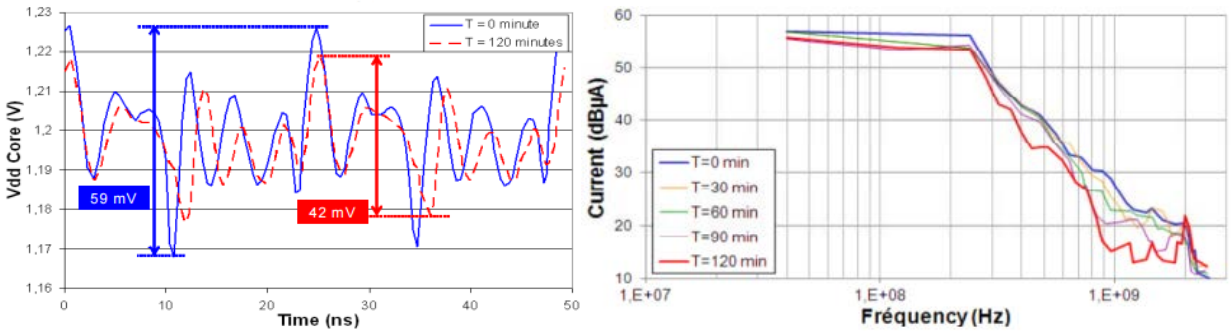

Figure I-39 Evolution of the core power voltage (left) and the spectral current of conducted noise (right) after aging [63]

3.3. Aging effect on electromagnetic susceptibility (EMS) of ICs

3.3.1.1 Aging effect on EMS of a digital circuit

The study of the susceptibility of ICs must guarantee a low level of conducted and radiated susceptibility to ensure the proper functioning of electronic devices. It is essential to study the impact of aging on the susceptibility of ICs. In fact, a study carried out on a 65 nm technology

circuit has demonstrated the evolution of the susceptibility of power supplies and inputs of the IC over a lifetime due to the drift of its internal structures. The stress condition for accelerated aging test is the LTOL; this stress is applied to validate the susceptibility level of automotive components. This allows the prediction of the behavior of internal structures of the IC after an operating lifetime of 10 years. The immunity measurement is based on the DPI standard test method [35] and the set-up is identical before and after accelerated aging. Thus, after several hours of LTOL stress, it was found that the IC has an output signal that exceeded the ± 20% criterion set before power injection. This example shows that degradation mechanisms deteriorate not only the quality of ICs, but also their immunity to EM disturbance. Figure I-40 shows the comparison of the immunity levels of the power supply of a 65 nm IC before and after aging, the circuit tested has a sensitivity which improves by a maximum of 3 dB on the frequency band 1 MHz - 5 MHz, but which degrades above 50 MHz up to 11 dB of EMI variation [30].

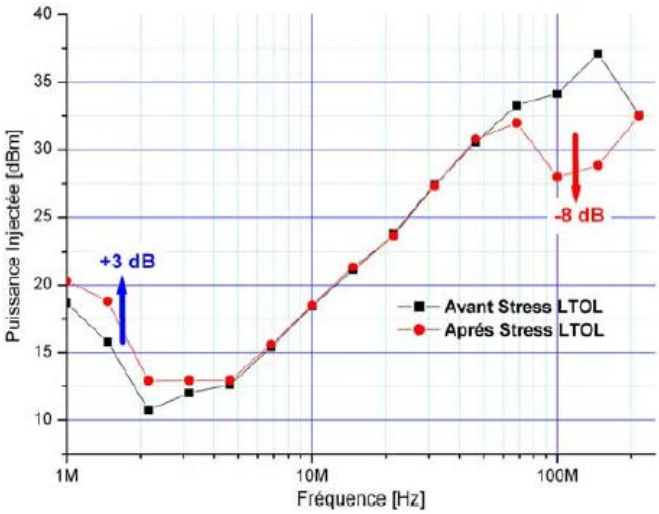

Figure I-40 The conducted immunity level of a 65 nm integrated circuit before and after aging [30]

The susceptibility of IC inputs varies according to the state of input during the characterization and the power injection frequency. After an accelerated aging, the characterization of the conducted immunity of the component inputs shows that the LTOL stress applied on the components has involved drifts on the susceptibility level of the circuit. It is difficult to identify a recurring trend of decreasing or increasing the susceptibility level. The applied accelerated aging has more impact on the circuits inputs controlled in the low state than those controlled in the high state. The power injected at the inputs of the integrated circuit propagates from the input to the output through the coupling paths which depend on the applied control signals.

The study of the susceptibility of a Phase-Locked-Loop (PLL) before and after aging consists in EMI injection following the DPI test protocol [35] on the phase comparator pin and power supply VCO. HTOL stress accelerates the aging of IC by applying a high temperature (150°) and a power supply 10% higher than the nominal supply voltage. These stress conditions accelerates the wearout failure mechanisms as TDDB and NBTI. In this study [67], the PLL operates at 24 MHz. Figure I-41 shows the accelerated aging effect on the susceptibility of power supply VCO

and the phase comparator. It was demonstrated that the disturbance on VCO is more sensible and shows a significant evolution of PLL susceptibility after aging that could reach up to +10 dB.

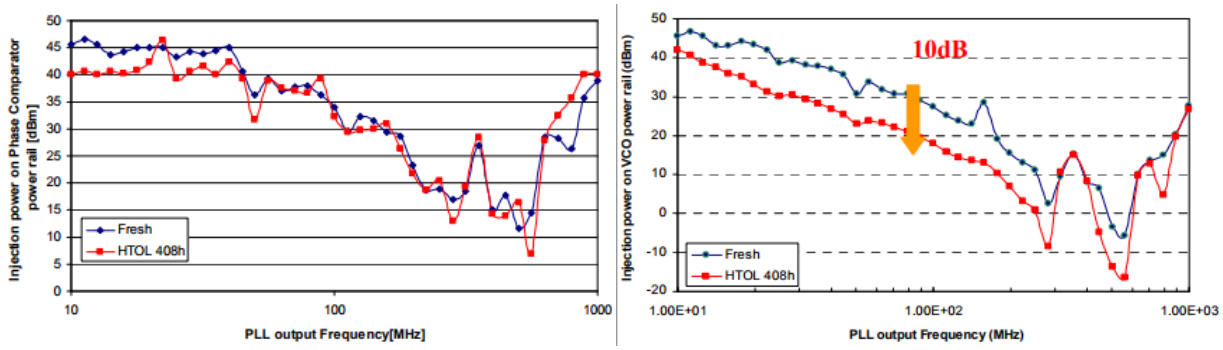

Figure I-41 PLL susceptibility threshold with an injection on Phase comparator (left) and VCO power rails (right) before and after ageing [67]

3.3.1.2 Aging effect on EMS of an analog circuit

Another case study concerns an analog circuit has also demonstrated the impact of aging on the susceptibility level. Low dropout voltage regulator (LDO) is widely used in embedded electronic applications with important EMC issues. It was demonstrated that the conducted susceptibility is related to the internal operational amplifier or the bandgap circuit cell [69] [70]. In [68], it was demonstrated that the susceptibility level of a 90 nm LDO drifted after accelerated aging using an electrical stress. During conducted injection of EMI on input or power supply an offset is induced on the regulated output voltage. With the application of an electrical stress, the susceptibility level increases when the forward power increase, Figure I-42 presents a gradual reduction of the forward power needed to induce EMI failure with the accelerated aging.

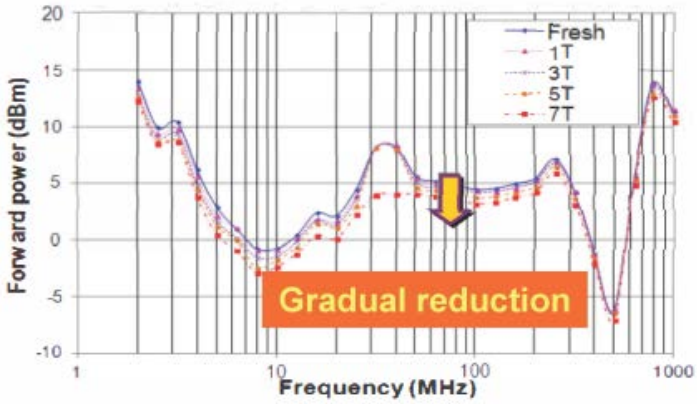

Figure I-42 Evolution of the forward power before and after aging [68]

The offset on the regulated output voltage induced by the DPI measurements increases with the aging as shown in the Figure I-43, this is due to the NBTI mechanism activation on the PMOS transistors of the circuit, especially the bias transistors of the internal operational amplifier.

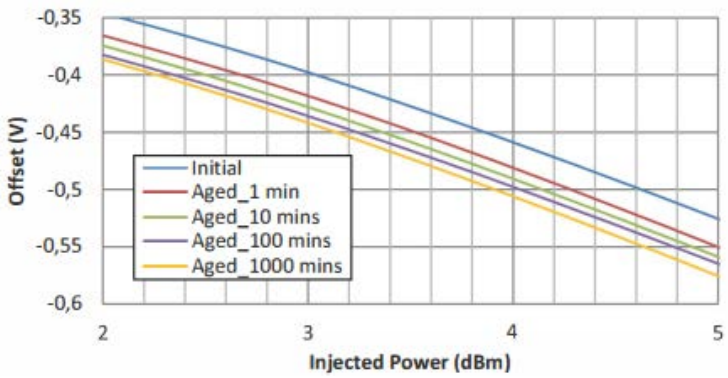

Figure I-43 Drift in the offset voltage with the injected voltage before and after aging [68]

3.4. EMC modelling taking into account the aging

As stated previously, aging has a considerable impact on the emission and susceptibility of digital and analog electronic circuits. The main drifts induce the increase of emission level and a reduction of immunity level in some frequencies. After several years' operation, the EMC drifts of an IC could reach important levels engendering a risk of wearout failure. In order to anticipate the risk of failure, it is possible to construct EMC models taking into account aging effect according to the applied stress conditions. In general, electromagnetic robustness models are constructed from EMC measurements before and after accelerated aging.

Figure I-44 presents the electromagnetic robustness model extraction workflow [71], it consists on the construction of a reliability model before and after aging that is linked to the integrated circuit EMC model. A statistical analysis of the degradation on various samples leads to the evaluation of the failure probability since it is difficult to predict the EMC drifts of one sample due to the dispersion of degradation.

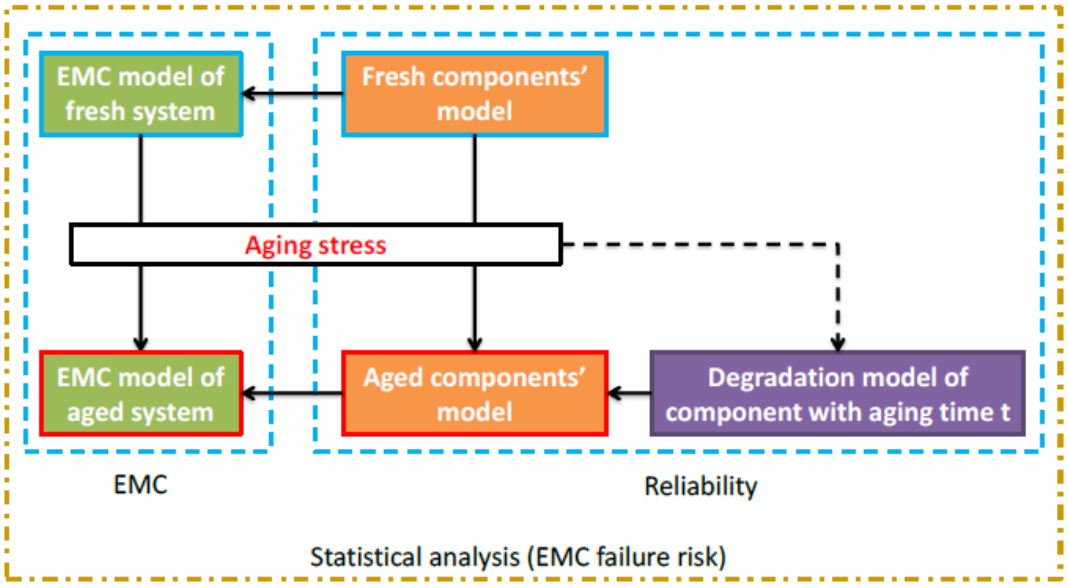

Figure I-44 Workflow of electromagnetic robustness model extraction [71]

For EMR modelling, the case study presented in 3.2.1.2 that concerns the aging of a 90 nm IC is considered. As presented, the aging leads to the evolution of power integrity and CE induced by the degradation at MOS level due to the activation of NBTI mechanism. In this study [63], an ICEM-CE model of the digital core was extracted on fresh components; its structure is presented in Figure I-45. It is composed of board decoupling equivalent model, the IC PDN model and the internal activity modeled using current sources.

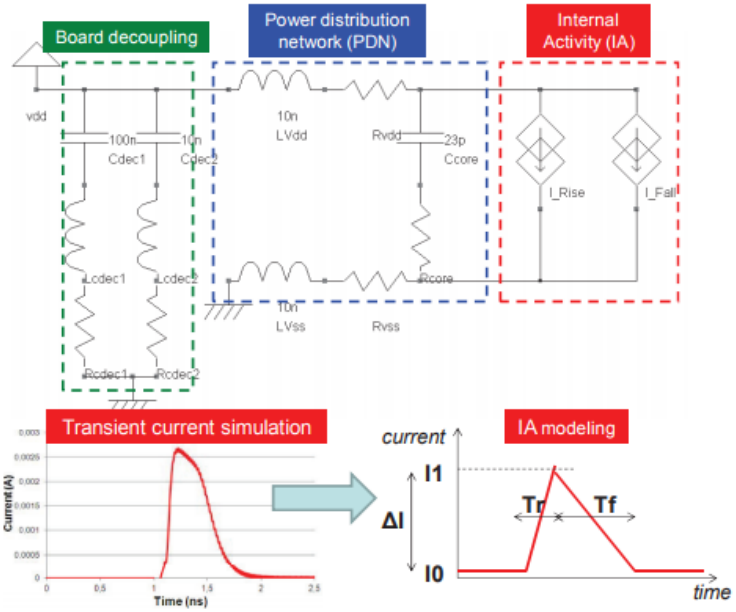

Figure I-45 ICEM-CE model of a 90 nm IC digital core [63]

In [63], the integration of aging model in ICEM-CE model concern the IA block. The falling and rising times (T_R, T_F) increased and the current amplitude ΔI decreased following the Equations I-7 and I-8, where δ is the degradation ratio, it varies between [0,1].

$$\Delta I_{stress} = \Delta I_{initial}(1 - \delta) \quad \text{(I-7)}$$

$$t_{r\,stress} = \frac{t_{r\,initial}}{1-\delta} \quad \text{(I-8)}$$

Integrating these parameters in the ICEM-CE model allows the simulation of power supply voltage fluctuation and CE after 120 min of 3,6 V electrical stress as shown in Figure I-46 and compared to the measurements. The comparison of the simulated power supply voltage bounces (39 mV) shows good agreement with the measurement (42 mV). Furthermore, the CE simulation after 120 min of electrical stress correlates with the measurement up to 1 GHz.

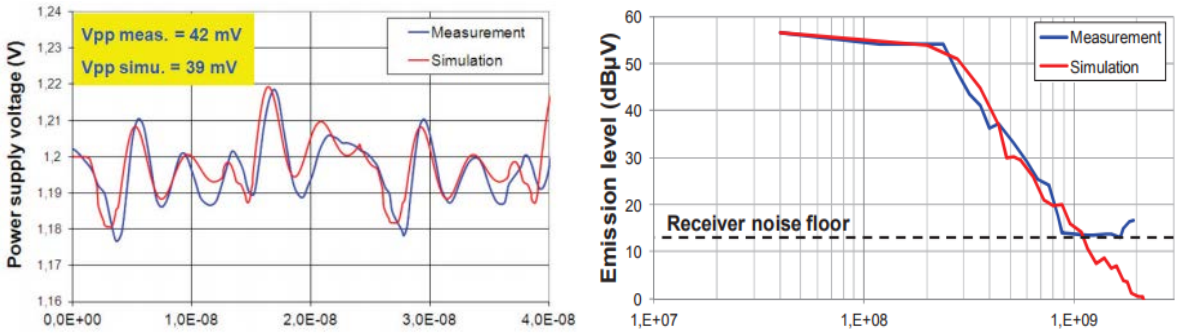

Figure I-46 Comparison between the measurement and simulation of power supply voltage fluctuation (left) and CE after 120 min under electrical stress of 3,6 V [63]

4. Conclusion

The different aspects of EMC and reliability for new integrated circuits technologies were addressed. The miniaturization of CMOS technology which involves the reduction of the gate length and the equivalent oxide thickness results in the increase of the transistors density in an IC and the increase of the switching frequencies and the decrease of the supply voltages. This implies a considerable increase of the parasitic emission produced by an electronic component and the reduction of immunity level for some integrated circuits. Several standards have been proposed for the qualification of electronic systems and circuits, and standards are proposed for EMC modeling and are used to predict the risks of non-conformity in term of EMC. However, these models have certain limitations:

- Despite the increase in computing power, the modeling of a complete electronic board and all of its components is not economically viable. EMC expertise must exist among suppliers to reduce the problem and simplify it by identifying the aggressor and the victim.
- The ground reference is always problematic in a simulation that considers it as unique and perfect. This leads to significant calculation errors.
- The perfect modeling of a strand of wires is impossible beyond few wires. A stochastic approach must be used for a worst case calculation. Some software includes Monte Carlo functions.
- The modeling of an electronic board is correct up to a hundred MHz beyond the parasitic elements and in particular forcing the return path of common mode current are badly taken into account.
- The modeling of the radiated emissions of an electronic board following a white box model requires taking into account a common phase reference to all the ICs,
- Finally, the modeling of complex components such as microprocessors or FPGA is difficult. Tools for automatic model extraction must be provided to the end user. This is the purpose of the next chapters.

In the second part of this chapter, integrated circuits reliability is introduced with a general presentation of the degradation mechanisms EM, HCI, NBTI and TDDB. As demonstrated, the activation of these mechanisms could occur prematurely with technology scaling. Hence, it is necessary to study the reliability of ICs to guarantee their well-functioning during the operating lifetime. The presented studies in the third part have shown the aging impact on EMC level of digital and analog circuits. The EMC drifts mainly concern the increase of emission level and the reduction of immunity level. According to the applied stress conditions an EMR model can be extracted and consists in integration of the aging model to EMC model (ICEM, ICIM).

Although the studies has demonstrated the ability of EMR models to simulate the drifts in EMC levels with a good precision, they does not allow the prediction of the integrated circuit lifetime, this limitation will be addressed in the next chapters.

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Chapter II. Electromagnetic compatibility modeling of integrated circuits

The EMC non-compliance problems become a real challenge for IC manufacturers and equipment suppliers. Electronic suppliers for aeronautics, space and automotive industries are facing to a strong economic competition; they are forced to use more and more COTS (Commercial off the shelf) components that own a high level of technological innovation to reduce costs. However, due to their short development cycle, their use increases the problem of components obsolescence. For a supplier, the cost of equipment requalification due to the obsolescence or second sourcing is around 30% of qualification total costs. To relieve these problems, the international committee IEC proposed standards for EM modeling for the prediction of the emission and susceptibility of ICs known as IEC 62433.

The evolution of IC technology and their complexity through the increase of the number of transistors and the miniaturization of electronic components has a huge effect on the dynamic power consumption and the increase of parasitic electromagnetic emissions. Thus, there is a crucial need to construct models to predict the noise generated by large and complex digital IC, which creates tight constraints on PCB routing and decoupling capacitor budget to meet power integrity (PI) and EMC requirements. For this purpose, IC end-users need circuit models that predict with a reasonable accuracy the main characteristics of power supply voltage fluctuation and conducted emission (CE) spectrum according to the circuit configuration. In order to be included within industrial design flow efficiently, these models must remain simple enough to ensure rapid simulations and compatible with usual simulation tools. Existing standards such as ICEM-CE (Integrated Circuit Emission Model – Conducted Emissions) known as IEC 62433-2 standard have been developed to respond to these requirements. However, ICEM-CE is rarely delivered by IC manufacturers. This situation leads IC end-users to look for efficient methods to construct their own ICEM-CE models. The standard describes measurement methods to extract PDN block. The construction of the IA block remains a challenging task for IC end-users. The construction methodology described in the standard is also based on measurement standards and present several limitations. Its drawbacks will be presented in this chapter and new methodologies for IA block construction are presented. Only the emission aspect will be discussed in this chapter. In addition, signal integrity problems are recurrent for fast digital buses, and the existing IBIS model allows the characterization of IO drivers for different JEDEC standards. The construction of an IBIS model is not the purpose of this chapter, but its contribution in EM modeling will be demonstrated.

The first section of this chapter is dedicated to a general overview on EMC and SI modeling and to describe ICEM-CE and IBIS standard. Secondly, the circuit under test and the test board will be presented. The third part concerns the construction of an ICEM-CE model of a complex IC following the approach proposed by the standard, the methodology and case studies are presented for the validation of ICEM-CE model, and particularly, the limitations of the measurement based IA block construction are pointed out. Finally, a new methodology for the construction of the

internal activity of a FPGA is proposed followed by the presentation of ICEM GENERATOR tool developed to automate the extraction of the internal activity.

1. General overview on EMC and SI modeling

1.1. Introduction

From their early design stages, electronic circuits may present EMC compliance problems. Hence, it is important to develop EMC models for electronic devices that allow prediction of the emission and susceptibility levels before fabrication. The design flow of a circuit makes it possible to establish the needed operations to control the functional and high-performance aspects before manufacture. Thanks to the development of advanced electrical and electromagnetic simulation tools (Spice, ADS, ANSYS, HFSS...), it is possible to build EMC models based on the circuit equivalent model during the design phase. The circuit could need certain improvements until it reaches a degree of EMC conformity adapted to the margins defined by the standards. The design flow of an electronic device taking into account the EMC performance is presented in the Figure II-1. This allows manufacturing costs optimization and reduces the manufacturing time of electronic devices.

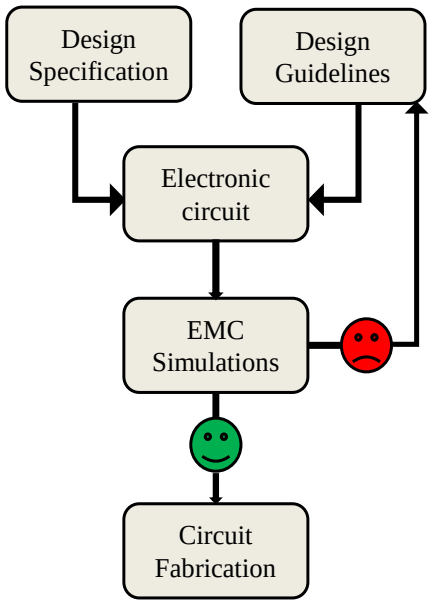

Figure II-1 Design flow of an electronic circuit taking into account the EMC performance

There are several levels of EMC modeling as shown in the Figure II-2. The modeling approach can be applied at the level of an electronic system by characterizing the electromagnetic behavior of the various functions of a system. In aeronautics, the Integrated Modular Avionics (IMA) architectures consist of several calculation modules capable of supporting different applications and presenting important EMC requirements. In this case, the modeling allows the evaluation of conducted electromagnetic disturbances carried out via the backplane or the evaluation of

radiated emission by parasitic coupling between the different electronic boards. Macro-models can be used to predict the emission and susceptibility of a system.

The second level of modeling is at the printed circuit board (PCB) level. The modeling of the various integrated circuits mounted on PCB may be necessary. This approach is based on the divide and conquer algorithm which consists in breaking down a problem into two or more sub-problems, this allows simplifying the modeling of each block before giving a solution to the initial problem by subsets recombination. Hence, it is also necessary to create an equivalent PCB model taking into account the decoupling capacitors for modeling the on-board resonance. Several existing numerical simulation tools are capable of modeling the PCB from electromagnetic simulations on PCB traces, power and ground planes, vias… These tools are based on the resolution of Maxwell's equation and integrate different numerical resolution methods. The most commonly known method is the FEM (Finite Element Method) [1] which allows the modeling of the parasitic effect with a volume meshing by dividing a region in order to solve the electromagnetic problem in the frequency domain for several sub-regions and finding an approximated solution to the initial problem. Other methods are also widely used, as the Method of Moment (MoM) [2] which is based on a frequency domain extraction of the current flowing in the conductors using a surface meshing, and the Finite Difference Time Domain (FDTD) [3] which used a direct translation of Maxwell's equations in a differential form into finite difference equations and is based on volume meshing. In general, the electromagnetic simulation tools support the macro-modeling, which allows speeding up the simulations for complex systems and could be integrated into SPICE simulators [4] [5].

Finally, EMC modeling at the level of an integrated circuit has become necessary. Electronic components are more disruptive and more sensitive to interference from their environment due to the increase of clock frequency, the integration of hundreds of millions of logic gates, and the reduction of the power supply voltages. EMC problems usually appear between analog and digital blocks. The modeling can go through black box models or through white box models with an elementary description of the different levels of an integrated circuit (Die, wire bonding, package…).The black box modeling approach consists of a representation of the behavior of an integrated circuit in an equivalent form, whereas the white box modeling approach describes the internal structures of the component as long as we know the physical description of the circuit. For confidentiality reasons, it is rarely possible to have access to the internal structures of the components in order to build white box models. Thus, the founders of ICs favor the black box approach for not disclosing information about the design of their circuits. These different models are based on the use of measurement results and on electromagnetic simulations. In this chapter, the EMC modeling of an integrated circuit at the level of a PCB will be discussed.

(a) (b) (c)

Figure II-2 The different level of EMC modeling: system level (a), PCB level (b), integrated circuit level (c)

With the emergence and strengthening of EMC requirements for electronic systems and components, the need for a prediction model for EMC has been felt with multiple goals [6]:

- Predict the compliance of electronic components to EMC constraints.
- Understand the influence of design parameters; as the traces dimensions, antenna, and the decoupling capacitors…, on EMC.
- Validate and provide solutions to reduce electromagnetic emission and immunity to interference.
- Assess the environment effect on EMC performance as the temperature, power supplies, and aging.

As seen in the previous chapter, a considerable effort from the standardization committee, especially from the W69 group of IEC, was deployed to produce standards for designers to develop the emission and immunity models of electronic components. The IEC 62433 project aims to develop generic models of integrated circuits for modeling conducted and radiated disturbances. A reminder of the EMC models of the integrated circuits is given:

- **ICEM-CE**: Integrated Circuit Emission Model for Conducted Emission (IEC 62433-2)
- **ICEM-RE**: Integrated Circuit Emission Model for Radiated Emission (IEC 62433-3)
- **ICIM-CI**: Integrated Circuit Immunity Model for Conducted Immunity (IEC 62433-4)

Currently, there is no standard for modeling radiated immunity at a circuit level. In the state of the art, the radiated immunity problems are related to the conducted immunity problems by coupling on PCB traces [7].

In addition, the same need for modeling also exists for signal integrity. In fact, it is essential to ensure the error-free transfer of digital data via high-speed communication buses. An important contribution to the modeling of signal integrity of the components comes from the IBIS [8] (I/O Buffer Information Specification) group, which proposed a standard for describing the electrical performance of input/output (IO) structures of integrated circuits at the beginning of the 1990s. IBIS is widely used by IC manufacturers and high speed PCB designers and is supported by numerous CAD tools [9].

We can also cite the IMIC model [10] (I/O Interface Model for Integrated Circuit), which was developed by the Japan Electronics and Information Technology Industries Association (JEITA) and published in March 2001. The IMIC model has been proposed to correct some disadvantages of the IBIS model. In particular, it integrates RL networks in the supply rails in series with the output transistors and it allows defining the waveform models for the output transistor

commands, which are only expressed with PWL (Piece-Wise Linear) files and are independent of the activity.
In this manuscript, we will discuss the EMC aspect of a complex integrated circuit and the methodology of integrating an IBIS file to the conducted emission simulation will be presented. Hence, we will be particularly interested in ICEM-CE and IBIS models.

1.2. IBIS model

Signal integrity (SI) is a major constraint of fast digital buses in order to limit the transmission of invalid bits, inter-symbol interference, transmission rate limitation, electrical stress applied to the IOs due to overshoot and undershoot. The study of SI consists in ensuring that the temporal profiles of signals transmitted to the digital receivers do not induce any error in the interpretation of the binary information carried by the signal. In order to anticipate SI problems from the design phase of electronic boards and improve the routing of fast buses, the IBIS standard has been developed by Intel in 1993, the last version V6.1 has been published in 2015 [8]. It is a behavioral model that focuses on the study of the characteristics of the inputs/outputs of the circuit. The approach followed is therefore a black box approach that does not require knowledge of the internal structure of the circuit.
The IBIS standard has appeared in order to be portable on any simulation tool platform, and to generate simulation times faster than simulations carried out with Spice models. The IBIS model is represented by an .ibs file written in ASCII format as presented in the Annex 2, and gives the following information:

- Electrical circuit of the package (R_{pkg}, L_{pkg}, C_{pkg}).
- The threshold voltage V_{th} of an input buffer.
- IOs capacitance (C_{comp}).
- The curve I(V) of the clamping diodes.
- The curve I(V) (Pull-up and Pull-down) of the output buffer.
- The curve V(t) of the rising and falling transitions.

An IBIS model can describe various types of IOs; single-ended or differential IOs, open-drain, 3-state IOs and push-pull collector. It is possible to build an equivalent model of an IO from the information given by the IBIS file; however, the IBIS standard does not describe the methodology of construction of this model.

1.2.1 IBIS model of an input

The model of an input is presented in the Figure II-3; it generally consists of the following elements:

- The connection between the chip and the external pin: it is characterized by a package capacitance C_{pkg} connected to the ground plane of the board, a resistor R_{pkg} and an inductance L_{pkg} including the package traces and the bonding wire.
- The input is modeled by two clamping diodes, when they exist, which are connected to the ground and to the power supply (ground clamp, power clamp).
- C_{comp} which is the equivalent capacitance of the IO structure.

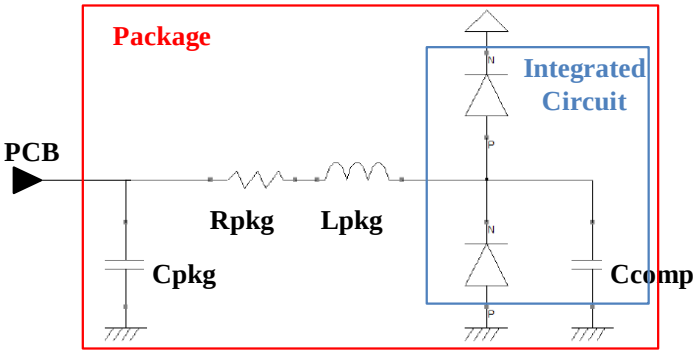

Figure II-3 IBIS model of an input

With these elements, the curve I(V) which characterizes the input is obtained. The models of the power clamp and ground clamp are built from the I(V) curves contained in the IBIS file.

1.2.2 IBIS model of an output

The Figure II-4 shows the structure of an output described by the IBIS model. It is composed of a pull-down and pull-up transistors, clamping diodes to protect the circuit from electrostatic discharges, the chip capacitance C_{comp} and the package equivalent parasitic circuit (RLC). The structure presented in this figure is the usual structure for push-pull and single-ended outputs, the clamping diodes are modeled only if they exist in the chip.

Rather than supplying the SPICE parameters for different standard models of devices, IBIS model gives the response curve I(V) of the corresponding output, for buffers at $V_{GS} = V_{DS}$ for a CMOS output, as shown in the Figure II-5 [11] (where V_{GS} is the voltage between the gate and the source, and V_{DS} the voltage between the drain and the source). Furthermore, the model presented in Figure II-4 is based on a push-pull stage activated by the pull-up and pull-down commands constructed from V(t) curves which allow to reproduce the output waveform. This allows an accurate simulation while preserving the confidentiality of the technological parameters and being independent of the model and its implementation.

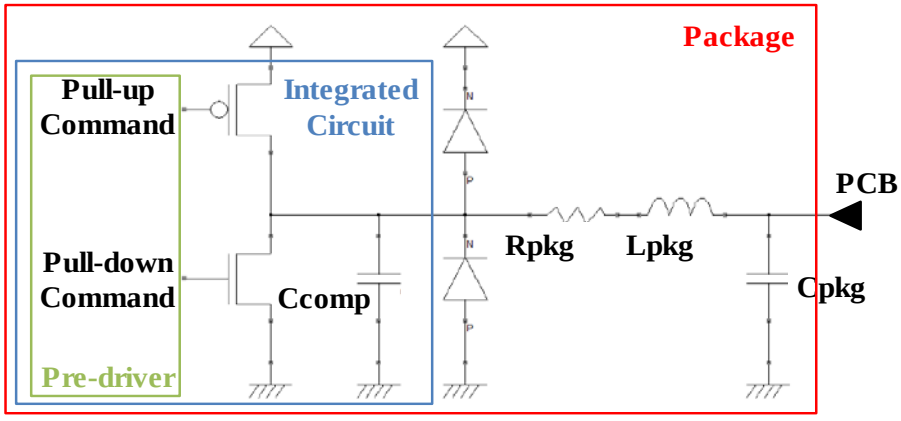

Figure II-4 IBIS model of an output

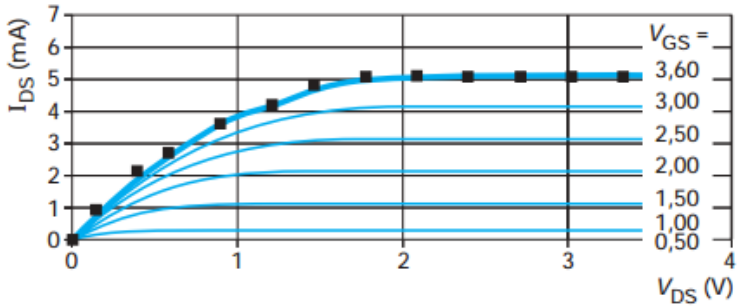

Figure II-5 I(V) curve for the simulation of an output response [11]

There are several limitations in the traditional version of IBIS model, which are increasingly visible during simulations of very fast switching IOs. The limitations arise from the nonlinear character of the equivalent output capacitance of the IO which is assumed to be constant and modeled by the capacitance C_{comp}. In addition, traditional IBIS was conceived to be used by an electric simulator (SPICE). However, the development of Gbits/s communication bus required the introduction of advanced signal processing techniques (SERDES, pre-emphasis, equalization) which is difficult to simulate with an electric simulator. An evolution of IBIS has been proposed as IBIS-AMI. On the other hand, the power supply network model is not integrated in the previous versions of IBIS, although it is expected for the recent versions, its integration is not systematic. Thus, the precision of IBIS model is less accurate. For this reason, IBIS model is not intended for EMC simulation. However, in this study, we will demonstrate that IBIS can be coupled to an EMC model (ICEM) for the IO noise prediction.

1.3. ICEM-CE model

1.3.1 Overview on ICEM-CE model

The ICEM-CE (Integrated Circuit Emission Model for Conducted Emission) model is standardized IEC 62433-2 and has been proposed since 2008. ICEM-CE model is supported by the French committee UTE-AFNOR. It is a simplified model of the representation of an integrated circuit and its environment from an EMC point of view. The ICEM-CE objective is to predict the generated disturbance on the circuit power and the ground rails.

The internal composition of a circuit allowing the analysis of the origin and transmission of the conducted emissions is given in the Figure II-6 [12]. The internal digital activity of the core and the IOs are sources of electromagnetic noise resulting from the switching of the transistors. The internal coupling paths propagate this noise to the external pins of the component.

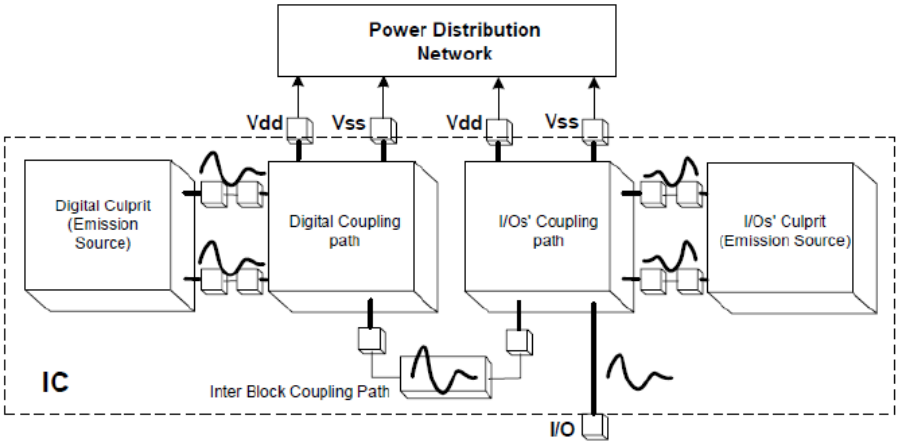

Figure II-6 Presentation of the noise source and the coupling path of an IC

The ICEM-CE model generally describes the conducted emission of a circuit by associating a current source representing the internal activity (IA) of the circuit with an impedance network PDN (Passive Distribution Network) where the disturbance flows through the power pins and the IO pins. The ICEM-CE model is presented in the Figure II-7.

The ICEM-CE model of an integrated circuit is conceived as a macro-model constructed from one or several PDNs and one or several IAs. The PDN includes both the parasitic elements of the chip and package. It includes the on-chip decoupling capacitors, the equivalent resistance and inductance of power and ground rails. This general macro-model has the least information on the internal design of the integrated circuit.

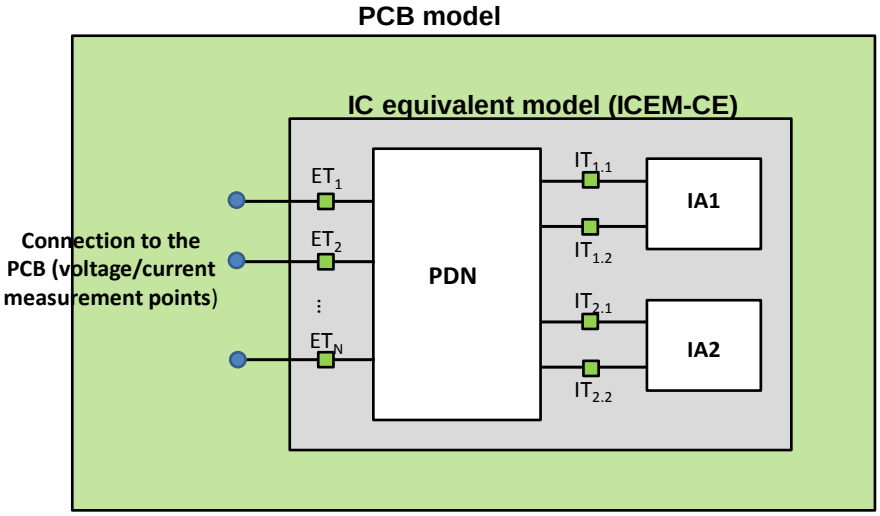

Figure II-7 Presentation of the ICEM-CE macro-model

There is also a general macro-model block which consists in the assembly of several basic elements. Each element is corresponding to a specific functional block with the PDN block directly connected to the functional block as a digital core with its power supplies, an analog function and IOs. This block is called Inter-Block Coupling (IBC), which is an impedance network representing the coupling between the different power rails and also between the

functional blocks, for example, between an analog function block and a digital function block. It could represent the substrate coupling which is modeled using an equivalent RC circuit. However, it requires a thorough knowledge of the circuit and is intended for circuit designers. The external terminals allow connecting the different blocks of the ICEM-CE model to the external environment of the integrated circuit. The internal terminals allow connecting the different blocks of ICEM model (PDN, IBC, IA) to each other.

Finally, the macro-model based on sub-models represents the electromagnetic behavior of some circuit functions. The accurate construction of this model requires a thorough knowledge of the design of the circuit and is reserved for ICs founders. It is suitable for describing the EMC behavior of digital circuits (memory, CPU, etc.). The sub-model can be used in the construction of ICEM-CE models of different circuits using the same function. The sub-model consists of a PDN and one or more IAs. The PDN has internal terminals and has no connection to the external pins of the circuit. The ICEM-CE model is constructed by associating one or more sub-models with a PDN of the chip and the PDN of the package. The PDN of the chip includes the power supply and ground network including on-chip decoupling capacitors.

1.3.2 Passive Distribution Network (PDN)

The passive distribution network (PDN) describes the internal power network structure and/or the passive distribution of the IOs. It is composed of passive elements (resistances, capacitances, inductances) which represent the electrical behavior of the logic blocks and the circuit structure connected between power and ground rails, the bonding wires, the interconnection and the parasitic elements of the package.

The PDN can be obtained with S-parameter measurement performed directly on the package of the IC; hence, the PDN obtained is linear. In the case of non-linearity, due to the clamping diodes, for example, a measurement of the I(V) characteristics may be necessary. IBIS model can be useful for providing information on the package parasitic elements.

An example of a constructed PDN in [13] of a Dspic33FJxxxGP706 microcontroller is given in the Figure II-8. The circuit is composed of four power supply twin pins and one decoupling core pin. The presented structure is supposed and constructed from the few information provided by the IC manufacturer (silicon technology, package, IBIS file…). The structure includes parasitic elements (R_{VDD}, L_{VDD}) and (R_{VSS}, L_{VSS}) of the power supply and ground pins and the IBC between the different power planes.

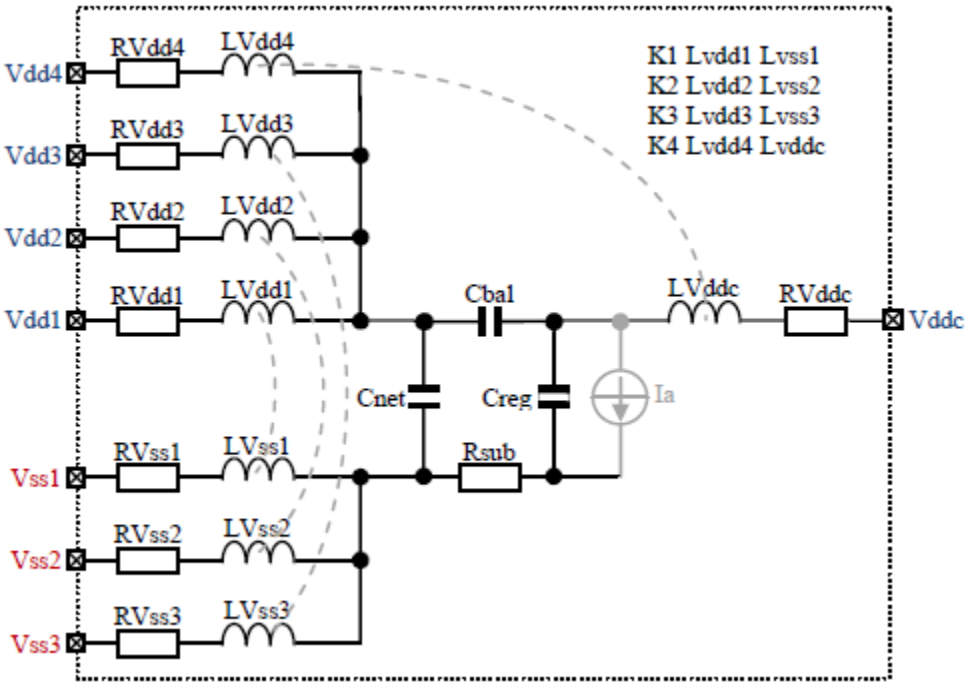

Figure II-8 PDN model of a microcontroller DSPIC [13]

In [29], a PDN model was developed and validated up to 12 GHz for a 16-bits microcontroller. This is possible when applying special calibration techniques and characterizing the power network impedance in a large frequency band.

Because of the lack of information on the internal structure of the integrated circuits, a simplified structure of the PDN can be assumed and completed by the S-parameters measurements and the IBIS file if the integrated circuit manufacturer provides it. Hence, the constructed PDN is validated by comparison between the measured and simulated S-parameters.

1.3.3 Internal Activity (IA)

1.3.3.1 IA extraction in the IEC standard

The internal activity describes the activity of the integrated circuit using a current or voltage source. This description can be expressed in the time or frequency domain. For the measurement of internal activity, the external current of the component must first be obtained between the pins VDD and VSS. As presented in the Figure II-9, the internal activity could be determined from the external current measurement I_{ext} and the equivalent impedance network of the circuit (PDN), the on board decoupling (Z_{dec}) and the measurement system R_m.

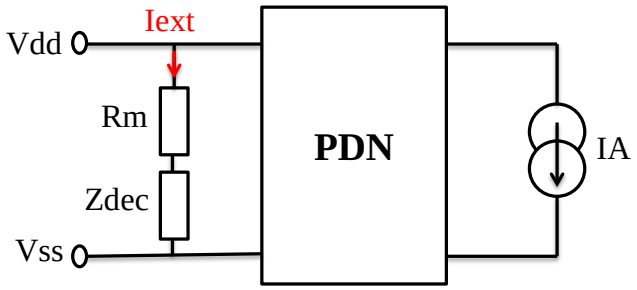

Figure II-9 IA construction based from the external current measurement

The IEC 61967 standard can be used to measure the external current. The standard is composed of 6 parts, proposing different measurement methods that were discussed in the previous chapter. In this chapter we will focus on the IEC 61967-4 standard which proposes a direct coupling method based on 1Ω/150Ω probes presented in the Figure II-10. Moreover, a new methodology for IA construction will be proposed later in this chapter.

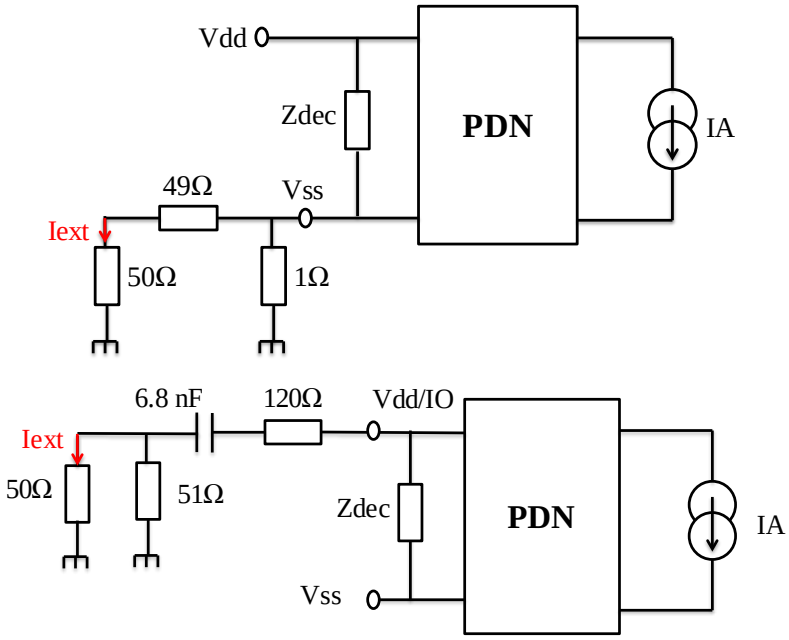

Figure II-10 IEC 61967-4 measurement methods: 1 Ω method (top) 150 Ω method (bottom)

The 1Ω/150Ω measurement methods are widely used for the construction of the ICEM-CE model, more particularly the 1 Ω method, because it is necessary not to disturb much the power supply network. The 150 Ω method generally provides the ICEM-CE model of the IOs, but can also be used to characterize the noise in power planes of the IC. The 150 Ω method is dedicated to voltage measurement; this method is justified by the IEC61000-4-6 standard, which indicates that in the majority of cases, 150 Ω is the impedance of the equivalent antennas of the cabling network (traces). With the constructed PDN of the microcontroller presented in the Figure II-8 and the measurement of the external current following the 1 Ω method, the Figure II-11 presents the constructed IA in the time and frequency domain and a comparison between the measured

and simulated external current with the 1 Ω probe [13]. This method allows the individual evaluation of the contribution of each pin in the conducted emissions; it is also linear and valid in very low frequency and is reproducible [14].

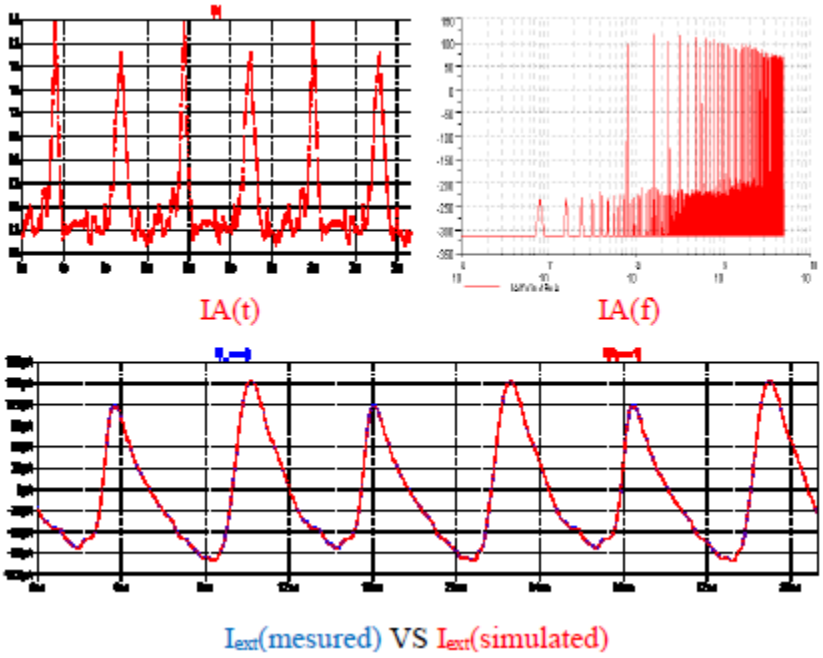

Figure II-11 IA construction and comparison between the measured and simulated external current [13]

1.3.3.2 Limitations of the IA extraction method based on 1 Ω measurement

The 1 Ω measurement offers the possibility to extract the internal current of an integrated circuit with a linear computation. The main drawback of the extraction approach based on 1 Ω measurement is its dependency on the PDN model and is extremely sensitive to any measurement error. Although this method is reproducible and gives good simulation result of the electromagnetic noise generated by the circuit in the V_{SS} pins which correlates with the measurement, it does not ensure a good estimation of the internal current. However, the extraction approach is still suitable for simple integrated circuits which do not have several power and ground pins.

The calculation of the internal current [I_{int}] requires a measurement of the external current [I_{ext}] that flows through the 1 Ω probe multiplied by the inverse of the transfer function of the integrated circuit, the PCB and the probe $[H]^{-1}$ as shown in Equation II-1. Thus the slightest error on the transfer function can lead to an overestimation of the amplitude of the internal current.

$$[I_{int}] = \begin{bmatrix} H_{11} \\ \vdots \\ H_{1n} \end{bmatrix}^{-1} . [I_{ext}] \qquad \text{(II-1)}$$

To understand the effect of the external current measurement and the transfer function simulation errors on the estimation of the internal activity using the inverse method, the schematic presented in Figure II-12 is considered to illustrate the link between the internal activity and the external

voltage measurement V_1 (V_2) when the transfer function H_1 (H_2) represent the equivalent filter using a 1 Ω probe (150 Ω probe).

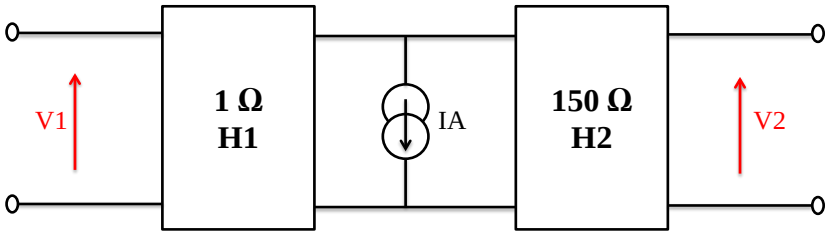

Figure II-12 Simplified illustration of the link between the transfer functions and the external voltages measured with the 1/150 Ω methods

The transfer functions H_1 and H_2 present several resonance points where the slightest error could induce very large errors on $|H_1|$ and $|H_2|$. Furthermore, the transfer functions are not exactly known because they are extracted from an optimization algorithm using measurements. Also, there is no direct access to these filtering systems from the side of the internal current; hence, the transfer functions could not be measured accepting the measurement errors ΔH_1 and ΔH_2. Let us consider the terms $\tilde{I}_{INT}$, $\tilde{V}_1$ and $\tilde{H}_1$ representing the modified values of I_{INT}, V_1 and H_1 by the error values ΔI_{INT}, ΔV_1 and ΔH_1 for each frequency point, as shown in the following Equations.

$$\tilde{I}_{INT} = I_{INT} + \Delta I_{INT} \quad \text{(II-2)}$$

$$\tilde{V}_1 = V_1 + \Delta V_1 \quad \text{(II-3)}$$

$$\tilde{H}_1 = H_1 + \Delta H_1 \quad \text{(II-4)}$$

The computation of the internal current $\tilde{I}_{INT}$ based on the external voltage measurement is given by the formula II-5:

$$\tilde{V}_1 = \tilde{H}_1 . \tilde{I}_{INT} \xrightarrow{yields} \tilde{I}_{INT} = \frac{\tilde{V}_1}{\tilde{H}_1} \quad \text{(II-5)}$$

Considering the Equation II-5 and the partial derivatives method given by Equation II-6, the absolute error of the internal current estimation ΔI_{INT} is expressed by Equation II-7.

$$\Delta I_{INT} = \left|\frac{\partial I_{INT}}{\partial V_1}\right| \Delta V_1 + \left|\frac{\partial I_{INT}}{\partial H_1}\right| \Delta H_1 \quad \text{(II-6)}$$

$$\Delta I_{INT} = \frac{\Delta V_1}{\tilde{H}_1} + \frac{\tilde{V}_1 . \Delta H_1}{\tilde{H}_1^2} \quad \text{(II-7)}$$

In the Equation II-7, two terms contributes in the internal current absolute error evaluation:

- The first term $\frac{\Delta V_1}{\tilde{H}_1}$ is linked to the measurement error of V_1. This term could be more important when H_1 is low.
- The second term $\frac{\tilde{V}_1 . \Delta H_1}{\tilde{H}_1^2}$ is linked to the estimation error of H_1. This term becomes dominant when H_1 is low, especially because of the denominator $\tilde{H}_1^2$.

However, the transfer functions H_1 and H_2 are often low because of the filtering effect of the PDN. Hence, $|H_1|$ and $|H_2|$ have always values less than 1. As illustrated by Figure II-13, ΔH_1 is large and H_1 is low, then, $\frac{\Delta H_1}{\tilde{H}_1^2}$ becomes very important.

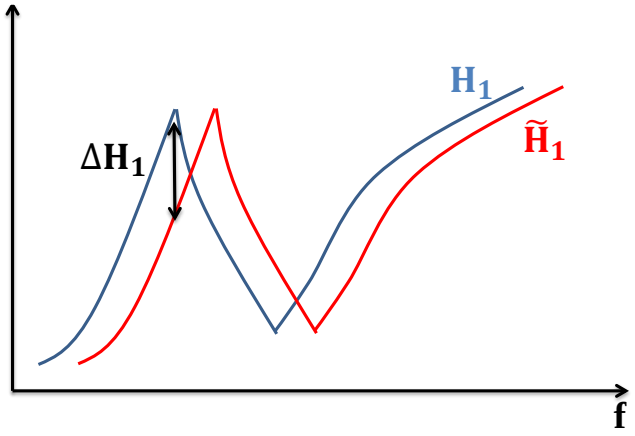

Figure II-13 Illustration of the induced absolute error on the transfer function

Assuming that the internal current extraction was performed using the inverse method based on the 1 Ω method, the simulation of the external voltage V_2 based on the transfer function H_2 that includes the filtering with the 150 Ω probe could be influenced by the estimated error on $\tilde{I}_{INT}$. The modified value $\tilde{V}_2$ of V_2 by the error ΔV_2 is given in the following Equations:

$$\tilde{V}_2 = V_2 + \Delta V_2 \tag{II-8}$$

$$\tilde{V}_2 = \tilde{H}_2 . \tilde{I}_{INT} \xrightarrow{yields} \tilde{V}_2 = \frac{\tilde{H}_2 . \tilde{V}_1}{\tilde{H}_1} \tag{II-9}$$

$$\Delta V_2 = \frac{\tilde{H}_2}{\tilde{H}_1}\Delta V_1 + \frac{\tilde{V}_1}{\tilde{H}_1}\Delta H_2 + \frac{\tilde{H}_2 . \tilde{V}_1}{\tilde{H}_1^2}\Delta H_1 \tag{II-10}$$

The estimation of the absolute error on V_2 given in the Equation II-10 shows the contribution of three terms:

- The first term is linked to the error on V_1. This term could be larger when $\tilde{H}_2$ is important and $\tilde{H}_1$ is low.
- The second term depends on the error on H_2. This term is amplified when $\tilde{V}_1$ is important and $\tilde{H}_1$ is low.
- The third term depends on the error on H_1. This term is larger when $\tilde{H}_2$ and $\tilde{V}_1$ are important. However, when $\tilde{H}_1$ is low, this third term will be the most important contribution in the absolute error ΔV_2.

The inverse method has an inherent problem of amplifying the measurement noise when the transfer function is low. However, in the circuit model, the PDN has several resonance points. Thus, any variation on the estimation of these resonances will lead to an amplification of the error contribution on the transfer function, due to the term $\frac{1}{\tilde{H}_1^2}$ as presented. At resonance frequencies, it is possible to overestimate the internal current. Consequently, when the internal current is

extracted using the inverse method, the prediction of conducted emission at another point will be influenced by the absolute error of the current extraction, which contributes not only to the total error, but can also be amplified.

1.3.3.3 Alternative IA extraction methods

The IA block can be constructed from the simulation of the transistors netlist, the transistor model library and the standard cell models [15]. However, this approach requires considerable simulation time and relies on unavailable data for IC end-users. The IA block may be estimated from basic technological information about the technology and IC characteristics (e.g. CMOS technological node, number of logic gates, die surface…), for example with tool like ICEM expert module in IC-EMC software [16]. The IA is estimated roughly from the floor-planning definition of the circuit or without exact information about the circuit, but the main drawbacks of this approach are the precision and the lack of consideration of the actual IC configuration made by the end-user (hardware or software).

The IA could also be constructed from the VHDL netlist modeled from a logic synthesis at the RTL level (Register Transfer Level) and using the standard cells libraries that integrates the current consumed by each logic gate for a given fan-out. This approach is faster than a SPICE simulation at the transistor level, because the logic gates are modeled using equivalent current sources. Furthermore, this approach can be coupled to a high level analyze of the chip floorplan to extract an equivalent circuit network [17][18]. Existing tools as ANSYS Redhawk and Sentinel CPM (Chip Power Model) allow the simulation of power integrity and CE including the chip, package and PCB model. These tools are very performant but are not adapted to an end-user when there is no information on the logic operations and the floor-planning [19].

In general, the major issue in the construction of an ICEM model is the extraction of the internal activity. Depending on the IC under test, a special care must be taken to choose the most appropriate methodology for the IA extraction. In this study, a new methodology for the IA extraction will be proposed and verified on a FPGA.

2. Presentation of the circuit under test

Modern digital circuits are an important source of disturbances in electronic systems. The simultaneous switching of hundreds of thousands logic gates enhance the noise generated by the ICs. In this chapter, the study of ICEM-CE model for conducted emission will be presented with a special focus on a new methodology for the extraction of IA. Before introducing the methodology of construction of ICEM-CE, this section is dedicated to the presentation of the circuit under test and the test environment (test boards).

2.1. The circuit under test

In this chapter, we will focus on the construction of an ICEM-CE model of a complex digital component; a Field Programmable Gate Array (FPGA). This choice is justified by the remarkable growth of reconfigurable technologies (FPGAs) since their introduction in 1984. This is due to their ability to perform effective digital processing without giving up on the software flexibility.

This characteristic allows to widen substantially the scope of use of these technologies and to absorb the non-recurring and very high manufacturing costs over a large sales volume. Also, it is possible to test the validity of new architectural concepts; the full implementation of a processor on FPGAs is possible leading to more evaluation possibilities than those offered by software simulators. Furthermore, due to their high volume and relatively straightforward scalability, the FPGAs will face the same underlying reliability issues as other VLSI (Very Large Scale Integration) devices [20]. Reconfiguration is also a main advantage of FPGAs. Modern large devices are able to be reprogrammed in real time during operation and are able to be fault-tolerant using hardware solutions.

The circuit under test is a XC6SLX16-2FT256 from Spartan 6 Xilinx FPGA family, manufactured with a CMOS 45-nm process [21].

The circuit includes 9152 configurable logic blocks (CLB) and up to 186 user IOs. The power distribution network of the FPGA is quite complex since it includes numerous power supply domains:

- **VCCINT**: dedicated to the CLB (1.2 V).
- **VCCOx** (x = 0 to 2): dedicated to the IOs organized in three different banks (3.3 V)
- **VCCO3:** dedicated to the MCB (Memory Control Block) and IOs supplied by 1.5 V and need a reference voltage of 0.75 V
- **VCCAUX**: dedicated to the JTAG configuration (3.3 V)

The circuit is mounted in a Fine pitch Thin Ball Grid Array with 256 balls (FTBGA256) package.

2.2. Description of the test boards

2.2.1 Test board for EMC characterization

In this study, a demonstrator was designed with the following objectives:

- Build and validate EMC models of fresh or aged components, including statistical dispersion.
- Aging components (thermal and electrical aging).
- Predicting the drift of EMC levels related to the aging of the components at the level of an electronic board, as well as the statistical dispersion.

For this purpose, the demonstrator ELECIS-F (**E**lectronic board for **L**ong-term **E**lectromagnetic **C**ompatibility **I**ssues **S**imulation – **F**PGA) has been designed. The ELECIS-F demonstrator is dedicated to EMC characterization of the FPGA, the extraction of data for the construction of the EMC and SI models, and the validation of these models. This demonstrator enables the activation of internal functions of the FPGA in order to characterize the electromagnetic noise produced (transient current, voltage fluctuation), and radiated emission (TEM cell) and also immunity to electromagnetic disturbances.

ELECIS-F also allows the characterization of IOs with different standards (LVCMOS33, SSTL15, DIFF_SSTL15). The FPGA is mounted on the PCB via a socket (Ironwood SG-BGA-6017MF) which allows testing fresh and aged components. The specification of ELECIS-F demonstrator is presented in Figure II-14.

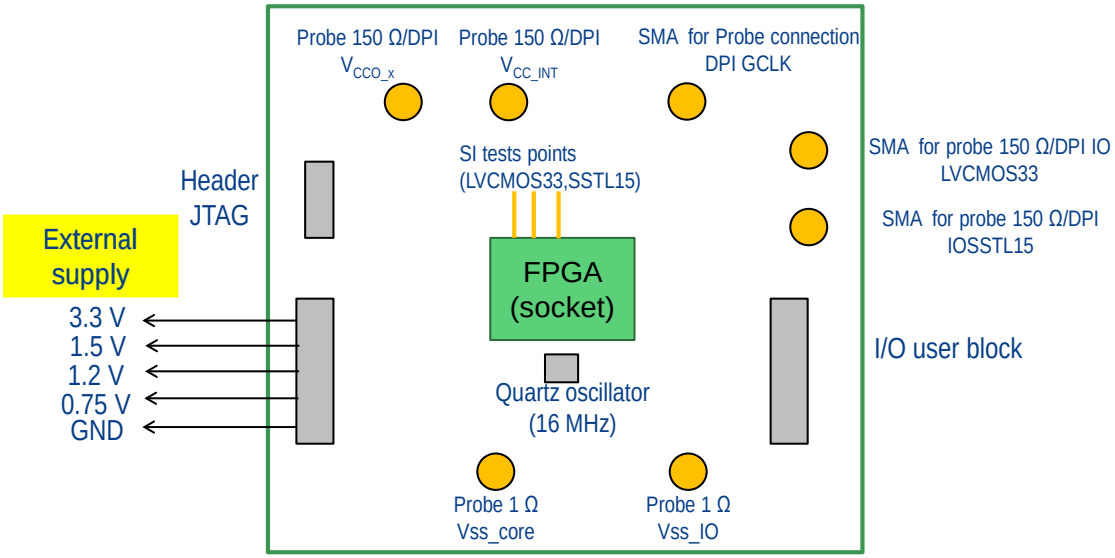

Figure II-14 Block diagram of ELECIS-F demonstrator

The ELECIS-F board has been designed according to 6 layers, 10x10 (cm) and meets the requirements of IEC 61967-1 for measurements in TEM cells. The constructed PCB is shown in Figure II-15, where several test points are provided, as specified, for signal integrity measurements, DPI injection, 150 Ω measurements on power planes and IOs, and the 1 Ω probe is connected directly to the V_{SS} pins of the FPGA. No other active circuit is mounted on the board.

Figure II-15 The designed demonstrator ELECIS-F

2.2.2 Test board for PDN extraction

For the construction of ICEM-CE model of the FPGA, a specific board has been designed in order to perform S-parameter measurements for the construction of the PDN block of ICEM model of the FPGA.

The test board is a 6 layers PCB; the power planes and ground planes are designed similarly to ELECIS-F test board. On the bottom side of the PCB as shown in the Figure II-16 left, GSG (Ground/Signal/Ground) footprints are connected as close as possible to the different power and ground pins and some IOs for S-parameter measurement using a GS probe. Furthermore, footprints of SMD resistors are connected to the ground pins; they allow leaving V_{SS} pins floating when the resistors are not mounted on the PCB in order to extract the parasitic capacitance between VSS pins and the board ground plane (common mode impedance). Otherwise if 0 Ω resistors are mounted, the V_{SS} pins are connected to the ground plane of the PCB. In the top face of the test board for PDN extraction which is presented in the Figure II-16 right, the FPGA is mounted in a HF (High Frequency) socket (SG-BGA-6017MF GHz BGA socket) for testing several components, the socket manufacturer guarantee low values of its parasitic elements; the manufacturer of this socket gives the following parasitic elements information:

- Contact resistance: 25 mΩ
- Inductance: 0.28 nH
- Capacitance to the PCB ground plane: 0.204 pF

Figure II-16 test board for PDN extraction: bottom side (left), top side (right)

3. Construction of an ICEM-CE model of a FPGA

3.1. Experimental protocol for the construction of the PDN model

3.1.1 Description of the experimental protocol

The power distribution network (PDN) component models the characteristics of propagation path of electromagnetic noises; it consists of a passive electrical network that describes the interaction between the different power supplies and ground terminals of an IC, at package and chip level. As presented in 2.2.2, a specific test board was designed for the construction of the PDN of the FPGA. Hence, this board is dedicated to the characterization of the impedance between the power pins and the IOs. As described in Figure II-17, the measurement of S parameters is realized using a 2 ports vector network analyzer (VNA) connected to a GS probing system to avoid the necessary de-embedding phases to minimize the coupling errors that appear from some hundreds of MHz. The FPGA is mounted in a RF socket in ELECIS-F_PDN board similarly to ELECIS-F

board. Although the parasitic elements of the RF socket are very low, they will be automatically integrated in the PDN model of the FPGA.

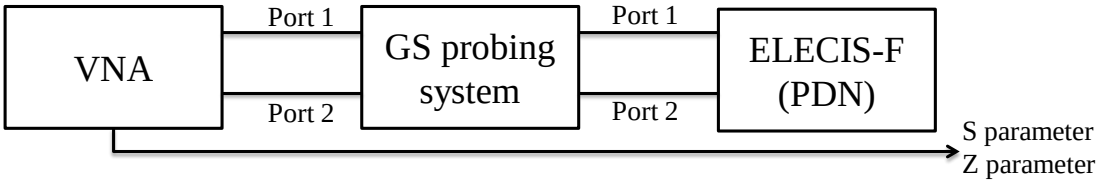

Figure II-17 Description of the workflow for S parameter measurements of the FPGA

The S parameter measurements are performed for different configurations for modeling the multiple parasitic coupling that could increase the noise generated by the FPGA. The selected configurations are:

- S parameter measurements performed directly on the pins of the FPGA as shown in the Figure II-18 (left), this allows the modeling of the parasitic coupling between the different power planes and models the substrate coupling, and the package and die impedance.
- S parameter measurements performed on the dedicated board for PDN extraction as shown in Figure II-18 (right), this allows the modeling of the common mode effect between the circuit and the PCB. Furthermore, all the S parameter measurements are performed when the FPGA is not powered (passive mode) and when it is powered using a bias tee that was designed for this purpose. Figure II-19 describes the test set-up for S parameter measurements with a bias tee test board. The bias tee is included in the system during the calibration phases.

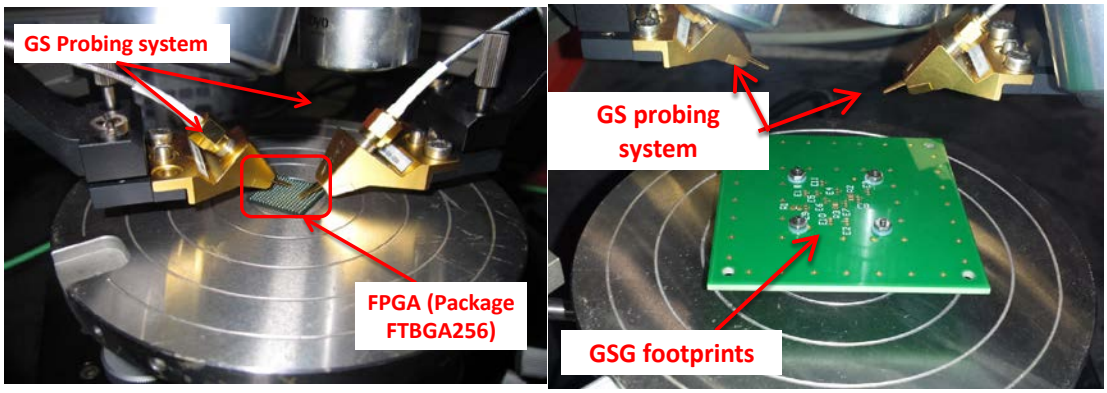

Figure II-18 S parameter measurements with a GS probing system: on the pins of the FPGA (left), on test board for PDN extraction (right)

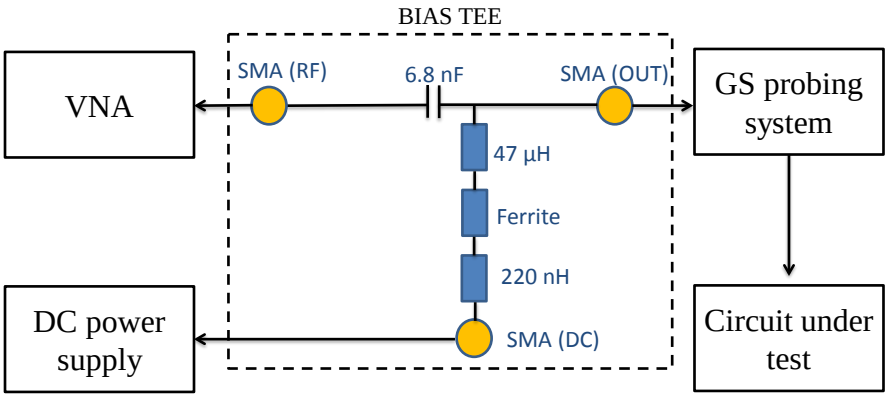

Figure II-19 Set up for S parameter measurements using a bias tee

For the PDN extraction, several pins were selected for S parameter measurements and are connected to GSG (Ground-Signal-Ground) footprints on the bottom face of ELECIS-F_PDN board as close as possible from the FPGA area. The selected pins allow the characterization of the different power and ground pins and some IOs; they are summarized in the Table II-1. During the S parameters measurements, all the combinations between the selected pins were characterized. Hence, the S parameters measurements were performed between:

- The pins of different power domains
- The different ground pins
- The power and ground pins
- The power pins and the IOs
- The ground pins and the IOs

Symbol	Pin	FPGA area
VCC0	B4	Power domain 3.3 V
VCC1	J15	Power domain 3.3 V
VCC2	R4	Power domain 3.3 V
VCC3	K4	Power domain 1.5 V
VCCINT	G7	Power domain 1.2 V
VCCAUX	E5	Power domain 3.3 V
VSSIO1	B11	IO ground domain
VSSIO2	R6	IO ground domain
VSSCORE	J8	Core ground domain
IO1	F1	Standard IO Bank 3
IO2	E16	Standard IO Bank 1

Table II-1 Selected pins for S parameter measurements

In this study, we will focus on the measurements obtained between the different power and ground pins. The model will not include the parasitic elements of the IOs. As presented, only one pin was selected for each power and ground plane to optimize the number of measurements since the FPGA contains 26 ground pins, 8 VCCAUX pins, 8 VCCINT pins, 5 VCC0 pins, 6 VCC1

pins, 4 VCC2 pins and 5 VCC3. The constructed model per power and ground plane will be considered as an equivalent model for all the pins.

3.1.2 Experimental results

The S parameter measurements performed on the ELECIS-F_PDN board allows the modeling of the common mode effect between the package and the PCB. This is possible with the 0 Ω resistors that can be connected or disconnected between the VSS pins of the FPGA and the ground of the PCB. Figure II-20 shows the measured impedance Z11 on the power plane VCC3 when the VSS pins are opened and when they are shorted to the ground of the PCB. The Figure shows an equivalent circuit capacitance of 549 pF between the power plane VCC3 and the ground plane when the VSS are shorted to the PCB ground. A capacitance of 134 pF is measured when the VSS are opened. It is induced by the common mode effect. At the package level, each IO has a parasitic capacitance around 1 pF, furthermore, the IOs are floating in ELECIS-F_PDN, and each IO presents a parasitic capacitance with the ground pins of 5 to 6 pF. With 186 users IO in parallel a total parasitic capacitance between the IOs and the VSS pins is nearly 134 pF, which explain the appearance of the common mode capacitance.

The measurement system was carefully calibrated before all the S parameter measurement and validated by measuring the impedance of known passive elements; the noise shown in the Figure II-20 below 1 MHz is due to the sensitivity of the VNA. This will have no impact on the construction of the PDN of the FPGA.

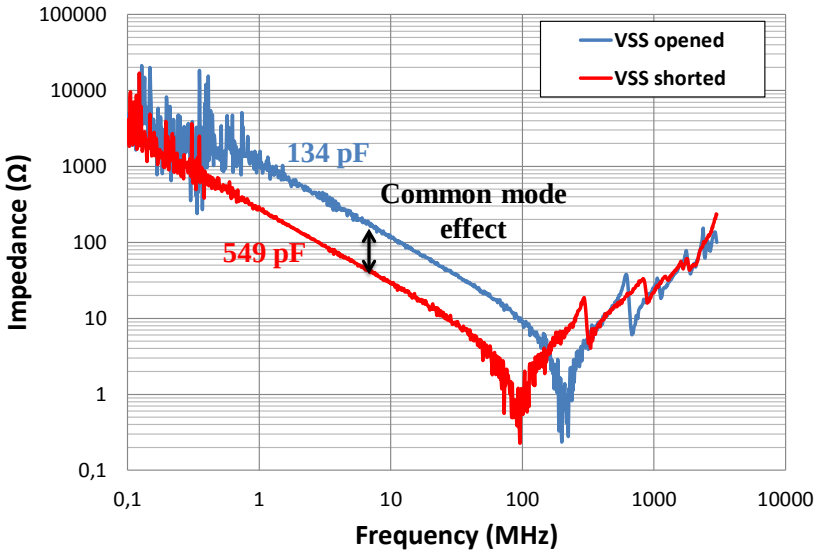

Figure II-20 Measured impedance Z11 on VCC3 when the VSS are opened and shorted

The measurement of the parameter S21 when the two ports of the GS probing system are set on the same power pin of the FPGA allows the evaluation of the die capacitance at low frequencies. However, depending on the polarization of the FPGA, the die capacitance value could change because the chip has several reversed PN junctions; the Nwell capacitor is the reversed biased PN junction capacitor between the Nwell and P-substrate. The Figure II-21 presents the measured impedance Z21 on powered and unpowered FPGA when the two ports of the GS probing system

are set either on the VCC0 power pin (left) or on the VCCINT power pin (right). In the case of the VCC0 power plane, the capacitance calculated at low frequencies increases from 665 pF when the FPGA is unpowered to 1.075 nF when it is powered. Also, the measured low frequency capacitance on VCCINT increases from 17.5 nF when the FPGA is unpowered to more than the double value of 37.5 nF when it is powered. The same measurements and ascertainments were accomplished on the other power pins. These values must be carefully integrated in the PDN model of the FPGA to correctly estimate the noise generated by the circuit with the ICEM-CE model

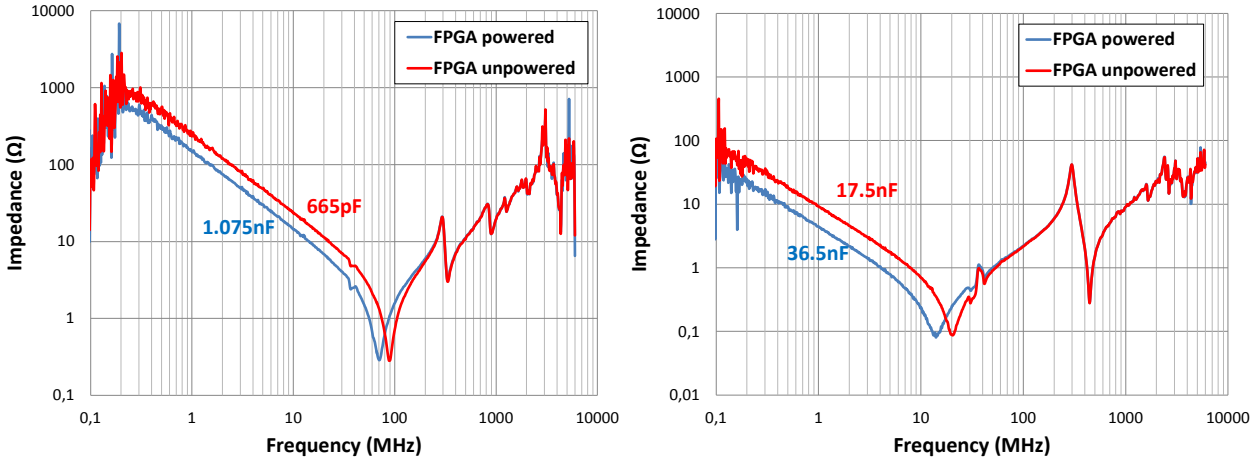

Figure II-21 Measured impedance Z21 on power and unpowered FPGA when the two ports are: VCC0 (left), VCCINT (right)

As presented previously, the S parameter measurements are also performed directly on the package. The reference of the measurement is set on the closest VSS pin of the FPGA. The Figure II-22 shows a comparison between the measured impedance Z21 on board and on the package when the port 1 of the GS probe is on the power plane VCC1 pin and the port 2 is on the VCC3 pin. The measured impedance on board was performed when the VSS is shorted to the ground plane of the PCB so that the reference of the measurement could be approximately on the VSS pins. This comparison shows the differences between the measured impedances from 2 MHz. The measurement performed on the package will allow the modeling the parasitic coupling between the different power planes. The impedance measurements on the package are influenced by the parasitic capacitance between the different power domains and also by the equivalent capacitance between the power domains and ground pins and the package inductance at high frequencies. The Table II-2 summarizes some of the parasitic elements of the FPGA deduced from measurements.

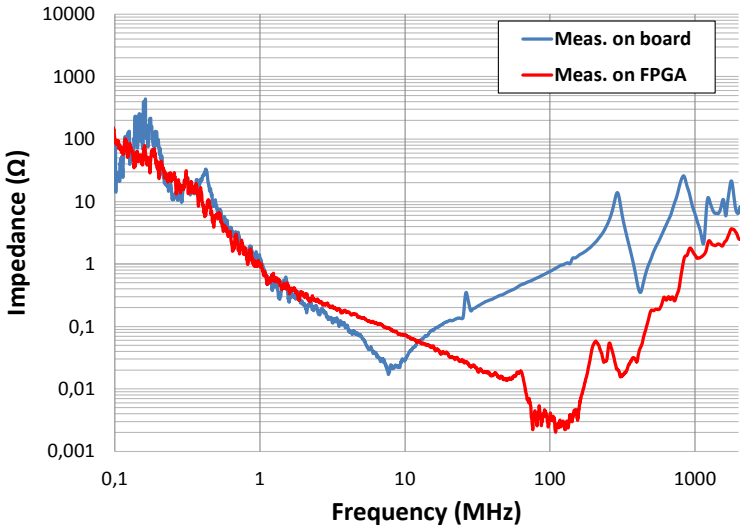

Figure II-22 Measured impedance Z21 on board and directly on the FPGA package when the port 1 is on VCC1 and the port 2 on VCC3

	Domain	Value	
		Unpowered	Powered
On-chip capacitance	VCC0	665 pF	1.075 nF
	VCC1	472 pF	776.8 pF
	VCC2	670.38 pF	1.049 nF
	VCC3	526.21 pF	897.5 pF
	VCCAUX	3.38 nF	5.42 nF
	VCCINT	17.5 nF	36.5 nF
Common mode capacitance		134 pF	
Package inductance	Power pins	0.1 nH	
	Ground pins	0.4 nH	
Package resistance		37 mΩ	

Table II-2 Parasitic elements of the FPGA

3.2. Construction of the PDN model

3.2.1 Description of the PDN model of the FPGA

The construction of the PDN model of the FPGA depends not only on the S parameter measurements but also on the internal structure of the circuit which could help identifying the topology of the PDN model [25]. The different elements of the circuit induce parasitic elements that will contribute on the measured impedance. For this purpose, the internal structure of the FPGA package has been analyzed with a 3D X-ray scanner by Continental Automotive, as shown in the Figure II-23. This analysis provides valuable information for IC modeling, such as the routing of power supply and ground at package level, presence of inner ground plane, die dimensions, number of bonding wires… In the X-ray image, the layer 2 is composed of a ring-

shaped plane that connects the VSSIO pins related to ground pins of the IO banks and a central plane connecting the VSSCORE pins related to the ground pins of the core of the circuit. After a thorough analyze of the layer 2, we have found 2 thin traces connecting the VSSIO domain to the VSSCORE domain. This induces a parasitic inductance between the internal ground planes. On the layer 1, we can see a central plane connecting the different pins of the power domain VCCINT. This domain is surrounded by ring-shaped track connecting the VCCAUX pins, and finally, several distributed traces connecting each power domain that supplies the IO banks. With the X-ray image we can also see that the die is connected to the internal 2 layers PCB through bonding wires. The die dimensions are 5.2 x 5.2 mm.

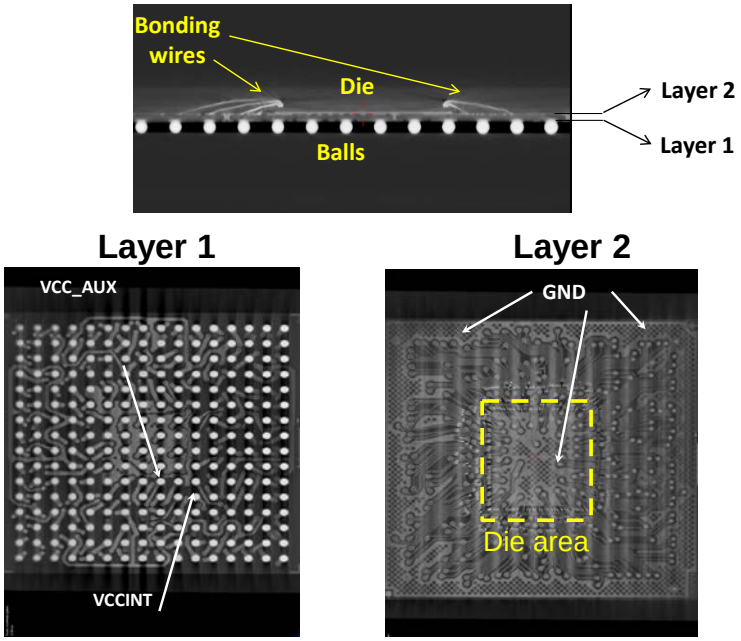

Figure II-23 X-ray images of the FPGA mounted on FTBGA256

Since the manufacturer of the FPGA Xilinx does not provide any equivalent model, the PDN model will be constructed following the workflow described in the Figure II-24. From the acquired details on the internal structure, a PDN model structure will be defined with a number of unknown values. From the impedance computation, a linear system can be solved regarding to the measured impedance to obtain the values of the RLC equivalent circuit. A comparison between the simulated and measured impedance on the different power and ground domains will allow either the validation of the PDN model or the modification of the proposed structure.

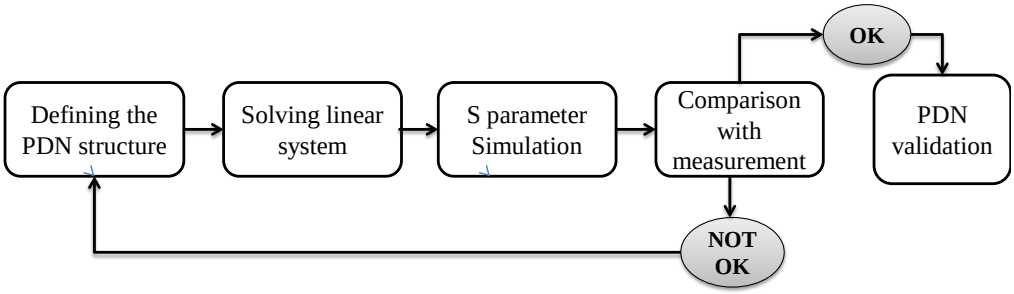

Figure II-24 Workflow of construction of the PDN model

After several system resolutions and fitting the values of the RLC elements with the S parameter measurements, an equivalent PDN model was proposed that describes all the parasitic coupling between the different power and ground domains. To analyze the PDN model, Figure II-25 presents a simplified view between the VCC0/VSSIO and the VCCINT/VSSCORE. The different elements of the PDN model are:

- Package model: represented by an inductance for the different power domains and by a RL circuit for ground rails. And the bonding wires model represented between the substrate and the ground pins by a RL series circuit.
- Die equivalent model: represented by a RLC series circuit between the power domains and the ground rails.
- Parasitic coupling between power domains: modeled by a parasitic capacitance.
- Substrate coupling: the parasitic elements induced by the substrate coupling are modeled using a RC parallel circuit
- Common mode effect: the equivalent capacitance of 134 pF induced by the common mode effect is distributed to the different power and ground domains.
- Ground domain coupling: the parasitic coupling between VSSCORE and VSSIO ground domains are represented by an inductance.

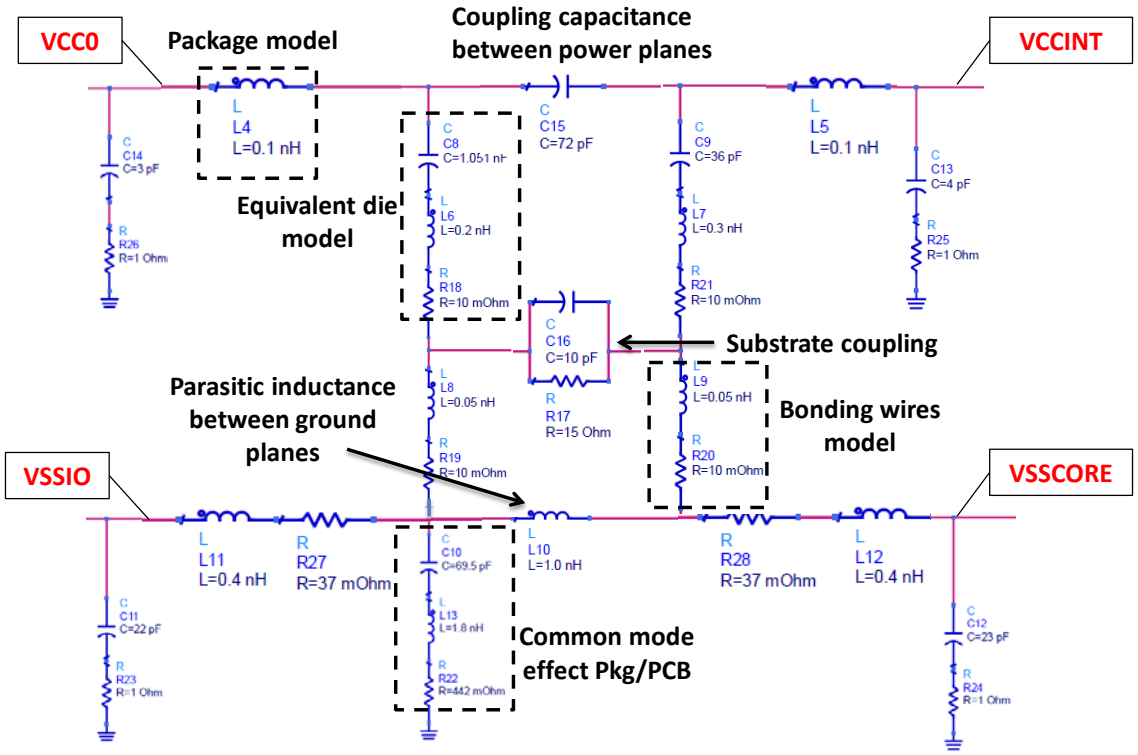

Figure II-25 Simplified view of the PDN model between VCCO/VSSIO and VCCINT/VCCINT

Figure II-26 presents the constructed PDN of the FPGA showing the different power and ground domains equivalent model.

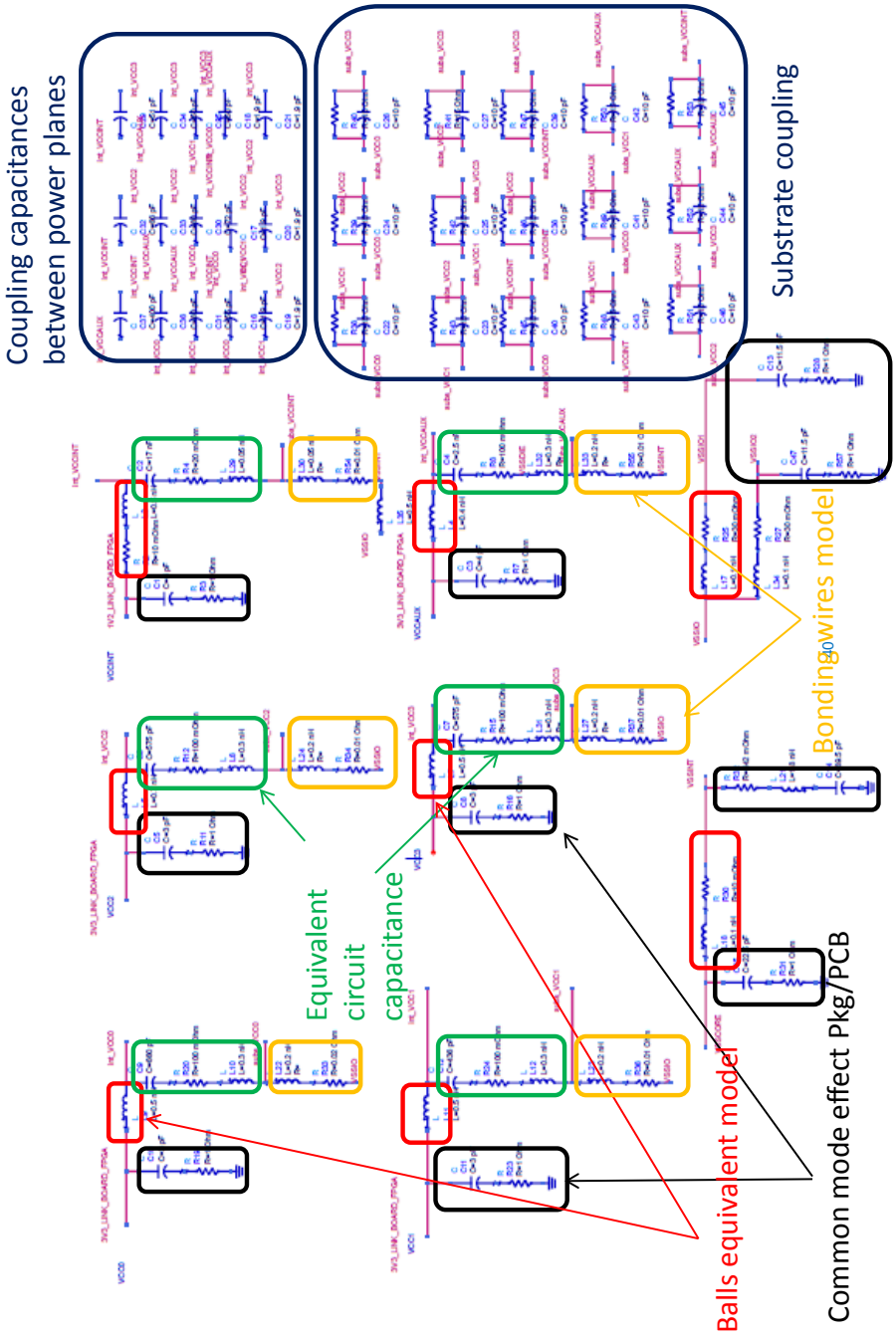

Figure II-26 General structure of the PDN of the tested FPGA

3.2.2 Validation of the PDN model

The constructed PDN model of the FPGA is integrated in the SPICE simulator Advanced Design System (ADS). Several validation cases were studied. Figure II-27 presents the comparison between the measured and simulated Z11 impedance of the power domain VCC0 when the VSS pins are opened and when they are shorted the ground of the PCB. The simulation results show that the constructed PDN is valid up to 2.5 GHz.

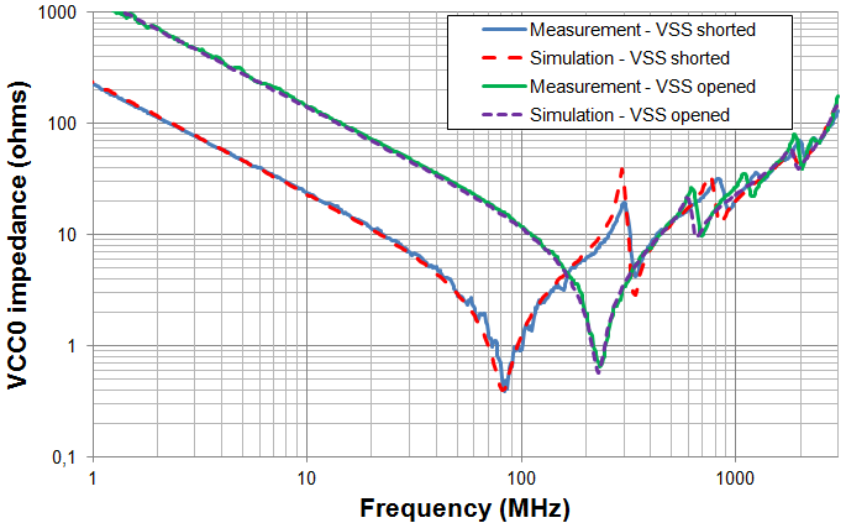

Figure II-27 Comparison between the measurement and the simulation of the impedance Z11 of VCC0 when the VSS are opened and when the VSS are shorted

Furthermore, the parasitic elements values that reproduce the coupling between the different power planes are validated. Figure II-28 shows a comparison between the measurement and simulation, performed directly on the FPGA and its PDN model, of the impedance Z21 when the port 1 is VCC1 and the port 2 is VCC3. The comparison shows a good correlation between the measurement and the simulation up to 2 GHz.

Similarly to the presented validation case, the PDN model of the FPGA was verified for the different power supply and ground domains. This is a primordial verification to ensure the construction of a reliable ICEM-CE model for the prediction of the conducted noise generated by the FPGA.

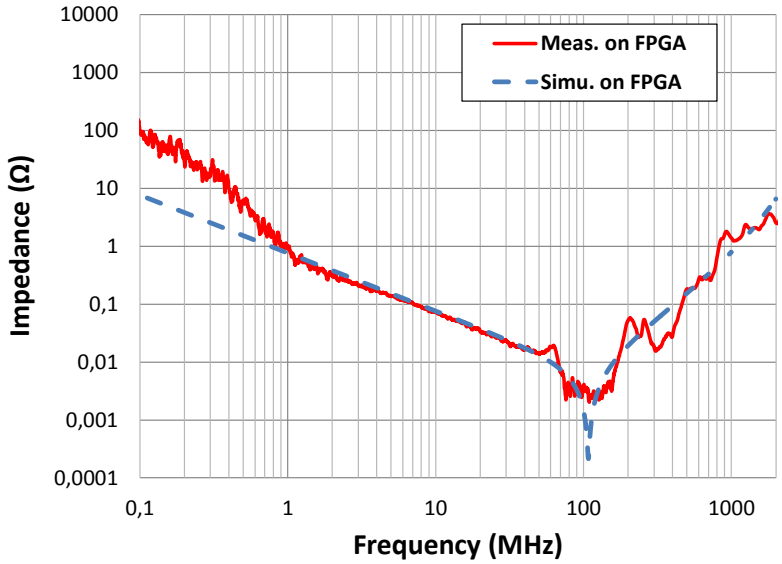

Figure II-28 Comparison between the measurement and simulation performed on the FPGA of the impedance Z21 when the port 1 is VCC1 and the port 2 is VCC3

3.3. Modeling of ELECIS-F board

3.3.1 Construction of ELECIS-F board equivalent model

The conducted emission measurements are performed on ELECIS-F board that integrates a 1 Ω probe connected directly to the VSS pins of the FPGA. The CE model must take into account the environment of the integrated circuit, in particular the PCB model that could have an important impact on the noise generated by the IC. In general, design files (ODB…) are accepted by EM simulators to create the 3D geometric model. As shown in Figure II-29, the 3D simulation generates the S/Z parameters and allows the extraction of a black-bloc macro-model that could be integrated into a SPICE simulator.

Figure II-29 General methodology for the PCB modeling

The board modeling is performed using the electromagnetic simulation software CST Studio Suite. The board model is created by importing the design files (ODB++) on the CST PCB module; this module support layout from different design tools (Cadence, Zuken, Altium). For the PCB model generation, all the coupling capacitors and the resistors of the 1 Ω probe are defined on the simulator as lumped elements taking into account their parasitic elements. For the S parameter simulation, 10 discrete ports are defined as shown in Figure II-30:

- Four ports are placed on the measurement points. SMA connectors are connected to the power planes (1.2 V / 3.3 V) and the 1 Ω probe where the S parameter measurements are performed for the PCB model validation.
- Six other ports are placed as close as possible to the FPGA area on the power planes (1.2 V / 3.3 V / 1.5 V) and on the VSS pins. In ICEM-CE model, these ports will be connected to the PDN model of the FPGA.

Table II-3 summarizes the ports definition on the CST simulator.

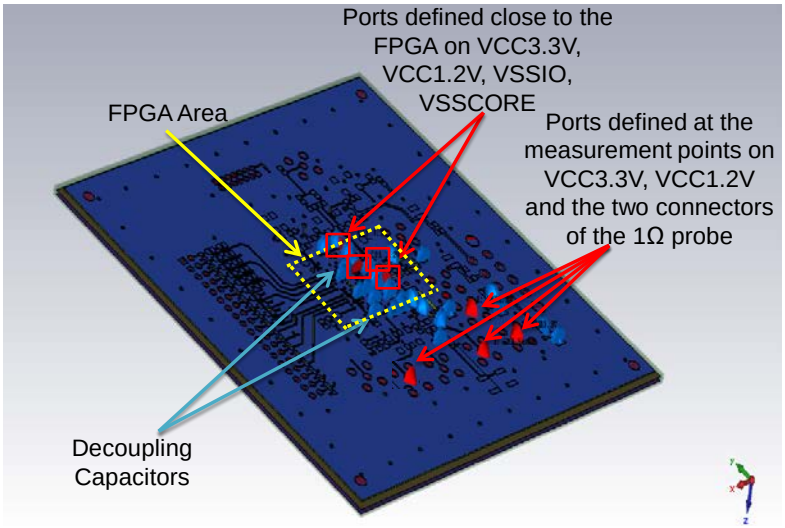

Figure II-30 ELECIS-F modeling with CST Studio Suite

Port number	Definition
P1	SMA P11 (3.3 V)
P2	SMA P14 (1.2 V)
P3	SMA P15 (1 Ω probe)
P4	SMA P9 (1 Ω probe)
P5	FPGA area (3.3 V)
P6	FPGA area (1.2 V)
P7	FPGA area (VSSCORE)
P8	FPGA area (VSSIO1)
P9	FPGA area (VSSIO2)
P10	FPGA area (1.5 V)

Table II-3 Ports definition for ELECIS-F modeling

CST Studio Suite includes several modules (PCB, Microwave …) that could be used according to the application domain. These modules offer the possibility for 2D/3D simulations using different solvers. For the ELECIS-F board modeling, four different solvers were tested and the S/Z parameters results were compared to the measurement to identify the most adapted method for the board model extraction.

- The transient simulator in CST MWS (Microwave Studio) is a very performant solver that delivers broadband frequency results. This solver is based on Finite Integration technique (FIT) which is a consistent discretization scheme for Maxwell's equations in their integral form. This real time simulator is commonly based on the hexahedral meshing technique which discretizes the geometric model into different regions for a volume meshing based on rectangular cuboids. The geometric model created on CST PCB Studio can be imported to CST MWS with the specified stack-up, ports and lumped elements definition (decoupling capacitors, 1 Ω probe…). Although this solver gives accurate results when the number of discrete ports is low, in the case of ELECIS-F board, the S parameters simulation for 10 discrete ports and more than 30 decoupling capacitors and a fine volume

meshing has last for several days even using a GPU (Graphic Processor Unit) for acceleration features.

- Frequency domain solver in CST MWS is based on the Finite Elements Method (FEM). It allows two different meshing techniques; hexahedral meshing as for the transient solver and a tetrahedral meshing technique. The main difference between the frequency and time domain solvers is the number of frequency sampling; in the time domain the sampling has no influence on the simulation duration whereas in the frequency domain the number of frequency samples will influence the simulation time since the solver perform the computation for each sample. Hence, using this solver has led to a long time simulation and reducing the frequency samples decreases the results accuracy.
- 3D PEEC (Partial Element Equivalent Circuit) solver in CST PCB Studio uses a quasi-static technique and generates a SPICE circuit for the selected nets for EM simulation by dividing them into partial elements. This solver was tested on ELECIS-F board and does not give accurate results while comparing them to the S parameter measurements. This is not surprising since the 3D PEEC solver is set for EM simulation on single and two layers board and is only valid on low and medium frequency ranges.
- The 3D FE FD (Finite Element Frequency Domain) solver in CST PCB Studio is based on the Finite Element Method (FEM) was chosen for the board modeling because it is capable to accurately analyze the entire PCB design and is completely adapted to a multi-layers board. The frequency domain solver includes a special meshing engine optimized for PCBs, which allows complex boards to be simulated faster than conventional methods. The number of mesh cells reaches 5,2M meshes, and the simulation lasts 30 minutes using a GPU (NVIDIA K40C) for the frequency range 10 KHz – 2.5 GHz. After the S parameter simulation, CST design module allows the generation of a black box macro-model based on S10P touchstone file that contains the simulation results.

Figure II-31 presents a comparison between the measurement and the simulation of the impedance when the port 1 is defined on the power plane 1.2 V and the port 2 on 3.3 V, and between the SMA connectors P15 (port 3) and P9 (port 4) defined on ELECIS-F as shown in Figure II-32. The comparison shows a good correlation between the measurement and simulation up to 2.5 GHz, but some differences could be noted between the measured and simulated anti-resonance of Z11 and Z22. A difference of almost 100 MHz for Z11 and 50 MHz for Z22 is shown in Figure II-31 and could be due to several simulation parameters; as the equivalent circuit definition of the decoupling capacitors, or even the board design parameters (stack-up, material…). The raised differences could have an impact on the internal activity extraction especially when using the inverse method as shown previously.

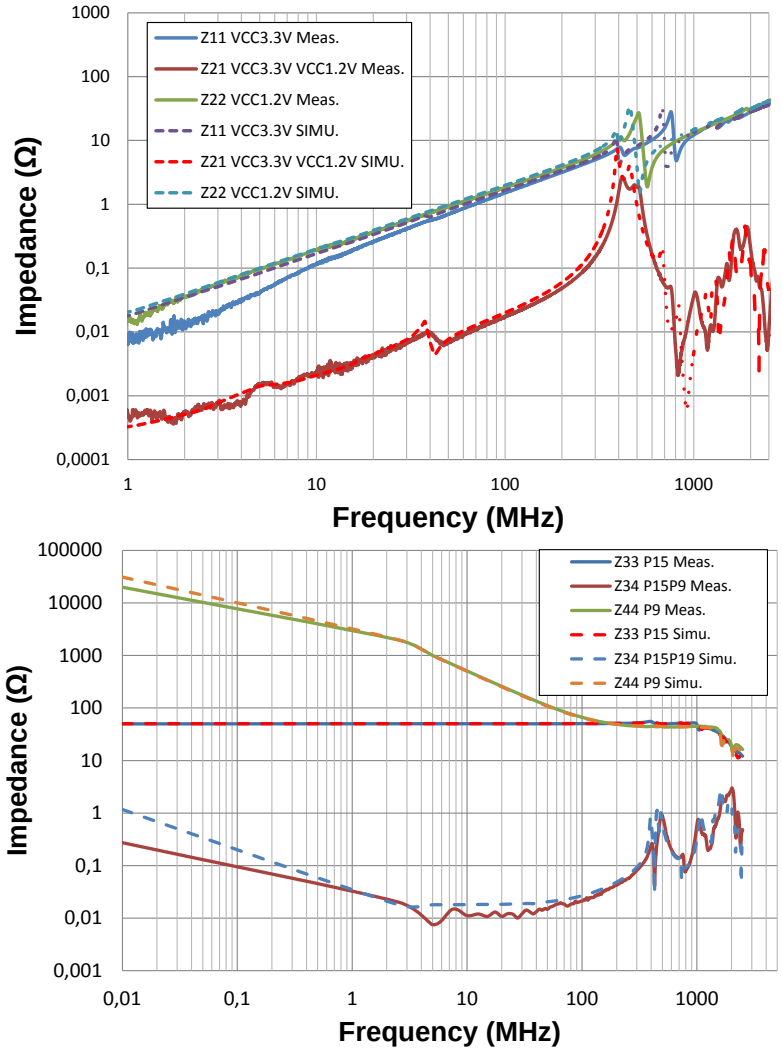

Figure II-31 Comparison between the measured and simulated impedance between 3.3 V and 1.2 V (up) and between P15 and P9 (down)

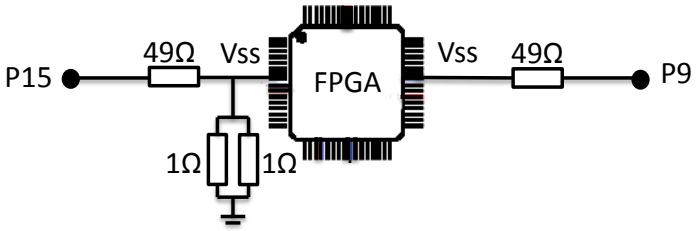

Figure II-32 Definition of the SMA connectors P15 and P9 on ELECIS-F

3.3.2 Validation of the board and PDN model

In the SPICE simulator ADS, the model of the board ELECIS-F is included as a S10P file, then, connected to the PDN model of the FPGA. To validate the constructed models of the board and the FPGA, S parameter simulations are performed on the port defined for the SMA connectors as shown in Figure II-33.

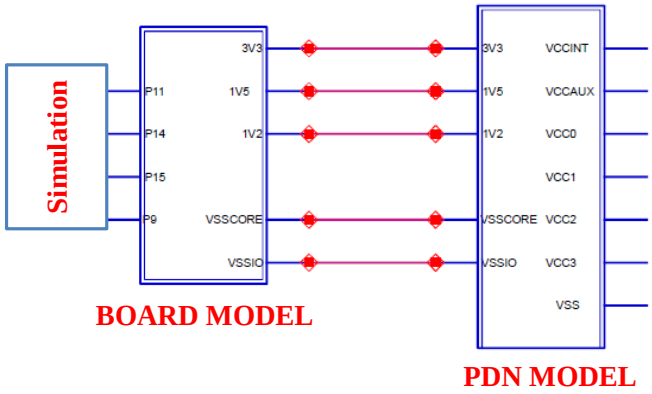

Figure II-33 SPICE model for S parameter simulation on ELECIS-F and the FPGA equivalent model

The S parameter simulation of the board and PDN model is compared the measurement when the port 1 is defined on the power plane 3.3 V and the port 2 on 1.2 V. Figure II-34 shows a good agreement between the measurement and simulated impedance between 2 MHz and 2.5 GHz. Below 2 MHz, some differences can be noted. This can be due to measurement error due to the sensitivity of the VNA or to the extracted PDN model.

Several comparisons between the measurement and the simulation of the impedance between the power planes and the ground planes were studied for the validation of the constructed model.

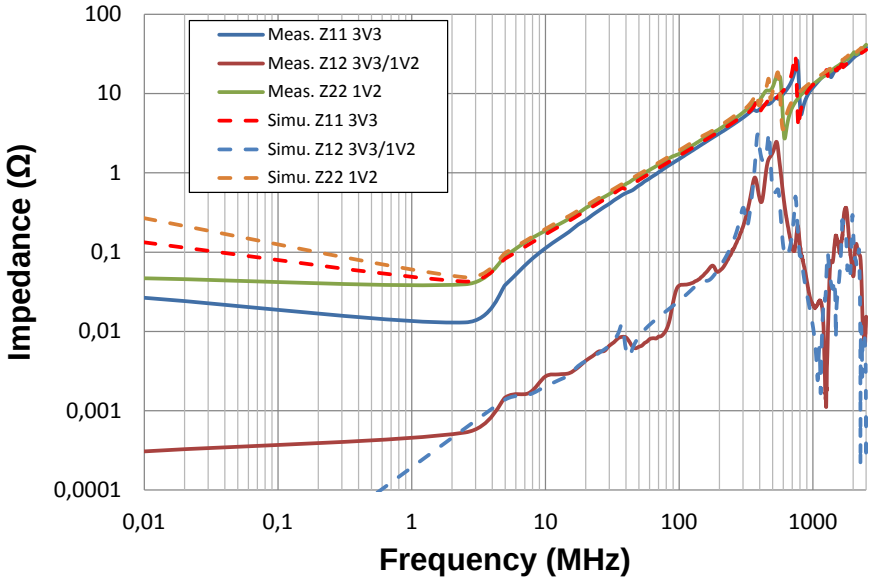

Figure II-34 Comparison between the measured and simulated impedance of the board and PDN model between the power planes 3.3 V and 1.2 V

3.4. Construction of the internal activity of the FPGA

3.4.1 Description of the sources of internal activity of the FPGA

In the standard IEC 61967-4 [23], the IA construction is based on voltage and/or current measurements in time domain at PCB level produced by the FPGA activity. If the transfer function between the measured current or voltage and the IA component is known, the IA current can be computed. However, in a complex IC such as the FPGA under test, numerous separated

internal blocks are activated and are associated to different IA components. The main contributors to the noise generated by the FPGA are presented in Figure II-35 and they are:

- **The core**: the activation of the internal logic blocs induces transient current consumption, which circulates between power and the ground rails. In the ICEM-CE model a specific IA bloc must be constructed to reproduce the noise generated by the core of the IC, which depends on the number of activated Configurable Logic Blocs (CLB), their implementation and routing in the die of the IC. In this manuscript, the internal activity of the core will be named IA Core.
- **The IOs**: the switching activity of the IO drivers is an important source of noise that the FPGA could generate. The noise generated by the IOs depends on the number of switching IOs, the type of standard used (e.g. LVCMOS33, SSTL15…), the configuration of the IOs (slew rate, drive current…) and the internal and/or external load. In the standard IEC 62433-2 [24], there is no recommendation for the construction of the IA block that reproduces the noise generated by the IO. However, in this chapter, a methodology of construction of the IA IO will be proposed.

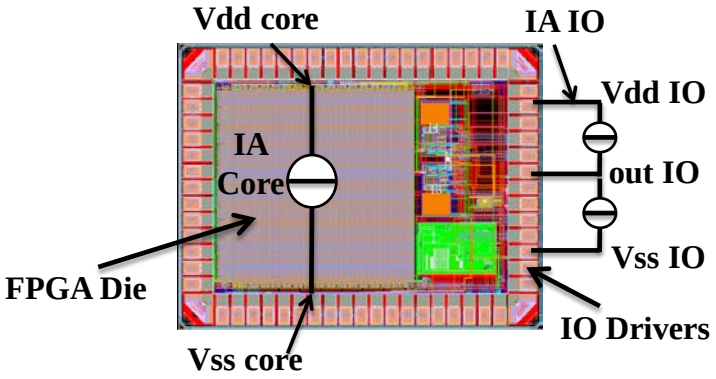

Figure II-35 Regions of the internal activity of a FPGA: Core and IOs

3.4.2 Construction of the IA core using the inverse method

3.4.2.1 IA Core construction

The approach of construction of the IA core in this paragraph is based on the inverse method based on 1 Ω measurement described in [23] and mentioned in 1.3.3.2. The purpose of this methodology is described in Figure II-36. It consists on the measurement of the external current I_{EXT} or voltage V_{EXT} measurement with the 1 Ω probe. The measurement of $V_{EXT}(t)$ is performed in the time domain using a digital oscilloscope because it gives the phase information of the signal, which is not present with a spectrum analyzer. The measurement is then converted to the frequency domain $V_{EXT}(f)$ with a FFT. In a SPICE simulator, the transfer function H(f) between the internal current and the external voltage is obtained with an AC simulation on the PDN model and the board model (including the 1 Ω probe model). Finally, the core internal current $IA_{Core}(f)$ can be computed using the formula II-11 and converted to the time domain using an inverse FFT.

$$IA_{Core}(f) = V_{EXT}(f).H^{-1}(f) \quad \text{(II-11)}$$

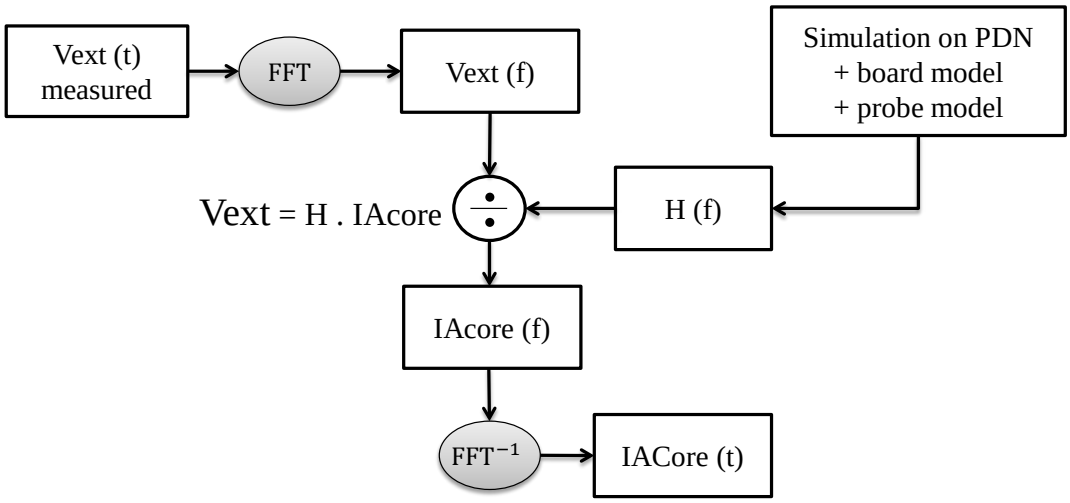

Figure II-36 Workflow of construction of the IA Core using the inverse method

This algorithm will be applied on a specific configuration: a delay line as presented in Figure II-37. For optimum dynamic power consumption, 90 delay lines have been cascaded in series, each delay line has N = 100 inverters. Due to its regular structure, its dynamic power consumption is regular; i.e. the number of switching gates remains identical at each clock transition. The clock frequency is set to 16 MHz. Furthermore, a multiplexer is added at the end of the delay lines to activate or deactivate the output buffer. Thus, we can remove the noise produced by the output buffer switching, which is significant. In this section, no IO is switching, only the activity of the core is generated.

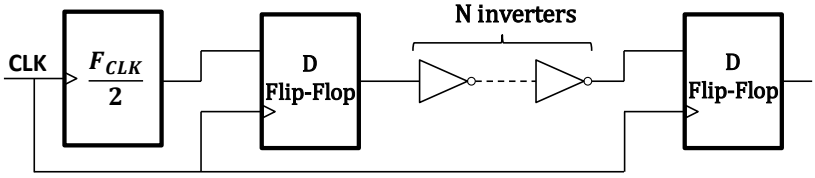

Figure II-37 Structure of the test configuration: Delay lines

The measurement of the external voltage using the 1 Ω probe is presented in Figure II-38, its amplitude is 11 mV peak to peak. In this measurement no filter was applied in the digital oscilloscope. The measurement shows the generation of two superposed noise: the clock activity that occurs with a period of 31.25 ns (32 MHz) because the clock buffers drives current on both the rising and the falling edges, and the activity of the Core (CLBs) which occurs every 62.5 ns (16 MHz) because the CLBs are switching every rising edge of the clock.

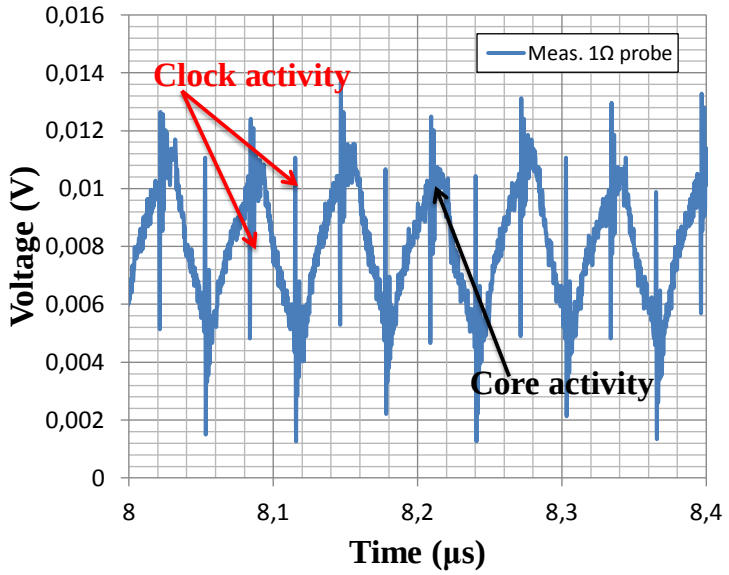

Figure II-38 Measured external voltage using the 1 Ω probe for the test configuration: Delay lines

To compute the internal current for this configuration, an AC simulation is performed on the PDN and the board model as presented in the Figure II-39, in order to compute the transfer function H between the internal activity and the external current. Considering the equation II-2 and the IA_{Core} = [1,0]A, the simulation external voltage on the 1 Ω probe will be equal to the transfer function H. the Figure II-40 presents the magnitude and the phase of the transfer function.

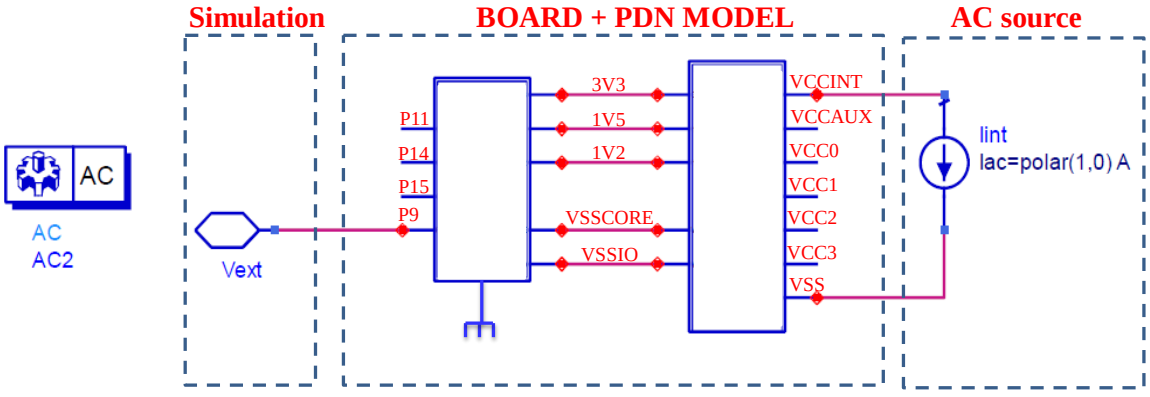

Figure II-39 Schematic for AC simulation to compute the transfer function

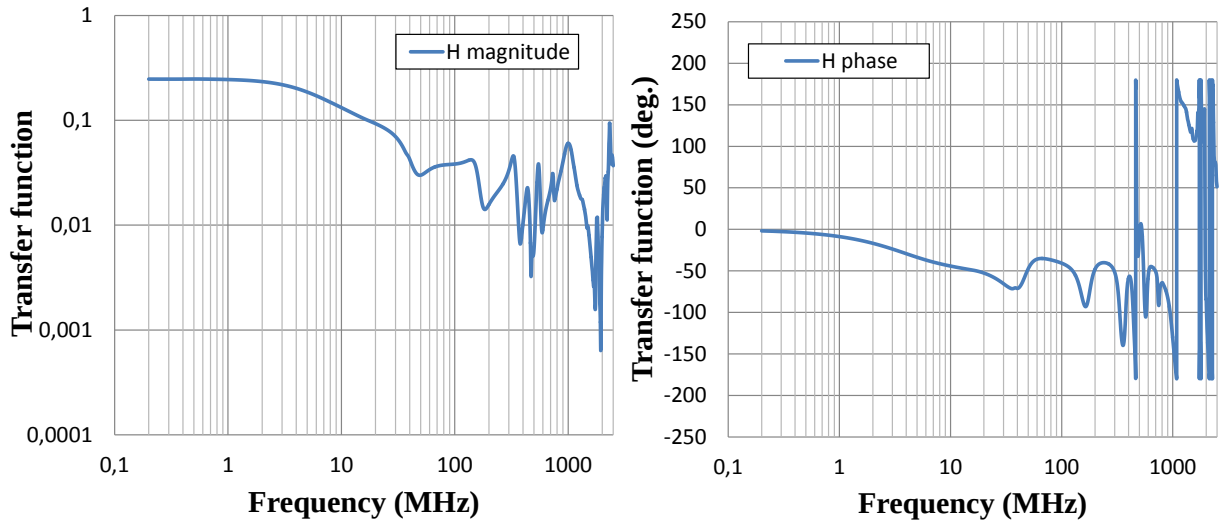

Figure II-40 The obtained magnitude and phase of the transfer function by AC simulation

The described inverse method for extraction of the IA Core with 1 Ω measurement is applied using the measured external voltage and the simulated transfer. Figure II-42 shows the computed IA Core in the time domain. The peak to peak amplitude is 450 mA. Figure II-42 shows the contribution of signals at 16 MHz and 32 MHz and a HF noise can be seen in the zoomed signal in Figure II-42. A FFT was computed to the extracted IA Core and is presented in Figure II-43 where it is clear that HF noise was not compensated and could be seen in the frequency range 350 MHz to 2 GHz.

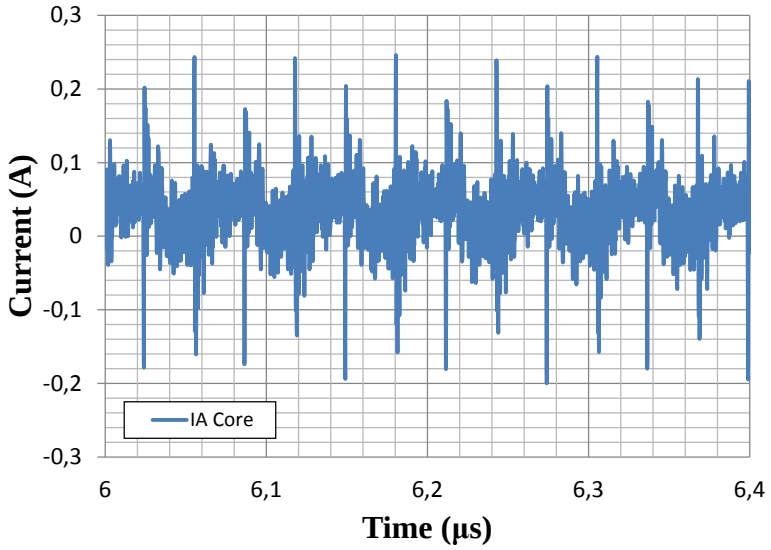

Figure II-41 The extracted IA Core for the configuration delay lines using the inverse method based on 1 Ω measurement

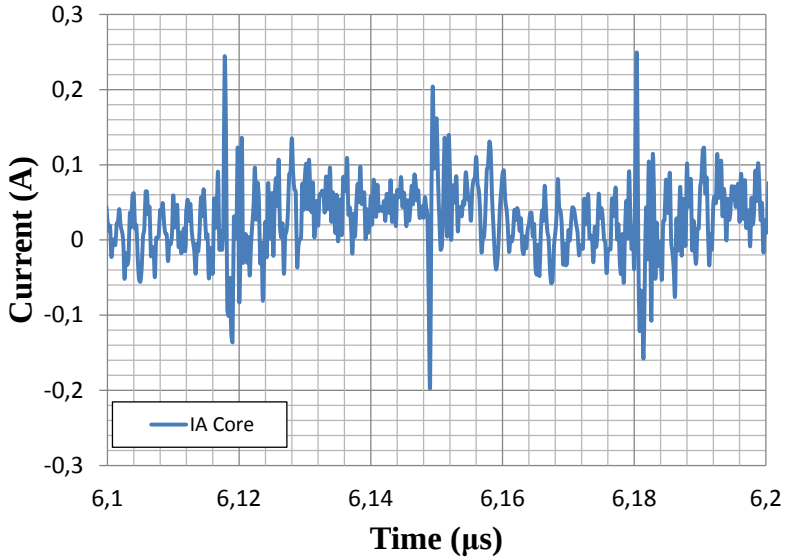

Figure II-42 Zoom on the extracted IA Core using the inverse method in the time domain

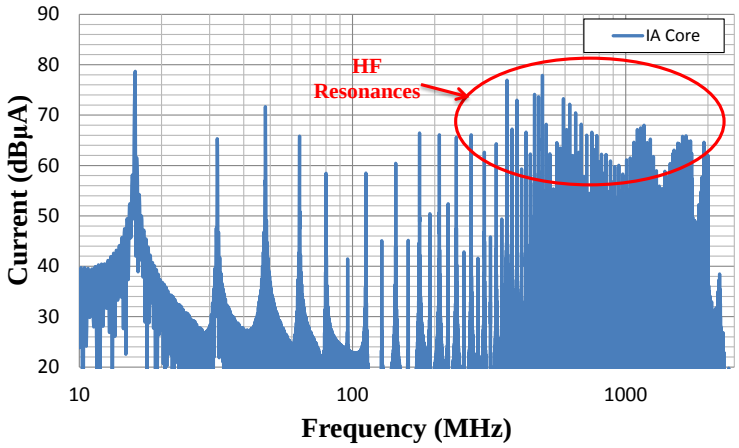

Figure II-43 The extracted IA Core for the delay lines configuration in the frequency domain

3.4.2.2 Validation of the IA Core

The constructed IA Core is then integrated to the board ELECIS-F model and the PDN model of the FPGA as a current source for the validation of the ICEM-CE model. A transient simulation is performed on the port corresponding to the SMA connector P15 connected to the 1 Ω probe as described in the Figure II-44. A comparison between the measured and simulated external voltage using the 1 Ω probe in the time domain is given in Figure II-45. The peak to peak amplitude of the simulated voltage is 10 mV and presents a good agreement with the measurement. Obviously, this result was expected since the construction of the IA Core is based on the external voltage measurement and the PDN model. As seen in the Equation II-11, the simulated voltage with the 1 Ω probe is obtained by multiplying the extracted IA Core and transfer function H; yet, IA Core was extracted using H^{-1}. Hence, the influence of the errors induced by the transfer function H is compensated. The small error is only due to the measurement random error on the external voltage.

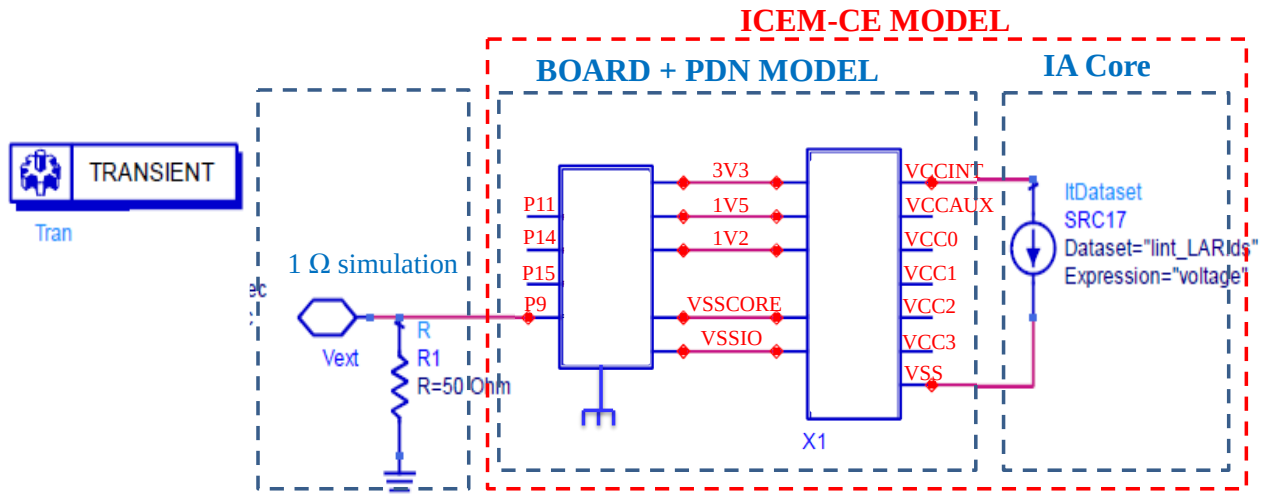

Figure II-44 Constructed ICEM-CE model for transient simulation using a 1 Ω probe

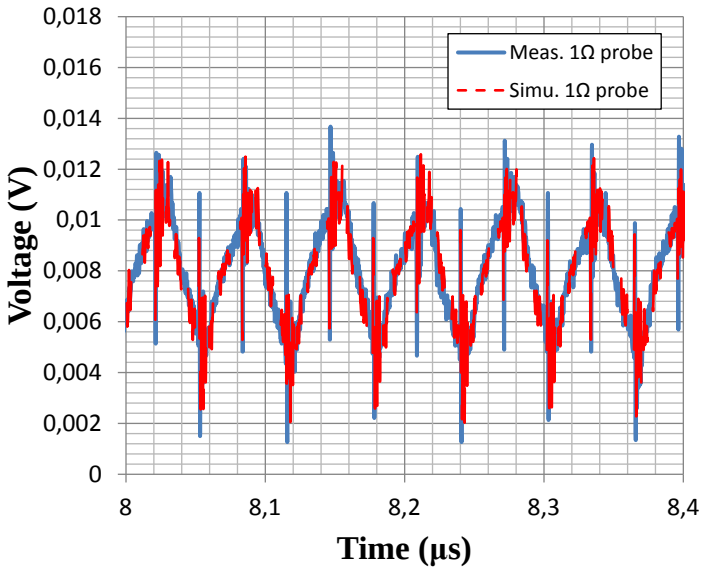

Figure II-45 Comparison between the measurement and the simulation in the time domain of the external voltage using the 1 Ω probe

The Figure II-46 presents a comparison of the spectral envelope in the frequency domain between the measured and simulated voltage using the 1 Ω probe. The comparison shows a good agreement between the measurement and the simulation up to 2.5 GHz with a RMS error of 5.27 dBµV calculated between 16 MHz and 2 GHz, above this frequency range, the CE measurement is close to the measurement system noise floor. Then, all the RMS errors for CE measurement using 1 Ω probe are calculated up to 2 GHz in this chapter. The correlation is good for the same reason explained previously in the time domain comparison.

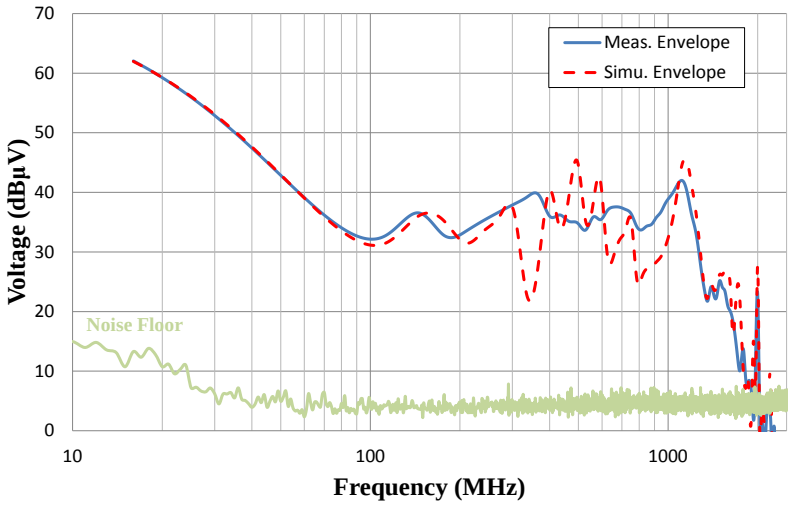

Figure II-46 Comparison of the measured and simulated envelope in the frequency domain of the external voltage using the 1 Ω probe

For the verification of the constructed IA Core, a transient simulation using a 150 Ω probe on the power plane 1.2 V was performed. The 150 Ω probe was designed in a specific board and characterized by S parameter measurement using a VNA. The obtained S2P file is integrated to the ICEM-CE model as shown in Figure II-47. For the 150 Ω measurement, the probe is placed as close as possible the power plane of ELECIS-F and also as close as possible to the measurement instrument; the spectrum analyzer. The measurement is performed with a spectrum analyzer because de external voltage level is too low because of the attenuation provided by the 150 Ω probe and it could not be measured using a digital oscilloscope.

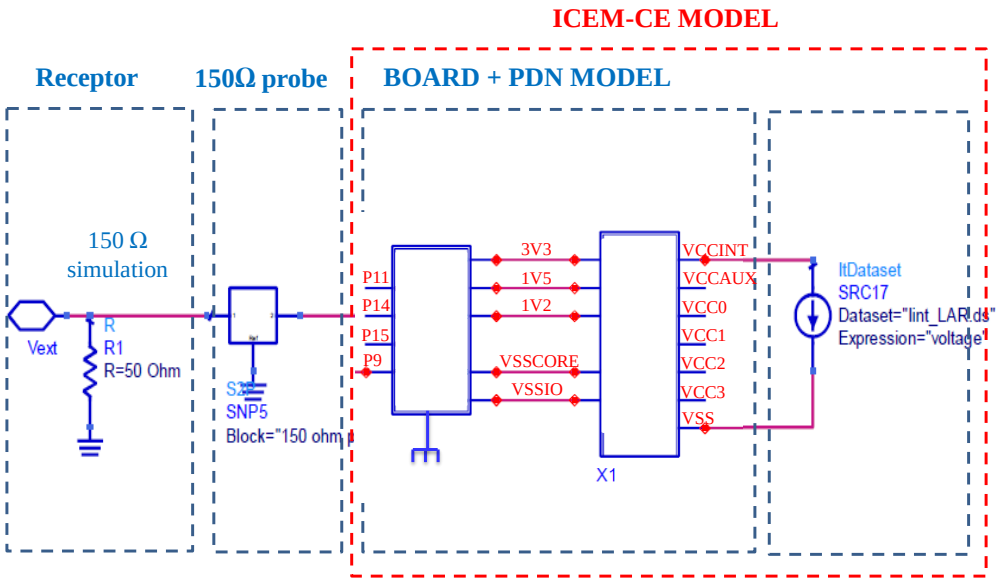

Figure II-47 Schematic for transient simulation on ICEM-CE model using a 150 Ω probe

Figure II-48 present a comparison of the spectral envelope in the frequency domain between the measurement and the simulation using the 150 Ω probe on the power plane 1.2 V. The simulation overestimates the measured level of noise and the computed RMS error is 15,68 dBµV calculated

up to 1 GHz, above this frequency, the measured CE is close the measurement system noise floor. Then, all the RMS errors for CE measurement using 150 Ω probe are calculated up to 1 GHz in this chapter. There are several possible explanations to these differences. Any error on the PDN model construction or the board model generation could affect the simulated voltage. Moreover, the IA Core construction is based on the external voltage measurement with the 1 Ω probe and the PDN and board models. Hence, there is no certainty on the constructed IA core. This is the main limitation of this method as discussed in 1.3.3.2. The improvement of the correlation between the measurement and the simulation is possible, but a long and random process will be necessary for the modification of the PDN model and the IA extraction. Furthermore, this process will not lead to a predictive methodology for ICEM-CE construction and is not adapted to industrial applications. Other studies were held for the construction of the IA independently to the PDN and the board model and will be presented later in this chapter.

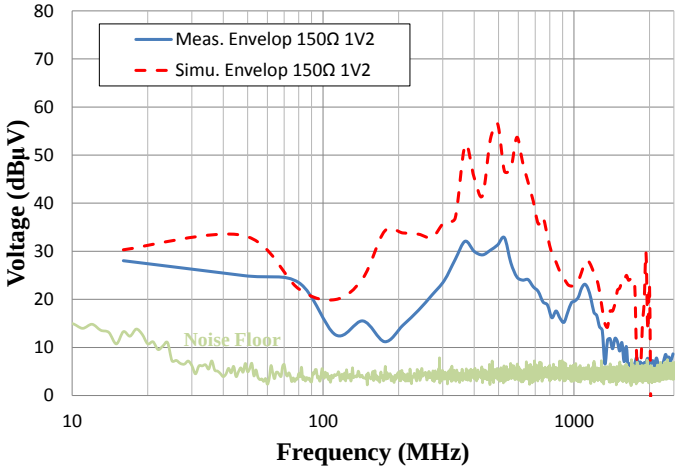

Figure II-48 Comparison between the measurement and the simulation of the spectral envelope of external voltage using the 150 Ω probe

As presented in this section, the extraction of the core internal activity was performed using the inverse method based on 1 Ω measurement. As seen in Figure II-42, $IA_{CORE}(t)$ presents residual oscillations due to the bad compensation of the transfer function and the external voltage measurements errors. This has an important contribution in the induced error of IA Core extraction. The switching activity of the CLBs produces a broadband impulse noise without the resonances phenomena linked to the PDN model. However, using the inverse method, HF resonance could be seen in the spectrum of the extracted IA Core.

Using the obtained result of $IA_{CORE}(t)$, the average current and power consumption was calculated and are respectively given by the values 31.8 mA and 38.16 mW. These results are compared to the estimation of Xilinx tool XPA (Xilinx Power Analyzer) that allows the estimation of power consumption of a design based on the floorplan analyze. Table II-4 shows the comparison between the estimated average current 27.33 mA and the average power 24 mW with the calculated values for the extracted current using the inverse method. The comparison shows that the applied approach for the IA Core extraction overestimates the average current and power consumption and could explain the difference between the measured and simulated

voltage using the 150 Ω probe shown in Figure II-48. Thus, it is necessary to use an alternative methodology for the IA extraction that could be based on the measurement or the estimation of the dynamic power consumption.

	IA inverse method	Xilinx estimator
Average current (mA)	31.8	27.33
Average power (mW)	38.16	24

Table II-4 Comparison of the average current and power between the IA extracted with the inverse method and the estimation of Xilinx tool

3.4.3 Construction of the IA of the IOs

3.4.3.1 Construction of IA IO using the inverse method

The internal activity of the switching IOs (IA IO) can also be modeled using the inverse method based on a measurement standard (e.g. 1 Ω measurement). Let consider the configuration described previously for the IA Core extraction. An output buffer will be activated and synchronized with the clock tree (16 MHz) on the bank 2 of the FPGA powered with 3.3 V. Since the configured logic blocs (CLBs) will not change, the IA Core is also considered unchanged and will be modeled as it was extracted previously following the inverse method. As seen in Figure II-49, ICEM-CE model will integrate two current sources that models IA Core and IA IO. To extract the IA IO using the inverse method, two transfer functions will be necessary to estimate using an AC simulation; H_{Core} the transfer function between the IA IO and the V_{EXT} and H_{IO} the transfer function between the IA IO and V_{EXT}. In this case V_{EXT} represents the measured voltage using the 1 Ω probe when one output buffer is activated. Then, the IA IO can be extracted considering the Equations II-12 and II-13.

$$V_{EXT}(f) = H_{Core}(f).IA_{Core}(f) + H_{IO}(f).IA_{IO}(f) \quad \text{(II-12)}$$

$$IA_{IO} = \frac{V_{EXT}}{H_{IO}} - \frac{H_{Core}.IA_{Core}}{H_{IO}} \quad \text{(II-13)}$$

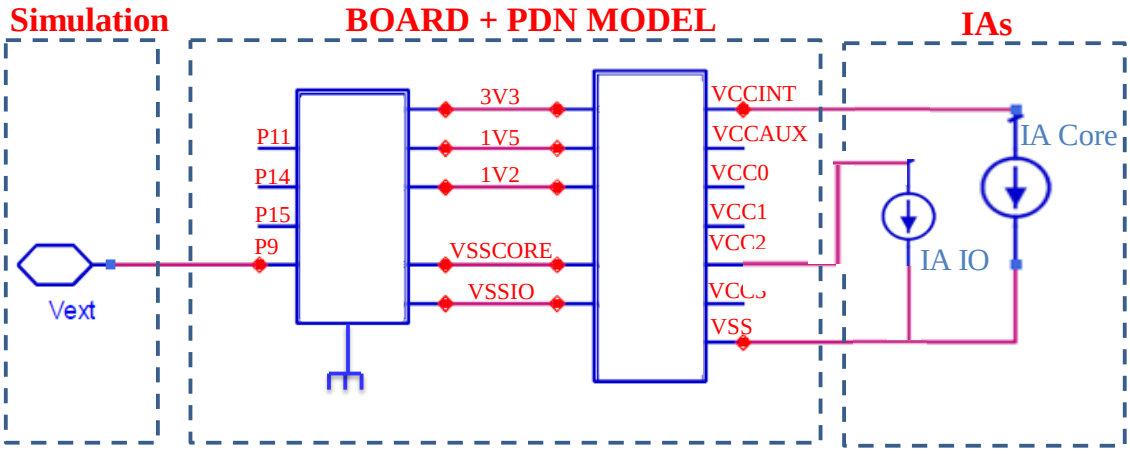

Figure II-49 Schematic of ICEM-CE integrating IA Core and IA IO

The IA IO has been extracted using Equation II-13 and is presented in Figure II-50 in the time and frequency domain. It is clear in this figure that the HF noise is dominant between 300 MHz and 1.5 GHz. The HF noise could also be seen in the time domain figure with an unreasonable peak-to-peak amplitude of 5.9 A.

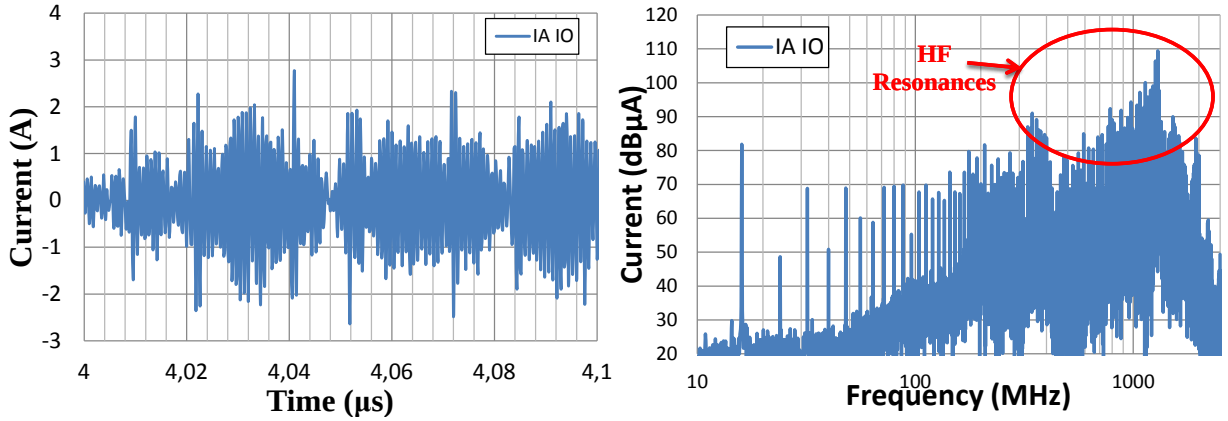

Figure II-50 Extracted IA IO in the time domain (left) and the frequency domain (right)

To understand how the extraction method influence the error induced in IA IO, let consider the modified values $\widetilde{H}_{Core}$, $\widetilde{H}_{IO}$, $\widetilde{IA}_{Core}$ and $\widetilde{V}_{EXT}$ of the transfer function, the IA Core and V_{EXT} by the absolute errors ΔH_{Core}, ΔH_{IO}, ΔIA_{Core} and ΔV_{EXT} as follow:

$$\widetilde{H}_{Core} = H_{Core} + \Delta H_{Core} \quad \text{(II-14)}$$

$$\widetilde{H}_{IO} = H_{IO} + \Delta H_{IO} \quad \text{(II-15)}$$

$$\widetilde{IA}_{Core} = I_{Core} + \Delta I_{Core} \quad \text{(II-16)}$$

$$\widetilde{V}_{EXT} = V_{EXT} + \Delta V_{EXT} \quad \text{(II-17)}$$

Equation II-13 could be written using these modified values, then, the absolute error of the IA IO can be calculated with the partial derivative principle as given by Equation II-18. Finally, based on the presented modified values and the equation II-13, the terms that contribute in the error of IA IO are shown in Equation II-19.

$$\Delta IA_{IO} = \left|\frac{\partial IA_{IO}}{\partial V_{EXT}}\right| \Delta V_{EXT} + \left|\frac{\partial IA_{IO}}{\partial H_{IO}}\right| \Delta H_{IO} + \left|\frac{\partial IA_{IO}}{\partial H_{Core}}\right| \Delta H_{Core} + \left|\frac{\partial IA_{IO}}{\partial IA_{Core}}\right| \Delta IA_{Core} \quad \text{(II-18)}$$

$$\Delta IA_{IO} = \frac{\Delta V_{EXT}}{\widetilde{H}_{IO}} + \frac{\Delta H_{IO}.\widetilde{V}_{EXT}}{\widetilde{H}_{IO}^2} + \frac{\Delta H_{IO}.\widetilde{H}_{Core}.\widetilde{IA}_{Core}}{\widetilde{H}_{IO}^2} + \frac{\Delta H_{Core}.\widetilde{IA}_{Core}}{\widetilde{H}_{IO}} + \frac{\Delta IA_{Core}.\widetilde{H}_{Core}}{\widetilde{H}_{IO}} \quad \text{(II-19)}$$

Equation II-19 shows the contribution of five terms in the error of the IA IO:

- The first and second terms are linked to the error on the external voltage measurement and the estimation of the transfer function H_{IO}. When H_{IO} is low, this term contribution will be important. Furthermore, the second term has a more important contribution since the inversed transfer function H_{IO} is squared.

- The three last terms are linked to the IA Core extraction error and the transfer functions H_{IO} and H_{Core} errors. When H_{IO} is low, the contribution of these terms is important. Especially for the third term where the inversed H_{IO} is squared.

Despite the important number of errors that contributes in the IA IO extraction, the generated waveform was used to simulate the CE in ICEM-CE model. As seen in Figure II-51, the comparison between the measurement and the simulation in the time domain still shows a good agreement in terms of peak-to-peak amplitude (11 mV measured and 14 mV simulated) and the activity of the clock tree and the IOs. Furthermore, in the frequency domain, the comparison between the measurement and the simulation shows a good correlation for the same reasons explained in the case of IA Core, although some resonances in HF could be seen due to the errors induced by the IA IO extraction. The calculated RMS error up to 1 GHz is 9.79 dB.

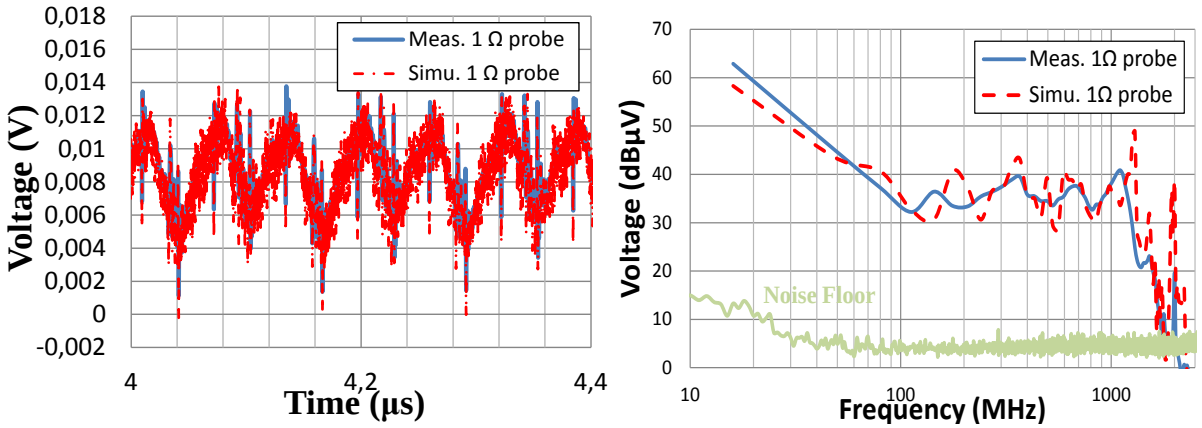

Figure II-51 Comparison between the simulated and measured CE using the 1 Ω probe in the time domain (left) and frequency domain (right)

Figure II-52 presents the comparison between the measurement and the simulation of CE in frequency domain when the 150 Ω probe was placed on the power planes 1.2 V and 3.3 V. These comparisons shows a very bad correlations between the CE measurement and simulation, especially in HF due to the bad compensation of the errors induced by the terms that contributes in the IA IO extraction. At low frequencies, the measured external voltage level using the 150 Ω probe is low because of the attenuation brought by the probe (the attenuation factor is 0.17). The calculated RMS errors up to 1 GHz is 14.68 dB on 1.2 V power plane and 9.26 dB on 3.3 V power plane.

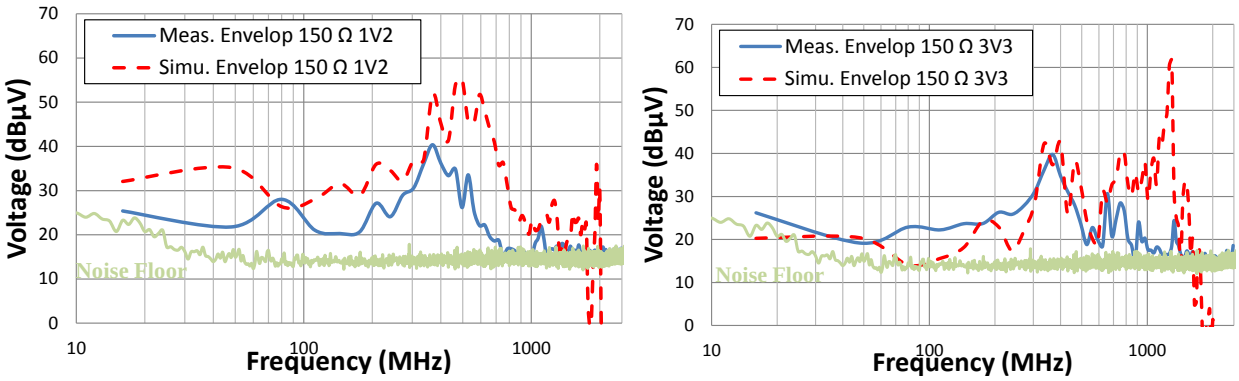

Figure II-52 Comparison between the measured and simulated CE using the 150 Ω probe on the power planes 1.2 V (left) and 3.3 V (right) in the frequency domain

This study has demonstrated that, as well as for the case of IA Core, the extraction of the IA IO using the inverse method based on standard measurement has several limitations due to the errors induced by the external voltage measurement and transfer functions estimation. This lead to an overestimated CE when the simulation is performed at another point (e.g. power planes), which is due to the bad compensation of errors. Especially on the estimation of the CE on the power plane 3.3 V which present a significant resonance around 1.3 GHz. This is due to the transfer function H_{IO} estimated between the internal domain VCC2 and the external voltage, and which contribution is inversed and squared in the IA IO error estimation. A new methodology of construction of IA IO will be proposed that allows the IA extraction independently from the PDN and the board model.

3.4.3.2 New method for IA IO construction

In the standard IEC 62433-2 [24], the construction of an IA bloc that reproduces the noise generated by the activity of the IOs is not discussed. The purpose of this work is to propose a new method for the construction of IA IO bloc, and case study will be presented for the methodology validation. Since the noise generated by the activity of IOs depends on the parameters that control the drivers as the type of standard (LVCMOS, SSTL, LVDS…), the configuration (slew rate, drive current…) and the load, the idea is to integrate an IBIS file in the constructed ICEM-CE. The IBIS file contains all the needed information on the IOs of the FPGA and could reproduce the transient profile of their output finely. The manufacturer Xilinx provides the users an IBIS file that was verified by static and SI measurements.

The main advantage of using an IBIS file is that it does not requires any measurement for the CE model construction, hence, the induced error by 1 Ω measurements are suppressed. Furthermore, IBIS is a well-established standard, widely employed by the manufacturer for the description of the switching profile and accessible to the IC end-users because it is not confidential. On the other hand, the model is independent of the design activity, but will be set as an input to the IBIS file.

Figure II-53 presents the configuration that will be used to for the integration of the IA IO block into the ICEM-CE model of the FPGA.

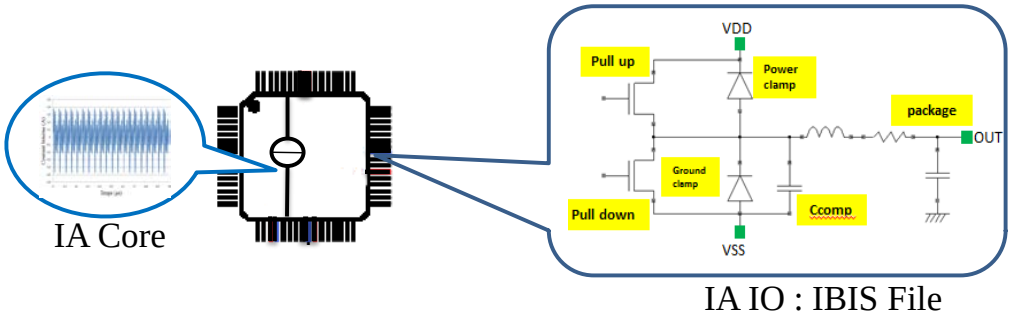

Figure II-53 Presentation of the IA Core and IA IO blocs of the ICEM-CE model

3.4.3.3 Validation of the new method of IA IO extraction

As described previously, the IBIS file is introduced in the ICEM-CE model of the FPGA as the IA IO. The selection of the type of IO is necessary while creating the IO buffer. Figure II-54 presents the schematic of the SPICE model used for the simulation of the external noise flowing through the 1 Ω probe. The IO buffer is connected to the internal terminal on the PDN model corresponding to the bank of IO to which it belongs. The same configuration presented for case of IA Core will be used, and for the validation of the IA IO, one LVCMOS IO is activated. Hence, only one IBIS file is added to the ICEM-CE SPICE model.

Figure II-55 shows a comparison between the measured and simulated external voltage using a 1 Ω probe when an IO is activated. In the time domain (left) the comparison shows a good agreement between the simulated peak to peak amplitude (10 mV) and the measured peak to peak amplitude (11 mV). In the frequency domain, there is a good correlation between the simulated and the measured spectral envelope up to 2.5 GHz with a computed RMS error of 7.28 dBµV calculated up to 2 GHz.

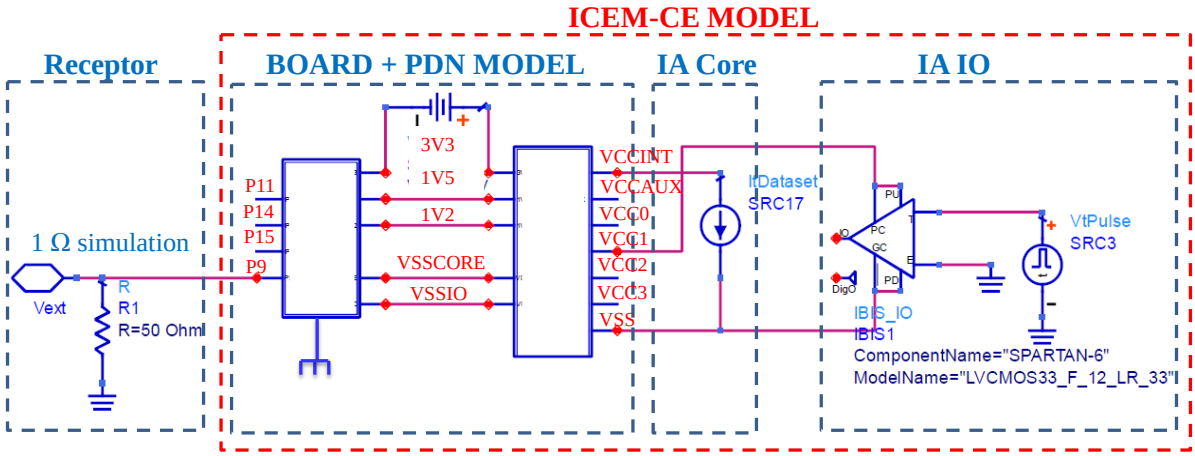

Figure II-54 Schematic of ICEM-CE model with the IA IO bloc

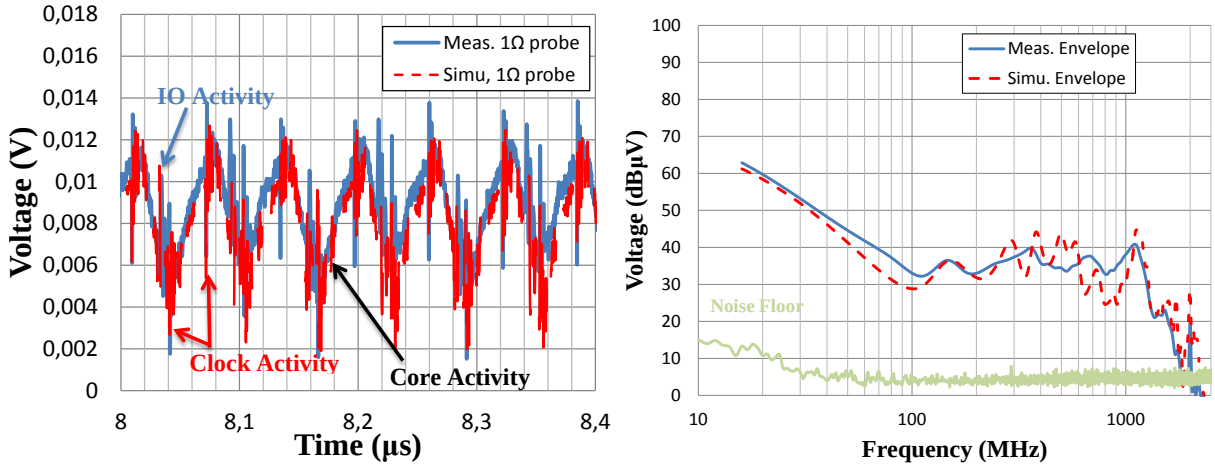

Figure II-55 Comparison in the time and frequency domain of the external voltage using a 1 Ω probe when an IO is activated

The proposed methodology could also be verified at other measurement points. A 150 Ω probe was placed as close as possible to the power planes 1.2 V and 3.3 V. Figure II-56 shows the comparison btween the measured and simulated CE. On the power plane 3.3 V, it is clear that the simulation presents a very low HF noise (between 800 MHz and 2.5 GHz), and in particular the resonance around 1.3 GHz shown in Figure II-52 which has been compensated using the new method. On the power plane 1.2 V, the simulated CE is still overestimated, this is due to the errors of the extraction of IA Core using the inverse method which are still existent. The calculated RMS up to 1 GHz on 1.2 V power plane is 14.29 dB and on 3.3 V power plane the RMS error is 8.22 dB.

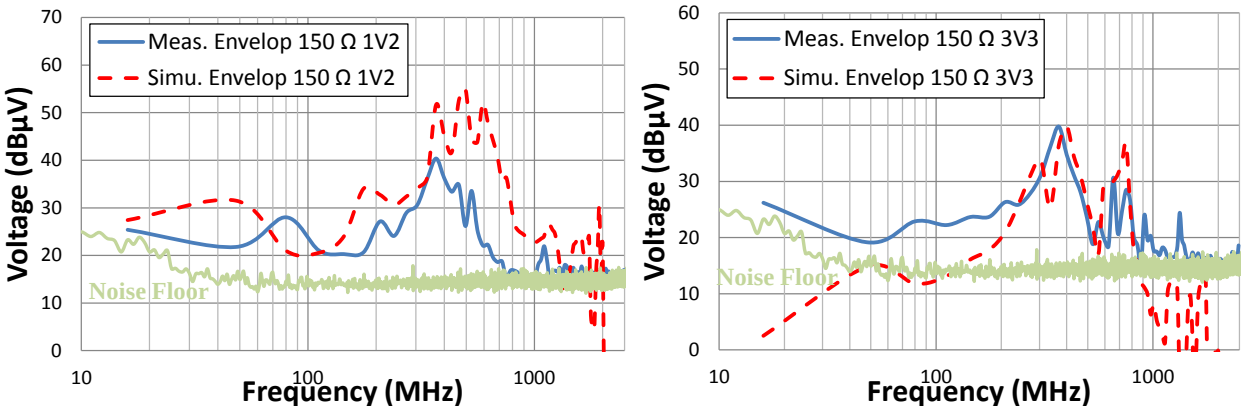

Figure II-56 Comparison between the measured and simulated CE using the 150 Ω probe on the power planes 1.2 V (left) and 3.3 V (right)

As seen in this section, the construction of the IA IO using the inverse method has led to the appearance of HF noise. This is mainly due to the inversed terms of the transfer function that contributes in the increase of the IA IO extraction error. A new method that allows segregating the IA IO construction from the PDN and the board model is based on the use of an IBIS file, because it is not confidential and reproduce the output buffers transient profile with a good accuracy. The new method presents a good estimation of CE using the 1 Ω probe. Using the 150 Ω probe to simulate the CE on the power plane 3.3 V, it is clear that the HF noise has been

compensated, although the underestimated level at low frequencies, which is close to the measurement system noise floor. However, the CE estimated with the 150 Ω probe still presents some desagreements on the 1.2 V power plane due to errors induced by the IA Core extracted with the inverse method. To have a more accurate position on the use of an IBIS file, a new method to extract the internal activity of the Core must be studied.

4. New methodology for the IA core construction

Within the ICEM standard, the construction of the IA block is uncorrelated from the design power consumption; this physical information is not included while it is completely related to the device switching activity. For some IC families such FPGAs, design tools provide to the end-users accurate estimation of the average dynamic power estimation from post-placement and routing simulations of a given configuration. Moreover, some advanced FPGA design tools are able to determine the instantaneous dynamic power consumption from a vector-based simulation, which allow the calculation of the time-domain profile of the dynamic current consumption and thus a precise extraction of IA core block [30]. However, this type of approach requires long simulation times, whose results are dependent on the input test vectors. To overcome this issue, we propose to estimate the IA block of a FPGA from vectorless power estimation and static timing analysis applied on post-placed and routed design. Compared to the vector-based approach, this solution is able to provide a good estimation of the IA block in a very short time, without additional steps in the FPGA design flow, and from a reduced set of data. Moreover, the proposed approach is able to take into account the random activity of the circuit. The proposed method can be applied to any FPGA end-user application or to any circuits developed with design tools providing necessary information.

The main advantage of this method is linked to the reduction of the effect of external voltage measurement error and the error of transfer function estimation. Considering the transfer function $\widetilde{H}_1$ and $\widetilde{H}_2$ as defined in 1.3.3.2 and the internal current $\tilde{I}_{INT}$. The absolute errors of the external voltages in two different measurement points are expressed as follow:

$$\Delta V_1 = \Delta H_1 . \tilde{I}_{INT} + \Delta I_{INT} . \widetilde{H}_1 \quad \text{(II-20)}$$

$$\Delta V_2 = \Delta H_2 . \tilde{I}_{INT} + \Delta I_{INT} . \widetilde{H}_2 \quad \text{(II-21)}$$

In the presented equations, only two terms contributes in the absolute errors ΔV_1 and ΔV_2:

- The first term is linked to the transfer function error ΔH_1 (ΔH_2), its contribution is proportional to the internal current $\tilde{I}_{INT}$. if the current amplitude decreases (especially in HF); then, the contribution of this term will also decrease.
- The second term is linked to the error of the internal current extraction ΔI_{INT}. Its contribution is proportional to the transfer function $\widetilde{H}_1$ ($\widetilde{H}_2$); if its value is low then the contribution of this is low.

Furthermore, the inversed terms of the transfer function $\frac{1}{H_1}$ and $\frac{1}{H_1^2}$ that amplifies the errors contribution, especially near the resonance frequencies and when H_1 and H_2 are low. Although,

the error in the external voltage are not suppressed, but still are reduced. And the induced errors by the extraction of the internal activity using the inverse method have disappeared.
Before presenting our IA core block construction methodology, a preliminary question is this: is it is necessary to determine precisely the time-domain waveform of the instantaneous current consumption to obtain an acceptable CE prediction? In the next paragraphs, we will demonstrate that the answer is no and that only two criteria must be respected to obtain a reliable prediction of CE.

4.1. Influence of the instantaneous current consumption waveform on emission spectrum

In digital synchronous circuits, current consumption appears mainly during transitions from logical state 0 to 1. Thus, the time domain profile of the instantaneous current is a periodic series of short pulses; its period is equal to the clock period Tc. As explained in [30], the power supply noise can be predicted if the charge consumed at each clock transition is determined correctly. The waveform of the current i(t) delivered by the IA block must reproduce this charge quantity, given by:

$$q = \int_0^{\tau} i(t)dt \qquad \text{(II-22)}$$

Where q is the transferred charge during a clock cycle and τ is the duration of the charge transfer or the current pulse. Moreover, to reproduce the CE spectrum, the duration τ of the charge transfer must be also known. In order to illustrate this principle, let consider the three basic periodic pulsed waveforms presented in Figure II-57, which model the dynamic current consumption of a digital circuit. The clock frequency is 10 MHz. The pulse durations are identical; their amplitudes are chosen such as the transferred charge is identical. These current waveforms are generated by a current source and form an IA block which is connected to the PDN block representative of a large digital IC.

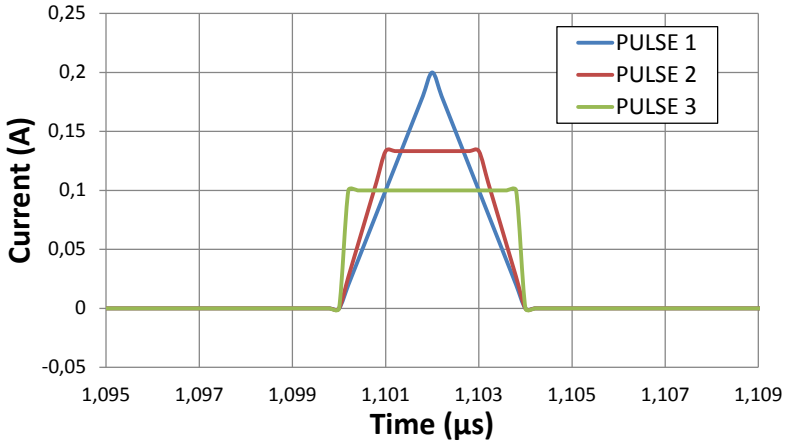

Figure II-57 The generated pulses for IA construction

The voltage across a 1 Ω resistor connected to the VSS pins of the circuit is simulated for each waveform. Figure II-57 presents a comparison of the simulated voltages using the different waveforms in time and frequency domain. Despite some differences in high frequency (around

the nulls of the spectral envelope), the envelopes of the spectra are very close, providing nearly identical estimation of the CE noise [26]. In the time domain, the peak-to-peak amplitudes between the simulated CE using the 1 Ω probe for the different pulse do not vary.

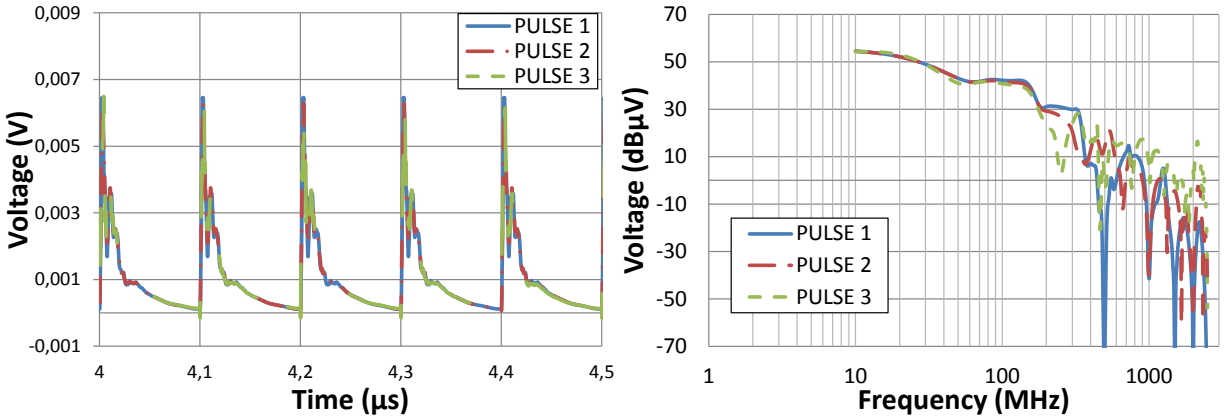

Figure II-58 The CE simulation for each pulse in the time domain (left) and the frequency domain (right)

The estimation of the difference between the CE simulations for the different pulses is given in Table II-5 as a RMS error calculated from 10 MHz to 2.5 GHz. This comparison shows that the RMS errors are nearly identical except between the triangular and the square pulses. This is explained by the HF resonances calculated for the different signals with the Fast Fourier Transform (FFT).

Difference between		RMS error (dBµV)
Pulse 1	Pulse 2	18.67
Pulse 1	Pulse 3	28.09
Pulse 2	Pulse 3	19.64

Table II-5 Calculated RMS errors between the different pulses

Whatever the waveform of the instantaneous current consumption, if the transferred charge and transfer duration are respected, an acceptable estimation of the CE can be obtained. This is the purpose of our methodology. Since there is no information on the internal current waveform, a triangular shape will be assumed for the IA Core construction.

4.2. Presentation of the IA construction methodology

The construction of IA Core is based on a current source constructed using a triangular pulse, since the comparison with other waveforms has not shown any important difference in the time domain CE simulation but only some difference in HF resonance which are due to the FFT of each signal. However, the amplitude and the pulse duration are still needed to construct the IA Core and are related the charge quantity transferred.

The charge quantity transferred at each clock cycle can be determined from measurements or the evaluation of the average dynamic power consumption P_{dyn_avg} by a design tool. It is given by Equation II-23:

$$P_{dyn\_avg} = F_C . \sum_{i=1}^{N} \alpha(i) . q_L . V_{DD} \quad \text{(II-23)}$$

Where N is the number of internal logical nodes or signals in the circuit, α(i) is the average number of transitions on signal i per clock cycle (toggle rate), $q_L(i)$ is the quantity of the charge associated to signal i, V_{DD} is the power supply voltage and F_C is the clock frequency of the circuit. For its Spartan 6 family, Xilinx provides inside its ISE software the Xilinx Power Analyzer (XPA) module [27] which gives a detailed estimation of the power consumption in the clock tree, the signals and logic blocks, and the IOs after a post-placement and routing simulation. XPA also gives a vectorless estimation of the toggle rates and average dynamic power of all the internal logic signals. From these estimated parameters, the average quantity of charge transferred during a clock cycle Q_L can be calculated. For each clock period T_C, the internal activity produces the same quantity of the charge as given by the formula II-24, where I_{avg} is the average dynamic current consumption.

$$Q_L = \sum_{i=1}^{N} \alpha(i) q_L(i) \quad \text{(II-24)}$$

ISE Xilinx tool performs a static timing analysis which gives a detailed report about the slack and the data path delays at the fast and slow PVT (Process/Voltage/Temperature) corners. For the construction of the IA, the pulse duration τ is considered to be the average value of the interval whose boundaries are the maximum data path τ_{max} and the minimum data path τ_{min} given by the static timing report, as presented in Equation II-25. The average dynamic current associated to a periodic pulsed waveform i(t) is calculated using Equation II-26.

$$\tau = \frac{\tau_{max} + \tau_{min}}{2} \quad \text{(II-25)}$$

$$I_{avg} = \frac{1}{T_C} . \int_0^{\tau} i(t)\, dt \quad \text{(II-26)}$$

In the next paragraphs, we consider that the dynamic current consumption waveform is a symmetrical triangular pulse. The peak amplitude of the pulse I_{max} is given by Equation II-27.

$$I_{max} = 2 . I_{avg} . \frac{T_C}{\tau} \quad \text{(II-27)}$$

From the resolution of the Equations II-24, II-26, and II-27 the maximum amplitude of the IA is calculated using the formula II-28. Figure II-59 summarizes the steps to get the required data from a FPGA design tool to solve the Equation II-28, which leads to the IA construction.

$$I_{max} = \frac{2 . P_{dyn\_avg}}{F_C . \tau . V_{DD}} \quad \text{(II-28)}$$

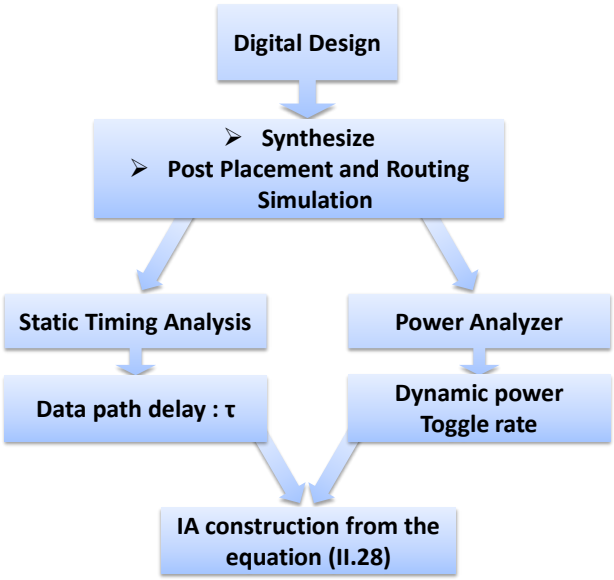

Figure II-59 Workflow of construction of the IA Core with a deterministic approach

The proposed workflow of construction of the IA is based on the average dynamic power consumption, hence, the approach proposed is deterministic; the amplitude of the IA is constant at each clock cycle. In practical cases, the IA profile is random due to the variation of the toggle rate and the power consumption of the active logic blocks. Thus, the peak-to-peak amplitude of the IA in the time domain could be under estimated and the envelope of the emission spectrum inaccurate. In the next part, an alternative approach is proposed for the construction of a random IA.

4.3. Statistical method for construction of a random IA

The construction of a random IA block is possible with a vector based simulation [30] but this may require long simulation time. However, the power analysis tool XPA gives the switching probability of each logic block of the circuit. The variability of the switching activity around its mean value can be estimated in a short simulation time. For the construction of a random IA, a methodology based on the statistical distribution of the transferred charge per clock cycle is proposed.

XPA tool gives a detailed report about the dynamic power consumption and the toggle rate for the routed signals and the logic blocks. Although the accuracy of calculation if guaranteed up to some fW, the XPA reports are limited to display result up to some mW. Hence, the power consumption of several signals and logic blocs are not displayed. However, Xilinx still propose the tool Xilinx Power Estimator (XPE) [28] as a Microsoft Excel spreadsheet and allows the importation of design information to estimation the power consumption of the difference activated blocs with a good accuracy (several fW). With these data, it is possible to calculate the Probability Density Function (PDF) of switching of each logic block of the circuit and thus the PDF of the transferred charge to each logic block per clock cycle. Although the logic states of each logic block are partially dependent, we neglect these interdependencies since they cannot be

determined through the vectorless estimation of XPE. Considering that each logic block of the circuit switches independently from the others, the PDF of the transferred charge to the circuit is the convolution product of the PDF of the transferred charge of each logic block. Statistical parameters such as the average and standard deviation can be calculated, and the most representative statistical law can be determined. In practice, due to the large number of switching logic nodes, the distribution tends to be Gaussian. Under this assumption, the probability that a logic block i transfers a charge quantity $q_L(i)$ per clock cycle is given by $p_j(i)$. Hence, the average transferred charge quantity $\overline{q_L}(i)$ for each logic block is calculated using the Equation II-29. Considering the charge quantity q(i) as a random variable, the expected variance σ_i^2 is given by the formula II-30, allowing the calculation of the PDF of each logic block j, where S is the number of logic states. For a binary case S=2 charges are only transferred to logic nodes during transition '0'-'1'.

$$\overline{q}_L(j) = \sum_{i=1}^{S} p_j(i).\, q_j(i) = \alpha(j).\, q_j \tag{II-29}$$

$$\sigma_j^2 = \sum_{i=1}^{S} p_j(i).\,(q(i) - \overline{q}_L(j))^2 = \alpha_j(1-\alpha_j).\, q_j^2 \tag{II-30}$$

The PDF of the transferred charge to the circuit follows the normal distribution $N(Q_L, \sigma^2)$, where Q_L is the average transferred charge quantity II-31 and σ^2 its variance II-32, N is the number of activated logic blocs. In the Equation II-32 the term of inter-dependence between the different logic blocs are neglected.

$$Q_L = \sum_{i=1}^{N} \overline{q}_L(i) \tag{II-31}$$

$$\sigma^2 = \sum_{i=1}^{N} \sigma_i^2 \tag{II-32}$$

Finally, in order to generate a SPICE compatible IA source, a series of random charge quantity Q(k) is generated at each clock cycle according to the previous PDF. Considering a symmetric triangular pulse, the amplitude $I_{max}(k)$ of the IA is given by the expression II-33, where k is the number of generated points. The IA is then modelled using a current source based on a Piece Wise Linear (PWL) function file. Figure II-60 summarizes the approach of construction of the IA using the statistical distribution.

$$I_{max}(k) = \frac{2.Q(k)}{\tau} \tag{II-33}$$

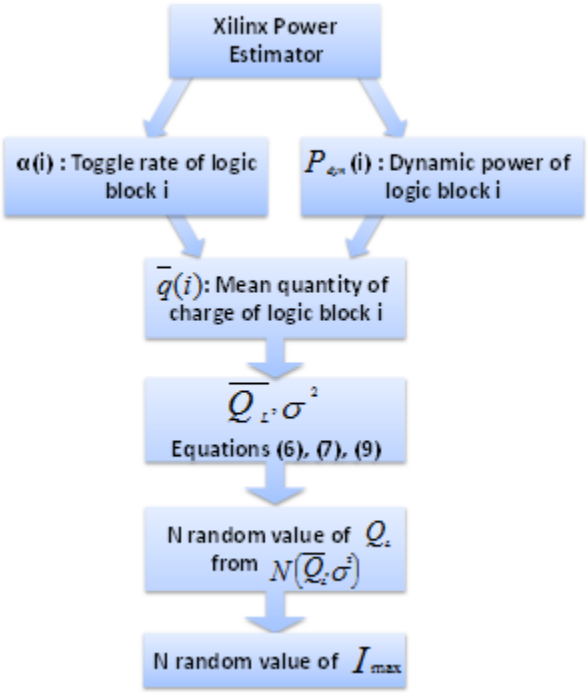

Figure II-60 Workflow of construction of the IA Core with the statistical approach

4.4. Validation of the IA core model

4.4.1 Presentation of the case studies

The construction of a predictive internal activity of the FPGA is performed for a given activity. The workflows presented previously are verified for different case studies of basic synchronous digital designs. The clock frequency is set to 16 MHz for the different case studies. The first case study is the delay lines presented previously. Due to its regular structure, its dynamic power consumption is deterministic; i.e. the number of switching gates remains identical at each clock transition.

For the second validation case, the 7-bits counter is a good example of synchronous circuit for which the internal signals present different toggle rates that could be known depending on the bits number. In this case, 800 7-bits counters have been cascaded in parallel.

As another validation case, a configuration with a random number of simultaneous switching gates is tested, with a Pseudo Random Number Generator (PRNG) blocks. The structure of the 5-bits PRNG is presented in Figure II-61. 200 identical PRNG have been cascaded in parallel to maximize the dynamic power consumption. For the different cases, no output buffer is switching. Hence, the 1 Ω measurements and simulations shows only the contribution of the internal logic blocs and the clock tree activity of the FPGA. Table II-6 summarizes the dynamic power consumption, data path delay and the average toggle rate collected from the estimation tools of Xilinx. The dynamic power has also been measured for each configuration and presents a low difference (around 2 to 4 mW) with Xilinx estimation tool.

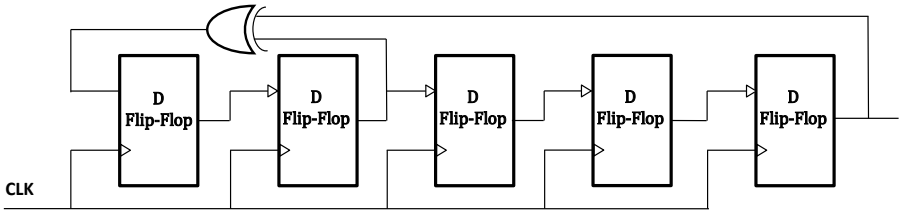

Figure II-61 Structure of the 5-bits PRNG configuration

Configuration	Measured Dynamic power (mW)	Estimated Dynamic Power (mW)		Data path delay (ns)		Average toggle rate (%)
		Logic	Clock	Logic	Clock	
Delay Line	26,8	24	1,5	40	0,75	100
5-bits PRNG	4,8	3,11	1,5	1,5	0,75	38,75
7-bits counter	7,2	9,60	1,5	3,8	0,75	28,35

Table II-6 Dynamic power consumption and the data path delay given by Xilinx reports for the case studies

4.4.2 Validation of the IA Core for the delay line

The first case study (delay line) has a toggle rate of 100 % because all the signals are switching at the rising edge of the clock. The clock tree presents non-negligible dynamic power consumption, its toggle rate is about 200 %, and hence, the signals representing the clock tree consumes energy at both rising and falling transitions of clock signal. Therefore, the internal activity of the clock tree is separated from the internal activity of the signals and the logic blocks. As shown in Figure II-62, two current sources are used to represent the activity of the clock, and one current source represents the activity of the signals and logic blocks. The IA waveform is supposed as a symmetric triangular pulse. The parameters are calculated from the resolution of the equations given in the sections 4.2 and 0.

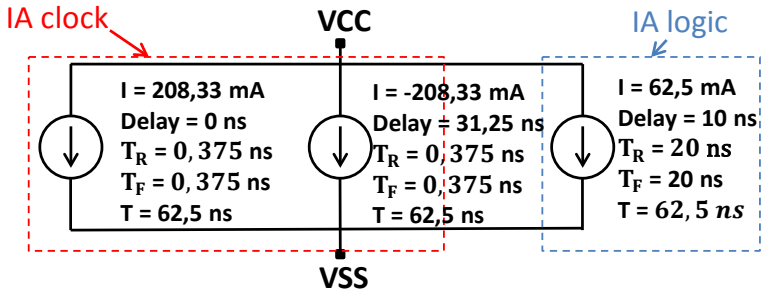

Figure II-62 Construction of IA Core bloc using current sources for the delay lines case study

4.4.2.1 Validation of the IA Core using the 1 Ω probe method

The constructed internal activity block is combined to the PDN and the board equivalent model. A transient simulation using ADS is performed to simulate the CE produced by the FPGA and measured through a 1 Ω probe. The time-domain simulation and measurement results are compared in Figure II-63 (left). The simulated peak-to-peak amplitude of the voltage fluctuation is equal to 9 mV and presents a good correlation with the measured amplitude equal to 11 mV.

Figure II-63 (right) shows a comparison between the measured and simulated external voltages with a 1 Ω probe in the frequency domain. The comparison presents a good correlation between the measured and the simulated spectrum with a RMS error of 5.15 dBµV. Simulation predicts that the frequency content of CE falls down above 1.2 GHz. This is confirmed by measurements.

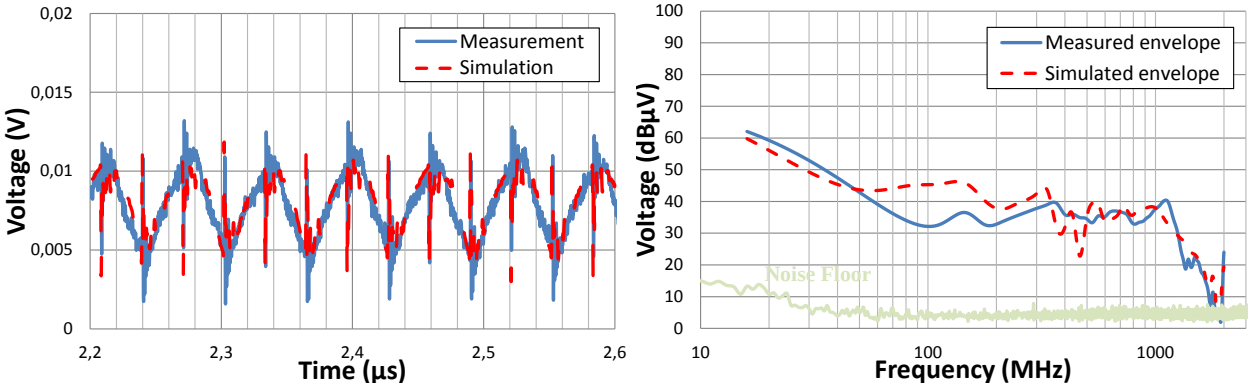

Figure II-63 Comparison between the measured and simulated CE with the 1 Ω probe in the time domain (left) and the frequency domain (right) for the delay line

Although some differences between the measured and simulated CE using the 1 Ω probe method, the peak-to-peak amplitude is well-estimated and general tendency of the spectral envelope in the frequency domain with an acceptable level. The observed differences could be linked to the assumption made on the IA Core waveform (triangular pulse), the errors of dynamic power consumption and toggle rate estimation, measurement errors, or even to the construction of the PDN and/or the board model.

4.4.2.2 Validation of the IA Core using the 150 Ω probe

The constructed IA Core is also verified using 150 Ω measurements and simulation on the power plane 1.2 V. Figure II-64 presents the results of the comparison between the measured and simulated spectral envelope CE in the frequency domain. The comparison shows a good agreement up to 1 GHz with a RMS error 4.95 dBµV. In 3.4.2.2, the RMS error was 16.58 dBµV. An important improvement on CE estimation using the 150 Ω probe can be noted using the new method. This improvement is due to the suppression of the inversed terms that contributed in the IA construction using the inverse method as explained in the introduction of this section.

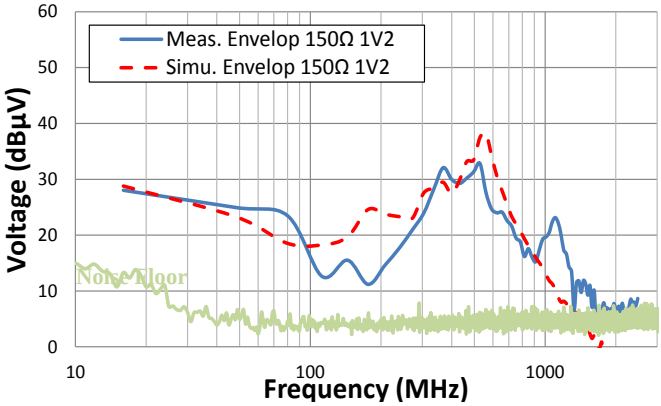

Figure II-64 Comparison between the measured and simulation CE with a 150 Ω probe on 1.2 V in the frequency domain for the delay line configuration

4.4.2.3 Validation of the IA Core and IA IO for the delay lines configuration

In 3.4.3.3, the advantage of the new method of IA IO construction using an IBIS file was explained. However, the simulation results using the 150 Ω probe did not present a good estimation of the measured CE; we assumed that it was due to the IA Core errors constructed using the inverse method. Let consider again the delay lines configuration when an output buffer is activated. For the CE simulation the IA Core has been constructed using the presented deterministic approach based on the dynamic power consumption, and IA IO has been constructed using an IBIS file. Figure II-65 presents the comparison between the measured and simulated CE on the power planes 1.2 V and 3.3 V. This figure shows a better agreement between the measurement and the simulation on the power 1.2 V with a calculated RMS error up to 1 GHz 5.21 dBµV, the errors induced previously by IA Core has been compensated thanks to the new method. However, the simulation on the power plane 3.3 V still underestimates the CE at low frequencies, although it correlates with the measurement between 200 MHz and 1 GHz. The new methods allow segregating the IA blocks extraction from the board and the PDN models.
The observed difference could be related to IA blocks construction or the PDN and the board model extraction.

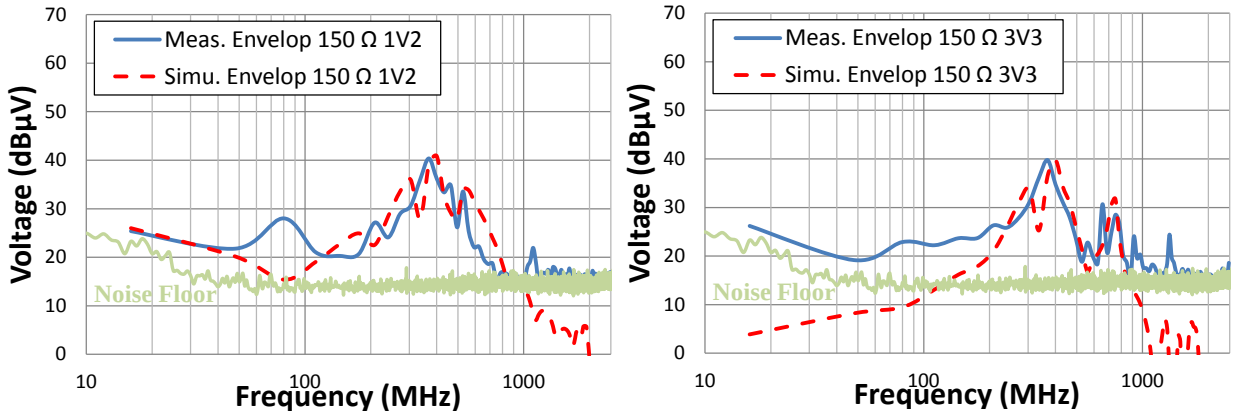

Figure II-65 Comparison between measured and simulated CE using the 150 Ω probe on 1.2 V power plane (left) and 3.3 V power plane (right) for the delay line configuration

4.4.3 Validation of the IA Core for the 7-bits counter configuration

The case of the 7-bit counter is particularly different from the previous case. The signals representing every bit of the counter have different toggle rates. Firstly, the IA is constructed following the deterministic approach as shown in Figure II-66. Figure II-67 (left) presents a comparison between the measured and simulated external voltage using a 1 Ω probe in the time domain. The simulated peak-to-peak amplitude of the voltage fluctuation reaches 13 mV and is underestimated compared to the maximum measured peak-to-peak amplitude of 21 mV because we consider that the instantaneous transferred charge at each clock cycle is constant and equal to the average transferred charge per clock cycle. However, if the activity is random, the instantaneous transferred charge varies around the average value. Figure II-67 (right) presents the Fast Fourier Transform (FFT) of the previous comparison. The sub-harmonics of the clock

frequency are not represented, but globally, the simulated CE shows a good correlation with the measurement, the RMS error is 5.19 dBµV.

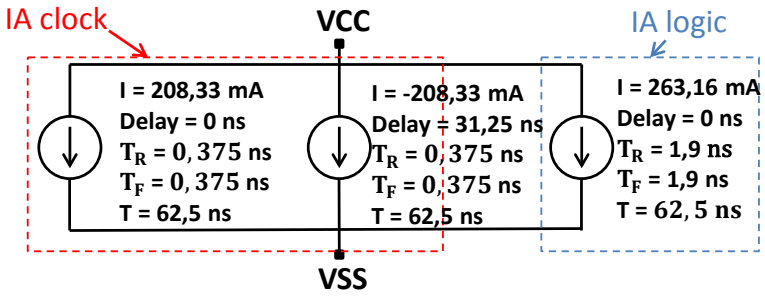

Figure II-66 IA Core construction for the 7-bits counter configuration

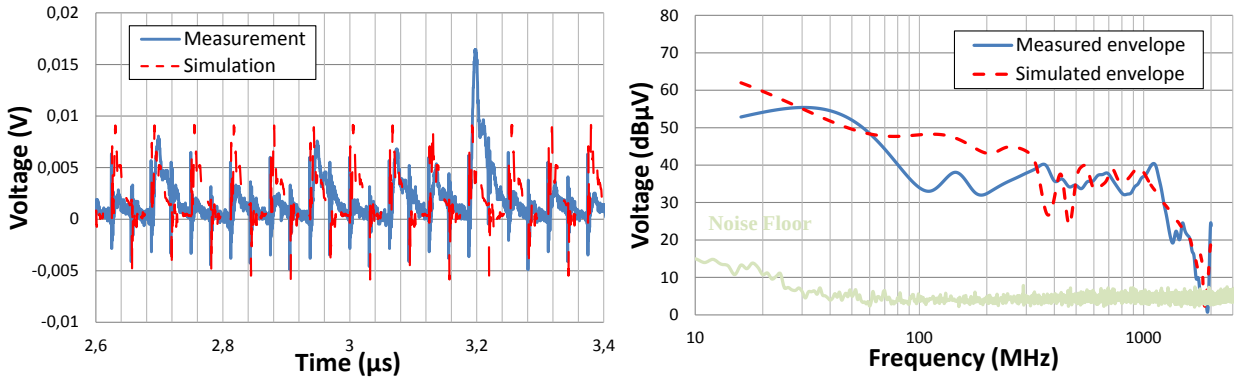

Figure II-67 Comparison between the measured and simulated CE with the 1 Ω probe in the time domain (left) and the frequency domain (right) for the 7-bits counter configuration using the deterministic approach

To overcome the presented issues, a random IA is constructed from the approach based on the statistical distribution for the case of the 7-bits counter. Figure II-68 shows the simulated and the measured external voltages using a 1 Ω probe. The simulated maximum peak-to-peak amplitude of the voltage fluctuation of 22 mV allows the prediction of the maximum peak-to-peak amplitude of 21 mV with a good precision. The simulated time domain profile reproduces the random character of the CE with a good approximation when the statistical method is used to construct the IA. Figure II-68 presents the comparison of the measured and simulated external voltages using a 1 Ω probe in the frequency domain. Not all the harmonics produced by the configuration are represented in the simulation, but an energy gain is visible below the clock frequency. The envelope of the simulated CE shows a good correlation with the measured envelop. The RMS error in this case is about 4.86 dBµV.

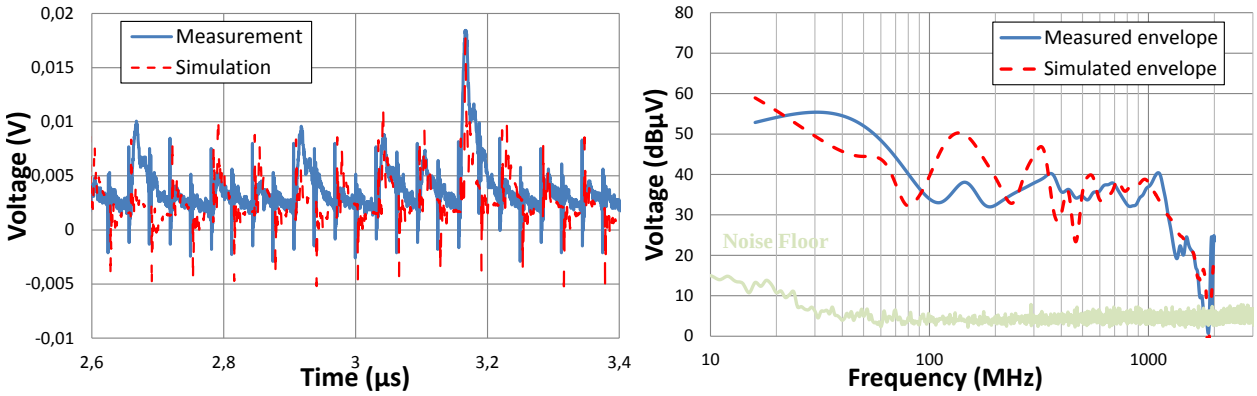

Figure II-68 Comparison between the measured and simulated CE with the 1 Ω probe in the time domain (left) and the frequency domain (right) for the 7-bits counter configuration using the statistical approach

The validation of this case study has also been performed at another test point. The 150 Ω probe is connected to the power plane 1.2 V. Figure II-69 presents the comparison between the measured and simulated CE for the 7-bits counter configuration. The general tendency of the measured CE is well reproduced by the simulation, although some overestimation at low frequencies which could be related to the same reasons explained previously. The calculated RMS error up to 1 GHz is 6.99 dBµV.

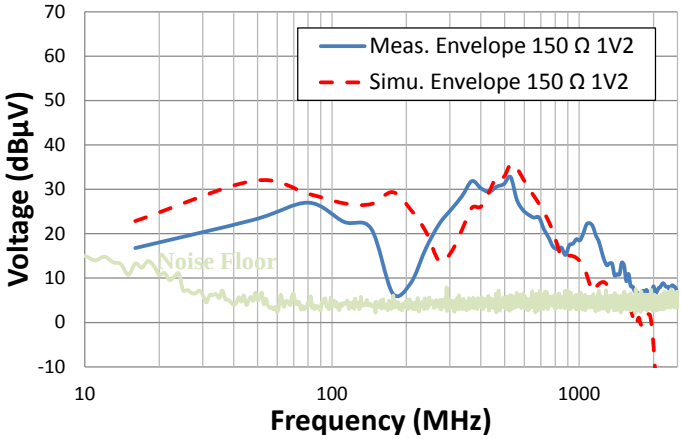

Figure II-69 Comparison between measured and simulated CE using the 150 Ω probe on 1.2 V power plane for the 7-bits counter configuration

4.4.4 Validation of the IA for the PRNG configuration

The case of the PRNG presents pseudo-randomly switching bits at every clock cycle. Thus, the dynamic power consumption will vary following the variation of the toggle rate of the active logic blocks. As a first approach, an IA is constructed following the deterministic approach for the CE simulation as seen in Figure II-70. Figure II-71 (left) shows the comparison in the time domain between the simulation and the measurement of the external voltage fluctuation using a 1 Ω probe. The simulated peak-to-peak amplitude 5.2 mV underestimates the measured maximum peak-to-peak amplitude 7 mV. Although the simulation gives an approximate estimation of the mean amplitude, it does not represent the variable character of the CE.

Figure II-71 (right) presents the Fast Fourier Transform (FFT) of the previous comparison. The first harmonics are under-estimated, but globally, the simulated CE shows a good correlation with the measurement, the RMS error is 5.89 dBµV.

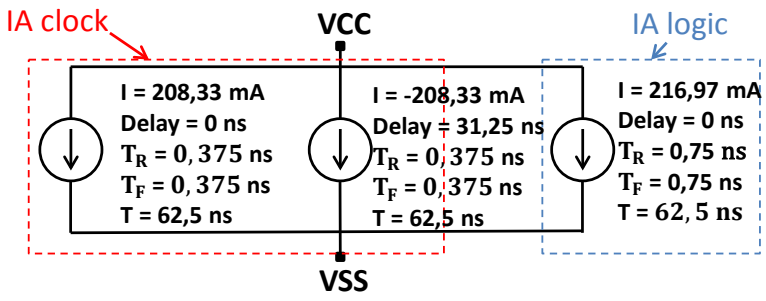

Figure II-70 IA Core construction for the PRNG test configuration

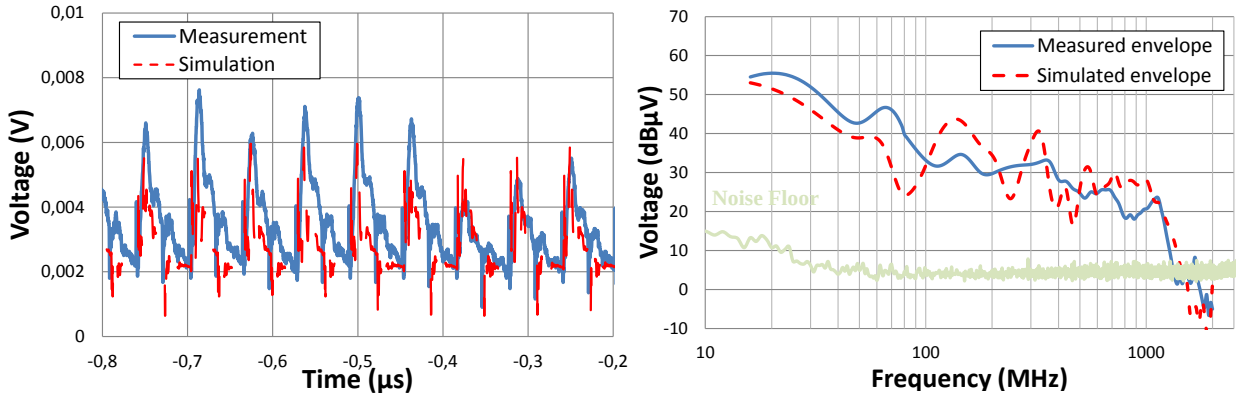

Figure II-71 Comparison between the measured and simulated CE with a 1 Ω probe in the time domain (left) and the frequency domain (right) for the PRNG using the deterministic approach

The use of the deterministic approach for IA Core construction does not influence the spectrum of CE. Furthermore, the estimated CE does not underestimate the voltage peak-to-peak amplitude when the fluctuations change between the different clock cycles.

To improve the relevance of the simulated CE results in the time domain, a random IA is constructed using the statistical method. Figure II-72 (left) shows the simulated and the measured external voltages using a 1 Ω probe. The simulated maximum peak-to-peak amplitude of the voltage fluctuation 7,1 mV is very close to the maximum peak-to-peak amplitude obtained in measurement. The simulated time domain profile reproduces the random behavior of the CE with a good approximation.

Figure II-72 (right) presents the comparison of the measured and simulated external voltages using a 1 Ω probe in the frequency domain. The envelope of the simulated CE shows a good correlation with the measured envelop. The RMS error in this case is about 5.26 dBµV, which is a little better than the error obtained with the deterministic approach.

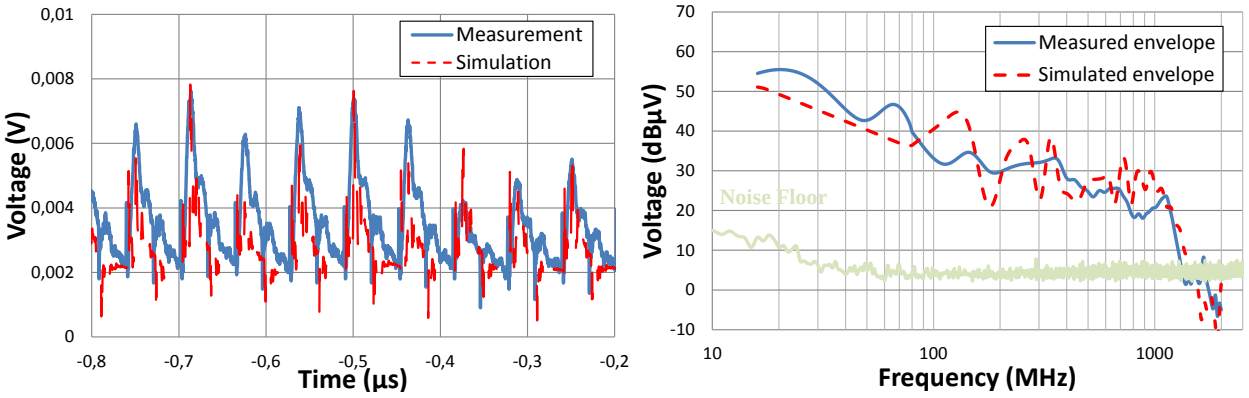

Figure II-72 Comparison between the measured and simulated CE with a 1 Ω probe in the time domain (left) and the frequency domain (right) for the PRNG using the statistical approach

This case study was also validated using the 150 Ω method on the VCCINT power plane 1.2 V. Figure II-73 presents the comparison between measured and simulated CE for the PRNG configuration using the 150 Ω probe and it shows a good estimation of the general tendency of CE level with a RMS error of 8.1 dBµV. However, some differences still could be noted at low frequencies, where the CE level is underestimated. To understand the origins of these disagreements a very long and random process of errors identification on the PDN and board models will be needed, and new afterthoughts on the assumptions for IA Core extraction may be necessary, which do not allow the construction of a predictive ICEM-CE model and is not suited to industrial applications that aims to reduce time and cost. Hence, although some noted differences, the proposed methodologies still allow the estimation of CE with an acceptable accuracy.

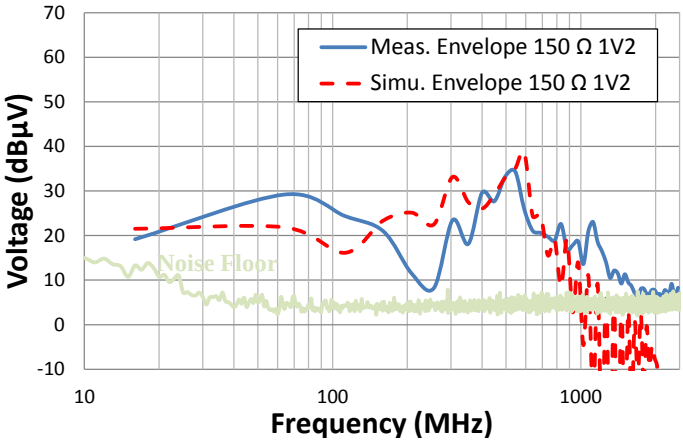

Figure II-73 Comparison between measured and simulated CE using the 150 Ω probe on 1.2 V power plane for the 5-bits PRNG configuration

4.5. Comparison between the inverse method and the new methodology for IA construction

The construction of IA Core with the new methodology based on simulation tools of dynamic power consumption and static timing analysis was validated for different case studies and using 1/150 Ω probes. The comparison between the measurement and the simulation of the CE using the inverse method based on the 1 Ω measurement had shown very good correlation for both

methods. However, the use of the 150 Ω for CE validation gave better results when the new methodology was applied as shown in Figure II-75. The new method of IA Core construction has proved that when the simulation is performed at a different location the result still correlates with the measurement. Figure II-74 compares the IA Core of the delay line configuration constructed with the inverse method based on the 1 Ω measurement as shown in part 3.4.2 and the IA Core constructed following the deterministic approach in part 4.4.2. The comparison shows that the peak to peak amplitude of the IA Core generated with the deterministic approach is 340 mA and with the inverse method is 450 mA. Furthermore, the calculated dynamic power for the IA constructed with inverse method is 38.16 mW and for the IA constructed using the new approach is based on the estimated dynamic power consumption using XPA 24 mW. However, a measurement of the dynamic power was performed and shows a power consumption of 26.8 mW, which is close to the estimated value using XPA. The proposed method for IA Core extraction is a one-shot approach; it does not require any optimization process to improve the accuracy of CE result. Moreover, it is a rapid method that does require neither the measurement methods (1/150 Ω methods) nor the de-embedding processes.

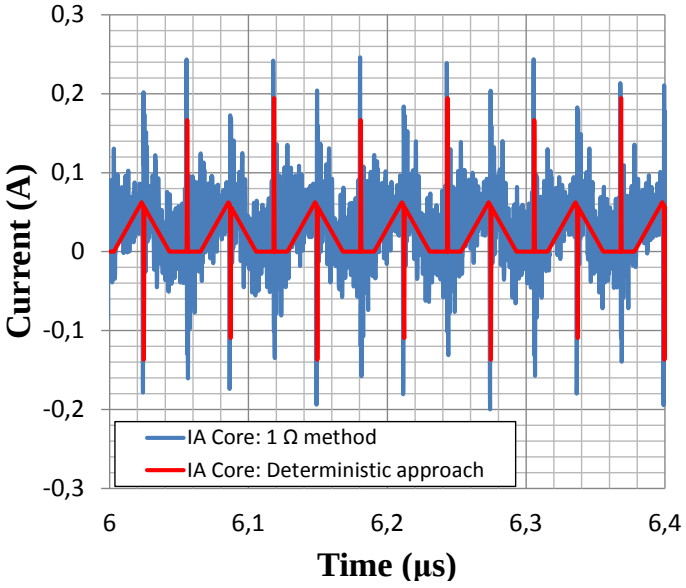

Figure II-74 Comparison between the IA core generated with the inverse method and with the deterministic approach for the delay line configuration

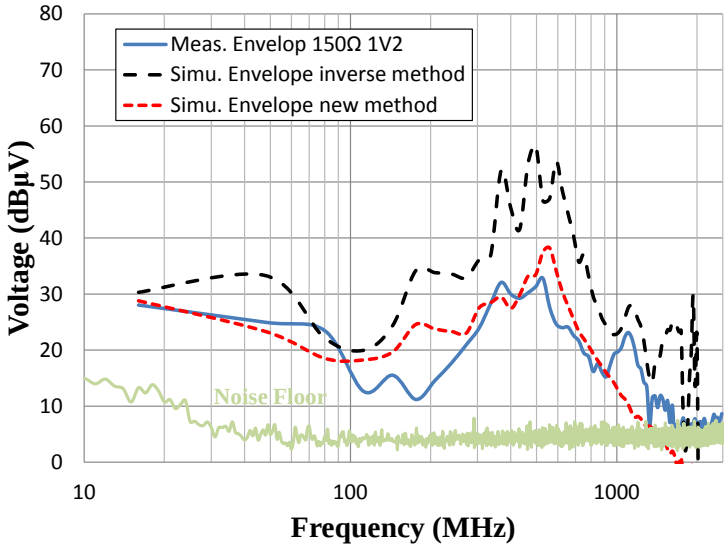

Figure II-75 Comparison between the measured and simulated CE with an extracted IA Core following the inverse method and the new approach for the delay line configuration

5. Presentation of ICEM Generator tool

5.1. ICEM GENERATOR tool

The proposed methodology for IA Core construction is based on the dynamic power and static timing analysis reports. The analysis of these reports could take a long time; hence, a dedicated tool was constructed with A. Boyer to automate the generation of the IA of the FPGA. The tool is named "ICEM GENERATOR". It integrates the algorithm described previously for the generation of a constant and a variable IA. The workflow of CE simulation using ICEM GENERATOR tool is described in Figure II-76. It consists on generating the power analysis report (.pwr) and the static timing analysis report (.twr) using Xilinx tool after synthesize and post placement and routing simulation of a given configuration. The ICEM GENERATOR tool reads both files and is based on XPE (Xilinx power Estimator) to analyze the reports. Finally, the constructed IA can be generator in different file format (IC-EMC, LTSPICE, ADS, PWL…) for CE simulation using SPICE tools.

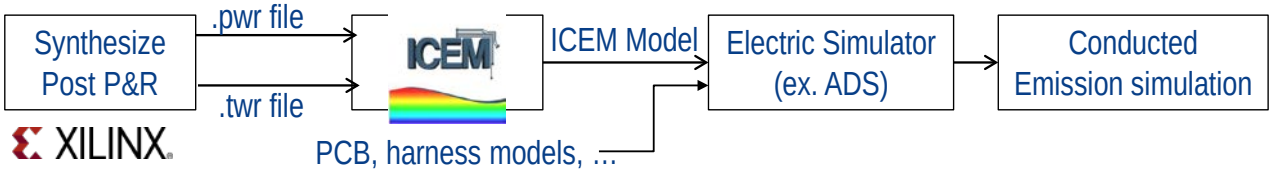

Figure II-76 Workflow of CE simulation using ICEM GENRATOR

Figure II-77 presents a view on ICEM GENERATOR tool. To summarize its utilization, the user can follow these steps:

- **First step**: power domains definition with pins attribution
- **Second step**: automatic current sources extraction from manufacturer reports
- **Third step**: equivalent SPICE model generation

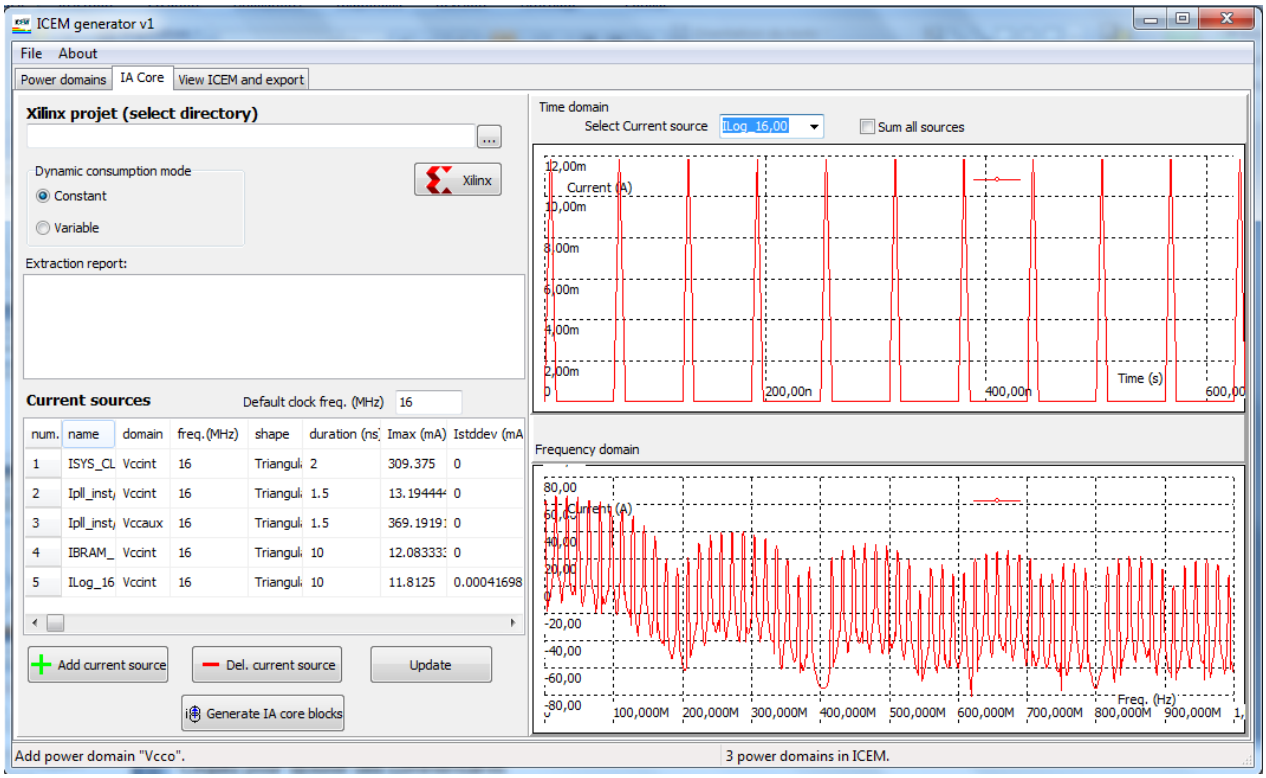

Figure II-77 ICEM GENERATOR tool window

5.2. Validation of ICEM GENERATOR tool

To validate the ICEM GENERATOR tool, a configuration representing an industrial design was implemented. It consists on generating sinusoid signal using the FPGA then computing the FFT after a filtering system as shown in Figure II-79. The clocking infrastructure: consists of a Digital Clock Manager (DCM), configured to 1:1 scaling of 16 MHz clock input. Its output clock is used to clock each block of the DSP chain. NAND gate, whose inputs are connected to DCM's LOCKED output and one of the board's GPIO with pullup, which asserts active-high system reset whenever any of these two inputs go LOW. Figure II-78 summarizes the on-chip power consumption and the resources utilization for the industrial application estimated by XPA tool. The total dynamic power estimated is 23 mW; it is very close to the measured power consumption (24 mW).

On-Chip Power Summary				
On-Chip	Power (mW)	Used	Available	Utilization (%)
Clocks	5.90	1	---	---
Logic	4.34	1799	9112	20
Signals	4.75	4821	---	---
IOs	4.50	19	186	10
BlockRAM/FIFO	1.20	---	---	---
8K BlockRAM	0.67	2	64	3
16K BlockRAM	0.53	2	32	6
DCMs	11.26	1	4	25
DSPs	1.74	30	32	94
Static Power	21.90			
Total	55.60			

Figure II-78 On-chip power consumption and resources utilization estimated by XPA

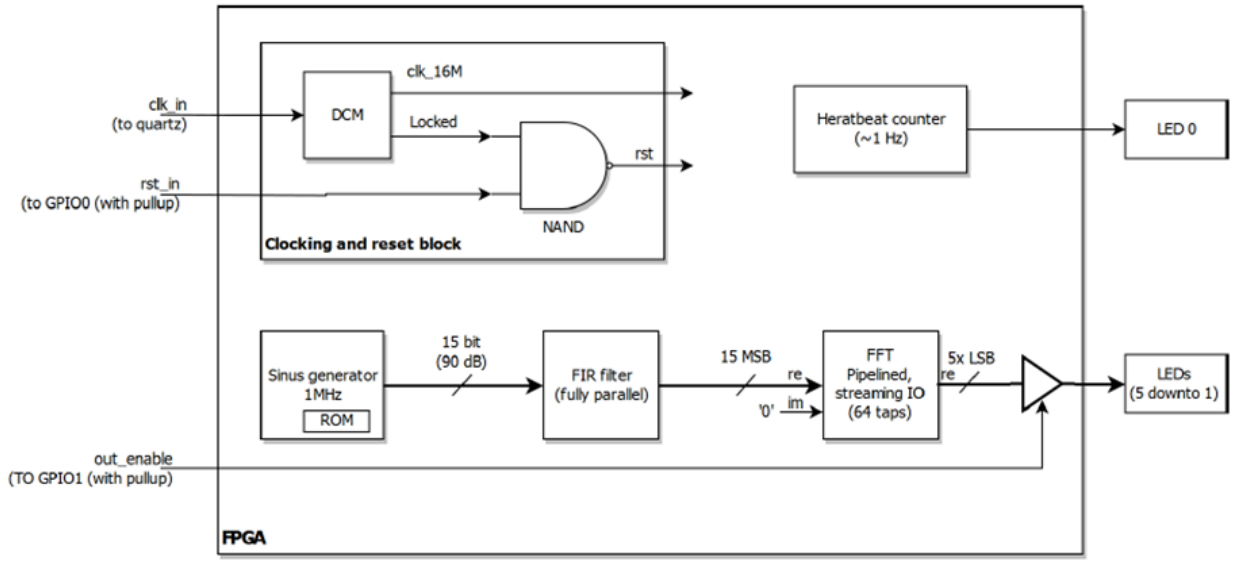

Figure II-79 Industrial application design block diagram

Using Xilinx tools, the power consumption and static timing reports have been generated. With the ICEM GENERATOR the extraction of the current sources corresponding to the activity of the different blocs of the FFT design in a SPICE format. After connecting the generated current sources to the PDN and board model, the simulation of the CE using a 1 Ω probe was performed. Figure II-80 presents a comparison between the measurement and the simulation in the time domain (left) and it shows a good correlation between the peak to peak amplitude of the simulated voltage (14 mV) and the measured voltage (13 mV). Figure II-80 (right) also presents the comparison between the measurement and the simulation in the frequency domain with a good correlation and a computed RMS error of 5.62 dBµV. Some differences between the measured and the simulated envelope could be due to any existing error on the different blocs of the ICEM-CE model. This result proves that the proposed algorithm to build IA Core model gives satisfactory result on an industrial case study. Moreover, the algorithm can be easily

implemented in a tool to automatize the model construction. As no extra steps are required and it is rapid, this is an approach adapted to the industry's needs.

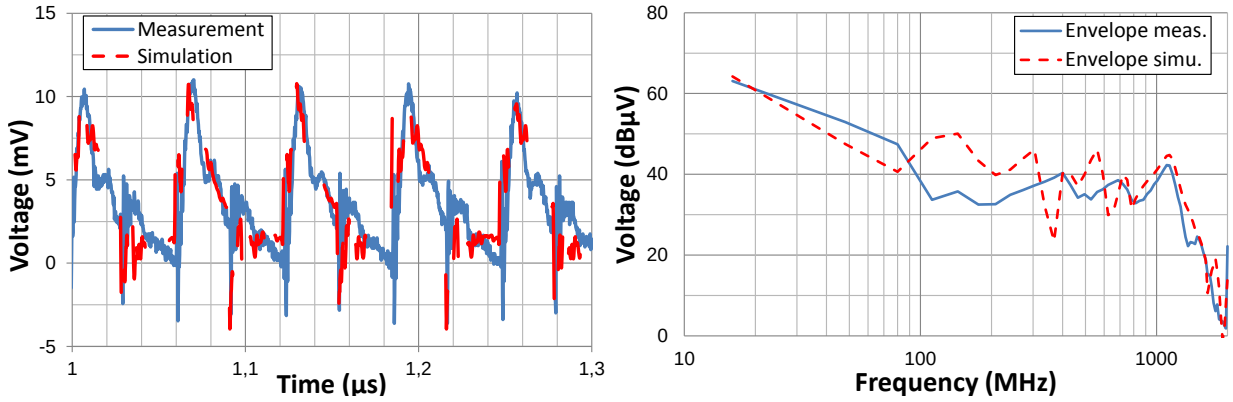

Figure II-80 Comparison between the measured and simulation CE using a 1 Ω probe in the time domain (left) and frequency domain (right) for the FFT test configuration

The constructed IA Core using ICEM GENERATOR tool has also been validated using CE simulation with the 150 Ω method. Figure II-81 presents a comparison between the measurement and the simulation and it shows that the simulated CE reproduces the tendency of the measured spectral envelope despite some differences that lead to an RMS error of 8.92 dBµV.

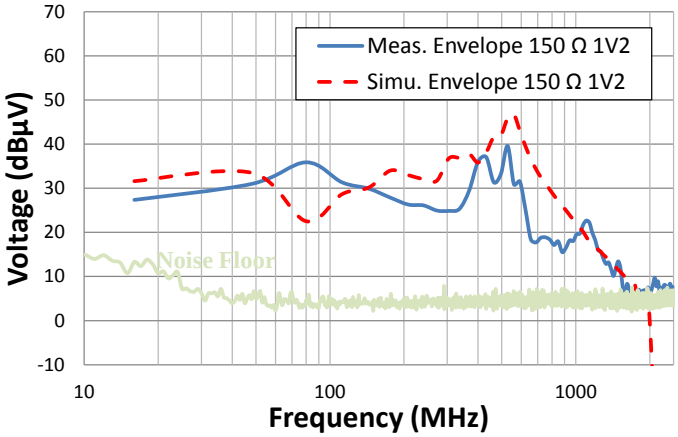

Figure II-81 Comparison between the measurement and simulation of CE on 1.2 V power plane using the 150 Ω probe for the industrial application

6. Conclusion

In this chapter, we have presented the purpose of ICEM-CE model and IBIS model for SI. The standardized method for ICEM-CE model construction is based on two different blocks: the PDN block which represents the propagation path of EM disturbance and it is generally modeled using an equivalent electric circuit constructed from S parameters measurements. The second block of ICEM-CE model is the IA block, which describes the noise generated by the switching activity of an IC; it is generally modelled using current sources. Several methods for IA block construction are proposed in the state of the art, but present several limitations as discussed in the second section of this chapter. Hence, the main difficulty in ICEM-CE model construction is the IA block extraction. An ICEM-CE model construction of a complex IC, a FPGA, was presented with the proposition of new methods of IA extraction.

The construction of ICEM-CE model of a FPGA was studied in this chapter, starting from the construction of the PDN model and the ELECIS-F board model. Several comparisons between the measurement and the simulation of the impedance were performed between the power and ground domains for the validation of the PDN and board model. The constructed model is valid up to 2.5 GHz. Then, the first approach studied for IA Core construction follows the standard inverse method based on the 1 Ω measurement. This methodology has several limitations due its dependency on the PDN and board model and it doesn't insure a correct level of the generated IA. As presented, this is related to the measurement and the estimation of transfer function errors that contributes in the absolute error of the IA construction. These limitations were observed in the comparison between the measured and simulated CE on the core power plane using a 150 Ω probe where the model overestimates the CE level.

As the extraction of the IA IO was isolated from the IA Core construction, a new approach for modeling the IO noise was proposed and compared the IA IO construction following the inverse method. The method is based on the integration of an IBIS file in ICEM-CE model to reproduce the transient profile of the activated output buffers. The comparison between CE measurement and simulation for different approaches shows using the IBIS file gives better results and allows compensating the HF noise.

Later in this chapter, a new methodology of construction of the IA Core block for ICEM-CE model of FPGA circuits has been presented, and the approach is based on the estimation of the dynamic power consumption. Firstly, the main idea is that whatever the internal dynamic current waveform is, the simulated conducted noise will not vary much if the transferred charge and the pulse duration are determined correctly. Secondly, the dynamic current of an integrated circuit depends mainly on three parameters: the dynamic power consumption, the toggle rate and the clock and data path delay. Using the estimation tools given by the manufacturers of FPGA, these parameters can be extracted rapidly and without extra steps in the FPGA design flow, and allow the modeling of the IA following two different approaches. The first approach consists in the construction of a stationary IA from the average value of the dynamic power and the toggle rate. This method under-estimate the peak-to-peak amplitude of the CE in the time domain, but it provides a good prediction of the envelope of the CE spectrum. On the other hand, a second approach is proposed for the construction of the IA. It is based on the estimation of the statistical

distribution of the toggle rates and the quantity of charge for all the active logic blocks. Different validation cases have been discussed and generally the comparisons between the measured and simulated CE spectrum present good correlations with measurement, and globally the envelope of the spectrum is predicted with a good approximation. The noted errors can be related to the extraction of the PDN block of ICEM-CE model, the assumptions of our proposed methodology and measurement accuracy. The main advantage of this approach is that it is independent from the external voltage measurement; hence, the inversed terms of the transfer function error that contributes in the IA construction absolute error are suppressed. Although the IA construction errors are not totally suppressed, they are reduced significantly.

The new presented methodology is adapted to FPGA and other integrated circuits when the manufacturer provides power and delay estimation tools to IC end-users. On the other hand, when the estimation tools are not provided, the principle is still adapted for CE prediction, but the needed parameter should be extracted from measurement. This methodology can be proposed within the ICEM standard as a guideline for IC end-users.

Finally, the developed ICEM GENERATOR tool has been presented. It allows the automatic generation of the IA bloc from the power and timing reports, and an industrial design was developed to validate the tool. In the next versions of ICEM GENERATOR tool, it will include an algorithm which allows the construction of the IA IO bloc. The tool will also be adapted to other IC families and will offer the possibility to construct the PDN model of an IC.

The proposed work has led to the construction of a predictive ICEM-CE model. However, after several operating lifetime, the predicted CE emission level could not be guaranteed, especially in the industrial applications where the ICs operate in harsh environment. The aging of ICs will trigger the degradation mechanisms presented in the last chapter according the operation conditions; hence, ICs reliability must be studied. In the next chapters, traditional and new approaches for reliability prediction will be presented. The objective is to study how the reliability and EMC models can be coupled to develop a predictive electromagnetic robustness model.

7. References

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Chapter III. Predictive reliability modeling

The different industrial applications such as the space, aeronautic and automotive industries are confronted with a strong global economic competition which sets economic constraints on the cost of the development of electronic functions. The use of Commercial Off-The-Shelf (COTS) components in embedded systems is increasingly necessary in order to reduce development costs and provide new functions.

However, the demand for electronic components comes mostly from the consumer sectors (telephony, computers, multimedia...). The requirement of these sectors is to provide, in fast development cycles, cost-effective technological innovations. These evolutions must integrate the specific constraints of embedded systems in terms of reliability, safety of operation, availability, maintenance in harsh environment and lifetime when implemented in Hi-Rel applications. The evolution of electronic devices to Very Large Scale Integration (VLSI) technology requires aggressive design rules and has led to the integration of a reliability prospection early in the design stages. In general, the reliability tests based on HTOL testing method are performed by the circuit manufacturer under standard nominal low stress conditions and do not guarantee the long-term reliability. Hence, it is mandatory for the industrial applications to characterize their electronic devices and equipment in order to investigate their performances and robustness. These constraints have obliged the industries to create guidelines and tools for the reliability prediction modeling.

On the other hand, EMC robustness has never been related to any existing reliability prediction model. It has always been characterized after standard accelerated test, but the EMC evolution as a failure in time has never been considered. Beforehand to the EMC robustness prediction that will be discussed in the Chapter V, the reliability modeling should be presented in order to introduce the existing mathematical laws for accelerated aging tests involving several degradation mechanisms. These degradations lead to the drift of operational parameters, as the timing performances of ICs, and can contribute to the drift in EMC level.

In the first section of this chapter, traditional and more recent reliability predictive guidelines and models used in the different industries will be introduced. Since these models are based on accelerated testing, the second section will concern the general reliability laws and models for accelerated tests. Finally, in the last section the new methodology of reliability prediction for modeling a multi-stress life-test proposed by J. Bernstein [27] will be presented.

1. Historical perspective of reliability prediction

1.1. General purpose of reliability prediction

The reliability is the ability of an item (system) to perform a required function under stated operation and maintenance for a specified period of time. Another concept definition is the dependability e.g. the ability of an item to perform a required function without failure under stated conditions for a stated period of time. The reliability of non-repaired items is due to the complexity to their dependability. The integration of microelectronic circuits in the various

industrial fields is limited by the reliability of the required product. The electronic components have strong constraints in terms of design rules for low operating voltages and maximum switching frequencies. To predict the reliability of an electronic component, a reliability model must be calculated for specific operating conditions. The concept of modeling and prediction of reliability emerged recently during the Second World War, when complex military electronic equipment had presented high failure rates [1]. From an operational point of view, the reliability of an electronic component is described with a "bathtub curve" representing failure rates λ(t) as presented in Figure III-1.

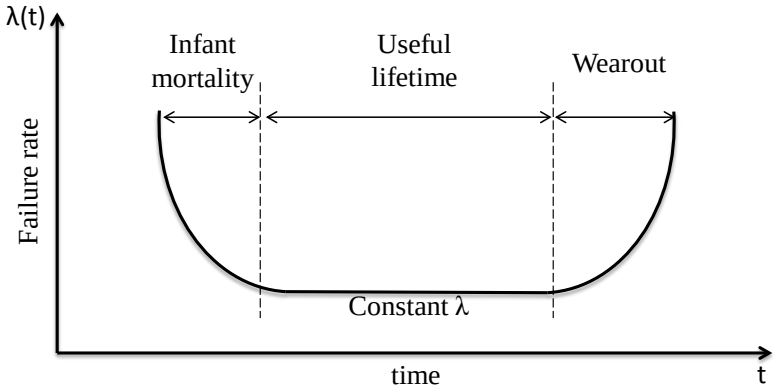

Figure III-1 Bathtub curve principle

The failure rate characterizes the change in the dependability of an item in the course of it lifetime. A typical "bathtub curve" has three major portions or periods of operating lifetime discussed previously, which are: infant mortality period, useful lifetime period and wearout period. The encountered defects during these periods have different origins [20]:

- Systematic failure due to defects in process or manufacturing. It will be manifested throughout the product's mission. They must be detected during the design validation tests (Design Validation) and during the manufacturing process validation (Product Validation). This region is dominated by manufacturing defects (materials with extremely low breakdown strength) and shows rather sharp reduction in failure rate time. This portion (higher failure rate region) can last for a year or more at normal operating voltage and temperature conditions. To avoid such very high failure rates at start, the supplier may sometimes choose to exercise the devices for a period of time (to eliminate the defective devices) before sending the product to their customers. This period of time, in which the devices are exercised to eliminate the defective devices, is often called burn-in.
- The random failure portion is due to very small defects in the materials (which tend to reduce the breakdown strength of the materials). The failure rate that is observed at the bottom of the bathtub curve is nearly constant and is due primarily to those intrinsic weaknesses found in population of otherwise good devices. This portion of curve is referred to as the intrinsic failure rate region. As λ is constant, the statistical distribution is described by the Poisson distribution often used in physics, engineering and manufacturing. It is used to describe the probability of occurrence for discrete random

events/processes. Random processes refer to physical events which are controlled purely by chance.

- Wearout defects, which must only appear after the end of the product's mission, are linked to aging. Indeed, if devices are operated long enough, they will eventually start to fail even though the material strengths may be excellent. The wearout region is correlated with the material type selection, design rules used, and the use conditions.

As seen in the previous chapters, the failure rate λ is an essential parameter to characterize the reliability of DSM components. The failure rate of each component must be estimated to compute the failure rate at the equipment level. For aeronautic applications, the failure rate must meet the requirements defined by the Design Assurance Level (DAL) described in the DO254 standard [2] and which presents the acceptable failure rates associated with a criticality level as shown in the Table III-1.

DAL classification	Criticality level	Acceptable failure rate (FIT)
A	Critical	1
B	Essential Hazardous	100
C	Essential Major	10^4
D	Non Essential	10^6
E	No Safety Effect	

Table III-1 Criticality level defined by DAL for aeronautic application in the standard DO254 [2]

The reliability prediction has therefore become a common notion in the reliability analysis. It allows the prediction of the failure rate of a component or an entire electronic system in order to evaluate the feasibility of the design and compare it with the various alternative designs. Reliability prediction also helps identify areas of potential failure, trade-off system design factor and track reliability improvement.

1.2. History of reliability prediction approach

1.2.1 Traditional reliability prediction approach

For a collection of devices, it is critically important to be able to understand the expected failure rate for the devices. For the supplier of such devices, the expected failure rate will be an important indicator of future warranty liability. For the customer, the expected failure rate will be an important indicator of future satisfaction. For high reliability mission applications, it is of paramount importance for one to know that the expected failure rate will be extremely low. Design engineers are continually asked reliability questions such as: how long is your newly designed device/product expected to last? And how can you make cost-effective design changes to improve the reliability robustness of the device?

As discussed before, in order to develop reliable electronic equipment, reliability issues should be taken into account earlier in the product development process. The needed information on the reliability of electronic components has led to the creation of reliability prediction models.

Until 1980's, the CFR (Constant Failure Rate) model (or the exponential model) has been widely used for the reliability modeling [3]. It was the only model to describe the useful life of an electronic component. From a mathematical point of view, the reliability R(t) of an electronic component or system represents the probability that it remains functional between time t_0 and an instant t. Assuming that it is operational at $t_0 = 0$, thus, the CFR model is given by Equation III-1.

$$R(t) = e^{-\lambda t} \quad \text{(III-1)}$$

The CFR model describes the failure distribution of a system appeared due to random events. However, since the introduction of complex ICs in the 1990's, the experiments have shown that the CFR model was no longer applicable. This is due to the dominance of infant mortality and wearout failures that appears prematurely for advanced CMOS circuits.

In 1962, the US Department of Defense has prompted a request for a military guideline for the reliability prediction of electronic equipments. Hence, on the basis of the CFR model, the military handbook known as MIL-HDBK-217 standard has been developed by RADC (Rome Air Development Center) [4] and became the reliability prediction reference for industry. Several updates of the military standard have been published until 1995; that results on MIL-HDBK-217F version. Since then, the standard has not been updated but is still widely used by military industry. In 1991, according the researches of IIT Research Institute/Honeywell SSED and the Westinghouse/University of Maryland, the CFR model was no longer recommended for updating the MIL-HDBK-217 model [5].

In the MIL-HDBK-217F standard, the expression used to estimate the failure rate for most traditional prediction methods is modified by several factors π; e.g. the configuration factor π_{CF}, the quality factor π_Q and the environmental factor π_E. The reliability prediction model is based on the effect of mechanical, electrical and environmental stress (temperature, humidity, voltage, current, vibration ...), so the failure rate varies according to the applied stress. For example, the failure rate of a microelectronic circuit can be expressed using Equation III-2, where λ_p is the part failure rate, π_T is the temperature acceleration factor, π_E is the environmental factor, π_Q the quality factor and π_L is the learning factor which considers the maturity of the device manufacturing line, C_1 and C_2 are the complexity of the die based failure rate (such as the number of gates) and the complexity of the package type (such as the pin count) [6].

$$\lambda_p = (C_1.\pi_T + C_2.\pi_E)\pi_Q.\pi_L \quad \text{(III-2)}$$

In 2004, a consortium of 8 French aeronautical and military industries have developed a new guide for reliability prediction under the supervision of the French Department of Defense DGA (Direction Générale de l'Armement), the reliability prediction guideline is named FIDES [7]. The main goals of FIDES development are various. It allows a realistic assessment of the electronic equipment reliability, including electronic systems operating in harsh environments (defense, aeronautic, industrial electronics, transport...), and provides a concrete simulation tool for reliability prediction. This approach takes into account intrinsic failures as well as the extrinsic failures resulting from equipment specification, and design data. It considers failures resulting from development, manufacturing process and the over-stress linked to the application. The

failure rate estimated by FIDES could be expressed by Equation III-3, where λ_{Phy} is the physical contribution, $\pi_{Manufacturing}$ is the manufacturing quality factor and $\pi_{Process}$ is the process quality factor.

$$\lambda = \lambda_{Phy} . \pi_{Manufacturing} . \pi_{Process} \quad \text{(III-3)}$$

In 2005, a new reliability prediction guide was published by the UTE (Union Technique de l'Electricité). The guide is known as RDF2000 (or UTE C 80-810) and is based essentially on the telecommunications industry data [9]. It allows calculating the failure rates of the electronic components mounted on a PCB. However, the factors influencing the failure rate can be defined with a good accuracy according to a mission profile [10]. At the transistor level, the failure rate could be expressed using Equation III-4, where λ_{die} is the die failure rate, $\lambda_{package}$ is the package failure rate and $\lambda_{overstress}$ is the failure rate related the applied over-stress.

$$\lambda = \lambda_{die} + \lambda_{package} + \lambda_{overstress} \quad \text{(III-4)}$$

For the same electronic component operating in a given environment, the failure rate was calculated using the different traditional approach presented above [10]. The Table III-2 presents the failure rate calculation results in FIT (Failure In Time) which means the number of failure in 10^9 hours. These results show that the MIL-HDBF-217F is the most pessimistic reliability prediction approach giving a higher failure rate than the other reliability approaches. These results are explained by the formulas used for the failure rate calculation and the elements taken into account. For the MIL-HDBK-217F, the failure rate expression is multiplicative, and therefore any slight modification of the formulas' parameters leads to a highly variation in the result. Moreover, unlike to the RDF2000 and FIDES standard, it does not take into account a real mission profile and several data have to be chosen from a limited data base.

	MIL-HDBK-217F	**FIDES**	**RDF2000**
λ (FIT)	7500	20,1	19,8

Table III-2 Failure rate values for an electronic component [10]

In 1958, the Electronic Industries Alliance (EIA) has created the JEDEC (Joint Electron Device Engineering Council) as an independent solid state engineering organization for semiconductors. The early work of JEDEC was about testing methods and product standards. Since then, the standard was widely used by electronic industry. The JEDEC allows the modeling of electronic devices' reliability on the basis of specific testing methods and reliability laws for FIT prediction. However, similarly to MIL-HDBK-217 standard, it only models the reliability of components for the two first stages of a bathtub curve and is based on the activation of a single degradation mechanism.

In general, the most prevalent method in the industry for the reliability of electronic components is to use prediction guidelines. These guidelines are based on empirical failure rate models derived from reliability feedback data given from users or manufacturers' experiments. Several prediction guidelines exist, and are adapted to the needs of different industries as shown in the Table III-3.

Procedural Method	Application
MIL-HDBK-217	Military
Telcordia SR-332	Telecom
CNET	Ground military
RDF-93 and 2000	Telecom
SAE Reliability Prediction Method	Automotive
BT-HRD-5	Siemens product
Siemens SN29500	Telecom
NTT procedure	Commercial and Military
PRISM	Aeronautical and Military
FIDES	Aeronautical and Military

Table III-3 Procedural method and application for reliability modeling

1.2.2 Physics-of-Failure approach

Physics-of-Failure (PoF) is a recent reliability prediction method. When it has been proposed by RCA (Root Cause Analysis) in 1973, it was rejected because of the lack of required data for reliability prediction. PoF is based on the analysis of manufacturing parameters, considering the fabrication technology, process, materials and packaging for the investigation of the failure point locations [14]. However, PoF approach was integrated in the military handbook in the 1990s to overcome the weakness of the traditional approach with the development of advanced technologies. The PoF model principle was summarized by [1] and consists in:

- The identification of potential failure mechanisms
- Accelerated stress to identify the most dominant root-cause of failure
- Identification of the dominant failure mechanism
- Modeling the failure mechanism
- Making the link between the collected data from the accelerated stress and the statistical distribution
- Developing a mathematical model for the dominant failure mechanism and compute the MTTF (Mean Time To Failure)

The main limitation of this approach is that it requires detailed information on manufacturing parameters that could be confidential. Thus, a statistical analysis is used to create a modified PoF approach. To help the assessment of PoF approach for reliability prediction, two computer-based modeling and simulation tools have been created; Computer-Aided Design of Microelectronic Packages (CADMP-2) for the assessment of electronic components at package level, and Computer-Aided Life-Cycle Engineering (CALCE) for the assessment of electronic components at printed wiring board level [13]. To assess the complexity of PoF approach, the inputs and outputs of CADMP-2 and CALCE tools for reliability prediction are presented in Figure III-2 and Figure III-3.

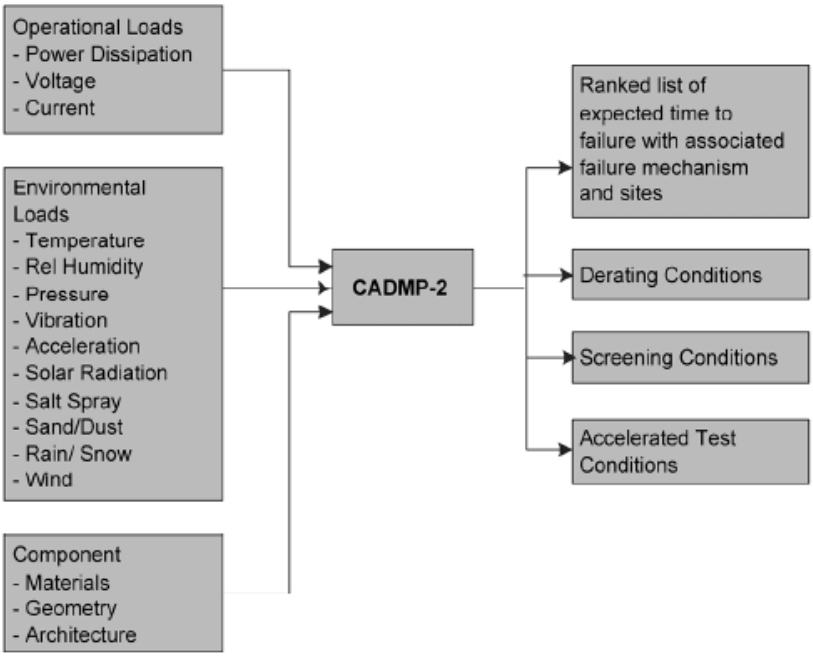

Figure III-2 Inputs and outputs of CADMP-2 tool [1]

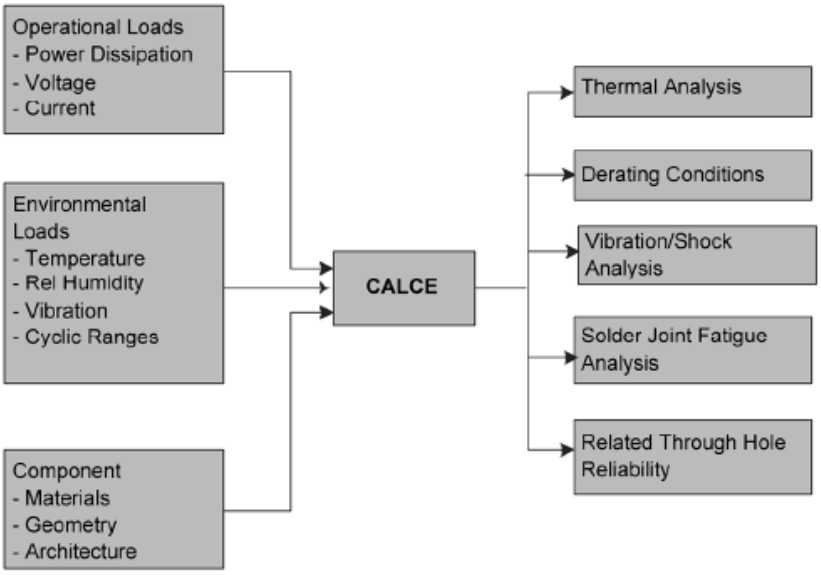

Figure III-3 Inputs and outputs of CALCE tool [1]

As stated by [5], the objective of PoF approach is the "*development of mixture models which consider both early and premature wearout failures caused by the displacement of the mean and variability due to manufacturing, assembly, handling, and misapplication*".

1.2.3 Most recent reliability prediction approach

In the previous section we have discussed what are the limitation and drawbacks of existing reliability models and why they need to be revisited. Most recent reliability prediction approaches have been proposed. Academic researchers have developed a new method to estimate the

reliability of a system at its functional level such as a microprocessor. In 2003, IBM (International Business Machines) published the Reliability Aware Micro-Processor (RAMP) model which is a permanent fault analysis tool for reliability prediction [11]. Different failure mechanisms are described at the transistor level and contribute to the circuit aging.

RAMP uses a proprietary electrical simulator and an academic temperature simulator to construct the circuit degradation model. This model is constructed by hierarchical combination of single element failure models and by the physics of failure phenomenon. RAMP allows the construction of a generic system failure model, based on the transistors failure time equations [12]. It only models intrinsic processor failures because long-term processor reliability is dominated by wearout and/or intrinsic failures. RAMP is based on Arrhenius model that will be described later, to show the dependence of processor failure on the temperature [1]. The model assumes that all failure mechanisms have constant failure rate. Although the assumption is inaccurate, it allows the combination of different failure mechanisms and it gives only one MTTF calculation based on the most dominant degradation mechanism. RAMP model is constructed from the sum of failure rates model considering that each structure on a chip separately with different failure mechanisms and failure rates.

Today, reliability models are an integrated phase of electronic circuits design process. The dedicated simulators to reliability prediction allow the modeling of the minimum lifetime before the activation of one of the most significant degradation mechanisms that were presented in Chapter II. With the advancement of CMOS technologies, a circuit integrates tens of thousands of transistors that will not be stressed and thus not degrade in the same way during their operating lifetime. Thus, reliability modeling is based on statistical approaches applied to the most dominant degradation mechanism. The new approach must take into consideration that the failure mechanisms are coexisting and depend both on intrinsic and extrinsic failure mechanisms all of them occurring simultaneously in parallel at their own rate governed by the environmental and biasing condition of use. Thus, the final reliability figure of a complex IC chip is described by statistical generation of failure modes randomly activated in various region of the chip (e.g. designed area). These degradation mechanisms could be activated with accelerated aging stress, as HTOL tests presented previously, in order to analyze the reliability of ICs.

1.2.4 Limitations of presented reliability prediction approaches

Despite the variety of traditional reliability prediction techniques, they suffer from several limitations. The MIL-HDBK-217F has not been updated for more than 20 years and the majority of the techniques developed later are derived from this standard. Furthermore, this standard is based on return of experiment and lesson learned not really yet known for new emerging processes. Moreover, the traditional approaches are based on the CFR model; they only allow modeling of the degradations during the useful life that occur mainly in a random manner.

On the other hand, RDF2000 suffers from insufficient recognition from the international scientific and industrial community, in particular because the conditions for validation and testing of the electronic components are not well known. Indeed, the relevance of the proposed modeling

approach is not guaranteed for certain predominant environments, such as storage or any other severe environments.

In addition, the construction of reliability prediction models with more recent approaches is complex because of the number of necessary parameters to take into account for the product lifetime modeling.

Overall, the existing reliability prediction approaches are based on separating the variables and consider a single stress at a time and a single failure mode and mechanism at a time. This is due to the fact that the present guidelines are based on testing methods that accelerates only one mechanism. Although the semiconductor industry has extremely advanced in understanding the processes and the failure mechanisms, qualification for failure rate has not improved. Standard HTOL for reliability testing presents the activation of several failure mechanisms (e.g. NBTI, HCI, TDDB…) even if it only models the most dominant one. New approaches should be studied to take into account the eventual combination between the different degradation mechanisms; hence, a special focus will be given on multiple stress testing methods in the last section.

2. Acceleration models for reliability prediction

2.1. General overview on accelerated tests

Aging of systems and components structures becomes a serious requirement in order to judge the adequacy of measurements intended to keep equipment in service within or beyond their initial lifetime. The Accelerated Tests (Accelerated Life Tests) method is one of the most common approaches for estimating reliability or other behavioral characteristics (failure rate, failure time…). This method is based on observations on electronic systems or components in short time duration. These tests consist in reducing the lifetimes of products by the acceleration of the phenomena causing the failure. For this, the stress levels (Voltage, temperature…) sustained by the electronic component are increased in order to obtain life data faster, and then used to assess the reliability under the nominal operating conditions. The extrapolation of the information obtained on accelerated experiments requires an accelerated model, in order to deduce the component behavior under unobserved constraints [20].

The objective of accelerated aging is twofold:

- Reduce the aging tests duration.
- Assess the reliability of a material according to its use conditions and environment.

This type of test should not be confused with:

- Aggravated tests outside the qualification field to assess the robustness of the design and to reveal some modes of failure (HALT: Highly Accelerated Life Test).
- The screening tests carried out to reveal the infant mortality breakdowns (HASS: Highly Accelerated Stress Screen).

The acceleration tests allow the construction of a reliability function $R_n(t)$ for a chosen stress conditions s_n, where n is the number of stress realized for different stress conditions. Thus, considering a transfer function commonly named the acceleration law that could be computed from the trend of the reliability functions of several stress conditions, the acceleration tests leads

to determine the reliability for the nominal conditions. The principle of an accelerated test is described in Figure III-4 [16].

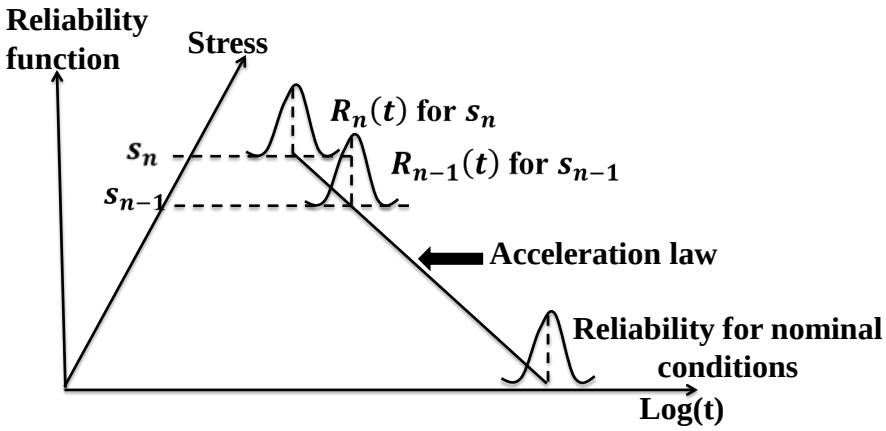

Figure III-4 Principle of an accelerated test

In general, acceleration tests rely on the standard Accelerated Lifetime Model (ALM) that assumes that a stress or a combination of several stresses change only the reliability curve scale. Hence, for a reliability function, the acceleration factor AF allows simply to go from an operating time under accelerated conditions t_{acc} to that at nominal conditions t_{nom} for the same reliability criterion, as described in Figure III-5. The acceleration factor corresponds to a degradation rate ratio under different stress levels; it is defined for several accelerations laws that will be presented later.

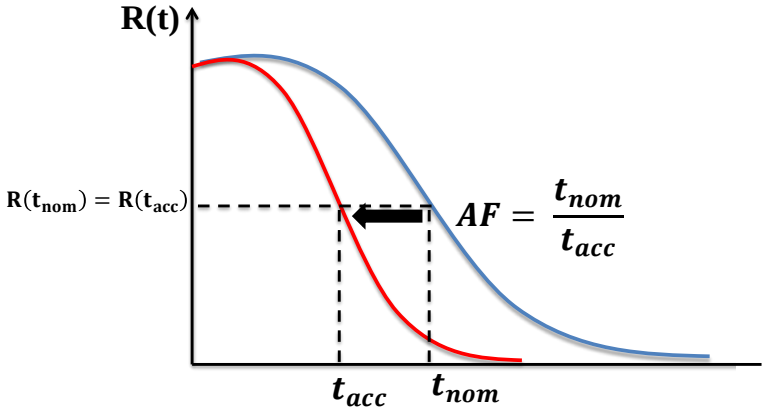

Figure III-5 Principle of standard Accelerated Life Model

The accelerated tests must be carried out according to a test plan which includes:

- The stress conditions accelerating the failure mechanism
- The stress levels ensuring that the original failure mechanism is maintained while acceleration test is applied
- The size of tested samples for the statistical analysis giving the accuracy of the estimations
- The acceleration law to analyze the test results in order to define the reliability function under the nominal conditions

The construction of a test plan for accelerated life tests is conditioned by the following information:

- The failure mode known as the electrical parameter (indicator) related to the degradation mechanism, to be measured periodically in order to determine the degree of aging of the product (it can be absolute or relative drift)
- The relevant failure criteria and the associated time to reach it: hence the TTF (Time To Failure) will be the series of time experiments measured on a given lot (e.g. the number of identical products submitted to every stress test) which corresponds to 50 % of the lot reaching this failure criteria.
- The various stress test conditions to be carried out and set generally at high temperature and biasing conditions required to experimentally deduce the TTF and then deduce the accelerating factors for a given single failure mechanism to calculate the TTF at nominal biasing and temperature conditions.

2.2. Scale reliability laws

Acceleration factor is always associated to a scale reliability law. The mathematical definition of a scale reliability law is given by Equation III-5, where R_0 is a standard reliability law accepting additional parameters called form factors, α and β are positive known or unknown parameters [21].

$$R(t) = R_0[(\frac{t}{\alpha})^{\beta}] \quad \text{(III-5)}$$

The scale parameter α accept a linear scale change when a multiplication factor k is introduced; assuming that t_r is a random lifetime; the scale change is described by Equation III-6:

$$t_r \sim R(t, \alpha, \beta) \implies k.t_r \sim R(t, k\alpha, \beta) \quad \text{(III-6)}$$

The most commonly used scale reliability laws are the exponential law, Weibull's law and the log-normal law.

- **The exponential law**:

The exponential law is calculated for a constant failure rate λ as shown in Equation III-7; its MTTF is calculated using the Equation III-8. The exponential law was the first law used in reliability, for its simplicity, and because it allows to model the reliability of the components in their longest useful life [17].

$$R(t) = e^{-\lambda t} \quad \text{(III-7)}$$

$$MTTF = \int_0^{\infty} R(t)dt = \frac{1}{\lambda} \quad \text{(III-8)}$$

- **Weibull's law**:

Weibull's law is a reliability law with two parameters: the scale factor η (hour) and the form factor β (without unit). The reliability law and its MTTF are given in Equations III-9 and III-10, where Γ is the generalization of the factorial function for real positive numbers, its expression is given in Equation III-11. By associating the three evoked possibilities of the failure rate evolution

in the bathtub curve, Weibull's law can represent the three stages of a components' life: early failure ($0<\beta<1$), useful life ($\beta=1$) or wearout failures ($\beta>1$). Thus, Weibull's law is very often used in reliability to model the distribution of components' lifetime [18].

$$R(t) = e^{-(\frac{t}{\eta})^{\beta}} \quad \text{(III-9)}$$

$$MTTF = \eta.\Gamma(1+\frac{1}{\beta}) \quad \text{(III-10)}$$

$$\Gamma(\alpha) = \int_0^{\infty} t^{\alpha-1}.e^{-t}dt \quad \text{(III-11)}$$

- **The Log-Normal law**:

The Log-Normal (LN) law is a reliability law with two parameters: the expectation μ and the standard deviation σ. If a random variable X follows a normal distribution N(μ,σ) then exp(X) follows the Log-Normal law LN(μ,σ). The Log-normal distribution is a frequently used model in reliability because it concerns positive random variables, and the form parameter σ allows various reliability representations [19].

$$R(t) = \int_t^{\infty} \frac{1}{t.\sigma.\sqrt{2\pi}} e^{-\frac{1}{2}(\frac{\ln(t)-\mu}{\sigma})^2} dt \quad \text{(III-12)}$$

$$MTTF = e^{(\mu+\frac{\sigma^2}{2})} \quad \text{(III-13)}$$

2.3. Accelerated lifetime models

To estimate the reliability of an electronic component, accelerated life models were proposed according to the stress conditions accelerating the degradation mechanisms (temperature, voltage, vibration, humidity ...). In order to estimate the lifetime of an electronic circuit or system, time-limited tests are carried out and lead to the computation of acceleration factor giving the ratio between the constant test stress parameter and the predicted operating parameter. This variable allows the construction of accelerated lifetime models.

The modeling of accelerated lifetime is made in two independent steps [20]:

- The choice of a parametric family with scale factor of reliability laws for modeling the lifetime under a given stress level. As we saw earlier, the most widely used laws are the exponential laws, Weibull's law or log-normal law.
- The choice of a functional relation allowing to express the acceleration factor AF as a function of the numerical stress conditions using parameters to be specified or to be estimated statistically

When applying a mono-stress acceleration test, the acceleration factor AF is expressed with a log-linear function, considering a stress parameter X with two different values (X_0, X_1):

$AF(X_0,X_1) = \exp(a_0+a_1.B_1)$ where B_1 is dependent of X_1 : $B_1 = f(X_1)$.

The multi-stress acceleration test is when several parameters are combined (voltage, temperature, humidity…). Its acceleration factor is constructed from the mono-stress acceleration factors; considering two stress conditions X and Y, the multi-stress AF is given by Equation III-14.

$$AF([X_0, Y_0], [X_1, Y_1]) = AF_X(X_0, X_1).AF_Y(Y_0, Y_1) \quad \text{(III-14)}$$

Where AF_X is the acceleration factor due to stress X and AF_Y is the stress acceleration due to stress Y. The interaction between the stresses X and Y is not considered.
Classical laws for the acceleration factor modeling have been constructed and are dependent on the applied stress conditions. The most commonly used acceleration lifetime models are described in this section.

2.3.1 Arrhenius law of temperature

The Arrhenius law is the basis of the reliability models for temperature-induced degradations. It was originally formulated by Arrhenius [22] and later resumed by Eyring [23]. Arrhenius law is an experimental law derived from the Transition State Theory (TST) which aims to explain kinetic reactions for elementary chemical reactions.
Arrhenius law of temperature is expressed mathematically as an exponential law and leads to the calculation of an acceleration factor for thermal stress accelerating the failure as given by Equation III-15:

$$AF = e^{\left[\frac{E_a}{K}\left(\frac{1}{T_0}-\frac{1}{T_1}\right)\right]} \quad \text{(III-15)}$$

Where T_0 is the reference temperature (Kelvin), T_1 is the acceleration temperature (Kelvin), K is Boltzmann's constant (8,6 10^{-5} eV/K) and E_a is the activation energy (eV) which represent the minimum energy needed by a molecule to participate in a reaction that activates the failure mechanism. E_a is an unknown parameter, and must be estimated statistically from experiments using different stress conditions. Usually, E_a varies between 0,3 and 2 eV. For some electronic application, the activation energy is fixed according to a selected failure mechanism [7].

2.3.2 Inverse Power Law (IPL)

The Inverse Power Law for accelerated test modeling is a general law that describes the effect of an electric stress (voltage, current) or the amplitude of thermal cycling or mechanical stress. The general expression of the AF of IPL is given by Equation III-16.

$$AF(S_0, S_1) = \left(\frac{S_1}{S_0}\right)^{\alpha} \quad \text{(III-16)}$$

Where S_0 is the reference stress level, S_1 is the accelerated stress level and α is the acceleration parameter.

2.3.3 Peck's law for temperature humidity

Peck's law is an accelerated lifetime model for the characterization of combined temperature and humidity stresses. It is issued from Arrhenius law of temperature and the IPL for relative humidity. It is described with the Equation III-17.

$$AF([T_0, RH_0], [T_1, RH_1]) = \left(\frac{RH_1}{RH_0}\right)^{n} . e^{\left[\frac{E_a}{K}\left(\frac{1}{T_0}-\frac{1}{T_1}\right)\right]} \quad \text{(III-17)}$$

Where T_0 and T_1 are the reference and acceleration temperature respectively (Kelvin), RH_0 and RH_1 are the reference and acceleration humidity level (%), k is Boltzmann's constant and E_a is the activation energy, n is the humidity effect parameter. n is an unknown parameter but it could be estimated with accelerated tests under different stress conditions.

2.3.4 Coffin-Manson based law for mechanical fatigue

Coffin-Manson based law for mechanical fatigue allows the modeling of cycling stress effect on reliability. The stress is modeled using a periodic profile of the parameter of acceleration (temperature, voltage…). The acceleration factor of Coffin-Manson based law is given by Equation III-18.

$$AF(T_0, T_1) = \left(\frac{\Delta T_1}{\Delta T_0}\right)^p . \left(\frac{f_0}{f_1}\right)^q . e^{\left[\frac{E_a}{K}\left(\frac{1}{T_0}-\frac{1}{T_1}\right)\right]} \quad \text{(III-18)}$$

Where ΔT_0 and ΔT_1 are the temperature change in use and accelerated environment respectively, f_0 and f_1 are the frequency of thermal cycle in use and accelerated environment, p and q are the parameters that characterize the effect of the difference in the amplitude and the frequency respectively.

2.3.5 Black's law

Black's law is a commonly used law with 2 stress parameters that describes the effect of the temperature and current density on IC interconnects involving electromigration mechanism. The equation that used for Black's law is a combination of Arrhenius law of temperature and the IPL for current density (J) as given by Equation III-19.

$$AF([T_0, \Delta J_0], [T_1, \Delta J_1]) = \left(\frac{\Delta J_1}{\Delta J_0}\right)^n . e^{\left[\frac{E_a}{K}\left(\frac{1}{T_0}-\frac{1}{T_1}\right)\right]} \quad \text{(III-19)}$$

2.3.6 Generalization

The general concept of accelerated law for multiple stresses $X_1, X_2 \ldots X_p$ is constructed considering the different acceleration laws presented above including the effect of each stress (Arrhenius law, IPL, exponential law) [8]. The transformation of the stress function is expressed by:

- V = 1/T for Arrhenius acceleration law
- V = ln(X) for the IPL
- V = X, for the exponential acceleration law

These transformations lead to the general acceleration factor for multiple stresses expressed by Equation III-20 named the log-linear modeling of the acceleration factor.

$$AF\left[(X_1, \ldots, X_p)_{base}, (X_1, \ldots, X_p)_{acc}\right] = e^{[\alpha_1(V_{1base}-V_{1acc})]} . e^{[\alpha_2(V_{2base}-V_{2acc})]} \ldots e^{[\alpha_p(V_{pbase}-V_{pacc})]} \quad \text{(III-20)}$$

2.3.7 Boltzmann Arrhenius Zhurkov (BAZ) model

BAZ model is a mathematical generalized model also derived from the Transition States Theory similarly to Arrhenius law. As shown in Figure III-6, this model assumes that one or more external stress acts as a catalyst for the reaction and decreases the activation energy required to switch from an initial nominal operating state to a final state of failure.

The model is valid providing the following hypotheses are verified:

- Same failure mechanisms are activated under various stress conditions: same life distribution shape and no new mechanism created.
- Several failure mechanisms may co-exist.
- Static stresses or constant stress are considered (stresses are not time dependent).
- Accelerating factors due to several stresses are independent: no interaction between the stresses $X_1 \ldots X_p$.

$$AF\left[(X_1,\ldots,X_p)_{base},(X_1,\ldots,X_p)_{acc}\right] = AF_1(X_{1base},X_{1acc})\ldots AF_p(X_{pbase},X_{pacc}) \quad \text{(III-21)}$$

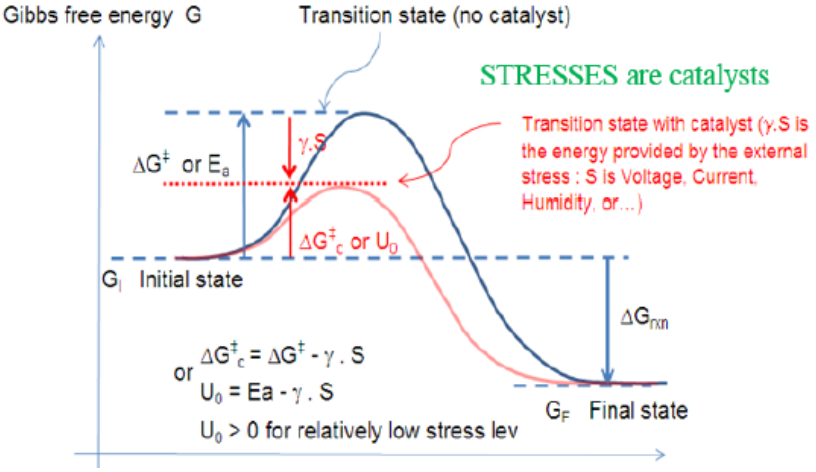

Figure III-6 External stress effect on the activation energy [20]

The Time To Failure (TTF) expression of BAZ model is given in Equation III-20, where E_a is the stress-free energy and γS is the energy provided by the external stress. In Zhurkov's tests S was a constant mechanical tensile stress, but it has been demonstrated that S can be any other stimulus (Voltage, current, humidity…) considered as a stress [24]. The effective activation energy is given in Equation III-23.

$$TTF = \tau_0 e^{\left(\frac{E_a-\gamma S}{K.T}\right)} \quad \text{(III-22)}$$

$$E_{a,eff} = E_a - \gamma S \quad \text{(III-23)}$$

BAZ model can be considered as a generalized model of existing reliability laws. Its use is particularly suited to multi-stress environments. It is also adapted to describe an electronic component or system by relating stress to a variation of an electrical parameter which is limited by a maximum acceptable value [10].

3. The Multiple Temperature Operational Life (MTOL) method

3.1. Introduction to MTOL model

The transistors technology advancement has involved strong requirements in the reliability of electronic components and systems. Until this day, manufacturers of electronic components are able to provide an expected reliability value in terms of FIT knowing that it is defined as a

function of an acceleration factor as expressed by the Equation III-24. FIT rate is calculated using Chi-square distribution at 60 % confidence interval from the small number of failures and limited sample size of the population tested. The Chi-squared value is calculated from the inverse Chi-squared distribution using the desired probability level and degrees of freedom. The failure rate is then calculated from the Chi-square value

$$\mathrm{FIT} = \frac{\chi^2(2f+2)}{2.\text{Device Hours.AF}}.10^9 \qquad \text{(III-24)}$$

Where χ^2 is the Chi-squared value at 60 % confidence level and (2f+2) the degrees of freedom, where f is the number of failures. The device hours is the number of the devices multiplied by the number of hours.

Using the standard HTOL test or other standard reliability testing methods, the electronic circuits' manufacturers report the zero-failure criterion corresponding to specific stress conditions for a single failure mechanism, which does not provide relevant information on the reliability prediction. Furthermore, HTOL test does not provide sufficient statistical data and the accelerated test is usually established for low stress conditions that guarantee the zero failure criterion. This approach could be acceptable when considering a single dominant degradation mechanism that is activated with temperature and/or voltage over-stress. Knowing that the acceleration factor is a non-linear function, it is expressed by multiplying the temperature acceleration factor AF_T and the voltage acceleration factor AF_V; thus the total acceleration factor AF is given by Equation III-25 [27].

$$\mathrm{AF} = \mathrm{AF_T}.\mathrm{AF_V} \qquad \text{(III-25)}$$

This term is widely used by industrial standards for reliability characterization. Yet, it is limited to modeling reliability for dielectric breakdown mechanism. However, the most accurate assumption is to consider that several failure modes are operating simultaneously and competes with each other to cause failure. This is not supported by HTOL testing methods since it considers that only one failure mode is dominant and is acting on the device. A new approach for modeling the multiple failure mechanisms was proposed by J. B. Bernstein [28] as a Multiple High Temperature Operational Life (M-HTOL) approach and will be discussed in detail in this section.

3.2. Presentation of the MTOL method

3.2.1 Reliability prediction for multiple mechanisms with matrix solution

The main principle of MTOL method is to identify the operating degradation mechanisms in an electronic circuit and to consider each failure mode as a sub-component. It has been demonstrated considering the voltage and temperature over stress, but is still applicable for other type of stresses (humidity, vibration…). Then, the failure rate of an IC for a given stress of temperature and voltage is computed as the sum the sub-components' failure rates. This approach is supported by the latest JEDEC standard JEP-122G which states that "*when multiple failure mechanisms are involved, then a proper summation technique, e.g, sum-of-the-failure-rates method is required*"

[12]. Thus the calculation of the FIT_i for a given degradation mechanism i leads to calculate the total FIT of the circuit, as described by Equation III-26.

$$FIT = \sum_i FIT_i \quad \text{(III-26)}$$

In order to solve the theoretical combination of the different laws modeling the degradation mechanisms, a matrix-based approach has been studied and allows linking the different acceleration factors of each degradation mechanism to the corresponding MTTF or failure rate.

This method is based on the results of measurements under different temperature and voltage stress conditions to activate the main degradation mechanisms and to calibrate the matrix of equations. For each applied stress, an acceleration factor can be calculated according to the mechanism considered as proportion to the system FIT.

However, since each failure mechanism has a unique failure rate, the matrix resolution follows Drenick's theorem [29] which considers that the combination of numerous degradation mechanisms with different statistical distributions, at the system level, has approximately constant rate. Thus, it is possible to construct a matrix combining the degradation mechanisms by considering that the total failure rate of the circuit is constant. This allows adapting the MTOL method to the algorithm proposed in traditional standards such as the MIL-HDBK-217F.

The construction of the matrix is based on the obtained results with the M-HTOL (Multiple High Temperature Over-stress Life test) accelerating test under different conditions among the four main degradation mechanisms in IC (EM, HCI, TDDB, NBTI). At least, four stress conditions are needed to evaluate the contribution of each degradation mechanism. Each stress will see a strong contribution of one mechanism relative to the others, which describes a well-defined failure point location based on the physics models (e.g. JEDEC).

Table III-4 presents the matrix of degradation mechanisms considered in this approach. Each row describes the stress conditions (V_i, T_i) of the accelerated test i. The result $MTTF_i$ represents the average time when the system will present a failure at a considered percentage of degradation to calibrate the system. The result is given in terms of failure rate λ and measured as FIT calculated as $\frac{10^9}{MTTF}$. For each stress conditions (V_i, T_i), a relative acceleration rate (a parameter proportional to acceleration factor) is reported in the different rows. The method assumes that each acceleration factor (A_i, B_i, C_i, D_i) affects linearly the performance of the system. The matrix solution leads to a linear system of equations as presented in Table III-5 which leads to the Equation III-25, its resolution allows finding the set of constants P_i, which characterized the impact of one degradation mechanism to the overall reliability of the circuit. The goal of solving the reliability matrix is the reliability prediction for any other operating conditions (e.g. nominal operating conditions) that were not tested using the extrapolation of the constructed reliability model. The acceleration factor formulas for each degradation mechanism are detailed in Table III-6.

	TDDB	HCI	NBTI	EM	Results
V_1,T_1	$W.A_1$	$X.B_1$	$Y.C_1$	$Z.D_1$	$\frac{1}{MTTF_1}$
V_2,T_2	$W.A_2$	$X.B_2$	$Y.C_2$	$Z.D_2$	$\frac{1}{MTTF_2}$
V_3,T_3	$W.A_3$	$X.B_3$	$Y.C_3$	$Z.D_3$	$\frac{1}{MTTF_3}$
V_4,T_4	$W.A_4$	$X.B_4$	$Y.C_4$	$Z.D_4$	$\frac{1}{MTTF_4}$

Table III-4 MTOL matrix to solve models with measured TTF [28]

$$\overbrace{\begin{bmatrix} A_1 & B_1 & C_1 & D_1 \\ A_2 & B_2 & C_2 & D_2 \\ A_3 & B_3 & C_3 & D_3 \\ A_4 & B_4 & C_4 & D_4 \end{bmatrix}}^{AF} \cdot \overbrace{\begin{bmatrix} W \\ X \\ Y \\ Z \end{bmatrix}}^{P_i} = \overbrace{\begin{bmatrix} \lambda_1 \\ \lambda_2 \\ \lambda_3 \\ \lambda_4 \end{bmatrix}}^{\lambda}$$

Table III-5 Matrix solution [28]

$$(\mathbf{AF}).(\mathbf{P_i}) = (\boldsymbol{\lambda}) \xrightarrow{\textbf{yields}} (\mathbf{P_i}) = (\mathbf{AF})^{-1}.(\boldsymbol{\lambda}) \quad \text{(III-27)}$$

Time dependent dielectric breakdown	$(A_i) = AF_{TDDB} = e^{-\beta(V_0-V)}.e^{\frac{E_a}{K}\left(\frac{1}{T_0}-\frac{1}{T}\right)}$
Hot Carrier Injection	$(B_i) = AF_{HCI} = \frac{f}{f_0}.\left(\frac{V}{V_0}\right)^N.e^{\frac{E_a}{K}\left(\frac{1}{T_0}-\frac{1}{T}\right)}$
Negative bias temperature instability	$(C_i) = AF_{NBTI} = \left(\frac{V}{V_0}\right)^{\frac{\alpha}{n}}.e^{\frac{E_a}{K}\left(\frac{1}{T_0}-\frac{1}{T}\right).\frac{1}{n}}$
Electromigration	$(D_i) = AF_{EM} = \frac{f}{f_0}.\left(\frac{V}{V_0}\right)^n.e^{\frac{E_a}{K}\left(\frac{1}{T_0}-\frac{1}{T}\right)}$

Table III-6 Equations for the acceleration factors matrix [28]

3.2.2 Application of matrix solution approach

The MTOL approach was applied for a set of experiences on a 28 nm integrated circuit [28]. The purpose was to determine the MTTF in nominal operating conditions set to (0.9 V, 30 °C). The test consists in applying several stresses under different conditions on a ring oscillator and calculating the failure rates λ_i for the $MTTF_i$ relative to a decrease of 10% of the output frequency. The results of the accelerated tests for 5 different conditions are shown in Figure III-7. The MTTF of the 10% degradation is obtained in the various cases by extrapolation.

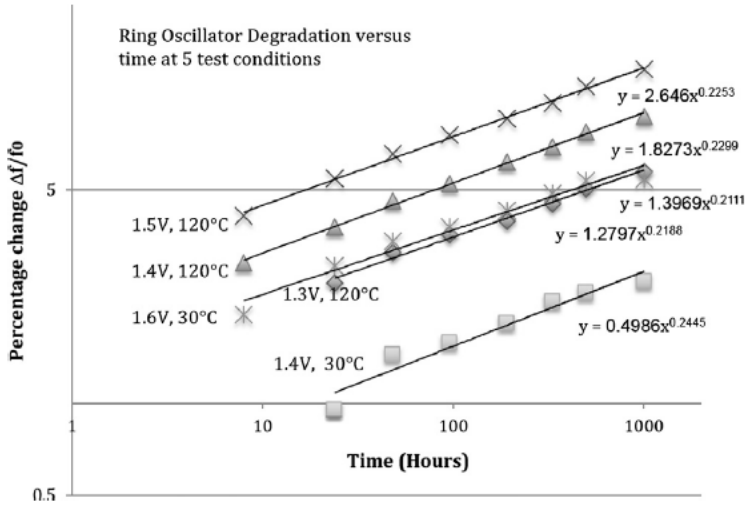

Figure III-7 Accelerating test results at different stress conditions [28]

The reliability matrix presented in Table III-4 is constructed according the calculated acceleration factor relative to the unity conditions for (0.9 V, 30 °C), which are the minimum operating conditions. The unity condition is necessary because it allows calculating the constants P_i according to a meaningful proportionality, which can be explained by the simple proportionality of the acceleration factor at arbitrary conditions.

The reliability matrix proposed by the MTOL approach presented in the previous section by Table III-4 is completed using the presented experimental results. The calculation of the acceleration factors for each degradation mechanism at the different conditions leads to the resolution of the matrix. Hence, the contribution of each mechanism to the total FIT is determined as a proportionality factor, as described Table III-7. However, a most accurate contribution of each mechanism is represented by the matrix given in Table III-8 where the last 4 rows are extrapolated results for untested conditions. This experimental study shows that Electromigration is the dominant mechanism at the stress conditions (0.9 V, 70 °C) and it is combined to the TDDB at higher stress conditions, although the proportionality factor of the TDDB presented in Table III-7 shows a little influence of TDDB to the total FIT. The proportionality factors are calculated for each degradation mechanism for the solved value of P_i in Equation III-25 according to P_{total} $\left(\frac{P_i}{P_{total}}\right)$. Overall, electromigration is the dominant mechanism for any test conditions, since it is the least accelerated mechanism by the HTOL test [28].

TDDB	HCI	NBTI	EM
0.00014%	0.52%	49.88%	49.62%

Table III-7 Proportionality factor of degradation mechanisms

	TDDB	HCI	NBTI	EM	Final FIT
1.6V,30°C	176329184	1667671	6762741	6	200624
1.5V,120°C	14658341454	275664	279314765	523745	4637933
1.3V,120°C	200284634	7532	5115828	523745	82997
1.4V,120°C	1850069880	45567	37801143	523745	615185
1.4V,30°C	3210449	45567	123864	6	4718
0.9V,30°C	1	1	1	1	0.1
0.9V,70°C	71	6	55	547	9.6
0.9V,85°C	185	6	141	3041	50.3
1.0V,105°C	15602	34	3034	29981	511.3
0.9V,105°C	661	6	411	29981	484.7

Table III-8 Matrix solution using experimental results and extrapolation to untested conditions (last 4 rows)

The extrapolated results from the reliability matrix resolution have been plotted for different voltages and involve the different degradation mechanisms according to the temperature as described by Figure III-8.

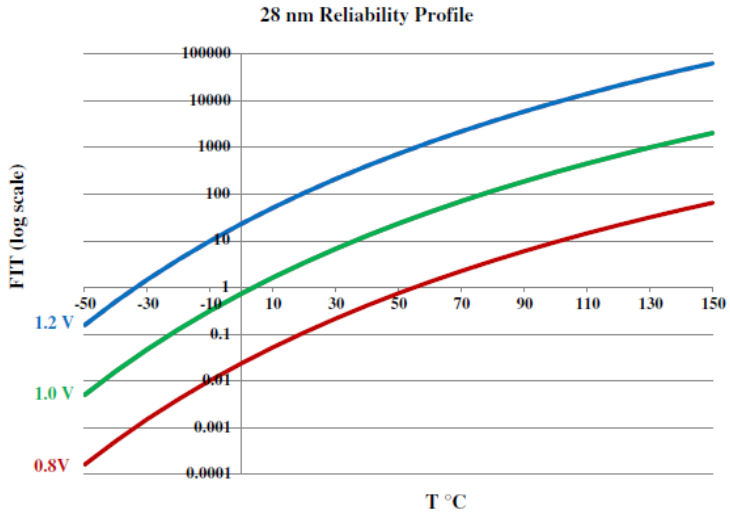

Figure III-8 Reliability curve for different voltages for 28 nm technology [11]

To sum up, MTOL approach is the first method that allows using existing physical models for reliability prediction to determine the multiple mechanisms activated on a chip for any condition of use and for a specific degradation criterion, which represents the key novelty of this approach. However the calculated constant P_i of the reliability matrix of MTOL model are dependent of the IC technology, hence, the study of an IC with a different technology process must be studied following the M-HTOL testing methods in order to segregate the different degradation mechanisms for the construction of the MTOL model. It should be noted that MTOL refers to the reliability prediction model based on matrix solution and M-HTOL refers to the test approach based on the application of multiple stresses conditions.

3.3. Presentation of MSTORM tool

3.3.1 General presentation of MSTORM tool

New investigations studied the MTOL model and proposed a recombination with the multidimensional Boltzmann model Arrhenius Zhurkov (BAZ). This study involved the creation of a new MSTORM (Multi-phySics mulTi-stressOrs predictive Reliability Model) tool to simplify the use of the new combined model (MTOL/BAZ) [26].

The basis of this approach comes from the TST (Transition State Theory) and the health of a population of components that grows over time and changes following the applied stress. As seen in the section 2.3.6, the concept of TST is that an identical and homogeneous lot of components degrade after an observation time due to aging or storage. Thus, because of the aging, the transformation is translated by the transition from a certain energy level to another. The BAZ model is based on a fundamental assumption cited by A. Bensoussan in [26] as: "*For a biasing set higher and close to the breakdown limit, the two failure mechanisms (E.G. the diffusion and the instantaneous catastrophic ones) are in competition and occurred simultaneously; for sake of simplicity it is assumed they are progressively and linearly combined from a pure diffusion mechanism at nominal biasing to a pure burnout at high bias (voltage or current of power dissipation)*".

According to the Boltzmann-Arrhenius-Zhurkov (BAZ) model which is in fact similar to COX model, we find λ for a material or a device experiencing the combined action of an elevated temperature and external stress S as given by:

$$\lambda = \lambda_0 \cdot \exp\left[-\frac{(E_a - \gamma \cdot S)}{k \cdot T}\right] = \lambda_0 \cdot \exp\left[-\frac{E_{a,eff}}{k \cdot T}\right] \quad \text{(III-28)}$$

Consequently, the derivatives determines the effective activation energy $E_{a,eff}$ and the γ factor as follows [31]:

$$E_{a,eff} = k \cdot \left[\frac{\partial(\ln(\lambda))}{\partial\left(\frac{1}{T}\right)}\right]_S = \left[\frac{1}{FIT_M} \cdot \frac{\partial FIT_M}{\partial\left(\frac{1}{k \cdot T}\right)}\right]_S \quad \text{(III-29)}$$

$$\gamma = -\left[\frac{\partial \lambda}{\partial S}\right]_T = \left[\frac{k \cdot T}{FIT_M} \cdot \frac{\partial FIT_M}{\partial S}\right]_T \quad \text{(III-30)}$$

The expression III-25 proposed in this study has been established assuming that the stressors are independent of the temperature effect. The proposed method of reliability is agile and consists in defining the physical limits of an electronic component through burnout or breakdown tests in order to normalize the new stress parameters. The activation energy approximation method is integrated in the MTOL model and allows the construction of a predictive reliability model through the MSTORM tool.

For the case study of a FPGA 28 nm process presented previously, the calculated effective activation energy is presented in Figure III-9 in 3D and 2D plots. These figures show the non-linearity of the activation energy when considering BAZ model. For each degradation criterion, the activation energy reaches a stabilization state when the degradation mechanism (EM, BTI or HCI) is activated. These values of activation energy are integrated in MSTORM model for the FPGA 28 nm process and should be reconstructed for any other technology.

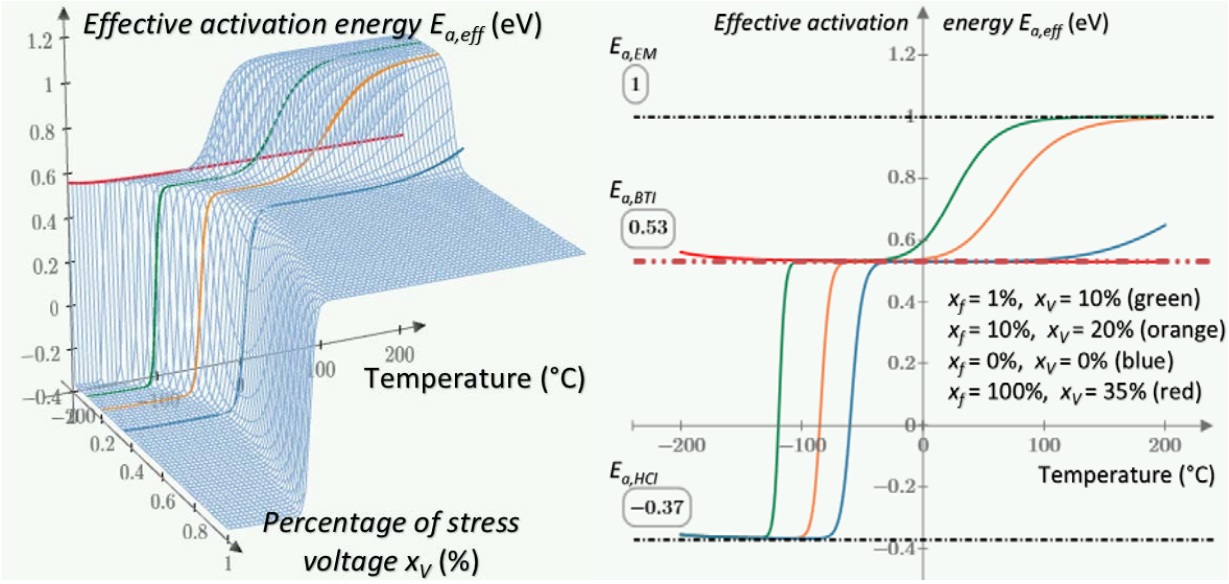

Figure III-9 Effective activation energy of 28 nm technology using M-STORM model (left) 3D plot for $E_{a,eff}$ (x_f = 10%, x_V, T), or (right) 2D plot for same various percentage of stress conditions (x_f=F/F_{max} and x_V=V/V_{br}) and temperature (F_{max} = 12 GHz, V_{br} = 3.3V).

3.3.2 Case study: FPGA 45 nm

The new reliability prediction methodology was studied on DSM commercial components: FPGAs designed in 28 nm and 45 nm technologies. Some results of the MTOL model on the 28 nm FPGA were briefly presented in 3.2.2.

In this section, the 45 nm FPGA reliability model will be detailed because it corresponds to the same IC family studied in our research work. We can assume that for the same CMOS technology embedded in two different components, the degradation mechanisms activated by a multi-stress of voltage and temperature will be similar. Considering this assumption, the results of the applied stress to the FPGA studied in our project will be compared with the results that will be presented in this section.

The tested FPGA is a Xilinx XC6SLX9 Spartan 6 (45 nm) built on a Mojo board. The test set-up consists in the stressed component (FPGA) that will be implemented with different Ring Oscillators (RO) running with several frequencies from 700 MHz down to 200 KHz, this allows seeing the frequency dependence to the failure mechanisms. The measurement system is composed of a 32-bit binary counter referenced to an on board clock signal of 9 Hz. The board is controlled with a communication interface using a computer as presented in Figure III-10.

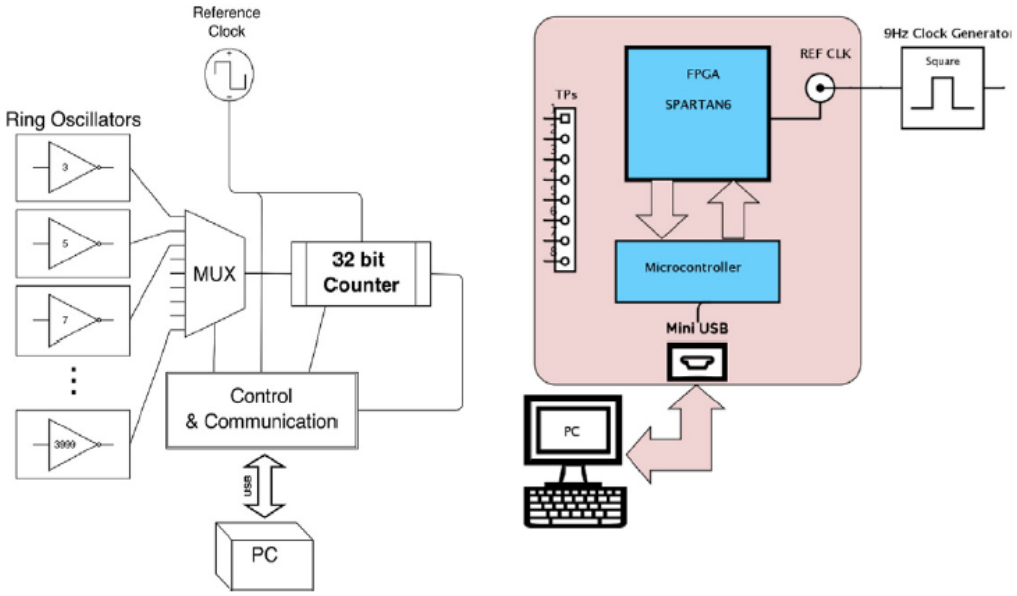

Figure III-10 Test set-up and the control and communication interface for accelerated tests [11]

According to the M-HTOL test methodology, temperature and voltage stress conditions are defined to accelerate the different degradation mechanisms separately. Only the HCI, BTI and EM mechanisms will be considered because the TDDB showed no contribution during these experiments. This can be explained by the fact that the TDDB mechanism is activated for voltages higher than 1.6 V, knowing that the nominal operating voltage of the FPGA is 1.2V. The acceleration tests are performed for temperatures from -50 to 150 °C.

The first part of this study consists of determining the activation energy E_a and the coefficient γ for each degradation mechanism. For this purpose the degradation criterion is defined as 10% variation of the ROs frequencies relative to the initial frequencies. The degradation criterion was randomly fixed, since the MTOL model construction is independent of this criterion. Only the parameters of acceleration factor and failure rate will change experimentally.

According to the FIT calculation for each degradation mechanism E_a and γ can be deduced using an interpolation with a linear function as seen in Figure III-11. These parameters are extracted for each degradation mechanism and are summarized in Table III-9.

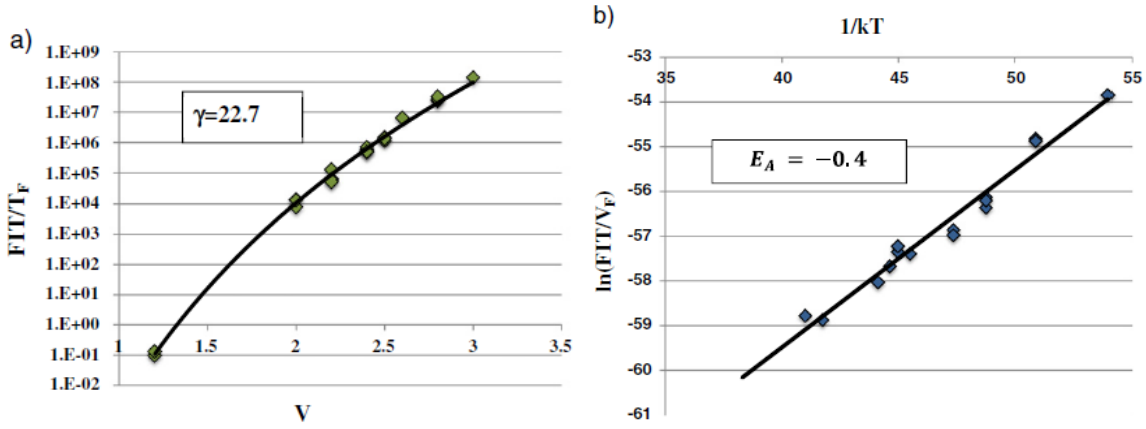

Figure III-11 Plotted results of γ (a) and E_a (b) for HCI mechanism [11]

	E_a (eV)	γ
HCI	-0.4	22.7
BTI	0.52	3.8 V^{-1}
EM	1.24	3.8

Table III-9 Results of E_a and γ for the 45 nm FPGA [11]

These results allow the application of MTOL method described before. Three different test points were considered to solve the reliability matrix for the three considered degradation mechanisms, considering the FIT calculation for each mechanism using the Equations given below.

$$FIT_{HCI} = f.V^{\gamma_{HCI}}.e^{-\frac{E_{a_{HCI}}}{kT}} \quad \text{(III-31)}$$

$$FIT_{BTI} = e^{\gamma_{BTI}V}.e^{-\frac{E_{a_{BTI}}}{kT}} \quad \text{(III-32)}$$

$$FIT_{EM} = f.V^{\gamma_{EM}}.e^{-\frac{E_{a_{EM}}}{kT}} \quad \text{(III-33)}$$

A relative weighting factor was found from the resolution of the reliability matrix, more details are given in [11]. This study allows the construction of a reliability profile extrapolated for untested conditions. The obtained results are presented in Figure III-12 showing the FIT versus the temperature for different voltages and operating frequencies.

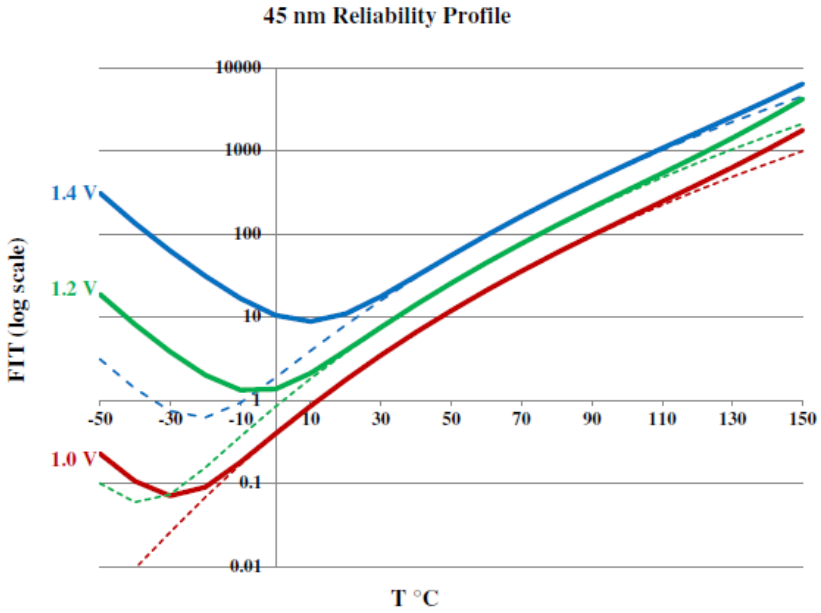

Figure III-12 Reliability curve for different voltages and frequencies from 10 MHz (dashed lines) to 2 GHz (solid lines) [11]

This study has given very practical information about the reliability of a FPGA 45 nm; it will allow the FIT calculation and the reliability prediction during the study that will be presented in the next chapter. Furthermore, since the reliability profile has been constructed from data obtained with measurements, the study held in this thesis could be considered as a case of

validation of the new MTOL model. We point out that we are especially concerned about the reliability prediction in terms of EMC level. Hence, many other degradation criteria must be considered.

4. Conclusion

In this chapter, the modeling for predictive reliability has been presented. From a historical perspective, several guidelines have been proposed in the different industrial applications, they allow the electronic component reliability modeling when activating a specific degradation mechanism. Since the publication of the MIL-HDBK-217 standard by the US defense industry, several other guidelines have been proposed for other industrial applications (FIDES, TELCORDIA ...).

However, these reliability prediction methods suffer from several limitations. Since they are based on the CFR model, they only allow modeling the random failures which appear during the useful life of the component. Moreover, the presented approaches model only one dominant degradation mechanism without taking into account the potential failures due to the activation of other mechanisms simultaneously. A more recent approach has also been introduced, the physics-of-failure approach which also models the electronic components reliability using manufacturing process information and leads to more accurate results for the failure rate prediction. However, it requires several manufacturing and processing data that could be confidential and does not take into account the combination between several degradation mechanisms.

In general, all models rely on accelerated aging tests; the approach for modeling these accelerated tests has been presented with the most commonly used mathematical laws. The added value of BAZ model has been demonstrated. It allows modeling the passage of activation energy from an initial state to another with the stress effect, based on the TST and Eyring model, and taking into account multiple stressors. These acceleration laws and the Physics-of-Failure approach are the basis for the creation of the new MTOL model which, in combination with the BAZ model, has led to the creation of the MSTORM tool for reliability prediction presented in the last section.

MTOL allows modeling the reliability and takes into account the activation of several mechanisms individually using the multi-stress life-test. The construction of MTOL models requires the resolution of a matrix of equations relating the acceleration factors of the different mechanisms to the corresponding failure rates with weighting factors. The resolution of this matrix allows identifying these factors for each mechanism and leads to the reliability extrapolation for untested conditions.

This approach was applied to FPGAs designed in 28 nm and 45 nm processes. The obtained results for the 45 nm FPGA are particularly interesting for our study; the tested component corresponds to the studied FPGA technology and belongs to the same Xilinx FPGA family (Spartan 6). The reliability profile constructed is involving the different degradation mechanisms at different voltages and temperatures. In the next chapter, it will be used to predict the FIT for the stress conditions that will be chosen to study the aging effect on the FPGA EMC and SI performances.

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Chapter IV. Long-term electromagnetic robustness

In the different industrial fields, embedded electronics equipments are increasingly integrating complex systems and components. Thus, EMC levels are a major constraint since all electronic equipments and systems must respect a certain level of EMC compliance. In addition, to reduce the costs, OEMs are obliged to use more and more COTS components that exhibit a strong technological evolution but require several requalification phases. To overcome this problem, as discussed in the previous chapters there are existing models for integrated circuit that allow prediction of EMC levels. As it has been presented, this study is focused on the modeling of conducted emissions of a complex FPGA due to its technological parameters, the number of power and ground pins, and the number of configurable logic blocks (CLBs). Hence, the ICEM-CE model of the FPGA was constructed with a proposal for a new methodology to build the IAs blocks. In addition, the effect of the signal integrity of the FPGA on the conducted emission has been presented.

However, since for industrial applications, integrated circuits are subject to harsh operating conditions (voltage, temperature, humidity, vibration...), the intrinsic degradation mechanisms of the components are liable to be triggered and accelerate aging of the circuit. Therefore, in order to study the impact of aging on the conducted emission level of the FPGA and integrate it into the ICEM-CE model, the MSTORM reliability model will be used to predict the failure expressed in FTT of a certain degradation criterion and at specific operating conditions. However, in order to validate the data established in the MSTORM model for a 45 nm FPGA, accelerated aging tests were carried out to calculate the reliability parameters according to the log-normal and Weibull's distribution laws. Finally, the time required for drift to occur can be predicted using the MSTORM model and the degradation criterion is integrated into the FPGA ICEM-CE model to simulate the evolution of conducted emission levels after aging.

The study of electromagnetic robustness of the FPGA is organized as follow; the first section is dedicated to a general presentation of the accelerated aging tests in order to introduce the M-HTOL testing method. The methodology carried out during this study for accelerated tests is presented in the second section and is followed by the experimental results for the observed degradation of signal integrity and CE level in the third section. Using the measured parameters after the aging of the FPGA, the reliability models are constructed following the log-normal and Weibull's distribution in the fourth section. Finally, the CE level after aging will be simulated using the ICEM-CE and the degradation data of MSTORM model.

1. General overview on reliability accelerated testing

The construction of the reliability MTOL (Multiple Temperature Operational Life) matrix based model presented in the previous chapter requires a set of experiences based on accelerated multiple tests to obtain, in a reduced time, the laws governing the components degradation according to their use. Despite the fact that the combination of Reliability and EMC domains is not widely explored, some research works have been done and allowed to observe the evolution of the EMC levels as a function of the applied stress. In [63], it was demonstrated that using

HTOL stress, the conducted emission level of a digital circuit with 90 nm process decreased. In addition, [30] shows that the activation of the degradation mechanisms of an integrated circuit with 65 nm process due to the LTOL stress lead to the decrease of its immunity level in high frequencies. The applied procedures for electromagnetic robustness characterization are based on temperature stresses based on HTOL (High Temperature Operating Life test) and LTOL (Low Temperature Operating Life test), which are standard accelerated aging tests that simulate the aging behavior of internal structures of electronic components. The accelerated aging tests are based on the application of the components under test in a climatic chamber with a high temperature for HTOL test (150 °C) and negative temperature for LTOL test (-40 °C) for a certain time duration to activate the intrinsic degradation mechanisms of the component.

However, HTOL testing methods suppose that only one mechanism is dominant and does not consider the possible combination between the different degradation mechanisms. As discussed previously, the new M-HTOL testing method allows separating the different failure mechanisms in such a way that the reliability prediction can be made for any user defined operating conditions [74]. Furthermore, MSTORM (Multi-phySics mulTi-stressOrs predictive Reliability Model) model has been developed as a combination of the multi-physic MTOL and the multi-stress BAZ (Boltzmann Arrhenius Zhurkov) model for considering the non-linearity of the activation energy [26]. MSTORM model is then based on the M-HTOL (Multiple High Temperature Overstress Life test) accelerated tests. On the other hand, the M-HTOL test consists in the application of over-stress conditions (Voltage, Temperature…) in order to accelerate different mechanisms in the same set of accelerated tests. As seen in Figure IV-1, the objective of this chapter is to study the aging of the tested FPGA which has been presented in Chapter II according to the M-HTOL testing method, in order to the calculate the reliability parameters (MTTF, FIT…) for a specific degradation criterion using the log-normal and Weibull's distribution and compare the computed parameters to that provided by MSTORM tool for the reliability model validation. Then, the obtained data will be used to study the long-term electromagnetic robustness of the FPGA.

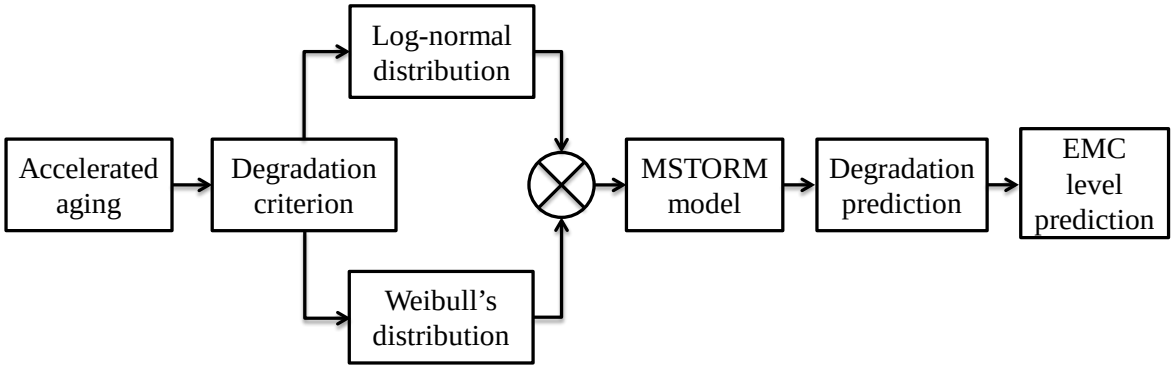

Figure IV-1 Workflow of EMC level prediction using the MSTORM reliability model

In this study, the parameters that will be used to accelerate the aging of the FPGA are voltage and temperature. Before the temperature overstress application, a preliminary study is necessary to fix the DC voltage limits. Hence, the main steps for reliability accelerated tests are:

- **Step-stress**: It consists on the application of different incremental stresses (e.g. voltage) at pre-specified times as presented in Figure IV-2, or after pre-specified number of failures. The objective of this test is to define the voltage level from which the FPGA starts degrading and to define the degradation limits rapidly. It can further reduce test time and the variability of failures times. In this type of test, it is essential to carry out design of experiment study which allows choosing the number of samples, the test conditions, the number of steps and their duration, and the tools for analyzing the test results [76].
- **Life test**: The multiple accelerated life test has been presented and consist on a multi-stress parameters application (voltage and temperature) for different operating stress conditions. Recovery measurements have to be performed for each stress in order to follow up the degradation criterion of the specified parameters.

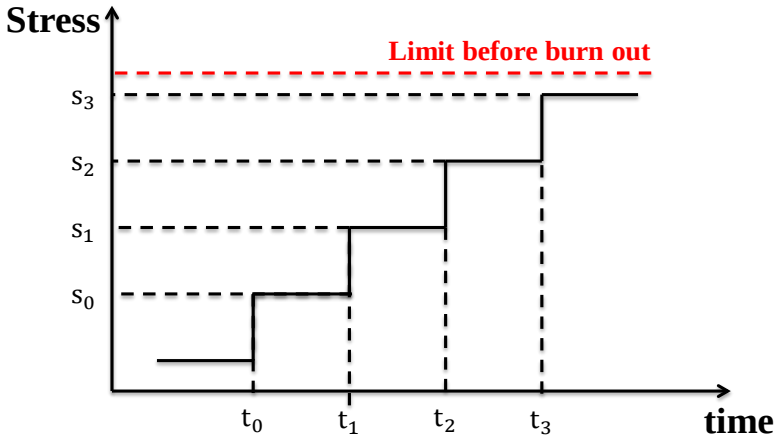

Figure IV-2 Step stress test purpose

2. Methodology of accelerated life testing

In order to construct a reliability model for the studied Spartan 6 FPGA, the application of the electrical step stress will allow setting the voltage limits to be applied and which will lead to the appearance of degradations according to the specified criterion. Then, in the life test stage, the effect of temperature will be combined with electrical stress in order to accelerate the aging of the component and different stress operating conditions will be applied to separate the different degradation mechanisms. In this section, the methodology followed in the study of the step stress and the life test is detailed.

2.1. Step-Stress Accelerated Life Test (SSALT)

The electrical characteristics of the Spartan 6 FPGA are given by the manufacturer. However, DC voltage values are given for absolute maximum ratings as shown in Table IV-1, and the manufacturer noticed that "*Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions are not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability* [78]". This means that the given values will only guarantee the

FPGA good functioning, and setting the maximum values will not systematically lead to the component burn-out or the appearance of any degradation in a reasonable time for an accelerated life test.

Power Domain	MIN.	NOM.	MAX.	NOM/MAX
VCCINT (V)	- 0,5	1,2	1,32	10 %
VCCAUX (V)	- 0,5	3,3	3,75	12 %
VCCO (V)	- 0,5	3,3	3,75	12 %
	_	1,5	1,65	10%
VREF (V)	_	0,75	0,825	10%

Table IV-1 Absolute maximum ratings for the Spartan 6 DC characteristics [78]

Since the manufacturer does not give exactly the voltage values that lead to the components burn-out, the DC voltage maximum ratings values are not precise enough to determine the voltages to be applied to the FPGA in each step of the step stress. Therefore, over voltage stress tests have been performed on the studied FPGA to determine the voltages burn-out limit. The test consists of applying the nominal voltages on the FPGA, then increasing the voltage on each power domain until obtaining a burn-out. The current consumption is recorded during this experience. The same procedure has been applied to each power domain; therefore, the tests are performed on three different components. The obtained maximum voltages that led to burn-out for each power domain are reported in Table IV-2 and compared to the nominal voltage values and the absolute maximum rating given by the manufacturer.

The Figure IV-3 shows the curves of the different supply voltages as a function of the current consumption measured using a digital precision multimeter. The figure shows that with the increase of the voltage, the current consumption could reach very high values which lead to the component degradation. The maximum voltages which led to the breakdown of the components are 4.7 V for the power domain VCCINT, and 6.7 V for the power domains $VCCO_x$ (where x refers to the bank number). The reference voltage VREF is always set as the half of the power domain VCCO3 value as specified by the manufacturer.

Power Domain	V_{nom}	V_{max_rating}	V_{max}
VCCINT	1,2	1,32	4,7
$VCCO_x$	3,3	5,75	6,7
	1,5	1,65	6,7
VREF	0,75	0,825	3,35

Table IV-2 DC characteristics for the different power domains at nominal, max rating and burn-out conditions

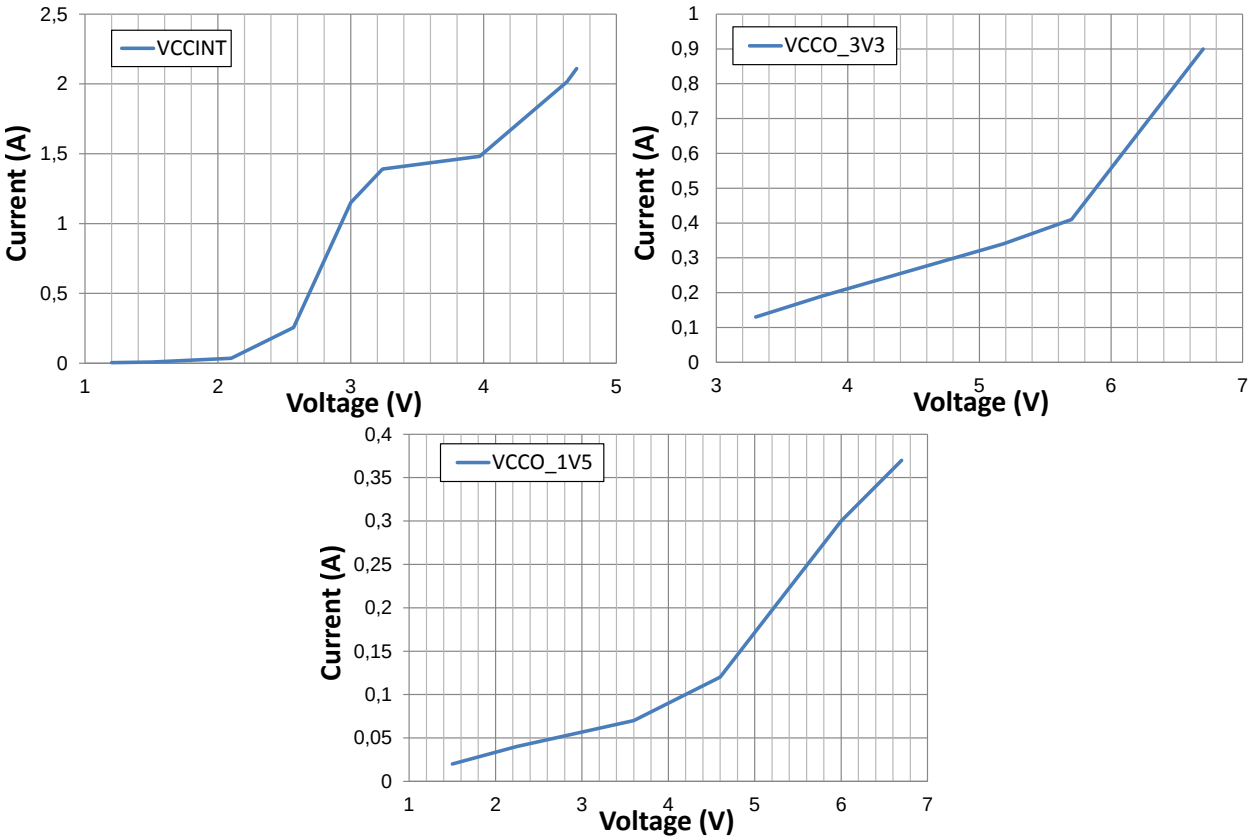

Figure IV-3 Evolution of the current consumption with the increase of the voltage on the different power domains of the FPGA

After the definition of the voltage values for burn-out limit, the step-stress is used to define the voltage values where the component begins to degrade according to a degradation criterion. During this stage it is necessary to control the ambient temperature (for example 20 °C.) that should not change during the step stress experience. The following diagram presented in Figure IV-4 shows the step-stress workflow, which consists in:

- Ambient temperature control during every stage of the step stress.
- Initial measurements for a set of specified configuration to follow up the FPGA degradation.
- The application of an initial over voltage stress V+ΔV to the supply pins of the component (where V is the nominal voltage and ΔV is the incremental stress voltage) for a duration of 168 h. Here, the step stress duration and the incremental stress voltage are fixed to be constant, however, in a step stress test, it is possible to have different stress periods and the stress levels do not have to be uniformly spaced [80].
- Perform the recovery measurement at the end of the step under the FPGA nominal operating conditions.
- If there is no degradation on the tested configuration the over voltage stress ΔV must be incremented.

- When a degradation is seen at the step number N, the voltage limit will be set at the operating conditions of the step N-1. No voltage stress will be applied beyond this limit during the life test. The voltages defined at the N-1 step will be noted V_{STEP}.

The voltage operating conditions applied in the step stress are resumed in Table IV-2, the degradations induced by the different steps will be discussed later. During the step stress, 3 different components will be tested and 2 control samples are kept to check the repeatability of the measurement test bench.

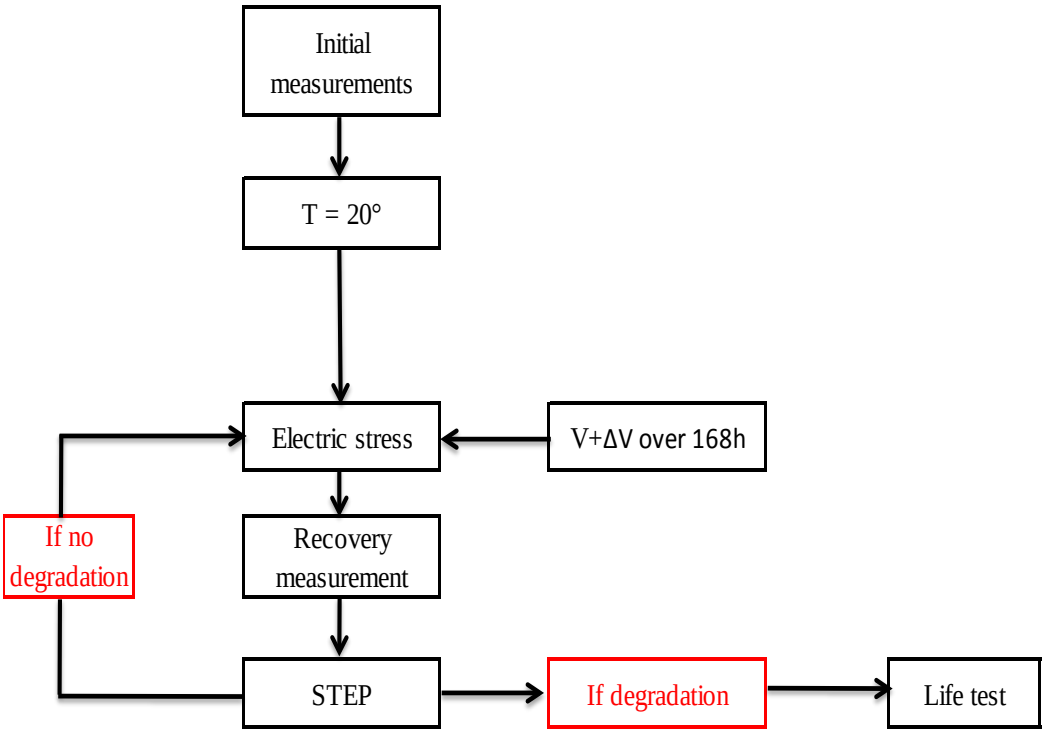

Figure IV-4 Step Stress workflow description

Power domain	V_{nom}	$V+\Delta V_1$	$V+\Delta V_2$	$V+\Delta V_3$	$V+\Delta V_4$	V_{max}
VCCINT	1,2	1,4	1,9	2,4	2,9	4,7
$VCCO_x$	3,3	3,5	4,25	5	5,75	6,7
	1,5	3,5	4,25	5	5,75	6,7
VREF	0,75	1,75	2,125	2,5	2,875	3,35

Table IV-3 Voltage operating conditions defined for the step stress

2.2. Multiple High Temperature Operating Life test (M-HTOL)

The M-HTOL testing method is based on the voltage over-stress combined to the temperature over-stress. For the studied Spartan 6 FPGA, the evolution of the current consumption according to the voltage and the temperature is not known. However, as seen in the Chapter I, the activation of the degradations mechanisms are linked to the device current density. Hence, prior to the life

test, a preliminary study must be performed to understand the link between the three parameters: current, voltage and temperature.

The preliminary test involves the selection of different temperatures, and different core supply voltages (VCCINT) and IO power supplies (VCCO), in order to establish a design of experiment that will define the life test operating conditions (V,T). In this preliminary study, the static and dynamic currents are measured to estimate the junction temperature for each voltage and current consumption and ambient temperature combination. The objective of this study is to be able to choose the couple (V, T) such as the lifetime (TTF: Time To Failure) predicted by the M-STORM model respect a reasonable duration, which were fixed in this study to 1000 h, in order to be able to study different conditions in the allotted time for this work.

Using the step stress and the preliminary test results, the operating conditions of the life test can be defined. The life test workflow is presented in Figure IV-5 and consists on the following operations:

- Initial measurements at ambient temperature.
- Stress application at the defined parameters (V_i,T_i) over a time t_j, where i is the stress number and j is the number of hours under which the components are under the stress. According to the MIL-STD-883H standard [77], the duration t_j varies following the TTF for the specified stress conditions as shown in Table IV-4.
- Recovery measurements in the nominal operating conditions.
- If the components do not show important degradations, a new stress is launched for a new duration t_{j+1}.
- The end of the life test for (V_i,T_i) occurs when the components reach the degradation criterion.

The presented workflow must be performed for multiple operating conditions (V_i,T_i).

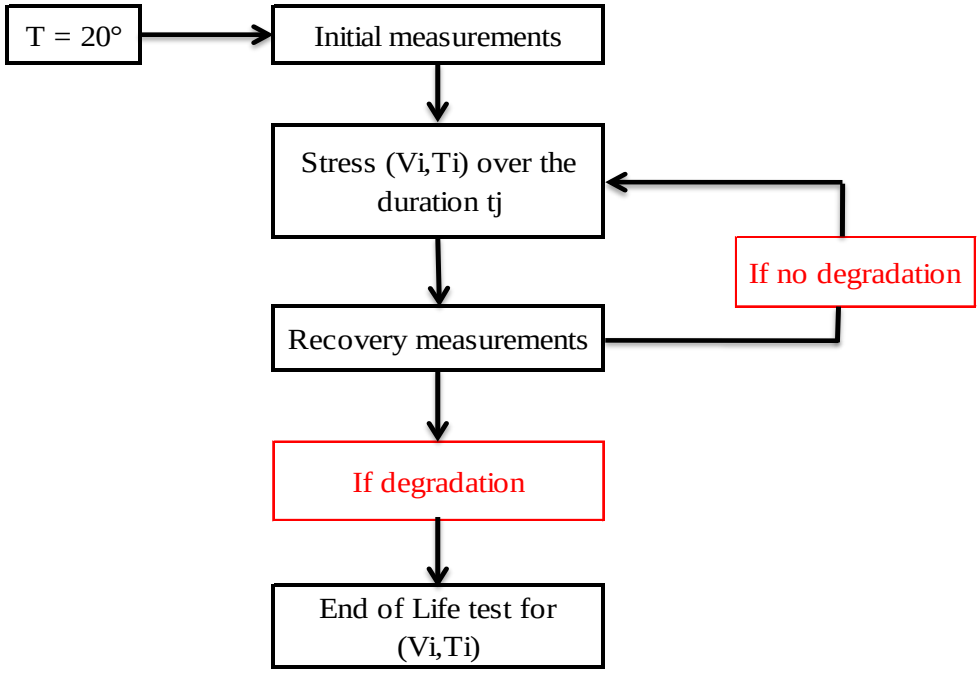

Figure IV-5 Presentation of the workflow of the Life test

TTF < 100h	1h	3h	7h	10h	30h	70h	100h
TTF > 100h	24h	48h	72h	96h	168h	332h	500h

Table IV-4 Life test time durations according to the TTF [26]

2.3. Experimental tests strategy

The experimental study of the aging of FPGA needs to set up an experimental tests strategy, in order to fix the number of samples to be tested, the parameters to be tested (degradation criteria) and the configurations to be implemented. It is necessary to provide a sufficient number of samples to perform a statistical study at the end of the life test. The Table IV-5 resumes the number of tested FPGA. During the preliminary study of step stress 3 FPGAs has been tested with no control sample since the goal was only to define the voltages burn-out limit of the component. In the step stress, 3 FPGAs were set to go through the electric stress with 2 control samples that allow the verification of the repeatability of the different measurements. The preliminary study of life test needs only one FPGA, since the goal is only to record the evolution of the current, voltages and junction temperature parameters. Furthermore, the component does not reach the burn-out limit since it was fixed in the previous test (step stress) and no control sample is needed. Finally, 5 different FPGAs were set for the life test with 1 control sample. Moreover, since the M-HTOL testing method needs a minimum of 3 stress conditions, the number of samples will be 15. This leads to a total of 25 FPGAs for the accelerated aging tests.

Test	Nb. aged samples	Nb. control samples
Preliminary study of Step Stress	3	0
Step Stress	3	2
Preliminary study of Life test	1	0
Life test	5 per (V_i,T_i) stress	1

Table IV-5 Number of tested samples at the different stages of the step stress and the accelerated life test

The tested parameters are chosen such as they contribute in the CE noise level. During the applied tests, several configurations were implemented, as presented in Table IV-6, to follow up the evolution of the following parameters:

- The delay between the different CLBs using a ring oscillator configuration. The ring oscillator design principle is presented in Figure IV-2, which consists in the configuration of (2N+1) inverters in chain. The output frequency is $f_{out} = \frac{1}{2.N.T_p}$ where T_p is the propagation delay per inverter and include the interconnections propagation delays. Hence, 99 inverters are implemented in order to fix the output frequency to around 10 MHz. Furthermore, the same design has been implemented in different areas at the FPGA floorplan level in order to consider each area as a single sample which allows increasing the samples number for the statistical analysis.

- Static and dynamic characteristics of the IOs in order to observe the induced degradation on the pull-up and pull-down devices for the different IO standard (LVCMOS33, SSTL15, DIFF_SSTL15). The test consists in the measurement of the I(V) characteristics of the NMOS and PMOS transistors using a sourcemeter and the V(t) measurement to characterize the time profiles of the signals at the rising and the falling edges. The objective is to evaluate the aging effect on these parameters, hence, on the FPGA signal integrity.
- Conducted emissions measurements are performed using the 1 Ω method for the delay line configuration, in order to study the effect of aging on the CE level. The delay line uses the same structure as seen in Chapter II, with a different number of inverters and number of cascaded delay line blocks. In this case, the configuration is set for 10 inverters per block, and 900 delay lines will be implemented in series to maximize the dynamic power consumption.

For SI measurements, different IO standards will be tested using static and time profile measurements. Different pins have been chosen for IO characterization:

- **LVCMOS33**: T9 pin positioned on the Bank 2 of the FPGA for static measurements and time profile characterization on a 22 pF capacitor.
- **SSTL15**: M1 pin positioned on the Bank 3 of the FPGA for static measurement. This IO standard is used in the digital communication with SDRAM-DDR3 memories.
- **DIFF_SSTL15**: E1 (CLKN), E2 (CLKP) pins positioned on the Bank 3 of the FPGA for time profile characterization on a 50 Ω pull-up or pull-down resistor. The static characteristics are the same as the SSTL15 pins

Configuration	Nb. IO	IO standard	Resources	Frequency	Implementation
Delay line	4	LVCMOS33 SSTL15 DIFF_SSTL15	800 CLBs 4001 LUT	16 MHz	Step stress Life test Recovery
Ring oscillator	1	LVCMOS33	99 LUT	10 MHz	Initial, recovery measurement
Output IO reads the input state	1	LVCMOS33 SSTL15	0	1 MHz	Recovery measurement
	2	DIFF_SSTL15			

Table IV-6 Summary of the tested configurations for the accelerated aging tests

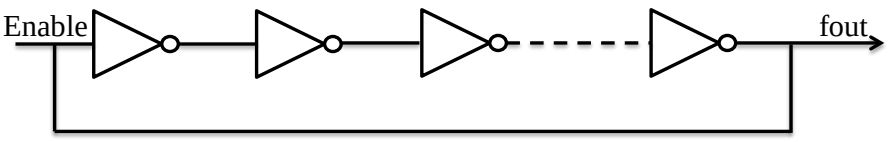

Figure IV-6 Design principle of the ring oscillator configuration

The ELECIS-F test board for CE/RE measurement and SI characterization was not designed for the accelerated aging tests under high temperature. Hence, a PCB was designed for burn-in tests and is presented in Figure IV-7. It is a 6-layers PCB, with 6 FPGAs mounted in a burn-in socket (NP352-256-81) in a daisy chain configuration in order to accelerate the aging of several FPGAs simultaneously.

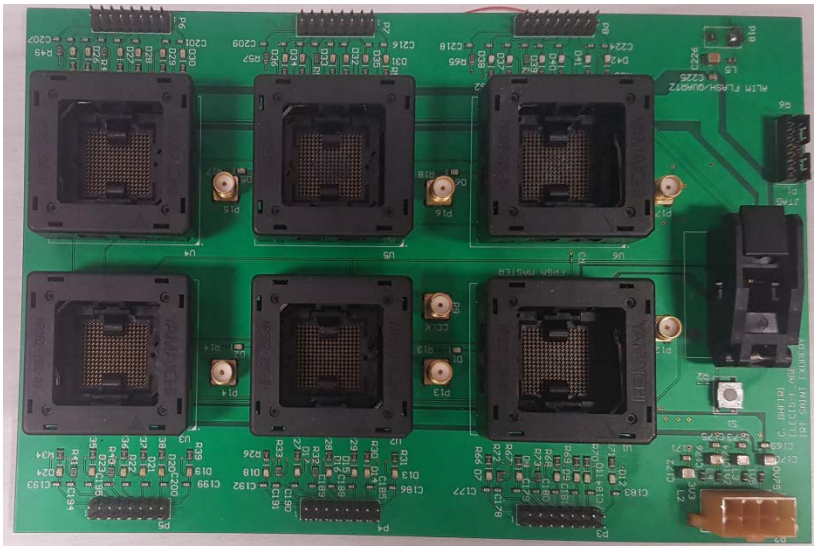

Figure IV-7 Designed PCB for burn-in tests for several FPGAs

3. Experimental results of accelerated life test

In this section, the experimental results of the accelerated tests will be presented, starting with the SSALT results of IOs characteristics and CE level evolution. These results will give valuable information about the electric stress effect on the studied parameters. Moreover, the power supply voltage limits which must not be exceeded during the life test will be defined. The second part of this section concerns the experimental results of aging obtained during the M-HTOL tests. The degraded parameters will be presented for each tested configuration and for the different stress conditions. These results will help calculating the TTF for the different experiences in order to confirm the model given by MSTORM, which will be used later to calculate the TTF for untested conditions and evaluate the evolution of CE using ICEM-CE model of the FPGA.

3.1. Experimental results of SSALT

3.1.1 Experimental results of IO characteristics

3.1.1.1 Static measurements characteristics

During the SSALT tests, the three aged FPGAs are named C1SE, C2SE and C3SE. And the control samples are named C1TEM, C2TEM. All the recovery measurements are performed under nominal operating conditions. Figure IV-8 describes the static measurement protocol of the pull-down (PD) and pull-up (PU) devices. The measurement consists in activating either the pull-up or the pull-down by setting the logic state of the tested output pin and measuring the current

delivered or absorbed by the output buffer. The measurement is performed using a sourcemeter. Two measurement configurations are possible:

- Relative to GND: the sourcemeter is referenced to the ground. The voltage is applied between the tested output pin and the ground.
- Relative to VCC: The sourcemeter is referenced to the IO power supply. The voltage is applied between the tested output pin and its power supply.

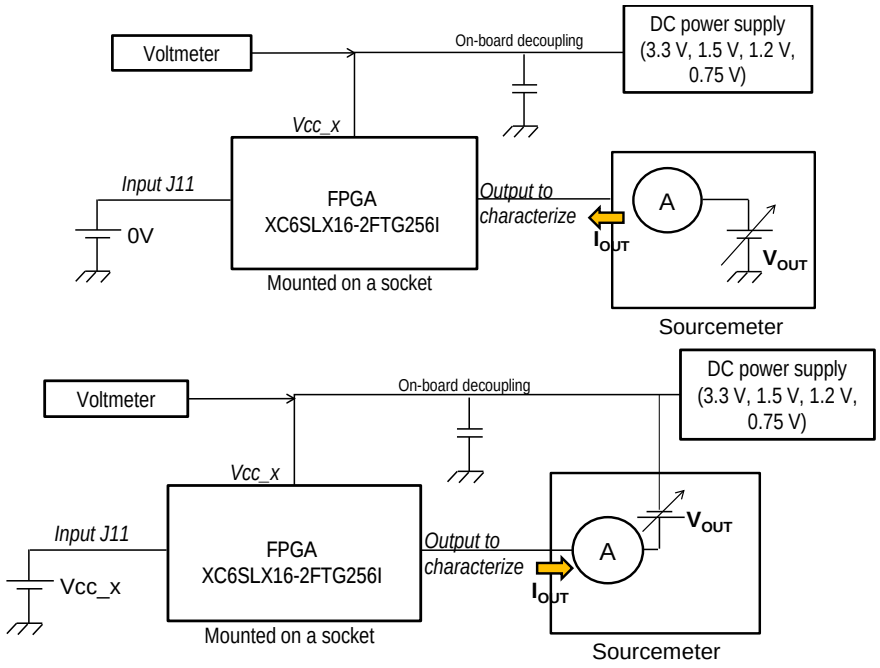

Figure IV-8 Experimental set-up for static measurements

The static measurements for each step at the operating conditions $V+\Delta V_i$ are presented in Figure IV-9 for the LVCMOS33 IO and in Figure IV-10 for the SSTL15 IO for the stressed component C1SE. The figures show that the FPGA starts degrading from the third step $V+\Delta V_3$. The degradation shows up as a decrease of the saturation current of the pull-down devices. No important variation in the pull-up device current has been noted. This means that, with the electrical stresses, only the NMOS transistors degrade due to the HCI mechanism activation, because of the higher mobility of the majority charge carriers. During the operation of NMOS device, the electrons gain enough energy to trigger impact ionization within the substrate. The generated electrons and holes get injected in the gate oxide and create defects in the interface. However, since the PMOS transistors are mainly affected by NBTI mechanism, with the applied step stress, no NBTI effect was observed. This could be due to the rapid recovery of NBTI on PU devices because of the long duration of the test. The HCI mechanism does not appear in PMOS transistors, because the charge carriers (holes) in PMOS have a lower mobility than electrons and are easier to scatter than electrons. Hence, the average energy of the charge carriers in PMOS is low and does not trigger impact ionization [79].

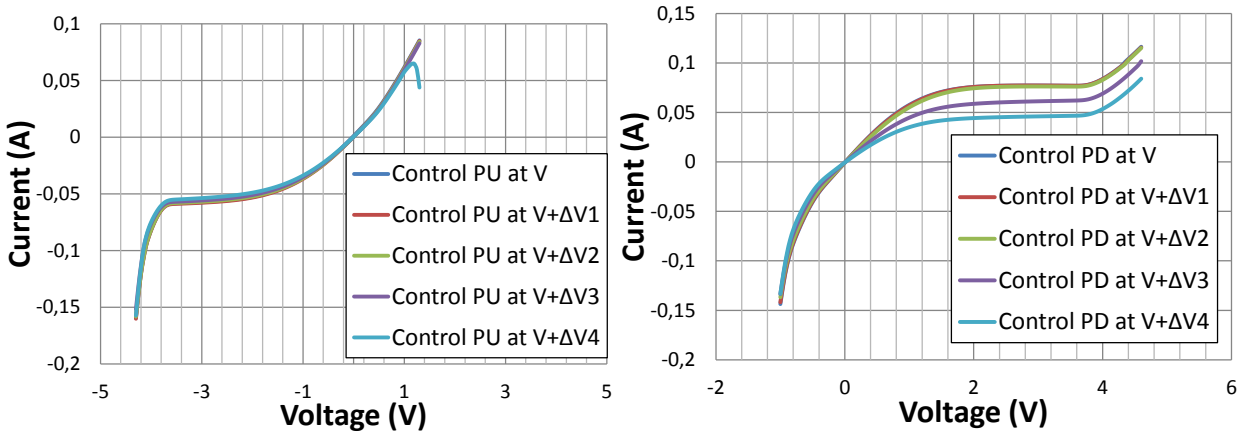

Figure IV-9 Pull-up and pull-down Static measurement on the LVCMOS33 pin of C1SE

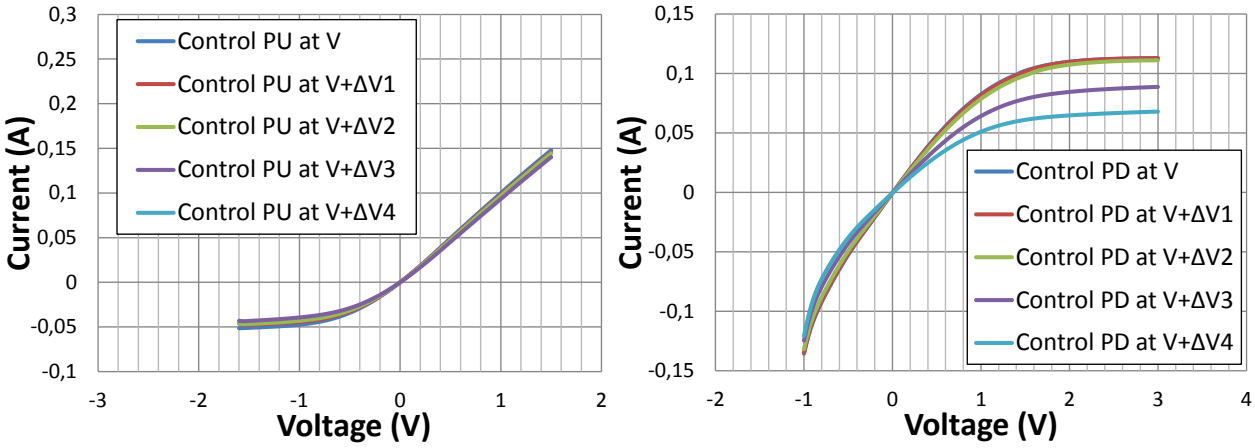

Figure IV-10 Pull-up and pull-down Static measurement on the SSTL15 pin of C1SE

The I(V) characteristics have been compared for the different aged and control samples components. To compare the induced degradation in the different FPGAs the saturation currents variation I_{var} at a specific voltage point V_p (3.3 V for LVCMOS33 IO and 1.5 V for SSTL15 IO) was calculated using the Equation IV-1.

$$I_{var}(\%) = \frac{I_{V+\Delta Vi}(V_p) - I_{initial}(V_p)}{I_{initial}(V_p)} \quad \text{(IV-1)}$$

Figure IV-11 presents the comparison of the current variation at each step for the pull-down devices of the different tested components. The comparison shows that there is no important evolution in the current variation of the pull-down devices of the control samples, which proves the repeatability of the test bench. However, the degradation reaches -20 % on the LVCMOS33 PD devices and -15 % on the SSTL15 PD devices for the electrically stressed components at the third step with the same tendency. But in the last step, the dispersion between the current variations becomes important. No variation is reported in the Figure IV-11 for C2SE component since it was completely burned out and no measurement could be done. Hence, only 4 tests were performed during the step stress (N = 4), and the voltage limits will be fixed at the third step (N-1).

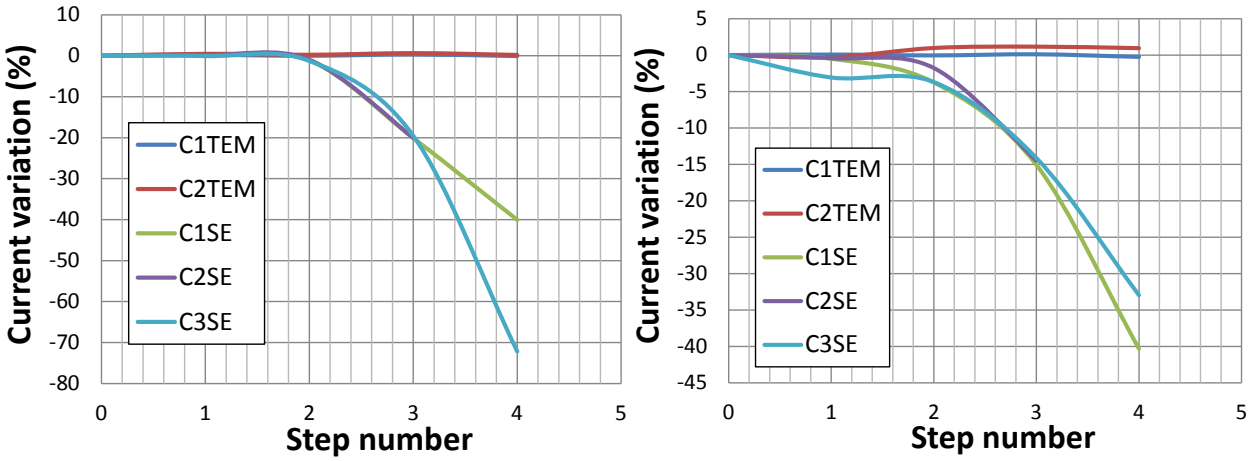

Figure IV-11 Current variation for the pull-down devices of the tested FPGAs for LVCMOS33 (left) and SSTL15 (right) IOs

3.1.1.2 Time profile characteristics

Figure IV-12 describes the experimental set-up for the SI tests on the FPGA IOs. A clock generator transmits a 1 MHz square signal to a GCLK (global clock) input. This signal is read by the tested outputs. A digital oscilloscope (DSO) is used to measure the time profiles with an active probe with load capacitors or resistors connected to the outputs. Only the profiles at the transition edges are recorded. The measurement of the input signal allows synchronizing the DSO acquisition data and to measure the required propagation delays between the input and the output for the rising and falling edges transitions.

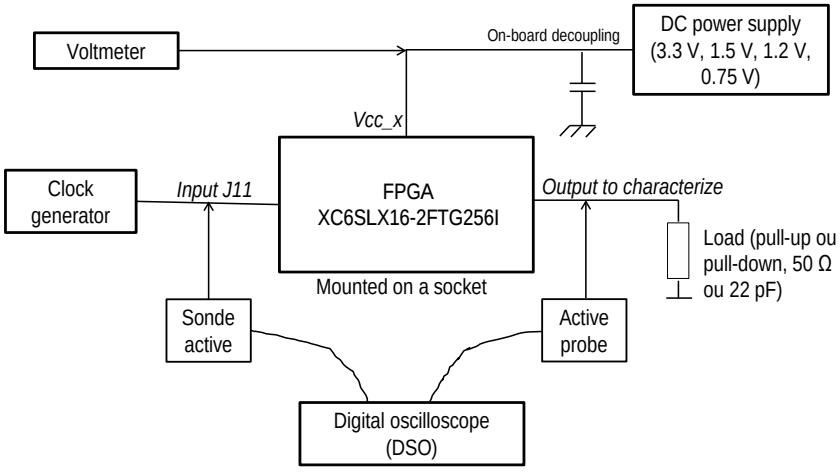

Figure IV-12 Experimental set-up for signal integrity measurements

Figure IV-13 presents the evolution of the rising and falling time delays of the LVCMOS33 output buffer at the different steps for the component C1SE. The figure shows the falling time starts increasing from the third step while the rising time does not vary between the different steps. This results could be predicted from the I(V) characteristics of the output buffers, since only the PD device degrades due to the activation of HCI mechanism. The asymmetric degradation of the PU and PD devices leads to a larger increase of the fall time.

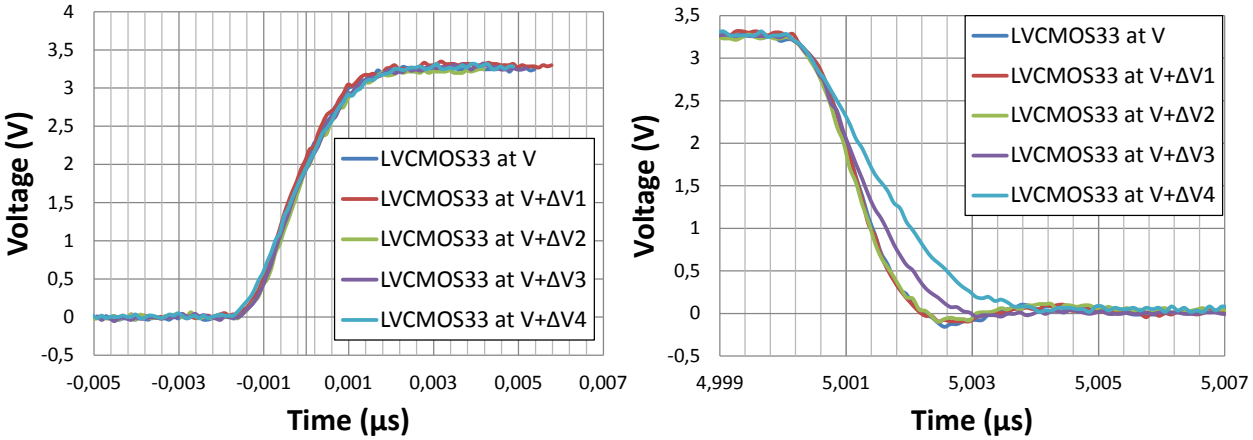

Figure IV-13 Rising and falling edges evolution at the different steps for C1SE LVCMOS33 output

Similarly to the component C1SE, the time profiles of the LVCMOS33 output buffers of the other tested components have been studied. The rising times T_r and falling time T_f are calculated for the tested samples between 10 % and 90 % of the maximum voltage level. The transitions time variation from the initial measurement are calculated at each step and presented in Figure IV-14, where the falling times present an important variation from the third step. This figure confirms once again the results obtained in the static measurements, where the stressed FPGAs PD devices degrade with the same tendency until the third step. Beyond this limit an important dispersion can be observed with the burn-out of C2SE FPGA.

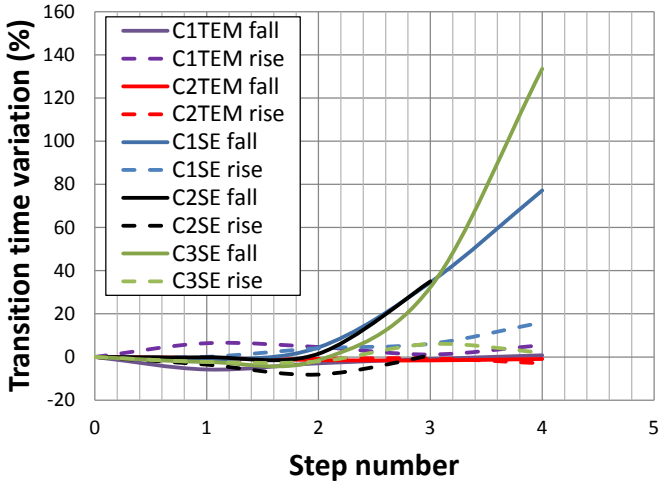

Figure IV-14 Transition time variation during the step stress for the tested components

With the step stress tests, the differential output buffers (DIFF_SSTL15) have presented a significant degradation on the PD and PU devices with an increase on the transition times, contrary to the single ended outputs where only PD devices were degraded. A reduction of the time profile signal amplitude of about 200 mV has been noted, between the initial and the last step measurements. As seen in Figure IV-15, the differential outputs have presented an asymmetric profile from the initial measurements. The output buffer E2 switched faster than E1 output, which is delayed of 300 ps from E2 output. A special care was given to the routing of the differential pins in ELECIS-F board; the traces and loads are placed symmetrically between the

differential output buffers. Furthermore, the measurements are realized using two identical active probes placed on the measurement points symmetrically. The reason of this dissymmetry is unknown and could be an intrinsic default of the FPGA linked to the technology or manufacturing process. However, the application of the electrical stresses has degraded the output buffers and the dissymmetry between the differential outputs increased.

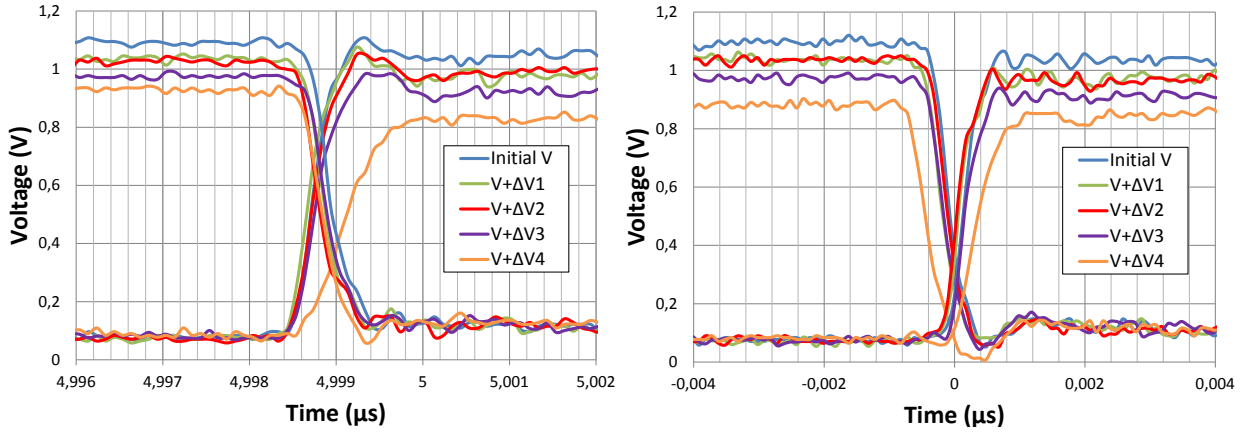

Figure IV-15 Time profile of the differential outputs E1/E2 on the rising edge (left) and falling edge (right) of E2

A differential pair must guarantee a symmetrical time profile signal, in order to reduce de common mode noise. Differential signals inherently create low radiated emissions when they are perfectly balanced (symmetric), because the electric fields created by one half of a signal are suppressed by the fields created by one half of the other signal. However, the degradation of the output buffers leads to an important asymmetric profile between the outputs of the differential pair, which have a major consequence on the electromagnetic emission of the FPGA. It will create the circulation of a common mode current on the traces, contributing strongly to the radiated emission of this differential pair. For the different measurements, the common and differential modes are calculated using the Equations IV-2 and IV-3. The results of the common and differential mode calculation on the rising and falling edges of E2 are presented in Figure IV-16 and Figure IV-17. The differential mode voltage switches between ± 500 mV at the initial measurements and the amplitude decreases to 700 mV. The fall time at initial measurement is 606.3 ps and increases to 1.09 ns at the final step. Furthermore, the rise time at the initial measurement was 550 ps and increases to 644.5 ps. However, the common mode varies at every transition and the amplitude of the variation increases from 300 mV to 400 mV from the initial measurement to the last step stress, this will be at the origin of a RF common mode current generation which increases the radiated emissions.

$$V_{CM} = \frac{V_{E2}+V_{E1}}{2} \quad \text{(IV-2)}$$

$$V_{DM} = \frac{V_{E2}-V_{E1}}{2} \quad \text{(IV-3)}$$

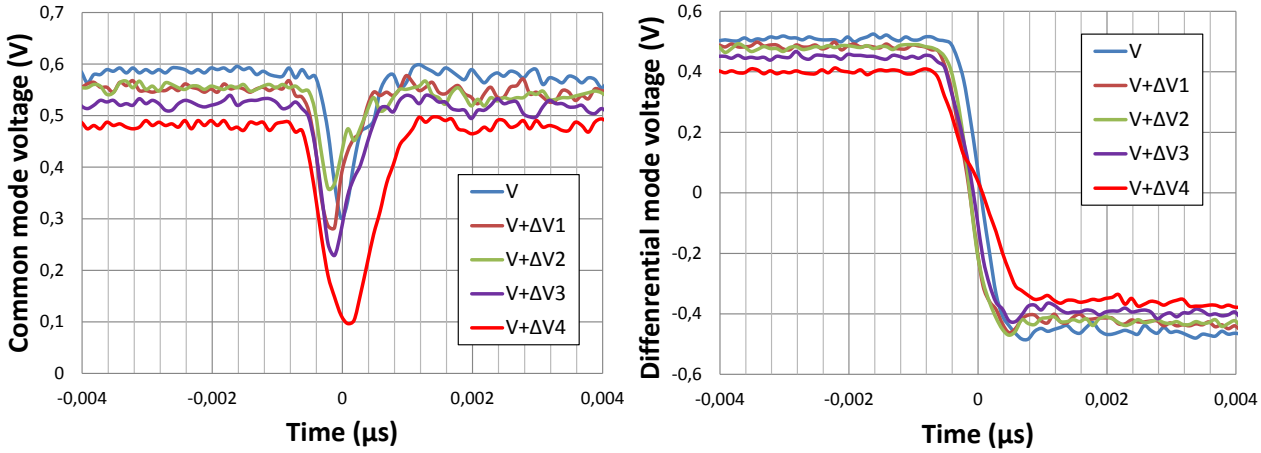

Figure IV-16 Common mode (left) and differential mode (right) voltages on the falling edge of E2 for the component C1SE

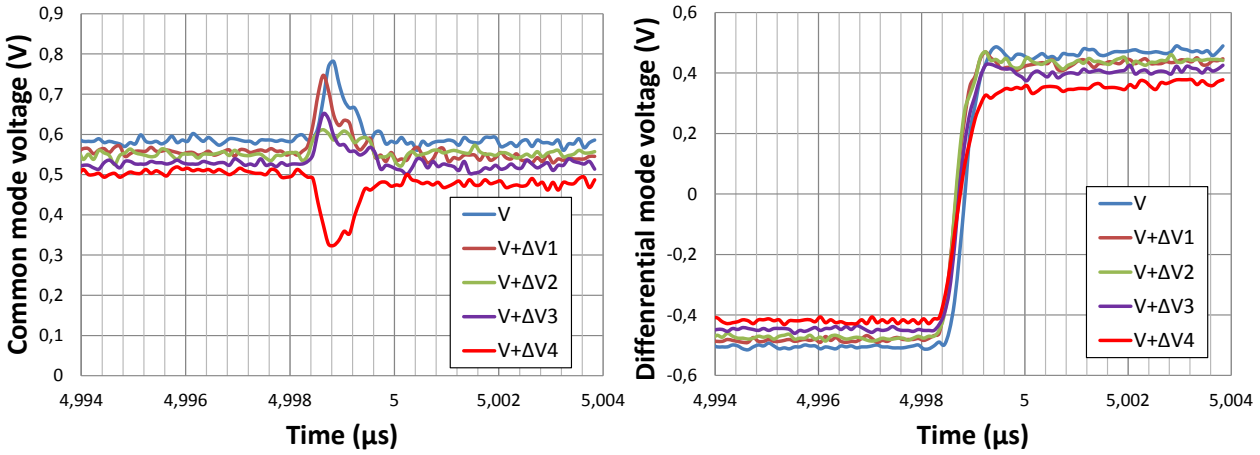

Figure IV-17 Common mode (left) and differential mode (right) voltages on the rising edge of E2 for the component C1SE

3.1.2 Experimental results of CE measurement

Conducted emission measurements have been performed at each stage of the step stress to follow up the evolution of CE level after electrical stresses. The delay line configuration presented in the Chapter II is used with the possibility of activation and deactivation of one output. Figure IV-18 presents a comparison of CE levels for the different steps, it shows no major variation. A very slight decrease of 2 dB is noted between the initial and the last step measurements. Although the electrical stresses have been performed at relatively high voltage values, the stress duration may not be sufficient to degrade the internal structures of the FPGAs. The ring oscillator configuration was planned to evaluate the core degradation, but during the electrical stresses the HCI mechanism has increased the threshold voltage of the internal transistors and the output frequency could not be measured at nominal operating conditions. A solution was found at the end of the step stress, it consists in increasing the core power supply until the stabilization of the ring oscillator output frequency, and going back to the nominal operating conditions allows the measurement of the output frequency. The aging effect on the internal signals propagation delays will be studied during the life test.

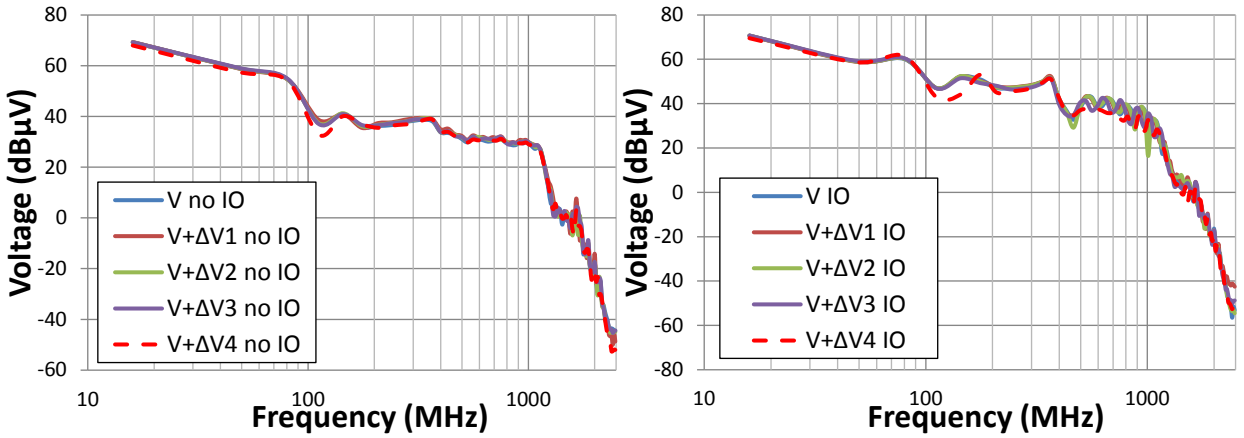

Figure IV-18 CE measurements using the 1 Ω probe on C1SE for the delay line configuration with no activated IO (left), with one activated IO (right)

3.1.3 SSALT results summary

The step stress allowed studying the effect of the electrical stress on the signal integrity and EMC performance of the FPGA. The main observed degradation concerns the output buffers characteristics, which consist in the degradation of the PD devices for the single ended pins with a decrease of the saturation current in the I(V) characteristics and a considerable increase in the fall time transitions due to the activation of the HCI mechanism in NMOS transistors. The differential pins presented a degradation in both PU and PD devices which has an impact on the common mode voltage which increases the radiated emission of the differential bus. Finally, the conducted emission measurement has not shown any notable evolution between the different steps, and may be related to the short time stress duration. Overall, for the different parameters the tested FPGAs has presented the same degradation tendency until the third step. The fourth step presented an important dispersion on the degraded parameters and the burn-out of the C2SE FPGA. Hence, the M-HTOL tests can be performed at the fixed voltages limits defined by the third step.

3.2. Experimental results of M-HTOL

3.2.1 Experimental results of preliminary tests

The M-HTOL test method consists in applying multiple voltage and temperature overstress. However, one of the parameter that influences the performance of the FPGA is the junction temperature, which is linked to the ambient temperature and the power supply voltages. The objective of this test is to be able to predict the junction temperature for the selected overstress conditions in order to activate the degradation mechanisms in acceptable stress duration and preventing the burn-out in a short stress period. Xilinx tool (XPA) is capable of calculating the junction temperature for different ambient temperatures, but the tool is limited to nominal biasing conditions and does not allow the variation of the power supply voltages beyond the manufacturer maximum rating limits.

Hence, prior to the M-HTOL, a preliminary test has been performed to study the evolution of the junction temperature according the operating conditions. Since the current consumption depends

in the power supply voltage, the parameters that will be varied are the ambient temperature T_a, the core and IOs power supply VCCINT and VCCO respectively. The junction temperature T_j is calculated using the Equation IV-4. In this work, it was not possible to access to substrate of the FPGA to measure directly the junction temperature and to extract the exact value of the thermal resistance R_{th}. Thus, its value is considered as given by the manufacturer Xilinx for the Spartan 6 family: R_{th} = 30.2 °C/W which is certainly a rough estimation but sufficient to estimate acceptable stress temperature. The current consumptions ICCINT (Core consumption) and ICCO (IO consumption) are measured using a precision multimeter.

$$T_j = T_a + R_{th}.(VCCINT.ICCINT + VCCO.ICCO) \quad \text{(IV-4)}$$

Since the preliminary study consists in varying three parameters (T_a, VCCINT, VCCO), a design of experiment has been constructed to limit the number of tests. As presented in Table IV-7, the chosen temperatures are 20° (ambient), 40 °C, 80 °C and 120 °C. All tests are carried out inside a thermal chamber which guarantees a minimum variation of ± 2 °C. The selected VCCINT voltages are 1 V, 2 V and 3 V. All IO banks are supplied with the following VCCO voltages: 3 V, 4.25 V and 5.5 V with a reference voltage VREF = VCCO/2. The design of experiment allows testing all the possible combination between the selected values of (T_a, VCCINT, VCCO).

T0 = amb		
T1 = 40 °C	VCCINT0 = 1V (34,5% Vstep)	VCCO0 = 3V (52,2% Vstep)
T2 = 80 °C	VCCINT1 = 3V (100% Vstep)	VCCO1 = 5,5V (96% Vstep)
T3 = 120 °C	VCCINT2 = 2V (69% Vstep)	VCCO2 = 4,25V (74% Vstep)

Table IV-7 Selected operating conditions for the preliminary test to M-HTOL

The obtained results are detailed on the table presented in the Appendix 3. These results are plotted in Figure IV-19, and show the evolution of T_j according the power supplies VCCINT and VCCO. As seen in this figure, the junction temperature is mainly influenced by the electric parameters of the core. The increase of VCCINT for a given ambient temperature leads to the increase of the current consumption ICCINT, hence, the junction temperature increases as well. This seems obvious in the Equation IV-4, but the tests show that this is the main contribution in the junction temperature calculation. The Figure IV-20 resumes the obtained results for every ambient temperature and every VCCINT, VCCO operating conditions. It shows an important increase in the junction temperature starting from VCCINT = 2 V at every T_a.

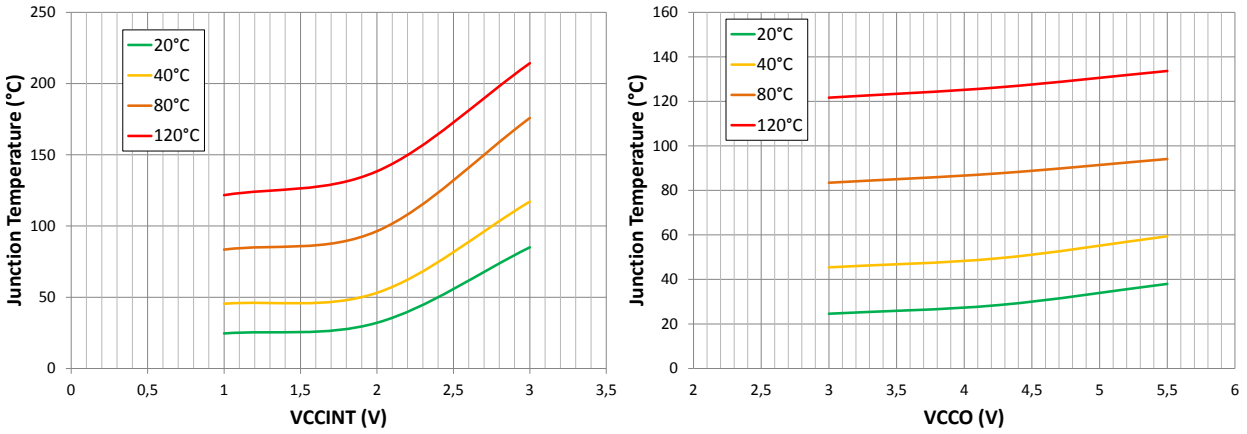

Figure IV-19 Evolution of the junction temperature according the power supply voltage VCCINT (left) and VCCO (right) for different ambient temperatures

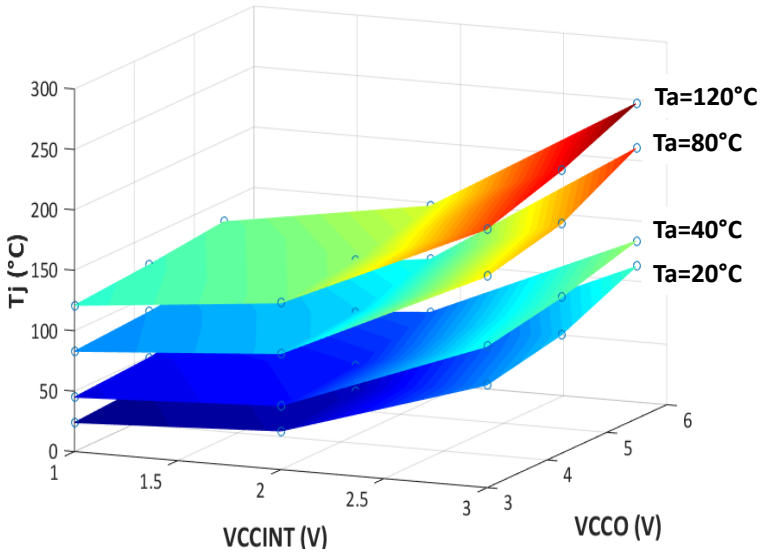

Figure IV-20 Evolution of the junction temperature according VCCINT,VCCO

However, the evolution of T_j is known only for the tested conditions. Then, to be able to predict the junction temperature for untested conditions, a polynomial interpolation has been performed considering two variables (x,y) = (VCCINT,VCCO) and two polynomial function $P_1(x,y)$ and $P_2(x,y)$ of the second degree to calculate the current consumptions ICCINT and ICCO respectively. Hence, the considered function for calculating the junction temperature at any ambient temperature T_a and any parameters (x,y) is given by the Equation IV-5.

$$T_j(x,y) = T_a + R_{th}.(x.P_1 + y.P_2) \quad \text{(IV-5)}$$

Figure IV-21 shows the plotted result for an untested operating conditions at an ambient temperature 70 °C and power supply voltages 2.3 V at VCCINT and 4.8 V at VCCO, the extrapolation of the junction temperature lead to compute the Tj (115 °C) for the specified operating voltages. In addition, the figure shows the limit of test at the ambient temperature 70 °C above which the FPGA could burn-out in less than 24h stress duration. Using the formula IV-5, three different stress conditions have been chosen for M-HTOL test and are presented in Table

IV-8. These stress conditions was chosen in a way that the aging of the FPGAs will be accelerated for a reasonable duration in order to observe degradation in the tested parameters.

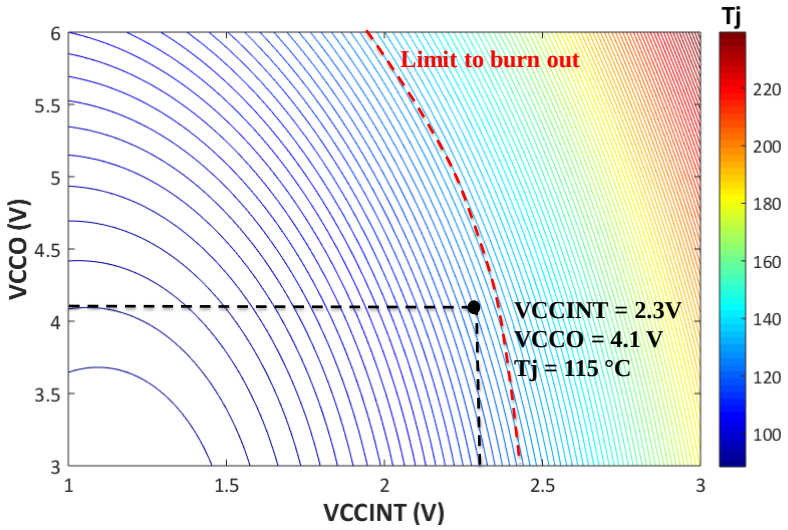

Figure IV-21 Junction temperature evolution at an ambient temperature 70 °C

Stress N°	VCCINT (V)	VCCO (V)	T_j (°C)
1	2,3	4,1	115
2	2,3	4,8	135
3	2,8	5,2	115

Table IV-8 Selected stress conditions for M-HTOL test

3.2.2 High temperature life test results

3.2.2.1 Aging effect on signal integrity

Aging effect on static measurements

During the multiple high temperature life tests, the delay line configuration has been implemented with different standard IOs (LVCMOS33, SSTL15, and DIFF_SSTL15) activated in order to accelerate their degradation and study its effect on signal integrity. The recovery I(V) measurements have been performed at nominal operating conditions and the current variation I_{var_i} is calculation for each component i ϵ [1,5] as expressed by Equation IV-6. The Figure IV-22 presents the average current variation I_{var} of LVCMOS33 and SSTL15 output buffers at the nominal power supply voltages V_{nom} (3.3 V and 1.5 V) recorded using I(V) measurements at the different stresses. The average current variation I_{var} is calculated for the N=5 tested components at each stress as given by Equation IV-7.

$$I_{var\_i}(V_{nom}) = \frac{I_{stress}(V_{nom}) - I_{i_{initial}}(V_{nom})}{I_{initial}(V_{nom})} \quad \text{(IV-6)}$$

$$I_{var} = \sum_{i=1}^{N} \frac{I_{var\_i}}{N} \quad \text{(IV-7)}$$

For each stress conditions, the figure shows a decrease in the current level for the PU and PD devices according the square root of time. In reliability, the evolution of characteristics during accelerated aging tests is mainly presented according to the log or the mean square of time. Furthermore, the current variation level decreases when the overstress voltage (VCCO) increases. The PD devices are once again degraded as seen in the step stress results, and the degradation level has increased up to – 22 % for the LVCMOS33 PD device and – 95 % for SSTL15 PU device due to the over temperature stress. However, in contrary to the step stress results, the LVCMOS33 PU devices are also degraded during the life test. This is due to the activation of NBTI mechanisms which is triggered when the applied voltage is 2 to 3 times the nominal voltage value and when the temperature is between 25 °C to 200 °C as explained in the chapter I.

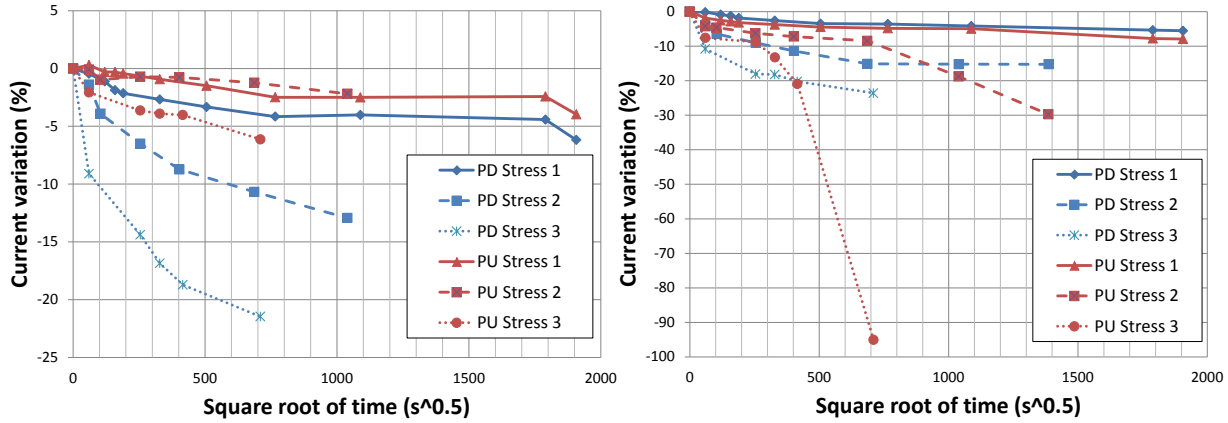

Figure IV-22 Current variation on PD and PU devices of LVCMOS33 (left) and SSTL15 (right) output buffers for the different stresses

Aging effect on timing profile measurements

As the aging affect the FPGA signal integrity, the timing profile of the signals have been measured in order to follow up the evolution of the rise and fall times for the different tested IO standards. Figure IV-23 presents the evolution of the average transition times at the rising and falling edges of an LVCMOS33 output buffer for the different tested FPGAs at the applied stress conditions. The transition time variation is calculated following the same principle as the current variation presented previously using Equations IV-6 and IV-7. The figure shows an important increase in the fall times when the applied stress conditions (voltage/temperature) increase. Furthermore, the rise times also increases, which follows the degradation of PU transistors as seen in I(V) measurements.

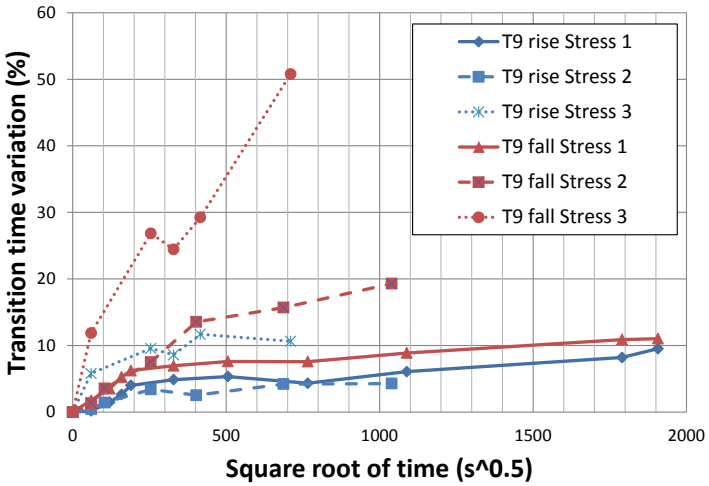

Figure IV-23 Transition time variation of LVCMOS33 output buffer for the different stresses

The measurements of the timing profiles of DIFF_SSTL15 pins have shown a significant decrease in the signals amplitude. Figure IV-24 presents the variation of the amplitude of the differential pins for the different applied stresses. The amplitude variation decreases when the applied stress voltage and temperature increases. Furthermore, although the differential pins E1 and E2 are manufactured symmetrically, the figure shows that they do not degrade systematically with the same percentage. For example, at the stress 2, the amplitude variation of E1 reaches – 30 % after 500 h (1342 $s^{1/2}$) of cumulative stress time, while it only reaches – 10% for E2 pin. This could be due to the dispersion of the degradation mechanisms activation or to the process manufacturing which is confidential. The reduction of the differential signal level mainly affects the device signal integrity.

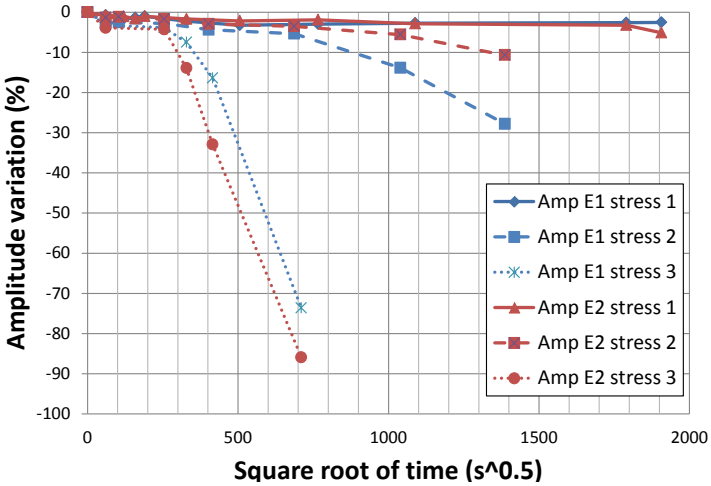

Figure IV-24 Amplitude variation on differential pins (DIFF_SSTL15) for the different stresses

Since the amplitude level of DIFF_SSTL15 pins decreases due to aging and the rise and fall times are calculated between 10 % and 90 % of the signals amplitude, it is more relevant to compare the evolution of the signals slew rate to assess the aging effect on the FPGAs signal integrity. Figure IV-25 shows the slew rate variation at the rising and falling edges of E1 and E2 pins for each stress conditions. This figure shows a significant decrease in the slew rate when the

stress voltage increases, and it reaches a variation of -90 % at the final recovery measurement of the stress number 3.

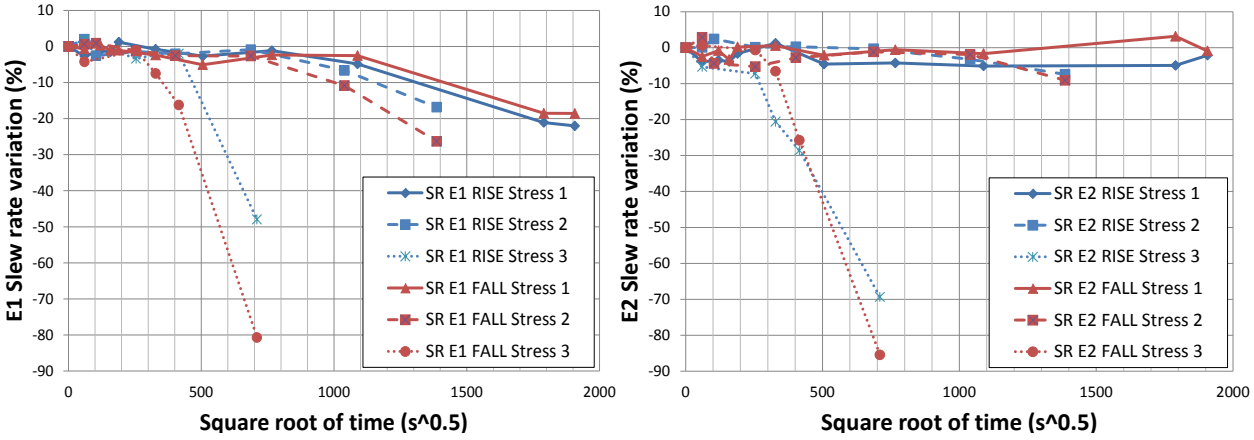

Figure IV-25 Slew rate variation on differential pins (E1/E2) for the different stresses

The degradation of differential output buffers has an important impact on the common voltage level as seen in the step stress results. During the life test, the recovery measurement of the differential pins profile time has been recorded for several periods in order to compute to common mode voltage in the frequency domain. Figure IV-26 shows the evolution of the common mode (CM) spectrum level after each recovery measurement of a FPGA at the stress conditions number 3 (2.8 V, 5.2 V, 115 °C). The figure shows a significant increase in the CM level at the final around + 30 dB at the frequency 1 MHz. This could contribute in the radiation emissions (RE) of the FPGA. However in this study no RE measurements have been performed since it is not the purpose of this work.

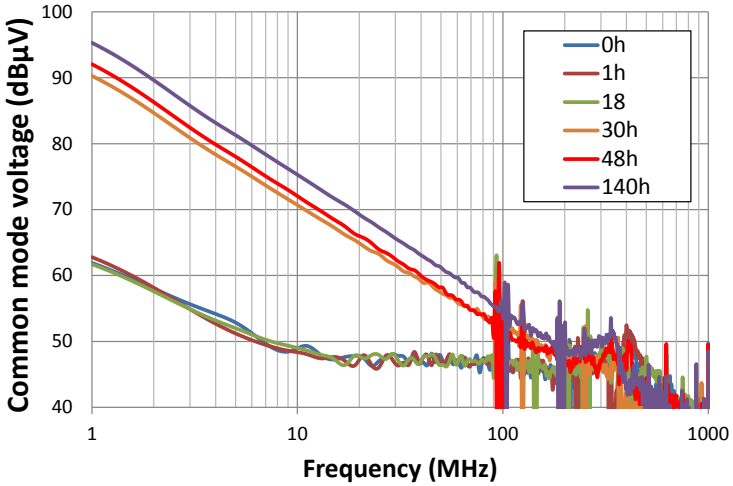

Figure IV-26 Common mode voltage in frequency domain of one stressed FPGA at the stress conditions N° 3

The common mode level evolution has been studied on the different stressed components and for every stress conditions. To summarize the obtained results, the average CM level is calculated at the frequency range [1, 100] MHz. Figure IV-27 presents the evolution of the average CM level for the different stress conditions. Although the temperature overstress accelerates the degradation of differential output buffers, it is mainly dependent on the overstress voltage.

Knowing that the nominal voltage of DIFF_SSTL15 pins is 1.5 V, the stress 1 is applied at 4.1 V and shows a slow evolution of the CM level which reaches +3.2 dB at the final recovery measurement after 1000 h (1906 $s^{1/2}$) stress duration. However, when applying a stress voltage 4.8 V, the CM level increases more rapidly and reaches +8 dB after 500 h (1341 $s^{1/2}$). Furthermore, at 5.2 V which represents 3.46 times the nominal voltage, the CM level increases of +14 dB after only 140 h (709 $s^{1/2}$) stress duration.

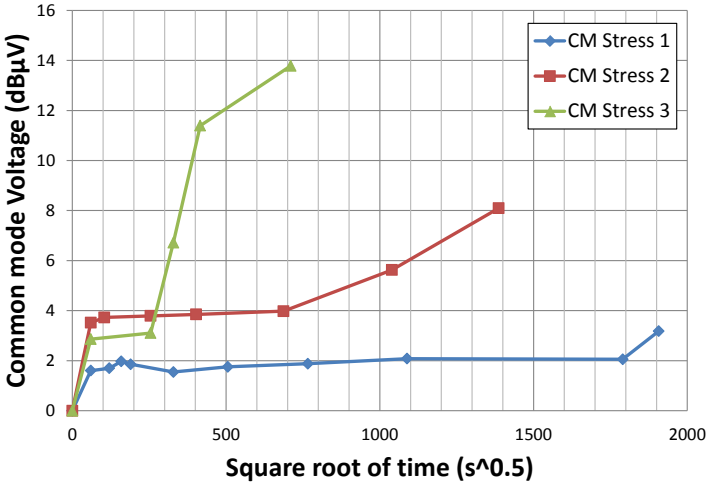

Figure IV-27 Average common mode voltage level evolution between [1,100] MHz for the different stresses

In this section, it was demonstrated that aging has a significant impact on the signal integrity of the studied FPGA. Using SI measurements, different IO standards have been characterized. The main impacts are listed as follow:

- I(V) measurements show that the current level of LVCMOS33 and SSTL15 output buffers decreases significantly and the reduction level depend on the stress conditions. This is due to the activation of HCI and NBTI degradation mechanisms on the NMOS and the PMOS transistors respectively.
- V(t) measurements have shown the increase of the rise and fall times of LVCMOS33 IO and an important decrease in the DIFF_SSTL15 IO amplitude. The degradation of the differential pins leads to an important dissymmetry in the signals profile time, thus, the outputs common mode voltage level increases.

The performance of IOs could also impact the conducted emissions. As seen in the Chapter II, an IBIS file was used to reproduce the internal activity of the switching IOs. The impact of aging of IOs on CE will be studied later in this chapter.

3.2.2.2 Aging effect on propagation delays in digital logical blocks

To assess the aging effect on the propagation delays between the FPGA internal logic blocks, the same structure of a ring oscillator was implemented in different areas of the FPGA in order to increase the number of tested structures. In fact, each area is considered as a different component which allows increasing the confidence level during the statistical study that will be presented in the next section. Overall, the aging increases the propagation delays, hence, the switching frequency become slower. Figure IV-28 shows the average variation of the ring oscillators (RO)

output frequencies for the different applied stresses. The aging phenomena are accelerated by voltage and temperature overstress. Thus, according to the applied stress conditions, the variation of ROs output frequencies will have a different level. The aging affects the timing performances of the FPGA and make it less reliable.

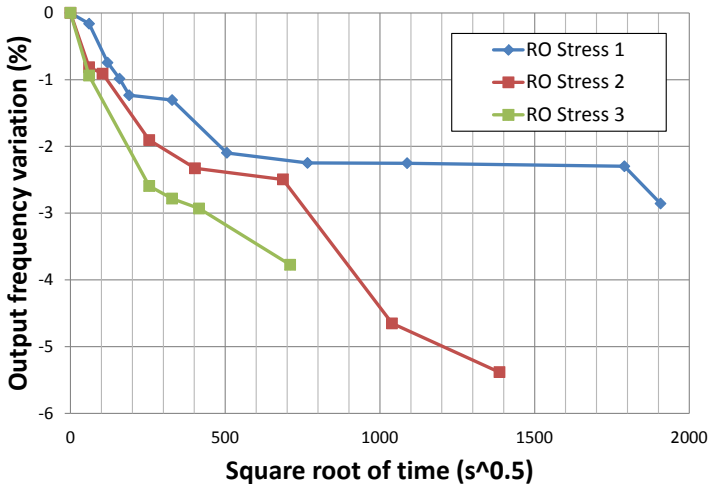

Figure IV-28 Average RO frequency variation for the different stresses

3.2.2.3 Aging effect on EMC

Conducted emissions measurements are performed at every step of the M-HTOL test using the 1 Ω probe for the delay line configuration when the IOs are activated and when they are disabled. Figure IV-29 presents an example of CE initial and after 500 h aging measurement when no IO is activated and when the FPGA was stressed under the second stress conditions (2.3 V, 4.8 V, 135 °C). In the time domain, the figure shows a reduction in the peak-to-peak amplitude of the measured voltage using the 1 Ω probe from 27.3 mV to 22.2 mV after 500 h aging. Furthermore, in the frequency domain, the envelope level presents around 3 dB reduction after aging. Since only the CE amplitude has reduced and the switching rate has not changed, this could be due to the degradation of the internal transistors which modified the transient current produced by the core of the FPGA.

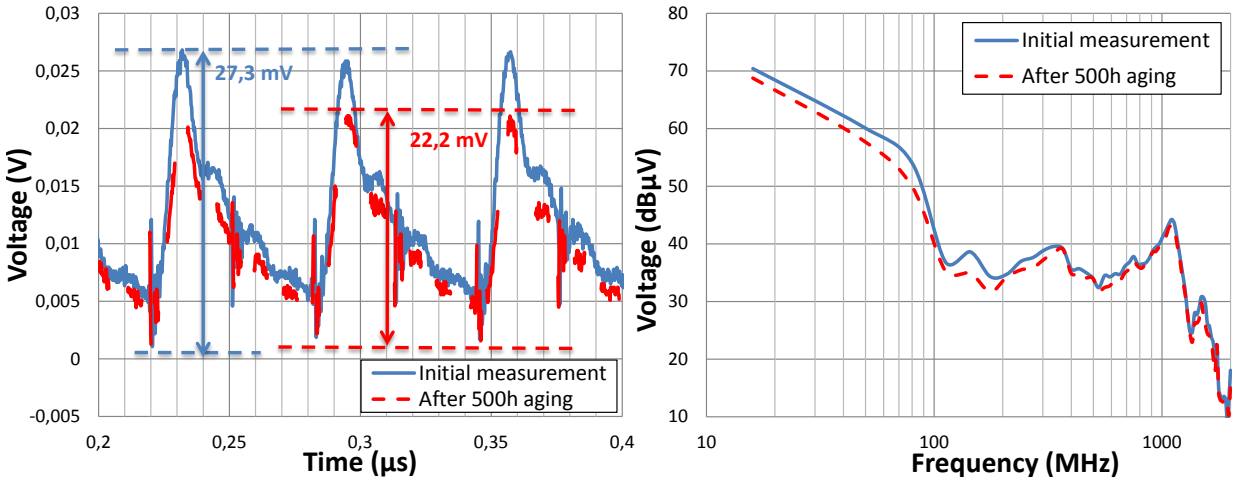

Figure IV-29 Initial and after 500 h aging CE measurement in the time and frequency domain using the 1 Ω probe at the stress conditions number 2

This study was held for the different studied FPGAs and at the different specified stress conditions. The evolution of CE is assessed using the calculation of the average different between the CE level after aging and the initial measurements on the frequency range [16 MHz, 1 GHz]. Figure IV-30 presents the evolution of the average CE with activated and deactivated IOs. The figure shows a gradual reduction of CE level after each recovery measurements which are more significant when the stress conditions are more severe. The parameters influencing the CE will be studied later in this chapter.

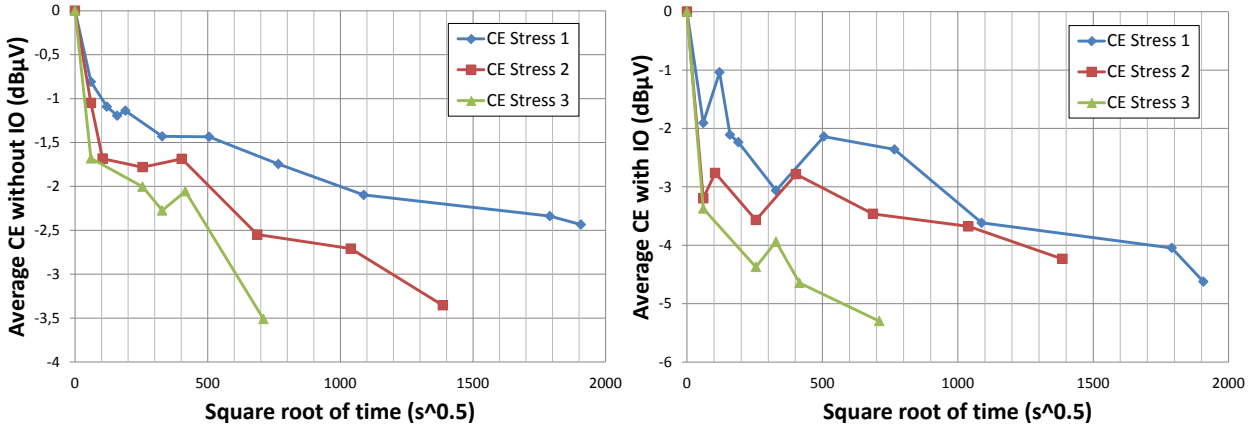

Figure IV-30 Evolution of the average CE variation without activated IOs (left) and with activated IOs (right) at the different stress conditions

4. Reliability model construction

The degradation of the intrinsic parameters of the studied FPGA in the previous section allows the construction a reliability model for a specified degradation criterion (e.g. IO static characteristic change, rise or fall time increase, emission level change, etc.). Moreover, the reliability models based on log-normal and Weibull's distribution will be used to calculate the number of FITs for each stress condition and compare these data to those provided by the MSTORM model. Several components have been tested in order to emphasize the statistical distribution purpose in the reliability model construction.

The obtained correlation between the constructed reliability parameters in this section with the MSTORM model allows the validation of the MSTORM model used for the prediction of FIT for untested operating conditions. In this section, the calculation steps of the reliability parameters will be detailed and validated.

4.1. Methodology of reliability model construction

4.1.1 Reliability model using the Log-Normal distribution

Several components have been tested for each stress conditions, their degradation can be assumed to follow the log-normal distribution as for the majority of semiconductor devices. The log-normal distribution is not used for the construction of MSTORM model, but it is the simplest method that allows the computation of the time to failure in the wear-out stage. It will be compared later to the Weibull distribution which is considered in the MSTORM model construction. The log-normal distribution assumption for semiconductor devices results from the

additive effects of random variables as is frequently found in measurements in mechanical assembly [80]. Furthermore, from a historical consideration, in [81], Reynolds has reported the log-normal failure mode of MOS transistors. Hence, for the reliability model construction, the main parameters that allow calculating the MTTF for the log-normal distribution are the acceleration factor and the standard deviation.

The acceleration factor is useful in describing the overall effect of a specific accelerated stress condition compared to that at a reference stress. It is the ratio of the longer time required to achieve a given failure state for the product at low stress to the shorter time required at higher stress [80]. For a log-normal (LN) distribution, the acceleration factor is the median lifetime noted $t_{50\%}$, which means the necessary time duration for 50 % of a population of component to reach the degradation criterion. The Mean Time To Failure (MTTF) is then calculated using Equation IV-8.

$$MTTF = t_{50\%}.e^{\frac{\sigma^2}{2}} \quad \text{(IV-8)}$$

To understand the methodology of construction of the reliability model using a log-normal distribution, let consider 5 stressed components noted C_i, where $i \in [1;5]$. For any measured parameter, the drift can be reported according to the stress duration in a curve as presented in Figure IV-31. The red dots present the calculated drifts for each component C_i, and the straight lines are the linear interpolation of the observed degradation d_i given by Equation IV-9, where a_i and b_i are constants. Using this equation, the time t to reach a degradation criterion d_i can be extrapolated.

$$d_i = a_i.\sqrt{t} + b_i \quad \text{(IV-9)}$$

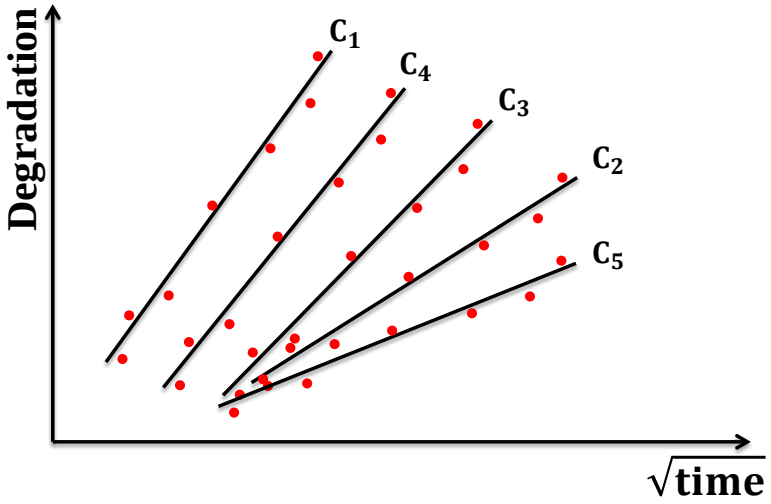

Figure IV-31 Illustration of the drift plot according to time for different stressed components

The second step consist in calculating the cumulative failure percentage which gives the rate of degraded components for a given degradation criterion. The cumulative failure percentage is calculated by dividing the cumulative failure by (N+0.5), where N=5 (the number of tested components). An example is given in Table IV-9 where for a given degradation criterion d (e.g.

10 % drift), the necessary time t_i for each component C_i to reach this degradation is calculated. Then, the times could be sorted in an ascending order in order to write the cumulative failure in the order given by Table IV-9. Finally, the cumulative failure percentage is computed.

Time to degradation criterion (h)	Cumulative failure	Cumulative failure (%)
$t_1 = \left(\frac{d - b_1}{a_1}\right)^2$	1	18,2
$t_2 = \left(\frac{d - b_2}{a_2}\right)^2$	2	36,4
$t_3 = \left(\frac{d - b_3}{a_3}\right)^2$	3	54,5
$t_4 = \left(\frac{d - b_4}{a_4}\right)^2$	4	72,7
$t_5 = \left(\frac{d - b_5}{a_5}\right)^2$	5	90,9

Table IV-9 Cumulative failure percentage for a given degradation criterion

The obtained data can be reported in a log-normal plot, i.e. the x and y axes stand for the cumulative percentage failure and the time in a log scale respectively. The linear interpolation of the plotted data gives the time $t_{50\%}$ to obtain 50% degraded components. Furthermore, transferring the straight line into the origin of the σ axis gives the value of the standard deviation σ. Finally, the MTTF given in Equation IV-8 can be computed.

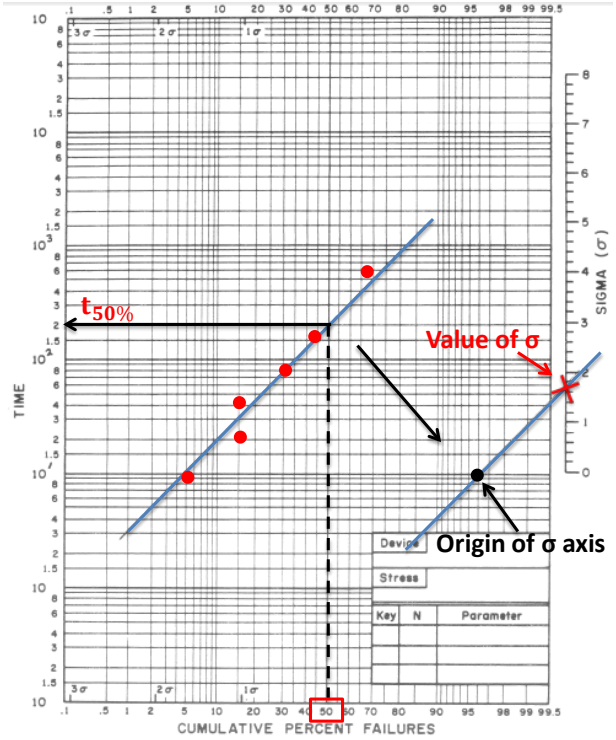

Figure IV-32 Log-normal plot to compute $t_{50\%}$ and σ

These information lead to the computation of the FIT using the formula defined in the previous chapter. Furthermore, since several samples have been tested, the failure number or percentage will vary statistically according to the binomial distribution [80]. Thus, there is a confidence level around each observed failure percentage. The confidence interval gives the limits around which one might expect to find the true value of the confidence percentage chosen. For a normal distribution, the confidence level is given by Equation IV-10.

$$t_{50\%}.e^{\frac{-t.\sigma}{\sqrt{N}}} < e^{\mu} < t_{50\%}.e^{\frac{t.\sigma}{\sqrt{N}}} \quad \text{(IV-10)}$$

Where e^{μ} is the exponential value of the true median of the distribution, and t is the Student's t distribution reported in the Figure IV-33 since its usual presentation is complicated, it is equal to 2.132 when considering 5 samples for a 90 % confidence level. It is given for double-ended confidence interval and the sample size N.

Double-ended Confidence Interval	80%	90%	95%	98%
Sample size, N				
2	3.078	6.314	12.706	31.821
3	1.886	2.920	4.303	6.965
4	1.638	2.353	3.182	4.541
5	1.533	2.132	2.776	3.747
10	1.383	1.833	2.262	2.821
15	1.345	1.761	2.145	2.624
20	1.328	1.729	2.093	2.539
25	1.318	1.711	2.064	2.492
30	1.311	1.699	2.045	2.462
40	1.303	1.684	2.021	2.423
60	1.296	1.671	2.000	2.390
120	1.289	1.658	1.980	2.358
∞	1.282	1.645	1.960	2.326

Figure IV-33 Student's t distribution adapted to confidence level and the sample size [80]

4.1.2 Reliability model using Weibull's distribution

Weibull's distribution for the statistical analysis of the failure mode allows modeling the three life stages of semiconductor components (infant mortality, useful life, wear-out). Each distribution of the failure rates which characterizes the three zones of the bathtub curve can be expressed by the different values of the Weibull parameter β. This distribution is therefore widely used in the analysis of the reliability of electronic circuits and systems. In order to build a reliability model using Weibull's law, the probability density function must be considered. It is given by Equation IV-11.

$$f(t) = \left(\frac{\beta}{\alpha}\right).\left(\frac{t}{\alpha}\right)^{\beta-1}.e^{-\left(\frac{t}{\alpha}\right)^{\beta}} \quad \text{(IV-11)}$$

Where α is referred as the characteristic TTF and β is Weibull slope parameter (or shape parameter). Considering the integral of the probability density function, it is possible to calculate the cumulative failure probability function using the Equation IV-12.

$$F(t) = 1 - e^{-\left(\frac{t}{\alpha}\right)^{\beta}} \quad \text{(IV-12)}$$

Considering the Weibull plot, the parameter α can be found when the cumulative failure percentage F is 63.212 %. This could be shown when rearranging Equation IV-12 as given by the Equation IV-13, when F is equal to 63.212 % in the Weibull plot, the expression ln(-ln(1-F) is equal to 0, which leads to $\ln\left(\frac{t}{\alpha}\right)=0$ then t = α.

$$\ln[-\ln(1-F)] = \beta.\ln\left(\frac{t}{\alpha}\right) \quad \text{(IV-13)}$$

In order to report the measured data of the degradation parameter in the Weibull plot, the median rank method can be used. The median rank estimator is used for the estimation of the unreliability of each failure. It gives the value of the true probability of failure. Considering the percentage P as given by Equation IV-13, the rank can be found by solving the cumulative binomial equation of Z, where j is the number of failures and N is the number of tested samples.

$$P = \sum_{k=j}^{N}\binom{N}{k}Z^k(1-Z)^{N-k} \quad \text{(IV-14)}$$

To simplify the resolution of this equation, the median rank (MR) value can be obtained using Bernard's approximation given by Equation IV-15.

$$MR = \frac{j-0.3}{N+0.4} \quad \text{(IV-15)}$$

In order to compute the Weibull's distribution, the logarithmic value of the MR is plotted according to the time for the calculated degradation of each sample as seen in Figure IV-34. The y axis is plotted using the formula given by IV-16. Thus, using a linear approximation of the plotted data, and regarding to the Equation IV-13, the shape parameter β can be obtained as the slope of the linear curve, and the TTF ($\alpha = t_{50\%}$) is obtained for MR = 63.212 %.

$$y = \ln[-\ln(1-MR)] \quad \text{(IV-16)}$$

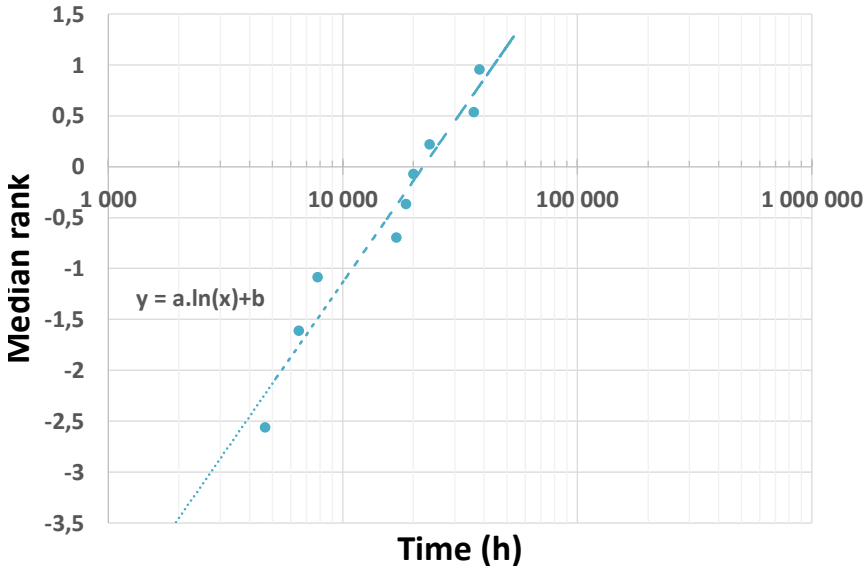

Figure IV-34 Degradation data plot using Weibull's distribution

Finally, the failure in time (FIT) can be computed using the Equation IV-17, when the standard deviation σ value is that one extracted using the log-normal distribution.

$$FIT = \frac{10^9}{t_{50\%}} . e^{\frac{\sigma^2}{2}} \quad \text{(IV-17)}$$

4.2. Construction and validation using MSTORM model

4.2.1 Construction using the Log-Normal distribution

As presented in 3.2.2.2, the calculated mean drifts on the five tested components for each stress conditions have shown a decrease in the ring oscillators' output frequencies, which means the increase of the propagation delays. In order to compute the reliability parameters following the methodology presented in the last section, the average drift of the three implemented ring oscillators will be calculated for each tested components C_i. This means that at given stress conditions, the drift RO_i for a component C_i is calculated after each recovery time t_j, where j is the number of recovery times, for the three implemented ring oscillators using the Equation IV-18.

$$RO_i = \frac{d_{RO1\_i} + d_{RO2\_i} + d_{RO3\_i}}{3} \quad \text{(IV-18)}$$

An example of the application of the presented methodology will be detailed for the stress conditions (2.3 V, 4.1 V, 115 °C). Figure IV-35 presents the calculated drifts for each stressed components and their linear interpolation according to the square root of time. It should also be noted that after 500 hours stress duration, the components C2-4 and C-5 were completely burned-out.

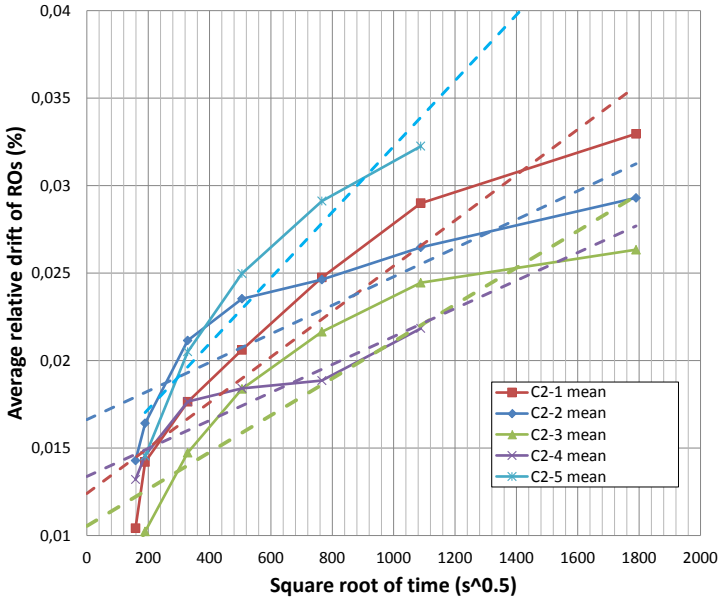

Figure IV-35 Average relative drift calculated on the three ROs at the first stress conditions for the five tested components

Using the plotted data in Figure IV-35, the linear interpolation equations are reported in Table IV-10 for each aged component C_i and the 10 %, 20 % and 30 % drifts are extrapolated. Considering the first line of the Table IV-10, the data means that 36.4 % of the tested components will reach a 10 % drift after 21316 hours, and 20 % drift after 97760 hours and 30 % drift after 229760 hours.

	Time to 10% drift (h)	Time to 20% drift (h)	Time to 30% drift (h)	N° of failures	CRF (%)
$d_1 = 10^{-5}\sqrt{t} + 0{,}0184$	21316	97760	229760	2	36,4
$d_2 = 8.10^{-6}\sqrt{t} + 0{,}0166$	30189	145987	348591	4	54,5
$d_3 = 10^{-5}\sqrt{t} + 0{,}0105$	22250	99750	232806	3	72,7
$d_4 = 7.10^{-6}\sqrt{t} + 0{,}0143$	32550	151126	356508	5	90,9
$d_5 = 3.10^{-6}\sqrt{t} + 0{,}0175$	5196	24154	57001	1	18,2

Table IV-10 Extrapolated drifts using the linear equations and the corresponding cumulative relative failures

These data are reported in the log-normal plot as presented in Figure IV-36. For each drift criterion, the linear interpolation will be performed. Thus, the green, blue and red straight lines lead to the MTTF calculation for 10 %, 20 % and 30 % drift respectively.

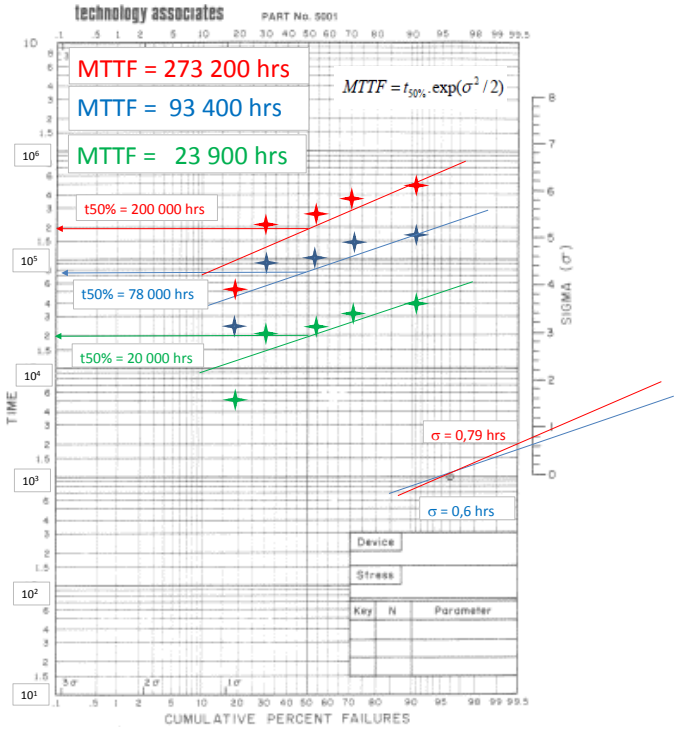

Figure IV-36 MTTF calculation using the log-normal plot for the stress conditions 1

Finally, the same strategy is applied to the second and third stress conditions. The MTTF is then calculated for the different drift criteria and is presented in Figure IV-37. It is clear that the more severe the stress conditions are, the more lower the calculated MTTF is. This leads to greater values of the Failure In Time (FIT).

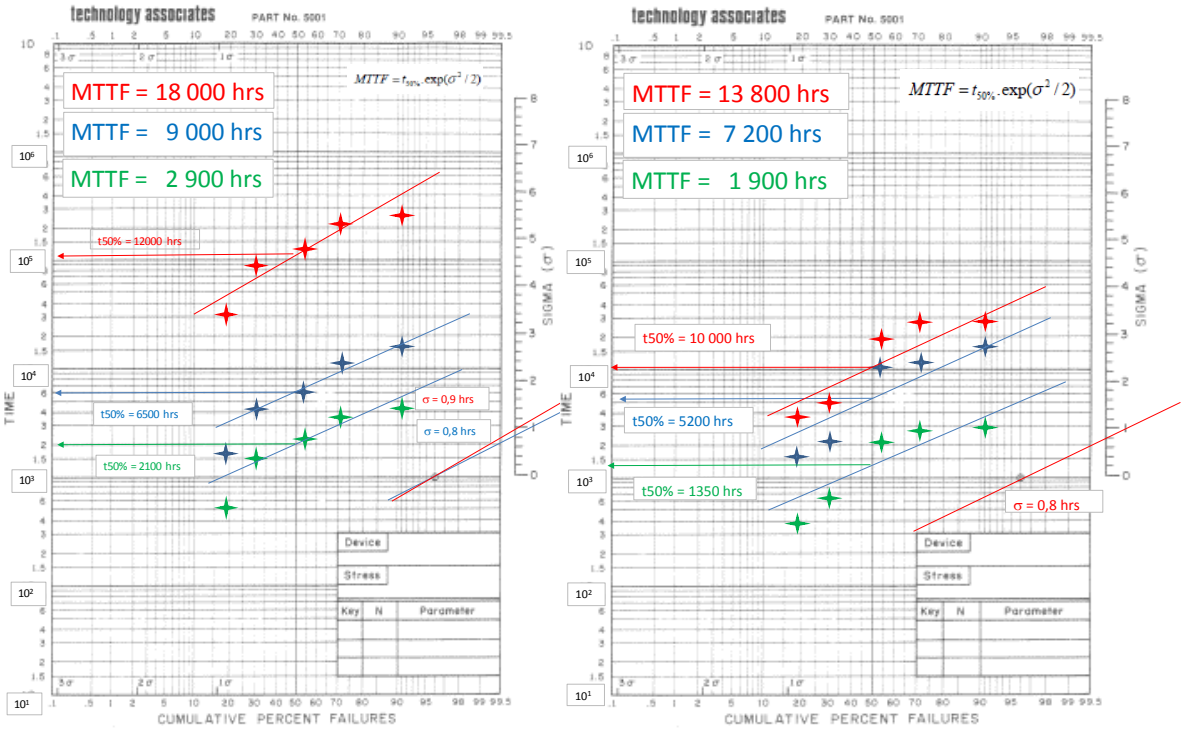

Figure IV-37 Log-normal plot of degradation data for the stress conditions 2 and 3

In this section, time to failure was calculated by considering the total average of drifts on the 5 tested components. To study as many samples as possible, it will be necessary to consider each configured ring oscillator in a different zone of the FPGA as a different component, which will lead to multiply the number of samples by three. This study will be carried out in the statistical calculation with the Weibull distribution. However, the 90% confidence levels for the reliability parameters calculated with the log-normal law are presented in the Table IV-11.

Stress condition	MTTF (h)			90 % Confidence level (h)		
	10 %	20 %	30 %	10 %	20 %	30 %
1	23900	93400	273200	± 94168	± 44019	± 11287
2	2900	9000	18000	± 5087	± 3031	± 979
3	1900	7200	13800	± 4663	± 2425	± 629

Table IV-11 Calculated MTTF and 90 % confidence level for the different stress conditions

The 90% confidence levels calculated in the table show a large spread of the calculated MTTFs. To have less dispersion, it is possible to calculate the confidence level at 60%, but the levels will be given with less precision. The use of the log-normal law to evaluate the statistical distribution of degradations of a batch of components is common in the reliability models that are interested in the wear-out phase. The failure rate is therefore not constant in this area of the bathtub curve. These data will, however, be compared with the statistical calculations established using the

Weibull's distribution, which allows to consider the phase of the constant and non-constant failure rate.

4.2.2 Construction using Weibull's distribution

As presented in 4.1.2, the methodology of construction of a reliability model using Weibull's distribution is applied on the tested FPGA. The degradation criterion concerns the drift on the output frequency of the ring oscillator. To study a large number of samples, the 15 implemented ring oscillators are considered as independent devices. As an example of the methodology application, the first stress conditions are studied. The first step of the analysis concerns the percentage drift calculation for each ring oscillator at the different recovery measurements. The linear interpolation of the obtained data allows the extrapolation to 10 %, 20 % and 30 % drifts. Then, the cumulative failure is computed using the median rank method. Table IV-12 summarizes the degradation information for the stress conditions 1 and the median rank calculation.

Time to 10 % Drift (h)	Time to 20 % Drift (h)	Time to 30 % Drift (h)	N° of failures	Median Rank
2402	10828	25314	1	-3,06787
3076	14142	33261	2	-2,14582
3207	14836	34962	3	-1,64628
10907	50935	120367	4	-1,29179
12641	58646	138313	5	-1,01026
14642	70365	167709	6	-0,77167
15593	79685	193335	7	-0,56029
33682	162524	387829	8	-0,36651
36088	171018	405918	9	-0,18361
38711	185740	442494	10	-0,00612
47704	241113	587042	11	0,171265
49542	253987	616793	12	0,354898
59270	292999	704146	13	0,554526
79815	440288	1068715	14	-0,790156
86023	462718	1161982	15	1,128508

Table IV-12 Calculated drifts and median ranks for the stress conditions 1

The data given by Table IV-12 are plotted in the Weibull plot as presented in Figure IV-38. The dots represent the calculated median ranks according to time in hours. This plot allows the linear interpolation which gives the slope of each degradation criterion and is considered as the shape parameter β. As seen in this figure, for the different cases the shape parameter β is close to 1 ($\beta \approx 1$), which means that the drifts result from the random degradation of the FPGAs and appeared in the useful life in the bathtub curve, where the failure rate is constant. Finally the TTF can be

obtained using the numerical analysis when the median rank is 63,212 % or when the linear interpolation of the y axis crosses the value zero (y = 0).

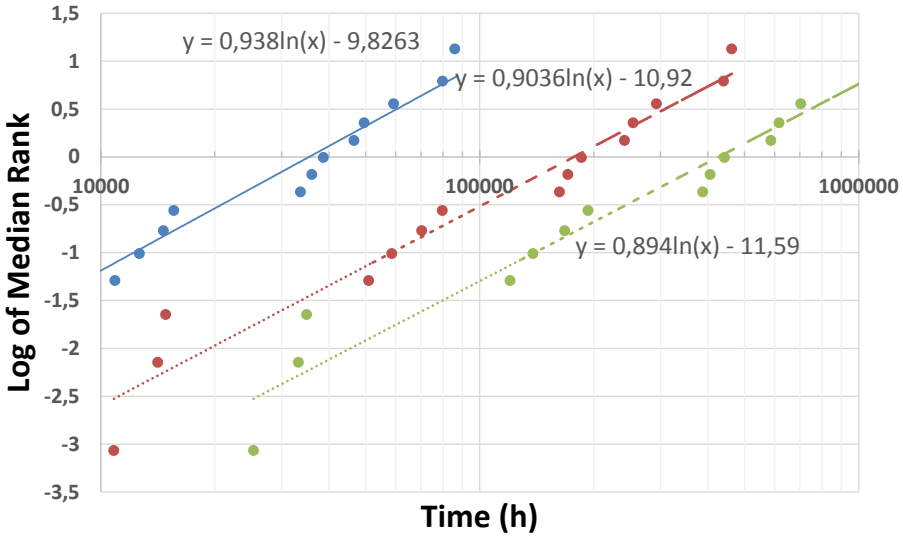

Figure IV-38 Weibull's distribution for the stress conditions 1 at 10 %, 20 % and 30 % drifts of the ROs output frequencies

The same strategy has been followed for the stress conditions 2 and 3. However, since these stress conditions are more severe than the first one, the plotted data using Weibull's distribution have shown that components reach the wear-out phase at the final recovery measurements. Figure IV-39 presents the Weibull plot for the stress conditions 2 when the ring oscillators' drifts are extrapolated to 30 %. This figure shows two linear interpolations for the same stress conditions, which gives two different slopes. The blue line represents the components that degrade randomly with a shape parameter β close to 1 (β ≈ 1), the orange line presents a slope greater than 1 (β > 1) which characterizes the wear-out phase. However, in the wear-out stage, the failure rate is non constant and this has not been studied in the MSTORM model but is considered in the perspectives of the reliability study. Hence, in this work, only the degradation of the useful life stage will be studied.

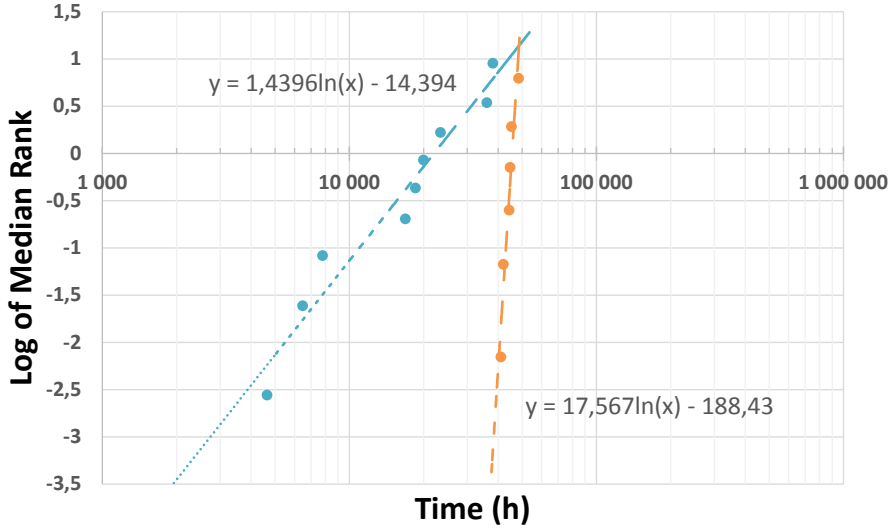

Figure IV-39 Weibull plot for the stress conditions 2 for 30 % drift

The Table IV-13 summarizes the MTTF calculation for the different stress conditions and at different drift percentages. These data will be considered for the constant failure rate and the Failure In Time (FIT) presented in the next section and compared to the log-normal distribution and MSTORM model.

Stress condition	MTTF (h)		
	10 %	20 %	30 %
1	35455	177193	426858
2	2442	9781	21996
3	2631	12364	29291

Table IV-13 Calculated MTTF for the different stress conditions using Weibull's distribution

4.2.3 Comparison with MSTORM model

The M-HTOL testing method has been performed during this study in order to compare the reliability results with the MSTORM model. The MSTORM model is constructed following the methodology presented in Chapter III, and it is able to predict the FIT for any degradation criterion at any operating conditions. For the calculated MTTF with Weibull's and log-normal distribution, the numbers of FIT have been computed. Furthermore, the different stress conditions for the core power supply VCCINT and the junction temperature T_j are included in the MSTORM model in order to predict the FIT. The Table IV-14 shows that for the different stress conditions, the calculated FIT using Weibull's and the log-normal distribution are respectively three and two times the predicted FIT with MSTORM. It can be seen, especially, in the stress conditions 2 and 3 that the calculated FIT in this study are greater than the predicted FIT with MSTORM model. This can be explained by the stress applied on the IO power supply voltages VCCO, which accelerates the aging of the component. The MSTORM model does not take into account the combination of three stress parameters (VCCINT, VCCO, T_j) but only the two parameters (VCCINT, T_j), the integration of a third parameter would make the model more complicated.

Stress condition	MSTORM		Weibull's distribution		Log-Normal distribution	
	MTTF (h)	FIT	MTTF (h)	FIT	MTTF (h)	FIT
1	47870	31320	177200	8461	93400	15348
2	21960	68290	9781	153300	9000	211865
3	39110	38330	12360	121300	7200	264832

Table IV-14 Comparison of the reliability parameters between MSTORM model and the log-normal and Weibull's distributions

However, the Figure IV-40 presents the placement of the calculated FIT using Weibull's distribution for 20 % drift on the generated MSTORM model for the FPGA 45 nm process. This figure shows that although the calculated FITs do not perfectly match the MSTORM prediction, but since the ratio is not very large, the calculated FIT are placed in the 90 % confidence level of

MSTORM model. The confidence level is limited by the dashed lines around the specified power supply voltage. Moreover, this figure shows that the calculated FITs are placed in the area of activation of the NBTI mechanism. Only Weibull's data are plotted since they represent the random degradation of the useful life ($\beta \approx 1$) which is comparable with MSTORM data as it is constructed for constant failure rate.

Although some improvement are needed in the MSTORM model, as including the aging effect on the IOs, it is possible to use the model for the prediction of FIT in nominal conditions (1.2 V, 3.3 V) and for any applied temperature. In the automotive and aeronautic industries, the operating temperature of the electronic components is 80 °C and 110 °C for the space industry. Hence, the reliability model of a FPGA manufactured under 45 nm technology process is reported in Figure IV-40 by the green curve (solid line) and the 90 % confidence level (dashed green lines). At the operating conditions (1.2 V, 80 °C), the FIT is predicted for 20 % drift using MSTORM data and placed in the figure with the star point. On the other hand, as provided by A. Bensoussan, FIDES and the MIL-HDBK-217 data, for respectively the temperatures 80 °C and 110 °C, has been extracted and used in the MSTORM model for FIT calculation. The Figure IV-40 presents the predicted FIT using MSTORM model at the nominal operating power supply voltage under 80 °C and 110 °C.

Table IV-15 summarize the predicted MSTORM reliability model for a different set of data provided from the different standards. It shows that for FIDES and MIL-HDBK data, the reliability model predicted using MSTORM gives a good correlation between the different data.

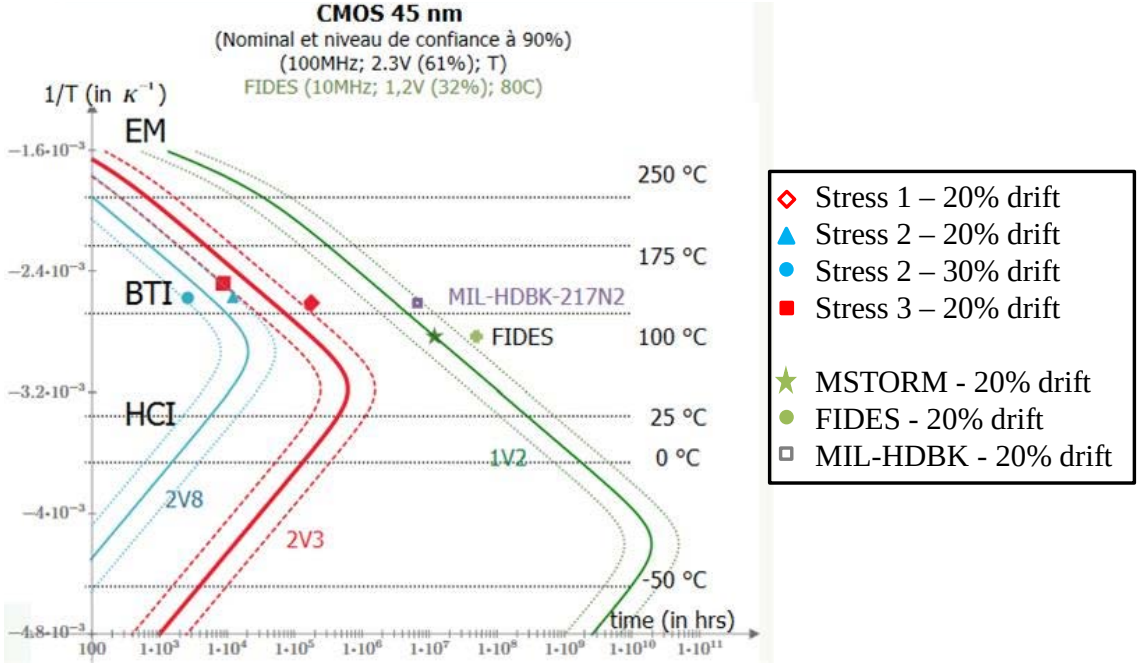

Figure IV-40 Calculated FITs with Weibull's distribution (red and blue points) for the three stress conditions placed on the MSTORM model for 2.8 V and 2.3 V on VCCINT

Operating conditions	MSTORM data		FIDES data		MIL-HDBK data	
	TTF (h)	FIT	TTF (h)	FIT	TTF (h)	FIT
1.2 V, 3.3 V, 1.5 V, 80°C	$1.2\ 10^7$	125	$5.3\ 10^7$	29	-	-
1.2 V, 3.3 V, 1.5 V, 110°C	$3.14\ 10^6$	477	-	-	$9\ 10^6$	167

Table IV-15 Predicted reliability using MSTORM model for MSTORM data and FIDES and MIL-HDBK data

4.3. Conclusion on reliability model construction

In this section, the reliability parameters (TTF, FIT…) have been extracted using two different reliability laws in order to study the statistical distribution of the observed degradation on the output frequency of the ring oscillators. Although the log-normal distribution was explained and applied in this work, it is mainly considered when the failure rate is non constant in the wear-out stage. However, the application of Weibull's distribution is more accurate since it allows the observation of the two slopes of the shape parameter β, which gives valuable information on whether the component is showing random degradation that appears in the useful life or hard failure that appears in the wear-out stage. The comparison of the computed data with MSTORM model prediction has shown some differences with a ratio that varies between two and three, which is acceptable since the computed data can be placed in the 90 % confidence level of MSTORM model. Furthermore, the MSTORM model shows that only NBTI mechanism was activated in FPGA digital core during the accelerated life test. Unlike the mathematical laws of Weibull's and the log-normal distribution that are used to compute the FIT only for experimental data, the MSTORM model allows the prediction of the FIT for untested conditions.

As presented, only the degradation of the propagation delays that is linked to the drift on the output frequency of ROs has been studied. The reliability model construction concerned the internal logic blocks similarly to the basement of MSTORM model. However, in this study, it was observed that NMOS and PMOS transistors of output buffers present important degradation which will certainly affect the signal integrity and the radiated emission of the FPGA. Yet, there is no existing reliability model that allows the prediction of the degradation of output buffers of DSM components. The main improvements expected for MSTORM model are the study of the wear-out stage in order to take into account the non-constant failure rate, and add one further stress parameters on the power supply voltage of IOs in order to extend the MSTORM model to the output buffers.

In order to quarry the actual MSTORM predicted reliability for a given drift percentage, the degradation of the propagation delays will be integrated in ICEM-CE model in order to study its influence on the conducted emission of the core of the FPGA. On the other hand, the degradation on the output buffers will be integrated in the IBIS file. Although, it is not a predictive method to study the degradation on the IOs but it will allow evaluating the effect of a modified IBIS file on conducted emissions.

5. Long-term electromagnetic robustness: Study of ICEM-CE model after aging

The construction of an ICEM-CE model of the tested FPGA has been performed from the construction of the PDN block and the IA blocks for the Core activity and IOs activity, this work was presented in the Chapter II. The aging effect on the PDN block parameters has not been studied in this work. Previous studies as [82] have shown that the PDN was not altered by the aging of a 90 nm digital integrated circuit. Thus, the construction of the ICEM-CE model of the FPGA after aging will not concern the PDN block which is considered unchanged. Furthermore, since, the accelerated aging tests have not been performed on the ELECIS-F board, then the decoupling capacitors and the PCB properties are not degraded and the board model is the same as that used in the Chapter II. With the advanced DSM components, the aging studies mainly concern the degradation of the chip properties with the activation of the different degradation mechanisms. Since the measured parameters concern the output buffers and the propagation delays of the internal signals, the IA Core and IOs blocks will be studied after the aging of the FPGA using EM numeric simulations.

5.1. IA Core block construction after aging

As seen in 2.3, the conducted emission measurements using the 1 Ω probe are performed for the delay line configuration with 900 cascaded delay line blocks in series and 10 inverters per block. In order to study the parameter influencing the internal activity of the FPGA, the obtained data from the ring oscillator measurements are considered for the variability of the propagation delay. As presented in Equation IV-19, the output frequency of the ring oscillator is inversely proportional to the propagation delay τ between the different logic blocs of the FPGA, with 2N+1 the number of inverters constituting the ring oscillator configuration. Hence as seen in the results of the M-HTOL tests, when the output frequencies of the ROs decrease, the propagation delay increases. Furthermore, the propagation delay is inversely proportional to the maximum current amplitude I_{max} of the switching activity of the FPGA, which is given in Equation IV-20. Thus, the current peak-to-peak amplitude will decrease with the aging and it can be expected that the external voltage measurement V_{EXT} will also decrease with aging, since it is proportional to the transient current I_{max}, as seen in Equation IV-21, where H is the transfer function between the external voltage and the internal activity.

$$f_{RO} = \frac{1}{2.N.\tau} \quad \text{(IV-19)}$$

$$I_{max} = \frac{2.P_{dyn\_avg}}{f_{clk}.V_{DD}.\tau} \quad \text{(IV-20)}$$

$$V_{EXT} = H.I_{max} \quad \text{(IV-21)}$$

Considering the stress condition N° 2 (2.3 V, 4.8 V, 135 °C), the measurements on the aged components C1, have shown a decrease of the output frequency of the RO of 5.5 % after 500 h. The IA Core block is constructed from the average dynamic power consumption estimated using XPA tool, and the propagation delay is extracted from the static timing analysis report. Then, the

propagation after aging τ_{stress} is calculated using Equation IV-22, where $\tau_{initial}$ is the initial propagation delay before aging and d is the drift percentage. The obtained data for the tested delay line configuration are summarized in Table IV-16.

$$\boldsymbol{\tau_{stress} = \tau_{initial} + d.\tau_{initial}} \quad \text{(IV-22)}$$

Delay line Configuration	Estimated Dynamic Power (mW)		Data path delay (ns)		Average toggle rate (%)
	Logic	Clock	Logic	Clock	
Before Aging	40	4	8	0,7	100
After 500h aging	40	4	**8,44**	**0,7385**	100

Table IV-16 Dynamic power consumption and data path delay before and after aging for the delay line configuration

The internal activity parameters are constructed from solving the Equation IV-20 using the data presented in Table IV-16. The IA Core block construction before and after aging are presented in Figure IV-41 and integrated in the ICEM-CE model for CE simulation.

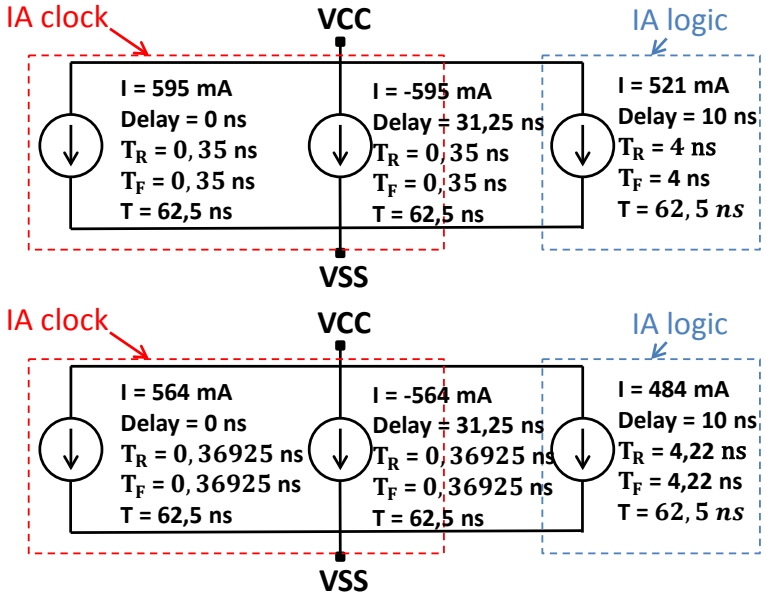

Figure IV-41 Internal activity of the Core block construction before (up) and after (down) aging

The comparison between the measured and simulated conducted emission using the 1 Ω probe is performed for the initial measurement and after 500 h under the stress condition 2 as presented in Figure IV-42. The simulated CE before aging shows a good prediction of the peak-to-peak amplitude (27.3 mV) in the time domain. After aging, the simulated CE amplitude (23.4 mV) slightly overestimates the measured peak-to-peak amplitude (21.8 mV), but overall, the constructed ICEM-CE model after aging provides a good prediction of the CE level in the time domain.

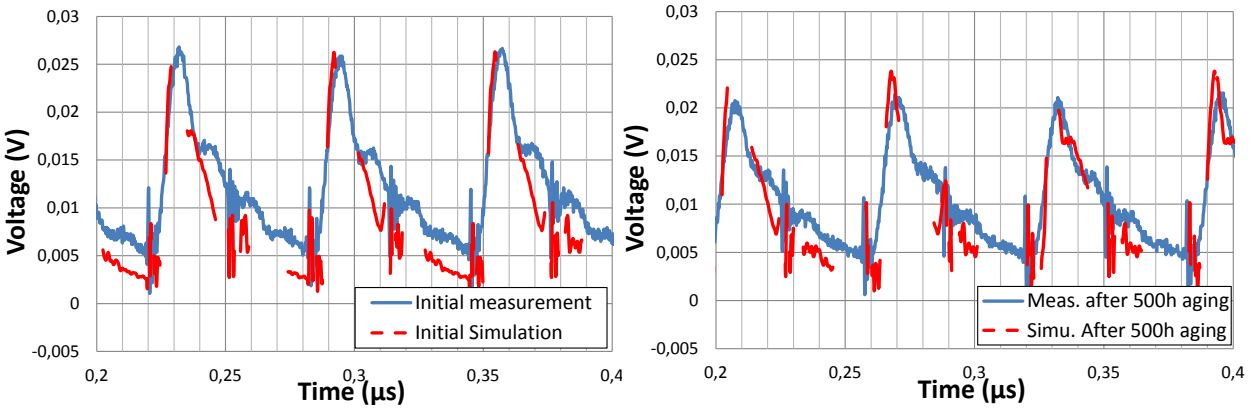

Figure IV-42 Comparison between the measured and simulated CE using the Ω probe at the initial measurements and after 500 h aging under the stress conditions 2 in the time domain

The comparison between the measurement and simulation of CE level before and after aging in the frequency domain has shown that at the initial state (before aging), the simulated envelope can predict the general trend of the CE with a calculated average RMS error around 6.79 dB. After aging, the simulated envelope of CE in the frequency domain provides a good prediction of the measured with a calculated average RMS error is 6.21 dB. Figure IV-43 presents the variation of the measured and simulated CE spectrum at 144 MHz, where the variation is more significant, before and after 500 h aging at stress condition 2. Although the simulation underestimates the variation of the CE degradation level but it is able to predict the trend nigh to 2 %.

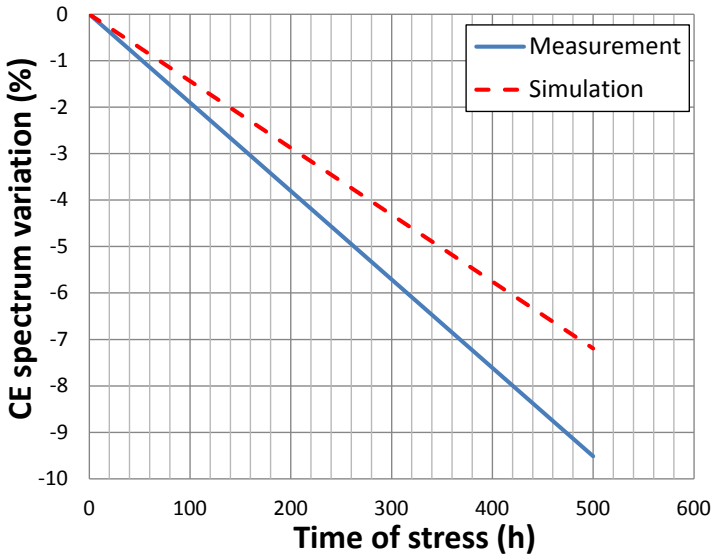

Figure IV-43 Comparison between the variation of the measured and simulated CE spectrum from the initial state and after 500 h aging under the stress conditions 2

In order to evaluate the simulated trend of CE for the different drifts studied in the previous section, CE simulation were performed for increased propagation delays τ_{stress} up to 10 %, 20 and 30 % from the initial value $\tau_{initial}$ and the maximum amplitude of the current sources are constructed according to each propagation delay evolution. Figure IV-44 presents the prediction of CE in the time and frequency domain for each drift. The figure shows the decrease of the peak-to-peak amplitude of the external voltage simulated using the 1 Ω probe when the drift

percentage increases. This results in the reduction of the envelope level in the frequency domain. However, since the impact of the degradation on CE is not significant, the simulated CE level in low frequencies shows very small variations.

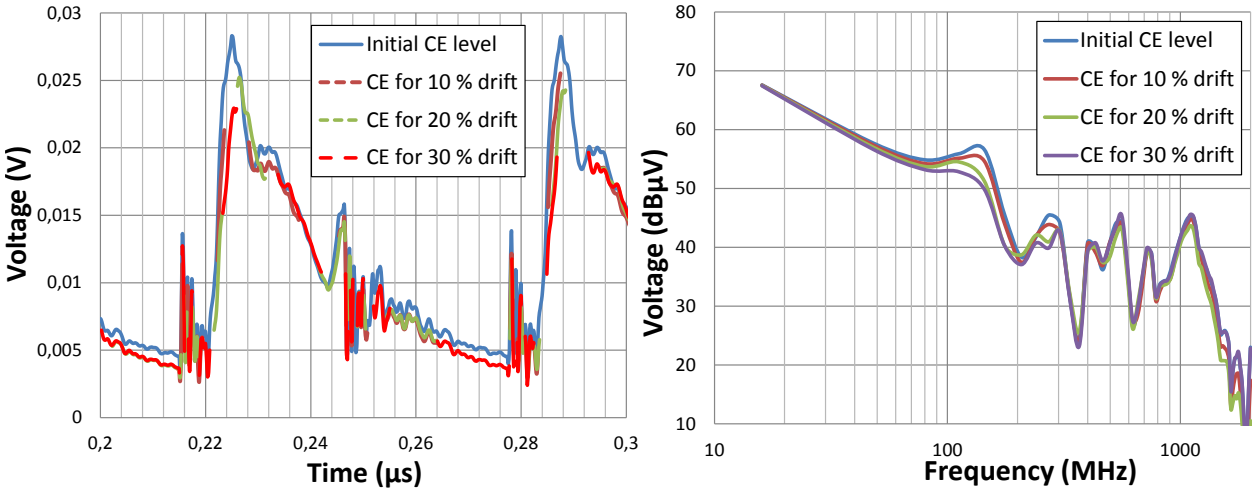

Figure IV-44 Prediction of CE level in the time and frequency domain for different propagation delay drift percentage

Figure IV-45 shows the predicted TTF for each conducted emission degradation in time and frequency domains. In the time domain the variation is calculated for the simulated CE peak-to-peak amplitude. In the frequency domain, the variation is calculated for the simulated CE at 144 MHz where the CE evolution is more significant. The MSTORM tool allows the prediction of the TTF for any degradation criterion at any operating conditions, then, the degradation can be integrated in ICEM-CE model for CE level prediction.

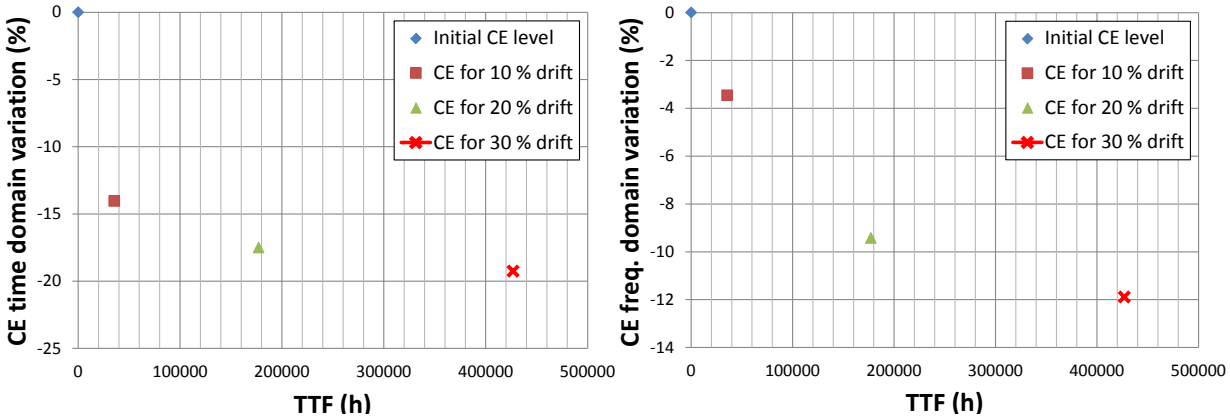

Figure IV-45 TTF prediction for CE variation in the time and frequency domain for different degradation criteria

The IA Core block depends mainly on the dynamic power consumption and the propagation delays of internal signals. During the accelerated tests using the over voltage and over temperature overstress only the degradation of the propagation delays was observed. For an aeronautic or automotive application, the MSTORM model predicted that the component will reach 20 % degradation after 1.2 10^7 hours of operating life. As presented in this section, the integration of the degradation of the propagation delay in the IA Core block construction allows

the prediction of the amplitude level in the time domain and a good accuracy of the trend in the frequency domain is obtained.
Although this study has shown a reduction in the CE level after aging which is not critical for the EMC purpose, but the components timing performances has presented serious degradations. Overall, the presented methodology for construction of the electromagnetic robustness model shows that for any degradation criterion, it is possible to estimate the time to failure and predict the evolution of CE level. The presented methodology can be applied for any integrated circuit, especially, the devices that could show an increased CE level after aging such as the DC/DC converter [83].

5.2. IA IO block construction

The construction of the IA block when the IOs are activated is based on the integration of IBIS files in the ICEM-CE model in order to reproduce the switching activities of the IOs depending on the type of output buffers standard and the termination loads. This methodology is explained in Chapter II, and is used in this section in order to compare the measured and simulated CE when the IOs are activated. The implemented configuration during the aging process includes three output buffers of LVCMOS33 standard: one output buffer of single-ended SSTL15 standard and a differential pair of DIFF_SSTL15 standard. Foremost, for each activated output buffer in the delay line configuration, an appropriate IBIS file is integrated in the ICEM-CE model with the IA IO constructed before aging presented in the previous section. Figure IV-46 presents a comparison between the measurement and simulation of CE using the 1 Ω probe before aging. The figure shows that in the time domain, the simulated peak-to-peak amplitude (48 mV) predict with a good accuracy the measured peak-to-peak amplitude (52 mV). Furthermore, the simulated envelope in the frequency domain reproduces the trend of the measured envelope with an average RMS error 7.05 dB. The differences presented between the measurement and the simulation could be due to same reasons explained in the previous section.

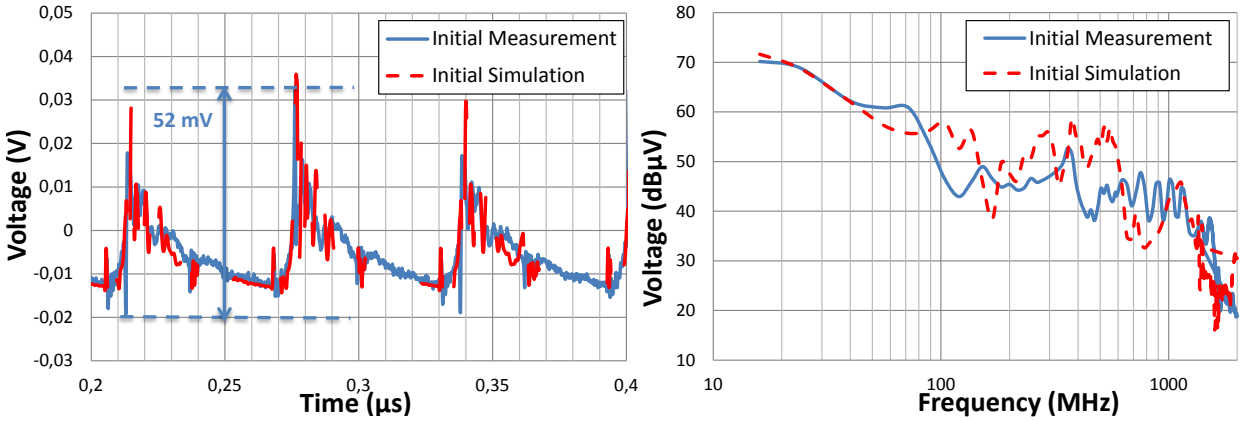

Figure IV-46 Comparison between measured and simulated CE using the 1 Ω probe before aging when the IOs are activated

After aging, the output buffers are degraded with a significant reduction in the current static current recorder using I(V) measurements and an increase in the rising and falling times shown

with the V(t) signal integrity measurements. The IBIS files are then modified with the measured I(V) curve and V(t) data after aging. Then, ICEM-CE model is constructed from the IA Core after 500 hours aging, the modified IBIS files with the after aging data (IA IO) and the unchanged PDN and board model. Figure IV-47 shows the comparison between measured and simulated CE using the 1 Ω probe after 500 h aging under test condition 2. It is shown that the simulated and measured peak-to-peak amplitude has been reduced after aging. Furthermore, the simulated amplitude (43 mV) is similar to the measured amplitude (45 mV). The comparison between the measured and simulated envelope in the frequency domain also shows a good correlation with a computed average RMS error 6.59 dB.

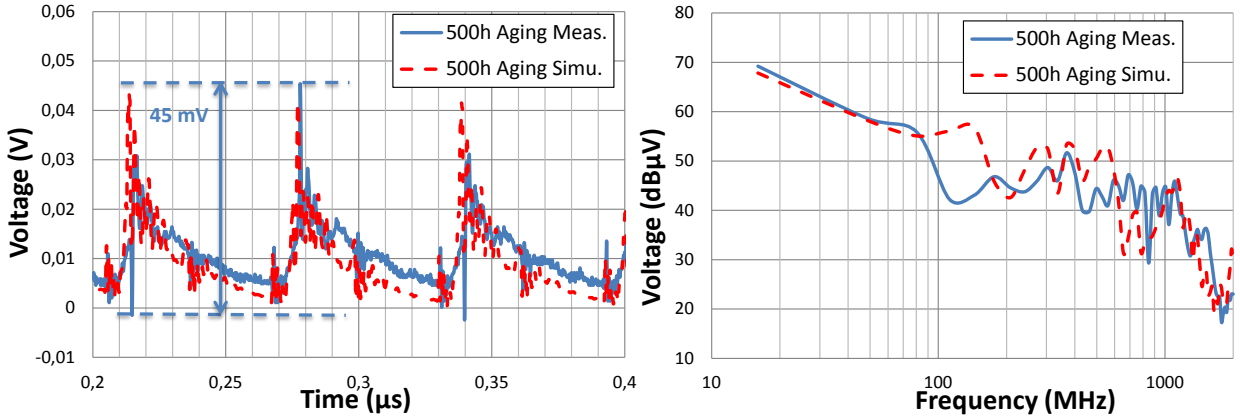

Figure IV-47 Comparison between the measured and simulated CE using the 1 Ω probe after 500 h aging under test conditions 2

In this section, it was demonstrated that using the appropriate IBIS file in the ICEM-CE model allows a good accuracy of the simulated CE before and after aging. The main parameters of static current and dynamic V(t) profiles must meet the performances of the tested FPGA. However, the presented results do not allow the construction of a predictive model when the IOs are activated, because several data are missed and should be studied experimentally for the construction of an adapted MSTORM model for the IOs which is completely feasible. It only shows the contribution of the IBIS file in the CE. On the other hand, the construction of a predictive IA IO model needs the study of the PU and PD devices in order to extract the IBIS file according to a degradation criterion and using an acceleration factor calculated with the experiments data.

To understand the parameters that activate an output buffer, let consider a 3 state output. The high impedance state is simulated by deactivating the PU and PD devices. This state is neglected in the following description since only an active and switching output stage is considered. The instantiation of the proposed equivalent model is presented in Figure IV-48 compatible with SPICE tools. The different components of the output buffers model are:

- The package model: represented by an equivalent RLC circuit. In the IBIS file, typical RLC values are given. In addition, the FPGA constructor provides a .pkg file that provides electromagnetic simulation results on the IC box. Therefore, a matrix of resistors, inductances, and capacities to model the RLC circuit of the tested output pins is provided.

- The capacitance C_{comp}: IBIS file can provide information about the equivalent capacitance of the output pad. This information can be extracted from the initial IBIS file and considered unchanged after aging. This assumption could simplify the construction of the IBIS file after aging.
- The ground clamp which models the current I_{GC} absorbed by the FPGA according to the output voltage V_{OUT}. Since the I(V) measured characteristics of the FPGA has drifter after aging, a statistical distribution law must be studied to construct the reliability model of the ground clamp device. But it is not essential since the ESD protections are not triggered during the test conditions of EMC and SI.
- I_{PD} and I_{PU} devices: the pull-down and pull-down devices are able to reproduce the current delivered or absorbed by the output, as well as the evolution of their according to the output voltage V_{OUT}. These currents depend not only on the output voltage V_{OUT}, but also on the pull-down and pull-up commands. For the same reason explained for the ground clamp device, a reliability law must be studied for the PU and PD devices. In addition, the strategy used to construct the predictive reliability model of the core of the FPGA can be extended to the IOs by specifying the degradation criterion on the evolution of the static current of the PU and PD devices.
- PD_cmd(t) and PU_cmd(t): the PU and PD control devices can be enabled to be activated or deactivated according to the logic state that must be taken by the output (out_state). By modulating the I_{PU} and I_{PD} currents according to their respective control signals, denoted $K_{PD}(t)$ and $K_{PU}(t)$, it is possible to reproduce the waveforms of transition times at rising and falling edges. These two control signals model the pre-driver of the output stage while preserving the confidentiality of the output buffer. During the accelerated life test, the transitions times has drifted with an increase in the falling and rising times, a deep study must be performed in order to understand if the observed drift could only be linked to the degradation of the PU and PD devices or if a reliability model must be constructed for the control devices as well.

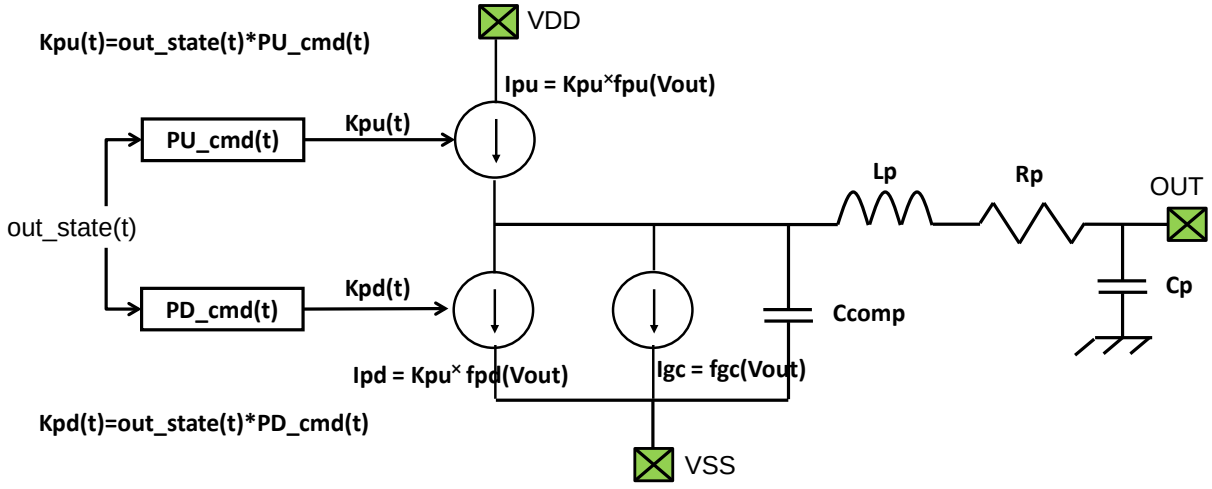

Figure IV-48 3-state output buffer equivalent model

In this work, an equivalent model of the output buffers that takes into account the aging effect for predictive CE simulation was not constructed. Some ideas have been discussed for using the reliability statistical distribution laws on the different devices constituting the output buffers equivalent model. On the other hand, it is also possible to create a new MSTORM model dedicated to the IOs and combine it to the equivalent model of the output buffers (IBIS file, macro-model, etc.). This study takes a long time for testing several IOs from different standard in order to find the most appropriate statistical distribution law for the reliability model construction.

However, it is completely possible to put on a strategy using a design of experiment to test several IOs of each power domain and for different IO standard (LVCMOS33, SSTL15, DIFF_SSTL15), since the FPGA has 186 IOs distributed in four different banks. Furthermore, a dedicated test board must be designed to automatically connect the test connections for SI and I(V) measurements. The degradation can be studied for the evolution of the drain current and also for the evolution of the timing profiles V(t) which mainly affect the PU and PD command. The specification of a statistical distribution law can be integrated in the IBIS file construction process or in the macro-model construction. This method will lead to the prediction of CE level and SI performances using the simulation tools.

6. Conclusion

Due to the technological evolution of ICs and the long-term EM robustness constraints in the embedded application have led to the study of an advanced technology of FPGA. The purpose of this work is the proposal of a new methodology for modelling the EMC level of integrated circuits, the model takes into account the aging effect, in order to allow the prediction of the long-term EM robustness level.

In this chapter, the aging effect on conducted emission level and SI of the FPGA was studied using the constructed reliability parameters that validate the use of MSTORM model. The main idea is setting the methodology of the accelerated tests for over voltage and over temperature stresses. Since the accelerated aging consists in combining two operating parameters, the step stress was applied in order to fix the voltage limits for the different power domains according to the degradation level of the FPGA. During the step stress, the third over voltage stress levels were set as operating conditions limits because above these levels the FPGA could burn-out. These results allow combining the voltage and the temperature during the preliminary study prior to the life tests. The major observation on the preliminary study, which was not applied for a long duration, is the evolution of the junction temperature according the VCCINT and VCCO voltages, and also the ambient temperature. The junction temperature is not calculated precisely, since the thermal resistance of the FPGA was roughly estimated using Xilinx tool. The consumed current increases as well which can lead to very high junction temperature values, hence, the preliminary study allows fixing the appropriate stress operating conditions so that the FPGAs do not burn-out too fast. The proposed methodology for accelerated aging tests can be generalized to any other type of integrated circuit. It is based on several testing phases to identify the most appropriate overstress conditions to guarantee the feasibility of aging in a reduced time. In addition, the proposed methodology is based on the multiple stress tests can be optimized using a design of experiments; this could be implemented in the industrial process of qualification to reduce costs and time.

During the accelerated life test, several FPGAs are stressed under three stress conditions, which is the minimum number of stress conditions. For each overstress conditions, several recovery measurements have been performed to follow up the evolution of the SI characteristics and conducted emission level. The main observations recorded from the experimental results are the reduction of the static current consumption in the I(V) characteristics and the increase in the rising and falling times in the V(t) measurements of the single-ended IOs (LVCMOS33 and SSTL15). These effects are related to the degradation of the PU and PD devices due to the activation of NBTI and HCI mechanisms. The main advantage of the proposed methodology of EMR modeling is its ability to predict the evolution of CE level after a given duration of operating lifetime or to predict the needed time for reaching a certain degree of failure. The proposed model that combines MSTORM and ICEM-CE models integrates the statistical distribution for a user defined degree of confidence level which allows the prediction of the risk of failure using the confidence interval. The prediction of the long-term EMR of integrated circuits allows the evaluation the risk of non-conformity at the nominal operating conditions, and

evaluating the relevance of EMC margins to better define the shielding size and the number of filtering devices.

On the other hand, the differential pins of DIFF_SSTL15 IO standard have shown a reduction of both the peak-to-peak amplitude and slew rate of the timing profiles. Furthermore, each output buffer of the differential pair does not degrade with the same trend as the other. It increases their dissymmetry and could have a serious impact on SI performances and also the radiated emissions of the FPGA. Same types of measurements have been performed on digital programmable blocks of the FPGA. The conducted emission levels at recovery measurements have decreased and the output frequencies of ring oscillators have been reduced after aging which increases the propagation delays of internal signals.

Since the MSTORM model was constructed for the degradation observed on the core a 45 nm FPGA using the degradation of the ROs frequency, hence, in this chapter the log-normal and Weibull's statistical distribution law are studied from the frequency drifts measured on the ring oscillators. The calculated TTF and FITs for 10 %, 20 % and 30 % drift are compared to MSTORM model, and although there are some variations, the calculated values meet with the 90 % confidence interval of MSTORM model. The validation of MSTORM data allows the prediction of TTF for any degradation criterion and operating conditions of the different industrial fields.

In the last section of this chapter, the ICEM-CE model was modified in order to reproduce the CE of the FPGA after aging. The methodology is based on the integration of the drift in the pulse duration of the IA Core. This variation based on the measured drift of the propagation delays of programmable logic blocks. This methodology was confirmed by comparison between CE simulation and measurements. Furthermore, the CE level can be predicted by ICEM-CE model for any drift predicted by MSTORM model. On the other hand, the integration of the degradation of I(V) and V(t) characteristics in the IBIS model allows the simulation of CE when the output buffers are activated and also the SI of the FPGA. A predictive model can be constructed for the degradation of IOs while considering a statistical distribution law and could be a perspective of this work. Furthermore, other perspective are expected for MSTORM model as taking into account the over voltage stress on the power domains dedicated to IOs which should modify the calculated acceleration factors of MSTORM model.

In the previous EMR studies, the testing methods and generated models only allow evaluating the aging effect on EMC level for a specified stress conditions in voltage and/or temperature after the stress period. Hence, no prediction of EMC level or the TTF for the nominal operating conditions could be performed. This issue is overcome with the proposed multiple stress testing method and the combination of MSTORM and ICEM-CE model. In addition, the method can be applied for any other integrated circuit. However, some perspective must be considered, such as extending the MSTORM model to the degradation of IOs and taking into account the non-constant failure rate mode for the prediction of wear-out degradations

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General Conclusion

In the aeronautical, space, and automotive industries, the constraints in terms of EMC compliance and reliability requirements are strong and restrictive for OEMs who manufacture and supply electronic equipment. With the development of numerical simulation tools, some OEMs turned over the modeling in order to overcome the problems of obsolescence and second sourcing, such as using EMC of ICs models, e.g. ICEM-CE model for conducted emission modeling of integrated circuits. Following the existing validation and qualification procedures, integrated circuits manufacturer have no certainty that in a given environment and after a given lifetime, the electronic circuit will always meet EMC requirements. No existing tool allows the prediction of EMC variations during the life cycle of an electronic circuit or system. The aim of this thesis has been the development of a predictive model to ensure the long-term electromagnetic robustness of an integrated circuit, which means an EMC model that takes into account the environment and aging effect. To construct a long-term electromagnetic robustness model, the EMC of IC model must be constructed in a reduced time and with a good accuracy, which is not guaranteed with the existing methods. In addition, the integration of the aging parameter required new information: the mission profile providing the stress conditions and the typical durations of stress for the construction of a design of experiment. Then, specifying a reliability model that allows the reliability prediction for any operating conditions. Using this model, it becomes possible to predict the evolution of EMC levels according to a drift criterion and time to failure.

This study focused on two main topics: EMC model of a FPGA and its reliability predictive model. Their combination led to the creation of an electromagnetic robustness model. The present manuscript was organized in four different chapters in order to address the long-term electromagnetic robustness purpose.

The first chapter dealt with the different aspect of EMC and reliability of integrated circuits in the state of the art and how the scaling of CMOS technology impacts these parameters. In fact, the miniaturization of CMOS technology with the reduction of the gate length and the equivalent oxide thickness lead to the increase of the current density and the switching frequencies and the reduction of the supply voltage. This technological evolution implies the increase of the number of transistors within an integrated circuit. As presented in the first chapter, the CMOS technology scaling leads to the increase of conducted and radiated emission levels of ICs and the reduction of their immunity level. As a result, these last years, several EMC standards have been proposed in order to assess the EMC compliance level and avoid the requalification phases. In addition, there are existing standardized measurement methods that allows the construction of EMC of ICs models, such as the 1/150 Ω probe method of conducted emission measurement on the ground and power pins of an integrated circuit. However, as discussed, the existing EMC models are suffering from some limitations. The modeling of electronic equipment using an IC model is still not viable and EMC expertise is still needed among suppliers to reduce EMC non-compliance risks. The modeling of the ground reference as a perfect plane using simulation tools induces

calculation errors. In addition, tools for automatic model extraction must be provided to IC end users, this was the addressed in the next chapter. On the other hand, as the long-term reliability of ICs is another restrictive topic for industrials, the main intrinsic degradation mechanisms have been introduced such as:

- Electromigration which is activated due to very high current density in chip metallization.
- HCI mechanism which is triggered due to a strong lateral electric field which lead to the injection of hot carriers in NMOS and PMOS transistors.
- TDDB mechanism is related to the breakdown of the gate oxide due to the creation of conductive path through the oxide which leads to the rise of the gate conductance.
- NBTI mechanism mainly appears in PMOS transistors due to a negative potential and high temperature that stresses the gate.

These degradation mechanisms could appear prematurely with technology scaling. As discussed in the second chapter, some research works have demonstrated the aging effect in EMC level, but no existing model allows the prediction of the EMC of IC level after a given lifetime duration or even to predict the needed time for an EMC drift to occur.

The second chapter addresses the results of the first topic of this dissertation which concern the construction of an ICEM-CE model of a complex IC. The studied component is a FPGA manufactured by Xilinx under 45 nm technology process and contains six different power domains and 186 IO users. Even if this circuit is not the most complicated commercial device, it is complex enough for EMC modeling purpose. The ICEM-CE model is constructed from two main blocks: the PDN block and the IA block. A special test board called ELECIS-F was designed in order to construct these two blocks. The PDN block is constructed using S parameter measurements between the different power and ground pins of the FPGA and for different configurations in order to model the different parasitic elements of the package, die capacitance, the parasitic coupling between the different power and ground domains, the substrate coupling and the common mode effect. The constructed PDN was validated up to 2.5 GHz using comparison between simulated and measured impedance. In addition, as the ICEM-CE model allows the modeling of conducted emission of an IC at PCB level, the ELECIS-F board was modeled using an electromagnetic simulation tool (CST Design Suite) with the 3D FE FD solver because it is capable to accurately analyze the entire PCB design in a reduced time and is completely adapted to a multi-layer board. The extracted PCB model has been validated by measurement up to 2.5 GHz. Finally, in order to construct the internal activity block, the extraction method proposed in ICEM standard was followed. The first step consisted in the separation of the core activity and the IOs activity, their modeling was based in two IA blocks: IA Core and IA IO blocks. The IA blocks construction was firstly performed following the standard inverse method that consists in the external voltage V_{EXT} measurement (e.g. 1 Ω probe on the ground pins) and the transfer function H of the estimated PDN and board model in order to compute the internal activity using: $IA = V_{EXT}.H^{-1}$. This method gives good CE level estimation

results when the simulation point is the same as that of the construction (e.g. 1 Ω probe). However, the CE simulation at another point such as 150 Ω probe on the power pins overestimated the measured CE level due to external voltage measurement errors and the transfer function estimation uncertainties. Thus, to overcome this issue, new methodologies for IA Core and IA IO construction have been proposed, to de-correlate the IA construction from the PDN model. For the IA IO construction, one or several IBIS files can be integrated in ICEM-CE model of the FPGA according to the number of activated IOs, which will reproduce the IOs activity following the IOs characteristics (IO standard, slew rate, load…). On the other hand, for the IA Core construction, the proposed methodology consists in using the manufacturer estimation tools for dynamic power consumptions, toggle rate and static timing analysis assuming that the IA waveform does not influence the CE simulation when the transferred charge is respected. A deterministic approach can be used when the switching rates of the internal signals and Configurable Logic Blocks (CLBs) do not vary much, and a statistical approach is proposed when an important variation exists between the signals and CLBs toggle rate. For different validation cases, it was proved that the method based on estimation tools allows a good estimation of CE level in the time and frequency domains. The main advantage of this predictive method is that it allows the construction of the IA independently from the PDN and the board model which reduces the errors in the IA extraction. In addition, this new method reduces the measurements since there is no need to a preliminary external voltage measurement, hence, there is no need to design a specific test board for the ICEM-CE model construction. Moreover, the new methodology integrates the influence of the implemented configuration on the IC without necessary extra measurement. Finally, a dedicated tool called ICEM GENERATOR was developed in order to automate the extraction of IA Core following the deterministic and even the statistical approach. A validation case representative of industrial application has been configured to validate the ICEM GENERATOR tool. This chapter has shown the construction of an ICEM-CE model of a FPGA and the proposition of new predictive methods to extract the IA block and is adapted to industrial applications. The proposed methodology should be adapted to other IC families when the manufacturers provide estimation tools. Otherwise, the extraction should rely on simple observable parameters such as the dynamic power measurements, but this method should be verified and validated on other IC families.

As the purpose of this work is the introduction of the aging effect in the EMC of IC model. The third chapter introduced the existing accelerated aging tests methods based on HTOL and LTOL testing standard and the traditional reliability model widely used in the industry such as MIL-HDBK-217F and FIDES. However, the main limitation of these models is the consideration of only one dominant failure mechanisms without taking into account the possible combination of several degradation mechanisms that accelerate the aging of ICs. In this chapter, the accelerated lifetime models are presented as Arrhenius law for thermal stress, the Inverse Power Law for electric stress, Peck’s law for combined thermal and humidity stresses, Coffin-Manson based law for mechanical fatigue, Black’s law for and Boltzmann-Arrhenius-Zhurkov (BAZ) law for multiple stresses. These accelerated aging laws and the Physic-of-Failure approach are the basis

of the creation of the MTOL model that is based on M-HTOL testing method for temperature and voltage stresses as presented in this chapter. The MTOL model was constructed for the reliability prediction at any operating conditions. It consists on solving a reliability matrix for a minimum of three test conditions in order to activate different degradation mechanisms. In addition, since the activation energy evolution is non-linear, the MTOL model was combined to BAZ model for modeling the non-linearity aspect of the activation energy which led to the development of MSTORM reliability prediction tool. The reliability prediction model was studied for two FPGAs manufactured using two technology processes (45 nm and 28 nm) considering the drift of the internal propagation delays that were observed using a ring oscillator configuration. Overall, this chapter has presented a new model for the reliability prediction taking into account the activation of several degradation mechanisms that allows the prediction of Time To Failure for a given degradation on the core of the FPGA. The next chapter has shown how this reliability model can contribute in the prediction of EMC level drift during lifetime.

The last chapter proposes a new method for testing the reliability of ICs in different characterization phases based on a design of experiments to reduce testing time and select the most appropriate operating conditions to accelerate the aging of the IC without reaching the burn-out state. Foremost, the step stress study defined the electrical operating conditions limits and shows how the electric stress impacts on the signal integrity parameters and conducted emission level. The main observations concern the reduction of drain current of NMOS devices for several IO standards (LVCMOS33, SSTL15), the increase of transition times and the reduction of timing profile amplitude of DIFF_SSTL15 IOs. On the other hand, except the important drift in the common mode noise produced by the differential IOs, no important degradation was observed in CE level. During the accelerated life test, the parameters specified as the stress inputs are core and IO power supply voltages (VCCINT and VCCO respectively) and the junction temperature T_j which was estimated using the thermal resistance given by Xilinx estimation tool but was sufficient to define the acceptable stress temperature. The accelerated life test has shown important degradation in the different tested parameters of signal integrity, propagation delay and CE level. The MSTORM model was constructed for the drift of the propagation delays. Then, in order to be comparable to MSTORM data, the log-normal and Weibull's statistical distributions were computed for the obtained degradation on the output frequencies of the ring oscillators. The calculated TTFs using these methods are located in the 90 % confidence interval of MSTORM model for 45 nm technology, which validate the use of MSTORM model to predict the TTF for untested operating conditions. For any other technology process, the predictive reliability model must be constructed following the same method of solving the reliability matrix using multiple stresses strategy. In this chapter, it was proven that the integration of the propagation delay drift in the construction if IA Core using the methodology described in the second chapter allows the estimation of CE level for a predicted TTF, or even for a given TTF the CE level can be predicted knowing the degradation percentage. On the other hand, the integration of the SI degradation in the IBIS file leads to the estimation of CE level when the IOs are activation. Even if it was not possible to build MSOTORM model for IO for time constraints reasons, it is possible to develop

a MSTORM model adapted to IOs reliability to predict the needed TTF to reach a certain level of degradation of SI or CE.

This work proposes a new method that combines a predictive EMC model for ICs, such as ICEM-CE model, and a predictive reliability model (MSTORM) for multiple stresses which is adapted to any IC family and functions. For example, it could be applied to DC/DC converters for which the evolution of CE level after aging is more critical after aging than for FPGAs. This combination leads to the construction of a predictive long-term electromagnetic robustness model, then, it is possible to predict the CE level at nominal operating conditions after a given time to failure. The proposed methodology is adapted to industrial applications since it allows the reduction of requalification time. Moreover, it may help to fix sufficient margins to respect the EMC compliance with a rigorous method, without applying overdesigned EMC margins.

Some improvements can be provided to this work such as identifying the origin of the differences that could be seen between the measured and simulated CE when the IA is extracted following the new method. Because although the new method provides a good estimation of CE level in the time domain, some differences persist in the frequency domain that lead to an average RMS error between 5 and 7 dB. In addition, the method must be tested in other type of integrated circuits than FPGAs, which do not constitute the most widely used class of embedded circuits. For the reliability aspect, the MSTORM model must be extended to the degradation of IOs in order to predict the signal integrity evolution in a long-term and its impact on CE level. In this thesis, it was presented that the MSTORM approach is valid for the EMC level prediction in addition to the integration the aging effect to the IOs model which gives good results. However, a complete demonstration of the application of MSTORM to the IOs degradation must be performed. Furthermore, one of the main assumptions of the MSTORM model is the constant failure rate mode, which is not realistic at the end of the circuit lifetime. The MSTORM model must take into account the non-constant failure rate mode for the prediction of wear-out breakdown.

ANNEX 1 - EMC requirements in the standards

1. EMC requirements at equipment level

The main disturbance source is the equipment itself which acts as an aggressor and as a victim. The coupling paths existing on a printed circuit board (PCB) or between 2 PCB installed into a calculator's rack are numerous. The origin of the parasitic emissions is mainly due to the dynamic current consumed during the activation of each logic gate of an IC. The sudden and rapid variation in the amplitude of the current conducted through the supply rails causes large fluctuations in the supply voltage due to the parasitic inductance of the internal IC tracks, the bonding wires, the package lead frames, and the PCB tracks.

The consequences of the disturbance on embedded electronic equipment could be dramatic for the transportation industries. For automotive industries, the safety level as required by the ISO 26262 is very high. All automotive functions as the engine calculator, the ABS calculator, the steering control and the indoor calculator are classified according a Automotive Safety Integrity Level (ASIL). Complex functions as the Advanced Driver-Assistance Dystems (ADAS) which allow today the anti-collision or the automatic parking as example will allow tomorrow the full automatic driving. The Safety level of this kind of equipment will be also drastic.

For an EMC point of view, some committees as the Comité International Spécial des Perturbations Radioélectriques (CISPR) founded in 1934 by the International Electrotechnical Commission (IEC) have published numerous norms and standards to define the EMC test set-up for Emission and Immunity. The CISPR is composed of six subcommittees, each responsible for a different area, defined as:

- A - Radio-interference measurements and statistical methods
- B - Interference relating to industrial, scientific and medical radio-frequency apparatus, to other (heavy) industrial equipment, to overhead power lines, to high voltage equipment and to electric traction
- D - Electromagnetic disturbances related to electric/electronic equipment on vehicles and internal combustion engine powered devices
- F - Interference relating to household appliances tools, lighting equipment and similar apparatus
- H - Limits for the protection of radio frequencies
- I - Electromagnetic compatibility of information technology equipment, multimedia equipment and receiver

For automotive OEM and suppliers, the applicable standard is the CISPR 25 - Radio disturbance characteristics for the protection of receivers used on board vehicles, boats, and on devices—Limits and Methods of Measurement. The CISPR 25 ed 4.0 has been published in October 2016. Compared to previous version 2008 dated, this edition take in account the specificities of Electric Vehicles (EV) and Plug-in Hybrid Electric Vehicles (PHEV) including test methods for shielded power supply systems for high voltages and batteries fast charger. As the CISPR 25 is only limited to the conducted and radiated emission, automotive OEM and suppliers also apply some

parts of the ISO 11452 Road vehicles -- Component test methods for electrical disturbances from narrowband radiated electromagnetic energy for the conducted and radiated immunity. The SAE J1113 Electromagnetic Compatibility Measurement Procedures and Limits for Components of Vehicles, Boats (up to 15 m), and Machines (Except Aircraft) (16.6 Hz to 18 GHz) published in 1995 (last revision in 2013) has adopted by reference the IEC CISPR 25 as the standard for the measurement of component emissions. Concerning the RF immunity, the SAE J1113 cover the same topics as the ISO 11452. As example the SAE J1113/27 (reverberation method) is covered by the ISO11452-11 and the SAE J1113/4 (Bulk Current Injection) is covered by the ISO 11452-4.

For aeronautics OEM and suppliers, the DO-160, Environmental Conditions and Test Procedures for Airborne Equipment is the applicable standard for the environmental testing of avionics hardware. DO-160 is published by the Radio Technical Commission for Aeronautics (RTCA) and by the European Organization for Civil Aviation Equipment EUROCAE. The sections 20 and 21 concern the RF emission and susceptibility test methods. The first DO 160 edition has been published in February 1975 and the latest version is the DO-160G or the EUROCAE-ED14 published in December 2014.

List of usual norms applied in transportation industries for the EMC (RF emission and immunity) is given by Table 17.

CISPR 25:2016	Vehicles, boats and internal combustion engines - Radio disturbance characteristics - Limits and methods of measurement for the protection of on-board receivers
RTCADO-160G EUROCAE ED14	Environmental Conditions and Test Procedures for Airborne Equipment Section 20.0 – Radio Frequency Susceptibility (Radiated and Conducted) Section 21.0 – Emission of Radio Frequency Energy
ISO 11452-1:2015	Road vehicles -- Component test methods for electrical disturbances from narrowband radiated electromagnetic energy -- Part 1: General principles and terminology
ISO 11452-2:2004	Road vehicles -- Component test methods for electrical disturbances from narrowband radiated electromagnetic energy -- Part 2: Absorber-lined shielded enclosure
ISO 11452-3:2016	Road vehicles -- Component test methods for electrical disturbances from narrowband radiated electromagnetic energy -- Part 3: Transverse electromagnetic (TEM) cell
ISO 11452-4:2011	Road vehicles -- Component test methods for electrical disturbances from narrowband radiated electromagnetic energy -- Part 4: Harness excitation methods (Bulk Current Injection)
ISO 11452-5:2002	Road vehicles -- Component test methods for electrical disturbances from narrowband radiated electromagnetic energy -- Part 5: Stripline
ISO 11452-7:2003	Road vehicles -- Component test methods for electrical disturbances from narrowband radiated electromagnetic energy -- Part 7: Direct radio frequency (RF) power injection

ISO 11452-8:2015	Road vehicles -- Component test methods for electrical disturbances from narrowband radiated electromagnetic energy -- Part 8: Immunity to magnetic fields
ISO 11452-9:2012	Road vehicles -- Component test methods for electrical disturbances from narrowband radiated electromagnetic energy -- Part 9: Portable transmitters
ISO 11452-11:2010	Road vehicles -- Component test methods for electrical disturbances from narrowband radiated electromagnetic energy -- Part 11: Reverberation chamber

Table 17 EMC standard of the transportation industry

The automotive and aeronautics OEM provide to their electronics suppliers their own EMC requirements in terms of test set-up and levels. Some specific products could have their own requirements in terms of level. OEM specifications always refer to the previous standards as CISPR25 or ISO 11452 for the test set-up. A non-exhaustive list of automotive OEM specification is given in the Table 18.

General Motors	GMW3097 General specification for electrical/electronic components and subsystems, Electromagnetic compatibility requirements
PSA B21-7110	Specification d'environnement des équipements électriques et électroniques, caractéristiques électriques
RENAULT 3600808	Resistance to electrical disturbances and electromagnetic compatibility: instructions concerning electrical, electronic and pyrotechnic equipment
VOLSWAGEN TL865	Interference Emission: requirements
BMW GS 95002	Electromagnetic Compatibility (EMC) Requirements and Tests
DAIMLER DC10614	Component EMC
FORD ES-XW7T-1A278-AC	Ford Motor Company Electronic Component EMC Requirements & Test Procedures.

Table 18 List of automotive OEM specification

To qualify their products, electronics suppliers perform EMC tests according OEM specification. The suppliers EMC laboratories are accredited by a certification company as the COFRAC or directly by the OEM. The Figure 49 illustrates the Conducted Emission measurement of an automotive calculator realized by CONTINENTAL.

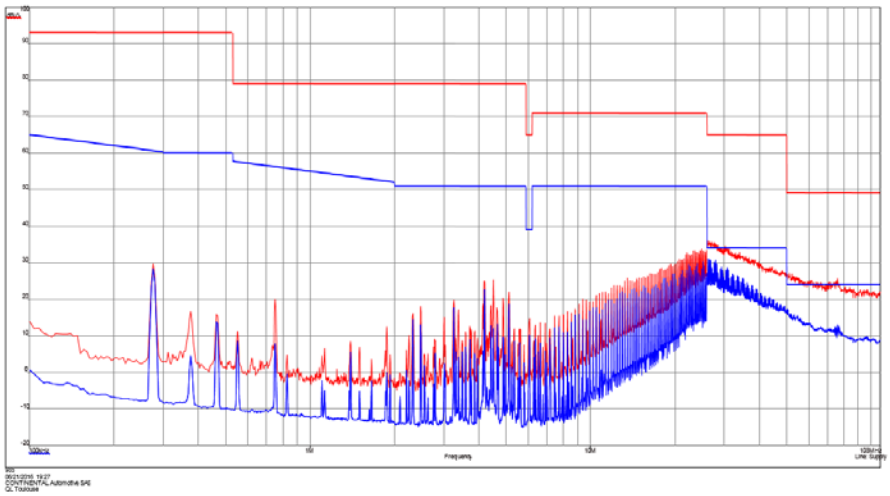

Figure 49 Conducted Emission (voltage method) measurements in Narrow Band (blue) and Broad Band (red) compared with limits given by Renault 3600808 specification.

2. EMC requirements at component level

To be able to success the during their qualification tests or to minimize the risk to fail, electronics suppliers impose to their components suppliers EMC constraints. For automotive suppliers, the requirements given by the Automotive Electronics Council are described by the AEC- Q100-G Failure Mechanism Based Stress Test Qualification dated May 2007. The EMC are evocated in the Annex 5 “Part Design Criteria to Determine Need for EMC Testing” without any reference to requirements or tests methods.

For this reason, each supplier has each own applicable norm. As an example, for SIEMENS VDO (CONTINENTAL AUTOMOTIVE since 2007) the applicable standard was in 2004 the A2C000027649AAA Electromagnetic Compatibility requirements for Integrated Circuits. The Figure 50 gives an example of requirements for CE 1 Ω.

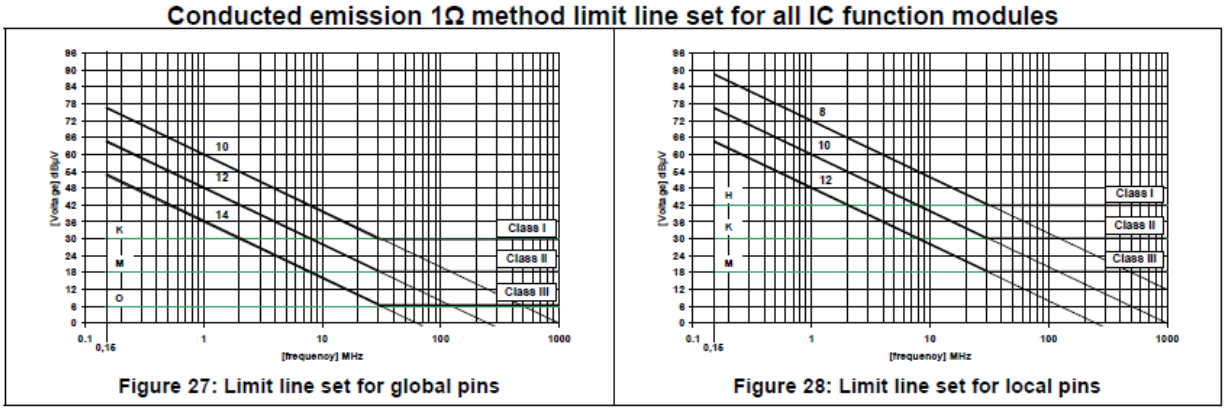

Figure 50 Example of requirements for CE level using the 1 Ω method

The Figure 51 gives an example of requirements for immunity tests.

Immunity limit classes	DPI [forward power] dBm		BCI [forward current] dBmA		TEM [E-field] V/m
	global pin	local pin	global pin	local pin	entire IC
I	18	0	34 (50 mA)	not required	200
II	24	6	40 (100 mA)		400
III	30	12	46 (200 mA)		800
C	customer specific				

Figure 51 Requirements classes for immunity tests

Compared to emission test, the immunity test is associated to a failure criterion which is measured during and after the test. The failure a criterion is not defined by the standard but is fixed by the manufacturer or by the customer. The gravity level of the observed failure for an Integrated Circuit is standardized by the IEC 62215-3 ed 1.0: Integrated Circuits – Measurement of Impulse Immunity – Part 3: Non-Synchronous Transient Injection Method. The gravity levels are resumed in Table XXX

Class A	The IC operates within its tolerances during and after the test
Class B	The IC operates outside its tolerances during the test and inside its tolerance after test
Class C	The IC does not operate during the test but operates within its tolerance after test
Class D	The IC does not operate during and after the test. The IC operates within its tolerance after a manual power SWITCH OFF SWITCH ON
Class E	The IC does not operates anymore even after an external operation

Table 19 Gravity level of an IC of the IEC 62215-3 standard

ANNEX 2 - Overview on the IBIS Standard

Signal integrity (SI) is the technical discipline that aims to ensure good performance of the transmitted signal between a transmitter and a receiver, which is synonym of the correct operation of an integrated circuit. In practical studies, this can be compromised by the characteristics of the transmission lines (impedance rupture, terminations, losses, crosstalk), all the discontinuities introduced by the vias, the package, fluctuations of power supply voltage, the differential and the common mode effect, the characteristics of the transmitter and the receiver. Different criteria allow evaluating the signal quality that can be shown using time domain measurements, such as the eye diagram representation.

Due to the increased bandwidth of digital signals transmitted in high-performance computing applications (e.g. 100 Gbps) and cloud computing (e.g. 50 Gbps), the EMC level and signal integrity become major issues. The last years, a lot of progress in controlling signal integrity has been noted due to proficiency in designing the PCBs, packaging or the circuit design. In addition, different techniques of equalization, adaptive pre/de-emphasizing have become commonly used in high-speed transmitters and receivers to compensate the distortions introduced by the transmission lines.

The control of signal integrity also requires accurate and efficient modeling methods to anticipate signal distortions, jitter, inter-symbol interference, and prevent the risk of errors. The modeling of SI problems requires not only accurate traces and power planes models to correctly predict mismatch problems, power failover, common/differential mode conversion, but also accurate drivers' models, which take into account the nonlinear aspect and pre-processing (SERDES, pre-emphasis ...). However, the manufacturers of ICs do not provide information of IO structures, because it is confidential. The manufacturers only give equivalent models to guarantee the manufacturing process confidentiality of their product.

Signal integrity modeling is performed using an IO description standard named IBIS (Input/output Buffer Information Specification). The IBIS model is a set of parameters represented by simple and usually linear elements designed to hide the exact structure of the circuits. The IBIS model takes into account the timing profile and drain current of IO buffers and the IC package parasitic elements. It provides a simplified but sufficiently fast and accurate description of an integrated circuit IO.

The characteristics of the clamping diodes are provided via a tabulated I(V) curve. Figure 52 presents an example of the I(V) curve of the ground and power clamp diode of the Freescale MPC5554 microcontroller.

```
|*****************************************************************************
|                              Model pad_ae_5p0_in
|*****************************************************************************
|
[Model]           pad_ae_5p0_in
Model_type        Input
Polarity          Non-Inverting
Vinl =    1.5000V
Vinh =    3.5000V
C_comp            8.5000pF            8.5000pF            8.5000pF
|
|
[Temperature Range]       25.0000             0.1500k             -40.0000
[Voltage Range]           5.0000V             4.5000V             5.2500V
[GND_clamp]
| voltage     I(typ)              I(min)              I(max)
|
  -5.0000       -3.9037A            -3.9769A            -3.8718A
  -4.8000       -3.7052A            -3.7789A            -3.6731A
  -4.6000       -3.5068A            -3.5811A            -3.4744A
  -4.4000       -3.3085A            -3.3833A            -3.2758A
 ...
   4.6000        4.7505uA            5.7881uA            4.2307uA
   4.8000        5.1464uA            6.2340uA            4.6271uA
   5.0000        5.5426uA           18.6050uA            5.0238uA
|
[POWER_clamp]
| voltage     I(typ)              I(min)              I(max)
|
  -5.0000        3.9466A             4.0361A             3.9062A
  -4.9000        3.8473A             3.9370A             3.8068A
  -4.8000        3.7479A             3.8379A             3.7073A
  -4.7000        3.6486A             3.7389A             3.6078A
...
  -0.3000        6.1374uA            6.2340uA            6.1159uA
  -0.2000        5.9390uA            5.9891uA            5.9172uA
  -0.1000        5.7408uA            5.7881uA            5.7186uA
   0.0000        5.5426uA            5.5899uA            5.5200uA
|
| End [Model] pad_ae_5p0_in
```

Figure 52 Power and Ground clamp model in an IBIS file

The characteristics of the output devices (Pullup and Pulldown) are provided by 2 tabulated curves: I(V) curve and a timing profile curve (rise and fall) for given load conditions.

Figure 53 shows an example of I(V) curve of the PU and PF transistors of the non-inverting tristate outputs of the Freescale MPC5554 microcontroller.

Figure 54 presents an example of the timing profile curves of the same output for a 50 Ω load (tristate to high-state and high-state to tristate). The IBIS file also provides tristate to low-state and low-state to tristate.

```
|*******************************************************************************
|                            Model pad_sh_5p0_01
|*******************************************************************************
|
[Model]           pad_sh_5p0_01
Model_type        3-state
Polarity          Non-Inverting
Enable            Active-High
C_comp            5.5000pF            5.5000pF            5.5000pF
|
|
[Temperature Range]       25.0000             0.1500k             -40.0000
[Voltage Range]           5.0000V             4.5000V             5.2500V
[Pulldown]
| voltage     I(typ)              I(min)              I(max)
|
  -5.0000       -0.2000mA           -40.0000uA          -0.3500mA
  -4.6000       -0.2000mA           -40.0000uA          -0.3500mA
  -4.2000       -0.2200mA           -40.0000uA          -0.3700mA
...
   9.2000       13.2971A            15.9333A            12.0694A
   9.6000       14.9472A            17.5737A            13.7251A
  10.0000       16.5980A            19.2147A            15.3813A
|
[Pullup]
| voltage     I(typ)              I(min)              I(max)
|
  -5.0000        0.3000mA            0.2000mA            0.3000mA
  -4.6000        0.2000mA            0.2000mA            0.3000mA
  -4.2000        0.3000mA            0.2000mA            0.3000mA
...
   9.2000      -13.3187A           -15.9209A           -12.1254A
   9.6000      -14.9178A           -17.4860A           -13.7434A
  10.0000      -16.5169A           -19.0511A           -15.3615A
```

Figure 53 Pull-up and Pull-down I(V) characteristics of an output

```
[Ramp]
| variable       typ                 min                 max
dV/dt_r          0.7777/0.5334n      0.4357/0.9417n      1.1284/0.3232n
dV/dt_f          0.7769/0.5372n      0.4002/0.9423n      1.1979/0.3406n
R_load = 50.0000
|
[Rising Waveform]
R_fixture = 50.0000
V_fixture = 5.0000
V_fixture_min = 4.5000
V_fixture_max = 5.2500
| time           V(typ)              V(min)              V(max)
|
  0.000s          3.7050V             3.8327V             3.2534V
   0.1020ns       3.7050V             3.8327V             3.2534V
   0.2041ns       3.7050V             3.8327V             3.2534V
   0.3061ns       3.7050V             3.8327V             3.2534V
...
   9.6939ns       5.0000V             4.4999V             5.2500V
   9.7959ns       5.0000V             4.4999V             5.2500V
   9.8980ns       5.0000V             4.4999V             5.2500V
  10.0000ns       5.0000V             4.4999V             5.2500V
|
[Falling Waveform]
R_fixture = 50.0000
V_fixture = 5.0000
V_fixture_min = 4.5000
V_fixture_max = 5.2500
| time           V(typ)              V(min)              V(max)
|
  0.000s          5.0000V             4.5000V             5.2500V
   0.1020ns       5.0000V             4.5000V             5.2500V
   0.2041ns       5.0000V             4.5000V             5.2500V
   0.3061ns       5.0000V             4.5000V             5.2500V
...
   9.6939ns       3.7052V             3.8331V             3.2535V
   9.7959ns       3.7052V             3.8331V             3.2535V
   9.8980ns       3.7052V             3.8331V             3.2535V
  10.0000ns       3.7052V             3.8330V             3.2535V
|
```

Figure 54 Timing profile characteristics of an output