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THÈSE POUR OBTENIR LE GRADE DE DOCTEUR DE L'UNIVERSITÉ DE MONTPELLIER

En Electronique

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Unité de recherche : Institut d'Electronique et des Systèmes, UMR CNRS 5214

InP based tandem solar cells integrated onto Si substrates by heteroepitaxial MOVPE

Présentée par Stefano SORESI

Le 1er octobre 2018

Sous la direction de Eric TOURNIE

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UNIVERSITÉ DE MONTPELLIER

Résumé

Titre: Cellules solaires tandem à base de InP intégrées sur substrats Si par hétéro-épitaxie MOVPE

Mots clés: Cellules solaires tandem, III-V/Si, MOVPE, Techno, InP/InGaAs, Jonctions tunnel

Résumé: Cette thèse s'intéresse à l'intégration sur Si de cellules solaires III-V à simple et double jonction par épitaxie en phase vapeur aux organo-métalliques (MOVPE). Les dispositifs photovoltaïques ont été réalisés avec des matériaux accordés sur InP. L'objectif était d'abord d'obtenir des dispositifs performants sur des substrats InP, puis de les intégrer sur une structure avec un paramètre de maille différent, en évaluant les effets sur les performances photovoltaïques. Ceci a nécessité la réalisation et l'optimisation de plusieurs étapes de fabrication.

Tout d'abord, nous avons réalisé une cellule InP à simple jonction, qui peut correspondre à la cellule top dans notre structure tandem. Cela était également nécessaire pour mettre en place un processus de fabrication pour toutes les cellules suivantes. Les conditions de croissance ont été optimisées en profitant des techniques de caractérisation des matériaux telles que la XRD, l'analyse C-V et le SIMS. En optimisant les épaisseurs et les niveaux de dopage des différentes couches du dispositif, ainsi que le procédé en salle blanche, nous avons obtenu une efficacité de conversion de 12.9%, avec un FF de 84.3%. Nous avons démontré que l'utilisation d'une couche fenêtre en AlInAs au lieu de l'InP peut augmenter l'efficacité à 13.5%, malgré une légère réduction du FF (81.4%). La même procédure a ensuite été étendue à la réalisation d'une cellule solaire InGaAs comme cellule bottom du dispositif tandem. Nous avons obtenu un rendement de 11.4% et un FF de 74.5%.

En parallèle, des jonctions tunnels capables de relier électriquement les deux sous-cellules dans un dispositif tandem ont été étudiées. En partic-

ulier, nous avons concentré notre attention sur les conditions de croissance de l'anode de la jonction, qui a été fabriquée en AlInAs et dopée avec le précurseur CBr_4. Les réactions chimiques d'un tel précurseur avec le précurseur de l'Al et l'In nécessitaient une importante réduction de la température de croissance à 540 °C. En déterminant les effets des flux sur la composition et les niveaux de dopage du composé, nous avons obtenu un dopage élevé de $+4\times10^{19}\,cm^{-3}$. En obtenant un niveau équivalent pour la cathode InP:S, nous avons réalisé un dispositif présentant un Jp de 1570 A/cm^2, capable de fonctionner dans des conditions de concentration solaire élevée. En combinant finalement les trois dispositifs présentés dans une cellule tandem, nous avons pu obtenir un rendement global de conversion de 18.3%, avec un FF de 83.9%.

Un template approprié pour l'intégration III-V/Si a été déterminé en testant plusieurs possibilités fournies par différents partenaires. Les caractérisations XRD et AFM ont démontré qu'un template InP/GaP/Si fourni par la société NAsP était la meilleure option. Ceci a été confirmé par la croissance d'une cellule InP à simple jonction sur le template. La techno sur un substrat Si a été rendu possible en déplaçant le contact arrière de la cellule sur la face avant du dispositif, ce qui a nécessité la mise au point d'un ensemble approprié de masques photolithographiques. La réussite de l'intégration des cellules solaires III-V sur Si a été confirmée par le photocourant produit. Celui-ci correspond à environ 60% de la valeur obtenue sur les substrats InP. De plus, les caractéristiques J-V mesurées donnent une tendance de type diode, démontrant la validité de l'approche proposée.

Abstract

Title: InP based tandem solar cells integrated onto Si substrates by heteroepitaxial MOVPE

Keywords: Tandem solar cells, III-V/Si, MOVPE, Processing, InP/InGaAs, Tunnel junctions

Abstract This thesis focuses on III-V/Si integration of single- and dual-junction solar cells by Metalorganic Vapour Phase Epitaxy (MOVPE). The photovoltaic devices were made with materials lattice matched to InP. The goal was to firstly obtain efficient devices on InP substrates and then to integrate them on a structure with a different lattice parameter by evaluating the effects on the photovoltaic performances. This required the realization and the optimization of several manufacturing steps.

Firstly, we realized an InP single junction device, which may correspond to the top cell of our tandem structure. This was also necessary to set up a manufacturing process for all the next cells. The growth conditions were optimized by taking advantage of material characterization techniques such as XRD, C-V profiling and SIMS. By optimizing thicknesses and doping levels of the various layers of the device, as well as the clean room process, we obtained a conversion efficiency of 12.9%, with a FF of 84.3%. We demonstrated that the use of an AlInAs window layer instead of InP may increase the efficiency to 13.5%, despite a slight reduction in FF (81.4%). The same procedure was then extended to the realization of an InGaAs solar cell as the bottom component of the tandem device. We obtained an efficiency of 11.4% and a FF of 74.5%.

In parallel, tunnel junctions able to electrically connect the two subcells in a tandem device were studied. In particular, we focused our attention on the growth conditions of the junction anode, which was made in AlInAs and doped with CBr_4 precursor. The particular chemical interactions that such a precursor has with Al precursor and In required a relevant reduction

of growth temperature to 540 °C. By determining the effects of the flows on composition and doping levels of the compound, we obtained a high doping of $+4\times10^{19}\,cm^{-3}$. By obtaining an equivalent level for the InP:S cathode, we realized a device presenting a J_p of 1570 A/cm^2, able to work under high solar concentration conditions. By finally combining the three presented devices in a tandem cell, we could obtain an overall conversion efficiency of 18.3%, with a FF of 83.9%.

A proper template for III-V/Si integration was determined by testing several possibilities provided by different partners. XRD and AFM characterizations demonstrated that an InP/GaP/Si template provided by NAsP Company was the best option. This was confirmed by the growth of an InP single junction cell over the template. The processing over a Si substrate was made possible by shifting the rear contact of the cell on the front side of the device, which required the development of a proper set of photolithographic masks. The successful integration of the III-V solar cells on Si was confirmed by the relevant produced photocurrent. This corresponds to around 60% of the value obtained on InP substrates. Furthermore, the measured J-V characteristics show a diode-like trend, which demonstrates the validity of the proposed approach.

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And here we are, finally. After three years. Three years that seemed very long some times, and mockingly fast some others. In any case, it is over now. And now, it is time to take stock of the situation. And here they are, Dear Reader; three years of very intensive work compressed into a practical, handy manuscript of about two hundred pages. Don't worry, Dear Reader, I know how it works: probably, you are here just to read these acknowledgements. It is fine, I guess. So let's go, Dear Reader, let's go...

Before starting, I would like to mention that this work was made possible only thanks to the contributions of several laboratories. III-V Lab (and his parents; Nokia Bell-Labs, Thalès and CEA Leti), where most of this thesis has been developed, had of course a primary role. From time to time, the help of external labs such as IES-University of Montpellier, GeePs-Supélec and C2N was crucial to overcome some tricky points. Out of France, this work could take advantage of the several partners involved in the ITN Marie Curie PROMIS[1] project. Such a heterogeneous, multicultural environment was crucial for my personal development and (spoiler alert) the success of this work. Therefore, thank you all for this.

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[1] Postgraduate Research On dilute Metamorphic nanostructures and metamaterials In Semiconductor photonics. Yes, Dear Reader, PROMIS.

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Stefano

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List of acronyms and abbreviations

Acronym	Unit	Description
AFM		Atomic Force Microscopy
ARC		Anti-Reflective Coating
BSF		Back Surface Field
CBE		Chemical Beam Epitaxy
DEZn		Diethylzinc
DIBS		Dual Ion Beam Sputtering
ECV		Electrochemical Capacitance Voltage profiling
EDX		Energy Dispersive X-ray spectrometry
EQE/IQE	%	External (Internal) Quantum Efficiency
FF	%	Fill Factor
HAADF		High Angle Annular Dark Field (-STEM)
ICP		Inductively Coupled Plasma
J_p	mA/cm^2	Peak tunnelling density of current
J_{SC}	mA/cm^2	Short-circuit density of current
MBE		Molecular Beam Epitaxy
MJSC		Multi Junction Solar Cell
MOVPE		MetalOrganic Vapour Phase Epitaxy
N_{eff}	cm^{-3}	Effective doping level
NDR		Negative Differential Region
PECVD		Plasma-Enhanced Chemical Vapour Deposition

Acronym	Unit	Description
PL		Photoluminescence
r_l	$\Omega \cdot cm^2$	Resistivity for low-applied biases
R_{sh}	Ω	Shunt resistance
R_s	Ω	Series resistance
RMS	nm	Root Mean Squared roughness
RSM		Reciprocal Space Mapping
RTA		Rapid Thermal Annealing
sccm		standard cubic centimeters per minute
SEM		Scanning Electron Microscopy
SIMS		Secondary Ion Mass Spectrometry
SQ	%	Shockley-Queisser (efficiency limit)
SR		Spectral Response
TDD	cm^{-2}	Trading Dislocations Density
TEM		Transmission Electron Microscopy
TJ		Tunnel Junction
TLM		Transmission Line Measurement
TM(Al,Ga,In)		Trimethyl(aluminium,gallium,indium)
V_{OC}	mV	Open circuit voltage
XRD		X-Ray Diffraction

Chapter 1

Introduction

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In this chapter, we will present the current context of the photovoltaic research and the motivations that drive this PhD work. After a quick reminder of the main definitions and properties of a generic solar cell, we will focus our attention on III-V multi-junction devices and on their importance in the reaching of high photovoltaic conversion efficiencies. We will then introduce the concept of their integration on Si to reduce the typical high cost of such devices. Brief summaries of the main techniques used and the current state of the art multi-junction devices and III-V/Si integration will allow us to introduce our personal choices about materials and techniques that will be tested in this work. Finally, the main steps of this work and the outline of the next chapters will be presented.

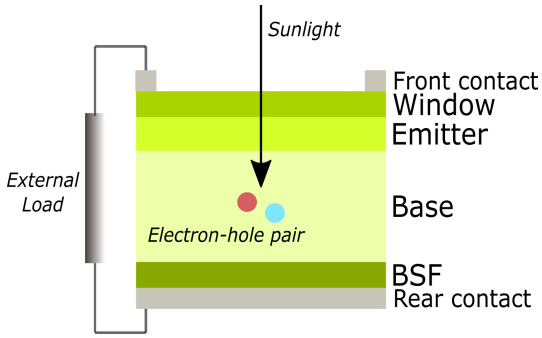


Figure 1.1: The basic structure of a single junction solar cell.

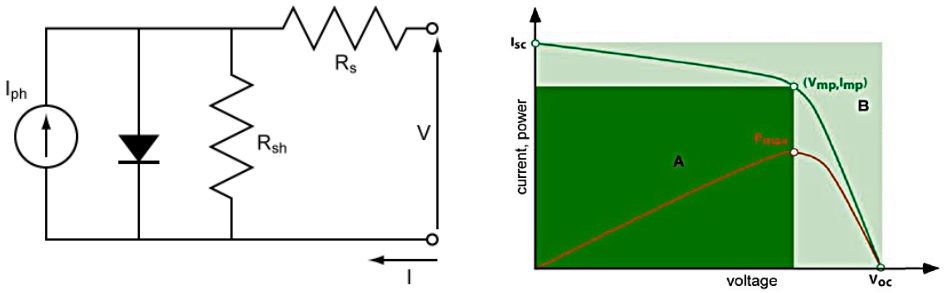
1.1 Single junction photovoltaic: a brief overview

A classical solar cell is basically a p-n junction. As shown in Figure 1.1, a single junction cell can be roughly represented as a four layer structure: the emitter and the base compose the so-called active region, where most of the incident light is absorbed and the electron-hole pairs are generated, the window layer and the back surface field (BSF), at the two ends of the device, act as minority carrier barriers, reducing the front and the rear surface recombination rate, respectively. An exhaustive dissertation on the physics of a solar cell would require too many pages and is, anyhow, outside the scope of this text. In the following subsections, we will limit ourselves to summarizing the most important definitions and concepts that will be used during the whole manuscript and that will justify the most important choices in our research.

1.1.1 An electric system

As mentioned above, a solar cell is nothing but a p-n diode. It is possible to represent its electrical structure with the equivalent circuit shown in Figure 1.2(a): in addition to the diode, we can notice a current source, that represents the photogenerated current J_{Ph} (we can speak equivalently in terms of current I by not normalizing to the surface), a shunt resistance R_{sh}, that represents all losses that tend to short-circuit the cell, and a series resistance R_s that includes the contributions of the materials resistivity and of the ohmic contacts resistance.

In dark conditions, the relation between the current density J and the voltage V of the device is represented by the classical Shockley diode equation:



(a) (b)

Figure 1.2: (a) Electrical equivalent circuit of a solar cell under illumination. (b) I-V characteristic of a cell under illumination (green curve) and relative output power (defined as $P = I \cdot V$, red curve). The intersections of the I-V curve with the x and y axis are respectively named open circuit voltage V_{OC} and short circuit current I_{SC}. The maximum power point has coordinates (V_{mp}, I_{mp}).

$$J = J_S \cdot \left[exp\left(\frac{qV}{nkT}\right) - 1 \right] \tag{1.1}$$

where q is the electron charge, n the ideality factor, k the Boltzmann constant, T the absolute temperature and J_S the dark saturation current density. This last value is very important as it is directly related to the recombination in the material and, consequently, to its quality: in general, a low J_S means a low recombination and, so, a high material quality.

Under illumination, the relation between J and V is also affected by J_{Ph} and the parasitic resistances R_{sh} and R_s. The diode equation thus becomes:

$$J = J_S \cdot \left[exp\left(q \cdot \frac{V - JR_s}{nkT}\right) - 1 \right] + \frac{V - JR_s}{R_{sh}} - J_{Ph} \tag{1.2}$$

From equation 1.2, we obtain the typical shape of a solar cell J-V curve, represented by the green curve in Figure 1.2(b). This figure allows highlighting of the most important parameters of a solar cell: the short circuit current density J_{SC} (I_{SC}), defined as $J(V = 0)$, the open circuit voltage V_{OC}, inversely defined as $V(J = 0)$ and the fill factor FF, defined as $FF = \frac{J_{mp} V_{mp}}{J_{SC} V_{OC}}$, where J_{mp} and V_{mp} are the values of J and V at the maximum power point, respectively (in other words, FF is defined as the ratio between the rectangles A and B in Figure 1.2(b)). By combining these values, it is possible to obtain the definition of the solar cell efficiency η as:

$$\eta = \frac{P_{Out/Max}}{P_{In/Max}} = \frac{J_M \cdot V_M}{P_{In/Max}} = FF \cdot \frac{J_{SC} \cdot V_{OC}}{P_{In/Max}} \tag{1.3}$$

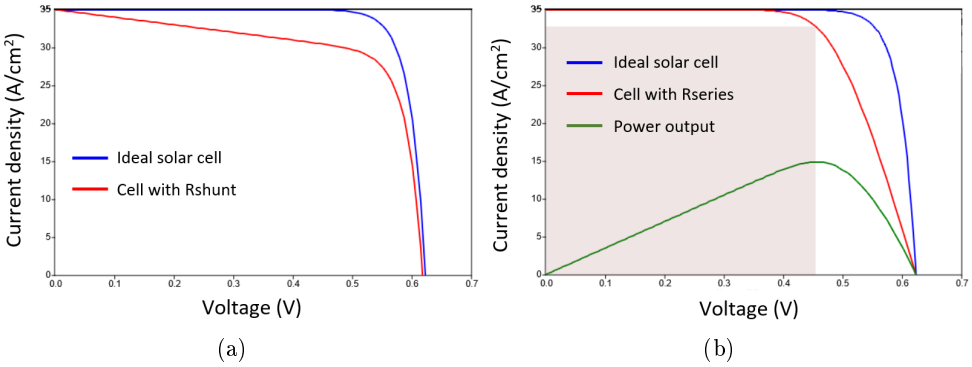


Figure 1.3: (a) Effect of a $100\,\Omega{\cdot}\mathrm{cm}^2$ shunt resistance (red curve) on an ideal cell (blue curve). (b) Effect of a $3\,\Omega{\cdot}\mathrm{cm}^2$ series resistance (red curve) on an ideal cell (blue curve). Both from pveducation.org.

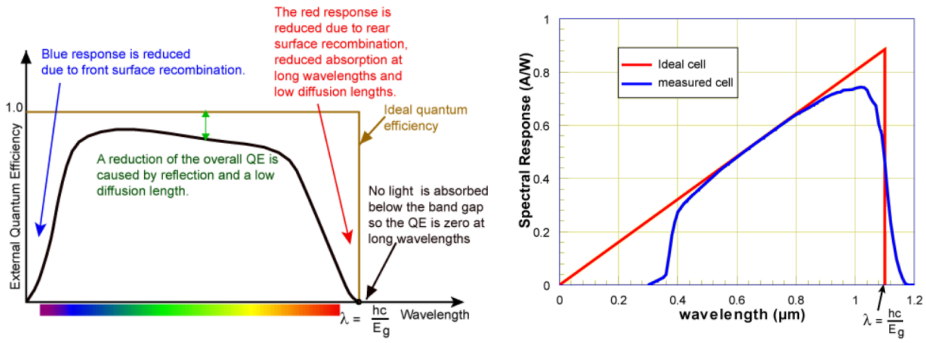
Under standard conditions of 25 °C temperature and AM1.5G solar spectrum[1], the power density $P_{In/Max}$ corresponds to $0.1\,\mathrm{W/cm}^2$.

It is important to evaluate the impact of the parasitic resistances on the solar cell behaviour. An ideal cell requires that $R_{sh} = \infty$. A decrease in R_{sh} means an increase of recombination current and so a decrease in V_{OC}. The impact of a low R_{sh} is particularly severe for low voltages and light concentration. On the other hand, R_s should be as low as possible, ideally 0. A high R_s can reduce the value of J_{SC}. It also affects the J-V curve shape in correspondence of V_{OC}, although it does not directly influence this value, especially at high light concentration. Both resistances have a high impact on FF. These considerations are summarized in the Figure 1.3(a) and (b).

1.1.2 Quantum Efficiency and Spectral Response

A common way to characterize the behaviour of a cell is to measure its Quantum Efficiency (QE). It is defined as the ratio of the number of carriers collected by the cell to the number of photons of a given energy incident on it and it is usually given as a function of the incident wavelength λ. As shown in Figure 1.4(a), an ideal cell should have an unitary QE for $\lambda < \lambda_g = \frac{h\,c}{E_g}$, where h is the Planck constant, c the speed of light in vacuum and E_g the lowest energy gap in the cell. Usually, the QE is measured starting

[1] The solar spectrum can be given under different standard air mass (AM) conditions: AM0 (spectrum out of atmosphere, corresponding to the 5800 K black body emission, typical for space applications), AM1.5G (global spectrum under one atmosphere, considering a solar zenith angle of 48.2%, typical for terrestrial applications in Europe, China, Japan and USA) and AM1.5D (like the previous, but considering only direct radiation, typical for high solar concentrations).



(a) (b)

Figure 1.4: (a) Example of an EQE curve. The most relevant limiting factors are indicated. (b) Example of a Silicon cell SR curve (blue) compared to an ideal cell (red). From pveducation.org.

from $\lambda = 350\,\mathrm{nm}$, as the incident power is too low for higher energies. By evaluating the discrepancy from unity for a given λ, it is possible to determine the impact of the limiting factors of the corresponding layer. The most common limiting factors are reported in Figure 1.4(a). Two kinds of QE can be extracted: the external QE, or EQE, which considers all the incident photons N_{ph}; and the internal QE, or IQE, which considers only the photons not lost by transmission T and reflection R. The two are connected by the simple relation:

$$EQE = \frac{J_{SC}}{N_{ph}} = (1 - T - R) \cdot IQE \tag{1.4}$$

In this work, we will consider EQE characteristics only.
It is also possible to extract J_{SC} from an EQE curve from the relation:

$$J_{SC} = q \cdot \int \Phi_{ph}(E)\, QE(E)\, dE \tag{1.5}$$

where $\Phi_{ph}(E)$ represents the spectral photon flux density.

A concept very similar to the EQE is the Spectral Response (SR). It is defined as the ratio of the current generated by the solar cell to the power incident on it. The SR shape of a typical Silicon cell is shown in Figure 1.4(b), together with the ideal one. As this value is easier to measure than the EQE, a typical cell characterization method consists in measuring its SR and then extracting the EQE from the relation:

$$EQE = \frac{h\,c}{q\,\lambda} \cdot SR \tag{1.6}$$

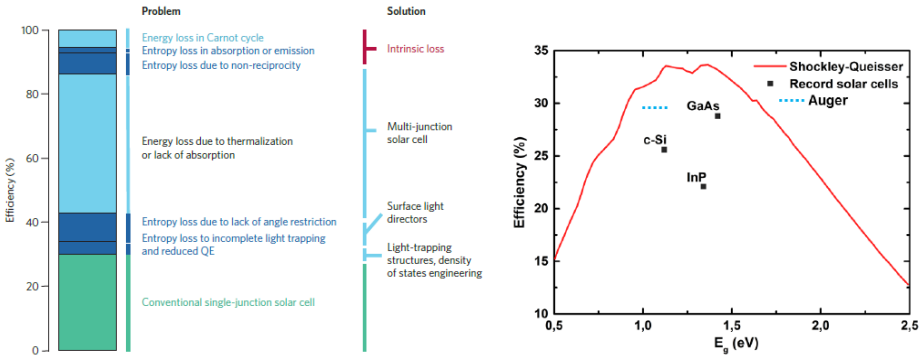
1.1.3 The Shockley-Queisser efficiency limit

The maximum efficiency that can theoretically be reached by a single junction solar cell as the one shown in Figure 1.1 is affected by multiple factors. The first of them comes directly from the second law of thermodynamics: as with every heat engine, the maximum energy conversion efficiency of a cell is limited by the Carnot rule [1]:

$$\eta_{max} = 1 - \frac{T_e}{T_s} \tag{1.7}$$

where T_e and T_s correspond to the Earth atmosphere and to the Sun surface temperatures, respectively (or, to the cold and to the hot reservoirs). Using the typical values of 300 K for T_e and 5800 K for T_s, we obtain that $\eta_{max} \sim 95\,\%$. A more precise study demonstrated that this value should actually be around 93 %, due to the fact that the emission of radiation by the sun is an irreversible process [2]. Another intrinsic (and unavoidable) limit comes from the Kirchoff law: since the solar cell is not a perfect black body, it will spontaneously re-emit part of the incident radiation, thus reducing its efficiency [3]. Despite these two intrinsic limits, most losses come from factors whose influence can theoretically be reduced, as shown in Figure 1.5(a). One of these factors is the difference between the absorption and the emission angles in the cell, which can be limited by maximizing the sunlight concentration. However, the most relevant limiting factor is the mismatch between the solar spectrum and the photons absorption potential of the single absorber material: for a given E_g, the carriers generated by the more energetic photons will lose part of their energy by thermalizing to the conduction band edge via interactions with lattice phonons; on the other hand, the photons with an energy lower than the bandgap will simply not be absorbed. A more detailed analysis on all of these limiting factors can be found in [4, 5].

What remains after considering all the above mentioned factors, is the so-called Shockley-Queisser (SQ) limit [6]. The trend is shown in Figure 1.5(b), together with current world records for some of the most used photovoltaic single junction technologies. This parabolic-like trend is easily understood as a net balance between the decrease of the absorption and thermalization losses when increasing the bandgap. An equivalent explanation takes into account the fact that V_{OC} increases with E_g, as the recombination current falls at high E_g, while J_{SC} increases as E_g decreases, since more absorption means more photogenerated carriers. As η is proportional to both V_{OC} and J_{SC} (equation 1.3), it should present a parabolic-like trend as a function of E_g. Figure 1.5(b) shows that η_{max} for a generic single junction cell can be



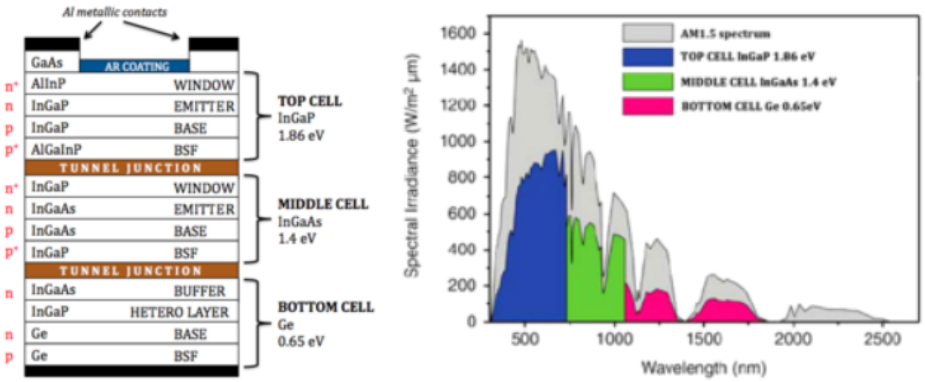
(a) (b)

Figure 1.5: (a) The main losses in a single junction solar cell that contribute to the SQ limit. Dark blue portions are related to the entropy losses, while light blue relate to the energy losses. The right column lists some possible solutions to the limiting factors. From [4]. (b) SQ limit for a single junction solar cell as a function of the absorber E_g. The dots indicate the actual efficiency records for some typical cells. It is important to notice the discrepancies of the real records from the theoretical ones. From [8].

around 33%, however we can notice that, despite the parabolic trend, the whole 1.1-1.5 eV range can guarantee an efficiency of $\sim$32%. It is therefore easy to understand why the most common solar cells are made with semiconductors with similar E_g such as c-Si, GaAs, InP and CdTe. The current efficiency world record for a single junction solar cell, obtained by Alta Devices with a GaAs-based device [7], is 28.8%.

1.2 Beyond the SQ limit: the Multi-junction

We saw in the previous paragraph how the SQ limit affects η_{max} of a single junction solar cell. We also saw from Figure 1.5(a) that the most limiting factor is the combination of carrier thermalizing and absence of absorption for a given E_g. This problem can be overcome by the use of multi-junction solar cells (MJSCs) [9–11]. The principle is very intuitive: by stacking multiple cells (and so, multiple absorber layers) from the highest to the lowest E_g (from the top to the bottom of the structure), it is possible to minimize the losses, as the top cell(s) will reduce the thermalizing and the bottom cell(s) the missed absorption. Every single cell is calibrated to a certain wavelength, so the whole device will guarantee a better coverage of the solar spectrum. Figure 1.6(a) shows the structure of such a MJSC while Figure 1.6(b) shows its spectrum coverage. By increasing the number of subcells up to 36, an efficiency limit of 72% can be reached [2]; this value agrees with



(a) (b)

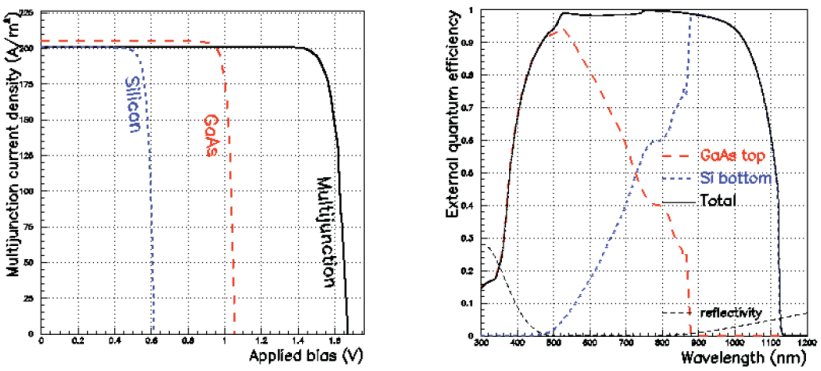
Figure 1.6: (a) Structure of a typical InGaP/(In)GaAs/Ge triple junction solar cell. Such a cell guarantees one of the best performances for a multi-junction device. (b) Coverage of the solar spectrum with the mentioned cell. This is a very generic principle for every N-junction device. Both from [11].

the one showed in Figure 1.5(a). Another study affirmed that, by combining an infinite stack with high solar concentration, an efficiency of 86.6% can be reached [12]. Of course, each additional subcell guarantees a higher overall efficiency (although the impact becomes less and less relevant), but it also increases the technical problems of the realization and the manufacturing costs. In general, this approach is advantageous up to four junctions per device, whereas the use of five or more junctions is, at least, questionable [13].

1.2.1 Electrical properties and current matching

As shown in Figure 1.6(a), a multi-junction solar cell is basically a stack of series-connected single junction cells, the definitions and properties given in the paragraphs 1.1.1 and 1.1.2 applying to each of them. These definitions are the same also for the whole device. Some of these parameters can be directly extracted from the single cell ones. In fact, being N series-connected cells, the overall V_{OC} will be simply given by the sum of all the single V_{OC}, while the overall J_{SC} will coincide with the lowest one.

Considering a system of two cells where J_{SC} is limited by the lower one, it is possible to reduce the upper cell thickness: in this way, the top cell J_{SC} will be reduced (less absorbed photons), whereas the bottom cell one will be increased (more incident photons). We speak of *current matching* when the top cell thickness allows that the two J_{SC} be equal (maximizing the overall contribution) [14]. The same process is not viable in the opposite situation, which is unfortunately the most common one (in general, the higher the bandgap, the lower the generated current should be). Since



(a) (b)

Figure 1.7: (a) J-V characteristics under light of the two components of a dual junction solar cell plus the overall characteristic. While the whole V_{OC} is given by the sum of the single ones, the total J_{SC} is limited by the lowest one. (b) EQE characteristic of the same cell. Both the single components and the overall effect are showed. Both from [15].

the FF is proportional to the top cell thickness [13], the current matching negatively affects this value; because of its effect on J_{SC}, it usually increases the overall η of a MJSC. This information is summarized in the image 1.7(a).

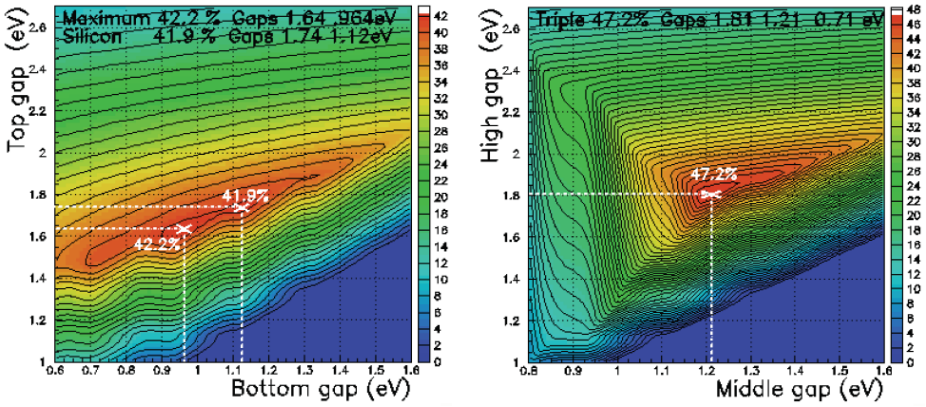
Although it is not possible to determine the overall EQE from the single cells behaviors, it is easy to understand how the contributions of multiple cells can increase the coverage of the whole solar spectrum, as shown in Figure 1.7(b).

1.2.2 Choosing the right bandgaps

The literature presents many different studies on the evaluation of the best bandgaps for a given number of junctions. Different results can be obtained because the number of parameters that affect the calculation is high: the number of junctions itself (starting from 3 junctions every new one adds a degree of freedom), the properties of the absorber material, the current matching, the concentration intensity, etc.

An interesting result was presented by Connolly *et al.* [15] (considering an AM1.5G solar spectrum without light concentration,) and is shown in Figure 1.8: considering a 2J (a) device, the presence of a typical Si bottom cell only decreases the maximum theoretical efficiency from 42.2% to 41.9%; whereas, in a 3J device (b), a 0.71 eV bottom cell (for example, in Ge or GaSb) allows to reach a 47.2% efficiency.

A more general result was obtained by Phillips *et al.* by using the EtaOpt



(a) (b)

Figure 1.8: Maximum radiative efficiencies for an AM1.5G solar spectrum for (a) a 2J cell, where the value is 42.2% (E_g of 1.64 and 0.964 eV) and the Si-based tandem efficiency maximum is 41.9% (E_g of 1.74 and 1.12 eV); and (b) a 3J cell, where the maximum efficiency is determined as a function of top and middle bandgap subcells (the bottom one is fixed). This maximum is 47.2% (E_g of 1.81, 1.21 and 0.71 eV). Both from [15].

software from the Fraunhofer Solar Institute [16]: Tables 1.1 to 1.3 show the optimal bandgap energies combinations for one- up to six-junction solar cells under the 1-sun AM0, AM1.5G 500-suns AM1.5D spectra, respectively.

A calculation based on ideal bandgaps gives the ideal efficiency. The crystalline quality of the materials however has a very high influence on the efficiency since any defect will lead to carrier recombination. As shown by Figure 1.9 (discrepancies from Figure 1.8 are due to a different spectrum and concentration considered and to the freedom in the choice of the bottom cell in the 3J cell), it is very complicated to obtain the whole set of optimized E_g at the same lattice parameter, despite the high flexibility of ternary and quaternary III-V compounds. Consequently, two approaches are possible [17]: keeping the same lattice constant, moving away from the optimal E_g [18, 19], or combining different lattice parameters by techniques such as metamorphic growth [20, 21] or wafer bonding [22–25] to maintain the right bandgaps. All the results that are currently most important were obtained with this last approach.

1.2.3 State of the art

The wide possibility of materials combinations (even without considering the numerous II-VI semiconductors), combined with the realization techniques

Subcell	1J	2J	3J	4J	5J	6J
1	1.24 eV	0.89 eV	0.74 eV	0.65 eV	0.64 eV	0.59 eV
2	–	1.58 eV	1.18 eV	0.99 eV	0.91 eV	0.83 eV
3	–	–	1.82 eV	1.40 eV	1.21 eV	1.07 eV
4	–	–	–	1.99 eV	1.60 eV	1.36 eV
5	–	–	–	–	2.15 eV	1.73 eV
6	–	–	–	–	–	2.26 eV
Efficiency	30.3%	42.2%	48.5%	52.3%	54.8%	56.7%

Table 1.1: Optimal bandgap energies combinations for one- up to six-junction solar cells under 1-sun AM0 spectrum. From [16].

Subcell	1J	2J	3J	4J	5J	6J
1	1.34 eV	0.93 eV	0.93 eV	0.72 eV	0.70 eV	0.51 eV
2	–	1.60 eV	1.37 eV	1.11 eV	1.01 eV	0.79 eV
3	–	–	1.90 eV	1.49 eV	1.33 eV	1.13 eV
4	–	–	–	2.00 eV	1.67 eV	1.41 eV
5	–	–	–	–	2.14 eV	1.73 eV
6	–	–	–	–	–	2.19 eV
Efficiency	33.8%	45.9%	51.8%	55.6%	57.9%	59.2%

Table 1.2: Optimal bandgap energies combinations for one- up to six-junction solar cells under 1-sun AM1.5G spectrum. From [16].

Subcell	1J	2J	3J	4J	5J	6J
1	1.12 eV	0.93 eV	0.69 eV	0.51 eV	0.54 eV	0.53 eV
2	–	1.57 eV	1.17 eV	0.96 eV	0.92 eV	0.79 eV
3	–	–	1.74 eV	1.37 eV	1.21 eV	1.11 eV
4	–	–	–	1.88 eV	1.56 eV	1.38 eV
5	–	–	–	–	2.03 eV	1.69 eV
6	–	–	–	–	–	2.13 eV
Efficiency	40.3%	53.8%	61.0%	65.1%	67.5%	69.1%

Table 1.3: Optimal bandgap energies combinations for one- up to six-junction solar cells under 500-suns AM1.5D spectrum. From [16].

reported in the previous paragraph and the possibility of concentrating the sunlight, gives rise to a series of not-always-comparable efficiency records. In this section, we will report relevant results, obtained under very different conditions. A recent, more exhaustive review can be found in [7].

Although the best efficiencies are usually obtained under high solar con-

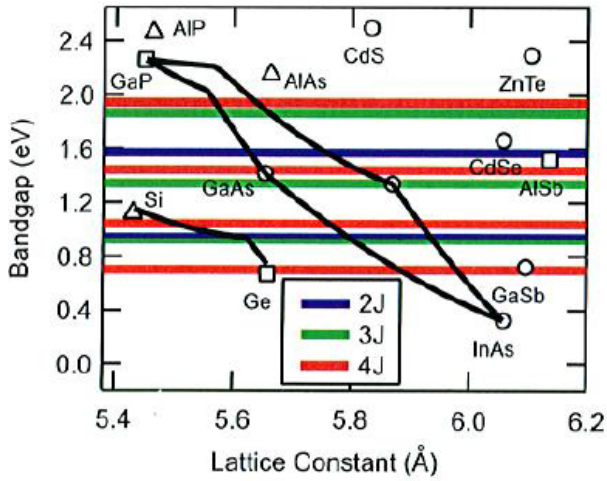


Figure 1.9: Energy gap as a function of the lattice parameter for some typical semiconductors. The optimal values of E_g for 2J, 3J and 4J cells are shown. The considered spectrum is the 500× concentrated AM1.5D. From [20].

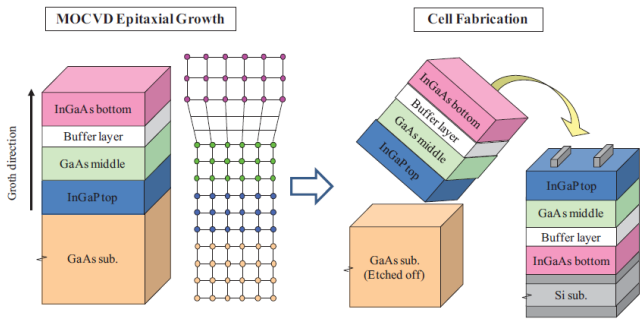


Figure 1.10: Growth and fabrication of the metamorphic 3J device proposed by Sharp [26].

centration, it is important to report a couple of very impressive results obtained under 1 Sun concentration, or 1×: the first one, of 31.6%, was obtained by Alta Devices with a monolithic $In_{0.49}Ga_{0.51}P/GaAs$ dual junction cell [27]. This device was grown in an inverted structure, then stuck on a flexible handle and finally its GaAs substrate was lifted away. Sharp obtained a 37.9% efficient device by adding a third bottom cell made by metamorphic growth of $In_{0.31}Ga_{0.69}As$ (1 eV) on the same structure and by reporting the cell on a Si substrate by metal bonding, as presented in Figure 1.10 [26].
The same device tested by Sharp under 302× concentration reached an efficiency of 44.4% [28]. Another relevant result obtained under concentration (234×) was published by NREL [29]: in this case, the usual InGaP/GaAs top couple was combined with two InGaAs bottom cells in a 4J (details on the two bottom cells are not given). The obtained efficiency was 45.7%.

Structure	η (%)	Intensity (suns)	Institution	References
InGaP/GaAs// InGaAsP/InGaAs	46.0 ± 2.2	508	Soitec/CEA	[30]
InGaP/GaAs/ InGaAs/InGaAs	45.7 ± 2.3	234	NREL	[29]
InGaP/GaAs/ InGaAs	44.4 ± 2.6	302	Sharp	[28]
InGaP/GaAs/ InGaNAs	44.4	942	Solar Junction	[32]
InGaP/(In)GaAs/ InGaAs	42.6	327	NREL	[33]
InGaP/(In)GaAs/Ge	41.6	364	Spectrolab	[34]
InGaP/InGaAs/Ge	41.1	454	Fraunhofer ISE	[35]
InGaP/GaAs/ InGaAs	37.9 ± 1.2	1	Sharp	[26]
InGaP/GaAs	31.6 ± 1.5	1	Alta Devices	[27]

Table 1.4: Some relevant current records for multi-junction solar cells.

The actual, absolute world record for photovoltaic was obtained by Soitec/CEA with a 4J device [30]: the structure, already presented in [31], was realized by growing an inverted InGaP/GaAs structure on GaAs and an $In_{0.84}Ga_{0.16}As_{0.31}P_{0.69}/In_{0.53}Ga_{0.47}As$ structure on InP. The first structure was then atomically bonded onto the second one and the GaAs substrate removed. The device presents a 46% efficiency at 508× concentration.

The above mentioned results, together with some other relevant ones, are reported in Table 1.4.

It is remarkable that all the above mentioned devices are characterized by an $In_{0.49}Ga_{0.51}P/GaAs$ tandem cell: as showed by Figure 1.9, the respective bandgaps of 1.88 and 1.42 eV make it very interesting for 3J and 4J photovoltaic. This is also the reason for the primary importance of GaAs-lattice matched materials in multi-junction photovoltaic. Unfortunately, the GaAs lattice parameter does not present an equivalent variety of low bandgap materials; the only exceptions are Ge (0.67 eV) and GaInNAs(Sb). This lack can be overcome by the use of InP-lattice matched materials such as $In_{1-x}Ga_xAs_yP_{1-y}$, $(Al_xGa_{1-x})_{0.47}In_{0.53}As$ and $In_{0.53}Ga_{0.47}As$ (on the contrary, this lattice parameter does not present high bandgap materials except $Al_{1-x}Ga_xAs_ySb_{1-y}$): it is not a coincidence that the current record was obtained by combining these two families.

1.2.4 Reducing the costs

The overview presented above, although not exhaustive, well emphasizes a very important point: binary, ternary and quaternary III-V compounds are needed to reach photovoltaic efficiencies above the SQ limit. Unfortunately, these materials are expensive and rare when compared to Silicon, which is still currently the leading material in photovoltaics. As a consequence, the research on this kind of devices not only aims at increasing the efficiency, but also at reducing the impact of these drawbacks. The two most promising ways were already mentioned in the previous section. The first one consists in concentrating the sunlight [36] through the use of optical lenses (for low concentrations) and waveguides (for high and ultra-high concentrations). Such an approach allows in fact to reduce the dimensions of the device, as the incident power has a higher density [37], and, consequently, the amount of expensive materials. Furthermore, by concentrating the sunlight, the cell efficiency should increase in consequence, since the photogenerated current is proportional to the number of incident photons and the voltage increases logarithmically with the current. As also the incident power increases with the light concentration, the net effect on η, extracted from the equation 1.3, is a logarithmic increase with the concentration.

The second approach consists of integrating the devices on cheaper substrates. Although other materials were tested in the literature [27], using Silicon substrates is of prominent importance. Not only multiple integration techniques are now well developed, Silicon can also be used as a 1.1 eV active solar cell in a multi-junction device [38]. In the next sections, we will present some of the most relevant techniques for the III-V/Si integration and some relevant photovoltaic results.

To conclude, it is important to mention the fact that the two mentioned methods are not incompatible: therefore, it is possible to exploit both for the same kind of devices.

1.3 Silicon integration

The many qualities of III-V compounds (ability to efficiently emit and detect light, very high carrier mobilities, the possibility of lattice parameter and bandgap engineering [39]) make them excellent materials for photovoltaic application (and not just this: we can also think about lasers, detectors for optical communication, light-emitting diodes etc.). At the same time, they present important limits such as the use of rare materials, expensive processes and complex fabrication techniques; hardly compatible with industrial solar cells size and throughput. These limits introduce restriction to the specific market of III-V cells (basically, only space applications justify this approach). In contrast, the absence of these limits makes Silicon the leading material in

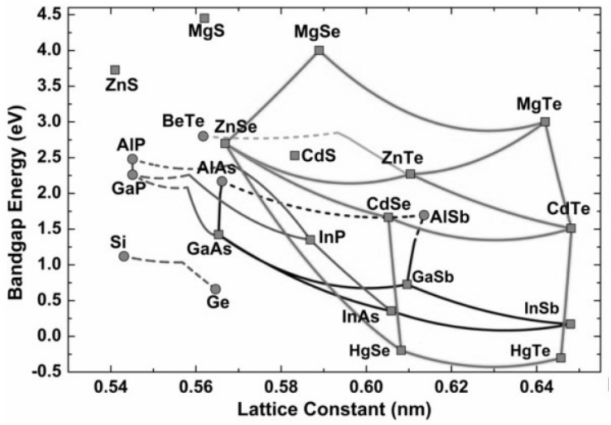


Figure 1.11: The typical energy gap - lattice parameter graph for the most common III-V, IV and II-VI semiconductors.

PV: low cost, abundance, strong industry background and an excellent heat conductivity are important assets for large scale production.

It is thus reasonable to think of taking advantage of the complementary qualities of these two families in order to obtain high efficiency and low cost devices. While III-V layers will act as top cells, Si can act at the same time as cheap substrate and, in certain cases, as bottom cell.

Unfortunately, important issues make the III-V/Si integration difficult. The first one is the high lattice mismatch: as deduced from Figure 1.11, it is $\sim 4\%$ between Si and GaAs and $\sim 8\%$ between Si and InP. When growing III-V solar cells on Si, this lattice mismatch, showed in Figure 1.12(a), will induce the generation of defects [41] that act as recombination centres reducing the carrier mobility and impacting the electrical performances of the devices. Furthermore, the Si thermal expansion coefficient is lower than that of GaAs and InP [42], as showed in Figure 1.12(b). The cooling of the III-V materials on Si can produce cracks. Last but not least, is the fact that III-V materials are polar and the Si is not: it means that their interface can generate antiphase domains, or APDs [43], in the very common case where a (001) Si substrate presents monoatomic steps [44], as shown in Figure 1.12(c). When it happens, III-III and V-V bonds are formed, resulting in antiphase boundaries (APBs). This kind of defects has a deleterious effect on the electrical behavior of the device.

A maximal trading dislocation density (TDD) of $\sim 10^6\,\mathrm{cm}^{-2}$ is acceptable to produce high quality III-V/Si solar cells [40], as in this case the average spacing between them is comparable with the carrier diffusion length, as shown in Figure 1.12(d). In general, the increase of TDD affects the V_{OC} of the device: considering for example GaAs, a TDD increase from 10^6 to $10^8\,\mathrm{cm}^{-2}$ results in a $\sim 100\,\mathrm{mV}$ drop for the V_{OC} [40].

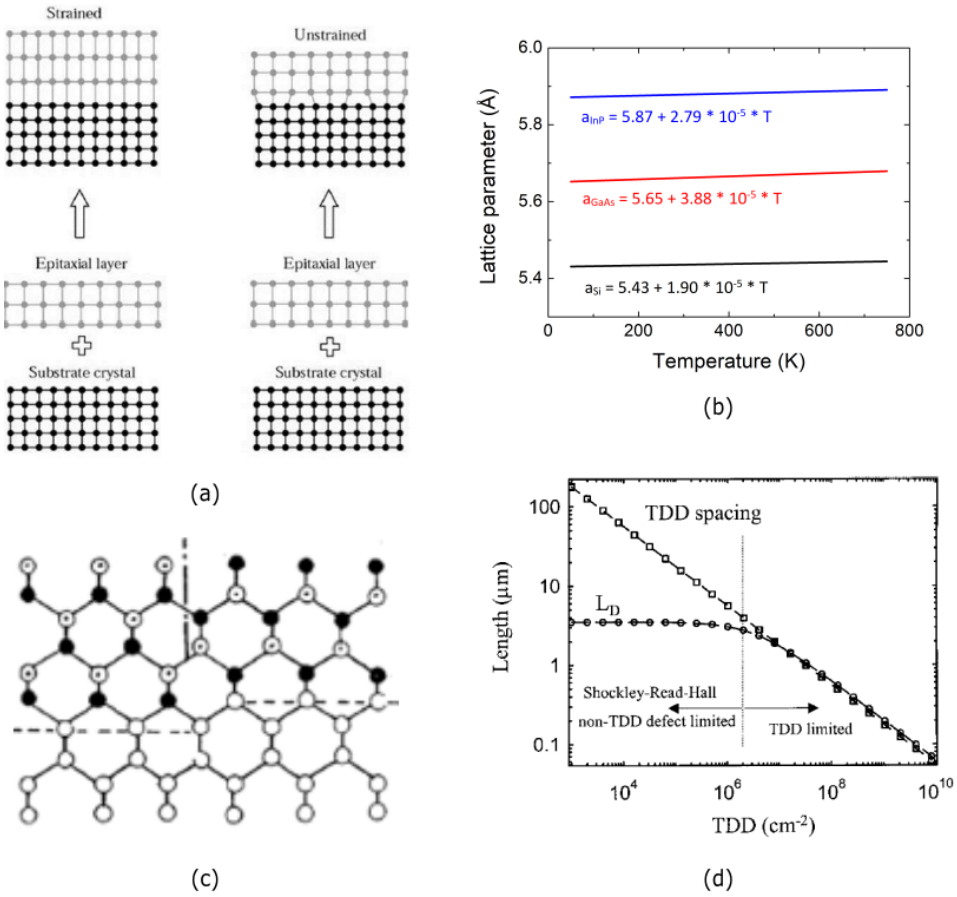


Figure 1.12: (a) Heteroepitaxy of a layer whose lattice parameter is bigger than the substrate one (typical III-V/Si case): the epitaxial layer can compressively strain its lattice parameter to match the one of the substrate (left) or relax to its typical structure, forming dislocations (right). (b) Thermal evolution of Si, GaAs and InP lattice parameter. The mismatch increases slightly with temperature. (c) Formation of antiphase domains at a III-V/Si interface due to the presence of a monoatomic step in the Si substrate. (d) Effect of the average trading dislocation spacing on the minority carriers diffusion length in a typical III-V semiconductor: for densities higher than $10^6\,\mathrm{cm}^{-2}$, L_D is limited by the recombination. From [40].

When integrating III-V materials on Si, it is thus essential to deal with these limits and to reduce the deleterious defects as much as possible.

In the following paragraphs, we will summarize some of the most important III-V on Si integration techniques and some of the most relevant photovoltaic results that these techniques have allowed.

1.3.1 III-V/Si integration

The aforementioned limits (lattice mismatch, thermal mismatch and polar/non polar interface) are the challenging points faced in III-V/Si integration. The two possibilities to obtain such integration consist of an epitaxial approach, where the III-V layers are directly grown on a Si substrate, and a non-epitaxial approach, where III-V materials are grown on a III-V substrate and subsequently integrated on Si. In this section, we will give an overview of these two paths, as well as their principal advantages and limits.

1.3.1.1 Epitaxial approach

The epitaxial approach implies to directly face the three main integration issues. The APDs can be reduced or even eliminated by using offcut Si substrates (this solution is valid for both GaAs and InP technologies [45–48]) and/or specific Silicon substrate preparations before III-V growth, while the high TDD and stress caused by lattice and thermal mismatch are much more serious limits.

The most intuitive and immediate way to integrate GaAs or InP on Si is the direct growth [49–51]: since the typical TDD ($\sim 10^9$-$10^{10}\,\mathrm{cm}^{-2}$) is too high for most applications, it is essential to develop methodologies to decrease this value. Focusing our attention on InP, we can find in literature multiple proposals to reduce the total amount of dislocations: Aspect Ratio Trapping [52], Epitaxial Lateral Overgrowth [53], and low temperature ($\sim 300\,^{\circ}\mathrm{C}$) InP nucleation [45, 54, 55]. A high-temperature post growth annealing ($\sim 700\,^{\circ}\mathrm{C}$) is also often performed to decrease the TDD. Basically, the two approaches that characterize these techniques are the confinement of TDs at the III-V/Si interface and the shift of the same TDs in order to make them collide and cancel each another. This means that the zone close to interface will be highly defective: although these techniques undoubtedly reduce the total TDD, they hardly guarantee a value suited to photovoltaics ($\sim 10^{-6}\,\mathrm{cm}^{-2}$). Further improvements to these technologies are, therefore, necessary.

A promising solution to reduce the high TDD between Si and III-V (particularly InP) is to include a buffer layer between them. If the buffer mechanical properties are intermediate between those of Si and of the layers that have to be integrated, then the effects of the abrupt change of lattice parameter can be limited. This is valid also for the polarity problems if the substrate is not offcut. Of course, if we want to use Si as a bottom cell, it is necessary to find a transparent buffer, compared to the 1.12 eV bandgap of Si.

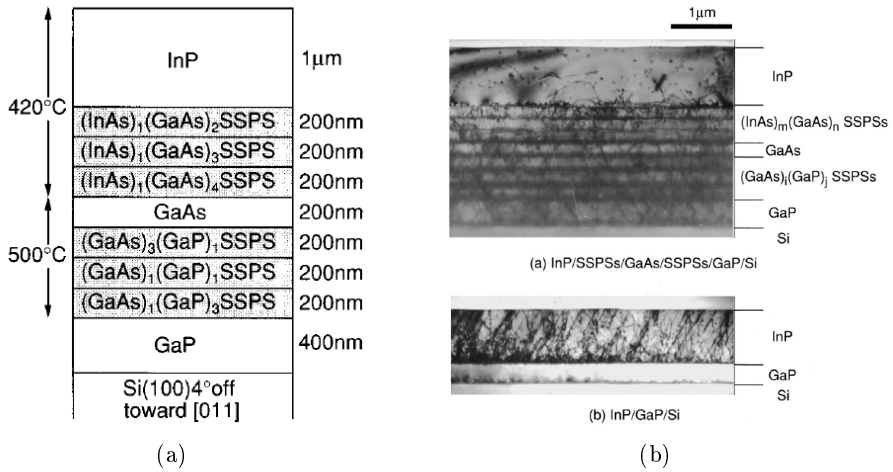


Figure 1.13: (a) Schematic drawing of an InP/SSPSs/GaAs/SSPSs/GaP/Si structure grown by molecular beam epitaxy to reduce the TDD in InP. (b) Top: cross-sectional TEM image of the described structure. Bottom: cross-sectional TEM image of an InP/GaAs/Si structure. A visual comparison of the two pictures well explains the beneficial effect of the two superlattices. Both from [56].

The high lattice mismatch between InP and Si allowed researchers to test multiple types of buffer layers. A very intuitive possibility is to use materials whose lattice parameter is approximately in the middle between InP and Si, such as GaAs [57–59] and Ge [60] (although its 0.67 eV E_g prevents the use of Si as a bottom cell). Although a buffer thickness of $\sim 1\,\mu$m should be indicated to reduce the TDD, the cited papers obtained more or less the same results with thinner layers of few hundreds of nm. Sugo *et al.* [59] reached a TDD of 8×10^6, the right order of magnitude for photovoltaic applications. Another principle is to use GaP buffer layers [58, 61]: in this case, the quasi lattice match between Si and GaP allows one to completely split the two problems of the formation of APDs and of the trading dislocations. In fact, while the APDs can appear only at the GaP/Si interface, the dislocation will be formed at the InP/GaP interface. Since the lattice mismatch of InP with GaP is basically the same obtained with Si, it can be necessary to add more structures to limit the TDD. A good solution can be given by the use of strained superlattices. Relevant attempts were made by Crumbaker *et al.* [62], with four strained $In_xGa_{1-x}P/In_yGa_{1-y}P$ superlattices (reaching a final TDD of $10^8\,cm^{-2}$), and by Samonji *et al.* [56], with an InP/SSPSs (strained short-period superlattices)/GaAs/SSPSs/GaP/Si structure, presented in Figure 1.13, where the two SSPS were made by $(InAs)_m(GaAs)_n$ and $(GaAs)_i(GaP)_j$, respectively. In this last study, the TDD was about $10^7\,cm^{-2}$, with a total buffer thickness of $2.8\,\mu$m. A different, more exotic approach for the III-V/GaP integration is given by the use of dilute nitrides

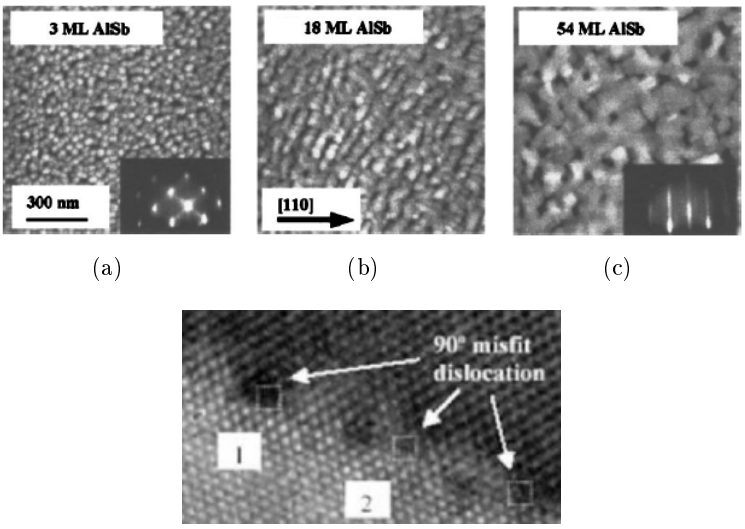


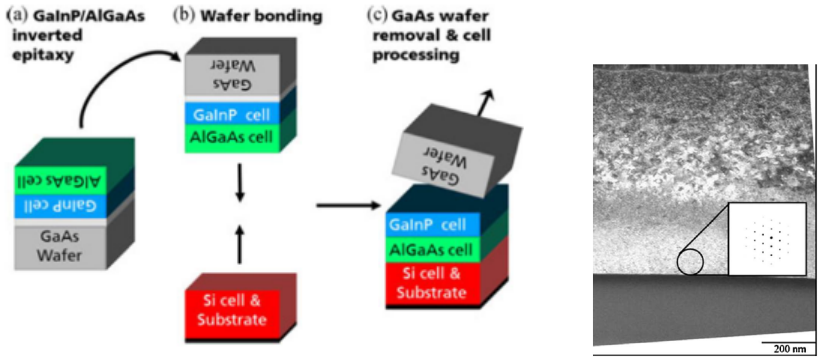
Figure 1.14: (a-c) AFM images showing surface structure after 3, 18 and 54 monolayers of AlSb deposition on Si, respectively. (a) and (c) show RHEED images for the corresponding growths as well. From [67]. (d) Cross-sectional TEM image of the interface between AlSb (top) and Si (bottom). From [64].

such as Ga(NAsP) [63].

Finally, an innovative solution can be given by the use of III-Sb materials, such as AlSb and GaSb [64–66]. As reported by Balakrishnan *et al.* [67], the growth of AlSb on Si is characterized by an efficient strain relaxation in the very first few monolayers (Figure 1.14) Up to now, this approach was tested only for the realization of GaSb-based device for Silicon Photonics [68–70]. However, the possibility of growing structures lattice matched on InP and GaAs is still open.

1.3.1.2 Non-epitaxial approach

Although the above mentioned epitaxial techniques undoubtedly represent the best solution for an industrial integration, they are affected by the presence of growth defects. This fact justifies a parallel research in non-epitaxial techniques such as wafer bonding and mechanical stacking. Ideally, two different solids such as InP and Si can be bonded at room temperature by pressing them together because of the formation of Van der Waals bonds between the two surfaces. In order to obtain such a bonding, some conditions are mandatory for the two surfaces put in contact: they have to be very smooth (a roughness inferior to 1 nm [73]), mirror polished and ideally



(a) (b)

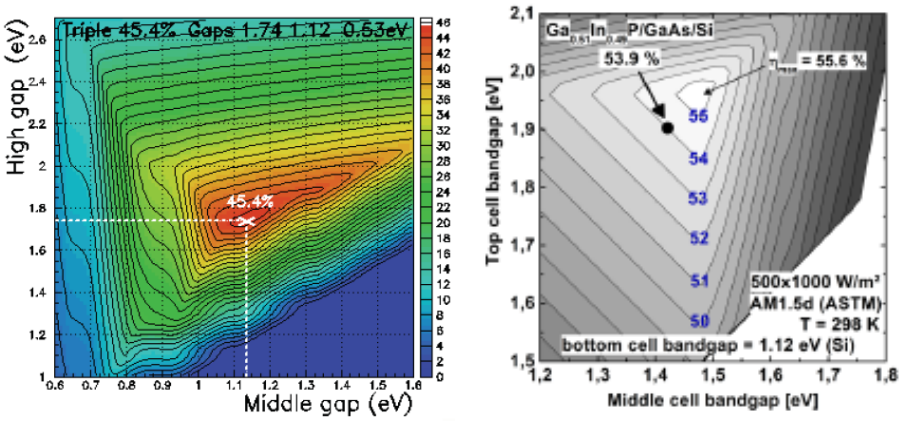
Figure 1.15: (a) Principle of wafer bonding between a III-V layer and Si substrate. From [71]. (b) Cross-sectional TEM image of an InP layer bonded to a Si substrate. Inset, selected-area diffraction image indicating that the InP adjacent to the bonded interface (within 200 nm) is crystalline. From [72].

clean. The originated Van der Waals bonds suppress the mismatch issues, allowing the growth of the III-V layers at their own lattice parameter. The bonding can be implemented by using techniques such as plasma treatment [73, 74] or hydrogen-induced exfoliation [75], that allow the formation of strong covalent bonds between III-V and Si [72]. Intermediate polymers like Benzocyclobutene (BCB) or oxides like SiO_2 can also be used to connect the different structures (taking care not to introduce electrical resistances or optical absorptions at the interface). Since this approach, unlike the previous one, requires the use of a III-V substrate (as shown in Figure 1.15(a) from [71]), it is mandatory that this last one be recovered to guarantee the sustainability of the process. Figure 1.15(b) from [72] shows a cross-sectional TEM image of an InP layer bonded to a Si substrate, and it is possible to notice the integrity of the InP layer at the interface. Such a bonding allowed the realization of an InGaAs based solar cell with an efficiency of 13.6%.

As this technique requires very long, careful surfaces preparation, an alternative solution is often considered, the mechanical stacking. In this case, the two surfaces are simply approached, without producing a real interface. In this way, the various subcells can be independently connected, thus avoiding the limit of current matching.

1.3.2 III-V/Si solar cells

As we saw in Figure 1.8(a), a tandem solar cell with a Si bottom cell can reach an efficiency of 41.9% at 1 sun, if coupled with a 1.74 eV top cell. Connolly *et al.* also demonstrated that, by adding a third cell of 0.53 eV bandgap (therefore using Si as middle cell), the total efficiency can jump to 45.4% [15],



(a) (b)

Figure 1.16: (a) Triple junction solar cell radiative limit efficiencies for an AM1.5G solar spectrum as a function of top and middle bandgap subcells for a single lower bandgap cell of 0.53 eV. A maximum of 45.4% occurs for a silicon middle cell. From [15]. (b) Triple junction solar cell efficiency map for a 500x concentration as a function of top and middle cells bandgaps, for a fixed Si bottom cell. From [76].

as shown in Figure 1.16(a). Another study, performed by Derendorf *et al.*, demonstrated that, using a Si bottom cell in a 3J, the maximum efficiency can reach 55.6% under a 500x concentration [76], as shown in Figure 1.16(b). As well as for the efficiency records presented in the section 1.2.3, all the best results were obtained using GaAs technology to realize the III-V side.

Of course, the different ways to integrate III-V on Si can have very different impacts on the real efficiency of these cells. The epitaxial way still presents evident limits in terms of efficiency, due in particular to the high TDD. The most important results are a 19.7% obtained by Dimroth *et al.* [7] with an InGaP/GaAs/Si 3J cell and 21.2% declared by Umeno *et al.* [77] with an AlGaAs/Si tandem cell. Both results are very far from the theoretical maximal efficiencies. More generally, literature presents no multi-junction cells with steps of III-V growth on Si substrates with efficiencies over the 25%. To exceed this limit, it was always necessary until now to separately grow the two components and to bond or stack them afterwards. Relevant results obtained with surface activated wafer bonding are a 21.8% with a 2J AlGaAs/Si and a 25.2% with a 3J InGaP/AlGaAs/Si (1 sun) obtained by Vache *et al.* [78], a 27.6% efficiency obtained by Shigekawa *et al.* [79] with a 3J InGaP/GaAs/Si cell and a 30.2% obtained by Cariou *et al.* [71] with a 3J InGaP/AlGaAs/Si cell, while the current world record was recently obtained at Fraunhofer [80], with a 31.3% efficiency with a 3J InGaP/GaAs/Si cell. Finally, regarding mechanical stacking, although some interesting re-

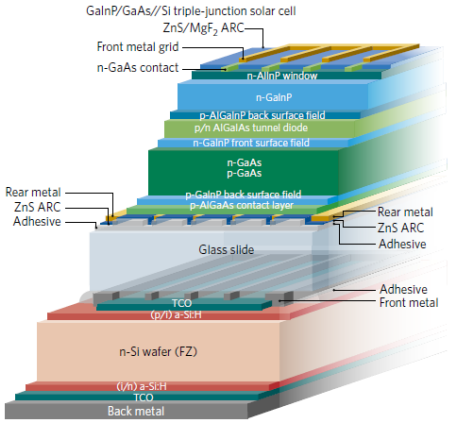


Figure 1.17: Design of the four-terminal GaInP/GaAs//Si 3J presented by Essig *et al.* [82], actual world record for hybrid III-V/Si photovoltaic. The GaInP top and GaAs middle cells are connected via a tunnel junction and stacked on a Si substrate.

Epitaxial techniques	**Non-epitaxial techniques**	
Direct and via buffer layer	Wafer Bonding	Mechanical Stacking
+ fewest process steps + lowest costs (no need for III-V substrate)	+ subcells fabricated separately at highest quality + low temperature integration - lift-off and re-use of growth substrates required	
- lattice and thermal expansion mismatches (defects, bowing, cracking) - epitaxy environment can impact Si minority carrier lifetime	- extra processing steps - mirror-polished clean surfaces required	+ flexible subcell design (e.g. Si front texture) - even more processing - optical losses due to intermediate conductive layer and metal grid
World record: 19.7% [7]	World record: 31.3% [80]	World record: 35.9% [82]

Table 1.5: Comparison between the most important III-V/Si integration techniques. Advantages, disadvantages and world records for every technique are reported.

sults were obtained with metallic bonding (e.g. via Pd nanoparticles, that allowed Mixuno *et al.* to obtain a 23.2% efficiency with an InGaP/GaAs/Si 3J [81]), the most efficient solution is to use adhesive bonding: the actual world records on 2J (GaAs/Si, 32.8%) and 3J (InGaP/GaAs/Si, 35.9%) cells were obtained by Essig *et al.* [82] with this technique (Figure 1.17). Both cells present a four terminal connection.

From these results, it is evident that, for the moment, the non-epitaxial techniques guarantee better efficiencies for hybrid III-V/Si solar cells. How-

ever, it is also worth remembering that such techniques are limited by their high costs and are hardly sustainable for an industrial production. Table 1.5 summarizes advantages, drawbacks and efficiency records for the presented approaches. In the last section of this chapter, we will present the three approaches taken in consideration for this work.

1.4 Aim of this PhD thesis

In the previous sections, we reviewed some of the most important milestones of the current photovoltaic research: the use of multi-junction stacking to overcome the Schockley-Queisser limit, the integration on Si to reduce the costs and make this technology more attractive, and the advantages and disadvantages of the most important III-V/Si integration techniques. This PhD takes place within this context.

III-V Lab has extensive experience on III-V growth and processing for the realization of devices such as lasers, amplifiers and photodiodes. The first aim of this thesis is to exploit this knowledge to develop a whole manufacturing process for the realization of high efficiency solar cells, from the sample growth to the final device characterization. In order to achieve this goal, we decided to work with materials lattice matched to InP (5.8687 Å): their most interesting advantage from a photovoltaic point of view is the optimized coverage of the solar spectrum, as mentioned before and presented again in Figure 1.18 from [83]. Although the InP technology (green line) lacks materials with bandgaps higher than 1.42 eV, it covers the whole range between 0.76 eV ($In_{0.53}Ga_{0.47}As$) and 1.42 eV ($Al_{0.48}In_{0.52}As$) thanks to the $Al_xIn_{1-x-y}Ga_yAs$ and $In_{1-x}Ga_xAs_yP_{1-y}$ alloys. On the other hand, we previously saw that the GaAs family (blue line) presents no materials whose bandgaps are comprised between 1.42 eV (GaAs) and 0.67 eV (Ge) and this last value is too low for 2J and 3J cells. In conclusion, where the GaAs technology requires the integration of lattice mismatched bottom cells ($In_{0.53}Ga_{0.47}As$ or Si), the InP technology allows to work with all lattice matched structures (bypassing the limitations due to the different interfaces). Leite *et al.* demonstrated that an optimized 3J device (red line) consisting in an $Al_{0.63}In_{0.37}As$ (1.93 eV) top cell, an $In_{0.38}Ga_{0.62}As_{0.57}P_{0.43}$ (1.39 eV) middle cell and an $In_{0.38}Ga_{0.62}As$ (0.94 eV) bottom cell (all presenting a 5.807 Å lattice parameter) can reach a photovoltaic efficiency higher than 51% for a relatively low 100 suns illumination [83]. Although the realization of such a structure is not the aim of this PhD, it is worth noting that the $\sim 1\%$ lattice mismatch between this optimized structure and the InP family makes it logical to test this very promising structure by starting from the InP parameter.

We decided to begin our research by realizing a simple, single junction cell in order to reduce the development difficulties, and then to extend the process to more complex dual junction devices. Our choice for the single cell material is the realization of an InP homojunction, as this material presents different advantages such as an 1.34 eV bandgap (very close to the optimal value for a 1J), a high electron mobility of 5400 $cm^2/(V{\cdot}s)$ at room temperature, a very high resistance to the degradation under irradiation [84] (this last characteristic is particularly interesting for space applications) and the possibility to be coupled with a lattice matched lower bandgap $In_{0.53}Ga_{0.47}As$ homojunction cell to realize a dual junction cell whose maximal theoretical efficiency is about 32% [15]. Last, but not least, as we can see from Figure 1.5(b), the actual world record of 24.2% [85] for this technology is still far from its theoretical maximum, unlike Si and GaAs. Therefore, improving this record should be possible. The realization of a MJSC requires the development of efficient tunnel junctions [86] lattice matched to InP, which are nowadays achievable only by ultrahigh vacuum techniques such as Chemical Beam Epitaxy (CBE) [87, 88].

In the second part of this work, we will deal with the integration of the InP-based cells on Si. We will focus our attention on the III-V/Si epitaxial growth via an intermediate buffer layer. Such a choice is motivated by the intention of completely removing the presence of fragile and expensive InP substrates from the whole manufacturing process (this is not possible with wafer bonding): this allows the reduction of the production costs without affecting the various realization steps, therefore maintaining the industrial sustainability of the whole process (the whole growth can be performed in the same reactor and the processing does not present relevant differences compared to the one performed onto InP). Another advantage of this principle is the fact that it can be easily extended to the realization of the optimized 3J structure presented by Leite *et al.* in Figure 1.18.

The integration of InP and the intermediate buffer(s) onto Si will not be directly carried out during this thesis: various templates grown onto Si substrates with an upper layer lattice matched to InP have been provided by different partners. Our tasks will consist of studying the epitaxy regrowth conditions, optimizing the process and evaluating how the presence of a lattice mismatched substrate can affect the final performances.

Multiple possibilities for the integration will be tested: first of all will be the use of the III-Sb materials presented in the section 1.3.1.1. This study will be performed with an academic partner, the Institut d'Electronique (IES) at the University of Montpellier. Our partner successfully used these templates for the integration onto Si of GaSb based devices. Our goal will consist into extend such a know-how to the InP family. A second possibility will be given by the use of an industrial template: these structures, presenting an intermediate GaP buffer layer, will be provided by the German society NAsP. Where

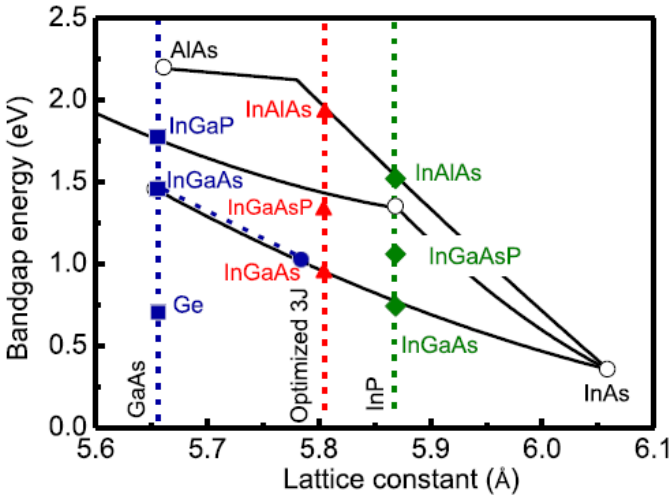


Figure 1.18: Optimized 3J devices lattice matched to GaAs (blue line), InP (green line) and a 5.807 Å lattice parameter (red line). This last device presents a $> 51\%$ efficiency under 100 suns concentration. The simulation considers a 1-dimensional device, assuming Lambert-Beer absorption, normal incidence of light, constant temperature (300 K), and AM1.5 direct 1-sun illumination. From [83].

the III-Sb templates represent an academic solution which still requires multiple optimization steps, this second possibility represents a very established process [61, 89, 90] that allows nowadays to uniformly grow InP/GaP layers onto 12" Si substrates. Finally, a third possibility will be given by the collaboration with the Laboratory of Microelectronics Technologies (LTM) of Grenoble, who will provide some templates characterized by intermediate GaAs buffer layers.

1.4.1 Outline of this manuscript

Chapter 1 presented the context in which this thesis work was developed. We underlined the importance of III-V semiconductors in the realization of high efficiency photovoltaic devices and the promising solution of the integration on Si to reduce the high costs of such cells. Finally, we presented the most important points that will be faced in this work.

Chapter 2 will be dedicated to some of the most important experimental tools used during this work. In particular, the MetalOrganic Vapour Phase Epitaxy reactors will be presented. Some of the most important material characterization techniques such as X-Ray Diffraction and Electrochemical Capacitance-Voltage profiling will be introduced as well.

Chapter 3 will present the technological realization of the individual single junction devices, as well as the evaluation of their photovoltaic performances. In particular, some important topics such as the design of a complete set of photolithographic masks and the development of an optimized processing system will be discussed. A preliminary, brief overview on the current state of such devices will be given too.

Chapter 4 will be dedicated to the realization of the tunnel junctions that allow the connection of the two subcells and to the realization of the tandem device. Special attention will be given to the low temperature epitaxial conditions necessary for the tunnel junctions' growth and to the integration steps of all the layers in the whole multi-junction cell growth.

Chapter 5 will present the characterization of the three above introduced templates (III-Sb, GaP and GaAs based) and the study of the epitaxy regrowth conditions over them. The realization of the cells presented in chapters 3 and 4 over the new Si substrates will be presented, giving a special emphasis to the technological challenges introduced by the new substrates. Finally, the obtained results will be compared with the corresponding ones obtained on the classic InP substrates.

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Chapter 2

Experimental techniques

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In this Chapter, we will present the growth and the material characterization techniques performed during this thesis. In the first part, the MetalOrganic Vapour Phase Epitaxy technique will be presented: after a preliminary theoretical introduction, we will present the two reactors successively used in this work. We will detail the main experimental aspects we had to deal with to increase the quality of the epitaxial samples. In the second part, we will present the two main characterization techniques performed for the calibration of our samples, X-ray diffraction and Electrochemical Capacitance-Voltage profiling, and mention some of the other techniques sometimes performed in addition.

2.1 MetalOrganic Vapour Phase Epitaxy

The growth technique chosen for this study is the MetalOrganic Vapour Phase Epitaxy (MOVPE), also called MetalOrganic Chemical Vapour Deposition (MOCVD). Nowadays, this technique is perhaps the most important pillar of the epitaxy industry, as it offers advantages such as a high level of control of the thicknesses of both thin and bulk layers, the possibility of achieving abrupt and complex heterostructures and the possibility of working out of ultra-high vacuum conditions. A huge variety of high quality microelectronic and optoelectronic components have been realized in the last decades by this technique [1–4]. Since one of the fundamental aspects of this work is the development of an industrial-compatible process, the excellent qualities of MOVPE make this technique ideal for such a purpose.

2.1.1 Principle

Vapour Phase Epitaxy, described for the first time by Manasevit in 1968 [5], is an epitaxial growth technique based on the chemical reactions between reactive species carried in the gaseous state in a cold-wall reactor to a high-temperature substrate. Although the first used species were mainly chlorides and hydrides (in these cases, we speak of ClVPE and HVPE, respectively), nowadays they are usually organometallics (hence the name MOVPE). This out-of-equilibrium technique allows the growth of a wide variety of materials such as II-VI semiconductors [6, 7] and superconductors [8, 9], but its main use is the growth of III-V semiconductors.

In this study, the precursors of the group V elements were hydrides, characterized by a V-H_3 structure; whereas those of the group III elements were organometallics of the trimethyl (TM) type, characterized by a III-$(CH_3)_3$ structure. The MOVPE growth mechanism is described in Figure 2.1: the organometallics and the hydrides, diluted in a high hydrogen (H_2) flow (which acts as vector gas), interact with the high temperature substrate surface and are pyrolyzed. The groups III and V elements are then released and free to organize themselves in a crystalline structure on the underlying substrate. For example, the chemical reaction that rules the growth of an InP layer from the precursors trimethylindium (TMIn) and phosphine (PH_3) is:

$$In\,(CH_3)_3 + PH_3 \rightarrow InP \downarrow + 3CH_4 \tag{2.1}$$

The products of this reaction are then an InP epitaxial layer and gaseous methane (CH_4), which is pumped away. In fact, equation 2.1 is only a gross representation of the real chemical phenomenon, since it does not consider all the intermediate decomposition steps that characterize this reaction [10, 11].

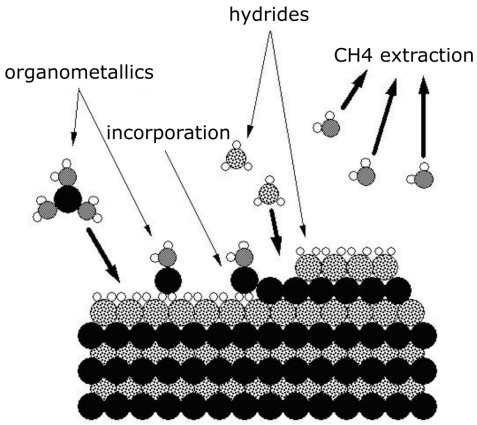


Figure 2.1: Illustration of the MOVPE process. Adapted from Wikipedia.

This is not the only complex passage: the same growth phenomenon is difficult to model, since it results in the net effect of multiple kinetics [12], fluid dynamics [13, 14] and thermodynamics [15] processes. Such uncertainties make this technique extremely empirical.

2.1.2 Experimental systems

We can distinguish two main geometries of commercial MOVPE reactors, the horizontal and the vertical. The two terms indicate whether the gases are injected in the reactor parallelly or perpendicularly to the substrate, respectively. In this work, both the horizontal and the vertical configurations were used.

The AIX200/4 horizontal reactor Figure 2.2 presents the schematic structure of the AIX200/4 horizontal reactor used in the first part of this thesis. The reactor has a mono-wafer capability for 2, 3 or 4 inches substrates. The substrate is placed on a graphite susceptor and kept in rotation thanks to a H_2 flux flowing in a proper circuit inside the susceptor [17], thus guaranteeing a better uniformity of the grown layers. The substrate-susceptor system is heated by a series of infrared lamps placed around the reactor, and the temperature is monitored by a thermocouple placed inside the susceptor. Since graphite has an excellent thermal conductivity, we can reasonably consider that the susceptor temperature is uniform. Dauelsberg *et al.* demonstrated that this assumption is true for growth conditions very

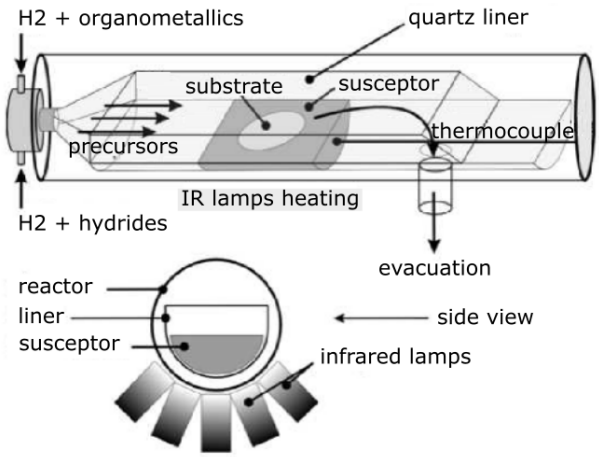


Figure 2.2: Schematic representation of the AIX200/4 reactor.

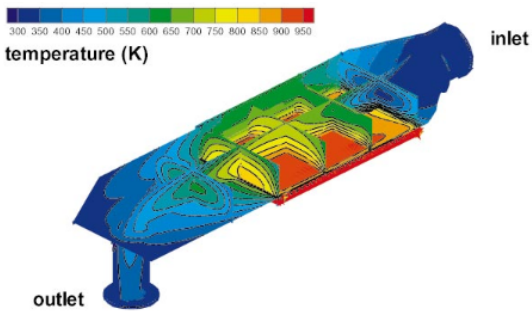


Figure 2.3: Computed temperature distribution in the gas phase in an AIX200/4 reactor at 20 mbar reactor pressure, 700 °C deposition temperature for H_2 carrier gas under optimized growth conditions. For visualization, a grid was put over the susceptor and the reactor is presented partly open (the ceiling and one sidewall are missing). From [16]

close to the ones used in this study [16] (Figure 2.3). The organometallic and the hydride gases, diluted in H_2, are injected inside the reactor by two different injection gas lines and reach the substrate as a laminar flow. The gaseous products of the reaction, as well as the reagents in excess, are evacuated on the opposite side of the reactor. In order to protect the reactor sidewalls from unintentional depositions, the growth system is placed in a quartz liner. This liner can be removed after the growth and separately cleaned in an aqua regia solution (a mixture of hydrochloric, HCl, and nitric, HNO_3, acids).

In addition to the reactor, the MOVPE system is composed by an introduction system, a gas panel and an evacuation system. The introduction system is in turn composed of two parts: a transfer chamber, that allows one to load and extract the samples and other components from the system

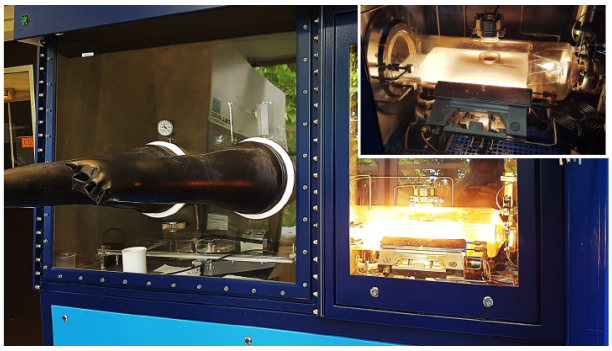
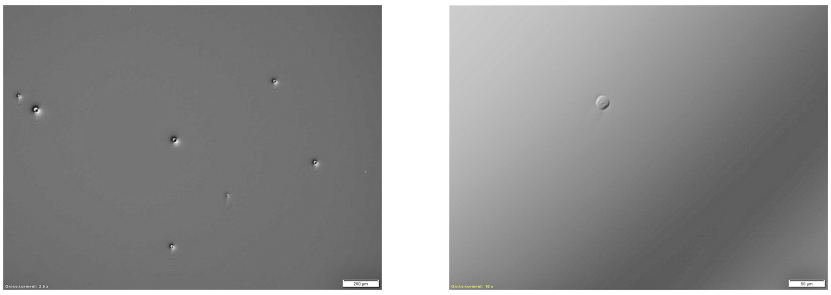


Figure 2.4: A picture of the AIX200/4 horizontal reactor used in the first part of this thesis. It is possible to identify the glove box on the left and the reactor (while heating) on the right. An upper view of the reactor is showed in the inset.

by switching from the external to an inert nitrogen (N_2) atmosphere, and a glove box connected to the reactor, that allows work in the system without exposing it to the external atmosphere. The pressure inside the box is usually kept slightly higher than 1 atm, in order to avoid external infiltrations. The gas panel includes the whole system of tubes that brings the precursors to the reactor, and will be presented in section 2.1.3. Finally, the evacuation system is composed by a filter and a pump whose function is to extract and treat the gaseous products of the reaction. A picture of the horizontal reactor used in the first part of this thesis is showed in Figure 2.4.

The *showerhead* vertical reactor In the second part of the thesis, the growths were performed in a vertical reactor (Close Coupled Showerhead, CCS). As previously mentioned, the difference lies in the direction along which the precursors are injected in the reactor and, therefore, reach the substrate. The main advantage, compared to the horizontal configuration, is protection of the sample from the fall of particles arising from parasitic depositions on the liner ceiling during the growth. Such particles can affect the homogeneity of the deposition and give rise to the formation of holes and/or clusters in the epitaxial layers (Figure 2.5). This phenomenon is more probable for long depositions, as in our case (several μm of deposition).

The structure of the CCS reactor, presented in Figure 2.6, is quite similar to the one of the AIX200/4: the main differences are a larger susceptor (able to receive six 2", three 3", one 4" or one 6" substrates) and a different heating system (Joule effect through resistive coil). The new reactor is furthermore equipped with a LayTec EpiCurve®TT SP in-situ metrology system. This system is able to evaluate (by Reflectometry at 405, 650 and 950 nm) the growth rate, thickness and morphology of the epitaxial layers, as well as substrate true temperature (Pyrometer 950 nm) and curvature. Finally, a



(a) (b)

Figure 2.5: Defects arising from particles fallen on a substrate surface otherwise perfectly mirror like. The magnifications are (a) 2.5x and (b) 10x. Such a phenomenon is more probable for long depositions.

Figure 2.6: A picture of the CCS reactor used in the second part of the thesis. It is possible to notice the gas panel on the left, the glove box and the reactor in the center and the transfer chamber on the right. In the inset, the open reactor (in the 6x2" configuration) is showed.

second pyrometer allows evaluation of the susceptor surface temperature.

2.1.3 Precursors

As already mentioned, we used organometallic precursors for the group III elements. These precursors were TMIn, trimethylgallium (TMGa) and trimethylaluminum (TMAl) for In, Ga and Al, respectively. Despite its name, this last one does not have the typical III-$(CH_3)_3$ structure, but it presents itself in the $Al_2(CH_3)_6$ formula, as dimer. The trimethyl- type

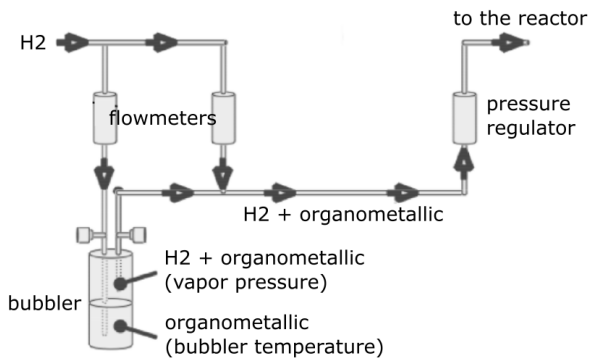


Figure 2.7: Schematic representation of an organometallic source system.

Precursor	A	B [K]
TMIn	10.52	3014
TMGa	8.07	1703
TMAl	8.22	2134
DEZn	8.28	2109
CBr_4	7.78	2346

Table 2.1: The values of the parameters A and B for all the used organometallics. From [18, 19].

precursors are very interesting because of their high stability (due to the small number of carbon bonds [18]) and vapour pressure. Therefore, they are in the liquid (or solid, in the TMIn case) state at room temperature, easy to handle and transport. We used organometallic sources for the p-type dopants: diethylzinc (DEZn, or $(C_2H_5)_2Zn$) and tetrabromomethane (CBr_4) were the precursors of Zn and C, respectively. Figure 2.7 presents the gas system that allows introduction of an organometallic precursor inside the reactor: the liquid source is stocked in a bubbler, the temperature of which is kept constant by immersing it in a thermostatic bath. The H_2 carrier gas is injected through a tube inside the liquid, then uptakes part of the vapour present in the bubbler upper part, carrying it through a second tube. The mix is then further diluted in H_2 and injected in the reactor. The total precursor flow is given by [20]:

$$F_{organometallic} = \frac{p}{p_0 - p} \cdot F_{H_2} \tag{2.2}$$

where F_{H_2} is the H_2 flow that pass through the bubbler, p_0 is the pressure in the bubbler and p is the vapour pressure of that organometallic precursor. This last value is given in turn by:

$$p\,[torr] = e^{\left(A - \frac{B}{T}\right)} \tag{2.3}$$

where T is the bubbler temperature in Kelvin and A and B two characteristic parameters for every organometallic source. Table 2.1, from [18, 19], summarizes these values for the used organometallic precursors.

Group V elements are provided by the use of hydrides precursors; in particular, PH_3 and arsine (AsH_3) are the sources of P and As, respectively. These precursors are characterized by a very high purity. Unfortunately, their extremely high toxicity makes them very dangerous. In our study, the n-dopant precursors were hydrides: disilane (Si_2H_6) and hydrogen sulfide (H_2S) were the sources of Si and S dopants, respectively. These precursors are stored under pressure and separately introduced in the reactor.

2.1.4 Main aspects of a MOVPE growth

In this section, we will give a brief summary of the most important factors that have to be kept under control to guarantee the quality and the correct composition of the epitaxial layers.

Equation 2.2 allows one to determine the effective flow of every organometallic precursor by knowing the diluting H_2 flow, the pressure inside the bubbler and its temperature. On the contrary, the hydride gas flows are directly set by the operator. The ratio between these two values is called *V/III ratio*. Usually, the vapour pressure of group V elements is much higher than that of group III elements; therefore they are very unstable in the solid phase for typical growth temperatures. In order to prevent a partial desorption of group V elements (and, therefore, to keep a good morphology), it is necessary to keep the hydrides flow much higher than that of the organometallics (V/III ratio $>> 1$). As a consequence, the chemical kinetics is controlled only by the group III elements: the growth rate is directly proportional to the group III elements' partial pressure and independent to that of group V elements. Therefore, the control on the V/III ratio allows one to monitor the morphology and the growth rate of the alloy.

In a similar way, when introducing a dopant precursor with a low vapour pressure (almost all the dopants reaching the crystal surface are incorporated), the dop/III (or dop/V) ratio allows to control the n-type or the p-type doping (mass-transport limit case). This is not true for high vapour pressure dopants such as Zn, when thermodynamics have to be taken into account to determine the effective dopants incorporation [21]. The dop/III and dop/V ratios describe indirectly the competition between different atoms

for the same sites in the crystal lattice: the higher they are, the more doped the alloys are (until the dopant saturation limit is reached).

When growing ternary and quaternary alloys, it is necessary to reach the correct chemical composition to obtain the desired lattice parameter and/or energy gap (Figure 1.11, page 15). Considering a ternary alloy such as $In_{1-x}Ga_xAs$, the lattice parameter is given by the Vegard law [22]

$$a_{In_{1-x}Ga_xAs} = xa_{GaAs} + (1-x)\, a_{InAs} \tag{2.4}$$

whereas the energy gap is given by

$$Eg_{In_{1-x}Ga_xAs} = xEg_{GaAs} + (1-x)\, Eg_{InAs} - bx\,(1-x) \tag{2.5}$$

where a_{GaAs}, a_{InAs} and Eg_{GaAs}, Eg_{InAs} are the lattice parameters and the energy gaps of the single binary compounds constituting the alloy and b is the bowing parameter, characteristic for every alloy. The same principle can be extended to a quaternary alloy such as $In_{1-x-y}Al_xGa_yAs$ [23, 24]. The chemical composition of a ternary alloy can be easily identified by X-ray diffraction (see section 2.2). The better way to adjust the composition in a new growth is to keep constant the flow of one of the two competing precursors and changing only the other one. The flow that allows one to reach the desired composition is given by:

$$\phi' = \phi \cdot \frac{x'}{x} \cdot \frac{1-x}{1-x'} \tag{2.6}$$

where ϕ is the previous flux, x the measured composition and x' the wanted one. In our growths, we usually keep the TMIn flux constant.

The greatest influence of temperature during growth is on the quality of the samples. A high growth temperature coincides with a high mean path of the atomic species on the sample surface, and consequently to a high crystal quality. At the typical growth temperatures (600-700 °C), the growth rate has a very low dependence on temperature, since it is only limited by the mass transport between the vapour phase and the solid [25]. The effects of the temperature on the growth rate are more relevant below 600 °C, where a temperature decrease coincides with a decrease of precursors cracking (and thus with a lower growth rate), and over 800 °C, when an increase of temperature induces a higher desorption and then a lower growth rate.

All the materials presented in this work were grown in the 600-700 °C range, except the cathodes and the anodes of the tunnel junctions presented in chapter 4 (in order to increase dopants incorporation at very low temperatures).

Another important aspect of a MOVPE growth is the hydrides commutation. It is very common, during a growth, to switch from a P-based semiconductor such as InP to an As-based one such as InGaAs, or vice versa. It is well known that InGaAs on InP interfaces are substantially smoother and more abrupt than InP on InGaAs interfaces [26–28]. This is due to the high binding energy between P and Ga: when InP is grown on an InGaAs layer, the P in excess on the surface tends to diffuse inside the underlying compound for tenths or even hundreds of nm, bonding to the Ga atoms. The high lattice mismatch introduced by this phenomenon can even crack this layer: in this case, it is common to notice the formation of little pyramids, whose presence can affect the final morphology of the sample [28] (the same phenomenon is much less significant with AlInAs layers, since the absence of Ga reduces the morphology issues). Even if this phenomenon cannot be completely prevented [29], it is known that a temporary, strong reduction of the AsH_3 and PH_3 flows during the switch, in addition to a brief epitaxy interruption at the interface, can significantly reduce this effect. Alternatively, very thin (few nm) InGaAsP quaternary compounds can be introduced at the interfaces to reduce this phenomenon.

Another phenomenon, although less relevant, may occur: during a P-based/As-based growth, some As atoms can diffuse in the upper layer, giving rise to $InAs_yP_{1-y}$ structure [30]: in this case, however, the low lattice mismatches do not affect the final morphology so much.

2.2 X-Ray Diffraction

X-ray diffraction (XRD) is one of the most important techniques to characterize the grown samples. It gives access to a wide range of physical and structural properties, from the strain, to the composition, to the thickness of the epitaxial layers. Since it is a non destructive technique, it can be systematically performed not only on the calibration samples, but also on the more complex structures that will be processed into devices, in order to check the quality of the growth.

The physics that rules the elastic scattering of X-rays on a periodic lattice and that is at the base of XRD technique is very well known [31–33]: the dimensions of the lattice parameter of typical crystals (some Å) are similar to the typical wavelengths λ of X-rays; therefore, when an X-ray beam is focused

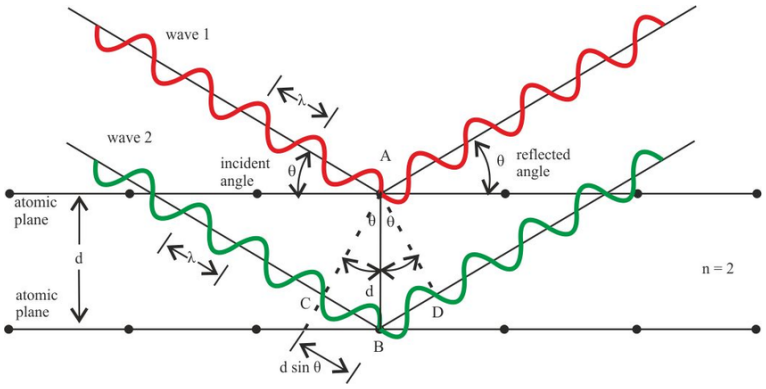


Figure 2.8: Schematic representation of the Bragg law for a generic crystalline plane.

on a crystal, a diffraction pattern will be generated by the interference of the scattered waves (Figure 2.8). This diffraction is governed by the Bragg law:

$$2\, d_{hkl}\, sin\theta = n\, \lambda \tag{2.7}$$

where n indicates the order of the diffraction, d_{hkl} is the distance between the reticular planes (h, k and l are the corresponding Miller indices) and θ is the angle between the diffractive planes and the incident/reflected angles. Since d_{hkl} is typical for every crystal and defined, for a tetragonal lattice, as:

$$\frac{1}{d^2} = \frac{h^2 + k^2}{a_{\parallel}^2} + \frac{l^2}{a_{\perp}^2} \tag{2.8}$$

where $a_{\parallel}$ and $a_{\perp}$ are respectively the in-plane and the out-of-plane (along the growth direction) parameters, it follows that also the so-called Bragg angles θ that maximize the diffracted intensity are fixed for a certain material. In most cases, the analyzed plane is the (0 0 4): it is easily accessible on our samples; being (0 0 1) oriented monocrystals, it allows to work on high angles, increasing the sensibility; and it gives direct informations on the $a_{\perp}$ parameter, as the condition $h = k = 0$ remove the dependence from $a_{\parallel}$.

2.2.1 Determining structural properties

Let us consider the case of the heteroepitaxy of a layer onto a substrate with the same crystalline structure (already mentioned in Figure 1.12(a) on page 16). Figure 2.9 presents the case of a compressively strained layer, where its $a_{\parallel}$ parameter is greater than the substrate one: the crystalline structure of the layer will deform itself to adapt to the substrate lattice parameter, thus

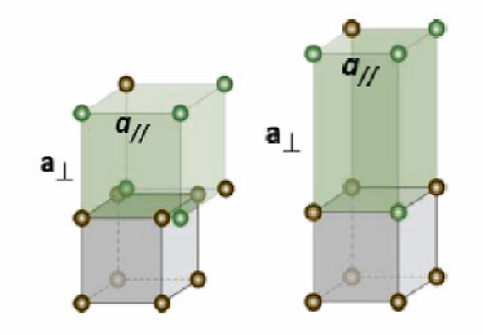


Figure 2.9: Example of the crystalline deformation of an epitaxial structure to match with the substrate structure (compressive strain case). Figure provided by and modified from Bruker.

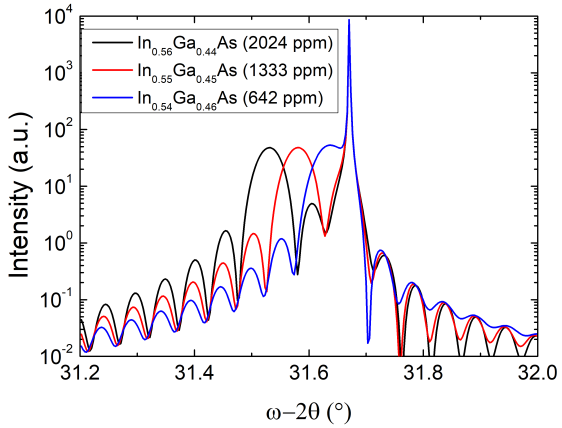
increasing its $a_{\perp}$ parameter. From equations 2.7 and 2.8, we can deduce a left-shift of the corresponding intensity peak (similarly, a tensile strain will coincide with a right-shift). In general, the XRD scan of any sample will present a peak for every different material (or composition) included in the structure.

By evaluating the angular difference between a layer peak and the substrate one, it is possible to obtain the layer mismatch $\frac{\Delta a}{a_{sub}}$ (usually expressed in parts per million, or ppm) and lattice parameter a. In the case of a ternary alloy, a allows us to determine the chemical composition from the Vegard law (equation 2.4). Figure 2.10(b) shows the simulated XRD scans for three 100 nm thick InGaAs layers grown onto an InP substrate, characterized by different chemical compositions: the reduction of the Ga content induces a higher compressive strain in the layers.

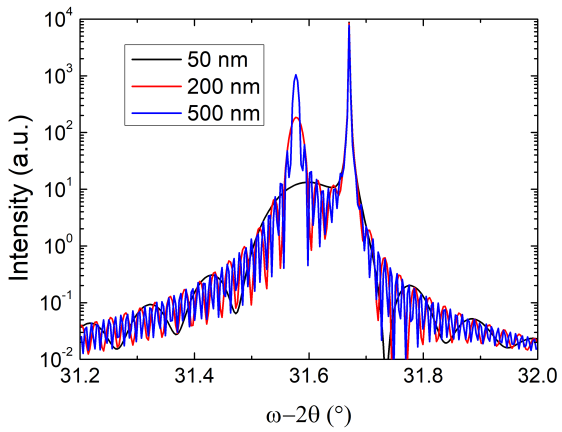
The thicknesses of the epitaxial layers can be estimated as well [31, 34, 35]: as shown in Figure 2.10(c), a thicker layer with the same composition (in the simulated case, $In_{0.55}Ga_{0.45}As$) gives rise to a more intense peak (for the same reason the substrate peak is particularly intense and sharp) and to shorter oscillation periods. By matching an experimental curve with a simulated one for the same structure, it is possible to obtain the various thicknesses with a high precision (around 1 nm).

We already mentioned in Chapter 1 that, over a certain limit thickness, the epitaxial layers tend to relax towards their original structure, giving rise to dislocations. Such a critical thickness depends, of course, on the original lattice mismatch between the epitaxial layer and the substrate: the higher the mismatch, the lower the amount of material that can be deposited without relaxation. For example, because of the 8% lattice mismatch, the limit thickness for InP on Si is only a few monolayers.

XRD also allows us to evaluate the percentage of relaxation in an epi-



(a)



(b)

Figure 2.10: (a) Effects of different chemical compositions on the XRD scans of three 100 nm thick InGaAs layers. A decrease in the Ga content consists of a compressive shift of the peaks. (b) Effects of different thicknesses on the XRD scans of three $In_{0.55}Ga_{0.45}As$ layers. An increase of the thickness consists of a more intense peak and a shorter oscillation period.

taxial layer: Figure 2.11(a) presents the effects of relaxation in the peak of a 200 nm thick InP layer grown onto Si (the dimensions of the layer were exaggerated for a better comprehension: as previously mentioned, such a thick layer cannot present a 100% strained structure). A completely relaxed layer (blue curve) presents a peak at the typical θ of InP ($\sim 31.67°$); a completely strained one (black curve) is compressively shifted. A partial relaxation coincides with an intermediate curve, of which peak position allows to evaluate

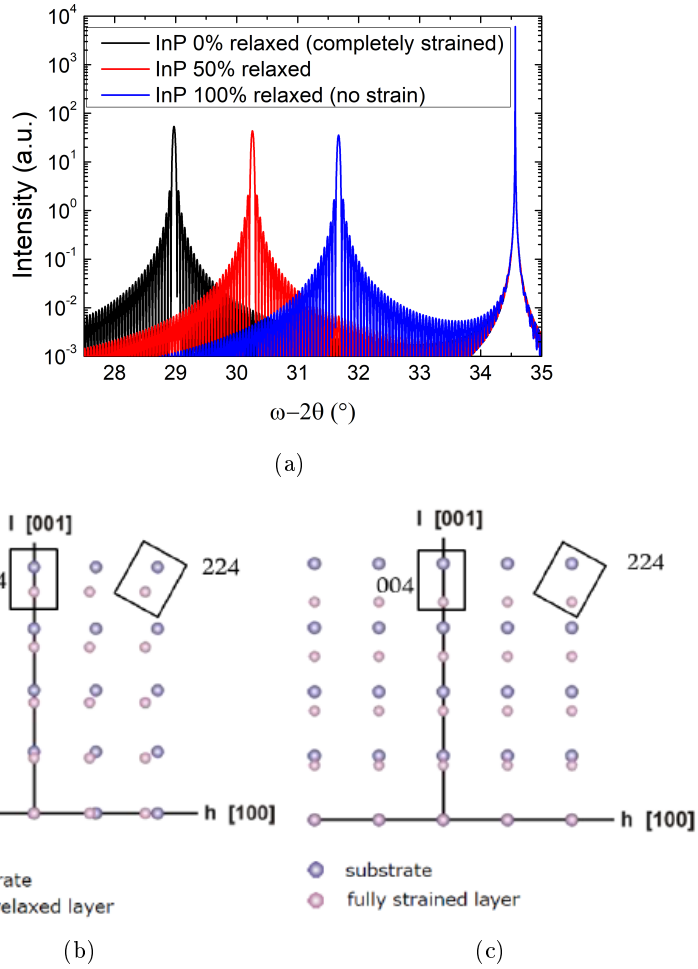


Figure 2.11: (a) Effects of different relaxation percentages on the XRD scans of three 200 nm thick InP layers grown onto Si substrates. An increase of the relaxation coincides with a peak more shifted to a higher angle. (b) RSM of a fully relaxed layer. When performing the scan around the (2 2 4) direction, an alignment of the layer and the substrate peak with the origin of the reciprocal space occurs. (c) RSM of a fully strained layer. When performing the scan around the (2 2 4) direction, an alignment of the layer and the substrate peak along the direction parallel to the (0 0 l) planes occurs. Figures (b) and (c) are provided by Bruker.

the degree of relaxation (for example, the red curve corresponds to a 50% of relaxation).

Unfortunately, it is not so easy to evaluate the relaxation of an epitaxial layer, since it is not possible to decorrelate the shift of the peak due to the relaxation from the one due to the composition for this kind of measure (the case of Figure 2.11(a) is special since InP has an unique chemical com-

position). Therefore, when growing a ternary alloy or a structure such as $Si_{1-x}Ge_x$ (unless the chemical composition is well known to be very close to the one of the lattice matched structure, thus guaranteeing a completely strained layer), a $\omega/2\theta$ scan along the (0 0 4) plane is not sufficient to determine both relaxation and chemical composition. In this case, a Reciprocal Space Mapping (RSM) is needed. RSM consists in a series of multiple $\omega/2\theta$ scans for different ω. The result is a rectangular mapping of the reciprocal space around the peak of interest. Even in this case, a mapping around the (0 0 4) peak is not particularly interesting: by comparing Figures 2.11(b) and (c), we can see that both the completely relaxed and the completely strained case present layer peaks aligned along the (0 0 l) direction and are, therefore, indistinguishable. On the contrary, when performing an asymmetric scan, typically along the (2 2 4) direction, the two maps present a substantial difference: a fully relaxed layer will present its maximum peak along the connecting line between the substrate peak and the origin of the reciprocal space (b); a fully strained layer, instead, will present this peak along the parallel direction to the (0 0 l) one (c). Finally, a partially relaxed layer will present its peak in an intermediate position.

2.2.2 The measurement

Two different diffractometers were used during this thesis: a Bruker D8 and an X'Pert PANalytical. Both systems utilise a Cu tube for X-ray generation, using the Kα radiation (λ = 1.54056 Å). The schematic structure of this second diffractometer is shown in Figure 2.12: ω and 2θ corresponds respectively to the angle between the X-ray source and the plane containing the sample and the angle between the projection of the incident beam inside the sample and the detector, the angle ϕ defines the rotation of the sample around its (0 0 1) direction and ψ the angle between this last direction and the Z-axis.

In typical conditions (symmetric reflexion), the signal is maximum at the Bragg angle when $\omega = 2\theta/2$ (in other words, when the incident and the reflected angles are equal). It may nevertheless happen that a certain difference between ω and θ occurs: such a difference, called offset, is usually due to little imperfections in the setup alignment or to the fact that the substrate is offcut by a certain angle along another crystalline plane. To evaluate such a misorientation, it is necessary to perform a so-called rocking curve (ω-scan at a constant 2θ, which allows also to determine other informations on the in-plane direction such as curvature and mosaicity) around the Bragg angle. A typical XRD measure is taken by performing an $\omega/2\theta$ scan (so, keeping constant the offset) after a proper, preliminary optimization of the four angles and the Z-axis to maximize the signal on the Bragg peak of the substrate.

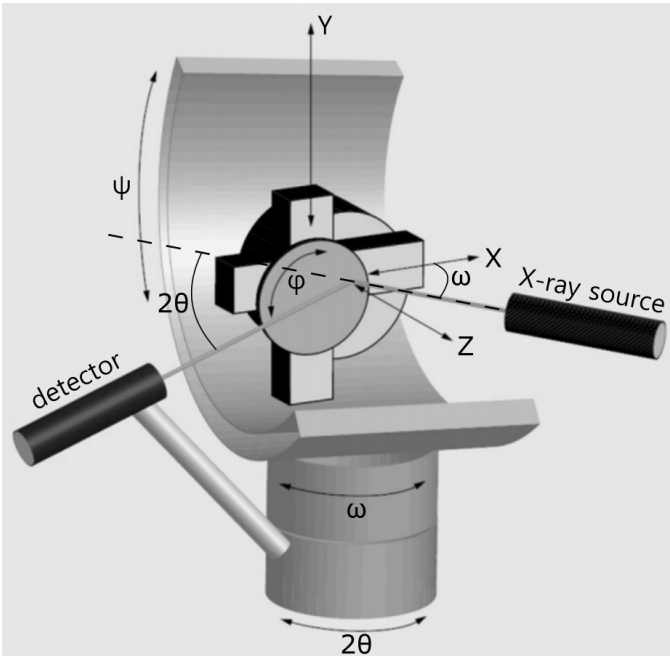
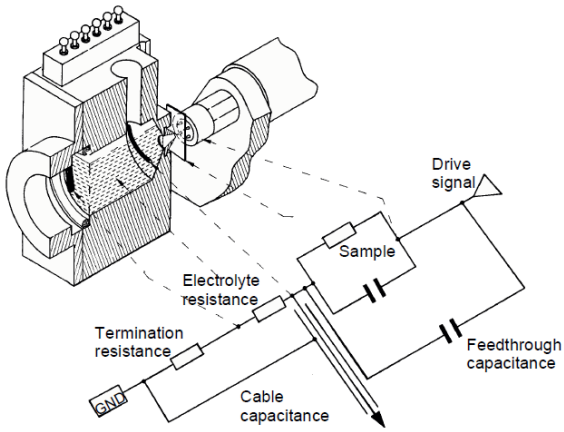


Figure 2.12: XRD apparatus of the X'Pert PANalytical system used during this thesis, showing the different scan (rotation) axis. Adapted from [34].

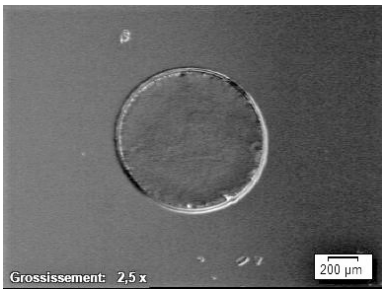
2.3 Electrochemical Capacitance-Voltage profiling

The Electrochemical Capacitance-Voltage (ECV) profiling is a destructive technique that allows us to measure the active carrier concentration profiles (the doping levels) of semiconductor layers. It exploits the principle of the electrolyte-semiconductor Schottky contact [37, 38] to create a depletion region free of carriers but containing ionized donors and electrically active defects or traps inside the semiconductor. Therefore, this region behaves like a capacitor. Depth profiling is achieved by electrolytically etching the semiconductor between every capacitance measurement (theoretically, with no depth limitation).

The electrochemical cell used is schematically presented in Figure 2.13(a): the sample is pressed against a sealing ring in the electrochemical cell containing an electrolyte. For typical As- and P-based semiconductors, such an electrolyte is usually ammonium tartrate ($C_4H_{12}N_2O_6$). The contact area is defined by the ring opening (Figure 2.13(b) shows an example of a generated crater). The depletion region is created by applying a potential V between the semiconductor and the platinum electrode measured with respect to the reference saturated calomel electrode (in order to keep the 'electrical circuit'



(a)



(b)

Figure 2.13: (a) The electrochemical cell and measurement circuit. Adapted from [36]. (b) $\sim$1.5 μm depth crater in a bulk InP sample (2.5x magnification).

closed, it is necessary that the substrate is doped). By measuring the capacitance C of the depleted region, it is possible to extract its doping level from the relation [36]:

$$N = \frac{1}{q\epsilon_0\epsilon_r A^2} \times \frac{C^3}{dC/dV} \tag{2.9}$$

where q is the electron charge, ϵ_0 and ϵ_r the vacuum and the relative permittivity of the semiconductor and A the effective contact area. It is therefore very important to evaluate the effective size of the contact area, avoiding the formation of bubbles or O-ring distortions resulting from variations in the pressure holding the sample against the cell.

Another important parameter is the applied voltage, since it allows us to control the etching rate and, consequently, the etching uniformity and the spatial resolution of the measurement. This technique can guarantee excellent spatial resolution, enabling us to distinguish the doping levels with

a depth resolution below 5 nm. Unfortunately, such a high resolution implies an extremely low etch rate. It is therefore necessary to find a good compromise between sensitivity and duration of the measurement.

In conclusion, ECV profiling is a very attractive technique, since it allows quick and reliable evaluations of the doping levels of bulk layers but also of thin interfaces and whole devices. By combining it with Secondary Ion Mass Spectrometry profiling, it is possible to estimate the dopants' activation and, therefore, the doping efficiency.

2.4 Other techniques

The two techniques presented above were sufficient to characterize most of the grown samples. Nevertheless, it was sometimes necessary to perform some additional characterizations depending on the property that had to be evaluated. In particular, these further techniques were optical microscopy (evaluation of surface morphology), profilometry (evaluation of thicknesses), Secondary-Ion Mass Spectrometry (SIMS, to evaluate the single elements - and in particular the dopants - concentration along the various layers), Hall effect (evaluation of superficial mobility and doping levels), photoluminescence (PL, evaluation of semiconductors energy gap), Transmission Electron Microscopy (TEM, to evaluate the crystalline quality and/or the TDD), Scanning Electron Microscopy (SEM, for high precision imaging of surfaces) and Atomic Force Microscopy (AFM, to evaluate the superficial roughness).

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Chapter 3

Realization of InP and InGaAs single junction devices

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In Chapter 1 we introduced the two single junctions solar cells (InP- and InGaAs-made) that we will finally combine in a tandem device. At first, these devices had to be independently realized and optimized: this chapter is dedicated to the presentation of the developed solar cells manufacturing process. Most of the chapter will be dedicated to the optimization of the InP top cell: after a brief overview of the state of the research for this type of

device, the basic structure of the cell, as well as the various parameters, will be presented. The growth and the general processing procedures will then be described (a special attention will be given to the design of an efficient set of photolithographic masks for processing). Next, the various implementations and corresponding results will be presented. Finally, the same presentation will be (briefly) given for the InGaAs based bottom cell as well.

3.1 InP single junction state of the art

As already mentioned in Chapter 1, InP is a very promising material for the realization of high efficiency single homojunction devices. This is due to multiple interesting characteristics such an almost ideal bandgap (1.34 eV), a lower sensitivity to temperature than Si [1], a lower surface recombination velocity (approximately 10^3 cm/s) than GaAs [2], and a higher resistance to degradation than both Si and GaAs [3, 4].

The potential of this material is more strongly indicated for the realization of thin, monocrystalline devices: although Yamaguchi *et al.* presented a polycrystalline device using some 10 μm thick grains, they obtained a lower than 10% efficiency. They further calculated that even a 100 μm thick device cannot overcome the limit of 15% [1]. Some successful photovoltaic results were obtained by using thermal diffusion of S inside InP:Zn substrates (18.0% efficiency under AM1.5G spectrum) [5]. As an alternative, even LPE was successfully tested (17.2% under AM0 spectrum) [6, 7]. However, most of the research over InP homojunction solar cells was performed by MOVPE growth.

The InP devices were usually grown by MOVPE on p-type (Zn) doped substrates, thus realising n^+-p junctions (the doping level of the emitter is more or less one order of magnitude higher than that of the base, 10^{18} versus 10^{17} cm^{-3}). All structures present emitters whose thicknesses are comprised between a tenth and a few hundreds of nm and bases of 3-5 μm thicknesses. In particular, Sugo *et al.* determined the effects of the emitter thickness on the final device performances [8]: a decrease in the thickness (and therefore, of the junction depth) coincides with an increase of J_{SC} but unfortunately also of J_s, and so a decrease of V_{OC} [9] and FF. As a net effect, a $\sim$ 200 nm thick emitter should be preferred. They also demonstrated the positive effect of a sufficiently highly doped substrate ($\geq 10^{18}$ cm^{-3}), which involves a significant reduction of R_s. By adding an Sb_2O_3 antireflective coating (ARC), they obtained a 20.0% efficiency. Other important results were obtained by Keavney *et al.*, by realizing a graded n-side from 3×10^{19} cm^{-3} doping level at the surface of the cell to 3×10^{18} cm^{-3} at the junction (and adding a

	J_{SC} (mA/cm^2)	V_{OC} (V)	FF (%)	η (%)
n^+p	42.37	0.9411	86.3	25.1
p^+n	41.49	0.9977	86.9	26.2

Table 3.1: Comparison of performance parameters of the optimally designed n^+p and p^+n InP solar cell structures (AM0, 1 sun, 137.2 mW/cm^2, 25 °C). From [13].

ZnS/MgF_2 bi-ARC) with a 19.1% efficiency [10], and by Spitzer *et al.* who, with a similar structure, obtained an efficiency of 17.9% (but with a higher FF of 83.7%) [11]. The state of the art for this kind of polarity was recently obtained by Wanlass [12]: the presented efficiency was 24.2%, but a detailed description of thicknesses and doping levels was not unfortunately given.

Although most of the InP solar cells were realized over p-substrates, Jain *et al.* demonstrated that an inverse polarity, where the base and the substrate are n-type and the emitter p-type, can be preferable [13]. By using PC-1D, a quasi-one-dimensional computer programme based on solving semiconductor transport equations by a finite-element method [14] and assuming optimal designs for both the configurations, zero front contact shadowing loss, 0.1 Ω·cm^2 series resistance and a ZnS/MgF_2 bi-ARC, they showed that, although the n^+p configuration offers a higher J_{SC}, the p^+n configuration guarantees improved V_{OC} (favoured by a decrease in J_S [15]) and overall gain in the cell efficiency. These effects are summarized in Table 3.1. Furthermore, the p^+n configuration should present a higher end-of-life efficiency, especially for space applications [16]. Finally, another advantage arises from the beneficial effect that the introduction of a thin (10-20 nm) $Al_{0.48}In_{0.52}As$ may have on a p^+n structure: the surface passivation guaranteed by this higher bandgap material (1.42 eV) can improve the efficiency of such a device from 15.4% to 23%. On the other hand, the same improvement does not occur in the n^+p configuration [17, 18]. A similar result can be obtained by considering tensile strained, 10 nm thick $Al_{0.60}In_{0.40}As$ (1.8 eV bandgap) window layer [19].

Despite what has been reported, the literature presents a very small number of devices realized in the p^+n configuration: we can mention the interesting results obtained by Choi *et al.* (15.4% efficiency) [20], and by Yamaguchi *et al.*, (22.0% efficiency) [21].

3.2 Presentation of the InP cell

We already mentioned in Chapter 1 that the first part of the thesis was dedicated to the realization of a single, homojunction device based on InP. Such an approach was motivated by the necessity of setting up a whole manufac-

Function	Material	Thickness (nm)	Dop. level (cm^{-3})
Contact layer	$In_{0.53}Ga_{0.47}As$:Zn	X	$+2\times10^{19}$
Window layer	X:Zn	X	$+1.5\times10^{18}$
Emitter	InP:Zn	X	$+1\times10^{18}$
Transition layer	InP nid	20	–
Base	InP:Si	X	X
BSF	InP:Si	700	-2×10^{18}
Substrate	InP:S	3.5×10^{5}	-2×10^{18}

Table 3.2: General structure of the studied device. The terms indicated by a *X* have to be optimized, the terms directly shown can be considered acceptable. The growth direction goes from the bottom to the top of the table.

turing process for this kind of device at III-V Lab. Furthermore, this device will represent the top cell of our future dual junction solar cell.

Table 3.2 presents the general structure of the cell that we want to optimize (it has to be read from the bottom to the top). It is based on the structures presented in the previous section, in particular on the one presented by Jain *e al.* [13]. The elements indicated by a *X* have to be optimized, whereas what is directly shown can be considered as set.

The first point to notice is the choice of a p^+n polarity for the cell. This choice was motivated by the calculations presented in [13], but also by our higher expertise on the growth on and processing of n-type substrates (the metallization techniques and the metals available at III-V Lab make it easier to take a p-type contact on the InGaAs top contact and a n-type contact on the InP substrate than the opposite).

The choice of a n+ substrate was motivated by the target of reducing R_s [8]. The back surface field (BSF), which also act as a buffer layer for the growth, was basically fixed: its most important parameter is the doping level [22], which has to be significantly higher than the base one (which should be on the order of $-1\times10^{17}\,cm^{-3}$). We decided therefore to keep the same doping level of substrate. Although a higher bandgap material than the one composing the base is suggested, we chose to use InP as well, since the only other available material (AlInAs) has a bandgap too close to InP (especially for n-type doping) to make a significant difference.

The base thickness and doping level had to be optimized: although most of the devices presented in literature present thicknesses of $\sim 5\,\mu m$, we decided to test values around $3\,\mu m$ to limit the overall thickness (in prevision of the future integration in a dual junction device grown on Si). In general, the optimal thickness arises from the competition between the maximization of the absorption and the minimization of the induced R_s. The optimal doping

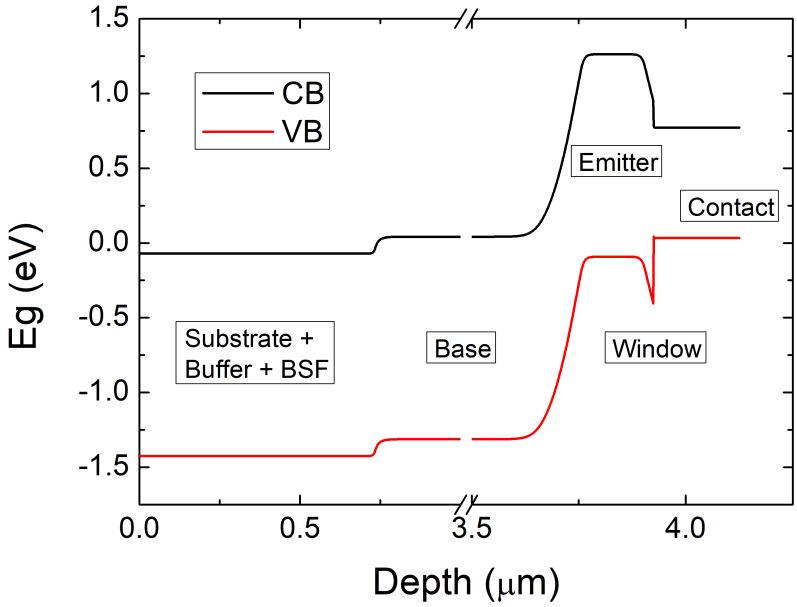


Figure 3.1: Simulated band alignment for an InP homojunction solar cell. The structure is the one presented in Table 3.2, with a 3 μm thick and -1×10^{17} cm^{-3} doped base, a 150 nm thick emitter, a 20 nm thick InP window and a 200 nm thick contact layer. The thickness of the substrate + buffer + BSF layer was reduced for a better overview. The simulation was performed by numerically solving the one-dimensional Poisson equation.

level is expected around -1×10^{17} cm^{-3} [16].

A non-intentionally doped (nid) zone of 20 nm thickness was placed between the base and the emitter. This is a very typical solution in p-n junctions (and in photovoltaic in particular) to reduce interdiffusion between the two opposite doped layers [23].

The emitter thickness was evaluated since the literature presents quite different results about this value (from some tens to around 200 nm). In contrast, the doping level was fixed at +1×10^{18} cm^{-3}: this is a very typical value for solar cells emitters, and furthermore the InP p-type doping is almost limited to this value [24, 25]. It also allowed the avoidance of bandgap-narrowing effects due to high doping.

The window layer bandgap, and consequently its composition (as well as its thickness and doping level), has to be chosen carefully: InP can be a good solution (despite, as said, we are very close to its doping saturation limit), but also lattice matched and mismatched AlInAs is a possibility.
Finally, an InGaAs contact layer can be highly doped with Zn to make an excellent, p-type ohmic contact. In this case, it was only necessary to grow

a thick enough layer to avoid metal diffusion into the underlying layers.

Figure 3.1 presents the simulated band alignment for a structure similar to the one presented in Table 3.2 (the details are given in the figure's caption). The simulation was performed by numerically solving of the one-dimensional Poisson equation.

In the next section, we will present the main structural aspects that had to be optimized for this device.

3.3 Growth of a cell

The growths of the buffer layer, the BSF and the base of the cells (all three InP-made) were performed by using Si as n-dopant. It was preferred to other typical n-dopants such as S because of its higher stability (10^{-11} Torr at 800 °C, [26]) and low diffusion coefficient in InP for typical growth temperatures [27]. The chosen precursor was disilane (Si_2H_6), since its doping yield is significantly higher than that of silane (SiH_4) [28]. The growth temperature was kept equal to that of intrinsic InP (680 °C) since it is demonstrated that there are no significant influences of the temperature on the doping level in the range 600-700 °C [29]. All these layers, as well as the ones presented afterwards, were grown at a reactor pressure of 150 mbar.

The growth of the p-type layers of the cells was performed at a lower temperature, $\sim$ 610 °C. This choice was motivated by the fact that Zn-doping is limited by exodiffusion due to the the volatile nature of this dopant [30]. Since the goal is to dope InP and InGaAs very close to their saturation level (1×10^{18} and $1\times10^{19}\,cm^{-3}$, respectively), it is necessary to reduce the growth temperature by some tens of degrees. At 610 °C, the concentration of incorporated dopant is proportional to the precursor flow [31]. This is true until the dopant reaches values close to its concentration limit.

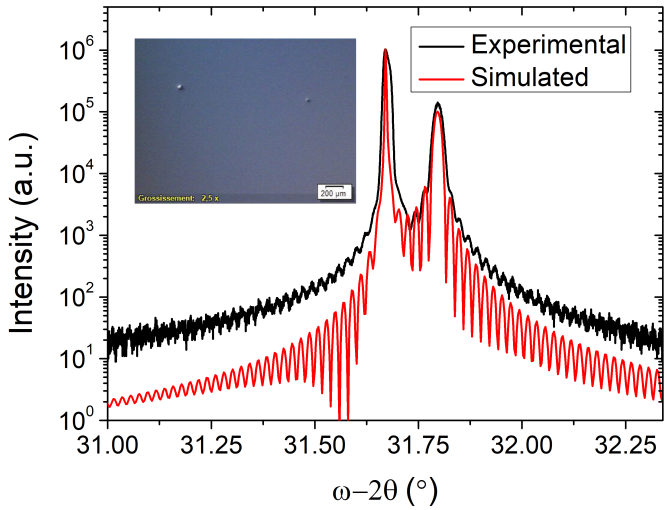
Two particular phenomena have to be taken into account when performing Zn-doping of an epitaxial structure: the diffusion and the deactivation. It is well known that the incorporation of such a dopant presents an abnormal behaviour [32, 33]: Zn penetrates in both substitutional and interstitial positions, and these last ones can diffuse inside the crystal. In InP, diffusion occurs in an excess of P-holes. It is possible to identify a double diffusion front mechanism [34, 35], composed of a shallow, 'slow' front with high Zn concentration and a deep, 'fast' front with low Zn concentration. This last one will partially diffuse inside the 20 nm thick nid layer, but it will be blocked when reaching a n-type doped layer. Deactivation is a very typical phenomenon in InP:Zn layers: by comparing SIMS and ECV measurements, it is possible to notice that a huge amount of the incorporated Zn is actually

Material (V/III ratio)	Function	dop/III ratio	Doping (cm^{-3})
InP (78.4)	Buffer/BSF n+	8.2×10^{-5}	-2×10^{18}
	Base n	3.9×10^{-6}	-1×10^{17}
	Emitter p+	1.3×10^{-2}	$+1\times10^{18}$
	Window p+	3.0×10^{-2}	$+1.5\times10^{18}$
$Al_{0.48}In_{0.52}As$ (16.0)	Window p+ (alternative)	3.3×10^{-2}	$+1.5\times10^{18}$
$Al_{0.60}In_{0.40}As$ (14.4)	Window p+ (alternative)	2.9×10^{-2}	$+1.5\times10^{18}$
InGaAs (11.1)	Contact layer	7.5×10^{-2}	$+2\times10^{19}$

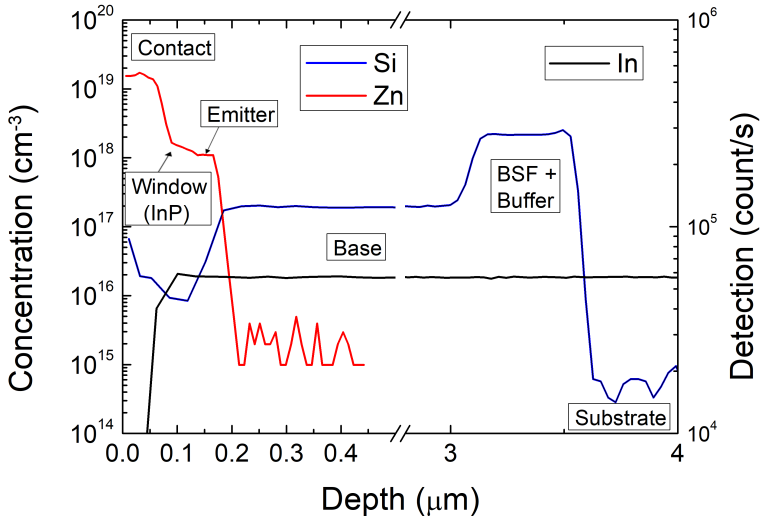
Table 3.3: V/III and some of the dop/III ratios (with respective doping levels) used during the growth of the solar cells (horizontal reactor).

passivated by formation of neutral Zn-H complexes [36]. Such a phenomenon is not affected by the H_2 gas vector flow, but rather by the hydrides flows, in particular AsH_3 [37]. The explanation has to be found in the low thermal stability of AsH_3 at typical growth temperatures: a huge amount of atomic H is released at the sample surface and diffuses inside the structure to bond itself with the Zn atoms [38]. The phenomenon is less affected by PH_3, since it has a higher thermal stability (and independent from H_2, even more stable). On the other hand, this phenomenon does not occur in InGaAs. The easiest solution to this problem is to cool the sample without hydrides flowing in the growth chamber: the already absorbed H will desorb because of the high temperature and it will not be substituted since no more species are injected into the reactor.

The V/III and dop/III ratios used in the various layers growths on the horizontal reactor are presented in Table 3.3. For minor doping variations, the precursors flows were changed proportionally to the desired value. Figure 3.2(a) presents the XRD scan (experimental and simulated curves in black and red, respectively) and, in the inset, the superficial morphology of a cell characterized by a 3 μm thick base ($-1\times10^{17}\,cm^{-3}$ doping level), a 150 nm thick InP emitter, a 30 nm thick InP window and a 200 nm thick contact layer (the remaining parameters are the same indicated in Table 3.2). Both characterizations demonstrate the high quality of the grown crystal, other than a completely smooth surface. Figure 3.2(b) presents the SIMS profile of a similar cell; the differences compared with the previous one lay in the different thicknesses of BSF + buffer (400 nm), emitter (60 nm) and contact layers (60 nm). This profile proves the homogeneity of the different doping levels.



(a)



(b)

Figure 3.2: (a) XRD scan of a grown solar cell (window in InP). The peaks intensities and widths prove the high crystalline quality of the growth. The InGaAs layer is strained at -250 ppm (49.5% of Ga content). In the inset is shown the morphology of the centre of the same cell. The quality is good despite the presence of some parasitic dust particles. (b) SIMS profile of In (majority element), Si and Zn (dopants) in the same sample. The different layers are easily recognizable (in this particular growth, the BSF + buffer thickness is lower than what was previously declared). We can appreciate the abrupt interfaces and the homogeneity of the dopings.

3.4 Processing

The processing allows us to transform the raw grown crystal into a complete device. In the next section, we will present in details all the developed steps that allow us to optimize this procedure. For the moment, we limit ourselves giving the basis of the whole process flow.

The first, main step in solar cell processing is the front contact metallization, presented in Figure 3.3(a). It consists of the deposition of a metallic layer on the surface of the cell to favour the extraction of the photogenerated carriers. The dimensions of this layer have to be reduced in order to limit the shading of the underlying semiconductor. The second main step consists of the electrical isolation of multiple small cells in the same sample. The interest arises from the isolation of local short-circuits on the plate. Although the most immediate solution is to cleave the sample into smaller

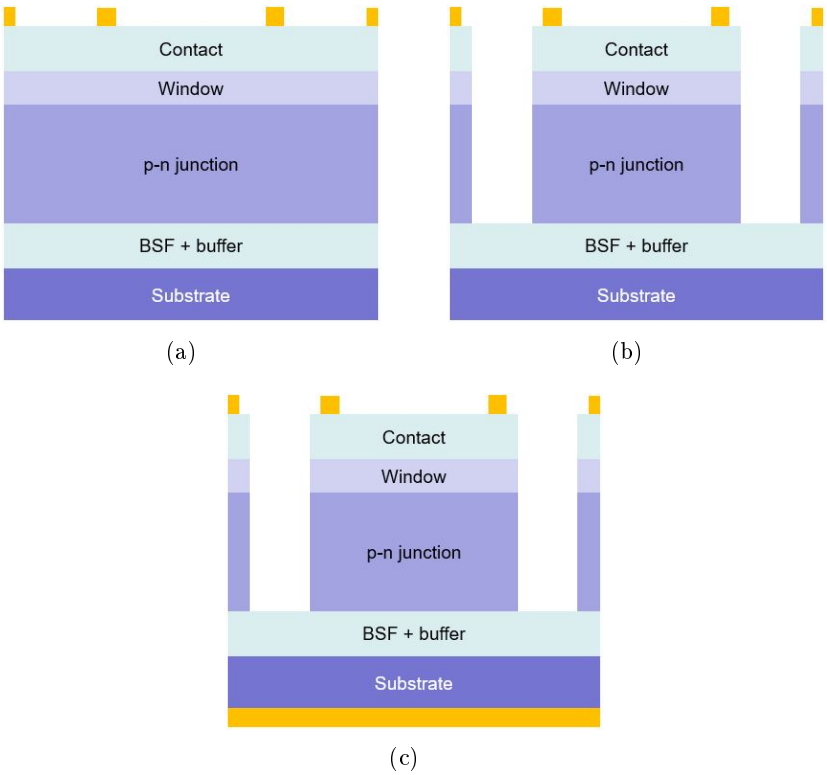


Figure 3.3: Main steps of solar cell processing: (a) Top contact metallization. (b) Mesa etching. (c) Back contact metallization.

pieces, Yamamoto *et al.* demonstrated that a so-called 'mesa etching' (presented in Figure 3.3(b)), consisting in separating the cells by etching the material between them until at least the p-n junction (thus avoiding the flowing of charges between different cells due to an electric field), guarantees better performances, since the cleaving affects V_{OC} by increasing the dark saturation current of the cells [5]. The third main step consists of the back contact metallization, presented in Figure 3.3(c): this step is very similar to the first one, although in this case a full plate deposition is possible since no light reaches the device from the bottom.

3.4.1 First generation of InP cells

The processing of the first cells was performed by using a dual layer of photolithographic masks inherited from a previous project. This set was designed for the processing of a 3" sample: the first layer, showed in Figure 3.4(a), is dedicated to the front contact metallization and the second, presented in Figure 3.4(b), to mesa etching. It allows us to realize a total of 38 squared cells on the same sample, 12 of 1 cm size and 26 of 0.5 cm size. Every cell presents two metallic busbars at two opposite edges and a series of fingers connecting the two busbars. The finger density defines the shading factor of the cell. The cells can present three different shading factors: 10% (4 big and 8 small), 5% (4 big and 9 small) and 3.3% (4 big and 9 small). The set also presents some patterns with which to perform transmission line measurements (TLM) and deep-level transient spectroscopy (DLTS), in order to evaluate respectively the front contact metal-semiconductor resistivity and the concentration of active defects, and two cells to perform QE measurements (similar to the photovoltaic cells but without fingers connecting the two busbars). The perfect alignment of the two layers can be performed thanks to a series of alignment crosses and other patterns presented in Figure 3.4(c) and repeated multiple times on the whole surface. Since our samples had a 2" diameter, we had to centre the mask on it, thus keeping only 4 big cells, 3 small cells, 1 QE cell and some TLM and DLTS patterns on the final device.

Although this set was useful for becoming familiar with the main aspects of a photovoltaic cell processing, it soon became clear that it was not adapted for our purpose for multiple reasons.

The first, obvious reason is the fact that the set is not optimized for a 2" wafer: every sample can finally present only 7 cells, making the process not very attractive. Consequently, the presence of large cells (1 cm size) is a limit, since they occupy a too large surface of the sample. Furthermore, the reduced dimensions make less attractive the presence of extended patterns such as diodes for DLTS measurements.

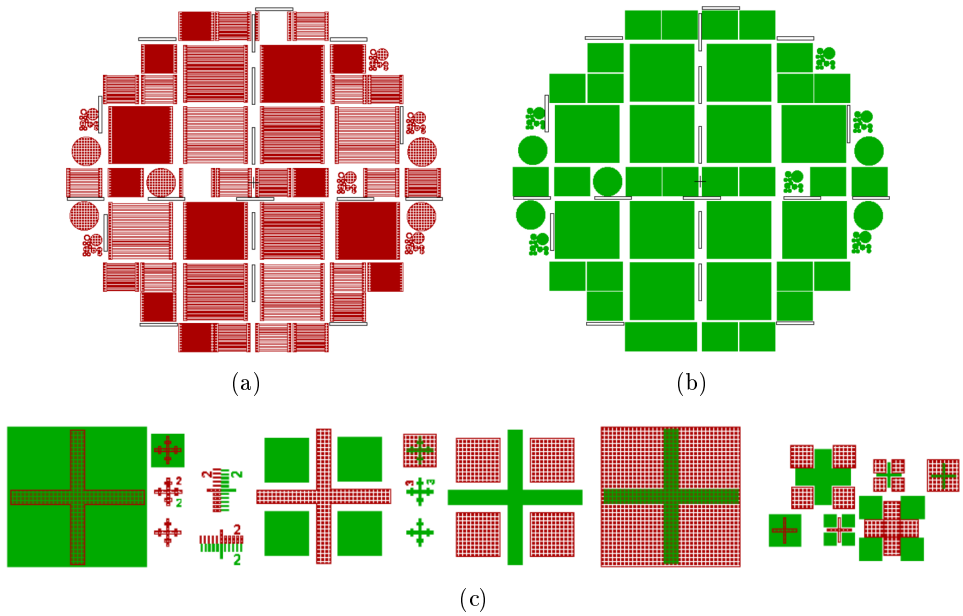


Figure 3.4: First photolithographic set: (a) Mask 1: front contact metallization. The red chessboards represent the metallized zones. (b) Mask 2: mesa etching. The green zones represent the not-etched parts. (c) Overlap of masks 1 and 2 for the alignment pattern (the whole length is around 3 mm).

Another problem arises from our contact layer: since InGaAs is very absorbent compared to InP, it is necessary to etch it away in order to allow radiation to reach the p-n junction without being absorbed. At the same time, the TLM measurements require that the InGaAs layer is not etched to better evaluate the metal-semiconductor contact resistivity. In conclusion, it is necessary to protect these patterns when etching InGaAs elsewhere, but this is not possible with the presented set. Furthermore, the TLM patterns are placed in very uncomfortable zones for measuring and present only linear configurations, without any circular (CTLM) one.

When depositing an ARC, the whole surface is covered. This presents a problem during the electrical characterization of the devices, since the bus-bars are covered and the ARC is too hard to be scratched away from them, thus impeding the measuring. It is thus necessary to protect the ARC deposited on the semiconductor during the physical or chemical removal of the one deposited on the metal. Initially, we used the first mask for a second time to perform lithography, but the reduced dimensions of some patterns made it impossible to perfectly match the mask with the previously deposited metal. Last, but absolutely not least, the shape of the alignment patterns: as we can see from Figure 3.4(c), some metallic layers are not protected during the mesa etching (where the red zones are not superposed to the green ones).

This fact makes the physical dry etching of the mesas impossible, since the metal cannot be directly exposed to the etching plasma, thus leaving the wet chemical etching as the only possible technique for the mesa realization.

3.4.2 The new set of masks

All the problems characterizing the older set and presented in the previous section were solved with the new set, realized with the L-Edit software. The number of available devices on the same sample was maximized by designing an optimized set for a 2" plate and removing all the bigger cells and DLTS patterns. The new design presents a total of 30 squared cells of 0.5 cm size: 26 solar cells (of which 8 present a 10% shading factor, 10 a 5% and 8 a 3.3%), 2 QE cells and 2 so-called 'TLM cells'. The cells are homogeneously distributed on the whole surface to reduce the incidence of any local defects. The distribution is symmetric with respect to the diameter perpendicular to the sample primary flat (only the QE and the TLM cells are inverted in the two sides) in order to make the cleaving of the sample possible to test two different processings in the same condition. The sides of the cells are parallel to the primary and the secondary flats of the sample since these are the crystal preferential cleaving directions. It is worth remembering that the 3-5 mm thick most external ring of the sample has to be considered inappropriate for the realization of devices since this zone can present some border inhomogeneities due to the epitaxy, the processing or the simple fact of being in the area that the tweezers grip the sample.

The problem of the incomplete protection of the metallic patterns constituting the alignment system was solved by introducing a preliminary mask (aligned along the primary flat), dedicated to the etching of some alignment crosses inside the bulk structure and presented in Figure 3.5(a) (the blue zones represent the etched sectors). All subsequent masks have to be aligned on some of these crosses, and the homogeneous distributions of such a pattern guarantees a highly satisfying alignment. The front metallization mask and the mesa etching mask, represented in Figures 3.5(b) and (c) respectively, are quite similar to the ones of the previous set.

The TLM patterns were grouped to simplify the contact resistivity measurements. We thus obtained a TLM cell, repeated twice in the device: every cell is characterized by two different patterns for linear TLM (both repeated twice) and a CTLM pattern. The advantage of this configuration arises from the fact that it does not need an etching step to isolate it from the surrounding zone [39]. The cell also presents a ring in a corner, which allowed us to open a window on the semiconductor surface to follow the dry etching of ARC. In order to protect these cells during the etching of the InGaAs contact layer, we introduced a fourth mask, depicted in Figure 3.5(d), corresponding of two simple squares in correspondence to the TLM cells. Figure 3.6(b)

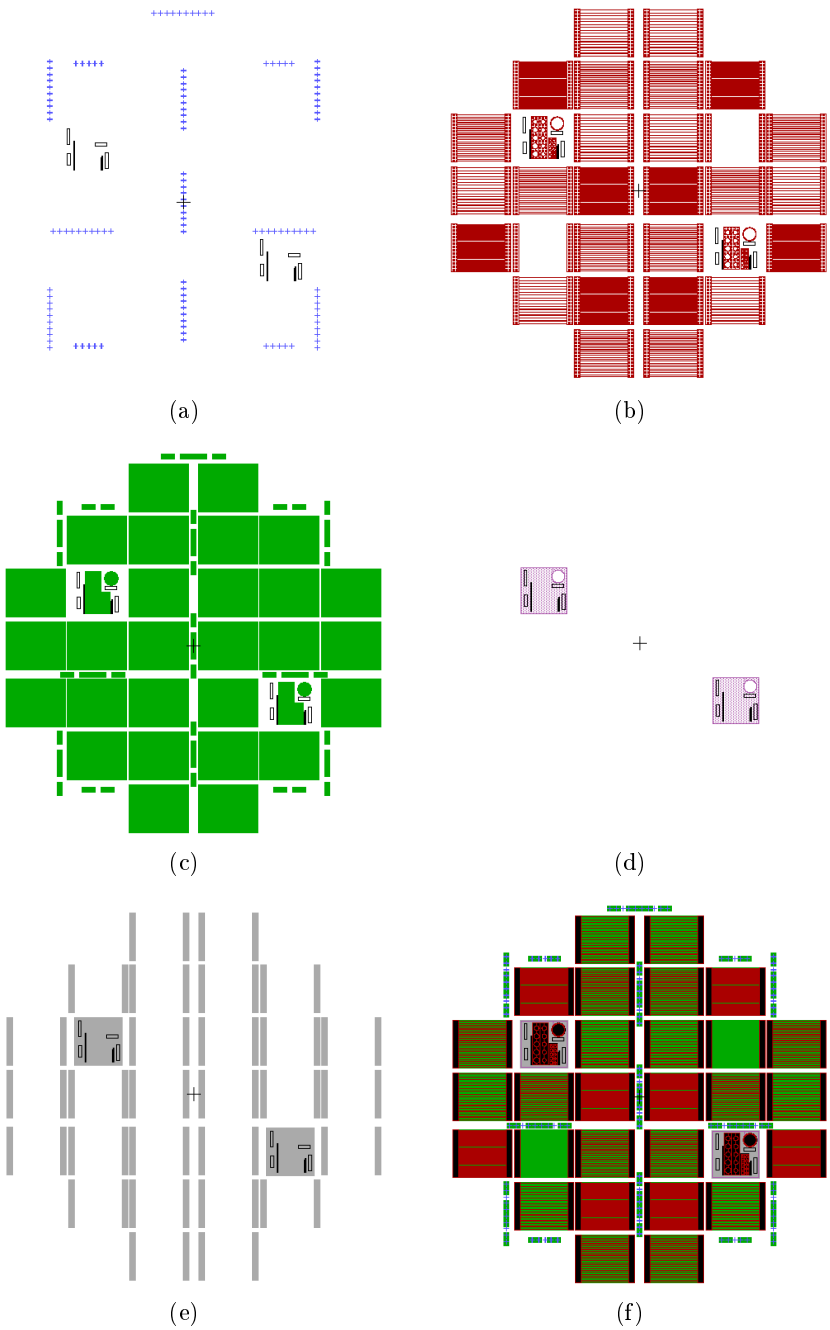
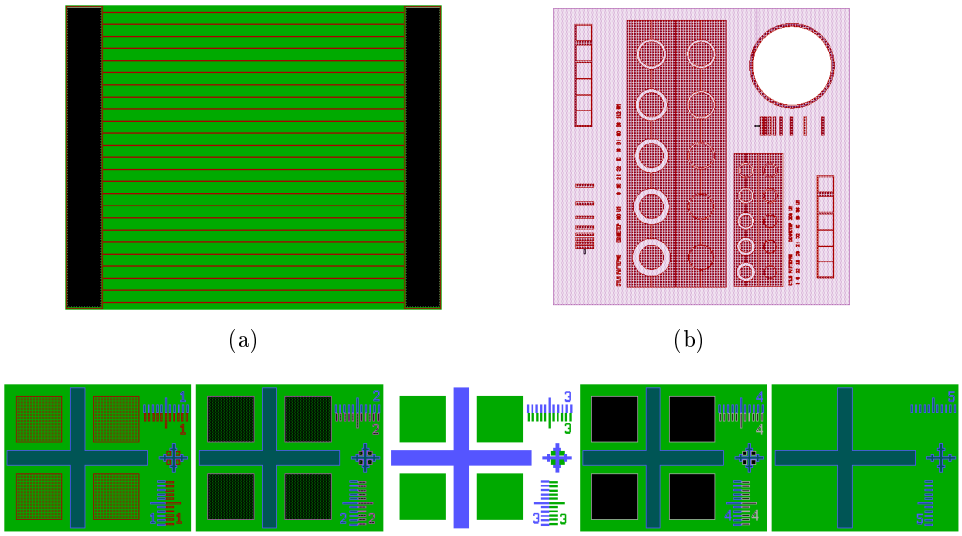


Figure 3.5: Second photolithographic set: (a) Mask 1: alignment patterns etching. The blue zones represent the not-etched parts. (b) Mask 2: front contact metallization. The red chessboards represent the metallized zones. (c) Mask 3: mesa etching. The green zones represent the not-etched parts. (d) Mask 4: InGaAs contact etching. The pink dotted zones represent the not-etched parts. (e) Mask 5: ARC opening. The grey zones represent the opened parts. (f) The whole set.



(a) (b)

(c)

Figure 3.6: (a) Example of 0.5 cm side cell (5% shading factor). We can identify the masks 2, 3 and 5. (b) Example of a 'TLM cell'. Only the layers 2 and 4 are shown. We can identify two different TLM patterns (both repeated twice), a CTLM pattern and a detection ring (it acts as a target for laser detection of the thickness during dry etching). (c) Overlap of all the masks for the alignment pattern. We can notice that all the metallic parts (red chessboards) are protected during the mesa etching.

presents an example of these cells (only the second and the fourth mask are showed, for a greater clarity).

The problem of the covering of the front metallic contact by the ARC was solved with the introduction of a fifth mask, represented in Figure 3.5(e). Once the ARC is deposited everywhere, 'windows' are opened in correspondence to the busbars and to the TLM contacts (that is, where the carriers can be extracted or injected). The second, the third and the fifth masks compose the final solar cell shape, as shown in Figure 3.6(a).

The whole set is depicted in Figure 3.5(f), whereas Figure 3.6(c) represents the new alignment system. Zone 1 is dedicated to the alignment of the metallization mask, zone 2 to the one of the InGaAs contact etching mask, zone 3 to the one of the mesa etching mask, zone 4 to the one of the ARC opening mask and zone 5 is preventively dedicated to an eventual, future mask. It is important to notice that, with this new set, all the metallic parts are covered and protected during the mesa etching step, thus making possible a physical, dry etching.

3.4.3 Main processing steps

In the next three paragraphs, we will present in more details the main processing steps: the front contact metallization, mesa etching (the etching of the alignment crosses introduced with the first mask of the new set is developed in the same way) and ARC coating. We will present the various stages that compose each step, highlighting the most critical points.

Metallization The p-type front contact of our cells was made with a 150 nm thick Pt layer followed by a 250 nm thick Au layer deposited on the InGaAs upper layer. The different stages of this step are presented in Figure 3.7: the cell (a) is covered with a spin-coated resist (b), then it undergoes photolithography (c) and development (d). The metal is deposited (e) and the remaining resist is lifted off (f), leaving the metal only where it is needed.

During this thesis, three different metallization techniques were performed: Inductively Coupled Plasma (ICP) for the very first tests, and Dual Ion Beam Sputtering (DIBS) and Evaporation during most of the thesis. These two techniques are differentiated by their degree of directionality (DIBS is anisotropic, whereas evaporation is isotropic). The evaporation technique should be preferred for the front metal deposition since the deposition zones are small and partially masked by the resist itself, while sputtering should be preferred for the full plate back contact deposition. Anyhow, the adopted technique does not seem to have a real influence on the final performances, as demonstrated by TLM and CTLM measurements, which gave similar results for both the techniques, as shown in Figure 3.8: a contact resistivity ρ_c of the order of $10^{-6}\,\Omega{\cdot}\mathrm{cm}^2$ is sufficiently low for our purpose.

In all these techniques, metal deposition was performed after a preliminary surface sputtering with a neutral Ar plasma. Such a treatment has the double effect of cleaning the surface and favouring the adhesion of the metallic atoms on the semiconductor.

The formation of a good ohmic contact between p-doped InGaAs and Pt/Au requires that the layers undergo rapid thermal annealing (RTA): a one minute annealing at 400 °C in a forming gas (a mixture of H_2 and N_2) is essential for an efficient metal diffusion inside the semiconductor.

The n-contacts were realized with the same techniques directly on the back side of the substrate. The metals used were Ti (50 nm), Pt (75 nm) and Au (250 nm). Also, in this case, the metal deposition had to be performed after a neutral Ar plasma etching to remove the superficial impurities of the semiconductor (in this case, the treatment had to be more intense and extended in time since the surface generally presents a lower quality). The

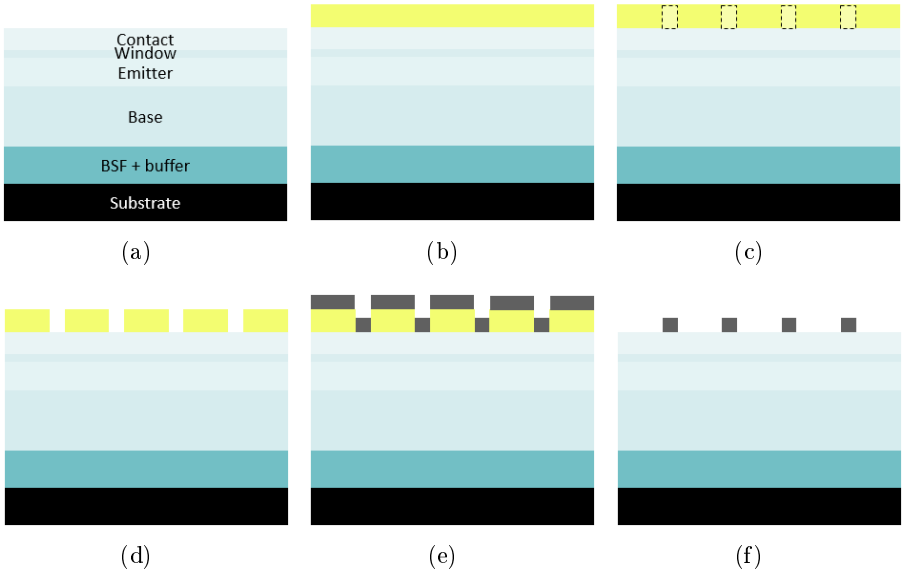


Figure 3.7: Front contact metallization: (a) Initial structure. (b) Resist spin-coating. (c) Lithography. (d) Development. (e) Metallization. (f) Lift-off.

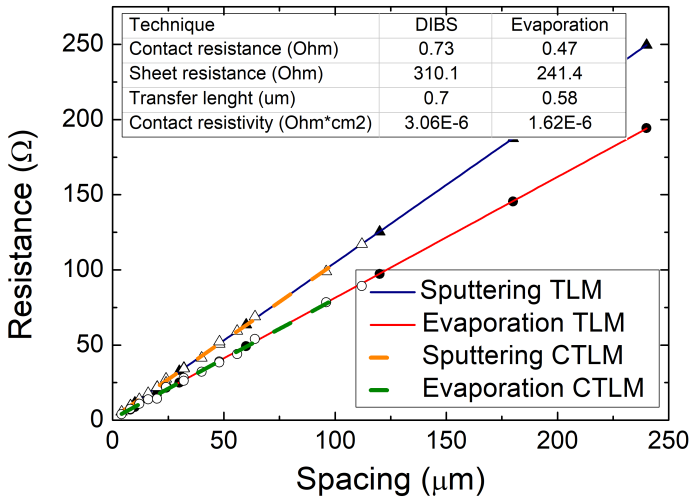


Figure 3.8: Comparison of the contact resistivities of metallic layers deposited by sputtering and evaporation and measured by both TLM and CTLM. All the results are sufficiently low for a solar cell front contact (order of $10^{-6}\,\Omega{\cdot}\mathrm{cm}^2$).

formation of a n-type ohmic contact between InP and Ti/Pt/Au does not require any type of annealing.

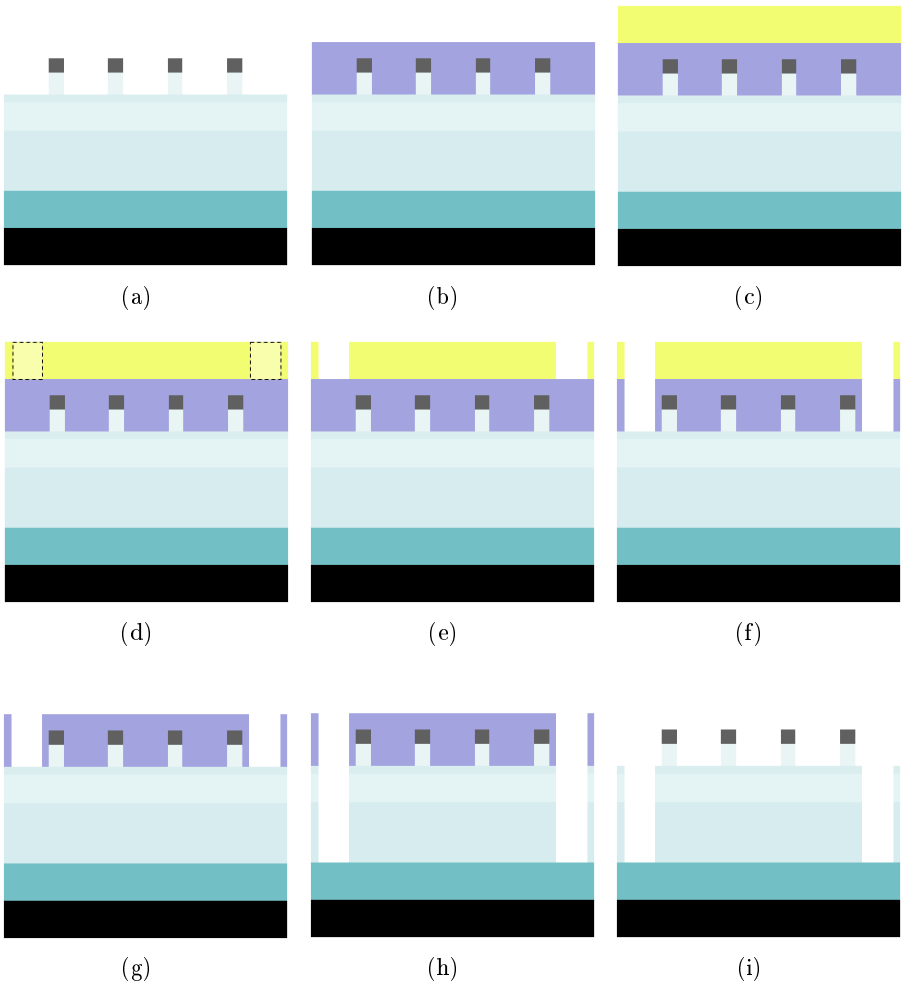
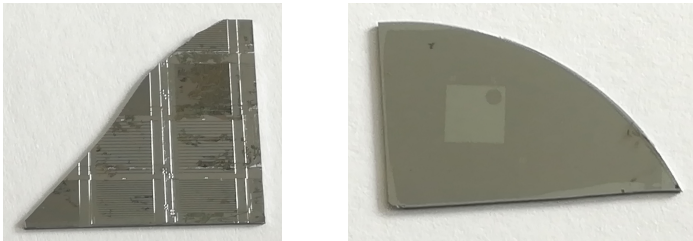


Figure 3.9: Mesa etching: (a) InGaAs etching. (b) SiO_2 deposition (PECVD). (c) Resist spin-coating. (d) Lithography. (e) Development. (f) SiO_2 etching. (g) Resist removal. (h) Mesa etching. (i) SiO_2 removal.

Mesa etching This step aims at electrically isolating the different cells. Figure 3.9 presents the various stages of this process: first of all, the InGaAs contact layer is etched (a). This step can be indistinctly postponed at the end of this step, just before the ARC deposition. An additional lithography step has to be added to protect the TLM patterns. The sample is then covered by a SiO_2 layer (b) deposited by Plasma-Enhanced Chemical Vapour Deposition (PECVD). The mesa patterns are realized by photolithography of a resist (c-e), transferred to the semiconductor surface by chemical or physical etching of the oxide (f). The resist is removed (g), then the mesa etching is chemically or physically performed (h) and the oxide is finally removed (i).



(a) (b)

Figure 3.10: Final superficial morphology of an InP test layer etched by (a) HCl:H_3PO_4 (1:3) (b) HCl:H_2O (1:5) solutions. In the first case, the bubbles generated during the reaction locally 'mask' the etching. The result is a very wrinkled morphology, whereas the second solution guarantees a very smooth, final morphology.

The etching of the InGaAs contact layer was always performed in a chemical way, as it can be easily, selectively etched from InP with a H_3PO_4:H_2O_2:H_2O solution in a 3:1:80 concentration [40]. The measured etching rate is $\sim$ 50 nm/min.

The mesas can be obtained by wet or dry etching. In the first case, two different solutions were initially tested: HCl:H_3PO_4 (1:3) [41] or HCl:H_2O (1:X) [42]. It is not possible to give an absolute etching rate since in the first case it is highly influenced by the doping of the layers (in fact, we noticed that the etching accelerates and slows down multiple times during the process) and in the second case of course by the HCl dilution. We noticed that the final morphology is very different in the two cases: the first reaction produces some bubbles on the semiconductor surface, which can have a 'masking' effect, therefore leaving a very wrinkled surface, as shown in Figure 3.10(a). This problem does not occur with a HCl:H_2O solution, as showed in Figure 3.10(b).

The physical, dry etching can instead be obtained with an active $H_2/Ar/Cl_2$ plasma (ICP).

ARC coating It is well known that InP-based devices present a high amount of electrical losses at the edges of the crystal, arising from unsaturated chemical bonds at the surface. This fact is particularly important for solar cells, since these losses can highly increase J_s. It is therefore very important to passivate the InP by saturating this bonds. At III-V Lab, this passivation is performed by depositing a Si_3N_4 layer. Luckily, this nitride can also be used as an ARC for InP solar cells [43]. In order to optimize this layer for both functions, it is necessary to determine its correct thickness t from the relation:

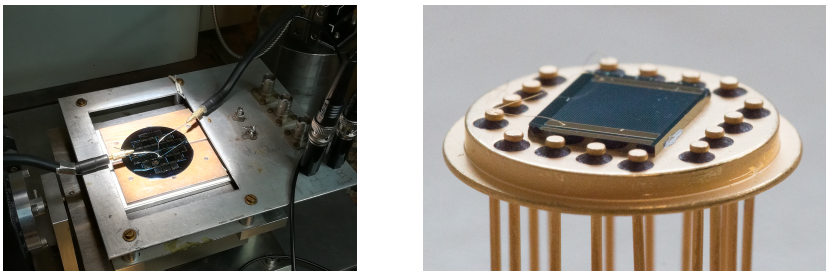
$$t = \frac{\lambda_{InP}}{2\,n^2} \tag{3.1}$$

where λ_{InP} is the maximal absorption wavelength of InP (925 nm) and n is the refractive index of Si_3N_4. Literature presents values between 1.95 and 2.05; we determined by reflectometry that our nitride has n $\sim$ 2. In conclusion, the optimal thickness to maximize the absorption is 115 nm.

The Si_3N_4 ARCs were deposited by PECVD at 245 °C. The windows in correspondence of the metallic busbars were opened by Reactive Ion Etching (RIE), with a CHF_3/O_2 (50/2 sccm) plasma.

3.5 Characterization

The final devices were tested at the Group of electrical engineering of Paris (GeePs). The J-V measurements were performed with an Oriel Instruments 81192 solar simulator (102x102 mm^2, 1 KW, spectrum AM1.5G). Before every set of measurements, the simulator state was analysed and corrected if necessary with GaAs and Si calibration cells. The measures were taken with Keithley 2400 and 2450 sourcemeters. The SR/EQE measurements were performed by a Fourier Transform Infrared Spectrometer (FT-IR). The instrument was modified to also perform Fourier Transform Photocurrent Spectroscopy (FT-PS), allowing us to evaluate RS/EQE with a few seconds delay ($<$ 5 s) with a 1 nm resolution. Some reference cells were used to calibrate the incident flow. The J-V measures were taken in a 4-wires configuration, the front contacts were taken with two probes placed on the two opposite busbars of each cell, while the double back contacts were directly



(a) (b)

Figure 3.11: (a) J-V characterization of a sample under a 1-sun AM1.5G spectrum at GeePs. (b) Example of a single cell wire bonded (Au soldering) to a holder at IES.

taken on a back conductive plate. This fact allowed us to keep the plate intact, facilitating the measurement (the probes can be moved from one cell to another), as showed in Figure 3.11(a).

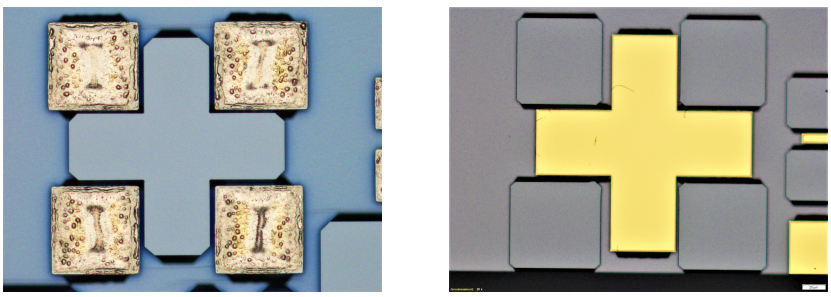
In some cases, the measurements were also performed at the IES of Montpellier and at the Department of Physics of the University of Lancaster (2-wires configuration). In these cases, the single cells had to be separately cleaved and wire bonded with Au soldering to proper holders before the measurements, as shown in Figure 3.11(b).

3.6 Main results

3.6.1 Horizontal reactor samples

The very first test structure (sample A) presented a 400 nm thick buffer/BSF layer (-2×10^{18} cm^{-3} doping level), a 3 μm thick base (-2×10^{17} cm^{-3}), a 20 nm thick transition layer (nid), a 60 nm thick emitter (+1×10^{18} cm^{-3}), a 30 nm thick InP window (+1.5×10^{18} cm^{-3}) and a 60 nm thick InGaAs contact layer (+2×10^{19} cm^{-3}). The SIMS profile of this structure was already presented in Figure 3.2(b).

Processing of this sample was quite simple: the first masks set was used, and the front and the back contact metallizations were performed by ICP. The annealing of the p-type metal-semiconductor contact was performed in a non optimal furnace: even if the temperature reached the desired value (400 °C) in a few seconds, the cooling took more than half an hour (instead of a few minutes). This fact had a strong impact on the front metals: as shown in Figure 3.12(a), taken by optical microscopy on an alignment pattern, the too-long exposition of Pt/Au at high temperatures caused a degradation and a hyper-diffusion of the metals inside the devices. This second



(a) (b)

Figure 3.12: Effects of a (a) slow and (b) rapid cooling of the device after annealing (samples A and B respectively). Too long time at high temperatures strongly affects the quality of the deposited metals.

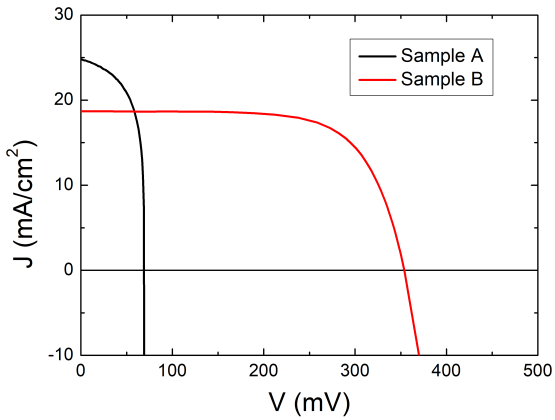


Figure 3.13: J-V characteristic of the best cells of samples A (black line) and B (red line) under illumination. In sample A (black line), the very low V_{OC} suggests a short circuit, probably caused by metallic diffusion. The problem is partially solved in sample B by increasing the contact layer thickness and performing a proper post annealing cooling down of the sample.

	A (5 cells average)	A (best)	B (7 cells average)	B (best)
J_{SC} (mA/cm^2)	23.5	24.8	19.9	18.6
V_{OC} (mV)	65.4	67.3	316.8	354.1
FF (%)	58.2	65.4	66.2	69.3
η (%)	0.91	1.09	4.10	4.56

Table 3.4: Obtained photovoltaic parameters in samples A and B (mean and best cells values. These last curves are presented in Figure 3.13).

phenomenon was also caused by a too-thin contact layer. The mesa etching was performed in the chemical way. In Figure 3.12(a) we can appreciate the different crystalline plans revealed by the anisotropic etching, in particular the (1 1 0) direction. This is a proof of the quality of the chemical reaction. No ARCs were deposited on this sample.

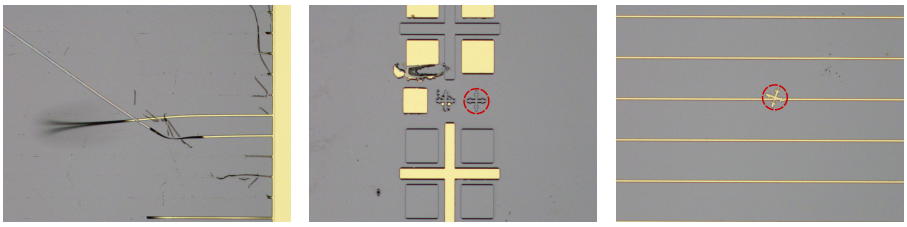
The J-V characteristic of the best cell of sample A is represented by the black curve in Figure 3.13: we obtained a J_{SC} of 25 mA/cm^2, a V_{OC} of 67 mV, a FF of 65.4% and a η of 1.2%. The mean values are quite similar, as presented in Table 3.4. The very low value of V_{OC} suggests that the cell is short-circuited (we can also evaluate a high contribution of R_{sh} from the slope of the curve at low applied voltages): this fact is in line with the observed effects of the non-optimal cooling down. In conclusion, what we could deduce for this first device is the importance of a proper post annealing cooling down, and it is also important to increase the thickness of the InGaAs contact in order to reduce the influences of strong metallic diffusions.

Sample B was therefore realized with a similar process, but this time increasing the thickness of the InGaAs contact layer from 60 nm to 200 nm and performing the annealing in a proper furnace. In this case, the duration of the cooling down has been reduced to about five minutes (the temperature took a few tens of seconds to descend below 200 °C). These accuracies allowed us to avoid the previous problems, as shown in Figure 3.12(b). The photovoltaic parameters of the new sample were then appreciably improved. As shown by the red curve of Figure 3.13, it presents a best device characterized by a 18.6 mA/cm^2 J_{SC}, a 354.1 mV V_{OC}, a 69.3% FF and a 4.56% η. The improvement is particularly evident at the V_{OC} level, and an important reduction of the R_{sh} is notable as well. Unlike sample A, no cells were completely lost during the process (complete short circuit). The mean values of sample B are also reported in Table 3.4.

Although the photovoltaic performances are sensibly increased, the results are very far from those of an optimal device. This is particularly true for V_{OC}.

In order to increase V_{OC}, and consequently η, of our devices, we carried out major changes to the whole structure in sample C. First of all, the emitter thickness was increased from 60 nm to 150 nm since, as demonstrated in [8], it has a strong impact on the voltage. Since this increase may reduce the J_{SC}, we tried to prevent this fact by halving the base doping to -1×10^{17} cm^{-3} [16]. The thickness of the BSF layer was increased to 800 nm to promote the absorption.

Another important change was performed by adding the previously presented Si_3N_4 ARC. In fact, the addition was primarily motivated by the passivating nature of this nitride: we expected a significant reduction of J_s and, consequently, an increase of V_{OC}. Of course, the anti-reflective function should increase the photovoltaic performances as well. Also, the front and back contact deposition techniques were changed, since they were performed



(a) (b) (c)

Figure 3.14: Sample C: local effect of BOE exposition on InGaAs layers containing diffused metals: (a) partial and (b) complete detachments of patterns and (c) casual re-depositions.

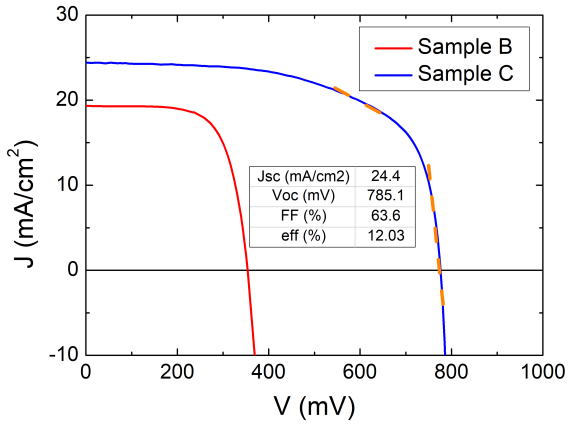


Figure 3.15: J-V characteristic of the best cell of sample C (blue curve) with the correspondent photovoltaic parameters. For comparison, the characteristic of the best cell of sample B is presented as well. A double resistance (orange dashed lines) at high applied voltages affects the FF.

by sputtering (this was simply due to a logistic choice; there are no scientific reasons).

During chemical removal of SiO_2 after the mesa etching (stage (i) of Figure 3.9) we noticed a surprising phenomenon, depicted in Figure 3.14: the thinner metallic patterns, such as the cells fingers and the smaller alignment cross, were sometimes partially (a) or completely (b) detached and re-deposited elsewhere (c) on the sample. This fact was more relevant at the edges of the sample and almost irrelevant at the centre. Since not only the metals, but also the InGaAs, seem to leave the sample in these zones, we concluded that the phenomenon was due to a reaction between the Buffered Oxide Etch (BOE) etchant and the metal-charged InGaAs. The different metal deposition technique compared to samples A and B may explain a different metal/semiconductor interconnection and thus a different reaction at the BOE exposition. In conclusion, we decided to exclude the expositions of the samples to BOE after the first metallization step.

The cells affected by BOE etching presented very low performances. However the four cells at the centre were characterized by almost identical photovoltaic parameters: the slightly better cell characteristic is presented in Figure 3.15, in comparison with the previous sample: while J_{SC} did not present a very significant change (24.4 mA/cm^2), V_{OC} jumped to 785.1 mV and, consequently, also η increased to 12.03%. Unfortunately, the appearance of a double series resistance (orange dashed lines) has limited FF, which did not exceed the 63.6%. This double resistance was present in all the four

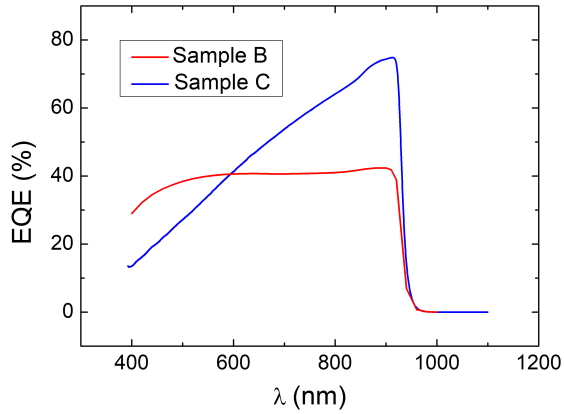


Figure 3.16: Comparison of the measured EQEs for samples B (red curve) and C (blue curve). This second one presents a significantly higher absorption, in particular for longer wavelengths.

good devices of sample C and we could not find a satisfactory explanation for the phenomenon. Perhaps the BOE had an effect on the central devices as well, but this does not explain why two different contributions to the series resistance do not simply add up.

Figure 3.16 presents a comparison between the measured EQEs of samples B and C: the notably higher quantum efficiencies for longer wavelengths can be explained by a lower reflectivity (introduction of the ARC) and lower rear surface recombination / higher absorption (thicker BSF and more proper thicknesses and doping levels at the p-n junction), respectively.

The obtained result is quite interesting in terms of efficiency and can be considered as a top cell for a dual junction device. Nevertheless, it can be interesting to introduce a higher bandgap window layer in order to reduce the front surface recombination and increase the EQE value for shorter wavelengths.

Samples D and E were grown by substituting the InP window layer with equally doped, 30 nm thick $Al_xIn_{1-x}As$ layers. In sample D, the AlInAs was lattice matched on InP (x = 0.48), as proposed in [17]; in sample E, a higher bandgap ($\sim$ 1.8 eV), lattice mismatched (-0.84%) layer with x = 0.60, as proposed in [19], was tested. The growth conditions (temperature, pressure) were the same as the previous windows, and the V/III and the dop/III ratios were given in Table 3.3.

The thickness and the composition of the mismatched layer of sample E were determined by XRD (Figure 3.17). Due to an experimental mistake, the measured curve (black line) does not cover the whole, correct angular range (not all the tensile strained peak was detected). Nevertheless the missing in-

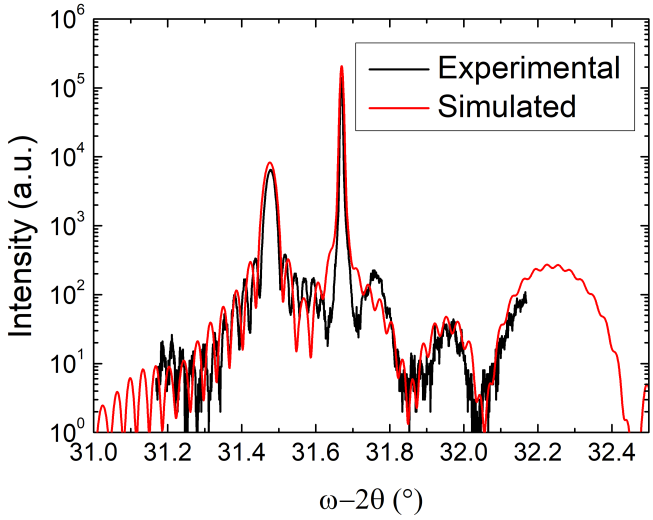


Figure 3.17: XRD plot of sample E, comparing experimental (black line) and simulated (red line) curves. The mismatched $Al_xIn_{1-x}As$ window layer presented a thickness of 26 nm and a composition x = 59%.

formation was recovered by simulations (red line). The best fit was obtained by considering a 26 nm thick layer with a composition of x = 0.59 (-0.77% lattice mismatch). On the other side the InGaAs contact presents a slight compressive strain, which should not much affect the final performances.

The processing of these devices presented significant changes compared to the previous samples. First of all, the new set of masks was introduced (Figure 3.18). The front contact deposition was performed by sputtering, and the back one by evaporation. The alignment patterns and mesa etchings were performed by ICP. Also, etching of the InGaAs contact layer needed some changes: first, this step was postponed after mesa etching in order to limit the oxidation of the Al-rich window (the ARC deposition was performed immediately after InGaAs etching); second, it was necessary to determine a new etching solution, since the H_3PO_4:H_2O_2:H_2O (3:1:80) is not selective at all for As-based materials (so, both InGaAs and AlInAs). The relatively high ratio between the two thicknesses (the InGaAs layer is approximately 7 times thicker than the AlInAs one) requires a selectivity $\gg 7$. A possible solution was given by a $C_6H_8O_7$:H_2O_2 mixture [44]: if $C_6H_8O_7$ (citric acid) is sufficiently diluted in H_2O_2, it has a very low influence on AlInAs. Since $C_6H_8O_7$ is a salt in standard conditions, it has to be diluted in de-ionized H_2O to perform this solution (1 g $C_6H_8O_7$:1 ml H_2O). Since the reaction between $C_6H_8O_7$ and H_2O_2 is endothermic and the temperature affects the etch rate, we performed the reactions in a thermostatic bath and always waited

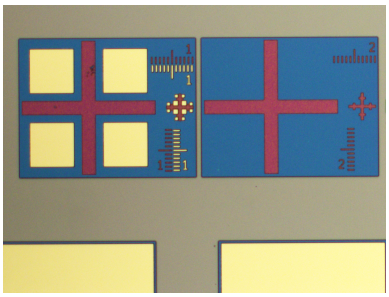


Figure 3.18: Detail of the surface's status after the dry mesa etching with the second set of photolithographic masks: the SiO_2 layer, not yet etched away, protects every metallic part (in yellow). The blue parts correspond to the InGaAs contact and the red ones to the etched InP; both are covered by SiO_2. The different colours are due to different thicknesses of the oxide (different etching rates for different depths). The grey parts correspond to the InP surface at the bottom of the mesas.

	D (window etched)	E (window etched)	F	G
J_{SC} (mA/cm^2)	18.8	19.6	14.8	18.8
V_{OC} (mV)	240.0	220.0	720.0	800.1
FF (%)	62.5	62.1	59.1	52.5
η (%)	2.83	2.67	6.30	7.52

Table 3.5: Photovoltaic parameters of the best cells of samples D, E, F and G. D and F present an $Al_{0.48}In_{0.52}As$ windows layer, whereas E and G an $Al_{0.60}In_{0.40}As$ one. In samples D and E the window layers were etched by mistake, in F and G all the cells except the ones presented were characterized by very low efficiencies (2-4%).

at least 5 minutes between the mixture preparation and the beginning of the etching to give time for the system to go back to the room temperature. By testing a $C_6H_8O_7$:H_2O_2 (1:2) solution, we determined a selectivity of ~ 60.

Unfortunately, during etching of the InGaAs contact layers of samples D and E, the effective selectivity of the $C_6H_8O_7$:H_2O_2 solution had proven to be completely different from the previously measured one, completely etching the two $Al_xIn_{1-x}As$ layers. New tests allowed us to understand how the degradation of the solution, due to the H_2O_2 presence, had an impact on the selectivity comparable to that of concentration and temperature. Samples D and E consisted then, basically, of sample C without a window layer. All the measured cells presented very low performances, and the best measured efficiencies, reported in Table 3.5, were 2.83% and 2.67%, respectively.

Since aging of the $C_6H_8O_7$ solution can be very aleatory, we decided to come back to the previous H_3PO_4:H_2O_2:H_2O solution, adding an interme-

diate 10 nm thick InP layer stop etch ($+1.5\times10^{18}\,cm^{-3}$) between the two As-based layers that had to be etched before the Si_3N_4 deposition. The front and the back metallic contacts of both the samples were deposited by evaporation.

The obtained results on samples F and G ($Al_{0.48}In_{0.52}As$ and $Al_{0.60}In_{0.40}As$ window layers, respectively) were quite surprising: most of the cells presented very low performances, comprised between 2% and 4%. Only one device for each sample presented significantly higher efficiencies (6.30% and 7.52%, respectively). In general, we noticed that the most limiting factors were the V_{OC}s, usually comprised between 200 and 300 mV, a fact suggesting a strong influence of the dark saturation current. Interpolating the corresponding dark J-V characteristics with equation 1.1 (page 3). We confirmed that the J_S of these devices presented very high values for solar cells ($\sim 10^{-5}\,A/cm^2$). Although at this stage it was difficult to identify a specific cause for this behaviour, we could conclude that samples F and G (and possibly either D and E) were affected by a damaging step which induced important electrical losses. Since some cells were (partially and, apparently, randomly) saved from this phenomenon, we could deduce an inhomogeneous influence of such a limiting factor.

3.6.2 Vertical reactor samples

In the second part of the thesis, the growths of the cells were performed in the new vertical MOVPE reactor. Although the growth conditions were nominally the same than in the horizontal reactor, the first step consisted of the validation of the new reactor. In order to achieve this goal, we again grew the structure of sample C with the new reactor: sample H is therefore supposed to present similar photovoltaic performances, although some discrepancies due to the new processing (new masks and dry etching) had to be taken into account.

The various cells of sample H presented a behaviour very similar to those of cells D-G: most of them were characterized by very poor photovoltaic parameters, whereas only 4 cells showed a reasonable behaviour. The J-V characteristic of the best cell of sample H is presented in Figure 3.19, in comparison with the record of sample C. As it is possible to notice, all four parameters are slightly lower in the new cell (although the characteristic double series resistance of sample C seems to disappear and can be, therefore, imputed to a structural defect developed during the previous growth). The average parameters for the working devices were $23.2\,mA/cm^2$ for J_{SC}, 719.0 mV for V_{OC}, 58.3% for FF and 9.72% for η.

The repetition of the same limiting phenomenon manifested in the previous samples on an already validated structure focused the attention on

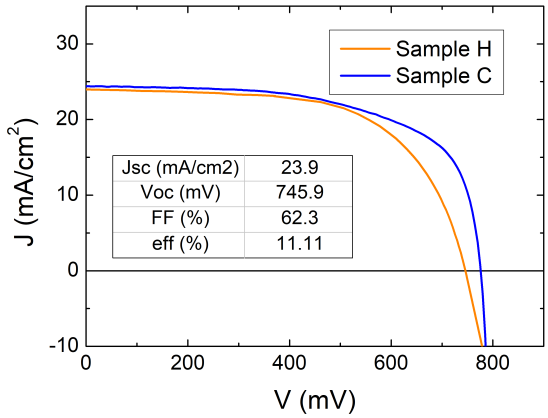


Figure 3.19: J-V characteristic under illumination of the best cell of sample H (orange line), compared with the one obtained with sample C (blue line). The structures were the same, in order to validate the new vertical reactor (although part of the processing was modified with time). It is possible to notice that the new device is slightly lower performing.

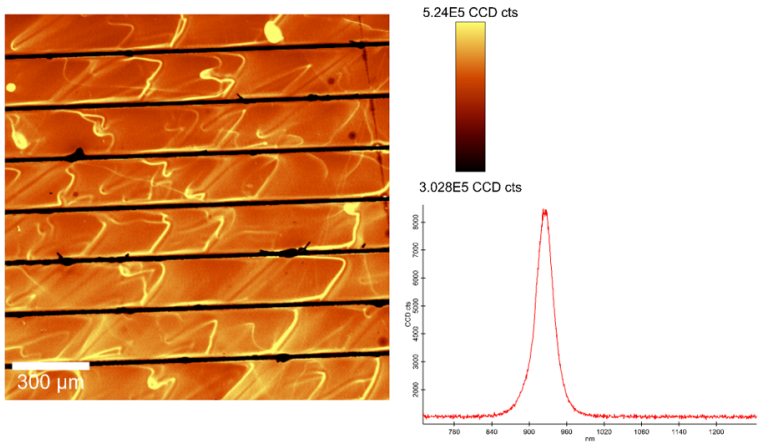


Figure 3.20: PL map of the most performing cell of sample H. Measurement performed with a laser at 532 nm (1.1 mW, 20x microscope objective). The irregular emission suggests a non homogeneous etching of the InGaAs contact layer.

the dry etching, a specific common step of the damaged samples. The reason for which this step could systematically (but non homogeneously) affect the samples is not completely clarified, but we suspect that the $H_2/Ar/Cl_2$ plasma can cause the ejection of Si micro particles from the holder during the etching. These particles may therefore randomly reach the edges of the mesas, which are not protected by the SiO_2 masks. Such a phenomenon can effectively be very limiting, as no later steps in our process guarantee removal

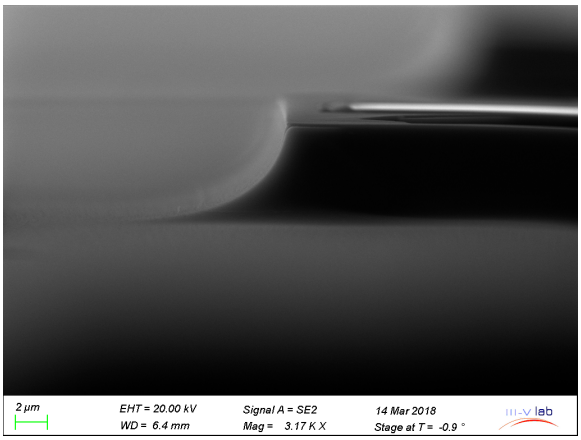


Figure 3.21: SEM image (3.17K magnification) of an InP test structure etched by a HBr:H_2O_2:H_2O solution for 1 min. The etched depth is $\sim 6\,\mu$m, and the characteristic etching profile has no relevant impact on our devices since the mesa heights are irrelevant compared to the dimensions of the patterns.

of these particles. They can therefore act as 'masks' during the deposition of the nitride, thus preventing a proper passivation of the devices. The high measured J_S values seem to confirm this hypothesis.

Figure 3.20 presents a PL map performed on the surface of the best cell of sample H. The inhomogeneous emission is probably due to a local, abnormal absorption at the surface of the device. This fact may be ascribed to an incomplete etch of the InGaAs contact layer, although profilometry scans on the surface did not reveal important inhomogeneity on the thicknesses. This fact is further accentuated on other devices of the same sample. In order to guarantee a complete removal of the first, absorbent layer, we decided to halve the water dilution of the H_3PO_4:H_2O_2:H_2O etchant solution.

In order to prevent the micromasking by Si particles, we considered two different solutions: the first is to subject the post etched samples to O_2 plasma cycles (to oxidize the particles) and HF etching (to remove the produced silica); the second, that we finally chose, consists of moving back to using chemical etching. In order to prevent all the previous problems related to wet etching (necessity of using different solutions for different layers, dependence of the etch rate from the doping levels of the various layers, etc.), we introduced a new, completely non selective solution: HBr:H_2O_2:H_2O (15:1:15). This solution etches all the deposited layers without any relevant influence from the material or the doping. The measured growth rate is $\sim 6\,\mu$m/min. Figure 3.21 presents the typical profile produced by this solution on the edges of an etched pattern.

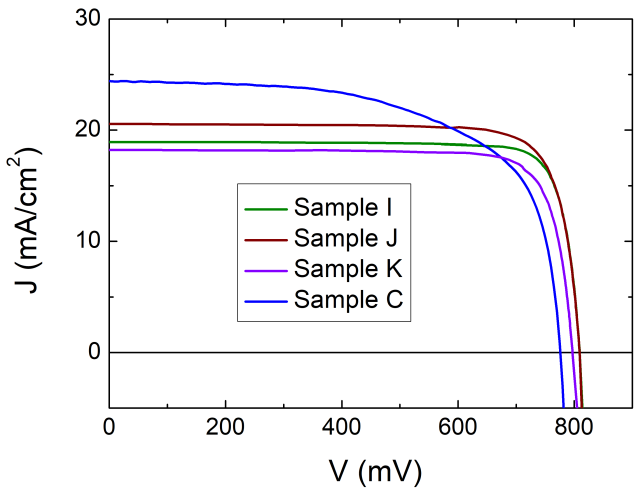


Figure 3.22: J-V characteristics under illumination of the best cells of samples I (green line, InP window), J (dark red line, AlInAs window), and K (violet line, AlInAs window with residually doped base) compared with the previous record (sample C, blue line).

We therefore realized one last series of samples: sample I, identical to sample H (InP window); sample J, presenting the same structure than sample F ($Al_{0.48}In_{0.52}As$ window); and sample K, identical to sample J, except for a less doped base (residual doping). During the processing, all metal contacts were deposited by sputtering and all mesas were etched by the above mentioned solution. The J-V characteristics under illumination of the best cells for the three samples are compared with the previous record (sample C) in Figure 3.22, whereas the correspondent photovoltaic parameters are reported in Table 3.6. The best cell of sample I, compared to sample C, shows sensitive improvements in V_{OC} and FF (809.3 mV versus 785.1 mV and 84.3% versus 63.6%, respectively), despite a reduction of J_{SC} (18.9 mA/cm^2 versus 24.4 mA/cm^2). The overall efficiency increased from 12.03% to 12.91%. Even more important, almost all (24) the cells presented a similar behaviour (the mean results were 807.0±1.4 mV, 19.0±0.2 mA/cm^2, 82.3±0.7% and 12.61±0.2%, respectively), thus demonstrating that the randomly limiting factor was effectively due to the dry etching. The important increase of FF in sample I, compared to C, demonstrates an overall, better crystalline quality of the grown materials in the new reactor. The reduction of R_s (as well as the disappearance of the double resistance) is probably also due to the better materials.

A comparison between samples I and J shows the beneficial effects of a high bandgap AlInAs layer (lattice matched to InP). The main advantage

	I	J	K
J_{SC} (mA/cm^2)	18.9	20.6	18.1
V_{OC} (mV)	809.3	809.3	797.0
FF (%)	84.3	81.4	82.2
η (%)	12.91	13.53	11.93

Table 3.6: Photovoltaic parameters of the best cells of samples I, J and K.

is an increase of the J_{SC} value, due to a better collection of the photogenerated carriers: the value measured for the best device is 20.6 mA/cm^2. On the other hand, V_{OC} does not present changes (809.3 mV and 805.8 mV for the best and the mean values, respectively). The FF is slightly reduced to 81.4% (80.9%), whereas η is increased to 13.53% (13.42%). In general, the measured improvements are in line with what is expected from [17].

Finally, sample K shows the effect of a less doped base (expected around a few 10^{16} cm^{-3}) with respect to sample J. As expected from [16], a lower base doping involves an overall reduction of the photovoltaic performances: the best and the mean values (on 22 cells) for every parameter are 18.2 and 17.8 mA/cm^2 for J_{SC}, 797.0 and 794.2 mV for V_{OC}, 82.2 and 80.9% for FF and 11.93 and 11.58% for η.

Like sample I, J and K present a high homogeneity, thus demonstrating the benefits of a HBr based chemical etching over a plasma dry etching. The mean values of J_S for the three samples decreased to the order of 10^{-8} A/cm^2 (sensitive reduction of the leaks). As a consequence, the various measured V_{OC} presented relatively high values.

Figure 3.23 compares the EQE characteristics of samples I, J and K with that of sample C. It is possible to notice a slight increase of the quantum efficiency for shorter wavelengths due to the presence of a higher bandgap window for sample J. However, the improvement is not particularly significant. This fact, together with the general trend of all the presented curves (constant decrease when moving towards shorter wavelengths), seems to suggest a surface passivation problem: a high surface recombination may explain the low efficiencies in this zone, together with the non negligible (although reduced) determined J_S. An implementation of the cells' passivation can therefore increase, at the same time, the EQE for shorter wavelengths and V_{OC}, thus allowing this latter to align with the InP state of the art. A possible solution, unfortunately not available at the moment, could be to treat the devices in a $(NH_4)_2S$ bath just before the Si_3N_4 deposition [45].

The last samples present a better efficiency for longer wavelengths, thus demonstrating once more the high quality of the new reactor growths.

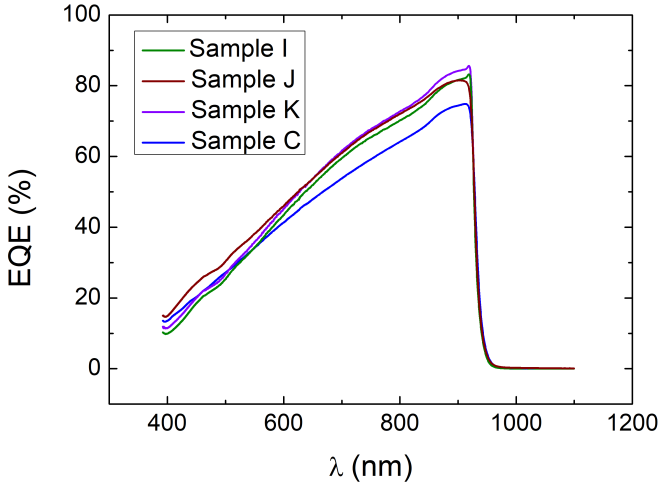


Figure 3.23: EQE characteristics of samples I, J and K, compared with sample C. The colours corresponds to those indicated in Figure 3.22.

3.6.3 Conclusions

Section 3.6 gave an overview of the main steps that characterized the development of a manufacturing process for InP solar cells, the main limiting factors, and the found solutions. The final validated process allowed us to obtain efficiencies record of 12.9% and 13.5% for devices presenting an InP and an AlInAs window layer, respectively. These efficiencies are not in line with the InP state of the art. Even so, a careful comparison demonstrates the high potential of our devices: the V_{OC} and FF are in line with the ones measured on the best known devices (to our knowledge, the 84.3% FF of sample I is one of the highest ever measured on this kind of device). The most limiting factor is J_{SC}, more or less half that of the best devices. This can be very well explained by our base: we already know that its doping level can affect J_{SC} [16]. Considering the results obtained with samples B and K, we can conclude that we have found an adequate doping concentration. Nevertheless, even the thickness plays an important role in this aspect since, trivially, a thicker layer means a higher absorption and, therefore, a higher amount of photogenerated carriers. Our devices present thinner bases compared to the state of the art devices (3μm versus $\sim 5\,\mu$m): by increasing this thickness, we should be able to measure values much closer to the best ones. Since this parameter should not affect V_{OC} and eventually, in a very minor way, FF, we can therefore conclude that our devices are potentially in line with the state of the art devices for single junction InP solar cells. We

should remember that our final goal is not to obtain a single junction device, but a tandem cell: a thicker base may significantly decrease the amount of radiation reaching the bottom cell, making it poorly efficient and, eventually, useless.

In conclusion, we can claim to have fulfilled the first main goal of this work: a complete manufacturing process for single (and eventually multi) junction solar cells was successfully realized. It allowed us to produce InP based devices characterized by very interesting performances, in line with the state of the art, which represent a significant possibility as a top cell in a dual junction device lattice matched to InP. In the next section, we will present the development of the correspondent InGaAs based bottom cell.

3.7 The InGaAs bottom cell

In parallel to the development of the InP top cell, the InGaAs bottom device was also studied. Since these devices were grown and processed together with the top cells, the development of their manufacturing process has been subject to the same, main tests and improvements presented in section 3.6 and, therefore, will not be presented again. In this section, we will therefore focus our attention on a quick presentation of the theoretical potential of this kind of device and on the presentation of our best results.

3.7.1 Theory and state of the art

The study of InGaAs based solar cells is mainly motivated by the research objective of an efficient bottom cell in 3J and 4J devices, as largely presented in Chapter 1. In fact, the low energy gap of this material (0.76 eV for a lattice matched to InP compound) makes it not very interesting for single junction applications. The SQ efficiency limit for this energy gap is $\sim$ 25%, as presented in Figure 1.5(b) (page 7), but the effective limit is much smaller. This value was recently determined by Korun and Navruz [46]. By taking the InGaAs optical and electrical parameters from [47], they obtained two different results by using two different simulation approaches. The most accurate simulation was obtained using a Drift Diffusion approach, in which not only the real absorption coefficient values and the effects of reflection due to refractive index differences were taken into account (Detailed Balance Approach), but also the thicknesses and the doping levels of the p-type emitter and the n-type base. The best effectively reachable efficiency for this kind of device is 12.06% (J_{SC} of 39.9 mA/cm^2, V_{OC} of 394.0 mV and FF of 76.6%). They also demonstrated that these devices have a higher potential compared to Ge based devices (typical bottom cell for GaAs devices), despite the similar bandgap: this fact represents one of the advantages arising from

the use of InP instead of GaAs.

The highest result reported in literature is very close to the theoretical maximum: Matsubara *et al.* obtained an efficiency of 11.8% (J_{SC} of 42.8 mA/cm^2, V_{OC} of 390.0 mV and FF of 71.0%); in this case, however, they used a 400 nm n-type (-1×10^{18} cm^{-3}) emitter and a 3 μm p-type (+4×10^{17} cm^{-3}) base [48]. The result obtained with the same doping polarity of [46] (keeping the same emitter and base thicknesses) was limited at 9.4% (probably because of the lower diffusion length). These devices, as well as all the ones presented in this section, were grown by MOVPE. A better result with the p/n polarity (where the p-doping was obtained by Zn diffusion) was presented by Ho *et al.* [49]: J_{SC} of 43.3 mA/cm^2, V_{OC} of 385.0 mV, FF of 54.3% and η of 10.35%. In this case, a 2 nm InP window layer was introduced.

Other relevant results were 9.3% obtained by Mathews *et al.* with a n-type base [50], 2.1% obtained by Lumb *et al.* [51] under 690 suns (in this case, the cell was used as a fourth junction transfer printing layer for a 3J InGaP/GaAs/InGaAsNSb device) with a p-type base and 13.6% declared by Zahler *et al.* [52] for a p base device grown onto a wafer bonded InP/Si substrate. Unfortunately, the used irradiation power density of 36.3 mW/cm^2 (AMG1.5 global illumination truncated at 850 nm) impedes comparison of this result with the other ones and determination of the effective influence of the lattice mismatched substrate (Zahler and his group showed that a Si substrate guarantees a better light trapping effect which increases both J_{SC} and EQE).

3.7.2 Realization of the InGaAs bottom cell

As already mentioned, the development of the InGaAs bottom cell followed the main steps of the corresponding InP device. For this reason, we will limit our description of this part to the presentation of the best obtained device.

Table 3.7 presents the structure of the best cell: although we started our research from the structure presented in [48], it was soon clear that both the proposed base doping level (-4×10^{17} cm^{-3}) and emitter thickness (400 nm) were too high and had a too-strong impact on the overall absorption. Both values were reduced during the following growths. The best result was obtained with values very similar to those used in the InP cell: -1×10^{17} cm^{-3} and 200 nm, respectively. The rest of the structure presents an InP buffer/BSF layer (the high bandgap of InP compared to InGaAs should sensibly reduce the rear recombination), a typical unintentionally doped transition layer, an AlInGaAs (lattice matched to InP, gap of $\sim$ 1.2 eV) window layer, an InP stop etch (to protect the window during the etch of the upper layer) and a typical highly doped InGaAs contact layer. Usually,

Function	Material	Thickness (nm)	Dop. level (cm^{-3})
Contact layer	$In_{0.53}Ga_{0.47}As$:Zn	250	$+2\times10^{19}$
Stop etch	InP:Zn	10	$+1.5\times10^{18}$
Window layer	$Al_{0.31}In_{0.53}Ga_{0.16}As$:Zn	30	$+1.5\times10^{18}$
Emitter	$In_{0.53}Ga_{0.47}As$:Zn	200	$+1\times10^{18}$
Transition layer	$In_{0.53}Ga_{0.47}As$ nid	20	–
Base	$In_{0.53}Ga_{0.47}As$:Si	3000	-1×10^{17}
BSF	InP:Si	400	-2×10^{18}
Substrate	InP:S	3.5×10^{5}	-2×10^{18}

Table 3.7: Structure of the best realized cell. The thicknesses and the doping levels are very similar to the ones optimized for the InP top cell. As for the InP cells, the n-type layers were grown at 680 °C, whereas the p-type were grown at 610 °C.

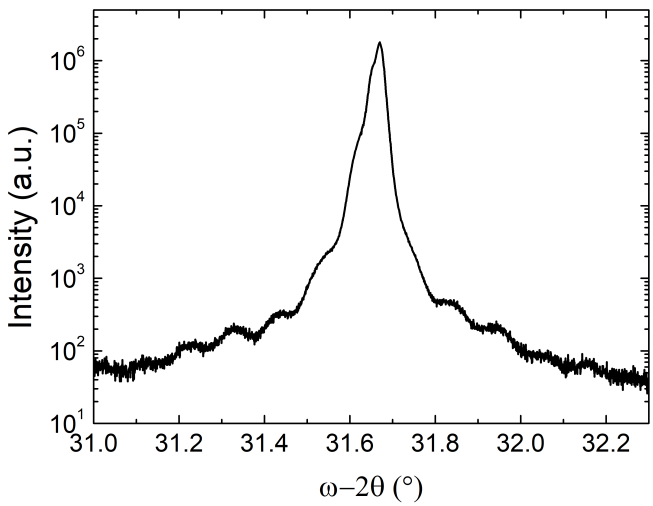


Figure 3.24: XRD scan of the best device before the processing. The width peak is due to the thick, almost lattice matched InGaAs layers. We can however appreciate the proper composition of the differently doped epilayers.

in this type of device, the window layer is InP [49]: this is a logical choice, since this layer can highly reduce the front recombination thanks to its high bandgap (same principle as the BSF) and can be very easily grown without particular calibrations. Nevertheless, we chose a lower bandgap quaternary alloy such as $Al_{0.31}In_{0.53}Ga_{0.16}As$: in this way, all the upper layers of this device present a lower bandgap than those of the InP cell. The performances of this bottom device should therefore give a more realistic idea of its effective contribution to the overall efficiency in a tandem device (since it is less

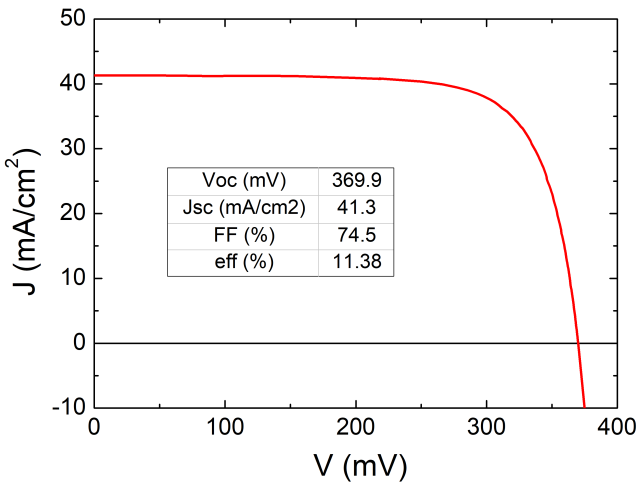


Figure 3.25: J-V characteristic under illumination of the best obtained InGaAs cell. The mean measured values (22 cells) were a J_{SC} of 41.3 mA/cm^2, a V_{OC} of 366.5 mV, a FF of 71.6% and η of 10.87%.

affected by the presence of an upper InP bulk layer).

This cell was grown in the vertical reactor, and Figure 3.24 presents the XRD scan of this structure: we can notice one single peak, which means that all the layers are almost lattice matched to the InP substrate.

The processing of this device was identical to the one performed on samples I, J and K of the InP series, and the only notable difference lies in the thickness of the Si_3N_4 ARC: the lower bandgap of InGaAs implies a longer absorption wavelength and, therefore, a 204 nm thick layer.

Figure 3.25 presents the J-V characteristic of the best obtained cell: a J_{SC} of 41.2 mA/cm^2, a V_{OC} of 369.9 mV, a FF of 74.5% and, mostly, a η of 11.38% are in line with the best performances reported in literature. To our knowledge, this device is less efficient only than the one presented by Matsubara *et al.* and establishes the state of the art for a p/n polarity. Also, in this case, the quality of our process is proven by the high homogeneity of the performances: 21 cells on 25 presented a similar behaviour, and the mean measured values were 41.3 mA/cm^2 for J_{SC}, 366.5 mV for V_{OC}, 71.6% for FF and 10.87% for η, respectively.

The dark saturation current extrapolated from the dark J-V characteristic is $\sim 1.5\times10^{-5}$ mA/cm^2: although this value is quite high for a solar cell, it can be justified by the relatively low V_{OC} that affects a so low bandgap material.

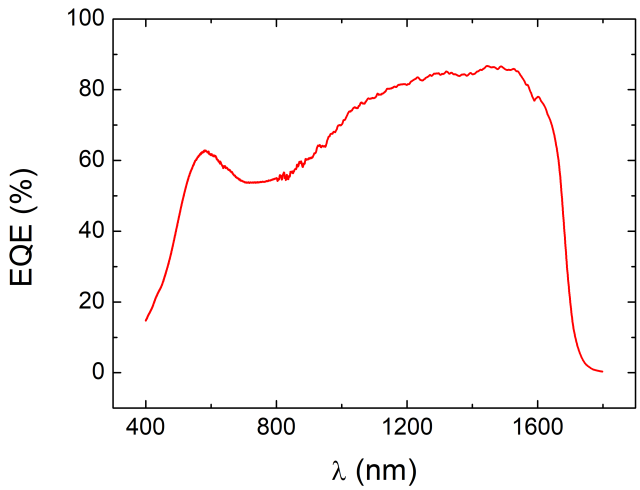


Figure 3.26: EQE characteristics of the best InGaAs solar cell.

Figure 3.26 presents finally the EQE characteristic of the best InGaAs cell: despite a slight valley in the 700-800 nm range, the amount of the collected charges is important for every wavelength, in particular in the 950-1650 nm range. A good collection for shorter wavelengths has to be highlighted as well. Compared to the InP top cell, this result seems to be less affected by the surface recombination and the non optimal passivation.

3.8 Conclusions

The photovoltaic parameters of the InGaAs cell presented in the previous section make it a very promising solution for a bottom cell in a tandem device lattice matched to InP. At the same time, we saw how samples I and J of the InP cells series can be used as top cells in the same device. Unfortunately, the only limiting factor between these two devices, the J_{SC} of the top cell, is very far from its potential value (almost double the obtained one). Since the two cells will be connected in series, the lower J_{SC} will limit the overall performance. Furthermore, the fact that this J_{SC} belongs to the top cell impedes using the current matching principle presented in Section 1.2.1. In fact, we can consider inverse application of this principle: by increasing the thickness of the top cell base, we should increase its J_{SC}. This fact will lead to a higher absorption in the top cell and, consequently, a lower amount of radiation reaching the bottom one, reducing its own J_{SC}. An accurate series of tests should allow us to optimize, at the same time, the two cells when series connected; this result is beyond the goal of this study. In conclusion,

although not optimized together, we realized a very promising InP top cell and an InGaAs bottom cell for a tandem solar cell application. The next step, presented in the next chapter, is the realization of the last 'brick' of the overall structure, the tunnel junction. After that, all the various components for the realization of a promising tandem device will be ready.

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Chapter 4

Tunnel junctions and tandem devices

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In the previous chapter, we presented the independent optimization of the two solar cells constituting the final tandem device. In the first part of this

chapter, we present the development of the last component of this device, the intermediate tunnel junction. After a preliminary presentation of the concept of the tunnel junction and the state of the art of its performances, we will propose a possible structure, highlighting its main advantages and potentials. We will then present the development of a proper growth procedure for this kind of structure and a series of material characterizations. Finally, we will present the processing and the final electrical performances of the structure.

In the second part of this chapter, we will combine the three components into a tandem device and we will present the final performances.

4.1 Tunnel junctions: a general review

When realizing a multi-junction solar cell in a 2 terminals configuration, reverse n on p junctions are formed at the interfaces between each subcell (for example, in our case, between the InP:Si BSF of the top cell and the AlInGaAs:Zn window of the bottom cell). These junctions may be extremely limiting for the final device performance, since they introduce high voltage drops that can affect both V_{OC} and η. The solution to this problem consists of inserting a tunnel junction between all the cells, which enables tunneling of the photogenerated carriers between the subcells [1].

These devices can also be successfully integrated in various devices such as VCSELs [2].

4.1.1 The principle

The tunnel junctions were described for the first time by Esaki in 1957 [3]. They consist of very highly doped p-n junctions characterized by degenerated states, which allow an alignment of the n-side conduction band with the p-side valence band. The behaviour of a tunnel junction when an external bias is applied is presented in Figure 4.1(a-g), whereas (h) represents the correspondent J-V characteristic. Clearly, at 0 V applied (a), the states are at the thermodynamic equilibrium and no current is flowing. When a small, forward bias is applied (b), the potential barrier is still too high to allow electrons in the n-side conduction band to be injected in the p-side one. Nevertheless, they can tunnel to the empty states of the p-side valence band: a forward bias tunnel current is generated. This phenomenon will become more and more intense by increasing the forward bias, until the energy of the majority of electrons in the n-side will be equal to that of the empty states in the valence band of the p-side: at this point, the maximum tunnel current is produced (c). By again increasing the bias, the tunnel current will start to decrease (d), as the number of electrons in the n-side that are directly opposite to the empty states in the p-side decreases: since

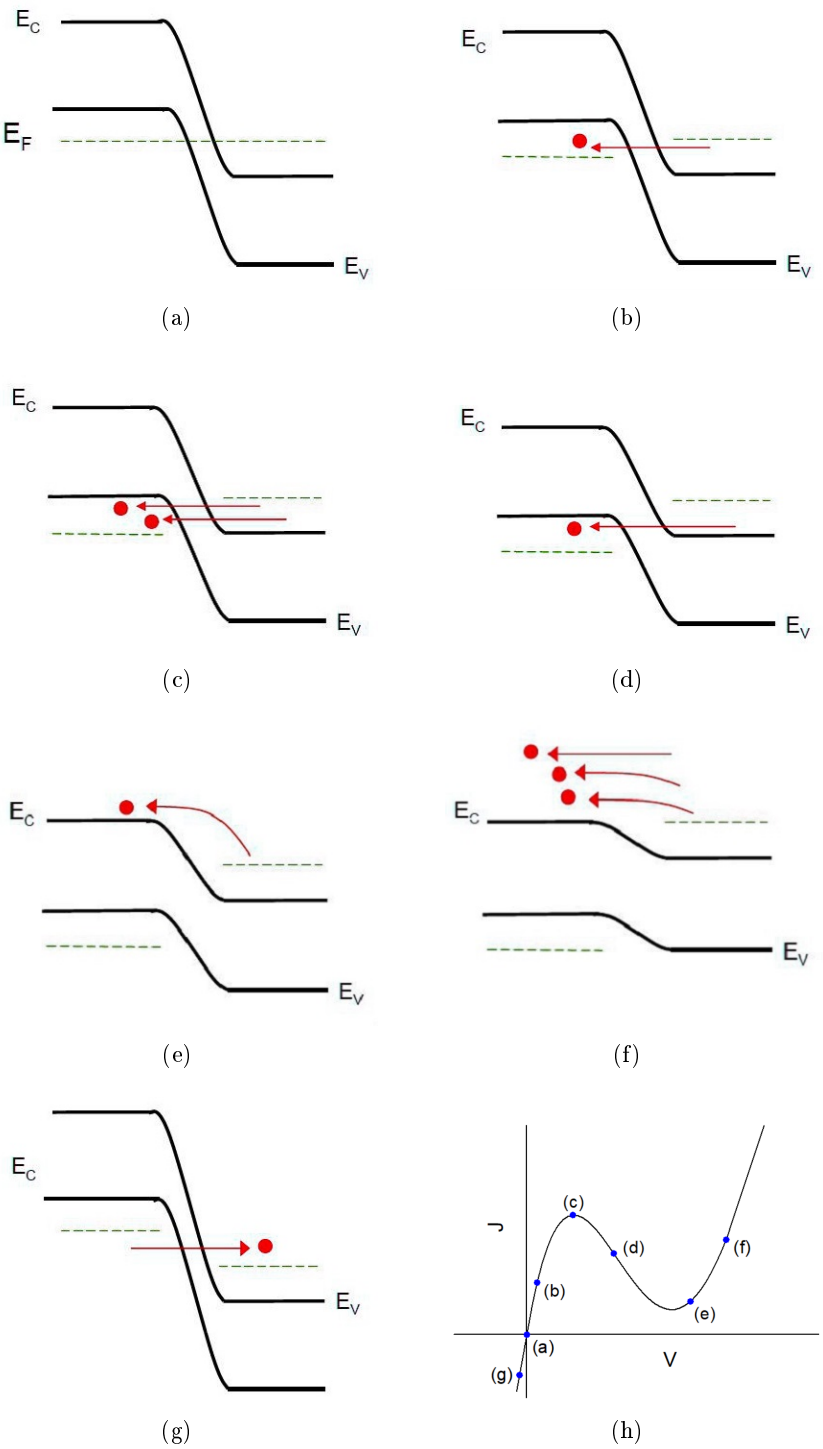


Figure 4.1: Evolution of the band diagram of a tunnel junction at the increase of (a-f) forward and (g) reverse bias and (h) correspondent J-V characteristic.

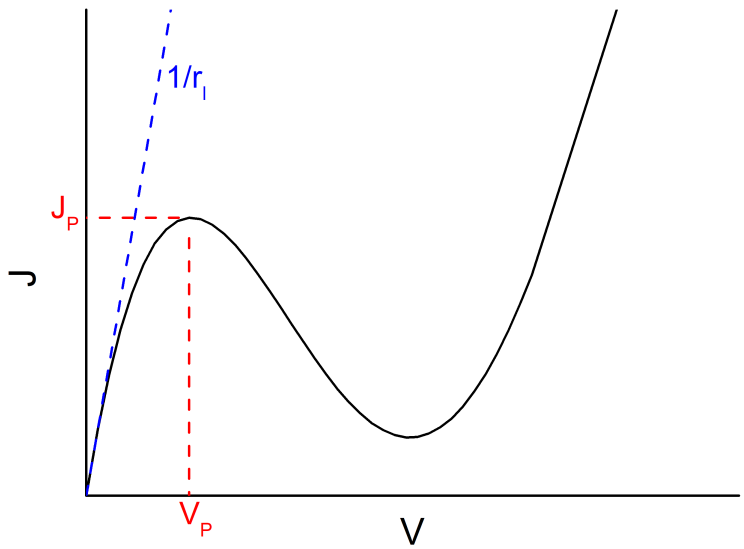


Figure 4.2: Typical J-V characteristic of a tunnel junction. The main electrical parameters are presented: J_p corresponds to maximal tunnel current (V_p is the relative voltage), r_l represents the resistivity of the device when low biases are applied.

an increase in V causes a reduction in J, we define this zone as a negative differential region (NDR). The tunnel current continues to decrease until it reaches zero; however, at this point, the potential barrier is small enough to present the regular diode forward current due to electron–hole injection (e). As the bias increases again, the J-V characteristic of the tunnel diode will present the typical exponential trend of a regular p-n diode (f). In the case of an applied reverse bias, the electrons of the p-side valence band will directly tunnel to the n-side conduction band empty states, thus producing a large tunnel current, proportional to the applied voltage (g).

4.1.2 The main parameters

Figure 4.2 presents the main electrical parameters that characterize a typical tunnel junction J-V curve: the peak tunnel current J_p, which corresponds to the maximal current that can flow across the junction by tunnel effect (in the same way, V_p is the correspondent voltage value), and the resistivity for low-applied biases r_l, which corresponds to the resistivity of the device in its ohmic region. For solar cells, J_p should at least equal the photogenerated

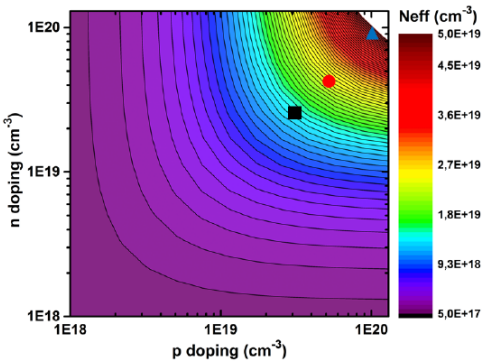


Figure 4.3: Tunnel junction effective doping level N_{eff} as a function of N_{n++} and N_{p++} doping concentrations.

current in a multi-junction device, in order to not impact the photovoltaic performances of the cell. When considering this, it is also worth remembering that the intensity of the photogenerated current is proportional to the light concentration on the device: considering the typical J_{SC} of our InP-based cells, a tunnel junction, in order to work under ultra high concentration (10 000 suns), must present a $J_p \geq 200\,A/cm^2$. We should also remember that the light concentrating optics system may not be completely uniform, thus locally increasing the J_{SC} [4, 5]. Since a reduction of J_p may occur because of the junction degradation due to the higher growth temperature of the upper cells [6, 7], it is preferable to obtain notably higher J_p than the minimum attended value.

According to [8]:

$$J_p \propto exp\left(\frac{-{E_g}^{3/2}}{\sqrt{N_{eff}}}\right) \tag{4.1}$$

with

$$N_{eff} = \frac{N_{n++} \cdot N_{p++}}{N_{n++} + N_{p++}} \tag{4.2}$$

N_{n++} and N_{p++} correspond to the doping level of the cathode and the anode of the junction, respectively: these equations show the necessity of having both sides highly doped, since the effective contribution is strongly limited by the less doped layer, as showed in Figure 4.3. From equation 4.1 we can also deduce the importance of using low bandgap materials. This is however in contrast with the necessity of having as transparent as possible device (in order not to limit the absorption of the lower cells): it is therefore important to find a good compromise between efficiency and transparency, maximizing, at the same time, the doping concentrations.

On the contrary, r_l (and, consequently, V_p) has to be as low as possible, in order to limit the contribution to the series resistance of the photovoltaic devices [9]. If both conditions on J_p and r_l are fulfilled, the voltage drop due to the tunnel junction in the final multi-junction device will be directly related to r_l [10].

The value of J_p in tunnel junctions can also be increased by the trap-assisted tunnelling (TAT) phenomenon [11, 12]: crystalline defects generated during growth of the samples can act as deep, trap levels for the electric carriers, thus considerably modifying the characteristics of the device.

4.1.3 State of the art

The literature presents a small number of tunnel junctions lattice matched to InP. These were mainly grown by CBE [13, 14] and MBE [15, 16]. The highest value of J_p reached on this lattice parameter, corresponding to a J_p of 1600 A/cm^2, was obtained by CBE growth with an InP/InP device by Vilela *et al.* [14]: the p-dopant (5-7$\times10^{18}$ cm^{-3}) was Be, whereas the n-dopant (1×10^{19} cm^{-3}) was Si. Such a result is difficult to explain, as the effective doping level of the presented device is low compared to all the others mentioned. Both layers presented a thickness of 75 nm. The determined voltage drop for a 100 suns (AM0 spectrum) concentration should only be on the order of mV. Furthermore, the performances seemed to not be affected by the following growth of the upper cell. The same group obtained another excellent result by substituting both InP layers by lattice matched InGaAs, with a final J_p of 1015 A/cm^2. Also, MBE allowed to obtain a proper device for ultra high light concentration: the InP:Be/InP:Si structure presented by Dotor *et al.* (200 and 500 nm thicknesses, 1×10^{20} and 7×10^{19} cm^{-3} doping levels respectively) was characterized by a final 258 A/cm^2 peak tunnel current [15]. To our knowledge, the only device grown by MOVPE was presented by Okuno *et al.* [17]: fabricated on a (3 1 1) substrate, it presented an InGaAs:Zn anode (10 nm, 5×10^{19} cm^{-3}) and an InP:Si cathode (20 nm, 2×10^{19} cm^{-3}). However, the details about the performances were not presented.

An alternative to the classical anode/cathode structure was suggested by the Lumb group [16, 18, 19]: they realized a double quantum-well (QW) InGaAs tunnel junction, with the addition of a series of $Al_{0.33}In_{0.52}Ga_{0.15}As$ (1.18 eV) quantum-barriers (QB). The motivation for this study was to exploit the tunnelling via the confined electron and hole energy levels of the QW, improving the resonant interband tunnelling probability. Furthermore, this approach allowed to increase the transparency of low bandgap InGaAs. The final structure presented this shape: AlInGaAs:p+ QB (5 nm),

p-type			n-type				
Mat.	Thick. (nm)	Dop. (cm^{-3})	Mat.	Thick. (nm)	Dop. (cm^{-3})	Tech.	J_p (A/cm^2)
InP:Be	75	5-7e18	InP:Si	75	1e19	CBE	1600 [14]
InGaAs:Be	200	5e19	InGaAs:Si	200	1.3e19	CBE	1015 [13]
InP:Be	200	1e20	InP:Si	500	7e19	MBE	258 [15]

Table 4.1: State of the art ($J_p \gg 100\,A/cm^2$) for InP-based tunnel junctions. The materials, thicknesses and doping levels are given for both anodes and cathodes. The relative growth techniques and J_p are given as well.

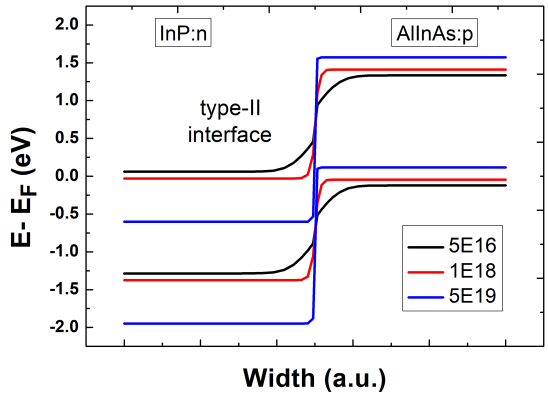
InGaAs:p++ QW (8 nm), AlInGaAs:p++ QB (2 nm), AlInGaAs:n++ QB (2 nm), InGaAs:n++ QW (8 nm) and AlInGaAs:n+ QB (5 nm). Both the p++ (Be) and the n++ (Si) layers presented doping levels of $1\times10^{19}\,cm^{-3}$, the used growth technique was MBE. This structure allowed them to obtain a final J_p of $112.9\,A/cm^2$. This result was approximately 45 times higher than the one obtain with a classic, bulk AlInGaAs:Be/AlInGaAs:Si structure with the same overall thickness and doping levels. A similar structure was obtained by using an $Al_{0.34}In_{0.66}As$ QW / $Al_{0.59}In_{0.41}As$ QB / InGaAs QW structure, obtaining a J_p of $47.6\,A/cm^2$ [20]. In both structures, they demonstrated that the presence of extremely thin InGaAs layers seems to not affect the transmittance of the device.
The best results present too excellent performances to be justified by the tunnel effect alone, therefore a TAT contribution should be taken into account. All the presented devices were characterized by resistivities r_l between 10^{-4} and $10^{-5}\,\Omega\cdot cm^2$, whose contribution to the series resistance of a multi-junction device were, therefore, completely irrelevant.

4.2 Presentation of the device

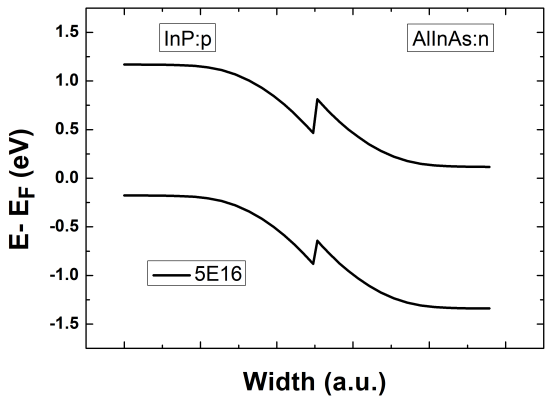
The previous section presented the main parameters that control the performances of an efficient tunnel junction, as well as the most important aspects related to their use in photovoltaic applications. It is now possible to present the choices made during this work in order to realize and optimize this kind of device.

4.2.1 Choice of the materials

Despite equation 4.1 demonstrating how the use of low bandgap materials can increase J_p in a tunnel junction, we concentrated our research on more transparent materials, in order to maximize the transmissivity of the device.



(a)



(b)

Figure 4.4: Simulated band diagram at the type-II interface between (a) a p-doped AlInAs and a n-doped InP for an absolute doping level of 5×10^{16} (black lines), 1×10^{18} (red lines) and $5\times10^{19}\,\mathrm{cm}^{-3}$ (blue lines) for both the sides and (b) a n-doped AlInAs and a p-doped InP for an absolute doping level of $5\times10^{16}\,\mathrm{cm}^{-3}$ (black lines) for both the sides. The width is given in arbitrary units.

An interesting possibility for the realization of the tunnel junction cathode and anode is given by the use of InP (1.34 eV) and $Al_{0.48}In_{0.52}4As$ (1.42 eV), since the interface between these two materials naturally presents a type-II band alignment, as shown by the simulations represented in Figure 4.4: this type of interface is very favourable for carrier tunnelling, due to a partial alignment of the p-side valence band with the n-side of the conduction band. Figure 4.4 also shows that this configuration is strongly dependent on the

polarity of the materials (in all cases, an equal, absolute doping is considered for both sides): whereas an AlInAs:p/InP:n structure (a) presents an ideal situation, enhanced by the increase of the doping concentration (the bands are more and more divided, until they reach a type-III like configuration over a $|2\times10^{18}\,\mathrm{cm}^{-3}|$ doping level for both the sides), an AlInAs:n/InP:p one (b) presents a typical spike at the bands' interface, which can impact the carriers' tunnelling.

The configuration presented in Figure 4.4(a) has also to be preferred because of some limitations of the MOVPE growth technique: whereas InP can be quite easily heavily n-doped by S (eventually even by Si, although the amphoteric behaviour of this element impacts the sample morphology for high concentrations), we already saw in chapter 2 that neither Zn (fast saturation) nor C (amphoteric behaviour) can lead to a high p-doping. On the other hand, AlInAs can be highly p-doped by C (as for InP, Zn-doping saturates very quickly), but not n-doped.

4.2.2 Sample description

The polarity of the single junction cells presented in the previous chapter is p/n. Therefore, in a multi-junction device, the tunnel junctions have to be grown with the InP cathode on the AlInAs anode. Unfortunately, this structure may not be possible to characterize: as already mentioned, the processing of n/p devices is complicated by some limiting factors (this aspect will be further presented in section 4.4). We therefore decided to grow and process both the p-on-n (p/n) and n-on-p (n/p) polarities: it is reasonable to expect a similar electrical behaviour, and furthermore, the materials' characterizations can demonstrate if a reverse growth can affect the quality of the structures.

In order to be electrically characterized, our tunnel junctions were inserted in the structures presented in Tables 4.2 and 4.3 (p/n and n/p polarities, respectively). The use of these structures has two main advantages: the first one is to help the carriers collection by inserting the junction between thicker layers which can act as electric ramps, due to the lower doping levels; the second one is to better simulate the influence of the junction inside a tandem cell, since the p+ and n+ spacers at the edges of the junction are very similar to the bottom cell's window layer and the top cell's BSF respectively, and can therefore represent real parameters such as the effective contact resistivity [5, 14, 21]. Besides the tunnel junction anode and cathode and the p+ and n+ spacers, the structures are characterized by typical, highly doped InGaAs contact layers and a preliminary InP buffer (in the p/n structure, the buffer coincides with the n+ spacer). Since the thickness of the junction should not affect the final performances (as shown by equation 4.1), we decided to test very thin layers (around 15 nm) in order to reduce

Function	Material	Thickness (nm)	Doping level (cm^{-3})
Contact layer	InGaAs:Zn	100	$+1.5\times10^{19}$
Spacer p+	AlInAs:C	300	$+7\times10^{18}$
Anode p++	AlInAs:C	15	$+4\times10^{19}$
Cathode n++	InP:S	15	-4×10^{19}
Spacer n+	InP:Si	200	-2×10^{18}
Substrate	InP:S	3.5×10^{5}	-2×10^{18}

Table 4.2: Scheme of the validation structure of the p/n device. The highly doped central layers represent the anode and the cathode of the tunnel junction, the p+ and n+ spacers (this last one acts also as a growth buffer) can represent the bottom cell window and the top cell BSF, respectively.

Function	Material	Thickness (nm)	Doping level (cm^{-3})
Contact layer	InGaAs:Si	150	-1.2×10^{19}
Spacer n+	InP:Si	300	-2×10^{18}
Cathode n++	InP:S	15	-4×10^{19}
Anode p++	AlInAs:C	15	$+4\times10^{19}$
Spacer p+	AlInAs:C	500	$+7\times10^{18}$
Buffer p+	InP:Zn	200	$+1.5\times10^{18}$
Substrate	InP:Zn	3.5×10^{5}	$+1.5\times10^{18}$

Table 4.3: Scheme of the validation structure of the n/p device. The functions of the various layers are the same of the previous Table. A further InP:Zn buffer had to be added.

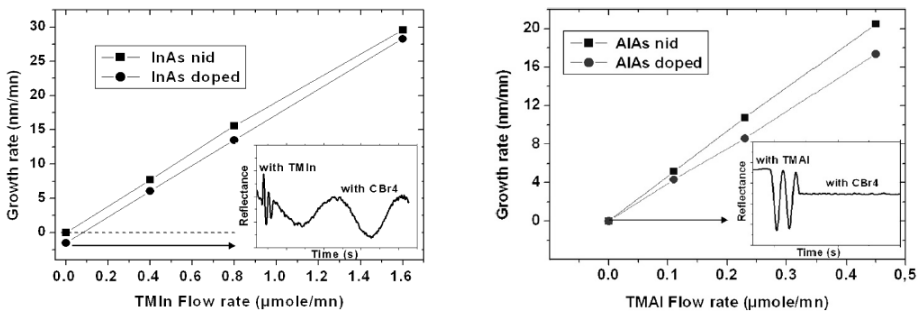
the overall thickness as much as possible.

4.3 Low temperature growth

The most challenging point of the realization of the presented devices is certainly the growth of highly p-doped AlInAs layers. As mentioned before, such a high doping can be obtained only by using C as a dopant. Nevertheless, the achievement of an adequate doping level for a tunnel junction application required us to work under very particular growth conditions: a low AsH_3 flow ($\leq$ 30 sccm) and a reduced growth temperature (nominally 540 °C). This low growth temperature is necessary to reduce the etching effect of CBr_4 (see next section). Furthermore, it results in a less efficient AsH_3 cracking: therefore, both conditions aim to increase the dop/V ratio by reducing the As content. In the next sections, we will present in detail how such a result was made possible.

4.3.1 A challenging precursor: the CBr_4

Over the past few decades, the use of C in MOVPE as a p-type dopant for different compounds became more and more widespread [23–25]. This was basically due to its very low diffusion coefficient, when compared to the more conventional Zn dopant, and to its very high achievable doping levels [26, 27]. In particular, Neuman et al. reported a p-type doping higher than $1\times10^{20}\,cm^{-3}$ for AlInAs by using CBr_4 as C precursor [28]. Literature shows that, by varying the flow of CBr_4 during the growth, it is possible to act not only on the doping levels of the various layers, but also on their growth rates [29, 30]. This fact is due to the etching ability of halomethanes [22]. In considering C doping of AlInAs, literature presents very different results about the etching ability of CBr_4 [31, 32]. However, Decobert et al. demonstrated that the net effect arises from the contemporary reaction of CBr_4 with vapour phase TMAl and its etchant effect on solid state InAs [22]: as shown in Figure 4.5(a), the introduction of CBr_4 in the reactor during the growth of an InAs layer involves a constant reduction of the overall growth rate (measured by reflectance), even when lacking TMIn flow. This fact demonstrates a constant etching of the semiconductor surface. On the other hand, when the same experiment is performed during the growth of AlAs (b), the etching rate is zero when no TMAl is flowing in the reactor and increases with TMAl flow: it is therefore possible to conclude that, in this case, the growth rate reduction is governed by a gaseous reaction of CBr_4 and TMAl. Finally they demonstrated that CBr_4 flow, V/III ratio and growth rate determine which of the two effects is more relevant during the growth. As a consequence, equation 2.6 (page 45) is not valid in this case and a proper control on the composition of an $Al_xIn_{1-x}As$ layer requires a careful consideration of all the above mentioned parameters. In the next



(a) (b)

Figure 4.5: (a) InAs and (b) AlAs growth rate reported as a function of the TMIn (TMAl) flow for undoped and doped epilayers. The inset shows the in-situ reflectance of a growing InAs (AlAs) layer followed by the InAs (AlAs) etching under CBr_4. From [22].

section, we will present how this type of calibration should be carried out.

4.3.2 Calibration of the AlInAs anode

Table 4.4 summarizes the tests performed to obtain a highly doped, lattice matched AlInAs:C layer. We realized three samples, characterized by three different V/III ratios. The composition was controlled by varying the flow of TMAl between the three samples, since the TMIn flow was always kept constant. AsH_3 flow rate was decreased in samples B and C, in comparison with sample A, in order to increase the incorporation of dopant. Every sample presented three AlInAs layers of 250 nm nominal thickness characterized by three different CBr_4 flow rates. The variations of the flows are expressed by the variations of the dop/V input gas ratio, and the lattice mismatches are indicated in ppm.

The compressive shift that characterizes the more doped layers compared to the less doped ones denotes a progressive decrease in the Al content when increasing the doping: we can conclude that, for our growth conditions, the interaction of CBr_4 with TMAl is more relevant than its etchant effect on InAs. Therefore, when the growth conditions are varied in order to increase the C incorporation, a contemporary increase in TMAl flow is mandatory to keep the proper chemical composition of the alloy.

The compressive shift that characterizes sample B when compared with sample A is then well explained by the reduction of the AsH_3 flow: a decrease of AsH_3 flow leads to a higher CBr_4/AsH_3 ratio at the surface of the sample, decreasing therefore the Al content. This strong change in composition was

	dop/V ratio	$\Delta a/a$ (ppm)	dop (cm^{-3})
sample A	1.0e-3	-2400	2.5e18
V/III ratio: 8.7	3.7e-3	-1830	6.5e18
TMAl: 43.7 μmol/min	1.8e-2	+500	2e19
sample B	1.5e-3	-1260	4e18
V/III ratio: 5.7	5.6e-3	-820	8e18
TMAl: 45.3 μmol/min	2.7e-2	+1120	4e19
sample C	1.5e-3	-2170	4e18
V/III ratio: 5.6	5.6e-3	-1650	8e18
TMAl: 48.5 μmol/min	2.7e-2	+300	4e19

Table 4.4: Summary of the study performed on the effects of CBr_4 doping on the composition of AlInAs. For every sample, the V/III ratio and the TMAl flow, as well as the dop/V ratio, the lattice mismatch from the InP substrate and the doping levels of every single AlInAs layer are indicated.

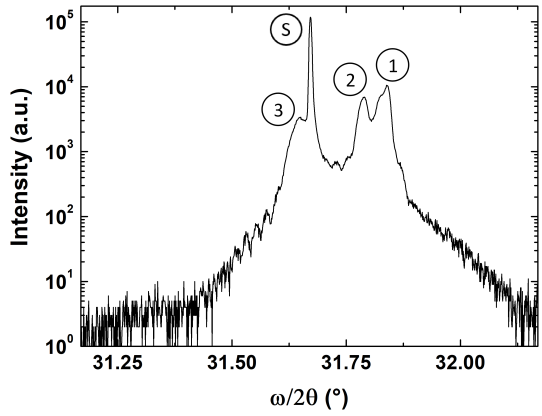


Figure 4.6: Experimental XRD $\omega/2\theta$ profile of sample C. The less doped layer (1) is strained at -2170 ppm, the intermediate one (2) at -1650 ppm and the most doped (3) at +300 ppm compared to the substrate (S).

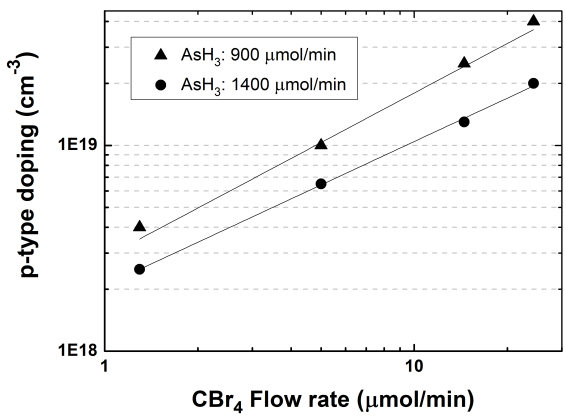


Figure 4.7: P-type doping of AlInAs as a function of CBr_4 flow rate for different AsH_3 flows at 540 °C. The measurements were taken by ECV profile and combined with the measurements reported in [22].

not sufficiently compensated by the small increase of the TMAl flow rate. On sample C, keeping a constant AsH_3 flow, the further increase of the TMAl source allowed us to reduce the compressive stress. As expected, the doping levels measured in samples B and C are higher than in sample A, because of the decrease of AsH_3 flow. Since the TMAl flow does not affect the doping, their measured levels are equal. The p++ layer of sample C presented a doping level of $4\times10^{19}\,cm^{-3}$ and was chosen to realize the anode of the tunnel junctions (the TMAl flow was slightly increased in order to

compensate the little lattice mismatch). The measured growth rate for this last layer was $\sim$ 40 nm/min. The mismatches of the three layers of sample C were extracted by the XRD $\omega/2\theta$ scan presented in Figure 4.6. In order to confirm the correspondence between every layer and the related peak, the layers were separately etched and new XRD scans were performed after each etch.

The linear relation between the p-type doping level of the layers and the correspondent CBr_4 flow is showed in Figure 4.7: the measured values are integrated with the ones presented in [22].

4.3.3 The InP:S cathode

Table 4.5 presents the V/III and the dop/V (dop/III) ratios of the various layers constituting the p/n and n/p tunnel junctions. The p++ layer of sample C was used as an anode. On the other side, the AlInAs p+ spacer was calibrated again, compared to the second layer sample A, in order to reduce the strain. The InP:S cathode was grown at 540 °C as well: although a low growth temperature is not mandatory to obtain a high n-doping, this choice allowed us to minimize the waiting time between the growth of the two sides of the junctions, thus guaranteeing a more abrupt interface. A dop/V ratio of 6.3×10^{-3} allowed us to obtain a n doping level of -4×10^{19} cm^{-3}, whereas the N_{eff} of the junction was 2×10^{19} cm^{-3}. The measured growth rate for this layer was 20 nm/min.

All the other layers were grown at the typical growth temperatures presented in section 3.3, 680 °C for the n-layers and 610 °C for the p-layers. In

Material (V/III ratio)	Function	dop/V ratio	Doping (cm^{-3})
$Al_{0.48}In_{0.52}As$:C (5.5)	Anode p++	2.7×10^{-2}	$+4\times10^{19}$
$Al_{0.48}In_{0.52}As$:C (8.7)	Spacer p+	8.7×10^{-3}	$+7\times10^{18}$
InP:S (78.4)	Cathode n++	6.3×10^{-3}	-4×10^{19}
Material (V/III ratio)	**Function**	**dop/III ratio**	**Doping (cm^{-3})**
InP:Si (78.4)	Spacer n+	1.0×10^{-3}	-2×10^{18}
$In_{0.53}Ga_{0.47}As$:Zn (11.1)	Contact p++	7.5×10^{-2}	$+1.5\times10^{19}$
$In_{0.53}Ga_{0.47}As$:Si (11.1)	Contact n++	8.3×10^{-4}	-1.2×10^{19}
InP:Zn (78.4)	Buffer p+	3.0×10^{-2}	$+1.5\times10^{18}$

Table 4.5: V/III and dop/V (dop/III) ratios (with respective doping levels) used during the growth of the presented tunnel junctions.

the case of the n/p structure, 5 minutes' annealing at 680 °C was performed before starting the growth of the p-side.

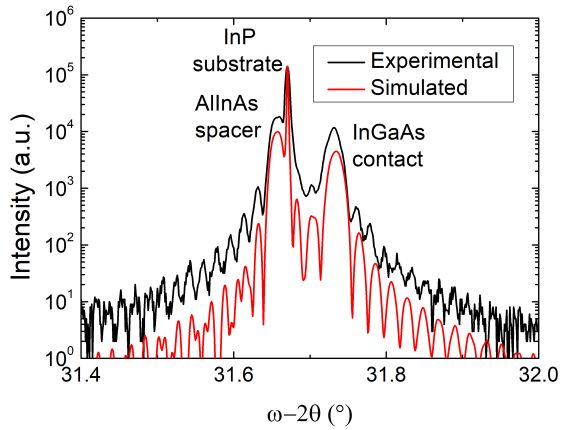
4.3.4 Material characterization

The crystalline structures of the two possible polarities were studied by XRD. Figure 4.8(a) presents the experimental scan performed on the p/n structure (black line), compared to a simulated curve (red line). The AlInAs p+ spacer presents a slight compressive strain of +170 ppm, which corresponds to a 47% Al content. On the other hand, the InGaAs contact is tensile strained at -860 ppm, for an overall 49% Ga content. In this first, test structure, we grew a 250 nm thick contact layer, which explains the intense correspondent peak. In Figure 4.8(b), the same experimental scan is compared with that of the n/p structure. We can notice a slight, tensile shift of both peaks (reduction of In content in both layers), which results in a lattice matched p+ spacer and a more strained contact (however, this fact should not affect the final performances of the device).

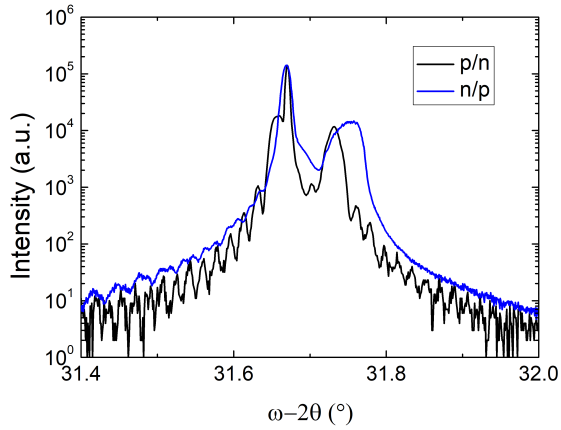
The p/n structure was analyzed using SIMS and compared to an ECV measurement, the results of which are presented in Figure 4.9. The InGaAs contact layer was preliminarily etched as its high doping level had the potential to affect the measurement of the underlying layers. The ECV measure artefacts at the junction are very common in this kind of measurement because of the abrupt interface where the polarity changes. Comparing the two measurements in the AlInAs layers, we can notice that part of the incorporated C is not active: this is in line with the observations made in other studies [22]. Since the structure underwent to the typical Zn activation procedure, we can deduce that this mechanism is completely different.

Figure 4.10 shows an HAADF-STEM image of the p/n sample, and this image demonstrates the absence of structural defects and the high quality of the materials (despite the low growth temperature). It is possible to notice the InP:S/AlInAs:C and the AlInAs:C/AlInAs:C interfaces at the centre and on the right of the picture, respectively. In the image, we can easily distinguish AlInAs from InP since its detected sites present more stretched shapes, due to the presence of two different large atoms such as In and As. On the other hand, P and Al are too small to be distinguished. The p-n interface is also magnified in the inset. The interface between the two different AlInAs:C layers is visible because of their two different chemical compositions. On the other hand, it is not possible to distinguish the interface between the two InP layers. The structure presented the same homogeneity even on larger areas.

Figure 4.11 presents the EDX profiles of the majority elements close to the p-n junction in the p/n sample. In particular, (a) represents In, (b) Al, (c) As and (d) P. The C and S elements were not detected because of their



(a)



(b)

Figure 4.8: (a) Comparison of experimental and simulated XRD profiles of the p/n structure. The left peak (+170 ppm) corresponds to the compressive strained AlInAs p+ buffer (∼ 47% of Al content), the right one (-860 ppm) to the tensile strained InGaAs contact (∼ 49% of Ga content). In this structure, the InGaAs thickness was increased at ∼ 250 nm. (b) Comparison with the n/p structures. In n/p, both the materials are slightly in tension compared to p/n: the p+ spacer is lattice matched to InP, whereas the more strained InGaAs should not affect the final operation. This last layer also presents a lower crystalline quality, as can be determined by its wider peak (despite the fact that we could not find satisfactory explanations for this).

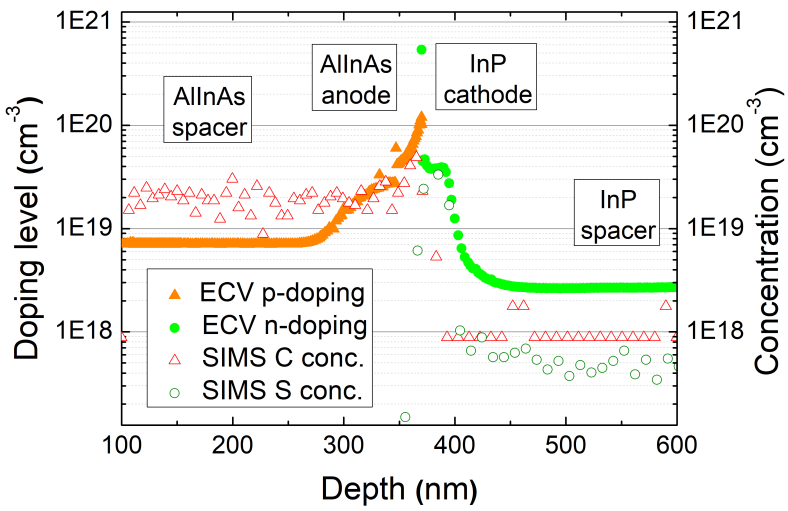


Figure 4.9: SIMS (C and S) and ECV profiles of the structure presented in Table 1 (empty and filled symbols, respectively). The InGaAs contact layer was etched before the ECV measure to prevent effects on the sensitivity of the deeper layers due to its high doping. In the n+ spacer layer, the doping was performed by Si.

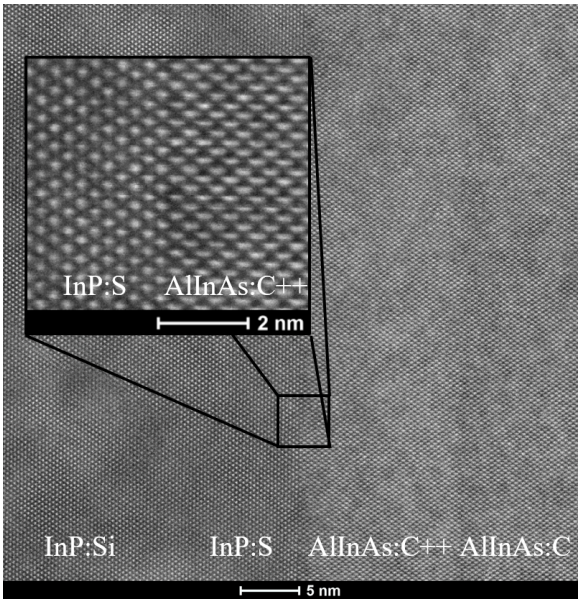


Figure 4.10: HAADF-STEM image of the sample showing, at the centre and in the subfigure, the interface between the InP:S (on the left) and the AlInAs:C anode (on the right); and, on the right, the interface between the two different AlInAs layers. This interface is visible as the layers have different chemical compositions.

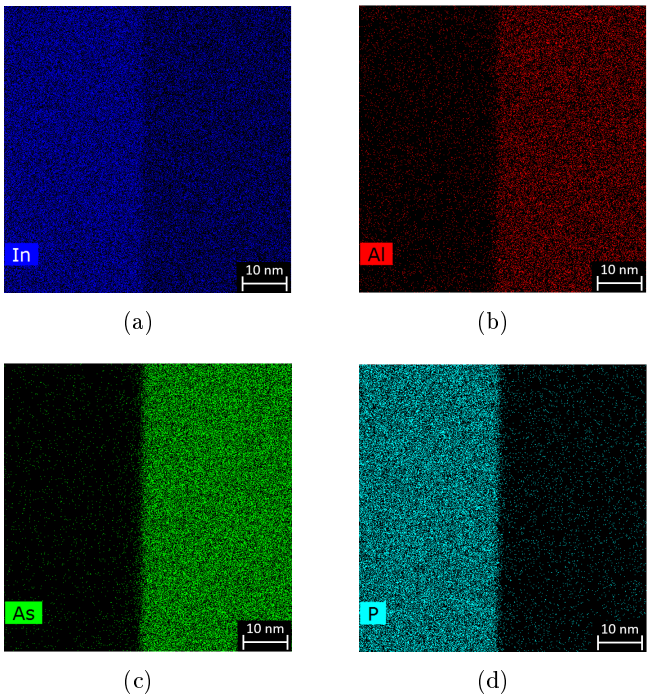


Figure 4.11: EDX pictures of (a) In, (b) Al, (c) As and (d) P (majority elements) distributions in correspondence of the junction.

very low concentration. It is possible to appreciate the abruptness of the interface for each element (only In is present in both the sides, although in very different concentrations).

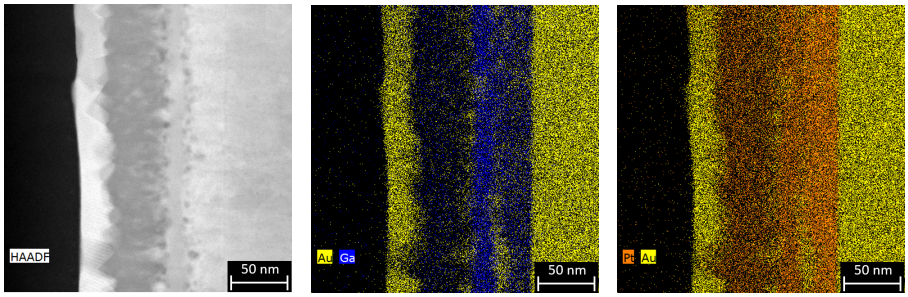
All the performed characterizations confirm the high quality of the structures. Such samples can therefore be processed into final devices.

4.4 Processing of the tunnel junctions

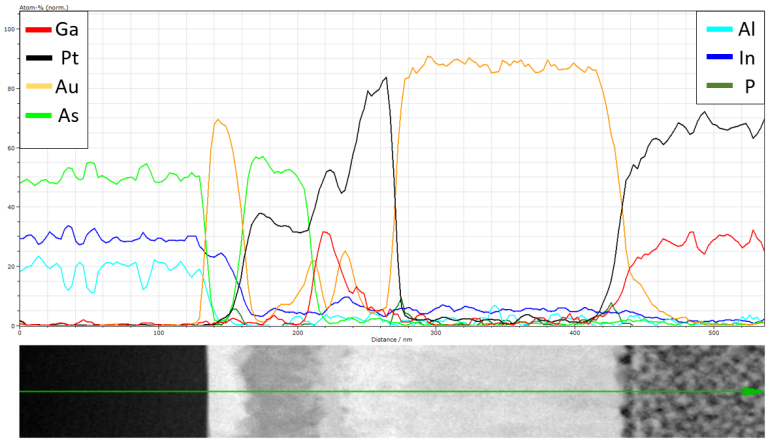
The processing of a tunnel junction is much more straightforward than that of a solar cell. It requires only one mandatory photolithographic step for the realization of the front contact. The other main steps are the mesa etching, the back contact deposition and, if necessary, the deposition of a passivating nitride.

In this case, the front metallic contact is obtained with the lift-off technique presented in section 3.4.3. The choice of the metallic contacts is driven by the polarity of the device: the p/n structure, like the solar cells, presents

a final p-type InGaAs layer and requires, therefore, the usual Pt/Au contact. Since the extraction of the carriers is less problematic than for solar cells, the thicknesses of these metals are reduced to 50 and 150 nm, respectively. Also, this time, a RTA is mandatory for the formation of a good contact. On the other hand the n/p structure requires a n-type front contact, which was made in Ti/Pt/Au (50, 75 and 150 nm thickness, respectively). In this case, an annealing has to be avoided. Figure 4.12 presents a curious phenomenon observed by both HAADF-STEM (a) and EDX (b-d) analysis in correspondence to the Pt/Au front contact interface with the InGaAs contact in a p/n device: a part of the Au seems to have diffused through the Pt and the InGaAs layers, stopped at the interface with the AlInAs spacer (on the left). The result is an Au-rich layer in correspondence with the AlInAs/InGaAs interface. A possible explanation is the reduced thickness of both InGaAs



(a) (b) (c)



(d)

Figure 4.12: (a) HAADF-STEM profile of the front metallic contact. (b) EDX picture of Ga/Au and (c) Pt/Au interdiffusions in correspondence to the front contact. (d) EDX profile of majority elements in correspondence to the front contact (red-Ga, black-Pt, yellow-Au, light green-As, light blue-Al, dark blue-In, dark green-P).

and Pt layers, together with a too-long RTA (in this case, only few seconds at 400 °C should be sufficient). Although not expected, this fact seems to increase the quality of our metallic contact; the barrier function of the AlInAs layer to the metallic diffusion is in turn a remarkable phenomenon that should be studied in more depth.

During the mesa etching, the front metallic patterns are used as masks, avoiding an additional photolithographic step. The mesa wet etching requires the upper side of the junction to be dissolved: in the p/n case, this can be easily obtained by the usual H_3PO_4:H_2O_2:H_2O solution, whereas in the n/p one, it is necessary to use a HCl:H_2O solution to etch the InP layer. As an alternative, the non selective HBr:H_2O_2:H_2O solution presented in section 3.6.2 can be used: for convenience, this second possibility was chosen. The etching time was limited to 15 seconds ($\sim 1.5\mu$m etched).

The back contact metallization was simply performed in the opposite way of the front one: a Ti/Pt/Au contact for the p/n structure and a Pt/Au for the n/p were respectively deposited. This last one required a RTA.

Finally, the deposition of a passivating nitride such as Si_3N_4 can be performed to reduce the electrical losses. In this case, a second photolithography to open the contacts is necessary. Since in this case the anti-reflective behaviour is not needed, there are no constraints on the nitride thickness: we therefore arbitrarily set it at 100 nm.

The n/p configuration requires the annealing of the back contact, while no annealing is required for the front one: it is therefore necessary to deposit the rear contact first to avoid damaging the front one. This involves however that the back contact deposition is performed before the mesa etching, these metals have therefore to be exposed to the acids. When doing this, we noticed that the back Au tends to detach from the sample, reducing the efficiency of the contact. This fact occurs for every chemical solution and is probably due to the use of InP instead of more typical InGaAs for p-type contact. Indeed, Pt/Au is not usually used in p-type contacts on InP; unfortunately, no alternative solutions for this metallization were available in our laboratory. Two possibilities to overcome the issues arising from the realization of this structure, presented in Figure 4.13(a), were proposed: the first one, presented in Figure 4.13(b) consists of introducing a thick, p-type InGaAs layer at the bottom of the structure: in this way, the mesas can be etched up to this layer and the back contact can be directly taken on the front side of the sample, depositing the metals on the exposed InGaAs for a more typical p-type contact. However, this solution presents multiple technical issues, such as the introduction of a further photolithographic mask. The alternative solution, presented in Figure 4.13(c), is to use a typical n-type substrate and to grow an inverted tunnel junction on the bottom of the structure: in this

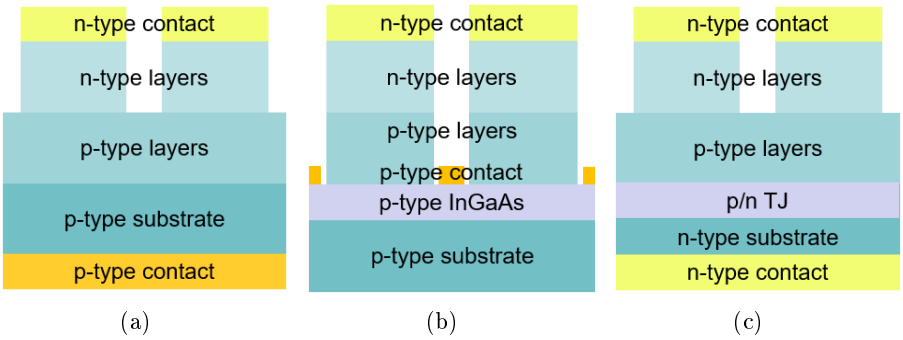


Figure 4.13: (a) Expected final structure for n/p structure. (b) First alternative: introduction of an InGaAs p-type layer. (c) Second alternative: introduction of a second TJ to switch the contact polarity.

way, the polarity of the contact can be inverted and the usual Ti/Pt/Au contact can be deposited on the substrate. Of course, the limitation of this solution is the fact that it can be very hard to distinguish the individual contributions of the two junctions in the final electrical characterization.

In conclusion, no definitive solutions were found for this problem. We could however try to characterize the n/p devices, but the evaluation of the p/n ones remains more promising. Since no particular reasons should justify a different behaviour in the two polarities, a correctly working p/n structure should validate both. Hopefully, the study of the tandem devices will give the proof of validity of the n/p structure as well.

4.4.1 Tunnel junction photolithographic mask

The tunnel junctions processing required the development of a new photolithographic mask. Since J_p of this type of device can be very high (order of $1\,\mathrm{kA/cm^2}$), it is necessary that the patterns not exceed the dimensions of a few hundreds of μm per side (the usual multimeters detecting limit is $\sim 1\,\mathrm{A}$). Such a small size allows us however to produce a lot of devices for every sample; therefore, we set up a production process for 2" quarters.

We designed a single 'cell' composed of 9 different patterns (3 different squares, 2 different circles, 2 different rings, 1 rectangle and 1 rectangle with rounded tips), some of which were repeated for a total of 15 patterns per cell. The different shapes and dimensions allowed us to increase the statistic and to evaluate eventual edge effects. A 2" quarter can contain 12 cells, and we furthermore added the same TLM cell drawn for the solar cell set.

As already mentioned, a passivating nitride can be added and therefore a second photolithographic level would be necessary to open the metallic patterns: it was simply designed by taking the first one and slightly reducing

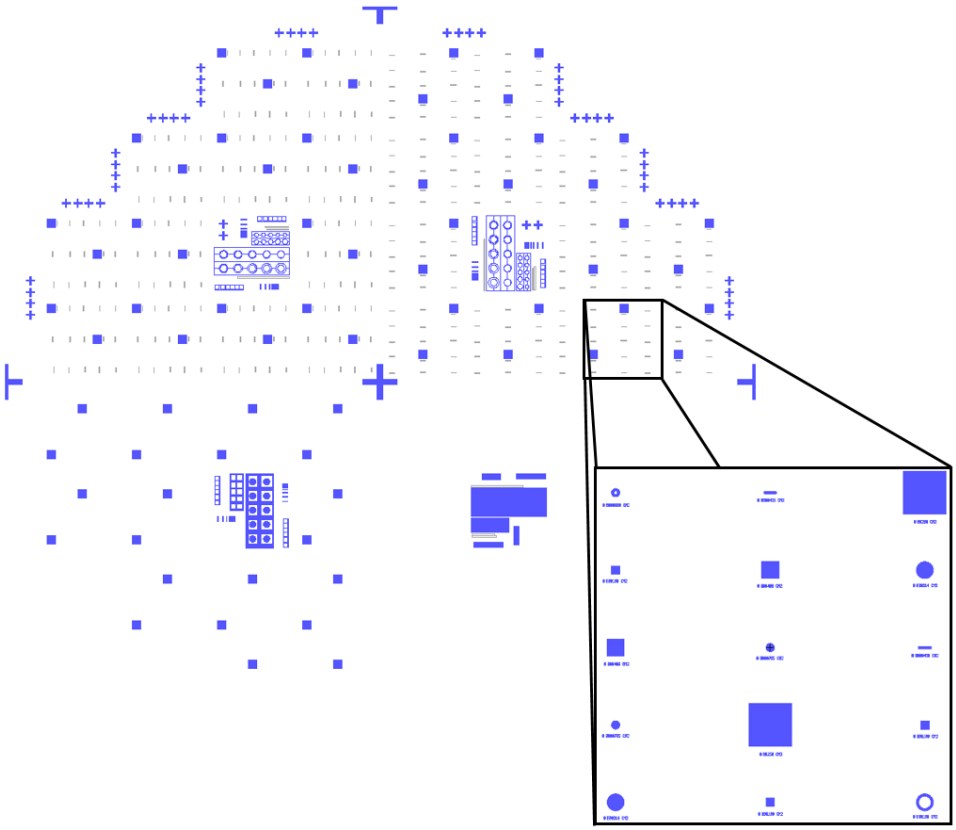


Figure 4.14: Overall mask for the tunnel junctions processing. It is divided into four quarters, each one rotated of 90°. The two top quarters are both for the metallization, the left bottom one for the opening of windows after the deposition of a passivating nitride and the right bottom one for the protection of TLM patterns during the mesa etching. In the inset, detail of the single 'cell' patterns: every one is composed of 9 different shapes, eventually repeated more than once.

every dimension.

The presence of TLM patterns requires us, finally, to protect them during the mesa etching, and we therefore designed a third level to protect this part of the sample.

In conclusion, three different levels were designed (optimized for 2" quarters), one mandatory and two optional. We therefore designed a single photolithographic mask (Figure 4.14) containing all the three levels: every layer is 90° rotated from the previous one, thus guaranteeing the perfect overlap of all the layers. The metallization layer was repeated twice, the other two only once. Figure 4.14 presents a zoom of a single cell.

4.5 Final device characterization

The J-V characteristics of the devices were measured with the four-point probe technique using a Keithley 2000 multimeter, limited to 1 A. The measurements presented unstable characteristics in correspondence to the NDR [33]: during both forward and backward sweeps, no experimental points could be detected in this zone if the scan was starting in one of the two external regions. It was therefore necessary to perform further measurements in the NDR alone to get some points. This precaution, however, did not allow us to accurately detect the steepest zones.

Figure 4.15 presents the J-V characteristic of one of the best results (on a 200 μm side square) for the p/n polarities. The measured J_p was 1022 A/cm^2, whereas r_l was 5.8×10^{-5} Ω·cm^2. The mean measured values were 997 A/cm^2 for J_p and 5.7×10^{-5} Ω·cm^2 for r_l [34]. Such a result proved at the same time the uniformity of the doping levels [35] and the independence of the electrical behaviour from the shape and the dimension of the pattern.

A value of $\sim$ 1000 A/cm^2 is in line with the highest tunnel junctions' lattice matched to InP performances of 1015 and 1600 A/cm^2 obtained by Freundlich [13] and Vilela [14], respectively. These records were however obtained with lower bandgap materials (InGaAs/InGaAs and InP/InP, respectively) and a different growth technique (CBE). Therefore, to our knowledge, our devices now represent the state of the art for MOVPE-grown tunnel

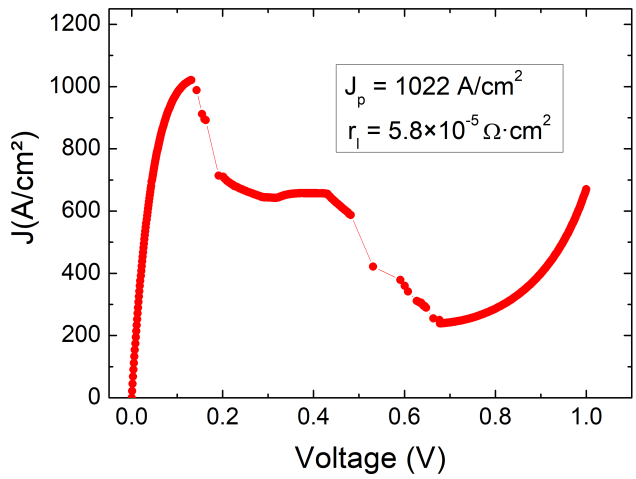


Figure 4.15: J-V characteristic of one of the best obtained p/n tunnel junctions. It was a square, 200 μm side device. The results were highly homogeneous on the whole device, and the mean measured values were 997 A/cm^2 for J_p and 5.7×10^{-5} Ω·cm^2 for r_l.

junctions lattice matched to InP.

The obtained result is much (approximately five times) higher than the minimum value required to operate under an ultra high concentration of 10 000 suns (for InP based cells). It should also be high enough to compensate for the degradation of the performances due to the upper cell high growth temperature, although no specific tests were performed to demonstrate it (the highest annealing to which we have subjected our devices was the one minute at 400 °C RTA).

By performing TLM measurements, we confirmed the results presented in Figure 3.8(b) at page 74 (contact resistivity at the order of $10^{-6}\,\Omega{\cdot}\mathrm{cm}^2$) and demonstrated therefore that $\sim$ 10% of the measured r_l was due to the contact resistance. The remaining 90% is a very reliable forecast of the tunnel junction contribution to the total resistance in a solar cell. Such a low value implies that the voltage drop at the junction is extremely low (only 10-12 mV in the case of 10 000 suns light concentration).

As expected, it was not possible to obtain a significant result from the measurement of the n/p devices because of the too-high contact resistance. However, the excellent results obtained with the inversely grown structure allow us to be highly optimistic about the final operation of the second structure as well. The best way to validate the second structure consists therefore of inserting it in the final tandem device and evaluating the final performances.

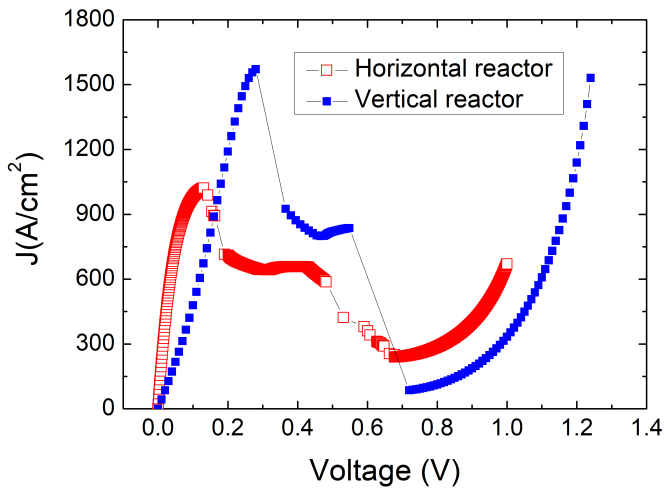


Figure 4.16: J-V characteristic of one of the best obtained p/n tunnel junctions grown with the vertical reactor (blue line). The previous result is reported as well (red line) for comparison. The new device presented a 1571 A/cm^2 J_p and a $1.6{\times}10^{-4}\,\Omega{\cdot}\mathrm{cm}^2$ r_l.

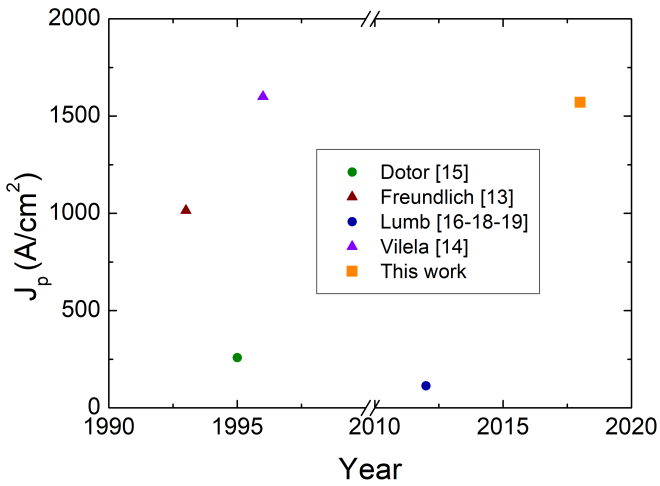


Figure 4.17: Summary of the current J_p state of the art for InP tunnel junctions. The square represents our MOVPE grown device, whereas the circles represent MBE grown and the triangles CBE grown devices. It is possible to notice how our devices are currently in line with the InP state of the art.

As in the solar cells study, moving from a horizontal reactor to a vertical one required to export the obtained know-how to a larger, industrial machine. All the previous studies were performed again and tunnel junctions identical to the presented p/n devices were grown and processed a second time, following the same procedures. Figure 4.16 presents the new result (blue line), compared to the previous result (red line): the new devices presented a noticeable increase in the mean J_p, moving from $\sim 1000\,A/cm^2$ to $\sim 1550\,A/cm^2$, and an analogous increase of the mean r_l from $5.7\times10^{-5}\,\Omega\cdot cm^2$ to $1.7\times10^{-4}\,\Omega\cdot cm^2$. Since the structure and the processing were kept the same, these increases were certainly due to the use of the new reactor. Actually, both increases, although not negligible, have no relevant impacts on the final performances of a tandem device working under high solar concentration: we saw previously that such a high J_p is largely sufficient to work even under high solar concentration, whereas the new r_l should imply a still negligible voltage drop of $\sim$ 32-34 mV under 10 000 suns concentration. Nevertheless, the new obtained J_p is in line with the record value presented by Vilela and can be considered a state of the art for tunnel junctions lattice matched to InP, as presented in Figure 4.17. Furthermore, it is worth noting once again that such a result was obtained with higher bandgap materials compared to the previous, meaning that our device is therefore better suited for photovoltaic applications.

4.6 The InP/InGaAs tandem solar cell

With the validation of the tunnel junction presented above, all the three components of the final InP/InGaAs tandem device were realized. It is then possible to combine them into a single cell. In the next sections, we will present the structure, the realization and the photovoltaic performances of this final device.

4.6.1 Presentation of the device

The structure of the tandem device is presented in Table 4.6. It is based on the structures optimized in the previous chapter, sample J (InP cell with AlInAs window layer) for the top cell and the presented InGaAs device for the bottom cell, and on the InP:S/AlInAs:C tunnel junction presented above. Nevertheless, some layers had to be slightly modified for the integration in the tandem cell. In particular, the top cell presents a thinner BSF compared to the single junction device (500 nm instead of 700), as it does not act as a buffer layer in this case. On the contrary, the BSF of the bottom cell is thicker (600 nm instead of 400) in anticipation of the future growth on a Si template, which will require a thicker buffer layer. The bottom cell was also

Function	Material	Thickness (nm)	Dop. level (cm^{-3})
Contact layer	$In_{0.53}Ga_{0.47}As$:Zn	250	$+2\times10^{19}$
Stop etch	InP:Zn	20	$+1.5\times10^{18}$
Window layer	$Al_{0.48}In_{0.52}As$:Zn	25	$+1.5\times10^{18}$
Emitter	InP:Zn	150	$+1\times10^{18}$
Transition layer	InP nid	20	–
Base	InP:Si	3000	-1×10^{17}
BSF	InP:Si	500	-2×10^{18}
TJ cathode	InP:S	15	-4×10^{19}
TJ anode	$Al_{0.48}In_{0.52}As$:C	15	$+4\times10^{19}$
Window layer	$Al_{0.31}In_{0.53}Ga_{0.16}As$:Zn	30	$+1.5\times10^{18}$
Emitter	$In_{0.53}Ga_{0.47}As$:Zn	200	$+1\times10^{18}$
Transition layer	$In_{0.53}Ga_{0.47}As$ nid	20	–
Base	$In_{0.53}Ga_{0.47}As$:Si	3000	-1×10^{17}
BSF	InP:Si	600	-2×10^{18}
Substrate	InP:S	3.5×10^{5}	-2×10^{18}

Table 4.6: Structure of the realized tandem solar cell. The InP top cell is based on sample J presented in the previous chapter, and the InGaAs bottom cell is similarly based on the best device presented in the same chapter. The two cells are connected by the tunnel junction presented above. Minor variations on BSFs thickness and bottom contact layer have been made.

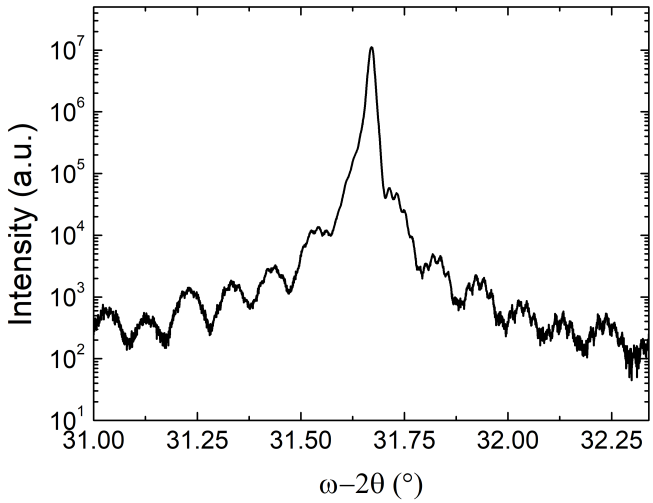


Figure 4.18: XRD scan of the realized tandem device. The width peak is due to the thick, almost lattice matched InGaAs layers.

grown without InGaAs contact layer and InP stop etch, which are useless in this new structure. None of these minor changes should affect (in a relevant way) the photovoltaic performances of the device. All other parameters (thicknesses of other layers and doping levels) were kept equal to those of the optimized structures. Only the anode and the cathode of the structure presented in Table 4.3 were used as a tunnel junction.

4.6.2 Growth and processing

The manufacturing process developed and optimized for single junction solar cells and presented in the previous chapter is completely transposable to a more complex system such as a tandem device.

The growth (performed in the vertical reactor) did not present any further difficulties compared to the previous cases and the growth conditions were the same. Figure 4.18 presents the material characterizations: the surface of the sample is completely mirror like, whereas the XRD scan shows a structure lattice matched to InP.

The processing followed the same procedure developed for the last solar cells: the front and back contact metallizations were performed by DIBS, whereas the mesa chemical etching was performed by $HBr:H_2O_2:H_2O$ solution. The ARC thickness was optimized on the InP absorption wavelength, at 115 nm. During the front contact lift off, some irregularities, probably due

to a degraded photoresist, have emerged: in some cells not all the surplus metal was lifted, whereas in others the internal fingers were locally lifted as well. In total, around half of the cells have been lost. However, the remaining devices allowed to characterize the photovoltaic performances of the structure.

4.6.3 Tandem device photovoltaic performances

The J-V characteristic under illumination of the best device of the presented structure is shown in Figure 4.19 (blue line), compared with the characteristics of the two single junction devices composing the tandem cell (red line for the InP top and green line for the InGaAs bottom cell, respectively). The photovoltaic parameters of this device are reported in Table 4.7, together with the best results obtained with the two single constituting cells: this device presented a J_{SC} of 20.8 mA/cm^2, a V_{OC} of 1.05 V, a FF of 83.9% and a η of 18.27%. From the comparison with the single cells' performances, we can effectively notice how the overall J_{SC} is limited by the lower one (the small discrepancy between 20.6 of the InP cell and 20.8 mA/cm^2 of the tandem is negligible). On the other hand, the overall V_{OC} is around 100 mV lower than expected (the sum of the single contributions): as the J_S extrapolated from the dark measurements is quite high (10^{-6} A/cm^2), we suspect that the usual passivation limit can affect this value. Nevertheless, the excellent quality of the device is demonstrated by FF, higher than those of the two

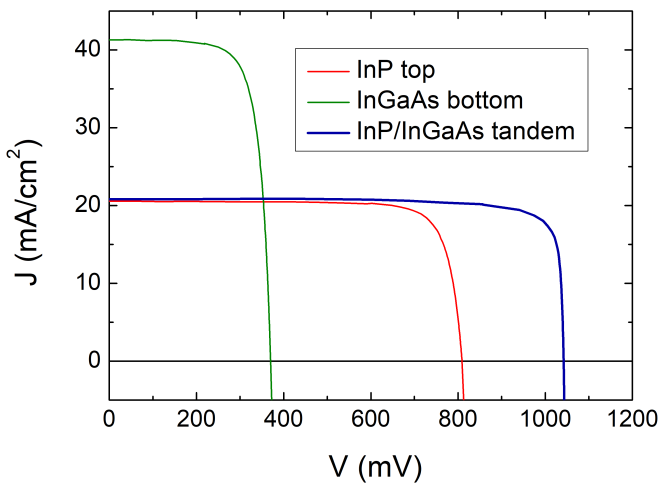


Figure 4.19: J-V characteristic under illumination of the best obtained InP/InGaAs tandem cell (blue line) compared to the single J-V characteristics of InP top cell (red line) and InGaAs bottom cell (green line).

	InP top	InGaAs bottom	InP/InGaAs tandem
J_{SC} (mA/cm^2)	20.6	41.2	20.8
V_{OC} (mV)	809.3	369.9	1045.9
FF (%)	81.4	74.5	83.9
η (%)	13.53	11.38	18.27

Table 4.7: Photovoltaic parameters of the best tandem cell, compared with the best records of the two single constituting cells.

constituents (thanks to an extremely low R_s and a very high R_{sh}). The overall η, although limited by the low J_{SC} of the top cell, is however a very interesting and promising result, notably higher than the few results that can be found in literature [14]. This is certainly also due to the excellent quality of our tunnel devices, which allow an optimal transmission of the photogenerated carriers. The use of transparent materials for this component was definitely another advantage. Reciprocally, the good performances of the tandem devices are the final proof of the quality of the n/p polarity for the tunnel junction (which, we recall, could not be validated alone). The very low R_s makes this device an interesting possibility for a concentrated photovoltaic application, as well.

Figure 4.20 presents the EQE characteristic of the best tandem device, compared to those obtained on the constituing InP (red line) and InGaAs (green line) cells standalone. To obtain this characteristic, the single contributions of the top (violet line) and bottom (orange line) cells had to be evaluated. In order to do that, each cell had to be separately saturated by a proper light source, so as to isolate the single contribution of the second one. In particular, the top cell was saturated by a 785 nm wavelength laser source; whereas the bottom cell by a properly filtered halogen lamp. As expected, the InP top cell standalone and the integrated one present similar behaviours, in particular in correspondence of the 600-900 nm range. On the other hand, the bottom cell contributions present a relevant difference if integrated or not. This is particularly true in the 1200-1600 nm range. Such a discrepancy can be partially explained by the different thickness of the ARC between the two cells: when standalone, the InGaAs cell presented a nitride thickness optimized for absorption wavelengths around 1600 nm, which guaranteed a minimization of the reflection. In the tandem cell case, the ARC thickness was optimized for wavelengths around 900 nm; which means an important increase of the reflection when moving far from this value. In fact, the bottom cell contribution to the tandem's EQE decreases when increasing the wavelength. Furthermore, the typical losses arising from a non-optimized passivation of the InP top cell may influence the performances of the bottom cell as well. However, the evaluation of a tandem cell's EQE is a compli-

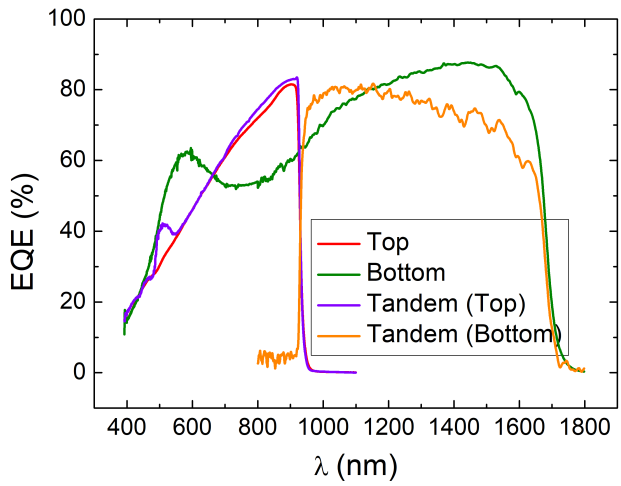


Figure 4.20: EQE characteristic of the best InP/InGaAs tandem solar cell. It was obtained by separately measuring the contributions of the top (violet line) and of the bottom (orange line) cells. The results are compared with the results obtained on the single cell (red line for InP and green line for InGaAs).

cated step, which requires many attentions compared to a single junction. Furthermore, we were not equipped with an experimental set-up optimized for kind of measurement. Therefore, we can not exclude that the obtained results presented some mistakes.

However, the presented graph shows a good coverage of the incident spectrum by the two cells, which demonstrates the validity of our choice for the constituting semiconductors. Of course, an improvement of the layers' thicknesses and of the ARC will allow to increase the overall coverage and performances.

4.7 Conclusions

In this chapter, we firstly presented the realization of high quality tunnel junctions, able to work in our typical conditions but also under high solar concentration conditions. We then combined these devices with the single junction InP and InGaAs solar cells presented in the previous chapter in an overall, tandem device. The photovoltaic performances of such a device are very promising and ready to be tested even under solar concentration conditions. With this excellent result, we can consider all the goals related to the photovoltaic devices realized onto InP substrates completely fulfilled. In the next chapter, we will then address the second and final part of this work: a proper template for the integration of the presented photovoltaic devices

onto Si substrates will be researched. Then, the devices will be realized onto Si and the effects of this integration on the photovoltaic performances will be evaluated.

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Chapter 5

Towards Si integration of III-V solar cells

Contents

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Once all the target photovoltaic devices were realized and optimized, our attention shifted to the integration of some structures onto Si substrate. The first part of this chapter will be dedicated to the choice of the best template to use for this integration. Different tests and characterizations will be presented and the final choice will be justified. In the second part, the quality of the preliminary growth will be evaluated and the characterizations of the first solar cell presented. We will then present the newly developed processing, which deals with the presence of a different type of substrate and then of different issues. The final part will be dedicated to the presentation of the photovoltaic results and a comparison with the same devices obtained on InP, showing the effects of the growth on a mismatched substrate and presenting the most limiting factors.

5.1 Presentation of the templates

The different templates and approaches investigated in this work were already briefly introduced in section 1.4. In this and the next sections, we will present in more details the properties of these structures. The choice of a final template for the Si integration of our solar cells will be justified.

The first approach was developed in collaboration with IES, a laboratory at the University of Montpellier-CNRS. The potential of an AlSb nucleation on Si has already been demonstrated [1]: this material leads to efficient strain relaxation after the growth of a few monolayers. By using an intermediate III-(As)Sb template, it could be therefore possible to grow materials with the same lattice parameter of InP.

The two provided templates, presented in Tables 5.1(a) and (b), were grown by Molecular Beam Epitaxy (MBE) using a reactor equipped with As/Sb valved cracker cells. The growths were carried out on off-axis (0 0 1) n-type Si substrates 6° tilted towards the [1 1 0] direction, in order to limit the formation of APDs. The substrates underwent preliminary ex-situ and in-situ treatments for surfaces cleaning and de-oxidation before the growths [2].

In the first template (IES_a), the first 4 AlSb monolayers were followed by 200 nm of GaSb. This structure was already successfully used for the realization of efficient III-Sb lasers integrated onto Si [3–5]. For our application, a final $In_{0.53}Ga_{0.47}As$ layer was added to move back to the InP lattice parameter (the choice of using an InGaAs layer instead of an InP one was motivated by the absence of a P source inside the MBE reactor).

InGaAs	78 nm
GaSb	200 nm
AlSb	4 ML
Si substrate	

(a)

InGaAs	500 nm
AlSb	4 ML
Si substrate	

(b)

InP	1 μm
GaP	60 nm
Si substrate	

(c)

InP	150 nm
GaAs	400 nm
Si substrate	

(d)

Table 5.1: (a) IES_a template. (b) IES_b template. (c) NAsP template. (d) LTM template.

The growth was monitored by Reflection high-energy electron diffraction (RHEED): since a 3D growth of the InGaAs layer after some tens of nm was noticed, the growth was stopped after deposition of the first $\sim$80 nm (although the initially target thickness was 500 nm). A new growth was performed without the intermediate GaSb layer: the new template (IES_b) was made of a 500 nm InGaAs layer directly grown onto the 4 AlSb monolayers.

The second approach was developed in a purely industrial environment, the tested template was indeed realized by the NAsP company [6]. In this case, the intermediate nucleation layer was GaP, which is almost lattice matched to Si [7].

The NAsP template, presented in Table 5.1(c), was grown on a 12" (0 0 1) Si substrate. After a chemical etching followed by a high temperature annealing directly in the VPE chamber to deoxidize the substrate, a $\sim$ 500 nm thick Si buffer was grown using SiH_4 as a precursor. A 60 nm thick GaP layer was then grown by MOVPE using tertiarybutylphosphine (TBP) and triethylgallium (TEGa) as majority precursors [6]. In this case, the APDs' formation was limited by combining a specific preliminary substrate annealing to form a double-stepped surface with a post growth thermal treatment of GaP [8].

The production of a high quality GaP/Si template opens a lot of interesting possibilities, from the growth of lattice matched Ga(NAsP) devices [9] to the development of mismatched structures from GaAs [10] to InAs/GaSb [11]. In the case of a mismatched growth, intermediate metamorphic layers such as $GaAs_xP_{1-x}$ and AlP_xSb_{1-x}, as well as direct growth, can be used. For our template, a 1 μm thick InP layer was directly grown by NAsP on the GaP layer by MOVPE.

The 12" template was then cleaved in smaller parts ($\sim$ 2/3 cm side squares) to be used in III-V Lab facilities.

The third approach can be seen as an intermediate solution between the two previously presented: produced by LTM, a laboratory from University of Grenoble-CNRS, the template used an intermediate lattice parameter buffer layer, GaAs.

This template is presented in Table 5.1(d): a 12" (0 0 1) Si substrate was initially deoxidized with a NF_3/NH_3 remote plasma and a high temperature annealing directly in a MOVPE reactor, followed by a quick reactor quenching to freeze the Si surface [12]. The GaAs layer was then deposited with a two-step process [13]: a 40 nm thick GaAs nucleation layer was deposited at low temperature (400-500 °C), followed by a 360 nm thick layer deposited at a higher temperature (600-700 °C), for an overall thickness of 400 nm. The precursors were TMGa and TBAs. Such a procedure allowed the growing of free layers, although the measured TDD was very high (10^9 cm^{-2}). Nevertheless, this structure was already successfully applied in the production of

quantum dot lasers grown onto Si substrates [14].

Finally, a 150 nm thick InP layer was grown atop the GaAs buffer layer. As for the previous template, the sample was cleaved in smaller parts to increase the number of possible tests.

By performing a series of preliminary characterizations on the provided templates, presented in the next section, it was possible to determine which of the proposed possibilities was the best for the Si integration of our solar cells.

5.2 Preliminary characterizations

The quality of the four different templates was evaluated by performing a series of characterizations such as optical microscopy, XRD and AFM. The same characterizations were performed after ten minutes' annealing at 700 °C (the IES templates under AsH_3 and the NAsP and LTM templates under PH_3 flows, respectively) in the MOVPE reactor, in order to evaluate the effects of the preliminary annealing during the growth of the solar cell structure.

The results on the template IES_a are presented in Figure 5.1: figures (a) and (b) represent the surface morphology before and after annealing, respectively. The surface before the growth was quite smooth and did not present relevant influences from the 3D growth suggested by the RHEED check. The high temperature annealing did not affect the quality at this macroscopic level. The comparison between the XRD scans (c) is much more interesting: the unannealed sample (black line) presents four peaks (plus Si substrate peak), none of them presenting the expected intensity for the considered thicknesses. The second peak from the left coincides with a 100% relaxed GaSb layer, whereas a 100% relaxed $In_{0.53}Ga_{0.47}As$ peak should fall between the third and the fourth peak. It is reasonable to see both these peaks as different phases of a 3D grown layer, as suggested by RHEED. The first peak on the left can be perhaps also be seen as a different InGaAs phase. The scan on the annealed sample (red line) presents divergent behaviours of the peaks: whereas the GaSb peak moves towards a less compressively strained position (due to the thermal effect), the other peaks present alternatively more or less compressive shifts (we could not find a satisfactory explanation for the more compressive one). The instability of the system led to the formation of different layers and perhaps polycrystals. This was confirmed by AFM: the measurements (d-e) pointed out the very high root mean squared (RMS) roughness of the initial structure (10.0 nm), which was further increased by annealing (42.0 nm). Such a value is abso-

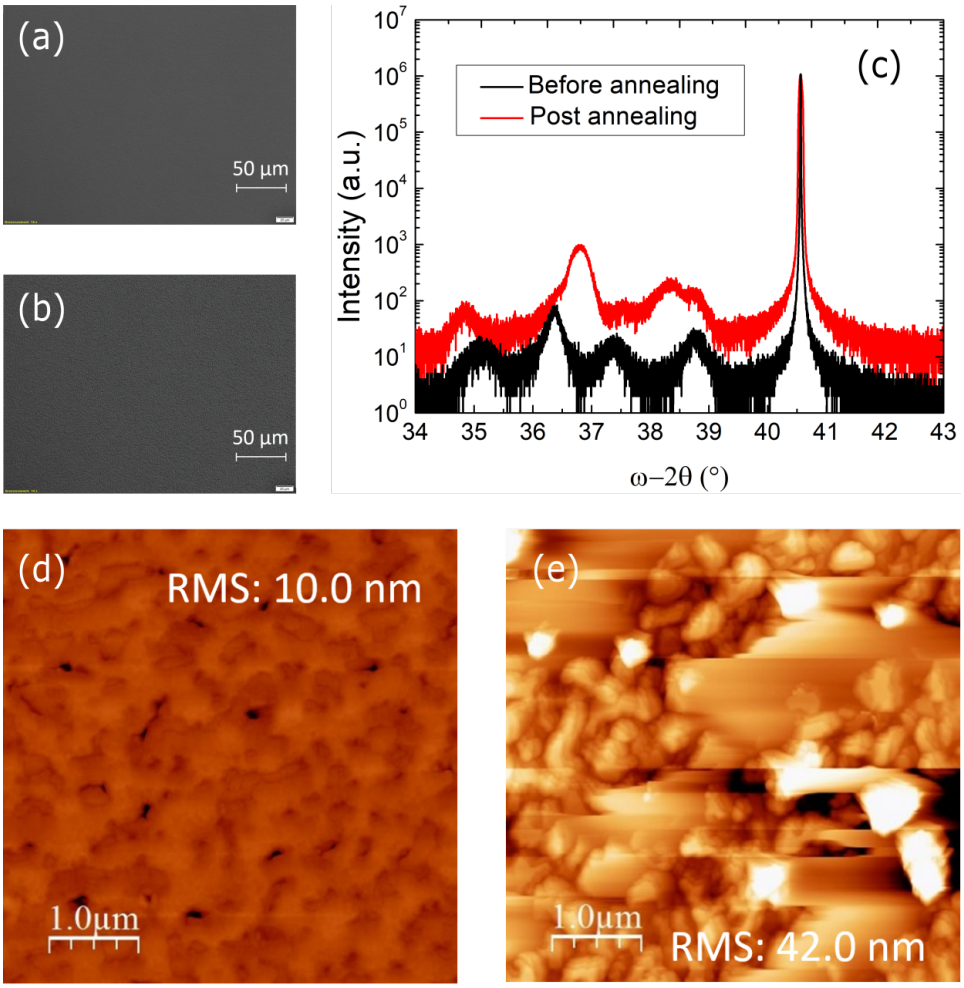


Figure 5.1: IES_a sample before and after the 700 °C annealing: morphology (a) before and (b) after; (c) XRD scan; AFM (d) before and (e) after.

lutely incompatible with epitaxial overgrowth.

The direct growth of the InGaAs layer onto the AlSb nucleation layer of template IES_b (the characterizations of which are presented in Figure 5.2) allowed us to prevent 3D growth. Compared to the previous template, the XRD scan presents only one defined peak for the InGaAs layer: assuming a 100% relaxation, this peak is fitted for a 43% Ga composition. The high temperature annealing did not considerably affect the crystalline structure. On the other hand, the RMS was increased from 8.6 nm to 19.0 nm during annealing: although this value is reduced compared to that of the previous template (despite having a worst macroscopic morphology), it is still too high for MOVPE regrowth.

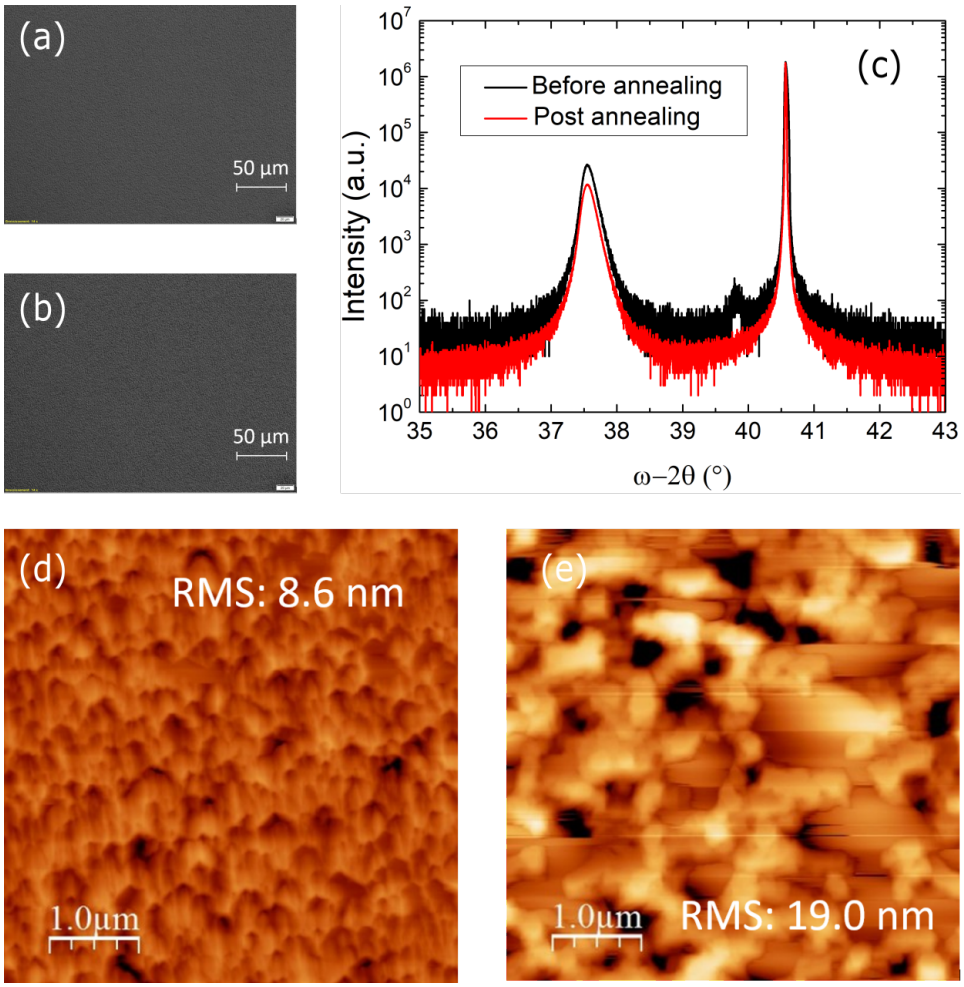


Figure 5.2: IES_b sample before and after the 700 °C annealing: morphology (a) before and (b) after; (c) XRD scan; AFM (d) before and (e) after.

The NAsP template presented a mirror like surface morphology, not affected by the usual high temperature annealing, as showed in Figures 5.3(a-b). The XRD scans (c) present very sharp peaks with reduced full width at half maximum: the peak mismatched at 0.77% corresponds perfectly to fully strained GaP, whereas the one at 8.38% matches with fully relaxed InP. The structure is not at all affected by annealing. The AFM scans presented an RMS of 1.9 nm before annealing and after annealing a RMS of 3.0 nm. This value is acceptable for our purposes, even if we have to consider that the deposition of several μm layers during the solar cells growth may either decrease or increase it.

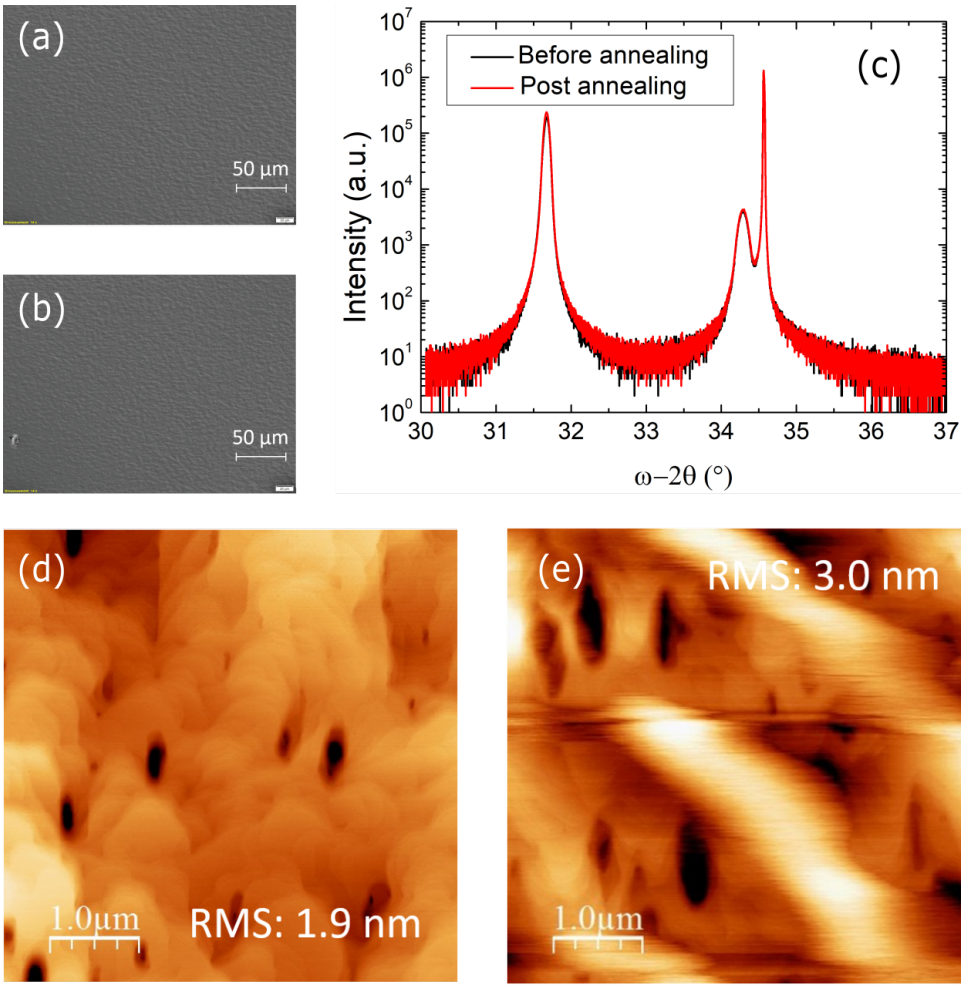


Figure 5.3: NAsP sample before and after the 700 °C annealing: morphology (a) before and (b) after; (c) XRD scans; AFM (d) before and (e) after.

Finally, the characterizations of the LTM template are presented in Figure 5.4. The morphology evaluated by optical microscopy is smooth, although the various samples present scratches due to the cleavage procedure. The XRD scan before annealing revealed a 100% relaxation for GaAs and 93% for InP. This result was confirmed by a RSM scan around the (2 2 4) direction. The annealed structure presented a slight shift of both peaks towards the substrate one, which was expected from the thermal relaxation. Annealing caused a very slight increase of the RMS from 1.4 nm to 1.5 nm.

Table 5.2 presents a summary of the main properties, before and after annealing. The most promising template is undoubtedly the one provided by NAsP, since it combines a good surface morphology with an excellent

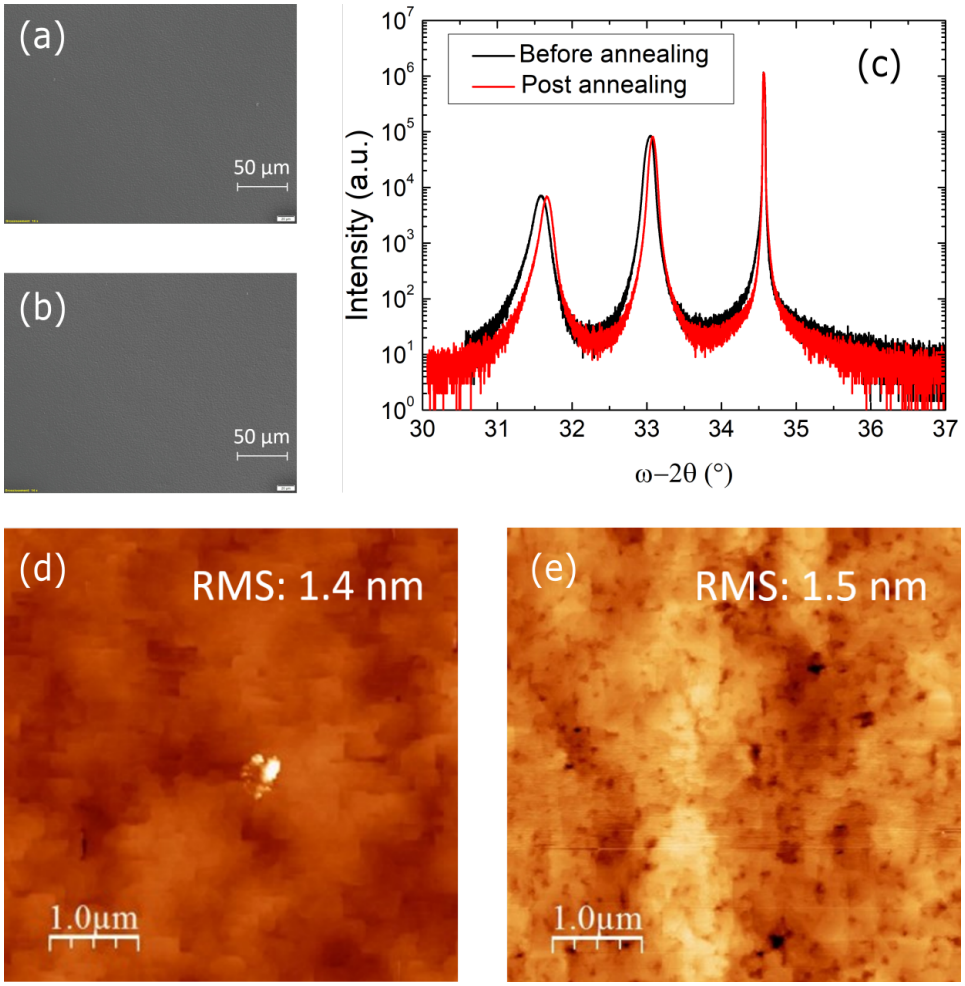


Figure 5.4: LTM sample before and after the 700 °C annealing: morphology (a) before and (b) after; (c) XRD scans; AFM (d) before and (e) after.

	Morphology		Relaxation [%]		RMS [nm]	
	Pre	Post	Pre	Post	Pre	Post
IES_a	✓	✓	3D	3D	10.0	42.0
IES_b	✗	✗	100	100	8.6	19.0
NAsP	✓	✓	100	100	1.9	3.0
LTM	✓	✓	93	> 93	1.4	1.5

Table 5.2: Summary of the main structural properties of the considered templates before and after annealing (optical microscopy, XRD and AFM characterizations).

crystal quality. The RMS should be further limited by our thick depositions. The LTM template presents interesting properties as well, although the not

completely relaxed superficial InP could affect the lower layers of our devices (the thick deposition should anyhow guarantee a complete relaxation of the overall devices). Between the two different templates, we decided to carry on the study on the NAsP one for a logistic reason (more substrates available). Finally, the IES templates, although potentially interesting, were not mature enough for our purpose.

5.3 TEM analysis of NAsP template

A deeper evaluation of crystalline properties of (0 0 1) NAsP templates was carried on by performing a series of STEM and TEM scans towards the (1 1 0) direction. Figures 5.5(a) and (b) present HAADF-STEM scans of the GaP/InP interface for different magnifications. In both images, it is possible to notice the presence of periodical misfit dislocations (examples indicated by the orange arrows) at the interface, arising from the different lattice parameters ($a_{GaP} = 5.4505$ Å and $a_{InP} = 5.8687$ Å, respectively). In particular, (b) was treated with a band-pass filter by ImageJ software [15] (c), then the FFT of the image was performed (d). From this last figure, it was possible to determine a GaP/InP ratio of 14/13 at the interface (in line with theory, as $14 \cdot a_{GaP} = 13 \cdot a_{InP}$), and the misfit periodicity, which corresponds to 5.07 nm. This value has to be corrected by a factor $\sqrt{2}$, arising from the angle's tilt of the sample during the measurement (the lattice's unity in the figure does not correspond to the lattice parameter, but to the half diagonal of the face-centered cubic structure). The actual misfit dislocations periodicity is therefore 7.17 nm; in line with the theoretical value (7.63 nm) within the experimental error limit. The presence of such a misfit periodicity and the absence of irregular rearrangements at the interface tend to confirm the high quality of the template.

Where STEM images allowed us to evaluate the crystalline structure of the template, TEM revealed the main defects characterizing the sample. Figure 5.6 presents two images for different magnifications of the whole stack. Figure 5.6(a) shows again the presence of misfit dislocations at the GaP/InP interface, as well as some twins. An image treatment allowed us to find a misfit periodicity of 5.2 nm (corrected to 7.35 nm), closer to the theoretical value than the previous case. Figure 5.6(b) presents a larger zone, highlighting the presence of other defects. They are almost completely confined in the InP layer, where the GaP layer was grown almost free of defects on the Si substrate. This is in line with what expected from the different lattice mismatches.

Unfortunately, the measurements performed do not allow us to evaluate

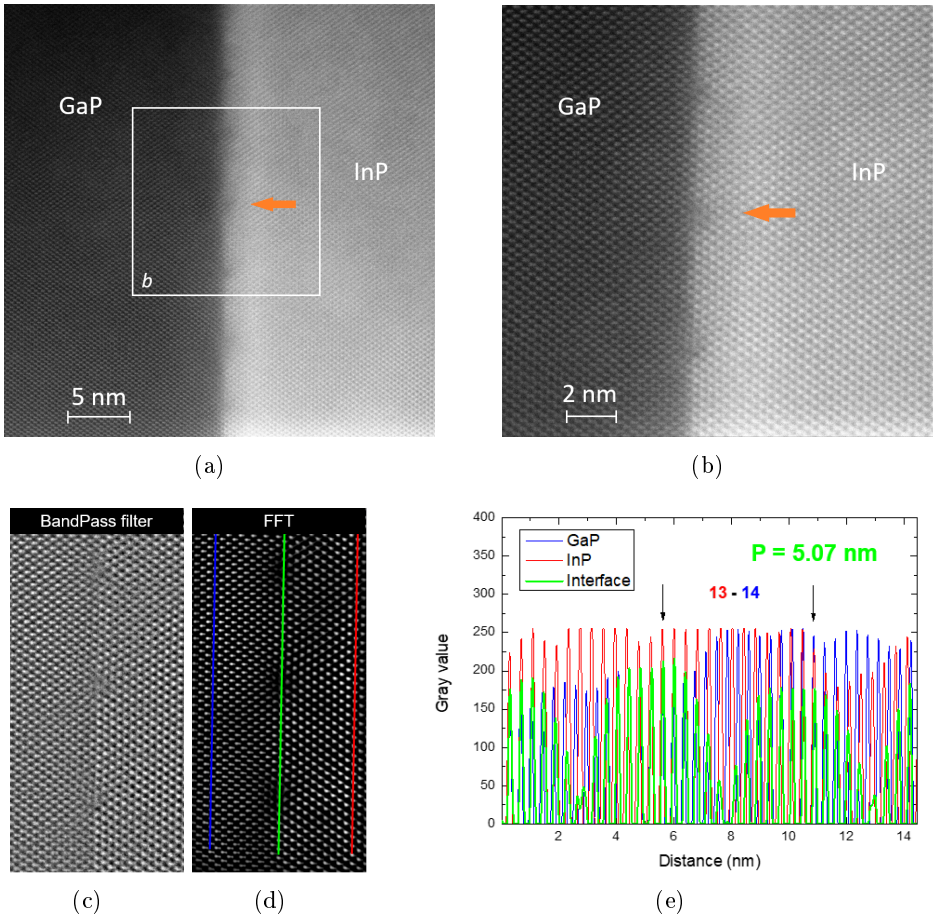
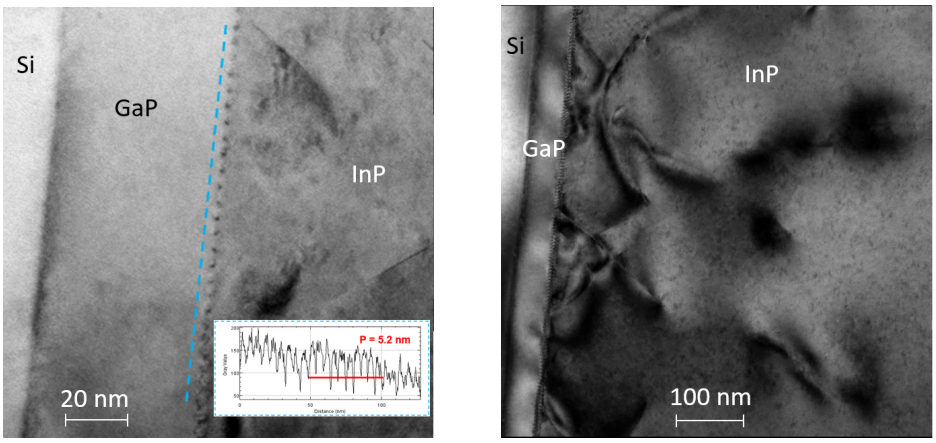


Figure 5.5: (a-b) HAADF-STEM images of the (0 0 1) NAsP template towards the (1 1 0) direction, showing GaP/InP interface for different magnifications. The different lattice parameters generate misfit dislocations (some examples are indicated by the orange arrows) at the interface; (c) band-pass filter treatment by ImageJ software [15] of previous image; (d) FFT treatment of previous image; (e) evaluation of misfits periodicity.

the TDD: the high currents used during the FIB preparation made a wide part of the sample amorphous, thus impeding a reliable statistics.

In conclusion, the measurements performed demonstrated that the crystalline quality of the template was high enough for our purposes, although the quality of the InP layer can be, of course, increased. Anyhow, the layers look sufficiently planarized; the thick depositions for the cells should limit the propagation of defects.



(a) (b)

Figure 5.6: TEM images of the NAsP template showing Si/GaP and GaP/InP interfaces for different magnifications: (a) evaluation of misfits periodicity; (b) some crystalline defects arising from the high mismatch.

5.4 InP cell grown on NAsP template

Once the choice of template was made, the next step was the validation of solar cells' epitaxial growth over the Si substrate. We therefore decided to use sample I presented in chapter 3 (InP solar cell with InP window layer) as a test structure. The reason was the simplicity of the structure (several μm of lattice matched material), compared to the InGaAs and the tandem cells. The InP cell was grown with the same growth conditions as sample I. It was then characterized by the same techniques used for the evaluation of the various templates' quality: optical microscopy, AFM and XRD. The obtained results are presented in Figure 5.7: the surface morphology, despite being completely mirror like to the naked eye, appears slightly rough at both the centre (a) and edges (b). AFM shows that the RMS decreases from 3.0 nm (measured after annealing at 700 °C) to 1.5 nm, a value lower than that we found in the unannealed template (the increasing thickness of the layer tends to level out the roughness). The thermal mismatch induced a series of cracks in the structure (vertical stripes on the whole figure surface, which may have a deleterious effect on the final performances). The XRD scan (d) demonstrates that the thick deposition did not affect the overall quality of the structure: the InP peak is not shifted, furthermore, it presents a thin full widths at half maximum of the peaks, demonstrating that the crystal quality is not affected by the long deposition.

The sample was also characterized by SEM, and the results are presented in Figure 5.8. The cross-section of the sample was evaluated at different magnifications (a-b): it is easy to distinguish the InP layer from the Si

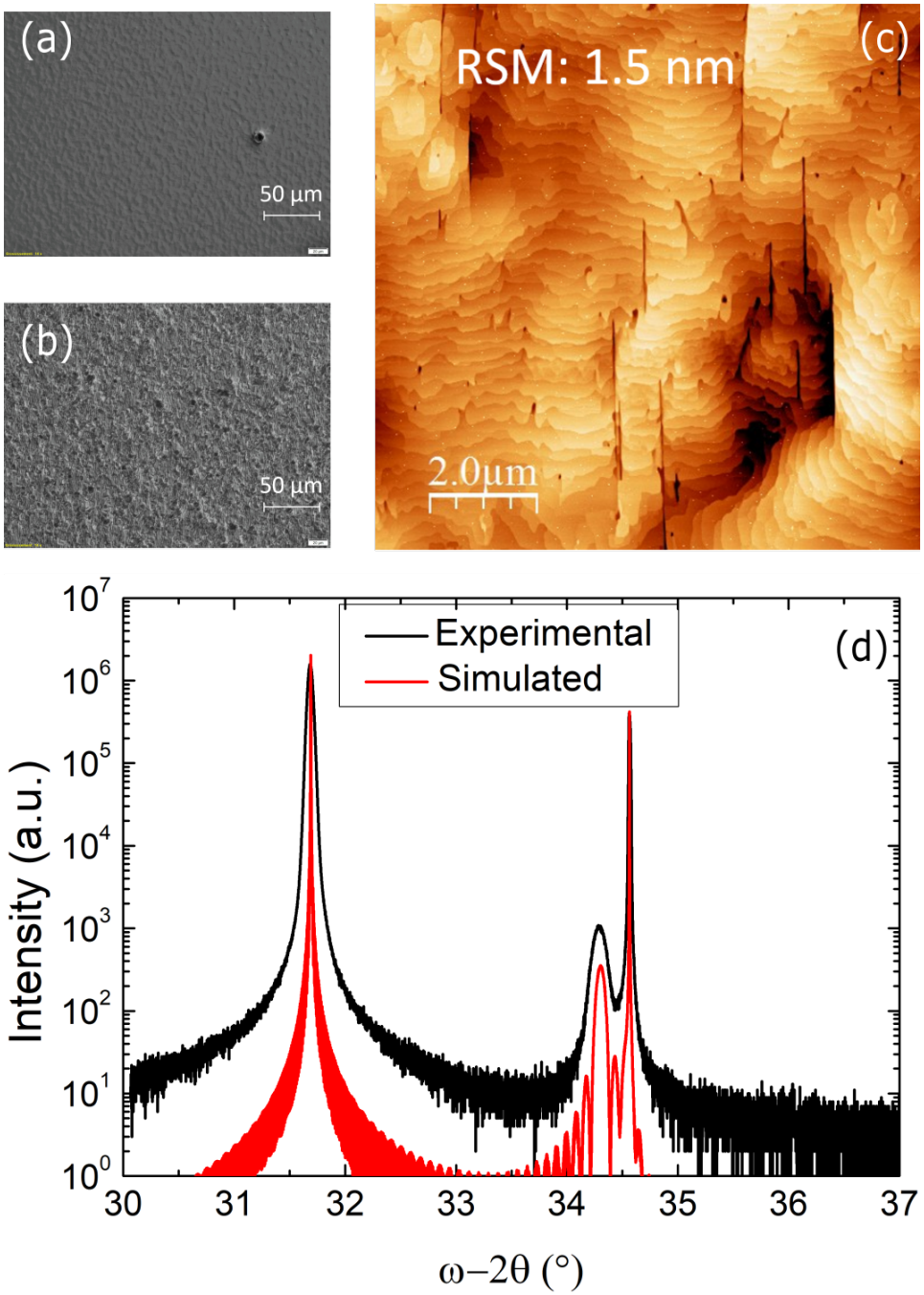


Figure 5.7: InP solar cell (sample I of chapter 3 like) grown onto NAsP template: morphology at (a) the centre and (b) at the edge of the sample; (c) AFM and (d) XRD experimental (black line) and simulated (red line) scans.

substrate, and the irregularities at the interface on the InP side which can

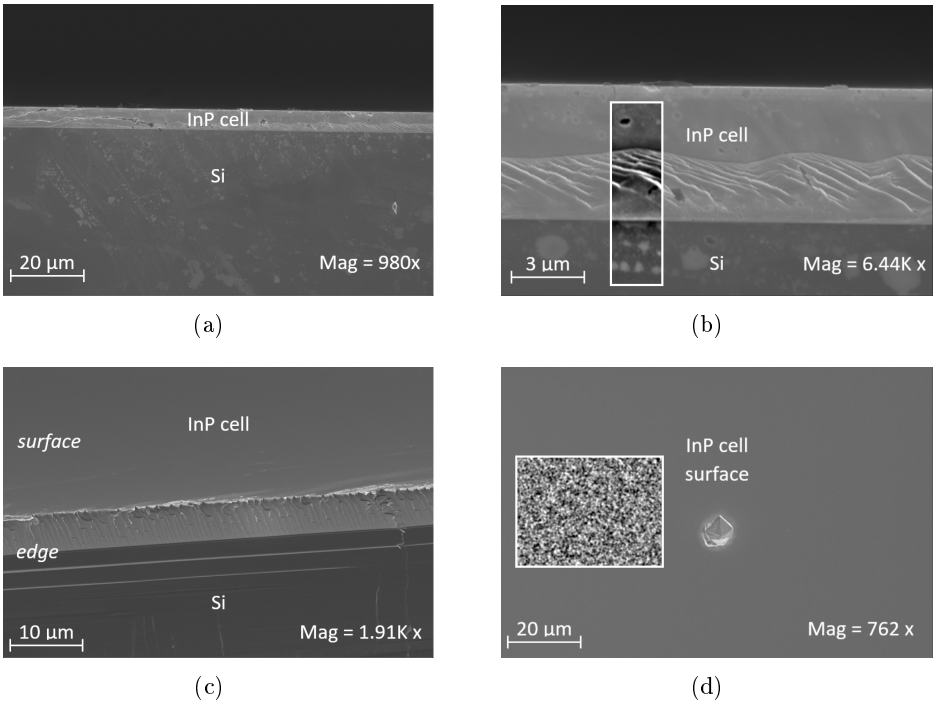
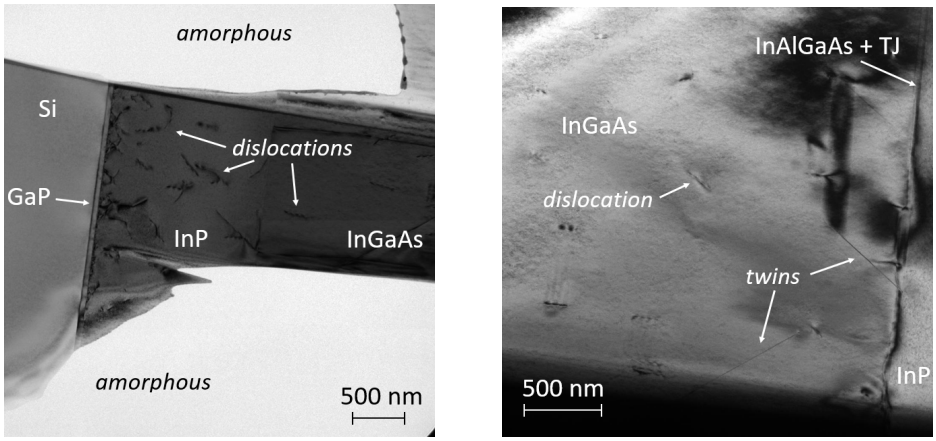


Figure 5.8: SEM images of the InP cell grown onto NAsP template: magnifications (a) 980× and (b) 6.44K× of the cross-section; (c) 1.91K× of the cross-section 35° tilted towards the surface and (d) 762× of the surface. Figures (b) and (d) present insets showing band-pass filter treatments performed with ImageJ software to highlight the effective roughness.

be noticed in (b) are probably due to cleaving. Figure 5.8(c) shows the cross-section 35° tilted towards the surface, where we can notice again the III-V/Si interface, whereas (d) presents the surface of the sample. Figure (b) and (d) present insets treated with a bandpass filter (ImageJ) to better reveal the irregularities, in particular, the filtered surface presents a similar shape than the one presented in Figure 5.7(a-b).

The preliminary characterizations presented no relevant issues due to the growth over the NAsP template.

In order to evaluate the effects of the mismatched substrate on the photovoltaic performances, we performed four different growths, integrating the four most promising devices onto the NAsP templates: the InP top cell with InP window (sample I), the InP top cell with AlInAs window (sample J), the InGaAs bottom cell (Table 3.7) and the tandem cell (Table 4.6), were separately grown. Each growth run was performed using a 3 cm square (to be processed) and a 1 cm square (for further characterizations) templates and a 2" InP substrate (as a reference).



(a) (b)

Figure 5.9: TEM images of the tandem cell grown on NAsP template for different magnifications: (a) reduction of dislocations density by increasing the deposition thickness; (b) defects in the InGaAs bottom cell.

Figure 5.9 presents some TEM images of the tandem device grown on NAsP substrate for different magnifications. Figure 5.9(a) presents a view of the first deposited layers (InP buffer + InGaAs base), as well as the template. In this figure, the dislocations arising from the mismatched structure are easily recognizable; nevertheless, we can also notice how the increase of the deposited thickness tends to reduce the total amount dislocations, as expected. Of course, the dislocations will have a deleterious effect on the photovoltaic performances of such devices; unfortunately, the TDD is hardly evaluable, because of the wide amorphous zones. Figure 5.9(b) presents a zoom of the InGaAs layers in correspondence of interface with the upper layers. It is possible to notice the presence of dislocations and twins. An electrical evaluation of the photovoltaic parameters in necessary to evaluate the effective influence of these defects.

5.5 A new processing

The high TDD, as well as other structural defects arising from III-V/Si growth, can act as recombination centres for the photogenerated carriers. In order to limit this influence on the carriers' collection, it is necessary to introduce an important change in device processing: the back contact has to be taken on the front side of the device, directly at the bottom of the mesas (InP:n+ buffer layer), as presented in Figure 5.10. By introducing a metallic grid between the various cells, the carriers can be ideally collected

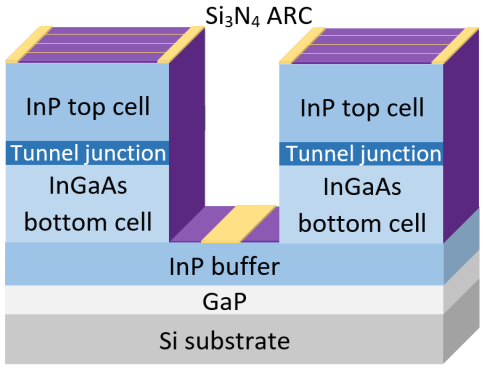


Figure 5.10: New back contact realization approach: since the contact can not be directly taken on the back of the Si substrate, it is deposited on the bottom of the mesas (on InP:n+ buffer), between each cell.

without influences from the template layers. In our case, we have placed the contact on the InP:n+ buffer layer, which makes the situation similar to the one on InP substrates: as the material and the doping level of the n-contact layer are the same, we can therefore realize the same metallic contact. Nevertheless, an interesting, alternative solution can be taken into account: by introducing an InGaAs:p++ layer and, subsequently, a second tunnel junction between the InP buffer and BSF, it is possible to switch the polarity of the contact from n to p, realizing therefore a double p-contact in the device (the principle is very similar to the one proposed in Figure 4.13 on page 123). The advantages of such a procedure can be a better quality of the contact (Pt/Au on p-InGaAs is known to be better than Ti/Pt/Au on n-InP) and, by properly modifying the sequence of the processing steps, the possibility of depositing both the front and the back contact in a single sequence, simplifying the process. Although very interesting, this possibility was not tested during this PhD.

5.5.1 The new photolithographic set

As mentioned in section 5.4, the III-V/Si solar cells to be processed were grown onto 3 cm squared templates. An optimal set of photolithographic masks should then be designed for this shape. Nevertheless, we decided to design a set optimized for typical 2" diameter circular substrates: the first reason was the possibility of keeping a part of the previous set (in particular, masks 1, 2 and 4), and the second reason was the fact that a processing for circular samples is preferable, since the squares may present more issues due to asymmetries.

As presented in Figure 5.11, the back contact metallization pattern was designed as a thin grid around every single cell. Every mesh is connected to

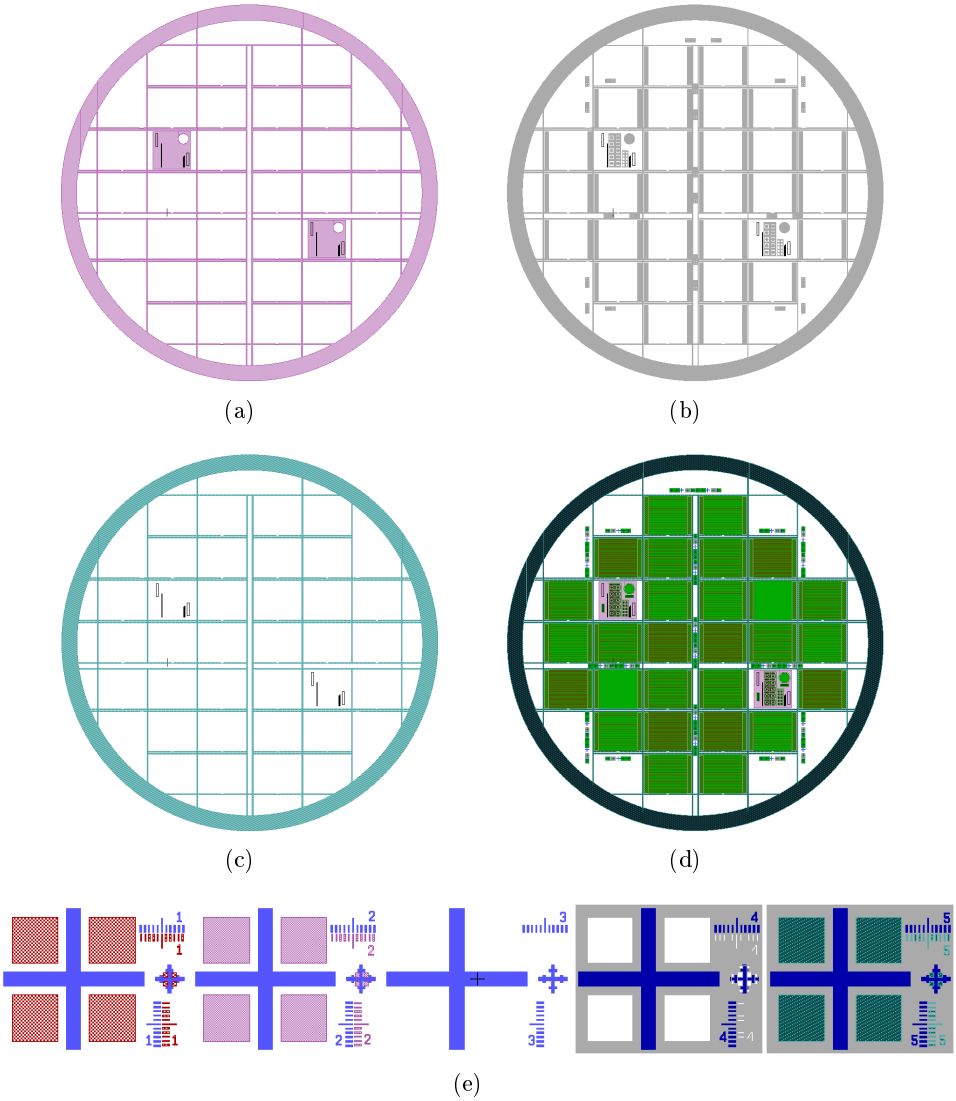


Figure 5.11: New photolithographic set for cells integrated onto Si substrates (masks 1, 2 and 3 were kept from the previous set). (a) Mask 4: InGaAs contact etching. The pink dotted zones represent the non-etched parts. (b) Mask 5: ARC opening. The grey zones represent the opened parts. (c) Mask 6 (new): back contact metallization. The turqouise lines represent the metallized zones. (d) The whole set. (e) Overlap of all the masks for the alignment pattern (the mesa mask was suppressed for a greater clarity).

a large ring surrounding all the cells along the substrate edge, from which the carriers can be collected with a probe during the measurement. As the reduced dimensions of our templates allowed us to align only the central part of each mask on the sample, the external ring was not included in our

processes. Nevertheless, the back contacts could even be taken on the thinner meshes around the cells.

This new design required us to modify some masks from the old set and to add the new grid structure in the pattern. The grid pattern had to be added to masks for InGaAs contact etching and ARC coating, which are presented in Figures 5.11(a) and (b), respectively. A new mask for the back contact realization was designed as well and is presented in Figure 5.11(c). By performing the back contact metallization after the ARC deposition, we guaranteed a greater protection of the cells sides from unintended metallic depositions: since the metallization has to be realized at the bottom of several μm deep trenches, a perfect coverage of the sides by the photoresist can not be a priori considered. Therefore, an intermediate dielectric layer can avoid eventual contacts between the sides and the metals.

Figure 5.11(d) represents the new, overall set, whereas (e) represents the new alignment patterns (without the mesa etching layer, for a greater clarity): mask 5 was slightly modified for a greater alignment convenience, whereas the previously free patterns were used to align the new mask.

5.5.2 The new process flow

Processing of solar cells integrated on NAsP templates required some cautions compared to that optimized for the cells grown on InP. The main difference is due to the fact that, in this case, mesa etching has to be stopped

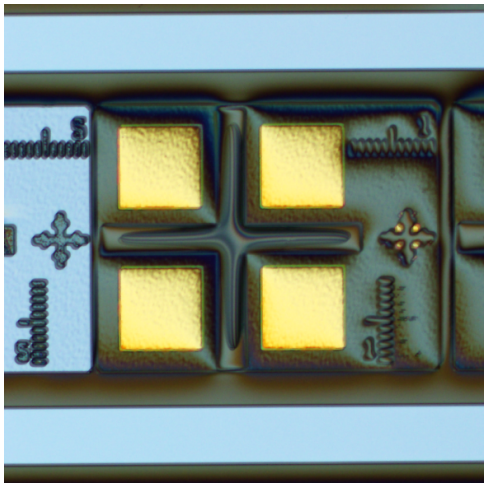


Figure 5.12: ARC opening in the mesa bottom of an InP cell on NAsP template. The light blue stripes correspond to the semiconductor surface (were the ARC was lifted away), whereas the grey zones correspond to the nitride. We can appreciate the mesa thickness from the convexity of Si_3N_4 in the central zone, compared to the zones close to the stripes.

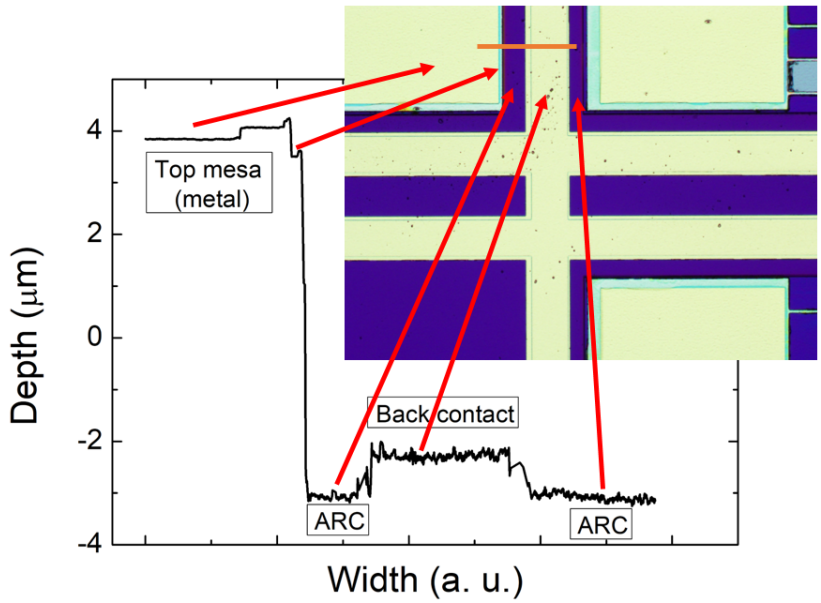
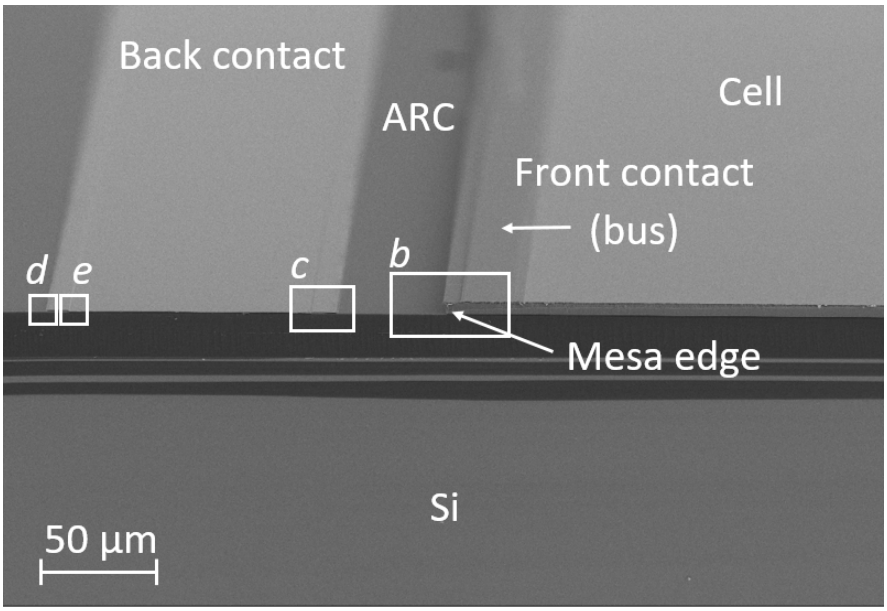


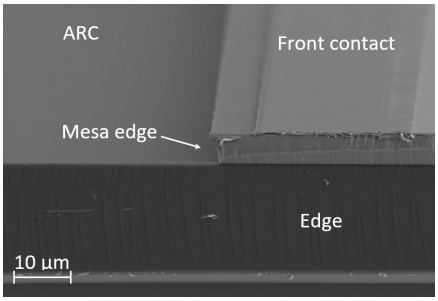
Figure 5.13: Profilometry scan of the metallized mesa bottom of the InGaAs cell. In the inset is an optical microscopy picture of the interest zone (the orange line marks the scanned zone). The correspondences between the various zones and the profile are highlighted. The width of each mesh is 100 μm.

at a very specific depth, namely the InP BSF of the bottom cell (which, from an electrical point of view, takes the role of the previous InP:n substrate). As a consequence, the HBr:H_2O_2:H_2O solution could not be used, as the etching rate was too high to guarantee an efficient control of the process. In the two InP cells, base and BSF are made with the same material: the use of a relatively slow etching solution for InP is therefore necessary to keep the etching depth under control. We then used the typical H_3PO_4:H_2O_2:H_2O (3:1:40) solution to etch the As-based layers, whereas the InP layers were etched by HCl:H_3PO_4 (1:3). This last choice was motivated by the good level of control on the InP etching rate and by the fact that preliminary tests demonstrated how the post-etching superficial roughness was considerably reduced. This fact is probably due to the use of a Si substrate, which considerably reduces the overall InP surface exposed to the solution: a much more localized reaction generates a lower amount of bubbles and, therefore, a reduced local masking effect.

A second issue was created by the necessity of processing the bottom of very thick mesas (Figure 5.12 presents an overview on the various thicknesses in correspondence of the alignment patterns after the opening of ARC): it was therefore necessary to use thick enough photoresists for the last two steps, notably a positive one for the ARC opening and a negative one for the back contact lift off, as well as their optimal bake, insolation and development



(a)



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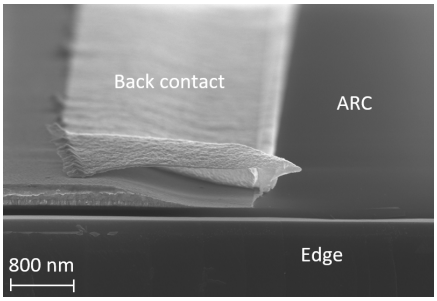

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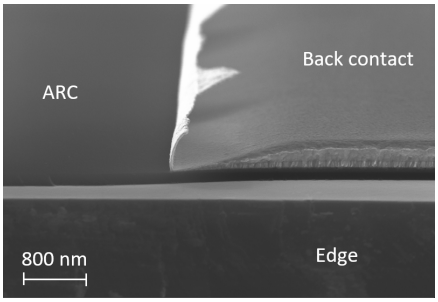
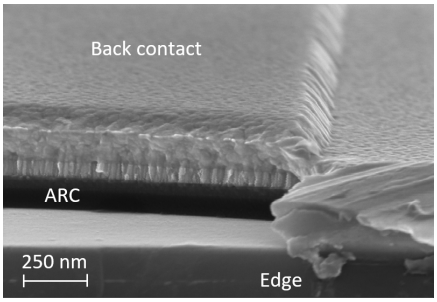


(d)



(e)

Figure 5.14: SEM images of bottom mesa processing of NAsP templates: (a) overview of top + bottom mesa; (b) zoom on mesa edge; (c-d) zoom on bottom contact; (e) high zoom on overlap of between back contact and ARC.

conditions.

Figure 5.13 presents a zoom on the final shape of the device (metallic grid around three cells). The various thicknesses were evaluated by a profilometry scan along the orange line. The presented scan shows the expected thicknesses and abrupt interfaces (demonstrating the validity of the chosen photoresists and processing conditions), as well as regular surfaces. The correspondences between the various zones and the measured thicknesses are indicated by the red arrows.

Figure 5.14 presents SEM scans at different magnifications of the cross-sections of a processed sample, tilted towards the surface. A general overview is presented in (a), from which we can identify the top (front contact metallic bus) and the bottom (back contact and ARC) of a cell mesa. Figure (b) presents a zoom on the border of the etched mesa, whereas (c) and (d) show the edges of the back contact. Finally, (e) presents the overlap of the more external slices of back contact on the underlying ARC (the grid of the back contact is slightly thicker than that of ARC opening to guarantee a full coverage of the exposed semiconductor). All the figures show abrupt interfaces and a general good quality of the process, therefore validating the proposed technology.

5.6 Photovoltaic performances

The distribution pattern of the cells in our photolithographic set made it possible to realize between 16 and 20 devices for each substrate (including the 2 EQE and the 2 TLM cells), depending on the optimal alignment of the masks, as presented in Figure 5.15. Unfortunately, all the cells close

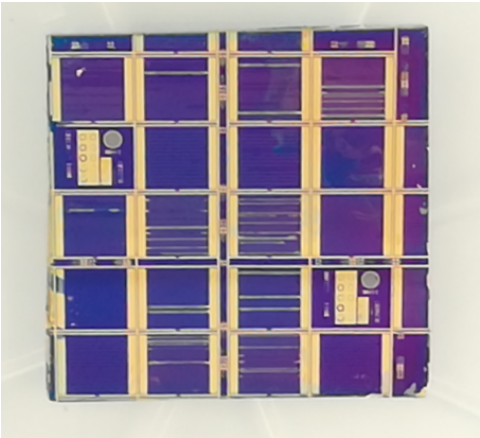


Figure 5.15: Processed InGaAs cells on NAsP template. Every sample can contain between 16 and 20 cells.

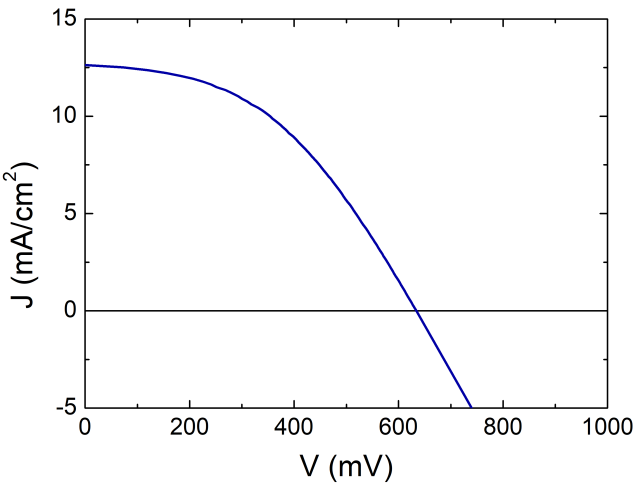


Figure 5.16: J-V characteristic under illumination of the best InP cell (AlInAs window) grown on NAsP template. The diode-like trend and the generated photocurrent make this device very promising for future developments.

	InP substrate	NAsP substrate
J_{SC} (mA/cm^2)	20.6	12.1
V_{OC} (mV)	809.3	634.0
FF (%)	81.4	46.4
η (%)	13.53	3.55

Table 5.3: Photovoltaic parameters of the best InP cell (AlInAs window) grown on NAsP template, compared with the same cell grown on InP substrate.

to the edges of the samples must be disregarded. This was due to both improper lithographies (the resist is irregularly spread in the edges) and tweezers gripping. In conclusion, around six cells per sample could be considered effectively reliable.

Despite the first measures on the InP cell with InP window layer being characterized by a low R_{sh} and presented therefore a linear trend which prevented the evaluation of the limiting factors, the second InP cell (AlInAs window) presented much more interesting results, as presented by Figure 5.16. Compared to the previous sample, the generated photocurrent is more intense, although lower than the one of the same structure grown on InP (J_{SC} decreased from 20.6 to 12.1 mA/cm^2, as presented in Table 5.3). In this device, a diode-like trend can be identified, although characterized by a high R_s, which reduces FF from 81.4 to 46.4%. Nevertheless, the curve

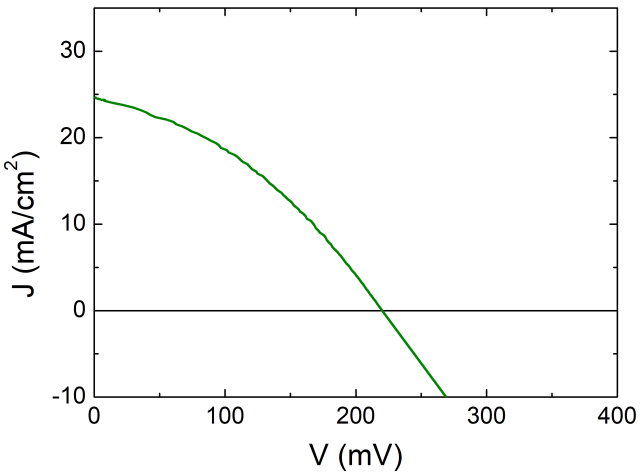


Figure 5.17: J-V characteristic under illumination of the best InGaAs cell grown on NAsP template. As for the previous result, the diode-like trend and the generated photocurrent make this device very promising for future developments.

	InP substrate	NAsP substrate
J_{SC} (mA/cm^2)	41.2	24.7
V_{OC} (mV)	369.9	220.2
FF (%)	74.5	36.9
η (%)	11.38	2.00

Table 5.4: Photovoltaic parameters of the best InGaAs cell grown on NAsP template, compared with the same cell grown on InP substrate.

undoubtedly presents a solar cell behaviour (with a 3.55% efficiency, against an original 13.53% obtained on an InP substrate), which demonstrates the validity of the proposed principle.

The potential of the proposed procedure was confirmed by the results obtained on the InGaAs bottom cell, presented in Figure 5.17 and Table 5.4. Even in this case, some of the cells presented an effective photovoltaic behaviour: despite FF being lower than in the previous sample (36.9%), the diode-like trend is always evident, whereas J_{SC} jumps to 24.7 mA/cm^2 (on the InP substrate this was 41.2 mA/cm^2). The measured V_{OC} was 220.2 mV (369.9 mV), whereas the total efficiency was 2.00% (11.38%). As in the previous case, the inhomogeneity of the results and the linear characteristic of some devices seem to suggest a processing limit.

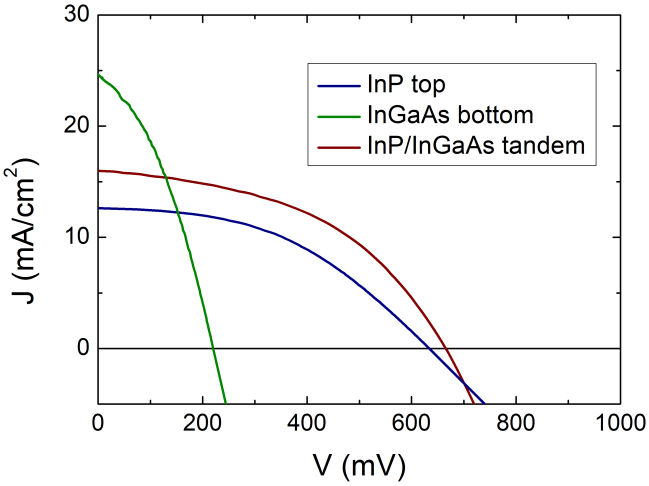


Figure 5.18: J-V characteristic under illumination of the best tandem cell grown on NAsP template (red line), compared to the single J-V characteristics of InP top (blue line) and InGaAs bottom cells (green line). Even in this case, a diode-like trend a relevant photocurrent generated make this device very promising for future developments.

	InP substrate	NAsP substrate
J_{SC} (mA/cm^2)	20.8	16.0
V_{OC} (mV)	1045.9	669.9
FF (%)	83.9	46.2
η (%)	18.27	4.95

Table 5.5: Photovoltaic parameters of the best tandem cell grown on NAsP template, compared with the same cell grown on InP substrate.

Finally, Figure 5.18 presents the J-V characteristic of the best tandem cell obtained on NAsP template, whereas Table 5.5 compares the photovoltaic parameters with those obtained on an InP substrate. The results are in line with the previous ones: the cells at the centre of the sample present a relevant photocurrent (J_{SC} of 16.0 mA/cm^2) and a diode-like trend similar to the InP/Si cell (FF of 46.2%). The measured V_{OC} is 669.9 mV, whereas the conversion efficiency is 4.95%. By comparing the total J-V curve (red line) with those of InP (blue line) and InGaAs (green line), it is hard to evaluate the influences of the single cells: the overall V_{OC} is only slightly higher than that of the InP alone, whereas the overall J_{SC} is not totally limited by the lower one of InP. This last fact may be explained by a random factor during the processing of InP and tandem cells or by a lower influence of the Si substrate on the upper cell when an intermediate bottom cell is added.

Variation	InP top	InGaAs bottom	Tandem
J_{SC}	-40%	-41%	-23%
V_{OC}	-22%	-40%	-36%
J_S	$\sim$+1000%	$\sim$+1000%	$\sim$+1000%

Table 5.6: Effects of the switch from an InP substrate to a NAsP template on the photovoltaic parameters.

The limitations introduced by the Si substrate on V_{OC} probably reduce the additivity principle.

By comparing the two single devices, we can notice how the Si integration had a very similar impact on J_{SC} (which was decreased by 40% in the InP cell and by 41% in the InGaAs one), whereas the V_{OC} behaviour was less similar (it decreased by 22% in InP and 40% in InGaAs). The effect on the tandem cell J_{SC} was less relevant (reduction of 23%), whereas its V_{OC} was decreased by 36%. As mentioned before, the lower reduction of the tandem J_{SC} may be due to a lower effect of the different lattice parameter of the substrate on the top device (because of the intermediate InGaAs cell): the InP cell is maybe less influenced and then its current is higher; but still lower than that produced by the bottom InGaAs (which is probably limited like in the single cell case). Therefore, the overall J_{SC} is still limited by the top cell, but higher than for InP alone.

The effects of the Si substrate on the various V_{OC} are less evident. We can anyhow remember the relation between V_{OC} and J_S: for all the three cells, the switch to the NAsP template leads to an increase of J_S of an order of magnitude. As the InP cell was characterized by a lower J_S, also the related V_{OC} will be less affected.

The decreases in FF (-43%, -50% and -45%, respectively) should not present any particular correlation, as they are mainly affected by R_s. As a consequence, neither a correlation between the efficiencies' decreases can be evaluated.

It has already been reported in literature that III-V solar cells can be integrated onto Si substrates without relevant decreases in J_{SC} and V_{OC} [16–18]. The main limitations due to the lattice mismatched substrate then affect FF (higher R_s and lower R_{sh}). This is true for both epitaxial and wafer bonding approaches. It is therefore necessary, for our purposes, to reduce such limitations. On the other hand, it demonstrates that our devices can be sensitively improved.

The effects of the switch from an InP substrate to the NAsP template on J_{SC}, V_{OC} and J_S are summarized in Table 5.6.

We can identify two possible explanations for the discrepancy between

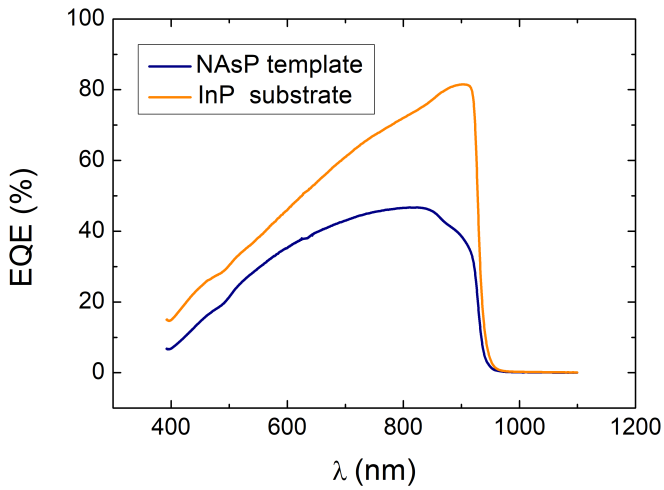


Figure 5.19: EQE characteristic of the best InP solar cell grown on NAsP template (blue line), compared to the same result obtained on a typical InP substrate (orange line).

the photovoltaic parameters of the cells grown on InP and on NAsP template: the first one is connected to the presence of defects, arising from the lattice mismatch, which can act as traps and recombination centres. This is in line with what determined by TEM. The second possibility is an inefficient collection of the carriers, especially at the back contact level. This possibility was partly explored by performing a TLM measurement of the n-type contact directly taken on the InP buffer. We determined a contact resistivity of $\sim 5\times10^{-7}\,\Omega\cdot\mathrm{cm}^2$, around half of the value obtained for the front p-type contact. This value is optimal for our purposes; unfortunately, this does not prevent us from totally excluding a limit arising from this zone. The carriers directed to this contact have to cover on average a larger path than those directed to the p-type contact, as well as than those collected by the n-type contact of the InP substrate. We should then take into account an overall, less efficient n-type contact.

Anyhow, both possible limitations can be overcome in future, and this demonstrates therefore the feasability of the proposed process.

Figure 5.19 presents the EQE characteristic of the best InP solar cell grown on NAsP template (blue line), compared with the best result obtained for the same device grown on InP (orange line). It was not possible to characterize the InGaAs and the tandem cells grown on NAsP template since we were not equipped with a Ge calibration diode for the longer wavelengths at the moment of the measurement. However, the result obtained with the InP cell is already relevant, as it presents a general reduction of

carriers collection compared to the device obtained on InP. The possible explanations coincide with those already presented.

5.7 Conclusions

In this chapter, we have presented three different approaches for the integration of the previously presented solar cells on Si substrates. By performing a series of preliminary material characterizations, we identified the NAsP commercial template (GaP nucleation over Si and following InP growth) as the best possibility for such an integration. A preliminary InP cell was then grown on the selected template. The various material characterizations performed demonstrated the success of the growth. A new processing procedure was developed to extend the previous methodology to the new structures. Then, all the best cells previously measured were realized on the new substrate and characterized. Very interesting results were obtained on the InP cell with AlInAs window layer and the InGaAs device: the new devices presented photocurrents corresponding to around the 60% of what was measured on InP substrates. This value increased to 77% for the tandem cell. Even more importantly, these devices presented a diode-like trend, thus demonstrating the effective possibility of realizing efficient devices on Si substrates. Auxiliary tests such as dark J-V, TLM and EQE measurements to start to quantify the effects of the Si substrate on the photovoltaic parameters, as well as to identify the most limiting factors.In general, literature presented examples of III-V solar cells integrated onto Si by both direct epitaxy and wafer bonding without relevant influences on J_{SC} and V_{OC}. Moreover, encouraging results with an approach similar to our [19], where a GaAs cell was integrated on Si via a SiGe buffer layer with only a 10% reduction of the overall efficiency, has already been obtained. We can therefore expect that our structure may significantly increase its overall performances. It is then necessary to reduce the total amount of defects in the structure and implement rear collection of carriers to make this new generation of solar cells competitive with the typical growth over InP substrates.

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General conclusions and perspectives

The use of III-V semiconductors is nowadays the most promising possibility for the realization of high efficiency, multi-junction solar cells able to overcome the theoretical efficiency limit of single junction devices. Furthermore, the use of cheap Si substrates offers an interesting solution to reduce the costs of this expensive technology, making it more attractive for future industrialization.

In this manuscript, we presented the realization of a promising InP/InGaAs tandem solar cell lattice matched to InP and we demonstrated the feasibility of its integration on a commercial Si template through MOVPE growth.

Summary

We first studied the epitaxy and the processing of an InP single junction device realized on an InP substrate. This study allowed us to export and adapt the expertise of III-V Lab in MOVPE growth and processing of photonics and optoelectronics devices to a completely new field such as photovoltaics. We studied the growth conditions of these cells at typical MOVPE temperatures (600-700 °C range) in both a horizontal and a vertical, industrial reactor and calibrated the optimal thicknesses and doping levels for the constituting layers. We determined the importance of a relatively thick emitter (150 nm) in obtaining competitive values of V_{OC} and showed how the consequential decrease in J_{SC} can be limited by appropriately setting the base doping level (which was fixed at -1×10^{17} cm^{-3}). We also correlated the increase of BSF thickness to a better adsorption of longer wavelength photons. The processing of these devices required the design of a set of photolithographic masks, which were optimized for 2" substrates. We confirmed by TLM and CTLM measurements that both sputtering and plasma evaporation techniques are appropriate for the deposition of metallic contacts for our devices, as the determined contact resistivity ρ_c is around $10^{-6}\,\Omega\cdot\text{cm}^2$ in

both cases. We determined that chemical wet etching of mesas is more appropriate than physical dry etching, as the latter has a strong impact on the dark saturation current, and therefore V_{OC}, of the devices. In particular, we demonstrated that $HBr:H_2O_2:H_2O$ is the best solution for mesa etching. We identified PECVD deposited Si_3N_4 as both a promising ARC and passivating layer and demonstrated its benefitial effect on the photovoltaic performances of the devices. The developed and optimized manufacturing process allowed us to realize 12.9% efficiency solar cells. The quality of the structure was demonstrated by the high 84.3% FF. The quality of the proposed process was demonstrated by the homogeneity of results across the whole wafer. We also demonstrated that the substitution of the InP window layer with a higher bandgap, lattice matched AlInAs layer can increase J_{SC} and therefore efficiency to 13.5% (despite FF is slightly reduced to 81.4%). The developed manufacturing process was completely generic and extendible to the realization of both InGAs and tandem solar cells.

Following the same procedure as the previous study, we have also realized InGaAs solar cells presenting a FF of 74.5% and a conversion efficiency of 11.4%. This result corresponds to the state of the art for a p/n polarity and is close to the simulated theoretical limit of 12.1% for this kind of technology.

The integration of the realized cells in a tandem device required the development of an intermediate tunnel junction. This was one of the most challenging point of this work, as until now only CBE and MBE demonstrated sufficiently efficient devices lattice matched to InP. We proposed a structure where the anode was made with AlInAs:C, whereas the cathode was InP:S. The advantages of this structure are a type-II band alignment at junction, which is a favourable condition for the carriers tunnelling, and a total transparency to the incoming light compared to the bottom cell. This structure required the achievement of very high doping levels for both sides of the junction. The extremely high etchant effect of C precursor (CBr_4) on AlInAs required to decrease the growth temperature to 540 °C (which also allowed us to increase the dopant incorporation). By performing a wide study on the various interactions between TMAl, AsH_3 and CBr_4, we finally obtained a doping level of $+4\times10^{19}\,cm^{-3}$. By combining this layer with an equivalently doped cathode, we obtained a tunnel junction characterized by a J_p of $1022\,A/cm^2$ and a r_l of $5.8\times10^{-5}\,\Omega\cdot cm^2$, able to work under high solar concentration conditions with only a few mV voltage drop introduction. The same structure, exported in the vertical reactor, reached a J_p of $1571\,A/cm^2$ and a r_l of $1.7\times10^{-4}\,\Omega\cdot cm^2$. By performing a series of material characterizations such as HAADF-STEM on the whole structure, we demonstrated the high quality of the low temperature deposition. Our results establish the state of the art.

The InP top cell, the tunnel junction and the InGaAs bottom cell were then combined in a tandem device. Minor changes to some thicknesses were performed to optimize the new structure. The obtained device presented a FF of 83.9%, demonstrating the quality of materials, and an efficiency of 18.3%. It was possible to distinguish the contributions of the two single junction cells from the total V_{OC} and J_{SC}. This promising result makes the proposed structure an interesting alternative to more typical tandem structures made on GaAs.

In order to study the integration of the developed devices onto Si, we investigated different templates, supplied by different partners. By performing material characterizations such as XRD and AFM on these templates before and after a 700 °C annealing (simulating the growth conditions during epitaxy regrowth), we identified an InP/GaP/Si template supplied by NAsP company as the best option for our studies. Such a template presented a 100% relaxed InP structure (not influenced by the annealing) and a 1.9 nm RMS (increased to 3.0 nm by the annealing). A preliminary growth of an InP cell on this template, followed by several characterizations, demonstrated the quality of the growth (the crystalline structure is not affected by the deposition, whereas RMS decreases to 1.5 nm) and the potential of this approach. TEM, EDX and HAADF-STEM analysis confirmed the potential of such a template for our purpose. We then integrated the most efficient structures obtained on the chosen template. The processing of these new structures required some very important changes such as the deposition of the back contact on the front face of the sample (in order to exclude the Si layer from the electrical circuit), which required an upgrading of the previous photolithographic set. The InP top cell with AlInAs window, the InGaAs bottom cell and the tandem device presented very promising results: these devices, although not reaching the same quality of the previous devices, presented a relevant photocurrent and a diode-like trend, which demonstrated the possibility of integrating this type of solar cells onto Si. We individuated a J_{SC} reduction of around 40% when moving from an InP substrate to a Si one. The tandem device is less affected, since the top cell photocurrent is less influenced by the substrate. We also individuated a J_s increase of around one order of magnitude when moving to Si; which have different effects on the various cells. The cells presented FFs of 46.4%, 36.9% and 46.2% and efficiencies of 3.6%, 2.0% and 5.0%, respectively. The reasons for this decrease may be connected to an increasing amount of defects in the structure, which can act as traps and recombination centres, or to a non optimal carriers collection on the back contact. This second reasons is connected to the little extension of the contact, compared to a full plate contact typical with InP substrates. In fact, we determined a contact resistivity of $5\times10^{-7}\,\Omega\cdot cm^2$; which demonstrates the quality of the metal/semiconductor contact. However, both the amount of defects and the unoptimized contact

can be overcome by further studies. Our devices still present some limits compared to III-V/Si solar cells presented in literature. Nevertheless, our first samples present a high potential for future improvements and applications, validating the proposed technology.

Perspectives

The two main aspects of this work were the development of a multi-junction device based on the InP technology and the integration of the same device on Si.

While the InGaAs bottom cell does not present particular challenges, the other components of the tandem cell can undoubtedly be improved. As we saw, the main limiting factor in our InP cells is J_{SC}, which seems to be limited by the reduced thickness of the base. From a technological point of view, implementations of both electrical passivation and ARC realization (which, in our case, are obtained through the same dielectric deposition) can increase the overall performances. As the high FF obtained is a proof of the high quality of our structures, we can therefore conclude that, overcoming the two problems mentioned, it will be possible to reach a new state of the art for InP single junction devices. This is also true for the tandem device. Furthermore, for this last device, a systematic study on the thickness of the top cell base (which is not necessary the right one for the single junction) should allow us to match the currents of the two devices, perceptibly increasing the overall efficiency.

The tunnel junction performances can be implemented as well. Since the n-doping of InP is already known to overcome the order of $10^{20}\,\mathrm{cm}^{-3}$, a deeper comprehension of the reaction resulting in the highly doped AlInAs:C growth may allow us to obtain the same order of magnitude for the doping and, therefore, much more efficient devices. This is very important as tunnel junctions have many applications also beyond the typical photovoltaic applications.

More generally, the InP photovoltaic technology may be implemented in several ways: an AlInAs top cell can be used instead of the InP top cell, as its slightly higher bandgap ensures a better coverage of the solar spectrum. A third, intermediate InGaAsP or AlInGaAs cell can also be introduced to increase the overall collection. The same AlInAs/InGaAsP/InGaAs structure can then be realized on a slightly different lattice parameter (5.807 Å), and the obtained structure is expected to overcome the limit of 50% under 100 suns illumination.

Finally, the integration on the InP/GaP/Si template presents different implementations which can be studied in the coming years. The quality of the growth on Si can surely be increased, with the aim of reducing the typical III-V/Si integration issues (in particular, trading dislocations). For a sufficiently low TDD, the Si substrate can be then included in the electrical circuit of the cell without relevant limitations. As a consequence, the back contact will be realized in a more correct and more efficient way, thus increasing the overall performances. As this is not possible yet, the implementation of the back contact on the front side is necessary for the same purpose.

To conclude, the proposed approach can be tested for other, more conventional technologies such as GaAs. A successful result may open the door to a new generation of both more efficient and more cost-effective photovoltaic devices.

Appendix A

Résumé substantiel en français

L'objectif de cette thèse était de développer des dispositifs photovoltaïques à double jonction accordées sur InP et intégrés sur des substrats Si. Toutes les étapes de la production de ces dispositifs ont été réalisées personnellement par l'auteur de ce manuscrit: épitaxie (MOVPE), caractérisation des matériaux, développement technologique et caractérisation électro-optique. Dans les cinq chapitres qui composent ce manuscrit, la présentation de ces étapes technologiques, ainsi qu'une présentation générale des motivations de ce travail et une conclusion générale, sont données intégralement.

Le premier chapitre était consacré à une introduction générale au problème. Dans un premier temps, un aperçu général des dispositifs photovoltaïques à jonction unique a été présenté: présentation des principaux paramètres électriques, efficacité quantique, réponse spectrale. En particulier, nous nous sommes concentrés sur la présentation de la limite de performance de ce type de dispositif, définie comme la limite Shockley-Queisser. Nous avons montré que cette limite est d'environ 30%, en fonction du bandgap E_g du semi-conducteur utilisé. Cela vient du fait que, fixé E_g, les photons trop énergetiques seront absorbés, mais les électrons produits seront partiellement perdus par thermalisation; tandis que ceux qui sont trop peu énergetiques ne seront pas absorbés.

D'où l'intérêt d'un appareil multijonction, qui permet ainsi de mieux couvrir le spectre solaire incident. Nous avons donc redéfini les principaux paramètres photovoltaïques dans le cas d'une multijonction et introduit le concept de matching de courant. Nous avons montré comment, dans le cas d'une multi-jonction, le choix des bandgaps des différents semi-conducteurs est important pour maximiser l'efficacité (en fonction du nombre de jonctions utilisées et du type de spectre incident considéré). A partir de là, nous avons démontré le grand intérêt des matériaux III-V pour les applications photovoltaïques : grâce à leur *bandgap engineering*, typique de ces matéri-

aux, il est possible d'avoir accès à une vaste série de paramètres de maille et de bandgaps, à travers la réalisation de structures ternaire et quaternaire. Nous avons également montré comment, actuellement, tous les principaux records photovoltaïques ont été réalisés à l'aide de la technologie GaAs, parfois combinée à la technologie InP pour avoir accès aux longueurs d'onde les plus élevées.

Nous avons donc montré comment le coût élevé des matériaux III-V rend nécessaire le développement de méthodologies pour réduire les coûts totaux. En plus de travailler sous une forte concentration solaire, une bonne alternative est d'utiliser des substrats moins chers, notamment à base de Si. Selon le cas, le silicium peut également être utilisé comme cellule bottom. Nous avons présenté les deux principales approches de l'intégration III-V/Si et leurs principales difficultés: la croissance épitaxiale, qui nécessite de faire face à un désaccord de maile élevé, ainsi qu'à un désaccord thermique et à la présence d'une interface polaire et non polaire; et l'approche non épitaxiale (collage ou empilément méchanique), qui nécessite l'utilisation des substrats III-V et donc un développement technologique plus complexe et coûteux pour récupérer ces substrats, ainsi que de limiter la dimension des dispositifs réalisés. En termes d'efficacité, la croissance épitaxiale a permis de réaliser des dispoditifs avec presque un 20% d'efficacité, tandis que l'empilémente mécanique a permis de dépasser le 35%.

Enfin, nous avons présenté notre approche: nous avons décidé d'utiliser une approche épitaxiale, attirés par sa simplicité d'intégration industrielle, et de réaliser des dispositifs sur le paramètre de maille de l'InP, attirés par la possibilité d'utiliser des semi-conducteurs à petits bandgaps. De cette façon, nous avons pu limiter l'utilisation de Si à un simple substrat économique, ce qui nous a permis de nous concentrer sur la réalisation de cellules photovoltaïques entièrement avec des matériaux III-V. De plus, le paramètre réticulaire de l'InP est très proche de celui qui permet une couverture optimale du spectre solaire avec une structure ternaire parfaitement accordée; ce qui peut donc représenter un développement futur de notre travail.

Le deuxième chapitre a été consacré à la présentation de l'appareil expérimental MOVPE pour la croissance épitaxiale des échantillons présentés, ainsi qu'à certaines des principales techniques de caractérisation des matériaux utilisés.

La croissance MOVPE a été présentée en détail: principe de fonctionnement, structure du réacteur, les deux principales configurations utilisées (réacteur horizontal AIX 200/4 et verticale Close Coupled Showerhead), précurseurs utilisés. En outre, certains des aspects les plus importants de la croissance MOVPE ont été introduits: rapport V/III, loi de Vegard, contrôle du débit et interfaces As/P.

Parmi les différentes techniques de caractérisation utilisées, un grand espace a été consacré à la diffraction des rayons X. Nous avons montré comment

ce type de mesure permet de déterminer des caractéristiques importantes telles que l'épaisseur, la composition et le relâchement des couches épitaxiales déposées et nous avons présenté l'appareil expérimental utilisé. Nous avons également présenté la technique de profilométrie électrochimique C-V, nécessaire pour déterminer le niveau de dopage des différentes couches, et d'autres techniques de caractérisation telles que SIMS, TEM, SEM et AFM.

Le troisième chapitre a été consacré à la présentation, au développement et à l'optimisation des deux cellules à simple jonction qui constituent le tandem que nous voulons réaliser: la cellule top en InP et la cellule bottom en InGaAs. Le choix de cette paire est motivé par le désir de créer un véhicule test pour démontrer la validité de l'approche proposée. Ces matériaux nous ont permis de développer une filière photovoltaïque sur InP face aux principales difficultés liées à cette approche. Par la suite, ces matériaux pouraient être rapidement remplacés par des structures ternaires ou quaternaires plus complexes, capables d'optimiser la couverture du spectre solaire incident. Nous avons choisi de présenter en détail le développement de la cellule InP; puis de présenter les meilleurs résultats obtenus pour la cellule InGaAs.

Tout d'abord, nous avons présenté un aperçu de l'état de l'art des cellules InP. Nous avons vu comment le record actuel présente une J_{SC} de $31.2\,\mathrm{mA/cm^2}$, un V_{OC} de 939.0 mV, un FF de 82.6% et une efficacité de 24.2%. Nous avons ensuite présenté notre structure et indiqué les principaux paramètres qui ont été optimisés: épaisseurs de BSF, émetteur, couch fenêtre et couche de contact; dopage de la base et matériau de la fenêtre (InP ou AlInAs). Nous avons présenté l'optimisation des conditions de croissance des différentes couches qui composent la cellule totale et la caractérisation des croissances obtenues, démontrant ainsi la bonne qualité cristalline des échantillons et une densité de dopage homogène et adéquate. Nous avons ensuite présenté le développement technologique des différents échantillons. Nous avons présenté le jeu de masque initialement utilisé et fourni par un projet précédent. Nous avons donc mis en évidence ses limites et défini notre propre jeu de masques, composé de cinq niveaux et optimisé pour nos échantillons. Les masques ont permis de produire 26 cellules par échantillon, plus 2 cellules pour mesurer l'efficacité quantique et 2 pour évaluer la qualité des contacts métalliques par des mesures TLM. Nous avons présenté les principales étapes de ce processus: gravure des croix d'alignement, métallisation face avant, gravure mesa, gravure de la couche de contact, dépôt ARC et métallisation face arrière. Nous avons ensuite présenté les conditions expérimentales de mesure.

Une série d'études a permis d'optimiser les différents paramètres des cellules mentionnées ci-dessus, ainsi que le développement technologique des cellules. Les deux métallisations ont été optimisées par sputtering; le contact de type p a été réalisé en Pt/Au et de le contact de type n en Ti/Pt/Au. Le recuit du contact de type p a été effectué dans un four RTA à 400°C pendant

une minute. Nous avons montré que la gravure chimique est préférable à la gravure sèche. En particulier, nous avons identifié la solution HBr:H_20_2:H_2O (15:1:15) comme la meilleure alternative en termes de forme de flancs et de performances. Nous avons développé une solution de H_3PO_4:H_2O_2:H_2O (3:1:40) pour la gravure des couches de contact. Nous avons également utilisé une couche de Si_3N_4 déposée pour PECVD comme ARC et couche de passivation pour l'InP. L'épaisseur du BSF a été optimisée à 700 nm, celle de l'émetteur à 150 nm, celle de la fenêtre à 25 nm et celle de la couche de contact à 250 nm. Le dopage de base a été augmenté à -1×10^{17} cm−3. Bons résultats en termes de performances ont été obtenus avec une fenêtre en InP (J_{SC} de 18.9 mA/cm^2, V_{OC} de 809.3,mV, FF de 84.3% et efficacité de 12.9%) et surtout avec une fenêtre en AlInAs (J_{SC} de 20.6 mA/cm^2, V_{OC} de 809.3,mV, FF de 81.4% et efficacité de 13.5%).

En comparant ces résultats avec l'état de l'art, nous avons pu constater que la différence en termes de performances était due à un J_{SC} plus faible, liée à l'épaisseur réduite de notre base (mais nécessaire en vue d'une future intégration dans une tandem sur Si) et à un V_{OC} plus faible (lié à une passivation non optimale de l'InP). Le FF élevé démontre la bonne qualité des cellules fabriquées.

Une étude similaire a permis de produire des cellules bottom en InGaAs caractérisées par une J_{SC} de 41.3 mA/cm^2, un V_{OC} de 369.9 mV, un FF de 74.5% et une efficacité de 11.4%. Il s'agit d'un résultat d'excellente qualité, qui correspond actuellement au nouvel état de l'art pour ce type de technologie.

Le quatrième chapitre était consacré à la réalisation d'une jonction tunnel et à sa combinaison avec les cellules présentées dans le chapitre précédent dans une cellule tandem. Tout d'abord, nous avons présenté une vue d'ensemble de la physique et de l'état de l'art de ce type de dispositif pour la technologie InP. Ce record consiste dans une jonction InP/InP caractérisée par un J_P d'environ 1600 A/cm^2. Nous avons démontré qu'une grande transparence et un dopage élevé sont essentiels pour obtenir un dispositif de haute performance. Nous avons donc justifié le choix d'une couche AlInAs:C comme anode et d'une couche InP:S comme cathode pour le dispositif.

Nous avons présenté le défi technologique d'obtenir un dopage élevé de type p pour l'AlInAs par le précurseur CBr_4; à cause de ses interactions avec la phase solide de l'In et la phase vapeur du précurseur de l'Al. Nous avons ensuite montré les conditions d'obtention d'une couche fortement dopée (+4e10^{19} cm−3) et accordée sur InP. Nous avons combiné cette anode avec une couche InP:S également dopée et placé la jonction dans une structure plus complexe pour faciliter l'évaluation de ses propriétés électriques. Nous avons présenté une série de caractérisations matériaux (XRD, ECV, SIMS, TEM) pour démontrer leur qualité. Nous avons ensuite évalué les performances électriques, obtenant un résultat conforme à l'état de l'art et encore

plus adapté aux applications photovoltaïques grâce à une plus grande transparence des matériaux. Le dispositif présenté peut également être utilisé pour des applications photovoltaïques à forte concentration solaire.

Enfin, nous avons réalisé et présenté une cellule tandem InP/InGaAs grâce à la jonction tunnel présentée. Nous avons présenté et justifié les variations mineures des deux structures à simple jonction lorsqu'elles sont combinées en une double jonction. Enfin, nous avons présenté la caractérisation de la tandem réalisée: en mesurant uune J_{SC} de 20.8 mA/cm^2, un V_{OC} de 1045.9 mV, un FF de 83.9% et une efficacité de 18.3%, nous avons établi un nouvel état de l'art pour ce type de cellule solaire. La caractéristique EQE de la même cellule a permis de démontrer l'excellente couverture du spectre solaire incident, bien que la cellule bottom présentait une réflectivité plus élevée que si elle était utilisée toute seule.

Le cinquième chapitre était consacré à l'intégration des cellules précédemment présentées sur des substrats Si. Nous avons d'abord présenté quatre templates possibles pour l'intégration InP/Si, qui présentaient des buffers intermédiaires différents: deux avec des matériaux III-Sb (fournis par l'IES de Montpellier), un en GaP (fourni par NAsP) et un en GaAs (fourni par le LTM de Grenoble). Grâce à une série de caractérisations, nous avons identifié le template NAsP comme la meilleure solution.

Nous avons présenté une caractérisation détaillée de ce template par XRD, AFM, TEM, STEM et EDX. Les mêmes caractérisations ont été présentées de nouveau après la croissance des trois cellules sur les templates, qui ont démontré la bonne qualité des dépôts. Nous avons montré les changements apportés au processus de développement technologique pour l'adapter à la nouvelle interface III-V/Si. En particulier, nous avons introduit un nouveau niveau de photolithographie pour réaliser le contact arrière directement sur la face avant des cellules, en introduisant une grille métallique.

Enfin, nous avons présenté les performances photovoltaïques des cellules ainsi obtenues: les J_{SC} des cellules InP top et InGaAs bottom ont montré une réduction d'environ 40%; alors que les courants d'obscurité ont augmenté d'un ordre de grandeur, affectant le V_{OC} différemment. Les FF ont montré une influence significative de les nouvelles résistances introduites. Cela a entraîné une réduction des efficacités de 13.5% à 3.6% et de 11.4% à 2.0%, respectivement. Enfin, la cellule tandem a présenté moins d'influence sur le J_{SC} (étant la cellule InP la moins performante plus éloignée du Si) et le même impact sur le V_{OC} (augmentation de le courant d'obscurité). L'efficacité de cette cellule est passée de 18.3% à 5.0%. La caractéristique EQE a montré une réponse généralement réduite pour chaque longueur d'onde incidente. Nous avons identifié la forte densité des dislocations et la géométrie non optimale du contact arrière comme étant les raisons de la réduction générale des performances. Néanmoins, toutes les cellules ont montré de bons résultats en termes de photocourant et, surtout, de caractéristiques de type diode:

ainsi, la qualité de nos dispositifs, et donc la validité de l'approche proposée, ont été démontrées.

En résumé, cette thèse a permis le développement d'une filière photovoltaïque pour la technologie InP, obtenant d'excellentes cellules InP top, InGaAs bottom et InP/InGaAs tandem (ces deux dernières constituaient de nouveaux états de l'art pour les technologies respectives). Nous avons obtenu des excellents jonctions tunnel, correspondant à un nouvel état de l'art et valables pour des applications photovoltaïques en concentration. Nous avons trouvé un template prometteur pour l'intégration InP/Si; nous avons aussi réalisées des premières cellules solaires intégrées sur un substrat Si qui ont présenté d'excellents résultats en termes de photocourant et de tendances.

Les voies possibles pour les développements futurs sont l'optimisation de la passivation des cellules InP, l'augmentation du dopage de type p de l'anode de la jonction tunnel, l'optimisation du matching de courant et des bangaps dans la cellule tandem, la réduction des dislocations et l'optimisation de la géométrie du contact arrière des cellules intégrées sur Si.