



Study of synergistic effects in integrated circuits subjected to ionizing and neutral radiation in space

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THÈSE POUR OBTENIR LE GRADE DE DOCTEUR DE L'UNIVERSITÉ DE MONTPELLIER

En Électronique – Composants et Systèmes

École doctorale Information, Structures et Systèmes (I2S)

Unité de recherche IES – UMR5214

Étude des effets de synergie dans les circuits intégrés soumis à l'environnement spatial de rayonnements ionisants et neutres

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Le 27 Novembre 2018

Sous la direction de Pr. Laurent DUSSEAU
et Dr. Alain MICHEZ

Devant le jury composé de

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Abstract

Tout composant envoyé dans l'espace est soumis à de nombreuses contraintes (radiations, température) qui peuvent conduire à une défaillance de l'ensemble du système. Dans un avenir proche, ces contraintes deviendront de plus en plus critiques à mesure que les agences spatiales développeront des missions visant d'autres planètes, telles que Jupiter, pour lesquelles la contrainte radiative est extrême. Dans ce travail, deux types d'effets dûs aux radiations sont étudiés : les effets cumulatifs et les effets transitoires. L'un correspond à la dégradation induite par les radiations au cours du temps, tandis que l'autre correspond à un événement ponctuel qui peut se produire à tout moment lorsque le système est dans l'espace. Pour garantir le bon fonctionnement en vol, des normes de qualification des composants électroniques ont été élaborées par différentes agences spatiales. Toutes ces normes précisent que les effets cumulatifs et transitoires doivent être vérifiés à l'aide de composants intacts pour chaque essai. Par conséquent, les effets cumulatifs sont traités séparément des effets transitoires, alors qu'il y a une forte probabilité qu'ils apparaissent simultanément pendant une mission spatiale. L'étude des effets de synergie est alors le thème principal de cette thèse.

Sur un amplificateur opérationnel bipolaire, la réponse de sortie du composant due à un événement transitoire est directement liée aux paramètres internes du composant, qui varient sous l'effet des radiations. À l'aide d'une comparaison entre trois amplificateurs opérationnels différents partageant la même référence, l'impact du design sur la dégradation due aux radiation est étudié.

Récemment, des défaillances imprévues ont été reportées pour lesquelles le mode de défaillance semblait indiquer qu'une structure de protection contre les décharges électrostatiques (ESD) était en cause. Par conséquent, pour comprendre si ces protections peuvent causer des défaillances inattendues, la dégradation des « Gate Grounded n-MOSFET » (GGnMOS) est également étudiée.

Any system sent to space is submitted to many constraints (radiations, temperature) which may lead to a failure of the whole system. In a close future, these constraints will become more and more critical as the space agencies are developing missions aiming at others planets such as Jupiter for which the radiative constraint is extremely harsh. In this work, two types of radiation effects are studied: the cumulative effects and the transient effects. One corresponds to the radiation-induced degradation over time, while the other corresponds to a punctual event that can happen at any time when the system is in space. To ensure a proper functioning of a system sent to space, qualifications standards for electronic components have been developed by different space agencies. All of these standards specify that the components must be tested for cumulative and transient effects, using pristine components for each test. Therefore, cumulative effects are treated separately from transient effects, while there is a significant probability that they will appear simultaneously during a space mission. The study of the synergistic effects is then the main frame of this thesis.

On a bipolar operational amplifier, the output response of the component due to a transient event is directly related to the internal parameters of the component, which vary over time once in space. Through a comparison between three different operational amplifier sharing the same reference, the impact of the design over the degradation is explained.

Lately, some unexpected failures were reported for which the failure mode seemed to indicate that an Electrostatic Discharge (ESD) protection structure was involved. Therefore, to understand if those protections may cause some unexpected failures, the degradation of gate grounded n-MOSFET (GGnMOS) will be investigated next.

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During those years, had the chance to perform my Ph.D. in two different laboratory. For one part in the Institute of Electronics and Systems (IES) of Montpellier, in France, within the RADIAC team, and for another part at the European Organization for Nuclear Research (CERN), in Switzerland, within the Engineering department. Throughout those different localizations, I had the chance to encounter countless number of people that led helped me, directly or indirectly, to the success of this Ph.D. I would like here to thank them all, those that I will mention below and those that I might have forgotten.

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General Introduction

Any system sent to space is submitted to many constraints (radiations, temperature) which may lead to a failure of the whole system. In a close future, these constraints will become more and more critical as the space agencies are developing missions aiming at others planets such as Jupiter for which the radiative constraint is extremely harsh [1], [2].

In order to ensure the proper functioning of space systems, several methods have been developed to be included in the design flow. In the frame of a Radiation Hardness Assurance (RHA) process, all activities are undertaken to ensure that the electronics and materials of a space system operate according to their design specifications after exposure to the space radiation environment

The increasing cost of electronic components designed to be resistant to radiation (radiation-hardened) and the budgetary restriction of the space agencies, cause industrial enterprises to make use of more and more COST components (Component Off The Shelf) . In addition, the fast development of the technologies drives a constant improvement in the design, leaving no room for radiation-hardened components that is sometimes older and less performant.

The utilization of COTS component into radiation electronic design gives larger opportunities by the large scale of performances and functionality. The lower cost of those components gives the possibility to create a wider span of systems with higher performances. However, depending on the application, a qualification of the component used is required.

Several standards, civilian and military, were developed, to give instructions on how to qualify a COTS component for space application [3], [4], [5], [6]. COTS are sometimes also used for others applications, none space related, but for systems evolving in a radiative environment. All of these standards specify that the components must be tested for cumulative and transients effects, using pristine components for each test. Therefore, cumulative effects are treated separately from transient effects, while there is a significant probability that they will appear simultaneously during a space mission. The synergy between these two types of effects, which is not taken into account by the test standards, is then a potential cause of vulnerability that could force equipment manufacturers to use prohibitive safety margins, increasing development costs. In this study, the synergistic effect is investigated to understand which effect is more sensitive to the combination of different effects.

Lately, some unexpected failures were reported for which the failure mode seemed to indicate that an Electrostatic Discharge (ESD) protection structure was involved. Indeed, the particles emitted by the sun, the plasmas of electrons in some orbits or an intentional electron burst can cause a voltage

difference between two surfaces and can create ESDs in space. On the ground, the maintenance of systems under radiation can also be subject to ESD caused by the contact between the operator and the electronic system.

In order to extend the knowledge on which synergistic effects can cause an unexpected degradation of an electronic component or system, in space or others radioactive environment, the RADIAC group of the IES (Institut d'Electronique et des Systèmes) at the University of Montpellier has investigated synergistic effect through different Ph.D. programs. Three different PhDs have already demonstrated the impact of this synergistic effect that occurs on bipolar devices evolving in a radiative environment, submitted to total ionizing dose and displacement damage, which could be subject to Single Event Transients (SET) or Transient Radiative Effects on Electronics (TREE), caused by natural events or intentional events [7], [8], [9].

Following of these studies, this Ph.D. subject proposes to investigate another type of synergistic effects that may affect future electronics systems and provide hints on how the test standards should evolve to take into account the associated threats.

In this manuscript, two different phenomena involving synergistic effects are presented. The first section investigates the radiation-induced degradation of three operational amplifiers from different manufacturers sharing the same reference but exhibiting a very different behavior under irradiation. The second section presents the synergistic effect TID-ESD that has never been studied before. The goal of this work is: (1) to understand if the ESD protection used inside integrated circuits may be responsible for some unexplained failure at IC level and (2), if after long-term exposure to a radiative space environment, the protection structure is still able to protect an electronic component from an ESD.

The first chapter presents an overview of different radiative environments originating from natural and manmade sources, in space and on the ground. The physical mechanisms causing the degradation of electronic components due to cumulative effects are explained along with their impact on bipolar and MOSFET technologies.

The second chapter aims at showing how a physical mechanism, i.e. the displacement damage-induced degradation at transistor level in an integrated circuit may cause an unexpected response at circuit level and how this effect may be amplified due to a slight modification in the design. This work is a sequel to the work done by F. Roig on the degradation of LM124 operational amplifiers designed by three different manufacturers [10], [11]. In this previous work, a large amount of experimental data was collected that could not be exploited in the time frame of a single Ph.D. Program. The present work focuses on some unexpected results and aims at understanding why slight changes in the structures affect so significantly the degradation of these operational amplifiers.

The third chapter initiates the first investigation ever made on a new synergistic effect that may occur between the radiation-induced degradation and ESD. The first part of this chapter will explain how ESD is created, what damage it may induce and the different methods developed over the years to protect integrated structures to ESDs. Next, to understand if those protections may cause some unexpected failures, the degradation of gate grounded n-MOSFET (GGnMOS) will be investigated on a component endowed with these protections using a black box approach.

In the last part, an analysis at structure level is performed. Thanks to Microchip Technology Nantes, we had access to technological data of GGnMOS structures that we have used to do some TCAD simulations with the TCAD software ECORCE developed at the University of Montpellier. Since no irradiation results were available on the actual GGnMOS structures and no standalone structures were available, Laterally Diffused MOSFETs (LDMOS) sharing a very similar internal structure were used as test structures. The results of the LDMOS structure have been used to formulate some assumptions on the degradation of the GGnMOS structure. Eventually, through simulations and theoretical analysis, the degradation of those structures to total ionizing dose is presented and some possible methods to increase their robustness are proposed.

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I.1. INTRODUCTION

Electronics embedded in systems submitted to radiation are subject to an alteration of their physical parameters. These modifications are still today the cause of a large number of failure of electronic systems in space. The radioactive space environment is one among the most frequently studied environment, in which it is nowadays vital to use electronics and yet, its effect induced on the matter is not fully understood. Radiation effects may be sorted in two different categories known as the cumulative effects and the single event effects.

The cumulative effects usually cause a modification of the electrical parameters over time by trapping charges into the insulators or modifying the crystal lattice of a component. Its degradation can result in a modification of the triggering voltage of a transistor or an increase in the current leakage of a component for example.

The single event effects are caused by a single particle that interacts locally in an integrated circuit but it can also be transmitted to the entire circuit or system, and its effect can be temporary or permanent. Several types of single event effects are known and each one of them induces a very specific modification or degradation on a single component.

In order to use electronics components in a radioactive environment, qualification tests standards recommend a study of the degradation of cumulative effects and single event effects only by using pristine components. However, in some cases, the response to a single event effect can vary depending on the ionizing dose already accumulated and may lead to a different response compared to what was expected.

In order to prove the importance of studying the degradation of the cumulative and single event effects together, we are investigating in this document the importance of taking into consideration the synergistic effects.

The first part of this chapter is dedicated to present different radioactive environments that embedded electronics system can meet. Both natural and man-made environment in space or on the ground act differently on the electronics, thus, different impact on a system is to be expected. Then, the two different cumulative effects induced by radiation on the matter are presented. Then, to understand how the radiation acts on the electronics, two main technologies of components, known as bipolar and MOSFET used in electronics are presented with their expected radiation induced-degradation. In the end, a short state of art on the synergistic effects studies already performed is presented. It will present the previous Ph.D. led on this subject and the different synergistic effects already studied.

I.2. THE DIFFERENT RADIATIVE ENVIRONMENTS

I.2.1. THE NATURAL RADIATIVE SPACE ENVIRONMENT

Any objects sent to space are submitted to specific constraints modifying its physical and electrical parameters. The natural radiative environment originates from four different sources known as the radiation belts, the cosmic rays, the solar wind and the solar flares. Those radiations are the cause of several failures of objects sent to space. Beside the natural radiative space environment, some others environment created by the human have to be taken into account because they can be also very critical for electronics systems.

I.2.1.1 The radiation belts

The radiation belts were introduced for the first time in 1958 by the scientist James Alfred Van Allen after analyzing the data obtained by the satellites Explorer 1 and Explorer 3 [1]. This radiation belts, called as Van Allen belts, act as a charge particles shield induced by the magnetic field surrounding our planet. Because of the Earth's magnetic field, most of the particles sent by the outer source toward Earth are deflected or trapped inside these radiation belts, protecting the earth from the radiations. The radiation belts consist of two donuts shaped region, called the inner belt and the outer belt, containing high energetic radiations. They are mainly composed of electrons and protons. An artistic representation of the radiation belts is represented in Figure 1.

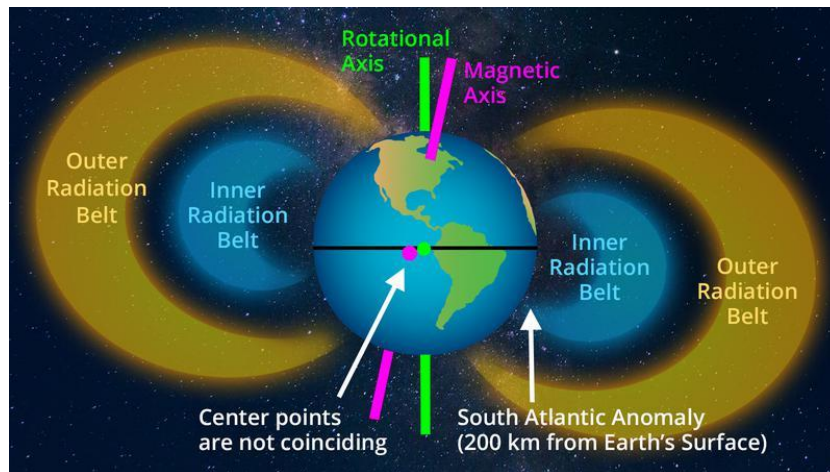


Figure 1: Artistic representation of the Van Allen belts surrounding the Earth. Credit: [2]

The inner belt evolves approximatively between 1,500 km and 13,000 km above the ground and is mainly composed of protons of few hundreds of MeV and electrons ranging between 1 MeV and 10 MeV. The outer belt evolves approximatively between 19,300 km and 40,200 km above the ground and is mainly composed of electrons with an energy between 0.04 MeV and few MeV and protons ranging between 1 MeV and 5 MeV [3], [4].

Because of these radiation belts, any spacecraft sent into space is submitted to irradiations, which will damage onboard electronics. In order to estimate the shielding needed to protect a satellite in development, different models were created by ESA and NASA. The empirical models AP8 and AE8, respectively corresponding to the Trapped Proton Model and the Trapped Electrons Model, are among the most used models by the different space agencies [5]. They contain two derivate models for minimum solar activity and maximum solar activity, known as AP8MIN, AP8MAX, AE8MIN and AE8MAX [3].

The space area is divided into three different orbits in which the satellites can evolve:

The lowest orbit area is the LEO for Low Earth Orbit. This orbit evolves between the Kármán line [6] and the beginning of the first radiation belt, between 160 km and 2,000 km. In this orbit, various types of satellites evolve for different missions like communications (ex: Iridium phones system), CubeSat, the International Space Station, and many others. Because of the low altitude, the energy required to send a satellite in this orbit is a lot smaller compared to the others orbits, and less power is required to communicate with Earth. Thus, the LEO orbit contains more spacecraft than any other orbits.

The MEO, standing for Medium Earth Orbit evolves between 2000 km and 35,786 km above sea level. The most common missions of the satellites in this region are for navigation, communication, and geodetic/space environment science [7]. Despite the very wide area, most of the satellites are positioned between 20,200 km and 20,650 km. Unlike the LEO, the MEO directly lies within the highest energetic protons of the radiations belts. Thus, any satellites sent in this orbit needs to be designed with adapted electronic and proper shielding.

The last existing orbit is the GEO orbit, which stands for geostationary orbit. This orbit, positioned at an altitude of exactly 35,786 km, allows for a full revolution in exactly one day. Because of this particularity, a satellite sent on this orbit will have a relatively static position at ground level [7]. The satellites sent on this orbit are not only submitted to high-energy protons and electrons but to heavy ions, and electrons plasma.

Depending on the satellite's mission, a specific orbit has to be selected and the satellite will be submitted to a range of radiations, as defined by the trapped particles models AP8 and AE8. Therefore, any satellites sent to space needs to have its own environmental study.

I.2.1.2 The cosmic rays

The cosmic rays are highly energetic radiation coming from distant galaxies, stars, supernovas, etc. with an energy starting from 100 MeV up to 10^{21} MeV for the highest energy [8]. They are composed of 1% heavy ions, 2% of electrons, 12% of helium and 85% of protons [9].

The galactic cosmic rays were discovered by Victor Franz Hess in 1912 by using three enhanced-accuracy electrometers at an altitude of 5,300 meters in a free balloon flight [10].

Due to their high energy, there is no efficient way to protect an electronic device from them. However, because the flux is very low, the interaction's probability with an electronic component is low. It is then often neglected for the radiation-induced damage estimation [11].

I.2.1.3 The solar wind

This phenomenon was first introduced to the community by the German astronomer Ludwig Biermann in 1951 in his article "*Kometenschweife und solare Korpuskularstrahlung*" (in English: Comet tails and solar corpuscular radiation). His discovery, based on the study and observation of comet, conclude that no matter whether a comet is headed towards or away from the Sun, its tail always points away from the Sun. Biermann postulated that this happens because the Sun emits a steady stream of particles that pushes the comet's tail away [12].

The solar wind is a plasma stream consisting essentially of ions and electrons that are ejected from the Sun's upper atmosphere. Because of the low energy, most of the particle can be stopped with an appropriate shielding.

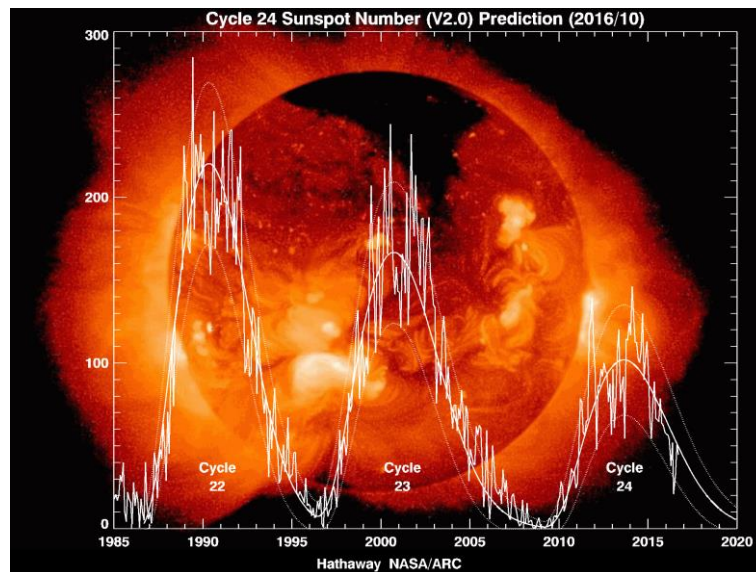


Figure 2: Solar activity recorded since 1985 up to now [13]

It is understood that the sun activity evolves following a cyclic pattern known as the solar activity. It varies following a pattern of 11 years with seven years of high activity and four years of low activity as presented in Figure 2 [14]. Depending on this activity, the particles emitted by the solar wind will be more or less energetic. Therefore, depending on the launch date, satellites may have to be designed to be more robust against radiation to survive to a high solar activity, and some missions are sometimes delayed to be sent during a low solar activity.

I.2.1.4 The solar flares

Compared to the solar wind that constantly emits particles, a solar flare is an unpredictable phenomenon caused by the rupture of the sun's magnetic field lines, ejecting at very high speed and high energy particles such as protons and ions. The energy range of those particles are not as high as the cosmic rays, but can still reach few hundreds of MeV for the protons and few tens to hundreds of MeV for the ions. A picture representing a solar flare is presented in Figure 2.

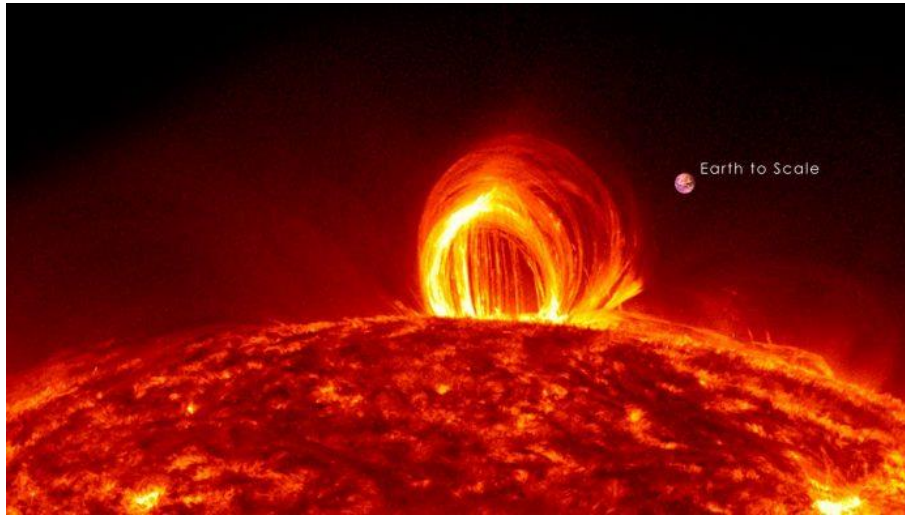


Figure 3: Picture representing a coronal mass ejection from the sun. The earth is represented on the same picture for scale [15].

When a solar flare occurs, the particle shower can last from hours to a couple of days depending on the intensity of the flare. Moreover, because the particles ejected have not the same mass, speed or energy, the first particles reaching the Earth's proximity are the light particles like the electrons, which reach a speed close to the speed of light and take around 8 minutes to reach the firsts satellites. Others particles like heavy ions or protons can take several hours or days to reach the Earth's outer space.

After a solar flare, the amount of trapped particle inside the radiation belts increases, protecting with higher efficiency the earth from others particles, but the environment is then more dangerous for the satellites. This increased amount of trapped particles is observable at the earth's poles as aurora borealis.

I.2.2. THE MAN-MADE RADIATIVE SPACE ENVIRONMENT: EXOATMOSPHERIC NUCLEAR EXPLOSIONS

In the case of an exoatmospheric nuclear explosion, that can be provoked intentionally with a weapon, two types of radiation-induced effects caused by radiation to any electronic systems within the range of the explosion: the direct effects and indirect effects.

The direct effects are caused by the nuclear explosion itself. Any satellite within range will be submitted to a large spectrum of high-energy radiations composed of γ -rays, neutrons, and x-rays. The x-rays are among the most energetic particle that can be over 100 times higher than the γ -rays [16]. However, because of its penetration power into the matter, the γ -rays causes more damages [17].

The indirect effects are caused by the particles emitted during the nuclear explosion that are trapped inside the Van Allen belts which, after the explosion, will stay inside the belts, causing an increase of the trapped particles or to the creation of artificial radiation belts. For example, following the series of exoatmospheric nuclear experiments accomplished by the USA and the USSR in the late 50's and early 60's, a series of at least 10 satellites successively failed (7 in 7 months), among which TELSTAR, TRANSIT 4B, TRAAC, and ARIEL, and a number of other ones were impaired such as OSO-1 (Orbiting Solar Observatory) due to the modification of the radioactive space environment [4].

I.2.3. THE MAN-MADE RADIATIVE TERRESTRIAL ENVIRONMENT: THE PARTICLE ACCELERATORS

Many facilities offer particles accelerators developed for science studies or medical purposes. CERN in particular is known for its Large Hadron Collider (LHC), the most energetic and the longest accelerator on the planet.

LHC's radiative environment consists of a mixed field of particles composed of charged and neutral hadrons (protons, pions, kaons, and neutrons), photons, electrons and muons [18]. This complex field is due to particles generated by the collision proton-proton (or ion-ion) in the experimental areas, the distributed and direct beam losses (protons, ions) around the machine caused by some particle of interacting with the pipes, and the beam interacting with the residual gas inside the vacuum [18], [19].

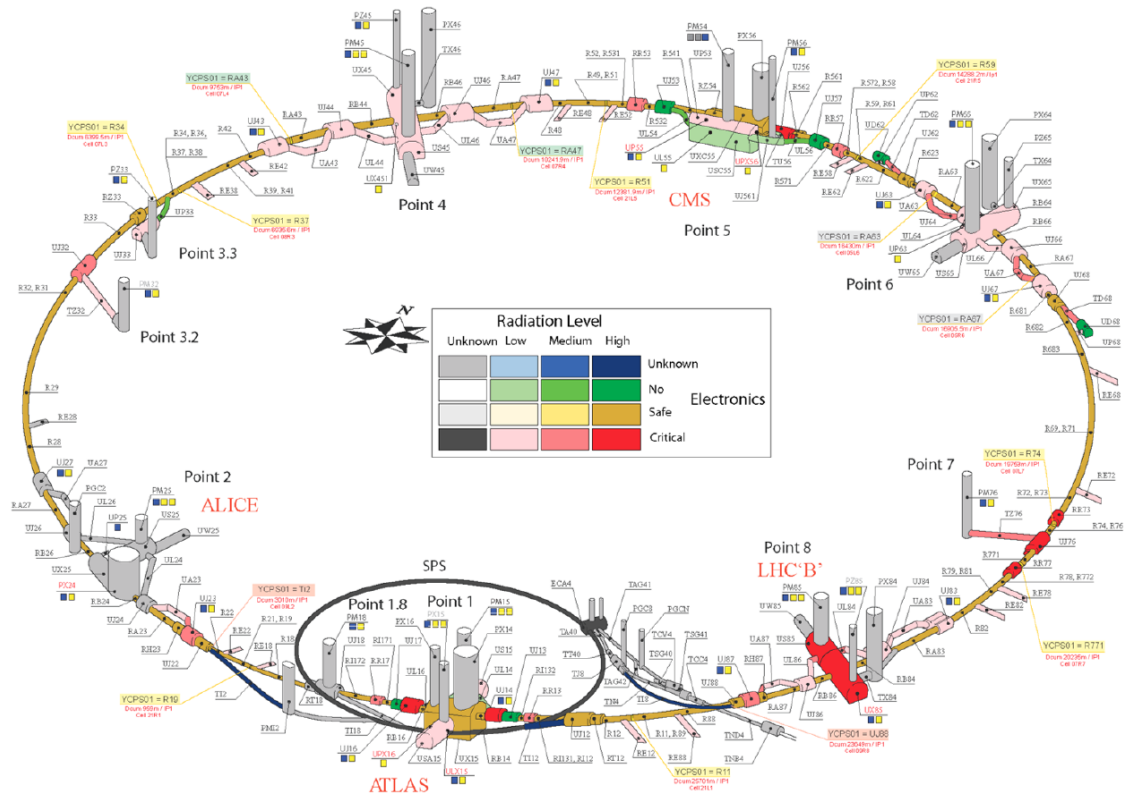


Figure 4: Representation of the radiation level all along the LHC tunnel. A color scale defines the criticality of the electronic depending on the expected radiation.

As presented in Figure 15, the LHC environment is very versatile and it can change a lot depending on the position inside the tunnel. In this picture, the color scale defines the level of radiation depending on the criticality of the electronics inside the LHC. For example, in all the tunnels, the dose expected is high but the electronics systems are not critical. Thus, most of the electronics used are COTS components. In comparison, some areas like the point 1, 2, 5 and 8 host a lot of electronics used to control the beam for the collisions. Therefore, the harsh radiation environment jeopardizes the control of the beam and hardened components have to be used.

A large part of CERN's accelerator control systems are not explicitly designed to be radiation hardened or radiation tolerant but are still exposed to a certain level of radiation that depends on their position in the tunnel [20]. Thus, most of the electronics placed inside the radioactive LHC environment have to be tested to radiation whereas the electronic for the critical areas are often radiation-hardened components.

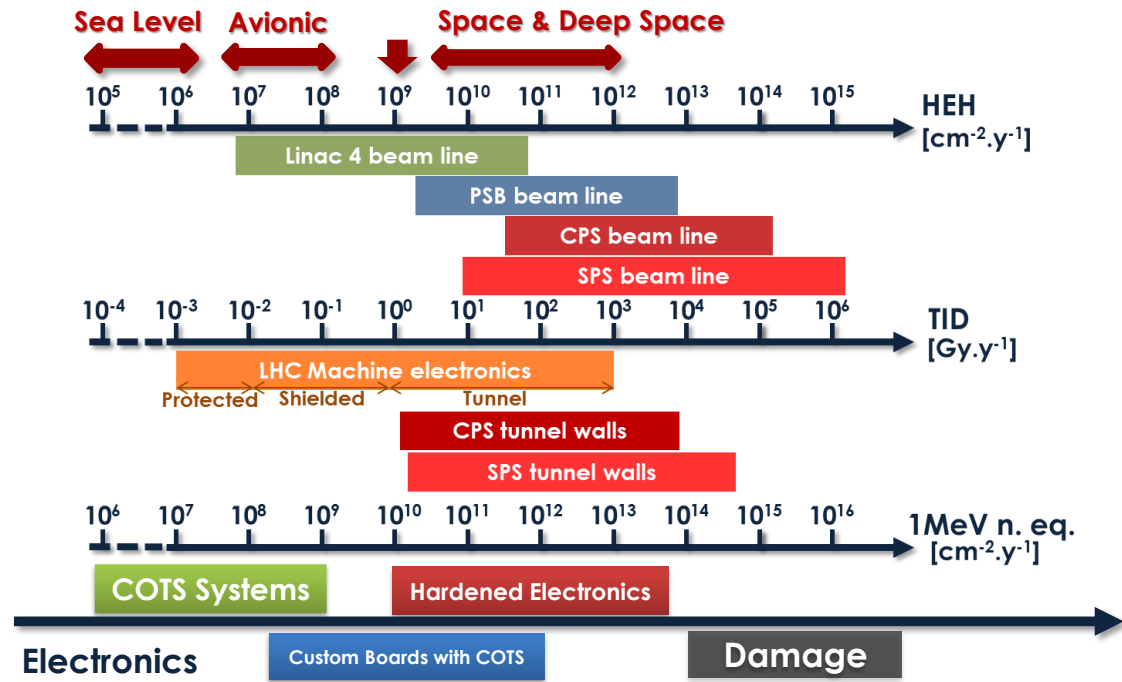


Figure 5: Usage of the electronic depending on the radiation levels inside the different tunnels of the CERN [19].

Figure 5 describes the utilization of the electronics inside the different CERN's tunnels depending on the doses, fluencies and High Energy Hadrons (HEH). As presented on this figure, not all the electronic used inside the CERN's facilities are designed with hardened components. Some systems placed inside the protected areas, for example, may be designed with an only board designed with COST component, but most of the system has to be designed with a custom board with COTS tested to radiation or radiation hardened components.

I.3. CUMULATIVE RADIATION EFFECTS ON ELECTRONIC DEVICES

I.3.1. THE TOTAL IONIZING DOSE

I.3.1.1 The concept of Total Ionizing Dose

The Total Ionizing Dose or TID is a cumulative effect that induces an energy deposition, by ionization of the matter causing a generation of electron-hole pairs. This ionization is caused either by the interaction of high-energy photons, by charged particles such as protons, electrons and sometimes heavy ions with atoms of the target material [9], [11], [21]. The TID corresponds to a certain quantity of energy deposited per mass unit:

$$D = \frac{\Delta E}{\Delta m} \quad \text{with } 1\text{Gy} = \frac{J}{kg} \quad \text{Equation I.3-1}$$

Where D is the ionizing dose expressed in Gray [Gy], ΔE corresponds to the energy deposited expressed in Joules [J], and Δm to the mass expressed in kilograms. The *Gray* unit is defined in the standards international system of unit since 1985, nevertheless, the previously used unit called the *rad* for *Radiation Absorbed Dose* is still used to quantify a dose degradation of the electronic component. One Gray corresponds to 100 rad.

Another parameters qualifying the TID is the dose rate. This unit expressed in $[\text{rad.s}^{-1}]$ or $[\text{Gy.h}^{-1}]$ corresponds to the energy deposit per time unit:

$$D' = \frac{\Delta D}{\Delta t} \quad \text{Equation I.3-2}$$

Depending on the technology, the dose rate can be a key parameter. Indeed, for bipolar technologies, the reduction of the dose rate increases the degradation of the component for the same TID level. This principle, called Enhance Low Dose Rate Sensitivity, has been largely studied in [22]–[26], however, this latter will not be discussed in this manuscript.

I.3.1.2 Photon-Matter interaction

TID radiation testing is usually performed with ^{60}Co γ -rays source. A ^{60}Co source produces a constant emission of γ -photons of 1.17 MeV and 1.33 MeV that interact with the matter mainly by Compton Effect [27]. As represented in Figure 6, during an interaction by Compton Effect, a part of the incident photon's energy, $h\nu$, is transferred to a peripheral electron and ejected it from its orbit. The initial photon passes then from an initial energy $h\nu$ to a lower energy $h\nu'$, with the difference corresponding to the

energy transferred to the electron [28]. The remaining photon, if it still has enough energy can interact with another electron from another atom, etc.

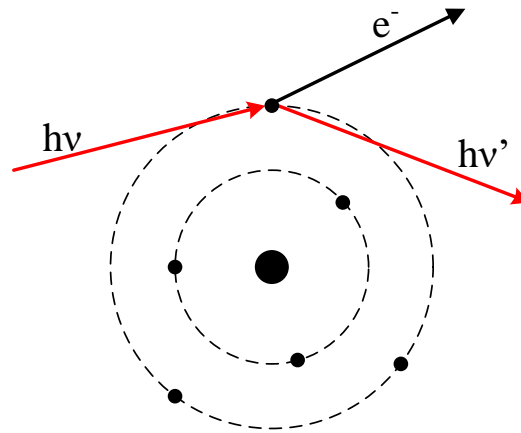


Figure 6: Representation of a Compton Effect

Even if γ -rays are not presents in the space environment, its controllability and penetration into the matter makes it a good source of radiation testing [29].

I.3.1.3 Degradation mechanism of the dose on the materials

Due to their intrinsic properties, the insulating material of electronic devices is the most sensitive part to ionizing dose. Its low charge density makes any electrical conduction impossible. Injection of additional charges will then modify, all along the dose accumulation, the electrical properties of the insulator [30]. Depending on the component's technology, the silicon oxide (SiO_2) plays a role more or less important.

The MOSFET technology uses the electric field generated inside the gate oxide, by applying a potential on the gate contact, and acts on the substrate to create a conduction channel. Because silicon oxide of the MOSFET generates this electric field, any modification of its electrical parameters would affect the electric field generated for the same voltage applied and modify the voltage threshold of the component [31], [32]. Nowadays, MOSFET's gate oxide tend to be as thin as possible, in order to increase their performances by reducing the amount of defects inside the oxide and manufacture a highly homogenous structure. The reduction of gate oxide thickness has been astonishingly successful so that oxides with a thickness of roughly 20 \AA are being manufactured [33].

Bipolar technology does not use the silicon oxide for the same reason as the MOSFET technology. Because of their structure, the silicon oxide is only used to protect the component from any external contamination (dust, light, UVs, etc.). Therefore, the quality of those oxides is often bad and does not affects the electrical properties of the component. No thickness reduction or increase in the quality is performed since that would increase unnecessarily the cost for a similar result.

Although the impact of the radiation affects all oxides based on the same fundamental mechanism, the radiation-induced degradation is completely different on BJTs and MOSFETS. Therefore, the studies of their degradation is considered separately.

The various physical phenomena detailing the entire process, i.e. from the initial deposition of energy by ionizing particles to the creation of defects in silicon oxide, can be broken down into four steps that are the electron-hole pair creation, the initial recombination, charge drift into the oxide and defect creation into the oxide and at the interface [34].

When an oxide is under irradiation, electron-hole pairs are created in the dielectric [31], releasing a kinetic energy that ionizes the matter. Just after the ionization, a large part of the electron-hole pairs created will be immediately recombined. Depending on the electric field into the oxide, the fractional yield of the electron-hole pairs varies [30], [35]. The remaining electrons are pushed outside the oxide, leaving the holes, which have a much lower mobility, trapped inside the oxide. The fraction of electron-hole pairs that escape the initial recombination is called the electron-hole yield. The holes that escaped the initial recombination will slowly move toward the higher potential with a speed that depends on the temperature, the electric field, the oxide thickness and the holes distribution inside the oxide [34]. When the holes get closer to the Si/SiO₂ interface, a part of the holes are recombined with the electrons of the substrate, and some other will react with hydrogen passivated Si dangling bonds to create interface traps at the Si/SiO₂ interface [36], [37]. During the hole drift and/or trapping, protons can be liberated in the bulk or near-interfacial SiO₂, leading to a modification of the potential under the oxide. In the end, fractions of the holes are trapped at defect sites near the Si/SiO₂ interface [36], [38].

I.3.2. THE DISPLACEMENT DAMAGE DOSE

I.3.2.1 Displacement Damage mechanism

The Total Non-Ionizing Dose or Displacement Damage is the result of nuclear interactions between a particle and the matter, causing lattice defects. It can be caused by several types of particle such as the neutrons, protons and heavy ions. Their interaction with a semiconductor material causes a creation of defects in the crystal lattice, leading to the reduction of the mobility, and increase the quantity of traps [39].

Silicon wafer used to manufacture the electronic component are created in a very specific way that organizes the silicon lattice close to a crystalline lattice. Therefore, when a particle interacts with this lattice, it creates a disorder in the silicon lattice. A representation of the displacement damage effect is represented in Figure 7. When the particle interacts with an atom from the silicon lattice, a part of its energy is transferred to this atom, displacing it somewhere else in the lattice. If the incident particle still

has enough energy, it will continue its travel inside the silicon lattice and will eventually interact with other atoms.

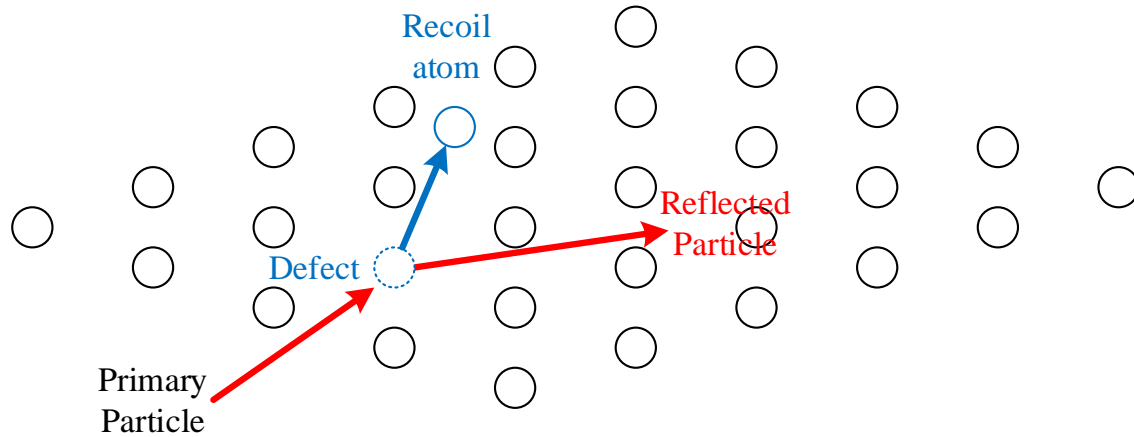


Figure 7: Representation of the mechanism of defect creation onto the silicon lattice. Displacement damage is caused by a displacement of atoms.

The empty space left to create a defect, while the recoiling atom will stay in the middle of the lattice as an interstitial particle. The combination of the defect and the interstitial atom is called a Frenkel pair [40], [41]. These defects result in the creation of energy levels in the forbidden band of the semiconductor, which influences the conductivity of this material.

A displacement defect occurs when an atom of the target material is displaced from its initial location by radiative energy particles, and produce a permanent degradation [40], [41].

When a particle interacts with the silicon lattice, the first atom to be displaced is called the Primary Knocked-on Atom (PKA). Depending on the type of interaction or the energy of the incident particle, two different situations can happen.

In the first case, if the energy exchange between the particle and the atom is too low, only the atom will be displaced. It is usually the case for the interaction with low energy particle because only the Rutherford or Coulomb diffusion occurs.

In the second case, if the exchange between the particle and the atom is high, the displaced atom will gain a high energy and in turn, will interact with others particle, etc. In this case, a large number of successive collision can be produced leaving a defect trail in the silicon lattice creating a cluster of defects. An example of a cascade is shown in Figure 8 for a silicon atom with a recoil energy of 50 keV produced by a 1MeV neutron. Clusters are similar to a cluster of displacement defects.

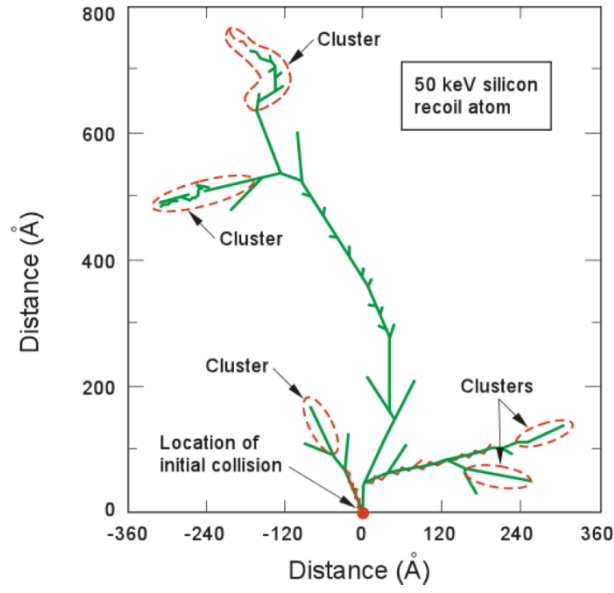


Figure 8: Cascade of defects calculated with a PKA of 50 keV produced by a 1MeV neutron into a silicon lattice [42]

I.3.2.2 Displacement damage on electronic devices

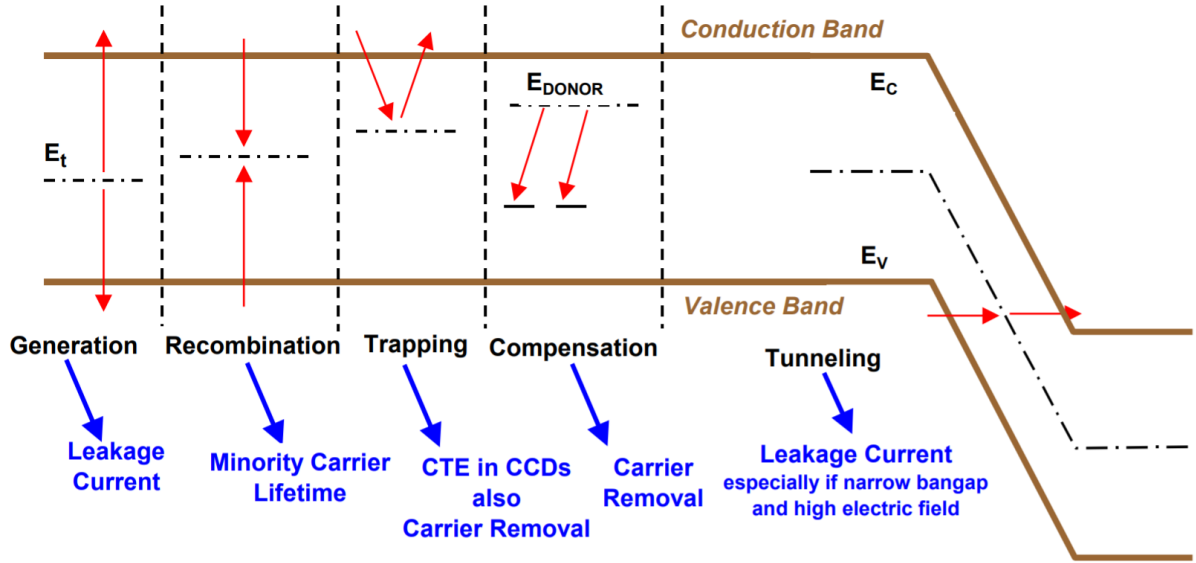


Figure 9: Electrical effects on a semiconductor material induced by the presence of energy levels in the band gap due to displacement damage[43].

After the creation of the defects, when the particle is stabilized and stop moving, it can interact with the electronic devices following five different processes that are presented in Figure 9 [38], [43], [44].

- The electron-hole pair recombination happens by the emission of an electron in the conduction band and a hole in the valence band. This mechanism leads to an increase in the leakage current in silicon material.

- The electron-hole pair recombination is explained by the trapping of a positive carrier with a negative carrier. Due to the proliferation of these traps within the band and due to displacement damage, the life of minority carriers is reduced.
- Trapping of carrier temporary. That will eventually be reemitted in its band after certain duration.
- The doping compensation is explained by trapping of the predominant carriers inside the traps, reducing the doping value of the area.
- The tunneling effect describes a particle going through the valence band up to the conduction band. This phenomenon is mainly caused by a modification of the band slope. More the electric field is high; more the particle will cross the bands easily. The tunneling effect causes an increase in the leakage current. This case is more relevant to MOSFET technologies.

I.4. THE BIPOLAR TRANSISTOR

I.4.1. WORKING PRINCIPLE

The bipolar transistor (or Bipolar Junction Transistor) was introduced to the community in 1948 by the Bell Telephone Laboratories [45]. It consists of three semiconductor layers stacked together with the two layers on the extremity of the same type (n or p) and one layer of the opposite type in-between. As represented in Figure 10, the NPN bipolar transistor is composed of two N doped semiconductors separated with a P doped semiconductor, and for the PNP transistor consists in two P doped semiconductor departed by an N doped semiconductor. For both components, from the left to the right, those layers are named the emitter, the base, and the collector. Those blocs consist in two PN junctions top to top for the NPN transistor and back to back for the PNP transistor. If we take the example of the NPN transistor, the doping value of the emitter is every time higher than the one of the collector because the emitter area emits the electrons that are collected by the collector.

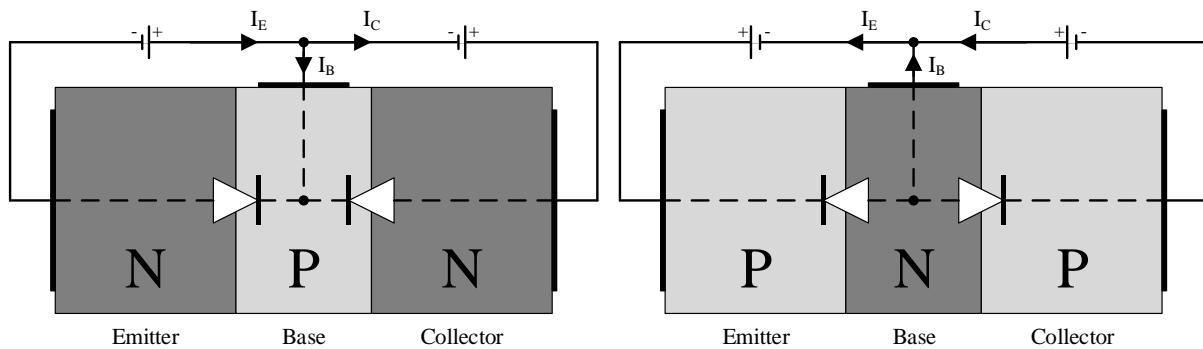


Figure 10: Representation of an NPN bipolar transistor on the left and a PNP bipolar transistor on the right.

When the diode between the base and the emitter is biased in forward mode, the majority carriers (electron for the case of the NPN) are injected from the emitter to the base. A part of the electrons injected is recombined with the holes present inside the base, but because of the low thickness of the base, the rest of the electrons injected are pushed toward the depletion area of the base-collector junction. The electrons that have reached the base-collector junction without being recombined are accelerated by the electric field of the depletion area of the diode in reversed bias mode. The higher the voltage of the base collection junction, the larger the depleted area will be and will accelerate the electrons. A simplified representation of this mechanism is presented in Figure 11.

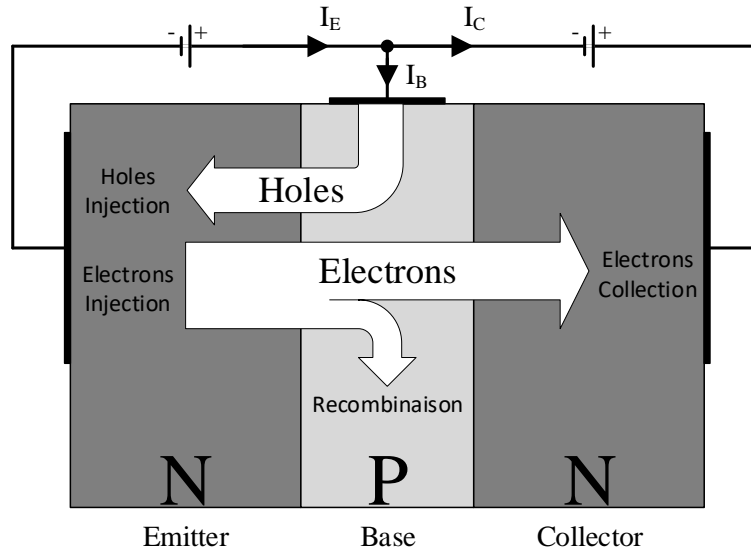


Figure 11: Representation of the transistor effect mechanism occurring on the normal operation of an NPN bipolar transistor

The current gain of the transistor corresponds to the ratio between the collector current and the base current.

$$\beta = \frac{I_C}{I_B} \quad \text{Equation I.4-1}$$

This gain is one of the main parameters of the bipolar transistors, defining its performances. Depending on the application, it ranges from 20 to 100 for high power applications and from 100 to 800 for the low power applications.

Integrated bipolar transistors exist in four different structures that can be used for specific purposes:

- Vertical NPN transistor (VNPN)
- Vertical PNP transistor (VPNP)
- Lateral PNP transistor (LPNP)
- Substrate PNP transistor (SPNP)

Besides their shape, each structure differs by their current flow. Those structures are presented in more detail in the section II.4.2.

I.4.2. THE SENSITIVITY OF BIPOLAR TRANSISTOR TO TID AND DD

I.4.2.1 Effect of the TID on bipolar structures

As presented before, ionizing radiation results in an increase of charges and defects inside the oxides, and creation of interface traps impinging on the mobility of the holes or electrons. Each one of those

effects acts on bipolar transistor in a different way, but, the main parameter degraded by irradiation is the current gain β [36], [46]–[48]. Figure 12 represents the current grain degradation depending on the base-emitter voltage for different total accumulated dose with, on the top left the curve before irradiation and on the bottom right, the curve after irradiation. As observed the gain current exhibits the most important decrease for the lower base-emitter voltages compared to the higher base-emitter voltage that does not show such a large degradation.

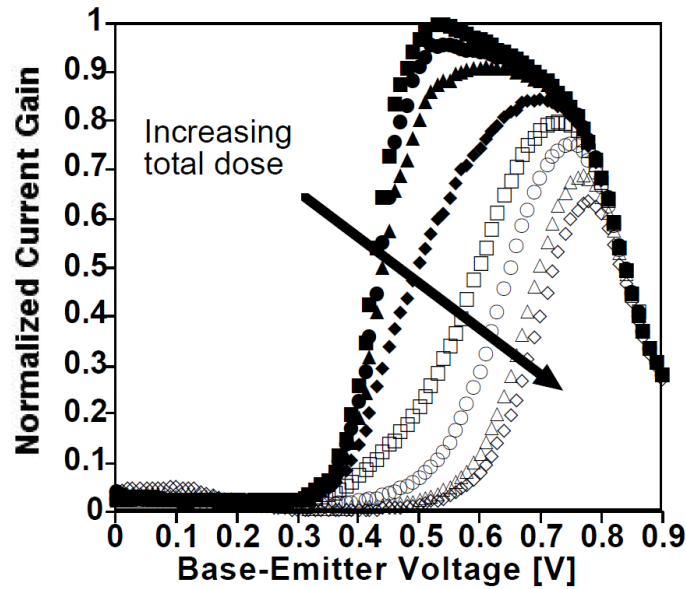


Figure 12: Normalized current gain vs. base-emitter voltage for an NPN bipolar transistor irradiated to various TID values [49].

This degradation can be explained by an increase of the base current of the bipolar transistor resulting from an increase of the recombination rate caused by a larger depletion region and the increase of the surface recombination speed [50] while the collector current remains roughly constant.

It is important to note that depending on the particle used to irradiate the component, the degradation will be different. For example, protons cause a TID and DD degradation on the component, so the radiation-induced degradation between proton and γ -rays or electrons will be different [51].

Besides the current gain degradation, an integrated bipolar structure can show a device-to-device or collector-to-emitter leakage current caused by radiation-induced degradation of the isolation oxides, deep trench and buried oxides [52]–[54].

As explained in the previous section, four different bipolar structures exist and all of them are often used as integrated bipolar transistor. Then, because the radiation-induced trapped charges degrade the component by impacting on the current flow, different sensitivities to TID are to expect for the different bipolar transistors structures.

I.4.2.2 Effect of the DD on bipolar structures

The first studies related to the radiation-induced degradation caused by displacement damage date back to the 60s. In their work, Messenger and Spratt developed an equation able to describe the degradation of the current gain amplification caused by neutron irradiation [55]–[57].

$$\frac{1}{\beta} = \frac{1}{\beta_0} + \frac{K \Phi_n}{2\pi f_T} \quad \text{Equation I.4-2}$$

Where β corresponds to the current gain, β_0 to the current gain before irradiation, Φ_n to the neutron fluence and K to constant of proportionality [49]. To summarize, the Equation I.4-2 describes that the base current is inversely proportional to the minority-carrier lifetime in the emitter-base depletion region or the neutral base. The same equation can be used to describe the displacement damage induced by other particles such as the heavy ions, protons, and electrons.

I.4.3. SENSITIVITY TO TID OR DD DEPENDING ON THE TRANSISTOR STRUCTURE

As explained before, most of the species trapped into the oxide are holes, thus, the resultant impact of those trapped charges will affect the component differently if it is an N-type or a P-type. Moreover, considering the current flow in each type of structure (lateral or vertical) the effect of the trapped charges on the current flow will be also different. Figure 13 presents the sensitivity of different types of bipolar transistors depending on their structure for a total dose of 500 krad(SiO₂). This graphic, presented by Schmidt *et al.* in [58], describes that lateral bipolar transistors are more sensitive to TID than vertical structures because the current flux passes close to the passivation oxide for the lateral and into a buried layer for the vertical structures.

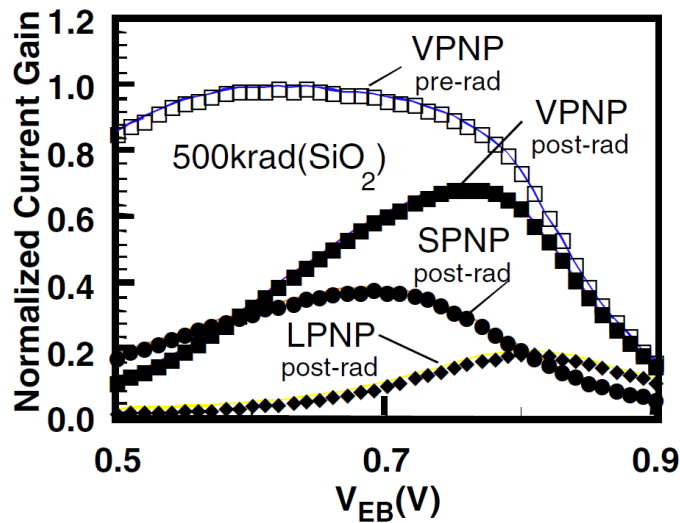


Figure 13: Comparison of post-irradiation current gain for three different types of PNP BJTs [58]

Like the radiation-induced degradation caused by ionizing dose, it is important to note that depending on the structure of the bipolar transistor, different degradations are expected with the displacement damages because the current flows for each structure are different. For example, Barnaby *et al* [46], [59] and Rax *et al.* [60] showed that the degradation of Vertical NPN, Vertical PNP, and Substrate PNP transistors are more important with proton and neutron irradiations compared to ionizing irradiation. Those irradiations simultaneously degrade the surface recombination velocity, the net positive oxide charge and the collector-region lifetime, which is a very sensitive parameter for bipolar technologies. As a result, both particles will subsequently cause an increased degradation of the current gain.

I.5. THE MOSFET TRANSISTOR

I.5.1. WORKING PRINCIPLE

The MOSFET transistor (Metal Oxide Semiconductor Field Effect Transistor) is nowadays one of the most commonly used transistors inside electronic components. The first idea of a MOSFET structure comes back to the year 1925 when it was patented by Julius Edgar Lilienfeld. Only 35 years after, in 1959, the first transistor was designed by Dawon Kahng and Martin M. Atalla at Bell Labs.

A simplified structure of a MOSFET transistor is presented in Figure 14. Its construction relatively simple is composed of two wells of the same type inside a silicon called the drain and the source (doped n for the N-MOS and p for the P-MOS), separated by the substrate of an opposite doping. Because of this structure, the current is blocked between the two wells. The gate added between the two wells is placed on the top of the silicon and is separated by a silicon oxide insulator. With this topology, no current passes by direct conduction through the channel. Only the generated electric field, by attracting the holes or electrons depending on the type of component (N-channel or P-channel), creates a channel allowing the conduction between the drain and the source.

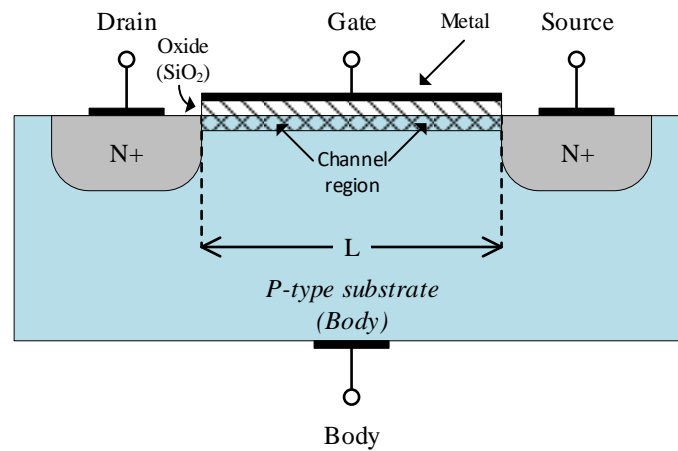


Figure 14: Simplified structure of an n-type MOSFET transistor

Several topologies of MOSFET transistors exist depending on their applications, but to sum up, the aim of the MOSFET is to be able to control the current flow between the source and drain by varying the gate voltage.

In this thesis, two different topologies of MOSFET transistors such as the GGnMOS (Gate Grounded N-MOSFET) and LDMOS (Laterally Diffused MOSFET) will be studied. Those two structures are presented in details in Chapter 3 and Chapter 4.

I.5.2. THE SENSITIVITY OF MOSFET TRANSISTOR TO TID

As explained before, the ionizing dose creates trapped charges into the oxide that moves from one side to another depending on the electric field inside the oxide. Those charges, while moving into the oxide, can be recombined or create defects by moving close to the interface, which changes the behavior of the component. On a MOSFET transistor, the typical radiation-induced degradation modifies the threshold voltage of the component and will then increase the drain leakage current. In a general case, the traps are created by a weak atomic link that creates holes traps [61].

A trapped charge into the oxide can be mobile, fixed, trapped inside the oxide or trapped at the Si/SiO₂ interface. The mobile charges and trapped charges are located into the entire volume and the interface traps are mostly located close to the Si/SiO₂ interface. This placement is mainly caused by the repartition of the electric field into the oxide during the irradiation. Positive electric field into the oxide will push the holes toward the Si/SiO₂ interface increasing the degradation of the parameters of the transistor.

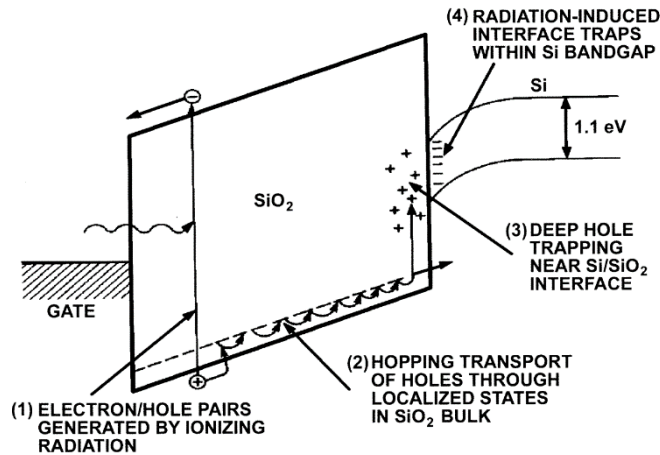


Figure 15: Representation of the four main degradation mechanism induced by ionizing radiation into a MOS structure with a positive biasing [62].

A representation of the four main mechanisms of degradation is presented in Figure 15. At first, ionizing radiation creates an electron-hole pair (1). The positive electric field generated by the voltage biasing at the gate pushes the holes toward the Si/SiO₂ interface by successive hopping (2), whereas the electrons will be pushed toward the gate contact. Once the holes have reached the Si/SiO₂ interface a part of them are trapped into deep traps (3), leading to a long-term trapping and some others generate interface traps within the Si band gap (4). Throughout all the irradiation, a continuous flow of holes is trapped, by flowing the four mechanisms presented. Over time, the increase of those trapped charges increase the impact on the shift of the threshold voltage of the MOSFET transistor. Furthermore, for the same irradiation, if the electric field in the oxide is higher because the holes will move faster toward the Si/SiO₂ interface, the quantity of recombined charges will be reduced. This lead to an increase in the

quantity of charges trapped and interface traps close to the interface. Consequently, the threshold shift will be higher.

The total shift of the voltage threshold is caused by the increase of the charges inside the oxide (Q_{ot}) and the charges trapped at the interface (Q_{it}).

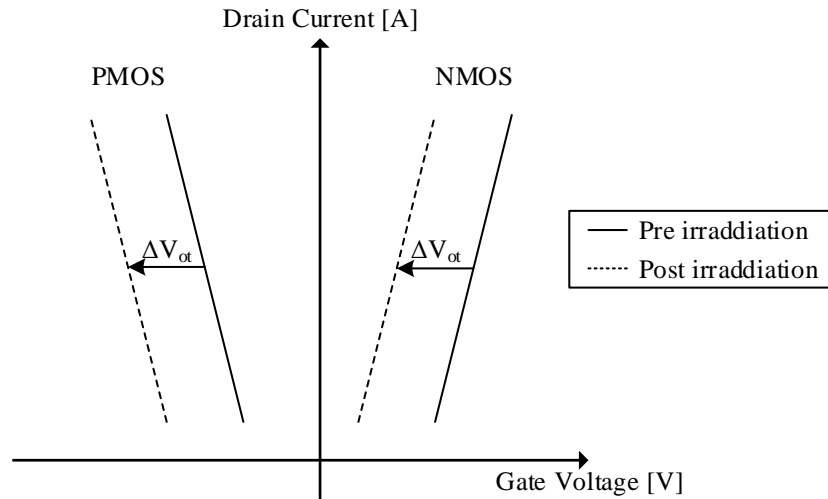


Figure 16: Representation of the impact of the positive trapped charges into the oxide on the characteristics of the MOSFET transistors.

The trapped charges inside the oxide can be positive or negative and its density is labeled N_{OT} . In the silicon oxide, the trapped electrons, because of their mobility higher than the holes, are evacuated by the metal contact. For the trapped holes, that are slower, moves gradually toward the Si/SiO₂ interface, therefore, the trapped charges inside the oxide is mainly positive. It is this last phenomenon that causes an alteration of the electrical characteristics of the electronic components such as the negative and parallel drift of the current-voltage characteristic of the MOSFET transistor. A representation of the variation of the MOSFET characteristics caused by the positive trapped charges inside the oxide is shown in Figure 16.

The interface traps density is labeled N_{IT} . They interact with the carrier inside the silicon by slowing down their mobility while crossing the channel. Therefore, as presented in Figure 17, this mobility reduction modify the MOSFET characteristic slope.

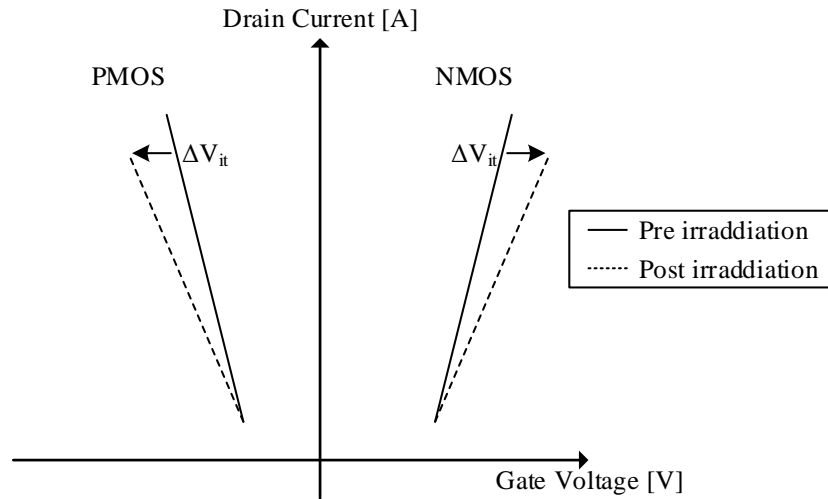


Figure 17: Representation of the impact of the interfaces traps on the characteristics of the MOSFET transistors.

In addition, in order to separate one component to another, shallow trench or deep trench are sometimes implemented as a separation wall between the components in order to avoid current to pass from one component to another and maybe disturb their normal operation. Radiation induced degradation on those oxides can lead to a creation of the path through them, increasing then the leakage current of the component.

I.6. STATE OF ART OF THE SYNERGISTIC EFFECTS STUDIES

Synergistic effects have been studied for more than ten years in the RADIAC (RADIAtion and Components) research group of the IES of the University of Montpellier. Several Ph.D. programs were dedicated to the investigation of different synergistic effects in collaboration with different civilian and military institutions such as the French Alternative Energies and Atomic Energy Commission (CEA, stands for *Commissariat à l'Énergie atomique et aux Énergies alternatives* in French), the French Directorate General of Armaments (DGA, stands for *Direction Générale de l'Armement* in French), the National Centre for Space Studies (CNES, stands for *Centre national d'études spatiales* in French) and Thales Alenia Space (TAS).

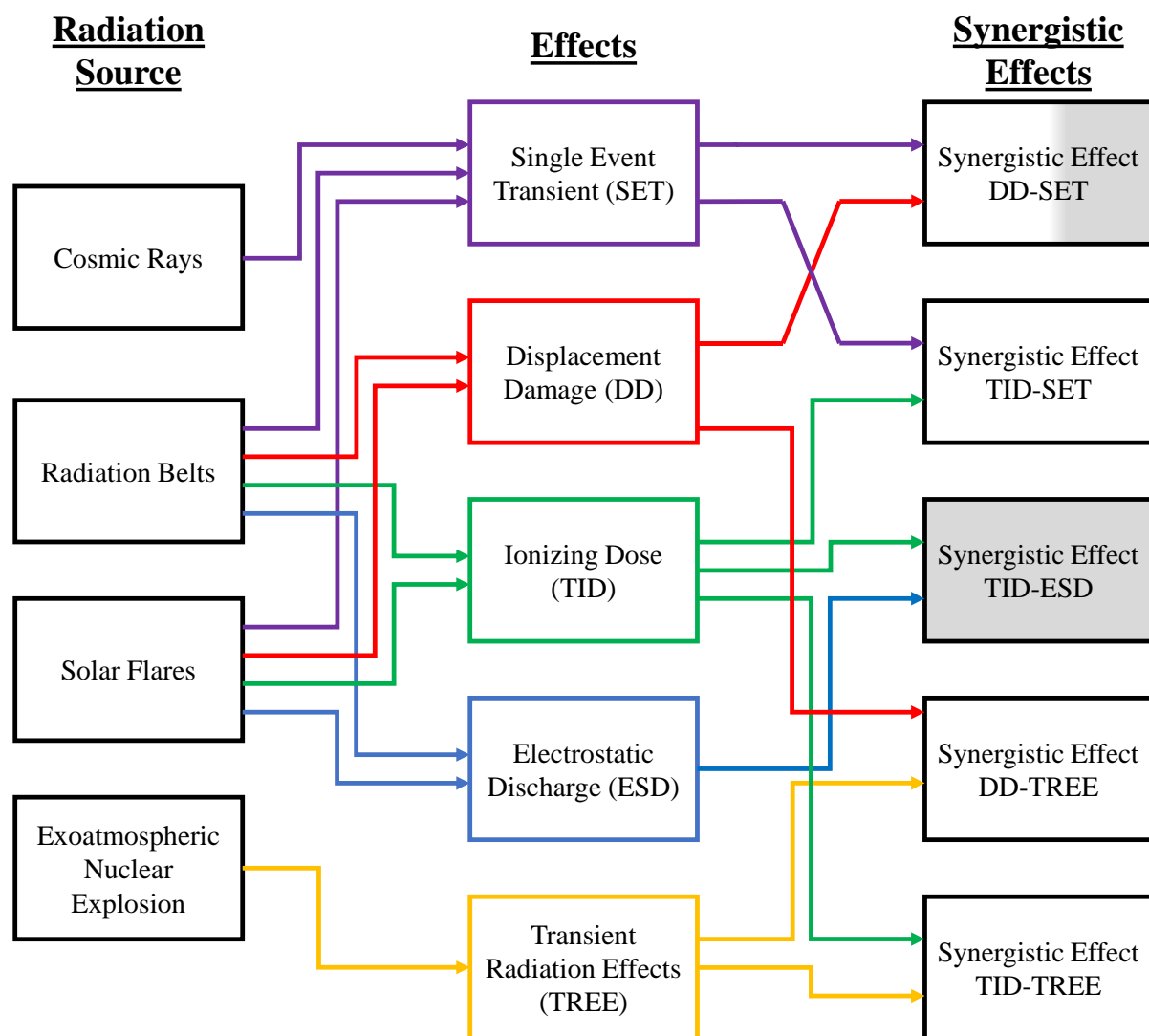


Figure 18: Presentation of different synergistic effects studied on this series of PhD

M. Bernard initiated this topic by investigate the synergistic effect between the TID and the SEE on a bipolar voltage comparator [63]. N. Roche extended the research of the synergistic effects by studying

the influence of the TID on the response to SEE and Transient Radiation Effects on Electronics (TREE, in the case of an exoatmospheric nuclear explosion) of bipolar operational amplifiers [16]. F. Roig continued this work by investigating the influences of the DD on the response to SEE and TREE of others bipolar operational amplifiers. In addition, a study of three bipolar operational amplifiers from a different manufacturer was investigated to understand how the layout design of a component could affect the response to synergistic effects [17].

Figure 18 depicts a simplified representation of the different synergistic effect with, in which the effects already studied and reported in the previous Ph.D. programs and in grey, the synergistic effects that are studied within the scope this Thesis.

I.7. CONCLUSION

This chapter has introduced at first the radiation-induced degradation origins for space environment as well as on the ground. Depending on where a system is located, it can be submitted to different types of particles such as photons, protons, neutrons, electrons for the most known. Each particle can have different energy and interact with the matter in a different way. Some effects produce a cumulative effect and others transient effect, that can act on electronic devices in a different way.

The cumulative effect is the result of the accumulation of radiation-induced degradation over time and tends to modify continuously the physical parameters of the component. Two different cumulative effects are today considered: The Total Ionizing Dose (TID) and the Displacement Damage dose (DD). The TID ionize the matter while the DD create defects inside the matter by displacing atoms inside the silicon lattice. Because those two effects are completely different, they deserve a proper separated study. Moreover, depending on the technology of the component (bipolar or MOSFET) the radiation induced-degradation caused by TID or DD will be completely different.

In addition to the cumulative effect, transient event can occur at any time while the system is under radiation. If the component is qualified for operation in a radiative environment, it means that all the necessary tests were already performed and proves that the component should resist to the transient radiation effect. However, this is not true for component already irradiated. As presented before, the different work performed by N. Roche and F. Roig have shown that depending on the accumulated dose of an electronic component, its response to transient effect may not corresponds to what it was qualified for. Indeed, because of several reasons such as the modification of the physical parameters, the increase of the leakage current, etc. the components do not react as there were expected to. Therefore, it is important to study the synergistic effect caused by both types of radiation effects in order to be able to anticipate the evolution of their response over time.

The work presented in this manuscript describes two different work performed linked to the synergistic effects. In the next chapter, the study of bipolar operational amplifiers is investigated. Some results produced by F. Roig left an unexplained response of one operational amplifier from one specific manufacture without any explanation. Therefore, the next chapter presented the complete investigation on those operational amplifiers and causes of the unexpected behavior is explained. In the following chapters, the question of the resistance of ESD protection structure to TID was investigated. Being nowadays implemented in all electronic devices, the potential failure of this structure would be catastrophic for a system. Those structures designed to protect a device from ESD stress could become inefficient after irradiation. Thus, a complete investigation of those structures was performed and the results are presented.

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II.1. INTRODUCTION

Electronics in spacecraft missions are subject to cumulative effects such as the Total Ionizing Dose (TID) and the Displacement Damage (DD). These effects will alter the electrical and functional parameters of the components [1]. Usually, the parameters observed during radiation testing are the positive (I_{CCP}) and negative supply bias current (I_{CCN}), the open loop gain (OLG), the slew rate (SR), the input bias currents (I_{INP} and I_{INM}), the input offset voltage (V_{OS}) and the input offset current (I_{OS}), which are all sensitive to both TID and DD. In many cases, the observed response is not only driven by the degradation of single transistors, but also by circuit effects consisting in the compensation or the enhancement of the degradation of a stage/transistor by the degradation of another stage/transistor. Barnaby *et al.* [2] and Dusseau *et al.* [1] have extensively studied circuit effects in linear devices and comparator devices. In previous papers, Roig *et al.* highlighted the influence of circuit design modifications [3]–[5] on LM124s from three different manufacturers. Indeed, modifications such as an increased value of the current biasing the amplification stage or the suppression of the current sources biasing the input common collector stages directly affect the operational amplifier radiation-induced degradation.

This second chapter aim at showing how a physical mechanism, i.e. the DD induced degradation at transistor level in an integrated circuit may cause an unexpected response at circuit level and how this effect may be amplified due to a slight modification in the design. This work refers to a DD test campaign, which has been led on LM124 operational amplifiers from three different manufacturers. Previously carried out, reported in [3], [5], the analyzes is mainly performed from the TID and design points of view. The present paper focuses on DD results that lead to an unexpected rebound-like behavior of the slew rate degradation of one of the tested components. These results are investigated and the root causes of this unusual phenomenon are presented in the following sections.

To start with, the first part of this chapter is dedicated to present the previous work performed by Fabien Roig's Ph.D. program [6]. Part two of this chapter focuses on the presentation of the internal electrical schematic of the LM124 operational amplifier and its overall functioning. In this part, an analysis at system level is performed and different degradation scenarios are presented theoretically and by simulation. To conclude, different analysis and measurements are performed with microphotography of LM124 from different manufacturers. The differences noted in the design of the three die layouts and their impact on the degradation is explained. Finally, the unusual shape of the radiation-induced degradation curve and its origin is explained.

II.2. PRESENTATION OF THE PREVIOUS RESULTS

II.2.1. PRESENTATION OF THE PREVIOUS RESEARCH

The following study is based on the experimental results obtained during Fabien Roig's Ph.D. program. Part of his work was aimed at studying the impact of the differences observed in the design of COTS linear operational amplifier LM124 from three manufacturers. The different parameters studied were the positive (ICCP) and negative supply bias current (ICCN), the open loop gain (OLG), the slew rate (SR) and the input bias currents (IINP and IINM). Those parameters are all known to be sensitive to TID and DD [7].

As presented in chapter I, several radiation-induced effects may lead to the degradation of an electronic component (i.e. the cumulative effects and the transient effects). All over the years, many qualification standards were developed to ensure a proper selection of the electronics components for space applications. Nonetheless, those standards are also used for others types of applications (Nuclear power plants, Accelerators etc.). Table II.2-1 summarizes the main qualification tests standards currently used.

Table II.2-1: Current qualifications test standards for space applications [8]

Standard	Reference	Revision date	TID	DD	SEE ¹
ESCC ² 22900-5	[9]	June 2016	X		
ESCC 25100-2	[10]	October 2014			X
MIL-STD ³ 883K Method 1019.9	[11]	February 2017	X		
MIL-STD 883K Method 1017.3	[12]	February 2017		X	
MIL-STD 750F Method 1017.1	[13]	August 2016		X	
MIL-STD 750F Method 1019.5	[14]	August 2016	X		
MIL-STD 750F Method 1080.1	[15]	August 2016			MOSFETs Heavy ions
EIA JESD ⁴ 57A	[16]	November 2017			Heavy ions

As observed in Table II.2-1, among all the standards, the different radiation-induced effects are all treated separately. For example, the qualification tests for single event effect (ESCC 25100-2 and EIA

¹ SEE : Single Event Effect

² ESCC: European Space Component Coordination

³ MIL-STD: US Military Standards

⁴ EIA JESD: Electronic Industries Association / JEDEC Standards

JESD57A) recommend a test with a particle accelerator with a non-irradiated electronic component. Therefore, the separate treatment of those effects raises a question on the effect of a synergistic effect between two different radiation-induced effects. Moreover, if a transient effect appeared on an electronic component after it has already accumulated a high dose, how would the component react and affect a full system?

The objective of the work lead by F. Roig was to investigate if a synergistic effect between a natural cumulative effect and a natural transient effect could appear and if it could lead to an overestimation or an underestimation of the degradation. In this work, two synergistic effects were investigated: the synergistic effect TID-ASET⁵ and the synergistic effect DDE⁶-ASET.

With these studies, TID and DD irradiation campaigns were performed. However, due to the very large amount of highly interesting data collected, it was not possible to analyze all the results in the framework of a single Ph.D. Thesis. In particular, DD causes an unexpected degradation on some devices that remained unexplained at that time. The present works aim at explaining those effects and close all the actions left behind in the previous work. All the details of the tests campaigns will be presented in the following section.

II.2.2. PRESENTATION OF THE EXPERIMENTS PERFORMED

II.2.2.1 Devices under test

The devices under test (DUTs) used during these irradiation campaigns are commercial off-the-shelf (COTS) LM124 operational amplifiers from three different manufacturers. In order to estimate the discrepancy in the design between those components, a reverse engineering process and an analysis of the die layout were performed by THALES TCS on the three LM124. Table II.2-2 summarize the components selected as DUT used for the study.

Table II.2-2: Summary of the different DUTs used for the study

Label	LM124-NS [17]	LM124-TI [18]	LM124-ST [19]
Components	Opamp - LM124	Opamp - LM124	Opamp - LM124
Manufacturer	National Semiconductor (NS)	Texas instruments (TI)	STMicroelectronics (ST)
Date code	JH148AB	2B-S 1225B	6411809A vb 64
Design year	N.R.	1995	2001
Technology	Bipolar	Bipolar	Bipolar
Packaging	Ceramic DIP 14	Ceramic DIP 14	Plastic DIP 14

⁵ ASET : Analog Single Event Transient

⁶ DDE : Displacement Damage Effect

II.2.2.2 Experimental details

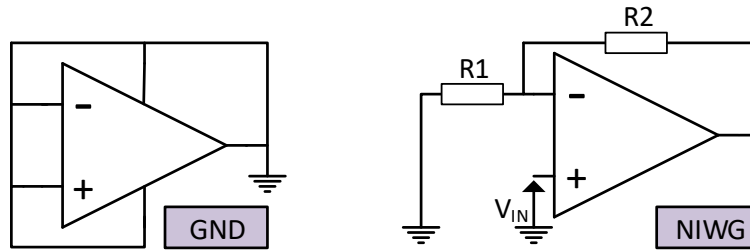


Figure 19: LM124 operational amplifier in all pins grounded configuration and Non-Inverter With Gain (NIWG) configuration. The value of the resistor are $R1 = 1k\Omega$ and $R2 = 10k\Omega$ and the gain of the NIWG configuration is +11.

II.2.2.2.1 Total Ionizing Dose irradiation

TID experiments were performed at TRAD (Toulouse, France) using ^{60}Co γ -rays source [20]. The dose rate was $10 \text{ mrad}_{(\text{Si})}.\text{s}^{-1}$ and the total dose delivered was $50 \text{ krad}_{(\text{Si})}$. The parts were irradiated in two different configurations, all pins grounded (GND in Figure 19) and non-inverter with a gain of 11 (NIWG in Figure 19). In this study, only the GND configuration is investigated.

It is generally assumed that an irradiation with all pins grounded is considered as the worst case, but as shown in [21]–[23], this is not always the case. In their previous work, Gonzalez Velo *et al.* [23] have shown the impact of the bias configuration by running tests on a COTS LM124 operational amplifier. Those tests highlighted the fact that not all of the parameters of a linear device see their sensitivity increase when grounded. Indeed, TID tests have shown that grounded components see their input bias current sensitivity decrease. This phenomenon is explained by the fact that if an irradiation performed all pins grounded maximizes the degradation of all transistors; it may also maximize the compensation mechanisms at circuit level. However, in our case, only the I_{CCP} , SR and OLG are studied, so the GND configuration is considered as the worst case for these parameters.

II.2.2.2.2 Displacement Damage Dose irradiation

DD experiments were performed at the PROSPERO fission reactor (CEA⁷, Valduc, France) using 1 MeV equivalent neutrons. A study of this fission reactor was performed by Azais *et al.*, and is presented in [24]. Two fluences were investigated, $1.10^{12} \text{ n.cm}^{-2}$ and $5.10^{12} \text{ n.cm}^{-2}$ (maximum cumulated level). The parts were irradiated in GND configuration.

II.2.2.3 Experimental results

Experimental results presented in Figure 20 through Figure 25 are extracted from the Ph.D. manuscript of F. Roig [6] and have already been published and discussed in [3] and [5]. Those results were used to

⁷ CEA: French Alternative Energies and Atomic Energy Commission

investigate the impact of the difference in the design of the three LM124 from different manufacturers, and to analyze the resulting radiation-induced degradations.

Results of the TID irradiation campaign:

Figure 20, Figure 21, and Figure 22 respectively depict the degradation of I_{CCP} , SR, and OLG observed during ^{60}Co experiments. It represents the average value of electrical parameters obtained from five samples per manufacturer in GND configuration. The error bars represent the minimum and maximum values obtained during the different tests.

As presented in those figures, the LM124-TI shows a quasi-insensitivity against TID. Indeed, none of its parameters strongly degrades. A variation of $41.6\mu\text{A}$ over $922.7\mu\text{V}$ is observed for I_{CCP} (4.51%) after $50\text{ krad}_{(\text{Si})}$. The SR itself degrades by 8.8% and the OLG by 5.5%. In comparison, the other manufacturers show a higher degradation. The LM124-NS shows a relatively strong degradation of 46.5% for the I_{CCP} , 91% for the SR and 92% for the OLG. Regarding the LM124-ST, degradation with a higher sensitivity is observed. Indeed, after irradiation, we obtain a diminution of 60% of I_{CCP} , 60% for the SR and 99.9% for the GBO.

To conclude on those results, whatever the degradation, all of the manufacturer's parts have their parameters (the SR and the OLG) following the same trend of degradation as the I_{CCP} .

Results of the DD irradiation campaign:

Figure 23, Figure 24, and Figure 25 respectively show the degradation of I_{CPP} , SR and OLG observed during the 1 MeV equivalent neutron experiments. They present the average value of electrical parameters obtained with eight samples per manufacturer in GND configuration. The error bars represent the minimum and maximum values obtained during the different test.

As presented in those figures, the LM124-NS and LM124-TI show a similar degradation of their parameters whereas the LM124-ST shows a larger degradation. Indeed, for a dose of $5.10^{12}\text{ n.cm}^{-2}$ a variation of ΔI_{CPP} for $146\mu\text{A}$ (22.3%) and $155\mu\text{A}$ (25.7%) respectively for LM124-NS and LM124-TI was observed. However, for LM124-ST, a degradation of $378\mu\text{A}$ (33%) for the ΔI_{CPP} was observed. Regarding the OLG, the trend of the degradation is similar for the LM124-NS and for the LM124-TI, whereas the LM124-ST show a more significant degradation trend. Concerning the SR, the same trend of degradation is observed for the LM124-NS and for the LM124-TI, while the LM124-ST show a different degradation.

Results obtained with TID irradiation:

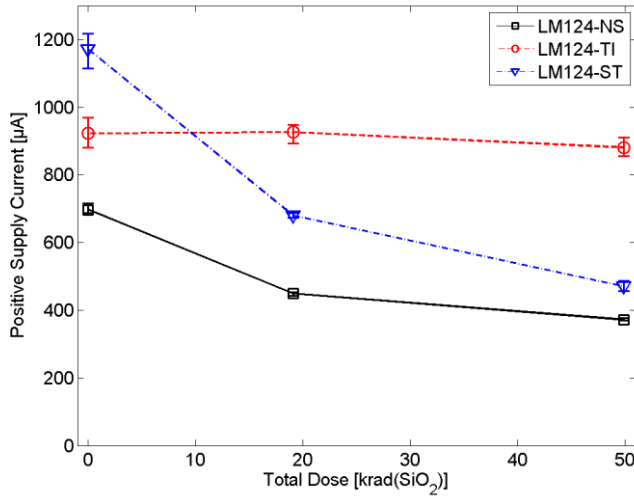


Figure 20: Degradation of the current consumption of three LM124 operational amplifiers from different manufacturers (LM124-NS, LM124-TI, and LM124-ST) irradiated with ^{60}Co in GND configuration [3]. The dose rate is $10 \text{ mrad}_{(\text{Si})} \cdot \text{s}^{-1}$

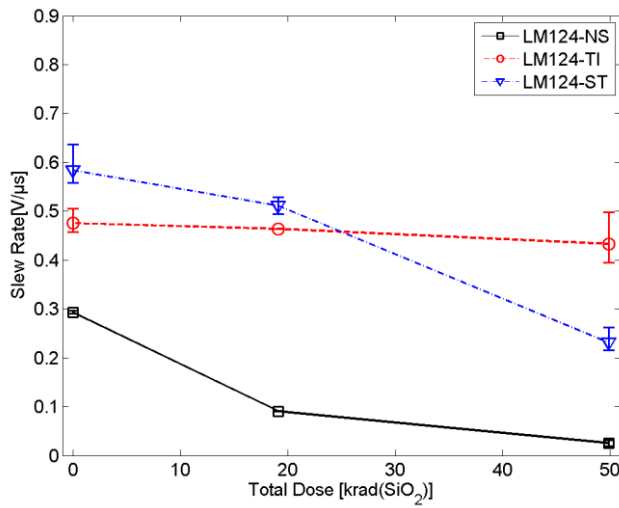


Figure 21: Degradation degradation of the slew rate of three LM124 operational amplifiers from different manufacturers (LM124-NS, LM124-TI, and LM124-ST) irradiated with ^{60}Co in GND configuration [3]. The dose rate is $10 \text{ mrad}_{(\text{Si})} \cdot \text{s}^{-1}$

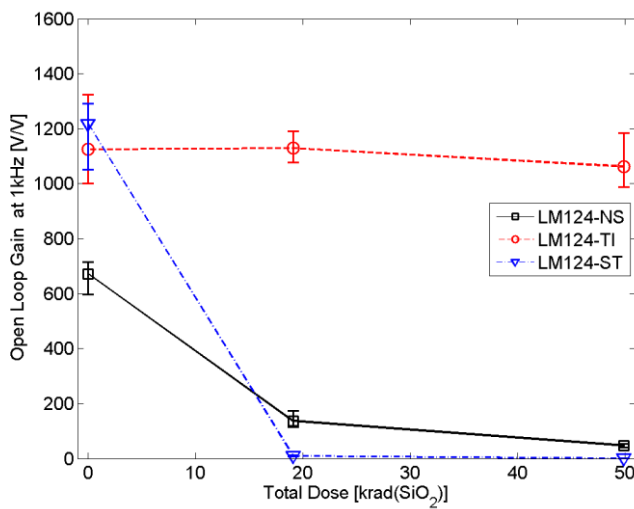


Figure 22: Degradation of the open loop gain of three LM124 operational amplifiers from different manufacturers (LM124-NS, LM124-TI, and LM124-ST) irradiated with ^{60}Co in GND configuration [3]. The dose rate is $10 \text{ mrad}_{(\text{Si})} \cdot \text{s}^{-1}$

Results obtained with DD irradiation:

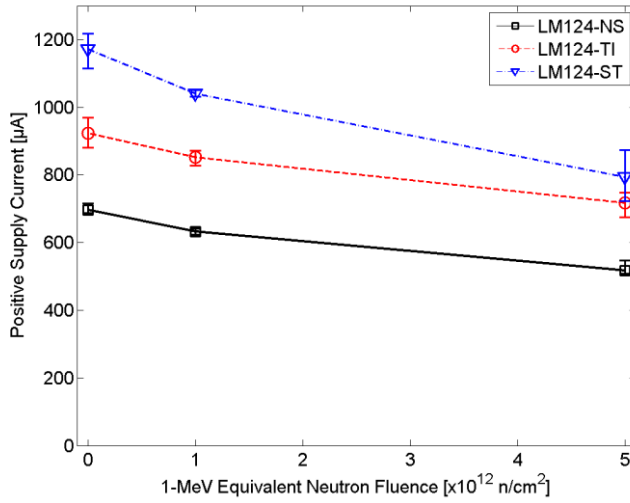


Figure 23: Degradation of the current consumption of three LM124 operational amplifiers from different manufacturers (LM124-NS, LM124-TI, and LM124-ST) irradiated with 1-MeV neutron equivalent in GND configuration [5].

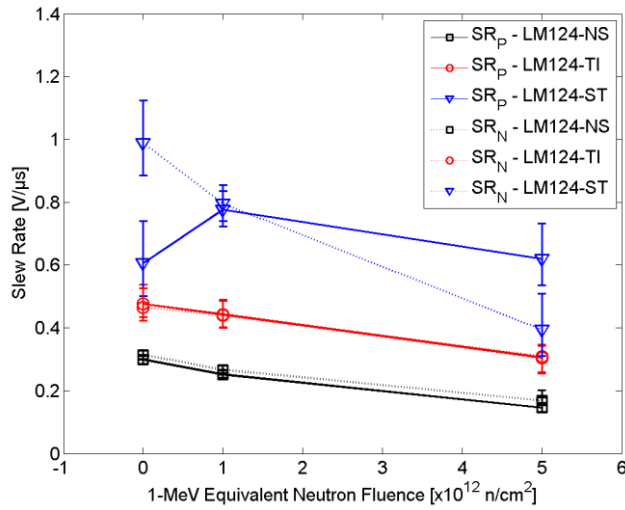


Figure 24: Degradation degradation of the slew rate of three LM124 operational amplifiers from different manufacturers (LM124-NS, LM124-TI, and LM124-ST) irradiated with 1-MeV neutron equivalent in GND configuration [5].

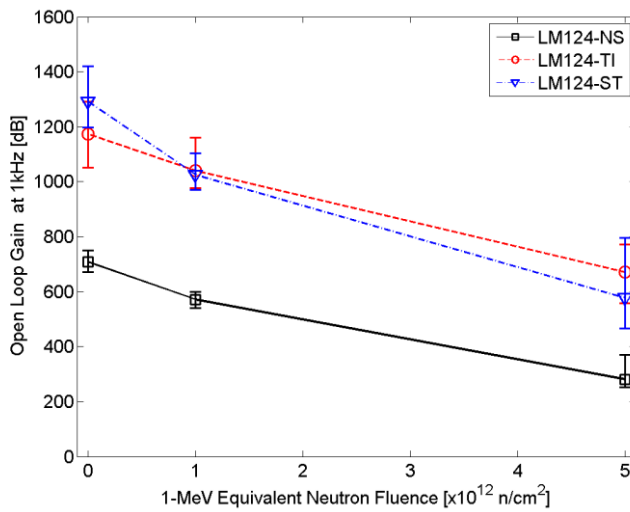


Figure 25: Degradation of the open loop gain of three LM124 operational amplifiers from different manufacturers (LM124-NS, LM124-TI, and LM124-ST) irradiated with 1-MeV neutron equivalent in GND configuration [5].

II.2.3. PROBLEMATIC

II.2.3.1 Unexpected degradation of the slew rate

As presented in [5] and [1], radiation induced-degradation on current sources leads to a decrease in the supply current either with TID or DD. This phenomenon is typical of the degradation of the current mirror with irradiation [1]. On the LM124-NS and LM124-TI, the slew rate degrades proportionally with respect to the supply current. However, on the curve of Figure 24, the slew rate of the LM124-ST exhibit an unusual degradation. Indeed, not only does the degradation show no decrease at a dose of 5.10^{12} n.cm⁻² compared to its pre-irradiation value, but it also increases significantly for a dose of 1.10^{12} n.cm⁻².

This behavior suggests that additional mechanism is at play for the DD degradation in the LM124-ST. In order to understand where this phenomenon comes from, an analysis at circuit level was performed. The following section presents the internal electrical schematic of the LM124 component. Then, a description of the slew rate mechanism, followed by a listing of the different degradation hypothesis yielded by the analysis.

II.3. CIRCUIT LEVEL ANALYSIS

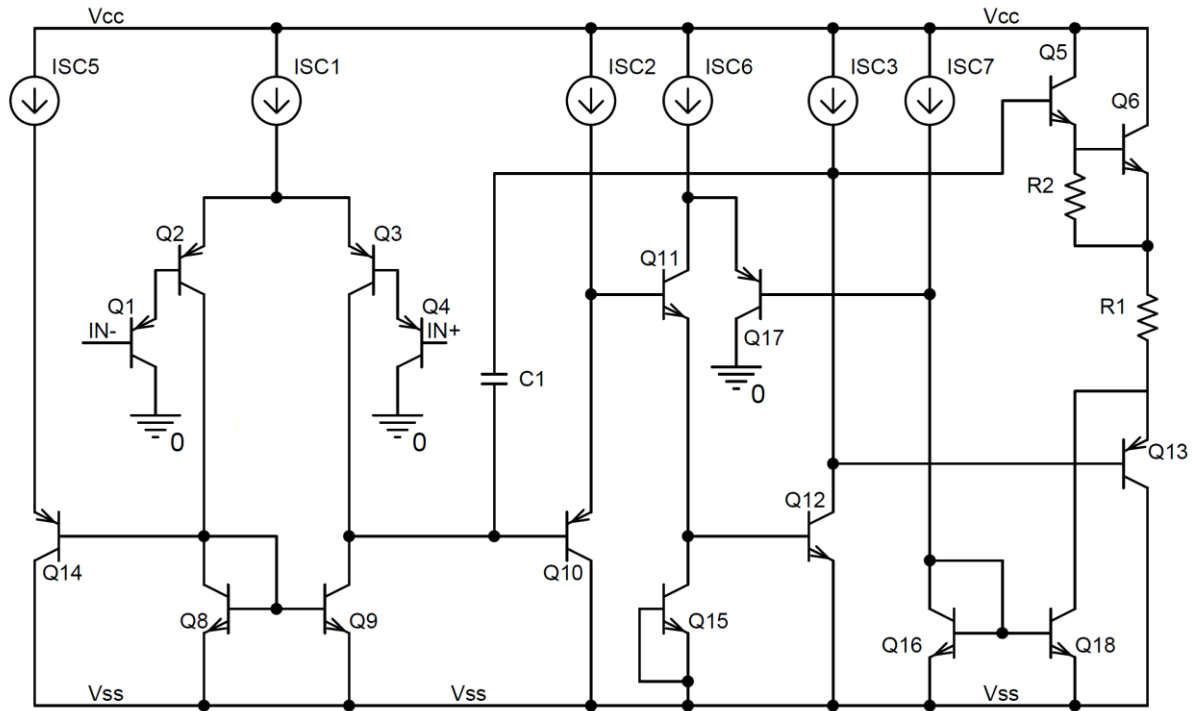


Figure 26: Simplified internal electrical schematic of the LM124

II.3.1. DESCRIPTION OF THE INTERNAL ELECTRICAL SCHEMATIC OF THE LM124

Figure 26 presents the simplified electrical schematics of the three LM124s. This schematic can be decomposed into three different parts that are **the differential stage**, **the amplification stage**, and **the output stage**.

II.3.1.1 The differential stage

The differential stage (or differential pair) is the most important part of an operational amplifier. It is used to measure the difference between the positive input voltage and the negative one (named after IN+ and IN- in Figure 26). In Figure 26, the differential pair is composed of the transistors Q1 to Q4, used as input transistor, and the transistors Q8 and Q9 used as a current mirror. A current mirror is a structure mainly used in analogic electronics. It is designed to copy a current through an active device by controlling the current in another active device of the circuit, keeping the output current constant regardless of the load. In our case, I_{C8} corresponds to the reference current and I_{C9} as the driven current. This means that at any time, $I_{C8} = I_{C9}$.

When the same voltage is applied on IN- and IN+, all the transistors are switched on and the current delivered by I_{SC1} equitably shares between the negative branch and the positive branch. In this case, we

can consider that $I_{E2} = I_{E3} = \frac{I_{SC1}}{2}$. At this moment the reference current $I_{C8} = I_{SC1} \div 2$, and because I_{C8} is the reference current, $I_{C9} = I_{SC1} \div 2$. At the end, there is no current goes out of the differential pair, and the output of the component stays at 0V.

When IN^- has a higher voltage than IN^+ , the transistors Q1 and Q2 are switched off, while the transistors Q3 and Q4 stays switched on. Therefore, the current delivered by I_{SC1} goes directly into the positive branch. At this moment, because the transistor Q2 is switched off, the reference current $I_{C8} = 0A$ and the current driven by the current source is also equal at 0A. In this case, all the current supplied by I_{SC1} starts first to load the capacitor C1 that was previously discharged, and the stage of the transistor will then switch to turn the output at the lower voltage of the operational amplifier.

When IN^- has a lower voltage than IN^+ , the transistors Q1 and Q2 stays switched on, while the transistors Q3 and Q4 are switched off. Therefore, the current delivered by I_{SC1} goes directly into the negative branch. At this moment, the reference current $I_{C8} = I_{SC1}$, and because I_{C8} is the reference current, $I_{C9} = I_{SC1}$. Because no current is passing through the transistor Q3, if the capacitor C1 was previously charged, it will discharge through Q9, and the stage of the transistor will then switch to turn the output at the higher voltage of the operational amplifier.

II.3.1.2 The amplification stage

The amplification stage is used to amplify the current going out of the differential stage. It is composed of the transistors Q10 to Q12 and Q15. At first, the transistor Q10 is a simple common emitter. Because of its high impedance input, it does not affect the equilibrium of the differential stage. The transistors Q11 and Q12 are then two common collectors, used to amplify the signal.

II.3.1.3 The output stage

The push-pull output stage constituted by Q6 and Q13 is used as a current buffer for the output of the component. It is endowed with a current protection not represented on the schematics. Because the output signal of the amplification stage is not able to drive a large amount of current, the structure created by the transistors Q5 in a Darlington configuration with Q6 is used to increase the input resistance of the stage and thus, avoid to lower the gain of the previous stage [25]. The transistors Q16 and Q18 are used as a current mirror to equilibrate the output voltage.

II.3.2. DESCRIPTION OF THE SLEW RATE MECHANISM

The slew rate corresponds to the maximum slope of the output signal that can be achieved by the component. As presented in Figure 27, it is measured by applying a square wave to one of the input terminals and recording the slope of the output signal during the linear slope. It is expressed in V/ μ s and is caused by the charge of the compensation capacitor, named C_1 in Figure 26.

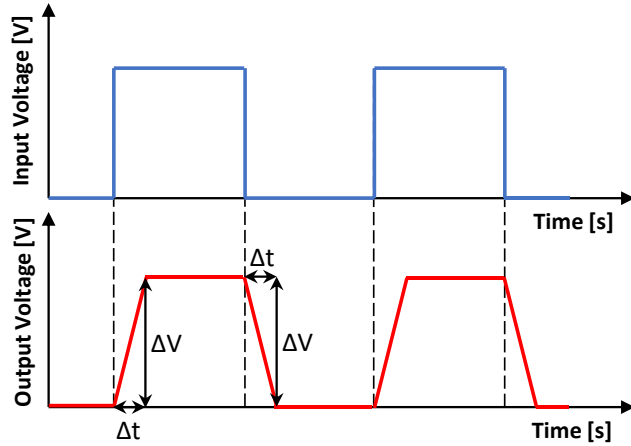


Figure 27: Presentation of the slew rate mechanism

In all the operational amplifiers, two different slew rates can be considered, such as the positive slew rate and the negative slew rate. Depending on if, the capacitor is charging or the discharging, the current will not take the same path and the resultant slew rate will not be the same.

II.3.2.1 The positive slew rate:

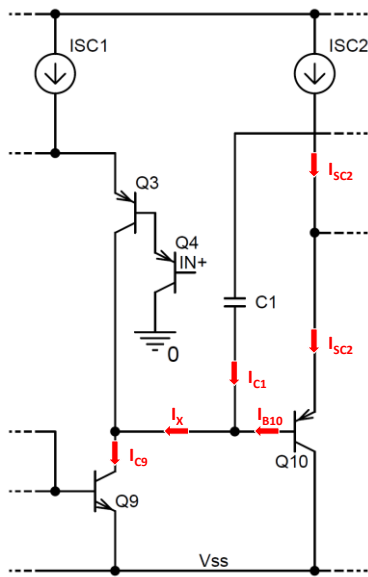


Figure 28: Part of the simplified internal electrical schematic presented in Figure 26 showing the current path of the positive slew rate

When the output switches from a low-level output state to a high-level output state, just before the process of commutation, the capacitor C_1 is fully charged. When the commutation starts, the capacitor begins to discharge. Because the discharges current is driven by the current source of the differential pair, the current discharging I_{C1} is limited by the current I_{B10} . At this moment, the positive slew rate can be described as following:

$$SR_P = I_{C9}/C_1 \quad \text{Equation II.3-1}$$

$$SR_P = (I_{C1} - I_{B10})/C_1 \quad \text{Equation II.3-2}$$

$$SR_P = \left(I_{C1} - \frac{I_{SC2}}{\beta_{10}} \right) / C_1 \quad \text{Equation II.3-3}$$

However, as explained before, the factor β of a pristine transistor is often not lower than 100. Thus, as long as the current gain of the transistor Q_{10} stays high enough, the current I_{B10} can be neglected compared to the value of I_{C1} . The equation of the slew rate can then be simplified as presented in the following equation:

$$SR_P = I_{SC1}/C_1 \quad \text{Equation II.3-4}$$

II.3.2.2 The negative slew rate:

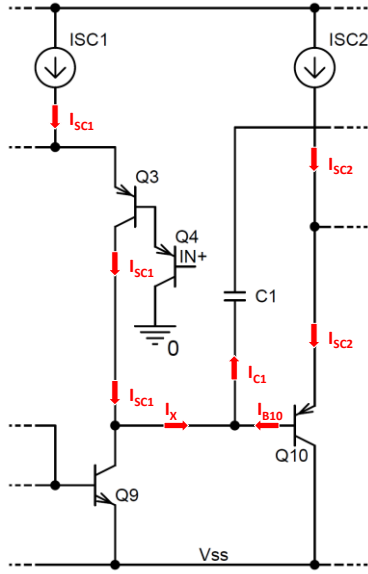


Figure 29: Part of the simplified internal electrical schematic presented in Figure 26 showing the current path of the negative slew rate

When the output switches from a high-level output state to a low-level output state, just before the process of commutation, the capacitor C_1 is empty. When the commutation starts, the capacitor begins to charge, with the current coming from I_{SC1} and the one coming from I_{SC2} divided by the β_{10} ⁸ factor. At this moment, the negative slew rate can be described as following:

$$SR_N = I_{C1}/C_1 \quad \text{Equation II.3-5}$$

$$SR_N = (I_{SC1} + I_{B10})/C_1 \quad \text{Equation II.3-6}$$

$$SR_N = \left(I_{SC1} + \frac{I_{SC2}}{\beta_{10}} \right) / C_1 \quad \text{Equation II.3-7}$$

However, for a pristine transistor, the factor β is often not lower than 100. Thus, as long as the current gain of the transistor Q_{10} stays high enough, the current I_{B10} can be neglected compared to the value of I_{SC1} . The equation of the slew rate can then be simplified as presented in the following equation :

$$SR_N = I_{SC1}/C_1 \quad \text{Equation II.3-8}$$

The equations (II.4) and (II.8) demonstrates that during irradiation, as the current from the current sources decreases; the slew rate is bound to decrease [26]. However, on the LM124-ST, the SR increases as observed in Figure 24 until the fluence reaches $1.10^{12} \text{ n.cm}^{-2}$, and then slightly decreases down to the fluence of $5.10^{12} \text{ n.cm}^{-2}$. According to (II.4) and (II.8), this phenomenon may be caused either by the current, which increases or by a decrease in the capacitor value.

Let us first examine the latter hypothesis. As we know, the capacitor value is not supposed to decrease during the irradiation. However, before irradiation, we can observe on the curves Figure 21 and Figure 24 that the values of the slew rate of the pristine device LM124-ST is higher than the slew rate of devices LM124-NS and LM124-TI.

Section II.3.3 presents the different degradation scenarios that were considered.

⁸ β_{10} = current gain factor of the transistor Q_{10} .

II.3.3. DEGRADATION SCENARIOS

II.3.3.1 The increase of the base current of Q10

As explained before, the slew rate is directly linked to the current source named I_{SC1} in Figure 26 used to bias the differential stage. If I_{SC1} decreases, the slew rate should decrease according to (II.4) or (II.8). In our case, we observe the opposite phenomenon. Instead of following the current source degradation that decreases, the slew rate increases. The only possible explanation for the observed increase in the slew rate is that the current injected in C_1 is no longer composed of I_{SC1} only. Considering the node at the C_1 input terminal, this current can only come from the base of Q10, which was previously neglected because of its low value on a pristine component.

The transistor Q10 is used to increase the amplification stage input impedance. In our case, Q10 is biased by the current source I_{SC2} . Some papers show that the radiation-induced current decrease of the current sources is not linear [1], [2]. Therefore, the first degradation observed on Q10 is an increase of its base current. This increase adds a new contribution to the current charging the capacitor and thus increases the slew rate until I_{SC2} itself degrades which will eventually decrease the slew rate.

Moreover, as presented in [3], F. Roig *et al.* showed that all parameters of the LM124-ST (including slew rate and open loop gain) are twice that of LM124-NS and 1.33 times higher than LM124-TI. According to this, the current source I_{SC2} should be greater for the LM124-ST than for the other devices, and so, the base current of Q10 should be more important for the LM124-ST.

In order to determine which impact would, the increase of the base current of the transistor Q10 have on the final slew rate, PSPICE simulations were performed using the software OrCAD Capture CIS - PSpice lite.

As already understood and presented in the first chapter, radiation-induced degradation on bipolar component usually degrades the current gain of the transistor. Thus, to simulate the effect of radiation with PSPICE, the gain of the transistor can be modified and as presented in [1], because the collector of the transistor is bound to the value of the current source I_{SC2} , the base current of the transistor Q10 will increase. Table II.3-1 summarizes the main parameters used during the simulation. Three values of the current source I_{SC2} were used to increase the range of the base current increase.

Table II.3-1: This table presents the different values taken for the PSPICE simulations of the increase of the base current of the transistor Q10

Parameter name	Current source I_{SC1}	Current source I_{SC2}	Current gain β_{10}
Value	6 μ A	4 μ A ; 6 μ A ; 8 μ A	From 100 to 1

Figure 30 presents the variation of the slew rate depending on the value of the base current of the transistor Q10. Those results were extracted from simulations using the electrical schematic presented

in Figure 26. The two slew rates are represented in this graphic, corresponds to the positive slew rate in continuous orange line and the negative slew rates in dashed blue line (see II.3.2). As we can observe on this graphic, both rising and falling slew rate are impacted by the increase of the base current of the transistor Q10 in a symmetrical way.

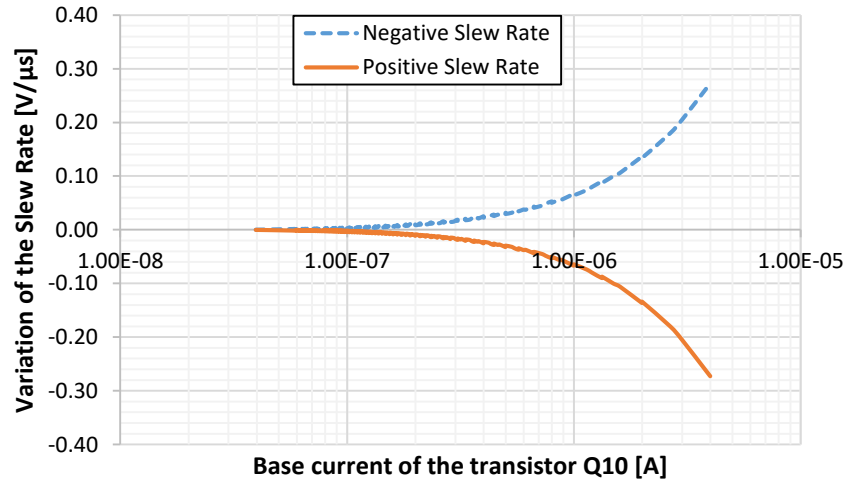


Figure 30: Variation of the positive and negative slew rate depending on the value of the base current of the transistor Q10

If we take for example an increase of the base current of Q10 up to $1\mu\text{A}$, the positive slew rate would increase of $0.08\text{ V}/\mu\text{s}$ and the negative one would decrease of $0.08\text{ V}/\mu\text{s}$. However, those values correspond to simulations performed with a theoretical model, depending on the parameters of all the component in the electrical schematics, presented in Figure 26, the result may differ. However, it gives a good indication of the radiation-induced degradation of the real components.

It is known that if a transistor is very sensitive to TID and DD, the value of its current gain may drop down to 1. In this case, the effect on the slew rate would be critical. For example, a difference of $4\mu\text{A}$ between the current sources would lead to an addition of $4\mu\text{A}$ when the component is completely degraded. Thus, the impact on the slew rate would be critical, because, as seen in Figure 30, such increase would lead to a variation of $0.3\text{V}/\mu\text{s}$. This point highlights the importance of the ratio between the current sources I_{SC1} and I_{SC2} that have to be properly designed.

II.3.3.2 Disequilibrium of the current source values

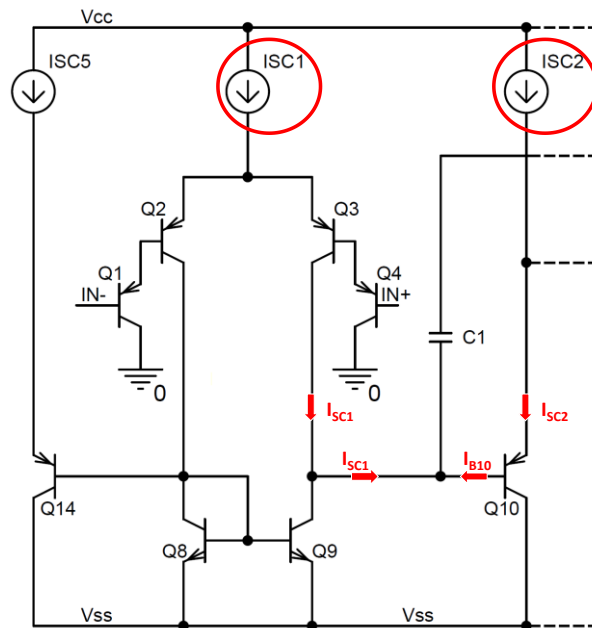


Figure 31: This schematic is a part of the electrical schematic of the LM124 presented in Figure 26. It presents the differential pair of the LM124 and current path during the commutation of the positive slew rate. This picture shows the importance of the ratio of I_{SC1} and I_{SC2} when the component degrades with TID or DD.

Another point in this electrical schematic is the ratio between the current source I_{SC1} and I_{SC2} as presented in Figure 31. Indeed, as mentioned in the previous paragraph, the impact of an increase in the base current of the transistor Q10 is a decrease in the value of the positive slew rate and an increase in the value of negative slew rate (see Figure 30). Because TID and DD affect the current gain of the transistor Q10 depending on the ratio between the current sources I_{SC1} and I_{SC2} , the impact may important:

Case 1:	Case 2 :	Case 3:
If $I_{SC1} \gg I_{SC2}$: Low impact	If $I_{SC1} \approx I_{SC2}$: High impact	If $I_{SC1} \ll I_{SC2}$: Important impact

In order to visualize the importance of this ratio, Figure 32 presents the variation of the positive slew rate (PSR) and negative slew rate (NSR), for three different values of the current sources I_{SC1} and I_{SC2} , corresponding to three different ratios. For the three different simulations, the current I_{SC1} was kept constant.

Table II.3-2: This table presents the different values taken for the PSPICE simulations to observe the importance of the ratio between the current source I_{SC1} and I_{SC2}

Parameter name	Current source I_{SC1}	Current source I_{SC2}	Ratio I_{SC1}/I_{SC2}	Current gain β_{10}
Value	6 μ A	4 μ A ; 6 μ A ; 8 μ A	1.5 ; 1 ; 0.75	From 100 to 1

Table II.3-2 summarizes the main values of the current sources used for the simulation. These values were selected to show the importance of the difference between the values of the current sources I_{SC1} and I_{SC2} , by testing three different ratios. For these simulations, the current gain of the transistor Q10 was swept from $\beta_{10} = 100$ (for a pristine component) down to $\beta_{10} = 1$ (for a completely degraded component).

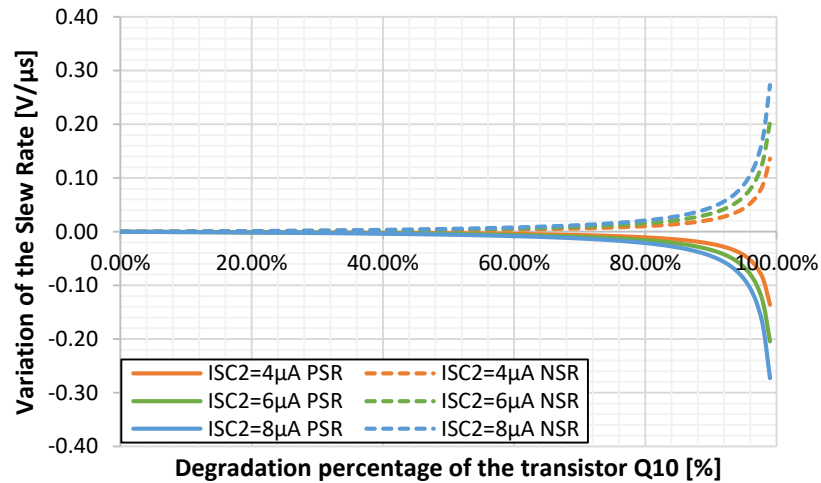


Figure 32: Variation of the positive slew rate (PSR) and negative slew rate (NSR) depending on the current sources I_{SC1} and I_{SC2} . All the simulations were performed with a constant current I_{SC1} of $6\mu A$.

Figure 32 presents the variation of the positive slew rate (PSR) and negative slew rate (NSR) depending on the degradation percentage of the transistor Q10. It is composed of three different curves representing different values of the current sources I_{SC1} and I_{SC2} . The point of this simulation is to show that depending on the ratio between the current sources I_{SC1} and I_{SC2} , the resultant degradation of the slew rate may be different. As observed on these curves, for a ratio of 1.5 ($I_{SC1} = 6\mu A$ & $I_{SC2} = 4\mu A$), represented by the orange color, the degradation of the transistor Q10 does not greatly affect the slew rate, compared to the case with the ratio of 0.5 ($I_{SC1} = 6\mu A$ & $I_{SC2} = 8\mu A$) represented by the blue curves. This higher degradation is explained by the base current of the transistor, which is higher because the current source I_{SC2} is higher.

However, by taking a closer look in Figure 26, another structure appears to be similar than the one around the transistor Q10. Indeed, the transistor Q14, connected to the negative branch of the differential pair, is similar to the transistor Q10 that is connected to the positive branch of the differential pair. Therefore, the degradation the transistor Q14 may add another contribution to the slew rate variation.

II.3.3.3 Disequilibrium of the regulation pair (Q10-Q14)

The structure formed by the transistors Q10 and Q14 is used to compensate any variation of the differential pair that would be induced by the temperature or by its leakage current. As presented in

Figure 33, in order to ensure a perfect equilibrium of the differential pair, the transistors Q8 and Q9 must be designed the same way to have the same amount of current driven by the current mirror, which will ensure a proper parallelism in the two branches. Therefore, because the base Q10 and Q14 are respectively connected to the collector of Q9 and Q8, they should have must have the same design. Therefore, after degradation, they should have the same leakage current, which will balance each other out.

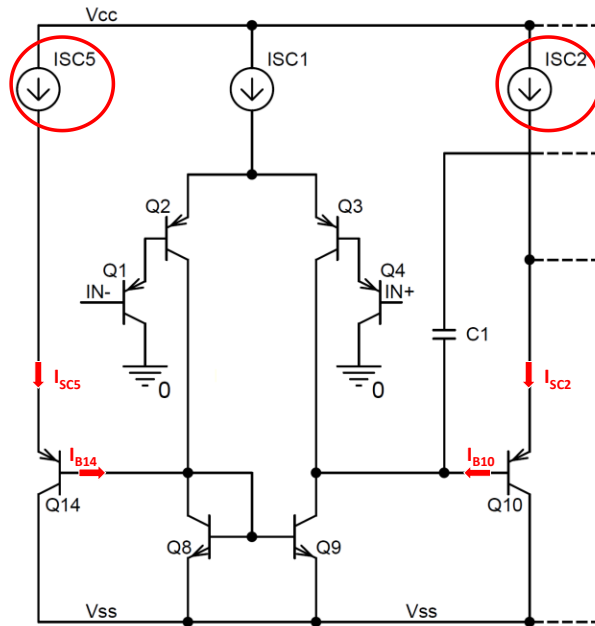


Figure 33: This schematic is a part of the electrical schematic of the LM124 presented in Figure 26. It presents the differential pair of the LM124 and the compensation structure. The current of the compensation structure formed by the transistors Q10 and Q14 are highlighted by red arrows.

In our case, when the transistors Q10 and Q14 degrade, if their current sources, known respectively as I_{SC2} and I_{SC5} , differ, the difference of current leakage will lead to a disequilibrium for the differential pair, and consequently, the SR will be impacted.

However, if we consider that, the transistors Q10 and Q14 have the same degradation, depending on the value of the current sources I_{SC2} and I_{SC5} , a different variation of the slew rate will occur.

Figure 34 presents the variation of the positive and negative slew rate depending on the value of the current sources I_{SC2} and I_{SC5} . Three different simulations cases are presented in this graphic, representing three different scenarios covering all the possible situations:

- The case of a positive disequilibrium: The value of the current source $I_{SC2} > I_{SC1}$, represented in orange;
- The case of an equilibrium = The value of the current source $I_{SC2} = I_{SC1}$, represented in green;
- The case of a negative disequilibrium: The value of the current source $I_{SC2} < I_{SC1}$, represented in blue;

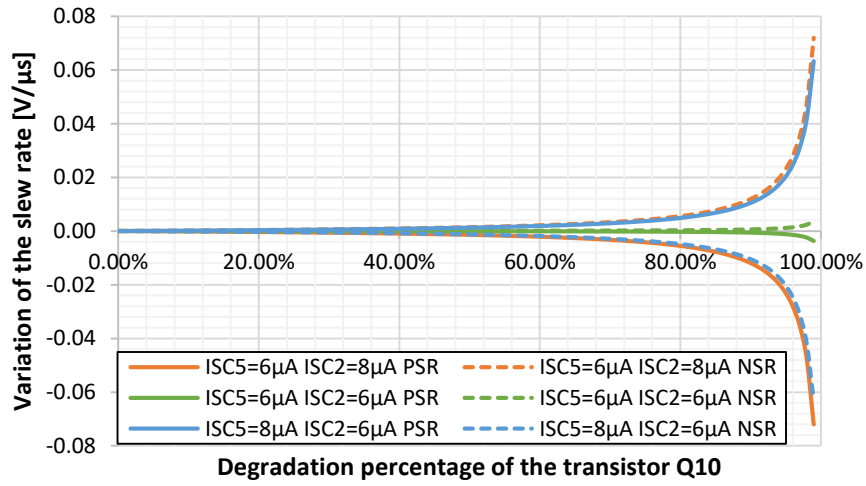


Figure 34: Variation of the positive slew rate (PSR) and negative slew rate (NSR) depending on the current sources I_{SC2} and I_{SC5} . All the simulations were performed with a constant current for I_{SC1} of $6\mu A$. This graphic show the disequilibrium of the pair of transistor Q10 and Q14.

Compared to the previous simulation, where the degradation of Q14 was not taken into account, if the current sources I_{SC2} and I_{SC5} have the same value and Q10-Q14 the same degradation, the increase of the base current of the transistors Q10 and Q14 will be the same. In this case, the base current of the transistor Q14 will be added at the current reference of the current mirror increasing the current I_{C9} . Thus, the current of the base of Q10 will be dragged by Q9. Therefore, both leakage currents will be compensated and no degradation will be observed. However, if the current sources I_{SC2} and I_{SC5} are not the same, a different contribution of current will be added.

As observed in Figure 34, when the current sources values create a positive disequilibrium (orange lines in Figure 34), a similar degradation as presented before happens, the positive slew rate sees the current discharging the capacitor reduced by the contribution of the base current of the transistor Q10, which reduces also the slew rate. For the negative slew rate, the current charging the capacitor is increased by the value of the base current of the transistor Q10 and the slew rate is increased.

However, when the current sources values create a negative disequilibrium (blue lines in Figure 34), the degradation of the slew rate observed is completely reversed. This behavior can be explained by the following equations.

$$SR_P = \left(I_{C1} + \frac{I_{SC2}}{\beta_{10}} - \frac{I_{SC5}}{\beta_{14}} \right) / C_1 \quad \text{Equation II.3-9}$$

$$SR_N = \left(I_{C1} - \frac{I_{SC2}}{\beta_{10}} + \frac{I_{SC5}}{\beta_{14}} \right) / C_1 \quad \text{Equation II.3-10}$$

Because we consider now that the transistor Q14 has the same degradation as the transistor Q10, the contribution of the current coming from the base of the transistor Q14 has to be taken into consideration. For the positive slew rate, as presented by the equation (II.9), the current I_{B14} has a negative contribution

to the current charging the capacitor, reducing eventually the value of the slew rate. For the negative slew rate, as presented by the equation (II.10), the current I_{B14} has a positive contribution to the current discharging the capacitor, increasing eventually the value of the slew rate.

In this case, if the current I_{SC2} is lower than I_{SC5} , instead of adding a parasitic current for the positive slew rate, it will subtract it, and the degradation of the slew rate will be reversed. The opposite behavior happens with the negative slew rate.

II.3.3.4 Capacitor undersized

We have already seen in the previous part different degradation scenarios leading to a variation of the value of the parasitic current, affecting then the slew rate. However, considering the values of the slew rate before irradiation presented in Figure 21 and Figure 24, the slew rate is already higher for the LM124-ST than the other components. According to (II.4) or (II.8), either the current source value is higher on the LM124-ST, or the capacitor value is smaller.

In order to evaluate the effect of the capacitor value on the slew rate, simulations were performed with various value of the capacitor and with the two different disequilibria of the regulation pair, as presented in section II.3.3.3.

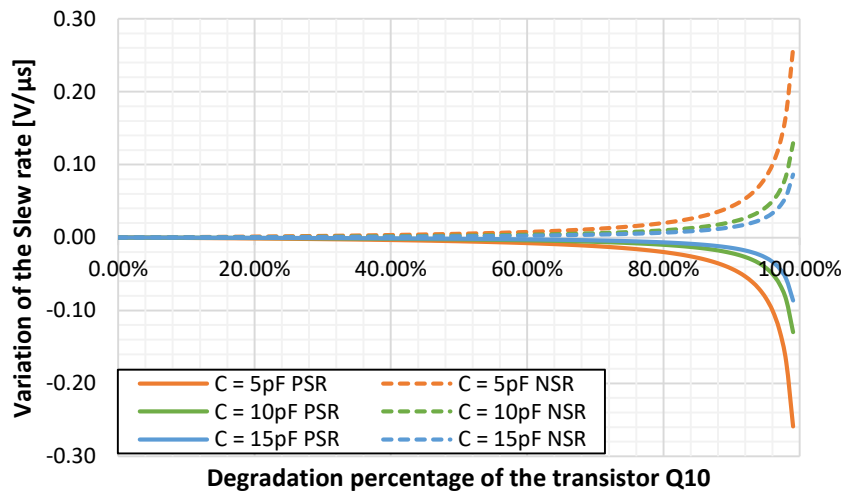


Figure 35: Variation of the positive slew rate (PSR) and negative slew rate (NSR) depending on the capacitor value. The simulations were performed with a constant current for I_{SC1} of $6\mu A$, I_{SC2} of $8\mu A$ and I_{SC5} of $6\mu A$.

Figure 35 and Figure 36 present the simulations results of the degradation of the slew rate depending on three different values of the capacitor, such as 5pF, 10pF, and 15pF. The graphics respectively correspond to the simulations with a positive disequilibrium (current I_{SC2} higher than I_{SC5}) and with a negative disequilibrium (current I_{SC2} lower than I_{SC5}). In both graphics, a larger variation of the slew rate is obtained with the smaller value of the capacitor. These results are in agreement with the equations (II.9) and (II.10).

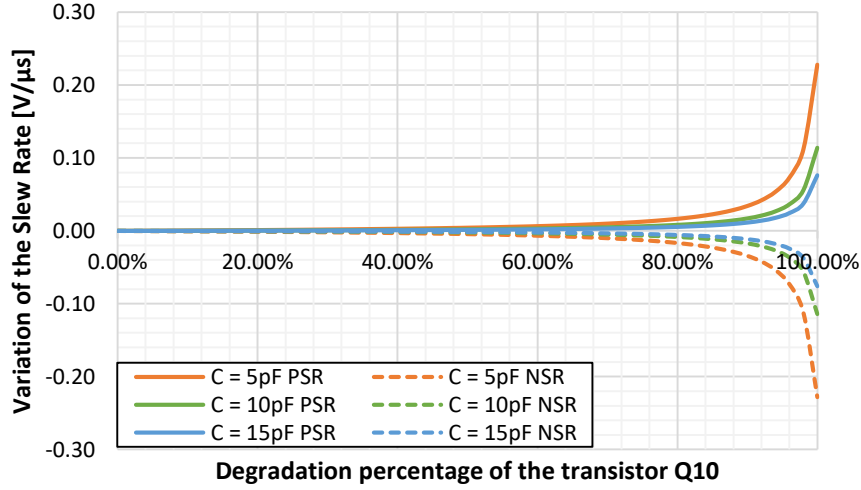


Figure 36: Variation of the positive slew rate (PSR) and negative slew rate (NSR) depending on the capacitor value. The simulations were performed with a constant current for I_{SC1} of $6\mu A$, I_{SC2} of $6\mu A$ and I_{SC5} of $8\mu A$.

As presented in section II.3.3.3, for a positive disequilibrium, the positive slew rate decrease and the negative slew rate increase; for a negative disequilibrium, the positive slew rate increase and the negative slew rate decrease. That explains the results obtained in Figure 35 and Figure 36.

II.3.3.5 Conclusion of the different degradation scenarios

In this section, different scenarios of degradation are presented

- An increase at the base of the transistor Q10 and Q14, caused by their degradation with TID or DD, is the main contributor to the variation observed of the slew rate,
- If the current source I_{SC1} is lower than I_{SC2} or I_{SC5} , the impact of the additional parasitic current will be higher,
- Depending on the value of the current source I_{SC2} or I_{SC5} , the degradation of the slew rate can be positive, negative or even can be compensated,
- A lower value of the compensation capacitor may induce a higher degradation of the slew rate.

It is important to note that all of the possible scenarios of degradation have all been treated and simulated separately; however, they all lead to an important variation of the slew rate. Therefore, by cumulating those degradation scenarios, an even higher variation of the slew rate is to expect.

The following section presents the different analysis performed after the different scenarios. Analysis at die layout level of the three different manufacturer's design is presented.

II.4. DIE ANALYSIS AND MEASUREMENTS

II.4.1. MICROPHOTOGRAPHY OF THE LM124

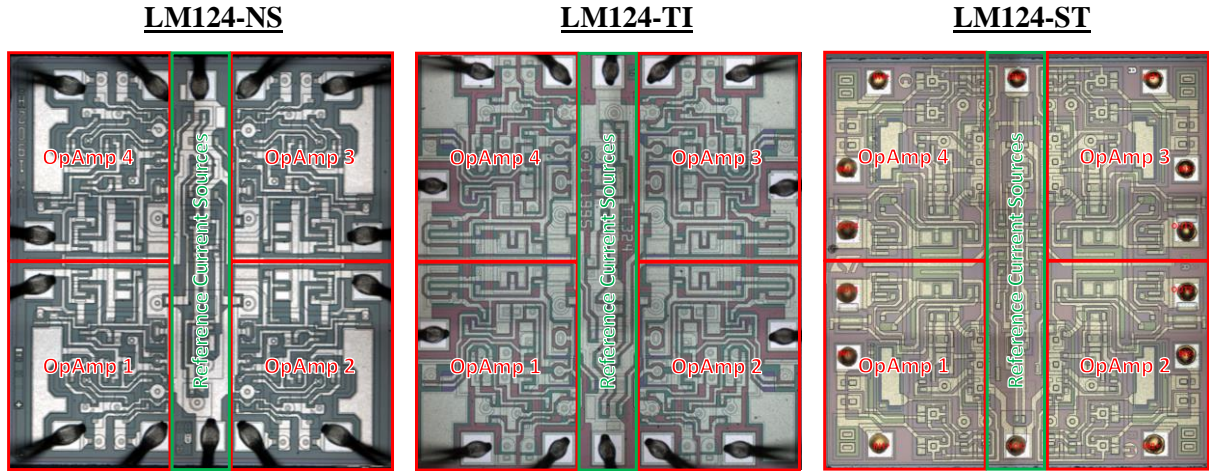


Figure 37: Microphotography of the complete die of the LM124 from National Semiconductors (NS), Texas Instruments (TI) and STMicroelectronics (ST)

The microphotographs presented in Figure 37 show the complete die layout of the LM124 from three different manufacturers. As observed on these pictures, each component is composed of four integrated operational amplifiers surrounded in red, all driven by a single common reference current source surrounded in green. The four integrated operational amplifiers are working independently one from the other. These microphotographs are used for all the analysis performed on the slew rate.

II.4.2. DIFFERENT BIPOLAR TRANSISTOR STRUCTURES

II.4.2.1 Vertical-NPN and Vertical-PNP structures

The vertical-NPN and vertical-PNP are the bipolar integrated component the most commonly used by the circuit designers. Their standard fabrication process gives the best ratio between the occupancy area and the performances. Figure 38 represents a theoretical cross section of a Vertical-NPN transistor [27]. In those transistors, the current flow (highlighted by the red arrows) is driven inside the volume of the component, far from the passivation oxide, through the N++ buried layer and is collected by the collector contact. The N++ buried layer is used to reduce the emitter-collector resistance when the component drives the current. The isolation doped P+ are placed to isolate the component one from another. The passivation oxide is placed on the top of the structure to protect the component to any exterior contamination (humidity, light, dust, etc.).

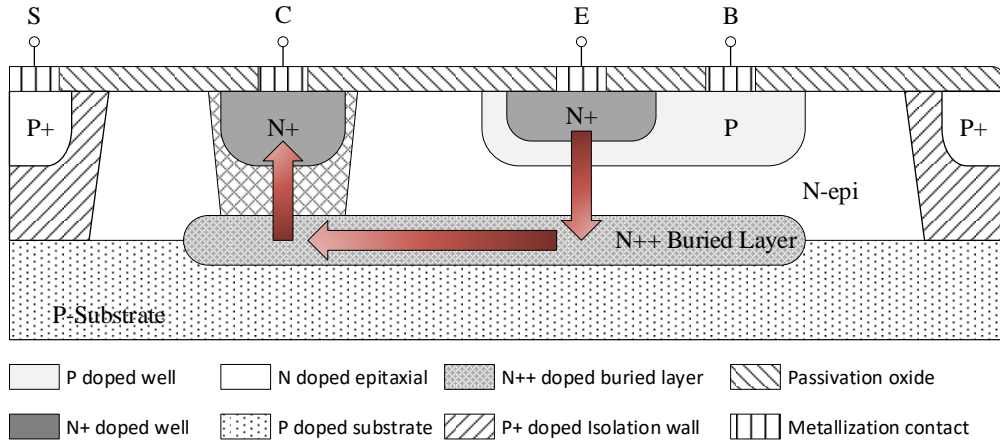


Figure 38: Cross section of the structure of a standard Vertical-NPN bipolar transistor. The component is composed of four different contacts: base (B), collector (C), emitter (E) and substrate (S). The current flow is represented by the red arrows.

II.4.2.2 Lateral-PNP structure

The Lateral-PNP transistors are less efficient than Vertical-PNP transistors; however, they are usually used as active charges of current sources in operational amplifiers. Figure 39 represents a theoretical cross section of a Lateral-PNP transistor [27]. The current flow is directly driven between the emitter and the collector, just below the passivation oxide. The N+ buried layer is used to limit the leakage current between the N-epi layout and the P-Substrate. The advantage of this structure is that they present higher isolations performances.

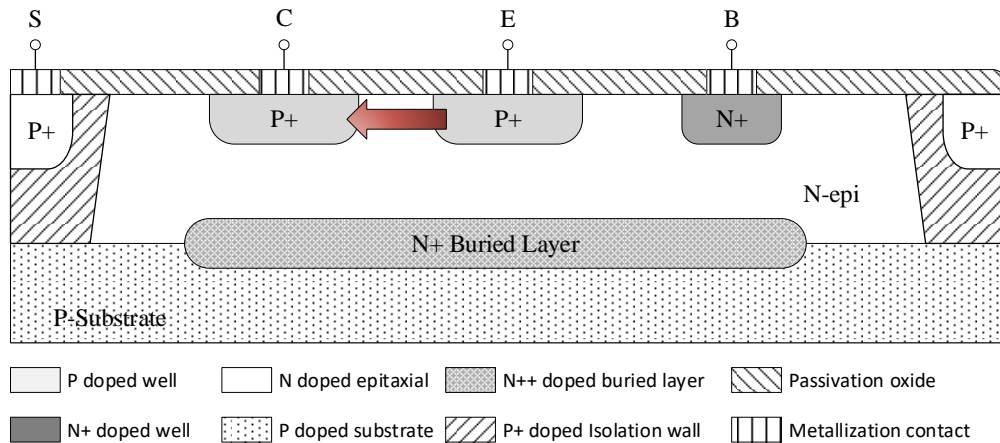


Figure 39: Cross section of the structure of a standard Lateral-PNP bipolar transistor. The component is composed of four different contacts: base (B), collector (C), emitter (E) and substrate (S). The current flow is represented by the red arrows.

The collector of L-NPN structures can be subdivided into several small transistors, sharing a common base and emitter. Such structure, called Split-collector transistor, is usually used as a current mirror. If the collectors share the same geometry, we can consider that they will have the same current. Moreover,

by changing the cross-section of the different collector, it is possible to tune the different currents supplied by each collector of the transistor.

II.4.2.3 Substrate-PNP structure

A Substrate-PNP is very similar to an L-PNP transistor, however the substrate act as the collector of the transistor. Therefore, the collector will always be connected to the lower potential of the component, which is usually the ground or the negative voltage of an operational amplifier. Those transistors are smaller than a standard V-PNP, and because the current flow can go everywhere around the emitter well, the emitter-collector resistor is smaller. Figure 40 presents the theoretical cross section of a Substrate-PNP.

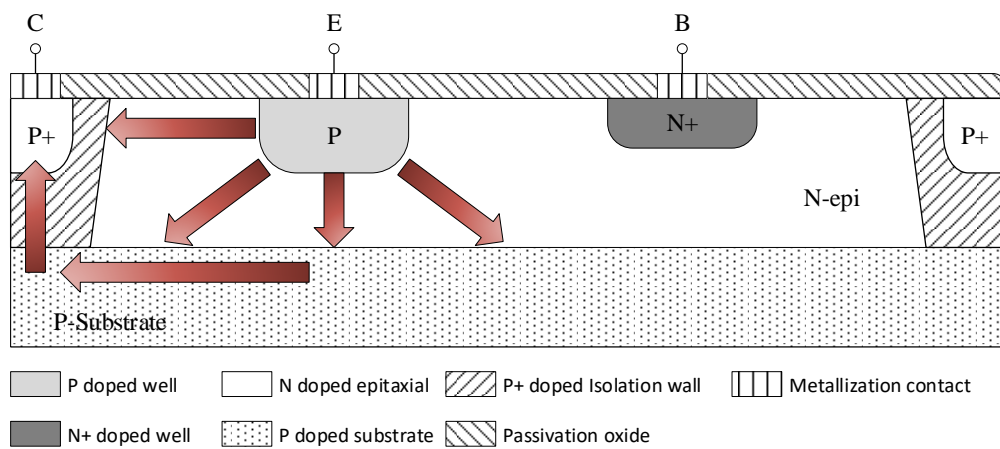


Figure 40: Cross section of the structure of a standard Substrate-PNP bipolar transistor. The component is composed of four different contacts: base (B), collector (C), emitter (E). For this particular design, the collector uses the substrate contact to collect the current. The current flow is represented by the red arrows.

II.4.3. LM124 DIE LAYOUT ANALYSIS

II.4.3.1 Structure of the transistor Q10

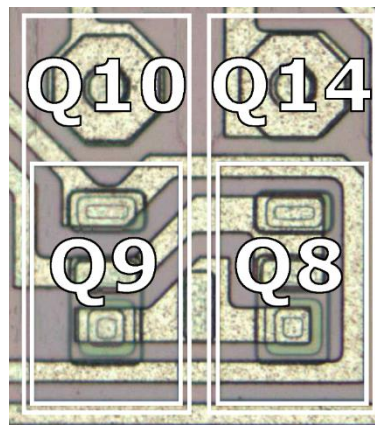


Figure 41: Microphotography of the transistor Q10 in the LM124-ST including Q9 inside its base region.

Figure 41 shows a microphotograph of the merged transistors Q9-Q10 and Q8-Q14 of the LM124-ST. As observed, each transistor is nested within another transistor. The utilization of such structure saves considerable space and is used for the differential pair of the operational amplifier [27]. Because of this specific structure, the transistor Q10 and Q14 are composed of more junctions than a normal transistor. Rodriguez *et al.* [28] have shown that when a cluster of defect is created inside a depletion region, because of thermal generation, the cluster act as a current generator. Thus, we suppose that depending on the location of the cluster, a significant increase of the Q10 base current can be induced by this thermal generation.

Figure 42 presents a tentative model structure of the transistor Q10 derived from the die layout picture presented in Figure 41. This structure was designed with another transistor inside its base. Because of this design and because Q9 and Q10 are respectively a vertical NPN transistor and a substrate PNP transistor, the current passes through vertically toward the substrate. Barnaby *et al.* [2], [29] and Rax *et al.* [30] showed that Vertical NPN, Vertical PNP, and Substrate PNP transistors are more sensitive to proton and neutron irradiations than TID. Those irradiations degrade simultaneously the surface recombination velocity, the net positive oxide charge and the collector-region lifetime (the base region of the two PNP transistors), which is a very sensitive parameter for bipolar technologies. As a result, both particles will subsequently cause an increased degradation of the current gain. Moreover, wider and deeper structures have an increased base width, which is another variable sensitive to DD.

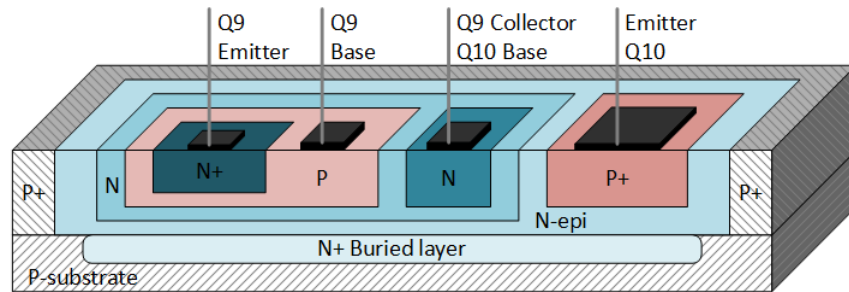


Figure 42: Estimated cross-section of the transistors Q9-Q10. This structure was designed with another transistor inside its base. Because of this design and because Q9 and Q10 are respectively a vertical NPN transistor and a substrate PNP transistor.

Because of this specific structure, the neutron-induced degradation will reduce drastically the gain of the transistor Q10 and consequently increase the base current of this transistor at the early stages of the irradiation.

II.4.3.2 Capacitor

In order to estimate the relative value of the capacitor C_1 between the three components, a frequency analysis was conducted. For this test, the operational amplifiers were configured in voltage follower as presented in Figure 43.

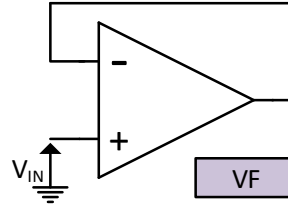


Figure 43: LM124 operational amplifier in voltage follower (VF) configuration used to perform a Bode diagram of each manufacturer

The results of the frequency analysis are presented in Figure 44. Each curve presents the average value obtained from ten samples per manufacturer. They express the gain of the operational amplifier in decibel, following the expression (II.11):

$$Gain [dB] = 20 \times \log \left(\frac{V_{OUT \text{ peak-peak}}}{V_{IN \text{ peak-peak}}} \right) \quad \text{Equation II.4-1}$$

As we can observe, the LM124-ST shows the highest cut-off frequency. The LM124-NS shows a cut off frequency of $2.6 \cdot 10^4$ Hz, $4.04 \cdot 10^4$ Hz for the LM124-TI and $7.26 \cdot 10^4$ Hz for LM124-ST. This is remarkable since the LM124-ST also exhibits the highest value of the current sources, consistent with a higher gain of the inverting stage, which should influence the Miller effect and reduce the cut-off frequency instead of increasing it.

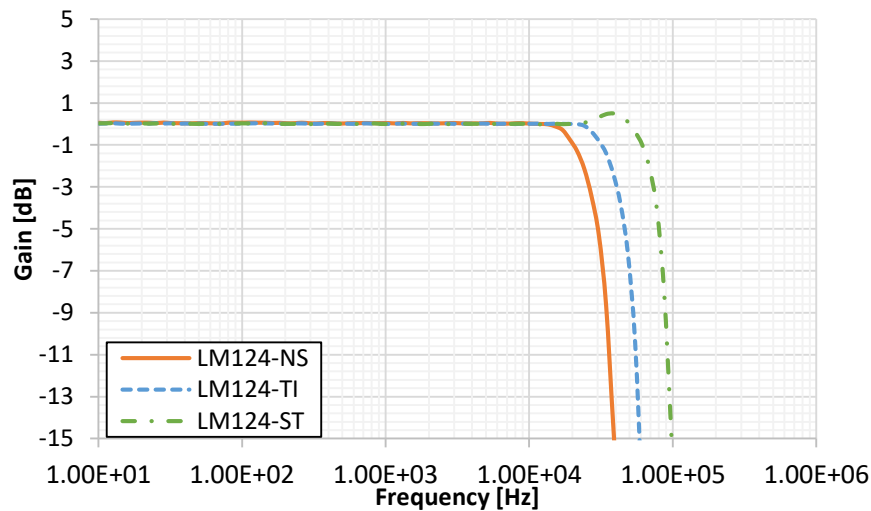


Figure 44: Baud diagram analysis performed on the three different LM124.

To achieve this higher bandwidth, it was obviously necessary for the manufacturer to reduce the value of the capacitor C_1 of the LM124-ST.

It was then interesting to verify if the capacitor area was smaller than the other manufacturers' parts. Therefore, the size of the capacitor on the chip was investigated visually. Figure 45 presents the microphotography of the different die for each manufacturer with, highlighted in red, the location of the capacitor on the die.

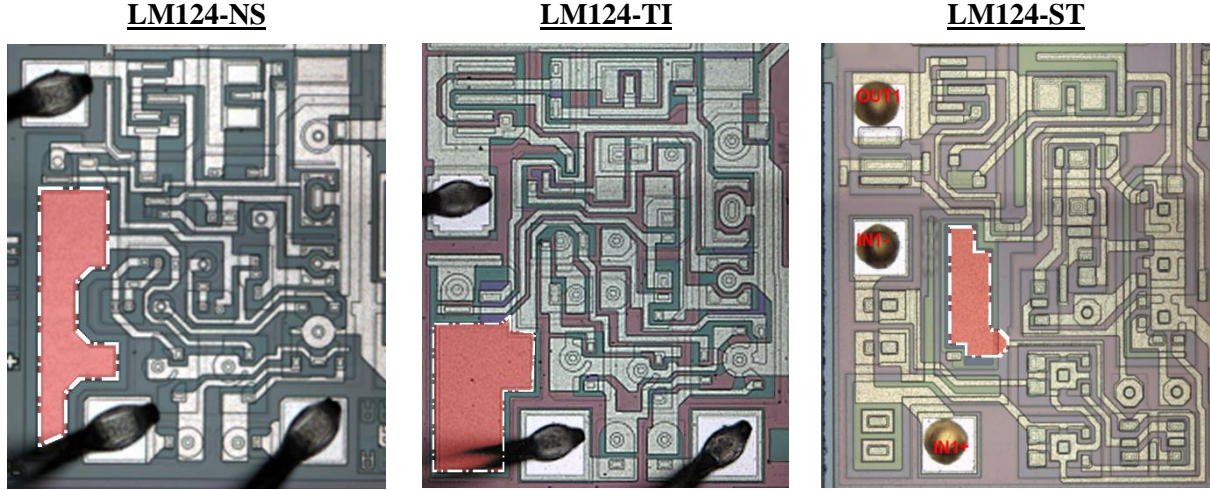


Figure 45: Photomicrography of one-quarter of each of the three die. These photos were taken with the same scale showing the capacitor size depending on the chip: LM124-NS, LM124-TI, and LM124-ST. On these pictures, the capacitor is highlighted in red and surrounded by white dashes.

It is understood that the visual size of the capacitor is not the only parameter conditioning the capacitor's value since the oxide thickness and the oxide permittivity impact on this value. Nevertheless, it is reasonable to think that a smaller occupancy size is an indication of a smaller value of the capacitor.

As we can see, the size of the capacitor for the LM124-ST seems to be the smallest of the three components. In order to estimate the real size of this capacitor, the area on the chip was compared to the total area of the chip for all the components.

Table II.4-1: Estimated size of the capacitor depending on their size on the chip

Component	LM124-NS		LM124-TI		LM124-ST	
Parameter	Area (%)	Area (μm)	Area (%)	Area (μm)	Area (%)	Area (μm)
Chip	100	182.09	100	215.84	100	183.48
Capacitor	3.27	5.96	2.85	6.15	1.12	2.05

Table II.4-1 summarizes the estimated size of each capacitor on the chip. The capacitor C_1 is much smaller for the LM124-ST compared to the other manufacturers. For the LM124-NS, the size occupied by the capacitor is $5.96 \mu\text{m}^2$. A similar size was measured for the LM124-TI, but for the LM124-ST the occupied area on the chip is only of $2.05 \mu\text{m}^2$, which corresponds to a size reduction of 34% compared to the LM124-NS and of 33% compared to the LM124-TI.

To conclude, all three investigations i.e. the frequency measurements, the impact of the miller effect with the higher OLG before irradiation and the size of the capacitor on the chip, suggesting that the capacitor value of the LM124-ST is much smaller than the others components.

According to the equation (II.9) and (II.10), the smaller value of the capacitor C_1 for the LM124-ST will lead to a larger variation of the SR with TID or DD.

II.4.3.3 Stabilization transistors

The structure formed by the transistors Q10 and Q14 is used to compensate any variation of the differential pair of Q10 induced by the temperature or by its leakage current. As presented in Fig. 8, in order to ensure a perfect equilibrium of the differential pair, the transistors Q8 and Q9 must be the same to have the same amount of current driven by the current mirror and ensure a proper parallelism in the two branches. Therefore, the transistors Q10 and Q14 must have the same design.

In our case, when the transistors Q10 and Q14 degrade, if their current sources, known respectively as I_{SC2} and I_{SC5} , are different, a disequilibrium will be observed for the differential pair, and consequently, the SR will be impacted.

II.4.3.4 Current sources

As presented in [3], Roig et al. showed that all parameters of the LM124-ST (including SR and OLG) are twice that of LM124-NS and 1.33 times higher than LM124-TI. According to this, the current source I_{SC2} should be greater for the LM124-ST than for the other devices, and so, the base current of Q10 should be more important for the LM124-ST.

In order to have a good estimation of the current source values, an analysis of the spread collector transistor used to provide the current for each part of the circuit, was performed.

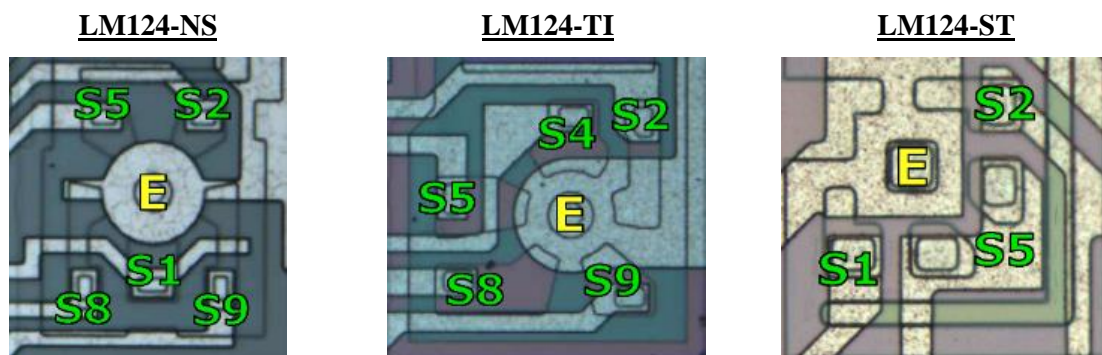


Figure 46: Photomicrography of split collector transistor of the three chips: (a) LM124-A, (b) LM124-B and (c) LM124-C. Those transistors are used to provide the current for some parts of the circuit. On these pictures, the labels S1, S2, S5, S8, S9 corresponds

Figure 46 presents the split collector transistor for each chip. The figure on the left corresponds to the chip LM124-NS, the one in the middle to the LM124-TI and the one on the right to the LM124-ST.

To create several different currents from a single transistor, the split collector transistor is commonly used in analog devices. It generates different currents values by shaping each collector area individually with different sizes. On this spread collector, only the current sources I_{SC1} , I_{SC2} , I_{SC5} , I_{SC8} , and I_{SC9} are generated because they have a relatively close value. In comparison with I_{SC3} , I_{SC6} , and I_{SC7} which generate a higher current.

To estimate the value of the current for each current source on the same component, the collector zone was measured and compared to the size of the current source I_{SC1} that was taken as a reference with a value of $6\mu\text{A}$. These values are not correlated to the real values of the current sources, but they give an analogy with respect to the actual values of the current sources.

Table II.4-2: Estimated value of the current source depending on their sizes

Current source	LM124-NS		LM124-TI		LM124-ST	
Parameter	Area	Estimated current	Area	Estimated current	Area	Estimated current
I_{SC1}	21.5 %	$6.0\mu\text{A}$	18.9 %	$6.0\mu\text{A}$	28.1 %	$6.0\mu\text{A}$
I_{SC2}	15.1 %	$4.2\mu\text{A}$	19.1 %	$6.1\mu\text{A}$	30.3 %	$6.5\mu\text{A}$
I_{SC5}	15.6 %	$4.3\mu\text{A}$	20.3 %	$6.4\mu\text{A}$	41.7 %	$8.9\mu\text{A}$
I_{SC8}	23.5 %	$6.4\mu\text{A}$	26.1 %	$8.3\mu\text{A}$	-	-
I_{SC9}	24.5 %	$6.8\mu\text{A}$	15.4 %	$4.9\mu\text{A}$	-	-

Table II.4-2 presents the estimated values for each current source on the spread collector transistor. On the chip of the LM124-ST, I_{SC8} and I_{SC9} were removed by design and are not present.

As presented here, the estimated values of the current sources show that for the LM124-NS, first the current sources I_{SC2} and I_{SC5} have a small current value compared to I_{SC1} , which, as seen in section II.3.3.2, reduce the parasitic additional current when the transistor Q10 degrades. Moreover, because the current sources I_{SC2} and I_{SC5} are equal, the increase of the base current of the transistor pair Q10-Q14, caused by their degradation, should balance each other out. Therefore, no degradation of the slew rate is to expect. Those results are consistent with the DD irradiation results presented in Figure 22 to Figure 24. Similar values and phenomenon are observed for the LM124-TI.

However, for the LM124-ST, the values of the current sources I_{SC1} , I_{SC2} and I_{SC5} are relatively different. Indeed, as presented in section II.3.3.2 and II.3.3.3, because the current sources I_{SC2} and I_{SC5} have a higher value than I_{SC1} , the degradation of the pair Q10-Q14 will lead to a higher parasitic base current. Moreover, as seen in section II.3.3.3, such values are the worst-case condition for the disequilibrium of the current sources values I_{SC1} and I_{SC2} . In addition, the current source I_{SC2} and I_{SC5} are completely different with the value of I_{SC5} a lot higher than I_{SC2} . Such value will lead to a negative disequilibrium of the regulation pair.

II.5. DISCUSSION

II.5.1. CONCLUSION ON THE DEGRADATION

In the section II.3, a circuit level analysis is performed and all the conceivable degradation scenarios leading to a degradation of the slew rate are presented. Depending on the value of the current sources I_{SC1} , I_{SC2} , and I_{SC5} , the resultant degradation of the slew rate may induce a large variation of the slew rate value. It was also shown that, depending on the value of the current sources I_{SC2} and I_{SC5} , the slew rate degradation could be amplified, compensate or even reverse (positive variation instead of a normal expected negative variation).

In order to determine the origin of the degradation of the slew rate observed in Figure 24, different analysis and measurement at die level were performed. As presented in section II.4.3, a large quantity of measurement revealed that most of the cases presented are the cause of the large variation of the slew rate:

- The transistors Q10 and Q14, because of their structure, are more sensitive to DD than to TID,
- Because of the lower value of the capacitor for the LM124-ST compared to the others components, for the same value of the parasitic current, a higher variation of the slew rate will be observed,
- The value of the current sources I_{SC2} and I_{SC5} have been estimated to supply respectively $6.5\mu A$ and $8.9\mu A$. Because of these values, according to equation (II.9), the slew rate is expected to increase when the structure Q10-Q14 degrades.

The variation of the slew rate observed in Figure 24 can now be explained:

Because of the higher value of the current sources I_{SC2} and I_{SC5} compared to I_{SC1} , the increase of their base current when the transistor Q10 and Q14 degrades is high enough to affect the slew rate. Moreover, when the LM124-ST switches from a low-level state to a high-level state, the positive slew rate starts limiting the switching of the output stage in time. Because the transistor Q10 and Q14 are already degraded, and because the current of I_{SC5} is higher than I_{SC2} , an additional current in the negative branch of the differential pair will increase the current pulled from the current mirror, speeding up the discharge of the capacitor. The slew rate is then increased. Moreover, because the value of the capacitor is almost three times smaller for the LM124-ST compared to other components, the influence on the slew rate will be three times higher.

In addition, when the LM124-ST switches from a high-level state to a low-level state, the negative slew rate starts limiting the switching of the output stage in time. Because the transistor Q10 and Q14 are already degraded, and because the current of I_{SC5} is higher than I_{SC2} , a current in the negative branch of

the differential pair will be generated, and the current mirror will pull some current, slowing down the discharge of the capacitor. The slew rate is then be reduced. Moreover, because the value of the capacitor is almost three times smaller for then LM124-ST compared to the others components, the influence on the slew rate will be three times higher.

II.5.2. IMPACT ON THE RADIATION HARDNESS ASSURANCE

System designers are sometimes constrained to use COTS for various reasons (cost, availability, etc.). As presented in this paper, screening of parts has to be done properly. Indeed, this paper points that a component with the same reference coming from different a manufacturer does not ensure the same behavior and reaction against radiation. Because each manufacturer has to design their own component with their own parameters involving the placement, the transistors types, the doping, etc., implies that each component will differ from the other components and will have to be tested in order to ensure system reliability against radiation.

Furthermore, parameters of linear operational amplifiers do not degrade in a monotonic way. Thereby, measurements during tests must consider this non-linearity, and intervals between measurements of parameters must be chosen to be sure that all phenomenon occurring during irradiation are detected. Indeed, in our case, without the step at 1.10^{12} n.cm⁻² fluence, during the DD tests campaigns, no atypical behavior would have been detected, moreover, depending on the specifications, this component would have displayed a perfect non-degradation of the slew rate.

II.6. CONCLUSIONS

During TID and DD irradiation test campaigns, operational amplifiers LM124 from three different manufacturers were tested. During those tests, most of the manufacturer's components were following the same degradation trend with different sensitivity, as expected. However, one of the components showed an unexpected variation of its slew rate during neutron irradiation. According to the internal electrical schematic and to the equations of the slew rate mechanism, the degradation of the slew rate is expected to follow the degradation of the supply current. However, the components from STMicroelectronics exhibit a non-logical degradation of the slew rate. Indeed, not only does the degradation show no decrease at a dose of 5.10^{12} n.cm⁻² compared to its pre-irradiation value, but it also increases significantly for a dose of 1.10^{12} n.cm⁻².

In order to understand which phenomenon modify the degradation logic of the slew rate, different simulations, analysis of the design and measurements were performed to compare which parameters differ from one component to another, and how it affects the slew rate mechanism.

First, an analysis of the internal electrical schematic was performed on the three different component. A reverse engineering shows that all the three components share the same internal electrical schematic, except for a slight difference in the input stage of the device LM124-ST in which the current sources were removed. The latter has no effect on the slew rate degradation and affect only the input stage of the component. Therefore, PSpice simulations were performed with the internal electrical schematic deduced from the reverse engineering, and different possible scenarios of degradation were considered.

Overall, it was shown that in all the degradation scenarios, an increase in the base current of Q10 and Q14 is responsible for the shape of the DD induced degradation of the LM124-C.

Next, a die layout analysis was performed with different microphotography of the three manufacturers' components. Compared to the LM2124-NS and LM124-TI, the LM124-ST showed that both the increased value of the current sources and the decreased value of the capacitor strongly enhance the degradation. Thing that is not observed on devices with the usual design. Moreover, it was shown that the compensation structure formed by Q10 and Q14, designed to compensate fluctuations in the differential pair, because of the value of their current sources; a negative disequilibrium is created in the differential pair during the irradiation, reversing the logic degradation of the slew rate.

Finally, it was shown that the two nested structures composed of Q9-Q10 and Q8-Q14 increases greatly the number of PN junction and makes this stage more sensitive to DD than it is for TID.

Whatever the designer's motivation for tuning the current values and changing the design at transistor level (increasing the performance, TID hardening...), this result shows, one more time, that it is critical

to screen parts properly and that devices with the same name but from different manufacturers, may exhibit very different behavior.

II.7. REFERENCES

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III.1. INTRODUCTION

Electrostatic discharge (ESD) has been a critical problem for businesses for hundreds of years. The EOS/ESD notes that issues can be traced back all the way to the 1400s when the military were using static control procedures and devices trying to prevent inadvertent electrostatic discharge ignition of gunpowder stores [1]. Back in our days, ESD remains a critical concern for electronic component manufacturers. The cost of electronic components losses due to ESD is estimated in a range from 500 million to 5 billion dollars and beyond each year [2], [3]. More and more protection types have been developed first to limit the production of ESD, from ESD bracelet to ESD carpet or floor, including ESD shoes [3], [4]. However, many others natural phenomena can generate an electrostatic charge which can lead to the destruction of an electronic component. Therefore, active ESD protections can also be used inside or outside a device, protecting electronics from ESD. Despite all the protections used in all domains, a large quantity of devices are still damaged by ESD stress when people touch them, by natural discharge, in space by spacecraft discharge etc. [5], [6].

In order to protect electronic devices, a large number of additional MOS structures are introduced in the IC which may affect the reliability of the whole device when exposed to radiation. This impact should be considered from two different points of views: (1) Radiation effects on ESD protection MOS structures may induce leakage currents; (2) After irradiation, the protection may degrade and thus, fail to protect the IC against ESD.

Very few studies on the radiation-induced degradation of ESD protections were carried out with Total Ionizing Dose (TID) while their degradation may be responsible for some unexplained behaviors observed. In their work, W. Liang *et al.* [7] have presented irradiation with He⁺ Ions response of different ESD protection types. They have highlighted the fact that some ESD protection structures can exhibit an increase of the on-resistance and an increase of the leakage current after irradiations. However, those tests do not prove the impact of TID irradiation.

Considering the potential reliability concern raised, it is important to evaluate the impact of a radiation-induced degradation on the efficiency of an ESD protection. It is also critical to understand if the ESD structure introduces failure mechanisms due to leakage currents, leading to a current overconsumption of irradiated components.

In the first section of this chapter, the fundamental principle of the electrostatic discharge is presented considering the generation, the discharge itself and its potential effect on electronic components. In a second section, the different mitigation techniques by means of different types of ESD protection structures, their role and their implantation inside an IC are explained. A specific type of ESD protection, the GGnMOS, considered as potentially at risk, was selected and used as a test structure on the entire thesis.

Because the GGnMOS ESD protection is an integrated structure, it is not possible to find this type of structure as discrete devices on the market. Moreover, the house made design and manufacturing of GGnMOS structures would have first required a complete knowledge of their fabrication processes and a large amount additional time to design, to manufacture and to test the structure, which was out of the scope of this thesis. Therefore, it was decided to study the GGnMOS ESD protection embedded in commercial off the shelf memory device. It is understood that the core of MRAM memories is very resistant to TID by construction [8], [9]. However, some MRAM devices, designed with GGnMOS ESD protection, exhibited an unexpected radiation-induced behavior. Therefore, it was decided to take this component as a test vector to determine, based on simple measurements, if those ESD protections may have caused the TID induced degradation. The investigation of a GGnMOS ESD protection integrated inside a MRAM memory is presented as the third section of this chapter.

III.2. CAUSES AND CONSEQUENCES OF AN ELECTROSTATIC DISCHARGE

III.2.1. ELECTROSTATIC CHARGE GENERATION

An Electrostatic Discharge (ESD) is always the result of charge disequilibrium between two objects. However, the electric charges can be generated in many different ways depending on the environment in which the object evolves.

At ground level, the generation can be caused by two different effects such as the triboelectric effect and the electrostatic induction. Triboelectric charges are generated when two dissimilar materials are rubbed against one another and then separated or when two materials are brought into physical contact. During this contact, an exchange of free electrons between the two materials is produced, leaving one material negatively charged and the other positively charged. The work function is the property of a material's ability to hold onto its free electrons (the electrons orbiting the outer most shell of the material). The greater the material work function, the less likely it will give up its free electrons during contact (triboelectric generation). The weaker the work function is, the more likely the material will acquire a positive charge by giving up some of its free electrons. So, materials with higher work functions tend to appropriate electrons from materials with lower work functions [10]. This exchange of electrons also depends on many others factors such as room temperature, relative humidity, and duration of contact, among others [11].

In aerospace, electrostatic charges can be generated in flight by static electricity under various flight conditions. The friction of the air onto the surface of any plan, rocket, etc. is the main cause of the generation of static electricity. The charges are accumulated in the material and the discharge happens to neutralize the accumulated charges [12].

In space, another phenomenon, called the *spacecraft charging*, is one of the main concerns for spacecraft and causes every year the destruction of space systems [13]. Indeed, photons and electrons emitted by the sun and electrons plasma in space, charge any surface of a spacecraft by photoelectric effect. Whenever the potential difference between the two surfaces is high enough, a discharge occurs between those two surfaces.

III.2.2. CAUSE OF AN ELECTROSTATIC DISCHARGE

An Electrostatic Discharge (ESD) is always the result of charge disequilibrium between two objects. The ESD event occurs to balance the charges between the two objects. Whenever a material has accumulated a sufficient amount of charges to break through the energetic exchange barrier, the ESD

discharge occurs. When the ESD current generated by the discharge passes through an object, the impedance of that object creates a difference of potential. An ESD can generate a voltage from a few kV on the ground up to tens of kV in space, with a current ranging from 1A up to 15A [13].

The high voltage generated and high current flow usually does not last more than a microsecond, however, longer discharges can sometimes happen depending on the materials in contact. This phenomenon is no longer referred to as ESD but as Electrical OverStress (EOS).

III.2.3. CONSEQUENCES OF AN ELECTROSTATIC DISCHARGE ON INTEGRATED CIRCUITS

Manipulation of electronic devices in an unprotected environment is the main cause of the destruction of electronic components. Nowadays, the improvement of the technology introduces important modifications in electronic devices such as shrinking dimension or thinning of gate oxide that tends to increase the sensitivity to ESD stress.

As explained before, ESD stress is an important concern for electronic devices because it may generate both high voltage (few kV) and high current (few A) discharges on very small devices that may lead to the destruction of the chip [14]–[16]. The energy released by an ESD aggresses the component by direct conduction, inductive coupling, and capacitive coupling. The result of an ESD stress goes from defect creation inside the component to the complete destruction of the device. Depending on several parameters, an ESD stress can damage a junction, the metal or the oxide [14], [17].

When an ESD stress strikes an electronic component, the discharges causes Joules heating into the depleted area of the silicon. The heat generated can be increased by the current flow flowing into the silicon because of an inhomogeneity of the doping. In case of an extreme heating, the silicon can melt and a redistribution of the charges of the doped area happens, which can lead to a modification of the charge distribution inside a component. Indeed, some component requires an abrupt charge distribution to improve performances and limit the current leakage. After an ESD stress, the gradient of the charge distribution may be reduced, altering the performances of an electronic component and an increasing of the leakage currents [14], [18].

Higher energy can also generate higher temperatures that may spread up to the contacts and cause the melting of the metal and the silicon, creating a thin intermediate alloy layer, which modifies the properties of the component [14].

The last degradation mechanism on the oxides is caused by charge trapping or defect creation at the interface. Due to the destruction of the atom's chemical bound, defects can be created at the Si/SiO₂ interface leading to the creation of interface traps [18].

However, the occurrence of the above damage mechanisms depends mainly on the energy, duration, and shape of the ESD.

III.2.4. ELECTROSTATIC DISCHARGE MODELS

III.2.4.1 The HBM model

The Human Body Model (HBM) is the oldest ESD model and one of the most commonly used to compare ESD sensitivity levels of parts [19]. The shape of the HBM discharge is defined by several tests standards such as the MIL-STD-883K method 3015.7, the JEDEC, or the ESDA⁹. However, each standard has its own specificity.

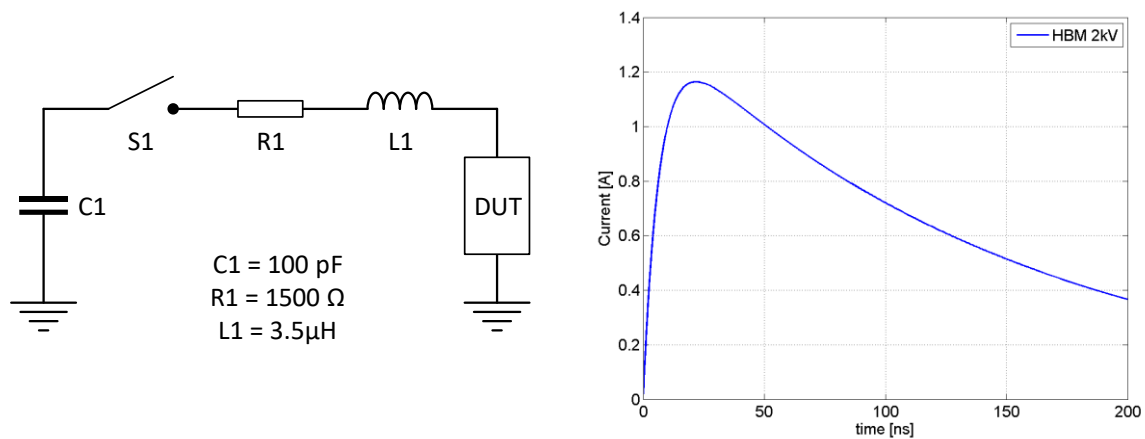


Figure 47: Simplified equivalent electrical schematic of an HBM stress and its current waveform.

Globally, it simulates a discharge of a standing person touching a component with his finger. The human body is a big source of ESD because it gets charged when walking on a carpet, touching objects, facing the sun, etc... The amount of charge that can accumulate on a body depends greatly on the environment (humidity, temperature etc.), the footwear, the healthiness etc. This model was developed by manufacturers mainly to avoid the destruction of the components on a wafer caused by the contact with an operator during the production process [20].

Figure 47 presents the simplified electrical schematic used to simulate an HBM ESD pulse with its current waveform. In this model, C1 and R1 represent the capacitor and the resistance of the body and these values have been standardized in [21] by the *Electrostatic Discharge Association*.

III.2.4.2 The MM model

The Machine Model (MM), was introduced first in Japan as a worst-case scenario of a discharge compared to the HBM model [22]. It is mainly used today to simulate the discharge of a machine/tool

⁹ ESDA: Electrostatic Discharge Association

(welder, screwdriver, etc.) into an electronic component. To do so, the serial resistance previously used to simulate the resistance of the human body is now replaced by a much lower resistance.

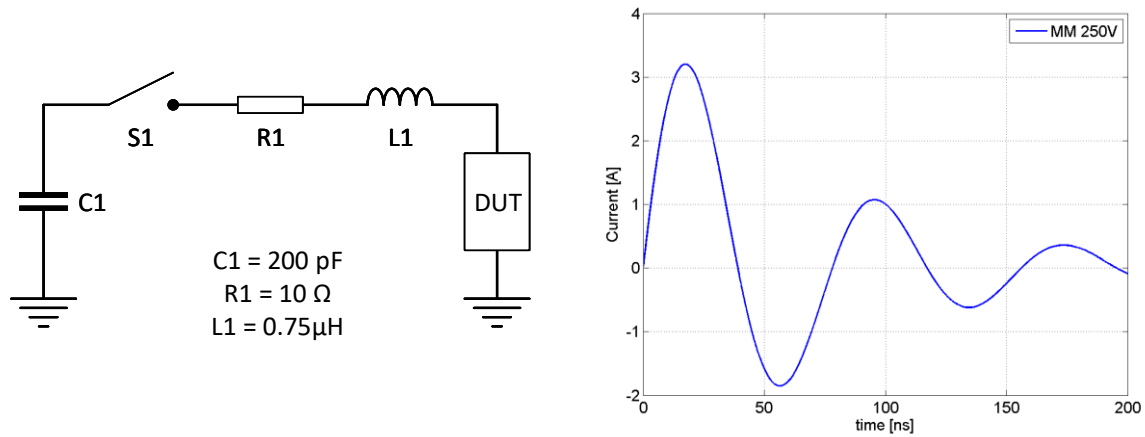


Figure 48: Simplified equivalent electrical schematic of a MM stress and its current waveform.

Figure 48 presents the simplified electrical schematic used to simulate a MM ESD pulse with its current waveform. In this model, C1 and R1 represent the capacitor and the resistance of the tool touching the component. These values have been standardized in [22] by the *Electrostatic Discharge Association* with the *JEDEC Solid State Technology Association*.

Due to the lower resistor value compared to the HMB model, the rising time of the discharge is faster and the current max is higher than the HMB's one. Moreover, because of the oscillation of the discharge, negative and positive discharges are successively generated.

III.2.4.3 The CDM model

The Charged Device Model (CDM) has been developed to simulate a very fast discharge of an integrated circuit, previously charged by electrical induction, on a ground plate or a metallic rail. It is mainly used to simulate a discharge produced in an autonomous manufacture. Compared to the HBM model or the MM model, because the discharge modeled is generated only by the contact between the metallic part themselves, the resistance and the parasitic elements are lower, resulting in a more powerful discharge in a shorter time.

Figure 49 presents the simplified electrical schematics used to simulate a CDM ESD pulse with its current waveform. In this model, C1 represents the charge accumulated inside a component itself and the discharge is made through the connection of the components. These values have been standardized in [23] by the *Electrostatic Discharge Association* with the *JEDEC Solid State Technology Association*.

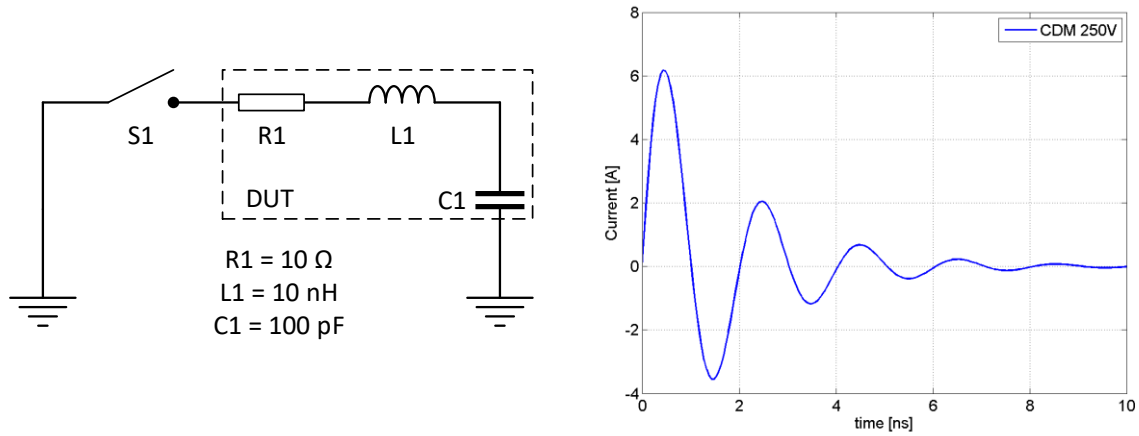


Figure 49: Simplified equivalent electrical schematic of a CDM stress and its current waveform.

III.2.4.4 Comparison between the three models

Figure 50 presents the current waveform of the three different ESD stress presented in this section. As observed, the CDM stress induces a higher current ($\sim 6\text{A}$) with a smaller rising time ($\sim 450\text{ ps}$) compared to the others models. Indeed, the HBM shows the smallest current spike ($\sim 1.16\text{ A}$) with a high rising time ($\sim 20\text{ ns}$) and the MM shows the higher current spike ($\sim 3.2\text{ A}$) with a rising time smaller ($\sim 15\text{ ns}$) compared to the HBM.

With a similar rising time and duration, the HBM and the MM produce the same failure mechanism since they generate the same amount of Joules heating. For CDM, because the rise time is much faster it often leads to a unique failure mechanism more destructive like oxide breakdown [24].

Even if the HBM has a lower current compared to the others models, the heat generated to dissipate is the larger than the CDM. In addition, because of the MM's discharge shape is oscillating, it is more sensitive to parasitic elements, making the tests and simulations more difficult to set up. Therefore, the HBM is used to assess the robustness of the component over time.

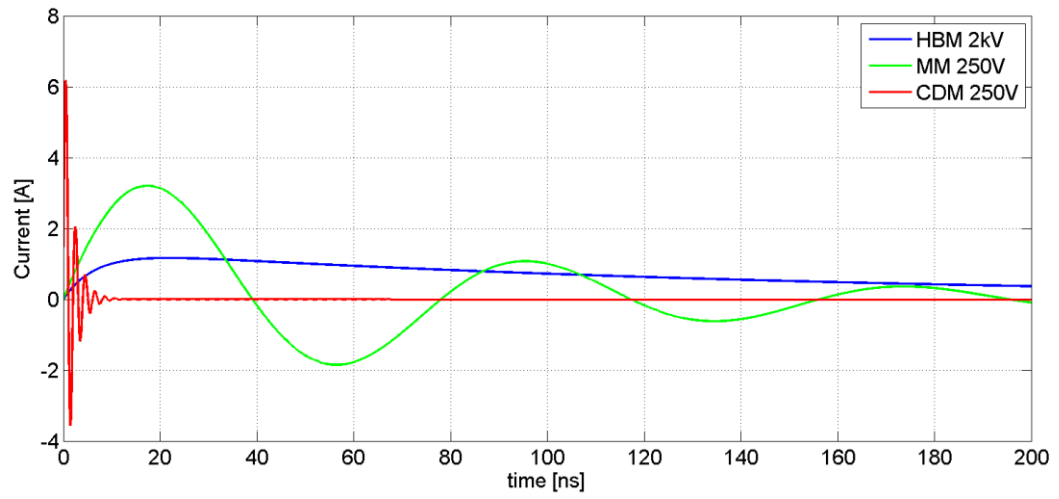


Figure 50: Comparison between the three ESD models discharge shapes presented previously.

III.3. PROTECTION AGAINST AN ELECTROSTATIC DISCHARGE EVENT

III.3.1. GENERALITIES

The incidence of ESD-related damage dates back to the dawn of semiconductors, but it did not become a prevalent problem until the 1980s where the microchip and thin-gate-oxide FETs for highly integrated ICs were introduced [7]. Later then, starting from the late 1990s, the technological improvement has led to a shrinking of IC geometries, making ICs more vulnerable to damage from ESD [25].

Therefore, to limit the creation of potential differences between two objects during the fabrication process, components manufacturers have implemented inside their working areas passives ESD protection discharging then any buildup charge. In addition, actives protection structures were also developed and included inside the design of the component, to protect it against ESD stress at any time.

III.3.2. DIFFERENT TYPES OF ESD PROTECTION

III.3.2.1 Passives ESD protections

All along its lifetime, an electronic component is meant to be manipulated several times by machines, operators, tools, etc. that can lead to an electrostatic discharge and could damage the electronic component. Therefore, in order to protect the electronics components, different passives ESD protection are used during the fabrication process to limit the charge generation and the evacuation of the charges contained in anything touching the components [26].



Figure 51: ESD prevention logo.

Some protections are used to prevent charge generation inside any material that could touch a component. To do so, different anti-static materials have been added on the test benches, on the working areas, on the composition of the handle of the tools that are manipulated, on a working space (working surfaces, transportation bags, components rails etc.) and to limit charge generation on the human body (antistatic gloves, antistatic shoe sole, antistatic carpet, antistatic strap band, etc.).

As second protection used to prevent ESD discharge is to connect all the equipment that touches the component with a common ground (working surfaces, welder pins, component, the human body, robotic system, etc.)

Another solution to avoid charge generation or discharge is to control the environment factors (humidity, temperature, air ionization, etc.) of the all the places where the electronic component are (storage area, working area, operating area).

Despite all of the precautions recommended to manipulate electronic components, those rules are mainly applied in the manufacture areas. Therefore, different types of protection have been developed and can be added to a component, internally and externally. Those protections are called actives protections because they are implemented inside the electrical design and their operation state changes depending on the voltage at their terminal.

III.3.2.2 Actives ESD protections

During the manufacturing process, besides the passive ESD protections that are used to avoid ESD-induced damages, actives protections can also be used as a protection against ESD discharge provoked by the manipulation of a user or by the charged environment. Therefore, to protect electronic devices, ESD protections are implemented in-chip as close as possible to the terminals of the component. Those ESD protections are mainly used to protect the component against standards ESD discharges (presented in a next section). However, depending on the environment, the ESD discharge may be stronger than expected. Therefore, external ESD protection can be added as an additional protection from ESD discharges.

III.3.2.2.1 On-chip protection

On-chip protections are directly implemented inside the component. They are mainly used to protect an integrated circuit to standards ESD that can appear on the pads of the component. Figure 52 presents the implementation principle of an on-chip ESD protection. In order to reduce the possible destruction of a component's track that could act as a fuse, that on-chip ESD protection are usually implemented as close as possible to the pad on the die. More detail on this type of ESD protection is given in section III.3.4.

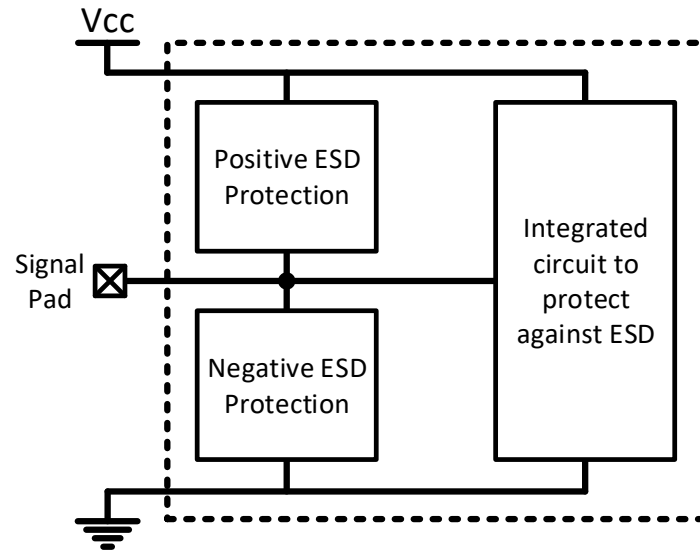


Figure 52: Implementation of an internal active ESD protection (or On-chip protection)

III.3.2.2.2 Externals ESD protections

When an electronic component is integrated inside an electronic system, the different pads of the component are usually connected to other component or connectors, creating then a direct path connecting a pad with an unprotected compound (sensor, antenna, etc.).

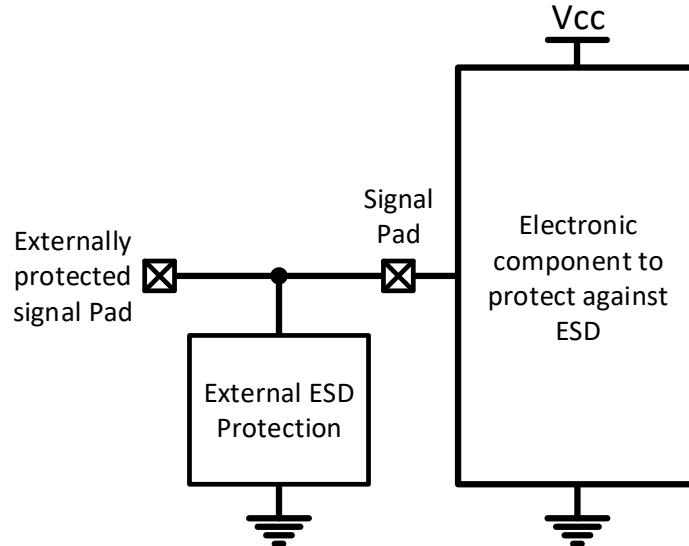


Figure 53: Implementation of an external active ESD protection

Depending on the environment where the electronic system evolves in, an important ESD discharge may be generated and driven to a pad of a component. In this case, an external ESD protection can be used as additional protection structure, giving less stress to the internal ESD protection.

Figure 53 presents the implantation principle of an external ESD protection. The external protection is usually placed as close as possible from the component. Therefore, if an ESD stress occurs, the external

protection is triggered before the component's protection, and all the heat generated by Joules effect is dissipated outside the component. Compared to an internal active ESD protection, the external protection are usually designed with a Zener diode or two diodes top to tail paralleled, protecting then the component from positive and negative ESD stress.

III.3.3. IDEAL ESD PROTECTION DESIGN

III.3.3.1 Working principle of an ideal ESD protection

In an ideal case, the working principle of an ESD protection is comparable to a controlled switch. When an ESD event occurs, the switch is switched on and the current generated by the ESD is directly driven to the lower voltage. Moreover, in a normal operation mode, the protection should act as an open switch with an infinite impedance and no parasitic capacitance. Figure 54 represents this ideal implementation of a protection for one signal pad.

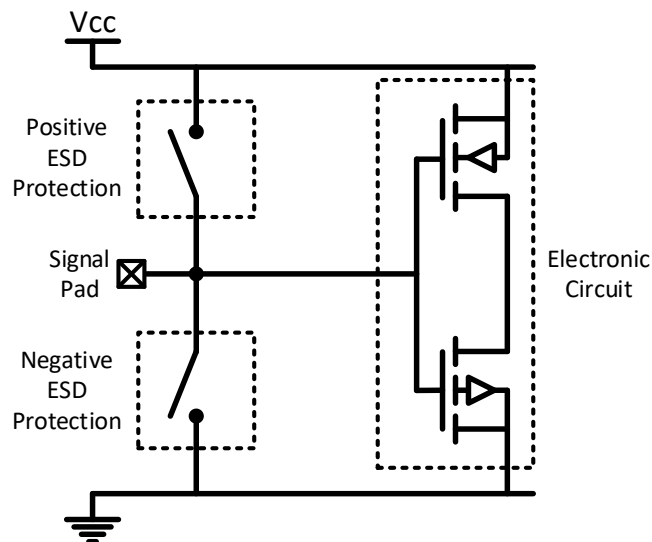


Figure 54: Ideal working principle and implantation of an ESD protection

To protect an electronic circuit behind one single pad, two different protection means are to be implemented. A negative ESD protection protects the circuit against a positive ESD discharge, and a positive ESD protection protects the circuit against a negative discharge. Moreover, as already mentioned, those protections have to be located close to the pads, avoiding then the destruction of the internal metallic connections.

III.3.3.2 Ideal specifications for an ESD protection

In order to protect efficiently an electronic component, ideally, the ESD protection structure shall respect those requirements [27]:

- Unnoticeable: an ESD protection structure must be electrically neutral. In other terms, any parasitic resistors and parasitic capacitors, which might be created by the addition of the structure in paralleled, shall be as low as possible. Moreover, the leakage current of the ESD protection shall be minimized.
- Effective: an ESD protection shall be able to limit effectively the voltage of an ESD event to protect the integrated circuit. Depending on the application and the technology node of the component, some ESD protection structures might be designed in multi-fingers configuration. This technic can be used to share the electrostatic current of the discharge among the different fingers, and limit the current to evacuate per finger.
- Robust: an ESD protection shall be able to resist to any ESD event and shall reduce the destruction risks of the electronic component.
- Compact: because the ESD protections structures implemented inside the integrated circuit can be numerous, their occupancy on the die layout must be as small as possible.
- Fast: as seen in the section III.2.4 because an ESD event can rise to up to a few kV within the nanoseconds, an ESD protection structure must trigger fast enough to protect the integrated circuit. In the eventuality that an ESD protection structure is not fast enough, an ESD event would damage the integrated circuit and may render the entire component inoperative.

III.3.3.3 Id-Vd characteristic of an ideal ESD protection with snapback

To achieve an effective ESD protection, the ESD protection should be carefully designed to limit the voltage across the device during an ESD stresses [28]. The effectiveness of every snapback ESD protection relies on their similarity with the ESD window design presented in Figure 55.

The main role of an ESD protection is to limit the I/O pad voltage below the breakdown voltage (V_{BD} in Figure 55) of the chip gate oxide, by bypassing most of the ESD stress current into the protections, preventing the internal circuits from any damage. In addition, this structure must not be triggered below the normal operating voltage ($V_{t1} > V_{DD}$, see Figure 9) [29]. The on-resistance of the ESD protection must be minimized in order to reduce the power to dissipate in case of ESD discharge. Moreover, the holding voltage (V_h in Figure 55) of the ESD protection device should be larger than V_{DD} to avoid latch-up [30].

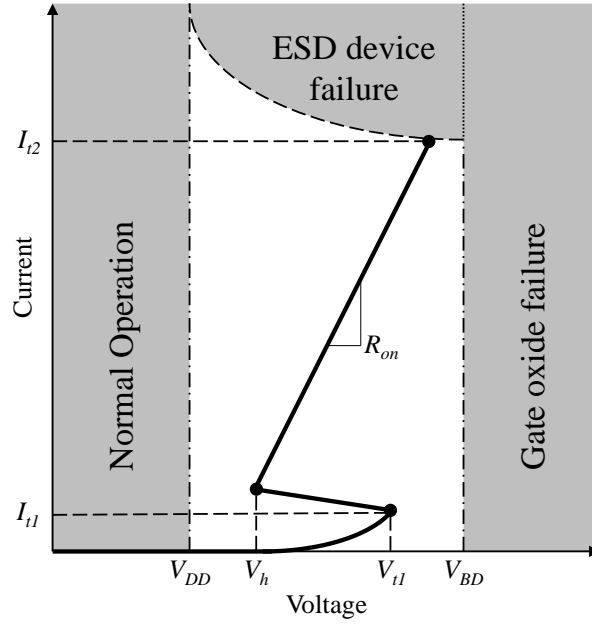


Figure 55: Typical ESD window design of an ESD protection with snapback [30]–[32].

III.3.4. IMPLANTATION STRATEGY OF AN INTERNAL ACTIVE ESD PROTECTION

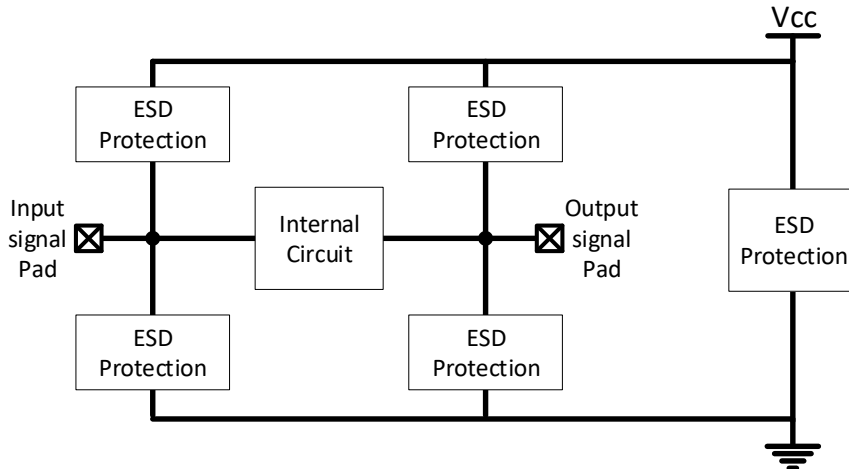


Figure 56: Implementation strategy of an internal active ESD protection structure of an integrated circuit

In order to protect efficiently an integrated circuit, all the pads on the component must be protected against both the positive and the negative discharges. To do so, each pad is designed with positive and negative ESD protections. Two different types of protection may be encountered: the signal ESD protection and the power clamp ESD protection.

Usually, the power clamp ESD protections are more robust than the signals ones because they are designed to survive to a higher overcurrent. Figure 56 presents the implementation strategy of any ESD

protection inside an integrated circuit. The goal of those protections is to provide a discharge path from a pad to the GND for any polarity of an ESD event.

III.3.5. TYPES OF INTERNAL ACTIVES ESD PROTECTION

All over the years, because of the damages caused by the ESD events, the manufactures started to integrate ESD protection inside the component on each peripheral of the die. Several types of protections were developed starting from the diode, which is still considered as one of the most effective protections. However, its occupation and its current leakage started have become simply too large to accommodate as and the components were getting smaller. Then manufacturers started implemented BJTs in bipolar-based component. Because of the increase of MOSFET based component, the GGnMOS were developed as a twin MOSFET based ESD protection based on the behavior of the BJT ESD protection. In the end, the SCR was developed for high voltage applications. Those ESD protections are among the most commonly used ESD protection, however, several others type of protection were developed but are not presented here.

III.3.5.1 The Diode

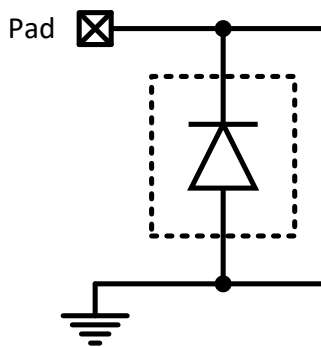


Figure 57: Representation of a diode-based ESD protection

The diodes are the oldest ESD protection used in microelectronics. Back in the 80's, this protection was the most commonly used and remains today quite often used for the input/output signal pads or for the power supply. When forward-biased, because of its low voltage threshold (around 0.6V), the diode protect efficiently the circuit. Indeed, the power to be dissipated and its on-resistance are very low, which gives to the diode a high robustness. When reverse-biased, the diode starts to conduct due to the avalanche breakdown or due to the Zener effect depending on the diode type. In this case, its on-resistance is higher and a higher power is dissipated.

Therefore, in order to ensure a proper efficiency of this ESD protection, the occupancy area of the diode must be large enough to ensure its robustness. Moreover, it is not possible to configure a specific triggering voltage with a diode. Depending on the required triggering voltage, several diodes are added in series, increasing then the triggering voltage of the whole set of diodes.

Nowadays, the diodes are mainly used in high-frequency domain because of their low parasitic capacity compared to the others ESD protection. However, their high leakage current is often a blocking point depending on the application of the component [14], [27], [33].

III.3.5.2 The bipolar NPN transistor

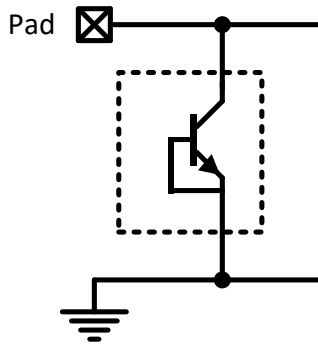


Figure 58: Representation of a NPN transistor-based ESD protection

The bipolar transistor used as an ESD protection has its base connected to its emitter. When a negative discharge occurs, the collector-base is similar to a forward-biased diode. Due to the low triggering voltage of its diode, the structure only has to dissipate a small amount of energy, making it robust. However, when a positive discharge occurs, the bipolar transistor is blocked until the avalanche breakdown of the collector-base junction. At this moment, because of its dynamic snapback characteristic, and when the current is high enough, the base-emitter junction is forward-biased and the voltage of the component drops down to the holding voltage, offering a high robustness due to the low power dissipated.

When an ESD event occurs, The low on-resistance and the voltage snapback makes this structure one of the most robust protection [14], [27], [34].

III.3.5.3 The NMOS transistor (or GGnMOS)

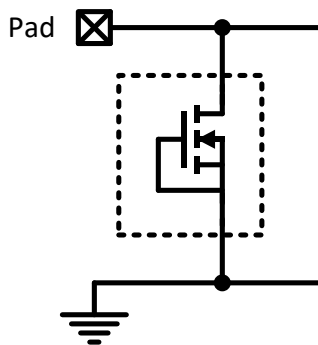


Figure 59: Representation of a N-MOS transistor-based ESD protection

The GGnMOS (or Gate Grounded N-MOSFET), is a structure similar to the bipolar NPN transistor. Because the gate, source, and substrate contacts are all connected to the ground, it is used in the same way as the bipolar NPN transistor. However, because the parasitic bipolar transistor formed by the source well, substrate, and drain well is a lateral structure, the dissipation of the power is less effective. When a negative discharge occurs, the diode formed by the drain/substrate junction is forward-biased, allowing a high current dissipation. When a positive discharge occurs, the parasitic bipolar transistor of the GGnMOS drives the ESD discharge to the ground.

GGnMOS protections are usually used in for CMOS devices for which the use of bipolar NPN transistor is not an option. However, compared to the bipolar, the GGnMOS does not resist as efficiently to high voltages, and is unable to handle high current; several GGnMOS transistors are the used in parallel in order to share the discharge current [14], [27], [34].

III.3.5.4 The Thyristor (or SCR)

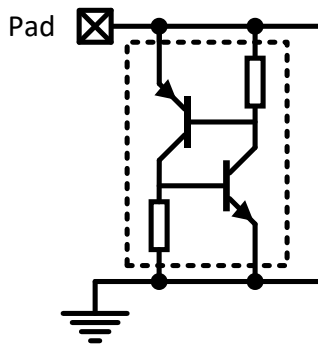


Figure 60: Representation of a Thyristor based ESD protection

The Thyristor (of the Silicon Controlled Rectifiers) is commonly used as switching elements in high power applications. It is usually composed of one PNP and one NPN transistors and can be triggered by a simple command. The advantage of this structure is that its on-resistance is very low, generating little heat to dissipate.

It is known to be the most efficient ESD protection with a low space occupancy, low holding voltage, and low current leakage. The triggering voltage is usually high, but can be reduced by adjusting some doped areas,

III.3.6. CHARACTERIZATION METHOD OF ESD PROTECTIONS

Different types of ESD protection used in microelectronics were presented in the previous section. Due to their small occupancy and their transient behavior, it is difficult to perform measurements using static methods on this type of structure. One of the most commonly used method to evaluate the performances of each structure consists in using a Transmitted Line Pulse that generates an input similar as an ESD event, a pulse with a high energy but with a very short duration in time. This method allows the characterization of the full characteristics of the ESD protection up to the thermal breakdown (I_{t2} in Figure 55). However, TLP measurements require a complex dedicated equipment. Without this equipment, it is still possible to perform static measurement by limiting the current of the source in order to avoid the thermal breakdown of the ESD protection.

III.3.6.1 Standard characterization method: Transmitted Line Pulse

A Transmitted Line Pulse (TLP) is a measurement method used for ESD protection devices. It is used to characterize performance attributes of devices under stresses that have a short pulse width and fast rise time similar to those of ESD events [35]. This characterization can be performed using standard TLP test bench in Figure 61 or a basic time domain reflection TLP as presented.

It consists of a coaxial cable load with a high voltage power source, discharges into the DUT. To charge this line, the switch connects the line to the power source to charge. Then, SW closes and all the energy stored inside the line gets discharged through the DUT. By sensing a succession of pulse, it is possible to measure the response of the ESD protection and then plot the ESD window characteristic.

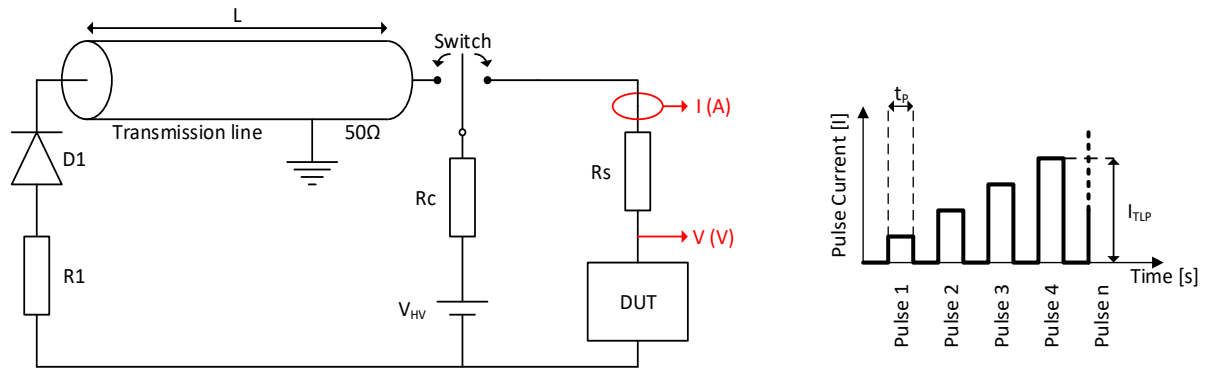


Figure 61: Basic TLP system sending successive pulse loaded inside the transmission line [35]

III.3.6.2 Alternative characterization method: DC measurement

Another characterization method that can be used consists in recording the characteristics of the ESD protection using the standard static characterization with a SMU or a similar device. DC measurement is seldom used to characterize ESD protection because the main interest of performing this type of characterization is to measure the ESD triggering voltage and determine how the protection structures behave with high current pulses. However, it is also possible to perform a DC measurement of the leakage current of the structure at low voltage or to detect the triggering voltage. The only constraint of these tests is that the current should remain very low to avoid thermal breakdown of the structure. Therefore, only the bottom part of an ESD design windows can be measured.

By using the SMU in voltage source mode as presented in Figure 62(a), it is possible to measure the current for low voltage operation. Raising the voltage above the breakdown voltage would directly bring the current up to the current limit of the SMU. Triggering the avalanche with a non-controlled current would definitely damage the ESD protection due to overheating. An example of these two measurements methods is presented in Section III.4.2.2.

By using the SMU in current source mode as presented in Figure 62(b), it is possible to control precisely evolution of the close and even above the breakdown voltage. Because the current is controlled, no sudden rise in the dissipated power is to expect. However, because of the low current leakage of the structure, the characterization of the component for the low voltage in this mode is not possible. An example of these two measurements method is presented in Section III.4.2.2.

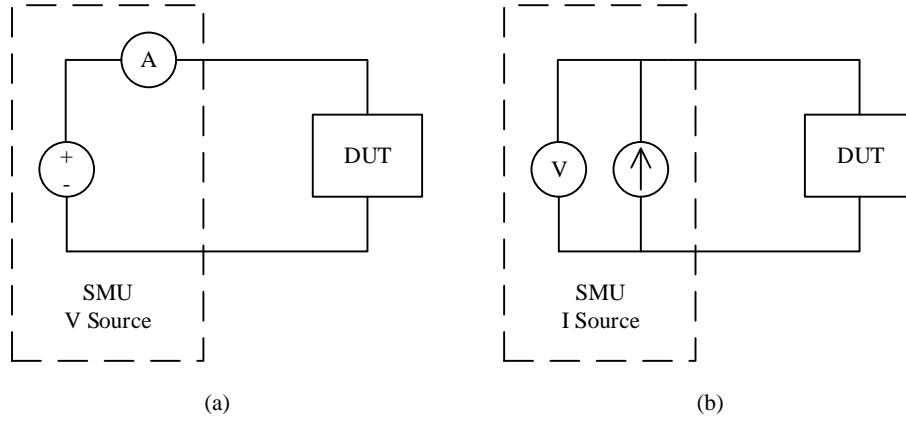


Figure 62: Working principle of an SMU in (a) voltage source model and (b) current source mode.

Therefore, by switching between current source and voltage source, it is possible to measure the triggering voltage and the leakage current of the ESD protection.

III.3.7. SELECTION OF THE ESD PROTECTION CANDIDATE

The aim of this work was to investigate the degradation of the GGnMOS based ESD protections. Indeed, this structure is expected to exhibit a degradation similar to the degradation observed on regular MOSFET transistors.

As explained in the section III.3.5.3 the GGnMOS is an ESD protection device used inside the CMOS integrated circuit. It consists of a structure similar to a MOSFET component with an access to the bulk. The contact gate, source, and bulk are all physically connected to the lower voltage of the circuit. To operate, this component uses the parasitic NPN bipolar transistor formed by the drain and source well and the substrate.

Figure 63 represents a simplified GGnMOS structure with its working principle. When the drain voltage increases, the P/N junction formed by the drain well and the substrate starts to leak (1). The hole current generated by this strong potential difference is driven through the substrate to the bulk contact. The increase of the current leads to an increase in the voltage between the source well and the bulk because the hole current passes through the substrate resistance (2). When the voltage V_{SUBS} reaches 0.6V – 0.7V, the bipolar transistor starts to drive an electron current from the drain to the source (3). In the end, the increase of this current auto-biases the parasitic bipolar transistor, leading to a voltage drop at the drain terminal (4). Then, depending on the energy to be evacuated, the current passing through the GGnMOS' channel determines the voltage at the drain terminal (Drain current \times Channel resistance). The ESD protection has then played its role and when all the energy is evacuated, the structure switches off and return to idle mode.

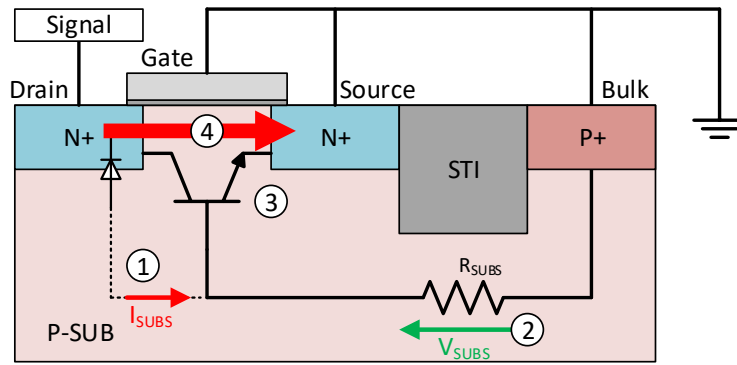


Figure 63: Simplified representation of a GGnMOS ESD protection and its working principle

The following section presents the results of the TID irradiation performed on a MRAM memory endowed with GGnMOS Protections. The challenge in this study was to evaluate the ESD protection efficiency after irradiation without having any access to the die.

III.4. EVALUATION OF THE ESD PROTECTION OF A MRAM MEMORY

III.4.1. CONTEXT

Because GGnMOS ESD protections are an integrated structure, it is not possible to find these types of standalone structures on the market. Moreover, a device layout is a well-protected industrial secret, which makes it very difficult to have access to the actual design. Therefore, it was decided to consider a black box device and try to evaluate the modifications in the efficiency of its ESD protections before and after irradiation.

Some previous work including irradiations performed on a MRAM memory had given interesting results. The supply current would rise drastically after a few tens of krad_(Si) while the core of the MRAM is supposed to be immune to radiations. These results suggest that the GGnMOS ESD structures played a significant role in this phenomenon. Several COTS MRAM devices were then procured to serve as DUT in this study.

A reverse engineering process should have been performed on this memory to confirm that it was endowed with GGnMOS protection. However, this process requires first to remove the lid of a component, and then to observe the component through an optical microscope, Scanning Electron Microscopes (SEM) or by X-Rays. Unfortunately, MRAM are equipped with a metallic shield used to protect the memory from external magnetic fields that is impossible to remove without destroying the device made this of observation. Thus, it was decided to proceed anyway with the characterization of ESD protections and consider it as a black box.

III.4.2. DUT CHARACTERIZATION

In order to evaluate the degradation of the GGnMOS structures' MRAM with TID, Id-Vd characterization was performed using a high-performance Source Measurement Unit (SMU) B2902A [36] from Keysight Technology. This SMU made possible to perform high precision current or voltage characterizations by sourcing the voltage or the current and limiting the current or the voltage. Thereby, no damage can be caused to the DUT. As presented in section III.3.4 (Protection methodology), the ESD protection structures are supposed to be different for the signal pins and for the power supply pins. Therefore, two different characterizations parameters were used.

III.4.2.1 Devices Under Test

The device under test is a MRAM memory manufactured by Everspin Technologies. This memory, referenced as MR0A08BCYS35, is an asynchronous memory with a memory capacity of 1Mb [37].

III.4.2.2 Power supply input characterization

To characterize the power supply pins, two types of measurements were performed:

Characterization type	Source Type	Source Value	Compliance
$I = f(V)$	Linear Voltage sweep	From 3 V to 10 V	0.2 A
$V = f(I)$	Logarithmic Current sweep	From 1.10^{-9} A to 0.2 A	9 V

The characterization of both power supply pins of the device was performed separately at first, then simultaneously.

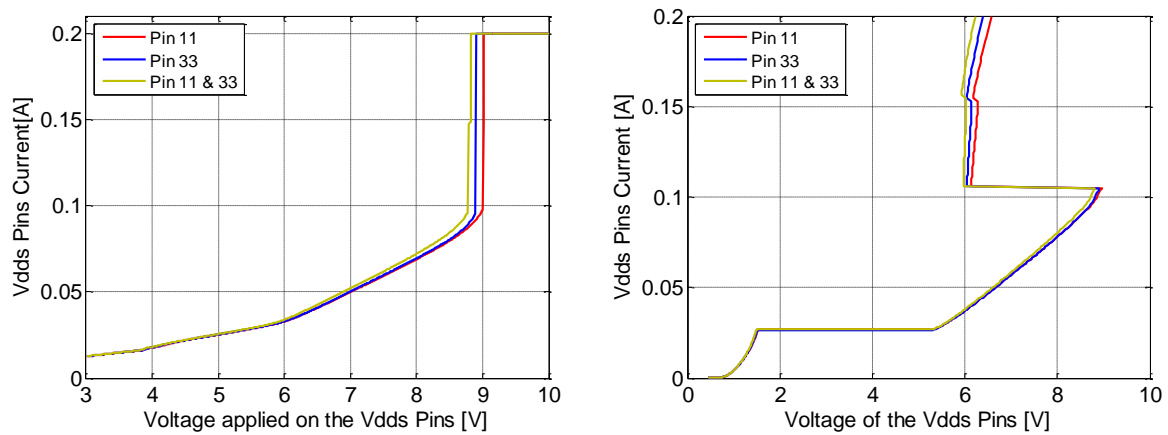


Figure 64: I_d - V_{ds} characterization of the power supply inputs of the memory before irradiation. The plot on the left (a) represents a characterization of those inputs by applying a voltage and by measuring the current. The plot on the right (b) represents a characterization of those inputs by applying a current and measuring the voltage.

Figure 64 represents the results given by the characterization of the power supply pads. Figure (a) represent the results obtained on the V_{DD} pads when applying a voltage and measuring a current, whereas figure (b) represents the results obtained on the V_{DD} pads when applying a current and measuring a voltage. The current on figure (a), exhibits a small increase during the voltage sweep, followed by a just strong rise before reaching 9V. This sudden increase is explained by the triggering of the protection structure only protected by the SMU current limiter. On the curve in figure (b), we can observe a different behavior of the voltage when a current is applied. If we take a closer look at the curves around 9V, we can observe the voltage snap-back as describe in III.3.3.3. As the current is kept constant, the voltage is controlled and no damage on the component is to expect.

To protect signal pads, designed to be less robust than the power supply pads, only characterizations using a current source characterization were performed.

Characterization type	Source Type	Source Value	Compliance
$V = f(I)$	Logarithmic Current sweep	From 1.10^{-9} A to 0.4 A	7 V

The memory device is endowed with many signal pads. A few of them only were characterized. However, all GGnMOS structures are designed to provide the same level of protection and they should all exhibit similar Id-Vd characteristics. In order to avoid any ESD stress, even the pads with no purpose (NC¹⁰, DC¹¹) are equipped with a GGnMOS structure.

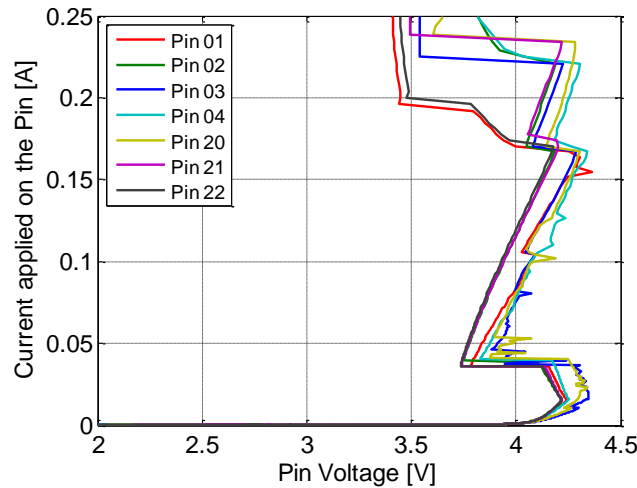


Figure 65: Id-Vds characterization of the signals inputs of the memory before irradiation.

Figure 65 presents the Id-Vds characteristics of different signals pins of the memory. As observed on this picture, no matter which signal pin is used, it triggers in a similar way. Each pin exhibits several small snapbacks at different value of the current. This mechanism is caused by the different fingers of the GGnMOS protections placed in parallel that triggers one after the other. As explained in the section III.3.3.3, to avoid latching-up the holding voltage, the ESD protection must go below the operating voltage of the device. The triggering voltage of the ESD protection on our memory is no more than 2V above the operation voltage. Thus, several GGnMOS in parallel trigger one after the other if the current keeps on increasing.

Even if the measurements seems to be different, globally all the different pins have more or less the same triggering voltages and similar holding voltages. Therefore based on those values, it was decided to proceed and to irradiate the memory to determine the impact of TID on the effectiveness of ESD protections.

¹⁰ NC : Not Connected

¹¹ DC : Do not Connect

III.4.3. RADIATION TESTING

III.4.3.1 Experimental details

TID experiments were performed using ^{60}Co γ -rays source at CERN¹² (Geneva, Switzerland) up to a dose of 110 krad_(Si) on two memories.

Table III.4-1: Description of the irradiation performed on the memory

Start date	End Date	Dose rate Memory 1	Dose rate Memory 2	Total dose Memory 1	Total dose Memory 2
01/03/2017 15:45	08/03/2017 13:27	550 rad/h	637 rad/h	91.1 krad	105.6 krad
08/03/2017 13:27	09/03/2017 11:29	238 rad/h	238 rad/h	96.3 krad	110.8 krad
09/03/2017 11:29	13/03/2017 15:01	238 rad/h	X	120.1 krad	110.8 krad

Table III.4-1 summarizes the different dose rates employed during the whole irradiation process. At first, both memories were irradiated with a dose rate of 550 rad/h and 640 rad/h (measured by means of an ionization chamber). The difference in the dose rates was caused by another test setup put in front of the memory setup. After a week of irradiation, a new user experiment was installed in the irradiation room, which caused the dose rate to be reduced down to 238 rad/h. After receiving a dose of 110.8 krad the memory n°2 had to be removed before the end of the irradiation because of a manipulation error that led to the destruction of the memory.

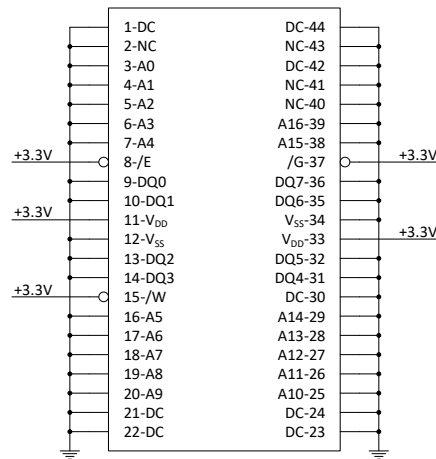


Figure 66: Biasing condition of the memory during the ^{60}Co irradiations.

The experiments were performed on both memories in the configuration presented in Figure 66. They were supplied with a voltage of 3.3V and the current consumption was monitored by the power supply

¹² CERN : European Organization for Nuclear Research

during all the irradiation. All the data and address pins were biased at 0V, except for the driving signals that were biased at 3.3V. This case corresponds to the standby mode of the memory.

As presented in the literature, this irradiation does not correspond to the worst-case irradiation of a memory. In order to maximize the degradation, the memory could be set in dynamical mode, or even static mode, however, the purpose of this irradiation was to evaluate the degradation of the memory's ESD protections. Therefore, in order to observe only the degradation of the ESD protection structure, the memory was set in standby mode, reducing then its sensitivity of the core to TID.

III.4.3.2 Experimental results

III.4.3.2.1 *Online current measurements*

Figure 67 presents the evolution of the current consumption of the two memories during the irradiation. As explained in section III.4.3.1, the memory M2 was removed from the irradiation room before the memory M1 due to a manipulation error. Therefore, the Figure 67.a and the Figure 67.b do not have the same irradiation time. As depicted on those two plots, after an irradiation of 110 krad_(Si) no degradation of the current consumption was observed for both memories.

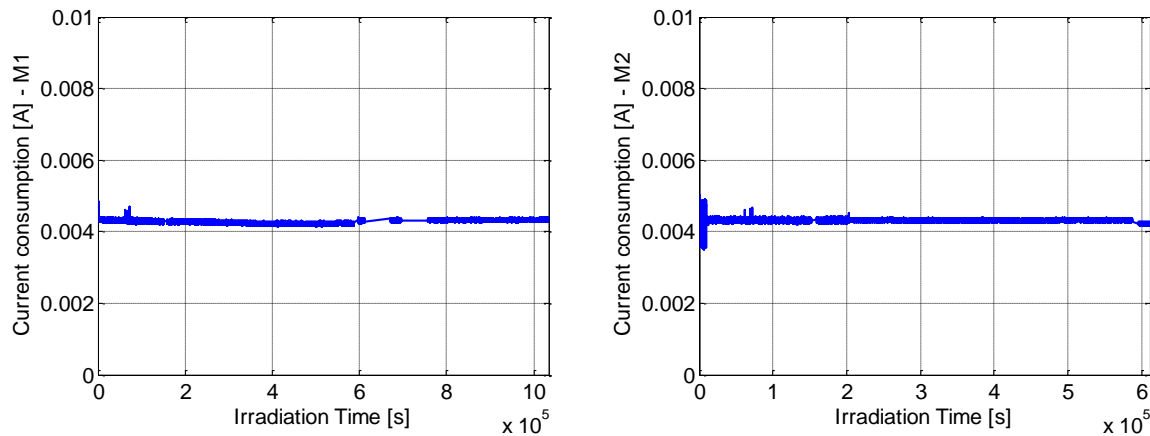


Figure 67: Evolution of the current consumption of the two memories all along the irradiation. The plot on the left (a) corresponds to the current consumption of the memory M1 and the plot on the right (b) corresponds to the current consumption of the memory M2.

Despite the absence of current increase on the memories, after irradiation, the memory n°1 was blocked in standby mode without any possibility to switch in idle mode. Therefore, after 120krad the memory was nonoperational.

III.4.3.2.2 *Response of ESD protection on power supply inputs*

Figure 68 presents the characterization of the power supply pins in voltage source mode before irradiation on the left and after irradiation on the right. As observed on those two graphics, the response

of the components is relatively similar except for the triggering voltage that has shifted from 8.9V to 8.7V corresponding to a difference of -0.2V.

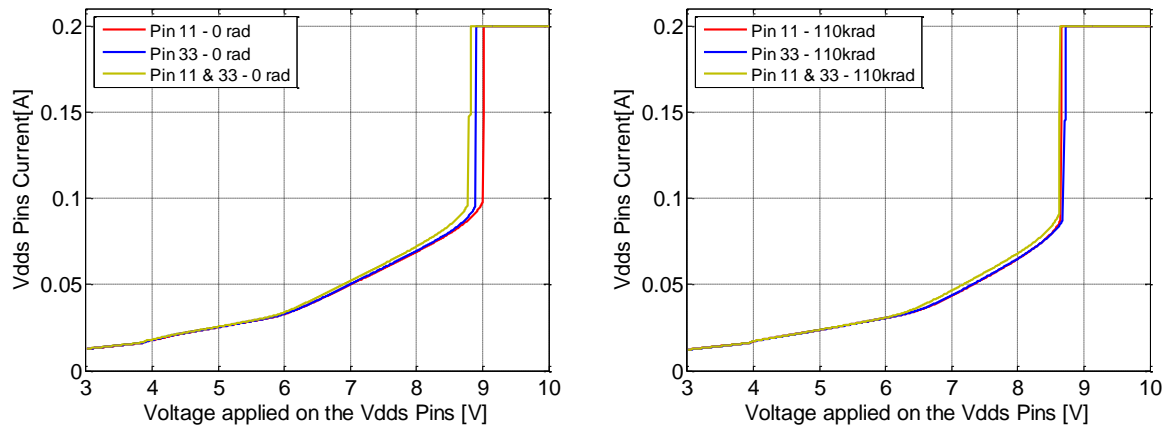


Figure 68: Characterization of the power supply pins in voltage source mode. The figure on the left presents the results of the characterization before irradiation and the figure on the right presents the results of the characterization after irradiation.

This behavior can be caused by the TID induced variation of the substrate resistance (more detail are given in Chapter 4).

Figure 69 presents the characterization of the power supply pins in current source mode before irradiation on the left and after irradiation on the right.

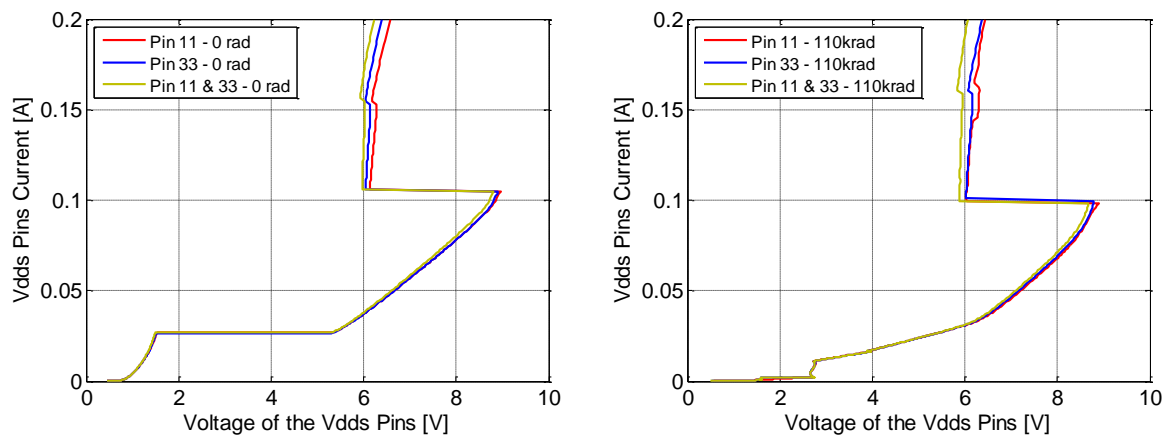


Figure 69: Characterization of the power supply pins in current source mode. The figure on the left presents the results of the characterization before irradiation and the figure on the right presents the results of the characterization after irradiation

As observed on this graphics, the triggering voltage observed seems to fit the results observed in Figure 22. Indeed, a very small difference is observed between the curve before and after irradiation. The only noticeable difference is for the current between 0V and 6V that have a completely different tendency. However, this difference is most probably mostly caused by the internal circuit of the component itself.

III.4.3.2.3 ESD protection response of signal inputs

Figure 70 corresponds to the characterization of different signal pins of the component before irradiation on the left and after irradiation on the right. As already explained previously, these curves are the results of the triggering of the ESD protection structure composed of several fingers. If we compare the curves before and after irradiation, the characterization of the component seems to be relatively similar because they exhibit almost the same triggering voltage, the same holding point and the same triggering of the others fingers.

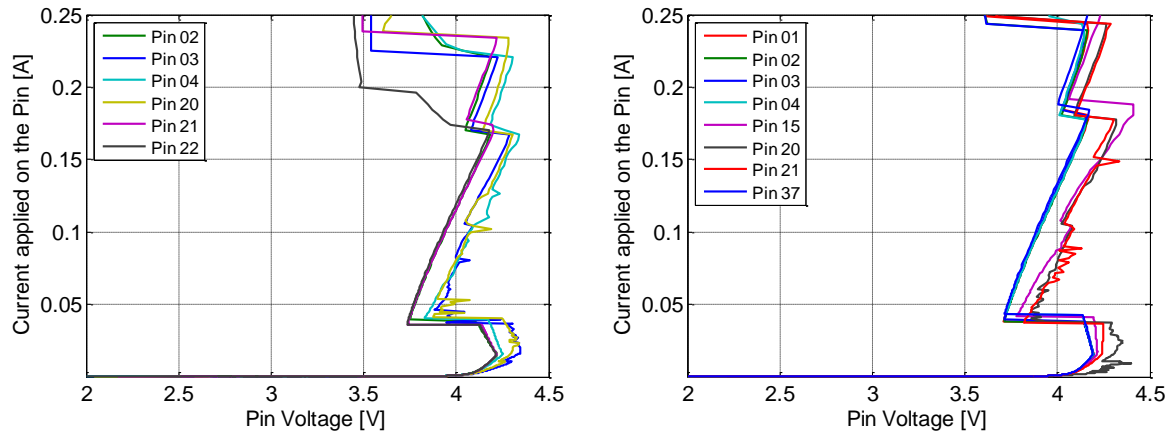


Figure 70: Characterization of the signal pins in current source mode in linear scale. The figure on the left presents the results of the characterization before irradiation and the figure on the right presents the results of the characterization after irradiation

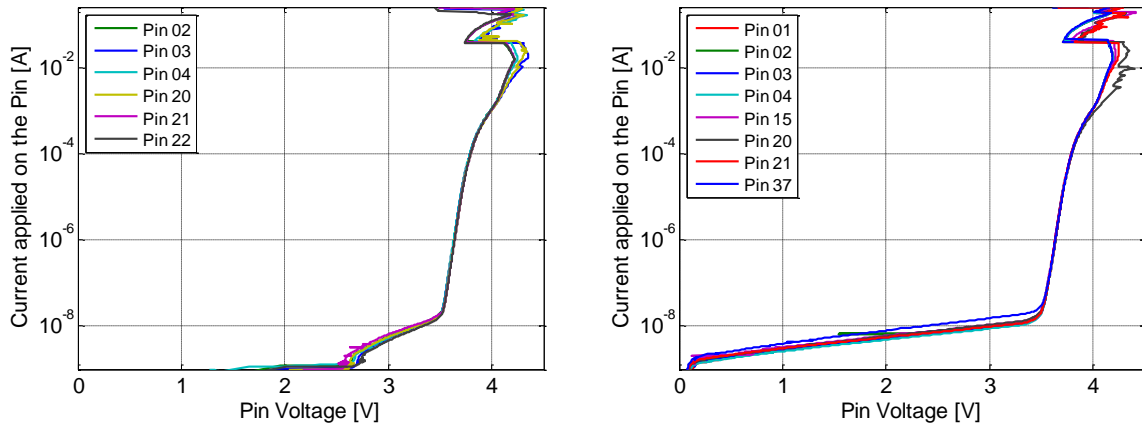


Figure 71: Characterization of the signal pins in current source mode in logarithmic scale. The figure on the left presents the results of the characterization before irradiation and the figure on the right presents the results of the characterization after irradiation

The Figure 71 presents the same plot as the Figure 70 but in logarithmic scale. They represent the leakage current of the different signals pins before and after irradiation. As observed, after a TID of 120 krad the current of the signal pin for a voltage below 3V increased. Before irradiation, because the

characterizations have been performed in current source mode starting from 1 nA no current below this point is available. However, we can still observe an augmentation of the current.

III.5. CONCLUSION

In this chapter, the assessment of the sensitivity of ESD protection to ionization was investigated.

As explained earlier ESD damages on electronic devices component cost each year billions of dollars of losses. Improvement in the technology has led to shrinking of the transistors dimensions, increasing their sensitivity ESD stress. Therefore, numerous ESD protections are nowadays implanted at the peripheral of the electronic components to protect them. Because of the protection methodology, ESD protections are implemented in large number inside the components.

Because of their similarity with a MOSFET transistor, the GGnMOS ESD protection structure was selected as component to study. Very few studies were carried out on that kind of structure, while their radiation-induced, degradation on those components could increase the leakage current, or alter the protection effectiveness of the ESD protection.

The point presented in this chapter allows in determining to determine if a component is still protected after TID irradiation and if the current leakage increases, causing a large increase all over the device considering the number of ESD protection inside a single component.

It is very difficult to find standalone GGnMOS protection and it is difficult to know if an electronic component is designed with this structure. Therefore, we have attempted to understand, by using a MRAM memory, if we are able to identify the type of ESD protection at first, and second, if the degradation of the ESD protection would overtake the degradation of the internal circuit of the component itself to observe only the degradation of the ESD protection.

The irradiations carried out at CERN on this memory have shown that the ESD protection embedded does not show any degradation. A variation of the leakage current was observed, however, nothing proves that the degradation comes from the ESD protection itself and no significant variation of the ESD triggering voltage was observed.

Therefore, this chapter shows that it is very difficult to evaluate the ESD protection already embedded inside a component because the radiation-induced degradation can degrade the component and the ESD protection at the same time. Therefore, the study of a standalone ESD protection was needed.

The next chapter presents the investigation performed on a GGnMOS structure. Thanks to a collaboration with Microchip Technology Nantes, we had access to technological data on GGnMOS structure. Those data helped us to understand the degradation of those structures via simulations and theoretical analysis.

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IV.1. INTRODUCTION

In the previous chapter, different ESD protection structures that can be used in integrated circuits were introduced. Due to their massive implementation in integrated circuits, it is important to understand how they could be affected by a possible total ionizing dose induced degradation and this in two different ways: (1) could this degradation affect the ability of the structure to protect the device against ESD; (2) could the radiation-induced degradation of the GGnMOS structures impact on the device's electrical and functional parameters.

At first, an MRAM¹³ memory was used as a test vector to observe the degradation of its ESD protection structures within the component. The challenge of these tests was to understand if it is possible to measure the degradation of this embedded structure, and more important if the radiation-induced degradation of that structure would prevail over the internal degradation of the memory itself.

After irradiation, it was shown that the memory did not exhibit any large variation in the triggering voltage or in the leakage current. Thus, with a black box approach, it was very difficult to understand where the observed degradation came from.

Thanks to a collaboration with Microchip Technology Nantes, we had access to the technological data of GGnMOS structures, which were implemented in ECORCE TCAD software. However, because no standalone GGnMOS structure was available for irradiation, no comparison between simulated results and manipulation was performed. On the one hand, it is difficult to test the embedded GGnMOS structures without proper equipment. On the other hand, their triggering mechanism using impact ionization makes it difficult for the simulations to converge properly. Therefore, in this study, a theoretical approach only was considered.

Figure 72 presents on the left a GGnMOS structure and on the right an LDMOS structure. As observed, both components share a similar structure composed of a STI and a buried oxide surrounding a P doped area, encircled in red in Figure 1. From this point of view, LDMOS structures can be considered as very similar to the GGnMOS. Radiation test of these LDMOS structures were already performed by Microchip Technology Nantes. It was then decided to study the LDMOS structures in ECORCE, assuming that the mechanisms leading to the radiation-induced degradation were similar. Then the results obtained were applied to extrapolate the degradation of the GGnMOS structure.

¹³ MRAM : Magnetoresistive Random Access Memory

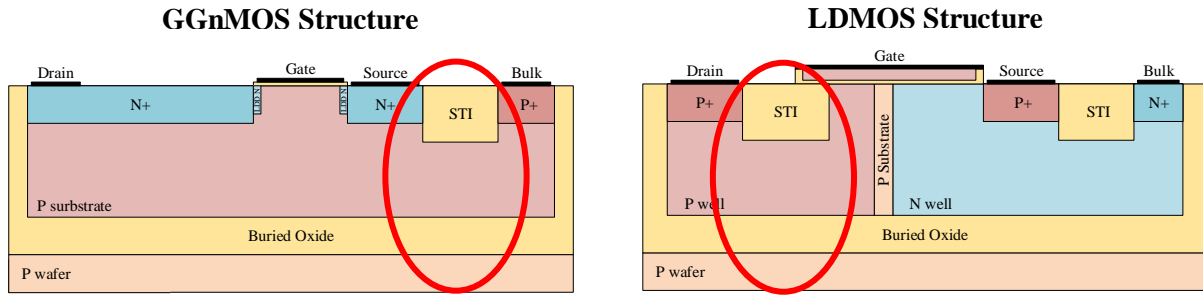


Figure 72: Representation of the simplified cross-section of a GGnMOS structure on the left, and an LDpMOS on the right. The part highlighted in red represents the sensitive part to TID to be studied.

An introduction of the TCAD software used is presented as the first part of this chapter. ECORCE is a software, developed at the University of Montpellier in the RADIAC team of the *Institut d'Electronique et des Systèmes* laboratory (stands for Electronics and Systems Institute), which we largely used to perform the studies. Because this software is relatively new, it is important to present the different calculations methods and the overall potential of this software.

The second part of this chapter presents the analysis performed on the LDMOS structures built with STI oxide and using a SOI substrate, with deep BOX [1], subject to total ionizing dose. In order to understand the degradation mechanism at play, the details and results of the TID test campaign are presented, followed by a presentation of the device structure and the TCAD simulations performed. In order to obtain accurate simulation results, a fit of the model had to be performed. The final results show how TID affects STI and BOX oxides, and how they alter the LDMOS characteristics.

Then, the third part of this chapter presents the study performed on the GGnMOS structure. In order to determine if the radiation-induced degradation of this ESD protection may jeopardize an electronic system by increasing the leakage current or by being no longer able to protect against ESD, a full analysis of this structure was performed through both theory and simulation. To start with, the device structure and simulation model are described. Then, the theoretical analysis of the failure mechanisms expected is presented. Finally, the last section describes the different results obtained by simulation and explains the mechanism at play in the TID-induced degradation of the GGnMOS structures.

IV.2. SIMULATIONS WITH ECORCE SOFTWARE

IV.2.1. PRESENTATION

ECORCE (in French: *Etude du Comportement sous Radiation des Composants Electroniques*, stands for *Study of electronic devices behavior under irradiation*) aims at modeling the behavior of the semiconductor-based electronic components and their response to radiation [2]. Indeed, this software models single event transients and the total ionizing dose in any semiconductor-based technology (Mosfet, capacitor, bipolar).

This software is based on various fundamental equations of the semiconductor physics:

- Drift-Diffusion equations, which calculate the transport of the charge carriers into the semiconductors using Poisson and holes and electrons transport equations.
- Trapping-Detrapping equations, which determine the charge trapping and charge detrapping into the oxides during irradiation using the MTD (Multiple Trapping-Detrapping) model.
- Heating equations, which define the temperature at any point of the mesh to understand the thermal behavior of semiconductor-based electronic component using the standards equation of thermal exchange.

This software is currently developed by Dr. A. Michez in the RADIAC [3] (RADIAtion and Components) team at the IES (in French: *Institut d'Electronique et des systèmes*, stands for *Institute of Electronics and Systems*) held by the University of Montpellier in France. It contains more than 85,000 coding lines and 67,000 comment lines. The evolution of this software is followed by a subversion software (SVN) developed by Apache [4]. Each section of the code was implemented separately in order to facilitate the creation of the modification of the physical laws. ECORCE is written in C++ and uses powerful libraries such as a library to automatically derivate nonlinear equations, SparseLib++ to solve linear equation systems, Qt5 for the graphical interface and Coin3D to define the geometry of the device graphically and plot the model the results.

Figure 73 introduces the development environment of ECORCE with QtCreator for the carrier recombination. A special care is taken to the readability of the code with explicit variable names and the additional comments and Doxygen type tag [5].

Figure 74 presents the graphical interface of ECORCE. This picture can be divided into three parts. On the left, the side panel is used to configure and select all the different items to be displayed on the component; the middle part of the screen is the graphical representation of the component; on the right, the side panel shows all the graphical information.

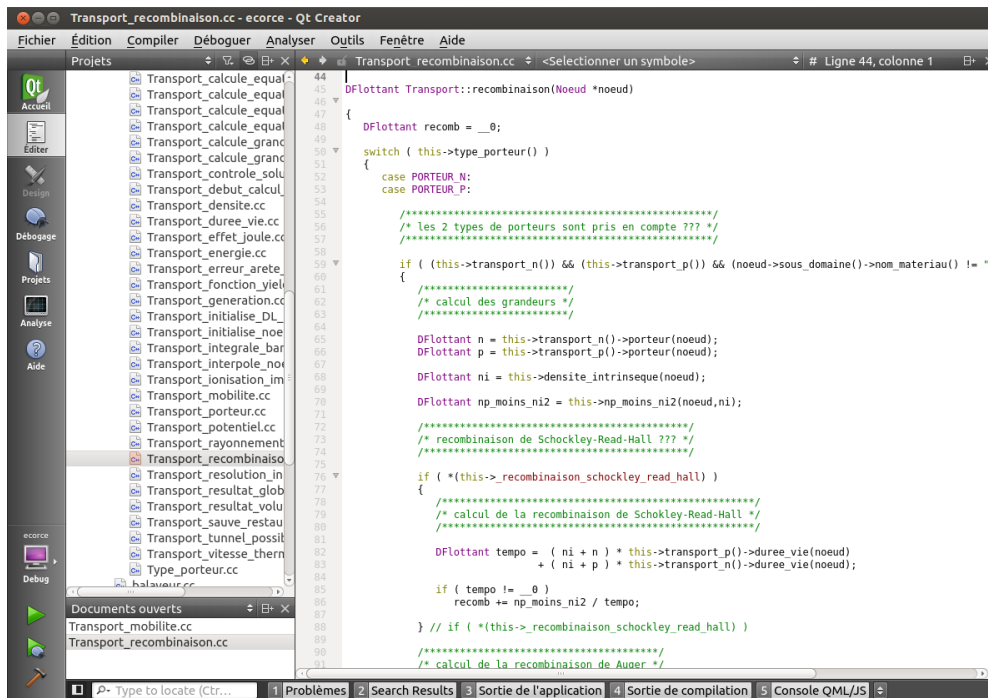


Figure 73: ECORCE development: Documentation and organization of the code for carrier recombination

ECORCE is based on the finite element method which is used to discretize and solve the Drift-Diffusion Model (DDM) with Poisson's equation (allow to compute the electrostatic potential distribution) and the continuity equations (calculating the electrons and holes concentration).

This TCAD software integrates a dynamic meshing that automatically adapts to describe optimally the gradient of the different variables (potential, carrier density, etc.) for each calculation step in stationary or transient analysis mode. The dynamic meshing adds and removes nodes all along the modeling process to minimize the discretization errors and improve the calculation time. Therefore, the user does not have to take care of the meshing quality and refinement to perform the simulation. By only specifying the precision the user wishes to obtain, the mesh size is automatically modified according to the requirements (polarizations, irradiations, etc.).

As seen in the previous chapters, the radiation effects are divided into two categories such as the cumulative effects and the Single Event Effects (SEE). Cumulative effects are related to the ionizing rays (TID) and non-ionizing rays (Displacement Damage). The TID induces a charge trapping into the oxides, which leads to a degradation of the electronic properties of the electronic components such as a voltage threshold drift for the MOSFET transistors or the decrease in current gain for the Bipolar Junction Transistors. Single events are caused by a single highly energetic particle that deposits its energy all along of its trajectory into the silicon. The understanding of these mechanisms and the radiation-induced degradation remain nowadays a serious technological challenge. Therefore, the development of simulation software able to visualize and understand the different induced physical mechanisms is very helpful to harden or develop mitigations techniques.

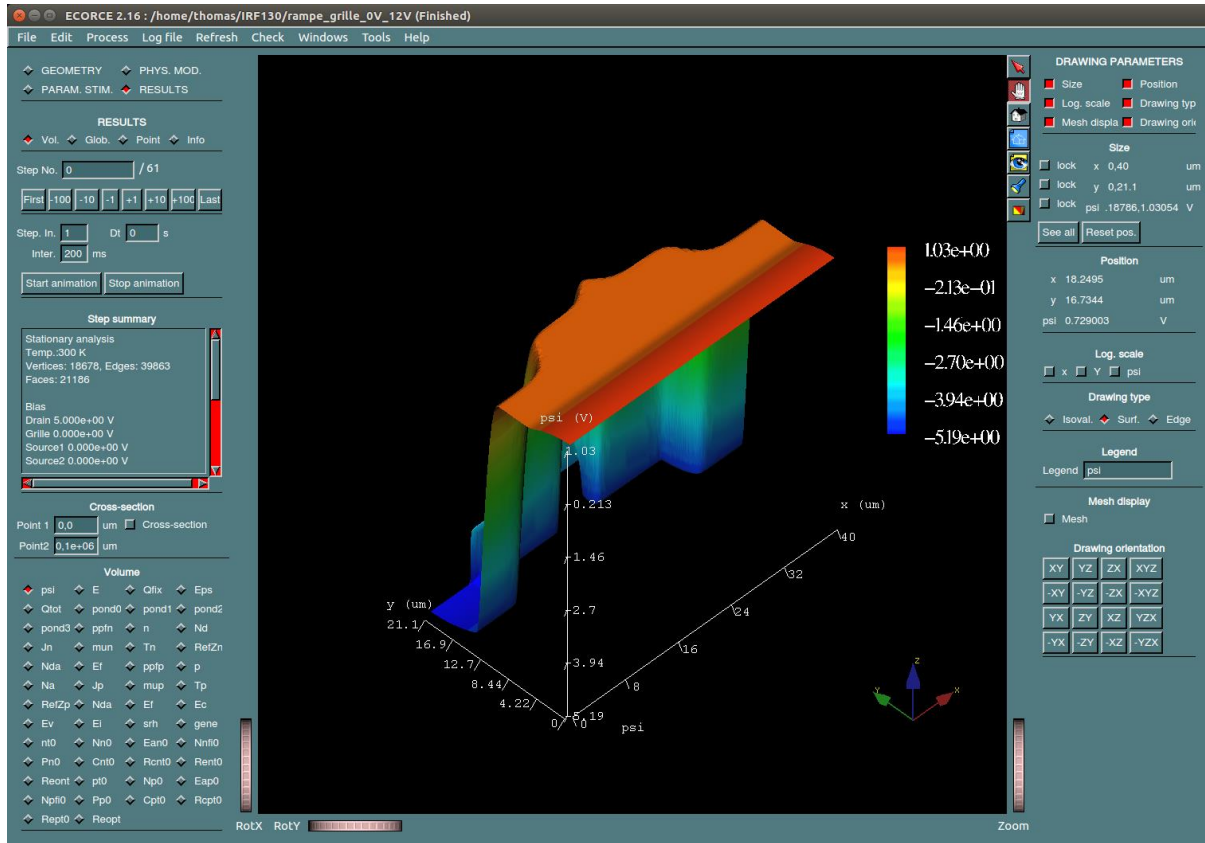


Figure 74: Graphical interface of ECORCE showing the electrostatic potential of a power MOSFET transistor

In the following section, the different physical laws used in the development of ECORCE are presented.

IV.2.2. PHYSICAL MODEL

ECORCE software is based on several fundamental equations of the semi-conductor physics such as the drift-diffusion equations, the trapping-detraping equations, and the heating equations. With the graphical interface, as presented in Figure 75, it is possible to select which fundamental equation to use for the simulations. In this figure, the area highlighted by a red rectangle correspond to the selection of different equations with “ ψ ” corresponding to the Poisson’s equation, “ T ” to the heating equations, “ n ” and “ p ” to the drift-diffusion equations and “ nt ” and “ pt ” to the trapping-detraping equations.

All the equations as presented and explained in the following subsection.

IV.2.2.1 Drift-Diffusion equations (Poisson, holes and electrons transport)

The drift-diffusion model [6] calculate the charges carriers diffusion into the semiconductors by resolving Poisson’s equations and electrons/holes transport with boundary condition specified.

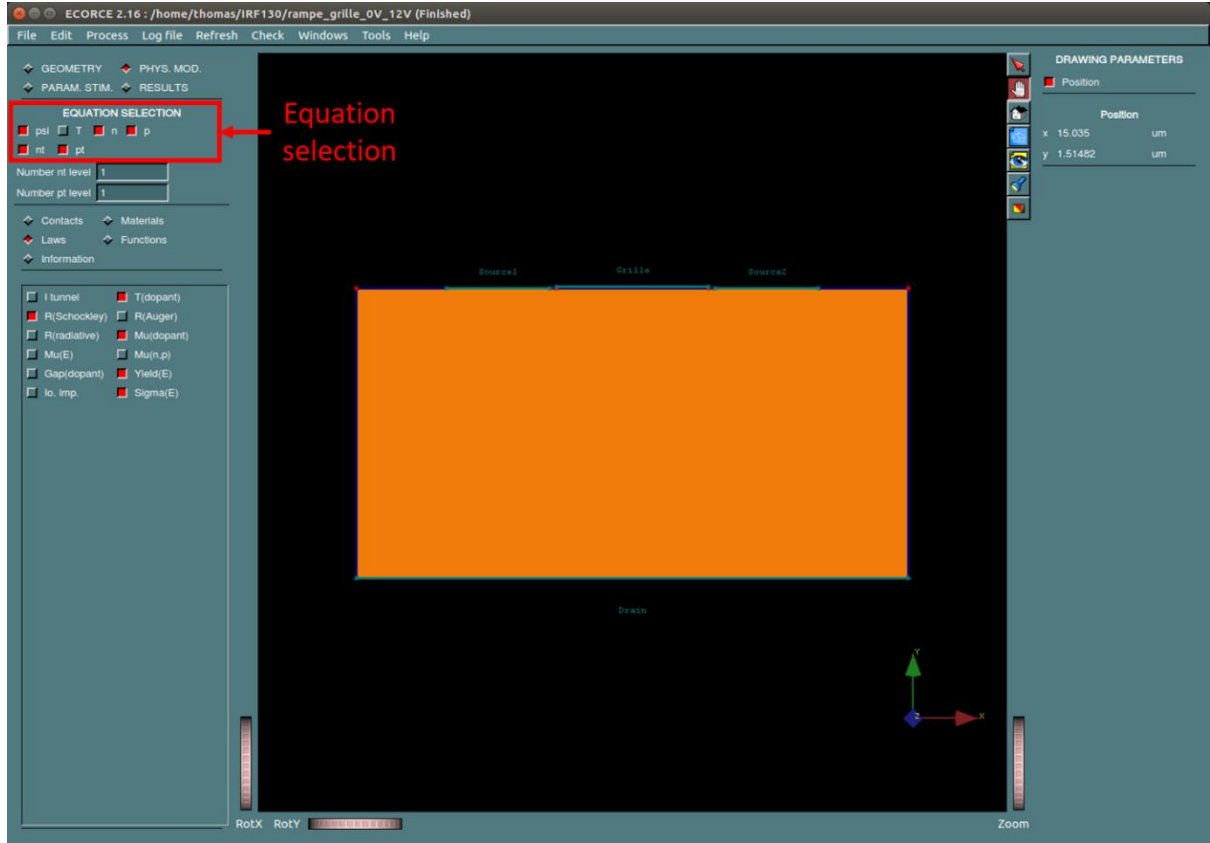


Figure 75: Graphical interface of ECORCE showing the different equations that can be selected. “psi” (Poisson’s equations), “T” (heating equations), n and p (diffusion-conductions equations), “nt” and “pt” (trapping-detraping equations)

IV.2.2.1.1 Calculation of the electrostatic potential ψ : Poisson’s equations

Poisson’s equations calculate the electrostatic potential distribution in each point of the mesh and describe the electric behavior of electronic component semiconductor-based. This law states that the number or n and p carriers have to be kept into a volume. After Maxwell’s equations, we know that:

$$\vec{\nabla} \cdot \vec{D} = Q \text{ and } \vec{D} = \epsilon \cdot \vec{E} \quad \text{Equation IV.2-1}$$

Where \vec{D} is the displacement vector, Q the total charge concentration [C/m^3], ϵ the permittivity ($\epsilon = \epsilon_r \cdot \epsilon_0$) and E the electric field. By combining those two equations, we obtain:

$$\vec{\nabla} \cdot \epsilon \cdot \vec{E} = Q \text{ or } \vec{E} = -\vec{\nabla} \psi \quad \text{Equation IV.2-2}$$

Where ψ is the electrical potential. Hence:

$$\nabla^2 \psi = -\frac{Q}{\epsilon} \quad \text{Equation IV.2-3}$$

The total electrical charge density Q is expressed as following:

$$Q = q \times (p - n + N_A^- - N_D^+) \quad \text{Equation IV.2-4}$$

Where q is the elementary charge [C], n and p respectively the electron and hole concentrations [m^{-3}], N_A^- the charge impurity of acceptors [m^{-3}] and N_D^+ the charge impurity of donors [m^{-3}]. Therefore, Poisson's equation is written as following:

$$\nabla^2 \psi = -\frac{Q}{\varepsilon} = -\frac{q}{\varepsilon} \times (p - n + N_A^- - N_D^+) \quad \text{Equation IV.2-5}$$

IV.2.2.1.2 Calculation of the electrons and holes concentration: Transport equation

The transport equation (or Continuity equation) of holes and electrons calculate their concentration at each point of the mesh. There are extracted following:

$$q \frac{\partial n}{\partial t} = \text{div} \vec{J}_n + q(G - R) \quad \text{Equation IV.2-6}$$

$$q \frac{\partial p}{\partial t} = -\text{div} \vec{J}_p + q(G - R) \quad \text{Equation IV.2-7}$$

With,

$$\vec{J}_n = qn\mu_n \vec{E} + qD_n \vec{\nabla} n \quad \text{Equation IV.2-8}$$

$$\vec{J}_p = qp\mu_p \vec{E} - qD_p \vec{\nabla} p \quad \text{Equation IV.2-9}$$

Where, for the electrons n , J_n , μ_n and D_n (same as p , J_p , and D_p for the holes) corresponds to the electron density, electron current density, and electron mobility and distribution coefficient of the electrons.

When an electric field \vec{E} is applied, it creates a displacement of the charge carriers. Whereas the conduction velocity depends on the electric field and the temperature. Moreover, those equations also depend on the electron and holes mobility, the diffusion coefficient bounded by the mobility of Einstein's relationship: $D_n/\mu_n = kT/q$ for the electrons and $D_p/\mu_p = kT/q$ for the holes. In addition, the electrons-holes generation rate G caused by ionization [7], [8] and the recombination rate R of the electrons-holes pairs related to the Shockley-Read [9] and Auger [10] equations have an important role.

Under irradiation, the generation rate of electron-hole pairs resisting to the initial recombination depends on the electric field. This phenomenon is taken into consideration with the *Yield* function [11], [12].

IV.2.2.2 Trapping-Detrapping equations for the oxides

The energy diagram presented in Figure 76 describes the charge trapping-detrapping phenomenon into the oxides implemented in ECORCE [13], [14]. The energy traps distribution into the oxide gaps can be represented by a set of level K for the electrons and level L for the holes. Both sets can be characterized by their activation thermal energy labeled as E_n for the electrons and E_p for the holes. Each trap level adds another equation to the drift-diffusion model. The interactions presented in Figure 76 represents:

- 1- The electron-hole pair generation caused by radiation,
- 2- The carrier drift in their respective bands,
- 3- The trapping of free carriers,
- 4- The recombination of trapped carriers by their free opposite carriers,
- 5- The thermal re-emission of trapped carriers in their respective bands.

The exchange of carriers between the level of the trap can be permitted only through their respective energetic bands. This model is known as the Multiple Trapping-Detrapping Model (MTD) [15]. An electron trap level is called acceptor (negatively charged when occupied by an electron) and a hole trap level is called donor (positively charged when occupied by a hole).

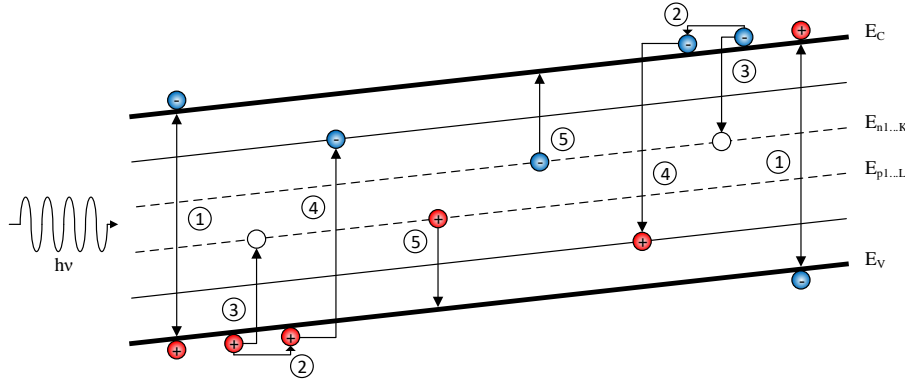


Figure 76: Interactions describing the charge trapping-detrapping model in the oxides [15]

For each electron trap level, ECORCE solves the following equations:

$$q \frac{\partial n_t^{(i)}}{\partial t} = C_n^{(i)} - Rec_n^{(i)} - Ree_n^{(i)} \quad \text{with:} \quad \text{Equation IV.2-10}$$

$$C_n^{(i)} = \sigma_{n_t}^{(i)} (N_n^{(i)} - n_t^{(i)}) (|\vec{J}_n| + J_{thn}) \quad \text{Equation IV.2-11}$$

$$Rec_n^{(i)} = \sigma_{p_r}^{(i)} n_t^{(i)} (|\vec{J}_p| + J_{thp}) \quad \text{Equation IV.2-12}$$

$$Ree_n^{(i)} = q R_n^{(i)} n_t^{(i)} \quad \text{Equation IV.2-13}$$

$$J_{thn} = q n v_{thn} \quad \text{Equation IV.2-14}$$

$$J_{thp} = q p v_{thp} \quad \text{Equation IV.2-15}$$

$$R_n^{(i)} = \sigma_{n_t}^{(i)} v_{thn} N_c e^{-q(E_c - E_n^{(i)})/kt} \quad \text{Equation IV.2-16}$$

For each hole trap level, ECORCE solves the following equations:

$$q \frac{\partial p_t^{(j)}}{\partial t} = C_p^{(j)} - Rec_p^{(j)} - Ree_p^{(j)} \quad \text{with:} \quad \text{Equation IV.2-17}$$

$$C_p^{(j)} = \sigma_{p_t}^{(j)} (N_p^{(j)} - p_t^{(j)}) (|\vec{J}_p| + J_{thp}) \quad \text{Equation IV.2-18}$$

$$Rec_p^{(j)} = \sigma_{n_r}^{(j)} p_t^{(j)} (|\vec{J}_n| + J_{thn}) \quad \text{Equation IV.2-19}$$

$$Ree_p^{(j)} = q R_p^{(j)} p_t^{(j)} \quad \text{Equation IV.2-20}$$

$$J_{thp} = q n v_{thp} \quad \text{Equation IV.2-21}$$

$$J_{thn} = q p v_{thn} \quad \text{Equation IV.2-22}$$

$$R_p^{(j)} = \sigma_{p_t}^{(j)} v_{thp} N_v e^{-q(E_v - E_p^{(j)})/kt} \quad \text{Equation IV.2-23}$$

For the electrons, $n_t^{(i)}$, $\sigma_{nt}^{(i)}$ and $N_n^{(i)}$ (same as $p_t^{(j)}$, $\sigma_{pt}^{(j)}$ and $N_p^{(j)}$, for the holes) respectively define the trapped charge carriers density, the trapping cross-section and the electrons density. As for the trapped carriers recombination cross-section and the energy level of electrons on the level i (and j for the holes) are defined by $\sigma_{pr}^{(i)}$ and $E_n^{(i)}$ for the electrons and $\sigma_{nr}^{(j)}$ and $E_p^{(j)}$ for the holes. Moreover, for the electrons, v_{thn} , N_c and E_c (same as v_{thp} , N_v , and E_v for the holes) respectively define the thermal velocity, the state density in the allowed band and the energy level in the allowed band for the electrons.

To take into account those traps level, the total electrostatic charge Q and the continuity equations become:

$$Q = \left(Q_{fix} + N_d - n - N_a + p - \sum_{i=1}^k n_t^{(i)} + \sum_{j=1}^l p_t^{(j)} \right) \quad \text{Equation IV.2-24}$$

$$q \frac{\partial n}{\partial t} = \text{div} \vec{J}_n + qG - \sum_{i=1}^k C_n^{(i)} - \sum_{j=1}^l Rec_p^{(j)} + \sum_{i=1}^k Ree_n^{(i)} \quad \text{Equation IV.2-25}$$

$$q \frac{\partial p}{\partial t} = -\text{div} \vec{J}_p + qG - \sum_{j=1}^l C_p^{(j)} - \sum_{i=1}^k Rec_n^{(i)} + \sum_{j=1}^l Ree_p^{(j)} \quad \text{Equation IV.2-26}$$

This model takes into consideration the trapping variation cross-section, the recombination depending on the electric field and the reduction of the activation energy of holes depending on the electric field, known as the Poole-Frenkel effect.

In addition, the drift-diffusion model considers as well the thermal conductivity variation depending on the temperature and the variation of the carrier mobility depending on the dopant concentration, electric field, and free carrier density.

IV.2.2.3 Heating equations (temperature calculation)

The heat equation [16] calculate the temperature at each point of the mesh and allows to describe the thermal behavior of electronic component semi-conductor based. The equation is written as follow:

$$\nabla^2 T = \frac{1}{D} \frac{\partial T}{\partial t} - \frac{P}{\lambda} \quad \text{with} \quad D = \frac{\lambda}{\rho c_p} \quad \text{Equation IV.2-27}$$

Where T is the temperature in Kelvin, D the thermal diffusivity, P the thermal power generated per volume unit [W.m^{-3}], λ the thermal conductivity [$\text{W.m}^{-1}.\text{K}^{-1}$], ρ the density [kg.m^{-3}], and c_p the thermal capacity of the material [$\text{J.kg}^{-1}.\text{K}^{-1}$].

The generated thermal power per volume unit P depends on the equation selected by the user. If all of the equations of the drift-diffusion model are selected, the generated thermal power by volume unit P can be written as follow:

$$P = P_{fix} + \vec{E} \cdot \vec{J}_n + \vec{E} \cdot \vec{J}_p \quad \text{Equation IV.2-28}$$

Where P_{fix} corresponds to a fixed thermal power defined by the user.

IV.2.2.4 Selections of the physical laws

In order to select the laws to use during the simulation, ECORCE propose a menu in the graphical interface, as presented in Figure 77, that allow to enable or disable different laws such as the tunneling current, the lifetime depending on the dopant, the Shockley Read Hall recombination, the Auger recombination, the radiative recombination, the mobility depending on the dopant, the mobility depending on the electric field, the mobility depending on the doping concentration, the gap depending on the dopant, the initial recombination and the impact ionization.

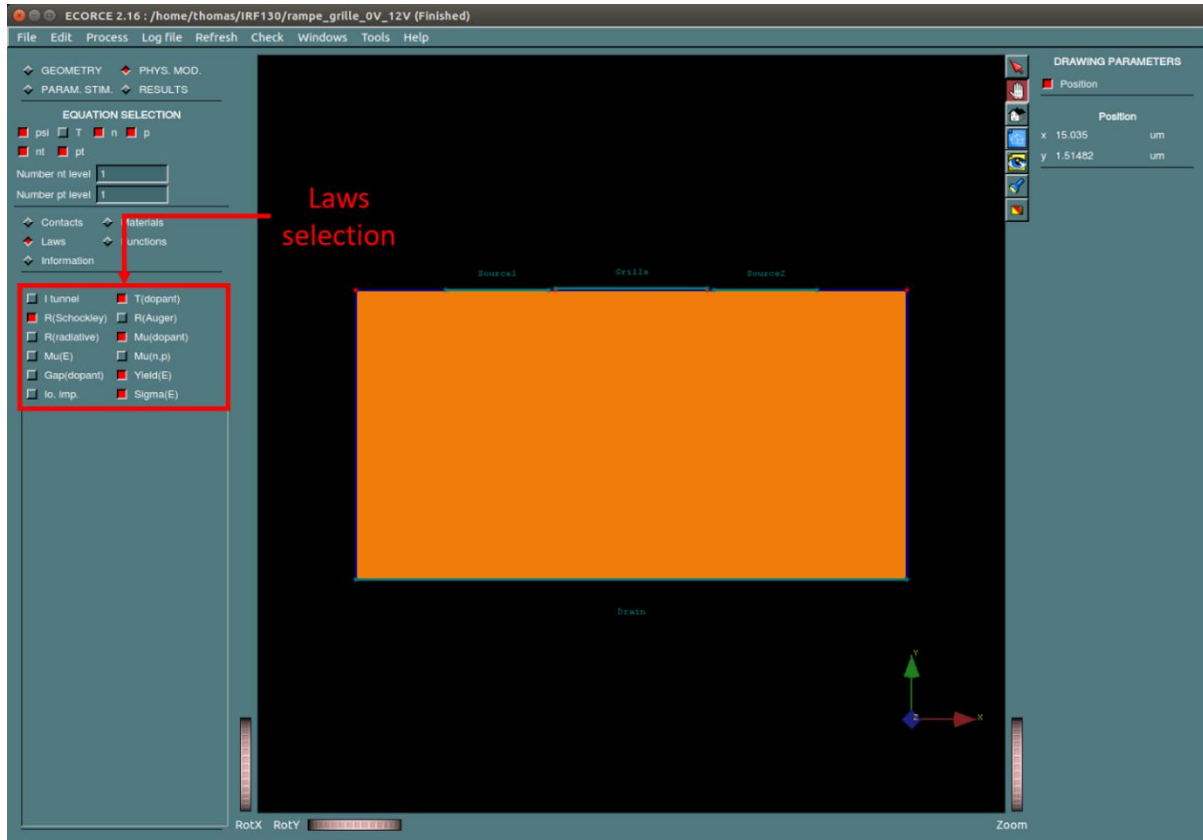


Figure 77: Graphical interface of ECORCE showing the different laws that can be selected. “I tunnel” corresponds to the tunneling current. “T(dopant)” corresponds to the lifetime depending on the dopant. “R(Shockley)” corresponds to the Shockley Read Hall recombination. “R(Auger)” corresponds to the Auger recombination. “R(radiative)” corresponds to the radiative recombination. “Mu(dopant)” corresponds to the mobility depending on the dopant. “Mu(E)” corresponds to the mobility depending on the electric field. “Mu(dopant)” corresponds to the mobility depending on the doping concentration. “Gap(dopant)” corresponds to the gap depending on the dopant. “Yield” corresponds to the initial recombination. “Io. Imp” corresponds to the impact ionization.

IV.2.3. NUMERICAL DISCRETIZATION METHODS

The equations are discretized spatially with the Box method and temporally with the Gear method. The discretized set of non-linear equations is then solved by the Raphson-Newton method. Depending on equations stiffness, solving non-linear system can be touchy. Furthermore, the Raphson-Newton method is sensitive to discontinuities in the derivatives of space-time equations.

IV.2.4. DYNAMIC MESHING

IV.2.4.1 Theory of the dynamic meshing

Various complex models have been developed over the years to consider radiation-induced degradation on electronic components. However, to solve the differential equations describing the behavior of semiconductor-based electronic devices it is necessary to discretize them since no analytical solution is known for most problems. The finite volume/finite element method is usually used to perform this kind of discretization. It consists in breaking down the geometrical domain into elements.

The degrees of freedom express the number of independent equations (Ψ , T , n , p , etc.) associated with all nodes of the mesh. Typically, the degrees of freedom are supposed to vary linearly within the element. This approximation is correct as long as the gradient is small enough between two consecutive elements. If, due to a coarse meshing, the gradient of degrees of freedom is not well defined, the results from the discretized equations can be very different from the results of the differential equation.

Each element is represented by a mesh constituting a meshing. A mesh is composed of nodes, edge, and faces as described in Figure 78. Each mesh (of faces) can be rectangular or triangular. The dynamic meshing prevents the creation of an obtuse angle triangle that is known to generate inaccurate results and numerical instabilities. Therefore, the meshing algorithm developed in ECORCE creates triangles with all angles below 90° and ensure that no obtuse angles exist among the mesh.

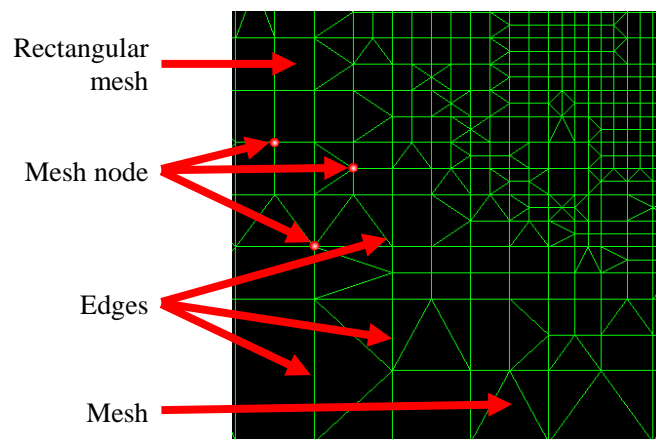


Figure 78: Presentation of the meshing used in ECORCE

ECORCE's dynamic meshing requires four parameters set by the user in the graphical interface as presented in Figure 79. Two parameters (maximum edge length and minimum edge length) drive the lowest and highest size of edges.

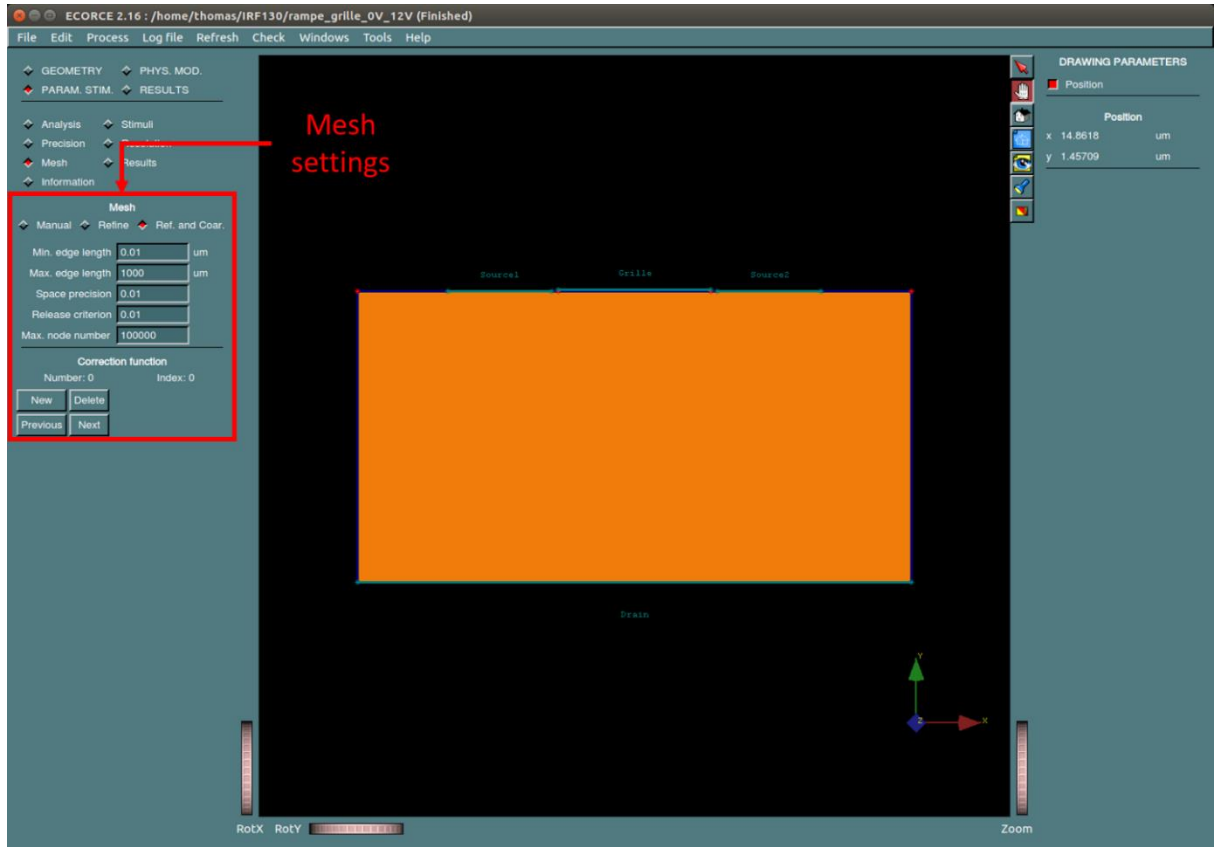


Figure 79: Graphical interface of ECORCE showing mesh settings that can be configured.

The space precision (P_{refine}) and the release criterion (P_{release}) are the two others parameters that also define the refinement and release of the mesh depending on the degrees of freedom gradient.

To correct the mesh, the error induced by the linear interpolation on one edge needs to be estimated. This estimation can be done by calculating the value in the middle of the edge using a quadratic interpolation and comparing with the same value calculated with a linear interpolation [17].

Interpolating value in the middle of the edge 32 assuming a linear interpolation between nodes 2 and 3 gives:

$$V_{32} = \frac{V_3 + V_2}{2} \quad \text{Equation IV.2-29}$$

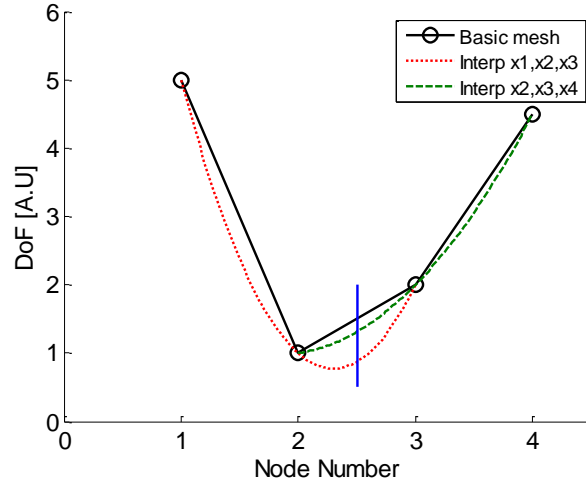


Figure 80: Quadratic interpolation on nodes 1, 2, 3 (red dotted line) and on node 2, 3, 4 (green dashed line). Differences between linear and quadratic interpolations are computed at the point $x_m = (x_2 + x_3)/2$ (blue line).

Interpolating the same value assuming a quadratic interpolation between nodes 1, 2, 3 (red dotted line in Figure 80) and between nodes 2, 3, 4 (green dashed line in Figure 80) gives:

$$V_{321} = L_1(x_m)V_1 + L_2(x_m)V_2 + L_3(x_m)V_3 \quad \text{Equation IV.2-30}$$

$$\text{With } L_i(x) = \prod_{j=1, j \neq i}^3 \frac{x - x_j}{x_i - x_j}$$

$$V_{432} = N_2(x_m)V_2 + N_3(x_m)V_3 + N_4(x_m)V_4 \quad \text{Equation IV.2-31}$$

$$\text{With } N_i(x) = \prod_{j=2, j \neq i}^4 \frac{x - x_j}{x_i - x_j}$$

$L_1(x)$, $L_2(x)$, $L_3(x)$ are the Lagrange polynomials of order 2 on nodes 1, 2, 3 and $N_1(x)$, $N_2(x)$, $N_3(x)$ are the Lagrange polynomials of order 2 on nodes 2, 3, 4.

Then the relative error of one DF on the edge 32 can be expressed by the maximum of the two differences:

$$E_{432}^{DF} = \max(E_{321}^{DF}, E_{432}^{DF}) \quad \text{Equation IV.2-32}$$

$$\text{With } E_{321}^{DF} = 2 \frac{|V_{321} - V_{32}|}{|V_{321} + V_{32}|} \quad \text{and} \quad E_{432}^{DF} = 2 \frac{|V_{432} - V_{32}|}{|V_{432} + V_{32}|}$$

In the end, with the four parameters defined in ECORCE, the conditions to refine one edge or merge two mesh are:

- Refine the mesh if :

$$(Length > Size_{max})OR((E_{edge} > P_{refine})AND(Length > 2Size_{min})) \quad \text{Equation IV.2-33}$$

Where Length and E_{edge} correspond to the edge length and the higher relative error for this edge.

- Merge two edges in one if:

$$\begin{aligned} & (E_{edge1} < P_{refine} * P_{release})AND(E_{edge2} \\ & < P_{refine} * P_{release})AND((Length_1 + Length_2) \\ & < Size_{max}) \end{aligned} \quad \text{Equation IV.2-34}$$

Where $Length_1$, $Length_2$, E_{edge1} , and E_{edge2} corresponds to the $edge_1$'s length; $edge_2$'s length, the higher relative error of $edge_1$ and the higher relative error of $edge_2$.

Low values of P_{refine} result in coarse meshes and low CPU time. High values of P_{refine} give finer meshes but higher CPU time and too high values of $P_{release}$ (more than 10%) can lead to oscillations between mesh refinement and release, increasing the CPU time for the mesh calculation. Too low values of $P_{release}$ limit the removal of nodes, increasing the CPU time [17].

Moreover, it is also possible to define a fixed meshing locally inside the mesh to increase the precision of the results. Therefore, the correction function overtakes locally the control of the meshing at the indicated position, and the rest of the meshing will still be defined by the dynamic meshing.

IV.2.4.2 Example of the dynamic meshing

To evaluate ECORCE dynamic meshing performances, we can compare the solutions obtained with a model for which an analytical solution is already known. As an example, consider the potential distribution induced by a fixed charge $Q(x)$ on a 1D device with a length of $1\mu m$.

$$Q(x) = Q_{max} \cdot e^{(-x/\sigma)} \quad \text{with} \quad \begin{cases} Q_{max} = q \times 10^{18} cm^{-3} \\ \sigma = 0.02 \mu m \\ q = 1.602 \times 10^{-19} C \end{cases} \quad \text{Equation IV.2-35}$$

In 1D, Poisson's equation, with an initial condition $\psi(0) = \psi(1 \mu m) = 0V$, becomes:

$$\frac{\partial^2 \psi}{\partial x^2} = -\frac{Q(x)}{\epsilon} \quad \text{Equation IV.2-36}$$

Therefore, this equation has for solution:

$$\psi = -\frac{Q_{max}\sigma^2}{\epsilon} \left[-e^{-\frac{x}{\sigma}} + \left(e^{-\frac{1}{\sigma}} - 1 \right) \times x + 1 \right] \quad \text{Equation IV.2-37}$$

The graphical representation of this equation is presented in Figure 81.

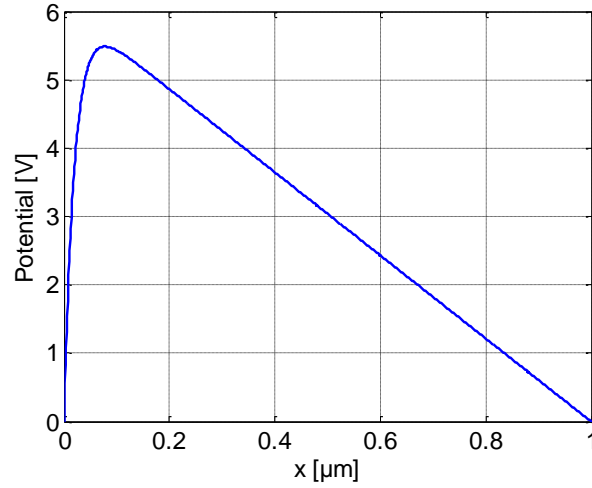


Figure 81: Analytical solution of the potential distribution induced by fixed charges $Q(x)$.

Figure 82 presents the relative error between the analytical solution calculated with the Equation IV.2-37 and several numerical solutions calculated with ECORCE.

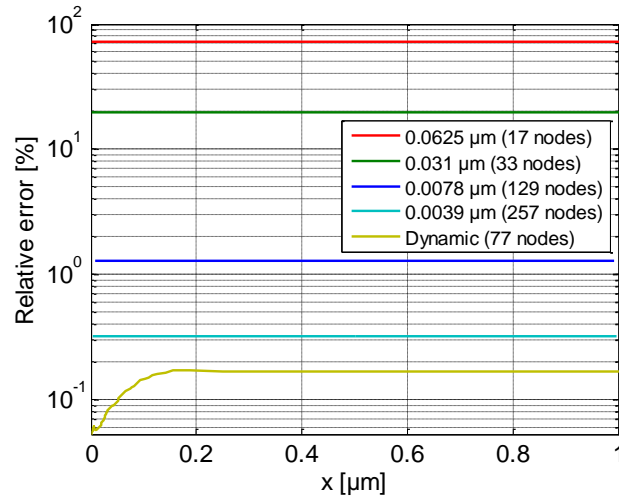


Figure 82: Relative error between the analytical solution and the numerical solution for several meshing sizes

The numerical solutions are tested with four different constant sizes of meshing such as 0.0625 μm , 0.03125 μm , 0.0078 μm and 0.0039 μm , and with a variable size mesh generated by the dynamic meshing of ECORCE. The mesh sizes computed by the dynamic mesh evolve between 4.8×10^{-4} and 0.25 μm . The final solution obtained with the dynamic mesh is from three to six times more precise, with fewer nodes than with a constant mesh of 0.0039 μm .

Various solutions have been proposed to correct automatically the meshing in a stationary mode such as the one presented in [18]. However, in transient mode, when important changes occur, for example when an ion passes through a device, the mesh size change drastically throughout the steps in order to follow the evolutions of the degrees of freedom. Indeed, during this kind of events, the ion trail will

extend radially and longitudinally and at each time step, the mesh must be refined in areas where the gradients increase to minimize the discretization error, and released in areas where the gradients decrease to reduce the computation time.

ECORCE works on a single mesh that is refined during the calculations (mesh subdivision) and/or released (mesh merge) according to the degrees of freedom gradient, at each step of the modeling in the stationary or transient analysis. When nodes are deleted and the degrees of freedom gradients are low, no interpolation is required to release the mesh. However, the degrees of freedom of the added nodes must be carefully interpolated in order to avoid local additions of errors on the electrical charge because it can create current peaks at the contacts. To solve this issue, after refining the mesh, ECORCE solves at first the equations on all the new nodes locking the degrees of freedom of the old nodes (Figure 83), and then it solves again the equations of the full mesh to improve the accuracy of the solution.

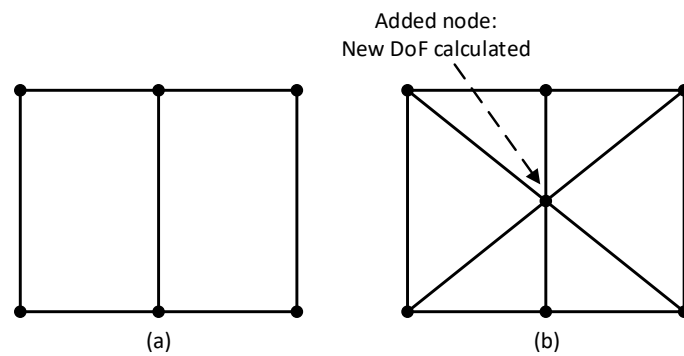


Figure 83: Element of the meshing. (a) Before refinement. (b) After refinement

The principle of the mesh creation in ECORCE for a transient modeling is describe in Figure 84. Starting from an initial coarse mesh, it subdivides or merges, depending on the gradients of the degrees of freedom (Ψ , T , n , p , etc.) until it reaches the precision defined by the user. The process is repeated for each time step/polarization step of the modeling to ensure the user's expected accuracy and optimize calculation times.

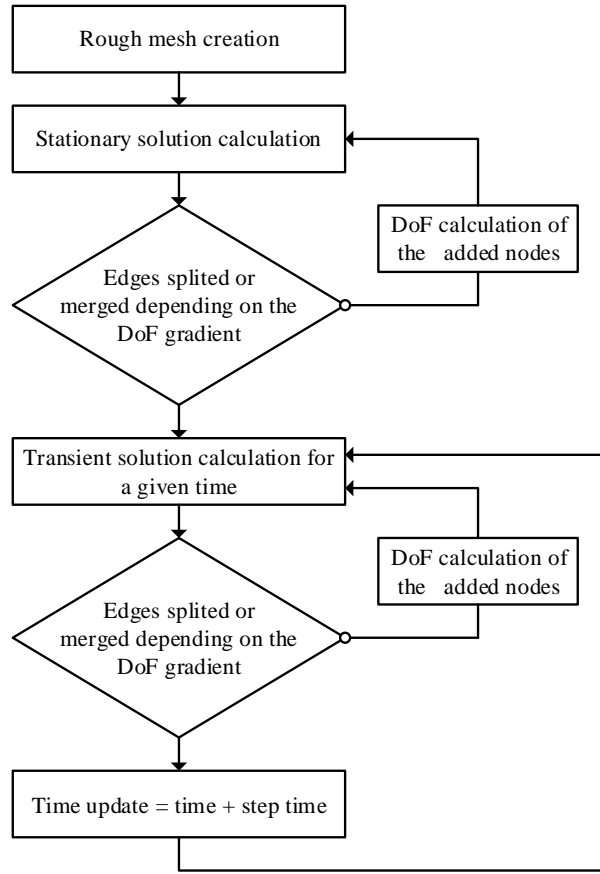


Figure 84: Principle of the mesh creation in ECORCE

In the case of a single event, as presented in [19], it is preferable to refine the meshing all along the ion trail before its passage. Thus, for each transient step, ECORCE checks if an ion passage is programmed at the considered time in order to refine automatically the mesh size.

In the next sections, we will be using ECORCE TCAD software to simulate the behavior of LDMOS and GGnMOS components under ionizing radiations and try to understand how it affects the characteristics of both structures.

IV.3. STUDY ON THE DEGRADATION OF A LDMOS STRUCTURE

IV.3.1. INTRODUCTION

The LDMOS transistor is by far the most common and used transistor for RF and power applications, which makes its proper functioning mandatory for every system. Moreover, for a satellite, RF communication is the only link between earth and space. In case of failure of the RF system, the whole spacecraft becomes useless.

Since the 80s, extensive studies have been performed on MOSFET technologies and have shown that charge trapping in the gate oxide was the main cause of the degradation [20]–[22]. Nowadays, improvements of the technology have led to the reduction of the technology node and thereby to a decrease in the oxide thickness (from > 100 nm to ~ 1 nm SiO₂ [23]). Thus, the impact of the charges trapped into the gate oxide does not prevail anymore over the impact of charges trapped into the isolation oxides. Trapped charges in the oxides such as the Shallow Trench Isolation (STI) or the Buried Oxide (BOX), have now to be taken into consideration because this effect may prevail on the gate oxide ones [24], [25].

Total Ionizing Dose (TID) irradiation performed by Microchip Technology Nantes (France) on LDMOS structures showed an unexpected degradation. Indeed, as most of the MOSFET-based component, it is expected to observe a shift of the triggering voltage of the component. However, another complete different degradation was observed. The devices under test were LDMOS structure with different voltages, type, and channel width dimensions, and the entire set of component showed a similar degradation. Therefore, in order to understand the origin of the degradation, the structure of the component was implemented in ECORCE TCAD software. After several models created and simulation, the origin of this unexpected degradation has been found.

This section analyses a LDMOS structure built with STI oxide and using a SOI substrate, with deep BOX [1], subject to TID. The devices can be isolated through deep trenches connected to the buried oxide. The STI oxide used inside the drain region of LDMOS is incorporated in order to increase the on-state and off-state breakdown voltages [26]. In order to understand the degradation mechanism of this structure, the section IV.3.2 presents the details and results of an experimental TID test campaign. Section IV.3.3 presents the device structure and the TCAD simulations model implemented in ECORCE. To use the model, an adjustment of the model had to be performed and is presented in the same chapter. The simulations result showing how TID affects STI and BOX oxides, and how they alter the LDMOS characteristics is then presented in section IV.3.4 with a comparison between experimental and simulated results.

IV.3.2. EXPERIMENTAL DETAILS AND RESULTS

IV.3.2.1 Devices under test

The devices under test (DUTs) used during the irradiation sessions are standard structures, P and N channel LDMOS PD-SOI 150nm mixed technologies from Microchip, designed for 25V (labeled as LDnMOS25V and LDpMOS25V) and 45V (labeled as LDnMOS45V and LDpMOS45V) operations. The tests were performed with three chips per channel type and operation voltage, and each part was composed of LDMOS with four different width dimensions. A summary of the number of components used is presented in Figure 85. The four different channel widths are represented by “W1”, “W2”, “W3” and “W4”. In the end, 48 components were tested.

LDMOS 25V								LDMOS 45V							
N Type				P Type				N Type				P Type			
W1	W2	W3	W4	W1	W2	W3	W4	W1	W2	W3	W4	W1	W2	W3	W4
#3	#3	#3	#3	#3	#3	#3	#3	#3	#3	#3	#3	#3	#3	#3	#3

Figure 85: Graphical representation of the number of components used during the TID test campaign

IV.3.2.2 Total Ionizing Dose Irradiation

TID experiments were performed at DCNS Indret (Nantes, France) using ^{60}Co γ -rays source. The dose rate was $182 \text{ rad}_{(\text{SiO}_2)} \cdot \text{h}^{-1}$ and three total doses were investigated were 30, 60, and 90 $\text{krad}_{(\text{SiO}_2)}$.

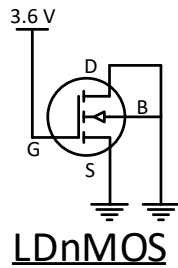


Figure 86: Biasing condition of the LDnMOS during the experimental and simulated irradiations

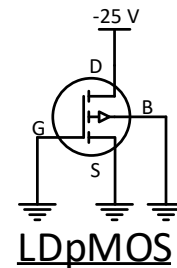


Figure 87: Biasing condition of the LDpMOS25V during the experimental and simulated irradiations

All the parts were irradiated at ambient temperature with the worst case biasing conditions. Figure 86 and Figure 87 presents the biasing conditions respectively of the LDnMOS and the LDpMOS during irradiation. For each LDnMOS, the gate was biased at 3.6V while the drain, source, and bulk contacts were biased at 0V. For each LDpMOS, the drain was biased at -25V for the LDpMOS25V while the gate, source, and bulk contacts were biased at 0V. These conditions have been defined as the worst case biasing after some preliminary irradiation sessions.

IV.3.2.3 Experimental Results

This study focuses on the investigation of the degradation of the LDnMOS25V and the LDpMOS25V for the four channel widths and for a total dose of 30 krad(SiO₂). However, after irradiation, all of the components exhibited the same behavior, with respect to their type and dimension.

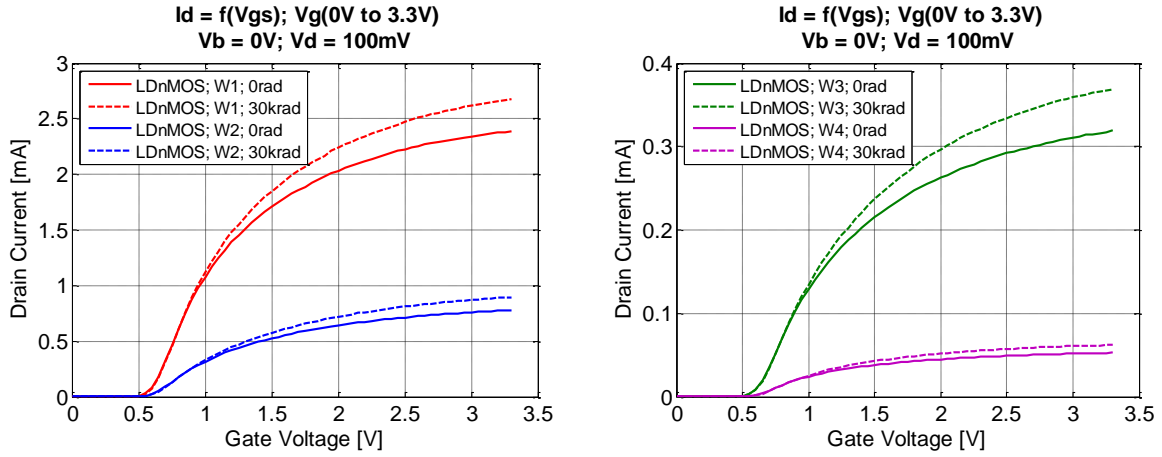


Figure 88: TID experimental results of the LDnMOS25V for the four different channel width tested. The plot on the left contains the curves before and after irradiation of the LDnMOS25V for the channel width W1 and W2. The plot on the right contains the curves before and after irradiation of the LDnMOS25V for the channel width W3 and W4.

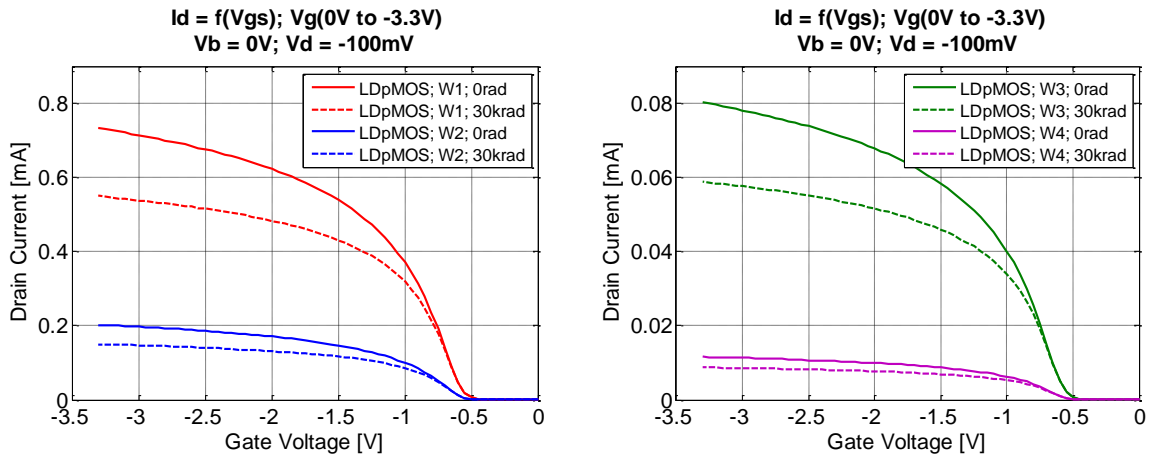


Figure 89: TID experimental results of the LDpMOS25V for the four different channel width tested. The plot on the left contains the curves before and after irradiation of the LDpMOS25V for the channel width W1 and W2. The plot on the right contains the curves before and after irradiation of the LDpMOS25V for the channel width W3 and W4.

The curves presented in Figure 88 depict the irradiation results of the LDnMOS25V. Both plots present $I_d=f(V_{gs})$ characteristics before irradiation in solid lines, and after 30 krad(SiO₂) in dashed lines. The plot on the left contains the curves before and after irradiation for the channel width W1 and W2. The plot on the right contains the curves before and after irradiation for the channel width W3 and W4.

The curves presented in Figure 88 and Figure 89 depict the irradiation results of the LDpMOS25V. Both plots present $I_d=f(V_{gs})$ characteristics before irradiation in solid lines, and after 30 krad(SiO₂) in

dashed lines. The plot on the left contains the curves before and after irradiation for the channel width W1 and W2. The plot on the right contains the curves before and after irradiation for the channel width W3 and W4.

As observed on the graphics in Figure 88 and in Figure 89, both devices exhibit different degradation behaviors. Indeed, the LDnMOS25V shows an increase in its current by 12.3% (0.29 mA over 2.33 mA) and the LDpMOS25V exhibit a decrease in its current by 24.9% (0.183 mA over 0.73 mA), respectively for a drain voltage of 100 mV and -100 mV; for a gate voltage of 3.3V and -3.3V; and for the channel width of W1. A similar behavior has been observed for all the others channel width. Moreover, for the entire set of components, no shift of the voltage threshold and no modification of the subthreshold slope was observed. These results show that oxides and interfaces traps are not the cause of the degradation, because TID irradiation only alters the on-resistance of the LDMOS [27].

To summarize, for both device, the main degradation is observed on the ON-resistance, with an increase of the power dissipated for the LDnMOS, and a decrease of the power dissipated for the LDpMOS.

In order to understand how TID affects the LDMOS structures, TCAD simulation is performed with ECORCE software. Thanks to Microchip, which gave us access to the technological data of the LDMOS25V, a simulation model has been created.

IV.3.3. SIMULATION MODEL

IV.3.3.1 Device structure

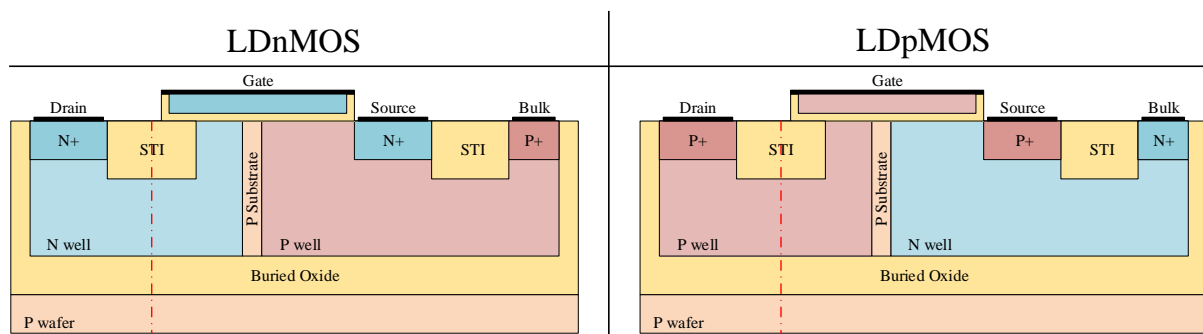


Figure 90: Representation of the simplified cross-section of the LDMOS structure. The figure on the left represents a LDnMOS structure and the figure on the right represents a LDpMOS structure. The red dashed line displays the cross section along which results are shown later in this chapter.

Figure 90 presents the two-dimension simplified structure of both devices LDnMOS on the left and LDpMOS on the right. The diffused drains are Nwell and Pwell for LDnMOS and LDpMOS, respectively. In both devices, the diffused drain is separated from the source by an intermediate p-substrate, allowing a higher voltage. When the device works in the linear region, the entire well region, located between the STI and the buried oxide, drives the current flow. The STI oxide used inside the

drain region of LDMOS is incorporated in order to increase the on-state and off-state breakdown voltages [26]. The structures are practically the same for the 25V and 45V topology, except for few dimensions.

IV.3.3.2 Simulations

In order to understand how TID affects the different structures, TCAD simulation was performed with ECRICE software [2]. This simulation helped us to observe how the charges trapped inside the different oxides affect the LDMOS electrical characteristics. With the help of Microchip Technology Nantes, we had access to the technological data of the LDMOS structures. Therefore, after implementation of the geometry, doped area, and oxide trapped zones the simulation model was completed.

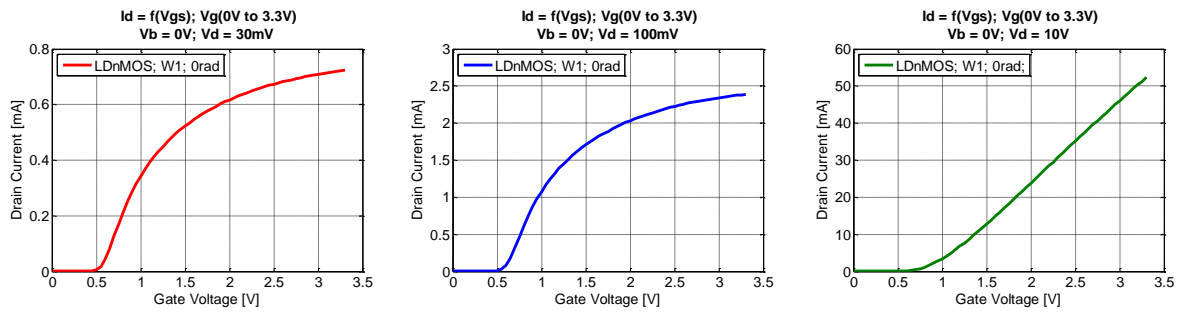


Figure 91: Measurement data for the LDnMOS25V with a channel width $W1$ and with three different biasing condition. From the left to the right, the drain voltage is 30mV, 100mV, and 10V. All those measurements were taken on pristine devices.

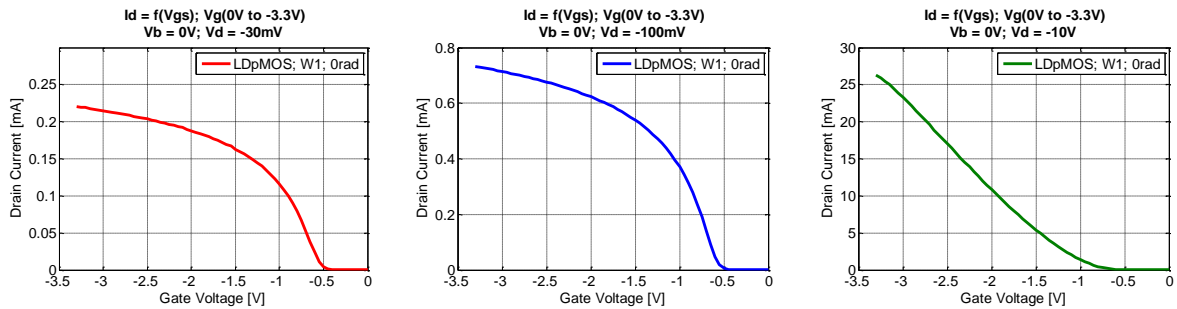


Figure 92: Measurement data for the LDpMOS25V with a channel width $W1$ and with three different biasing conditions. From the left to the right, the drain voltage is -30mV, -100mV, and -10V. All those measurements were taken without irradiation.

Our model was validated on $I_d=f(V_{gs})$ characteristics measured for three different biasing condition per LDMOS: 30mV, 100mV and 10V for the LDnMOS and -30mV, -100mV and -10V for the LDpMOS. Those measurements are shown in Figure 91 and Figure 92 respectively for the LDnMOS and the LDpMOS. For the two plots on the left, the current reaches the saturation value, which is not the case on the +10V and -10V drain biasing shown on the right, for which the current remains in linear regime. For this reason, the data with the drain voltage of +10V and -10V have not been used to compare

our simulated model to the measurements. Moreover, because ECORCE is for now programmed to simulate 1D and 2D structures, the resulting current is expressed in A/ μm , which, depending on the channel width of the component, leads to the computation of very small current values. Therefore, only the biasing for the drain voltage of 100mV and -100mV were used to compare the simulated results with the experimental data.

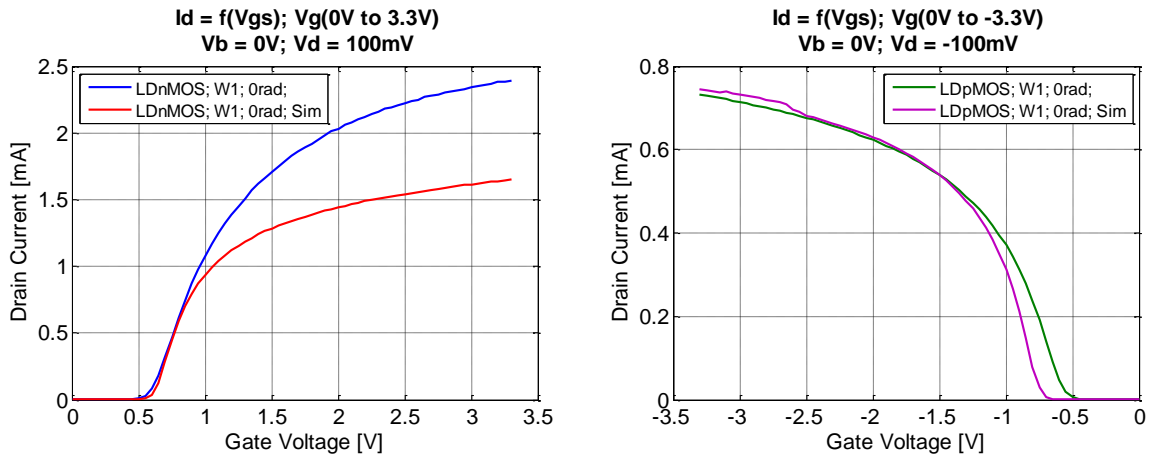


Figure 93: First comparison of the results obtained by simulated model with the real measured values.

The first simulation of the LDMOS models was performed using the data provided by Microchip without any modification. Figure 93 presents the results of the first simulation for the LDnMOS on the left and the LDpMOS on the right. The curves labeled with “Sim” at the end corresponds to the simulated results. As depicted on both graphics, the simulated values, and measured ones do not match, and differences are exhibited. Those differences can be explained by the imperfection of a multitude of parameters used inside the software. Therefore, before using this model to analyze the degradation, a fitting of the model was necessary.

IV.3.3.3 Adjustment of the simulation model to fit the experimental results

In order to fit the model of the LDnMOS and the LDpMOS, because the dimensions had to stay still, several attempts of modification of the doping values had to be performed on the different part of the model. Therefore, the first step was to understand how the modification of the doping values of each part of the model affects the output response.

For this reason and because the LDpMOS was the first model to fit, only fitting for the LDpMOS is presented here. However, the fitting mechanism was similar to the LDnMOS model.

IV.3.3.3.1 Modification of the LDpMOS' P-well doping

Figure 94 presents the results of the simulation performed with the original model without modification and two models with a higher doping of the left P-well and a lower doping of the left P-well. The value

labeled as X_P in the legend corresponds to the doping value of the P-well. This simulation was performed to understand how the doping of this area acts on the component response.

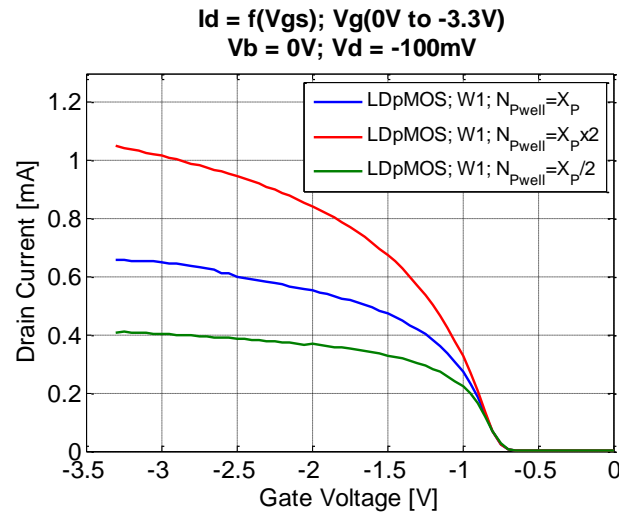


Figure 94: Simulation results on the LDpMOS model comparing different values of the left P-Well of the LDpMOS.

By comparing those curves, we understand that, by changing the left well (P-well for the LDpMOS and N-well for the LDnMOS), we act on the on-resistance of the component and then on saturation level of the component. By adding more charges into the diffused drain of the component, we act directly on the value of the drain to source resistance. Therefore, an increase in the doping value will reduce the on-resistance, increasing the saturation value, and a decrease of the doping value will increase the resistance and then reduce the current value of the LDpMOS.

Because the LDnMOS is composed of an N-well on the left side of the component, the variation of the doping of the N-well changes in the same way.

IV.3.3.3.2 Modification of the LDpMOS' N-well doping

Figure 95 presents the results of the simulation performed with the original model without modification and with two models with a higher doping of the right N-well and a lower doping of the right N-Well. The value labeled as X_N in the legend corresponds to the doping value of the N-well. This simulation was performed to understand how the doping of this area acts on the component response.

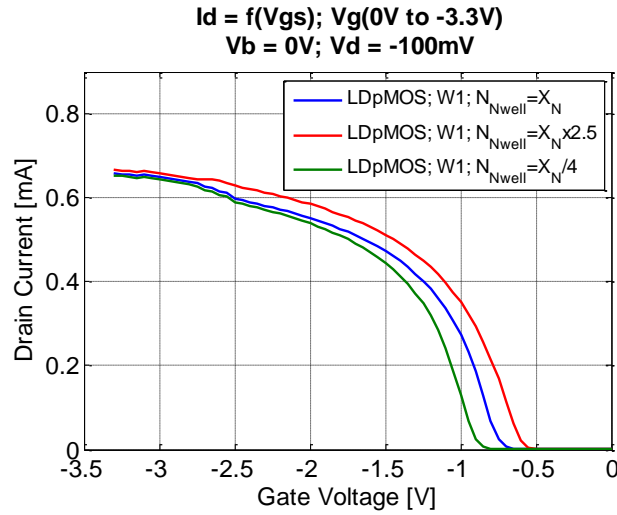


Figure 95: Simulation results on the LDpMOS model comparing different values of the right N-Well of the LDpMOS.

As observed on this graphics, the right N-well acts on the triggering voltage of the LDMOS.

IV.3.3.3.3 Modification of the LDpMOS' P-substrate doping

Figure 96 presents the results of the simulations performed with the original model without modification and with two models with a higher doping of the central P-substrate and a lower doping of the central P-substrate. The value labeled as X_P in the legend corresponds to the doping value of the P-substrate. This simulation was performed to understand how the doping of this area acts on the component response. This P-substrate area allows having a gradual lateral junction, which will hold higher voltages.

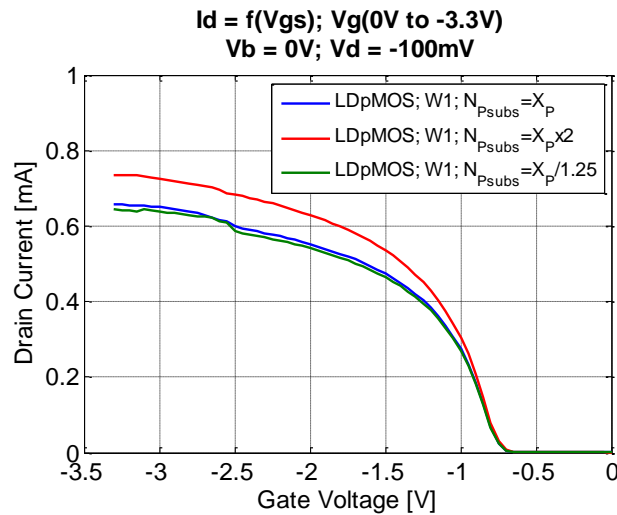


Figure 96: Simulation results on the LDpMOS model comparing different values of the central P-Substrate of the LDpMOS.

As observed on this plot, the value of the P-Substrate acts, as the P-Well, on the on-resistance of the LDpMOS, therefore, the same mechanism is observed. However, because of the lower value of the doping, the impact of the modification of the doping affects less the output characteristics.

IV.3.3.3.4 Fitting of the TID degradation

As explained before, the TID degradation is calculated depending on several parameters including the quantity of traps inside the oxides. This value is usually relevant for the quality of the oxide. A good oxide quality provides a homogeneous SiO_2 structure with few trapped charges, compared to a low-quality oxide, which contains many traps due to the inhomogeneity inside its structure. Therefore, because this value depends mainly on the fabrication process of the components, it is important to fit the trap density of the component to match with the measured data after irradiation. Moreover, because the LDnMOS and LDpMOS have been designed by the same manufacturer in the same foundry, the quantity of the oxide should be the same between the models of the LDnMOS and the LDpMOS.

It would be possible to determine a more precise distribution profile with the help of others irradiation in temperature, but for these simulations, a simple homogeneous repartition was used.

IV.3.3.3.5 Final model

After several modifications of the different doping values of the LDnMOS and LDpMOS, we managed to fit the measured data with the simulated data for the two models. Figure 97 presents the plots of the comparison between the measured data provided by Microchip with the simulated data for the LDnMOS on the left and for the LDpMOS on the right.

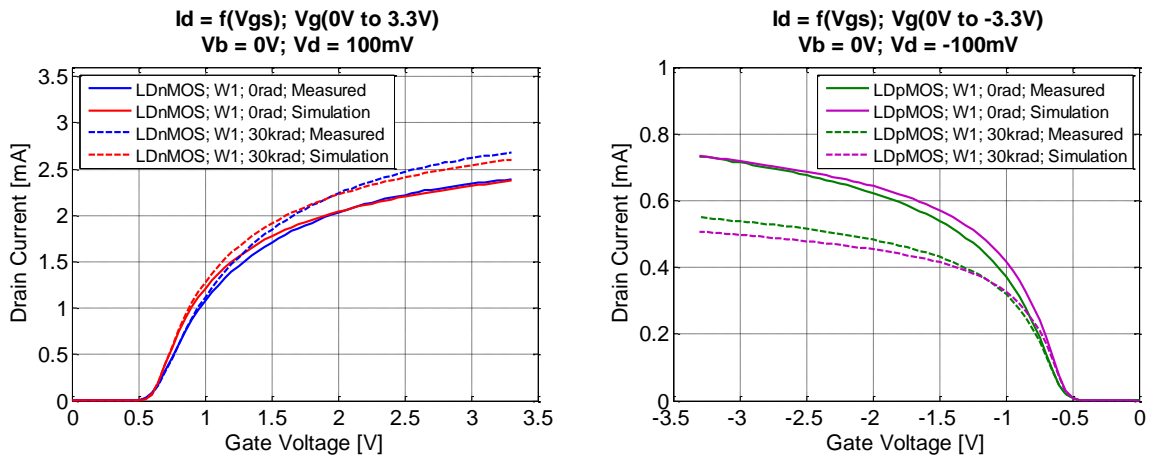


Figure 97: Comparison of the results obtained with the last simulation model with the real measured values.

The final models used have an average error of 10.63% between the simulated value and the measured one for the LDnMOS25V with a channel width W1 considering only the currents with a significant value (current $> 1 \times 10^{-6}$ A). For the LDpMOS25V with a channel width W1, an average error of 8.83% is obtained considering only the currents with a significant value (current $> 1 \times 10^{-6}$ A). Such errors between the measured data and the simulated ones will not affect the degradation behavior of the structure. The errors calculations were performed using the following equation:

$$< error > = \frac{\sqrt{(I_{manipulation} - I_{simulation})^2}}{\left(\frac{\sqrt{(I_{manipulation} + I_{simulation})^2}}{2} \right)} \quad \text{Equation IV.3-1}$$

IV.3.4. SIMULATION RESULTS

IV.3.4.1 Trapped charges distribution inside the oxides

The graphics on the left of Figure 98 and Figure 99 show the cross-section of the charges density inside the components before and after irradiation, for the LDnMOS and the LDpMOS. Both holes and electrons are respectively represented in red and blue lines. The solid line and the dotted-dashed line represent the charges density before irradiation and the dashed and dotted lines correspond to the charges density after irradiation. The graphic on the right of Figure 98 and Figure 99 represent the cross-section of the trapped charges density inside the component after irradiation. Both, trapped holes and trapped electrons are represented respectively in red and blue lines with the solid line and the dot-dashed line.

Both components are designed with an STI and a BOX. The electric field in the oxides drive the initial separation of electron/hole pairs and is responsible for the trapped charge distribution in the oxides. Depending on its sign, trapped charges will be accumulated on one side or another side of the oxide.

For the LDnMOS, the applied voltages ($V_d = 0V$; $V_g = 3.6V$) generate an electric field that pushes trapped holes towards the P-wafer into the BOX, and toward the n-well into the STI. Furthermore, the gate bias is low (3.6V) and the generated field in the STI (0.315 MV.cm) and in the BOX (0.009 MV.cm) are low. Thus, because of the low initial separation of pairs, the maximum density of trapped pairs at the end of irradiation is reduced (STI: $2.83 \times 10^{16} \text{ cm}^{-3}$, BOX: $1.54 \times 10^{16} \text{ cm}^{-3}$). Moreover, these trapped holes are mainly accumulated at the P-wafer interface for the BOX, and their effect on the charges of the diffused drain is low. Nevertheless, accumulated trapped holes in the STI attract some electrons toward the n-well/STI interface, leading to a small increase of the electron density in the resistive path. In the end, the resistance of the path is slightly decrease but not much compared to the resistance before irradiation.

For the LDpMOS, because of the different applied voltages ($V_d = -25V$; $V_g = 0V$), the generated electric field attracts trapped holes close to the n-well in the BOX, and close to the n-well in the STI. Moreover, the drain bias is high (-25V) and the generated field in the STI (2.1 MV.cm) and in the BOX (0.25 MV.cm) are higher. Thus, because of the high initial separation of pairs, the maximum density of trapped pairs at the end of irradiation is maximized (STI: $4.39 \times 10^{16} \text{ cm}^{-3}$, BOX: $4.34 \times 10^{16} \text{ cm}^{-3}$). Those trapped holes being mainly accumulated around the n-well, their effect on the holes distribution is very

high. They push the holes far from the interface while the electrons are attracted toward the p-well/STI and the p-well/BOX, narrowing the holes density inside the diffused drain leading to an increase of the resistance.

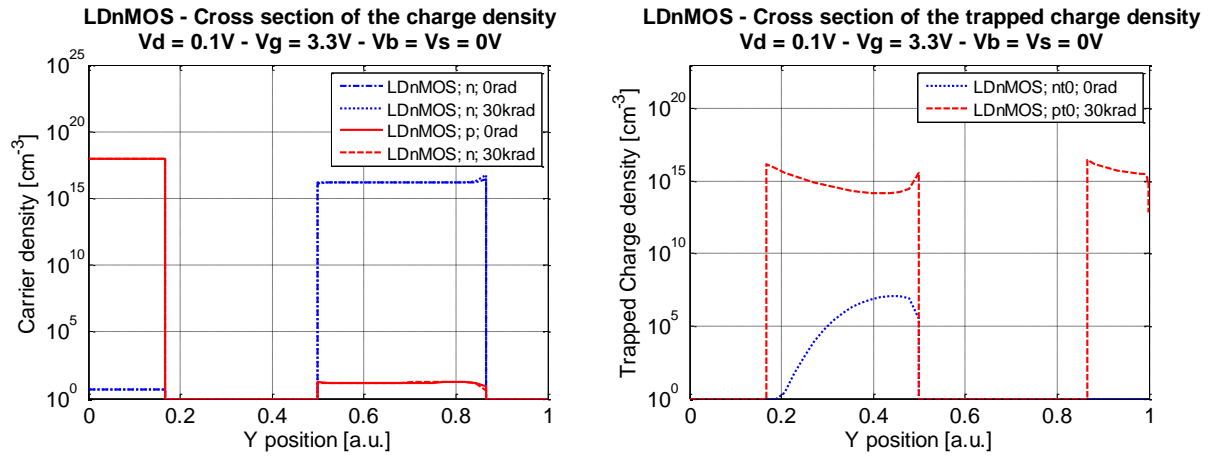


Figure 98: Cross section of the charges distribution inside the LDnMOS following the dashed-dotted line in Figure 90. Both graphics represent respectively the charges distribution density before and after 30 krad_(SiO2) and the trapped charges density distribution inside the oxide after 30 krad_(SiO2).

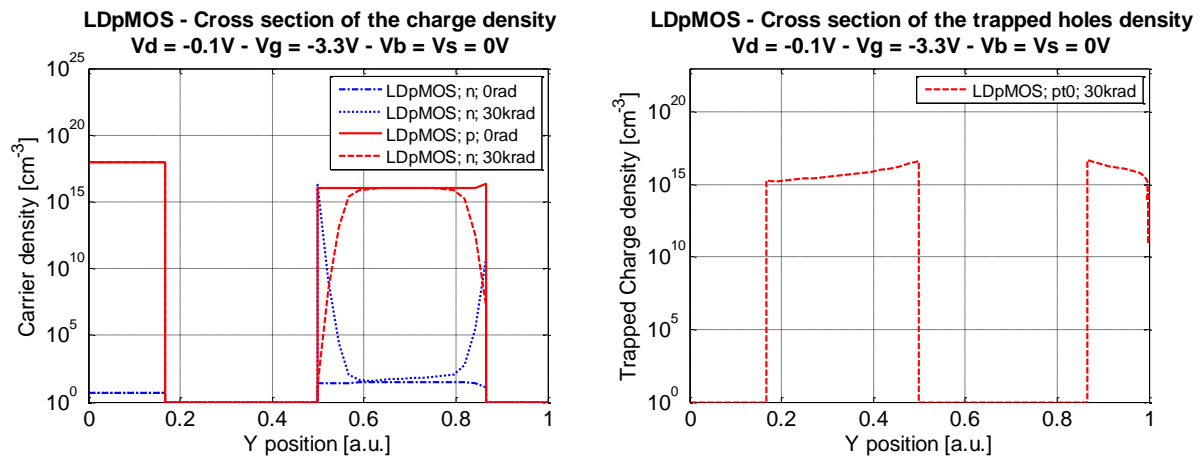


Figure 99: Cross section of the charges distribution inside the LDpMOS following the dashed-dotted line in Figure 90. Both graphics represent respectively the charges distribution density before and after 30 krad_(SiO2) and the trapped charges density distribution inside the oxide after 30 krad_(SiO2).

IV.3.5. CONCLUSION ON THE DEGRADATION OF THE LDMOS STRUCTURES

This section addresses the question raised by the observation of two effects of radiation-induced degradation, leading to a different response for LDnMOS and LDpMOS structures.

An increase of the $I_d=f(V_{gs})$ characteristic was observed for a LDMOS N-channel and a reduction of this characteristic was observed for a LDMOS P-channel during TID test campaigns performed with

^{60}Co γ -rays. In order to understand how TID irradiations affect both structures, TCAD simulations were performed.

The simulation results have shown that both STI and buried oxides surrounding the diffused drain, trap a large quantity of charges during irradiation. This effect is enhanced by the electric field, trapping charges close to the diffused drain/STI and diffused drain /BOX.

Those trapped charges, consisting mainly of holes, attract the electrons at the interfaces drain diffused/STI and drain diffused/BOX, and repelling the holes. Therefore, the P drain diffused well for the LDpMOS, sees its holes density decreasing, leading to an increase in the on-resistance and a reduction of the $I_d=f(V_{gs})$ characteristic.

For the N drain diffused well of the LDnMOS, a small reduction of the resistance is observed and is due to a small augmentation of the electron density caused by the increase of the trapped holes into the oxide. Such increase results in the augmentation of the $I_d=f(V_{gs})$ characteristic.

This results presented for the LDMOS 25V are also valid for the LDMOS 45V. Indeed, because of the difference of parameters of the 45V structure, the sensitivity of the TID degradation should be different. However, the degradation mechanism should be similar.

Based on those observations, an analogy of the degradation of the LDMOS has been used to understand how the GGnMOS triggering voltage would react against ionizing radiation.

IV.4. STUDY OF THE DEGRADATION OF A GGnMOS STRUCTURE

IV.4.1. INTRODUCTION

ESD protection structures are embedded in most electronic devices. Electrically neutral in normal operation mode, their role is to evacuate the electric charges injected at any terminal of an IC in case of an ESD event occurs.

A widely used way of achieving ESD protection is to connect a series of GGnMOS to each terminal of an IC. GGnMOS structures provide the advantage of simple construction, easy triggering and low space occupancy [28], however, they introduce in the IC a large number of MOS structures that may degrade in case of exposure to radiation, ionizing or not. This section raises the question of the impact of such degradation on the IC in two cases: (1) in normal mode of operation where leakage currents may be observed, (2) in case of ESD, as the efficiency of the protection may be reduced.

Very few studies on the radiation-induced degradation of ESD protection were carried out with TID while their degradation may be responsible for some unexplained behaviors observed. In their work, W. Liang *et al.* [29] and D. Linten *et al.* [30] have presented irradiation with He^+ and ^{58}Ni ions response of different ESD protection types, including GGnMOS structure. Even though the structure and the irradiation method are not the same, they give a good analogy compared to our study. They have highlighted the fact that GGnMOS structures can exhibit an increase of the on-resistance and an increase in the leakage current after irradiations. However, those tests do not prove the impact of TID irradiation.

In order to determine if the degradation of ESD protection may jeopardize an electronic system by increasing the leakage current or by being no longer able to protect against ESD, the GGnMOS structure provided by Microchip Technology Nantes is first presented. This structure has been used to perform a theoretical analysis and TCAD simulation with the TCAD software ECORCE.

At first, a theoretical analysis based on the structure analysis and literature is presented with the different degradations hypothesis. Then, those hypotheses are studied through different simulations in order to estimate the expected degradation on the GGnMOS structure.

IV.4.2. SIMULATION MODEL

IV.4.2.1 Device structure

Figure 100 presents the structure of the GGnMOS used for this study. Technological data of this structure was provide by Microchip Technology Nantes. It corresponds to a PD-SOI 150nm mixed technology GGnMOS 5V.

This structure is similar to a standard lateral MOSFET transistor, composed of an N+ drain well and an N+ source well. The P substrate is connected to the bulk that is separated from the source by a STI. The drain well is extended on purpose to increase the input resistance and thus limit the current flowing inside each GGnMOS during an ESD stress. To customize the ESD holding voltage, the length of the channel is wider than the channel of any conventional MOSFET transistor. Indeed, in the studied structures, the channel size is approximately twice as wide as in the conventional MOSFETs to increase its on-resistance. The whole component is enclosed within an oxide box that isolates the component from any other component with a deep trench and the substrate from the wafer with a buried oxide.

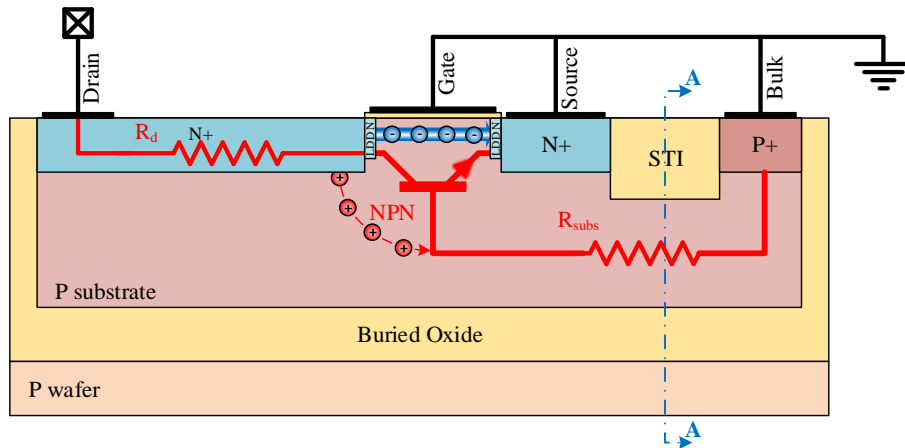


Figure 100: Simplified structure of the GGnMOS used in this study, based on the technological data obtained by Microchip Technology. The A-A cut corresponds to the cross section used to determine resistance.

As already presented in previous sections, the gate contact of the component is physically connected to the ground as much as the source contact and the bulk contact, whereas the drain contact is connected to the pad to protect.

For confidentiality reason, none of the technological data such as the dimensions, doping, and contact type will be given. All the dimensions presented will be modified as an arbitrary unit (A.U.) ranging from 0 to 1.

IV.4.2.2 Simulation

The GGnMOS model presented was implemented in ECORCE to perform the first simulations. However, no conclusive results were produced. GGnMOS structures use impact ionization or avalanche breakdown as triggering mechanisms, which makes difficult, to come up with results straight away. To simulate that triggering mechanism, a current injection at the contact would be required [31]. ECORCE being still in development, it does not allow for simulation with a current injection yet. Several others attempts of simulation were performed using voltage injection or by adding a resistor at the entrance of the structure, but none of them have been proven successful to simulate a GGnMOS triggering mechanism. Impact ionization is a complex mechanism difficult to simulate properly because it tends to create convergence errors. The development of ECORCE does not allow either, for now, a proper simulation of this structure with the impact ionization models.

Therefore, based on a theoretical analysis of the structure, two different radiation-induced degradation hypothesis were pointed out. Simulation with ECORCE was then performed to determine if the parameters suspected in the theoretical analysis were modified by the TID without simulating the structure in its normal operation.

IV.4.3. THEORETICAL DEGRADATION ANALYSIS

IV.4.3.1 Degradation hypothesis

The main role of an ESD protection is to keep the I/O pad voltage below the breakdown voltage of the chip gate oxide by bypassing most of the ESD stress current into the protections. Being based on MOSFET technology, GGnMOS ESD protections are designed with a gate oxide, which, under irradiation, traps charges. It is already well known that when the gate oxide of a MOSFET transistor has been submitted to irradiation, the trapped holes migrate at oxide/silicon interface [21], leading to a shift of the threshold voltage and an increase of the drain current. The consequence for a GGnMOS-based protection would be a critical point for an IC embedded in a system with a limited energy power budget. Indeed, because GGnMOS are not able to handle a large amount of current, each pad is usually designed with several GGnMOS fingers [32]. The resultant current leakage for a full IC would be very important and may cause an excess of the current consumption.

However, GGnMOS structures are designed with a physical grounded gate, reducing the electric field in the gate oxide and the effect of charge trapping during irradiation compared to standards MOSFET. In order to understand if the charges trapped into the gate oxide due to TID can lead to an excess of current consumption, the increase of the leakage current caused by the trapped charges into the gate oxide is investigated.

As presented in the section III.3.3.3 (Id-Vd characteristic of an ideal ESD protection, Chapter 3), the effectiveness of an ESD protection relies on the triggering voltage of the GGnMOS and on the time response of the transistor when an ESD event strikes. To ensure a perfect protection of the IC, the structure must trigger before an eventual failure occurs on the others components of the IC. The critical limit is considered as the gate oxide breakdown that would lead to the destruction of the IC itself.

As explained in the section III.3.7, when an ESD event starts striking, the GGnMOS structure starts generating a current of holes, flowing through the substrate. That current generates then a voltage difference between the bulk and the base of the parasitic NPN transistor. Because that voltage depends only on the resistance substrate that is crossed, any variation of the resistance value would lead to a modification of the triggering voltage. This resistance depends on the charges distribution and the mobility of the charges within the p-substrate. Any trapped charges inside the STI or the BOX would interact with this charge distribution and would lead to a modification of the resistance surrounded by those two oxides. The study performed on LDMOS structure presented in section IV.3 have already highlighted the fact that because of ionizing radiation, the resistance of the area in-between the STI and the BOX can be modified by the trapped charges inside those oxide. Therefore, in order to understand if such failure is possible on GGnMOS structures, a detailed theoretical explanation is given section IV.4.3.3, and simulations performed with ECORCE on the study of the variation of this resistance is presented next.

To summarize, two different types of radiation-induced degradation are investigated:

- Variation of drain leakage current caused by the gate oxide charges trapped. (Theoretical analysis in section IV.4.3.2 and simulations in section IV.4.4.1),
- Variation of the triggering voltage caused by charges trapped into the STI and BOX (theoretical analysis in section IV.4.3.3 and simulations in section IV.4.4.2).

IV.4.3.2 Degradation of the gate oxide with TID

In order to understand if a GGnMOS structure can show an increase in its leakage current with TID, TCAD simulations were performed based on the technological data provided by Microchip.

As presented in Figure 101, during the irradiation process, the electric field inside the oxide determines the amount of trapped charges. In their work, T.R. Oldham *et al.* have presented that the fractional yield of generated electron-hole pairs depends on the electric field inside an oxide and the particle of interaction [21].

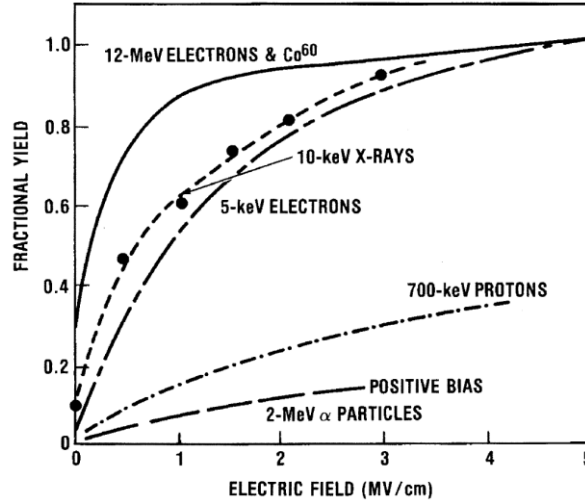


Figure 101: Fractional hole yield as a function of applied field, for a number of incident particles [21].

Because the gate of a GGnMOS is physically biased at 0V, the only electric field existing is generated by the band diagram of the junction metal/oxide/semiconductor. As presented by the energy band diagrams in Figure 102, depending on the work function of the contact material used, this electric field can have a different magnitude of direction that can lead to a variation of the quantity of trapped charges close to the interfaces and to a modification of the direction of the holes and electrons.

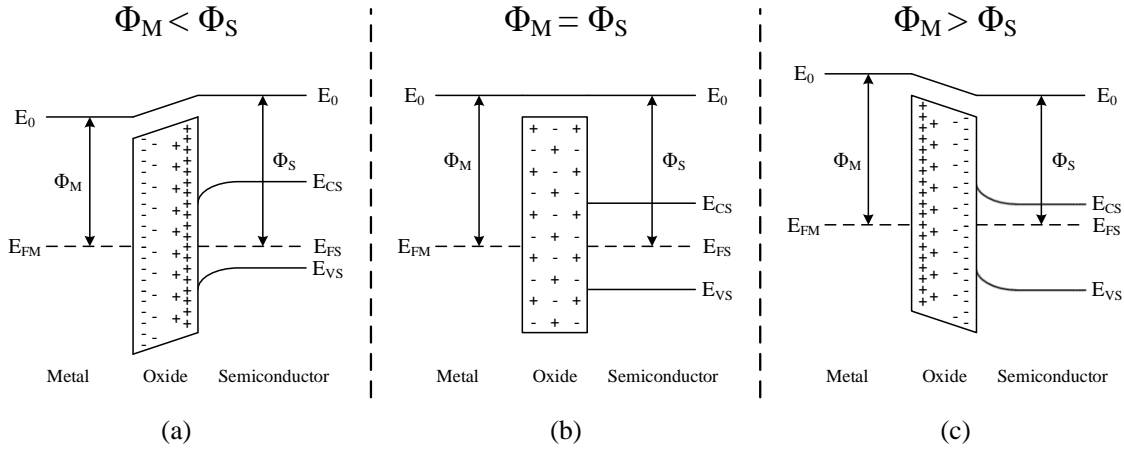


Figure 102: Representation of the Metal Oxide Semiconductor band diagram for three different cases: $\Phi_M < \Phi_S$ (a), $\Phi_M = \Phi_S$ (b) and $\Phi_M > \Phi_S$ (c).

The Figure 102 shows how the MOS band diagram is modified depending on the contact material work function, noted as Φ_M . The work function of the silicon is known to vary depending on the doping and the type of the material and is noted Φ_S . Any variation of Φ_M to be lower or higher than Φ_S would change the direction of the electric field inside the oxide. Three different cases can be expected:

- If $\Phi_M < \Phi_S$, as presented in Figure 102 (a), the electric field inside the oxide will be positive. The generated electrons holes pairs by ionizing radiation, because of the fractional yield, will see the electrons moving toward the metal while the holes will move toward the silicon.
- If $\Phi_M = \Phi_S$, as presented in Figure 102 (b), no electric field will be present. In this case, the generated electrons holes pairs by ionizing radiation will stay still and eventually get recombine. However, depending on the incident particles, some particle will still be trapped inside the oxide.
- If $\Phi_M > \Phi_S$, as presented in Figure 102 (c), the electric field inside the oxide will be negative. The generated electrons holes pairs by ionizing radiation, because of the fractional yield, will see the electrons moving toward the silicon while the hole will move toward the metal.

Therefore, depending on the contact metal used, a modification of the electric field is to expect and would modify the radiation induced-degradation.

Besides the electric field inside the oxide, it is already well known that oxide thickness is a determinant variable leading to charge trapping. Indeed, a thicker gate oxide will trap more charges than a thinner one, but depending on the position of the trapped charges, the effect on the channel can vary. A higher positive electric field will accumulate more hole at the interface oxide/silicon, which would lead to a higher impact on the leakage current.

It has been shown in [33] that the threshold voltage shift could be estimated according to the Equation IV.4-1:

$$\Delta V_{th} = \frac{q}{\epsilon_{SiO_2}} \int_0^{t_{ox}} xQ(x)dx \quad \text{Equation IV.4-1}$$

Where ΔV_{th} corresponds to the voltage threshold shift after irradiation, q to the charge of an electron, ϵ_{SiO_2} to the mobility in the oxide and $Q(x)$ the electric charge within the oxide t_{ox} . It expresses the expected V_{th} shift depending on the trapped charges distribution inside the gate oxide.

Because the gate contact and the oxide thickness are the two main parameters acting on the degradation, different structures were implemented on ECORCE with different gate contact and different thickness to observe the variation of their degradation.

IV.4.3.3 Degradation of the ESD triggering voltage with TID

As explained in the previous chapter presenting the ESD triggering mechanism, the triggering voltage depends on the current of hole generated at the depletion area because of the intense electric field by impact ionization. Inside a depletion area, when the electric field gets too high, electron/hole pairs tend to be separated, which creates a free electron and a free hole. The electrons generated will move toward the drain while the holes will move toward the bulk. The holes will then generate a potential difference

between the bulk and the base of the parasitic NPN transistor by passing through the substrate. The resistance formed by the substrate between the base of the parasitic NPN transistor and the bulk can be determined by using the holes distribution and the hole mobility into the substrate. The Figure 103 represented the theoretical cross section of the hole distribution following the y-axis in the middle of the STI following the A-A cut represented in blue point-dashed line in Figure 100. With a pristine component, the hole distribution inside the substrate is supposed to be homogeneous inside the p-substrate. Therefore, the calculation of the resistance will only depend on the doping value of the substrate and the mobility of the particle.

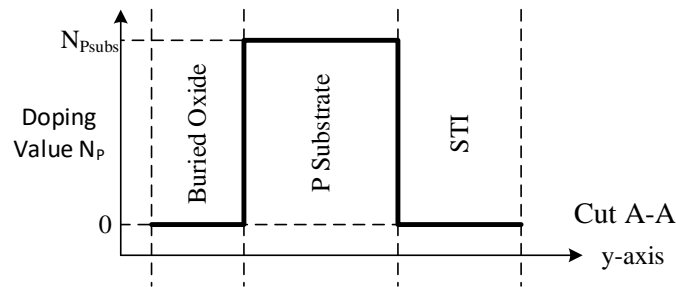


Figure 103: Theoretical cross-section A-A in Figure 100 of the hole distribution inside the canal

The GGnMOS structure is endowed with a STI between the source and the bulk, with a deep BOX. Under irradiation, both oxides will trap particles. These trapped charges, mainly constituted of trapped holes, attract some electrons toward the p-well/STI and p-well/BOX interfaces, increasing slightly the density of electrons while the holes will be pushed away from the interfaces. At the end the holes density in the region between the STI and the BOX will reduce close to the oxide and be narrowed to the center of the substrate, leading to a modification of the resistance.

If the holes generation caused by the high drain voltage stays unchanged, the current will generate a potential difference between the bulk and the base of the parasitic bipolar transistor. In this case, the ESD triggering voltage is expected to shift.

IV.4.4. DEGRADATION ANALYSIS WITH TCAD SIMULATIONS

IV.4.4.1 Current leakage analysis

IV.4.4.1.1 *Description of the different modeled structures*

Table 2 presents the different gate contact materials used in several simulations with the same structure and their respective work functions used to understand if an increase of the leakage current could be observed with TID on GGnMOS structures. It is important to note that some components listed in this table are known to be alpha particle emitter, which can induce a single event effect. More information can be found in [34].

The different values of the work functions for each material that can be used as contact are extracted from [35], [36]. A model was created for each material with three different gate oxide thicknesses i.e. 1tox, 2tox, and 3tox where tox corresponds to the oxide thickness of the model given by Microchip.

Table 2: Presentation of the Different Metals Used as Gate Contact.

Material of contact	Chemical Symbol	Work function
Hafnium	Hf	3.9 eV
Aluminum	Al	4.28 eV
Tungsten	W	4.55 eV
Copper	Cu	4.7 eV
Gold	Au	5.1 eV
Nickel	Ni	5.25 eV
Platinum	Pt	5.65 eV

Four different contact materials were first used with two worst cases of contact with a very low and very high work function (i.e. Hafnium and Platinum) and two commonly used materials (i.e. Aluminum and Tungsten). The three different gate oxide thicknesses investigated are the real oxide thickness, labeled “1tox”, medium oxide thickness that corresponds to two times the normal thickness, labeled “2tox”, and a thicker oxide thickness that corresponds to three times the normal thickness, labeled “3tox”.

IV.4.4.1.2 Analysis of the Leakage Current Increase with TID

Figure 104 presents the $I_d=f(V_g)$ characteristics of eight different structures, before and after irradiation at 150krad_(SiO₂). The first figure on the left corresponds to the structures with an oxide thickness of 1tox, and the second figure on the right corresponds to the structures with an oxide thickness of 3tox. On both figures, the continuous lines represent the characteristics before irradiation for the four different materials of contact, and the dashed line corresponds to the characteristics after 150krad_(SiO₂) simulated with ⁶⁰Co γ -rays.

If we look at the characteristics before irradiation, we can observe that a contact with high work function leads to a higher V_{th} before irradiation, reducing the current at $V_g = 0V$ while a lower work function leads to a lower V_{th} before irradiation, which increases the current for $V_g = 0V$.

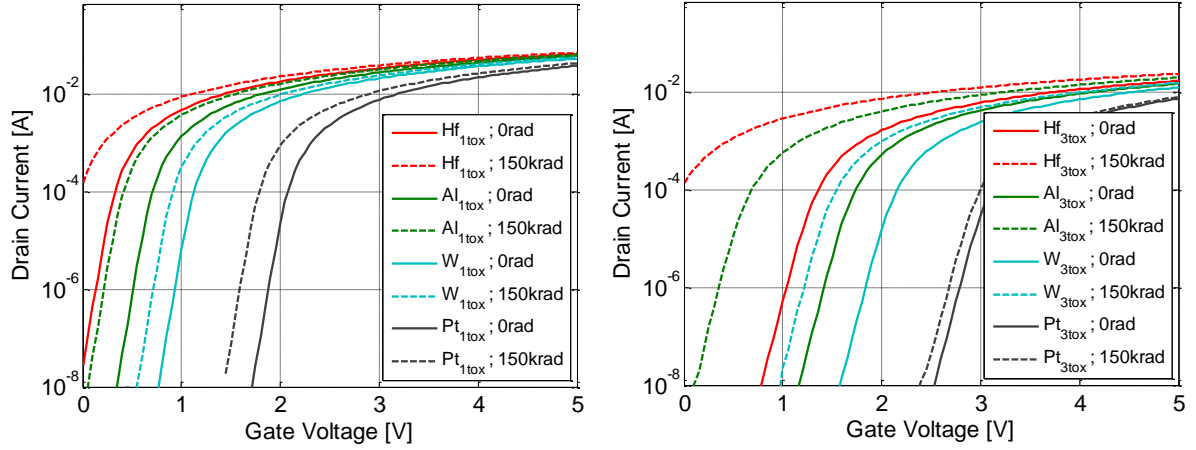


Figure 104: $I_d = f(V_{gs})$ characteristics of the different GGnMOS structures. These curves indicate that the threshold voltage shift depends on their contact material and oxide thickness. The figure on the left corresponds to the oxide thickness $1xTox$. The figure on the right corresponds to the oxide thickness $3xTox$. Both oxide sizes were simulated with Hafnium, Aluminum, Tungsten and Platinum as contact material.

As observed on the curve of the hafnium for $3tox$, corresponding to the worst-case design, a significant variation of the current is observed. Indeed, it increases from $1 \times 10^{-13} \text{ A}$ to $1 \times 10^{-4} \text{ A}$ after irradiation. This example shows that depending on the design of the structure, a significant increase of current with TID can appear.

IV.4.4.1.3 Work function dependency on the degradation

By taking a closer look at the curves in Figure 104 for $3tox$, the V_{th} shifts seem to vary depending on the materials used and thus, to the work function of the material. Indeed, if we compare the curves before and after irradiation for the four different materials, the V_{th} shift decreases for the higher work function.

Figure 105 presents the variation of the voltage threshold after $150 \text{ krad}_{(SiO_2)}$ depending on the seven gate contacts used, described in Table 2 for three different oxide thicknesses. As observed, for the three oxide thicknesses, the V_{th} shift decreases up to a work function of around 5 eV , then a slow increase of the V_{th} shift. We can also observe that after a work function of 5 eV , the V_{th} shift is lower for a thicker oxide.

This result can be explained by the band diagram of the junction metal/oxide/silicon as presented in Figure 102. Indeed, as explained in the previous section, the electric field is generated by the difference between the work function of the silicon and the one of the metal. For an acceptor doping of 10^{16} cm^{-3} of the substrate we obtain a work function of the silicon of 4.96 eV [36], when the work function of the metal range between 3.9 eV and 4.96 eV , a positive electric field is generated into the oxide, which, pushes the holes toward the oxide/silicon interface attracting more electron at the interface. In addition, a larger difference will lead to a higher magnitude of the electric field. When the work function of the

metal rises over 4.96eV, the electric field is reversed. The trapped holes will be pushed toward the oxide/metal interface and the electrons at interface Si/SiO₂. With a larger oxide, the influence of the trapped holes over the electrons of the channel becomes lesser, and a diminution of the V_{th} shift is observed. This phenomenon can be explained by the drawing presented in Figure 102

This point shows the importance of the gate contact metal used to build this kind of structure.

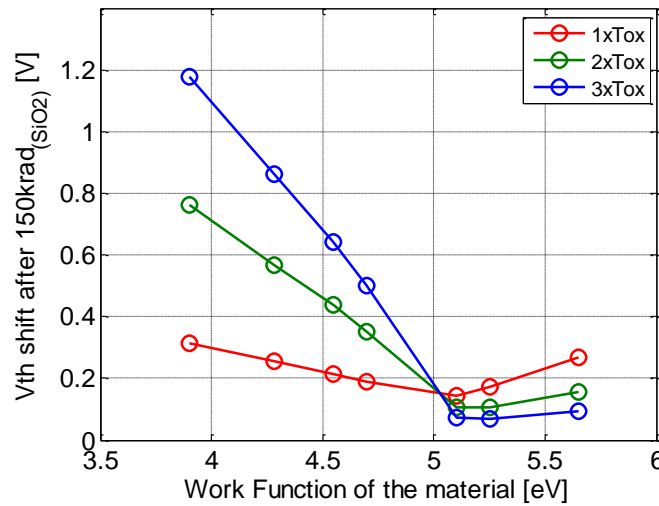


Figure 105: Variation of the threshold voltage shift after irradiation depending on the material work function. The three curves correspond to three different oxide thicknesses 1.tox, 2.tox, and 3.tox.

IV.4.4.2 Analysis of the ESD triggering voltage

IV.4.4.2.1 Determination of the substrate resistance before irradiation

As explained in the section IV.4.3.3, because the structure is endowed with a p-Substrate surrounded by an STI and a buried oxide, it is expected to be sensitive to TID as seen on the example of the LDMOS structures.

If we look at the simplified schematic of the structure of the GGnMOS, because of its narrow height, the area surrounded in red dashed line in Figure 106 should be the most resistive area. If we consider the resistance between the STI and the buried oxide, any modification of the doping value in this area would modify the value of the resistance.

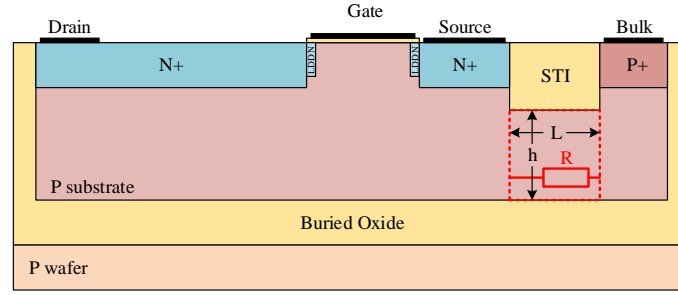


Figure 106: Representation of the resistance sensitive to TID located between the STI and the buried oxide.

To calculate the resistance of a semiconductor, it is necessary to know the dimensions of the area and the resistivity as presented in the Equation IV.4-2.

$$R = \rho \frac{L}{S} = \rho_{PSubs} \frac{L}{h \times W} \quad \text{Equation IV.4-2}$$

Where R is the value of the resistance, ρ the resistivity of the material, L the length of the STI and S the section that equals the height of the channel multiplied by the width of the component.

The resistivity of the material depends on the elementary electrical charge, the doping of the particles and their mobility. The relation can be expressed as the following:

$$\rho = \frac{1}{q(n \mu_n + p \mu_p)} \quad \text{Equation IV.4-3}$$

Where q is the elementary charge, n and p the electron and hole densities, and μ_n and μ_p the mobility of the electrons and the holes.

In an ideal case, the mobility of the electrons and holes would be constant like the charge density of the carriers, with, the holes being the majority carrier. Therefore, in this case, the minimum value of the resistance to expect (maximum doping and maximum mobility) in this area would be:

$$R = \frac{1}{q(n \mu_n + p \mu_p)} \times \frac{L}{S} \quad \text{Equation IV.4-4}$$

$$R = \frac{1}{1.6 \times 10^{-19} (2 \times 10^{15} \times 450)} \times \frac{L}{S}$$

$$\underline{R = 75.7 \text{ k}\Omega}$$

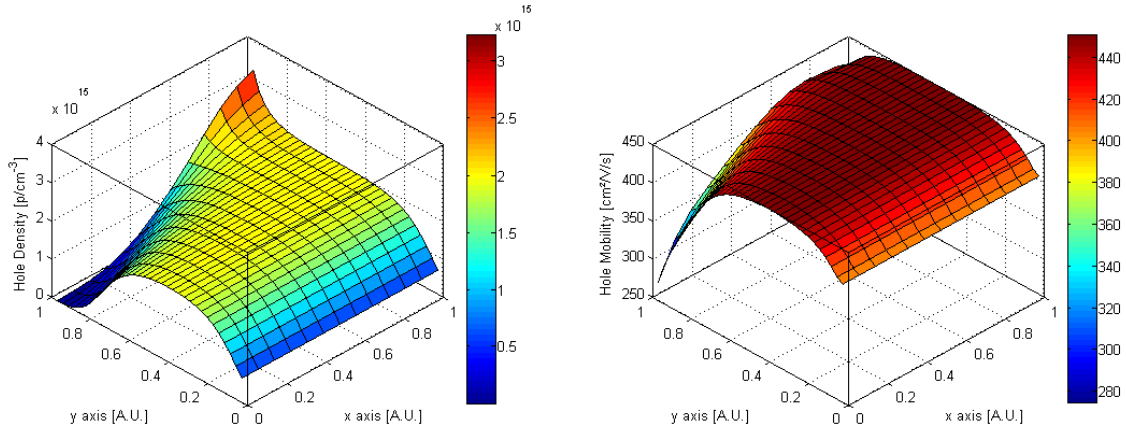


Figure 107: Variation of the hole density (left) and the mobility (right) of the holes inside the resistance as defined in Figure 106.

However, as presented in Figure 107, the doping and the mobility are not constant along the surface. In this figure, the plot on the left represents the variation of the hole density inside the resistance. The plot on the right represents the variation of the holes mobility inside the resistance. This variation is caused by an increase of the holes close to the P doped bulk and a reduction of the holes close to the N doped source.

In order to calculate the total resistance of this area, we need to calculate the resistance at each point of the mesh. To facilitate the calculation, let us consider that the current is displaced linearly inside the surface, as presented in Figure 108(a). In this way, each line is considered to have its independent current.

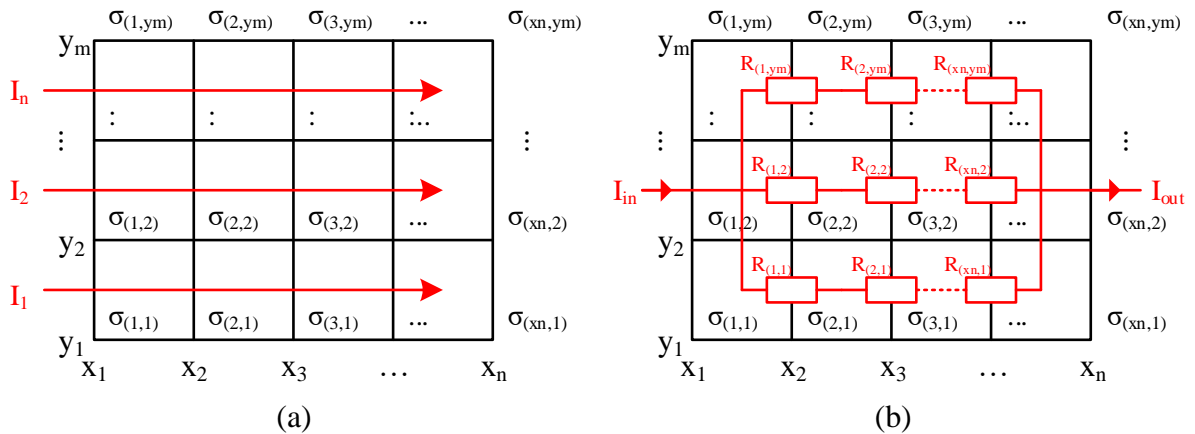


Figure 108: Representation of the calculation method to determine the analytical value of the resistor under the STI as presented in Figure 106.

Figure 108(b) represents the calculation method used to determine the resistance of the area. Each element of the meshing is broken down into one resistance. By adding the resistance on the same line,

we obtain the linear resistance, which has to be calculated with the others resistors as they were in parallel. The calculation performed is presented by the following equations.

$$\sigma_{(x,y)} = q(N_{n(x,y)}\mu_{n(x,y)} + N_{p(x,y)}\mu_{p(x,y)}) \quad \text{Equation IV.4-5}$$

$$R_{(x,y)} = \frac{1}{(\sigma_{(x,y)} + \sigma_{(x+1,y+1)})/2} \times \frac{L/n}{S/m} \quad \text{Equation IV.4-6}$$

$$R_{Total} = \left(\sum_{y=1}^{m-1} \frac{1}{\sum_{x=1}^{n-1} R_{(x,y)}} \right)^{-1} \quad \text{Equation IV.4-7}$$

With this calculation, we obtain $R_{Total} = 103.43 \text{ k}\Omega$ for $V_{Drain} = 0V$ inside the area under the STI. This value is higher than the theoretical value because of the variation of the mobility and the doping inside the area.

IV.4.4.2.2 Determination of the substrate resistance after irradiation

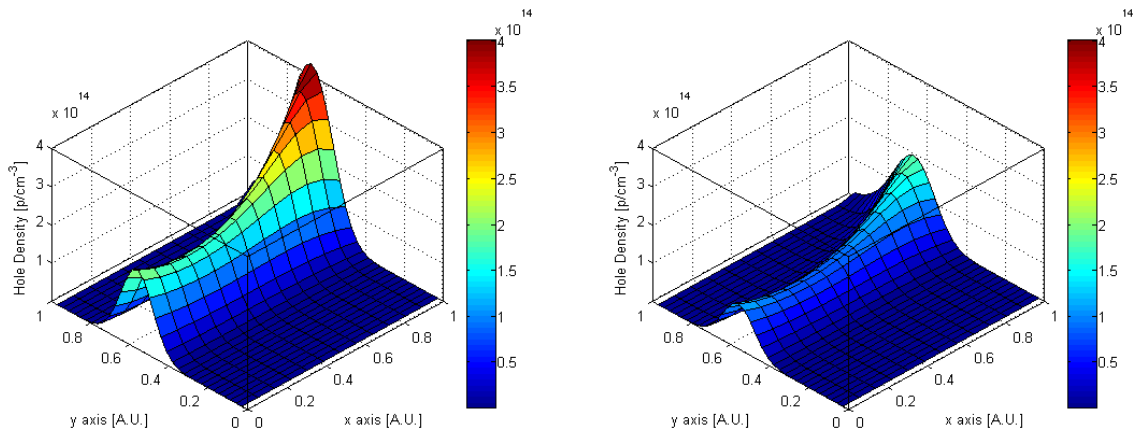


Figure 109: Variation of the hole density inside the resistance after 30krad_(SiO2) on the left and 150krad_(SiO2) on the right.

As presented in the section IV.3, radiations induced degradation on the LDMOS structure composed of the STI, p-substrate, and BOX acts on the resistance on the substrate channel. For an n-Substrate, the resistance of the channel is supposed to decrease slightly, whereas the resistance of the channel for a p-Substrate is supposed to increase significantly. Based on the observation made on the LDMOS structure, it is expected that the GGnMOS structure should present a similar behavior. Based on the same methodology, the resistance of the area under the STI has been determined for a TID of 30krad_(SiO2) and 150krad_(SiO2).

Figure 109 presents the hole density obtained after 30krad_(SiO2) on the left and 150krad_(SiO2) on the right. In comparison with the hole density before irradiation, as presented in Figure 107, the hole density is divided by a factor 10 in the center of the resistance. This reduction will modify the resistance value

inside the channel. Based on the calculation method of the resistance used previously, the resistance after irradiation of this area is estimated at 2.95M Ω for a TID of 30krad_(SiO₂) and 3.57M Ω for a TID of 150krad_(SiO₂). The trapped holes inside the STI and the BOX will have a large influence at the beginning of the irradiation, and once the oxide have trapped enough charges less and less holes will be trapped. It is important to note that the calculation method used does not determine the real resistance. Because it is based on a simplified calculation method and the parameters used are only simulated values. However, despite the inaccuracy of the calculation, it gives a good idea of the degradation with respect to the actual values.

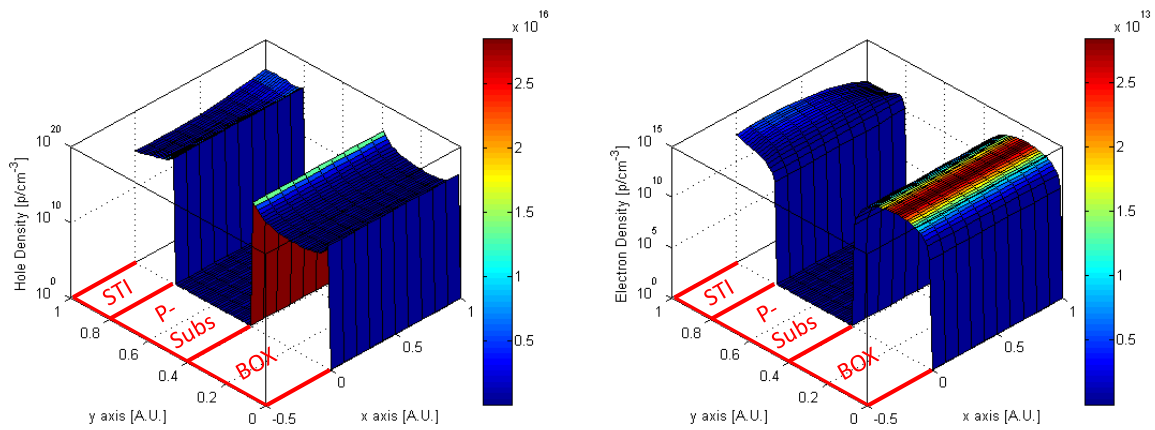


Figure 110: Trapped holes density and trapped electrons density simulated inside the STI and the BOX after 30krad_(SiO₂).

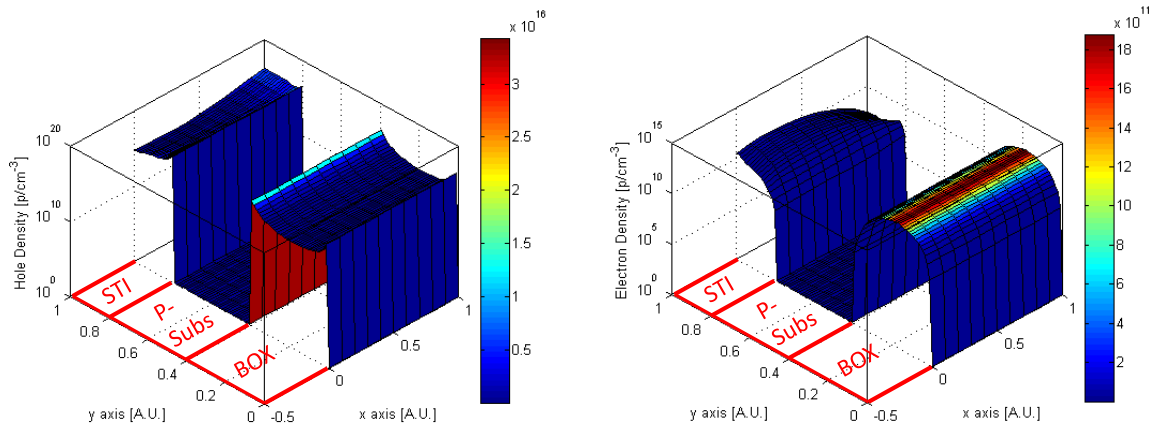


Figure 111: Trapped holes density and trapped electrons density simulated inside the STI and the BOX after 150krad_(SiO₂).

As already presented in the section IV.3, the variation of the resistance is caused by the trapped charges inside the oxides surrounding the p-substrate. Figure 110 and Figure 111 represents the trapped charges density inside the oxides surrounding p-substrate for a TID of 30krad_(SiO₂) and 150krad_(SiO₂). As presented on these pictures, a high amount of holes are trapped inside both oxides (up to 3×10^{16} at

30krad_(SiO₂) and 3.5×10^{16} at 150krad_(SiO₂)) whereas the value of trapped electron is lower (3×10^{13} at 30krad_(SiO₂) and 2×10^{12} 150krad_(SiO₂)). As explained in the introduction, the quantity of trapped holes is higher because the electron mobility is higher than the hole mobility and the electrons are evacuated faster from the oxides.

IV.4.4.2.3 Impact of the modification of the substrate resistance

In order to describe the impact of the TID on the substrate resistance, the triggering mechanism of the GGnMOS structure must be precisely described. As presented in the chapter III, the Figure 112 describes an ESD design window of an ESD protection with snapback. This characteristic can be broken down onto three different parts using different mechanisms.

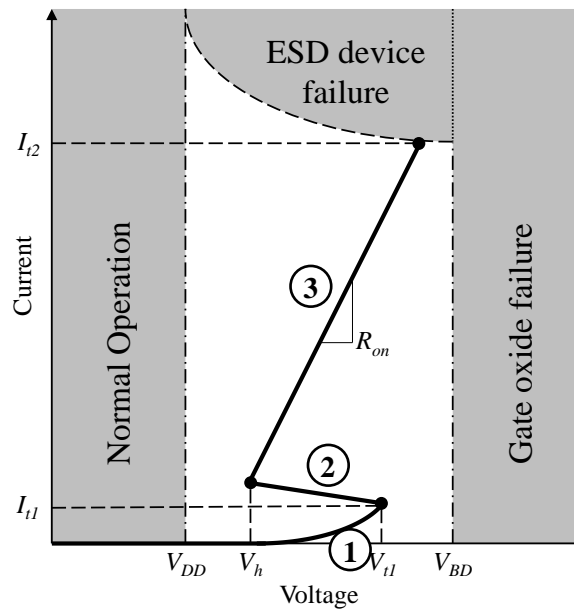


Figure 112: ESD design window of an ESD protection with snapback decomposed in three different mechanism: 1) Thermal generation, 2) Impact Ionization, and 3) Conduction.

①: because of the increase in the drain voltage, the depletion area surrounding the drain Nwell is getting larger. Thus, as in a reversed junction diode, a thermal generation appears in the depleted area. This phenomenon is called the Shockley-Read-Hall thermal generation. The electrons are then collected by the drain while the holes pass through the substrate to be collected by the bulk. This phenomenon increases slightly the consumption current of the structure [37].

②: because the thermal generation creates only a few pairs, the electric field is still getting higher. Once the electric field is very intense, the Impact Ionization is triggered. At this moment, the parasitic bipolar NPN transistor is activated and the voltage drops down to the holding voltage.

③: once the impact ionization reaches saturation, the parasitic bipolar NPN transistor is auto supplied and the conduction between the drain and the source is done through the channel. Thus, the resistance

of the conductive path drives the current, which depends on the carrier density generated, the length of the channel, the mobility and the temperature of the device.

To summarize, as presented in Figure 113, a GGnMOS can be assimilated to a bipolar NPN transistor driven by a current source I_{Gene} through the substrate resistance R_{subs} . The current source I_{Gene} corresponds to the current generated by the high electric field.

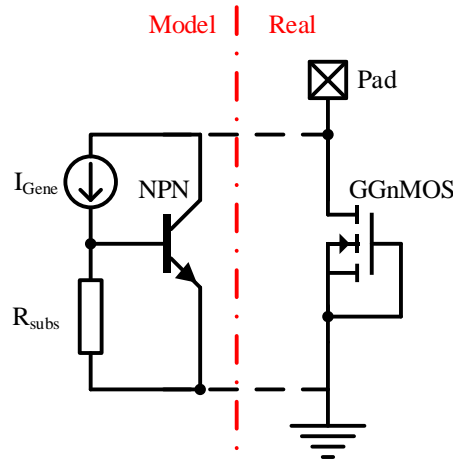


Figure 113: Simplified model of the GGnMOS ESD protection. This schematic presents the GGnMOS that can be assimilated as a bipolar NPN transistor driven by a current source I_{Gene} through the substrate resistance R_{subs} .

As observed in the previous section, the substrate resistance is bound to increase with TID. Because the electric field generated by the depleted area will be the same with or without irradiation, for the same current generated, the resulting voltage of the substrate resistance will be higher. Then, because a bipolar NPN transistor is triggered around 0.7V, the GGnMOS should be triggered before its actual triggering voltage prior-irradiation.

The different cases of radiation-induced degradation presented proves that the GGnMOS structure should be sensitive to the total ionizing dose depending on several factors such as the gate contact material, thickness of the gate oxide, positioning of the oxide or design with a buried oxide. Depending on the quality of those oxides, the radiation-induced degradation would differ but the same physical mechanism should happen on a different scale. Even if the model studied does not correspond fully to the reality, it gives a good representation of radiation mechanisms and their impact on the different parameters of the component.

IV.4.5. CONCLUSION ON THE DEGRADATION OF THE GGnMOS

This section presents the study performed on an ESD protection PD-SOI 150nm mixed technology GGnMOS5V from Microchip. The goal was to determine if GGnMOS ESD protection structures embedded in an integrated circuit could present a critical TID-induced degradation.

By using the cross-section of the GGnMOS structure, a first theoretical analysis was performed. This analysis highlighted two potential degradations of this structure:

- A GGnMOS structure is based on a MOSFET technology designed with a thick gate oxide. It has already been shown that when a MOSFET gate oxide is submitted to irradiation, the trapped holes in the oxide migrate at oxide/silicon interface. This latter generates a positive electric field inside into the gate oxide, which affects the threshold voltage and the subthreshold drain current in the channel. Thus, because a GGnMOS structure is usually added in large quantity inside and IC, the resultant current leakage for a full component would be very important and may cause an excess of the current consumption. However, because GGnMOS structures are designed with a physically grounded gate, the electric field in the gate oxide is then reduced and the effect of charge trapping during irradiation is limited compared to standards MOSFET. Here, the contact metal work function plays a critical role and the choice of the metal used is critical.
- When an ESD stress occurs, the parasitic NPN transistor of the structure is triggered. When the electric field at the interface drain/substrate is too high, a current starts to be generated by impact ionization. The electron current is evacuated by the drain contact while the holes current flows toward the bulk by passing through the substrate. Once the voltage difference between the bulk and the base of the parasitic transistor is high enough, the parasitic NPN transistor is enabled and the electron current is evacuated through the channel. As explained in the section presenting the degradation of the LDMOS structures, a structure composed of a p-substrate surrounded by a STI and a BOX may see its resistance reduced because of the trapped charges inside those oxides. Therefore, a variation of the substrate resistance may cause a negative shift of the triggering voltage of the GGnMOS structure.

Based on those two assumptions, TCAD simulations were performed with the GGnMOS model given by Microchip to quantify the radiation-induced increase of the leakage current and the variation of the ESD triggering voltage.

A first set of simulations were performed using several models composed of different contact material and gate oxide thickness. Those models were used to determine how the GGnMOS gate oxide acts on the channels with TID. The results have shown that when the gate contact metal has a lower work function than the silicon one, a positive electric field is generated inside the oxide. As a result, the trapped holes are pushed toward the SiO₂/Si interface while the trapped electrons are evacuated by the gate contact. In the case where the gate contact metal has a higher work function than the silicon, a negative electric field is generated inside the oxide. As a result, the trapped holes are pushed toward the gate contact while the trapped electrons are moves toward the SiO₂/Si interface. In addition, a larger

difference between those two work functions would increase the magnitude of the electric field and increase the amount of electrons holes pair generated.

These results show that depending on the gate contact metal used, different degradation due to the gate oxide can be expected. The utilization of gate contact material with high work function could be considered as a better solution than using traditional metals (i.e. hafnium, aluminum, tungsten, etc.) with low work function. Because the type of metal used for the gate contact does not affect the triggering efficiency of GGnMOS structures, any kind of metals could be used with the structure to provide higher protection and robustness to TID.

Concerning the second degradation hypothesis, TCAD simulation helped us to understand if the substrate resistance of the GGnMOS may be modified with TID. It was shown that the two oxides endowing the structure, once they have trapped charges, act on the charge distribution of the p-Substrate. As a result, an increase of the electron density and the diminution of the hole density is observed inside the p-substrate surrounded by the STI and the BOX. Moreover, because of the trapped holes inside the oxide, the p-substrate is narrowed.

These results show that after irradiation, because of a variation of the p-substrate carrier density, the resistance may be reduced and a shift of the triggering voltage is to be expected. This phenomenon is difficult to counteract since oxide will trap particles anyway. A solution to reduce this variation would be to increase the quality of the oxide to reduce the trap density.

Since no proper triggering of the structure was simulated, no observation of the ESD triggering voltage shift was observed. However, these results based on an assumption and a theoretical analysis should draw attention on a potential failure mechanism, which deserves to be further investigated.

In addition, in order to prove the reality of this potential failure mechanism, it would be important to correlate simulation results with experimental measurements. Radiations tests on GGnMOS structure are planned to be performed with standalone structures provided by the Microchip as a sequel of this thesis.

IV.5. CONCLUSION

In this chapter, the analysis was performed on LDMOS structures and GGnMOS structure using ECORCE, a TCAD software developed by the University of Montpellier.

The first section of this chapter details this software. The different physical laws and equations implemented in the software code are explained and their usefulness is also described.

In the second section, a study performed in collaboration with Microchip Technology Nantes on LDMOS structure shown to be similar to GGnMOS is presented. This study is based on experimental results obtained by irradiating several samples of LDMOS structure. The results obtained showed a variation of the structure's dynamic resistance and no variation of the triggering voltage. It has been assumed at first that this degradation would come from the trapped charges inside the oxides surrounding the diffused drain. Therefore, because this structure is built with a similar structure to a GGnMOS, an analysis with ECORCE was performed. As a result, it has been proven that the structure composed of the STI/diffused drain/Buried oxide is indeed responsible for the variation of the dynamic resistance of the component. Those results have been at the end used to perform a similar analysis of GGnMOS ESD protection presented in the last part of this chapter.

The last part of this chapter presents the analysis performed on GGnMOS structure. Because no experimentation was performed on this structure, the results obtained with the LDMOS structure were used to make an analogy of the degradation of the GGnMOS structure. The first point presented the degradation obtained by trapping charges into the STI and buried oxide endowing the structure. The trapped charges in those oxides would change the substrate resistance and may modify the triggering voltage of the GGnMOS structure. Based on the simulations, the resistance of the p-substrate surrounded by the STI and the buried oxide shows a diminution by a factor of 10 times after irradiation. However, no proper simulation of the model was performed and the mechanism that at play doesn't constitute an evidence of the potential degradation. The second point of this analysis was performed on the variation of the leakage current due to the trapped charges inside the gate oxide. The GGnMOS structure is designed with a gate contact and a bulk contact physically connected to the ground, only the band diagram of the Metal/Oxide/Semiconductor generates the electric field into the oxide. Therefore, depending on the work function of the metal used as a contact, different degradation levels are expected. A low work function would lead to an increase in the degradation whereas a high work function would lead to a diminution of the leakage current. In any case, the addition of the leakage currents of the multiple GGnMOS structures, as small as it could be would definitely end up with a non-negligible leakage current between the positive supply terminal and the ground of an integrated circuit.

IV.6. REFERENCES

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General Conclusion

The work proposed in this thesis is divided into two independent studies. The first part investigates the influence of the design on cumulative effects, TID and DD, in a bipolar operational amplifier. The second part is dedicated to studying the sensitivity synergistic effects that may exist between ESD and TID.

The first chapter of this manuscript is an attempt to summarize all the information necessary for the understanding of both studies led. An overview of different radiative environments originating from natural and manmade sources, in space and on the ground is presented. The physical mechanisms causing the degradation of electronic components due to cumulative effects are explained along with their impact on bipolar and MOSFET technologies.

The second chapter describes a standalone study based on the experimental results obtained by F.Roig on LM124 operational amplifiers from three different manufacturers. After TID and DD irradiation, two devices out of three exhibited a degradation in agreement with the literature. This typical behavior is characterized by a degradation of the slew rate scaling with the degradation of the supply current. However, one of the components showed an unexpected variation, that is an increase of the slew rate. SPICE simulations, circuit analysis, die layout analysis and measurements performed on the three component, highlighted several discrepancies on this third device. A reverse engineering performed on the three components showed that they all shared the same internal electrical schematic, except for a current source of the input stage, which does not affect the variation of the slew rate but only the input currents. However, it was shown that in all the degradation scenarios simulated, an increase in the base current of two transistors (named Q10 and Q14) explained the important variation of the slew rate. In addition, on the LM124-ST, the designers have increased the value of some current sources and decreased the value of the compensation capacitor, which strongly enhanced the variation of the slew rate. In the end, it was shown that the nested structures composed of Q9-Q10 and Q8-Q14 and known to be very sensitive to cumulative effects increased greatly the sensitivity of the component.

The third chapter of this thesis is dedicated to the study of the synergistic effect between TID-ESD. The bibliographical study showed that ESD might occur in space as well as on the ground. In space, the accumulation of charges on the surfaces exposed to an electron plasma is likely to generate an ESD. This ESD may occur at any time of the mission, including at the end, when the device has already been exposed to a significant dose of radiations. Therefore, it is important to understand if an irradiated ESD protection would still be effective or if a synergistic effect may jeopardize the system. Among the most widespread protection structure, GGnMOS (Gate Grounded N-MOSFET) are of special interest, since

they constitute an integrated MOS structure directly added at the input pads. They provide the advantage of a simple construction, an easy triggering and a low space occupancy. However, they introduce directly between the ground and the supply rails a large number of MOS structures that may degrade in case of exposure to radiation, causing a significant current leakage, thus an increase in the supply current. The goal of this study was to understand if the ionizing radiation-induced degradation on an IC, the GGnMOS structures could:

- (1) exhibit an increase of their leakage current in normal mode of operation;
- (2) in case of ESD, present a reduction of the efficiency.

A first series of measurements were performed on a COTS MRAM memory that had already shown an unusual degradation to TID during previous irradiation tests. Considering the impossibility to open the package and perform a reverse engineering on the circuit, a black box approach was used. Characterization of the input pads have shown that the triggering mechanism of the memory was similar to a GGnMOS triggering, therefore, irradiation tests were performed. Unlike the previous tests performed on a different lot, the irradiation results have shown no increase in the supply current and no increase in the input currents after 100 krad_(SiO₂). The characterization performed after irradiation on the input pads have shown a little variation of the holding voltage, but no variation of the others parameters like the leakage current. In the end, we came to the conclusion that it is very difficult to state that the variations observed could result from a degradation of the GGnMOS protections. Indeed, due to the black box approach, all the ESD protections are connected to the circuit and it is not possible to determine where the degradation originates from. Thanks to a late collaboration with Microchip Technology Nantes, we had access to technological data on GGnMOS structures that enabled a new study consisting in analyzing the radiation-induced degradation of the GGnMOS structure through theoretical analysis and TCAD simulations

Due to a lack of experimental data on GGnMOS structures, Laterally Diffused Metal Oxide Semiconductors (LDMOS) devices provided by Microchip, sharing a very similar structure and for which irradiation test results were already available were used to support this study. The results obtained were then extrapolated to GGnMOS, making possible to understand their degradation modes.

Radiation tests results on Laterally Diffused Metal Oxide Semiconductors (LDMOS) structure from Microchip, performed with ⁶⁰Co gamma rays, revealed a high sensitivity of the on-resistance, which seemed to be the only parameter sensitive to TID. To investigate which degradation mechanism came at play, TCAD simulations were performed. First, the ECORCE model was calibrated to fit the experimental results. The following analysis of the radiation-induced degradation showed that irradiation reduces the resistance of the diffused drain due to the charges trapped in the surrounding oxides. The Structure of GGnMOS being quite similar, it is reasonable to assume that this result also applies to the degradation of the GGnMOS structures.

The first order analysis is based on the assumption that the MOSFET based GGnMOS are designed with a gate oxide thick enough to trap charges. The holes trapped in the oxide migrate at oxide/silicon interface leading to a shift of the threshold voltage and an increase of the subthreshold drain current. Such degradation for a GGnMOS protection would be a critical issue for an IC embedded in a system with a limited power budget. Indeed, because a single GGnMOS is not able to handle a large amount of current, each pad is usually designed with several GGnMOS fingers. Therefore, the resultant current leakage for a full IC would be very high and may cause an excess of the current consumption. However, GGnMOS structures are designed with a physically grounded gate. The electric field in the gate oxide is then reduced and the effect of charge trapping during irradiation is also reduced compared to standards MOSFET. Thus, only the work function of the gate contact material used determines the electric field inside the gate oxide. Depending on the material, the degradation will be completely different, and in some cases, an increase in the leakage current may appear.

Another degradation mechanism found depends on the triggering mechanism itself. When an ESD stress occurs, the parasitic NPN transistor of the structure is triggered. TCAD simulations performed on this structure show that the trapped charges inside the isolation oxides of the component modify the resistance of the substrate, which may cause the triggering of the protection before the specified value and increase the power to dissipate.

However, in order to prove the reality of this potential failure mechanism, it would be important to correlate simulation results with experimental measurements. Radiations tests on GGnMOS structure are planned to be performed with standalone structures provided by Microchip as a sequel of this thesis. Only then, we will be able to prove the validity of the simulations performed.

Publications and communication by the author

Publication accepted in a journal as first author

T. Borel, F. Roig, A. Michez, B. Azais, S. Danzeca, N. J-H. Roche, F. Bezerra, P. Calvel and L. Dusseau, "**Atypical Effect of Displacement Damage on LM124 Bipolar Integrated Circuits**," in IEEE Transactions on Nuclear Science, vol. 65, no. 1, pp. 71-77, Jan. 2018.

T. Borel, S. Furic, E. Leduc, A. Michez, J. Boch, A. Touboul, B. Azais, S. Danzeca, L. Dusseau, "**Total Ionizing Dose Effect in LDMOS oxides and devices**", accepted for publication in the IEEE-TNS journal.

T. Borel, A. Michez, S. Furic, E. Leduc, J. Boch, A. Touboul, B. Azais, S. Danzeca, L. Dusseau, "**Gate Grounded n-MOS Sensibility to Ionizing Dose**", Accepted as a proceeding for RADECS 2018

Publication accepted in a journal as co-author

S. Danzeca, P. Peronnard, G. Foucard, G. Tsiligiannis, R. Secondo, R. Ferraro, C.G. McAllister, **T. Borel**, M. Brugger, A. Masi, S. Gilardoni, "**Compendium of Radiation-Induced Effects for Candidate Particle Accelerator Electronics**," 2017 IEEE Radiation Effects Data Workshop (REDW), New Orleans, LA, 2017, pp. 1-6.

S. Danzeca, P. Peronnard, G. Foucard, G. Tsiligiannis, R. Ferraro, G. Piscopo, C.G. McAllister, **T. Borel**, A. Masi, S. Gilardoni, "**2018 Compendium of Radiation-Induced Effects for Candidate Particle Accelerator Electronics**", 2018 IEEE Radiation Effects Data Workshop (REDW), NSREC 2018.

Participation to an international conference

Oral presentation

T. Borel, A. Michez, S. Furic, E. Leduc, J. Boch, A. Touboul, B. Azais, S. Danzeca, L. Dusseau, “**Gate Grounded n-MOS Sensibility to Ionizing Dose**”, accepted as a proceeding for RADECS 2018.

Poster presentation

T. Borel, S. Furic, E. Leduc, A. Michez, J. Boch, A. Touboul, B. Azais, S. Danzeca, L. Dusseau, “**Total Ionizing Dose Effect in LDMOS oxides and devices**”, accepted for publication in the IEEE-TNS journal.

T. Borel, F. Roig, A. Michez, B. Azais, S. Danzeca, N. J-H. Roche, F. Bezerra, P. Calvel and L. Dusseau, "Atypical Effect of Displacement Damage on LM124 Bipolar Integrated Circuits," in IEEE Transactions on Nuclear Science, vol. 65, no. 1, pp. 71-77, Jan. 2018.