Characterization of TFETs made using a Low-Temperature process and innovative TFETs architectures for 3D integration

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Caractérisation de transistors à effet tunnel fabriqués par un processus basse température et des architectures innovantes de TFETs pour l'intégration 3D

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To my parents, my sister and

all members of my family

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General Index

Abstract/Résumé

Characterization of TFETs made using a Low-Temperature process and innovative TFETs architectures for 3D integration

This thesis presents a study of FDSOI Tunnel FETs (TFETs) from planar to trigate/nanowire structures. For the first time we report functional "Low-Temperature" (LT) TFETs fabricated with low-thermal budget (630°C) process flow, specifically designed for top tier devices in 3D sequential integration. "Dual I_DV_{DS}" method confirms that these devices are real TFETs and not Schottky FETs. Electrical characterization shows that LT TFETs performance is comparable with "High-Temperature" (HT) TFETs (1050°C). However, LT TFETs exhibit ON-current enhancement, OFF-current degradation and V_{TH} shift with respect to HT TFETs that cannot be explained via BTBT mechanism. Charge pumping measurements reveal a higher defect density at the top silicon/oxide interface for geometries with narrow widths in LT than HT TFETs. In addition, low-frequency noise analyses shed some light on the nature of these defects. In LT TFETs, we determined a non-uniform distribution of defects at the top surface and also at the tunneling junction that causes trap-assisted tunneling (TAT). TAT is responsible of the current generation that degrades the subthreshold swing. This indicates the tight requirements for quality epitaxy growth and junction optimization in TFETs. Finally, we proposed novel TFET architectures. TCAD study shows that the extension of the source into the body region provides vertical BTBT and a larger tunneling surface. Ultra-thin heavily doped boron layers could allow the possibility to obtain simultaneously a good ON-current and sub-thermal subthreshold slope in TFETs.

Keywords: Tunnel FET, TFET, SOI, BTBT, Low-Temperature, 3D integration, Charge pumping, low-frequency noise, Extended-source, Pure Boron.

Caractérisation de transistors à effet tunnel fabriqués par un processus basse température et des architectures innovantes de TFETs pour l'intégration 3D

Cette thèse porte sur l'étude de transistor à effet tunnel (TFET) en FDSOI à géométries planaire et triple grille/nanofils. Nous rapportons pour la première fois des TFETs fabriqués par un processus basse température (600°C), qui est identique à celui utilisé pour l'intégration monolithique 3D. La méthode "Dual I_DV_{DS}" confirme que ces TFETs fonctionnent par effet tunnel et non pas par effet Schottky. Les résultats des mesures électriques montrent que l'abaissement de la température de fabrication de 1050°C (HT) à 600°C (LT) ne dégrade pas les propriétés des TFETs. Néanmoins, les dispositifs réalisés à basse température montrent un courant de drain et de fuite plus élevés et une tension de seuil différente par rapport aux HT TFETs. Ces phénomènes ne peuvent pas être expliqués par le mécanisme d'effet tunnel. Le courant de pompage de charges révèle une densité d'états d'interface plus grande à l'interface oxide/Si pour les dispositifs LT que dans les TFETs HT pour les zones actives étroites. Par ailleurs, une analyse de bruit basse fréquence permet de mieux comprendre la nature des pièges dans les TFETs LT et HT. Dans les TFETs réalisés à basse température nous avons mis en évidence une concentration en défauts non uniforme à l'interface oxide/Si et à la jonction tunnel qui cause un effet tunnel assisté par piège (TAT). Ce courant TAT est responsable de la dégradation de la pente sous seuil. Ce résultat montre la direction à suivre pour optimiser ces structures, à savoir une épitaxie de très haute qualité et une optimisation fine des jonctions. Finalement, nous avons proposé de nouvelles architectures innovatrices de transistors à effet tunnel. L'étude de simulation TCAD montre que l'extension de la jonction tunnel dans le canal augmente la surface de la région qui engendre le courant BTBT. Une fine couche dopée avec une dose ultra-haute en bore pourrait permettre l'obtention à la fois d'une pente sous le seuil faible et un fort courant ON pour le TFET.

Mots clés: transistor à effet tunnel, TFET, SOI, BTBT, basse température, intégration 3D, pompage de charges, bruit basse fréquence, jonction étendue, Bore.

List of constants, symbols and acronyms

Constant	definition	magnitude	Units
k/k_B	Boltzmann constant	1.38×10^{-23}	$J\cdot K^{-1}$
q	Elementary charge	1.602×10^{-19}	C
ε_{Si}	Si relative permittivity	11.8	dimensionless
h	Planck constant	6.626×10^{-34}	J·s

Symbol	definition	Units
A	Effective channel area	μm^2
α	Gate activity factor	dimensionless
β	Inverse of thermal voltage	V^{-1} or mV^{-1}
C_D	Bulk depletion capacitance	F/cm^2
C_{LOAD}	Load capacitance	F/cm^2
C_{ox}	Oxide capacitance	F/cm^2
$CV_{DD}{}^2$	Switching energy	J or eV
D_n	Electron diffusion	cm^2/s
$\Delta\Phi$	Tunneling window	V or eV
ΔV_G	Amplitude gate pulse	V
E_C/E_V	Conduction/Valence band energy	eV
E_F	Energy Fermi level	eV
E_G/E_g	Energy bandgap	eV
E_{max}	Maximum electric field	V/cm
E_T	Energy interface state level	eV
f	Frequency	Hz or GHz
f_{elas}	Elastic force	N
f_{elec}	Electric field-induced force	N
Φ_F	Fermi potential	V or eV
Φ_G	Gate work function	eV
$f_s(E)/f_D(E)$	Source and drain fermi distributions	dimensionless
$\varphi_s/\Delta\Phi_S$	Electrostatic surface potential	V or eV
g_m	Transconductance	A/V
I_{CP}	Charge pumping current	A
I_D	Drain/drive/tunneling current	µA/µm or A/ µm or A
I_{OFF}	Off current	µA/µm or A/ µm or A
I_{ON}	On current	µA/µm or A/ µm or A
I_{ON}/I_{OFF}	Device performance ratio	Dimensionless
I_P	Peak current	A or A/µm or µA/µm
I_V	Valley current	A or A/µm or µA/µm
λ	Tunneling length	nm
L_G/L	Gate length	nm
L_{IN}/L_I	Intrinsic region	nm
L_{rt}	Extension depth	nm
L_{und}	Underlapped region	nm
m^*	Effective mass	kg
N_D/N_A	Donor/Acceptor dopant concentration	cm^{-3}

N_{it}	Defect density	$cm^{-2} \cdot eV^{-1}$
P_{dyn}	Dynamic power consumption	W/cm^2
P_{static}	Static power consumption	W/cm^2
S_{id}	Drain current power spectral density	A^2/Hz
S_{Vfb}	Flat-band voltage power spectral density	V^2/Hz
S_{Vg}	Input-referred gate voltage noise	V^2/Hz
T	Temperature	K or °C
T_{BOX}	BOX Thickness	nm
$T(E)$	Tunneling probability	dimensionless
T_{Si}	Body thickness	nm
T_{WKB}	Tunneling probability WKB	dimensionless
V_{BG}	Back-gate voltage	V or mV
V_D	Drain voltage	V or mV
V_{DD}	Bias supply voltage	V or mV
V_{FB}	Flat band voltage	V or mV
V_G	Gate voltage	V or mV
$V_{G,base}$	Pulse base level	V or mV
$V_{G,top}$	Pulse top level	V or mV
V_p	Peak Voltage	V or mV
V_{pi}	Pull-in voltage	V
V_R	Reverse voltage	V or mV
V_S	Source voltage	V or mV
V_{TH}	Threshold voltage	V or mV
V_V	Valley Voltage	V or mV
W/W_{fin}	Channel width	nm
x_{depl}	Depletion width	nm

Acronym	**definition**
1D	Unidimensional
2D	Bidimensional
3D	Tridimensional
ALD	Atomic Layer Deposition
ATLAS-TFET	Atomically Thin and Layered Semiconducting Tunnel FET
BOX	Buried OXide
BTBT	Band-To-Band-Tunneling
CEA	Commissariat à l'Energie Atomique et aux Energies Alternatives
CFET	Complementary Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nanotubes
CP	Charge pumping
CPU	Central Processing Unit
CTFET	Complementary-TFET
CVD	Chemical Vapor Deposition
DG	Double Gate
DRAM	Dynamic Random Access Memory
DS	Dopant Segregation
DTFET	Drift TFET
ENIAC	Electronic Numerical Integrator And Computer
EOR	End Of Range
EOT	Effective Oxide Thickness
ESD	Electrostatic Discharge
ES-TFET	Extended-Source Tunnel FET

ETSOI	Extremely Thin Silicon On Insulator
FDSOI	Fully Depleted Silicon On Insulator
FinFET	Fin Field Effect Transistor
GAA	Gate-All-Around
GeOI	Germanium On Insulator
GIDL	Gate-Induced Gate Leakage
GRN	Graphene nanoribbon
HDD	Highly Doped Drain
HRTEM	High-Resolution Transmission Electron Microscopy
HT	High-Temperature
IC	Integrated circuit
IIS	Implantation Into Silicide
IMOS	Impact Ionization MOSFET
IRDS	International Roadmap for Devices and Systems
JLTFET	Junctionless Tunnel FET
JTFET	Junction Tunnel FET
KMC	Kinetic Monte Carlo
LDD	Lightly Doped Drain
LFN	Low-Frequency Noise
LT	Low-Temperature
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MuGFET	Multiple Gate Field Effect Transistor
NC-FET	Negative Capacitance MOSFET
NDR	Negative Differential Resistance
NEMS	Nano-Electromechanical Switches
NEREID	Nano-Electronics Roadmap for Europe: Identification and Dissemination
NW	Nanowire
PAI	Pre-Amorphization Implant
PB-TFET	Pure Boron Tunnel FET
PJTFET	Pocket-Junction modulation TFET
PNA	Post-Nitridation Anneal
RSD	Raised Source and Drain
SBFET	Schottky Barrier FET
SCE	Short-Channel Effects
SEM	Scanning Electron Microscope
SJL-TFET	Source Junctionless Tunnel FET
SOI	Silicon On Insulator
SPER	Solid Phase Epitaxy Regrowth
SRAM	Static Random Access Memory
SRH	Shockley-Read-Hall
SDG	Source Doping Gradient
SS	Subthreshold Swing
TAT	Trap-Assisted tunneling
TASE	Template-Assisted Selective Epitaxy
TCAD	Technology Computer-Aided Design
TEM	Transmission Electron Microscopy
TFET	Tunnel Field Effect Transistor
TMD	Transition Metal Dichalcogenides
TSB-TFET	T-Gate Schottky Barrier TFET
VLSI	Very-Large Scale Integration
WKB	Wentzel-Kramers-Brillouin
Z^2-FET	Zero subthreshold swing and zero impact ionization FET

Introduction

During the first half of 20th century electronics was based on the vacuum tube triode technology. A great number of innovations were developed such as amplification of audio signals or the first electronic computers powered by vacuum tubes in late 1940's and early 1950's (ENIAC). However, due to the increase of complexity in the electronic circuits implemented in new computer designs, the use of vacuum tubes was unsustainable and this technology became obsolete.

The invention of the transistor by William Shockley, John Bardeen and Walter Brattain in 1947 and the first bipolar junction transistor in 1948 (William Shockley), marked a milestone for the research in solid state electronics. Compared to previous technologies, transistors were more reliable, longer lasting, produced less heat and consumed less power. At that time transistors were fabricated as individual electronic components and eventually circuits implemented with this approach were extremely difficult to assemble. Therefore, despite of the astonishing capabilities the feasibility of this new technology required the miniaturization in order to reduce the effective cost of the elements. In 1958 Jack Kilby came up with the idea of monolithic integration and proved that devices could be made on a same substrate and interconnected "in situ". Robert Noyce requested the patent of the integrated circuit in 1959 with the aim to make multiple devices on a single piece of silicon to make interconnections as part of the process fabrication. From that moment on, integrated circuits began to include more devices (not only transistors, but also interconnects, capacitors, resistors, etc.). In 1965, Gordon Moore published a paper predicting that the density of transistors on a chip would double every 18 months [1]. He claimed that by 1975 a state-of-the-art microchip should contain 65000 transistors and the actual count on a memory chip of that period, was deviated only 1% with respect to Moore's analysis. Each new processor released since then has doubled the transistor count with respect to the previous one, because the technology companies adopted this strategic principle as a figure of merit to characterize the progress.

Since early-1980's the requirements for energy consumption reduction of the computer industry made the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) the main type of transistor for logic and memory applications. Moreover, CMOS (Complementary Metal Oxide Semiconductor) technology is still the basic building block of the circuitry for logic integrated circuits. From that moment and until late 1990's the geometry scaling of silicon transistors allowed one to fabricate smaller devices with a higher performance and a lower switching energy for each new technological node. However, it became clear that with the physical gate length approaching values of hundreds of nanometers it will not be longer possible to provide a good electrostatic control of Short-Channel Effects (SCEs) via front gate voltage. Another important limiting factor was the impossibility to continue scaling the gate oxide thickness (SiO_2). In early 2000's the semiconductor industry adopted the equivalent scaling path. The objective is to keep under control the SCEs not only with geometry reduction, but also using new materials for the channel layer or for the gate oxide, combined with new architectures based on multiple gates such as trigate/nanowire transistors to significantly improve the electrostatic control. A great number of boosters are being used to

continue increasing the performance, such as SiGe material, strained silicon, Gate-Last technology, high-k metal gate, etc. However, all these process fabrication improvements are not enough to achieve devices with very low power consumption.

During the last decade state-of-the-art microprocessors have experienced a change of paradigm with respect to the design rules. Currently, delivery of the highest performance possible is no longer always the major concern, and one often requires a computation efficiency which means the maximum performance at the lowest possible power consumption. This is consequence of the industrial needs for lower power consumption in battery-operated handheld devices. However, in nodes with a gate length shorter than 100 nm the static power consumption (device should be in off-state) has significantly increased to values close to the dynamic power consumption as shown in Figure 1.

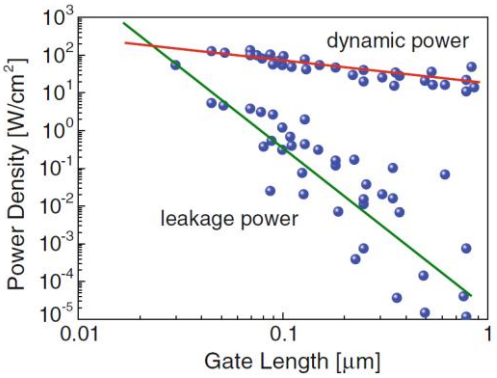

Figure 1. Evolution of dynamic and static (leakage) power consumption in CMOS technology with geometry scaling [2].

Therefore reduction of the static power consumption requires devices with a very steep subthreshold slope to minimize the off-current. Unfortunately, even the most innovative solutions in CMOS technology, such as FinFETs [3] or FDSOI [4] (Fully Depleted Silicon On Insulator) architectures, are unable to solve this problematic. The physics involved on the carrier injection mechanism of MOSFETs, thermionic emission of carrier overcoming a potential barrier, inherently tie the minimum achievable subthreshold swing value to 60 mV/dec at room temperature (Figure 2). This confirms the necessity to implement new physics in transistors in order to achieve very steep subthreshold slopes enabling the possibility to fabricate devices for ultra-low power applications (V_{DD} < 0.4 V).

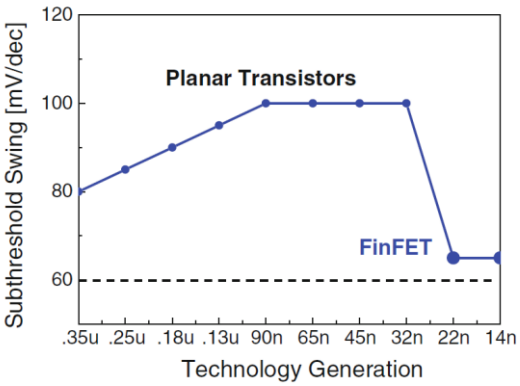

Figure 2. Subthreshold swing (SS) characterized in different CMOS technology generations. Last generation of planar structures SS was constrained to values close to 100 mV/dec. Only trigate architectures (FinFET or FDSOI) achieve SS values close to the thermal limit of 60 mV/dec [2].

The International Roadmap for Devices and Systems (IRDS) have identified a great number of devices with the potential capabilities to achieve SS below 60 mV/dec, called "Beyond-CMOS" devices [5]. However, there are important conditions to fulfill: firstly, the process fabrication of these steep slope devices must be compatible with the co-integration of MOSFETs. Secondly, the viability as a technology with possibilities to be extended for 3D Power scaling [6]. These conditions severely restrict the candidates, but Tunnel FETs (TFETs) still stand out as one of the most important. During the last decade TFETs have been extensively studied and considered as one of the most promising devices for ultra-low power applications. Unfortunately, the mismatch showed between experiments and simulations linked to the inability for achieving simultaneously a high on-current and a steep slope [7], focused the attention on other type of devices. Despite this context, TFET investigations are still ongoing because the technology is based on the same architecture, materials and boosters used in CMOS devices. This implies that successive improvements in process fabrication, specifically in junction formation and new epitaxy techniques for extremely thin film layers with a good quality control, will reveal the true performance of TFETs, that it is currently degraded.

The work of this thesis is focused on the study of FDSOI Tunnel FET devices from planar to trigate/nanowire structures. Its aim is to shed light on the capabilities of silicon or SiGe TFETs for ultra-low power applications. It also aims at identifying which are the major challenges that prevent TFETs to be co-integrated with CMOS technology. We have studied well-known parameters such as I-V characteristic, I_{ON}/I_{OFF} ratio and subthreshold swing which serve as performance indicators. We have measured devices made using different thermal budgets and extracted information on defects through charge pumping method and with low-frequency noise analysis (LFN). Using these measurements it is possible to differentiate whether TFET performance limitations are intrinsic to device physics or are a fabrication maturity issue. TCAD simulations were also used to evaluate possible device architecture improvements that can simultaneously lower the subthreshold slope and achieve higher high on-current.

The originality of this thesis work resides in:

1. The first demonstration of functional "Low-Temperature" (LT) Tunnel FETs based on a compatible CMOS process fabrication and with similar performance to conventional TFETs. This opens the door of TFETs as a potential candidate for 3D integration.

2. The confirmation that interface oxide traps and junction defects are not passivated enough with the LT annealing process. This results in a trap-assisted tunneling (TAT) effect, which generates a higher on-current in the subthreshold region that degrades the subthreshold slope.

3. The design and simulation of TFET device engineering and innovative planar architectures, proving the possibility to obtain simultaneously steep slope and high on-current via interband tunneling in extremely thin silicon films.

The manuscript is organized as follows:

Chapter 1. We explain why the equivalent scaling cannot overcome limitations on power consumption and delay degradation in ICs. It is also noticed the importance of power efficiency in the emerging and profitable handheld device market and the limitations of MOSFET physics for low-voltage application. Lastly, we identified the most studied Beyond-CMOS devices and explained why Tunnel FETs are still one of the most promising steep slope devices in spite of the current challenges in device performance.

Chapter 2. It is dedicated to the operation principle of Tunnel FETs and, in particular, the potential for achieving a steep subthreshold slope. Also, the main reasons for the discrepancy between simulated and fabricated devices are discussed. In addition, a TCAD study identifies the impact of different parameters (T_{Si}, L_G, L_{IN}, EOT and materials) on performance and allows one to highlight the most important challenges for TFET optimization. The structure and fabrication process of the TFETs made by the CEA are detailed and a list of the most interesting current research efforts on TFETs is provided. Finally, we benchmark the performance of the most important TFETs fabricated during the last decade.

Chapter 3. We report for the first time functional TFETs made with a low-temperature process, indicating that can be a promising candidate for 3D Power scaling such as CoolCube™. Using an electrical characterization method called "Dual I_DV_D" it is possible to determine if a device has a real interband tunneling behavior or if it is a Schottky FET. LT TFETs exhibit higher on-current and degraded off-current than their "High-Temperature" (HT) TFETs counterparts. Besides, a simulation study confirms the results obtained from experiments for gate overdrive voltages. Several hypotheses are made to explain this unexpected behavior.

Chapter 4. This chapter is focused on explaining why LT TFETs present a higher on-current and a higher leakage current than HT devices. Charge pumping measurements confirm a higher density of interface states at the top interface in LT than HT TFETs. Besides, a low-frequency noise analysis confirms that LT devices exhibit more traps in the junctions that give place to TAT tunneling current instead of interband tunneling, which degrades the subthreshold slope. These results suggest the evidence that the main constraints for a good TFET operation are related with the maturity of the current process fabrication.

Chapter 5. This chapter is dedicated to an extensively TCAD simulation analysis of innovative planar architectures to achieve simultaneously a steep subthreshold slope and a significant on-current. Best options rely on increasing the surface for the interband tunneling via extension of the tunneling junction into the body region. Also, a better electrostatic control can be achieved with extremely thin films.

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Chapter 1.
Context of the thesis and Beyond-CMOS devices

1.1. The end of planar scaling

Among all the available mechanisms to accomplish Moore's trend [1] in a cost-effective way, miniaturization or geometry scaling was identified as one of the most important. In order to fulfill this requirement during 1980's and 90's the industry relied on the "constant-field scaling" method proposed by Dennard *et al.* [2], that considers the impact of the device geometry scaling on the device performance. Basically, reducing the size of transistors increases their density on a chip, which for a constant chip size, increases the functionality of the circuits for a lower cost. Unfortunately, in the new millennium pure geometrical scaling came to an end (and with that Dennard's rules), because it was no longer possible to guarantee good electrostatic control of transistors due mainly to of Short-Channel Effects degrading the performance [3]:

1) Electric field-induced mobility degradation: the mobility of the carriers in the channel decreases when gate voltage is increased, due to surface roughness scattering.

2) Depletion capacitance of poly-Si gate and inversion layer capacitance: Both these effects increase the effective gate oxide thickness and, therefore, reduce the current drive of the transistor.

3) Subthreshold swing: the transistor cannot "instantly" switch from OFF to ON. The laws of thermodynamics impose the gate voltage to increase by at least $ln(10) \times kT/q$ (= 60 mV) in order for the current below threshold to increase a tenfold.

4) Parasitic resistance of devices: the shorter the channel, the larger the relative importance of source, drain and contact resistances.

5) Leakage current (gate insulator leakage, gate-induced drain leakage).

6) Threshold voltage roll-off with gate length.

7) Drain-induced barrier lowering: threshold voltage decreases with drain voltage.

In order to overcome all these undesired physical effects it is necessary to increase the performance via innovative boosters. Mobility degradation can be improved using different materials such as Germanium (with higher electron and hole mobility than silicon), SiGe or III-V compounds. Strain technology has also been widely used to boost mobility. Gate capacitance can be increased using high-k dielectrics in order to obtain a small EOT with a

relatively large dielectric film thickness, thereby avoiding gate tunnel current. Parasitic source and drain resistance is highly improved with raised source and drain and silicidation process. With respect to the off-current, the implementation of Silicon On Insulator (SOI) layers, isolating the body region from the substrate has demonstrated the reduction of leakage current by several orders of magnitude compared to bulk transistors. However, the issue of a steep subthreshold slope is still under investigation, CMOS technology is unable to provide a sub-thermal subthreshold slope (further explained in next section).

The implementation of these boosters is expensive and has caused a rapid increase of technology cost ($/mm^2) in every new technological node below 130 nm. But according to recent data (Figure 1.1), this higher cost can be offset by higher transistor density per mm^2 and by an increase of wafer volume production [4].

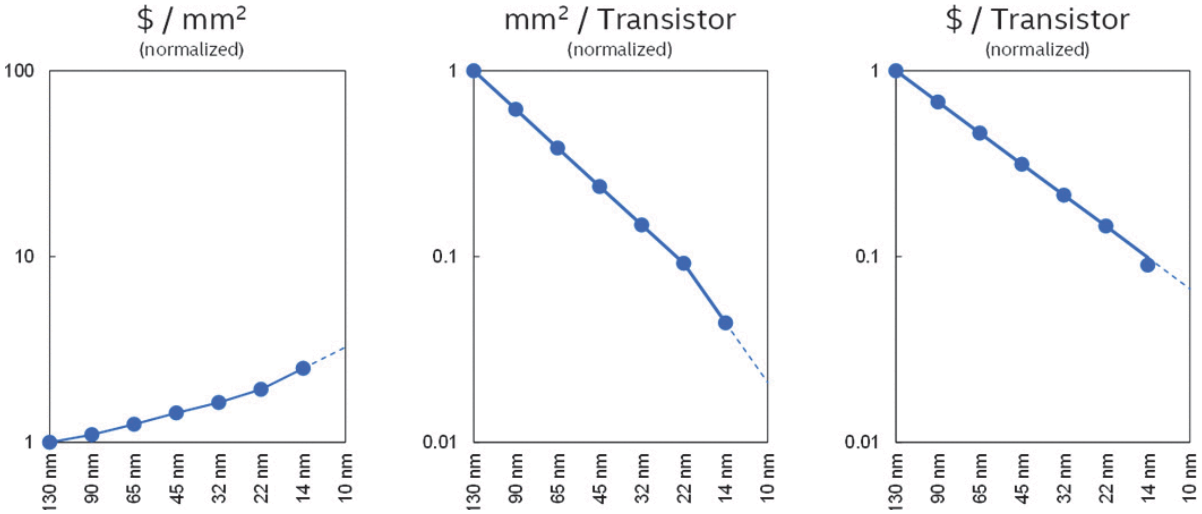

Figure 1.1. Increase of the cost/area in new nodes because of boosters and reduction of area/transistor with node scaling. Result is a reduction of the cost/transistor [4].

Moore's law has continued the historical trend of increasing transistor count (More Moore), but in in the last decade new options such as co-integration of CMOS with other functions (More than Moore) have emerged. Silicon transistor scaling continues to deliver higher performance and lower power in a cost-effective way. There is a strong demand for further scaling due to a great number of services that request superior performance. For example data centers, based on clusters of servers and memory banks, have a power consumption into the hundreds of megawatts range [5]. Unfortunately, IRDS has foreseen that after 2027 there will be no room for further 2D geometrical scaling, because it is projected that the physical channel length of transistors would saturate around 12 nm. In addition, below 5-10 nm of gate length undesired direct source-to-drain tunneling takes place, increasing the leakage current and degrading the performance of the device.

Trigate architectures such as FinFETs offer better electrostatic control than planar MOSFETs and will be used as the key device architecture in order to extend 2D scaling until 2021 for high-performance logic applications. However, beyond 2019, scaling of passive elements such as interconnects becomes one of the major concerns as a consequence of tightening design rules. Even before reaching such small gate length, the delay of metal interconnections is already much larger than gate delay, hence the global delay of the integrated circuit is degraded due to the dominance of the capacitance of the metal lines (Figure 1.2).

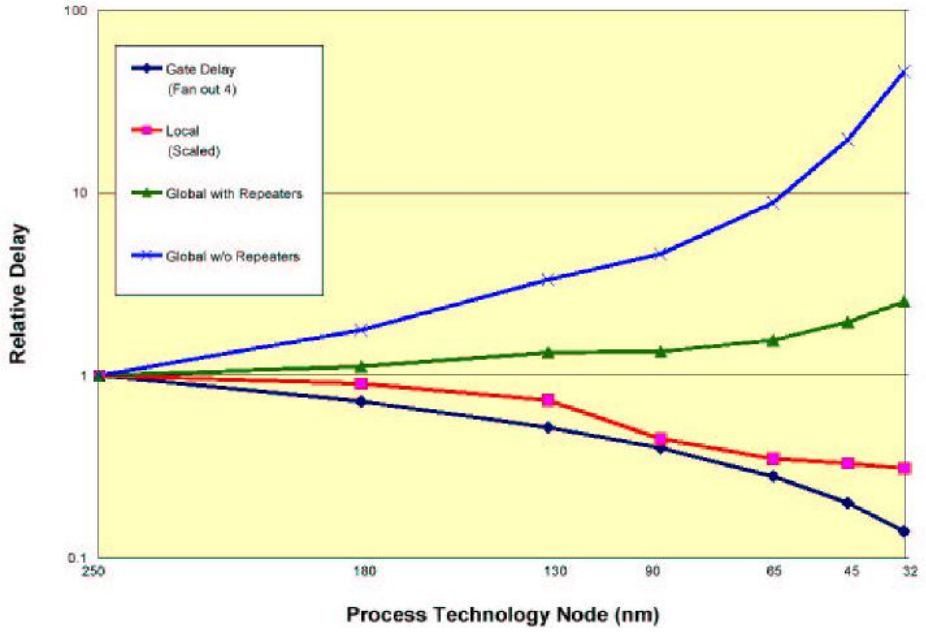

Figure 1.2. Projection of on-chip electrical interconnect delays with technology scaling [6].

When this happens, it will be necessary to develop a new technology called monolithic 3D integration. The idea is to fabricate devices on top of each other to maintain the transistor density, but shortening the overall metal interconnection length. Currently under research on trigate architectures, a transition to Gate-All-Around (GAA) it is mandatory in order to reduce the power supply and keep a good electrostatic control. Eventually an evolution to vertical structures will be necessary: beyond-CMOS devices with steep slope and the addition of new functionalities, such as the integration of several memory circuits on top of logic circuits.

The integrated circuit is the concept that triggered the era of information and technology in which we are living nowadays and caused an inflection point in our society. In addition, it has transformed the semiconductor industry in a profitable market size of over $350 billion.

1.2. Towards the path of enhanced power efficiency

The first computer system developed by IBM (System/360) was fabricated based on bipolar solid logic technology. At that time, bipolar transistors were better switches and more reliable than any MOSFET device fabricated so far. On the contrary, they presented a higher cost and also a higher power consumption than MOSFETs. Despite these drawbacks, since only large corporations could afford to buy a computer, expensive heat dissipation systems were implemented in order to obtain the maximum performance. The computer industry relied on bipolar technology until early-1980's. The apparition of the personal computer (1981) and the introduction of small computers at all levels of society confirmed that it was necessary to find an alternative to bipolar transistors, partly because large energy consumption was no longer sustainable. Therefore, CMOS technology with acceptable power consumption and lower cost than bipolar ICs, became the choice for logic and memory applications.

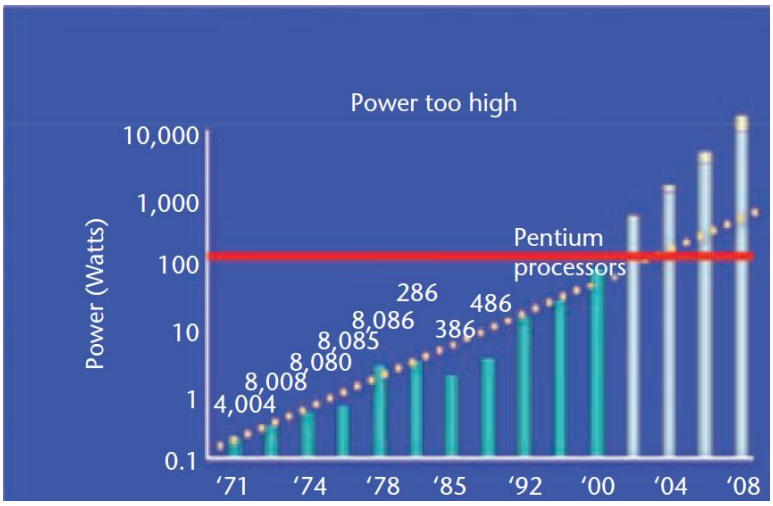

Figure 1.3. Power consumption of Intel's CPUs in history. In early 2000's the limit of 100 Watts was already reached [7].

Due to a lower switching energy in successive technology generations, each new released microprocessor could operate at higher frequencies and therefore, offered higher computer performance. Unfortunately, device shrinking was accompanied by an increase in IC power density. Figure 1.3 shows that the power consumption has increased from almost 2 W/cm^2 in the i386 processor (1.5 µm gate length) to nearly 100 W/cm^2 in Pentium processors (0.13 µm gate length). At this point it became clear that it would be impossible to simultaneously increase the transistor density and the operation frequency of microprocessors. Finally, the solution adopted was to continue increasing the number of transistors according to Moore's law, while limiting the microprocessors operating frequency to a few GHz in order to make ICs able to work under practical thermal conditions. However, to solve the limitations of this constraint with respect to the output performance, it was necessary to modify the process architecture from single core to multi-core. With this approach, each core would run up to 2 GHz, while the total output rate of the microprocessor is fold by the output combination of the multiple cores.

In order to fabricate low power logic devices it is necessary to understand what is causing an increase of the energy consumption during the binary switching in a CMOS inverter:

$$P_{consump} = P_{dyn} + P_{static} = \alpha f C_{Load} V_{DD}^2 + I_{OFF} V_{DD} \qquad (1.1)$$

Before specific ICs were fabricated for mobile phones, the voltage supply was still high (~3 V). From equation (1.1), one can notice that the most effective technique for decreasing power consumption in an integrated circuit is simply to reduce the supply voltage V_{DD}. However, Figure 1.4 shows that the scaling of V_{DD} below 0.8 V has become extremely challenging [8]. In order to keep up performance, which is proportional to the current drive $I_D \sim (V_{DD} - V_{TH})^2$, threshold voltage ($V_{TH}$) must be decreased together with V_{DD}. Reducing V_{TH} increases leakage current due to the finite value of the subthreshold slope, short channel effects and other effects such as random dopant fluctuation. This implies that for new technological nodes, the switching energy ($\sim CV_{DD}^2$) cannot be scaled as low as it should be due to the unmatched V_{DD} scaling and to the increase of short-channel effects with gate length reduction. When the threshold voltage is lowered, the OFF current increases exponentially, such that the static power consumption ($I_{OFF} \times V_{DD}$) reaches levels equal to those of the (useful) active power consumption.

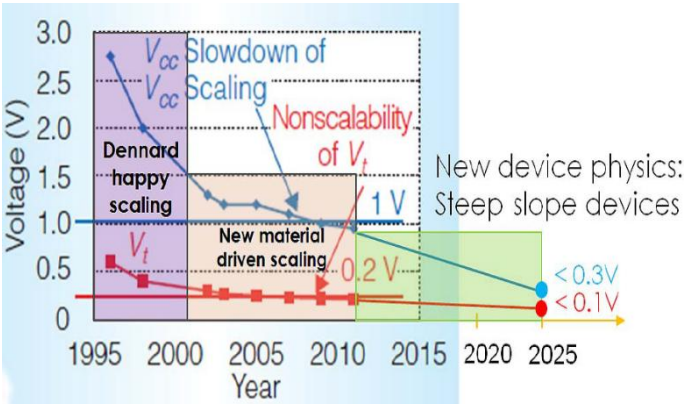

Figure 1.4. Supply voltage scaling (V_{DD}) based on Dennard's rules (early 2000's) and new material scaling (up to 2010). Currently V_{DD} scaling saturates at around 0.8 V [8].

1.2.1. CMOS limitation for low-voltage applications

Transport in MOSFET devices is based on the drift-diffusion mechanisms. For an N-type bulk MOSFET (p-type substrate) with no applied bias, majority carriers from source and drain junctions (electrons) diffuse into the channel region (Figure 1.5a). The same occurs for the majority carriers in the channel (holes) that diffuse towards the source and drain. As a result depletion regions are created in the junctions, together with potential barriers (local potential variations). Under thermodynamical equilibrium the diffusion current is exactly compensated by the drift current due to the potential variations. If a positive gate voltage is applied, the energy of the barriers start to decrease, electrons can diffuse from the source and drain in the P-type region, and an inversion layer is created at the channel surface, connecting the source and drain. If a positive drain voltage is applied, electrons can flow from source to drain.

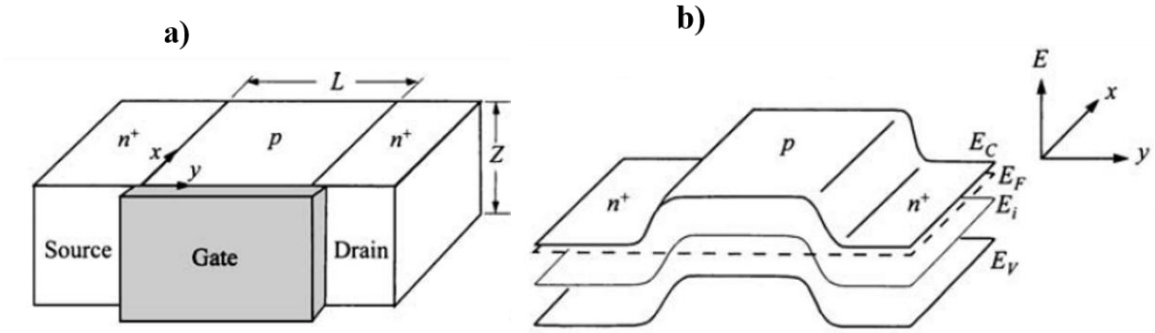

Figure 1.5. (a) N-channel MOSFET device structure schematic; (b) Energy band diagram in flat-band zero-bias equilibrium condition. High energy barriers at the junctions prevent that electrons cross towards the drain terminal [9].

The channel charge density in a MOSFET is given by the Boltzmann distribution:

$$Q \propto e^{\frac{q\phi s}{K_B T}} \qquad (1.2)$$

where ϕ_s is the surface potential at the Si/insulator interface. As the subthreshold current is proportional to the charge density, the drain current in a MOSFET can be expressed by [10]:

$$I_D = \frac{D_n W C_D k T e^{\phi_s}}{L q e^{2\phi_F}} \left(1 - e^{-\beta V_D}\right) \qquad (1.3)$$

From equation (1.3) we can calculate the subthreshold swing, which is an important figure of merit to determine if a device is a good candidate for ultra-low power applications.

$$SS \stackrel{\text{def}}{=} \frac{dV_G}{d(\log_{10} I_D)} = \frac{dV_G}{d\phi_s}\frac{d\phi_s}{d(\log_{10} I_D)} = m \times n \qquad \textbf{(1.4)}$$

Subthreshold swing indicates how much voltage one must apply to the front gate terminal to achieve an increase change of the drain current by one order of magnitude. This provides a measure of how abruptly a device can be switched from off-state to on-state. A lower SS is desirable because it represents a sharper switching between the ON and OFF states. Conversely a higher SS implies "spending" a grand deal of gate voltage to turn the device from OFF to ON. The term m in equation (1.4) is the body factor and for a bulk MOSFETs is given by relationship $m = 1+C_D/C_{ox}$, where C_D is the bulk depletion capacitance and C_{ox} is the gate oxide capacitance. Both C_{ox} and C_D are positive in CMOS technology, so the best case scenario occurs when $C_{ox} >> C_D$ and thus, m is close to unity although slightly greater. The term n is given by:

$$n = \frac{d\phi_s}{d(\log_{10} I_D)} = \ln(10)\frac{K_B T}{q} = 2.3 \times 25.8\frac{mV}{dec} \sim 60\frac{mV}{dec} \qquad \textbf{(1.5)}$$

Equation (1.5) confirms that the kT/q term is limiting the minimum achievable subthreshold slope of MOSFETs to 60 mV/dec at room temperature (300K). It is a fundamental limit due to the Boltzmann distribution of electrons in the energy bands. When SCEs began to degrade the electrostatic behavior of the devices (technology node 0.35 µm), the doping of the channel region was progressively increased to achieve reduced short-channel effects. However, a higher doping caused a reduction of the depletion width and therefore a higher C_D ($\sim \varepsilon_{si}/x_{depl}$), increasing the body factor and the subthreshold swing. The last bulk technology nodes based on planar architectures (from 90 nm to 32 nm) introduced high-k materials for the gate oxide to keep a constant C_D/C_{ox} ratio from node to node, obtaining values of SS around 96 mV/dec [11]. However, this value is too high for low-power applications purposes. The introduction of trigate architectures such as FinFETs allows one to reduce the SCEs without increasing the channel doping and C_D is significantly reduced (with values of n close to 1.1), achieving SS values in the range of 65-75 mV/dec. Similar results are obtained for FDSOI architectures owing to the presence of the Buried Oxide (BOX) layer.

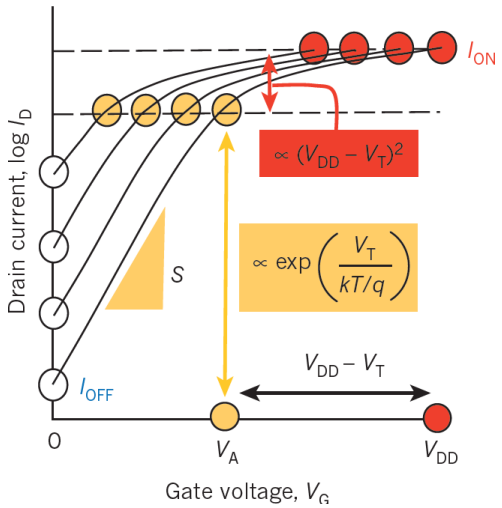

Figure 1.6. Transfer characteristic of a MOSFET showing that for a fixed subthreshold slope, reducing the threshold voltage implies a significant degradation (increase) of the off-current [12].

Unfortunately, it is not possible to reduce SS below 60 mV/dec in a MOSFET, even in the absence of SCEs.

Figure 1.6 shows that a reduction of the bias supply V_{DD} requires also the proportional reduction of V_{TH} to maintain constant performance (constant current drive). However, reducing V_{TH} implies increasing the off-current and, therefore, increasing the static power consumption. As a result, MOSFET technology is not suitable for ultra-low power applications (V_{DD} < 0.4 V). The only way V_{TH} can be reduced without increasing the OFF current is to reduce the subthreshold slope (SS < 60 mV/dec). Such devices will need to be based on different physics principles with a different carrier injection mechanism than in MOSFET. An ideal steep slope switch enables the reduction of the threshold voltage without increasing the off-current (Figure 1.7) compared to a regular switch. There are two possibilities: either obtain a body factor slightly higher than unity ($m > 1$) and $n < 60$ *mV/dec* (Tunnel FETs, Phase-FETs) or $m < 1$ (negative capacitance effect) and $n \sim 60$ *mV/dec* as happens in Ferroelectric-gate "negative capacitance" FETs.

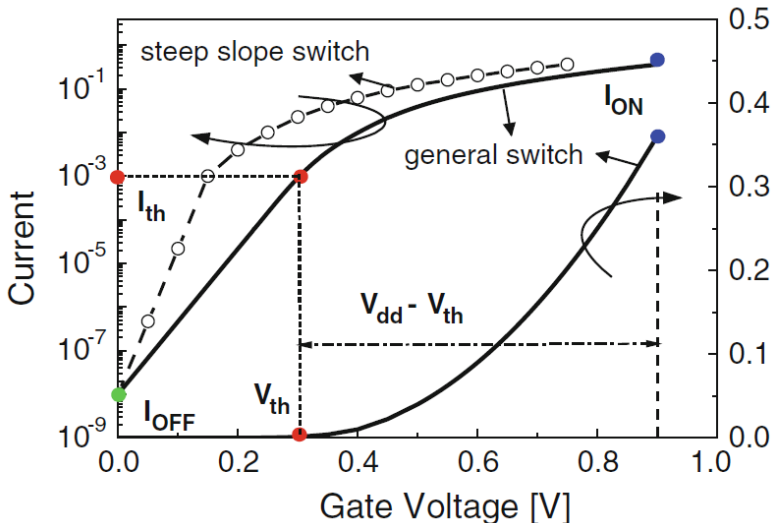

Figure 1.7. $I_D(V_G)$ curves of a general switch and a steep slope switch. With a steep subthreshold slope it is possible to reduce V_{TH} without degrading the off-current [11].

1.3. Beyond-CMOS devices

Innovative computing paradigms and applications such as big data, artificial intelligence, exascale supercomputing and robotics are requesting simultaneously higher performance and efficiency requirements that are extremely challenging to provide using the current CMOS technology, despite of all the implemented boosters [13]. However, beyond-CMOS technologies based on state-of-the-art architectures, processes and materials open the door to new solutions that can be extended even for 3D power scaling. According to the European NEREID project, a significant investment effort has been done in emerging computing paradigms, namely: Quantum computing, Molecular Electronics, Spintronics, 2D materials, Neuromorphic computing and beyond-CMOS. Of course, the disruption from the classical von Neumann approach differs in each case. Quantum and Neuromorphic computing completely disrupts all system levels from device to algorithm [14], while for extended and beyond-CMOS only the device and logic levels are affected right now, although 3D power scaling will most likely also have an important impact on the processor's microarchitecture.

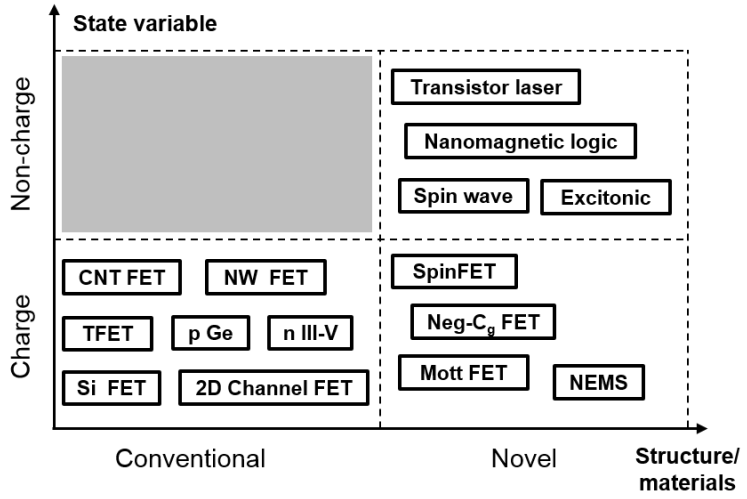

Figure 1.8. Classification of beyond-CMOS devices based on the structure/materials (conventional or novel) and the computational variables charge (voltage, current), non-charge (spintronic, orbitronic) [13].

Figure 1.8 shows the classification done by IRDS for emerging logic devices, based on the level of innovation of structure/materials (similarity with the current CMOS process fabrication), with charge based devices (transistor-like) or non-charge devices (sprintronic or orbitronic). Recently, benchmarking studies have been published with beyond-CMOS devices for logic integrated circuits [15] and boolean and Neuromorphic representative circuits [16]. Despite the fact that the majority of devices are evaluated via simulations, results suggest a general trend indicating that steep slope switches present some advantages over high-performance CMOS in terms of lower switching energy, though they are inferior to CMOS in delay (slower switch). Now, we present some of the most promising steeper slope devices that have already been fabricated.

1.3.1. Impact ionization MOSFET (IMOS)

The impact-ionization field-effect transistor (IMOS) [17] uses modulation of the impact ionization (avalanche breakdown) of a gated p-i-n structure to realize sharp switching. Figure 1.9a shows the schematics of an n-channel IMOS device with an intrinsic region between gate and source. On the contrary to MOSFETs, where the carriers are supplied by thermal injection from the source to the channel, carriers in IMOS are provided by avalanche breakdown in the intrinsic region (L_I) from the source to the channel when $V_G > V_{TH}$ (Figure 1.9c). The role of the gate is to accumulate electrons (N^+ electrostatic doping) that reduce the effective length from the nominal value (OFF state) to that of the intrinsic region (ON state) increasing the lateral effective field.

Very steep slopes have been obtained for p-channel SOI IMOS (L_G = 2 µm, L_{IN} = 0.2 µm) in the range of 10-15 mV/dec [18] and for complementary IMOS on SOI (L_G = 200 nm = L_{IN}) down to 2 mV/dec with on-current similar to CMOS [19]. Unfortunately, the threshold voltage and the drain polarizations required to trigger avalanche breakdown are too large (~ 20 V), although the breakdown voltages scale down in smaller geometry devices with a reduced intrinsic region [18]. In addition, when the device is under stress with repeated measurements, the threshold voltage increases monotonically and the subthreshold swing is severely degraded. This is consequence of the high electric field needed for avalanche

breakdown, causing hot carrier injection into the gate dielectric. There are reliability issues because of damage created by the impact ionization process to the gate oxide and spacers.

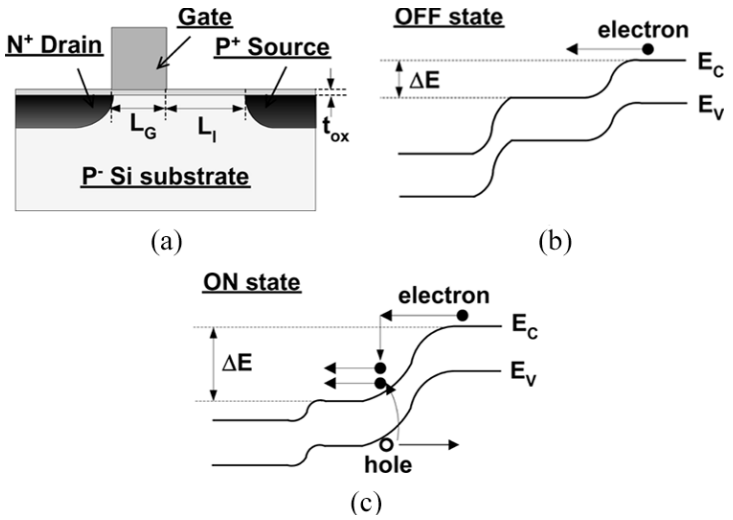

Figure 1.9. (a) Schematics of an n-channel IMOS device. (b) Energy band diagram in off-state. When $V_G < V_{TH}$ the electric field between channel and drain is not high enough to trigger the impact ionization. (c) For $V_G > V_{TH}$, the effective channel length is reduced and avalanche breakdown is triggered, causing an abrupt increase of the drain current [20].

1.3.2. Z^2-FET

The Z^2-FET is a forward biased p-i-n diode fabricated in FDSOI technology and featuring an intrinsic region (L_{IN}), which is not covered by the front gate. Figure 1.10a presents the schematics of a p-type Z^2-FET, where the P$^+$ source is grounded ($V_S = 0$), and the N$^+$ drain is forward biased ($V_D < 0$). The negative and positive polarizations of the front and bottom gates ($V_G < 0$, $V_{BG} > 0$) create a hole injection barrier in the L_G region and an electron injection barrier in L_{IN} region, disabling the carrier flow at low drain voltage. With this configuration we have a pnpn thyristor-like structure. The operation principle of the Z^2-FET involves a strong positive feedback between the carrier flow and the gate-controlled injection barriers that turns on the device sharply due to the suppression of both injection barriers (with no need of impact ionization) [21]. The $I_D(V_G)$ curve in Figure 1.10b shows an abrupt subthreshold slope (< 1 mV/dec), a high current I_{ON}/I_{OFF} ratio > 10^8 at supply voltage around 1 V.

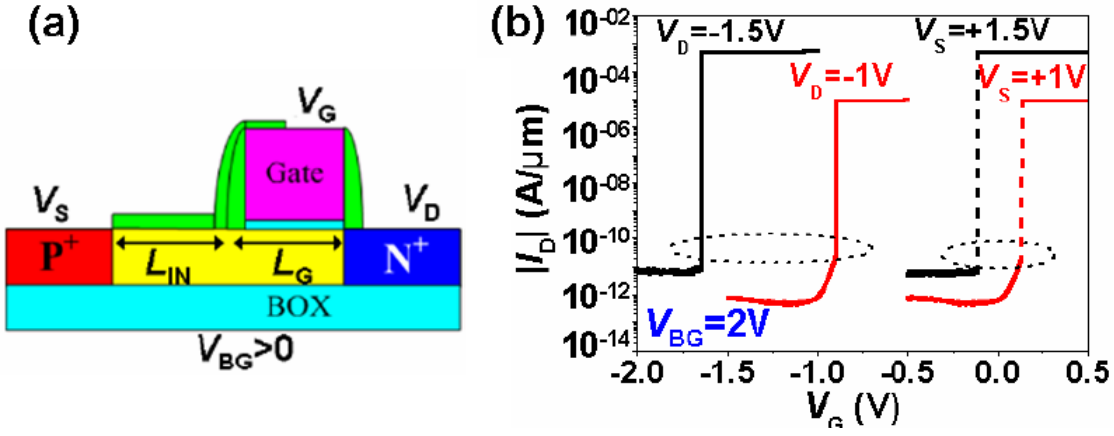

Figure 1.10. (a) Schematic of a p-type Z^2-FET. (b) Transfer characteristics showing a steep subthreshold slope for a Z^2-TFET with T_{Si} = 20 nm, T_{BOX} = 145 nm, L_G = 400 nm and L_{IN} = 500 nm [22].

The $I_D(V_D)$ curves of the Z^2-FET exhibit a gate-controlled hysteresis, which in fact limits the possibilities of this steep switch device for logic circuits unless very fast pulses are applied on the gate [23]. On the other hand, the hysteresis makes the Z^2-FET very interesting for memory applications, such as capacitor-less single-transistor DRAM (1T-DRAM), single-transistor SRAM or Electrostatic Discharge (ESD) protection and charge sensors.

1.3.3. Negative capacitance FET (NC-FET)

The negative capacitance MOSFET aims at achieving a steep slope by boosting the increase of the surface potential φ_s with respect to the gate voltage, instead of modifying the carrier injection mechanism. In conventional MOSFETs fabricated with high-k dielectrics, C_{ox} is always positive and it is not possible to achieve a body factor $m < 1$. To reduce the body factor below unity, one can replace part of the gate dielectric by a material that has a "negative capacitance", which can be obtained using some ferroelectric materials [24]. Using such a gate stack, the surface potential can increase faster than the gate voltage, creating a large amount of charge and a higher current compared to a conventional MOSFET. Experimental devices with ferroelectric/SiO_2 gate stack reporting a SS of 13 mV/dec have been demonstrated [25]. Unfortunately, a permanent polarization of the ferroelectric layer is usually observed, which results in a shift of the threshold voltage and a hysteresis effect in the $I_D(V_G)$ curves. This effect is extremely useful for memory applications but it jeopardizes the use of such materials for logic gates, because the gate voltage partly loses ability to turn off the device. Different solutions to suppress the hysteresis can be found in the literature.

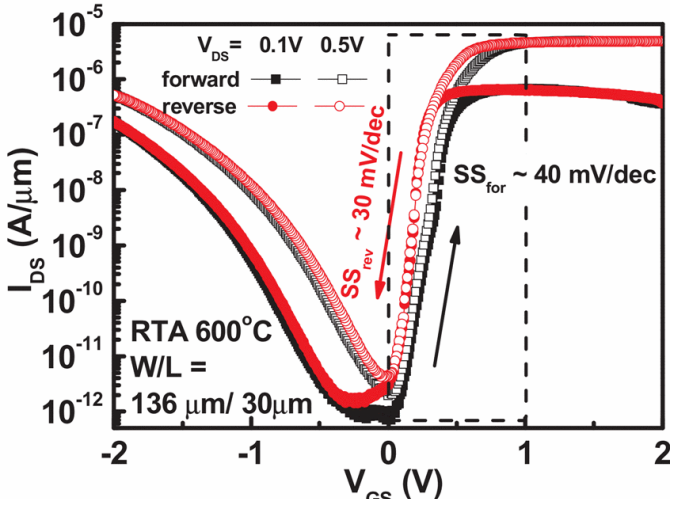

Figure 1.11. $I_D(V_G)$ curves of a Fe-HZO FET showing a reduced hysteresis window of 0.1 V and a subthreshold swing below 60 mV/dec for forward and reverse bias ramps [26].

Recently, a ferroelectric HfZrOx (Fe-HZO) FET was reported exhibiting a small hysteresis window with a V_T shift below 0.1 V (Figure 1.11) and a subthreshold swing below 60 mV/dec [26]. Moreover, some strategies to achieve hysteresis-free devices have been proposed, for example a gate stack formation of Fe-HZO/epi-Ge/Si FETs with an experimental 3 mV V_{TH} shift [26] and the first reported NC-FinFET with HfZrO2 with higher ferroelectricity (higher crystallinity by annealing at higher temperature) that suppresses the hysteresis [27]. Despite of all the efforts, there are still important challenges with respect to the ferroelectric material growth and process compatibility with conventional MOSFET process fabrication.

1.3.4. Nano-electromechanical Switches (NEMS)

Nano-electromechanical switches (NEMS) based on a mobile gate have also been considered for ultra-low power applications, because of two important characteristics: firstly, they feature a zero off-state leakage current and secondly, they have a zero subthreshold swing [28]. In early 2000's a device called the NEM-FET was proposed, which combined a conventional MOS transistor and a suspended metal membrane [29], [30] as shown in Figure 1.12a. The operation principle is simple: when a gate voltage is applied, there is an electric field-induced force (f_{elec}) that reduces the air gap, so the intrinsic voltage in the gate oxide is tuned with the capacitor divider formed by C_{air} and C_{ox}.

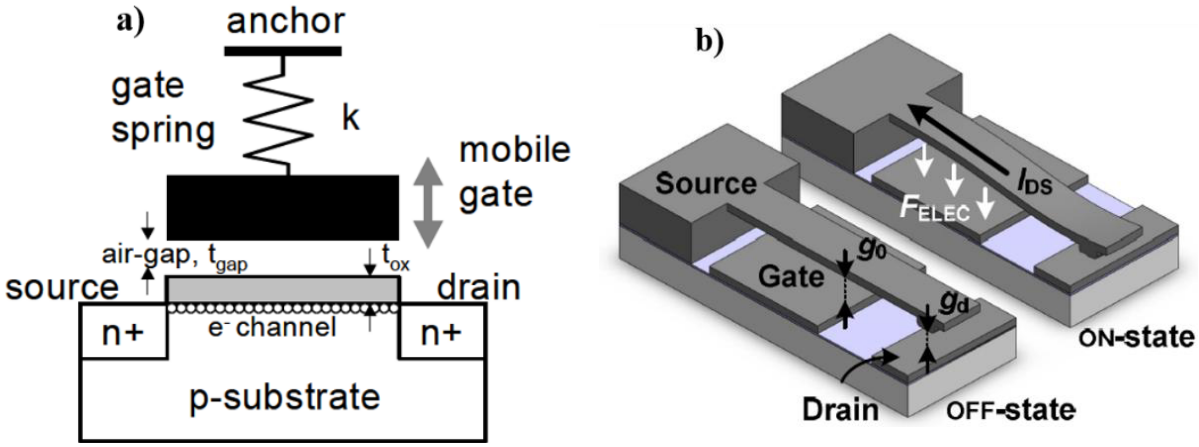

Figure 1.12. (a) Schematic of a Suspended-Gate MOSFET with a mobile gate terminal [30]. (b) Schematic of a planar three terminal electrostatic switch [31].

Simultaneously, an elastic force appears (f_{elas}) with same magnitude as f_{elec}, but in opposite direction. At a given gate voltage V_{pi} (pull-in voltage) the system balance is lost and the gate terminal connects to the gate oxide. Therefore, there is abrupt change in the surface potential (amplification) from the intrinsic voltage to the V_{pi}, which induces an increase of the drain current. An experimental SS of 2 mV/dec was reported, together with an ultra-low leakage current (< 0.1 pA) due to the air gap [30]. However, the gate voltage required to trigger the effect is quite high (~9 V). Furthermore, a shift in the V_{pi} voltage appears after several OFF/ON cycles due to oxide degradation, giving rise to a hysteresis effect. This renders the device rather unsuitable for logic applications. In addition, this device cannot be easily scaled down.

During last decade, a great effort has been done to improve the design (Figure 1.12b) and reliability of integrated circuits based on mechanical relays [31], but miniaturization is still one of the main challenges. Unfortunately, logic NEMS still suffers from requiring large supply voltages and large area compared to MOSFETs. In addition, the fabrication steps are very different from those used in conventional CMOS technology [28]. Nowadays, the use of electromechanical switches is oriented to auxiliary devices to help conventional CMOS circuits for being more energy efficient, for example as non-volatile elements to facilitate the power gating without data loss in the registers. The idea is to use the back-end-of-line process to integrate 3D NEMS switches with CMOS transistors for ultra-low power logic and memory circuits.

1.3.5. Tunnel FETs (TFETs)

Tunnel FETs are considered as one of the most feasible contenders for ultra-low power applications because they have the theoretical capability of providing a sub-thermal subthreshold slope. This is possible because TFETs rely on interband tunneling as carrier injection mechanism, which is temperature independent. Unfortunately, TFETs are very sensitive to defects located in the semiconductor region and at the interface. The trap-assisted tunneling (TAT) mechanism, which is temperature dependent, is causing band-to-band tunneling (BTBT) to occur when the device is supposed to be turned off, resulting in a generation current that degrades the subthreshold slope. This explains why very few experimental TFETs reach a SS below 60 mV/dec [32].

A qualitative comparison between TFETs and the rest of the previously listed steep-slope devices suggests that TFETs have a lower on-current and a less steep subthreshold slope than the IMOS, the Z^2-FET, the NC-FET and NEMS. However, the TFET is still the most studied and fabricated steep-slope switch device for low-power logic applications purposes. The main reason for so much research ongoing on TFETs is that TFETs have the same architecture/materials boosters as CMOS devices, and thus their fabrication is compatible with CMOS. In addition, TFETs do not present hysteresis effects and the gate terminal has full control on the device operation. According to the IRDS, the TFET is one on the most viable devices for the 3D power scaling and can be co-integrated with CMOS for future applications leveraging many parallel cores.

For these reasons, it is so important to understand the major problems that prevent TFETs from simultaneously achieving a steep slope and a high on-current, and to explore solutions that can eventually solve these issues.

1.4. Conclusions

Silicon transistor scaling continues to deliver higher performance and lower power in a cost-effective way for each new technology generation. In order to accomplish the control of the SCEs, the equivalent scaling allows one to increase the performance not only through geometry reduction, but also via innovative materials and new architectures based on multiple gates such as FinFET or FDSOI technology to enhance the effective electrostatic control.

State-of-the-art microprocessors are nowadays designed based on very tight and restrictive power consumption rules. Currently, deliver the highest performance possible is no longer always the major concern; we need to provide the maximum performance at the lowest possible power consumption. Unfortunately, equivalent scaling cannot overcome the limitations on power consumption and delay degradation in logic integrated circuits. Moreover, specific integrated circuits for ultra-low power applications will demand a bias supply lower than 0.4 V, but in CMOS technology scale V_{DD} below 0.8 V has become extremely challenging. The reason is that the physics involved on the carrier injection mechanism of MOSFETs, limits the subthreshold swing to a minimum value of 60 mV/dec at room temperature. V_{DD} reduction requires also the proportional reduction of the threshold voltage to maintain a constant performance. However, V_{TH} reduction increases the off-current and therefore the static power consumption. As a result, MOSFET technology is not suitable for ultra-low power applications (V_{DD} < 0.4 V). It is mandatory to introduce new physics in the transistors to modify the carrier injection mechanism.

Beyond-CMOS devices have the capabilities to achieve a sub-thermal subthreshold slope (SS < 60 mV/dec). IRDS have identified a great number of potential candidates, but here we highlight the most feasible candidates besides from Tunnel FETs, namely: Impact ionization MOSFET (IMOS), Z^2-FET, Negative capacitance FET (NC-FET) and Nano-electromechanical Switches (NEMS). Despite of the general low performance of TFETs architectures, this technology is still considered the most promising contender for ultra-low power applications since it fulfills important conditions: firstly, TFET process fabrication is fully compatible with the co-integration with MOSFETs. Next, TFETs do not present hysteresis effect that degrades the electrostatic control for logic purposes. Finally, IRDS has identified TFETs as a viable technology with significant capabilities to be extended for 3D Power scaling.

The key messages of this chapter are: First, **in next decade the semiconductor industry will face the end of 2D geometrical equivalent scaling**, and new options as co-integration of CMOS with other functions will emerge. Secondly, **tightening integrated circuits design requirements for ultra-low power consumption (bias supply) are unattainable for MOSFET technology and new physics in transistors are necessary**. Beyond-CMOS devices have the potential capabilities to provide sub-thermal subthreshold slopes. Specifically, **Tunnel FET technology gathers the most important conditions to be considered a realistic choice for 3D Power scaling. This thesis aims at determining the nature of the TFET performance limitations and the possible solutions.**

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Chapter 2.
Tunnel FET devices

2.1. Interband tunneling (Esaki diode)

According to classical mechanics, in a PN diode an electron in the conduction band of the N-region can be injected into the P-region only if it has an energy higher than the built-in potential; otherwise the electron cannot cross the barrier. However, according to the laws of quantum mechanics an electron is represented by a wave function. So, if the width of this potential barrier is thin enough (space charge region in the diode), there is a finite probability that an electron can tunnel through it.

The tunnel effect was reported for the first time by Leo Esaki in 1958 [1] on narrow Germanium p-n junctions. The I-V characteristic of this device presents a non-conventional behavior in forward bias (Figure 2.1a). A negative differential resistance (NDR) means that when the voltage is increased beyond V_P, a current decrease is observed [2]. Note that, this behavior cannot be explained by the equation $I = I_S([exp(qV/kT)] - 1)$ for a regular p-n diode. The latter expression can only account for the diffusion current component in Figure 2.1b.

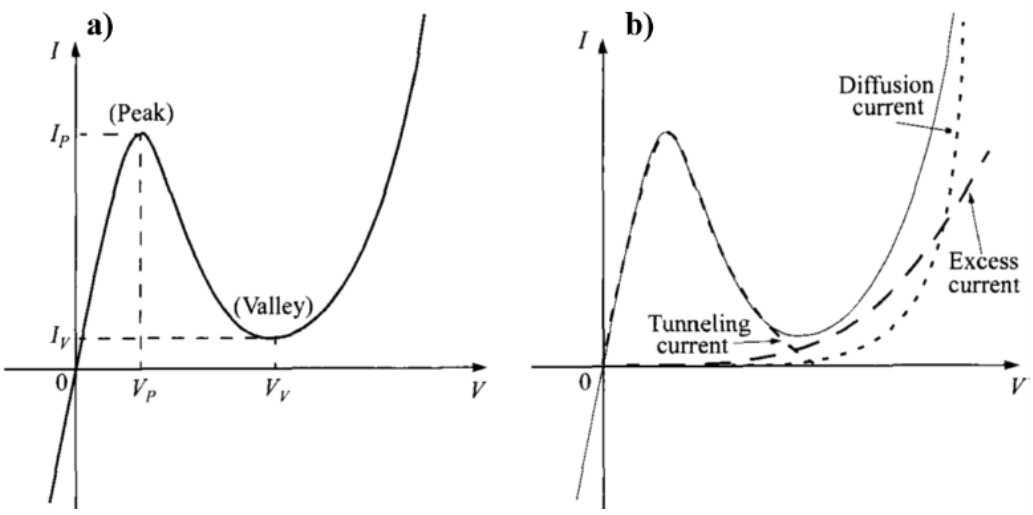

Figure 2.1. (a) I-V characteristic of a Germanium p-n junction with NDR between the regions (I_P, V_P) and (I_V, V_V). (b) Split of the total current in three components: tunneling current, excess current and diffusion current [3].

In a PN tunnel diode the tunneling occurs when the P- and N-type regions are degenerately doped. The Fermi level in the P-type is below the maximum of the valence band and in the N-type region it is above the minimum of the conduction band (Figure 2.2a). Because of the heavy doping concentrations, the depletion region is very thin (~ 10 nm) increasing the probability of tunneling through the depletion potential barrier. It is important to recall that during tunneling the energy of the electron is conserved. It thus moves on a horizontal line in energy-band diagrams [4].

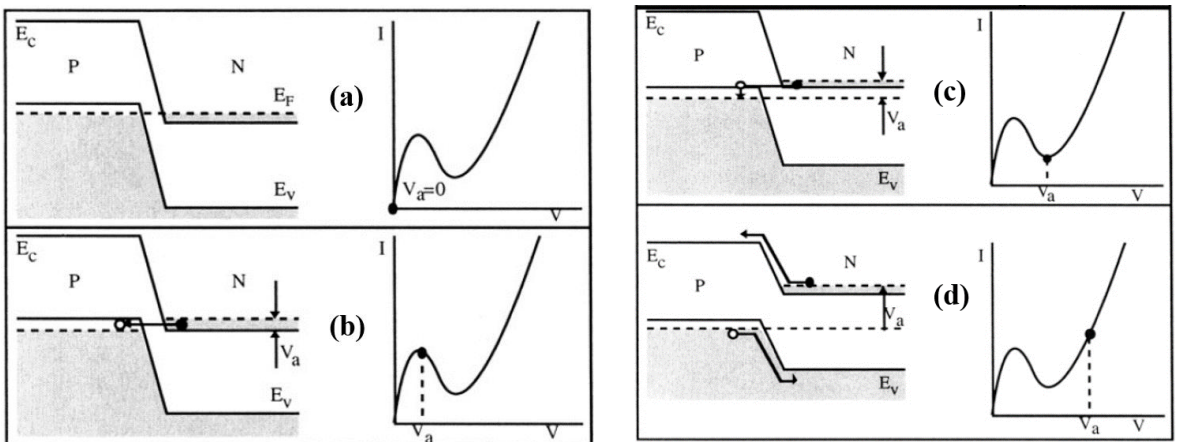

Figure 2.2. Energy band diagrams of a tunnel diode in forward bias; (a) at zero bias; (b) peak tunneling current; (c) valley current; (d) diffusion current [4].

In order to understand the I-V curve of a tunnel PN junction (Figure 2.1a), the energy band diagrams are used (Figure 2.2) under different bias conditions [4]:

a) **At zero applied bias:** The Fermi-Dirac distributions are equal for both P- and N-type regions because there is a single Fermi level in the entire structure, such that the tunneling current is equal to zero.

b) **At forward bias (up to V_P):** In the N-type region the quasi-Fermi level and the energy bands move up regards to the P-type region. This way, electrons from the conduction band of the N-region can tunnel into empty states in the valence band of the P-region. Applying V_P, the energy of majority large number of electrons in the conduction band of the N-region is equal to that of the empty states in the valence band of the P-region, so tunneling can occur, resulting in a peak of current when the energy overlap of empty states in the valence and occupied states in the conduction band is maximized (Figure 2.2b).

c) **At forward bias (up to V_V):** If the forward bias is increased beyond V_P, the overlap of the conduction band of the N-type region with the valence band in the P-type side decreases. As a result the tunnel current decreases because of the lack of allowed states of corresponding energies for tunneling (Figure 2.2c). The "valley" operation point is reached when there are no longer any available energy states for tunneling.

d) **Forward bias beyond V_V:** The barrier potential is significantly reduced and electrons (holes) have enough energy to overcome the barrier to the P-region (N-region). Diffusion current dominates over drift current and the behavior is the same as for a regular forward biased PN junction diode (Figure 2.2d).

For reverse bias conditions, a similar tunneling mechanism can take place. This time electrons from the valence band of P-type region tunnel into the conduction band of N-type region.

2.2. Tunnel FET operation

Tunnel FETs (TFETs) are reverse-biased gated p-i-n diodes in which the on-state current is generated by band-to-band tunneling carrier injection [5]–[7], as opposite to CMOS technology where the transport current is based on the thermionic emission of carriers overcoming the potential barrier (detailed in Chapter 1). Besides, a single TFET device can be used either in n- or p- operation mode.

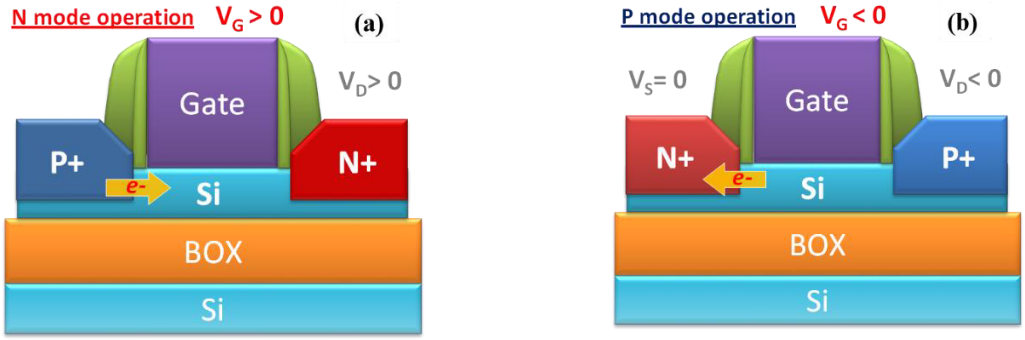

Figure 2.3. TFET bias scheme for (a) n-mode operation with positive polarization in the gate and the drain (cathode); (b) p-mode operation with negative polarization in the gate and the drain (anode).

In a standard Tunnel FET architecture the BTBT generation always takes place at the source/channel junction. In N-TFET configuration (Figure 2.3a) tunneling occurs at the P^+-I junction, while for a P-TFET mode it takes place at the N^+-I junction (Figure 2.3b).

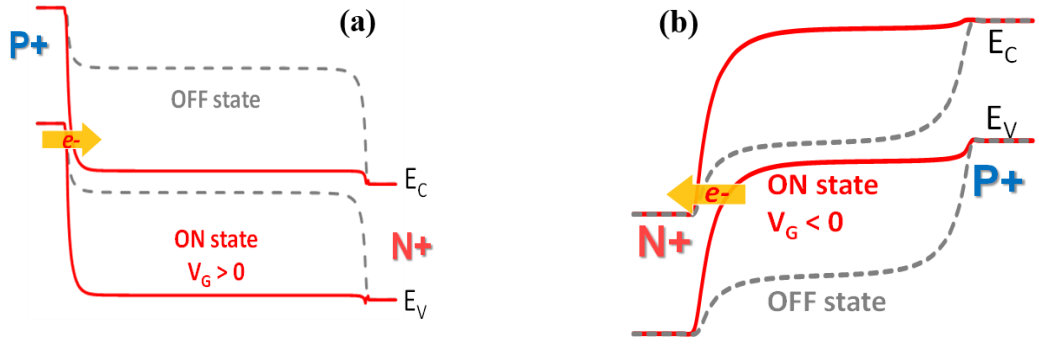

Figure 2.4. Energy band diagram showing the OFF state (dashed grey lines: the distance between the N^+ and P^+ region is too long for BTBT to occur) and ON state (solid red line: abrupt P^+-N^+). (a) in N-TFET, the N^+ region under the gate is due to the formation of an electron inversion layer for $V_G > 0$ V; (b) in P-TFET, the P^+ region under the gate results from the formation of an hole inversion layer for $V_G < 0$ V.

For N-mode operation in the **off-state** (at zero gate voltage), $E_{C,chan} > E_{V,p}$ and the tunneling length is too wide for interband tunneling to occur. When applying a positive gate voltage in the gate terminal, the N^+ region extends into the channel and an electron inversion layer is generated, forming an abrupt P^+-N^+ junction. From the point of view of the energy band diagram (Figure 2.4a), increasing the gate voltage pulls down the energy of the channel and progressively a sharper band bending at the junction is achieved, lowering the tunneling length. In the **on-state** ($E_{V,p} > E_{C,chan}$), interband tunneling can take place and electrons flow from the valence band of the P^+ into the conduction band of the inversion layer. However, in order to have a net flux of tunnel current it is necessary to apply a reverse voltage to the drain terminal (in an N-TFET a positive voltage at the cathode). This enhances the built-in potential in the space charge region of the P^+-N^+ junction, thereby increasing the tunneling probability.

The applied drain voltage generates an electric field that makes the electrons drift into the drain terminal.

In P-mode operation the operation scheme is similar, but in this case when a negative gate voltage is applied to the gate terminal, the P^+ region expands underneath the gate, generating a hole inversion layer. When $E_{V,chan} > E_{C,n}$ interband tunneling can take place and electrons flow from the valence band of the inversion layer into the conduction band of the N^+ region (Figure 2.4b). In summary:

- N-TFET configuration: $V_{S,P} = 0$, $V_G > 0$, $V_{D,N} > 0$.
- P-TFET configuration: $V_{S,N} = 0$, $V_G < 0$, $V_{D,P} < 0$.

The tunneling current of a TFET can be described by the Landauer equation [8]:

$$I_D = \frac{2q}{h} W \int_{Ev^{ch}}^{Ec^S} T(E)[f_s(E) - f_d(E)]dE \qquad \textbf{(2.1)}$$

where $T(E)$ is the electron tunneling probability and $f_{s,d}\ (E)$ are the source and drain Fermi distributions functions. In order to increase the drain current it is necessary for the transmission probability of an electron tunneling through the barrier to be as close to 1 as possible. In addition there needs to be a difference in the Fermi functions between source and drain so that current can flow. The band bending at the source/channel junction can be approximated by a triangular barrier [3]. Using the WKB (Wentzel-Kramers-Brillouin) approximation [3], the tunneling probability is given by:

$$T_{WKB} \approx exp\left(-\lambda \frac{4\sqrt{2m^*}E_g^{3/2}}{3q\hbar\left(E_g + \Delta\Phi\right)}\right) \qquad \textbf{(2.2)}$$

In equation (2.2), λ is the tunneling length [9] and represents the extension of the transition region at the source/channel junction (the smaller λ, the greater the band bending in the tunneling region), E_g is the energy bandgap of the source and $\Delta\Phi$ is the tunneling window where the BTBT is allowed.

One of the most important features of TFETs is the theoretical capability of achieving a subthreshold swing below 60 mV per decade of current. The lower the SS, the steeper the slope of the device making it possible to scale the threshold voltage while keeping the off-current very low. In contrast, for MOSFETs the minimum SS is limited to 60 mV/dec because of the thermionic emission of the carriers from source to drain which contains a kT/q term. The subthreshold swing for a TFET $SS = \ln 10 \left(\frac{\partial I_D}{\partial V_G}\frac{1}{I_D}\right)^{-1}$ is calculated from [10] using [8]:

$$\frac{\partial I_D}{\partial V_G} = \frac{2q^2}{h}\left(\frac{\partial T_{WKB}}{\partial E_v^{ch}} F\left(E_V^{ch}\right) + T_{WKB}\frac{\partial F\left(E_V^{ch}\right)}{\partial E_V^{ch}}\right) \qquad \textbf{(2.3)}$$

The terms of equation (2.3) are not limited by kT/q and there are two contributions in the SS. If the tunneling probability changes quickly with gate voltage, the first term prevails and the subthreshold swing is given by [8]:

$$SS \approx \ln 10 \frac{3\hbar\left(E_g + \Delta\Phi\right)^2}{\lambda 4\sqrt{2m^*}E_g^{3/2}} \qquad \textbf{(2.4)}$$

Equation (2.4) establishes that in order to obtain a low SS, it is required to reduce the tunneling window ($\Delta\Phi$) and to increase the tunneling length (λ). $\Delta\Phi$ is directly linked with the gate voltage and according to equation (2.2), if $\Delta\Phi$ is increased there will be an enhancement of the tunneling probability. However, there will be a fast degeneration of SS, because of the quadratic term in equation (2.4). The same goes for λ, increasing it will reduce SS but it will also decrease T_{WKB}. Besides, a large value for λ means that there is a weak modulation of the energy bands at the source/channel junction (provided by the gate terminal), and it will be necessary to apply a higher V_{GS} to achieve a sharper band bending. It is thus to take into account this trade-off to understand TFETs physics. One needs to reduce λ as much as possible because this will be translated into a better control of the tunnel junction from the gate and a lower gate voltage (also a lower $\Delta\Phi$) and as consequence the subthreshold swing decreases.

The second term in equation (2.3) is dominant when the tunneling probability T_{WKB} is close to unity. In that case the subthreshold swing is given by [8]:

$$SS \sim \frac{\ln 10}{q}\Delta\Phi \qquad (2.5)$$

Decreasing the tunneling window ($\Delta\Phi$) in equation (2.5) as much as possible, SS can be reduced below 60 mV/dec. This is explained from a qualitative point of view in Figure 2.5. The tunneling window acts as a band-pass filter [6] and only the carriers between the minimum of the conduction band in the source and the maximum of the valence band in the channel can contribute to the drain current. Electrons in the Fermi tail of the distribution, which are more energetic cannot tunnel because, they are aligned with the bandgap of the channel. Only the cool carriers of the Fermi function participate effectively in the tunneling and transport process, making feasible to obtain SS below 60 mV/dec.

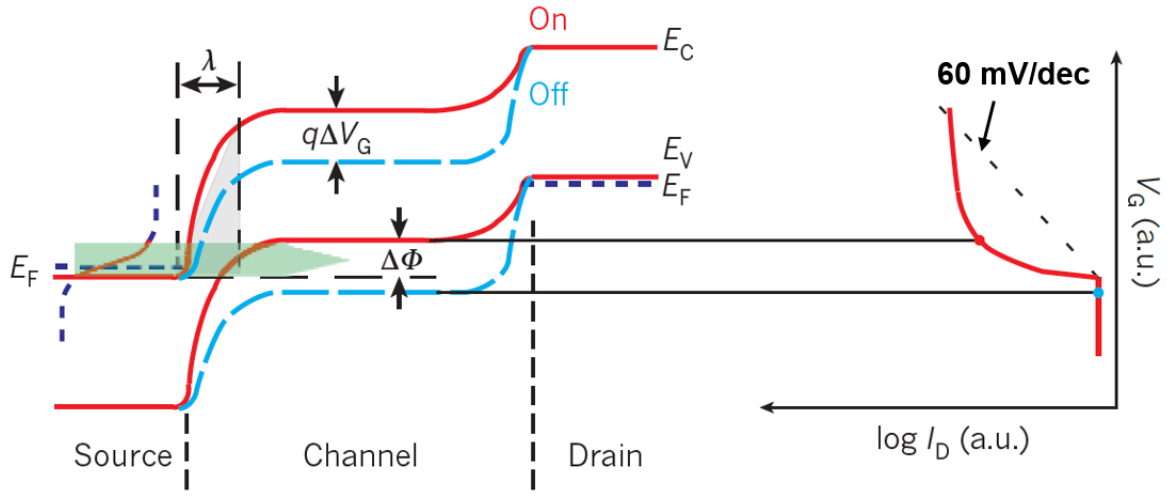

Figure 2.5. Energy bands diagram of a P-TFET showing the off- and on-state configuration. The tunneling window ($\Delta\Phi$) is related to the applied gate voltage and delimits the filtering function efficiency to achieve SS below 60 mV/dec. TFET I_D-V_G curve with a non-linear slope, showing that SS depends on the applied gate voltage [6].

2.2.1. Simulation TFETs vs. Experimental TFETs

New requirements to decrease energy consumption are based on reducing supply voltage and keeping the off-current low. This is consequence of the industrial needs for low power consumption in handheld devices, where the span life of the batteries is a major concern. The scaling of V_{DD} in CMOS technology is limited by the thermal limit of subthreshold slope in MOSFETs, which degrades the performance at low V_{DD}. Since the early 2000's, the Tunnel FET has been the most promising of the studied steep-slope devices because of it predicted outstanding characteristics for ultra-low power applications (V_{DD} < 0.4 V).

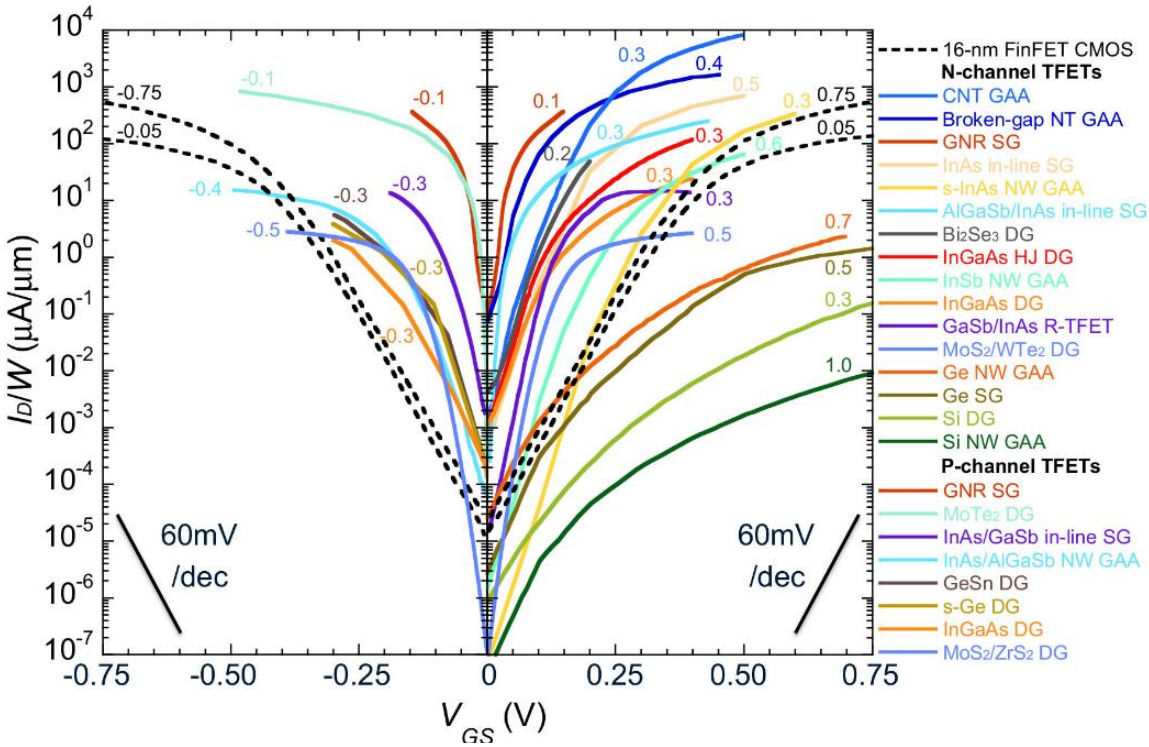

Figure 2.6. $I_D(V_G)$ comparison for simulated P- & N-TFETs. Black dashed lined indicate experimental 16 nm FinFET CMOS technology. Numbers on top of the curves indicate the drain voltage [11].

Figure 2.6 shows the simulated $I_D(V_G)$ curves for P- and N-TFETs published since 2010 [11], compared with a 16 nm low-power FinFET CMOS [12]. Silicon TFETs present the lowest on-currents [13], [14] and a subthreshold above 60 mV/dec. This is due to the wide and indirect bandgap of silicon (E_G = 1.12 eV) that decreases the tunneling probability. Next, TFETs fabricated with Germanium [15] have a higher on-current because the bandgap of the resulting compound material (including Ge) is lower with respect to silicon. But, the drive current is still lower compared to FinFET CMOS. It is also important to notice that increasing the number of gates using Double-Gate (DG) [16] or Gate-All-Around (GAA) architectures, a better electrostatic control is accomplished, resulting in a steeper subthreshold slope. Only TFETs simulated with III-V materials [17]–[19] with a small and direct bandgap, surpass the performance of the FinFET (Figure 2.6). Another important characteristic of group III-V is the flexibility in structure engineering, because changing the alloy composition makes it possible to obtain different types of heterojunctions such as AlGaSb/InAs and InAs/GaSb [11] where the starting point at the tunneling junction is characterized by a small tunneling length λ that enhances the on-current with a lower gate voltage.

P-TFETs simulations exhibit a higher performance for graphene nanoribbons (GRN) [20] and 2D materials such as $MoTe_2$ [21] because of high electrostatic gate control expected in single atomic layer materials. In N-TFETs, the on-current is maximized for Carbon nanotube (CNT) GAA [22] and broken-gap nanotube GAA [23].

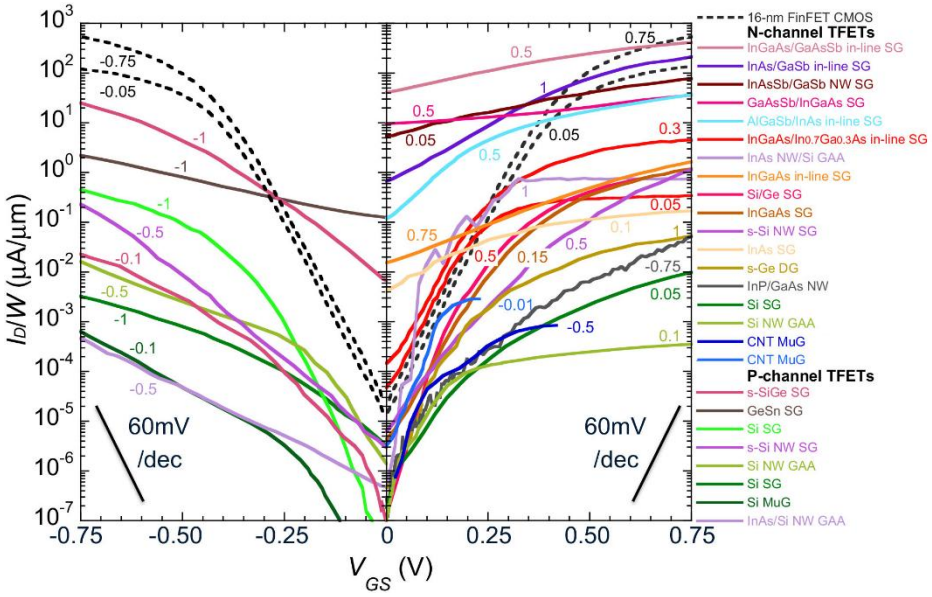

Figure 2.7. $I_D(V_G)$ comparison for fabricated P- & N-TFETs. Black dashed lined indicate experimental 16 nm FinFET CMOS technology [11].

The transfer characteristics for experimental TFETs are gathered in Figure 2.7. On one hand silicon TFETs show the lowest on-currents [24], [25] of all studied materials which is consistent with prospects. On the other hand, the subthreshold slopes are steeper [24], [26] than for III-V group, in contrast with simulations. Progress in BTBT materials and process fabrication based on strain engineering in silicon (sSi) [27], SiGe heterojunctions [28], strained Germanium (sGe) [29], GeSn [30] and strained SiGe (sSiGe) have demonstrated to enhance the tunnel current. TFETs based in heterojunctions of III-V materials exhibit the highest on-currents (Figure 2.7), but the subthreshold slopes are completely degraded [11]. At the present time, carbon nanotubes have not shown the high drain current predicted by simulations. Despite the fact that several models have been proposed for Graphene Nanoribbon (GNR) Tunnel FETs [31]–[33], the fabrication has not been accomplished until very recently [34]. 2D material TFETs have been already fabricated, but the maturity of the technology is still limited and the performance exhibited by these TFETs is low.

Comparing the simulated (Figure 2.6) and fabricated TFETs (Figure 2.7) it is clear that there is a gap between optimistic simulations and disappointing measurements. Simulations predicted simultaneously a high on-current and a steep slope. However, measurements show that when the subthreshold slope is either relatively steep (less than 60 mV/dec) the drive current is low. On the contrary, when the drive current is high the subthreshold slope is completely degraded. This indicates that there is a significantly divergence in the subthreshold characteristics of the simulated TFETs and suggests that second order effects were not taken into account in simulations. These non-ideal effects are responsible of SS degeneration at low gate voltage, such as band tails due to phonons and heavy-doping, trap-assisted tunneling, interface roughness and density of interface states at the high-k dielectric/semiconductor interface [11].

One added difficulty to Tunnel FETs in TCAD simulations is the necessity to include a BTBT model to solve the tunneling transport in the source/channel junction. Previous models were not very accurate [35], [36], because they do not restrict the tunneling phenomena only to the tunneling window, but in the whole band bending region. This issue was fixed with the Non-Local Path BTBT model [37], but still there are some challenges. TCAD calculates the BTBT generation based on two parameters and if they are used as fitting parameters without a physical meaning results cannot be trusted. Simulations based on homojunction silicon or homojunction SiGe TFETs provides results consistent with measurements [38]. However, if we want to simulate heterojunctions TFETs it is necessary to know the effective masses of the carriers for the different materials, because this will also change the tunneling probability and by extension the BTBT generation.

2.2.2. Trap Assisted Tunneling (TAT)

In TFETs there are three dominant transport mechanisms: BTBT, TAT and Shockley-Read-Hall (SRH) recombination. The tunneling current is given by the sum of these three components, albeit the last two components are parasitic effects that need to be minimized in order avoid the degradation of the TFET characteristics. SRH is a recombination/generation process that occurs when an electron from the conduction band "falls" into a trap (defect) present at some location of the energy bandgap. Eventually this electron will "fall" into an empty state of the valence band. SRH has a strong dependence on temperature [39], but only a weak dependence on the electric field generated by the gate terminal. TAT is also a SRH mechanism with a strong dependence with the electric field, but with the particularity that involves tunneling via a trap state in the bandgap [39]. TAT occurs because of bulk traps, traps at semiconductor/semiconductor interface in the case of heterojunctions and traps at the oxide interface [40]. All these traps are located inside the bandgap of the tunneling junction. This means that one trap can split the tunneling length (λ) in two regions, such that it requires less energy for tunneling from the valence band into the conduction band through the trap than when only pure interband tunneling is considered (direct tunneling). Unfortunately, only the BTBT mechanism enables the possibility to obtain SS below 60 mV/dec, because TAT results in a thermally activated tunneling process [41].

Among all the non-idealities that contribute to degrade the SS in TFETs, a great number of recent published results verify that TAT is the main responsible for the degradation of the subthreshold slope [42]–[45]. Moselund *et al.*, have reported that the nature of traps is conditioned by the geometry and dimensions of the device [46]. In that paper reporting the operation of an InAs/GaSb N-TFETs, the SS is controlled by the density of interface defects from the non-optimized gate stack, while for InAs/Si P-TFETs a large lattice mismatch was reported to be responsible for the generation of a great number of traps densities at the heterojunction.

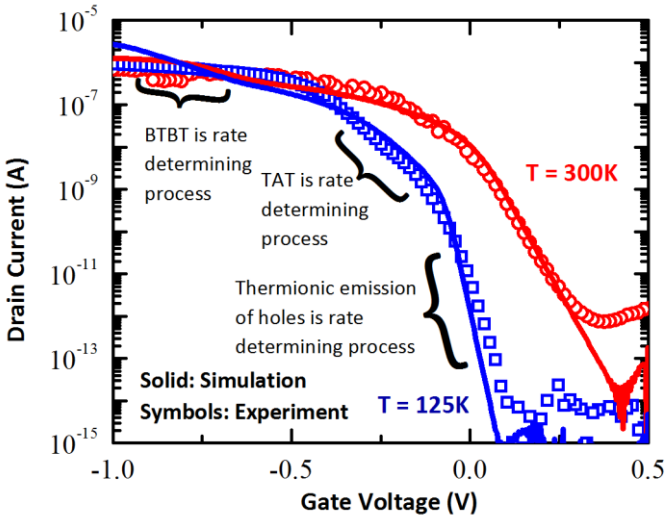

Figure 2.8. $I_D(V_G)$ curves of InAs/Si P-TFET for simulations and measurements at different temperatures [46].

Figure 2.8 shows that distinct conduction mechanisms prevail at different gate voltages. BTBT is the main mechanism responsible for the drain current at high gate voltages (beyond -0.7 V), and it is possible to conclude that the dependence of the BTBT on temperature is low. Similar current values are obtained for the two studied temperatures (125K and 300K). At medium gate voltages, TAT is the main contribution, as a consequence of the high density of traps at the heterojunction. Carriers are trapped in defects inside the tunnel region; this degrades the subthreshold slope. In this voltage region, TAT is clearly the dominant conduction mechanism because is more sensitive to temperature. As a consequence, at T = 125K defects are deactivated and the slope is steeper. This suggest, that for a fully optimized TFET architecture, all the mechanisms involving TAT (interface density of states, heterojunctions, doping and materials defects) will be the limiting factor for achieving a steep slope in the subthreshold region [46]. Depending on the TFET architecture and the material used, the nature of traps will change and the solutions to reduce TAT will be also different.

As for semiconductor traps (bulk traps), the location of defects plays an important role with respect to the degradation of the subthreshold slope and simulations studies have demonstrated the impact of shallow and deep traps [47]. The $I_D(V_G)$ characteristics of a simulated TFET without traps (Figure 2.9c) show a negligible leakage current, (I_{OFF} ~ 10^{-17} A/µm). If there is a deep trap close to the source region (Figure 2.9a), a recombination of a trapped electron with a hole from the valence band is quite likely, because the hole density nearby the source is higher. This explains the increase of the current in the subthreshold region and the degradation of the slope in Figure 2.9c. Nonetheless, for a shallow trap that is close to the conduction band of the channel (Figure 2.9b), the probability that a trapped electron recombines with a hole from the valence band is reduced, because the hole density is low, so the leakage current is very similar (I_{OFF} ~ 10^{-16} A/µm) to the ideal case with no traps. These results indicating that the degradation of the subthreshold slope and increase of leakage current are due to the deep-level traps [47], are consistent with the transfer characteristics of TFETs based on III-V materials (Figure 2.7). The maturity of the process fabrication for III-V materials is not as well-controlled as it is for silicon technology and this increases the concentration of semiconductor traps.

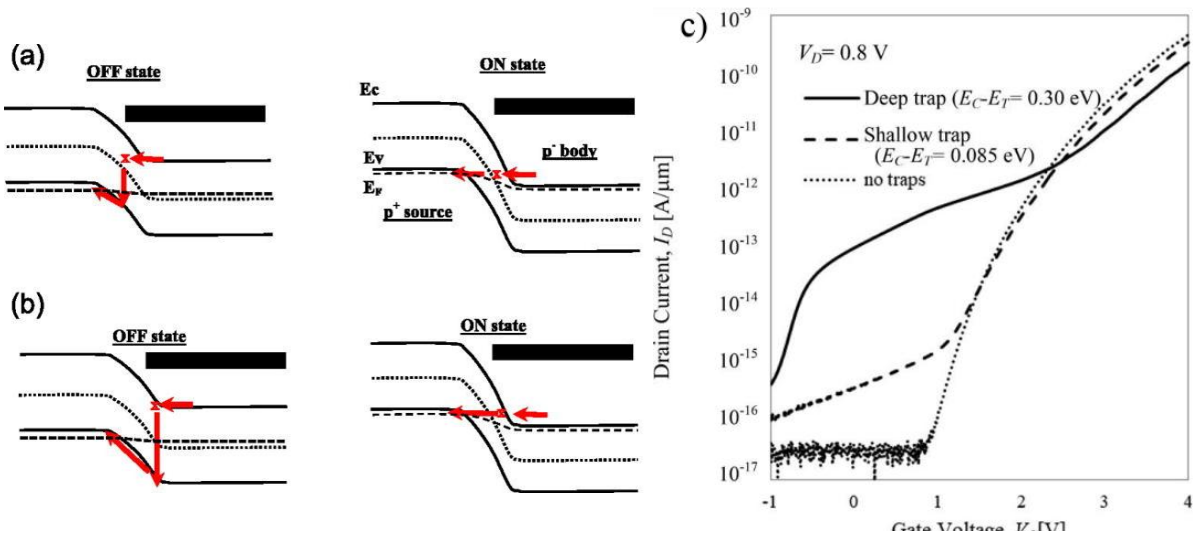

Figure 2.9. (a) Schematic of a deep trap; (b) Schematic of a shallow trap; (c) $I_D(V_G)$ curves of simulated TFET for no traps and TAT for shallow trap (dash line) and deep trap (solid line) at 400 K [47].

2.3. TFET device engineering

2.3.1. Silicon homojunction TFET

The tunneling rate T_{WKB} (equation (2.2)) is the key factor to enhance the drive current. It has been shown that fabricated silicon TFETs (section 2.2.1) have a limited performance due to the fact that wide bandgap and indirect tunneling degrade T_{WKB}. But, simulations of TFETs structures using silicon are accurate and reliable enough to study different problematics [48] like superlinear regime in output characteristics, impact of tunneling at the drain junction, etc. In Figure 2.10 is represented the schematic of a planar homojunction TFET, simulated with Sentaurus TCAD tool to study the impact of different boosters on the performance. Geometry parameters have been chosen to match our fabricated TFETs: gate length L_G = 500 nm, silicon body thickness T_{Si} = 11 nm, T_{BOX} = 145 nm, intrinsic body length L_{IN} = 0 nm, gate work function Φ_{gate} = 4.61 eV, EOT = 1.18 nm and a dopant concentration in source and drain of $N_D = N_A = 10^{20}$ cm^{-3}. The intrinsic region (L_{IN}) separates the drain from the gate. This allows to minimize the effect of the gate terminal in the drain/channel region, which is responsible of TFET ambipolarity in off-state (detailed in section 2.3.2.3).

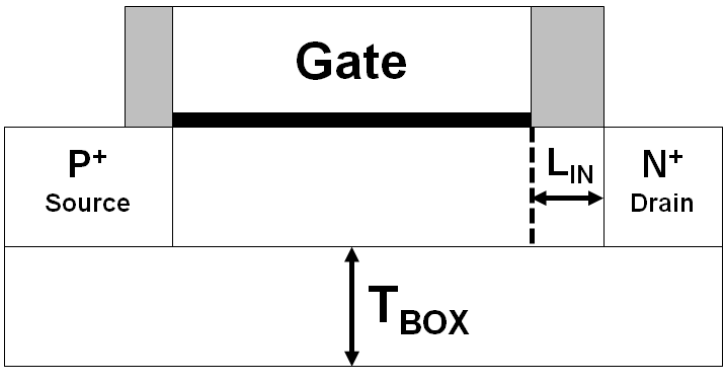

Figure 2.10. Schematic of a silicon N-TFET simulated with Sentaurus TCAD tool to determine the impact of different boosters on the current.

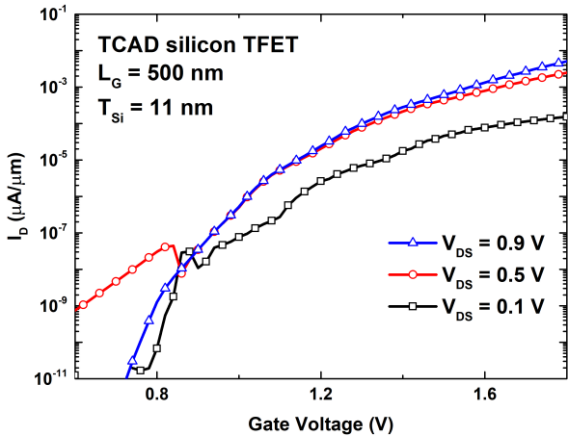

Figure 2.11. $I_D(V_G)$ curves of TCAD simulation of silicon N-TFET at different drain voltages. Low on-current at V_{GS} = 1.8 V.

The $I_D(V_G)$ curves of TCAD simulations for a silicon N-TFET (Figure 2.11) show that for the best case (V_{DS} = 0.9 V), the on-current at a given gate voltage of V_{GS} = 1.8 V is 5 nA/μm. For lower drain voltages the tunneling current is even more degraded. Once the gate voltage is large enough to sustain an inversion layer, the drain voltage triggers the tunneling mechanism and electrons are attracted to the drain terminal generating a net flux of current. Figure 2.11 also shows that the tunneling current increases with drain voltage, but this effect eventually saturates (as seen for V_{DS} = 0.5 V and 0.9 V). In TFETs there is a competition between the vertical electric field generated by the V_{GS} and the parallel electric field created by the V_{DS}. If one keeps increasing the drain voltage, depletion of the inversion layer occurs near the drain junction where electrons are attracted [49]. As a result, the tunneling begins to occur at the channel/drain junction and not in the source/channel region, and to create the inversion layer near the source it will be necessary to apply a higher gate voltage, which is clearly not suitable for low-power applications.

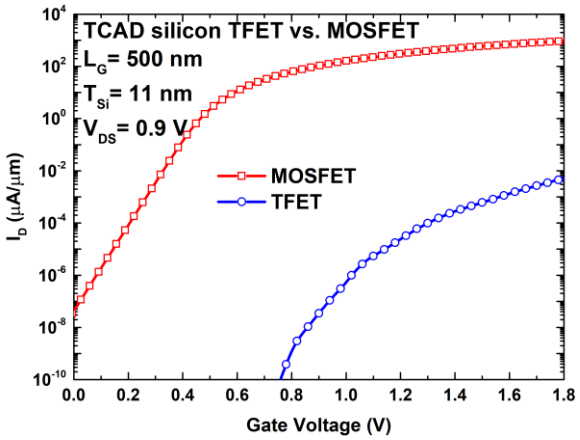

Figure 2.12. $I_D(V_G)$ curves of TCAD silicon TFET and MOSFET for long channel (500 nm). MOSFET outperforms TFET.

The comparison of an unoptimized silicon homojunction MOSFET with a long channel (L_G = 500 nm) with a TFET (Figure 2.12) shows a much lower on-current (~ 5 nA/μm) in the TFET, than in the CMOS device (~ 1 mA/μm), a degraded subthreshold slope and a higher threshold voltage. TFETs only surpass MOSFETs in achieving a low off-current. Figure 2.12 clearly establishes that boosters are necessary in TFETs in order to increase the performance (higher on-current, steep subthreshold slope and reduced threshold voltage).

2.3.1.1 Complementary TFET in CMOS Foundry

During last decade many innovations have been reported reflecting attempts made at improving Tunnel FET performance, but even today there are not many publications of Complementary TFETs (C-TFETs) in the literature [50]. Such devices are critical to the adoption of TFET technology for high production. Manufacturing of N- and P-TFETs monolithically integrated with standard MOSFETs based on 0.13 µm silicon CMOS technology was reported in 2015 [51]. In addition, the fabrication of a planar silicon C-TFET inverter was also demonstrated.

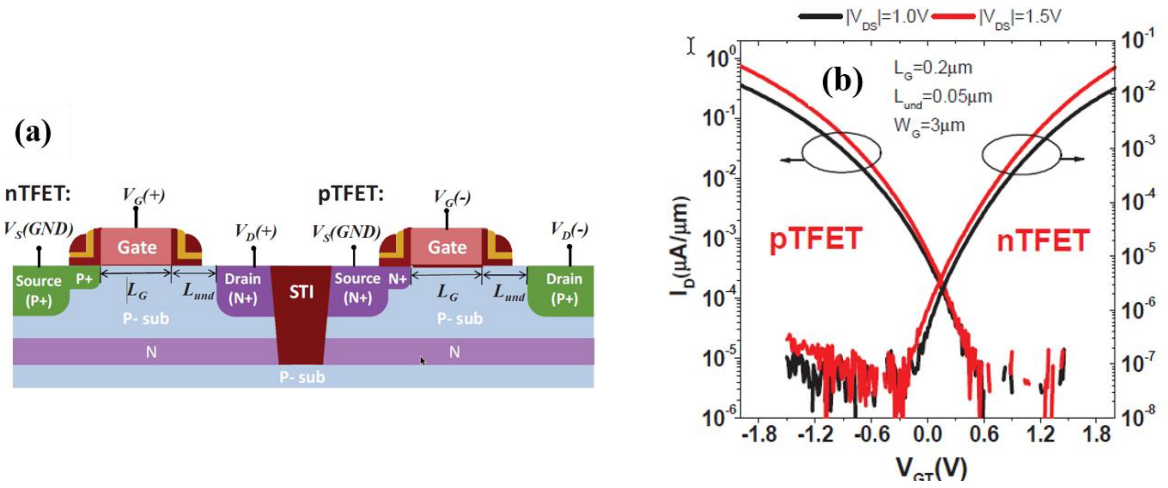

Figure 2.13. (a) Schematic of Complementary TFET. (b) $I_D(V_G)$ transfer characteristics of N- and P-TFET at different drain voltages (V_{DS} = 1.0 V and V_{DS} = 1.5 V) [51].

TFETs fabricated in high-resistivity bulk silicon substrate (Figure 2.13a) using ion implantation to form the source junctions, have been optimized to get abrupt and shallow tunnel junctions and thus enhance the drive current. The implementation of an underlapped region (L_{und}) between gate and drain minimizes the off-current. The transfer characteristics are shown in Figure 2.13b, where one can see a better performance for P-TFETs than for N-TFETs. This could be explained by the formation of more abrupt tunnel junction due to the lower diffusion rate of As than BF_2 [51].

Despite of all the efforts made to optimized the process fabrication (different dopant concentrations, temperature annealing, oxide thickness and gate work function) the P-TFET biased at V_{DS} = -1.0 V and V_{GS} = - 2.0 V shows a limited on-current of 0.33 µA/µm. The off-current is slightly degraded ($1.5 \cdot 10^{-5}$ µA/µm) but this could be explained by the fact that a bulk substrate was used rather than an SOI substrate, which would more efficiently suppress parasitic effects due to dielectric isolation of source, channel and drain by the BOX. A rough estimation indicates an average SS of ~ 300 mV/dec, which is very poor. The variability is also an important concern, because the limited BTBT generation area results in a large device-to-device variation. This explains why the main cause of variability, due to its direct effect in the tunneling area, is the source doping gradient (SDG) [51]. The measured parameters of this "optimized" silicon C-TFET are consistent with the simulation results and highlight the need of boosters to increase the performance of TFETs.

2.3.2. TFET optimization

Tunnel FETs design rules differ from those used in CMOS technology, because interband tunneling requires the enhancement and better control of the electric field generated at the source/channel junction. According to Kane's formula the BTBT generation is given by [52]:

$$G_{BTBT} \propto exp\left(-\frac{E_G^{3/2}}{E_{max}}\right) \qquad \textbf{(2.6)}$$

An increase of BTBT generation rate at the source can be achieved by decreasing bandgap and/or increasing the electric field. Equation (2.6) is directly linked to the tunneling probability T_{WKB}, indicating that higher on-currents need a $T_{WKB} \sim 1$, which means a small bandgap (E_G), small effective carrier mass (m^*) and small tunneling length (λ). E_G and m^* are material dependent, so using in the process fabrication semiconductor materials like strained silicon (sSi), SiGe, strained SiGe (sSiGe), GeSn, III-V materials or Ge/III-V, will improve the on-current. Achieving a small λ depends on additional factors such a Multiple-gate device geometry (MuGFETs), an abrupt doping profile at the source with a high doping, a reduced oxide thickness, a high-k gate dielectric and a small body thickness. The advantage is that the majority of these boosters are already used in CMOS technology and can thus be easily implemented in a TFET fabrication process. In theory the solution seems evident, but the implementation of all these optimizations in body thicknesses lower than 10 nm is complex and because of the immaturity of lower bandgap materials, this will introduce a great number of defects and interface states, which will be responsible of the subthreshold slope degradation.

It is possible to classify the tunneling boosters (related to BTBT injection) as:

- **Gate Stack engineering:** For steep switching and high ON current with strong gate electrostatic control.
  - Thin EOT and gate-edge structure.
  - Low interface density of traps.

- **Source junction engineering:** For steep switching and high ON current with narrow tunnel barrier.
  - Steep doping profile and optimized activation of impurity concentration.
  - Defect-less junction control of gate overlap length.
  - Alignment of junction and hetero interface.

- **Drain junction engineering:** Minimize OFF current in the drain region.
  - Underlapped intrinsic region between the gate and the drain (L_{IN}).
  - Low GIDL current.
  - Optimized impurity profile and material with higher bandgap.

- **Channel engineering:** To increase tunneling probability $T_{WKB.}$
  - Narrow bandgap materials (sSi, SiGe, sSiGe).
  - III-V materials (Staggered of broken gap III-V materials).
  - Thin body or nanowire structures.
  - Multigate architectures.

To test some of these boosters it has been performed a TCAD study based on a reference Tunnel FET architecture (Figure 2.10) with the same default values used in section 2.3.1. The objective is to characterize the impact on the performance of each booster at a time, while the others remain unchanged.

2.3.2.1 Impact of body thickness

TCAD simulations focused on the variation of the body thickness have been performed from thick (T_{Si} = 50 nm) to thin Si films (T_{Si} = 4 nm). As long as the thickness is reduced (Figure 2.14) the drain current is enhanced and a steeper subthreshold slope is achieved. This is due to the fact that the electric field generated at the source junction exerts a more efficient control on the band bending and the interband tunneling increases. For gate voltages higher than 1.6 V the on-current seems to converge and for values above 2.0 V (not shown in Figure 2.14), the drain current for a T_{Si} = 6 nm or 7 nm is higher than for T_{Si} = 4 nm. This issue has been observed in other simulations studies in the past [53] and suggests that a very thin body thickness (T_{Si} < 6 nm) could lead to drain current reduction because of minimizing the cross-sectional area available for the current flow. This is a key aspect because it has been established that for Tunnel FETs a steep subthreshold slope (SS < 60 mV per decade) is only possible for a scaled body thickness around 5 nm, even without taking into account any TAT generated by defects [39]. The positive aspect is that CMOS technology uses for the 28FDSOI node a silicon thickness of T_{Si} = 7 nm [54] and for the 14FDSOI node a T_{Si} = 6 nm [55]. So, they are optimized and the transference to Tunnel FET technology is straightforward.

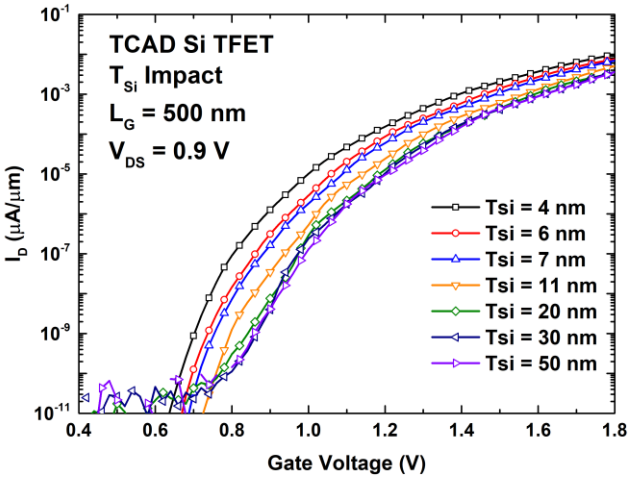

Figure 2.14. $I_D(V_G)$ curves of TCAD silicon TFET to characterize the impact of the body thickness (T_{Si}).

2.3.2.2 Impact of gate length

It is well known that in MOSFETs the drain current is limited by carrier transport and is inversely proportional to the gate length. On the contrary, in TFETs the BTBT generation mechanism occurs in the source/channel junction, which implies that the tunneling current is independent on gate length. This being true, aggressive reduction of the dimensions in TFETs could affect the electrostatic control of the device [56]. This was assessed through an analysis of TFET characteristics for values of gate length ranging from L_G = 500 nm to L_G = 15 nm.

Simulation results in Figure 2.15 show that for values of gate length from 500 nm down to 50 nm there is no impact of gate length reduction on subthreshold slope and drain current. For L_G = 30 nm a degradation of the slope appears. At L_G = 15 nm and 10 nm a huge degradation of the off-current is observed. This indicates that for short lengths the gate terminal loses the electrostatic control of the interband tunneling at the source/channel junction. The most consistent explanation is that if source and drain are too close, the electric field generated by the drain side perturbs the control of the BTBT when gate voltage is below 1 V (Figure 2.15). Besides, the drain voltage can bend the energy bands of the channel region close the drain, allowing tunneling from the channel to the drain which generates the increase of the current in the subthreshold region.

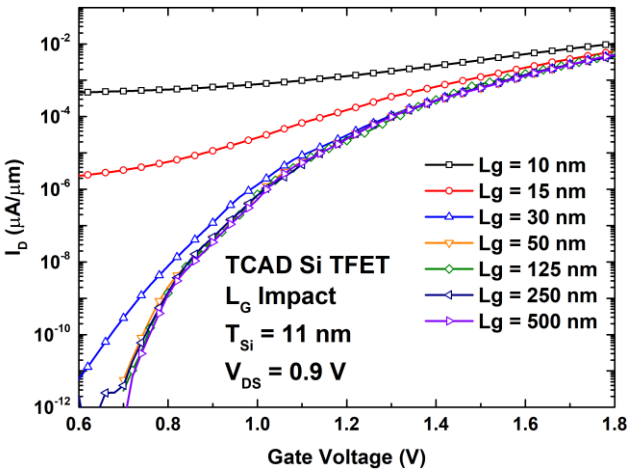

Figure 2.15. $I_D(V_G)$ transfer characteristic of TCAD silicon TFET to characterize the impact of the gate length.

2.3.2.3 Impact of intrinsic region: Ambipolarity

Ambipolar current flow is an undesired effect that happens in Tunnel FETs because of the similarity of an n-TFET (p-i-n) and a p-TFET (n-i-p) structure. Ambipolar currents occur when the device is conducting for high positive and negative supply bias, while keeping unchanged the drain bias. In a N-TFET configuration, when $V_G > 0$ and $V_D > 0$ BTBT takes place in the source/channel region, but when $V_G < 0$, BTBT occurs now in the channel/drain region. This can generate an undesirable behavior in TFET inverter-based logic and two possible solutions have been proposed to reduce the ambipolar current [57]. The first method relies in the use of an underlapped region (L_{IN}) between the gate and the drain, so that the influence of the gate electric field in the drain is significantly minimized and the BTBT at the drain is eliminated. The major problem with this method is that this intrinsic region increases the dimensions of the devices. A wrapped-around approach has been proposed to solve this problem [58]. The second method is based in the reduction of the drain doping concentration. Published results have demonstrated that with a low drain doping is possible to reduce the ambipolarity and off-current. However, there are also some challenges involved: it is not possible to decrease indefinitely the drain doping concentration because it should be high enough to facilitate contact formation. A lower doping concentration implies a higher series resistance and a decrease of the on-current.

We have chosen to study the reduction of the ambipolar current with the study of the impact of the horizontal underlapped region shown in Figure 2.10.

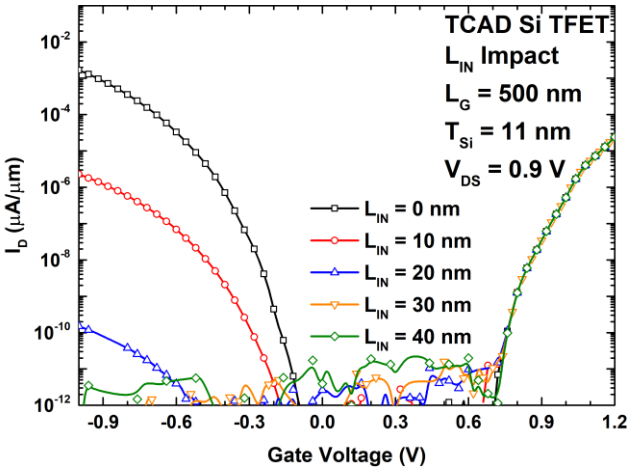

Figure 2.16. $I_D(V_G)$ transfer characteristics of TCAD silicon TFETs showing the impact of the underlapped region to reduce ambipolarity.

Results in Figure 2.16 show that when the TFET is symmetric (no intrinsic region close to the drain) the ambipolar current for negative gate bias is high. As long as the underlapped region is increased the ambipolarity is reduced and for L_{IN} = 30 nm the leakage current is negligible. For a technological node below 28 nm, an intrinsic region of 30 nm is not realistic, so there is necessary trade-off between the maximum intrinsic region and the maximum ambipolar current allowed. It has been established that for a L_G = 13 nm, Tunnel FETs require an intrinsic region of 10 nm [58].

2.3.2.4 Impact of Equivalent Oxide Thickness (EOT)

The reduction of the EOT (Figure 2.17) shows an interesting trend in the simulations, namely a simultaneous enhancement of both on-current and subthreshold slope. The explanation is that the electrostatic control is optimized (better gate coupling) for thinner EOT. A thicker EOT of 2 nm presents a degraded slope and drain current. A common value for EOT at CEA process fabrication when using Hafnium dioxide (HfO_2) is 1.18 nm [59].

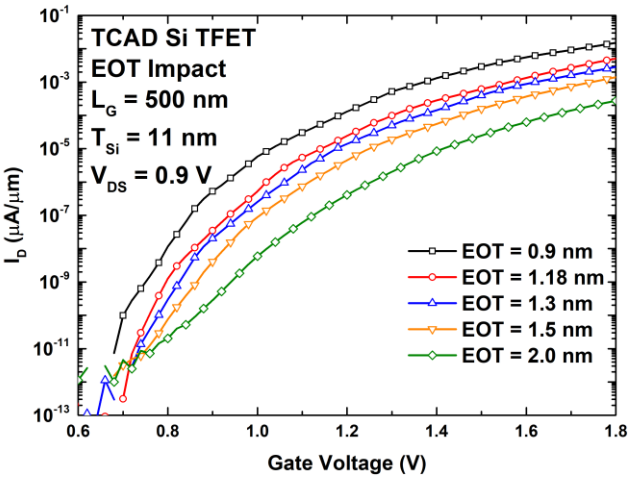

Figure 2.17. $I_D(V_G)$ transfer characteristics of TCAD silicon TFETs to characterize the impact of the EOT thickness.

Figure 2.17 verifies that the real boost occurs for EOT lower than 1 nm. Currently is possible to achieve EOT of 0.9 nm [60], but TFETs need a very good quality at the interface of the body material and the oxide to minimize the defects and not degrade the subthreshold slope. New materials like zirconium dioxide (ZrO_2) and titanium dioxide (TiO_2) with higher dielectric permittivity would allow eventually achieve EOT lower than 0.9 nm and closer to 0.5 nm. As CMOS technology also needs the lowest EOT possible, all the optimization efforts from CMOS achieved can be transferred to Tunnel FETs devices.

2.3.2.5 Si TFETs vs. SiGe TFETs

Using silicon is not the best choice for Tunnel FETs because of the wide bandgap. This means that the modulation of the tunneling barrier thickness requires a high gate voltage. It is necessary to use different materials and heterojunctions in the source/channel region to increase tunneling probability and SiGe appears as a good candidate.

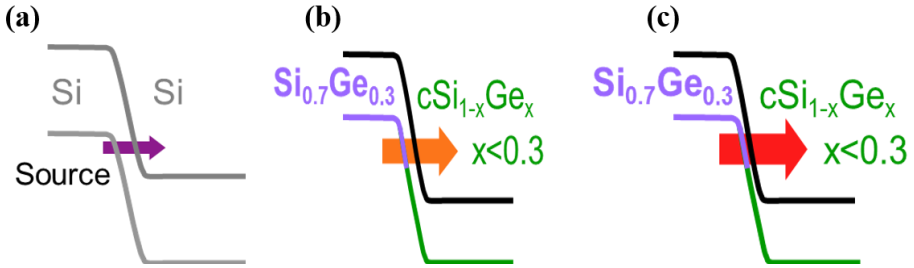

Figure 2.18. Schematic of energy bands at source/channel junction for (a) silicon, (b) SiGe to reduce the bandgap and (c) source junction abruptness [61].

The objective is to achieve a lower bandgap and an abrupt junction to improve the tunnel injection. Figure 2.18 qualitatively shows that using a $Si_{0.7}Ge_{0.3}$ raised source and drain and a compressively strained $Si_{1-x}Ge_x$ channel is possible to increase the band bending (more states will be available for tunneling) and minimize the tunneling length. In fact, with some modifications of the process fabrication (implant doping, temperature anneal…) it is possible to obtain an extra junction abruptness with sharper band edges, increasing the tunneling probability. Strained SiGe is a common booster on CMOS, so it can be adopted in a straightforward manner to TFETs.

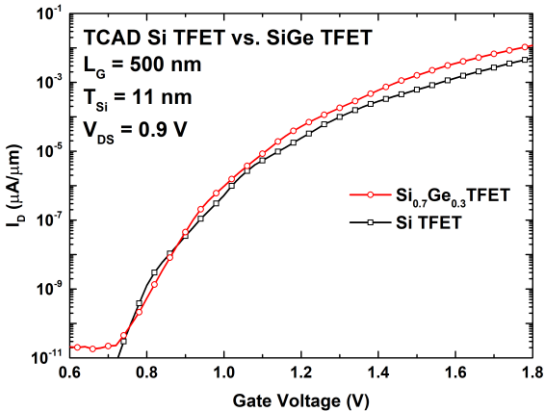

Figure 2.19. $I_D(V_G)$ curves for Si TFET (black squares) and SiGe TFET (red circles).

Figure 2.19 shows that a TFET with $Si_{0.7}Ge_{0.3}$ homojunctions provides a better drain current and a slightly steeper subthreshold slope. Increasing the percentage of Germanium

would allow a higher drain current because of the smaller bandgap, but in real TFETs the fabrication process with percentages higher than 30% generates a great concentration of defects and the consequence will be the degradation of the slope due to TAT.

2.3.3. TFET optimization challenges

To fabricate devices for ultra-low power applications several requirements are necessary. In first place, a very low off-current is needed; this has been already achieved in TFETs owing to FDSOI architecture. Secondly, a low SS (below 60 mV/dec) is sought after. Unfortunately is almost impossible to find in the literature a fabricated TFET with a reduced SS covering an extend range of subthreshold currents. Finally, a high I_{ON}/I_{OFF} ratio is needed. TFETs with a decent I_{ON}/I_{OFF} ratio have been published (~10^4-10^5), but these ratios are obtained thanks to an extremely low off-current and not because of a high drain current. The main challenge is the difficulty to get a steeper slope and high on-current regardless of materials, architectures and specific fabrication steps.

The boosters which are more likely to be adopted to increase the performance are:

- **Junction optimization:** Abrupt tunneling junction with a sharp band profile will allow a wide tunneling window and a small tunneling length, so more states will be available for interband tunneling.
- **Heterojunctions:** New compound materials in the source/channel junction to decrease the bandgap where tunneling takes place. Best candidates are SiGe or GeSn. III-V materials offer a great number of possibilities because of a small mass and direct bandgap, but integration on silicon platforms is not straightforward.
- **Gate dielectric permittivity:** High-k materials with EOT lower than 1 nm will increase the electrostatic coupling, enhancing both drain current and steeper slope.
- **Body thickness:** Aggressively scaled body below 6 nm is mandatory to achieve a steep subthreshold slope.
- **Ultrathin geometry:** Trigate/nanowire, FinFET or GAA architectures will increase the electrostatic control of the device.
- **Drain-Gate underlap:** The proximity of the drain to the gate compromises the accurate control of the BTBT by the gate voltage. Besides, the ambipolar current will increase. Using an intrinsic region near the drain will minimize this effect. However, new geometries or configurations are necessary to avoid increasing the surface too much.

The requirements to achieve a steep slope pass through an aggressively thin body. However, this implies that for the gate stack formation, implantation processes and the technological immaturity of new compound materials, the concentration of semiconductor traps and oxide traps will increase with respect to silicon. If TAT is not minimized, the off-current will be degraded and the SS could never be lower than 60 mV/dec. Therefore, a low density of traps in the tunnel junction is a key asset in increasing the tunneling probability. All the prospects show that TFET requirements are more stringent in comparison with MOSFETs.

2.4. CEA TFETs: State of the art

2.4.1. $Si_{1-x}Ge_xOI$ and GeOI TFETs

First generation of TFETs was fabricated on SOI, $Si_{1-x}Ge_xOI$ and GeOI substrates with a FDSOI CMOS process flow in order to study the impact of different semiconductor materials on the BTBT injection [62]. Figure 2.20a shows the cross-section of an SOI TFET where a high-k metal gate stack composed of HfO_2 (3 nm), TiN (10 nm) and polysilicon. In order to optimize the junctions and enhance the on-current, a second set of spacers was implemented and LDD extensions. $I_D(V_{GS})$ results for the P-TFET configuration show a point SS of 42 mV/dec, but for low values of drain voltage and at low drain current range (~10^{-13}-10^{-12} A/µm). The average SS, however, is approximately 120 mV/dec (well above the limit of 60 mV/dec). Also, very low off-currents of ~10-100 fA/µm are measured. With respect to the junction optimization the experimental results reported in [62] show that for a N-TFET configuration the extension of the P-type region enhances the on-current, while for a P-TFET it is the extension of the N-type region that enables the increase of the on-current. This is consistent with the fact that for an N-TFET (P-TFET) the BTBT takes place in the P-type (N-type) region.

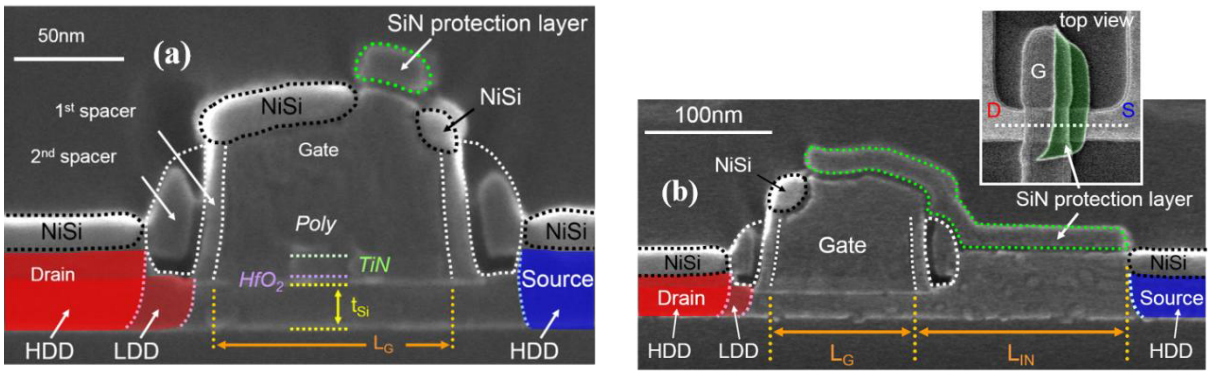

Figure 2.20. (a) SEM cross-sections of an SOI TFET showing the gate stack configuration and junction optimization (spacers and extension). (b) SEM cross-section of a Drift TFET (DTFET) with an intrinsic region to reduce ambipolar current [62].

To reduce the ambipolar current a novel architecture based on the extension of the intrinsic area (L_{IN}) was proposed (Figure 2.20b). Results show that there is a reduction of the parasitic current of 2 decades. Furthermore the impact in the on-current is limited as long as the resistance of the intrinsic region is minimized. However, this horizontal increase of the dimension goes against general scaling trends, but it can be minimized using an L-shape intrinsic region [58].

For the SOI and $Si_{1-x}Ge_xOI$ devices (with x = 15% and 30%) the body thickness is 20 nm; it is 60 nm for GeOI devices. Figure 2.21 verifies that SiGe enhances the on-current with respect to the SOI TFET. When the Ge percentage is increased, the bandgap becomes smaller and the BTBT higher. The highest on-current is obtained in Ge TFETs. For a P-TFET configuration in an SOI wafer the on-current is 1.48 nA/µm, while in a GeOI wafer the on-current is 4 µA/µm. This implies a gain factor in the performance of 2700×.

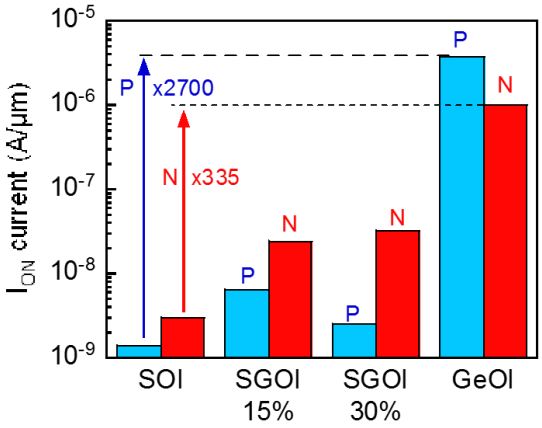

Figure 2.21. I_{ON} (at V_{DS} = 0.8 V and V_{GS} = 2 V) for SOI, SGOI 15%, SGOI 30% and GeOI for L_G = 400 nm. Increase of the on-current using narrow bandgap materials [62].

2.4.2. Strained TFETs with ultra-thin body

The second generation of TFETs was fabricated by co-integration with CMOS FETs in a FDSOI CMOS technology using Extremely Thin SOI (ETSOI) material, a high-k metal gate, ultra-thin compressively strained $Si_{1-x}Ge_x$ body thickness and $Si_{0.7}Ge_{0.3}$ raised source and drain [61]. The objective is to increase the BTBT injection thanks to the use of narrow channels and small EOT, strain, as well as low bandgap material in the source and low-temperature anneal of junctions.

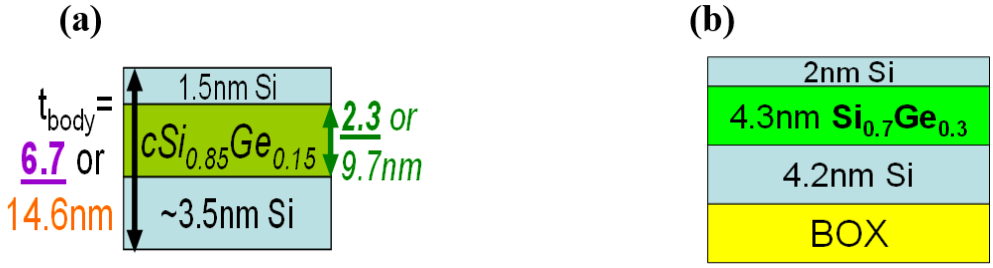

Figure 2.22. Schematics of ultra-thin body thickness (a) to study the impact of body thickness reduction and (b) to characterize the impact of the annealing temperature [61].

The results of TFETs with different body thicknesses (Figure 2.22a) establish that for a body of 14.6 nm the I_{ON} is ~ 1µA/µm (V_{GS} = - 2.5 V, V_{DS} = - 1 V) and I_{OFF} ~ 10^{-6} µA/µm. When the body thickness is reduced to 6.7 nm the I_{ON} is enhanced up to ~ 90 µA/µm and I_{OFF} is degraded to ~ $4 \cdot 10^{-4}$ µA/µm. Also the SS is improved from 190 mV/dec to 130 mV/dec. This confirms that BTBT can be increased using a smaller body thickness due to improved electrostatic control of the BTBT junction by the gate.

Using the body configuration of Figure 2.22b and a 950°C spike anneal (versus 1050°C) for junction formation, one notices an increase of the I_{ON} current from 0.3 µA/µm to 428 µA/µm (at V_{GS} = - 2.5 V, V_{DS} = - 1V). This increase is, however, accompanied by a degradation of the I_{OFF} current from 10^{-6} µA/µm (1050°C) to $3 \cdot 10^{-5}$ µA/µm (950 °C). Furthermore, the SS is improved from 230 mV/dec to 150 mV/dec. This remarkable performance in P-TFET configuration is attributed to a better positioning of the gate with respect of the N^+/channel junction (more favorable position of the gate edge) and the sharper abruptness of the junction [61].

Enhancement of the on-current achieved by either reducing body thickness and/or decreasing anneal temperature are impressive, but unfortunately the SS is still far above of the 60 mV/dec limit. A more recent electrostatic analysis and TEM images revealed that the high drain current was the result of a silicide contamination in the active area (more particularly in the N^+ region) that generated a Schottky contact [63]. Therefore, devices were not real TFETs (p-i-n structures) but hybrid P-i-Metal structures. The main issue is than in a Schottky barrier FET (SBFET) it is possible to have "high" drain currents, but the tunneling takes places from conduction band to conduction band and not by interband tunneling. P.M. Solomon [64] has demonstrated the inability of SBFET to achieve a SS below 60 mV/dec. As a side remark, we cannot say that the impact of narrow body thickness and low temperature anneal will have the same effects in SBFETs and in TFETs.

2.4.3. Nanowire TFETs

The most recent TFET architecture evolution relies on the use strained SiGe nanowires with a Ω-gate configuration to improve electrostatic control [65]. In addition all the features implemented in previous generations, such as the use of a high-k metal gate, SiGe raised source and drain are also included in nanowire TFET processing [61], [62]. Nanowires were fabricated with a body thickness of 11-12 nm and a total width perimeter of 37 nm and 27-29 nm respectively.

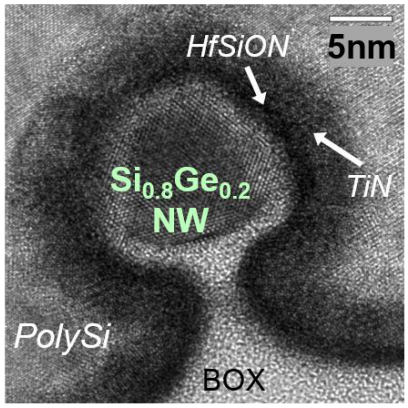

Figure 2.23. Cross-section HRTEM of a SiGe nanowire Tunnel FET fabricated at CEA [65].

So far, the main limitation of TFETs is the inability to achieve high on-currents and a steep subthreshold slope. High-quality crystalline SiGe in the junctions and a Ω-gate configuration are expected to solve this problem. A TFET nanowire with a 100 nm gate length and a 5 nm width (perimeter width of 27 nm) with a $Si_{0.75}Ge_{0.25}$ channel in P-TFET configuration, was reported to provide an I_{ON} of 760 µA/µm and an off-current of 20 pA/µm with a SS of 80 mV/dec over two decades. Nevertheless, an extra electrostatic analysis and TEM images showed an excessive Ni diffusion in the N^+ region, creating a Schottky contact in the N^+ region [61]. Therefore, these nanowires were not real TFETs, but again hybrid P-i-Metal structures. Further analysis of the devices revealed that the possible causes for uncontrolled silicide formation are aggressive device width scaling in conjunction with i) possible epitaxial raised source and drain non-uniformity; ii) high-dose As implant damage; iii) partial or total consumption of the SiGe in raised source and drain during the post implant stripping and iv) low temperature activation anneal. A combination of these factors is most likely responsible for Ni excess diffusion [63].

Despite of these silicidation issues, trigate/nanowire architecture based on SiGe material seems the right evolution path for increasing the performance on TFETs due to enhancement of the electrostatic field control. Since the process fabrication is CMOS compatible, all the boosters applied to MOSFETs can be transferred to Tunnel FETs.

2.5. Ultimate innovative Tunnel TFETs

Other research centers and universities are currently investigating TFETs with different architecture approaches, materials and specific process fabrications in order to obtain a high on-current (hundreds of µA/µm) and steep slope (SS < 60 mV/dec) over a several decades. This section compiles the most promising and interesting studies.

2.5.1. Strained Si and SiGe GAA nanowire TFET

Gate-all-around geometry allows one to reduce the tunneling length λ due to a better electrostatic control. But, a steeper doping profile in source and drain is also essential to minimize λ. The Dopant Segregation (DS) technique [66] makes it possible to achieve abrupt tunneling junctions (minimize the defect density) with implantation into silicide (IIS) for silicon nanowires fabricated in 20 nm SOI substrates (Figure 2.24). Besides, epitaxial silicide contacts (nickel aluminum silicide) reduce contact resistivity and line edge roughness.

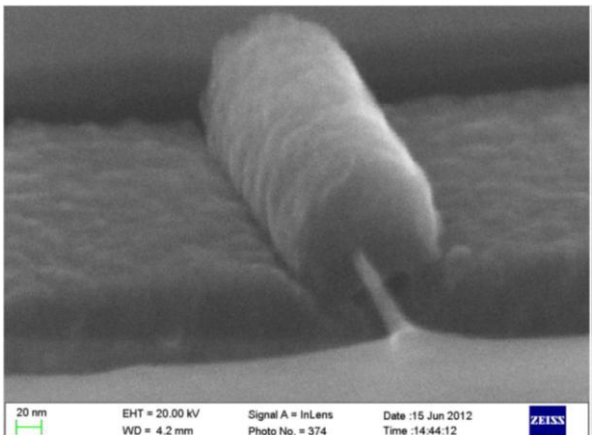

Figure 2.24. SEM of a Si GAA nanowire TFET with 8 nm diameter and high-k metal gate [66].

In 2015 new improvements were reported, such as the formation of uniaxial strain in nanowires to reduce the bandgap and improve BTBT [67]. Direct ion implantation with subsequent spike anneal degrades sharp doping profiles (via extended dopant diffusion) and introduces a great number of defects. On the contrary, DS technique with low energy implantation into the silicide and thin Ni source and drain contacts with a low temperature annealing enables the formation of steep profiles. The scaling of the nanowire diameter also provides a significantly increase of the performance: for a 10 nm GAA TFET the on-current is 64 µA/µm at $V_{DS} = V_{GS}$-V_{off} = - 1.0 V and SS ~ 70-80 mV/dec for two decades [67]. Compound materials like SiGe with lower bandgap also increase the on-current, however the higher the percentage of Germanium the more defects are created in the semiconductor, increasing the off-current. Minimizing this density of defects is very important, because with a Germanium content higher than 80% it becomes possible to have direct-valley tunneling resulting in higher BTBT current. Finally, SiGe/Si heterojunctions nanowire architectures can

optimize the performance in the on-state since a SiGe junction with a small bandgap can be formed at the source, while in the off-state the higher bandgap of the silicon at the drain junction reduces the off-current.

Recently the impact in the performance of the ion implantation and dopant activation has been studied in sSi GAA nanowire TFETs [68]. For an N-TFET, an implantation in the normal direction (0°) and a low temperature activation (500°C) provide an I_{ON} = 15 µA/µm at V_{DD} = 0.5 V and a SS of 76 mV/dec over 4 decades of drain current.

2.5.2. Junction TFET and T-Gate Schottky barrier TFET (TSB-TFET)

The Junction-modulated TFET (JTFET) offers the possibility to achieve a sharper band bending at the tunnel junction using a striped gate instead of changing the type of material at the source [69]. Extending the gate into the source enables a junction depleted-modulation in the overlapped region, which means a higher tunneling area compared to a symmetric TFET architecture (Figure 2.25a). The transfer characteristics show a better on-current and steeper SS over 3 decades of drain current for the JTFET ($5 \cdot 10^{-8}$ A/µm & 85 mV/decade) than for the TFET ($8 \cdot 10^{-9}$ A/µm & 145 mV/decade). From these results it is clear that using silicon as material is the main limitation to enhancing the on-current. An architecture evolution called Pocket-Junction modulation TFET (PJTFET) uses an implantation of a doped pocket (N-type) before the source dopant implantation (P^+) [69]. This provides a sharper band bending in the source/channel junction generating a more efficient tunneling. However, the PJTFET performance is still far away from that of MOSFETs.

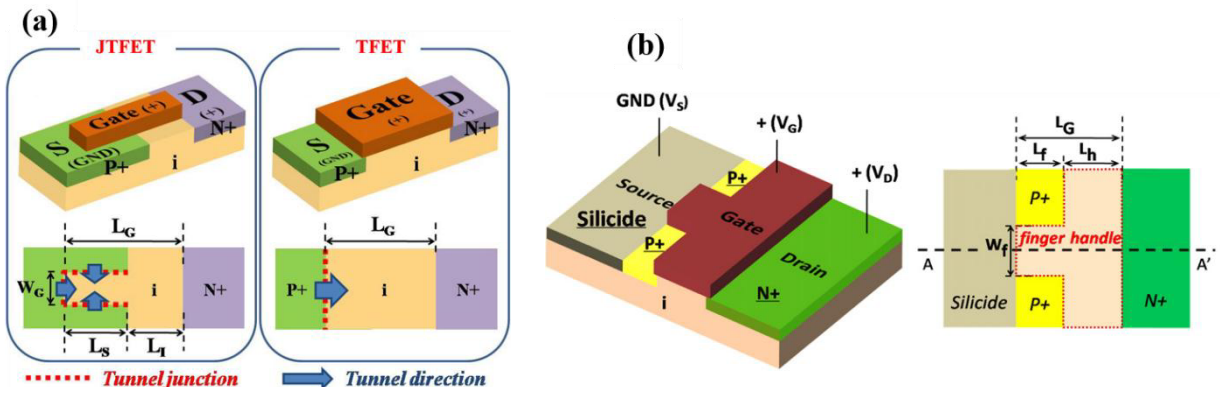

Figure 2.25. (a) Schematic structures and top view of a JTFET and a symmetric TFET [69]. (b) Schematic representation of a TSB-TFET and top view with the geometry description [70].

In an attempt to solve the problem of the low on-current a T-gate Schottky barrier Tunnel FET (TSB-TFET) was proposed [70]. This device comprises a T-shaped gate (Figure 2.25b) with a silicide source Schottky junction and two additional tunneling junctions (P^+-type) next to the source. With this architecture the on-current is enhanced due to the Schottky current, but the off-current is degraded because the Schottky barrier height is low in off-state, which enables thermal emission of electrons from the drain to the source. Besides, it has been proved by Solomon [64] the impossibility to achieve SS below 60 mV/dec using a SB-junction. It is claimed that it is possible to minimize the leakage current by shrinking the gate finger width (W_f), because the two P^+ regions (Figure 2.25b) can fully deplete the adjacent surface, thereby increasing the energy barrier, and thus minimizing the thermal emission leakage. However, the reduction is limited to less than half a decade of drain current.

Experimental results show for a TSB-TFET with a 5 µm finger length (L_f) and 3 µm finger width (W_f) at V_{DS} = 0.6 V an improvement of the on-current and SS ($4 \cdot 10^{-7}$ A/µm & 75 mV/dec), when compared with the TFET ($2 \cdot 10^{-8}$ A/µm & 86 mV/decade).The off-current of the TSB-TFET, however is an order of magnitude than in the corresponding TFET.

Recently, an improved architecture fabricated in SOI with multiple fingers and an additional dopant-segregated Schottky source junctions (MFSB-TFET) was proposed to increase the on-current [71]. The transfer characteristic shows an I_{ON} = 10 µA/µm at V_{DS} = 0.6 V and V_{GS} = 1.0 V.

2.5.3. Parallel electric field TFET

One of the challenges facing standard TFET architectures is that BTBT generation area is confined to a small region at the top of the source/channel junction, limiting the amount of tunneling current. In addition, the electric field generated by the gate is perpendicular to the flux of carriers and only modulates the band bending at the gate edge. An innovative solution is extending the source doping into the channel region [72] to achieve vertical BTBT and increase the on-current since in this configuration the tunneling direction is parallel to the gate electric field. As added benefit, the electrostatic control of the gate over band bending is increased, which improves the SS.

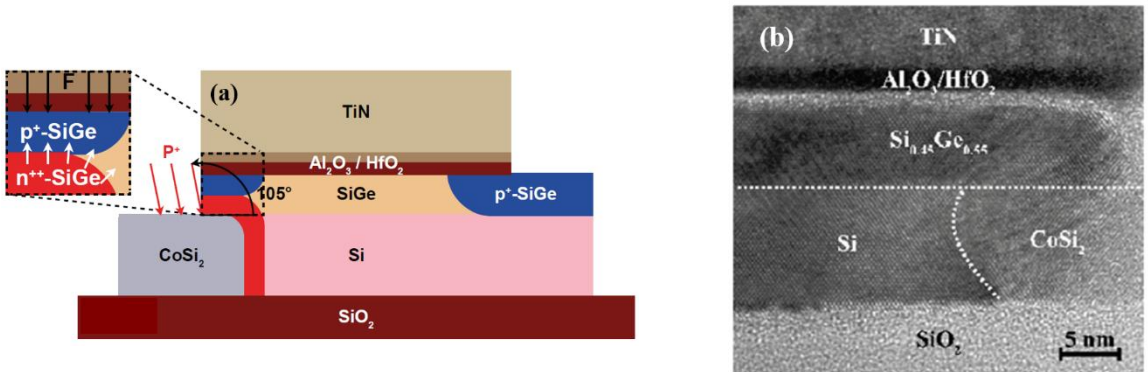

Figure 2.26 (a) Schematic of a SiGe/Si line TFET with tilted implantation of B^+ and P^+ at the source region and self-adjusted silicidation with $CoSi_2$ (magnified view of vertical BTBT in p^+-n^{++} junction). (b) TEM image showing the $CoSi_2$ layer [73].

A SiGe/Si line-TFET was fabricated by the Jülich laboratory [73] (Figure 2.26a) with specific fabrication steps based on a selective and self-adjusted silicidation (Figure 2.26b) and using a counter doped pocket at the source junction (achieved by the implantation into the silicide method). Doping activation is achieved at low temperature to form a N^{++}-P junction with a sharp doping profile and a high doping level concentration. These devices show an on-current of 6.7 µA/µm at a supply voltage of - 0.5 V and a SS = 80 mV/dec over 4 decades of drain current. The advantages of this fabrication process are the strong suppression of the ambipolar switching and a significant increase of performance. The complexity and number of additional steps to fabricate the counter doped pocket with the silicidation are high, however.

Other research centers have also investigated novel TFET architectures and determined that reducing the channel thickness below 10 nm and using a wrapped gate electrode configuration are key aspects to achieve an increase of the on-current and steep SS [74], [75].

However, vertical BTBT is dependent of the gate length for an aggressively scaled pitch; a short gate length implies a small vertical tunneling current (due to a small BTBT area). Therefore, it is necessary to find new solutions like heavily doped source extensions to compensate the reduction of current drive due to the gate length scaling.

2.5.4. III-V based TFETs

During the last 10 years, the number of TFETs based on heterojunction fabricated using compounds materials of III-V families has increased dramatically [46], [76]–[82]. Unlike silicon, III-V materials are direct-gap semiconductors with low bandgap and small effective masses. As we know from T_{WKB} equation, all these characteristics increase the tunneling probability, but the most important BTBT enhancing factor is the introduction of new bandgap engineering opportunities. Changing alloy composition is possible to fabricate staggered and broken bandgap junctions (Figure 2.27). Using this, it is only necessary to apply a small gate voltage to generate interband tunneling, which is perfect for ultra-low power applications.

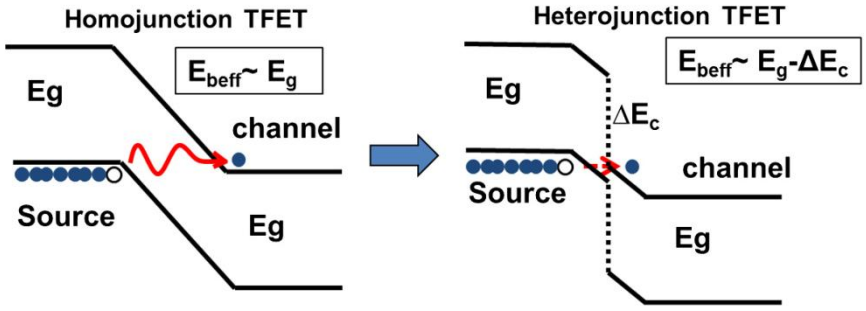

Figure 2.27. Schematics of a homojunction TFET with a wide tunneling barrier and a heterojunction TFET with band structure engineering [81].

However the use of these materials has several drawbacks, because the process fabrication is not straightforward to transfer to a silicon platform. Also high-k interface with III-V semiconductors presents a high interface state density and defects that are responsible for trap-assisted tunneling (TAT) and the degradation of the subthreshold slope.

A III-V heterojunction TFET was developed by Intel with 3D-Trigate architecture using a lower source/channel tunnel barrier height to achieve a steep slope [76]. The EOT scaling and a higher source doping allows for on-current enhancement. A III-V nanowire TFET made on a silicon substrate and using a surrounding-gate architecture was reported by Hokkaido University [83]. It consists in a vertical III-V nanowire channel, with a high-k dielectric and an EOT lower than 1 nm. The challenges in the fabrication process are related to the reduction of the NW diameter. It shows a really steep subthreshold slope but apparently it is a one-shot work. One of the major drawbacks is the co-integration of vertical structures with standard (silicon) CMOS technology. A complementary III-V structure Tunnel FET has been developed by IBM and the idea is the co-planar integration of III-V TFETs on silicon substrate with a new technique called Template-Assisted Selective Epitaxy (TASE) [46]. Despite all the efforts, the CMOS-like integration is far from straightforward because TAT degrades the TFET behavior at low gate voltages. A vertical InAs/GaAsSb/GaSb TFET has been developed by Lund University [84], providing an I_{ON} = 10 µA/µm for I_{OFF} = 1 nA/µm at

V_{DS} = 0.3 V. One most recent investigation is based in III-V/Ge compound materials, developed by Tokyo University [85]. The architecture is planar with InGaAs and Ge/strained SOI TFETs. The defect-less p^+-n source junction formation with steep impurity profiles is a key for high performance.

2.5.5. Junctionless TFET

The requirements to increase the drain current in TFETs highly relies in the ability to fabricate ultra-high doped and abrupt tunnel junctions. But as seen in [51] the source doping gradient is the main responsible of the threshold voltage variability in fabricated TFETs. This problematic is also present in CMOS technology because at each time the dimensions of transistors are scaled, the fabrication of ultra-sharp doping junctions is more difficult. Recently demonstrated is a nanowire transistor without junctions and no doping concentration gradient called the junctionless transistor [86]. The doping is identical in source, channel and drain and the depletion of carriers in the channel region is achieved electrostatically. The work functions of the gate materials are chosen to help with device turn-off characteristics. The use of thin body thickness (below 10 nm) and trigate or GAA structures are mandatory to develop junctionless devices.

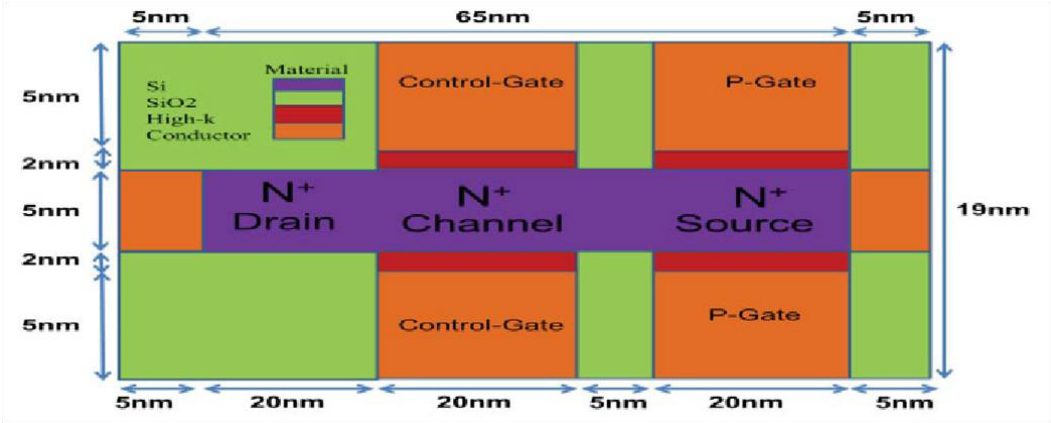

Figure 2.28. Schematic of a simulated Junctionless TFET (JLTFET) with N-type doping in source, channel and drain regions. Two sets of gates are implemented to electrostatically generate the p-i-n structure of a TFET [87].

To implement a junctionless TFET it is necessary to fabricate two sets of gates to form a p-i-n structure (as shown in Figure 2.28), one for the channel region to deplete carriers and other in the drain region to generate electrons or holes. There are a considerable number of simulation studies with similar architectures that claim the possibility to achieve a high on-current and SS below 60 mV/dec [88]–[92]. The problem is that the fabrication process of two gates in very short devices and with different gate work functions is non-trivial and so far there are no published results of experimental junctionless TFETs based on these types of architectures with such enhanced performance.

A different approach architecture called Source Junctionless TFET (SJL-TFET) has been simulated [93] and experimentally demonstrated by Toshiba [94]. This device has been fabricated in SOI using a silicon CMOS platform. First a boron ion implantation is done in the whole active area and there is no source junction, because the source and the channel are uniformly doped. But, there is a junction formation with the drain diffusion in order to use

only a gate terminal in the channel region. When the gate voltage is increased the inversion layer is formed under the gate and there is BTBT generation in the whole channel region (vertical BTBT). Results show a small I_{ON} of $2.1 \cdot 10^{-4}$ µA/µm and I_{OFF} ~ 0.01 pA/µm (V_{GS} = 1.0 V and V_{DS} = 0.2 V) and a lower SS in the range from 10^{-14}-10^{-12} A/µm compared to a regular p-i-n structure most likely due to the no junction formation architecture.

2.5.6. 2D materials TFETs

The thinning of 3D materials to obtain body thicknesses below 10 nm presents some challenges in relation with film roughness as consequence of fabrication variability [95], TAT effects at the oxide and heterojunction interfaces due to lattice mismatch [96] and conventional substitutional doping methods [97] (dopant diffusion and ion implantation). All together these effects prevent the formation of a sharp band bending in the tunneling junction. 2D layered materials have emerged as one of the most promising alternative for channel materials, because of a better device electrostatic control with a lower natural length scale. Besides, it is easy to obtain a thin atomic layer of a few angstroms per layer due to the van der Waals bonding (weak bonding) between planes. These materials are also easier to pattern due to their planar structure than 1D structures such as nanowires and nanotubes [98]. In addition, accurate control of the bandgap is possible as it depends on the number of layers. Also the possibility to obtain pristine and dangling-bond free interfaces and a weak electron-phonon interaction is important to achieve a steep subthreshold slope.

There is a great number of identified 2D materials [99], but for MOSFETs and TFETs the Transition Metal Dichalcogenides (TMD) materials are the most interesting due to a wide selection of bandgaps and band alignments. Of course, there are also challenges with 2D TFETs fabrication: it is still necessary to form highly doped sources and drains, albeit ion implantation cannot be used because it damages the thin crystalline structure of 2D materials. Therefore, new doping methods are being explored, such as surface charge transfer [100], [101], field-effect doping and covalent functionalization [102]. Even using these techniques, traps states are still present within the bandgap, degrading the TFET performance. However, it has been proven that with chemical treatment it is possible to passivate the active defects and achieve a sharp band edge.

Das *et al.* [103] experimentally demonstrated Schottky barrier tunneling of holes in back-gated MoS_2 FETs and Roy *et al.* [96] reported the first gate-controlled BTBT in a TMD heterostructure. The BTBT occurs between the 2D layered semiconductor MoS_2 (N-type) and WSe_2 (P-type) which can be easily stacked together and coupled by van der Waals forces, forming a staggered gap heterojunction. The top and bottom gate electrodes are used independently to control the electrostatic potential and modify the band offset at the MoS_2/ WSe_2 interface. In both cases the use of electrostatic doping requires a back gate terminal to control the devices.

Sarkar *et al.* [98] have successfully fabricated an atomically thin and layered semiconducting TFET (ATLAS-TFET). This device is a vertical Tunnel FET implemented with Germanium in the source region and a 2D TDM material (MoS_2) bilayer of 1.3 nm in the channel (Figure 2.29a). This heterojunction configuration formed thanks to the van der Waals bonds, allows the formation of a staggered heterojunction as shown Figure 2.29b with strain-free interfaces. The aggressively scaled body thickness enhances the electrostatic control by

the gate and the use of MoS_2 minimizes the tunneling length, which increases BTBT. Moreover, as the Germanium doping is extended into the channel region, the interband tunneling is not limited to the source/channel junction, but occurs in the whole area (vertical BTBT) and the current is increased with respect to the standard TFET. In the off-state (Figure 2.29c) the conduction band of the MoS_2 is above the valence band of the Ge, so there are not available empty states to tunnel through. Only electrons in the conduction band of Ge (in a small concentration because is P-type) can tunnel, which provides a very low off-current. In on-state (Figure 2.29d), the conduction band of the MoS_2 is lower than the valence band of the Ge, thus there are available states to tunnel into. The maturity of TMD materials is limited and the fabrication of high-k dielectric is still under research, so for this device the gate dielectric is a solid polymer electrolyte [98].

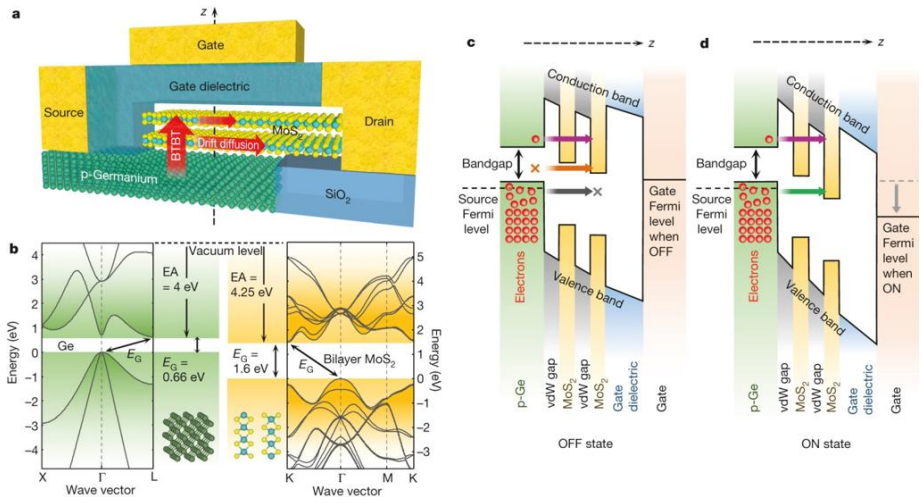

Figure 2.29. (a) Schematic of the ATLAS-TFET; (b) E-k diagrams of germanium and 2D layered MoS_2 showing the formation of a staggered vertical heterojunction. Energy band diagrams for off-state (interband tunneling is not allowed) and on-state [98].

The transfer characteristics of this device in Figure 2.30a for three different drain voltages (0.1 V, 0.5 V and 1.0 V) shows a normalized on-current (at V_{GS} = 0.5V and device width of 15 µm) of 0.066 µA/µm, 0.46 µA/µm and 1.0 µA/µm respectively. The SS ranges between 36.5 mV/dec and 31 mV/dec over 4 decades of drive current (from 10^{-13} A to 10^{-9} A). In Figure 2.30b the 2D TFET is compared with a conventional MOSFET fabricated using the same MoS_2 material [98]. The SS of the conventional MOSFET is always above 60 mV/dec, while the ATLAS-TFET shows a minimum SS of 31.1 mV/dec.

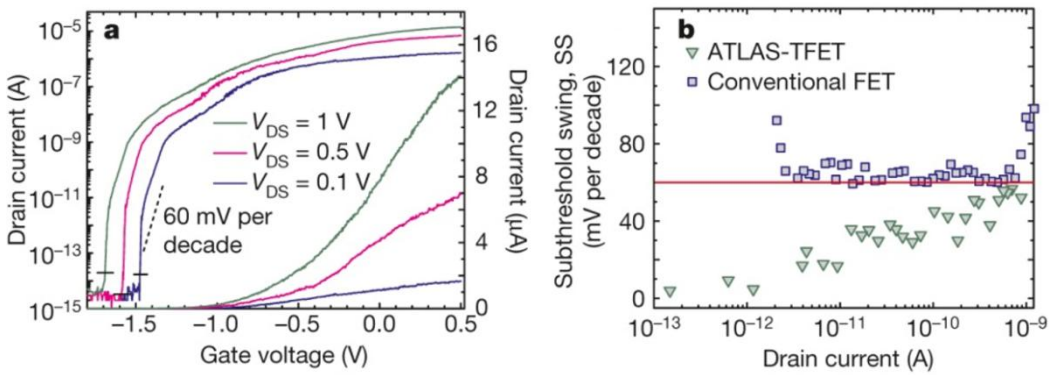

Figure 2.30. (a) Transfer characteristics of ATLAS-TFET for different V_{DS} (0.1 V, 0.5 V & 1.0 V). Steeper SS below 60 mV/dec over 4 decades of current; (b) SS(I_D) for the ATLAS-TFET and a CFET at V_{DS} = 0.5 V [98].

Finally, Roy et al. [104] have fabricated the first TFET based on two different layered semiconductors using $WSe_2/SnSe_2$ heterostructures. The P-TFET shows an I_{ON}/I_{OFF} ~ 104 and a SS ~ 100 mV/dec over 2 decades of current. The device performance is degraded, but an improvement of the contacts and heterojunction interface quality can provide better results.

2.6. TFET Benchmark

In this section are gathered the most representative Tunnel FET devices with different architectures, materials and process fabrication steps in order to compare their performance (drain voltage, on-current, off-current, I_{ON}/I_{OFF}, average SS and CMOS compatibility). The aim is to determine the trends and the possible future prospects.

Structure	V_D (V)	I_{ON} (µA/µm)	I_{OFF} (µA/µm)	I_{ON}/I_{OFF}	SS_{avg} (mV/dec)	CMOS Compt.
SOI [62]	-1.0	0.036	$5.1 \cdot 10^{-7}$	$7.1 \cdot 10^{4}$	120	Yes
SOI Ge-Source [28]	0.5	0.42	$1.2 \cdot 10^{-7}$	$3.5 \cdot 10^{6}$	50	Yes
Si NW GAA [105]	0.1	0.003	$3.0 \cdot 10^{-7}$	$1.0 \cdot 10^{4}$	50	Yes
Si NW GAA [106]	0.1	0.44	$3.0 \cdot 10^{-6}$	$1.6 \cdot 10^{5}$	50	Yes
GeOI [62]	-1.0	3	0.022	$1.4 \cdot 10^{2}$	200-300	Yes
SOI MuGTFETs [107]	-1.2	8	$3 \cdot 10^{-6}$	$2.7 \cdot 10^{6}$	250	Yes
SOI NiSi [24]	-1.0	3	$2 \cdot 10^{-8}$	$1.5 \cdot 10^{8}$	60	Yes
III-V SG InGaAs [76]	0.3	8	$5 \cdot 10^{-3}$	$1.6 \cdot 10^{3}$	140	No
III-V SG InGaAs/InGaAs [76]	0.3	17	$5 \cdot 10^{-3}$	$3.4 \cdot 10^{3}$	106	No
III-V Htj GaAsSb/InGaAs [108]	0.5	135	13.5	10	750	No
Strained SiGe/SOI [61]	-1.0	112	$3.7 \cdot 10^{-5}$	$3.1 \cdot 10^{6}$	133	Yes
Hmj InGaAs [109]	0.5	30	$5 \cdot 10^{-3}$	$6.0 \cdot 10^{3}$	200	No
Moderate Htj InGaAs [109]	0.5	78	$5.2 \cdot 10^{-3}$	$1.5 \cdot 10^{4}$	179	No
High Htj InGaAs [109]	0.5	135	$5.0 \cdot 10^{-3}$	$2.7 \cdot 10^{4}$	169	No
III-V (InAs) NW/Si Htj [79]	1	1	$1.0 \cdot 10^{-7}$	$1.0 \cdot 10^{7}$	110	No
Si Bulk JTFET [69]	0.6	0.13	$4.5 \cdot 10^{-7}$	$2.9 \cdot 10^{5}$	85	Yes
Si Bulk poc-JTFET [69]	0.6	0.15	$4.2 \cdot 10^{-7}$	$3.6 \cdot 10^{5}$	81	Yes
sSi NW [67]	-1.0	64	$2.8 \cdot 10^{-4}$	$2.3 \cdot 10^{5}$	90	Yes
SOI Wrapped gate [75]	-0.05	0.5	$1.0 \cdot 10^{-8}$	$5.0 \cdot 10^{7}$	100	Yes
SGOI NW [65]	-0.9	760	$2.0 \cdot 10^{-5}$	$3.8 \cdot 10^{7}$	80	Yes
Bulk Si [51]	-1.0	0.33	$1.5 \cdot 10^{-5}$	$2.2 \cdot 10^{4}$	300	Yes
SiGe/Si line [73]	-0.5	6.7	$2.0 \cdot 10^{-4}$	$3.4 \cdot 10^{4}$	80	Yes
III-V heterostructure InAs/Si [46]	-0.5	~ 4	$1.0 \cdot 10^{-5}$	$4.0 \cdot 10^{5}$	70-80	Yes
2D Ge-MoS_2 TFET [98]	1.0	1	$6.3 \cdot 10^{-9}$	$1.6 \cdot 10^{8}$	35	Yes

Table 2.1. Tunnel FET Benchmark with the comparison of different architectures, materials and process fabrication steps. Green="good performance", yellow="average", red="poor performance".

The benchmark in Table 2.1 verifies that using silicon as channel material does not provide a good on-current even if Germanium is used in the source [28] or if a nanowire GAA architecture with small diameter of 30-40 nm [105] or 18 nm [106] is used. An average SS lower than 60 mV/dec has been demonstrated, indicating that the process fabrication for silicon is well controlled and the concentration of traps is small. An SOI TFET with nickel silicide source [24] demonstrated a drain current of 3 µA/µm and a SS of 60 mV/dec. In another publication a strained silicon (sSi) nanowire [67] was shown to exhibit a high on-current of 64 µA/µm, but a degraded SS of 90 mV/dec. To obtain tunneling currents higher than tens of µA/µm it is mandatory to use heterojunctions of III-V materials in the channel with vertical trigate/nanowire or GAA architectures [76], [108], [109]. However because of the lack of maturity of these BTBT materials the presence of defects in the semiconductor and

the lattice mismatch with the silicon platform result in a degraded SS higher than 100 mV/dec. Moreover, these devices cannot be co-integrated with silicon CMOS. Recently, the planar integration of III-V TFETs on silicon has been demonstrated [46], but the performances are still limited. With respect to research in 2D-materials TFETs [98], the trends are very promising because of the intrinsically small body thickness (several atomic layers), but further optimization is necessary to achieve acceptable performance levels.

Examining Table 2.1 we have to conclude that not a single fabricated TFET has so far demonstrated simultaneously high on-current and a subthreshold slope below 60 mV/dec over 4 decades of drive current. The best option for the co-planar integration of TFETs with CMOS technology involves the use of trigate/nanowire architectures with very narrow body thickness (trigate) or diameter (nanowire) in SOI structures and materials such as SiGe, sSiGe, or Ge, which are commonly used in CMOS fabrication processes. It is worth noting that GeSn is emerging as a promising candidate for channel material, because of the direct bandgap, small effective mass, strain engineering and silicon compatibility. All these characteristics can enhance the performance of TFETs.

It is extremely difficult to provide an accurate benchmark of TFETs devices because there is no standard procedure to extract parameters such as SS_{avg}, I_{ON} and I_{OFF}. This explains the large spread of drain voltages used to extract the on-current in Table 2.1. The same applies to gate voltages (which are not shown in the benchmark). With respect to the average SS, the IRDS establishes that the SS should be averaged over four decades of current. Many reported data, however, only quote the minimum value of SS or an average value covering only two or three decades of drain current. In addition, the average SS is usually calculated at very low values of the drain current. To be useful for circuit applications, the values of currents for which the SS is lower than 60 mV/dec should range from 10^{-2} µA/µm to 10 µA/µm. Unfortunately, the SS in this region is degraded in all reported devices.

2.7. Conclusions

This Chapter presents an overview of Tunnel FET devices. First, the carrier injection mechanism on which TFETs rely, interband tunneling or BTBT, was introduced. Next, we used energy band diagrams for the N- and P-TFET configuration to qualitatively show that the BTBT occurs only in the source/channel junction. The Landauer equation indicates that the tunneling current is dependent of the tunneling probability T_{WKB}. Therefore, it is mandatory to reduce the tunneling length, the bandgap at the source/channel junction and the effective mass of the carriers in order to maximize BTBT. Theoretically TFETs have ability to achieve a subthreshold swing below the 60 mV/dec. The comparison of the simulated and experimental TFETs shows a gap between optimistic simulations and modest fabricated devices, because non-ideal effects such as Trap-Assisted-Tunneling, were not considered in simulations. Published results show that TAT is the major factor responsible for the SS degradation. Simulated and fabricated silicon channel planar structures yield poor TFET performance, outlining the need for boosters. Our TCAD study shows the impact on TFET performance of aggressively scaling of body thickness, gate length, EOT and the introduction of an underlapped region near the drain and new materials with small bandgap. The most important boosters to increase the performance are related to junction optimization, use of heterojunctions materials, high dielectric permittivity, body thickness, ultrathin geometry and drain-gate underlap.

Focusing on fabricated TFETs, an overview of the architectures, structures and materials used at CEA to develop Tunnel FETs is presented. The first generation of devices was based on planar $Si_{1-x}Ge_xOI$ and GeOI TFETs structures. The SOI devices show poor performance, but characteristics improve when Ge is used. The second generation of devices was fabricated in ETSOI with compressively strained $Si_{1-x}Ge_x$ body in order to increase BTBT injection. Narrow channels, high-k metal gate, strain, low bandgap in the source and low temperature anneal were used. The most innovative architecture involves making SiGe nanowire TFETs with a Ω-gate configuration in order to increase the electrostatic control with small body thickness. Trigate/nanowire architectures are one of the most promising architectures to achieve a higher on-current due to in the improvement of the electrostatic field. These are compatible with standard silicon CMOS.

Other interesting techniques for making TFETs are based on strained Si and SiGe GAA nanowire TFET structures which show good results for the on-current, although the SS is somewhat degraded. Junction TFETs and T-Gate Schottky barrier TFETs were fabricated using a Schottky junction to increase the tunneling current, but the electrical characteristics are not significantly enhanced with respect to those of standard TFETs. Another topic of interest is the parallel electric field TFETs with extension of the source into the channel and a specific silicidation process in the source, which shows improvements of BTBT current. III-V based TFETs have the objective of forming heterojunctions with a reduced tunneling length. In these devices the on-current is significantly improved, but due to the lack of maturity of these materials the presence of defects degrades the SS. As defects in the junction are responsible for a degraded SS, the junctionless TFET has been proposed to solve the problem. Simulations show that it is possible to obtain a steep SS because there are no junctions, which reduces defect generation in the semiconductor. On the other hand experimental junctionless TFETs have shown a small on-current and SS higher than 60 mV/dec. Recent research on 2D

material TFETs stems on the idea of using atomic layers in the channel region to increase the tunneling length and the electrostatic control by the gate. However, the quality of the junctions made in these materials needs to be improved. Finally, benchmarking TFETs shows that not a single fabricated TFET has demonstrated simultaneously a steep slope and high on-current. The use of trigate/nanowire architectures with SiGe, sSiGe, Ge or GeSn seem the most probable options to increase the performance in TFETs while keeping the compatibility with standard CMOS.

The key messages of this chapter are: the **comprehension of the interband tunneling mechanism through the equations that govern the tunnel probability** and the main factors that allow to enhance it. Next, it is explained that the significant **difference between simulated and fabricated TFETs it is due to secondary order effects**. Specifically, **TAT** is one of the main responsible that **degrades the possibility to achieve a sub-thermal subthreshold slope**. Via a **TCAD** study it is introduced the most important boosters to increase the TFET performance. To continue, we summarize the **fabrication TFET path followed at CEA based on co-integrability with MOSFETs**. In addition, we make an overview of other TFET state-of-the-art investigations such as III-V compounds or 2D materials. Finally, a **benchmark of the fabricated TFETs in the last decade, clearly shows the difficulty to achieve simultaneously a steep slope and high on-current**.

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Chapter 3.
Low-Temperature TFETs

3.1. Basis of 3D sequential integration

Conventional 2D planar CMOS integration based on Moore's law is reaching its limits, not only because at the transistor level the control of SCEs requires more complex architectures [1], but also because the implementation of boosters increases the overall cost of production [2]. Moreover, at the chip level, each time the density of transistors is increased, the overall length of metal interconnections is enlarged. As a result, the global delay in ICs becomes dominated by the capacitance of the metal lines. 3D monolithic integration [3], [4] appears as an alternative to the scaling of planar CMOS integration because it allows one to minimize the delay through shortening the interconnections by stacking devices on top of each other [5]. This solution is compatible with the More Moore and More-Than-Moore paths [6]–[8]. The latter relies on adding innovative functionalities and capabilities to CMOS circuits by stacking onto them extra logic levels, sensors, etc.

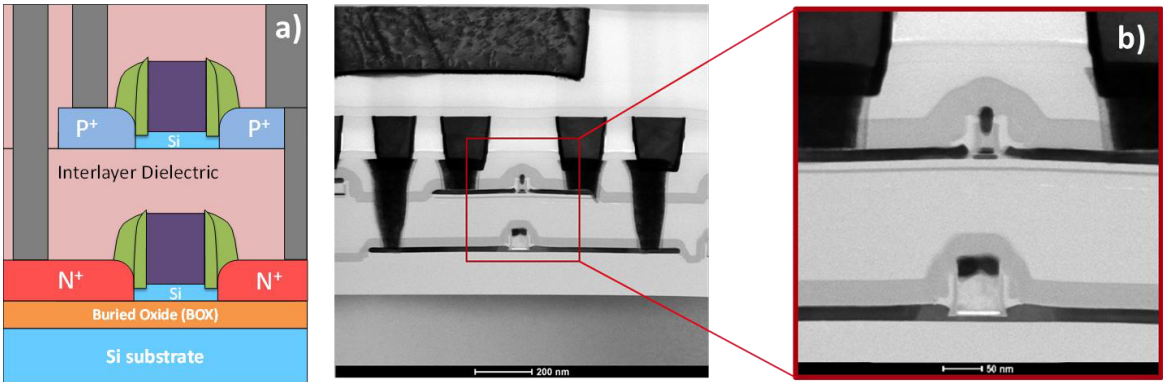

Figure 3.1. (a) 3D sequential integration schematics. Bottom tier fabricated with standard process (High-Temperature annealing). Top tier fabricated with a Low-Temperature process. (b) TEM cross-section of a sample of CMOS-over-CMOS 3D sequential integration [9].

There are two possible approaches for 3D integration, namely: (i) Parallel integration (3D Packaging), where the wafers or chips are processed separately and in a second step are stacked and contacted. The main drawback with this technique is that the contact pitch (3-8 µm) and vias density (10^5 vias/mm^2) are limited by the wafer bonding alignment [2]. (ii) Sequential or monolithic integration (3D VLSI), illustrated schematically in Figure 3.1a, is the most suitable solution owing to two main advantages. Firstly, it allows the formation of vertically stacked devices layers (bottom and top layers) processed sequentially using the same front-end process steps with a very high contact density due to the use of state-of-the-art lithography alignment [10] (via density higher than 10^7 vias/mm^2 has been demonstrated in [11]). Figure 3.1b shows an example of lithography alignment accuracy achieved in a 3D sequential CMOS structure [9]. Secondly, the co-integration of heterogeneous architectures enables the implementation of future circuits with enhanced functionality and

reconfigurability that are suitable for emerging applications requiring high 3D vias densities such as imagers, CMOS with NEMS, etc [12].

There are still important challenges to solve in 3D VLSI. More specifically, low-temperature process steps are needed for integrating the top level transistors in order to avoid the degradation of the already fabricated bottom devices and inter-tier metallization [13]. The bottom level FETs can be fabricated with a standard "High-temperature" (HT) process (annealing at 1050 ºC). So far, characteristics of devices made using the LT process have only been reported for MOSFETs. In this chapter, low-temperature (LT) TFETs are investigated [14]. These TFETs that can be used at the top level for CoolCube™ integration.

3.2. Low-temperature TFET process

3.2.1. Process flow

MOSFETs and TFETs were fabricated on 300 mm SOI wafers (11 nm thick initial silicon film) following the process flow described in Figure 3.2. The gate stack was formed using a chemical oxide interlayer (IL), plasma oxidation at 200°C, 2 nm atomic layer deposition (ALD) of high-k HfO_2, plasma nitridation at 250°C and post-nitridation anneal (PNA) at 600°C. Then, silicon nitride spacers were formed at low temperature (630°C). Intrinsic $Si_{0.73}Ge_{0.27}$ selective epitaxy was used at T = 630°C to increase the thickness of source and drain regions. An extension last (Xlast) integration scheme [15] was used for the LT devices, where junctions are implanted after source and drain epitaxy. Figure 3.2 shows that there is a split in the process flow for junction doping because there were two different anneal temperatures applied to reach the highest possible dopant concentration. Dopant activation using the SPER technique is achieved by annealing at 600°C for 2 minutes. For comparison, in the High-Temperature process, the standard LDD (Lightly Doped Drain) and HDD (Highly Doped Drain) implants are followed by a 1050°C spike anneal.

High Temperature (HT) *1050 °C max.*	Low temperature (LT) *630 °C max.*
SOI : Si 11 nm / 145 nm BOX)	
Si MESA patterning	
Gate stack deposition, litho., etching PolySi 50 nm / TiN 6.5 nm / HfO_2 (525°C)	
Spacers 1 (nitride)	
$Si_{0.73}Ge_{0.27}$ Raised Source-Drain epitaxy (630°C)	
LDDp (extensions p) lithography	
BF2 implant	Ge Pre-amorphization implant (PAI) *see TEM image in Fig. 3.3* + B implant
LDDp (extensions p) resist stripping	
LDDn (extensions n) lithography	
As implant	Ge Pre-amorphization implant (PAI) + P implant
LDDn (extensions n) resist stripping	
Anneal **950°C** Spike	Anneal **600°C** 2 min (**SPER**)
Spacers 2 (nitride / oxide)	
HDDp (litho., B & BF_2 implants, strip)	
HDDn (litho., As & P implants, strip)	
Dopant activation **1050°C** spike	
NiPt silididation, Back-end process	

Figure 3.2. Simplified process flow for CMOS TFET fabrication. The new low-temperature process with Xlast and SPER techniques (LT: 600°C) is compared to the reference (HT: 1050°C) [14].

TFETs can readily be made using a standard SOI CMOS process, although fabrication sequence used here was not specifically optimized for Tunnel FET architecture. The integration of TFETs into our silicon platform is straightforward and all the boosters used to increase the performance in CMOS technology can be also implemented for TFETs. In addition, this approach will permit direct comparison between identical device structures made using either a hot or a cold process.

3.2.2. Focus on PAI and SPER techniques

For dopants activation, low-temperature (600°C) solid-phase epitaxial regrowth (SPER) is used. Prior to this step the amorphization of the source and drain regions is required [4], [16], [17]. We use a Germanium Pre-Amorphization Implant (PAI) in order to form a homogeneous amorphous region [18]. This step is critical because dopants will only be activated in the amorphized region. Next, the implantation of dopants (boron and phosphorus) is performed. The recrystallization occurs from the bottom of the SOI film, which acts as a seed. Therefore, the energy of implantation for Germanium PAI has to be well controlled in order to avoid the amorphization of the whole SOI film and preserve a monocrystalline bottom layer. Figure 3.3 shows that indeed the amorphized region after PAI (green dashed lines) does not reach the film-BOX interface.

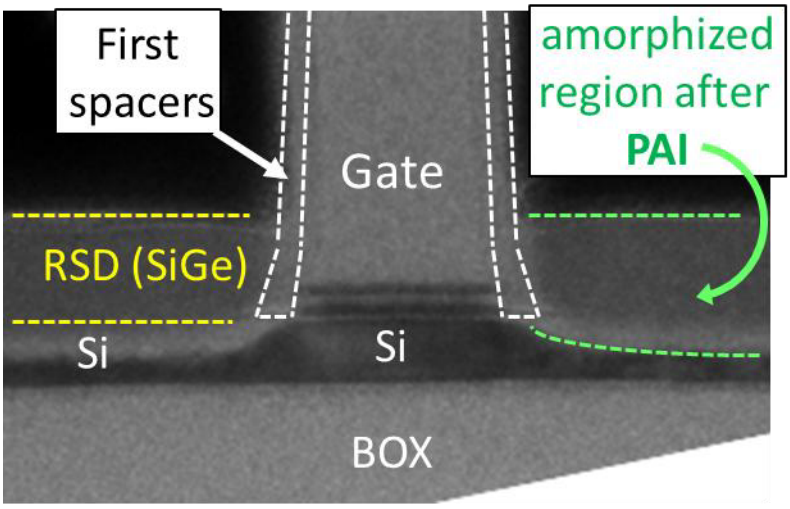

Figure 3.3. Cross-sectional TEM image of a LT device after Pre-Amorphization Implant showing the amorphized region prior to dopant implantations.

3.3. Electrical characterization

3.3.1. Dual I_D-V_{DS} method

A previous study using Cross-sectional Transmission Electron Microscopy images and Energy-Dispersive X-ray spectroscopy analysis [19] demonstrated that the silicidation process was giving rise to diffusion of Nickel into the N^+ junction in some fabricated devices, spreading under the gate. As a result, p-i-n gated structures were not behaving as TFETs, but rather as p-i-Metal structures (SBFETs). The dual I_D-V_{DS} electrical characterization method

[20], [21] allows to determine whether the current in the gated diodes is governed by band-to-band tunneling or by Schottky Barrier (SB) conduction. As established in Chapter 2, we have to determine if devices are TFETs or SBFETs because even though SBFETs have a higher drain current than TFETs, they are unable to achieve a SS lower than 60 mV/dec [22] at room temperature. On the other hand in TFETs, a poor interface quality leads to TAT [23] which degrades the subthreshold slope of the device, increasing SS well above 60 mV/dec at room temperature.

Dual I_D-V_{DS} method consists in interchanging the roles of the contacts. The polarization schemes in TFET structures are:

1) P-TFET bias "natural" scheme: $V_P < 0$, $V_G < 0$, V_N = Grounded.
2) P-TFET bias "swapped" scheme: V_P = Grounded, $V_G < 0$, $V_N < 0$.
3) N-TFET bias "natural" scheme: V_P = Grounded, $V_G > 0$, $V_N > 0$.
4) N-TFET bias "swapped" scheme: $V_P > 0$, $V_G > 0$, V_N = Grounded.

In the "swapped" scheme the probes are basically swapped between the N^+ and P^+ junctions, with respect to the "natural" scheme, but keeping the same voltage. The SBFET is a symmetrical device, which means that we should obtain approximately the same $I_D(V_{DS})$ characteristics for both natural and "swapped" schemes. However, when a TFET is biased with the "swapped" scheme, the p-i-n gated diode is forward biased and the device cannot be turned off by the gate terminal (explained in more detail in [19]). The schematic of Figure 3.4 presents the expected behavior for "natural" mode (quasi-identical for TFET and Schottky, hence not informative enough), "swapped TFET" and "swapped Schottky" mode. With this method and taking advantage of the asymmetry of TFETs it is possible to differentiate between a real TFET behavior and a Schottky behavior. Note the lack of saturation at high V_D which is typical from a PIN diode.

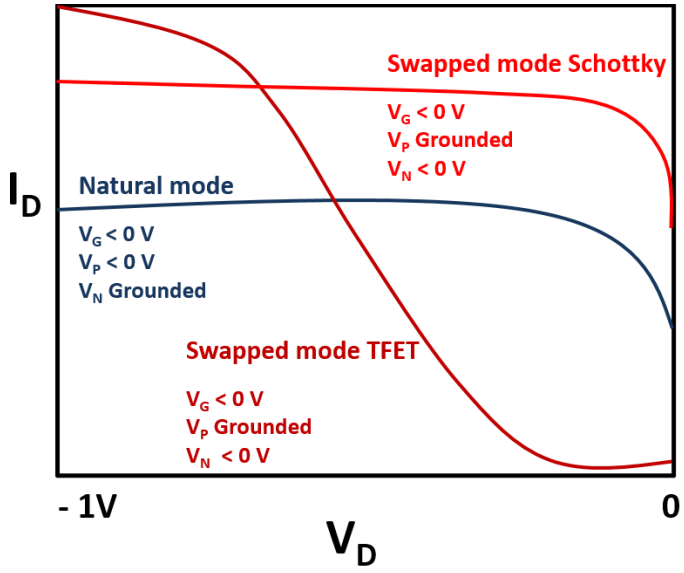

Figure 3.4. Schematic of Dual I_D-V_{DS} method for P-TFET operation. Blue line represents $I_D(V_D)$ for "natural" TFET or Schottky polarization. Dark red line exhibits the expected response of a gated p-i-n diode with BTBT behavior (TFET) and red line shows the expected response of a gated diode with Schottky behavior (SBFETs) [24].

3.3.2. Analysis of the tunneling process

The impact of using either a Low-Temperature or a High-Temperature process on the electrical characteristics is investigated using TFETs operating in the p-type mode. The TFET behavior of the fabricated devices was verified using the swapped dual I_D-V_{DS} method [19]. Swapped I_D-V_{DS} curves in Figure 3.5a and Figure 3.5b unmistakably confirm the asymmetrical behavior of the p-i-n gated diodes. It is noticeable that the current is essentially independent of gate voltage in the "swapped" mode of operation. We can, therefore, conclude that the HT and LT wide devices presented in this study are real TFETs and not Schottky-based transistors.

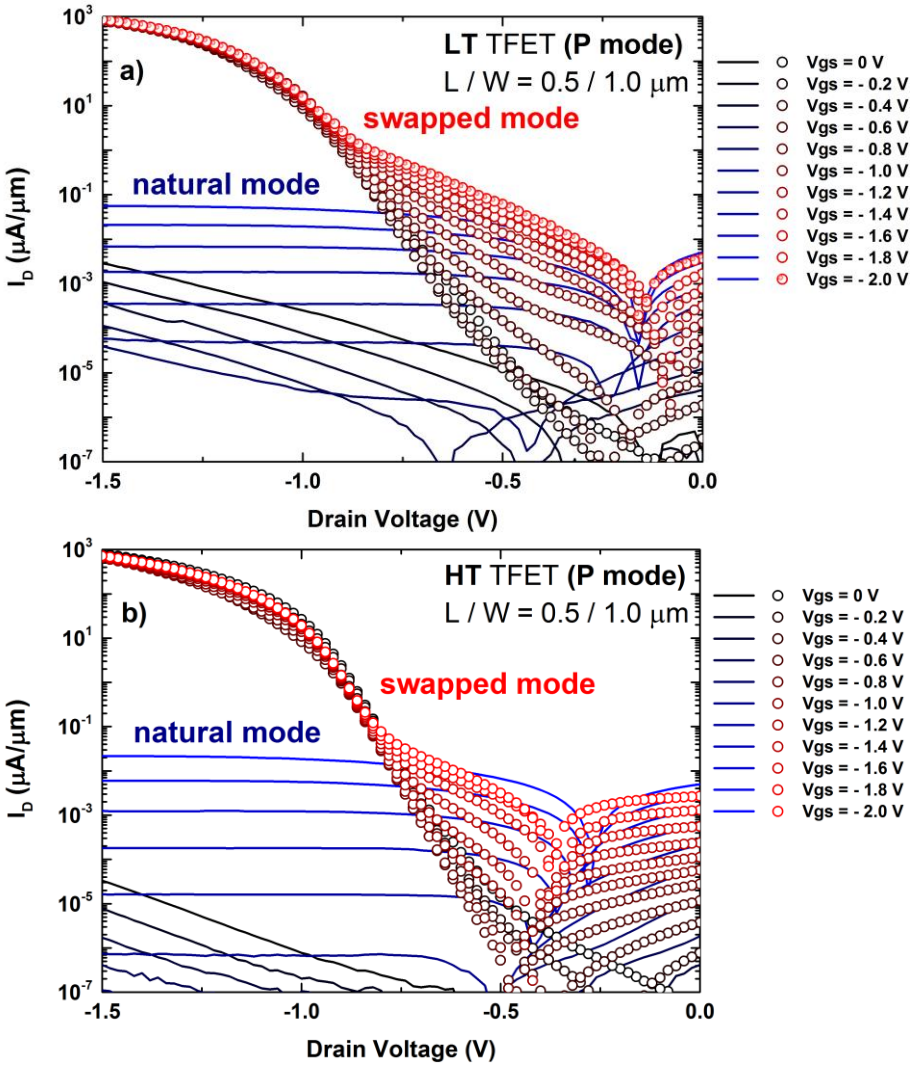

Figure 3.5. Example of dual $I_D(V_{DS})$ measurements of (a) LT TFET and (b) HT TFET, performed according to the TFET validation method detailed in [19] and showing that tunneling is BTBT and not Schottky related.

Using the swapped dual I_D-V_{DS} method, it is possible to identify the impact of the size: wide and medium-width structures (width range 2.0-0.1 µm) exhibit a well-defined TFET behavior as shown in Figure 3.5. Low-temperature narrow devices (width = 30 nm) on the other hand, show a gate voltage dependence (purple circle in Figure 3.6a) which fits a Schottky Band-to-Band tunneling behavior rather than a TFET one. However, High-Temperature narrow devices (width = 30 nm) show a voltage dependence for low values of

V_G, while for higher values of V_G the current is mostly independent of the gate voltage, which indicates a TFET behavior (Figure 3.6b). Based on this observation, we can conclude that this narrow HT device has characteristics that are in-between those of TFET and Schottky devices. The comparison of narrow devices in Figure 3.6a and Figure 3.6b establishes that the High-Temperature process yields TFETs with BTBT operation (Figure 3.6b), while the considered Low-Temperature process does not for narrow devices (Figure 3.6a).

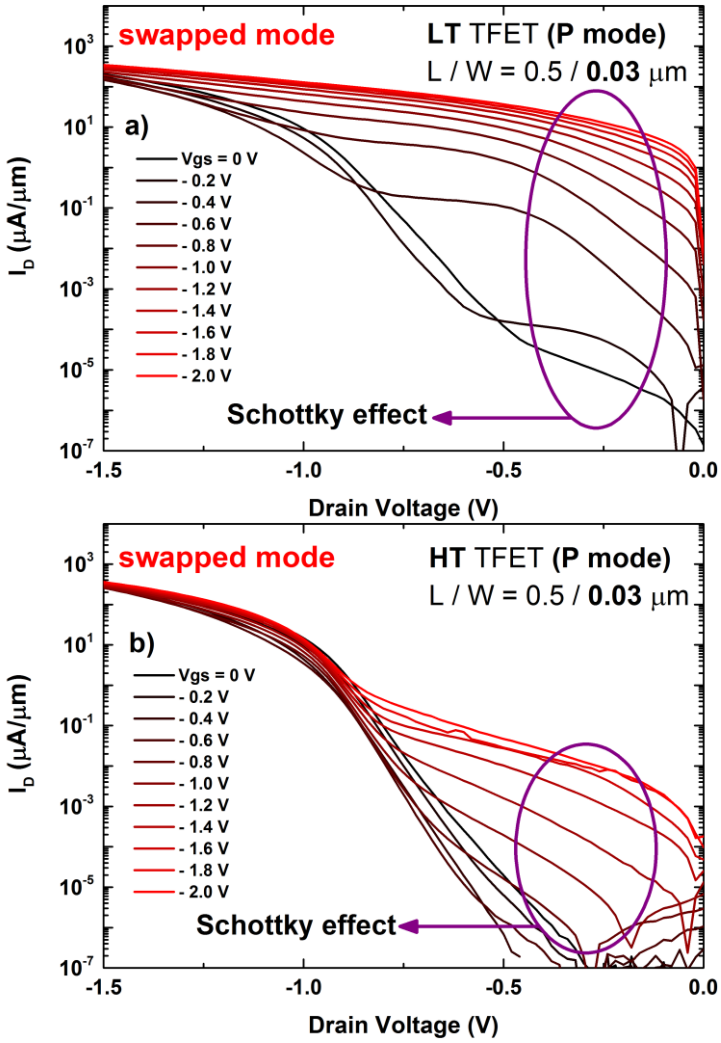

Figure 3.6. Dual $I_D(V_{DS})$ measurements for Low-Temperature and High-Temperature diodes performed on narrow devices (W = 0.03 µm). (a) In narrow LT devices the tunneling is Schottky related. (b) In narrow HT devices a transition from TFET to Schottky behavior for low values of V_{GS} is observed.

3.3.3. $I_D(V_G)$ characteristics

The $I_D(V_G)$ characteristics of the single-channel TFETs with a gate length of 0.5 µm and a width of 1.0 µm are well behaved with low leakage and reasonable I_{ON}/I_{OFF} ratio (10^4-10^6). However, the average on-current (defined at V_G = 2.0 V & V_D = 0.9 V) for both HT (~ $2.0 \cdot 10^{-2}$ µA/µm) and LT (~ $5.0 \cdot 10^{-2}$ µA/µm) TFETs is small. This is due to the fact that the channel is made of silicon, and the source/channel junction is not developed for optimized band bending: the tunneling length (λ) is not minimized, which means that a high gate voltage is required (V_{GS} = - 2 V) to obtain tunneling current.

The electrical measurements in Figure 3.7a and Figure 3.7b show a very low dispersion of the I_D-V_G curves within a given wafer for both drain biases under consideration (V_{DS} = - 0.5 V and V_{DS} = - 0.9 V). The small variation between measured devices indicates that High-Temperature and Low-Temperature processes are well controlled. The threshold voltage (V_{TH}) was defined as the gate voltage for which $I_D = 10^{-5}$ µA/µm. The use of the Low–Temperature process results in a V_{TH} reduction (approximately ~ 300 mV) and to an increase of the base leakage current (+ 1.5 decades off-current), which could be attributed to SPER related defects not entirely annealed out in the relatively thick silicon film (11 nm) [25]. Moreover, if these defects are present inside the semiconductor this could explain why the drain current is higher for LT than for HT TFETs, because a part of the drain current will be a consequence of the Trap-Assisted-Tunneling and not the BTBT. For small-medium gate voltages (from - 0.7 V to - 1.5 V) the influence of the TAT component dominates, but for higher values of applied bias at the gate terminal (from -1.6 V to 2.0 V) BTBT prevails and the drain current for HT and LT TFETs have comparable values (Figure 3.7).

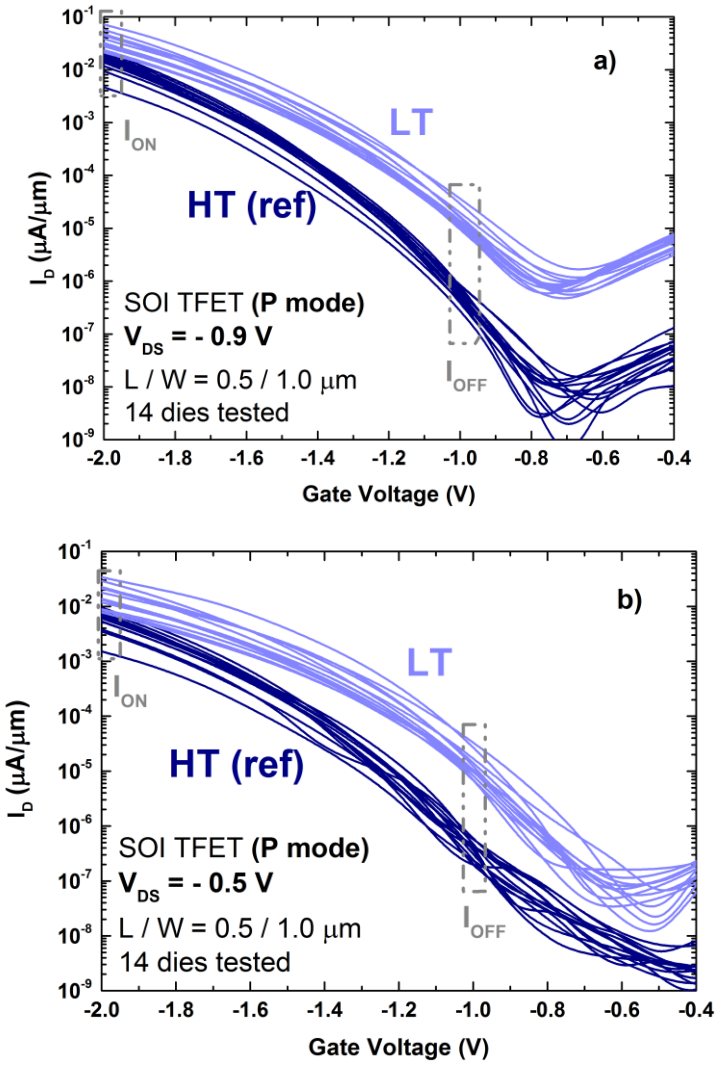

Figure 3.7. (a) Measured p-mode $I_D(V_{GS})$ curves of SOI Tunnel FETs fabricated using high-temperature and low-temperature processes (14 dies wafer) for V_{DS} = - 0.9 V; (b) Measured p-mode $I_D(V_{GS})$ curves of SOI Tunnel FETs fabricated with HT and LT processes (14 dies per wafer) for V_{DS} = - 0.5 V.

The V_{TH} lowering results in a promising increase of the on-current for Low-Temperature TFETs of ~ 100-200% over the High-Temperature in I_{ON} plots (Figure 3.8). This shift of the

threshold voltage could be explained by the impact of the junction position on the device performance. Because of the temperature difference of annealing between the HT (1050°C) and LT (650°C) process, dopant diffusion in the source/channel junction is not the same and affects junction abruptness and the location where BTBT takes place.

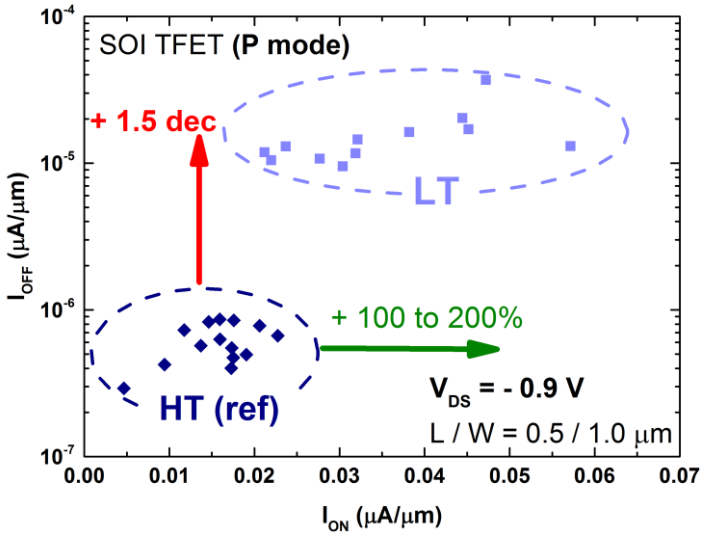

Figure 3.8. Impact of TFET process (HT vs LT) on $I_{ON}(I_{OFF})$ plots with on-current measured at V_{GS} = -2 V, off-current at V_{GS} = - 1 V (for p-mode TFETs) and V_{DS} = - 0.9 V.

The subthreshold swing extractions at V_{DS} = - 0.9 V in Figure 3.9 show very similar performance in LT and HT TFETs. As the fabrication CMOS process flow is not optimized for tunneling switches, the minimum slope obtained is 160 mV/dec which remains well above of the theoretical 60 mV/dec value and the current is still modest. These Tunnel FETs devices lack the abrupt doping profile at the source junction that is necessary to achieve steep-slope switching. In addition, silicon is not the best choice for tunneling devices due to its relatively wide bandgap. For example, replacing silicon with SiGe or Ge has been documented to increase the tunneling probability [26], [27]. **The main conclusion drawn from this analysis is that the performance of LT TFETs is comparable to that of HT devices and no noticeable degradation due to the LT process is observed**. It is worth noting that the LT process can easily be adapted to SiGe or Ge.

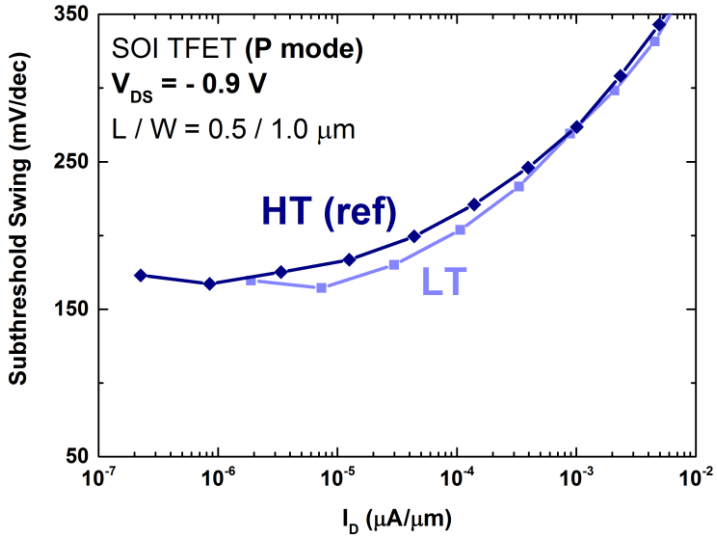

Figure 3.9. Figure of merit SS(I_D) of p-mode TFETs (for HT versus LT devices) at V_{DS} = - 0.9 V.

We have also investigated the impact of the gate length reduction on $I_D(V_G)$ curves. TFETs physics states that the on-current is not limited by transport (as it is in MOSFETs), but by the BTBT generation, which does not depend on gate length. Results in Figure 3.10a show that gate length reduction in wider (W = 2.0 µm) HT TFETs does not impact the on-current significantly, except for very small values (L_G < 70 nm), where a small degradation due to short-channel effects is noticeable [28]. For wider (W = 2.0 µm) LT TFETs in Figure 3.10b, there are minor effects in on-current down to L_G = 0.15 µm. Beyond this point, a very aggressive gate length scaling generates a significant degradation of the on-current (not shown in Figure 3.10b). LT device with L_G < 0.15 µm were not functional. Process optimization to make short-channel MOSFETs and TFETs is currently in progress.

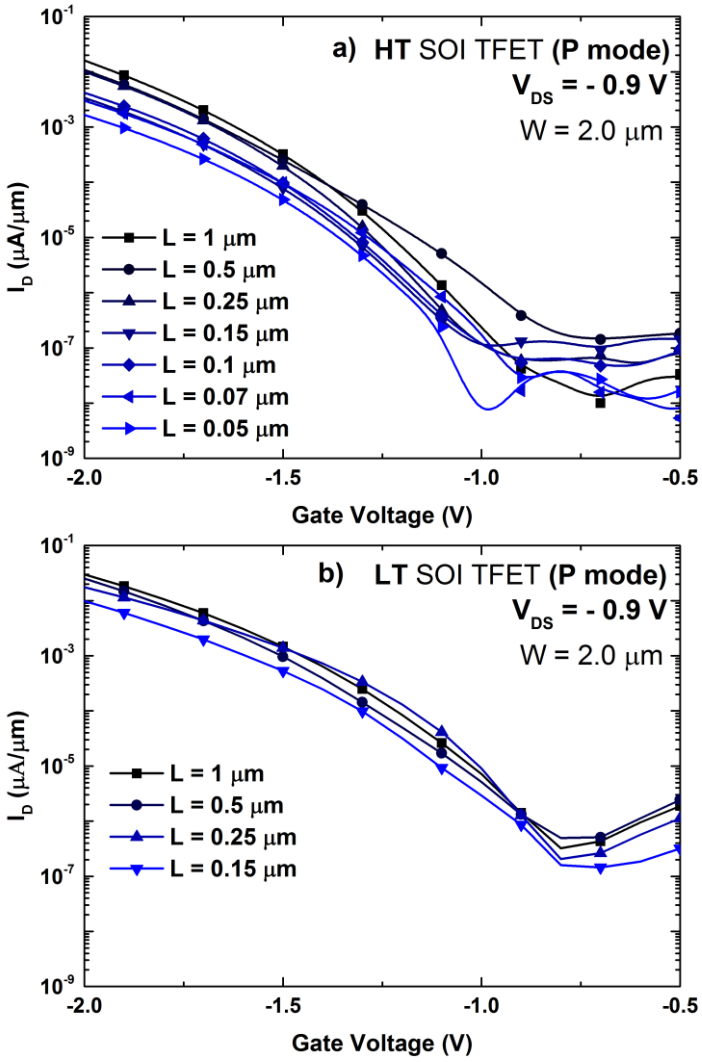

Figure 3.10. Impact of gate length reduction on (a) wide (W = 2 µm) HT SOI TFET at V_{DS} = - 0.9 V. Minor degradation of on-current for L_G < 0.15 µm is observed; (b) wide (W = 2 µm) LT SOI TFET at V_{DS} = - 0.9 V. More aggressive (shorter) gate lengths show excessive gate leakage current.

3.4. Simulation of Low-Temperature TFETs

2D TCAD simulations of TFETs with silicon source, drain and channel were carried out to analyze the physical reasons behind the HT/LT differences observed in the measurements. For the simulation deck we have used the same parameters as in the fabricated TFETs. The most significant values are: L_G = 0.5 µm, W = 1.0 µm, T_{BOX} = 145 nm, T_{Si} =11 nm, EOT =1.18 nm and a dopant concentration of $N_D = N_A = 10^{20}$ cm^{-3} for Source and Drain. We assumed dopant profile parameters (lateral junctions position, abruptness) typical of the "HT" and "LT" processes: overlapped junctions with standard abruptness for HT (higher dopant diffusion because of spike anneal has been simulated with a smooth Gaussian decay of 1.5-2.0 nm/dec) and underlapped abrupt junctions for LT (with a reduced Gaussian decay of 0.5-0.7 nm/dec, due to the lower temperature of SPER process). Even if this description (Figure 3.11) does not exactly correspond to the real doped regions, it enables one to capture the difference in terms of tunneling efficiency.

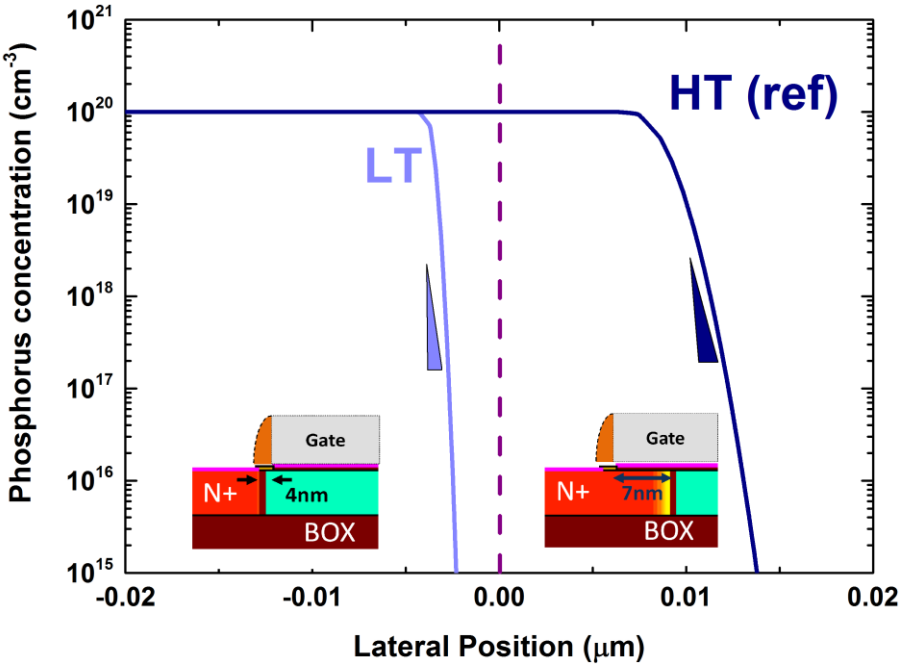

Figure 3.11. Doping profile of simulated "HT" and "LT" structures, showing the junction position with respect to the gate edge. Inset images show the schematic of the simulated TFETs. [24]

In the simulated $I_D(V_{GS})$ transfer characteristics curves (Figure 3.12), it is possible to observe that drain current is higher in "High-Temperature" TFETs than in "Low-Temperature" TFETs in apparent contrast with experimental results reproduced in Figure 3.7a. In order to get rid of the threshold voltage variations and obtain an accurate comparison, we have defined on-current at a given gate overdrive (V_{GS}-V_{TH}).

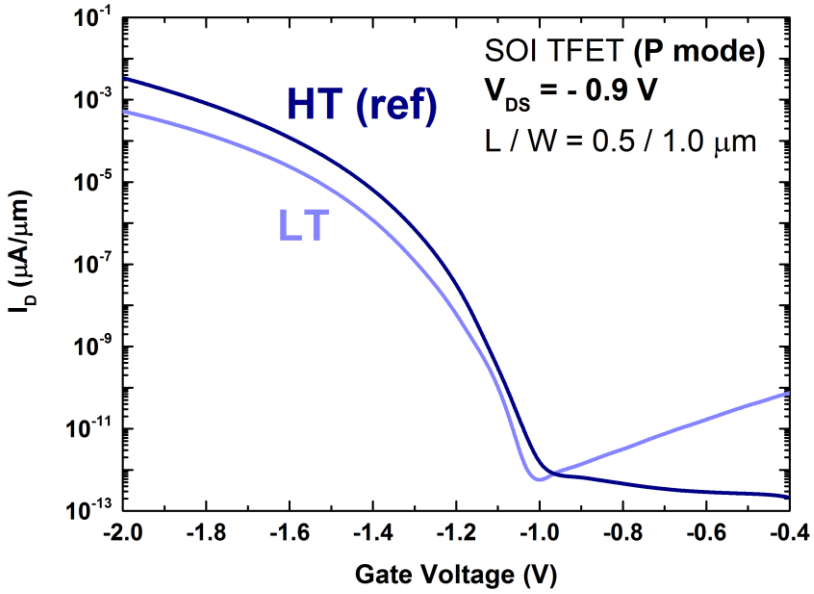

Figure 3.12. Simulated p-mode $I_D(V_{GS})$ curves of SOI Tunnel FETs with overlapped junctions ("HT" process) and underlapped junctions ("LT" process).

One can note in Figure 3.13 that HT structures still yield better on-current performance although the LT performance is not far behind.

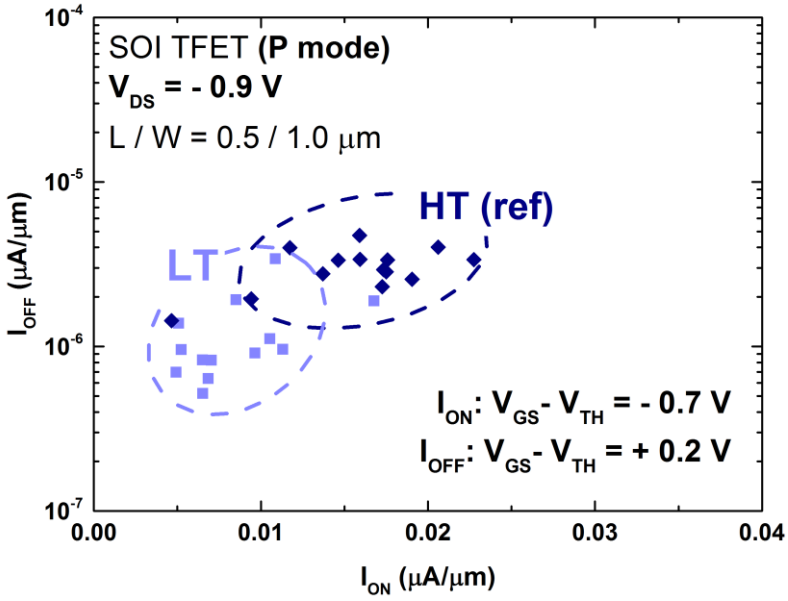

Figure 3.13. Updated $I_{ON}(I_{OFF})$ plots (measurements data) with corrected definitions of I_{ON} and I_{OFF}: I_{ON} extracted at V_{GS}-V_{TH} = - 0.7 V and I_{OFF} at V_{GS}-V_{TH} = + 0.2 V.

The trends of simulations results in Figure 3.12 are confirmed by $I_{ON}(I_{OFF})$ experimental data when corrected for V_{TH} (Figure 3.13). High-Temperature TFETs exhibit on-current that is roughly twice that of Low-Temperature devices ones, but the off-current defined at V_{GS} - V_T = + 0.2 V is approximately 5 times higher. The minimum leakage current, however, is lower in HT devices as shown in Figure 3.7a.

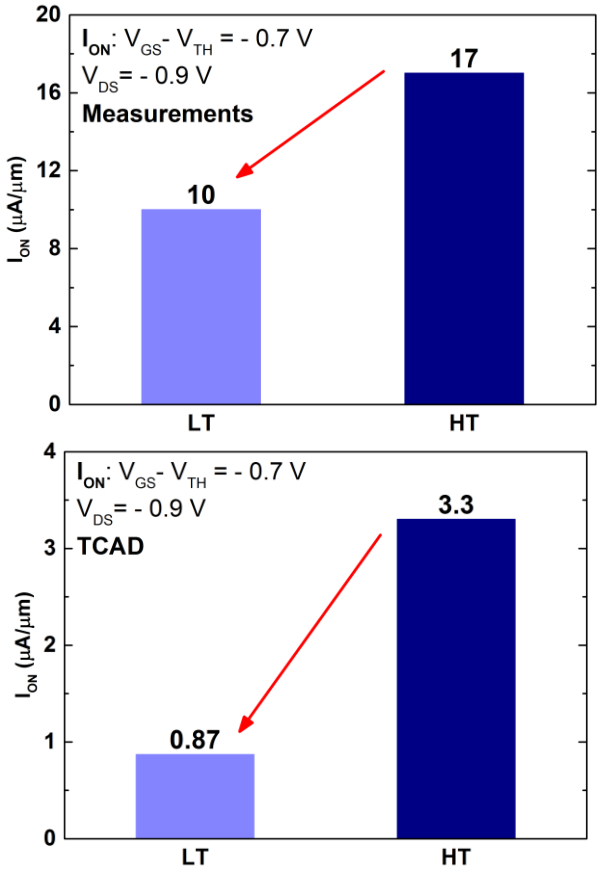

Figure 3.14. Tentative comparison of HT vs. LT performance by measurements and TCAD simulations. Relative on-current at V_{DS} = - 0.9 V.

It is well stablished that for a given gate overdrive, in both experimental results and TCAD simulations (Figure 3.14) the High-Temperature TFETs present a higher relative on-current than the Low-Temperature TFETs. The difference between measurements and simulations relative to the on-current could be explained by simulations being performed with full silicon source, drain and channel, while the fabricated TFETs structures have SiGe raised source and drain which in fact increase the performance of the pTFET. SiGe acts as a booster by decreasing the energy band gap in the source region (where BTBT takes place) which generates an increase of the on-current with respect to the simulated silicon-only TFET.

3.5. TFET Benchmark comparison

Table 3.1 benchmarks our Low-Temperature and High-Temperature TFETs to other TFET from the literature. **These planar SOI Tunnel FETs are the first reported with Low-Temperature process fabrication**. HT and LT TFETs with different gate lengths, from L_G = 500 nm down to L_G = 50 nm, were fabricated and measured. LT TFETs exhibit an on-current in line with SOI past results obtained at CEA-Leti [29] but lower than TFETs with a SiGe channel [30]. Besides, LT TFETs presents a higher off-current (~ 10 pA/µm) than HT TFETs (~ 0.7 pA/µm), as consequence of defects that cause TAT are less passivated at low-temperature annealing. For both HT/LT devices, the subthreshold swing is degraded because the process fabrication it is not yet optimized for TFETs.

Reference	Structure	EOT (nm)	T_{BODY} (nm)	L_G (nm)	V_{DS} (V)	I_{ON} (µA/µm)	I_{OFF} (µA/µm)	I_{ON}/I_{OFF}	SS_{avg} (mV/dec)
This work	SOI HT	1.18	11	500/50	-0.9	$2.3 \cdot 10^{-2}$	$6.6 \cdot 10^{-7}$	$3.4 \cdot 10^{4}$	175
	SOI LT				-0.5	$5.7 \cdot 10^{-2}$	$1.3 \cdot 10^{-5}$	$4.4 \cdot 10^{3}$	179
F.Mayer et al. (CEA-Leti) [29]	SOI	3	20	100	-1.0	$3.6 \cdot 10^{-2}$	$5.1 \cdot 10^{-7}$	$7.1 \cdot 10^{4}$	120
C. Le Royer et al. (CEA-Leti) [30]	SGOI	2.3	12	1000	-0.9	0.1	$4.0 \cdot 10^{-7}$	$2.5 \cdot 10^{5}$	188
Q. Huang et al. (Pekin U.) [31]	Bulk Si	-	-	200	-1.0	0.33	$1.5 \cdot 10^{-5}$	$2.2 \cdot 10^{4}$	~280
M. Kim et al. (Tokyo U.) [32]	Ge/sSOI (1.1%)	2.5	10-13	-	1.0	1.0	$1.0 \cdot 10^{-8}$	$1.0 \cdot 10^{8}$	70
S. Blaeser et al. (FZ Jülich) [33]	SiGe line	4	5	200	-0.5	6.7	$2.0 \cdot 10^{-4}$	$3.4 \cdot 10^{4}$	80
M. Noguchi et al. (Tokyo U.) [34]	III-V planar (InGaAs)	1.3	100	-	0.15	2.0	$1.0 \cdot 10^{-6}$	$2.0 \cdot 10^{6}$	64
R. Pandey et al. (Pennsylvania U.) [35]	III-V vertical	0.8	-	200	-0.5	14	$3.0 \cdot 10^{-4}$	$4.7 \cdot 10^{4}$	~200
K. Moselund et al. (IBM) [36]	III-V planar	1.75	27	900	-0.5	4	$1.0 \cdot 10^{-5}$	$4.0 \cdot 10^{5}$	70-80
E. Memisevic et al. (Lund U.) [37]	III-V NW	-	20	100	0.3	10.6	$1.0 \cdot 10^{-3}$	$1.1 \cdot 10^{4}$	~55
S. Glass et al. (FZ Jülich) [27]	SiGe/Si	2	13	-	0.05	$2 \cdot 10^{-2}$	$1.0 \cdot 10^{-8}$	$2.0 \cdot 10^{6}$	87

Table 3.1. Benchmark for different TFET structures (planar, SOI, bulk Si, vertical) and materials (Si, SiGe, III-V materials), which are currently under research.

In general, all-silicon TFETs exhibit a performance that is lower than that of SiGe and III-V TFETs. Results on Bulk Silicon TFETs [31] have proven the importance of using boosters to increase tunneling performance. These boosters are:

- Asymmetrical structures to reduce the off-current at the drain region.
- EOT scaling to achieve a steep switching and high on-current by means of an enhancement of the gate electrostatic control.
- Narrow bandgap materials (Ge, III-V) for increasing on-current with high tunnel probability.
- Abrupt doping profile at source junction for steep switching and high on-current due to a thin tunneling barrier.

The TFET with Ge-source and a strain SOI [32] shows a limited on-current of 1 µA/µm and a SS of ~ 70-80 mV/dec over four decades of current. Other solutions to improve the tunneling current rely on vertical BTBT generation using architectures such as the SiGe line TFET [33], which exhibits a higher on-current (6.7 µA/µm) with one of the lowest SS ever reported, but over a reduced range of I_D current. New innovations related to the fabrication process have been recently presented in order to enhance the vertical BTBT and improve the SS. Among those are the use of an $Si_{0.50}Ge_{0.50}$/Si heterostructure with vertical tunneling path [27].

III-V based TFETs [34]–[37] show the highest on-currents owing to the possible formation of a staggered or broken gap in the tunnel junction [35], [36], but their SS is severely degraded because the processing of these materials is less mature than that of silicon, and a large number of defects (traps) is generated in the semiconductor [23]. New improvements such as the formation of an Zn-diffused source in InGaAs TFET [34] allows for a steeper doping profile with a smaller defect density. This results in an SS of 64 mV/dec over 3 decades of drain current (from 10^{-5} µA/µm to 10^{-3} µA/µm), although the achieved on-current in only of 2.0 µA/µm. The most promising solution is the use of vertical nanowires architectures with an aggressively scaled diameter (lower than 20 nm) to increase the electrostatic control. The most recent example is a vertical InAs/GaAsSb/GaSb TFET [37] on silicon with an on-current of 10.6 µA/µm (at V_{DS} = 0.3 V) and a SS of ~ 55 mV/dec over 3 orders of current (from 10^{-3} µA/µm to 10^{-1} µA/µm). Unfortunately, the integration of these III-V materials into silicon platform is very challenging [36], so further improvements need to be investigated to increase the on-current and extend the range of reduced Subthreshold swing in the area of interest, namely from 10^{-2} µA/µm to 10^{1} µA/µm.

3.6. Impact of fin width on TFET performance

The study of the impact of the fin width on device performance has revealed an interesting dependence. The transfer characteristics in Figure 3.15a show that there is an enhancement of the drive current in multi-channel TFETs with narrow fins (W_{fin} = 0.1 µm) when compared with thicker fins (W_{fin} = 1.0 µm or 0.5 µm). The effective width of the devices is given by $W_{eff} = N_{channels} \times [(W_{fin} - \Delta W) + 2 \times T_{Si}]$. This behavior seems to be the opposite to the drain current-width dependence known in MOSFETs, where a reduction of the width implies a reduction of the drain current. In order to determine if this phenomena is related to the effective electric field, the drive current has been plotted versus the gate voltage overdrive V_G - V_{TH} for different fin widths in Figure 3.15b. We consider that V_{TH} is the voltage for which the drain current is equal to 10 nA. Results indicate that that the 4 curves are superimposed; if the current is normalized (in µA/µm), the current actually increases as the fin width is decreased, meaning that in narrow fin the effective electric field in the BTBT region is higher. It also suggests that the BTBT occurs in the corners of the devices, since total current is independent of fin width.

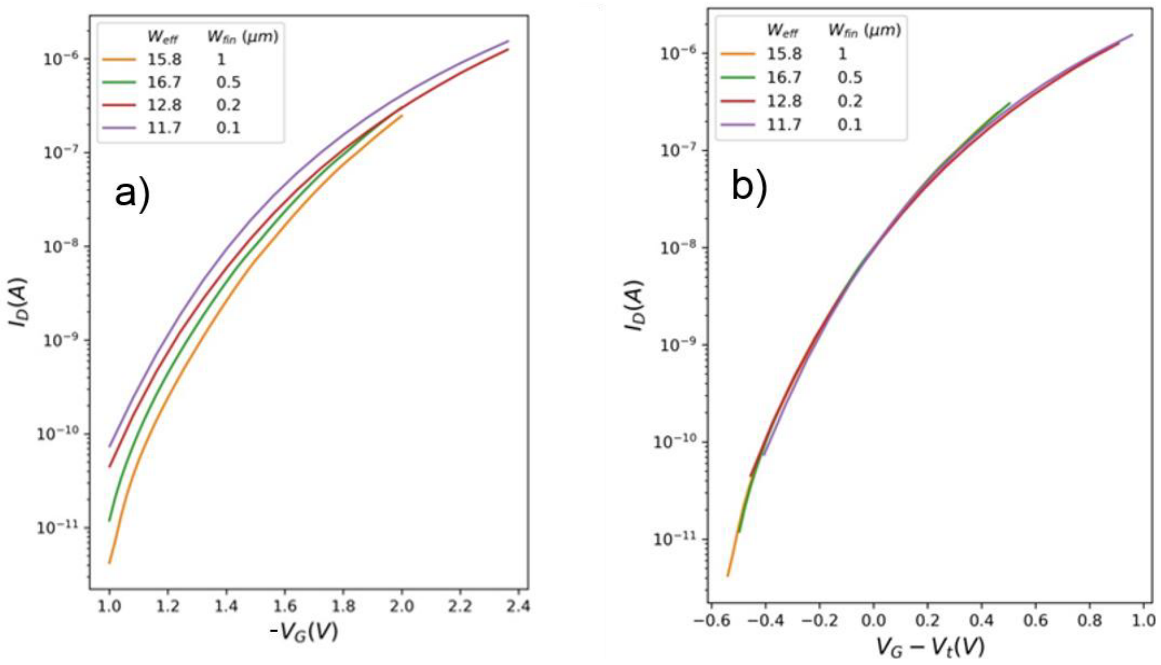

Figure 3.15. (a) Average $I_D(V_G)$ curves of multi-channels HT P-TFETs with L_G = 0.5 µm and different fin widths and number of channels: orange (15 channels, over 50 dies), green (30 channels, over 74 dies), red (50 channels, over 100 dies) and purple (75 channels, over 100 dies); (b) Average drain current versus gate voltage overdrive. V_{DS} = - 0. 9V.

3D TCAD simulations were performed for different widths, while keeping the gate length constant (L_G = 50 nm) in order to shed light on the trend exhibited by experimental Tunnel FETs. The geometry of the simulated TFETs, with narrow widths and shorter gate length, differs from the fabricated TFETs, because it would be computationally expensive and in some cases infeasible to simulate devices with the same geometries as in the measured devices. Figure 3.16 clearly shows that the BTBT generation in a trigate TFET architecture with W_{fin} = 40 nm, is concentrated in the source junction at the top sidewall corners. Moreover, the contribution to the tunnel current of the rest of the top surface (W_{top}) is

negligible for fin widths over 40 nm. This could explain why the progressive reduction of the width on fabricated TFETs does not show a decrease of the tunneling current. In addition, as explained in Chapter 2, TFETs based on nanowire structures with very narrow diameters present an increase of the performance and steep subthreshold slope attributed to a better electrostatic control by the front gate voltage. Now, we present the 2D mapping of the BTBT for widths narrower than 40 nm.

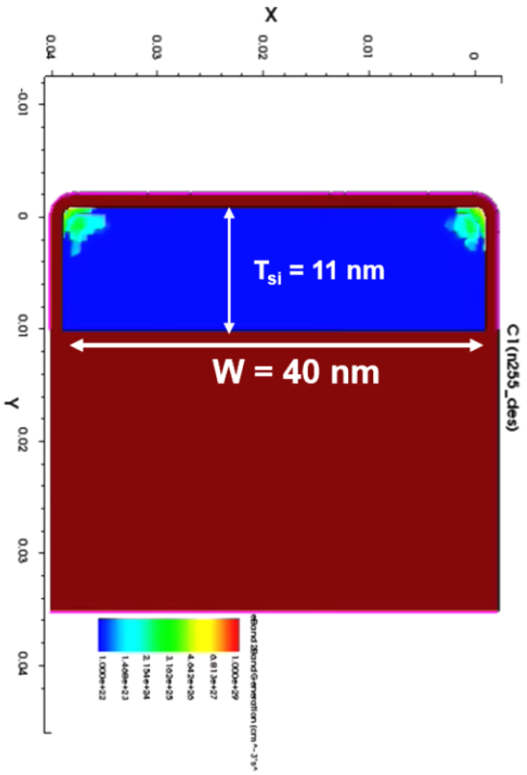

Figure 3.16. Longitudinal cut of a 3D simulated TFET with T_{Si} = 11 nm, W_{fin} = 40 nm and L_G =50 nm showing that the electron BTBT generation is located at the corners of the sidewalls. V_G = 2.0 V and V_{DS} = 0.9 V.

Figure 3.17a shows the electron BTBT generation for a TFET with W_{fin} = 18 nm. BTBT is still almost only located at the corners, but due to the reduction of the width and thus, the surface, the electrostatic control via the gate voltage has improved at the channel top surface. This becomes even clearer for a W_{fin} = 10 nm (Figure 3.17b) where the W_{top} significantly starts to contribute to the tunneling current. Besides, BTBT is present not only at the top-channel but also at the mid-channel region.

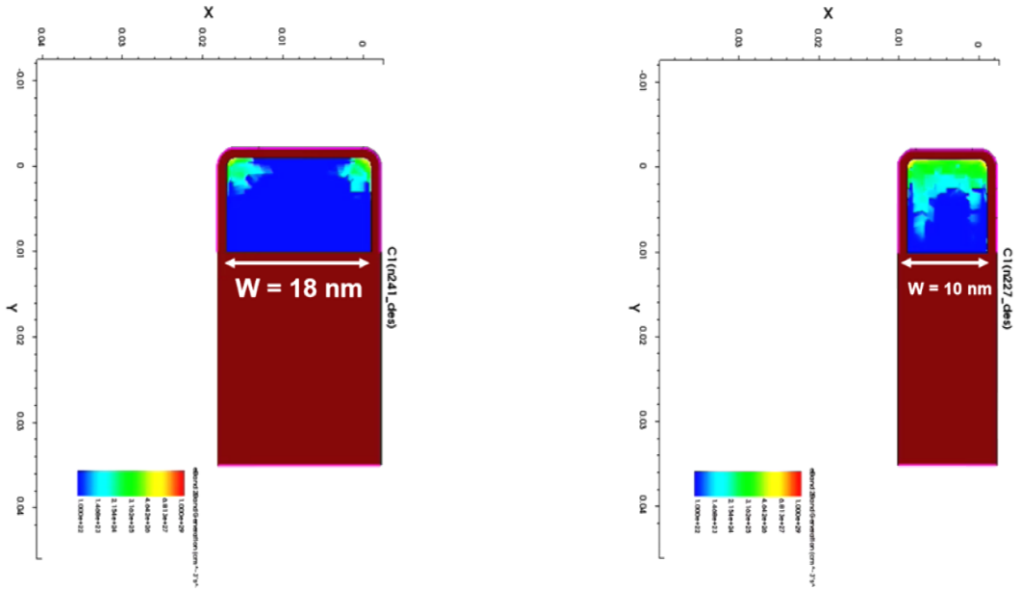

Figure 3.17. Longitudinal cut of 3D simulated Tunnel FET devices with T_{Si} = 11 nm and L_G = 50 nm for: (a) W_{fin} = 18 nm and (b) W_{fin} = 10 nm. V_G = 2.0 V and V_D = 0.9 V.

Finally, for W_{fin} = 5 nm we can observe in Figure 3.18 that BTBT generation occurs in the whole silicon cross section. The major contributions are still found at the corners and the top surface, but there is also a secondary contribution at the bottom of the channel and the sidewalls. Therefore, the tunneling generation area is higher for W_{fin}= 5nm than for wider widths, because the gate terminal has a more efficient electrostatic control over the body region. These results could explain why in experimental measurements a higher drive current is obtained for extremely narrow fins. On the other hand, the additional contribution of the volume in nano-scaled devices reminds us the concept of "volume inversion" in MOSFETs [38].

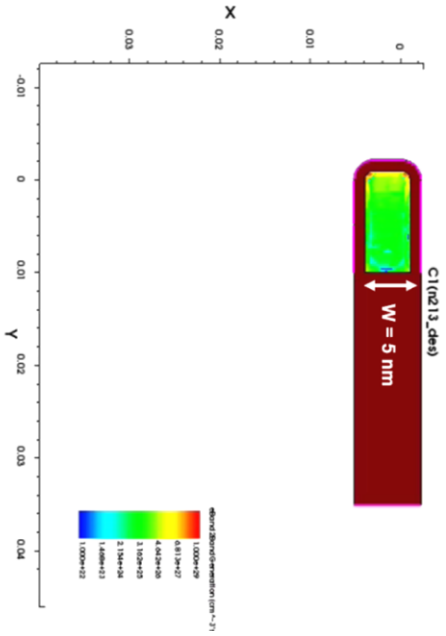

Figure 3.18. Longitudinal cut of 3D simulated TFET with T_{Si} = 11 nm, L_G = 50 nm, and W_{fin} = 5 nm showing that BTBT generation occurs across the whole silicon body thickness.V_G = 2.0 V and V_D = 0.9 V.

The simulated I-V characteristics in Figure 3.19a show the very same behavior as the experimental data. Tunnel FETs with W_{fin} = 5 nm show a higher drain current than wider devices. Moreover, the drain current versus the gate voltage overdrive (at 0.01 nA) in Figure 3.19b shows the matching of the 4 curves, which confirms that the total current is independent of fin width. These results are important because, they indicate that multi-finger structures with narrow widths deliver a higher tunneling current and steeper subthreshold slope than a wider device with same W_{eff}. Besides, the output current will be given by the total number of fabricated fins.

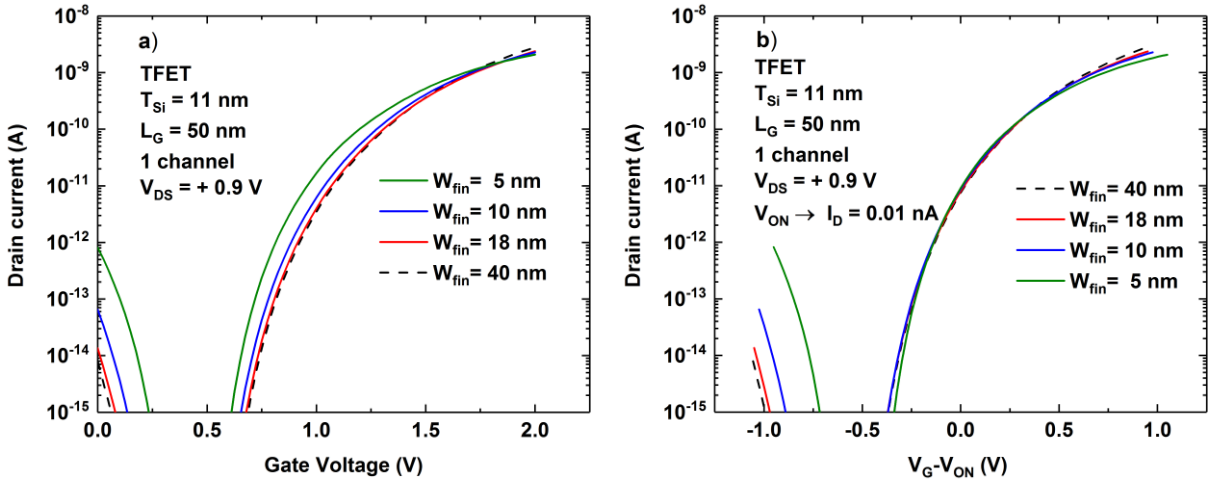

Figure 3.19. (a)Transfer characteristic of 3D simulated TFETs with L_G = 50 nm and different fin widths (40 nm, 18 nm, 10 nm and 5 nm); (b) Drain current versus gate voltage overdrive.

3.7. Conclusions

3D sequential integration emerges as an alternative to 2D planar scaling based on the formation of vertically stacked tiers with a very high contact density and enabling the co-integration of heterogeneous architectures to implement circuits with higher functionality. The thermal budget of the top tier is limited to low temperatures (for dopant activation, gate oxide stabilization, epitaxy and spacer deposition) to avoid the degradation of the transistors and metallic lines in the already fabricated bottom layers.

In this chapter, we have analyzed the electrical characteristics of TFETs made using a Low-Temperature process (600°C) designed for 3D sequential integration. In order to achieve complete dopant activation at LT it is necessary to use a Germanium Pre-Amorphization Implant (PAI) and SPER. Dual I_D-V_{DS} characterization confirms that wide devices studied for both HT and LT present a TFET behavior. On the other hand, narrow devices present a Schottky behavior in Low-Temperature devices, while High-Temperature devices have characteristics comprised between those of a TFET (for high gate voltage) and a Schottky FET (for low gate voltage). Systematic measurements show a well-defined behavior, from which we can conclude that the decrease of processing temperature (600°C) does not alter the electrical characteristics of LT TFETs. These characteristics remain comparable to those of reference devices fabricated at 1050°C, verifying that in both cases the process fabrication is well controlled. LT TFETs exhibit a higher on-current and off-current than the HT TFETs, most likely due to the presence of defects not annealed out at low-temperature. Also, LT and HT devices have different threshold voltages, which can be explained by a difference in junction position. The subthreshold swing is larger than 60 mV/dec, because the process flow fabrication is CMOS compatible and the junction engineering is not optimized for tunneling switches. A study of the gate length reduction shows a limited impact in the performance for HT TFETs, while for LT process aggressively scaled gate lengths TFETs are not functional. TCAD simulations based on full silicon homojunction structures and experiments show similar trends for a given gate overdrive.

These proof-of-concept devices have demonstrated the feasibility of LT TFETs. Their performance is modest but similar with that of other all-silicon TFETs fabricated at a higher temperature. Based on these new results, technology boosters such as SiGe or Ge in the channel, III-V materials or Gate-All-Around architectures such as nanowires with a reduced diameter, or vertical BTBT are being implemented for device optimization. In addition, our experimental Tunnel FETs exhibit an increase of the tunneling current with the fin width reduction. 3D TCAD analysis has demonstrated a larger tunneling generation surface in extremely narrow TFETs (W_{fin} = 5 nm) due to a more efficient electrostatic control from the gate terminal to trigger the BTBT mechanism. Therefore, multi-finger trigate/nanowire structures with an ultra-thin reduced channel thickness/diameter appears as a feasible option for TFET implementation in 3D Power scaling.

The key messages of this chapter are: First, **the planar Low-Temperature TFET has potential for 3D sequential integration as a top level device for use with low bias supply operation**. Secondly, **the performance of LT TFETs is comparable to that of HT devices, but low-thermal budget TFETs present a higher off-current** than HT counterparts**.** This is most likely due to the presence of implantation defects not sufficiently annealed. Moreover,

the **LT process can be adapted to SiGe or Ge body** in order to reduce the tunneling length at the source/channel junction and increase the tunneling probability. Finally, the **enhancement of performance in multi-channel trigate/nanowire TFET architectures**, open the door to consider Tunnel FET as an interesting option for ultra-low power applications in 3D Power scaling.

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Chapter 4.
Investigation of defects in Tunnel FET devices

4.1. Introduction

The characterization of Low-Temperature P-type TFETs in Chapter 3 has shown an interesting V_{TH} lowering compared to the High-Temperature Tunnel FETs. Furthermore, an on-current increase (at V_G = - 2.0 V) and, unfortunately, a significant off-current degradation (at V_G = - 1.0 V) were observed for different drain polarization conditions (V_D = - 0.9 V and - 0.5 V). The overall consequence of this effect is an undesired reduction of the I_{ON}/I_{OFF} ratio.

This problem arises when the low-temperature (< 650°C) SPER technique [1] is used to achieve activation of dopants in the source and drain regions. A considerable amount of defects are created at the interface between the amorphous region and the bottom of the SOI film (crystalline seed). Published results based on FDSOI devices with an extremely thin channel (T_{Si} = 6 nm) report the same leakage current for HT and LT processes [2]. The reason is that the End of Range (EOR) defects are in a high proportion located close to the BOX interface and they do not impact the drive current.

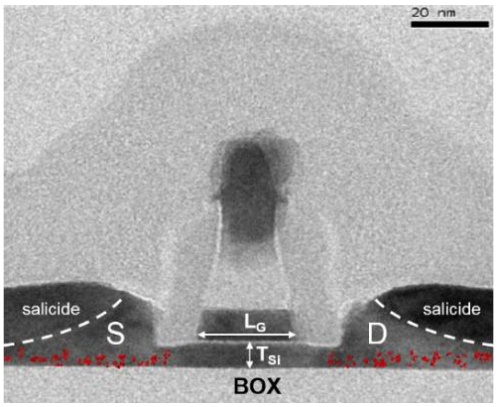

Figure 4.1. Cross-sectional TEM image of an FDSOI device (L_G = 27 nm, T_{Si} = 6 nm and T_{BOX} = 145 nm) with the superposition of the evolution of defects obtained by means of KMC simulations (red dots) [2].

In Figure 4.1 one can notice the presence of defects near the edges of the gate close to the source and drain regions even at T_{Si} = 6 nm. The presence of these defects suggests that in a TFET where current is generated by BTBT lateral tunneling, trap-assisted-tunneling (TAT) process will be involved, and will degrade the subthreshold slope. Furthermore, our TFETs were fabricated in a 11nm-thick silicon film, such that the EOR defects will be mainly located in the middle of the silicon film thickness, which increases the density of TAT defects. As a result, TAT will dominate over BTBT at low gate voltages, jeopardizing the possibility of obtaining a subthreshold swing below 60 mV/dec (as demonstrated in the previous chapter).

In order to assess whether the LT TFETs present a higher density of traps than the HT devices, due to the above-mentioned lower annealing process, this Chapter is dedicated to measuring interface states using the charge pumping method. This technique allows to

characterize a current which is proportional to the recombination of the electrons trapped in these states with holes. From the charge pumping current it is possible to calculate the average defect density near the source/channel junction where BTBT takes place, including the interface states at silicon/oxide interfaces (both gate oxide and BOX). Hopefully, charge pumping will be able to let us determine whether the density of traps and defects can be correlated with the on-current enhancement. In addition, low frequency noise analysis will allow us to carry out assessment of the quality of the junctions for TFETs with different annealing temperature; the results of this analysis indicate a higher density of defects at the source junction for devices made using the LT process.

4.2. Charge Pumping

4.2.1. Basic principle

The charge pumping method was demonstrated by Brugler and Jespers [3] in enhancement-mode MOSFETs. This technique consists in applying a periodic signal at the gate terminal (switching from inversion to accumulation mode and vice-versa), while keeping the source and drain short-circuited and reverse biased [4].

In the inversion mode for an N-type MOSFET (Figure 4.2a), electrons are attracted from the source and drain towards the channel, forming an inversion layer. In this phase all the interface states with energy lower than the Fermi level ($E_T < E_F$) will be filled with electrons. Next, when switching to the bottom level (negative value) of the pulse, the "non-trapped" minority carriers of the inversion layer are quickly collected by the source and drain. The negative voltage at the gate attracts holes from the bulk substrate, so these majority carriers will recombine with the electrons released from the traps with energy levels higher than the Fermi level ($E_T > E_F$) (Figure 4.2b). This recombination process induces a substrate current (charge pumping current), that is proportional to the average density of defects at the Si/SiO_2 interface and frequency [5]. The schematics shown in Figure 4.2 are only an overview; a more thorough explanation of the different currents flowing during one cycle of the gate pulse can be found in [4].

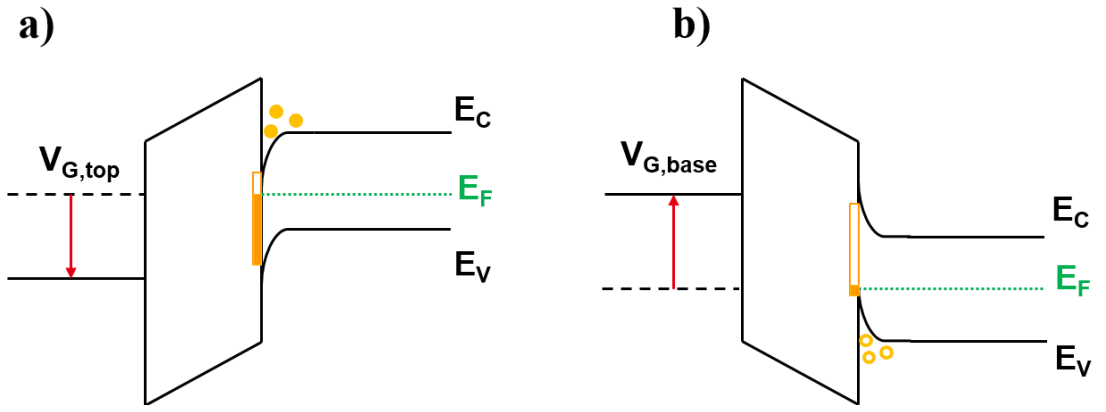

Figure 4.2. Energy band diagrams explaining the principle of the charge pumping method: (a) in inversion electrons from the source and drain are captured in the interface states (orange region). (b) In accumulation holes from the substrate recombine with the trapped electrons. This induces a substrate charge pumping current.

When the gate is pulsed at frequency *f*, the charge pumping current is given by [6]:

$$I_{CP} = q^2 f A \overline{N_{it}} \Delta\phi_S \qquad (4.1)$$

where *A* is the effective channel area of the transistor, $\overline{Nit}$ is the average density of defects and $\Delta\Phi_S$ is the surface potential range scanned within the bandgap. From equation (4.1), it is noticeable the charge pumping current is linearly proportional to frequency. Therefore, it is possible to determine the average density of interface states from the slope of the $I_{CP}(f)$ curve. Although the above equation was derived for bulk silicon MOSFETs, it can be also applied to gated p-i-n diodes [5], which lateral SOI TFETs essentially are.

4.2.2. Set up configuration in FDSOI TFETs

The charge pumping method requires the presence of majority and minority carriers to generate a current, which arises from the recombination of electrons and holes during the cycle of a pulse. In SOI layers the channel region is separated from the substrate by the BOX. In addition, the body region is thin and lightly doped (~ 10^{15} cm^{-3}), such that the amount of available majority carriers is very limited. Fortunately, in our FDSOI TFETs structures (P^+-N^--N^+) both types of carriers are available because the doping polarities in the source and drain regions are opposite. The terminals serve as reservoirs being able to supply instantly the demanded amount of electrons and holes.

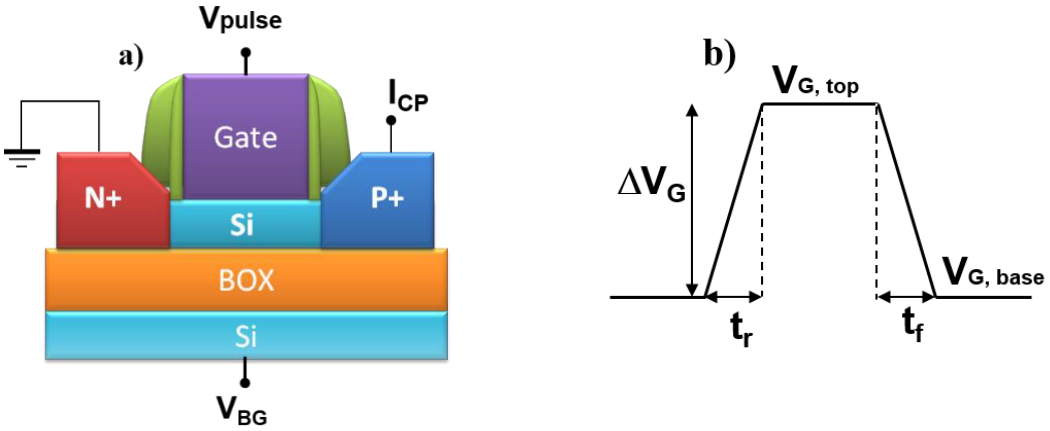

Figure 4.3. (a) Charge pumping method configuration in TFET structures. (b) "Square" pulses applied to the front-gate terminal to generate the I_{CP} current.

Figure 4.3a presents the configuration used in our Tunnel FET devices for charge pumping measurements. The N^+ region is grounded (or reverse biased) and a "square" pulse from a waveform generator is applied to the front gate terminal (Figure 4.3b). The charge pumping current is measured at the P^+ contact. In FDSOI devices it is possible to separately characterize the different contributions of density of defects at the channel top and bottom interfaces using back gate polarization.

The I_{CP} current has been measured by varying the pulse base level ($V_{G,base}$) from accumulation ($V_{G,base}$ = - 1.5 V) to inversion ($V_{G,base}$ = 0 V), while keeping the amplitude of the pulse constant (ΔV_G = 1.3 V). The rise and fall time of the pulse is 50 ns. Measurements were made for frequencies ranging from 200 kHz to 2000 kHz with a step of 200 kHz. Moreover, different back gate voltages were used to better determine the density of defects at top and bottom interfaces. Published results have already studied the influence of gate pulse

shape (triangular or rectangular) and pulse base level on the measured I_{CP} current [4]. Usually, studies based on charge pumping measurement for SOI gated PIN diodes have implemented square pulses [5]–[8].

Experimental results of charge pumping current versus the pulse base level ($V_{G,base}$) show a well-defined bell shape characteristic as in Figure 4.4a. This is explained by the position of the pulse with respect to the flat band voltage (V_{FB}) and threshold voltage (V_{TH}). Several stages are defined in Figure 4.4b:

1) Both top and base levels of the gate pulse are below the flat band voltage, which implies that the top channel surface is always in accumulation. The defects are always filled with holes (absence of electrons), and thus there is no CP current.

2) The pulse base level induces accumulation ($V_{G,base} < V_{FB}$) and the pulse top level induces weak inversion ($V_{G,top} < V_{TH}$). This mean that some defects will be filled with electrons and will recombine with holes, increasing the charge pumping current. The CP current increases steadily with base level voltage.

3) In this region, the pulse base level forms an accumulation channel ($V_{G,base} < V_{FB}$) and the top level voltage induces strong inversion ($V_{G,top} > V_{TH}$). In this state all the defects will be filled with electrons and holes at the top and bottom of the pulse, respectively. This bias condition generates the maximum charge pumping current.

4) Here, the pulse base level induces weak accumulation ($V_{G,base} > V_{FB}$) and the top level generates inversion ($V_{G,top} > V_{TH}$). So, all the traps will be filled with electrons but there will not be enough holes to recombine with all the “trapped” electrons. The charge pumping current now decreases with increasing base voltage.

5) Both pulse base and top level induce inversion. In this case the traps are constantly filled with electrons. These electrons are never released from the traps. Therefore, the I_{CP} current is negligible.

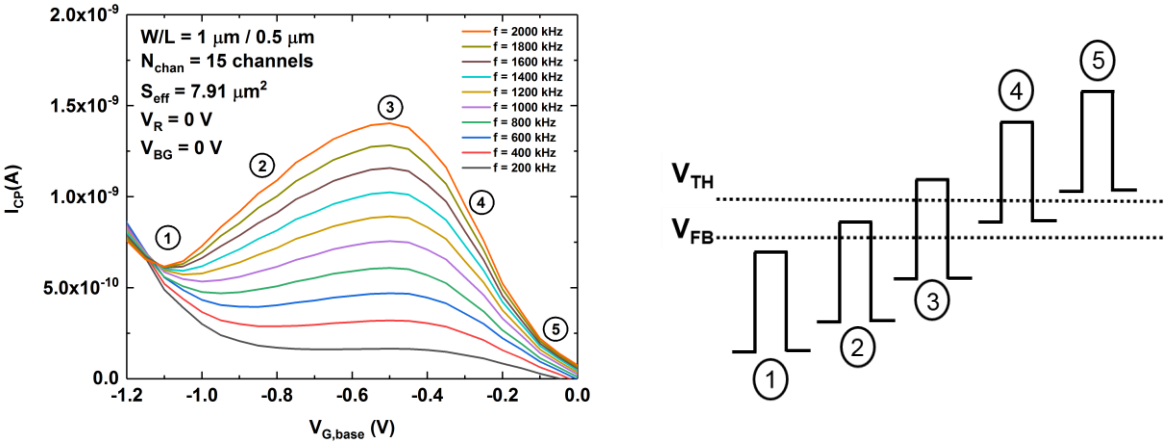

Figure 4.4. (a) $I_{CP}(V_{G,\,base})$ curves showing the recombination current measured at given pulse amplitude and for different frequencies. (b) Schematic of the gate pulse at different phases: in phase 3 it is obtained the maximum charge pumping current.

Now, obtaining the maximum charge pumping current for each frequency and plotting the results in Figure 4.5, we observe that the I_{CP} variation with frequency is linear. By means of a linear regression we determine the slope of the $I_{CP}(f)$ curve. Using equation (4.1) it is possible to determine the average density of defects $\overline{Nit}$. We have taken into account the fact that the energy range scanned within the bandgap ($q{\cdot}\Delta\Phi_S$) is approximately equal to 1 eV.

Our experimental results indicate that applying to the cathode a reverse bias (thus different from 0 V) is counterproductive and reduces the measured CP current. For example, when increasing V_R (to 0.1 V, 0.3 V and 0.5 V) the bias difference between gate and cathode is reduced. In particular, for V_R = + 0.5 V, the film top surface is almost depleted of electrons and the net recombination is severely degraded. Therefore, we have performed the charge pumping extractions at V_R = 0 V, to have the certainty that the electrons and holes are fully controlled by the gate pulse. This issue will be further explained in Section 4.3.

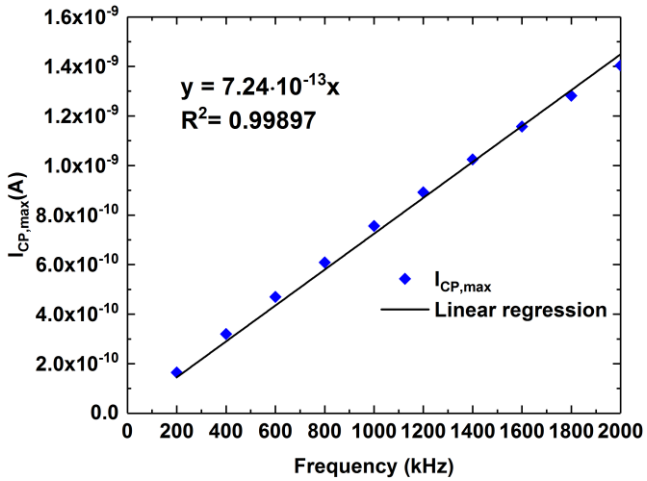

Figure 4.5. $I_{CP,\ max}$ for different frequencies. With a linear fit is obtained the slope of the data set, which allows to calculate the average density of defects.

4.2.3. Impact of back-gate voltage on charge pumping current

One of the advantages of charge pumping characterization in FDSOI structures is the possibility to determine the density of defects in the front and back interfaces separately. In thin films (< 50 nm), the top and bottom surfaces are very close to each other and therefore, carriers from the top region could be trapped in defects located at the bottom interface and eventually contribute in the charge pumping current during front-interface characterization. This implies that we cannot be certain that the I_{CP} current, measured when no back-gate voltage is applied (Figure 4.6a), is only due to the presence of defects at the gate oxide/channel interface.

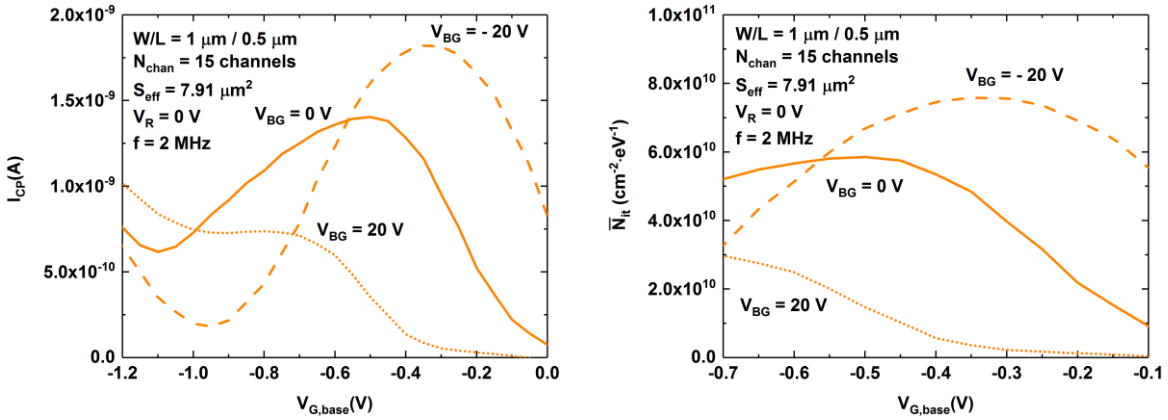

Figure 4.6. (a) Charge pumping current evolution with respect to the pulse base level at different back-gate voltages in a TFET (T_{Si} = 11 nm, T_{BOX} = 145 nm). (b) Evolution of the average density of defects, showing the relationship with the I_{CP} current.

To obtain accurate front-channel measurements we have to apply a proper back-gate voltage to the substrate underneath the BOX. In particular, for V_{BG} = - 20 V an accumulation layer of holes is formed at the bottom interface. This does not allow the front-gate pulse to induce trapping of electrons at the bottom interface. As a result, the contribution of the bottom traps to I_{CP} is significantly reduced. Note that, with a thicker T_{BOX} = 145 nm, back-gate voltages even lower than - 20 V are required to completely deactivate the back interface. In addition, the electrostatically doped P-type layer created at the bottom decreases the channel potential. This implies that a higher gate voltage must be applied to the front gate to generate an inversion layer, so the threshold voltage is increased. This is shown in Figure 4.6a, where a shift of the I_{CP} curve towards less negative values of the pulse base level for V_{BG} = - 20 V is observed. On the other hand, applying a back-gate voltage of 20 V generates a virtual N-type doping at the bottom interface. In that case (Figure 4.6a) we observe a decrease of the threshold voltage, which corresponds to a shift of the I_{CP} curve towards more negative values of $V_{G,base}$. Note that in this configuration the back interface is full of electrons which could be "trapped" by defects located at the front interface.

The influence of the substrate bias on the charge pumping behavior for SOI devices has been extensively investigated. In thicker films of 450 nm, Wouters *et al.* [9] reported that there was not a significant change in the $I_{CP}(V_{G,base})$ curves, regardless of the applied back-gate voltage. However, Ouisse *et al.* [5] reported that for SOI gated p-i-n diodes with a film thickness below 300 nm there was a clear variation of $I_{CP,max}$ with back-gate bias. When the back interface was in accumulation or inversion regime the density of traps at the bottom were deactivated and did not contribute to the charge pumping current. In depletion mode (V_{BG} = *0V*) an increase of the $I_{CP,max}$ peak was observed, unlike in the case of the 450 nm-thick film of Ref [9]. This additional charge pumping current arises because the back interface was also scanned by the pulse signal applied in the front gate. This behavior was confirmed in later publications with even thinner (100 nm) FDSOI MOSFETs [8].

Our TFETs have a much smaller film thickness (T_{Si} = 11 nm). A clear change of I_{CP} current maximum can be seen when back bias is changed. Specifically, there is an increase of the charge pumping current at V_{BG} = - 20 V, when the back interface is theoretically deactivated. In addition, a decrease of I_{CP} current is noticed for V_{BG} = 20 V. Furthermore, when zero back-gate voltage is applied, the front-gate pulse should cause a sweep of the back surface potential between accumulation and inversion and thus add a contribution of the

defects at the bottom of the channel to the CP current arising from the front-interface defects. In addition, a lower $I_{CP,max}$ is obtained in Figure 4.6a for V_{BG} = 20 V in comparison to V_{BG} = - 20 V case. Similar results have been also obtained for other FDSOI devices with T_{Si} = 7 nm and a T_{BOX} = 25 nm [10]. One possible explanation could be related with the fact that when applying a V_{BG} < 0, since the silicon film is very thin (T_{Si} = 11 nm), an extra depletion region is generated in the mid/bottom channel region coming from the back gate. Therefore, when pulsing the front gate, defects present in this region, and not only from the top interface, will participate in the recombination process (Figure 4.7).

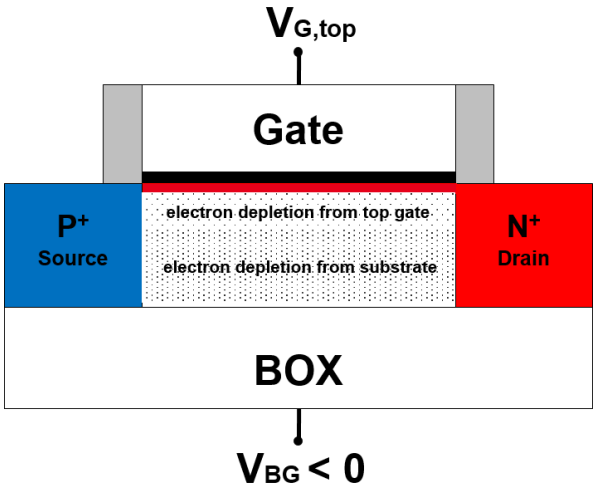

Figure 4.7. Cross section of the schematic TFET structure showing the depletion region generated by the pulse top level and the depletion due to the substrate bias. Defects in this region can trap electrons from the top inversion layer, increasing the charge pumping current.

To explain the physics behind these measurements, TCAD simulations were used, the results of which will be described in Section 4.3. There will be shown that the charge pumping current is limited by the concentration of carriers that are able to recombine. In other words, if the difference between electron and hole concentrations present in the film during a charge pumping cycle is significant, the recombination will be proportional to the lowest density of carriers available (either holes or electrons). This indicates that a balance between available holes and electrons concentrations is necessary to yield reliable charge pumping measurements. Figure 4.6b shows the average density of defects obtained at the laboratory for different back-gate voltages. We can notice the link between a higher charge pumping current at V_{BG} = - 20 V and a higher density of defects. The challenge consists in understanding the contributions of the density of defects located at various depths. Since a whole range of frequencies were used to characterize the devices, we used the slope of the $I_{CP,max}$ *(f)* curve to calculate N_{it}.

4.2.4. Density of interface states for LT and HT TFETs

In Tunnel FETs, the BTBT generation is located at the source junction, close to the gate oxide/silicon film interface. Therefore, here we present the average density of defects obtained with the charge pumping method at the front interface for a back gate voltage of - 20 V for both High-Temperature (HT) and Low-Temperature (LT) devices.

L_G = 0.5 µm; $V_{G,base}$ = - 0.65 V; ΔV_G = 1.3 V			HT (1050°C)	LT (650°C)
Width (µm)	N° channels	A_{eff} (µm^2)	N_{it} (cm^{-2}eV^{-1})	N_{it} (cm^{-2}eV^{-1})
1.0	15	7.91	$7.01 \cdot 10^{10}$	$1.50 \cdot 10^{11}$
0.5	30	8.33	$7.81 \cdot 10^{10}$	$8.83 \cdot 10^{11}$
0.2	50	6.38	$4.84 \cdot 10^{10}$	$7.28 \cdot 10^{10}$
0.12	70	6.13	$8.10 \cdot 10^{10}$	$1.15 \cdot 10^{11}$
0.10	75	5.81	$6.45 \cdot 10^{10}$	$1.13 \cdot 10^{11}$
0.08	75	5.06	$7.89 \cdot 10^{10}$	$5.11 \cdot 10^{10}$
0.07	75	4.69	$8.63 \cdot 10^{10}$	$3.96 \cdot 10^{11}$
0.06	75	4.31	$5.61 \cdot 10^{10}$	$1.41 \cdot 10^{11}$
0.055	75	4.13	$4.85 \cdot 10^{10}$	$9.69 \cdot 10^{10}$
0.05	75	3.94	$4.14 \cdot 10^{10}$	$4.28 \cdot 10^{11}$

Table 4.1. Average density of defects obtained at the front-interface for High-Temperature (HT) and Low-Temperature (LT) processes. In general LT TFETs exhibit a higher density of defects than HT TFETs. A_{eff} is the effective area of the transistor.

The LT TFETs characterized in Chapter 3 with a gate length of 500 nm and 1 µm width show a higher on-current and off-current than their HT counterparts. The hypothesis we made tries to attribute this current enhancement to TAT due to a higher presence of traps located in the semiconductor-insulator interfaces or in the bulk of the semiconductor, resulting in a generation current that degrades the subthreshold slope. The average density of defects listed in Table 4.1 for the LT TFETs is $1.5 \cdot 10^{11}$ cm$^{-2} \cdot$eV^{-1}, while it is $7.0 \cdot 10^{10}$ cm$^{-2} \cdot$eV^{-1} for HT TFETs. These results suggest a higher density of traps in the low-temperature TFETs, regardless of the applied back-gate bias (Figure 4.8). Other geometries also exhibit a higher density of defects at the front interface in LT TFETs than in HT devices.

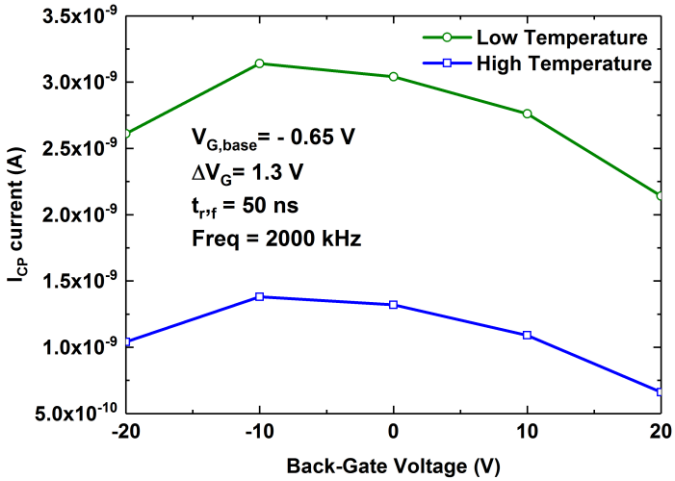

Figure 4.8. $I_{CP}(V_{BG})$ for HT & LT TFETs at $V_{G,base}$ = - 0.65 V. I_{CP} current for LT process is higher for all V_{BG} with respect to HT. This implies a higher density of defects in LT TFETs.

4.3. Charge pumping: Density of carriers and I_{CP} current

4.3.1. Impact of back-gate voltage on density of carriers

We have performed a TCAD study based on the simulation of the carrier density at the top and back interface of the body for different applied back-gate voltages. The objective is to determine if there is some correlation between the experimental charge pumping current

(Figure 4.8) and the concentration of carriers. To generate an I_{CP} current both types of carriers need to be present in order to recombine. A very low concentration of electrons at an interface means that traps at the interface will be empty of electrons and electron-hole recombination will not be possible. Conversely, a reduced concentration of holes, even if traps are filled with electrons, will not generate a significant I_{CP} current. For the simulation deck we have used the same geometry as in Chapter 3, but we have simplified the junction doping profiles: we used overlapped junctions with standard abruptness for HT devices and underlapped abrupt junctions for the LT TFETs. In CP current simulations, the junctions are located at the gate edge. The pulse gate is simulated by two different voltage conditions: the pulse base level is -0.65 V and the top level is + 0.65 V. These are the values used for the measurements reported in Table 4.1.

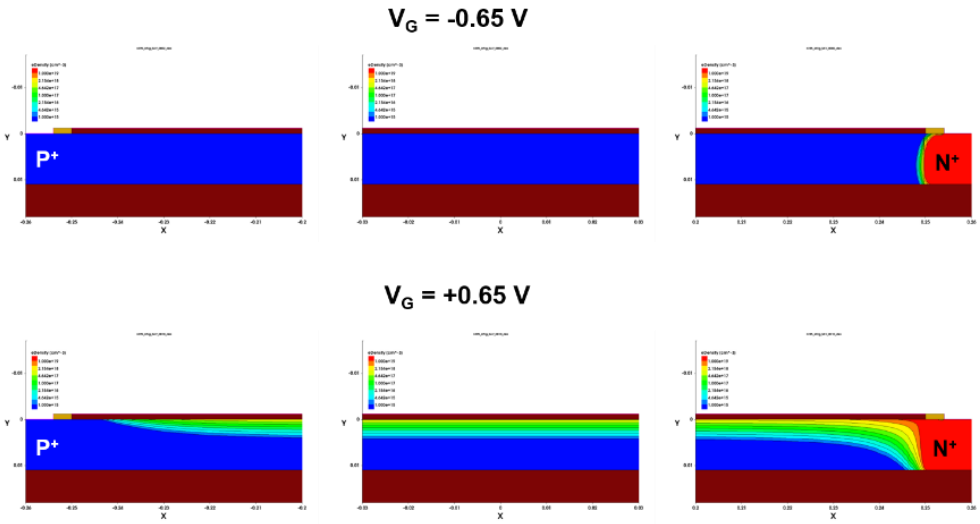

Figure 4.9. Electron density in different regions of the TFET structure (anode, channel and cathode): (top) at pulse base level the whole film thick is depleted of electrons; (bottom) at pulse top level the electrons are located at the top-interface (V_R = 0 V and V_{BG} = - 20 V).

Figure 4.9 shows the 2D mapping of the electron density across the whole silicon film thickness, and in different regions of the TFET structure for a back-gate voltage of - 20 V. When the gate is biased at the pulse base level, the channel is completely depleted of electrons (concentration around 10^{15} cm^{-3}). Switching to the top pulse level, we observe that an inversion layer is created at the front interface, while the back interface is depleted of electrons due to the applied back gate voltage. As for the hole density (Figure 4.10) at pulse base level, two layers of holes are formed at the channel interfaces. During the rising edge of the pulse, holes are collected progressively by the P^+ region keeping the channel depleted of holes. Now, if we consider both mechanisms at the same time, during the falling edge of the pulse the concentration of electrons that could be trapped by defects at the back interface is at best equal to 10^{15} cm^{-3}. Although, the concentration of holes is four orders of magnitude higher, the recombination at the back-interface is negligible because it is proportional to the lowest concentration of either carriers (electrons in this case). This indicates that traps at the back interface are in average always empty of electrons and the contribution of that interface to the I_{CP} current is low.

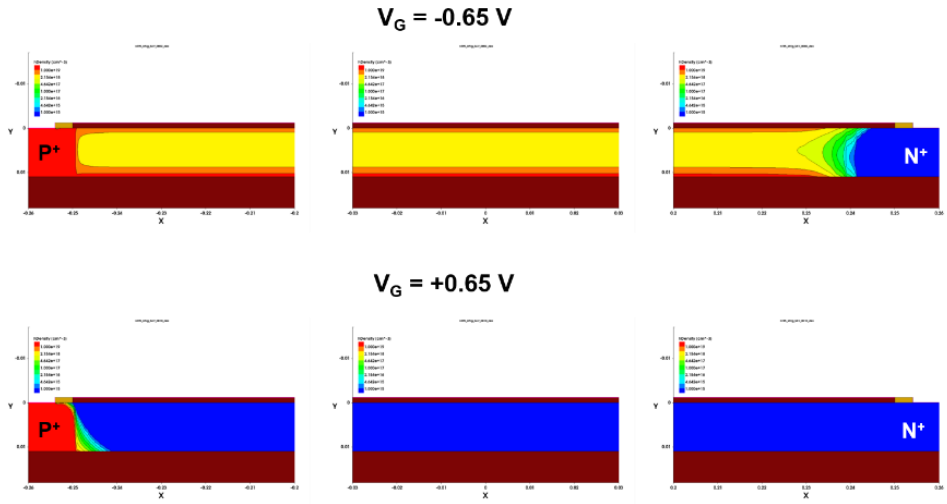

Figure 4.10. Hole density in different regions of the TFET structure (anode, channel and cathode): (top) at pulse base level front and back interface are filled with holes; (bottom) at pulse top level the channel is depleted of holes which are swept into the P^+ region (V_R = 0 V and V_{BG} = - 20 V).

At V_{BG} = + 20 V (Figure 4.11), not only the top interface, but also the back interface is always filled with electrons at the pulse top level (V_G = 0.65 V). However, when switching the gate voltage to the pulse base level (V_G = - 0.65 V), one can notice a complete depletion of electrons in the whole channel region.

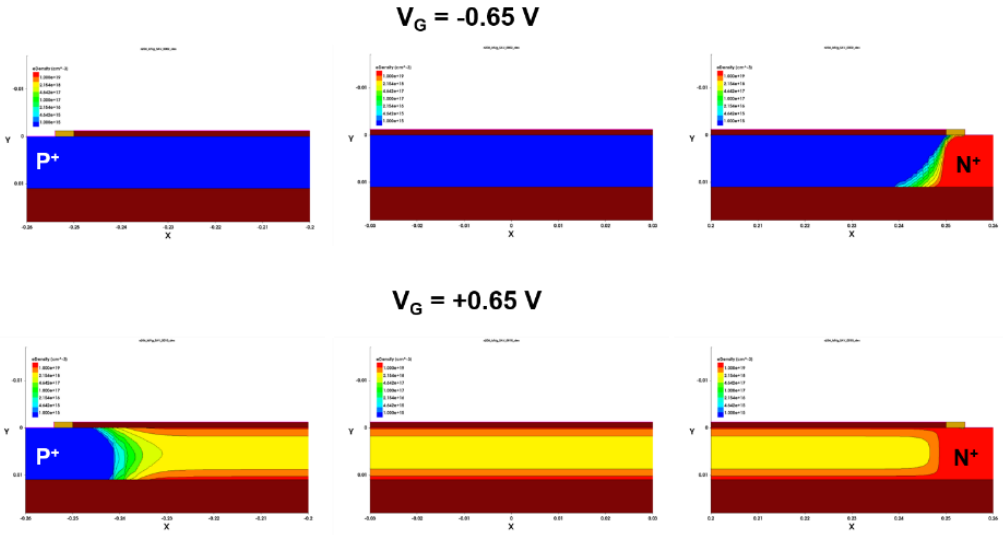

Figure 4.11. Electron density in different regions of the TFET structure (anode, channel and cathode): (top) at pulse base level the whole film thick is depleted of electrons; (bottom) at pulse top level the electrons are located at both top and back-interface (V_R = 0 V and V_{BG} = + 20 V).

Regarding the hole density at V_{BG} = + 20 V (Figure 4.12), an accumulation layer of holes is created at the top interface at the pulse base level. In this configuration recombination with electrons is low, basically because the channel is depleted of electrons. When switching to the pulse top level, the hole layer is collected by the P^+ region, and the concentration of remaining holes in the channel is very low (10^{15} cm^{-3}) in comparison to the electron concentration. This indicates that the recombination at the bottom is unlikely, because there are not enough holes. As a result, the contribution of the back interface to the I_{CP} current is not significant, due to the impossibility to scan the entire band gap at the back interface using CP pulses applied to the front gate.

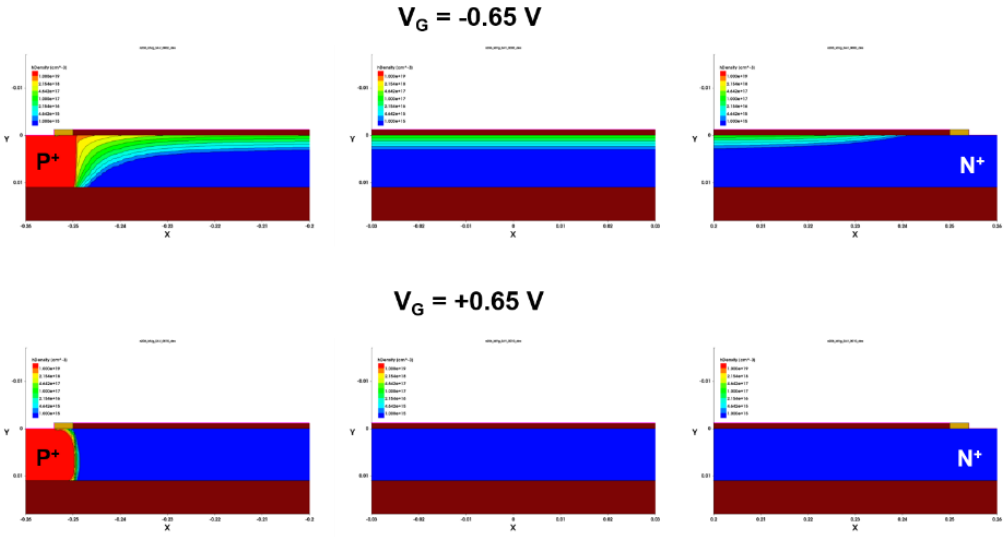

Figure 4.12. Hole density in different regions of the TFET structure (anode, channel and cathode): (top) at pulse base level only the front interface is filled with holes; (bottom) at pulse top level the channel is depleted of holes which are swept into the P^+ region (V_R = 0 V and V_{BG} = + 20 V).

The concentrations of electrons at the silicon/BOX interface are more balanced with respect to the front interface only when a zero back gate voltage is applied (Figure 4.13). For the pulse top level, there is an inversion layer of electrons at the top surface, but also there are a significant concentration of electrons at the mid-channel and back interface, respectively. At the pulse base level the device is completely depleted of electrons across the whole channel thickness.

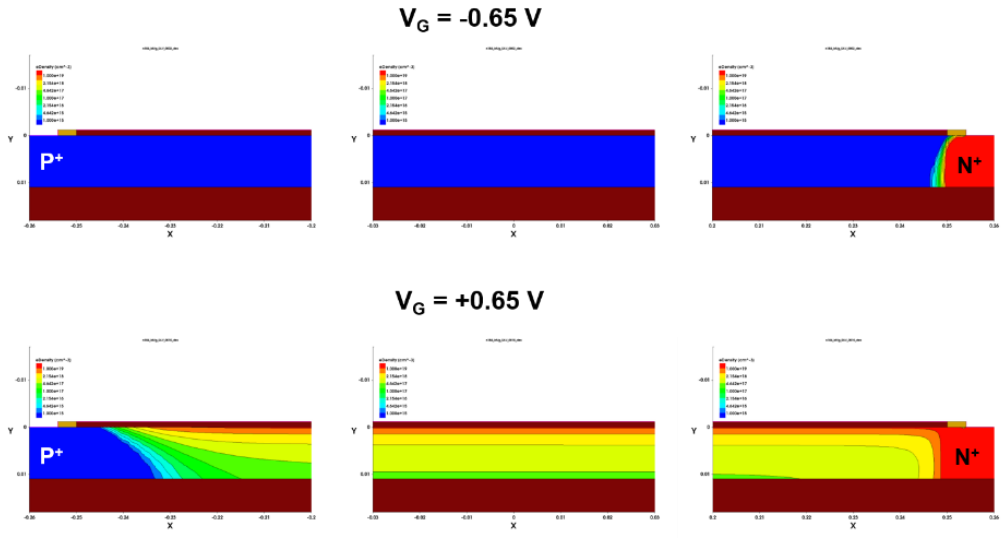

Figure 4.13. Electron density in different regions of the TFET structure (anode, channel and cathode): (top) at pulse base level the whole film thick is depleted of electrons; (bottom) at pulse top level electrons are available in the whole channel region (V_R = 0 V and V_{BG} = 0 V).

The hole density for V_{BG} = 0 V (Figure 4.14), shows the exact opposite behavior to that of the electron density: at the pulse base level, an accumulation layer of holes is created at the top interface, but there also an important concentration of holes in the rest of the channel region. When switching to the top level, holes are collected by the top P channel and there is only a low hole concentration of 10^{15} cm^{-3}. Left in the bulk of the channel region.

Comparing both figures, it is clear that for this bias configuration (V_{BG} = 0 V) and when the square-wave periodic signal applied at the gate terminal switches reciprocally, the entire silicon film can be repeatedly swept from inversion to accumulation and thus, participate to the charge pumping current. On the contrary, when a back gate polarization is applied the front gate cannot fully scan the bandgap at back interface and, thus I_{CP} generation only arises from electron and hole recombination at the top interface.

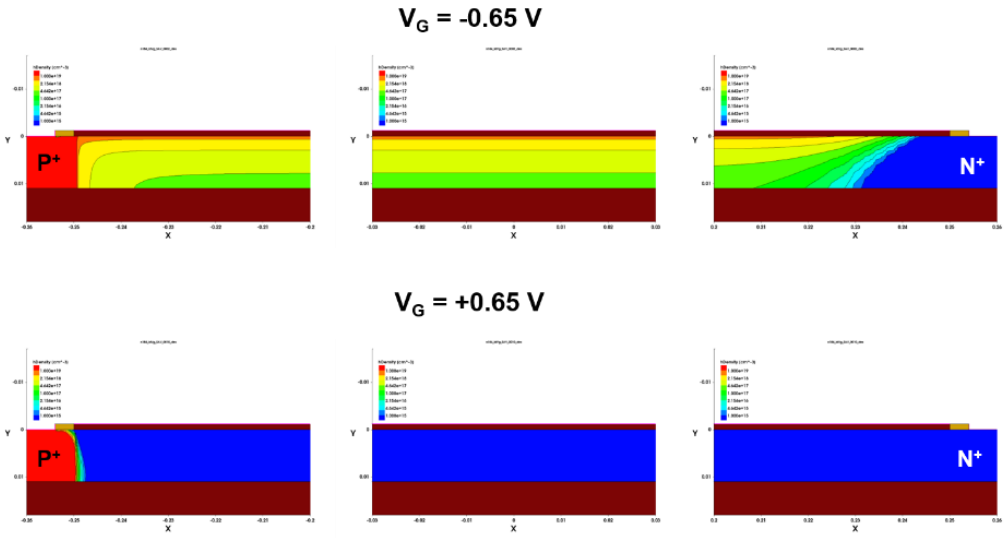

Figure 4.14. Hole density in different regions of the TFET structure (anode, channel and cathode): (top) at pulse base level the whole film thick is depleted of electrons; (bottom) at pulse top level electrons are available in the whole channel region (V_R = 0 V and V_{BG} = 0 V).

The TCAD simulations yield the carrier concentrations at the top and bottom interfaces (to be more precise, at a 0.5 nm distance from the front and back interfaces). We assume that charge pumping current is proportional to the minimum carrier concentration. Moreover, we consider that concentrations lower than 10^{15} cm^{-3} in a top/bottom channel region is too low to significantly contribute to I_{CP} current.

V_{BG} (V)	V_G (V)	Top h (cm^{-3})	Top e (cm^{-3})	Bottom h (cm^{-3})	Bottom e (cm^{-3})	Rec. conc. at Top (cm^{-3})	Rec. conc. at Bottom (cm^{-3})	Sum of e contrib. (cm^{-3})	Sum of h contrib. (cm^{-3})
- 20	-0.65	**$4.6\cdot10^{18}$**	0	**$1.3\cdot10^{19}$**	0	$6.2\cdot10^{17}$	**$1.4\cdot10^{10}$**		$1.8\cdot10^{19}$
	0.65	0	**$6.2\cdot10^{17}$**	$1.1\cdot10^{9}$	**$1.4\cdot10^{10}$**			$6.2\cdot10^{17}$	
0	-0.65	**$4.0\cdot10^{18}$**	0	**$3.6\cdot10^{17}$**	0	$4.0\cdot10^{18}$	**$3.6\cdot10^{17}$**		$4.4\cdot10^{18}$
	0.65	0	**$7.5\cdot10^{18}$**	0	**$4.3\cdot10^{17}$**			$7.9\cdot10^{18}$	
20	-0.65	**$7.4\cdot10^{16}$**	0	**$1.6\cdot10^{9}$**	$8.6\cdot10^{9}$	$7.4\cdot10^{16}$	**$1.6\cdot10^{9}$**		$7.4\cdot10^{16}$
	0.65	0	**$8.2\cdot10^{18}$**	0	**$1.3\cdot10^{19}$**			$2.1\cdot10^{18}$	

Table 4.2. Concentration of carriers obtained at the top and back interfaces. Two cases are studied: when only the top contribution is taken into account and when both top and bottom contributions are considered.

The variation of CP current depends on the concentration of electrons and holes available for recombination at the front and back interfaces. Results from Table 4.2 confirm that either one of these concentrations decreases when the back-gate voltage is more negative (fewer electrons) or more positive (fewer holes), not only at the back but also at the top interface. The recombination concentrations at the top and at the bottom (blue columns) are obtained considering that the recombined electron/hole pairs from top and bottom are isolated from

each other and there is not possible contribution from recombination between carriers from opposite interfaces (*i.e.*: electrons from top interface and holes from bottom interface, or reciprocally; black arrows for top interface). Analyzing the bottom region separately from the top, one can notice that when applying a back-gate bias, the total amount of recombined carriers is much lower than 10^{15} cm^{-3} (red arrows), which suggests that the back interface is deactivated. However, at V_{BG} = 0 V, the hole and electron concentration have the same order of magnitude (~ 10^{17} cm^{-3}, green arrow), indicating that the back interface will contribute to the I_{CP} current. Figure 4.15 shows the results of TCAD simulations of the minority carriers (which limit the recombination rate, and, therefore, set the CP current) for different values of back-gate voltages at $V_{G,base}$ = - 0.65 V. This curve shape of the carrier concentration is the same as the ones obtained for the experimental charge pumping measurements in Figure 4.8 and explains the recombination mechanism. The results match with has been previously explained regarding the impact of the back gate voltage in experimental data Furthermore, it shows that the traps at the back interface have negligible contribution to the (front-pulsed) CP current.

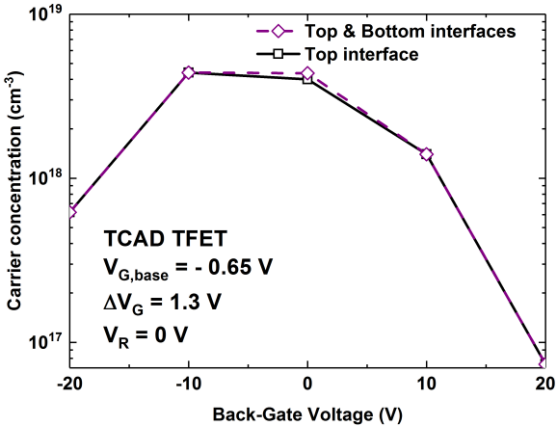

Figure 4.15. Simulation of carrier concentration for different V_{BG} at $V_{G,base}$ = - 0.65 V. No remarkable difference when only the top concentration is considered, with respect to the top and bottom concentration contributions.

4.3.2. Extraction of defect density at different pulse base levels

The average defect density extracted for various pulse base levels by different methods serves as an additional evidence of the close relationship between experiments and simulations.

- Firstly, we consider the experimental value obtained from laboratory measurements for a frequency of 2 MHz (HT/LT CP meas).

- Secondly, from the slope calculation of the $I_{CP,max}(f)$ curve and using equation (4.1) the average N_{it} is extracted from experimental results (HT/LT slope calculation).

- Finally, using again equation (4.1) with the I_{CP} current measured at a given pulse base level and frequency and with the effective gate voltage scanning the entire bandgap at the top interface (at 0.5 nm below the front gate), the trap density can be extracted from simulations (HT/LT I_{CP} simulated).

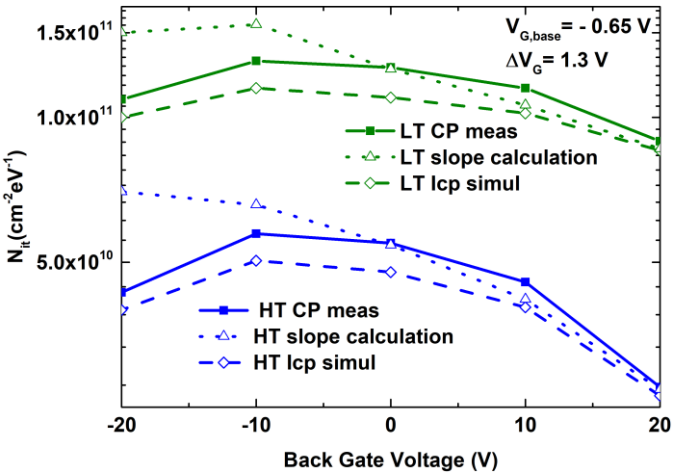

Figure 4.16. Density of traps in HT/LT TFETs obtained using different methods for $V_{G,base}$ = - 0.65 V. CP meas (experimental); "slope" technique (I_{CPmax} ($V_{G,base}$) curves) and I_{CP} simul (simulation). In all cases density of traps is higher in LT TFETs than HT TFETs.

A comparison of the average defect density at $V_{G,base}$ = - 0.65 V obtained by the previous methods (Figure 4.16) yields similar results for $V_{BG} \geq 0$. However, when $V_{BG} < 0$ the experimentally measured and the simulated N_{it} values are underestimated because the front interface is not fully scanned from accumulation to inversion. The "slope calculation" technique uses a wider gate voltage scan that ensures full bandgap scanning at the front interface, which yields a larger charge pumping current than the two other techniques [5]. All methods, however, agree on a higher N_{it} for Low-Temperature devices than for High-Temperature TFETs. This study was repeated for different pulse base gate levels while keeping the pulse amplitude constant, to further explore if our interpretation of the results is still valid.

4.3.2.1 Pulse gate base level of - 0.35 V

From experimental measurements in Figure 4.17a, we observe an increase of the charge pumping current for negative values of the back gate voltage in comparison with positive bias. The reason is that for $V_{BG} < 0$, the I_{CP} peak is shifted towards less negative values of the pulse base level. Therefore, for $V_{BG} > 0$, the I_{CP} peak is shifted towards more negative values of $V_{G,base}$. The simulated carrier concentration (Figure 4.17b) exhibits the same trend. In addition, the contribution of the back-interface carriers is not negligible for $V_{BG} < 0$. Since the gate amplitude is kept constant at 1.3 V, the gate pulse switches from - 0.35 V to 0.95 V. This implies that at the pulse base level holes are in weak accumulation, while at the top level of the pulse electrons are in strong inversion. The electron density obtained from TCAD 2D mapping confirms that electrons at the front-interface are in much higher concentration than holes (in a range of 3-5 orders of magnitude higher, depending of the back gate voltage). So, the charge pumping current will be limited by the minor carrier concentration (in this case holes). When a negative back gate voltage is applied and only the top-interface is considered, there are more holes in the channel region at the pulse base level. Therefore the carrier concentration that participates to the recombination process is increased (black line in Figure 4.17b).

The back interface does not have a significant impact on CP current for $V_{BG} > 0$, because the hole density is not sufficient. However, for $V_{BG} < 0$ the increase of the hole concentration

at the back interface is higher, so the electron and hole concentrations are more balanced. This generates a greater number of carriers that can be involved in the recombination process (purple line in Figure 4.17b).

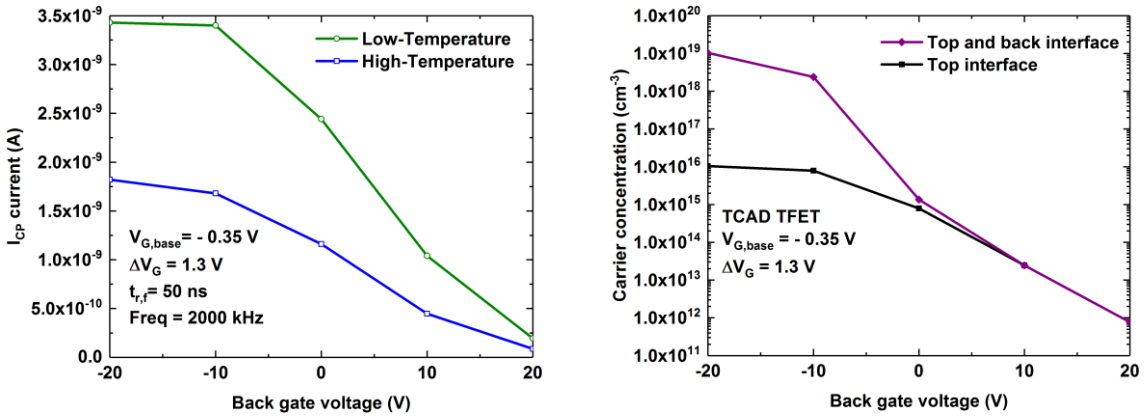

Figure 4.17. (a) Experimental I_{CP} (V_{BG}) curves for HT and LT TFET at $V_{G,base}$ = - 0.35 V showing a higher I_{CP} current for LT than HT. (b) Simulated carrier concentration for different back gate voltages.

The calculation of the average defect density in Figure 4.18 shows a good match between the different methods used for negative back gate bias. However, when a positive back gate voltage is applied there is a significant difference between the result obtained from the slope calculation and the other methods. Density of defects calculated using the slope is always carried out at $I_{CP,max}$, but for the others methods it is done for the charge pumping current obtained at $V_{G,base}$ = - 0.35 V. Therefore, for V_{BG} < 0, the $I_{CP,max}$ is close to the pulse base level explaining why similar average density of defects are obtained. On the other hand, for V_{BG} > 0 the $I_{CP,max}$ occurs format values lower than $V_{G,base}$ = - 0.65V (see Figure 4.6) and I_{CP} current does not correspond to a full scan of the bandgap. As a consequence, the experimental and simulated N_{it} values are underestimated for V_{BG} > 0.

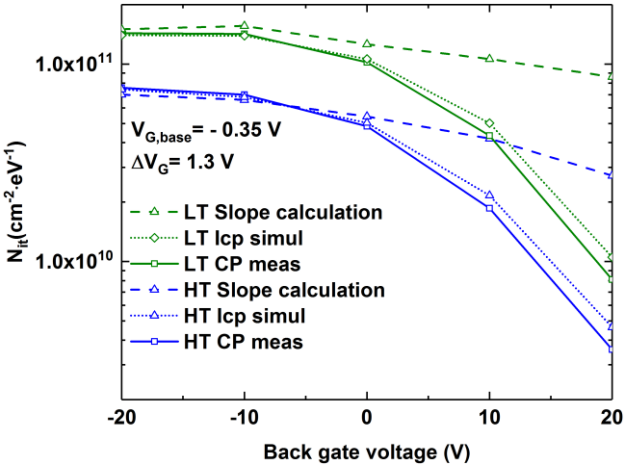

Figure 4.18. Density of traps in HT/LT TFETs obtained using different methods at $V_{G,base}$ = - 0.35 V. In all cases higher density of traps is obtained for LT TFETs.

4.3.2.2 Pulse gate base level of - 0.85 V

When the charge pumping current is measured for a pulse base level of - 0.85 V, we observe the opposite behavior to the case with $V_{G,base}$ = - 0.35 V. When a positive back gate voltage is applied, the $I_{CP,max}$ is shifted towards more negative values of $V_{G,base}$. This explains

why the measured charge pumping is higher in Figure 4.19a. On the contrary, for $V_{BG} < 0$, $I_{CP,max}$ is shifted towards less negative values of $V_{G,base}$ and at - 0.85 V the maximum charge pumping current is not reached.

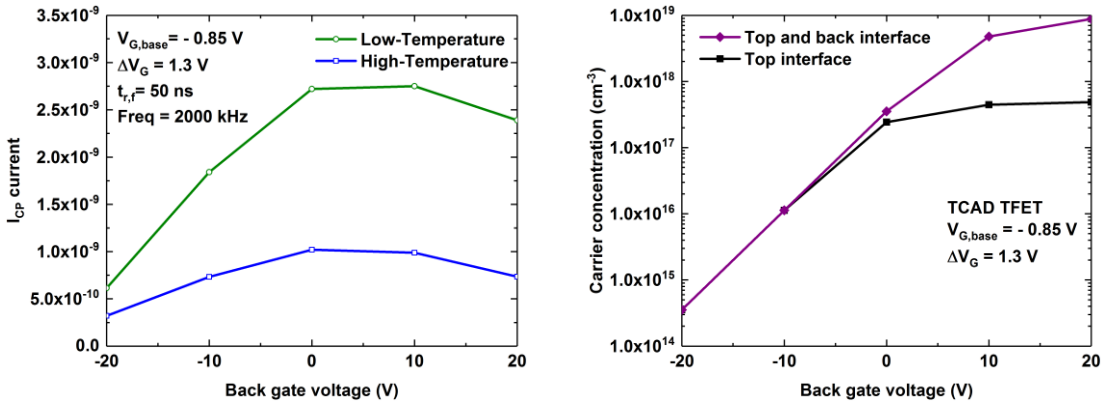

Figure 4.19. (a) Experimental I_{CP} (V_{BG}) curves for HT and LT TFET at $V_{G,base}$ = - 0.85 V showing a higher I_{CP} current for LT than HT. (b) Simulated carrier concentration for different back gate voltages.

Figure 4.19b represents the simulation of carrier concentration and the results obtained are consistent with the experimental values of the charge pumping current. At $V_{G,base}$ = - 0.85 V the top interface is in strong accumulation of holes, while at pulse top level (0.45 V) the top interface is in weak inversion of electrons. Therefore, the carrier concentration that participates in the recombination process is controlled by the electrons, because they are fewer. Applying a negative back gate voltage increases the threshold voltage, and since the amplitude of the pulse is constant, the concentration of electrons is reduced with respect to the case where no back bias is applied. On the other hand, for a positive back gate voltage the threshold voltage is reduced and for $V_{G,top}$ the density of electrons increases and so does the carrier concentration that participates in recombination when only the top interface is considered.

When the back interface is also taken into account and $V_{BG} < 0$, a great number of holes are available, however the number of electrons is not significantly enhanced. This explains why the back gate does not provide an increase of the density of carriers that participate in the recombination mechanism, and thus in the CP current. For $V_{BG} > 0$, the concentration of electrons is increased and is more balanced with the concentration of holes, so the carrier density is increased (Figure 4.19b).

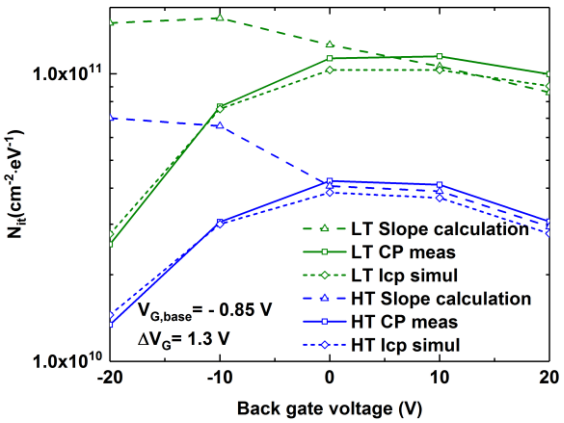

Figure 4.20. Density of traps in HT/LT TFETs obtained using different methods at $V_{G,base}$ = - 0.85 V. In all cases higher density of traps is obtained for LT TFETs.

A comparison of the different methods used to calculate the average density of defects shows a good match for positive values of back gate bias (Figure 4.20) because $I_{CP,max}$ is close to the I_{CP} values measured at $V_{G,base}$ = - 0.85 V for the experimentally measured and the simulated N_{it} values. Unfortunately, when the back gate polarization is negative the measured charge pumping current is significantly lower than the $I_{CP,max}$. The difference between these methods and the slope calculation is explained by the difference of energy range that is scanned in the bandgap, leading to underestimation of the average N_{it}. In all cases, however, the LT TFET consistently exhibits a higher density of defects than the HT TFET by an approximate factor of three.

4.4. Low-Frequency Noise analysis

The objective of our low frequency noise (LFN) analysis is to provide more evidence not only about the distribution of traps at the top interface (done via charge pumping method), but also about the source/drain junction defect density difference between LT devices and their HT counterparts.

4.4.1. Impact of the process temperature

Figure 4.21a shows the average $I_D(V_G)$ curves for LT and HT TFETs measured on 74 dies. The results are consistent with the ones obtained in Chapter 3, where only 14 dies were tested. This time, we have also performed electrical characterization on MOSFETs (10 dies) fabricated in the same batch (Figure 4.21b). The I-V characteristics of TFETs and MOSFETs present a different shift between High-Temperature and Low-Temperature process. Specifically, in MOSFETs only a small threshold voltage shift is observed (~ 0.1V) due to the impact of different thermal budgets on the Equivalent Oxide Thickness (EOT) [11]. However, a much larger shift is seen in TFETs (~ 0.3 V), which cannot be explained only by the EOT change. In fact, it can be attributed to a combination of TAT current increase and the presence of a more abrupt tunnel junction region due to lower dopant diffusion in the LT devices. The presence of a higher defect density (N_{it}) at the top interface for TFETs with LT process has been already confirmed via charge pumping method. Now, LFN measurements are used to further probe the differences between LT and HT devices [12].

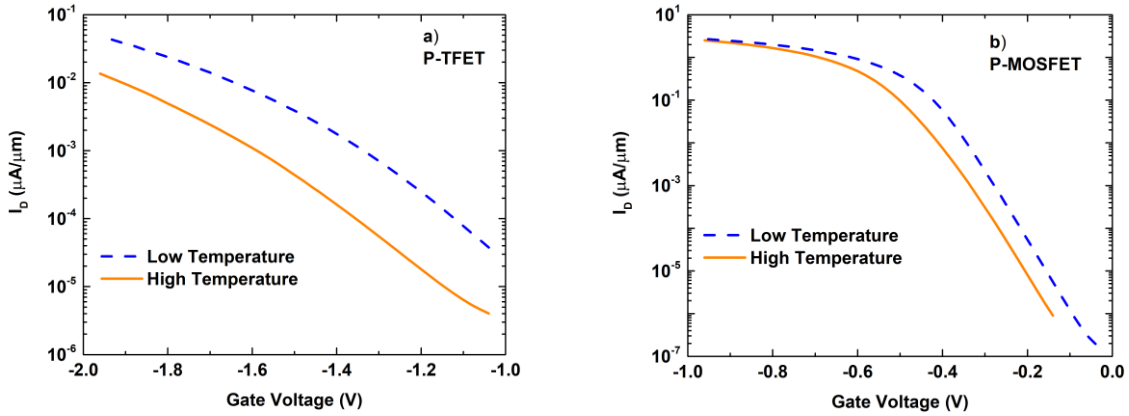

Figure 4.21. Comparison of drain current characteristics between: (a) P-TFET (74 dies average) and (b) P-MOSFET (10 dies average) drain current density characteristics fabricated on the same wafers (HT and LT). L_G = 1 µm, MOSFET V_{DS} = - 30 mV, TFET V_{DS} = - 0.9 V.

One of the most important parameters to characterize noise is the input-referred gate voltage ($S_{Vg} = S_{id}/g_m^2$), as it translates all the current fluctuations into equivalent gate voltage variations. When S_{Vg} is increasing with V_G, it is an indicator of high series resistance noise, related to the defect presence in the source and drain junctions. For the same gate voltage (V_G = - 0.65 V) where N_{it} was extracted using the charge pumping method, the average input-referred gate voltage noise spectrum (Figure 4.22) is higher for LT than for HT MOSFETs in all the range of frequencies. Therefore, this reveals a higher density of traps either in the oxide, or at the junctions for LT process. For MOSFETs, as they are based on drift-diffusion mechanisms (thermionic carrier injection through the potential barrier), the higher density of

traps it is not severely affecting the performance as seen in Figure 4.21a. In strong accumulation of holes (V_G < - 0.7 V) the drain current converges to the same values for LT and HT.

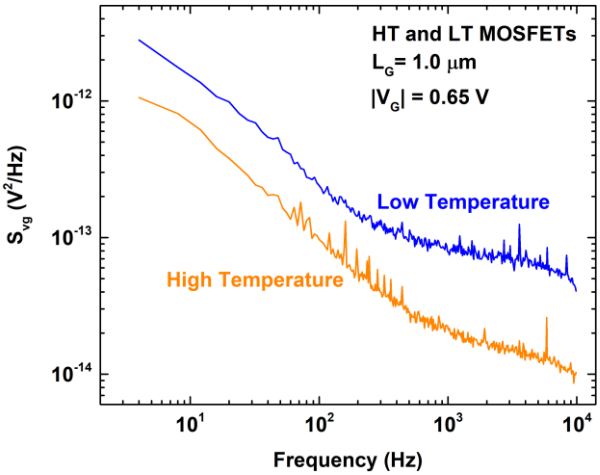

Figure 4.22. Input-referred gate-voltage noise spectra of p-channel HT and LT MOSFETs for a gate polarization of $|V_G|$ = 0.65 V.

This experimental study of LFN has been also performed for TFETs fabricated on the same wafers as MOSFETs. The comparison between the average (74 dies) LFN levels of HT and LT TFETs (Figure 4.23) at 10 Hz shows not only a higher noise level for LT devices, but also a rise with gate voltage. This is typical for a high density of defects at the source and drain regions, leading to higher series resistance noise [12]. On the contrary, S_{Vg} is more or less constant with V_G for HT devices, revealing a negligible junction defect density. These results confirm that the lower annealing temperature used after source and drain implantations in LT TFETs (600 °C), gives rise to a higher density of traps in the vicinity of the junctions, as well as a sharper junction profile (reduced diffusion into the channel region compared to high-temperature process). These two features are responsible for the increase of both on-current and off-current in LT devices, as well as the increase in noise levels. Therefore, not only interband tunneling is involved in the enhancement of the current compared to HT TFETs (Figure 4.21a), but also TAT. In fact, TAT is the main contribution for low gate voltages.

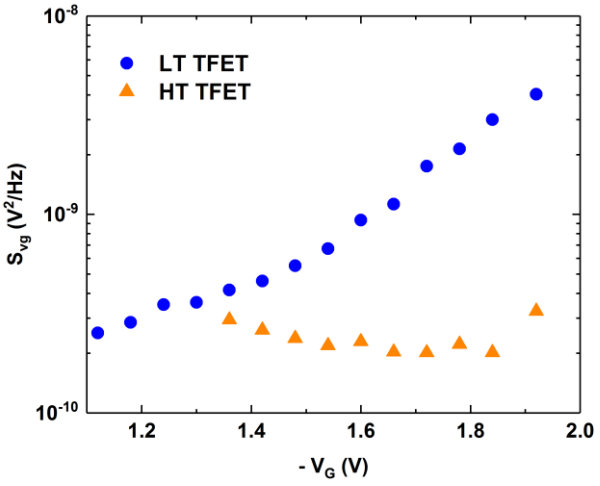

Figure 4.23. Comparison of input-referred gate voltage noise (S_{Vg}) versus gate voltage at 10 Hz between HT and LT P-type TFETs.

Figure 4.24 illustrates schematically the increase of on-current and off-current with the increase of the trap density. The higher is the density of traps in the junction, the more "stepping stones" channels are available for TAT. Using the hypothesis that each trap filled with an electron generates a unit of noise, the higher the trap density, the higher the noise, as it is observed by comparing the noise between LT and HT devices (Figure 4.23).

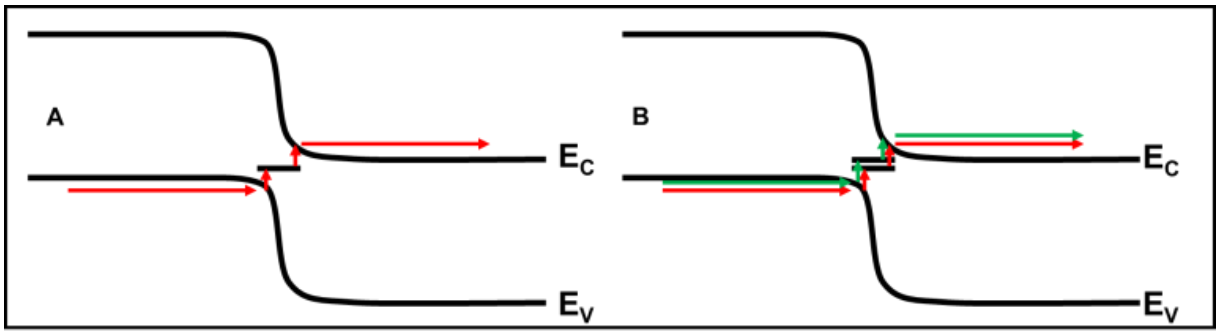

Figure 4.24. Schematic of trap-assisted tunneling (TAT) showing the increase of the current and noise with trap density. A: one trap; B: two traps.

In Figure 4.25, the area-normalized noise level in TFETs and MOSFETs, where $A_{eff} = N_{ch} \times (W_{mask} - \Delta W + 2.t_{Si}) \times L$ is plotted versus the drain current density. As one can observe, the TFET noise level is almost two orders of magnitude higher than the MOSFET noise for the same technology wafers. This is consistent with the different noise sources in the two types of transport mechanisms: in MOSFETs the noise is a combination of fluctuations in the carrier number due to trapping/de-trapping in slow oxide traps and in the mobility of the channel [13]. In Tunnel FETs, on the other hand, the noise is related to fluctuations in the effective electric field or the TAT rate [14]. This implies a fundamental difference, because in TFETs the tunneling region for which the electric field plays a significant role (Figure 4.24) is located in a distance of approximately 10 nm from the source junction [15], even if the gate length of the device is as long as 1 µm. And since this is not accounted for in A_{eff}, there are seemingly higher LFN levels in the TFETs, because of to the reciprocal dependence of noise on the device area. Moreover, this highlights how important it is to fabricate good-quality junctions and use a defect-free film body, especially for TFETs, where the impact of defects in the tunnel junction area severely affects performance.

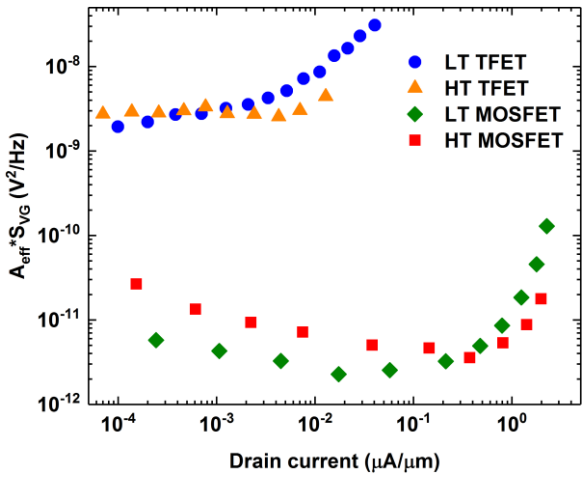

Figure 4.25. Surface-normalized input-referred gate voltage noise versus gate voltage for both HT/LT TFETs and MOSFETs.

In order to provide more evidence for the larger defect density in the junctions of TFETs fabricated with a LT process, we have also analyzed the variability in the drain current noise spectra. Figure 4.26a shows the evolution of the normalized drain current noise with respect to the frequency for a HT process over 50 dies. The logarithmic mean clearly shows a *1/f* average behavior (a change of one decade of magnitude causes one decade shift of the drain current noise), which is an indication of a uniform distribution of traps, typical for oxide defects [16]. On the contrary, the logarithmic mean of the drain current noise (over 74 dies) for LT TFETs in Figure 4.26b shows a non-*1/f* behavior. This suggests a non-uniform distribution of traps in the oxide region, or/and the presence of additional defects, for example in the junctions. All these analyses prove that the lower passivation achieved with LT annealing is the main cause of a higher density of defects at the junctions and thus, higher levels of LFN in all the studied cases.

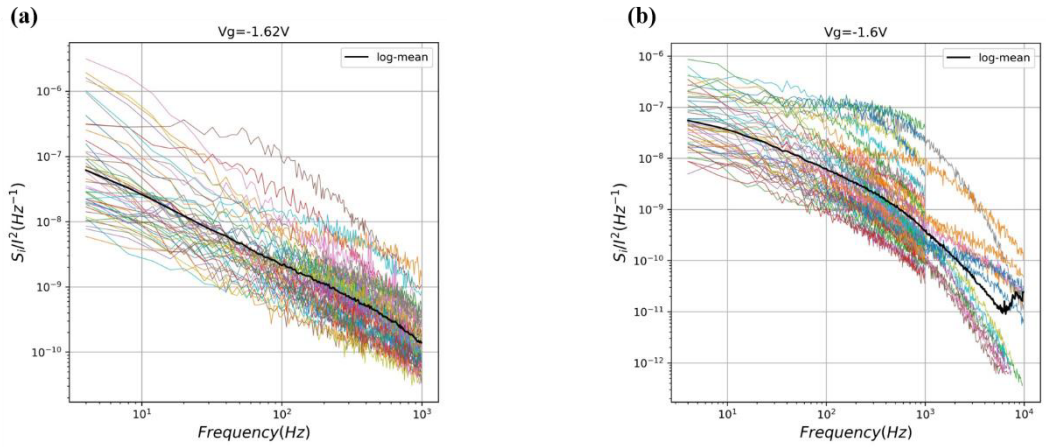

Figure 4.26. Variation of normalized drain current noise versus frequency for: (a) HT P-TFETs with the logarithmic mean over 50 dies and (b) LT P-TFETs with the logarithmic mean over 74 dies. In both cases for V_{DS} = - 0.9 V, W_{fin} = 1 µm, L_G = 0.5 µm and 15 channels.

4.4.2. Impact of TFET fin width on LFN behavior

The impact of the fin width in multi-channel structures of trigate TFETs on the LFN behavior has been studied experimentally. In order to obtain trustworthy results, a relevant statistical sample of at least 50 dies has been measured for different fin widths (W_{fin}): 1 µm, 0.5 µm, 0.2 µm and 0.1 µm. Of course, the results are presented for the effective width given by $W_{eff} = N_{channels} \times [(W_{mask} - \Delta W) + 2 \times T_{Si}]$. Figure 4.27 shows that the average gate voltage noise for TFETs with a large width fin (W_{fin} = 1 µm, blue circles) seems to follow the flat-band voltage fluctuations power spectral density (S_{Vfb}) and the noise is not significantly increased for higher gate voltages. As soon as the width of the fin is decreased (W_{fin} = 0.5 µm, orange circles) the average gate voltage noise begins to diverge from the flat-band noise voltage reference, despite the fact that the effective width is quite similar to the case of W_{fin} = 1µm. This effect is even more pronounced for TFETs with narrower fin and effective width. The evolution of the noise is identical to the case seen for LT TFETs (Figure 4.23), which indicates that a smaller fin width enhances the junction defects impact on the LFN.

This could be a serious challenge for TFETs because one of the possibilities to overcome the low on-current is to rely on multi-channel structures with very narrow fin. However, if the quality of the fin is not good enough, even for conventional annealing temperatures, the

density of traps in the junction will be higher (similar to LT process) and will completely degrade the performance and the subthreshold swing for low-power applications.

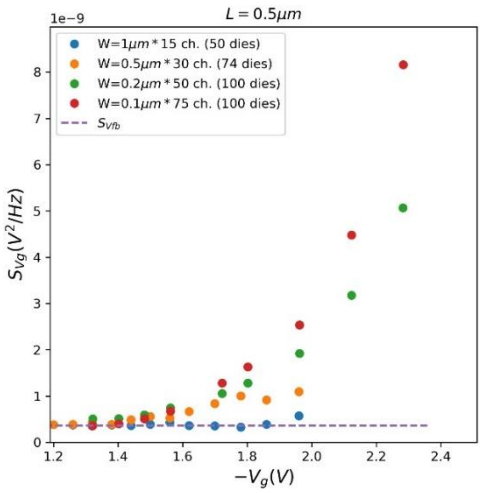

Figure 4.27. Comparison of average input-referred gate voltage noise for different fin width HT TFETs in P-type configuration (V_{DS} = - 0.9 V).

4.4.3. Impact of temperature on TFET LFN

Another way to confirm the presence of TAT in the junctions is via heating the wafer when the electrical characterization is performed. Figure 4.28a shows the transfer characteristics of a HT TFET device measured at different temperatures. In theory, interband tunneling is independent of the temperature, which means that it should be obtained the same $I_D(V_G)$ curve regardless of the environment temperature. On one hand, from Figure 4.28a it is clear that increasing the temperature from 300K to 400K there is a proportional increase of the drive current. On the other hand, TAT is temperature dependent and this provides another evidence indicating the presence of traps in the junctions of our TFETs. If we consider the gate voltage overdrive V_G-V_{ON}, where V_{ON} is the voltage at which the drain current is equal to 0.1 nA, in Figure 4.28b it is clear that the curves are superimposed, meaning that there is a linear dependence between the TAT current and the temperature, regardless of the applied gate voltage. This can be attributed to the thermally activated junction defects, responsible for the additional TAT current.

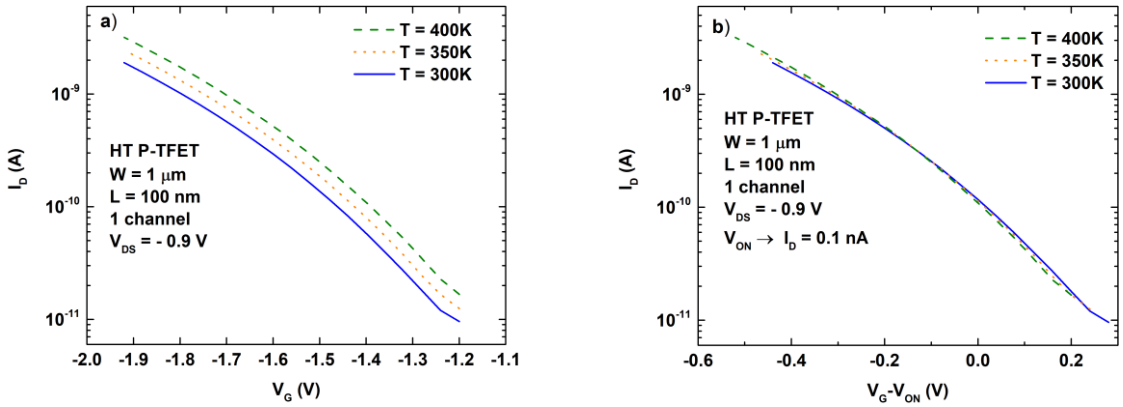

Figure 4.28. (a) $I_D(V_G)$ curves of HT TFET obtained at different environment temperatures; (b) Drain current versus gate overdrive voltage (V_G-V_{on}).

The study of the drain current noise will provide a better understanding of what is happening with respect to the density of traps when the temperature is increased beyond 300K. Figure 4.29a shows the variation of the temperature-normalized relative drain current noise versus the frequency. From here we observe that for 300K there is a *1/f-like* behavior which indicates a uniform distribution of oxide traps. On the contrary, for 400K there is a clear Lorentzian-type $1/f^2$ trend providing evidence for the existence of new non-oxide traps. Basically at 400K there is a group of traps at the junctions that is now thermally activated, while for 300K were deactivated or very slow to observe. As qualitatively explained in Figure 4.24, the higher the trap density, the higher the LFN as measured in Figure 4.29a. Also, more "stepping stone" channels are available for TAT and the drain current is increased, not because interband tunneling, but through TAT (Figure 4.28a). These trends of noise with temperature are also confirmed when comparing under the same gate overdrive voltage (Figure 4.29b).

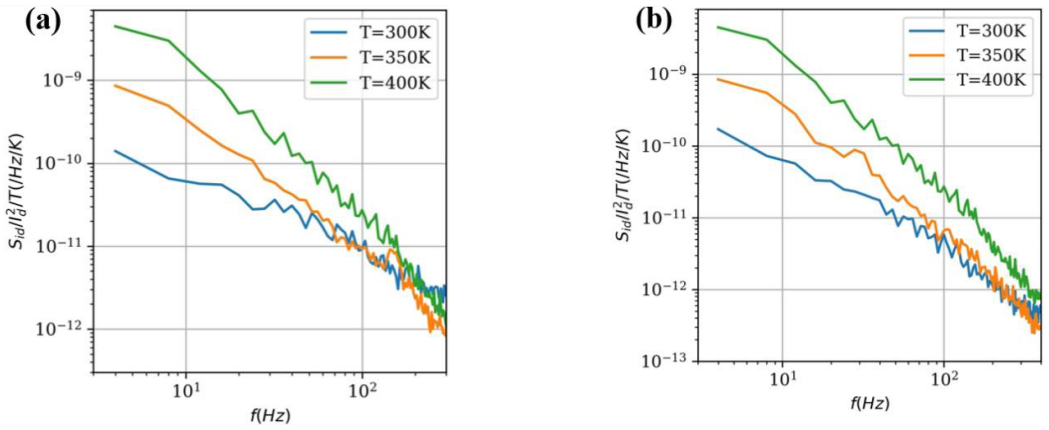

Figure 4.29. (a) Variation of the drain current noise normalized by the temperature versus the frequency at different environment temperatures (V_G = - 1.76 V & V_D = - 0.9 V); (b) drain current noise normalized by the temperature for gate voltage overdrive ($V_G - V_{ON}$ = 0.12 V & V_D = - 0.9 V).

Selecting a given frequency of 4 Hz from Figure 4.29a and representing the drain current noise with respect to the drain current in Figure 4.30a, we observe that the noise is almost 2 orders of magnitude higher for 400K than at room temperature. Figure 4.30b shows the drain current noise normalized with respect to the temperature. Results indicate that even after normalization, TFETs at 400K still present 2 orders of magnitude higher LFN levels for all voltage and current regions.

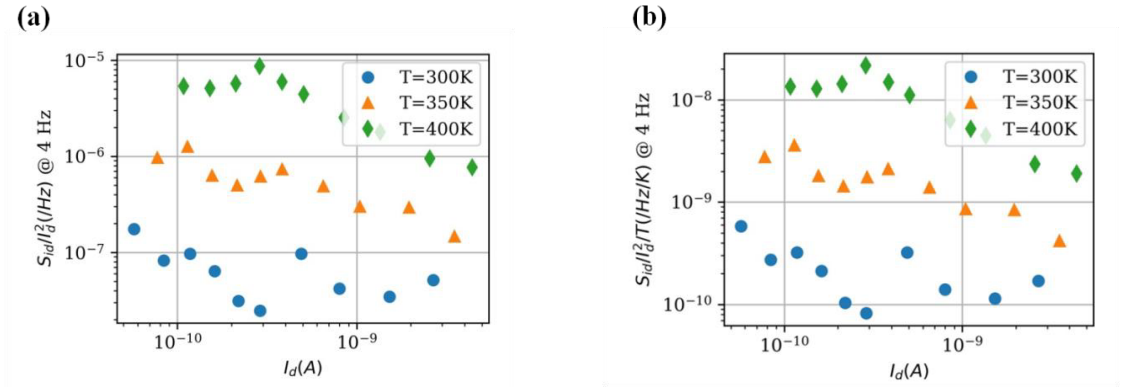

Figure 4.30. (a) Variation of the normalized drain current noise versus drain current at 4 Hz for different temperatures; (b) drain current noise normalized by the temperature versus drain current at 4 Hz.

4.5. Conclusions

In this chapter, we provide evidence which suggest that the enhancement of the on-current and the degradation of the off-current in LT TFETs is due to junction region defects that cause TAT to occur when the device is supposed to be turned off. Once this hypothesis made, we make the assumption that a higher density of traps located in the bulk of the semiconductor or at semiconductor-insulator interfaces are responsible for the larger degradation in LT TFETs than in HT Tunnel FETs. Moreover, these traps result in a generation current that degrades the subthreshold slope.

We have characterized the average density of traps using the charge pumping method. This type of measurement is particularly interesting for gated PIN diodes (as our fabricated TFETs), because both types of carriers are necessary to generate the recombination process which generates the charge pumping current. The application of a periodic squared signal on the front gate allows one to sweep the front interface from accumulation to inversion. From the slope of $I_{CP,max}$ as a function of frequency, it is possible to calculate the average defect density. In addition, applying a negative back-gate voltage to the substrate deactivates the back interface. In that case, we can obtain the density of defects only from the front interface. Experimental results, show a higher density of traps in LT TFETs (~ $1.5 \cdot 10^{11}$ $cm^{-2} \cdot eV^{-1}$) than in HT tunnel FETs (~ $7.0 \cdot 10^{10}$ $cm^{-2} \cdot eV^{-1}$). Several TFET geometries were tested with different narrow widths and the LT TFETs always exhibit a higher density of traps than the HT TFETs.

In order to confirm these data, we have performed TCAD simulations based on the evolution of the carrier concentration at different pulse base levels, while keeping the amplitude of the pulse constant. The objective is to establish a relationship between the experimentally measured charge pumping current and the recombining carrier concentrations for the different cases: when only the top interface contributes to the CP current and when the back interface also contributes. For $V_{G,base}$ = - 0.65 V, simulations of carrier concentrations as function of back gate voltage show the same trend that the experimental charge pumping current. More importantly, the impact of the contribution of the back interface to the carrier density that participates in the recombination process is negligible, regardless of the applied back gate voltage. However, when changing the pulse base level (to - 0.35 V and - 0.85 V) it is observed that depending of the applied back gate voltage we are not measuring $I_{CP,max}$, but only a fraction of it. Therefore, the calculation of the average density of defects is underestimated. Specifically, this happens for negative back gate voltages when $V_{G,base}$ = - 0.85 V and for positive back gate voltages when $V_{G,base}$ = - 0.35 V. This indicates that the calculation of N_{it} using the slope of the $I_{CP,max}(f)$ curve is the most accurate method. Finally, we note that the charge pumping method requires that $V_{G,base}$ and $V_{G,top}$ sweep the front-interface from accumulation to inversion. Otherwise, we cannot be certain about measuring the whole charge pumping current.

Low-Frequency noise analyses have shed light on the nature of the traps in LT and HT processes. Increase of the input-referred gate voltage noise S_{V_g} with the gate voltage for LT TFETs is an indicator of the presence of defects at the source junction. Moreover, the non *1/f* behavior of the average drain current noise spectra reveals a non-uniform distribution of traps in the oxide region, or/and the presence of additional defects, namely in the junctions. Lastly,

noise measurements at different temperatures evidence a drain current increase for temperatures above 300K. This is due to the activation of a number of traps located at the junction due to the broadening of the electron distribution energy (Fermi-Dirac distribution) when temperature is raised. As a result, these traps are enhancing the tunneling current through trap-assisted tunneling instead of BTBT and induce higher level of noise. As expected, this effect is much larger in LT TFETs than in HT devices.

The key messages of this chapter are: **charge pumping measurements confirm a higher average density of defects at the top interface for LT TFETs** fabricated with different geometries than HT devices. Secondly, **TCAD simulations** show the **relation between carrier concentration in the channel region and the charge pumping current for different values of the back gate voltages**. Low-Frequency noise analysis provides a better understanding of the nature of the defect density for TFETs at different thermal budget. **The non-*1/f* behavior of the noise spectrum for LT TFETs suggest a non-uniform distribution of defects close to the junctions**. Therefore, **TAT is responsible of increasing the drain current and not the interband tunneling**, which in fact degrades the possibility to achieve a sub-thermal subthreshold slope. Finally, **the temperature dependence of LFN further proves the dominance of TAT** in the low current region in the devices under test.

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Chapter 5.
Innovative TFET architectures

5.1. Motivation

The state-of-the-art presented in Chapter 2 establishes that all-silicon Tunnel FETs show the steeper subthreshold slope possible [1]–[3] (in some cases lower than 60 mV/dec over several decades of drain current). The well-controlled process fabrication and the maturity of silicon as semiconductor enable a low density of defects, but with a degraded drive current due to a large indirect energy bandgap, heavier electron (hole) effective mass and a wider tunneling length. On the other hand, new BTBT materials like SiGe, Ge or III-V compounds provide a narrow direct bandgap, small carrier effective masses and a narrow tunneling distance that should increase the tunneling current. However, the maturity of these materials is limited, more defects being generated in the semiconductor region [4], degrading the subthreshold slope.

Low subthreshold swing, low off-current and high I_{ON}/I_{OFF} ratio are crucial for ultra-low power applications (V_{DD} < 0.4 V) [5] and BTBT enables very low off-current (which has been demonstrated). Moreover, interband tunneling has the theoretical capability of achieving a SS lower than 60 mV/dec at room temperature (300K) [6]. These characteristics make TFETs promising candidates for ultra-low power applications. Nevertheless, the systematic measurements of our fabricated TFETs have shown a small drain current ($5.7 \cdot 10^{-2}$ µA/µm) and a degraded subthreshold swing of 160 mV/dec over 3 decades of current, as presented in Chapter 3 [7]. In practice and after a thorough search in the literature it has been proven extraordinarily difficult to get a steeper slope and "high" on-current simultaneously, regardless of materials [8]–[13], architectures [14], [15] or specific fabrication steps [16], [17] considered to increase the tunneling probability [18].

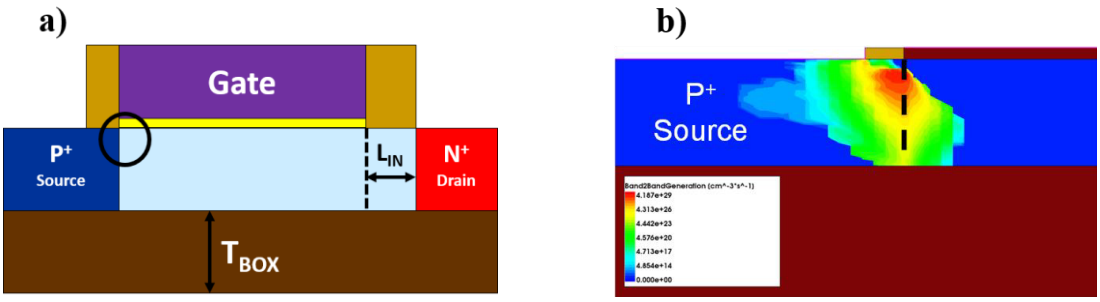

Figure 5.1. (a) Standard reference N-TFET structure simulated with TCAD Sypnosys [19]. (b) Magnified view of the BTBT generation region indicating that in a lateral TFET (L_G = 500 nm and T_{Si} = 11 nm), the tunneling occurs in the source/channel junction below the front gate with V_G = 2.4 V and V_D = 0.9 V.

The simulation of a p-i-n gated diode with the same geometric dimensions as our measured TFETs (Figure 5.1a) shows that the BTBT generation is located at the source/channel junction below the front gate (Figure 5.1b), being independent of the gate length. So, to increase the tunneling current it is necessary to maximize the tunneling

generation area. New state-of-the-art approaches on TFETs architectures such as vertical nanowires based on III-V compound materials have been recently demonstrated [20] with optimistic results for on-current and SS below 60 mV/dec, although only over three decades of drive current. These solutions are challenging because the transfer onto silicon platform is not straightforward [12] and the co-integration of vertical nanowires with trigate architectures is not yet feasible nowadays.

5.2. Proposed TFET architectures

This chapter is focused on the simulations of innovative planar TFET architectures with different variations of the source junction architectures, designed to increase the tunneling generation area. The aim is to determine which solution provides best performance (Extended-Source TFET, Pure Boron TFET or Sharp Tip TFET), while staying compatible with a silicon platform and the enabling co-integration with CMOS technology.

We have performed 2D TCAD simulations of silicon Tunnel FETs using the Nonlocal Path Band-to-Band model of Sypnosys tool with default tunneling parameters and coupled to classical Drift-Diffusion equation with constant mobility [21]. The standard TFET from Figure 5.1a serves as a reference to compare the results obtained from the proposed architectures. The parameters common to all devices are: gate length L_G from 500 nm down to 15 nm, T_{BOX} =145 nm, EOT = 1.18 nm, intrinsic body length L_{IN} = 20 nm near the drain region to suppress the ambipolarity effect [22], a gate work function Φ_{gate} = 4.0 eV and dopant concentration in source and drain of $N_D = N_A = 10^{20}$ cm^{-3}.

5.2.1. Extended-Source TFET

The extension of the source region into the channel region is a feasible solution to enhance the tunneling area. When the source is extended (Figure 5.2a) and an inversion layer of electrons is formed at the top surface of the channel (V_G > 0), an effective vertical p-i-n structure is generated in the whole gate region. This is confirmed thanks to the BTBT generation mapping in Figure 5.2b, where two tunneling contributions are noticed. One is located at the source/channel junction (the lateral tunneling contribution) and the other one is located along the extension of the source at the body bottom (with $N_{ext} = N_A$). The latter component significantly increases the BTBT generation area and therefore, the drive current. Consequently, the Extended-Source TFET (ES-TFET) presents a higher tunneling area and current than the standard TFET.

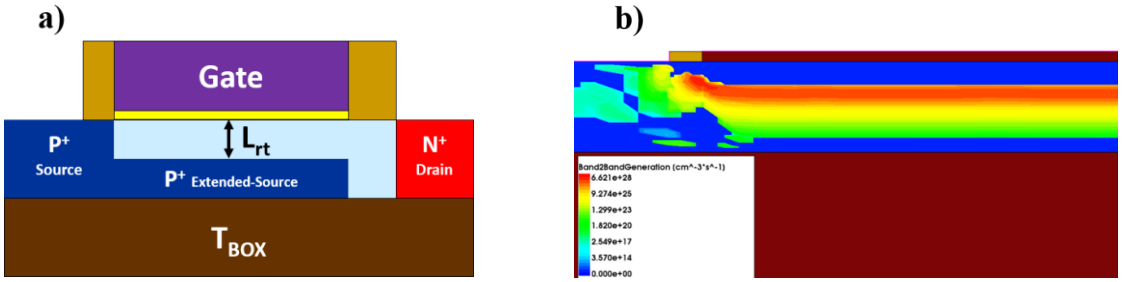

Figure 5.2. (a) Schematic of Extended-Source N-TFET architecture (T_{Si} = 11 nm, L_{rt} = 3 nm and L_G = 500 nm) with tunneling parallel to the gate electric field. (b) BTBT generation showing the presence of vertical BTBT in the extension of the source into the channel region (with V_G = 2.4 V and V_D = 0.9 V) [19].

The concept of source extension has already been demonstrated in several studies. For example, Y. Morita *et al.,* proved a Tunnel FinFET with ultrathin epitaxial channel on silicon CMOS platform [23]. The FZ Jülich laboratory has also added new boosters in planar TFET structures. For example, a counter-doped pocket in the source junction to enable vertical BTBT aligned with the gate electric field in an enlarged area. Besides, a selective and self-adjusted silicidation process was used for on-current enhancement [24]. In both fabricated devices the aim was to make the vertical tunneling component the main contribution of the drain current.

The ES-TFET architecture presents two main differences compared to the previous fabricated Tunnel FETs. Firstly, the source junction extends in the channel region underneath the whole front gate and thus, features a large tunneling area. In addition, the implementation of an intrinsic region (L_{IN}) reduces the undesired BTBT current in the drain region and other possible parasitic effects. Secondly, the tunneling can be modulated by changing the thickness of the silicon film, which determines the contribution of the vertical BTBT and modifies the vertical distance between the source extension and the gate oxide (given by the extension depth L_{rt}). A small L_{rt} distance means a thin channel region (smaller vertical tunneling length), providing a more efficient band bending control by the gate bias and thus, a larger drain current.

5.2.2. Pure Boron TFET

The Pure Boron TFET (PB-TFET) architecture is designed as an improved version of the ES-TFET, because it presents the capabilities to accomplish, at least theoretically, a SS lower than 60 mV/dec based on ultra-thin channels (T_{Si} < 10 nm). Note that the fabrication of an ES-TFET with a heavily doped extended region, only a few nanometers thick, is not feasible using a conventional implantation process. The generated defects, as result of the implantation, will completely degrade the steepness in the subthreshold region.

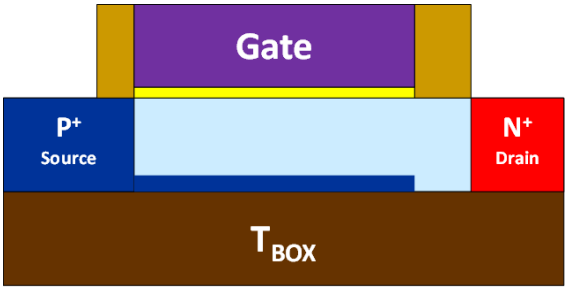

Figure 5.3. Schematic architecture of a Pure Boron TFET (PB-TFET) in N-mode configuration. An ultra-heavily doped 1 nm boron layer is implemented at the bottom body to generate an enhanced vertical BTBT.

The PB-TFET is schematically shown in Figure 5.3. Like the ES-TFET it features an extension of the source into the channel region, by means of a very high dopant concentration in a thin bottom epitaxial layer. We have performed the simulations with a heavily doped 1 nm thick pure boron layer (N_A = 10^{20} cm^{-3} and 10^{21} cm^{-3}) located at the bottom [25]. This configuration allows the simultaneously presence of electrons and holes in the channel for very thin SOI layers, in order to increase the drive current. Moreover, this heavily doped layer avoids the supercoupling effect [26], [27] which prevents the formation of electrons and holes bilayers in ultrathin silicon films (T_{Si} < 11 nm), because a high concentration of holes is

achieved by actual doping and not by field effect [19]. This chapter is specifically dedicated to TCAD simulations, but the Pure Boron technology has already been demonstrated [28]. Therefore, the fabrication of Tunnel FETs with an architecture similar to that of Figure 5.3 could be a reality.

L.K. Nanver *et al.* have demonstrated the feasibility to fabricate Pure-Boron thin-film layers deposited by Chemical Vapor Deposition (CVD), which present electrical and processing properties that are very interesting for device integration [25]. It is important to notice that this technology process allows the implementation of shallow junctions in p^+-n diodes that are extremely useful for photodiodes applications [25].

Pure Boron deposition takes place in an epitaxial CVD reactor using diborane (B_2H_6) and hydrogen (H_2) at a range of temperatures comprised between 400°C-700°C. The boron deposition rate depends of the diborane pressure, concentration and flow rate, but also of the thermal budget (which involves the temperature and the exposure time). The thermal budget is the key parameter because it allows for example at 700°C to form a 2 nm thick boron layer in 160 seconds. Moreover, the resulting boron layer is uniformly deposited on the crystalline silicon and ellipsometry measurements have confirmed a roughness of 0.2-05 nm in the previous temperature range. This is crucial for the PB-TFET architecture because in extremely thin films it is mandatory to achieve the smoothest possible thin bottom layer, to reduce variability that could affect the performance.

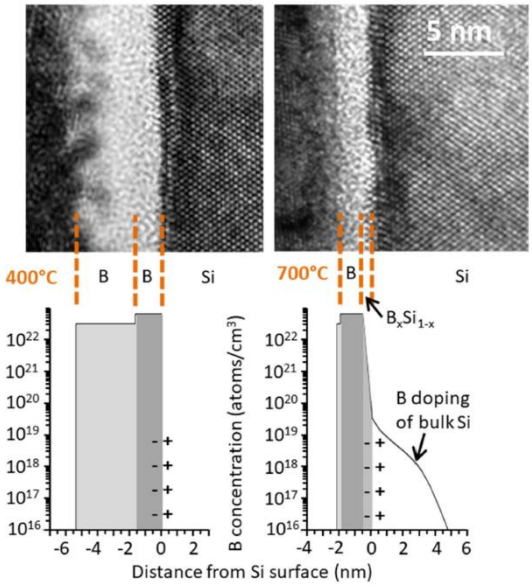

Figure 5.4. Top: HTRM images of PB layers grown at 400°C (left) and 700°C (right). Bottom: Boron-induced doping concentration in the amorphous Boron (*α-B*) layers with the equivalent of about 10^{22} cm^{-3} in a couple of nanometers thick layer [29].

An important property of this technology is that the boron layer can act as an abundant source of boron dopants for ultra-shallow junctions. Besides, this high doping concentration is achieved due to the interface conditions between the boron layer and the crystalline silicon and not due to the doping of the bulk silicon. When the monolayer of acceptor states is created and filled with electrons at the interface, a fixed negative charge is created (Figure 5.4). This negative charge attracts about $5 \cdot 10^{14}$ cm^{-2} surface density of holes, which behave just like a p-doped layer with respect to the hole injection from the p-region into the n-layer and electron injection from the n-layer into the p-layer. The boron doping concentrations

(Figure 5.4) confirm that is possible to get the equivalent of about 10^{22} cm^{-3} in a couple of nanometers thick layer [29]. After the α-Boron layer removal there is a boron concentration left of 10^{14} cm^{-2}, which is equivalent to a boron peak-concentration around 10^{21} cm^{-3}.

Pure Boron layers have also different properties according to the deposition temperatures as it can be seen from the HTRM top images of Figure 5.4. In both cases a uniform and compact amorphous boron layer is created on the crystalline silicon surface. At 700°C there is also the formation of a 1 nanometer B_xSi_{1-x} layer, while the 400°C deposition leaves the silicon surface flat. However, at 400°C there is a formation of an incomplete layer of non-compact boron (above the α-Boron layer and thicker than this one), while at 700°C there is no presence of this layer.

For PB-TFET it is most interesting to process the boron layer at 400°C. The reason is the lack of boron impurity doping in the bulk silicon (at 700°C the boron can diffuse a few nanometers into the bulk silicon, doping it to values of $2 \cdot 10^{19}$ cm^{-3} [29]). Moreover, activating the boron with higher temperature steps is counter-productive because the annealing will finally destroy the attractive interface properties and the bulk doping is limited by the solid solubility, so it will not be possible to reach the high doping levels required. Therefore, the opportunities to fabricate PB-TFETs will depend on the thermal budget of post-boron deposition steps and the possibilities for performing the deposition. Lastly, there will be also boundary conditions not described here in order to achieve a successful deposition.

5.2.3. Sharp Tip TFET

The last proposed innovating architecture is the Sharp Tip TFET (Tip-TFET), the schematic of which is presented in Figure 5.5. This device configuration relies on the implementation of a sharp tip at the source junction, to achieve an enhancement of the electric field. BTBT generation rate and tunneling current, given by Kane's equation [30], is proportional to the electric field. Therefore, if the electric field is increased the drive current should be also higher.

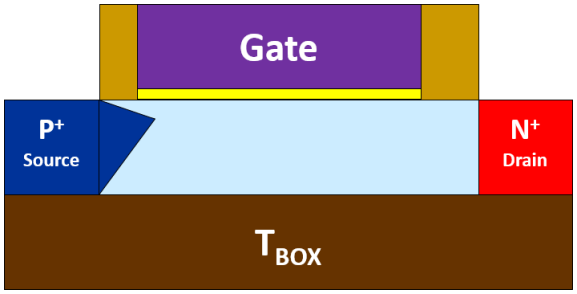

Figure 5.5. Schematic architecture of a Sharp Tip TFET in N-mode configuration to enhance the electric field at the source junction.

The objective with this architecture is to evaluate the possibility of taking advantage of an embedded raised source and drain process with a sharp source junction tip. Intel's trigate CMOS transistors were the first to demonstrate these embedded structures for the 45 nm technology node with high-k metal gate dielectric (Figure 5.6) [31]. This process innovation was initially developed for strained PMOS transistors to increase the hole mobility and thus, performance. 32 nm logic technology also includes these embedded SiGe regions [32], but they are closer to the channel region to increase the channel strain.

It is important to notice that two technological parameters will drive the enhancement of the tunneling current: first, the proximity of the embedded tip source and drain areas to the channel region (if the tip is overlapped or underlapped w.r.t. the gate edge) and secondly, the position of the peak with respect to the front gate. Both are key in order to maximize the BTBT generation rate. Note that, for films below 10 mn thick, it will be more challenging to fabricate these regions, so a well-controlled process fabrication will be necessary.

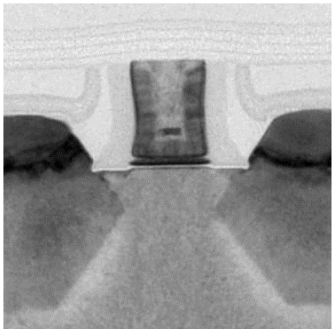

Figure 5.6. TEM image of a high-k + metal gate PMOS transistor with embedded source and drain SiGe process in 45 nm technology node to stress-enhancement [31].

5.3. Extended-Source TFET

5.3.1. Impact of the restricted tunneling length for a given Si film thickness

The most important aspect of the ES-TFET architecture is to determine the impact of the undoped body region thickness (L_{rt}) in the performance.

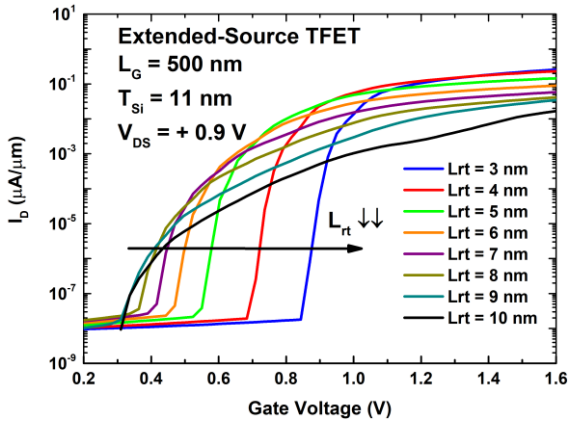

Figure 5.7. $I_D(V_{GS})$ curves of Extended-Source TFET for a 11 nm silicon body thickness and different extension depths (L_{rt}) with respect to the gate.

Figure 5.7 shows the transfer characteristics for different L_{rt} distances ranging from L_{rt} = 3 nm to L_{rt} = 10 nm, with a silicon body thickness of 11 nm. The ES-TFET exhibits a higher on-current and steeper slope for small vertical distances between the extension and the gate oxide (L_{rt} =3 nm, blue line). Consequently, for larger L_{rt} distances there is a degradation of the electrostatic control, because the front gate bias cannot trigger properly the vertical BTBT. In addition, the drain current begins to decrease due to the increase of tunneling distance, causing a visible degradation of the subthreshold slope. Good performance is kept until L_{rt} = 7 nm (purple line), but for larger undoped regions the tunneling distance becomes too

large. A larger L_{rt} creates a lower electric field and thus a small band bending. Figure 5.7, indeed, verifies that TFET technology requires a very thin body and explains why it is not possible to obtain an SS below 60 mV/dec for channel thickness in the range of 11-10 nm for a standard TFET [4].

One of the major problems of ES-TFET lies in the non-desired enhancement of the threshold voltage, as long as the P^+ extension of the source occupies the majority of the channel region. In this case the channel is at a lower potential than in a fully undoped channel region (as in a standard TFET), so it will be necessary to apply a higher front gate voltage to create an inversion layer at the top of the channel. Even though we are using a gate work function of 4.0eV instead of 4.61eV (which provides an extra electrostatic control of 0.61 V and thus a V_{TH} reduction), the threshold voltage is higher than 0.8 V for L_{rt} = 3nm, which is not convenient for ultra-low power applications (V_{DD} < 0.4 V). In TCAD studies it is possible to lower the value of the work function parameter to reduce the threshold voltage. Unfortunately, for a real process fabrication, gate materials with work functions lower than 4.0 eV such as potassium (3.0eV), calcium (2.87eV) or even cesium (1.95eV) are unpractical in N-TFET devices. On the other hand, for P-TFETs it is possible to find useful gate metals with a high work function, such as platinum (5.63eV) that at least in theory can work with a lower bias supply. For L_{rt} = 5nm there is a trade-off between a low threshold voltage (~ 0.5 V) and a high on-current, although slightly lower compared to L_{rt} = 3nm, but without changing the gate work function.

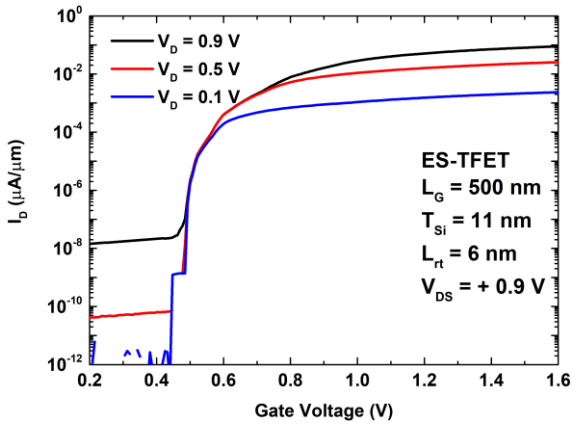

Figure 5.8. $I_D(V_G)$ curves of Extended-Source TFET with long channel (L_G = 500 nm) for T_{Si} = 11 nm, L_{rt} = 6 nm, and different drain voltages.

The applied drain voltage has also an important impact in the drive current, because it is responsible for the tunneling of carriers and their drift towards the drain terminal. $I_D(V_G)$ curves of an ES-TFET with L_{rt} = 6nm, for different V_D polarizations (Figure 5.8), confirm that a progressive V_D increase (from 0.1 V to 0.9 V) causes an enhancement of 1.5 decades in the on-current. Essentially, a higher lateral electric field generates and attracts more carriers. Unfortunately, the off-current is also increased owing to unwanted tunneling in the drain junction and thus, degrading the performance. However, apply a V_D beyond 0.9 V is not recommended, because it will start to deplete the inversion layer, shrinking the tunneling area and current. For V_D higher than 0.5 V the on-current tends to saturate but the off-current is further degraded, reducing the I_{ON}/I_{OFF} ratio. The off-current degradation will be magnified for short gate lengths, because the drain voltage will bend the energy band diagram of the channel region increasing the undesired tunneling in the drain junction. Finally, TFETs aimed

for ultra-low power applications require the lowest drain voltage (and gate voltage) possible, so the idea is to reduce and not to increase the drain voltage. Therefore, the simulations for all the studied architectures presented in this chapter have been done with a drain voltage of 0.9 V.

5.3.2. Impact of Si film thickness for a given restricted tunneling length (L_{rt})

Figure 5.9a shows the transfer characteristics for L_{rt} = 3nm and different silicon thicknesses. Thinning down the T_{Si} from 11nm to 4nm, one can observe a progressive enhancement of the on-current, and the best case occurs for T_{Si} = 6nm. This is related with a better electrostatic control and a more efficient band bending for a narrow body thickness. However, for T_{Si} = 4nm, there is a noticeable degradation of the on-current and the subthreshold slope. This is most likely due to the fact that when the body thickness is reduced, with L_{rt} being fixed to 3nm, the extended source is thinner and therefore more resistive, minimizing the on-current.

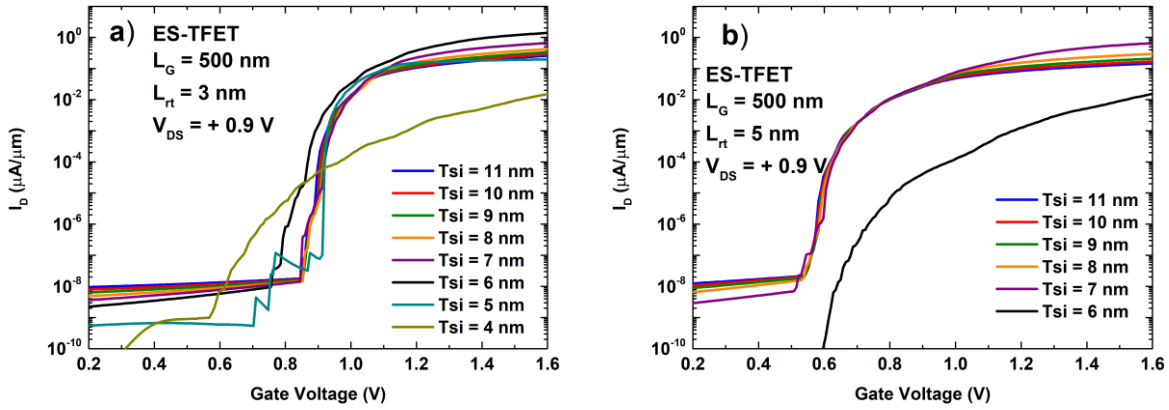

Figure 5.9. $I_D(V_{GS})$ curves of Extended-Source TFET for a gate length of 500 nm and different silicon body thickness ranging for a given extension depth: (a) L_{rt} =3 nm and (b) L_{rt} = 5 nm.

Figure 5.9b shows the $I_D(V_G)$ curves, but in this case for an extension depth of 5nm (trade-off case from Figure 5.7). The best I_{ON}/I_{OFF} ratio is obtained for a silicon body thickness of 7nm, while for T_{Si} = 6nm one can notice a clear degradation of the drive current and subthreshold slope respectively. In both cases the degradation occurs when the thickness of the extended source is only 1nm thick (L_{rt} =3nm for T_{Si} =4nm and L_{rt} =5nm for T_{Si} = 6nm).

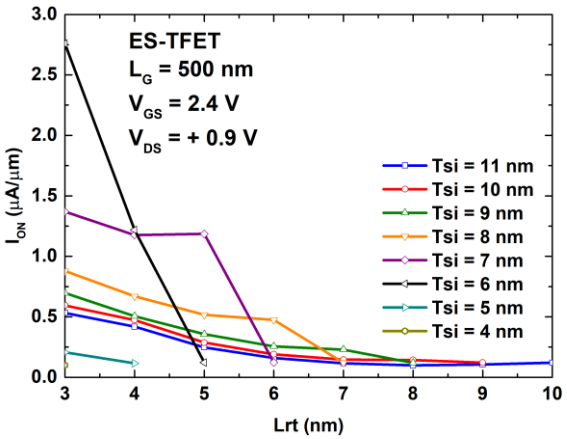

Figure 5.10. I_{ON} versus extension depth (L_{rt}) for different silicon thickness of ES-TFET architecture with L_G = 500 nm.

To obtain a better knowledge of the ES-TFET with respect to the extension depth (L_{rt}), Figure 5.10 shows the on-current at V_{GS} = 2.4 V, obtained for different L_{rt} values with the variation of the silicon body thickness. We can observe a general trend in all the studied cases: when L_{rt} is decreased the on-current increases, because of a shortening of the tunneling length. Regardless of the simulated film thickness the highest on-current is always obtained for the smallest vertical distance possible between the extension and the gate oxide (L_{rt} = 3 nm). The most optimized ES-TFET architecture features a film thickness of 6 nm, while for T_{Si} = 5 nm and 4 nm the on-current is degraded. Other simulation results (not shown in Figure 5.10) indicate that an ultra-thin body thickness (T_{Si} < 6 nm) requires an extension depth lower than 3 nm to achieve a tunneling current enhancement. Unfortunately, the potential fabrication of this junction extension into the channel architecture with enough quality and accuracy is not feasible nowadays via a conventional implantation process.

5.3.3. Comparison of Extended-Source TFET with Standard TFET

The comparison of the ES-TFET architecture with an 11 nm body thickness and an extension depth L_{rt} = 3 nm with respect to the standard Tunnel FET (Figure 5.11a) clearly establishes how the ES-TFET outperforms the standard architecture for a long gate length (L_G = 500 nm). The higher drive current exhibited is consequence of the vertical BTBT that takes place in the whole source extension, while in the standard TFET it is located at the source junction. The steeper subthreshold slope is the result of an important reduction of tunneling path length (3 nm) due to the extended source in the channel region, which significantly improves the electrostatic control compared to the standard TFET. The SS extractions in Figure 5.11b confirm that ES-TFET achieves SS below 60 mV/dec over 4-5 decades of current. For comparison, in the standard TFET the SS is degraded (~ 75 mV/dec) even at very low values of drain current.

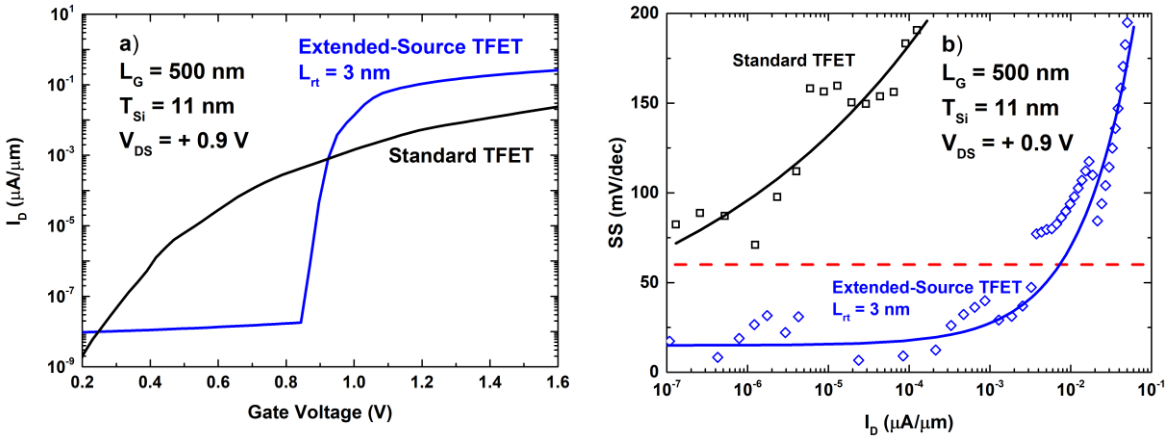

Figure 5.11. Comparison of: (a) $I_D(V_G)$ curves and (b) figure of merit SS(I_D) for standard and Extended-Source TFET.

The same comparison conducted for a film thickness of 6 nm (Figure 5.12a) shows that the extended-source architecture still outperforms the standard TFET. In fact the tunneling current is higher for T_{Si} = 6 nm than for T_{Si} = 11 nm. Only when T_{Si} is in the range of 4 nm (Figure 5.12b), the standard TFET presents a higher drive current and a stepper slope than the ES-TFET, not due to an improvement of the standard structure but because of an severe degradation in the performance of the ES-TFET. Most likely, the reduced cross-section of the

channel is responsible of the series resistance degradation, which masks the extra tunneling current generated from the extended source. The previous results are done for long gate devices (L_G = 500 nm). However, in current technological nodes the physical gate length of devices is shorter than 50 nm. This shrinking will heavily affect the vertical tunneling because the tunneling area is restricted. Therefore, the next section presents a thorough study to determine the impact of the gate length in the total tunneling current and how much it is possible to extend the benefits of the vertical BTBT as long as the gate length and SOI layer thickness are reduced.

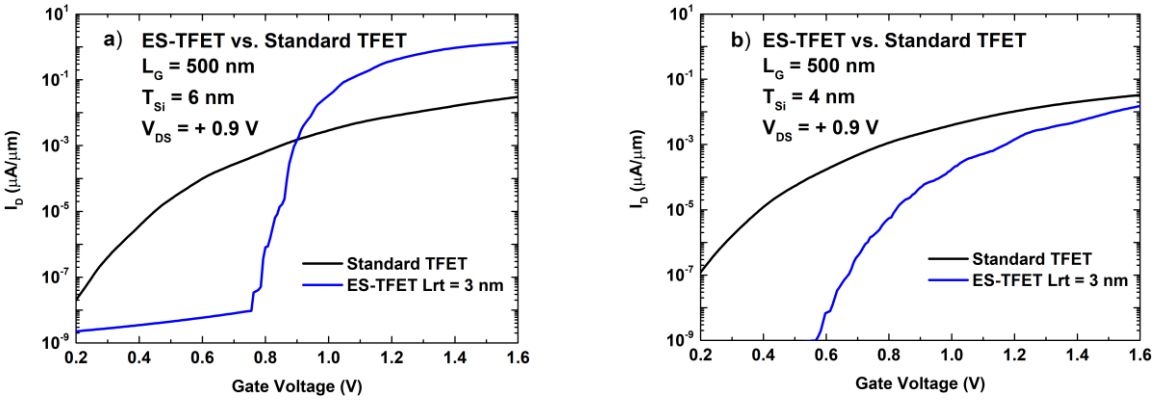

Figure 5.12. Transfer characteristics comparing the ES-TFET and standard TFET architectures with long channel (500 nm) for: (a) T_{Si} = 6 nm and (b) T_{Si} = 4 nm.

5.3.4. Impact of gate length on drive current

The current independence with respect to the gate length in a standard TFET is documented in Figure 5.13. In an ES-TFET, on the contrary, the magnitude of the on-current depends on the length of the extension of the source into the body. Therefore, if the gate length is reduced (L_G < 100 nm) the current will be degraded because the tunneling area will be reduced (as shown in Figure 5.13). A thorough analysis of the simulation results shows that for long channel distances we obtain an on-current that outperforms the standard TFET by a factor of 3x in the best case where L_{rt} = 3 nm. For larger extension depths the current decreases, but the advantage is kept until L_{rt} = 5 nm. For L_G < 50 nm, the benefit of the vertical BTBT disappears due to the reduction of the BTBT generation area and the standard TFET shows better on-current values.

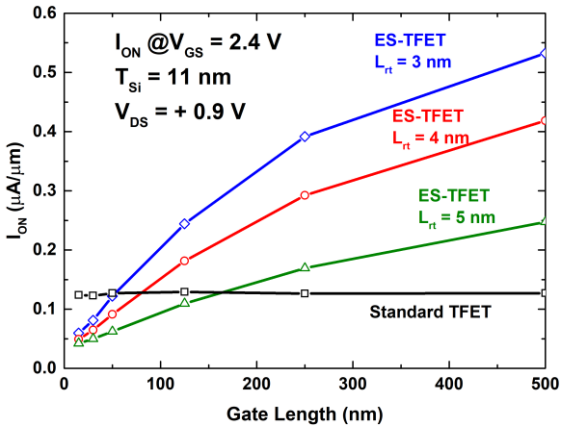

Figure 5.13. $I_{ON}(L_G)$ for standard and ES-TFET architecture. Long enough lengths (> 100 nm) for ES-TFET architecture achieve better I_{ON} than for standard TFET.

The reduction of the body thickness improves the electrostatic control for the ES-TFET and enhances the on-current. For long channel devices with T_{Si} = 8 nm (Figure 5.14a) on-current is boosted by a factor of 7x and the benefits of vertical BTBT are extended for L_G down to 30 nm. For T_{Si} = 6 nm (Figure 5.14b) vertical BTBT dominates even for extremely short gate lengths. Not only is the tunneling rate improved, but also the short-channel effects are mitigated by the film thinning which enhances the electrostatic gate control.

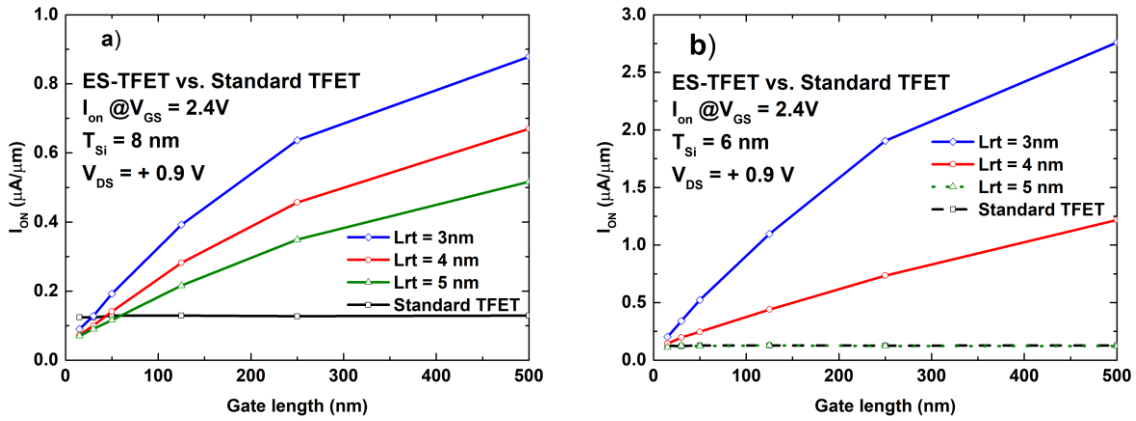

Figure 5.14. $I_{ON}(L_G)$ for standard and ES-TFET with different thickness. (a) T_{Si} = 8 nm: the benefits of vertical BTBT are extended down to L_G = 30 nm. (b) T_{Si} = 6 nm: vertical BTBT dominates even for very short gate lengths.

5.4. Pure Boron TFETs

5.4.1. Impact of silicon body thickness

As explained in the previous section, when the thickness of the extended source was limited to only 1 nm thick due to the extension depth (L_{rt}), the on-current and the subthreshold slope were degraded (Figure 5.9).

The Pure Boron TFET (PB-TFET) with a doping of 10^{20} cm^{-3} in the thin bottom layer (Figure 5.15) presents a complex trend when the silicon body thickness is thinned down from 11 nm to 4 nm. At first there is a progressive sharpening of the slope when reducing T_{Si} down to 7 nm, and from that point on, further thinning the SOI layer degrades the subthreshold slope. An enhancement of the drain current for medium gate voltages (up to 1.0 V) is noticeable for intermediate values of T_{Si} and a significant degradation is observed for very thin values (from 6 nm to 4 nm). However, at high gate voltages the tunneling current converges to some low value regardless of the body thickness. These non-conclusive simulation results are not consistent with the prospects of a steeper slope for TFETs with a body thinner than 10 nm. They suggest that a higher doping concentration in the thin bottom layer is required in order to achieve the expected results for ultra-thin body thickness.

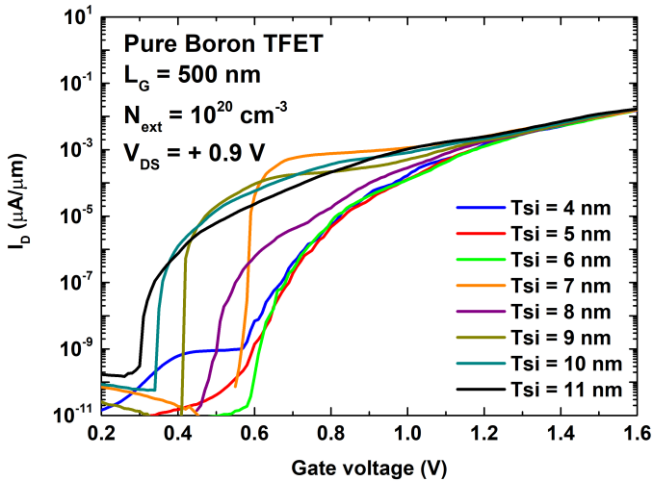

Figure 5.15. Transfer characteristics of PB-TFET architecture with variable body thickness and a Pure Boron doping in the thin bottom layer of 10^{20} cm^{-3}.

New TCAD simulations with an ultrahigh doping concentration of 10^{21} cm^{-3} in the thin bottom layer of the PB-TFET show an improved electrostatic control for narrow channels (T_{Si} < 7 nm) and overall results are far more promising. There is an outstanding performance for T_{Si} = 4 nm (solid blue line) in Figure 5.16 with a 10-fold on-current increase with respect to the ES-TFET with L_{rt} = 3 nm. By increasing the body thickness, by one nanometer increments, it is possible to maintain good transfer characteristics until T_{Si} = 6 nm is reached. For thicker channels (from 7 nm to 11 nm) the performance begins to be significantly altered due to the larger tunneling distance, which results in a reduction of the interband tunneling probability (less BTBT current) and a less efficient electrostatic control by the front gate (degradation of the subthreshold slope).

Like the ES-TFET, the PB-TFET also shows an increase in V_{TH} when film thickness is decreased due to the ultrahigh P-type doping concentration at the bottom of the channel region. Consequently, it is necessary to apply a higher front gate voltage to create an inversion layer at the top of the channel. The shift in the threshold voltage ($\Delta V_{TH}/\Delta T_{Si}$) can reach 0.2 V per nanometer.

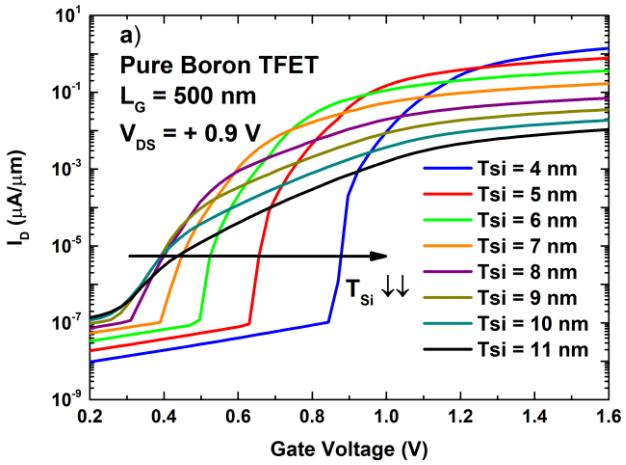

Figure 5.16. $I_D(V_G)$ curves of Pure Boron TFET architecture for long channel devices (500 nm), different silicon thickness, and a ultrahigh doping concentration of 10^{21} cm^{-3} in the thin bottom layer.

5.4.2. Comparison of Pure Boron TFET with Standard TFET

The implementation of an ultrahigh doping concentration of 10^{21} cm^{-3} in a thin bottom layer of the PB-TFET improves the on-current by more than two orders of magnitude compared to the standard TFET architecture (Figure 5.17a). In addition, the subthreshold slope is also steeper as documented on Figure 5.17b. However, the main drawback of the PB-TFET is the degradation of V_{TH} in ultra-thin films that will make difficult its implementation for ultra-low power applications. SS reaches values below 60 mV/dec over 4 decades of current (Figure 5.17b) and is lower than 100 mV/dec for relatively "high" drain current of 10^{-2} µA/µm. By comparison, for the standard TFET, SS is higher than 60 mV/dec in all the current ranges. The problem is to determine how far it is possible to extend this gain in performance in devices with very short gate length, where the tunneling area for the vertical BTBT is constricted.

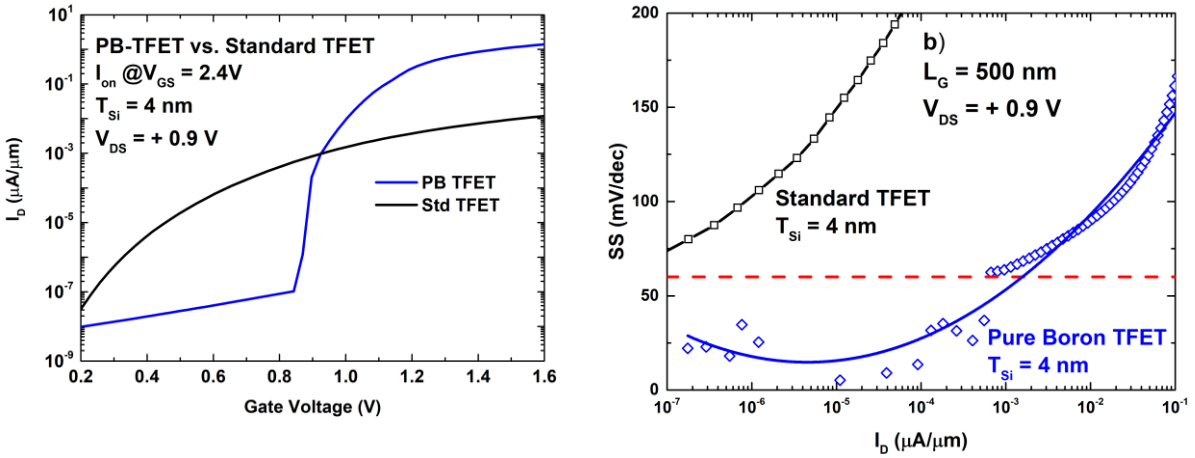

Figure 5.17. (a) $I_D(V_G)$ curves of Pure Boron and standard TFET architectures with long channel (500 nm) and ultra-thin film (T_{Si} = 4 nm). (b) Subthreshold swing versus drain current for standard and PB-TFETs.

5.4.3. Impact of gate length on drive current

Figure 5.18a confirms that a heavily doped boron layer combined with an extremely thin body (4 nm, 5 nm and 6 nm) significantly increases the vertical BTBT for long gate lengths with respect to the standard TFET with T_{Si} = 4 nm. The benefits of Pure Boron technology are maximized for very narrow channels (T_{Si} = 4 nm). When the thickness is increased, there is a degradation in performance because the ultrahigh doped layer is further away from the front gate and the band bending is not so well controlled. Again, the problem arises when devices are made with shorter gates and the tunneling surface in the channel region is shrunk. Figure 5.18a shows that as long as the gate length is decreased, the tunneling current decreases as well. However, as opposite to the ES-TFET, the PB-TFET has better performance than the standard TFET device, even for short gate lengths. This suggest that PB-TFET stands as a feasible option to obtain simultaneously a steep slope and a high on-current. This demands not only a customized Pure Boron layer, but also a very small body thickness. From Figure 5.18a one can notice that for T_{Si} thicker than 6 nm it will not be possible to extend the gain of the vertical BTBT, in particular for small gate lengths.

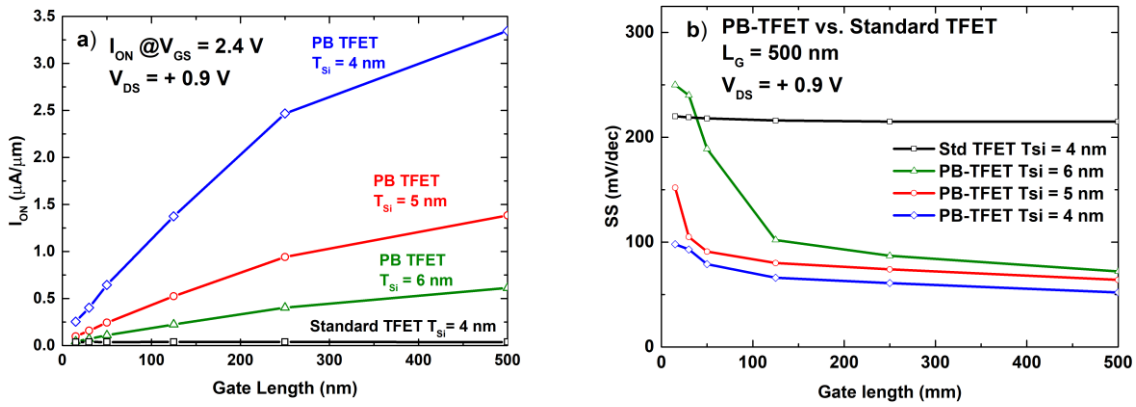

Figure 5.18. (a) $I_{ON}(L_G)$ for standard and Pure Boron TFET architectures with different T_{Si} values. (b) SS versus drain current for standard TFET (I_D range: 10^{-6} – 10^{-3} µA/µm) and PB-TFET (I_D range: 10^{-5} – 10^{-2} µA/µm).

The SS extractions as a function of gate length (Figure 5.18b) show for the PB-TFET architecture a SS degradation with gate length reduction. For PB-TFET with T_{Si} = 4 nm at short gate lengths (L_G < 100 nm) the SS is beyond 60 mV/dec, but limited to 100 mV/dec (for L_G = 15 nm). However, when increasing the body thickness (5 nm and 6 nm) the electrostatic control is reduced and causes a severe increase of the SS still at medium gate lengths. For the standard TFET with T_{Si} = 4 nm, the subthreshold swing is completely degraded and almost the same values are obtained (~ 215 mV/dec). This is confirmed regardless of the gate length and despite the fact that a lower I_D range (from 10^{-6} to 10^{-3} µA/µm) has been used compared to PB-TFET (from 10^{-5} to 10^{-2} µA/µm). When lateral tunneling is involved decent SS values are only obtained for very low range current (< 10^{-8} µA/µm).

5.5. Sharp Tip TFET

5.5.1. Impact of the silicon body thickness

The comparison of the Sharp Tip TFET architecture (Tip-TFET) for different body thicknesses with respect to the standard TFET (T_{Si} = 4 nm) in Figure 5.19a, confirms that the design of a sharp tip in the source junction has no significant impact on the tunneling current (only slightly higher than for the standard architecture). The subthreshold swing follows the same trend in both architectures and it is only better for Tip-TFET for a very low range of drain current (Figure 5.19b). The location of the tip with respect to the front gate and the extension into the channel region are main parameters. Therefore, for a given body thickness the right combination of these parameters must be achieved to maximize the BTBT at the junction. However, for this TCAD study and for the sake of simplicity we have used the same tip parameters regardless of the thickness of the body region.

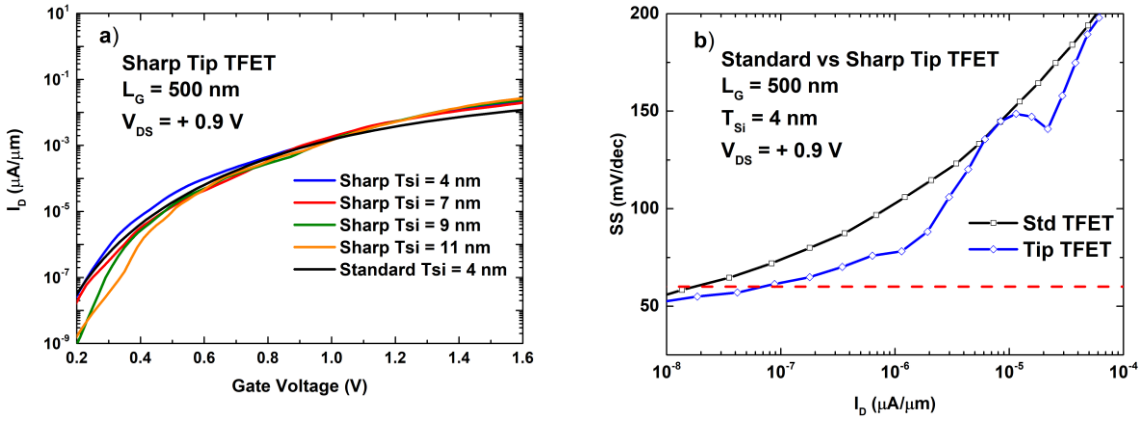

Figure 5.19. $I_D(V_G)$ **curves of Tip-TFET for different body thickness compared with standard TFET (**T_{Si} **= 4 nm). (b) SS versus drain current for Tip-TFET and standard TFET (**T_{Si} **= 4 nm).**

The 2D mapping of the electric field (Figure 5.20a) and the BTBT generation (Figure 5.20b) shows that the tip causes a shift in the position of the maximum electric field. The BTBT rate is improved only where the overlap of this field and the P^+ region takes place. It was thought that this enhanced electric field would break a great number of covalent bonds on the P^+ region, enabling more electrons to participate in the interband tunneling process from the valence band of the P^+ region to the conduction band of the channel region. However, results from Figure 5.19a show that the benefit of this tip junction is marginal. The electric field is enhanced with this architecture but without increasing the tunneling area, which explains why the current is not significantly increased as it is for the ES-TFET and PB-TFET architectures.

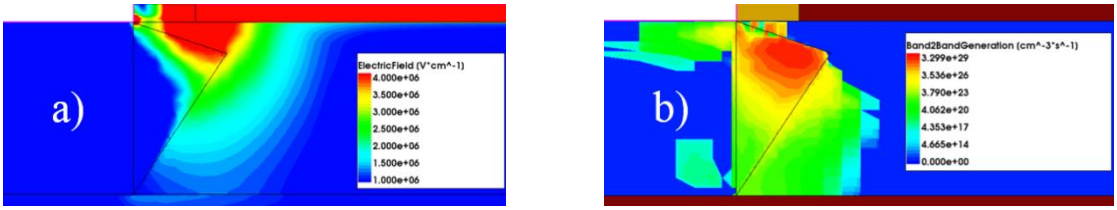

Figure 5.20. 2D mapping of Sharp Tip-TFET with T_{Si} **= 11 nm and a gate length of 500 nm: (a) Maximum electric field and (b) BTBT generation. In both cases applied polarization is** V_G **= 2.4 V and** V_D **= 0.9 V.**

5.5.2. Impact of gate length on drive current

From the 2D mapping of the BTBT generation in Figure 5.20b it is clear that the Tip-TFET architecture produces only lateral BTBT and not vertical BTBT. This is definitely verified in Figure 5.21 which illustrates the on-current for different gate lengths. The Tip-TFET presents the same behavior as the standard TFET, indicating that the current is independent on gate length. For a particular body thickness (T_{Si} = 4 nm), the Tip-TFET shows a slightly increase of the on-current in comparison to the standard TFET due to the presence of the embedded tip source. However, for both architectures the tunneling current is considerably smaller than in the ES-TFET and the PB-TFET for long gate devices (L_G > 100 nm), and in the same range for short gate devices (L_G < 100 nm). The Tip-TFET exhibits an increase of on-current for larger channel thicknesses, which is related with the electric field peak position (in all the cases 2 nm below the front gate). This set-up seems to maximize the on-current for a body thickness of 11 nm, but for T_{Si} = 4 nm it is necessary to located the peak closer to the gate, otherwise the on-current is reduced.

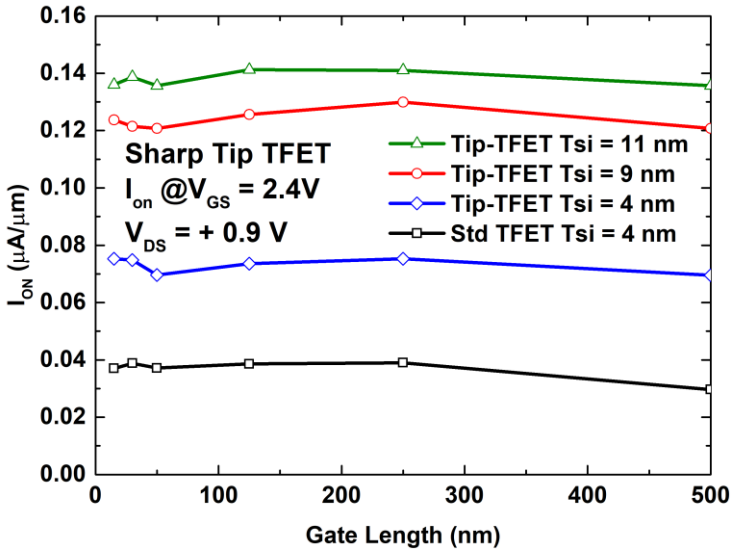

Figure 5.21. $I_{ON}(L_G)$ **for Sharp Tip-TFET with different** T_{Si} **and standard TFET with** T_{Si} **= 4 nm.**

5.6. SiGe TFETs

The PB-TFET exhibits the highest tunneling current among all the simulated architectures. So far the TCAD study was carried out for silicon homojunction structures. In this section, additional simulations have been run using SiGe material with different germanium concentrations (30%, 50% and 100%) to evaluate possible performance improvements in homojunction structures. TFET TCAD simulations with materials other than silicon are particularly challenging, due to the change in the effective masses for the valence and conduction bands. They modify the values of the parameters that set up the BTBT generation rate in the simulator. These new values have been obtained from literature [33] for unstrained SiGe (Ge at 30% and 50%) and pure germanium. For both materials [110] is the tunneling direction.

5.6.1. Pure Boron and Standard TFET

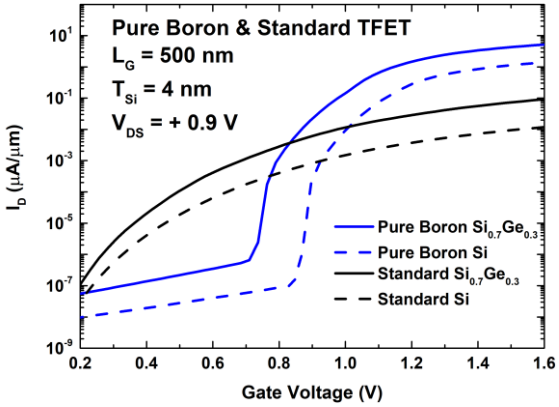

Figure 5.22. $I_D(V_G)$ curves of PB-TFET and standard TFET for Si and $Si_{0.7}Ge_{0.3}$ (T_{Si} = 4 nm). The tunneling current is enhanced for $Si_{0.7}Ge_{0.3}$ TFET in both architectures.

Results in Figure 5.22 show that using $Si_{0.7}Ge_{0.3}$ instead of silicon significantly increases the drain current in both Pure Boron and standard TFET architectures. In particular for T_{Si} = 4 nm, the performance of PB-TFET is higher and the slope is also steeper. Simulations are consistent with experimental data already obtained for SiGe TFETs [34]. Due to the relatively wide bandgap, silicon is not the best material to increase the tunneling probability even when architecture boosters are taken into account.

Simulations for $Si_{0.5}Ge_{0.5}$ TFETs (Figure 5.23a) show a better on-current because of a reduced bandgap in comparison to $Si_{0.7}Ge_{0.3}$. However, the off-current is also increased because a lower bandgap induces a higher tunneling current in the channel/drain junction. This implies a small I_{ON}/I_{OFF} ratio and a degradation of the subthreshold slope. Using pure germanium, in contrast with their silicon counterparts, shows an outstanding increase of the on-current (Figure 5.23b). The germanium PB-TFET exhibits an increase by one order of magnitude (drain current higher than 10 μA/μm) and the germanium standard TFET an improvement of two orders of magnitude. Unfortunately, the increase of the off-current is severely pronounced and completely degrades the subthreshold slope as shown in Figure 5.23b. Our results reveal that in order to enhance the tunneling current it is necessary to reduce the energy bandgap in the source/channel junction and in the extended region into the

channel. Also, to avoid the off-current degradation a higher bandgap is suitable in the drain region, which could be achieved with heterojunction architectures. Using materials with a high forbidden bandgap (like silicon) will keep low the off-current and a steeper subthreshold slope will be obtained. Currently, it is possible to process standard SiGe TFETs with a germanium concentration of 30% via a well-controlled technology fabrication. However, if the germanium concentration is increased beyond 30% the capability of the silicon platform to implement compound materials does not provide enough quality and a large concentration of defects may affect the SiGe layers. Therefore, the tunneling mechanism will be dominated by TAT and not by the interband tunneling, degrading the subthreshold leakage and the SS cannot be lower than 60 mV/dec.

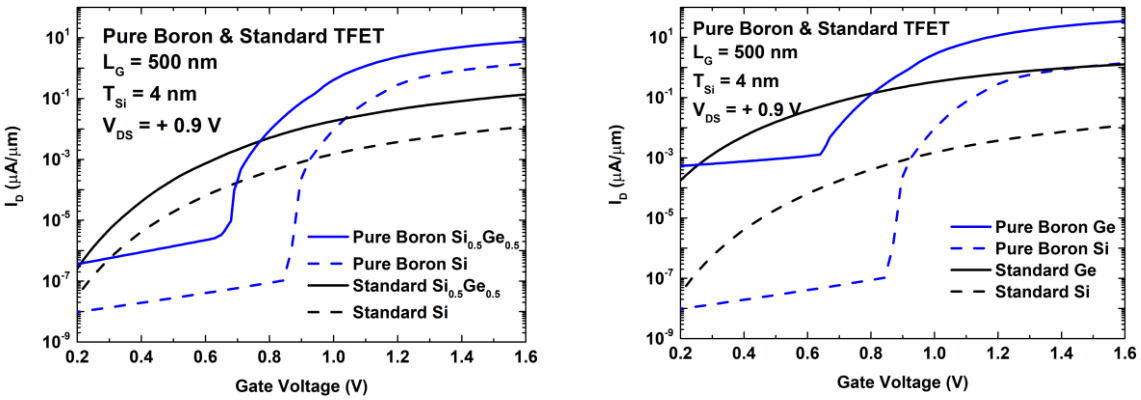

Figure 5.23. $I_D(V_G)$ **curves of PB-TFET and standard TFET (**T_{Si} **= 4 nm): (a)** $Si_{0.5}Ge_{0.5}$ **and (b) pure germanium. Tunneling current is enhanced for a higher Ge concentration, but the off-current is degraded.**

The SS extractions for the standard TFET, with different Ge concentrations (Figure 5.24a), exhibit a shift towards higher drain currents and an improved SS with respect to the silicon case. In particular, for a pure Ge standard TFET, SS reaches values below 60 mV/dec until $I_D = 10^{-5}$ µA/µm. The PB-TFET shows (Figure 5.24b) a shift in the SS for higher drain currents, when increasing the Ge concentration. For low I_D (< 10^{-3} µA/µm), better SS results below 60 mV/dec are obtained for lower Ge concentrations. On the contrary, for higher I_D (> 10^{-2} µA/µm) SS is reduced using pure Ge. However, the range for which SS is lower than 60 mV/dec is minimized compared to standard TFET. It is expected that using a material in the drain region with a larger energy bandgap will allow to reach SS below 60 mV/dec for several decades of current when increasing the Ge concentration in source and channel regions.

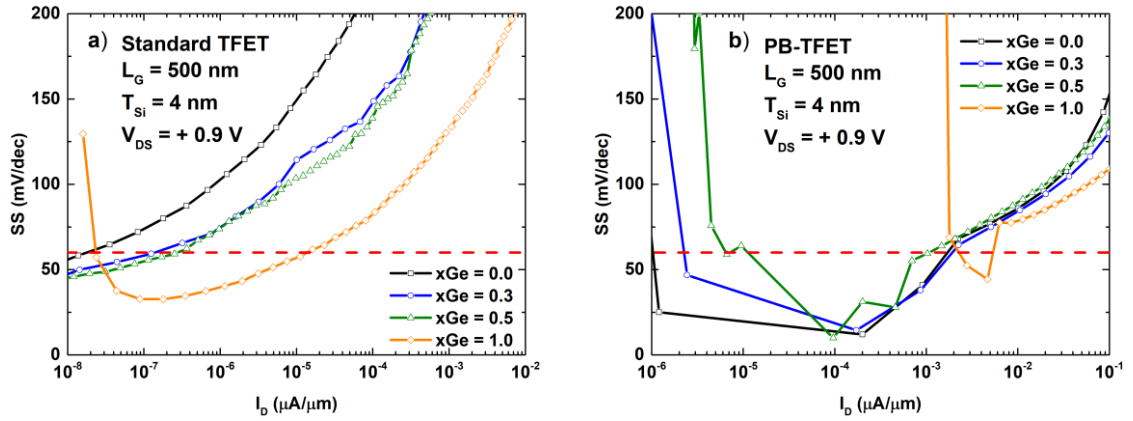

Figure 5.24. SS versus drain current curves with different germanium concentration for long gate devices (500 nm) with T_{Si} **= 4 nm: (a) Standard TFET and (b) Pure Boron TFET.**

5.6.2. Impact of gate length and body thickness in the drive current

In this section we explore the impact of the gate length reduction on current and the extension of vertical BTBT for PB-TFET architecture with different film thicknesses and germanium concentrations.

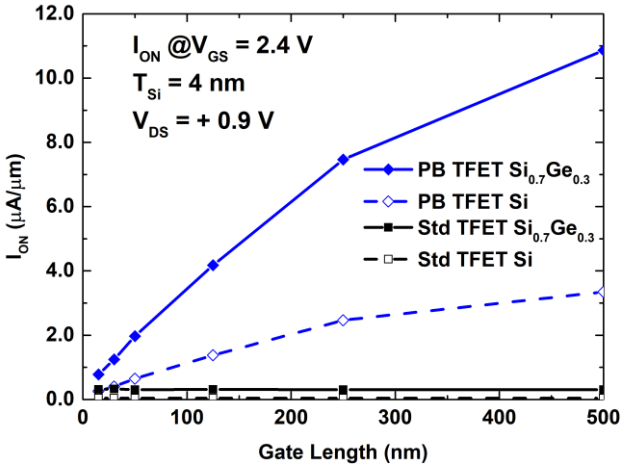

Figure 5.25. $I_{ON}(L_G)$ for standard and Pure Boron $Si_{0.7}Ge_{0.3}$ TFETs with T_{Si} = 4 nm. Even for short gate lengths, PB $Si_{0.7}Ge_{0.3}$ TFET shows higher on-current than the standard TFET.

Figure 5.25 shows that for a film thickness of 4 nm and a gate length of 500 nm the silicon PB-TFET presents good on-current (~ 3.3 μA/μm). But as explained before, for shorter gate lengths the tunneling current decreases due to the reduction of the extended source area. Nevertheless, the excellent electrostatic control due to the narrow thickness allows to extend the benefits of the vertical BTBT even at short gate lengths (L_G < 100 nm). For the standard architecture using $Si_{0.7}Ge_{0.3}$ material, there is only a slightly enhanced current. In the PB-TFET there is a significantly gain of on-current with respect to the silicon variant. This advantage is visible for all considered gate lengths at T_{Si} = 4 nm (Figure 5.25).

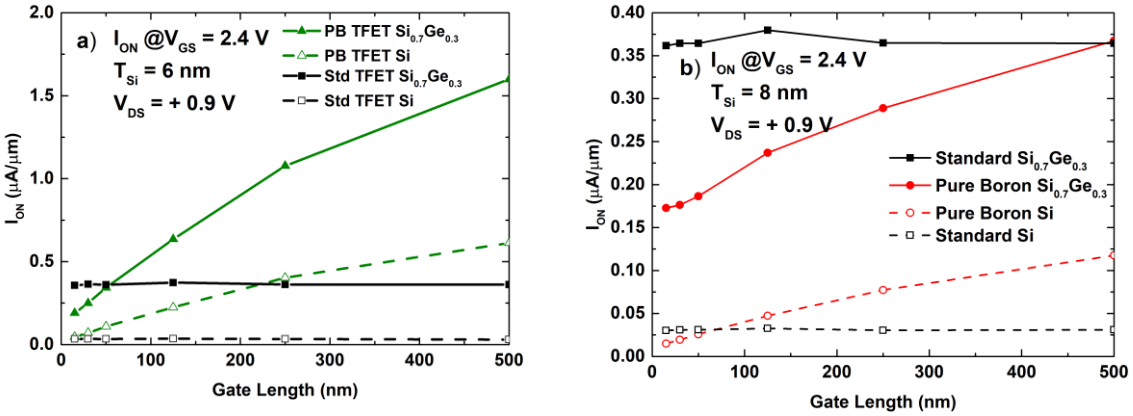

Figure 5.26. $I_{ON}(L_G)$ for standard and PB-TFET with silicon and $Si_{0.7}Ge_{0.3}$ materials: (a) For T_{Si} = 6 nm PB-TFET shows better performance except for shorter gate lengths (L_G < 100 nm) compared to the standard structure. (b) For T_{Si} = 8 nm $Si_{0.7}Ge_{0.3}$ PB-TFET is completely degraded for all gate lengths.

Increasing the channel thickness from 4 nm to 6 nm implies a wider tunneling length for the PB-TFET, and therefore a reduction of the tunneling current. For silicon PB-TFET the vertical BTBT is still higher than the lateral tunneling of the standard TFET even for short gate lengths (Figure 5.26a). However, when using $Si_{0.7}Ge_{0.3}$ material, the Pure Boron

architecture starts to show a loss of electrostatic control. For shorter gate lengths (L_G < 50 nm), it exhibits actually a lower on-current than the standard TFET with $Si_{0.7}Ge_{0.3}$.

This trend is accentuated with T_{Si} = 8 nm (Figure 5.26b) because the tunneling length is too large and on-current is severely degraded. In the case of silicon, the vertical BTBT of the PB-TFET architecture dominates over the standard TFET only for long gates, but for short gates (L_G < 100 nm) the current is degraded in comparison with lateral tunneling. Using $Si_{0.7}Ge_{0.3}$ material does not improve the on-current enough even at L_G = 500 nm where the standard TFET presents the same current as the PB-TFET architecture, simply because the device is too thick.

5.6.3. Impact of gate length for different germanium concentrations

The PB-TFET architecture with silicon film and 8 nm body thickness remains superior to standard TFET for long and medium gate lengths (> 50 nm). However, when using compound materials like $Si_{0.7}Ge_{0.3}$ the on-current is lower than for a standard TFET and there is no advantage of vertical BTBT compared to lateral BTBT, even with a gate length of 500 nm (Figure 5.26b).

We have performed simulations of PB-TFETs and standard TFET with either SiGe (50 % concentration) or pure germanium, in order to investigate if the vertical BTBT dominates or not in 8 nm thick films. Using $Si_{0.5}Ge_{0.5}$ compound we obtain better on-currents for PB-TFETs for gates longer 250 nm (Figure 5.27a). On the other hand, for germanium the tunneling current is significantly increased and the vertical component dominates for all gate lengths exceeding 50 nm (Figure 5.27b). Due to the complexity to fabricate $Si_{0.5}Ge_{0.5}$ or pure germanium layers with low density of defects, we explore the benefit of body thickness, expected to enable higher on-current for reduce germanium concentration.

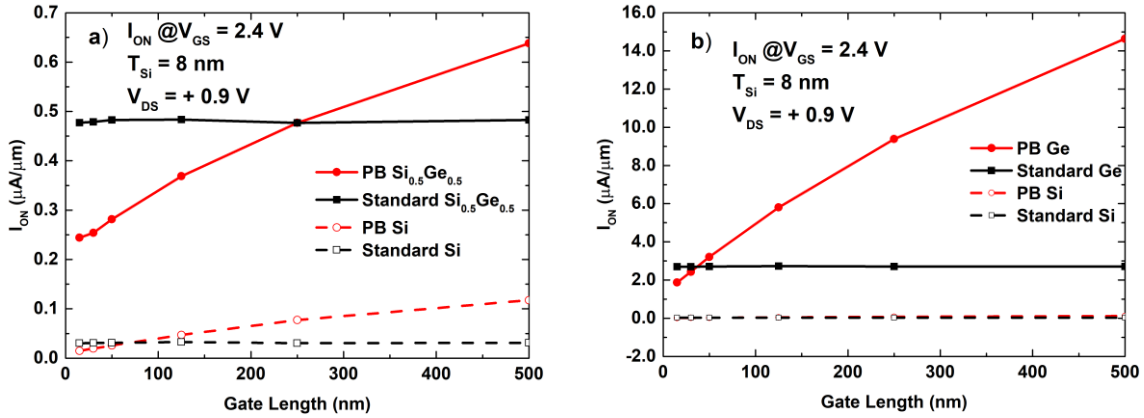

Figure 5.27. $I_{ON}(L_G)$ for standard and Pure Boron TFETs architectures with T_{Si} = 8 nm: (a) for a germanium concentration of 50%; (b) for pure germanium.

Thinning down the body from 8 nm to 6 nm results in an increase of the tunneling current for both $Si_{0.5}Ge_{0.5}$ and pure germanium. Nevertheless, for $Si_{0.5}Ge_{0.5}$ it is not possible to extend the prevalence of vertical BTBT beyond a gate length of 50 nm (Figure 5.28a). In the case of the germanium PB-TFET, because of the narrow bandgap, the vertical tunneling dominates even for extremely short gate lengths (L_G = 30 nm) as shown in Figure 5.28b.

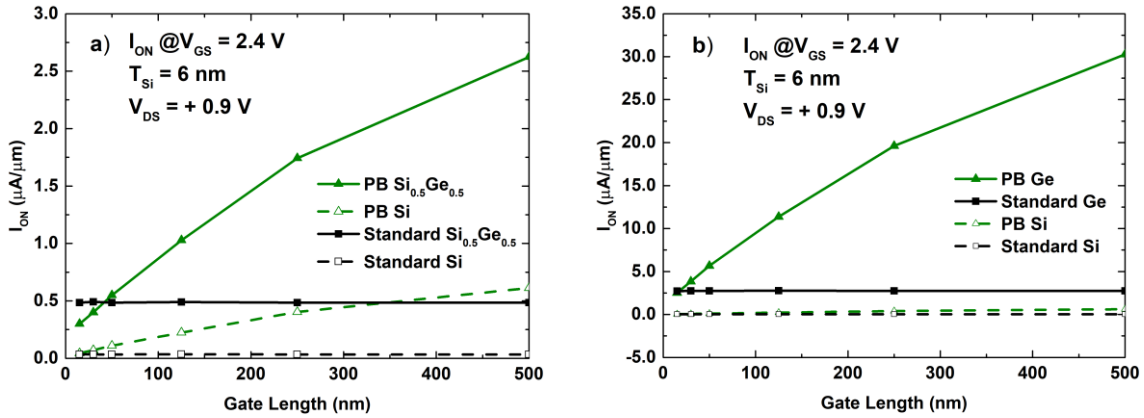

Figure 5.28. ***$I_{ON}(L_G)$*** **for standard and PB-TFET architectures with 6 nm body thickness: (a) with $Si_{0.5}Ge_{0.5}$ material; (b) with pure germanium.**

The same trend is obtained for a 4 nm body thickness. It is remarkable that a reduction in thickness by 2 nm leads to 2-6 fold increase of the drive current. The outstanding electrostatic control is responsible of the dominance of vertical BTBT over the lateral tunneling for very short gate lengths (L_G < 50 nm) when using $Si_{0.5}Ge_{0.5}$ material (Figure 5.29a). For germanium, simulation results are even much better (Figure 5.29b) for all the studied gate lengths. These results indicate that TFETs with architectures based on vertical BTBT, require an extremely narrow channel thickness (T_{Si} < 6 nm) and a small bandgap in the source and channel regions, in order to benefit from increase of tunneling current.

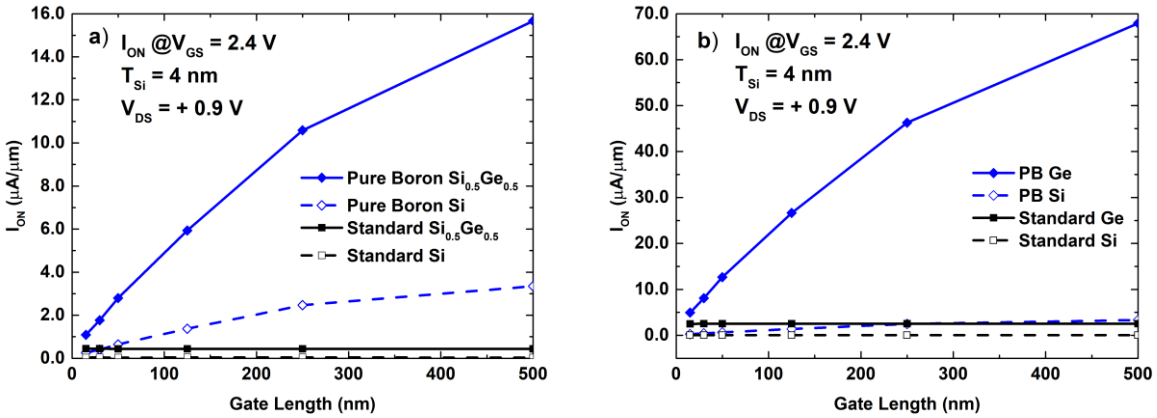

Figure 5.29. ***$I_{ON}(L_G)$*** **for standard and PB-TFET architectures with 4 nm body thickness: (a) with $Si_{0.5}Ge_{0.5}$ material; (b) with pure germanium.**

5.7. Conclusions

This Chapter introduces a thorough TCAD study of three innovative Tunnel FETs architectures. The objective is to determine which solution allows to solve the recurrent issue of low on-current and degraded subthreshold slope in the standard TFET structure. The Extended-Source TFET (ES-TFET) is characterized by the extension of the source in the intrinsic channel region. With this geometry, the vertical BTBT component benefits of extended tunneling area and hence the tunneling current is magnified with respect to the standard TFET (lateral tunneling). The main parameter for this innovation consists in optimizing the distance between the extension and the gate oxide (L_{rt}). The transfer characteristic shows, for a relatively thick body of 11 nm, a high on-current and a stepper SS below 60 mV/dec (over 4 decades of current) for small values of L_{rt} (3 nm, 4 nm and 5 nm). A larger L_{rt} causes a longer tunneling length and on-current degradation due to a lower effective electrostatic control from the front gate. The ES-TFET shows a better performance than the standard TFET for long and medium gate lengths, but for gate smaller than 100 nm the reduction of the tunneling surface jeopardizes the on-current enhancement.

The implementation of an extremely thin layer of heavily doped boron (10^{21} cm^{-3}) takes advantage of the Pure Boron technology for small body thickness (T_{Si} < 6 nm) to solve the on-current degradation for small gate lengths (L_G < 100 nm). There is an increase of the vertical BTBT due to a small tunneling length and better electrostatic control. This implies a higher on-current compared to the ES-TFET and standard TFET architectures. The body thickness is a key parameter for the PB-TFET performance. In thicker channel thickness (T_{Si} > 7 nm), the effect of the pure Boron layer is attenuated.

The design of a sharp tip in the source junction is based on the implementation of embedded source and drain junctions developed in CMOS technology to improve the strain characteristic and the performance. However, TCAD results show that this architecture does not significantly impact the on-current and subthreshold slope, hence the benefit is marginal. Even though the electric field can be enhanced with this tip configuration, the tunneling area does not increase which explains why similar performance as the standard TFET is obtained.

TCAD simulations based on SiGe compounds and pure germanium for Pure Boron TFET and standard TFET present an increase of the tunneling current, when compared to silicon. The thinner the body thickness (down to T_{Si} = 4 nm), the higher the on-current for PB-TFETs. Furthermore, the benefits of the vertical BTBT are extended for short gate lengths (L_G < 50 nm). If the body thickness is increased (6 nm or 8 nm), a higher concentration of germanium is required to compensate a large tunneling length. However, the complexity of SiGe or Ge device fabrication can produce a higher density of defects, and thus TAT mechanism can preclude the devices from achieving a SS lower than 60 mV/dec.

From this exhaustive TCAD study we can conclude that the most promising architecture for technological implementation appears to be the Pure Boron TFET with the thinnest body thickness possible and a heterojunction structure. A reduced bandgap in the source and the channel regions will enhance the on-current and a large bandgap in the drain region will keep a low off-current and good I_{ON}/I_{OFF} ratio.

The key messages of this chapter are: First, the **standard TFET architecture with T_{Si} > 10 nm cannot provided a good tunneling current and steep slope simultaneously**. Secondly, the **extension of the source junction into the channel region generates vertical BTBT**. Besides, a **small extension depth (L_{rt}) allows one to obtain a steep subthreshold slope**. However, reduction of channel length jeopardizes the increase of the tunneling current. Next, the implementation of **ultrahigh boron doping concentration in a thin bottom layer improves the drive current with a steep slope for ultra-thin channel thickness** (T_{Si} < 7 nm). Finally, it is necessary to use **more talented materials in source and channel regions to increase the tunneling probability**, but for the **drain junction we need large bandgap materials** to keep under control the leakage current and maintain a good I_{ON}/I_{OFF} ratio.

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General conclusions

The work presented in this thesis manuscript is focused on the electrical characterization, TCAD simulation and defect density studies, in planar and trigate Tunnel FET FDSOI devices. The lack of a competitive performance of TFETs compared to current MOSFETs, calls for a thorough and extensive research of the mechanisms that jeopardize full interband tunneling operation. In addition, 3D sequential integration (CoolCube^{TM}) uses novel, low-temperature process steps for top tier device fabrication. It is important to know if the use of a low thermal budget leads to devices that have degraded performances. In this Thesis, we provide the most likely perspectives and challenges for TFET technology made using the low thermal budget of a 3D monolithic integration process. Combining 3D monolithic integration with low-voltage, low-power TFET technology could become an important breakthrough for ultra-low power integrated circuits.

The starting point of the manuscript (Chapter 1) gives a general overview of the current status of silicon technology and integrated circuits design. While silicon transistor scaling it is still done in a cost-effective way due to boosters, the change of paradigm in ICs impose very restrictive design rules to meet modern requirements of power consumption and global IC delay. Reduction of power consumption at constant performance requires one to decrease the supply voltage and the threshold voltage. The latter can unfortunately not be reduced due to the non-scalability of the subthreshold slope below 60 mV/decade. The reason is that thermionic emission prevents to achieve a sub-thermal subthreshold slope. Ultra-low power applications required devices based on physics that is different from that of MOS transistors, in order to obtain a SS below 60 mV/dec. The steep slope devices presented in this Chapter usually exhibit better on-current and steep subthreshold slope than TFETs. However, they also show some important drawbacks such as hysteresis effect, large supply voltages and large footprint. TFET devices, on the other hand, do not present these limitations. Moreover, its process fabrication is fully compatible with CMOS, such that both technologies can be co-integrated.

An exhaustive description of Tunnel FET devices can be found in Chapter 2. Interband tunneling, which governs the operation mechanism in TFETs, is detailed by equations confirming the theoretical capability of this technology to achieve a steep slope. Unfortunately, the discrepancy between simulations and experimental results reveal that a great number of secondary orders effects were most likely not taken into account in past simulated structures. In particular, trap-assisted tunneling (TAT) is identified as the main effect that prevents the device to achieve simultaneously a good on-current and a sub-thermal subthreshold slope. A TCAD study on the impact of different parameters via indicates that EOT reduction and the use of a very small body thickness enhance the control of the gate on the BTBT triggering mechanism. Moreover, for gate lengths shorter than 30 nm the gate terminal shows inability to switch off the device, because the drain voltage perturbs the control of BTBT at low gate voltages. The implementation of an intrinsic region near the

drain side is shown to reduce ambipolarity, which is necessary for use in memory applications. However, innovative structures approaches are required to avoid an increase of the gate pitch in current technology nodes. Successive TFET generations have been fabricated at CEA based on the principles of co-integrability with MOSFETs and same optimization boosters (SiGe or Ge layers, strained technology, nanowire structures etc.) to guarantee process fabrication compatibility. Other TFET investigations, on the other hand, present more disruptive approaches in terms of materials, process fabrication and structures, for example with III-V compounds and 2D materials. However, different benchmark exercises show that these state-of-the-art TFETs have a higher on-current, but a degraded off-current and SS due to the immaturity of the integration of innovative BTBT materials onto standard CMOS process fabrication (due to low quality of epitaxy growth and, therefore, high defect density).

In Chapter 3 we have performed the electrical characterization in P-mode configuration of TFETs fabricated with two different annealing temperatures: conventional High-Temperature (HT) at 1050°C and Low-Temperature (LT) at 630°C. This allows one to determine the feasibility to build TFETs in the top tier of 3D sequential integration process. The "Dual I_DV_D" technique has confirmed the TFET behavior in wider structures (W_{fin} = 1.0 µm) used in this chapter. However, for narrow structures (W_{fin} = 30 nm) LT devices present a complete Schottky FET behavior, while HT devices show characteristics comprised between those of a TFET (at high gate voltage) and a Schottky FET (for low gate voltage). The low performance measured in HT TFETs (2.3×10^{-2} µA/µm) suggest that silicon body is not the best choice, and there are better BTBT materials such SiGe or Ge with a lower energy bandgap that increases tunneling probability. The performance exhibited by LT TFETs (5.7×10^{-2} µA/µm) is comparable to that of HT devices, however a degradation of the off-current and a drive current enhancement are noticed, not because of BTBT effect but most likely due to a higher density of defects that are not annealed out at low temperature. In addition, a V_{TH} reduction by ~0.3 V is observed for LT TFETs compared to HT devices. For MOSFETs fabricated in the same batch, the V_{TH} shift is only ~0.1 V as consequence of the impact of different thermal budgets on the EOT. The hypothesis is that in TFETs the combination of TAT current increase and the presence of more abrupt tunnel junction region due to lower dopant diffusion in LT TFET are the phenomena involved in this V_{TH} shift. In fact the severe degradation of the subthreshold swing for both HT/LT devices (beyond 60 mV/dec) indicates that parasitic mechanisms influencing BTBT are making it impossible to achieve a steep subthreshold slope. TCAD simulation of temperature dopant diffusion and junction abruptness in underlapped (LT) and overlapped (HT) source junctions, based on a full silicon homojunction structure, shows a trend matching experimental results. Finally, the study of the impact of fin width on device performance shows that the tunneling current increases when as the fin width is decreased, which increases the effective electric field and gives better control of the BTBT. TCAD study shows that in wider devices the tunneling generation region is located at the corners and the effect of varying of the top width (trigate structure) is reduced. When W_{fin} is significantly reduced, the top contribution starts to be more important and the current increases. This is an indication of the great capabilities of trigate/nanowire multi-channel structures to achieve a good on current for TFETs.

In Chapter 4 charge pumping (CP) measurements and low-frequency noise (LFN) analyses confirm that TAT in the tunneling junction is the main factor limiting the performances of our TFETs.

CP current (I_{CP}) is the result of recombination of holes with electrons released from traps at a semiconductor-oxide interface. Devices studied in Chapter 3 present a higher I_{CP} for LT than HT process, regardless of the applied back-gate voltage to limit the scanning of the body bottom. This indicates a higher presence of defects (oxide traps) at the top surface. Using $I_{CP,max}$ it is possible to calculate the average defect density N_{it} via the "slope calculation" technique to guarantee a full bandgap scanning at the front-interface. We obtain a higher average defect density in LT TFETs (~1.5×10^{11} $cm^{-2}eV^{-1}$) than for HT devices (~7.0×10^{10} $cm^{-2}eV^{-1}$). Others extraction methods provide also the same trend but with an underestimated N_{it}, because depending of the pulse base level ($V_{G,base}$) the amplitude of the pulse is not enough to scan the front interface in the whole range, yielding a lower I_{CP} and thus, a lower N_{it}. Moreover, different TFET structures were tested for different widths and the LT TFETs always exhibit a higher defect than HT TFETs. The study of the top and bottom carriers concentration at $V_{G,base}$ and $V_{G,top}$ allows us to connect the trend of both of them with the measured I_{CP}. The idea is that either one of these concentrations decreases when the gate voltage is more negative (fewer electrons) or more positive (fewer holes) at the top interface modifying the I_{CP}.

The identification of defects nature in LT and HT processes is done with the LFN measurements in a more accurate way. The input-referred gate voltage S_{Vg} presents for LT TFETs higher values than for HT devices and also a progressive increase with V_G, an indication of defect density increase at the junctions that gives place to a higher series resistance noise. The analysis of the average drain current noise spectra shows a non *1/f* behavior for LT TFETs which reveals a non-uniform distribution of traps in the oxide region and most likely the presence of additional defects in the junctions. HT TFETs, on the other hand, present a *1/f* behavior which indicates a homogeneous defect distribution along the top surface. Therefore, a higher defect density at the tunneling junction implies that are more paths available for the carriers to tunnel through TAT instead of BTBT and the inability to achieve a steep slope. The surface-normalized input-referred gate voltage noise is two orders of magnitude higher than the MOSFET noise for same technology wafers, due to the different noise sources in the two types of carrier injection mechanisms. This indicates the importance of very good-quality epitaxy layers and extra process fabrication steps to obtain abrupt and defect-free junctions to limit TAT, which are not mandatory for MOSFETs but are essential in TFETs. The reduction of fin width in HT TFETs shows an increase in S_{Vg} noise similar to the case of LT TFETs. Maybe there are not more defects than for a wider structure, but the smaller surface enhances the junction defects impact on the LFN. If this issue is not solved, could reduce the possibilities of TFETs to be considered as a feasible candidate for 3D Power scaling, because it will severely degrade the performance. Finally, the increase of environment temperature demonstrates that the enhancement of the drive current is due to TAT, which is temperature dependent, and not because of BTBT (which is independent of temperature).

Finally, Chapter 5 introduces an extensive TCAD study based on the proposal of innovative planar architectures aiming at simultaneously achieving a steep slope and high on current. The problem of conventional TFET architectures with lateral tunneling, is due to the fact that the tunneling generation area is located at the corners of the top surface in a limited region of ~10 nm nearby the tunneling junction. As seen in previous chapters the use of innovative BTBT materials allows one to increase the tunneling current, but the quality of layers and junctions is reduced, which eliminates the possibility of achieving a steep subthreshold slope.

The extension of the source into the whole channel region in a TFET architecture with T_{Si} = 11 nm, increases the current thanks to a large tunneling area. For extension depths (L_{rt}) smaller than 5 nm, the gate terminal presents a very efficient control to trigger the BTBT mechanism and makes it possible to achieve very steep subthreshold slopes. However, for longer values of L_{rt} the tunneling distance increases, which degrades the slope. The comparison with a standard TFET, shows that is possible to extend the benefit of the vertical BTBT for large and medium gate lengths, but for L_G shorter than 100 nm the shrinking of the tunneling surface compromises the on-current enhancement. The only possibility is to extend the positive impact below 100 nm is to user a thin layer in the body region (8 nm, 6 nm). The implantation of this architecture would however be associated to several challenges, because the implant of the source extension will damage the body region and the passivation have to anneal out the majority of defects. Moreover, with the current maturity level of technology it would be extremely challenge to achieve an accurate extension depth below 5 nm, due to dopant diffusion in the annealing process. We suggest that ultra-thin heavily doped boron layers (10^{21} cm^{-3}) fabricated with Pure Boron technology have the capabilities to extend the benefits of the vertical BTBT for small gate lengths (L_G < 100 nm) for very small film thicknesses (T_{Si} < 6 nm) and achieving higher on-current than in the previous structure. Indeed, the TCAD study confirms that body thickness is a key parameter, because in relatively “thick” films (T_{Si} > 7 nm) the effect of the Pure Boron layer in the performance is reduced. The last proposed structure is based on the tip shape that presents the junctions when strain technology is used to enhance the performance of CMOS devices in P-mode configuration. However, simulations indicate the low impact on the on-current and subthreshold slope with respect to the standard TFET. Despite of the junction electric field is increased, the tunneling are does not increase and no significant benefit is obtained. The impact of the body material in TCAD analysis, reveals that small bandgap materials present higher tunneling current, but also a degraded off-current that affects the performance. An intrinsic region near the drain junction complemented with a higher bandgap material in drain junction implementation provide a low off-current. Therefore, an ultra-thin film layer combined with a heterojunction structure enable the options to achieve a good I_{ON}/I_{OFF} ratio and a steep subthreshold slope simultaneously. It is important to notice that introduction of these BTBT materials in process fabrication requires an excellent quality of the epitaxy layers, otherwise TAT will suppress the possibility to obtain sub-thermal subthreshold slope.

The most important key learnings acquired in this research and the perspectives of the TFET technology are:

1. **Main constraints for good Tunnel FET operation are related with the maturity of current CMOS fabrication process.**
    a. TFET devices required ultra-thin film layers (T_{Si} < 10 nm) to efficiently trigger the BTBT mechanism.
    b. New lower-bandgap BTBT materials in the channel are necessary: SiGe or Ge.
    c. Exhaustive control of gate deposition and junction implementation is essential to reduce TAT at low gate voltage operation.
    d. Conventional CMOS process fabrication is not enough for TFET fabrication.
    e. More processing steps are mandatory to build low-defect abrupt junctions.

2. **Trigate and nanowire architectures enhance the BTBT.**
    a. In current planar structures, BTBT is located at the top corners and the contribution of the top width is limited.
    b. For very narrow fins, the BTBT takes place in the whole film thickness.
    c. Multi-channel structures are key to achieve a good TFET on-current.

3. **Opportunities in 3D Power scaling will determine the feasibility of TFET technology.**
    a. Demonstration of functional LT TFETs.
    b. 95% of top tier LT MOSFETs are as good as HT devices.
    c. New epitaxy growth techniques for top tier (with low thermal budget) and bottom tier are necessary to reduce defect density at the junctions, responsible of degrading the subthreshold slope.

4. **TFET applications**
    a. TFETs are not going to replace High-Performance CMOS as the basic building block in the circuitry logic.
    b. TFETs present advantages in logic performance compared to MOSFETs for bias supply lower than V_{DD} < 0.4 V.
    c. Any TFET solution that difficult the co-integration with MOSFETs will not be adopted by the semiconductor industry. The path followed at CEA with TFET fabrication, has been so far the right one.
    d. Microprocessors with multi-core configuration and multi-parallelism can take advantage of TFETs when running specific background tasks.
    e. All the research and proposed solutions for TFETs in this thesis manuscript are focus for circuit logic. TFETs have also interest for memory and electrostatic discharge (ESD) applications, but are out of the scope of this work.

Author publication list

International conferences articles

"First SOI Tunnel FETs with Low-Temperature Process"

C. Diaz Llorente, C. Le Royer, C-M. V. Lu, P. Batude, C. Fenouillet-Beranger, S. Martinie, F. Allain, M. Vinet, S. Cristoloveanu and G. Ghibaudo. In 2017 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), April 2017, Athens, Greece.

"Innovative Tunnel FET architectures"

C. Diaz Llorente, S. Martinie, S. Cristoloveanu, J.-P. Colinge, C. Le Royer, G. Ghibaudo, J. Wan and M. Vinet. In 2018 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), March 2018, Granada, Spain.

"Impact of Low-Temperature CoolCube^{TM} Process on the performance of FDSOI Tunnel FETs"

C. Diaz-Llorente, J.-P. Colinge, C. Le Royer, M. Vinet, C.G. Theodorou, S. Cristoloveanu and G. Ghibaudo. In 2018 IEEE SOI-3D-Subthreshold microelectronics technology unified conference (S3S), October 2018, San Francisco, United States.

Journal articles

"New insights on SOI Tunnel FETs with low-temperature process flow for CoolCube^{TM} integration"

C. Diaz Llorente, C. Le Royer, P. Batude, C. Fenouillet-Beranger, S. Martinie, C-M. V. Lu, F. Allain, J.-P. Colinge, S. Cristoloveanu, G. Ghibaudo and M. Vinet. In 2018 Solid-State Electronics Journal, vol. 144, pp.78-85, June 2018.

"New prospects on high on-current and steep subthreshold slope for innovative Tunnel FET architectures".

C. Diaz Llorente, J.-P. Colinge, S. Martinie, S. Cristoloveanu, J. Wan, C. Le Royer, G. Ghibaudo and M. Vinet. In 2018 Solid-State Electronics Journal. Submitted.

Résumé du travail de la thèse en français

Le travail décrit dans cette thèse porte sur l'étude de transistors à effet tunnel (TFETs) en FDSOI à géométries planaire et triple grille/nanofils. Le but est d'explorer le potentiel des TFETs en silicium et à source/drain en SiGe pour applications ultra-basse puissance. La thèse vise aussi à identifier les problèmes fondamentaux qui peuvent empêcher l'intégration de TFETs performants dans une technologie CMOS.

Chapitre 1. Contexte de la thèse et dispositifs "post-CMOS"

La réduction de la taille des transistors a permis d'améliorer les performances et de diminuer la puissance consommée, génération technologique après génération technologique. Pour contrecarrer les effets canaux courts, de nouveaux matériaux et de nouvelles architectures de transistors telles que le FDSOI ou les transistors multigrilles (FinFET, nanofil) ont dû être adoptés. Les contraintes imposées aux microprocesseurs requièrent non seulement une haute performance en vitesse d'exécution, mais aussi d'atteindre cette performance en dissipant le moins de puissance possible. Malheureusement, la simple réduction de la taille des transistors ne permet pas (ou plutôt, ne permet plus) d'atteindre ces buts. Pour atteindre les basses consommations il faut réduire la tension d'alimentation V_{DD}, à 0.4V ou moins, ce qui tue les performances en vitesse des circuits CMOS logiques ou crée des courants de fuite énormes. En pratique, il est pratiquement impossible de réduire la tension d'alimentation (à performance constante) en-dessous de 0.7-0.8 V. Ceci est dû à la physique du transistor MOS, et en particulier à la distribution Fermi-Dirac des porteurs dans les bandes d'énergie, et au mécanisme d'injection de ces porteurs par émission thermoïnique par-dessus la barrière de potentiel entre la source et le drain. A cause de ces 2 facteurs, la pente sous seuil à une valeur minimum de 60 mV/décade à T = 300K.

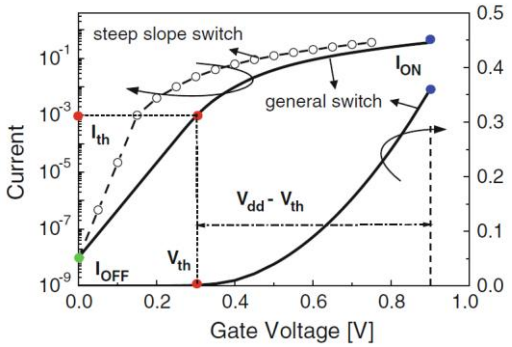

Figure 1. Courbes $I_D(V_G)$ d'un transistor MOS (général switch) et d'un interrupteur à pente sous seuil raide. La pente sous seuil raide permet de réduire la tension de seuil sans faire croître le courant de fuite [1].

La Figure 1 montre que réduire V_{DD} implique une réduction équivalente de la tension de seuil (V_{TH}) si l'on veut maintenir la performance (c.à.d. le courant) constant. Si la pente sous le seuil reste constante, une diminution de la tension de seuil entraîne une augmentation du

courant de fuite (I_{OFF}). De cette analyse succincte ressort que le transistor MOS n'est pas apte à fonctionner efficacement aux faibles tensions d'alimentation nécessaires pour les applications à puissance extrêmement basse (V_{DD} < 0.4 V). Il existe d'autres dispositifs "beyond CMOS", dont la physique n'est pas basée sur le franchissement d'une barrière de potentiel par mission thermoïonique, et qui sont capables d'atteindre une pente sous seuil plus basse que 60 mV/décade. Le fonctionnement de différents dispositifs qui sont candidats à produire une pente sous seuil raide De l'étude de tous ces dispositifs, il ressort que le TFET, malgré ses défauts, est le dispositif le plus pragmatique et le plus compatible avec la technologie CMOS. De surcroît, il est intégrable dans une technologie 3D monolithique.

Chapitre 2. Transistors à Effet Tunnel

Ce Chapitre analyse en détail les phénomènes physiques qui contrôlent l'injection de porteurs par effet tunnel. On y identifie également des phénomènes d'injection parasite qui dégradent les performances du TFET. Ce Chapitre brosse également un tableau de l'état de l'art en la matière.

La Figure 2a montre une coupe schématique d'un TFET fabriqué au CEA en technologie SOI et polarisée en opération à mode de type N. Le mécanisme d'émission tunnel de bande à bande (BTBT) est illustré dans le diagramme de bade de la Figure 2b. L'injection par effet tunnel se produit à la jonction entre la source P^+ et le canal.

Ce Chapitre souligne la différence qui est systématiquement observée entre les caractéristiques simulées et les caractéristiques mesurées des TFETs. The tunneling assisté par pièges (trap-assisted tunneling, TAT) est identifié comme étant le principal facteur qui empêche l'obtention d'une pente sous le seuil raide.

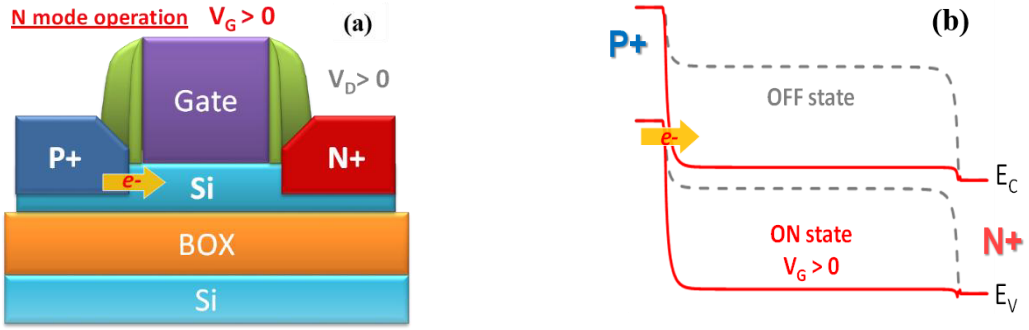

Figure 2. (a) Polarisation du TFET pour opération en mode de type N: tension positive sur la grille et sur le drain (cathode). (b) Diagramme de bandes d'énergie montrant l'état OFF (ligne pointillée) et l'état ON (ligne continue).

L'utilisation d'outils TCAD nous a permis d'identifier l'impact de différents paramètres tels que l'épaisseur du film SOI, la longueur de grille, la longueur de la zone intrinsèque près du drain, l'EOT et l'utilisation de matériaux à faible bande interdite, sur les performances du TFET. Ces informations définissent des lignes de conduite pour la conception de futur TFETs. La Figure 3a montre l'impact de l'épaisseur du film SOI T_{Si} sur les caractéristiques électriques: l'utilisation de films très fins (T_{Si} < 7 nm) augmente le courant de drain et améliore la pente sous le seuil. La Figure 3b montre que les TFETs qui ont une longueur de grille inférieure à 30 nm présentent une perte de contrôle électrostatique de la grille parce que la source et le drain sont trop proches l'un de l'autre. Les simulations révèlent que l'utilisation d'un oxyde de grille mince (EOT < 1nm) améliore le contrôle électrostatique, l'utilisation de

matériaux autres que le silicium peut accroître le taux de BTBT, et que la présence d'une région intrinsèque près du drain peut réduire le courant de fuite et le courant ambipolaire.

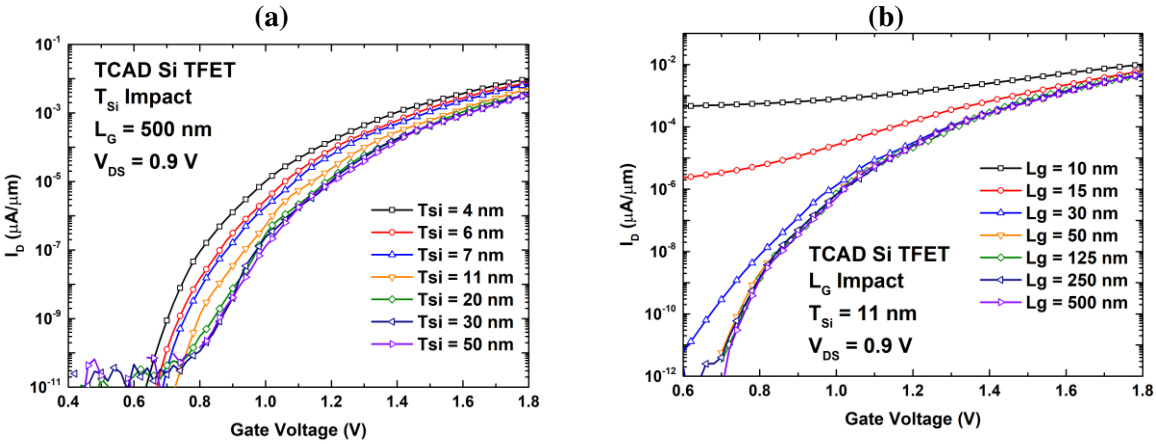

Figure 3. Courbes $I_D(V_G)$ simulées par TCAD montrant (a) l'impact de l'épaisseur du film SOI (T_{Si}); (b) l'impact de la longueur de grille (L_G).

Le Chapitre 2 donne des détails sur les structures des dispositifs fabriqués au CEA-LETI et sur leur processus de fabrication. La Figure 4 montre une des structures les plus innovantes: il s'agit d'un TFET réalisé sur un nanofil en SiGe avec une grille de forme Ω. Cette configuration permet un excellent contrôle électrostatique de la grille sur le canal. Les architectures de type nanofil avec triple grille améliorent les performances du TFET grâce à un contrôle électrostatique très efficace de l'enclenchement du BTBT. De plus, ces architectures sont compatibles avec une technologie CMOS. Ce Chapitre passe également en revue les résultats les plus intéressants obtenus sur les TFETs III-V et les TFETs réalisés en matériaux 2D. Il fournit également une comparaison de meilleurs TFETs publiés durant les 10 dernières années.

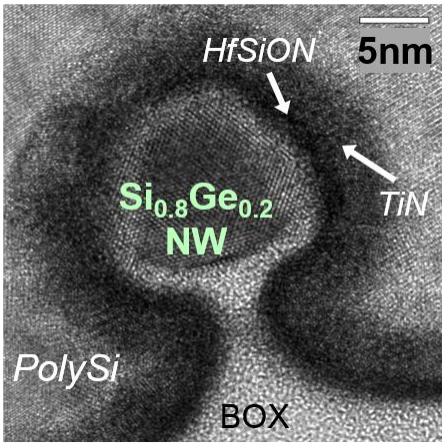

Figure 4. Coupe HRTEM d'un TFET réalisé dans un nanofil en SiGe [2].

Chapitre 3. TFETs fabriqués par un processus à basse température.

Ce Chapitre décrit les résultats de mesures effectuées sur des TFETs fabriqués par un processus basse température (600°C). Ce processus basse température est identique à celui utilisé pour l'intégration monolithique Coolcube^{TM}. L'activation des dopants de source et drain avec un faible budget thermique est réalisé par pré-amorphisation par implantation de Ge (PAI) suivi d'une recristallisation par épitaxie en phase solide (SPER) après l'implantation.

La méthode de mesures électriques “Dual $I_D(V_{DS})$”, utilisée sur des dispositifs larges (W_{fin} = 1.0 µm) confirme de façon expérimentale que les TFETs fabriqués par processus haute température (HT) et basse température (LT) fonctionnent bien par effet tunnel et non pas par effet Schottky.

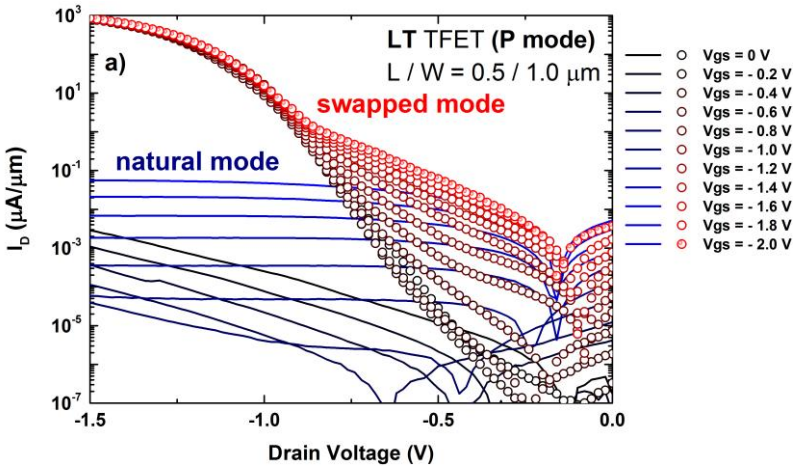

Figure 5. Exemple de mesures effectuées par la méthode "dual $I_D(V_{DS})$" sur des TFETs "basse temperature" d'une largeur de 1.0 µm, montrant que le courant est bien engendré par un mécanisme BTBT, et non par effet Schottky.

D'un autre côté, la même mesure effectuée sur des dispositifs étroits (W_{fin} = 0.03 µm) révèlent un courant par effet Schottky dans les TFETS LT. Dans les dispositifs HT on observe à la fois un comportement BTBT à forte tension de grille et Schottky à basse tension de grille (Figure 6b).

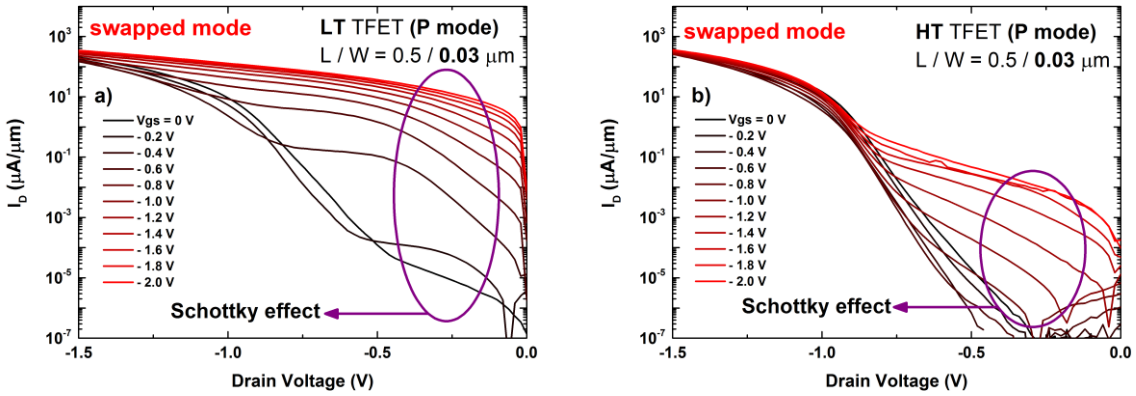

Figure 6. Résultats de mesures "dual $I_D(V_{DS})$" sur des diodes LT et HT. La largeur des diodes est de 0.03 µm. (a) Dans une diode étroite LT le courant est généré par effet Schottky; (b) Dans une diode étroite HT on observe une transition entre un transport Schottky à basse tension de grille et BTBT à forte tension de grille.

Les résultats de mesures présentés dans la Figure 7a montrent un fonctionnement en mode TFET bien défini. On peut également y voir que l'abaissement de la température de fabrication de 1050°C (HT) à 600°C (LT) ne dégrade pas les propriétés des TFETs. Il faut cependant noter que les dispositifs LT ont un courant de fuite plus élevé que les dispositifs HT. Ceci est probablement dû à la présence de défauts d'implantation qui n'ont pas été suffisamment recuits. On observe aussi que les dispositifs HT et LT ont des tensions de seuil différentes, probablement à cause d'une différence de position de la jonction de source. On voit sur la Figure 7b que tous les dispositifs ont une pente sous le seuil supérieure à 60

mV/décade, ce qui est plutôt normal puisque le processus de fabrication est optimalisé pour la fabrication de transistors MOS, et non pour les TFETs. Vu sous un angle plus positif, le procédé LT peut être modifié relativement facilement pour obtenir une zone de canal en SiGe ou en Ge de façon à augmenter l'effet tunnel. Il est aussi confortant de voir que les simulations TCAD collent relativement bien aux résultats expérimentaux.

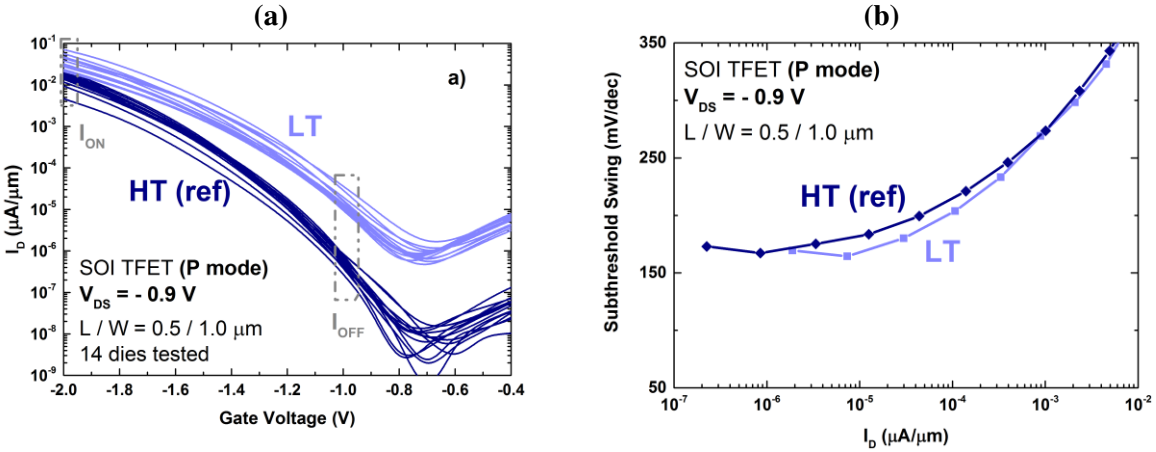

Figure 7. (a) Courbes $I_D(V_{GS})$ de SOI TFETs polarisés en mode P fabriqués par des processus HT et HT (14 mesures par plaque) à V_{DS} = - 0.9 V; (b) Pente sous le seuil en fonction du courant à V_{DS} = - 0.9 V.

L'étude de l'impact de la variation de la largeur du TFET sur les caractéristiques électriques révèle un phénomène intéressant: les dispositifs les plus étroits conduisent plus de courant que les dispositifs plus larges Figure 8a). Lorsque l'on trace le courant en fonction de la tension de grille pour des dispositifs de largeurs différentes, on s'aperçoit que l'effet tunnel se produit dans les coins du dispositif, et non à sa surface supérieure, sous la grille, vu que le courant est indépendant de la largeur. De surcroît, des simulations TCAD 3D montrent qu'il y a une plus grande surface de génération de courant par effet tunnel dans des dispositifs extrêmement étroits (W_{fin} = 5 nm). De cette étude il ressort que l'architecture TFET nanofil à grille triple et à faible épaisseur ou diamètre apparait comme solution possible pour la réalisation de circuits monolithiques 3D à très faible consommation d'énergie.

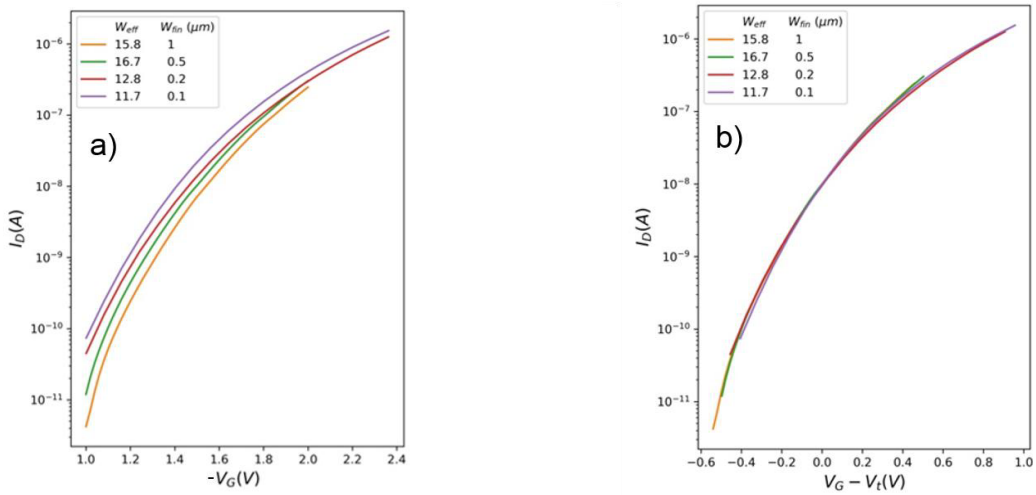

Figure 8. (a) Courbes moyennées $I_D(V_G)$ de p-TFETs avec L_G = 0.5 µm et différentes largeurs et différent nombre de dispositifs en parallèle: orange (15 canaux mesurés sur 50 puces), vert (30 canaux mesurés sur 74 puces), rouge (50 canaux mesurés sur 100 puces) et violet (75 canaux mesurés sur 100 puces); (b) Courant moyen en fonction de V_G-V_T. V_{DS} = - 0.9 V.

Chapitre 4. Etude des défauts dans les TFETs

Ce chapitre apporte de l'eau au moulin du chapitre 3, où l'on avait suggéré que l'accroissement de courant ON et la dégradation du courant OFF est dû à un effet tunnel assisté par défauts (TAT). L'hypothèse selon laquelle les transistors LT contiennent plus de défauts d'interface et de défauts à la jonction de source que les transistors HT est vérifiée expérimentalement.

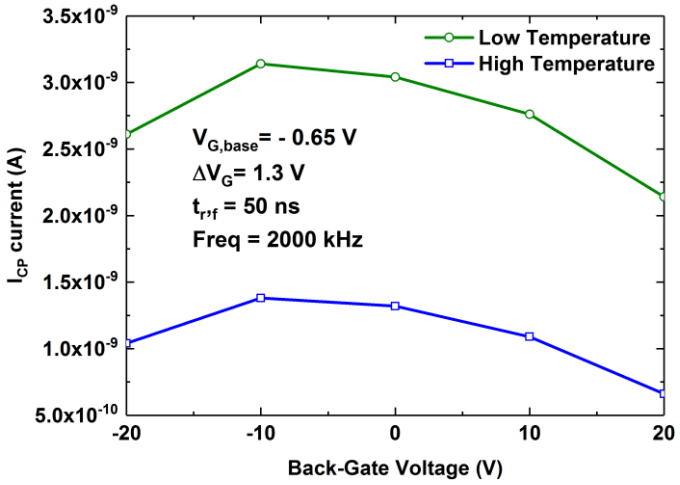

Figure 9. Courbes $I_{CP}(V_{BG})$ pour TFETs HT et LT pour une tension de base $V_{G,base}$ = - 0.65 V. Le courant I_{CP} dans les transistors LT est plus élevé que celui dans les dispositifs HT pour toutes les valeurs de la tension arrière V_{BG}, ce qui indique la présence d'une plus grande quantité de défauts dans es TFETs HT.

Nous avons mesuré la densité moyenne des états d'interface en utilisant la technique de pompage de charge (CP). Cette méthode permet de mesurer in courant CP qui est proportionnel au taux de recombinaison de porteurs piégés et ré-émis par les états d'interface. La Figure 9 montre que les TFETs LT produisent plus de courant CP que les transistors HT pour toutes les valeurs de tension de grille arrière (tension appliquée pour activer ou désactiver l'interface arrière). Il y a donc plus d'états d'interface dans les transistors LT que dans les dispositifs HT. On a vérifié par simulation TCAD qu'il y a bien une relation entre la concentration en porteurs dans le canal et le courant CP, pour différentes valeurs de tension de grille arrière.

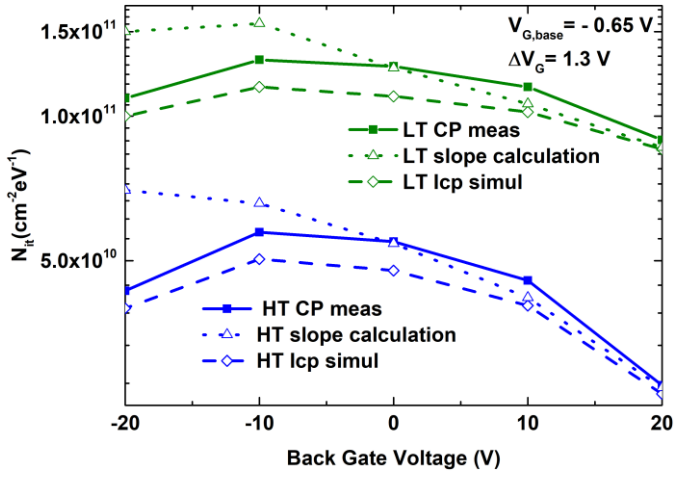

Figure 10. Densité d'états d'interface dans des TFETS HT/LT obtenue par 3 différentes techniques et pour une tension de base $V_{G,base}$ = - 0.65 V. Dans tous les cas la densité de pièges est plus grande dans les transistors LT que dans les dispositifs HT.

La mesure de la densité d'états d'interface par différentes méthodes de mesure CP confirme dans tous les cas que les TFETs LT ont une plus grande densité d'états d'interface que les TFETS HT (Figure 10).

Une analyse de bruit basse fréquence permet de mieux comprendre la nature des pièges dans les transistors HT et LT. Le bruit en tension reporté à la grille (S_{Vg}) est plus élevé dans les transistors LT que dans les TFETs LT, ce qui indique la présence de défauts à la jonction de source (Figure 11a). De surcroît, le comportement non *1/f* du spectre de bruit de courant de drain (Figure 11b) est caractéristique d'une distribution de pièges non uniforme à proximité des jonctions.

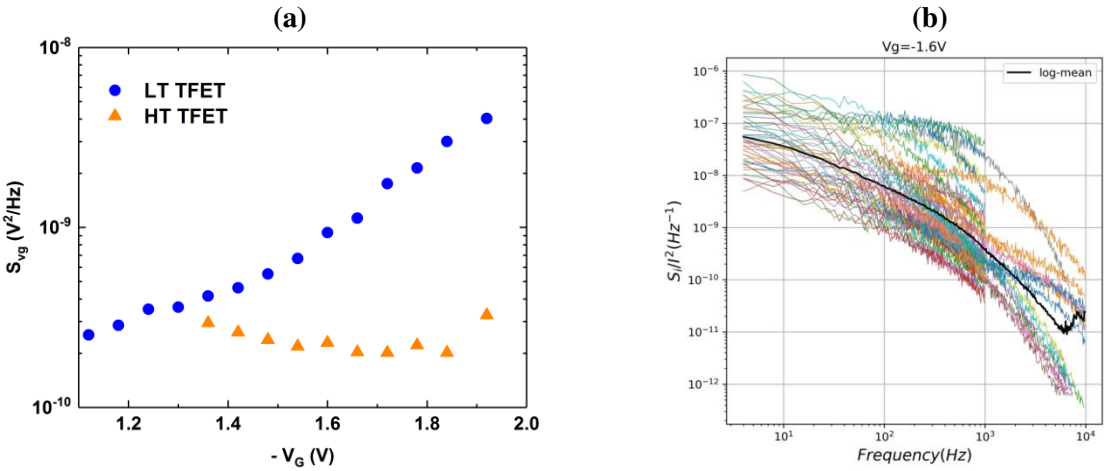

Figure 11. (a) Bruit en tension reporté à la grille (S_{Vg}) en fonction de la tension de grille à une fréquence de 10 Hz dans des TFETs LT et HT en mode canal P; (b) Bruit du courant de drain normalisé en fonction de la fréquence dans des P-TFETs LT (mesure effectuée sur 74 puces).

La Figure 12 illustre le mécanisme d'accroissement des courants ON et OFF en fonction du nombre de pièges dans les TFETs. Au plus il y a de défauts, au plus il y a de "canaux" possibles pour le passage de courant tunnel, ce qui augmente le courant et le bruit.

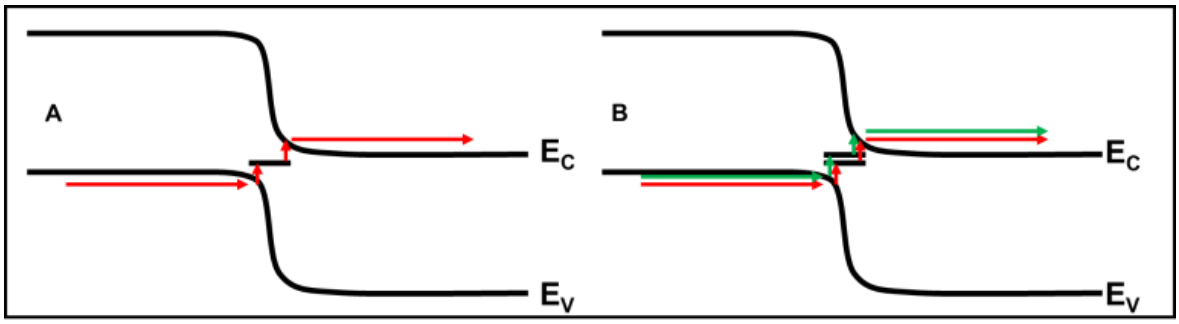

Figure 12. Schéma illustrant le tunneling assisté par pièges (TAT). Le courant augmente avec le nombre de pièges. A: un piège; B: deux pièges.

Chapitre 5. Architectures TFET Innovantes

Le dernier Chapitre de cette thèse est consacré à la simulation TCAD d'architectures innovatrices de transistors à effet tunnel. Le but est d'atteindre à la fois une pente sous le seuil faible et un fort courant ON.

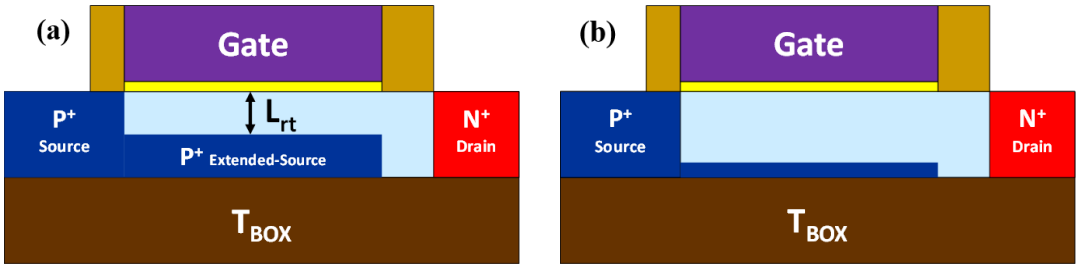

Figure 13. Architectures proposées: (a) N-TFET avec extension de source; (b): TFET avec une fine couche surdopée en bore.

Les architectures proposées sont basées sur l'extension de la jonction tunnel dans la région du canal pour augmenter la surface de la région qui engendre le courant BTBT. La Figure 13a montre le TFET à extension de source avec une épaisseur SOI T_{Si} = 11 nm, pour différente longueurs de l'extension (L_{rt}). Pour des dispositifs extrêmement fins, on propose un TFET avec une fine couche dopée avec une dose ultra-haute en bore (Figure 13b).

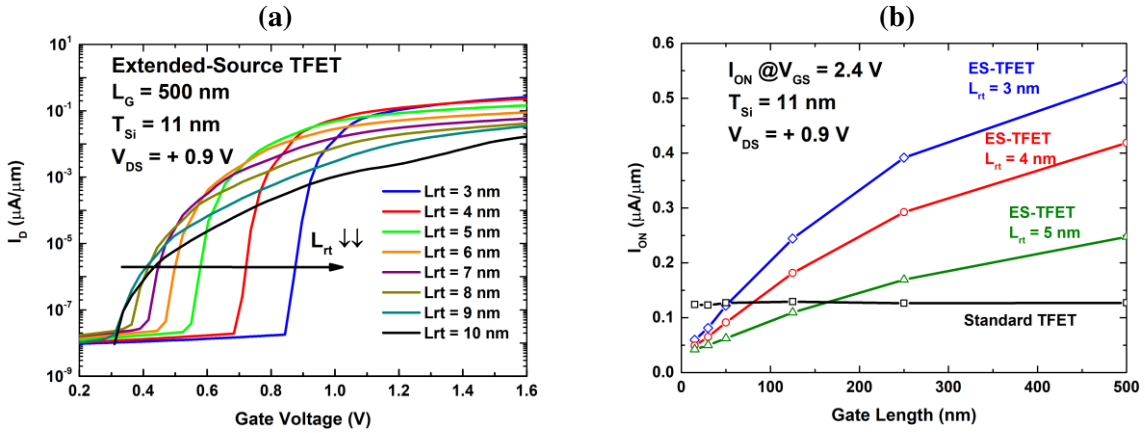

Figure 14. (a) Courbes $I_D(V_{GS})$ pour un long TFET à extension de source (L_G = 500 nm); (b) Courant $I_{ON}(L_G)$ dans des TFETs à extension de source en fonction de la longueur de grille. Si la grille est suffisamment longue (> 100 nm) on obtient un plus grand courant I_{ON} que dans un TFET standard.

La Figure 14a montre que les distances entre l'extension de source et la surface du SOI courtes (L_{rt} < 6 nm) permettent d'obtenir une pente sous le seuil raide et un courant de drain important parce que la grille a un très bon contrôle sur la région où se produit le BTBT. Ce contrôle diminue si la distance L_{rt} est augmentée. Malheureusement, un courant important n'est obtenu que pour des grilles longues (Figure 14b).

Pour remédier à ce problème, on propose un TFET avec une fine couche dopée avec une dose ultra-haute en bore (10^{21} cm^{-3}). On peut voir l'amélioration apportée par cette couche en comparant les courants obtenus ans les Figures 14 et 15.

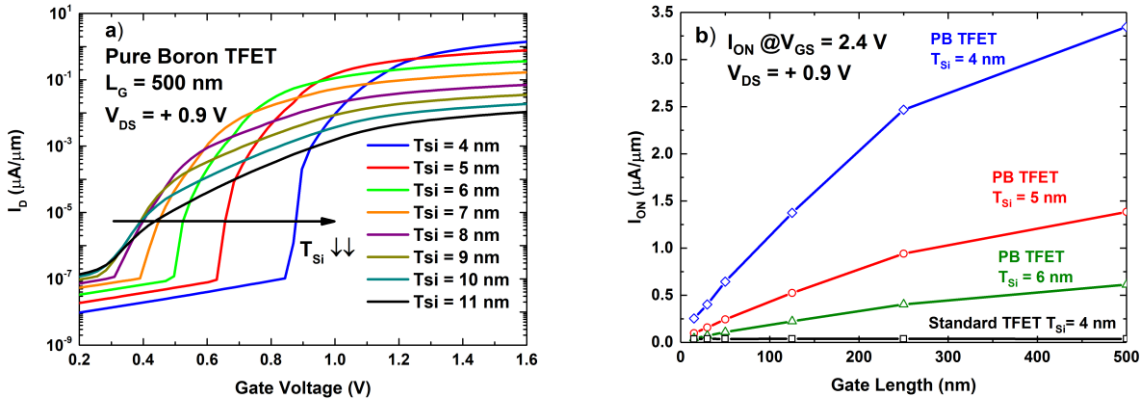

Figure 15. (a) Courbes $I_D(V_{GS})$ pour un long TFET avec une fine couche dopée avec une dose ultra-haute en bore (L_G = 500 nm); (b) Courant $I_{ON}(L_G)$ dans des TFETs avec une fine couche dopée avec une dose ultra-haute en bore en fonction de la longueur de grille. On obtient un plus grand courant I_{ON} que dans un TFET à extension de source.

Conclusions Générales

Nous avons étudié les raisons pour lesquelles les TFETs dont nous disposions ne présentent pas des caractéristiques dues uniquement à un effet tunnel intra-bandes. Ces effets ont été étudiés su des transistors produits à la fois par un processus de fabrication standard "haute température" et un processus basse température de type Coolcube™. Les performances des TFETs produits par ces deux techniques sont comparées par différentes techniques de mesure. Les principaux enseignements tirés de cette analyse sont:

1. **Les principales limitations à une bonne opération des TFETs sont liées au manque de maturité du processus de fabrication.**
    a. Les TFETs doivent être fabriqués dans une couche SOI mince (T_{Si} < 10 nm) pour déclencher un mécanisme BTBT efficace.
    b. L'inclusion de nouveaux matériaux tels que le SiGe ou Ge est nécessaire pour augmenter le taux de BTBT.
    c. Un bon recuit des défauts créés par l'implantation et une bonne qualité de l'interface de l'oxyde de grille sont nécessaires pour réduire le TAT sous le seuil.
    d. Un process CMOS standard ne remplit pas les conditions énumérées ci-dessus.
    e. Il faut développer de Nouvelles étapes de fabrication pour obtenir des jonctions plus abruptes.

2. **Les architectures triple grille et nanofils augmentent le BTBT**
    a. Dans les structures planaires, le BTBT est généré essentiellement dans les coins supérieurs et la contribution de la face supérieure du canal est négligeable.
    b. Dans des dispositifs très étroit, le BTBT est généré dans tout l'épaisseur du film SOI.
    c. Les structures multicanaux sont essentielles pour engendrer un courant ON satisfaisant.

3. Evaluation de TFETs en technologie 3D monolithique

a. Démonstration de TFETs fonctionnels.
b. 95% des MOSFETs LT de l'étage supérieur sont aussi performants que les dispositifs HT
c. De Nouvelles techniques de croissance épitaxiale (dont une croissance à basse température pour l'étage supérieur) doivent être développées pour réduire la densité de défauts aux jonctions, ces défauts étant responsables du TAT qui dégrade la pente sous le seuil.

4. Applications des TFETs

a. Les TFETs ne vont pas remplacer le CMOS classique en logique.
b. Par rapport au CMOS, les TFETs offrent un avantage en performance logique uniquement pour des tensions d'alimentation inférieures à 0.4V.
c. Pour être viable, une technologie TFET doit être co-intégrable avec du CMOS. Le chemin emprunté par le CEA est donc le bon.
d. Les microprocesseurs "multicore" et parallélisme massif peuvent tirer profit des TFETs pour certaines tâches spécifiques.
e. Toute la recherche et les solutions proposes dans cette thèse sont centrées sur les circuits logiques. Les TFETs peuvent également être utilisés pour des applications en mémoire en en protections électrostatiques (ESD), mais celles-ci sont en dehors du sujet de cette thèse.

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Appendix A.
Tunnel FET TCAD simulation

A.1. Band-To-Band Tunneling

The simulation of TFET architectures has comprised an important part of the present thesis study. One of the fundamental bases has been focused on increasing the band-to-band tunneling generation rate based on different geometries, film materials and dopants concentrations in FDSOI architecture. In order to accomplish this task it has been necessary to run a great number of simulation decks with a trade-off between the dedicated computational effort and the accuracy of the simulation. In particular, TCAD Sypnosys Sentaurus tool fits all the requirements related with the simulation time restraints.

In MOSFETs the thermal injection of the carriers is consequence of the drift-diffusion mechanisms. As TCAD is mainly an electrostatic study is possible to obtain well controlled simulations based on the energy bandgap, electron affinity and permittivity for different drain and gate polarizations. However, simulations on TFETs are more challenging because the tunneling mechanism is a transport contribution, which means that it is necessary to include the BTBT model to the electrostatic part. For this reason it is more complex to obtain accurate simulations. Sypnosys software provides different band-to-band tunneling models like Schenk, Hurkx and Kane [1], where the generation of carriers is proportional to the local electric field. Unfortunately, these models do not take into account the band bending of the energy bands at the source/channel junction, so the tunneling current is overestimate.

In order to obtain more accurate results, we have run all the simulations using the Nonlocal Path model based on the Landauer equation [2], which takes into account not only the tunneling probability but also the occupancy function [3]. This indicates that the model considers the band bending at the source/channel junction and the availability of empty states for the carriers to tunnel through the PN junction. This has allowed to the LSM laboratory at CEA to create a physics-based compact model for fully depleted TFETs [4]. The simulator solves the BTBT generation rate, given by [1]:

$$G = AF^{P}e^{\frac{-B}{F}} \qquad \textbf{(A.1)}$$

where F is the applied electric field and P is equal to 2.5 for a phonon-assisted tunneling process (indirect tunneling), because the channel material is silicon. In equation (A.1) the prefactor A and the exponential factor B for indirect tunneling are given by the equations [1]:

$$A = \frac{g(m_V m_C)^{3/2}\left(1 + 2N_{op}\right)D_{op}^{2}(qF_0)^{5/2}}{2^{21/4}h^{5/2}m_r^{5/4}\rho\varepsilon_{op}\left[E_g(300K) + \Delta c\right]^{7/4}} \qquad \textbf{(A.2)}$$

$$B = \frac{2^{7/2}\pi m_r^{1/2}\left[E_g(300K) + \Delta c\right]^{3/2}}{3qh} \qquad \textbf{(A.3)}$$

where m_C (m_V) is the conduction (valence) band density of states effective mass obtained through the calculation of the transversal and longitudinal electron effective masses; g is the electron spin degeneracy factor; N_{op} is the occupation number of the transverse acoustic phonon at temperature T; m_r is the reduced tunneling mass; D_{op} is the deformation potential of transverse acoustic phonons; ε_{op} is the phonon energy that indicates if the tunneling process is direct or phonon-assisted; E_g is the energy bandgap of the channel material and Δ_C is the conduction band offset with a non-zero value when the quantum confinement is taking into account for ultrathin films.

Symbol	Parameter name	Default value	Unit
A	Apath	4×10^{14}	$cm^{-3}s^{-1}$
B	Bpath	1.9×10^{7}	Vcm^{-1}
gD_{op}^2/ρ	Cpath	0	J^2cmkg^{-1}
g	degeneracy	0	1
Δ_C	Dpath	0	eV
m_C	m_c	0	m_0
m_V	m_v	0	m_0
ε_{op}	Ppath	0.037	eV
m_V/m_C	Rpath	0	1

Figure A.1. Table with default parameters for nonlocal path BTBT model [1].

For TFETs with silicon at the channel we have used the default values provided by Sentaurus as shown in Figure A.1. However, for simulations with SiGe it is necessary to recalculate the A and B parameters, because the electron effective masses (among others physical parameters) change with the germanium mole fraction. K-H. Kao et al [5], provide a thorough calibration of the A and B parameters for different germanium percentages and different tunneling directions (in our case [110]). For a 30% Ge the prefactor $A = 1.30x10^{15}cm^{-3}s^{-1}$ and $B = 1.81\ x10^{7}Vcm^{-1}$. Of course there is attached an uncertainty in the theoretical calculation of A and B, but the method is reliable. In addition the results obtained in these simulations are consistent with the performance of our experimental TFETs [6].

The domain to which we have limited the framework of the simulations lies entirely within a classical TFET simulation based on Drift-Diffusion and coupled with a constant mobility model. The use of BTBT model with the nonlocal option is enough to evaluate the relative performance of proof-of-concept TFET architectures and explore a first-order impact of the device structure on tunneling characteristics. For this reason, quantum effects such as subband formations and variation of bangap energy in thin-film devices have been neglected. In particular the quantum confinement in TCAD uses the Density Gradient (DG) model, which needs calibration. This has been already done by default for MOSFET transistors, however it is not verified with the doping dependence because it is time consuming and challenging in terms of parameter extraction in regards to Poisson-Schrödinger simulation. Moreover, as TFET analysis is performed usually at I_{ON} (high V_{DS} and V_{GS} polarizations), the quantum confinement has a second order impact for I_{ON} current because the channel is in full depletion.

With respect to the inclusion of highly doped regions inside the channel for Extended-Source TFET and Pure Boron TFET architectures [7] proposed in Chapter 5, this could lead to the appearance of band tails inside the bandgap, which could also degrade the subthreshold

swing. Nevertheles, for the sake of simplicity, in our simulations we have neglected the effects of high doping concentrations on the distribution of density of states in the semiconductor. Further studies should, however, include the effects of bangap narrowing and the formation of band tails inside the bandgap, which may affect the tunnel characteristics and degrade the subthreshold slope.

Another important consideration for future studies based on simulated TFETs, is the impact of the gate leakage in the performance of the proposed structures for relatively high voltages. We have tried to evaluate the impact of the leakage current versus the main tunneling current. However, we have not a sufficient background to fit the gate current with current TCAD simulation. The solution seems to use another nonlocal approach, which it is not full understood in terms of parameters extraction. Nevertheless, the possible tunneling through thin gate oxides has been neglected since the EOT of 1.18nm can in practice be achieved by using a high-k dielectric significantly thicker than the EOT. To conclude the lack of physical understanding of the gate current couple to a non-clear methodology on BTBT parameters lead us to continue the investigation in this issue.

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