New integrated architectures of sensors interfaces in SOI technology for very high temperature applications

Emna Chabchoub

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NOUVELLES ARCHITECTURES INTEGREES D'INTERFACES CAPTEURS EN TECHNOLOGIE SOI, POUR APPLICATIONS TRES HAUTES TEMPERATURES

Présentée par Emna CHABCHOUB
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Sous la direction de Pascal NOUET
et Mohamed MASMOUDI

Devant le jury composé de

Hélène TAP, Professeure, TOULOUSE INP-ENSEEIHT	Rapporteur
Kamel BESBES, Professeur, Université de Monastir	Rapporteur
Pascal NOUET, Professeur, Université de Montpellier	Co-directeur
Mohamed MASMOUDI, Professeur, ENI de Sfax	Co-directeur
Mounir SAMET, Professeur, Université de Sfax	Examinateur
Franck BADETS, Ingénieur-Chercheur, CEA-LETI	Examinateur
Frédérick MAILLY, Maître de Conférences, Université de Montpellier	Examinateur

UNIVERSITÉ DE MONTPELLIER

To my parents for believing in me and encouraging me continually …

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Abstract

This thesis is related to the field of harsh environment sensor interfaces, particularly high temperature environment. In this research, an integrated sensor interface for resistive sensors and which is able to operate over a wide operation temperature range is developed.

The main challenges of high temperature sensor interfaces are the exponential increase in the leakage current, and the decrease of both the threshold voltage and carrier mobility which degrade the performances of CMOS circuits over temperature variation.

The proposed sensor interface is a fully differential time-domain architecture. This offers the advantage of better thermal stability compared to analog based architectures. This is because time domain signals have higher thermal stability than analog signals. The sensor interface converts the differential sensor output voltage into a phase shift difference by means of a pair of Injection Locked Oscillators (ILOs). The so-obtained phase shift is digitized using a counter as a Time to Digital Converter. This approach has the advantage of circumventing the need of thermally stable time and voltage references. Indeed, the sensor interface is designed in a way that makes its digital output depend only on the ratio of the circuit parameters, leading thus to a high robustness against temperature variation.

The sensor interface has been fabricated using a 0.18µm Partially-Depleted Silicon on Insulator technology (PD-SOI) from XFAB which has been chosen for its robustness against temperature variations. The fabricated sensor interface achieves a low temperature dependence. Measurements show that a thermal variation of 178ppm/°C over ±60mV input full scale and a thermal variation of 65ppm/°C over ±40mV input full scale is obtained over a wide operation temperature range extended from -20°C to 220°C.

***Key words*— high temperature, injection locked oscillator, partially depleted silicon on insulator, differential, phase shifter, time domain**

Résumé étendu en Français

Dans le cadre de cette thèse, une interface de capteur haute température est développée et fabriquée en technologie silicium-sur-isolant (SOI) pour interfacer des capteurs résistifs fonctionnant à très haute température (allant jusqu'à 250°C). L'interface de capteur est située au plus proche du capteur. Par conséquent, elle doit être capable de fonctionner dans un tel environnement sévère sans dégradation de ses performances.

L'interface de capteur est développée pour une application de mesure du courant qui circule à l'intérieur des circuits de pilotage de puissance (« power drivers ») contrôlant les moteurs électriques. Elle convertit la tension de sortie du capteur de courant en une valeur numérique. Le cahier des charges exige un gain de 31LSB/mV sur une pleine échelle d'entrée de 66mV et une résolution de 11 bits.

L'étude de l'état d'art des interfaces de capteurs hautes températures résume les défis à relever pour que le circuit développé soit le plus stable thermiquement. Ces défis sont principalement les effets de la variation de la température sur les paramètres des technologies de fabrication des circuits intégrés. Ces effets sont essentiellement la décroissance de la mobilité des charges μ, la décroissance de la tension seuil V_{th} du transistor et l'augmentation exponentielle des courants de fuite I_{Leak} en fonction de la température. Signalons que ce dernier effet (l'augmentation exponentielle de I_{Leak}) détériore évidement les performances du circuit et peut conduite à sa destruction par latch-up.

Le choix d'une technologie plus robuste aux variations de la température que les technologies conventionnelles CMOS BULK est donc le majeur défi à relever. L'étude de l'état d'art a montré que la technologie SOI est plus adaptée aux environnements hautes températures. Ceci notamment grâce à ses moindres courants de fuite. En effet, grâce à la couche d'isolation dans les transistors en technologie SOI et étant donné que la profondeur des zones de diffusion drain-source est réduite, la surface des zones de jonction est fortement réduite. Cela conduit à une réduction des courants de fuite par rapport aux technologies conventionnelles. En outre, ces courants de fuite ont une plus faible sensibilité à la température. La tension de seuil V_{th} des transistors en technologie SOI est plus faible et plus stable thermiquement ce qui permet d'avoir des circuits plus rapides et offre la possibilité de baisser la tension d'alimentation sans aucune crainte d'augmentation des courants de fuite.

Ensuite, différentes techniques de conception sont utilisées pour mieux durcir les circuits contre les variations de la température. Ces techniques peuvent être divisées en quatre catégories:

- La première technique s'agit de durcir chaque bloc de l'interface de capteur séparément. Les exemples qui peut être cités sont la polarisation des transistors dans leurs zone ZTC (« Zero temperature coefficient ») et la technique de conception digitalement

assistée. Cette première technique conduit à des circuits avec un niveau de complexité élevée, une grande consommation et une faible fiabilité particulièrement aux hautes températures.

- La deuxième technique réside dans l'utilisation des architectures différentielles. Elle revient à utiliser, en parallèle avec la chaine de mesure principale, une chaine secondaire. Cette dernière est liée à une mesurande fixe et donc ne dépend que de la température de fonctionnement. L'utilisation de la même topologie pour la chaine principale et la chaine secondaire permet d'avoir la même dépendance thermique. Ainsi, la sortie différentielle du circuit, qui correspond aux rapports ou à la différence des sorties des deux chaines, sera insensible aux variations de la température.

- La troisième technique est l'utilisation des architectures bouclées. L'exemple le plus répandu est l'architecture delta-sigma (qui est utilisée surtout dans les convertisseurs analogiques numériques). La boucle assure la stabilité des performances du circuit. Toutefois, cette technique est limitée par la variation thermique de la fréquence d'échantillonnage et des composants mis à l'extérieur de la boucle et par les courants des fuites des « switches » qui peuvent devenir rédhibitoires aux hautes températures.

-La quatrième technique s'agit d'utiliser des architectures dans le domaine temporel. Son principe est de faire tout le conditionnement du signal dans le domaine temporel. Précisément, la sortie du capteur est convertie en un signal dans le domaine temporel : un signal modulé en fréquence, un signal modulé en largeur d'impulsion (Pulse Width Modulated signal: PWM) ou un signal modulé en position d'impulsion (Pulse Position Modulated signal PPM). Ce signal est ensuite numérisé grâce un convertisseur temporel-numérique.

Les signaux dans le domaine temporel, que l'on peut considérer comme des signaux numériques, sont plus stables en température que les signaux analogiques. Par conséquent, l'utilisation des interfaces de capteurs dans le domaine temporel aboutit à des circuits avec une faible dérive thermique par rapport aux interfaces de capteurs classiques qui ont une nature plutôt analogique.

Notamment, la technique de modulation de largeur d'impulsion (PWM) présente de meilleures performances que les autres techniques dans le domaine temporel. En effet, elle offre l'avantage d'un codage quasi-numérique de l'information. Par conséquent, les signaux PWM sont moins sensibles à la température et au bruit que les signaux modulés en fréquence, ce qui permet de maintenir l'intégrité du signal pendant sa transmission.

Afin de tirer profit de ces avantages, on propose une nouvelle technique PWM qui est au cœur de l'interface de capteur haute température. Cette technique est à base des oscillateurs verrouillés par injection utilisés comme déphaseurs.

Les oscillateurs verrouillés par injection sont des oscillateurs particuliers qui ont une entrée de synchronisation. Ils sont caractérisés par une plage de synchronisation et une fréquence d'oscillation libre f_0. Lorsque la fréquence d'entrée de synchronisation (i.e.,

fréquence de synchronisation f_{lock}) est dans la plage de synchronisation, les oscillateurs verrouillés par injection oscillent à f_{lock} ; tandis qu'hors de la plage de synchronisation, ils oscillent à leur fréquence libre f_0. La théorie Huntoon and Weiss montre que dans la plage de synchronisation, le déphasage de la sortie de l'oscillateur verrouillé par injection par rapport au signal de synchronisation Φ_{ILO} est fonction de la différence entre les deux fréquences f_{lock} et f_0.

Le principe de la nouvelle technique PWM repose sur cette propriété des ILOs. En effet, le déphasage généré Φ_{ILO} représente la largeur d'impulsion du signal PWM. Il est fonction de la différence entre deux fréquences dont l'une est fonction de la tension de sortie du capteur.

Précisément, la tension de sortie de l'interface de capteur est d'abord utilisée pour modifier la fréquence d'oscillation libre f_0 de l'oscillateur verrouillé par injection tandis que la fréquence de synchronisation est fixée à une valeur dans la plage de synchronisation. Ainsi, le déphasage de l'oscillateur verrouillé par injection Φ_{ILO} est fonction de f_0 uniquement et donc fonction de la tension de sortie du capteur. Ce déphasage correspond à la largeur d'impulsion d'un signal PWM qui oscille à f_{lock}.

Pour plus de robustesse, une architecture différentielle est adoptée. Grâce à une paire d'oscillateurs verrouillés par injection, la sortie différentielle du capteur commande simultanément les fréquences d'oscillation libre des deux oscillateurs. Cela fait varier leurs déphasages symétriquement en fonction de la tension de sortie différentielle du capteur. Cette dernière est ainsi convertie en une différence de déphasage qui représente la largeur d'impulsion du signal PWM. L'architecture différentielle permet de s'affranchir de la dépendance thermique des fréquences d'oscillations.

Des oscillateurs verrouillés par injection à relaxation (RILOs) sont choisies pour leur meilleure linéarité comparé aux oscillateurs harmoniques, et ceci afin que l'interface de capteur ait une grande plage de linéarité.

Vu que les oscillateurs verrouillés par injection à relaxation ont une entrée en courant, il est nécessaire de convertir la tension de sortie différentielle du capteur en une paire de courant afin de pouvoir contrôler les fréquences d'oscillation libre des deux oscillateurs. Un amplificateur à transconductance est donc utilisé pour réaliser cette conversion tension-courant. Vu que cet amplificateur est le premier block de l'interface de capteur, il est impératif que celui-ci ait une bonne linéarité: un amplificateur à transconductance dégénéré avec rétroaction a été sélectionné.

Le signal PWM obtenue est ensuite est converti en un signal digital en utilisant un convertisseur temporel-digital ; un compteur qui mesure la largeur d'impulsion du signal PWM. Le signal digital ainsi obtenu est fonction du signal de sortie du capteur.

L'horloge de compteur est générée à partir du signal de synchronisation par un multiplieur de fréquence: précisément une boucle à verrouillage de phase (PLL: Phase Locked

Loop). Ce choix a été fait afin de s'affranchir de la sensibilité thermique de la fréquence de synchronisation f_{lock} et de la fréquence de comptage $f_{counter}$. Néanmoins, un oscillateur de référence intermédiaire est utilisé pour réduire le facteur de multiplication de la PLL. Cette dernière génère l'horloge du compteur à partir de l'oscillateur de référence, et le signal de synchronisation est généré à partir de l'oscillateur de référence par un diviseur de fréquence purement digital.

Le développement théorique de l'interface de capteur montre que sa sortie digitale est fonction de la différence de déphasage des deux oscillateurs verrouillés par injection et du rapport entre les fréquences du compteur et de synchronisation $f_{counter}$ et f_{lock} respectivement. D'une part, vu que le signal de synchronisation et l'horloge du compteur sont générés à partir du même oscillateur de référence et étant donné que la PLL et le diviseur de fréquence sont stables thermiquement, les fréquences f_{lock} et $f_{counter}$ ont la même variation thermique. D'autre part, puisque les deux oscillateurs verrouillés par injection ont la même topologie, leurs déphasages ont la même dépendance thermique, ainsi leur différence de déphasage n'est pas influencée par la variation de la température. Par conséquent, cette architecture aboutit à une bonne stabilité thermique.

L'architecture de l'interface de capteur a été ensuite validée en utilisant un modèle comportemental développé en verilog AMS. Ce modèle a été aussi utilisé pour valider le choix des valeurs des paramètres de l'interface de capteur pour répondre au cahier des charges.

L'implémentation de l'interface de capteur a été réalisée en considérant l'environnement de fonctionnement hautes températures en utilisant la technologie silicium-sur-isolant partiellement-déplété (PD-SOI) 0,18µm de XFab. Un soin particulier est porté au choix de topologie de de l'oscillateur de référence parce elle conditionne la pleine échelle de l'interface de capteur. En effet, sa stabilité thermique affecte celle de la fréquence de synchronisation qui doit être toujours égale à la fréquence d'oscillation libre des deux oscillateurs verrouillés par injection à tension de sortie de capteur nulle quel que soit la température. Cette dernière affirmation est une condition nécessaire pour aboutir à la pleine échelle maximale de la largeur d'impulsion du signal PWM (i.e, $T_{lock}/2$).

Deux astuces de conception sont adoptées pour limiter ax maximum les effets de la variation de la température sur l'interface de capteur. Finalement, on obtient une sortie numérique de l'interface de capteur qui ne dépend que de la variation des rapports des différents paramètres du circuit ayant la même nature ou ayant la même variation thermique. Ainsi, une faible dépendance à la température doit être obtenue.

Cette faible dépendance thermique a été validée par simulation qui montre que, sur une plage de température étendue de -40°C à 250°C, la variation thermique de la sortie numérique de l'interface de capteur est inférieur à 34ppm/°C. En outre, les résultats de la simulation montrent que l'interface capteur satisfait le cahier des charges : un gain égal à 30LSB/mV et une résolution de 11 bits sont obtenus. Par ailleurs, une bonne linéarité est

obtenue par simulation ; un INL (Integral non-linearity) inférieur à ±2% de la pleine échelle de sortie, et ceci grâce à l'utilisation des oscillateurs verrouillés par injection à relaxation.

Un prototype de l'interface de capteur a été fabriqué en technologie PD-SOI 0,18µm comme preuve de concept. L'interface de capteur occupe une surface totale de 1860,1µm par 1885,9µm et une surface effective 0.21mm^2. Le prototype est mis dans un package céramique DIL 40.

Le prototype de l'interface de capteur est caractérisé en utilisant un environnement de test Labview pour une acquisition de donnés automatique. Le signal de sortie du capteur est généré avec des convertisseurs analogique-numérique. Un conditionneur thermique, Thermostream ATS, est utilisé afin de tester le prototype sur une plage de température étendue de -20°C to 220°C.

La caractérisation statique du prototype montre que le circuit a un gain égal à 30LSB/mV et une résolution de 11 bits sur toute la plage de température. En outre, cette caractérisation montre que l'interface de capteur est capable d'interfacer des capteurs avec une pleine échelle de ±60mV. Il consomme au maximum 1,53mW, mesurée à 220°C.

L'interface de capteur fabriquée présente un offset d'entrée maximal égal à -220µV et un offset de sortie maximal égal à 22LSB. L'offset de sortie est dû essentiellement à l'offset de l'amplificateur de transconductance et qui est la conséquence du mismatch entre les deux miroirs de courant qui génèrent les courants de polarisation de l'amplificateur. L'augmentation des dimensions des transistors de ces miroirs de courant a été considéré efficace pour diminuer l'offset de l'amplificateur à transconductance et ainsi l'offset de l'interface de capteur.

L'INL mesurée est plus importante que celle simulée. La valeur maximale de l'INL, égale à ±6% de la pleine échelle de sortie, est obtenue aux extrémités de la pleine échelle. L'étude de la non-linéarité a montré que les oscillateurs verrouillés par injection ont la plus grande contribution. Ainsi, l'utilisation des oscillateurs verrouillés par injection à relaxation avec une topologie dont la plage de linéarité est encore plus étendue peut résoudre ce problème. Toutefois, d'autres solutions sont envisageables sans changer la topologie de l'oscillateur telle que la réduction de la pleine échelle ou/et la réduction du gain de l'interface de capteur.

Les mesures de l'interface de capteur sur une plage de température étendue montrent que le circuit a une faible dépendance à la température. Toutefois, la variation thermique de l'interface de capteur est supérieure à celle obtenue en simulation. La valeur maximale de la variation thermique est égale à 178ppm/°C et elle est obtenue à l'extrémité de la pleine échelle de l'interface de capteur. Grâce aux simulations Monte Carlo, il a été montré que cela est dû aux effets des variations du processus de fabrication et aux mismatches qui sont plus prononcés aux extrémités de la pleine échelle d'entrée. En réduisant la pleine échelle d'entrée à ±40mV, une très faible dépendance thermique est obtenue: la variation thermique de l'interface de capteur fabriqué est toujours inférieur à 65ppm/°C. Cela est, selon notre

connaissance, est la plus faible variation thermique obtenue pour des interfaces de capteurs à 11 bits de résolution

L'étude dynamique du prototype montre que l'interface de capteur a une bande passante autour de 14kHz sur toute la page de température, qui est une bande passante suffisante pour des applications de mesure de courant. Le comportement dynamique de l'interface de capteur est dû à celui des oscillateurs verrouillés par injection puisque les autres blocks présentent des bandes passantes très élevées. Le comportement dynamique des oscillateurs verrouillés par injection est défini par leur temps d'acquisition qui est défini comme le temps nécessaire pour que l'oscillateur acquise le bon déphasage correspondant à son entrée.

La comparaison de l'interface de capteur proposée dans ce travail par rapport aux travaux répertoriés dans la littérature montre que des meilleures performances sont obtenues particulièrement en terme de stabilité thermique.

***Mots clés*— haute température, oscillateurs verrouillés par injection, domaine temporel, déphasage, architecture différentielle, silicium-sur-isolant partiellement déplété, signal modulé en largeur d'impulsion.**

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General introduction

Today, there is a high demand for sensor nodes operating in severe temperature environments. Application fields are in automotive, aeronautic and petroleum. High temperatures require sensing systems (sensor + sensor interface) that are able to work over a wide temperature range, typically from -40°C up to 250°C.

In most applications, sensor interface must be located close to the sensor for “noise considerations”. This offers the advantages of high signal to noise ratios which preserve the integrity of the signal delivered by the transducer (i.e., preserve the information given by the sensor) and of better system reliability.

Sensor interface electronics is then exposed to the same temperature constraints as the sensor. Cooling techniques may be used but these techniques are no longer adapted because they are bulky. Besides, cooling techniques require long wires and this degrades the signal integrity and reduces the system reliability.

Typical sensor interfaces, consisting of an amplifier stage and an Analog to Digital Converter (ADC), are limited by the high thermal sensitivity of its constitutive blocks. In fact, typical sensor interfaces are highly analog circuits. These latter are known for their high sensitivity to temperature variations due to the effect of temperature on MOS transistors. These effects are mainly an exponential increase of leakage currents, a reduction of threshold voltages and a decrease of carrier mobility.

The objective of this research work is to design a new architecture of sensor interface for resistive sensors suitable to work over a wide temperature range from -40°C up to 250°C. Silicon-on-insulator (SOI) technology has been chosen for its high robustness against temperature variations compared to bulk technology. More precisely, a Partially Depleted Silicon-On-Insulator (PD-SOI) technology, which operates over a wide temperature range, is chosen.

A Time-Domain differential sensor interface has been proposed, designed and fabricated. Time domain architecture leads to a quasi-digital sensor interface circuits that are less sensitive to temperature variations compared to analog based sensor interfaces. Indeed, digital signals have higher noise margins which make them more robust against temperature variations.

The sensor interface is based on a Voltage to Pulse-Width-Modulated signal (PWM) conversion using Injection Locked Oscillators (ILOs). The sensor interface is designed in such a way that makes its output depend only on the ratio of electrical parameters rather than their absolute values. Thus, the sensor interface is expected to achieve very low temperature dependence. The thesis is composed of four chapters and it is organized as follows.

Chapter 1 presents the design challenges of high temperature sensor interfaces. On the one hand, effects of temperature variation on CMOS technology, that limit performances of

CMOS integrated circuits in high temperature environment, are presented. A comparison between performances of SOI and bulk technologies over a wide temperature range is performed; it highlights major benefits of SOI technology in such a harsh environment. On the other hand, a review of existing high temperature sensor interfaces is performed. Existing design techniques used to mitigate temperature effects are listed and main limitations are highlighted.

Chapter 2 describes the proposed high temperature sensor interface which is based on ILOs. Background theory of ILOs is firstly introduced; Huntoon and Weiss theory is particularly presented. From this theory, main properties of ILOs are highlighted to illustrate their potentiality for the realization of high temperature sensor interfaces. Principle of a new high temperature sensor interface is then presented. A theoretical development is conducted to demonstrate thermal stability of the proposed architecture.

Chapter 3 details the context, the specifications and the implementation of the proposed sensor interface. The choice of the ILO is first justified. A Relaxation-ILO (RILO) has been chosen based on a theoretical analysis. A behavioural model has been built to validate circuit parameters satisfying system specifications. Implementation of the RILO-based sensor interface in a 180nm Partially-Depleted SOI (PD-SOI) technology is then presented. Physical implementation of each constitutive block and design constraints are detailed. Further high temperature design considerations are discussed in order to ensure thermal stability of the RILO-based sensor interface. Simulation results over a large temperature range are finally presented to demonstrate a low temperature dependence and a centred design with respect to specifications.

Chapter 4 is dedicated to the experimental characterisation of the fabricated sensor interface. A proof-of-concept has been fabricated in a 180nm PD-SOI technology with 1.8 V power supply voltage. Static and dynamic characterisations of the fabricated sensor interface have been performed over a wide temperature range extending from -20°C to 220°C. The silicon prototype allowed proving the expected low temperature dependence.

Finally, the conclusion sums up the presented work; it summarizes the major performances of the developed sensor interface. Suggestions for possible future prospects and areas of improvement of the sensor interface are also proposed.

CHAPTER1:
Design Challenges of High Temperature Sensor Interfaces

Introduction

The need for high temperature sensor interfaces for some applications with important potential for market and technological development has been clearly identified. The most well-known applications with added industrial value, where high temperature sensing systems are required, are automobile, oil and gas exploration and aeronautic applications. Engine industry is also interested in high temperature electronics for performance monitoring purpose.

In automotive applications, sensor nodes are used to collect information used to minimize fuel consumption as well as the emission of the exhaust.

In modern aircrafts, electrical actioners are used as alternatives to hydraulic actioners in order to lighten the aircraft weight and to reduce maintenance cost. In such applications, electrical and electronic circuits have to operate close to the engine. This offers the advantage of reducing the wiring complexity but it imposes stronger constraints on the electronics (i.e., a high temperature environment).

The purpose of sensing systems in oil and gas applications is to control the drilling process by delivering relevant information on the drilling environment. Moreover, they serve for geologic sites to investigate the presence of oil or gas by mounting them deeply in the wells.

The common barrier to these applications is the high temperature operation conditions which are summarized in table1.

Table 1. Operation temperature range of high temperature applications (Verbeck, Zimmermann, and Fiedler 1996).

Application		Operation temperature range(°C)
Automotive application	Compartment	-40 ; 85
	Engine	-40 ; 165
	Brakes	-40 ; 250
Aeronautic	Aircraft Surface	-40 ; 80
	Engine Intake	-40 ; 185
	Jet Engine	-40 ; 320
Satellites Space exploration		-150 ; 200 -150 ; 450
Oil Exploration Geothermal exploration		-40 ; 175 -40 ; 320

High temperature applications require high precision sensing systems. Each sensing system is composed of a transducer (sensor) that converts the physical parameter (temperature, pressure, electromagnetic field) into an electrical quantity (voltage, current,

electrical charges, resistance or capacitance variations) and a conditioner circuit (or readout circuit), also called sensor interface which converts the electrical quantity into a more exploitable information generally a digital information.

For the sake of signal integrity, the sensor interface has to be put as close as possible to the sensor. This necessitates reducing the sensor interface volume and thus, a greater integration of electronic functions is needed. Moreover, this leads to reduce wiring complexity, which improves the sensing system reliability and performances (Neudeck, Okojie, and Chen 2002) . However, this is challenging for circuits because they have to operate under a wide temperature range extended from -40°C to 250°C and even higher. Nowadays, there is not many commercial integrated circuits designed to operate in such temperature conditions and conventional CMOS technologies break down at such high temperatures.

Usually, these sensor interfaces are cooled passively or actively in order to be able to perform correctly. Cooling systems add more complexity to the sensing system because they use additional long wirings and connectors which results in elevated failure risk especially when exposed to temperature cycling (Kirschman 1999). Besides, there is a high concern regarding the reliability of cooling systems beyond 150°C. Furthermore, cooling systems are bulky and consume a lot of power (Neudeck, Okojie, and Chen 2002). That is why, even for applications whose operating temperature does not exceed 150°C; cooling systems are no longer used. Then, sensor interface electronics must be able to sustain these harsh conditions; they must be able to operate correctly over a large temperature range without any degradation of their performances and without breaking-down at extreme temperature.

Most of the integrated circuits (IC) are designed and fabricated using Complementary Metal-Oxide-Semiconductor (CMOS) technologies mostly because they enable the integration of analog and digital blocks on the same chip and because of their reduced fabrication cost. However, CMOS technologies suffer from various limitations when they operate in wide temperature range because of their sensitivity to temperature variations. Therefore, performances of electronic circuits fabricated using CMOS technologies are subject to major thermal variations.

Moreover, exponential increase in leakage currents with temperature causes malfunction of CMOS circuits at high temperatures. Indeed, leakage currents of CMOS technologies are important because of the small bandgap barrier of silicon. Therefore, wide bandgap technologies, such as SiC or GaN, have been recently considered in very high temperature applications; i.e., above 300°C (Neudeck, Okojie, and Chen 2002). These wide bandgap promising technologies are able to extend the operation temperature until 600°C.

Table 2 lists fabrication technologies according to their maximum operating temperature.

Table 2. Maximum operation temperature of fabrication technologies (Werner and Fahrner 2001).

Technology		Maximum operating temperature (°C)
CMOS	Bulk	150
	SOI	300
Wide Bandgap	3C-SiC	600
	6H-SiC	700
	4H-SiC	750
	GaN	>700
	Diamond	1100

Back to CMOS technology, proper design techniques must be adopted to mitigate the effect of temperature on IC parameters. The most pronounced effects causing the failure of CMOS high temperature electronics are the reduction of the carrier mobility, the degradation of the threshold voltage and the exponential rise of leakage currents (F.Patrick McCluskey 1996) (Majerus, Merrill, and Garverick 2013a). These effects are more pronounced in bulk CMOS technology than in Silicon-on-insulator (SOI). Indeed, the buried insulator layer in the SOI structure reduces the junction leakage current drastically which extends the operation range until 300°C (Pathrose et al. 2012).

1.1. Challenges for high and wide temperature range sensor interfaces

The semiconductor material is sensitive to temperature changes that affect several parameters of the circuits and increase the possibility of its failure especially when exposed to temperature cycling.

1.1.1. Carrier mobility

When a voltage is applied to the gate of the transistor, a channel is created between the drain and the source. If a voltage is applied between the source (S) and the drain (D), the carriers are subjected to an electrostatic force F expressed in the following equation:

$$F = q\,E \quad (1.1)$$

where q is the carrier charge, E is the electrical field applied across the semiconductor created by the V_{DS} voltage. Then, the electrons move in the opposite direction of the electric field, while the holes will move in the same direction of the electric field. A current flowing between the drain and the source is hence created.

The carrier mobility depends on its average velocity (v) during a certain amount of time called τ_C which is the average time between the scattering events (Simon M.Sze 2016) .

The average velocity is governed by the electrical field and the carrier mass m (law of momentum conservation):

$$qE\tau_C = mv \quad (1.2)$$

where m is the mass of the carrier,

The ratio between the average velocity and the electrical field defines the carrier mobility. It represents the relation between drift velocity of carriers and the vertical electrical field E:

$$\mu = \frac{q\tau_C}{m} \quad (1.3)$$

The temperature dependence of the mobility is defined by two scattering mechanisms: lattice scattering and impurity scattering. Lattice scattering is the carrier scattering by lattice vibrations. The probability of a carrier to be scattered by lattice vibration increases with temperature because this latter (i.e., lattice vibration) increases with temperature as well. This phenomenon (Lattice scattering) causes decrease of the mobility. Impurity scattering is the carrier scattering by impurity atoms which depends on the carrier velocity. The carrier velocity increases with temperature; leading to the increase in the mobility from the impurity scattering. However, the overall effect of the two scattering mechanisms makes the mobility decrease when temperature increases as expressed by the following equation (F.Patrick McCluskey 1996):

$$\mu(T) = \mu_0(\frac{T_0}{T})^{1.5} \quad (1.4)$$

where μ_0 is the carrier mobility at the reference temperature T_0. Figure 1.1 shows the electron and hole mobility of silicon semiconductor and for doping level equal to $10^{16}cm^{-1}$ (Simon M.Sze 2016) .

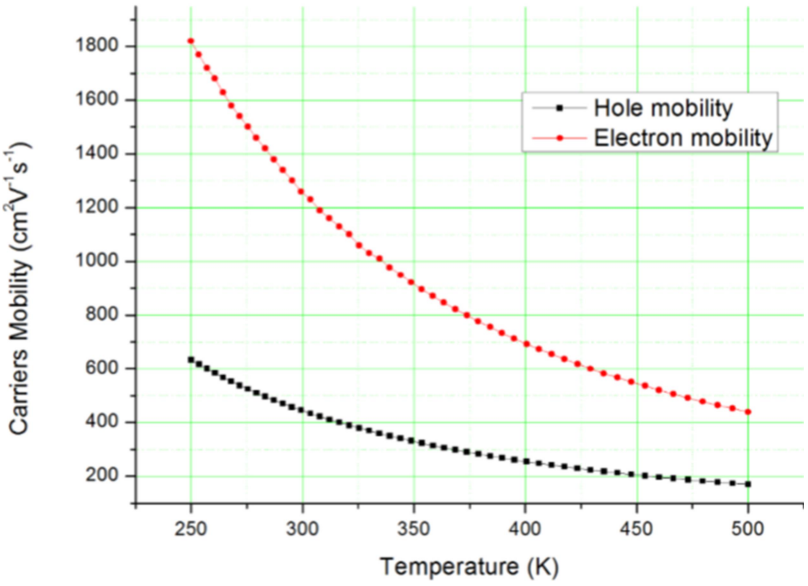

Figure 1. 1 : Variation of carrier mobility with temperature (Simon M.Sze 2016).

1.1.2. Threshold voltage

Threshold voltage is one of the most important factors resulting in the transistor temperature behaviour. The threshold voltage of MOSFET is given by (Simon M.Sze 2016):

$$V_{th} = V_{FB} + 2\emptyset_F + \gamma\sqrt{2\emptyset_F} \quad (1.5)$$

where γ is the body effect parameter given by equation (1.6), Φ_F is the fermi potential given by equation (1.7) and V_{FB} is the flat band voltage given by equation (1.8).

$$\gamma = C_{ox}\sqrt{2q\varepsilon_{Si}N_A} \quad (1.6)$$

where ε_{si} is the relative permittivity of the silicon.

$$\emptyset_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) \quad (1.7)$$

$$V_{FB} = \emptyset_{gs} - \left(\frac{Q_{ss}}{C_{ox}}\right) \quad (1.8)$$

where C_{ox} is the oxide capacitance, Q_{ss} is the surface charge density, $\emptyset_{gs}$ is the gate-substrate contact potential which is expressed as follows:

$$\emptyset_{gs} = -\frac{kT}{q}\ln\left(\frac{N_A N_G}{n_i{}^2}\right) \ (NMOS) \quad (1.9)$$

$$\emptyset_{gs} = -\frac{kT}{q}\ln\left(\frac{N_G}{N_A}\right) \ (PMOS) \quad (1.10)$$

where N_A and N_G are the substrate and gate doping concentrations, n_i is the intrinsic carrier concentration given by:

$$n_i = \sqrt{N_c\, N_v}\exp\left(\frac{-E_g}{2kT}\right) \quad (1.11)$$

where N_C is the effective density of states for electrons in the conduction band, N_V is the effective density of states for holes in the valence band, Eg is the energy bandgap of the semiconductor, T is the temperature in Kelvin, and k is the Boltzmann constant (8.62×10-5 eV/K).

The temperature dependence of the threshold voltage is thus given by (Filanovsky and Allam 2001) :

$$\frac{dV_{th}}{dT} = \frac{dV_{FB}}{dT} + 2\frac{d\emptyset_F}{dT} + \frac{\gamma}{\sqrt{2\emptyset_F}}\frac{d\emptyset_F}{dT} \quad (1.12)$$

where

$$\frac{dV_{FB}}{dT} = \frac{d\emptyset_{gs}}{dT} = \frac{1}{T}\left(\emptyset_{gs} + \frac{E_g}{q} + \frac{3KT}{q}\right) \quad (NMOS) \quad (1.13)$$

$$\frac{dV_{FB}}{dT} = \frac{d\emptyset_{gs}}{dT} = \frac{\emptyset_{gs}}{T} \quad (PMOS) \quad (1.14)$$

$$\frac{d\emptyset_F}{dT} = \frac{1}{T}\left(\emptyset_F - \frac{E_g}{q} - \frac{3KT}{q}\right) \quad (1.15)$$

Consequently, the temperature dependence of the threshold voltage V_{th} depends on that of $\emptyset_F$ and $\emptyset_{gs}$ resulting in a negative temperature coefficient; where the value of the temperature coefficient of V_{th} depends on the technology parameters. Besides, it has been proved that the threshold voltage of NMOS and PMOS go almost to the half when temperature goes from 25°C to 250°C for standard CMOS process (F.Patrick McCluskey 1996) .

1.1.3. Leakage currents

Leakage currents are composed of the subthreshold channel current, the junction leakage current, the gate leakage current and the channel punch through current. Leakage currents depend on the threshold voltage, the doping profile, the junction depth and the thickness of the oxide layer (K.Roy, Mahmoodi-Meimand, and Mukhopadhyay 2003). From the mentioned leakage currents, the subthreshold leakage current and the junction leakage current have the highest contribution to the overall leakage currents. In fact, the gate leakage current has very minor temperature dependence and the channel punch through current is very small compared to other leakage currents and it can be unconsidered.

When the gate-to-source voltage is below the subthreshold voltage, the transistor is in the off-state. However, an undesirable current flows between the drain and the source; this current represents the subthreshold leakage current.

The temperature dependence of the subthreshold leakage current I_{sub} arises from the temperature dependence of both the threshold voltage and the carrier mobility; I_{sub} rises exponentially with temperature.

At higher temperatures, the threshold voltage decreases sharply which has the effect of substantially increasing the leakage current.

At zero V_{gs} ; I_{sub} is represented by the Shockley diode model (E.S.Oxner 1988) :

$$I_{sub} = I_0 exp(\frac{V_{ds}}{kT/q} - 1) \quad (1.16)$$

where V_{ds} is the source to drain voltage, k is the Boltzmann constant and I_0 is the reverse saturation current which is also responsible for the exponential temperature dependence of I_{sub}.

$$I_0 = ATexp(-\frac{1{,}12}{2kT/q}) \quad (1.17)$$

where A is a constant.

Junction leakage current is caused by the reverse biased diodes (Jong, Meijer, and Roermund 1998) . In conventional CMOS technologies (bulk CMOS) reverse biased diodes exist between the source and the bulk and between the drain and the bulk. These diodes are not supposed to pass any current and they are used as an isolation to have only one main current flowing between the drain and the source. However, a leakage current from these diodes occurs. It represents the junction leakage current and it is one of the major limitations to the high temperature operation of transistors and CMOS circuits.

Junction leakage current has two components; the generation current and the diffusion current, which are responsible for the increase in the junction leakage current with temperature. The generation current is due to the generation of electron-hole pairs in the depletion region which pass through the junction with the help of the electrical field. The generation current is proportional to the intrinsic concentration and it usually dominates on the diffusion current until a temperature up to 100-150°C. Diffusion current is created by diffusion of thermally generated minor carriers. This phenomenon is proportional to the square of the intrinsic carrier concentration. This diffusion current dominates on the generation current at higher temperature (i.e., for temperature below 100°C-150°C).

The simplified expression of the total junction leakage current including the generation and the diffusion components is expressed as follows: (Simon M.Sze 2016) .

$$I_{J-L}(T) = I_{diffusion}(T) + I_{generation}(T) = \frac{q\,A}{\tau}\sqrt{\left(\frac{D_p}{\tau}\right)}\,{n_i}^2(T) + qA\frac{w}{2\tau}V_A\,n_i\,(T) \quad (1.18)$$

where, A is the area of the p-n junction, V_A is the voltage applied to the reverse biased diode, N_D is the n-type doping level, w is the width of the junction depletion region under voltage V_A, D_p is the minority carrier diffusion constant, and τ is the effective minority carrier lifetime. T is the temperature. n_i is the intrinsic carrier concentration given by:

$$n_i = \sqrt{N_c\,N_v}\exp(\frac{-E_g}{2kT}) \quad (1.19)$$

Equation (1.19) shows that the intrinsic carrier concentration is increasing with temperature. Therefore, according to equation (1.18), the junction leakage current increases with temperature. Figure 1.2 is an illustration of the temperature dependence of the junction leakage current.

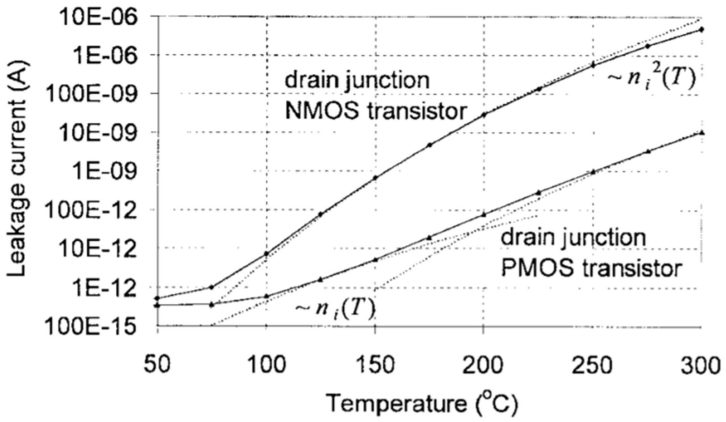

Figure 1.2: Temperature dependence of the junction leakage current (Verbeck, Zimmermann, and Fiedler 1996).

The increase in the leakage current with temperature has many drawbacks on CMOS integrated circuits; self-heating, the apparition of latch up phenomenon, modification of the operation points of analog circuits, charge losses at dynamic nodes, reduction of the output resistance of high impedance nodes and a more significant mismatching between devices (Yucai Wang 2015). Therefore, leakage current is considered as the main limitation to the circuit operation at high temperature.

1.1.4. Bulk versus Silicon on Insulator for CMOS technologies

Silicon-On-Insulator (SOI) technologies have been first proposed to minimize radiation and latch-up susceptibilities of integrated circuits. It has been first used for military and space applications (VANDANA.B and M.SIVA KUMAR 2013).

Transistors in SOI technology contain an isolation layer under the active area. Two types of SOI technology exist according to the thickness of the active layer; Fully Depleted SOI (FD-SOI) for thin active layer and Partially Depleted SOI (PD-SOI) for thick active layer. The isolation layer ensures isolation between the substrate and the active area. In the FD-SOI the active area is fully depleted and it forms the drain source channel, while in PD-SOI, the active area is depleted only until a certain depth and the rest remains neutral. Figure 1.3 shows the structure of bulk, PD-SOI and FD-SOI transistors.

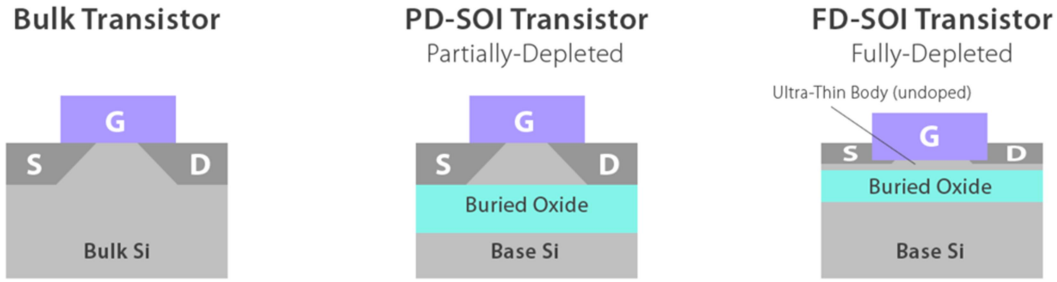

Figure 1.3: Structure of Bulk transistor, PD-SOI transistor and FD-SOI transistor (Olejarz et al. 2012) .

Over the last decade, interest in SOI technologies has increased due to their attractive advantages and their improved life time in harsh environments compared to classical bulk CMOS technologies (Udrea et al. 2012). Despite the additional cost of the substrate, SOI

technologies have been adopted to implement circuits for high-speed applications, low power applications as well as for several niche applications.

In high temperature applications, the circuit has to work over a wide temperature range going from -40°C to 250°C. Conventional bulk CMOS technologies are in fact unsuitable because of their leakage currents that increase exponentially with temperature and quickly become very important. SOI technologies, with lower leakage currents, can extend the temperature range of operation and the life-time of integrated circuits working under high temperature conditions.

In addition to the reduced leakage current, SOI technologies offer many other advantages that are presented hereafter.

1.1.4.1. Leakage currents

In SOI transistors, the depth of the drain and source diffusions is limited by the thickness of the thin silicon layer and thus, the junction area is strongly reduced (Shin et al. 1998). This leads to a reduction of the leakage current associated with the drain and source junction capacitances.

Moreover, in SOI transistor, the diffusion component of the overall junction leakage current is supressed. Only the contribution of the generation current remains. Then, the junction leakage current is a function of the intrinsic carrier concentration over the entire operation temperature range contrary to the junction leakage current in bulk transistors as illustrated in figure 1.4.

Consequently, the leakage current in SOI is smaller and it has smaller temperature dependence than that of bulk MOSFET, which makes them more suitable for high temperature applications.

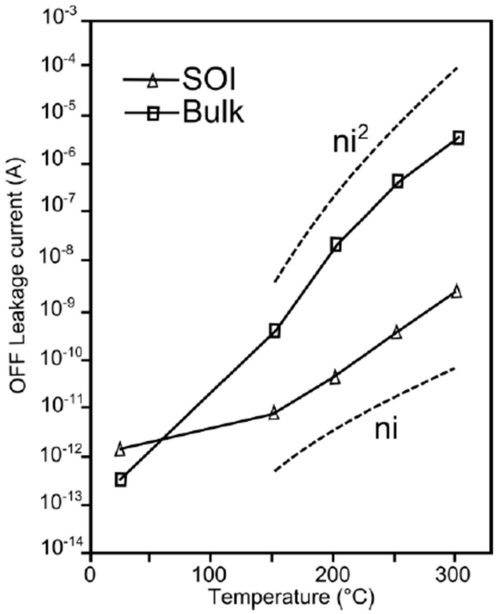

Figure 1. 4: Temperature dependence of leakage current: Bulk vs SOI (Arbess 2012) .

It is worth saying that, in SOI MOSFETS, the temperature dependence of the leakage current is also affected by the silicon film thickness. Thicker is the silicon film, higher is the temperature dependence of the leakage current and the thermal behaviour of SOI gets closer to that of bulk MOSFETS (Rudenko et al. 1999).

1.1.4.2. Integration density

In SOI MOSFETS, the isolation of the PMOS and the NMOS structures is smaller. In fact, the isolation layer in SOI technology ensures the complete isolation of the transistors instead of the isolation by junction as in bulk CMOS technology (Pavageau 2005). This leads to a decrease of about 30% in the silicon area occupied by a transistor compared to CMOS bulk technologies (Martineau 2008) (VANDANA.B and M.SIVA KUMAR 2013).

1.1.4.3. Mobility

According to equations (1.2) and (1.3), carrier mobility is inversely proportional to the vertical electrical field (Pavageau 2005) (Tsividis and McAndrew 2010) (Sturm, Tokunaga, and Colinge 1988). Higher is this electrical field, closer are the carrier to the gate, the more is the number of collision and hence lower is their average speed. It has been demonstrated in (Sturm, Tokunaga, and Colinge 1988) and (Yoshimi et al. 1988) that the vertical electric field is weaker for SOI transistors than for Bulk transistors. Therefore, SOI transistors have higher carrier mobility.

1.1.4.4. Threshold voltage

The thermal variation of the threshold voltage depends on the thermal variation of the depletion region depth (D.Flandre 1995).

In SOI transistors, the depletion region depth remains almost constant over the operation temperature range (Goel and Tan 2006). Therefore, the threshold voltage of SOI is less sensitive to temperature. This low sensitivity is more apparent in fully depleted SOI since the body film remains fully depleted compared to the partially depleted SOI.

However, above a critical temperature, evaluated around 250°C, the threshold voltage acquires the same thermal dependence as that of CMOS bulk technologies. In fact, when temperature reaches this critical value, intrinsic carrier concentration increases and the depletion region depth decreases. The variation of the threshold voltage as a function of the temperature in bulk and SOI transistors is presented in figure 1.5, where the thin film SOI transistor (i.e., FD SOI) is considered.

The figure shows that SOI transistors have a lower threshold voltage than bulk transistors whatever temperature is. This allows faster circuits and enables the use of low power supply voltage without any increase in the leakage current.

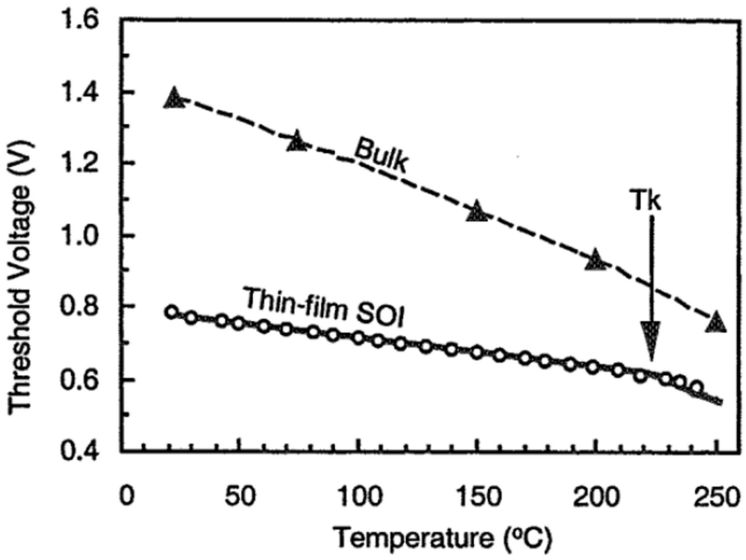

Figure 1. 5: Variation of the threshold voltage with temperature: Bulk vs SOI (Arbess 2012) .

1.1.4.5. Junction capacitance

Junction capacitances are the drain/bulk and the source/bulk capacitances, which also represent the transistor parasitic capacitances. In bulk technology, higher junction capacitances are due to the high doping level while, for SOI transistors, the junction capacitances are defined by the thickness of the isolation box. Besides, since the isolation layer in SOI has a lower permittivity than silicon; SOI transistors have smaller parasitic capacitances; they are 4 to 7 times smaller in SOI than in bulk (Marshall Andrew and Natarajan Sreedhar 2012). This offers the advantage of a reduced dynamic consumption for SOI transistors, (Le Coz 2012), as illustrated in figure 1.6.

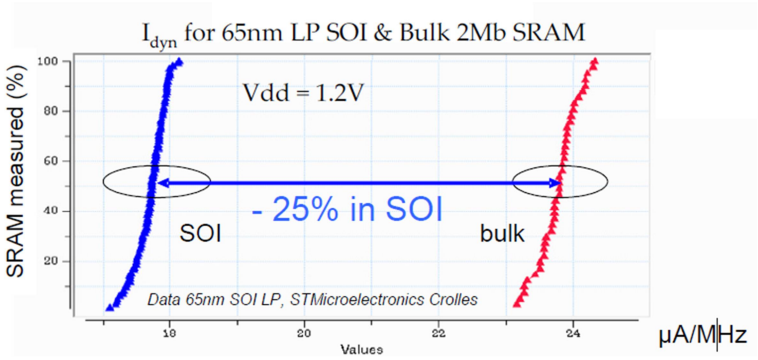

Figure 1. 6: Dynamic power reduction in SOI transistors (Martineau 2008).

What is more, the reduced junction capacitance leads to a lower propagation delay in SOI circuits (A.K.Goel 2006). Figure 1.7 shows the variation of the propagation delay with temperature of bulk and SOI transistors.

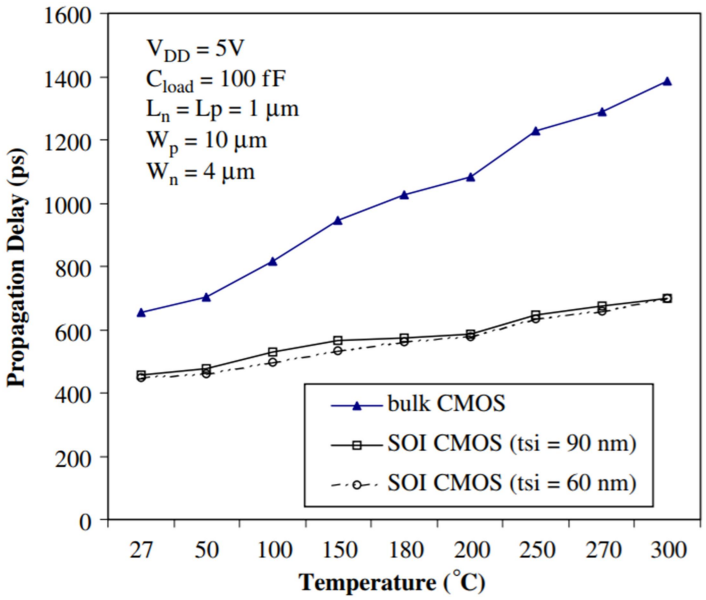

Figure 1. 7: Variation of the propagation delay with temperature: Bulk Vs SOI (Goel and Tan 2006).

The thermal variation of the propagation delay is caused by the increase in the junction capacitance due to the decrease of the depletion region depth with temperature. However, in SOI transistors, the depletion region depth has a very small temperature dependence compared to bulk transistors. Consequently, the thermal variation of propagation delay in SOI is lower than in bulk (A.K.Goel 2006).

1.1.4.6. Drain current and ZTC point

The temperature dependence of the drain current is affected by that of the threshold voltage and by that of the mobility.

$$I_{ds} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \qquad (1.20)$$

At low gate bias, in the weak inversion region, the temperature dependence of the drain current is dominated by the temperature dependence of the threshold voltage (A.K.Goel 2006). Therefore, the drain current increases with temperature.

At high gate bias, in the high inversion region, the temperature dependence of the drain current is dominated by the temperature dependence of the mobility (A.K.Goel 2006). Then, the reduction of the mobility causes the reduction of the drain current with temperature.

Consequently, the drain current has positive temperature dependence at low gate bias while it has negative temperature dependence at high gate bias. These two effects cancel each other at a certain gate bias voltage V_{gs} where the drain current has the minimum temperature dependence. This point is called Zero Temperature Coefficient (ZTC) and exists in both linear and saturation regions as the figure 1.8 outlines.

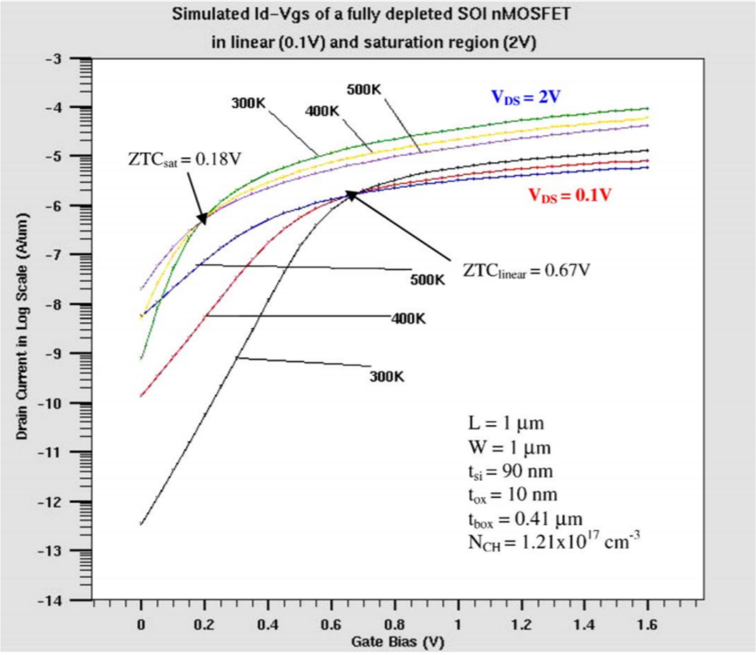

Figure 1. 8: ZTC illustration in FD-SOI (Goel and Tan 2006) .

SOI technology has the advantage of exhibiting ZTC point over a wider temperature range than bulk technology. ZTC point in SOI exists over a temperature range extended until 300°C while this point is identifiable only up to 200°C in bulk CMOS technologies (Eggermont et al. 1996). This is because, in bulk transistors, the leakage current at high temperature becomes comparable to the drain current at the ZTC point which leads to a big drift in the drain current. In SOI transistors, the reduced leakage current explains the reason behind the identification of the ZTC point until 300°C.

1.1.4.7. Output impedance

The output impedance, referred as r_{ds}, is the inverse of output conductance which is the derivate of the drain current with respect to the V_{ds} voltage.

$$r_{ds} = \frac{1}{g_{ds}} = \frac{1}{\partial I_{ds}/\partial V_{ds}} \quad (1.21)$$

The output conductance g_{ds} of bulk transistors has two components. The first component is related to the drain channel current component (channel component) which decreases with temperature because of the reduction of the drain current. The second component, the junction component, is related to the drain junction component (i.e., the leakage current) which increases with temperature.

In bulk transistors, the second component dominates the first component at higher temperature (around 150°C) because, above this temperature, the leakage current becomes very important (D.Flandre 1995). Therefore, for temperature lower than 150°C, the g_{ds} of bulk transistors decreases with temperature, while it increases with temperature above 150°C (Figure 1.9).

In SOI transistors, the output conductance is dominated by the channel component. This is because the junction component is drastically reduced due to reduced leakage current in SOI technology. Therefore, the temperature dependence of the g_{ds} of SOI transistors depends only on the drain current, hence, g_{ds} of SOI transistors is always a decreasing function of the temperature (Figure 1.9).

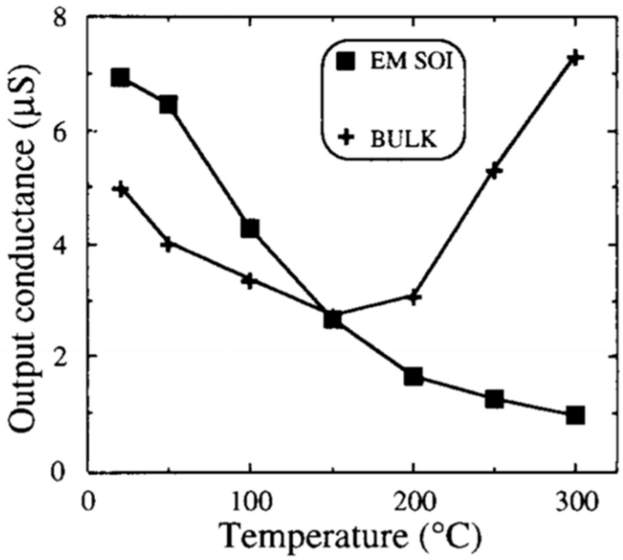

Figure 1. 9: Output conductance as a function of the temperature: Bulk vs SOI (Flandre 1995) .

The output impedance r_{ds} is inversely proportional to the output conductance g_{ds}, and it is always preferred for the output impedance to be as high as possible. Consequently, according to figure 1.9, the output impedance of SOI transistors is greater than that of bulk transistors for temperatures above 150 °C. This represents one of the advantages of SOI transistors at high temperature.

1.1.4.8. The g_m over I_d ratio for analog circuits

The g_m over I_d is the preferred figure of merit to evaluate performances of analog circuits. In strong inversion, it is expressed as:

$$\frac{g_m}{I_d} = \frac{2\,I_d}{V_{gs} - V_{th}} \frac{1}{I_d} = \frac{2}{V_{gs} - V_{th}} \qquad (1.22)$$

Hence, the temperature dependence of this ratio is due to that of the threshold voltage. Then the g_m / I_d ratio decreases as temperature increases.

As explained in section 1.1.4.4, V_{th} of SOI transistors has smaller sensitivity to temperature variation than V_{th} of bulk transistors. Therefore, g_m over I_d figure of merit has lower temperature dependence in SOI devices compared to bulk devices.

1.1.4.9. I_{on} over I_{off} ratio for digital circuits

Digital circuits are also affected by temperature variation. To evaluate the performance of digital circuits the I_{on} over I_{off} ratio is used as a figure of merit. Higher is this ratio; better are the performances of the digital circuit.

Figure 1.10 represents the drain current as a function of the gate voltage for different temperatures; a PMOS transistor is considered (i.e., for negative gate voltage the device is in the ON state and for a positive gate voltage the device is in the OFF state) (Arbess 2012) (Rudenko et al. 1999).

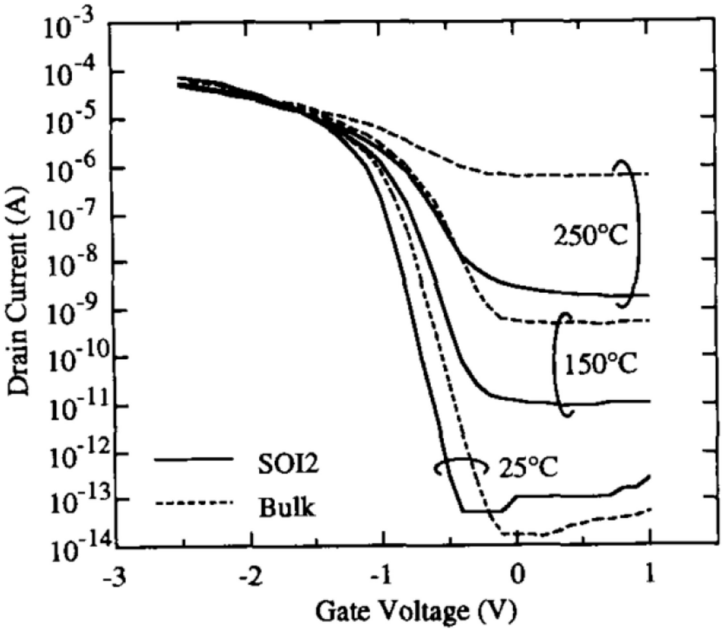

Figure 1. 10: Drain current as a function of V_{gs} of SOI and Bulk transistors (Arbess 2012) .

The figure shows that the OFF current of SOI transistor (I_{OFF_SOI}) is lower than that of the bulk transistor (for temperature higher than 25°C) and it has a lower thermal variation. In fact, the OFF current is related to the leakage current at off state of the logic gates. Knowing that SOI has less leakage current and that this latter has reduced temperature dependence; a higher and more thermally stable I_{on}/I_{off} ratio is observed for SOI MOSFETS. This characteristic offers the advantage of a reduced current consumption at off state for SOI circuits compared to bulk circuits.

1.1.4.10. Short channel effects

The short channel effects (SCE) are due to the loss of the electrostatic control of the gate; the depletion charge in the conduction channel (i.e., the space charge region in the conduction channel) is no longer fully controlled by the gate. This phenomenon appears when the channel length is shortened to the same order as the source and drain layer width. It affects the performances and the reliability of the transistors.

Short channel effects cause the lowering of the potential barrier; this effect makes the carriers able to travel between drain and source when V_{gs}=0 (carriers should not travel between drain and sources when V_{gs}=0).

Under normal conditions, when V_{gs} is no longer zero, the barrier is reduced by the gate effect in order to enable the carriers to flow between the drain and the source. Only V_{gs} has this effect on the potential barrier. In fact, for a long transistor, the space charge of drain/bulk and source/bulk junctions are extended mainly in the substrate (because it has a low doping level) and the depletion charge in the conduction channel (i.e., the space charge region in the conduction channel) is controlled only by the gate.

By reducing the transistor length, space charge of drain/bulk and source/bulk junctions (drain and source depletion regions) get closer. This leads to the apparition of charges sharing regions (Figure 1.11). Then, the depletion charge in the conduction channel becomes mostly controlled by the junctions and not only by the gate (i.e., the lowering of the gate control on the channel.). This leads to the lowering of the potential barrier (Daniel Chanemougame 2005).

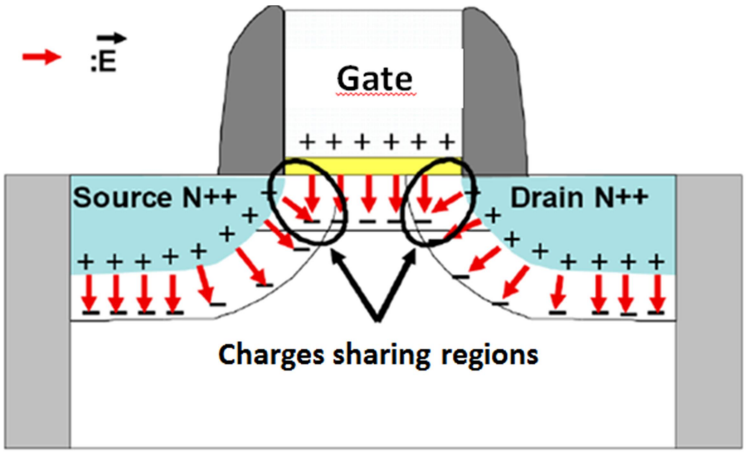

Figure 1. 11: Short channel effect phenomenon (Aime 2007).

Besides, in short transistors, when the drain voltage V_d increases, the drain depletion region becomes larger and it causes an additional lowering of the potential barrier. This phenomenon is called Drain-Induced Barrier Lowering (DIBL).

Short channel effects cause the decrease of the threshold voltage V_{th} which increases drastically the transistor leakage current and limits the performances of the transistor at high temperature. In fact, this phenomenon makes the threshold voltage depend on the transistor length in both linear and saturated regimes. Hence, any change in the channel length makes the threshold voltage vary as well as the transistor performances. Therefore, SCE deteriorate the circuit efficiency and they are responsible for the I_{off} current increase in short channel transistors.

In SOI MOSFETS, the effect of the drain and source depletion regions and the effect of the drain voltage on the barrier lowering in short transistors are reduced compared to bulk (Pavageau 2005). In fact, SOI technology does not favour the electrostatic coupling between

the drain and the source; the depletion charge in the conduction channel (i.e., the space charge region in the conduction channel) is well controlled by the gate. Hence, short channel effects are reduced (Arbess 2012). This ensures better control on V_{th} and then better control on the leakage current, which favours the electronic high temperature operation.

1.1.4.11. Latch-up

Latch-up is extremely dangerous for integrated circuits as it creates a low impedance path between the power supply and the ground that can lead to the destruction of CMOS integrated circuits. The latch-up phenomenon appears due to the existence of NPN and PNP parasitic transistors in bulk technologies, which activates a parasitic thyristor formed by these bipolar transistors. The presence of substrate/well is at the origin of these parasitic bipolar transistors by providing the low-doped base of both bipolar transistors while emitters are implemented by N+ and P+ source diffusions. Efficient design rules for latch-up immunity exist but they lead to large surface overheads to isolate both P and N well and/or substrate in order to suppress the collector-base junctions.

In SOI technologies, there is a complete isolation between N and P transistors and thus there is neither parasitic bipolar transistors, nor thyristor structures (VANDANA.B and M.SIVA KUMAR 2013b). Figure 1.12 illustrates the latch-up phenomenon in bulk versus the nonexistence of this phenomenon in SOI.

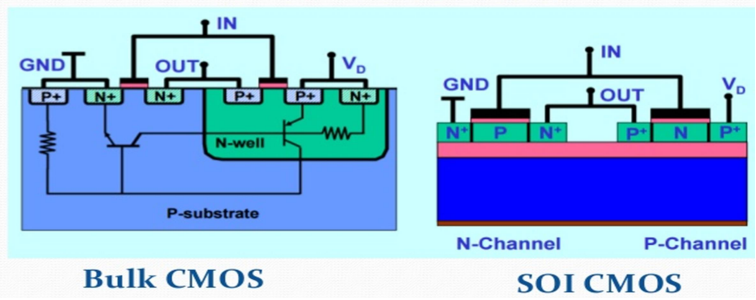

Figure 1. 12: Latch-up in bulk vs no latch-up in SOI (KASHISH GROVER 2016).

1.1.4.12. Self-heating in FD-SOI

Self-heating appears because the thermal conductivity of the isolation layer is smaller than that of silicon, making difficult the heat evacuation inside a SOI device. This phenomenon is more pronounced in FD-SOI due to the thinner silicon layer.

Figure 1.13 reports $I_{ds}(V_{ds})$ characteristic with and without self-heating. It shows that self-heating affects the slope of the curve; it leads to a negative slope compared to the case where there is no self-heating. This is due to drain current and mobility reduction due to intensive internal heating. This effect is more pronounced at high gate voltage and thinner silicon film.

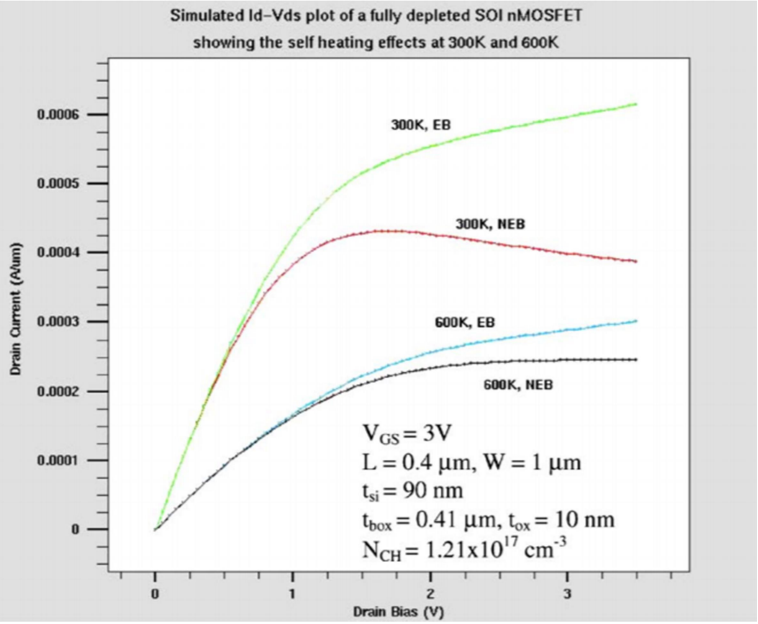

Figure 1. 13: Self-heating effect is FD-SOI (EB without self-heating and NEB with self-heating) (Goel and Tan 2006).

1.1.4.13. Kink effect in PD-SOI

The silicon film in PD-SOI is partially depleted leaving a neutral zone inside the silicon film. Inside this neutral zone, impact by ionization effect occurs. To explain this phenomenon, we take for example a NMOS transistor (Figure 1.14). Negative carriers are flowing in the channel from source to drain. Hence positive carriers (holes) will move to source as well as to the body. In bulk, these holes are evacuated and they will be recombined inside the substrate. However in SOI and due to the isolation layer, they are accumulated inside the non-depleted zone. Therefore, Body voltage V_b increases which lowers the threshold voltage, this phenomenon is called floating body or kink effect. More holes are accumulated with the increase in the drain current, and V_b continues to increase. When the body to source diode becomes on, accumulation stops and the holes are evacuated in the source. Figure 1.14 illustrates this phenomenon.

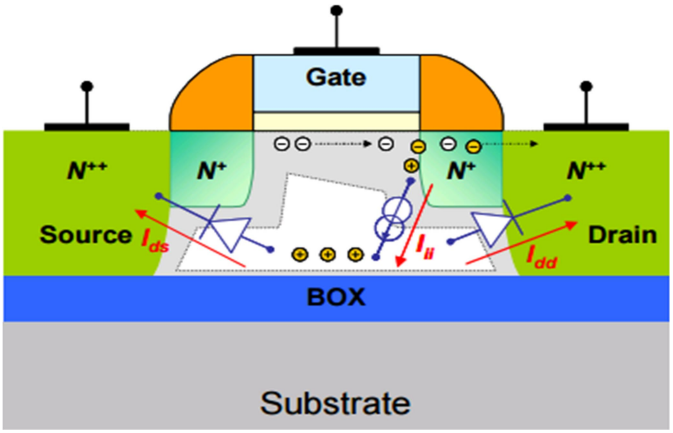

Figure 1. 14: Impact by ionization effect in PD-SOI (Martineau 2008) .

The increase in the body voltage leads to high current and higher conductance and this is expressed by a kink in the transistor characteristic $I_{ds}(V_{ds})$ as shown in figure 1.15. Kink effect can be avoided by limiting the V_{ds} voltage.

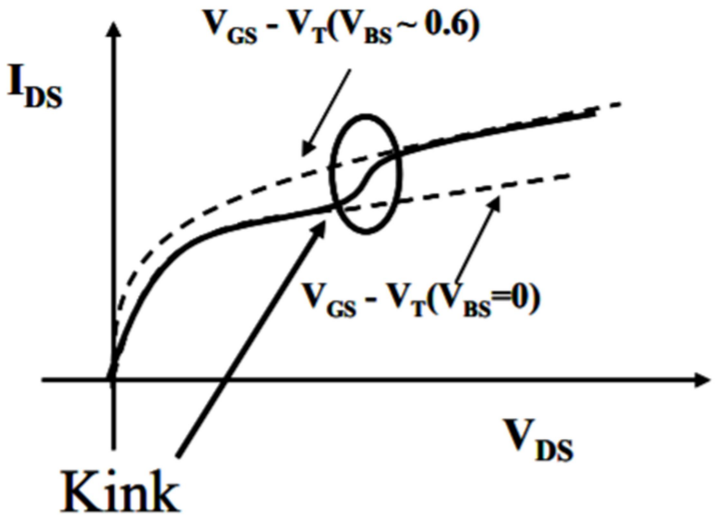

Figure 1. 15: Kink effect in PD-SOI (Martineau 2008) .

1.1.4.14. Reliability

The increase in the complexity level of integrated circuits makes the reliability requirements of devices and systems at severe conditions very challenging. Specific attention has to be paid not only to thermally activated degradation mechanisms, but also to the metallization, bonding, die attach and packaging.

Several physical phenomena are involved in the circuit reliability. These physical phenomena are affected by temperature, thus, affecting the life-time of circuits working at high temperature conditions (Arbess 2012) .

1.1.4.14.1. Electro-migration

Electro-migration is caused by the gradual movement of ions in a conductor. This leads to the transport of material due to the momentum transfer between the diffusion metal atoms and the conducting electrons. In an integrated circuit, the momentum transfer between electrons and metal creates a hole in the conductor that is why this phenomenon is also called dish effect. Electro-migration is dangerous for integrated circuits and it is more dangerous at high temperature since the electron concentration is higher. Connections fabricated using aluminium are more resistant to electro-migration than their copper counterparts.

A common technique to address electro-migration uses conductors with large sections since the mean time to failure (MTF) is proportional to the connector section as shown in the so-called Black Equation (Chain et al. 1997):

$$MTF = \frac{A}{j^2} \exp(\frac{E_a}{KT}) \quad (1.23)$$

where j is the current density, A is the section of the conductor and E_a is the activation energy.

Electro-migration is a major challenge in high temperature circuits. Yet, in recent high temperature technologies, founders have hardened metallization by adding tungsten because this latter is known for its high reliability with respect to electro-migration.

1.1.4.14.2. Reliability of the gate oxide

The gate oxide is subject to an electrical stress during the operation of the transistor. The time to breakdown t_{BD} of gate oxide (i.e., the time for the oxide to breakdown in the presence of a constant gate voltage) decreases with the decrease of the thickness of gate oxide.

The increase in temperature reduces t_{BD} and makes gate oxide more susceptible to break down. Figure 1.16 shows the variation of t_{BD} with temperature for different thicknesses of gate oxide (Kaczer et al. 2000). It shows that it is advantageous to choose technologies with thick gate oxide if the circuit is exposed to high temperature.

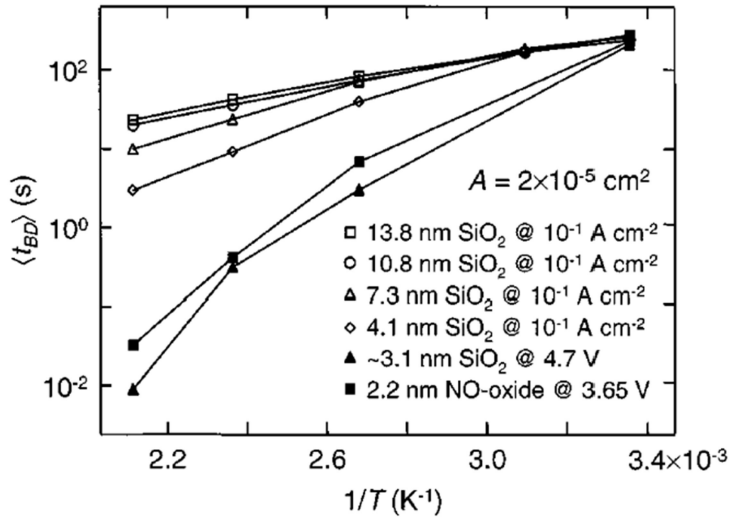

Figure 1. 16: Temperature effect on t_{BD} for different oxide thickness (Kaczer et al. 2000).

1.1.4.14.3. Contact metal barrier

High temperature degrades metallic contacts, thus inducing metallic ion atoms to diffuse in the silicon substrate. Chemical techniques are used to prevent the apparition of this phenomenon.

1.1.4.15. SOI technology process maturity

Nowadays, SOI process is sufficiently mature to ensure good performances with high yields. Among available SOI technologies from different foundries, one may note:

- ATMEL, which developed a 0.18µm SOI technology called SMARTIS able to work until 200°C,
- XFab, which proposes a SOI technology that contains high voltage options which enlargers the panel of high temperature applications,

- Honeywell, the high temperature world leader, who developed a technology called HTMOS tested and guaranteed until 250°C but it is able to work at 300°C. Reliability has been proven up to 5 years at 225°C.
- ST microelectronics, which proposes the leading-edge 28nm FD-SOI technology. This technology is guaranteed until 125°C with a very high reliability.

Other SOI foundries exist but, to our knowledge, the previously listed are representative of existing SOI technologies. Some academic initiative could be also listed such as Fraunhofer institute (IMS) that developed a high temperature SOI technology guaranteed until 250°C. This technology uses Tungsten connections for high immunity to electro-migration; hence longer life-time can be ensured.

1.1.4.16. Conclusion: SOI vs Bulk

SOI technology includes an isolation layer that reduces the PN junction areas. Therefore, the junction leakage current of a SOI MOS transistor is decreased by a factor of 3 or 4 compared to its bulk counterpart. Threshold voltage is 2 or 3 times smaller and the output trans-conductance is improved at high temperature. This enables the design of sensing systems able to work over a wider temperature range with a lower thermal drift. These are in summary the reasons why we choose to work with a SOI technology.

1.2. Design techniques for high temperature sensor interfaces

A typical sensor interface is composed of a low-noise amplifier (LNA), a low-pass filter and an Analog to Digital Converter (ADC). The amplifier is required to meet the ADC input dynamic range requirements and to have more accurate voltage measurements since low voltages are highly affected by noise and external perturbations. The filter, also called anti-aliasing filter, is used to ensure Shannon condition; i.e., to cut frequencies higher than the sampling frequency and to avoid folding of high-frequency noise. Then, the filter output is digitized by means of an ADC in order to get a digital output for easier interfacing with the digital world.

Technology developments are conducted for the purpose of obtaining smaller chip area, higher circuit speed and lower power consumption. Downscaling the device dimensions fulfils these objectives with a continuous reduction of transistor lengths that imposes a reduction of the supply voltage. However, downscaling has some negative effects; it leads to a reduction of threshold voltages, which increases the leakage current, limiting the performances of integrated circuits at high temperature (Lewyn et al. 2009). Besides, it affects immunity to noise and degrades SNR. For conventional sensor interfaces, downscaling can reduce performances because it limits the input dynamic range and the ADC resolution and most important for us, it limits the operation temperature range.

Indeed, conventional sensor interfaces are highly analog circuits. Then, operating points of their constitutive blocks are subject to major variations with temperature (due to

thermal variation of transistor parameters). This leads to drastic degradation of circuit performances.

Although SOI transistors parameters have less thermal variation making them more adapted to harsh conditions, special design techniques should be also adopted in order to mitigate the effects of temperature variation. Various techniques have been reported in the literature. They are reported next in four main sections: separate block hardening, closed loop architecture, differential topology and time domain architecture.

1.2.1. Separate block Hardening

Separate block hardening consists in the hardening of each block of the circuit separately against temperature variations. Some basic principles are reported below.

1.2.1.1. Zero Temperature Coefficient point

Zero Temperature Coefficient (ZTC) point corresponds to a bias gate voltage where the drain current and/or the transistor trans-conductance have the lowest temperature variation. This point exists in both linear and saturated regions for the drain current while it exists only in the saturation region for the trans-conductance. This technique ensures constant current and/ or trans-conductance which leads to stable performances over temperature (Jiang, Shu, and Chang 2017) .

The main limitation of this technique is that once biased at the ZTC point, performances are still affected by the increase in junction leakage currents with temperature. Besides, taking into account process variations, any drift of the gate bias will make the transistor shift from the ZTC point.

1.2.1.2. Leakage current matching technique

Since leakage current is the most important limitation to high temperature operation, some hardening techniques are based on leakage current minimization and are called “leakage current matching”. They are based on the fact that a transistor has two reversely biased diodes; the first one between drain and bulk and the second one between source and bulk. These diodes are the major contributors to the leakage current.

The technique consists in adding a dummy PMOS in series with the NMOS and a dummy NMOS in series with the PMOS so that their leakage currents would cancel each other (the leakage current of the PN junction of the PMOS drain and the leakage current of the NP junction of the NMOS source have opposite current flow direction). An illustration of this technique is presented in figure 1.17 where the reverse biased diodes and the leakage current flow directions are presented.

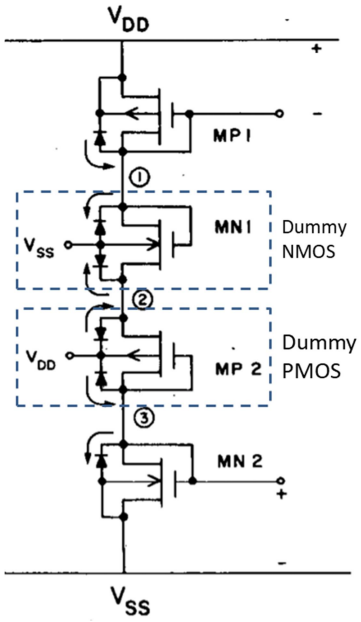

Figure 1. 17: Leakage current matching technique (Shoucair 1986) .

However, this technique has a practical limitation. In fact, the PMOS and the NMOS must have exactly the same leakage current and the same sensitivity of this leakage current to temperature, a condition difficult to guarantee. Then, this technique remains conceptual and difficult to implement. However, it can be used as an optimization method rather than a high temperature hardening technique (Shoucair 1986).

1.2.1.3. Constant g_m bias circuit

The use of constant g_m bias technique is very common in high temperature circuits to mitigate the effect of the mobility reduction due to temperature increase. This technique is well suited when a circuit requires a thermally stable trans-conductance g_m. This is particularly true in amplifiers because g_m affects stability, gain and bandwidth (Yucai Wang and Chodavarapu 2015a). A schematic of constant g_m bias circuit is represented in figure 1.18. The temperature dependence of the resulted trans-conductance is limited to the temperature dependence of the bias resistance as expressed in equation (1.24). Therefore, a thermally stable bias resistance is required to ensure the trans-conductance thermal stability.

$$g_m = \frac{2}{R_b}\sqrt{\frac{W}{L}}\left(\sqrt{\frac{L_1}{W_2}} - \sqrt{\frac{L_2}{W_2}}\right) \quad (1.24)$$

In some technologies, resistances with low temperature coefficients are not available. When available, the resistance R_b can be designed using two resistances with opposite temperature coefficients.

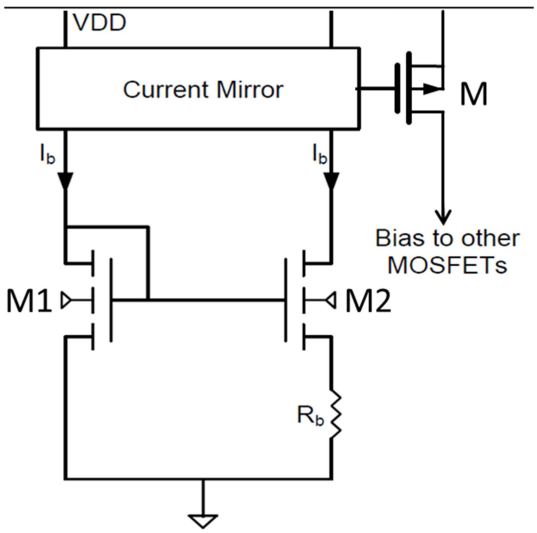

Figure 1. 18: Constant bias g_m circuit (Yucai Wang 2015) (Majerus, Merrill, and Garverick 2013).

1.2.1.4. Reverse Body Biasing (RBB)

Reverse Body Biasing is used for PD-SOI MOSFETS to make the depletion region depth always constant with temperature (Ba and Kim 2017). Since the depletion region depth influences temperature dependence of both threshold voltage and leakage current, thermal stability is improved by RBB and thus, this enlarges the maximum operation temperature of PD-SOI MOSFETS (Alexander Schmidt, Kappert, and Kokozinski 2013). Figure 1.19 shows the observed reduction of off-sate currents when using RBB in analog switches.

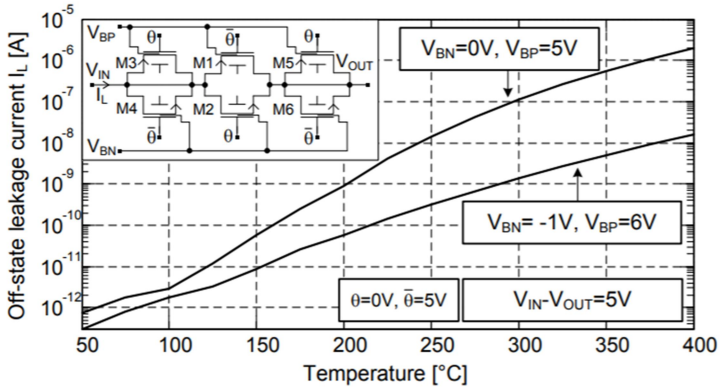

Figure 1. 19: OFF_state leakage current reduction using RBB in an analog switch (V_{BN} and V_{BP} are respectively the reverse bias voltage of the NMOS and PMOS transistors) (A. Schmidt, Kappert, and Kokozinski 2013).

However, RBB is possible only in some technologies. Besides, it is difficult to control independently the body bias of a circuit with many transistors; it requires more silicon area, additional biasing voltages and monitoring circuits. This leads to complex systems and performance is limited by the accuracy of the reverse biasing voltages.

1.2.1.5. Adaptive biasing

If the temperature behaviour of a parameter is known, it can be compensated using a voltage or current bias having the opposite temperature behaviour (Chen et al. 2017). This

technique is commonly used bandgap voltage references (BGVR) where a proportional to absolute temperature (PTAT) voltage is used in order to compensate the complementary to absolute temperature (CTAT) behaviour of the base emitter voltage of a bipolar transistor. Then, these two voltages are added to provide thermally stable voltage reference.

This technique is limited by the non-linearity of the parameter to be compensated. For example, the base emitter voltage has harsh non-linearity over a wide temperature range. Thus, it is required for the PTAT voltage to have the same harsh non-linearity; which is very difficult to guarantee. That is why most BGVRs have a curvature shape as a function of temperature.

1.2.1.6. Digitally assisted design

In order to address power challenges and thermal performances, digitally assisted analog circuits are a promising trend to meet today high temperature requirements. It gets benefit from the fast advance in digital circuits. Some digital blocks are used to improve thermal stability of analog circuits over temperature. They monitor analog performances of elementary stages of the circuit and they adjust their parameters (resistance, capacitance, bias current, bias voltage) according to the operation temperature.

Since analog parameters are controlled by a digital input word, a Digital to Analog Converter (DAC) is required. For example, in bandgap voltage references (He, Zhao, and Cheng 2014), a digital calibration is used to compensate the non-linear CTAT thermal variation of the base-emitter voltage by means of a trimmable resistance (Luong et al. 2014). Digitally Assisted Design (DAD) is also used to design oscillators having low temperature drift (Tran et al. 2017), (Roy et al. 2016).

Figure 1.20 shows an example of a relaxation oscillator with a digital calibration. The digital feedback controls the loop delay to compensate the thermal drift of the oscillation frequency; the delay tuning blocks is consisted of different delays lines that are controlled by feedback bits. A pulse is generated, using a reference voltage (V_{ref2}) and a replica comparator ($COMP_2$), which is used as a reference in the calibration process.

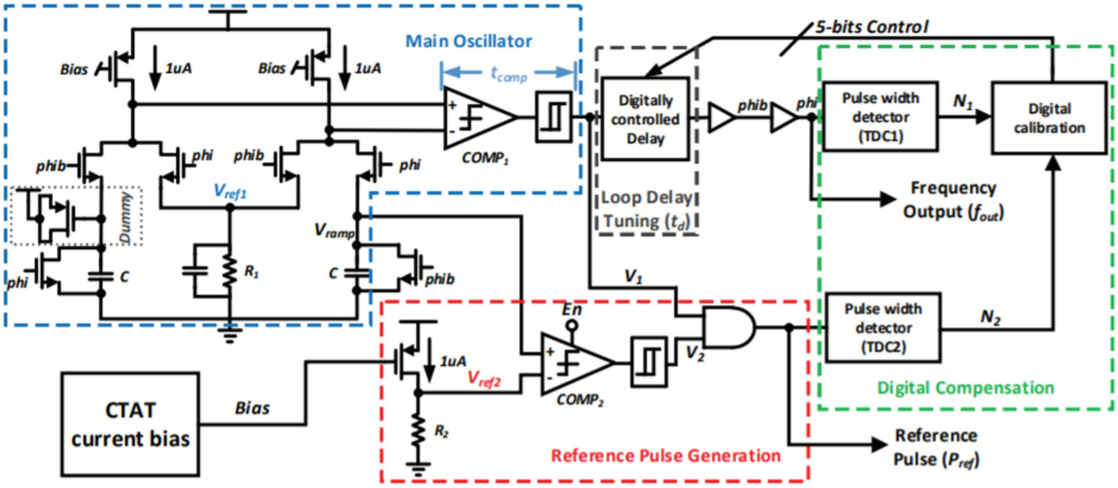

Figure 1. 20: An example of a relaxation oscillator designed using digitally assisted design technique (J. Wang et al. 2015).

The digital control signal required to compensate the thermal drift of analog parameters depends on the operation temperature. Then, the full range of operating temperature should be divided into a maximum number of temperature sub-ranges. Higher is the number of the sub-ranges, higher is the precision and better is the overall thermal stability of the circuit. This is very challenging because this technique requires accurate temperature measurement in order to detect different temperature sub-ranges. Besides, this technique is limited by the accuracy of the different temperature sub-ranges threshold. Moreover, the thermal stability of the overall circuit is limited by the resolution and the temperature sensitivity of the ADC.

1.2.1.7. Limitations of the separate block hardening design technique

Separate block hardening design technique may be a good choice for medium operation temperature range but not the best choice for high temperatures above 150°C because of the leakage currents which are difficult to supress even with leakage matching techniques. Besides, it leads to very complex circuits, and this affects their reliability and may reduce their life-time. Moreover, the so-obtained temperature hardened circuits will exhibit larger power consumption and large silicon area.

1.2.2. Differential architecture

Differential topology is used in order to compensate the effect of temperature on the sensing channel by means of a reference channel.

The main channel is connected to the sensor and it delivers an output Out_{Sensor} that is function of the measured physical parameter. The reference channel is commonly connected to a reference sensor that is affected by temperature in the same manner but not by the physical quantity to be measured. Hence, its output Out_{Ref} does not depend on the measured parameter. The output of the sensor interface is then defined by a differential measure between both outputs (i.e., the ratio or the difference between Out_{Ref} and Out_{Sensor}). Using the same topology for sensing and reference channels, the same temperature dependence is

obtained and thermal sensitivity of the sensing channel may be compensated. Hence, the output of the differential architecture achieves a low thermal sensitivity (Y. Wang and Chodavarapu 2014) (Geeter, Nys, and Bardyn 1997) (Bianchi, Karam, and Courtois 1999).

An example of differential sensor interface is presented in figure 1.21. The sensing channel generates a frequency f_{meas} proportional to the parameter to be measured. This frequency is mixed with another frequency f_{ref} generated from the reference sensor. The output of the overall sensor interface is then the difference between the two frequencies (i.e., $f_{meas} - f_{ref}$).

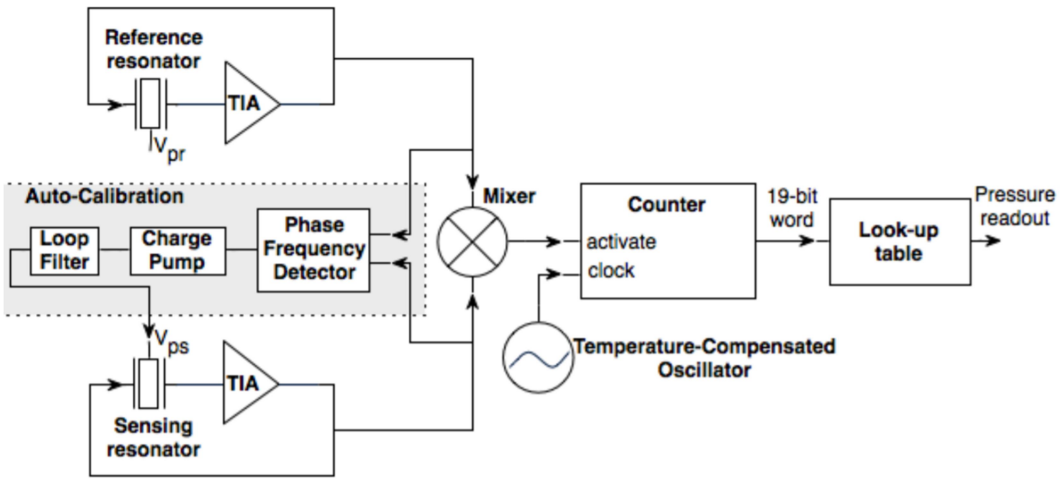

Figure 1. 21: Differential sensor readout circuit (Taghvaei et al. 2010) .

Performances of differential topologies are limited by process variability that affects the matching between both reference and sensing channels; temperature dependence of the sensing channel may then be different from that of the reference channel. Hence, the thermal stability of the differential output is degraded (George et al. 2016). To address this limitation, calibration is thus required.Yet, calibration over a wide range of temperature leads to expensive test time, especially for large volume production (K.Bowman, 2015). Sometimes, researchers prefer to implement calibration circuits inside the chip. However, this technique has also some limitations related to extra circuitry to perform the in situ calibration, which is complex and may lead to an increase in the overall chip area and power consumption (B.Wang 1998).

1.2.3. Closed loop architecture

Closed loop architecture has been widely used in the design of high performance modulators and Analog to Digital Converters (ADC). The most famous example of closed loop architecture is the Δ-Σ architecture which has the advantage of good noise immunity due to its high signal to noise ratio (SNR).

Closed loop architectures have been also used in high temperature circuits (Liu 2006). The loop ensures constant operating points of the different constitutive blocks over a large temperature range. So-obtained systems then exhibits a low temperature sensitivity and overall performances are not affected by temperature variations (Davis and Finvers 2003) even if elementary blocks have not been optimized for a wide temperature range. Hardening the global measurement chain using a closed-loop is a good alternative to hardening

individual blocks as it reduces the complexity of the circuit, which in turns ameliorates reliability and thermal stability. Besides, it leads to reduced power consumption and area. An example of closed loop architecture is presented in figure 1.22, a first order modulator used for sensing systems.

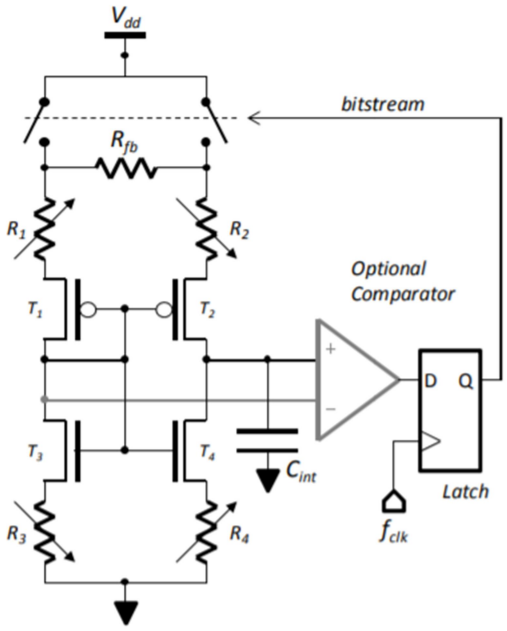

Figure 1. 22: Schematic of the sensor architecture based on the Active Bridge cell placed into a 1st order ΣΔ modulator (Hacine et al. 2011).

The efficiency of a closed loop architecture over a large temperature range is limited by the thermal drift of the reference sampling frequency and the outside loop components (Demeus, Viviani, and Flandre 1998). On the one hand, it is a challenge to ensure the stability of the sampling frequency over a wide temperature range (Kularatna 2008). On the other hand, the thermal drift of the outside loop components are not compensated by the loop. As an example, switches are highly affected by the increase in temperature and they may be responsible for thermal drift of overall circuit performances (e.g., signal to noise ratio, SNR). Indeed, when temperature increases, leakage current increases exponentially; this leads to a thermally activated loss of charges inside the switches that lowers their efficiency. To address this issue designers tend to increase the sampling frequency (Demeus, Viviani, and Flandre 1998). Moreover, switches are affected by technology downscaling; the leakage current then increases, which lowers the SNR of closed loop architectures (Alvarado, Bistué, and Adín 2011).

1.2.4. Time Domain Architecture

Time domain architecture is a new trend that addresses limitations of the previously mentioned techniques. The information delivered by the sensor is encoded in the time domain; i.e., a frequency, a Pulse Width Modulated (PWM) signal, a Pulse Position Modulated (PPM) signal, a delay or a phase shift. Signal conditioning is firstly performed in the time domain and a Time to Digital Converter (TDC) is then used to obtain a digital output word representing the sensor measure. This approach leads to quasi-digital-like sensor

interfaces. The use of quasi-digital signals is very promising because of the simplicity of their interface circuits. They offer the advantage of direct transmission without degradation of signal integrity and they can be easily converted into digital signals using simple counters.

Moreover, digital signals are less sensitive to temperature variations compared to analog ones because of their higher noise margin that ensures a reduced sensibility to noise and other interfering signals. Time domain architectures, which have a digital nature, benefit from this advantage, and consequently, this may lead to low temperature dependence of integrated sensing systems.

In addition to that, time domain architectures take advantage of technology downscaling. Thanks to a simplified analog front-end and thanks to the quasi-digital approach, architecture is easily portable to lower technology nodes. Therefore, lower supply voltage can be used without SNR degradation. It is worth saying that portability may be impossible for conventional sensor interface architectures because they have an intensive analog nature. In fact, the reduction of power supply voltage lowers the threshold voltage, which in turn causes an increase in the leakage current especially at high temperatures. Hence, since analog parts are very sensitive to leakage currents compared to digital circuits, their performances are highly affected by temperature variations and this may lead to their dysfunction at extreme temperature conditions. Consequently, time domain architecture is more convenient for modern technology nodes especially when high temperature applications are targeted.

Furthermore, using time domain architecture, reduced power consumption and reduced silicon area are achieved. In addition to that, the accuracy and the reliability are improved.

Practically, analog to time domain conversion is performed by means of two basic techniques. The first technique, voltage to frequency conversion, converts the analog information into a frequency using a Voltage Controlled Oscillator (VCO). The second technique covers both pulse width modulation (PWM) and pulse position modulation (PPM). As PPM is not often used in the literature, this technique is not presented below.

1.2.4.1. Voltage to frequency conversion

Voltage to frequency conversion is performed using a voltage controlled oscillator; typically a ring oscillator (Valero et al. 2011) (Fick et al. 2014). The analog input controls the delay of inverters constituting the ring oscillator and they define the oscillation frequency. Figure 1.23 shows a starved ring oscillator used in wireless transmission. The inverter delay is fixed by its bias current. This latter is the drain current of a transistor whose gate to source voltage is controlled by the sensor output voltage.

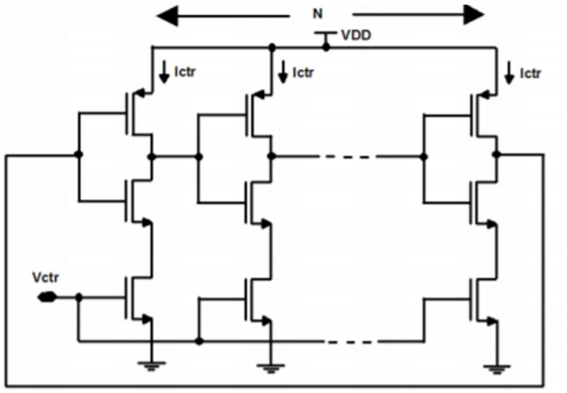

Figure 1. 23: Ring oscillator based VCO (Nebhen et al. 2012).

The inverter bias current is linear as a function of the sensor output voltage only over a reduced range. Hence, the oscillation frequency has a reduced linearity range with respect to the sensor output voltage. Besides, when temperature increases, the mobility degradation and the exponential increase in leakage current, cause a thermal drift of the inverters bias current. This affects temperature stability of the oscillation frequency. Consequently, the voltage to frequency conversion design technique is limited by the non-linearity of oscillation frequency and by the thermal drift of its internal components.

Recently, a solution that improves linearity of VCOs has been proposed by J.Nebhen, but the obtained non-linearity is still high at about 2% (Nebhen, Meillere, and Masmoudi 2017). Moreover, thermal sensitivity of the VCO frequency is higher than 100ppm/°C, this makes the overall frequency variation of the VCO based sensor interface too high for operation under very wide temperature range.

1.2.4.2. Pulse Width Modulation technique (PWM)

Pulse width modulation is a technique used to encode the sensor information into a square-wave signal whose duty cycle depends on the sensor output voltage (De Smedt, Gielen, and Dehaene 2012a) (Georg Glaser 2017). PWM technique has the advantage of delivering time-domain information with good accuracy only with only few components.

An obvious advantage compared to voltage to frequency conversion is the quasi-digital encoding of the information. Hence, PWM signals are less sensitive to noise than frequency modulated signals. This offers the advantage of maintaining the signal integrity during transmission (Fei Hu and Qi Hao 2016) (Patrick Powers 2012).

In the conventional implementation, the sensor output voltage is integrated. Then, it is compared to a reference voltage. Every time the integrated sensor output voltage reaches the reference voltage, the state of the PWM signal changes. The duty cycle of the so-obtained PWM signal is then a function of the sensor measure. Figure 1.24 shows the principle of the PWM technique.

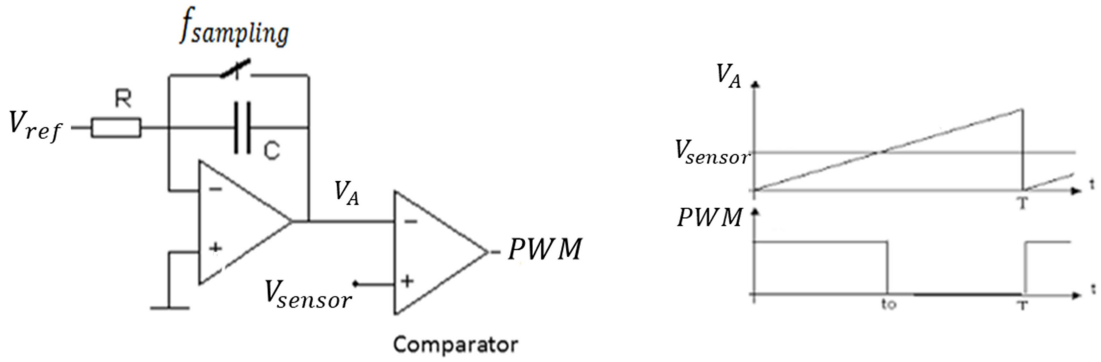

Figure 1. 24: Pulse Width Modulation technique (PWM).

Thermal stability of a PWM signal is limited by the temperature dependence of the reference voltage and the sampling frequency. Moreover, threshold voltage variations of the comparator and comparator's delay variations with temperature both degrade efficiency. The comparator's parameters are also very sensitive to ageing and process variations (Kokolanski et al. 2013).

PWM provides a linear relationship between sensor output voltage and duty cycle of the output signal, but only over a limited range of input voltage; e.g., due to the non-linearity of the ramp slope over the temperature range. Consequently, sensor interfaces using PWM technique are not adapted for sensors with large dynamic range in terms of output voltage. Higher signal distortion can be also obtained by heavy fluctuations in the power supply voltage.

A new PWM technique, proposed by V.De Smedt in (Smedt, Gielen, and Dehaene 2013), is based on a ratio-metric measure that is frequency independent. A differential sensor drives two delay stages; hence the sensor value is converted into a PWM signal whose duty cycle is the ratio of two delay measurements. The measured thermal drift of the sensor interface circuit is 79ppm/°C.

In (Gläser et al. 2017), G.Glaser proposed a PWM based sensor interface that amplifies the sensor output voltage by means of an analog amplifier before converting it in a PWM signal. Then, an elegant switching scheme is used to realize different measurements such as offset and temperature of the die. However, thermal drift of both gain and offset of the amplifier limits performances. Besides, performances of the switching scheme can be degraded by the increase in leakage currents with temperature. Two calibration points are used to compensate temperature drift and a ±43ppm/°C thermal drift is obtained.

1.3. Conclusion

A major interest in sensing systems, particularly in **sensor interfaces**, used for **high temperature applications** has been observed.

Conventional sensor interface architectures are not adapted for this harsh environment; their performances are degraded because of **thermal variation of CMOS technology**

parameters, and this limits their operation under this harsh condition. Main challenge of high temperature operation is the exponential increase in **leakage currents,** which deteriorates circuit functioning and might leads to its total destruction by inducing Latch up.

State of the art has shown that SOI CMOS technology has lower leakage currents than bulk CMOS technology due to the **isolation layer** below the active area. SOI transistors parameters are improved compared to bulk transistors and they beneficiate from a less temperature dependence of their parameters. Hence, **SOI appears more adapted for high temperature applications up to 300°C**. Moreover, the design of high temperature sensor interfaces must take into account changes in transistor parameters with temperature. High temperature design techniques reported in state of the art are then the use of **separate block hardening techniques**, **differential topology**, **closed loop architecture** and **time domain architecture**.

Time domain architecture achieves lowest temperature sensitivity because **time domain signals have a low temperature dependence** compared to analog signals due to their **high noise margin**. Besides, they are not affected by technology down scaling; this makes possible the use of low supply voltage and hence **reduces the power consumption**. Time domain architecture uses either a **VCO** to convert the sensor measure into a frequency or a **PWM technique** to convert the sensor measure into a PWM signal. This latter has advantages compared to VCO leading to **larger dynamic range** and to **a better signal integrity for transmission**. However, conventional PWM technique suffers from limitations. It is highly affected by **thermal variations of both reference voltage and sampling frequency**. Besides, it is limited by the high **sensitivity of the comparator to process variability and ageing**.

In order to get benefit of the advantages of PWM based techniques and to remedy its limitations, a novel PWM technique should be adopted. We are proposing another technique of PWM by means of **phase shifters** based on **Injection Locked Oscillators** (ILOs). The generated phase shift represents the pulse width of the PWM signal and it is a function of **the difference between two frequencies** where one of them is a function of the sensor output voltage. Using this novel PWM technique, no thermal stable frequency is required any more, which should lead to **simpler** and hence smaller circuits. The obtained phase shift depends on the **relative accuracy** of the phase shifter circuit parameters. Therefore, **low temperature sensitivity** can be achieved. Moreover, good **immunity to noise and process variations** can be obtained.

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Chapter 2:

High Temperature Sensor Interface based on PWM and Injection Locked Oscillators

In this chapter, a novel differential sensor interface architecture for resistive sensors, which is able to operate over a wide temperature range, is presented. This interface is based on voltage to pulse width modulation (PWM) signal conversion using injection locked oscillators (ILOs) as phase shifters.

The principle of the sensor interface is studied regardless of the topology of the ILOs. It is first established that such architecture depends on the ratio of device parameters rather than their absolute values. Finally, the resolution and the limitation of the proposed interface architecture are discussed.

2.1. Injection Locked Oscillators

2.1.1. Overview of Injection Locked Oscillators

An oscillator is an autonomous circuit that generates a periodic output signal. Injection Locked Oscillator (ILO) is a particular kind of oscillator with an external input signal as presented in figure 2.1. This external signal, called a locking signal, is periodic and it runs at a locking frequency f_{lock}.

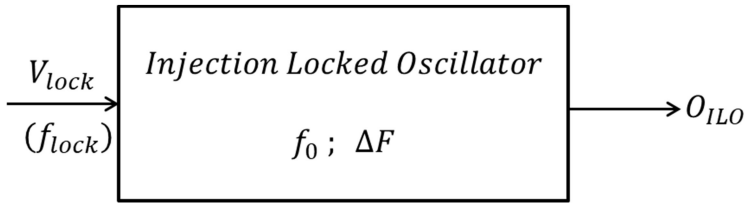

Figure 2.1: Illustration of Injection Locked Oscillators
(f_0 is the free running oscillation frequency and ΔF is the locking range).

In the absence of this locking signal, the ILO runs at its free running oscillation frequency f_0 which is defined by its topology and its components. When the locking signal is applied to the ILO and if its frequency is not too far from the free running frequency, the ILO tracks the locking signal and hence it oscillates at f_{lock}. This phenomenon is called injection locking and it appears only if f_{lock} is in a frequency range, called locking range, close to the free running frequency of the oscillator. Outside this range, the ILO runs at its free running oscillation frequency as presented in figure 2.2. The locking range is a function of the ILO topology and the locking signal strength.

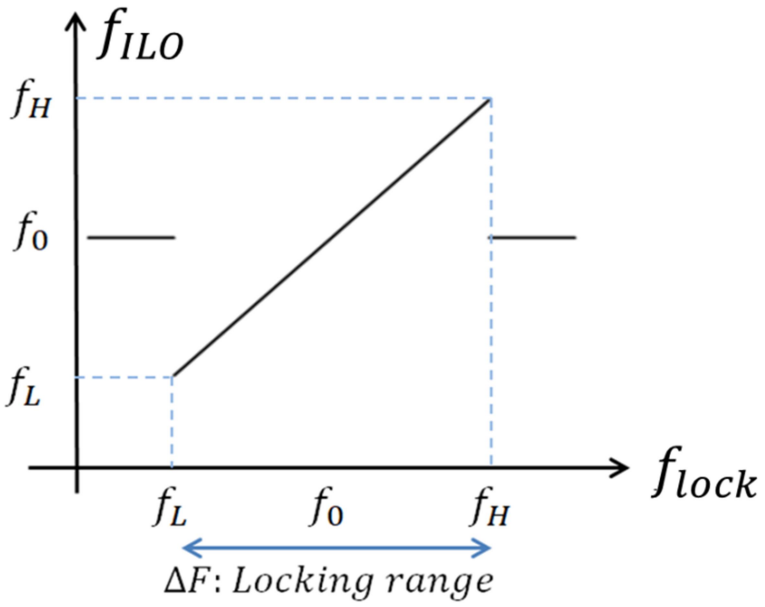

Figure 2.2: Characteristic function of Injection Locked Oscillators (f_{ILO} is the ILO oscillation frequency).

2.1.2. Properties of Injection Locked Oscillators (Huntoon & Weiss theory)

Injection locking is common to any kind of oscillators: mechanical, electrical and even biological. It was firstly discovered by Huygens (1629-1695) who observed that two clocks not beating at the same frequency end by being synchronized (i.e., locked) when they are coupled (Franck Badets 2000). Models of electrical Injection Locked Oscillators have been introduced by Alder in 1946 (Adler 1946). Later in 1947, Huntoon and Weiss studied theoretically the behaviour of Injection Locked Oscillators (Huntoon and Weiss 1947).

According to the theory, an ILO is considered as a black box in order to generalize this theory to ILOs with different topologies. The locking signal is connected in series with the ILO load Z (Figure 2.3).

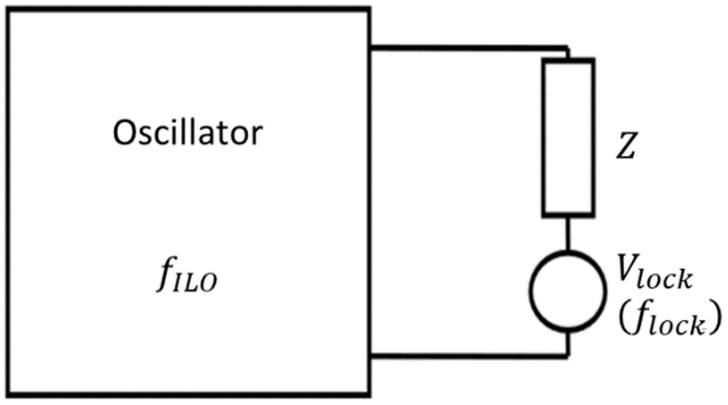

Figure 2.3: Injection Locked Oscillators representation (Franck Badets 2000).

This study is performed considering a sinusoidal locking signal and it is based on two main assumptions:

- Injection locking phenomenon appears in oscillators whose free running oscillation frequency is a continuous function of the load Z.
- The locking input signal V_{lock} can be modelled by a small variation in the load impedance (referred as "dz", as presented in figure 2.4) if the locking frequency is close to the free running frequency (i.e., f_{lock} is in the locking range).

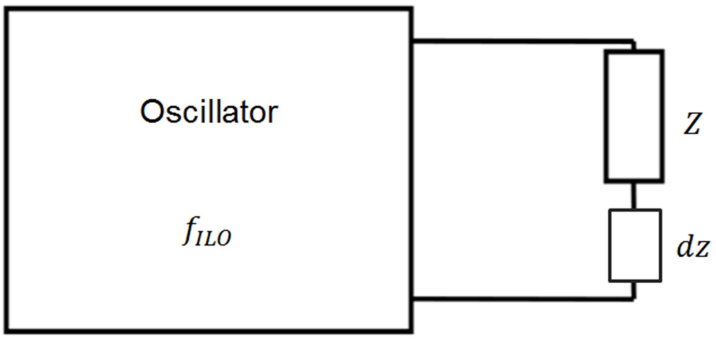

Figure 2.4: Representation of Injection Locked Oscillators at locking (Franck Badets 2000).

2.1.2.1 Phase shift of Injection Locked Oscillators

The locking signal V_{lock} generates a small variation "*dz*" of the load. Consequently, the frequency and the amplitude of the oscillator output are susceptible to be changed. The dependence of the oscillator output frequency and amplitude on the load impedance variation "*dz*" is specified using a set of compliance coefficients: the amplitude compliance coefficient E_A and the frequency compliance coefficient E_F.

$$E_A = \frac{\partial A}{dz} = |E_A|e^{j\alpha} \quad (2.1)$$

$$E_F = \frac{\partial f}{dz} = |E_F|e^{j\beta} \quad (2.2)$$

The locking signal is written as follows:

$$V_{lock} = |V_{lock}|e^{j2\pi f_{lock}} \quad (2.3)$$

Once locked, the ILO output signal is written as follows:

$$O_{ILO} = |O_{ILO}|e^{j2\pi f_{lock}+\Phi_{ILO}} \quad (2.4)$$

where $\emptyset_{ILO}$ is the phase shift of the ILO output with respect to the locking signal.

According to Huntoon and Weiss theory, this phase shift is governed by the compliance coefficients:

$$\frac{1}{2\pi}\frac{\partial \Phi_{ILO}}{\partial t} = (f_{lock} - f_0) - \frac{|E_F||V_{lock}|}{|I_0|}\cos(\Phi_{ILO} + \beta) \quad (2.5)$$

where I_0 is the current flowing in the oscillator load in the absence of locking signal and f_0 is the free running oscillation frequency of the ILO.

Once locked, $\frac{\partial \Phi_{ILO}}{\partial t}$ is equal to zero. Then, equation (2.5) becomes:

$$(f_{lock} - f_0) = \frac{|E_F||V_{lock}|}{|I_0|}\cos(\Phi_{ILO} + \beta) \quad (2.6)$$

where

$$\frac{|E_F||V_{lock}|}{|I_0|} = \frac{\Delta F}{2} \quad (2.7)$$

ΔF is the ILO locking range defined as the range of the locking frequency satisfying the injection locking conditions. Consequently, (2.6) becomes (2.8).

$$\cos(\Phi_{ILO} + \beta) = \frac{2(f_{lock} - f_0)}{\Delta F} \quad (2.8)$$

Therefore, the ILO phase shift with respect to the locking signal is given by:

$$\Phi_{ILO} = arcos\left(\frac{2(f_{lock} - f_0)}{\Delta F}\right) \quad (2.9)$$

Equation (2.9) shows an important property of Injection Locked Oscillators: the phase shift is a function of the difference between the locking signal frequency and the free running frequency (Figure 2.5).

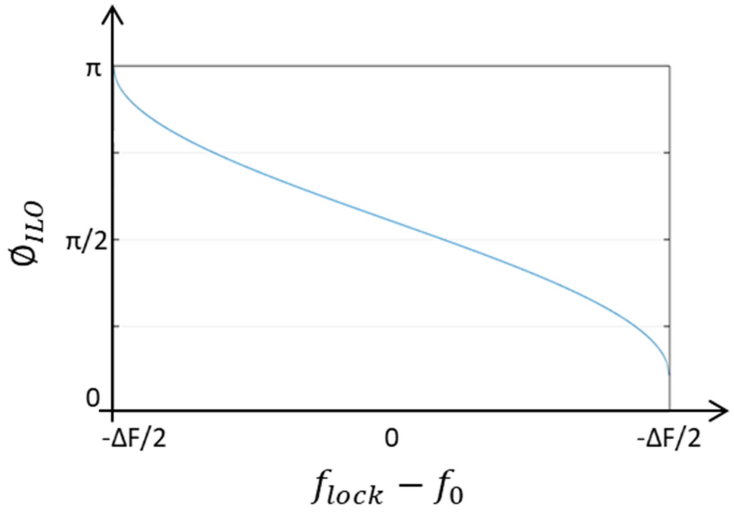

Figure 2.5: Phase shift of harmonic Injection Locked Oscillators.

2.1.2.2. Phase noise of Injection Locked Oscillators

ILOs have another interesting property that concerns the phase noise. Once locked, the ILO phase noise is the result of two main contributions: the oscillator's intrinsic phase noise and the phase noise of the locking signal.

The phase of a non-locked ILO can be expressed as follows:

$$\Phi_{ILO}(t) = 2\pi f_0 t + \Phi_{b0}(t) \quad (2.10)$$

where $\Phi_{b0}(t)$ is the oscillator phase noise due to all its noisy elements.

The phase of the locking signal is expressed as follows:

$$\Phi_{lock}(t) = 2\pi f_{lock} t + \Phi_{bS}(t) \quad (2.11)$$

where $\Phi_{bS}(t)$ is the phase noise of the locking signal.

Once locked, the output phase shift of the ILO is expressed as follows:

$$\Phi_{ILO}(t) = 2\pi f_{lock} t + \Phi_{\varepsilon}(t) - \Phi_0 \quad (2.12)$$

where $\Phi_{\varepsilon}(t)$ is the phase noise of the locked ILO. It includes the phase noise effect of the locking signal $\Phi_{bS}(t)$ and the internal phase noise of the oscillator $\Phi_{b0}(t)$. Φ_0 is a constant.

According to (Franck Badets 2000), the ILO phase noise is governed by the following equation:

$$\frac{d\Phi_{\varepsilon}}{dt} - \left[2\pi \frac{|E_F||V_{lock}|}{|I_0|} \sin(\Phi_{ILO} + \beta)\right] \Phi_{\varepsilon} = \frac{d\Phi_{b0}}{dt} - \left[2\pi \frac{|E_F||V_{lock}|}{|I_0|} \sin(\Phi_{ILO} + \beta)\right] \Phi_{bs} \quad (2.13)$$

Consequently, in the frequency domain, the ILO phase noise $\emptyset_{\varepsilon}$ contains the contribution of Φ_{bs} and Φ_{b0} as follows:

$$\Phi_{\varepsilon}(p) = \frac{p}{p + w_n} \Phi_{b0}(p) + \frac{w_n}{p + w_n} \Phi_{bs}(p) \quad (2.14)$$

f_n ($f_n = w_n / 2\pi$) is the noise bandwidth and it is expressed as:

$$f_n = -\frac{|E_F||V_{lock}|}{|I_0|} \sin(\Phi_{ILO} + \beta) = -\frac{\Delta F}{2} \sin(\Phi_{ILO} + \beta) \quad (2.15)$$

Therefore, in the ILO noise bandwidth, a locked ILO copies the phase noise of the locking signal while its internal phase noise is rejected (as shown in figure 2.6). This behaviour is similar to the behaviour of a first order PLL. Outside the noise bandwidth, the phase noise of the ILO is due to the internal components of the oscillator and the phase noise of the locking signal is rejected.

This means that in the ILO's noise bandwidth, the ILO's phase shift with respect to the locking signal is not affected by the noise of the internal oscillator. Moreover, this phase shift is insensitive to the phase noise induced by the locking signal because the ILO has the property of tracking this noise (Badets 2000, Finateu et al. 2005).

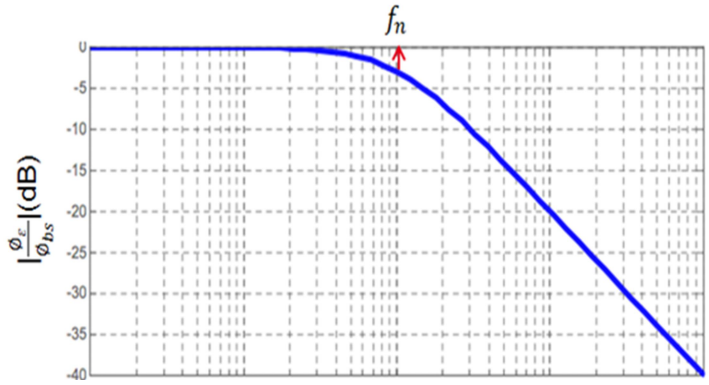

Figure 2.6: Bode diagram of the ILO phase noise over the locking signal phase noise.

2.2. High temperature PWM based sensor interface architecture using Injection Locked Oscillators

The sensor interface is designed for sensors delivering an output voltage; the most well-known example of this kind of sensors is resistive sensors. Using ILOs as phase shifters, the sensor output voltage is converted into a pulse width modulated signal (PWM) which is easily converted into a digital output.

2.2.1. Sensor interface principle based on voltage to PWM conversion

The phase shift of ILOs is a function of the difference between the locking frequency f_{lock} and the free running oscillation frequency f_0. Hence, ILOs can be used as phase shifters by controlling either f_{lock} or f_0.

Sensor interface can take benefit of this property. Firstly, the sensor output voltage is used to modify the free running oscillation frequency of the ILO f_0. The locking frequency f_{lock} is kept at a constant value in the ILO locking range. Then, a phase shift Φ_{ILO}, which is a function only of f_0, is obtained thanks to the property of ILOs. Hence, the sensor output voltage is converted into a phase shift Φ_{LO} (i.e., the phase shift of the ILO output with respect to the locking signal).

The delay t_{pw} between the locking signal V_{lock} and the ILO output O_{ILO} is then a function of the sensor voltage and it is linked to the phase shift of the ILO by:

$$t_{pw} = \frac{\Phi_{ILO}}{2\pi} T_{lock} \qquad (2.16)$$

This delay represents the pulse width of a Pulse Width Modulated (PWM) signal running at f_{lock} (Figure 2.7). The represented PWM signal can be obtained, for example, by connecting the ILO output O_{ILO} and the locking signal V_{lock} to a XOR logic gate enabled only when V_{lock} is at high logic level.

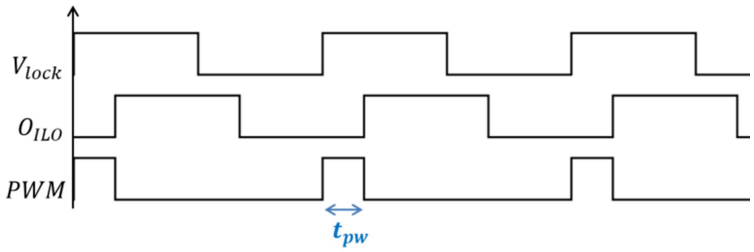

Figure 2.7: Representation of the output PWM signal.

According to the value of the sensor output voltage V_S, the ILO phase shift Φ_{ILO} varies between zero and π; thus the pulse width of the so-obtained PWM signal varies between zero and the half period of the ILO output (i.e., $T_{lock}/2$ because $f_{ILO}=f_{lock}$). Consequently, using ILOs, the sensor value is encoded into a PWM signal.

This PWM signal is then converted into a multi-bit digital output using a Time-to-Digital Converter (TDC). For this purpose, a high frequency counter is used as the simplest way of characterizing a PWM signal with high speed and high resolution (G.W.Roberts et al. 2010) (V.Sharma et al. 2016). The counter measures the pulse width t_{pw} and encodes it into a digital word N given by:

$$N = \frac{t_{pw}}{T_{counter}} \qquad (2.17)$$

where $T_{counter}$ is the period of the counter clock ($f_{counter}$ =1/$T_{counter}$; $f_{counter}$ is the counter clock frequency). Based on equation (2.16), the digital output can be also expressed as:

$$N = \frac{\Phi_{ILO}}{2\pi}\frac{f_{counter}}{f_{lock}} \qquad (2.18)$$

The counter clock is generated from the locking signal generator (presented under the name of Reference oscillator) by means of a frequency multiplier which can be implemented with a Phase Locked Loop (PLL) for example. This offers the advantage of a thermally stable ratio $f_{counter}/f_{lock}$ because the PLL is a closed loop circuit and it achieves a multiplication factor independent of temperature. Figure 2.8 is a possible implementation of a PWM based sensor interface using ILO. For a better robustness, a differential architecture will be presented in the next section.

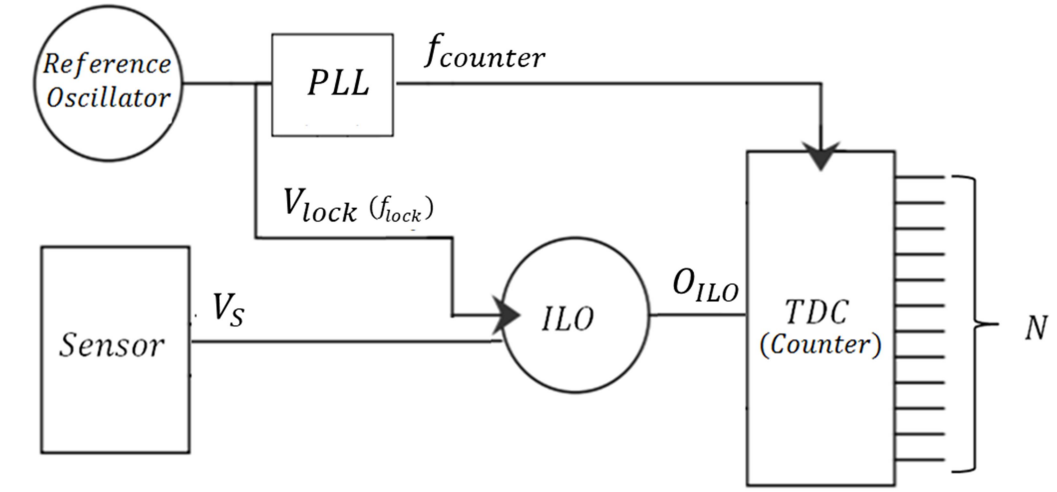

Figure 2.8: Schematic diagram illustrating the principle of the PWM based sensor interface using ILOs.

2.2.2. Architecture of the high temperature sensor interface

To improve the sensor interface performances, a differential PWM based architecture is proposed for conditioning resistive sensors with differential output voltage (for example resistive transducers embedded in a Wheatstone bridge). This differential architecture offers the advantage of rejecting the effects of process variations, temperature variations and common-mode noise.

The sensor interface converts the sensor differential output voltage into a PWM signal using a pair of ILOs. The differential sensor output voltage V_S is converted into a phase shift difference which represents the pulse width of the so-obtained PWM signal and which is then converted into a digital output using a counter. Figure 2.9 presents the architecture of the so-obtained sensor interface.

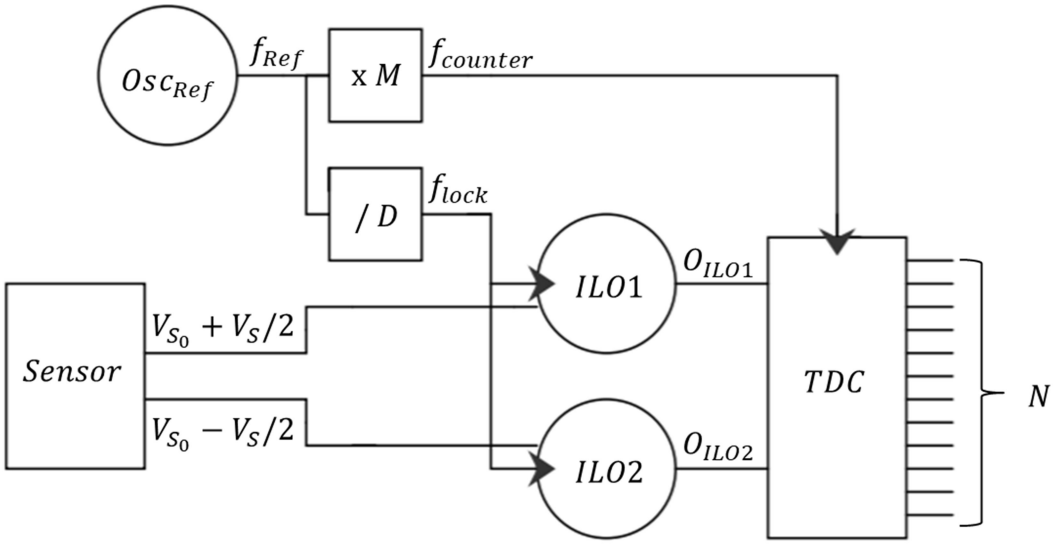

Figure 2.9: Architecture of the high temperature sensor interface.

The sensor output voltage V_S controls simultaneously the phase shifts of both ILO1 and ILO2 by controlling their free running oscillation frequencies f_{01} and f_{02} (they are respectively the free running oscillation frequencies of ILO1 and ILO2).

When the sensor output voltage V_S is zero, f_{01} and f_{02} are equal; hence both ILOs have the same phase shift with respect to the locking signal. Then, the variation of the sensor output voltage V_S makes the ILO free running oscillation frequencies f_{01} and f_{02} vary symmetrically with V_S. Consequently, the phase shifts of ILO1 Φ_{ILO1} and the phase shift of ILO2 Φ_{ILO2} vary symmetrically with respect to their initial values at zero V_S. The obtained difference between Φ_{ILO1} and Φ_{ILO2}, $\Delta\Phi_{out}$, is a function of the differential output voltage of the sensor, V_S, and defines the output of the sensor interface circuit.

The sensor interface is designed so that, at zero V_S, the initial phase shift of both ILOs would be equal to $\pi/2$ with respect to the locking signal. Consequently, each ILO output will have a full scale of $\pm\pi/2$. Hence, the full scale of the difference (Φ_{ILO1} - Φ_{ILO2}) is $\pm\pi$ (equivalent to $\pm T_{lock}/2$) which represents the output full scale of the sensor interface.

Considering the difference between phase shifts of both ILOs, a PWM signal is obtained whose pulse width is defined by $\Delta\Phi_{out}$ ($\Delta\Phi_{out} = |\Phi_{ILO2} - \Phi_{ILO1}|$) as follows:

$$t_{pw} = \frac{\Delta\Phi out}{2\pi f_{lock}} \qquad (2.19)$$

Then, the obtained pulse width of the PWM signal is encoded into digital information using a high frequency counter that works as follows: on rising edge of either O_{ILO1} or O_{ILO2}, depending on which signal is in phase advance (O_{ILO1} for positive V_S and O_{ILO2} for negative V_S), the counter starts counting and it is incremented at each rising edge of the counter clock. Counting stops at the rising edge of the other O_{ILO} and the value stored in the counter is then proportional to t_{pw} which is in turn proportional to the sensor output voltage V_S. After each cycle, the counter output is stored in a register and then, counter is reset till the next enable signal (i.e., the next rising edge of either O_{ILO1} or O_{ILO2}). The TDC resolution is defined by the counter clock frequency; higher is this frequency, higher is the resolution. This is obvious from the expression of the digital output of the sensor interface:

$$N = \frac{t_{pw}}{T_{counter}} = \frac{T_{lock}}{T_{counter}} \frac{\Delta\Phi_{out}}{2\pi} = \frac{f_{counter}}{f_{lock}} \frac{|\Phi_{ILO2} - \Phi_{ILO1}|}{2\pi} \qquad (2.20)$$

In the proposed architecture of the sensor interface, counter clock and locking signal are both generated from the same reference oscillator Osc_{Ref}. The counter clock frequency is generated using a PLL as a frequency multiplier, while the locking signal is obtained by means of a frequency divider. This choice is made in order to reduce the multiplication factor of the PLL for the sake of its bandwidth. In fact, it is highly desirable to increase the PLL bandwidth in order to cancel out the phase noise of the voltage-controlled oscillator in the largest possible bandwidth.

Figure 2.10 depicts the timing diagram of the sensor interface. Only the case of positive sensor output voltage is presented. When V_S increases, f_{01} increases, while f_{02}

decreases. Since the ILO phase shift is inversely proportional to the ILO free running oscillation frequency (Equation (2.9)), Φ_{ILO1} decreases and Φ_{ILO2} increases for a positive V_S. For negative V_S, the opposite happens. Therefore, an additional bit is added to the TDC output to determinate the sign of V_S by detecting which ILO is in phase advance with respect to the other one.

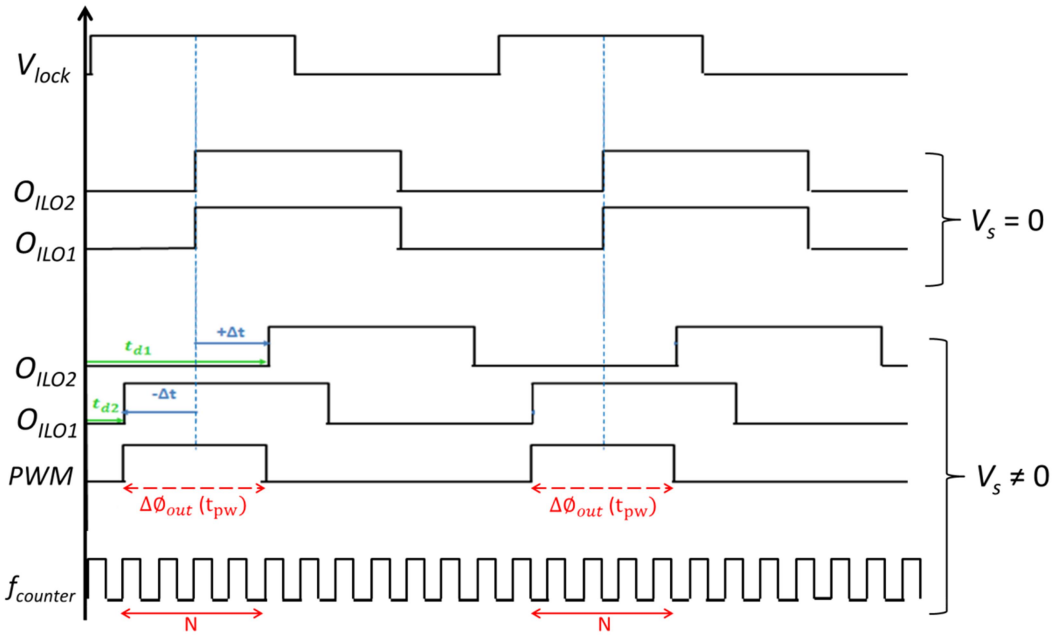

Figure 2.10: Timing diagram of the sensor interface architecture.

2.2.3. Thermal stability

Since digital signals are highly immune to temperature variations, the proposed time domain architecture is expected to exhibit a low temperature dependence.

Regardless of the topology of oscillators, the sensor interface output is a function of the ratio of its parameters rather than their absolute values. That is why, the architecture of the sensor interface is supposed to be thermally stable.

As expressed in equation (2.21), the digital output, and thus its thermal stability, depends on the ratio of two frequencies ($f_{counter}/f_{lock}$) and on the difference of two phase shifts (Φ_{ILO2}-Φ_{ILO1}).

2.2.3.1. Thermal stability of the ratio $f_{counter}/f_{lock}$

The counter frequency and the locking signal are both generated from the same reference oscillator. Then, the thermal stability of the ratio ($f_{counter}/f_{lock}$) depends on the thermal stability of the frequency division and the frequency multiplication factors, D and M respectively. The frequency divider, used to generate the locking signal, is a digital circuit. Hence, it is thermally stable. The multiplicative PLL is a closed loop circuit. Then, it achieves the same multiplication factor over the temperature range. Therefore, the ratio ($f_{counter}/f_{lock}$) is temperature independent.

2.2.3.2. Thermal stability of $\Delta\Phi_{out}$

The output phase shift $\Delta\Phi_{out}$ is defined as the difference between the phase shifts of two ILOs. Since both ILOs have the same topology; they present the same thermal dependence and hence, their phase shifts Φ_{ILO2} and Φ_{ILO1} have the same thermal drift. Therefore, thanks to the differential architecture, the difference of phase shifts ($\Delta\Phi_{out} = \Phi_{ILO2} - \Phi_{ILO1}$) is not affected by temperature variations.

2.2.3.3. Effect of process variations on thermal stability

The differential architecture offers a good immunity against process variations. Both oscillators will have the same sensitivity to temperature over process variations. Hence, the phase shifts of the two ILOs, Φ_{ILO1} and Φ_{ILO2}, are expected to have similar temperature dependence whatever are the process parameters. Therefore, the sensor interface output which is defined as the difference between the ILOs phase shifts ($\Phi_{ILO2} - \Phi_{ILO1}$) has a good thermal stability regardless of the process parameters. Of course, mismatches between both ILOs may induce some mismatches in thermal dependence.

As a conclusion of previous subsections 2.2.3.1, 2.2.3.2 and 2.2.3.3, the presented sensor interface architecture achieves a low sensitivity to temperature variations over a wide temperature range.

2.2.4. Resolution of the sensor interface

Resolution of the sensor interface is defined by the ratio of two parameters: the full scale of the output time delay t_{pw} (equivalent to the output phase shift $\Delta\Phi_{out}$) and the minimum detectable delay.

The full scale of the delay t_{pw} is the maximum pulse width of the obtained PWM signal. It is equal to the half period of the ILO output (or of the locking signal because $T_{ILO}=T_{lock}$):

$$t_{pw_{FS}} = \frac{T_{lock}}{2} = \frac{1}{2\,f_{lock}} \quad (2.21)$$

The minimum detectable time delay is the smallest pulse width value that the counter is able to measure. It corresponds to the counting period $T_{counter}$.

Then, the resolution of the sensor interface is defined by the ratio of the counter frequency and the locking frequency as expressed in (2.22):

$$2^{Resolution} = \frac{t_{pw_{FS}}}{T_{counter}} = \frac{1}{2}\frac{f_{counter}}{f_{lock}} \quad (2.22)$$

where *Resolution* is considered as an equivalent number of bits.

Due to the use of a common reference oscillator, both frequencies of the above equation can be expressed as:

$$f_{lock} = \frac{f_{Ref}}{D} \quad (2.23)$$

$$f_{counter} = M\, f_{Ref} \quad (2.24)$$

where D is the frequency division factor, M is the PLL multiplication factor and f_{Ref} is the reference oscillator frequency. Therefore, it can be written:

$$2^{Resolution} = \frac{1}{2}.M.D \quad (2.25)$$

Finally, as expressed in equation (2.25), the resolution of the sensor interface is defined by the PLL multiplication factor M and the frequency division factor D.

2.2.5. Limitation of the proposed sensor interface architecture

The presented architecture is adapted to any type of ILOs (i.e., harmonic and non-harmonic). However, its overall linearity is limited by the non-linearity of the ILOs.

In fact, based on the Huntoon and Weiss study on the phase shift of harmonic ILOs, the ILO phase shift follows an arcos function of (f_{lock}-f_0). Hence, the linear range of the ILO phase shift is limited to a phase shift range of π/2 (Figure 2.5) (i.e., the linear range is limited to very small differences between the locking frequency f_{lock} and the ILO free running frequency f_0). This limited linear behaviour of the ILO decreases the linear range of the PWM sensor interface based on harmonic ILOs to the half of the full scale.

2.3. Conclusion

The proposed sensor interface is based on a **time-domain** and **fully differential** architecture. It converts the sensor output voltage into a digital output and takes benefit of the properties of **Injection Locked Oscillators** when used as **phase shifters**. The presented architecture is generic and it could be **adapted to any type of ILOs**.

Time domain architecture leads to a quasi-digital circuit. This ensures better **immunity to noise**. In addition, differential architecture makes the sensor interface depend on ratios of the circuit parameters instead of their absolute values: **low dependence to temperature** is then expected.

However, the overall linearity of the sensor interface is limited by the non-linearity of the ILO. The linearity range of this PWM sensor interface based on harmonic ILOs is **limited to the half of the output full scale** because of the limited linear range of harmonic ILOs. Therefore, **an ILO with an extended linear range is required** to improve the linear behaviour of the sensor interface.

2.4. References

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Chapter 3:

Sensor Interface Circuit Design: From Concept to Implementation

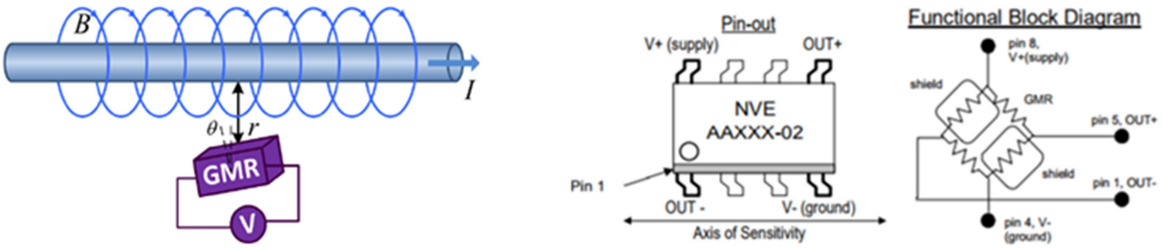
This chapter describes the process of designing the high temperature sensor interface presented in chapter 2; its specifications and its implementation using Relaxation Injection Locked Oscillators (RILO) that has been chosen because of their extended linearity range compared to harmonic ILOs.

Section 3.1 introduces the applicative context of the sensor interface. Section 3.2 justifies the choice of a RILO and presents its topology. The architecture of the RILO based sensor interface is presented in section 3.3. A behavioural model of the sensor interface has been developed in order to validate the architecture and the parameters values of its constitutive blocks. Section 3.4 details the implementation of the constitutive blocks considering the high temperature environment. Finally, simulation results over a wide temperature range are reported in section 3.5; they show that the sensor interface has an excellent thermal stability.

3.1. Context of the sensor interface circuit and specifications

The application of the sensing system consists in measuring the current for the control and monitoring of electrical engines. Precisely, the sensing system is used to measure the current that flows inside the power drivers controlling electrical engines.

The current sensor is based on Giant Magneto Resistances (GMR). It works as follows: the current induces a magnetic field and the GMR value changes as a function of this magnetic field (Ouyang et al. 2012) (Figure 3.1). A GMR current sensor from NVE (Figure 3.1), "component of the shelf", was chosen because it has a large temperature range. This sensor is connected as a Wheatstone bridge and delivers a differential voltage as a function of the measured current.



GMR current sensor (Ouyang et al. 2012) GMR sensor from NVE ("NVE AA and AB-Series Analog Sensors" n.d.)
Figure 3. 1: Illustration of current measurement using GMR based current sensor.

The measured current is converted into a magnetic field according to the following equation:

$$B = \frac{\mu_0 I_{measured}}{2\pi r} \qquad (3.1)$$

where μ_0 is the magnetic permeability constant, equal to $4\pi 10^{-7}$ T.m/A, and r is the distance between the sensor and the electrical wire.

Since the current sensor has a 4.2mV/Oe typical sensitivity with a 1.2V excitation voltage, knowing that in an environment having a relative permeability of 1, B(T)=10^{-4}H(Oe), the sensor output voltage is related to the magnetic field by the following equation:

$$V_S(V) = 42\,B \quad (3.2)$$

Consequently, replacing equation (3.1) into (3.2), the sensor output voltage V_S can be written as a function of the measured current as follows:

$$V_S\,(mV) = 8.4\,\frac{I_{meas}}{r\,(in\,mm)} \quad (3.3)$$

Taking r = 1.4 mm, equation (3.3) is written as:

$$V_S\,(mV) = 6\,I_{meas} \quad (3.4)$$

Taking into account a full scale of current of ±11A, the sensor output voltage has ±66 mV full scale. The minimum detectable current must be in the order of 5 mA, this means that the current must be measured with 11 bits of resolution (11A/2^{11}=5.37mA) plus one bit of sign. This also means that the so-obtained ADC needs a gain of 31 LSB/mV (2^{11}/66).

The sensing system will be used to measure the current flowing inside the power drivers of industrial engines. Hence, the overall sensing system is exposed to high temperatures (the operation temperature may exceed 200°C). This harsh operation environment must be taken into account in the design of the sensor interface.

3.2. Architecture of the Injection Locked Oscillator

3.2.1. Harmonic versus non- harmonic Injection Locked Oscillators

Considering any kind of electrical ILO, the phase shift of the ILO output with respect to the locking signal is a function of the difference between the free running oscillation frequency f_0 and the locking frequency f_{lock}. Harmonic ILOs (HILOs) suffer from reduced linear range. In fact, as expressed in previous chapter (Equation (2.9)), the phase shift of HILOs is an arcos function of (f_{lock} - f_0) and therefore the linear range of HILOs is limited (i.e., the linear behaviour is limited to a phase shift range of π/2). Therefore, phase shifters and hence sensor interfaces based on HILOs exhibit a limited linear range.

That is why, to achieve a good linear behaviour, relaxation ILOs (i.e., non-harmonic ILOs) seem to be good candidates because they rely on the charge and discharge of capacitors with a constant current. Their behaviour is then linear by nature.

Moreover, the use of relaxation ILOs (RILOs) offers additional advantages. They have higher locking range than harmonic ILOs because relaxation oscillators have low quality factor compared to harmonic oscillators (Razavi 2004) (Zhou and Yuan 2015). This leads to higher resolution bandwidths where the ILO rejects the noise of its components. Besides,

RILOs offer easier integration for low oscillation frequencies making them more adapted for low bandwidth applications, which is our case.

Motivated by these advantages, it has been decided to use RILOs in the sensor interface presented in chapter 2.

3.2.2. Architecture of Relaxation Injection Locked Oscillator

3.2.2.1. Topology of the Relaxation Injection Locked Oscillator

3.2.2.1.1. Relaxation free running oscillator

The free running oscillator is the relaxation oscillator presented in figure 3.2 (F. Badets et al. 2004). It is based on the alternate charges of two capacitors C_1 and C_2 with the same current; when one capacitor is charged, the other capacitor is grounded. The voltage across the charged capacitor is compared with a reference voltage (here the switching voltage of an inverter). The time duration required to reach this reference, which depends on the capacitor value and the charge current, defines the oscillation period.

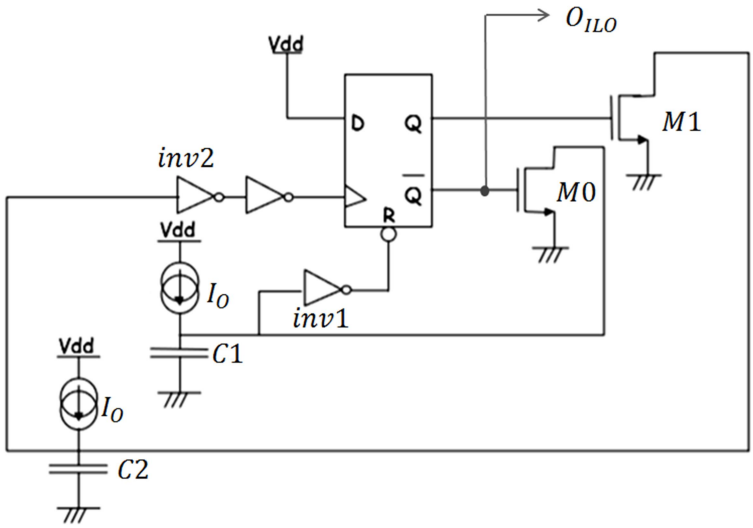


Figure 3.2: Schematic of relaxation free running oscillator.

In order to explain the operation principle of the free running oscillator, the output of the oscillator O_{ILO} is assumed equal to zero at initial state. Therefore, the output of the flip flop DFF is at high logic level. Hence, M1 is on while M0 is off. The voltage U_{C2} across C_2 capacitor is grounded while the capacitor C_1 is charged by the bias current I_0. The voltage across C_1 increases from zero to the switching voltage of the inverter inv1. At this time, the reset signal R goes to "1"; the DFF is reset, its logic output is low and the ILO output is high. This turns off M1 and turns on M0. The voltage across C_1 is grounded while the capacitor C_2 is charged by the bias current I_0 until the switching voltage of inv2. When this voltage is reached, a rising edge appears at the clock input of the DFF, the flip-flop copies its input signal, which is at high logic level, and output switches from 1 to 0.

This cycle is repeated continuously, which makes ILO output oscillate between low and high logic levels with a frequency defined by the current source, the capacitance and the switching voltage of both inverters.

The duty cycle of the obtained output signal is defined by capacitances C_1 and C_2 (Equation (3.5)). Therefore, in order to obtain a 50% duty cycle, identical values are adopted for C_1 and C_2 (assuming that both inverters have identical switching voltage and both current sources are the same).

$$duty\ cycle = \frac{C_2}{C_2 + C_1} \qquad (3.5)$$

Figure 3.3 shows the timing diagram of the relaxation free running oscillator for two identical capacitances.

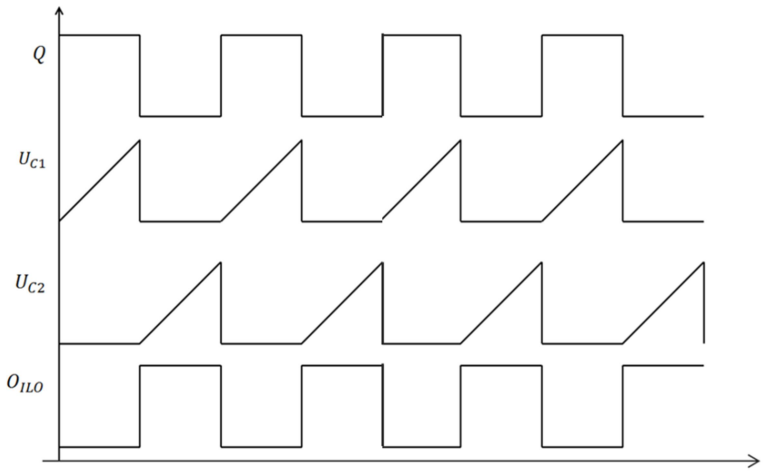


Figure 3.3: Timing diagram of the free running oscillator.

The oscillation frequency of the relaxation free running oscillator is given by:

$$f_0 = \frac{I_0}{2\ C\ V_{th}} \qquad (3.6)$$

where C is the capacitance of C_1 and C_2 and V_{th} is the switching voltage of the inverters.

3.2.2.1.2. Relaxation oscillator under injection locking

A circuit based on a differential pair is used to lock the free running oscillator frequency to the frequency f_{lock} of an external signal V_{lock} (F. Badets et al. 2004) by modulating the charging currents of the capacitors which define the oscillation frequency. The locking is performed by varying periodically the capacitors charge current to make the average charging current equal to the current that makes the oscillator run at the locking frequency f_{lock}. This current is from now refereed as I_{ch} and it is given by:

$$I_{ch} = 2\ f_{lock}\ C\ V_{th} \qquad (3.7)$$

Figure 3.4 shows the topology of the ILO; the free running oscillator and the locking circuit.

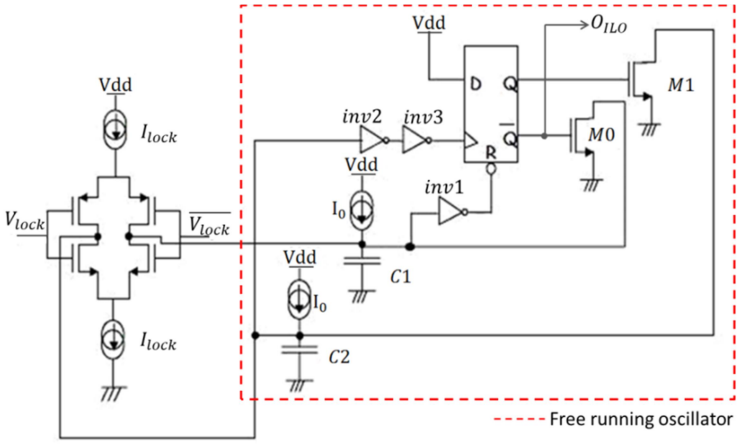


Figure 3. 4: Schematic of the Relaxation Injection Locked Oscillator.

A locking current is added or subtracted to the nominal capacitor charging current I_0 according to the value of V_{lock}. For example, at high level of V_{lock}, a current I_0-I_{lock} flows into *C2*, while a current I_0+I_{lock} charges *C2* at low level of V_{lock} (Figure 3.5). However, the capacitor *C2* is charged only when the ILO output is at high level. Hence, in order to be able to adjust the charge current by adding and subtracting the locking current, the ILO output O_{ILO} and the locking signal V_{lock} should not have the same phase.

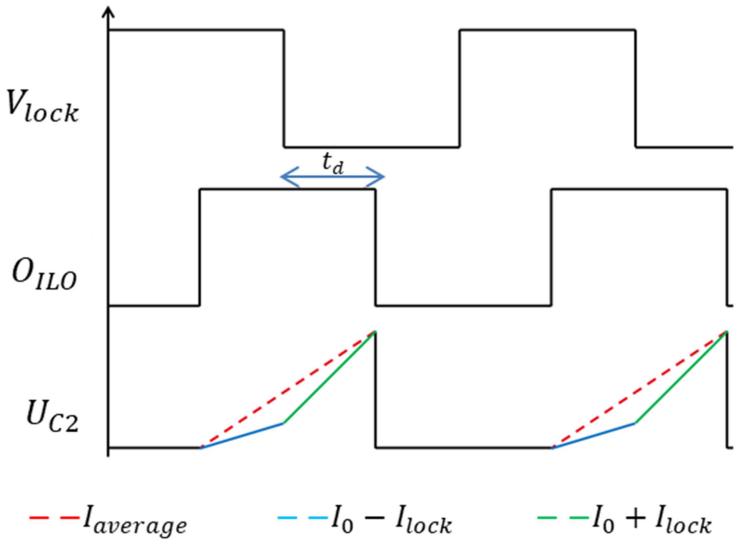


Figure 3.5: Timing diagram of the Injection Locked Oscillator.

Table 3 presents the charge current of the two capacitors *C1* and *C2* according to the logic level of O_{ILO} and V_{lock}.

Table 3. Charging current of the two capacitors.

O_{ILO}	V_{lock}	*C1*	*C2*
0	0	I_0+I_{lock}	X[1]
0	1	I_0-I_{lock}	X[1]
1	1	X[1]	I_0-I_{lock}
1	0	X[1]	I_0+I_{lock}

[1] X means that the capacitor is grounded.

Based on figure 3.5, the average charge current of *C2*, $I_{average}$, is expressed as a function of the time delay t_d between O_{ILO} and V_{lock}, the nominal charge current I_0, the locking current I_{lock} and the locking period T_{lock} (Figure 3.5).

$$I_{average} = \frac{(I_{lock} + I_0)t_d + (I_0 - I_{lock})(\frac{T_{lock}}{2} - t_d)}{\frac{T_{lock}}{2}} = I_0 + I_{lock}(4\frac{t_d}{T_{lock}} - 1) \qquad (3.8)$$

The time delay t_d, equivalent to the phase shift of the ILO output with respect to the locking signal, is comprised between 0 (obtained if $I_{average}=I_0-I_{lock}$) and $T_{lock}/2$ (obtained if $I_{average}=I_0+I_{lock}$).

3.2.2.2. Phase shift of the Relaxation Injection Locked Oscillator

The locking process sets the time delay between the ILO output O_{ILO} and the locking signal V_{lock} to the right delay that ensures an average charge current equal to I_{ch}. Therefore, using equations (3.7) and (3.8), it can be written:

$$I_0 + I_{lock}(4\frac{t_d}{T_{lock}} - 1) \; = \frac{2\,C\,V_{th}}{T_{lock}} \qquad (3.9)$$

The time delay t_d and hence the phase shift of the ILO output Φ_{ILO} with respect to the locking signal can be derived from equation (3.9):

$$t_d = \frac{C\,V_{th}}{2\,I_{lock}} - \frac{T_{lock}}{4}\left(\frac{I_0}{I_{lock}} - 1\right) \qquad (3.10)$$

$$\Phi_{ILO} = \frac{2\pi\,t_d}{T_{lock}} = \frac{\pi}{2} + \frac{\pi}{2I_{lock}}\left(\frac{2C\,V_{th}}{T_{lock}} - I_0\right) \quad (3.11)$$

Knowing that: $f_0 = \frac{I_0}{2\,C\,V_{th}}$ (cf. equation (3.6)); the ILO phase shift is given by:

$$\Phi_{ILO} = \frac{\pi}{2} + \frac{\pi\,C\,V_{th}}{I_{lock}}\,(f_{lock} - f_0) \qquad (3.12)$$

Equation (3.12) shows that the phase shift of the RILO is a linear function of (f_{lock}-f_0). This proves the extended linear range of RILOs compared to their harmonic counterparts whose phase shift is $\Phi_{ILO} = arcos\left(\frac{2(f_{lock}-f_0)}{\Delta F}\right)$.

From equation (3.11), it can be noticed that the phase shift of the RILO is also a linear function of the ILO bias current I_0. Then, once this ILO is used in the sensor interface, if the ILO bias current is a linear function of the sensor output voltage V_S, the ILO phase shift will be highly linear with respect to V_S.

3.2.2.3. Locking range of the Relaxation Injection Locked Oscillator

The locking range of ILOs is defined by the locking frequency range where the ILO output is able to be locked on the locking signal (i.e., the ILO output runs at f_{lock}) (Huntoon

and Weiss 1947). It is limited by a lower locking frequency F_L and an upper locking frequency F_H. F_L is defined by a zero phase shift between O_{ILO} and V_{lock} (i.e., $t_d = 0$) and F_H is defined by a π phase shift between O_{ILO} and V_{lock} (i.e., $t_d = T_{lock}/2$). Hence, F_L and F_H are obtained from (E.Chabchoub et al. 2017):

$$0 = \frac{C\ V_{th}}{2\ I_{lock}} - \frac{1}{4\ F_L}\left(\frac{I_0}{I_{lock}} - 1\right) \quad (3.13)$$

$$\frac{T_{lock}}{2} = \frac{C\ V_{th}}{2\ I_{lock}} - \frac{1}{4\ F_H}\left(\frac{I_0}{I_{lock}} - 1\right) \quad (3.14)$$

Hence, F_L and F_H are expressed as:

$$F_L = \frac{I_0 - I_{lock}}{2CV_{th}} = f_0 - \frac{I_{lock}}{2\ C\ V_{th}} \quad (3.15)$$

$$F_H = \frac{I_0 + I_{lock}}{2CV_{th}} = f_0 + \frac{I_{lock}}{2\ C\ V_{th}} \quad (3.16)$$

Consequently, the RILO locking range is given by this equation:

$$\Delta F = 2\frac{I_{lock}}{2\ C\ V_{th}} = 2\frac{I_{lock}}{I_0} f_0 \quad (3.17)$$

Equation (3.17) shows that the locking range is a function of the ILO topology (i.e., the capacitors value and the inverters threshold voltage V_{th}), its free running frequency f_0, its biasing current I_0 and the locking signal strength (i.e., the locking current I_{lock}).

3.2.2.4. Simulation of the Relaxation Injection Locked Oscillator (locking range and phase shift)

The RILO has been designed using a 0.18µm Partially-Depleted-Silicon-On-Insulator (PD-SOI) technology. The ILO parameters are the locking current I_{lock}, the locking frequency f_{lock} and the capacitance value C. The capacitance value C and the locking frequency are fixed to 10pF and 35kHz respectively. A locking current of 400nA is chosen to limit the ILO power consumption.

3.2.2.4.1. Simulation of the locking range

In order to characterise the ILO locking range (i.e., the range of f_{lock} where the ILO is locked), we vary f_{lock} while the free running oscillation frequency f_0 is kept constant (at 35kHz for example).

According to equation (3.17), the theoretical locking range ΔF is equal to 40kHz and it should be ranged from 15kHz (i.e., f_0-ΔF/2) to 55kHz (i.e., f_0+ΔF/2). Figure 3.6 shows some simulations of the output signal for locking frequencies ranging from 15 kHz up to 55kHz. It is demonstrated that the locking range is equal to 39kHz and that it is extended from 16 kHz up to 55kHz. Reversely, there is no locking for frequencies below 16 kHz (Figure 3.6.a) and above 55kHz (Figure 3.6.d).

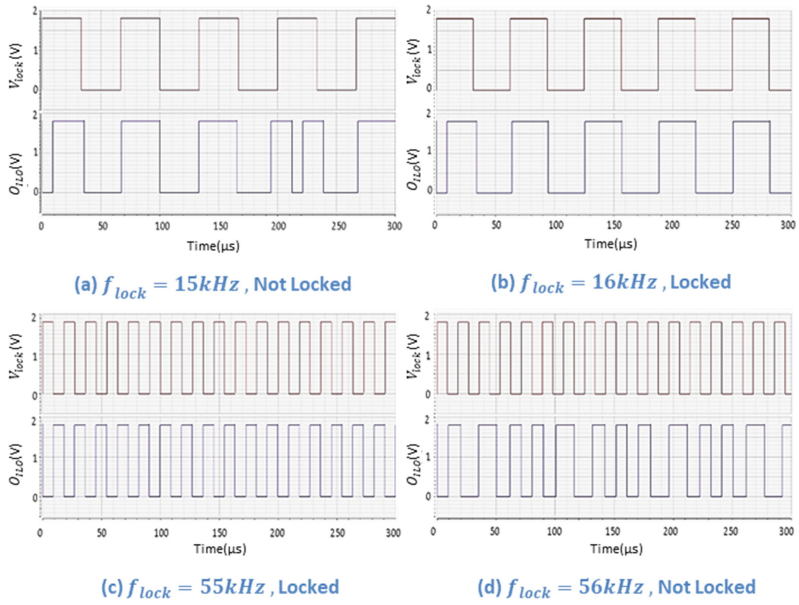


Figure 3. 6: Simulation of the Relaxation Injection Locked Oscillator for different locking frequencies.

3.2.2.4.2. Simulation of the phase shift

In order to simulate the ILO phase shift, its locking frequency f_{lock} is fixed to 35kHz while its free running oscillation frequency f_0 is swept from about 16kHz up to 55kHz by sweeping its bias current I_0 (from 320nA to 1.1µA).

Figure 3.7 reports the obtained phase shift, Φ_{ILO}, as a function of (f_{lock}- f_0). A good linear behaviour is obtained; the maximal linearity error is of 0.046% and the goodness-of-fit of the linear regression is of 0.9996 (R^2).

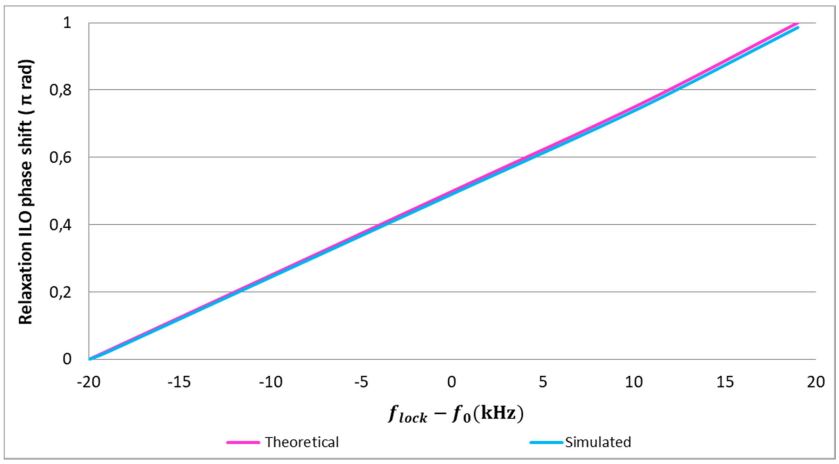


Figure 3.7: Phase shift of Relaxation Injection Locked Oscillator.

Simulation results of the last two sub-sections are in good agreement with the previous theoretical study. It is also confirmed that RILOs have a very good linearity over the entire locking range.

3.3. High temperature sensor interface using Relaxation Injection Locked Oscillators

3.3.1. Architecture of the proposed sensor

Figure 3.8 presents a detailed architecture of the proposed high temperature sensor interface. Compared to the previously given architecture (Figure 2.9), a Transconductance amplifier is added to perform the voltage-current conversion, and this in order to be able to control the RILOs free running oscillation frequencies by the sensor output voltage V_S. In addition, a *Bias* block has been added to generate all biasing currents of the sensor interface; the locking current I_{lock}, the bias current of the Transconductance Amplifier (TA) I_{GM} and the bias current of the reference oscillator I_{oscRef}.

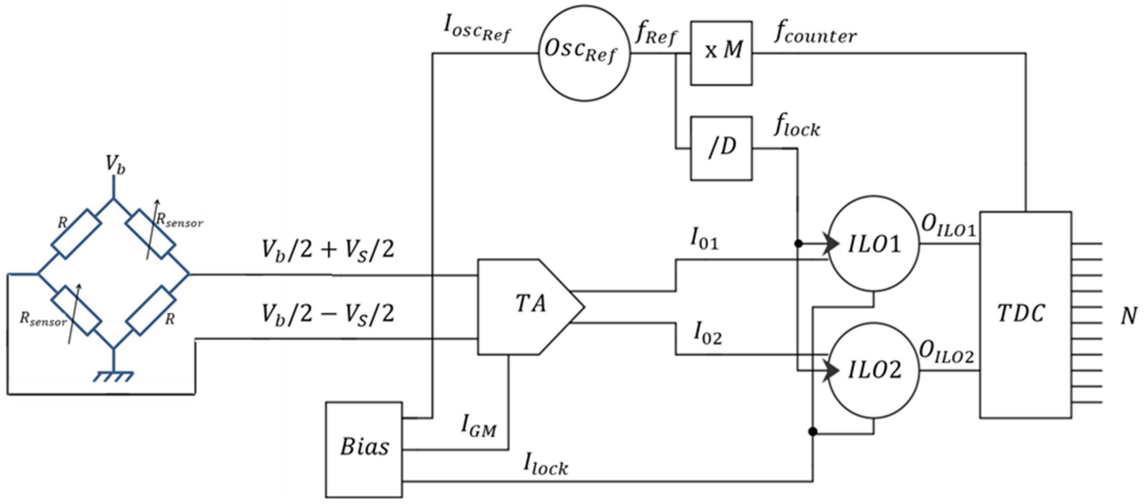


Figure 3.8: Sensor interface circuit based on Relaxation ILOs.

This interface converts the differential output voltage of the sensor into a pair of currents I_{01} and I_{02} thanks to a Transconductance Amplifier (TA). Both currents are then used to control the free running frequencies of both ILOs. The TA output currents (I_{01} and I_{02}) vary symmetrically as a function of the sensor output voltage V_S; this makes the free running frequencies of ILO1 and ILO2 (f_{01} and f_{02} respectively) also vary symmetrically. I_{lock} being constant, a phase shift difference appears between both ILOs outputs as soon as I_{01} and I_{02} are not equals; the sensor output voltage then drives proportionally and symmetrically the phase shifts of both ILOs (Φ_{ILO1} and Φ_{ILO2} which are respectively the phase shifts of ILO1 and ILO2). The difference Φ_{ILO2}-Φ_{ILO1} is hence a function of the sensor output voltage.

3.3.2. Behavioural modelling of the RILO based sensor interface

A behavioural model has been developed using Verilog AMS, a high level modelling language. This model is developed in order to validate the overall architecture of the sensor interface from a behavioural point of view. Furthermore, it is used to validate the circuit parameters and the specification of its blocks.

3.3.2.1. Behavioural modelling of elementary blocks

Figure 3.9 presents the behavioural model of the sensor interface where the constitutive blocks are considered as non-bandwidth-limited linear transfer functions (i.e., the bandwidths of these blocks are higher than that of the overall sensor interface).

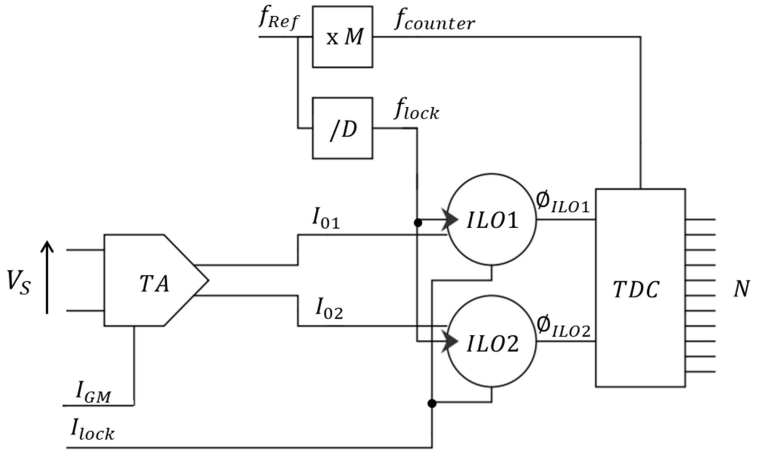


Figure 3.9: Illustration of the sensor interface behavioural model.

- Transconductance amplifier (TA): the TA generates two symmetrical currents I_{01} and I_{02} as follows:

$$I_{01} = I_{GM} + G_m V_s \quad (3.18)$$

$$I_{02} = I_{GM} - G_m V_s \quad (3.19)$$

where G_m is the transconductance (its gain) of the TA block.

- Injection locked oscillator (ILO): the ILO is modelled considering that its input is the bias current I_0 and its output is the phase shift Φ_{ILO} as follows:

$$\Phi_{ILO} = \pi\left(\frac{C\,V_{th}}{I_{lock}}\,f_{lock} + \frac{1}{2}\right) - \frac{\pi}{2\,I_{lock}} I_0 \quad (3.20)$$

where I_{lock} is the ILO locking current.

- The counter encodes the phase shift difference (Φ_{ILO2} - Φ_{ILO1}) into a digital output N:

$$N = \frac{f_{counter}}{2\pi\,f_{lock}}\left(\Phi_{ILO2} - \Phi_{ILO1}\right) \quad (3.21)$$

where $f_{counter}$ and f_{lock} are respectively the counter clock frequency and the locking frequency.

From the two last equations, the digital output of the sensor interface is given by:

$$N = \frac{1}{4\,I_{lock}} \frac{f_{counter}}{f_{lock}}\left(I_{01} - I_{02}\right) \quad (3.22)$$

Then, the transfer function T_F of the sensor interface circuit is expressed as:

$$T_F = \frac{N}{V_S} = \frac{G_m}{2\, I_{lock}} \frac{f_{counter}}{f_{lock}} \qquad (3.23)$$

- Frequency generation: locking and counter frequencies are generated from the frequency reference f_{Ref}. This latter is generated by means of an auxiliary oscillator not considered in the behavioural model.

$$f_{lock} = \frac{f_{Ref}}{D} \qquad (3.24)$$

$$f_{counter} = M f_{Ref} \qquad (3.25)$$

3.3.2.2. Identification of model parameters

From the previous set of equations, it is possible to identify a list of parameters that will determine the sensor interface specifications. Knowing that some parameters have been previously fixed (C=10pF, V_{th}=1V, f_{lock} =35kHz and I_{lock}=400nA), five parameters must be determined:

- The TA gain G_m and its bias current I_{GM}
- The counter frequency $f_{counter}$
- The PLL multiplication factor M
- The division factor of the frequency divider D

- Value of I_{GM}

Based on equations (3.18) and (3.19), I_{GM} defines the value of I_{01} and I_{02} at zero V_S, which in turn defines the free running oscillation frequency of the ILOs at zero V_S.

The sensor interface is designed so that, at zero V_S, the phase shifts of both ILOs would be equal to π/2. Based on equation (3.12), this is obtained if, at zero V_S, the free running frequencies of ILO1 and ILO2, f_{01} and f_{02} respectively, are equal to the locking frequency f_{lock} (i.e., $f_{01(Vs=0)} = f_{02(Vs=0)} = f_{lock}$ =35kHz). $f_{01(Vs=0)}$ and $f_{02(Vs=0)}$ are defined by the bias current of ILO1 and ILO2 at zero V_S, $I_{01(Vs=0)}$ and $I_{02(Vs=0)}$ respectively ($f_{01(Vs=0)} = I_{01(Vs=0)} / 2CV_{th}$ and $f_{02(Vs=0)} = I_{02(Vs=0)} / 2CV_{th}$). Therefore:

$$I_{01(Vs=0)} = I_{02(Vs=0)} = 2\, C\, V_{th} f_{lock} \qquad (3.26)$$

Consequently, the TA bias current must be equal to $2CV_{th} f_{lock}$ which is of 700nA.

$$I_{GM} = 700nA$$

- Value of G_m

The transconductance G_m is expressed as the following (Equations (3.18) and (3.19)):

$$G_m = \frac{I_{01} - I_{02}}{2\, V_S} \qquad (3.27)$$

Then, G_m is defined according to the full scale of ($I_{01} - I_{02}$) and the full scale of the sensor output voltage $V_{S_{FS}}$. This latter is a specification of the sensor interface.

In order to determine the full scale of ($I_{01} - I_{02}$), let's take for example the case where V_S is positive. I_{01} can vary only from I_{GM} (at zero V_S) until a maximum current I_{0max} giving a 0 rad phase shift (ILO1 for positive V_S). I_{02} can vary only from I_{GM} (at zero V_S) until a minimum current I_{0min} giving a π rad phase shift (ILO2 for positive V_S). Then, it can be written:

$$I_{01_{FS}} = I_{0\max} - I_{GM} \quad (3.28)$$

$$I_{02_{FS}} = I_{GM} - I_{0min} \quad (3.29)$$

By analogy, for a negative V_S:

$$I_{01_{FS}} = I_{GM} - I_{0min} \quad (3.30)$$

$$I_{02_{FS}} = I_{0\max} - I_{GM} \quad (3.31)$$

Hence, for both positive and negative V_S,

$$|I_{01} - I_{02}|_{FS} = I_{0max} - I_{0min} \quad (3.32)$$

Using equation (3.11), these currents are expressed as:

$$I_{0min} = \frac{2\ C\ V_{th}}{T_{lock}} - I_{lock} \quad (3.33)$$

$$I_{0\max} = \frac{2\ C\ V_{th}}{T_{lock}} + I_{lock} \quad (3.34)$$

Therefore, it can be concluded that:

$$|I_{01} - I_{02}|_{FS} = I_{0max} - I_{0min} = 2\ I_{lock} \quad (3.35)$$

Consequently, the transconductance is defined as:

$$G_m = \frac{|I_{01} - I_{02}|_{FS}}{2\ \ V_{S_{FS}}} = \frac{I_{lock}}{V_{S_{FS}}} \quad (3.36)$$

where $V_{S_{FS}}$ is the full scale of the sensor equal to ±66mV according to the sensing system specifications (section 3.1). Then:

$$G_m = 6.06\mu A/V$$

- Values of $f_{counter}$, M and D

The counter frequency is chosen in order to satisfy the required resolution of 11 bits. This resolution is defined by the ratio $f_{counter}/2f_{lock}$. Hence, a counter frequency that is 4096 times the locking frequency is required. Since the locking frequency is equal to 35kHz, the counter clock frequency is:

$$f_{counter} = 143.36MHz$$

The 4096 factor between the locking and the counter frequency is obtained by means of the frequency multiplier and the frequency divider:

$$M.D = 4096 \quad (3.37)$$

A multiplication factor of 256 is chosen in order to decrease the bandwidth constraint of the PLL. Hence, the reference oscillator must run at 560kHz and the frequency divider factor must be equal to 16 (in order to generate a 35kHz locking frequency).

3.3.2.3. Simulation of the behavioural model

The behavioural model has been simulated using Cadence Virtuoso. Simulation results are presented in figure 3.10; it depicts the digital output as a function of the differential input V_S. This voltage is swept from -66mV to 66mV as defined in the circuit specifications.

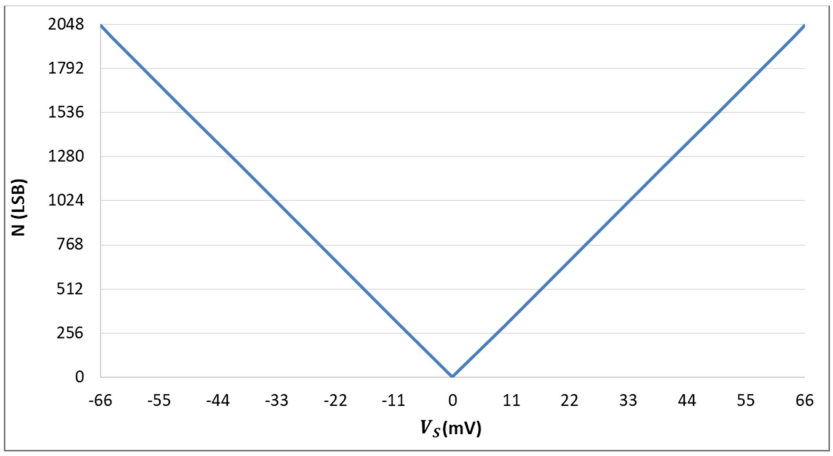


Figure 3.10: Simulation of the behavioural model (Digital output *N* as a function of V_s).

Obtained results are in good agreement with our expectations. Required specifications are obtained; a gain of 31.026LSB/mV corresponding to a resolution of 11 bit. A bit sign is used to discriminate positive and negative values of V_s.

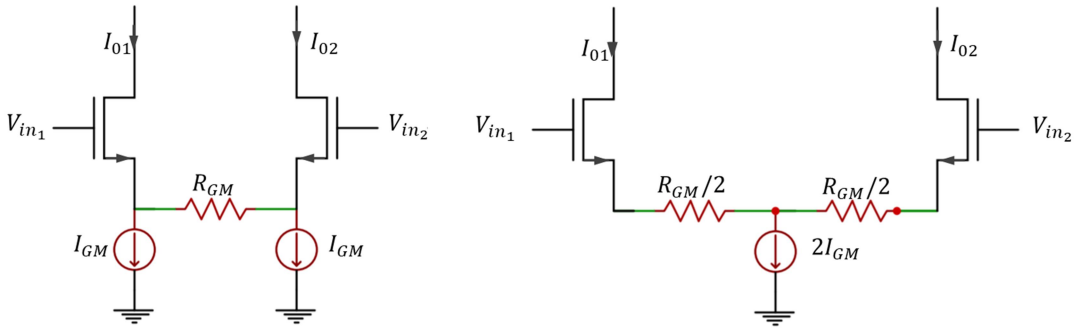
3.4. Design of the sensor interface

3.4.1. Transconductance amplifier

The Transconductance Amplifier (TA) must generate two symmetrical output currents I_{01} and I_{02}; whose difference (I_{01}- I_{02}) is proportional to the input differential voltage V_S. I_{01} is the bias current of ILO1 and I_{02} is the bias current of ILO2.

Since the TA is the first block in the sensor interface, it must be highly linear so that the sensor interface would achieve a good linearity. The straightforward implementation of a transconductance amplifier consists in using a differential pair. The so-obtained transconductance is equal to the transistor transconductances. Since, this topology of TA is highly non-linear (Sansen 2006), a degenerated TA is preferred because it has an extended linearity range (Elamien and Mahmoud 2016) (L and Yagain 2011).

Figure 3.11 depicts two well-known topologies of a degenerated TA. Both configurations are similar in terms of power consumption, transconductance and linearity rang. The first topology (Figure 3.11.a) has been selected because it has a higher input full scale (Sansen 2006).



(a) First architecture **(b) Second architecture**

Figure 3.11: Possible architectures of degenerated TA.

The transconductance of the selected TA is given by:

$$G_m = \frac{1}{R_{GM}} \qquad (3.38)$$

According to section 3.3.2.2, a transconductance of 6.06µA/V, equivalent to a resistance R_{GM} of 165kΩ, is required. A P+poly resistance is used to implement R_{GM}.

The linearity range of the degenerated TA can be extended by means of some linearization techniques. One of the most common techniques is the local feedback that is implemented using operational amplifiers (OPA) as shown in figure 3.12. The feedback is realized by connecting the inverting input of each OPA to the source of each input transistor. By doing this, V_S is applied across R_{GM} and the current flowing through R_{GM} is proportional to V_S over a large range of voltage magnitudes.

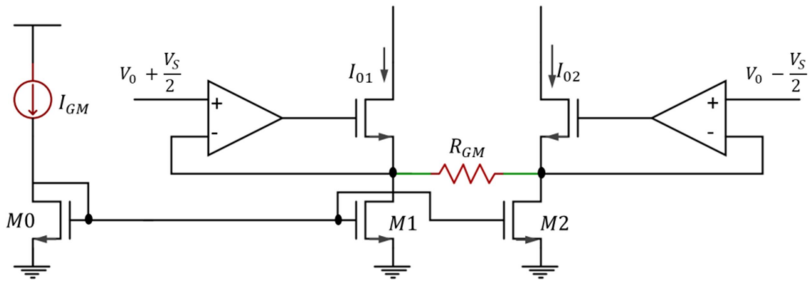


Figure 3.12: Degenerated TA with local feedback.

Special attention has to be paid to the design of currents mirrors to have identical currents flowing inside M1 and M2 (so that the TA output currents would be equal at V_S=0). Hence, transistors M1 and M2 must be well matched; in addition, small-signal output resistance of M1 and M2 must be large enough to avoid a significant change in I_{M1} and I_{M2} with V_S. These two constraints lead to large dimensions for M1 and M2. Assuming that

I_{M1}=I_{M2}=I_{GM} over the full range of V_S, we can now express the output currents of the TA as follows:

$$I_{01} = I_{GM} + V_S/R_{GM} \quad (3.39)$$

$$I_{02} = I_{GM} - V_S/R_{GM} \quad (3.40)$$

Then, the difference between output currents (I_{01}-I_{02}) is given by:

$$I_{01} - I_{02} = 2\,V_S/R_{GM} = 2\,G_m V_S \quad (3.41)$$

In addition, special attention has to be paid to the design of the OPA; a high thermally stable gain is required in order to ensure negligible input referred offset voltages over the entire operation temperature range. Each amplifier is a two stages differential PMOS operational amplifier (Miller amplifier). In order to obtain a high gain, transistors with sufficiently large sizes form the input pair and the amplifier is biased with 5µA current. This biasing current is obtained from a constant gm bias circuit (Figure 3.13) to improve the thermal stability of the gain (Majerus, Merrill, and Garverick 2013) (Wang and Chodavarapu 2015). Indeed, the thermal stability of the amplifier gain depends on the gm stability, which in turn depends on the temperature coefficient of the resistance R_b. Therefore, a rpoly resistance with a temperature coefficient equal to -0.11×10^{-3}/°C has been used to implement R_b.

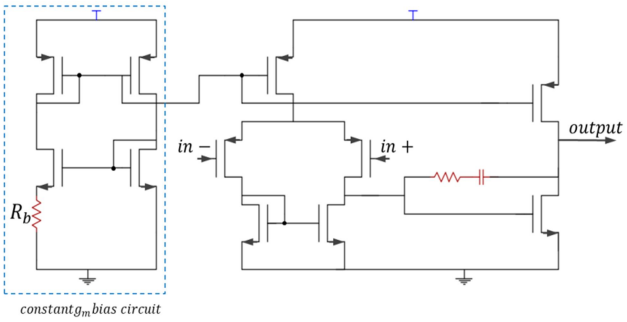
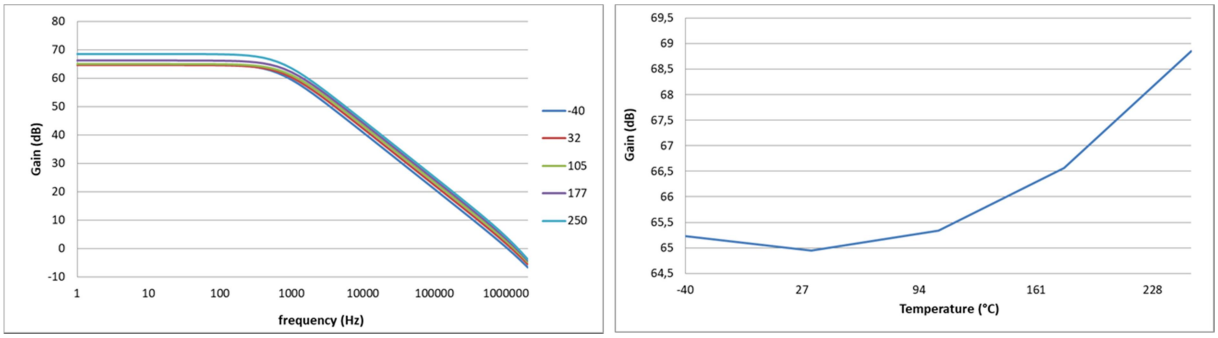


Figure 3.13: Architecture of the operational amplifier (OPA) using the constant g_m bias circuit.

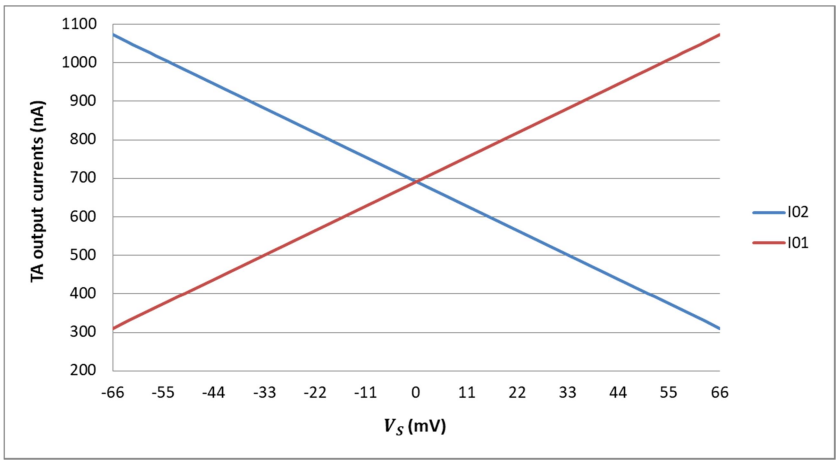
We have first simulated the OPA frequency response (Figure 3.14.a) for temperatures ranging from -40°C up to 250°C. Then, the gain is reported versus temperature (Figure 3.14.b). At 27°C, the amplifier has a gain of 65dB, a unity gain frequency of 1.2 MHz and a bandwidth of 760 Hz. The amplifier gain varies only of 3.9dB over the full range of temperature.



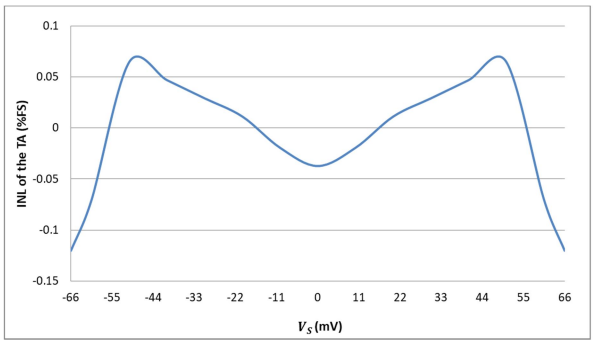
(a) Simulated open-loop frequency response **(b) The amplifier gain as a function of temperature**

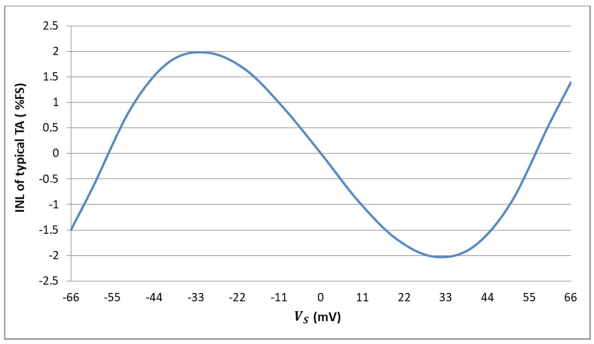
Figure 3.14: Simulation result of the open-loop gain of the OPA at different temperatures.

We have then studied the linearity of the TA. Figure 3.15.a reports TA output currents as a function of the input voltage V_S. A good linearity is confirmed by an INL of the difference between output currents (I_{01} - I_{02}) always below than 0.1% (Figure 3.15.b); while an INL of 2% is obtained for a typical TA (Figure 3.15.c).



(a)The TA output currents as a function of the input voltage.

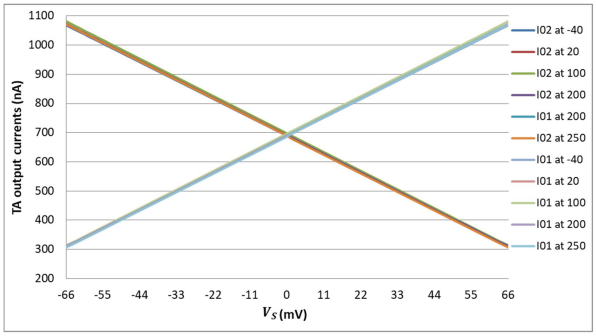




(b) INL of designed TA. **(c) INL of typical TA.**

Figure 3.15: linearity assessment of the designed TA at 27°C.
a) output currents, b) INL of the chosen TA and, c) INL of a standard TA.

The good linearity of our TA is maintained even with the variation of the temperature as illustrated on figure 3.16; an INL lower than 0.19% is obtained over the operation temperature range which extends from -40°C up to 250°C.



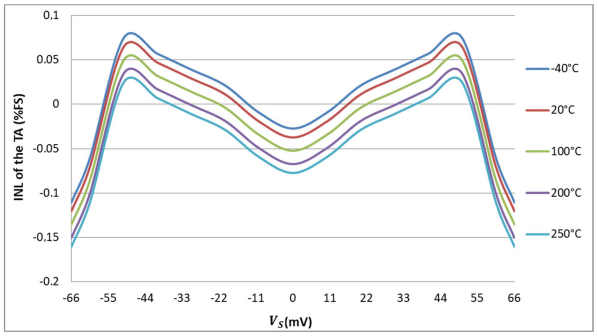


Figure 3. 16: Simulation of the chosen TA over the operation temperature range.

3.4.2. Implementation of the reference oscillator

The reference oscillator is used as an intermediate oscillator from which the locking and the counter clock signals are generated, respectively, by means of a frequency divider and a frequency multiplier. As previously mentioned, the reference frequency must be 16 times higher than the locking frequency (i.e., 560kHz).

The reference oscillator must be designed taking into consideration the following constraint; the locking frequency f_{lock} has to be equal to the free running oscillation frequency at zero V_S of both ILOs whatever temperature is ($f_{01(Vs=0)} = f_{02(Vs=0)} = f_{0(Vs=0)} = f_{lock}$). This equality is required to achieve a maximum full scale of π of the phase shift difference (Φ_{ILO2}-Φ_{ILO1}) over the full temperature range. This condition can be obtained if the locking and the free running frequencies, particularly at zero V_S, have the same thermal sensitivity.

The thermal sensitivity of the locking signal frequency depends on that of the reference oscillator frequency (because the digital divider is temperature independent). Therefore, it is required for the reference and the free running oscillators to have identical thermal variations. This can be obtained if they have both the same topology. The chosen topology for the reference oscillator (Figure 3.17) is then identical to the free running oscillator (Figure 3.2). Its frequency is then given by:

$$f_{Ref} = \frac{I_{os\ Ref}}{2\ C_{Ref}\ V_{th}} \qquad (3.42)$$

where V_{th} is the inverter switching voltage (equal to 1V), C_{Ref} is the capacitance and I_{oscRef} is the bias current.

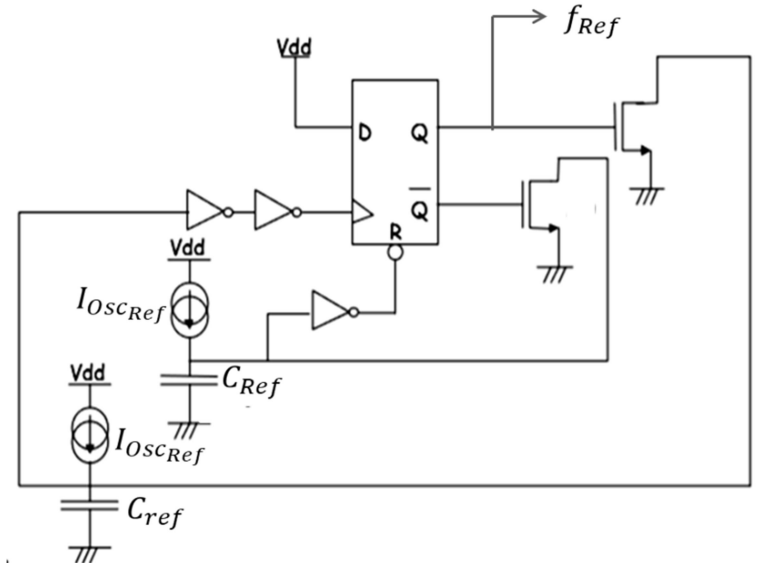


Figure 3.17: Reference oscillator.

Nevertheless, the thermal sensitivity of the reference oscillator does not depend only on its topology but also on the temperature dependence of its biasing current I_{oscRef}. Consequently, this latter must have the same thermal variation as the ILOs bias currents I_{GM}

that define f_0 at zero V_S. A simple solution is to use the same current I_{GM} for the reference oscillator and for the free running oscillators. Then:

$$f_{Ref} = \frac{I_{GM}}{2\, C_{Ref}\, V_{th}} \qquad (3.43)$$

$$f_{0(V_S=0)} = \frac{I_{GM}}{2\, C\, V_{th}} \qquad (3.44)$$

where C is the 10pF capacitance used for the RILO. Since the requested ratio between both frequencies is 16, regardless of temperature and process variations, capacitance C_{Ref} must be equal to C/16 (i.e., 0.625pF).

The reference oscillator has been simulated over a temperature range from -40°C up to 250°C (Figure 3.18). The targeted frequency (560kHz @27°C) is not reached; assuming an exact ratio of capacitances, this may be caused by an effect of the voltage slope on V_{th} or an uncertainty on the current. This will be discussed later.

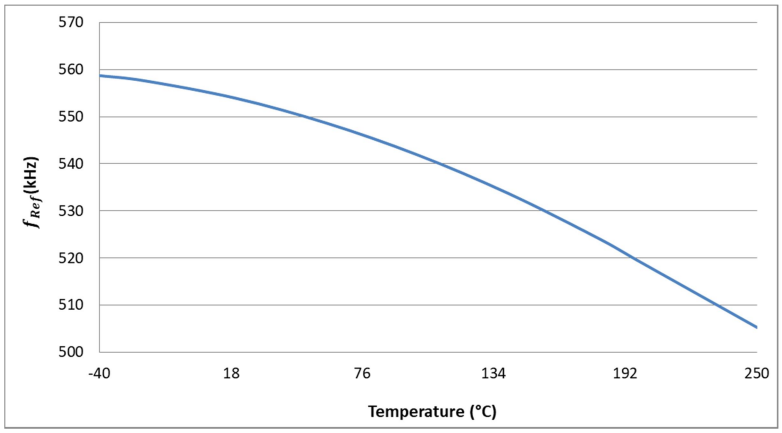
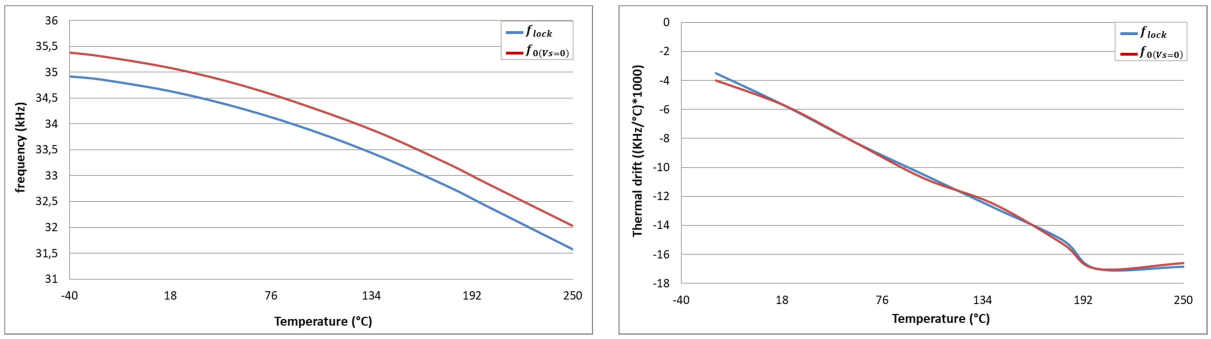


Figure 3.18: Variation of the reference frequency as a function of the temperature.

After dividing f_{Ref} using the frequency divider, we present in figure 3.19, the simulated variations of f_{lock} and f_0 at zero V_S over the full range of temperature. As expected, both frequencies have similar temperature dependence; obviously, the slight difference observed for f_{ref} is translated, after frequency division, into a mismatch of 450 Hz between f_{lock} and $f_{0(Vs=0)}$.



(a) Frequencies versus temperature **(b) Temperature coefficient**

Figure 3.19: Temperature variations of locking signal frequency and free running oscillator frequency at zero V_S.

3.4.3. Implementation of the biasing block

The role of the biasing block is to generate the locking current I_{lock}, the TA bias current I_{GM}, the bias current of the reference oscillator I_{oscRef} and the bias currents of the frequency multiplier. The biasing block is based on a bandgap voltage reference (BGVR) whose output voltage is converted into a reference current, from which the mentioned currents are generated.

3.4.3.1 Bandgap voltage reference

The bandgap voltage reference (BGVR) generates a temperature independent voltage reference; this voltage is generally equal to 1.22V. The principle of the bandgap voltage reference, described in figure 3.20, is to compensate the negative temperature dependence (CTAT: Complementary To Absolute Temperature) of a p-n junction threshold voltage with a positive temperature dependent voltage (PTAT: Proportional To Absolute Temperature). The PTAT voltage is generally the amplified difference between the base emitter voltages of two forward biased bipolar transistors. The amplification factor K is named as the adjustment factor.

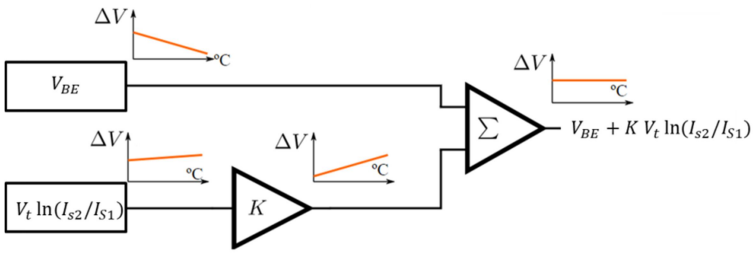


Figure 3.20: Principle of the bandgap voltage reference.

The chosen topology of the bandgap reference voltage is depicted in figure 3.21. The PTAT voltage is obtained by means of a pair of bipolar transistors (*Q1* and *Q2*), which are biased with the same current. The difference of their base-emitter voltages is expressed as:

$$\Delta V_{BE} = V_{BE} - V_{BE1} = V_t \ln\left(\frac{I_{S2}}{I_{S1}}\right) \quad (3.45)$$

where I_{S1} and I_{S2} are respectively the saturation current of *Q1* and *Q2* and V_t is the thermal voltage which is expressed as:

$$V_t = \frac{k_B\, T}{q} \quad (3.46)$$

where k_B is the Boltzmann constant, T is the temperature and q is the elementary charge.

The objective of the PTAT circuit is to obtain across R_p a voltage drop such as:

$$V_{R_P} = \Delta V_{BE} + V_{offset} \approx \Delta V_{BE} \quad (3.47)$$

where V_{offset} is the offset voltage of the amplifier A1. Then, the offset voltage of the amplifier A1 must be neglected with respect to ΔV_{BE}. To increase ΔV_{BE}, a ratio I_{S2}/I_{S1} of 100 is chosen. The obtained ΔV_{BE} at 27°C is equal to 120mV.

The current flowing inside the resistance R_P is copied into the resistance R_L thanks to the M2-M3 current mirror. Hence, the voltage across R_L is a PTAT voltage and the obtained output voltage is finally expressed as follows:

$$V_{BG} = V_{BE_L} + \frac{R_L}{R_P}\Delta V_{BE} \qquad (3.48)$$

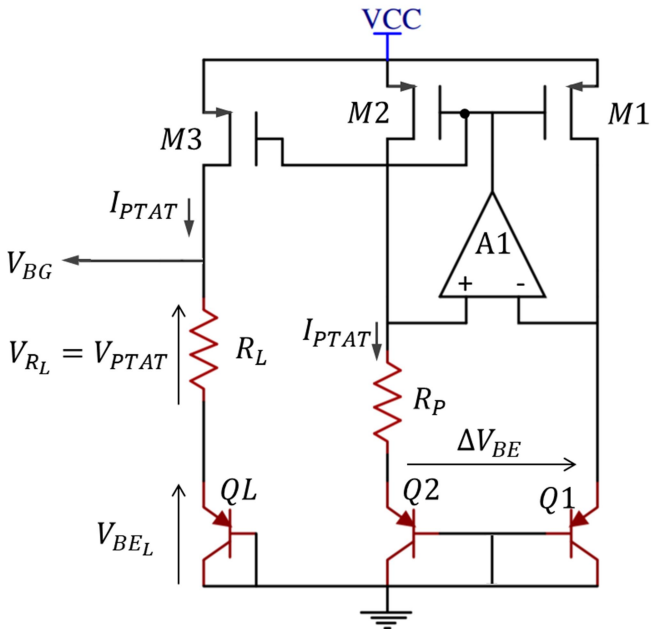


Figure 3.21: Typical architecture of a bandgap voltage reference (BGVR).

By analogy with figure 3.20, the ratio R_L/R_P is the adjustment factor K. This factor has to be correctly chosen so that the PTAT voltage V_{PTAT} would vary with the same slope as the CTAT voltage V_{BEL}. In other words, the adjustment factor is chosen so that:

$$\left|\frac{dV_{BE_L}}{dT}\right| = K\frac{d(\Delta V_{BE})}{dT} \qquad (3.49)$$

where dV_{BEL}/dT =-1.5mV/°C is the thermal derivate of V_{BEL} and $d(\Delta V_{BE})/dT$ = 0.39mV/°C is the thermal derivate of ΔV_{BE} calculated from:

$$\frac{d\Delta V_{BE}}{dT} = \frac{k_B}{q}\ln(100) \qquad (3.50)$$

Therefore, the required adjustment factor K is equal to 3.85.

A resistance R_P of 15KΩ is then chosen in order to set the current flowing in each branch of the BGVR to 8µA under ΔV_{BE}@27°C=120mV. Hence, a resistance R_L equal to 57.75kΩ is required to obtain the required value of K.

The designed BGVR has been first simulated using ideal R_L and R_P resistances (i.e., constant with temperature). In this case, the PTAT voltage is perfectly linear with respect to the temperature. Figure 3.22 shows the BGVR output voltage as a function of temperature. The BGVR exhibits a full scale of variation with temperature of about 12mV for temperature ranging from -40°C up to 250°C.

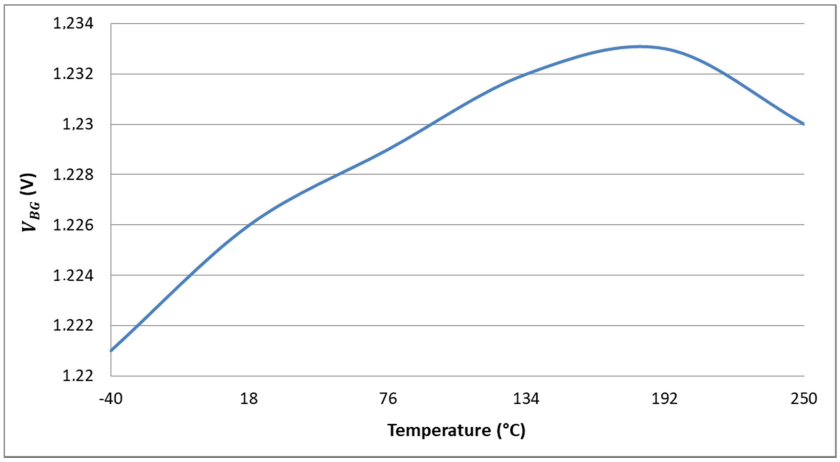


Figure 3.22: Bandgap voltage reference as a function of the temperature using ideal resistances.

We can notice that the output voltage of the BGVR has a curved thermal variation. This is caused by the non-linearity of the base-emitter voltage V_{BEL} with respect to temperature. The thermal dependence of V_{BEL} is a sum of a linear component and a non-linear one. In the BGVR of figure 3.21, the PTAT voltage is perfectly linear. Hence the non-linear component of $V_{BEL}(T)$ is still not compensated.

To overcome this limitation, designers usually propose to add a non-linear component to the PTAT voltage in order the compensate the non-linear component of V_{BEL} (Jin et al. 2016). What I propose, is to reduce the thermal non-linearity of the V_{BEL} voltage while keeping the PTAT voltage linear with respect to temperature.

The thermal non-linearity of V_{BEL} is affected by the temperature dependence of its bias current I_{bias_QL}. The temperature dependence of this current depends not only on that of ΔV_{BE} but also on that of the resistance R_P (Equation (3.51)):

$$I_{bias\_Q_L} = I_{PTAT} = \frac{V_{R_P}}{R_P} = \frac{\Delta V_{BE}}{R_P} \qquad (3.51)$$

Figure 3.23 depicts the non-linearity of V_{BEL} with respect to temperature for different temperature coefficient of R_P (t_{c_Rp} is swept from -1.5m/°C and +1.5m/°C). It shows that V_{BEL} exhibits the lowest thermal non-linearity for a temperature coefficient t_{c_Rp} of -1.5m/°C, which is the minimum temperature coefficient available in the design technology. Hence, the resistance R_P is implemented using a rnp resistance (t_{c_rnp} = -1.5m/°C).

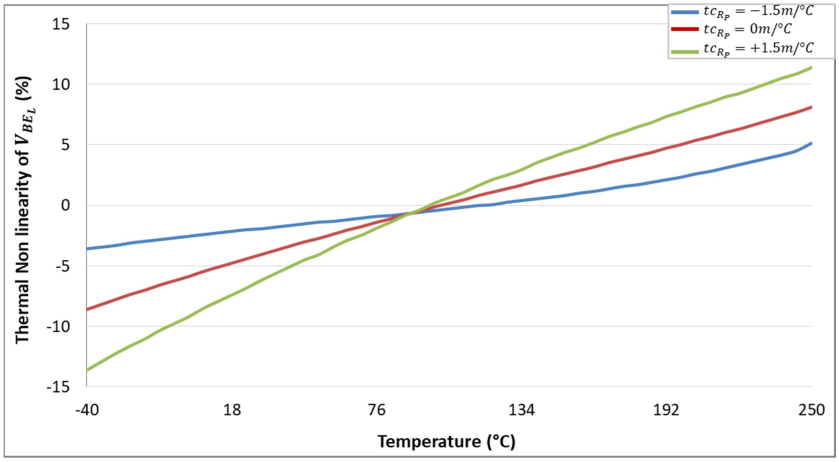


Figure 3.23: Thermal non-linearity of V_{BEL} for different temperature coefficients of R_p.

The same type of resistance is chosen for the resistance R_L (i.e., a rnp resistance), and this is in order to keep the PTAT voltage, $V_{RL}=(R_L/R_P).(k_BT/q).ln(I_{S2}/I_{S1})$, linear with respect the temperature as explained before.

Finally, V_{BEL} and V_{PTAT} voltages exhibit close and opposite thermal variations over the entire operation temperature range as shown in figure 3.24.

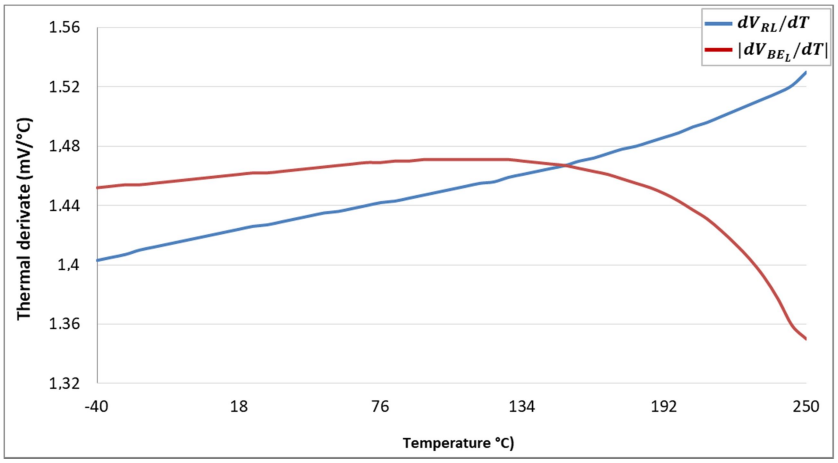


Figure 3.24: temperature sensitivity of V_{BEL} and V_{RL}.

In the end, the BGVR achieves a thermal variation of 5.72mV over the full temperature range from -40°C up to 250°C (Figure 3.25).

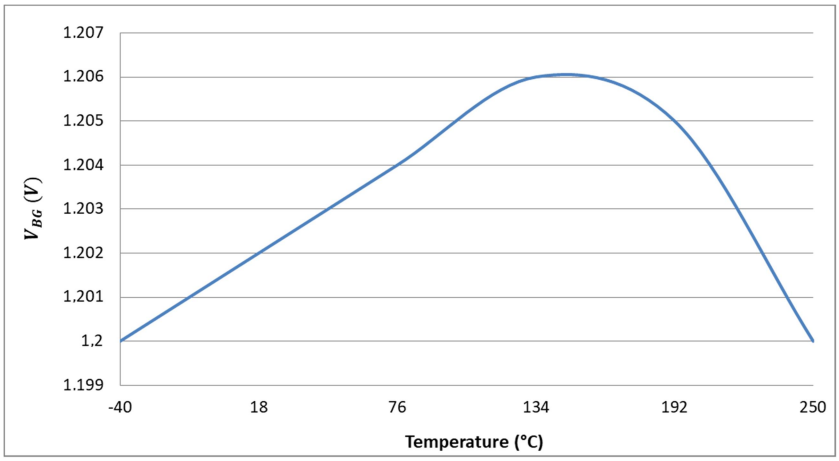
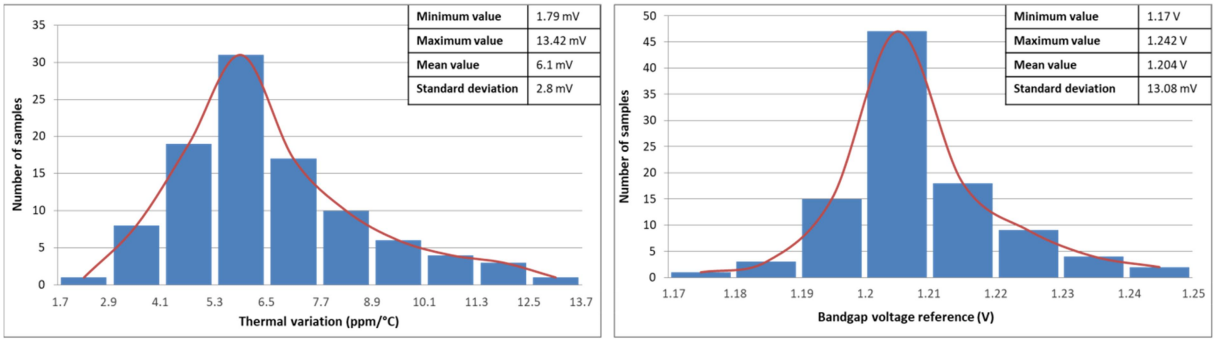


Figure 3. 25: Bandgap voltage reference as a function of the temperature.

We have then studied the robustness of the proposed BGVR with process variations. A hundred of Monte Carlo simulations have been performed and we report (Figure 3.26) the value of V_{BG} (@27°C, right side) and the full scale of voltage variation ΔV_{BG} (left side). Typical values (respectively 1.2V and 5.72mV) and immunity against process variations are demonstrated.



(a) Thermal variation of the BGVR **(b) BGVR output voltage at 27°C**

Figure 3.26: Monte Carlo simulation of the bandgap voltage reference (100 runs).

3.4.3.2 Biasing block

Figure 3.27 shows the architecture of the biasing block, which is based on the designed BGVR. The biasing block provides a reference current I_{ref} of 700nA from which all biasing currents are generated (I_{oscRef}, I_{GM}, I_{lock} and the PLL input currents).

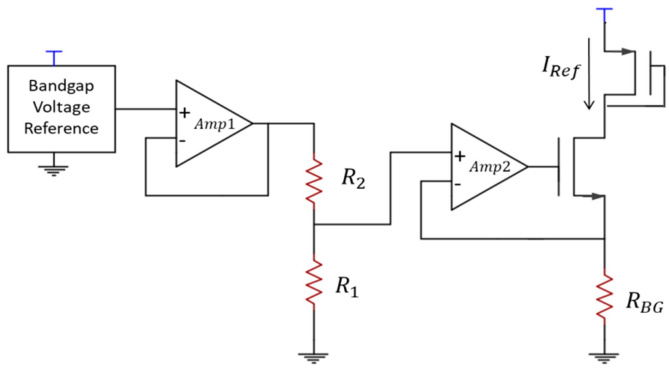


Figure 3.27: Architecture of the biasing block core.

First, the bandgap voltage is attenuated by means of a voltage divider. Then, it is converted into a current using a resistance R_{BG}. This architecture has been chosen to reduce the value of R_{BG} and thus its surface. This surface optimisation is not detailed here. The reference current I_{Ref} is expressed as follows:

$$I_{Ref} = \frac{R_1}{R_1 + R_2}\frac{V_{BG}}{R_{BG}} \quad (3.52)$$

It was decided to divide the bandgap voltage by four; a resistance R_1 of 16.6 kΩ and a resistance R_2 of 50kΩ are then used to respect maximum output current of the follower amplifier *Amp1*. Hence, a resistance R_{BG} of only 430kΩ is required to obtain the required 700nA reference current in the diode-like MOS transistor.

From the reference current I_{Ref} (Figure 3.28), the TA bias current I_{GM} and the reference oscillator bias current I_{oscRef} are generated by means of current mirrors having a unit copy factor (M0/M1 and M0/M2) while the locking current I_{lock} is generated by means of a current mirror having a copy factor of 0.57 (M0/M3). $I_{GM,}$ I_{oscRef} and I_{lock} are expressed as:

$$I_{GM} = I_{OscRef} = I_{Ref} = \frac{1}{4}\frac{V_{BG}}{R_{BG}} \quad (3.53)$$

$$I_{lock} = 0.57\, I_{Ref} = \frac{0.57}{4}\frac{V_{BG}}{R_{BG}} \quad (3.54)$$

The main constraint of the biasing block is that the bias current of the TA I_{GM} and the bias current of the reference oscillator I_{oscRef} must be well matched at all temperatures. In fact, this equality is required so that the free running frequency of the ILOs at zero V_S would be always equal to the locking frequency as explained in section 3.4.2. Consequently, large dimensions must be used for M0, M1, M2 and M3.

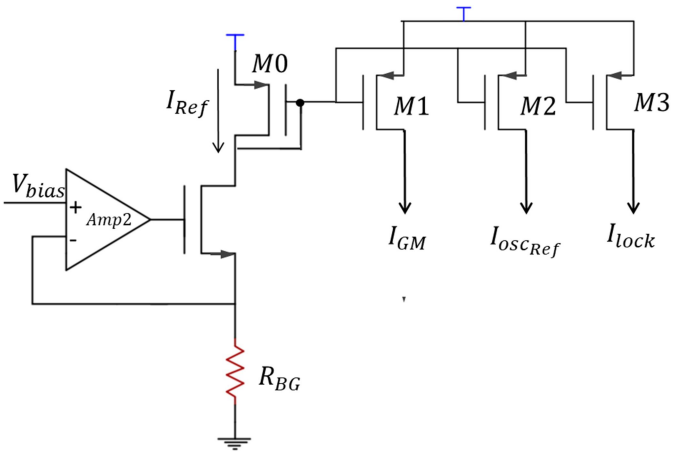


Figure 3.28: Generation of I_{GM}, I_{oscRef} and I_{lock}.

3.4.3.3 Simulation of the biasing block

The obtained reference current is equal to 693nA at 27°C in typical simulation; which is very close to the specification. The difference between this obtained value and the targeted

value (i.e., 700nA) explains the difference between the obtained reference frequency and the targeted value (Figure 3.18).

I_{GM} and I_{oscRef} are required to be identical over the operation temperature range. This is in order to have the same value for the bias current of the reference oscillator (I_{oscRef}) and the ILOs bias current at zero V_S ($I_{0(Vs=0)}$) ($I_{0(Vs=0)}$ is indeed a copy of I_{GM} by means of unit factor current mirrors). Figure 3.29 reports the effect of the temperature variation on these currents. It shows that I_{oscRef} and $I_{0(Vs=0)}$ have almost the same thermal variation.

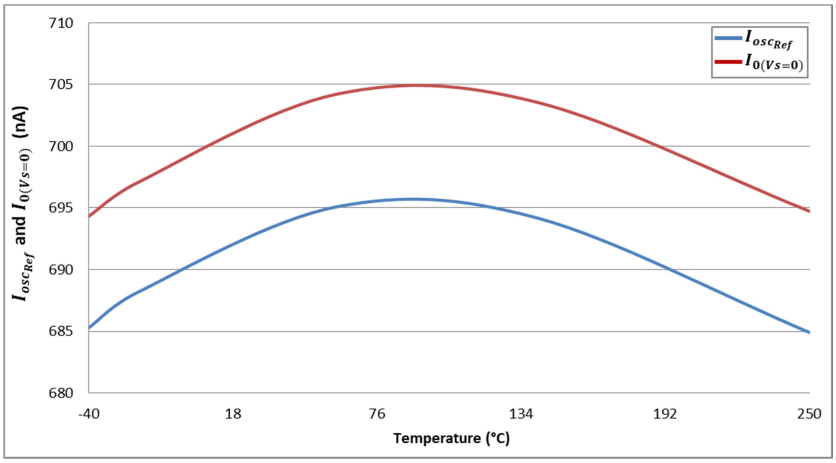
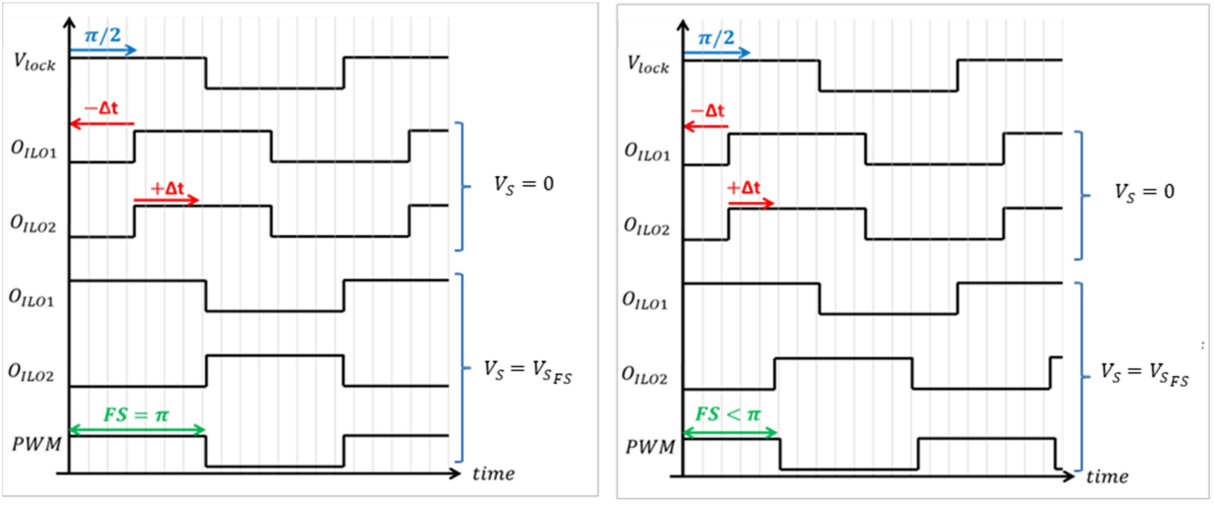


Figure 3. 29: I_{GM} and I_{oscRef} as a function of the temperature.

A slight difference is observed between these currents due to uncertainty on the copying factors of the current mirrors. This difference is at the origin of the difference between f_{lock} and $f_{0(Vs\,=\,0)}$. According to equation (3.12), this difference makes the phase shifts of both ILOs at zero V_S $\Phi_{ILO(Vs=0)}$ different from π/2. This affects the full scale of the sensor interface as illustrated in figure 3.30.



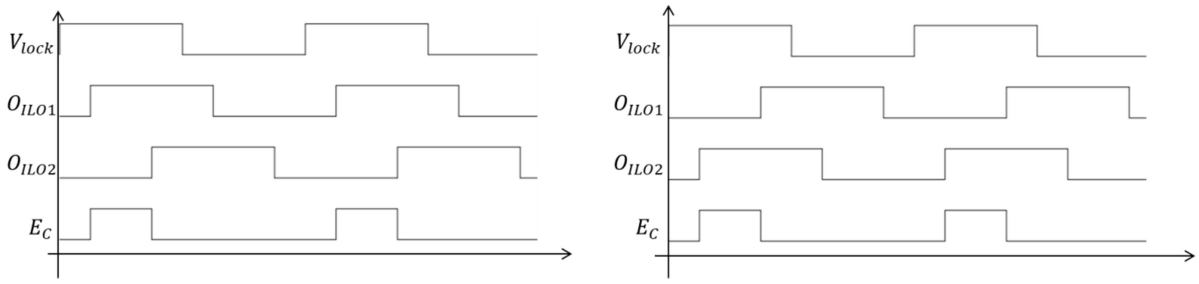
$\Phi_{ILO(Vs=0)} = \pi/2$ $\Phi_{ILO(Vs=0)} \neq \pi/2$

Figure 3. 30: Explanation of the effect of $\Phi_{ILO(Vs=0)}$ on the full scale of the sensor interface.

3.4.4. Implementation of the counter

The counter is used in order to convert the phase shift difference (Φ_{ILO2} - Φ_{ILO1}) into a digital output word N of 11 bits plus a bit of sign. Hence, the counting is enabled when V_{lock} is up and only one of the ILO outputs is up (Figure 3.31). The enable signal is written as:

$$E_C = V_{lock}.[ILO1.not(ILO2) + ILO2.not(ILO1)] \quad (3.55)$$



(a) V_S>0 **(b) V_S<0**

Figure 3.31: Chronograms of the counting enable signal E_c.

When counting is enabled (i.e., E_c is up), the counter output is incremented at each clock period until the counting reaches its end (i.e., E_c falls down). Then, the counting result is saved in a register at the falling edge of the locking signal, and the output of the counter is reset and the counter is ready to count again at the next rising edge of the enable signal.

The counter is able to detect which ILO output is in phase advance. This gives the sign of the sensor output voltage V_S (which is the input voltage of the sensor interface). Indeed, when the output of ILO1 is in phase advance, this means that V_S is positive (Figure 3.31). An additional lead/lag bit (i.e., the lead/lag between the two ILOs outputs) is used to give the sign of V_S.

Hence, a 12 bit digital word is obtained at the output of the counter; 11 bit for the digital output N and 1 bit for the lead/lag bit. The main sub-blocks of the counter are:

- a 11 bits counter made of 11 half adders in series,
- a detector of rising and falling edges to appear on the locking signal,
- a sign detector for the sensor output voltage (lead/lag bit).

Figure 3.32 depicts the sub-block used to detect the falling edge of the locking signal. It uses a synchronous DFF flip-flop (D1), which is activated on falling edge of the locking signal. The second flip flop D2 is a simple digital buffer which delivers the information about the occurrence of the falling edge signal synchronously with the counter clock. The same principle is used to detect the rising edge of V_{lock}.

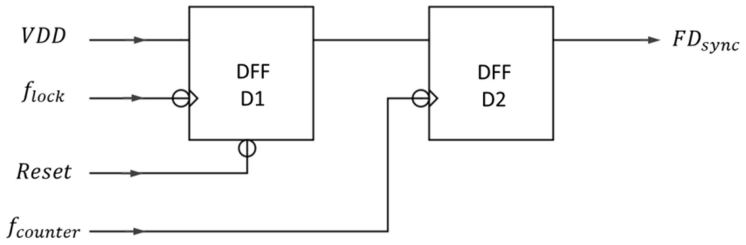


Figure 3.32: Detector circuit of the falling edge of V_{lock}.

Figure 3.33 depicts the sub-block used to detect the sign of V_s. A simple DFF controlled by the falling edge of E_c is used. From Figure 3.31, it is obvious that when V_S is positive, the output of ILO1 is up on the falling edge of E_c and then, a high logic level is obtained at the output of the DFF (i.e., the lead/lag bit A_v='1'). The delay cell is used for delaying the signal O_{ILO1} in order to respect the DFF timing constraint.

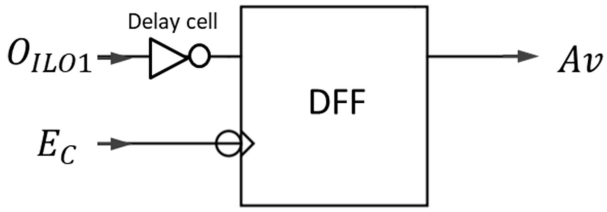


Figure 3.33: Generator of the lead/lag bit.

3.4.5. Implementation of the phase locked loop

A Phase Locked Loop (PLL) is used to multiply the reference frequency f_{Ref} by a factor of 256. This block provides the counter clock signal $f_{counter}$.

A PLL consists of five basic elements (Figure 3.34): a phase detector, a charge pump, a loop filter, a voltage controlled oscillator and a frequency divider (f_{in} stands for f_{Ref} and f_{out} stands for $f_{counter}$).

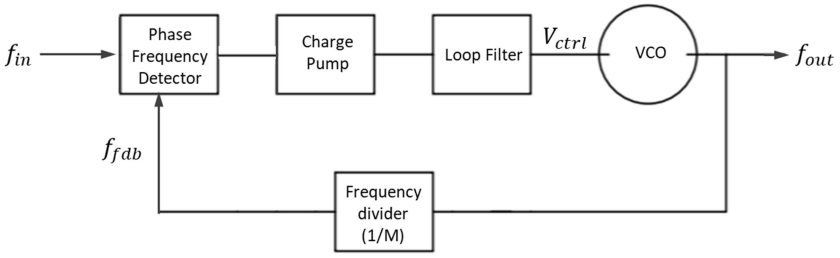


Figure 3.34: Schematic diagram of the PLL.

When the PLL is locked, the instantaneous phase difference between the input and the feedback signals (f_{in} and f_{fdb} respectively) is constant. Then, since the frequency is the derivate of the phase, the input and the feedback signals have the same oscillation frequency (f_{in}=f_{fdb}). Since the feedback frequency f_{fdb} is 1/M the output frequency f_{out}, where M is the division factor of the frequency divider, we obtain:

$$f_{out} = M\, f_{in} \quad (3.56)$$

Hence, the division factor M is 256.

The PLL works as follows: the phase frequency detector (PFD) compares the feedback signal to the input signal. It generates a digital output signal that charges or discharges the capacitor of the loop filter (LPF). Then, the LPF output voltage, which controls the frequency of the VCO, increases and decreases (according to the sign of the frequency difference between the input and the feedback signals) until it reaches the value that makes the VCO oscillate at the targeted output frequency (i.e., $f_{out} = M\, f_{in}$). The PLL is then locked.

The PLL is required to perform the same multiplication factor over the entire operation temperature range and for all process corners. Thanks to its closed loop architecture, as long as the PLL is locked, the output frequency is always equal to the input frequency multiplied by 256. In order to make sure that the PLL is always locked, it is just required to make sure that the VCO can generate a signal whose frequency is 256 times the input frequency for a control voltage V_{ctrl} between 0.3V and V_{dd}-0.3V. This is due to the operation condition of the charge pump. More details are presented next.

3.4.5.1. Phase frequency detector (PFD)

The PFD is the core element in a PLL, it detects not only the phase difference between the feedback and the input signals, but also their frequency difference. One key advantage of using a PFD compared to a simple phase detector is that the PFD compares not only the phase difference but also the frequency difference. A phase frequency detector avoids a false lock in the PLL, in which the PLL may be locked with a wrong input frequency or with a wrong input signal phase (e.g., the PLL may lock on a harmonic of the input signal).

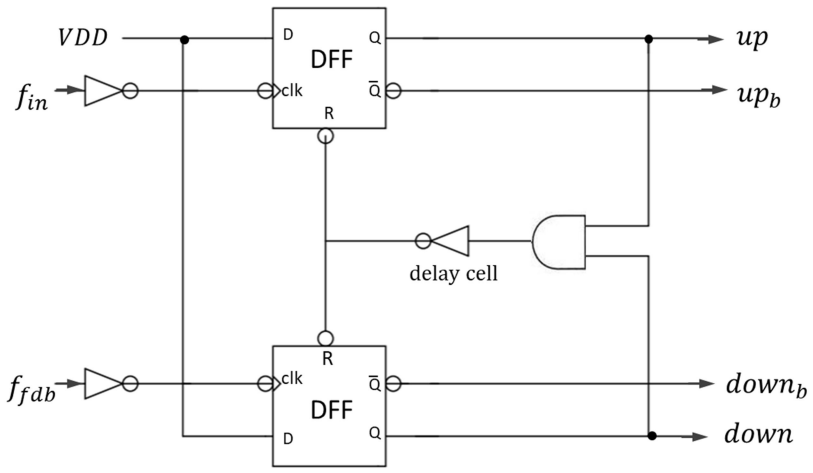


Figure 3.35: Phase frequency detector circuit.

The PFD shown in figure 3.35 is based on D flip-flops. The delay cell, presented by the inverter, is used to avoid the dead zone induced by the reset of the two flip-flops. The PFD generates two digital signals ("up" and "down"). These signals (Figure 3.36) are then converted into analog signals by the charge pump to control the VCO through the loop filter.

To illustrate the frequency detection, let's consider that the f_{fdb} signal is twice the input frequency. In this case, the PFD generates a pulse on the up signal whose pulse width is equal to the phase difference. The short pulses appeared in the down signal is indeed parasitic picks, called "a spur", and this is due to the delay in the reset path of the PFD.

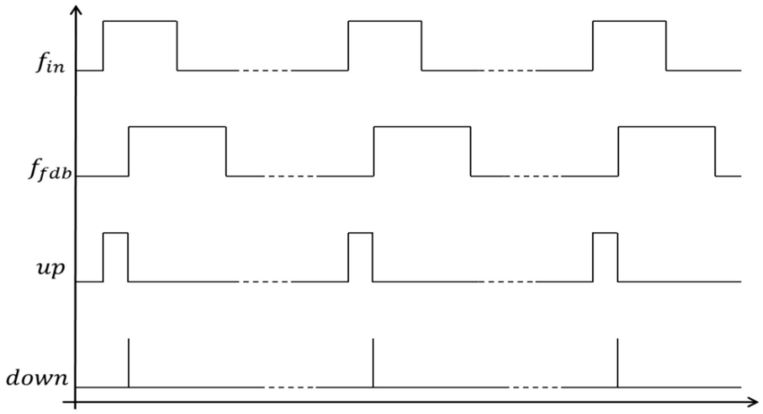


Figure 3.36: PFD chronograms when f_{in} is in phase advance with respect to f_{fdb}.

3.4.5.2. Charge pump (CP)

The charge pump converts the PFD output signals into an analog signal that drives the VCO through the loop filter. A double state CP with current steering switchers is used (Figure 3.37). This structure has the advantage of a speed switching (Kalenteridis, Papathanasiou, and Siskos 2008). The charge pump current I_{CP} is either pulled up or push down according to the PFD output signals which in turn depend on the sign of the frequency and phase difference between the input and feedback signals.

The two transistors M_{up} and M_{down} must be well matched so that the CP output current I_{out} would have the same value whatever if the current is flowing from Vdd (through M_{up}) or to the ground (through M_{down}). Therefore, large dimensions are required for M_{up} and M_{down}. Moreover, large W/L ratios, for M_{down} and M_{up}, are required for faster switching (George Tom VARGHESE 2009).

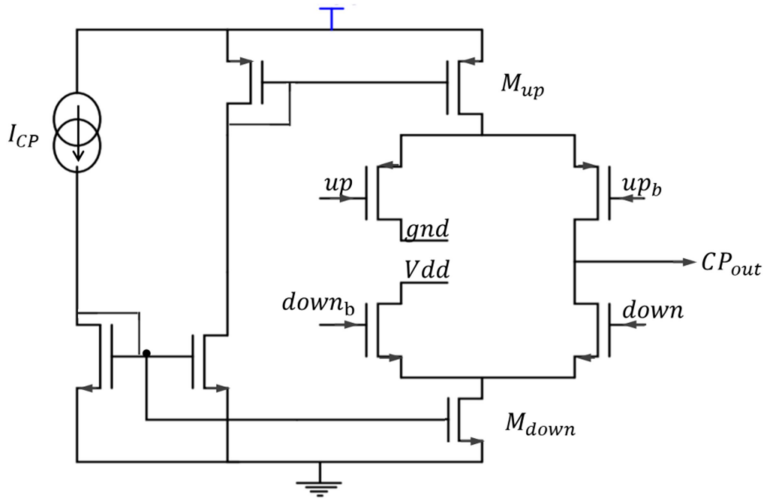


Figure 3.37: Charge pump circuit with current steering switchers.

3.4.5.3. Loop filter (LPF)

The loop filter is a critical block in the PLL because it sets its bandwidth and ensures its stability. The filter integrates the current generated by the CP by means of a capacitor C_f in series with a resistance R_f. However, for each change in polarity of the charge current, a jump occurs across the RC circuit (George Tom VARGHESE 2009). Therefore, to filter these jumps, a second capacitor C_2 is added in parallel with R_f and C_f as shown in figure 3.38. The so obtained output voltage V_{ctrl} is used to control the VCO.

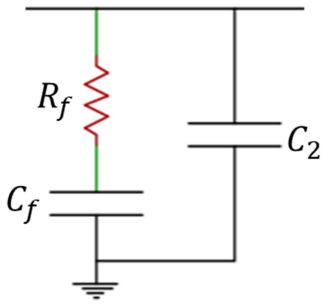


Figure 3.38: Loop filter circuit.

3.4.5.4. Voltage controlled oscillator (VCO)

The schematic of the VCO is presented in figure 3.39. It is composed of a 5 stages current starved ring oscillator, a buffer and a level shifter.

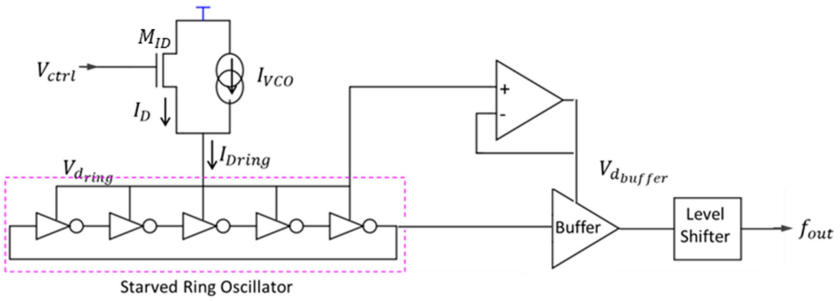


Figure 3.39: Topology of the voltage controlled oscillator.

The output frequency (Equation (3.57)) is given by the ring oscillator, which represents the core of the VCO.

$$f_{out} = \frac{1}{5\,t_D} \qquad (3.57)$$

where t_D is the delay of one stage of the ring oscillator. This delay is set by the ring oscillator bias current I_{Dring}. This current is the sum of a fixed bias current I_{VCO} and a voltage controlled current I_D:

$$I_{D_{ring}} = I_D + I_{VCO} \qquad (3.58)$$

The current I_D is generated by means of a transistor M_{ID} whose gate is connected to V_{ctrl} (V_{ctrl} is the LPF output voltage); then I_D a function of V_{ctrl} as expresses the following equation:

$$I_D = \frac{1}{2}\mu_P C_{ox}\frac{W_{M_{ID}}}{L_{M_{ID}}}(V_{ctrl} - V_{dd} - V_{th})^2 \qquad (3.59)$$

Hence, the so-obtained VCO output frequency is a function of V_{ctrl}. However, the so-obtained frequency is a linear function of V_{ctrl} only over a small range. This is due to the non-linearity of I_D with respect to V_{ctrl} (Equation (3.59)).

Dimensions of M_{ID} and of inverters must be carefully chosen so that M_{ID} would remain saturated. Besides, we must ensure that the value of the control voltage V_{ctrl} that makes the VCO run at the targeted frequency is ranging between 0.3V and 1.5V (knowing that Vdd=1.8V). This voltage range arises from the saturation condition of the transistors M_{up} and M_{donw} of the charge pump (Figure 3.37).

The current I_{VCO}, which is added to I_D, is chosen in order to obtain a VCO frequency of 143MHz (the targeted output frequency of the PLL which is indeed the counter frequency) for an input voltage V_{ctrl} around 900mV.

The adopted buffer consists of 3 inverters whose supply voltage ($V_{dbuffer}$) is the same as that of the inverters of the 5 stages ring oscillator. This choice has been made to ensure the same dynamic range for the buffer and for the ring oscillator. As a consequence the output signal of the buffer has a limited dynamic range (0-$V_{dbuffer}$). Hence, a level shifter is added after the buffer so that the VCO output square signal would have the full dynamic range.

Figure 3.40 shows that the VCO characteristic function is quasi-linear over a control voltage range extended from 0.3V to 1.1V. Frequencies from 110MHz up to 440MHz may be obtained with a gain of about 400MHz/V.

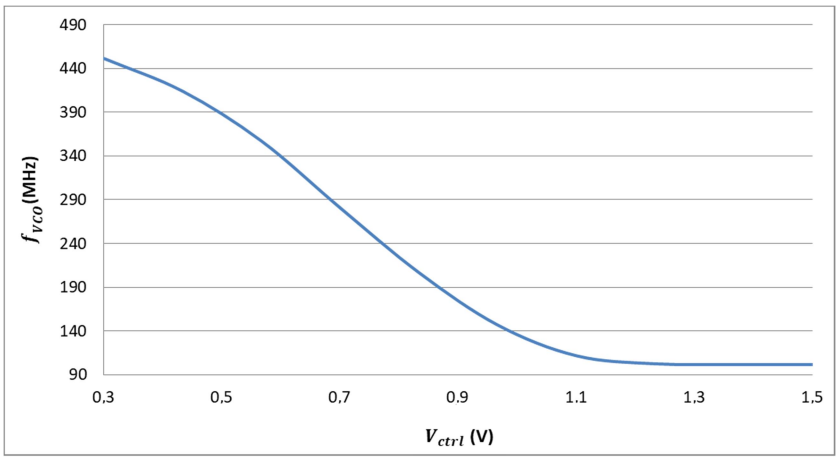


Figure 3.40: Characteristic function of the VCO at 27°C.

As mentioned before, the VCO must be able to generate a frequency 256 times the reference frequency for all temperatures. Knowing that the reference frequency (i.e., f_{in}) varies

with temperature from 559kHz to 505kHz (Figure 3.18), and that the VCO itself is affected by temperature variations, the VCO must be able to generate frequencies between 143.1MHz and 129.3MHz for an input voltage V_{ctrl} ranging between 0.3V and 1.5V. The characteristic function of the VCO at different temperatures (Figure 3.41) shows that the VCO achieves this requirement.

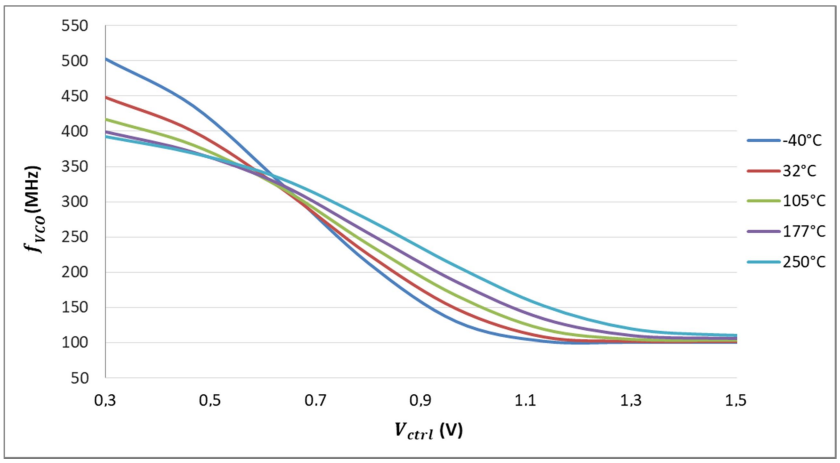


Figure 3.41: VCO characteristic function for different temperatures.

3.4.5.5. Phase locked loop (PLL)

The design of the PLL consists in choosing its parameters (I_{CP}, R_f, C_f and C_2) in order to guarantee its stability. This is ensured if the phase margin of the PLL is positive. The values of R_f, C_f and C_2 have been chosen in order to obtain a phase margin of around 45°C (Equation (3.60)).

$$M\varphi = \arctan(R_f C_f w_c) - \arctan\left(\frac{R_f C_f w_c}{1 + \frac{C_f}{C_2}}\right) \quad (3.60)$$

where $w_c = 2\pi f_{in}/10$ and $C_f w_c = \frac{\sqrt{\frac{C_f}{C_2}}\, I_{CP}\, K_{VCO}}{2\pi\, N\, f_c}$; N=256.

A PLL behavioural model, illustrated in figure 3.42, has been developed using Verilog AMS. It is used to extract the phase margin from the PLL different parameters and to validate the chosen parameters.

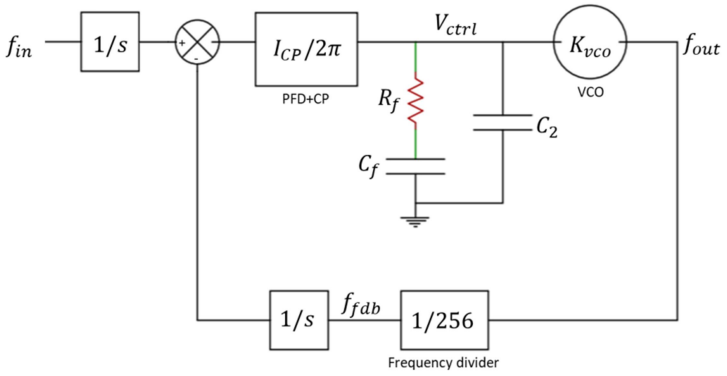


Figure 3.42: Behavioural model of the PLL (KVCO is the VCO gain).

Finally, the PLL parameters are as follows: I_{CP} =1µA, C_f =18pF, R_f =500kΩ and C_2=2pF. Simulation of the PLL behavioural model shows that these values lead to a phase margin of 55° which satisfies the stability condition of the PLL.

However, the PLL stability has to be maintained over temperature and process variations. In order to verify this stability, a worst-case simulation of the PLL behavioural model is performed. Equation (3.60) shows that the phase margin is a function of K_{VCO}, I_{CP} and R_f. After testing several combinations using the minimum and maximum values of these parameters, it was found that the minimum phase margin is obtained for the minimum values of K_{VCO}, I_{CP} and R_f over temperature and process variations. The so-obtained lowest phase margin is equal to 31.7° which satisfies the stability condition of the PLL.

Finally, the timing diagram of the PLL is presented in figure 3.43. It shows that the PLL is well locked since the control voltage converges to a constant voltage value around 900mV.

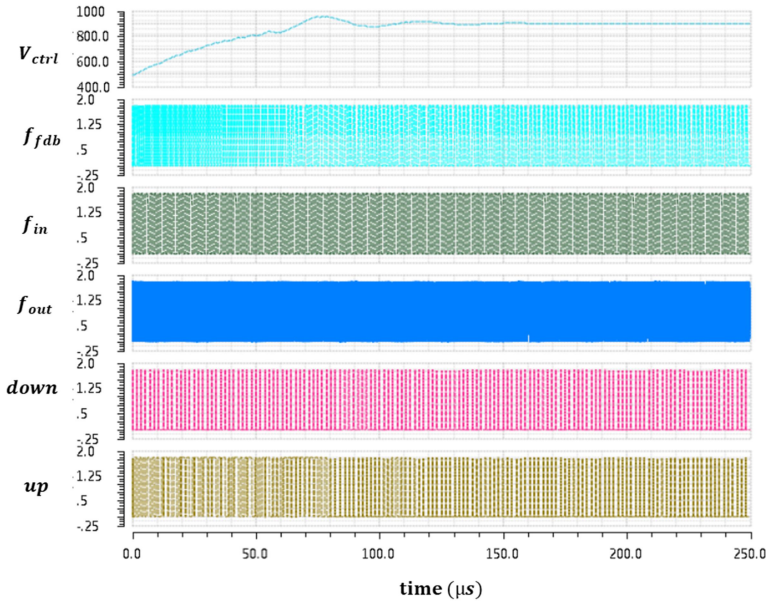


Figure 3.43: Timing diagram of the PLL.

3.4.6. Frequency divider

The frequency divider generates the locking frequency from the reference oscillator; it must realise a division factor of 16. This is done using four D-type flip-flops connected in series, as describes figure 3.44, where each flip-flop performs a frequency division factor of two.

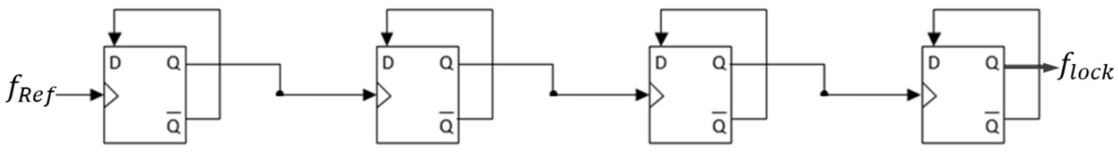


Figure 3.44: Frequency divider circuit.

Since this technique is purely digital, this division factor is not sensitive to temperature and process variations.

3.4.7. High temperature design considerations

The sensor interface circuit converts the sensor output voltage into a phase shift difference. This latter is digitized using a high frequency counter. As previously demonstrated, the proposed sensor interface is robust against temperature variations. However, some high temperature design refinements need to be considered.

3.4.7.1. Reduction of TA and ILO mismatches

The phase shift difference between the two ILOs outputs, which defines the output of the sensor interface, is expressed as:

$$\Phi_{ILO2} - \Phi_{ILO1} = \frac{\pi}{2\, I_{lock}} (I_{01} - I_{02}) = \frac{\pi}{I_{lock} R_{GM}}\ V_S \qquad (3.61)$$

The locking current I_{lock} is generated from the reference current using a simple current mirror as described in section 3.4.3.2. Since the transistors of the current mirror are designed with sufficiently large dimensions, the copying factor of the current mirror α_{CM2} can be considered temperature independent (α_{CM2} = 0.57).

Then, based on equation (3.54), I_{lock} is given by:

$$I_{lock} = \beta \frac{V_{BG}}{R_{BG}} \qquad (3.62)$$

where β is a temperature independent factor (β = α_{CM2}/4). Using equation (3.62), equation (3.61) can be written as:

$$\Phi_{ILO2} - \Phi_{ILO1} = \frac{\pi}{\beta} \frac{R_{BG}}{R_{GM}\, V_{BG}}\ V_S \qquad (3.63)$$

Then, the thermal stability of the phase shift difference Φ_{ILO2} - Φ_{ILO1} is influenced by the non-zero temperature coefficient of the resistances R_{GM} and R_{BG}. If both R_{GM} and R_{BG} have the same temperature coefficient (i.e., same type of resistances), their ratio will be temperature independent. Consequently, the thermal stability of the phase shift difference, and therefore the thermal stability of sensor interface output N, after posing $R_{bias} = \frac{R_{BG}}{\beta}$, depends only on that of the bandgap voltage:

$$N = \frac{1}{2} \frac{R_{Bias}}{R_{GM}} \frac{f_{counter}}{f_{lock}} \frac{V_S}{V_{BG}} \qquad (3.64)$$

3.4.7.2. Wheatstone bridge biasing

To further improve the thermal stability of the sensor interface output *N*, the Wheatstone bridge is biased by the bandgap voltage (Figure 3.45). This eliminates the contribution of the bandgap voltage to the thermal sensitivity of the sensor interface output.

Indeed, by biasing the Wheatstone bridge by the bandgap voltage, the sensor output voltage V_S is expressed as:

$$V_S = \frac{-\Delta R_{sensor}}{2R_0 + \Delta R_{sensor}} V_{BG} \quad (3.65)$$

where

$$\Delta R_{sensor} = R_{sensor} - R_0 \quad (3.66)$$

Notice here that the sensor output voltage is inversely proportional to ΔR_{sensor}. This latter is inversely proportional to the value of the measured magnetic field "B" ("NVE AA and AB-Series Analog Sensors" n.d.). This finally makes the sensor output voltage proportional to "B" and hence proportional to the measured current.

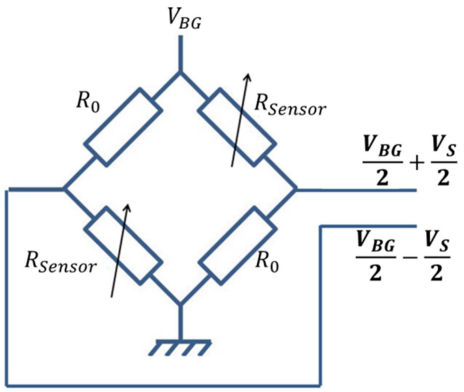


Figure 3.45: Wheatstone bridge sensor.

Consequently, using equations (3.64) and (3.65), the sensor interface output is given by:

$$N = \frac{1}{2}\frac{R_{Bias}}{R_{GM}}\frac{f_{counter}}{f_{lock}}\frac{-\Delta R_{sensor}}{2R_0 + \Delta R_{sensor}} \quad (3.67)$$

As a conclusion, using these two design refinements, the digital output is highly temperature independent. As a matter of fact, since $f_{counter}$ and f_{lock} are both generated from the same reference oscillator using respectively a PLL and a frequency divider (which are insensitive to temperature variation), the ratio $f_{counter}/f_{lock}$ is temperature independent. Furthermore, resistors embedded in the Wheatstone bridge have all the same temperature coefficient because they are of the same nature. Hence, the ratio of resistances $\Delta R_{sensor}/(2R_0 + \Delta R_{sensor})$ is insensitive to temperature variations. What is more, the use of the same resistance nature for R_{BG} and R_{GM} makes their ratio R_{BG}/R_{GM} temperature independent. Therefore, the digital output of the sensor interface achieves a low thermal dependence.

3.5. Simulation results

The sensor interface is designed using a PD-SOI technology, which is chosen for its high robustness against temperature variations. The sensor interface is simulated for an input voltage with a full scale of ±66mV. This voltage is temperature independent and it emulates the sensor differential output voltage V_S.

3.5.1. Characteristic function: thermal stability and linearity

The simulated digital output N of the sensor interface at 27°C as a function of the sensor output voltage V_S shows that the input full scale of the sensor interface is equal to ±63mV (Figure 3.46). In addition, this simulation shows a gain of 29.4LSB/mV at 27°C and since the sensor interface achieves an output full scale of 1855LSB, 11 bits of resolution is obtained.

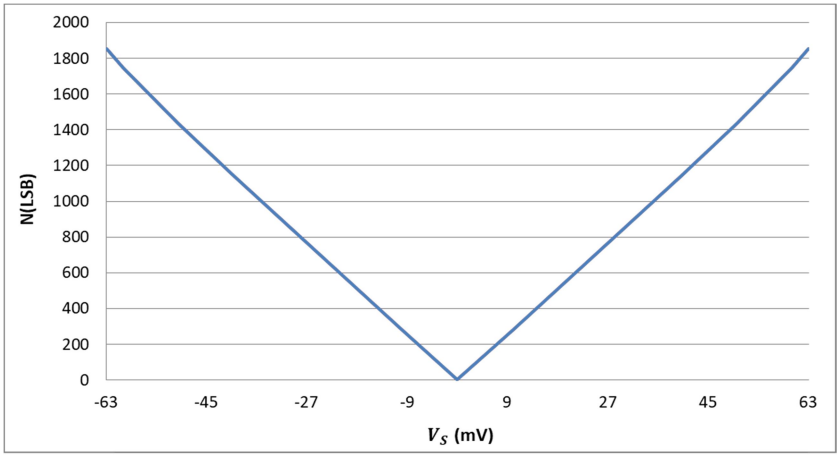


Figure 3.46: Simulated characteristic function of the sensor interface at 27°C.

Considering a temperature range from -40°C up to 250°C, the simulated input full scale is finally limited to only ±60mV as shown in figure 3.47. The sensor interface achieves a gain of about 30LSB/mV with 11 bits of resolution whatever temperature is.

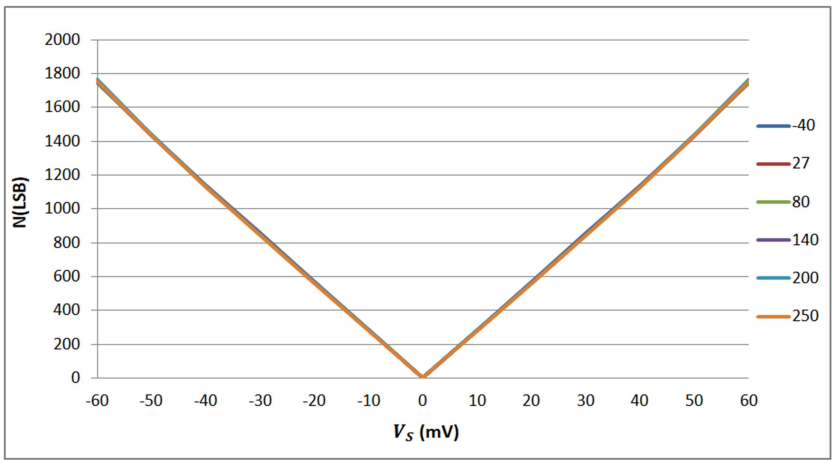


Figure 3.47: Simulated characteristic function of the sensor interface for different temperatures.

These results are in good agreement with the sensor interface specifications mentioned in section 3.1. The reduced full scale compared to the specifications is caused by the mismatch between the free running oscillation frequency at zero V_S ($f_{0(Vs=0)}$) and the locking frequency f_{lock}. This is due to the mismatch between the reference oscillator bias current I_{oscRef} and the TA bias current I_{GM} as previously mentioned. Indeed, this leads to an output full scale lower than π (π is the maximum output full scale equivalent to 2048LSB). Then, since the obtained gain corresponds to the expected gain, an input full scale lower than the targeted one is obtained.

The thermal sensitivity of the sensor interface is evaluated using its relative thermal variation that is written as:

$$\Delta N_{Rel}(ppm/°C) = \frac{\Delta N}{N_{FS}} \frac{10^6}{\Delta T} \quad (3.68)$$

where

$$\Delta N = N_{max} - N_{min} \quad (3.69)$$

where N_{min} and N_{max} are respectively the minimun and the maximum value of the digital output N over the temperature range ΔT and N_{FS} is the output full scale.

Figure 3.48 shows that the sensor interface achieves a low temperature dependence over a wide temperature range; the value of this thermal variation is lower than 34ppm/°C for a full scale of ±60mV. Furthermore, thermal sensitivity is null at zero V_S since the sensor exhibits no offset whatever temperature is.

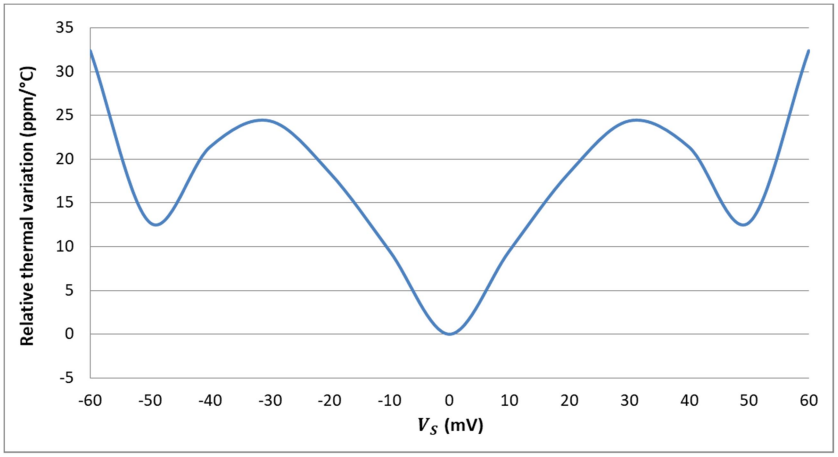


Figure 3.48: Simulated relative thermal variation of the sensor interface output as a function of V_S.

The simulated characteristic function of the sensor interface over the full temperature range (Figure 3.47) highlights the good linearity of the sensor interface, which is obtained thanks to the use of RILOs. Figure 3.49 depicts the simulated integral non-linearity (INL), defined as (simulated value - linear fitted value)/(linear fitted value). An INL lower than 1.8% is obtained over the entire temperature range.

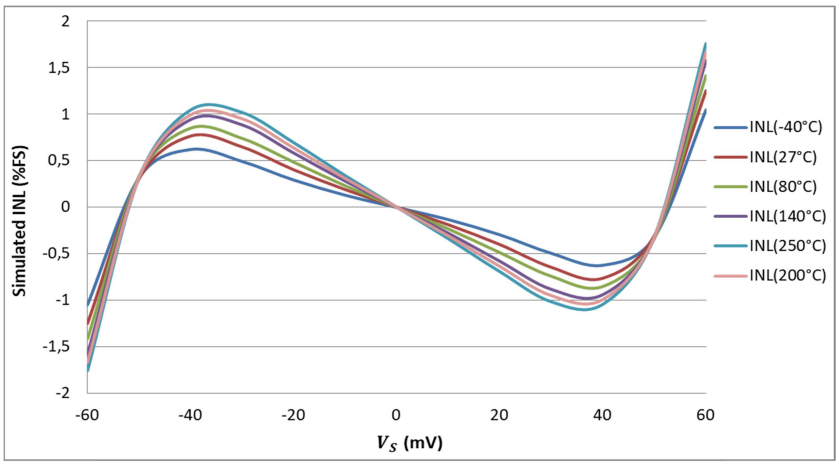
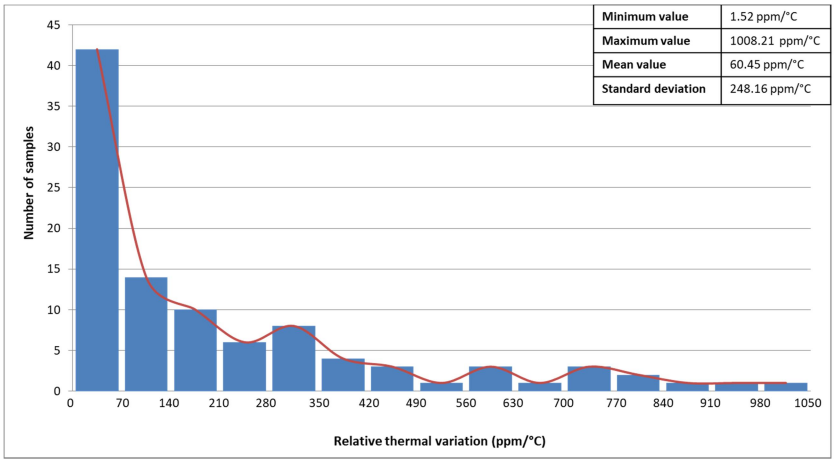


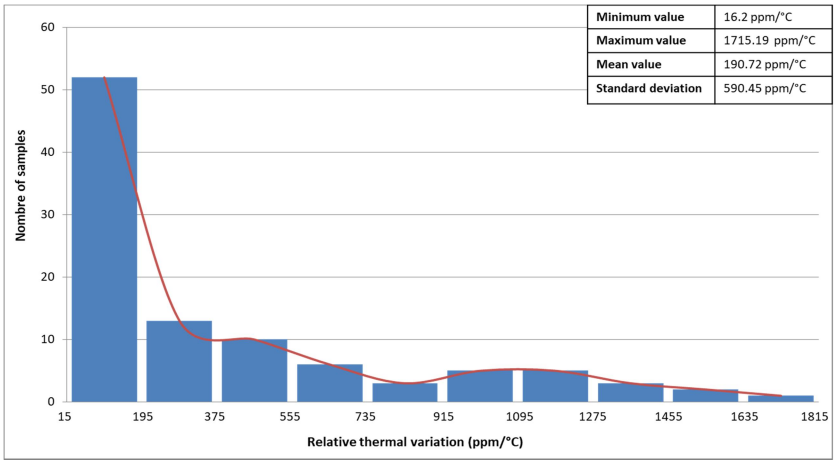
Figure 3.49: Simulated INL of the sensor interface over different temperatures.

3.5.2. Effect of process variations

The thermal stability of the sensor interface is influenced by process variations. Monte Carlo simulations have been performed to investigate the impact of process variations on the temperature dependence. Obtained results are presented in figure 3.50 for two different values of V_S (30mV and 60mV).



(a) V_S =30mV



(b) V_S = 60mV

Figure 3.50: Monte Carlo Simulation of the thermal stability for the sensor interface circuit.

3.6. Conclusion

In this chapter, the **context** and the required **specifications** of the sensor interface are firstly introduced. Based on these specifications, the parameters values of the sensor interface are chosen and then verified using a **behavioural model**.

The sensor interface is based on **Relaxation ILOs (RILOs)** for their **extended linearity range** compared to their harmonic counterparts. Thanks to this property, **the sensor interface exhibits a good linear behaviour**. Because of the use of RILOs, some **design refinements** are added to the original architecture to ensure a good thermal stability of the sensor interface. The digital output of the sensor interface depends on a **ratio of several parameters from same nature**. Hence, its thermal stability depends on the thermal variations of the sensor interface parameters ratios rather than their absolute thermal variations. That is why a low temperature dependence can be obtained. Simulation results show that the sensor interface **achieves a low sensitivity to temperature variations (34ppm/°C)** over a wide temperature range extended from -40°C to 250°C.

In the following chapter, experimental results obtained with a prototype of the sensor interface are reported.

3.7. References

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Chapter4:
Experimental Results of The Sensor Interface

This chapter presents measurement results obtained with the fabricated sensor interface. Static and dynamic characterisations have been performed over a wide temperature range. Measurement results show that the fabricated sensor interface meets the system specification and achieves very low thermal drift over a wide temperature range.

4.1. Overview of the silicon prototype

A sensor interface has been fabricated using a 0.18µm Partially Depleted Silicon On Insulator technology (PD-SOI) from XFab. Its layout is depicted in Figure 4.1. The overall chip dimension is 1860.1µm by 1885.9µm and the active area is of 0.21mm^2.

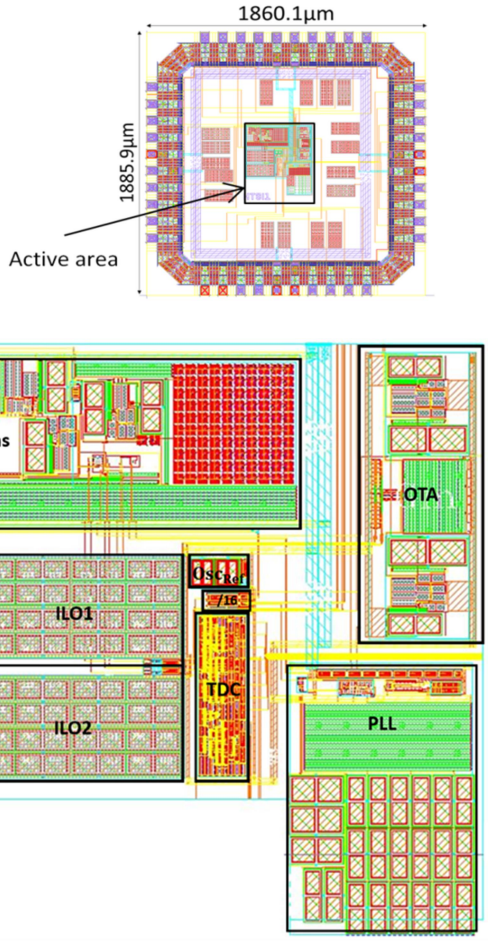
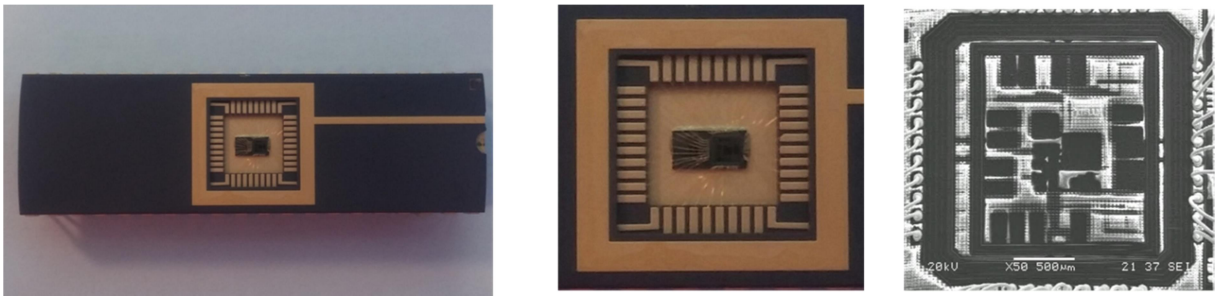


Figure 4.1: Layout of the sensor interface.

The circuit has been packaged in a ceramic DIL-40 package. A ceramic package is chosen because of its robustness to high temperatures. The photography of the fabricated circuit is presented in figure 4.2.



(a) Sensor interface in the package b) Sensor interface in the package (zoom) (c) Chip Microphotography

Figure 4.2: Photography of the fabricated sensor interface.

4.2. Characterisation test bench

A Printed Circuit Board (PCB) has been realized to enable the circuit characterisation over a wide temperature range. Input differential voltage and digital configuration bits are generated by a FPGA and digital-to-analog converters (Figure 4.3).

The sensor output voltage V_S is emulated through a temperature independent differential signal which is generated by means of an on-board signal generator.

A LabVIEW test environment is used for automatic data acquisition. For each value of the differential input voltage V_S, the digital output of the sensor interface is obtained by averaging 2000 samples.

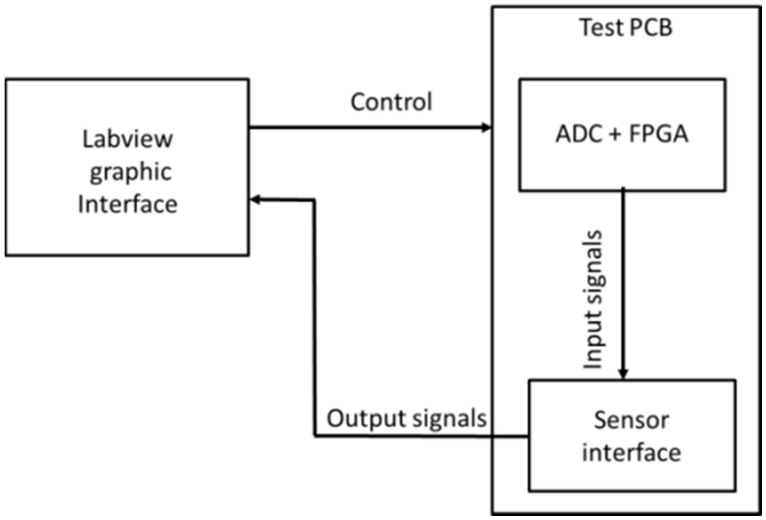
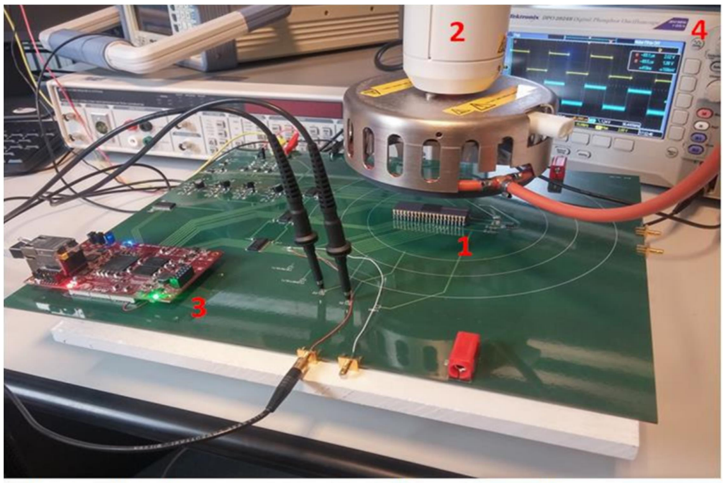


Figure 4.3: Principle of the measurement test bench.

In order to characterise the circuit over a wide temperature range, a thermal conditioner (Thermostream ATS), which sets the operation temperature by blowing a temperature-controlled air, is used. The prototype is placed under the nozzle of the thermal conditioner to vary its temperature from −20 °C to 220 °C, which are the minimum and maximum temperatures of the thermal conditioner (Figure 4.4).



1- The circuit prototype
2- Thermostream ATS
3- FPGA
4- Timing diagram of O_{ILO1} and O_{ILO2}

Figure 4.4: Characterisation test bench for the fabricated prototype.

4.3. Transfer function of the sensor interface

The sensor interface converts the sensor output voltage V_S into a phase shift difference between the two ILOs outputs, which is then converted into a digital output N.

Figure 4.5 depicts the locking signal V_{lock} and the two ILOs outputs O_{ILO1} and O_{ILO2} visualised by an oscilloscope for positive and negative sensor output voltage V_S. It shows that both ILOs are well locked on the locking signal; they run at the locking signal frequency which is equal to 38kHz (typical simulations run at 35kHz). Besides, Figure 4.5 also shows that the phase shift between the ILOs outputs is a function of the sensor output V_S, which confirms the operating principle of the sensor interface. Moreover, as expected, ILO1 output is in phase advance with respect to ILO2 output for positive V_S, while ILO2 output is in phase advance for negative V_S.

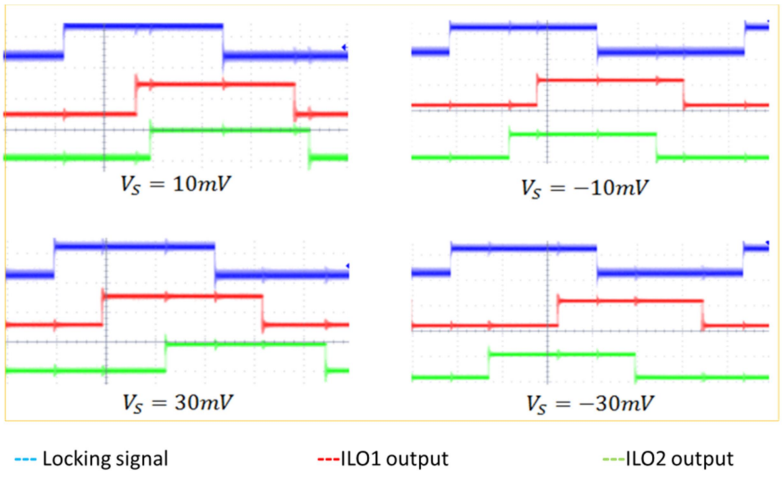


Figure 4.5: Visualisation of locking signal and ILO's outputs (at room temperature).

The measured transfer function is reported in figure 4.6 over a temperature range extended from -20°C up to 220°C. It shows that the sensor interface LSB corresponds to 33.3µV (i.e., the sensor interface gain is around 30LSB/mV) whatever temperature is. This result is in good agreement with the system specifications (chapter 3). In addition, since the output full scale is equal to 1872.5 LSB, the sensor interface achieves a resolution of 11 bits.

A bit sign is used to differentiate positive from negative sensor output voltages (Figure 4.7). The lead/lag output bit gives the sign of the sensor output voltage V_S. This bit is at high logic level for positive V_S and at low logic level for negative V_S.

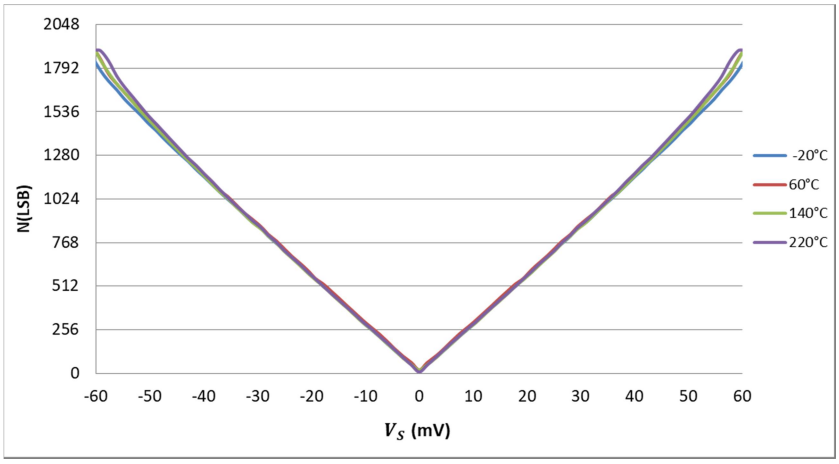


Figure 4.6: Experimental transfer function of the sensor interface [-20°C; 220°C].

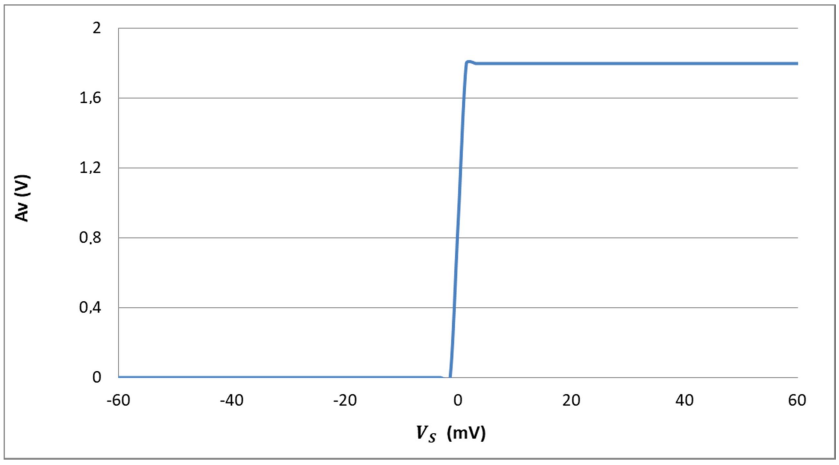


Figure 4.7: Measured lead/lag output bit to determine the sign of the differential input voltage.

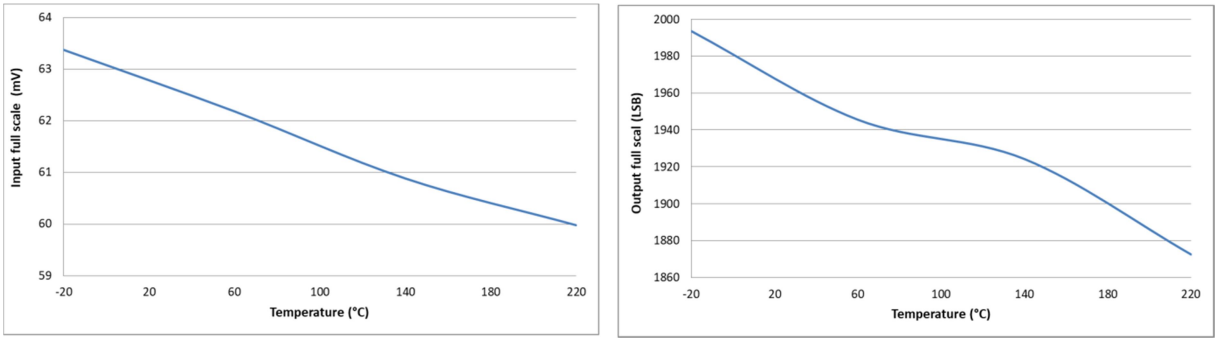
4.3.1. Full scale of the sensor interface

4.3.1.1. Measured full scale

The sensor interface was designed to interface sensors with an output full scale of ±66mV. However, measurements show an input full scale lower than ±66mV leading to an output full scale lower than the specified one (i.e., 2048LSB).

Figure 4.8 depicts the measured input and output full scales of the sensor interface as a function of the temperature. It shows that the maximum measurable sensor output voltage

(i.e., the sensor interface input full scale) and hence the sensor interface output full scale decreases with temperature. Considering the entire temperature range (-20°C to 220°C), the sensor interface is suitable for sensors with an output full scale of ±60mV.



(a) Input full scale $V_{S\text{-}FS}$ **(b) Output full scale N_{FS}**

Figure 4.8: Measured full scale of the sensor interface.

4.3.1.2. Analysis of the sensor interface full scale

This section is dedicated to explain the origin of the full scales reported in figure 4.8. Let's recall the equation of the sensor interface output:

$$N = \frac{\Delta\phi_{out}}{2\pi} \frac{f_{counter}}{f_{lock}} \quad (4.1)$$

where $\Delta\Phi_{out}$ is the phase shift between the ILOs outputs. $f_{counter}$ and f_{lock} are respectively the counter and the locking frequencies.

Hypothesis

The ILOs are designed to obtain a phase shift difference between the ILO's outputs (i.e., $\Delta\Phi_{out}$) equal to π for a sensor output voltage V_S of ±66mV.

Then, if the phase shift difference $\Delta\Phi_{out}$ has a full scale lower than π, the equivalent sensor output voltage V_S, which represents the interface input full scale, is lower than ±66mV. Then, the full scale of the digital output (i.e., the output full scale) is also limited and its value is lower than 2048 LSB (a phase shift difference $\Delta\Phi_{out}$ of π corresponds to 2048 LSB).

Verification

Figure 4.9 shows the ILO's outputs at the input full scale of the sensor interface (i.e., ±62.8mV at 20°C). It shows that the full scale of $\Delta\Phi_{out}$ is lower than π; it is equal to 0.963π (t_{pw_FS}=12.53µs). This confirms the previous hypothesis.

The equivalent full scale of $\Delta\Phi_{out}$ should correspond to an output full scale of ±1972 LSB ($f_{counter}/f_{lock}$ = 4096). Figure 4.8 shows that the measured output full scale of the sensor interface (N_{FS}) at this temperature is of ±1968 LSB.

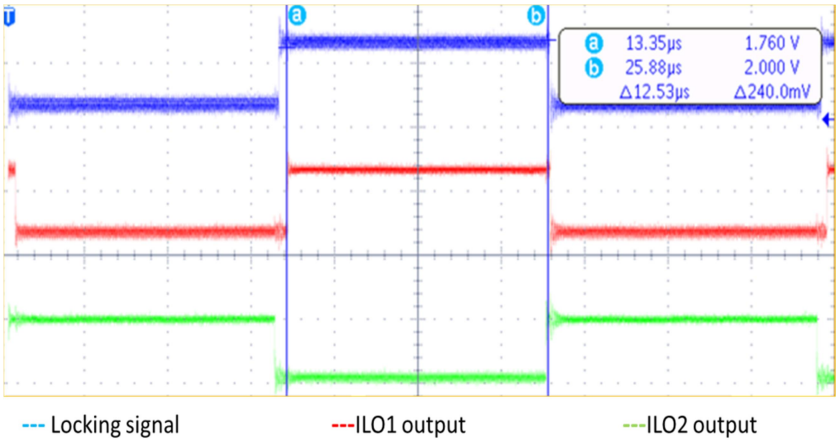


Figure 4.9: Timing diagram of the fabricated sensor interface at full scale; Temperature equals to 20°C.

The small residual difference between N_{FS} equivalent to the full scale of $\Delta\Phi_{out}$ (i.e., ±1972 LSB) and the measured N_{FS} (i.e., 1969 LSB) can be explained by noise. Indeed, noise is at the origin of counter clock jitter that leads to some instabilities of $f_{counter}$ (Figure 4.10) and, therefore, to some changes in the ratio $f_{counter}/f_{lock}$ ($f_{counter}/f_{lock}$ is then different from 4096).

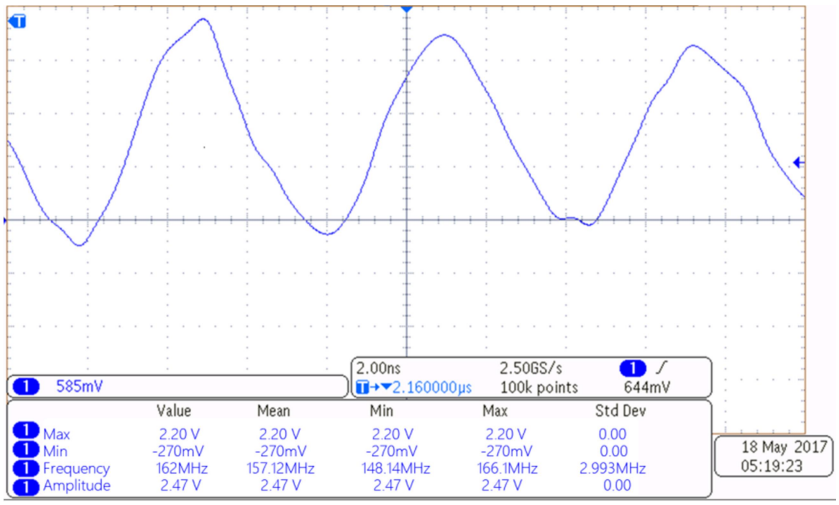


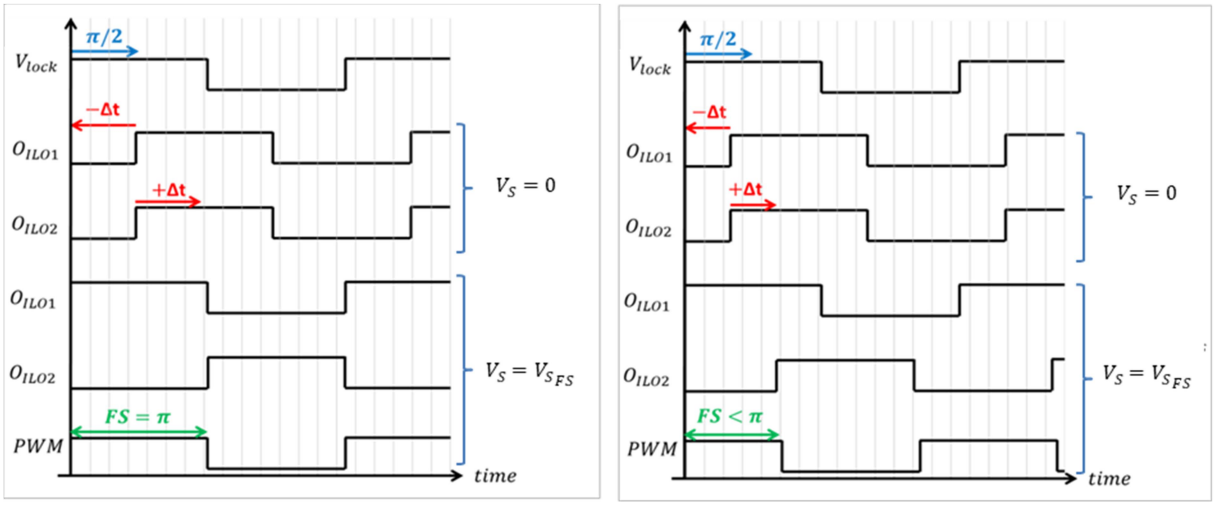
Figure 4.10: Visualisation of the counter clock signal.

Discussion of the $\Delta\Phi_{out}$ full scale

The full scale of $\Delta\Phi_{out}$ is lower than π because phase shifts of both ILOs at zero V_S are different from π/2 (Figure 4.11). The full scale of the sensor interface is defined by the differential input voltage V_S where one ILO saturates (i.e., its phase shift equals to zero or π).

If phase shifts at zero V_S are both equal to π/2 (Figure 4.11.a), both ILOs reach the end of their locking range for the same input voltage and the so-obtained full scale of $\Delta\Phi_{out}$ is equal to π (for example $\Phi_{ILO1} = 0$ and $\Phi_{ILO2} = \pi$). In presence of mismatch-induced offset, ILOs phase shifts at zero V_S are different from π/2 (Figure 4.11.b); when V_S changes (increases in the given example), the two ILOs phase shifts vary symmetrically with respect to their initial value. Consequently, ILO1 saturates (i.e., $\Phi_{ILO1} = 0$) while ILO2 did not (i.e.,

$\Phi_{ILO2} < \pi$). Consequently, the full scale of $\Delta\Phi_{out}$ is lower than π; this phenomenon defines the full scale of the sensor interface.



(a) Ideal case **(b)Real case**

Figure 4.11: Explanation of the reduced output full scale.

From equation (3.12), it is obvious that the ILO's phase shift is different from π/2 if and only if the locking frequency f_{lock} is not equal to the ILO's free running frequency f_0. We can then conclude that this difference is due to the difference between the locking frequency f_{lock} and the ILOs free running frequencies at zero V_S: $f_{0(Vs=0)}=f_{01(Vs=0)}=f_{02(Vs=0)}$.

This phenomenon, already identified in the design phase (Section 3.4.3.3), is due to a mismatch between the reference oscillator bias current (I_{OscRef}) and the ILOs bias currents at zero V_S ($I_{0(Vs=0)}$). Moreover, this mismatch increases with temperature, which makes the difference between f_{lock} and $f_{0(Vs=0)}$ more important at higher temperatures. Consequently, as shown in figure 4.12, the full scale of $\Delta\Phi_{out}$ decreases with temperature. This explains why the sensor interface full scales reduce with temperature.

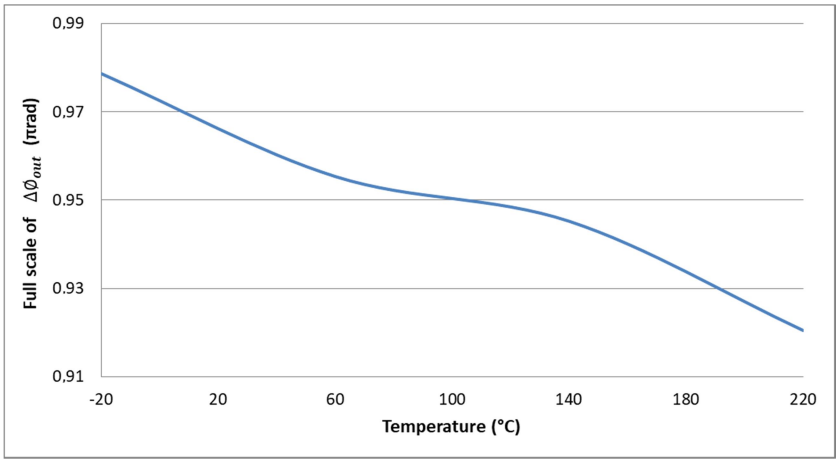


Figure 4.12: Measured full scale of $\Delta\Phi_{out}$ of the fabricated sensor interface.

A calibration loop can be implemented in order to obtain a full scale of π for $\Delta\Phi_{out}$ over the whole temperature range. This could be performed by ensuring the equality between

the locking frequency f_{lock} and the ILOs free running oscillation frequencies at zero V_S whatever temperature is. This would finally guarantee the specified input full scale (i.e., ±66mV).

4.3.2. Offset of the sensor interface

4.3.2.1. Input offset

Considering the transfer function of the sensor interface (Figure 4.6), the input offset (i.e., the input voltage corresponding to N=0) is reported as a function of temperature (Figure 4.13).

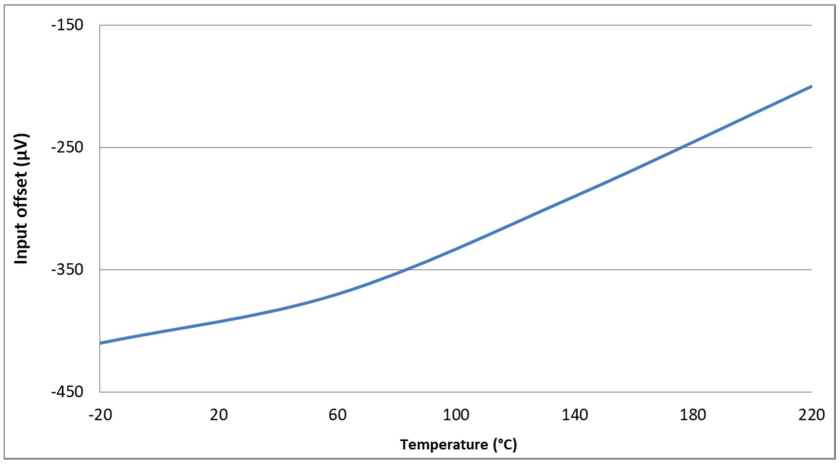


Figure 4.13: Measured input offset for different temperatures.

4.3.2.2. Output offset

At zero input voltage V_S, the digital output of the sensor interface is different from zero. Figure 4.14 depicts this output offset as a function of temperature.

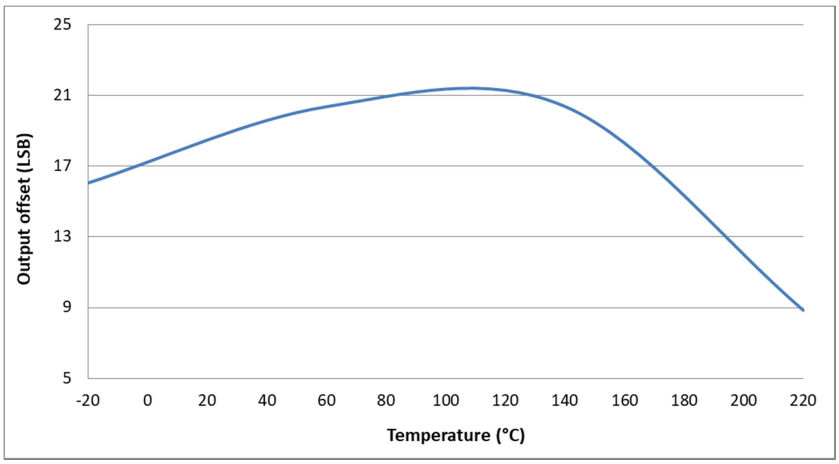


Figure 4.14: Measured output offset for different temperatures.

4.3.2.3. Analysis of the sensor interface offset

Since output and input offsets are related to each other, the analysis of the sensor interface offsets is limited to the analysis of the output offset.

The output offset of the sensor interface is caused either by the mismatch between the ILOs (i.e., the ILOs do not have the same phase shift when they are biased by the same current) or by an offset of the transconductance amplifier (i.e., the difference between the TA's output currents is not equal to zero at zero input voltage). In order to investigate the origin of the output offset, mismatches between the ILOs and TA offset have been simulated in presence of process variations (at a fixed temperature of 20°C).

Figure 4.15 shows Monte Carlo simulations of the pulse width t_{pw} that represents the phase shift between the ILOs at V_s=0 ($\Delta\Phi_{out} = 2\,\pi\,f_{lock}\,t_{pw}$). In this simulation, both ILOs are biased by the same current. A standard deviation of 100ns is obtained that corresponds to 14LSB.

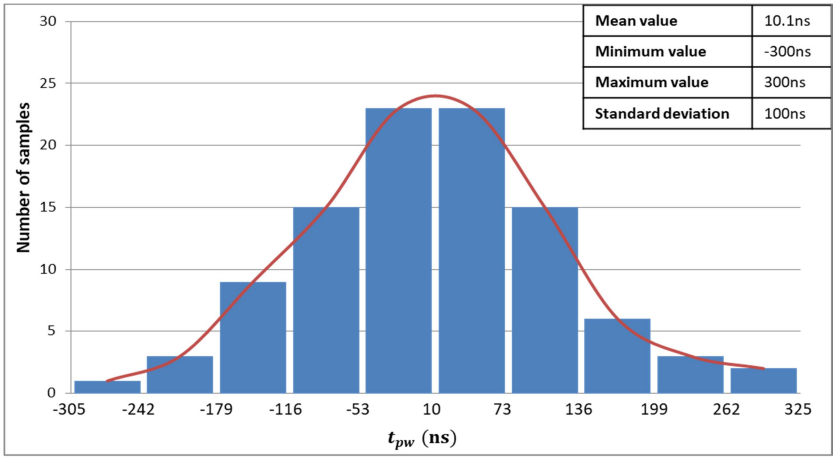


Figure 4.15: Monte Carlo simulation results of the mismatch between the ILOs.

Figure 4.16 shows the Monte Carlo simulations of the difference between the TA output currents I_{01}-I_{02} at zero input voltage V_S. A standard deviation of 31 nA corresponding to 89LSB is obtained. Therefore, it can be concluded that the Transconductance Amplifier (TA) offset is the main source of offset.

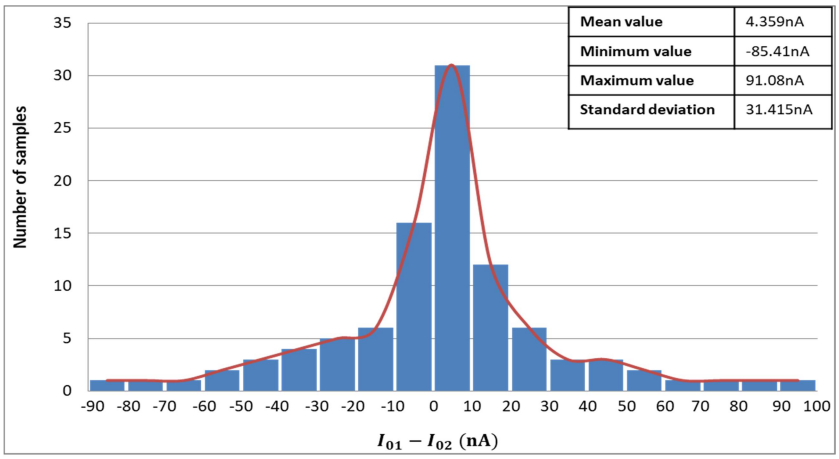


Figure 4.16: Monte Carlo simulation results of the TA output offset.

According to the expression below (Equation (4.2)), the TA offset relies on mismatches between I_{GM1} and I_{GM2} and between $V_{offset1}$ and $V_{offset2}$:

$$I_{01} - I_{02} = (I_{GM} \ - I_{GM2}) + 2\,\frac{V_S + (V_{offset1} - V_{offset2})}{R_{GM}} \qquad (4.2)$$

where I_{GM1} and I_{GM2} are the TA bias currents which are generated from a reference current I_{GM} by means of current mirrors. $V_{offset1}$ and $V_{offset2}$ are respectively the offset voltages of the left and right sides amplifiers (Figure 4.17).

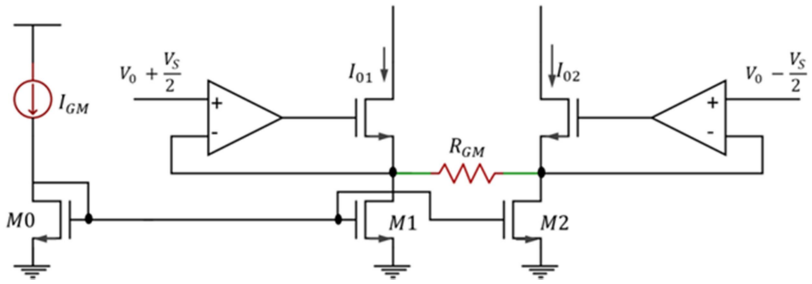
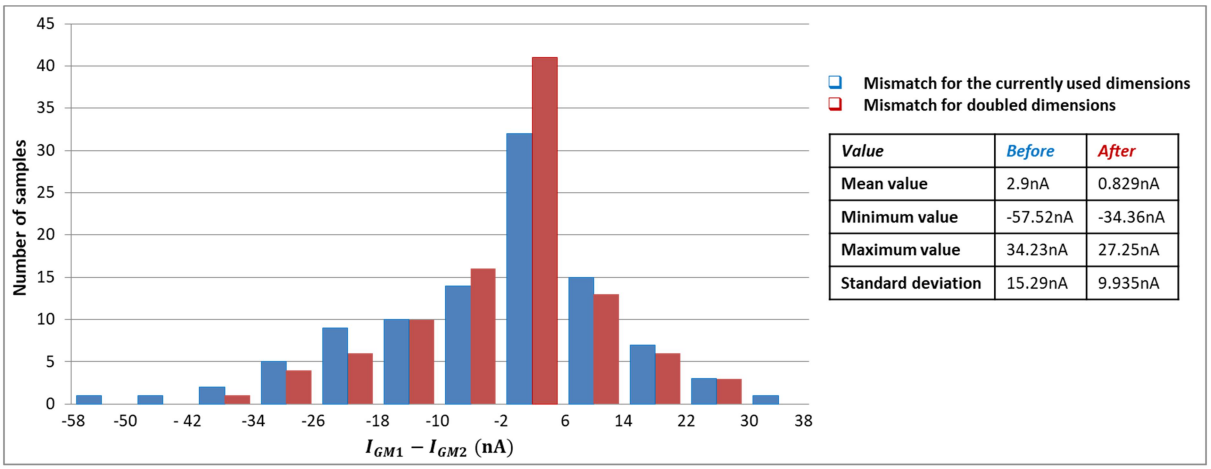


Figure 4.17: Transconductance amplifier.

4.3.2.4. Proposed solution to reduce the offset of the sensor interface

Since the mismatch between I_{GM1} and I_{GM2} is one of the causes of the measured output offset, the use of larger transistors for the transistors constituting the current mirrors (M_0, M_1 and M_2) should reduce it.

Figure 4.18 depicts Monte Carlo simulation results of the mismatch between I_{GM1} and I_{GM2}, for the currently used dimensions of M_0, M_1 and M_2 (in blue) and after doubling their dimensions (in red). As expected, increasing the size of transistors reduces the mismatch between I_{GM1} and I_{GM2}. The impact of this solution has been also evaluated at the output of the TA by evaluating again the offset of I_{01}-I_{02} at zero input voltage V_S (Figure 4.19).



Value	Before	After
Mean value	2.9nA	0.829nA
Minimum value	-57.52nA	-34.36nA
Maximum value	34.23nA	27.25nA
Standard deviation	15.29nA	9.935nA

Figure 4.18: Effect of dimensions of M_0, M_1 and M_2 on the mismatch between I_{GM1} and I_{GM2}.

On the one hand, it is demonstrated that the increase in dimensions of the current mirrors reduces the output offset but, on the other hand, the limitted improvement demonstrates that some effort should be concentrated on reducing the offset of both amplifiers.

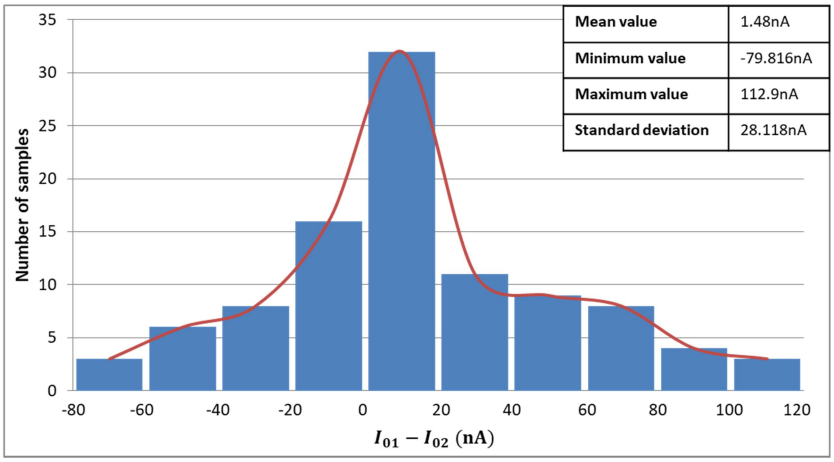


Figure 4.19: Monte Carlo simulations of the TA offset after doubling transistor dimensions.

4.4. Non linearity of the sensor interface

The transfer function of the sensor interface exhibits a good linearity thanks to the use of RILOs as phase shifters. Figure 4.20 depicts the integral non-linearity of the circuit (INL), i.e., the difference between the measured values and values obtained from the linear fit of the experimental curve, for different temperatures.

A maximum non-linearity of 6% of the full scale is observed at the extremities of the input range. Moreover, as temperature increases, the non-linearity of the sensor interface slightly increases. Note that measured INL is higher than the simulated one (section 3.5.1); this can be explained by process variations.

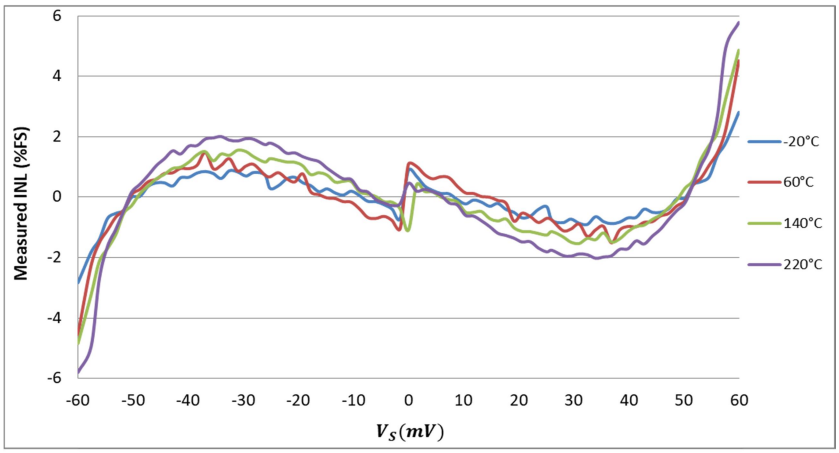


Figure 4.20: Measured integral non-linearity of the fabricated sensor interface.

4.4.1. Analysis of the sensor interface non-linearity

The contributing blocks to the non-linear behaviour of the sensor interface are the TA and the ILOs. Simulations of non-linearity of the TA and the ILOs have been performed to identify the highest contribution to the sensor interface non-linearity.

4.4.1.1. Non linearity of the TA

The non-linearity of the TA output current difference (I_{01}-I_{02}) is simulated for an input voltage V_S ranging from -60mV up to 60mV (Figure 4.21). This figure shows that the TA has a good linearity since its INL is lower than 0.08%.

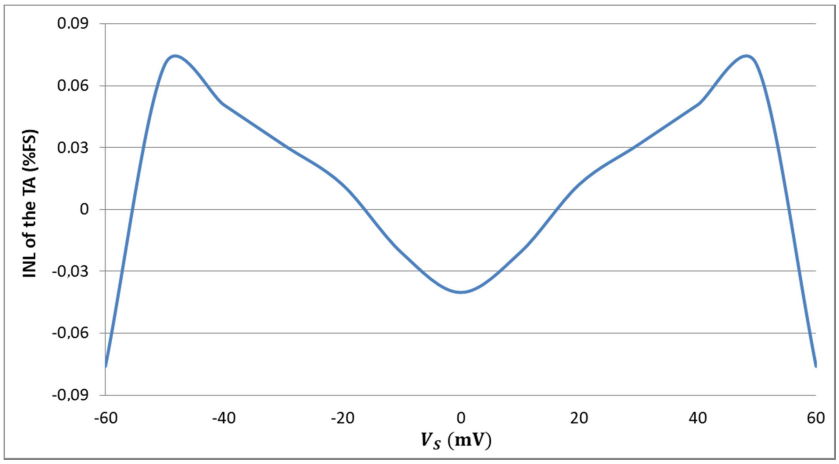


Figure 4.21: Simulated INL of the TA.

4.4.1.2. Non linearity of the ILO

The non-linearity of the ILO phase shift Φ_{ILO} is simulated for an input bias current I_0 from 300 to 1100nA (Figure 4.22), respectively the minimum current I_{0min}, that gives a π phase shift, and the maximum one I_{0max}, that gives a 0 phase shift. Figure 4.22 shows that the maximum INL of the ILO is around one order of magnitude higher than that of the TA. Moreover, it shows that the ILO INL is higher at lower bias current.

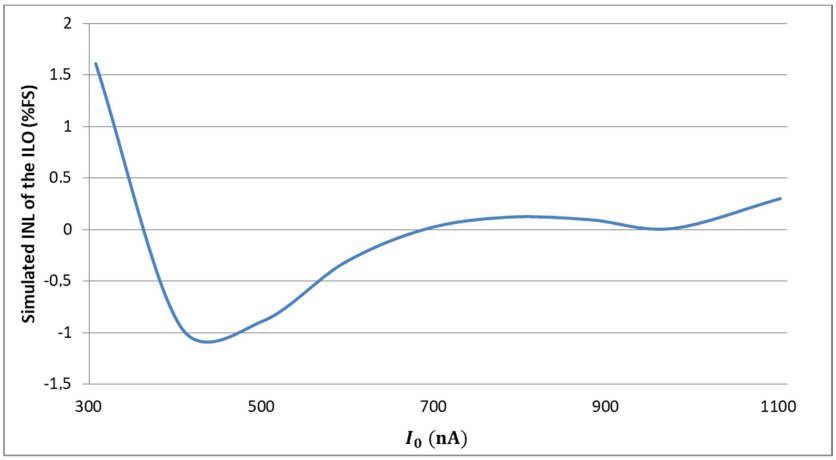


Figure 4.22: Simulated INL of the ILO.

Origin of the non-linear behaviour of the ILO

Let's recall the expression of the ILO phase shift with respect to the input bias current I_0:

$$\phi_{ILO} = \pi\left(\frac{C\,V_{th}}{I_{lock}}\,f_{lock} + \frac{1}{2}\right) - \frac{\pi}{2\,I_{lock}}I_0 \quad (4.3)$$

where I_{lock} is the locking current.

Variations of the ILO phase Φ_{ILO} with I_0 are inversely proportional to the locking current I_{lock}. Then, I_{lock} must be constant over the full range of the input current to obtain a good linear behaviour. This condition is obtained only if the locking current sources (I_{lock_up} and I_{lock_down}) are in the saturation region (Figure 4.23).

By analysing the operation of the ILOs, it was found that the upper locking current source I_{lock_up} is always in the saturation region while the saturation of the lower locking current source I_{lock_down} depends on the voltage across the capacitor U_{C2} (Figure 4.23). Indeed, I_{lock_down} is in the saturation region (i.e., M_{ID} is saturated) only when U_{C2} is higher than $V_{ds\_sat}(M_{ID})+V_{ds}(M_2)$ (where $V_{ds\_sat}(M_{ID})$ is the saturation voltage of M_{ID}) (Figure 4.24).

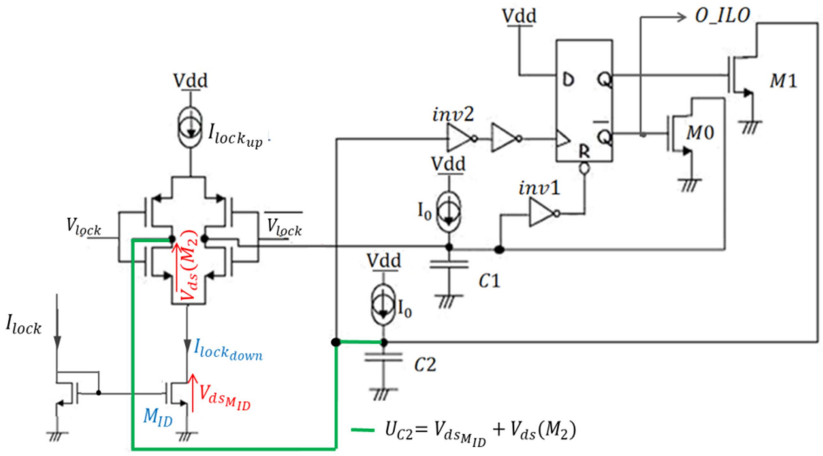


Figure 4.23: Architecture of the ILO.

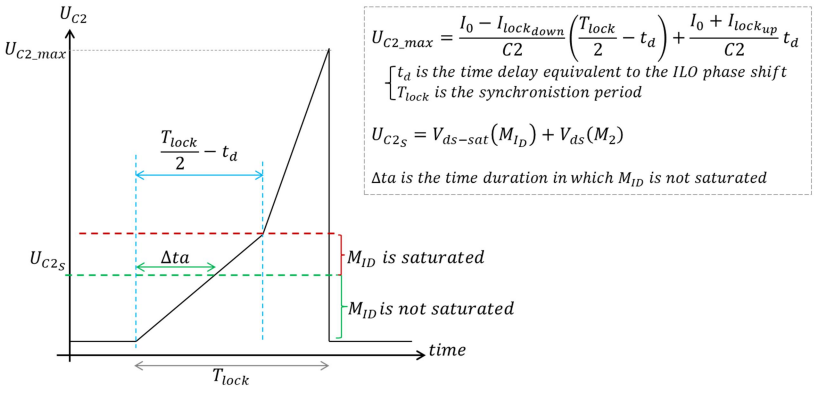


Figure 4.24: Explanation of the saturation condition of M_{ID}.

Given that I_{lock_down} contributes only during the first part of time of the T_{lock} period (Figure 4.24), the fact that I_{lock_down} is not always saturated is probably at the origin of the ILO non-linearity.

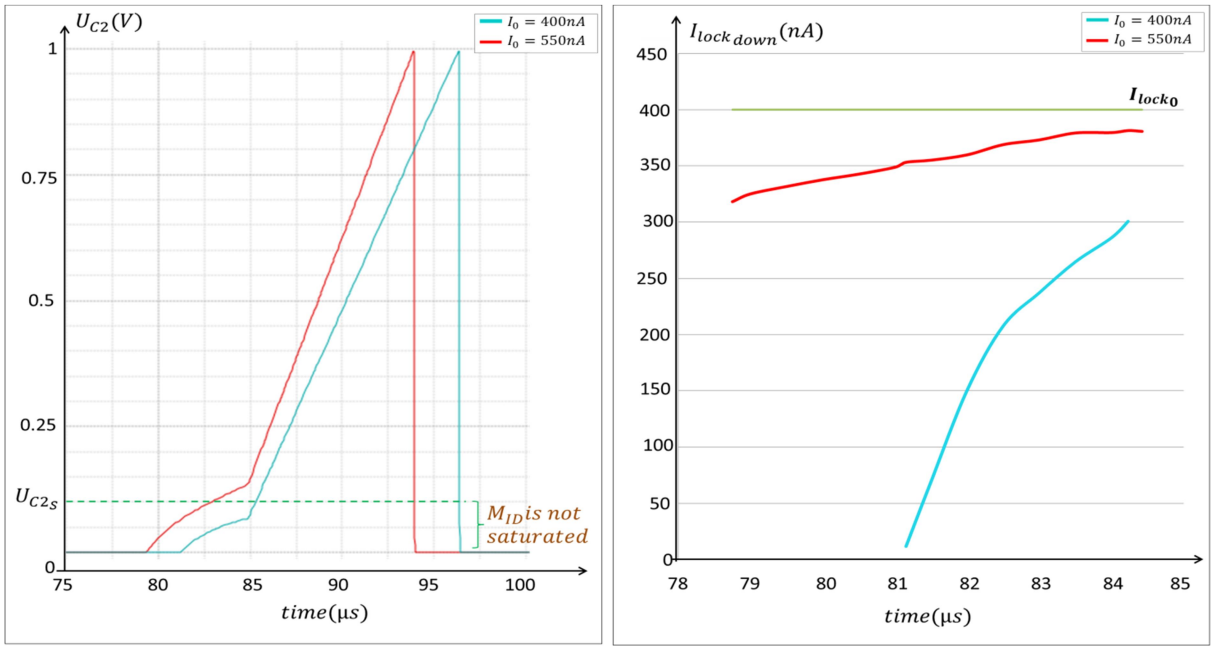
On the one hand, when the locking current source connected to ground is not in the saturation region, the value of I_{lock_down} depends on the M_{ID} drain to source voltage $V_{ds}(M_{ID})$ and thus its value is lower than expected.

On the other hand, the M_{ID} drain to source voltage is a function of the voltage U_{C2} and therefore, of the input bias current I_0 (since the integration slope of U_{C2} depends on I_0).

Therefore, the value of I_{lock_down} depends on the ILO input bias current I_0. Then, the gain of the ILO phase shift is not the same over the full range of input current I_0 which explains the non-linear behaviour of the ILO.

Figure 4.25 reports the magnitude of U_{C2} and I_{lock_down} for two different input currents I_0. It is obvious that at lower bias current, the voltage U_{C2}, and hence the drain to source voltage of M_{ID}, has a lower value particularly during ((T_{lock}/2) - t_d). Thus, I_{lock_down} obtained for a bias current I_0 of 400nA is lower than that obtained for a bias current I_0 of 550nA. This confirm the non-uniformity of the locking current I_{lock_down} over the range of the ILO input bias current I_0.

Knowing that the gain of the ILO is a function of the locking current, the difference between the ILO gain (i.e., π/I_{lock_down}) with respect to the ideal gain (i.e., π/I_{lock_0}) and hence the difference between the ILO phase shift (obtained for I_{lock_down}) with respect to the perfectly linear ILO phase shift (obtained for I_{lock_0}) is higher at lower bias current I_0. This explains the harsher non-linearities at lower I_0 values.



(a)Timing diagram of U_{C2} for different bias currents **(b) Generated I_{lock_down} current for different bias currents**

Figure 4. 25: Explanation of the high non-linearity of ILOs at lower bias current I_0.

4.4.1.3. Conclusion

The non-linear behaviour of the sensor interface is the result of the TA non-linearity and the ILOs non-linearity according to equation (4.4). The demonstration of this equation is given in Appendix A:

$$INL_{SI} = INL_{TA} + INL_{ILO} + 2\,INL_{TA}\,INL_{ILO} \qquad (4.4)$$

where $INL_{SI,}$ INL_{TA} and INL_{ILO} are respectively the Integral Non-Linearities of the sensor interface, the transconductance amplifier and the ILO. According to previous sections, the INL_{ILO} is much higher than that of the transconductance amplifier. Therefore, ILOs have the highest contribution to the non-linearity of the sensor interface.

What is more, ILOs exhibit higher non-linearity at lower bias current which corresponds to the upper limit of their locking range (i.e., when the ILO phase shift is equal to π). Considering the overall sensor interface, the minimum ILO bias current I_{0min} corresponds to the bias current of ILO1 when V_S equals the positive input full scale (i.e., the upper extremity of the input full scale) and to the bias current of ILO2 when V_S equals the negative input full scale (i.e., the lower extremity of the input full scale). Thus, at the upper extremity of the input full scale, ILO1 has a harsher non-linear behaviour; while at the lower extremity of the input full scale, ILO2 has a harsher non-linear behaviour. This explains why the overall sensor interface exhibits the highest INL at the extremities of its input full scale.

Calibration techniques can be used to compensate the obtained non-linearity of the sensor interface by means of numerical techniques such as look up tables.

4.4.2. INL of the sensor interface over a reduced full scale

Since the maximum INL is obtained at the extremities of the full scale, it is interesting to limit the input full scale of the sensor interface in order to have a better linearity. Figure 4.26 depicts the measured INL on a reduced full scale of ±40mV. The maximum measured INL is then lower than 1.5% of FS over the entire operation temperature range.

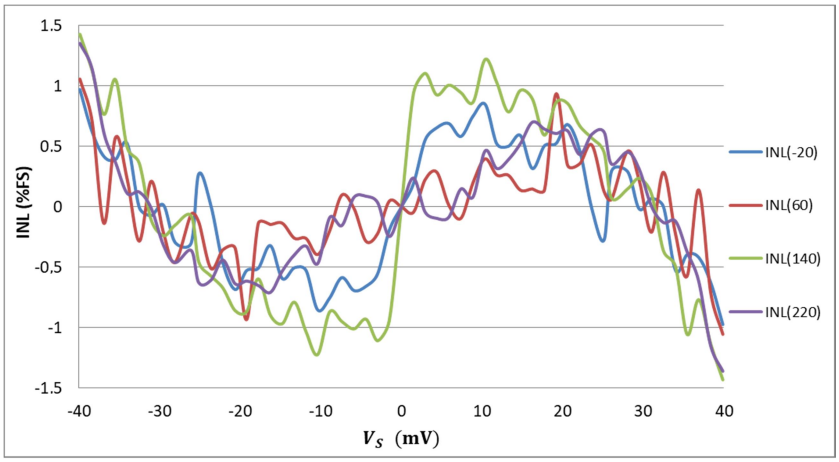


Figure 4.26: Measured INL of the fabricated sensor interface over a full scale of ±40mV.

Another possible solution to extend the linear range of the sensor interface is to decrease its gain (by using a higher locking current or a lower transconductance gain). This solution enables the extension of the input voltage range in which the sensor interface exhibits a good linearity but this is obtained at the expense of the sensor interface resolution. However, using a higher ratio $f_{counter}/f_{lock}$ could resolve this problem.

Moreover, the use of another RILO topology with a better linearity could improve the INL of the RILO-based sensor interface. Figure 4.27 shows an alternative RILO topology that

is expected to have a better linearity. Indeed, by analogy with the currently adopted RILO, and considering I_0 as an input, the gain of the phase shift (i.e., $d\Phi_{ILO}/dI_0$) of the RILO presented in figure 4.27 is a function of I_{lock}. Since the locking current sources I_{lock} are always saturated, their values are invariable and the gain of the RILO phase shift is expected to be constant which leads to a better linearity.

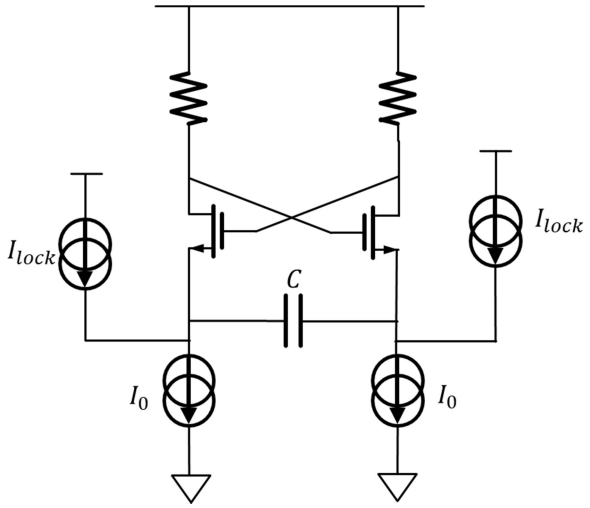


Figure 4.27: Alternative topology of the Relaxation Injection Locked Oscillator (Badets et Belot 2003).

4.5. Temperature dependence of the sensor interface

The temperature dependence of the sensor interface is evaluated, for different values of the input voltage, using equation below that expresses the relative thermal variation of the digital output.

$$\Delta N_{Rel}(ppm/°C) = \frac{\Delta N}{N_{FS}} \frac{10^6}{\Delta T} \quad (4.5)$$

where

$$\Delta N = N_{max} - N_{min} \quad (4.6)$$

where N_{min} and N_{max} are respectively the minimun and the maximum value of the digital output N over the temperature range ΔT and N_{FS} is the output full scale.

Figure 4.28 depicts the relative thermal variation of the digital output of the sensor interface as a function of the sensor output voltage V_S for temperatures from -20°C to 220°C. It shows that the sensor interface achieves a low temperature dependence over this wide operation temperature range and that the maximum sensitivity is obtained at the extremities of the input full scale (i.e., 178ppm/°C for V_S of ±56.2 mV).

The measured relative thermal variation is higher than that obtained by simulations mainly at the extremities of the input full scale. Let's recall the expression of the digital output of the sensor interface:

$$N = \frac{1}{2}\frac{R_{Bias}}{R_{GM}}\frac{f_{counter}}{f_{lock}}\frac{V_S}{V_{BG}} \qquad (4.7)$$

During experimentations, the sensor output voltage V_S is emulated with a temperature independent voltage. Then, the thermal drift of the bandgap voltage V_{BG} is not compensated. This contributes to an additional thermal variation of the prototype compared to that obtained by simulation. Two other sources of the measured thermal sensitivity are studied in the following section.

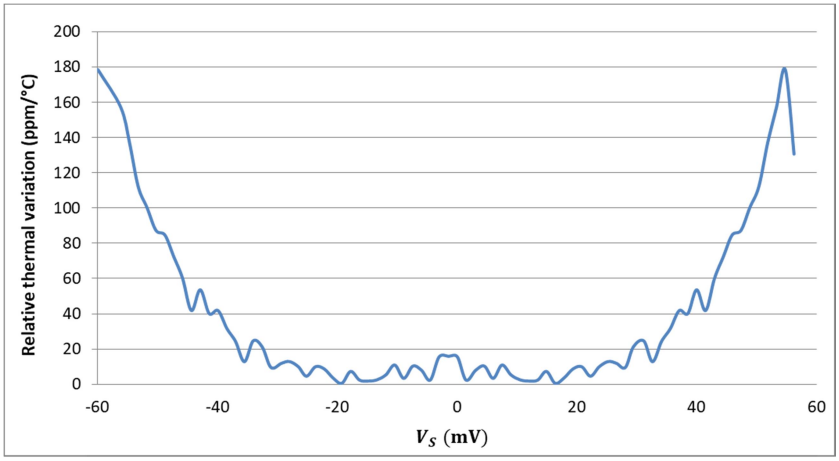


Figure 4.28: Relative thermal variation of the fabricated sensor interface.

4.5.1. Thermal variation of the ratio $f_{counter}/f_{lock}$

The measured ratio between the counter and locking frequencies $f_{counter}/f_{lock}$ is presented in figure 4.29. The observed variation of this ratio is probably caused by experimental noise that makes the counter clock signal slightly deviate from its ideal oscillation frequency (i.e., 4096 times f_{lock}). Yet, this ratio is stable over the entire operation temperature range (5.8 ppm/°C) and this stability is obtained thanks to the fact that both signals are generated from the same reference oscillator. Hence, this cannot explain the residual measured thermal variation (compared to simulations).

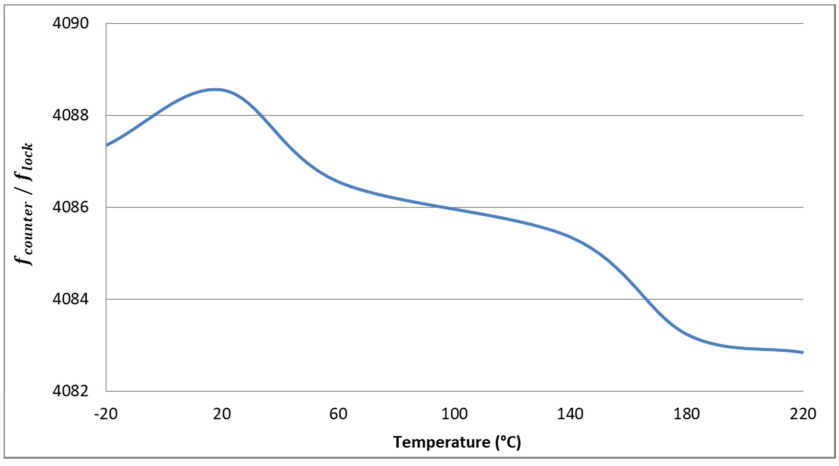


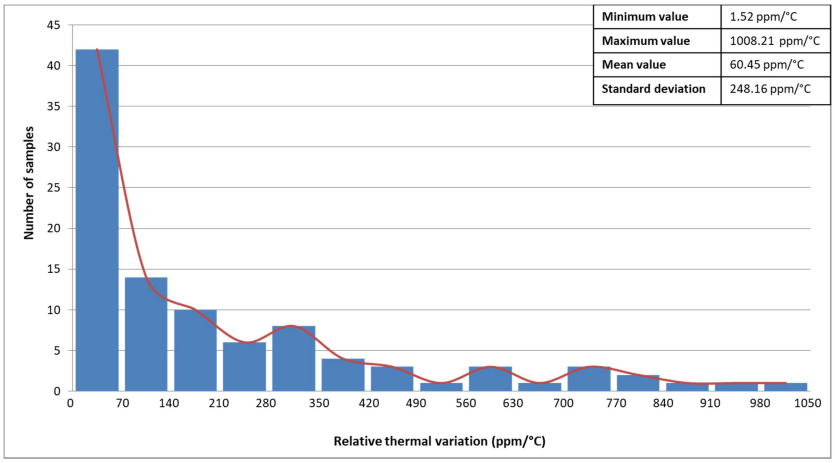
Figure 4.29: Measured ratio $f_{counter}$ / f_{lock} versus temperature.

4.5.2. Process variations and mismatch

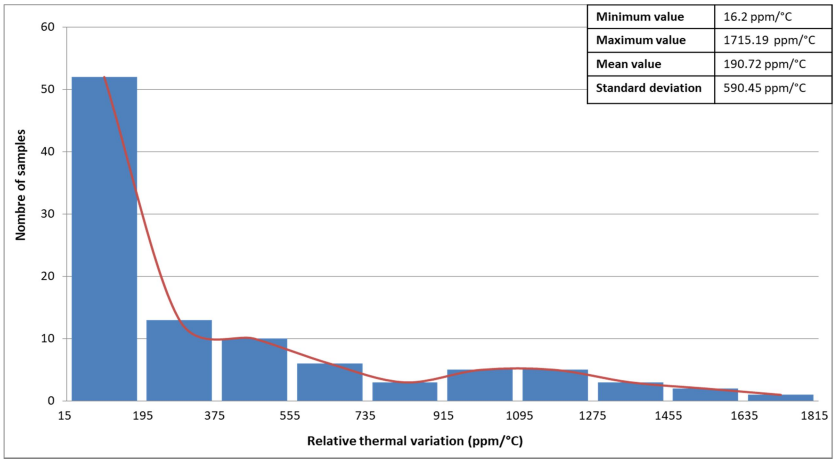
Thermal stability of the fabricated sensor interface is influenced by process variations and mismatches. Their effects on the thermal stability have been assessed through Monte Carlo simulations (Figure 4.30). The relative thermal variation of the different Monte Carlo samples is evaluated using the following equation:

$$\Delta N_{Rel}(ppm/°C) = \frac{N_{max} - N_{min}}{N_{FS}} \frac{10^6}{\Delta T} \quad (4.8)$$

where N_{max} and N_{min} are respectively the maximum and the minimum digital output values over the temperature range ΔT.



(a) V_S =30mV



(b) V_S = 60mV

Figure 4.30: Monte Carlo Simulation results of the thermal stability of the sensor interface.

From the above graphs, it can be observed that relative thermal variations obtained by Monte Carlo simulation is higher than the one obtained by typical simulation (i.e., 24.36 ppm/°C and 32 ppm/°C for V_S equal to 30mV and 60mV respectively). Therefore, it can be concluded that the effect of process variation and mismatch may be the predominant cause of experimentally observed thermal sensitivity.

In addition to that, the high temperature dependence measured at the extremities of the full scale mainly relates to the estimator that was used (Equation (4.8)). Indeed, dividing the

thermal dependence (N_{max}-N_{min}) by a constant (the full-scale N_{FS}) is intrinsically a source of high sensitivity for large values of N. Moreover, this may be explained by the fact that the effect of process variation and mismatch is more pounced in the extremity of the full scale.

4.5.3. Measured relative thermal variation over a reduced full scale

Since the highest thermal sensitivity is obtained at the extremities of the full scale, it would be interesting to reduce the input full scale. Figure 4.31 depicts the relative thermal variation measured over an input full scale of ±40mV. For this reduced input full scale, a very low temperature dependence is obtained; the absolute value of the thermal variation is always below 65ppm/°C over the full temperature range.

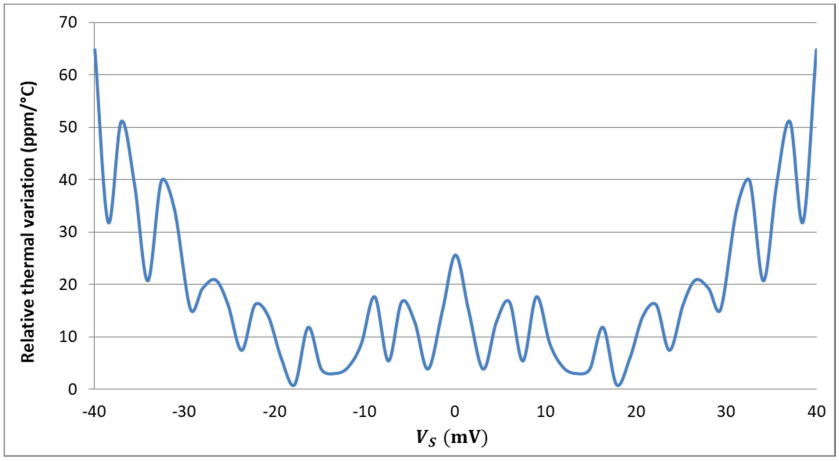


Figure 4.31: Measured relative thermal variation of the fabricated sensor interface over a reduced full scale.

4.6. Dynamic behaviour of the sensor interface

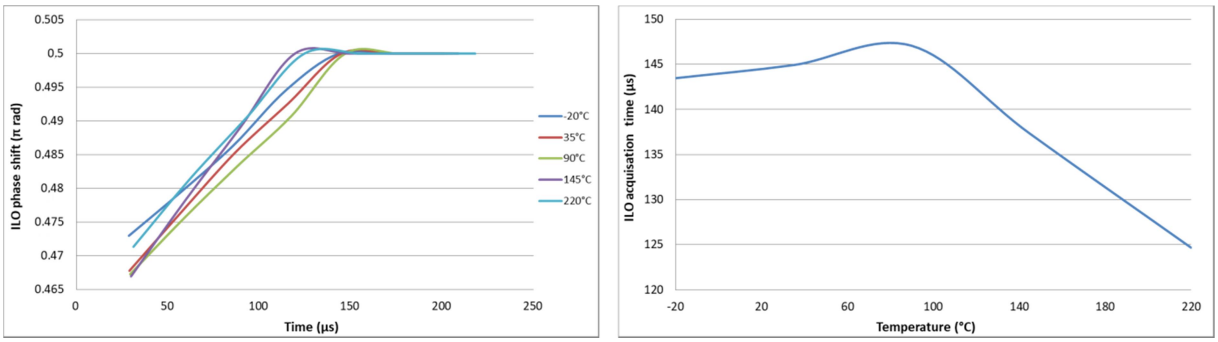
In the sensor interface, the TA, the counter and the ILOs may contribute to the dynamic behaviour of the circuit. Since the counter works at a high frequency rate (143MHz) and since the TA has a high bandwidth of about 790kHz, the dynamic behaviour of the fabricated sensor interface will be limited by the dynamic behaviour of the ILOs.

4.6.1. Dynamic behaviour of the ILOs

ILOs are intrinsically characterised by an acquisition time, T_{aq}, which is defined as the time required for the ILO to be locked on the locking signal and to acquire the phase shift corresponding to the sensor output voltage V_S. In other words, if the sensor output voltage V_S changes during this acquisition time (i.e., changes faster than the acquisition time), ILOs will not be able to track the variations of V_S and thus, the obtained phase shift will not match with the one corresponding to the dc input. To respect the Shannon criteria, the input voltage frequency must be two times lower than $1/T_{aq}$ so that the ILOs and hence the sensor interface would follow the variation of V_S and work correctly.

Figure 4.32 shows the simulation result of the ILO acquisition time over the operation temperature range. Figure 4.32.a depicts the ILO phase shift as a function of time, from which the acquisition time is extracted as a function of the temperature in figure 4.32.b.

The maximum acquisition time of the ILO, extracted from figure 4.23, is roughly equal to 150µs which is equivalent to a frequency of 6.6kHz ($1/T_{aq}$). Therefore, the maximum frequency of V_S that ensures a proper function over the entire operation range is around 3.3kHz.



(a) Phase shift of the ILO as a function of time. **(b) ILO acquisition time vs temperature.**

Figure 4.32: Simulated dynamic behaviour of the ILO.

4.6.2. Measured Bode Diagram of the sensor interface

Bode diagram of the fabricated sensor interface is plotted in figure 4.33 for different temperatures for an input voltage V_S with a peak-to-peak voltage of 50mV (f_{V_S} the frequency of the input voltage V_S).

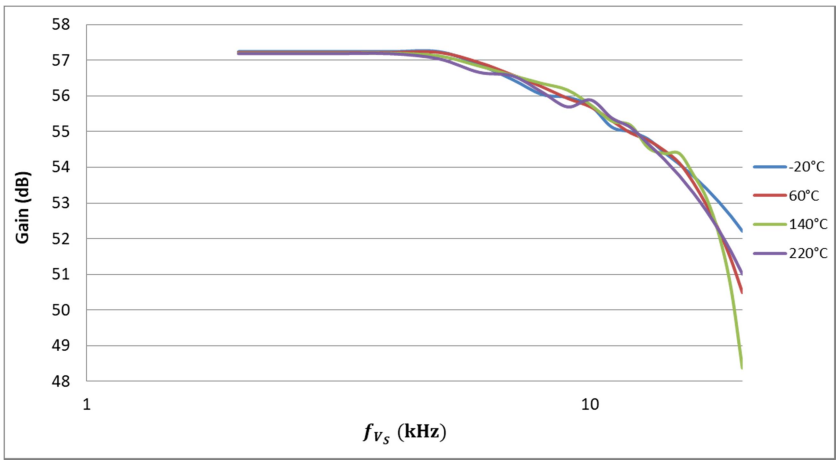


Figure 4.33: Bode diagram of the fabricated sensor interface over the operation temperature range.

Measurement shows that the circuit operates correctly until a 4kHz input frequency over the entire operation range. This zone is defined by the frequency range where the gain of the sensor interface is constant (i.e., 57.2dB).

This is consistent with the ILOs dynamic behaviour described previously. In fact, for an input frequency f_{V_S} lower than 4kHz, the output N of the sensor interface can follow perfectly the input voltage V_S.

Above this frequency (i.e., 4kHz), there is an error in the digital output N because of the ILO acquisition time; which is manifested by a gradual decrease in the bode diagram

curves. For temperatures ranging from -20°C up to 220°C, an average bandwidth of 14kHz is measured.

Figure 4.34 depicts the measured bandwidth of the sensor interface as a function of the temperature. This bandwidth is almost independent of the temperature.

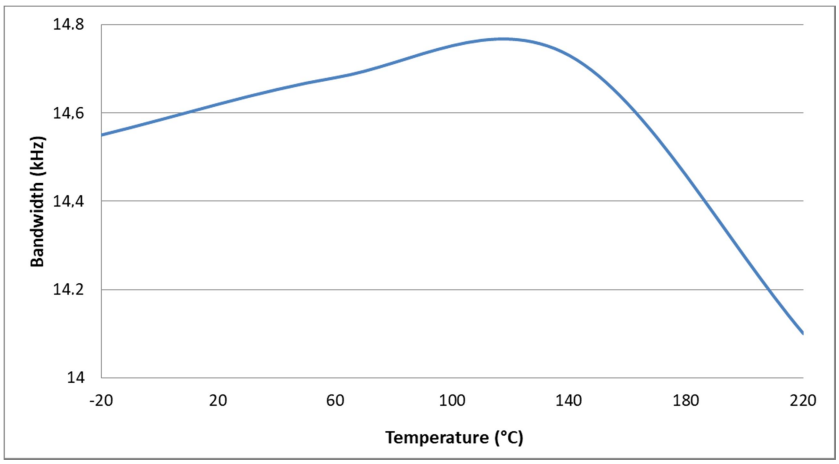


Figure 4.34: Measured bandwidth of the sensor interface as a function of the temperature.

4.7. Consumption of the sensor interface

Figure 4.35 depicts the power consumption of the sensor interface over the full temperature range. The maximum current is equal to 850µA which is equivalent to a maximum power consumption of 1.53mW (Vdd=1.8V).

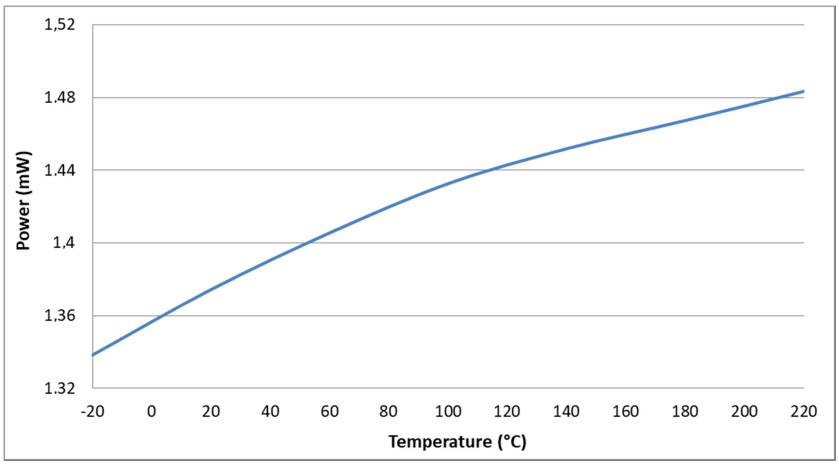


Figure 4.35: Measured power consumption of the fabricated sensor interface vs temperature.

Table 4 details the contribution of each constitutive block of the sensor interface to the overall power consumption. It gives their simulated values over the operation temperature range.

Table 4. Simulated power consumption of the sensor interface constitutive blocks.

Sensor interface constitute blocks	Power consumption (µW)	
	-20°C	220°C
Reference oscillator	2.5	8.2
ILO1[1]	1.5	6.4
ILO2[2]	1.7	6.4
TA	119.8	138.1
Bias block	228.8	305.1
Frequency divider	40.1	46.1
PLL	734.7	753.3
Counter	249.1	265.6

[1]the maximum power consumption is obtained at V_S= + 60mV
[2]the maximum power consumption is obtained at V_S= - 60mV

Among the sensor interface constitutive blocks, the PLL, the counter and the biasing block are the most consuming. The high power consumption of the biasing block is due, in addition to the multiple current mirrors, to the operational amplifiers and to the bandgap voltage reference (BGVR) that consume 66µW and 84µW respectively.

The high power consumption of the PLL and the counter is due to their high operation frequency (the power consumption is proportional to the frequency).

4.8. Conclusion

The sensor interface has been fabricated using a 0.18µm Partially Depleted-SOI technology with 1.8 V power supply. Measurement results show that the sensor interface has **a low temperature dependence over a wide temperature range** extended from -20°C up to 220°C (178ppm/°C over an input range of ±60mV and **65ppm/°C over an input range of ±40mV**).

Measurements showed that the sensor interface is able to interface sensors with a full scale of **±60mV**. Moreover, the fabricated sensor interface has **a bandwidth around 14kHz**.

Overall performances are generally **in agreement with that obtained by simulations and meet the system specifications**. Several discrepancies between measured and simulated performances (residual temperature dependence, offset, higher non-linearity, and reduced full scale) have been explained by process variations and mismatches. Using **devices with larger dimensions** would be efficient to ameliorate the sensor interface performances.

Table 5 summarizes the performances of the sensor interface compared to previous similar works. It shows that the presented sensor interface achieves good performances.

Table 5. Performances of the sensor interface.

Performances	This work	Smedt et al. 2013	Gläser et al. 2017	De Smedt et al. 2012	Portmann et al. 2002	Grezaud et al. 2017
Temperature range (°C)	-40 to 250 (Sim.) -20 to 220 (Meas.)	-20 to 100 (Meas.)	0 to 300 (Meas.)	-40 to 120 (Sim.)	25 to 300 (Meas.)	-40 to 180 (Meas.)
Thermal drift	38ppm/°C (Sim.) 65ppm/°C (Meas.)[1] 178ppm/°C (Meas.)[2]	79ppm/°C	±1.3%FS (±43ppm/°C)	N.A	±4% of FS (±123ppm/°C)	N.A
Sensor type	resistive	resistive	resistive	resistive	magnetic	resistive
Non-linearity	5.79%FS (Meas.)[1] 1.43%FS (Meas.)[2]	0.7%	N.A	0.19%	N.A	N.A
Consumption	1.38mW at -20°C 1.53mW at 220°C	18 µA	N.A	96µW	4.5 mA	34µA
Resolution	11 bit for the output +1 bit for the V_S sign	N.A	N.A	9 bit	8 bit	10 bit
Maximum input frequency	4kHz	N.A	N.A	N.A	N.A	N.A
Size	1860.1x1885.9(µm^2) 0.21mm^2 (active)	550x300 (µm^2) 95x95(µm^2) (active)	N.A	N.A	3.3 x 1.7(mm^2)	4.25x4.25(mm^2)
Technology	180nm HT SOI Vdd :1.8V	40 nm CMOS Vdd : 1V	N.A	130 nm CMOS Vdd : 1.2V	1 µm CMOS Vdd : 5V	180nm HT SOI Vdd :1.8V

[1]Measurements over a full scale of ±60mV.

[2]Measurements over a full scale of ±40mV.

4.9. References

De Smedt, Valentijn, Georges Gielen, and Wim Dehaene. 2012. "A Novel, Highly Linear, Voltage and Temperature Independent Sensor Interface Using Pulse Width Modulation." *Procedia Engineering*, 26th European Conference on Solid-State Transducers, EUROSENSOR 2012, 47 (Supplement C): 1215–18. https://doi.org/10.1016/j.proeng.2012.09.371.

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Grezaud, R., L. Sibeud, F. Lepin, J. Willemin, J. C. Riou, and B. Gomez. 2017. "A Robust and Versatile, -40°C to 180°C, 8Sps to 1kSps, Multi Power Source Wireless Sensor System for Aeronautic Applications." In *2017 Symposium on VLSI Circuits*, C310–11. https://doi.org/10.23919/VLSIC.2017.8008520.

Portmann, L., H. Ballan, and M. Declercq. 2002. "A SOI CMOS Hall Effect Sensor Architecture for High Temperature Applications (up to 300 °C)." In *Proceedings of IEEE Sensors*, 2:1401–6 vol.2. https://doi.org/10.1109/ICSENS.2002.1037326.

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Conclusion and Future Works

Conclusion

The context of this thesis is related to the domain of sensor interfaces for harsh environments, particularly sensor interfaces for high temperature environment. High temperature sensing systems are exhibiting a continuous market growth in many applications (automotive, aeronautic and oil and gas applications). Therefore, developing high temperature sensor interfaces is getting more and more crucial.

For the benefit of the Signal to Noise Ratio, the sensor interface must be put as close as possible to the sensor. Hence, the sensor interface electronics are exposed to high temperature environment.

Temperature affects the parameters of CMOS technology; this degrades the performances of integrated sensor interfaces. Thus, the sensor interface electronics must be designed in a way to mitigate the effect of temperature variations. This issue was the subject of the research presented in this work.

The objective of this thesis was to design an integrated sensor interface for high temperature applications, it must be able to sustain high temperature operation condition and to work under a wide operation temperature range.

In chapter 2, the principle of the high temperature sensor interface was proposed. Chapter 3 detailes the architecture of the high temperature sensor interface using relaxation ILOs (RILOs). RILOs were chosen for their extended linearity range compared to typical ILOs. In chapter 4, experimental results of the fabricated sensor interface were presented as a proof of concept of the low temperature dependence of the sensor interface.

The sensor interface has a fully differential time-domain architecture. Differential architecture offers good immunity against process variations and against common mode noise. Time Domain architecture leads to quasi-digital circuits which are known to have a good robustness against temperature variations compared to analog based sensor interfaces.

The Time Domain architecture of the sensor interface is based on the use of Injection Locked Oscillators (ILOs) as phase shifters. Indeed, it is based on converting the sensor output signal into a Pulse Width Modulated signal.

The sensor interface is designed to interface resistive sensors, typically Wheatstone bridge sensors. It converts the sensor output voltage into a phase shift difference which is converted into a digital signal by means of a Time –to- Digital Converter.

The sensor interface is designed so that the digital output is a ratio of the circuit parameters. This makes the sensor interface achieve a low temperature dependence.

A proof-of-concept has been implemented using a 0.18µm Partially-Depleted SOI technology because of its higher robustness against temperature variations compared to CMOS bulk technologies.

In order to demonstrate the low temperature dependence of the sensor interface, this latter is simulated over a temperature range from -40°C to 250°C and its prototype is characterised over a temperature range from -20°C to 220°C (due to the limitations of the characterisation bench).

Simulations and experimental results show that the sensor interface achieves an excellent temperature stability over a wide temperature range. In simulations, the value of the maximum relative thermal variation is of 34ppm/°C over a temperature range extending from -40°C to 250°C. The relative thermal variation of the fabricated sensor interface, over a temperature range extended from -20°C to 220°C, is always below 178ppm/°C for an input full scale of ±60mV and below 65ppm/°C for an input full scale of ±40mV.

Measured relative thermal variation is higher than that obtained by simulations. The residual temperature dependence is explained by process variations and mismatches. The use of larger area devices should reduce this effect and thus the obtaining of further improved performances.

Static characterisation shows that, over the operation temperature range extended from -20°C to 220°C, the sensor interface is able to interface sensors with a full scale of ±60mV which is a consistent range with large numbers of sensors.

Dynamic characterisation shows that the fabricated sensor interface has a bandwidth of 14kHz over an operation temperature range from -20°C to 220°C. This means that the sensor interface is adapted to low bandwidth applications which are typically industrial monitoring applications.

The measured maximum non-linearity over a -20°C to 220°C temperature range is equal to 6% of the output full scale over an input full scale of ±60mV and equal to 1.5% of the output full scale over an input full scale of ±40mV.

The total power consumption of the sensor interface is 1.4mW at -20°C and 1.5mW at 220°C.

It can be concluded that the sensor interface achieves the initially defined objectives. The sensor interface has an excellent temperature stability over a wide temperature range. The obtained result (65ppm/°C for an input range of ±40mV) is, to our knowledge, the lower thermal drift ever reported for a 11 bit resolution. For the initially input range of ±60mV, the performance degrades both in terms of linearity and temperature stability.

Future works: Prospects

The presented work opens many prospects. Main possible future works are summarized.

1. The sensor is designed for resistive sensors but it can be used with any other type of sensors. The principle of the high temperature sensor interface remains the same, which is to convert the sensor output signal into a free running frequency of the ILO in order to obtain a phase shift function of the sensor output signal.

However, if capacitive sensors are considered, the sensor interface is limited by the non-linearity of the ILO free running oscillation frequency ($f_0 = I_0/(2C_{sensor}V_{th})$; where C_{sensor} represents the sensor capacitance).

2. Measurements show that the sensor interface suffers from reduced full scale compared to specifications which is due to the fact that the full scale of the phase shift difference is lower than π. This makes the sensor interface not take advantage of its entire full scale. It has been shown that this is caused by the mismatch between the locking frequency f_{lock} and the free running oscillation frequency at zero input voltage $f_{0(Vs=0)}$.

An auto-calibration loop can be used to ensure the equality between f_{lock} and $f_{0(Vs=0)}$. This auto-calibration loop detects the difference between the common mode of the two ILOs phase shifts (i.e., $(\Phi_{ILO1}+\Phi_{ILO2})/2$, which represents the phase shift of both ILOs at zero input voltage $\Phi_{ILO(Vs=0)}$) and π/2. This difference, which is proportional to the difference between $f_{0(Vs=0)}$ and f_{lock}., is converted into a current that is added to or subtracted from the ILOs bias currents. This acts on the free running oscillation frequency at zero input voltage of both ILOs identically in order to make them equal to the locking frequency.

The calibration loop shifts the two ILOs phase shifts Φ_{ILO1} and Φ_{ILO2} similarly in a point where their common mode (i.e., $(\Phi_{ILO1}+\Phi_{ILO2})/2$ which is equal to the ILOs phase shifts at zero V_S) is equal to π/2. Figure 5.1 simplifies the principle of the auto-calibration loop.

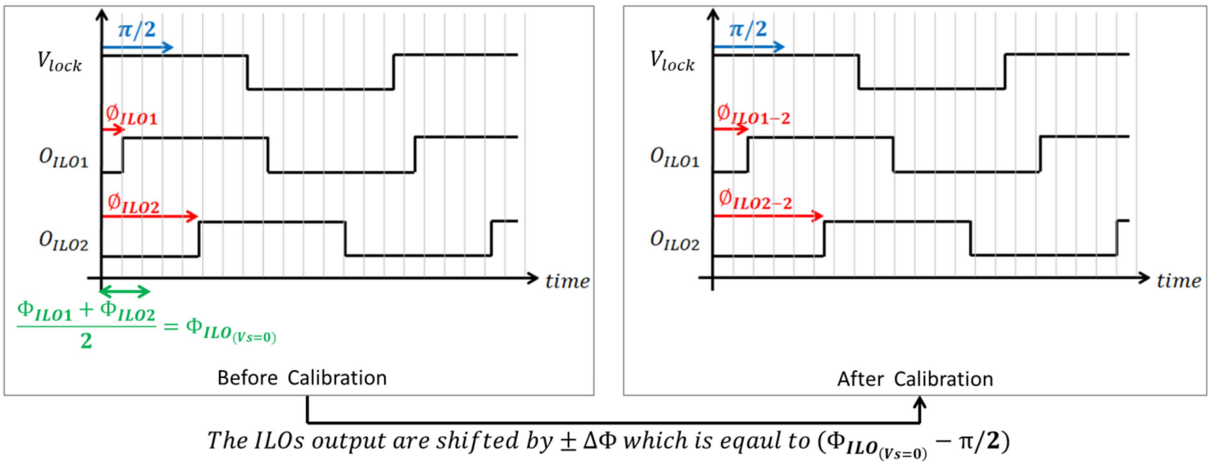

Figure 5. 1: Principle of the auto-calibration loop.

Thanks to the auto-calibration loop, the constraint of using the same topology for the reference oscillator and the ILO free running oscillator (whose goal is to ensure the quality between $f_{0(Vs=0)}$ and f_{lock}) is no longer a must. This leaves more freedom in the choice of topology of the reference oscillator.

3. According to the application, other than the thermal stability, the low power consumption could be a very important criterion especially in autonomous commutating node sensors.

Since the PLL and the counter are the most consuming blocks, two options can be considered in order to reduce power consumption.

a. Replace the counter-based time-to-digital converter by a low power new generation time-to-digital converter.

b. Remove the PLL. Then, the reference oscillator must be replaced by a high frequency oscillator running at 4096 times the locking frequency f_{lock} (this choice aims to obtain a 11 bit resolution) and having another topology than that of the reference oscillator. Indeed, if the currently used reference oscillator must run at 143.36MHz (f_{lock} = 35kHz), it must be polarized with 179µA which is not feasible.

Then, only digital divider, which has a low power consumption, is then required to generate the locking frequency from the reference high frequency oscillator (i.e., 143.36MHz).

4. Reliability and long term thermal stability of high temperature sensor interfaces is an essential criterion. In the characterisation of the fabricated sensor interface, tests were performed only on short duration. Testing the sensor interface during longer test time (>few hundreds of hours) would be interesting to perform in order to study the stability of the circuit performances over time and the reliability of the sensor interface in the high temperature environment.

List of Publications

International patent

- Emna Chabchoub, Franck Badets “Sensor interface for harsh environment”, Patent N°: 17196830.8-1568

International journal

- Chabchoub, E.; Badets, F.; Mailly, F.; Nouet, P.; Masmoudi, M; “A Temperature-Hardened Sensor Interface with a 12-Bit Digital Output Using a Novel Pulse Width Modulation Technique”, Sensors, 2018, doi:10.3390/s18041107.

International conferences (with acts)

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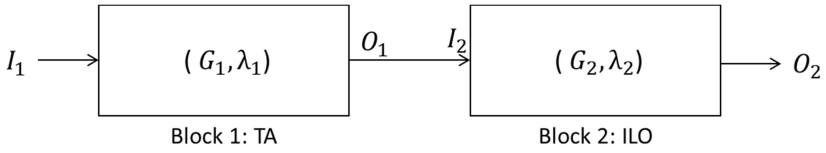
Appendix A: Demonstration of The Equation of The Sensor Interface INL

Considering a system constituted of two non-linear blocks (Figure below). Each block is characterised by a gain G and a non-linearity coefficient λ.

Here the system is indeed, the sensor interface. The two blocks are the transconductance amplifier (TA) and the injection locked oscillator (ILO).



In order to express the INL of the sensor interface, let's first express the INL of each block.

The output of the first block, the TA, is given by:

$$O_1 = \left(I_1 + \lambda_1 {I_1}^2\right) G_1 \quad (A.1)$$

The INL is defined as the difference between the output of the block and the linear fit, divided by the linear fit:

$$INL_1 = \frac{O_1 - G_1 I_1}{G_1 I_1} \quad (A.2)$$

Then, the INL of the first block (i.e., the TA) is:

$$INL_1 = INL_{TA} = \frac{I_1 G_1 + \lambda_1 {I_1}^2 G_1 - G_1 I_1}{G_1 I_1} = \lambda_1 I_1 \quad (A.3)$$

By analogy, the INL of the second block (i.e., the ILO) is:

$$INL_1 = INL_{ILO} = \lambda_2 I_2 \quad (A.4)$$

Now, let's express the output of the system O_2 as a function of its input I_1:

$$O_2 = \left(I_2 + \lambda_2 {I_2}^2\right) G_2 = \left(O_1 + \lambda_2 {O_1}^2\right) G_2 \quad (A.5)$$

$$O_2 = O_1 \; G_2 + \lambda_2 {O_1}^2 G_2 \quad (A.6)$$

$$O_2 = G_2 \, G_1 I_1 + G_2 \, G_1 \lambda_1 {I_1}^2 + \lambda_2 \, G_2 \, {G_1}^2 {I_1}^2 (1 + \lambda_1 \, I_1)^2 \quad (A.7)$$

$$O_2 = G_2 \, G_1 I_1 + G_2 \, G_1 \lambda_1 {I_1}^2 + \lambda_2 \, G_2 \, {G_1}^2 {I_1}^2 \left[1 + 2 \, \lambda_1 \, I_1 + {\lambda_1}^2 {I_1}^2\right] \quad (A.8)$$

Neglecting the term ${\lambda_1}^2 {I_1}^2$, we can write the following:

$$O_2 = G_2 \, G_1 I_1 + G_2 \, G_1 \lambda_1 {I_1}^2 + \lambda_2 \, G_2 \, {G_1}^2 {I_1}^2 + 2 \, \lambda_1 \lambda_2 \, G_2 \, {G_1}^2 \, {I_1}^3 \quad (A.9)$$

$$O_2 = G_2 \, G_1 I_1 \left(1 + \lambda_1 \, I_1 + \lambda_2 G_1 I_1 + 2 \, \lambda_1 \lambda_2 G_1 \, {I_1}^2\right) \quad (A.10)$$

Therefore, the INL of the overall system (i.e., the sensor interface) is writing as following:

$$INL_{SI} = \frac{G_2 \, G_1 I_1 \left(1 + \lambda_1 \, I_1 + \lambda_2 G_1 I_1 + 2 \, \lambda_1 \lambda_2 G_1 \, {I_1}^2\right) - G_2 \, G_1 I_1}{G_2 \, G_1 I_1} \quad (A.11)$$

Hence,

$$INL_{SI} = \lambda_1 \, I_1 + \lambda_2 G_1 I_1 + 2 \, \lambda_1 \lambda_2 G_1 \, {I_1}^2 \quad (A.12)$$

By making the following approximation: $I_2 \approx G_1 I_1$, the previous expression is now:

$$INL_{SI} = \lambda_1 \, I_1 + \lambda_2 I_2 + 2 \, \lambda_1 I_1 \lambda_2 I_2 \quad (A.13)$$

Based on equations (A.3) and (4.4), the INL of the sensor interface is expressed as:

$$INL_{SI} = INL_1 + INL_2 + 2 \, INL_1 INL_2 \quad (A.14)$$

Finally, the sensor interface INL is a function of the TA and the ILO INLs as follows:

$$INL_{SI} = INL_{TA} + INL_{ILO} + 2 \, INL_{TA} INL_{ILO} \quad (A.15)$$