Integration of a 3.3 kW, AC/DC bidirectional converter using printed circuit board embedding technology

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Integration of a 3.3 kW, AC/DC Bidirectional Converter using Printed Circuit Board Embedding Technology

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Résumé

Introduction

Les énergies fossiles (Pétrole, Gaz naturel, Charbon) représentent 80 % des énergies consommées. Malheureusement pour l'environnement, elles sont les plus polluantes. Le remplacement actuel des énergies fossiles permet au marché de l'électronique de puissance de grandir d'année en année. De nombreuses applications sont présentes dans de nombreux domaines comme, par exemple, le transport (les voitures électriques, l'avion "plus électrique", le ferroviaire), l'énergie (les réseaux photovoltaïque ou éolien, réseau intelligent) ou l'informatique (téléphonie mobile, centre de données).

L'électronique de puissance permet d'adapter l'énergie électrique à son utilisation finale. L'adaptation de l'énergie électrique utilise des convertisseurs. En plus de respecter le volume, l'efficacité et la fiabilité imposés par le cahier des charges de chaque application, l'électronique de puissance doit aussi permettre de réduire sensiblement les coûts. La conception, l'implémentation et la fabrication d'un convertisseur sont des problèmes multi-physiques. Le convertisseur doit assurer le fonctionnement électrique du circuit, le support mécanique et le refroidissement des composants électroniques.

Le package utilisé par les nouveaux composants à grand gap est le facteur limitant. L'intégration des convertisseurs doit développer des méthodes d'interconnexion permettant d'éliminer ce package tout en gérer la complexité et le grand nombre d'interconnexion. La thermique doit aussi être prise en compte. L'objectif de la recherche sur l'intégration des convertisseurs est de repousser les limites imposées par un cahier des charges standard tout en assurant ces 3 fonctions principales.

L'intégration de plus composants électronique de puissance dans un seul système permet d'obtenir une réduction de volume, de poids, de coût tout en augmentant la fiabilité. Parmi les nombreuses techniques d'interconnexion, le circuit imprimé (PCB) est très mature industriellement et permet la fabrication collective. Sa fabrication et l'assemblage des composants peuvent aussi être automatisés.

Le PCB était principalement utilisé pour connecter électriquement les composants électroniques à travers leurs packages. Dans les recherches sur l'intégration des convertisseurs, le PCB est utilisé pour former le package de certains composants. Cette technique va être utilisée dans cette thèse. Le but est de généraliser cette technique à l'ensemble des composants de puissance ainsi que les composants de commande. Avec pour objectif final, la conception, la réalisation et la caractérisation d'un convertisseur utilisant cette méthode. Les avantages et les inconvénients pour chaque composant seront discutés.

Etat de l'art

Un circuit imprimé, aussi appelé carte électronique ou PCB, est un support permettant de maintenir et de relier électriquement des composants électroniques. Il est constitué d'un assemblage d'une ou plusieurs couches de cuivre séparées entre elles par un matériau isolant. Les couches de cuivre sont gravées par un procédé chimique pour obtenir un ensemble de pistes, terminées par des pastilles. Les pistes relient électriquement les différentes pastilles. Les pastilles, une fois perforées, établissent une liaison électrique, soit entre les composants soudés sur le circuit imprimé, soit entre les différentes couches de cuivre. Il existe des pastilles non perforées servant à souder d'autres composants (les composants montés en surface).

Les PCB sont des produits adaptés à chaque application. La conception demande un effort de design mais la fabrication et l'assemblage des composants peuvent être automatisés. La conception peut être simplifiée à l'aide de programme informatique (conception assistée par ordinateur pour l'électronique). La fabrication de PCB est peu coûteuse et rapide.

Les PCB peuvent être simple face, avec une seule couche de cuivre, double face, avec deux couches de cuivre, ou encore multicouches, avec au moins trois couches conductrices. Les PCB multicouches permettent une densité de composant plus importante en utilisant les couches internes pour les connexions électriques.

La fabrication des PCB présente de nombreux avantages. Une carte multicouche permet d'avoir beaucoup de couches pour les interconnexions avec des dimensions faibles adaptées aux composants électroniques. L'avantage principal est la maturité du procédé de fabrication à une échelle industrielle. Pour les applications d'électronique de puissance, le PCB a quelques désavantages comme l'épaisseur maximum des couches conductrices ($400\,\mu\mathrm{m}$ pour du standard) réduisant le courant maximum ainsi que la conductivité thermique des couches isolantes ($0.4\,\mathrm{W}/(\mathrm{m}\cdot\mathrm{K})$) augmentant la résistance thermique du système. La photographie d'un PCB avec des composants assemblés est présentée dans la figure 2.1.

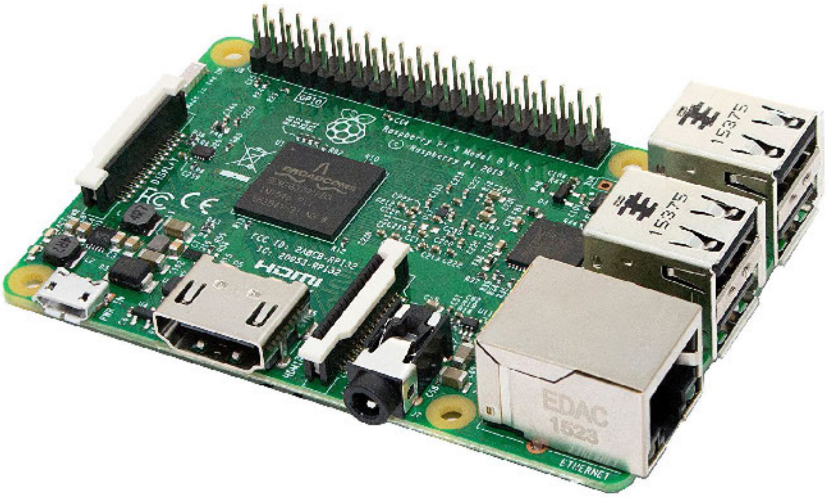


Figure 1: La photographie d'un PCB avec des composants assemblés [1].

Un PCB est composé de 2 types d'éléments: les couches de cuivre et les couches isolantes. Le seul paramètre d'une couche de cuivre est son épaisseur ($18\,\mu\mathrm{m}$, $35\,\mu\mathrm{m}$, $70\,\mu\mathrm{m}$ ou plus). Les couches isolantes sont constitués de prepregs. Ce sont des feuilles contenant des fibres imprégné de résine époxy partiellement polymérisée (B-stage). La polymérisation de la résine se fait pendant le procédé de fabrication d'un PCB. Les prepregs sont utilisées pour coller les couches de cuivre ou les couches isolantes entre elles. Il existe plusieurs épaisseurs, matériaux, structure et de pourcentage de résine pour les prepregs. Les couches isolantes à base de fibre de verre sont les plus utilisées dans l'industrie. Les couches isolantes à base de fibre de verre sont les plus utilisées dans l'industrie. Mais il existe d'autres matériaux comme l'aramid pour les applications haute fréquence. La fabrication de PCB utilise aussi des laminés qui sont des PCB simple ou double couches déja laminé. Les laminés permettent de simplifier l'assemblage de PCB multicouches.

Un large nombre d'étapes sont nécessaires pour la fabrication d'un PCB. La plupart des PCB utilise des étapes identiques. Le procédé de fabrication d'un PCB multicouches est présenté en figure 2.3.

La fabrication commence avec un laminé double face, un panneau avec deux couches de cuivre séparées par une couche isolante. Le panneau est dans un premier temps percé pour former les vias (Vertical Interconnect Access ou Accès d'Interconnexion Vertical en français) pour connecter les deux couches de cuivre. Pour obtenir la connexion électrique, du cuivre est électrodéposé. L'épaisseur de cuivre déposé dépend

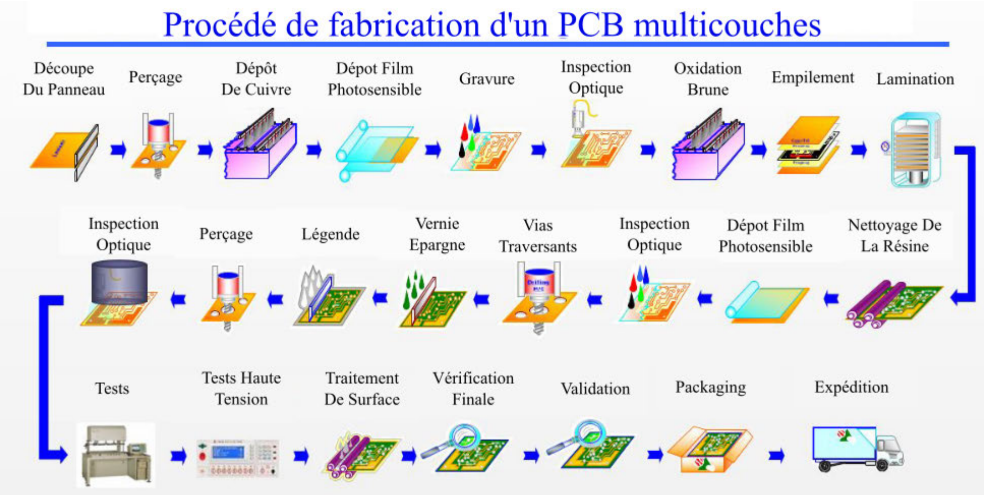


Figure 2: Procédé de fabrication d'un PCB multicouches [2].

de la durée pendant laquelle le panneau reste dans le bain chimique. Une fois les vias formés, le panneau est recouvert d'une couche photosensible. Cette couche photosensible est exposé à une lumière UV à travers un masque représentant les pistes de cuivre voulues (ou le négatif selon le type de couche photosensible). Le panneau est placé dans un bain chimique pour le développement. La partie non exposée (ou exposée) se dissout dans le bain chimique. Un autre bain chimique grave le cuivre qui n'est pu protéger par la couche photosensible. Des couches conductrices sont ensuite ajoutées grâce à des prepregs pour obtenir un multicouche. Le procédé est recommencé pour graver les nouvelles couches de cuivre.

Quand toutes les couches de cuivres sont gravées, un vernis épargne est déposé sur les surfaces externes du PCB. Ce vernie à seulement des ouvertures pour les connexions électriques avec les composants. Les connexions électriques sont protégées avec un traitement de surface. Le PCB est ensuite testé pour vérifier la fonctionnalité du circuit. Le circuit est testé pour vérifier les circuits ouverts ou les courts-circuits.

Les composants sont ensuite assemblés. Il y a deux types de technologies: les composants traversants et les composants montés en surface. Les composants traversants sont insérés dans des perçages à travers le PCB. Les pattes des composants sont soudées de l'autre côté. Les composants montés en surface sont directement placés et soudés sur les pastilles. L'avantage est l'utilisation d'une seule couche externe au contraire des composants traversants qui traverse l'ensemble des couches d'un PCB.

Ces deux méthodes d'interconnexion sont utilisées pour les composants discrets tout comme les circuits intégrés. Cependant pour les composants actifs, la puce est placée dans un package permettant l'assemblage avec un PCB. Ce package limite la performance des composants actifs à grand gap (exemples: SiC et GaN). Une nouvelle méthode d'interconnexion a été developpé pour se débarrasser du package et utiliser les nouveaux composants à leurs performances maximum. La nouvelle méthode d'interconnexion est l'enfouissement de puce (Die embedding en anglais). Cette nouvelle méthode consiste à enfouir la puce directement dans le PCB. Elle permet une meilleure miniaturisation, des performances électriques et thermiques améliorées.

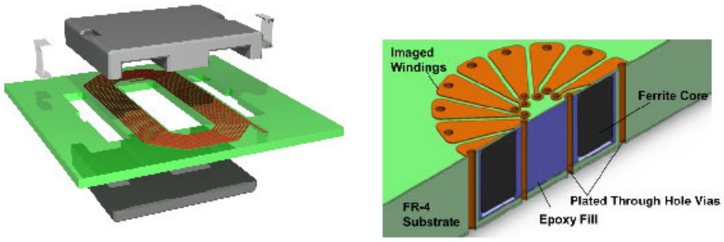
Avant le développement de cette technique, les fabricants de PCB ne manipulaient pas les composants électroniques. L'assemblage des composants est habituellement réalisé par des entreprises différentes que les fabricants de PCBs. Les fabricants de PCB ont développé chacun leurs méthodes dans la pratique pour réaliser l'enfouissement de puces. L'ensemble des solutions utilise 3 étapes similaires. La puce est dans un premier temps collée sur une couche de cuivre. L'ensemble est ensuite laminé avec des prepregs et une seconde couche de cuivre pour enfouir la puce. Ensuite des connections sont ajoutées sur la puce si nécessaire.

La première étape est le collage de la puce qui peut être fait avec une connexion conductrice ou non conductrice. Les connexions conductrices peuvent être réalisées avec une soudure, du frittage d'argent ou alors une pâte conductrice. Les connexions non conductrices sont réalisées avec de la colle ou un adhesive.

La puce collée sur la couche de cuivre est ensuite placé dans un empilement avec des prepregs découpés et des prepregs pleins. Les prepregs découpés sont utilisés pour compenser l'épaisseur de la puce. Les prepregs pleins sont utilisés pour l'isolation. Une couche de cuivre supérieure est ajoutée. L'empilement est laminé avec la puce au milieu. On obtient un PCB double face avec des puces enfouies.

Des connexions supplémentaires peuvent être nécessaires. En effet, les composants verticaux ont des pads de connexion sur le dessus et le dessous de la puce. Au contraire des composants latéraux qui n'ont que des pads de connexion sur une seule de leur face. Pour ajouter des connexions, le PCB est ouvert par perçage des couches sur le dessus des puces. Le perçage peut être mécanique (fraiseuse ou perceuse) ou être réalisé avec un laser. Dans tous les cas, les puces sont modifiées avec une épaisseur de cuivre supplémentaire pour compenser la tolérance du perçage. L'épaisseur supplémentaire est en cuivre car la connexion électrique est réalisée par un dépôt de cuivre électrolytique. Une fois la ou les puces connectées par ce dépôt, le PCB peut être utilisé comme un laminé dans un nouvel empilement pour obtenir un multicouche.

La méthode utilisée dans cette thèse utilise une couche non conductive avec un perçage laser des deux côtés de la puce. Elle permet d'orienter les puces de manière différentes les unes des autres. Les puces utilisées ont une surface avec un seul pad



(a) (b)

Figure 3: (a) Dessin d'une inductance "Planar". (b) Dessin d'une inductance "Toroidal Enfoui" [3].

et une autre surface avec trois pads. Avec cette méthode, la surface avec l'unique pad peut être placée vers le haut pour une puce et vers le bas. Cet avantage simplifie les connexions et réduit les éléments parasitic du circuit électrique. Les connexions réalisées ont une très bonne conductivité thermique.

Les composants magnétiques occupent une part importante du volume d'un convertisseur ($13\,\%$ in []). Ils sont des composants fabriqués sur mesure pour une application. Il y a un fort intérêt pour une technique permettant de réduire le volume de ces composants ou de simplifier leur fabrication.

Les composants "Planar" répondent partiellement à ces demandes (Figure 2.13). Le bobinage est réalisé à l'aide des couches de cuivre et vias d'un PCB. Le noyau magnétique est ensuite clipsé autour du PCB. Cependant, cette forme n'est pas totalement intégrée car le noyau magnétique dépasse du PCB obligeant à un usinage du radiateur pour le management thermique.

Des structures complètement enfouies permettent de résoudre ce problème (Figure 2.14). Cependant, les recherches sont principalement orientées vers les applications basses puissances ($1\text{-}100\,\mathrm{W}$). Dans ces structures, le noyau magnétique est enterré dans le PCB. Le bobinage est formé à l'aide des couches de cuivre et des vias du PCB. Les avantages de cette structure sont sa capacité thermique et sa capacité d'empilement. Cependant, les noyaux magnétiques sont des matériaux fragiles qui peuvent casser sous la pression appliquée pendant le procédé de fabrication du PCB. Il existe donc des recherches utilisant des matériaux classiques (fragile) mais aussi des matériaux conciliants (souple).

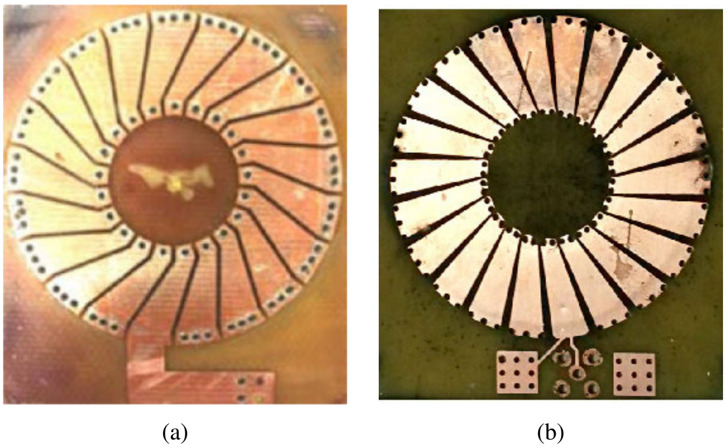
Plusieurs réalisations de prototype sont présentées dans la littérature. La publication [4] présente deux inductances couplées avec un noyau de ferrite enfouie dans du PCB. L'épaisseur du noyau magnétique est de $1.5\,\mathrm{mm}$. Le noyau à une forme plate permettant de résister à la pression mécanique. Mais le succès de l'enfouissement dépend grandement de la forme du matériau. Dans [4], un noyau magnétique de forme "Planar" est enfouie dans du PCB. Les deux prototypes réalisés présentent des cassures dans le matériau magnétique. Le premier essai n'avait pas assez de prepregs, la pression était directement appliquée sur le noyau magnétique. L'empilement du second essai avait plus de prepregs, la pression n'était plus directement sur le noyau magnétique mais il y avait toujours des cassures. Le choix de l'empilement pour l'enfouissement est critique et complexe.

Un noyau magnétique de ferrite de forme "Planar" a été enterré [5]. La méthode utilisée enterre séparément les deux noyaux magnétiques formant le "Planar". Puis les deux PCBs avec les noyaux enfouis sont assemblées. Elle n'est pas idéale car l'assemble a besoin de 3 laminations. Cette structure a été réalisée avec deux prepregs différents pour étudier l'impact des matériaux isolants. La structure avec un prepreg dont le CTE est proche de celui du matériau magnétique a passé 1000 tests thermique sans cassure du noyau magnétique ou délamination du PCB. La seconde structure avec un CTE plus éloigné de celui du matériau magnétique présente des cassures et des délaminations seulement après 150 cycles. Il est donc nécessaire de bien choisir les matériaux de l'empilement pour obtenir une structure fiable.

Au final, l'enfouissement de matériau magnétique est complexe car ce sont des matériaux fragiles. L'empilement doit être optimisé pour limiter la pression mécanique sur le matériau magnétique. De plus, les matériaux utilisés dans l'empilement doit être sélectionnés pour limiter les contraintes dues au fonctionnement. Des recherches ont été effectués avec un des matériaux plus conciliant. Ces matériaux magnétiques supportent plus facilement la pression.

Dans [6], une inductance enfouie utilise de fine plaques de ferrite (IBF15) (Figure 2.17a). Grâce à leur épaisseur, ces plaques de ferrite sont souples. La perméabilité relative du matériau est de 110 (contre 2000-3000 pour une ferrite classique). De plus, après la lamination, la perméabilité relative observée a baissé à 95. Une étude au microscope montre une dégradation du matériau. La pression mécanique sépare les fragments. Il y a donc une création d'un air-gap distribué réduit la perméabilité relative. La dégradation du matériau à cause de la lamination n'est pas encore parfaitement étudiée.

Une autre inductance enfouie est réalisée par enfouissement de poudre de MnZn ferrite directement dans le PCB (Figure 2.17b) [7]. Une cavité est formée dans un empilement de prepreg avec une couche de cuivre inférieure pleine. La poudre est placée dans la cavité. L'empilement est fermé par une couche de cuivre supérieure. Après lamination, la perméabilité relative obtenue est seulement de 24. Une observation d'une micro-section montre que la résine ne s'infiltre pas au centre de la poudre.



(a) (b)

Figure 4: (a) Photographie d'un prototype d'inductance utilisant des plaques de ferrites très fines [6]. (b) Prototype utilisant un noyau magnétique formé par l'enfouissement de poudre de ferrite directement dans le PCB [7].

Il n'y a donc pas de réduction de l'air-gap distribué ce qui explique la faible perméabilité relative.

Les matériaux magnétiques conciliants sont une alternative intéressante pour obtenir un composant enfoui sans une grande complexité dans la fabrication du PCB. Cependant, les performances de ces matériaux sont plus faibles que ceux des matériaux dits standards. Avec l'objective d'obtenir les meilleures performances, cette thèse se concentre sur la réalisation d'inductance utilisant l'enfouissement de large noyau magnétique standard.

En plus des composants actifs et magnétiques, de nombreux composants sont nécessaires pour réaliser un convertisseur de puissance (résistances, capacités, driver IC, ...). Ces composants sont enfouis dans le PCB avec les mêmes objectifs que les composants actifs. Un composant avec son package enterré dans le PCB est appelé composant "inséré" ("inserted component" en anglais). Un composant formé grâce à des couches spécifiques dans l'empilement du PCB est appelé composant "formé" ("formed components" en anglais).

Les composants formés peuvent être des résistances ou des capacités. Les résistances utilisent des couches résistances avec deux pads à chaque extrémité. Les capacités utilisent des couches capacitives placées au milieu de deux plans de cuivre. L'avantage principal des composants formés est de libérer la surface extérieure en remplaçant les composants montés en surface (Figure). Cette modification permet d'empiler les PCBs ou de rapprocher les composants pour obtenir un circuit avec moins d'éléments parasites.

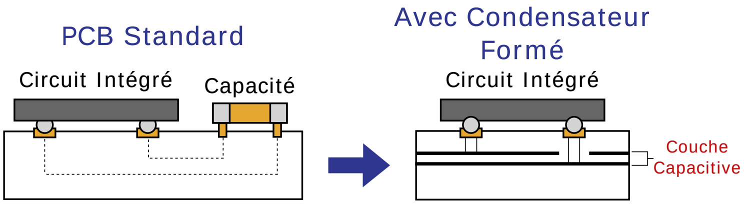


Figure 5: A gauche, un dessin d'un PCB standard avec les composants montés en surface. A droite, un dessin d'un PCB utilisant un condensateur formé avec le circuit intégré placé juste au-dessus [8].

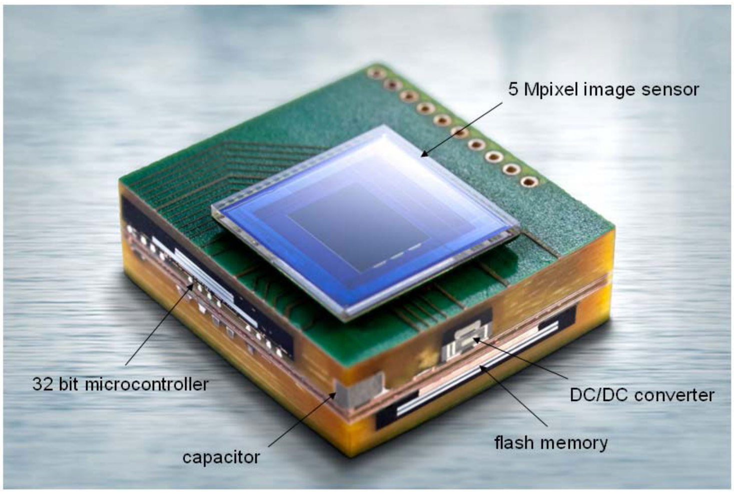


Figure 6: Vue en coupe de la caméra modulaire de Fraunhofer IZM avec 72 composants passifs enfouis[9].

Les composants insérés sont déjà utilisés dans certains smartphones. Cependant, les composants utilisés sont de petite taille (boitiers 0201, 0402, 0603). Un exemple de réalisation avec 72 composants insérés est présenté dans la figure 2.23. Ces tailles de boitier sont rarement utilisées en électronique de puissance à cause de leur valeur ou tenue en tension non adaptée.

Le procédé doit être adapté pour des tailles de boitier plus grandes. Cependant, les composants insérés vont être utilisés dans cette thèse parce qu'ils permettent d'obtenir les valeurs imposées par l'électronique de puissance. De plus, l'utilisation de composants formés utiliserait une trop grande surface pour atteindre ces valeurs.

Les convertisseurs de puissance ne transforment pas l'énergie électrique de manière parfaite. Une partie de l'énergie est perdue sous forme de chaleur. Cette énergie doit être évacuée pour obtenir un fonctionnement des composants à une température ac-

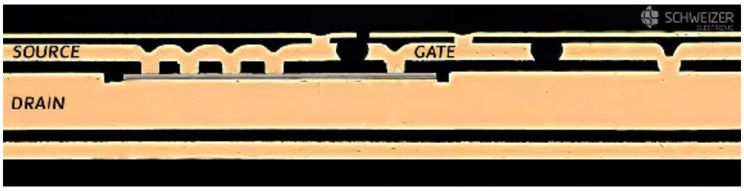


Figure 7: Vue en coupe d'un module utilisant la technologie PCB appelé p^2 Pack®(Schweizer). La puce est connectée en utilisant le frittage d'argent sur le cuivre épais. Les connexions supérieures sont réalisées à l'aide de microvias [10].

ceptable. Les transferts thermiques sont basés sur trois principes: la conduction, la convection et la radiation. La conduction est utilisée pour évacuer la chaleur depuis les composants jusqu'aux surfaces extérieures du PCB. Ensuite la convection et la radiation sont utilisées pour évacuer la chaleur dans l'environnement extérieur.

La conductivité thermique des couches isolantes du PCB est faible ($0.3\,\mathrm{W/(m\cdot K)}$) pour un matériau standard). Les recherches sont orientées vers l'augmentation de la conductivité thermique de ces matériaux. Il existe des matériaux avec des poudres céramiques donnant une conductivité thermique de $7\,\mathrm{W/(m\cdot K)}$. Cette valeur est encore très inférieure à la conductivité thermique du cuivre ($390\,\mathrm{W/(m\cdot K)}$). Une autre solution est le remplissage d'une zone avec des vias thermiques. Ces vias sont percés au laser et ensuite remplis de cuivre. La conductivité perpendiculaire aux couches grâce au vias thermique est d'environ $70\text{-}80\,\mathrm{W/(m\cdot K)}$ avec des règles de design standard. Une autre solution est enfouissement de couche de cuivre avec une épaisseur importante ($1\text{-}2\,\mathrm{mm}$). Cette couche de cuivre permet d'étaler la chaleur en plus acceptée un fort courant. Cette méthode est surtout utilisée pour les applications fortes puissances. Une découpe d'un module utilisant cette méthode est présentée dans la figure 2.24.

Une approche plus extrême est l'enfouissement de caloduc. Un caloduc est destiné à transporter la chaleur grâce au principe de changement de phase d'un fluide. Des caloducs utilisant la technologie PCB ont été développés dans [11]. Le prototype réalisé pour une puissance de $12\,\mathrm{W}$ donne une conductivité thermique équivalente de $4250\,\mathrm{W/(m\cdot K)}$. Cette conductivité thermique ne peut pas être comparée avec la conductivité thermique d'un solide car elles ne sont pas basées sur les mêmes principes physiques.

Les caloducs sont souvent sous la forme de tube. Cette forme n'est pas très adaptée aux PCBs qui ont une forme plate. L'amélioration du caloduc s'appelle "chambre de vapeur" ("vapour chamber" en anglais). Le fonctionnement est le même que le caloduc mais il est fabriqué pour avoir une forme 2D similaire au PCB. Une "chambre de vapeur" a été réalisé en PCB. Les performances sont encore impressionnantes. Le problème de ces deux systèmes est l' asséchement. Ce problème est dû à une trop grande puissance dissipée. C'est-à-dire quand le fluid est totalement à l'état de gaz et qu'il n'y a plus aucun transfert de chaleur.

Une fois la chaleur évacuée aux surfaces extérieures du système, elle doit être évacuée dans l'environnement alentour. Cette partie est réalisée grâce à la convection et à la radiation. Pour améliorer ces deux phénomènes physiques, un dissipateur est souvent ajouté au système. Le dissipateur augmente la surface d'échange entre l'extérieur et le système. Les dissipateurs classiques ont des ailettes droites. Cependant, il existe de nombreuses formes permettant d'améliorer un peu plus les performances. L'avantage des radiateurs à ailettes droites est qu'ils sont fabriqués par extrusion réduisant grandement leur prix. De plus ce sont des composants disponibles sur étagère. Les autres formes sont principalement conçues pour une application particulière.

Avec l'ajout d'un radiateur, il est nécessaire d'utiliser un matériau d'interface thermique. En effet, le contact entre deux surfaces rigides est séparé par des minuscules bulles d'air à cause de la rugosité des matériaux. Cet air crée une isolation thermique alors que l'objectif est que la chaleur soit conduite jusqu'au radiateur.

Les matériaux d'interface thermique ont une faible conductivité thermique. Les pâtes thermiques ont une conductivité thermique comprise entre 2 et $8\,\mathrm{W/(m\cdot K)}$. Il existe des matériaux d'interface thermique sous forme de feuille. Les performances sont souvent plus faibles ($1.8\,\mathrm{W/(m\cdot K)}$ pour Sil-Pad 1500ST de chez Bergquist). Mais ils sont beaucoup plus simple d'utilisation.

L'objectif de la thèse est de réaliser un convertisseur en utilisant la technologie PCB. Cette technologie va être orientée vers l'enfouissement des composants. L'enfouissement des composants actifs est déja maitrisé par les fabricants de PCB. Cependant, les composants magnétiques et annexes ne sont qu'au stade de recherche et seulement pour les faibles puissances. Dans ce projet, le management thermique est réalisé à l'aide d'un dissipateur utilisant la convection naturelle.

Design d'un convertisseur intégré

Le projet est séparé en 2 thèses "Topologie" et "Implémentation". La thèse décrite dans ce manuscrit correspond à la partie "Implémentation". La thèse "Topology" travaille sur le choix de la topologie du convertisseur et de son optimisation. Le projet est la réalisation d'un prototype d'un convertisseur AC/DC bidirectionnel. Ce type de convertisseur est utilisé, par exemple, comme chargeur de véhicule électrique.

Table 1: Cahier des charges du convertisseur AC/DC bidirectionnel.

$V_{IN_{RMS}}$(AC)	230 V
$I_{IN_{RMS}}$(AC)	15 A
V_{OUT}(DC)	400 V
I_{OUT}(DC)	12 A
P_{OUT}	3.3 kW
Volume	1 L
η	97 %
Temperature	−40 °C to 60 °C
C.E.M	EN55001 Classe B IEM conduite

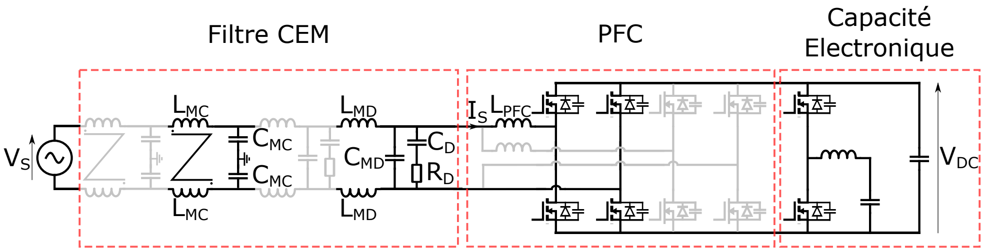


Figure 8: Schéma de la topologie choisie. La topologie utilise un filtre CEM, un PFC (Power Factor Corrector) et une "Capacité Electronique".

Le cahier des charges du convertisseur est présenté dans le tableau 3.1. L'objectif principal de ce projet est la densité de puissance qui doit être de 3.3 kW/L ce qui donne un volume total de 1 L pour l'enveloppement (La plus petite boîte rectangulaire dans lequel le convertisseur peut être placé).

La partie "Topologie" a comparé plusieurs topologies. Le résultat est l'utilisation d'un "Power Factor Corrector" (PFC) avec plusieurs cellules entrelacées. Un filtre CEM est placé du coté AC pour respecter la norme CEM (EN 55001 Classe B IEM conduite). Le filtre CEM est composé d'un filtre de mode commun et d'un filtre de mode différentiel. Ces deux parties peuvent être réalisées en utilisant plusieurs cellules. Du coté DC, une "Capacité Electronique" (PPB pour "Power Pulsating Buffer") est placée pour le filtrage du DC. Le schéma de la topologie est présenté en figure dans la figure 3.1.

La topologie est ensuite optimisée. L'optimisation est faite séparément pour la "Capacité Electronique" et le PFC avec le filtre CEM. En effet, la conception du PFC a un impact important sur le filtre CEM. L'impact de la "Capacité Electronique" sur les autres éléments est réduit. Son optimisation est donc séparée pour limiter la complexité de la procédure. Pour le PFC avec le filtre CEM, les paramètres de l'optimisation sont le nombre de cellules utilisé et la valeur des composants. Le volume et l'efficacité de chaque solution sont calculés. Le convertisseur avec le meilleur compromis entre son volume et son efficacité est considéré comme le convertisseur optimal. Le volume du convertisseur est calculé en sommant le volume de tous ces composants. Le volume du radiateur est calculé à partir des pertes totales en utilisant un coefficient de $5\,\mathrm{cm}^3/\mathrm{W}$.

La figure 3.2 présente la procédure d'optimisation pour le PFC et le filtre CEM. La procédure d'optimisation pour la "Capacité Electronique" est similaire.

Pour l'optimisation du PFC et du filtre CEM, les paramètres d'entrés sont le nombre de cellules entrelacées (N), la fréquence de commutation (f_{sw}), l'ondulation de courant haute fréquence (ΔI), le nombre d'étages pour le filtre de mode commun ($N_{f_{CM}}$) et le nombre d'étages pour le filtre de mode différentielle ($N_{f_{DM}}$). Avec une combinaison de paramètres, les formes d'onde du convertisseur sont calculées analytiquement. La première étape est le choix des interrupteurs. La deuxième étape est le choix des condensateurs pour le filtre CEM. Et finalement, les inductances pour le PFC et le filtre CEM sont optimisées.

Avec les formes d'onde du convertisseur, les pertes de chaque composant actif présent dans la base de données sont calculées. La puce avec le moins de pertes est le choix optimal. Avec l'utilisant de la technologie "Die Embedding", le volume des puces est considéré négligeable. A cause de la technique d'enfouissement, le nombre de puces disponibles dans la base de données est limité.

Les condensateurs du filtre CEM sont ensuite choisis. Pour le filtre de mode commun, la limite est imposée par le courant maximum à la terre acceptable ($3.5\,\mathrm{mA}$. La valeur de capacité maximale $C_{CM_{max}}$ est définie avec l'équation (3.3).

$$C_{CM_{max}} = \frac{I_{Terre_{Max}}}{V_{IN_{RMS}} \cdot \omega_{IN}} = 45.6\,\mathrm{nF} \tag{1}$$

avec $I_{Teere_{Max}}$ le courant maximum à la terre acceptable ($3.5\,\mathrm{mA}$), $V_{IN_{RMS}}$ la tension RMS du réseau ($230\,\mathrm{V}$) et ω_{IN} la pulsation du réseau ($50\,\mathrm{Hz} \times 2\pi$). Cette valeur de condensateur est distribué sur les différents étages de mode commun.

La capacité maximale pour le filtre de mode différentielle $C_{DM_{max}}$ est définie avec le facteur de puissance ($cos\phi$= 0.995) pour le pire cas, c'est-à-dire quand le convertisseur fonctionne à $10\,\%$ de sa puissance nominale ($P_{MIN} = 330\,\mathrm{W}$). C'est équivalent à une puissance réactive de Q_{max}= $33\,\mathrm{VAr}$. La capacité maximale est définie avec l'équation (3.4).

$$C_{DM_{max}} = \frac{Q_{max}}{V_{IN_{RMS}}^2 \cdot \omega_{IN}} = 2\,\mathrm{\mu F} \tag{2}$$

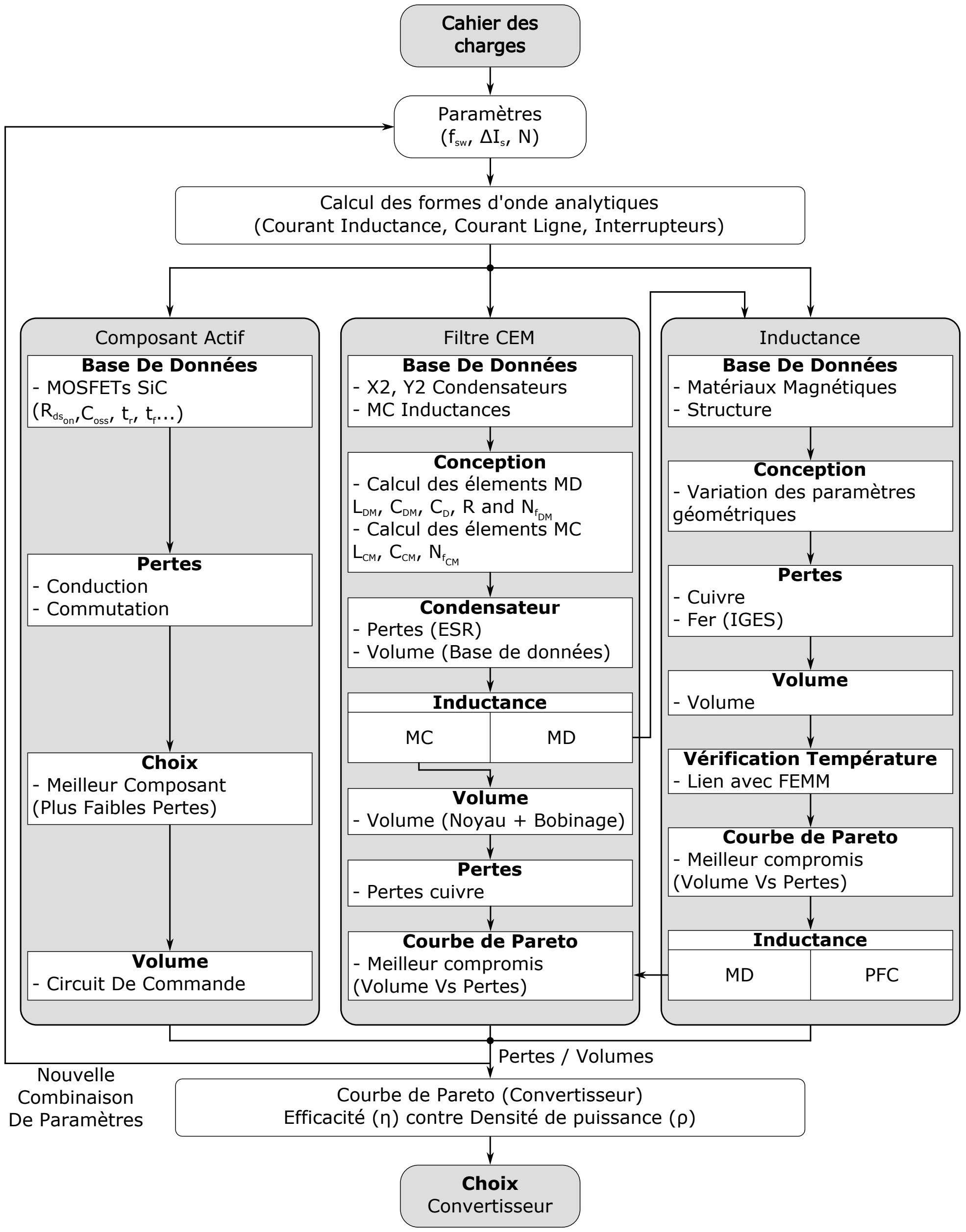


Figure 9: Procédure d'optimisation pour le PFC et le filtre CEM.

Table 2: Détails du PFC et du filtre CEM optimisés.

Données Générales	
η	$98.01\,\%$
ρ	$5.41\,\mathrm{kW/dm^3}$
N	4
f_{sw}	$180\,\mathrm{kHz}$
ΔI	$4\,\mathrm{A}$
Nb d'étages de filtre CEM	$N_{f_{DM}}$=4, $N_{f_{CM}}$=3
Volume	
Total	$609.5\,\mathrm{cm^3}$
Inductance PFC	$59.5\,\mathrm{cm^3}$
Filtre DM	$151.5\,\mathrm{cm^3}$
Filtre CM	$61.5\,\mathrm{cm^3}$
Interrupteurs et Commandes	$8\,\mathrm{cm^3}$
Dissipateur	$329\,\mathrm{cm^3}$
Pertes	
Totales	$66\,\mathrm{W}$
Inductance PFC	$33\,\mathrm{W}$
Interrupteurs	$17\,\mathrm{W}$
Filtre CEM (MC and MD)	$16\,\mathrm{W}$

Avec les valeurs maximales des condensateurs connues, l'atténuation requise est calculée en utilisant une FTT sur le modèle du LISN placé en amont du convertisseur (côté AC). Avec cette atténuation, la valeur des inductances est calculée avec l'équation (3).

$$L = \frac{1}{2} \cdot \sqrt[N_f]{\frac{10^{Att_{req}/20}}{(2\pi f_D)^{2N_f} \cdot \prod C}} \tag{3}$$

Les inductances pour le PFC et le filtre CEM de MD sont conçues dans la partie "Implementation" car elles utilisent la technologie PCB. La procédure d'optimisation de ces inductances est présentée en détail dans la suite.

Le tableau 3.2 présente les résultats obtenus pour la topologie optimisée du PFC et du filtre CEM. Le tableau 3.4 présente les résultats obtenus pour la topologie optimisée de la capacité électronique.

Table 3: Détails de la capacité électronique (PPB) optimisée.

General	
η	99.3 %
ρ	18.22 kW/dm^3
f_{sw}	140 kHz
L_{PPB}	20 µH
Tension Minimale	250 V
C_{PPB}	277 µF
Volume	
Total	181.1 cm^3
Inductance PPB	28.7 cm^3
Interrupteurs et Commandes	0.5 cm^3
Condensateur	36.4 cm^3
Dissipateur	115.5 cm^3
Pertes	
Totales	23.1 W
Inductance PPB	14.1 W
Interrupteurs	8.8 W
Condensateur	0.2 W

La conception des composants magnétiques est réalisée dans la partie "Implémentation". Ce sont des composants fabriqués sur mesure en utilisant la technologie PCB. Le volume des composants magnétiques est aussi dépendant de la thermique. Dans le but de limiter le volume des composants magnétiques une procédure d'optimisation a été réalisé pour les inductances. Cette procédure est utilisée pour les inductances du PFC, du filtre CEM de mode différentiel et de la "Capacité Electronique". La procédure d'optimisation pour les inductances est présenté dans la figure 3.7. Elle est incluse dans la procédure d'optimisation du convertisseur.

Les données d'entrée de la procédure sont la forme d'onde du courant et la valeur d'inductance requise provenant de la procédure d'optimisation du convertisseur. En plus, la forme de l'inductance ("Planar" ou "Toroidal Enfoui") étudiée est choisie. La dernière donnée est le matériau magnétique utilisé. Le matériau magnétique est défini par sa perméabilité relative, son induction à saturation et ces coefficients de Steinmetz (Ils sont utilisés pour calculer les pertes).

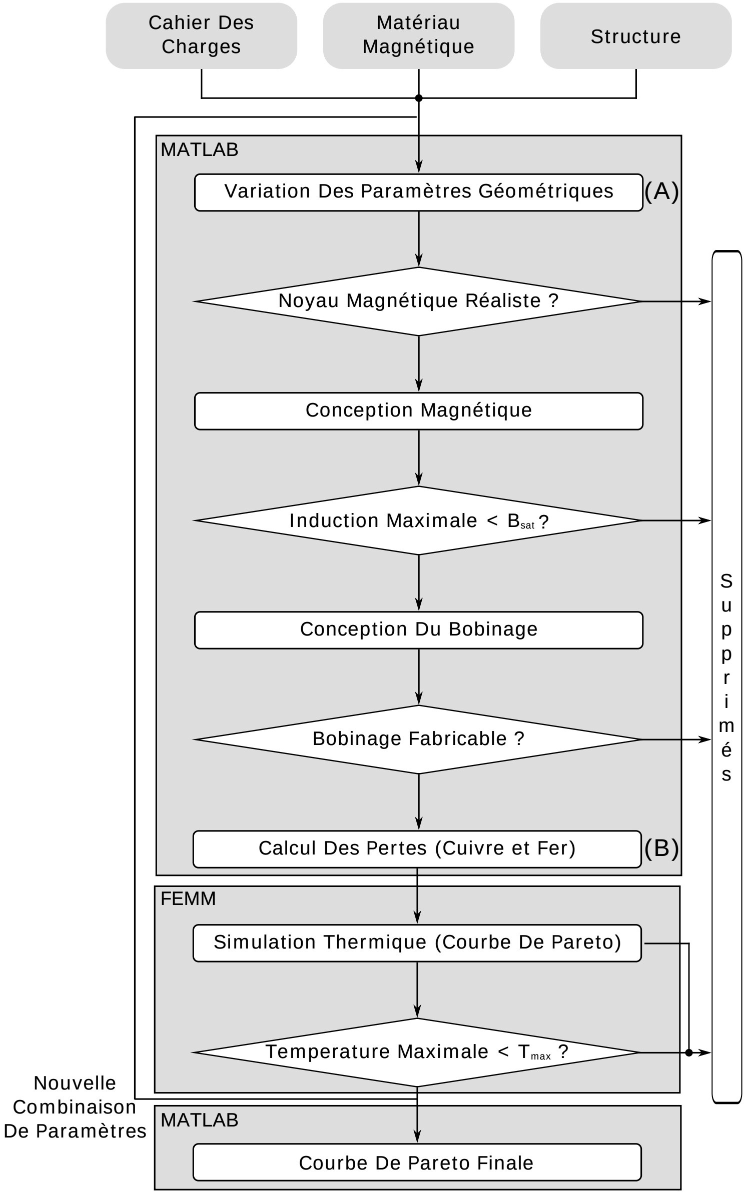


Figure 10: Procédure d'optimisation pour les inductances du filtre CEM de MD / PFC / de la "Capacité Electronique".

Chaque paramètre géométrique du noyau magnétique de la structure choisie varie depuis une limite basse à une limite haute avec un incrément constant. Une matrice avec toutes les combinaisons possibles est générée. Cette matrice représente tous les noyaux magnétiques, de différentes tailles, étudiés par la suite. Les noyaux magnétiques avec des dimensions impossibles (par exemple: un diamètre intérieur plus grand que le diamètre extérieur pour le "Toroidal Enfoui") sont supprimés.

La première étape est le calcul de la longueur magnétique et de la section magnétique pour chaque combinaison. Les solutions sont placées dans une matrice de mêmes dimensions que celle des noyaux magnétiques. Avec les résultats, le nombre de tour nécessaire et la longueur de l'air-gap pour obtenir la valeur d'inductance requise sont calculés.

Pour avoir une inductance constante pour tous les points de fonctionnement, il est décidé de rester dans la partie linéaire de la courbe BH du matériau magnétique. Il est donc vérifié que l'induction maximum reste inférieure à $70\,\%$ de l'induction à saturation. Les solutions qui ne respectent pas cette condition sont supprimées de la matrice.

Avec le nombre de tour nécessaire, la forme du bobinage peut être calculée. Les bobinages des deux structures choisies sont fabriqués à l'aide des pistes de cuivre et de vias du PCB. La forme du bobinage est calculée en utilisant les dimensions du noyau magnétique et les règles de design du PCB. Pour comparer les deux structures, les règles de design choisies sont standard. Elles peuvent être améliorées en discutant avec les fabricants de PCB pour un projet long terme. Avec certaine taille de noyau, il n'est pas possible de respecter le nombre de tour nécessaire et les règles de design (par exemple: la distance minimum entre 2 pistes). Ces solutions sont supprimées de la matrice.

Les solutions restantes sont définies par les dimensions de leur noyau magnétique et de leur bobinage. Elles respectent la valeur d'inductance avec une induction maximale acceptable. Ces inductances peuvent être fabriquées en respectant les règles de design des fabricants de PCB. Les pertes doivent maintenant être calculées.

Le calcul des pertes est séparé entre les pertes cuivre et les pertes fer. Les pertes fer sont calculées avec l'équation de Steinmetz généralisée et améliorée (iGSE). Le choix de cette équation correspond à la forme d'onde du courant dans les inductances qui est composé d'un sinus avec une fréquence de $50\,\mathrm{Hz}$ et d'un signal triangulaire à la fréquence de commutation qui est un paramètre d'optimisation du convertisseur. Le calcul des pertes avec cette équation permet de prendre en compte les pertes dues aux boucles mineures générées par la somme de ces deux signaux. Elle ne prend pas en compte les pertes dues à la composante continue, ce qui est acceptable car il n'y a pas de composante continue dans les inductances du PFC. L'iGSE est présentée dans

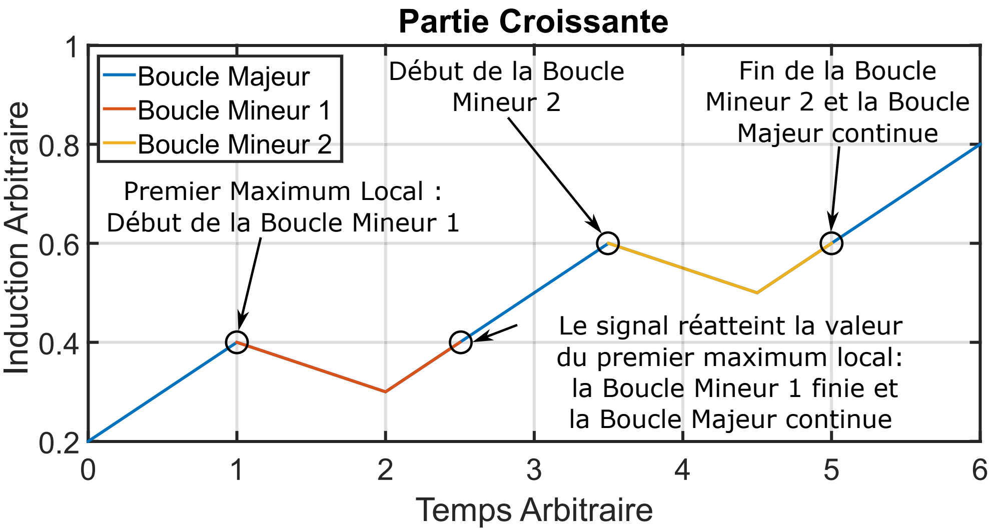


Figure 11: Forme d'onde arbitraire (Croissante) séparée en boucle majeure et boucles mineures pour le calcul des pertes fer. Les conditions de séparation sont inversées pour la partie décroissante.

l'équation (3.22).

$$P_{v_i} = \frac{1}{T}\int_0^T k_1 |\frac{dB}{dt}|^{\alpha} (\Delta B])^{\beta-\alpha} dt \tag{4}$$

avec:

$$k_1 = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{5}$$

avec (k, α, β) les coefficients de Steinmetz, B l'induction, T la période du signal, i l'indice de la boucle and P_{v_i} les pertes par unité de volume pour la boucle d'indice i.

Pour le calcul, la forme d'onde de l'induction sur une période est séparée en une boucle majeure et des boucles mineures. La séparation se fait d'abord sur la partie croissante du signal puis sur la partie décroissante. La séparation de la forme d'onde est expliquée dans la figure 3.10 pour la partie croissante du signal. Les conditions de séparation sont inversées pour la partie décroissante.

Les pertes fer totales P_{fer} sont obtenues en utilisant l'équation (3.24).

$$P_{fer} = \sum_i P_{v_i} \frac{T_i}{T} \tag{6}$$

avec T_i la période de la boucle d'indice i et T la période de la forme d'onde.

Il faut ensuite calculer les pertes cuivre. Le calcul est séparé pour les pertes dues au signal sinusoïdal de fréquence $50\,\text{Hz}$ et au signal triangulaire haute fréquence (Pertes AC). La résistance DC (R_{DC}) est calculée en utilisant la géométrie du bobinage avec la formule classique de $R_{DC} = \rho\frac{l_w}{S_w}$ avec l_w la longueur du bobinage et

S_w la section du bobinage. Les pertes cuivre DC P_{DC} sont ensuite calculées avec l'équation (3.26).

$$P_{DC} = R_{DC} \cdot I_{rms,BF}^2 \tag{7}$$

avec $I_{rms,BF}$ la valeur RMS de la sinusoïde de fréquence $50\,\mathrm{Hz}$ obtenue avec la procédure d'optimisation du convertisseur.

Le calcul des pertes AC est difficile à cause des effets de peau et de proximité dans les conducteurs. Pour obtenir une valeur précise de la résistance AC, la solution est de faire une simulation magnétique par éléments finis. Cette simulation est longue (plusieurs heures) ce qui n'est pas acceptable dans une procédure d'optimisation réalisant le design de nombreuses inductances. La solution choisie est de réaliser une unique simulation avec un design simplifiée est d'utiliser les valeurs obtenues pour toutes les solutions. Les valeurs obtenues pour le facteur K, défini comme R_{AC}/R_{DC}, en fonction de la fréquence sont données dans le tableau 3.6.

Table 4: Facteur K, R_{AC}/R_{DC}, utilisé pour le calcul des pertes cuivre haute fréquence.

Fréquence (kHz)	Facteur K
< 160	2.88
$160 - 200$	3.37
$200 - 240$	3.58
$240 - 280$	3.77
$280 - 320$	3.99
> 320	4.40

Les pertes cuivre AC P_{AC} sont ensuite calculées avec l'équation (8).

$$P_{AC} = R_{DC} \cdot K \cdot I_{rms,HF}^2 \tag{8}$$

avec $I_{rms,HF}$ la valeur RMS de l'ondulation haute fréquence obtenue avec la procédure d'optimisation du convertisseur.

Les pertes cuivre totales sont la somme des deux valeurs précédemment calculées. Ensuite la température maximale dans l'inductance doit être calculée pour éviter un composant non fonctionnel. La température maximale dans l'inductance permise est de $100\,^{\circ}\mathrm{C}$ ce qui correspond à la température utilisée pour les valeurs des coefficients Steinmetz utilisés. Le calcul de la température maximale est réalisé en utilisant une simulation par éléments finis avec le programme FEMM. Ces simulations sont automatiques avec une interface entre MATLAB (où est programmée la procédure

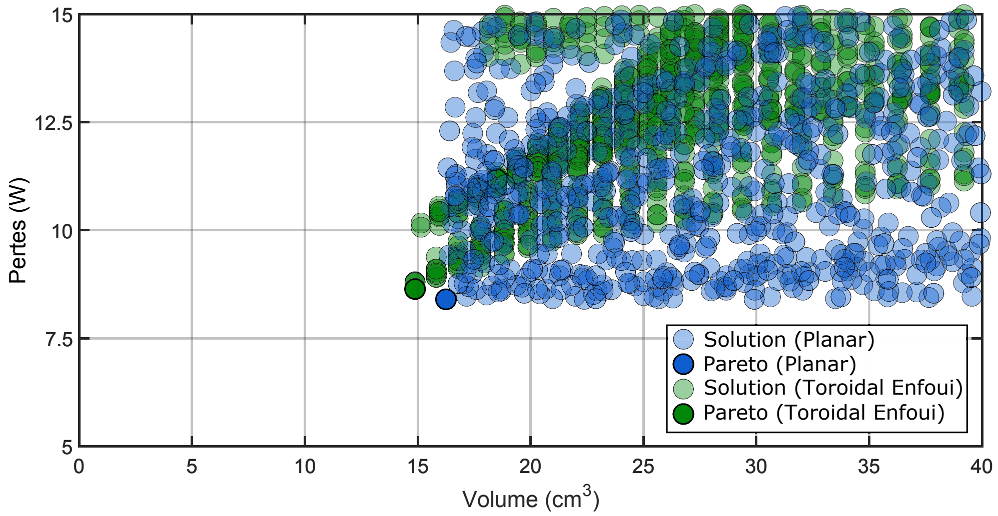


Figure 12: Résultats de la procédure d'optimisation d'inductance pour le PFC pour les deux structures, après que les solutions avec des températures trop élevées ont été supprimées.

d'optimisation) et FEMM. Ces simulations sont rapides (environ 1 s). Cependant pour réduire le temps de la procédure au maximum, les simulations ne sont effectuées que sur les meilleures solutions. Ces solutions sont celles qui présentent le meilleur compromis entre leur volume et leurs pertes. Elles forment sur la courbe de Pareto.

Après la première série de simulations, il y a deux possibilitées. Soit toutes les inductances sur la courbe de Pareto ont une température maximale inférieure à 100 °C alors la courbe de Pareto représente les meilleures solutions disponibles. Soit certaines inductances ont une température maximale trop élevée alors elles sont supprimées de la matrice. Une nouvelle courbe de Pareto est calculée et de nouvelles simulations thermiques sont réalisées jusqu'à obtenir une courbe de Pareto contentant seulement des solutions acceptables.

Les résultats de la procédure d'optimisation d'inductance pour le PFC sont présentées dans la figure 3.17 pour les deux structures d'inductance ("Planar" et "Toroidal Enfoui"). Ces résultats correspondent au PFC optimal utilisant 4 cellules entrelacées avec une fréquence de commutation de 180 kHz et un courant entrelacé avec une ondulation haute fréquence de 4 A d'amplitude. Les inductances utilisent des noyaux magnétiques de ferrite (N87 de chez EPCOS). Ces résultats sont présentés sous la forme d'un nuage de points dans lequel chaque point représente une inductance. La courbe de Pareto est surligné pour les deux structures.

Table 5: Résultat pour l'inductance "Planar" optimale.

Planar	
Pertes	$8.4\,\mathrm{W}$
Volume	$16.2\,\mathrm{cm}^3$
Temperature Maximale	$97\,^{\circ}\mathrm{C}$
Matériau Magnétique	Ferrite N97
Noyau Magnétique	ELP 32/6/20 & I 32/3/20
Nombre De Tour	11

Table 6: Résultat pour l'inductance "Toroidal Enfoui" optimale.

Toroidal Enfoui	
Pertes	$8.6\,\mathrm{W}$
Volume	$14.9\,\mathrm{cm}^3$
Temperature Maximale	$92\,^{\circ}\mathrm{C}$
Matériau Magnétique	Ferrite N87
Noyau Magnétique	R 63/38/3
Nombre De Tour	38

Pour la structure "Planar", il y a de nombreuses solutions supprimées pour des raisons thermiques. Au contraire, pour la structure "Toroidal Enfoui", il n'y a pas de solution supprimée à cause d'une température trop élevée. On peut conclure que les considérations thermiques ne sont pas limitantes pour cette structure. Elle a un meilleur aspect thermique grâce à sa grande surface en contact avec le dissipateur. Cette structure permet d'avoir une plus grande liberté sur la gestion thermique du convertisseur. Le facteur dimensionnant pour le "Toroidal Enfoui" est la conception du PCB. En effet, un nombre maximum de tour est réalisable à cause de l'écartement nécessaire entre les vias et l'espace disponible à l'intérieur du noyau magnétique. De plus, l'épaisseur du noyau magnétique est limitée à $3\,\mathrm{mm}$ à cause de l'épaisseur maximale du PCB. Toutes les meilleures solutions utilisent cette épaisseur maximale car elle se rapproche le plus d'une section magnétique carrée qui représente l'optimale. Ces 2 limites imposent un grand diamètre extérieur qui limite le minimum box volume atteignable.

Les caractéristiques des meilleures inductances sont présentées dans le tableau 5 pour le "Planar" et dans le tableau 6 pour le "Toroidal Enfoui".

Les inductances ont des pertes similaires cependant le volume du "Toroidal Enfoui" est plus petit que celui du "Planar". Avec ces résultats, on obtient que le convertisseur avec le meilleur compromis entre efficacité et densité de puissance utilise la structure "Toroidal Enfoui". Cette structure présente un avantage avec sa capacité d'empilement grâce au fait que la thermique n'est pas le facteur limitant.

Implémentation d'un convertisseur intégré

Le travail d'implémentation est principalement orienté sur les cellules du PFC. L'optimisation de la capacité électronique a été réaliser seulement dans un deuxième temps. Le filtre CEM de mode différentiel utilise aussi des inductances "Toroidal Enfoui".

Une cellule de PFC est composé de trois PCB. Les trois PCBs ont une taille identique pour avoir un empilement formant un parallélépipède. Le premier PCB contient 4 puces enfouies. Le second contient les 2 circuits de commande. Le troisième PCB contient l'inductance. Le PCB le plus proche du dissipateur est le PCB contenant les puces à cause de l'évacuation de chaleur. Le PCB avec les circuits de commande est placé juste au-dessus pour limiter les éléments parasites du circuit électrique. Finalement, le PCB avec l'inductance est placé sur le dessus. Cet assemblage permet d'avoir les éléments séparés en cas de problème avec la fabrication. Avec cette configuration, l'air d'un convertisseur standard est remplacé par de la résine. Cette résine permet une meilleure conduction de la chaleur des composants jusqu'au dissipateur. L'objectif final de cet assemblage 3D est l'étude de faisabilité du procédé de fabrication pour chaque élément. Cet assemblage permet aussi d'étudier l'intérêt de l'enfouissement pour chaque composant. Les PCB sont conçues avec le logiciel Altium Designer.

La taille de la cellule du PFC est imposée par la taille de l'inductance. Chaque PCB est carré pour assurer leurs interconnexions. Cela permet aussi d'obtenir un faible volume pour l'enveloppe. L'assemblage est présenté dans la figure 4.1.

Un PCB multicouches peut être fabriqué en utilisé différent empilement. Le choix est fait selon les interconnexions entre couches de cuivre nécessaire. Les PCB sont fabriquées avec 2 panneaux. Le premier panneau contient les PCB avec les puces enfouies. Le deuxième panneau contient les PCB avec les circuits de commande et avec les inductances. Les 2 panneaux sont nécessaires car les épaisseurs des couches de cuivre et isolantes sont différentes. De plus, la méthode d'interconnexion des puces n'est pas compatible avec celle des composants utilisés dans le circuit de commande.

Le premier panneau est un PCB 4 couches avec les puces enfouies entre les couches 2 et 3. La couche supérieure est numérotée 1 alors que la couche inférieure est numérotée 4. La fabrication commence avec une couche de cuivre de 35 µm (Couche 3) sur laquelle les puces sont collées avec une colle non conductrice élec-

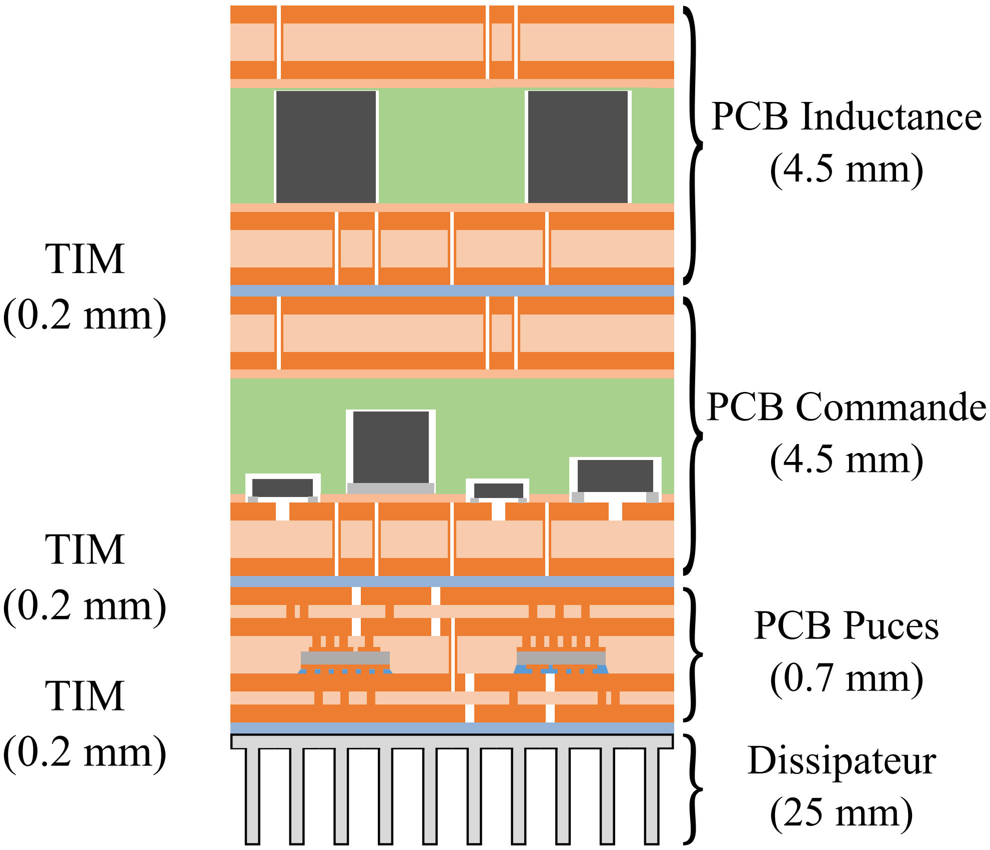


Figure 13: Assemblage 3D d'une cellule de PFC. L'épaisseur des PCB est exagérée par rapport à l'épaisseur du dissipateur.

triquement. Cet ensemble est placé dans un empilement avec la couche 2 qui a une épaisseur de 35 μm. La couche isolante est composée de prepregs découpés pour compenser l'épaisseur des puces et de prepregs plein pour l'isolation entre la couche 2 et les puces. Cet empilement est laminé pour former un ensemble solide. Les puces sont ensuite connectées à l'aide de microvias des deux côtés. Le positionnement des microvias doit être précis pour arriver sur les pads de connexion des puces. Après déposition du cuivre, l'épaisseur des 2 couches de cuivre est de 70 μm. Puis, les couches sont gravées.

Ensuite les couches 1 et 4 (35 μm) sont ajoutées avec l'aide de 2 prepregs de chaque côté. Les microvias sont percées et le cuivre est électrodéposé pour arriver à un PCB 4 couches de 70 μm. Puis, les couches sont gravées. Le procédé de fabrication est détaillé dans la figure 4.3.

Le second panneau est un PCB 4 couches avec les composants des circuits de commande et le noyau magnétique enfouis entre les couches 2 et 3. Le procédé de fabrication commence avec un laminé double couches de 70 μm. Les premières étapes sont similaires à celles d'un PCB standard. Les vias traversants sont percés mécaniquement. Du cuivre est électrodéposé pour obtenir la connexion entre les 2 couches. La couche de cuivre 3 est ensuite gravée.

Les composants sont assemblés sur la couche 3 à l'aide d'un four à braser. Les pads des composants sont seulement entourés d'une fine ligne de vernis épargne pour assurer une brasure propre. Ensuite l'entretoise utilisée pour enfouir les composants est assemblée à l'aide de deux prepregs. Le laminé supérieur qui est fabriqué de la même façon que le précédent mais qui n'a pas de composant en surface est assemblé avec deux autres prepregs au-dessus de l'entretoise. Les objectifs de l'entretoise sont de formées les cavités, de remplir les cavités de résine et d'empêcher le noyau magnétique de subir la pression mécanique du laminage. L'ensemble est percé pour réaliser les vias traversants, du cuivre est déposé puis les couches externes sont gravées. Le procédé de fabrication pour le second panneau est présenté dans la figure 4.7.

Avec l'objectif de connaitre les températures de fonctionnement des composants et de vérifier quelles sont acceptables, une étude thermique de l'empilement avec les 3 PCB est réalisée. Le dissipateur est dans un premier temps modélisé. L'empilement est ensuite modélisé dans une simulation avec éléments finis. Dans cette simulation, le dissipateur représenté uniquement par son coefficient de convection. Cette méthode permet de réduire le nombre de mailles.

Le modèle du dissipateur est basé sur une étude avec le logiciel Icepak (Mécanique des fluides dynamique). La géométrie du dissipateur est dessinée en 3D. Le dissipateur est placé dans un volume d'air dont les grandeurs sont 2 fois plus grandes que celles du dissipateur pour ne pas gêner le flux d'air. Les faces latérales du volume

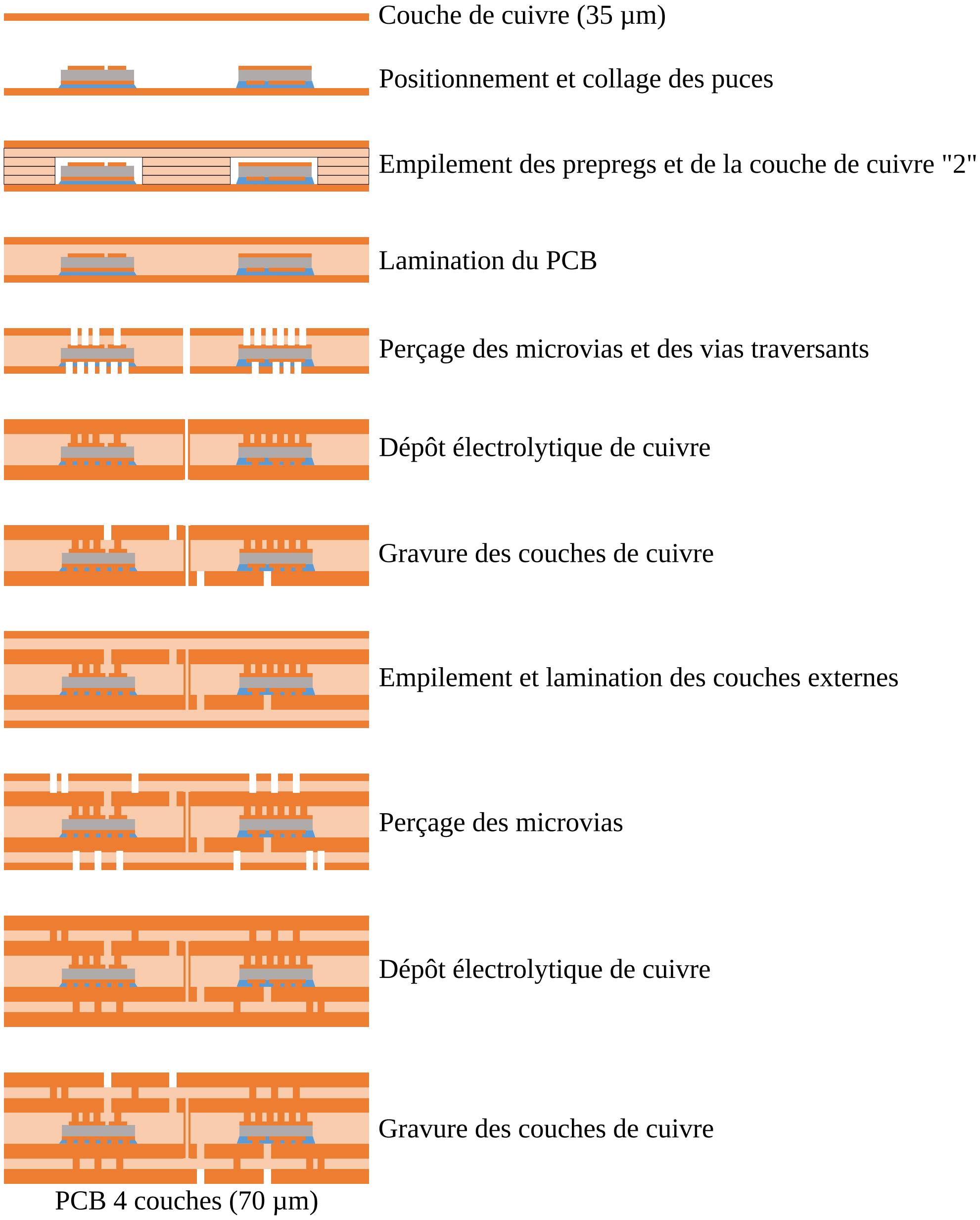


Figure 14: Procédé de fabrication pour le PCB avec les puces enfouies.

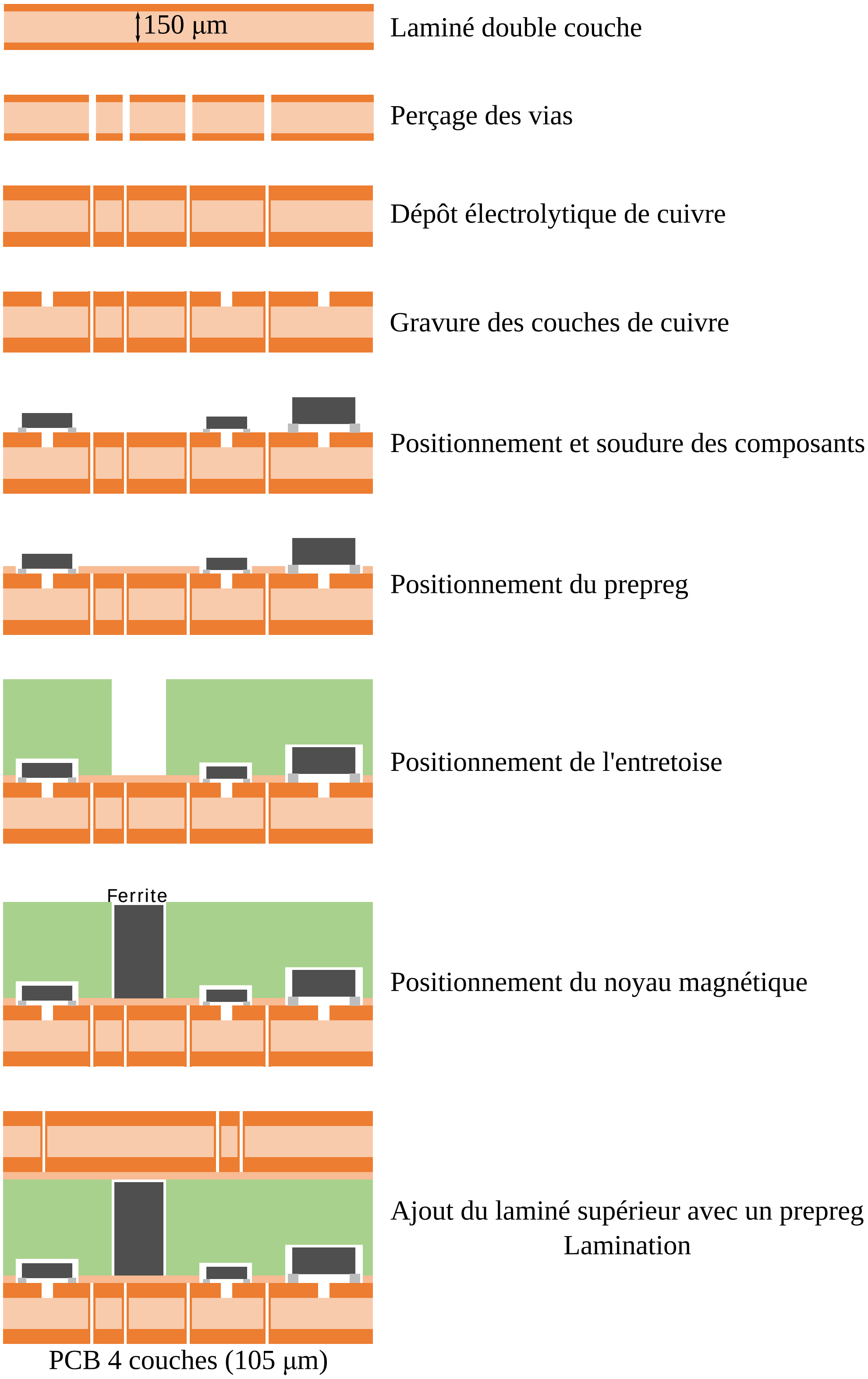


Figure 15: Procédé de fabrication du panneau de PCB avec les circuits de commande et les noyaux magnétiques enfouis.

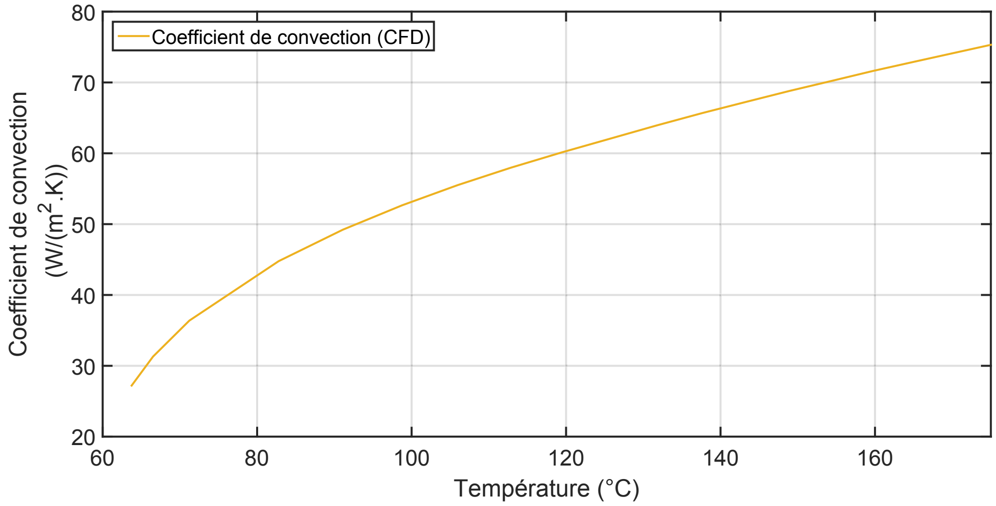


Figure 16: Coefficient de convection en fonction de la température du dissipateur.

d'air sont fermées, au contraire de la face supérieure et de la face inférieure. La gravité est appliquée dans le modèle. L'évacuation de chaleur par radiation est calculée en plus celle par convection. Des pertes sont appliquées sur le dessus de la semelle du dissipateur. La température ambiante est de $60\,°\mathrm{C}$. Les simulations sont réalisées pour des puissances de $1\,\mathrm{W}$ jusqu'à $50\,\mathrm{W}$. La température du dissipateur, considérée comme uniforme, est extraite pour chaque simulation. Le coefficient de convection h est calculé avec l'équation (4.15).

$$h = \frac{P}{S \cdot \Delta T} \tag{9}$$

avec P la puissance dissipée sur la semelle, S la surface supérieure de la semelle du dissipateur et ΔT la différence de température entre le dissipateur et l'ambiante. Le coefficient de convection en fonction de la température du dissipateur est présenté dans la figure 4.14.

Pour la simulation de l'empilement des 3 PCB, la simulation est réalisée avec le module transfert de chaleur dans les solides de COMSOL. La géométrie est importée depuis les fichiers créés directement par Altium Designer. La géométrie est simplifiée pour réduire le nombre d'éléments et de réduire le temps de résolution. Les pistes des circuits de commande et les vias associés sont enlevés. Les plans de cuivre sont gardés car ils permettent d'étaler la chaleur. Les TIM qui sépare chaque PCB est représentées. Le dissipateur est représenté par le coefficient de convection équivalent en surface inférieure de sa semelle. La condition aux limites de la surface supérieure à un coefficient de convection de $12\,\mathrm{W}/(\mathrm{m}^2 \cdot \mathrm{K})$ (Hypothèse pour une plaque horizontale).

Table 7: Températures obtenues pour les différents composants en simulation.

Nom	Géométrie Importée
Modèle du dissipateur	CFD
Puce HF	$128.2\,°\mathrm{C}$
Puce BF	$115.6\,°\mathrm{C}$
Magnetic Core	$125.5\,°\mathrm{C}$
RTD Puce HF	$121.3\,°\mathrm{C}$
RTD Puce BF	$116.2\,°\mathrm{C}$
RTD Extérieure Inductance	$118.9\,°\mathrm{C}$
RTD Intérieure Inductance	$119.1\,°\mathrm{C}$

Les températures obtenues pour les différents composants (puce haute fréquence, puce basse fréquence et noyau magnétique) ainsi que celles des capteurs de température (RTD P1000) enfouis dans le PCB de commande et de l'inductance sont présentées dans le tableau 4.2.

Les puces haute fréquence sont les points les plus chauds du convertisseur. Elles sont dans en dessous de la limite donnée par la datasheet (Température maximale de $175\,°\mathrm{C}$). Cependant, les pertes étaient calculées en utilisant les caractéristiques pour une température de $100\,°\mathrm{C}$. Cette observation est aussi vraie pour le matériau magnétique. Les composants des circuits de commande ont une température maximale de $125\,°\mathrm{C}$. La température maximale obtenue par simulation est de $121.3\,°\mathrm{C}$. Ce modèle sera vérifié avec une expérience thermique sur le prototype.

La procédure d'optimisation considère seulement les composants, les éléments parasites sont grossièrement estimés pour le design du filtre CEM de mode commun. Alors qu'ils ont un impact important sur les commutations des puces et le filtre CEM de mode commun. Les capacités parasites entre le $DC+$ et la terre ainsi que le $DC-$ et la terre ont un impact positif sur le filtrage du mode commun. Ces capacités ont été grossièrement estimées à une valeur de $10\,\mathrm{nF}$. Au contraire, les capacités parasites entre les points milieux et la terre ont un impact négatif sur le filtrage du mode commun. Ces capacités ont été grossièrement estimées à une valeur de $1\,\mathrm{nF}$. Les capacités parasites en parallèle de chaque interrupteur sont considérées nulles pour la première itération de la procédure d'optimisation.

La géométrie du PCB avec les puces enfouies est importées dans Q3D Extractor grâce au fichier ODB créé directement depuis Altium Designer. Le matériau d'interface thermique ainsi que la semelle du dissipateur, qui représente la terre, sont ajoutés en dessous du PCB. La simulation est ensuite réalisée à une fréquence de $500\,\mathrm{kHz}$. La fréquence n'a que peu d'impact sur la valeur des capacités parasites

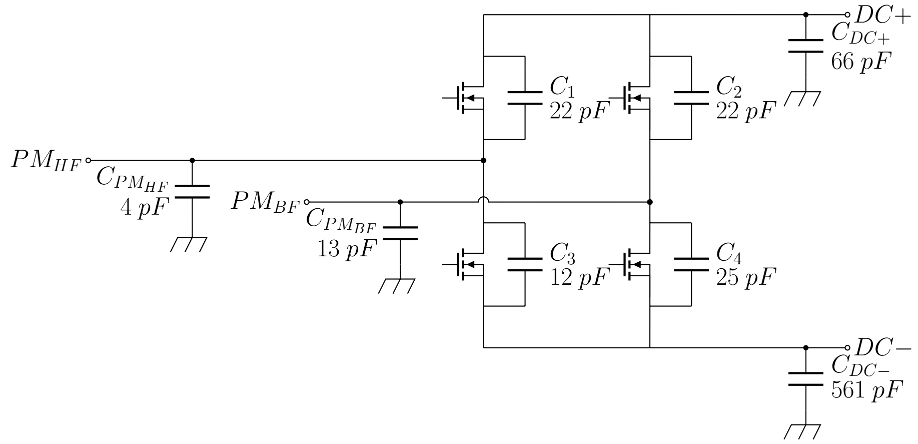


Figure 17: Schéma d'une cellule de PFC avec les capacités parasites obtenues par simulation.

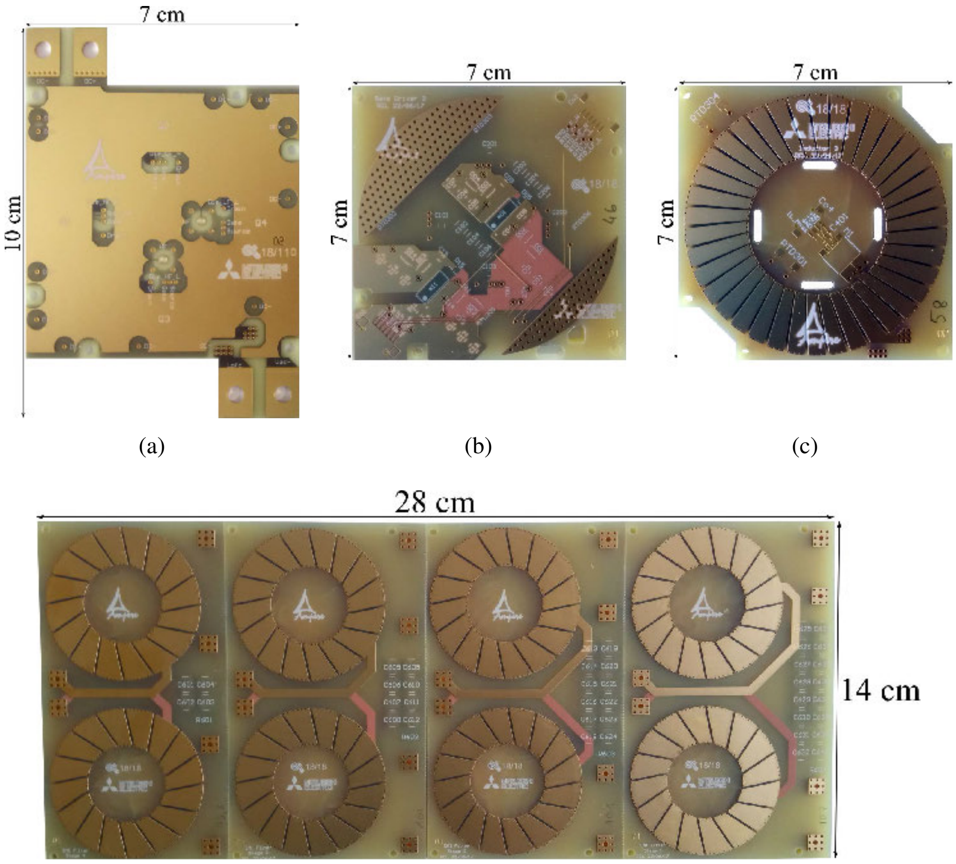
dans la plage de fréquences du gabarit CEM. Q3D Extractor est basé sur la méthode des moments. Les capacités parasites obtenues sont présentées dans la figure 4.22.

Les capacités parasites étaient clairement surestimées pour la première itération. La plus grande valeur est de $561.1\,\mathrm{pF}$ pour la capacité entre le $DC-$ et la terre. La valeur entre le $DC+$ et la terre est seulement de $65.5\,\mathrm{pF}$. Ces capacités ont un impact positif sur le filtrage, la première itération était optimiste. Cependant, les capacités entre les points milieux et la terre ont aussi étaient grandement surestimées. En effet, la capacité entre le point milieu haute fréquence et la terre est seulement de $3.6\,\mathrm{pF}$ alors que la capacité entre le point milieu basse fréquence et la terre est de $12.9\,\mathrm{pF}$. La première itération est pessimiste. Les capacités parasites en paralèle des interrupteurs sont de $22.2\,\mathrm{pF}$, $24.6\,\mathrm{pF}$ et $11.9\,\mathrm{pF}$. Ces valeurs sont faibles comparées par rapport au capacité parasite des puces (C_{oss} $=80\,\mathrm{pF}$).

A cause de contrainte de temps, le premier prototype a été fabriqué avec les hypothèses grossières. Ces simulations ont été effectuées pendant la fabrication du prototype. Les valeurs vont être comparées avec les valeurs mesurées sur le prototype.

Les éléments pour former le prototype sont présentés dans la figure 4.2. Ces éléments sont testés individuellement pour assurer leurs fonctionnalités.

Les tests commencent par ceux sur le PCB avec les 4 puces enfouies. La première étape consiste à mesurer la tension de seuil V_{th} de chaque puce. Pour cela une SMU (Keithley 2636) est utilisée avec le logiciel ACS. Le schéma de test est présenté dans la figure 19. Le canal A applique une tension V_{DS} constante de $5\,\mathrm{V}$. Le canal B applique une tension V_{GS} de $-5\,\mathrm{V}$ jusqu'à $15\,\mathrm{V}$ par pas de $0.2\,\mathrm{V}$. Le courant de drain est mesuré ainsi que le courant de grille car c'est une bonne indication de la fonc-



(a) (b) (c)

(d)

Figure 18: Photographie du PCB avec (a) 4 puces enfouies. (b) 2 circuits de commande enfouis. (c) une inductance "Toroidal Enfoui". (d) le filtre CEM de MD.

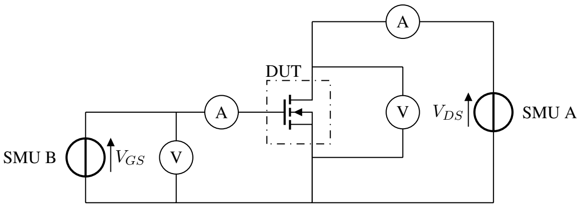


Figure 19: Schéma du test effectué pour la mesure de la tension de seuil de chaque puce.

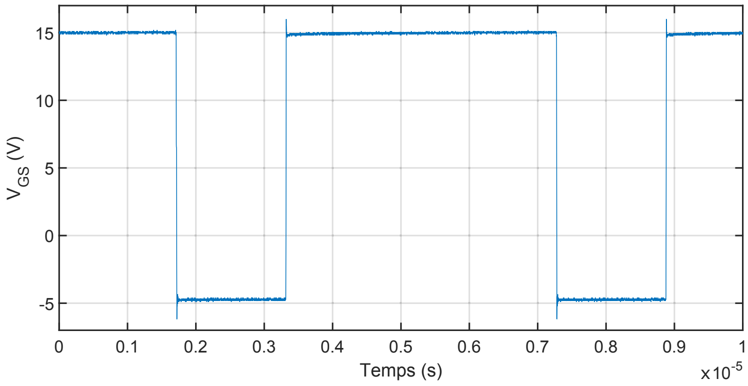
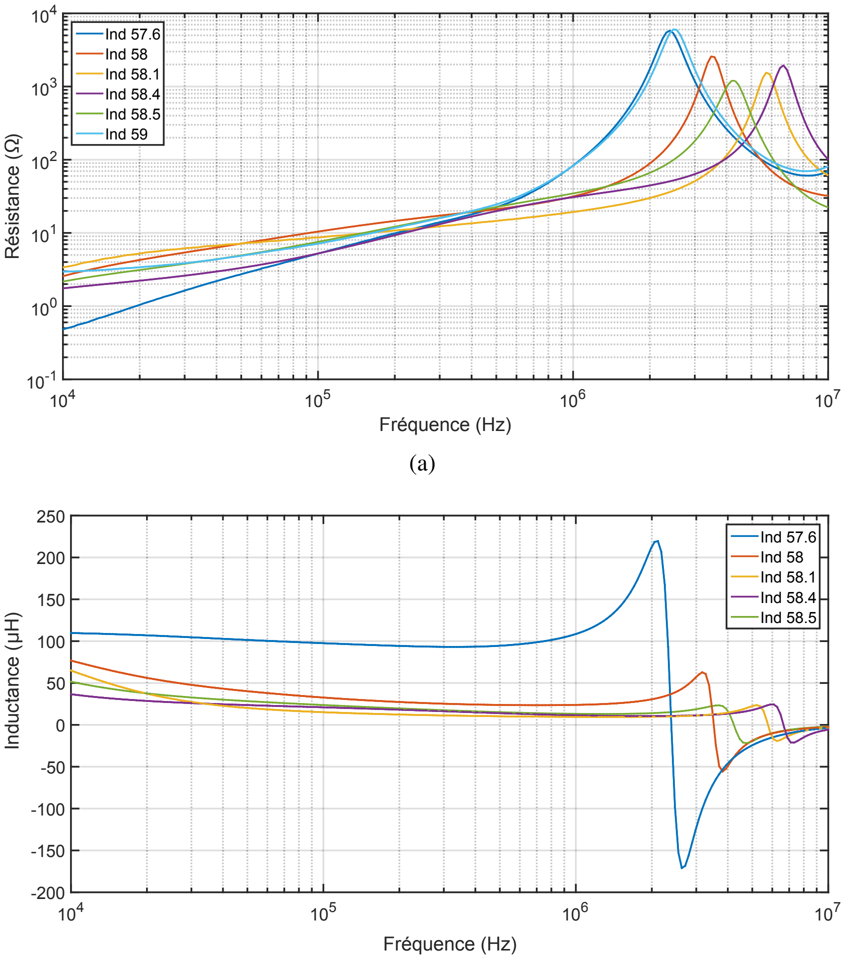


Figure 20: V_{GS} mesurée sur un circuit de commande enfoui (signal haute fréquence).

tionnalité de la puce. La V_{th} est définie pour un courant de drain compris entre $5\,\mathrm{mA}$ et $6\,\mathrm{mA}$. La V_{th} minimale mesurée est de $2.1\,\mathrm{V}$ alors que la V_{th} maximale mesurée est de $2.85\,\mathrm{V}$. Ces valeurs correspondent à la V_{th} de la datasheet du composant. Le courant de grille pour une V_{GS} de $0\,\mathrm{V}$ et une V_{DS} de $2.5\,\mathrm{V}$ sont environ de la dizaine de pA sauf la puce numérotée "02 G LF L" qui a courant de $2.04 \times 10^{-7}\,\mathrm{A}$. L'origine de cette dégradation n'est pas définie. Avec 9 modules reçus, il y en a 8 de totalement fonctionnels.

Les PCB avec les circuits de commande ont été testés en utilisant un PCB auxiliaire connecté à une carte de démonstration comprenant un DSP (F28379D Delfino Experiment Kit). Le code pour le contrôle est développé dans la partie "Topologie". Un signal carré entre $0\,\mathrm{V}$ et $3\,\mathrm{V}$ avec un rapport cyclique variable est appliquée sur la commande haute (ou basse) du circuit intégré driver. La tension grille-source V_{GS} est observé pour la puce haute (ou basse). Les tests n'ont montré aucun problème avec les circuits de commande. Un exemple de mesure est montré dans la figure 5.13.

Les inductances du PFC sont testées avec l'impédancemètre (Keysight E4294A) avec la sonde 42941A. Les résultats utilisant un modèle Rs-Ls sont présentés respectivement dans les figures 5.15a et 5.15b. La valeur requise pour les inductances est de $34.7\,\mu\mathrm{H}$. Cette valeur n'est pas respectée pour toutes les inductances. La prin-



(a)

(b)

Figure 21: Caractéristiques électriques des inductances du PFC (a) Résistance (b) Inductance.

cipale hypothèse est l'impact d'augmentation de la section magnétique au niveau de l'entrefer sur la valeur d'inductance. Cet effet est dû à la longueur de l'entrefer $1.9\,\mathrm{mm}$ pour une épaisseur du noyau magnétique de seulement $3\,\mathrm{mm}$. La longueur de l'entrefer n'est donc pas négligeable. Une valeur d'inductance plus élevée n'est pas acceptable pour le circuit car le ZVS (commutation au zéro de tension) n'est pas obtenu. Une autre observation est la forte augmentation de la résistance en fonction de la fréquence. La résistance à $180\,\mathrm{kHz}$ est d'environ $10\,\Omega$ (+/- $2\,\Omega$ selon les échantillons). Cette résistance est bien plus haute que la résistance calculée dans la procédure ($332\,\mathrm{m}\Omega$).

Avec la même méthode, les inductances du filtre CEM de mode différentiel ont été caractérisées. Les observations sont les mêmes que pour les inductances du PFC.

Une étude plus approfondie des inductances est présentée plus tard. Les inductances sont fonctionnelles même si les valeurs de résistance et d'inductance vont avoir une influence négative sur la fonctionnalité du convertisseur. Les cellules sont donc assemblées pour vérifier la faisabilité de la méthode d'interconnexion. Une cellule de PFC est composée du plus bas au plus haut élément: d'un dissipateur, d'un PCB avec 4 puces enfouies, d'un PCB avec 2 circuits de commande enfouis et d'un PCB avec une inductance "Toroidal Enfouie". Ces éléments sont séparés par une TIM. L'assemblage est présenté dans la figure 5.18. Les fils pour les interconnexions sont soudées sur le PCB des puces avant l'étape (c). Le PCB avec les drivers est ensuite connecté après l'étape (e). Le PCB avec l'inductance est connecté après l'étape (g). Le courant dans l'inductance est présenté dans la figure 23. La charge est une résistance. Les cellules interconnectées sont fonctionnelles.

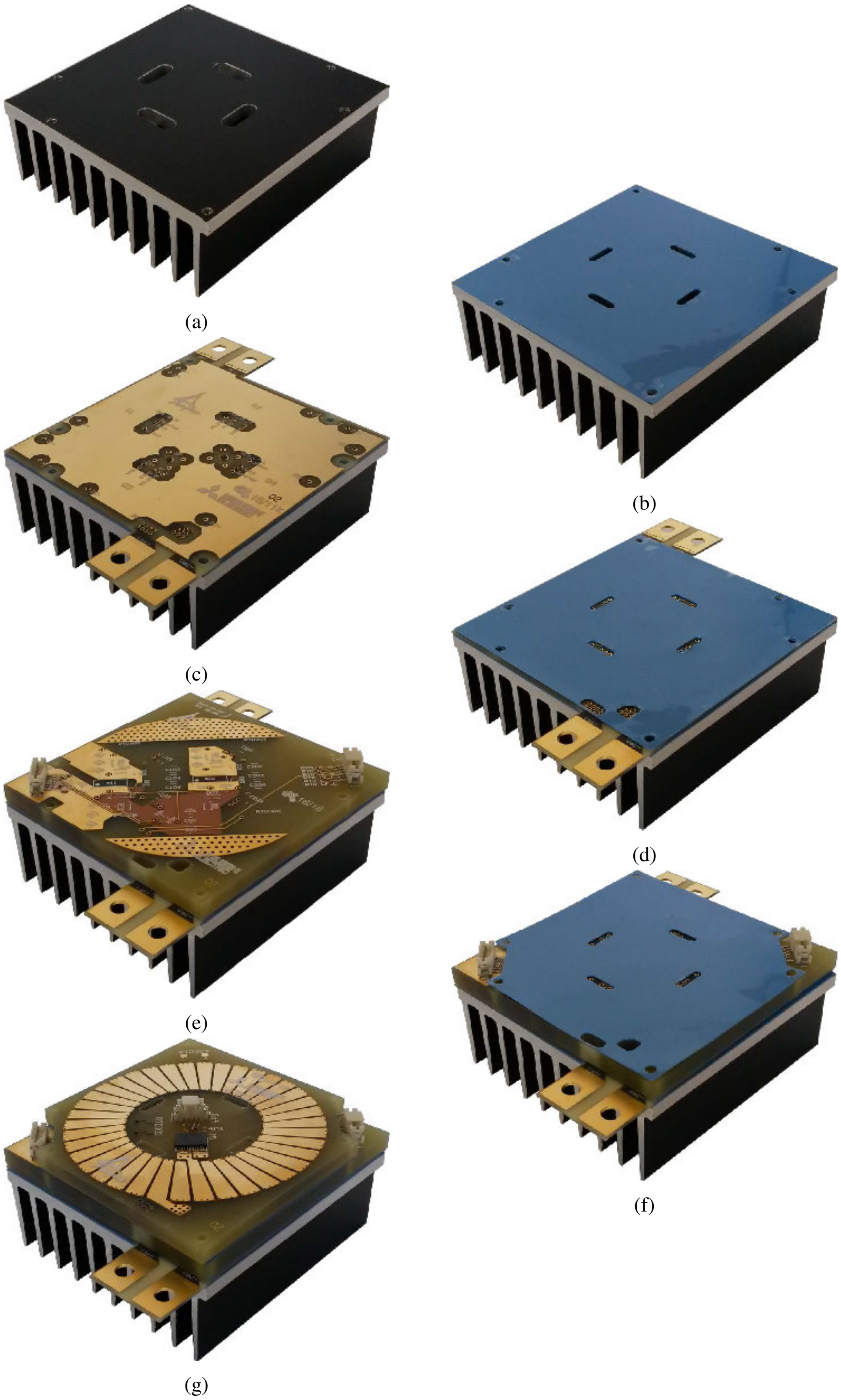
Résultats expérimentaux

Les 4 cellules du PFC sont assemblées ensemble à l'aide du bloc de capacité. L'objectif est de mesurer le courant entrelacé. Une photographie du PFC totalement assemblé avec les capacités est présentée dans la figure 5.24.

Le courant dans chaque cellule et le courant entrelacé sont respectivement présentés dans les figures 5.25 et 5.26. L'entrelacement du courant n'est pas parfait. En effet, la fréquence du courant est de $180\,\mathrm{kHz}$ alors qu'un courant parfaitement entrelacé à une fréquence de $720\,\mathrm{kHz}$ ($4 \times 180\,\mathrm{kHz}$). Le filtre CEM a été conçu pour un courant parfaitement entrelacé, la norme CEM n'est donc pas respectée. Ce résultat était prévisible car les 4 inductances n'ont pas la même valeur. Le PFC est fonctionnel. Les inductances doivent être améliorées pour obtenir la même valeur et une résistance réduite.

Les capacités parasites et la thermique ont quand même été mesurés sur une cellule pour vérifier les modèles précédemment présentés.

La capacité parasite entre le $DC-$ et la terre est mesurée avec l'impédancemètre. La capacité parasite mesurée est de $816\,\mathrm{pF}$ à $500\,\mathrm{kHz}$. La valeur obtenue en simulation était de $561\,\mathrm{pF}$. Le problème est que tout le circuit électrique est relié à travers les capacités parasites des puces. La capacité parasite entre le $DC+$ et la terre s'ajoute donc à la mesure. Sa valeur est de $65.5\,\mathrm{pF}$. On obtient donc une capacité parasite simulée de $626.5\,\mathrm{pF}$. L'erreur entre les deux valeurs est de $30\,\%$. La différence est due à la différence d'épaisseur de la TIM. La pression est appliquée sur le PCB mais le cuivre dépasse de $70\,\mathrm{\mu m}$ réduisant l'épaisseur entre le cuivre et le dissipateur. La mesure des autres capacités n'est pas possible à cause des capacités



(a)

(b)

(c)

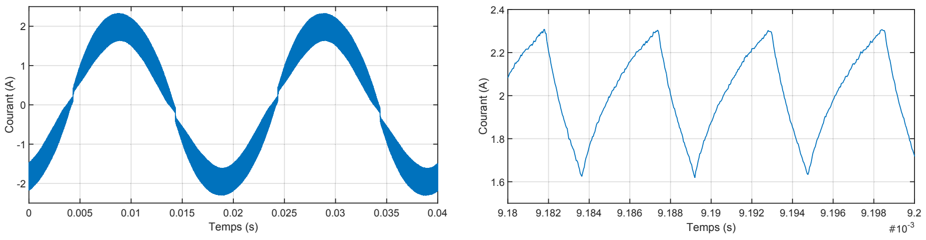
(d)

(e)

(f)

(g)

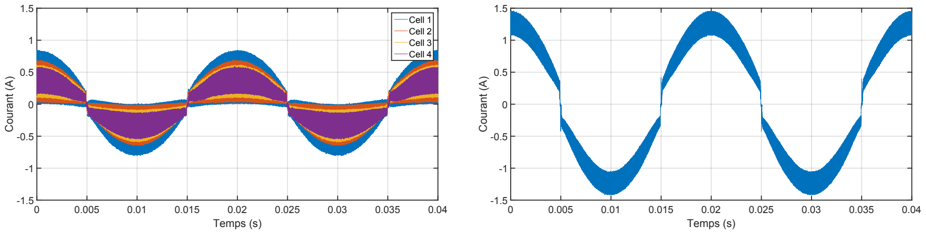
Figure 22: Procédé d’assemblage d’une cellule de PFC.



(a) (b)

Figure 23: (a) Courant à la fréquence de 50 Hz dans la charge. (b) Zoom sur l'ondulation de courant à 180 kHz.

Figure 24: Photographie du PFC totalement assemblé avec les capacités. Les capacités doivent être remplacées par la capacité électronique pour réduire le volume du convertisseur.



(a) (b)

Figure 25: (a) Courant dans chaque cellule du PFC. (b) Courant entrelacé en sortie du PFC.

Table 8: Pertes générées dans chaque élement d'une cellule de PFC pour l'expérience thermique.

Nom	Pertes (W)
1 Puce Haute Fréquence	4 W
1 Puce Basse Fréquence	0.81 W
1 Inductance	2 W

Table 9: Comparaison des températures obtenues par simulation et par expérience au niveau des capteurs.

Nom	Expérience	Simulation
RTD Die HF	36.8 °C 35.3 °C	37.1 °C
RTD Die LF	33.8 °C 33.3 °C	34.1 °C
RTD Outer Ind	27.3 °C	30.9 °C
RTD Inner Ind	30.2 °C	31.2 °C

parasites des puces enfouies. Mais les résultats sont concordants avec la formule d'un condensateur plan.

L'expérience thermique consiste à générer des pertes dans les composants du circuit. Les capteurs de température enfouis dans le PCB driver et dans le PCB inductance permettent de vérifier les valeurs obtenues par simulation. Les pertes générées dans les composants sont présentées dans le tableau 5.4. Ces pertes sont inférieures à celles générées en fonctionnement à cause de la limitation des alimentations disponibles. La simulation est donc adaptée avec ces pertes pour vérifier les températures.

Les températures obtenues par simulation et par expérience sont présentées dans le tableau 5.8.

L'écart maximal entre une température obtenue en simulation et en expérience est obtenue pour le capteur à l'extérieur de l'inductance avec une différence de 3.6 °C. La température obtenue en simulation est supérieure. En effet, la chaleur se propage de façon plus importante dans la simulation que dans le prototype. La conductivité thermique des couches isolantes doit être revue ainsi que le coefficient de convection sur la surface supérieure.

Pour les puces, le plus grand écart de température est 1.8 °C. Encore une fois, la simulation est pessimiste par rapport à la réalité. Cette différence de température est acceptable. Le modèle thermique du convertisseur est validé.

Les inductances "Toroidal Enfoui" présentent plusieurs problèmes. Le premier problème est la différence de valeur entre chaque composant. Le deuxième problème est la diminution de l'inductance avec la fréquence ainsi que la forte augmentation de la résistance avec la fréquence. Pour essayer de comprendre ces problèmes, plusieurs prototypes ont été réalisés à la plateforme 3DPHI de Toulouse.

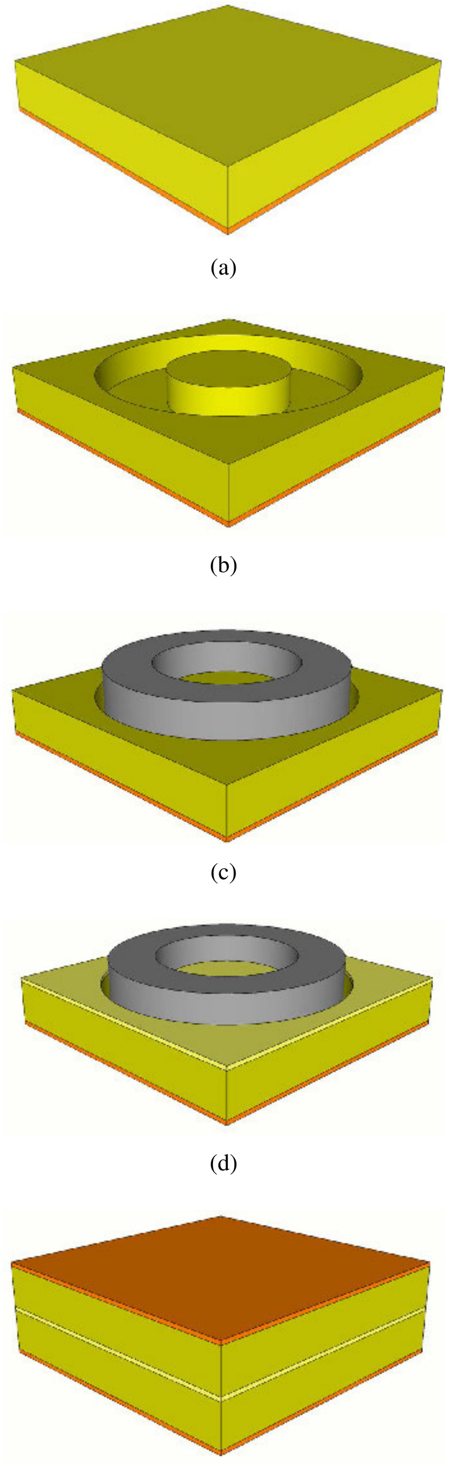
Le procédé de fabrication utilisé est présenté dans la figure 5.32. Le procédé commence par l'usinage d'une cavité à l'aide d'une fraiseuse dans 2 laminés simple face d'une épaisseur de 1.6 mm. Le noyau magnétique est placé manuellement dans une cavité. Une feuille de prepreg découpé est placée par-dessus le laminé. Ce prepreg permet de coller les 2 laminés. Le deuxième laminé usiné précédemment est placé par-dessus. L'ensemble forme un PCB doubles couches. Cet ensemble est laminé pour former un unique solide. Ensuite, les perçages sont effectués puis le cuivre est électrodéposé pour connecter les 2 couches. Les pistes de cuivre sont ensuite gravées. Un exemple de prototype est présenté dans la figure 5.33.

Il y a été observé sur les échantillons fabriqués que la cavité n'est pas totalement remplie de résine. Le management thermique de l'inductance sera plus difficile que ce qui a été considéré dans la procédure d'optimisation. Une deuxième observation est que la répétabilité est excellente.

Avec une étude thermique consistant en une observation à la caméra thermique du PCB pendant le fonctionnement d'une inductance, un point chaud au niveau de l'entrefer a été observé. Ce point chaud est dû au "fringing effect". En effect, le champ magnétique a une section magnétique plus grande au niveau de l'entrefer que dans le noyau magnétique. Le champ magnétique traverse les pistes et crée des courants induits donc des pertes. Pour éviter ce problème, la longueur de l'entrefer doit être négligeable devant les dimensions de la section magnétique.

Cependant, les problèmes liés à la fréquence apparaissent aussi sur les échantillons sans entrefer. Le cuivre proche de l'entrefer du prototype a été retiré. Les pistes manquantes ont été remplacées par un fil plus éloigné du noyau. Les problèmes sont moins importants mais sont toujours présents.

Des noyaux magnétiques ont été caractérisés à plusieurs étapes de la fabrication (après découpe, après enfouissement). Le problème n'apparaît que pour les noyaux enfouis dans le PCB. la préparation du noyau magnétique n'est pas en cause. Alors des noyaux enfouis dans le PCB ont été testés avec différents bobinages (bobinage PCB, bobinage avec un fil). L'échantillon avec un bobinage classique utilisant un



(a)

(b)

(c)

(d)

(e)

Figure 26: Procédé de fabrication utilisée à la plateforme 3DPHI pour les inductances "Toroidal Enfoui".

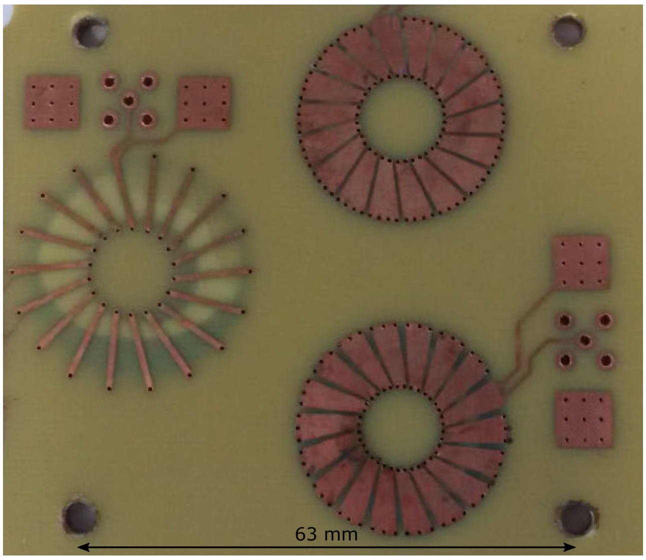


Figure 27: Fabrication collective de 3 inductances "Toroidal Enfoui".

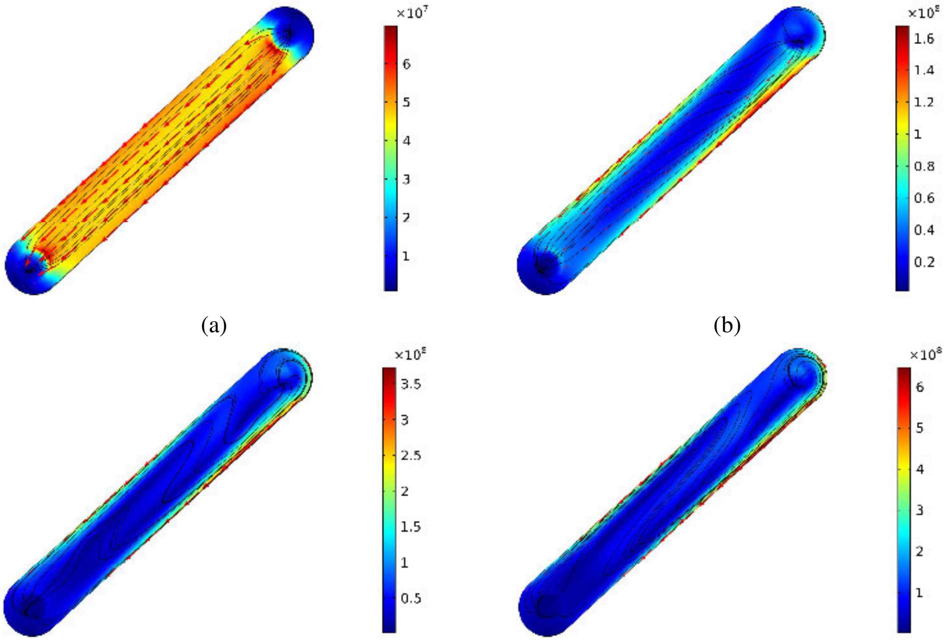
fil ne présente pas de problème. Le problème vient donc de la forme du bobinage utilisant le PCB.

Des simulations magnétiques 3D ont été réalisées à l'aide de COMSOL pour étudier ce problème. Les résultats des simulations sont présentés dans la figure 5.42. Les simulations sont faites pour plusieurs fréquences ($10\,\mathrm{kHz}$, $40\,\mathrm{kHz}$, $70\,\mathrm{kHz}$ et $100\,\mathrm{kHz}$). Le courant utilise toute la section de la piste à la fréquence de $10\,\mathrm{kHz}$. A partir de $40\,\mathrm{kHz}$, le courant commence à utiliser un chemin en "Z" pour aller d'un bout à l'autre de la piste. Cet effet s'accentue avec l'augmentation de la fréquence. De plus, il augmente grandement la résistance puisque la section utilisée est plus faible et le chemin est plus long que l'équivalent à $10\,\mathrm{kHz}$.

L'origine de cet effet n'est pas encore totalement compris. D'autres recherches sont nécessaires pour comprendre et résoudre les problèmes pour limiter les pertes des inductances "Toroidal Enfoui".

Discussion

Le volume du convertisseur est utilisé (à travers la densité de puissance) pour choisir le meilleur convertisseur dans la procédure d'optimisation. Le volume obtenu avec le prototype est donc vérifié par rapport aux valeurs calculées dans la procédure. Le tableau 6.2 présente le volume calculé dans la procédure, mesuré avec le prototype et le volume considérant seulement l'enveloppe des composants dans chaque PCB (Seules les connexions internes) pour chaque élément. Un exemple de "Volume Modifié" pour le second étage du filtre de MD est présenté dans la figure 6.7.



(a) (b)

(c) (d)

Figure 28: Densité de courant dans un plan de la piste supérieure (a) $10\,\mathrm{kHz}$ (b) $40\,\mathrm{kHz}$ (c) $70\,\mathrm{kHz}$ (d) $100\,\mathrm{kHz}$.

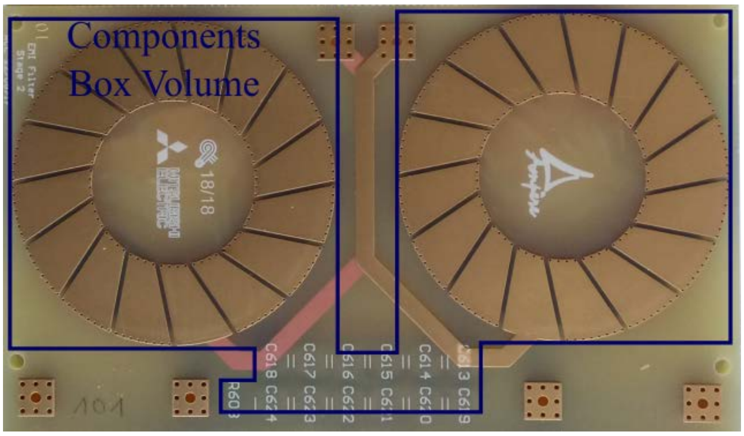


Figure 29: Photo du second étage du filtre CEM de MD. Les lignes bleues sont utilisées pour le calcul du "Volume Modifié" dans le tableau 6.2.

Table 10: Comparaison du volume calculé dans la procédure, mesuré avec le prototype et le volume considérant seulement l'enveloppe des composants dans chaque PCB "Volume Modifié" (Seules les connexions internes) pour chaque élément.

	Box Volume (cm^3)		
Nom	Procédure	Prototype	Modifié
Inductance Planar	17.51	61.25	17.48
Inductance Toroidal Enfoui	15.82	22.05	22.05
DM EMI Filter ("Toroidal Enfoui")	151.1	176.4	128.7
Circuits de commande	2	22.05	9
Puces	7.6×10^{-3}	3.33	1.25
Dissipateur	329	490	490

La différence de volume pour l'inductance "Planar" entre la procédure et le prototype est due à l'assemblage mécanique qui est basé sur une cellule utilisant des PCB de $7{\times}7\,\mathrm{cm}^2$. Les connexions sont réalisées dans les angles, il n'y a donc pas de différence entre le volume calculé dans la procédure et le volume modifié. Pour l'inductance "Toroidal Enfoui", la différence entre les volumes est seulement due à l'épaisseur du PCB ($3.2\,\mathrm{mm}$ pour la procédure contre $4.5\,\mathrm{mm}$).

L'erreur est très importance pour le PCB contenant des puces enfouies et le PCB avec les circuits de commande. Pour le PCB avec les puces, l'erreur est due à l'assemblage mécanique du convertisseur. Pour le PCB contenant les circuits de commande, l'erreur est due aux interconnexions nécessaires pour le circuit et la clearance (Ecartement minimal entre 2 composants) entre les nombreux composants utilisés.

Le volume du second étage du filtre de MD est $43.7\,\mathrm{cm}^3$ alors que le volume calculé est de$37.8\,\mathrm{cm}^3$. L'erreur relative est donc de $15.6\,\%$. Elle est due à la prise en compte seulement des composants sans leurs interconnexions dans la procédure. Les interconnexions dans le filtre CEM ont un volume non négligeable. Avec la prise en compte de ces interconnexions dans la procédure d'optimisation, le nombre d'étages du filtre CEM (MD et MC) devrait être réduit.

Le volume du dissipateur dans la procédure d'optimisation a été calculé en utilisant un coefficient de $5\,\mathrm{cm}^3/\mathrm{W}$. Ce coefficient était très optimiste. Le coefficient obtenu sur le prototype (qui présente des températures à la limite de celles des composants) est de $9.8\,\mathrm{cm}^3/\mathrm{W}$. Le convertisseur optimal est négativement impacté cette erreur. En utilisant un coefficient plus réaliste, l'efficacité du convertisseur aurait un plus grand poids dans les résultats.

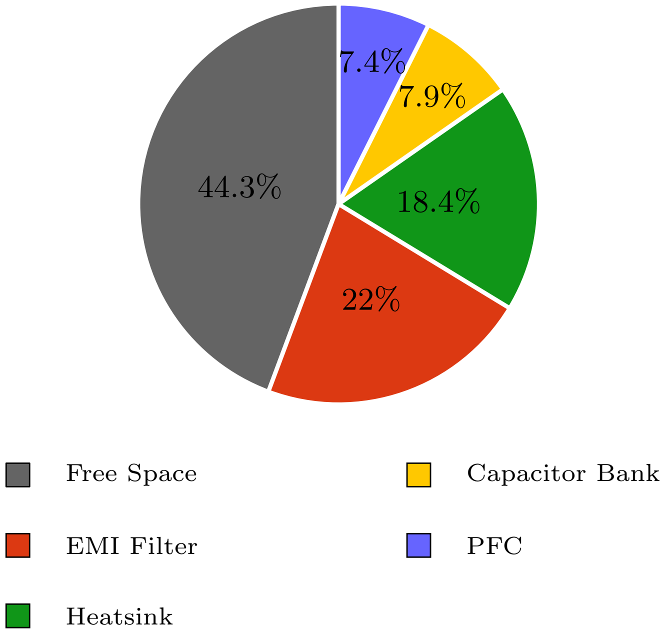


Figure 30: Pourcentage des volumes de chaque élément utilisé dans le prototype.

Le cahier des charges donne un volume à atteindre de $1\,\mathrm{L}$. Le volume du convertisseur avec les inductances "Planar" (Filtre CEM et PFC) est de $2.65\,\mathrm{L}$ donnant une densité de puissance de $1.25\,\mathrm{kW/L}$. La répartition des volumes est présentée dans la figure 6.8. La densité de puissance peut être amélioré grâce à un meilleur assemblage mécanique. En effet, l'espace vide due à la différence d'assemblage mécanique entre le filtre CEM et les 4 cellules du PFC occupe $0.675\,\mathrm{L}$. L'espace vide due au banc de condensateur (Largeur minimale des pistes pour le courant) est de $0.5\,\mathrm{L}$.

Conclusion

La tendance en électronique de puissance est de réduire le volume et d'augmenter l'efficacité du système. L'objectif de cette thèse est l'implémentation d'un convertisseur AC/DC bidirectionnel en utilisant la technique d'enfouissement dans le PCB. L'objectif est d'étudier et de discuter l'intérêt de cette technique sur chaque composant utilisé dans un convertisseur. Il a été montré dans l'état de l'art que l'enfouissement de puces dans le PCB est bien maitrisé par les fabricants de PCB. Pour les condensateurs et des résistances, l'enfouissement des composants discrets dans le PCB est utilisé. Une procédure d'optimisation a été réalisé pour comparer les deux structures "Planar" et "Toroidal Enfoui". La structure "Toroidal Enfoui" a montré que le volume du convertisseur pouvait être réduit par rapport à la structure "Planar". Cette nouvelle structure est limitée par les règles de design du PCB.

Une cellule de PFC est composé de 3 PCBs: PCB avec les puces enfouies, PCB avec les circuits de commande, PCB avec l'inductance. Le procédé de fabrication des deux panneaux utilisés pour la fabrication de ces 3 PCB a été discuté avec les fabricants de PCB. La fabrication avec des composants enfouis est plus longue à cause de la nécessité de plan supplémentaire et la complexité plus importante. Les 3 PCBs sont empilés en étant séparé par une TIM permettant d'améliorer le contact thermique et d'assurer l'isolation électrique. Un dissipateur est placé en dessous pour former une cellule compacte.

Le rendement de fabrication pour le PCB avec les puces enfouies est de $97\,\%$. L'enfouissement des circuits de commande a aussi été un succès avec un rendement de fabrication de $100\,\%$. En effet, aucun problème n'a été trouvé sur ces PCBs. Cependant, l'enfouissement de noyau magnétique pour fabriquer des inductances doit être amélioré. Premièrement, le problème de la forte augmentation de la résistance avec la fréquence doit être résolu. Deuxièmement, le procédé d'enfouissement doit être changé pour éviter la casse des noyaux magnétiques. Il faut noter qu'avec le procédé actuellement la cavité est parfaitement remplie. Les inductances "Toroidal Enfoui" ont été remplacées par des inductances "Planar" pour les tests à puissance nominale.

Un simple modèle thermique a été developpé pour une cellule de PFC. Ce modèle présent un temps de calcul correct avec des résultats précis pour les puces. Il doit être amélioré pour avoir une valeur de température plus précise de l'inductance. Le modèle pour les capacités parasites présente une erreur de $30\,\%$. Cette erreur est principalement due au mauvais contrôle de l'épaisseur du TIM. Cependant, les valeurs obtenues sont bien plus précise que celles utilisées pour la première itération.

Le résultat de cette thèse est un convertisseur fonctionnel utilisant 4 cellules de PFC entrelacées. Le filtre CEM est composé de 4 étages de MD et de 3 étages de MC. La technique d'enfouissement dans le PCB a été utilisé pour les puces, les circuits de commande et les inductances. Le volume demandé n'a pas été atteint à cause de l'assemblage mécanique entre les 3 éléments (Filtre CEM, PFC, Banc de condensateur). L'amélioration principale est la prise en compte de l'assemblage mécanique au début de la procédure d'optimisation.

Abstract

Today, the efficient management of the electrical energy relies on power electronic converters. The conception of a converter is a multiphysic problem: the converter has to ensure electrical functionality, mechanical support and proper thermal management. The new wide-band gap components hold the key for dramatic improvement in performance, but they are currently limited by their package. The integration of a converter should use new interconnection methods to avoid the use of packaged components. The trend is to integrate the maximum of components into a single system. This integration can offer benefits such as size and weight reduction, cost saving and reliability improvement by managing the complexity of the interconnects. Among many integration technologies available, Printed Circuit Board (PCB) is well known in the industry, allowing mass production with automated manufacturing and assembly. The PCB integration was developed with the “Die Embedding” technology in which a bare die is embedded directly in the PCB without any intermediate package. This thesis investigates the use of the embedding technology on all the components necessary to build a converter (Capacitors, Magnetics, . . .). An optimization of the converter is done to take into account the advantages of this new technology. A prototype of an AC/DC bidirectional converter fully integrated using this technology is presented, and its performances are discussed. The embedding processes are developed according to the routing to achieve the best thermal and EMI performances. The process yield is very high ($97\,\%$ for the die board). The "Embedded Toroidal" inductors manufactured present some issues. There were replaced by more standard "Planar" inductor to work at nominal power. The achieved power density is $2.6\,\mathrm{kW/L}$ for the two first stages. Some propositions are given to achieve the specification of $4.2\,\mathrm{kW/L}$.

Contents

Chapter 1

Introduction

Because of its flexibility and the improvements in efficiency it enables, power electronics is a key technology in the management of electrical energy. The number of applications is increasing in numerous field as, for example, transport (electric car, "more electric" aircraft, train), energy (photovoltaic, smart grid) or information technology (smartphones, datacenters).

Beyond meeting the volume, efficiency and reliability specifications of each application, power electronics should also substantially reduce costs. Today, the managing of the electric energy uses power electronic converters. The conception of a converter is a multiphysic problem: the converter has to ensure electrical functionality, mechanical support and proper thermal management.

Due to a high number of interconnections, the integration of a converter with new components is the limiting factor. The trend is to integrate the maximum of components into a single system. It allows to reduce the interconnections and so the parasitic inductors limiting the EMI (Electromagnetic Interference). The integration also improves the value of parasitic capacitors.

Integration of multiple power electronic components into a single system can offer benefits such as size and weight reduction, cost saving and reliability improvement by managing the complexity and the high density of interconnection. Among the many integration technologies available, Printed Circuit Board (PCB) is well known, allowing mass production with automated manufacturing and assembly.

PCB was firstly used as a simple substrate to mechanically support and electrically connect electronic components. Today, PCB allows die embedding or thick copper layer for improved electrical or/and thermal performances. PCB conception is an important phase for a converter. The PCB should be a mechanical support offering the smallest volume, without impacting the electronic components functionality and allowing a proper thermal management. The PCB integration will be explored and used in this thesis.

The objective of this thesis is the design, the realization and the characterization of a converter using PCB integration methods. The chapter 2 presents a literature review of PCB embedding for actives and passives components and PCB thermal management. The chapter 3 describes the framework. A focus is made on the topology optimization and the magnetic components optimization procedure. The chapter 4 presents the implementation of the converter with the PCB manufacturing process flow. A thermal analysis and a parasitic analysis of the converter are presented. The chapter 5 presents the experiments realized on the converter and on several test coupons. The experimental results are compared with the simulation results. The chapter 6 presents a discussion about the design procedure, the models and the fabrication processes.

Chapter 2

State-of-the-art of power electronics integration

2.1 Introduction

For a long time power devices have dictated the pace of development of power electronics. Wide Band Gap (WBG) components have recently been introduced, and potentially offer a significant increase in operating temperature and frequency [12]. Indeed, Silicon carbide (SiC) and gallium nitride (GaN) components offer lower conduction losses and faster switching speeds, enabling a higher power density compared with their silicon (Si) counterparts [13]. However, in modern power electronics, the size of the passive components and thermal management dictate the overall size [14]. So, the capability for WBG materials to work at high frequency and high efficiency makes it possible to reduce the size of associated passive components and heatsink, and therefore to dramatically reduce the overall size of the converter. However, the WBG performances are only as good as those of their package. In order to use the full potential of WBG components, the interconnections have to be short to reduce the parasitic elements and packaging materials have to support high temperature. These two specifications add complexity to the package as compared to using Si components. Today, even as the WBG power devices are continually improving, integration technology is not keeping pace with these developments. The integration is limiting the development of power converters, and we now can consider that packaging technology is the main limitation to power electronics progress [12] [13].

Among the many integration technologies available, Printed Circuit Board (PCB) is well known, allowing mass production with automated manufacturing and assembly. Power electronics integration using PCB technology will be explored in this thesis. An overview of the current PCB technology and recent developments regarding the embedding of power semiconductor dies is given in section 2.2. Sections 2.3 and 2.4 are dedicated to the other components used in a converter (Magnetics, Capacitors and other peripheral components for driving). Finally, section 2.5 will address thermal management.

2.2 Integration using PCB technology

2.2.1 Standard PCB technology

A printed circuit board (PCB) electrically connects electronic components using conductive tracks, pads and other features etched from one or more layers of copper bonded around sheet layers of a non conductive substrate. Components are generally soldered onto the PCB, providing electrical connections and mechanical support. Figure 2.1 presents a picture of a PCB with mounted components.

As they are custom items, tailored to each application, PCBs require a significant design effort to lay out the circuit, but the manufacturing and the components assembly can be automated. Specialized computer assisted design (CAD) software is available to simplify the work of layout. Mass-producing of circuits with PCBs is cheap and fast.

PCBs can be single-sided (one copper layer on a substrate layer), double-sided (two copper layers on both sides of one substrate layer) or multilayer (alternative copper and substrate layers). Multilayer PCBs allow for much higher component density, using inner layers for interconnection to free space on external layers.

PCB manufacturing process has numerous advantages. It offers many layers for interconnection. The dielectric layer thickness can go down to $50\,\mu\mathrm{m}$ with a clearance between two PCB traces of $100\,\mu\mathrm{m}$. The main advantage for industrial products is the maturity of the PCB process at industrial scale. However, regarding power electronics application, the process also has drawback such as the limited copper thickness ($400\,\mu\mathrm{m}$ in a standard stack-up) which can be a limit for current-carrying capability. Also, the thermal conductivity of dielectric layers is low ($0.4\,\mathrm{W/(m\cdot K)}$) impacting system thermal resistance.

Structure

As seen previously, the structure of the PCB can be separated into 2 types of elements: the substrate layers and the copper layers. Practically, a PCB is manufactured from 3 elements: copper foils, prepregs and laminates.

Copper foils are sheets of copper which only parameter is their thickness (usually $18\,\mu\mathrm{m}$, $35\,\mu\mathrm{m}$, $70\,\mu\mathrm{m}$, $105\,\mu\mathrm{m}$ or $210\,\mu\mathrm{m}$).

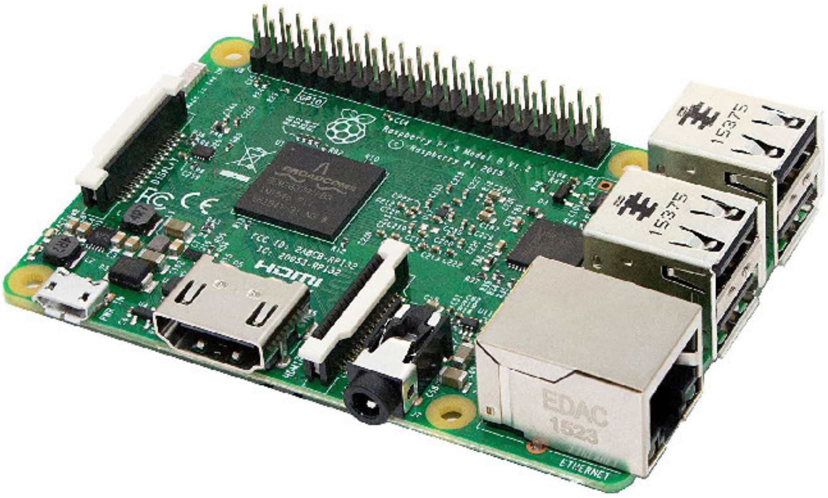
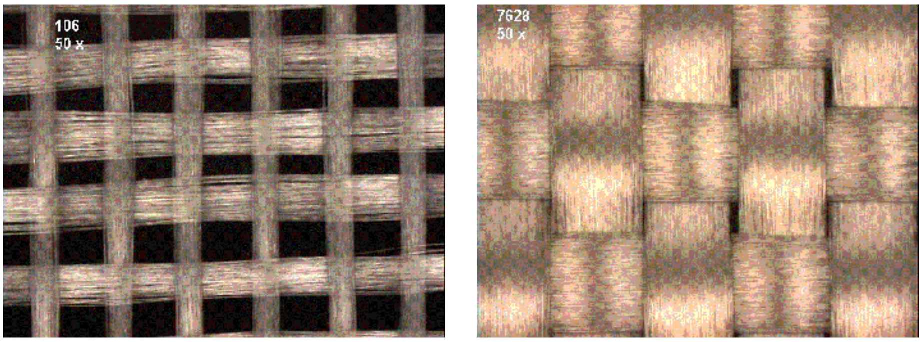


Figure 2.1: Picture of a PCB with mounted components [1].

Prepregs are sheets of a fibrous matrix (usually woven fiberglass) impregnated with partially cured epoxy resin (B-stage). The B-stage means that the resin is applied onto the fiberglass and pre-dried to form a solid but not definitively hardened material. During the manufacturing process, prepregs are fully cured under pressure to bond together laminates and/or copper foils. Prepregs choice is based on four parameters : the matrix structure, its material, the resin content and its composition. The structure of the matrix can be based on woven or un-woven fibers. Regarding the (common) woven structure, many configurations exist, depending on the way the fibers are bundled together (Figure 2.2). Each configuration is referred to using numbers, and results in a different layer thickness. For example, 106 prepregs have a thickness of approximately $60\,\mu\mathrm{m}$ and 7628 prepregs have a thickness of approximately $180\,\mu\mathrm{m}$ [15]. Regarding the material, fiberglass is the most common ('FR-4' is the industry workhorse material), but other materials such as aramid can also be used (i.e. microwave application). Prepregs can have a standard, a medium or a high resin content version. A higher resin content means that more resin will be allowed to flow during the manufacturing process to fill possible cavities in the stack-up. The resin content can vary from $45\,\%$ (7628 prepregs) up to $76\,\%$ (106 prepregs) for Isola prepregs. Others resins can be used such as PTFE or polyimide.

Finally, laminates are pre-pressed stacks of copper foil - prepregs - (optional) copper foil forming a definitively hardened material (C-stage). They are basically a pre-made 1 or 2-sided PCB, and come in a variety of thicknesses and materials.



(a) (b)

Figure 2.2: Pictures of fiberglass configuration for two different prepregs (a) 106 (b) 7628 [16].

Manufacturing

A large number of process steps are used to manufacture a PCB [17]. However, in many cases, they consist in repeating identical or similar basic steps. An overview of the manufacturing process flow for a multilayer PCB is presented in figure 2.3. The process starts with a double-sided laminate, a panel with two copper layers bonded around a substrate layer.

The double-sided laminate is first drilled where the two copper layers will eventually be connected together to form vertical interconnect access, called vias. A drilling bit or a laser can be used to drill those holes. In order to form an electrical connection in the vias, copper is electroplated along the surface of the hole: the board is immersed in a palladium chloride bath. The palladium acts as a catalyst for the galvanic copper deposition. Then, the panel is placed in another bath for the copper deposition. This results in a copper layer with a thickness determined by the duration of the immersion.

Once the vias are formed, the panel receives a photo-sensitive film, also called photo resist for the image transfer step. The photo-sensitive film is covered with a mask (black and transparent area). These two films are maintained on the panel through the help of alignment pins. The assembly receives an exposition to UV light. With a negative photo resist, the exposed part will be insoluble which means the black area on the mask are the image of the desired PCB traces. On the contrary, with a positive photo resist, the exposed part will be soluble which means the mask black area has to be a negative of the desired PCB traces. The unexposed photo resist is washed away giving access to the unwanted copper. The insoluble parts of the photo-sensitive film are still protecting the desired PCB areas.

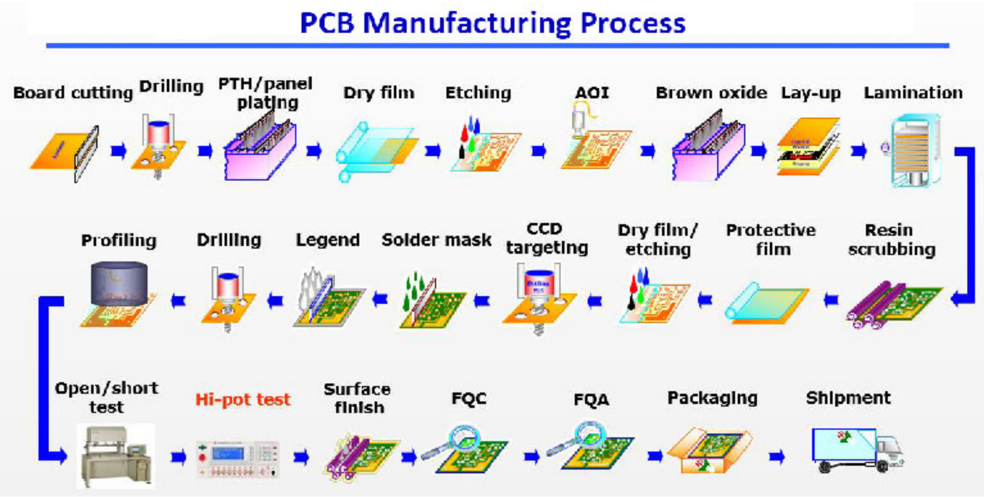
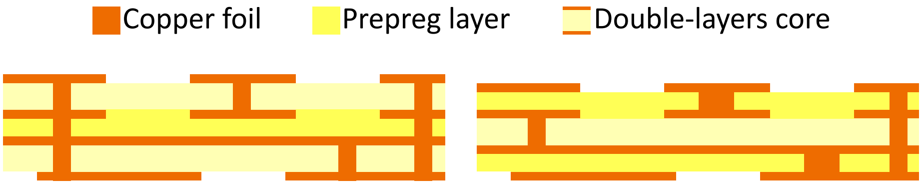


Figure 2.3: Overview of the most main steps in the production of a multilayer PCB [2].

Then, PCB traces are patterned by chemical etching. The etching process is the core PCB manufacturing process. It is a subtractive method which involves removing copper from the undesirable areas. Several chemical reactants can be used. Once the exposed copper areas have been etched away, the photo resist is removed.

The most widely used method for making multilayer boards is by laminating or bonding several double-sided boards or copper foils with prepreg layers. The steps for manufacturing multi-layer boards are generally similar to those used for double-sided boards. For example a 4-layer PCB can be made by assembling two thinner double-sided laminates using a prepreg layer, which corresponds to the following stack-up: double-layer core / prepregs / double-layer core (figure 2.4a). Alternatively, another stack-up can be used: copper foils / prepregs / double-layer cores / prepregs / copper foils (figure 2.4b). The choice between a copper foil and a laminate depends on the PCB design (location of the vias, copper thicknesses) with the objective of keeping the structure as symmetric as possible to prevent bending.

In a multilayer PCB, several types of vias can be manufactured. Through hole vias connect the two outer and one or more inner copper layers of the final PCB structure. Buried vias connect only several inner layers. Lastly, blind vias connect one external layer and one or more inner layers. The types of via have a strong impact on the copper deposition process. A through-hole via can be filled by both sides when blind via are accessible from one side only. This impacts the allowed aspect ratio (hole diameter divided by hole length) possible. The aspect ratio can be



(a) (b)

Figure 2.4: 4-layer PCB realized with the stack-up: (a) double-layer core / prepregs / double-layer core (b) copper foils / prepregs / double-layer cores / prepregs / copper foils

1:10 for vias accessible from both sides when it is limited to 1:1 for vias accessible from one side only.

For protection and to facilitate the soldering of components on the PCB, the practice is to apply a soldermask. The soldermask is opened only where electrical access is required (soldering of components, connectors). The openings are coated with a surface finish to be protected from oxidation. The surface finish can be done with electroless nickel/immersion gold, silver or tin.

The PCB is then tested to ensure the proper functionality of the electrical circuit. The test checks for short, open and net list connectivity.

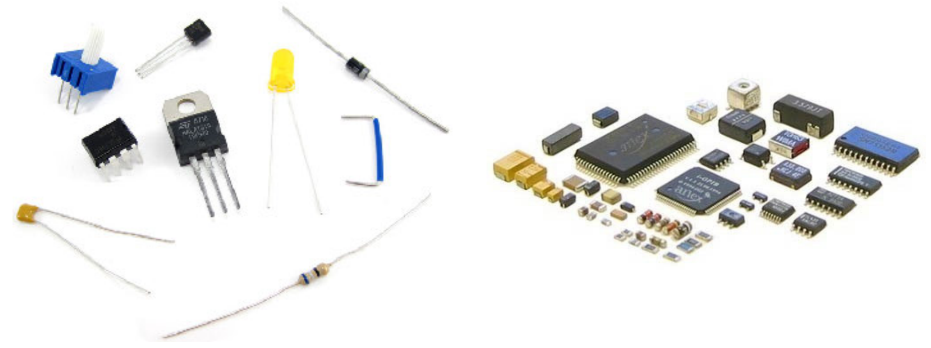
Finally, the PCB panel receives some marking (silk screen) and the individual circuits are separated by mechanical routing.

Assembly

Once the PCB has been finalized, the components are assembled. There are two standard assembly processes: through-hole technology (THT) and surface-mounted technology (SMT) (Figure 2.5).

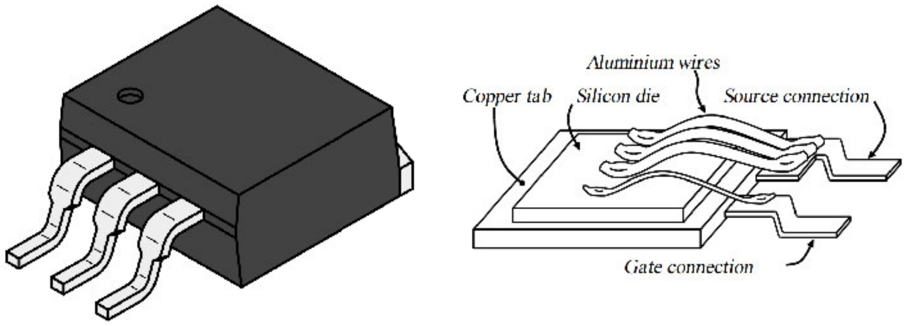
The first PCBs used THT where electronic components are attached by inserting their leads through holes in the board. The components are soldered onto copper traces on the other side. Leads may be soldered either manually or by a wave soldering machine. However, this technology requires aligning precisely the leads with the holes in the board, which can be difficult (bent leads) and limits the available routing area due to through hole. This technology is still mostly used for components with high power requirements or mechanical limitations, such as connectors.

SMT uses components with small metal tabs or end caps that can be soldered directly onto the PCB surface. The components are classically soldered using a solder paste deposed by stencil printing on component footprint. The components are placed on the paste. The soldering process is done using a reflow soldering oven. SMT al-



(a) (b)

Figure 2.5: Pictures of (a) THT components (b) SMT components.



(a) (b)

Figure 2.6: (a) Drawing of a T0 263 package. (b) Drawing of a packaged active component without the resin mold . The backside of the chip is soldered to the tab and the topside is connected to the leads using wirebonds [19].

lows the use of small components such as the "0402" metric package ($0.4\times0.2\,\mathrm{mm}^2$), a much higher component density and a higher connection density (no holes restricting the available area on inner layers). It also presents electrical advantages such as lower parasitic resistance and inductance.

These two interconnection methods are used with discrete components as well as ICs. For standard power semiconductors, the die is placed inside a package (figure 2.6). The die backside is soldered to an electrical tab. The top side pads are connected to the leads using wirebonds. The assembly is molded in resin. The package should ensure a good electrical, mechanical and thermal functionality. The parasitic elements, such as the parasitic inductance induced by wirebonds, limit the performance of the components [18]. This becomes a critical point for the WBG materials (SiC and GaN) which allow fast power devices to be made.

New interconnection methods were developed to be able to use the WBG components at their full potential. A new interconnection method is the die embedding technology in which bare dies are directly embedded in the PCB substrate. This new method is presented in section 2.2.2.

2.2.2 PCB embedding

The embedding of bare dies in the PCB is used to get the best performance of the new power semiconductor devices. The embedding of active chips in PCB is a 3-dimensional integration enabling a high degree of miniaturization, improved electrical and thermal performances. Indeed, embedded chips use the space available inside the PCB, reducing the overall thickness and allowing 3D stacking. The driver circuit can be then located directly above the embedded chips, improving electric performance by reducing the parasitic elements. Also, embedded chips are closer to the thermal management system without the thermal barrier which is formed by the package, improving the thermal performance. The embedding of passive component or driving circuit allows better electrical performance.

The objective of a reduced size is achieved for the module developed for WBG components using die embedding technology presented in figure 2.7. The die embedding technology allows to place the decoupling capacitors and the command circuit directly above the dies to reduce parasitic elements. The DC link inductance is below 8 nH [9].

In [20], a module using embedded dies in a PCB is developed and investigated considering thermal resistance and reliability. Figure 2.8 presents the developed module, which is compared to a classic wire-bonded module. The thermal resistance of the PCB module (active components to cooler) is comprised between $0.50\,°\mathrm{C/W}$ and $0.61\,°\mathrm{C/W}$. This corresponds to a 30-44 $\%$ reduction in thermal resistance compared to the classic module. In addition, for the same cooling condition and current rating, the PCB module has a longer lifetime during active power cycling that the classic module, due to a lower peak temperature, thus lower temperature swing.

Before the development of this technology, PCB manufacturers were not used to manipulate components. Component assembly is usually performed by different companies than PCB manufacturing. So, each PCB manufacturer developed its own method to embed chips. Each solution developed can be summarized with 3 steps. The first step is to bond the die on a copper layer with a conductive or a non conductive die attach. Prepreg layers and a top copper sheet are then stacked-up and laminated to form a double-sided PCB with embedded dies. If more connections are needed, the PCB is opened with mechanical or laser drilling. Then, electrical connec-

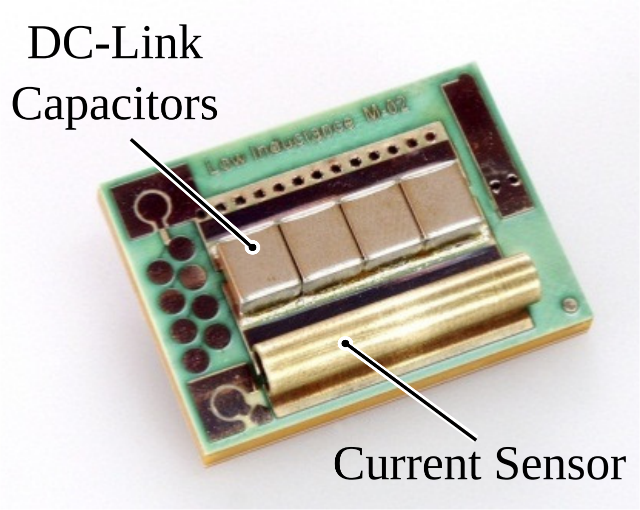


Figure 2.7: A module developed for WBG components using dies embedding. The parasitic inductance is greatly reduced due to the short distance between the embedded switching components and decoupling capacitor and command circuit [9].

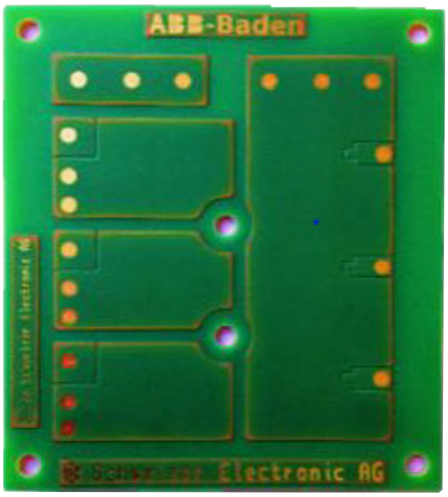


Figure 2.8: A module with embedded components (6 IGBTs and 6 diodes). The module is compared with a classic wire-bonded module in [20].

tions are made with galvanic copper deposition. The outer layers are structured by etching. The double-sided PCB with embedded dies can then be used as a laminate in a multilayer PCB.

In power electronics, it is possible to use lateral (e.g. GaN Transistors E-HEMT GS66516B, GaN Systems) or vertical (e.g. SiC MOSFET CPM2-1200-0080B, Wolfspeed) devices. Therefore, in the first case, we need to make electrical connection only from one side, in the other case we need to connect the device from both sides. This impacts the packaging method, the isolation and the thermal management.

Details of each step (Die attach, Embedding, Added Connection) are explained below for the different methods.

Die Attach

The first step is the die attach. The attach can be done with a conductive or non conductive bond on a substrate. The substrate can be a copper foil, a laminate or a direct bonded copper (DBC) substrate. The copper foil and laminate present the advantage of being standard elements in a PCB. The DBC substrates, which are a ceramic layer sandwiched between two copper layers, present better thermal performance.

The die attach can use several technologies. For example, the die can be soldered. The first step is to structure the substrate conductive layer with a footprint adapted to the interconnection of the die. Then the die is soldered to the substrate as a standard SMT component.

Silver sintering can also be used as a die attach [21]. As for soldering, the first step is to structure the conductive layer. The silver paste is then deposited on the component landing pads and the components are positioned. The silver paste is processed under moderate temperature (lower than 300 °C). Mechanical pressure can be needed according to the type of silver paste used. The diffusion mechanisms form a solid joint with a melting temperature of 961 °C. The formed attach is reliable and suited to high temperature. However, silver sintering is not a standard step of the PCB process and the mechanical pressure can damage the chips.

A conductive die attach method was also developed by Würth Elektronik [22]. The process is presented in figure 2.9. The substrate conductive layer is patterned as for the previous methods. The footprint is then covered with some anisotropic conductive adhesive. Gold stud bumps are deposed on the chip pads. The die is placed onto its footprint. The electrical connections are done by the particles of the adhesive pressed by the gold stud bumps. Between stud bumps, the particles are not in contact due to the anisotropic particle repartition of the paste avoiding short-circuit. The process is simple but slow and expensive due to the deposition of the gold stud

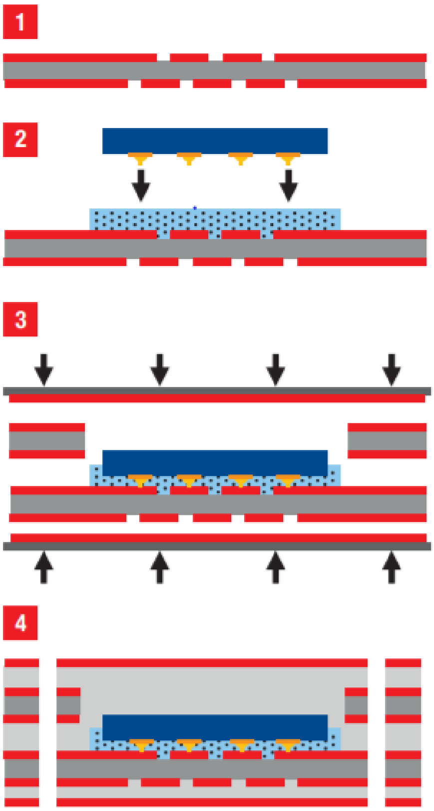


Figure 2.9: Flip-chip embedding technology using gold stud bump and anisotropic conductive adhesive [23].

bumps on each pad of the embedded die. Also, this process is not suited to the high current values of power electronics.

A non-conductive die attach method is used by [24]. The die is bonded on the substrate with the help of glue or non-conductive adhesive. With this method the electrical connections are made after the lamination as it will be seen in the "Additional Connection" section.

Embedding

In order to embed the dies, the PCB has to be stacked-up and laminated. The stack-up is composed of a copper foil or a laminate bonded using prepreg layers to the assembly with the mounted dies. The prepreg layer stack-up has to compensate the die thickness and isolate the die from the copper layer. In the implementation, some prepreg layers are cut to form the cavity around the die and some prepreg layers are kept plain for the isolation between the die and the copper. The choice of the prepreg (type, resin content) is important since the cavity created should be filled with resin during lamination. The stack-up is then laminated to form a solid assembly.

Additional Connection

Once the dies have been embedded, more interconnects may be needed, either on one side or on both, depending on the die attach method (Soldered or sintered dies are already electrically connected on one side, while bonded dies with non conductive die attach are not).

A process using microvias is presented in figure 2.10. Holes are drilled with a laser to access the die pads [24]. Then, they are filled with copper using electro-deposition to form microvias. This requires the dies to have a copper metalization thicker than 6 µm as their pad finish. Indeed, a copper metalization is needed to obtain a good attach between the die and the electro-deposed copper. The thickness is necessary to ensure the laser drilling ablates PCB material all the way to the pads but does not damage the dies. This connection technique presents a good thermal conductivity but it cannot be used with a thick copper layer above the die due to the limitation in the diameter/length ratio of microvias (1:1). The copper metalization of the dies is a drawback since it is not standard. Dies with such finish are difficult to procure and are often obtained from re-processed standard dies.

The opening to access the pads can also be done with mechanical machining [26]. In this process, the embedded die pads are covered with gold stud bumps. These stud bumps are 60 µm thick, and the aim is to increase the equivalent pad thickness to make it compatible with the accuracy of mechanical router used to machine the openings. The openings are plated with electro-deposited copper to form a contact with the stud bumps. A paste is deposited inside the cavity to equalize the surface and allow to use the PCB in a multilayer stack-up. The process advantages are the simplicity of the mechanical machining and the absence of thick copper metalization. But the process is slow and expensive due to the numerous gold stud bump needed. The cross section of an embedded die is presented in figure 2.11 and the corresponding module in figure 2.7.

Another mechanical process is presented in [27]. Copper interposers machined out of a 400 µm copper sheet are soldered on the top side of the die. The objective of these interposers is to increase the thickness of the top die metalization. The embedded die (actually the copper interposers) can then be reached by mechanical drilling to make the top connections. The openings are plated with electro-deposited copper. The simplicity of the mechanical drilling is one of the main advantage of this process along with the use of dies with standard metalization (Aluminum on

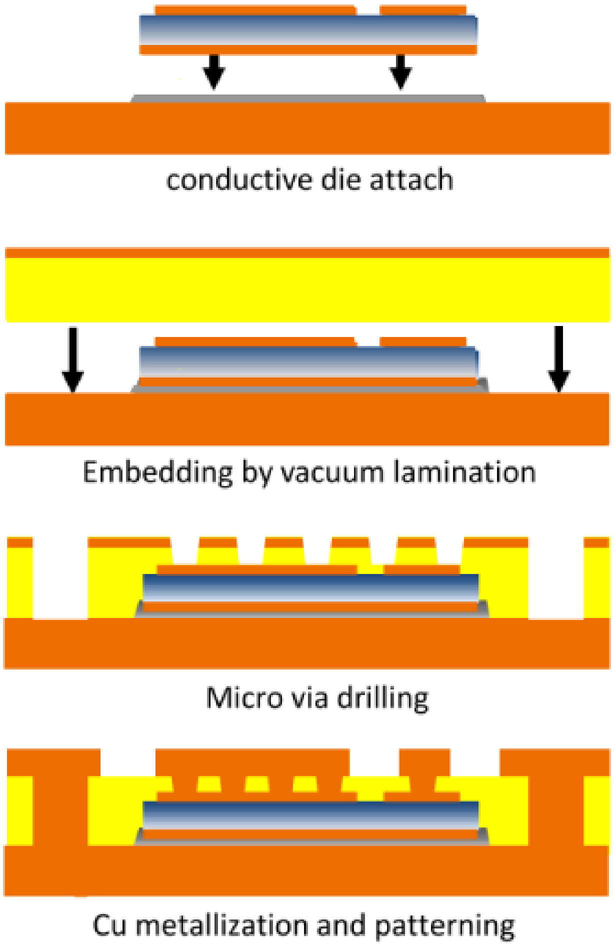


Figure 2.10: Embedding technology using microvias [25].

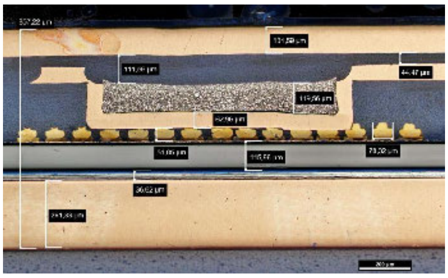


Figure 2.11: Cross section of a die embedded using gold stud bump and mechanical drilling technology. The cavity is filled with paste to equalize the surface and allow multilayer stack-up [26].

(a) Insulated Leadframe fabrication

(b) Die-attach

(c) Interposer over semiconductor dies

(d) Milling cavities into the PCB

(e) Adhesive bonding of leadframe into PCB

(f) Blind via mechanical drilling

(g) Electroplating of interconnections

(h) Structuring of interconnections

Figure 2.12: The manufacturing process flow of the embedding technology using mechanical drilling with copper interposers [27].

the front and silver on the back). However, dies modification with the soldering of copper interposers is done die by die which makes it slow and expensive. The process is presented in figure 2.12.

The prototype of this thesis is going to use the process with a non conductive die attach (Non conductive glue) and connection using microvias on both sides of the die. This process presents the advantage to provide a connection with a good thermal conductivity. It also allows mounting dies in any orientation as no assumption is made regarding the layout of the die side which is bonded first. Indeed, power dies have a side with only one pad taking the whole surface (i.e. Drain for a MOSFET), while the other side can have one or several pads (i.e. Source and gate for a MOSFET). Connecting dies with microvias on both sides allow to mix chips in both orientations ("Flipped" and "Non flipped"). The drawback of this process is that it requires chips with a double copper metalization, on top and bottom, which is not standard. In our case, this was not an issue because dies with copper metalization were readily available.

2.3 Magnetic Components

The magnetic components occupy a large part of a typical power converter volume (e.g. 13 % in [28]). Furthermore, they are custom components, individually wound according to the target application. As a consequence, there is an interest in technologies which enable more compact magnetic components to be designed, or which simplify the manufacturing.

Planar components (Figure 2.13) answer this latter issue. The winding is manufactured using PCB copper layers and vias. An external magnetic core is clamped around the PCB. This forms a low profile component with a good thermal management, a high power density, an easy manufacturability and good repeatability. The drawbacks are a large footprint, a low copper filling factor and a high interwinding capacitance [29]. In addition, these components are not fully integrated since the magnetic core sticks out of the PCB. Then thermal management system has to be adapted (e.g. by machining pockets in the heatsink) and stacking capability is reduced.

Fully embedded structures, as seen in figure 2.14, address all these issues. However, research investigations have mainly been focused on low-power application (1-100 W) using either no magnetic material at all (coreless components) [31] or magnetic cores with small size [3]. In theses structures, the magnetic core is embedded inside the PCB. The winding is formed around the copper using PCB copper layers

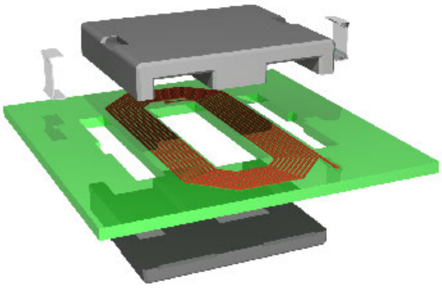


Figure 2.13: Drawing of a planar component. The magnetic core is clamped around PCB winding [30].

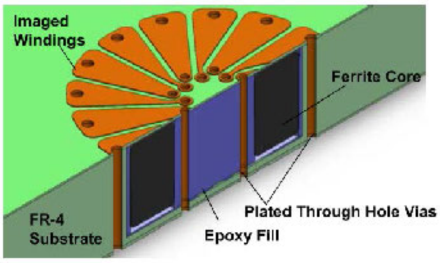


Figure 2.14: Drawing of an embedded magnetic device. The magnetic core is embedded inside the PCB. The winding is manufactured around the core using PCB traces and vias [3].

and vias. The advantages of such structure are the thermal management capability and the stacking capability.

Magnetic components embedding with standard magnetic materials (Ferrite, Iron Powder cores, etc...) and with mechanically compliant magnetic materials is presented below.

2.3.1 Standard Magnetic Materials

In [4], a ferrite magnetic core is embedded in the PCB to realize two coupled inductors. The coupled inductors are used in an EMI filter for a $30\,\mathrm{W}$ converter. They have a value of $3\,\mu\mathrm{H}$ each. The PCB integration allows reducing the volume of the filter by $58\,\%$ with an improvement on CM and DM attenuation. The final PCB size is $4.5 \times 4 \times 0.25\ \mathrm{cm}^3$. The magnetic core thickness is $1.5\,\mathrm{mm}$. The prototype is presented in figure 2.15a. The flat shape of the magnetic core allows it to withstand mechanical pressure during the lamination.

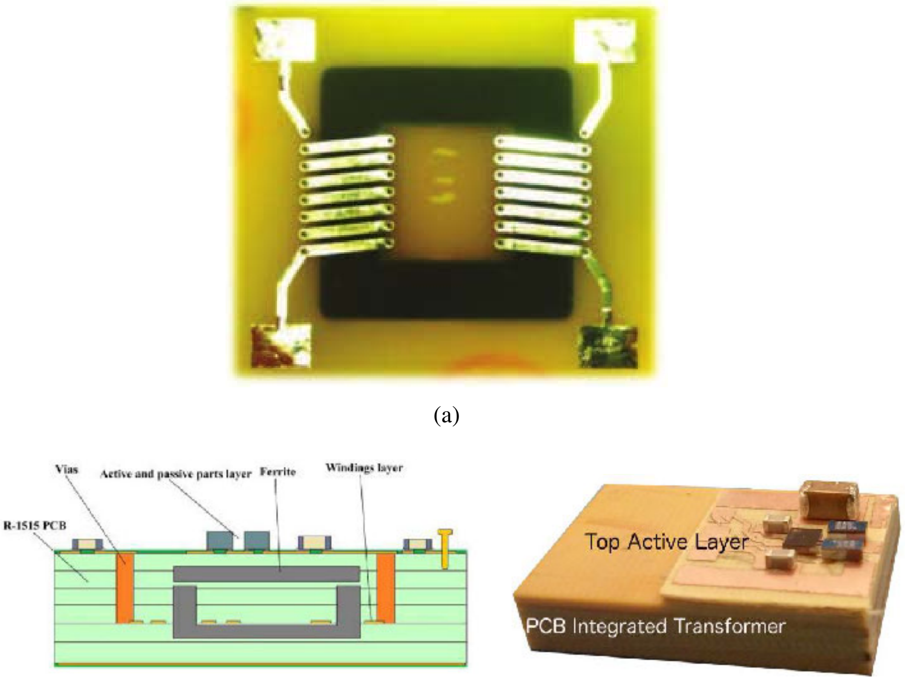
Small transformers can also be formed by embedding ferrite cores vertically inside the PCB [5]. A transformer for a 2 W power supply is prototyped. The size of the prototype is $1.5 \times 2.2 \times 0.36\ \mathrm{cm}^3$. The embedded transformer uses two cores, a U-shape and an I-shape. The embedding process is separated in three steps. First of all, both magnetic cores are embedded separately. The two PCBs are then assembled together by prepreg layers. The added prepregs layers are used to control the air-gap length. This separated process allows to limit the mechanical stress on the magnetic cores during the lamination step to avoid cracks, at the expense of a more complex manufacturing process. Figures 2.15b and 2.15c respectively present a drawing of the cross section of the PCB with embedded magnetic core and a picture of the prototype.

The one step embedding of such a "vertical core" is investigated in [4], with two objectives. The first one is the embedding of the two magnetic parts without damage. The second one is the control of the air-gap length. For the study, two prototypes were made. The first prototype show cracks in both magnetic parts due to a direct contact between them, resulting in an important pressure. The second prototype in which prepreg layers were added for better mechanical compliance still shows cracks. Also, the two magnetic parts are not in contact anymore which results in excessive air-gap length. From these results, it is possible to see that embedding brittle magnetic cores in a PCB is a complex operation.

In addition, two transformer prototypes were made with the process using three embedding steps. These two prototypes were made using two different PCB substrate materials. The two substrates were chosen for their z-axis CTE (Coefficient of Thermal Expansion). The first one has a z-axis CTE of $22 \times 10^{-6}\ \mathrm{ppm/K}$ and the second one a z-axis CTE of $60 \times 10^{-6}\ \mathrm{ppm/K}$. As a reference, the CTE of the embedded MnZn ferrite core is $10 \times 10^{-6}\ \mathrm{ppm/K}$. After 1000 thermal cycles, from $-55\ {}^\circ\mathrm{C}$ to $200\ {}^\circ\mathrm{C}$ with a $20\ {}^\circ\mathrm{C/min}$ ramp and a $20\ \mathrm{min}$ holding period at the extreme temperatures, no delamination or defects are observed on the sample using the low CTE substrate. On the contrary, the prototype using high CTE substrate presents cracks in the core and delamination of the substrate after only 150 thermal cycles.

The embedding process and the materials have to be perfectly chosen to not damage the magnetic core. Indeed, the embedding process might crack the magnetic core due to the mechanical pressure. The materials have to be chosen with a CTE close to that of the magnetic material to avoid stress in operating conditions. With larger magnetic cores, one can expect these issues to become more significant.

A possible workaround is to use more compliant materials. This is described in the next section.

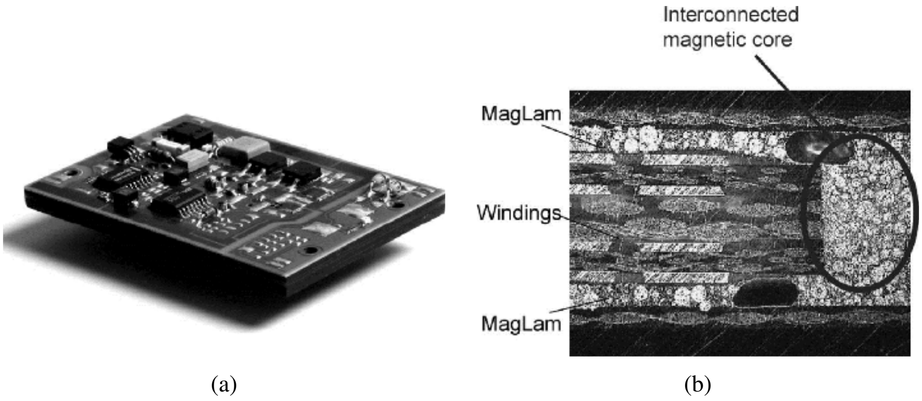


(a)

(b)

(c)

Figure 2.15: (a) Two coupled inductors using an embedded magnetic core in a 30 W converter [32]. (b) Cross section drawing of the transformer using an embedded magnetic core for a 2 W power supply. The other components for circuitry are reported on the top layer. (b) The prototype corresponding to the cross section drawing [5].



(a) (b)

Figure 2.16: (a) Picture of the prototype using an embedded transformer. The magnetic core is formed using a ferrite polymer compound material (MagLam by Isola). (b) Cross section of the PCB of the prototype. The material becomes soft during the lamination which allows to fill holes to form closed core [34].

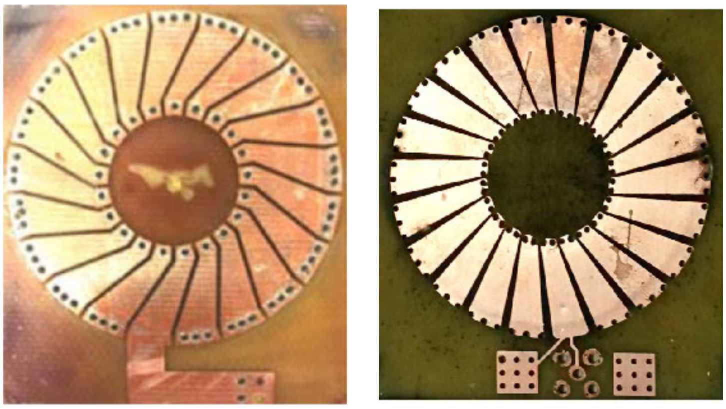
2.3.2 Compliant Magnetic Materials

Compliant materials are materials which will not crack under the mechanical pressure in the lamination steps of PCB manufacturing. For example, it can be flexible layer or powder.

In [33], embedded magnetic components were made of nanocrystalline and amorphous materials. The core is realized by a stack of $20\,\mu\mathrm{m}$ thin magnetic foils. The layer is flexible due to its low thickness. A transformer with a rated power of $76\,\mathrm{W}$ for a volume of $13.9\,\mathrm{cm}^3$ is prototyped. The main constraint is the machining of such materials.

In [34], a converter containing an embedded transformer is prototyped. The PCB size is $80\,\mathrm{mm} \times 55\,\mathrm{mm} \times 4\,\mathrm{mm}$. The prototype is presented in figure 2.16a. The transformer uses Ferrite Polymer Compounds (FPC). They consist of ferrite powder in a polymer matrix. The typical relative permeability of such materials is between 10 and 20. The chosen material is "MagLam" developed by Isola ($\mu_r = 17$). The material is compatible with PCB process. In addition, it becomes soft during the lamination which allows to fill holes to form a closed core or complex shape (Figure 2.16b). The drawback is its low relative permeability.

In [6], an embedded inductor is manufactured to be used in a $400\,\mathrm{W}$ boost converter working at frequency comprised between 2 and $8\,\mathrm{MHz}$ (Figure 2.17a). The magnetic material is a super-thin sintered ferrite platen (IBF15). The magnetic material has a relative permeability of 110. However, it is observed that after lamination the relative permeability drops to 95. A microscope observation shows a degradation



(a) (b)

Figure 2.17: (a) Photography of the power inductor prototype using super-thin sintered ferrite platen magnetic core [6]. (b) Prototype using a magnetic core formed by a direct embedding of MnZn ferrite powder in a prepreg layers stack-up [7].

of the material. The fragments are separated creating an additional distributed air-gap. The effect on performance of the material degradation due to the lamination is not well known.

Another embedded inductor for power application is also studied in [7]. In this process, MnZn ferrite powder is directly embedded in a cavity formed in a stack-up of prepreg layers. A relative permeability of 24 was achieved for large core ($50\,\mathrm{mm}$). It was observed in large core that the resin from prepreg layers does not infiltrate between most of the ferrite particle. So the resin does not reduce the distributed air-gap which explained the low relative permeability. Powder materials show lower relative permeability compared to materials sintered at high temperature due to the distribution of the air-gap. A manufactured prototype is presented in figure 2.17b.

An embedded inductor is made by mixing an organic paste (polyimide) with some NiZn ferrite powder (Figure 2.18) [35]. For the implementation, a 4-layer PCB is manufactured with a spiral winding on the inner layers. A hole is drilled at the center of the spiral winding. The mixed material is screen printed on the top and bottom surfaces. The paste fills the hole at the center of the spiral. It is then cured at $180\,^{\circ}\mathrm{C}$ during $4\,\mathrm{h}$ in a vacuum oven, a process compatible with standard PCB process temperatures. The prototype is $4.5 \times 4.5 \times 0.5\ \mathrm{mm}^3$, with an inductance of $0.81\,\mu\mathrm{H}$. This method can be used for larger inductors but the relative permeability is low ($\mu_r = 4.34$).

Another process is the electroplating of a permalloy ($Ni_{80}Fe_{20}$) [36]. A PCB is manufactured as previously with the winding on the inner layers. The magnetic mate-

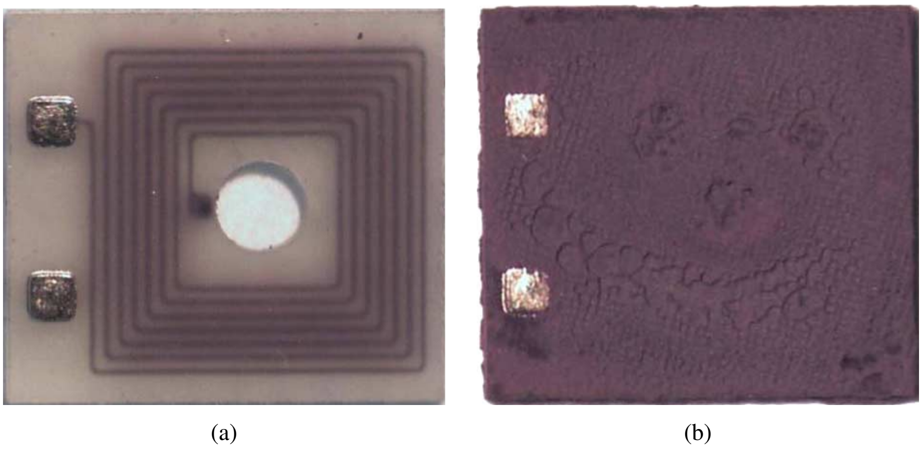

(a) (b)

Figure 2.18: (a) Picture of the 4-layer PCB with winding. (b) Picture of the prototype after the screen printing and curing of the paste [35].

rial is electroplated on the external layers and in the center hole. The material shows a relative permeability of 2000. However, the material conductivity is $5 \times 10^6\,\mathrm{S/m}$ which limits the core thickness to avoid eddy current effects, at 2 times the skin depth of the material ($10\,\mathrm{\mu m}$ at $1\,\mathrm{MHz}$). Better materials with a conductivity lower than that of $Ni_{80}Fe_{20}$ are possible. A patent [37] was deposed where the magnetic material comprises rhenium, cobalt and phosphorus. But even without eddy current effects, the rate to deposit magnetic material with electro-deposition still limits this process for thick inductors (more than a few ten of $\mathrm{\mu m}$).

These compliant materials constitute a good alternative to keep the embedding process compatible with the current PCB technology. But the performances tend to be lower than those of standard magnetic cores. With the aim to achieve the best performance in the best volume and to address higher power levels ($3\,\mathrm{kW}$), this thesis will focus on the embedding of large, solid, magnetic cores.

2.4 Passive, Peripheral and Driving Components

Beside active power devices and magnetic components, many other components are required to form a power converter (resistors, driver IC, capacitors ...). These components can be embedded inside the PCB with the same goals as for power chips. Embedding them in PCB could allow an overall miniaturization and improved electrical performance. A packaged component embedded inside the PCB is called an inserted component. A formed component is a component created using specific lay-

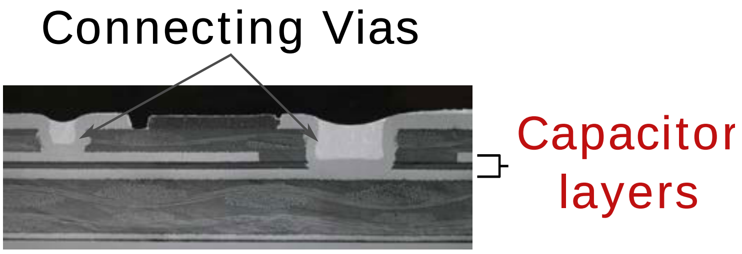


Figure 2.19: Micro-section of a formed capacitor with the connecting vias on the electrodes [8].

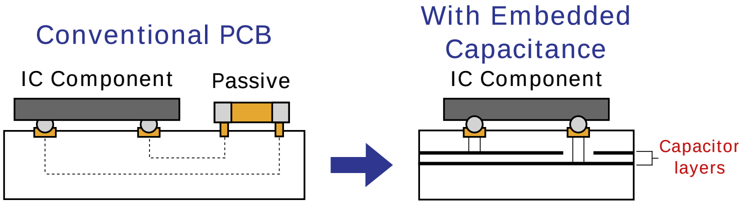


Figure 2.20: On the left, a drawing of a conventional PCB assembly with IC component and SMD capacitor mounted on top layer. On the right, the improved assembly using embedded capacitance material reducing the parasitic inductance between the two components [8].

ers inside the PCB stack-up (Figure 2.19) [8]. First, the embedding of resistors and capacitors as formed components are presented.

2.4.1 Formed Components

Formed Capacitor

A formed capacitor uses a capacitive film placed in the PCB stack-up between two copper foils as represented in figure 2.20 (right). This forms a single layer plane capacitor distributed over a large surface. The formed capacitor has a capacitance: $C = \epsilon \cdot \frac{S}{t}$, with ϵ the permittivity of the dielectric material, t its thickness and S the surface of the capacitor. The two main advantages of formed capacitors are the reduction of the parasitic inductance and to free some of the surface on the PCB by eliminating discrete capacitors.

With embedded capacitance materials, it is possible to obtain a capacitance density of $3.4\,\mathrm{nF/cm^2}$ with a voltage rating of $100\,\mathrm{V}$ (FaradFlex MC8T, Oak-Mitsu Technologies, [8]). For a higher voltage rating of $500\,\mathrm{V}$, the capacitance density will drop to $0.65\,\mathrm{nF/cm^2}$ (FaradFlex MC12TM, Oak-Mitsu Technologies). However,

Table 2.1: List of embedded capacitance material from the three major brands [8][38][39].

Capacitance Materials Name	Manufacturer	Voltage Rating (V)	Capacitance Density ($\mathrm{nF/cm^2}$)
MC8T	Oak-Mitsui Technologies	100	3.4 (at 1 MHz)
MC8TM	Oak-Mitsui Technologies	250	1.1 (at 1 MHz)
MC12TM	Oak-Mitsui Technologies	500	0.65 (at 1 MHz)
C4003	3M	10	6.2 (at 1 kHz)
C2006	3M	50	3.1 (at 1 kHz)
C1012	3M	100	1.6 (at 1 kHz)
HK04J25	Dupont	500	0.26

power electronics often require capacitance values of more than one micro-farad with voltage ratings which can reach hundreds of volts. At this voltage rating, the capacitance density is way inferior to that of SMD components. It will require a large footprint ($39 \times 39 = 1539\,\mathrm{cm^2}$) to obtain the desired $1\,\mu\mathrm{F}$ with a voltage rating of $500\,\mathrm{V}$ capacitor (to be compared with the capacitance density of discrete capacitors: $3508\,\mathrm{nF/cm^2}$ for a $1\,\mu\mathrm{F}$ $500\,\mathrm{V}$ 2220 SMD capacitor). Table 2.1 presents a short list of the three major brands of embedded capacitance materials. This technology is mostly used in high frequency applications to reduce the high speed switching noise. A micro-section of a formed capacitor is presented in figure 2.19.

Formed resistor

As with formed capacitors, formed resistors use a specific (resistive) layer laminated in the PCB. The manufacturing process is presented in figure 2.21. It uses a 3-step etching process to pattern the copper and the resistive layer, and then to open the copper pattern where the resistors must be formed. The formed resistor value is calculated using equation (2.1).

$$R = s \cdot \frac{L}{W} \tag{2.1}$$

where R is the resistance (Ohms), s is the sheet resistance (Ohms/square), L is the length of the resistor and W its width. It is important to note that the term "square" is dimensionless. Table 2.2 presents different available resistive materials.

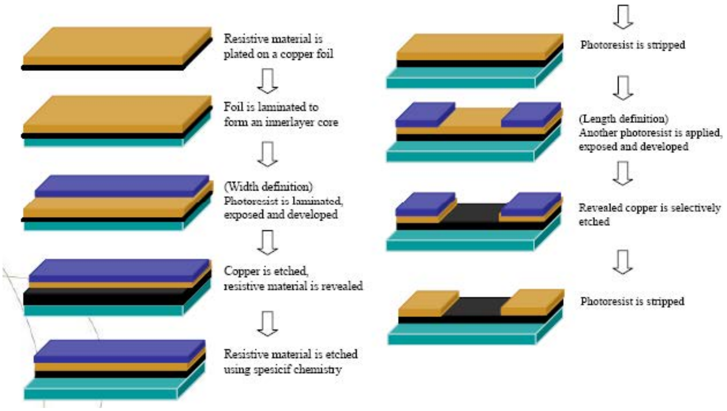


Figure 2.21: Manufacturing process for a formed resistor. [40]

Table 2.2: List of embedded resistance material [41][42].

Resistance Materials Name	Manufacturer	Sheet Resistance (Ω/sq)	Sheet Resistivity Tolerance (%)
TCR® NiCr	Ticer Technologies	25, 50, 100	±5
TCR® NCAS	Ticer Technologies	25, 50, 100, 250	±5
TCR® CrSiO	Ticer Technologies	1000	±7
Ohmegaply® RCM	Omega Technologies	10, 25, 40, 50, 100	±5
Ohmegaply® RCM	Omega Technologies	250	±10

2.4.2 Inserted components

An inserted component is a classic SMD device embedded inside the PCB. Inserted components present the advantage to offer a wide range of possibilities (Passives, ICs ...) with values which may be more suited to power electronics. The only limitation is the component thickness limited by the PCB thickness. An embedding process for small components (0201, 0402, 0603 cases) is going to be presented below.

The process is detailed in figure 2.22. It begins with a double-layer laminate. The double-layer laminate is manufactured as a standard PCB to form tracks and vias. The SMD components are soldered on the PCB using a standard process. A cavity is formed around each component using prepreg layers. The stack-up will depend of the embedded components. In particular, the resin content has to be calculated to fill all cavities with resin. And the layers thicknesses must be well controlled to avoid applying pressure on the embedded components. Then, the stack-up is laminated to form a solid assembly. The external copper layers can be patterned. More layers can be added successively as for a standard PCB [43].

Figure 2.23 represents a modular camera with a 32 bit image processor, 2 memory chips, 4 voltage regulators and 72 passives, all embedded in the PCB. In this example small passives are inserted [9]. In the modular camera, the embedded inductors use 0603 case ($1.6\times0.8\times0.8\,\mathrm{mm}^3$) while the embedded resistors are limited to 0201 case ($0.6\times0.3\times0.25\,\mathrm{mm}^3$). Both case sizes are used for capacitors. However, such small component sizes are rarely used in power electronics. Indeed, the power rating for a resistor or the voltage rating for a capacitor depends on the case size. For example, two pads with a voltage of $500\,\mathrm{V}$ should be spaced by $2.5\,\mathrm{mm}$ according to the IPC-2221B standard [44] which is larger than the distance between the components two pads for small cases such as 0603.

The process may have to be adapted for bigger cases (i.e. 1812 case). Inserted components are going to be used in this thesis because they allow us to meet the requirements imposed by the design. In our case, formed components would require too large footprints to achieve meaningful values.

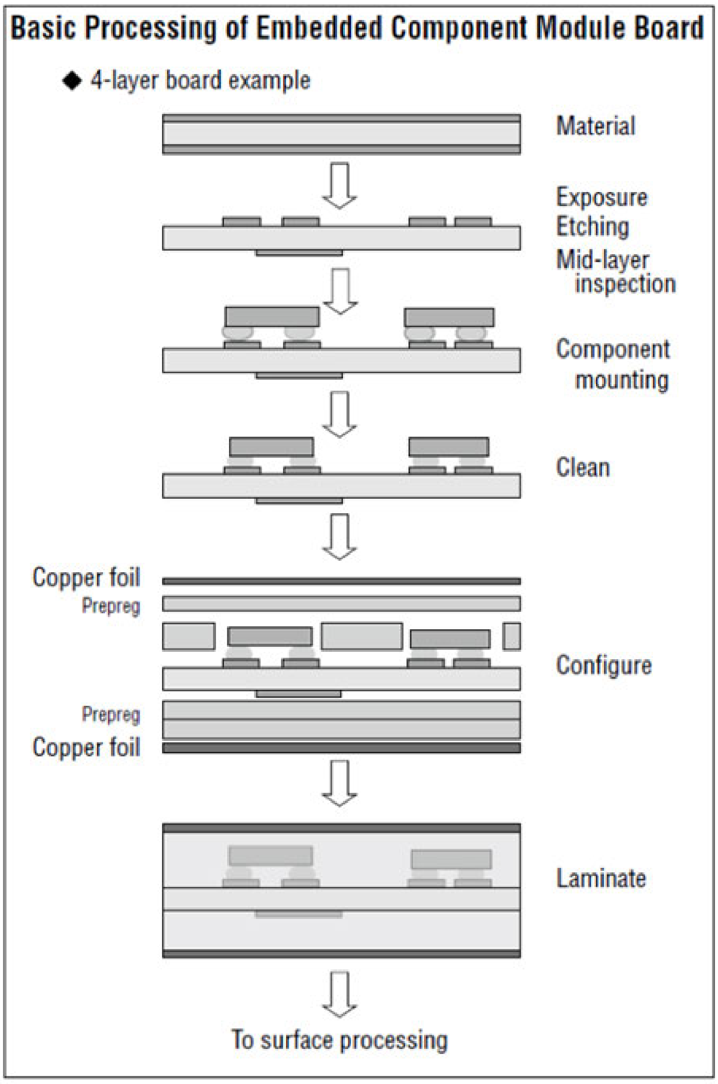


Figure 2.22: A process used for the embedding of SMD components inside a PCB [43].

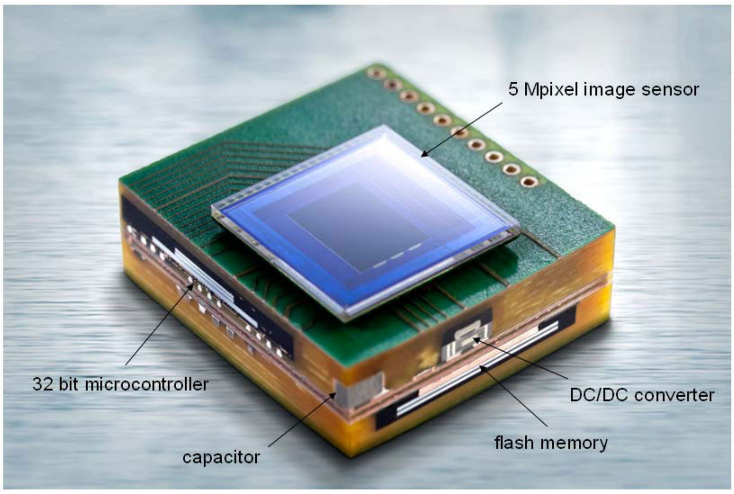


Figure 2.23: Cross section view of the Fraunhofer IZM modular camera with a 32 bit image processor, 2 memory chips, 4 voltage regulators and 72 passives, all embedded [9].

2.5 Thermal Management

Because power electronic converters are not perfect, they lose some of the energy they manage. The losses caused by the converter have to be evacuated to keep its components at an acceptable operating temperature.

Heat transfer can rely on three different mechanisms: conduction, convection and radiation. The thermal conduction is used for the heat transfer from the different heat sources to the system external surfaces. The thermal convection and radiation are used to evacuate the heat from the external surfaces to the environment.

2.5.1 Heat transfer in PCB

Conductive Materials

The thermal conductivity close to the heat source is important to spread the heat over a large area, thus avoiding "hot spots" and so reducing the thermal resistance of the system. Indeed, the thermal resistance of the heat path will decrease due to a more important cross section for the heat path in respect with equation (2.2).

$$R_{th} = \frac{e}{\lambda \cdot S} \tag{2.2}$$

where R_{th} is the thermal resistance, e is the thickness of the layer, λ is the thermal conductivity of the layer and S is the cross section of the heat path. The heat spreading close to the component allows to reduce the component temperature.

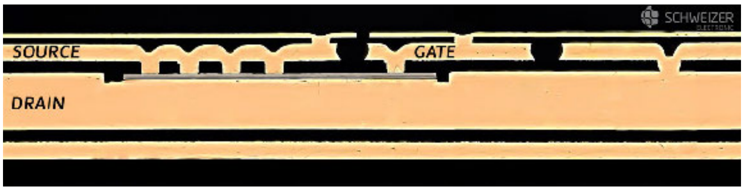


Figure 2.24: A cross section of a PCB technology called smart p^2 Pack®(Schweizer). The die is connected by silver sintering on the drain (Leadframe) inside a cavity. The top connections are done using microvias [10].

However, standard PCB substrate materials have poor thermal conductivities (around $0.4\,\mathrm{W/(m\cdot K)}$). In order to improve thermal management, research was done to increase the thermal conductivity of PCB materials. These improved materials use alumina (Al_2O_3) as a filler in the epoxy. Alumina has a thermal conductivity between 12 and $38.5\,\mathrm{W/(m\cdot K)}$ (depending on its grade). With a high percentage of filler, PCB material can have thermal conductivities up to $7\,\mathrm{W/(m\cdot K)}$ [45]. But this value is still far lower than the thermal conductivity of the copper ($390\,\mathrm{W/(m\cdot K)}$).

Thick copper conductors can provide better heat spreading. The p^2Pack® technology from Schweizer uses this idea. A leadframe, which is a several millimeters thick copper layer, is used. The dies are directly placed in cavities manufactured inside the leadframe. A PCB is laminated on the top for the other circuitry. A cross section of a version of the module is presented in the figure 2.24. This technology reduces significantly the thermal resistance compared to conventional DBC substrates. Also, the electro-plating process remplacing bond wire reduces on-resistance of the entire package. However, the major drawback is the die attach of the device inside the cavity due to the difference between the cavity height and the die thickness.

In [46], copper layers are also used to spread the heat. The $500\,\mathrm{W}$ converter using embedding technology uses two Insulated Metal Substrates (IMS). An IMS is an insulated layer sandwiched by two layers of metal. In this case, the IMS stack-up is $300\,\mathrm{\mu m}$ of copper, $100\,\mathrm{\mu m}$ of prepreg, $100\,\mathrm{\mu m}$ of copper. The IMSs are used as heat spreaders on both sides of a PCB with embedded dies. Figure 2.25 presents a photo of the IMS module. The new prototype is compared with a standard module. When attached to a heatsink on one side, the IMS module shows a thermal performance similar to that of the standard module, but with a reduced size. A double side cooling can also be used with the IMS module further reducing the thermal resistance. Depending on the die position, the IMS module thermal resistance with double sided cooling varies between $3.28\,\mathrm{K/W}$ and $5.34\,\mathrm{K/W}$.

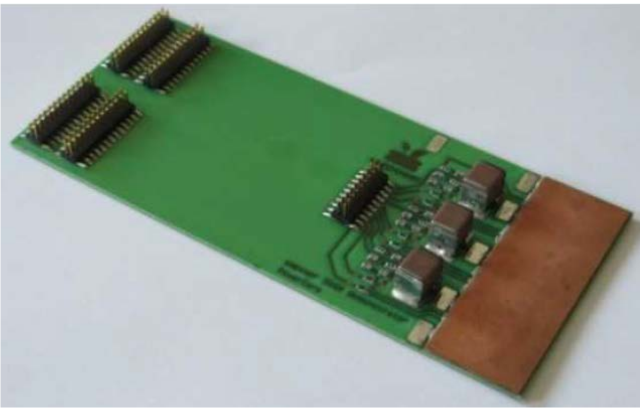


Figure 2.25: Module using two IMSs acting as heat spreaders for the embedded power modules [46].

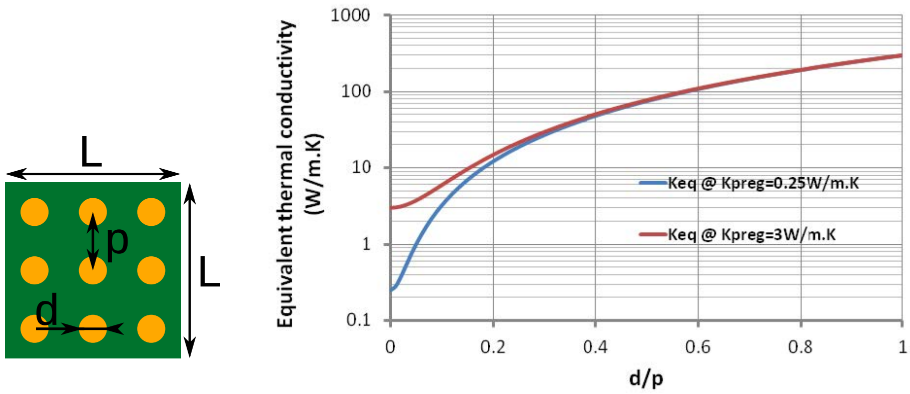
The thermal conductivity in a PCB can also be improved with vias. However, in this case, the thermal conductivity only increases in the vias axis. There is no radial heat spreading because of the thermal conductivity of the dielectric layer which separates vias. An analytical model of the equivalent conductivity of an area populated with vias is proposed in [18], using 1D thermal resistance. The model was validated by FEM simulation. Figure 2.26 presents a drawing of a via region with the different dimensions marked and the model results for two different prepreg materials. Equation 2.3 gives the equivalent thermal conductivity for a layer with vias.

$$\lambda_{eq} = \lambda_{PrePreg} \cdot \left[1 + \frac{\pi}{4} \cdot \frac{d_{via}^2}{p^2} \cdot \left(\frac{\lambda_{Copper}}{\lambda_{PrePreg}} - 1 \right) \right] \tag{2.3}$$

where λ is the thermal conductivity of the different materials, d_{via} is the diameter of the via and p is the distance between the center of two vias. The equivalent thermal conductivity of a via region is around 70-80 $\mathrm{W/(m \cdot K)}$ with standard design rules. The thickness of the electro-plated copper inside the vias has an important impact since it provides the preferential heat path. But copper electro-plating is a slow process so the walls of the vias cannot be thicker than some tens of micrometer.

Dual-Phase Systems

A more radical approach is to embed dual-phase cooling system such as heatpipes [11]. Heatpipes are closed and passive systems which rely on the phase change of a fluid to transfer the heat with a higher efficiency. A heatpipe has 3 essential parts: an evaporator, an adiabatic transport section and a condenser. The fluid is vaporized due to the heat at the evaporator. The vapor goes to the condenser through the adiabatic transport section due to the difference of pressure. At the condenser, fluid



(a) (b)

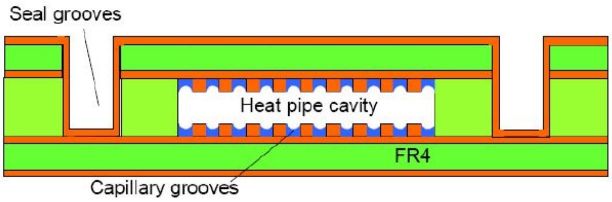
Figure 2.26: (a) A drawing of a via region with the dimensions used in the calculation. (b) Results of the analytical model for the equivalent thermal conductivity for two different prepreg materials [18]. Note that the d/p ratio cannot actually be more than 0.7 due to manufacturing restrictions.

condensates because of the lower temperature. The liquid goes back to the evaporator with the help of a capillary or wick structure.

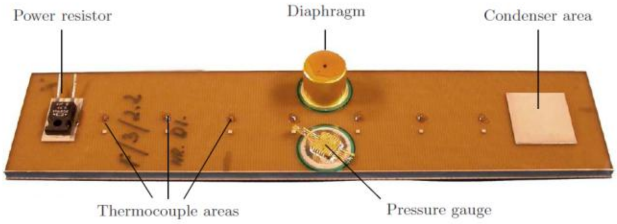
A heatpipe based on PCB technology is presented in [11]. The capillary structure is manufactured inside a cavity using standard PCB techniques. Another solution is the embedding of a copper foam. The cavity with the structure is closed and sealed. Figure 2.27 presents a drawing of the cross section of an integrated heatpipe inside a PCB and a picture of a prototype.

The prototype is able to transport up to $12\,\mathrm{W}$ giving an equivalent thermal conductivity of $4250\,\mathrm{W}/(\mathrm{m}\cdot\mathrm{K})$. This equivalent thermal conductivity gives an idea of the heat transfer efficiency of the heatpipe. But it cannot be considered and compared with the thermal conductivity of a solid since heatpipe is not based on thermal conduction. The heatpipe is limited in power due to the transport of the liquid in the wick structure. In case of high power, there will not be enough liquid at the evaporator (dry-out condition) resulting in a sudden and strong increase of the component temperature.

A development of the heatpipe system to 2D heat spreading is the thermal ground plane (TGP), also known as vapour chambers or flat heatpipe. It works as a heatpipe but it is manufactured in a flat two-dimensional configuration. Its thickness is small compared to the two others dimensions. This shape is more suited to thin systems as, for example, a PCB. The Defence Advanced Research Projects Agency (USA) launched a large campaign of research of thermal ground plane with several univer-



(a)



(b)

Figure 2.27: (a) A drawing of a cross section of a heatpipe integrated inside a PCB (b) Prototype of a heatpipe integrated inside a PCB. The losses are generated using the power resistor mounted on the evaporator. The diaphragm is used to fill the heatpipe [11].

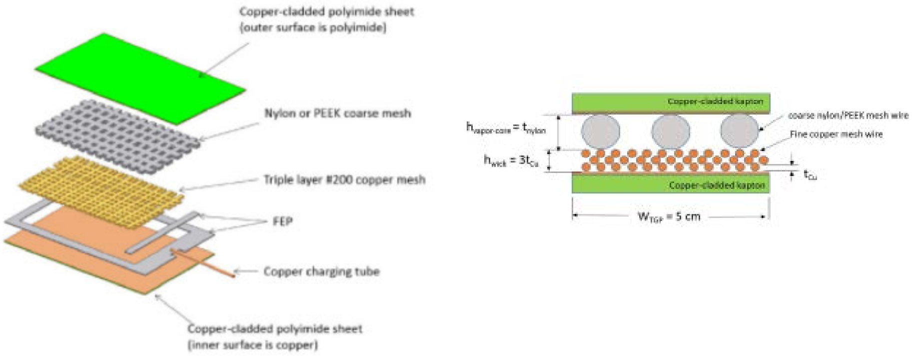
sities [47]. The university of Colorado proposed to use PCB technology to manufacture a thin and flexible thermal ground plane [48]. The choice of the PCB was to have light, low-cost and large scalability manufacturing. Figure 2.28 presents an exploded schematic of the stack-up used for the thermal ground plane (layer thickness is exaggerated for clarity) and a cross section of the stack-up. The TGP has a difference of temperature between condenser and evaporator of 28 °C at a power input of 27 W. As for the heatpipe, the limit of the TGP is the dry-out of the evaporator.

2.5.2 Heat Evacuation

Once the heat has been transferred to the boundary of the converter using conduction, it is removed thanks to convection and radiation from the external surface. The thermal resistance R_{th} between the converter and the environment is defined by equation (2.4).

$$R_{th} = S \cdot h \tag{2.4}$$

where S is the converter surface area in contact with the environment and h is the heat transfer coefficient. The thermal resistance can be decreased by increasing the surface areas with the help of a heatsink. Figure 2.29 shows heat transfer coefficients achievable for different cooling technologies. The convection can use air or liquid and can be natural or forced (in this case the fluid is put in motion with an external



(a) (b)

Figure 2.28: (a) Exploded schematic of the flexible TGP where the thicknesses are exaggerated for clarity. (b) Detailed schematic of the cross section of the TGP [48].

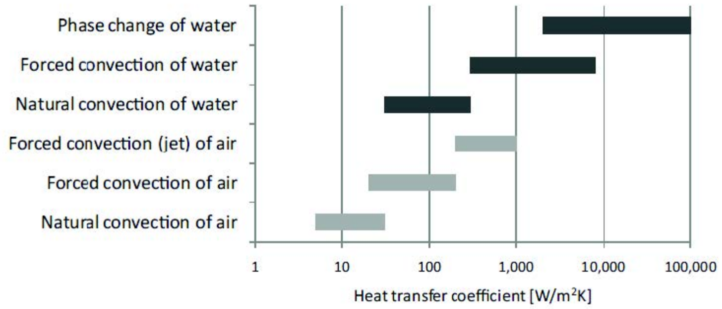
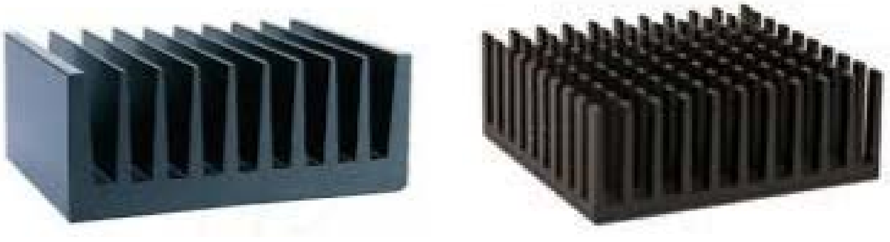


Figure 2.29: Range of heat transfer coefficient for different cooling technologies [49].

system such as a pump). Air cooling shows lower performance than liquid cooling. However, air cooling is easier to implement than liquid cooling. Using the same fluid, a forced convection system shows better heat transfer than a natural convection system. However, an external system like a fan or a pump is then necessary.

Heatsinks can use different shapes and materials. They are mostly made from aluminum or copper. Copper heatsinks show better performance due to better thermal conductivity but they weight and cost more than aluminum heatsinks. Industrial products mostly use aluminum.

In this thesis, we will use thermal natural convection and radiation in the ambient air. The choice was made to avoid the use of an external system which increases the complexity the implementation of the converter. The theoretical models for both heat transfer types are well known and will be presented.



(a) (b)

Figure 2.30: Different shapes of heatsink: (a) straight fins, (b) pin fins.

For the radiation, with hypotheses of black external surface, the radiated flux Φ is calculated using equation (2.5).

$$\Phi = \epsilon \cdot S \cdot \sigma \cdot (T^4 - T_{amb}^4) \tag{2.5}$$

where $\sigma = 5.67 \times 10^{-8}\,\mathrm{W/(m^2 \cdot K^4)}$ is the Stefan-Boltzmann constant, ϵ is the emissivity of the radiating material, S is the radiating surface, T and T_{amb} are respectively the temperature of the radiating surface and that of the environment. However, heatsinks have a complex shape (figure 2.30). In order to take into account surface-to-surface radiation for a heatsink, the model has to be adjusted as developed in [50]. The form factor to adapt the model will be presented in chapter 4.

Aluminum has an emissivity of 0.1, which gives poor performance from a radiation point of view. A surface treatment is then used to increase emissivity. The anodizing is an electrolytic passivation process used to increase the thickness of the natural oxide layer on the surface of metal parts. With this oxide layer, the heatsink has an emissivity of 0.85.

Convection models depend on the system orientation because natural convection is based on the mass movement due to the temperature-dependent fluid density. Even for a single configuration (vertical rectangular fins), a review of the literature presented in [51] shows more that 8 models for natural convective heat transfer. The model used in this thesis will be presented in chapter 4.

Heatsinks use different shapes in order to maximize the contact area with the environment. The off-the-shelf heatsinks have straight fin or pin fin. Figure 2.30 presents a picture for both heatsink shapes. In natural convection, pin fin heatsink presents better performance than straight fin heatsink [52]. However, straight fin heatsink are preferred in industrial product due to their low manufacturing cost (they are produced by extrusion).

The design of a heatsink is a complex task but can allow important volume gain since the thermal management system takes a large part of converter volume. Com-

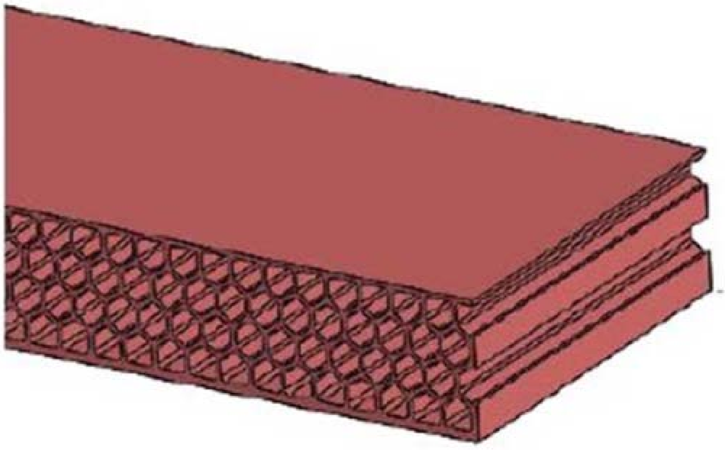


Figure 2.31: Honeycomb structure heatsink minimizes the components temperature [53].

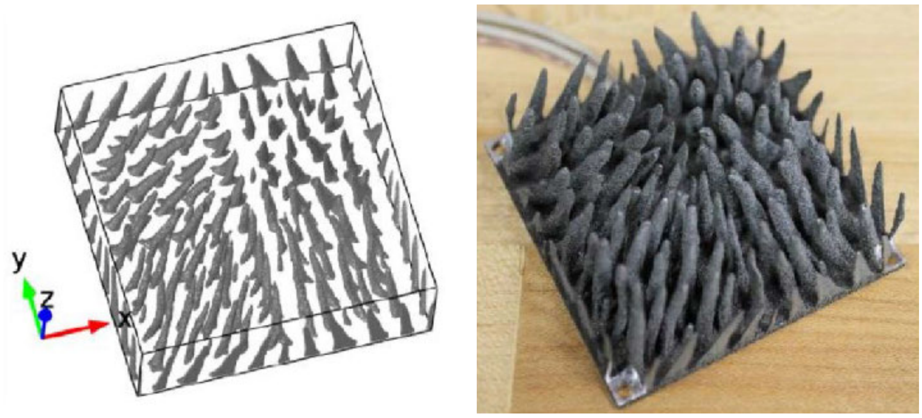
plex shapes can be obtained to improve heat transfer performance with an increase of the cost. They are used in highly critical applications. In [53], a comparison of heatsink shapes is made to reduce the hot spot temperature. The best results are obtained for a honeycomb heatsink (Figure 2.31).

In [54], a heatsink optimization is presented. The result is prototyped using 3D printing. 3D printing is an additive manufacturing in which the material is solidified layer by layer to create a 3D object. Figure 2.32 presents the result of the optimization and the prototype. The heatsink has performance equivalent to similar standard heatsinks (straight or pin fins) but need a smaller fan due to a lower pressure drop.

2.5.3 Thermal Interface Materials

In most cases, a dedicated thermal interface material (TIM) is required between the surface of the converter and the baseplate of the heatsink. Indeed, because of their surface roughness, the contact of two hard surfaces forms a quantity of insulating voids at the interface. These air-gaps create a thermal insulating barrier increasing the thermal resistance. The TIM will fill the voids to improve the thermal path. As with the dielectric layers of the PCB, the TIM represents a weak point for the thermal management due to its low thermal conductivity.

A generally used TIM is thermal grease or paste. Thermal grease consists of a liquid matrix with a large volume fraction of thermally conductive filler (usually electrically insulated). The thermal pastes have a conductivity of 2 to $8\,\mathrm{W/(m \cdot K)}$.



(a) (b)

Figure 2.32: (a) Result of the optimization. (b) Prototype of the optimized heatsink realized by 3D printing [54].

The application of thermal paste can be quite messy. It is mostly used to fill small gaps.

Thermals pads are also used as TIM. Thermals pads are under sheet form. They are not as effective as a thin-layer of thermal grease ($1.8\,\mathrm{W/(m\cdot K)}$ with thickness of $200\,\mathrm{\mu m}$, Sil-Pad 1500ST, Bergquist). Thermal pads can be found with adhesive layers to simplify the positioning. However, this added adhesive layer represents a thermal resistance. An external clamping system is preferable to apply a well controlled and well distributed pressure. An innovating thermal pad material is Pyrolytic Graphite Sheet (PGS). With an aim of reducing the components temperature, it is essential to increase the cross section of the heat path before it crosses low thermal conductivity materials as seen with some solutions presented previously. In cases in which it is impossible, the PGS can be used. It has a z-axis (through the thickness) thermal conductivity of "only" $15\,\mathrm{W/(m\cdot K)}$ for a $25\,\mathrm{\mu m}$-thin layer, which is already better than most standard TIMs. But most important, its x- and y-axis thermal conductivity can go up to $1500\,\mathrm{W/(m\cdot K)}$, which is useful for heat spreading. The structure giving this property to the PGS, carbon atoms arranged as honeycomb, is shown in figure 2.33.

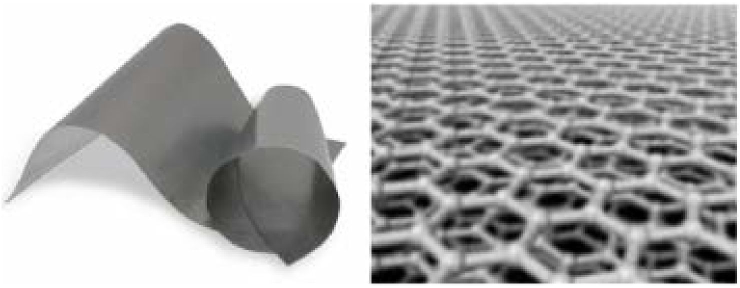


Figure 2.33: Photograph of a Pyrolylic Graphite Sheet with a zoom on this structure [55].

2.6 Conclusion

In this chapter, I gave a review of PCB technology, with a special focus on component embedding, which will be used throughout the thesis. It allows to obtain a converter with the best efficiency in the smallest volume possible. The embedding technology is well known by PCB manufacturers for the dies. For SMT components, it is only used for small cases. The embedding of magnetic components is limited to low power or/and high frequency applications. The embedding of dual-phase system or better materials for the thermal management are still in the research phase.

The embedding technology which will be used for the dies uses interconnection with microvias on both sides. This interconnection method gives a good thermal conductivity. The embedding for large solid magnetic cores will be studied to see the potential of such solution for medium power application. The embedding of large discrete component (case 1812) will also be studied because it corresponds to component sizes used in power electronics.

In the second part of the chapter, we discussed the thermal management solutions. Indeed, in their classical form, PCB substrates have poor thermal conductivity. Specific features (copper inlays, vias, high conductivity materials) are required for power electronics. Suitable thermal interfaces and heatsinks are also required. In this thesis, the thermal management will use natural convection.

The objective of this thesis is the implementation of an AC/DC bidirectional converter using the PCB embedding technology. The aim is to study and to discuss the interest of such technology on each component. The converter is also optimized to achieve the smallest volume. The chapter 3 presents the project to which this thesis contributes.

Chapter 3

Design of an integrated converter

3.1 Framework of the study

This thesis is part of a project aimed at the design and the realization of an AC/DC bidirectional converter. These power converters are commonly used in grid connected applications such as an electrical vehicle on-board battery charger [56], which is the application case being investigated here. While the present thesis is mainly dedicated to the implementation of the converter using PCB embedding technology, another thesis (J. Le Leslé [57]) is focused on defining the optimal circuit topology, using the most suitable components. As part of the optimization process relies on technological parameters, and because the development of an optimization procedure for the magnetic components (Section 3.2) was done in this thesis, some information are given here regarding circuit design, which was done in the other thesis (Section 3.1.3).

3.1.1 Specifications

The converter specifications are presented in table 3.1. On the AC side, an RMS voltage of $230\,\mathrm{V}$ with an RMS current of $15\,\mathrm{A}$, which corresponds to the domestic electrical grid, is defined. On the DC side, the voltage wanted is $400\,\mathrm{V}$, which corresponds to the battery voltage for a current of $8.25\,\mathrm{A}$ (Controlled output voltage). The output power is $3.3\,\mathrm{kW}$. The converter should have a volume of less than $1\,\mathrm{L}$ (considering the box volume, i.e. the volume of the smallest rectangular box which can enclose the converter). This is the main challenge in the project which translates into a power density objective of $3.3\,\mathrm{kW/L}$ all-inclusive. The minimum efficiency at nominal power was fixed to $97\,\%$. In addition, thermal management is to rely on natural convection only.

Table 3.1: Specification of the AC/DC bidirectional converter.

$V_{IN_{RMS}}$(AC)	$230\,V$
$I_{IN_{RMS}}$(AC)	$15\,A$
V_{OUT}(DC)	$400\,V$
I_{OUT}(DC)	$8.25\,A$
P_{OUT}	$3.3\,kW$
Volume	$1\,L$
η	$97\,\%$
Ambient Temperature	$-40\,°C$ to $60\,°C$
E.M.C	EN55001 Class B conducted EMI

3.1.2 Project Management

With the objective to present a prototype which meets the specification, the project was separated into two work packages referred to as "Topology" and "Implementation". The "Topology" work is the comparison of topologies and the optimization of the chosen topology by the selection of the most suited components. The "Implementation" work is the implementation of this topology and components using PCB technology with a dedicated thermal management system. The present thesis corresponds to the "Implementation". The optimization procedure results from a collaboration between the two thesis.

3.1.3 Topology

Several topologies were compared in the "Topology" work package. As a result (Figure 3.1), it was chosen to use an interleaved full bridge power factor corrector (PFC). The number of cells (N) used in the PFC is a parameter of the converter optimization procedure. A PFC cell has a leg switching at high frequency ($f_{sw_{PFC}}$) (which is the second parameter of the converter optimization procedure) and a leg switching at the grid frequency ($50\,Hz$). The third parameter is the ripple allowed on the line (I_s). An EMI filter is placed on the AC side of the PFC to comply with the harmonic standard (EN 55001 Class B conducted EMI). The choice of an interleaved PFC was done to reduce the size of the EMI filter [58]. The EMI filter is used for the common mode (CM) and the differential mode (DM) filtering. Both parts can be composed of several stages ($N_{f_{CM}}$ and $N_{f_{DM}}$ respectively for CM and DM which are also two parameters for the converter optimization procedure). On the DC side, a power pul-

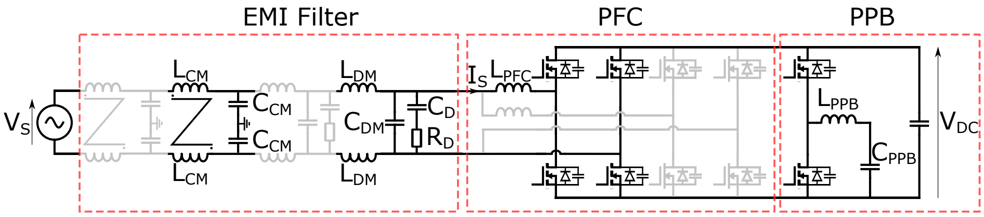


Figure 3.1: Circuit diagram of the chosen topology cell. The topology includes an EMI filter, a power factor corrector (PFC) and an "electronic capacitor" (PPB). The implementation can use several interleaved cells for the PFC and several DM and/or CM stages for the EMI filter (Grey).

sating buffer (PPB), also called electronic capacitor, is used for the DC filtering. The PPB is used to obtain a better power density [59]. The optimization parameters of the PPB are the switching frequency ($f_{sw_{PBB}}$), the inductor value (L_{PPB}) and the minimum capacitor bank voltage ($V_{C_{min}}$).

3.1.4 Optimization

As explained above, the main objective of the optimization process is to achieve the best power density while meeting all other specifications. Firstly, the PFC and the EMI filter are optimized together because the PFC input current ripple has a strong impact on the EMI filter. A smaller PFC inductor value allows to reduce the volume of the PFC. But, it also requires more attenuation from the EMI filter, which leads to an increase of the filter volume. An optimization of the PFC followed by an optimization of EMI filter would lead to an globally non-optimal solution. On the contrary, the third stage of the converter, the PPB is relatively independent from the filter and the PFC and can be optimized separately (to reduce the complexity of the optimization process).

Both power density and efficiency are considered during the optimization process. With those two parameters, the optimization produces a Pareto front [28], which is the set of designs for which one parameter cannot be improved without degrading the other. This optimization method is based on the calculation of the solutions for all input combinations. Then, the solution which fits the best the specification is chosen. In our case, the converter designs are compared with the trade-off between efficiency and power density. The power density is calculated using the sum of each component box volume.

Power Factor Corrector and EMI Filter

Firstly, the PFC and the EMI filter are optimized together. The optimization flowchart is presented in figure 3.2. For the optimization, the inputs are the number of interleaved PFC cells (N), the switching frequency (f_{sw}), the current ripple (ΔI), the number of stages for the common mode (CM) EMI filter ($N_{f_{CM}}$) and the number of stages for the differential mode (DM) EMI filter ($N_{f_{DM}}$). The number of interleaved cells varies from 2 to 5. The switching frequency varies from $140\,\mathrm{kHz}$ to $260\,\mathrm{kHz}$ by steps of $40\,\mathrm{kHz}$. The current ripple varies from $2\,\mathrm{A}$ to $12\,\mathrm{A}$ by steps of $2\,\mathrm{A}$. The number of stages for EMI filter, both CM and DM, varies from 2 to 4. Then, the waveforms are calculated analytically for one input combination [58].

Then, the optimization script is separated into three parts. Firstly, PFC semiconductor devices are selected. Then, the optimization is done for the capacitors of the EMI filter. In the third part, the inductors of the PFC and the EMI filter are optimized.

Semiconductor

Starting from the theoretical waveforms generated from the analytical model above, switches losses are calculated for various transistors (SiC MOSFETs of various ratings). This takes into account the soft switching under zero voltage switching (ZVS) condition when it occurs ($E_{sw_{ON}}$ is considered negligible / $E_{sw_{OFF}}$ is calculated using equation 3.2). The switches volume is the addition of the box volume of the corresponding gate driver components and that of the transistors. The switches are compared with respect to losses. The chosen switch is the one with the lowest losses. In order to use PCB die embedding, the semiconductor database is restricted to SiC bare dies from Wolfspeed (which are the only devices we were able to source with a suitable copper finish, as discussed in chapter 2). The drawback is the limitation of the database to $900\,\mathrm{V}$ and $1200\,\mathrm{V}$ MOSFETs which are not ideal for our voltage range. The procedure also considers the association of several switches in parallel. The semiconductors losses calculation is separated for conduction and switching losses. The conduction losses calculation uses the simulated current waveform for each converter design and the on-state resistance given in the component datasheet. The parameters are taken from the datasheet considering a $150\,^{\circ}\mathrm{C}$ junction temperature (worst case). Turn OFF and turn ON energies are calculated with equations 3.1 and 3.2 [60], respectively.

$$E_{sw_{ON}} = \frac{1}{2} \cdot V_{DC} \cdot I_D \cdot t_r + \frac{1}{2} \cdot C_{oss} \cdot V_{DC}^2 + Q_{rr} \cdot V_{DC} \tag{3.1}$$

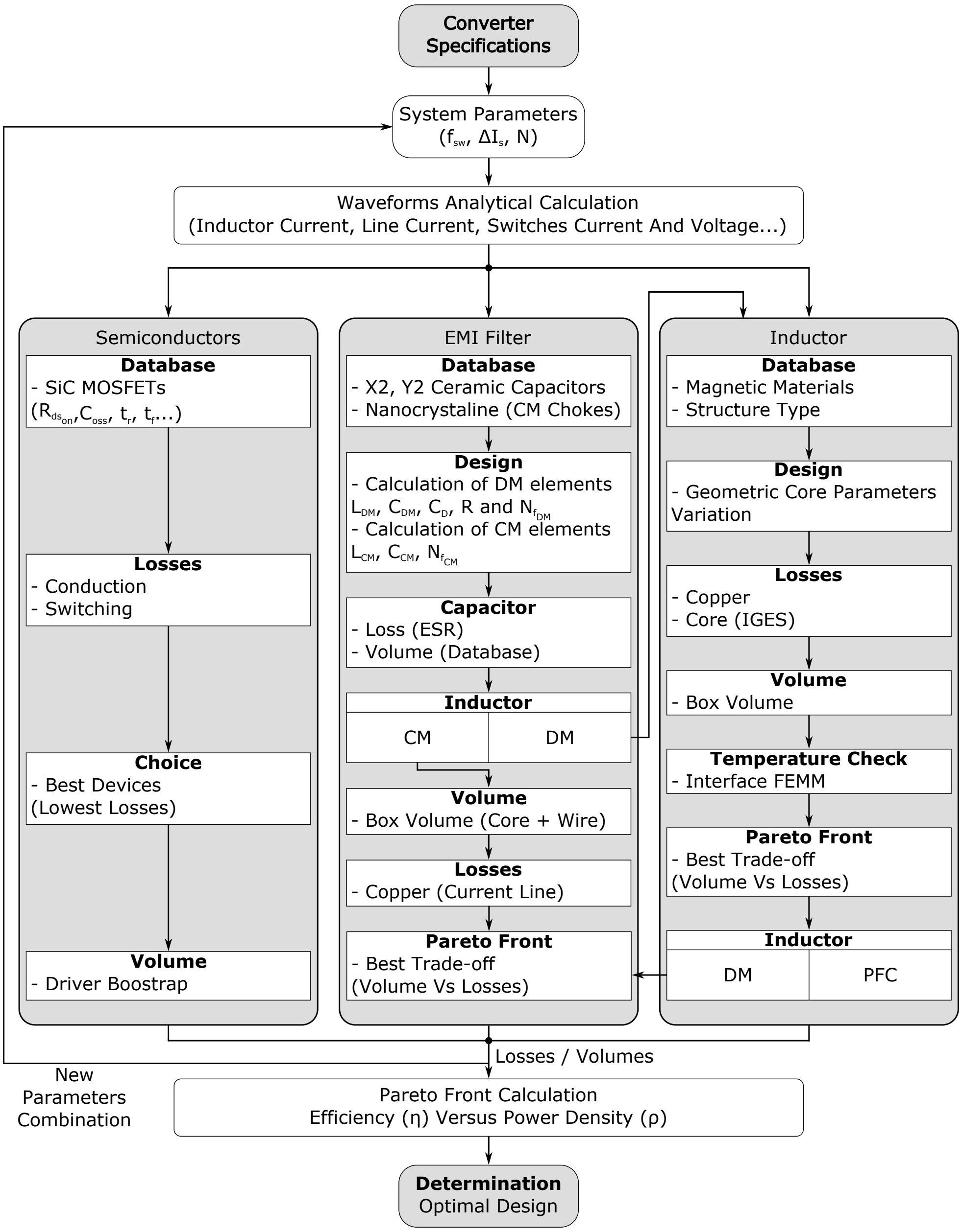


Figure 3.2: Flowchart of the optimization process for the PFC and the EMI filter [58].

$$E_{sw_{OFF}} = \frac{1}{2} \cdot V_{DC} \cdot I_D \cdot t_f \tag{3.2}$$

with t_r the rise time, t_f the fall time, C_{oss} the output capacitance and Q_{rr} the reverse recovery of body diodes.

Capacitor

The EMI filter optimization begins with capacitors. Indeed, the energy storage density is higher for capacitors than inductors so the EMI filter capacitor value is maximized. For the common mode (CM) filtering stage, the use of Y2 class capacitors is imposed for security. Class-Y capacitors are also known as the "line to ground capacitors". The maximum allowed capacitor value is calculated according to the maximal earth current allowed ($3.5\,\mathrm{mA}$). The maximum capacitor is calculated using equation (3.3).

$$C_{CM_{max}} = \frac{I_{Earth_{Max}}}{V_{IN_{RMS}} \cdot \omega_{IN}} = 45.6\,\mathrm{nF} \tag{3.3}$$

where $I_{Earth_{Max}}$ is the maximum current to the earth ($3.5\,\mathrm{mA}$), $V_{IN_{RMS}}$ is the RMS voltage on the grid side ($230\,\mathrm{V}$) and ω_{IN} is the angular frequency of the input voltage ($50\,\mathrm{Hz} \times 2\pi$). The capacitor value is then distributed (not equally) according to the number of CM filter stages. The value of the maximum capacitance is split between each stage of the CM EMI filter with the largest capacitor value close to the converter and the lowest capacitor value close to the grid side.

For the differential mode filtering, the use of X2 capacitors is imposed for security. Class-X capacitors are also known as the "across the line capacitor".The maximum capacitor value is calculated to have a minimal power factor of $cos\phi$= 0.995 for the worst case which is when the converter operates at $10\,\%$ of its full load ($P_{MIN} = 330\,\mathrm{W}$), which is the minimum power in operation. It gives a reactive power of Q_{max}= $33\,\mathrm{VAr}$. The maximum capacitance value is calculated using the equation (3.4).

$$C_{DM_{max}} = \frac{Q_{max}}{V_{IN_{RMS}}^2 \cdot \omega_{IN}} = 2\,\mathrm{\mu F} \tag{3.4}$$

As for CM capacitor, the value of the maximum capacitance is split between each stage of the DM EMI filter with the largest capacitor value close to the converter and the lowest capacitor value close to the grid side with the aim to obtain an equal current ripple in capacitors of each stage. Also, each stage contains a filtering capacitor and a damping capacitor which are considered of identical values. The capacitor losses are calculated using the simulated current waveform and a curve fitting of the equivalent series resistance (ESR) of the capacitor over the range from $50\,\mathrm{Hz}$ to $1\,\mathrm{MHz}$ given in the component datasheet. The final step is the determination of damping resistors, for which Middlebrook's theorem is used [60].

Inductor

Once the capacitors have been selected, the inductors of the CM and DM filter can be chosen to achieve the required attenuation. The required attenuation is the difference between the EMI standards and the estimated noise peak value. The noise peak is calculated by modeling the LISN and the current is calculated analytically (Estimations of the parasitic capacitors and switching times are used). With the required attenuation, the dimensioning frequency and the CM EMI capacitor values, the value for the CM choke can be determined using equation (3.5)

$$L_{CM} = \frac{1}{2} \cdot \sqrt[N_f]{\frac{10^{Att_{req}/20}}{(2\pi f_D)^{2N_f} \cdot \prod C_{CM}}} \tag{3.5}$$

where L_{CM} is the inductance value of each CM EMI filter inductor, Att_{req} is the required attenuation and f_D is the dimensioning frequency. The latter is the first harmonic in the frequency range of the EMI standard. The inductors in each stage are coupled to cancel the flux in the core from the DM current [61].

The CM chokes are designed using a database with standard nanocrystalline cores. The number of turns is calculated according to the required inductance. The saturation is checked with the maximum induction from the datasheet. Losses are calculated with the current flowing through the windings. Natural convection is considered for CM chokes with a limit of temperature increase fixed to $40\,°\mathrm{C}$.

As for CM inductors, DM inductors value can be calculated according to the required attenuation, dimensioning frequency and DM filter capacitances using the equation (3.6).

$$L_{DM} = \frac{1}{2} \cdot \sqrt[N_f]{\frac{10^{Att_{req}/20}}{(2\pi f_D)^{2N_f} \cdot \prod C_{DM}}} \tag{3.6}$$

where L_{DM} is the inductance value of each DM EMI filter inductor, Att_{req} is the required attenuation and f_D is the dimensioning frequency. The inductors for the DM EMI filter and the PFC are using PCB embedding. The design script is presented in the section 3.2.

Optimized Topology

Each combination of input gives a solution with a corresponding efficiency and a power density. When these solutions are plotted on a graph, the best solutions are forming the Pareto front (Figure 3.3). The optimized solution for the PFC and the

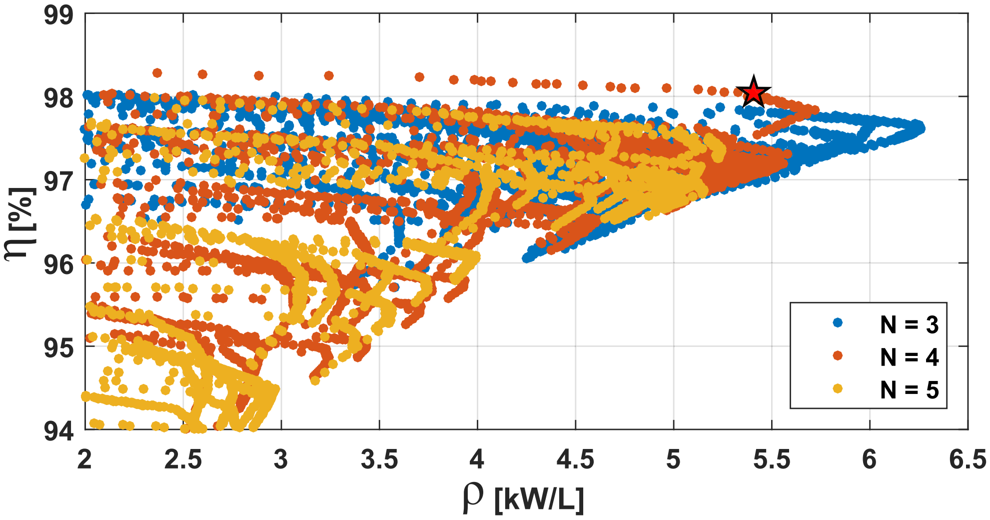


Figure 3.3: Results of the optimization procedure for the PFC and EMI filter. Each combination of input gives a solution with a corresponding efficiency and a power density.

EMI filter is the solution which presents the best power density with an efficiency above $98\,\%$. For example, the converter that will be described further (PFC and EMI filter stages) is predicted to have an efficiency of $98.01\,\%$ for a power density of $5.41\,\mathrm{kW/dm^3}$. The converter uses 4 interleaved cells with a switching frequency of $180\,\mathrm{kHz}$ and a current ripple of $4\,\mathrm{A}$. The DM EMI filter is composed of 4 stages while the CM EMI filter is composed of 3 stages. Some details of the converter are given in table 3.2 with the corresponding volumes and losses for each component group. The heatsink volume is calculated using a coefficient of $5\,\mathrm{cm^3/W}$ (coarse estimation).

Power Pulsating Buffer

In a second step, the PPB design is optimized. Two different topologies for the PPB were studied: a buck or a boost topology. In the boost topology, the voltage across the buffer capacitor is higher than the DC voltage. Thus, the semiconductors in the power buffer do not have the same voltage rating as in the PFC stage. The selection is made upon the voltage across the buffer capacitors. So, the buck topology was chosen to keep a voltage of the buffer capacitor lower than the DC bus voltage. Consequently, the same semiconductor devices can be used for the PFC and the PPB. As for the PFC and the EMI filter, the optimization design can be separated into three parts: Semiconductors, Capacitor and Inductor. The flowchart is presented in figure 3.4. The inputs of the optimization script are the switching frequency (f_{sw}), the inductor

Table 3.2: Details of the optimized power factor corrector (PFC) and EMI filter.

General	
η	$98.01\,\%$
ρ	$5.41\,\mathrm{kW/dm^3}$
N	4
f_{sw}	$180\,\mathrm{kHz}$
ΔI	$4\,\mathrm{A}$
Nb EMI filter stages	$N_{f_{DM}}$=4, $N_{f_{CM}}$=3
Volume	
Total	$609.5\,\mathrm{cm^3}$
Inductor PFC	$59.5\,\mathrm{cm^3}$
DM filter	$151.5\,\mathrm{cm^3}$
CM filter	$61.5\,\mathrm{cm^3}$
Switch and Driver	$8\,\mathrm{cm^3}$
Heatsink	$329\,\mathrm{cm^3}$
Losses	
Total	$66\,\mathrm{W}$
Inductor PFC	$33\,\mathrm{W}$
Switch	$17\,\mathrm{W}$
EMI filter (CM and DM)	$16\,\mathrm{W}$

value (L_{PPB}) and the minimum capacitor bank voltage (V_{Min}). The maximal voltage is limited to $0.93 \cdot V_{DC}$ to avoid control issues [59]. The switching frequency varies from $40\,\text{kHz}$ to $220\,\text{kHz}$ by $40\,\text{kHz}$ steps. The inductor value varies from $10\,\mu\text{H}$ to $80\,\mu\text{H}$ by $10\,\mu\text{H}$ steps. The minimum capacitor bank voltage varies from $50\,\text{V}$ to $300\,\text{V}$ by $50\,\text{V}$ steps. However, the higher the voltage variation across the capacitor, the higher the current flowing through the inductor, which impacts its conduction losses. This is taken into account in the design because the allowed voltage swing is one of the input parameters of the optimization procedure.

Semiconductor

As for the first optimization, the waveforms in the PPB are calculated analytically. Switch current and voltage waveforms are used to calculate losses. Due to the use of small bare dies, the semiconductor volume is actually assumed to be that of its driver circuit. The switch which is found to dissipate the fewer losses is chosen. The losses are calculated as presented previously.

Capacitor

The capacitor value can be determined from the PFC rated power P_{DC} ($3.3\,\text{kW}$ as only one PPB stage is considered here) and the voltage excursion allowed across the capacitor. The capacitor bank is designed using the equation (3.7)

$$C_{PPB} = \frac{2 \cdot P_{DC}}{\left(V_{PPBmax}^2 - V_{PPBmin}^2\right) \cdot \omega_{IN}} \tag{3.7}$$

where C_{PPB} is the capacitor value, ω_{IN} is the angular frequency of the grid and V_{PPB} is the voltage across the capacitor bank.

Several capacitor technologies were studied. The capacitors are compared with their capacitance density (nF/cm^3) with a DC bias of $370\,\text{V}$, which is a first approximation of the DC voltage of the capacitor bank. They should also have an acceptable current ripple per capacitance superior to $0.0271\,\text{A}/\mu\text{F}$ at $100\,\text{Hz}$. Table 3.3 presents the comparison. The capacitor bank is made of ceramic capacitors to obtain a high power density.

The X6S capacitors have the best capacitance density with an acceptable current per capacitance so it is the best candidate. Then, the volume is calculated using the box volume of the capacitor bank. The capacitor losses are calculated using the simulated current waveform and a curve fitting of the equivalent series resistance (ESR) of the capacitor over the range from $50\,\text{Hz}$ to $1\,\text{MHz}$ given in the component datasheet.

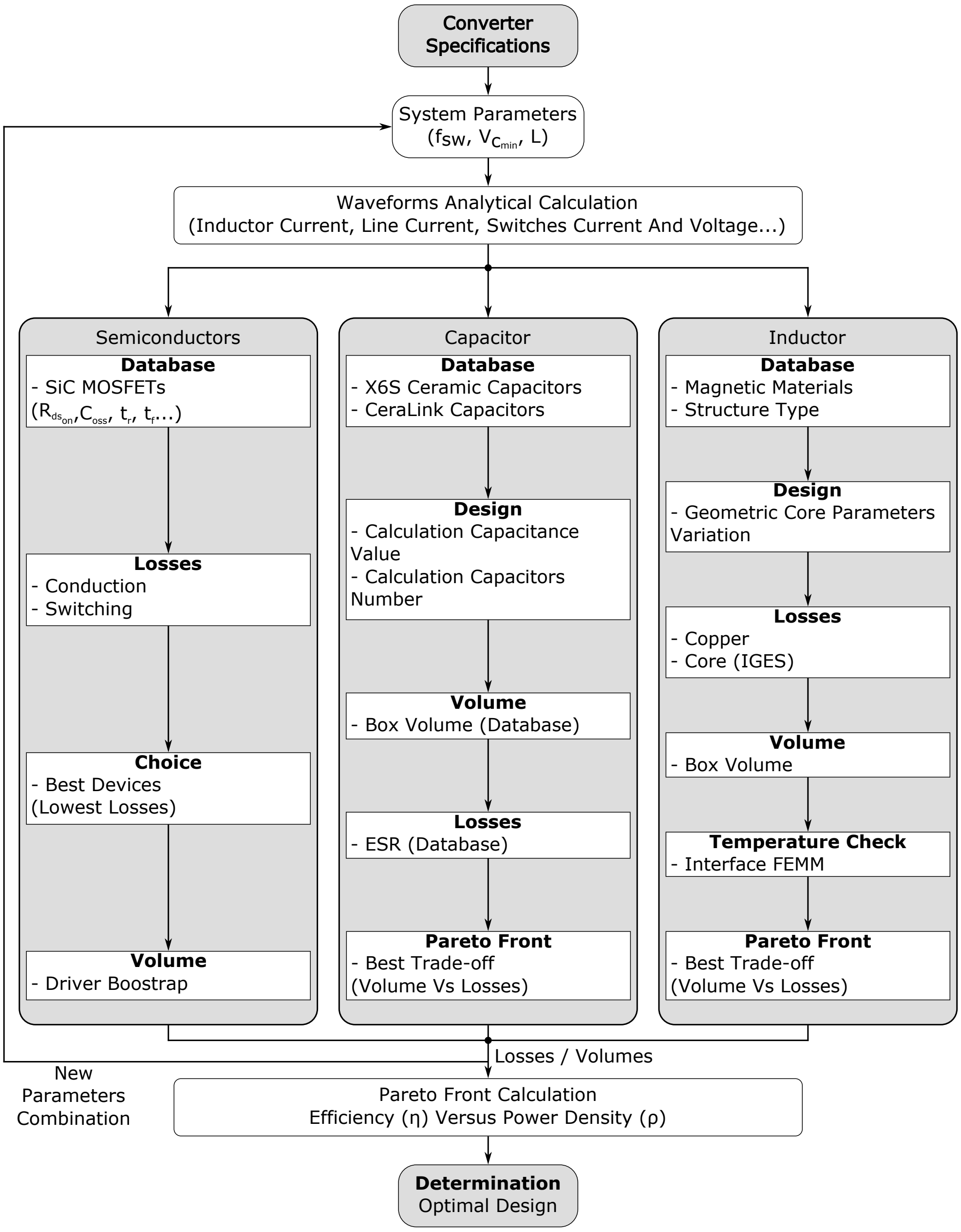


Figure 3.4: Flowchart of the optimization process for the power pulsating buffer (electronic capacitor) [59].

Table 3.3: Comparison of the capacitor technologies according to the current per capacitance and the capacitance density.

	Current Per Capacitance ($\mathrm{A/\mu F}$)	Capacitance Density ($\mathrm{nF/cm^3}$)
X6S Capacitor (450 V)	0.39	6531
X7R Capacitor (500 V)	1.45	1561
CeraLink Capacitor (500 V)	0.97	1469

Inductor

As for the PFC and the EMI filter, the PPB inductor is going to use PCB embedding. Details regarding the actual inductor design script are presented in section 3.2.

Optimized Topology

As for the first script, the power density is calculated using the sum of the box volume of each component. As the PPB is a 2-terminal converter connected in parallel to the PFC output its efficiency cannot be computed as $\frac{P_{OUT}}{P_{IN}}$. Efficiency η is thus defined by the equation (3.8).

$$\eta = \frac{P_{DC} - \sum P_{Loss}}{P_{DC}} \tag{3.8}$$

where P_{DC} is the PFC rated power ($3.3\,\mathrm{kW}$) and $\sum P_{Loss}$ is the sum of losses of each PPB component. The results of the optimization procedure for the PPB are presented in figure 3.5. The optimized solution for the PPB is the solution which presents the best power density with an efficiency above $99\,\%$. In the case described below, the optimized PPB has an efficiency of $99.3\,\%$ with a power density of $5.41\,\mathrm{kW/dm^3}$. This "electronic capacitor" uses a switching frequency of $140\,\mathrm{kHz}$ with an inductance value of $20\,\mathrm{\mu H}$ and a minimum voltage of $250\,\mathrm{V}$ for a $277\,\mathrm{\mu F}$ capacitor bank. Some details of the PPB design are given in table 3.4 with the corresponding volumes and losses. The heatsink volume is calculated using a coefficient of $5\,\mathrm{cm^3/W}$.

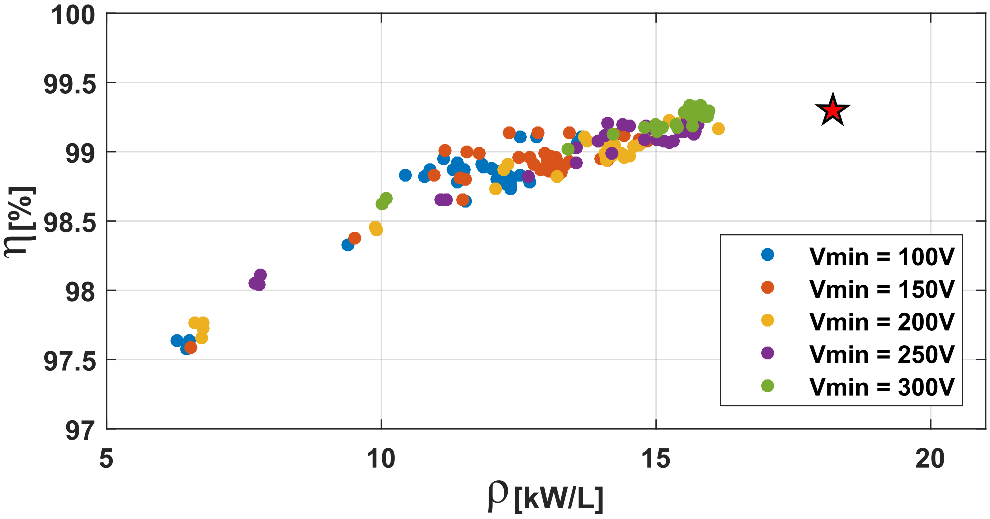


Figure 3.5: Results of the optimization procedure for the PPB. Each combination of input gives a solution with a corresponding efficiency and a power density.

Table 3.4: Details of the optimized power pulsating buffer (PPB), also called electronic capacitor.

General	
η	$99.3\,\%$
ρ	$18.22\,\mathrm{kW/dm^3}$
f_{sw}	$140\,\mathrm{kHz}$
L_{PPB}	$20\,\mathrm{\mu H}$
Minimum voltage	$250\,\mathrm{V}$
C_{PPB}	$277\,\mathrm{\mu F}$
Volume	
Total	$181.1\,\mathrm{cm^3}$
Inductor PBB	$28.7\,\mathrm{cm^3}$
Switch and Driver	$0.5\,\mathrm{cm^3}$
Capacitor Bank	$36.4\,\mathrm{cm^3}$
Heatsink	$115.5\,\mathrm{cm^3}$
Losses	
Total	$23.1\,\mathrm{W}$
Inductor PBB	$14.1\,\mathrm{W}$
Switch	$8.8\,\mathrm{W}$
Capacitor Bank	$0.2\,\mathrm{W}$

3.2 Inductor optimization

The magnetic components represent a large share of a converter volume ($13\,\%$ in [28]) along with empty space and the thermal management system. In order to increase the power density of the converter, inductors must be optimized according to two metrics: their box volume and their losses. The optimization is done using a Pareto front [62]. The inductor optimization script is integrated in the converter optimization script described in section 3.1.4. The design procedure is applied to the inductors of the interleaved PFC, of the DM EMI filter and of the PPB. The inductors which give the best trade-off between efficiency and power density for the converter are selected. Th CM inductors are coupled so they are not considered in this procedure.

3.2.1 Design Procedure

For a converter iteration from figure 3.2, which corresponds to one inductor value and current waveform, a magnetic material and an inductor structure are chosen (figure 3.6). The core geometric parameters of the chosen structure vary between a low and a high limit with constant increments. A matrix, with all combinations of magnetic core geometric parameters is then generated, giving a list of all core dimensions to be investigated (figure 3.7(A)). Each of these combinations results in an inductor design.

The inductor optimization script is run for both structures from figure 3.6. The first structure is called "Planar", and is well established in the industry. The winding is made on the PCB with copper traces and vias. External magnetic cores, a "U" core and a "I" core, are clipped around the PCB.

The second design is called "Embedded Toroidal". The winding is also made by PCB copper traces and vias, but in this structure, the magnetic core is embedded in a cavity inside the PCB. Due to the PCB manufacturing limitations, the core thickness is limited to $3\,\mathrm{mm}$ for a final thickness of the PCB of $3.2\,\mathrm{mm}$.

Both structures share some advantages and drawbacks. The shared advantages are a low profile, a good thermal characteristic, a low cost and a good repeatability. The shared drawbacks are the large footprint and the low copper filling factor. In addition, the "Embedded Toroidal" has the advantage to use "free" space inside the PCB. The positioning of the core can also be automatized, which allows a collective manufacturing and automation. But his manufacturing process is not standard. Also, the PCB top layer can be used to mount SMD components while a heatsink can be attached on the bottom side. Contrary to the "Planar", the "Embedded Toroidal" inductor has flat surfaces, so the heatsink does not need to be machined.

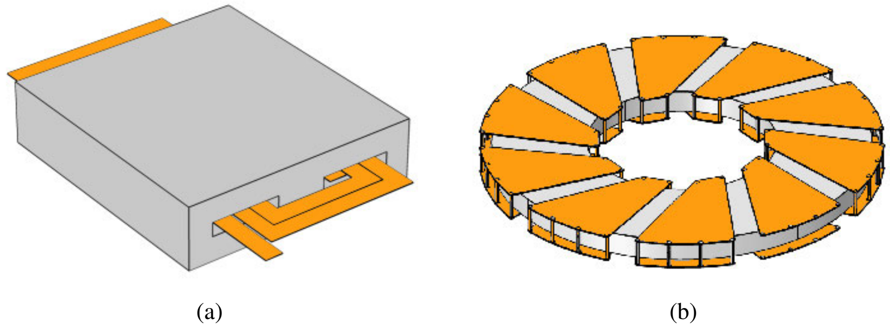

(a) (b)

Figure 3.6: (a) Drawing of the "Planar" structure, where winding is formed on the PCB (dielectric layers not shown) and a magnetic core is clipped around. (b) Drawing of the "Embedded Toroidal" structure, where the magnetic core is embedded inside the PCB (dielectric layers not shown), prior the patterning of the copper layers to form the winding.

The inductor design procedure is implemented using MATLAB. It is integrated in the overall converter design procedure (which also uses MATLAB) described in figure 3.2. For some calculations, a finite element software (FEMM) is interfaced with the MATLAB script to automatically check the temperature distribution of the solutions and decide whether they are acceptable or not. The design procedure is presented in the flowchart in the figure 3.7 and detailed below.

Input Sets

The design procedure uses 3 sets of inputs.

The first set is generated by the global converter design procedure (either for the PFC, EMI filter or PPB as the inductor design script is run for each of these). It consists in the inductor value (L) required and two vectors (time and current) which describe the inductor current waveform ($I_L(t)$) over a period of the $50\,\mathrm{Hz}$ mains. An example of such a current waveform, for a 3 interleaved cell PFC with a zoomed area on the triangular high frequency component, is given in figure 3.8. This waveform contains a low frequency component at $50\,\mathrm{Hz}$ and a high frequency component at the switching frequency (which itself is an input of the converter design procedure in figure 3.2).

The second set of inputs is the magnetic material database which contains ferrite and iron powder materials. Each material is described using 5 parameters. The first parameter is the relative permeability (μ_r). The second one is the induction at saturation (B_{sat}). The last three properties are the Steinmetz coefficients (k, α, β) used

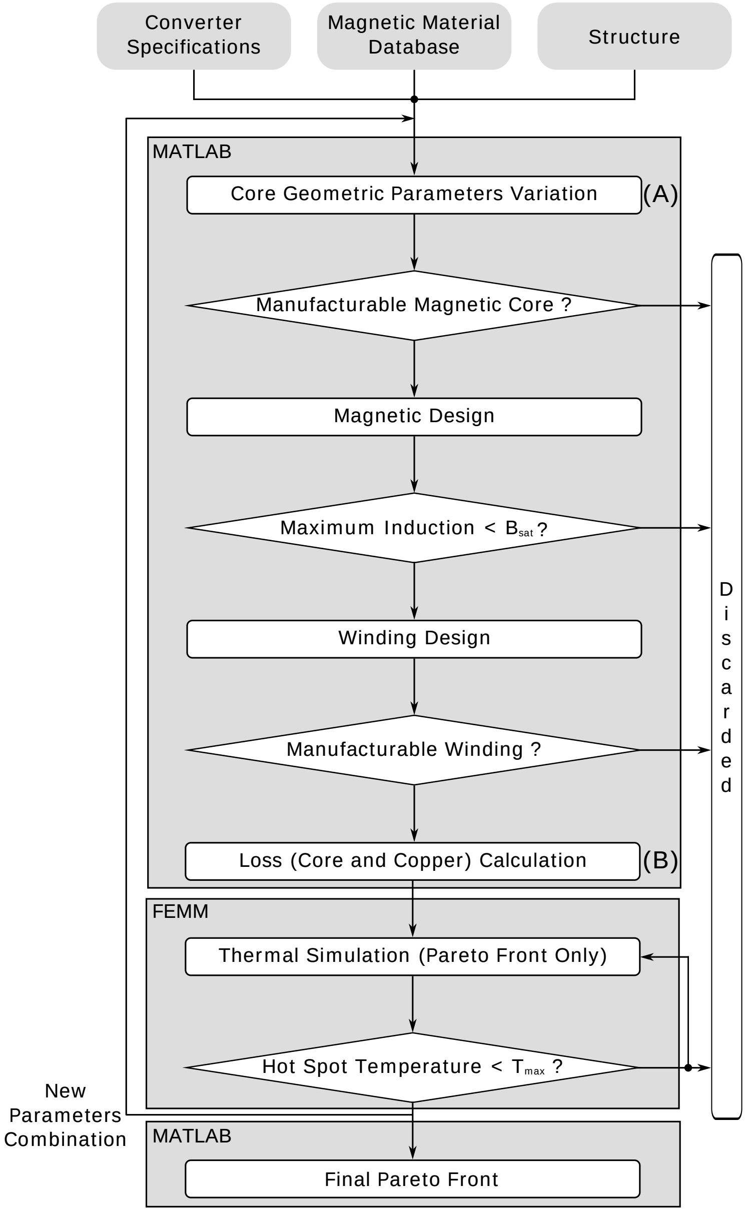


Figure 3.7: Flowchart used for the design of DM EMI Filter / PFC / PPB inductors.

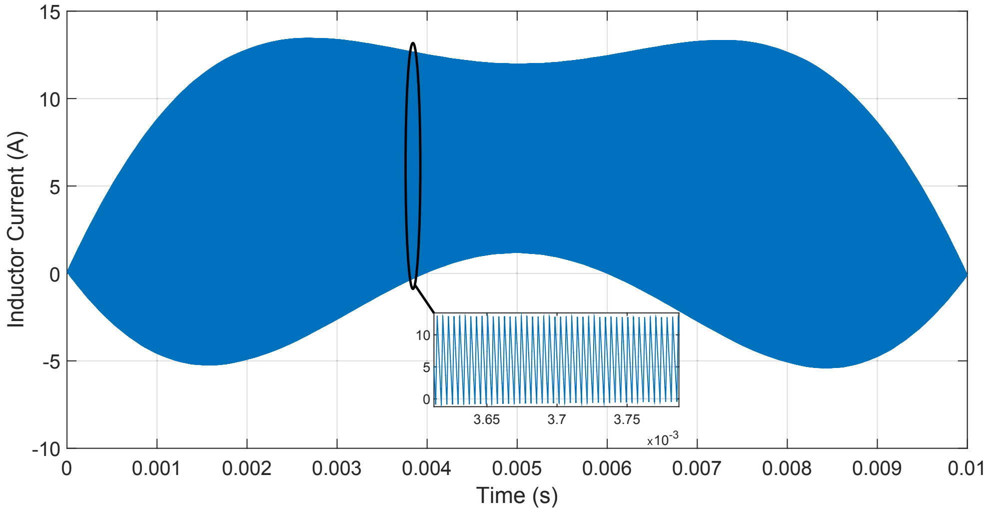
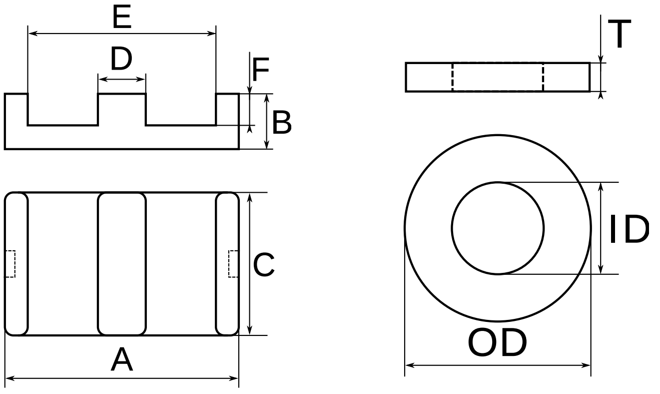


Figure 3.8: Inductor current waveform example for a 3 interleaved cell PFC.

to calculate the core losses [63]. The Steinmetz coefficients present the advantage of being given by all the manufacturers. Iron powder materials present a low permeability, as the highest permeability for iron powder materials in the database is 550 [64]. They are generally used for frequencies below to $100\,\mathrm{kHz}$. The induction at saturation is comprised between $0.7\,\mathrm{T}$ and $1.6\,\mathrm{T}$. However, the maximum permeability of available materials decreases with the increase of the induction at saturation. On the contrary, ferrite materials present higher permeabilities up to 4400 (N95, EPCOS) in the database but their induction at saturation is lower, in the range of $0.4\,\mathrm{T}$. They can be used for frequencies up to $1\,\mathrm{MHz}$ for MnZn ferrite with acceptable losses. NiZn ferrite materials can be used with higher frequency but their permeability is lower. NiZn ferrite materials are thus not considered in this study since the expected converter switching frequency remains below $1\,\mathrm{MHz}$ due to MOSFET switching capability. In order to avoid saturation, an air-gap is considered for ferrite materials.

The third set of inputs is the selection of one of both inductor structures ("Planar" and "Embedded Toroidal"). Each structure is associated with its core geometric dimensions. The core geometric dimensions are presented in figure 3.9 for both structures. The "Planar" structure is defined by dimensions C, D, E and F. The dimensions A and B are calculated to have a constant magnetic section along the magnetic path which gives $A = D + E$ and $B = \frac{D}{2} + F$. This allows to reduce the number of geometric variables. The lower limit for F is $2\,\mathrm{mm}$ to have magnetic core legs longer that the PCB thickness. The "Embedded Toroidal" structure is defined by dimensions OD, ID and T. The lower limit for T is $3\,\mathrm{mm}$ which is the limit for the PCB embedding.



(a) (b)

Figure 3.9: (a) Drawing of the core geometric dimensions for the "Planar" structure. (b) Drawing of the core geometric dimensions for the "Embedded Toroidal" structure.

Magnetic Design

The first step is to calculate the magnetic path length (l_c) and the magnetic section (A_c) for each combination. The magnetic path length (l_c) and the magnetic section (A_c) are calculated with equations (3.9) and (3.10) respectively for the "Planar". For calculation, two "U" cores are used for the "Planar" inductor.

$$l_{c_{Planar}} = \frac{A}{2} + \frac{E}{2} + 2 \cdot B + 2 \cdot F \tag{3.9}$$

$$A_{c_{Planar}} = min(D \cdot C, 2 \cdot (B - F) \cdot C, (A - E) \cdot C) \tag{3.10}$$

The magnetic path length (l_c) and the magnetic section (A_c) are calculated with equations (3.11) and (3.12) respectively for the "Embedded Toroidal".

$$l_{c_{EmbeddedToroidal}} = \pi \cdot \frac{(OD + ID)}{2} \tag{3.11}$$

$$A_{c_{Planar}} = \frac{(OD - ID)}{2} \cdot T \tag{3.12}$$

As seen previously, the inductor can be designed using iron powder material without air-gap or using ferrite material with an air-gap. The equations will be presented for both cases.

With a design using an iron powder material without air-gap, the number of turns necessary to obtain the expected inductance N value is calculated using the equation (3.13).

$$N = \sqrt{\frac{L \cdot l_c}{\mu_0 \cdot \mu_r \cdot A_c}} \tag{3.13}$$

where L is the inductance value, μ_0 is the vacuum permeability, μ_r the relative permeability of the magnetic material and N is the number of turns necessary. The subscript c refers to the core. The actual number of turns used in the design N_L is rounded to the integer just above the calculated value.

In order to keep a constant inductance value for any operation point, it is chosen to stay in the linear part of the BH curve (i.e. not to reach saturation of the magnetic core, even at full power). The maximum induction level is calculated for each solution and compared with the saturation level for the corresponding material as presented in equation (3.14). A security factor (0.7) is applied to be sure to remain in the linear domain of the material.

$$0.7 \cdot B_{sat} > \mu_0 \mu_r N_L \frac{I_{max}}{l_c} \tag{3.14}$$

where I_{max} is the maximum current (the maximum value reached by the current waveform supplied as an input of the design script). The solutions which lead to saturation are discarded. For all the other solutions, the design process continues further.

For a design using ferrite material with an air-gap, the permeability of the magnetic circuit will depend on the size of the air-gap. The equivalent reluctance of the gapped core is the sum of the individual reluctances which gives the equation (3.15).

$$\mathcal{R} = \mathcal{R}_c + \mathcal{R}_g = \frac{l_c}{\mu_0 \mu_r A_c} + \frac{g}{\mu_0 A_g} \tag{3.15}$$

where the subscript g refers to the air-gap and g is the length of the air-gap. This is a reasonable assumption when g is small compared to the dimensions of the cross-section, because fringing effects can be neglected. These effects will be discussed later. The equivalent reluctance can also be calculated with equation (3.16).

$$\mathcal{R} = \frac{l_c}{\mu_0 A_c} \left[\frac{1}{\mu_r} + \frac{1}{l_c/g} \right] = \frac{l_c}{\mu_{eff} \mu_0 A_c} \tag{3.16}$$

If $\mu_r >> 1$, the effective relative permeability can be approximated with equation (3.17). This approximation will be used in the design script.

$$\mu_{eff} = \frac{l_c}{g} \tag{3.17}$$

Replacing μ_r by μ_{eff} in equations (3.14) and (3.13) yields equations (3.18) and (3.19)

$$L = \mu_0 \mu_{eff} N^2 \frac{A_c}{l_c} \tag{3.18}$$

$$0.7 \cdot B_{sat} > \mu_0 \mu_{eff} N \frac{I_{max}}{l_c} \tag{3.19}$$

Assuming, the inductor works at $0.7B_{sat}$ for the maximum current, it is possible to associate the last two equations (3.18) and (3.19) to calculate the number of turns needed and the effective permeability with the equations (3.20) and (3.21) respectively.

$$N = \frac{L \cdot I_{max}}{A_c \cdot 0.7 \cdot B_{sat}} \tag{3.20}$$

$$\mu_{eff} = \frac{(0.7 \cdot B_{sat})^2 \cdot l_c \cdot A_c}{\mu_0 \cdot I_{max}^2 \cdot L} \tag{3.21}$$

The actual number of turns of the inductor N_L is the integer just above the calculated value. Once the effective permeability has been calculated, the air-gap length (g) can be calculated using equation 3.17.

Once the number of turns is known, the geometry of the winding can be defined. The winding dimensions are calculated according to the core geometry and the PCB design rules presented in table 3.5 for both structures. Standard design rules were chosen because the "Embedded Toroidal" structure is not common, and manufacturers could not commit to more advanced values. They could have been improved with discussion with PCB manufacturer on a long term project. The "Planar" PCB is arbitrarily limited to 6 layers to avoid an important increase of the manufacturing cost.

With some cores, it is not possible to calculate dimensions which meet the design rules, in particular the clearance between two PCB traces or between two via pads. The solutions which do not meet the design rules are discarded.

The remaining solutions are now defined with their core and winding geometries. They also provide the required inductance value. Their maximum induction remains lower than 70 $\%$ of the induction at saturation of the magnetic material. These inductors can be manufactured with respect to the PCB design rules. Next, the losses have to be calculated.

Losses Calculation

The inductor losses can be separated into core losses and copper losses.

As the current has a complex waveform (for example a 50 Hz sinewave with a superimposed high frequency ripple for the PFC inductors), the calculation of the core losses is based on the improved Generalized Steinmetz Equation (iGSE) [63]. Indeed, the Steinmetz equation was developed to calculate core losses for a sinusoidal excitation [65], and then improved and generalized to be adapted to more complex waveforms. The iGSE allows to take into account losses due to minor loops. The iGSE does not consider the DC bias and the relaxation effects, which is acceptable

Table 3.5: PCB design rules used to design both inductor structures.

Planar	
Number Of Layers	6
Copper Layer Thickness	105 µm
Prepreg Layer Thickness	200 µm
Clearance	200 µm
Distance between Magnetic Core and PCB	500 µm
Distance between PCB Edge and Winding	500 µm

Embedded Toroidal	
Number Of Layers	2
Copper Layer Thickness	105 µm
Prepreg Layer Thickness	200 µm
Clearance	200 µm
Via Pad Diameter	600 µm
Via Drill Tool Diameter	350 µm
Via Final Inner Diameter	250 µm

in our case since there is no DC bias [65]. It also uses the Steinmetz parameters which are valid only for a limited flux density and frequency range, but present the advantage of being given by magnetic material manufacturers.

The iGSE is presented in equation (3.22)

$$P_{v_i} = \frac{1}{T}\int_0^T k_1 \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{3.22}$$

where:

$$k_1 = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{3.23}$$

where (k, α, β) are the Steinmetz coefficients, B is the flux density, T is the period of the signal, i is the index of the hysteresis loop and P_{v_i} is the core power loss per unit volume of the i^{th} loop.

When considering the input current waveform (20 ms, or one period of the 50 Hz fundamental frequency), the iGSE has to be applied on one major loop and many minor loops. An algorithm is needed to split an arbitrary waveform in a major loop and one or more minor loops. First, the waveform is separated into "rising" and "falling" sections. The "rising" section starts at the lowest point and ends at the highest point of the waveform. On the contrary, the "falling" section starts at the highest point and ends at the lowest point of the waveform. Both sections can contain

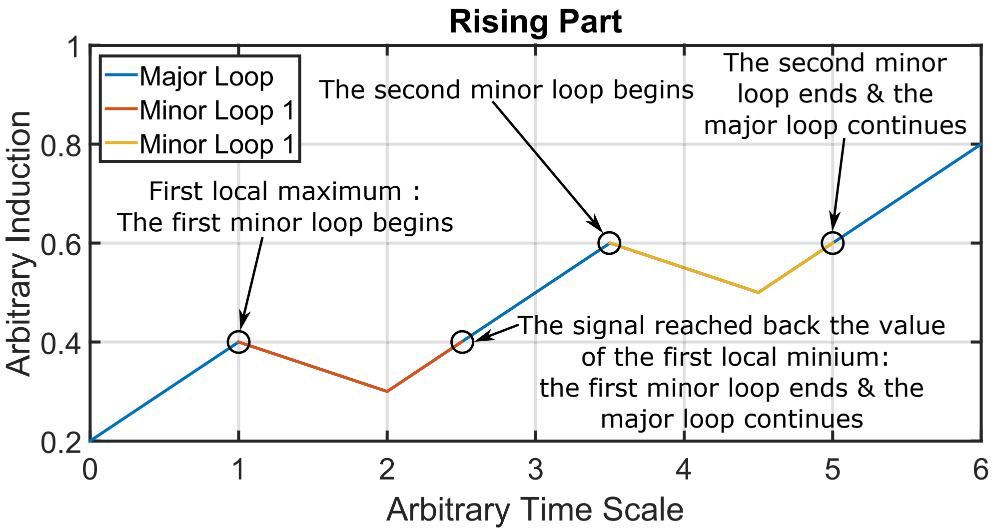


Figure 3.10: Arbitrary waveform (rising section) split into major loop and minor loops for core loss calculation. The conditions are all based on the opposite slopes for falling section.

positive and negative slopes but are on average rising or falling respectively between the first point and the last point.

For each section, the minor loops must then be identified. The method for separating minor loops for the rising section is shown in figure 3.10. The waveform is scanned, and the data is allocated to the major loop until the first local maximum is reached. The data is then associated with the first minor loop until it goes through a local minimum and comes back to the first local maximum value. From this point to the second local maximum, the data is added to the major loop. At the second local maximum, the second minor loop begins. This procedure is repeated up to the global maximum. At the global maximum, the falling part begins, and a comparable (albeit inverting local minimums and maximums) procedure starts. The same process is applied to all minor loops to account for the possible existence of sub-loops. Equation (3.22) is then applied to each loop.

The core power loss per unit volume P_{core} is calculated with the equation (3.24).

$$P_{core} = \sum_i P_{v_i} \frac{T_i}{T} \tag{3.24}$$

where T_i is the period of the i$^{\text{th}}$ loop and T is the period of the waveform.

The copper losses can be separated into losses due to the $50\,\text{Hz}$ sinewave and losses due to the high frequency triangular ripple. The DC resistance (R_{DC}) of the winding is used to calculate joule losses associated with the low frequency sinewave.

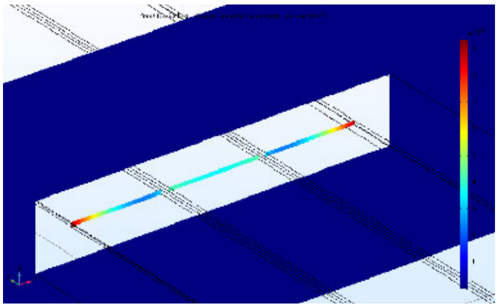


Figure 3.11: Current density inside the winding of the simulation used to define the K factor to calculate high frequency copper losses.

R_{DC} is calculated using the geometry and the copper resistivity ($17\,\mathrm{n\Omega \cdot m}$) using equation (3.25).

$$R_{DC} = \rho \frac{l_w}{S_w} \tag{3.25}$$

where l_w is the length of the winding and S_w is the cross section of the winding. For the "Planar" inductor, the vias interconnecting the different layers are not taken into account. The joule losses caused by the $50\,\mathrm{Hz}$ sinewave P_{DC} are calculated with equation (3.26)

$$P_{DC} = R_{DC} \cdot I_{rms,LF}^2 \tag{3.26}$$

where $I_{rms,LF}$ is the RMS value of the $50\,\mathrm{Hz}$ sinewave current.

The copper losses due to the HF current ripple are calculated using an equivalent AC resistance (R_{AC}). The actual value of this AC resistance is difficult to estimate because of skin and proximity effects. As the distribution of the current in the conductor is affected by the magnetic field in the same inductor, there is no analytical expression to calculate R_{AC}. The variety of the winding geometries considered in the design procedure makes it difficult to define the resistance increase with the frequency.

A single 3D finite element simulation, using COMSOL, was done to calculate the R_{AC} for 3 PCB tracks surrounded by a magnetic core taking into account skin and proximity effects (Figure 3.11). The geometry used is not similar to the designed inductors. However, a magnetic simulation is too time consuming to be added in the converter optimization script. A factor K, defined as R_{AC}/R_{DC}, obtained from this FEM simulation is used in the inductor optimization procedure instead. The value of the K factor as a function of the frequency is given in table 3.6. The K factor values are then used for every inductor design.

Using such look-up table to calculate R_{AC} only provides a coarse estimation of the high frequency copper losses. But magnetic 3D finite element simulations

Table 3.6: K Factor, R_{AC}/R_{DC}, used for the calculation of the high frequency copper losses.

Frequency Range (kHz)	K Factor
< 160	2.88
$160 - 200$	3.37
$200 - 240$	3.58
$240 - 280$	3.77
$280 - 320$	3.99
> 320	4.40

are time consuming (several hours) so they cannot be integrated in the design flow from figure 3.7, as initially planned. Measurements on the first prototype will be used as a feedback to correct the K factor values for future improvements. This will be discussed in details in chapter 4. The total copper losses are then calculated using equation (3.27). The RMS currents are calculated by performing a FFT on the inductor current waveform.

$$P_{Copper} = R_{DC} \cdot I^2_{rms,LF} + R_{DC} \cdot I^2_{rms,HF} = R_{DC} \cdot (I^2_{rms,LF} + K \cdot I^2_{rms,HF}) \quad (3.27)$$

Only the fundamental frequency of the ripple is used to select the R_{AC} value in table 3.6. The losses due to the harmonics of the ripple current are calculated with the same R_{AC}.

An example of the results of the design procedure at the end of the stage B (figure 3.7), for a 4 interleaved cells PFC with a ripple of $4\,\text{A}$ at a frequency of $180\,\text{kHz}$ using the "Planar" inductor structure and N87 MnZn ferrite (EPCOS), is presented in figure 3.12. Each point corresponds to an inductor design. However, at this stage, only the box volume and the losses are known. There is no guarantee that all design from figure 3.12 would work. In particular, small inductors with a high power dissipation might turn out to be impossible to cool down. These would operate at unacceptable high temperatures. Therefore, the next step is to calculate the temperature distribution in the inductors to ensure it remains acceptable, and to discard unrealistic designs.

Thermal Verification

After the losses have been estimated, the temperature distribution in the inductor has to be calculated. The maximum allowed temperature chosen for the optimization

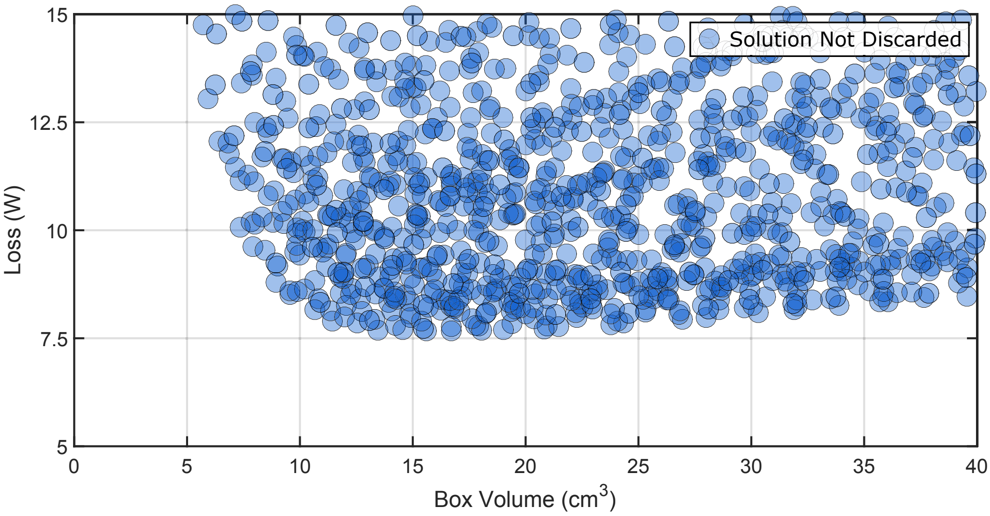


Figure 3.12: Results (Losses vs Box Volume) of the inductor designed for a 4-interleaved cells PFC with a ripple of $4\,\mathrm{A}$ at a frequency of $180\,\mathrm{kHz}$ using the "Planar" inductor structure and N87 MnZn ferrite (EPCOS).

process is $100\,^{\circ}\mathrm{C}$, which corresponds to the temperature used for the definition of the Steinmetz coefficient. It is also the maximum continuous operating temperature of the PCB ($130\,^{\circ}\mathrm{C}$ for ISOLA PCL 370HR), with a safety margin.

The temperature distribution in the inductor is calculated by finite element simulation using the FEMM software. This software offers the possibility to be interfaced with MATLAB so the model can be created and simulated from the MATLAB command line. However, FEMM is limited to 2D and 2D axis-symmetric models. In our case, thermal simulations use a 2D axis-symmetric model, which was found to offer a suitable simplification for the "Embedded Toroidal" and the "Planar" geometries. The advantage of 2D or 2D axis-symmetric models is that the computation time is much faster than for 3D model ($1\,\mathrm{s}$ per geometry) with an automatically generated mesh.

The models are defined by the geometry of the inductor and the properties of their materials. The geometry is generated by the design code for each inductor using the dimensions of the magnetic core and the winding as defined by the design procedure. The materials are defined by a thermal conductivity in both model directions (r-direction and z-direction) and a volume heat generation density ($\mathrm{W/m^3}$). The volume heat generation density corresponds to the losses value calculated previously. Table 3.7 presents the thermal conductivity of the materials. These thermal models ("Embedded Toroidal" and "Planar") are used for their simplicity, variability (automated study of a high number of core geometries) and short computation time.

Table 3.7: Materials thermal conductivity used for thermal models.

Material	Thermal Conductivity $(\mathrm{W}/(\mathrm{m}\cdot\mathrm{K}))$
Copper	390
FR4	0.3
Magnetic Core	5
TIM	1.8

The thermal model of an "Embedded Toroidal" is presented in figure 3.13. This 2D axis-symmetric model accurately represents the annular shape of the magnetic core. The magnetic material has a thermal conductivity fixed at $5\,\mathrm{W}/(\mathrm{m}\cdot\mathrm{K})$ in both directions. The volume heat generation density imposed in the magnetic core is the core losses calculated previously divided by its volume. On the contrary, the PCB substrate and the TIM are in reality square shaped and therefore are only coarsely described using a 2D axis-symmetric model. However, this deformation has little effect on the simulation results because these materials have a low thermal conductivity ($0.3\,\mathrm{W}/(\mathrm{m}\cdot\mathrm{K})$ and $1.8\,\mathrm{W}/(\mathrm{m}\cdot\mathrm{K})$ respectively), resulting in limited heat spreading.

A special care is given to copper conductors. In the model, a difference is made between the PCB traces and the vias. Indeed, because of the 2D simplification, the clearance between the PCB traces or the spacing between the vias are not considered in the model geometry. The clearance between PCB traces is only $200\,\mathrm{\mu m}$ which is negligible in comparison with the width of the PCB traces themselves (several millimeters). Then, the thermal conductivity of the top and bottom copper layers is considered as equal to that of plain copper ($390\,\mathrm{W}/(\mathrm{m}\cdot\mathrm{K})$).

On the contrary, the clearance between the PCB vias is comparable to the diameter of the PCB vias. Also, the PCB vias are not fully filled with copper (they have a hollow structure similar to a thin-walled tube). The thermal conductivity of the via material has to be modified to reflect the average conductivity of the via areas. The thermal conductivity of the vias is calculated using equation (3.28).

$$\lambda_{ModelVia} = \lambda_{Copper} \cdot \frac{V_{Real}}{V_{Model}} \tag{3.28}$$

where $\lambda_{ModelVia}$ is the vias thermal conductivity in the model, λ_{Copper} is the thermal conductivity of the copper ($390\,\mathrm{W}/(\mathrm{m}\cdot\mathrm{K})$, V_{Real} is the real volume of copper in the PCB vias and V_{Model} is the volume of the PCB via area. The real and simulated volumes are shown in figure 3.14. The volume heat generation density in the copper

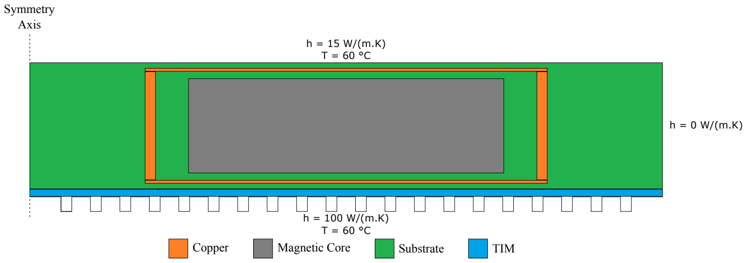


Figure 3.13: 2D axis-symmetric finite element thermal model for the "Embedded Toroidal". The fins are only represented for illustration.

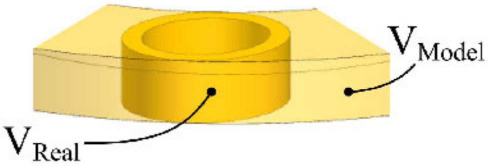


Figure 3.14: Drawing of the real volume (non-transparent) and the model volume (transparent) of vias.

also has to be adapted. The previously calculated copper losses are divided by the real volume. The inductor is placed on a heatsink which is modelled as a constant heat transfer coefficient of $100\,\mathrm{W}/(\mathrm{K}\cdot\mathrm{m}^2)$ which is a coarse estimation of a heatsink. The natural convection on the top surface is considered with a constant heat transfer coefficient of $15\,\mathrm{W}/(\mathrm{K}\cdot\mathrm{m}^2)$ [66].

The thermal model of a "Planar" design is presented in figure 3.15. As for the "Embedded Toroidal", some material properties have to be adapted to the 2D model to represent 3D effects. Here again, the volume heat generation density in the copper and in the magnetic core is calculated using the copper and core losses obtained previously, with respect to the winding and the magnetic core volumes. However, the thermal conductivity of the materials is not modified, because the tracks are basically continuous in the z-direction, and vias are not considered here. Because the actual shape of the magnetic core is parallelepipedic and not discoidal, the heat transfer coefficient on the top and on the bottom surface are multiplied by the ratio between the real surface (square) and the simulated surface (round).

This FE simulation is run only for solutions on the Pareto front because it represents the inductors with the best trade-off between box volume and loss. The Pareto front just before the thermal FE simulations is highlighted in figure 3.16a. After FE simulations, the solutions with a hot spot temperature exceeding $100\,^\circ\mathrm{C}$ are discarded. A new Pareto front is then calculated. In the example presented in figure 3.16b, all solutions of the first Pareto front are discarded due to a hot spot of

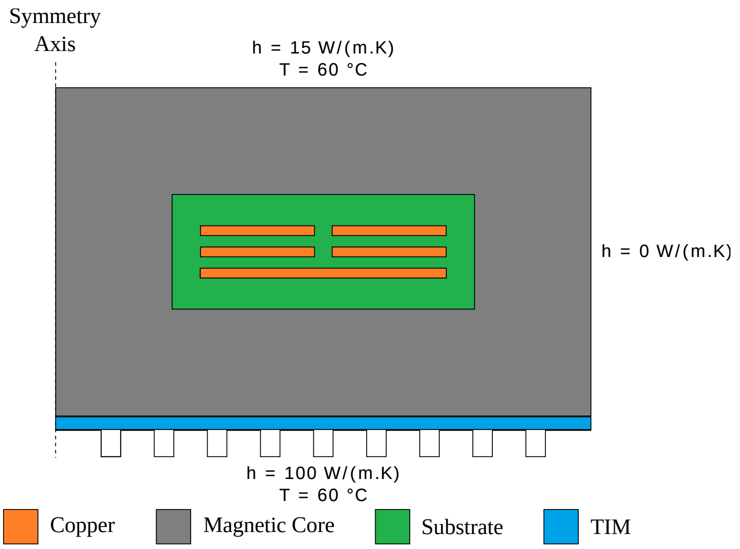


Figure 3.15: 2D axis-symmetric finite element thermal model for the "Planar". The fins are only represented for illustration.

more than 100 °C. New thermal simulations are done on the new Pareto front. The thermal simulations are repeated until all solutions on the Pareto front have an acceptable temperature (Figure 3.16c). In this case, only one inductor forms the Pareto front for the "Planar"’ structure.

The same principle is applied to the structure "Embedded Toroidal" which is not shown in this example. At this part in the design process, the solutions have been completely explored, and the remaining ones correspond to inductors which can actually be built.

3.2.2 Results

The results of the design procedure, for "Embedded Toroidal" and "Planar" structures are presented in figure 3.17. These results are for a 4 interleaved cells PFC with a ripple of 4 A at a frequency of 180 kHz, using N87 the MnZn ferrite (EPCOS) (Other configurations were investigated, for more information, look at J. Le Leslé PhD thesis). In each case, these results are represented as a cloud of points in which each point corresponds to an inductor design. The chosen solution is positioned on the Pareto front which is formed by inductors with the best trade-off between the box volume and the loss. The Pareto front is highlighted for both structures.

For the "Planar" structure, many solutions were removed from the Pareto front because of excessive temperatures reached in the inductor. On the contrary, for the "Embedded Toroidal", no solutions were discarded by the thermal simulations. This

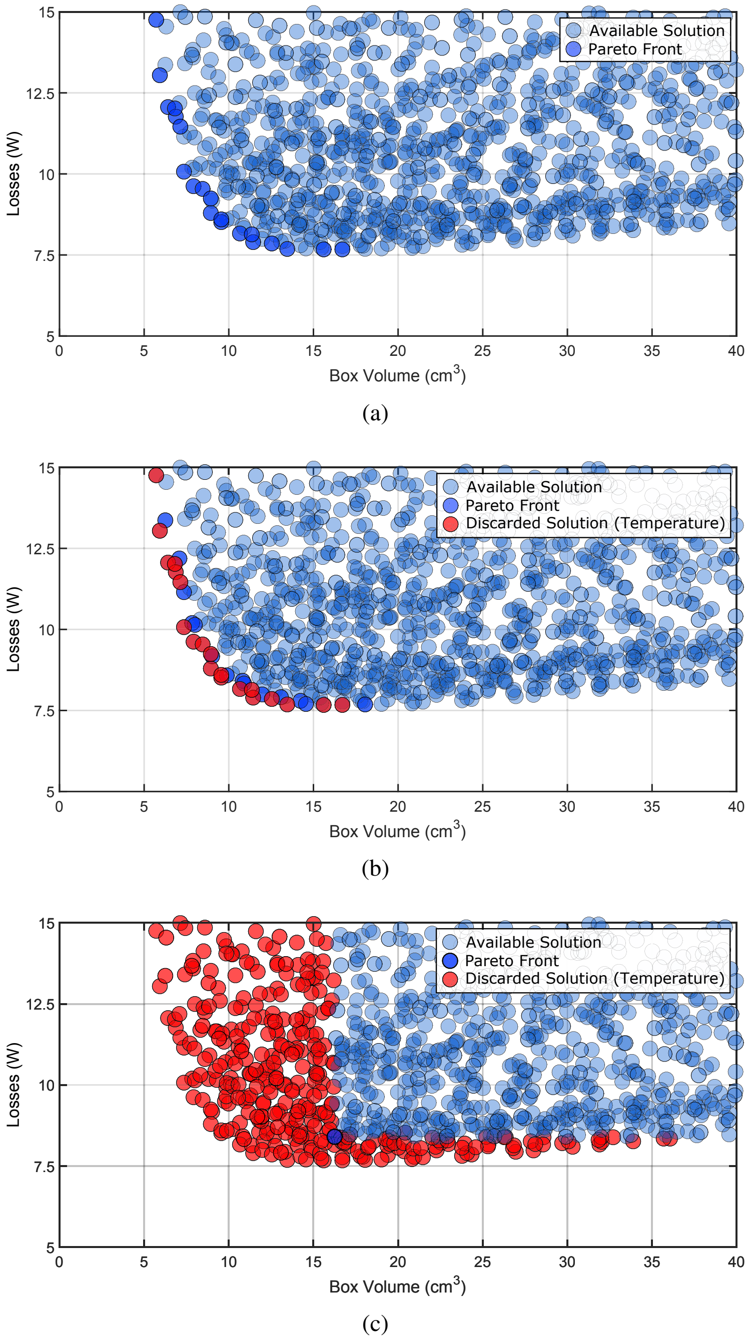


Figure 3.16: Results (Losses vs Box Volume) of the inductor designed for a 4 interleaved cells PFC with a ripple of 4 A at a frequency of 180 kHz using the "Planar" structure and N87 MnZn ferrite (EPCOS). (a) The Pareto front prior to thermal FE simulations is highlighted. (b) FE simulations show that the solutions on the first Pareto front do not have a hot spot temperature inferior to 100 °C. A new Pareto front is calculated. (c) The process is repeated until the solutions placed on the Pareto front have an acceptable temperature.

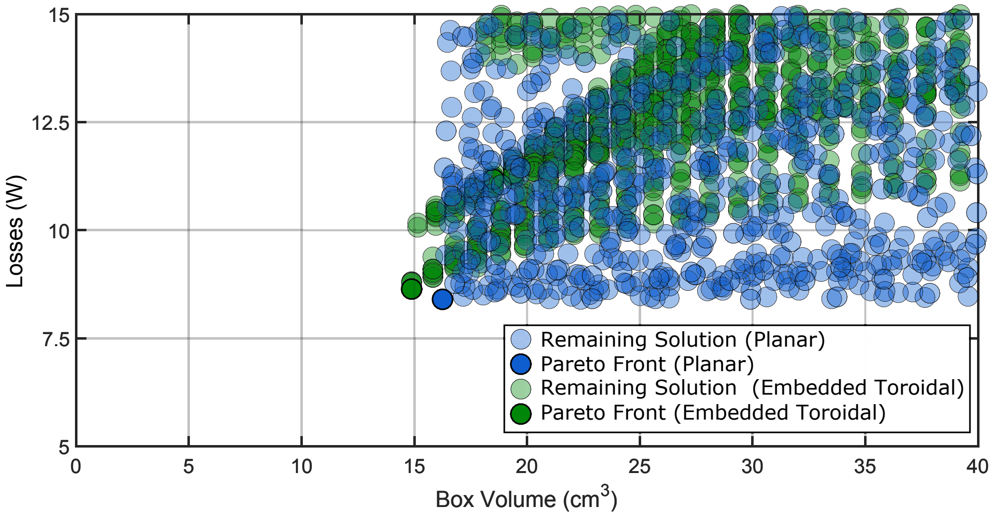


Figure 3.17: Results of the design procedure, for both structures "Embedded Toroidal" and "Planar", after all the solutions which resulted in excessive temperature have been discarded.

means that the thermal considerations are not a limiting factor for this structure. The structure has a more efficient cooling, due to its large surface.

The dimensioning factor for the "Embedded Toroidal" structure is the PCB design. A maximum number of turns is imposed by the magnetic core inner diameter and the size and spacing of the vias. This puts a lower limit on the core inner diameter. Also, the thickness of the magnetic core is limited to $3\,\mathrm{mm}$. All the best solutions used the maximum thickness because it is the closest of the optimal magnetic design which is for a square cross section. These two limits result in a larger outer diameter, which in turn sets a limit on the minimum box volume achievable.

The fact that the temperature is not dimensioning for the "Embedded Toroidal" allows to decrease the performance of the thermal management system. This modification would increase the inductor temperature closer to the limit ($100\,°\mathrm{C}$) and reduce the converter volume by, for example, reducing the length of the heatsink fins.

The inductor solutions for both structures are given in table 3.8. The best trade-off is obtained for the "Embedded Toroidal". As for the presented results, the converter with the best trade-off between efficiency and power density is using "Embedded Toroidal". The fact that the temperature is not the limiting factor for the "Embedded Toroidal" is also an advantage for the 3D assembly of the converter. This structure will allow an easier 3D stacking as will be presented later. So "Embedded Toroidal" inductors are going to be used for the realization of a $3.3\,\mathrm{kW}$ PFC and DM EMI filter.

Table 3.8: Results for the inductors designed with the optimization script ("Planar" and "Embedded Toroidal") for the PFC inductor.

Planar	
Loss	8.4 W
Box Volume	16.2 cm^3
Hot Spot Temperature	97 °C
Magnetic Material	Ferrite N97
Magnetic Core	ELP 32/6/20 I 32/3/20
Number Of Turns	11

Embedded Toroidal	
Loss	8.6 W
Box Volume	14.9 cm^3
Hot Spot Temperature	92 °C
Magnetic Material	Ferrite N87
Magnetic Core	R 63/38/3
Number Of Turns	38

3.3 Conclusion

In this chapter, I firstly presented an overview of the framework of the study. The project aimed at the design and the realization of an AC/DC bidirectional converter. The project is separated in two work packages "Topology" and "Implementation". Several topologies were compared (not presented here) in the "Topology" work package. It was chosen to use an interleaved full bridge power factor corrector (PFC). An EMI filter is placed on the AC side of the PFC to comply with the standards. On the DC side, a power pulsating buffer (PPB), also called electronic capacitor, is used. This thesis corresponds to the "Implementation" work package and aims at designing the actual hardware from the circuit diagram using PCB embedding technology. In addition, the magnetic component optimization is made in the "Implementation" work package. Indeed, a new design ("Embedded Toroidal") for power inductor is investigated. The new design, with an embedded magnetic core and a winding formed using PCB copper tracks and vias, is compared to the "Planar" inductor.

The inductor design procedure uses simple models (i.e. considering HF behavior with an AC resistance based on only one 3D simulation). But, it allows to include the inductor design procedure as part of the overall converter design procedure, while keeping a short computation time. The number of turns to obtain the required inductance value is calculated. The losses are calculated using the DC resistance and the AC resistance for the copper losses and the iGSE for the core losses. The inductor hot spot temperature is studied with an interface between FEMM and MATLAB.

At the end, inductors which do not respect manufacturability of the magnetic core, exceed the maximum induction, do not meet the PCB design rules or may become too hot are discarded. The results are presented on a Pareto front (Losses Vs

Box Volume) representing inductors with the best trade-off between efficiency and box volume.

The ferrite materials present an advantage due to lower core losses compared to the iron powder materials at the frequency studied (above 100 kHz). For the two structures studied, the "Planar" is limited by its operating temperature. Indeed, many "Planar" designs are removed from the Pareto front due to a high temperature reached in the inductor. On the contrary, for the "Embedded Toroidal", the thermal considerations are not a limiting factor. But the limiting factor is the PCB design rules (mostly the clearance between the vias pads or the maximum thickness of the board). The "Embedded Toroidal" structure is found to present a smaller volume for a same amount of losses compared to the "Planar", and to be easier to cool down.

The next step is the comparison of the models with prototypes. The prototypes can be made in house or with a PCB manufacturer. The full converter, which is going to use "Embedded Toroidal" inductor, is going to be manufactured by a PCB manufacturer. The converter implementation, the chosen stack-up and the manufacturing processes, as the converter thermal management and parasitic elements calculations are presented in chapter 4.

Chapter 4

Implementation of an integrated converter

4.1 Introduction

The previous chapter addressed the optimization of a converter by selecting the most suitable circuit topology and components. Here, we consider the physical implementation, i.e. the circuit routing and component assembly to form an actual converter. This implementation step is as important as the optimization to obtain the best power density. Indeed, empty spaces represent the largest volume in a converter [14]. The empty space is mostly due to the difference in height between components placed on a 2D layout.

Along with empty space, the thermal management system occupies a large part of a converter volume. With an assembly which has poor thermal properties, the heatsink size has to be bigger to keep component temperatures acceptable compared to an assembly with better thermal properties. Having in mind the 3D assembly and the thermal management at an early stage of the project will allow to obtain a better converter from a power density point of view. The chosen 3D structure will be presented. As a reminder, the thermal management chosen for this project relies on natural convection.

There is at minimum 2 batches with embedded components needed to manufacture all converter elements. Indeed, the power dies cannot be embedded inside the same PCB as the SMD components or the ferrite cores. The height of the SMT components does not permit to use microvias for power dies interconnection. The SMT components are too tall (up to $2\,\mathrm{mm}$-thick) to allow for the microvias required to connect the power dies.

4.2 3D Assembly

As several PCBs are used to form a single PFC brick, a "stacked" assembly is chosen, where three PCBs of identical surface are used: one with the 4 power dies, one with the 2 driver circuits, and one with the inductor. The bottom PCB, closest to the heatsink, receives the 4 embedded dies because they are the most demanding regarding thermal management due to their higher losses density. The PCB with the 2 embedded driver circuits is placed just above to limit parasitic elements in the interconnects. Finally, the PCB with embedded inductors is placed on the top. The PCBs are interconnected using soldered wires. This 3D assembly allows to keep each element separated in the case of an issue in the manufacturing process.

With this configuration, the empty space created around each component is filled with resin compared to air in a standard converter. The replacement of air by resin allows a better conduction of the heat from the components to the heatsink and allows easier interconnection. In addition, vias can be used to improve the thermal conductivity. However, the weight increases while the volume stays the same.

The final aim of such a 3D assembly is to study the feasibility of the manufacturing process for each element in a first run. It also allows to evaluate the interest of embedding for each component. A second run would make a better use of the volume, i.e. by placing components such as the gate drivers in the center of the inductors and on the surface of the top PCB. So, this described second run would only have 2 PCBs for a PFC brick. One PCB with "thin" components which contains embedded dies and one PCB with "thick" components which contains the magnetic core and the SMD components.

The size of the PFC brick is driven by the size of the inductor. The PCB is kept square to allow for easy assembling of several bricks together while keeping the converter box volume low. The brick can be placed vertically or horizontally in regard of the heatsink. It means that the heatsink can be placed at the bottom of the 3 PCBs stack (horizontal configuration) or on the side of 3 PCBs stack (vertical configuration). This is discussed below.

4.3 Thermal Management Limitation

In order to choose the best configuration for the converter, a coarse evaluation of the heatsink dimensions is done for both configurations (heatsink at the bottom or on the side of the PCB stack). This evaluation will use the cooling system performance index $CSPI$ $(\mathrm{W}/(\mathrm{K}\cdot\mathrm{dm}^3))$, defined by equation (4.1).

$$CSPI = \frac{1}{R_{th}\cdot V} \tag{4.1}$$

where R_{th} (K/W) is the heatsink thermal resistance and V (dm^3) is the heatsink volume. The heat due to converter loss has to be evacuated using heatsink in natural convection. After a study of 5 straight fin heatsinks on the market, with similar baseplate dimensions that to required ones, it is found that the CSPI for heatsink in natural convection are approximately between $1.5\,\mathrm{W}/(\mathrm{K}\cdot\mathrm{dm}^3)$ and $2.5\,\mathrm{W}/(\mathrm{K}\cdot\mathrm{dm}^3)$. The value of $2.5\,\mathrm{W}/(\mathrm{K}\cdot\mathrm{dm}^3)$ for the CSPI is chosen as it corresponds to the best heatsink while remaining realistic.

The estimated heatsink volume can be calculated with equation (4.2).

$$V = \frac{P}{\Delta T\cdot CSPI} \tag{4.2}$$

where P are the losses evacuated and ΔT is the temperature difference between the heatsink and the environment. We assume a heatsink with a CSPI of $2.5\,\mathrm{W}/(\mathrm{K}\cdot\mathrm{dm}^3)$ and an arbitrary temperature difference of $45\,^{\circ}\mathrm{C}$ between the heatsink and the environment, which corresponds to a heatsink temperature of $105\,^{\circ}\mathrm{C}$. The maximum losses for each converter part (EMI filter, PFC and PPB) are fixed to $33\,\mathrm{W}$ which correspond to $1\,\%$ of the converter nominal power. Then, the losses in a PFC brick are $8.25\,\mathrm{W}$ (4 cells are interleaved in the optimal converter).

The estimated heatsink volume is $73\,\mathrm{cm}^3$.

The size of the PCB with the embedded inductor is driving the size of the heatsink. The PFC brick is $7\times 7\times 1$ cm^3. From the heatsink volume and the dimensions of its baseplate, the fin height can be calculated. In the horizontal configuration, the heatsink baseplate is 7×7 cm^2 which gives a fin height of $1.5\,\mathrm{cm}$. In the vertical configuration, the heatsink baseplate is 7×1 cm^2 which gives a fin height of $10.4\,\mathrm{cm}$.

The heatsinks used to define the CSPI have a fin thickness close to $2\,\mathrm{mm}$. The fin form factor for the vertical configuration is high resulting in a poor fin efficiency (capability to conduct the heat to the bottom of the fin, which was not taken into account in the hypothesis) decreasing the heatsink efficiency. On the contrary, the horizontal configuration presents a heatsink with realistic dimensions. So, the horizontal configuration was chosen. The stack-up is represented in figure 4.1.

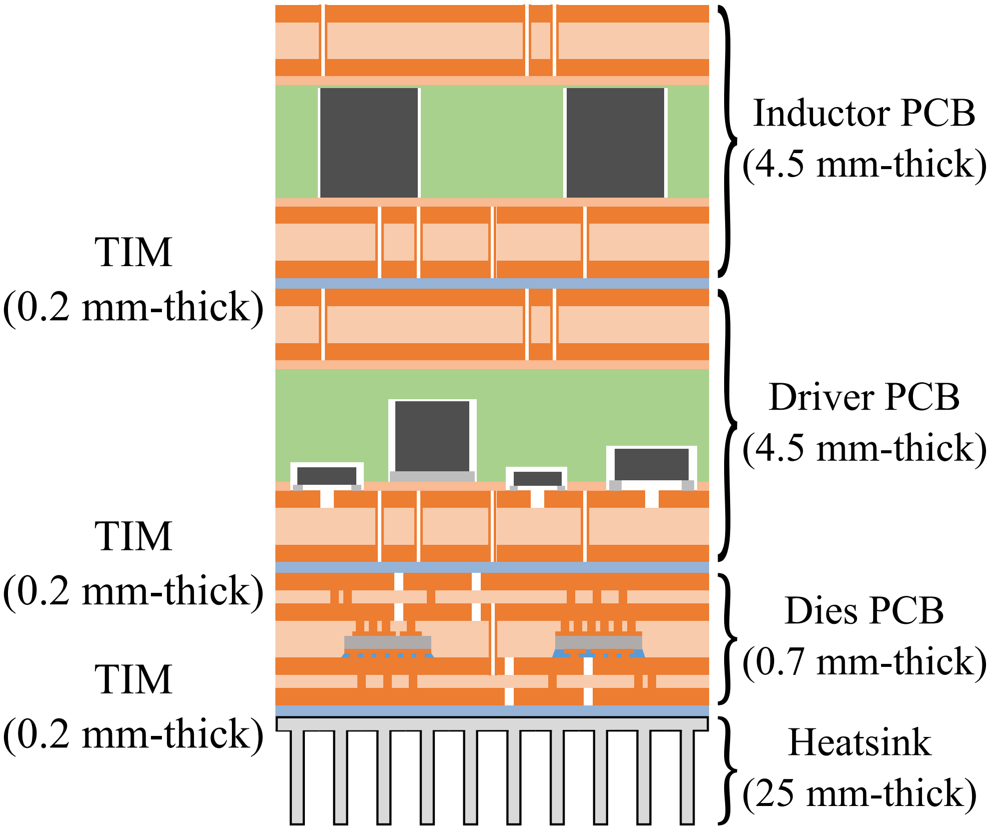


Figure 4.1: Stack-up of the PCB used for the thermal simulation. The thicknesses of the PCBs are exaggerated in regard of the heatsink thickness. The thermal vias and the PCBs interconnection wires are not represented.

4.4 Manufacturing Solution

As seen in chapter 2, a multilayer PCB can be assembled using different stack-ups. The choice is done according to the interconnections required between the copper layers. In this section, the manufacturing solutions used for the manufacturing of the prototype are presented and explained. It corresponds to the realization of the PFC (4 cells) and the DM EMI filter. The process flow was developed in collaboration with the PCB manufacturer Cimulec. The PCBs routing was done in this thesis. The PCBs routing objectives are to control the parasitic capacitors to reduce the EMI filter volume and to spread the heat properly to reduce the heatsink volume. More details on the different patterns are presented in chapter 5/section 5.2.

The PFC is formed of 4 interleaved cells composed of a full bridge, driven by 2 driver circuits, with an inductor connected to the midpoint of the high frequency leg. The DM EMI filter is formed with 4 similar PCBs, each corresponding to a single LC stage. Each stage of the DM EMI filter contains two embedded inductors and several embedded capacitors. A photo of each PCB is presented in figure 4.2.

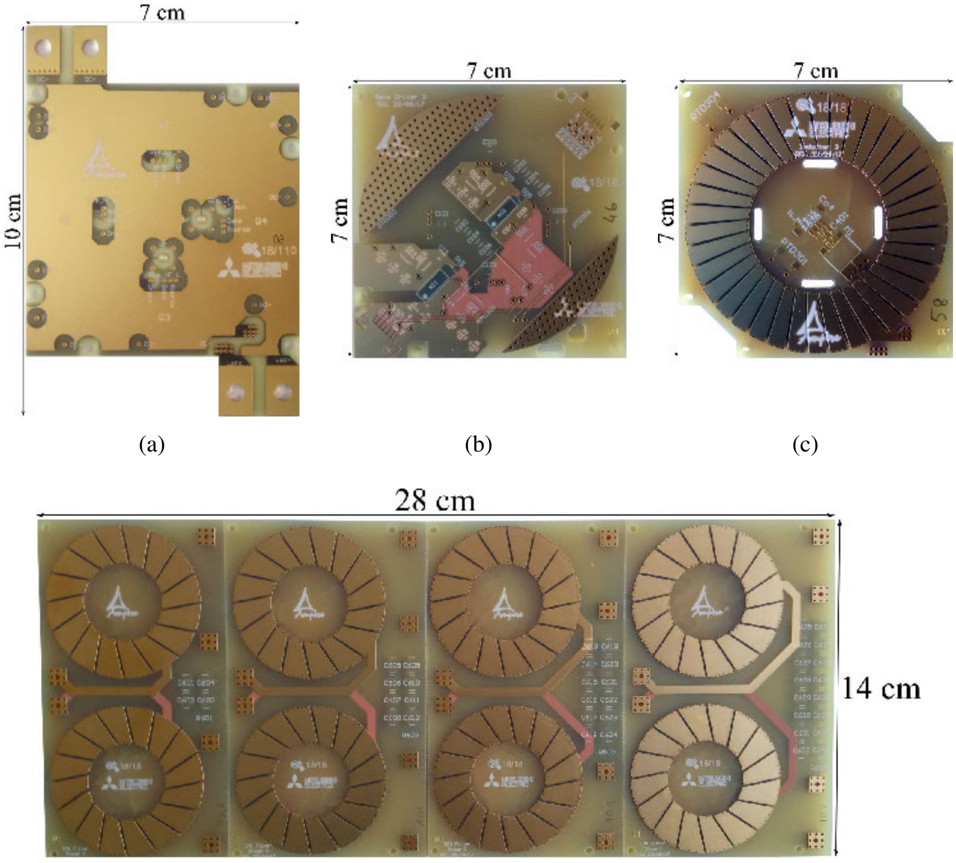
The prototype is manufactured with 2 different PCB panels due to the incompatibility between interconnection of power dies and SMD components embedding. The first panel is called "thin PCB" and contains only embedded dies. The second panel is called "thick PCB" and contains embedded SMD components and magnetic cores. The layers are numbered from the top to the bottom. The top layer is the layer 1 while the bottom layer is the layer 4.

4.4.1 Thin PCB

The "thin PCB" panel is a 4-layer PCB in which the dies are embedded between the two inner layers (layers 2 and 3). The process is presented in figure 4.3.

The process starts with a $35\,\mu\mathrm{m}$ copper sheet (layer 3) on which the dies are positioned and bonded with non conductive glue. This step requires a good accuracy for the positioning. It also requires additional information (a drawing) to show the dies orientation. The additional drawing is made on a mechanical layer (which are non physical layers used to display information). The die footprint in the ECAD software is associated with a keying on a mechanical layer to show die orientation (Figure 4.4). In standard PCB, the keying is generally a point on the silk screen which shows the position of a pin of the corresponding component. However, at this step, there is not silk screen to show dies orientation so this information does not actually appear on the board.

The dies are positioned with an angle on the board. Here, the dies are placed with an angle of $45°$ or $225°$. These two angles cannot be differentiated for flipped dies



(a) (b) (c)

(d)

Figure 4.2: Photograph of the (a) "thin" PCB with 4 embedded dies. (b) "thick" PCB with 2 embedded driver circuits (c) "thick" PCB with 1 "Embedded Toroidal" inductor. (d) "thick" with an embedded DM EMI filter.

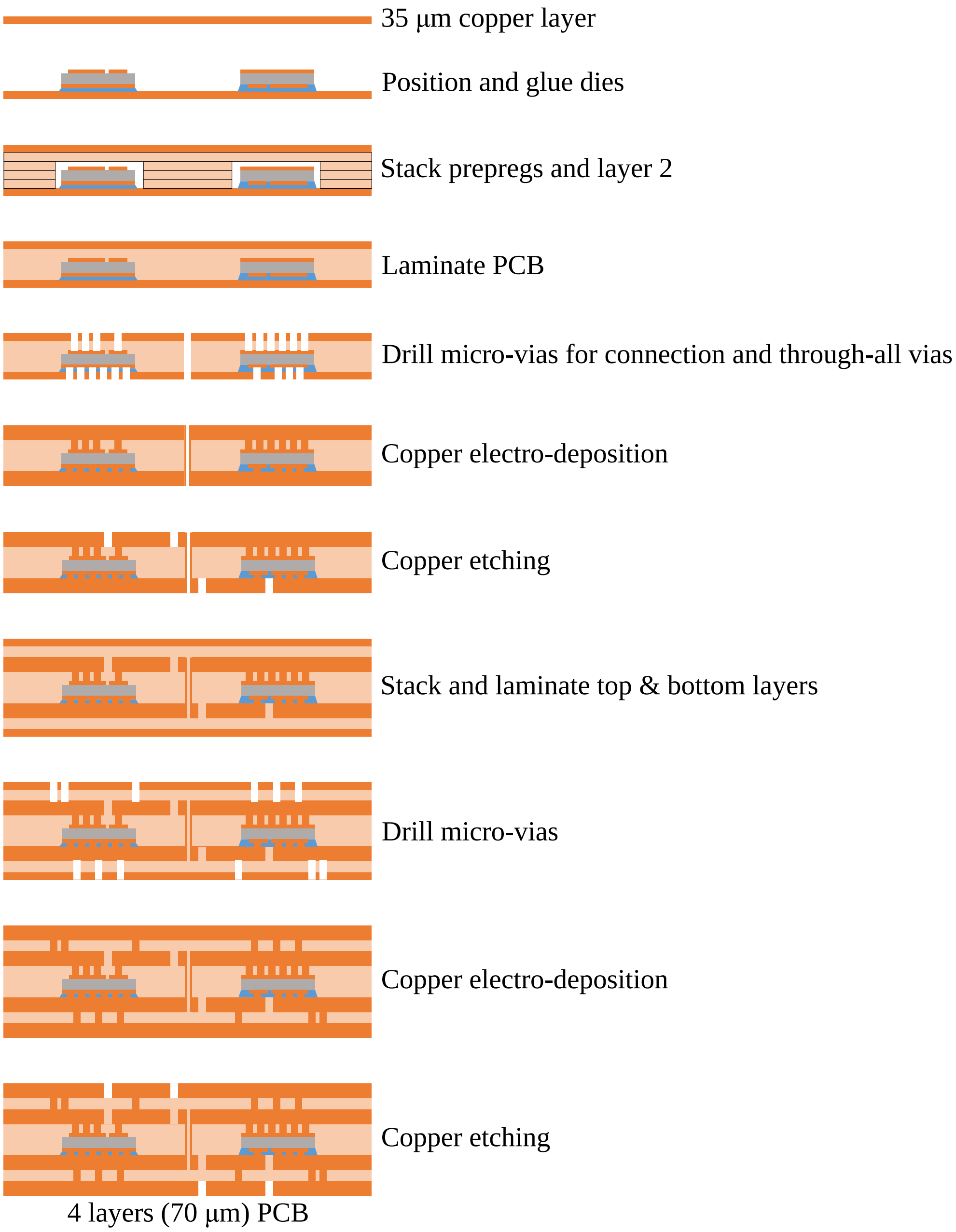
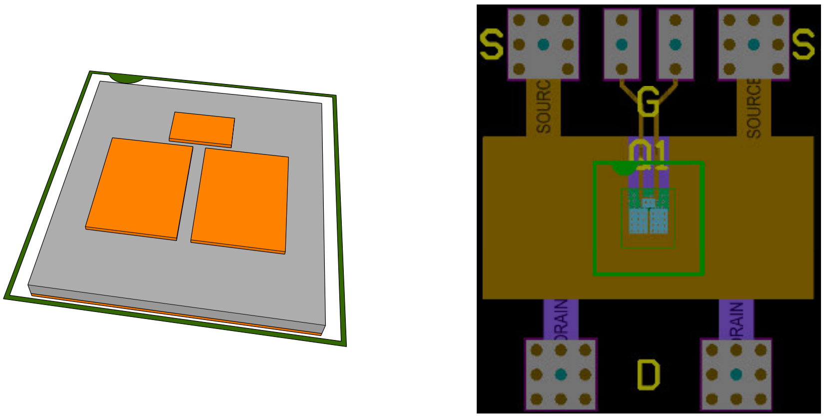


Figure 4.3: Manufacturing steps for the panel with embedded dies: "Thin PCB". Connections are not representative.

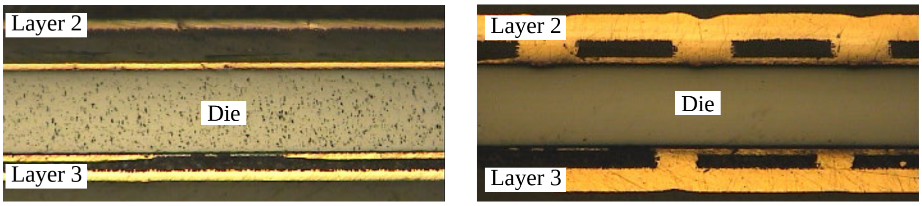


(a) (b)

Figure 4.4: (a) 3D drawing of a die with keying. (b) Picture of a GERBER with apparent die keying on mechanical layer.

with an observation from the top because the drain pad takes the entire surface of the die. On the 4 dies in a PFC cell, there are two flipped dies. The mix between the non-flipped and flipped dies improves the routing of the power nets. Indeed, the source of the top die and the drain of the bottom die for both legs are placed on the same layer. It is also the case for the DC nets. The non-flipped dies have their gate pad toward the top layer. On the contrary, the flipped dies have their gate pad facing the bottom layer. The dies are positioned properly thanks to the keying on the drawing and their known orientation in the chip tray.

In order to compensate for the die thickness, prepreg layers are used. The openings in the prepregs (which forms the cavities) cannot be cut using a laser because it would polymerize the resin of the prepregs at the edges of the openings. Then, the resin would not be able to fill the cavity during the lamination. Instead, the cutting is done using a drilling tool. Plain prepreg layers are added above the cut prepreg layers for the isolation between the dies and the copper layers. The standard practice for the PCB manufacturer is to use 2 plain prepreg layers. In order to reduce the thickness of the PCB and thus to improve the thermal capability of the converter stack-up, it was decided to use only 1 prepreg layer. As this might be insufficient to ensure the proper filling of the cavity (not enough resin available in the prepregs around the cavity), a test was performed on another panel. This test did not show any issue. So the stack-up to form the cavity used the copper sheet with glued dies, 3 cut prepreg layers to compensate the dies thickness, 1 full prepreg layer and the top copper sheet (layer 2). This stack-up is laminated to form a solid assembly. A picture of this assembly is shown in figure 4.5a.



(a)

(b)

Figure 4.5: (a) Cross section of the 2 layers PCB with embedded dies before drilling microvias. (b) Cross section of the microvias connecting a die on both sides.

The dies interconnection is done on both sides using microvias. The microvias must be drilled on die pads so the die positioning has to be accurate. The die positioning and the laser drilling have an accuracy of $30\,\mu\mathrm{m}$ with this stack-up. Also, the power of the laser must be set to stop the drilling within the thickness of the pads copper metalization. The pads copper metalization has a thickness of $8\,\mu\mathrm{m}$ on both sides. Two laser setting must be used because the isolation thickness is different on both sides. The glue has a thickness of approximately $25\,\mu\mathrm{m}$ while the full prepreg layer has a thickness of approximately $50\,\mu\mathrm{m}$. A microsection of the microvias is shown in the figure 4.5b. Through-all vias can also be drilled to directly interconnect the layers 2 and 3.

Copper is electro-plated. The dies are now interconnected to the layers 2 and 3. After the copper electro-deposition, the thickness of the layers 2 and 3 is $70\,\mu\mathrm{m}$. The inner layers (layers 2 and 3) are then etched to form the PCB traces.

Then, the top layer (layer 1) and the bottom layer (layer 4) are added, using standard PCB technology. $35\,\mu\mathrm{m}$ copper sheets are bonded using 2 prepreg layers on each side. The stack-up is laminated to form a solid assembly. The microvias are drilled from layer 1 to 2 and from layer 4 to 3. Through-all vias are also drilled. Copper is electro-plated. The PCB is then a 4-layer PCB, each of them with a thickness of $70\,\mu\mathrm{m}$. The full assembly is shown in figure 4.6. It can be seen that the desired copper thickness ($70\,\mu\mathrm{m}$) is not fully achieved. The inner layers have a copper thickness of approximately $61\,\mu\mathrm{m}$ while the external layers have a copper thickness of approximately $84\,\mu\mathrm{m}$. It can also be seen that the microvias are not fully filled with copper creating a small recess on their surface. As this recess can degrade connection of stacked microvias, it was decided to not stack microvias to avoid this issue.

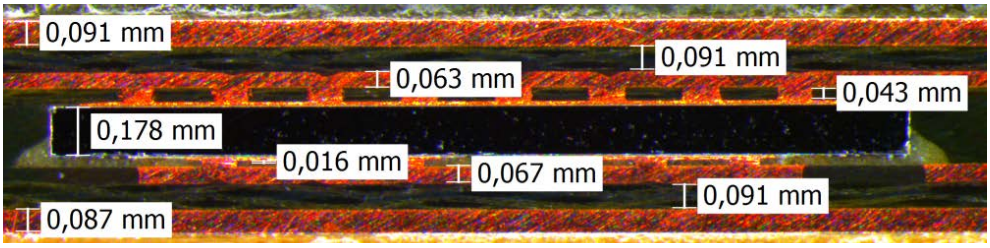


Figure 4.6: Cross section of a PCB with embedded dies according to the embedding process of the "Thin" PCB.

4.4.2 Thick PCB

The "Thick PCB" panel also has 4 layers, and the SMD components and magnetic cores are embedded between the two inner layers (layers 2 and 3). The process is presented in figure 4.7.

The process begins with a double-sided laminate with $70\,\mu\mathrm{m}$ thick copper. The first process steps are the same as for a standard PCB. The through-all vias are mechanically drilled. The copper is electro-plated to obtain connections between the two copper layers. The copper is then etched to form the circuit on both sides using a photo-resist and chemical etching as in the standard process.

The components are then mounted on layer 3. The solder paste is deposed by stencil-printing following the component footprint. The components are placed on the paste and the soldering process is done using a reflow soldering oven. Contrary to a standard PCB, the layer on which the components are mounted is not an external layer. So this layer does not have a solder mask. In order to achieve proper soldering without degrading the bonding of the stack-up, only a thin line of solder mask (green) is drawn around the components pads instead of covering the layer fully as it can be seen in figure 4.8.

First of all, 2 cut prepreg layers are placed on the layer 3. The aim of these prepreg layers is to bond the spacer and to isolate the magnetic cores from the layer 3. The spacer is composed of several PCB cores and prepregs layers. The cavity formed in the spacer should be just large enough to embed components while ensuring a filling by resin. The objective of the spacer is to protect SMD components and magnetic cores from mechanical pressure during the lamination step. Solder thickness has to be taken into account for the cavity height calculation. The stack-up of the spacer used to manufacture the first prototype of the "Thick PCB" is presented in figure 4.9. Note that this stack-up is relatively complex because no special care was taken regarding component selection (except a thickness inferior to $3\,\mathrm{mm}$). This

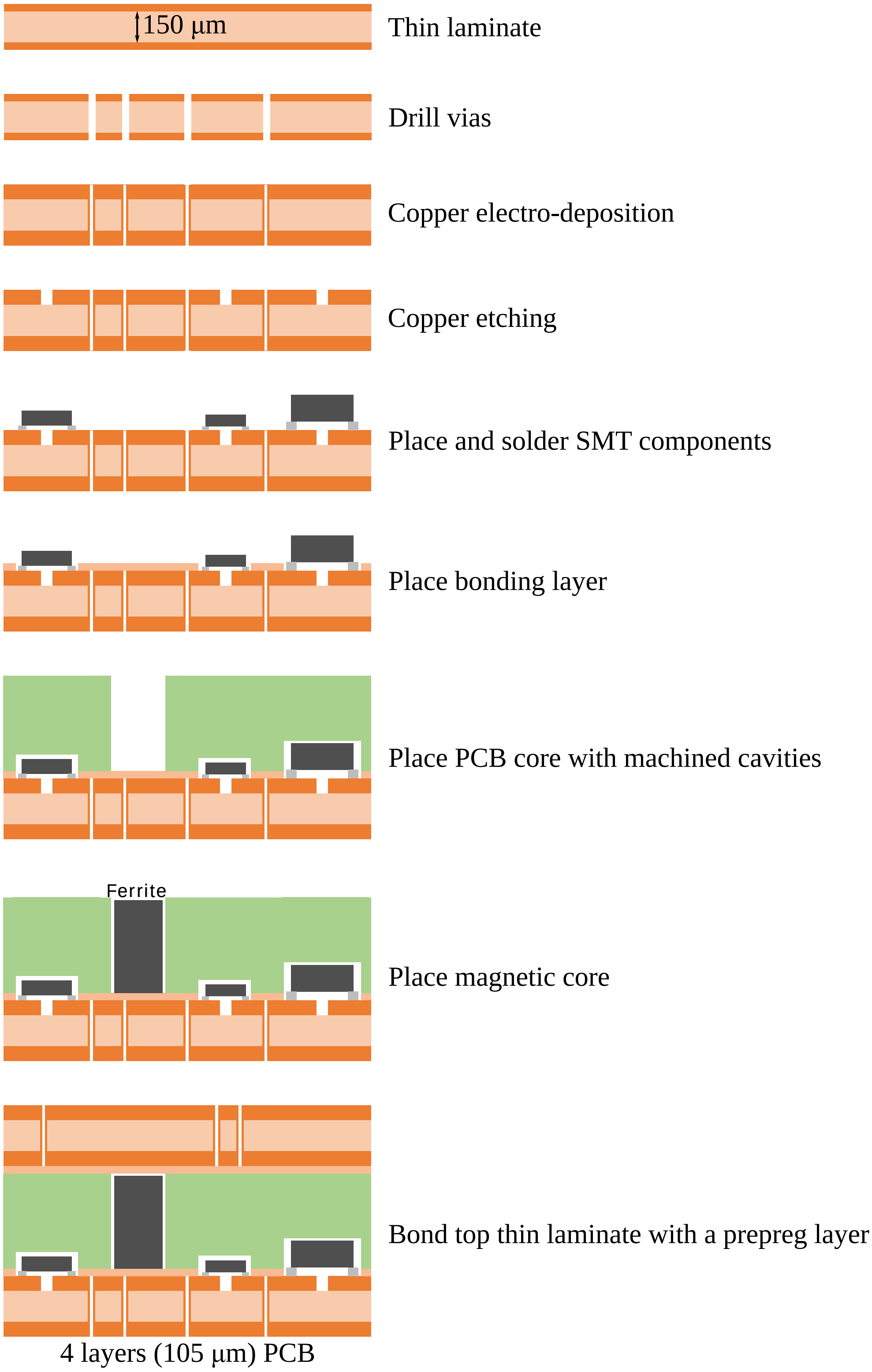


Figure 4.7: Manufacturing step for the panel with embedded SMT components and magnetic cores: "Thick PCB". Connections are not representative.

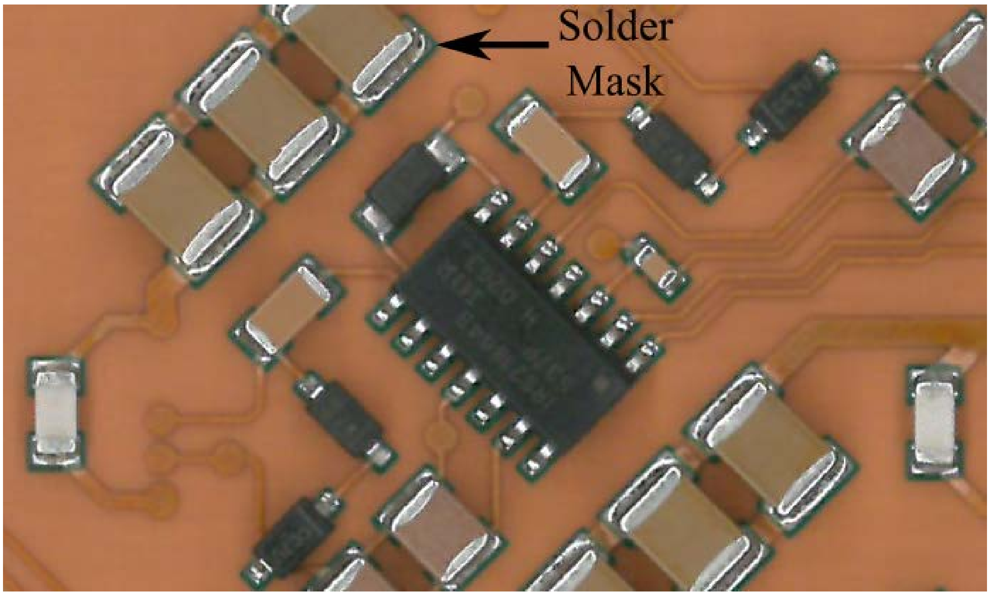
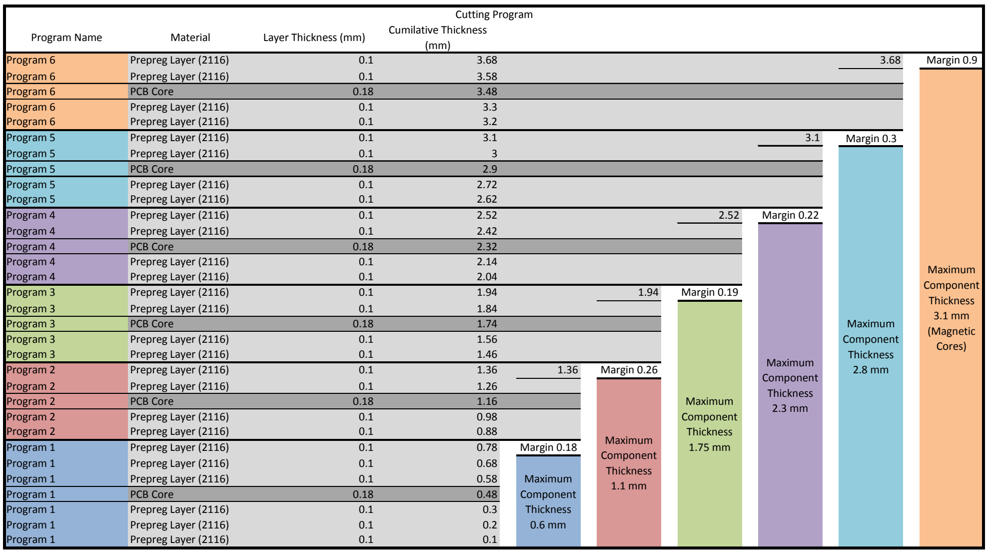


Figure 4.8: View of SMD components mounted on the layer 3. A fine line of solder mask (green) is deposited around each pad to prevent the solder attach from flowing along the copper tracks.

resulted in a large variety in component thicknesses. A much easier process could be achieved by selecting components with consistent thicknesses.

Then, above the spacer, two prepreg layers are placed to isolate the magnetic core from the layer 2. These two prepreg layers are also used to bond the laminate forming the layers 1 and 2. The laminate was previously manufactured in the same way as the laminate forming the layers 3 and 4. The full stack-up is then laminated to obtain a 4 copper layers PCB ($105\,\mu\mathrm{m}$). As for standard PCB, through-all vias can be manufactured to interconnect several layers with a particular attention to the components positioning. Although it is not as critical as with the "thin" PCB because in the "thick" PCB all vias are located between copper tracks, as in a conventional PCB (as opposed to the "track to dies" vias in the "thin" PCB). The through-all vias are used to form the inductor winding. Figure 4.10 presents a micro-section of the "Thick PCB". The embedded component is a 1206 SMD resistor. The green part is the solder mask as explained before. The final thickness of the PCB is $4.5\,\mathrm{mm}$.



Cutting Program

Program Name	Material	Layer Thickness (mm)	Cumilative Thickness (mm)
Program 6	Prepreg Layer (2116)	0.1	3.68
Program 6	Prepreg Layer (2116)	0.1	3.58
Program 6	PCB Core	0.18	3.48
Program 6	Prepreg Layer (2116)	0.1	3.3
Program 6	Prepreg Layer (2116)	0.1	3.2
Program 5	Prepreg Layer (2116)	0.1	3.1
Program 5	Prepreg Layer (2116)	0.1	3
Program 5	PCB Core	0.18	2.9
Program 5	Prepreg Layer (2116)	0.1	2.72
Program 5	Prepreg Layer (2116)	0.1	2.62
Program 4	Prepreg Layer (2116)	0.1	2.52
Program 4	Prepreg Layer (2116)	0.1	2.42
Program 4	PCB Core	0.18	2.32
Program 4	Prepreg Layer (2116)	0.1	2.14
Program 4	Prepreg Layer (2116)	0.1	2.04
Program 3	Prepreg Layer (2116)	0.1	1.94
Program 3	Prepreg Layer (2116)	0.1	1.84
Program 3	PCB Core	0.18	1.74
Program 3	Prepreg Layer (2116)	0.1	1.56
Program 3	Prepreg Layer (2116)	0.1	1.46
Program 2	Prepreg Layer (2116)	0.1	1.36
Program 2	Prepreg Layer (2116)	0.1	1.26
Program 2	PCB Core	0.18	1.16
Program 2	Prepreg Layer (2116)	0.1	0.98
Program 2	Prepreg Layer (2116)	0.1	0.88
Program 1	Prepreg Layer (2116)	0.1	0.78
Program 1	Prepreg Layer (2116)	0.1	0.68
Program 1	Prepreg Layer (2116)	0.1	0.58
Program 1	PCB Core	0.18	0.48
Program 1	Prepreg Layer (2116)	0.1	0.3
Program 1	Prepreg Layer (2116)	0.1	0.2
Program 1	Prepreg Layer (2116)	0.1	0.1

Figure 4.9: Description of the stack-up to realize the brace for the components embedding in "Thick PCB" (Document: Cimulec (PCB Manufacturer)).

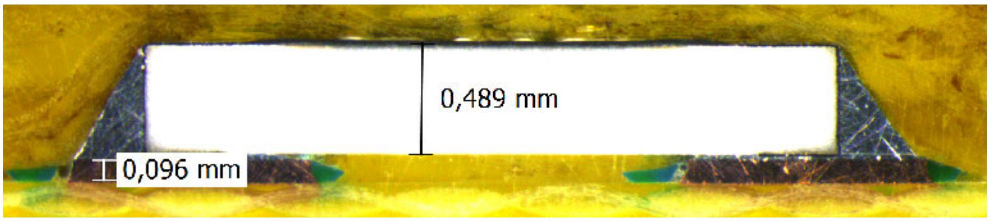


Figure 4.10: Micro-section of a 1206 SMD resistor with the process of "Thick PCB".

4.5 Converter Thermal Models

After the coarse thermal study to evaluate the assembly configuration for a PFC brick (see section 4.3), a more specific thermal study of the chosen assembly (horizontal) is presented below to evaluate components temperature. First, models of convection and radiation for the evacuation of the heat from the heatsink are presented. Second, models for the conduction inside the PCB are presented. For both parts, two models are studied. The objective is to compare the complexity and the computation time of these models, and to select the most suitable one in our case. A comparison with experiment will be performed in chapter 5 to assess the accuracy of the models.

4.5.1 Heatsink Models

A heatsink is used to increase the exchange surface between the converter and its environment, so as to improve heat removal. The heatsink uses convection and radiation to transfer heat to the environment. These two mechanisms have to be modeled in order to have a heatsink properly designed according to the converter needs.

In the following, two models are compared. The first model considers a heat transfer coefficient calculated using the heatsink dimension. The second model uses a heat transfer coefficient obtained by CFD (Computational Fluid Dynamics) finite element simulation of the heatsink. These two models are going to be compared with the geometry of the heatsink used for a PFC cell of the prototype. The dimensions of the parallel-plates heatsink (Machined SK42-75-SA from Fischer Elektronik) used in the following equations are presented in figure 4.11. The dimensions are the following: L_{base} $=70\,\mathrm{mm}$, $L = 70\,\mathrm{mm}$, H $=21\,\mathrm{mm}$, e $=2\,\mathrm{mm}$ and d $=5\,\mathrm{mm}$. The ambient temperature is $60\,^{\circ}\mathrm{C}$. The fin height was chosen just above the calculated value (H $=15\,\mathrm{mm}$) in the available heatsink. The baseplate is considered perfect with a negligible thermal resistance and a heat source uniform on its surface.

Analytical model

The first model is based on [51]. The heat transfer coefficient is calculated using fluid dynamics equations in which a straight fin heatsink is seen as several parallel plates.

The heat transfer coefficient h is defined by equation (4.3).

$$h = \frac{\lambda \cdot N_{U_{D_H}}}{D_H} \tag{4.3}$$

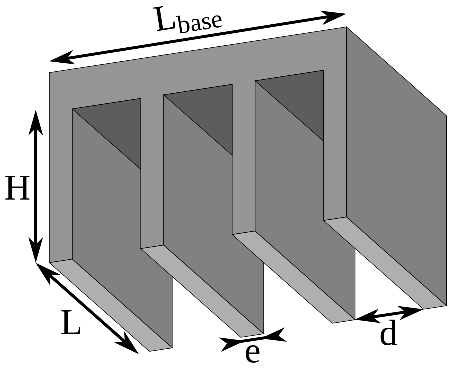


Figure 4.11: Drawing of a straight fin heatsink with dimensions used in heat transfer models.

where λ is the thermal conductivity of the fluid, $N_{U_{D_H}}$ is the Nusselt number and D_H is the hydraulic diameter. The Nusselt number $N_{U_{D_H}}$ is defined by equation (4.4).

$$N_{U_{D_H}} = \left[\frac{576}{\left(R_{a_{D_H}} \cdot \frac{D_H}{L}\right)^2} + \frac{2.873}{\left(R_{a_{D_H}} \cdot \frac{D_H}{L}\right)^{0.5}} \right]^{-0.5} \tag{4.4}$$

where $R_{a_{D_H}}$ is the Rayleigh number defined by the equation (4.5):

$$R_{a_{D_H}} = \frac{g \cdot \alpha \cdot \Delta T \cdot D_H^3 \cdot P_R}{\nu^2} \tag{4.5}$$

with g the gravitational constant ($9.81\,\mathrm{m}^2/\mathrm{s}$), α the thermal expansion ($1/T$ for gases), ΔT the temperature difference between heatsink and environment, P_R the Prandtl number (0.7) and ν the kinematic viscosity of air ($2.317 \times 10^{-5}\,\mathrm{m}^2/\mathrm{s}$). The hydraulic diameter is defined by equation (4.6).

$$D_H = \frac{2 \cdot H \cdot d}{2 \cdot H + d} \tag{4.6}$$

where H is the fin height and d is the spacing between two consecutive fins.

The fins efficiency η_{fins} is used to approximate the heat flux according to the real temperature distribution along the fins and to calculate the thermal resistance. It allows to take into account heatsinks with low fin thickness to height ratio (i.e. fins which are too thin to carry the heat up to their extremity). The fins efficiency η_{fins} is defined by equation (4.7).

$$\eta_{fins} = \frac{\tanh(H/H_c)}{H/H_c} \tag{4.7}$$

where H is the fin height. H_c, which is equivalent to a length, is defined by equation (4.8).

$$H_c = \frac{\lambda_{fins} \cdot A_b}{h \cdot P} \tag{4.8}$$

where λ_{fins} is the thermal conductivity of the heatsink material (Aluminum : $237\,\mathrm{W/(m\cdot K)}$ in our case), A_b is the base area of a fin ($e\cdot L$) and P is the perimeter of a fin ($2\cdot(e+L)$).

The convection heatsink thermal resistance can then be calculated using the equation (4.9)

$$R_{Conv}=\frac{1}{h\cdot(N\cdot S_{fins}\cdot\eta_{fins}+S_{base})} \tag{4.9}$$

where N is the number of fins, S_{fins} is the surface of a fin ($(2\cdot H+L)\cdot e+2\cdot H\cdot L$) and S_{base} is the surface of the heatsink baseplate without fins ($L_{base}\cdot L-N\cdot L\cdot e$).

In systems using natural convection, the radiation is a non negligible part of the thermal flux. The radiation flux ϕ_{Rad} between a surface of area A at a temperature T and its environment at T_{env} is given by the Stefan-Boltzmann law:

$$\phi_{Rad}=\sigma\cdot\epsilon\cdot A\cdot(T^4-T_{env}^4) \tag{4.10}$$

where σ is the Stefan-Boltzmann constant ($5.67\times10^{-8}\,\mathrm{W/(m^2\cdot K^4)}$) and ϵ is the emissivity of the heatsink material. However, with the complex geometry of a heatsink, a part of the heat radiated by a fin is absorbed by its neighbors. A view factor has to be defined to calculate the difference between the radiation emitted and received by a surface. In [67], a model is introduced for straight-fin heatsinks. The view factor F for surfaces in vis-a-vis is defined by equation (4.11).

$$F=1-\frac{2\cdot\overline{H}\cdot\left(\sqrt{1+\overline{L}^2}-1\right)}{2\cdot\overline{H}\cdot\overline{L}+\sqrt{1+\overline{L}^2}-1} \tag{4.11}$$

where $\overline{H}=\frac{H}{d}$ and $\overline{L}=\frac{L}{d}$. The thermal flux due to radiation ϕ_{rad} for a straight-fin heatsink is then calculated with equation (4.12).

$$\phi_{Rad}=\sigma\cdot(T^4-T_{env}^4)\left(\epsilon\cdot A_{ext}+(N-1)\cdot\frac{(d+2\cdot H)\cdot L}{\frac{1-\epsilon}{\epsilon}+\frac{1}{F}}\right) \tag{4.12}$$

where A_{ext} is the external surface of the heatsink ($N\cdot(L\cdot e+2\cdot H\cdot e)+2\cdot H\cdot L$). The thermal resistance due to the radiation R_{Rad} is calculated using equation (4.13)

$$R_{Rad}=\frac{(T-T_{env})}{\phi_{rad}} \tag{4.13}$$

In the heatsink model, the thermal resistance between the heat sources to the fins base is not taken into account. So, the thermal resistance of the heatsink R_{Ht} is composed of the two thermal resistances (convection and radiation) in parallel:

$$R_{Ht}=\frac{R_{Conv}\cdot R_{Rad}}{R_{Conv}+R_{Rad}} \tag{4.14}$$

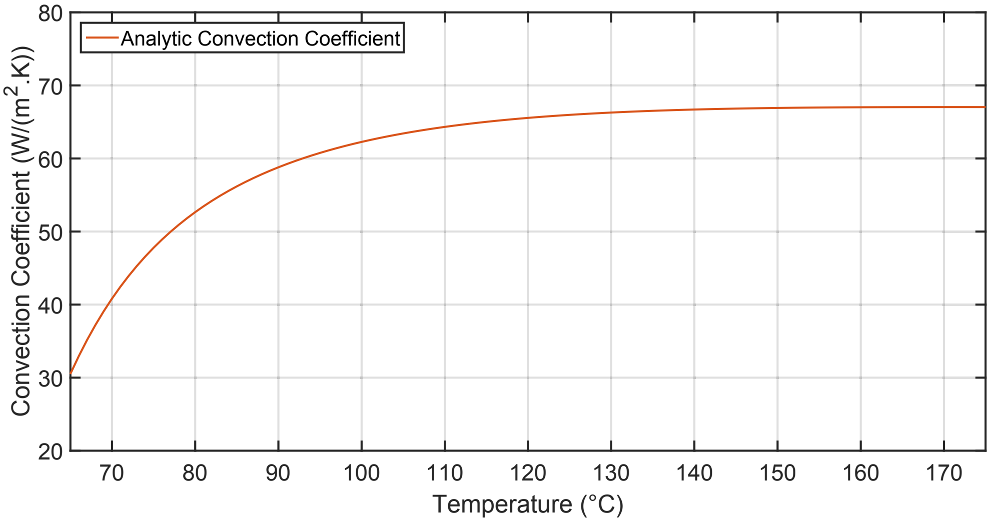


Figure 4.12: Equivalent heat transfer coefficient as a function of the temperature of the heatsink using the analytical model, and considering convection and radiation effects, for an ambient temperature of 60 °C.

As in the coarse estimation, it is possible to calculate the equivalent heat transfer coefficient h with the surface area of the baseplate A_{base} and the heatsink thermal resistance R_{Ht} using equation (4.3). The evolution of heat transfer coefficient as a function of the temperature is presented in figure 4.12.

CFD model

The second model is based on CFD (Computational Fluid Dynamics) using the Icepak software. The heatsink geometry is drawn in 3D. The heatsink is placed inside a cabinet which represents a large volume of air around the heatsink. The cabinet dimensions need to be larger (twice, in our case) than the heatsink dimensions so its boundaries do not disturb the airflow. The cabinet sides boundaries are closed, which means the air flow cannot cross them. On the contrary, the top and bottom boundaries are open. The gravity is applied on the z-axis. The radiation calculation is performed in addition to that of convection. A view of the graphic user interface with the different elements is presented in figure 4.13. The air flow velocity is represented by white arrows. The temperature is represented by the colormap.

A power dissipation using a uniform heat source is applied on top of the heatsink baseplate. The temperature of the heatsink is the results of the simulation. Note that in the example the heatsink temperature is at 180.6 °C (considered uniform) for a power loss of 50 W. The ambient air temperature is 60 °C. Several simulations are made with a power dissipation ranging from 1 W to 50 W. The heatsink tem-

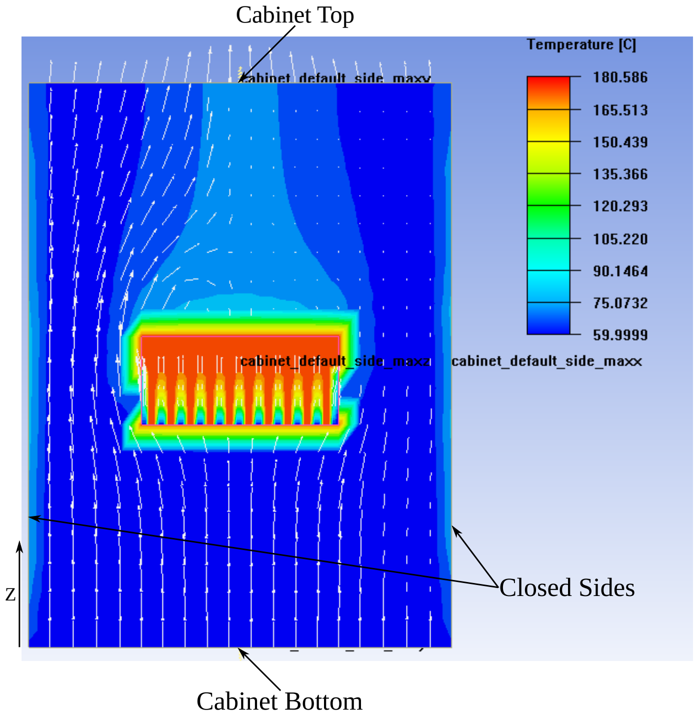


Figure 4.13: View of the Icepak graphic user interface with the heatsink used for the prototype. The air flow is represented by the white arrows. The temperature is represented by the colormap. The power dissipation applied on the baseplate of the heatsink is 50 W.

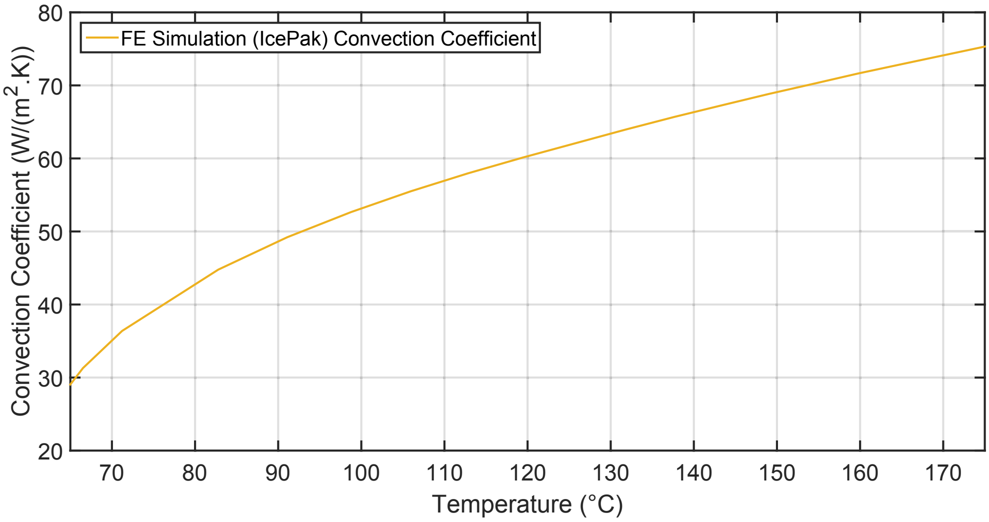


Figure 4.14: Equivalent heat transfer coefficient as a function of the temperature of the heatsink using the CFD model, and considering convection and radiation effects, for an ambient temperature of 60 °C.

perature is extracted for each simulation. The corresponding equivalent heat transfer coefficient h at baseplate level is defined with:

$$h = \frac{P}{A_{base} \cdot \Delta T} \tag{4.15}$$

with P the power dissipation, A_{base} the top surface area of the baseplate and ΔT the temperature difference between the heatsink and the environment. The heat transfer coefficient as a function of the temperature is presented in figure 4.14.

Comparison between the 2 heatsink models

Figure 4.15 presents the 2 models on the same graph.

The CFD model should have the best accuracy. The analytical model and CFD model accuracy are going to be validated against experiment on the prototype. But the CFD model has a computation time much higher than the analytical model. Once the script has been made, the heat transfer coefficient of a heatsink geometry can be obtained in a few seconds. While it takes approximately 1 h to draw the geometry and to make the simulation with an increasing power to obtain data for the temperature range needed. Still, the main drawback is the necessity of the CFD software.

This equivalent heat transfer coefficient (Equation obtained by a power curve fitting of the results) will be used to represent the heatsink in the PCBs stack-up simulation. It allows to reduce the computation time. Indeed, the simulation of the

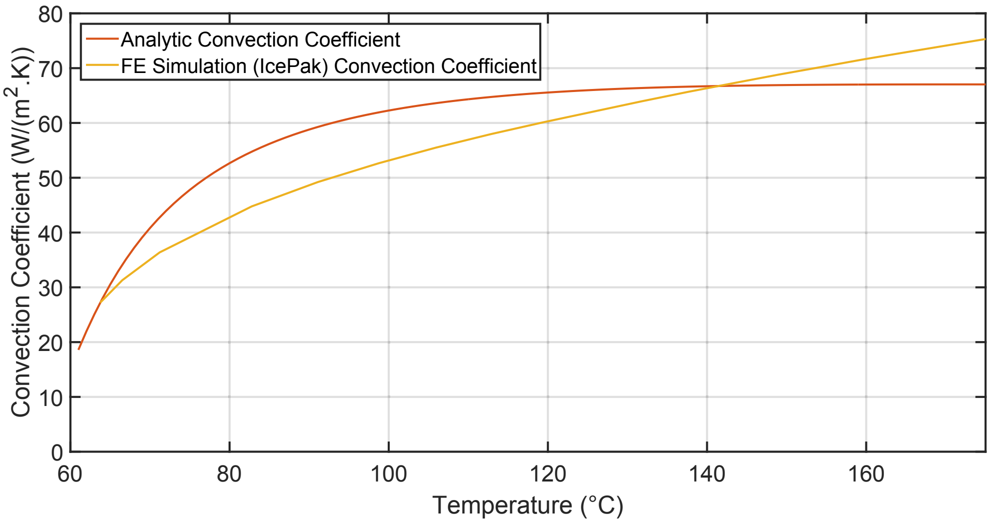


Figure 4.15: Equivalent heat transfer coefficient as a function of the temperature of the heatsink for the two models previously presented, and considering convection and radiation effects, for an ambient temperature of 60 °C.

PCBs stack-up does not have to be coupled with CFD simulation of the heatsink. In addition, heatsink fins are not represented, because the heat transfer coefficient is calculated at baseplate level.

The maximum error between the analytical and the CFD models is approximately 20 %. As this corresponds to a fraction of the overall thermal resistance, junction to ambient, such an error is considered as acceptable and will be evaluated in the comparison with experiments.

4.5.2 PCB Models

The heat conduction in the PCB stack-up from the components to the interface with the heatsink is studied by 3D finite elements. The first model is called "Approximated Stack-up": the actual PCB tracks and thermal vias are not represented, the thermal conduction of each layer is adapted to represent the reality. The second model uses an imported (but simplified) geometry of the copper layout. These two simulations are done using COMSOL. The losses in the inductor are 8.25 W, uniformly distributed over the volume of the magnetic core. The losses in a high frequency die are 5.83 W (2 Dies). The losses in a low frequency die are 0.81 W. The losses in the driver components are assumed negligible.

Table 4.1: Thermal conductivities of the different layers for the approximated stack-up thermal model.

Layer Name	Thermal Conductivity (x,y,z)
Copper Layer : Plane	$\lambda = (400, 400, 400)\ \mathrm{W/(m \cdot K)}$
Copper Layer : PCB Traces	$\lambda = (0.3, 0.3, 400)\ \mathrm{W/(m \cdot K)}$
Substrate layer : Standard	$\lambda = (0.3, 0.3, 0.3)\ \mathrm{W/(m \cdot K)}$
Substrate layer : Vias	$\lambda = (0.3, 0.3, 50)\ \mathrm{W/(m \cdot K)}$
TIM	$\lambda = (1.8, 1.8, 1.8)\ \mathrm{W/(m \cdot K)}$
Baseplate	$\lambda = (237, 237, 237)\ \mathrm{W/(m \cdot K)}$

Approximated Stack-up

The objective of this simulation is to obtain a low computation time simulation giving acceptable results. In this approximated geometry, each layer is represented by a unique prismatic block. In order to represent the real geometry, the thermal conduction of each block is adapted. Indeed, a plain copper layer is going to spread the heat. On the contrary, a copper layer with PCB tracks covering only a small part of the surface is going to have a limited heat spreading. For the substrate layer, an area with a high concentration of vias will increase the thermal conductivity in the z-axis. These approximations are done to reduce the number of elements in the mesh. Indeed, each block is meshed with numerous elements. However, there are fewer singularities for the meshing than with a complex geometry (vias, PCB tracks). Thermal conductivities of the different layers are presented in table 4.1.

The thermal conductivity of the substrate layer is $0.3\,\mathrm{W/(m \cdot K)}$ taken from the datasheet. The thermal vias improve the z-axis thermal conductivity. The thermal conductivity of the z-axis for substrate layers is $50\,\mathrm{W/(m \cdot K)}$, calculated with the equations presented in the chapter 2, while the thermal conductivities in the x-axis and y-axis are the same as the raw material. The thermal conductivity of the copper is chosen at a value of $400\,\mathrm{W/(m \cdot K)}$. For the thin PCB traces, the thermal conductivities in the x-axis and y-axis are chosen at the value of the substrate layer because the heat spreading is negligible ($0.3\,\mathrm{W/(m \cdot K)}$). The thermal interface material has a thermal conductivity of $1.8\,\mathrm{W/(m \cdot K)}$ taken from the datasheet. As explained previously, the heatsink is only represented by its baseplate with the equivalent heat transfer coefficient on the bottom. The baseplate of the heatsink in aluminum is represented in the model which a thermal conductivity of $237\,\mathrm{W/(m \cdot K)}$. The heat transfer coefficient of the top surface of the PCB stack-up is $12\,\mathrm{W/(m^2 \cdot K)}$ (approximation of a horizontal, plane surface) [66].

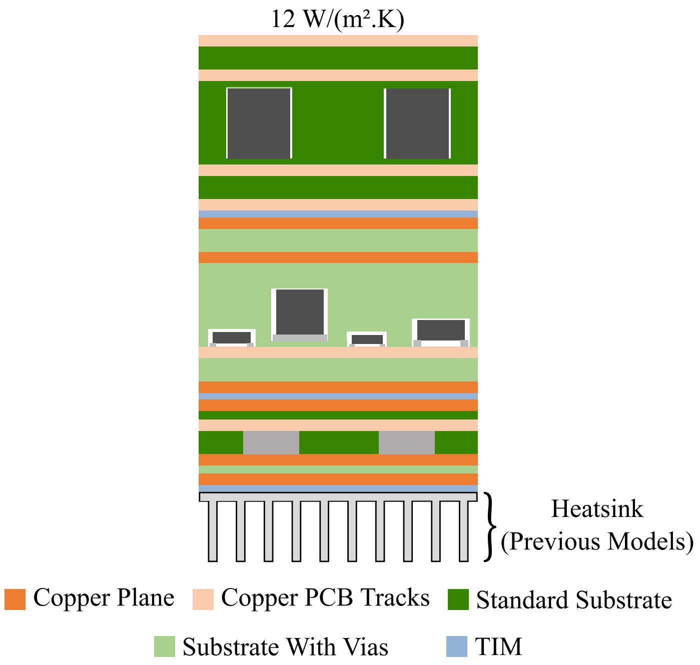


Figure 4.16: Stack-up used in the "Approximated Stack-up" model.

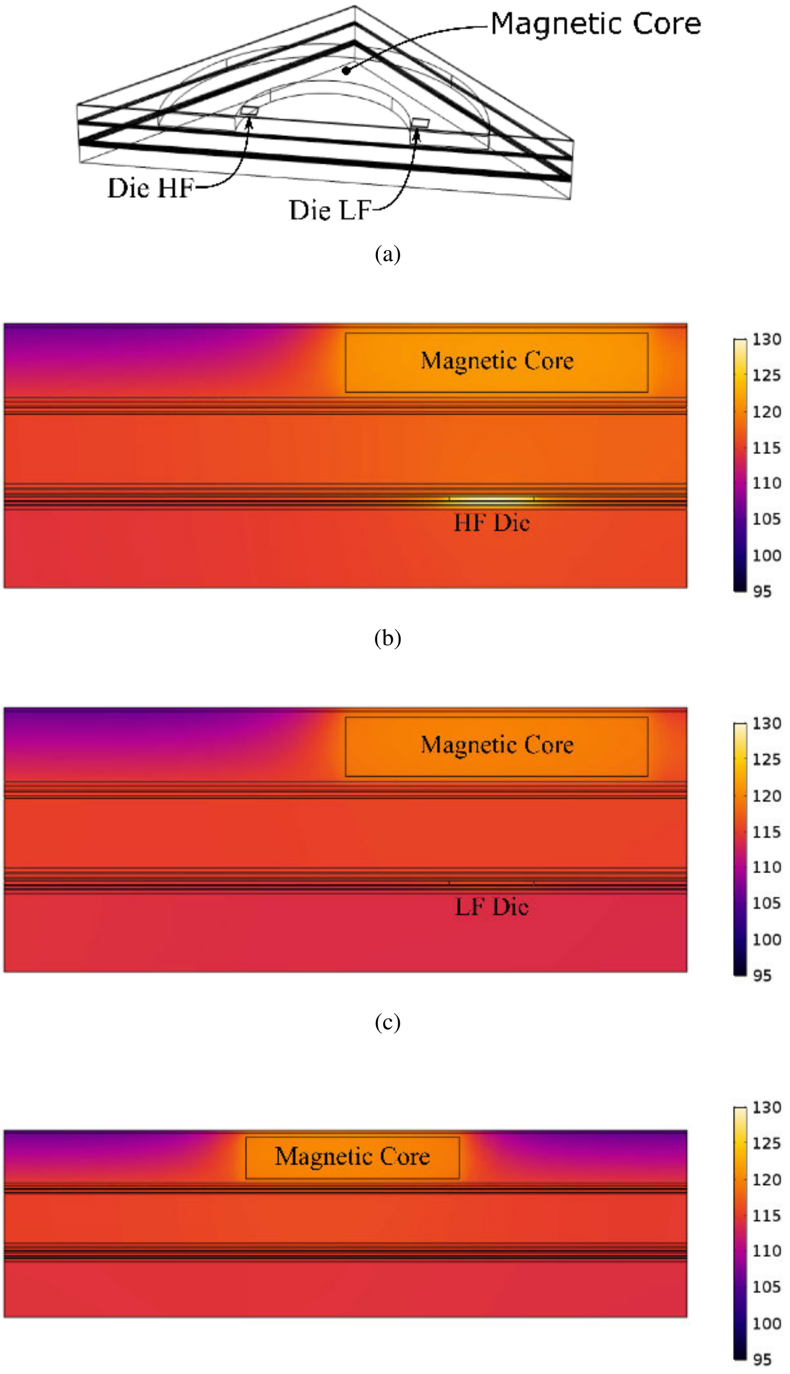
The stack-up is represented in figure 4.16. The results are presented in figure 4.17.

The PCBs stack-up models are going to be compared with the two heatsink models. But first, the second model PCBs stack-up model is presented.

Imported Stack-up

The imported model uses the ODB files generated from Altium designer to build a 3D model in COMSOL. The geometry is simplified to reduce the number of elements and to keep the computation time acceptable. In order to simplify the model, the driver PCB tracks and associated vias are removed. The copper planes for power nets and ground net are represented. The vias are also represented. The heatsink and the different TIM are added to the model. As for the previous model, the heatsink fins are represented through an equivalent heat transfer coefficient on the bottom of the baseplate. As in the previous model, the heat transfer coefficient of the top surface of the PCB stack-up is $12\,\mathrm{W}/(\mathrm{m}^2\cdot\mathrm{K})$.

Temperature plots obtained in cut planes are presented in figure 4.18.



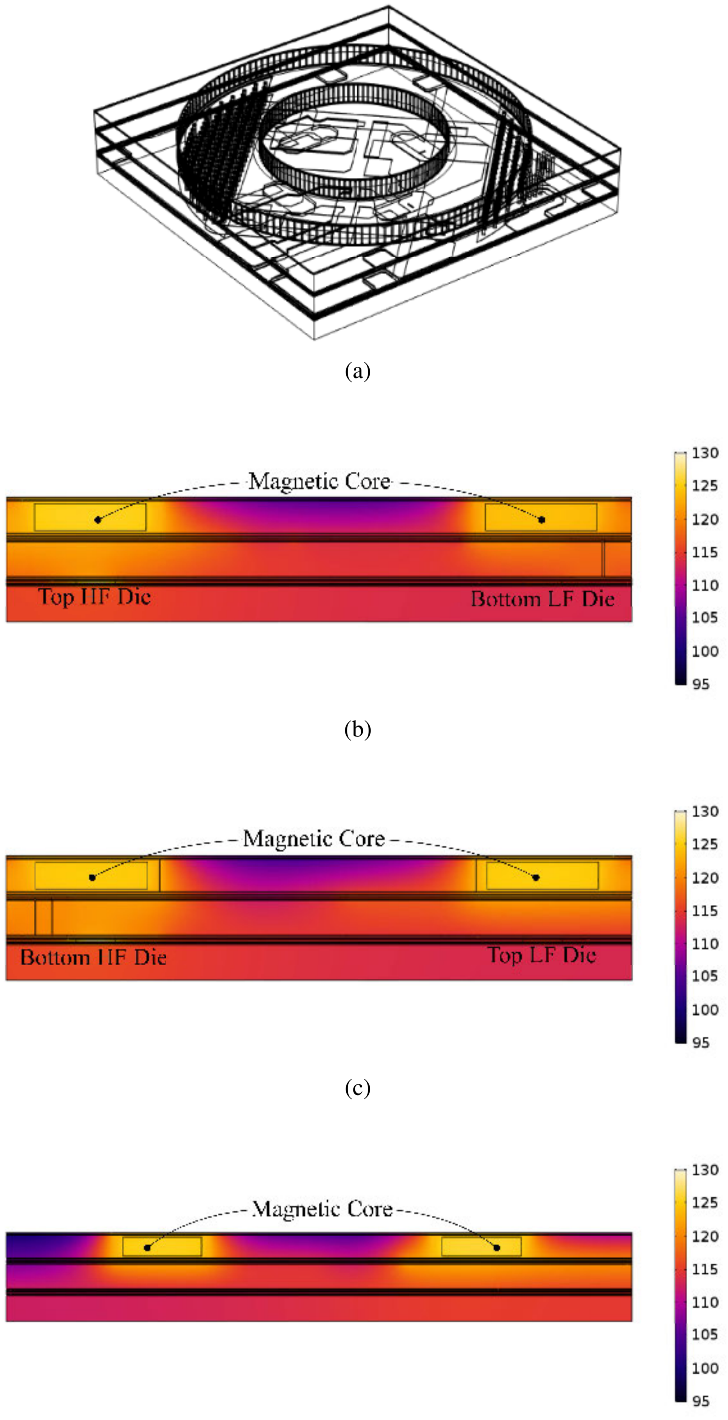
(a)

(b)

(c)

(d)

Figure 4.17: (a) Geometry of the "Approximated Stack-up" model. A symmetry is used to reduce the computation time. (b) Temperature plot of a cut plane cutting through the HF die and the center of the PCB. (c) Temperature plot of a cut plane cutting through the LF die and the center of the PCB. (d) Temperature plot of a cut plane cutting through the diagonal of the PCB.



(a)

(b)

(c)

(d)

Figure 4.18: (a) Geometry of the "Imported Stack-up" model. (c) Temperature plot of a cut plane cutting through the top HF die and the bottom LF die. (c) Temperature plot of a cut plane cutting through the bottom HF die and the top LF die. (c) Temperature plot of a cut plane cutting through a diagonal of the PCB.

Table 4.2: Temperature comparison of the 4 models developed.

Name	Approximated Stack-up		Imported Stack-up	
Heatsink Model	CFD	Analytic	CFD	Analytic
Die HF	129.1 °C	131.1 °C	128.2 °C	130.9 °C
Die LF	115.8 °C	118.3 °C	115.6 °C	118.2 °C
Magnetic Core	121.4 °C	123.9 °C	125.5 °C	127.9 °C
RTD Die HF	118.0 °C	120.5 °C	121.3 °C	123.8 °C
RTD Die LF	115.5 °C	118.0 °C	116.2 °C	119.4 °C
RTD Inductor Outer	114.8 °C	116.8 °C	118.9 °C	118.8 °C
RTD Inductor Inner	115.3 °C	117.8 °C	119.1 °C	119.2 °C

Comparison both conduction models

The temperature comparison for both models is presented in table 4.2. The temperatures are taken at the component center and at the RTDs (Resistive Temperature Devices) location (as these sensors will be used in the experimental validation).

The temperature of high frequency dies is close to 130 °C. The temperature of the low frequency dies is close to 115 °C or 118 °C depending on the heatsink model used. The heatsink using the CFD model has a higher heat transfer coefficient compared to the heatsink analytical model at these temperature differences. This results in lower temperatures for the CFD model.

With the same heatsink model, the approximated stack-up model is pessimistic compared to the model using imported stack-up. It is due to the limited interaction between die PCB (Bottom) and inductor PCB (Top) through the driver PCB. The biggest temperature difference between the two stack-up models is 4.1 °C for the magnetic core with CFD model. This temperature error is considered acceptable.

The temperature of the dies, which are the hottest points in the structure, are in the acceptable range (their datasheet indicates a maximum junction temperature of 175 °C). However, the losses calculation was realized considering a junction temperature of 150 °C. The calculated losses are then over-estimated. This observation is also true for the magnetic material (119 °C). The driver PCB which is placed at the middle has components with a maximum temperature of 125 °C. The maximum obtained temperature is 123.8 °C for the RTD HF die which is embedded in the driver PCB. The driver components are therefore working at an acceptable temperature.

The accuracy of these models is going to be checked with experiment in the chapter 5. The model using the analytical model for the heatsink and the approximated stack-up model is the most suited for an optimization. It can be obtained only with

COMSOL (without additional COMSOL module). The CFD model needs the IcePak software. In addition, the computation time is approximately $1\,\mathrm{h}$ for only $1\,\mathrm{min}$ for the analytical model. For the imported stack-up an additional COMSOL module is needed (ECAD). The geometry also has to be simplified manually. The computation time is also higher ($1\,\mathrm{h}$) while it is approximately $10\,\mathrm{min}$ for the approximated stack-up model. The generation of the approximated stack-up model could be automated with an interface with MATLAB (additional COMSOL module). It was not the case in this study.

4.6 Parasitic Elements Analysis

The converter optimization script, which was introduced in the chapter 3, contains the choice of semiconductors and the design of the CM EMI filter. However, in the script, the parasitic elements are coarsely estimated, although they have a strong effect on the switching behavior of the transistors and on the EMC. Once the PCBs are routed, it becomes possible to compute the parasitic elements and to introduce them in the electrical model of the converter.

4.6.1 Parasitic Capacitors

The CM perturbations are conducted by the capacitances occurring between power nets and the ground net. The parasitic capacitors between the DC bus nets and the ground net have a positive impact on the filtering. On the contrary, the parasitic capacitors between the midpoints and the ground net have a negative impact [68].

In the first optimization iteration, the capacitance values were coarsely approximated. A $10\,\mathrm{nF}$ was considered between DC buses and the ground. A $1\,\mathrm{nF}$ was considered between midpoint nets and the ground. In order to have better approximation, the routing of the converter has to be known, which was not the case at that time. In this first iteration, no parasitic capacitors were considered in parallel of the switches. The parasitic capacitors values used for the first iteration are presented in figure 4.19.

Q3D extractor software (Ansys Electromagnetic) is used to compute the parasitic capacitances of the design. Q3D Extractor is based on the method of moments (MoM). These capacitances are compared to the capacitances chosen for the first iteration. Most importantly, the obtained values are used for a second optimization. The imported geometry is presented in figure 4.20.

As previously presented, the PCB with embedded dies has 4 copper layers. Both mid point nets, low frequency and high frequency, are routed on layer 2. The DC

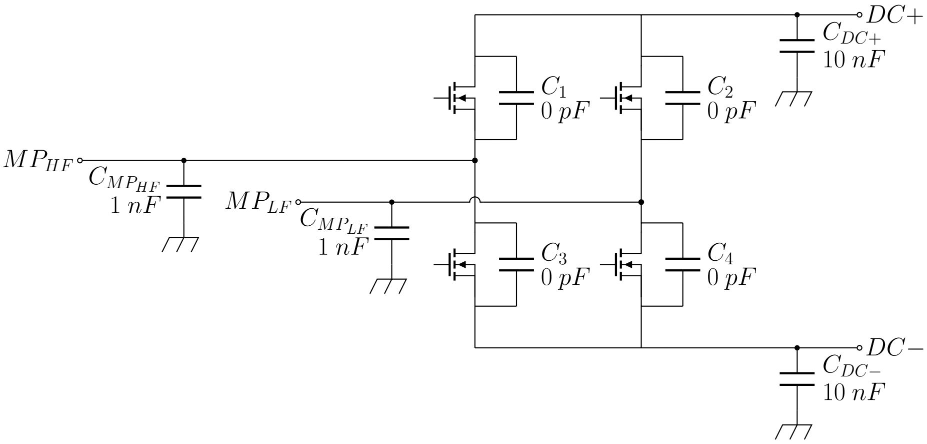


Figure 4.19: Circuit diagram of a PFC cell with parasitic capacitors. The first iteration of the converter optimization was done using values marked in the circuit.

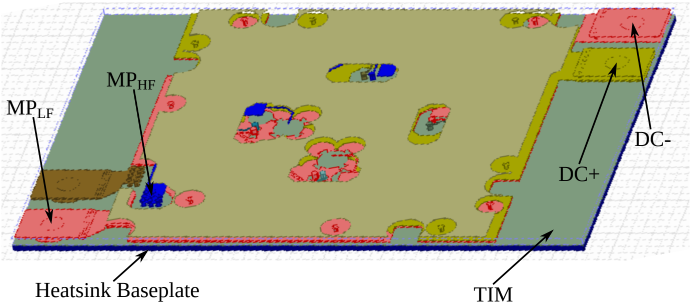
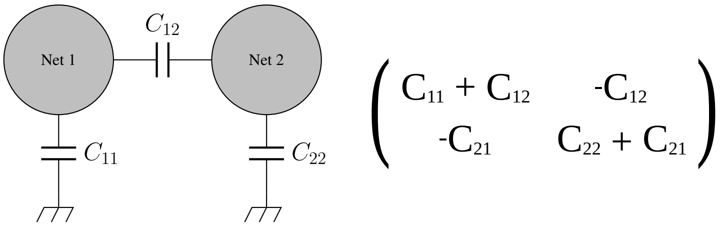


Figure 4.20: Picture of the imported geometry of the PCB with embedded dies in Q3D Extractor software.



(a) (b)

Figure 4.21: (a) Example of a circuit diagram with two nets and their parasitic capacitances (b) Corresponding Maxwell capacitance matrix.

nets, plus and minus, are routed on layers 3 and 4. The copper plane on the layer 1 is not connected to any net because it was not known which net would present the best interest. However, connection pads were placed on the top layer so this plane could be easily connected to the ground or one of the DC nets to study the impact of this layer. The layout of the dies PCB was designed to reduce the parasitic capacitors between mid-point nets and the ground. The routing on layer 2 of both mid point nets allows to reduce the surface in vis-a-vis between the midpoint nets and the ground (heatsink). Also, the parasitic capacitors with a positive impact on CM (i.e. those between the DC buses and the ground) are maximized. The DC nets are routed using copper planes while the mid point nets are routed using PCB tracks with a maximum width of $5.5\,\mathrm{mm}$, enough to carry the current, but thin enough to limit their capacitance.

The geometry of the PCB with embedded dies is imported from Altium Designer into Q3D Extractor using ODB files. Two blocks are added in the geometry under the PCB to represent the TIM and the heatsink baseplate as there are not taken into account in Altium and yet they have a major role in parasitic capacitances. The heatsink baseplate is the ground net.

Q3D Extractor gives the parasitic capacitors between each net under the form of a Maxwell capacitance matrix. The Maxwell capacitance matrix and the equivalent schematic are shown in figure 4.21. Note that $C_{12} = C_{21}$. The parasitic capacitances between each net are extracted from the Maxwell capacitance matrix. The frequency of the simulation is $500\,\mathrm{kHz}$. The capacitor values obtained by simulation have a small variation on the EMC standard range ($150\,\mathrm{kHz}$ to $30\,\mathrm{MHz}$).

The parasitic capacitors values given by the simulation are presented in figure 4.22. It appears that compared to figure 4.19, the parasitic capacitors with the ground were highly overestimated. The biggest value is $561.1\,\mathrm{pF}$ for the capacitor between DC- net and ground. The value between DC+ net and ground is $65.5\,\mathrm{pF}$.

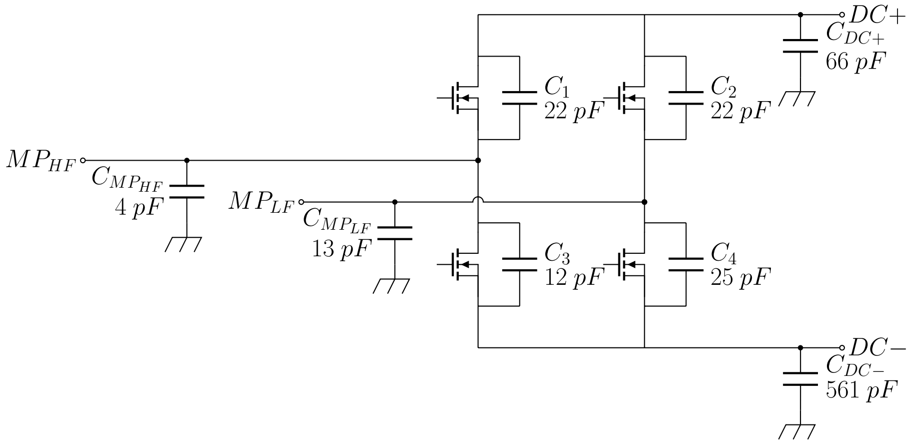


Figure 4.22: Circuit diagram of a PFC cell with parasitic capacitors values obtained using Q3D software. Several nets layouts are presented in figure 4.23.

These two capacitors have a positive impact on the CM filtering so the first iteration was too optimistic. However, the capacitors between the midpoint nets and the ground were also highly overestimated. Indeed, the capacitor between the high frequency mid point and the ground is $3.6\,\mathrm{pF}$ while the capacitor between the low frequency mid point and the ground is $12.9\,\mathrm{pF}$. The first iteration was pessimistic. The parasitic capacitors in parallel with the switches ($22.2\,\mathrm{pF}$, $24.6\,\mathrm{pF}$ or $11.9\,\mathrm{pF}$) have values lower than those of the dies used in the prototype (output capacitance $C_{oss} = 80\,\mathrm{pF}$ for a CPM2-1200-0080B, Wolfspeed).

Because of time constraints, the prototype was designed based on the assumptions presented in figure 4.19. The simulation above was performed while the prototype was being built. The parasitic capacitors are going to be compared with the measured values in the chapter 5.

Parasitic inductance modeling was not addressed in this thesis, both because of lack of time and because the expected low inductance values would have been difficult to validate experimentally. The full power tests which are currently being carried out will confirm whether these inductors have a strong effect or not.

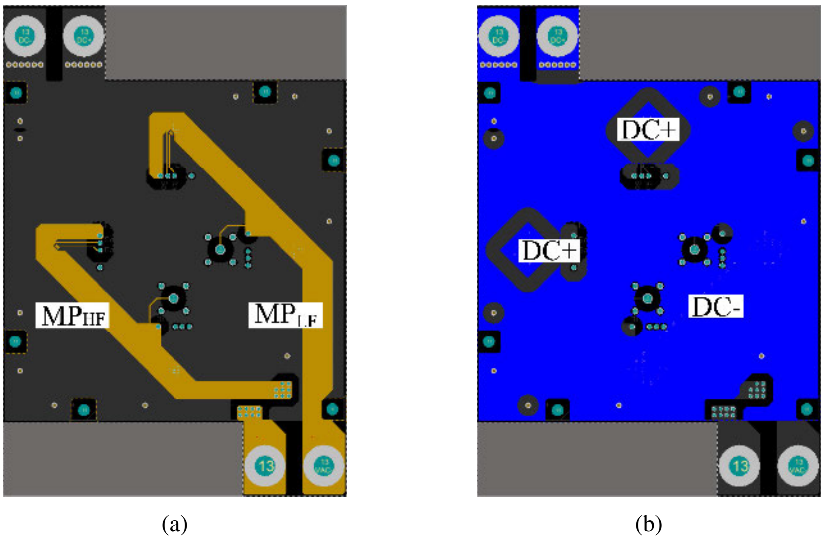


Figure 4.23: (a) Layout for the MP_{HF} and MP_{LF} nets. (b) Layout for the $DC-$ and $DC+$ nets.

4.7 Conclusion

In this chapter, the mechanical assembly of the converter was explained. The converter stack-up uses 3 PCBs (Die, Driver and Inductor). The heatsink is placed directly under the PCB with embedded dies as they are the most demanding components regarding thermal management due to their higher losses density. The PCB with the embedded driver circuit is positioned just above the die PCB to limit the parasitic inductances of the interconnects. The manufacturing process for each PCB was explained. The process uses standard steps but many components are inserted during PCB manufacturing to produce the embedding. This cause the manufacturing process to become more complex, with additional description required in the design files (location and orientation of the dies, for example), and with much more manufacturing steps (e.g. the multi-level cutting program required to accommodate the many components heights on the gate driver board). Improvement can be made in a second prototype to simplify manufacturing.

The 3 PCBs stack-up and the heatsink were modeled with several thermal models. The models were compared regarding their temperature predictions and computation time. The components temperatures are expected to be high (123.8 °C for driver components and approximately 130 °C for high frequency dies) but they remain within the specification for these components. The models are going to be compared with experiment in chapter 5.

The parasitic elements of the PCB with embedded dies were studied. The simulation gave more precise parasitic capacitors values than the one used for the first iteration. The parasitic capacitors were highly overestimated in the first iteration. The parasitic capacitors between the midpoints and the ground have low value thanks to the routing ($4\,\mathrm{pF}$ and $13\,\mathrm{pF}$) compare to the parasitic capacitors between the DC nets and the ground ($561\,\mathrm{pF}$ and $66\,\mathrm{pF}$). This will allow to down size the CM EMI filter in a new iteration. However, both DC nets should be equal ideally present similar capacitances to ground in a new routing to maximize symmetry and prevent mode transfer. The simulated values are going to be compared with the experiment in the chapter 5.

The next chapter will present the experimental results obtained with the prototype. The tests are going to be performed on individual elements to check their functionality and the impact of the embedding technology as well as on the full converter.

Chapter 5

Experimental study

5.1 Introduction

The models used for the inductor optimization script (chapter 3) were simple in order to keep a short computation time. Chapter 4 addressed the converter implementation, which enabled more detailed models to be generated, in particular thermal models and models of the parasitic capacitance. Here, we consider the experimental results from the prototype to validate the models predictions. The objective is to check the accuracy of the optimization script or to improve it for the purpose of a new prototype.

As a reminder, the converter was optimized considering efficiency and power density. It is also based on the use of an innovative design for the power inductors, despite the not standard manufacturing process. So, the models used for the calculation of the volume and the losses will be checked.

The full bridge of a PFC cell and the associated driver circuits were implemented using PCB embedding technology. As the effect of this technology on the performances of the components is unknown, it needs to be evaluated. Individual test coupons were designed and built, and their characterization is presented in the section 5.3 of this chapter, along with tests of the main functional blocks of the converter (gate driver, EMI filter). The thermal models developed in the previous chapter are compared with temperature measurements in section 5.4. Finally a full section is dedicated to the embedded inductors, as they were found to behave very differently from what was expected. 3D FEM simulations and additional experiments are performed to analyze this difference.

5.2 Prototype PCBs Overview

For the description of the "Thin" and "Thick" panels, please refer to chapter 4 page 81.

"Thin" Panel

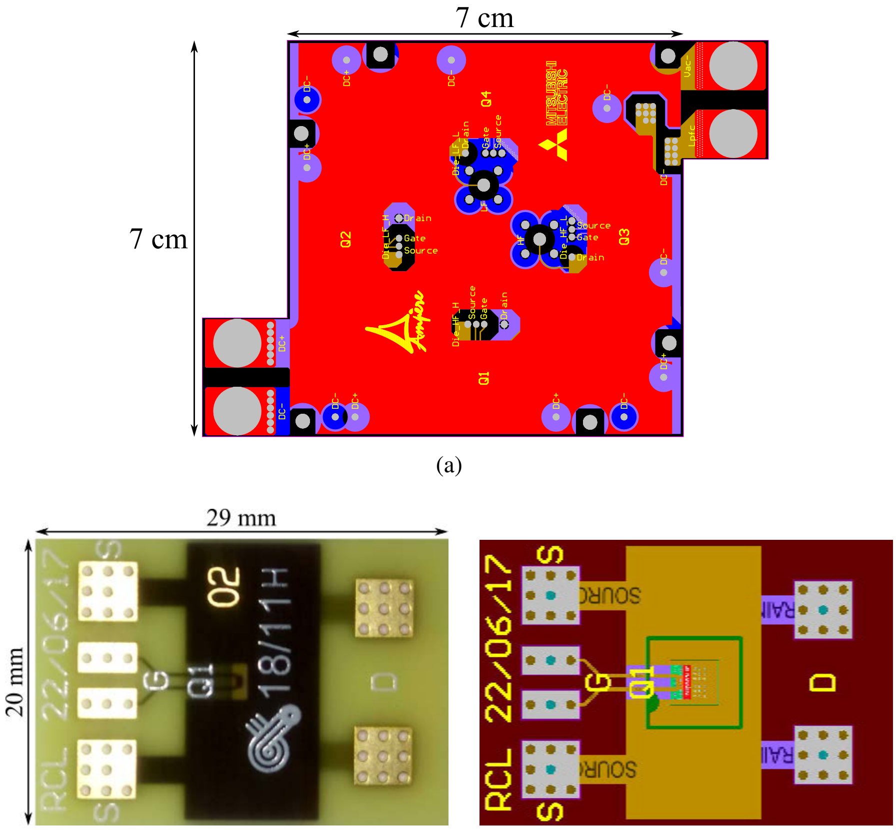
In the "thin" panel, only dies are embedded. This panel has only 2 patterns. The first pattern (Figure 5.1a) has 4 embedded dies with 2 mounted face-up (non-flipped) (Q1 and Q2) and 2 mounted flip-chip (Q3 and Q4). This pattern is the full bridge used in a PFC cell. The optimal converter uses 4 interleaved cells (i.e. 4 boards with such pattern). However, note that in this prototype, each switch of the full bridge is composed of one single $1200\,\mathrm{V}$ MOSFET, while the optimum converter would require two $900\,\mathrm{V}$ MOSFETs in parallel. Indeed, only CPM2-1200-0080 MOSFETs with suitable Cu finish were already available which offered a drastic reduction of the production time. Overall, 9 boards with this pattern were manufactured, but could not be tested before delivery because of the embedded components. This is true for all the boards presented in this thesis. The first objective of the tests presented here was to check the functionality of each board we received.

The second pattern of the "thin" panel is a coupon, with only one die embedded mounted face-up (5.1b and 5.1c). This coupon is used for the characterization of SiC dies after embedding. 8 boards were delivered.

"Thick" Panel

The "thick" panel is composed of 9 patterns. The first 3 are used in the converter already presented: the first one is a PCB with 2 embedded driver circuits. It is placed directly above the PCB with embedded dies in a PFC cell and used to drive the switches. The second one is the PCB with the "Embedded Toroidal". It is placed on the top of a PFC cell. The last pattern used in the converter is the DM EMI filter. It is composed of 8 "Embedded Toroidal" inductors and numerous capacitors. These patterns were already presented in figure 4.2.

The last six patterns are test coupons. There are test coupons with embedded diodes and embedded capacitors (Figure 5.2). There are 3 different capacitor coupons. The first embedded capacitor has a value of $330\,\mathrm{nF}$ for a nominal voltage of $500\,\mathrm{V}$ with a X7R classification. This capacitor reference is used as a decoupling capacitor between the DC nets. The second capacitor has a value of $56\,\mathrm{pF}$ for a nominal voltage of $500\,\mathrm{V}$ and is classified C0G. This capacitor reference is placed in parallel of every switch to limit the impact of the change in the MOSFET parasitic

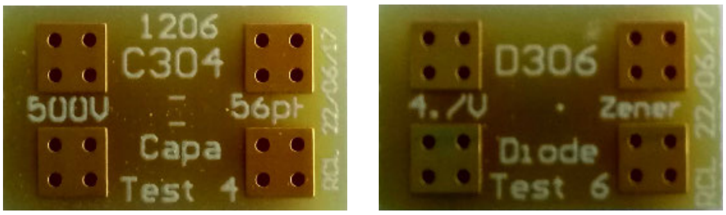


(a)

(b)

(c)

Figure 5.1: (a) Layout of the full bridge using 4 embedded dies used for a PFC cell. (b) Photography of the die test coupon. (c) Layout of the die test coupon.



(a) (b)

Figure 5.2: Test coupon with an embedded (b) 56 pF 500 V capacitor (b) 4.7 V Zener diode.

capacitance due to the voltage (This is to ensure soft switching [57]). The third capacitor is a X8R capacitor with a value of 3.3 µF for a nominal voltage of 25 V. This capacitor reference is used in the driver circuit. 3 samples of each design were built.

There are 3 different diode coupons. The first diode is a 600 V diode used for the bootstrap supply of the upper stage of the gate driver. The second coupon design contains a 15 V Zener diode to ensure positive gate voltage. The negative gate voltage is ensured by a 4.7 V Zener diode which is embedded in the third coupon types. 4 samples of each design were built.

5.3 Preliminary Tests

5.3.1 Die Coupon

The first series of tests on the die coupons is conducted using a Source Measure Unit (SMU) (Keithley 2636). The first experiment is to measure the threshold voltage V_{th}. The two channels of the SMU are connected using a probe station to form the test circuit presented in figure 5.3. The channel A applies a V_{DS} of 5 V while the channel B applies a V_{GS} ramping from -5 V to 15 V with 0.2 V steps. The drain current is measured. According to the MOSFET (CPM2-1200-0080) datasheet, V_{th} is defined by the measured V_{GS} for a drain current comprised between 5 mA and 6 mA. The measured V_{th} for the 8 die coupons are presented in table 5.1a. The minimum V_{th} is 2.1 V and the maximum V_{th} is 2.5 V. The results are in the range given by the datasheet (2 V for the minimum and 4 V for the maximum).

With the same experimental setup, the gate current I_g is measured at V_{GS} equal to 0 V and V_{DS} equal to 2.5 V. Indeed, the oxide of the gate is the weak point of the MOSFETs and could have been damaged by the embedding process. A typical order of magnitude for the gate current at these voltage levels is the pA. The results are

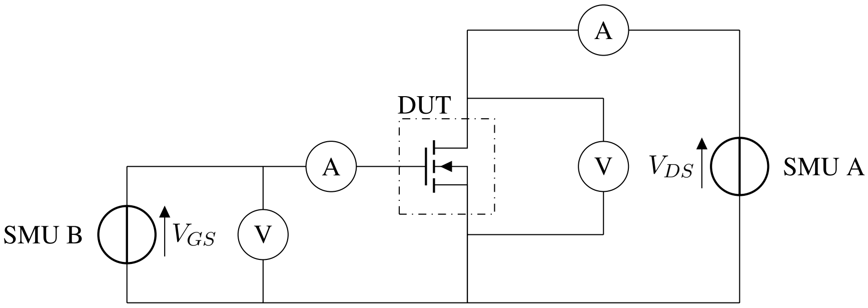


Figure 5.3: Test circuit used to measure the V_{th} and the I_g of the test coupons.

Table 5.1: Experimental results of the functionality tests perform on the die coupons. (a) V_{th} (b) I_g at V_{GS} = 0 V and V_{DS} = 2.5 V

(a)

Coupon CPM2-1200-0080	V_{th} (V)
01 H	2.45 V
01 J	2.3 V
01 L	2.1 V
01 M	2.25 V
02 H	2.3 V
02 J	2.4 V
02 L	2.5 V
02 M	2.1 V

(b)

Coupon CPM2-1200-0080	I_g (A) (V_{GS} = 0 V ; V_{DS} = 2.5 V)
01 H	4.49×10^{-11} A
01 J	5.56×10^{-11} A
01 L	4.98×10^{-11} A
01 M	4.88×10^{-11} A
02 H	4.77×10^{-11} A
02 J	4.58×10^{-11} A
02 L	4.52×10^{-11} A
02 M	5.05×10^{-11} A

given in table 5.1b. The results show no issue with the embedded components. So, after the functionality test, 8/8 coupons are considered as working.

The R$_{DS_{On}}$ of the die coupons (1 embedded die) is measured with a curve tracer (IWATSU CS-5400). The resistance was calculated from the I-V characteristics measured using four-wire sensing method. As it can be seen in the layout from figure 5.1c, the coupons allow for 4-wire sensing all the way up to the copper layer around the dies. The measured R$_{DS_{On}}$ therefore includes the die, the vias and part of the copper layers. An example of the obtained I-V characteristics is given in figure 5.4. For the I-V characteristics, the V_{GS} is increased by 1 V steps from 0 V to 17 V. The maximum V_{DS} is fixed to 10 V. The power is limited to 450 W. The R$_{DS_{On}}$ is calculated using the curve corresponding to V_{GS} equal to 17 V. The results are given in table 5.2. The maximum resistance is 89.1 mΩ. The typical die R$_{DS_{On}}$ is 80 mΩ. Note that this value could not be measured on the dies prior to embedding

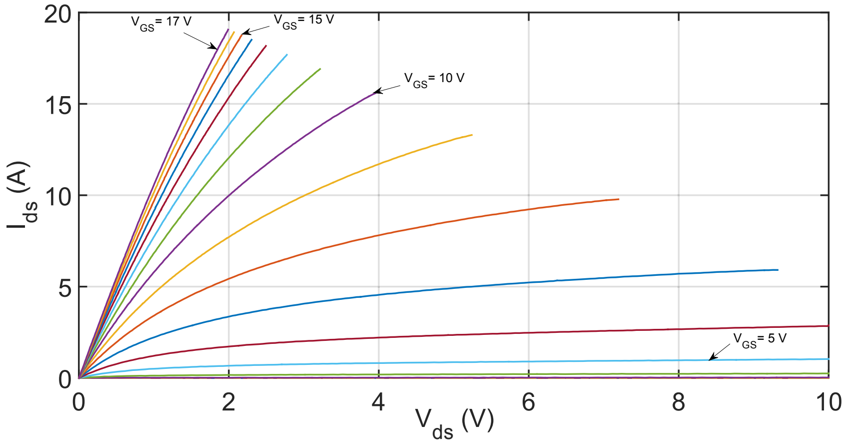


Figure 5.4: I-V characteristic of an embedded SiC MOSFET (CPM2-1200-0080).

Table 5.2: Values of the R$_{DS_{On}}$ of the die coupons measured using a curve tracer (IWATSU CS-5400) and four-wire sensing method.

Coupon CPM2-1200-0080	Coupon ($R_{DS_{On}}$ (A)
01 H	$88.7\,\mathrm{m\Omega}$
01 J	$77.9\,\mathrm{m\Omega}$
01 L	$82.2\,\mathrm{m\Omega}$
01 M	$83.3\,\mathrm{m\Omega}$
02 H	$86.3\,\mathrm{m\Omega}$
02 J	$89.1\,\mathrm{m\Omega}$
02 L	$88.9\,\mathrm{m\Omega}$
02 M	$84.2\,\mathrm{m\Omega}$

due to the high current value required, which is incompatible with probe testing. It can be concluded that the access resistance (vias + copper layers) is small in comparison of the die R$_{DS_{On}}$ but non negligible. A coarse calculation of the access resistance gives a value of $3.1\,\mathrm{m\Omega}$ which is small in comparison of the R$_{DS_{On}}$ die .

The dies breakdown voltage was validated. The maximum I_{DS} at V_{GS} equal to $0\,\mathrm{V}$ and V_{DS} equal to $1200\,\mathrm{V}$ is $1.6\,\mathrm{nA}$ (Figure 5.5). The datasheet gives a typical I_{DS} of $1\,\mathrm{\mu A}$ for the same voltage values. The die test coupons show good characteristics.

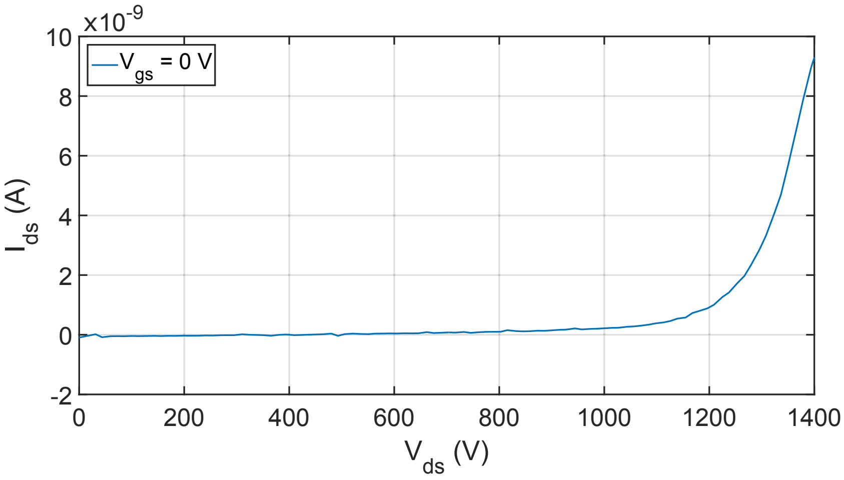


Figure 5.5: Check of the breakdown voltage of an embedded SiC MOSFET (CPM2-1200-0080).

Microvias Position

A picture of a die coupon obtained with X-ray imaging is presented in figure 5.6. The die pads are highlighted for visibility. The dark grey microvias (Drop shape) are on the top of the die (source and gate pads). The light grey microvias are on the bottom of the die (drain pad).

The smallest margin measured (distance between the microvias and the edges of the copper pad) is $32.4\,\mu\mathrm{m}$ on a source pad. The maximum positioning error calculated due to the process was $\pm 100\,\mu\mathrm{m}$. The margin on the GERBER files, corresponding to the smallest margin measured, is $127\,\mu\mathrm{m}$. The maximum positioning error is in accordance with the measured values.

Thermal Resistance

The thermal resistance of a die coupon was measured using a thermal impedance analyzer (Analysis Tech Phase 12B Thermal Analyzer [69]). The experiment is composed of an oven, a water-cooled plate and a high power controller. The DUT is a test coupon with an embedded die.

The first step is to calibrate the component (CPM2-1200-0080) using the oven. The oven temperature is brought to $125\,^{\circ}\mathrm{C}$. The oven is then turned-off and then let cool down slowly to the ambient temperature due to the heat transfer with the environment. The MOSFET threshold voltage is measured under a $20\,\mathrm{mA}$ bias every $5\,^{\circ}\mathrm{C}$ step. With the slow cooling of the oven inside, it is assumed that the component temperature is uniformly at the oven temperature. A curve is obtained, giving a

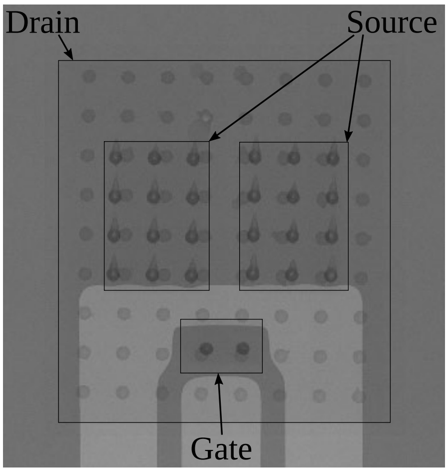


Figure 5.6: Picture of a die coupon obtained by X-ray imaging. The pads edges are highlighted for visibility. Die size is $3.36\,\mathrm{mm}\times 3.1\,\mathrm{mm}$.

relation between the junction temperature and the V_{th} giving a temperature coefficient of $-3.3\,\mathrm{mV}/°\mathrm{C}$. It is presented in figure 5.7.

The component is then placed on the cold plate. A thermal interface material is used to ensure a proper heat transfer between the component and the cooler. Then, some power is dissipated into the coupon using the MOSFET ($2.7\,\mathrm{W}$). This power was chosen due to the small size of the test coupon. The threshold voltage is measured to obtain the junction temperature with the calibration curve. The temperature of the cold plate is measured with an integrated thermocouple. The software calculates the thermal resistances and capacitances as a structure function [69].

The experiment is done with two different TIMs (Water and Thermal Paste). The thermal capacitance as a function of the thermal resistance curves are plotted for both experiments. These curves differ only because of the TIMs used. It is considered that the test coupon actual thermal resistance corresponds to the value when the curves diverge. The curves for both TIMs are presented in figure 5.8. The measured thermal resistance for the die coupon is approximately $12\,°\mathrm{C}/\mathrm{W}$. Note, that because both curves diverge very little, this measurement is rather imprecise.

5.3.2 Full Bridge

Each die of the full bridge board was tested with the same configuration as the test coupons (Probe station + SMU). This corresponds to 36 dies. The minimum V_{th} is $2.1\,\mathrm{V}$ and the maximum V_{th} is $2.85\,\mathrm{V}$. The V_{th} distribution for the PFC full bridge dies is given in figure 5.9. However, the die numbered "02 G LF L" has a gate current of $204\,\mathrm{nA}$ at V_{GS} of $0\,\mathrm{V}$ and V_{DS} of $2.5\,\mathrm{V}$. The datasheet gives a maximum

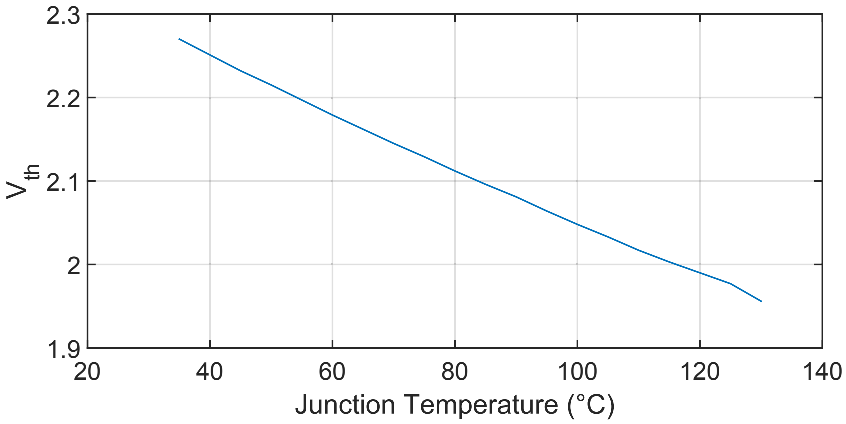


Figure 5.7: V_{th} as a function of the junction temperature for the MOSFET (CPM2-1200-0080).

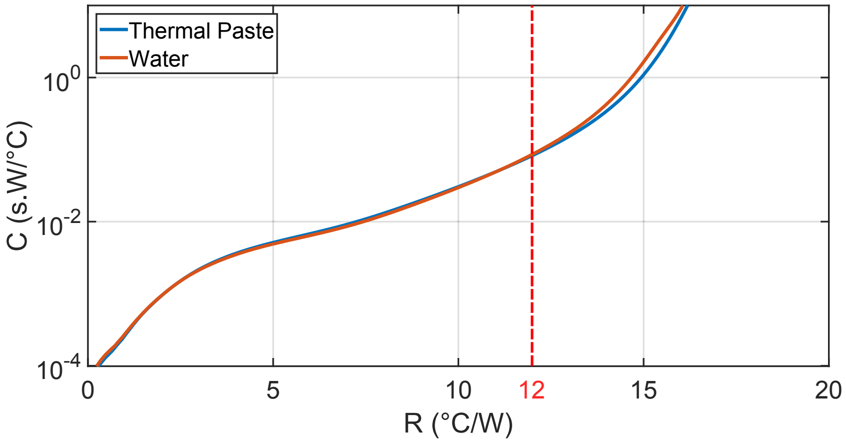


Figure 5.8: Structure function (Thermal capacitance as a function of thermal resistance) of the die coupons for two different thermal interface materials.

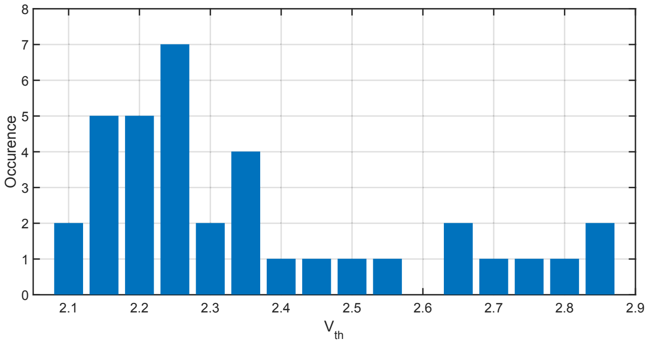


Figure 5.9: V_{th} distribution for the PFC full bridge dies.

gate current of $250\,\mathrm{nA}$ at V_{GS} of $0\,\mathrm{V}$ and V_{DS} of $20\,\mathrm{V}$. This is an abnormally high leakage current compared to the tens of pA for the other dies. The origin of the degradation is not known. Some dies were randomly tested before embedding and showed no such issue. Because of the deteriorated die, 8/9 embedded full bridge boards are considered as working.

5.3.3 Capacitor Coupon

The larger capacitors ($330\,\mathrm{nF}$ and $3.3\,\mathrm{\mu F}$) were tested with a capacitance meter. The value of the $56\,\mathrm{pF}$ capacitor is too low for reliable measurements. The measurements were found to be in accordance to the nominal value.

In addition, the leakage current of the capacitors was measured for both $500\,\mathrm{V}$ capacitor references as it is expected to be a good indication of the condition of the capacitor. Ceramic capacitors are brittle and may have cracked during the embedding process. Such cracks should increase the leakage current of the capacitors or reduce its breakdown voltage. The voltage was applied by a SMU (Keithley 2410). The leakage current was measured after an arbitrary waiting time of $15\,\mathrm{min}$, and compared to a surface-mounted component. The results are presented in table 5.3. The leakage currents have the same order of magnitude for embedded and surface-mounted capacitor. The embedded capacitors have the good specifications. The embedding process did not deteriorate their characteristics.

5.3.4 Diode Coupon

The diode coupons were tested with a curve tracer (IWATSU CS-5400). The current-voltage (I-V) characteristics is observed. The results are presented in figure 5.10.

The datasheet of the $600\,\mathrm{V}$ diodes indicates a maximum leakage current of $3\,\mathrm{\mu A}$ at the rated voltage and a typical forward voltage of $1\,\mathrm{V}$ for a current of $1\,\mathrm{A}$. It can

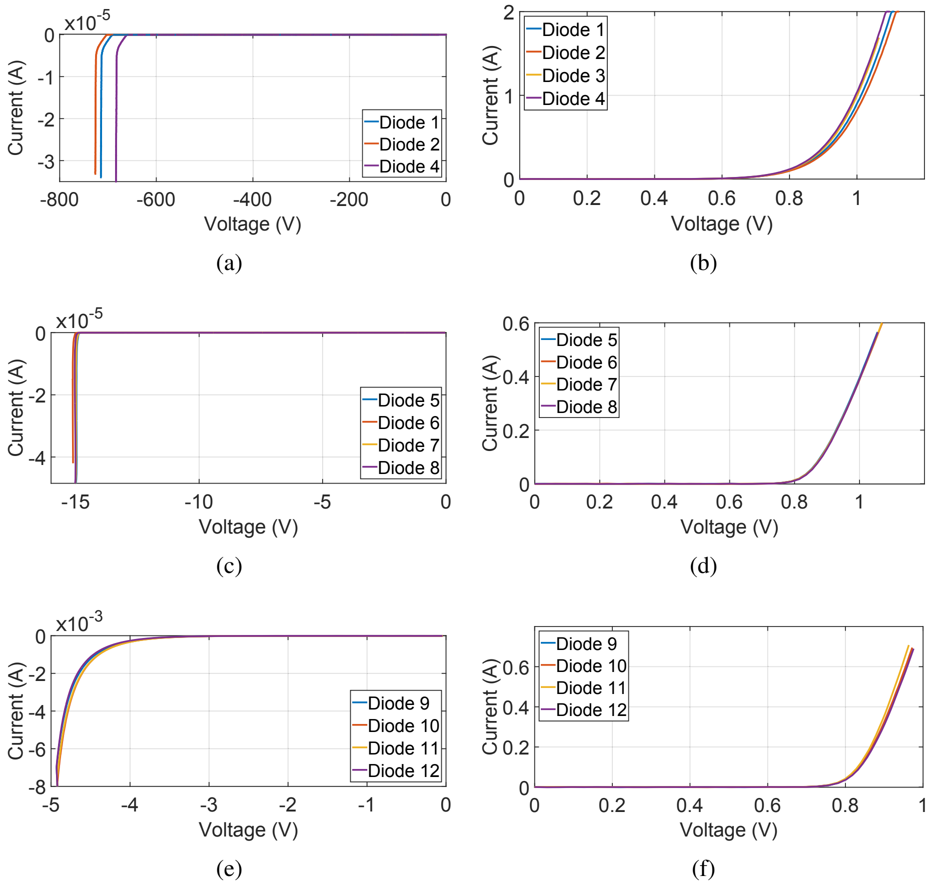
Table 5.3: Measured leakage current for (a) 500 V 330 nF capacitor. (b) 500 V 56 pF capacitor.

(a)

500 V 330 nF Capacitor				
Current (nA) / Voltage (V)	Embedded Capacitor			Pristine Capacitor
	n° 1	n° 2	n° 3	
250	10.44	12.24	30.8	24.86
500	83.01	95.76	105.97	107.46
750	415.00	415.57	407.44	433.16
1000	1710.30	1565.00	1485.30	1628.50

(b)

500 V 56 pF Capacitor				
Current (nA) / Voltage (V)	Embedded Capacitor			Pristine Capacitor
	n° 1	n° 2	n° 3	
250	1.07	0.34	0.35	0.47
500	2.64	0.81	0.86	1.02
750	4.76	1.32	1.3	1.63
1000	5.63	1.9	1.92	2.19



(a) (b) (c) (d) (e) (f)

Figure 5.10: I-V characteristic of the 600 V bootstrap diodes (a) Reverse (b) Forward / 15 V Zener diodes (c) Reverse (d) Forward / 4.7 V Zener diodes (e) Reverse (f) Forward. / 4 samples for each measurement.

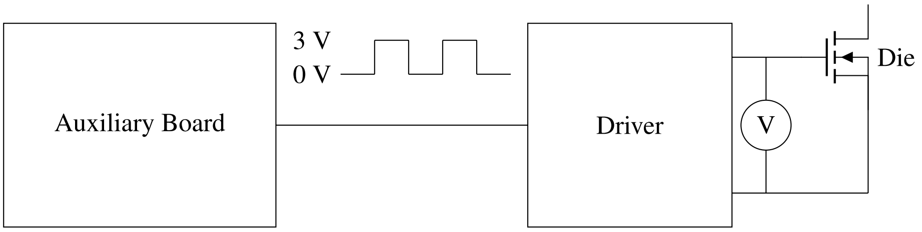


Figure 5.11: Test circuit used to measure the V_{gs} to validate the driver circuit.

be seen in figure 5.10a and 5.10b respectively that these two values are respected. However, a diode (numbered 3) failed during the forward test. So it was not possible to perform the reverse test on this component. The cause of this failure is not known.

The datasheet of the $15\,\mathrm{V}$ Zener diode gives a reverse Zener voltage between $14.25\,\mathrm{V}$ and $15.75\,\mathrm{V}$. The curves show that the Zener voltage V_z is in the range given by the datasheet. The maximum forward voltage is $0.9\,\mathrm{V}$ for a current of $10\,\mathrm{mA}$ according to the datasheet. The maximum forward voltage is respected for all coupons.

The datasheet of the $4.7\,\mathrm{V}$ Zener diode gives a reverse Zener voltage between $4.4\,\mathrm{V}$ and $5\,\mathrm{V}$ for a current of $5\,\mathrm{mA}$. The curves show that the Zener voltage V_z is in the range given by the datasheet. The maximum forward voltage is the same as for the $15\,\mathrm{V}$ Zener diode. The maximum forward voltage is respected for all coupons.

The embedded diodes have the good specifications. The embedding process did not deteriorate their characteristics.

5.3.5 Driver Circuit

The driver boards are tested by connecting them to a DSP demo board (F28379D Delfino Experimenter Kit) using an adapter board which also provides power to gate drivers (Figure 5.12). The control code was developed by J. Le Leslé. A square signal between $0\,\mathrm{V}$ and $3\,\mathrm{V}$ with a variable duty cycle is supplied to the inputs of the drivers. The V_{GS} of the high or low-side dies was observed. The diagram circuit used for the test is presented in figure 5.11. An example of measured waveforms is given in figure 5.13. No issues were found with this test, all driver boards behaved satisfyingly. So, there are 7 PCBs with embedded driver circuit available to assemble the converter. However, the tests were performed without high voltage on the top switch.

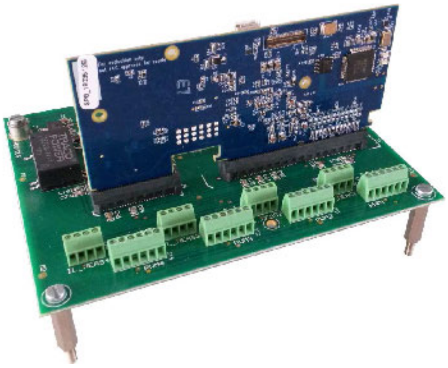


Figure 5.12: Auxiliary power supplies and break-out board for the DSP controller (the vertical daughter board).

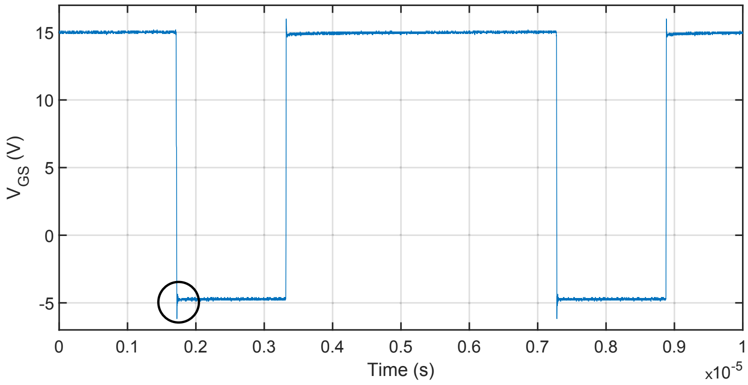


Figure 5.13: Measured V_{GS} on one of the outputs of an embedded driver circuit (HF signal). The zoom is presented in figure 5.14.

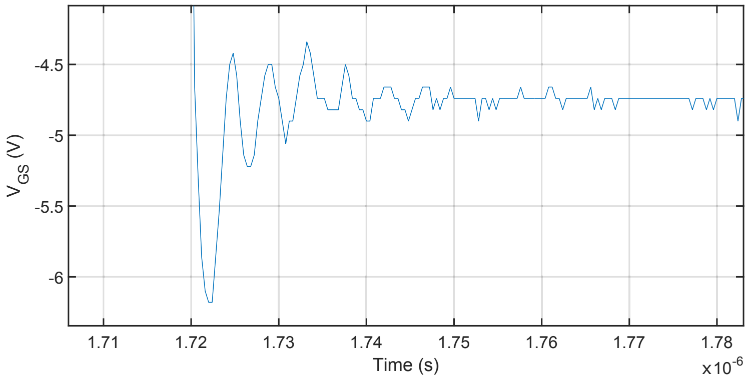


Figure 5.14: Zoom on the measured V_{GS} on one of the outputs of an embedded driver circuit (HF signal).

5.3.6 Inductor

The PFC inductors are tested with an impedance analyzer (Keysight E4294A) with a 42941A probe after probe compensation. Resistance and inductance of the inductors as a function of the frequency, are presented in figures 5.15a and 5.15b respectively for the 6 samples which were built.

The required PFC inductance value is $34.7\,\mu\mathrm{H}$. It can be observed that this value is not achieved for all inductors. The inductance values are decreasing from $10\,\mathrm{kHz}$ to $1\,\mathrm{MHz}$. Except for the inductors numbered "57.6" and "59" which have almost a constant value. Also, the resistance shows a strong increase as a function of the frequency. The resistance at $180\,\mathrm{kHz}$ is approximately $10\,\Omega$ (+/- $2\,\Omega$ depending on the sample). This AC resistance is way higher that the value calculated ($332\,\mathrm{m}\Omega$).

Several additional investigations are presented in section 5.5 to understand the inductance decrease and the resistance strong increase.

5.3.7 EMI Filter

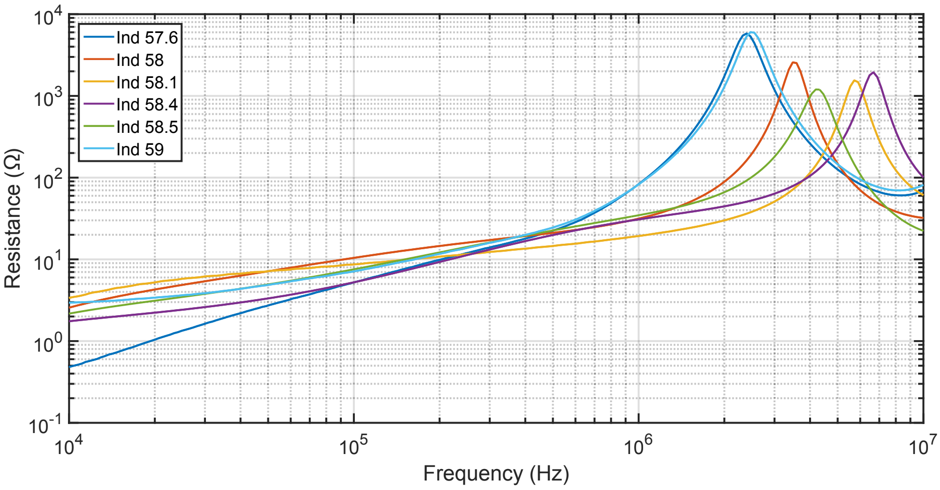
With the same method as for PFC inductors, the DM EMI filter inductors were electrically characterized. Resistance and inductance as a function of the frequency are presented in figures 5.16a and 5.16b respectively.

The required DM inductance value is $7.96\,\mu\mathrm{H}$. As for PFC inductors, the value is not achieved for all inductors. The inductors do not have a constant value with the frequency. In addition, figure 5.16a shows a strong increase of the resistance with the frequency. The resistance at $180\,\mathrm{kHz}$ is comprised between $720\,\mathrm{m}\Omega$ and $5.74\,\Omega$ for all samples. This is way higher that the calculated value ($83.3\,\mathrm{m}\Omega$). This is also addressed in section 5.5.

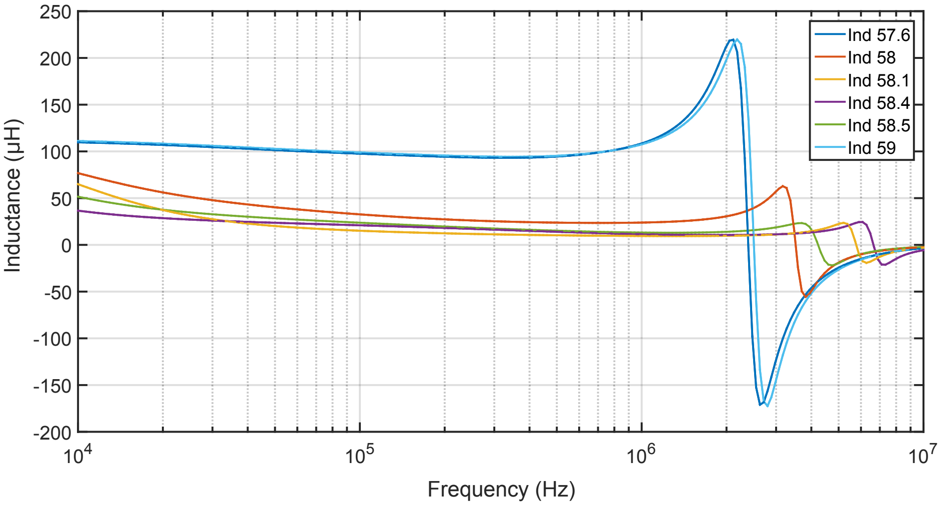
5.3.8 Assembly of a PFC Cell

A PFC was assembled to check the PCBs interconnection. A PFC cell is composed of a heatsink, a PCB with embedded dies, a PCB with embedded driver circuits and a PCB with an embedded inductor. These elements are separated by a TIM to improve the heat path to the heatsink. This TIM was chosen thanks to its good thermal conductivity ($1.8\,\mathrm{W}/(\mathrm{m}\cdot\mathrm{K})$) for this type of material and its low thickness ($203\,\mu\mathrm{m}$). The TIMs are cut with an automatic cutting machine "Silhouette Cameo 1" (Figure 5.17). The assembly work flow is presented in figure 5.18 and below:

(a) A Heatsink (7x7x2.5 cm^3) is used. The heatsink is machined with slots to prevent short circuits around the board-to-board interconnection, and tapped holes to secure the PCBs.

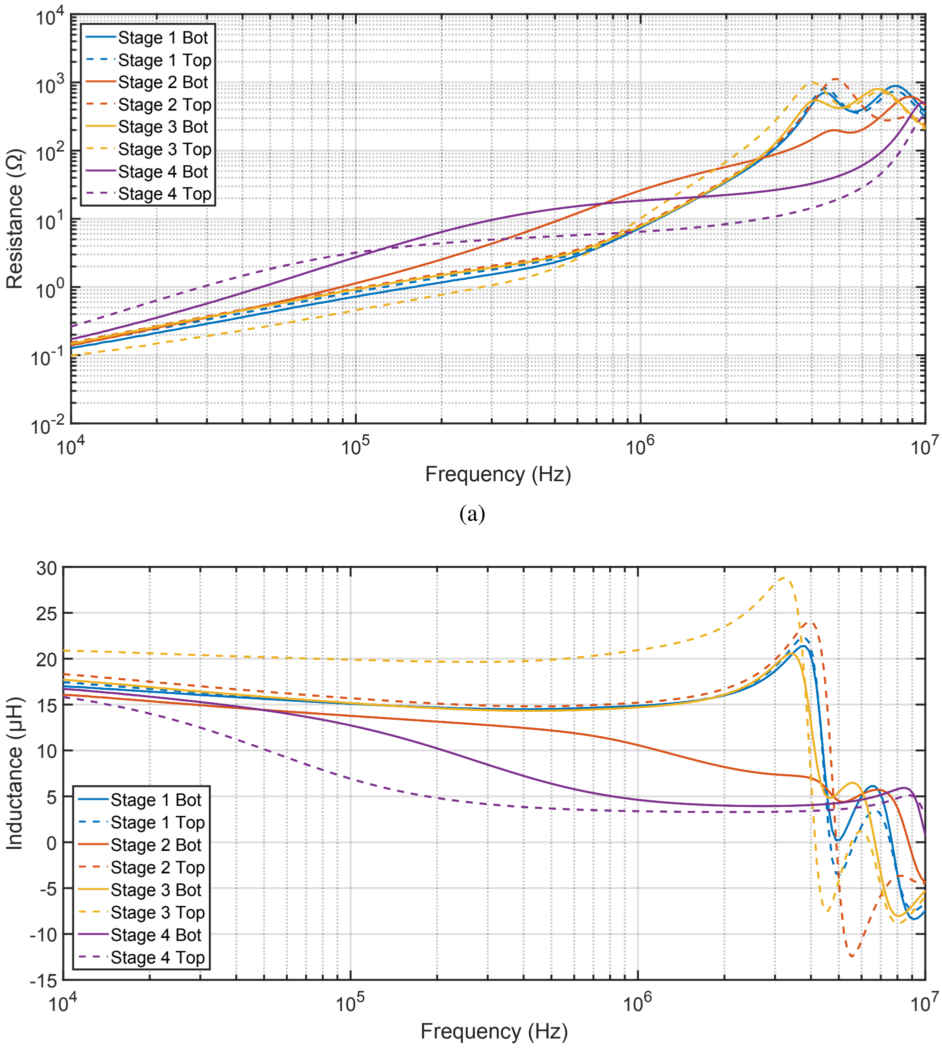


(a)



(b)

Figure 5.15: Electrical characterizations of the PFC inductors (a) Resistance (b) Inductance.



(a)

(b)

Figure 5.16: Electrical characterizations of the DM EMI filter inductors (a) Resistance (b) Inductance.

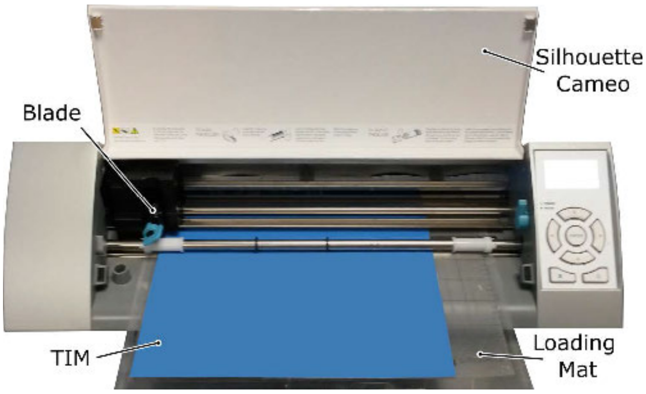


Figure 5.17: Automatic cutting machine used for the TIM (Silhouette Cameo 1).

(b) A TIM layer is placed between the heatsink and the die PCB ($680\,\mu\mathrm{m}$-thick).

(c) The die PCB is placed on the TIM (with soldered wires-not shown-to interconnect the driver circuits, the decoupling capacitors and the inductor).

(d) A second TIM layer is placed between the die PCB and the driver PCB. The wires have to be guided through the holes and soldered.

(e) The PCB driver ($4.5\,\mathrm{mm}$-thick) is then positioned. The driver circuit and the decoupling capacitors are connected to the die PCB by soldering wire in the corresponding through-hole vias.

(f) A third TIM layer is placed between the driver PCB and the inductor PCB.

(g) The inductor PCB ($4.5\,\mathrm{mm}$-thick) is positioned. The inductor is then connected.

The last step is to screw the PCBs to the heatsink. An exploded view of a PFC cell is presented in figure 5.19.

The diagram circuit to test a PFC cell is presented in figure 5.20. The cell is connected to an external DC source ($30\,\mathrm{V}$, maximum of the source). The load is a resistor on the AC side ($3.3\,\Omega$). The load current is measured with a current probe (Tektronix TCP0030) and an oscilloscope (Tektronix DPO 40348). Control signals are generated with the auxiliary board (Figure 5.12). An example of a measured current is given in figure 5.21 and figure 5.22.

The fundamental frequency of the current waveform measured is $49.92\,\mathrm{Hz}$, which is very close to the $50\,\mathrm{Hz}$ required. If the PFC was connected to the mains, this fundamental frequency would be synchronized with it, to ensure it has the same frequency. While the measured current high frequency is $180\,\mathrm{kHz}$, which is the required value. The PFC cells are considered as working.

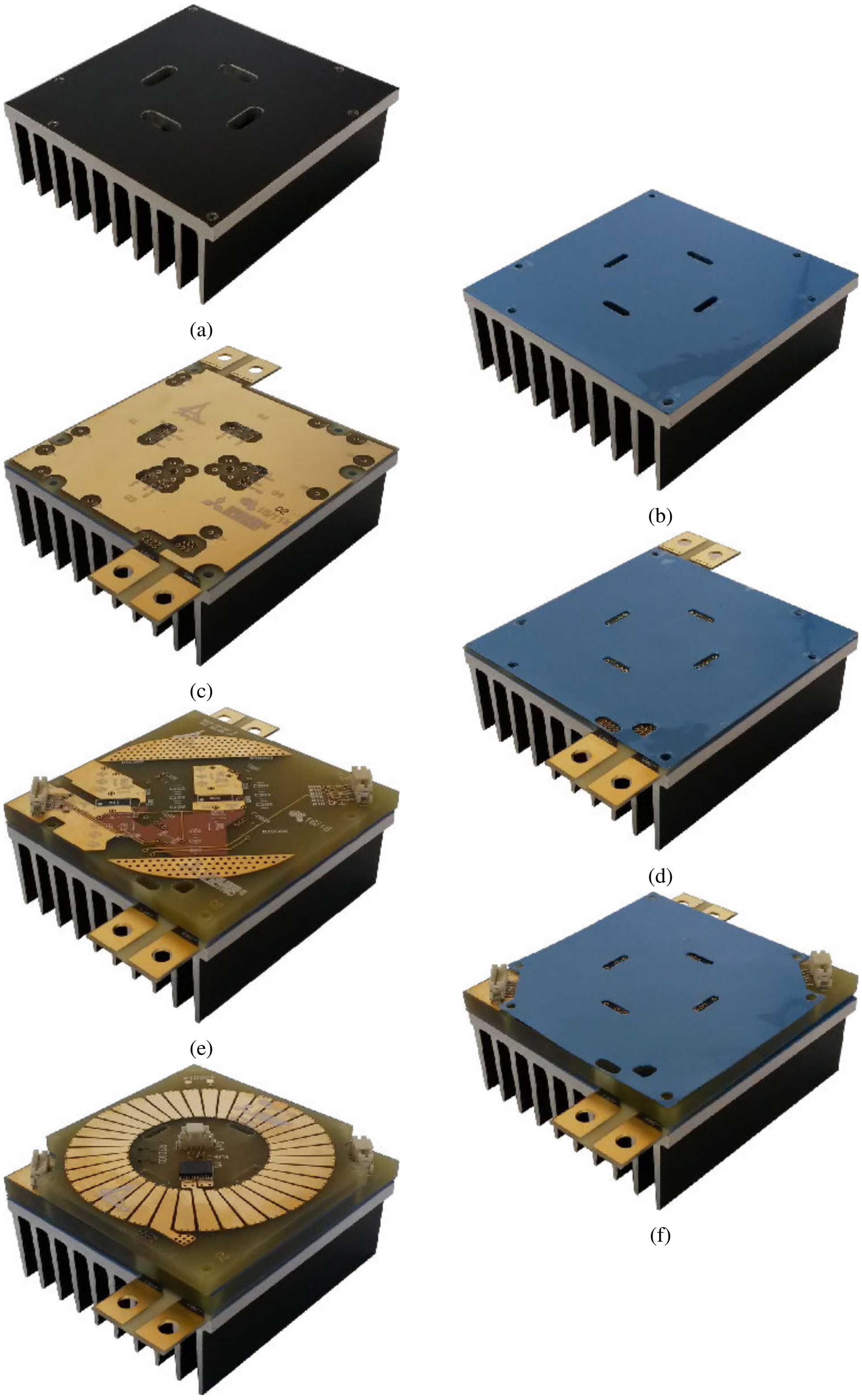

(a) (b) (c) (d) (e) (f) (g)

Figure 5.18: PFC cell assembly work flow.

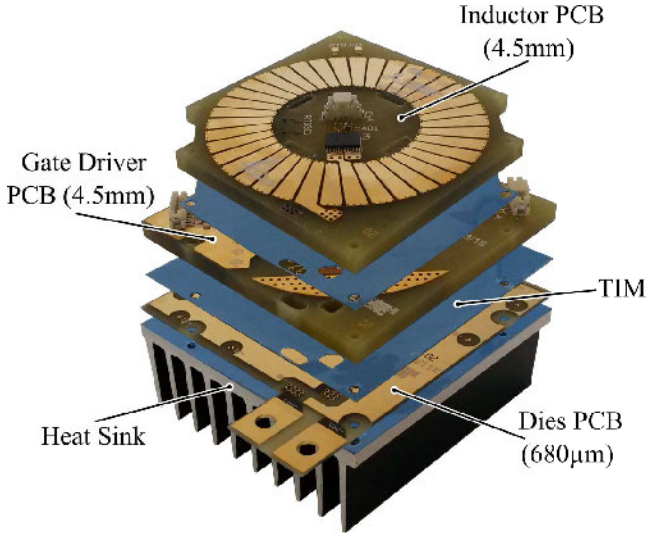


Figure 5.19: Exploded view of a PFC cell.

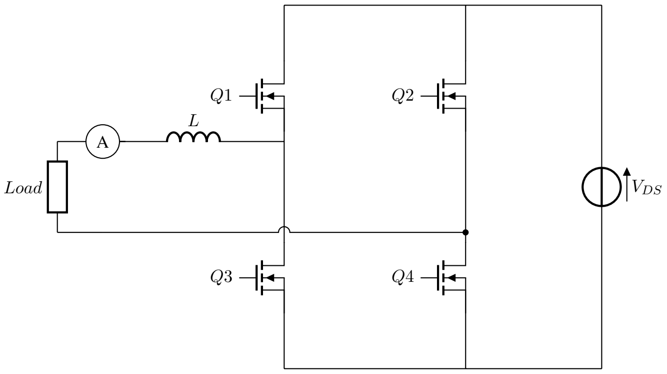


Figure 5.20: Circuit diagram of the experiment to check the functionality of a PFC cell.

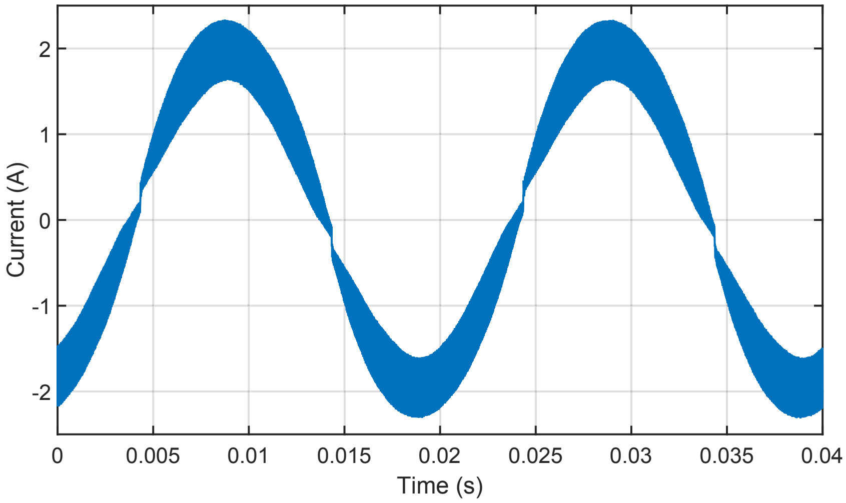


Figure 5.21: Current in the load at 50 Hz.

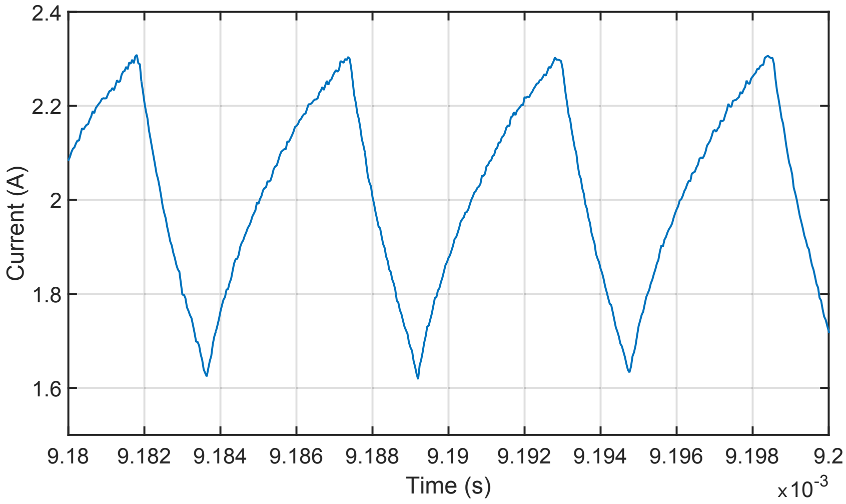


Figure 5.22: Zoom on the ripple at 180 kHz.

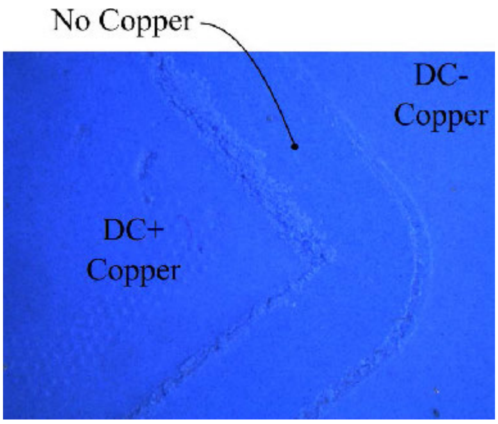


Figure 5.23: Photograph of the TIM with the copper mark of the $DC+$ and the $DC-$ nets. The TIM is $30\,\mu\mathrm{m}$-thicker where there is no copper (Measurement performed using a Dektak ISO Stylus profilometer).

Parastic Capacitance

The parasitic capacitance between the net $DC-$ and the ground is measured using an impedance analyzer. The parasitic capacitance has a value of $816\,\mathrm{pF}$ at $500\,\mathrm{kHz}$ compared to $561\,\mathrm{pF}$ for the simulated value. Two hypotheses can explain this discrepancy between simulation and measurement: first, as the experiment is performed on a populated board (with 4 dies), all potentials are coupled together through the capacitances of the MOSFETs, which are not negligible at $0\,\mathrm{V}$ bias. Therefore, one can consider that the measurement corresponds to the sum of all parasitic capacitors to ground ($561\,\mathrm{pF} + 66\,\mathrm{pF} + 13\,\mathrm{pF} + 4\,\mathrm{pF} = 644\,\mathrm{pF}$).

Secondly, the thickness of the TIM layer located between the die PCB and the heatsink obviously has a tremendous influence of the capacitance. In the simulation, it was assumed that the thickness of the TIM was $203\,\mu\mathrm{m}$. Upon observation, using a microscope, it is found to be $230\,\mu\mathrm{m}$ thick on the prototype. This should result in a lower capacitance value. However, this measurement is taken between the dielectric material of the PCB and the heatsink. As the copper layer of the PCB is $70\,\mu\mathrm{m}$ thick, it means the actual thickness of the TIM might actually be thinner than $203\,\mu\mathrm{m}$ (Actually $160\,\mu\mathrm{m}$), which would be enough to make-up for the difference in capacitance between simulation and experiment. It is difficult to measure the actual TIM thickness (The PCB probably also bends a little), but after disassembling of the cell, a clear, $30\,\mu\mathrm{m}$-deep imprint remains in the TIM (Figure 5.23). Overall, the $30\,\%$ error between measurement and simulation is found to be acceptable given our poor control over the TIM thickness.

Figure 5.24: Photograph of the PFC with a capacitor bank. The capacitor bank should eventually be replaced by an electronic capacitor to reduce the box volume.

5.3.9 Full PFC Converter

The 4 cells of the PFC were assembled to measure the effect of interleaving on the AC current. A photograph of the assembled PFC with a capacitor bank is shown in figure 5.24. This full converter was tested in a similar way as the individual cells (Figure 5.20), with a low power supply connected to the DC side, and a load ($3.3\,\Omega$) on the AC side.

The current in each cell is presented in figure 5.25. As it was expected from the differences in inductor values previously presented, the currents do not have the same amplitude. Consequently, the line current has a higher ripple that expected due to the poor interleaving of the 4 currents (Figure 5.26). The ripple already has an amplitude of $0.37\,\mathrm{A}$ despite a really low voltage being applied ($30\,\mathrm{V}$). The interleaved current should have a frequency of $720\,\mathrm{kHz}$ ($4 \times 180\,\mathrm{kHz}$). This is not the case due to the poor interleaving. This can be seen in the zoom presented in figure 5.27. On the same figure, it can be noted that the shift of a quarter of the $180\,\mathrm{kHz}$ period ($1.39\,\mu\mathrm{s}$) between each cell current is obtained.

The poor interleaving will not allow to respect the E.M.C. standard on the AC side with the EMI filter designed. In addition, inductors losses will be higher than the expected ones resulting in higher temperatures. However, the current shifting between each cell in due to the control is correct. Only the PFC inductors have to be changed to obtain a fully working converter.

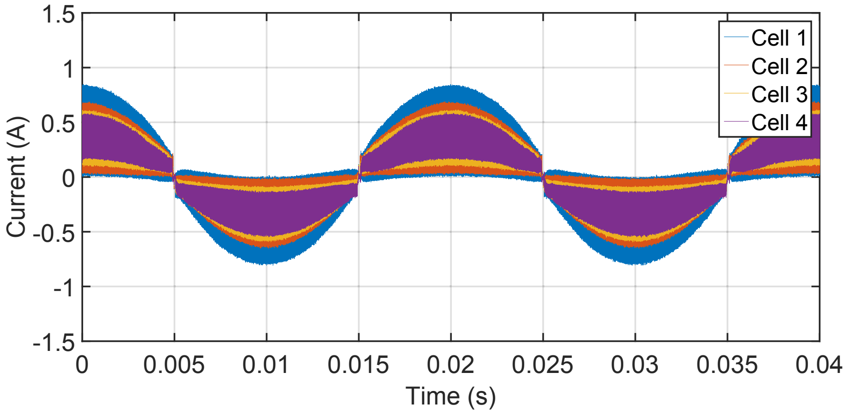


Figure 5.25: Measured current in each cell of the PFC.

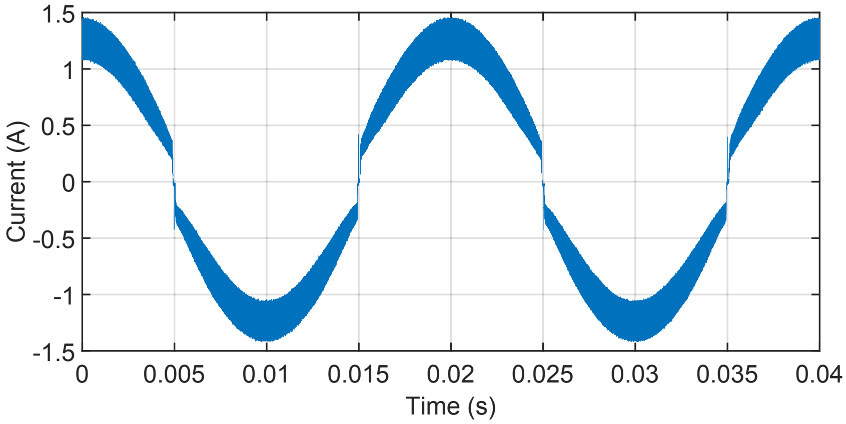


Figure 5.26: Measured interleaved current of the 4 cells.

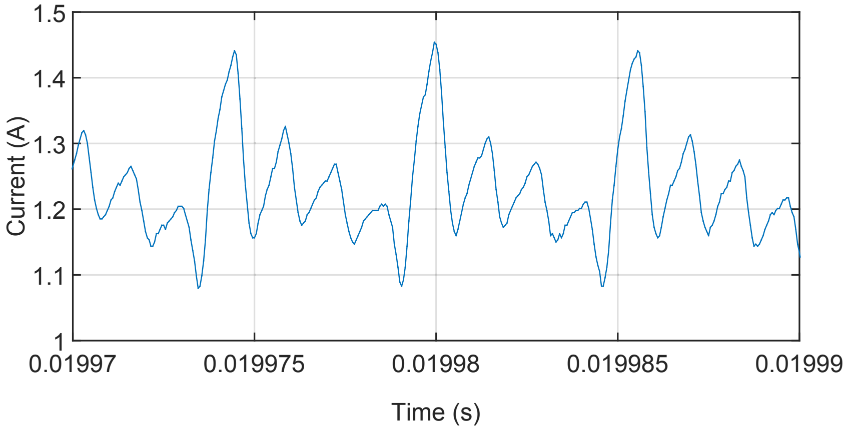


Figure 5.27: Zoom on the interleaved current of the 4 cells.

The EMI filter was not tested due to the results with the impedance analyzer. In addition, the converter could not be operated at nominal power due to the high PFC inductors resistance at $180\,\mathrm{kHz}$. For the tests performed at nominal power (Chapter 6/Figure 6.2), "Planar" inductors are designed and built.

5.4 Thermal Test

5.4.1 Test Setup

The objective of the thermal tests presented here is to validate the thermal models (chapter 4) and ensure that all parts of the converter operate within an acceptable temperature range. The previous thermal simulation considered 3 different heating elements: low frequency dies, high frequency dies and PFC inductor.

The losses generated by each element (calculated with the converter optimization script) are presented in table 5.4. The tests presented here aim at dissipating a representative power level in each element of the PFC cell, measuring the corresponding temperature rise and finally comparing it with FEM predictions.

For the thermal test, a PFC cell is assembled with the TIM but the 3 PCBs are not interconnected. Wires are soldered on the PCB to have access to the drain, the source and the gate of each die. As can be seen in figure 5.28, the gate and the drain of each transistor are shorted together. A current source is connected between the source and the drain to apply power. With this setup, 4 current sources are needed (one Keithley SMU 2636 and one 2602 which have two channels each). This configuration allows to control the power dissipated in each transistor, and to achieve a relatively high power dissipation with a moderate current level (1-2 A).

Inducing a realistic inductor heating is more difficult because power dissipation and distribution are dependent on the complex current waveform applied on the AC side of the PFC. Therefore a different approach was chosen: the first step is to measure the power dissipated by the inductor. Calorimetry is a simple and accurate way to measure losses compared to electrical technique which are inaccurate. For that, the

Table 5.4: Losses in each power element of a PFC cell for the converter at nominal power (Calculated with the converter optimization script).

Name	Losses (W)
High Frequency Die (Per die, 2 dies per cell)	$5.83\,\mathrm{W}$
Low Frequency Die (Per die, 2 dies per cell)	$0.81\,\mathrm{W}$
Inductor (One inductor per cell)	$8.25\,\mathrm{W}$

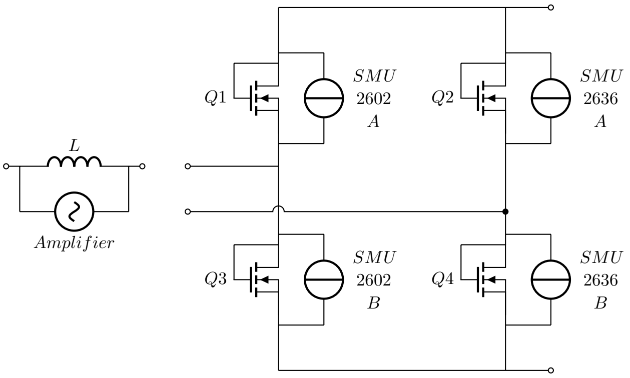


Figure 5.28: Circuit diagram of the thermal experiment.

inductor is placed in a calorimeter (described below) and supplied (using an amplifier) with a 70 kHz sinewave. This frequency was chosen to obtain the highest power dissipation possible taking into account the limitations of the amplifier. The inductor losses are measured with the help of the calorimeter and the amplitude of the signal generated by the amplifier is adjusted to achieve the desired power level. Then, the inductor is placed in the PFC cell assembly. The same signal is applied to generate heat. Note that this method does not ensure that the heat distribution between the core and the winding is the same as in the operating PFC. However, it is assumed that this has little impact on the thermal management. With this method, the measurement of the heating power is relatively accurate. Also, the distribution of losses is nearly identical to those under PFC operations condition at nominal power. This method also does not take into account the change of losses due to the temperature dependent parameters.

The cooling is done through the heatsink in natural convection. The PFC cell is raised above the working surface to have a proper airflow in the heatsink placed on the bottom. The PCBs external surfaces also participate to the cooling with natural convection. The ambient temperature is 30 °C.

5.4.2 Definition of power losses in the inductor

This section provides more details regarding the calorimetric measurement introduced above. The objective of the calorimeter is to measure the inductor losses in a way which is more simple and accurate than performing electric measurement.

The calorimeter setup is presented in figure 5.29 with a diagram in figure 5.30. The system is composed of an enclosure which ideally should be adiabatic (a Dewar jar). In the enclosure are placed a calibration resistor, the DUT and a temperature probe. All these elements are submerged into a dielectric liquid (Novec 7500). This

Figure 5.29: Photograph of the calorimeter setup. The DUT size was $7{\times}7{\times}0.45\,\mathrm{cm}^3$. The DUT can have a thickness up to $1\,\mathrm{cm}$. DUT with a cubic shape are limited to $4{\times}4{\times}4\,\mathrm{cm}^3$.

fluid was chosen because of its relatively low toxicity, its high boiling point ($128\,^{\circ}\mathrm{C}$), its chemical and electrical compatibility with power electronics, and because it does not leave any residue on the DUTs after drying. A propeller connected to a motor placed outside of the enclosure is used to stir the liquid to ensure a homogenous temperature distribution. The temperature of the bath is measured with a PT100 connected to a multimeter (Keithley 2700) interfaced with a MATLAB script. The principle of this measurement setup is first to calibrate the total heat capacity (the liquid bath and all the elements it contains) using the calibration resistor, as described below. The DUT is then operated for a fixed amount of time, and the corresponding temperature increase of the bath is measured. A typical curve of temperature as a function of time is presented in figure 5.31. Because the jar is not perfectly adiabatic, some heat exchange takes place between the bath and the environment, resulting in slow change in temperature of the bath even when the DUT is off. The temperature difference is therefore calculated using the asymptotes of the curve before and after the heating phase.

The experimental work begins with the calibration of the system. The bath is heated with the help of a calibration resistor. The resistor current and voltage are

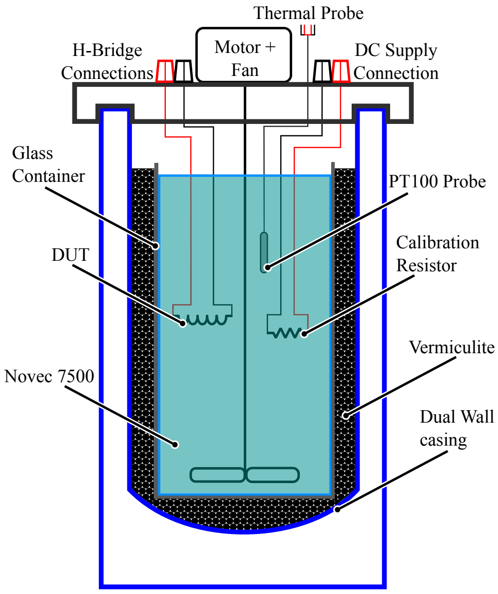


Figure 5.30: Diagram of the calorimeter setup.

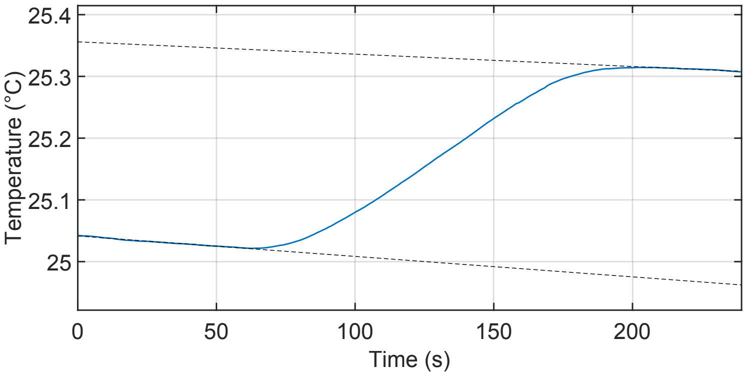


Figure 5.31: Example of temperature measurement obtained.

measured accurately (they are DC signals), yielding the dissipated power. The heating time is measured with a chronometer. The sum of the mass and the specific heat of each element in the calorimeter is defined by equation (5.1).

$$\sum(m_i \cdot C_i) = \frac{\Delta T}{P \cdot t} \tag{5.1}$$

where P is the (measured) losses, m_i is the mass of the i-th element in the calorimeter, C_i is the specific heat of the i-th element in the calorimeter, ΔT is the temperature difference of the bath before and after heating and t is the heating time.

Once this value is calculated, the system can be used to measure losses into the DUT. As for the calibration, the DUT is allowed to dissipate power for a set amount of time and the temperature of the bath is monitored. Equation (5.2) is used to calculate the losses.

$$P = \sum(m_i \cdot C_i) \cdot \frac{\Delta T}{t} \tag{5.2}$$

The calorimetric measurement error is calculated below. The voltmeter (Keysight U1242B) accuracy is giving an error of $0.11\,\%$. The ammeter (Keysight U1242A) error is $0.65\,\%$. The thermal probe (PT100) relative error is $\pm 0.2\,\%$. The heating time measurement is not automatized, which has a strong impact on the error. With an hypothesis of $60\,\mathrm{s}$ for the heating time and a delay of $\pm 1\,\mathrm{s}$, the error is $1.67\,\%$. The error is given by equation (5.3).

$$\epsilon_{Meas} = \epsilon_{Calib} + \epsilon_{DUT} = \frac{\Delta U}{U} + \frac{\Delta I}{I} + 2 \cdot \frac{\Delta T}{T} + 2 \cdot \frac{\Delta t}{t} = 4.49\,\% \tag{5.3}$$

The power dissipated in the tests ranges between $2\,\mathrm{W}$ and $10\,\mathrm{W}$. The test is taking approximately $10\,\mathrm{min}$ for the calibration and the power dissipation measurement. The calorimetry has a better accuracy than the electrical measurement which has an error of $5.5\,\%$ only considering the error of the voltage and current probes (but neglecting timing or quantification errors).

5.4.3 Results

The losses generated in each element are presented in table 5.5. These values are lower than the calculated ones (Table 5.4) due to the amplifier and the SMU limitation.

The temperatures inside a PFC cell are measured with 6 RTDs (Resistive Temperature Device, PT1000 in this case). 4 RTDs are placed in the driver PCB directly above the dies. The 2 others RTDs are placed in the inductor PCB. The first one is placed in the center while the second is placed at the exterior. The temperature obtained are presented in table 5.6. The ambient temperature is measured at $30\,^{\circ}\mathrm{C}$.

Table 5.5: Losses generated in each power element of a PFC cell for the thermal tests.

Name	Losses (W)
1 High Frequency Die	4 W
1 Low Frequency Die	0.81 W
1 Inductor	2 W

Table 5.6: Temperature measured with the help of embedded RTDs.

Name	Temperature
RTD Die HF Low	66.8 °C
RTD Die HF High	65.3 °C
RTD Die LF Low	63.5 °C
RTD Die LF High	63.8 °C
RTD Outer Ind	57.3 °C
RTD Inner Ind	60.2 °C

It can be noted that both LF dies temperature are close. The LF dies temperatures are high compared to the power they dissipate. It is mostly due to the positioning of the RTD in the driver PCB directly above the dies. The heat mostly comes from the inductor PCB. There is difference of 1.5 °C between the HF dies. The die with the higher temperature is mounted flip-chip. The pad area in the heatsink direction is smaller (Gate + Source) than the pad area of the other die (Drain). The number of microvias is also reduced due to the pad size. Both reasons explain the temperature difference.

A new simulation is run with the power listed in table 5.5. The models are the same as presented in the chapter 4. The simulation has an ambient temperature of 60 °C to use the heatsink model obtained by CFD simulation. The temperatures were taken for the components and at the RTD locations. The results are presented in table 5.7.

The comparison of the temperature difference between the RTDs and the ambient is given in table 5.8 for the simulated and measured results.

The difference between the ambient temperature and the temperatures of the RTDs above the dies (LF and HF) in the experiment are comprised between that of the two models (Approximated Geometry and Imported Geometry). The model using a unique block to represent a layer (Approximated Geometry) is optimistic. The model using the imported geometry is pessimistic due to the elements removed to reduce the computation time. Both models have an error of approximately 1 °C, which can

Table 5.7: Temperature obtained by finite element simulation. The power losses of each element were adapted to correspond to the experiment.

Name	Approximated Geometry	Imported Geometry
Die HF	103.6 °C	103 °C
Die LF	95.1 °C	95 °C
RTD Die HF	95.2 °C	97.1 °C
RTD Die LF	93.6 °C	94.1 °C
RTD Outer Ind	92.2 °C	90.9 °C
RTD Inner Ind	92.8 °C	91.2 °C
Magnetic Material	95 °C	95.2 °C

Table 5.8: Comparison of the temperature difference between the RTDs and the ambient obtained by experiment and simulation.

Name	Experiment	Approximated Geometry	Imported Geometry
RTD Die HF	36.8 °C 35.3 °C	35.2 °C	37.1 °C
RTD Die LF	33.8 °C 33.3 °C	33.6 °C	34.1 °C
RTD Outer Ind	27.3 °C	32.2 °C	30.9 °C
RTD Inner Ind	30.2 °C	32.8 °C	31.2 °C

be considered small in comparison with the temperatures achieved (Temperature difference higher than 30 °C. The model using imported geometry is pessimistic giving a security factor in the last step of a design. However, the model with approximated geometry can be automated with a short computation time to give an estimation of the temperature for the critical components in an optimization script, with a reasonable error.

For the RTDs in the inductor PCB, both models are found to be pessimistic. Indeed, the RTDs are placed on the side of the magnetic core. The heat spreading inside the substrate of the PCB is more important in the simulation than in reality. This results in a higher temperature. The difference is mostly due to the top surface cooling model which is constant over the entire surface in the simulation. In reality, the heat transfer coefficient is dependent on the local temperature difference. In the prototype, there is a high gradient of temperature between the copper and the substrate at the top of the PCB stack, observed using a thermal camera. This effect is negligible at the bottom due to the representation of the baseplate which properly spreads the heat.

In consequence, both models are found to give a satisfying results with a maximum error on the temperature difference of 1.8 °C for the dies. For the inductor, a more accurate estimation could be achieved by considering a temperature-dependent convection coefficient on the top surface of the PCB. Both models are found to be satisfying, and their use depends on the objectives ("Imported Geometry": more accurate, "Approximated Geometry": faster).

5.5 Inductor Issues

The "Embedded Toroidal" inductors present several issues. The first issue is the difference in electrical characteristic between inductors with an identical design. The other issues are the inductance decrease and the strong resistance increase with the frequency. In order to understand these issues and improve the inductor design, prototypes are manufactured in house using the 3DPHI platform in Toulouse.

5.5.1 In House Manufacturing Process

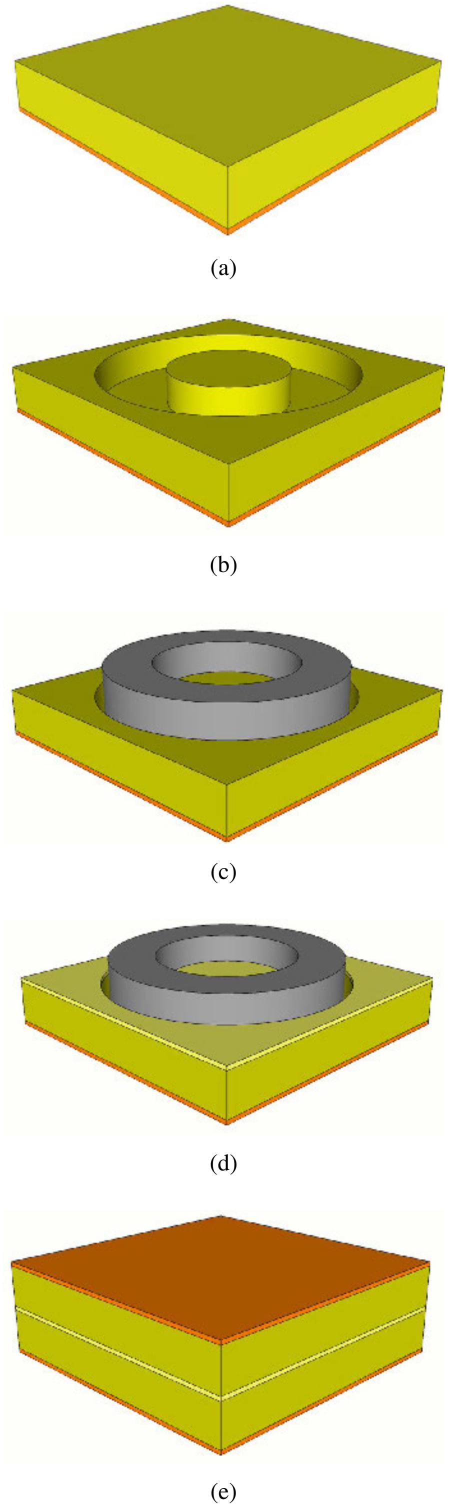
The process uses two one-sided 1.6 mm-thick single face PCB laminates (370HR material, Isola group) (Figure (a)). They are machined using a CNC router (Charly-robot 4U) (Figure (b)). Some clearance (a few 100s of microns) is required in the cavity depth to ensure the magnetic core will fit, and that it will not be pressed during the lamination cycle. This clearance is also required to account for planarity issues during the machining of the laminates. The maximum cavity thickness is defined by the isolation required between the winding (copper tracks) and the magnetic core. The magnetic core is placed inside the cavity manually (Figure (c)). A prepreg sheet (Isola PCL370 HR 1080, Tg=$180\,^{\circ}\mathrm{C}$) is cut using a CO2 laser (Gravograph). This sheet is placed on top of the PCB laminate (Figure (d)). The center part is positioned manually in the interior of the magnetic core. A second machined PCB laminate is placed on top of the stack to fully encapsulate the magnetic core (Figure (e)). Sheets of release film (Pacolon HT2000) are placed under and over the PCB stack. Metal plates and alignment pins (which register with holes drilled in the PCB laminates) are used to maintain the assembly. The latter is placed in a heating press (Specac Atlas) for the PCB lamination cycle. The temperature is increased at a rate of $6\,^{\circ}\mathrm{C/min}$, up to $195\,^{\circ}\mathrm{C}$ and it is maintained at this level for 90 minutes. The laminating pressure is $10\,\mathrm{bar}$ at the beginning and is then increased up to $20\,\mathrm{bar}$ once the temperature exceeds $100\,^{\circ}\mathrm{C}$. At the end of this cycle, the assembly forms a unique, solid part. Via holes (used to form the winding) are drilled in the PCB laminate using a CNC drill (Bungard CCD/2/ATC). The holes are plated with copper, using regular PCB chemistry (Bungard, using a Compacta plating station from the same manufacturer). Finally, the copper layers are selectively masked with a photosensitive dry film (Dupont Riston), according to the Gerber files generated by the design program, and patterned using ferric chloride. An example of collective manufactured prototypes is shown in figure 5.33.

For our prototypes two magnetic materials were used. The first material is a Ni-Fe-Mo powder core (MPP200, Magnetics). The second material is a MnZn ferrite (N87, EPCOS). The MPP200 toroidal core is embedded without any air-gap on the contrary of the N87 one ($1.3\,\mathrm{mm}$ single air-gap). All cores were cut into $3\,\mathrm{mm}$-thick slices using a diamond saw (Struers Discotom 100, equipped with a blade Struers MOD31).

5.5.2 Tests

Embedding Process

The objective of the tests is to investigate the inductor issues. These samples presents the same issues than the samples manufactured by the PCB manufacturer Cimulec. A hypothesis is that the pressure applied on the magnetic core during the lamination process damages its properties. However, with the "in-house" process, there is no pressure on the magnetic core because we machined a cavity deeper than the core thickness. A micro-section of a sample is presented in figure 5.34. This micro-section shows the magnetic core inside the cavity, with an approximately $400\,\mu\mathrm{m}$ clearance between the core and the top of the cavity. No damage is noticeable on



(a)

(b)

(c)

(d)

(e)

Figure 5.32: Process used in-house to manufacture "Toroidal Embedded" inductors.

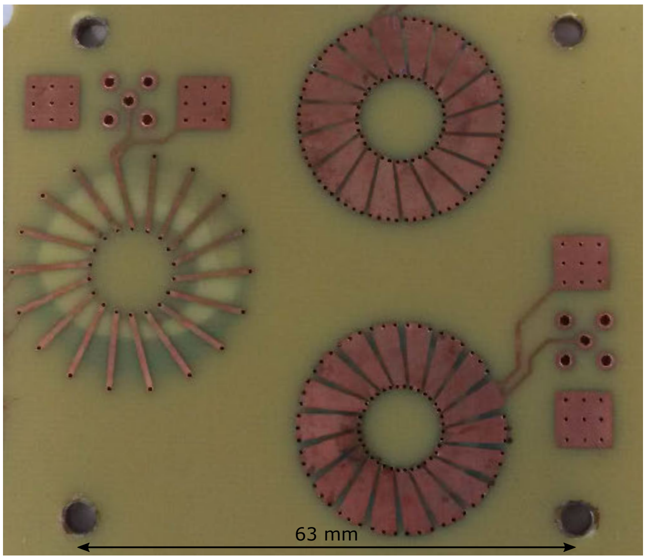


Figure 5.33: In-house collective manufacturing of 3 "Toroidal Embedded" inductors.

the core, except some chipping on the edges (which might have been caused during the preparation of the micro-section). Some of the resin flowed in the cavity during the lamination and maintains the magnetic core at the center. The rest of the cavity remains empty because only one prepreg layer is used to bond the two single-sided PCB. The pressure is not the cause of the electrical issues. It can be noted that with this process the cavity filling is not optimal for the thermal management. More prepreg layers would be required to provide more resin.

The next test is focused on the impact of the machining and the embedding of the magnetic core. The prototype uses a MPP 200 powder core. The machined magnetic core is characterized with a hand wound wire winding prior to embedding. The magnetic core is then embedded in the PCB and characterized again using the PCB winding. Then, copper tracks and vias are removed by etching and the embedded core is characterized using again a wire winding. The inductance results are presented in figure 5.35.

The 3 inductors present the same inductance value at low frequency (inferior to $20\,\mathrm{kHz}$) which is in accordance with the calculation used in the optimization procedure. However, the inductor using an embedded core with a winding formed on the PCB has a strong inductance decrease just after $30\,\mathrm{kHz}$. This inductance decrease also corresponds to a strong resistance increase. This inductance drop is not due to the core machining because the non-embedded core with wire winding presents a curve similar to the characteristic of the magnetic core. With similar tests, the same conclusion was obtained for a ferrite core without air-gap. Therefore, we can con-

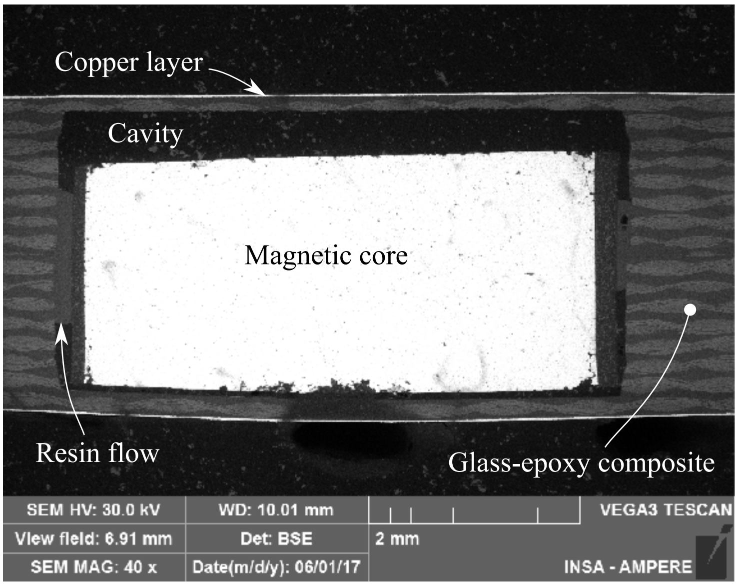


Figure 5.34: Micro-section of an in-house made inductor. Core is maintained inside the cavity at the middle by the prepreg sheet resin. The vias winding are not shown. The barrel shape is an artefact caused by using the microscope at low magnification. The outer surfaces of the sample are actually flat.

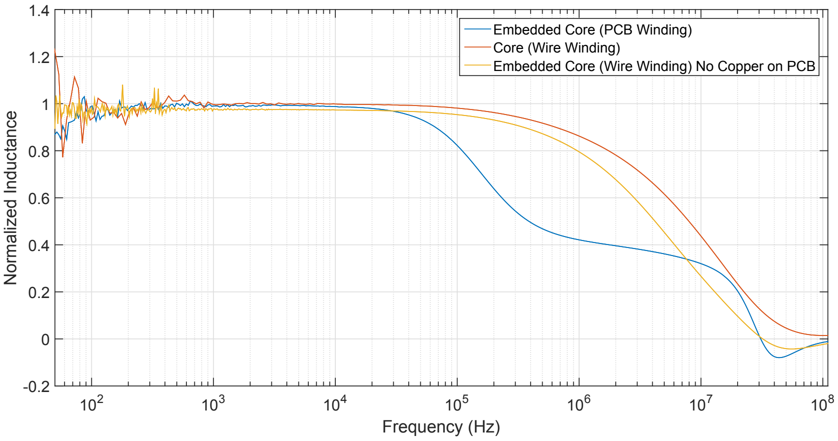


Figure 5.35: Inductance as a function of the frequency for the 3 presented tests (Measured using a E4990A Keysight impedance analyzer).

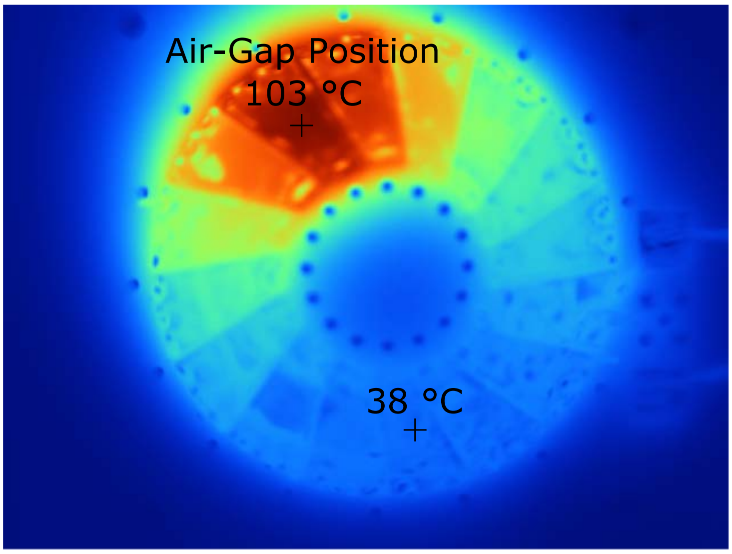


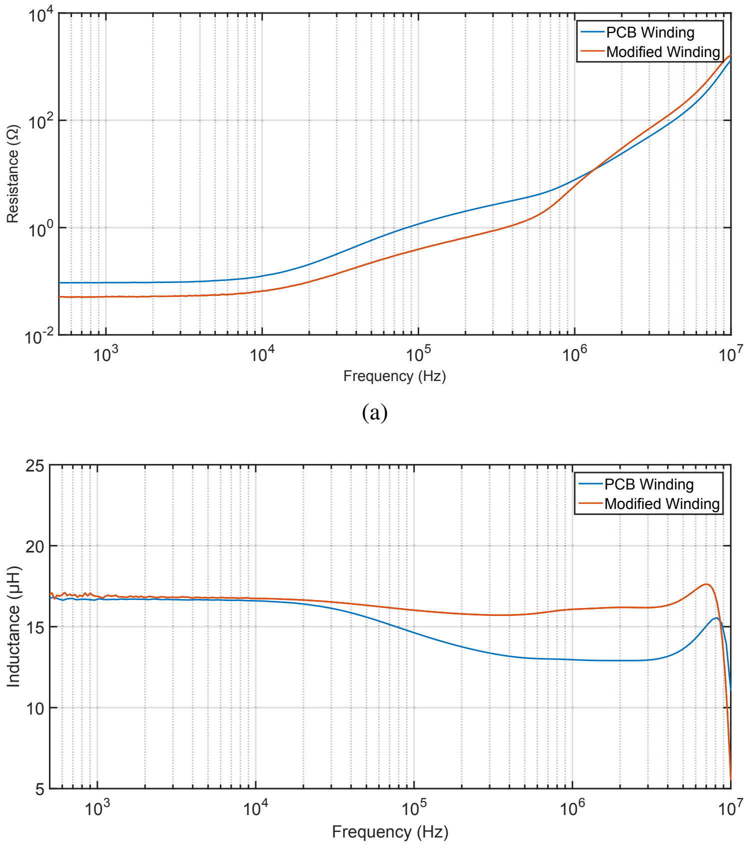
Figure 5.36: Thermography of the DM EMI filter inductor with a 20 kHz, 14 A peak-to-peak current.

clude that the performances of the magnetic core are not significantly affected by the embedding process. This result allows us to focus the tests on the PCB winding.

"Fringing Effect"

The previous tests were done on core without air-gap to not add the negative impact of the "fringing effect". The next tests show the impact of the air-gap. The prototype used a N87 ferrite core. A thermal observation (Figure 5.36) shows that the air-gap has a negative impact on the resistance due to "fringing effect". For the observation, the prototype PCB is covered with a resin to obtain a homogenous emissivity. The inductor is supplied through an amplifier with an arbitrary $20\,\mathrm{kHz}$ $14\,\mathrm{A_{p-p}}$ current.

The clear increase in temperature can be attributed to eddy currents induced in the copper layer by the air-gap. The temperature close to the air-gap is $103\,^{\circ}\mathrm{C}$ while the temperature far to the air-gap is only $38\,^{\circ}\mathrm{C}$. The electrical characterization of the inductor was done through the PCB winding. This winding presents a large surface close to the air-gap. Then, the inductor was modified. The copper close to the air-gap on both sides was mechanically removed. The missing turns were made with a wire soldered to the PCB winding far from the air-gap. As the modified winding presents a lower inductance decrease this confirms the negative impact of the "fringing effect" (Spreading of the magnetic flux path in a non magnetic material compared to in magnetic material). The "fringing effect" can be neglected when the air-gap length is small compared to the dimensions of the magnetic cross section. Here, the air-gap



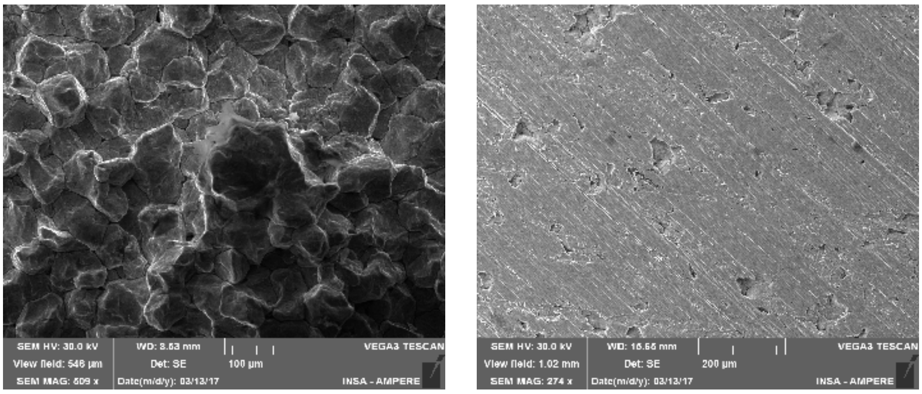
(a)

(b)

Figure 5.37: Electrical characterization of an inductor using N87 ferrite core with a single air-gap. The modified winding corresponds to an "Embedded Toroidal" where the turns close to the air-gap have been replaced by classic round wire turns.

length is $1.9\,\mathrm{mm}$ for a magnetic core thickness of $3\,\mathrm{mm}$. In such case, the air-gap length is no longer negligible in comparison with the magnetic core thickness. The real air-gap cross section of the flux path is bigger that the one used for the design resulting in a higher inductance value than calculated.

It can be noted in figure 5.37 that the inductance has the same value at low frequency because the missing turns were replaced using a wire. The "DC" resistance (the value at $500\,\mathrm{Hz}$) is not equal due to the modification of the winding. The modification of the winding has a positive impact on the inductance. The decrease in inductance value as a function of the frequency is reduced. The resistance increase as a function of the frequency is also reduced (Note that the resistance scale is logarithmic). The "fringing effect" due to the high air-gap length ($1.9\,\mathrm{mm}$ in this case) compared to the magnetic core thickness ($3\,\mathrm{mm}$) has a negative impact on the AC



(a) (b)

Figure 5.38: Picture of the surface using a MEB of the magnetic core surface (a) Crack (b) Cut

resistance and inductance above $20\,\mathrm{kHz}$. The air-gap length has to be limited in the design procedure to limit the "fringing effect". It is also possible to remove the copper close to the air-gap. However, radiated EMI are going to be high.

Nevertheless, the AC resistance at $180\,\mathrm{kHz}$ of the "Embedded Toroidal" inductor is still high regardless of the air-gap. The strong resistance increase was observed on the powder core without air-gap prototypes and on the ferrite core with a single air-gap (with the copper removed close to the air-gap) prototypes. For example, the DC resistance of the previous inductor with the modified winding is $51\,\mathrm{m\Omega}$ while the AC resistance at $180\,\mathrm{kHz}$ is $600\,\mathrm{m\Omega}$. The resistance is multiplied by almost 12.

PCB Winding

The next tests only used cores without air-gap (Iron Powder) to avoid adding issues together. The objective is to investigate the issue coming from the PCB winding. The first hypothesis was the contact between several vias and the magnetic core, which could be caused by an inaccurate process. This contact would create a resistive secondary winding. The powder cores are formed by isolated grains to avoid eddy current at low frequency, which gives a non conductive surface (Figure 5.38a). However, in the preparation prior to the embedding, the magnetic core is cut to obtain a thickness of $3\,\mathrm{mm}$. The cut surface becomes conductive (Figure 5.38b), because the metal is spread across the grains boundaries.

To illustrate the effect of a resistive secondary winding, we compare the inductance (as a function of the frequency) of a powder core embedded in a PCB with that of an identical core (without embedding) with 2 wire-wound windings: one is

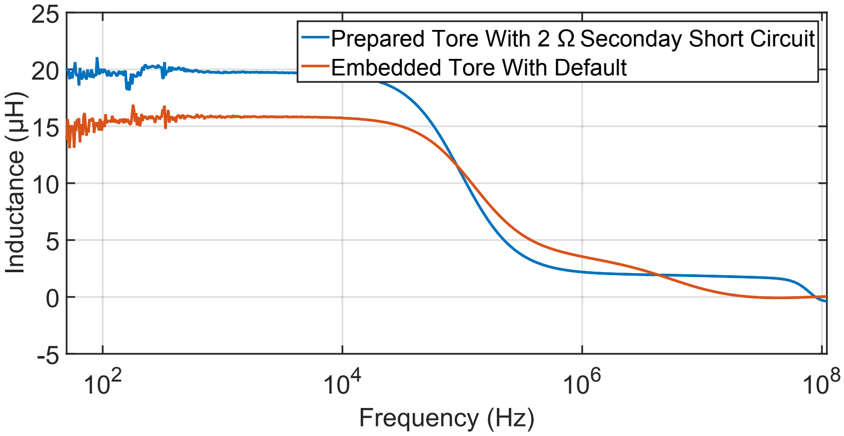


Figure 5.39: Comparison of a sample with issues and a not embedded magnetic core with two windings where one is closed by a $2\,\Omega$ resistor.

connected to a $2\,\Omega$ resistor, while the other is used for the measurements. The results are given in figure 5.39. They show that such a resistive secondary produces similar effects on the inductance as those observed previously.

To investigate this hypothesis further, a hole was drilled in the PCB-embedded inductor to get access to the embedded core. A conductivity check between the core and the winding did not reveal any unwanted contact between these elements. This means that even if the powder core surface had become conductive, this would not explain the drop in inductance with frequency.

In order to understand the inductance decrease and the strong resistance increase as a function of the frequency, 3D magnetic simulations (COMSOL) were performed. Figure 5.40 presents the geometry used for the simulation and the boundaries conditions. Only a part of the inductor (no air-gap considered here) is represented to reduce the number of elements. This choice is due to the observation that the air-gap has a negative impact on the electrical characteristics due to the "fringing effect" but that it is also not the only cause of the issues.

The inductor is surrounded by air with infinite element condition at the outer radius of the sphere. The winding is made of copper. The vias are described as cylinders instead of as hollow tubes as they are in reality to reduce the number of elements in the model. The magnetic core material is custom. It has a linear BH curve with a relative permeability of 200 without induction at saturation. Periodic condition is applied on the cut sphere sides (for the induction and the current density).

The simulation is run for a frequency of $10\,\mathrm{kHz}$, $40\,\mathrm{kHz}$, $70\,\mathrm{kHz}$ and $100\,\mathrm{kHz}$. A $10\,\mathrm{A}$ current is applied at the input of the winding.

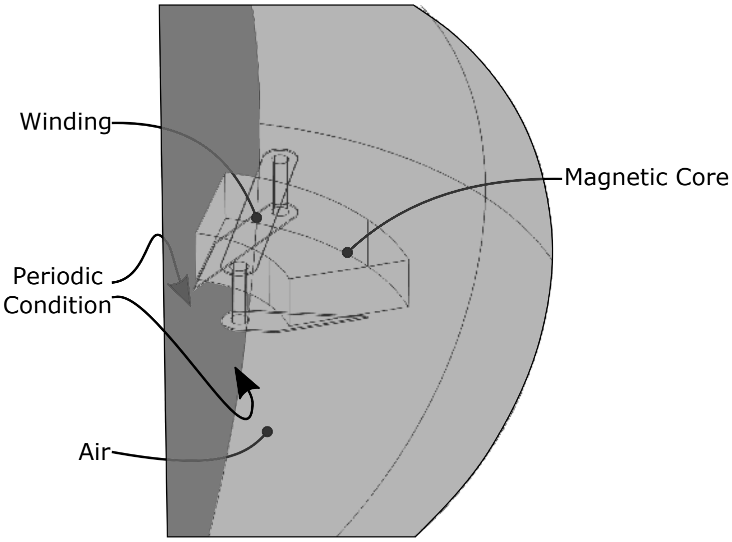


Figure 5.40: Geometry used for the magnetic 3D COMSOL simulation. The periodic conditions are applied on the side of the cut sphere.

The current density is observed in a cut plane of the top PCB track (Figure 5.41). The results for the 4 frequencies are presented in figure 5.42. The colorbar shows the current density value in $\mathrm{A/mm^2}$. Note that the colorbar scale is different for the 4 figures. The black lines show the current density lines (same as the red arrows).

It can be observed that the current uses the full width of the PCB track at $10\,\mathrm{kHz}$. However, with the increase of the frequency, the current density becomes higher on the PCB track edge on one side and on the opposite PCB track edge on the other side. It looks like the current is continuously crossing the PCB track. This effect increases with the frequency. At $100\,\mathrm{kHz}$, the current density lines form a "Z" shape. The AC resistance is then negatively impacted by the decrease of the section and by the increase of the path length.

Several prototypes were manufactured to understand this phenomenon. The first test is to compare the AC resistance increase for the 5 prototypes with different winding width (PCB tracks). Pictures of two prototypes are shown in figure 5.44.

The resistance as a function of the frequency is presented in figure 5.45. The winding width increases with the inductor number. The inductor numbered "1" corresponds to the figure 5.44a and the inductor numbered "5" corresponds to the figure 5.44b. It is obvious that the DC resistance is different for each sample, which is expected. However, there is only a big difference for the inductor "1". The strong resistance increase is similar for the inductor "2" to "5". This increase is a bit lower for inductor "1". The factor K, R_{AC}/R_{DC}, for this inductor is equal to 7 at $180\,\mathrm{kHz}$. So, it can be observed that the strong increase can be reduced using thinner winding.

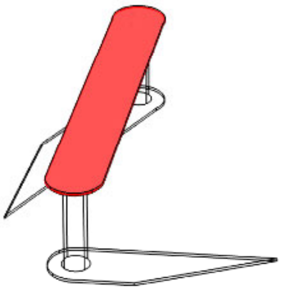
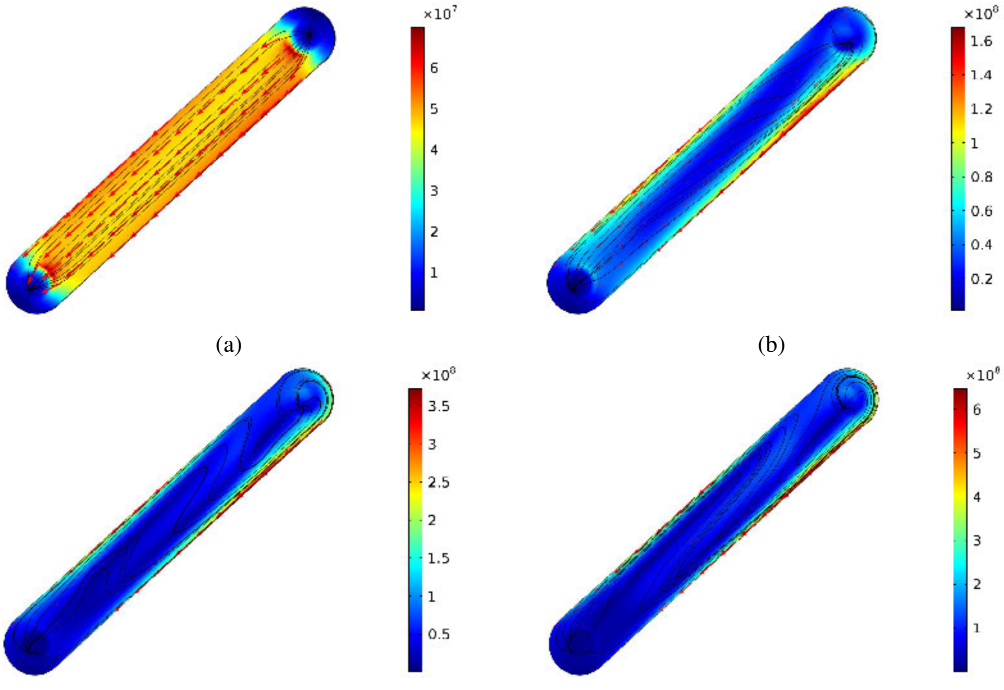


Figure 5.41: View of the cut plane used to observe the current density inside the top PCB track of the winding. The cut plane is the surface at the middle of the top PCB tracks thickness.



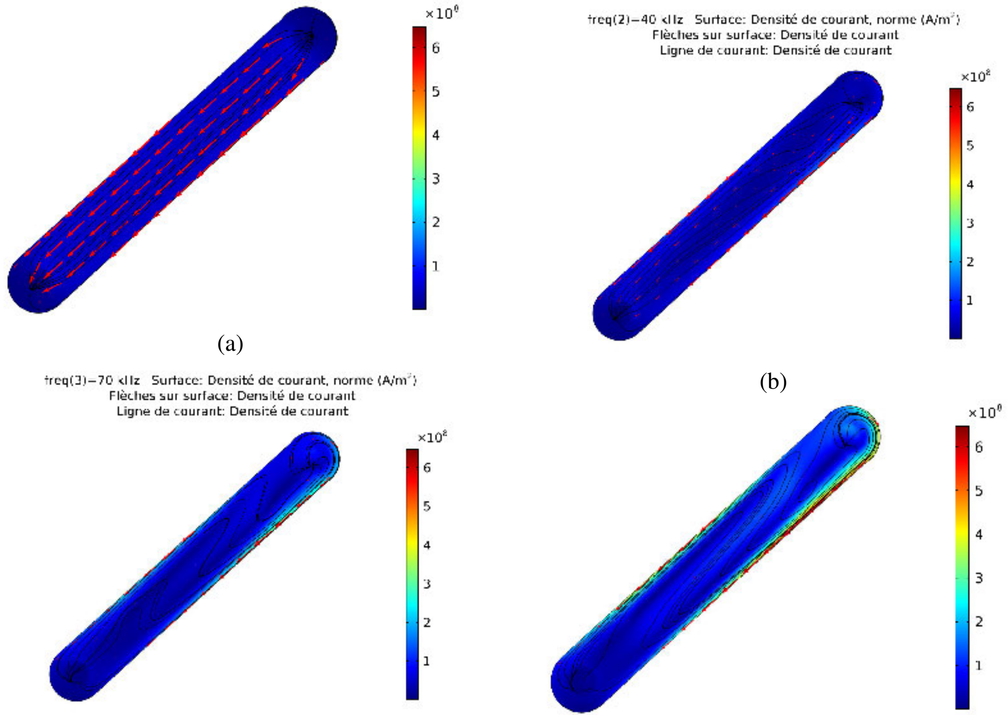
(a)

(b)

(c)

(d)

Figure 5.42: Current density in the cut plane (Figure 5.41) at a frequency of (a) $10\,\mathrm{kHz}$ (b) $40\,\mathrm{kHz}$ (c) $70\,\mathrm{kHz}$ (d) $100\,\mathrm{kHz}$. The colorbar shows the current density value in $\mathrm{A/mm^2}$. Note that the colorbar scale is different for the 4 figures. The black lines show the current density lines (same as the red arrows). These results with the same scale are presented in figure 5.43



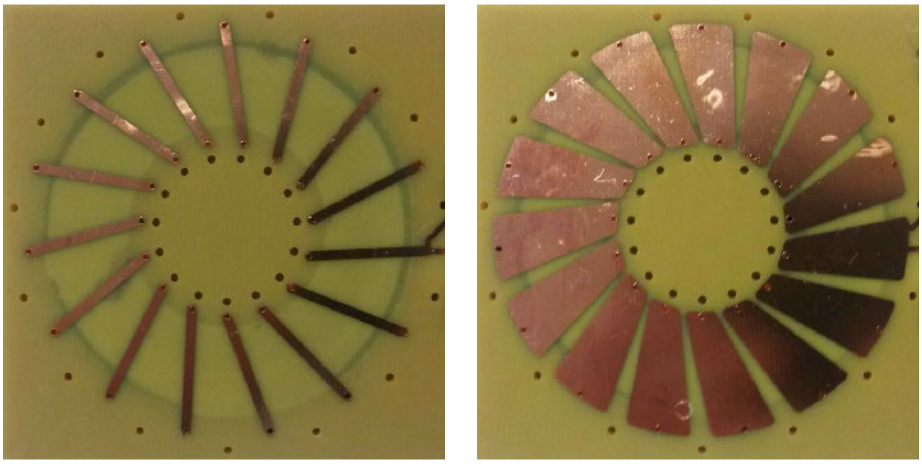
(a)

(b)

(c)

(d)

Figure 5.43: Current density in the cut plane (Figure 5.41) at a frequency of (a) $10\,\mathrm{kHz}$ (b) $40\,\mathrm{kHz}$ (c) $70\,\mathrm{kHz}$ (d) $100\,\mathrm{kHz}$. The colorbar shows the current density value in $\mathrm{A/mm^2}$. The black lines show the current density lines (same as the red arrows).



(a)

(b)

Figure 5.44: Pictures of two prototypes using two different PCB tracks width (a) Thin (b) Large.

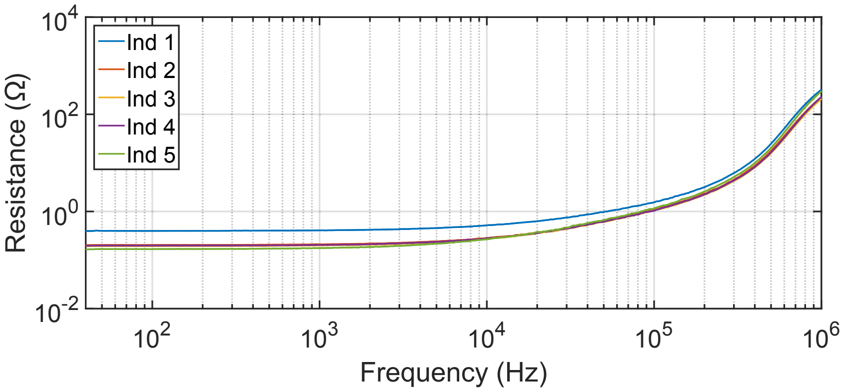


Figure 5.45: Resistance comparison for several prototypes using different winding widths.

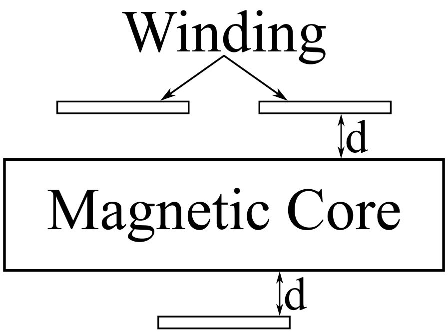
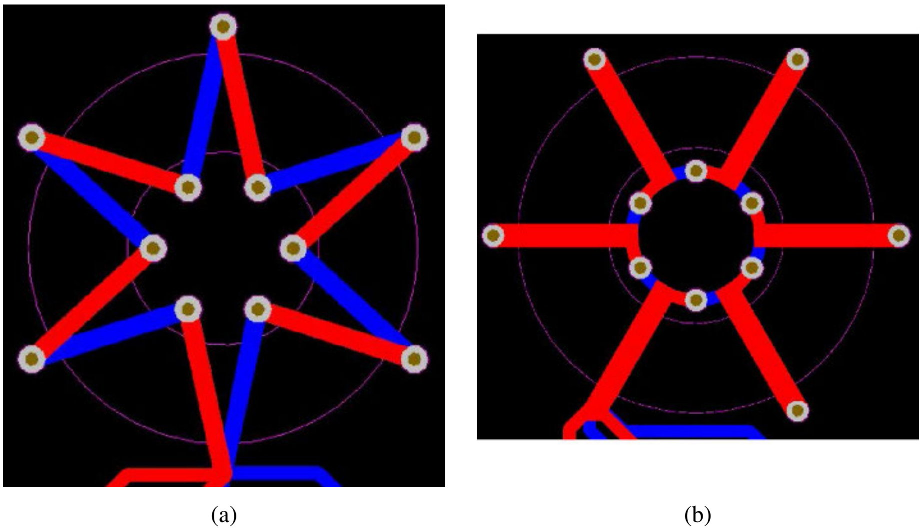


Figure 5.46: Cross section of an inductor showing the winding (top and bottom) and the magnetic core. The distance d is variable for each sample.

However, it is not a practical solution because the DC resistance using thin winding is higher than the ones of samples using larger winding resulting in comparable AC resistance at high frequency.

Another test was to study the impact of the distance between the winding (PCB tracks) and the magnetic core (Figure 5.46). The distance d is different for each sample ($0.2\,\mu m$, $0.5\,\mu m$, $0.8\,\mu m$). Several prototypes were manufactured but no changes were observed in the resistance increase.

The last test considers inductors with only radial turns (Figure 5.47b). It is compared with inductors (with the same magnetic core) using a classic winding (which are at an angle with the radiuses of the magnetic core, both on top and bottom, Figure 5.47a). The hypothesis leading to radial winding is that the current shape obtained in simulation may be due to the magnetic field created by the tangential component of the current in the classic winding. A view of an "Embedded Toroidal" is presented in figure 5.48. A magnetic field crossing perpendicularly the winding is created. The


(a)

(b)

Figure 5.47: Gerber files of two prototypes using two different windings (a) Classic (b) Radial.

resistances of the prototypes are plotted in figure 5.49. It can be observed that the increase is reduced but the resistance at 180 kHz is higher for inductors using radial winding and still does not explain the large increase in resistance with frequency. This solution is not acceptable for power inductors.

As a temporary conclusion, we have not been able to identify the root cause of the performance degradation of the inductors with frequency. The origin of this phenomenon is still not well defined and still under investigation. At this stage, it can be confirmed that it is not caused by the slicing of the cores, nor by the embedding process, but has to do with the PCB winding.

X-ray analysis of the inductors of the PFC / DM EMI filter prototype

The inductors made by the PCB manufacturer use a more complex stack-up. The objective is to fill the cavity with resin. A fully filled cavity reduces the thermal resistance between the magnetic core and the PCB. The risk of delamination or deformation of the PCB is also reduced. As the electrical performance of the inductors was found to vary noticeably from one inductor to the other (Figure 5.15) these inductors were studied with X-ray imaging. The objective is to check the presence of cracks in the magnetic core. Figure 5.50 presents pictures obtained by X-ray imaging of two inductors of the DM EMI filter.

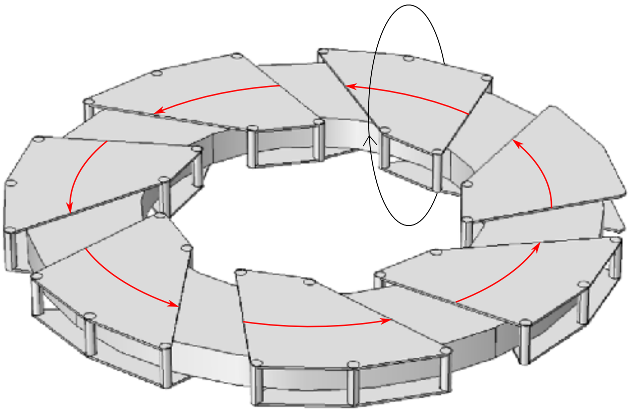


Figure 5.48: View of an "Embedded Toroidal" inductor. The red arrow represents the tangential component of the current in the top layer. The bottom layer has the same tangential component. The loop created induced a magnetic field (black arrow).

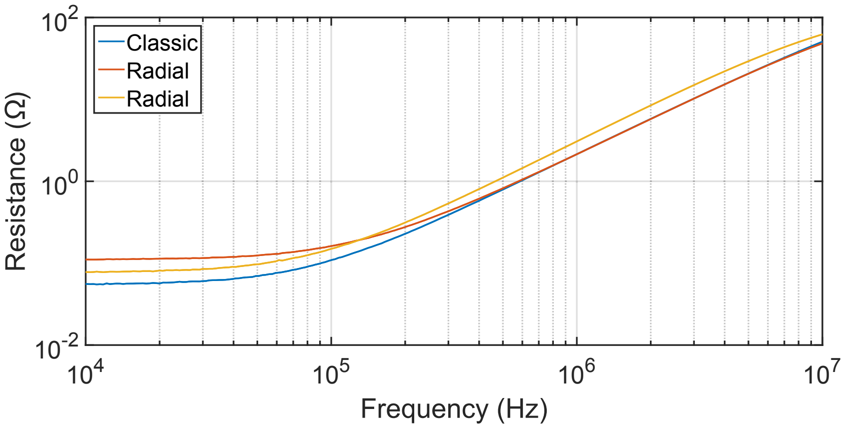
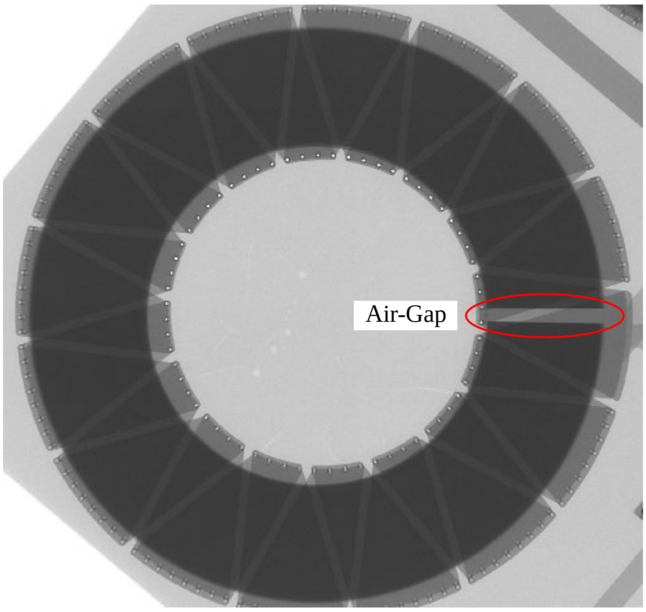
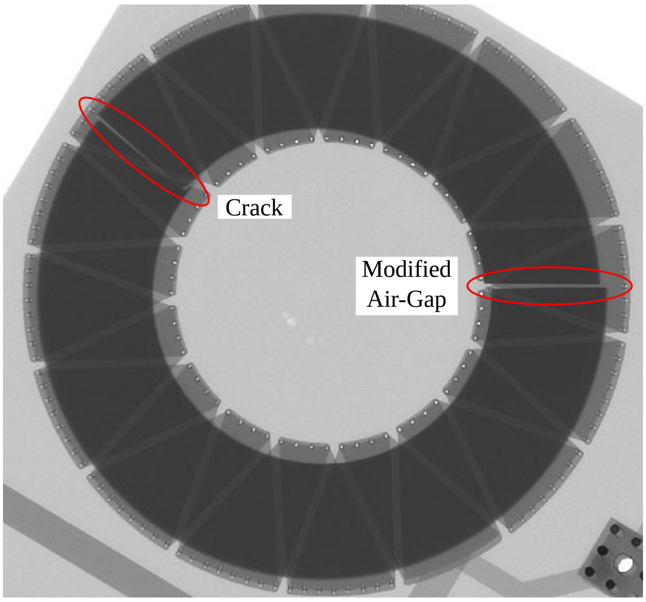


Figure 5.49: Resistance comparison for several prototypes using different windings.



(a)



(b)

Figure 5.50: X-ray imaging of PCB inductors. The magnetic core is (a) not damaged (b) broken on the top left.

It can be seen that the magnetic core present an unwanted crack in figure (b). On 6 PFC "Embedded Toroidal" inductors manufactured, only 1 inductor has a damaged magnetic core. For the DM EMI filter, 3 out of 10 inductors have an unwanted crack. It can also be observed that the magnetic core is not perfectly centered with the winding.

There is no correlation between the inductor issues (Decrease of the inductance with the frequency) and the broken magnetic cores.

The process has to be improved to obtain a high manufacturing yield. However, the cavity is well filled for each sample.

These inductors still have a strong increase of their resistance with the frequency. This issue should be resolved to perform tests on the converter at nominal power.

5.6 Conclusion

In this chapter, the functionality of the converter elements was checked. First, each component was considered separately, starting with the embedded dies. The die coupons show a production yield of $100\,\%$. So, the microvias manufacturing, which was critical, was properly realized. This can also be observed on the PFC module with 4 embedded dies. In these modules, only 1 on 36 dies presents an abnormal gate current (which might have been present prior to embedding). The access resistance of the die coupons has a negligible value compared to the die $R_{DS_{on}}$. Two drivers circuits were also embedded in a PCB to drive the embedded dies in the PFC modules. No functionality issue was shown on the driver circuit. 7 out of 7 Driver PCB are working. Embedded capacitors and embedded diodes were tested into test coupon. The leakage current was used as parameter for capacitor. No change was observed on the embedded capacitors compared to non-embedded capacitors. The forward and reverse characteristics of the embedded diodes show characteristics in agreement to their datasheets.

On the contrary, the embedded inductors show several issues. It was observed that the required value is not achieved. The resistance exhibits a strong increase with the frequency. The causes were investigated with in house prototypes and 3D magnetic simulation. The "fringing effect" has a negative impact due to the non negligible air-gap length compared to the magnetic core thickness. However, it is not the only cause of the issues. Several tests show that the behaviour of the cores is not affected by the embedding process. The 3D magnetic simulation shows that the current in the PCB windings has a "Z" path increasing strongly the resistance with the frequency. Several prototypes were built to try to reduce the resistance of the inductors. These tests were not conclusive. The causes of this change in the current path are still under investigation.

Then, PFC cells were assembled with the 3 PCBs (Die, Driver, Inductor). Each PFC cell current is well shift from 1/4 of the $180\,\mathrm{kHz}$ period. The line current is not properly interleaved because of the inconsistent inductor values. However, the stack-up of 3 PCBS interconnected with wires is working.

The parasitic capacitors were measured on a PFC cell. The error between the simulation and the measurement was $30\,\%$ mostly due to poor control in the TIM thickness.

In one PFC cell, the dies and the inductor were heated up to check the thermal model. The model gives a error of $1\,^{\circ}\mathrm{C}$ for the dies for a $30\,^{\circ}\mathrm{C}$ temperature rise and a large error ($5\,^{\circ}\mathrm{C}$) for the inductor, which remains acceptable. The thermal models are therefore validated.

Chapter 6

Results Analysis

6.1 Introduction

The previous chapter addressed the experiments on the prototype. Several components were checked separately using test coupons. The dies and the driver circuit did not show any issues. However, the "Embedded Toroidal" inductor, which was chosen thanks to its better heat evacuation capability than the "Planar" inductor, shows an inductance decrease and a strong resistance increase after only 10 kHz which was not expected.

In this chapter, each task (Inductor Optimization Script, Converter Implementation, etc) will be discussed. The objective is to remind the objective of each task. The discussion will address the items which are working properly and those which need improvement for a new manufacturing run. In particular, the prototype volume is going to be discussed according to the specifications and the predictions.

6.2 Inductor Optimization Script

6.2.1 Design

The objective of the inductor optimization procedure is to obtain the best inductor regarding two parameters: Volume and Losses. The script is used for the PFC and the DM EMI filter. The optimization procedure allows to compare two structures ("Planar" and "Embedded Toroidal") and magnetic materials.

The first step is the calculation of magnetic parameters and the number of turns to achieve the required inductance value. This step is different for the two types of materials studied (iron powder and ferrite). The inductors using iron powder materials do not have an air-gap. With prototypes made in the platform 3DPHI in Toulouse using iron powder core without air-gap, it is observed that the calculated values for the inductance (at low frequency for "Embedded Toroidal") corresponds to the values expected in the design. On the contrary, the inductors using ferrite materials have an air-gap. The air-gap length is not limited in the procedure. The hypothesis of a negligible air-gap length compared to the dimensions of the magnetic section is not respected for all designs. The "fringing effect" has an impact on the achieved inductance value, and it is observed that the measured inductance values differ noticeably from the predicted values for those designs. In the previous chapter, it was observed that the "fringing effect" was not negligible in the "Embedded Toroidal" due to an air-gap length of more than $1\,\mathrm{mm}$ for a magnetic core thickness of only $3\,\mathrm{mm}$. A possible improvement to the design script is to limit the air-gap length according the magnetic section. The solutions which cannot have a negligible air-gap length compared to the magnetic section should then be discarded. Another improvement which would be required in the design is to prevent copper tracks to cover the air-gap, as this was found to generate strong eddy currents (Figure 6.1). Another solution is to use a distributed air-gap to limit the "fringing effect" but this solution increases the complexity due to the manipulation of several magnetic core parts.

Then, the inductor losses are calculated. The DC resistance is also properly calculated using winding geometry. The error is inferior to $10\,\%$ for the tested prototypes. The AC resistance calculation was estimated using a table with set AC resistance to DC resistance ratios for different frequencies obtained from a single 3D magnetic finite element simulation. This arbitrary simulation does not represent the geometry of any designed inductor. This choice was done to limit the computation time of the optimization script. It was seen that the AC resistance of the "Embedded Toroidal" shows a strong increase of resistance after only $10\,\mathrm{kHz}$, the table gives a K factor of 3.37 for a frequency of $180\,\mathrm{kHz}$.

As the "Embedded Toroidal" was found not to be suitable in our case, a "Planar" inductor was manufactured to be used as PFC inductor. The "Planar" inductor used a 6-layer PCB ($105\,\mathrm{\mu m}$-thick copper layers). The magnetic core is formed by two N97 cores (E32/6/20 and I32/3/20). The windings is composed of 11 turns with a width of $3.25\,\mathrm{mm}$ for the layer with 2 turns or $6.75\,\mathrm{mm}$ for the layer with 1 turn. This allows the converter to operate at nominal power ($3.3\,\mathrm{kW}$) to validate the "Topology" work package (Figure 6.2). The resistance and inductance as a function of the frequency for the "Planar" inductor is presented in figures 6.3 and 6.4 respectively.

The comparison of the K factor used in the script and for both previous prototypes is presented in table 6.1.

It can be seen that the AC resistance used in the script for the high frequency copper losses calculation remains optimistic. For the chosen frequency ($180\,\mathrm{kHz}$),

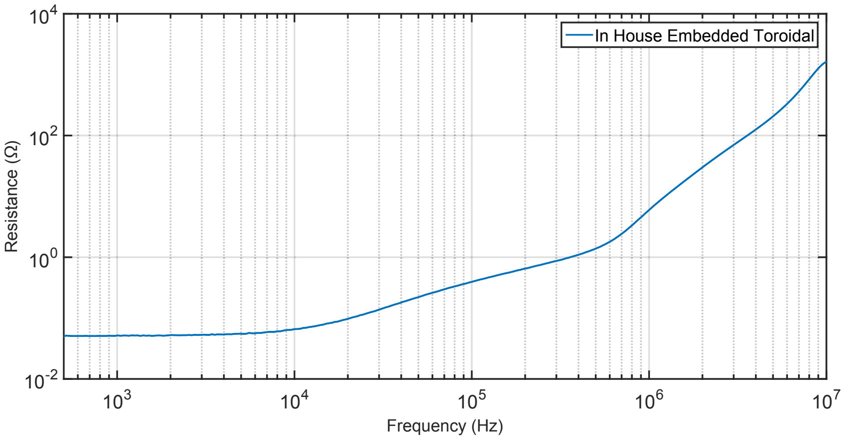


Figure 6.1: Resistance as a function of the frequency for an in-house "Embedded Toroidal" prototype.

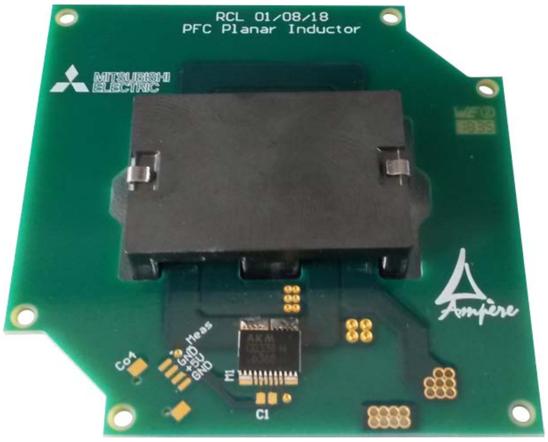


Figure 6.2: A "Planar" inductor manufactured for a PFC cell. The objective is to replace the "Embedded Toroidal" inductors to test the converter at nominal power.

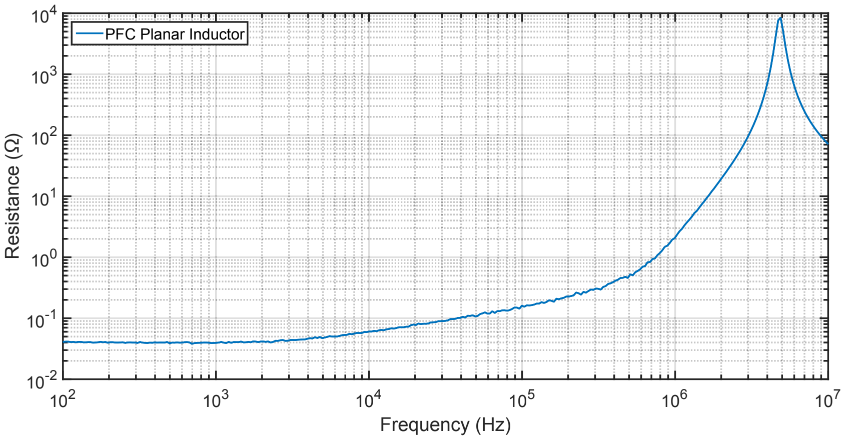


Figure 6.3: Resistance as a function of the frequency for the "Planar" inductor used for the PFC.

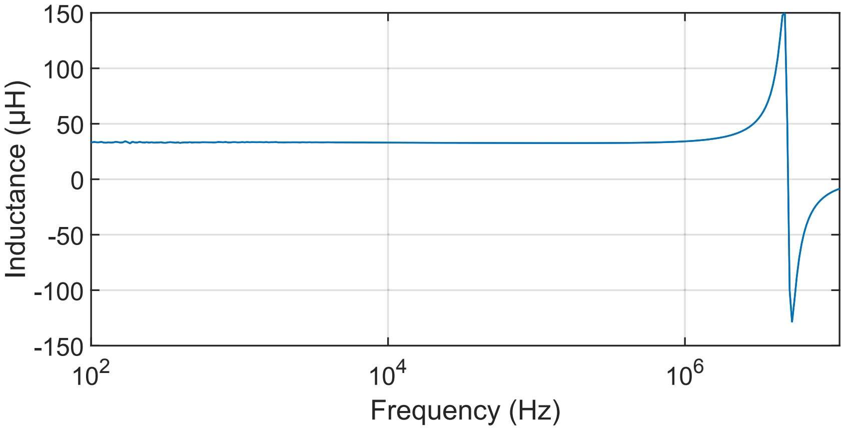


Figure 6.4: Inductance as a function of the frequency for the "Planar" inductor used for the PFC.

Table 6.1: K Factor (R_{AC}/R_{DC}). Comparison between the values used in the script and measured on both inductor types.

Frequency	K Factor		
(kHz)	Script	Planar	Embedded Toroidal
140	2.88	4.48	9.93
180	3.37	5.13	11.95
220	3.58	5.76	13.76
260	3.77	6.37	15.5
300	3.99	7.43	17.24
340	4.40	7.9	18.83

the relative error between the script and the "Planar" prototype is $52.2\,\%$. At the same frequency, the relative error between the script and the "Embedded Toroidal" prototype is $254.6\,\%$. The losses of the "Planar" inductor are still going to be higher than expected but the difference is much smaller than with the "Embedded Toroidal" inductor, allowing full power tests to be performed. The core and copper losses were not separated in the experiment. So the calculation of the core losses was not properly checked.

After losses calculation, the inductor temperature is calculated to ensure it is running at an acceptable temperature (providing it dissipates the power level expected from the script). In the coarse thermal simulation (2D) used in the optimization script, the inductor is directly placed on the heatsink with the help of a TIM. In the prototype, the inductor PCB is positioned as the top element above the die PCB and the driver PCB. The converter PCB stack-up was not decided yet when the converter optimization script was firstly used. Due to the prototype production schedule, it was not possible to run another simulation taking into account the converter assembly. The inductor temperature is then higher that the one expected which was checked with the converter thermal simulation. These thermal simulations should consider the full stack-up in the optimization run.

The parameters of the magnetic materials are dependent of the temperature. The magnetic design of the inductor (for both structure) uses 5 parameters: Relative permeability (μ_r), Induction at saturation (B_{sat}) and Steinmetz coefficients (k, α, β). A database was created for each material with these parameters, taken from the datasheet for a temperature of $100\,°\mathrm{C}$. The resistivity of the copper for losses calculation was also taken at $100\,°\mathrm{C}$. The inductor temperature calculated could be used in a new iteration to obtain the real values of these parameters. The temperature calculation is in the last step of the procedure, just before the choice of the best inductor, so the procedure should include a loop (which would increase the computation time). The computation time is discussed more in detail in section 6.2.2.

The last step is the choice of the inductor according to the best trade-off between the losses and the box volume. The box volume calculation is discussed later in section 6.5.

6.2.2 Computation Time

The inductor script is included in the converter script so a short computation time is needed. For one iteration of the converter optimization procedure, numerous designs of inductors for the PFC and the DM EMI filter are studied. The inductor script studies a high number of magnetic cores in a short time. The converter script takes approximately $7\,\mathrm{h}$ to gives the optimum converter. In the converter optimization procedure, the inductor optimization script takes most of the time (typically 5-$6\,\mathrm{h}$ over the $7\,\mathrm{h}$ total) because it relies on 2D FEM or IGSE calculations. The respective weight of FEM and IGSE is largely dependent on the inductor design. In some cases, the thermal simulations take most of the time (if many configurations have to be discarded for thermal reasons), in other cases, it is the IGSE calculations.

The initial steps of the inductor optimization procedure (Core geometric parameters variation, Magnetic design, Winding design, Induction check) have a short computation time thanks to the matrix (parallel) calculation. It is also the case for the copper losses calculation. However, the core losses calculation is done one inductor at a time. The same is true for the thermal simulation. To save time, the thermal simulations are not performed on all design configurations, but only to those which belong to the Pareto front (and, if these we found to exceed $100\,^{\circ}\mathrm{C}$ maximum temperature, to their closest neighbour until a suitable configuration is found). These two steps represent more than $90\,\%$ of the total computation time of the inductor optimization procedure.

A thermal simulation alone takes approximately $1\,\mathrm{s}$. The computation time is very dependent on the inductor structure and on the core geometric parameters variation limits. With the "Embedded Toroidal" structure, which as a good thermal management capability, only a few iterations are required to discard designs which would lead to overheating inductors because the temperature limit is easily met. On the contrary, the "Planar" structure needs numerous iterations to obtain a Pareto front with acceptable inductors, which increases strongly the computation time. The range of core geometric parameters can be reduced to limit the computation time. But with this method, it is possible to miss a good solution.

As previously explained, the thermal simulations are only run for for the inductors on the Pareto front. Only the inductors with a hot spot temperature exceeding $100\,^{\circ}\mathrm{C}$ are discarded, resulting in a new Pareto front. The other inductors are simulated again. The computation time could be reduced by not doing a new simulation of validated inductors.

The core losses calculation is also time consuming. The calculation is done using iGSE. The signal has to be separated into major loop and minor loops. Due to this separation, the calculation is done inductor by inductor.

In conclusion, with a moderate effort, it is estimated that the inductor design procedure could be accelerated. It is however already fast enough to be used in the design procedure, especially compared to a manual design or to a prototyping step.

6.3 Models

6.3.1 Converter Thermal Simulation

The converter thermal simulation was separated into two studies: the heatsink and the PCBs stack-up (including the heatsink baseplate). The separation allows to use an equivalent heat transfer coefficient to simplify the heatsink (only its baseplate is considered) in the PCBs stack-up simulation, drastically reducing the computation.

The heatsink was represented with two models. The first model is analytical. The second model is based on a CFD software (IcePak). The computation time of the first model is only few seconds (Once the script made) for at least $1\,\mathrm{hour}$ for the second model (Plus a licensed software). The two models give similar heat transfer coefficients in the operating temperature range (120-140 $^{\circ}\mathrm{C}$).

The PCB stack-up was also represented with two models, both based on FEM. The first model uses a unique prismatic block to represent each layer. The thermal conductivity of each block is adapted to represent the average layout of the corresponding layer (heat spreading, area filled with vias). The heating elements are also added to the model with an associated power dissipation. The second model uses the imported geometry of each PCB using ODB files directly exported from Altium Designer. The small PCB tracks of the driver PCB and the associated vias are removed to reduce the computation time. In both models, the TIMs and the heatsink baseplate are added. The equivalent heat transfer coefficient from the heatsink models is applied to the bottom of the baseplate (Equation obtained by a power curve fitting of the results). On the top surface, a heat transfer coefficient of $12\,\mathrm{W}/(\mathrm{m}^2 \cdot \mathrm{K})$.

The results show a difference of only $1\,^{\circ}\mathrm{C}$ between the temperatures obtained by simulation and experiment for the RTD located above the dies. The difference is more important for the RTD in the inductor PCB ($5\,^{\circ}\mathrm{C}$). This can be improved by defining a topside heat transfer coefficient with a temperature dependence (It is considered constant, which is a coarse approximation). Such temperature-dependent natural convection models are available in the literature.

The model using the analytical model for the heatsink and the approximated geometry has the lowest computation time. An improvement can be the automation of this model. Indeed, the heatsink analytical model inputs are the dimensions of the heatsink. The calculation of the equivalent heat transfer and the curve fitting could be automated with MATLAB and exported into COMSOL using the interface module. The geometry could also be described using this interface because it is simple (one unique block per layer). The thermal conductivity adaptation of each layer to represent the reality could be done with a GERBER files analysis. For example, the copper layer thermal conductivity in the plane could be calculated using the percentage of copper over the total surface area. In the same way, the substrate layer conductivity could be calculated from the number of vias, their size and the copper thickness deposition. With an automated process, each block could even be subdivided (i.e 10×10 blocks) to be more accurate for large-area PCBs. This idea was not implemented in this thesis.

6.3.2 Parasitic Elements Simulation

The separate measurement of the parasitic capacitors is difficult due to the embedded components. Due to the routing, the only parasitic capacitor we measured is between the $DC-$ and the ground but it also includes $DC+$ to ground (among others). The measured value is close to the simulated value taking into account the poor control in the TIM thickness.

The parasitic capacitors were calculated to be used in the CM perturbation model in order to design the CM EMI filter. For the prototype, the CM EMI filter was designed using arbitrary values because the routing was not decided yet. However, the parasitic capacitors between HF or LF midpoint and the ground have lower values than the arbitrary values used for the first iteration. The CM EMI filter volume would be reduced in the next iteration.

In addition, the parasitic capacitors between the $DC+$ or the $DC-$ and the ground are helping to filter CM. However, the values of these two parasitic capacitors have to be of the same value to prevent mode transfer. This observation was done after the routing of the prototype so these two parasitic capacitors are not equal.

Also, the mode transfer was not taken into account in the filter design. The next iteration has to be routed to ensure equal parasitic capacitors between the DC nets and the ground. This change will allow to ensure the respect of the standard.

Parasitic inductance modeling was not addressed in this thesis, both because of lack of time and because the expected low inductance values would have been difficult to validate experimentally. The full power tests which are currently being carried out will confirm whether these inductors have a strong effect or not.

6.4 Converter Implementation

In the initial planning, the "Implementation" work package was supposed to rely on 2 manufacturing runs to provide a prototype meeting the specifications. Due to delays in the "Topology" work package and manufacturing time of 8 months for the prototype, there was eventually time for a single prototype only.

It was observed that some "Embedded Toroidal" realized with the PCB manufacturer present crack in the magnetic core. The stack-up used to form the spacer has to be modified to limit the pressure on the magnetic core while filling cavities completely to ensure a good thermal management. While the manufacturing issues should be solved easily, this is not clear regarding the large increase in resistance we observed above 10 kHz. The origin of the strong resistance increase was attributed to the shape of the winding but could not be fully explained. More investigations are necessary to find a winding shape reducing the AC resistance while maintaining the DC resistance at a low value.

The converter implementation was mainly focused on the mechanical assembly of a PFC cell. A PFC cell uses 3 different PCBs with embedded components (Dies, Driver Circuits, Inductors). Each element was built as a separate PCB to limit the risk of functionality issues. In addition, the PCBs with embedded driver, embedded inductor and DM EMI filter were manufactured on the same panel to limit the panel number. There is not limitation to embed SMD components with magnetic core. The dies are embedded in another panel as they require a PCB with different stack-up configuration. However, it can be imagined that the driver PCB and inductor PCB could be integrated in a single PCB. The magnetic core would be embedded alongside driver components. This PCB should be placed directly on the top of the die PCB. The objectives are to reduce the assembly complexity, to keep the driving parasitic elements low and to achieve a better thermal management of the inductor.

In the current prototype, the available space in the inductor PCB is not large enough for all driver components. The aim is to embed the output stage of the driver for the high frequency dies. In addition, the driver PCB and inductor PCB had 4 copper layers. A stack-up using 4 $105\,\mu\mathrm{m}$-thick copper layers was chosen to reduce the manufacturing complexity when the circuits (Inductor or Driver circuit) only needed 2. The routing space available with these 2 more copper layers was not used in the prototype. The components which cannot be embedded (Driver for the low frequency dies for example) could be placed on the top of the PCB. The components for the control (Measurement conditioner, DSP, etc...) can also be split over the PFC cells. In the current prototype, the control components were placed on an auxiliary PCB, which strongly increases the box volume of the converter.

Another issue is both isolation and interconnection of the PCBs. In the prototype, the interconnections were made using wire soldered to the PCBs. This method needs machining of the PCBs and heatsink around the soldering area to accommodate for the solder volume while ensuring contact between flat surfaces. The machining cannot be placed at the location of an embedded component, so the PCB routing has to be adjusted, resulting in larger the parasitic elements. Also, the reliability of such interconnection for power was not studied. The isolation is made using an electrically insulated TIM. TIMs are expensive material. The chosen TIM cost approximately 33 € for a sheet of $305 \times 254\mathrm{mm}^2$ which is fully used for the realization of 4 PFC cells (1 converter). Another interconnection method for PCBs is the sinter and lamination technology developed by Fraunhofer IZM. The interconnections are realized with silver sintering while the isolation is done using prepreg layers. Both are performed during the same lamination step. With this technology, the parasitic elements due to the interconnection between the die PCB and the driver PCB could be reduced compared to the ones in the prototype.

The prototype used embedding technology for all electrical components. However, for the thermal management, only a classic straight fin heatink is used. The heat is spread in the die PCB through copper planes. However, the copper thickness in this PCB is limited to $70\,\mu\mathrm{m}$ for dies interconnection. The heat spreading could be improved with a dual-phase system. Today, heat pipes can have a ranging size from $2\,\mathrm{mm}$ and rectangular shaped cross sections. For example, such heat pipes are used in smartphones. These dimensions are compatible with PCB dimensions. In [70], a heat pipe embedding technology is called "heat pipe last". The PCB is firstly manufactured then the heat pipe is positioned in a cavity and connected with galvanic copper deposition. Figure 6.5 presents the concept of inserted heat pipe in PCB. With this technology, it is possible to ensure PCB functionality before connecting the heat pipe, avoiding waste of materials.

The converter free space could be filled with capacitor banks. Indeed, the optimum PPB (E-capacitor, not implemented in this thesis but designed in J. Le Leslé thesis [57]) uses 512 ceramic capacitors. These capacitors were chosen due to their

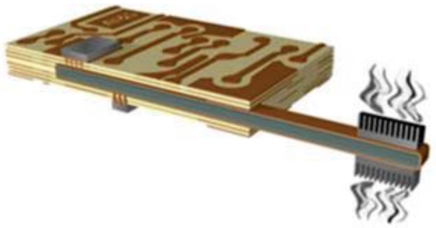


Figure 6.5: Concept of the "heat pipe last" technology. The heat pipe is assembled in the PCB after manufacturing [70].

high capacitance density and their low losses. These capacitors could be split into several capacitor banks to suit the shape of the different converter stages. The box volume would not increase with this method.

6.5 Converter

In order to have a fully working converter (PFC + EMI Filter), the PFC "Embedded Toroidal" inductors were replaced with "Planar" inductors. The prototype DM EMI filter using "Embedded Toroidal" has broken magnetic cores in addition of a high resistive behavior. A proper EMI filter (CM and DM) was manufactured using "Planar" inductors. The new EMI filter is presented in figure 6.6. The details of the design are not presented here, for the sake of brevity.

6.5.1 Box Volume

The converter volume is used (through the power density calculation) to choose the best converter. The volume calculation method has to be checked. Table 6.2 compares the box volume calculated by the script, measured on the prototype and measured without free space due to the mechanical assembly driven by the inductor PCB. This latter value is obtained by restricting the calculation of the envelope of the components and internal interconnects (Figure 6.7 as an example).

A prototype of "Planar" was realized for the PFC, the volume calculated is $17.51\,\mathrm{cm}^3$ while the prototype has a volume (using inductor contour) of $17.48\,\mathrm{cm}^3$. The volume of the "Planar" inductor prototype is $61.25\,\mathrm{cm}^3$ because the PCB outline ($7{\times}7\,\mathrm{cm}^2$) designed for the "Embedded Toroidal", while the magnetic core thickness of the "Planar" is more important and its form factor is close to a cube. The small difference between the script and the measurement using contour is due to machining tolerance. For the "Embedded Toroidal" used for the PFC, the calculated volume is $15.82\,\mathrm{cm}^3$ while the prototype volume is $22.05\,\mathrm{cm}^3$. However, the difference is only

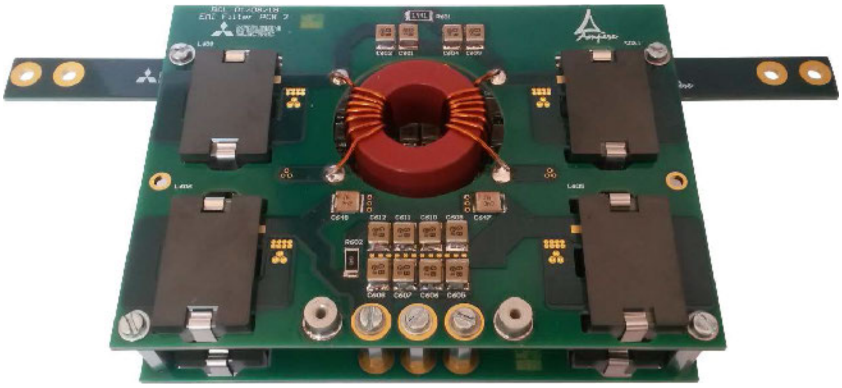


Figure 6.6: Picture of the EMI filter (CM and DM) using "Planar" inductors used as a replacement for the faulty EMI filter based on "Embedded Toroidal" inductors in the full power tests (Not presented here).

due to the difference between the expected and real thickness of the PCB. Indeed, the thickness in the script was $3.2\,\mathrm{mm}$ while the real thickness is $4.5\,\mathrm{mm}$. The manufacturer confirmed that, the thickness of the PCB can be reduced for a second production run by improving the stack-up used for the spacer. Also, using the knowledge of the PCB manufacturer and of the prototype, a better thickness can be defined in the script. The PFC inductor volume is well estimated in the script because the PCB design rules were considered at the optimization stage. The PCB to PCB interconnection are also located in the inductor volume, taking advantage of the free angles.

On the contrary, a DM EMI filter stage is composed of several capacitors and 2 inductors. A stage has 4 connections to other PCBs in addition of the inner interconnections. The volume is increased by these interconnections. The volume of a second stage is $43.7\,\mathrm{cm}^3$ while the calculated volume using the components box volume is $37.8\,\mathrm{cm}^3$. A picture of the second stage is presented in figure 6.7. The relative error in the volume calculation is $15.6\,\%$ ($5.9\,\mathrm{cm}^3$). The calculation only considers the PCB and not the interconnections between PCBs.

The optimal number of stages for the DM EMI filter is 4. So, the error volume due to interconnection in the DM EMI filter is $4{\times}11.9\,\mathrm{cm}^3 = 47.6\,\mathrm{cm}^3$. This volume is almost twice the volume calculated for a stage in the script. It is also a little bit higher than the measured volume of the second stage. With a volume calculation taking into account the interconnection between the components and the different stages of the EMI filter, the optimal number of stages would probably be reduced compared to the result obtained for the prototype.

The driver circuit also shows a high error. It is composed of numerous small components, requiring clearance and interconnection, which already induces an error

Table 6.2: Box volume comparison between the values calculated by the script, measured on the prototype and measured considering only the envelope of the components and their internal interconnects.

Components	Box Volume (cm^3)		
Name	Script	Prototype	Modified
Planar	17.51	61.25	17.48
Embedded Toroidal	15.82	22.05	22.05
DM EMI Filter (Embedded Toroidal)	151.1	176.4	128.7
Driver	2	22.05	9
Dies	7.6×10^{-3}	3.33	1.25
Heatsink	329	490	490

in the volume. But most importantly, the converter is using a stack-up of several bricks with a common outline of $7{\times}7\ \mathrm{cm}^2$ and the driver PCB is manufactured on the same panel as the inductor PCB, which means its thickness is $4.5\,\mathrm{mm}$. As a result, the layout and the thickness of the driver PCB are much larger than strictly required, hence the large error.

Improving this calculation would require a good knowledge of the converter structure at the optimization stage. For example, in this case, increasing the inductor diameter or thickness results in an increase of the volume of the driver PCB.

The bare die size is $3.36{\times}3.1{\times}0.180\,\mathrm{mm}^3$. Obviously the PCB is thicker than the die due to the interconnection and the copper ($70\,\mu\mathrm{m}$) used to carry power current. In addition, to spread the heat, a copper plane bigger that the die is placed under the die. The current capability and the thermal management design rules are not taken into account in the script and increase strongly the volume which induces a strong error in the volume calculation. However, note that the optimal design should contain twice as many dies in the same footprint reducing the corresponding error.

The volume of the heatsink was calculated using the losses with a coefficient of $5\,\mathrm{cm}^3/\mathrm{W}$. This coefficient was really optimistic. The feedback of the coefficient value using the heatsink is $9.8\,\mathrm{cm}^3/\mathrm{W}$. In a new run, this coefficient should be increased which will strengthen the impact of the thermal management on the optimum converter. With this new coefficient, the optimal converter efficiency should be higher to limit the volume of the heatsink.

As for the thermal simulation (Inductor placed on a heatsink while it is not the case in the converter assembly), an idea of the converter assembly at the beginning

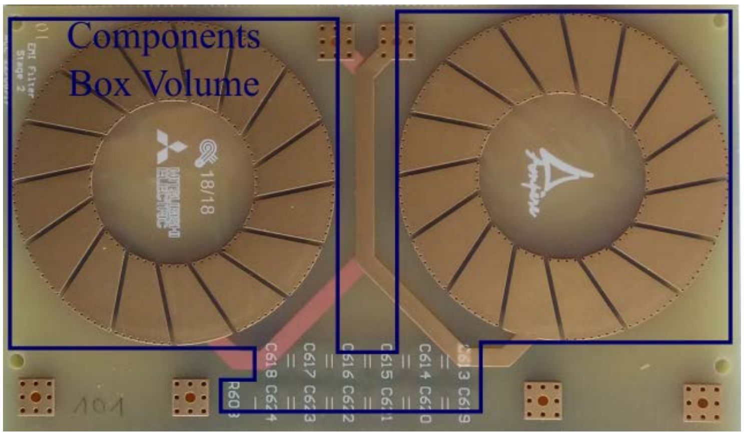


Figure 6.7: Photography of the second stage of the DM EMI filter. The blue line is used for the calculation of the "Modified" box volume in table 6.2.

of the project would improve the volume calculation. The optimum converter is negatively impacted by the error on the volume calculation. Another possible improvement for an industrial product is to add the cost in the optimization.

The box volume objective in the specification is $1\,\mathrm{L}$ all inclusive which gives a power density of $3.3\,\mathrm{kW/L}$. The prototype using "Planar" with the capacitor bank is $2.65\,\mathrm{L}$ which gives a power density of $1.25\,\mathrm{kW/L}$. The power density could be improved with a better mechanical assembly of the EMI filter. Indeed, the EMI filter creates free space due to its length ($13\,\mathrm{cm}$) shorter than the 4 aligned PFC cells ($28\,\mathrm{cm}$). The free space due to its difference has a volume of $0.675\,\mathrm{L}$. The capacitor bank also has free space due to the power nets $DC+$ and $DC-$ routing on the PCB. This free space has a volume of $0.5\,\mathrm{L}$. Without this free space, the power density is $2.2\,\mathrm{kW/L}$ ($1.5\,\mathrm{L}$). The volume repartition is given in figure 6.8.

The interconnection also increases the converter volume compared to the calculations used in the script. It is possible to achieve the target power density, even if this objective is challenging, with an optimization taking into account an mechanical assembly between the 3 elements (EMI filter, PFC and capacitor bank).

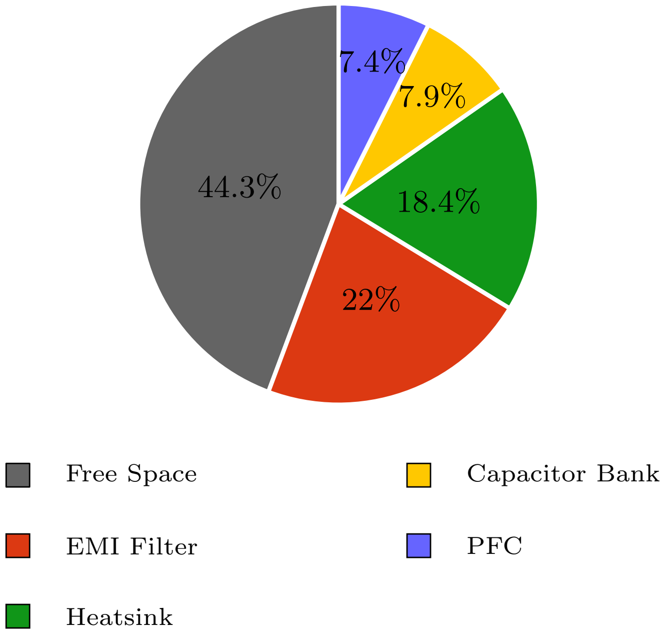


Figure 6.8: Percentage of the volume of each element in the prototype.

6.6 Conclusion

In this chapter, the experiments results were compared to the models. The analysis of the results shows some possible improvements for the inductor optimization procedure. The magnetic design should take the air-gap length into account to have a negligible "fringing effect". The AC resistance calculation of the inductor was optimistic. The inductor losses were under evaluated so the optimum converter puts an important constraint on the PFC inductors. The "Embedded Toroidal" presents a strong resistance increase with the frequency. Investigations are necessary to understand and limit this AC resistance. The manufacturing process developed by the PCB manufacturer is not optimal but presents good results for a first try. The stack-up for the spacer has to be modified to reduce the pressure on the magnetic core. The computation time of the converter optimization procedure is acceptable to compare several sets of input, but solutions were proposed to accelerate it.

The converter simulations give a good estimation of the dies temperature. Nevertheless, the top heat transfer coefficient can be improved to obtain a better temperature estimation of the inductor PCB. The model using heatsink analytical model and PCB stack-up approximated geometry can be automated. The calculation of the parasitic capacitors also shows good results. It allows to reduce the volume of the EMI filter. In a new iteration of the prototype, the parasitic capacitors between the DC nets and the ground should be equal.

The main possible improvement in a converter design in general is to consider the converter mechanical assembly at an early stage of the design. The different mechanical assembly between the EMI filter, PFC and capacitor bank occupies $44.3\,\%$ of the converter volume. For the EMI filter, it is mostly due to the change needed because of the dysfunctional "Embedded Toroidal" inductors. The capacitor bank free space is due to the components type and the design rules for the ampacity. The PPB has a smaller volume and reduces the free space created by the difference in PCBs heights.

By considering the mechanical assembly at an early stage of the design, a better calculation of the volume of each element, taking into account the interconnections, could be achieved. The inductor procedure could use a thermal simulation which represents the real implementation of magnetic components. This simulation could give a feedback on the inductor temperature to change the values of the temperature dependent parameters. A first converter routing also allows to obtain a first estimation of the parasitic capacitors which are used for the CM EMI filter design. The mechanical assembly can also be used to check the converter thermal management at an early stage.

The optimization of the PFC gives interesting results with 4 interleaved cells. The PCB embedding technology was used for all dies, driver circuit and inductors. The 4 cells occupy $0.69\,\mathrm{L}$. The volume of the EMI filter is $0.59\,\mathrm{L}$. The sum of the volume of these two elements is $1.28\,\mathrm{L}$. The converter volume is more important ($2.65\,\mathrm{L}$) than expected ($1\,\mathrm{L}$) largely due to the interconnection between these two elements. It is mostly due to the change of in EMI filter (Change from "Embedded Toroidal" to "Planar" inductors). The converter box volume could be strongly reduced with a new mechanical assembly. And a new optimization step, including the improvements proposed above, would likely result in a different design (fewer filter stages to reduce interconnects, stronger focus on efficiency to save on heatsink volume).

Chapter 7

General Conclusion

The trend in power electronics is to decrease the volume and increase the efficiency of the systems. Power electronics integration is used to manage the numerous interconnections. However, the integration is currently the limiting factor for the development of power converters. The PCB integration allows to achieve mass production with automated manufacturing and assembly, while reducing the system volume. The embedding technology using PCB is well developed for active components. However, it is still in a research phase for passive and thermal components. Yet, these components represent a large share of a converter volume.

The objective of this thesis was the implementation of an AC/DC bidirectional converter using the PCB embedding technology. The aim is to study and to discuss the interest of the embedding technology on each power component. It was shown in the state of the art that the die embedding is well developed. In order to achieve the value of capacitor or resistor needed in power electronics, SMT components are embedded. An inductor optimization procedure was done to compare classic "Planar" inductor with a new design called "Embedded Toroidal". This new design uses an embedded magnetic core in the PCB. It was shown that the volume of inductors could be reduced using this new design. In addition, this design is limited by the PCB design rules which can be improved in the future.

The mechanical assembly was developed around a PFC cell which is composed of 3 PCBs: Die PCB, Driver PCB and Inductor PCB. The manufacturing processes for the two panels were discussed with the PCB manufacturer. Embedding the components increased the manufacturing time due to the necessity of additional plans and increased complexity compared to a standard PCB process.

The 3 PCBs are stacked and separated by a TIM to improve the thermal contact and ensure the electrical insulation. A heatsink is placed at the bottom, forming a compact assembly for a PFC cell. The results of the die embedding are excellent with 97 % yield. It is the same for the driver components which were all found to be working after embedding. However, the "Embedded Toroidal" inductors showed some issues and were replaced by "Planar" inductors. The issues are still under investigation. However, the connected PFC cells are working.

A simple thermal model was developed for the PFC cell. This model has a short computation time and can be automated. It was validated by thermal experiment. The model for parasitic capacitors, generated using the files from the routing software, was also validated. An automatic interface between these software could improve the leadtime of a converter implementation.

The result of this thesis is a working PFC with a 4 interleaved cells. The EMI filter is composed of 4 DM stages and 3 CM stages. The PCB embedding technology was used for all dies, driver circuits and inductors. The target volume (from the specifications) was not achieved, due to the mechanical assembly between the 3 elements (EMI filter, PFC, Capacitor Bank). An essential perspective is to take into account the global mechanical assembly from the initial stages of the optimization process.

Bibliography

[1] "https://www.raspberrypi.org."

[2] "http://www.heros-electronics.com."

[3] Radial Electronics, "Embedded Magnetics Technology Overview," 2012.

[4] M. Ali, E. Labouré, F. Costa, and B. Revol, "Design of a Hybrid Integrated EMC Filter for a DC-DC Power Converter," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4380–4390, 2012.

[5] R. Perrin, B. Allard, C. Buttay, N. Quentin, W. Zhang, R. Burgos, D. Boroyevic, P. Preciat, and D. Martineau, "2 MHz High-Density Integrated Power Supply for Gate Driver in High-Temperature Applications," in *Applied Power Electronics Conference and Exposition*, 2016.

[6] G. Hérault, D. Labrousse, A. Mercier, and S. Lefebvre, "PCB integration of a magnetic component dedicated to a power factor corrector converter," in *PCIM*, 2016.

[7] R. Caillaud, C. Buttay, J. Le Lesle, F. Morel, R. Mrad, N. Degrenne, S. Mollov, and C. Combettes, "High power PCB-embedded inductors based on ferrite powder," in *MiNaPAD*, 2017. [Online]. Available: https://hal.archives-ouvertes.fr/hal-01535727

[8] Oak-Mitsui Technologies, "FaradFlex Ultra Thin Laminates for Higher Performance PCBs, Modules & Chip Packages - Embedded Capacitance."

[9] Fraunhofer IZM, "European competence in electronic packaging."

[10] Schweizer, "Thermal Management of Embedded Power Boards," in *ECPE Workshop "Advances in Thermal Management And Systems For Electronics"*, 2015, p. 26.

[11] W. W. Wits and G. Jan te Riele, “Advances in Heat Pipe Technology for Printed Circuit Boards,” *40th International Conference on Enrironmental Systems*, 2010. [Online]. Available: http://www.sciencedirect.com/science/article/pii/B978008027284950070X

[12] J. D. V. Wyk and F. C. Lee, “On a Future for Power Electronics,” *Journal of emerging and selected topics in power electronics*, vol. 1, no. 2, pp. 59–72, 2013.

[13] S. Seal and H. A. Manthooth, “High Performance Silicon Carbide Power Packaging - Past Trends, Present Practives and Future Directions,” *Energies*, 2017.

[14] J. Popovic-Gerber, “Passive Components Packaging,” in *ECPE Tutorial "Power Electronics Packaging"*, 2015, pp. 1–79.

[15] Advanced Circuit, “www.4pcb.com/media/prepreg-thickness-chart.pdf.”

[16] Isola Group, “Laminate & Prepreg Manufacturing.”

[17] R. S. Khandpur, *Printed Circuit Boards: Design, Fabrication and Assembly*, 2006.

[18] G. Regnat, P.-O. Jeannin, G. Lefevre, J. Ewanchuk, D. Frey, S. Mollov, and J.-P. Ferrieux, “Silicon Carbide Power Chip On Chip Module Based On Embedded Die Technology With Paralleled Dies,” pp. 4913–4919, 2015.

[19] C. Buttay, “Contribution à la conception par la simulation en électronique de puissance : application à l’onduleur basse tension,” Ph.D. dissertation, INSA-Lyon, 2004.

[20] D. Kearney, S. Kicin, E. Bianda, A. Krivda, and D. Bauman, “PCB Embedded Power Electronics for Low Voltage Applications,” in *CIPS*, 2016, pp. 3–8.

[21] V. Bley, Y. Chenjiang, C. Buttay, C. Combettes, and E. Labouré, “Highly integrated power electronic converters using active devices embedded in printed-circuit board,” in *Micro/Nano-Electronics, packaging and assembling, design and manufacturing forum MiNaPAD*, 2015. [Online]. Available: https://hal.archives-ouvertes.fr/hal-01197043

[22] J. Wolf and M. Matthes, “Embedded Component Technology Pioneering solutions,” 2014.

[23] Würth Elektronik, “Embedding Technology: Design Guide.”

[24] AT&S, “Embedded Device Packaging Ramping Up Next Generation SiP,” *JISSO European Council Seminar*, 2011.

[25] L. Böttcher, “Laminate based embedding of power semiconductors: Requirements and technology.”

[26] E. Hoene, “Ultra Low Inductance Package for SiC,” in *PEMC (Power Electronics and EMC)*.

[27] A. B. Sharma, D. Paul, M. Kreck, Y. Rahmoun, P. Anders, M. Gruber, and T. Huesgen, “PCB Embedded Power Package with Reinforced Top-Side Chip Contacts,” in *ESTC 2016*, pp. 1–5.

[28] D. Bortis, D. Neumayr, and J. W. Kolar, “$\eta\rho$ -Pareto Optimization and Comparative Evaluation of Inverter Concepts considered for the GOOGLE Little Box Challenge,” *Control and Modeling for Power Electronics (COMPEL)*, no. Compel, 2016.

[29] Z. Ouyang, “Advances in Planar and Integrated Magnetics,” Ph.D. dissertation, Technical University of Denmark, 2011.

[30] “https://fr.m.wikipedia.org/wiki/Fichier:Planar_core_assembly_exploded.png.”

[31] M. Madsen, A. Knott, M. A. E. Andersen, and A. P. Mynster, “Printed circuit board embedded inductors for very high frequency Switch-Mode Power Supplies,” *2013 IEEE ECCE Asia Downunder - 5th IEEE Annual International Energy Conversion Congress and Exhibition, IEEE ECCE Asia 2013*, 2013.

[32] M. Ali, “Nouvelles Architectures intégrées de filtre CEM Hybride,” Ph.D. dissertation, Ecole National Supérieur de Cachan, 2012.

[33] C. Marxgut, J. Muhlethaler, F. Krismer, and J. W. Kolar, “Multiobjective optimization of ultraflat magnetic components with pcb-integrated core,” *IEEE Transactions on Power Electronics*, vol. 28, no. 7, pp. 3591–3602, 2013.

[34] E. Waffenschmidt, B. Ackermann, and J. A. Ferreira, “Design method and material technologies for passives in printed circuit board embedded circuits,” *IEEE Transactions on Power Electronics*, vol. 20, no. 3, pp. 576–584, 2005.

[35] D. Bang and J. Park, “Ni-Zn ferrite screen printed power inductors for compact DC-DC power converter applications.” *IEEE Transactions on Magnetics*, vol. 45, no. 6, pp. 2762–2765.

[36] M. Ludwig, M. Duffy, T. O'Donnell, P. McCloskey, and S. C. Ómathùna, "Design Study for Ultraflat PCB-Integrated Inductors for Low-Power Conversion Applications," *IEEE Transactions on Magnetics*, vol. 39, no. 5, pp. 3193–3195, 2003.

[37] P. McCloskey, B. Jamieson, and S. Roy, "FORMINGELECTROPLATED INDUCTOR STRUCTURES FOR INTEGRATED CIRCUITS US 2009/0169874 A1," 2009.

[38] Dupont, "Dupon Interra Embedded Passives Materials - Datasheet."

[39] 3M, "3M Embedded Capacitance Material (ECM)," no. July, pp. 4–7, 2017.

[40] H. Chammas, "Embedded Passive Technology," in *STMA International*, 2014.

[41] Ohmega Technologies Inc, *OhmegaPly Product Selection Guide*, 2015.

[42] Ticer Technologies, "http://www.ticertechnologies.com/products/tcr/."

[43] N. Fujimaki, K. Koike, K. Takami, S. Ogata, and H. Linaga, "Development of Printed Circuit Board Technology Embedding Active and Passive Devices for e-Function Module," *Oki Technical Review*, vol. 77, no. 216, 2010.

[44] "IPC-2221B Generic Standard on Printed Board Design, www.ipc.org."

[45] R. Randoll, M. Asef, W. Wondrak, L. Böttcher, and A. Schletz, "Microelectronics Reliability Characteristics and aging of PCB embedded power electronics," *Microelectronics Reliability*, vol. 55, no. 9-10, pp. 1634–1639, 2015. [Online]. Available: http://dx.doi.org/10.1016/j.microrel.2015.06.072

[46] H. Stahr, M. Unger, J. Nicolics, M. Morianz, S. Gross, and L. Böttcher, "Thermal Benchmark of a Classic and Novel Embedded High-Power 3-Phase Inverter Bridge," in *ESTC 2016*, 2016, pp. 1–6.

[47] "https://www.darpa.mil/program/thermal-management-technologies/thermal-ground-plane."

[48] L. A. Liew, C.-y. Lin, R. Lewis, S. Song, Q. Li, R. Yang, and Y. C. Lee, "Flexible Thermal Ground Planes Fabricated With Printed Circuit Board Technology," *Journal of Electronic Packaging*, vol. 139, 2017.

[49] W. W. Wits, "Integrated cooling concepts for printed circuit boards," Ph.D. dissertation, University of Twente, 2008.

[50] Y. Shabany, “Radiation Heat Transfer from Plate-Fin Heat Sinks,” in *24th Annual IEEE Semiconductor Thermal Measurement and Management Symposium (SemiTherm 24)*, 2008.

[51] G. Mostafavi, “Natural Convective Heat Transfer from Interrupted Rectangular Fins,” University of Tehran, 2012.

[52] A. I. Zografos and J. E. Sunderland, “Natural Convection from Pin Fin Arrays,” *Experimental Thermal and Fluid Science*, vol. 3, pp. 440–449, 1990.

[53] F. Frebel, P. Bleus, O. Bomboir, and D. Rixhon, “Transformer-less 2 kW Non Isolated 400 VDC/230 VAC Single Stage Micro Inverter,” 2016.

[54] E. M. Dede, M. Ishigaki, S. N. Joshi, and F. Zhou, “Design for Additive Manufacturing of Wide Band-Gap Power Electronics Components,” in *3D Power Electronics Integration and Manufacturing*, 2016.

[55] Panasonic, “"PGS" Graphite Sheets Datasheet,” 2015.

[56] B. Whitaker, A. Barkley, Z. Cole, B. Passmore, D. Martin, T. R. McNutt, A. B. Lostetter, J. S. Lee, and K. Shiozaki, “A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices,” *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2606–2617, 2014.

[57] J. Le Leslé, “Design, Modeling and Evaluation of an Highly Integrated Bidirectional AC/DC Converter,” Ph.D. dissertation, Ecole Centrale de Lyon, 2019.

[58] J. Le Leslé, R. Caillaud, F. Morel, N. Degrenne, C. Buttay, R. Mrad, C. Vollaire, and S. Mollov, “Volume Optimisation of a bidirectional Interleaved Single-Phase Power Factor Corrector with PCB-Integrated Components,” in *PCIM Europe*, 2018.

[59] J. Le Leslé, R. Caillaud, F. Morel, N. Degrenne, C. Buttay, R. Mrad, C. Vollaire, and S. Mollov, “Optimum Design of a Single-Phase Power Pulsating Buffer (PPB) with PCB-integrated Inductor Technologies,” in *International Conference on Industrial Technology (ICIT)*, 2018.

[60] J. Le Leslé, R. Caillaud, F. Morel, N. Degrenne, C. Buttay, C. Vollaire, and S. Mollov, “Multi-objective optimisation (efficiency vs power density) of a bidirectional single-phase grid connected AC / DC converter (PFC) with two different modulation principles,” in *ECCE*, 2017, pp. 1–8.

[61] M. Ali, E. Laboure, and F. Costa, "Integrated hybrid EMI filter: Study and realization of the active part," *15th European Conference on Power Electronics and Applications, EPE 2013*, 2013.

[62] R. Caillaud, C. Buttay, R. Mrad, J. Le Lesle, F. Morel, N. Degrenne, and S. Mollov, "Comparison of planar and Toroidal PCB integrated inductors for a multi-cellular 3.3 kW PFC." in *IEEE International Workshop On Integrated Power Packaging (IWIPP)*, 2017.

[63] K. Venkatachalam, C. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters," *IEEE Workshop on Computers in Power Electronics*, no. June, pp. 36–41, 2002.

[64] "https://www.mag-inc.com/Products/Powder-Cores/MPP-Cores."

[65] J. Mühlethaler, "Loss Modelling of Magnetic Components," in *ECPE Workshop Innovations in Passive Components for Power Electronics Applications*, 2014.

[66] E. Labouré, *Intégration hybride des dispositifs de l'électronique de puissance*, 2007.

[67] R. Remsburg, *Thermal Design of Electronic Equipment*, 2001.

[68] J. L. Schanen and P. O. Jeannin, "Integration solutions for clean and safe switching of high speed devices," in *Conference on Integrated Power Electronics Systems*, 2018, pp. 1–11.

[69] Analysis Tech, "http://analysistech.com/semiconductor-thermal-tester/phase-12b-thermal-analyzer/."

[70] J. S. De Sousa, P. Fulmek, M. Unger, P. Haumer, and J. Nicolics, "Enhanced Heat Transport in Printed Circuit Boards via Passive Components Embedding," *IMAPS Nordic Conference on Microelectronics Packaging*, pp. 84–89, 2017.

Appendix A

Magnetic Materials Table

Table A.1: Magnetic materials database for Iron Powder materials.

Name	Manufacturer	Maximum Induction (T)	Relative Permeability	Steinmetz Coefficient		
				K	α	β
MPP 14	Magnetics	0.7	14	1.52×10^{-3}	1.38	1.074
MPP 26	Magnetics	0.7	26	8.47×10^{-3}	1.37	2
MPP 60	Magnetics	0.7	60	2.43×10^{-3}	1.37	1.585
MPP 125	Magnetics	0.7	125	1.81×10^{-3}	1.56	2.222
MPP 147	Magnetics	0.7	147	1.81×10^{-3}	1.56	2.222
MPP 160	Magnetics	0.7	160	1.81×10^{-3}	1.56	2.222
MPP 173	Magnetics	0.7	173	1.81×10^{-3}	1.56	2.222
MPP 200	Magnetics	0.7	200	1.96×10^{-3}	1.59	2.322
MPP 300	Magnetics	0.7	300	1.96×10^{-3}	1.59	2.322
MPP 500	Magnetics	0.7	500	2.32×10^{-3}	1.54	1.999
Kool Mu 26	Magnetics	1	26	5×10^{-3}	1.46	2.09
Kool Mu 40	Magnetics	1	40	5×10^{-3}	1.46	2.09
Kool Mu 60	Magnetics	1	60	2.6×10^{-2}	1.29	2.01
Kool Mu 75	Magnetics	1	75	2.6×10^{-2}	1.29	2.01
Kool Mu 90	Magnetics	1	90	2.6×10^{-2}	1.29	2.01
Kool Mu 125	Magnetics	1	125	1.18×10^{-2}	1.63	2.2
High Flux 14	Magnetics	1.4	14	4.42×10^{-2}	1.21	1.386
High Flux 26	Magnetics	1.4	26	4.74×10^{-2}	1.35	2.170
High Flux 40	Magnetics	1.4	40	6.49×10^{-1}	1.14	2.280
High Flux 60	Magnetics	1.4	60	2.43×10^{-3}	1.43	1.585
High Flux 125	Magnetics	1.4	125	2.43×10^{-3}	1.43	1.585
High Flux 147	Magnetics	1.4	147	5.61×10^{-3}	1.52	2.163
High Flux 160	Magnetics	1.4	160	5.61×10^{-3}	1.52	2.163
X Flux 26	Magnetics	1.6	26	1.78×10^{-1}	1.21	1.977
X Flux 60	Magnetics	1.6	60	1.22×10^{-1}	1.19	1.909

Table A.2: Magnetic materials database for Ferrite materials.

Name	Manufacturer	Maximum Induction (T)	Relative Permeability	Steinmetz Coefficient		
				K	α	β
N95	EPCOS	0.41	4400	1.11×10^{-6}	2.069	2.661
PC47	EPCOS	0.42	4250	2.72×10^{-5}	1.790	2.772
N92	EPCOS	0.44	3500	4.50×10^{-5}	1.798	2.875
N97	EPCOS	0.41	4075	5.46×10^{-5}	1.727	2.711
N96	EPCOS	0.41	3150	1.12×10^{-4}	1.727	2.868
N87	EPCOS	0.39	3500	1.85×10^{-4}	1.668	2.868
N88	EPCOS	0.40	3650	2.50×10^{-4}	1.572	2.368
N72	EPCOS	0.37	3340	9.04×10^{-4}	1.567	2.822
N51	EPCOS	0.38	3200	6.90×10^{-3}	1.443	3.140
N27	EPCOS	0.41	4600	8.91×10^{-3}	1.306	2.096
N49	EPCOS	0.40	1700	1.22×10^{-2}	1.357	2.918
N41	EPCOS	0.39	2750	1.29×10^{-2}	1.268	2.045
3C90	FerroxCube	0.47	2300	2.96×10^{-2}	1.222	2.737
3C91	FerroxCube	0.47	3000	4.52×10^{-6}	1.697	1.273
3C92	FerroxCube	0.52	1500	1.84×10^{-8}	2.170	1.078
3C93	FerroxCube	0.50	1800	6.35×10^{-4}	1.322	1.713
3C94	FerroxCube	0.47	2300	6.45×10^{-6}	1.663	1.074
3C95	FerroxCube	0.53	3000	7.51×10^{-7}	1.807	1.100
3C96	FerroxCube	0.50	2000	4.32×10^{-7}	1.907	1.181

FOLIO ADMINISTRATIF

THESE DE L'UNIVERSITE DE LYON OPEREE AU SEIN DE L'INSA LYON

NOM : Caillaud DATE de SOUTENANCE : 17/01/19

Prénoms : Rémy

TITRE : Integration of a 3kW, AC/DC bidirectional converter using printed circuit board embedding technology.

NATURE : Doctorat Numéro d'ordre : 2019LYSEI001

Ecole doctorale : ED 160 / Electronique, Electrotechnique et Automatique

Spécialité : Génie Electrique

RESUME : Les énergies fossiles (Pétrole, Charbon, …) représentent 80 % des énergies consommés. Malheureusement pour l'environnement, elles sont les plus polluantes. Le remplacement actuel des énergies fossiles permet au marché de l'électronique de puissance de grandir d'année en année. L'électronique de puissance permet d'adapter l'énergie électrique à son utilisation finale. Dans la pratique, l'adaptation de l'énergie électrique utilise des convertisseurs. En plus de respecter le volume, l'efficacité et la fiabilité imposés par le cahier des charges pour chaque application, l'électronique de puissance doit aussi permettre de réduire sensiblement les coûts. Le convertisseur doit assurer le fonctionnement électrique du circuit, le support mécanique des composants et la gestion thermique. Le package utilisé par les nouveaux composants à grand gap limite leurs performances. L'intégration des convertisseurs doit développer des méthodes d'interconnexion permettant d'éliminer ce package. L'objectif de la recherche sur l'intégration des convertisseurs est de repousser les limites imposées par un cahier des charges standard tout en assurant ces 3 fonctions principales. Parmi les nombreuses techniques d'intégration, le circuit imprimé (PCB) est mature industriellement, permet la fabrication collective et un assemblage automatisé. L'intégration utilisant le PCB a développé la technique d'enfouissement de puce avec laquelle la puce est directement enfouie dans le PCB sans son package. Cette thèse va étudier la méthode d'enfouissement pour les autres composants nécessaires à la réalisation d'un convertisseur (Condensateurs, Composants Magnétiques). Une optimisation du convertisseur qui doit être réalisé permet de prendre en compte les avantages de cette nouvelle technologie. Un prototype de convertisseur intégré a été réalisé avec des composants utilisant cette technologie.

MOTS-CLÉS : Convertisseur, Intégration, Enfouissement PCB

Laboratoire (s) de recherche : AMPERE

Directeur de thèse: Cyril BUTTAY

Président de jury :

Composition du jury :
- Eckart HOENE (Prof, Fraunhofer-Institut für Zuverlässigkeit und Mikrointegration IZM
- Maeve DUFFY (Lecturer, National University of Ireland Galway)
- Mark JOHNSON (Prof, University of Nottingham)
- Éric LABOURE (Prof, Université Paris Sud - IUT de Cachan)
- Florent MOREL (MCF, Ecole Centrale de Lyon)
- Cyril BUTTAY (CR, INSA-Lyon)