Deep levels characterizations in SiC to optimize high voltage devices

Teng Zhang

To cite this version:

Teng Zhang. Deep levels characterizations in SiC to optimize high voltage devices. Electronics. Université de Lyon, 2018. English. NNT : 2018LYSEI108 . tel-02124529

HAL Id: tel-02124529
https://theses.hal.science/tel-02124529
Submitted on 9 May 2019

N°d'ordre NNT : 2018LYSEI108

THESE de DOCTORAT DE L'UNIVERSITE DE LYON
opérée au sein de
INSA de Lyon

Ecole Doctorale N° ED160
Électronique, Électrotechnique, Automatique

Spécialité de doctorat : Génie Électrique

Soutenue publiquement le 13/12/2018, par :
Teng ZHANG

Caractérisations des défauts profonds du SiC et pour l'optimisation des performances des composants haute tension

---

Devant le jury composé de :

TARTARIN, Jean-Guy	Professeur des Universités	Labo. LAAS	Président
TARTARIN, Jean-Guy	Professeur des Universités	Labo. LAAS	Rapporteur
BI, Jinshun	Professeur des Universités	UCAS, Beijing	Rapporteur
LOCATELLI, Marie-Laure	Chargée de Recherche	Labo. LAPLACE	Examinatrice
JUILLAGUET, Sandrine	Maître de Conférences	Labo. L2C	Examinatrice
PLANSON, Dominique	Professeur des Universités	INSA de Lyon	Directeur de thèse
RAYNAUD, Christophe	Maître de Conférences	INSA de Lyon	Co- encadrant

Département FEDORA – INSA Lyon - Ecoles Doctorales – Quinquennal 2016-2020

SIGLE	ECOLE DOCTORALE	NOM ET COORDONNEES DU RESPONSABLE
CHIMIE	**CHIMIE DE LYON** **http://www.edchimie-lyon.fr** Sec. : Renée EL MELHEM Bât. Blaise PASCAL, 3e étage **secretariat@edchimie-lyon.fr** INSA : R. GOURDON	M. Stéphane DANIELE Institut de recherches sur la catalyse et l'environnement de Lyon IRCELYON-UMR 5256 Équipe CDFA 2 Avenue Albert EINSTEIN 69 626 Villeurbanne CEDEX **directeur@edchimie-lyon.fr**
E.E.A.	**ÉLECTRONIQUE, ÉLECTROTECHNIQUE, AUTOMATIQUE** **http://edeea.ec-lyon.fr** Sec. : M.C. HAVGOUDOUKIAN **ecole-doctorale.eea@ec-lyon.fr**	M. Gérard SCORLETTI École Centrale de Lyon 36 Avenue Guy DE COLLONGUE 69 134 Écully Tél : 04.72.18.60.97 Fax 04.78.43.37.17 **gerard.scorletti@ec-lyon.fr**
E2M2	**ÉVOLUTION, ÉCOSYSTÈME, MICROBIOLOGIE, MODÉLISATION** **http://e2m2.universite-lyon.fr** Sec. : Sylvie ROBERJOT Bât. Atrium, UCB Lyon 1 Tél : 04.72.44.83.62 INSA : H. CHARLES **secretariat.e2m2@univ-lyon1.fr**	M. Philippe NORMAND UMR 5557 Lab. d'Ecologie Microbienne Université Claude Bernard Lyon 1 Bâtiment Mendel 43, boulevard du 11 Novembre 1918 69 622 Villeurbanne CEDEX **philippe.normand@univ-lyon1.fr**
EDISS	**INTERDISCIPLINAIRE SCIENCES-SANTÉ** **http://www.ediss-lyon.fr** Sec. : Sylvie ROBERJOT Bât. Atrium, UCB Lyon 1 Tél : 04.72.44.83.62 INSA : M. LAGARDE **secretariat.ediss@univ-lyon1.fr**	Mme Emmanuelle CANET-SOULAS INSERM U1060, CarMeN lab, Univ. Lyon 1 Bâtiment IMBL 11 Avenue Jean CAPELLE INSA de Lyon 69 621 Villeurbanne Tél : 04.72.68.49.09 Fax : 04.72.68.49.16 **emmanuelle.canet@univ-lyon1.fr**
INFOMATHS	**INFORMATIQUE ET MATHÉMATIQUES** **http://edinfomaths.universite-lyon.fr** Sec. : Renée EL MELHEM Bât. Blaise PASCAL, 3e étage Tél : 04.72.43.80.46 Fax : 04.72.43.16.87 **infomaths@univ-lyon1.fr**	M. Luca ZAMBONI Bât. Braconnier 43 Boulevard du 11 novembre 1918 69 622 Villeurbanne CEDEX Tél : 04.26.23.45.52 **zamboni@maths.univ-lyon1.fr**
Matériaux	**MATÉRIAUX DE LYON** **http://ed34.universite-lyon.fr** Sec. : Marion COMBE Tél : 04.72.43.71.70 Fax : 04.72.43.87.12 Bât. Direction **ed.materiaux@insa-lyon.fr**	M. Jean-Yves BUFFIÈRE INSA de Lyon MATEIS - Bât. Saint-Exupéry 7 Avenue Jean CAPELLE 69 621 Villeurbanne CEDEX Tél : 04.72.43.71.70 Fax : 04.72.43.85.28 **jean-yves.buffiere@insa-lyon.fr**
MEGA	**MÉCANIQUE, ÉNERGÉTIQUE, GÉNIE CIVIL, ACOUSTIQUE** **http://edmega.universite-lyon.fr** Sec. : Marion COMBE Tél : 04.72.43.71.70 Fax : 04.72.43.87.12 Bât. Direction **mega@insa-lyon.fr**	M. Jocelyn BONJOUR INSA de Lyon Laboratoire CETHIL Bâtiment Sadi-Carnot 9, rue de la Physique 69 621 Villeurbanne CEDEX **jocelyn.bonjour@insa-lyon.fr**
ScSo	**ScSo*** **http://ed483.univ-lyon2.fr** Sec. : Viviane POLSINELLI Brigitte DUBOIS INSA : J.Y. TOUSSAINT Tél : 04.78.69.72.76 **viviane.polsinelli@univ-lyon2.fr**	M. Christian MONTES Université Lyon 2 86 Rue Pasteur 69 365 Lyon CEDEX 07 **christian.montes@univ-lyon2.fr**

*ScSo : Histoire, Géographie, Aménagement, Urbanisme, Archéologie, Science politique, Sociologie, Anthropologie

Acknowledgement

Sincere appreciation to my advisors Christophe Raynaud and Dominique Planson, as huge hints along with precious guidance and support have been provided which help me to unlock the door to the physics throughout these 3 years of my PhD study that is worshipful.

In addition, I'd like to acknowledge my dear colleges in laboratory Ampère, INSA who helped a lot: R. Caillaud, S. O. Avino, S. Niu, B. Asllani, M. Beye el al., as well as enlightening professors such as B. Allard and G. Bermond. Thanks to my friends of China namely B. Yu, C. Zhou, X. Wang, B. Cuan, X. Jiang, C. Xu, X. Zhu, Y. MA, F. Liu, Y. Li et al. as well for the skylark.

Remarkable acknowledgment to the Labo Ampère, INSA de Lyon, and the CSC also quenching any menace from the "rear" that could come across to me: from delicious menu I appreciate a lot, basic funding for the comfortable lives, to the well-designed curriculum enlarging my knowledge about the fundamental modern theory and keeping my brain CPU lighting for overcoming those struggles that block the road to scientific accomplishment.

At last, I would like to give my sincere and special to my family for supporting the journey for studying in France, the one that had been attracting me a lot, and this footmark I left in Lyon and INSA is so glittering that will never come to the ennui.

Abstract

Due to the increasing appeal to the high voltage, high temperature and high frequency applications, Silicon Carbide (SiC) is continuing attracting world's attention as one of the most competitive candidate for replacing silicon in power electric field. Meanwhile, it is important to characterize the defects in semiconductors and to investigate their influences on power devices since they are directly linked to the carrier lifetime. Moreover, reliability that is also affected by defects becomes an unavoidable issue now in power electrics.

Defects, including point defects and extended defects, can introduce additional energy levels in the bandgap of SiC due to various metallic impurities such as Ti, Fe or intrinsic defects (vacancies, interstitial…) of the cristalline lattice itself. As one of the widely used defect characterization method, Deep Level Transient Spectroscopy (DLTS) is superior in determining the activation energy E_A, capture cross section σ and defect concentration N_T as well as the defect profile in the depletion region thanks to its diverse testing modes and advanced numerical analysis.

Determination of Schottky Barrier Height (SBH) has been confusing for long time. Apart from experimental measurement according to I-V or C-V characteristics, various models from Gaussian distribution of SBH to potential fluctuation model have been put forward. Now it was found that these models are connected with the help of flat-band barrier height Φ_{BF}. The Richardson plot based on Φ_{BF} along with the potential fluctuation model becomes a powerful tool for SBH characterization. SBHs with different metal contacts were characterized, and the diodes with multi-barrier are verified by different models.

Electron traps in SiC were studied in Schottky and PiN diodes, while hole traps were investigated under strong injection conditions in PiN diodes. 9 electron traps and 4 hole traps have been found in our samples of 4H-SiC. A linear relationship between the extracted E_A and log(σ) indicates the existence of the intrinsic temperature of each defects. However, no obvious difference has been found related to either barrier inhomogeneity or contact metal. Furthermore, the electron traps near interface and fixed positive charges in the oxide layer were investigated on SiC power MOSFETs by High Temperature Gate Bias (HTGB) and Total Ionizing Dose (TID) caused by irradiation. An HTGB-assist-TID model was established in order to explain the synergetic effect.

Two carrier freeze-out regions were found near 40 K and 100 K that will degenerate the accuracy of traditional capacitance DLTS test. Meanwhile, concentration of certain defects can be reduced by high temperature annealing, that is also a cause to the multi-barrier effect. Special attentions were paid on defects with tiny activation energy at extremely low temperature as well as the abnormal DLTS signal caused by negative-U centers. Irregular switch on DLTS transient (i.e. between capture and emission) is found related to width of detection zone in depletion region.

Future works are mainly focused on interface characterization as well as improvement on trapping models at low temperature. In addition, the stress effect especially introduced by the characterization method should be paid attention as well.

List of figures

List of tables

List of symbols

A	Richardson constant / Amplitude of transient
A^*	Effective Richardson constant
B	Offset during transient
C	Capacitance
$C(t)$	Capacitance as a function of time
$C'(t)$	Capacitance as a function of time after the second pulse of DDLTS
ΔC	Amplitude of capacitance transient
ΔC_i	Amplitude of individual capacitance transient
C_0	Capacitance before transient
C_{iss}	Input capacitance of MOSFET
C_R	Capacitance at reverse bias
D^+	Positive charge state
D^-	Negative charge state
D^0	Neutral charge state
D_n	Diffusion constant of electron
D_S	Interface states density
$\mathcal{E}$	Electric field
E_a	Activation energy
$\mathcal{E}_B$	Breakdown field
E_C	Energy level of conduction band
E_F	Fermi level
E_F^m	Fermi level in the metal
E_F^s	Fermi level in the semiconductor
E_g	Energy gap between conduction band and valence band
E_g^{eff}	Measured effective forbidden band gap
$E_g(0)$	Energy gap between conduction band and valence band at 0 K
E_V	Energy level of valence band
F_n	Discrete Fourier Transform
$\mathcal{E}_i$	Electric field between metal and semiconductor
$\mathcal{E}_{\max}$	Maximum electric field over the barrier
$\mathcal{E}_S$	Surface electric field
E_T	Energy level of trap
I	Current

$I(t)$	Current as a function of time
I_0	Saturation current of p-n junction
I_{dss}	Drain-source leakage current of MOSFET
I_{gss}	Gate leakage current of MOSFET
I_R	Current at reverse bias
I_s	Saturation current of SBD
J	Current density
J_0	Saturation current density of rectifier
J_{ms}	Current density from metal to semiconductor
J_r	Recombination current density
J_{sm}	Current density from semiconductor to metal
J_{te}	Current density according to thermal emission theory
L	Distance intersection Fermi level and trap level
N	Number of sampling values
N_C	Electron effective density of states
N_A	Doping concentration of acceptor
N_D	Doping concentration of donor
N_S	Shallow doping concentration
N_T	Trap concentration
Q_d	Net positive charge in the semiconductor
Q_m	Negative charge on the surface of metal
Q_{ss}	Net positive charge due to interface state
R_{on}	On-resistance
R_S	Series resistance
S	Effective surface
S_i	Effective surface of region i.
T	Temperature
T_0	Parameter involved in T_0 effect
T_P	Pulse width in DLTS
T_W	Period width in DLTS
U	Energy between donor and acceptor level in negative-U system
U_r	Recombination ratio
U_H	Pulse height in DLTS
U_P	Pulse voltage in DLTS
U'_P	Second pulse voltage in DDLTS

U_R	Reverse bias in DLTS
V	Bias voltage
V_B	Breakdown voltage
V_d	Difference between Φ_B and ξ
V_{d0}	Difference between Φ_B and ξ at balance condition
V_{ds}	Drain-source voltage
V_{gs}	Gate-source voltage
V_I	Intersection with x-axis of $1/C^2 \sim V_r$ plot during C-V analysis
V_i	Voltage drop between metal and semiconductor if electrically connected
V_r	Reverse bias voltage
V_{th}	Gate threshold voltage of MOSFET
X_n	Entropy factor during emission process
a_i	Fraction of effective surface of individual region with total contact surface
a_n	Cosine coefficient of Fourier transform
b_n	Sine coefficient of Fourier transform
c_1	Electron capture rate between trap level and conduction band
c_2	Electron capture rate between trap level and valence band
c_n	Electron capture rate / Complex Fourier coefficient
c_n^D	Discrete Fourier coefficients
d	Distance where the barrier falls by a value of kT/q from its maximum
e^-	Electron
e_1	Electron emission rate between trap level and conduction band
e_2	Electron emission rate between trap level and valence band
e_n	Electron emission rate
$f(t)$	Continuous function of time
f_k	Discrete sampling value
h	Planck constant
k	Boltzmann constant
l	Carrier mean free path
m	Free electron mass
m^*	Electron effective mass
n	Electron concentration / Ideality factor
n_0	Concentration of free electrons
n_i	Electron concentration in intrinsic semiconductor
n_{Tc}	Filled traps during the capture process

n_{Te}	Filled traps during the emission process
p	Hole concentration
p_t	Tunneling probability
q	Magnitude of the electron charge
t_0	Time between end of charging pulse and the first sampling value
$\bar{v}$	Average thermal velocity
v_{th}	Thermal velocity of carrier
$v_{th,n}$	Thermal velocity of electrons
v_S	Saturation drift velocity
w	Depletion region width
w_{eff}	Effective depletion region width where traps can be detected by DLTS
w_P	Depletion region width at pulse voltage
w_R	Depletion region width at reverse bias
x_m	Position where the maximum value of Schottky potential height is reached
Φ_B	Schottky barrier height
$\bar{\Phi}_B$	Average of Schottky barrier height
$\bar{\Phi}'_{B0}$	Calculated average of SBH based on Φ_{BF} and ρ_2
Φ_{B0}	Schottky barrier height at zero bias
$\bar{\Phi}_{B0}$	Average of Schottky barrier height at zero bias
Φ_{BF}	Schottky barrier height on flat-band condition
$\Phi_{Bn,i}$	Individual constant barrier height of a series of ideal regions
$\Phi_{Bn,l}$	Individual constant barrier with the lowest barrier height
Φ_B^{eff}	Effective Schottky barrier height involving image-force lowering
Φ_{C-V}	Schottky barrier height determined by C-V
$\Delta\Phi_i$	Reduction on barrier height due to image-force lowering
Φ_m	Work function of metal
Φ_s	Work function of semiconductor
α	Effective tunneling constant
β	Temperature coefficient of band gap
χ_s	Electron affinity of semiconductor
δ	Distance between metal and semiconductor
ε_0	Permittivity in the vacuum
ε_i	Permittivity of the interfacial layer
ε_{ir}	Relative permittivity of the interfacial layer
ε_s	Permittivity of the semiconductor

ε_s'	Permittivity of the semiconductor under high frequency
ϕ_0	Neutral level of interface states
γ	Temperature coefficient of saturation current in p-n junction
μ	Carrier mobility
μ_n	Electron mobility
ρ_2	Linearity coefficient of $\bar{\Phi}_B$ varies with bias voltage
ρ_3	Linearity coefficient of σ_S varies with bias voltage
σ	Capture cross section
σ_n	Capture cross section of electrons
σ_p	Capture cross section of holes
σ_S	Standard deviation in Gaussian distribution
σ_S'	Calculated standard deviation in Gaussian distribution based on Φ_{BF} and ρ_3
σ_{S0}	Standard deviation in Gaussian distribution at zero bias
τ	Time constant
τ_c	Capture time constant
τ_e	Emission time constant
τ_r	Carrier lifetime within the depletion region
ω_0	Angular velocity involved in Fourier transform
ξ	Difference between E_F and E_C
ψ	Constant parameter in the expression of saturation current of p-n junction

Table of contents

Introduction

Silicon carbide, as one of the well-known potential substitute materials of silicon in power electrics, has been attracting attention due to its high temperature, high power, and high frequency applications. The mature on large size of SiC wafer as well as cutting process bring hope to the commercial massive production, which in turn speeds up the research on SiC as the material of new generation.

Reliability is another vital issue throughout the practical application of power devices, and its importance has becoming more and more prominent. As a consequence, studying the failure mechanism and maintaining high performance of devices especially under harsh environment such as space application have turned into a significant branch of power electrics.

The crystal models are widely studied as a fundamental basis in semiconductor research. However, it is never possible to find perfect crystal in nature. As all materials are tangible with finite volume, the periodical array of atoms will be destroyed at the boundary which leads to large friction of broken bonds near material surface. In addition, other things such as impurities or stress that occur during the growth or formation of the crystal can contribute to the departure from the perfect crystal as well. Furthermore, the process of device fabrication (cutting, polishing, doping, etching etc.) will also introduce the defect in the semiconductor crystal with no doubt. Defects can not only result in degradation on performance of power semiconductor devices, but could also lead to the destruction under certain circumstances. On top of that, the impact on those optical devices such as LED chips due to defects should not be ignored. Since those defects and the related trap levels are inevitable, the improvements on the semiconductor process technology have never stopped in order to get rid of the disadvantages as much as possible. On the other hand, doping is one of the most widely used technologies for changing the conductivity by modifying the free carrier concentration. Moreover, carrier life time has to be carefully controlled in some bipolar devices though introduced trap levels as recombination centers. Therefore, it is significant to make use of imperfect crystal and study the effects due to the trap levels.

This work mainly focuses on the investigation of deep levels in the 4H-SiC power devices, especially their influence on Schottky barrier height. The thesis is organized as follows.

Chapter 1 gives a brief introduction on development of wide band gap SiC power devices as well as the multi-barrier effect discovered in those Schottky barriers. Meanwhile, the classification of defects is discussed and a review is given on those defects reported in 4H-SiC with DLTS measurement

Chapter 2 is an introduction of Schottky contact, including the basic structure, current transportation mechanisms, determination and measurement of barrier height. A review on different models related is given and their relationships are discussed as well as those models on barrier height inhomogeneity.

Chapter 3 focuses on deep levels detection, especially on behalf of DLTS measurement. After a review on basic theory of capture, emission and transient due to trap levels, DLTS principle is mainly introduced as well as either different category of DLTS or their optimizations.

Chapter 4 is dedicated to the experimental results on SiC Schottky diodes with either static measurements (I-V and C-V) or DLTS test within wide temperature range. Following a typical case study of Ti/W SBD, the comparison on both single/multi barrier diodes and SBDs with different metal contact is presented. Furthermore, the evolution of barrier height on Ti/W sputtering sample is discussed.

Chapter 5 provides the study on PiN diodes as well as the influence of irradiation on MOSFETs. Some effects revealed during the experiments are discussed such as freeze-out and annealing on high temperature. The behavior at extremely low temperature is explored as well.

Chapter 6 is the conclusion and perspective.

Chapter 1
Start of art

1.1 Background

1.1.1 Development of modern power electronics and its limitation

After invention of the first transistor fabricated with germanium in 1947, Ge had been considered as the most useful material for semiconductor technology the following decade until 1960s, when Silicon replaced germanium thanks to its superior thermal stability, reliable oxide and abundance [1]. From then on, the semiconductor industry has been entering a golden, not only specifically in the evolution on integrated circuit which influences everywhere in our daily lives, but also in the various inventions of power devices such as PiN diode, Vertical Diffused Metal Oxide Semiconductor Field Effect Transistor (VDMOS), Insulated-Gate Bipolar Transistor (IGBT) and their derivatives.

Even though nowadays most of the commercial power semiconductor devices such as VDMOSs or IGBTs are silicon-based, the performance of these Si devices is facing their limitation in power applications owing to the material properties. As an example, the well-known 'silicon limit' that describes the relationship for high power MOSFET between the on-resistance R_{on} and its breakdown voltage V_B can be presented as: [2]

$$R_{on} = 5.93\times10^{-9}V_B^{2.5} \tag{1.1}$$

Therefore the R_{on} will increase dramatically at high voltage application, which is always the problem when it comes to the unipolar device like Schottky diode. Even if this drawback can be overcame by either bipolar device such as IGBT or special structure like Super Junction, the storage of minority carriers in bipolar devices as well as the complicate manufacturing process of novel structure should still be challenging. As a result, it is significant to turn to those new generation after-silicon materials.

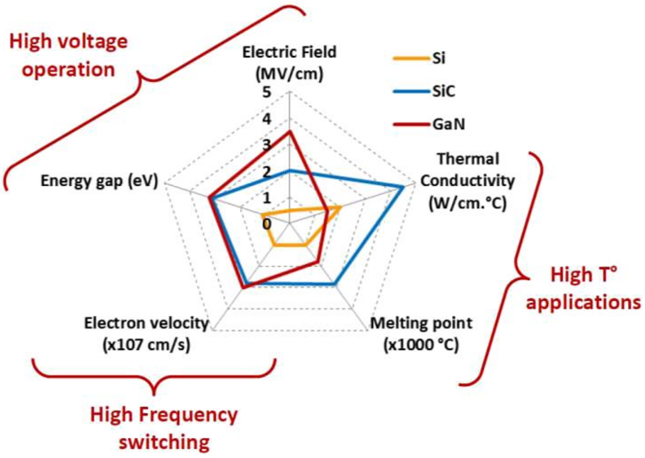


Figure 1.1. Comparison of material properties of Si, SiC and GaN [3].

As shown in Figure 1.1, the breakthrough of wide bandgap semiconductor material made by silicon carbide (SiC) and gallium nitride (CaN) brings hope for the development of a new generation of power electronics thanks to their superior characteristics relate to high power application compared to silicon. And these new generation materials have been attracting more and more attentions in the power field.

1.1.2 Silicon carbide (SiC)

Silicon carbide, as was first discovered by Jons Jakob Berzelius in 1824 [4], is one of the attractive semiconductors for high temperature, high power, and high frequency application [5]. The commercial value of SiC has been discovered early days such as abrasive, high-temperature ceramics and fireproofing thanks to its advantages in either hardness or melting characteristics [6]. Soon it has emerged as the most mature of the wide-bandgap semiconductors since the release of commercial 6H-SiC bulk substrates in 1991 and 4H-SiC substrates in 1994 [7]. As is shown in Table 1.1, SiC is superior to Si especially for power device application due to its large bandgap, high breakdown field and high thermal conductivity. As a result, the SiC devices can benefit from higher blocking voltage, lower on-resistance, reduced leakage current and higher operation temperature/frequency compared to that made by Si. Therefore, silicon carbide is an ideal alternative to silicon for devices over 10 kV, as shown in Figure 1.2. A great deal of SiC devices with ultra-high breakdown voltage have been reported such as 15~20 kV 4H-SiC IGBTs [8] and 20 kV 4H-SiC gate turn-off thyristors [9].

Table 1.1. Main Physical Properties of 3C-, 6H-, 4H-SiC, and Si [10, 11].

Properties	3C-SiC	6H-SiC	4H-SiC	Si
Energy gap: $E_g(eV)$	2.4	3.0	3.2	1.12
Electron mobility: $\mu_n(cm^2/V_S)$	1000	500	1000	1350
Breakdown field: $\mathcal{E}_B(V/cm)\times10^6$	2	2.5	2.2	0.25
Thermal conductivity $(W/cm°C)$	5	5	5	1.5
Saturation drift velocity: $v_S(cm/s)\times10^7$	2.5	2	2	1
Maximum operating temperature $(°C)$	1240	1240	1240	300

The crystal lattice of SiC is recognized as closely packed silicon-carbon bilayers (or Si-C double layers), which can be regarded as the alternately arranged planar sheets of silicon or carbon atoms. Due to the variation of stacking sequences, different polytypes can be presented. Among over 150 polytypes found in SiC, however, only the 6H- and 4H-SiC polytypes are commercially available in both bulk wafers and custom epitaxial layers. Between the two polytypes, 4H-SiC is preferred for power devices primarily because of its high carrier mobility, particularly in c-axis direction and its low dopant ionization energy [12].

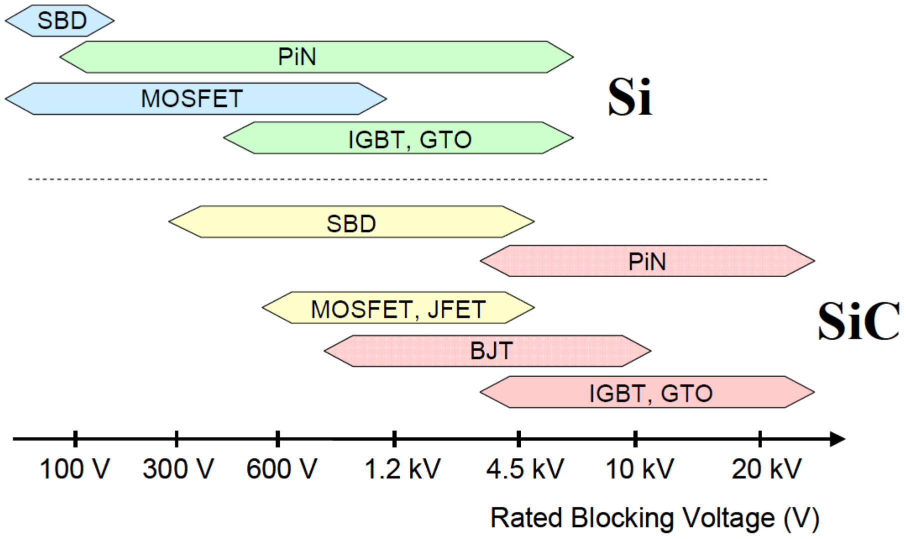


Figure 1.2. Major territories of individual unipolar and bipolar power devices for Si and SiC in terms of the rated blocking voltage [13].

Apart from those breakthroughs reported from the laboratories, as listed in Table 1.2, lots of commercial SiC power devices are now available on thousand volt class with reduced on-resistance compared to Si devices. With the development on breakthrough of SiC wafer fabrication and maturity of the process, SiC devices will continue to expend their influences in power field.

Table 1.2. The maximum blocking voltage available for some commercial high power SiC devices and their fabricants. Information is updated to August 2018.

SiC device	Blocking voltage	Typical Fabricants
MOSFET	1.7 kV	Cree, GeneSiC, IXYS, Microsemi, Rohm
SBD	1.7 kV	Cree, Microsemi
Thyristors	6.5 kV	GeneSiC
IGBT	600 V	IXYS
PiN Diode	15 kV	GeneSiC

1.1.3 Schottky barrier diodes (SBD)

SiC p-n junctions could suffer a higher forward power loss compared to Si due to its higher built-in voltage. However, this can be avoided by a Schottky structure [14]. Nowadays, the 4H-SiC Schottky-barrier diodes (SBDs) have already shown much attraction in power systems because of their low conduction loss, fast switching speed and high operating temperature [15]. Junction Barrier Schottky (JBS) diode is another significant family of SiC power devices which consist of an interconnected grid of p-type regions in the n-type drift layer. As a result, JBS combine the advantages of both SBD and PiN diode and are wildly used in various fields such as power supplies, aerospace power systems, high-performance communication systems, and power conversion systems [16].

Both the electric and dielectric properties of the Schottky Barrier Diodes (SBDs) are dependent on various factors. The most effective of them among interface states are the impurity, the thickness and homogeneity of interfacial layer and barrier height (BH) at M/S interface [17].

1.1.4 Multi-barrier in SBD

During the characterization of Shottky diodes in our laboratory, a double barrier phenomenon has been discovered, which can be identified as abnormal high current under low forward bias, as is shown in Figure 1.3. This has shown up not only among different metals such as Ni, Ti/W, Mo, but also in various metal processes like sputtering or lift-off.

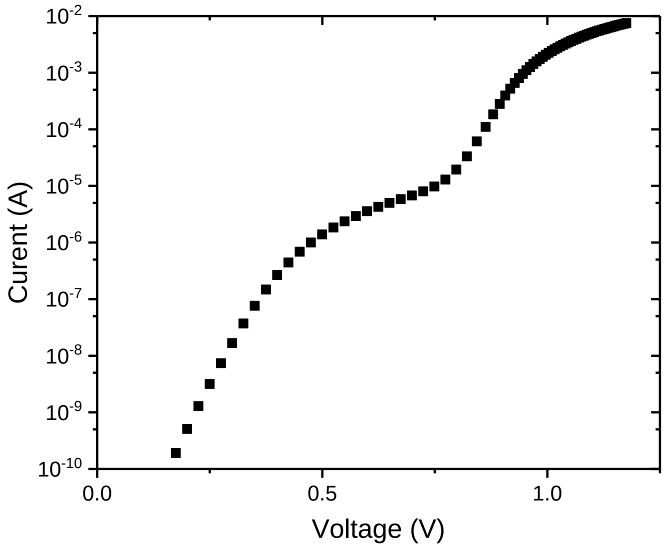


Figure 1.3. Double barrier phenomenon in Schottky diode.

Similar phenomenons have been reported, and it was highlighted that these ‘non-ideal’ diodes occurred regardless of growth technique, pre-deposition cleaning method, or contact metal [18]. Moreover, this double barrier was found to be more common at lower temperature, as shown in Figure 1.4, which was explained by barrier height inhomogeneities [19].

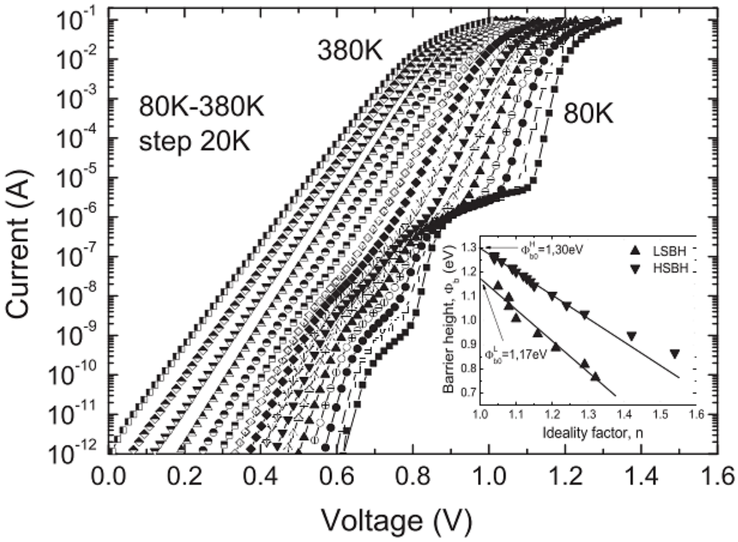


Figure 1.4. Temperature dependence of forward I-V characteristics for 4H-SiC rectifier reported in [19].

As widely reported, the multi-barrier phenomenon should have an origin in common, and those invisible deep levels that can greatly influence the device performance are one of the most possible contributions to this.

1.2 Reliability and Defects

Defects and impurities in semiconducting materials can result in poorer property such as a carrier lifetime reduction [20]. Especially those deep level defects, which are close to midgap, can be efficient recombination centers or carrier traps. Meanwhile, charged interface traps directly affect the device performance by increasing the threshold voltage, degrading the channel mobility and causing leakage current for MOS applications [21]. On the other hand, trap levels can be sometimes important for carrier lifetime adjustment as well as in the application of LEDs. These deep level defects can not only be caused by irradiation [22] or impurities such as Ti, V, Cr [23] but also be intrinsic defects introduced by manufacturing process such as carbon vacancy (V_C) [24, 25]. Activation Energy (E_a), capture cross section (σ) and defect concentration (N_T) are all significant parameters for deep level defects identification.

1.2.1 Classification of defects

1.2.11 Forms of defects

According to different forms in semiconductor, defects can be simply classified as point defects and extended defects, while extended defects includes various of defect types based on their dimension and characteristics, one example is listed in Table 1.3.

Table 1.3. Classification on defects in crystals.

Dimension	Defect type	Examples
0	Point defects	Vacancies Interstitial defects Substitutional defects Frenkel defects
1	Line defects	Edge dislocations Screw dislocations
2	Planar defects	Stacking faults Twins Grain boundaries Surface defects
3	Volume defects	Precipitates (Cluster) Voids

Some common defects are explained as follows:

❖ Vacancies

A vacancy, one of the simplest point defect also known as a Schottky defect [26], comes from the absence of an atom in the lattice [27], while the missing usually takes place in pairs in those ionic crystals (e.g. the alkali halide crystals) to maintain charge balance [28]. Irradiation is regarded as a common way to introduce vacancies by using various particles (electrons, protons, neutron or even He^+) with wide energy range [29-32], and part of them can be annealed at high temperature [33-35]. On the other hand, secondary defects can be produced after annealing at 400 ℃ [35] and the agglomeration of defects to larger vacancy complexes has been reported as well [36, 37].

❖ Substitutional defects

Substitutional defects stand for the replacement of original atom by an impurity such as the doping process of semiconductor that usually contributes to introducing shallow levels in the bandgap. This normally refers to those atoms of either original ones or impurities that have the comparable size (e.g. N or Al in SiC or Si), otherwise the interstitial defects will be formed.

❖ Interstitial and Frenkel defects

If the gap of lattice is occupied where no atom should exist, this type of defect is known as interstitial. Another possibility is the share of one lattice site by two or more atoms. Frenkel defects can be regarded as the combination of both an interstitial atom and related vacancies caused by lattice atoms.

❖ Dislocations

As a common example of extended defects, dislocation stands for the bending of atom planes surrounding due to the termination of the atom plane in the crystal. It was first put forward by Volterra in 1970 [38], and can be classified as screw dislocation or edge dislocation according to different types. By studying the dislocations parallel to the Schottky contact, FIGIELS has discussed that the kinetics of electron emission from dislocation will be drastically modified due to the configuration entropy. As a consequence, the Deep Level Transient Spectroscopy (DLTS) transients no longer follow the exponential law and results in the broadening of DLTS signal [39].

❖ Stacking faults

Stacking faults refer to the locally changed stacking order of atom layer(s) in the structure. For example, instead of the typical stacking sequence ABCABCABC of face-centered cubic (fcc) structure, the structure with stacking fault may be ABCABABCAB. Furthermore, the correlation between stacking faults and double barrier phenomenon has been reported [40].

❖ Surface defects

Surface defect is another significant category of defect. Generally speaking, surface defects do not refer to the specific defect type as discussed before, but focus on the position where large fraction of dialing bond occur and the periodic of lattice is destroyed. As a result, the carrier lifetime, mobility etc. can be affected near the surface. In addition, similar defects can lie in the interface between semiconductor and metal/oxide and is recognized as interface states, which can be the decisive factor of Schottky barrier height under certain circumstance instead of the metal type.

1.2.12 Shallow and deep levels

Apart from the classification of defects according to their forms or crystal condition, defects can also be classified as shallow or deep defects based on the location of their energy levels in the bandgap of the semiconductor. A defect level is regarded as shallow level if its energy level is located near the band edges (conduction or valence band) of the semiconductor. One of the most common shallow levels is those impurities introduced by doping, which directly modifies the electrical properties (conductivity, carrier mobility etc.) of the semiconductors. In addition to impurities that usually take place as substitutions, the interstitial atoms that contribute to shallow levels have been reported as well [41, 42].

On the other hand, generally the deep levels have less contribution to conduction compared with the shallow levels of dopants due to their relatively low concentration and large activation energy. However, these deep levels can play an important role in the recombination process and are regarded as a significant limitation on carrier lifetime especially when the energy levels lie near the middle of the bandgap. As one of the applications, it is possible to release the carrier storage effect by limiting carrier life time with the help of recombination center introduced by Au impurities in silicon devices, since Au is known as a lifetime killer in silicon [43].

1.2.2 Defects reported in SiC devices

Since 1990s, a great deal of researches about deep level defects in SiC has been done with the help of DLTS or other investigation methods. The donor deep levels with almost full range of activation energy have been reported, as is shown in Figure 1.5. Obviously, these deep levels focus on activation energy from 0.1 eV to 0.9 eV, including the well-known $Z_{1/2}$ defect with E_a around 0.68 eV.

Various of impurity defects have been investigated by means of doping or implantation [44, 45], part of them found in 4H-SiC are illustrated in Table 1.4. Other impurity defects such as O and Er have been reported in 6H-SiC [46, 47].

Recently, more attention has been payed on characteristic of deep level defects and its relation to device properties. Danno and Kimoto have pointed out the similarity between $Z_{1/2}$ and $EH_{6/7}$ (with E_a around 1.6 eV) due to the fact that the concentration of $Z_{1/2}$ and $EH_{6/7}$ have the same trend regardless of As-growth, irradiation or annealing. They believe both centers contain the same defect such as a carbon vacancy [48]. As the two dominant electron traps, $Z_{1/2}$ and $EH_{6/7}$ could both survive after high temperature annealing at 1700 ℃ [49]. However, Klein argued that $Z_{1/2}$ acted alone as the lifetime limiting defect [50]. By comparing the concentration of carbon vacancy (V_C) determined by electron paramagnetic resonance with that of $Z_{1/2}$ defect obtained by C-V and DLTS, Kawahara argued that the $Z_{1/2}$ originates from V_C [51], similar conclusion has been drawn in [52].

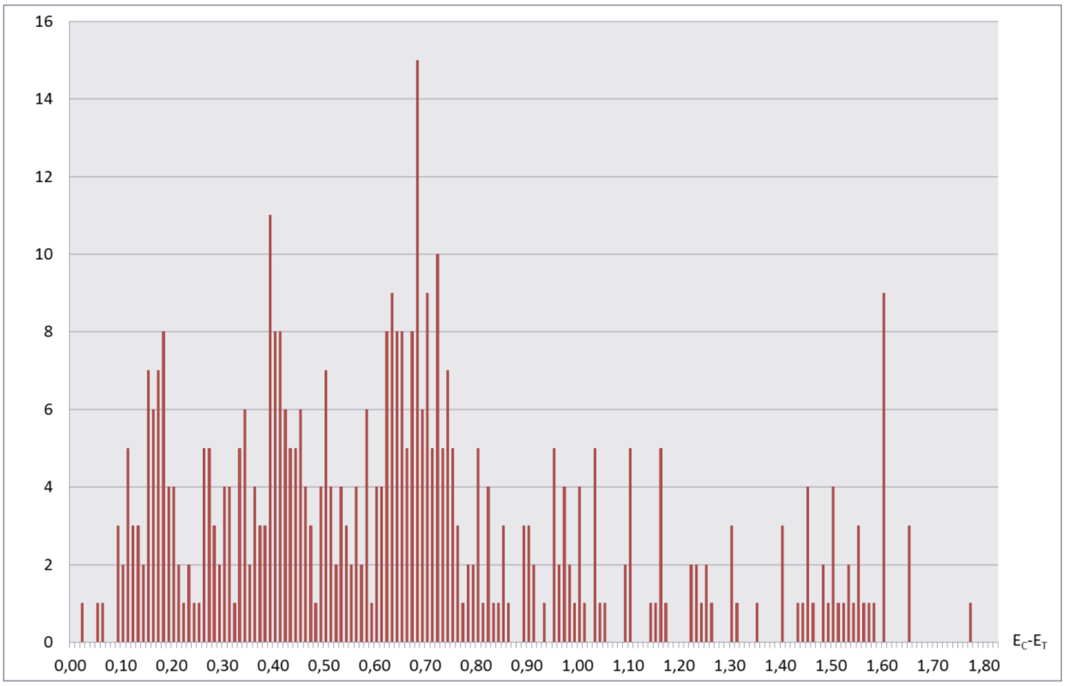


Figure 1.5. Number of articles which report defects with certain activation energy $(E_C - E_T)$ *in 4H-SiC.*

Meanwhile, several effects have been put forward as

- Poole-Frenkel Effect: The strong electric field close to the metal-semiconductor interface enhances the emission rate by lowering the potential barrier over which the carrier is thermally emitted. Therefore, increased applied electric field should lead to lower activation energy [53].
- Carrier Freeze-out Effect: Strong compensation of the dopant and the high concentration of radiation-induced defects takes place at low temperature [54].
- Lambda Effect (λ Effect): When measuring the deep levels in semiconductor diodes, the transition zone near the edge of the space charge region (SCR) owing to the extended Debye tail of free carriers from the neutral material should be taken into consideration. Particularly, this width of correction λ should be further modified in non-steady state [55].

In addition, certain traps are invisible to the measurements that should be paid attention as well. In particular, in the certain region near surface, electrons are not captured by the traps during the filling pulse. Whereas near the opposite edge of a depletion layer, electrons in the deep level located below the Fermi level even when the reverse bias is applied can be always trapped without emission [56].

On the other hand, the correlation between the observation of the two barrier height behavior in the I-V characteristics and traps measured from DLTS and Random Telegraph Signal (RTS) dates back to year 2002 [57]. It was pointed out that the I-V characteristics tended to degrade with increasing deep-level concentration and those inhomogeneous diodes tended to contain defect clusters, which can lead to a local Fermi-level pinning [18]. Gelczuk also argued that traps partially are responsible for the observed barrier height inhomogeneities [19].

Table 1.4. Several defects reported in 4H-SiC.

Defects	$E_a = E_C - E_T \ (eV)$	$\sigma \ (cm^2)$	$N_T \ (cm^{-3})$	Reference
Ti	0.13	7×10^{-15}	3.66×10^{10}	[45, 58, 59]
	0.17	1×10^{-15}	1.17×10^{11}	
Cr	0.15	2×10^{-15}	1.4×10^{13}	[45, 58, 60-62]
	0.18	8×10^{-16}	1.3×10^{13}	
	0.74	2×10^{-15}	\	
V	0.80	1.79×10^{-16}	3×10^{17}	[63]
	0.89	\	$< 1 \times 10^{14}$	[62]
	0.97	6×10^{-15}	\	[45, 58, 59]
Fe	0.39	2×10^{-15}	7.6×10^{12}	[64]
Ta	0.68	8×10^{-15}	\	[65]
Intrinsic	0.56	5×10^{-17}	\	[56]
	0.62	\	1.2×10^{15}	[49, 62]
	0.66	1.31×10^{-14}	\	[50, 66-68]
	0.68	7×10^{-15}	1×10^{13}	[69-71]
	0.72	2×10^{-14}	9.5×10^{14}	[48]

Chapter 2
Barrier height determination of Schottky diodes

2.1 Energy band diagram and formation of Schottky barrier diode

2.1.1 Ideal Schottky contact

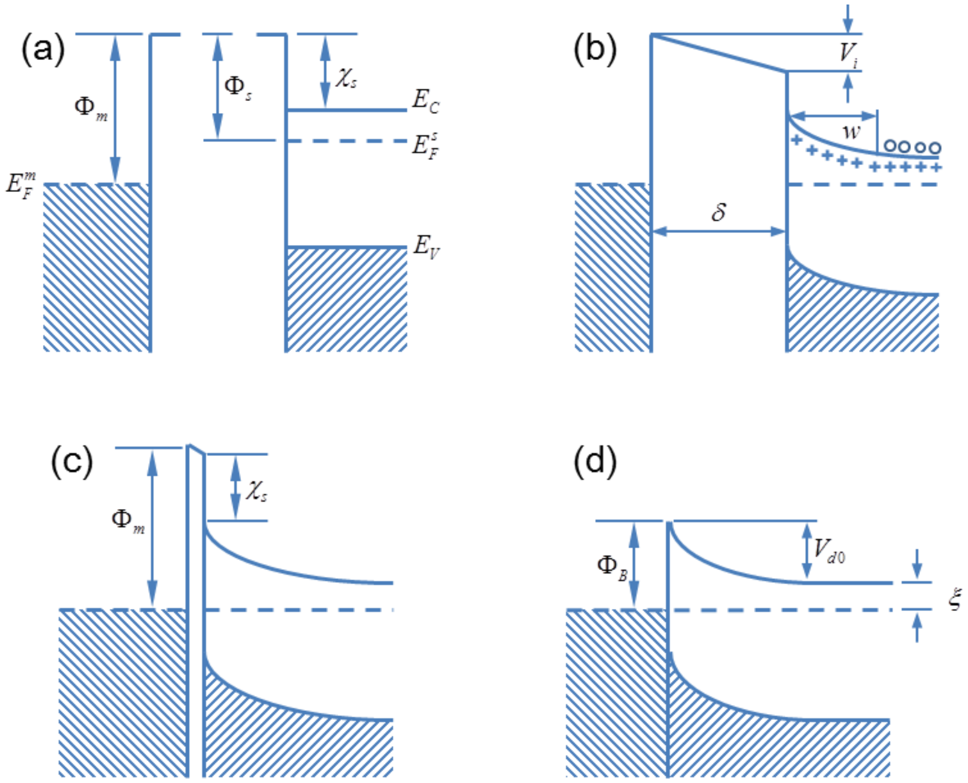


Figure 2.1. Formation of an ideal Schottky barrier between a metal and an n-type semiconductor (a) neutral and isolated, (b) electrically connected by a wire, (c) separated by a narrow gap, (d) in perfect contact. Cross and circle marks in (b) denote donor ion and electron in conduction band respectively.

Consider an n-type semiconductor with a work function Φ_s less than that of the metal Φ_m, as shown in Figure 2.1(a). In this case, electrons will transfer from semiconductor to metal if they are connected by using a wire, and eventually the Fermi level in both metal and semiconductor would be consistent with uncompensated donor charge left near interface which leads to band bending and formation of a depletion layer as shown in Figure 2.1(b). Since the electron affinity of semiconductor χ_s does not change, the difference of work function between metal and semiconductor falls on the voltage drop V_i between them, as presented by $V_i = \delta \mathcal{E}_i$ if we assume the electric field $\mathcal{E}_i$ between two materials keeps constant, and the depletion layer near interface. As a result, the band bending becomes stronger with larger depletion region if the separation δ reduces which leads to reduction on V_i, as illustrated in Figure 2.1(c). When they finally keep in touch [Figure 2.1(d)], the barrier owing to the vacuum no longer exists and it contributes to the ideal Schottky contact. In this case, the Schottky barrier height relates to the Fermi level is given by

$$\Phi_B = \Phi_m - \chi_s \tag{2.1}$$

In order to obtain Eq. (2.1) namely Schottky-Mott limit, a series of assumptions have been made:

- The surface dipole contributions to Φ_m and χ_s does not change or at least their difference does not change when the metal and semiconductor keep in touch.
- No localized states exist on the semiconductor surface.
- The contact between the metal and semiconductor is perfect.

Similar analysis could be done with Schottky contact on p-type semiconductor where $\Phi_m < \Phi_s$, while $\Phi_m < \Phi_s$ with n-type semiconductor or $\Phi_m > \Phi_s$ with p-type semiconductor result in ohmic contact without rectifying effect. In this thesis we focus only on the n-type Schottky contact.

2.1.2 The effect of interface states

According to Eq. (2.1), the barrier height should directly depend on the metal work function Φ_m or in other words, the type of the metal. However, it has been experimentally found that the Φ_B is less sensitive to Φ_m as indicated by Eq. (2.1), and under certain circumstances it could be almost independent of the metal type. This is because that the ideal situation illustrated in Figure 2.1(d) is never reached in real case. Even though the metal-semiconductor is well fabricated, a thin insulating film still exists at the interface due to the surface oxidation layer (~10 to 20 Å) on the side of semiconductor, which results in the case more closed to that shown in Figure 2.1(c).

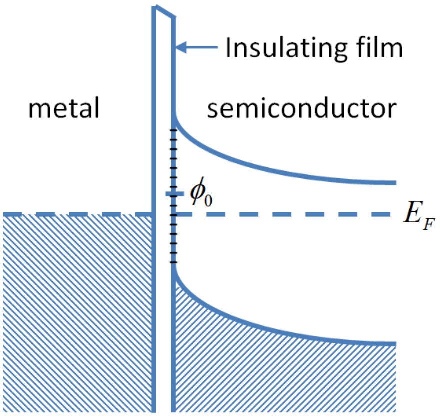


Figure 2.2. Metal-semiconductor contact with interface states.

In order to explain this weak dependence on Φ_m, the effect due to surface state has been put forward by Bardeen [72]. As shown in Figure 2.2, a thin insulating layer with a continuous distribution of interface states is assumed between the metal and semiconductor. The interface states are characterized by a neutral level ϕ_0 and the 'absolute-zero' approximation on Fermi level is purposed, namely all energy levels above the Fermi level are empty while those levels below the Fermi level are occupied. In this case, if ϕ_0 is above the Fermi level (Figure 2.2), a net positive charge Q_{ss} shows up at the interface than the neutral condition (or without interface states). In this case, instead of the relation under ideal circumstance that $Q_m + Q_d = 0$, where Q_m is the negative charge on the surface of metal and Q_d represents those positive charge due to the uncompensated donors in the semiconductor, the interface charge should also take into consideration which results in $Q_m + Q_d + Q_{ss} = 0$.

Now consider the case shown in Figure 2.2 where ϕ_0 lies above the Fermi level. Owing to the existence of Q_{ss}, Q_d should be smaller than where interface states were absent, which leads to the reduction of the depletion region width w. Since the barrier height Φ_B equals to the sum of band bending V_{d0} and ξ [Figure 2.1(d)], Φ_B would be reduced compared to the ideal case. This reduction on Φ_B will in turn reduce the positive charge in the interface states by pushing the ϕ_0 towards the Fermi level. This functions as a negative-feedback loop which forces to reduce the difference between the Fermi level and ϕ_0. Eventually, if the interface states density is large enough, the Fermi level will be pinned to ϕ_0 and the barrier height will be expressed as

$$\Phi_B \approx E_g - \phi_0 \tag{2.2}$$

This is the so-called Bardeen limit. On the other hand, with similar analysis, the results would be somewhat the same if ϕ_0 is below E_F at the initial state. Now trying to focus on the interface states with a limited density, that is more approach to the real case. With the help of the flat-band analysis, the barrier height on flat-band condition Φ_{BF} (under certain bias) could be expressed as [73]

$$\Phi_{BF} = \gamma(\Phi_m - \chi_s) + (1-\gamma)(E_g - \phi_0) \tag{2.3}$$

where

$$\gamma = \frac{\varepsilon_i}{\varepsilon_i + q\delta D_s} \tag{2.4}$$

here $\varepsilon_i = \varepsilon_{ir}\varepsilon_0$ is the permittivity of the interfacial layer and D_s the interface states dentity.

It could be seen that if the density of interface states is small enough to be ignored, γ tend to be unit which leads to the ideal case. On the other hand, γ approaches zero and the barrier height is closed to the Barden limit with thick interfacial layer and large D_s.

2.2 Current transport mechanisms though Schottky barrier

2.2.1 Introduction

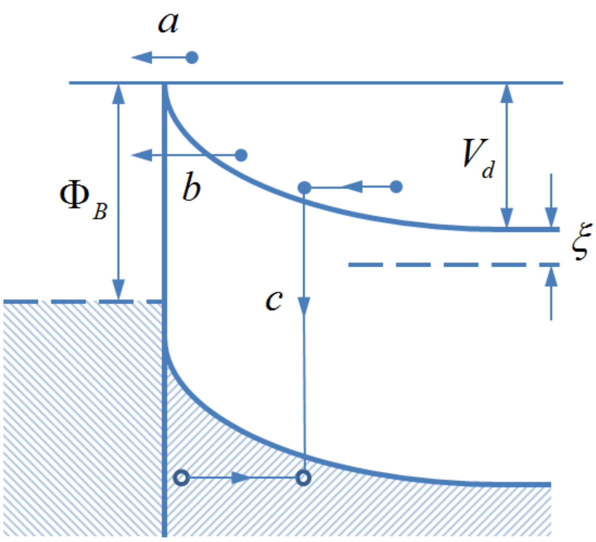


Figure 2.3. Main current transport processes in a forward-biased Schottky barrier.

If a Schottky contact is forward biased (the electric potential on the metal side is higher than the semiconductor for the n-type case), electrons will flow though the Schottky barrier which contributes to the diode current. If we ignore the hole injection that usually takes place when the SBH is greater than half of the band gap and a high density of holes appear near the interface of the semiconductor, three main current transport processes are illustrated in Figure 2.3: [74]

(a) Electron emission over the top of the barrier;

(b) Tunneling through the barrier;

(c) Recombination in the space charge region;

Practically (a) takes charge of the main current transportation. In this process, electrons are first transported from interior of the semiconductor to the interface under the mechanisms of diffusion within the depletion region, and then emitted into the metal. By contributing the limitation of current transportation to different processes discussed above, two theories namely diffusion theory and thermionic-emission (TE) theory have been put forward. Meanwhile, (b) often shows up at high bias condition with the help of strong electric field or low temperature where carriers do not have enough energy to emit through the barrier. On top of that, (c) could greatly influence the forward characteristics if there are a huge number of recombination centers namely deep levels.

2.2.2 The diffusion theory

According to the diffusion theory discussed by Wagner and Schottky, the electron transportation within the depletion region should be the limiting factor [75, 76]. That is usually the case when the width of the depletion region is large compared to the carrier mean free path. As a result, the current density over the junction could be expressed based on the carrier diffusion-drift:

$$J = nq\mu_n\mathcal{E} + qD_n\frac{dn}{dx} \tag{2.5}$$

where n is the electron concentration in the n-type semiconductor, μ_n the carrier mobility, D_n the diffusion constant, $\mathcal{E}$ the electric field over the barrier and q the magnitude of the charge on electron.

By assuming that only drift and diffusion in the depletion region contributes to the entire current flow, the current density J on function of forward bias V could be deduced as:

$$J = 2kT\mu N_C a^2 w(e^{\frac{qV}{kT}} - 1)e^{-\frac{q\Phi_B}{kT}} \tag{2.6}$$

or

$$J = qN_C\mu\mathcal{E}_{\max}e^{-\frac{q\Phi_B}{kT}}(e^{\frac{qV}{kT}} - 1) \tag{2.7}$$

where $a = (q^2N_D/2\varepsilon_s kT)^{1/2}$ and $\mathcal{E}_{\max} = qN_D w/\varepsilon_s = 2kTa^2w/q$.

Even though Eq. (2.7) has the form closed to that of the ideal rectifier $J = J_0[\exp(qV/kT) - 1]$, the $\mathcal{E}_{\max}$ arises with increase of the bias voltage and is proportional to $(V_{d0} - V)^{1/2}$, which results in the growth of saturation current under increasing reverse bias.

2.2.3 The thermionic-emission (TE) theory

Unlike in the diffusion theory, the transportation of electrons over the interface of metal-semiconductor is considered as the current-limiting process in the TE theory. In other words, it is assumed that the quasi-Fermi level for electrons keeps constant throughout the depletion region and the electron mobility on the semiconductor side near interface is infinite and thus the effects of drift & diffusion in the depletion region could be neglected. This condition could be reached if the mean free path l is large compared with w , or with a much weaker condition for the validity that l only needs to exceed the distance d where the barrier falls by a value of kT/q from its maximum as cited by Bethe [77].

By analyzing the tunneling process through the barrier with a probability p_t , the current density owing to the electrons passing from the semiconductor into the metal could be expressed as:

$$J_{sm} = \frac{p_t q N_C \bar{v}}{4} e^{-\frac{q(\Phi_B - V)}{kT}} \tag{2.8}$$

where $\bar{v}$ is the average thermal velocity of electrons in the semiconductor and with a value of $(8kT/\pi m^*)^{1/2}$ for a Maxwellian distribution.

By taking into consideration the reverse process namely electrons passing through the barrier from metal to the semiconductor that is independent on the bias due to a constant barrier height, the current density from metal to semiconductor J_{ms} could be deduced in the same way and the total current density should be the sum of these two:

$$J = J_{sm} - J_{ms} = \frac{p_t q N_C \bar{v}}{4} e^{-\frac{q\Phi_B}{kT}} (e^{\frac{qV}{kT}} - 1) \tag{2.9}$$

Being aware that $N_C = 2(2\pi m^* kT/h^2)^{3/2}$ and replacing p_t by 1, which has been proved by Baccarani [78] and Berz [79], the TE theory could be finally expressed as:

$$J = A^* T^2 e^{-\frac{q\Phi_B}{kT}} (e^{\frac{qV}{kT}} - 1) \tag{2.10}$$

where

$$A^* = \frac{4\pi m^* q k^2}{h^3} \tag{2.11}$$

Compared with the Richardson constant A, A^* namely effective Richardson constant could be regarded as replacing the free-electron mass m by the effective mass m^*, with a value of

$$A^* = 120(m^*/m)\ A \cdot cm^{-2} \cdot K^{-2} \tag{2.12}$$

2.2.4 Tunneling and Thermionic-Field Emission (TFE) model

Thanks to the quantum-mechanical tunneling effect, it may be possible for an electron passing through the barrier which is higher than its energy under certain circumstances. As is known to all that tunneling probability strongly depends on the density of states and the width of the potential barrier instead of barrier height, current transport mechanisms could be greatly affected especially under low temperature and high electric field.

Apart from the thermal emission that dominates at high temperature as discussed before, if the semiconductor is heavily doped, electrons could still overcome the barrier at low temperature with the help of tunneling, which is known as 'field' emission (FE). Therefore, when the electric field becomes higher, the electron will not only directly emit over the Schottky barrier as discussed in the TE model, but also tunnel though the barrier, which could dominate the whole current under high bias (e.g. $8\times10^4\,V/cm$ for Au-GaAs or $4\times10^5\,V/cm$ for Au-Si [80]). This is the Thermionic-Field Emission (TFE) model. By assuming that the current increases exponentially with surface field $\mathcal{E}_S$, the current flow could be expressed as [81]

$$J = AT^2 e^{-\frac{q(\Phi_B - \alpha|\mathcal{E}_S|)}{kT}} \tag{2.13}$$

where α is an effective tunneling constant given by $\alpha \equiv (kT/q)(d\ln J/d\mathcal{E}_S)$.

2.2.5 Recombination in the depletion region

In addition to the emission process (either TE or FE), recombination sometimes plays an important role in current transportation as well. According to the recombination process, there are two types of recombination: (a) **direct recombination** that is due to the direct transition of carriers between conduction band and valence band. and (b) **indirect recombination** that functions with the help of localized states, which is also called Shockley-Read-Hall (SRH) recombination [82, 83].

According to SRH theory of semiconductor, the recombination ratio U_r with a single trapping center could be denoted as

$$U_r = \frac{\sigma_p \sigma_n v_{th} N_t (np - n_i^2)}{\sigma_n [n + n_i \exp\left(\frac{E_t - E_i}{kT}\right)] + \sigma_p [p + n_i \exp\left(\frac{E_i - E_t}{kT}\right)]} \tag{2.14}$$

where E_t is the energy level of localized state, N_t its concentration, v_{th} the thermal velocity of carrier, σ_p and σ_n the capture cross section of holes and electrons.

It is clear that those defect centers with the energy levels near the middle of forbidden band (namely deep levels) can be the most effective combination centers. As a result, the recombination may become the major mechanism under low forward bias where a considerable width of depletion region remains if those effective trapping centers participate in. The current J_r due to recombination through a Schottky barrier is:

$$J_r = J_{r0} e^{\frac{qV}{2kT}} (1 - e^{-\frac{qV}{kT}}) \tag{2.15}$$

where $J_{r0} = qn_i w / 2\tau_r$, and τ_r is the lifetime within the depletion region which strongly depend on the combination center as illustrated in (2.15).

This recombination current has the similar form as discussed in TE theory unless there is a factor of 2 in the denominator of the main exponential term. Taking into consideration of current owing to both emission and recombination, the total current density is given by:

$$= J_{te} + J_r = (J_{t0} e^{\frac{qV}{kT}} + J_{r0} e^{\frac{qV}{2kT}})(1 - e^{-\frac{qV}{kT}}) \tag{2.16}$$

On top of that, it has been uncovered that carrier lifetime could greatly depend on the shape of the sample and its surface states, which due to the accelerated recombination process at the surface because of those surface states and defects. This indicates that the recombination owing to the interface states of the Schottky contact could also have a big impact on I-V characteristic.

2.2.6 Image-force lowering of SBH

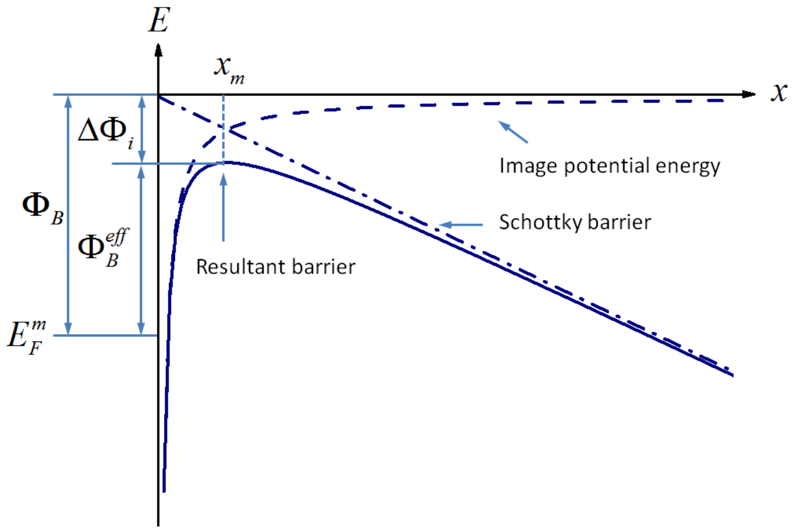


Figure 2.4. Image-force lowing of SBH.

Image-force lowering or in other words, Schottky barrier lowering describes the phenomenon that the SBH will be reduced due to the image force when the carrier transfers from the semiconductor to the metal under forward bias.

In order to analyze the image force, we first consider a metal-vacuum system. When an electron is presented in front of the metal with a distance of x, the induced electric field at the surface of metal could be regarded as if there were a positive charge of magnitude q located at the mirror-image of electron with respect to the metal surface. Therefore, the force on the electron towards the metal is:

$$F = \frac{-q^2}{16\pi\varepsilon_0 x} \tag{2.17}$$

As a result, the reduction on Schottky barrier owing to the image force is its integration from infinite, and the potential of the barrier should be

$$E(x) = \frac{-q^2}{16\pi\varepsilon_s' x} - q\mathcal{E}_{\max} x \tag{2.18}$$

where $\mathcal{E}_{\max}$ is the electric field in the semiconductor and regarded constant with the maximum value of that in the semiconductor. Here ε_s' is the permittivity of the semiconductor under high frequency rather than the static permittivity since no enough time is permitted for the semiconductor to become fully polarized by the electric field, as is indicated by Sze [84].

As shown in Figure 2.4, by calculating the position x_m where the maximum value of potential height is reached, the reduction on effective Schottky barrier height compared to that without image force in reduced as

$$\Delta\Phi_i = \sqrt{\frac{q\mathcal{E}_{\max}}{4\pi\varepsilon_s'}} \tag{2.19}$$

Image-force lowering is one of the important factors that drive the I-V characteristic of Schottky diode away from the ideal case. However, it is significant to be aware of the basic precondition that electrons should transfer into the metal through the barrier. In other words, image-force lowering should be taken into consideration only in the I-V case. On the other hand, the C-V test without carrier transportation over the barrier should not be affected by the image-force lowering.

2.3 Measurement of SBH

As discussed above, the SBH not only depends on the type of metal/semiconductor along with its doping concentration, but is also influenced by the interface states. Therefore it is more practical to determine the SBH with experimental measurements. A number of methods are developed in order to measure the barrier height, for example:

- forward current-voltage characteristics
- reverse capacitance-voltage measurements
- photoelectric measurements
- photoelectron emission spectroscopy

Thanks to the easy setup and convenient to analyze, I-V and C-V characteristics are widely adopted for SBH determination, which will be mainly introduced in this section.

2.3.1 I-V characteristics

Based on the discussion on current transport mechanisms, the true behavior in practical seems to lie somewhere between the TE theory and the diffusion theory if we ignore the low temperature or high electric field conditions. However, normally the TE theory is more suitable to forecast the I-V characteristics on those well fabricated diodes based on high mobility semiconductors [74]. According to TE theory, if the forward bias is low enough that the voltage drops on the series resistance could be ignored, the forward current is given by:

$$I = I_s \left(e^{\frac{qV}{kT}} - 1 \right) \tag{2.20}$$

where I_s is the saturation current that is

$$I_s = SA^* T^2 e^{-\frac{q\Phi_B}{kT}} \tag{2.21}$$

where S is the effective surface of Schottky diode.

Since transportation of carriers takes place under forward bias, image-force lowering should be taken into consideration. Therefore, instead of real barrier height Φ_B, it should be replace by the effective barrier height Φ_B^{eff} here as shown in Figure 2.4, which is given by $\Phi_B^{eff} = \Phi_B - \Delta\Phi_i$. However, as though the target is to measure the barrier height from experimental method, it makes no sense to separate these two concepts and as a result, only Φ_B will be used for discussion in the following sections.

According to Eq. (2.20), if the forward bias is large enough that $qV \gg kT$ while the series resistance could still be neglected, the plot ln(I)-V should be linear with a slope equals to q/kT and the ordinate at the origin gives the saturation current I_s and as a result, Φ_B could be calculated if A^* is known. However, A^* could not always be a known parameter. To determine the effective Richardson constant A^*, the Richardson plot is commonly used in practical case. Based on Eq. (2.21), $\ln(I_S/T^2)$ *vs.* $1/T$ should be linear with a slope related to the barrier height and an ordinate originally bound to A^*.

2.3.2 C-V measurements

If the Schottky diode is nearly ideal where the effect due to the minority carriers can be neglected and a uniform donor concentration is presented in the semiconductor as assumed in the TE model, the electric field at the interface is due to only the uncompensated donors. Thus the differential capacitance under reverse bias is linked to the width of the space charge region w and doping concentration $N_D - N_A$ as

$$C = \frac{\varepsilon_s S}{w} \tag{2.22}$$

$$w = \sqrt{\frac{2\varepsilon_s}{q\left(N_D - N_A\right)}\left(V_I - V_r\right)} \tag{2.23}$$

where ε_s is the dielectric constant of semiconductor and V_r is the reverse bias.

Since the uniform doping concentration is assumed, the function of $1/C^2 = f\left(V_r\right)$ ought to be a straight line, where the intersection with x-axis V_I gives the barrier height Φ_B as [85]:

$$\Phi_b = V_I + \frac{kT}{q} + \left(E_C - E_F\right) \tag{2.24}$$

At the same time, doping concentration could also be extracted base on the slope:

$$N_D - N_A = \frac{2}{q\varepsilon_s S^2 \left|slope\right|} \tag{2.25}$$

Since no mechanism of carrier transportation over the barrier takes charge during C-V characterization, the effect of image-force lowing should be wiped out. Therefore the SBH obtained from C-V should always higher than that from I-V on the same Schottky contact in the ideal case.

2.4 Review on SBH models

2.4.1 Ideality factor and zero-bias barrier height

Generally speaking, the slope of log(I)-V plot discussed in 2.3.1 could never be found unit due to the dependence of SBH on bias as well as the effect of image-force lowering. Considering the bias dependence of barrier height as linear, such that $\Phi_B = \Phi_{B0} + \gamma V$, where Φ_{B0} is the barrier height at zero bias and $\gamma(=\partial\Phi_B/\partial V)$ is positive, Eq. (2.20) can be modified to

$$I = I_s e^{\frac{qV}{nkT}}\left(1 - e^{\frac{-qV}{kT}}\right) \tag{2.26}$$

with the saturation current I_S as

$$I_s = SA^* T^2 e^{\frac{-q\Phi_{B0}}{kT}} \tag{2.27}$$

Here $n = 1/(1-\gamma)$ is called the ideality factor of the diode [86].

Based on Eq. (2.26) and Eq. (2.27), if the series resistance is small enough to be ignored, the relationship between $\log(I)$ and V should be linear. Therefore, either ideality factor or zero bias barrier height can be deduced via direct I-V plot.

On consideration of the effect of a thin interfacial layer as well as the effect of image force and surface charges on the barrier height, that also manifests at 0 V and results in $n \neq 1$, Hackam and Harrop [87] have proposed that it is necessary to involve ideality factor n into the expression of saturation current I_S, and Eq. (2.27) is amended as follows:

$$I_s = SA^* T^2 e^{\frac{-q\Phi_{B0}}{nkT}} \tag{2.28}$$

2.4.2 T$_0$ effect

In order to precisely fit the experimental I-V characteristics of Schottky diodes, where a variation of n with temperature is observed, Padovani and Sumner [88] have suggested replacing T by $T + T_0$ in the thermos-ionic emission model, therefore Eq. (2.20) becomes (neglecting series resistance):

$$I = SA^* T^2 e^{-\frac{q\Phi_{B0}}{k(T+T_0)}}\left[e^{\frac{qV}{k(T+T_0)}} - 1\right] \tag{2.29}$$

where T_0 neither depends on temperature nor voltage over a wide temperature range. Therefore, this relation amounts to introducing an ideality factor in the two exponential terms:

$$n = 1 + \frac{T_0}{T} \tag{2.30}$$

2.4.3 Gaussian distribution

To explain the difference between SBH measured by I-V and C-V over the range of measurement temperatures, Song et al. [89] assumed that barrier height is normally distributed with a probability density:

$$P(\Phi_B) = \frac{1}{\sigma_S \sqrt{2\pi}} e^{-\frac{\bar{\Phi}_B - \Phi_B}{2\sigma_S^2}} \tag{2.31}$$

where $\bar{\Phi}_B$ is the average of SBH and σ_S is its standard deviation.

In this case, the SBH can be expressed as:

$$\Phi_B = \bar{\Phi}_B - \frac{\sigma_S^2}{2kT/q} \tag{2.32}$$

Practically, the SBH at 0 V Φ_{B0} can be calculated at each temperature based on Eq. (2.28) if we know the value of A^*. Thus Eq. (2.32) is usually modified to:

$$\Phi_{B0} = \bar{\Phi}_{B0} - \frac{\sigma_{S0}^2}{2kT/q} \tag{2.33}$$

where σ_{S0} is the standard deviation of Φ_{B0} at 0 V. Therefore it is possible to extract $\bar{\Phi}_{B0}$ and σ_{S0} by plotting Φ_{B0} vs. $q/2kT$.

2.4.4 Potential Fluctuation model

This model was developed by Werner and Guttler [90] to explain the temperature dependence of the ideality factor. The barrier height is assumed to be normally distributed, but the mean and standard deviation are assumed to vary linearly with voltage as

$$\bar{\Phi}_B = \bar{\Phi}_{B0} + \rho_2 V \tag{2.34}$$

and

$$\sigma_S^2 = \sigma_{S0}^2 + \rho_3 V \tag{2.35}$$

to explain the temperature dependence of the ideality factor. We can then show that the ideality factor can be expressed in the form:

$$\frac{1}{n}-1=-\rho_2+\frac{q\rho_3}{2kT} \tag{2.36}$$

The valus of ρ_2 and ρ_3 can be obtained from the slope and the ordinate at the origin on the $n^{-1}-1$ vs. $q/2kT$ plot.

2.4.5 Flat-band barrier height

Since the barrier height depends on the electrical voltage, i.e. in fact on the electric field, Wagner et al. [91] proposed to define the barrier height in flat bands (under zero field) Φ_{BF}, which would be a more fundamental magnitude because independent of the applied voltage and given by:

$$\Phi_{BF}=n\Phi_{B0}-(n-1)\frac{kT}{q}\ln\frac{N_C}{N_D} \tag{2.37}$$

2.4.6 Modified Richardson plot

As is discussed, to determine the effective Richardson constant A^*, the Richardson plot is commonly used and the plot on $\ln(I_S/T^2)$ *vs.* $1/T$ should be linear based on Eq. (2.21). However, owing to the deviation from linear region on traditional Richardson plot, the so-called modified Richardson (MR) plot is adopted as $\ln(I_S/T^2)$ *vs.* $1/nT$ based on Eq. (2.28) [87]. Meanwhile, other types of MR plot have also been put forward according to model of Gaussian distribution as $\ln(I_S/T^2)-q^2\sigma_{S0}^2/2K^2T^2\ vs. q/kT$ [92] and on the basis of flat-band barrier height as $\ln(I_S/T^2)+(1-1/n)\ln(N_C/N_D)$ *vs.* $1/nT$ [93]. These could help us to determine A^* and the relative SBH (Φ_{B0}, $\bar{\Phi}_{B0}$ or Φ_{BF}).

On top of that, adjustment of modified Richardson plot has been put forward by BHUIYAN et.al. [94] as $n(T)\log(I_S ST^2) vs. 1/T$ by considering the linear change of SBH due to temperature.

2.4.7 Relationships between different models

❖ T_0 Effect

Even though a number of well fitted T_0 on Au/GaAs, Cr/Si and Cu/Si have been reported, it was pointed out by Werner and Güttler that Eq. (2.29) could not be generally valid for n prediction, especially on high temperature [90]. Meanwhile, they explained the T_0 effect as follows:

According to Eq. (2.36), one obtains that

$$n = \frac{1}{1 - \rho_2 + \rho_3 / \left(2kT/q\right)} \tag{2.38}$$

In case of $-\rho_2 + \rho_3/(2kT/q) \ll 1$, Eq. (2.38) can be expressed as

$$n \approx 1 + \rho_2 - \frac{\rho_3}{2kT/q} \tag{2.39}$$

Consider that in most cases it exists that $\rho_2 \ll \rho_3/\left(2kT/q\right) \ll 1$, and as a result, a second approximation could be drawn as

$$n \approx 1 - \frac{\rho_3}{2kT/q} \equiv 1 + \frac{T_0}{T} \tag{2.40}$$

Compare Eq. (2.40) with Eq. (2.30), it is clear that

$$T_0 \approx -\frac{\rho_3}{2k/q} \tag{2.41}$$

which reveals the relationship between T_0 and the Gaussian barrier distribution narrowing coefficient ρ_3 upon the application of a bias voltage.

- **Modified Richardson plot**

If we introduce T_0 effect as a well approximation among wide temperature range to the expression of the flat-band barrier height, Eq. (2.37) could be approximated by

$$\Phi_{BF} = n\Phi_{B0} - \frac{kT_0}{q} \ln \frac{N_C}{N_D} \tag{2.42}$$

As the determined T_0 is small (~ 100 K) in our case, and as a result, the second item in Eq. (2.42) could normally be neglected compared to the first one. Therefore the Φ_{BF} can be simply degenerated as

$$\Phi_{BF} \approx n\Phi_{B0} \tag{2.43}$$

This could explain the conventional MR plot based on Eq. (2.28), which extracts the value of SBH approach to the Φ_{BF}. However, as the negative item is neglected when using the approximation Eq. (2.43), the A^* obtained from the conventional MR plot is always larger than that from MR plot according to flat-band barrier height. Meanwhile, at high temperature where ideality factor is usually approach unity, the value of Φ_{B0} is closed to Φ_{BF}. As a result, the Richardson plot keeps linear at high temperature region even though the A^* extract is much smaller. Examples will be shown and discussed in the experimental results in section 4.3.

- **Gaussian distribution model and potential fluctuation model**

According to Eq. (2.43), if we replace Φ_{B0} by Φ_{BF}/n in Eq.(2.33), the relation between the ideality factor and the parameters of the Gaussian distribution can be revealed in the form:

$$\frac{1}{n}-1=\frac{\bar{\Phi}_{B0}-\Phi_{BF}}{\Phi_{BF}}-\frac{q\sigma_{S0}^{2}}{2kT\Phi_{BF}} \tag{2.44}$$

Comparing with Eq.(2.36), it can be shown that:

$$\begin{cases} \rho_2=\dfrac{\Phi_{BF}-\bar{\Phi}_{B0}}{\Phi_{BF}} \\ \rho_3=-\dfrac{\sigma_{S0}^{2}}{\Phi_{BF}} \end{cases} \tag{2.45}$$

or

$$\begin{cases} \bar{\Phi}_{B0}=(1-\rho_2)\cdot\Phi_{BF} \\ \sigma_{S0}^{2}=-\rho_3\cdot\Phi_{BF} \end{cases} \tag{2.46}$$

This highlights the links between the Gaussian distribution model and the potential fluctuation model. Our results that will be given in Chapter 4 fit well with this relation on either single barrier diodes or those diodes with multi-barrier.

2.5 Barrier inhomogeneity in Schottky devices

2.5.1 Introduction

Various non-ideal behaviors are frequently observed in Ti, Ni, and Pt-based 4H-SiC Schottky barrier diodes as well as metal insulator semiconductor (MIS) GaAs Schottky diodes [95, 96], and these are widely recognized owing to the so-called barrier inhomogeneity. As an intuitive feeling, the inhomogeneity of SBH should be able to analyze as individual area where the SBH is uniform within each region. This is known as the parallel diode model. In addition, Tung's model which explains also the pinch-off of low SBH region as well as the Fermi level pinning and the multi Gaussian distribution of barrier height is widely recognized and discussed.

Based on determining the nature and energy levels of the defects with EBIC and DLTS, Ewing et al. suggested that the low-SBH are caused by defect clusters which locally pin the Fermi level [18]. However, Bolen and Capano argued that single threading edge and threading screw dislocations do not significantly affect the electrical characteristics of 4H-SiC SBDs based on the fact that no significant conglomeration of defects found clustered together [97]. Furthermore, Dohyun Lee et al. reported the uniformity of Schottky barrier height could be improved by post-oxidation annealing in nitric oxide ambient (NO POA) [98].

2.5.2 Parallel diode model

By assuming that the Schottky contact consists of a series of ideal regions with individual constant barrier height $\Phi_{Bn,i}$ and corresponding effective area given by the fraction of total contact surface $S_i = S / a_i$, the total current though this Schottky contact under forward bias V is given by the sum of current from each individual area based on TE model:

$$I \cong \sum_{i=1}^{m} S_i A^* T^2 e^{-\frac{q\Phi_{Bn,i}}{kT}} e^{\frac{qV}{nkT}} \tag{2.47}$$

where m is the number of parallel diodes (i.e. individual homogeneous SBH regions). By introducing the lowest barrier height $\Phi_{Bn,l}$ among those regions, Brezeanu et. al. provided the expression of conventional barrier height $\Phi_{Bn,T}$ as

$$\Phi_{Bn,T} \cong \Phi_{Bn,l} - \frac{kT}{q} \ln \sum_{i=1}^{m} \frac{1}{a_i} \exp\left(-\frac{q\Delta\Phi_{Bn,i}}{kT}\right) \tag{2.48}$$

and its limit on temperature [99]:

$$\lim_{T\to 0}\Phi_{Bn,T} = \Phi_{Bn,l} \tag{2.49}$$

$$\lim_{T\to \infty}\Phi_{Bn,T} = \sum_{i=1}^{m}\frac{\Phi_{Bn,i}}{a_i} \tag{2.50}$$

This indicates that the limit of SBH measured at low temperature is determined by the parallel path with the lowest SBH, while that should be the weighted average based on their effective areas if the temperature is high enough. And this high temperature limit should be exactly the mean barrier height $\bar{\Phi}_B$ described in the Gaussian distribution model.

However, J. L. Freeouf et. al. have reported that the low barrier region will be more effectively "pinched off" by large area with higher SBH. (i.e. Even though the ratio for high SBH and low SBH keeps constant, the overall barrier height and ideality factor will shift towards the value on larger surface area with higher SBH.) Only those areas with linear dimensions larger than Debye length of the substrate could be treated as separate parallel diodes [100]. This "pinch-off" effect has been discussed in various bibliographies [89]. And the barrier height determined by C-V measurement is dominated by the phase with larger contact area [89].

2.5.3 Tung's model

Early in 1992, Tung highlighted that leakage, edge-related currents, greater-than-unity ideality factors, T_0 and other dependences of the ideality factor on temperature, soft reverse characteristics, and the dependence of the SBH on the measurement technique are all natural results of SBH inhomogeneity, which could be explained by model containing low-SBH regions shown in Figure 2.5. The localized low barrier height patches were later strongly suggested though electron beam induced current (EBIC) [95]. Meanwhile, the phenomenon that conduction-band minimum (CBM) potential pinch-off in the low-SBH region was illustratred in [101]. However, Im et al. argued that Tung model can account for highly nonideal behavior only by assuming an unphysical patch distribution in which the excess current is dominated by a few patches in the extreme tail of the patch distribution, and suggested that all the diodes contain a broad ''intrinsic'' distribution of shallow patches, while the large excess current in highly nonideal diodes is due to a few large defects of extrinsic origin [102].

Sabih Uddin Omar et al. pointed out that Tung model is applicable for SiC Schottky diodes with ideality factor $n < 1.2$, and indicated the presence of high-density of electron traps at the Schottky interface with a uniform distribution across the wafer which can explain the hysteresis and the associated Schottky nonideality [40]. Apart from [18, 19] mentioned before, S. Tumakha et al. also suggested that SiC defect levels can account for the maximum range of barrier heights [103].

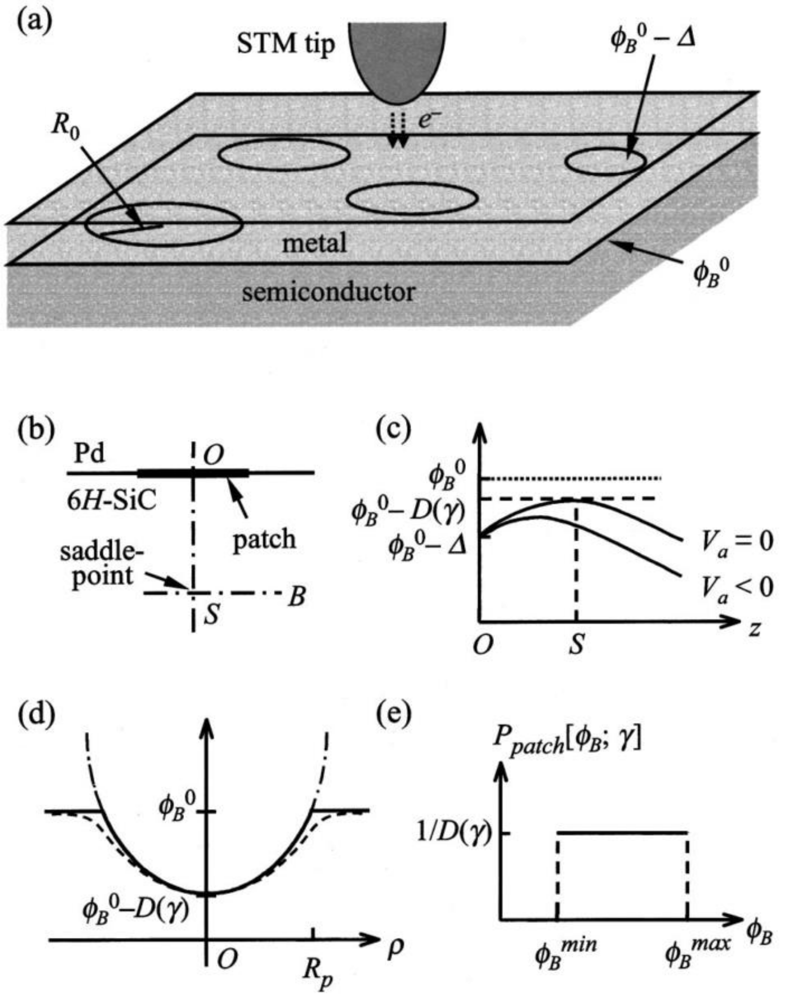


Figure 2.5. (a) Schematic of the Tung model. A random distribution of circular patches of size R_0 and barrier height $\phi_B^0 - \Delta$ in the otherwise homogeneous background of SBH ϕ_B^0. (b) A patch of size comparable to or smaller than the semiconductor Debye length gives rise to a potential saddle-point S beneath the patch center O. (c) Potential profile along the interface normal (along O-S) for zero applied bias V_a, and for a reverse bias $(V_a < 0)$. Reverse bias reduces the potential maximum (i.e., an increased depth) near S. (d) Lateral profile of the potential maximum projected normally onto the MS interface. The dashed line is the exact potential, the dash-dot line is Tung's parabolic approximation, and the solid line is the truncated paraboloid used to calculate the microscopic BHD. (e), Calculated probability density for a single low-barrier patch of strength γ, with $\phi_B^{\min} = \phi_B^0 - D(\gamma)$ and $\phi_B^{\max} = \phi_B^0$ [102].

2.5.4 Multi Gaussian distribution model

Chand and Kumar argued that the abnormal decrease of zero-bias barrier height and increase of ideality factor with decrease in temperature (T) and nonlinearity in the activation energy plot can be attributed to barrier inhomogeneity by assuming a Gaussian distribution of barrier heights at the silicide/silicon interface. Moreover, they suggested that the use of a zero-bias barrier height versus inverse temperature plot is able to indicate the presence of single/multiple distribution(s) of barrier heights and to determine the respective parameters [86]. As shown in Figure 2.6, two linear region can be distinguished and the corresponding $\bar{\Phi}_{B0}$ and σ_{S0} can be extracted by linear fitting under different temperature zone, which indicates the existence of multi-SBH. The double Gaussian distribution of the barrier heights was also verified at graphene/Si (GaAs) Schottky junctions [104], Au/p-GaTe Schottky contact [105], Ru/Pt/n-GaN Schottky diodes [92], alloy FeCrNiC on p-Si [106], and Hg contact on n-type silicon with <100> orientation [107].

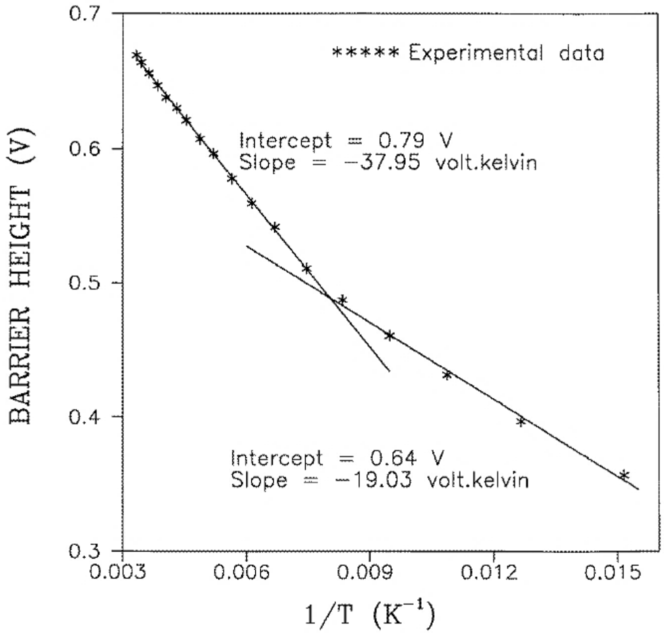


Figure 2.6. The barrier height obtained from I-V measurements as a function of inverse temperature in [86].

Chapter 3
Deep levels detection

3.1 Overview

Unlike doping in semiconductor, deep levels could hardly be detected directly with simple I-V or C-V measurement. However, with the development of modern technology, deep levels can be investigated thanks to the DLTS, Laplace Deep Level Transient Spectroscopy (LDLTS), PL (Photoluminescence), Low Temperature Photoluminescence (LTPL), Deep Level Optical Spectroscopy (DLOS) Optical Absorption (OA), and Hall Effect [46, 53, 108, 109]. In addition to conventional DLTS, alternative improvement such as Double Correlation Deep Level Transient Spectroscopy (DDLTS) [110, 111] and Constant-Capacitance Deep Level Transient Spectroscopy (CCDLTS) [112] were also reported.

Shortcomings of early used defect detection methods such as photocapacitance and admittance spectroscopy are remarkable. For example, even though benefiting from high sensitivity, photocapacitance is less practical due to complex data collection and analysis in order to obtain the accurate parameters of traps. Moreover, it is not applicable to those traps with E_a less than 0.3 eV. On the other hand, only majority carrier traps could be investigated by using admittance spectroscopy and its sensitivity will decrease for those deeper traps with large activation energy [113].

3.2 Electron capture-emission mechanism

3.2.1 Capture

If the trap level is capable of electron accommodation, the capture will take place when there are free carriers in the conduction band, or in other worlds when the Fermi level approaches the E_C, and the filled traps n_{Tc} during the capture process is:

$$n_{Tc}(t) = N_T(1 - e^{-t/\tau_c}) \tag{3.1}$$

where N_T is the trap concentration and τ_c is the capture time constant with the expression as:

$$\tau_c = \frac{1}{\sigma_n v_{th,n} n_0} \tag{3.2}$$

with σ_n the capture cross section for electrons, $v_{th,n}$ the thermal velocity of eletrons and n_0 the concentration of free carriers. The electron thermal velocity can be calculated based on effective mass of electrons m^* and Boltzman constant k at each temperature T as:

$$v_{th,n} = \sqrt{\frac{3kT}{m^*}} \tag{3.3}$$

and n_0 is usually regarded as shallow doping concentration for the electron traps and with the expression as:

$$n_0 = N_C e^{-\frac{E_C - E_F}{kT}} \tag{3.4}$$

where N_C is the state density of conduction band that is:

$$N_C = 2\left(\frac{2\pi m^* kT}{h^2}\right)^{\frac{3}{2}} \tag{3.5}$$

with h the Planck constant.

As a consequence, the capture rate c_n can be expressed as:

$$c_n = \sigma_n v_{th,n} n_0 = 1/\tau_c \tag{3.6}$$

3.2.2 Emission

As the opposite process, the electrons can also emit from the trap level to the conduction band, and the filled traps n_{Te} during the emission process can be expressed as:

$$n_{Te}(t) = N_T e^{-t/\tau_e} \tag{3.7}$$

with the emission time constant τ_e as:

$$\tau_e = \left(\sigma_n v_{th,n} X_n N_C e^{-\frac{E_C - E_T}{kT}} \right)^{-1} \tag{3.8}$$

where X_n is the entropy factor.

The emission rate e_n should be the reciprocal of the emission time constant:

$$e_n = 1/\tau_e \tag{3.9}$$

By transforming Eq. (3.8), certain Arrhenius-equation exist:

$$\ln\left(\tau_e v_{th,n} N_C\right) = \frac{E_C - E_T}{k} \frac{1}{T} - \ln\left(X_n \sigma_n\right) \tag{3.10}$$

where the $X_n \sigma_n$ is the capture cross section extracted by the experiments, also called sigma (σ).

According to Eq. (3.10), if the emission time constant at different temperature can be measured, the activation energy of trap level and its capture cross section can be deduced from the Arrhenius plot by linear fitting of $\ln(\tau_e v_{th,n} N_C)$ vs. $1/T$.

Another possibility for the y-axis of the Arrhenius plot can be expressed as $\ln(\tau_e T^2 C)$, where C is all the constants other than the temperature or in other words:

$$C = \frac{v_{th,n} N_C}{T^2} \tag{3.11}$$

3.2.3 Steady state capture-emission

Figure 3.1 illustrates the combination effect of carrier capture-emission through a trap level. Even though the capture (c_1, c_2) and emission (e_1, e_2) processes take place throughout and obey the corresponding law introduced above, the trap state can be determined by one or certain main process that depends on the state of semiconductor. Here an n-type semiconductor is assumed for discussion, while that should be similar when it comes to the p-type one.

❖ **Common state**

The 'common state' indicates that the conduction band is full of free electrons and no obvious minority carrier injection takes place, which is the common case for the n-type semiconductor without external interference. If the capture rates for those trap levels are much larger than the emission rates, the emission process can be neglected on steady state and as a result, only capture process should be taken into consideration in the expression of trapped electrons n_T:

$$n_T = \frac{c_1}{c_1 + c_2} N_T \tag{3.12}$$

where c_1 is the majority carrier (electron) capture rate (recombination rate) proportional to the majority carrier concentration and c_2 is the minority carrier (hole) capture rate proportional to the concentration of injected minority carriers. As no obvious injection of minority carrier is assumed in this common state, certain relation holds that $c_1 \gg c_2$. As a result, the trap level is filled with electrons with the concentration closed to that of the trap.

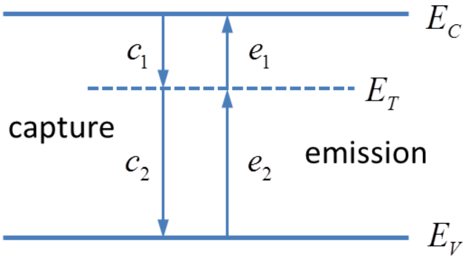


Figure 3.1. Schematic of electron capture-emission through trap levels.

- **Depletion**

When the n-type material keeps in contact with a p-type one or certain metal in order to present a Schottky contact, a depletion region is formed and those trap levels lie in the n-type side within the depletion region are regarded as in the depletion state. Since almost no free carrier exists in the depletion region, the capture rates tend to be zero and the trap state n_T is dominated by the emission process:

$$n_T = \frac{e_2}{e_1 + e_2} N_T \tag{3.13}$$

In that case, if $e_1 \gg e_2$, it should be regarded as electron (majority carrier) trap and is almost empty at depletion state. On the other hand, if $e_1 \ll e_2$, this trap is capable of trapping holes and tend to be full here. According to Eq. (3.8) and (3.9), the emission rate is largely depend on the difference between trap level and the conduction band (electron traps) or the valence band (hole traps). As a result, those electron traps usually lies in the upper half of the bandgap with their activation energies marked as $E_a = E_C - E_T$, while those hole traps tend to be in the lower half with their activation energies as $E_a = E_T - E_V$.

- **Injection**

When the minority carrier concentration is large enough to reach the level of the majority carrier (e.g. due to the forward bias in the p-n junction if we focus on the depletion region), the capture rate of minority carrier (hole) could exceed that of the majority ones (electron) and so $c_2 \gg c_1$. In that case, almost no trap level will be captured by electron according to Eq. (3.12) and these trap centers are filled with holes instead. In other words, those minority traps could only be detected under the injection state with the help of large forward bias in a p-n junction namely saturating injection pulse [113].

3.2.4 Transient

In order to characterize trap levels, the measurement of pulsed bias capacitance transients are commonly adopted. As discussed above, if the trapping state is switched, which usually can be realized by changing the voltage bias through the sample under test, the transient of carrier will take place due to the unbalanced state by either emission or capture that comply with the time law [Eq. (3.1) or Eq. (3.7)]. Because of the relatively long emission process compared to capture due to larger time constant, the emission process is much easier to characterize and measure by the capacitance transient. For example, the transient of electrons will take place if the Fermi level is forced to shift by applying different bias through a Schottky contact or p-n diode, and a direct performance, the change of capacitance will be observed during the transient. To discuss this kind of capacitance transient, the applied bias is considered to switch from a relatively high value (pulse voltage U_P) to a lower one (reverse voltage U_R). In that case, the transient of capacitance due to the emission process is:

$$C(t) = C_R - \Delta C e^{-t/\tau_e} \tag{3.14}$$

where the transient amplitude ΔC is:

$$\Delta C = C_R \frac{N_T}{2N_S} \frac{L_R^2 - L_P^2}{w_R^2} \tag{3.15}$$

and

$$L_{R,P} = w_{R,P} - \lambda \tag{3.16}$$

where L is the distance intersection Fermi level and trap level. Here the index R resp. P means the value at reverse bias U_R resp. at pulse voltage U_P. The lambda shift involved is illustrated in Figure 3.2, with the voltage independent distance λ:

$$\lambda = \sqrt{\frac{2\varepsilon_s \left(E_F - E_T\right)_0)}{q^2 n_0}} \tag{3.17}$$

where $(E_F - E_T)_0$ is the energy difference between trap level and Fermi level in the undisturbed semiconductor.

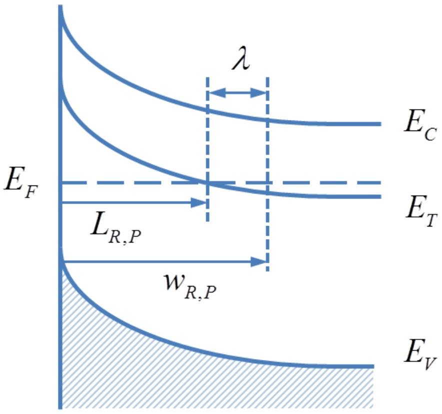


Figure 3.2. Lambda shift under either reverse bias or pulse voltage.

If proper bias condition is selected that makes $L_P \approx 0$ and $\lambda \ll w_R$, Eq. (3.15) can be simplified with the approximation:

$$\Delta C = C_R \frac{N_T}{2N_S} \tag{3.18}$$

In short, if the transient can be measured, the emission rate of trap and its concentration can be deduced from the time constant and amplitude of capacitance transient respectively.

3.2.5 Limitation on trap detection

Even though the transient measurement for trap characterization is suitable for most condition, several limitations exist and cannot be ignored especially at low temperature.

- **Carrier freeze-out**

According to Eq. (3.15), the defect concentration is determined with the help of the shallow doping concentration. However, when temperature is below 120 K, carriers will be partly frozen on shallow levels that results in reduction of free carriers in the conduction band. Meanwhile, as a prerequisite that $N_T \ll N_S$, traditional transient measurement will no more provide the accurate results if most carriers are frozen out at low temperature. This freeze-out effect is especially prominent at temperature below 40 K, and will be discussed in detail in 5.3.1.

- **Poole-Frenkel (PF) effect**

Similar as the TFE model discussed in 2.2.4, the strong electric field close to the metal-semiconductor interface will enhance the emission rate at the same time by lowering the potential barrier over which the carrier is thermally emitted. Therefore, increased applied electric field should lead to lower activation energy, which is recognized as the Poole-Frenkel (PF) effect [53]. This PF effect not only lies in wide bandgap semiconductors, but should also be taken into consideration when it comes to the narrow bandgap semiconductor materials [114]. The emission rate of PF increases exponentially with the square root of the applied electric field, that leads to the decrease of the activation energy of trap level, and this PF emission can be the dominate mechanism for electron emission from trapping centers for temperatures above 250 K [115]. Furthermore, the PF effect related to the dislocation will be affected by the presence of attractive dislocation deformation potential as well [116]. On the other hand, the electron trap levels are considered as acceptor type if no Poole-Frenkel effect is observed [117, 118].

3.3 DLTS Principle

As one of the well-known defect detection methods, Deep Level Transient Spectroscopy (DLTS) is widely used thanks to its high sensitivity, wide detection range of trap depths, reduced measurement time and easy analysis. The defect type, activation energy and its concentration could be determined from the sign, position and height of those peaks shown up on the DLTS signal [113].

3.3.1 Basic DLTS principle

It is commonly accepted as logarithmic filling law that a DLTS signal can be regarded as the fingerprint of an extended defect, and particularly of dislocations [39]. And as a result, it becomes one of the most versatile techniques to determine the abovementioned deep levels over a wide range of depths in semiconductor material.

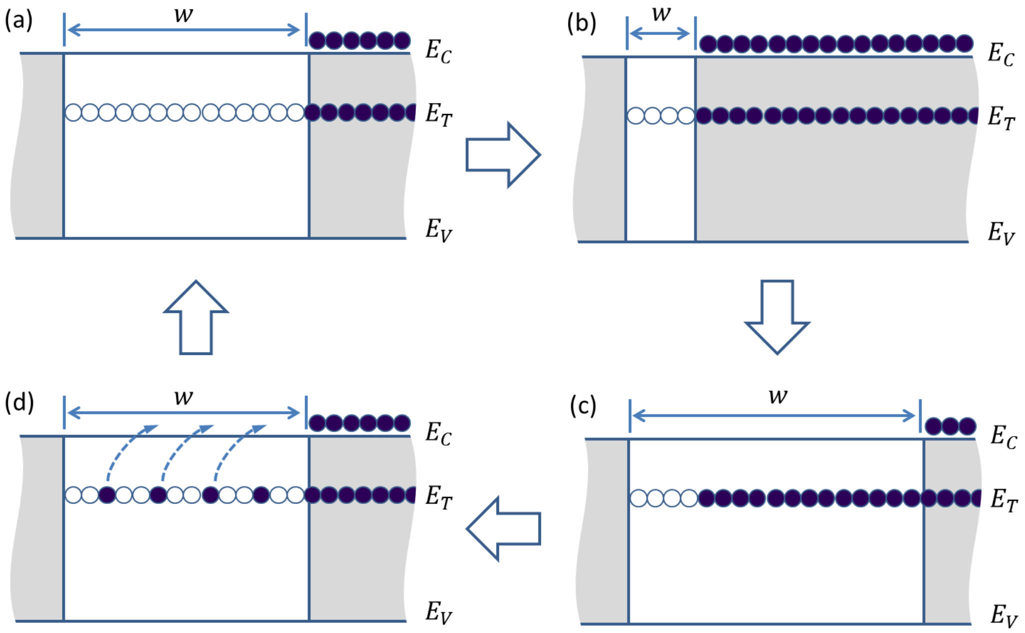


Figure 3.3. A schematic of the DLTS transient signal generation. (a): Steady state reverse bias, (b): Applying pulse; (c): Just after removing pulse; (d): Capacitance transient due to thermal emission of carriers.

Based on basic theory of emission/recombination in semiconductors, the DLTS measures the change of junction capacitance of the sample due to the emission of charge carriers from the defects existing in the space charge region. To better understand the DLTS theory, let’s consider a reverse biased n-type semiconductor Schottky device with a deep level marked as E_T, as is shown in Figure 3.3 [6]. When a pulse U_P is applied [Figure 3.3(b)] the SCR is reduced and thus the capacitance increases drastically. Therefore the traps begin to gather carriers from the bulk region, and will be fulfilled if the pulse duration T_P is long enough. With return of the reverse bias U_R to its quiescent level, the width of the SCR restores [Figure 3.3(c)]. As the filled traps are above the Fermi level, the system will relax into thermal equilibrium by emitting trapped charge carriers [Figure 3.3(d)], and the capacitance will gradually increase until the steady-state value of Figure 3.3(a).

In that case, a transient of capacitance occurs during carrier emission, as is shown in Figure 3.4. While the capacitances are measured at fixed time (double boxcar) under various temperatures, the relationship between difference of capacitance ΔC and temperature can be obtained, as illustrated in Figure 3.5. Here the time different $t_2 - t_1$ is regarded as the period width T_W of DLTS measurement if the time delay t_1 keeps constant during the whole characterization. However T_W becomes more complicate in real DLTS test system and will not be explained in detail here. The temperature where maximum appears corresponds to specific deep level. By locating the maximum temperature point under different period width, the Arrhenius plot can be drawn to extract the trap parameters, and this is the so-called DLTS maximum analysis.

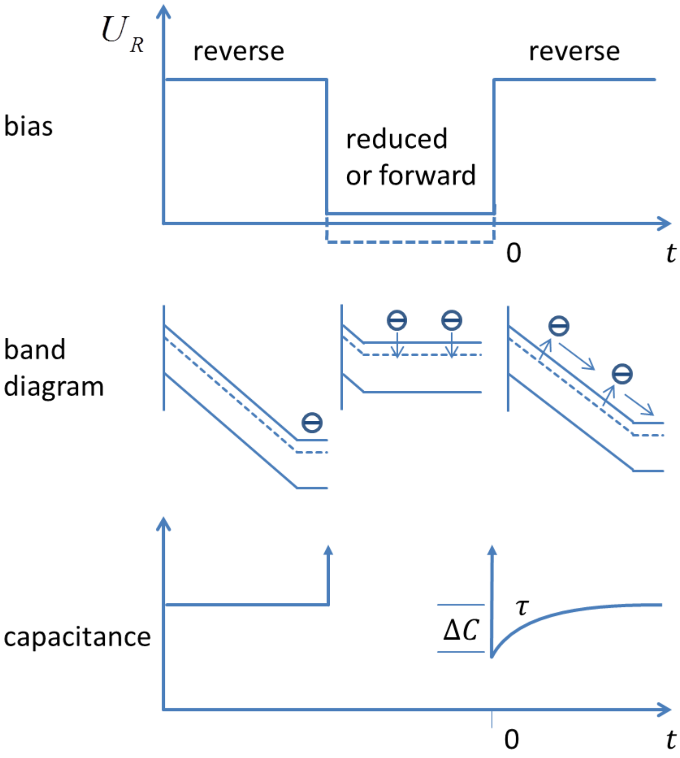


Figure 3.4. Capacitance and band diagram evolution based on bias condition.

To pursue higher resolution, an inverse Laplace transform of a digitally averaged transient is adapted to replaces Lang's double boxcar, which could remove the instrumental broadening from DLTS. This is the so-called Laplace DLTS or LDLTS. As an isothermal measurement, it can separate defects with very similar emission rates $(e_1 / e_2) \sim 2$, i.e. a resolution of ~2 meV at 100 K due to dynamic determination of regularisation parameters based on Tikhonov approach [119]. These high resolution DLTS will be explained in the following sections.

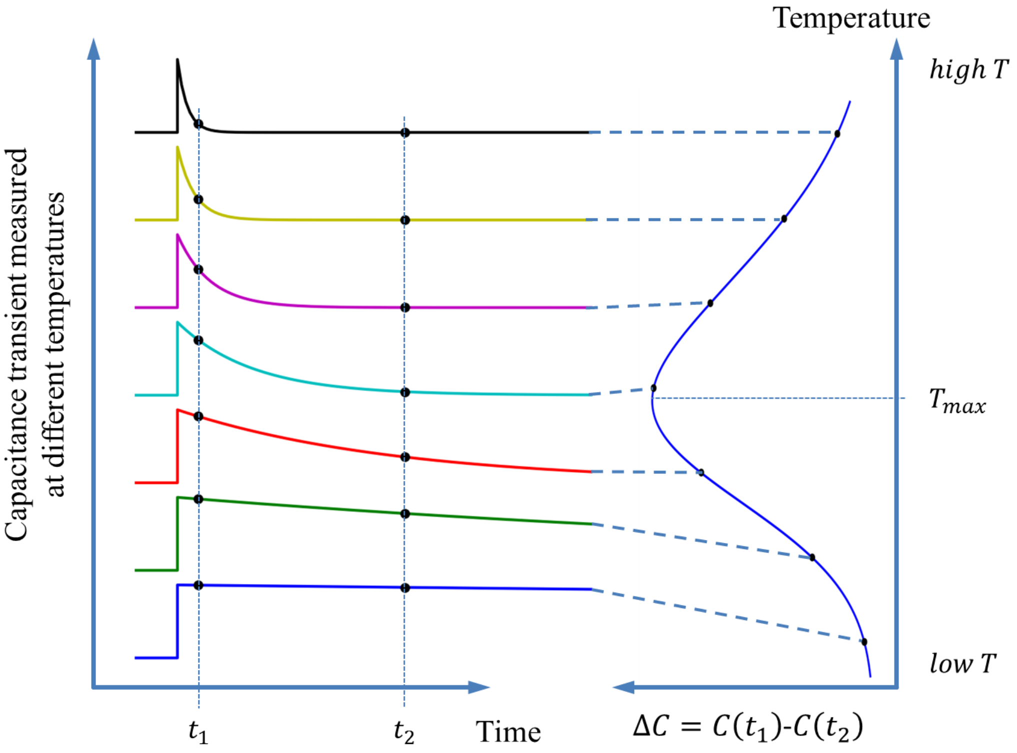


Figure 3.5. Difference in capacitance between two time points at various temperatures [113].

3.3.2 Fourier transform and DLTFS

❖ Fourier transform

Consider a digital system that scans the periodic analog signal $f(t)$ with the help of an analog-digital converter (ADC) in N discrete equidistant times and the sampling interval Δt. Thus the period width $T_W = N\Delta t$ contains N intervals and $N+1$ real values ($f_0, \ldots, f_N$).

For the continuous Fourier transform, the coefficients c_n of the Fourier series are:

$$c_n = \frac{1}{T_W} \int_0^{T_W} f(t) \exp(-in\omega_0 t)\, dt \tag{3.19}$$

with

$$\omega_0 = \frac{2\pi}{T_W} \tag{3.20}$$

and the corresponding cosine coefficients a_n and the sine coefficients b_n can be expressed as:

$$c_n = \frac{1}{2}(a_n - ib_n) \tag{3.21}$$

On the other hand, the continuous time-dependent signal $f(t)$ can be recorded and reconstructed by using the discrete sampling if the sampling law is fulfilled, and it exists the Discrete Fourier Transform (DFT) that:

$$F_n = \sum_{k=0}^{N-1} f_k \exp\left(-2\pi ink/N\right) \tag{3.22}$$

If it does not follow the trapezium rule that $f_0 = f_N$, the first term f_0 in Eq. (3.22) should be replaced by $(f_0 + f_N)/2$, and the discrete Fourier coefficients c_n^D are:

$$c_n^D = F_n/N \tag{3.23}$$

❖ DLTFS

In order to improve the basic DLTS method where two time points are preset, the Deep Level Transient Fourier Spectroscopy (DLTFS) has been put forward thanks to the Fourier transform [120]. Consider the transient signal that follows the exponential time law:

$$f(t) = Ae^{-\frac{t-t_0}{\tau}} + B \tag{3.24}$$

where A is the amplitude of transient, B the offset and τ the time constant, the coefficients can be expressed as:

$$a_0 = \frac{2A}{T_W} e^{t_0/\tau}(1 - e^{-T_W/\tau})\tau + 2B \tag{3.25}$$

$$a_n = \frac{2A}{T_W} e^{t_0/\tau}(1 - e^{-T_W/\tau}) \frac{1/\tau}{\frac{1}{\tau^2} + n^2\omega_0^2} \tag{3.26}$$

$$b_n = \frac{2A}{T_W} e^{t_0/\tau}(1 - e^{-T_W/\tau}) \frac{n\varpi_0}{\frac{1}{\tau^2} + n^2\omega_0^2} \tag{3.27}$$

These coefficients should relate to the corresponding coefficients obtained from Discrete Fourier Transform (DFT), which means that instead of the double boxcar function, all coefficients that contain the information of original transient signal can be calculated and analyzed.

Furthermore, the time constant can be deduced from the ratio of different coefficients such as:

$$\tau\left(a_n, b_n\right) = \frac{1}{n\omega_0} \frac{b_n}{a_n} \tag{3.28}$$

where neither signal amplitude nor offset are included in the expression any more.

3.3.3 HERA DLTS

Even though the maximum analysis of traditional DLTS and its corresponding Arrhenius plot is convenient with high accuracy on single trap analysis, large numbers of deep levels can lie closed to each other, given overlapped peaks on the traditional DLTS signal. As a result, apart from the maximum analysis, a series of mathematic tools such as Laplace transformation or multi exponential transient fit are involved in the High Energy Resolution Analysis (HERA) in order to improve the accuracy especially for separation of trap levels.

Backtracking to Eq. (3.14) which describes the capacitance transient from single level, if multi trap levels are involved in the same emission process, the capacitance should be calculated separately and thus the total response on capacitance is:

$$C(t) = C_0 - \sum_{i=1}^{N} \Delta C_i e^{-t/\tau_i} \tag{3.29}$$

where i represents the individual emission from each trap level and N is the maximum number of traps. Therefore if the transient curve that contains several trap emissions is recorded, it is possible to separate these individual processes and to calculate the corresponding time constant with the help of a proper mathematic tool for multi exponential fit.

On the other hand, thanks to Laplace transformation, Eq. (3.29) can also be expressed as:

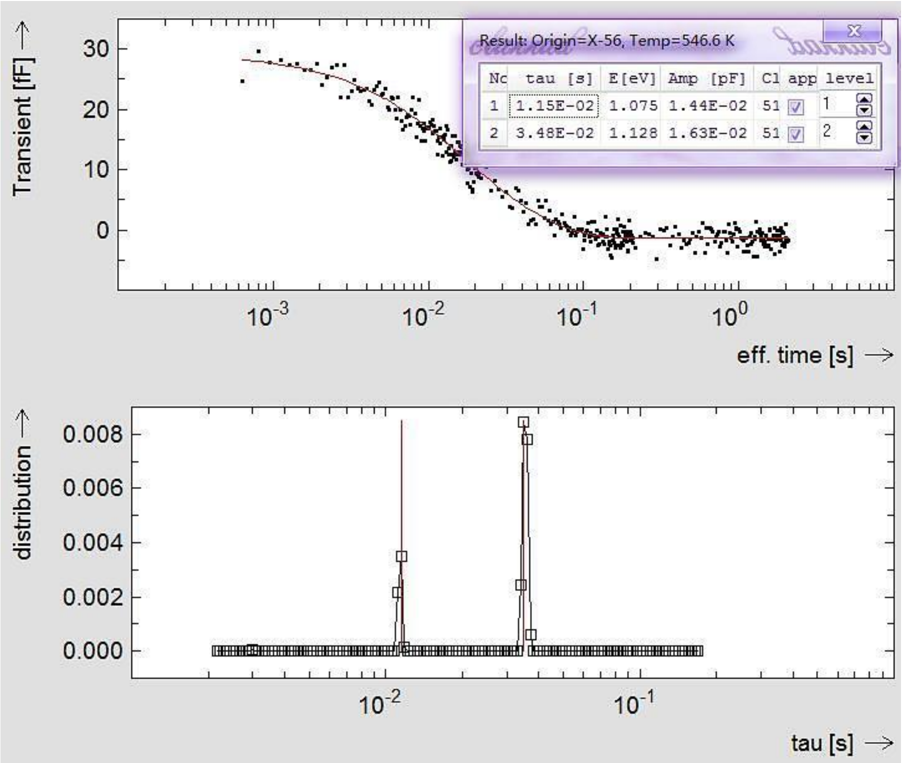
$$C(t) - C_0 = \int_0^{\infty} F(s) e^{-st} ds \tag{3.30}$$

where $F(s)$ is the spectral density function.

In this way, the resolution of analysis can be improved by more than an order of magnitude compared to the traditional one [119].

An example of HERA (Laplace) from our experimental DLTS system is given in Figure 3.6. Instead of analysis of the DLTS signal from whole temperature range, here the

Laplace analysis focuses on deconvolution of signal transient curve and two levels are obtained with their time constants and activation energies, and the fitted curve is in great accordance with original transient data. Therefore even if these two levels belong to a broad peak in conventional DLTS signal that can hardly separate, it is possible to distinguish them with the contribution of Laplace analysis.



Result: Origin=X-56, Temp=546.6 K

Nc	tau [s]	E[eV]	Amp [pF]	Cl	app	level
1	1.15E-02	1.075	1.44E-02	51	☑	1
2	3.48E-02	1.128	1.63E-02	51	☑	2

Figure 3.6. Original capacitance transient signal (upper plot) and its Laplace transform spectra (lower plot). Inner table lists the extracted parameters of two different levels, where their fitting curve is presented in the upper plot as solid line.

Unfortunately, as a noise signal is inevitably involved in the original transient signal, sometimes the HERA can be too sensitive and will identify those strong noise signal or fake levels as well, which can in turn affect the true trap analysis. As a consequence, the resolution or sensitivity should be properly chosen and set.

3.4 Category of DLTS

In the previous sections the DLTS principles have been introduced according to the capacitance transient. However, apart from the common capacitance DLTS (C-DLTS) mode, transients of current DLTS (I-DLTS), voltage DLTS (U-DLTS) or Charge DLTS (Q-DLTS) are all available with their advantages as the supplement of traditional C-DLTS measurement. On top of that, other types of DLTS mode such as Deep Level Optical Spectroscopy (DLOS) that is based on photostimulated capacitance transients measurements after electrical, thermal, or optical excitation [121] and optical current DLTS (O-I-DLTS) in order to fill both majority and minority carrier traps [122] have been reported as well.

On the other hand, isothermal DLTS measurement is another significant category that measures the transient at fixed temperature instead of the traditional DLTS Tempscan (DLTS temperature scan) method that records the transient signal in wide temperature range with a relative small interval (usually few Kelvins). With the help of isothermal DLTS, it is easier to characterize doping profile or capture cross section if the activation energies of trap levels have been investigated in advance.

3.4.1 DLTS transient modes

❖ **C-DLTS**

As the widely used DLTS mode, C-DLTS (or DLTS if not emphasized) benefits from its simplicity on both measure and analysis, and the sensitivity can be terrific when capacitance compensation is used in the DLTS system. However, it is hard to provide the accurate DLTS results if the resistance of the device under test is high [123]. Moreover, the freeze-out as introduced in 3.2.5 can be another drawback for C-DLTS to investigate those trap levels with tiny activation energies.

❖ **I-DLTS**

Current DLTS (I-DLTS) is a candidate for trap characterization in order to overcome those drawbacks mentioned with C-DLTS, which can be suitable for investigation on material with large resistivity [122]. Different from the capacitance transient described in Eq. (3.14), in the case of I-DLTS the current transient is:

$$I(t) - I_R = \frac{1}{2} q S w_R N_T \frac{1}{\tau_e} e^{-t/\tau_e} \tag{3.31}$$

As the time constant is also involved outside the exponential term, the amplitude of current transient is temperature depending, which adds up the complexity of analysis. Meanwhile, as the leakage is strongly depend on temperature, the noise of I-DLTS can be quite large which leads to inaccurate results at high temperature where considerable leakage current shows up especially on Schottky diodes. Moreover, the sensitivity of I-DLTS is also limited by the sensitivity of current measurement, which is normally lower than capacitance measurement.

❖ Q-DLTS

Even though similar as I-DLTS that current transients are measured at charge DLTS (Q-DLTS), these transients are calculated by numerical integration which overcomes the disadvantages that the amplitude is temperature dependent at I-DLTS. However, these integrations need correct information of current offset. Otherwise the signal will be overlapped by a linear noise signal which will ruin the useful information. In addition, it is a powerful tool for investigation on the structure with the high frequency capacitance that is independent of the charge state of either interface or bulk traps, that can be the case for MIS with Fermi level pinning [124]. As a result, Q-DLTS is active in bulk and interface traps characterization due to its relatively high sensitivity [125].

❖ U-DLTS

Voltage DLTS (U-DLTS), also known as Constant Capacitance DLTS (CC-DLTS), measures the voltage transient produced by trap emission when the capacitance is kept constant with the help of feedback loop to adjust the applied bias. Since the capacitance is kept constant, the investigation zone of the deep level traps is well defined and controlled during the measurement. As a result, it can rule out the refilling effect owing to the displacement of the space charge region edge while the C-DLTS fails [126].

However, due to the complexity of the measurement set up for U-DLTS where fast feedback and control system is necessary, it is not generally use for defect characterization. Furthermore, as the capacitance should depend on voltage in U-DLTS, this method is impossible to adapt to the region where C-V curve is flat, which can be the case on MIS samples under accumulation and deep inversion.

Table 3.1. Comparison of different DLTS modes from our DLTS manual, it marks with '+' as good, 'o' as medium and '−' as bad.

DLTS mode	**C**	**I**	**Q**	**U**
Sensitivity	+	−	o	o
Recovery time	−	o	o	−
Offset compensation	+	−	−	+
Measurement	+	+	o	o
Exponential	o	+	o	+
N_T calculation	+	o	o	+
N_T s, depth profile	o	−	−	+

❖ Comparison of DLTS modes

In short, the conventional C-DLTS offers high sensitivity and is suitable for most of trap characterizations. However, it is important to switch to I-DLTS or Q-DLTS when $N_T \ll N_S$ no longer holds. On the other hand, if the hardware permits, the U-DLTS can provide focus on specific region. The comparison on 4 DLTS modes from our DLTS manual is listed in Table 3.1.

3.4.2 Isothermal DLTS

The discussion on DLTS above mainly focuses on the DLTS Tempscan where transient curves are measured at different temperatures with wide range and small steps (e.g. 2~3 K). Therefore it is unrealistic to reach stable temperature at each measure point since too many transient are being recorded. As a result, a temperature difference is unfortunately introduced during each transient measurement (e.g. the ΔT for the transient with a measurement time of 10 s and temperature step of 2 K could be 0.2 ~ 0.6 K if no additional waiting time is applied). Even if this difference can be neglected for most of the trap identifications, it is wise to reduce that as much as possible when characterizing those sensitive traps. In that case, the isothermal DLTS can be quite convenient owing to its small ΔT (less than 0.1 K if the parameters are well set). In addition, the isothermal DLTS can improve the characterization on either capture cross section or profile of defect concentration under different variation modes.

3.4.21 Variation of period width

This period scan method namely Isothermal Transient Spectroscopy (ITS) is the most used method among isothermal measurements, which can investigate the trap levels with higher accuracy. Instead of the temperature scan used in Tempscan, ITS scans the period width T_W and records the transient of each T_W at a fixed temperature. After the period scan at several temperatures that are closed to the peak in the traditional Tempscan and with a relative large step (e.g. 10 K), the maximum analysis or HERA can be done for trap identification just as discussed in Tempscan. In order to locate the target temperature where the researched trap lies, a pre-Tempscan is always needed for ITS, which can be a drawback. However, ITS is rather significant for characterization on those traps sensitive to temperature variation.

3.4.22 Variation of pulse width

If pulse width T_P is chosen as the scan parameter with others parameters kept constant (including the period width), it is working at the DLTS mode with variation of pulse width. According to the variation step (linear or logarithmic), it can be used for either capture cross section calculation or trap identification.

- **Logarithmic variation of** T_P

When discussing the DLTS principle, the time constant of capture τ_c is assumed small compared to the common used T_P, which leads to the filling on all trap levels. However, this no more fulfills if T_P is comparable with τ_c or even smaller. In that case, the traps filled during the pulse n_{Tc} rises up with increase of T_P, which results in larger amplitude of the transient signal during emission. On the other hand, the point defect is likely to saturate with large T_P while those cluster traps such as dislocation can hardly saturate even at large pulse width and will still increase with the growth of T_P. Therefore, if the pulse width is scanned with a logarithmic width on a large range (e.g. from 10 nm to 10 ms), both trap type and the overlap (if exists) can be identified.

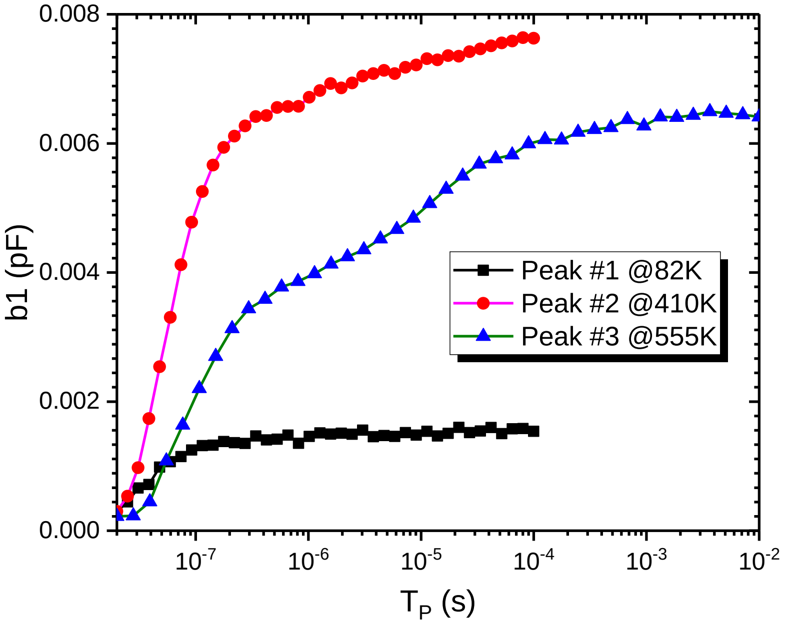


Figure 3.7. Isothermal DLTS signal (b1) with variation of pulse width logarithmically on 4H-SiC SBD with metal contact of tungsten. Three signals were measured at different temperature marked in the plot.

As an example, three signals measured at different temperatures are shown in Figure 3.7. Apart from the signal heights that are related to the trap concentrations, the trends of signals with increase of the pulse width are distinct. #1 that is measured at 82 K saturates with relative low T_P (200 ns) and then keeps constant, that indicates that it belongs to the point defect. On the other hand, the signal at 410 K rises up rapidly with T_P lower than 200 ns, and continue to increase at large T_P without any appearance of saturation. This is the feature of extended traps such as dislocation. On top of that, two regions can be identified from signal #3 with a demarcation point around 3 µs, which is suggested to be due to the overlapped trap levels. Therefore the isothermal DLTS with T_P variation on logarithm is a powerful auxiliary tool for trap identification.

- **Linear variation of T_P**

Call back to Eq. (3.1), if the pulse width is so small where $T_p \ll \tau_c$ exists, the capture process can be simplified as:

$$n_{Tc}(t) = N_T \frac{t}{\tau_c} \tag{3.32}$$

Since the signal height correspond to the occupied trap levels, in that case the plot amplitude vs. pulse width should be almost linear within certain region ($T_p \ll \tau_c$), and in turn the capture cross section can be determined from its slope.

3.4.23 Variation of bias voltage

As explained in DLTS principle, the effective zone of trap investigation is based on the depletion region under different bias, or in other words, is determined by the U_R and U_P values. Therefore it is possible to focus on certain region by selecting proper bias condition. Moreover, it is easy to draw the profile of trap concentration with the help of voltage scan, and this can be realized by the isothermal DLTS with variation of bias conditions. According to the sweep parameter, three modes are commonly available:

❖ **Variation of U_P**

Measure the transients at different U_P while U_R keeps constant. It is possible to calculate the trap concentration by the amplitude vs. U_P plot.

❖ **Variation of U_R**

Measure the transients at different U_R while U_P keeps constant. It is possible to calculate the trap concentration by the amplitude vs. U_R plot.

❖ **Variation of U_P and U_R**

U_P and U_R varies simultaneously with its difference $U_P - U_R$ keeps unchanged. The concentration profile is more intuitive at this mode.

3.4.3 Other DLTS

3.4.31 DDLTS

Double correlation DLTS (DDLTS) was first put forward by Lefevre et al. [111] as an improvement to conventional DLTS method. In order to rule out the field dependence of the capture cross section and those undesired effects in the contact area, a second pulse is used and its capacitance transient is measured and analyzed. Deep level profiles with low concentration (i.e. 10^4 times lower than the background doping) can now be determined thanks to DDLTS.

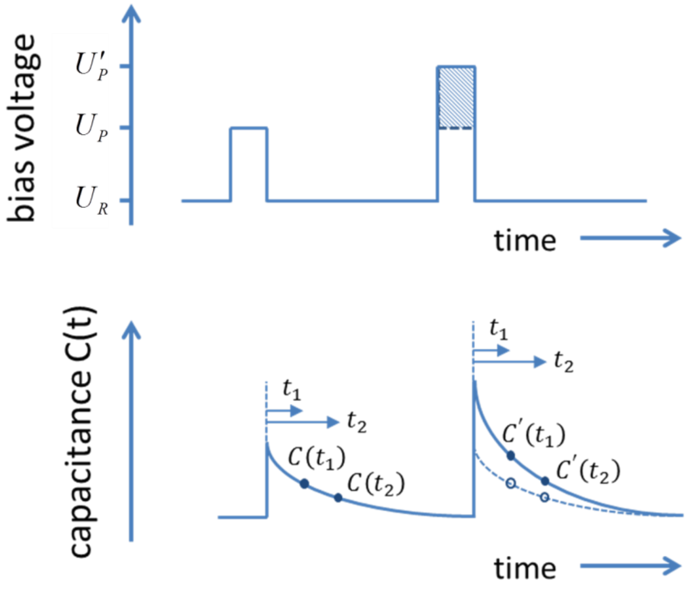


Figure 3.8. Schematic illustration of pulse shape and capacitance transient in DDLTS [111].

The principle of DDLTS is shown in Figure 3.8 as a two-step process [111]. 1) A normal pulse ($U_P - U_R$) is added as the conventional DLTS. If measuring the difference from capacitance transient namely $\Delta C = C(t_1) - C(t_2)$, the DLTS signal will be obtained. 2) A second pulse ($U'_P - U_R$) is adopted and its transient is measured where time t_1 and t_2 are fixed as the former one. By calculating the new correlation function which is $[C'(t_1) - C(t_1)] - [C'(t_2) - C(t_2)]$ or $\Delta C(t_1) - \Delta C(t_2)$, only those traps filled solely during the higher pulse will be observed.

Since the capacitance variation during DLTS are required to be large enough, even though DDLTS is similar as setting the reverse and pulse bias as U_P and U'_P, the signal-to-noise ratio is greatly improved. Another thinking is to present two conventional DLTS Tempscans with only difference of pulse heights U_P. In that case, similar signal will be obtained as the DDLTS when the difference of two Tempscans is calculated.

S. Loualiche also argued that when it comes to multi deep traps involving acceptor-like defects, modification should be done to the expression of trap concentration as given by Lefevre [110].

3.4.32 Developments on CC-DLTS

❖ CR-DLTS

The Constant Resistance DLTS (CR-DLTS) was first put forward by Plamen for MOSFETs characterization. Similar to the CC-DLTS, the CR-DLTS measure the voltage that keeps the conductance constant with the help of the feed-back system [127]. Compared to the CC-DLTS, only those traps inside space charge region that can be controlled by the gate are investigated. CR-DLTS is regarded as simple, sensitive and device area independent technique which is useful for characterization on FETs where the drain-source conductance can be affected by the charge emission [128].

- **CS-DLTS**

As a compromise between C-DLTS and U-DLTS, the Constant Space charge region DLTS (CS-DLTS) can avoid the setup problem with U-DLTS. Instead of keeping the capacitance constant by real time feed-back during transient of U-DLTS, the equilibrium or static values of capacitance of reverse bias and pulse voltage are set constant with variation of U_R and U_P. This can be simply realized by the lookup method with measuring the C_R and C_P in advance before each transient. As a result, even if the capacitance during the transient is never sure to be constant, it does benefit from U-DLTS method to some extent.

- **CC-DLOS**

If the idea of constant capacitance is applied in DLOS mentioned before, it comes up with the Constant Capacitance DLOS (CC-DLOS), which can be used for investigation on very deep interface states [129].

- **LT-CC-DLTS**

As a complement to the conventional CC-DLTS, the long-time constant-capacitance DLTS (LT-CC-DLTS) was introduced by Bassler which allows the use of remarkable long time constant that can be up to 1 h in practice [130].

Chapter 4
Experimental study on SiC SBD

4.1 Sample used in this study

4.1.1 Overview

Table 4.1. 4H-SiC SBD samples used in this study.

Label ID	Metal contact	Identification	T-annealing (℃)
S2	Ni	1000 Å	500
S3	Ti/W	lift-off	350
S4	Ti/W	sputtering etch 1 min	350
S5	Ti/W	sputtering etch 3 min	350
S6	Mo	lift-off	500
S7	W	barrier high	500
S8	Mo	etch	500

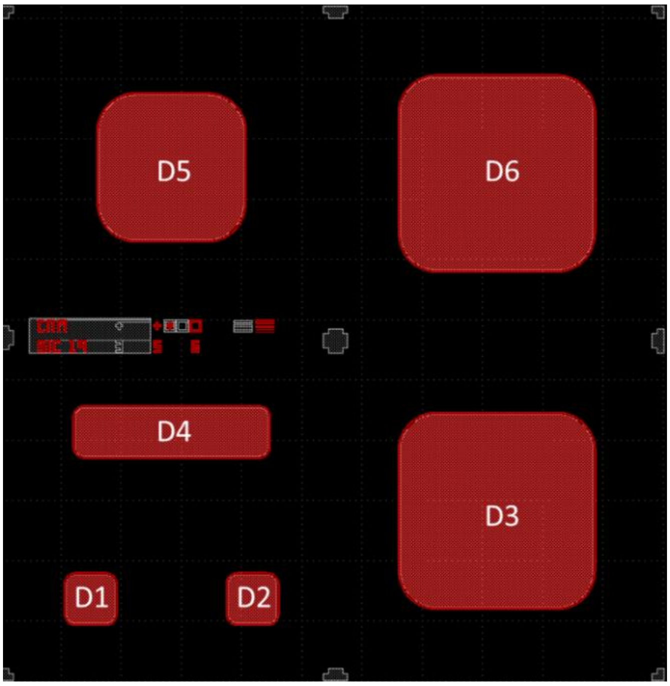


Figure 4.1. Map of cell of SBD samples, diodes within each cell are labeled from D1 to D6.

Seven SiC Schottky samples with 4 different metal contacts provided by our collaborator were fabricated under various conditions as listed in Table 4.1. Unfortunately, no further detailed information about fabrication process is available in addition to those listed in the column *Identification*. All samples are fabricated with the same cell illustrated in Figure 4.1, including 5 square diodes and 1 rectangle diode. The specific size parameters and surface information for each diode can be found in Table 4.2. Although all diodes were involved in a preliminary measurement (I-V and C-V characterization at room temperature), considering the DLTS installation where the metal probe is used as surface contact, further characterization and DLTS test only took place on those large diodes (D3 and D6) if no additional highlight is given in this study.

Table 4.2. Size parameters of diodes illustrated in Figure 4.1.

Diode ID	Size (µm)	Radius of curvature (µm)	Surface (mm2)
D1	400×400	75	0.155
D2	400×400	75	0.155
D3	1600×1600	300	2.48
D4	400×1600	75	0.63
D5	1200×1200	300	1.36
D6	1600×1600	300	2.48

4.1.2 Preliminary statistics

The primary I-V and C-V measurements have been done by using *ACS* software*, Keithley 2636A System SourceMeter, B1505A Power Device Analyzer* and the semi-automatic probe station. The primary parameters, especially ideality factor and Schottky barrier height were deduced based on either I-V or C-V results in order to locate those diodes with double barrier. As an example, Figure 4.2 presents the mapping of SBH on samples with three metal contacts. With the help of Python for data processing, those SBHs and ideality factors were calculated according to those formulas discussed in Chapter 2. Complete statistics for all samples are listed in Table 4.3. It is clear that diodes characteristics vary a lot from one to another, and could also be influenced by manufacturing process. Ni diodes always shows a multi-barrier phenomenon regardless of diode size, while those double barrier diodes have only been found on the smallest squares when it comes to the Ti/W liftoff sample. After the first characterization, samples are cut into small pieces for subsequent measurements, owing to the limited size of our characterizing system. Thanks to this mapping on preliminary measurements, those big diodes, especially the ones with double barrier phenomenon have been located, that is the main focus in the following characterization as discussed before.

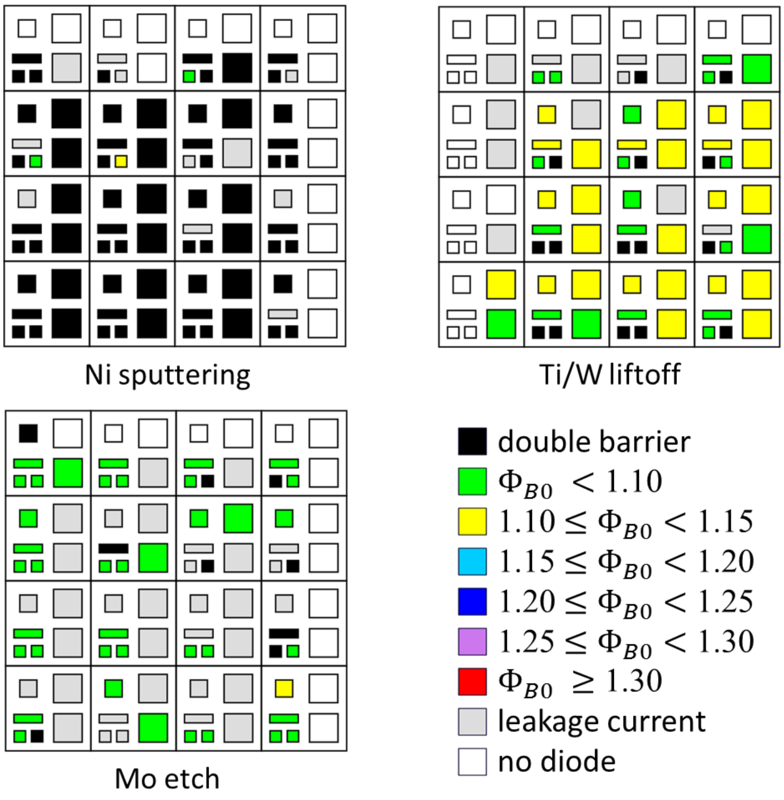


Figure 4.2. Mapping of barrier height on 3 SBD samples. Those marked "no diode" are lack of effective diodes due to wafer cutting.

Table 4.3. Statistics on each sample from the preliminary I-V charactrization.

Label	**Total diodes**	**High leakage current**	**Double barrier**
S2	80	10	67
S3	72	12	15
S4	67	18	28
S5	81	28	22
S6	64	22	10
S7	81	23	17
S8	82	33	9

4.2 Measurements setup

Due to relatively high series resistance and large temperature mismatch on DLTS system especially at high temperature, cryostat system is adopted for I-V and C-V measurements under wide temperature range in order to determine those electric parameters. On the other hand, various of DLTS tests have been taken out by DLTS system as well as I-V curves measured for qualitative analysis.

4.2.1 Hardware setup

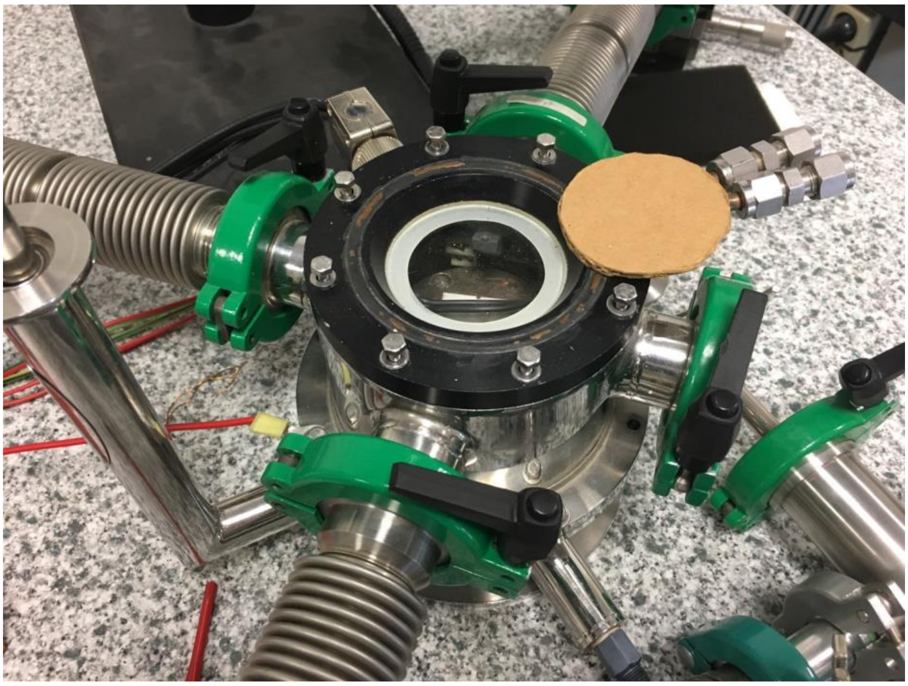


Figure 4.3. Cryostat system used for I-V and C-V measurements.

- **Cryostat**

As illustrated in Figure 4.3, samples were set in the vacuum cryostat and insulated by a potassium aluminosilicate plate. Silver lacquer was used to paste the sample on the plate in order to make back-contact and ensure good thermal conductivity. I-V and C-V characteristics were measured with *Keithley K2410* and *Keysight E4990A Impedance Analyser* by four-point measurement. Temperature was automatically and accurately controlled with liquid nitrogen and input heater adjusted by the temperature value measured by *PT100*. All measure has been performed in the dark to rule out the influence of light.

- **DLTS**

The DLTS tests have been realized with FT-1230 HERA DLTS (High Energy Resolution Analysis Deep Level Transient Spectroscopy) system by PhysTech. As shown in Figure 4.4, samples are kept in dark vacuum as that in cryostat. Meanwhile, samples are isolated and pressed by ceramic plate in order to enhance the thermal contact and finally high accuracy was achieved on measured temperature. However, large temperature mismatch has still been found at high temperature especially over 600 K. Unlike the four-point measurement described above, only two contacts are used for DLTS that will inevitably induces additional series resistance around 100 Ω in this case. However, since our attentions are drawn on transient of capacitance and the compensations are taken out, this series resistance could be ignored during DLTS characterization.

Capacitances are measured by Boonton 7200 capacitance meter in DLTS system, with 4 ranges of 2 pF, 20 pF, 200 pF and 2000 pF for static measures and can achieve the accuracy of fF class during the transient measurement thanks to the compensation system.

The bias and pulse source are controlled by the software within a range of –20 V to +20 V with a resolution of 1mV, and can be extended to –100 V or +100 V if height voltage module is used.

The current resolution is 10 pA for measuring current or current transient by the DLTS system, with 5 different range of 1 µA, 10 µA, 100 µA, 1 mA and 10 mA. Therefore the current limit during DLTS test is limited to 10 mA. However, this current limit can hardly be reached owing to the existence of series resistance.

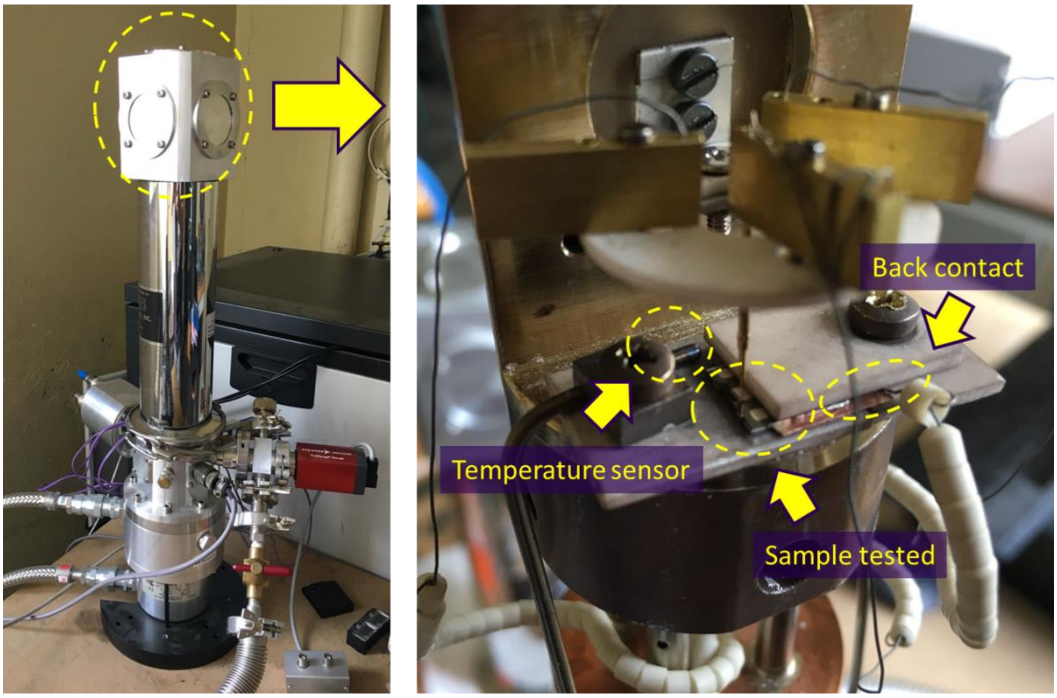


Figure 4.4. DLTS test system (left) and its inside view on head part for sample installation (right).

4.2.2 I-V measurements

- **Cryostat**

Owing to the temperature limitation of liquid nitrogen, I-V measurements in the cryostat are limited to 80 K at cryogenic temperature, while a maximum of 400 K is adopted with a step of 20 K. Forward characteristics were measured every 0.01 V with a limitation of 30 mA which is high enough for the study on linear region of the diodes. Meanwhile, reverse characteristics were measure from 0 V to –40 V with a step of 1 V. However, leakage current would not be used for calculation but only to filter diodes with high leakage current due to the sensitivity limitation on *Keithley K2410*.

- **DLTS**

Same voltage step is adopted for the current measurement by using the DLTS system. However, as the existence of high series resistance discussed before, the DLTS software will recalculate the voltage applied directly on sample. As a result, the current is usually lower than 10 mA with the converted sample voltage limited to a certain value rather than input value. (e.g. when the voltage applied is 1.5 V, the sample voltage could be only 1.1 V due to the series resistance.)

For those I-V curves measured during DLTS scan, the step is around 20 K when temperature is higher than 150 K, and becomes shorter at lower temperature. (see 4.2.4)

4.2.3 C-V measurements

- **Cryostat**

Same temperature range and step as I-V measurements were adopted for C-V characteristics performed in the cryostat. Applied voltage varies from 0 V to –10 V with a frequency of 100 kHz to examine the linear performance on the plot of $1/C^2$ vs. V , while only those data with bias form 0 V to –5 V are used for calculation in order to improve the accuracy.

- **DLTS**

The C-V measurements were usually taken out between –10 V and 0 V with a step of 0.25 V under 1 MHz AC signal in DLTS system. However, C-V curves measured with DLTS are not used for parameters extraction but only for providing an intuitive impression, especially the measured C_R and C_P during DLTS scan.

4.2.4 DLTS measurement

Due to the freeze-out effect which will be discussed in section 5.3.1, the conventional capacitance DLTS scan mainly took place at relevantly high temperature, while current DLTS took charge of the rest part. On top of that the isothermal DLTS measurement was also used especially for researches under extremely low temperature.

❖ Capacitance DLTS

Due to huge experimental error between sample temperature and the value measured by sensors in DLTS, C-DLTS was typically used between 200 K and 550 K with 3 windows (T_W) in order to extract those energy levels from either Arrhenius plot for maximum search or HERA analysis. The main measurement parameters are listed in Table 4.4. Furthermore, under certain circumstances, 60 K could be a possible start of scan for signal comparison.

Table 4.4. Typical parameters used for capacitance DLTS scan.

DLTS parameters	Value(s)
Pulse width T_p (μs)	100
Reverse bias U_R (V)	–10
Pulse voltage U_P (V)	–0.1
Period width T_W (ms)	20.48, 204.8, 2048

❖ Current DLTS

Same DLTS parameters were used for I-DLTS with the temperature range of 20 K to 60 K. However, T_W was limited to 2.048, 20.48 and 204.8 ms rather than that listed above due to high noise results from large T_W between 70 K and 170 K.

Table 4.5. Common isothermal DLTS modes.

Type	Description	Function
T_p (lin)	T_p varies with a linear step	Determine σ_S
T_p (log)	T_p varies with an exponential step	Defect overview
T_W	T_W varies with an exponential step	Defect analysis
U_R	U_R varies with fixed U_P	Defect profile
U_P	U_P varies with fixed U_R	Defect profile
$U_P - U_R$	U_P and U_R varies with fixed $U_P - U_R$	Defect profile

❖ Isothermal DLTS

Different from DLTS temperature scan (C-DLTS or I-DLTS), the isothermal DLTS measurement will improve the accuracy by fixing the test temperature. Common modes used are explained in Table 4.5.

Apart from those listed above, the period scan (variation of T_W) could be done at distinct temperature of with different parameter variation (e.g. U_P). This will be discussed in specific section.

4.3 Experimental results

4.3.1 Case study: Ti/W liftoff sample

4.3.11 Statistic measurements

❖ **Forward I-V characteristics**

The forward I-V curves of the diode Ti/W liftoff is shown in Figure 4.5 in a wide temperature range (80 K to 400 K). Considering the existence of series resistance, maximum current is limit to 0.01 A in the figure in order to highlight the linear region where we pay attention. It is clear that the forward I-V curves keep linear over whole studied temperatures.

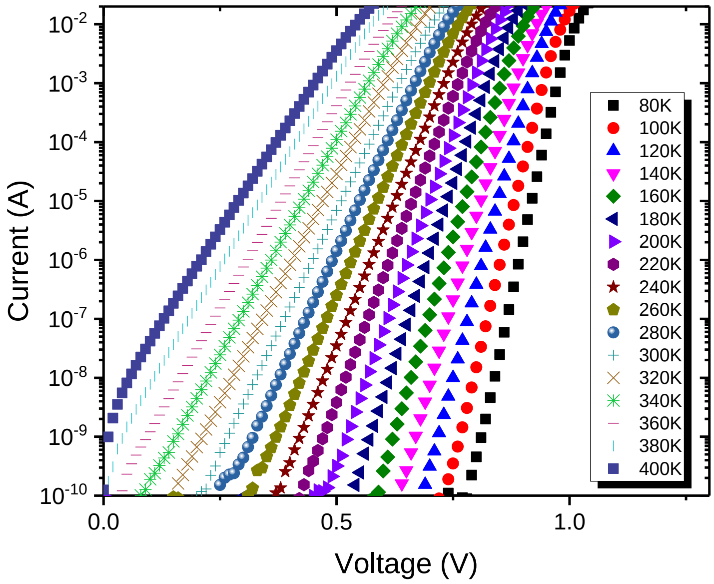


Figure 4.5. Forward I-V characteristic on diode Ti/W liftoff.

❖ **C-V characteristics**

Results calculated according to the C-V characterization within the same temperature range are illustrated in Figure 4.6. Even though the shallow doping concentration rises up with the increase of the temperature, the total shift is rather limited ($\approx 1\%$) except the value around 80 K, where an obvious gap shows up due to carrier freeze-out. Meanwhile, the SBH by C-V is somewhat symmetric with a maximum around 250 K.

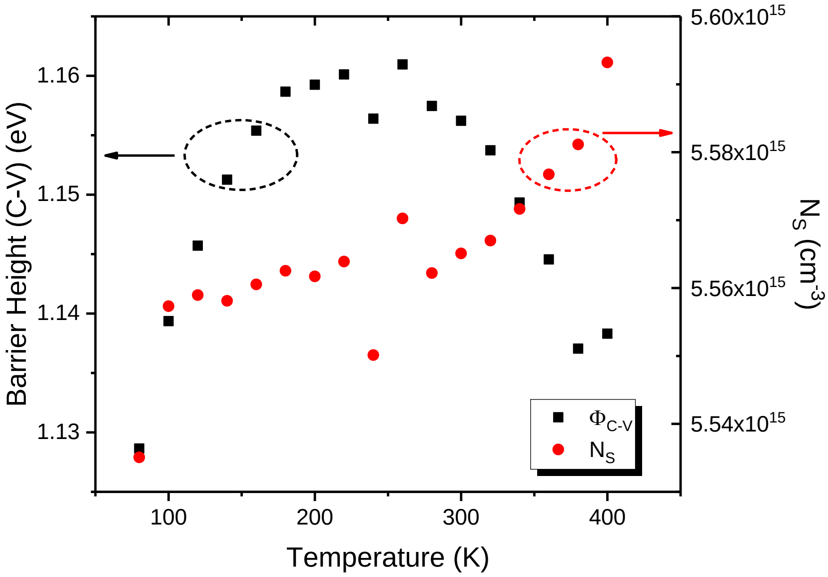


Figure 4.6. Calculated Schottky barrier height and shallow doping concentration on Ti/W liftoff diode based on C-V characterization.

❖ Conventional Richardson plot & modified Richardson plot

In order to obtain the effective Richardson constant, Richardson plot (Figure 4.7) is drawn thanks to the saturation current calculated with forward I-V characterization based on Eq. (2.21). Even the points could be linear at high temperature on this plot, the deviation becomes distinct at low temperature. Furthermore, the calculated Richardson constant is too small compared to the theoretical value, and so is the SBH according that from C-V.

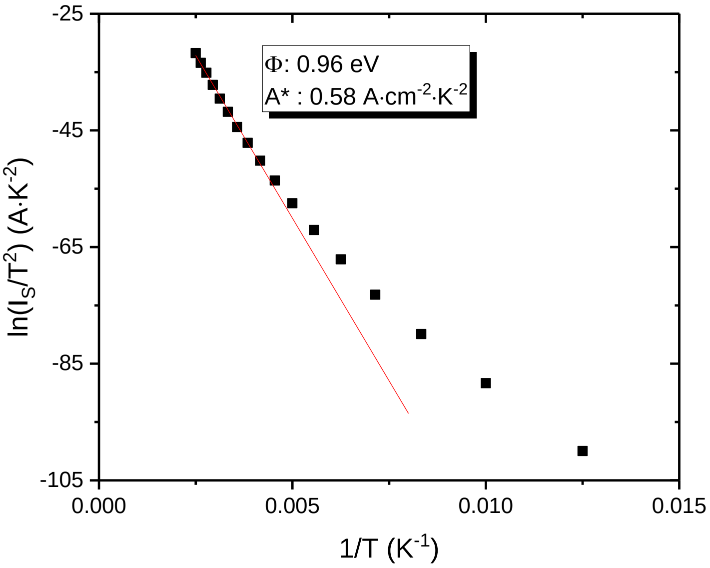


Figure 4.7. Richardson plot on Ti/W liftoff diode.

On the other hand, the modified Richardson plot based on Eq. (2.28) and its modification relates to the flat-band barrier height according to Eq. (2.37) could be drawn, as shown in Figure 4.8, thanks to those values obtained from I-V and C-V characterization.

The Richardson plots are much more linear on both modifications over whole temperature, with a reasonable value of SBH closed to that calculated from C-V. Moreover, the modified Richardson plot based on Φ_{BF} is more linear fitted with R^2 = 0.99999 compared to that of the conventional modified Richardson plot R^2 = 0.99995. Taking into consideration the more reasonable value of Richardson constant, the modified Richardson plot based on Φ_{BF} functions better and will be adopted as main tool for extraction of effective Richardson constant in this work.

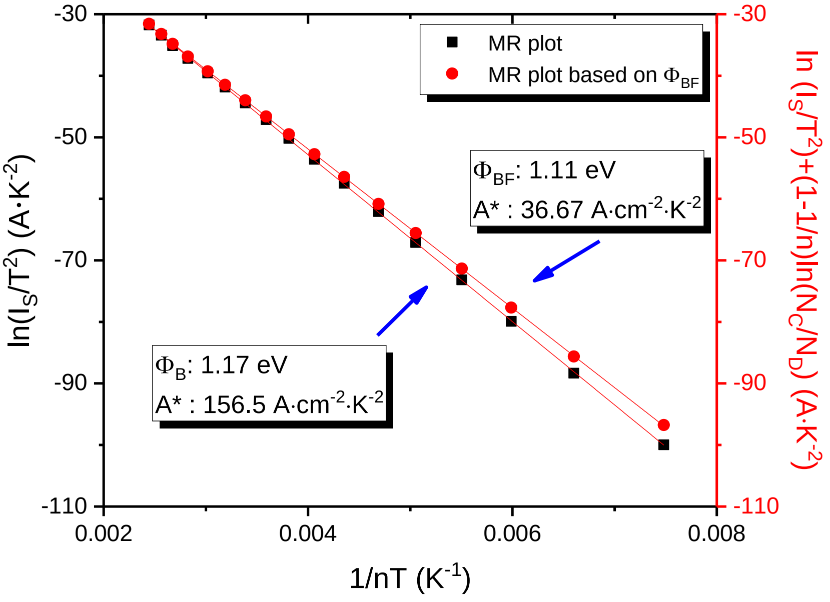


Figure 4.8. Modified Richardson plot and its modification based on flat-band barrier height.

❖ Gaussian distribution model and potential fluctuation model

According to the effective Richardson constant obtained (A^* = 36.67 A·cm^{-2}·K^{-2}), the zero-bias barrier height could be extracted at each temperature based on Eq. (2.27). Meanwhile, those variables of Gaussian distribution model (section 2.4.3) and potential fluctuation model (section 2.4.4) are possible to determine. As shown in Figure 4.9, both calculated values stay linear from 120 K to 320 K, with those main parameters marked beside the fitting lines. Regarding the relationship of these two model discussed in section 2.4.7, if we adopt Φ_{BF} above, the calculated $\bar{\Phi}_{B0}$ and σ_{S0}^2 are 1.24 eV and 0.009 V^2 based on Eq. (2.46), which is rather closed to the value directly from the Gaussian distribution model (1.25 eV and 0.01 V^2). Owing to the convenience and high accuracy, the potential fluctuation model where only ideality factor n is desired is mainly adopted for further characterization.

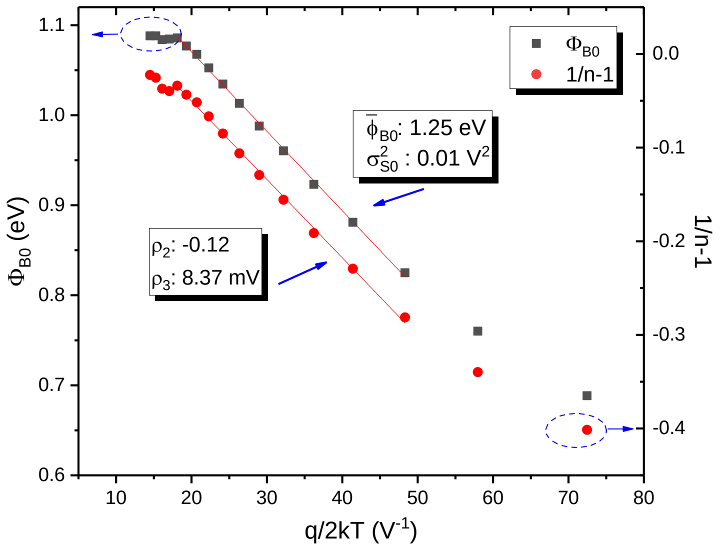


Figure 4.9. Zero-bias barrier height Φ_{B0} *and* $1/n-1$ *as a function of* $q/2kT$ *.*

❖ Discussion

After recalculating Φ_{BF} at each temperature based on Eq. (2.37), the barrier heights determined by different models are compared in Figure 4.10. The $n\Phi_{B0}$ values are closed to Φ_{BF} , and their differences are tolerable even under low temperature, that well explains the perfect linear fitting even in the conventional modified Richardson plot as discussed before. All values are approach and almost keep constant over the temperature range studied except Φ_{B0}, and as a result, the simple zero-bias barrier height Φ_{B0} is not generally recommended for SBH determination.

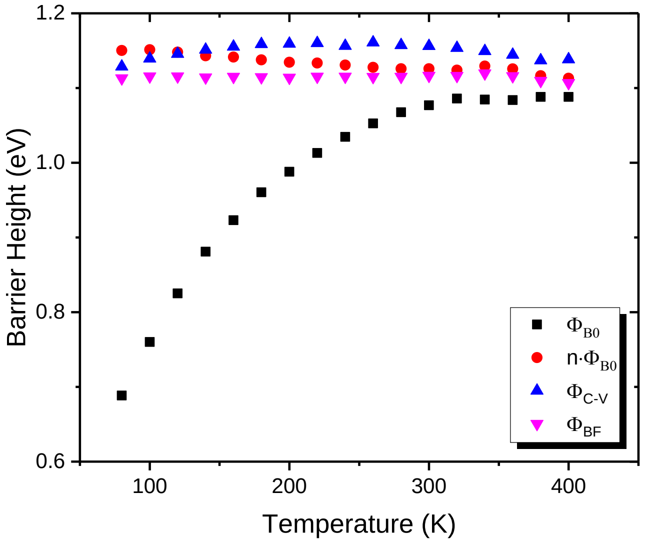


Figure 4.10. Comparison of zero-bias barrier height Φ_{B0}*,* $n\Phi_{B0}$*, SBH determined by C-V* Φ_{C-V} *and flat-band barrier height* Φ_{BF} *.*

4.3.12 DLTS results

DLTS scans have been taken out after statistic measurements. In order to relieve the influence due to freeze-out effect (discussed in 5.3.1), the I-DLTS was adopted for low temperature region (below 200 K) instead of conventional DLTS measurement that takes charge of higher temperature part.

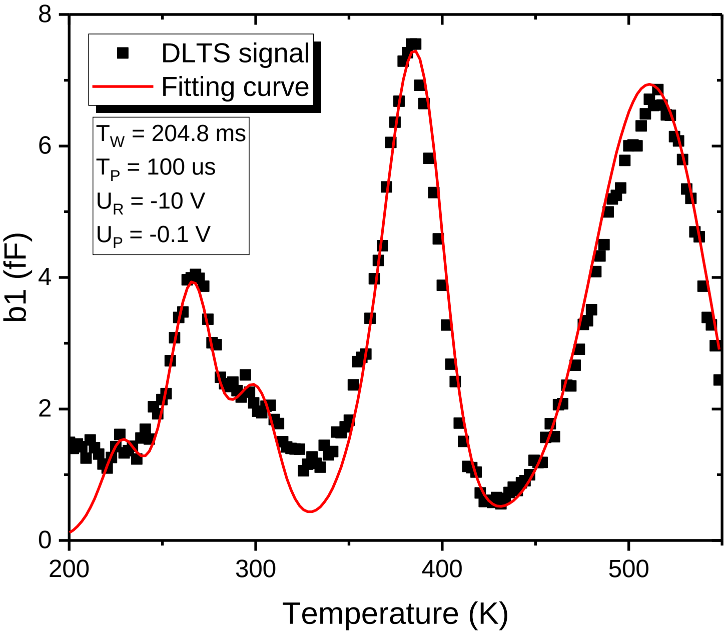


Figure 4.11. DLTS signal (correlation b1) and the simulation fitting curve according to the parameters of 6 trap levels extracted by Arrhenius analysis list in Table 4.6 on Ti/W liftoff diode between 200 K and 550 K.

Figure 4.11 illustrates the capacitance DLTS signal at high temperature region. 3 peaks can clearly be distinguished (260 K, 380 K and 510 K) while a fourth one shows up at around 300 K in the form of shoulder. With the help of correlation functions based on Fourier Transform, different deep levels could be identified as shown in Table 4.6, and the simulating results is shown as the red line in Figure 4.11 according to those extracted trap levels. Most of the defect levels are well fitted especially the highest peak, except the one around 295 K, that shows up as a shoulder of the higher peak at 265 K. In addition to the often reported $Z_{1/2}$ defects, the defect level at around 385 K with the highest concentration detected is close to the one labeled as NB center. Meanwhile, the peak over 500 K is analyzed as double defects with energy levels approaching 1 eV. Even though a sixth defect level marked EH1 shows up at 227 K, no obvious peak locates from the signal of correlation b1 and the concentration is rather low compare to other defects. In this case, existence of noise can be foreseen that will reduce the accuracy from the Arrhenius analysis. It needs to be pointed out that except the famous $Z_{1/2}$, the origins of other defects found are not clearly identified to the best of author's knowledge.

Table 4.6. Calculated deep level parameters based on Arrhenius plot by DLTS measurement between 200 K and 550 K and those interpretations. The defects are indicated by the position of the positive peak shown in Figure 4.11.

T (K)	$E_C - E_T$ (eV)	σ (cm^2)	N_T (cm^{-3})	Interpretation	Reference
227	0.470	1.45×10^{-15}	4.21×10^{11}	EH1	[131]
265	0.514	2.36×10^{-16}	1.16×10^{12}	$Z_{1/2}$	[62, 132-134]
295	0.602	4.25×10^{-16}	7.19×10^{11}		
385	0.794	4.74×10^{-16}	2.35×10^{12}	NB center	[135]
515	0.945	4.89×10^{-17}	9.99×10^{11}	$RD_{1/2}$	[25, 132, 133]
515	0.995	4.00×10^{-17}	1.62×10^{12}		

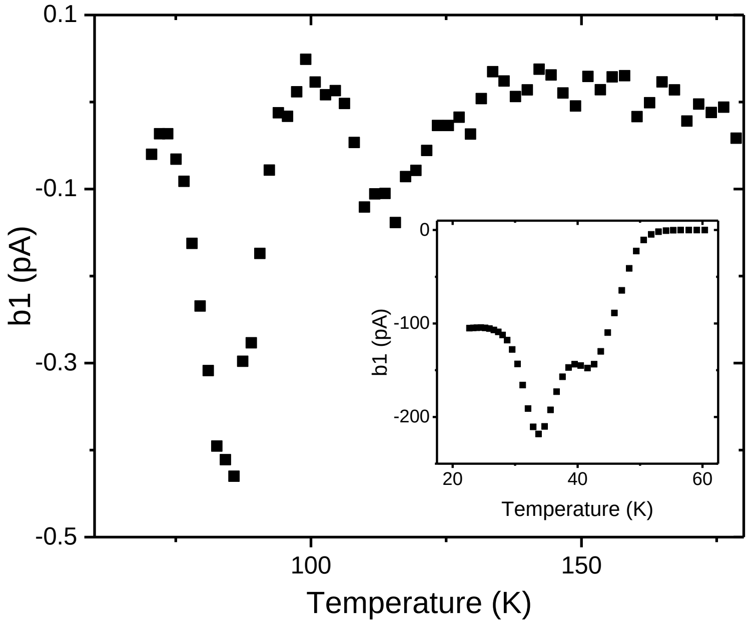


Figure 4.12. Current DLTS (I-DLTS) signal (correlation b1) on Ti/W liftoff diode from 70 K to 170 K and between 20 K and 60 K (inner plot), with a period width of 204.8 ms.

On the other hand, four defect levels as negative peaks illustrated in Figure 4.12 are recognized and the analysis results are listed in Table 4.7. The two highest peaks with largest defect concentrations result from nitrogen level, which is the shallow level of doping in this case. However, the energy level around 0.15 eV could not attribute to those levels reported even though the concentration is too high to be ignored.

Table 4.7. Calculated deep level parameters based on Arrhenius plot by I-DLTS measurement between 20 K and 170 K and those interpretations. The defects are indicated by the position of the negative peak shown in Figure 4.12.

T (K)	$E_C - E_T$ (eV)	σ (cm^2)	N_T (cm^{-3})	Interpretation	Reference
35	0.074	7.39×10^{-13}	7.81×10^{13}	N	[24, 70, 136]
42	0.083	4.65×10^{-14}	5.35×10^{13}		
83	0.149	8.46×10^{-16}	1.44×10^{13}	\	\
115	0.246	4.79×10^{-14}	6.09×10^{11}	Metal impurities	[23]

4.3.2 Research on diode with multi-barriers

4.3.21 Mo-etch samples

❖ **Forward I-V characteristics**

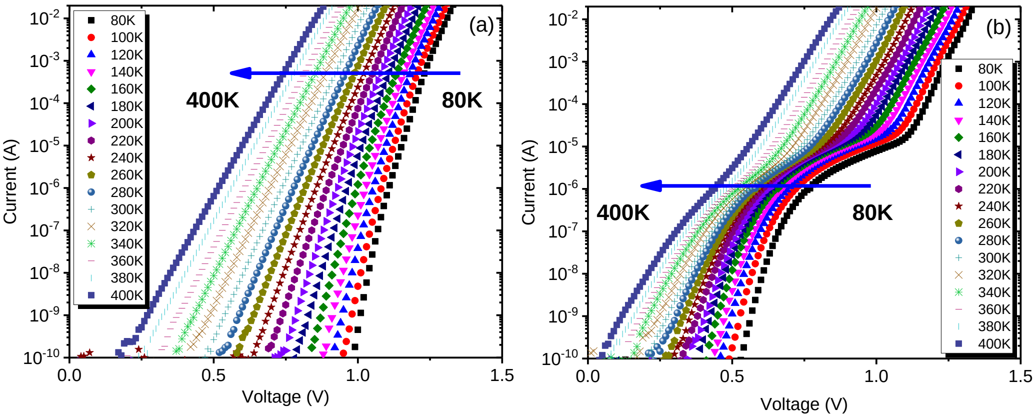


Figure 4.13. Forward I-V characteristics on two diodes (a) and (b) of Mo-etch samples.

Two diodes of Mo-etch with the largest surface were characterized and labeled diode (a) and (b). As shown in Figure 4.13, the characteristics log(I)-V of diode (a) are almost linear over the entire temperature range. On the contrary, for the diode (b), the I-V curves clearly show a phenomenon of multi-barrier, especially at low temperature. Indeed, under high current (> 10 µA) even at 80 K, log (I)-V still keeps linear as for diode (a). While under low voltage, the current is abnormally strong compared to the diode (a), although its variation log (I) vs. V is also linear up to about 100 nA. Such multi-barrier behavior has been observed by Gelczuck et al. [19] who attributed these two parts of the I-V curve to inhomogeneity of barrier height, low SBH L-SBH and higher SBH H-SBH. In this case, the log(I)-V characteristics can be divided into two linear regions, each giving a coefficient of ideality and a saturation current extracted from equations (2.26) and (2.27).

❖ C-V characteristics

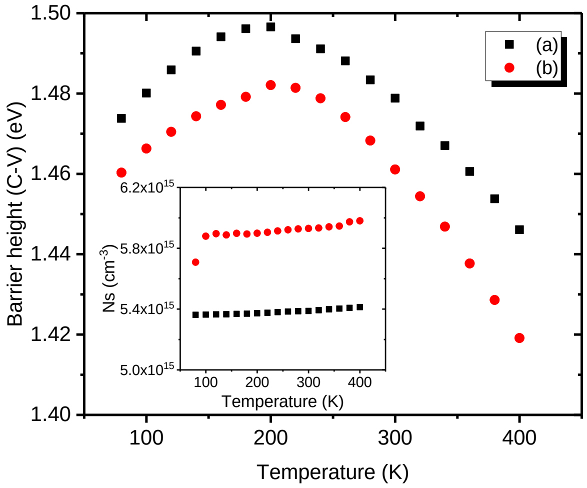


Figure 4.14. Calculated SBH Φ_{C-V} based on C-V characterization. Inner plot shows the extracted doping concentration.

Figure 4.14 shows the barrier height and doping concentration extracted from C-V as a function of temperature. Φ_{C-V} has a maximum of about 200 K, that is similar as that of the Ti/W liftoff sample. On the other hand, doping increases very slightly with temperature except at 80 K that may be due to experimental errors.

❖ Modified Richardson plot

Although the I-V curves appear linear throughout the temperature range for diode (a), the modified Richardson (MR) plot [Figure 4.15(a)] shows two distinct regions: between 80 and 200 K, Φ_{BF} = 1.20 eV and between 220 and 400 K Φ_{BF} = 1.50 eV. Diode (b) [Figure 4.15(b)] has similar barrier heights (1.30 eV between 80 and 160 K, and 1.59 eV between 300 and 400 K). Furthermore, an additional lower barrier height Φ_{BF} = 0.67 eV can be recognized over the entire temperature range (80 – 400 K). This lower barrier height is responsible for the excess current at low temperature on (b). A^* was also calculated in each linear region of the MR plot using the diode surface S , and the value obtained is used for subsequent calculations. Another solution would be to use a constant value A^* (the high value extracted, 1.50 eV), and to calculate a ratio between the areas of the high and low SBH regions. The A^* values are substantially different from several orders of magnitude in different regions, which indicate the surface ratio could be rather small for L-SBH region. Even for a ratio of 5.7×10^{-10} (area of the low SBH on the total surface of the diode), its influence on the I-V characteristic cannot be neglected.

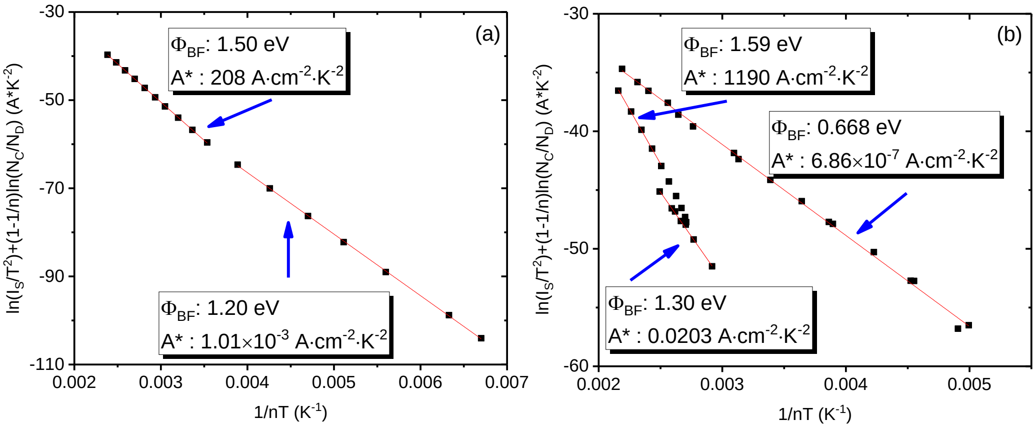


Figure 4.15. Modified Richardson plot based on the flat-band barrier height Φ_{BF} on diode (a) and (b). n and I_S were calculated in the different linear zones of the I-V curves.

For the transition zone between 180 K and 280 K on the diode (b), which can result from the coexistence of two different barriers, the value used for further calculation is that obtained at high temperature.

❖ Potential fluctuation model

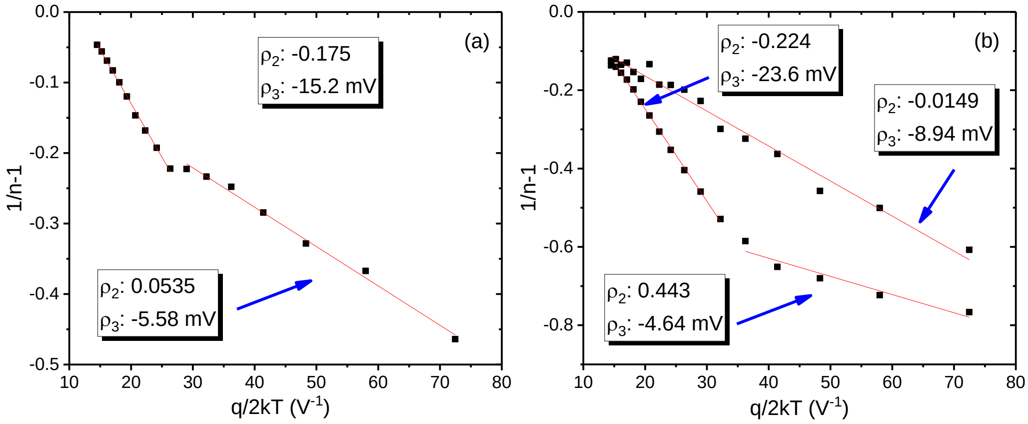


Figure 4.16. $1/n-1$ as a function of $q/2kT$ on diode (a) and (b).

Figure 4.16 shows the experimental plot of $1/n-1$ vs. $q/2kT$. The values of ρ_2 and ρ_3 are obtained from the slope and the intercept of each linear region. It is clear that these separated linear regions are similar to that determined by modified Richardson plot above even though ideality factor is merely analyzed in this model, which has proved the accuracy of these two models.

Parameters of Gaussian distribution have also been extracted based on the corresponding plot. Mean barrier heights and standard deviations calculated according to Eq. (2.46) are given in Table 4.8, as well as the other parameters used in these two models.

The calculated $\bar{\Phi}_{B0}$ and $\bar{\Phi}'_{B0}$, σ^2_{S0} and σ'^2_{S0} values are in good agreement, which means it functions well even on those diodes with multi-barrier, especially for diode (a). On the diode (b) the slight disagreement could come from the errors related to the linear approximations of the experimental curves or to the approximation of the Eq. (2.43).

Table 4.8. Comparison of the parameters of the Gaussian model and the potential fluctuation model. The two parameters $\bar{\Phi}'_{B0}$ and σ'^2_{S0} are calculated from the Eq. (2.46) with extraction of the MR plot of Figure 4.15.

Diode	Φ_{BF} **(eV)**	ρ_2	ρ_3 **(mV)**	$\bar{\Phi}_{B0}$ **(eV)**	σ^2_{S0} **(V^2)**	$\bar{\Phi}'_{B0}$ **(eV)**	σ'^2_{S0} **(V^2)**
(a)	1.50	−0.175	−15.23	1.75	0.021	1.76	0.023
	1.20	0.0535	−5.58	1.17	0.0068	1.14	0.0067
(b)	1.59	−0.224	−23.57	1.92	0.034	1.95	0.037
	1.30	0.443	−4.64	0.81	0.0066	0.72	0.0060
	0.67	−0.0149	−8.94	0.73	0.0067	0.68	0.0060

❖ DLTS

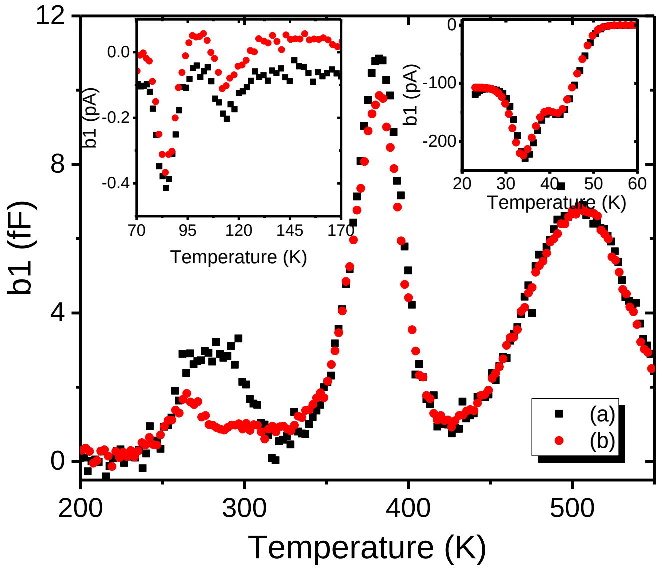


Figure 4.17. DLTS signal (correlation b1) with a period width of 204.8 ms on the diodes (a) and (b) of Mo sample between 200 K and 550 K. The inserts are I-DLTS spectrum between 20 K and 60 K (top right) and 70 K to 170 K (top left).

Figure 4.17 shows the DLTS spectra of the diodes obtained after their I-V and C-V characterizations. In order to avoid an annealing effect due to the temperature ramp, a fast preliminary DLTS scan was carried out on the two diodes (from 300 to 550, then back to 300 K for a total time of 3 hours). The I-DLTS spectra are dominated by two negative peaks between 70 and 170 K, and two other peaks below 60 K, which are similar as the spectra obtained on Ti/W liftoff sample (Figure 4.12), and so are the DLTS results on high temperature part. All deep levels found on Mo diodes have the values and their origins similar as that discussed on diode Ti/W liftoff (Table 4.6 and Table 4.7). Meanwhile, as can be seen in Figure 4.17, the DLTS results are rather similar between the two diodes, with the exception of the peak around 280 K. Considering the uncertainties inherent in the Arrhenius analysis, the energies extracted for this peak are very close to each other, which means that the defects observed are common to the two Mo diodes.

4.3.22 Ti/W sputtering 1 min samples

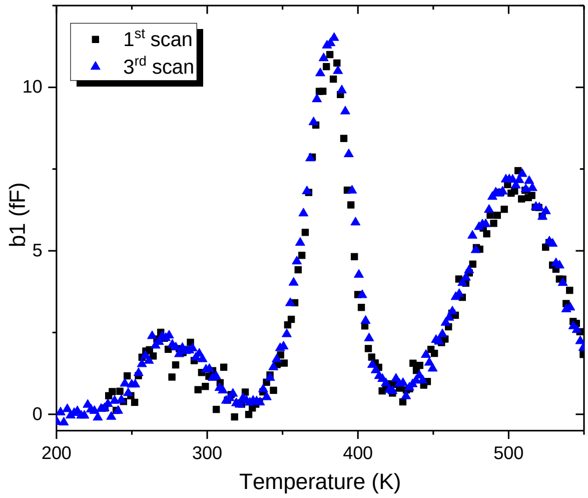


Figure 4.18. DLTS signal (b1) with a period width T_W = 204.8 ms of different scan cycles on Ti/W sputtering 1 min diode (A).

During DLTS study, several temperature scans could be applied on the same diode, for example the diode (A) of Ti/W sputtering 1 min sample shown in Figure 4.18. Even with almost the same results on DLTS spectra, the I-V characteristics could be rather different, as illustrated in Figure 4.19. Considering that samples are reserved in the vacuum dark chamber of DLTS system, the evolution of I-V characteristic could only be attributed to the multi DLTS scan applied.

In order to study the origin of this I-V characteristic evolution, DLTS temperature scan and Isothermal DLTS tests have been applied on another diode (B) of Ti/W sputtering 1 min sample, as listed in Table 4.9, by tracking the deep level defects and defect levels with tiny activation energy. Meanwhile, pure temperature treatments with small bias that could be neglected have also been adopted during the test targeting on research on high temperature annealing effect as well as annealing at room temperature.

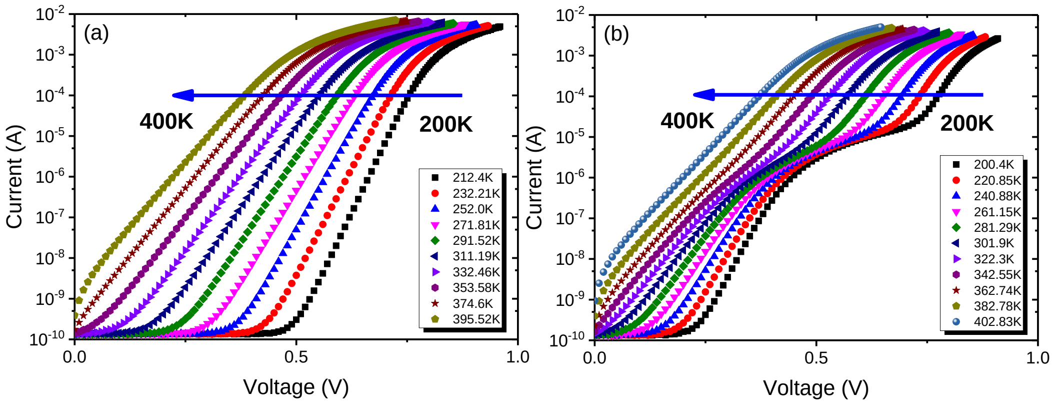


Figure 4.19. Forward I-V characteristic on diode (A) of Ti/W sputtering 1 min between 200 K and 400 K measured during the DLTS test of (a) : 1st scan and (b) : 3rd scan illustrated in Figure 4.18.

Table 4.9. Measure steps and addition condition on diode (B) of Ti/W sputtering 1 min sample. General measure condition of I-V and DLTS temperature scan are given in section 4.2, while that of Isothermal DLTS tests are illustrated in Figure 4.23.

Step	Measure	Temperature (K)	Condition	Label
1	Isothermal DLTS	17.5	\	ITS-0
2	I-V	60	\	IV-0
3	DLTS scan	60 – 300	2.5 h	Tempscan-1
4	I-V	60	\	IV-1
5	Annealing	550	AC track signal, 200 min	\
6	I-V	60	\	IV-2
7	Isothermal DLTS	17.5	\	ITS-1
8	DLTS scan	60 – 300	2.5 h	Tempscan-2
9	Annealing	300	Bias = –0.1 V, 3 days	\
10	I-V	60	\	IV-3
11	Isothermal DLTS	17.5	\	ITS-2
12	DLTS scan	60 – 550	6 h	Tempscan-3
13	Isothermal DLTS	17.5	\	ITS-3
14	I-V	60	\	IV-4
15	DLTS scan	60 – 550	$U_P = 0.5$ V, 6 h	Tempscan-4
16	Isothermal DLTS	17.5	\	ITS-4
17	I-V	60	\	IV-5

18	DLTS scan	60 – 300	3 h	Tempscan-5
19	Annealing	300	Bias = –0.1 V, 100 h	\
20	Isothermal DLTS	17.5	\	ITS-5
21	I-V	60	\	IV-6
22	DLTS scan	60 – 300	3 h	Tempscan-6

As shown is Figure 4.20(a), the multi-barrier shows up right after annealing at 550 K for 200 minutes with only tiny bias applied (–0.01 V). Moreover, the second barrier that generated from high temperature treatment seems not smooth enough, which indicate the possible existence of additional SBH(s). Meanwhile, annealing at room temperature without bias does not affect the I-V characteristic.

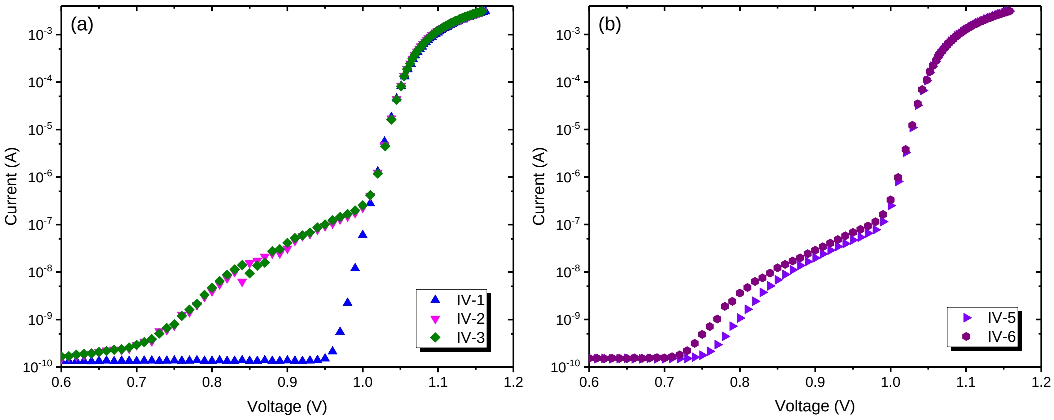


Figure 4.20. Evolution on forward I-V characteristic due to (a):annealing before DLTS scan with high temperature and (b) room temperature annealing after high temperature DLTS scan on diode (B) of Ti/W sputtering 1 min with labels illustrated in Table 4.9.

On the other hand, the DLTS temperature scan with reverse bias –10 V that is normally applied in our case could be regarded as the combination effect of bias stress and high temperature, or in other words the accelerated bias stress under high temperature, especially for long time DLTS test involving high temperature zone. As illustrated in Figure 4.21, even though no obvious influence on I-V curve could be found owing to low temperature DLTS scan, evolution on I-V characteristic can be identified due to high temperature DLTS scan (IV-3 to IV-5). However, thanks to high temperature scan, the form of I-V curve becomes smoother and the additional SBH is reduced, which indicates that bias stress under high temperature possibly takes charge of reform on SBH especially those low SBH regions. (i.e. to flat the surface and ‘pinch-off’ of those region with low SBH.) Meanwhile, the effect on the low SBH regions’ ‘pinch-off’ could be recovered at room temperature to some degree, as can be seen from Figure 4.20(b).

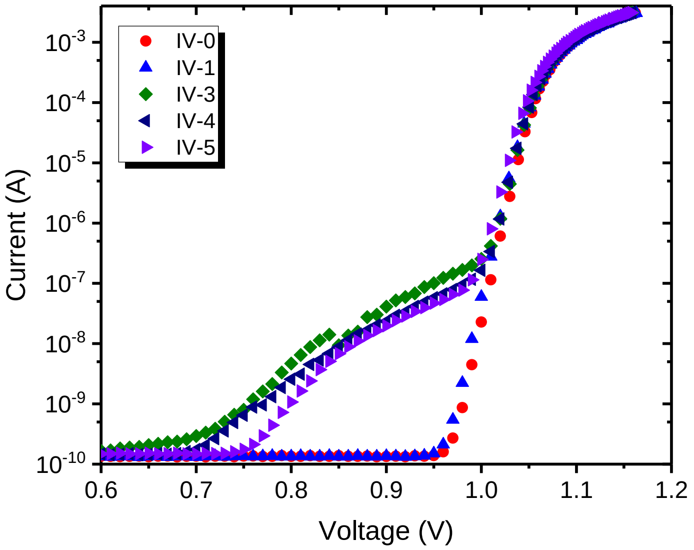


Figure 4.21. Evolution on forward I-V characteristic due to DLTS scan on diode (B) of Ti/W sputtering 1 min with labels illustrated in Table 4.9.

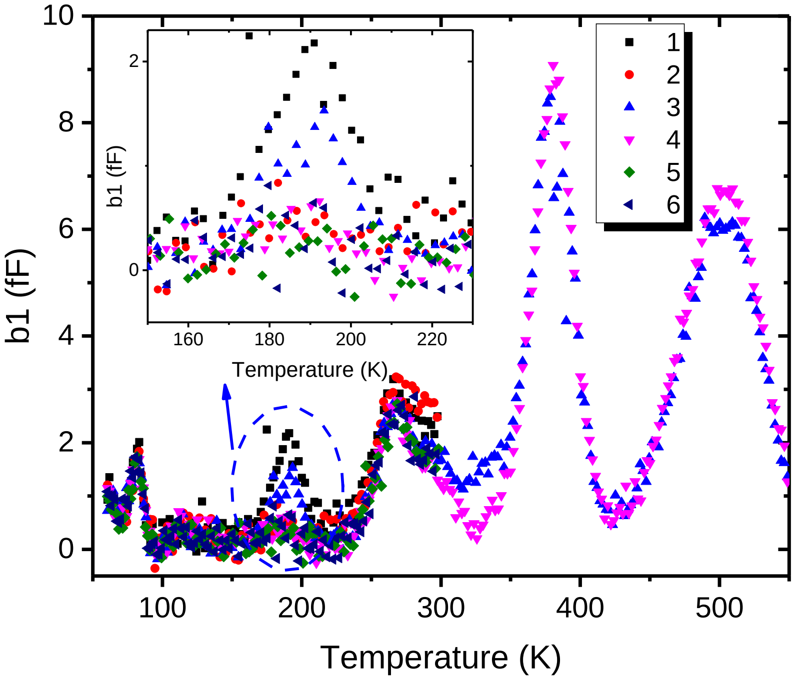


Figure 4.22. DLTS signal (b1) with a period width T_W = 204.8 ms of different scan cycles on Ti/W sputtering 1 min diode (B). The labels indicate the number of DLTS scan cycles (Tempscan) marked in Table 4.9.

Figure 4.22 illustrates the DLTS scan signals on diode (B). The main evolutions of DLTS signal take place at around 190 K. As indicated by the height of DLTS signal, the concentration of defect identified at 190 K is reduced owing to high temperature annealing. However, this reduction recovers after storing at room temperature. On the contrary this reduction in concentration due to high temperature DLTS scan (bias stress at high temperature) could not be recovered even after 100 hours' annealing at room temperature. Another change on DLTS signals is uncovered at around 330 K, which indicates that certain deep level is annealed out during temperature scan. Annealing effect on this defect level will be detailed discussed in section 5.3.2.

Isothermal DLTS tests have also been tracked as a complementary of simple profile on low energy defect levels. Two negative peaks and one positive peak could be identified in Figure 4.23. The concentration of energy level showing up with a period width of 1 ms is always reduced after each experimental step. At present, there is no explanation to this trend of such tiny energy level due to low temperature and small T_W to the best of author's knowledge. Apart from the pure treatment at either high temperature or room temperature where the influence on DLTS signal could be neglect, the effect according to bias stress with high temperature is highlighted. However, the evolution is still odd, especially the sharp increase after the last 100 hours' annealing at ambient temperature (ITS-4 → ITS-5). Even though the manner is strange on these two defect levels, there trend are consistent. (i.e. The peak heights increase/decrease at the same time.) Considering the corresponding I-V characteristics, it is safe to say that no special link exists between double-barrier behavior and those energy levels detected at extremely low temperature, and these levels at extremely low temperature will be discussed in 5.3.5.

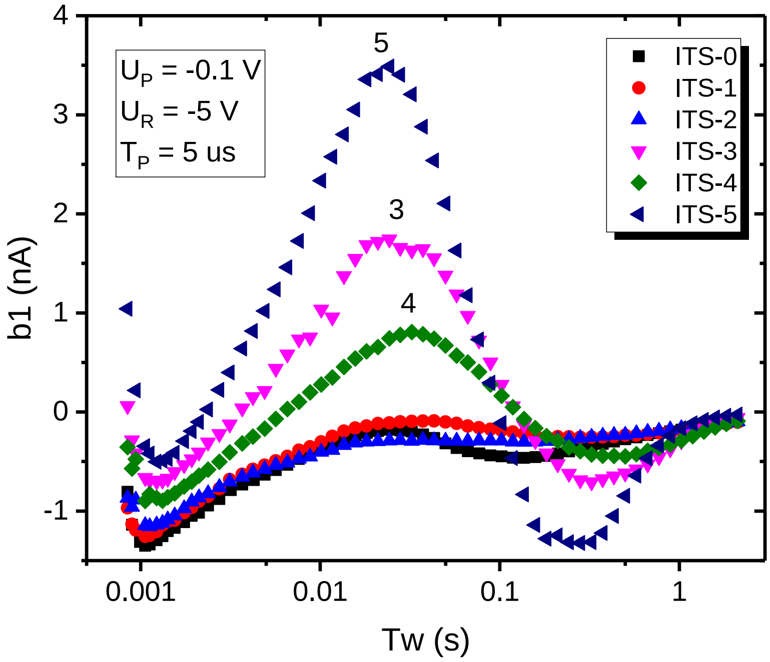


Figure 4.23. Isothermal DLTS scan with variation of period width (T_W) from 0.6 ms to 3 s on diode (B) of Ti/W sputtering 1 min sample. Labels of test number are illustrated in Table 4.9.

In short, the double-barrier on Ti/W sputtering 1 min samples results directly from high temperature treatment, which cannot be annealed out at room temperature. This high temperature annealing could also reduce the concentration of the defect level at round 190 K, which can be recovered to some degree. On the other hand, the DLTS scan namely bias stress under high temperature could reform and smooth the interface, if we think this uneven curve is due to the inhomogeneity of the Schottky contact, which leads to reduction on low SBH region that can be annealed and smooth the interface condition. Furthermore, the reduction on defect level around 190 K due to DLTS scan could not be recovered. Meanwhile, no clear connection between these two treatments (pure high temperature and bias under high temperature) and those defects with tiny activation energy is found, and no influence is uncovered on I-V curves due to these defects.

4.3.3 Comparison on samples with different metal contacts

❖ Static measure

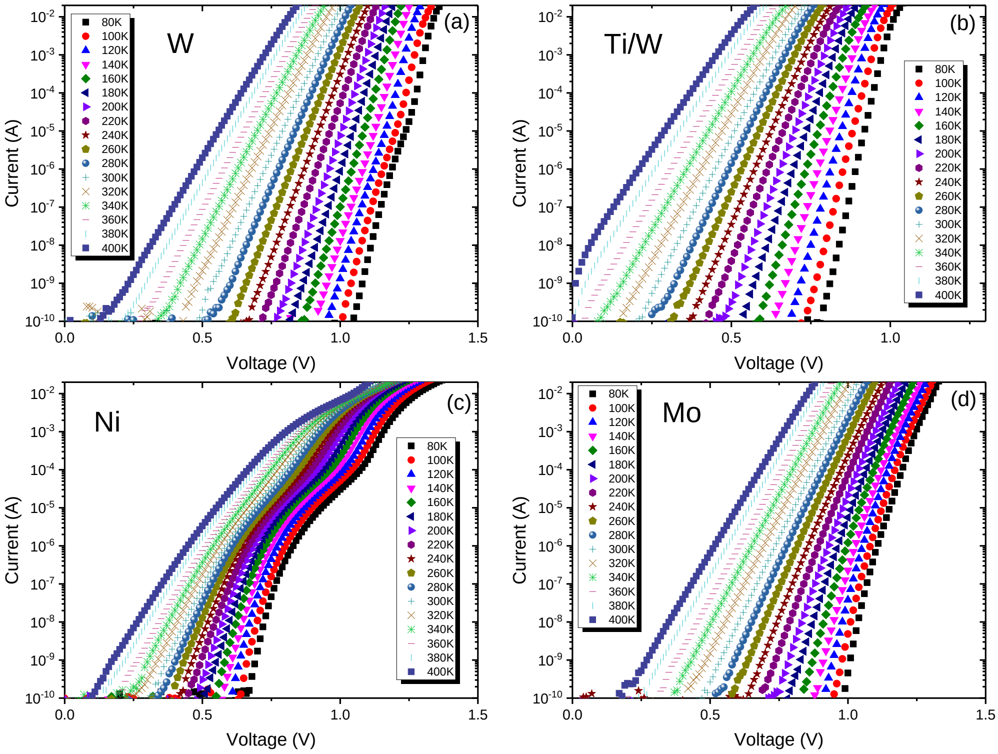


Figure 4.24. Forward I-V characteristics between 80 K and 400 K measured in the cryostat with a step of 20 K on samples of (a): Tungsten (S7); (b): Titanium/Tungsten (S3); (c): Nickel (S2) and (d): Molybdenum (S8). Sample descriptions are illustrated in Table 4.1.

Figure 4.24 shows the forward I-V curves on diodes with 4 different metal contacts (W, Ti/W, Ni and Mo) within a wide temperature range (80 K – 400 K). It is clear that Ti/W and Mo diodes keep linear on log(I)-V curve under whole temperature range studied, while the Ni sample always reveals a multi-barrier phenomenon. Furthermore, barrier inhomogeneity shows up only under temperature below 100 K on W diode. The forward I-V characteristics vary tremendously from one metal contact to another, especially the status of SBH.

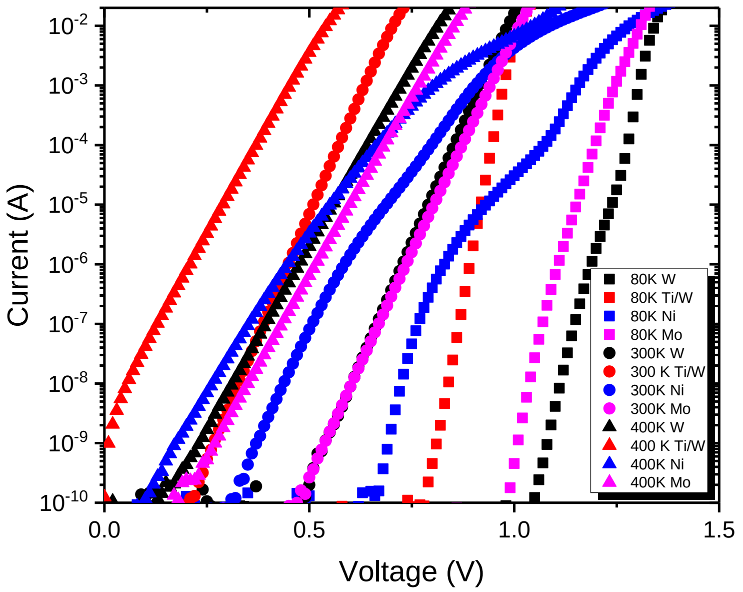


Figure 4.25. Comparison of forward I-V curve at 80 K, 300 K and 400 K on four SBDs with different metal contacts.

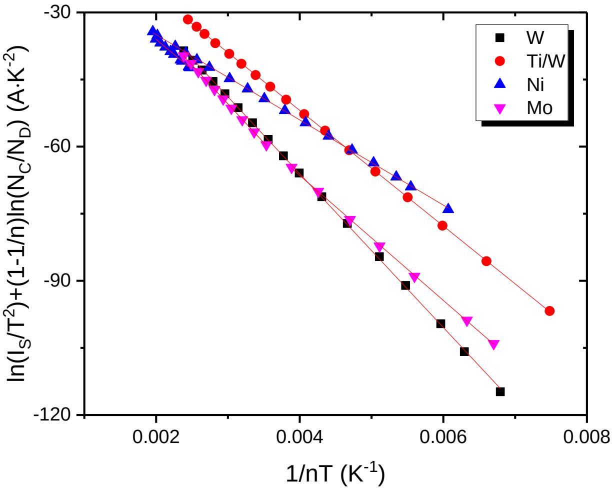


Figure 4.26. Modified Richardson plot according to flat-band SBH of 4 diodes with different metal contacts.

In order to compare the I-V characteristics of samples with 4 metal contacts, their I-V curves at 80 K, 300 K and 400 K are shown in the same plot (Figure 4.25). Apart from the different SBH behaviors (i.e. single barrier or multi-barrier) discussed above, the increments of SBH differs as well. For example, the W diode appears with the highest SBH among four diodes at 80 K, while its SBH value could be lower than that of the Mo sample at high temperature.

Table 4.10. Flat-band SBH and effective Richardson constant of diodes with different metal contacts extracted from MR plot shown in Figure 4.26.

Metal	Φ_{BF} (eV)	A^* ($A\cdot cm^{-2}\cdot K^{-2}$)
W	1.48	585
Ti/W	1.11	32.7
Ni	0.82	4.84×10^{-6}
	1.16	4.60×10^{-3}
Mo	1.20	1.01×10^{-3}
	1.50	208

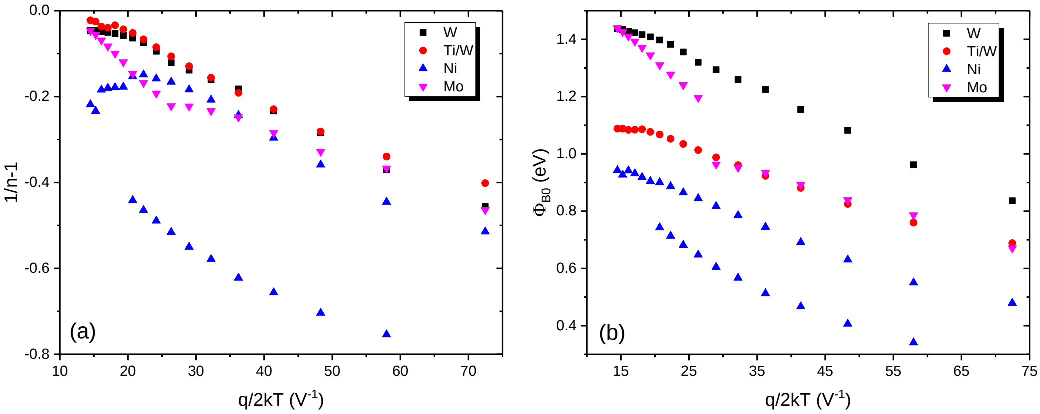


Figure 4.27. (a): $1/n-1$ *as a function of* $q/2kT$ *(potential fluctuation model) and (b) zero-bias barrier height* Φ_{B0} *as a function of* $q/2kT$ *(Gaussian distribution model) on 4 diodes with different metal contacts.*

The modified Richardson plots according to Φ_{BF} on 4 diodes are illustrated in Figure 4.26, with the correspondent Φ_{BF} and A^* extracted listed in Table 4.10. As is discussed in 4.3.21, two SBH regions are identified with MR plot on Mo diode even though its I-V characteristic is always linear enough. Considering that different temperature zones are dominated by different SBH on Mo, it is indicated that these two SBHs have similar I-V performance especially during the transient region, which results in the quasi-linear behavior over the whole temperature range. On the other hand, only one SBH has been marked on W diode since too little data on multi-barrier region (below 100 K) are measured to extract the lower SBH value. On top of that, the Ni diode always presents multi SBHs, which results in two straight lines in the MR plot that cover full temperature range. However, the calculated A^* are rather small even when it comes to the high SBH region compared with other diodes, which indicates the complex SBH status on the Ni sample.

Figure 4.27 shows the comparison of potential fluctuation model and Gaussian distribution model, and those parameters extracted are listed in Table 4.11. It is clear that different SBH regions can also be separated according to the potential fluctuation model, as presented in their MR plots. However, linearity degenerated on potential fluctuation fitting at high temperature among all samples except the Mo one. Especially when it comes to the Ni sample, no specific linear trend shows up at temperature higher than 300 K. Considering the excellent linearity on MR plot shown in Figure 4.26, the experiment error on temperature and the calculation of ideality factor should be well controlled. On the other hand, even though linear fitting works better on Gaussian distribution model at high temperature (Figure 4.27b), same problem still exists, which indicates that other effect may take charge when the temperature is high enough.

Furthermore, since σ_{S0}^2 reflects the speed that the measured Φ_{B0} increases when the temperature rises up (Eq. (2.32)), large σ_{S0}^2 on Mo sample of high SBH part compared to that of W sample indicates the differences between measured Φ_{B0} (W) and Φ_{B0} (Mo) should be reduced at higher temperature, which corresponds well with the I-V curves as discussed above.

Table 4.11.Parameters in potential fluctuation and Gaussian distribution model of diodes with different metal contacts extracted from plots shown in Figure 4.27 between 80 K and 400 K.

Metal	ρ_2	ρ_3 (mV)	$\bar{\Phi}_{B0}$ (eV)	σ_{S0}^2 (V^2)
W	0.079	–7.48	1.61	0.01
Ti/W	–0.117	–8.37	1.25	0.01
Ni	–0.078	–9	1.10	0.01
	0.208	–11.55	1.05	0.02
Mo	–0.175	–15.23	1.75	0.02
	0.054	–5.58	1.17	0.01

In addition, this trend of growth could be much easily identified in Figure 4.28(a). Apart from the irregular Ni diode, the SBH determined by C-V is closed to the highest SBH (if multi-barrier exists) obtained from MR plot (Table 4.10).

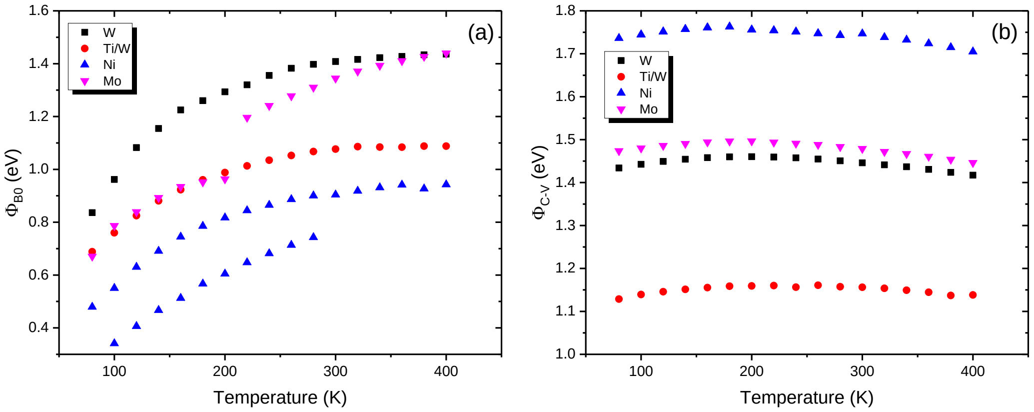


Figure 4.28. Temperature dependence on (a): zero-bias barrier height Φ_{B0} and (b): the SBH extracted from C-V Φ_{C-V} of diodes with 4 different metal contacts.

❖ DLTS results

DLTS tests have taken place on these 4 samples within the temperature range of 60 K – 550 K, while I-DLTS was adopted for the temperature below 200 K, as shown in Figure 4.29 and Figure 4.30. The formats of DLTS signals above 200 K are similar: a double peak below 300K; a sharp high one near 380 K and another overlapped peak around 550 K.

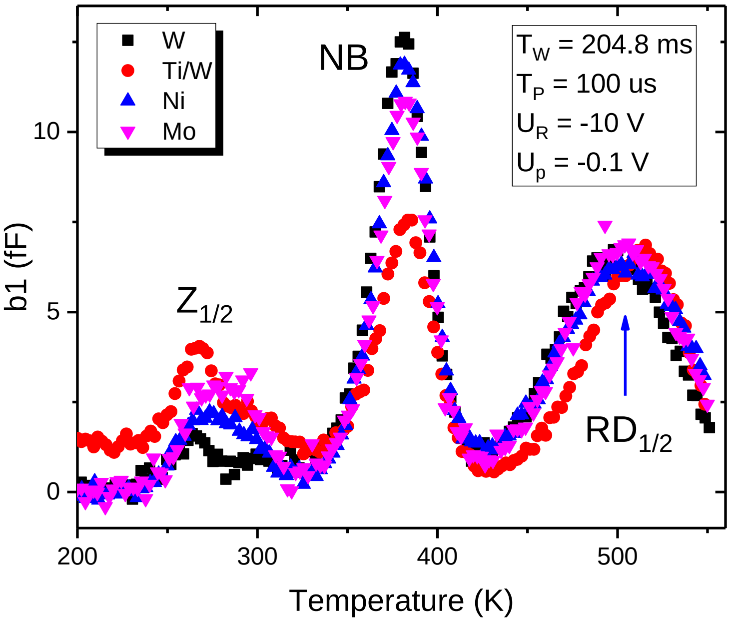


Figure 4.29. Comparison of DLTS signal (correlation b1) between 200 K and 550 K on 4 diodes with different metal contacts.

Regarding the overlapped peak at high temperature (550 K), signals almost completely coincides except the Ti/W one, which indicates this overlapped peaks namely RD$_{1/2}$ could be intrinsic defect levels on SiC regardless of metal contact or fabrication process.

Meanwhile, it could be found on Ti/W sample that the right side of the overlapped peak corresponds well with other signals, which means the error from temperature record could be ruled out. However, the left side of this peak on Ti/W diode is lower compared to others, which indicates the defect levels with lower activation energy do differ from diodes with other contacts.

When it comes to the highest peak around 380 K, the difference only lies in the signal magnitude. In other words, this defect level (NB center) should also be a common one but could be influenced by the surface contact or treatment process.

In addition, the defects below 300 K which have been marked as $Z_{1/2}$ (or Z_1/Z_2) are more complex among samples studied. This should mainly be due to the variation of defect concentrations and their proportions, which result from different manufacturing processes.

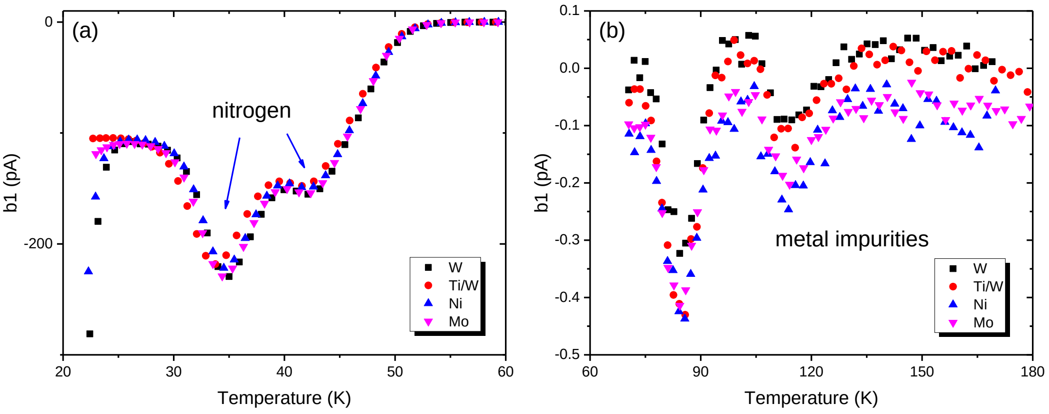


Figure 4.30. Comparison of I-DLTS signal (b1) with a period width of 204.8 ms and temperature range (a): 20 K to 60 K and (b): 70 K to 170 K.

However, on the other hand no obvious difference can be distinguished on lower temperature part (60 K – 200 K). Considering the shallow doping controlled during process are similar among all samples according to the C-V measurements, these defects discovered with low activation energy should be intrinsic common defects (e.g. shallow levels of nitrogen doping).

Furthermore, more negative signal appears at 20 K especially on W and Ni samples, that suggests the existence of levels with tiny energy. These energy levels that show up at extremely low temperature will be discussed in 5.3.5.

Figure 4.31 shows the activation energies and their capture cross sections of defect levels from Arrhenius analysis according to the DLTS spectra in Figure 4.29 and Figure 4.30. Defect concentrations are not presented here as they directly relate to the heights of DLTS signals. No specific defect level owing to different metal contacts is recognized among these diodes. Most defects could be separated with no doubt since there activation energies are closed to each other and near the defects that have been identified, except the double level $Z_{1/2}$ and $RD_{1/2}$ where larger error may exist during the analysis.

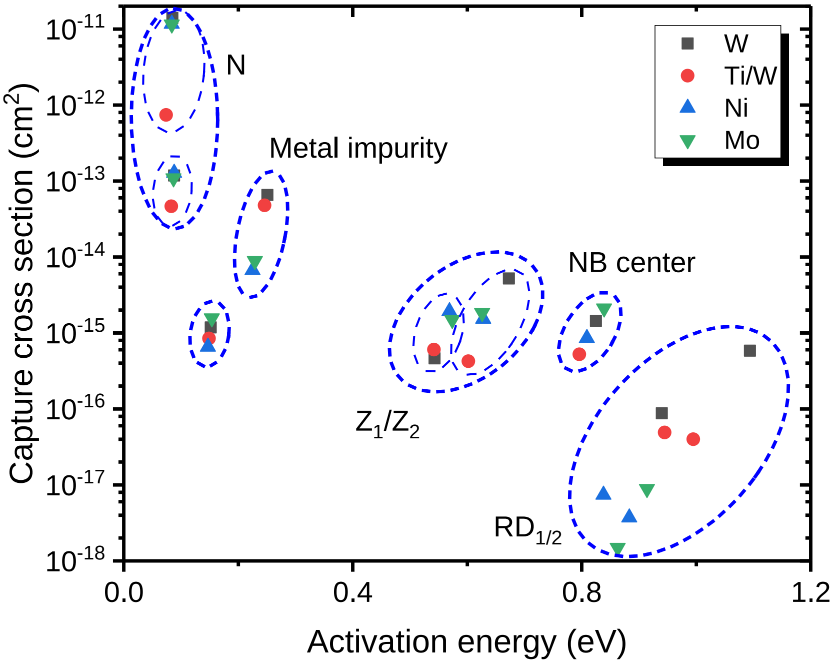


Figure 4.31. Mapping of defect activation energy compared to the conduction band and its capture cross section with the help of Arrhenius analysis based on DLTS results on 4 diodes with different metal contacts. Those points circled with dash lines are suggested to originate from the same defect labeled beside.

An interesting phenomenon is that a linear relation could be identified from the extracted activation energies and capture cross sections, especially on NB center and the energy level around 0.15 eV where the defect level is easy to analyze thanks to the sharp peak of DLTS signal. This will be detailed studied in section 5.3.2.

Chapter 5
Characterization on other samples and discussion

5.1 PiN diode

5.1.1 Sample overview

The 10 kV 8 A 4H-SiC PiN diodes fabricated by Supergrid have been characterized with static measurements and DLTS. The diodes with a square size of 3 µm×3 µm have been realized by Junction Termination Extension (JTE) technique. On top of that, in addition to a short annealing of 2 minutes at 950 ℃ following the deposition and etching of Ti/Al/Ni, a 2 hours′ annealing at 300 ℃ has been performed after the final passivation.

5.1.2 Experiment setup

Two PiN diodes on the same wafer labeled (L) and (R) have been investigated, while the second diode (R) was only involved in the annealing test that will be discussed later. All measurements here have been taken out with the help of DLTS system described in the former chapters. I-V characteristics were normally measured during the DLTS Tempscan with a range of forward bias from 0 V to 4 V at every 0.01 V, while current limit (0.01 A) has never been reached due to the relatively high series resistance of DLTS system. The temperature interval for I-V was 20 K if above 150 K, while that became smaller when cooling down. Capacitances at either reverse bias or pulse condition have also been marked during DLTS.

In order to rule out the effect on high temperature annealing during DLTS, two quick tempscan were adopted from 300 K to 550 K and back to 300 K with almost 2 hours on each direction. An additional 30 min annealing at 550 K has been added with tiny bias (–0.01 V) between these two tempscans.

After a first DLTS tempscan from 20 K to 550 K along with the I-V characterization explained above, other DLTS with variation of either U_P or T_P have been used to investigate the characteristics of defect levels. I-DLTS mainly took charge of extracting the defect levels at low temperature, where two temperature ranges (20 K – 60 K) and (60 K – 280 K) were separated to avoid losing accuracy. On top of that, those energy levels closed to conduction band have also been discovered thanks to the isothermal DLTS at 17.4 K. Specific conditions on DLTS measurements will be explained at each part.

5.1.3 Static Characterization

Figure 5.1 shows the forward I-V curves measured during the DLTS tempscan. It is clear that those curves on log(I)-V plot show traditional characteristics of PiN diode except those three below 40 K, where the free-out effect of shallow levels cannot be ignored. Measured current deviate linear under small bias with smaller slope, which is mainly due to the recombination current similar to that discussed in Schottky diode, while the characteristics with higher bias seem more 'ideal' and will be the main region for extracting electric parameters. Considering the series resistance as cited, even those maximum voltage applied should always be 4 V for each measure, the sample bias after normalization could seldom reach that and results in the bending of log(I)-V curve at high current levels.

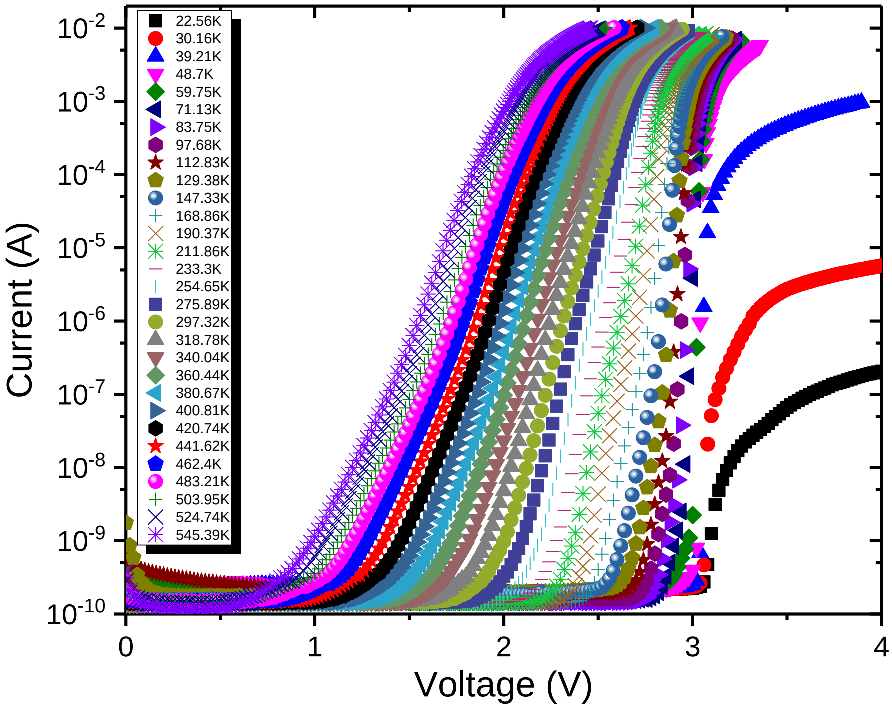


Figure 5.1. Forward I-V characteristics on diode (L) from 20 K to 550 K.

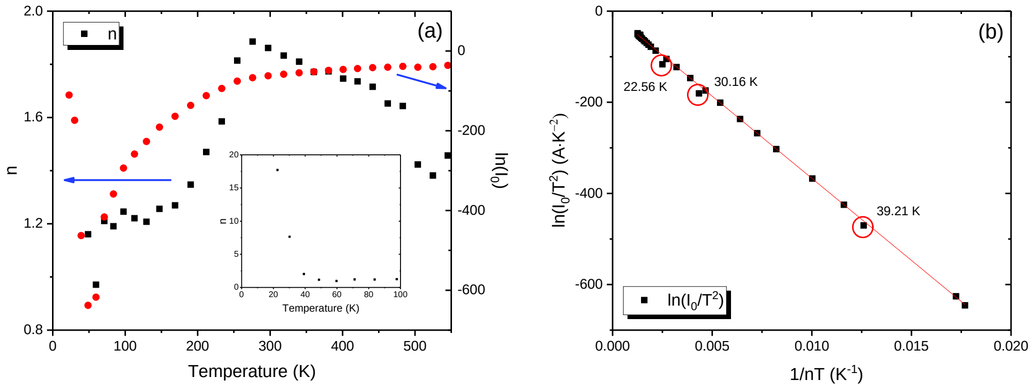


Figure 5.2. (a): Extracted ideal factor n and saturation current I_0 at different temperatures according to linear regions with relatively high current illustrated in Figure 5.1. and (b): plot of $\ln\left(I_0/T^2\right)$ as a function of $1/nT$. Three points marked with red circles were those measured at lowest temperatures (labeled beside the circles) and are not involved in the linear fitting.

As shown in Figure 5.2(a), if we ignore those values measured below 80 K where freeze-out takes charge, the ideality factor first rises up with increase of temperature, and then drops almost linearly after reaching its maximum at 275 K. Since n represents the component of current, or in other words, whether diffusion current ($n=1$) or recombination current becomes the main issue, the recombination current plays an important role under the middle temperature (250 K – 450 K). On the other hand, I_0 increases rapidly at low temperature, and becomes almost saturate after 300 K.

More interesting result could be seen in Figure 5.2(b), where a relationship similar as the so called Modified Richardson plot discussed in 2.4.6 is perfect represented if those three points with carrier freeze-out are ruled out. Consider the ideal equation that describes the general I-V characteristics of the PiN diode:

$$I = I_0\left(e^{\frac{qV}{nkT}} - 1\right) \tag{5.1}$$

The linear relationship shown in Figure 5.2(b) indicates that the saturation current I_0 obey certain temperature relation:

$$I_0 = ST^2 e^{\frac{\psi}{nT}} \tag{5.2}$$

where S is the effective surface of the diode, ψ is the constant parameter determined by the plot. By reminding the temperature relationship given by diffusion theory that

$$I_0 = T^{\gamma} e^{-\frac{E_g}{kT}} \tag{5.3}$$

where the forbidden band gap $E_g = E_g(0) + \beta T$ if we assume it changes linearly with temperature. By comparing Eq. (5.3) with (5.2), it could be found that $\gamma = 2$ in this case. Moreover, instead of linear increase on E_g with temperature, the measured effective forbidden band gap E_g^{eff} that given by $E_g^{eff} = E_g(0)/n$ should be more suitable for characteristic analysis. By introducing E_g^{eff}, the band gap calculated according to the slope in Figure 5.2(b) is 3.11 eV, which matches well with the theoretical value listed in Table 1.1.

5.1.4 DLTS characterization

❖ Tempscan: variation of U_P

Figure 5.3 shows DLTS spectra under various U_P. Generally speaking, the absolute height of both positive peak and negative peak rise up with increase of the pulse voltage. This could be simply explained by enlarged depletion region under bias approach to zero, which results in more active volume on defect detection. However, 3 different types of negative peaks show up in this case: (a) The height of the signal peak increases gradually for the negative peaks around 75 K [Figure 5.3(b)]; (b) The peak could only be identified with a minimum pulse voltage (–1 V) and increase obviously with variation of U_P (the peak near 130 K); (c) with the same threshold as (b), but is almost independent on U_P (the peaks around 270 K and 500 K). This indicates the existence of three different hole traps.

For the first one (75 K), they should be the common defect levels all over the diode, and the freeze-out effect could also contribute to this phenomenon as the freeze-out can be affected by the bias voltage.

It can be easily come up with that the second one (130 K) owing to the hole trap that lies close to the interface with large concentration, which may originate from the interface states. As a result, the detected defects depend not only on the trap concentration, but also on the concentration of hole injected in the zone of investigation. Therefore if the pulse is too small, the effective detection zone could not be reached where enough holes exist, and leads to no peak shown up at small reverse bias. Meanwhile, even when the U_P is large enough to show the peak in the DLTS signal, the concentration of hole injected is still not able to fill all the traps under relatively small U_P, and this could be released by increasing the bias, which leads to the obvious increase on DLTS results with large U_P.

The threshold for the 3rd type of defect levels should be the same as the second one, while the difference should lie in the defect type. Unlike the 2nd type that is possibly due to the interface traps, this trap level may be due to intrinsic hole defects, which exists among the material except the region near interface. In that case, the peak height of DLTS signal trends to saturate even under high pulse bias because of the boundary of the defect. Meanwhile, the effect of increasing on injected hole concentration in the detective zone should also be neglected since the defect concentration is small and easy to be fulfilled.

On top of that, the positive peak at around 300 K performs commonly except under large pulse voltage, where the height of peak should be influenced by the appearance of the negative one.

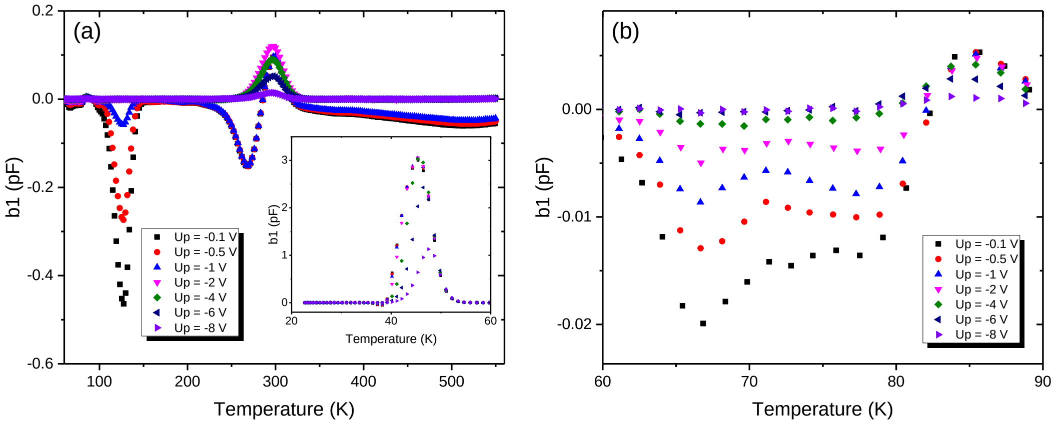


Figure 5.3. (a): DLTS spectra under different pulse voltages U_P between 20 K and 550 K with $Tw = 204.8$ ms, $U_R = -10$ V, $T_P = 100$ µs. (b) shows the same signals with a temperature range from 60 K to 90 K.

❖ Tempscan: variation of T_P

Figure 5.4 shows the DLTS spectra with various of T_P from 1 μs to 100 μs. It can be seen that all negative peaks only appear with pulse width no smaller than 20 μs, which should be the minimum time for hole injection. Most of the negative peaks tend to saturate even with larger T_P as is the feature of the point defect, except those around 70 K. This indicate that the hole defects detected at low temperature are complex defects such as line defects or dislocations.

On the other hand, the defect of electrons according to the positive peak at 300 K shows up with small T_P (1 μs). Meanwhile, this electron level should also be due to the point defect since the signal no more changes under large pulse width.

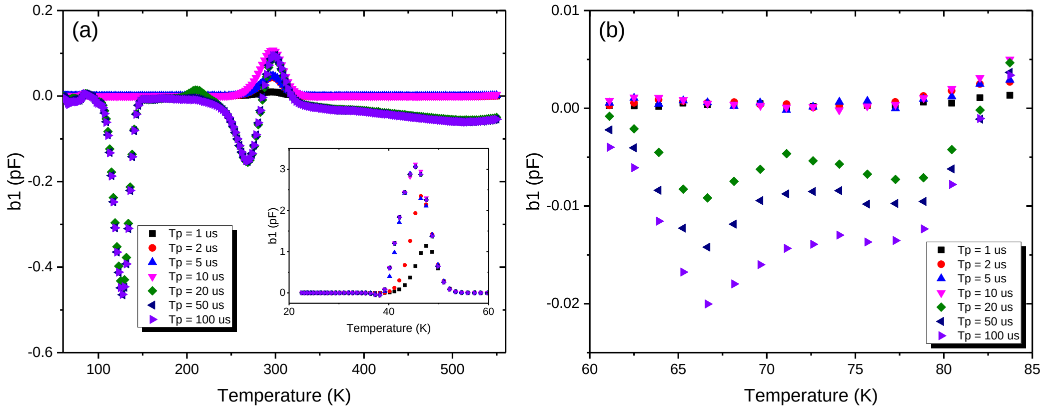


Figure 5.4. (a) DLTS spectra under different pulse width from 20 K to 550 K with Tw = 204.8 ms, $U_R = -10$ V, $U_P = -0.1$ V. (b) is the same signals with a temperature range from 60 K to 85 K.

❖ DLTS spectra with different T_W : strong and weak hole injection

As discussed before, the threshold voltage for the hole defect detection lies around $U_P = -1$ V. Therefore, we define here the conditions of strong hole injection with $U_P = -0.1$ V and weak hole injection with $U_P = -2$ V, as shown in Figure 5.5(a) and (b). A negative peak around 80 K shows up under bother strong and weak hole injection conditions. This abnormal phenomenon may be linked to the negative-U center discussed in 5.3.4. In addition, unlike other peaks that do not change their heights with different period widths, the height of the negative peak around 130 K increases with decrease of the period width. This may due to the freeze-out effect that will be discussed later. Generally speaking, under the temperature region where freeze-out takes place, the smaller T_W we use, the higher temperature the peak will appear on the DLTS spectra, the less freeze-out will influence and as a result, the higher the signal peak will be obtained due to larger reverse capacitance. However, this negative peak still exist at weak hole injection condition with a period width of 2.048 s, which could hardly be explained as the height of the signal peak should be the smallest compared to those short T_W , except it performs as negative-U centers discussed later.

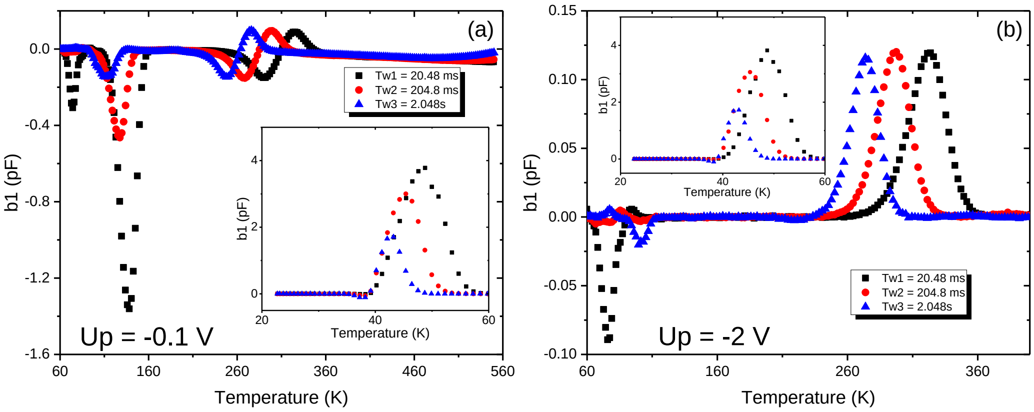


Figure 5.5. DLTS spectra (20 K – 550 K) with three different period widths for (a): strong hole injection with $U_P = -0.1$ V and (b) weak hole injection with $U_P = -2$ V. Other parameters are as follows: $U_R = -10$ V, $T_P = 100$ µs. The flat area with no peak identified above 400 K in (b) are hided for better illustration.

On top of that, attention should be paid on the positive peak around 90 K as shown in Figure 5.5(b), which reveals the existence of an electron trap. Even though it could be clearly identified under weak hole injection, it is easy to be ignored under strong hole injection, due to either signal compensation or scale effects due to the large negative signal.

❖ Current DLTS spectra at low temperature region

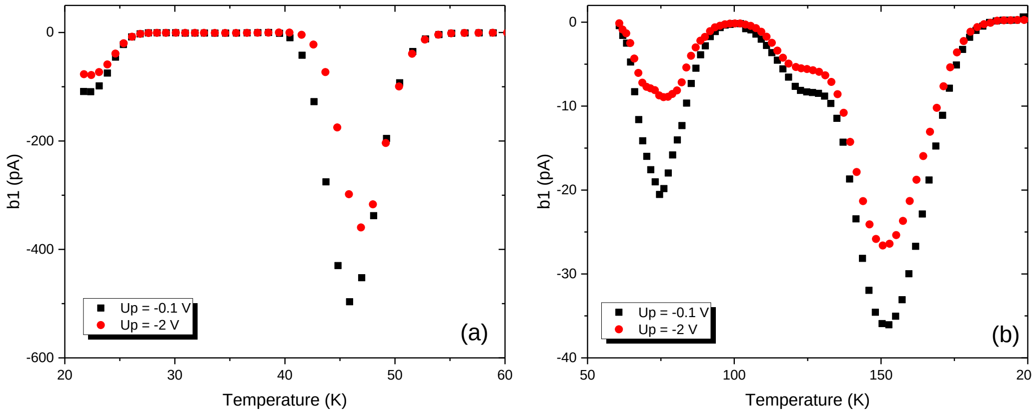


Figure 5.6. I-DLTS signal with a period width of 204.8 ms of both weak and strong injection condition for the PiN diode within the temperature range of (a): 20 K – 60 K and (b): 60 K – 200 K.

As explained, I-DLTS were adopted in order to extract the defect levels accurately with Arrhenius analysis. The I-DLTS spectra for conditions of both strong and weak hole injection between 20 K and 200 K are illustrated in Figure 5.6. Those results of I-DLTS over 200 K are not shown here because no further peak could be recognized till 280 K. Same settings for I-DLTS were adopted as explained in 4.2.4 except the pulse voltage. 5 peaks can be recognized including the one at ~ 20 K which is not fully displayed. However, only negative peaks are obtained from I-DLTS, which is quite different from the capacitance DLTS spectra where the defect levels according to either electrons or holes are indicated by the sign of the peak among DLTS signal. Therefore to characterize the defect levels, C-DLTS are also taken into consideration in the Arrhenius analysis.

- **Arrhenius analysis: I-DLTS**

Table 5.1. Calculated deep level parameters based on Arrhenius plot by I-DLTS measurement between 20 K and 280 K for both strong and week hole injection. The defects are indicated by the position of the negative peak shown in Figure 5.6.

T (K)	E_a (eV)	σ (cm^2)	N_T (cm^{-3})	E_a (eV)	σ (cm^2)	N_T (cm^{-3})
	Strong hole injection			Weak hole injection		
22	0.032	3.04×10^{-16}	2.32×10^{13}	0.033	6.87×10^{-16}	1.81×10^{13}
46	0.098	1.62×10^{-13}	2.36×10^{13}	0.097	7.32×10^{-14}	1.74×10^{13}
75	0.117	2.22×10^{-15}	1.19×10^{14}	0.099	1.91×10^{-16}	8.73×10^{13}
127	0.167	2.51×10^{-18}	1.00×10^{13}	0.163	1.92×10^{-18}	8.67×10^{12}
152	0.178	5.25×10^{-19}	1.11×10^{14}	0.194	1.81×10^{-18}	1.94×10^{13}

As listed in Table 5.1, those extracted trap levels are quite similar for both strong hole injection and weak hole injection. Therefore the extracted defect levels are due to electron levels only. Compared with that form the SiC SBD as listed in Table 4.7, some common defects can be identified (e.g. the level of shallow doping).

- **Arrhenius analysis: C-DLTS**

Those calculated trap parameters according to the convention DLTS as shown in Figure 5.4 and Figure 5.5 are listed in Table 5.2 by means of condition on both strong and weak hole injection. Owing to the influence of the hole trap under strong hole injection where a compensation of signal could take place, most of the electron traps could not be well recognized under strong hole injection except the one near 300 K. As will be discussed in detail later, this electron trap should be identified as $Z_{1/2}$ even though it could not be accurately separated at present. No direct link can be found between the extracted hole traps and that list in Table 5.1, which suggests that hole traps could not be well recognized with I-DLTS.

Table 5.2. Calculated deep level parameters based on Arrhenius plot by C-DLTS measurement for both strong and weak hole injection. The defects are indicated by the position of the peak shown in Figure 5.4 and Figure 5.5 with the period width of 204.8 ms, while the activation energy is related to either conduction band (electron traps) or valence band (hole traps).

T (K)	E_a (eV)	σ (cm^2)	N_T (cm^{-3})	Type
Strong hole injection				
66	0.160	5.71×10^{-13}	2.68×10^{13}	hole
125	0.296	9.97×10^{-14}	4.15×10^{13}	hole
270	0.625	2.16×10^{-14}	6.58×10^{12}	hole
300	0.667	6.19×10^{-15}	4.47×10^{12}	electron
515	1.431	7.02×10^{-13}	1.86×10^{12}	hole
Weak hole injection				
85	0.166	2.80×10^{-15}	4.00×10^{11}	electron
296	0.656	4.45×10^{-15}	4.89×10^{12}	electron
382	0.806	9.13×10^{-16}	8.19×10^{10}	electron

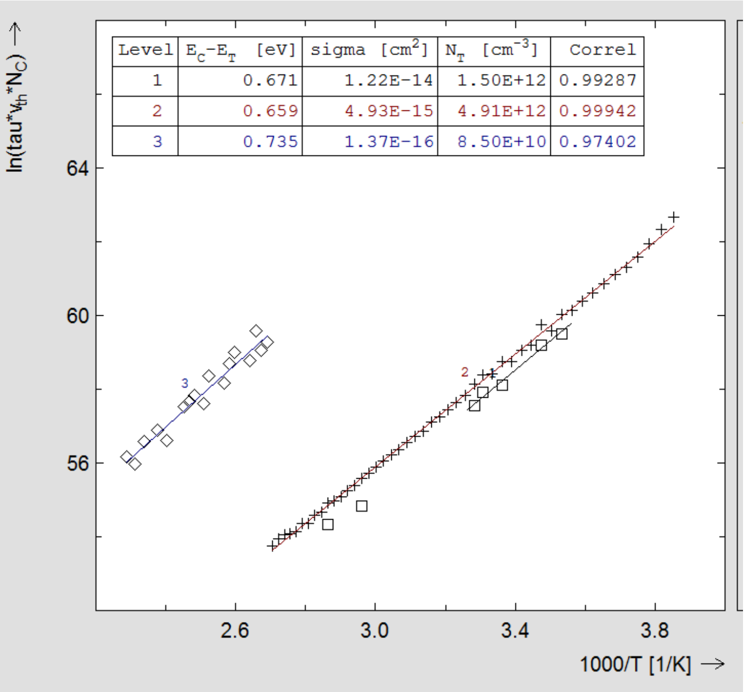
❖ **Trap levels identification**

Taking into consideration of the results from both C-DLTS and I-DLTS, the extracted trap levels in the investigated PiN diode are listed in Table 5.2. Those calculated based on C-DLTS under low temperature are ruled out and are only used for reference owing to the freeze-out effect. Apart from those electron levels discovered in SiC SBDs, two hole traps are reported here. The electron traps around 76 K and 382 K are extracted with weak hole injection condition, while they tend to disappear under strong hole injection due to the influence of the hole trap at 66 K and 515 K.

In addition, when it comes to the $Z_{1/2}$ that usually reported as the overlapped energy levels, we fail to separate that with accurate analysis. However, the existence of the second energy level around 300 K could be suggested from the HERA analysis as shown in Figure 5.7, even only few points are involved in the trap determination on the first level. And considering the peak position in the spectra and its activation energy compared to that of the SBD discussed, it is safe to classify it as the intrinsic defect $Z_{1/2}$.

Table 5.3. Trap levels identification. The type C or I indicates the measure used (C-DLTS or I-DLTS), while the (e) or (h) in identification points out the defect type (electron trap of hole trap).

Type	T (K)	E_a (eV)	σ (cm^2)	N_T (cm^{-3})	Identification	Reference
I	22	0.032	3.04×10^{-16}	2.32×10^{13}	(e) Nitrogen	[24, 70, 136]
	46	0.098	1.62×10^{-13}	2.36×10^{13}		
	75	0.099	1.91×10^{-16}	8.73×10^{13}	(e)	\
	127	0.167	2.51×10^{-18}	1.00×10^{13}	(e) Cr/Ti	[45, 58, 136]
	152	0.178	5.25×10^{-19}	1.11×10^{14}		
C	270	0.625	2.16×10^{-14}	6.58×10^{12}	(h) V/p	[137, 138]
	300	0.667	6.19×10^{-15}	4.47×10^{12}	(e) $Z_{1/2}$	[62, 133, 134]
	382	0.806	9.13×10^{-16}	8.19×10^{10}	(e) NB center	[135]
	515	1.431	7.02×10^{-13}	1.86×10^{12}	(h) V_C	[139]



Level	E_C-E_T [eV]	sigma [cm^2]	N_T [cm^{-3}]	Correl
1	0.671	1.22E-14	1.50E+12	0.99287
2	0.659	4.93E-15	4.91E+12	0.99942
3	0.735	1.37E-16	8.50E+10	0.97402

Figure 5.7. HERA analysis results for the defect between 250 K and 450 K, the extracted level 1 and 2 indicate the possible overlap of the trap levels.

5.2 MOSFET

5.2.1 Introduction

As another important structure, Metal Oxide Semiconductor Field Effect Transistor (MOSFET) based on SiC is commercially available for thousand voltage class, and is quite active in especially the space applications. However, the reliability of the gate oxide is always a key focus that could greatly influence the device performances. In major position in the risk sheet will appear the failure modes related to the SiC MOSFET and failure mechanisms related to the gate oxide.

High Temperature Gate Bias (HTGB) test, as part of the existing standard tests, is widely adopted for power MOSFETs' reliability qualification, especially the gate oxide robustness [140-142]. Based on test conditions, Threshold Voltage (V_{th}) could be either improved or degraded after HTGB [143].

SiC devices in satellites face harsh radiation environment with high energy charged particles, where Total Ionizing Dose (TID) effect becomes a significant issue by reducing channel mobility and generating electron-hole pairs which could be trapped by increased oxide/interface trap concentration, and the electronic characteristic may be strongly affected [144, 145]. The annealing effect under high temperature has also been proved for device recovery, especially when proper electric field is applied during annealing process [146, 147]. Furthermore, for long lifespan exploration mission, SiC devices will encounter electro-thermal aging and TID issues at the same time. There is a large literature on TID effects on SiC diodes, MOS capacitors and transistors [147, 148]. But to our best knowledge, there are few reports on the synergetic effects of HTGB and TID on SiC MOSFETs. Therefore it is necessary to investigate the synergetic combination of HTGB and TID, which should be considered as an candidate to evaluate SiC MOSFETs.

5.2.2 Experiments setup

30 n-type 1200 V, 22 A commercial SiC power MOSFETs (Rohm SCT2160KE) were characterized. HTGB test has been performed under 200 ℃ and gate bias of 22 V (other terminals grounded) for 0 hour (reference), 162 hours and 332 hours respectively. Samples after HTGB were sorted out in two groups (10 for each) before radiation, while the rest 10 were stored at room temperature for control purpose. Co60 γ -ray TID radiation was carried out in IONISOS Company (Lyon, France) with a Gamma reactor and total dose of 1 kGy, 3 kGy, 5 kGy and 10 kGy respectively. Devices were kept in small cardboard boxes and pins were all grounded during the dynamic TID radiation at room temperature and in air, in order to ensure no additional stress was applied. Even though the dose rate was not constant, which varied in the range 0.5 to 1 kGy/h, total dose was closely controlled by dosimeters on 2 opposite sides of the cardboard boxes. The average doses

measured were 1.1 kGy, 3.3 kGy, 5.1 kGy and 10.7 kGy. However no separation will be drawn between target dose and real dose below as their deviation is negligible.

I_{dss} V_{th} and output characteristic of MOSFETs were measured using B1505A Power Device Analyzer / Curve Tracer (Keysight), while I_{gss} and C_{iss} were characterized using B1506A Analyzer (Keysight) before and after each experiment (HTGB and/or radiation). Detailed characterization conditions are listed in Table 5.4.

Table 5.4. Main electric parameters tested and test condition.

Symbol	**Name**	**Measure Condition**
V_{th}	gate threshold voltage	V_{gs} @ I_{ds} = 2.5 mA, V_{ds} =2.8 V
I_{dss}	drain-source leakage current	V_{gs} = 0 V, V_{ds} from 0 V to –1200 V
C_{iss}	input capacitance	V_{ds} from 100 mV to 100 V, AC = 0.03 V
I_{gss}	gate leakage current	V_{ds} = 0 V, V_{gs} from –6 V to 22 V

A time delay was unfortunately introduced between HTGB and/or radiation and characterization: i.e. about 30 minutes to one hour of natural cooling down to room temperature for HTGB and several hours for collecting back samples after TID from the remote facility. The time delay on part of TID is listed in Table 5.5.

Table 5.5. Maximum time delay between the end of radiation and first characterization following TID test.

Target dose (kGy)	**Real dose (kGy)**	**Time delay (h)**
1	1.1	42
3	3.3	16
5	5.1	6
10	10.7	76

5.2.3 Experimental results

5.2.31 HTGB

As shown in Figure 5.8, V_{th} shifts by 14.1% and 16.4% after 162 and 332 hours of HTGB. However, the changes in I_{gss} are negligible. As the Bias Temperature Instability (BTI) has been well explained by electrons directly electric-bias depending tunneling to and from near-interfacial oxide traps namely E′-type oxide defect associated with an oxygen vacancy, this observed V_{th} increase is due to accumulation of trapped electrons [143, 149, 150]. Unlike High Temperature Reverse Bias (HTRB) which commonly leads to leakage current increase [141, 143, 149], no obvious high drain-source leakage current was observed. Meanwhile, shift of C_{iss} curve could also reflects the enhancement of V_{th}, as shown in Figure 5.9, because C_{iss} evolution mainly originates changes in gate-to-drain capacitance (C_{gd}) when it comes to commercial power MOSFETs, which is directly related to threshold voltage [151]. After HTGB stress, the DUTs not involved in TID test remained at room temperature for a week without electrical bias, as shown in Figure 5.10. The variation of V_{th} is rather limited over time so it is considered as negligible. The variation of C_{iss} is also considered as non-significant over time but not with V_{ds} (Figure 5.9).

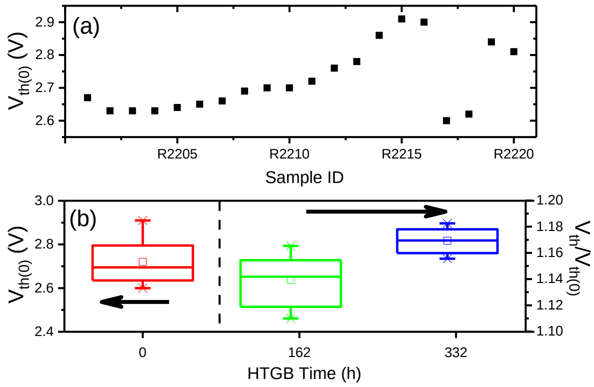


Figure 5.8. (a): Original threshold voltage for all 20 samples involved in HTGB test and (b): Dispersion of normalized Vth before (left part) and after HTGB (right part), with 10 MOSFETs for each group (162 h or 332 h). The first 10 samples (ID R2201 to R2210) belong to 332 h HTGB test and the rest 10 are in the 162 h group. Normalized V_{th} *was separately calculated.*

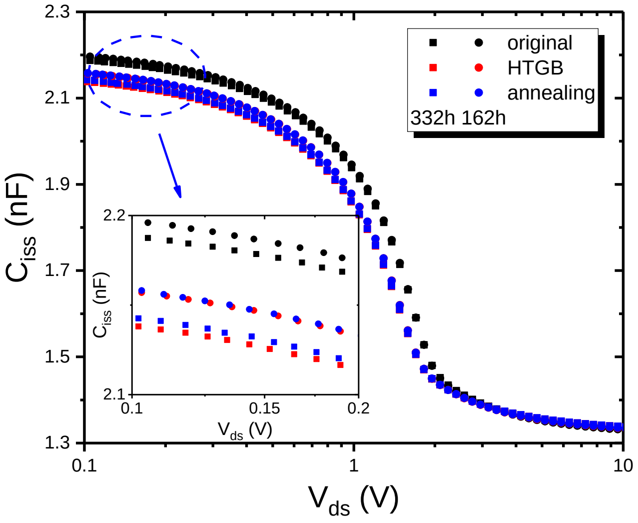


Figure 5.9. Input capacitance C_{iss} *as a function of applied drain-source voltage* V_{ds} *on 162h-HTGB device (R2217) and 332h-HTGB device (R2207) before and after HTGB along with data measured after room temperature annealing for a week.*

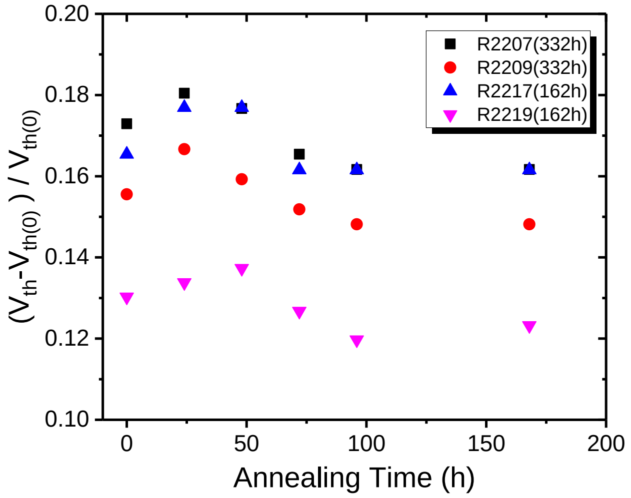


Figure 5.10. Time dependence of normalized threshold voltage during one week after HTGB. No bias was added during this annealing at room temperature.

5.2.32 TID radiation effect

- **Threshold voltage** V_{th}

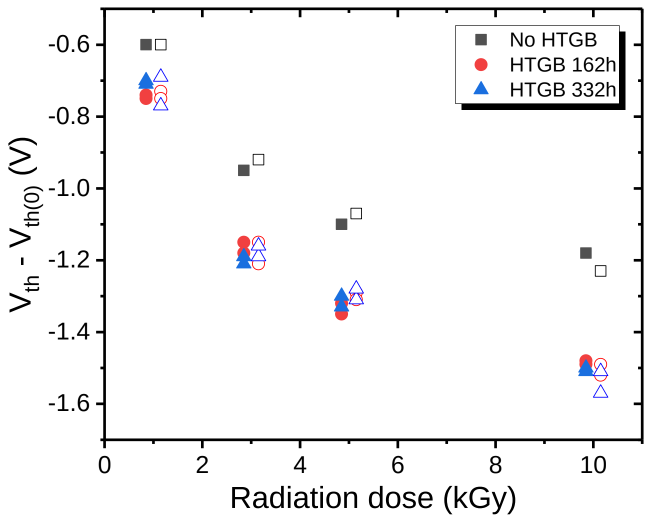


Figure 5.11. Threshold voltage shift as a function of radiation dose with different HTGB time, compared to the value right before the radiation experiment. Open symbols present data measured after annealing. X-axis is slighted adjusted within each TID dose group for better reading.

Even though no electric field was applied during TID radiation, threshold voltage V_{th} was still greatly affected by radiation dose on all samples, as illustrated in Figure 5.11.

This means that a considerable part of holes generated due to radiation should have been captured within the oxide near interface even under zero-bias condition. The samples with HTGB of both 162 h and 332 h suffered in a larger manner with larger V_{th} shift. On top of that, considering the positive shift in V_{th} as Figure 5.8 shows, even though HTGB does amplify degradation during TID test, the total shift in V_{th} was still no larger than the one in non-HTGB samples compared to their virgin values.

❖ **Drain-source leakage current I_{dss}**

As shown in Figure 5.12, all samples suffered a higher drain-source leakage current with increased radiation dose. HTGB could mitigate this deterioration. However, leakage current of samples with 332 h HTGB is much larger than in 162 h HTGB ones. So regarding I_{dss}, HTGB combined with radiation do not produce similar trend as for V_{th}. This increased leakage levels either due to V_{th} lowering or sidewall/peripheral leakage path formation [151]. The latter one could especially dominate in thin gate oxide MOSFETs due to build-up of defects in the sidewalls of the shallow trench isolation oxide near the main conduction channel [152]. The shifts on V_{th} correspond well with the I_{dss} increase as shown in Figure 5.12, which indicates that leakage current should mainly be related to the degradation on V_{th}. Meanwhile, we suggest that although all the samples in TID benefit lower I_{dss} from HTGB, long HTGB samples (HTGB-332h) suffer higher leakage current due to formation of sidewall leakage path that results from additional activated defects near interface during long time HTGB compared to HTGB-162h samples.

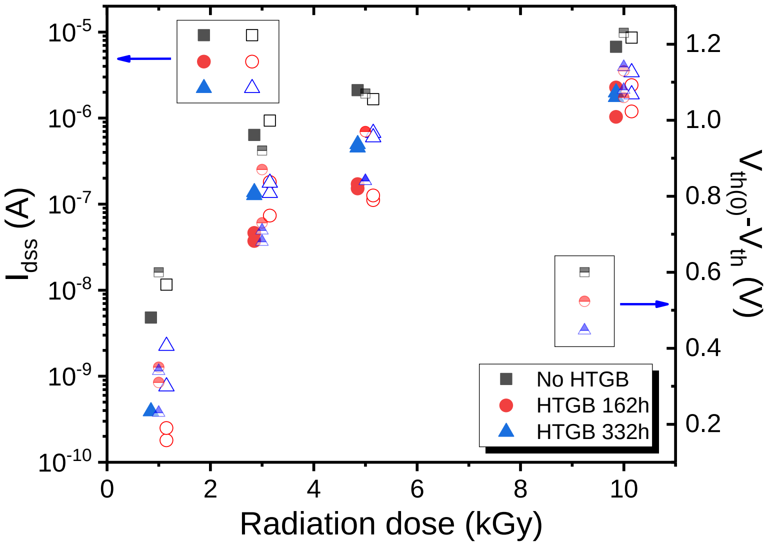


Figure 5.12. Drain-source leakage current @V_{ds} = 1200 V and the shift on threshold voltage as a function of radiation dose and HTGB time. Several I_{dss} much lower in 1 kGy group are not shown here. Open symbols present data measured after annealing and the half-filled symbols are the threshold shift compared to their original values. X-axis is slighted adjusted within each TID dose group for better reading.

❖ Gate leakage current I_{gss}

MOSFETs tested also suffered a higher gate leakage current I_{gss} under high radiation dose, as illustrated in Figure 5.13, which may be due to the charges captured in the gate oxide where the quality is relatively low by multi-trap assisted tunneling [153]. HTGB could possibly reduce this deterioration to a small extent. However, the recovery of I_{gss} at room temperature could be clearly identified especially in samples with higher dose, which is different from either V_{th} or I_{dss}.

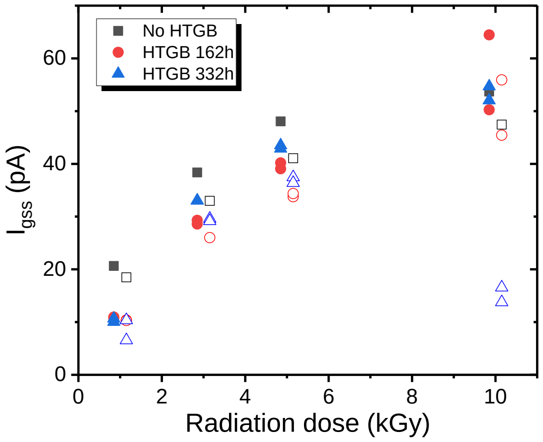


Figure 5.13. Gate leakage current @V_{gs} = 22 V as a function of radiation dose and HTGB time. Open symbols present data measured after annealing. X-axis is slighted adjusted within each TID dose group for better reading.

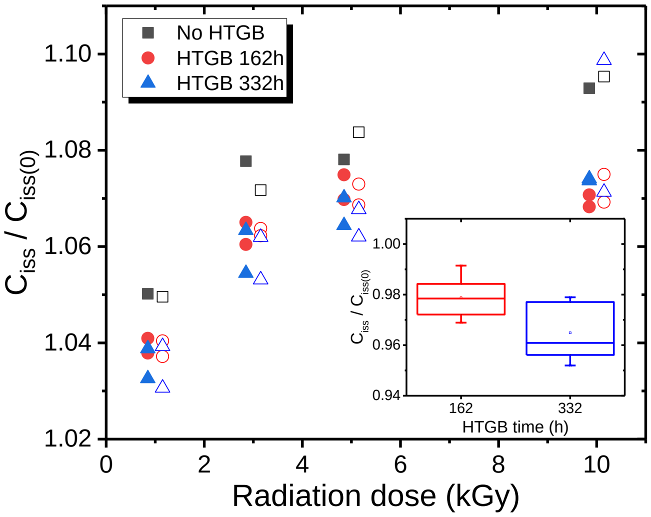


Figure 5.14. Normalized input capacitance @V_{ds} = 0.1 V as a function of radiation dose and HTGB time. Open symbols present data measured after annealing. X-axis is slighted adjusted within each TID dose group for better reading. The insert shows the variation of C_{iss} due to HTGB before TID.

❖ **Input capacitance** C_{iss}

Input capacitance increased with the increase of radiation dose (Figure 5.14). This increase was enhanced on samples with HTGB.

Annealing Effect at Room Temperature

Since some time-delay exists between sample collection after TID radiation and characterization, it is difficult to evaluate any quick annealing right after the radiation. However, almost no annealing was observed at room temperature except I_{gss} during our track for one week starting several hours after radiation. It is safe to say that no quick annealing was involved.

5.2.4 Discussion

The whole synergetic effects could be explained by a HTGB-assist-TID model as shown in Figure 5.15. A negative charged layer is generated after HTGB due to tunneling and capture of electrons. This will generate electric field that can accelerate the hole displacement during TID irradiation. However, as the electron-hole pairs' generation process takes place in each device, the influence on the accumulated electron layer should be neglected. In this case, the electric parameters shift would be enhanced with HTGB samples when focus only on TID process. Nevertheless, as the net charge near interfacial is more negative compared to the case of no HTGB samples, the total degradation is always lower if pre-HTGB is presented. This corresponds well with our result in V_{th} and C_{iss} .

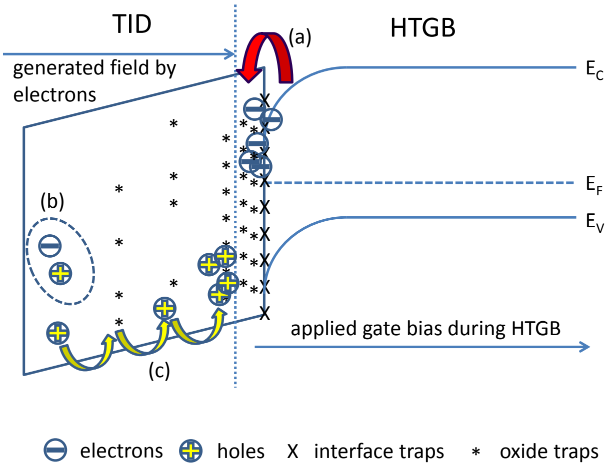


Figure 5.15. Illustration of band diagram near interface during HTGB (right) and TID (left), with the marked process (a): electrons directly tunneling and capture (b): electron-hole pairs generation due to irradiation and (c): holes displacement and capture.

As the synergetic effects mainly focus on charge capture near semiconductor/oxide interface, post-oxidation annealing in NO could be a candidate solution for reducing the instability due to traps passivation, especially those interface traps [154, 155]. Irradiation resisted dielectrics such as HfO_2 are also worth trying according to lower trapping efficiency during TID [156]. Meanwhile, proper pre-HTGB treatment (162 hours in this work) could greatly improve the performance after TID radiation, especially on drain-source leakage current, which could be of interest for further investigation.

5.3 Discussion

5.3.1 Freeze-out effect

According to Eq. (2.22) and (2.23), the measured capacitance under certain reverse bias should decrease gradually when the sample cools down. However, that is no longer valid under cryogenic temperature. As shown in Figure 5.16, two sharp drops of capacitance appear at around 40 K and 100 K on both forward and reverse bias conditions. Moreover, similar trend shows up among all the SiC devices tested including those SBDs with different metal contacts. This measured capacitance gap at 40 K with DLTS test has also been report by Menichelli et. al., and is contributed to the freeze-out of the shallow doping [66].

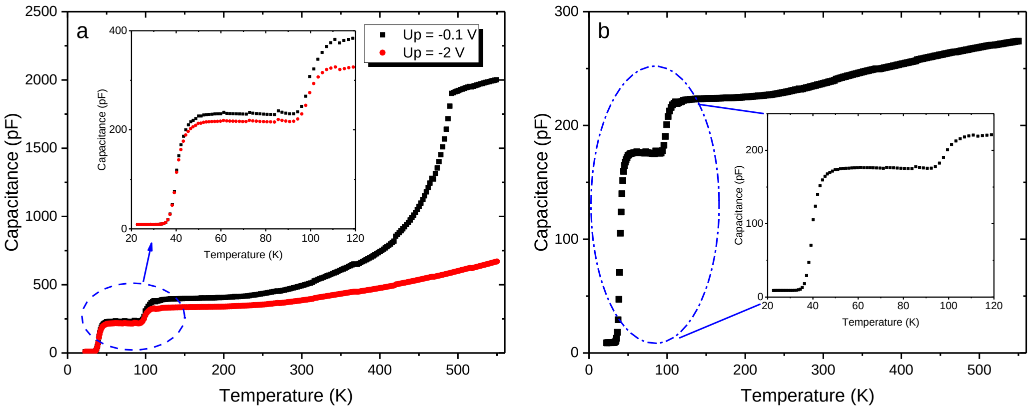


Figure 5.16. (a): pulse capacitance and (b): reverse capacitance with a bias of –10 V measured during DLTS scan between 20 K and 550 K on PiN diode discussed in section 5.1.

Even though energy level of shallow dopant usually lies near the conduction band (n-type) or valence band (p-type), a number of dopant will still be frozen and cannot be fully activated if the temperature is too low compared to their activation energy. These majority traps have been investigated through various techniques during experiments such as admittance spectroscopy on 6H-SiC [157] or traveling-wave method on 4H-SiC [158]. The more general case has been summarized by Los et al. as list in Table 5.6 [159].

Due to the structure especially the atomic stacking arrangement of either 4H- or 6H-SiC where two types of bonding namely zinc bonding (cubic) and wurtzite (hexagonal) exist, the activation energy of doping traps are separated with h-site (hexagonal) and k-site (cubic) respectively [7]. Therefore the capacitance gaps in Figure 5.16 present the transient region where carriers on certain site start to be frozen and trapped. And as a result, the traditional DLTS with capacitance measurement could no more provide the accurate results and the current DLTS or other types discussed in 3.4.1 should be used in low temperature region in order to extract the information on traps with the help of Arrhenius analysis.

Table 5.6. Activation energies of common SiC doping impurities summarized in [159].

	N donor	**Al acceptor**	**B acceptor**
4H-SiC	52.1 mV h-site 91.8 mV k-site	0.19-0.23 eV	0.258-0.39 eV
6H-SiC	81 mV h-site 137.6 mV k_1-site 142.4 mV k_2-site	0.20-0.25 eV	0.27-0.40 eV

5.3.2 Relationship between activation energy and capture cross section of certain defect level.

As is indicated by Figure 4.31, there seems to be certain relationship between the extracted activation energy E_a and its capture cross section σ for those trap levels with the same origin. Another two SBDs of Ti/W sputtering 1min (S4) have been investigated with the help of DLTS in order to reveal more details on this phenomenon.

- **Test setup**

In order to introduce the uncertainty, a diode with the largest surface (2.48 mm^2) labeled diode (L) and another with the smallest surface (0.155 mm^2) labeled diode (S) were involved in this test. DLTS have been taken out between 80 K and 400 K with numerous combinations of T_P and T_W , and the parameters extracted from Arrhenius plot are based on single period width which is different from that we did in Chapter 4. A bias range from −0.5 V (U_R) to 0.6 V (U_P) were adopted for all the DLTS scans which is commonly not recommended for DLTS as more noise will be involved if the pulse height ($U_P - U_R$) is too small.

- **Results**

As shown in Figure 5.17, a number of possible peaks labeled from A to J have been revealed with peak analysis from Origin software, while another peak K is marked for the diode (S) which may due to the signal noise of single point and can be neglected. Similar trap levels could be corresponded between these two diodes even though the height of peaks can vary a lot. This may due to the different surface conditions since the target region of DLTS test here is more closed to the interface and can be much easily influenced by noise. Three clear peaks namely A, E and H have been analyzed with DLTS Maximum Analysis in order to ensure the accuracy. However, not all combination of T_P and T_W resulted in the effective analysis on these three defect levels, and only those valuable data are used in the following discussion which leads to the difference on number of tests of these trap levels.

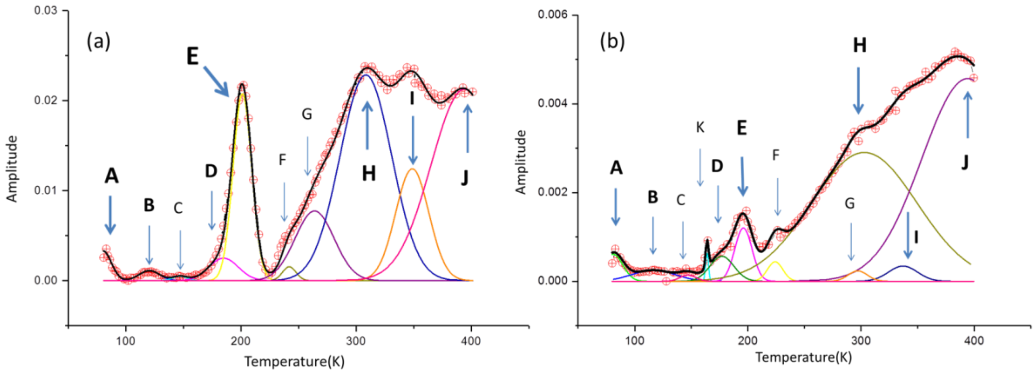


Figure 5.17. DLTS signal and the peak analysis by Origin on (a): diode (L) with T_P = 1 ms, T_W = 100 ms and (b): diode (S) with T_P = 1 ms, T_W = 200 ms between 80 K and 400 K. The sizes of the Alphabets represent the height of each individual peak.

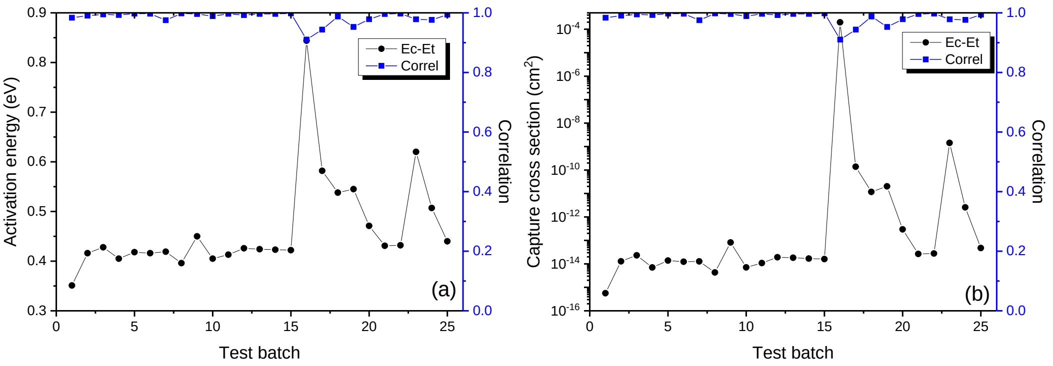


Figure 5.18. Extracted (a): activation energy relate to conduction band $E_C - E_T$ and (b): capture cross section as a function of the test batch with different T_P-T_W combinations of peak E on diode (L), along with their correlation on linear fitting during Arrhenius analysis.

As an example, the extracted activation energy and capture cross section of peak E on diode (L) are illustrated in Figure 5.18. Most of the analyzed results are well fitted with high correlation, especially the first 15 data. An interesting thing is that both activation energy and capture cross section in logarithmic coordinates have the same form, which indicates a linear connection between them. By plotting the log(σ) as a function of E_a as shown in Figure 5.19(a), a perfect line appears. This relationship suggests that even though the correlation of no. 16 point in Figure 5.18 is not high enough, this extracted data should still belong to the level of peak E. On the contrary, two points marked red in Figure 5.19(b) largely deviate from the linear fitting of other points, which suggests that these two points extracted from the Arrhenius plot may belong to other trap levels (e.g. peak I) or due to the experiment error during the analysis.

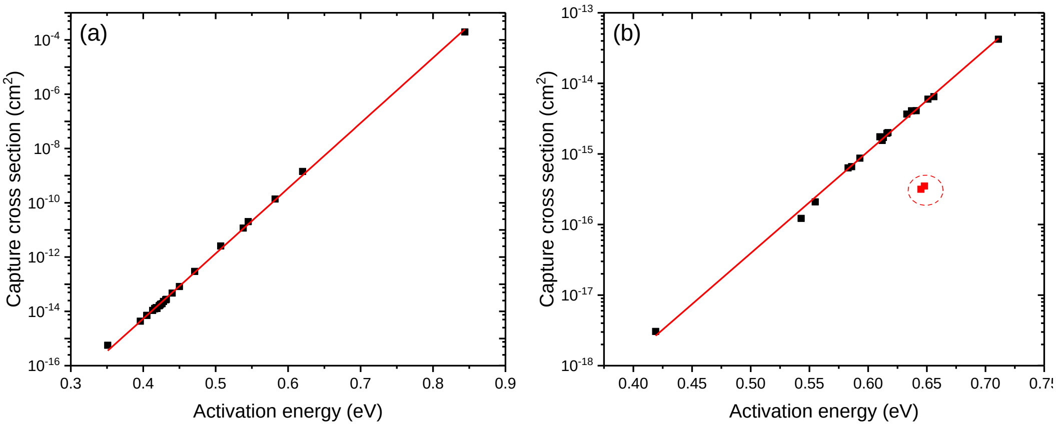


Figure 5.19. Linear relationship between activation energy and capture cross section of (a): peak E and (b): peak H on diode (L). Two points marked red in (b) are suggested to be the error data and are not used in the linear fitting.

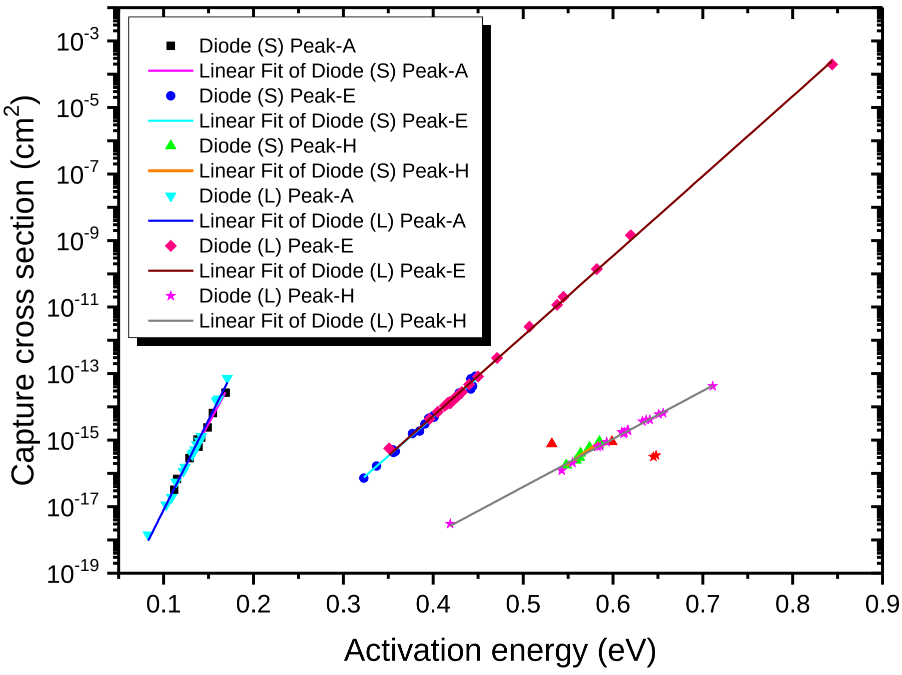


Figure 5.20. Linear relationship between activation energy and capture cross section of all three peaks (A, E, and H) on diode (L) and diode (S). Several points of peak H are suggested to be the error data and are marked red.

This linear relationship will be clearer if we draw all the points of three trap levels together, as shown in Figure 5.20. Although the overlap of extracted E_a exists between peak

E and peak H, three groups of fitting lines are distinct and relate to different peaks illustrated in DLTS signals. We define the analytical average here as

$$Avg(Y)=\frac{\sum_{n=1}^{N}\frac{Y(n)}{1-CorrelY(n)}}{\sum_{n=1}^{N}\frac{1}{1-CorrelY(n)}} \tag{5.4}$$

where Y could be either E_a, N_T or $\log(\sigma)$ and the $CorrelY(n)$ represents the corresponding correlation of fitting during Arrhenius analysis as explained in Figure 5.18. Therefore, the average parameters of each trap level could be calculated and listed in Table 5.7 along with the corresponding linear fitting parameters shown in Figure 5.20.

Table 5.7. Calculated trap parameters on average based on Eq. (5.4) along with he slope and intercept of linear fitting of each peak shown in Figure 5.20.

	Parameter	**Diode (S)**	**Diode (L)**
Peak A	Average E_a (eV)	0.142	0.131
	Average σ (cm^2)	1.23×10^{-15}	3.86×10^{-16}
	Average N_T (cm^{-3})	3.00×10^{11}	3.19×10^{11}
	Fitting slope	50.0	54.0
	Fitting intercept	–22.0	–22.5
Peak E	Average E_a (eV)	0.395	0.427
	Average σ (cm^2)	3.98×10^{-15}	2.32×10^{-14}
	Average N_T (cm^{-3})	1.51×10^{12}	2.43×10^{12}
	Fitting slope	23.6	24.0
	Fitting intercept	–23.7	–23.9
Peak H	Average E_a (eV)	0.568	0.608
	Average σ (cm^2)	5.69×10^{-16}	1.17×10^{-15}
	Average N_T (cm^{-3})	3.29×10^{12}	1.84×10^{12}
	Fitting slope	18.5	14.4
	Fitting intercept	–26.0	–23.6

The averaged trap parameters of each defect level are similar on both diodes, with a relatively large mismatch on peak H due to the complicity of the overlapped energies. On the other hand, those slopes and intercepts are also in great agreement on each peak, except the slope of peak H on diode (S) which is owing to the limited arrange of extracted data compared to diode (L) as shown in Figure 5.20. Meanwhile, whatever the diode is, the fitting intercept of all three levels are quite close to a value around –23 while the slopes are distinct on each peak. This indicates that certain relation between E_a and σ exists and can be expressed as:

$$\log(\sigma) = u \cdot E_a + v \tag{5.5}$$

where u and v are constant parameters only related to the trap. By using the natural logarithm and bringing Eq. (5.5) in the expression of Arrhenius plot [Eq. (3.10)], it can be deduced that:

$$\ln(\tau_e v_{th,n} N_C) = E_a \left(\frac{1}{kT} - u \right) - v \tag{5.6}$$

where the left part of the equation mark usually relates to the y-axis of the Arrhenius plot. This means that if the temperature equals $(ku)^{-1}$, the value of y-axis on Arrhenius plot should always be v when focusing on certain trap level. Or in other words, this ‘fixed point’ on Arrhenius plot indicates that at one trap level is easier to be discovered around this ‘fixed temperature’, which could be an intrinsic characteristics to separate different defect levels.

5.3.3 Annealing effect during DLTS

In addition to the annealing effect on trap level around 190 K as shown in Figure 4.22 and discussed in 4.3.22, the annealing (or to be more precise, the bias stress under high temperature scan) during DLTS will influence the trap levels that appear at higher temperature region as well.

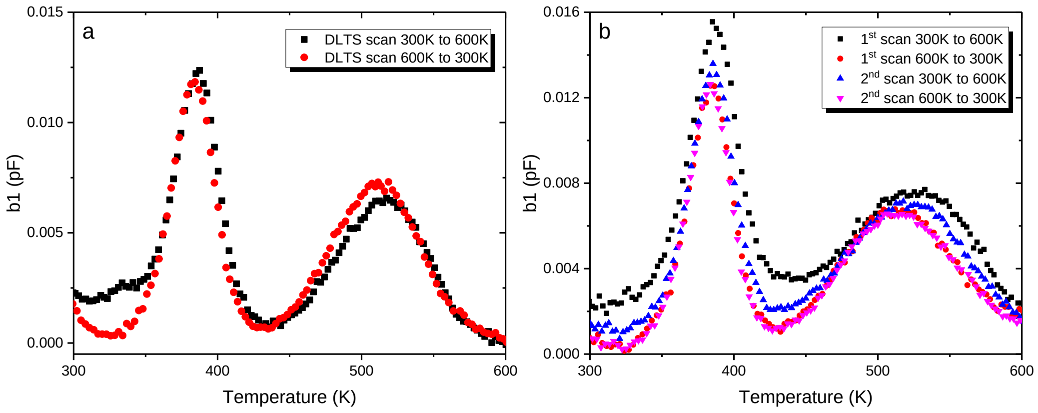


Figure 5.21. DLTS signal (correlation b1) with a period width of 204.8 ms on (a): Ti/W sputtering 1min sample (S4) and (b): Ni sputtering sample (S2) during temperature scan in different directions (heat up or cool down). The waiting time between scan of 300 K – 600 K and 600 K – 300 K is limited to minutes and can be neglected.

For example, ‘something’ diminished at around 330 K after two high temperature DLTS scan with different directions as illustrated in Figure 5.21(a), and this has been observed among all of the Schottky samples. However, the problem becomes more complicate when it comes to the Ni sample. As shown in Figure 5.21(b), another possible trap level at around 430 K diminished after annealing, and the mismatch of the peak position on temperature shows up. This shift on maximum of the peak owing to the error of temperature record by sensors, but can be ignored if we only compare the signal height. Furthermore, the whole signal height decreases after each scan cycle (300 K – 600 K – 300 K) and recovers at room to a certain degree, which is similar to but different from that shown in Figure 4.22. Considering that the signal of cooling down on Ni diode during both 1st and 2nd scans well overlaps, this vanished signal height should present as the unique ‘white noise’ of trap levels in Ni SBDs (e.g. the fast states at interface with a distribution of E_A and σ [160]) and can be totally removed by high temperature-bias stress process.

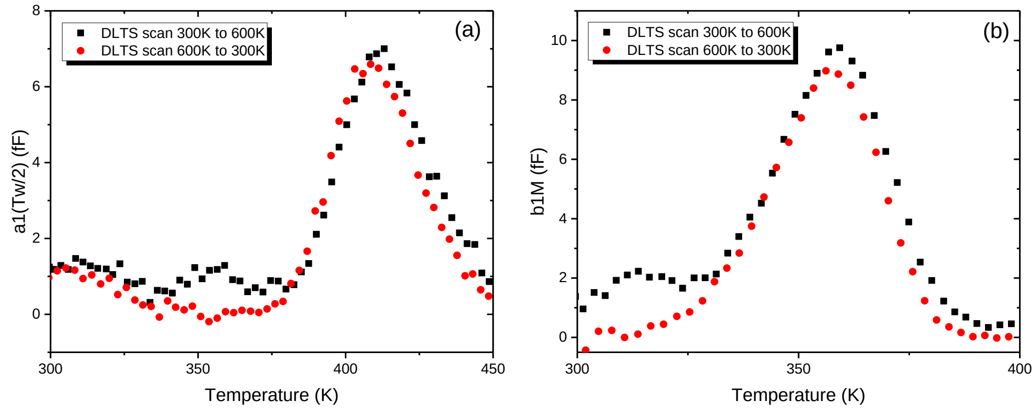


Figure 5.22. Signal DLTS on different correlations (a): a1(Tw/2) and (b): b1M on the Ti/W sample with the same scan 300 K – 600 K – 300 K as in Figure 5.21(a).

Table 5.8. Extracted trap parameters on Ti/W and Ni samples with the help of Maximum (maximum Arrhenius analysis) and HERA analysis.

Sample	**Tool**	**E_a (eV)**	**σ (cm^2)**	**N_T (cm^{-3})**
Ti/W	Maximum	0.667	2.83×10^{-16}	6.58×10^{11}
	HERA	0.720	2.80×10^{-15}	5.52×10^{11}
Ni	Maximum	0.661	1.91×10^{-16}	7.01×10^{11}
	HERA	0.676	2.40×10^{-16}	6.76×10^{11}

Other correlation functions are also involved to analyze the disappeared trap level around 330 K, and this peak is much clear shown with certain correlation parameter such as a1(Tw/2) and b1M as illustrated in Figure 5.22. In order to cut back the error from the strong trap levels near our target, both HERA and maximum analysis have been used to extract the trap parameters. Those Arrhenius results are listed in Table 5.8 which indicates that they originate from the same defect level with activation energy near 0.67 eV where the $Z_{1/2}$ are usually reported. However, no more reference can be obtained on this trap level found here. Unfortunately, the trap level appears at 430 K of the Ni sample cannot be precisely analyzed due to the significant influence on defect levels at 380 K and 530 K.

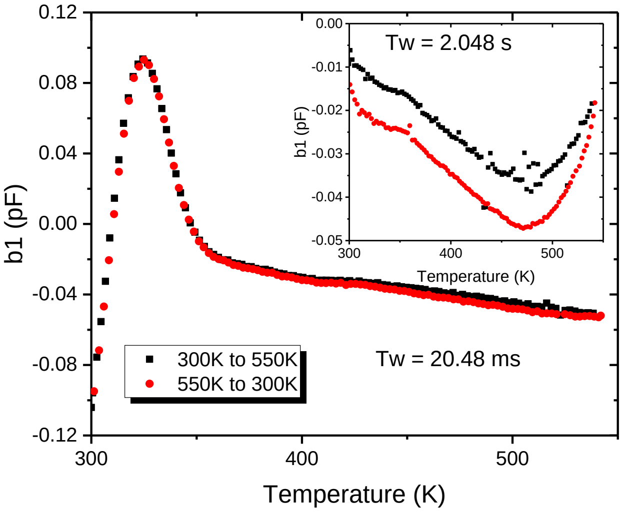


Figure 5.23. DLTS signal (correlation b1) between 300 K and 550 K on PiN diode discussed in section 5.1 with a period width of 20.48 ms and 2.048 s (top-right plot). Before the DLTS scan 550 K – 300 K, an additional waiting time of 30 min are applied with tiny bias (–0.1 V) right after the heat-up scan (300 K – 550 K).

On the other hand, no specific trap levels disappear on PiN diode after high temperature DLTS scan, as shown in Figure 5.23. Meanwhile, only the increase (negative shift) on the peak near 500 K has been observed, and this difference is clearer revealed with large T_W . One assumption is that the trap level found above among all SBDs is influenced by the hole trap level in PiN diode, and as a result, the vanishing of this trap level cannot be observed.

In short, considering also the results discussed in 4.3.22, the high temperature DLTS scan does influence the DLTS results namely trap conditions. This can be quite significant especially when that leads to the disappearance of certain trap levels, and should be taken special care of. Therefore in this paper, all DLTS results given for device characterization are those temperature scan after a first high temperature scan (usually 300 – 550 – 300 K) in order to rule out the influence of that.

5.3.4 Negative-U center

As has been discussed in 5.1.4 where an abnormal peak shows up at around 80 K (Figure 5.5), this irregular phenomenon has also been uncovered on those SBDs. Figure 5.24 shows the DLTS spectra with 3 values of T_W . Except that around 80 K, a clear trend for all peaks is revealed from the spectra: peaks shift to left with large period width while their heights slightly increase. This increase on signal heights is normally owing to the change of reverse/pulse capacitance at different temperatures. However, even if this trend of signal height is taken into consideration, the peak at around 80 K with T_W = 2.048 s should be the dash line illustrated in Figure 5.24(b) rather than the experimental one.

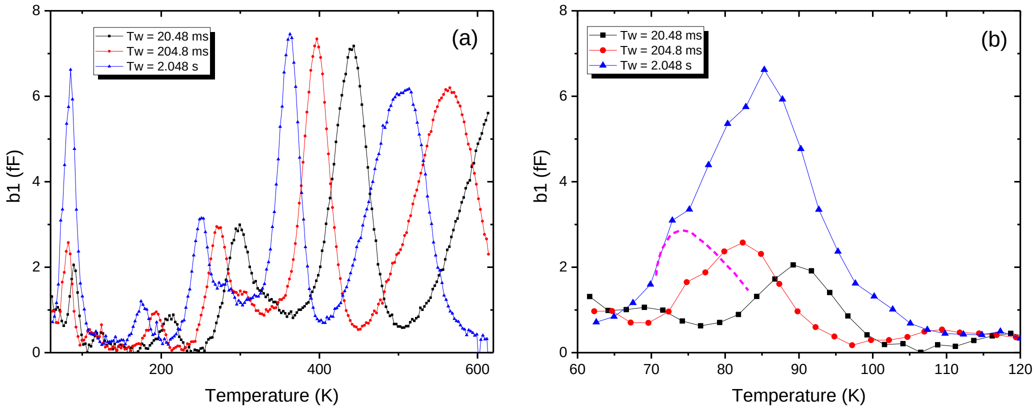


Figure 5.24. DLTS spectra with 3 different period widths on diode Ti/W liftoff (S3) between (a): 60 K and 600 K, while (b) is the same signal between 60 K and 120 K in order for better illustration, with $U_R = -10$ *V,* $U_P = -0.1$ *V and* $T_P = 100$ *µs.*

In order to study this irregular peak at around 80 K, DLTS has been taken out on Tungsten sample (S7) that also presents this strange behavior, with more T_W and smaller steps as shown in Figure 5.25(a), while more intuitional description can be obtained from its plot in 3D (Figure 5.26). As illustrated in the 3D-plot, 2 distinct peaks can be recognized: a normal peak with its center temperature shifts to left under large T_W (black dash line), and an abnormal one with its center temperature moves to right when the period increases (red dash line). Meanwhile, the height of both peaks changes differently: the peak heights of normal one almost keeps constant with the period less than 2 s, and dramatically decrease with increase of T_W . On the other hand, the special peak overlaps with the normal one and cannot be well separated with T_W less than 1 s, while greatly increase with large period width. This can somewhat explain the only irregular signal with the period width of 2.048 s shown in Figure 5.24(b). Furthermore, a negative peak appears at 80 K with large T_W which may lead to the sharply decrease of normal peak height. However, this negative peak is unrealistic to analyze due to lack on experimental data.

In order to study on this special peak, the Arrhenius plot is used according to search on maximum peak position with various correlations. As can be seen in Figure 5.25(b), an irregular but perfect fitting line shows up as presented by the red circles in addition to the normal peak (black squares). However this special peak can be only found in those correlations of 'series b or sine coefficients' namely the odd items in the Fourier transform which results in relatively less points presented on the Arrhenius plot of the special peak. Since the slope of fitting line in the Arrhenius plot corresponds to the activation energy, the negative slope of special peak indicate the existence of negative activation energy which cannot be analyzed by our DLTS software rather than the positive activation energy obtained from the positive slope of the normal one. And this negative activation energy is different from the hole trap discovered in p-n junction with the help of negative peak in the DLTS spectra, which highlights its particularity.

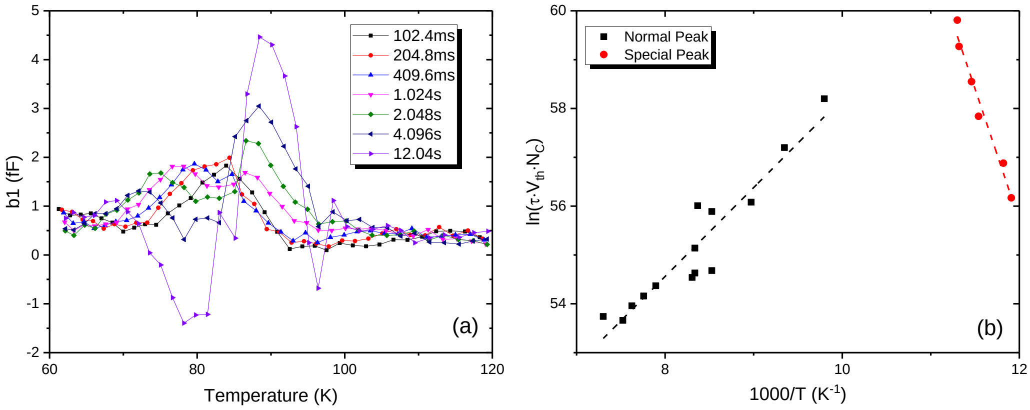


Figure 5.25. (a): DLTS spectra (b1) between 60 K and 120 K with 7 different period widths on Tungsten diode (S7) and (b) is its Arrhenius plot extracted.

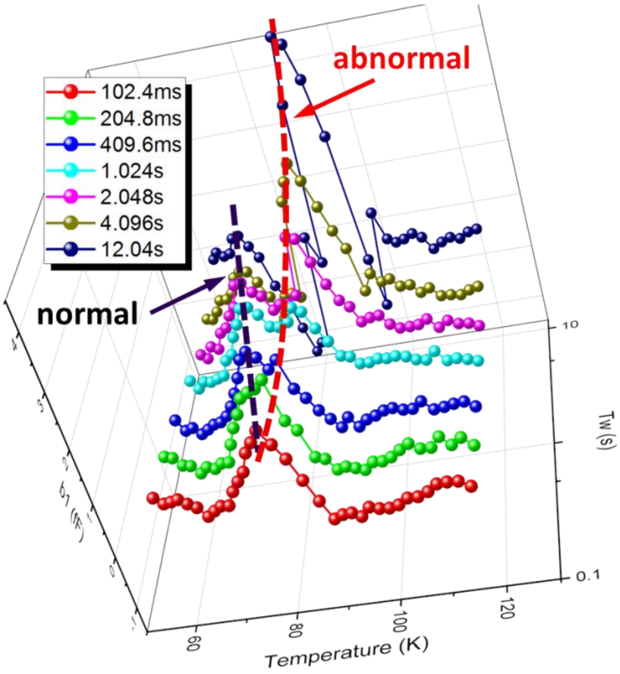


Figure 5.26. 3D-plot of Figure 5.25(a). The blue and red dash lines indicate the evolution trend on two peaks.

This irregular peak detected can be partly explained with the negative-U system. If a defect can trap two electrons (or holes) while the second bond is more tight than the first one, it can be regarded as a negative-U system or with the negative-U properties [161]. For example, three possible charge states (D^+, D^0 and D^-) exist for a simple point defect with a single donor (0/+) and acceptor (–/0) level. However, if it has negative-U properties, the neutral level D^0 can be no more stable. Instead of stay neutral, certain process will take place as

$$2D^0 \to D^+ + D^- + |U| \tag{5.7}$$

where U is the energy between donor and acceptor level.

As a results, if Fermi level coincident the half way between the donor and acceptor levels, there will be the compound of D^+ and D^- rather than D^0.

The negative-U centers have been observed not only in 4H- ($Z_{1/2}$) and 6H- ($E_{1/2}$) SiC [162-164], but also in 3C-SiC [165], and have been suggested to result from the carbon vacancies (V_C) with the *first-principles* calculations [165, 166].

As a feature of negative-U center, the DLTS signal height should be twice the trap concentration since during the emission process that

$$D^- \to D^0 + e^- \to D^+ + 2e^- \tag{5.8}$$

If the second emission process is much faster than the first one, almost no time delay appears before the neutral level loose its second electron. Therefore, second emission will not show up as a peak in DLTS signal and instead, the signal height of the first process is doubled due to the emitted electrons on pair. However, as has been pointed out by Dobacrewski, the neutral can stay at a high concentration with a certain time during the same process if the emission rate of D^- level is much larger than D^0 [167].

Based on the negative-U system, the special peak that appears at around 80 K in our DLTS experiment can be explained by the combination effect of emission and capture in the negative-U trap. It is suggested that the emission rate of D^- is smaller than D^0, and most of the traps stay at D^0 because the pulse width is not long enough for all traps enter the balance states as indicated by Eq. (5.7). In that case, after U_P withdraws, not only the emission of neutral level (second process in Eq. (5.8)) takes place, but also the process indicated by Eq.(5.7) and could be somewhat the major process. However, only the emission can be detected in this stage since no electron is released in Eq.(5.7). As a result, only the emission from neutral level appears in the DLTS signal with small T_W. On the other hand, after the first stage entering its end where certain traps become negative charged, the whole process in the Eq. (5.8) becomes major, which results in the extremely high peak in DLTS signal detected with large period width. Furthermore, the negative activation energy extracted from the special peak in Figure 5.25(b) is due to the process implied by Eq. (5.7) in first stage works with energy emission. Or in other word, instead of the conventional emission process with energy absorption, this energy emission process is presented by the negative activation energy in the Arrhenius plot. Meanwhile, the phenomenon that the height of special peak in DLTS signal increases with large T_W is owing to either slow process of emission from D^- or the less freeze-out effect at higher temperature.

5.3.5 Behavior at extremely low temperature

As mentioned in 4.3.22, the behavior can be quite weird under extremely low temperature (below 20 K). On the other hand, the investigation method is limited due to either freeze-out effect or the restriction of our DLTS system (the valid temperature is limited to 15 K). As a result, the isothermal DLTS becomes the main tool for research on this low temperature region.

- **Tempscan below 25 K**

In the previous study on SiC SBD within the temperature range of 20 K – 60 K, the signal increases towards lower temperature part near 20 K, as presented by the black squares in Figure 5.27, which indicates the existence of higher peak at lower temperature, or in other words the additional trap levels with large concentration and tiny activation energy can be forecasted. This is true if we expend the temperature until 15 K, as shown by the red circles. However, owing to the temperature restriction, the whole profile at low temperature cannot be drawn by using the DLTS tempscan even another clear peak appears at 20 K.

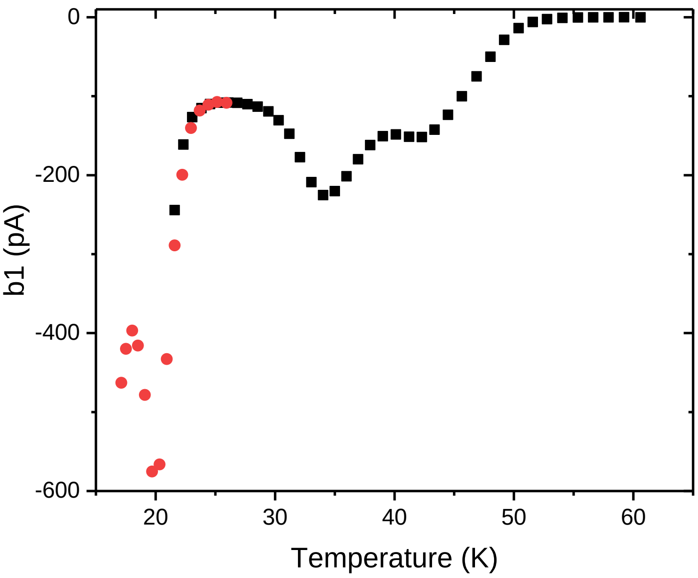


Figure 5.27. I-DLTS signal (correlation b1) on Ti/W sputtering 1 min sample (S4) at low temperature. The black squares are that discussed in Chapter 4, while the red circles are the focus in this section.

In order to investigate these trap levels at extremely low temperature, the isothermal DLTS have been adopted. The ITS have been measured between 15 K and 25 K with a temperature step of 0.5 K, which is much smaller than the one commonly used (~ 10 K). Both positive and negative peaks show up after ITS of I-DLTS, and the results of Arrhenius analysis are shown in Figure 5.28. Even with different bias condition, similar trap levels are extracted with $E_a \approx 0.03$ eV and $\sigma \approx 1\times10^{-15}$ cm^2. As the electron trap levels reported in 4H-SiC closest to the conduction band are those defect of nitrogen with E_a around 0.05 eV [70], it is hard to sort these two trap levels with lower E_a. Meanwhile, it is hard to make a conclusion about the accuracy of determined levels owing to the small step used in ITS test although both levels in Figure 5.28 are rather linear fitted. Whatever, it is sure that some traps do exist at low temperature with large concentration.

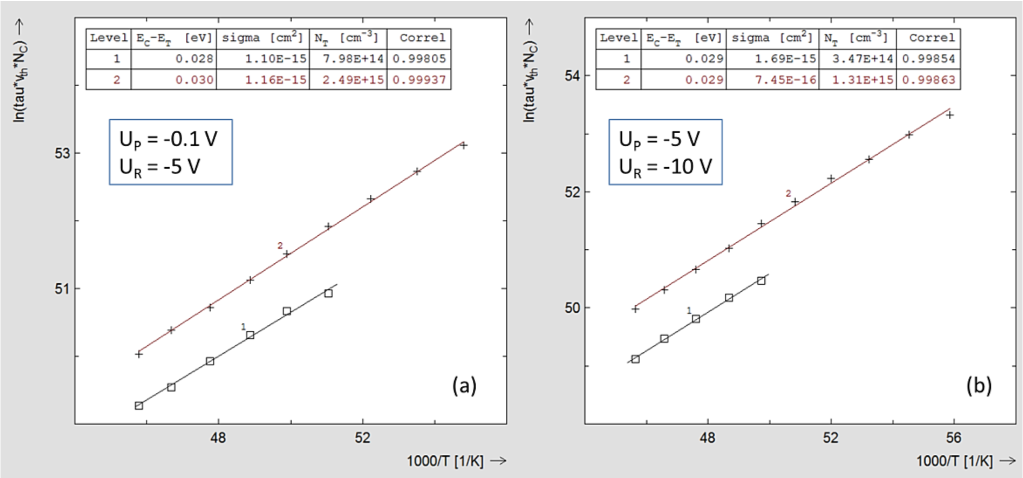


Figure 5.28. Arrhenius plot from maximum analysis of DLTS on diode S4 at temperature below 25 K. The pulse width is 5 µs and the bias condition on (a) and (b) are listed inside plot. Some points extracted with maximum analysis that do not belong to these two levels are not shown in the plot.

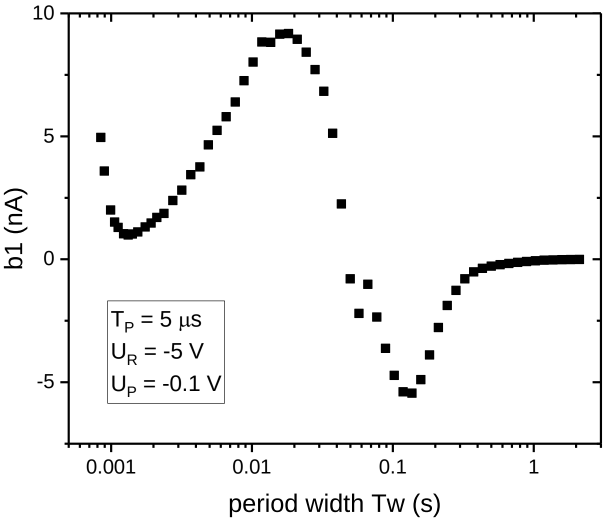


Figure 5.29. I-DLTS signal (correlation b1) from ITS period scan at 17.35 K on sample S4 with $T_P = 5\ \mu s$, $U_R = -5\ V$ and $U_P = -0.1\ V$.

Further studies on these trap levels at low temperature have been taken out at the lowest temperature available on sample (~17.5 K) in our DLTS system with isothermal

DLTS tests. As shown in Figure 5.29, two clear peaks show up with different signs in the period width scan, while the region at lower period width part (< 0.6 ms) that is limited by the measurement also draws attention.

As I-DLTS commonly presents those trap levels as negative peaks, two minima (~ 200 ms and 1 ms) have been specially focused on as well as the blank region (T_W < 600 μs) in Figure 5.29 with T_W chosen as 200 μs.

- **ITS T_W = 200 ms**

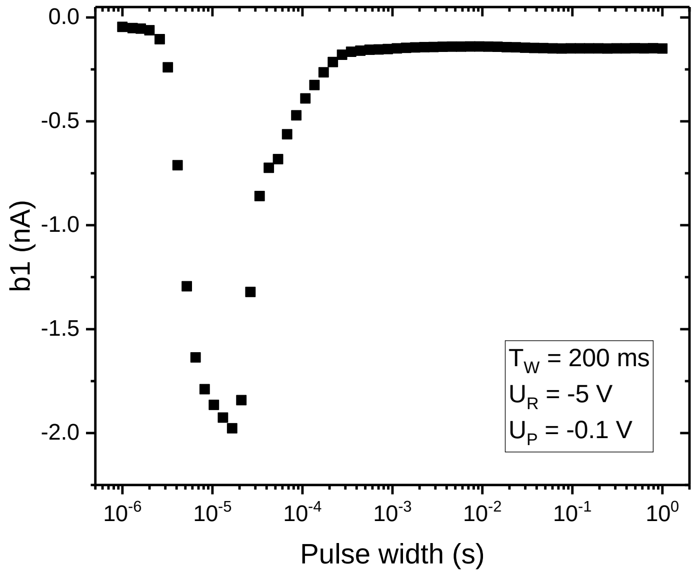


Figure 5.30. I-DLTS signal (correlation b1)of isothermal variation of T_P at 17.35 K with a fixed period width of 200 ms.

As shown in Figure 5.30, only negative signal is obtained with the period width of 200 ms. However, different from the normal ITS with variation of T_P which performs as a monotonic function, a peak with a minimum value shows up with T_P near 20 ms. It is suggested that there are at least two highly compensated trap levels with opposite defect types and different σ. Therefore it appears as the traditional trap when the capture of the normal trap level takes charge at small T_P, while it saturates and the compensation effect take place due to additional trap level at large T_P. Finally, signal trends to zero when the pulse is large enough where high compensation is reached due to relatively closed active concentration. Another possibility relates to the negative-U center discussed in the previous chapter. If the trap levels detected here come from the negative-U center, this abnormal behavior can be explained as the majority captured levels with different pulse width. It is assumed that only the fast emission process can be detected with the period width of 200 ms, while the signal that originates the slow progress can be neglected. As a result, most of the trap levels are occupied as D^o with small T_P, and the fast process presents as the negative signal in Figure 5.30. However, more and more traps will be in the D^- states when T_P becomes larger, and finally almost all defects are trapped as D^- centers if T_P is large enough. Since the emission form D^- level is limited and presented as slow process, it can hardly be detected and this contributes to the tiny negative signal at large T_P. As the negative-U center can be regarded as two trap levels, only the condition of two trap level with opposite defect types will be further discussed, and those conclusions can be applied to the case of negative-U centers as well.

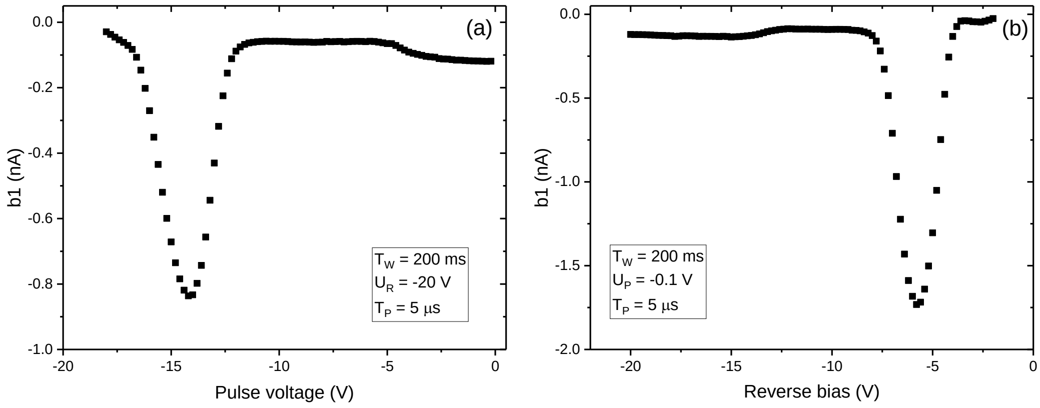


Figure 5.31. I-DLTS signal (correlation b1)of isothermal variation of (a): U_P and (b): U_R at 17.35 K.

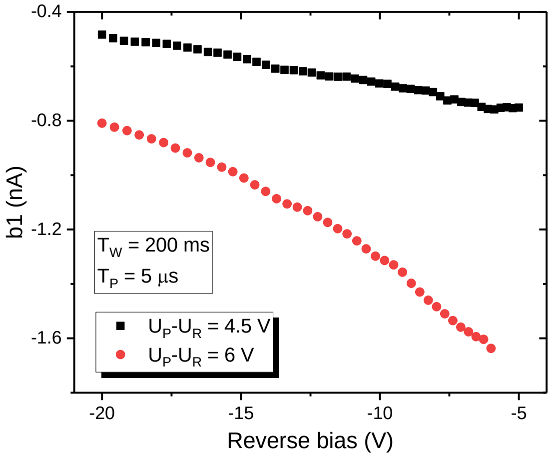


Figure 5.32. I-DLTS signal (correlation b1)of isothermal variation of both U_P and U_R with pulse heights keep constant.

However, more interesting results can be found from Figure 5.31, where a negative peak and one negative shoulder can be clearly identified in both plots. This reveals the existence of third trap level. Due to the mirror relationship between Figure 5.31 (a) and (b), it can be assumed that the major trapping level that determines the measured DLTS signal only depends on the voltage difference $U_P - U_R$ during the transient process, and this is verified by Figure 5.32, where the transient type is somewhat fixed with constant $U_P - U_R$ value.

Table 5.9. Extracted V_I of sample S4 at different temperature according to C-V analysis measured by DLTS system during the tempscan.

Temperature (K)	V_I **(V)**	**Correlation coefficient of linear fitting**
21.84	17340	0.502
29.33	2175	0.946
38.18	6.5	0.999
48.48	1.5	0.999

Even though the conventional C-V analysis discussed in section 2.3.2 can no longer provide precise results at extremely low temperature owing to the carrier freeze-out effect, it can still be a reference for approximation. It can be found from Table 5.9 that V_I becomes so huge that $V_I \gg (|U_R| + |U_P|)$ at low temperature with worse linearity where carrier freeze-out occurs. As a result, the approximation of the effective detection zone w_{eff} can be expressed as:

$$w_{eff} = w_R - w_P \propto \sqrt{V_I - U_R} - \sqrt{V_I - U_P} \approx \frac{U_P - U_R}{2\sqrt{V_I}} \tag{5.9}$$

where w_R and w_P are the widths of depletion region at reverse bias and pulse condition.

Therefore the electric distribution within the effective zone that relates to only w_{eff} if the doping near interface is assumed uniform is determined exclusively by the bias difference $U_P - U_R$ at a fixed low temperature. In that case, the weird behavior in Figure 5.31 can be caused by the Poole-Frenkel effect under strong electric field of at least one trap level at high $U_P - U_R$.

❖ ITS T_W = 1 ms

The 3-phase evolution (a-b, b-c and c-d) is clearer shown in Figure 5.33 with a period width of 1 ms, which indicates the existence of a pair of compensated defect levels and another cluster trap level. However, the sign is somewhat opposite compared to that shown in Figure 5.30. Furthermore, even though the normal signal obtained can offer its relatively large concentration during the isothermal test with variation of bias under small $U_P - U_R$ condition, as illustrated in Figure 5.34(a), the circumstance becomes much complicated with large $U_P - U_R$ as (b) shows. On the other hand, Figure 5.34(a) can be regarded as part of the signal in (b) with U_P less than –10 V. This will be discussed in detail in the case followed (T_W = 200 μs) with similar condition.

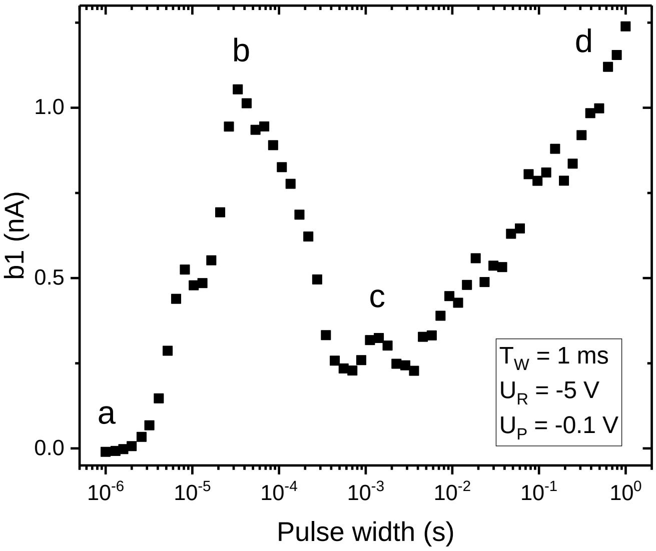


Figure 5.33. I-DLTS signal (correlation b1)of isothermal variation of T_P at 17.35 K with a fixed period width of 1 ms.

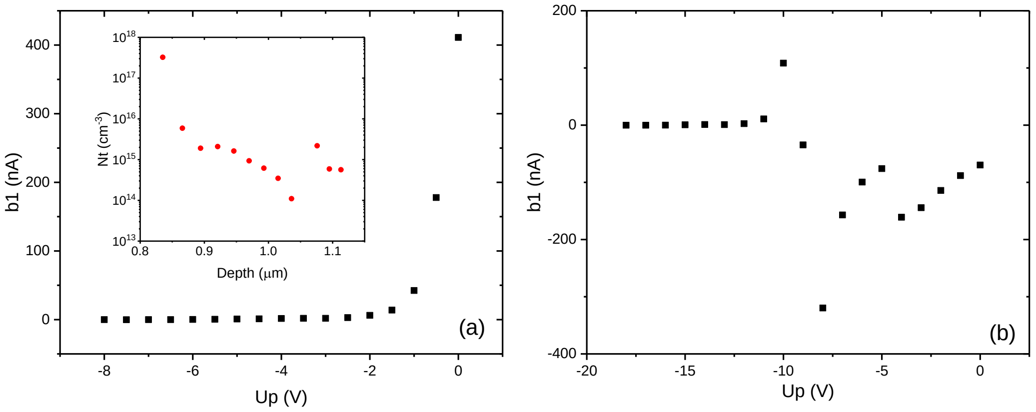


Figure 5.34. I-DLTS signal (correlation b1)of isothermal variation of U_P at 17.35 K with (a): U_R = –10 V and (b): U_R = –20 V. The pulse width is 30 μs and period width is 1 ms. Inner plot in (a) shows the trap concentration profile calculated based on results in (a).

❖ ITS T_W = 200 μs

In order to draw a brief profile of the trap presented at low T_W where no information has been provided by ITS scan shown in Figure 5.29 due to system limitation, a period width of 200 μs was chosen for further investigation. The scan of T_P shown in Figure 5.35 is more closed to the one discussed above with T_W = 1ms (Figure 5.33). The 3-phase (a-b, b-c and c-d) in the plot presents 3 different trap levels, which corresponds with the previous results and can be examined by those transient curves illustrated on the right part of Figure 5.35. However, the height of signal tend to decrease at large T_P, which is different from the case of either T_W = 1 ms or 200 ms.

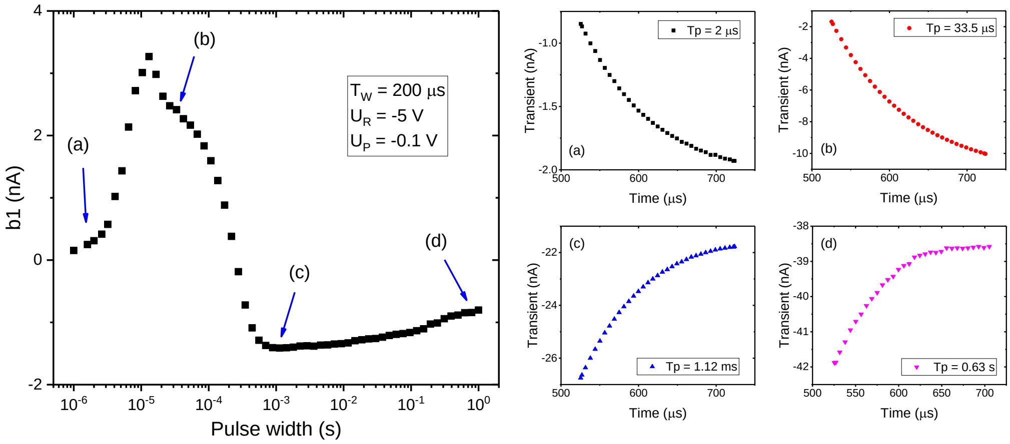


Figure 5.35. Left plot : I-DLTS signal (correlation b1)of isothermal variation of T_P at 17.35 K with a fixed period width of 200 µs. And right plot: the measured transient curve at different T_P in the left plot.

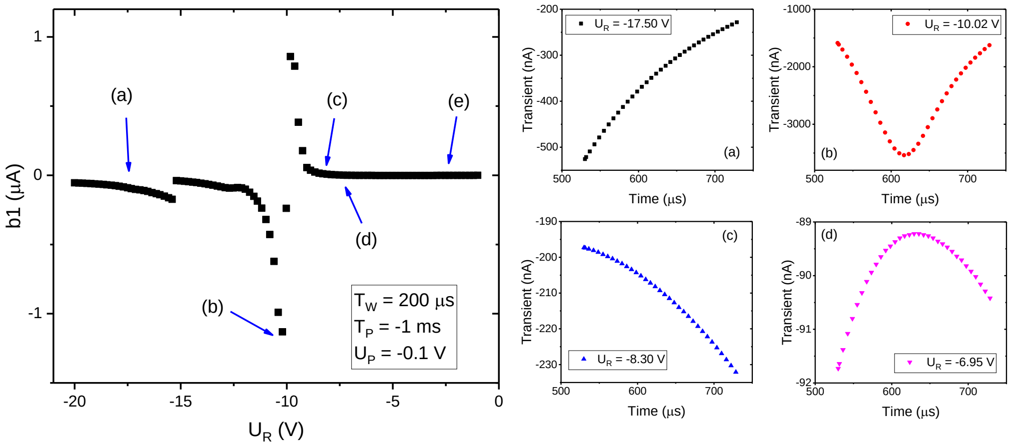


Figure 5.36. Left plot : I-DLTS signal (correlation b1)of isothermal variation of U_R at 17.35 K with a fixed period width of 200 µs. And right plot: the measured transient curve at different U_R in the left plot.

The isothermal with variation of U_R has also been taken out with a period width of 200 µs. As shown in the left plot of Figure 5.36, the signal is similar to that shown in Figure 5.34(b), but should be regarded as mirror relationship, which indicates the dependence on only pulse height $U_P - U_R$ as has been discussed with Figure 5.31. Furthermore, the transient information presented in Figure 5.36 describes the signal evolution, which is illustrated in Figure 5.37. (The transient curve with the label (e) is similar as that of (a), but not shown in the plot owing to the limitation of space.) In order to simply the discussion, the transient is regarded as ‘positive’ if the corresponding DLTS signal (b1) is positive such as (c), and the ‘negative transient’ describe those transients result in negative DLTS signal for example (a) and (e). Therefore at low pulse height the transient is negative, and the amplitude increases when the pulse height rises up. After a minima point is reached around (b), the transient become positive until its maxima (d). If the pulse is high enough, it enters the region (e) with a trend as one normal trap level.

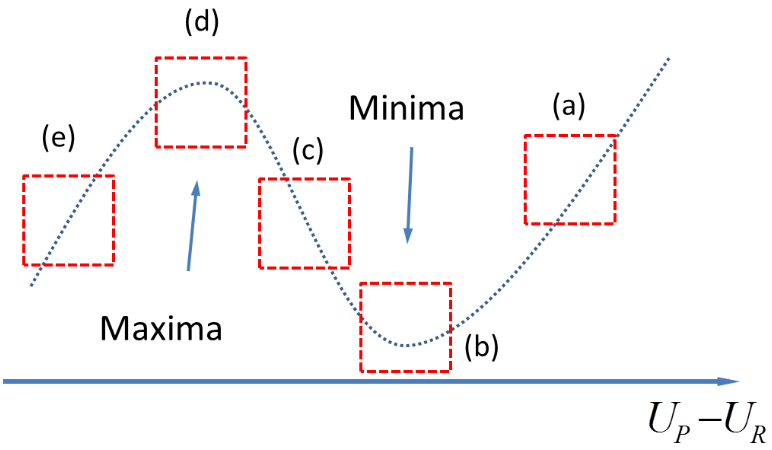


Figure 5.37. Relationship between the observed transient curve and $U_P - U_R$ during the DLTS shown in Figure 5.36. The blue dots surrounded by rad dash square indicate the measured transient signals which correspond to that in Figure 5.36 with the same label.

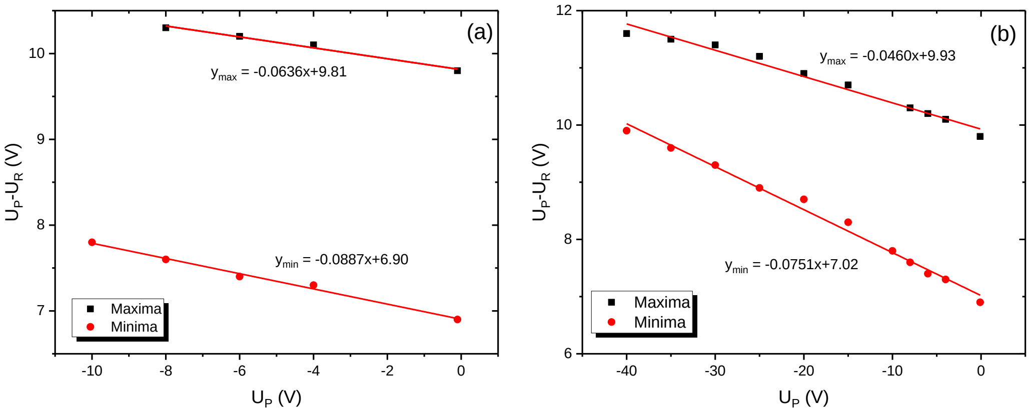


Figure 5.38. The maxima and minima voltage illustrated in Figure 5.37 as a function of pulse voltage used in the DLTS isothermal variation of U_R measures. Different voltage sources were used that (a): low voltage module up to 20 V and (b): high voltage module up to 100 V.

In order to verify if the type of transient depend only on pulse height, the maxima and minima voltages illustrated in Figure 5.37 [(d) and (b)] are extracted based on either isothermal variation of U_R with different U_P values (Figure 5.38) or variation of U_P with different U_R values (Figure 5.39). It is clear that pulse height at both maxima and minima stay linear at low bias (within –20 V), while the linearity drops at high bias condition (up to –50 V). Even though less precise on voltage can be achieved when using high voltage module exceed –20 V, this system error can never lead to the same trend on linearity that the slope become less negative with large bias on both sample and points studied.

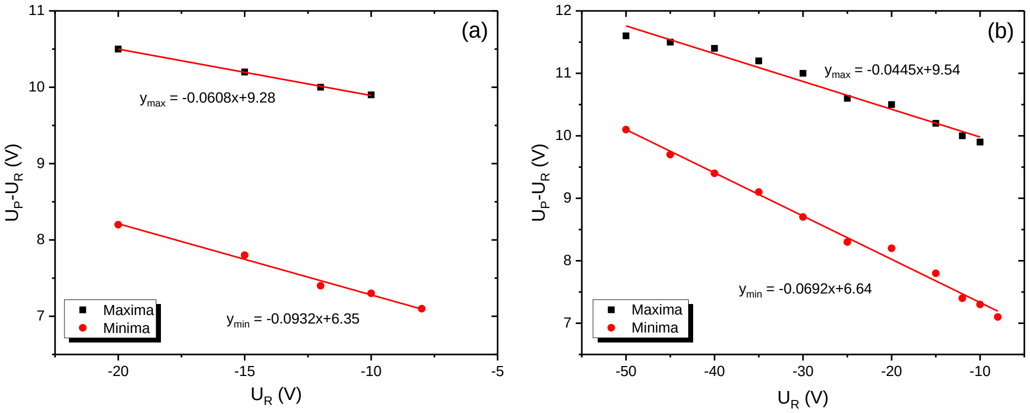


Figure 5.39. The maxima and minima voltage illustrated in Figure 5.37 as a function of reverse bias used in the DLTS isothermal variation of U_P measures. Different voltage sources were used that (a): low voltage module up to 20 V and (b): high voltage module up to 100 V.

On the other hand, this linear trend can be deduced with the help of Eq. (5.9). Here the pulse height U_H is defined as $U_H = U_P - U_R$, therefore the depletion width at fixed temperature is only related to that:

$$w_{eff} \propto \sqrt{V_I - U_R} - \sqrt{V_I - U_P} = \frac{U_H}{\sqrt{V_I - U_R} + \sqrt{V_I - U_H - U_R}} \qquad (5.10)$$

In order to keep the depletion constant at different bias condition, Eq. (5.10) should results in a constant value c, therefore U_H can be written as:

$$U_H = c\left(\sqrt{V_I - U_R} + \sqrt{V_I - U_H - U_R}\right) \qquad (5.11)$$

by ignoring the U_H in the square root term, the differential can be expressed as:

$$\frac{\partial U_H}{\partial U_R} = -c\left(\frac{1}{2\sqrt{V_I - U_R}} + \frac{1}{2\sqrt{V_I - U_H - U_R}}\right) \qquad (5.12)$$

According to Eq. (5.12), when the bias is small compared to V_I the plot of U_H vs. U_R is linear with a negative slope value proportional to $V_I^{-1/2}$. As the bias becomes larger, U_R can no more be neglected and results in the smaller value of the slope magnitude of linear fitting. This corresponds well with the experimental results. The conclusion is similar when U_R is replaced by U_P from those isothermal tests with variation of U_R as is shown in Figure 5.38. By comparing Figure 5.38(a) and Figure 5.39(a), it can be found that the slopes are closed to each other on either minima points or maxima points, which means the feasibility of the approximation made at low bias condition.

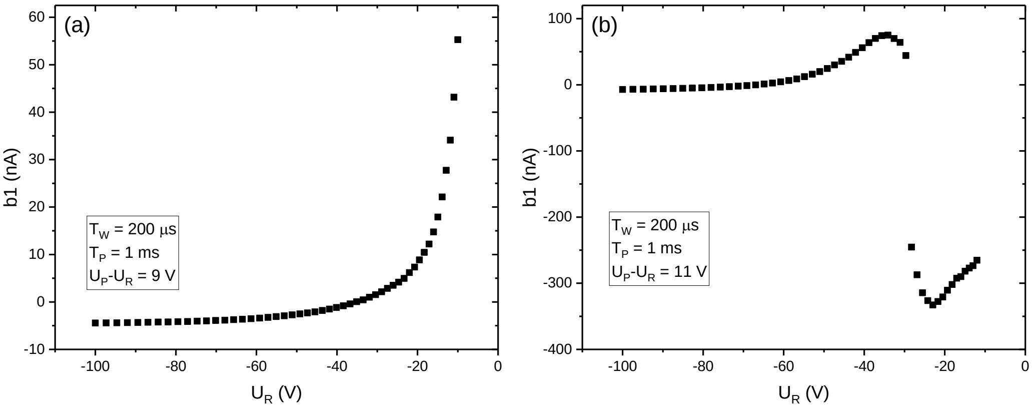


Figure 5.40. I-DLTS signal (correlation b1)of isothermal variation of U_P and U_R at 17.35 K with fixed difference of (a): $U_P - U_R = -9$ V and (b): $U_P - U_R = -11$ V.

Since the transient type mainly depends on U_H, conventional isothermal DLTS curve with bias variation can be obtained by selecting proper U_H, for example Figure 5.40(a). Meanwhile, since the quasi-linear relationship on U_H with U_R or U_P is suggested, change of transient type can still be observed under certain circumstance as shown in Figure 5.40(b) even though the U_H is set constant.

Even though the behavior of trap at extremely low temperature has merely been studied and the mechanisms contributing to these performances discussed above is not yet clear, this work still provide a possible way to snoop the trap with tiny activation energy at low temperature. Meanwhile, certain trap behavior can be focused on by choosing the proper bias parameters during the DLTS test. However, special attention should be paid when it comes to the transient zone of DLTS signal [e.g. Figure 5.40(b)].

Chapter 6
Conclusion and prospective

6.1 Conclusion

This dissertation mainly studies the deep level defects and their influences on SiC power devices especially Schottky diodes. The main conclusions can be summarized in the following aspects.

- **Determination of SBH**

Based on the fundamental theory of Schottky contact, various of SBH models have been reviewed such as Gaussian distribution model, potential fluctuation model and flat-band barrier height. The Richardson plot based on Φ_{BF} is revealed to be suitable for determination of Richardson constant. The equivalence of Gaussian distribution model and potential fluctuation model has been discussed. Moreover, both parallel diode assumption and Tung's model on Schottky barrier inhomogeneity have been introduced.

- **Deep level detection**

Following an overview on defect classification, the detection of defect levels with DLTS has been mainly introduced according to basic capture-emission theory in semiconductor. Apart from different transient models in DLTS, the isothermal tests have been highlighted.

- **Investigation on SBDs and PiN diodes**

Both static and DLTS tests have been taken on SBDs and PiN diodes. The comparison on either single/multi barrier SBD or SBD with different metal contacts (Ti/W, W, Ni and Mo) have been presented along with the DLTS results. 9 trap levels are commonly found in SiC SBDs including the overlapped energy level such as $RD_{1/2}$. However, no obvious difference has been found related to either barrier inhomogeneity or contact metal. The hole traps have been investigate with PiN diodes under strong injection condition, and the interaction between electron traps and hole traps under different bias has been discussed.

- **Radiation effect and bias stress instability on power MOSFET**

The synergetic effects of HTGB and TID on SiC power MOSFETs have been investigated. It is found that V_{th} seems sensitive to both HTGB and TID, while the trend is opposite under separate tests (i.e. HTGB tend to increase V_{th} while V_{th} decreases after TID). This results from different types of charges captured in the gate oxide. Meanwhile, acceleration of V_{th} degradation due to HTGB was observed, which may result from the generated electric field due to captured electrons near interface after HTGB. However, No clear annealing effect was observed over the short period of test at room temperature for either HTGB or TID radiation.

- **Temperature related effects**

The carrier freeze-out has been revealed in both SiC SBD and PiN diodes. A negative-U behavior is suggested to show up at around 80 K. The annealing effect at high temperature is proved to take responsibility for the reduction on certain trap levels as well as direct impact on the direct I-V performance which leads to the double barrier phenomenon. On top of that, the DLTS behavior at extremely low temperature has been studied with isothermal test and the abnormal signal has been obtained, which indicates the existence of the trap level with tiny activation energy and large calculation.

6.2 Perspective

As one of the most attractive "after-silicon" materials for power application, the impact of SiC and related devices is becoming more and more important in the future thanks to the development of modern technology on SiC wafer fabrication and manufacturing process. Not only reliability but also the demand of precisely control of carrier lifetime in device has highlighted the significance of defect investigation, which is a large wasteland that has not yet been well investigated.

The future work mainly includes:

- **Interface characterization**

As illustrated in Tung's model (2.5.3), interface condition plays a significant role in forward characteristics. Therefore, it is possible to find links between abnormal forward I-V behavior and the interface states. Both investigations of interface traps and direct mapping of surface states by photos (e.g. Atomic Force Microscopy, AFM) as well as mapping current distribution during device operation should be powerful tools.

- **Improvement on trapping models at low temperature**

The model that suits the extremely low temperature involving the negative-U center should be well developed, especially the detailed capture / emission process along with the trap distribution.

- **Investigation of stress effect.**

As has been pointed out, high temperature annealing, bias stress and radiation can greatly affect the characteristic of device as well as the trap states. Further study can focus on the combination effect of bias stress at high temperature, which is often the case to many high temperature characterization methods.

- **Reverse characterization**

Even though the characteristics under reverse bias have not been well studied due to the precision limit of current measurement, the behavior under reverse bias is an important characteristic related to trap centers. It is also a complement to the forward characteristics study.

Reference

[1] R. H. Mari, "DLTS characterisation of defects in III-V compound semiconductors grown by MBE," University of Nottingham, 2011.

[2] J. Baliga, "Modern power devices," 1987.

[3] R. Brown, "A novel AlGaN/GaN based enhancement-mode high electron mobility transistor with sub-critical barrier thickness," PHD thesis of University of Glasgow, 2015.

[4] J. J. Berzelius, "Untersuchungen über die Flussspathsäure und deren merkwürdigsten Verbindungen," *Annalen der Physik,* vol. 77, pp. 169-230, 1824.

[5] D. Zhuang and J. H. Edgar, "Wet etching of GaN, AlN, and SiC: a review," *Materials Science and Engineering: R: Reports,* vol. 48, pp. 1-46, 2005.

[6] M. A. Mannan, "Defect Characterization of 4H-SIC by Deep Level Transient Spectroscopy (DLTS) and Influence of Defects on Device Performance," 2015.

[7] J. B. Casady and R. W. Johnson, "Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review," *Solid-State Electronics,* vol. 39, pp. 1409-1422, 1996.

[8] T. Tamaki, G. G.Walden, Y. Sui, and J. A. Cooper, "Optimization of on-State and Switching Performances for 15–20-kV 4H-SiC IGBTs," *IEEE TRANSACTIONS ON ELECTRON DEVICES,* vol. 55, pp. 1920-1927, 2008.

[9] L. Cheng, A. K. Agarwal, C. Capell, M. O'Loughlin, K. Lam, J. Richmond, *et al.*, "20 kV, 2 cm 2, 4H-SiC gate turn-off thyristors for advanced pulsed power applications," in *2013 19th IEEE Pulsed Power Conference (PPC)*, 2013, pp. 1-4.

[10] Itoh, Akira, Matsunami, and Hiroyuki, "Single crystal growth of SiC and electronic devices," *Critical Reviews in Solid State and Materials Sciences,* vol. 22, pp. 111-197, 1997.

[11] C.-M. Zetterling, "Silicon dioxide and aluminium nitride as gate dielectric for high temperature and high power silicon carbide MOSFETs," 1997.

[12] A. Elasser and T. P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," *Proceedings of the IEEE,* vol. 90, pp. 969-986, 2002.

[13] T. Kimoto and Ieee, "SiC Technologies for Future Energy Electronics," *2010 Symposium on Vlsi Technology, Digest of Technical Papers,* pp. 9-14, 2010.

[14] M. Ruff, H. Mitlehner, and R. Helbig, "Sic Devices: Physics and Numerical Simulation," *IEEE TRANSACTIONS ON ELECTRON DEVICES,* vol. 41, pp. 1040-1054, 1994.

[15] H. Yuan, X.-Y. Tang, Y.-M. Zhang, Y.-M. Zhang, Q.-W. Song, F. Yang, *et al.*, "4H-SiC Schottky barrier diodes with semi-insulating polycrystalline silicon field plate termination," *Chinese Physics B,* vol. 23, p. 057102, 2014.

[16] Q. Song, H. Yuan, C. Han, Y. Zhang, X. Tang, Y. Zhang, *et al.*, "Fabrication of a monolithic 4H-SiC junction barrier schottky diode with the capability of high current," *Science China Technological Sciences,* vol. 58, pp. 1369-1374, 2015.

[17] E. E. Tanrıkulu, D. E. Yıldız, A. Günen, and Ş. Altındal, "Frequency and voltage dependence of electric and dielectric properties of Au/TiO2/n-4H-SiC (metal-insulator-semiconductor) type Schottky barrier diodes," *Physica Scripta,* vol. 90, p. 095801, 2015.

[18] D. J. Ewing, Q. Wahab, R. R. Ciechonski, M. Syväjärvi, R. Yakimova, and L. M. Porter, "Inhomogeneous electrical characteristics in 4H-SiC Schottky diodes," *Semiconductor Science and Technology,* vol. 22, pp. 1287-1291, 2007.

[19] Ł. Gelczuk, P. Kamyczek, E. Płaczek-Popko, and M. Dąbrowska-Szata, "Correlation between barrier inhomogeneities of 4H-SiC 1A/600V Schottky rectifiers and deep-level defects revealed by DLTS and Laplace DLTS," *Solid-State Electronics,* vol. 99, pp. 1-6, 2014.

[20] J. P. Doyle, M. O. Aboelfotoh, B. G. Svensson, A. Schoner, and N. Nordell, "Characterization of electrically active deep level defects in 4H and 6H SiC," *Diamond and Related Materials,* vol. 6, pp. 1388-1391, Aug 1997.

[21] V. Afanasev, M. Bassler, G. Pensl, and M. Schulz, "Intrinsic SiC/SiO2 interface states," *physica status solidi (a),* vol. 162, pp. 321-337, 1997.

[22] Z. Q. Fang, B. Claflin, D. C. Look, and G. C. Farlow, "Effects of Electron Irradiation on Deep Centers in High-Purity Semi-Insulating 6H-SiC," *Journal of Electronic Materials,* vol. 36, pp. 307-311, 2007.

[23] A. Uddin, H. Mitsuhashi, and T. Uemoto, "Investigation of deep levels and residual impurities in sublimation-grown SiC substrates," *Japanese Journal of Applied Physics Part 2-Letters,* vol. 33, pp. L908-L911, Jul 1994.

[24] T. Kimoto, A. Itoh, H. Matsunami, S. Sridhara, L. L. Clemen, R. P. Devaty*, et al.*, "Nitrogen donors and deep levels in high-quality 4H–SiC epilayers grown by chemical vapor deposition," *Applied Physics Letters,* vol. 67, p. 2833, 1995.

[25] K. Danno, T. Kimoto, and H. Matsunami, "Midgap levels in both n- and p-type 4H–SiC epilayers investigated by deep level transient spectroscopy," *Applied Physics Letters,* vol. 86, p. 122104, 2005.

[26] W. Bollmann, "Formation Volume of Schottky Defects (Vacancies) in Inorganic and Organic Compounds and the Defect Formation Mechanism of Melting," *Crystal Research and Technology,* vol. 27, pp. 673-684, 1992.

[27] K. Harafuji and K. Kawamura, "Point defects induced by physical sputtering in wurtzite-type GaN crystal," *Japanese Journal of Applied Physics,* vol. 49, p. 011001, 2010.

[28] B. S. Rao and S. Sanyal, "Charge transfer effect on formation and binding energies of vancancy pairs in NaCl and KCl," *physica status solidi (b),* vol. 164, pp. 351-356, 1991.

[29] L. Storasta, J. Bergman, E. Janzén, A. Henry, and J. Lu, "Deep levels created by low energy electron irradiation in 4 H-SiC," *Journal of applied physics,* vol. 96, pp. 4909-4915, 2004.

[30] H. Itoh, A. Kawasuso, T. Ohshima, M. Yoshikawa, I. Nashiyama, S. Tanigawa*, et al.*, "Intrinsic defects in cubic silicon carbide," *physica status solidi (a),* vol. 162, pp. 173-198, 1997.

[31] S. Orlinski, J. Schmidt, E. Mokhov, and P. Baranov, "Silicon and carbon vacancies in neutron-irradiated SiC: A high-field electron paramagnetic resonance study," *Physical Review B,* vol. 67, p. 125207, 2003.

[32] S. J. Zinkle, "Effect of H and He irradiation on cavity formation and blistering in ceramics," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms,* vol. 286, pp. 4-19, 2012.

[33] A. Kawasuso, H. Itoh, S. Okada, and H. Okumura, "Annealing processes of vacancy-type defects in electron-irradiated and as-grown 6 H-SiC studied by positron lifetime spectroscopy," *Journal of applied physics,* vol. 80, pp. 5639-5645, 1996.

[34] A. Kawasuso, F. Redmann, R. Krause-Rehberg, P. Sperr, T. Frank, M. Weidner*, et al.*, "Annealing process of defects in epitaxial SiC induced by He and electron irradiation: Positron annihilation study," in *Materials Science Forum*, 2001, pp. 537-542.

[35] Z. Chen, M. Maekawa, A. Kawasuso, S. Sakai, and H. Naramoto, "Electron irradiation-induced defects in ZnO studied by positron annihilation," *Physica B: Condensed Matter,* vol. 376, pp. 722-725, 2006.

[36] S. Brunner, W. Puff, A. Balogh, and P. Mascher, "Induced defects in ZnS by electron and proton irradiation and defect-annealing behavior," *Physica B: Condensed Matter,* vol. 273, pp. 898-901, 1999.

[37] S. Dannefaer, P. Mascher, and D. Kerr, "Annealing studies of vacancies in proton irradiated silicon," *Journal of applied physics,* vol. 73, pp. 3740-3743, 1993.

[38] V. Volterra, "Sur l'équilibre des corps élastiques multiplement connexes," in *Annales scientifiques de l'École normale supérieure*, 1907, pp. 401-517.

[39] T. Figiels, "Electron Emission from Extended Defects : DLTS Signal in Case of Dislocation Traps," *phys. stat. sol. (a),* vol. 121, pp. 187-193, 1990.

[40] S. U. Omar, T. S. Sudarshan, TawhidA.Rana, H. Song, and M. V. S. Chandrashekhar, "Interface Trap-Induced Nonideality in As-Deposited Ni/4H-SiC Schottky Barrier Diode," *IEEE TRANSACTIONS ON ELECTRON DEVICES,* vol. 62, pp. 615-621, 2015.

[41] H. Kim, K. E. Kweon, C.-Y. Chou, J. G. Ekerdt, and G. S. Hwang, "On the nature and behavior of Li atoms in Si: a first principles study," *The Journal of Physical Chemistry C,* vol. 114, pp. 17942-17946, 2010.

[42] A. B. Anderson and S. Mehandru, "n-type dopants and conduction-band electrons in diamond: Cluster molecular-orbital theory," *Physical Review B,* vol. 48, p. 4423, 1993.

[43] J. Fairfield and B. Gokhale, "Gold as a recombination centre in silicon," *Solid-State Electronics,* vol. 8, pp. 685-691, 1965.

[44] A. Uddin and T. Uemoto, "TRAP CENTERS IN GERMANIUM-IMPLANTED AND IN AS-GROWN 6H-SIC," *Japanese Journal of Applied Physics Part 1-Regular Papers Short Notes & Review Papers,* vol. 34, pp. 3023-3029, Jun 1995.

[45] N. Achtziger, D. Forkel-Wirth, J. Grillenberger, T. Licht, and W. Witthuhn, "Identification of deep bandgap states in 4H- and 6H-SiC by radio-tracer DLTS and PAC-spectroscopy," *Nuclear Instruments & Methods in Physics Research Section B-Beam Interactions with Materials and Atoms,* vol. 136, pp. 756-762, Mar 1998.

[46] T. Dalibor, H. Trageser, G. Pensl, T. Kimoto, H. Matsunami, D. Nizhner*, et al.*, "Oxygen in silicon carbide: shallow donors and deep accepters,"

Materials Science and Engineering B-Solid State Materials for Advanced Technology, vol. 61-2, pp. 454-459, Jul 1999.

[47] O. Klettke, S. A. Reshanov, G. Pensl, Y. Shishkin, R. P. Devaty, and W. J. Choyke, "Electrical and optical properties of erbium-related centers in 6H silicon carbide," *Physica B-Condensed Matter,* vol. 308, pp. 687-690, Dec 2001.

[48] A. Castaldini, A. Cavallini, and L. Rigutti, "Assessment of the intrinsic nature of deep levelZ1/Z2by compensation effects in proton-irradiated 4H-SiC," *Semiconductor Science and Technology,* vol. 21, pp. 724-728, 2006.

[49] K. Kawahara, G. Alfieri, and T. Kimoto, "Detection and depth analyses of deep levels generated by ion implantation in n- and p-type 4H-SiC," *Journal of Applied Physics,* vol. 106, p. 013719, 2009.

[50] P. B. Klein, "Identification and carrier dynamics of the dominant lifetime limiting defect in n-4H-SiC epitaxial layers," *physica status solidi (a),* vol. 206, pp. 2257-2272, 2009.

[51] K. Kawahara, X. Thang Trinh, N. Tien Son, E. Janzén, J. Suda, and T. Kimoto, "Investigation on origin of Z[sub 1/2] center in SiC by deep level transient spectroscopy and electron paramagnetic resonance," *Applied Physics Letters,* vol. 102, p. 112106, 2013.

[52] K. Kawahara, X. Thang Trinh, N. Tien Son, E. Janzén, J. Suda, and T. Kimoto, "Quantitative comparison between Z1⁄2 center and carbon vacancy in 4H-SiC," *Journal of Applied Physics,* vol. 115, p. 143705, 2014.

[53] A. O. Evwaraye, S. R. Smith, M. Skowronski, and W. C. Mitchel, "Observation of surface defects in 6H-SiC wafers," *Journal of Applied Physics,* vol. 74, p. 5269, 1993.

[54] M. Gong, S. Fung, C. D. Beling, and Z. You, "Electron-irradiation-induced deep levels in n-type 6H–SiC," *Journal of Applied Physics,* vol. 85, p. 7604, 1999.

[55] S. Brotherton, "The width of the non-steady state transition region in deep level impurity measurements," *Solid-state electronics,* vol. 26, pp. 987-990, 1983.

[56] K. Danno and T. Kimoto, "Investigation of deep levels in n-type 4H-SiC epilayers irradiated with low-energy electrons," *Journal of Applied Physics,* vol. 100, p. 113728, 2006.

[57] N. Sghaier, A. Souifi, J. M. Bluet, and G. Guillot, "Correlation between direct characteristic deficiencies and deep levels in 6H-SiC Schottky diodes," *Materials Science & Engineering C-Biomimetic and Supramolecular Systems,* vol. 21, pp. 283-286, Sep 2002.

[58] N. Achtziger and W. Witthuhn, "Band gap states of Ti, V, and Cr in 4H–silicon carbide," *Applied Physics Letters,* vol. 71, p. 110, 1997.

[59] K. V. Nguyen and K. C. Mandal, "Ru-Induced Deep Levels in Ru/4H-SiC Epilayer Schottky Diodes by Deep Level Transient Spectroscopy," *ECS Journal of Solid State Science and Technology,* vol. 5, pp. P3078-P3081, 2015.

[60] A. Castaldini, A. Cavallini, L. Rigutti, F. Nava, S. Ferrero, and F. Giorgis, "Deep levels by proton and electron irradiation in 4H–SiC," *Journal of Applied Physics,* vol. 98, p. 053706, 2005.

[61] I. Thurzo, R. Beyer, and D. R. T. Zahn, "Experimental evidence for complementary spatial sensitivities of capacitance and charge deep-level transient spectroscopies," *Semiconductor Science and Technology,* vol. 15, pp. 378-385, Apr 2000.

[62] Z. Q. Fang, D. C. Look, A. Saxler, and W. C. Mitchel, "Characterization of deep centers in bulk n-type 4H-SiC," *Physica B-Condensed Matter,* vol. 308, pp. 706-709, Dec 2001.

[63] J. R. Jenny, J. Skowronski, W. C. Mitchel, H. M. Hobgood, R. C. Glass, G. Augustine*, et al.*, "Deep level transient spectroscopic and Hall effect investigation of the position of the vanadium acceptor level in 4H and 6H SiC," *Applied Physics Letters,* vol. 68, p. 1963, 1996.

[64] F. C. Beyer, C. G. Hemmingsson, S. Leone, Y. C. Lin, A. Gällström, A. Henry*, et al.*, "Deep levels in iron doped n- and p-type 4H-SiC," *Journal of Applied Physics,* vol. 110, p. 123701, 2011.

[65] J. Grillenberger, N. Achtziger, R. Sielemann, and W. Witthuhn, "Radiotracer identification of a Ta-related deep level in 4H–SiC," *Journal of Applied Physics,* vol. 88, p. 3260, 2000.

[66] D. Menichelli, M. Scaringella, F. Moscatelli, M. Bruzzi, and R. Nipoti, "Characterization of energy levels related to impurities in epitaxial 4H-SiC ion implanted p+n junctions," *Diamond and Related Materials,* vol. 16, pp. 6-11, 2007.

[67] S.-i. Nakamura, T. Kimoto, and H. Matsunami, "High-Sensitivity Analysis of Z1Center Concentration in 4H-SiC Grown by Horizontal Cold-Wall Chemical Vapor Deposition," *Japanese Journal of Applied Physics,* vol. 41, pp. 2987-2988, 2002.

[68] F. C. Beyer, C. Hemmingsson, H. Pedersen, A. Henry, J. Isoya, N. Morishita*, et al.*, "Defects in low-energy electron-irradiated n-type 4H-SiC," *Physica Scripta,* vol. T141, p. 014006, 2010.

[69] K. Fujihira, T. Kimoto, and H. Matsunami, "Growth and characterization of 4H–SiC in vertical hot-wall chemical vapor deposition," *Journal of Crystal Growth,* vol. 255, pp. 136-144, 2003.

[70] F. Nava, A. Castaldini, A. Cavallini, P. Errani, and V. Cindro, "Radiation detection properties of 4H-SiC Schottky diodes irradiated up to 10(16) n/cm(2) by 1 MeV neutrons," *Ieee Transactions on Nuclear Science,* vol. 53, pp. 2977-2982, Oct 2006.

[71] I. D. Booker, J. U. Hassan, L. Lilja, F. C. Beyer, R. Karhu, J. P. Bergman*, et al.*, "Carrier Lifetime Controlling DefectsZ1/2and RB1 in Standard and Chlorinated Chemistry Grown 4H-SiC," *Crystal Growth & Design,* vol. 14, pp. 4104-4110, 2014.

[72] J. Bardeen, "Surface states and rectification at a metal semi-conductor contact," *Physical Review,* vol. 71, p. 717, 1947.

[73] A. Cowley and S. Sze, "Surface states and barrier height of metal-semiconductor systems," *Journal of Applied Physics,* vol. 36, pp. 3212-3220, 1965.

[74] E. Rhoderick and R. Williams, "Metal-Semiconductor Contacts. 1988. Clarendon," *Oxford,* 1988.

[75] C. Wagner, "Theory of current rectifiers," *Phys. Z,* vol. 32, pp. 641-645, 1931.

[76] W. Schottky, "W. Schottky and E. Spenke, Wiss. Veroff. Siemens-Werke 18, 225 (1939)," *Wiss. Veroff. Siemens Werken,* vol. 18, p. 225, 1939.

[77] H. A. Bethe, *Theory of the boundary layer of crystal rectifiers* vol. 43-12. Cambridge, Mass., [Cambridge, Mass.]: Radiation Laboratory, Massachusetts Institute of Technology, 1942.

[78] G. Baccarani, "Current transport in Schottky-barrier diodes," *Journal of Applied Physics,* vol. 47, pp. 4122-4126, 1976.

[79] F. Berz, "The Bethe condition for thermionic emission near an absorbing boundary," *Solid-state electronics,* vol. 28, pp. 1007-1013, 1985.

[80] C. Crowell and S. Sze, "Current transport in metal-semiconductor barriers," *Solid-state electronics,* vol. 9, pp. 1035-1048, 1966.

[81] J. Shannon, "Thermionic-field emission through silicon Schottky barriers at room temperature," *Solid-State Electronics,* vol. 20, pp. 869-872, 1977.

[82] W. Shockley and W. Read Jr, "Statistics of the recombinations of holes and electrons," *Physical review,* vol. 87, p. 835, 1952.

[83] R. N. Hall, "Electron-hole recombination in germanium," *Physical review,* vol. 87, p. 387, 1952.

[84] S. Sze, C. Crowell, and D. Kahng, "Photoelectric determination of the image force dielectric constant for hot electrons in Schottky barriers," *Journal of Applied Physics,* vol. 35, pp. 2534-2536, 1964.

[85] C. Raynaud, "Caracterisations électriques de matériaux et composants en carbure de silicium," Lyon, INSA, 1995.

[86] S. Chand and J. Kumar, "Evidence for the double distribution of barrier heights in Schottky diodes from I - V - T measurements," *Semicond. Sci. Technol,* vol. 11, pp. 1203-1208, 1996.

[87] R. Hackam and P. Harrop, "Electrical properties of nickel-low-doped n-type gallium arsenide Schottky-barrier diodes," *IEEE Transactions on Electron Devices,* vol. 19, pp. 1231-1238, 1972.

[88] F. Padovani and G. Sumner, "Experimental Study of Gold-Gallium Arsenide Schottky Barriers," *Journal of Applied Physics,* vol. 36, pp. 3744-3747, 1965.

[89] Y. Song, R. Van Meirhaeghe, W. Laflere, and F. Cardon, "On the difference in apparent barrier height as obtained from capacitance-voltage and current-voltage-temperature measurements on Al/p-InP Schottky barriers," *Solid-State Electronics,* vol. 29, pp. 633-638, 1986.

[90] J. H. Werner and H. H. Güttler, "Barrier inhomogeneities at Schottky contacts," *Journal of Applied Physics,* vol. 69, pp. 1522-1533, 1991.

[91] L. Wagner, R. Young, and A. Sugerman, "A note on the correlation between the Schottky-diode barrier height and the ideality factor as determined from IV measurements," *IEEE electron device letters,* vol. 4, pp. 320-322, 1983.

[92] N. N. K. Reddy and V. R. Reddy, "Barrier characteristics of Pt/Ru Schottky contacts on n-type GaN based on I–V–T and C–V–T measurements," *Bulletin of Materials Science,* vol. 35, pp. 53-61, 2012.

[93] S. Chand and J. Kumar, "Current-voltage characteristics and barrier parameters of Pd2Si/p-Si (111) Schottky diodes in a wide temperature range," *Semiconductor science and technology,* vol. 10, p. 1680, 1995.

[94] A. Bhuiyan, A. Martinez, and D. Esteve, "A new Richardson plot for non-ideal schottky diodes," *Thin Solid Films,* vol. 161, pp. 93-100, 1988.

[95] B. Skromme, E. Luckowski, K. Moore, M. Bhatnagar, C. Weitzel, T. Gehoski*, et al.*, "Electrical characteristics of Schottky barriers on 4H-SiC: The effects of barrier height nonuniformity," *ELECTRONIC MATERIALS,* vol. 29, pp. 376-383, 2000.

[96] M. K. Hudait and S. B. Krupanidhi, "Effects of thin oxide in metal–semiconductor and metal–insulator–semiconductor epi-GaAs Schottky diodes," *Solid-State Electronics,* vol. 44, pp. 1089-1097, 2000.

[97] M. L. Bolen and M. A. Capano, "Defect Analysis of Barrier Height Inhomogeneity in Titanium 4H-SiC Schottky Barrier Diodes," *Journal of Electronic Materials,* vol. 38, pp. 574-580, 2009.

[98] D. Lee, C. Kim, H. Lee, S. Lee, H. Kang, H. Kim*, et al.*, "Improving the Barrier Height Uniformity of 4H–SiC Schottky Barrier Diodes by Nitric Oxide Post-Oxidation Annealing," *IEEE ELECTRON DEVICE LETTERS,* vol. 35, pp. 868-870, 2014.

[99] G. Brezeanu, G. Pristavu, F. Draghici, M. Badila, and R. Pascu, "Characterization technique for inhomogeneous 4H-SiC Schottky contacts: A practical model for high temperature behavior," *Journal of Applied Physics,* vol. 122, p. 084501, 2017.

[100] J. L. Freeouf, T. N. Jackson, S. E. Laux, and J. M. Woodall, "Effective barrier heights of mixed phase contacts: Size effects," *Applied Physics Letters,* vol. 40, pp. 634-636, 1982.

[101] R. T. Tung, "Electron transport at metal-semiconductor interfaces: General theory," *Physical Review B,* vol. 45, pp. 13509-13523, 1992.

[102] H. J. Im, Y. Ding, J. P. Pelz, and W. J. Choyke, "Nanometer-scale test of the Tung model of Schottky-barrier height inhomogeneity," *Physical Review B,* vol. 64, 2001.

[103] S. Tumakha, D. J. Ewing, L. M. Porter, Q. Wahab, X. Ma, T. S. Sudharshan*, et al.*, "Defect-driven inhomogeneities in Ni⁄4H–SiC Schottky barriers," *Applied Physics Letters,* vol. 87, p. 242106, 2005.

[104] D. Tomer, S. Rajput, L. J. Hudy, C. H. Li, and L. Li, "Inhomogeneity in barrier height at graphene/Si (GaAs) Schottky junctions," *Nanotechnology,* vol. 26, p. 215702, May 29 2015.

[105] M. Gülnahar and H. Efeoğlu, "Double barrier nature of Au/p-GaTe Schottky contact: Linearization of Richardson plot," *Solid-State Electronics,* vol. 53, pp. 972-978, 2009.

[106] A. N. Beştaş, S. Yazıcı, F. Aktaş, and B. Abay, "Double Gaussian distribution of barrier height for FeCrNiC alloy Schottky contacts on p-Si substrates," *Applied Surface Science,* vol. 318, pp. 280-284, 2014.

[107] A. Bobby, S. Verma, K. Asokan, P. M. Sarun, and B. K. Antony, "Phase transition induced double-Gaussian barrier height distribution in Schottky diode," *Physica B: Condensed Matter,* vol. 431, pp. 6-10, 2013.

[108] E. Omotoso, W. E. Meyer, F. D. Auret, A. T. Paradzah, and M. J. Legodi, "Electrical characterization of deep levels created by bombarding nitrogen-doped 4H-SiC with alpha-particle irradiation," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms,* vol. 371, pp. 312-316, 2016.

[109] V. Lauer, G. Bremond, A. Souifi, G. Guillot, K. Chourou, M. Anikin*, et al.*, "Electrical and optical characterisation of vanadium in 4H and 6H-SiC,"

Materials Science and Engineering B-Solid State Materials for Advanced Technology, vol. 61-2, pp. 248-252, Jul 1999.

[110] S. Loualiche, A. Nouailhat, and G. Guillot, "Study of E3 trap annealing in GaAs by DDLTS technique," *Solid State Communications,* vol. 44, pp. 41-45, 1982.

[111] H. Lefevre and M. Schulz, "Double correlation technique (DDLTS) for the analysis of deep level profiles in semiconductors," *Applied physics,* vol. 12, pp. 45-53, 1977.

[112] A. F. Basile, J. Rozen, J. R. Williams, L. C. Feldman, and P. M. Mooney, "Capacitance-voltage and deep-level-transient spectroscopy characterization of defects near SiO2/SiC interfaces," *Journal of Applied Physics,* vol. 109, p. 064514, 2011.

[113] D. V. Lang, "Deep-level transient spectroscopy: A new method to characterize traps in semiconductors," *Journal of Applied Physics,* vol. 45, pp. 3023-3032, 1974.

[114] S. Zachman, E. Finkman, and G. Bahir, "Adaptation of deep level transient spectroscopy for narrow bandgap semiconductor materials," *Semiconductor Science and Technology,* vol. 8, p. S90, 1993.

[115] O. Mitrofanov and M. Manfra, "Poole-Frenkel electron emission from the traps in AlGaN/GaN transistors," *Journal of Applied Physics,* vol. 95, pp. 6414-6419, 2004.

[116] M. Trushin and O. F. Vyvenko, "Impact of Electric Field on Thermoemission of Carriers from Shallow Dislocation-Related Electronic States," in *Solid State Phenomena*, 2014, pp. 299-304.

[117] G. Alfieri, E. V. Monakhov, and B. G. Svensson, "Evidence for a deep two charge state defect in high energy electron irradiated 4H-SiC," in *Materials Science Forum*, 2004, pp. 481-484.

[118] M. Kato, K. Yoshihara, M. Ichimura, T. Hatayama, and T. Ohshima, "Observation of deep levels and their hole capture behavior in p-type 4H-SiC epilayers with and without electron irradiation," *Japanese Journal of Applied Physics,* vol. 53, p. 04EP09, 2014.

[119] L. Dobaczewski, P. Kaczor, I. Hawkins, and A. Peaker, "Laplace transform deep-level transient spectroscopic studies of defects in semiconductors," *Journal of applied physics,* vol. 76, pp. 194-198, 1994.

[120] S. Weiss and R. Kassing, "Deep Level Transient Fourier Spectroscopy (DLTFS)—A technique for the analysis of deep level properties," *Solid-State Electronics,* vol. 31, pp. 1733-1742, 1988.

[121] A. Chantre, G. Vincent, and D. Bois, "Deep-level optical spectroscopy in GaAs," *Physical Review B,* vol. 23, p. 5335, 1981.

[122] E. Gaubas, D. Bajarūnas, T. Čeponis, D. Meškauskaitė, and J. Pavlov, "Optically induced current deep level spectroscopy of radiation defects in neutron irradiated Si pad detectors," *Lithuanian Journal of Physics,* vol. 53, 2013.

[123] K. Yoshihara, M. Kato, M. Ichimura, T. Hatayama, and T. Ohshima, "Deep levels in p-type 4H-SiC induced by low-energy electron irradiation," in *Materials Science Forum*, 2013, pp. 373-376.

[124] V. Polyakov, A. Rukovishnikov, N. Rossukanyi, V. Varnin, I. Teremetskaya, B. Druz*, et al.*, "Charge transient spectroscopy study of deep centers in

CVD diamond and diamond-like films," *MRS Online Proceedings Library Archive,* vol. 442, 1996.

[125] T. Okamoto, J. Long, R. H. Wilke, J. Stitt, R. Maier, and C. A. Randall, "A charge-based deep level transient spectroscopy measurement system and characterization of a ZnO-based varistor and a Fe-doped SrTiO3 dielectric," *Japanese Journal of Applied Physics,* vol. 55, p. 026601, 2016.

[126] L. Enriquez, S. Duenas, J. Barbolla, I. Izpura, and E. Muñoz, "Influence of refilling effects on deep-level transient spectroscopy measurements in Se-doped Al x Ga1− x As," *Journal of applied physics,* vol. 72, pp. 525-530, 1992.

[127] P. V. Kolev and M. Deen, "Constant Resistance DLTS in Submicron MOSFETs," in *Proceedings of the Fourth Symposium on Low Temperature Electronics and High Temperature Superconductivity*, 1997, p. 147.

[128] P. V. Kolev, M. J. Deen, J. Kierstead, and M. Citterio, "Constant-resistance deep-level transient spectroscopy in Si and Ge JFET's," *IEEE Transactions on Electron Devices,* vol. 46, pp. 204-213, 1999.

[129] C. M. Jackson, A. R. Arehart, E. Cinkilic, B. McSkimming, J. S. Speck, and S. A. Ringel, "Interface trap characterization of atomic layer deposition Al2O3/GaN metal-insulator-semiconductor capacitors using optically and thermally based deep level spectroscopies," *Journal of Applied Physics,* vol. 113, p. 204505, 2013.

[130] M. Bassler and G. Pensl, "Long-time constant-capacitance DLTS investigations of 6H SiC/MOS structures: comparison of dry and wet oxidation," *Materials Science and Engineering B,* vol. 61-62, pp. 490-492, 1990.

[131] C. Hemmingsson, N. T. Son, O. Kordina, E. Janzen, J. L. Lindstrom, S. Savage*, et al.*, "Capacitance transient studies of electron irradiated 4H-SiC," *Materials Science and Engineering B-Solid State Materials for Advanced Technology,* vol. 46, pp. 336-339, Apr 1997.

[132] D. V. Davydov, A. A. Lebedev, V. V. Kozlovski, N. S. Savkina, and A. M. Strel'chuk, "DLTS study of defects in 6H-and 4H-SiC created by proton irradiation," *Physica B-Condensed Matter,* vol. 308, pp. 641-644, Dec 2001.

[133] T. Dalibor, G. Pensl, T. Kimoto, H. Matsunami, S. Sridhara, R. P. Devaty*, et al.*, "Radiation-induced defect centers in 4H silicon carbide," *Diamond and Related Materials,* vol. 6, pp. 1333-1337, Aug 1997.

[134] E. Kalinina, G. Onushkin, D. Davidov, A. Hallen, A. Konstantinov, V. A. Skuratov*, et al.*, *Electrical study of 4H-SiC irradiated with swift heavy ions*, 2002.

[135] M. Kato, S. Tanaka, M. Ichimura, E. Arai, S. Nakamura, T. Kimoto*, et al.*, "Optical cross sections of deep levels in 4H-SiC," *Journal of Applied Physics,* vol. 100, p. 053708, 2006.

[136] E. Omotoso, W. E. Meyer, S. M. M. Coelho, M. Diale, P. N. M. Ngoepe, and F. D. Auret, "Electrical characterization of defects introduced during electron beam deposition of W Schottky contacts on n-type 4H-SiC," *Materials Science in Semiconductor Processing,* vol. 51, pp. 20-24, 2016.

[137] S. Mitra, M. V. Rao, K. Jones, N. Papanicolaou, and S. Wilson, "Deep levels in ion implanted field effect transistors on SiC," *Solid-State Electronics,* vol. 47, pp. 193-198, Feb 2003.

[138] S. Mitra, "Deep-level transient spectroscopy study on double implanted n[sup +]–p and p[sup +]–n 4H-SiC diodes," *Journal of Applied Physics,* vol. 95, p. 69, 2004.

[139] K. Danno and T. Kimoto, "High-Temperature Deep Level Transient Spectroscopy on As-Grown P-Type 4H-SiC Epilayers," *Japanese Journal of Applied Physics,* vol. 45, pp. L285-L287, 2006.

[140] R. Green, A. Lelis, and D. Habersat, "Application of reliability test standards to SiC Power MOSFETs," in *Reliability Physics Symposium (IRPS), 2011 IEEE International*, 2011, pp. EX. 2.1-EX. 2.9.

[141] R. Green, A. J. Lelis, and D. B. Habersat, "Charge trapping in SiC power MOSFETs and its consequences for robust reliability testing," in *Materials Science Forum*, 2012, pp. 1085-1088.

[142] E. Pomès, J.-M. Reynès, P. Tounsi, and J.-M. Dorkel, "Investigation of failure mechanisms in low-voltage power VDMOSFETs linked with gate oxide process quality," in *Microelectronics (MIEL), 2012 28th International Conference on*, 2012, pp. 251-254.

[143] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic mechanisms of threshold-voltage instability and implications for reliability testing of SiC MOSFETs," *IEEE Transactions on Electron Devices,* vol. 62, pp. 316-323, 2015.

[144] A. C. Ahyi, S. Wang, and J. R. Williams, "Gamma irradiation effects on 4H-SiC MOS capacitors and MOSFETs," in *Materials science forum*, 2006, pp. 1063-1066.

[145] S. K. Dixit, "Radiation-induced charge trapping studies of advanced Si and SiC based MOS devices," 2008.

[146] S. Dhombres, A. Michez, J. Boch, F. Saigne, S. Beauvivre, D. Kraehenbuehl*, et al.*, "Study of a Thermal Annealing Approach for Very High Total Dose Environments," *IEEE Transactions on Nuclear Science,* vol. 61, pp. 2923-2929, 2014.

[147] C. X. Zhang, E. X. Zhang, D. M. Fleetwood, R. D. Schrimpf, S. Dhar, S.-H. Ryu*, et al.*, "Effects of bias on the irradiation and annealing responses of 4H-SiC MOS devices," *IEEE Transactions on Nuclear Science,* vol. 58, pp. 2925-2929, 2011.

[148] T. Ohshima, S. Onoda, N. Iwamoto, T. Makino, M. Arai, and Y. Tanaka, "Radiation response of silicon carbide diodes and transistors," *Physics and Technology of Silicon Carbide Devices], Intech, Rijeka,* pp. 378-402, 2013.

[149] L. Yang and A. Castellazzi, "High temperature gate-bias and reverse-bias tests on SiC MOSFETs," *Microelectronics Reliability,* vol. 53, pp. 1771-1773, 2013.

[150] A. J. Lelis, D. Habersat, R. Green, A. Ogunniyi, M. Gurfinkel, J. Suehle*, et al.*, "Time dependence of bias-stress-induced SiC MOSFET threshold-voltage instability measurements," *IEEE Transactions on Electron Devices,* vol. 55, pp. 1835-1840, 2008.

[151] A. Akturk, J. McGarrity, S. Potbhare, and N. Goldsman, "Radiation effects in commercial 1200 V 24 a silicon carbide power MOSFETs," *IEEE Transactions on Nuclear Science,* vol. 59, pp. 3258-3264, 2012.

[152] I. S. Esqueda, H. J. Barnaby, and M. P. King, "Compact modeling of total ionizing dose and aging effects in MOS technologies," *IEEE Transactions on Nuclear Science,* vol. 62, pp. 1501-1515, 2015.

[153] E. Vianello, F. Driussi, D. Esseni, L. Selmi, M. Van Duuren, and F. Widdershoven, "Does multi-trap assisted tunneling explain the oxide thickness dependence of the statistics of SILC in FLASH memory arrays?," in *2006 European Solid-State Device Research Conference*, 2006, pp. 403-406.

[154] M. Gurfinkel, H. D. Xiong, K. P. Cheung, J. S. Suehle, J. B. Bernstein, Y. Shapira*, et al.*, "Characterization of transient gate oxide trapping in SiC MOSFETs using fast I-V techniques," *IEEE Transactions on Electron Devices,* vol. 55, pp. 2004-2012, 2008.

[155] T. Chen, Z. Luo, J. D. Cressler, T. F. Isaacs-Smith, J. R. Williams, G. Chung*, et al.*, "The effects of NO passivation on the radiation response of SiO2/4H-SiC MOS capacitors," *Solid-State Electronics,* vol. 46, pp. 2231-2235, 2002.

[156] Y. Xu, J. Bi, G. Xu, K. Xi, B. Li, and M. Liu, "Total ionizing dose effects and annealing behaviors of HfO 2-based MOS capacitor," *Science China Information Sciences,* vol. 60, p. 120401, 2017.

[157] C. Raynaud and G. Guillot, "Dopant level freeze-out in 6H-SiC Schottky diodes and junctions," in *Semiconducting and Semi-Insulating Materials Conference, 1996. IEEE*, 1996, pp. 227-230.

[158] T. Takase, M. Sakaino, Y. Sun, and T. Miyasato, "Measurement of Ionization Energies of Nitrogen in 4H-SiC by Traveling-Wave Method," *Japanese Journal of Applied Physics,* vol. 52, p. 091301, 2013.

[159] A. V. Los and M. S. Mazzola, "Influence of carrier freeze-out on SiC Schottky junction admittance," *Journal of electronic materials,* vol. 30, pp. 235-241, 2001.

[160] H. Yoshioka, T. Nakamura, and T. Kimoto, "Generation of very fast states by nitridation of the SiO2/SiC interface," *Journal of Applied Physics,* vol. 112, p. 024520, 2012.

[161] G. Watkins, "Negative-U properties for point defects in silicon," *MRS Online Proceedings Library Archive,* vol. 2, 1980.

[162] C. Hemmingsson, N. Son, A. Ellison, J. Zhang, and E. Janzén, "Negative-U centers in 4H silicon carbide," *Physical Review B,* vol. 58, p. R10119, 1998.

[163] C. Hemmingsson, N. Son, and E. Janzén, "Observation of negative-U centers in 6H silicon carbide," *Applied physics letters,* vol. 74, pp. 839-841, 1999.

[164] M. Weidner, G. Pensl, H. Nagasawa, A. Schöner, and T. Ohshima, "Negative-U-centers in 4H-and 6H-SiC detected by spectral light excitation," in *Materials Science Forum*, 2004, pp. 485-488.

[165] J. Furthmüller, A. Zywietz, and F. Bechstedt, "Monovacancies in 3C and 4H SiC," *Materials Science and Engineering: B,* vol. 61, pp. 244-247, 1999.

[166] A. Zywietz, J. Furthmüller, and F. Bechstedt, "Vacancies in SiC: Influence of Jahn-Teller distortions, spin effects, and crystal structure," *Physical Review B,* vol. 59, p. 15166, 1999.

[167] L. Dobaczewski and P. Kaczor, "Ionization and capture kinetics of DX centres in AlGaAs and GaSb: approach for a negative-U defect," *Semiconductor Science and Technology,* vol. 6, p. B51, 1991.

FOLIO ADMINISTRATIF

THESE DE L'UNIVERSITE DE LYON OPEREE AU SEIN DE L'INSA LYON

NOM : ZHANG DATE de SOUTENANCE : 13/12/2018

Prénoms : Teng

TITRE : Caractérisations des défauts profonds du SiC et pour l'optimisation des performances des composants haute tension

NATURE : Doctorat Numéro d'ordre : 2018LYSEI108

Ecole doctorale : Électronique, Électrotechnique, Automatique

Spécialité : Génie Électrique

RESUME : Il est important de caractériser les défauts des semi-conducteurs et d'évaluer leur influence sur les dispositifs de puissance. De plus, la fiabilité, qui est également affectée par les défauts, devient une question incontournable dans le domaine de l'électricité de puissance. Les défauts, que ce soit des défauts ponctuels ou des défauts étendus, peuvent introduire des niveaux d'énergie supplémentaires dans la bande interdite du SiC. En tant que méthode de caractérisation des défauts largement utilisée. La spectroscopie des transitoires de capacité ou de courant (DLTS) est une méthode de caractérisation des défauts Le tracé de Richardson basé sur Hauteur de barrière en bandes plates ainsi que le modèle de fluctuation potentielle deviennent un outil puissant pour la caractérisation HBS. Les HBSs avec différents contacts métalliques ont été caractérisées, et les diodes à barrières multiples sont vérifiées par différents modèles. 9 pièges à électrons et 4 pièges à trous ont été trouvés dans nos échantillons SiC-4H. Une relation linéaire entre l'énergies d'activation extrait et le log(sigma) indique l'existence de la température intrinsèque de chaque défaut. Cependant, aucune différence évidente n'a été constatée en ce qui concerne l'inhomogénéité de la barrière ou le métal de contact. De plus, les pièges à électrons près de la surface et les charges fixes positives dans la couche d'oxyde ont été étudiés sur des MOSFET de puissance SiC par des stress HTGB (tension de grille constante à haute température) et dose ionisante totale (TID) provoquées par irradiation. Un modèle HTGB-assisté par-TID a été établi afin d'expliquer la synergie entre ces deux effets.D'autres effets tels que le gel du support, le recuit à haute température et le comportement U-négatif ont également été discutés. Une attention particulière a été portée aux défauts à faible énergie d'activation à très basse température.

MOTS-CLÉS : Défaut, HBS, SiC-4H, inhomogénéité du contact, DLTS, HTGB, TID, Fiabilité

Laboratoire (s) de recherche : AMPÈRE, UMR CNRS 5005

Directeur de thèse: Dominique PLANSON, AMPERE, INSA de Lyon

Président de jury : J. TARTARIN

Composition du jury :

M.	J. TARTARIN	Professeur, LAAS	M.	J. BI	Professeur, UCAS
Mme.	M. LOCATELLI	Chargée de Recherche, LAPLACE	Mme.	S. UILLAGUET	Maître de Conférences, L2C
M.	D. PLANSON	Professeur, INSA de Lyon	M.	C. RAYNAUD	Maître de Conférences, INSA de Lyon