Design and optimization of power-clock generator and distribution network for adiabatic logic

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Conception et optimisation d'une alimentation-horloge et d'un réseau de distribution pour la logique adiabatique.

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A ma famille et mes amis,
Qui m'ont soutenu tout au long de ce voyage,

"Ce n'est pas assez d'avoir l'esprit bon, mais le principal est de l'appliquer bien."

René Descartes

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Résumé

La densité de puissance est devenue l'une des principales préoccupations lors de la conception d'un système numérique. Comme pour tous les systèmes embarqués, chaque nouvelle génération de système numérique a plus d'applications que la précédente et exige en fin de compte une plus grande densité de puissance. C'est pourquoi de nombreux chercheurs et de concepteurs industriels se sont penchés sur de nouvelles méthodes de réduction de la consommation électrique des circuits numériques.

De plus, du point de vue de la consommation énergétique, avec l'augmentation du nombre d'objets connectés, de centres de données et de dispositifs de communication, ces appareils électroniques pourront représenter jusqu'à 51% de la demande énergétique mondiale en 2030. Pour limiter l'augmentation de la consommation énergétique, il y a trois axes de recherches : développer de nouveaux composants, développer de nouvelles techniques de conception au niveau des portes, des circuits et des systèmes ainsi que développer de nouvelles architectures.

Cette thèse se concentre sur un style de conception de portes alternatif, la logique adiabatique. Cette logique peut réduire la consommation d'énergie dynamique [1]. La plupart de la consommation d'énergie dans les circuits numériques provient des dissipations dynamiques, cette dissipation vient de la façon dont sont alimentées les portes numériques. L'énergie nécessaire pour charger les portes numériques conventionnelles sont dissipées deux fois, à la charge, la même quantité d'énergie stockée dans la capacité équivalente est dissipée dans la porte et ensuite à la décharge où l'énergie est dissipée à la masse. L'essence de la logique adiabatique est de charger la porte logique avec une rampe puis de la décharger vers l'alimentation. Pour économiser de l'énergie, la charge et la décharge doivent être effectuées à la fréquence la plus basse possible. Même si le principe adiabatique est connu depuis les années 70, le compromis entre la consommation énergétique

et la fréquence n'était pas particulièrement intéressant. Avec l'émergence de nouveaux transistors comme les transistors à effet de champ à base de nanotubes de carbone, CNTFET, les interrupteurs nano-électro-mécaniques, NEMS, ou encore les transistors à effet de champ à fente verticale, VeSFET, les recherches sur la logique ont gagné un nouvel intérêt.

L'une des particularités de la logique adiabatique est que l'alimentation sert également d'horloge et est appelée alimentation-horloge. Le premier objectif de cette thèse est d'étudier comment générer le signal d'alimentation-horloge, puis de proposer une topologie d'alimentation-horloge afin de maximiser le rendement énergétique d'un circuit adiabatique.

En conception intégrée, un des problèmes concerne l'intégrité des signaux d'alimentation et d'horloge. Les problèmes potentiels d'intégrité proviennent des parasites du réseau de distribution d'énergie et celui de distribution d'horloge. Pour les circuits adiabatiques, le réseau de distribution d'énergie et celui de distribution d'horloge sont combinés dans un réseau de distribution d'alimentation-horloge. Le second objectif de cette thèse est d'étudier l'impact du réseau de distribution sur le rendement énergétique du circuit adiabatique puis de proposer une optimisation de ce même réseau de distribution.

Cette thèse a été financée par l'ANR, avec le projet ADIANEMS2 (numéro de subvention : ANR-15-CE24-0013). Ce projet est une collaboration entre l'ESIEE, le CEA-LETI et le LIRMM. Les objectifs du projet sont d'évaluer les économies d'énergie potentielles d'un circuit adiabatique à l'aide de nanosystèmes électromécaniques, NEMS. L'objectif du LIRMM est de développer une alimentation-horloge et son réseau de distribution. La recherche de l'ESIEE se porte sur la conception de nouveaux NEMS pour leur utilisation dans la conception de portes logiques adiabatiques. Le rôle du CEA-LETI est de concevoir de nouvelles portes logique en utilisant ces NEMS.

Cette thèse est divisée en 7 chapitres. Elle comporte une introduction et une conclusion et 5 chapitres sur le travail de thèse. Nous allons résumer l'ensemble des contributions de cette thèse chapitre par chapitre.

Le **chapitre 2** présente l'état de l'art de la logique adiabatique ainsi que les problèmes rencontrés par l'utilisation des portes logiques adiabatiques conçues avec des transistors CMOS. La dissipation d'énergie d'une porte logique adiabatique est la somme de trois dissipations : la dissipation adiabatique, la dissipation due aux fuites et celle due à la tension de seuil. La dissipation adiabatique est proportionnelle à la fréquence, tandis que la dissipation due aux fuites est inversement proportionnelle à celle-ci. Il existe donc une fréquence optimale pour limiter ces deux dissipations. La dissipation due à la tension de seuil est une dissipation indépendante de la fréquence, qui provient de la décharge incomplète des portes logiques dans l'alimentation-horloge.

Grâce à l'état de l'art, nous sélectionnons la logique adiabatique PFAL, pour réaliser notre étude sur l'alimentation-horloge et son réseau de distribution. Nous optimisons la dissi-

pation d'énergie d'une porte logique PFAL avec les paramètres suivants : le nœud technologique CMOS, la tension de seuil et la tension d'alimentation. Grace à cette optimisation, nous sélectionnons des transistors CMOS Low-V_{TH} 45nm pour concevoir un tampon PFAL, qui dissipe idéalement $13aJ$ par cycle à une fréquence optimale de $5MHz$.

Le **chapitre 3** présente le réseau de distribution d'alimentation-horloge, PCN, qui est simultanément le réseau de distribution d'énergie et le réseau de distribution d'horloge. Un état de l'art sur ces réseaux pointe les problèmes qu'un PCN peut avoir : le retard du signal de l'horloge, la chute de tension IR et la sensibilité aux bruits du signal d'alimentation-horloge.

Nous avons divisé l'étude du PCN en deux étapes : nous étudions son impact sur une porte unique, puis sur de multiples portes.

Grâce à l'étude du PCN sur une seule porte, nous modélisons la dissipation d'énergie de la porte par rapport à sa propre résistance et capacité, à la résistance du PCN et à la fréquence de fonctionnement. Afin de montrer l'impact du PCN, nous introduisons trois contraintes sur la résistance du PCN : R_5, R_{999} et R_{CRIT}. R_5 limite la dissipation d'énergie supplémentaire maximum due au PCN à 5% de la dissipation d'énergie d'une porte idéale. R_{999} est la valeur maximale de la résistance du PCN, où la porte logique est complètement chargée à la fin de la phase de maintien. Enfin, R_{CRIT} est la valeur maximale de la résistance du PCN, où la porte adiabatique dissipe moins d'énergie qu'une porte classique idéale. Cette étude nous permet de nous assurer que la dissipation adiabatique peut être exprimée comme ci-après : $E_{AL} = 2\frac{RC}{T}CV_{DD}^2$ où la résistance est la somme des résistances de la porte et du PCN.

L'étude de l'impact du PCN sur de multiples portes nous a permis d'établir des lignes directrices pour concevoir et dimensionner le PCN afin d'optimiser la dissipation énergétique. À partir de cette étude, nous obtenons la valeur maximale de la résistance et de la capacité du PCN en prenant en compte la fréquence de fonctionnement, le nombre de portes et à la dissipation d'énergie supplémentaire tolérable. Avec ce guide de conception, nous proposons de dimensionner le PCN afin d'avoir des valeurs de résistance et de capacité parasites inférieures aux valeurs maximales que nous avons obtenues.

Le **chapitre 4** présente l'étude des alimentations-horloges. L'alimentation-horloge génère un signal à 4 phases. L'état de l'art sur ces alimentations nous indique qu'il y a deux familles d'alimentation-horloge : celles à base de capacités ou celles résonantes. Nous avons choisi d'étudier les alimentations résonantes.

Nous étudions des topologies pour l'alimentation-horloge dans deux cas différents. Dans le premier cas, l'alimentation-horloge doit alimenter un pipeline composé de tampons PFAL en CMOS 45nm, avec une tension d'alimentation de 0.5V et une fréquence de fonctionnement de $5MHz$. Dans le second cas l'alimentation-horloge doit alimenter un

pipeline composé de tampons PFAL en CMOS 65nm, avec une tension d'alimentation de 1,2V et une fréquence de fonctionnement de 2,5MHz.

Nous proposons une nouvelle topologie d'alimentation-horloge à base d'inductance. La nouveauté réside dans la synchronisation de chaque alimentation-horloge. Nous optimisons cette topologie afin de minimiser la dissipation d'énergie.

Dans le premier cas, le résultat est qu'un pipeline CMOS 45 nm composé d'un tampon PFAL dissipe 167aJ par cycle à 5MHz, soit 2,9 fois moins qu'un pipeline composé d'un tampon conventionnel en CMOS 45 nm. Toutefois, à la fin de la phase d'évaluation, la charge directe de la porte est plus importante que prévu, ce qui nuit à le rendement énergétique.

Pour comprendre pourquoi la dissipation énergétique est plus importante que prévue, nous étudions les différences entre notre modèle et les simulations. Le résultat de cette étude est que la résistance de la porte ne peut pas être modélisée comme une résistance à valeur constante lorsque la tension d'alimentation n'est pas à sa valeur nominale.

C'est pourquoi nous étudions le second cas. Après optimisation, un pipeline composé d'un tampon PFAL en CMOS 65nm dissipe 433aJ par cycle à 2,5MHz, soit 3,23 fois moins que le pipeline composé d'un tampon conventionnel en CMOS 65 nm.

Le **chapitre 5** présente la réalisation d'un circuit adiabatique, conçu en CMOS 65nm. Il est composé d'un pipeline PFAL et de 4 alimentations- horloges ainsi que leurs contrôles associés. Le circuit est prêt à être envoyé en fabrication.

Afin d'évaluer la dissipation d'énergie, nous extrayons les résistances et capacités parasites du PCN puis nous avons créé un modèle pour inclure les dissipations du pipeline, du PCN et des alimentations-horloges. Il en résulte que le circuit, composé d'un pipeline de 123952 portes, de 4 réseaux de distribution et de 4 alimentations-horloges et leurs contrôles associés, dissipe 59,2pJ par cycle. Le pipeline représente 33,8% de la dissipation d'énergie, les alimentations-horloges représentent 57,9% et les réseaux de distribution représentent 8,3%. Le pipeline, dont la tension d'alimentation est de 1.2V et dont la fréquence d'opération est de 2,5MHz, dissipe 3 fois moins d'énergie qu'un pipeline classique idéal.

Le **chapitre 6** présente une prometteuse famille de logique adiabatique: Le CNTFET PFAL. Nous remplaçons les transistors CMOS par des transistors à base de nanotubes de carbone, les CNTFETs. Pour évaluer les performances de la logique CNTFET PFAL, nous utilisons le modèle de CNTFET développé à Stanford. Nous optimisons les paramètres afin de minimiser la dissipation d'énergie.

Ensuite, nous comparons le tampon CNTFET PFAL avec un tampon PFAL en CMOS 45nm. Les résultats de cette comparaison sont les suivants : 1) Le tampon CNTFET PFAL a un plus grand courant de fuite, donc le tampon PFAL en CMOS 45nm a un meilleur rendement

énergétique pour les fréquences les plus basses, à savoir $f \geq 18\text{MH}z$. 2) En diminuant la tension d'alimentation, le tampon CNTFET PFAL a une plus faible dissipation énergétique.

Avec une tension d'alimentation nominale, à savoir V_{DD} = 1V, la fréquence de fonctionnement maximale du PFAL CNTFET est de $2,5\text{GH}z$. A la fréquence optimale $f = 400\text{MH}z$, le tampon CNTFET PFAL dissipe $20,8aJ$. Afin d'évaluer les performances de cette logique adiabatique, nous introduisons la figure de mérite du produit du délai et de l'énergie, l'EDP: EDP = $T.E_{DISS}$. Grâce à l'EDP, nous montrons qu'un tampon CNTFET PFAL alimenté par une tension d'alimentation de 1V a une performance 273 fois plus élevée qu'un tampon PFAL en CMOS 45nm.

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CHAPTER

1 Introduction

1.1 Energy Efficiency in Integrated Circuits

1.1.1 Historical Contest

Power density has become the primary concern when a digital system is designed. As in any embedded systems, each new digital system generation has more applications than the previous one and ultimately demands more power density. This is why many researchers and industrial designers have been looking into novel methods for reducing power consumption of digital circuit.

Moreover, in an energy consumption point of view, with the increase numbers of Internet of Things, IoT, which are electronics devices with wireless communication, data centers and communication devices, they can represent up to 51% of the global energy demand in 2030 [2]. Fig. 1.1 shows the prediction of the electrical footprint in TWh of communication devices from 2010 to 2030. They are three scenarios: 1) the worst case scenario where the use of communication devices is increased and their energy efficiency stay the same, 2) the expected case scenario, where the increase of the communication devices is counterbalanced with a better energy efficiency and 3) the best case scenario, where there are less usage of communication devices and a better energy efficiency.

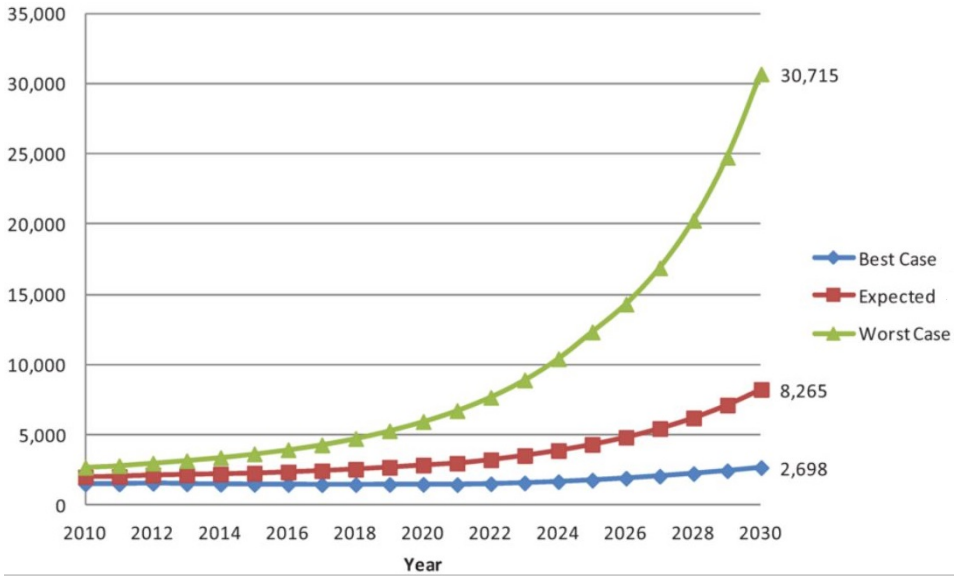

Figure 1.1 – Electricity footprint (TWh) of communication devices 2010-2030, source: [2].

In 2030, the expected case energy consumption of communication devices is 3.7 times lower than the worst case energy consumption. A parameter of the energy consumption increase is that more and more communication devices will be used. The other parameter is that communication devices have more applications and denser functional block, which lead to a higher energy consumption. The integration of the functional block follows Moore's law. In 1965, Moore has predicted that the number of transistors per mm^2 will doubled every two years [7].

From 1970 to the early 2000's, doubling the number of transistor has been made by shrinking the dimensions of CMOS by a factor of 0.7. This is the first era of transistor scaling, which is known as the geometrical scaling. The scaling of CMOS leads to a lower supply voltage, which leads to a lower energy dissipation per operation. However, it also leads to a higher integration and a higher operating frequency, which increase the overall power consumption [8].

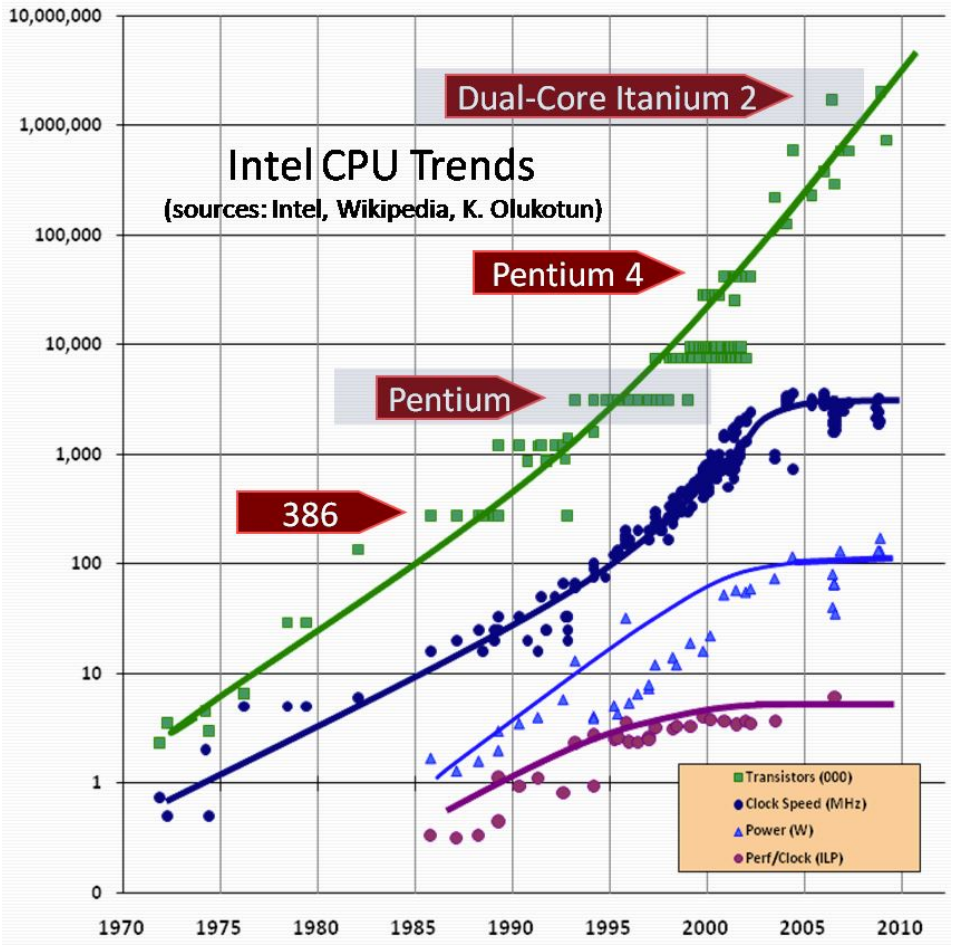

Figure 1.2 – Evolution of the Intel CPU from 1970 to 2010, source: [3].

In Fig.1.2, characteristics, such as the number of transistors, the operating frequency, the power consumption and the performance, of Intel CPU are shown in a time-line. Since the early 2000's, the operating frequency has been capped in order to limit the power consumption. The main blocking factor in the increase of the transistor integration is to be able to dissipate the heat coming from the energy dissipation. Heat cooling is mostly done using heat sinks, which have a fixed heat cooling density. Thus, in order to limit the circuit power dissipation density, the frequency has been capped: this is the operating frequency wall [3]. In order to continue the integration, researchers have focused their research in finding new materials to limit the transistor energy dissipation, such as high-k dielectric [9] or strained silicon [10]. These new materials reduce the effective CMOS dimension, which leads to a second era of transistor scaling: the effective scaling.

The operating frequency wall has also an impact on the performance of digital circuits. As

it is shown in Fig.1.2, the figure of merit of the performance, which is the power divided by the frequency, has been constant since the operating frequency was capped. In order to improve the value of such devices, the community has proposed two research axis: 1) to continue the transistor scaling 'More Moore' and 2) the diversification of functional blocks 'More than Moore'. In Fig.1.3, the representation of the miniaturization of digital circuit is shown with respect to the miniaturization of transistors and the diversification of the functionalities. In order to increase the value of digital systems 'More than Moore', researchers have developed system in package with non-digital functions, such as power management, sensing or communications [4].

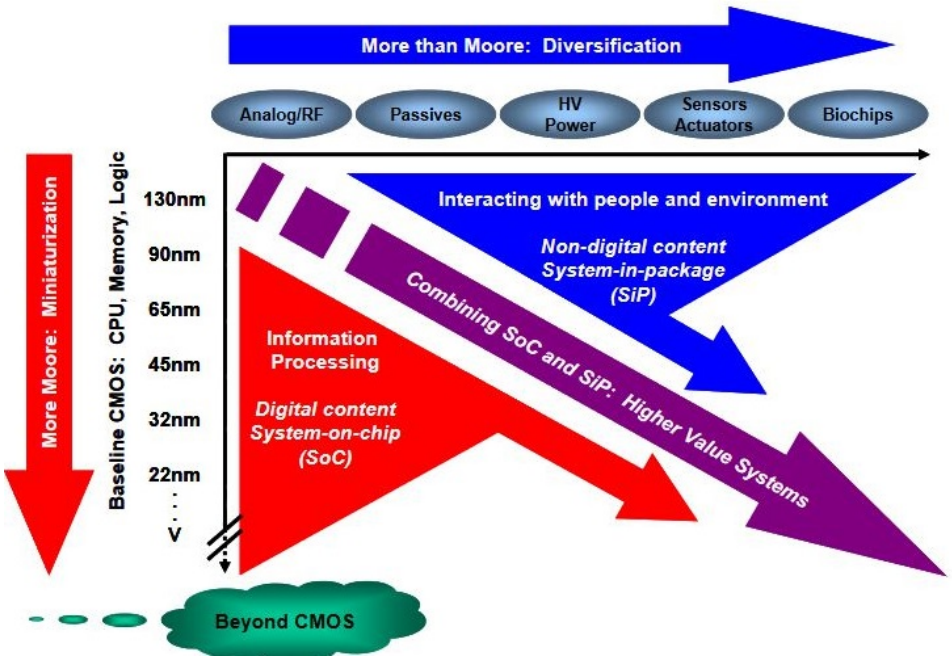

Figure 1.3 – Representation of the miniaturization of the digital functions ("More Moore") and the functional diversification ("More than Moore"), source: [4]

The CMOS miniaturization has been slowed down due to the difficulty of decreasing the length of the CMOS gate for a length lower than $28nm$. This difficulty comes from the dielectric. In order to create conduction in the channel, the gate should have a minimal capacitance, which is impacted by the dielectric permittivity, ϵ, surface, S and thickness, t. The capacitance is expressed as follows:

$$C = \epsilon \frac{S}{t} \tag{1.1}$$

The permittivity depends on the dielectric, the surface is proportional to the CMOS node and the thickness has a minimal value in order to isolate the gate capacitor. Thus, with the scaling, the decrease of the surface leads to a lower capacitance value. Hence, the channel is harder to control for lower CMOS nodes. In order to continue the miniaturization of transistors, researchers have to develop new switching devices, which are known as beyond CMOS devices.

1.1.2 End of Moore's law and research on the energy efficiency

With the emergence of beyond CMOS devices, Moore's law has been officially ended [11]. In order to continue to increase the density of transistors in digital circuits, scientists have focus their research in four main areas: the development of beyond CMOS transistors, the diversification of functionalities, the monolithic 3D integration [12] and the development of new memories [13]. The goal is to scale one trillion of transistors by 2025 [14]. This is the third era of transistor integration: the hyper scaling. In order to improve the performance of such circuits, the energy dissipation has to be taken care of. Otherwise, the frequency will be reduced similarly to the operating frequency wall. There are 3 research axis to reduce the energy dissipation: novel technologies and devices, new devices-, circuit- and system-level design and new architecture design style.

Beyond CMOS transistors

On novel technologies and devices level, research is axed on proposing new energy efficient devices such as switches like the evolution of CMOS, Carbon Nanotubes Field Effect Transistor, CNTFET, Vertical Slit Field Effect Transistor, VeSFET or Micro Electro Mechanical Switches, MEMS, as memories like Static Random Access Memory, SRAM. Another axis of research is the study of more energy efficient interconnections.

Following Moore's law, bulk CMOS faces two main issues: leakage current has increased with the CMOS scaling and the gate capacitance (Eq.(1.1) is too low to control efficiently the channel known as Short Channel Effect, SCE [15]. In order to face these issues, there are two main research axes: Fully Depleted Silicon On Insulator, FDSOI and Fin Field Effect Transistor, FinFET. FDSOI is a MOSFET, which has an additional buried oxide instead of a bulk. This oxide can be polarized. This polarization is referred as the body-biasing. Thanks to this additional oxide, the capacitance, which controls the channel has a higher value. It results with a lower SCE. The second advantage of the additional oxide is the reduction of leakage [16]. The aim of FinFET is to control the channel with a 3 dimensional gate. This way, it increases the facing surface of the gate oxide and the channel, which leads to a higher gate capacitance, thus, less SCE [17]. There are two types of FinFet: bulk FinFet [18] and SOI FinFET [19].

Carbon Nanotubes Field Effect Transistor, CNTFET is a promising replacement for CMOS

as CNTFET does not have SCE [20]. The aim of CNTFET is to replace the doped silicon channel by Carbon Nanotubes, CNT [6]. Thus, the control of the channel resistance is easier. Another improvement of the CNTFET is that, unlike CMOS, most of the electrons are carried thanks to the ballistic transport. Ballistic transport reduces the scattering, thus the channel is less resistive and CNTFET-based logic can achieve a better performance [21].

Vertical Slit Field Effect Transistor, VeSFET is a 4 terminal FET. The novelty on this transistor is that the channel is grown vertically and it is controlled by two independent gates [22]. Thanks to the two capacitances, leakage current is reduced. Due to the 4 terminals, scientists have designed novel gates, such as AND and OR functions using a single VeSFET [23].

Micro-Electro-Mechanical Switch, MEMS is a mechanical switch. Thus, the leakage current is drastically reduced. However, the performance of the switching is based on the mechanical cutting frequency of MEMS [24]. Thus, MEMS performances are lower than the performances of Field Effect Transistors, FET. Similarly to CMOS, MEMS benefits from the scaling, researchers have developed Nano-Electro-Mechanical Switch, NEMS, which have better performances than MEMS [25]. Another research axis is to develop NEMS as high ratio capacitance switch. Such devices are used in radio frequency applications or for capacitive-based logic [26].

Energy Efficient Memories

The data storage can represent up to 50% of the whole energy dissipation in electronics devices. Scientists have focused their research on reducing this energy dissipation, especially the leakage dissipation. There are two types of random access memory, the Dynamic Random Access Memory and the Static Random Access Memory, SRAM. The difference between the two memory types is that DRAM needs to refresh the stored data periodically. Thus, in an energy efficiency point of view, SRAM is a better solution. However, SRAM needs more transistors in order to store one bit of data as the two SRAM cells are composed with 6 or 8 transistors [27]. SRAM benefits from the emergence of new technologies devices as researchers have developed SRAM using CNTFET [28] or FDSOI [29].

Energy Efficient Interconnect

Interconnect has become a main concern in high performance and low energy applications. Interconnect lowers the energy efficiency and increases the signal delay. Historically interconnects are made with copper [30]. With the CMOS scaling and the emergence of others FET technologies, scientist have focused their effort on improving the interconnects. There are two research axes: CNT based interconnects and optical interconnects. CNT based interconnects replace copper wire by carbon nanotube [31] while optical interconnects uses light signals instead of electrical ones [32].

Energy Efficient Architecture Styles

On architecture design style, the research focuses on proposing more energy efficient architectures than Von Neumann architecture [33]. Researchers have focused their effort on optical computing, neuromorphic computing, quantum computing and probabilistic computing.

Optical computing uses optical systems to perform numerical computations [34]. The operations are done in the Galois Field. In order to make these operations, dedicated optical gates have been designed, especially XOR gates. In addition to a higher energy efficiency, these gates have a maximal energy frequency of 7.4 THz up to now [35]. Using the designed optical gates, all-optical logic gates have been designed [36].

The aim of neuromorphic computing is to replicate how the brain computes data in order to have higher performance and a lower energy dissipation [37]. The goal of the neuromorphic computing is to design systems with neurons, synapses and dendrites. A special effort has been made on replicating synapses with electronics devices [38]. Another research area is the optimization of the architecture, i.e. where and how to place the neurons, the synapses and the dendrites [39]. Neuromorphic systems have been designed in order to highlight the performance of such systems [40].

Quantum computing relies on the quantum information theory. Thanks to this theory and proper architecture, quantum computing can achieve a better performance for a lowest energy consumption. The particularities of the quantum computing are that 1) data are stored and process thanks to quantum dots [41] 2) algorithms are needed to decipher the data stored in the quantum dots [42]. Using quantum dots, researchers have designed quantum logic [43]. The most advanced research on quantum computing has been made by IBM and its 5 Qubit quantum computer [44].

Probabilistic computing and approximate computing is a trade-off between the accuracy of the information and the energy consumption [45]. It means that the probabilistic computing introduces an error tolerance in order to be able to use less logic gates, a lower frequency or a lower supply voltage. Probabilistic computing relies on algorithms in order to optimize the system architecture with respect to the error tolerance [46]. Like the conventional computing, approximate computing benefits from the emergence of novel technology devices such as magnetic bits [47].

Energy Efficient Techniques and Design Styles

On circuit and system-level, researchers develop techniques and design style in order to reduce the energy dissipation. A common technique to lower the dynamic energy dissipation is the Dynamic Voltage Frequency Scaling, DVFS [48]. DVFS adapts the supply voltage with respect to the needed frequency. As the dynamic energy dissipation is CV_{DD}^2, reducing the supply voltage results in an energy dissipation. In order to optimize the DVFS energy

saving, researchers have rethought the power management. The most efficient management to use DVFS is the granular power management, i.e. each function of the circuit has its own power supply [49].

There are also alternative design styles to reduce dynamic power such as the adiabatic logic [1] or sub-threshold logic [50]. The aim of the Sub-threshold logic is to have a supply voltage lower than the threshold voltage. Hence, CMOS operates in the weak inversion region instead of the strong inversion region. It leads to lower leakage current. The cost of such logic is that the maximal operating frequency is reduced. Sub-threshold logic reduces the leakage dissipation but also the dynamic dissipation. Indeed, similarly to DVFS, the supply voltage is reduced thus, the dynamic dissipation is also reduced [51].

Most of the power consumption of the digital circuit comes from the dynamic power - conventionally, the energy stored in the capacitor is dissipated twice. The essence of adiabatic logic is to charge the capacitor with a ramp then discharge the capacitor back to the supply. To save energy, the charge and discharge have to be done at the lowest frequency possible. Even if the adiabatic principle has been known since the 70's, the trade-off between the power consumption and frequency was not of particular interest. With the advancements on novel switch technologies such as carbon nanotube field effect transistors, nano-electro-mechanical switches [52] or vertical slit field effect transistors, adiabatic logic has gained a fresh interest. Even if most of the adiabatic logic families are switch-based families, some researchers have developed MEMS variable capacitors in order to be used in capacitive-based adiabatic logic [53].

1.2 Structure of the Thesis

This thesis focuses on the adiabatic logic. One of the particularity of the adiabatic logic is that power signal is also clock signal and it is referred as power-clock signal. The first objective of this thesis is to study how the power-clock signal can be generated and then to propose a power-clock supply topology in order to maximize the energy efficiency of adiabatic circuit.

In integrated design, one concern is the signal integrity [54]. The potential integrity issues come from the power delivery network and the clock delivery network. For adiabatic circuits, power delivery network and clock delivery network are combined in power-clock delivery network. The second objective of the thesis is to study how the power-clock delivery network impacts the energy efficiency of the adiabatic circuit and then to propose an optimization of the power-clock delivery network.

This thesis has been funded by the French National Research Agency, ANR, with the project ADIANEMS2 (Grant number: ANR-15-CE24-0013). This project is a collaboration between ESIEE, CEA-LETI and the LIRMM. The objectives of the project is to evaluate the poten-

tial energy saving of an adiabatic circuit using Nano-Electro-Mechanical-Switches, NEMS. While the LIRMM objective is to develop a power-clock supply and its delivery network, ESIEE research is about designing new NEMS to be used in adiabatic logic, and the role of the CEA-LETI is to develop new design logic using these NEMSs. The thesis is organized as follows:

Chapter 2: Principle of Adiabatic Logic and its Challenges

This chapter presents the adiabatic principle, i.e. how it is possible to save energy by tuning the operating frequency. Then, we introduce the challenges of the adiabatic logic using switches. Afterwards, a state of the art on the adiabatic logic families is presented. Using this state of the art, we decide to use Positive Feedback Adiabatic Logic, PFAL, as test case for our thesis objectives. In the last part of this chapter, we present how the PFAL buffer is impacted by different parameters in order to optimize it for the test case.

Chapter 3: Study of the Power-Clock Network

In the third chapter, we study the impact of the power-clock networks, PCN, on the energy efficiency of the PFAL logic. Firstly, we present a state of the art on the power-clock networks and theirs issues. Then, we study of the PCN parasitic impact on a PFAL energy dissipation. Thanks to this study, we derive constraints on the PCN parasitic in order to limit their impact. Afterwards, we investigate the impact of PCN on a circuit level and then we develop a guideline in order to optimize PCN in order to minimize the PFAL energy dissipation.

Chapter 4: Study of the Power-Clock Supply

In the fourth chapter, we study the power-clock supplies. Firstly, we present a state of the art on the power-clock supply topologies. Then, we present a power-clock supply topology in order to drive PFAL at their optimal V_{DD}. With this topology, the power-clock signal never reaches V_{DD} during this evaluation, which leads to an higher energy dissipation. Thus, we explain why and we propose the following solution to remove the additional dissipation. We use the proposed topology while the PFAL gates are supplied at their nominal V_{DD}. The solution is optimized for CMOS 65nm PFAL pipeline.

Chapter 5: Design of a CMOS Adiabatic Circuit

In the fifth chapter, we present the adiabatic circuit we have designed. The adiabatic circuit is composed of a PFAL pipeline and 4 power-clocks supplies, which are designed in CMOS 65nm. The aim of this realization is to evaluate the energy saving of adiabatic circuit using our proposed power-clock supply topology and power-clock network optimization. After

we extract the PCN parasitic, we propose a model to evaluate the energy dissipation of the circuit.

Chapter 6: Adiabatic Logic Beyond CMOS

In the sixth chapter, we propose an enhancement of the positive feedback adiabatic logic. We replace CMOS by a promising field effect transistors: CNTFET. Firstly, we present a state of the art of the CNTFET. Then, we propose an optimization of theses transistors in order to have the most energy efficient PFAL gate. Afterwards, we compare PFAL CNTFET buffers with PFAL CMOS buffers in order to highlight the qualities and the drawbacks of such logic.

Chapter 7: Conclusion

In the conclusion, we remind the objectives of the thesis. Then, we present the thesis contributions. We conclude the thesis with an opening on the current research work on the energy efficiency.

Thesis Contributions

Table 1.1 lists the thesis contributions.

Table 1.1 – THESIS CONTRIBUTIONS

Problem	Proposed solution	Chapter
Does the PCN has an impact on the adiabatic logic energy efficiency ? How can it be limited?	PCN impacts the adiabatic logic in two ways: it lowers the energy efficiency of the adiabatic logic, and it lowers the optimal operating frequency. We propose a design guideline to optimize PCN grids in order to limit its impact.	Chapter 3
How can the adiabatic logic be supplied at nominal V_{DD}?	We propose a power-clock topology which can supply any adiabatic logic, which uses switches. To our knowledge, it is the first topology which includes the synchronization between each power-clock.	Chapter 4
Why is there an additional energy dissipation in the power-clock proposed topology for a V_{DD} near threshold voltage?	The glitch is due to the pass-transistor in the PFAL buffer, we cannot model it as a constant resistance when V_{DD} is not at its nominal value. It results that an adiabatic circuit supplied by our proposed topology is more efficient at nominal V_{DD}.	Chapter 4
How much energy an adiabatic circuit with the proposed topology dissipate?	We design an adiabatic pipeline, which is supplied by the proposed power-clocks in order to quantify the energy dissipation of such supplies. With this topology, a pipeline composed of 123952 gates dissipates $59.2pJ$ per cycle, which is 3 times less than a classic CMOS pipeline.	Chapter 5
The PFAL is frequency limited. Is there a solution to improve the operating frequency?	We propose to replace CMOS transistors with CNTFET in PFAL logic. This way, PFAL is more energy efficient and its optimal operating frequency increases from $2.5MHz$ to $400MHz$.	Chapter 6

CHAPTER

2 Principle of Adiabatic Logic and its Challenges

In this chapter, we aim to present the adiabatic logic and its challenge with CMOS type logic. The chapter is organized as follows: in Section 2.1, we introduce the adiabatic logic. Then, in Section 2.2, we explain several challenges of using switches-based adiabatic logic. In Section 2.3, we present different adiabatic logic families. Finally, in Section 2.4, we introduce our most studied adiabatic logic family, the Positive Feedback Adiabatic Logic (PFAL).

2.1 Introduction of Adiabatic Logic

In this section, we introduce the principle of adiabatic logic - charging a capacitor with a ramp. Then, we explain how the adiabatic logic works.

2.1.1 Adiabatic Principle

The adiabatic switching principle is based on an efficient way to charge and discharge a capacitor by using a voltage ramp [55]. For example, the energy dissipated during the charge of the gate and load capacitances, C_{gate} through an active logic gate represented by its equivalent resistance, R_{gate} is as:

$$E_{charge} = \int_0^T R_{gate} i^2(t) dt \tag{2.1}$$

where T is the time when the power-clock supply voltage $V_\phi(t)$ ramps up from 0 to V_{DD}.

The necessary requirement to maintain the adiabatic conditions is that the output voltage is equal to the power-clock supply voltage V_ϕ, hence ramp time $T >> R_{gate}C_{gate}$ [56]. Thus, the stored charge in C_{gate} within the adiabatic conditions is $Q(t) = C_{gate}V_\phi(t)$. In addition,

the flowing current during the ramp time is constant as $i(t) = \mathrm{I} = \frac{\Delta \mathrm{Q}}{\Delta \mathrm{T}}$. Therefore, the energy dissipated during the charge time is:

$$\mathrm{E}_{charge} = \int_0^{\mathrm{T}} \mathrm{R}_{gate} i(t) \mathrm{d}t = \mathrm{R}_{gate} \mathrm{I}^2 \mathrm{T} = \frac{\mathrm{R}_{gate} \mathrm{C}_{gate}}{\mathrm{T}} \mathrm{C}_{gate} \mathrm{V}_{\mathrm{DD}}^2 \tag{2.2}$$

Similarly, by using the same equations, the energy dissipated during the discharge time can be derived. Thus, the total energy dissipated per cycle, E_{AL} is as:

$$\mathrm{E}_{\mathrm{AL}} = 2 \frac{\mathrm{R}_{gate} \mathrm{C}_{gate}}{\mathrm{T}} \mathrm{C}_{gate} \mathrm{V}_{\mathrm{DD}}^2 \tag{2.3}$$

There are two main schemes for adiabatic power-clock supply: resonant- and capacitive-based power supply. If the capacitor is charged by a capacitive-based power supply, the capacitor is charged by a ramp then the energy dissipation is E_{AL}. Else if the capacitor is charged by a sinusoidal supply instead of a ramp, the adiabatic gate will dissipate more energy. We can accurately quantify the increase in energy dissipation by multiplying the energy dissipated by $\frac{\pi^2}{8}$. Hence the adiabatic energy dissipation E_{AD} per cycle using sinusoidal signal is as:

$$\mathrm{E}_{\mathrm{AD}} = \frac{\pi^2}{4} \frac{\mathrm{R}_{gate} \mathrm{C}_{gate}}{\mathrm{T}} \mathrm{C}_{gate} \mathrm{V}_{\mathrm{DD}}^2 \tag{2.4}$$

2.1.2 Adiabatic Logic

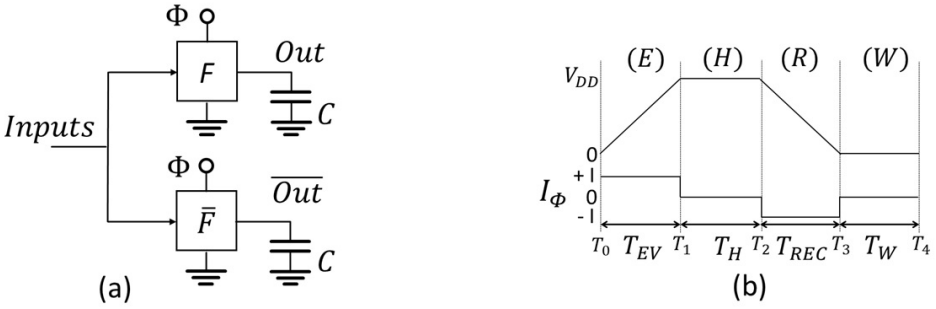

Figure 2.1 – (a) Illustration of an adiabatic logic gate with the signal and its inverted output and (b) the representation of a four phase power-clock voltage and current.

Each adiabatic gate has as output both the function and its inverse as shown in Fig.2.1.a. Most of the adiabatic logic families use the inverted signal to maintain the output signal.

Overall, adiabatic logic requires more signals than conventional logic. For example, in conventional logic, there is a power signal, clock signal, and ground, whereas in adiabatic logic there are four power-clock supply signals and ground.

The power-clock signal which is shown in Fig.2.1.b consists of four phases: the evaluation, the hold, the recovery, and the waiting phase. In normal operating conditions, an adiabatic circuit running at the frequency f has a ramp time of T. The evaluation phase occurs between T_0 and T_1, then the hold phase between T_1 and T_2. The recovery phase occurs between T_2 and T_3, and finally, the waiting phase is between T_3 and T_4.

As the power-clock signal has 4 phases, an adiabatic circuit has to have 4 different power-clock signals. Two consecutive power-clocks have a 90° phase shift. The input signal which is the output signal of the previous gate has to be in the hold phase when the power-clock signal is in the evaluation phase. Thus, in order to have the same ramp time T, each phase has the same duration then the frequency is as:

$$f = \frac{1}{4T} \tag{2.5}$$

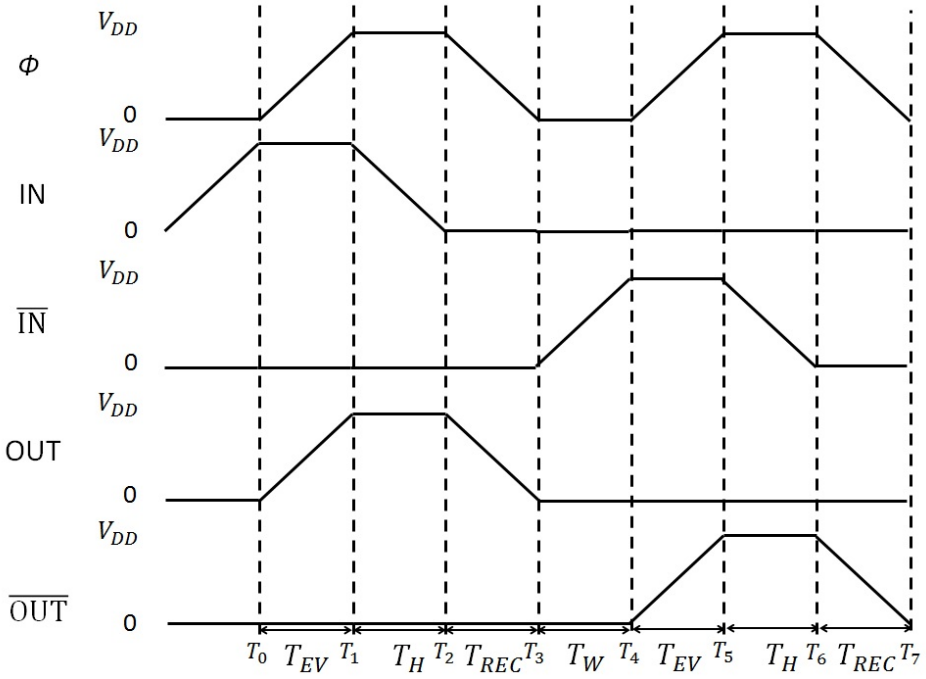

Figure 2.2 – Representation of the different signals from an adiabatic buffer.

While the conventional logic uses voltage levels to create a logic $'0'$ or $'1'$, the adiabatic logic is a pulse-based logic. For example, if the output signal stays at ground voltage V_{SS}

for a whole period, then a logic $'0'$ is created, whereas if the output signal is a 4-phase ramp (same as the power-clock signal) then a logic $'1'$ is created also shown in Fig.2.2. Due to the presence of the output and its inverted signal, the activity factor of an adiabatic circuit is always one.

2.2 Challenges of the adiabatic logic using switches

In this section, we introduce the challenges of the adiabatic logic using switches. Most of adiabatic families are designed with CMOS or NEMS, and future switch-based adiabatic logic can be designed using CNTFET or VeSFET. Despite the chosen technology, every switch-based adiabatic logic has the same challenges: the threshold voltage or the pulling voltage for the MEMS and leakages.

2.2.1 The threshold voltage

A switch-based adiabatic logic is often composed as follow: a functional block and its complementary block, and two signal hold block, one for each output signal which are shown in Fig.2.3.a. Complementary inpput signal is the input of the output signal hold block and vice-versa. Then, the hold block has to be active when its input signal is '0'. For example, the hold block can be a PMOS for CMOS based adiabatic logic.

During the recovery phase, the two input signals are at the waiting phase. It means that we can not rely on the functional block to ensure a conduction path between the output and the power-clock. Thus, the recovery is going through the hold block, in our example a PMOS.

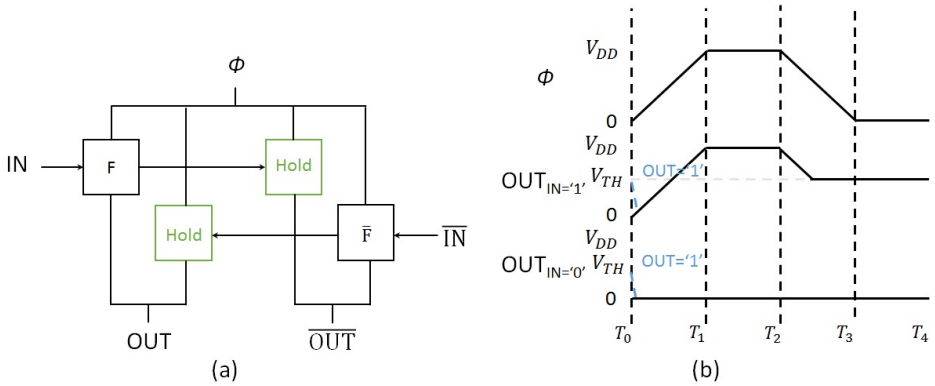

Figure 2.3 – (a) Switch-based adiabatic logic, and (b) representation of the power-clock and output signals.

Every switch has a threshold voltage, to distinguish off- and on-state. As the hold block is active when its input is '0', the output signal is passing when its voltage is between V_{TH} and V_{DD}. It means that during the recovery phase, there is a conduction path between power-clock and output as long as the power-clock signal is higher than V_{TH}. Thus, the stored energy in the output can not be fully recovered. In Fig.2.3.b, the output signal is shown with respect to V_{TH}. Moreover, the stored energy, which has not been recovered during the recovery phase is lost at the next evaluation phase. Thus, we define the energy dissipation due to the threshold voltage, E_{TH} as:

$$E_{TH} = \frac{1}{2} C V_{TH}^2 \tag{2.6}$$

As this threshold effect is not dependent of the ramp time, using Eq.(2.3) and Eq.(2.6), the minimum energy dissipation per cycle of a switch-based adiabatic logic is the threshold dissipation.

2.2.2 Adiabatic logic principle vs leakages

As we introduced in the previous subsection, the threshold voltage causes a non-adiabatic loss. Thus, we could consider to reduce V_{TH} in order to increase the recovered energy. However, the threshold voltage is one key parameter of the switch leakages. Energy dissipation per cycle coming from the leakages is expressed as:

$$E_{Leak} = V_{DD} I_{Leak} T \tag{2.7}$$

where I_{Leak} is the gate leakage current.

The total energy dissipation coming from an adiabatic circuit is expressed as:

$$E_{Tot} = E_{AL} + E_{TH} + E_{Leak} \tag{2.8}$$

When V_{TH} increases, I_{leak} is decreasing. Thus, there is a trade-off between V_{TH} and I_{Leak}. Fig.2.4 shows the different types of energy dissipation as a function of the operating frequency defined in Eq.2.5. As E_{Leak} is inversely proportional to the frequency, f, and E_{AL} is proportional to f, there is an optimal frequency f_{opt} where the leakage and the adiabatic dissipation are equivalent. There are two cases: 1) The threshold dissipation is lower than the leakage dissipation at the optimal frequency, thus f_{opt} is also the optimal frequency of the gate. 2) The threshold dissipation is higher than the leakage dissipation, thus there is a range of frequencies, where the threshold dissipation is predominant, which are the optimal frequencies of the gate. In order to highlight these two cases, the energy dissipation shown in Fig.2.4 has been done with a gate resistance of $10k\Omega$ and capacitance of $1fF$, a supply voltage of 1V and two threshold voltages: 0.3V and 0.6V.

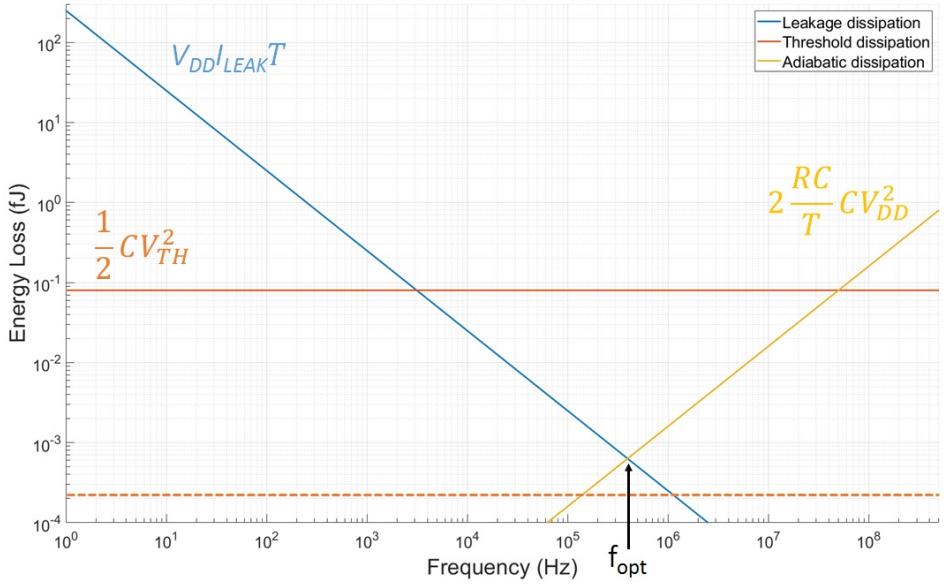

Figure 2.4 – Asymptotic representation of the different energy dissipation coming from an adiabatic logic gate as a function of the operating frequency.

In conclusion, the best switch for switch-based adiabatic logic is a switch with a low $\frac{V_{TH}}{V_{DD}}$ in order to recover most of the energy, which is stored in the gates, and with no leakage in order to reach the lowest energy dissipation E_{TH}.

2.3 Adiabatic logic families

In this section, 7 different adiabatic logic families are presented. These logics are representative of the different types of adiabatic logic. Each of these families are considered as quasi-adiabatic logic families i.e. the energy stored in the gate cannot be fully recovered due to the threshold voltage effect during the recovery phase. We could also present full-adiabatic logic families which can fully recover the energy during the recovery phase. However, due to the complexity of their implementation, these families have not been taken into consideration as a load for the power-clock study.

2.3.1 Positive Feedback Adiabatic Logic

Positive Feedback Adiabatic Logic, PFAL, is one of the most widely used adiabatic logic family [57, 58]. It is supplied by a 4-phase ramp power-clock. Thus, the frequency is as defined in Eq.(2.5).

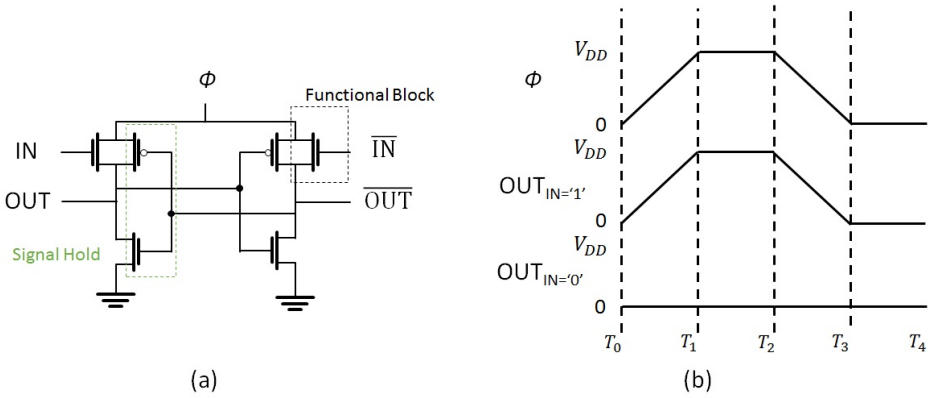

Figure 2.5 – (a) PFAL buffer, and (b) representation of the power-clock and output signals.

In Fig.2.5.a, a PFAL buffer is shown. The functional block is in parallel with a PMOS, which ensures the hold phase. Each PMOS are driven by the other output signal i.e $\overline{output}$ drives the PMOS connected to the output and vice versa. The role of the NMOS connected to V_{SS} is to discharge the energy which has not been recovered during the evaluation phase.

In Fig.2.5.b, power-clock and output signals are shown. If the buffer input is '1', then the output copies the power-clock. Else, the output remains at V_{SS}.

PFAL logic costs more area than classic logic. Indeed, hold block are composed of 4 transistors, it needs the same number of transistors to create the function, plus additional transistors for the complementary function.

2.3.2 Clocked Adiabatic Logic

Clocked Adiabatic Logic, CAL, is a 4-phase power-clock adiabatic family where the gates can be disconnected from the power-clock [59]. As the activity factor of an adiabatic gate is always 1, disconnecting the not-needed gate will decrease the adiabatic energy dissipation and the threshold dissipation.

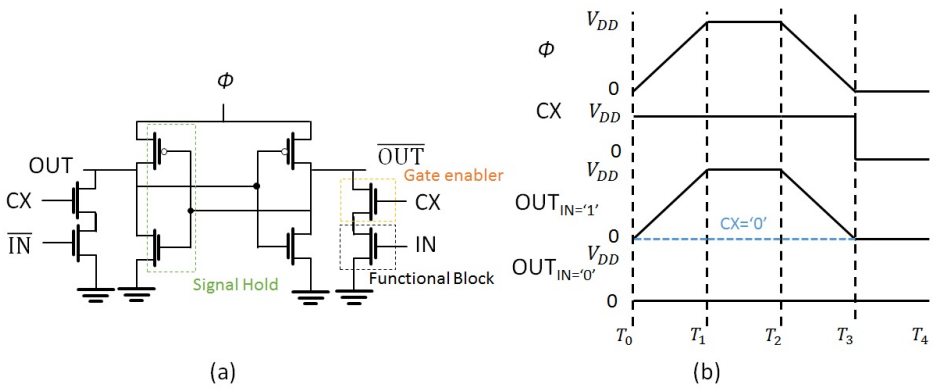

Figure 2.6 – (a) CAL buffer, and (b) representation of the power-clock and output signals.

In Fig.2.6.a, a CAL buffer is shown. There is an additional signal CX which connects the functional blocks. The main difference with PFAL is that the functional block connects the complementary output to V_{SS} instead of connecting the output to the power-clock.

In Fig.2.6.b, power-clock, CX and output signals are shown. If CX is '0', then output and $\overline{output}$ remain at V_{SS}. Else, it acts as a PFAL buffer.

CAL logic costs more area than PFAL logic due to the two additional NMOS needed to disconnect the gate. Moreover, CX signal is not an adiabatic signal, thus, the energy dissipation to charge and discharge CX NMOS is CV_{DD}^2: disconnecting gates too frequently might not save energy.

2.3.3 Two Phase Adiabatic Static Clock Logic

Two Phase Adiabatic Static Clock Logic, 2PASCL, is a two-phase power-clock adiabatic logic family [60]. It has two main advantages: as a two-phase power-clock family, for the same adiabatic dissipation Eq.(2.3), the frequency doubles; and the complementary input is not needed, i.e. the activity factor could not be 1.

In order to have a two-phase power-clock adiabatic logic without complementary signal, each gate needs two different power-clock signals (Fig.2.7), a positive power-clock which

voltage is between $\frac{V_{DD}}{2}$ and V_{DD}, and a negative power-clock which voltage is between $\frac{V_{DD}}{2}$ and V_{SS}. The next gate positive (or negative) power-clock has a 180° phase shift with the positive (resp. negative) power-clock. In total, there are 4 different power-clocks.

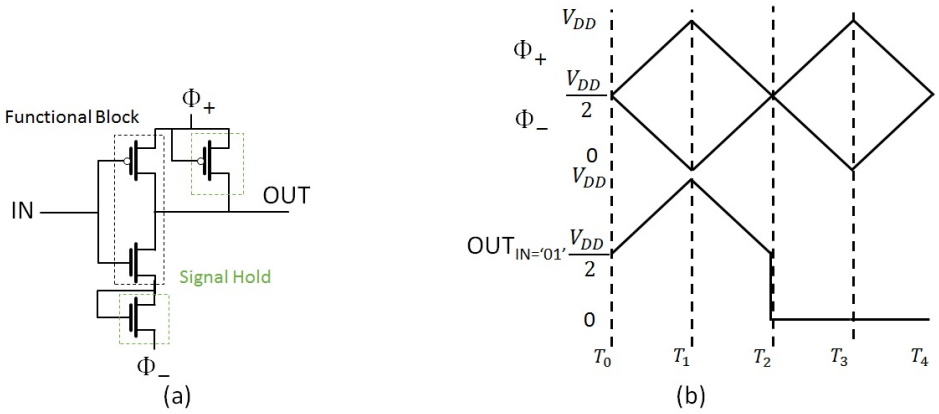

Figure 2.7 – (a) 2PASCL inverter, and (b) representation of the power-clock and output signals.

In Fig.2.7.a, a 2PASCL inverter is shown. There are the functional block and two additional hold signal MOS which are connected to the different power-clock.

In Fig.2.7.b, power-clock and output signals are shown. If the input is '0', then the output copies the positive power-clock, else it remains at V_{SS}. As the signal is recovered only from V_{DD} to $\frac{V_{DD}}{2}$ every time the input changes, there is a non-adiabatic dissipation of $\frac{1}{8}CV_{DD}^2$. It means that for high activity factor, 2PASCL can dissipate more energy than PFAL or CAL.

As there is no complementary signal, 2PASCL costs less area than the two previous families but it is also more sensitive to the noise coming from the inputs signals and the two different power clocks.

2.3.4 Pass-transistor Adiabatic Logic

Pass-transistor Adiabatic Logic, PAL, is a two-phase power-clock adiabatic family [61].

In Fig.2.8.a, a PAL buffer is shown. There are the functional and its complementary functional blocks and two hold signal PMOS. The difference with a PFAL logic is that there are no NMOS to discharge the outputs, instead there are two power-clocks. The positive power-clock which is used to charge and discharge the outputs and the negative power-clock which is used to fully discharge the outputs.

Positive and negative power-clocks have a 180° phase shift. Thus, the positive (negative)

next gate power-clock is the negative (resp. positive) current gate power-clock. A PAL circuit has only 2 power-clocks.

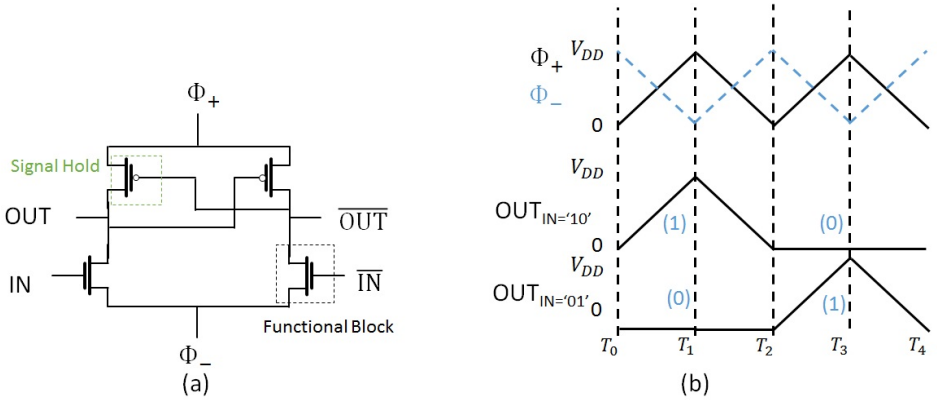

Figure 2.8 – (a) PAL buffer, and (b) representation of the power-clock and output signals.

In Fig.2.8.b, power-clock and output signals are shown. If the input is '0', then the output remains at V_{SS}, else, the input copies the positive power-clock.

PAL logic costs less area than PFAL logic but as it has two different power-clock signals and no hold phase, the noise sensitivity is increased.

2.3.5 Latched Pass-transistor Adiabatic Logic

Latched Pass-transistor Adiabatic Logic, LPAL, is a two-phase power-clock adiabatic family [59] where the gate can be disabled. It is the equivalent of the CAL family for the PAL.

In Fig.2.9.a, a LPAL buffer is shown. It is the architecture of a PAL buffer plus one NMOS and one PMOS. The aim of these additional MOS is to connect or disconnect the gate to the power-clocks. Two more signal mode and $\overline{mode}$ are needed to drive these MOS.

In Fig.2.8.b, power-clock and output signals are shown. If mode is '1', the LPAL buffer acts as a PAL buffer. Else, the output are idle. It means that the output voltages will stay at V_{DD} or V_{SS} until the gate is reconnected.

LPAL gate costs more area than a PAL gate and the same area as a PFAL gate due to the two extra MOS. As the CAL, mode and $\overline{mode}$ are not adiabatic signals which mean that every time there is a connection or a disconnection, there is an extra loss of CV_{DD}^2.

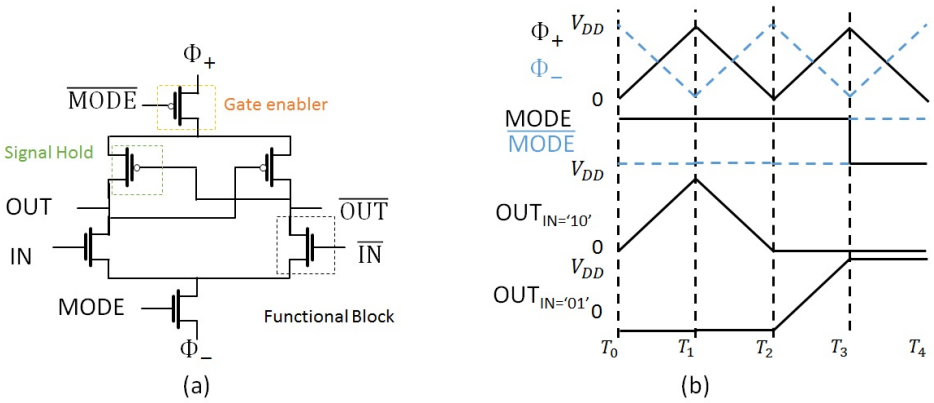

Figure 2.9 – (a) LPAL buffer, and (b) representation of the power-clock and output signals.

2.3.6 Single Rail Adiabatic Dynamic Logic

Single Rail Adiabatic Dynamic Logic, SRADL, is a 4-phase NEMS-based adiabatic logic family [52]. The 4 phases differ from the CMOS-based adiabatic families. The evaluation phase is a pre-charge phase, it charges the output if needed. The hold phase is still a hold phase, the output signal remains at V_{DD} while the input is transitioning. The recovery phase is an evaluation phase, the input is evaluated while the power-clock is ramping down. The waiting phase is an idle phase, the output is maintained. As the 4 phases are different, the state '0' and '1' are also different. A '0' (resp. '1') state is when the idle phase is at V_{DD} (resp. V_{SS}).

In Fig.2.10.a, a SRADL inverter is shown. It is composed of one NEMS. Output signal is held thanks to the second electrode of the NEMS. In order to hold the signal, a bias voltage, V_B, has to be applied to this electrode.

In Fig.2.10.b, power-clock and output signals are shown. If the input is '1', the output voltage should be at V_{DD}. Then, if the previous input was '1', the output is already at V_{DD}, thus there is no charging during the evaluation phase. Else, the output signal ramps up to V_{DD}. If the input is '0', the output should copy the power-clock. However, if the previous state was '1', the output is non-adiabatically discharged before copying the power-clock.

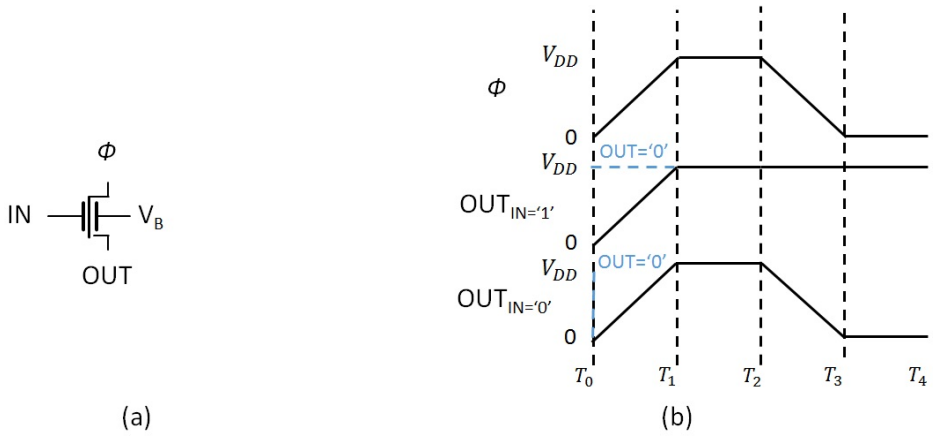

Figure 2.10 – (a) SRADL inverter, and (b) representation of the power-clock and output signals.

SRADL costs less area than the previous presented topology. As it has only one input and one 4-phase power-clock, the noise sensitivity is decreasing in comparison with the previous topology. On the other hand, NEMS is an electro-mechanical switches, thus the maximum frequency is limited by the mechanical properties of the NEMS and it will be lower than in any CMOS-based adiabatic families.

The main problem of this family is the non-adiabatic dissipation which can occur during the pre-charge phase. This energy dissipation is evaluated as $\frac{1}{2}CV_{DD}^2$.

2.3.7 Double Rail Adiabatic Dynamic Logic

Dual Rail Adiabatic Dynamic Logic, DRADL, is a 4-phase NEMS-based adiabatic logic family [52]. The main advantage of this family is that there is no non-adiabatic energy dissipation during the pre-charge phase.

In Fig.2.11.a, a DRADL inverter is shown. It is composed of one 4 NEMS. 2 NEMS are used to design the function and its complementary, and two are used to hold the signal. Similarly to the PFAL family, the complementary signal is used in order to maintain the output signal during the pre-charge phase.

In Fig.2.10.b, power-clock and output signals are shown. If the previous ouput was '0', the output remains at V_{DD} during the pre-charge and the hold phases. Then, if the input is '1', the output remains at V_{DD} during the evaluation and the idle phases, else, the output copies the power-clock.

DRADL costs more area than the SRADL as the complementary input is needed. The noise sensitivity and the maximum frequency are the same as the SRADL. The main advantage

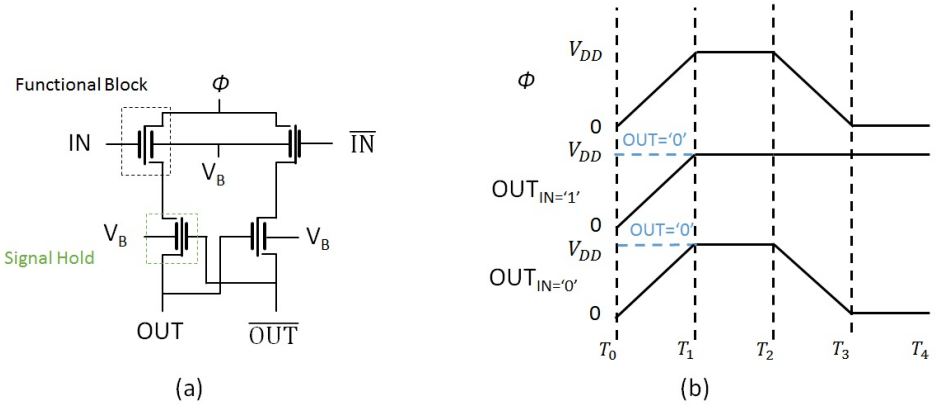

Figure 2.11 – (a) DRADL inverter, and (b) representation of the power-clock and output signals.

of this family is that there is no non-adiabatic dissipation during the pre-charge, thus the energy saving of the DRADL is better than the SRADL one.

Adiabatic Logic benefits from the innovation at the switch level as the two NEMS-based adiabatic logic families SRADL and DRADL families are the most energy-saving families. Choosing an adiabatic logic family depends on the application. There is a trade-off between the maximum frequency, the energy saving, the surface cost and the noise sensitivity. In the rest of the thesis, we choose to study the PFAL family due to its energy saving and its noise sensitivity.

2.4 Positive Feedback Adiabatic Logic

In this section, we present the load of our power-clock supplies: a PFAL pipeline. Then, we introduce the different parameters which can impact the energy dissipation such as the node technology, the MOS type, the temperature or the supply voltage.

2.4.1 PFAL pipeline

In order to develop a power-clock supply, we need a load. We choose a PFAL pipeline due to the ease of implementation. A PFAL pipeline is composed of several PFAL buffers (Fig.2.5.a). As any adiabatic circuit, a pipeline needs 4 different power-clock in order to work. Two consecutive power-clock have a 90° phase shift. In Fig.2.12, the power-clocks and the different output of a 4 stage pipeline are shown.

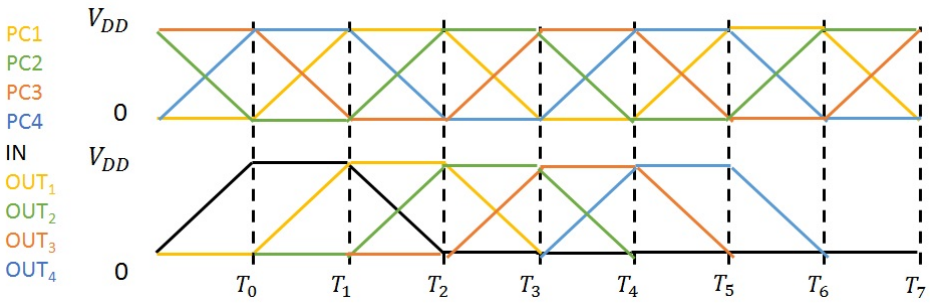

Figure 2.12 – Representation of the power-clock, the input and the output signals for a 4-pipeline.

2.4.2 Energy Dissipation

The aim of this subsection is to optimize the energy dissipation of the load. We compute the energy dissipation per cycle of a PFAL buffer. The test bench is shown in Fig.2.13.

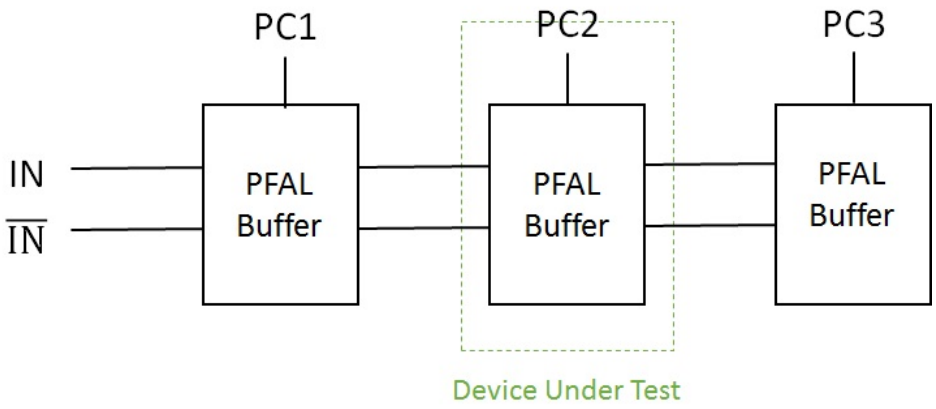

Figure 2.13 – Test bench in order to compute the energy dissipation of a PFAL buffer.

Impact of the Node Technology

In this subsection, we study the impact of the node technology on the PFAL energy dissipation. Our aim is to know if the adiabatic logic benefits from the CMOS scaling. We perform simulations in order to find the energy dissipation of PFAL using CMOS 45nm, 65nm and 180nm. PFAL is supplied by the nominal supply voltage of each node technology, e.g. V_{DD} = 1.8V for CMOS 180nm, V_{DD} = 1.2V for CMOS 65nm and V_{DD} = 1V for CMOS

45nm. CMOS have their minimal width and length in order to have the minimal energy dissipation. Simulations have been done using Berkeley model BSIM3v3.3. In Fig.2.14, PFAL energy dissipation per cycle for different CMOS technologies as a function of the operating frequency is shown.

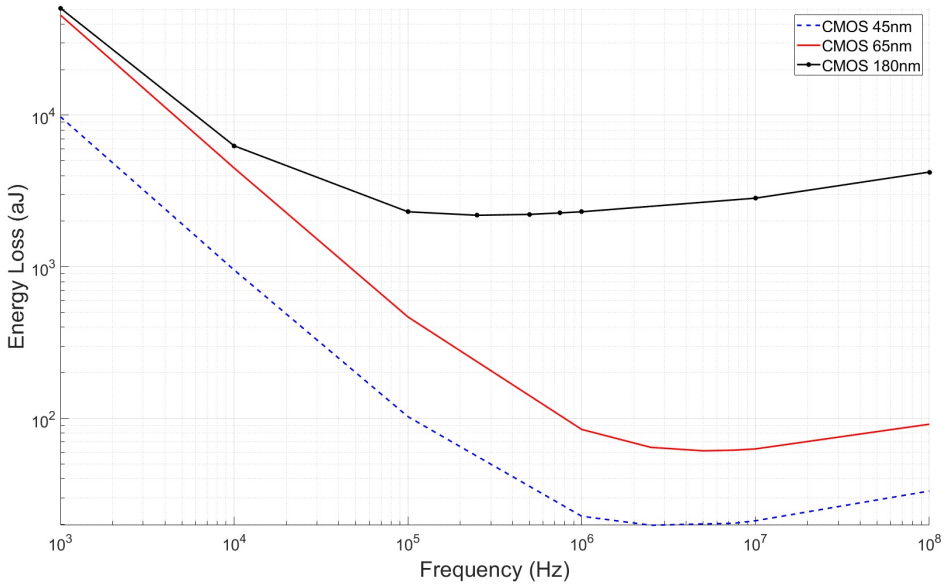

Figure 2.14 – Energy dissipation per cycle as a function of the frequency for 45, 65 and 180nm CMOS node technologies.

As the leakage current Eq.(2.7) is increasing as the node size decreases, the optimal frequency is increasing. Once could think it is an advantage of the newest nodes but with lower leakages, PFAL buffer might reach the minimum energy dissipation E_{TH}. Thanks to the CMOS scaling, C_{GATE} and V_{TH} decrease, thus, the theoretical minimum energy dissipation is decreasing Eq.(2.6). The scaling also decreases V_{DD}, thus, the adiabatic dissipation is decreasing Eq.(2.3).

Overall, adiabatic logic benefits from the CMOS scaling [62]. Indeed, even if the leakages have a higher impact for the most advanced nodes, adiabatic circuit saves energy thanks to the reduction of V_{DD}, V_{TH} and the equivalent gate capacitance C_{GATE}. For the rest of this chapter, we will study the 45nm node.

Impact of the Device Type

In this subsection, we study the impact of the device type on the PFAL energy dissipation. Our aim is to select the device type which has the best trade-off between V_{TH} and I_{leak}. Typically, CMOS have three different types of device: 1) LVT MOS, which has low-

V_{TH}, for higher frequencies applications, 2) SVT MOS, which has standard-V_{TH}, for general purposes, and 3) HVT MOS, which has high-V_{TH}, for low energy applications. As we use 45nm CMOS, the supply voltage is 1V. We perform simulations in order to compute the energy dissipation of PFAL designed with the three types of MOS devices in order to compute the energy dissipation. The energy dissipation per cycle for buffers designed with different CMOS type LVT, SVT and HVT as a function of the operating frequency is shown in Fig.2.15.

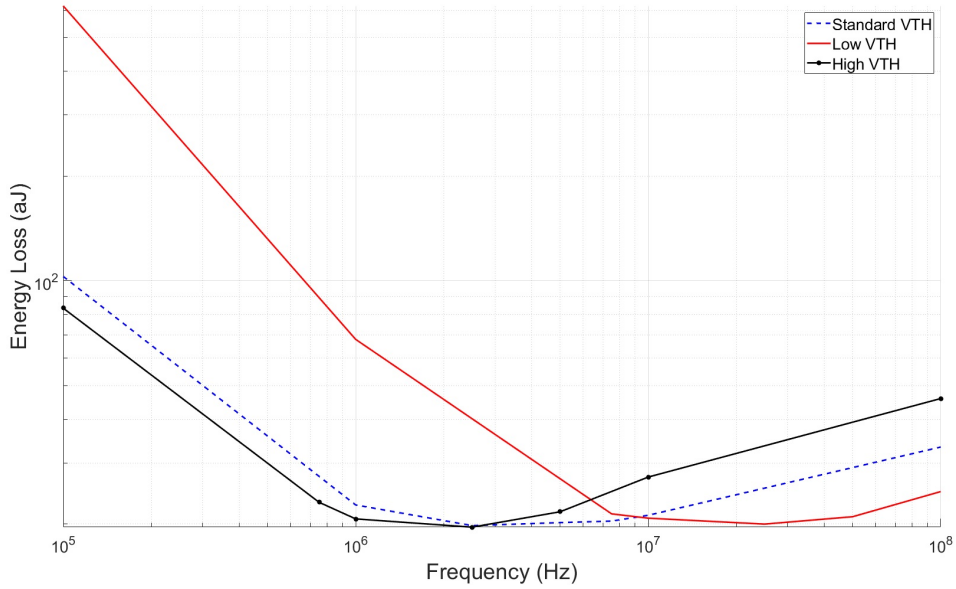

Figure 2.15 – Energy dissipation per cycle as a function of the frequency for LVT, SVT and HVT MOS.

The threshold voltage has an impact on E_{TH} and E_{Leak} as the leakage is a function of V_{TH}. Lowering V_{TH} decreases E_{TH}. However, as the leakages are increasing, the optimum frequency increases, then the PFAL buffer never reaches its theoretical minimum energy dissipation E_{TH}. Thus, High-V_{TH} CMOS are the optimal choice in order to reduce the leakages current.

Impact of the Temperature

In this subsection, we study the impact of the temperature on the PFAL energy dissipation. We perform simulations with different temperatures in order to evaluate the energy dissipation of a Standard V_{TH} CMOS PFAL buffer. The energy dissipation with different temperatures as a function of the frequency is shown in Fig.2.16.

The temperature impacts two main parameters of the energy dissipation, the leakages and the equivalent gate resistance R_{GATE}. Increasing the temperature increases the optimum

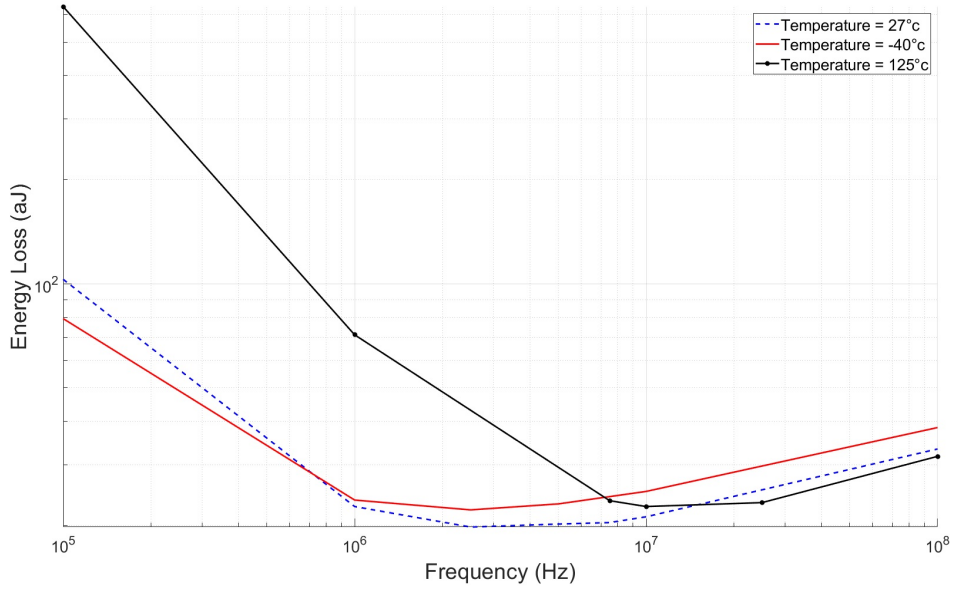

Figure 2.16 – Energy dissipation per cycle as a function of the frequency for different temperatures.

frequency. However, decreasing the temperature increases R_{GATE}. The nominal temperature, i.e. 27^o, is the best trade-off between the leakage and R_{GATE}.

Impact of the Supply Voltage

In this subsection, we study the impact of the supply voltage on the PFAL energy dissipation. The aim is to assess the potential energy saving of adiabatic logic while the supply voltage is near the threshold voltage. We perform simulations with different supply voltages to evaluate the energy dissipation of a High-V_{TH} and Low-V_{TH} PFAL buffers. In Fig.2.17, energy dissipation per cycle with two different V_{DD} as a function of the frequency is shown.

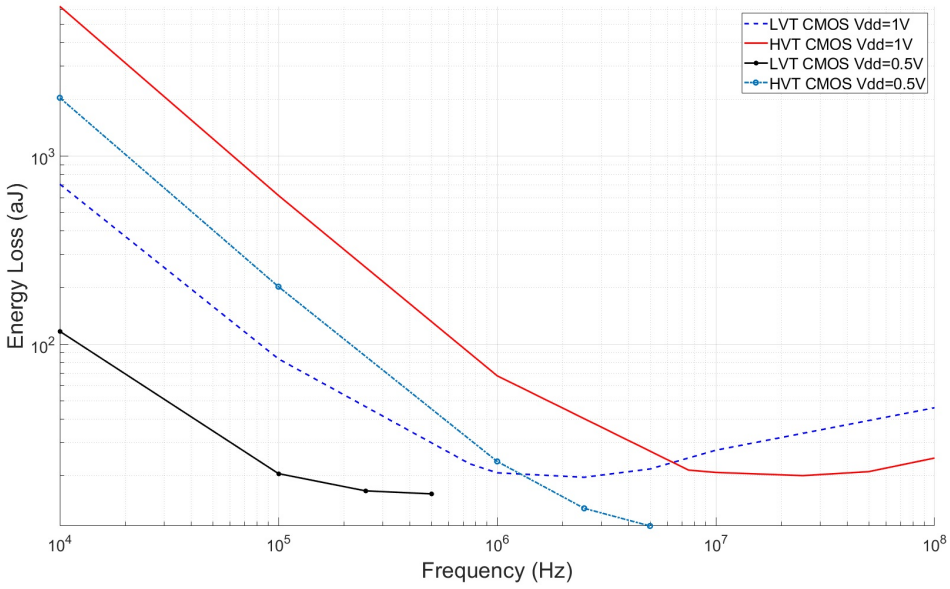

Figure 2.17 – Energy dissipation per cycle as a function of the frequency for different V_{DD} and MOS types.

When V_{DD} decreases, it reduces E_{Leak} (Eq.(2.7)) and E_{AL} (Eq.(2.3)). Similarly to the digital voltage frequency scaling [48], there is a trade-off between the maximum frequency and V_{DD}. The result of this maximum reduction is that the optimum frequency cannot be reached for the lowest V_{DD}. Thus, in order to reach the highest frequency which means the lowest dissipation, the Low-V_{TH} CMOS are the optimal choice when the circuit is supplied by near threshold V_{DD}.

In order to find the optimal supply voltage, we perform simulations to evaluate Low-V_{TH} PFAL buffer with such voltages. In Fig.2.18, the lowest energy dissipation per cycle and its optimal frequency are shown as a function of V_{DD}.

The lowest energy dissipation occurs when V_{DD} is between 0.3 and 0.5V. In order to select V_{DD}, we have also to pay attention to the operating frequency, this is why we select a V_{DD} of 0.5V as the operating frequency is 5 times higher than the frequency for a V_{DD} of 0.3V.

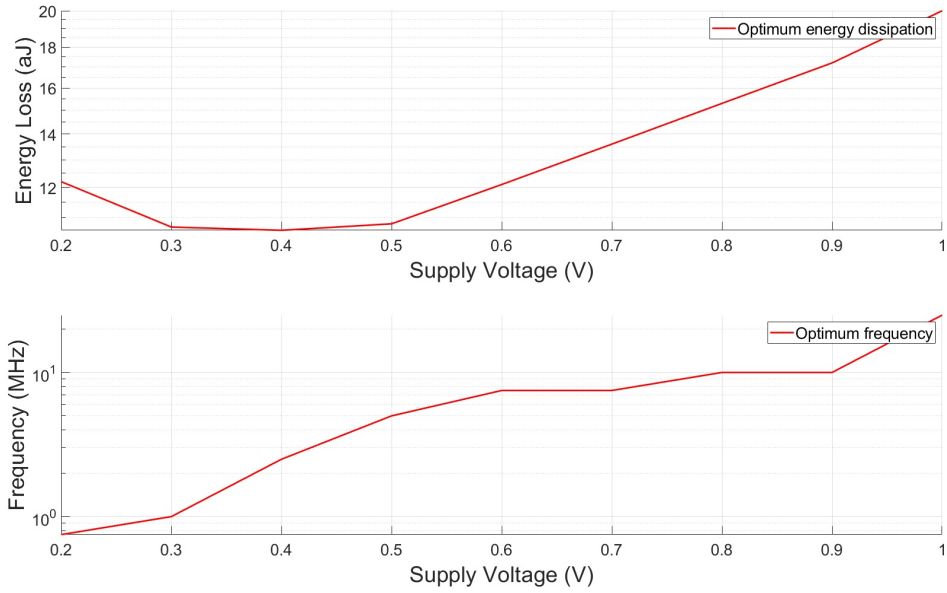

Figure 2.18 – Optimal energy dissipation and its associated frequency as a function of V_{DD}.

In this subsection, we introduce the different parameters which can impact the energy dissipation of a PFAL buffer. We choose to design PFAL buffers with Low-V_{TH}, 45nm CMOS, a supply voltage of 0.5V and a temperature of 27^oC.

2.5 Chapter conclusion

In this chapter, we present the adiabatic logic and its challenge. Adiabatic logic is based on the most efficient way to charge a capacitor: using a ramp. Instead of the classic logic, the adiabatic energy dissipation per cycle is frequency-dependent. Thus, in theory, an adiabatic gate should dissipate no energy for ultra-low frequency.

In addition to the adiabatic dissipation, switch-based adiabatic circuits have two other main dissipations: leakages dissipation and the threshold dissipation. The threshold voltage stops the discharge of the gate during the recovery phase which leads to a constant dissipation of $\frac{1}{2}CV_{TH}^2$. Leakages dissipation are also frequency-dependent and are predominant for low frequencies. Thus, there is an optimal frequency when leakages and adiabatic dissipations are equivalent.

Then, we present different types of adiabatic family. Adiabatic families can have one or two power-clocks for each gate and each power-clock can have two or four-phases. Additional

signals can be added in order to handle the activity of the gate. For our power-clock supply load, we decide to design a PFAL pipeline.

Finally, we introduce the different parameters which can impact the energy dissipation of a PFAL buffer: the node technology, the MOS type, the temperature and the supply voltage. PFAL buffer from the pipeline are designed with Low-V_{TH}, 45nm MOS, a supply voltage of 0.5V and a temperature of 27^{o}C.

CHAPTER

3 Study of the Power-Clock Network

In this chapter, we aim to investigate the power-clock network (PCN) impact on adiabatic logic. The chapter is organized as follows: in Section 3.1, we define power-clock networks and present the state of the art on the PCN. Then, in Section 3.2, we study the impact of the PCN parasitic on a single adiabatic logic gate; we aim to determine constraints on the PCN parasitic in order to limit their impact on the energy dissipation. Finally, in Section 3.3, we investigate the impact of PCN parasitic on multiple adiabatic logic gates and then we develop a guideline in order to design PCN while taking into account the impact on the overall energy dissipation.

3.1 Definition of Power-Clock Network

The aim of the power-clock network is to deliver power-clock signal to each gate of an adiabatic circuit. As mentioned in chapter 1, adiabatic circuits require four power-clock signals as each one drives one-fourth of the gates only. As the power-clock signal is both a power and a clock signal, PCN can be considered as a power delivery network [63] and a clock distribution network.

In standard design practice [64], power delivery networks can be designed as a mesh, tree or hybrid network topologies to allow for minimal voltage drop, i.e. the impedance from the power supply to the gate as shown in Fig.3.1.

As we use the same type of topologies as power delivery network, we can model the PCN parasitics using the same methods [65] and [66] i.e. modeling each branch resistance and capacitance of the chosen topology.

As a clock distribution network, the main issue of a PCN is the delay introduced by the PCN

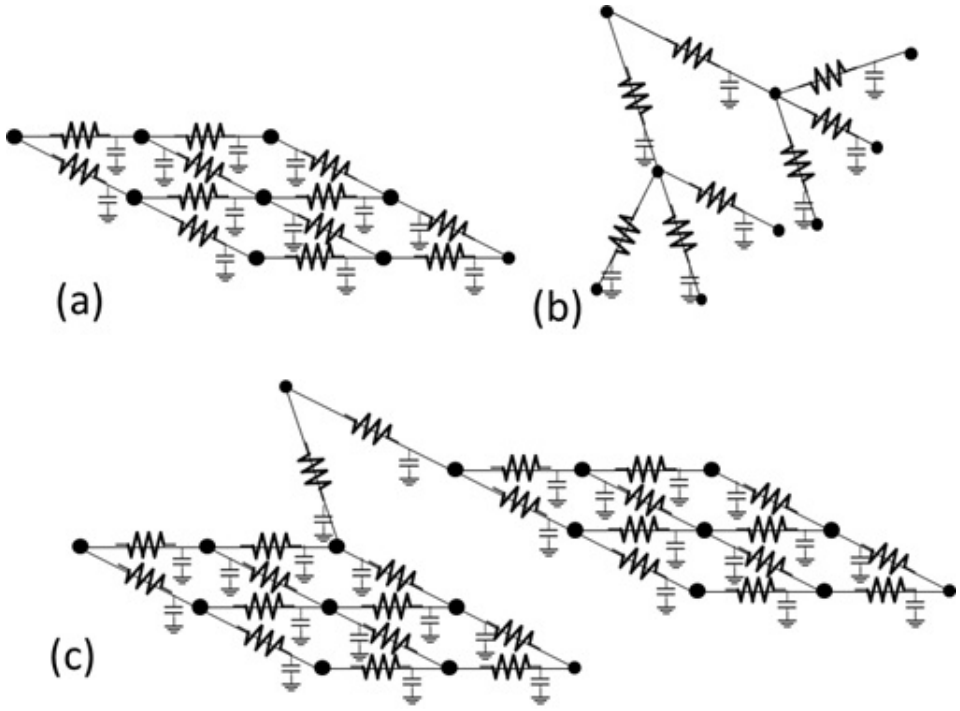

Figure 3.1 – Presentation of power delivery as (a) Mesh network, (b) tree network, (c) hybrid network.

parasitics [67]. Indeed, PCN parasitic act as a RC low pass filter which can lead to phase shifting or gain issues. Despite digital logic where the main objective is to be at the highest possible frequency, adiabatic logic tends to run at the lowest possible frequency in order to lower the adiabatic energy dissipation. Thus, the time requirements are easier to meet while designing a PCN.

As a power delivery network, PCN main issues are the IR drop [68] and the power signal noises [69]. IR drop may occur during the hold phase. Indeed, the power-clock supply acts as a DC power supply during the hold phase, thus the switches of the adiabatic gate leak. In order to limit the IR drop due to the leakage current, PCN parasitic resistances have to be sized.

Power supply noises can have an impact on the the adiabatic logic operation. During the hold phase, the input signal has to remain steady in order to avoid non adiabatic loss and insure the correct function of the gate. As the input signal is a copy of the power-clock signal of the previous gate, the power signal ripple cannot be higher than V_{TH}.

A common solution to reduce the power noises is to use a coupling capacitor [70]. In adi-

abatic logic, we cannot afford to use it as it will increase the adiabatic loss. Overall, the coupling capacitor has two main negative impacts:

— the coupling capacitor lowers the cutting frequency of the PCN parasitic low-pass filter, which can lead to phasing or gain issues.

— the coupling capacitor is also charged and discharged during the evaluation and recovery phases. Thus, it increases the adiabatic loss. For example, if we use a coupling capacitor of 1µF, in order to limit the energy dissipation coming from the coupling capacitor by the PCN by 10%, the power-clock supply has to drive at least a load capacitance of 10µF. In CMOS 45nm, it means that the power-clock supply should drive 14 billion gates in order to have the needed load capacitance.

In 2018, [71] proposes a solution to assess the parasitics of a power delivery network by testing the PDN input pad directly. This solution allows us to derive the impact of the PCN on the overall energy efficiency.

In 2016, [72] has demonstrated the benefits of using Bennett clocking on digital logic by designing a mini-MIPS microprocessor. They have to design 12 PCNs in order to deliver the 12 different power-clocks. As we are using adiabatic logic, which needs 4 different power-clock supplies, we can rely on the past work to show the feasibility of such PCNs.

3.2 Impact of the PCN Parasitics on a Single Gate

Parasitic impedance of power-clock networks (PCN) can increase the overall energy dissipation and also it may prompt to lowering switching frequency for adiabatic principle. Our objective is to show the impact of the network parasitic resistance and derive analytical formulas to quantify its effect on the adiabatic dissipation. To do so, we solve voltage differential equations from an electrical modelling of one adiabatic gate and its PCN. In this section, we study the adiabatic loss only.

3.2.1 Modelling the Energy Dissipation

Power-clock network can be designed in a tree, mesh or hybrid mesh-tree type topology. PCN interconnects can be represented by the parasitic inductance, capacitance and resistance with respect to their geometries. In this subsection, we take into account only their parasitic resistance as the capacitive and inductive effect can be ignored in a first order model. Thus, the total resistance of the charging capacitor is as:

$$R = R_{GATE} + R_{PCN} \tag{3.1}$$

where R_{PCN} is the PCN effective parasitic resistance. The complete model is presented in Fig.3.2b. Including the total resistance R, the energy dissipated by the charging and the

discharging of a single gate is as:

$$E_{ALPCN} = 2\frac{RC}{T}CV_{DD}^2 \tag{3.2}$$

Eq.(3.2) is valid as long as the adiabatic condition $T \gg RC$ is met. Otherwise, it will lead to non-adiabatic losses which reduce the energy saving.

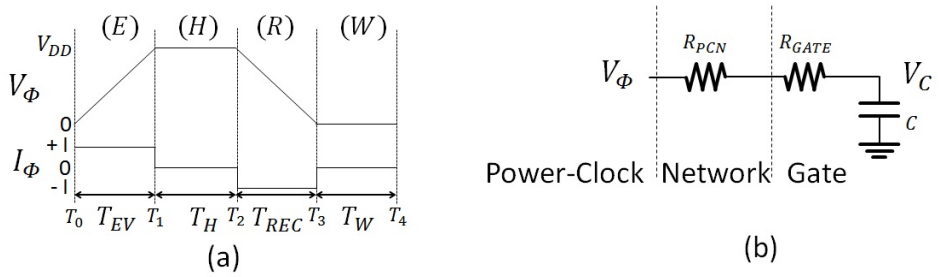

Figure 3.2 – (a) Voltage and current of power-clock signal, (b) RC modeling of one gate and power-clock network.

Voltage and Energy Dissipation

This section describes the capacitor voltage and the energy consumed by an adiabatic logic gate regardless of the ramp time. The capacitor voltage follows the first order differential equation:

$$RC\frac{\partial V_C(t)}{\partial t} + V_C(t) = V_\Phi(t) \tag{3.3}$$

Evaluation Phase

During the evaluation phase, V_Φ is ramping up to reach V_{DD} at time T_1. Using Eq.(3.3) and $V_C(T_0) = 0$, the capacitor voltage, V_C is defined as:

$$V_C(t) = \underbrace{\frac{t - T_0}{T_{EV}}V_{DD}}_{V_\Phi} + \frac{RC}{T_{EV}}V_{DD}(e^{-\frac{t-T_0}{RC}} - 1),\ T_0 \le t \le T_1 \tag{3.4}$$

where T_{EV} is the duration of the evaluation (shown in Fig.3.2a). Then, the energy loss during the evaluation time, E_{EV}, calculated between T_0 and T_1, is as:

$$E_{EV} = \frac{RC}{T_{EV}}CV_{DD}^2 - \frac{3}{2}(\frac{RC}{T_{EV}})^2CV_{DD}^2 + (\frac{RC}{T_EV})^2CV_{DD}^2 e^{\frac{-T_{EV}}{RC}}(2 - \frac{1}{2}e^{-\frac{T_{EV}}{RC}}) \tag{3.5}$$

If T_{EV} is not long enough, V_C cannot reach V_{DD}. So, we have introduced V_{EVF}, which is the V_C voltage level at time T_1:

$$V_{EVF} = V_C(T_1) = V_{DD} - \frac{RC}{T_{EV}} V_{DD}(1 - e^{-\frac{T_{EV}}{RC}}) \tag{3.6}$$

Hold Phase

The hold phase occurs between T_1 and T_2. If the circuit is not in adiabatic conditions, the capacitor will be charged while V_Φ will stay at V_{DD}. Thus, using Eq.(3.3) and $V_C(T_1) = V_{EVF}$, V_C is as:

$$V_C(t) = \underbrace{V_{DD}}_{V_\Phi} - (V_{DD} - V_{EVF}) e^{-\frac{t-T_1}{RC}}, T_1 \leq t \leq T_2 \tag{3.7}$$

Then, the energy loss during the hold phase, E_H is as:

$$E_H = \frac{1}{2} C V_{DD}(V_{DD} - V_{EVF})(1 - e^{-\frac{2T_H}{RC}}) \tag{3.8}$$

where T_H is the duration of the hold phase. In the worst case, the capacitor is not fully charged after the hold phase, we introduce V_{HF} representing the capacitor voltage at T_2:

$$V_{HF} = V_{DD} - (V_{DD} - V_{EVF}) e^{-\frac{T_H}{RC}} \tag{3.9}$$

Recovery Phase

The recovery occurs between T_2 and T_3. During the recovery phase, the power supply voltage ramps down. Using Eq.(3.3) and $V_C(T_2) = V_{HF}$, V_C is determined as:

$$V_C(t) = \underbrace{\frac{T_3 - t}{T_{REC}} V_{DD}}_{V_\Phi} + \frac{RC}{T_{REC}} V_{DD}(1 - e^{-\frac{t-T_2}{RC}}) - (V_{DD} - V_{HF}) e^{-\frac{t-T_2}{RC}}, T_2 \leq t \leq T_3 \tag{3.10}$$

where T_{REC} is the duration of the recovery phase. It leads to the energy dissipation E_{REC}:

$$E_{REC} = k_1 \frac{RC}{T_{REC}} C V_{DD}^2 + k_2 \frac{RC}{T_{REC}} C V_{DD}(V_{DD} - V_{HF}) + k_3 \frac{1}{2} C (V_{DD} - V_{HF})^2 \tag{3.11}$$

where k_1, k_2 and k_3 are defined as follows:

$$k_1 = 1 - \frac{3}{2}\frac{RC}{T_{REC}} + \frac{RC}{T_{REC}} e^{-\frac{T_REC}{RC}} (2 - \frac{1}{2} e^{-\frac{T_{REC}}{RC}}) \tag{3.12}$$

$$k_2 = 1 - e^{-\frac{T_REC}{RC}} (2 - e^{-\frac{T_REC}{RC}}) \tag{3.13}$$

$$k_3 = 1 - e^{-\frac{2T_{REC}}{RC}} \tag{3.14}$$

As the capacitor might not be fully discharged when the recovery phase is over, we introduce V_{RECF} as the capacitor voltage at T_3.

$$V_{RECF} = \frac{RC}{T_{REC}} V_{DD}(1 - e^{-\frac{T_{REC}}{RC}}) - (V_{DD} - V_{HF}) e^{-\frac{T_{REC}}{RC}} \tag{3.15}$$

Waiting Phase

The waiting phase occurs between T_3 and T_4. Finally, the capacitor is fully discharged during the waiting time. Using Eq.(3.3) and $V_C(T_3) = V_{RECF}$, V_C is determined as:

$$V_C(t) = V_{RECF} e^{-\frac{t-T_3}{RC}} \tag{3.16}$$

The difference between the others phases is that the final capacitor voltage is zero due to the reset which is mandatory in order to insure the logic function of the gate. Thus, E_W, the energy loss during the waiting phase is as:

$$E_W = \frac{1}{2} C V_{RECF}^2 \tag{3.17}$$

The total dissipated energy for one clock cycle, E_{TOT}, is given by:

$$E_{TOT} = E_{EV} + E_H + E_{REC} + E_W \tag{3.18}$$

Model Validation

The model is developed in MATLAB and has been validated by comparing it to HSPICE simulations. In Fig.3.3, the model capacitor voltage is compared to the HSPICE capacitor voltage for a ramp time of $104 * R_{GATE}C$ and a R_{PCN} of $0.1 * R_{GATE}$ with $R_{GATE} = 10k\Omega$, $C = 1fF$ and $V_{DD} = 1V$. This is an example to show how the model fit the electrical simulations, the parameters have been taken randomly regardless of the adiabatic conditions. The model is valid for any resistance or capacitance at any frequency.

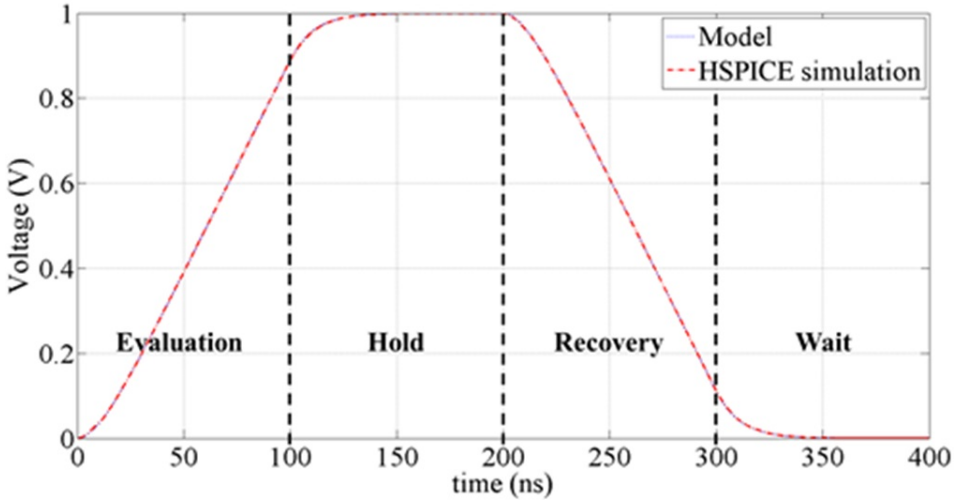

Figure 3.3 – Analytical equation resolution vs electrical simulation for the capacitor voltage.

3.2.2 Simulations

In this subsection, we derive the impact of PCN on the energy dissipation for a single adiabatic logic gate. We use clock period parameters as $T = T_{EV} = T_H = T_{REC} = T_W$ in order to represent the clock properties for most of the adiabatic logic families, $V_{DD} = 1V$, $R_{GATE} = 10k\Omega$ and $C = 1fF$ to represent a PFAL gate with high-V_{TH} CMOS 45nm technology.

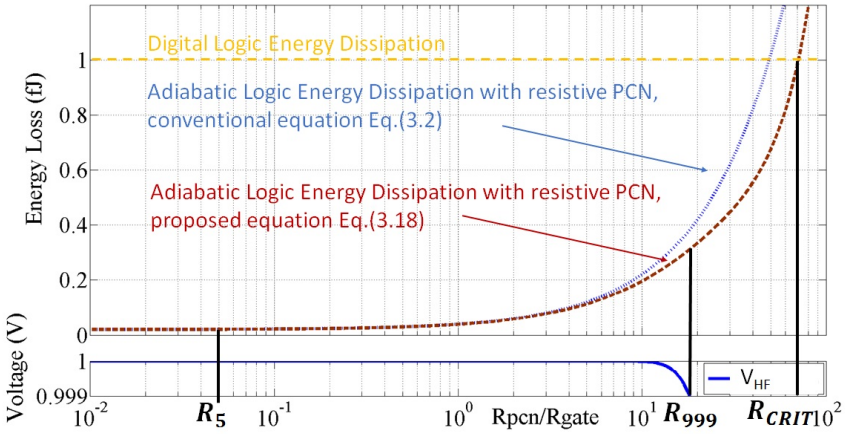

Figure 3.4 – Energy loss and V_{HF} against the total PCN resistance.

In Fig.3.4, the energies calculated from different expressions are shown against the total PCN resistance for a ramp time of $10000 * R_{GATE}C$ i.e. $T = 100ns$ which is a usual value for adiabatic logic designs. For a given T, we introduce three boundaries in order to help designers to find the optimal resistance considering their constraints. Regardless of the chosen maximum resistance between these constraints, E_{TOT} is lower than E_{ALPCN} defined in Eq.(3.2) because the negative term $\frac{RC}{T}^2$ in Eq.(3.5) and Eq.(3.8) is predominant. It means E_{ALPCN} can be used as a pessimistic estimation of the total energy loss.

In Fig.3.4, we also introduce 3 different constraints on the PCN: R_5, R_{999} and R_{CRIT}.

With R_5 as the maximum resistance, the total energy loss is at most 5% higher than the energy dissipated without power-clock network, i.e. as the expression defined in Eq.(3.2). Designers can change this constraint to operate at a higher frequency or to save more energy.

With R_{999} as the maximum PCN resistance, we impose a constraint on V_{HF} in order to have the load capacitor fully charged. As R_{999} is 19 times higher than R_{GATE}, this value is never reached in practice. It means that the output will always be at V_{DD} during the hold phase, which ensures the operation of the adiabatic circuit.

With R_{CRIT} as the maximum resistance, the circuit will dissipate the same energy using the conventional logic, which means there is no point to use the adiabatic logic. The conventional logic energy loss is actually lowered by the activity factor of the circuit, whereas the adiabatic logic energy loss is not. This is why designers have to pay a particular attention to the activity factor of the operation in order to ensure that the circuit dissipates less energy than with conventional logic.

As the total energy loss is lower than Eq.(3.2), we can use Eq.(3.2) to directly derive an expression combining the maximum tolerated PCN resistance, R_{PCNT}, R_{GATE}, and the maximum tolerated additional energy dissipation, A_{PCN}: $R_{PCNT} = A_{PCN}R_{GATE}$. A_{PCN} is linked to the constraint on the resistance, e.g. if designers choose R_5, A_{PCN} will be 0.05.

This model validates the use of expression Eq.(3.2) as the total energy loss. Eq.(3.2) allows a quantitative answer on the tolerated parasitic resistance of the PCN without disrupting adiabatic conditions and gives the minimum ramping time in order to meet the adiabatic conditions for a given PCN resistance.

3.2.3 Conclusion

In this section, we investigate the impact of the power-clock network on the energy efficiency of an adiabatic circuit. We present analytical models for computing the dissipated energy in order to determine the maximum resistance of Power-Clock Network for a given frequency such that adiabatic conditions are met.

This model gives the energy dissipation with respect of the Power-Clock Network, PCN,

resistance. Based on mathematical simulations, we fix a constraint on the maximum PCN resistance in order to quantify the impact of the PCN on the energy dissipation.

We also demonstrate that Eq.(3.2) can be used as a fair estimation of the adiabatic logic energy dissipation as it is is always a pessimistic estimation of the energy dissipation derived from our model Eq.(3.18).

Then, we define three constraints in order to assess the impact on the energy dissipation of the PCN: R_5, R_{999} and R_{CRIT}. The energy dissipation will increase by 5% if the PCN resistance is equal to R_5. If the PCN resistance is higher than R_{999}, the load capacitance, i.e. the gate, cannot be fully charged. Thus for higher PCN resistance value, the functionality cannot be ensured. Finally, if the PCN resistance is higher than R_{CRIT}, the energy dissipation of an adiabatic logic gate is higher than the one of digital logic.

In conclusion, we demonstrate the impact of the PCN on the adiabatic energy dissipation using a single gate. We can improve this study by investigating the impact of the PCN on multiple gates as a standard application case would be and by considering the leakage and threshold energy dissipations also. This is the work that is presented in the next section.

3.3 Impact of the PCN parasitics on multiple gates

Here, we investigate PCN impact on adiabatic energy consumption and provide a design guideline for optimal PCN to limit power dissipation. As a case study, we utilize a high-V_{TH} 45nm CMOS based adiabatic pipeline benchmark. The main objective of this section is to derive the parasitic resistance, and capacitance values of the PCN interconnect such that it minimizes the PCN energy dissipation. This is performed in two steps. In a first step, we determine the maximum tolerable PCN interconnect resistance as a function of the given design parameters such as the number of gates and the targeting operating frequency. In a second step, we determine the maximum tolerable PCN interconnect capacitance for the design parameters and the derived interconnect resistance from step one. Based on these analytical formulas, we finally propose a design guideline to determine the optimal PCN interconnect resistance and capacitance for minimal energy consumption in adiabatic pipeline circuits.

3.4 Motivational Experiment

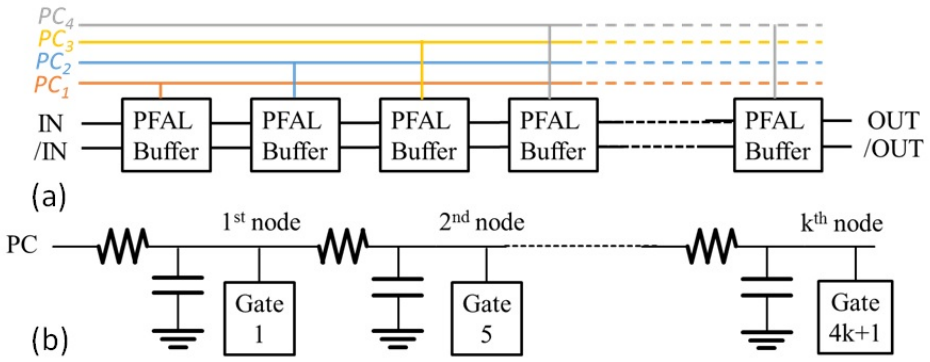

Figure 3.5 – (a) Illustration of the vehicle adiabatic pipeline circuit of 48 stages with PFAL buffer gates and power-clock supplies, (b) model of the power-clock network with parasitic resistance and capacitance.

To motivate our work and highlight the importance of the power-clock network on adiabatic logic, we perform simulations on a vehicle adiabatic pipeline circuit as shown in Fig.3.5a. The circuit is a 48-stage pipeline with PFAL buffer gates. As aforementioned, the adiabatic pipeline circuit requires four sinusoidal power-clock supplies, hence four different power-clock networks. Fig.3.5b shows the model of one of the power-clock network. The model is based on a tree-type topology where each PCN branch is represented by its parasitic resistance and capacitance. We study the impact of these parasitics on adiabatic energy dissipation and operating frequency.

To investigate the influence of PCN on adiabatic logic, we compare three different pipeline circuits. The first benchmark is a 48-stage pipeline with PFAL buffer gates without PCN parasitics (ideal PCN); the second one is the same 48-stage PFAL buffer gates with PCN parasitics (non-ideal PCN), and the third benchmark is a 48-stage pipeline with standard CMOS buffer gates with an activity factor of one and designed in 45nm technology node. For the non-ideal PCN, we have chosen arbitrarily the parasitic resistance of 100Ω and capacitance of $10fF$ to represent each branch found in the power delivery network [73].

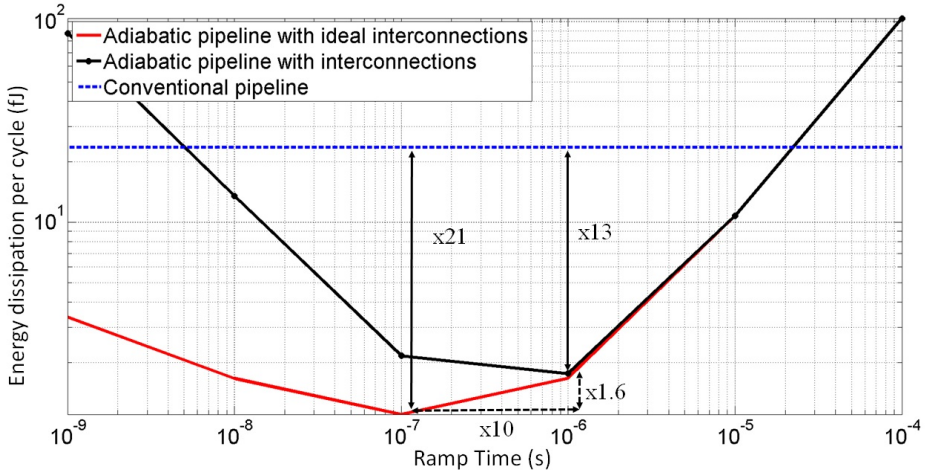

Figure 3.6 – Energy dissipation per cycle of a 48-stage buffer pipeline as a function of the ramp time while using adiabatic and conventional CMOS buffer gates.

In Fig.3.6, we show the energy dissipation per cycle as a function of the power-clock time ramp for each pipeline circuit. We derive that for the adiabatic logic with ideal PCN, the optimal ramp time is 10^{-7}s or an optimal frequency of 2.5MHz while consuming up to 21 times less energy than the CMOS-buffer pipeline circuit. Whereas, for adiabatic logic with non-ideal PCN, the optimal ramp time is obtained at 10^{-6}s or an optimum frequency of $250kHz$ while consuming up to 13 times less energy than the CMOS-buffer pipeline circuit.

This experiment shows that a 48-stage pipeline adiabatic logic can dissipate 21 times less energy per cycle than a conventional CMOS pipeline. Thus, there is a potential gain to use adiabatic logic. However, when PCN parasitics are included, the adiabatic logic circuit dissipates 13 times less energy only than the conventional CMOS pipeline and also the optimum frequency is lowered by 10. This example clearly underlines the effect of PCN parasitics and the need to study thir effect on the overall power saving to achieve ultra-low power adiabatic circuit.

We propose a design guideline to determine the maximum tolerable PCN resistance and

capacitance to limit the impact on energy dissipation while the adiabatic circuit is supplied by a sinusoidal power-clock.

3.4.1 Design Guideline to Limit the Impact of Power-Clock Networks on Adiabatic Logic

In this section, we describe our heuristic design guideline approach based on empirical data obtained from circuit-level simulation. The objective of our heuristic design approach is to determine the maximum R_{max} and C_{max} parasitic values to limit the impact of PCN on adiabatic energy loss by up to 5%. In other words, we aim to identify the PCN branch sizing to minimize the impact on adiabatic energy efficiency. Please note that the threshold of 5% is simply used as a case study to show our heuristic approach. However, other threshold limits can be imposed depending on the circuit.

The proposed heuristic design guideline is based on three main steps:

— We determine the maximum R_{max} value based on empirical data from circuit simulation while varying the number of pipelined buffer gates, N and ramp time, T.

— Once R_{max} is determined, we derive maximum C_{max} based on empirical data from circuit simulation with respect to R_{max}, the number of pipelined buffer gates, N and the ramp time, T.

— To validate our findings of R_{max} and C_{max}, we compare the results of our empirical formulas with different pipeline buffer circuits.

Based on empirical data from simulations, we derive formulas to determine the maximum PCN parasitics (R_{max} and C_{max}). We choose to study the energy dissipation per cycle with a ramp time, T from $1ns$ to $10\mu s$. Below $1ns$, the gate output signal does not reach the supply voltage V_{dd} because the equivalent gate capacitance cannot be fully charged. Above $10\mu s$, the leakage current becomes so important that the conventional CMOS pipeline dissipates less energy than the adiabatic pipeline. Hence, we focus our study on voltage ramp time between $1ns$ to $10\mu s$.

The objective is to determine the relation between R_{max}, the number of gates N and ramp time T. The purpose of simulations is to derive a model and to ensure the independence of the parameters N and T. This is why we find R_{max} as a function of N with different values of T then as a function of T.

Once R_{max} is determined, we can derive C_{max}. C_{max} has an additional parameter, the PCN parasitic resistance R. This parameter has to be lower than R_{max} by definition. We perform several simulations to model the relation between C_{max} and R, N, and T but also ensure the independence of the parameters. This is why we find C_{max} as a function of R with different values of N and T, then as a function of N with different values of R and T, and finally as a function of T.

To validate our models, we compare the results from our formulas to a typical N-size pipeline to prove their accuracy.

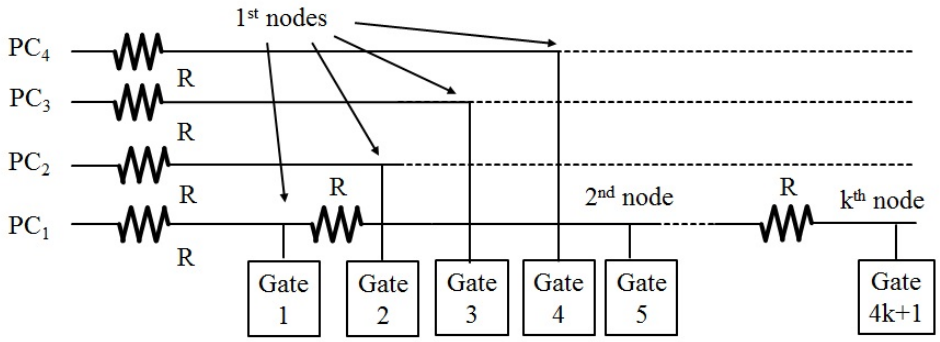

Figure 3.7 – Illustration of four power-clock networks represented by parasitics resistances only.

Deriving Maximum Resistance, R_{max}

One of the main impacts on adiabatic energy efficiency is due to the energy dissipation of parasitic PCN resistance. To determine R_{max}, PCNs are modeled without parasitic capacitance. There are four PCNs connected to each gate by a parasitic resistance network as shown in Fig.3.7.

To determine the relation between R_{max} and the number of gates N, we perform simulations on adiabatic pipelines with several values of N. We also use different ramp times T to be certain that the parameters N and T are independent. Fig.3.8 shows the results of R_{max} versus the number of gates and different ramp times. The analytical formula to describe the relation of R_{max} and N based on the simulation results is derived by mathematical regression as:

$$R_{max}(N,T) = \frac{R_N^o(T)}{N^{1.89}} \tag{3.19}$$

where R_N^o is a function of the ramp time.

To determine R_N^o, we perform simulations with different ramp times for a 48-stage adiabatic pipeline as shown in Fig.3.9. To derive R_N^o, we have to split the modeling into two parts: adiabatic and leakage dissipations. If the adiabatic dissipation is predominant, the energy loss decreases when T is increasing.Whereas, if the leakage dissipation is predominant then the energy dissipation increases when T is increasing.

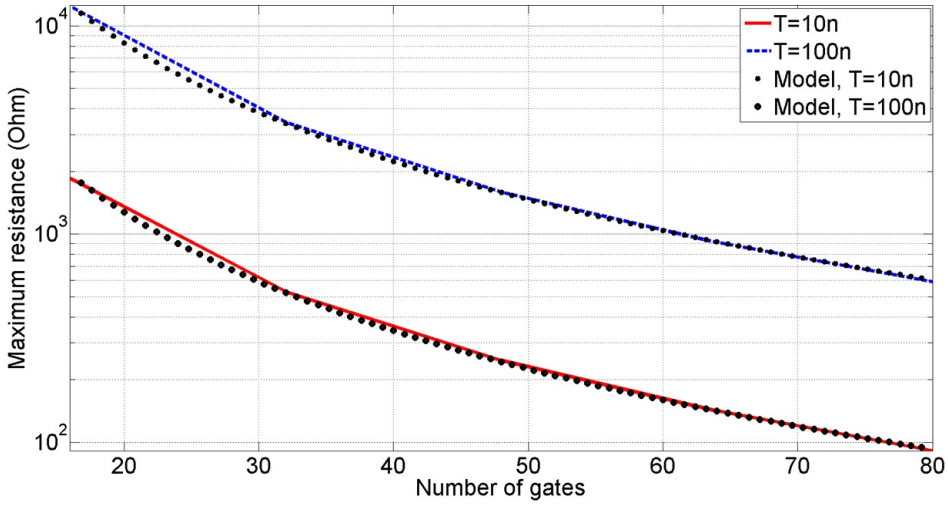

Figure 3.8 – Parasitics resistance, R_{max} versus the adiabatic pipeline number of gates for various ramp times.

Referring to the Fig.3.6, we observe that the adiabatic losses are predominant when the time ramp is less than $500ns$. If the time ramp is larger than $5\mu s$, the leakage losses become predominant. Both the adiabatic and leakage predominant parts are proportional to the ramp time. We derive a model that can fit the electrical simulation by applying a 3^{rd} and 2^{nd} order linear regression of the adiabatic and the leakage dissipation, respectively. Thus, R_N^o determined by the leakage dissipation model R_{leak} is as:

$$R_{leak}(T) = \beta_{leak} T^2 - \alpha_{leak} T + R_{leak}^o \tag{3.20}$$

where $R_{leak}^o = 33.6M\Omega$, $\alpha_{leak} = 26,9T\Omega.s^{-1}$ and $\beta_{leak} = 33.3E\Omega.s^{-2}$.

Then, R_N^o determined by the adiabatic dissipation model R_{ad} is as:

$$R_{ad}(T) = \gamma_{ad} T^3 - \beta_{ad} T^2 + \alpha_{ad} T + R_{ad}^o \tag{3.21}$$

where $R_{ad}^o = 77.8k\Omega$, $\alpha_{ad} = 26,9T\Omega.s^{-1}$, $\beta_{leak} = 47.9E\Omega.s^{-2}$ and $\beta_{leak} = 95Y\Omega.s^{-3}$.

Finally, R_{max} can be determined by combining the above equations as:

$$R_{max}(N,T) = \frac{R_N^o(T)}{N^{1.89}} = \frac{min(R_{leak}(T); R_{ad}(T))}{N^{1.89}} \tag{3.22}$$

Based on these analytical formulas, we can determine the maximum parasitic resistance, R_{max} to limit PCN impact on adiabatic energy efficiency by 5%. The dimensions (i.e. width,

length) of the PCN interconnect branch can also be derived based on the R_{max} for a given technology node.

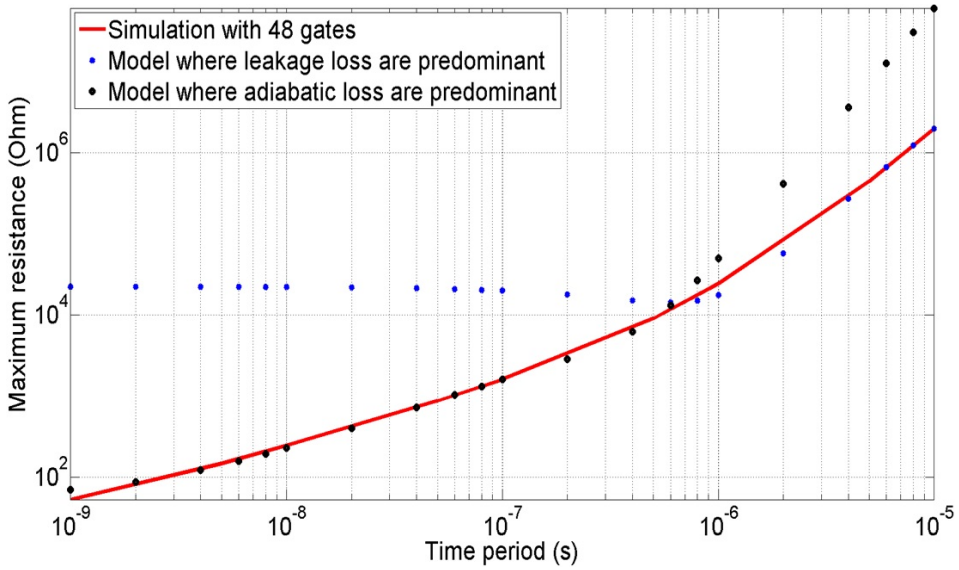

Figure 3.9 – Maximum PCN resistance as a function of the ramp time.

Deriving Maximum Capacitance, C_{max}

The presence of parasitic capacitance on PCNs also plays a crucial role on the adiabatic energy efficiency. PCN capacitance increases the energy dissipation in two ways: power-supplies have to charge a higher capacitance and the PCN interconnect resistance and capacitance act as a low-pass RC filter. To determine C_{max}, we utilize the same PCN configuration as shown in Fig.3.7.

To determine the maximum PCN capacitance, we perform simulations on adiabatic pipelines with several gates, N, different ramp times, T while also varying the maximum PCN resistance, R_{max}. Fig.3.10 shows the simulation results for a different number of gates, ramp times and PCN resistances. We also plot C_{max} based on our analytical model and simulation results. Based on these simulations, we can model the relation between C_{max} and N by using linear regression as:

$$C_{max}(R,N,T) = \frac{C_N^o(R,T)}{N} \tag{3.23}$$

where C_N^o is a function of the parasitic PCN resistance and the ramp time.

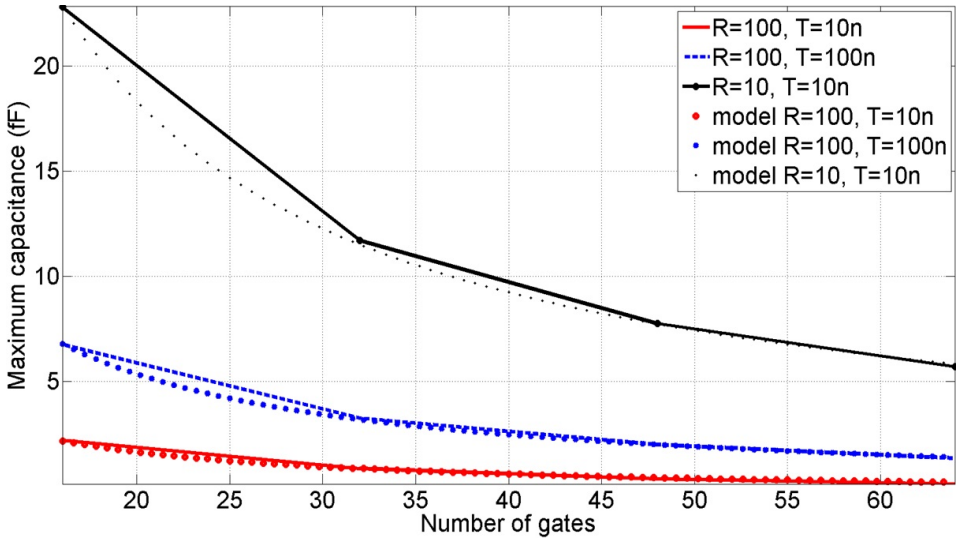

Figure 3.10 – Maximum capacitance as a function of the number of gates and the model.

We perform simulations to determine the relation between C_N^o and R_{max}. Results are shown in Fig.3.11 where C_{max} is inversely proportional to PCN resistance. By applying linear regression, we model C_{max} as:

$$C_{max}(R,N,T) = \frac{C_N^o(R,T)}{N} = \frac{C_R^o(T)}{N\sqrt{R_{max}}} \tag{3.24}$$

where C_R^o is a function of the ramp time.

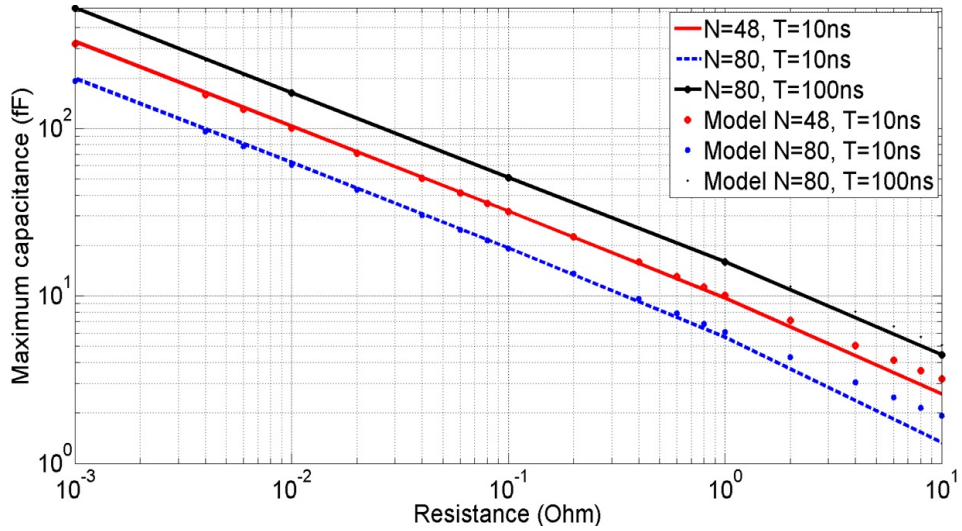

Figure 3.11 – Maximum PCN capacitance as a function of the interconnect parasitic resistance. Comparison between analytical model versus the simulation results.

Now, we determine the relation between C_R^o and the ramp time, T. We model C_R^o when the leakage losses are predominant, C_{leak} and when the adiabatic losses are predominant, C_{ad}. The results are shown in Fig.3.12.

We model C_{leak} as:

$$C_{leak}(T) = \delta_{leak} T \tag{3.25}$$

where $\delta_{leak} = 388nF.\Omega.s^{-1}$.

Then, we model C_{ad} as:

$$C_{ad}(T) = \delta_{ad} T^{0.39} \tag{3.26}$$

where $\delta_{ad} = 662pF.\Omega.s^{-0.39}$. Finally C_{max} is computed as the maximum of C_{leak} and C_{ad} as:

$$C_{max}(R,N,T) = \frac{C_R^o(T)}{N\sqrt{R_{max}}} = \frac{MAX(C_{leak}(T), C_{ad}(T))}{N\sqrt{R_{max}}} \tag{3.27}$$

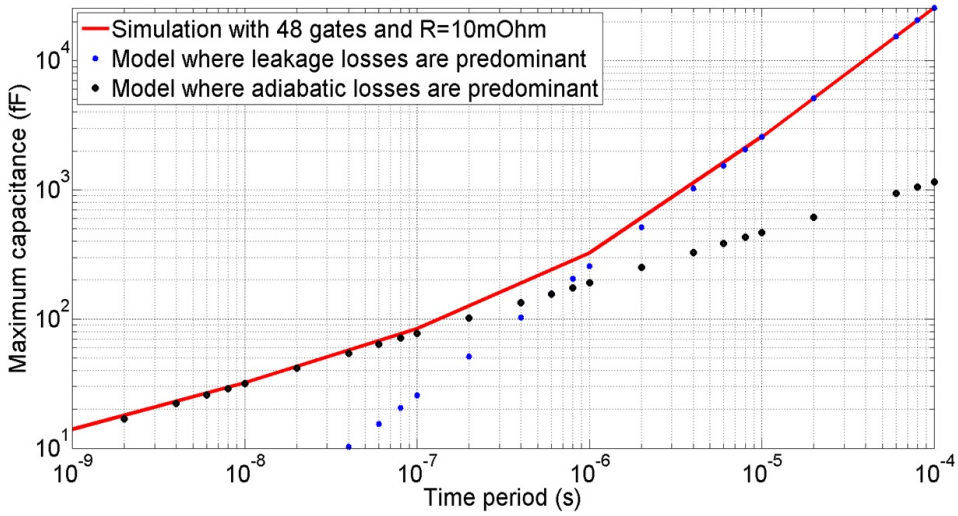

Figure 3.12 – Maximum capacitance as a function of the ramp time and the associated models of C_{leak} and C_{ad}.

In summary, we have derived analytical formulas for maximum PCN resistance and capacitance based on exhaustive simulations to capture their trend with different size of the adiabatic pipeline and power-clock signal ramp time. Deriving R_{max} and C_{max} allows us to further determine the geometrical dimensions of the PCN interconnect branches for minimal impact on energy dissipation. The size of each PCN branch will also determine the overall size of the PCN network for each power supply.

3.5 Simulations

We perform experiments on several benchmarks with different sizes of adiabatic pipelines. We derive R_{max} and C_{max} on three different benchmarks and with six different power-clock ramp times. The pipeline sizes from 48- to 80-stages are simulated where each power-clock network is driving from 12 to 20 gates. The ramp time values have been chosen to represent the operating frequency of an adiabatic circuit.

3.5.1 Validation of R_{max} and C_{max}

To determine the accuracy of the R_{max} analytical model, we study three cases: $case1$ is a 40-stage adiabatic pipeline; $case2$ is a 64-stage adiabatic pipeline and $case3$ is an 80-stage adiabatic pipeline. In Table 3.2, we show the percentage of difference between R_{max} when computed using our analytical model versus simulation data.

Table 3.1 – PERCENTAGE OF DIFFERENCE BETWEEN THE ELECTRICAL SIMULATION R_{max} AND THE ANALYTICAL MODEL

	Ramp Time, T (ns)					
N	1	10	100	1000	10k	100k
48-stage	31.76%	3.98%	0.20%	37.71%	0.30%	0.01%
64-stage	32.13%	3.87%	0.18%	36.53%	0.33%	0%
80-stage	27.56%	3.76%	0.05%	37.50%	0.29%	0%

The model fits simulation data with some discrepancies, and we deduce two regions where it lacks accuracy. For ramp time values, T less than $1ns$, there is a mean error of 30%. This is because the pipeline is working at its maximum reachable frequency. Hence, the gate capacitances cannot be fully charged what changes the behavior of the energy dissipation.

The second discrepancy region is from $500ns$ to $5\mu s$ where neither the leakage and adiabatic losses are predominant that is why the analytical model does not fit the simulation. It means that our model is accurate only if leakage losses or the adiabatic loss are predominant.

To determine the accuracy of the C_{max} model, we study three cases: $case1$ is a 40-stage adiabatic pipeline with PCN interconnect resistance of $10m\Omega$; $case2$ is a 40-stage adiabatic pipeline with a PCN interconnect resistance of $100m\Omega$ and $case3$ is an 80-stage adiabatic pipeline with a PCN interconnect resistance of 1Ω. Table 3.2 shows the percentage difference of C_{max} between the electrical simulation data and the analytical model.

Table 3.2 – PERCENTAGE OF DIFFERENCE BETWEEN THE ELECTRICAL SIMULATION C_{max} AND THE ANALYTICAL MODEL

	Ramp Time, T(ns)					
{N-stage,R(Ω)}	1	10	100	1000	10k	100k
{48, 0.01Ω}	7.86%	1.63%	4.29%	27.2%	5.19%	1.25%
{48, 0.1Ω}	3.81%	3.45%	3.33%	26.9%	0.33%	0.25%
{80, 1Ω}	6.62%	7.92%	1.18%	27.2%	1.85%	0%

The model fits simulations with some discrepancy for the ramp time region between $500ns$ and $5000ns$. The mean error is 27% similarly as our analytical model of C_{max}, which is not accurate in this region where neither adiabatic nor leakage losses are predominant.

Long-Size Pipeline

We develop our analytical model from short-size pipeline because of the exponential increase in the simulation time as function of the number of gates. Nevertheless, we validate the model with long-size pipeline. To determine the accuracy of R_{max} model, we study three different pipeline size: 1024, 4096 and 16384 numbers of gates.

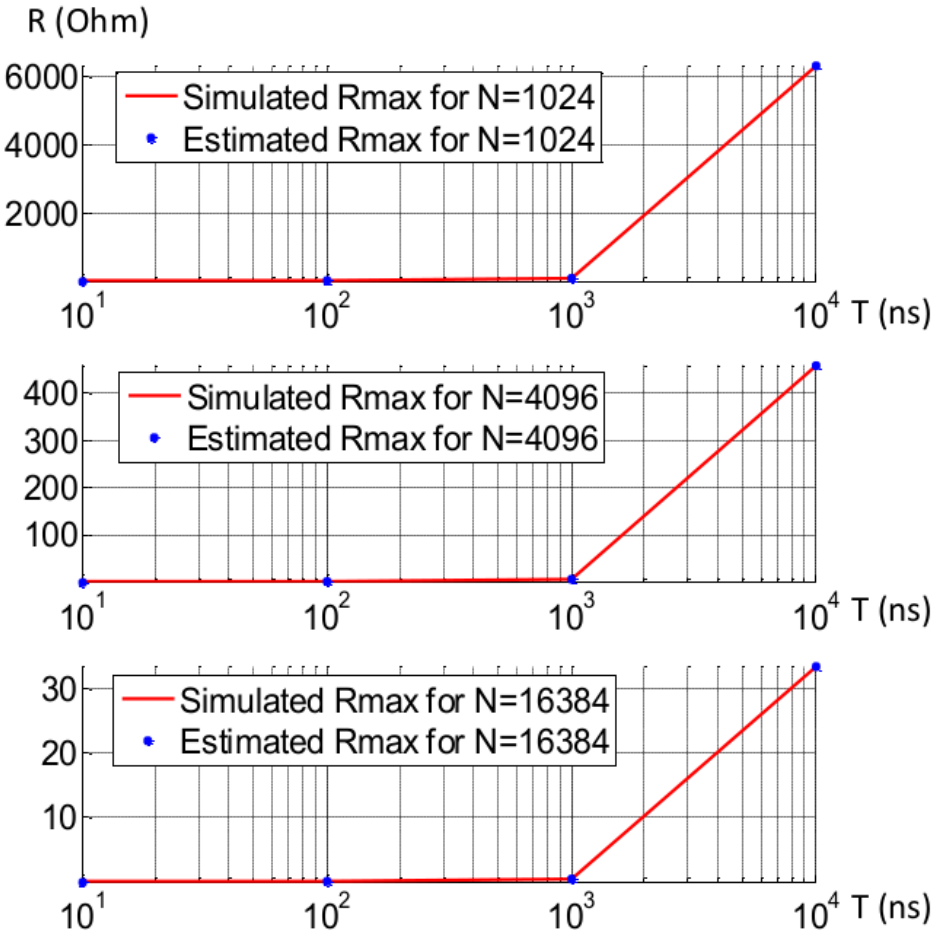

Figure 3.13 – Maximum PCN resistance as a function of the ramp time. Comparison between analytical model versus the simulation results.

In Fig.3.13, we present the simulation results of R_{max} as a function of the ramp time for different pipeline sizes and also R_{max} from our analytical model. The percentage of difference between simulation and model results are shown in Table 3.3.

As the mean error is 2.96% for a ramp time of $10ns$, we can conclude that the R_{max} model still fits simulations for long-size pipelines.

Table 3.3 – PERCENTAGE OF DIFFERENCE BETWEEN THE ELECTRICAL SIMULATION R_{max} AND THE ANALYTICAL MODEL FOR REAL-CASE APPLICATION

	Ramp Time, T (ns)			
N	10	100	1000	10k
1024-stage	1.86%	0.41%	0.37%	0.48%
4096-stage	2.55%	0.85%	0.17%	0.22%
16384-stage	2.96%	1.55%	0.46%	0.30%

In order to determine the accuracy of C_{max} model, we study the same pipeline sizes as we do for R_{max} model and we choose a PCN resistance of $10m\Omega$.

In Fig.3.14, we present the simulation results of C_{max} as a function of the ramp time for different pipeline sizes and also C_{max} from our analytical model. The percentage difference between simulation and model results are shown in Table 3.4. There is no error percentage for a 16384-pipeline C_{max} at $10ns$ as the maximum PCN resistance is $3.8m\Omega$.

Table 3.4 – PERCENTAGE OF DIFFERENCE BETWEEN THE ELECTRICAL SIMULATION C_{max} AND THE ANALYTICAL MODEL FOR REAL-CASE APPLICATION

	Ramp Time, T(ns)			
{N-stage,R(Ω)}	10	100	1000	10k
{1024, $10m\Omega$}	1.45%	0.84%	0.34%	0.28%
{4096, $10m\Omega$}	1.65%	0.33%	0.27%	0.56%
{16384, $10m\Omega$}	//	0.66%	0.54%	0.66%

As the mean error is 1.65% for a ramp time of $10ns$, we can conclude that the C_{max} model is relevant for long-size pipelines.

To summarize, the analytical model can be developed for short-size pipeline. The model stays accurate for any pipeline-size.

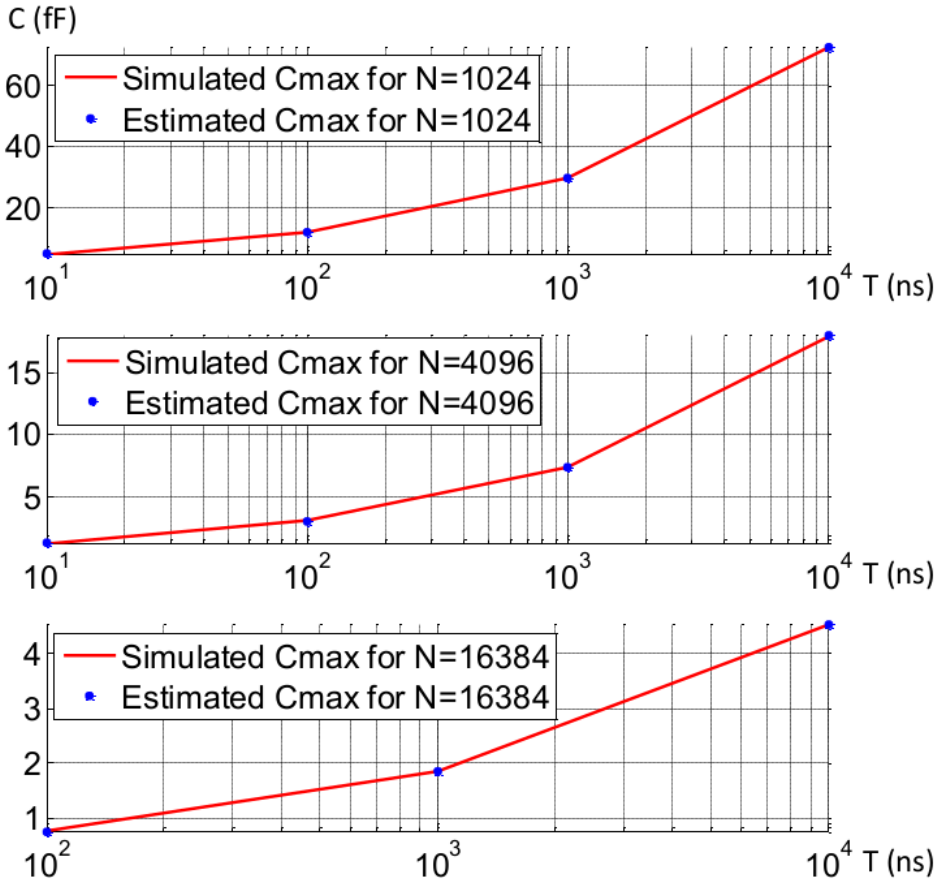

Figure 3.14 – Maximum PCN capacitance as a function of the ramp time. Comparison between analytical model versus the simulation results.

Power-Clock Grid Area

In this section, we present how the power-clock grid area and the energy dissipation are related. A power-clock grid can be divided on several branches. PCN resistance and capacitance are the parasitics of these power-clock branches. We can estimate the value of the parasitics with the metrics of the branches. Hence, in order to meet the requirements provided by R_{max} and C_{max}, we may have to resize the power-grid branches, what changes the total power-clock grid area.

The PCN resistance is expressed as:

$$R_{PCN} = \frac{\rho L}{W t} \tag{3.28}$$

where ρ is the resistivity of copper, L, W and t respectively the length, the width and the thickness of the branch.

In [74], the PCN capacitance is expressed as:

$$C_{PCN} = \epsilon\{\frac{W}{H} + 2.22\frac{S}{S+0.70H}^{3.19} + 1.17\frac{S}{S+1.51H}^{0.76}\frac{t}{t+4.53H}^{0.12}\} \tag{3.29}$$

where ϵ is the air permittivity, S the spacing between two branches and H the distance from ground. Note that we neglect the coupling capacitance.

The spacing is expressed as:

$$S = \frac{W_{tot} - kW}{k} \tag{3.30}$$

where W_{tot} is the total width of the power-clock grid and k the number of tracks.

In Eq.(3.28) and Eq.(3.29), the two only parameters we can change are the width and thickness of the branch. Indeed, ρ and ϵ are material-dependent, the length, distance from the ground are fixed by the circuit and the spacing is a function of the width. If we increase the width of a power-clock branch, it will decrease the PCN resistance and increase the PCN capacitance. If we increase the thickness of a power-clock branch, it will decrease the PCN resistance and have almost no effect on the PCN capacitance. Thus, if the PCN resistance is too high, we will increase the width of the power-clock branch then if the PCN capacitance is too high, we will decrease the width of the power-clock branch and if the PCN resistance is too high again, we will increase the thickness of the PCN branch.

From a power-grid area point of view, if we have to resize a power-clock grid, we may save some areas. In the case of a too large PCN capacitance, we will decrease the width of the power-clock grid and we may increase the thickness, which does not impact the power-grid area. On the other hand, if the PCN resistance is too large, we will increase the width of the power-clock grid and thus, increase the total area.

3.5.2 Design Guideline

In this subsection, we explain our algorithm by applying our analytical models to determine R_{MAX} and C_{MAX} as a design guideline for our PCN network for different circuits and then we will resize the power-clock grid (if needed). The objective is to determine the maximum PCN parasitics for a circuit benchmark with 1024-stage PFAL pipeline implemented in 45nm CMOS technology node, with operating frequency at 50MHz or ramp time of 10ns.

We follow the steps of the A$lgorithm$ 1. In the first step, we determine the parasitic PCN resistance of a power-clock branch; R_{PCN} which is derived using Eq.(3.28).

For our example, the power-clock grid is 1µm by 1µm. The thickness is 1µ and the distance from ground is 1µm. The power-clock grid has 5 horizontal and vertical tracks, i.e track has

Algorithm 1 Determination of R_{PCN} and C_{PCN} with respect to N and T

Require: N, T, W, L, t, k, S
  $R_{PCN} \leftarrow f(W, t)$ Eq.3.28
  $R_{MAX} \leftarrow f(N, T)$ Eq.3.22
  while $R_{PCN} > R_{MAX}$ **do**
    $W \leftarrow 1.1W$
    $R_{PCN} \leftarrow f(W, t)$ Eq.3.28
  end while
  $C_{MAX} \leftarrow f(N, T, R_{PCN})$ Eq.3.27
  $C_{PCN} \leftarrow f(W, t, S)$ Eq.3.29
  while $C_{PCN} > C_{MAX}$ **do**
    $W \leftarrow 0.9W$
    $R_{PCN} \leftarrow f(W, t)$ Eq.3.28
    if $R_{PCN} > R_{MAX}$ **then**
      while $R_{PCN} > R_{MAX}$ **do**
        $t \leftarrow 1.1t$
        $R_{PCN} \leftarrow f(W, t)$ Eq.3.28
      end while
    end if
    $C_{PCN} \leftarrow f(W, t, S)$ Eq.3.29
    $C_{MAX} \leftarrow f(N, T, R_{PCN})$ Eq.3.27
    if $C_{PCN} < C_{MAX}$ **then**
      break
    end if
  end while
  $W_{TOT} \leftarrow f(W, k, s)$ Eq.3.30
  $area \leftarrow W_{TOT} L$

a width of $0.1\mu m$, length of $1\mu m$, spacing of $0.1\mu m$, thickness of $1\mu m$ and distance from ground of $1\mu m$. Each interconnection between tracks makes a branch, thus there are 4 branches per track giving a total of 100 branches. Each branch has a width of $0.1\mu m$, a length of $0.2\mu m$, a spacing of $0.1\mu m$, a thickness of $1\mu m$ and a distance from ground of $1\mu m$. Using Eq.(3.28), we estimate the value of R_{PCN} as $43.8m\Omega$.

The second step is to determine R_{max}. We derive the parameters needed for Eq.(3.22) by performing simulations of a N-stage pipeline with a resistive PCN only, e.g. N = 48, with ramp times varying from $1ns$ to $1\mu s$. Once all the parameters are known, we check if R is lower than R_{max} at the selected ramp time. In our example,the value of R_{MAX} is evaluated as $699m\Omega$ (Table 3.5) which is higher than the resistance of a PCN branch. If we need

to lower the PCN resistance, we would go to the third step and increase the width of the power-grid.

The forth step is to evaluate C_{PCN} using Eq.(3.29). In our example, the PCN capacitance is estimated as $193aF$. The fifth step is to determine C_{MAX} using Eq.(3.27). The value of C_{MAX} is evaluated as $4900aF$ (Table 3.5) which is higher than the capacitance of a PCN branch.

If the PCN capacitance is higher than C_{MAX}, the last step is to decrease the width of the power-grid and then to evaluate the new R_{PCN}. If R_{PCN} is higher than R_{MAX}, we will increase the thickness and then evaluate C_{MAX} again. In our example, the resizing is not needed, thus, the energy dissipation from the power-clock grid is less than the 5% energy tolerance we have chosen.

For our second example, we use the same power grid configuration but the circuit is now composed of 16384 gates. As we do for our first example, we determine the value of R_{MAX} which is $25.8m\Omega$ (Table3.5). As R_{PCN} is higher than R_{MAX}, we have to increase the width of the power-clock branch. To fit R_{MAX}, we choose a new width of $0.2um$, thus the value of R_{PCN} is now $22m\Omega$ (Table3.5). The next step is to evaluate C_{PCN} using Eq.(3.29) and C_{MAX} using Eq.(3.27). The values of C_{PCN} and C_{MAX} are respectively $281aF$ and $433aF$. Thus, C_{PCN} is lower than C_{MAX}.

The last step is to calculate the new power grid area due to the resizing. Using Eq.(3.30), we evaluate the total width and then we evaluate the new area. In our example, the total width is now $1.5um$ which means that the new area is $1.5um^2$. In order to meet our energy dissipation conditions, we have to increase the total area by 1.5.

To conclude, we succeeded in determining the maximum PCN interconnect parasitic resistance and capacitance for an N-stage adiabatic pipeline and ramp time. We are able to resize the power-grid in order to keep the energy dissipation into our requirements.

Table 3.5 – DETERMINATION OF R_{max} AND C_{max}

Number of gates	Ramp time (ns)	R($m\Omega$)	C(aF)	R_{MAX}($m\Omega$)	C_{MAX}(aF)	Area increase
1024	10	44	193	699	4900	1X
16384	10	44	193	25.8	/	1X
16384	10	22	281	25.8	433	1.5X

3.5.3 Conclusion

In this section, we study the impact of power-clock networks (PCNs) on the energy dissipation of an adiabatic circuit. Then, we propose a design guideline to optimize the power-

clock networks of an N-stage adiabatic pipeline designed in 45nm technology node using sinusoidal power supplies. An adiabatic pipeline can dissipate 21 times less energy per cycle than a conventional pipeline at an optimal frequency. Nonetheless, if power clock networks are not optimized, the PCN parasitic will hamper this savings and moreover decrease the optimal frequency. Hence, we derive the PCN interconnect parasitic resistance R_{max} and capacitance C_{max} such that the energy dissipation per cycle due to PCN is constrained within 5%.

We model R_{max} as a function of the ramp time, T and the number of gates, N. Then C_{max} is determined based on PCN parasitic resistance R_{max}, T and N. By deriving R_{max} and C_{max}, designers can derive the optimal size of the PCN interconnect branches and the overall size of the PCN network that induces minimal energy dissipation within 5%. Then we link the R_{max} and C_{max} values to the parasitic of the power-clock grid. This relation shows that by resizing the power-clock grid we can limit the energy dissipation due to PCN within 5% but we could increase the total power-clock grid area.

3.6 Chapter conclusion

In this chapter, we present the power-clock network, PCN, which is power delivery network and a clock distribution network. Thus, the power-clock network faces the same issue as a power delivery network and a clock distribution network. We need to pay attention to the delay introduced by the PCN parasitic, the IR drop, which occurs during the hold phase of the power-clock signal and the potential power-clock noises. However, the main goal of this chapter is to optimize the PCN in order to limit the overall energy dissipation.

To do so, we study the impact of PCN on a single gate energy dissipation. We model the energy dissipation of a single gate with respect to the gate own resistance and capacitance, the PCN resistance and the operating frequency. Thanks to this model, we define three constraint on the PCN resistance: R_5, R_{999} and R_{CRIT}. R_5 is the maximum PCN resistance value, which ensures that the additional dissipation is less than 5% of the overall energy dissipation. Then, R_{999} is the maximum PCN resistance value, where the load capacitance is fully charged. Similarly, R_{CRIT} is the maximum PCN resistance value, which ensures that the adiabatic gate dissipates less energy than the digital logic gate.

We also demonstrate that we can still use the well-known equation $E_{AL} = 2\frac{RC}{T}CV_{DD}^2$ where the resistance is the sum of the gate own resistance and the PCN one.

Then, we study the impact of PCN on multi-gate energy dissipation. We perform several simulations in order to quantify the impact and then we propose a design guideline in order to optimize the power-clock networks. As a function of the tolerable energy dissipation, we can evaluate the maximum PCN resistance as a function of the number of gates and the

operating frequency. Then, we can also evaluate the maximum PCN capacitance as a function of the number of gates, the operating frequency and the actual PCN resistance.

We base our guideline on these evaluations. If the PCN resistance or capacitance are too large, then we propose a way to resize the power-grid to meet the requirement.

CHAPTER

4 Study of the Power-Clock Supply

In this chapter, we investigate the power-clock supply impact on adiabatic logic. The chapter is organized as follows: in Section 4.1, we define how a power-clock supply operates and present the state of the art. Then, in Section 4.2, we present a power-clock supply in order to drive gates at their optimal V_{DD}. In Section 4.3, we propose another power-clock supply in order to drive gates at nominal V_{DD}. Finally, in Section 4.4, we conclude the chapter.

4.1 Definition of Power-Clock Supply

The aim of the power-clock supply is to deliver a 4-phase signal. During the hold and waiting phase, the supply acts as a DC-DC converter, which delivers V_{DD} and V_{SS}, respectively. During the evaluation and the recovery phase, the power-clock supply acts as a DC-AC converter, which charges and discharges the gates.

There are two main topology families, which are represented in Fig.4.1: capacitive-based and inductive-based power-clock supply [75].

Capacitive-based topologies (Fig.4.1.a) simulates a ramp during the evaluation and recovery phases by connecting and disconnecting several tank capacitors. It is a switch capacitor converter [76], where each tank capacitor is charged under the same voltage V_{TANK}, which is defined as:

$$V_{TANK} = \frac{V_{DD}}{N} \tag{4.1}$$

where V_{DD} is the maximum voltage and N the number of tank capacitors.

Each time we connect (or disconnect) a tank capacitor, we increase (respectively decrease) the power clock voltage by V_{TANK}. Thus, at each connection, we can model the energy dissipation due to the gap E_{DISS} as:

$$E_{DISS} = \underbrace{CV_{NEXT}(V_{NEXT} - V_{PREV})}_{\text{Delivered energy}} - \underbrace{\frac{1}{2}C(V_{NEXT}^2 - V_{PREV}^2)}_{\text{Stored energy}} \tag{4.2}$$

where V_{NEXT} is the voltage after the connection of a new switch and V_{PREV} is the voltage before the connection of a new switch, which are represented in Fig.4.1.b.

Using (4.1) and (4.2), we can determine the overall energy loss due to each gap E_{GAP} as:

$$E_{GAP} = \frac{1}{2N}CV_{DD}^2 \tag{4.3}$$

The number of tank capacitor is a function of the leakage of the switches, E_{GAP}, and the switching dissipation. [77] shows that for a CMOS 180nm capacitive power-supply, the optimal number of tank capacitors is 3.

During the Hold phase, all the tank capacitors are connected to ensure that the power-clock voltage remains at V_{DD}. During the Waiting phase, the gates are connected to the ground. The power-clock signal waveform is shown in Fig.4.1.b.

In order to connect the switches and change the states, a capacitive based power-clock supply needs N+1 control signals. The synchronization between the 4 different capacitive power-clock supplies can be done by synchronizing the control signals.

In [78], an improvement of this type of power-clock supply has been made. With only 3 tank capacitors, this work presents a 6-step switched capacitor converter. It means that with the same leakage dissipation, this power-supply dissipates half E_{GAP} (4.3).

The objective of the inductive based power-clock supplies is to make a resonance between the load capacitance (i.e. the gates) and an inductor during the evaluation and recovery phases similarly to the design for resonant clock [79]. A topology is shown in Fig.4.1.c. When the power-clock signal has to remain constant, during the hold and waiting phases, gates are directly connected to V_{DD} or V_{SS} through a switch.

A power-clock signal waveform is shown in Fig.4.1.d. Unlike capacitive based power-clock supplies, inductive based power clock supplies charge and discharge the gates with a sinusoidal signal. A sinusoidal signal multiplies the adiabatic dissipation by a factor of $\frac{\pi^2}{8}$.

Another main difference with capacitive power-clock supplies is the way the synchronization is handled. In order to limit the energy dissipation from the inductive power-clock supply, a change of phase has to be done when the inductor has stored zero energy, i.e. we need to do a zero-current switching. As we use different inductances, there is a chance that

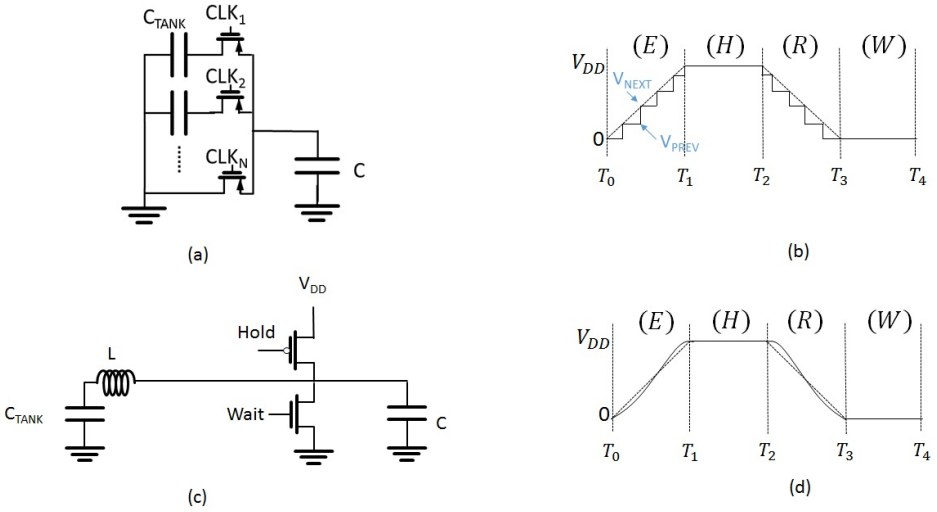

Figure 4.1 – (a) Capacitive based power-clock supply, (b) ideal capacitive based power-clock signal waveform, (c) inductive based power-clock supply, (d) ideal inductive based power-clock signal waveform.

they will be a mismatch. Thus, if we handle the synchronization via the control signals, we could not use the zero-current switching method. A way to handle the synchronization is to add a switch to disconnect the inductor. This solution has two drawbacks:

— It adds a resistance in the power path, which decreases the quality factor of the LC filter and increases the energy dissipation.

— an additional control signal is needed.

An inductive based power-clock network needs 2 control signals or 3 if we synchronize the 4 power-clock supplies with an additional switch.

For the rest of the chapter, we study the inductive based power-clock supplies only. We choose this solution because it has less control signals, less transistors and less components. On the other hand, the gates dissipate more energy.

4.2 Proposed Topology at Optimal V_{DD}

In this section, we propose and optimize a topology in order to drive PFAL gates at optimal V_{DD}, i.e. 0.5V for CMOS 45nm. The section is organized as follows: first, we propose a topology, then we explain the roles of the control signals. In addition, we validate our model with experiments and finally we conclude the section.

4.2.1 Topology

The topology is described in Fig.4.2. There are three switches (i.e. two PMOS and one NMOS transistors) and an inductor. The idea behind this topology is to make the equivalent gate capacitances resonate with the inductor as an LC filter. The value of C_{TANK} is chosen such as $C_{TANK} >> N.C_{GATE}$, thus it can be modeled as a dc voltage supply, which provides $V_{IN} = \frac{V_{DD}}{2}$. During the evaluation (Fig.4.2.a) and the recovery phases (Fig.4.2.e), the CTRL transistor is closed while the Hold and Wait transistors are open. During these phases, the resonance occurs and the circuit can be modeled as shown in Fig.4.2.b. R_s is the equivalent resistance of the CTRL switch and the series resistance of the inductor. R_{on} and C_l are the equivalent resistance and capacitance of a buffer gate, where N is the number of gates.

From the circuit model, we can determine the size of the inductor as a function of the running frequency and equivalent circuit capacitance as:

$$L = \frac{1}{4\pi^2 f N C_l} = \frac{T}{\pi^2 N C_l} \quad if\ Q > 10 \tag{4.4}$$

where Q is the quality factor of the circuit model.

During the hold phase (Fig.4.2.c), the CTRL and Wait switches are open, and the Hold switch is closed. Thus, the power-clock signal stays at V_{DD}. During the waiting phase (Fig.4.2.g), the CTRL and Hold switches are open while the Wait switch is closed. Thus, the power-clock stays at V_{SS}.

One can also think of a topology without the CTRL power switch to reduce the series resistance and increase the quality factor for the resonance. However, this switch must be kept to short circuit the inductance during the hold and waiting phases in order to avoid the charge of the inductance, which leads to a faster charge or discharge of the capacitor.

In order to size the transistors, we have to set up constraints on the maximum ON resistance. We can derive the maximum serial resistance R_s^{max} with respect to the quality factor Q of the LC filter as:

$$R_s^{max} = \frac{1}{2\pi f Q N C_l} - \frac{R_{on}}{N} \quad with\ Q = 10 \tag{4.5}$$

90% of R_s^{max} is allocated to the maximum CTRL switch resistance R_{ctrl}^{max} and the remaining 10% to the maximum equivalent serial resistance ESR^{max} of the inductor. We choose such repartition to limit the switching energy loss due to the gate capacitance of the CTRL switch.

Then, the Hold switch resistance is sized with respect to the leakage current occurring

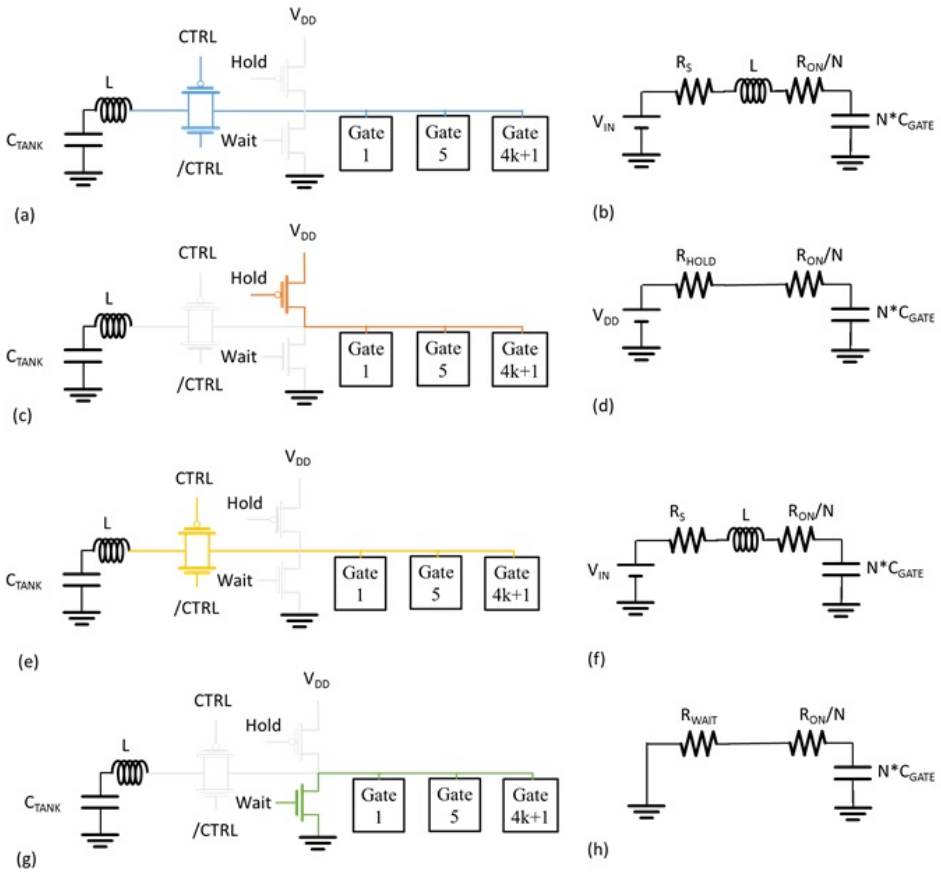

Figure 4.2 – (a) The power-clock supply with the control switches and (b) model of the circuit during the evaluation phase. (c) The power-clock supply with the active control switches during the hold phase and (d) its circuit model. (e) The power-clock supply with the active control switches during the recovery phase and (f) its circuit model. (g) The power-clock supply with the active control switches during the waiting phase and (h) its circuit model.

during the hold phase. We decide that the power-clock signal should be at least at 95% of V_{DD}. Thus, the maximum hold resistance R_{hold}^{max} is defined as:

$$R_{hold}^{max} = \frac{0.95V_{DD}}{I_{leakage}} \tag{4.6}$$

where $I_{leakage}$ is the leakage current during the hold phase.

We do not need to set any constraint for the wait switch resistance as there is no current during the waiting phase. Hence, there is no energy dissipation but leakage.

4.2.2 Synchronized Control Signals

Control signals have two purposes: 1) ensure that the power-clock supply is in the correct phase and 2) that the phase shift between two following power-clock signals is 90°.

Each power-clock supply has three control signals in order to drive the three power switches. These control signals are a function of a clock and the power-clock signal. The clock has a frequency of 2T.

The evaluation phase starts when the previous state of the power-clock is the waiting phase, and there is a falling edge on the clock. During this state, the CTRL and Wait signals are at V_{SS} while the Hold signal is at V_{DD}. The evaluation phase ends when the clock has a rising edge, or the power-clock signal reaches V_{DD}.

After the evaluation phase, there is the hold phase. During this state, the CTRL signal is at V_{DD} while the Hold and Wait signals are at V_{SS}. The hold phase ends when the clock has a falling edge.

Then, there is the recovery phase. During this state, the CTRL and Wait signals are at V_{SS} while the Hold signal is at V_{DD}. The recovery phase ends when the clock has a rising edge, or the power-clock signal reaches V_{SS}.

The fourth and last phase is the waiting phase. During this state, the CTRL, Hold and Wait signals are at V_{DD}. The hold phase ends when the clock has a falling edge.

An example of how the synchronized control signals work is shown in Fig.4.4.

In order to ensure the phase shift, clocks from two following power-clock supplies have a 90° phase shift, which is shown in Fig.4.5.

4.2.3 Simulations

In this subsection, we perform simulations on adiabatic logic circuits to show how the resonant power-clock supply works and its energy efficiency. For our simulation, we use a 4-stage PFAL pipeline circuit implemented in 45nm CMOS technology node. The benchmark is shown in Fig.4.3.

Validation

Experiments show that the optimal running frequency for 4-stage PFAL pipeline in the 45nm technology node is around 5MHz -if we use Bennet clocking, there are still 4 power-clocks but the running frequency will be 1MHz only with a supply voltage V_{dd} at 0.5V in order to dissipate the smallest amount possible of energy. At this frequency, there is the optimal trade-off between the leakage from the CMOS gates and the adiabatic losses. As a PFAL buffer has an equivalent capacitance of 700fF, we can find the size of the inductors using (4.4). Then, we use 12 different control signals (i.e. three signals CTRL, Hold, and

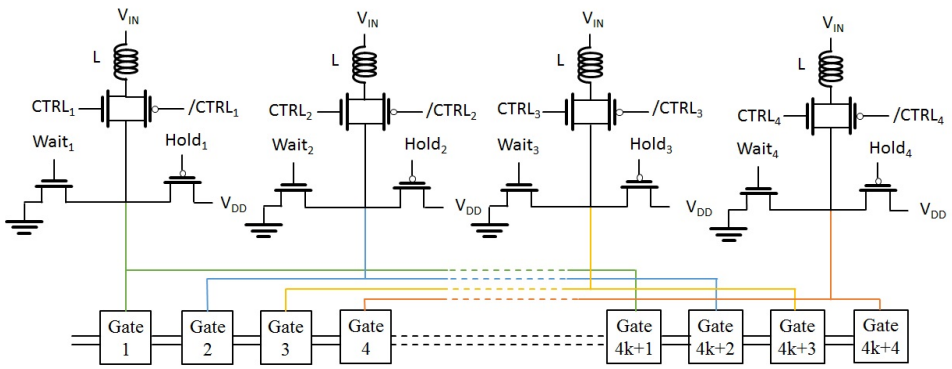

Figure 4.3 – Illustration of a N(4k+4)-stage PFAL pipeline and its four power-clock supplies.

Wait for each power-clock supply) - one signal per power switch. Please note that there are four power-clock supplies used in the PFAL pipeline.

In Table 4.1, we present the values of resistance and inductance required to size the power-clock supplies. Please note that these values are dependent on the number of gates and power-clock supplies. To find the actual passive R and L values, we need to divide the values in the table by the number of gates.

Table 4.1 – PASSIVE FOR POWER-CLOCK SUPPLY OF A 45NM PIPELINE

Passives	Number of Gates	L(mH)	ESR^{max}($k\Omega$)	R$^{max}_{ctrl}$($k\Omega$)	R$^{max}_{hold}$(MΩ)
Values	1	1440	455	4090	65800
	10000	0.144	0.0455	0.409	6.58

In Fig.4.3, the first power-clock supply and its control signals are shown. During the evaluation phase, power-clock signal never reaches V_{DD}. Thus, the transition between the evaluation and hold phase is done by using the control clock. Then, the transition between the recovery and waiting phase is done when the power-clock signal reaches V_{SS}.

In Fig.4.4, power-clock supply, input and output signals are shown. We notice that during the evaluation phase some glitch occurs. They increase overall energy dissipation during the transition from evaluation to hold phase. There is an exponential energy dissipation increase because the power-clock supply is not at V_{DD}, what deteriorates the overall adiabatic energy savings.

This glitch occurs due to non-ideal transistors between the inductance and capacitance, which changes the quality factor of the resonant power-clock supply. Thus, power-clock

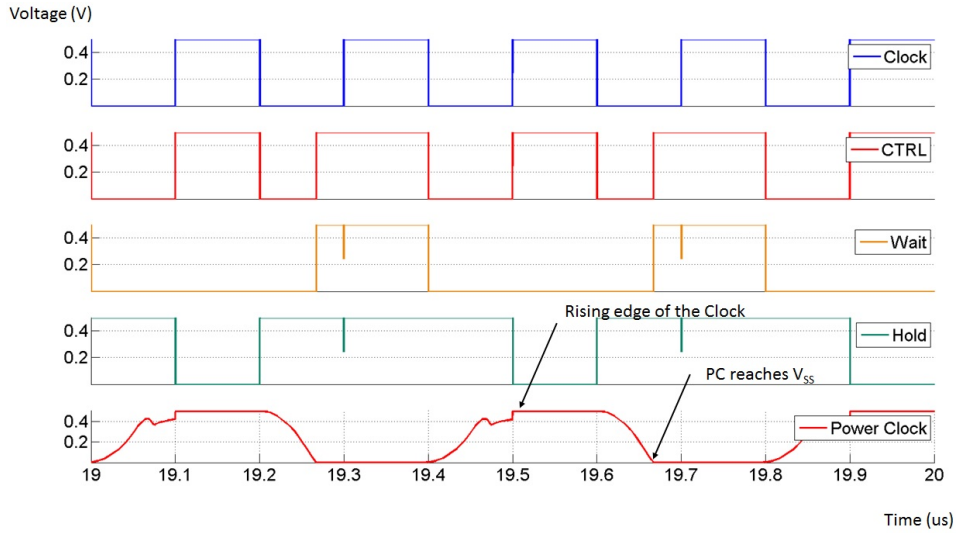

Figure 4.4 – Simulation waveforms of the power-clock signal and its control signals.

Table 4.2 – ENERGY DISSIPATION FOR ADIABATIC PIPELINE WITH DIFFERENT TOPOLOGIES

Circuit	Energy Dissipation (aJ)	Energy Gain (X)
Non-adiabatic CMOS pipeline with ideal power supply	492	1X
Adiabatic PFAL pipeline with ideal power-clock supply	20	25X
Adiabatic PFAL pipeline with proposed power-clock supply	167	2.9X
Adiabatic PFAL pipeline with proposed power-clock supply without direct charging	56	8.8X

supply, which is initially in a pseudo-periodic mode diverts in an aperiodic mode and explains the occurrence of glitches. A more detailed explanation is shown in 4.3.1.

Power-clock signals have the correct phase shift thanks to the different clocks. We also observe glitches in the output signals, which arise from the non-idealities of the CMOS transistor of the PFAL gates. During the recovery phase, when the power-clock signal reaches the threshold voltage of the PMOS transistor, the voltage between the gate and the source

of the PMOS at the PFAL buffer is too low to keep the switch open. Thus, the output signal stays at the threshold voltage minus the leakage of the PMOS transistor until the evaluation phase. At the end of this phase, there is an exponential charge of the load capacitance. Its dissipation known as direct charging is defined as:

$$E_{charging} = \frac{1}{2} C_{Load} (V_{DD}^2 - V_{EV}^2) \tag{4.7}$$

where V_{EV} is the power-clock voltage at the end of evaluation phase.

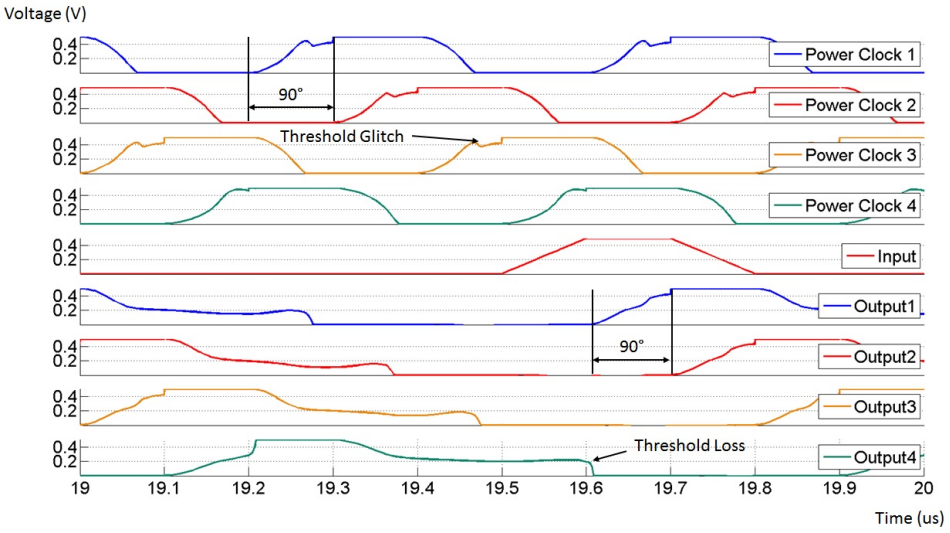

Figure 4.5 – Simulation waveforms of a 4-stage PFAL pipeline and its power-clock supplies.

Finally, we derive the energy consumption of the power-clock supply. We focus our study on a single power-clock supply as they have the same load and power consumption. We choose to study the third power-clock supply.

The power-clock supply dissipates 41.8aJ where 2% comes from the switching losses, 30% from the resonance and 68% from the direct load charging. Most of the dissipation comes from the direct load charging, which is defined in (4.7).

In order to quantify the energy gain of our proposed power-clock supply, we quantify the energy dissipations: 1) of a non-adiabatic CMOS pipeline using an ideal power supply, 2) an adiabatic pipeline supplied by an ideal power-clock, and 3) an adiabatic pipeline supplied by our proposed topology with and without direct charging. The last column represents the potential energy gain between the different topologies and a non-adiabatic CMOS pipeline. The results are shown in Table 4.2.

A non-adiabatic CMOS pipeline dissipates 492aJ per operation while an adiabatic pipeline dissipates 20aJ per operation. There is a potential 25X energy gain to use an adiabatic pipeline, i.e. the adiabatic pipeline dissipates 25 times less energy than a non-adiabatic CMOS pipeline.

Despite the threshold effect, which implies direct charging losses, an adiabatic PFAL pipeline with the proposed power-clock supply still dissipates 2.9 times less energy than a conventional CMOS pipeline.

As most of the energy dissipation of the power-clock supply comes from the direct charging losses, we could regulate V_{DD} in order to avoid such losses. This regulation will make the control part dissipate more energy, but we make the assumption that the power supply will drive thousands of gates and the impact of the control on the overall energy dissipation is negligible. As a result, the adiabatic PFAL pipeline will dissipate 8.8 times less energy than a conventional CMOS pipeline.

The difference between the energy gain from an ideal adiabatic pipeline and the adiabatic pipeline supplied by our proposed topology is due to the $threshold\ voltage$ of the CMOS transistors. Indeed, the threshold voltage has two main effects on the energy dissipation:

— The load capacitance cannot fully discharge during the recovery phase, and the remaining energy is discharged to the ground (threshold losses).

— There is a direct charging loss at the end of the evaluation because the power-clock signal cannot reach V_{DD} (threshold glitch).

The prospect of novel devices in adiabatic logic, such as nano-electro-mechanical switches (NEMS), carbon nanotube based field effect transistors (CNTFETs) or vertical-slit field effect transistors (VESFETs), should significantly increase the energy efficiency gain of the adiabatic logic and the proposed power-clock supply topology. Indeed, these novel devices have much lower threshold voltage compared to CMOS. Thus, the adiabatic logic will gain energy efficiency by lowering the threshold loss dissipation and the proposed power-clock topology will dissipate less energy without the threshold glitch.

Synchronization

In order to show that the proposed topology still works with unmatched inductances, we used the test bench presented in Fig.4.3 with different inductance values of 0.95L, 1.05L, 1.1L and 0.9L respectively in the 4 power-clock supplies.

In Fig.4.6, one of the power-clock supplies and its control signals are shown. The main difference with the case of ideal matched inductance is that the power-clock voltage level at the end of the evaluation phase is not the same. Thus, the unmatched inductance will increase the energy dissipation but the circuit is still functional.

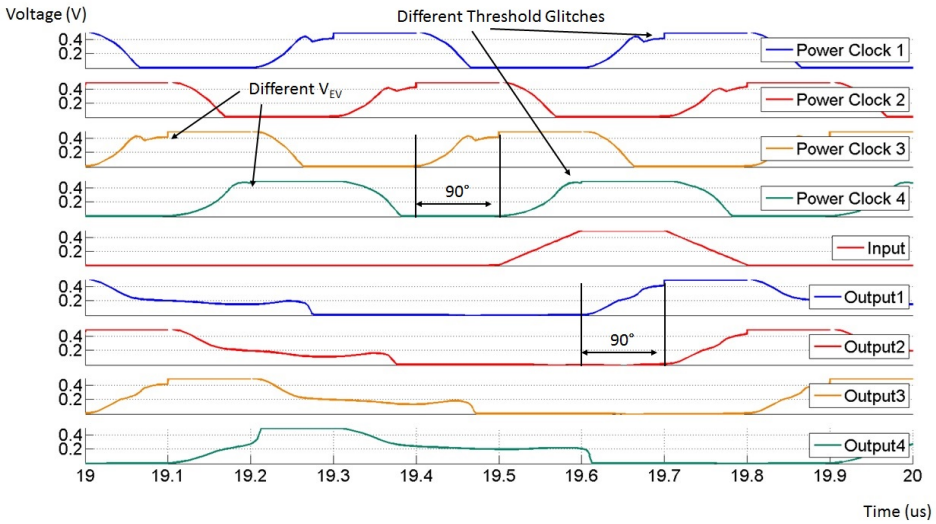

Figure 4.6 – Simulation waveforms of a 4-stage PFAL pipeline and associated power-clock supplies with unmatched inductances.

Table 4.3 – ENERGY DISSIPATIONS OF THE THIRD POWER-CLOCK SUPPLY WITH DIFFERENT INDUCTANCES

$\frac{L}{L_0}$	Switching Loss (aJ)	Resonant Loss (aJ)	Direct Charging Loss (aJ)	Total Energy Loss (aJ)	Energy Gain
1	0.8	12.4	27.8	167	2.9
1.1	0.8	12.4	29.7	172	2.9
2	0.8	12.4	50.6	255	1.9

In order to quantify the impact on the energy dissipation, we derive the energy dissipation of one of the power-clock supplies with an inductance value of 10% and 100% higher than the other inductances. The results are shown in Table 4.3.

We notice that the switching losses are not impacted by the size of the inductance. The transistors will switch the same number of times even if the resonance frequency is different from the expected one. Similarly, the unmatched inductances have no impact on the resonance loss. However, they have an impact on voltage signal at the end of the evaluation phase, V_{EV}. Large difference between the inductances of two following power-clock supplies induces a low voltage at the end of the evaluation phase. Thus, the direct charg-

ing loss increases and the energy efficiency decreases. Nevertheless, this topology does not need inductances to be matched in order to be functional.

4.2.4 Conclusion

In this section, we propose a resonant power-clock supply design for adiabatic logic. The design consists of one inductor and three switches. The resonance is established by exploiting the equivalent capacitance of the adiabatic logic and insertion of an inductor, thus creating an LC filter. We perform simulations on adiabatic PFAL pipelines supplied with the proposed resonant power-clock supplies. The results demonstrate the effectiveness of such topology and where the adiabatic pipeline dissipates 167 aJ per operation. An adiabatic PFAL pipeline supplied with the proposed topology will dissipate 2.9 times less energy per operation than a non-adiabatic pipeline. It can dissipate up to 8.8 times less energy if supply voltage V_{DD} is regulated in order to avoid any direct charging of the load capacitance.

The main advantage of this topology is that the four different inductances do not need to be matched. The synchronization of the power-clock signals will be ensured by the control signals.

The energy efficiency of adiabatic logic with the proposed power-clock supply topology will further increase using novel devices such as nano-electro-mechanical switches, carbon nanotube based field effect transistors or vertical-slit field effect transistors as the impact of the threshold voltage will be lowered or nullified.

4.3 Proposed Topology at Nominal V_{DD}

In this section, we propose a power-clock supply at nominal V_{DD}. We study it with 65nm CMOS technology as our design is taped-out with this technology node. In order to avoid the threshold glitch, we decide to work at nominal V_{DD}, i.e. 1.2V. The increase in energy dissipation coming from gates is counterbalanced by the suppression of the threshold glitch and the direct charging. The section is organized as follow: we explain why we need to work at nominal V_{DD}, then we propose a new topology. Finally, we optimize it with experimental simulations.

4.3.1 How to Suppress the Threshold Glitch

When we designed the LC oscillator at optimal V_{DD}, there is a glitch, which increases the adiabatic loss and also adds a direct charging loss. This glitch is coming from the variation of the gate resistance. Indeed, the resistance is varying as a function of the power-clock voltage (Fig.4.7).

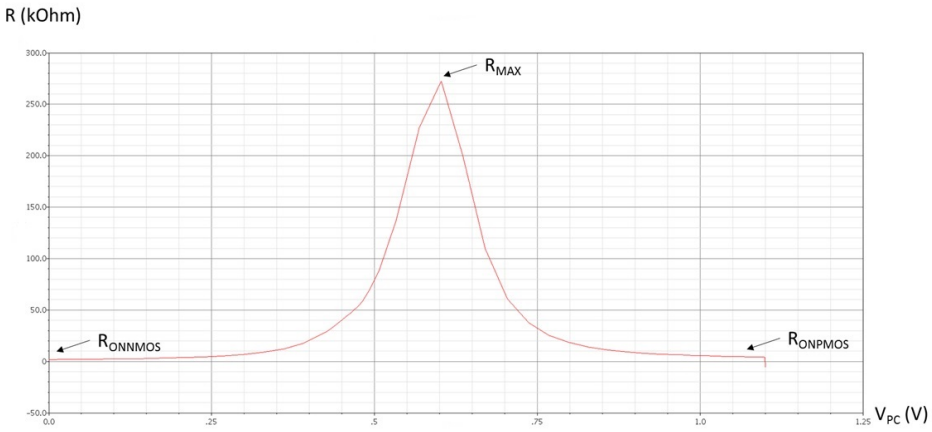

Figure 4.7 – Gate resistance as a function of the Power-Clock voltage.

When the power-clock voltage is between 0 and V_{THN}, the gate resistance can be modeled as the NMOS on-state resistance. At nominal V_{DD}, when the power-clock voltage is between $V_{DD} - V_{THP}$ and V_{DD}, the gate resistance can be modelled as the PMOS on-state resistance. Between V_{THN} and $\frac{V_{DD}}{2}$ there is an exponential increase of the gate resistance.

Finally, Between $\frac{V_{DD}}{2}$ and V_{THN} there is an exponential decrease of the gate resistance. We derive R_{MEAN} as the mean gate resistance during the evaluation phase. For nominal V_{DD}, R_{MEAN} is equal to R_{ON}, the on-state resistance of the CMOS (Fig.4.8).

As V_{DD} is decreasing, the maximum resistance is increasing (Fig.4.7). At optimal V_{DD}, R_{MEAN} differs from R_{ON} (Fig.4.8), it means that the quality factor of the oscillator is decreasing, which changes the RLC filter mode from pseudo-periodic to aperiodic. Thus, the way to avoid the glitch and the additional losses is to use the nominal V_{DD} value, i.e. 1.2V.

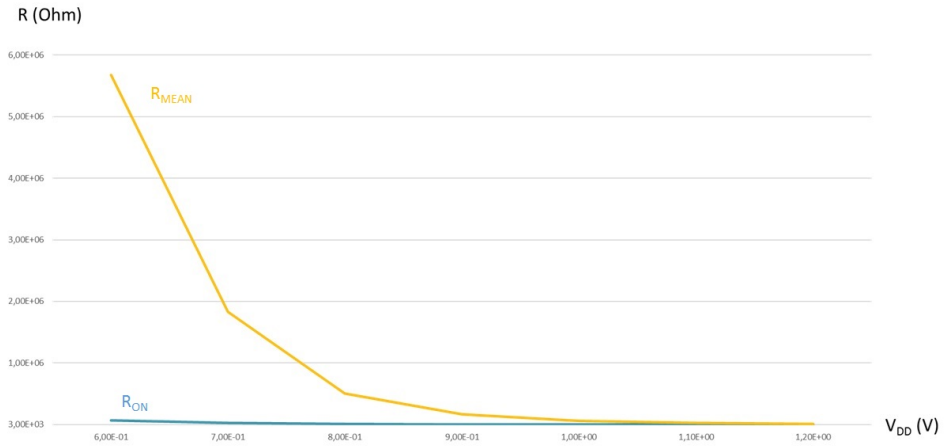

Figure 4.8 – R_{MEAN} and R_{ON} as a function of the maximum Power-Clock voltage.

4.3.2 Topology

The main difference with the topology from the previous section is that we now use a tank capacitor as V_{IN} supply in order to have a fully reversible power-clock supply. This tank capacitor is chosen to not disturb the frequency of the LC filter i.e., $C_{TANK} >> C_{LOAD}$. In practice, we choose a tank capacitor 1000 times higher than the load capacitance.

In order to disconnect the inductor during the hold and waiting phases, we can use a pass transistor between the tank capacitor and the inductor (a) or between the output and the tank capacitor (b). If we use the solution (a), there will be a resonance between the load capacitor, the oscillator and the pass transistor parasitic capacitor. If we use the solution (b), there will be a resonance between the tank capacitor, the oscillator and the pass transistor parasitic capacitor. Both oscillations dissipate additional energy. The difference between the solutions is that if we use solution (a), when we close the switch to be in evaluation or recovery phases, the energy stored in the parasitic capacitance is lost to the ground. If we use the solution (b), a significant part of the energy can be recovered to the tank capacitor. The other advantage to use the solution (b) is that this topology is more immune to the power noises. Indeed, if we sue the solution (a), there will be an oscillation during the hold phase due to the parasitic CMOS capacitance, which will increase the sensibility to the power noise.

In Fig.4.9, the proposed topology is shown. Besides the tank capacitor, the main difference with the previous topology is the position of the control switch and the fact that we have to use a pass transistor in order to have the full range of the power-clock signal. Thus, we need to have an additional control signal $\overline{CTRL}$, which is the complementary signal of CTRL.

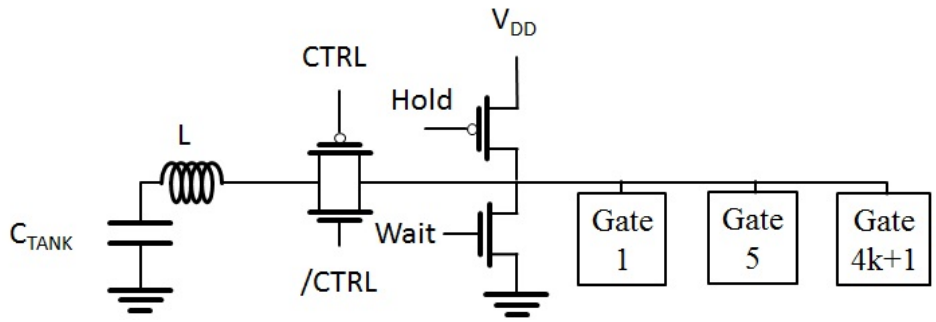

Figure 4.9 – Proposed topology for a power-clock supply at nominal V_{DD}.

4.3.3 Simulations and Optimization of the Topology

In this subsection, we perform simulations on adiabatic logic circuits to derive the optimal transistors width in order to have the highest energy efficiency. For our simulation, we employ a PFAL pipeline circuit implemented in 65nm CMOS technology node with 4 power-clok supplies. The benchmark is the same we used in the previous section and is shown in Fig.4.3.

In Fig.4.10, the first power-clock supply, its control signals, its zero current detection and the tank capacitor input voltage V_{IN} are shown.

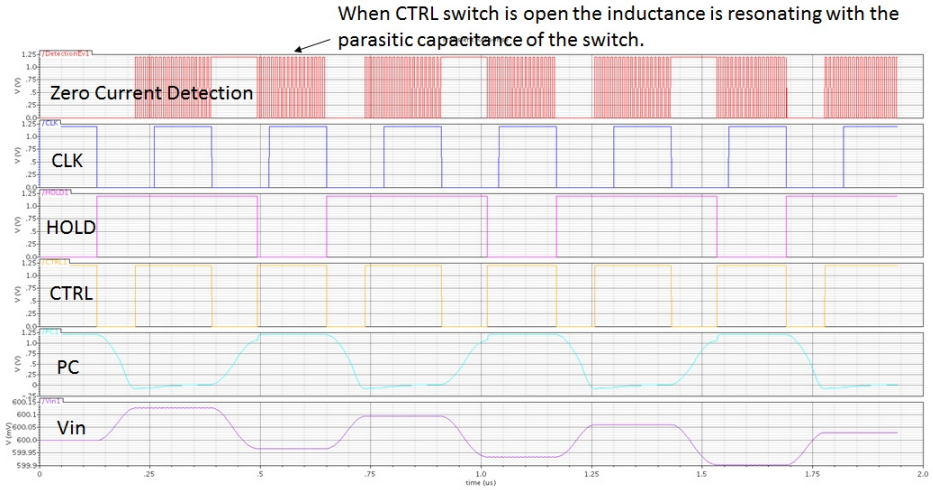

Figure 4.10 – Signal Waveform of a 65nm PFAL pipeline.

As in the previous topology, power-clock signal never reaches V_{DD}. However, the power-clock signal reaches its maximum when the zero current detection is triggered. It means,

there is still a direct charging dissipation with this topology but there will be no more lost energy in the inductance at the end of the evaluation, which will decrease the overall energy dissipation.

During the hold and waiting phases, there is a resonance between the CTRL pass transistor parasitic capacitance and the inductance, which triggers the zero-current detection. Thus, we enhance the control system in order to bypass the zero-current detection during the hold and waiting phases.

Another difference with the previous topology is that $V_{IN} \neq \frac{V_{DD}}{2}$. During the evaluation phase, V_{IN} is decreasing as the energy stored in the tank capacitance is charging the gate. Then, during the recovery phase, V_{IN} is increasing as the energy stored in the gate is being recovered. Still, the mean tank capacitance voltage is not $\frac{V_{DD}}{2}$ as $\bar{V_{IN}}$ is a function of the gate to charge but also the leakages. If the mean voltage is too low, then additional energy is given during the hold phase through the hold switch, then the mean voltage increases. Else, if the mean voltage is too high as it is the case in Fig.4.10, then less energy is given during the hold phase, thus the mean voltage decreases.

We perform several simulations in order to find the optimal width of the CTRL pass transistor in term of overall energy efficiency. There are 6 main dissipations, 1) the adiabatic dissipation, 2) the parasitic oscillation losses, which occur during the evaluation and the recovery phase, 3) the leakage during the hold phase, 4) the switching losses, which occur when the state of the transistors is changing, 5) the direct charging, which occurs at the end of the evaluation phase and 6) the threshold dissipation, which occurs during the recovery phase.

For the size of the tested load, i.e. from 1 to 50000 gates, increasing the width of the Wait NMOS or the Hold PMOS is decreasing the energy efficiency due to the increase in the switching losses so we decided to use the minimal width for these transistors.

In order to have the same resistance in the CTRL NMOS and PMOS, the width of the PMOS is 3 times higher than the width of the NMOS. In classical power supply optimization there is a trade-off between the resistive losses (here the adiabatic losses) and the switching losses. In our case, the switching losses are never predominant, thus the trade-off is between the adiabatic losses and the parasitic oscillation losses.

In Fig.4.11, the overall energy efficiency is shown as a function of the pass transistor width. When we increase the width, the resistance is decreasing and the parasitic capacitance is increasing. When the resistance decreases, the quality factor is increasing, which leads to a decrease in the adiabatic loss and an increase in the maximum power-clock voltage during the evaluation. It means that the direct charging losses are decreasing. One could think that we try to decrease the resistance in order to suppress the direct charging. However, the parasitic capacitance is increasing when the resistance decreases, what leads to higher parasitic oscillation losses and nullifies the gain due to less direct charging. As we can see

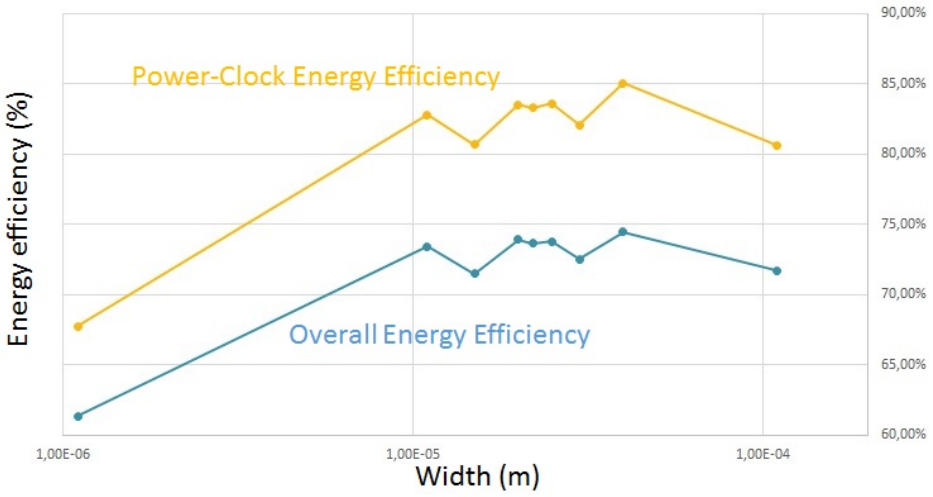

Figure 4.11 – Energy efficiency as a function of the width of the Pass transistor.

in Fig.4.11, the energy efficiency is increasing when the width increases until the parasitic oscillation losses become predominant.

We can model the energy efficiency as follow:

$$\eta = \eta_{PC} * \eta_{TH} \tag{4.8}$$

where η_{TH} is the energy efficiency with the threshold losses as the only energy dissipation and η_{PC} is the overall energy efficiency without the threshold losses.

In Fig.4.11, η_{PC} is shown as a function of the width. Without threshold losses, we theoretically achieve an energy efficiency of 85% instead of 74.8%. η_{TH} is architecture and technology dependent. For a 65nm PFAL logic gate, η_{TH} is 0.88. As we are using CMOS, we cannot have an energy efficiency higher than η_{TH} using (4.8). The threshold voltage has also an impact on η_{PC} as we choose the threshold voltage as a trade-off between the on-state CMOS resistance and the leakage.

In Table 4.4, we present the different CMOS width for our topology. We verify that the width is proportional to the number of gates by simulation. The difference between the width of CTRL NMOS and PMOS is due to the difference in the mobility of an electron in a NMOS and PMOS.

Table 4.4 – MOS WIDTH FOR POWER-CLOCK SUPPLY OF A 65NM PIPELINE

Number of Gates	CTRL NMOS (nm)	CTRL PMOS (nm)	WAIT NMOS (nm)	HOLD PMOS (nm)
10	200	600	W_{MIN}	W_{MIN}
10000	20000	60000	W_{MIN}	W_{MIN}

4.3.4 Discussion

In this subsection we discuss of the advantages and disadvantages of using the power-clock supply at nominal V_{DD} instead of using it at optimal V_{DD}.

Both topologies ensure the synchronization of the 4 power-clock supplies as they share the same control system.

In order to compare the energy gain of our two proposed topologies, we quantify the energy dissipations 1) of a non-adiabatic CMOS pipeline using an ideal power supply, 2) an adiabatic pipeline supplied by an ideal power-clock and 3) an adiabatic pipeline supplied by our proposed topology with and without direct charging. The last column presents the potential energy gain between the different topologies and a non-adiabatic CMOS pipeline. The results are show in Table 4.5.

Table 4.5 – ENERGY DISSIPATION FOR ADIABATIC PIPELINE WITH DIFFERENT TOPOLOGIES AT NOMINAL V_{DD}

Circuit	Energy Dissipation (aJ)	Energy Gain (X)
Non-adiabatic CMOS pipeline with ideal power supply	1400	1X
Adiabatic PFAL pipeline with ideal power-clock supply	161	8.69X
Adiabatic PFAL pipeline with proposed power-clock supply	433	3.23X

As the CMOS nodes are not the same, we cannot compare the energy dissipation directly so we choose to compare the energy gain. As intended, the energy gain from an adiabatic PFAL pipeline with ideal power clock supply is less with nominal V_{DD} than with optimal V_{DD}. Indeed, a 45nm-PFAL buffer dissipates 25 times less energy at optimal V_{DD} than a classic buffer whereas a 65nm-PFAL buffer dissipates only 8.69 times less energy at nomi-

nal V_{DD}. As we first choose to optimize the energy dissipation from the gate, the difference in energy gain is understandable.

Despite the higher gate dissipation, the second topology has a better energy gain that in the first one. Indeed, a 45nm-PFAL buffer and its power-clocks dissipate 2.9 times less energy at nominal V_{DD} than a classic buffer and its ideal power supply whereas a 65nm-PFAL buffer dissipates only 3.23 times less energy at nominal V_{DD}. We have an additional gain of 11.4% if we use the nominal V_{DD}. To be fair, in the previous section, we model the tank capacitor as a DC current voltage so we do not take into account the parasitic oscillation loss. This loss should decrease the energy gain, thus the difference between the energy gain from the two proposed topologies should be even higher.

4.3.5 Conclusion

In this section, we propose a resonant power-clock supply design for adiabatic logic running at nominal V_{DD}. The design is an enhancement of the one we presented later in the Section 4.3.2. We had a tank capacitor in order to make the power supply fully reversible. Due to this capacitor, we have to pay a special attention to the CTRL switch. Indeed, the switch parasitic capacitance is resonating and causes additional loss.

Then we derive the width of the switch in order to have the optimal energy efficiency. The width of the pass-transistor is proportional to the number of gates to drive.

We highlight why the CMOS is not the more suitable device for adiabatic devices: the threshold voltage. Due to the threshold voltage, quasi-adiabatic logic has an additional loss, the threshold loss. It also has an impact on the performance of the power-clock supply:

— the resistance of the pass transistor cannot be modeled as a constant R when V_{DD} is not at its nominal value,

— the on-state resistance and the leakages imply the choice of V_{TH} impacts the overall energy efficiency.

In CMOS 65nm, the adiabatic pipeline with the proposed topology dissipates $433aJ$ per operation. This pipeline dissipates 3.23 times less energy than a classical CMOS pipeline. The previous topology, which was chosen to lower the energy dissipation in the gate dissipates 2.9 times less energy than a classical CMOS pipeline. We gain 11.4% using the enhanced solution.

4.4 Chapter Conclusion

In this chapter, we present the power-clock supply. It is a 4-phase power supply, which has 2 idle states. Ideally, it is a 4-phase ramp in order to be a constant current source

during the evaluation and recovery phases. They are two main types of power-clock supplies: a capacitive-based step-up or a inductive-based resonant supplies. Even if the capacitive based topologies present the most efficient way to charge a capacitor with a ramp, we choose to study the inductor based topologies as they have less control signals, less transistors and less leakage.

At first, we decided to minimize the energy dissipation from the gates. Thus we developed a solution to drive the gates at optimal V_{DD}, 0.5V for CMOS 45nm. We propose 4 power-clock supplies with their own inductance and synchronized together. With this solution, an adiabatic pipeline dissipates 2.9 times less energy than a classical pipeline per operation. The main issue of this solution is that there is a glitch at the end of the evaluation, which causes more adiabatic loss and a direct charging loss. These additional dissipations lowers the potential energy saving. Indeed, with an ideal power-clock supply, the adiabatic PFAL pipeline dissipates 25 times less energy than a classical CMOS pipeline.

We investigated to find why there is this glitch. It comes from an error in the modeling: we model the gate as a constant resistance in series with a capacitance. However, if the model is correct at nominal V_{DD}, it is incorrect at optimal V_{DD}. When neither the NMOS nor the PMOS are fully on, the resistance reaches a maximum value. The maximum value of the resistance is inversely proportional to V_{DD}. This non on-state nor constant resistance is decreasing the quality factor of the LC filter, which causes the glitch.

Thus, we decide to develop a solution at nominal V_{DD}, i.e. 1.2V for CMOS 65nm. The solution is an enhancement of the previous developed solution. We use a pass transistor as the CTRL switch instead of a PMOS in order to have the full range of the power-clock signal. With this solution, an adiabatic pipeline dissipates 3.23 times less energy than a classical pipeline per operation. There is 11.4% more energy gain than with the previous solution. The main issue of this solution is the parasitic capacitance, which resonates with the inductance during the hold and waiting phase. This resonance increases the overall energy dissipation and limits the width of the pass transistor, which causes a direct charging.

The last main key point of this chapter is that the threshold voltage has a critical impact on the overall energy efficiency. On the gate side, due to the threshold loss, there is a minimum energy dissipation. On the power-clock supply side, the threshold voltage is the source of the glitch as the CMOS resistance is a function of V_{TH}. Thus, we cannot exploit the optimal V_{DD} solution. A perfect switch based device for adiabatic logic would be a device with a lower V_{TH}, less leakage and a constant resistance.

CHAPTER

5 Design of a CMOS Adiabatic Circuit

In this chapter, we present how we implemented an adiabatic circuit and its power supplies in order to evaluate the energy saving of such a circuit using our proposed power-clock supplies. The chapter is organized as follows: in Section 5.1, we present the circuit layout, in Section 5.2, we propose a model in order to be able to evaluate the energy dissipation with respect to the post layout extraction. Section 5.3 concludes the chapter.

5.1 Description of the Circuit

In this section, we present our prototype. The prototype is a PFAL pipeline and its power-clock supplies. It will be taped out in TSMC 65nm and its total area is 2 mm^2. The aim of this prototype is to evaluate the energy dissipation of the power-clock supplies. The operating frequency of the circuit is 2.5MHz which is the optimum frequency in terms of energy saving for the 65nm PFAL buffer (Fig.2.14). The supply voltage is 1.2V. We divided the circuit in three main parts: the digital load, which is the PFAL pipeline and its power-clock networks, the integrated part of the power-supplies, and the control blocks which ensure the 4 phases of power-clocks.

5.1.1 PFAL Pipeline and its Power-Clock Network

In order to reduce the power-supply inductance, the circuit should contain the largest number of PFAL buffer. Thus, the area of one PFAL buffer should be minimized. In Fig.5.1, the layout of a PFAL buffer is shown. A PFAL buffer has 2 inputs and 2 outputs that we have aligned in order to ease the pipeline placement. In order to polarize NMOS and PMOS bulks, we add V_{DD} and GND lines. We place a PC input at the top center of the buffer in

order to have an access to the Power-Clock Network. In terms of area cost, a PFAL buffer is a rectangle with a width of 2.025µm and a length of 3.765µm. A standard 65nm buffer has a width of 2µm and a length of 1.6µm. A PFAL buffer has an area 2.4 times bigger than a standard buffer.

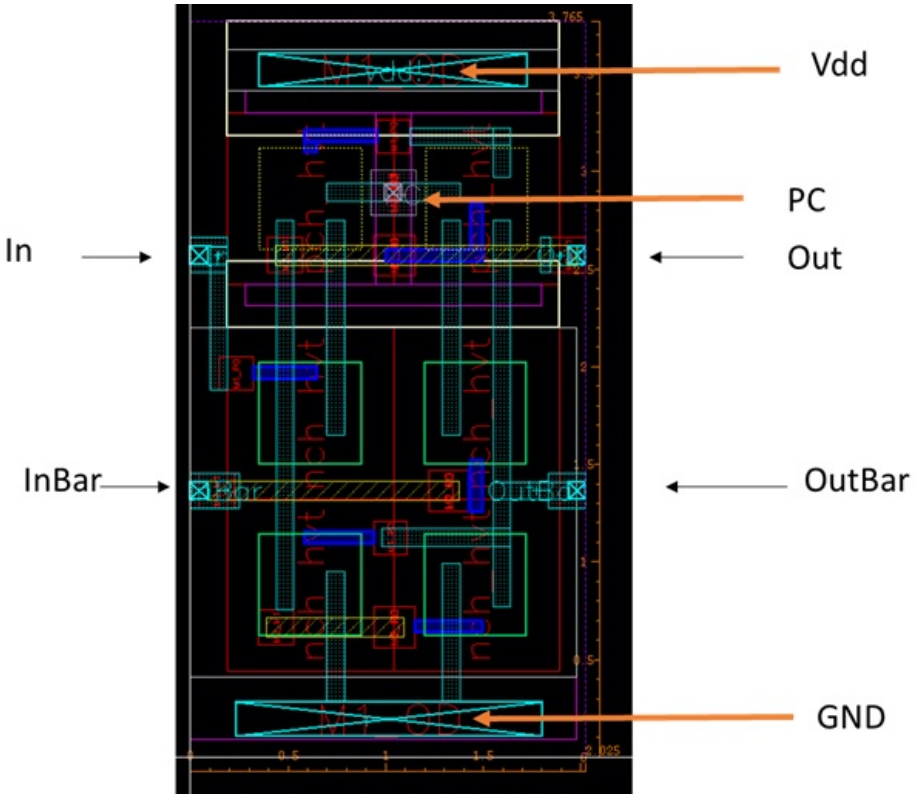

Figure 5.1 – Layout of a PFAL buffer.

In terms of layout, we aim to have a square with a side of 1.412mm. If we withdraw the area of the I/Os, the remaining area is a square with a side of 1.024mm. In order to determine the number of buffers, we allocate 90% of the remaining area to the pipeline. Thus, the pipeline is composed of 244 lines of 508 PFAL buffers. Each Power-Clock supply drives 30988 gates.

In Fig.5.2, a part of the pipeline layout and its power-clock networks are shown. Any adiabatic circuit needs the same networks: there are the signals, the bulk and the power-clock networks.

For the pipeline, the signal network is the connection of the outputs of a PFAL buffer to the next buffer's inputs. The bulk network is V_{DD} and GND lines at the top and the bottom of every buffer. The most challenging implementation of a network is the power-clock networks implementation.

Between two consecutive lines, the buffers, which have the same position in each line, are not supplied by the same power-clock. Thus, in order to supply correctly the gates, we have shifted the odd lines. In order to maximize the spacing between two power-clock networks, the shift is half of the width of a buffer (Fig.5.2). Each power-clock network is composed of two mesh networks. The first one supplies the odd lines and the second one supplies the even lines.

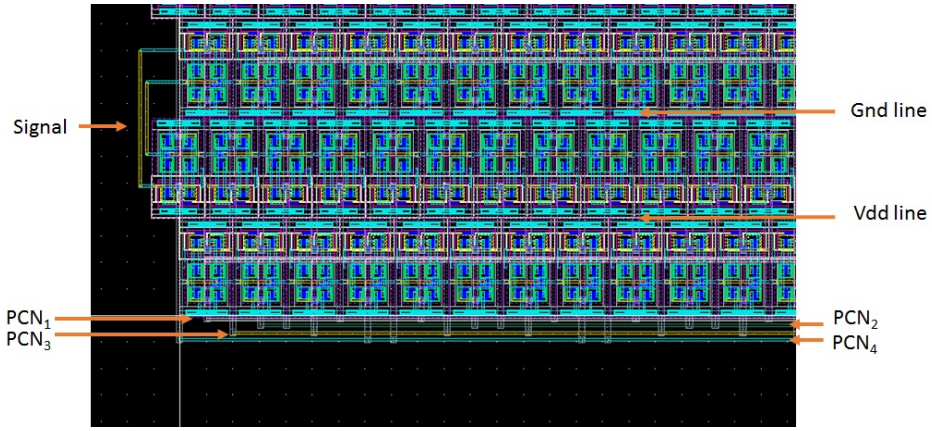

Figure 5.2 – Part of the pipeline layout and its power-clock networks.

5.1.2 Power-Clock Supplies

The circuit needs 4 power-clock supplies. The schematic of the proposed power-clock supply is shown in Fig.5.3. We have decided to use an external inductor and tank capacitor. The inductor cannot be integrated as we need an inductance of 11.7µH in order to supply the 30988 gates at 2.5MHz. One of the weakness of our proposed topology is the high value of the inductance.

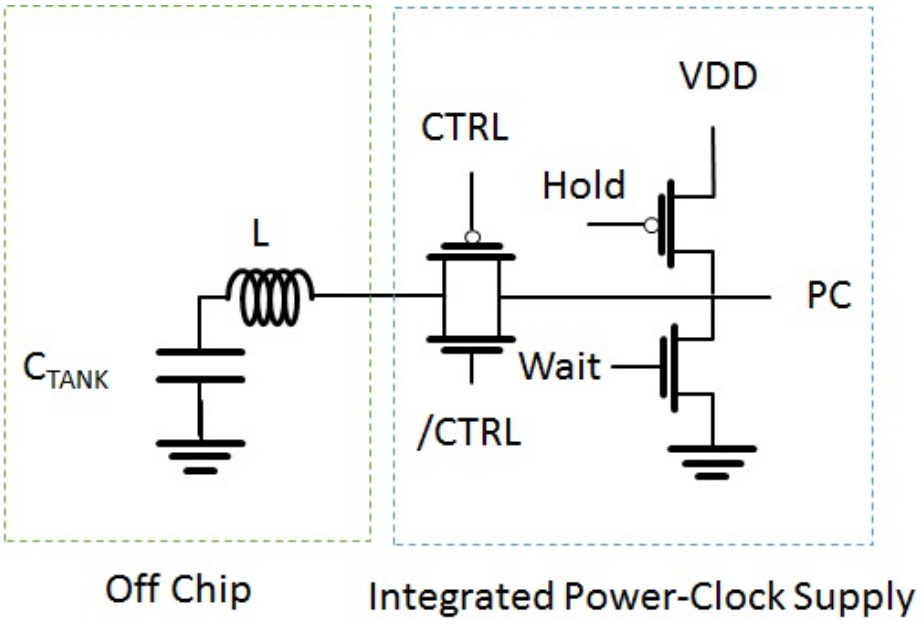

Figure 5.3 – Schematic of a power-clock supply.

In order to size the different transistors, we use the optimization that we describe in Section 4.3.3. Each power-clock drives 30988 gates, CTRL PMOS has a width of 18.59mm and CTRL NMOS has a width of 6.20nm. Hold and Wait MOSFET has the minimal width. All the MOSFET have the minimal length. The off-chip inductance and the tank capacitor have a value of 11.7µH and 2.1nF respectively.

The layout of the integrated part of the power-clock supply is shown in Fig.5.4. We have two objectives: power-clock supplies should fit in the remaining chip area, and its area has to be minimized. Moreover, we add a guard ring to protect the power-clock supply MOSFET as they are directly connected to an I/O.

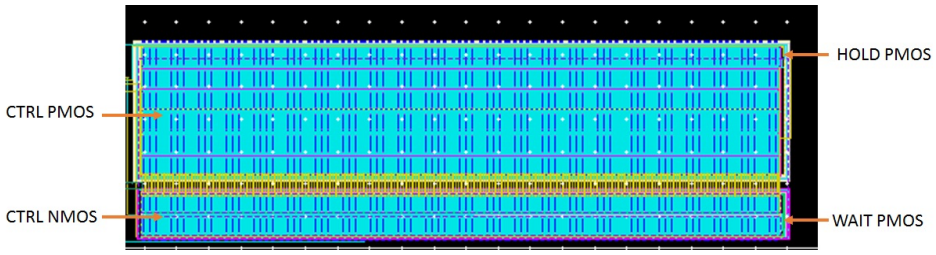

Figure 5.4 – Layout of the integrated part of a power-clock supply.

5.1.3 Control

Each power-clock supply needs a control block in order to ensure the 4 phases of the power-clock signal. The control block uses an external clock signal and a zero-current detection signal in order to have the synchronized control signals we have presented in Section 4.2.2.

Control can be divided in three main parts: the zero-current detection, the power-clock supply control and the clock divider. The aim of the zero-current detection is to minimize the energy dissipation at the end of the evaluation and recovery phase. Each power-clock supply has its own zero-current detection. The power-supply control ensures the synchronization between the 4 power-clock supplies and also the 4 phases of the power-clock signal. The clock divider ensures that two consecutive clock signals have a 90^o phase shift.

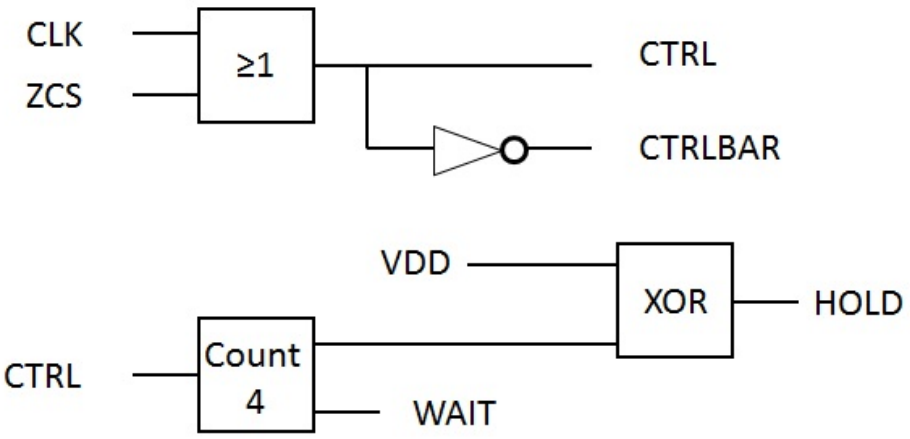

Figure 5.5 – Schematic of the control block.

The control signals are a function of the zero current detection signal, ZCS, and the external clock signal, CLK. The schematic of the control block is shown in Fig.5.5.

The zero current detection is made with a Schmitt trigger, a current mirror and a coupling capacitor. The schematic of the zero current detection is shown in Fig.**??**. The coupling capacitor is sized in order to have a differentiator with the connected PMOS. In our application, the coupling capacitor is a MOM capacitor of $20fF$ in order to be able to differentiate the power-clock signal.

The Layout of the control block and its zero-current detection is shown in Fig.5.6. We adapt the length of the MOM capacitor in order to have the same length of the Power-Clock MOSFETs then we minimize the area of the control block and the zero current detection.

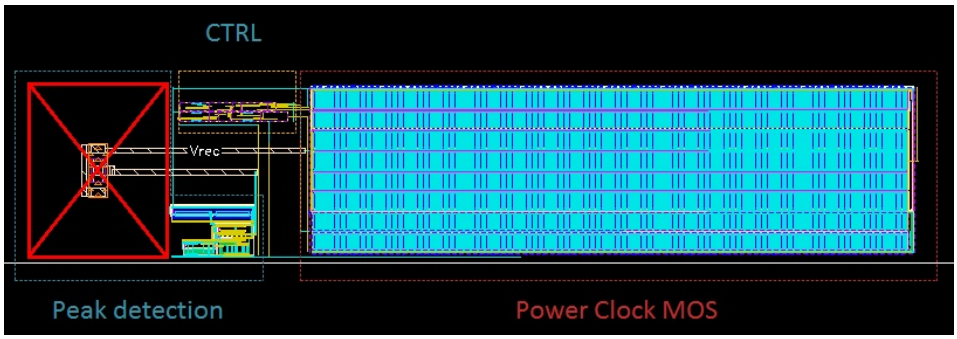

Figure 5.6 – Layout of one power-clock supply and its control block.

The clock divider is composed of 4 D flip-flop gates, DFF, each output of one DFF is an external clock signal. The layout of the clock divider is shown in Fig.5.7.

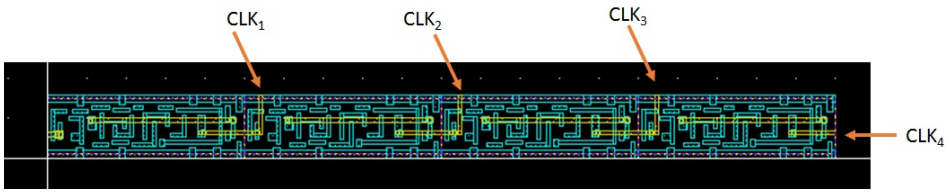

Figure 5.7 – Layout of the clock divider.

5.1.4 Top view

In this subsection, we present the top view with the I/O ring and how to test the circuit. We choose to use 24 I/Os. There are 12 test pins, 4 signal pins and 8 power-clock pins. The top view of the layout is shown in Fig.5.8.

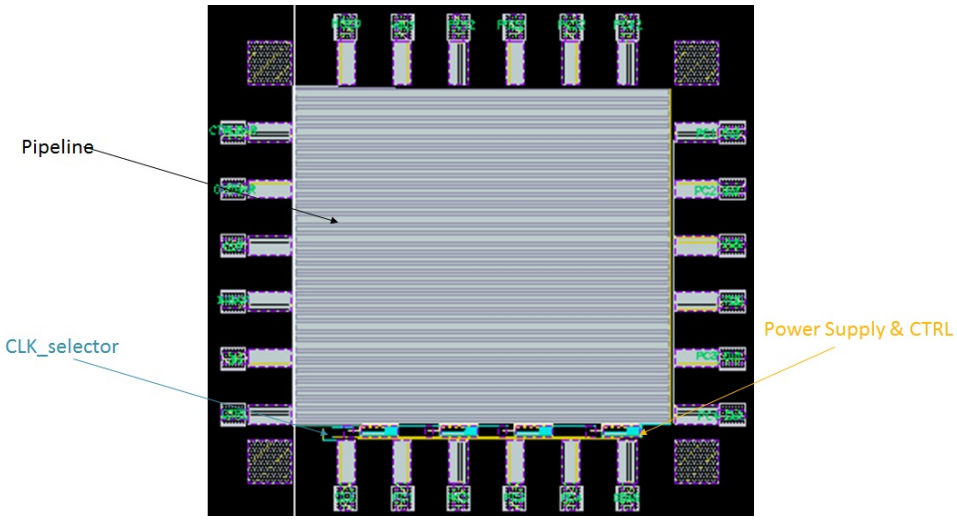

Figure 5.8 – Layout of the adiabatic pipeline and its power-clock supplies.

With this prototype, we have two objectives: 1) evaluate the energy dissipation of our power-clock supply. 2) evaluate the impact of the power-clock network on the power-clock signal.

As the inductance and the tank capacitor are off chip, we can directly evaluate the energy dissipation of the power-clock supplies thanks to the tank capacitor current and voltage. Another advantage of this externalization is that we can connect an ideal power-clock supply to each power-clock input. It means that during the test of the chip, we will be able to evaluate the energy dissipation coming from the PFAL pipeline and its power-clock networks and the energy dissipation coming from the power-clock supply.

In the 12 test pins, 4 are used to test the functionality of the control block and 8 are used to evaluate the impact of the power-clock network on the power-clock signal. We get the voltage at the output of each power-clock supply thanks to a test pin. Then, we get the voltage that a buffer from the last line receives. We choose the buffer which is the most impacted by the power-clock network parasitic in order to evaluate the critical impact of the power-clock network. Then we compare the voltage from the power-clock output and the power-clock gate input in order to evaluate the phase shift.

5.1.5 Conclusion

In this section, we present the circuit we will use in order to evaluate the energy dissipation of our proposed topology for power-clock supply. It is composed of an adiabatic PFAL pipeline, which frequency is 2.5MHz, 4 power-clocks supplies and its control blocks. The pipeline is composed of 123952 PFAL buffers, thus each power-clock supplies 30988 gates. The circuit is ready to be tape-out in CMOS 65nm.

In order to evaluate the energy dissipation of the power-clock supply, we measure the energy variation in the tank capacitor which is off chip. In order to evaluate the impact of the power-clock network, we compare the voltage at the output of the power-clock supply and at the power-clock input of the most impacted buffer.

5.2 Post Layout Simulations

In this section, we introduce our methodology in order to estimate the energy dissipation in the circuit while we extract the parasitic resistances and capacitances due to the layout.

5.2.1 Pipeline Model

Due to the license restrictions, we cannot perform post-layout simulations on the block from the digital library. Thus, in order to evaluate the impact of the power-clock network parasitics, we model the PFAL pipeline and its power-clock networks.

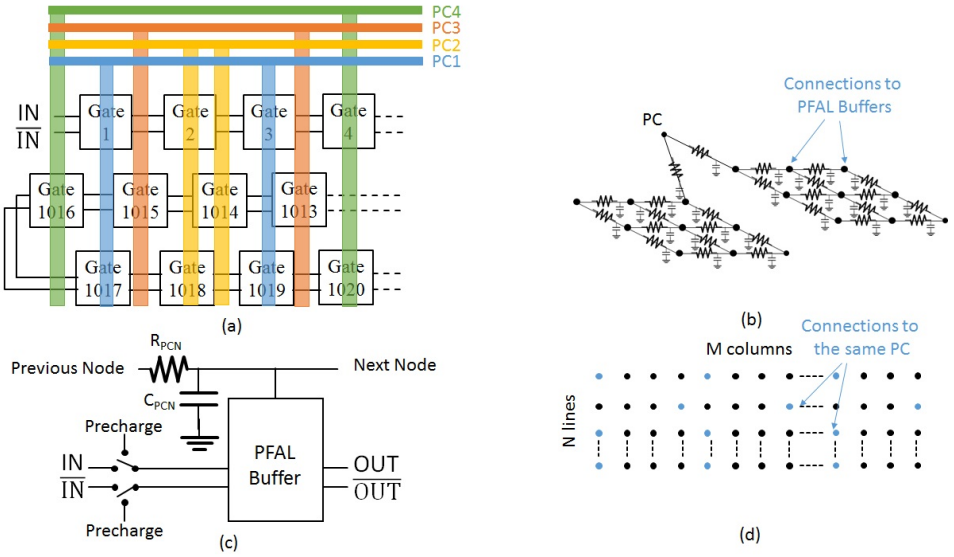

Figure 5.9 – (a) Power-clock networks in the adiabatic pipeline, (b) schematic of one power-clock network, (c) a PFAL buffer and its associated power-clock network parasitics and (d) symbolic matrix representation of the connections between the PFAL buffers and the different power-clocks

In Fig.5.9.a, the 4 different power-clock networks and the pipeline are represented. For example, we can represent the pipeline as a matrix of buffers, B. A buffer, which is in the M^{th} line at the N^{th} position is refer as B(M,N). Two buffers which are at the same position on two consecutive lines, thus, B(M,N) and B(M+1,N) are not supplied by the same power-clock. Thus there are two different mesh networks in order to distribute the same power-clock signal, one mesh network delivers the power-clock signal to the odd lines and the other one delivers it to the even lines. A representation of the two mesh networks for one power-clock supply is shown in Fig.5.9.b.

The PFAL pipeline is composed of PFAL buffer modeled as described in Fig.5.9.c. Each PFAL buffer has its own power-clock network parasitic resistance and capacitance. A buffer B(M,N) (Fig.5.9.d) is connected to buffers, which have the same position and one is two lines above B(M-2,N) and the other one is two lines below B(M+2,N). The buffer is also connected to buffers, which are on the same line and one is in the $N-4^{th}$ position, B(M,N-4) and another one is in the $N+4^{th}$ position, B(M,N+4). Thus, each node is a connection between 4 buffers.

We need to pre-charge each buffer in order to bypass the charge time of the pipeline, which is dependent of the number of gates. In our case, we need $12.4ms$. Thus, we add a pre-charge input in the PFAL buffer, which is composed of an ideal 3 branch switch. The

PFAL buffer is charged during the first cycle then it is connected to the signal network. The precharge has no impact on the energy dissipation as the first cycle is not evaluated.

In order to find the parasitic capacitance and resistance of the power-clock networks, we have done a post-layout parasitic extraction. The power-clock network node resistance has a value of $480 m\Omega$ and the power-clock node capacitance has a value of $301 a$F.

5.2.2 Energy dissipation of the circuit before the parasitic extraction

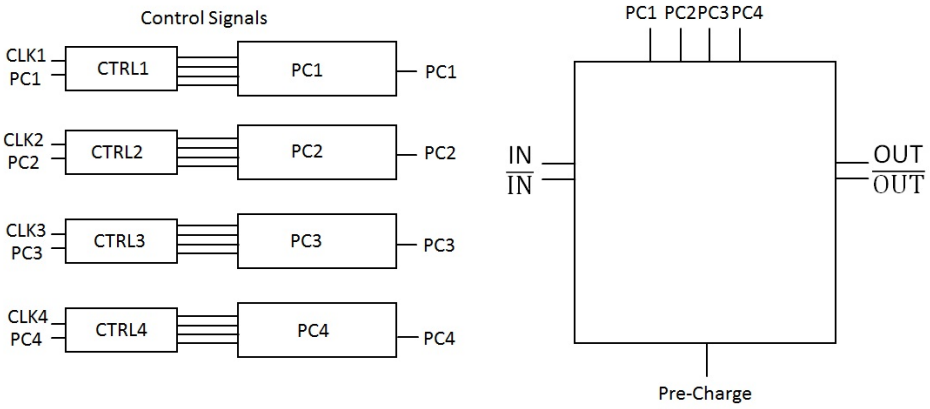

Figure 5.10 – Circuit test bench.

In this subsection, we compare the energy dissipation of the circuit, which is supplied by ideal and the proposed power-clock supplies. Power-clock network parasitics have not been considered in the following simulations. In Fig.5.10, the test bench is presented. It is composed of the 4 power-clock supplies and their control blocks and the pipeline composed of the PFAL buffer described above.

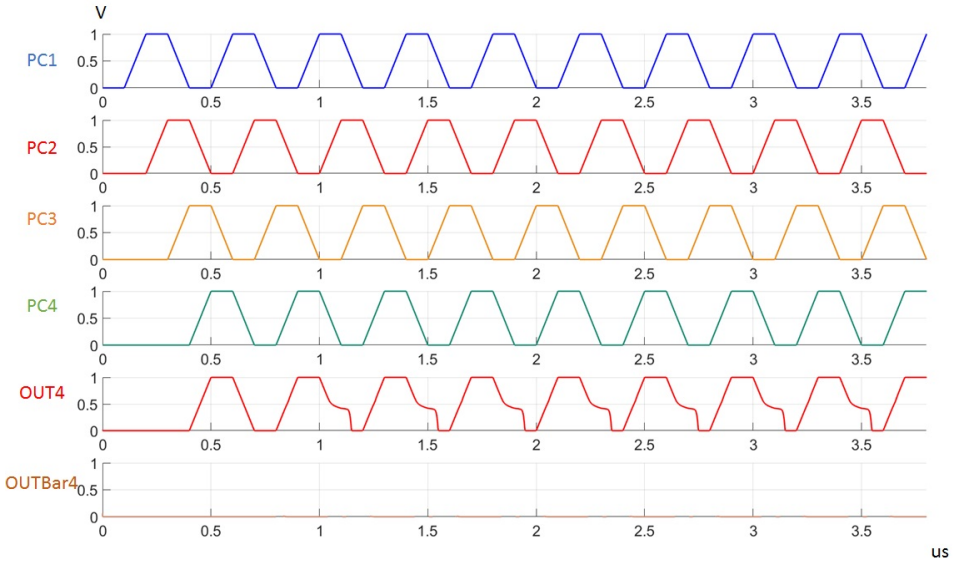

Figure 5.11 – Ideal power-clock voltages and last buffer signal voltages.

In order to find the energy dissipation of the adiabatic pipeline, we perform a 10-cycle transient simulation of the test bench. Simulation results with ideal power-clock supplies are shown in Fig.5.11. The pre-charge can be seen for the first period of the output voltage. In order to find the energy dissipation per cycle of the pipeline, we compute the energy dissipation of each power-clock for the last five cycles, in order to have a mean energy dissipation per cycle, and we sum the mean result. With the ideal power-clock supplies, the PFAL pipeline dissipates $20pJ$ per cycle.

Simulation results with the proposed power-clock supplies are shown in Fig.5.12. We size the MOSFETs of power-clock supplies thanks to the optimization in Section 4.3.3. The power-clock waveforms are very different from the ideal power-clock waveforms. One could think that the pass-transistor resistance is too high and makes this difference. However, if we increase the size of the pass-transistor, we will increase the energy dissipation coming from the resonance of the pass-transistor capacitance and at the end, the overall energy dissipation will be increased. With the proposed power-clock supplies, the PFAL pipeline dissipates $54.3pJ$ per cycle. The energy dissipation has been computed using the same process that we followed for the energy dissipation of the pipeline which is supplied by ideal power-clock.

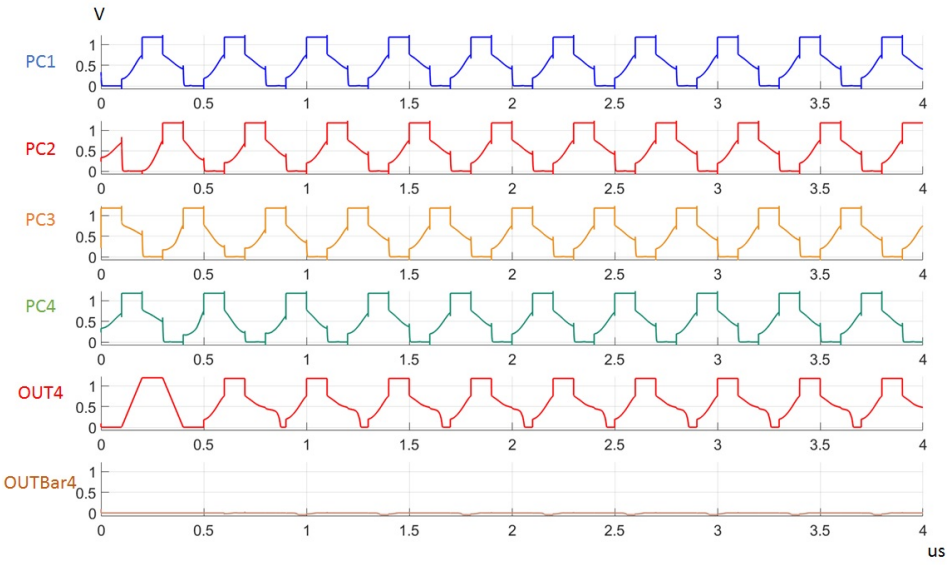

Figure 5.12 – Real power-clock voltages and last buffer signal voltages.

In Table 5.1, the energy dissipations for the adiabatic pipeline with ideal and proposed power-clock supplies are compared to the non-adiabatic CMOS pipeline. A non-adiabatic CMOS pipeline composed of 123952 buffers and supplied by an ideal power supply dissipates 178pJ per cycle.

Table 5.1 – ENERGY DISSIPATION OF THE DIFFERENT PIPELINES FOR DIFFERENT POWER-CLOCK SUPPLIES

Circuit	Energy Dissipation (pJ)	Energy Gain (X)
Non-adiabatic CMOS pipeline with ideal power supply	178	1X
PFAL pipeline with ideal power-clock supplies	20	8.9X
PFAL pipeline with proposed power-clock supplies	54.3	3.28X

The adiabatic pipeline dissipates 20pJ with ideal power-clock supplies and 54.3pJ with proposed power-clock supplies. It means that the adiabatic pipeline could save 8.9 times more energy than the non-adiabatic pipeline and 3.28 times more energy with our pro-

posed power-clock supplies. These results are in accordance with the optimization in Section 4.3.4.

5.2.3 Energy dissipation of the circuit after the parasitic extraction

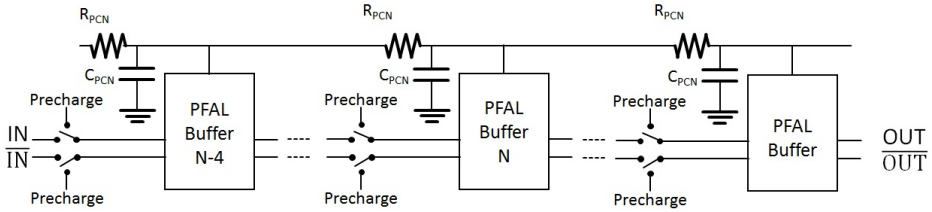

Figure 5.13 – Model of the PFAL pipeline with its power-clock networks.

In this subsection, we compute the energy dissipation of the adiabatic pipeline with respect to the ideal and the proposed power-clocks and the power-clock network parasitics. The benchmark is the same as in the previous subsection and shown in Fig.5.10. In order to simulate the worst case scenario, we decided to model branch power-clock networks instead of the network described in Fig.5.9.b. The new pipeline model is presented in Fig.5.13.

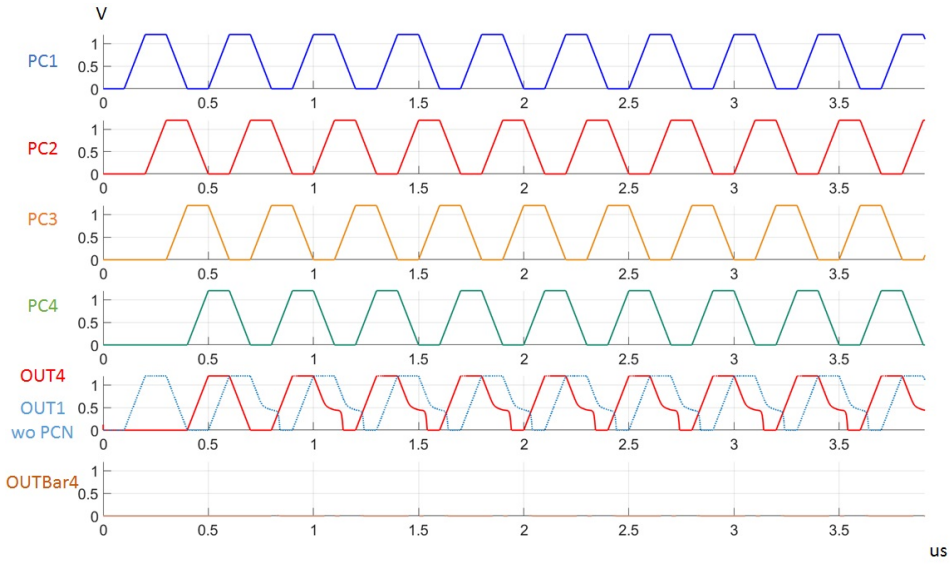

Figure 5.14 – Ideal power-clock voltages and last buffer signal voltages.

We perform the same transient simulations that we have done above in order to evaluate the impact of power-clock networks on the energy dissipation of the adiabatic pipeline. In order to find the energy dissipation of the adiabatic pipeline, we perform simulations with ideal and proposed power-clock supplies. Simulation results for the ideal power-clock supplies are shown in Fig.5.14. In order to show the influence of the power-clock network on the output voltage, we also show the output voltage of one buffer supplied by an ideal power-clock without power-clock network parasitics.

In term of functionality, power-clock network has no impact. However, with the power-clock network parasitics, the pipeline dissipates 20.8pJ with ideal power-clock supplies. Thus, the power-clock network contributes to 3.8% of the overall energy dissipation.

Then, we perform the same transient simulations where we substitute the ideal power-clock supplies by the proposed power-clock supplies. Simulation results are shown in Fig.5.15. Like the previous figure, we also add the output voltage of one buffer supplied by a proposed power-clock without the power-clock network parasitics in order to show the influence of the parasitics on the output voltage.

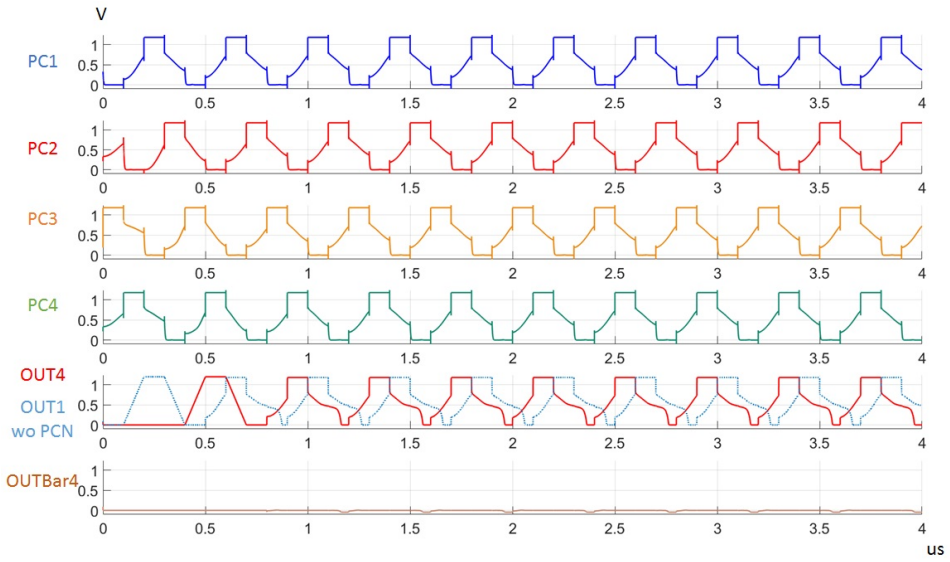

Figure 5.15 – Proposed power-clock voltages and last buffer signal voltages.

Power-clock network parasitics have no impact on the functionality of the adiabatic pipeline supplied by the proposed power-clock supplies. However, power-clock network parasitics impact the energy dissipation. It increases from 54.3pJ to 59.2pJ. Thus, the power-clock network contributes to 8.2%.

The energy dissipation of the pipeline is more impacted by the power-clock network par-

asitics when it is supplied by the proposed power-clock supply than an ideal one because power-clock network parasitics have a higher impact on the energy dissipation due to two main reasons: 1) the power-clock network parasitic capacitor increases the total load capacitance, which lowers the resonance frequency of the power-clock supply. 2) the power-clock parasitic resistor increases the total resistance which lowers the quality factor of the power-clock supply.

Table 5.2 – ENERGY DISSIPATION OF THE DIFFERENT PIPELINES AND THEIR POWER-CLOCK NETWORKS FOR DIFFERENT POWER-CLOCK SUPPLIES

Circuit	Energy Dissipation (pJ)	Energy Gain (X)
Non-adiabatic CMOS pipeline with ideal power supply	178	1X
PFAL pipeline with ideal power-clock supplies	20.8	8.56X
PFAL pipeline with proposed power-clock supplies	59.2	3.00X

In Table 5.2, the energy dissipations for the adiabatic pipeline with ideal and proposed power-clock supplies are compared to the non-adiabatic CMOS pipeline. The adiabatic pipeline dissipates 20.8pJ with ideal power-clock supplies and 59.2pJ with proposed power-clock supplies. The non-adiabatic pipeline has an ideal power delivery network and power supply. Thus, it dissipates 178pJ. It means that the adiabatic pipeline could save at most 8.56 times more energy than the non-adiabatic pipeline and 3 times more energy with our proposed power-clock supplies.

5.2.4 Conclusion

In this section, we perform simulations in order to quantify the energy dissipation of the PFAL pipeline supplied by the proposed power-clock supplies. We also perform post-layout parasitic extraction in order to evaluate the power-clock network parasitic and assess the impact on the overall energy dissipation.

Without the power-clock network parasitic, the adiabatic pipeline dissipates 54.3pJ per cycle when it is supplied by the proposed power-clock supplies and 20pJ when it is supplied by ideal ones. Thus, for the overall energy dissipation, 20pJ are dissipated by the adiabatic pipeline and 34.3pJ are dissipated by the power-clock supplies.

With the power-clock network parasitic, the adiabatic pipeline, which is supplied by the proposed power-clock supplies, dissipates 59.2pJ per cycle and 20.8pJ when the pipeline is

supplied by the ideal power-clock supplies. The power-clock network contributes to 3.8% of the overall energy dissipation when the pipeline is supplied by ideal power-clock supplies and 8.3% when the pipeline is supplied by the proposed ones. Power-clock networks have a higher impact on the energy dissipation as they lower the resonance frequency and the quality factor of the power-clock supplies.

The circuit we have realized in TSMC 65nm, which has a supply voltage of 1.2V, and an operating frequency of 2.5MHz dissipates 59.2pJ per cycle. This pipeline dissipates 3 times less energy than a classic CMOS pipeline. 33.8% of the overall energy dissipation comes from the PFAL pipeline, 57.9% comes from the power-clock supplies and 8.3% comes from power-clock networks.

5.3 Chapter Conclusion

In this chapter, we present the realization of an adiabatic PFAL pipeline and its power-clock supplies. The circuit will be taped out in TSMC 65nm. In addition to the PFAL pipeline with a supply voltage of 1.2V and an operating frequency of 2.5MHz, the circuit has the 4 power-clock supplies and control blocks. The circuit has an area of $2mm^2$. The pipeline represents 90% of the active area, which is the remaining area after the I/O placement. Thus, the pipeline has 123952 buffers. It means that each power-clock has to supply 30988 gates.

The main advantage of the proposed power-clock supply is the synchronization between each power-clock supply. The synchronization is ensured by the control blocks. Their other objective is to ensure the 4 phases of the power-clock signal. In order to reach these objectives, the control blocks have two input signals: an external clock and a zero current detection. Power-clock supplies and their control block represent less than 5% of the area.

Then, we choose to design 24 I/Os: 4 I/Os are dedicated to the signal, 8 I/Os to the power-clock supplies and 12 I/Os for the test of the circuit. In addition to the test of the functionality of the circuit, we have two objectives: 1) quantify the energy dissipation of the circuit, 2) evaluate the impact of the power-clock network parasitics on the pipeline signal.

In order to quantify the energy dissipation before we can test the circuit, we perform post-layout simulations. As we do not get the authorization to perform post layout simulation on the digital block that we are using for the control block, we made a pipeline model which includes power-clock network parasitic. We perform different simulations in order to quantify the contribution on the energy dissipation of the pipeline, the power-clock supplies and the power-clock network parasitic.

Without the power-clock network parasitic and ideal power-clock supplies, the pipeline dissipates 20pJ per cycle. The energy dissipation is 54.3pJ when the pipeline is supplied

by the proposed power-clock supplies. These results are expected as we have optimized power-clock supplies as in Section 4.3.4.

Then, we perform simulations with power-clock network parasitic. The PFAL pipeline dissipates $59.2pJ$ when it is supplied by the proposed power-clock supply. In term of contribution, 33.8% of the energy dissipation comes from the PFAL pipeline, 57.9% comes from the power-clock supplies and 8.3% comes from power-clock networks.

In conclusion, we expect that the pipeline we have designed will dissipate 3 times less energy than a classic CMOS pipeline.

CHAPTER

6 Adiabatic Logic Beyond CMOS

In this chapter, we propose an enhancement of the positive feedback adiabatic logic, PFAL. We replace CMOS by a promising field effect transistors: Carbon Nanotube Field Effect Transistor, CNTFET. The chapter is organized as follows: in Section 6.1, we introduce CNTFET; in Section 6.2, we propose an optimization of CNTFET in order to minimize the energy dissipation of a PFAL buffer; then, in Section 6.3, we compare CMOS and CNTFET PFAL buffers. Section 6.4 concludes the chapter.

6.1 Introduction to CNTFET

In this section, we introduce the Carbon Nanotube Field Effect Transistor, CNTFET [5]. CNTFET is shown in Fig.6.1. The aim of this field effect transistor is to keep the source, drain and gate configuration, where the channel is made with single-walled Carbon Nanotubes (CNTs). The idea behind is that carbon nanotube has a higher electrical and thermal conductivity than doped silicon.

CNTFETs are a promising replacement for CMOS thanks to three proprieties. Unlike the CMOS, there is no electron diffusion transport [20]. The electron transport is ruled by the quantum mechanics and it is called ballistic transport. The ballistic transport reduces the scattering effect [21]. Thus, the electron has a higher speed than via the diffusion transport. The other propriety of is that the current density in CNTFET is higher than in CMOS. One of the main issues with the CMOS scaling is the short channel effect [80]. It leads to a shift of the threshold voltage, which impacts the leakage current and the maximum operating frequency. Short channel effect comes from the fact that there is a need of a large gate capacitance in order to create the channel. Thus, it is dependent on the doped silicon. Hence, there is no short channel effect on CNTFET.

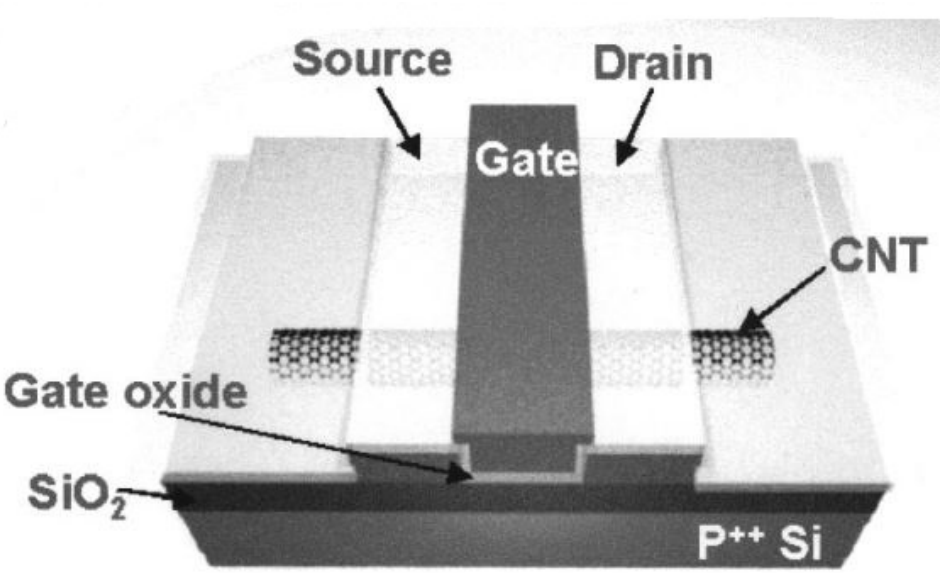

Figure 6.1 – Carbon Nanotube Field Effect Transistor, source: [5].

Typical applications for CNTFET are high performance applications such as data storage [81] or high computational performance [82]. Our objective is to use these CNTFET to develop ultra-low power logic using the adiabatic principles.

There are two types of CNTFET transistor: Schottky barrier transistor and MOS-like transistor. The idea behind Schottky barrier transistor is to modulate the contact resistance instead of the channel resistance [83]. In this chapter, we use MOS-like transistors, the resistance of the carbon nanotube is controlled by the gate voltage.

In order to quantify the energy dissipation of a PFAL gate using CNTFET, we use the Stanford model [6]. The representation of the model is shown in Fig.6.2. The model presents an accurate description of the gate capacitance, the channel resistance and the parasitic capacitances and resistances. Moreover, it includes p-type and n-type CNTFETs [84], which are mandatory to design logic gates.

From an adiabatic gate point of view, the energy dissipation is impacted by the supply voltage, V_{DD}, the operating frequency, f, the gate on-state resistance, R and capacitance, C, and the transistor threshold voltage, V_{TH}. All of these parameters are impacted by the transistor characteristics. In the Stanford model, there are 6 parameters a designer can change, in order to vary the transistor characteristics: the contact length, L_c, the gate length L_g, the external length, L_{ext}, the space between the carbon nanotubes, s, the diameter of the carbon nano-tube, d and the width of the CNTFET, w.

We decide to use the minimum values of L_c, L_g and L_{ext} in order to minimize the intrinsic

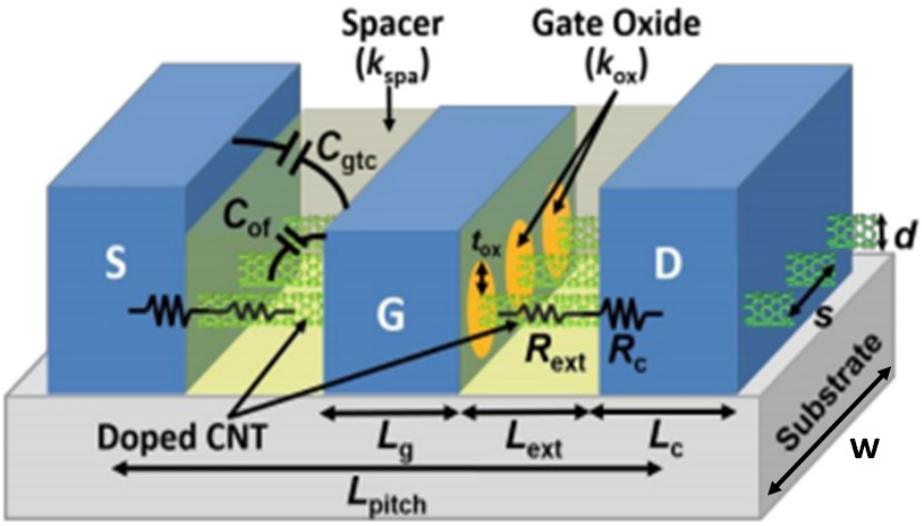

Figure 6.2 – Representation of a CNTFET with Stanford model and model parameters, source: [6].

capacitance of the transistor [85]. It means that we have 3 parameters left to optimize the CNTFET: s, d and w. These three parameters are dependent on each other. This dependence is expressed as follows:

$$w = d + (\mathrm{N} - 1)s \tag{6.1}$$

where N is the number of carbon nano-tubes on a channel.

Beside V_{DD}, which is limited by the model to 0.7V up to 1V, f, R, C and V_{TH} are impacted by these three parameters. Similarly to CMOS, the width impacts R and C. The impact of d on V_{TH} is expressed as follows:

$$V_{TH} = \frac{aV_\pi\sqrt{3}}{3d\,e} \tag{6.2}$$

where a is the carbon to carbon atom distance constant, V_π is the carbon π-π bond energy and e the unit electron charge.

The maximum operating frequency is impacted by the gate passives and V_{TH}. Thus, it is impacted by d and w.

6.2 Optimization of a PFAL CNTFET Buffer

In this section, we propose an optimisation of the CNTFETs in order to minimize the energy dissipation of a PFAL CNTFET buffer, which is shown in Fig.6.3a. In order to design this buffer, we use the PFAL architecture and we replace PMOS with p-type CNTFET and NMOS with n-type CNTFET. Buffer CNTFETs has the same w, s and d.

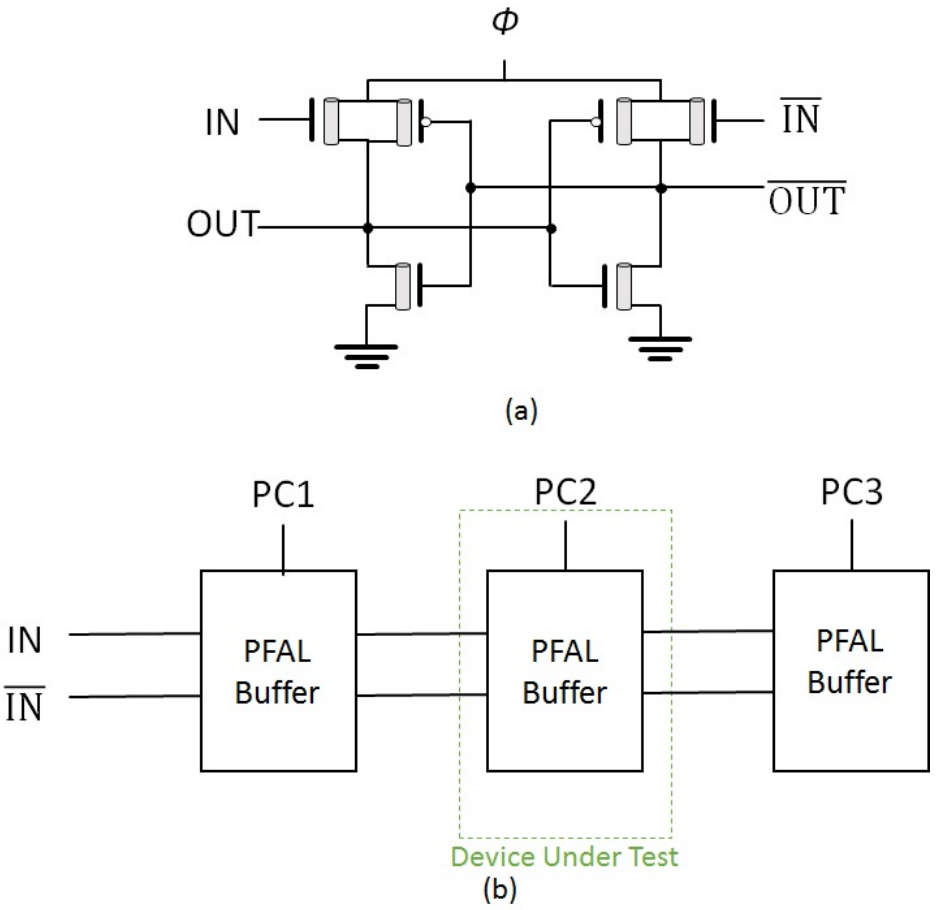

Figure 6.3 – (a) Schematic of a PFAL CNTFET Buffer and (b) test-bench in order to quantify the energy dissipation.

In order to evaluate the energy dissipation, we use the test bench presented in Fig.6.3b which is the same as the one we used in Section 3.4.2 to evaluate the energy dissipation of PFAL CMOS buffer. Power-clocks deliver ideal 4-phase ramp signals. As CNTFET is a switch, it faces the same challenges we have presented in Section 3.2. It means that the en-

ergy dissipation is impacted by the leakage current, the threshold voltage and the adiabatic dissipation. The total energy dissipation, E, is expressed as follows:

$$E = \underbrace{V_{DD} I_{Leak} T}_{Leakage\,Dissipation} + \underbrace{\frac{1}{2} C V_{TH}^2}_{Threshold\,Dissipation} + \underbrace{2\frac{RC}{T} C V_{DD}}_{Adiabatic\,Dissipation} \tag{6.3}$$

where I_{Leak} is the leakage current and T is the ramp time.

6.2.1 Impact of the CNTFET Width on the PFAL Energy Dissipation

The first parameter we study is the width of the CNTFET and its impact on the PFAL buffer energy dissipation. Stanford model is valid if N ≥ 3. In this subsection, we set $s = 10nm$ and $d = 1.2nm$, which are the model default values. Thus, using Eq.(6.1) the model is valid if $w \geq 21.2nm$. We perform several simulations with different width values in order to evaluate its impact. Fig.6.4 shows the energy dissipation of a PFAL CNFET as a function of the operating frequency with different width values from $70nm$ to $1um$.

With such configuration, the maximum operating frequency of the PFAL buffer is 10GHz. For an operating frequency lesser than 9GHz, the leakage losses are predominant in the PFAL energy dissipation. When the frequency is between 9GHz and 10GHz, the adiabatic and leakage losses impact the energy dissipation. Similarly to the CMOS buffer, the V_{TH} effect is never predominant in the total energy dissipation.

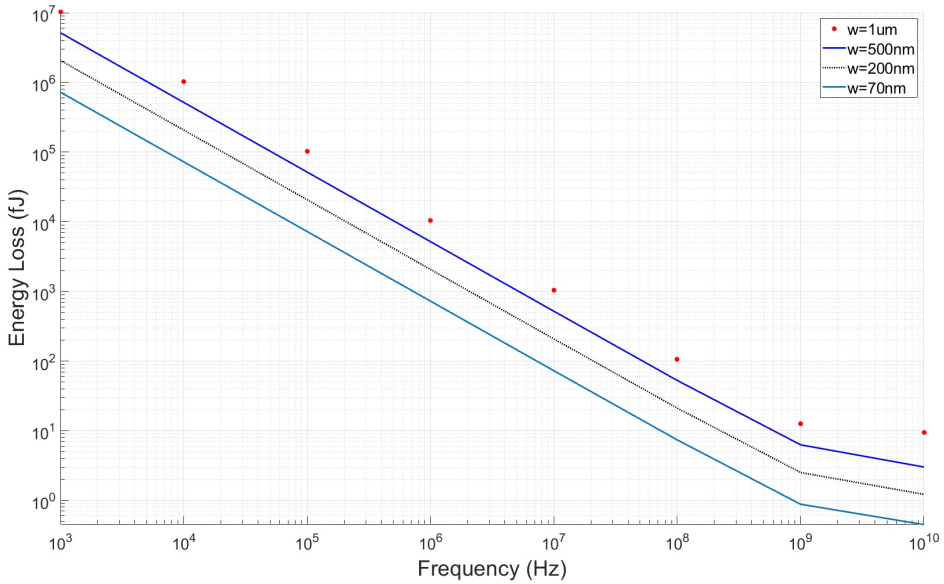

Figure 6.4 – Energy dissipation of PFAL CNTFET buffer as a function of the frequency for different CNTFET width values.

Physically, decreasing the width of the CNTFET increases the contact resistances and decreases the gate capacitance. As we set s and d, it also decreases the number of carbon nanotubes. As we can see in Fig.6.4, decreasing w decreases the leakage dissipation. The leakage dissipation is highly linked to the number of carbon nanotubes [86]. Thus, if we decrease N, we decrease the energy dissipation. In conclusion, we should set the width at the minimum value in order to limit N.

6.2.2 Impact of the Spacing between two Carbon Nanotubes on the PFAL Energy Dissipation

In this subsection, we study the impact of the spacing between two carbon nanotubes on the PFAL buffer energy dissipation. We set $w = 70nm$ and $d = 1.2nm$, as the PFAL buffer dissipates less energy with these parameter values (Fig.6.4). Using Eq.(6.1) with N = 3, we find the maximum spacing value, which is $34.4nm$. Thus, in these conditions, the Stanford CNTFET model is valid for a spacing between $2.5nm$ and $34.4nm$. We perform several simulations with different spacing values in order to evaluate its impact. Fig.6.5 shows the energy dissipation of a PFAL CNTFET buffer as a function of the operating frequency with different spacing values from $12nm$ to $25nm$.

With such configuration, the maximum operating frequency of the PFAL buffer is still $10GHz$. Leakage losses are predominant for an operating frequency less than $9GHz$. When

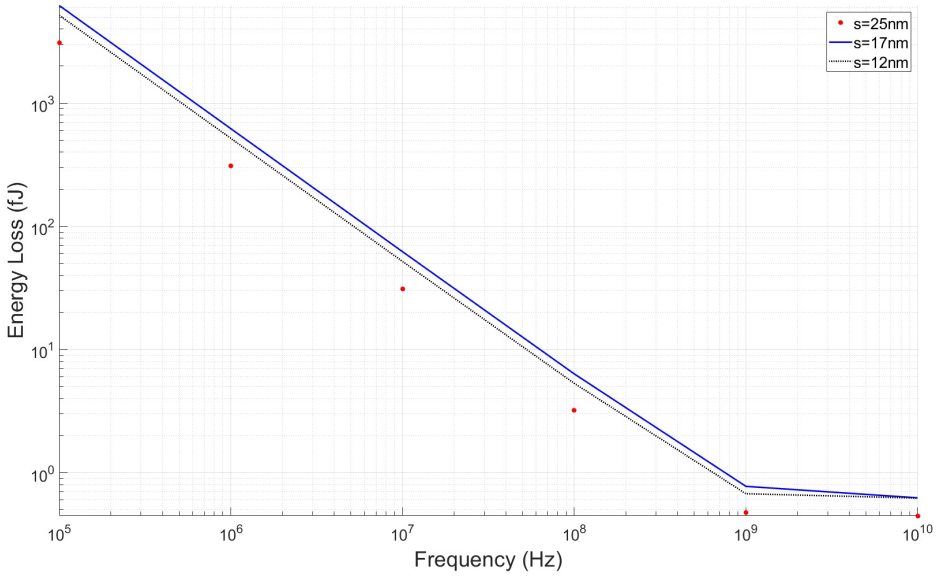

Figure 6.5 – Energy dissipation of PFAL CNTFET buffer as a function of the frequency for different Carbon Nanotubes spacing values.

the frequency is between 9GHz and 10GHz, the adiabatic and leakage losses impact the energy dissipation. Similarly, the V_{TH} effect is never predominant in the total energy dissipation.

Decreasing the spacing of the carbon nanotubes increases N and the parasitic capacitances. Tuning s impacts the leakage loss only. It means there are too many carbon nanotubes, what increases the predominance of the leakage losses. Hence, we need to set the width, w, and the spacing, s to reduce N at its minimum value: N = 3.

6.2.3 Impact of the Diameter of the Carbon Nanotube on the PFAL Energy Dissipation

In this subsection, we study the impact of the diameter of a carbon nanotube on the PFAL buffer energy dissipation. We set $w = 70nm$ and $s = 25nm$, as the PFAL buffer dissipates less energy with these parameter values (Fig.6.5). The Stanford CNTFET model is valid for a diameter between $1nm$ and $2nm$. We perform several simulations with different diameter values in order to evaluate its impact. Fig.6.6 shows the energy dissipation of a PFAL CNTFET buffer as a function of the operating frequency with different diameter values from $1nm$ to $1.5nm$.

In contrary to the two previous parameters, in the same simulation conditions, tuning d

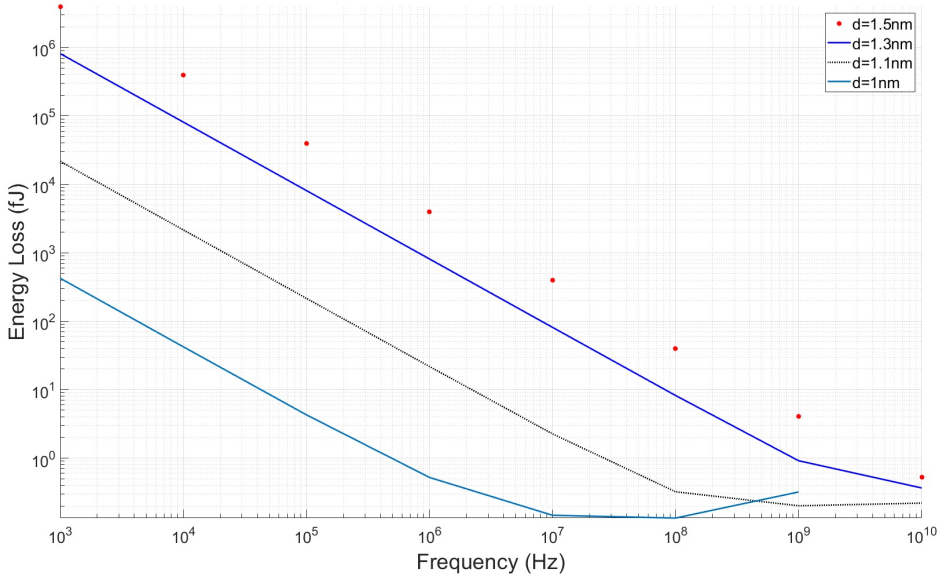

Figure 6.6 – Energy dissipation of PFAL CNTFET buffer as a function of the frequency for different Carbon NanoTubes diameter values.

does not change N. However, it has an impact on V_{TH} (Eq.(6.2)). Decreasing d increases V_{TH}. Thus, it decreases the leakage dissipation and lowers the maximum operating frequency as we can see in Fig.6.6.

With $d \geq 1.5nm$, the optimal frequency is the maximum operating frequency, i.e. 10GHz. For lower d, adiabatic losses are predominant for the highest frequency. Hence, there is an optimum frequency, which is not the maximum operating frequency. In order to minimize the energy dissipation of the PFAL buffer, we set d at its minimum value, i.e. $d = 1nm$.

6.2.4 Optimization

In this subsection, we optimize the CNTFET in order to minimize the energy dissipation. We set $d = 1nm$ as this parameter value minimizes the energy dissipation, and we set w and s such as N = 3.The Stanford CNTFET model is valid for $s \geq 2.5nm$. We perform several simulations with different $\{w, s\}$ in order to minimize the energy dissipation. Fig.6.7 shows the energy dissipation of a PFAL CNTFET buffer as s varies from $2.5nm$ to $11nm$.

In order to minimize the energy dissipation of the PFAL buffer, we have to use the minimum spacing value. If we increase s, then w increases. Thus, it leads to an increase in the CNTFET intrinsic resistance and capacitance which has three impacts: 1) it reduces the maximum operating frequency, 2) it increases the threshold dissipation and 3) it increases the adiabatic dissipation.

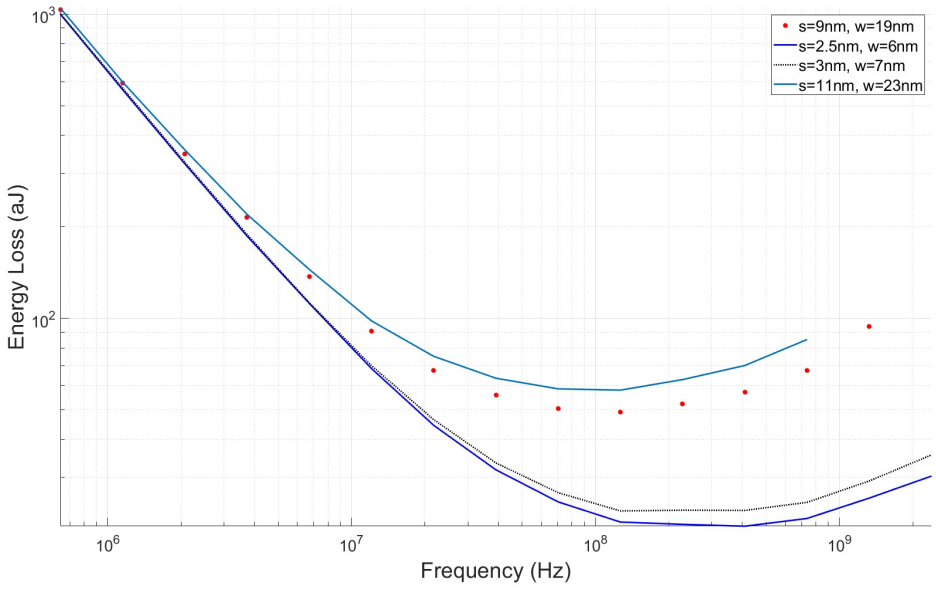

Figure 6.7 – Energy dissipation of PFAL CNT buffer as a function of the frequency for different CNTFET width and CNT spacing values.

In conclusion, we set the parameters to their minimum values i.e. N = 3, $w = 6nm$, $s = 2.5nm$ and $d = 1nm$ in order to minimize the energy dissipation of the PFAL buffer. With this configuration, a PFAL CNTFET buffer dissipates $20.8aJ$ per cycle at an operating frequency of $400MHz$.

6.3 Comparison with PFAL CMOS buffer

In this section, we compare the PFAL CNTFET buffer with the PFAL CMOS 45nm buffer in order to highlight the potential benefits to use CNTFET adiabatic logic. We choose to compare the CNTFET buffer with CMOS 45nm as they have the same supply voltage, i.e. V_{DD} = 1V. We use the same test bench for the two type of buffer, which is represented in Fig.6.3.b.

CNTFETs have the parameters selected in the previous section and MOSFETs have the minimum length and width available in 45nm node, i.e. L = $45nm$ and W = $120nm$.

6.3.1 Comparison at Nominal V_{DD}

In this subsection, we compare PFAL CNTFET buffer with PFAL CMOS 45nm buffer, which both are supplied under their nominal supply voltage, i.e. V_{DD} = 1V. In this subsection,

MOSFETs have high V_{TH} as these MOSFETs are the most efficient option for V_{DD} = 1V as we described in Section 2.4.2.2. Fig.6.8 shows the energy dissipation of the two types of PFAL buffer as a function of the operating frequency.

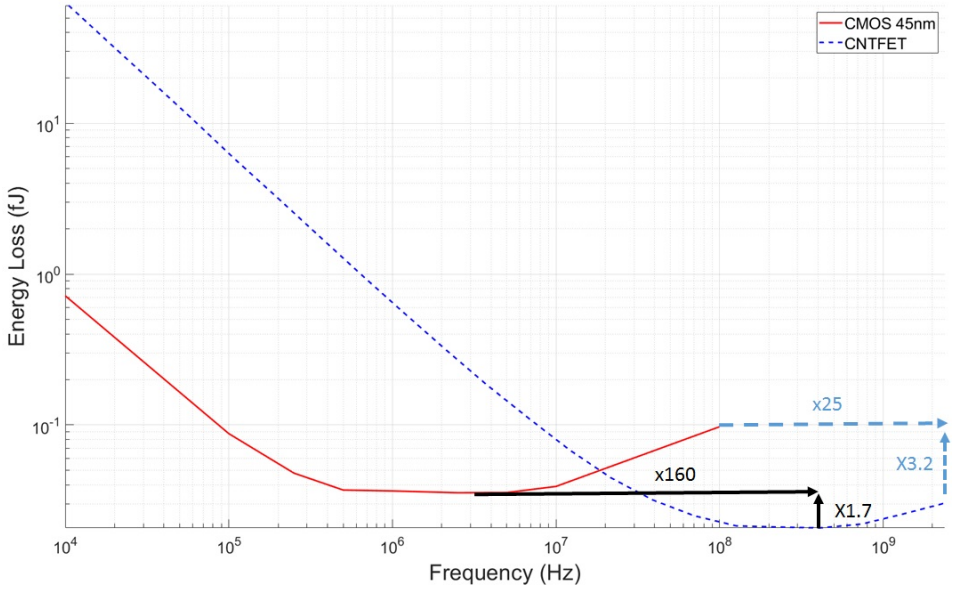

Figure 6.8 – Energy dissipation of PFAL buffer using CMOS or CNTFET transistors as a function of the frequency.

For a frequency between $10kHz$ and $100kHz$, leakage losses are predominant on both buffer dissipations. As the slope of the CNTFET energy dissipation curve is higher than the CMOS energy dissipation one, we can assume that PFAL CNTFET logic has more leakage than the CMOS PFAL logic.

The maximum operating frequency of the PFAL CNTFET buffer is $2.5GHz$. At this frequency, the buffer dissipates $30.3aJ$ per cycle. The maximum operating frequency of the PFAL CMOS buffer is $100MHz$. The buffer dissipates $97.3aJ$ per cycle. Hence, the PFAL CNTFET buffer can run at a maximum operating frequency 25 times higher than the CMOS buffer while its energy dissipation it 3.2 times less.

The optimal energy dissipation of the PFAL CNTFET buffer, which is $20.8aJ$ per cycle, occurs for a frequency of $400MHz$. The optimal energy dissipation of the PFAL CMOS buffer, which is $35.5aJ$ per cycle, occurs for a frequency of $2.5MHz$. Hence if the PFAL CNTFET buffer operates at its optimal frequency, which is 160 higher than the CMOS optimal frequency, it dissipates 1.7 times less energy than the CMOS buffer.

PFAL CNTFET buffer is the most efficient option when the operating frequency is higher

than 18MHz. The reason behind is that CNTFETs have a higher leakage current than CMOS 45nm. Thus, for lower frequency, PFAL CMOS logic dissipates less energy.

6.3.2 Comparison at Optimal V_{DD}

In this subsection, we compare PFAL CNTFET buffer with PFAL CMOS 45nm buffer which both are supplied by their optimal supply voltage, i.e. V_{DD} = 0.7V for CNTFET and V_{DD} = 0.5V for CMOS 45nm. In this subsection, CMOS have low V_{TH} as these CMOS are the most efficient option for V_{DD} = 0.5V as we see in Section 3.4.2.2. Fig.6.9 shows the energy dissipation of the two types of PFAL buffer as a function of the operating frequency.

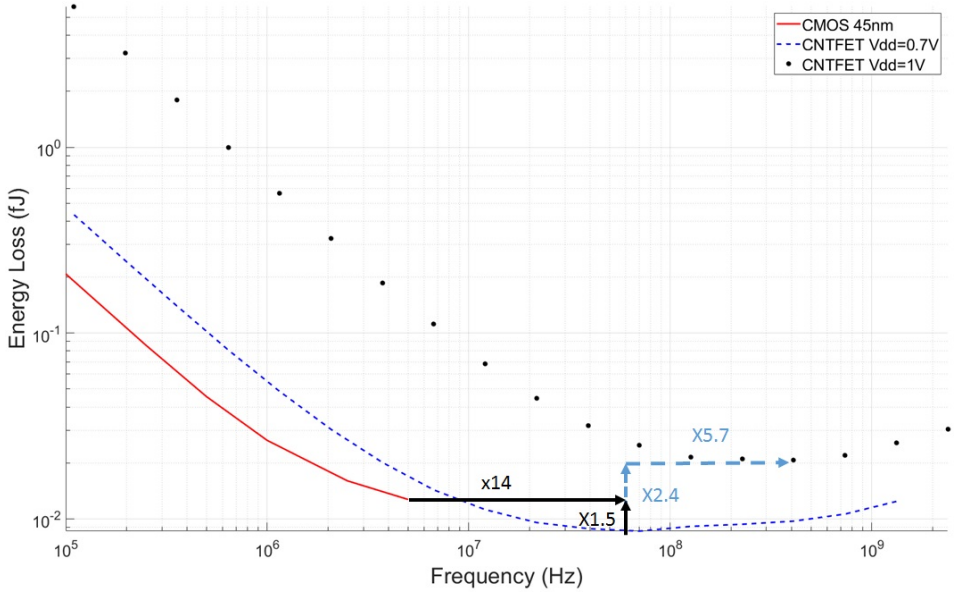

Figure 6.9 – Energy dissipation of PFAL buffer using CMOS or CNTFET transistors as a function of the frequency for optimal V_{DD}.

Lowering V_{DD} from 1V to 0.7V decreases the overall energy dissipation as V_{DD} impacts the energy dissipation in three ways: 1) it decreases the adiabatic dissipation Eq.(6.3), 2) it decreases the leakage dissipation Eq.(6.3), 3) it decreases the leakage current. Hence, decreasing V_{DD} modifies the optimal energy frequency. As the leakages have a lesser impact, the optimal frequency decreases. With V_{DD} = 0.7V, the PFAL CNTFET buffer dissipates 8.6aJ per cycle for an optimal operating frequency of 70MHz. The optimal frequency is 5.7 times lower but the buffer dissipates 2.4 times less energy thanks to the V_{DD} reduction.

The reduction of V_{DD} also impacts the maximum operating frequency, which is 1.25GHz. However, for $f \leq$ 1.25GHz, PFAL CNTFET buffer dissipates less energy if it is supplied with V_{DD} = 0.7V. Hence, PFAL CNTFET buffer benefits from the reduction of the supply voltage.

The optimal V_{DD} for CMOS 45nm buffer is 0.5V. In such conditions, the optimal frequency is the maximum operating frequency, which is 5MHz. The PFAL CMOS buffer dissipates 12.7aJ per cycle. Hence if the PFAL CNTFET buffer operates at its optimal frequency, which is 14 times higher than the CMOS optimal frequency, it dissipates 1.5 times less energy than the CMOS buffer.

However, CMOS 45nm is a better option for a frequency $f \leq$ 5MHz as PFAL CMOS buffer have less leakage dissipation.

To summarize, with CNTFET, PFAL buffers can dissipate less energy while running at a higher frequency, which is promising for high performance, low energy applications. CNTFETs have a higher leakage current than CMOS 45nm. Hence, the PFAL CNTFET buffer dissipates more energy than the PFAL CMOS ones for lower frequency. They benefit both from the supply voltage reduction. Finally, a PFAL CNTFET buffer, supplied under V_{DD} = 0.7V, dissipates 8.6aJ per cycle et the operating frequency of 70MHz, which is 4 times less than a PFAL CMOS buffer, supplied under V_{DD} = 1V.

In order to be able to compare the performance of each PFAL configuration, we introduce the figure of merit Energy Delay Product (EDP). In conventional logic, EDP is a metric to compare the performance of digital circuits [87]: the lower the EDP, the better the digital circuit. EDP is defined as the delay times the energy. As the delay is induced by the 4 phases of the power-clock, we expressed EDP for adiabatic logic as:

$$\text{EDP} = \text{E.T} \tag{6.4}$$

where E is the energy dissipation of the adiabatic logic circuit and T the ramp time.

As the energy is frequency dependent, EDP is also frequency dependent. In order to be able to compare two different types of adiabatic logic, we compare EDP at the optimal frequency, i.e. the frequency where the energy dissipation is minimized.

PFAL CNTFET buffer supplied under V_{DD} = 1V has an EDP of 13$aJ.ns$ while a PFAL CMOS buffer supplied by the same V_{DD} has an EDP of 3550$aJ.ns$. Thus, it means that the per-

formance of PFAL CNTFET buffer is 273 times higher than the one of PFAL CMOS buffer. The EDP of PFAL CMOS buffer supplied under V_{DD} = 0.5V is $635aJ.ns$. Even under the optimal conditions of the PFAL CMOS buffer, PFAL CNTFET performs 49 times better than the PFAL CMOS buffer. Using EDP, PFAL CNTFET buffer has a better performance when V_{DD} = 1V than when V_{DD} = 0.7V. Indeed, PFAL CNTFET buffer supplied under V_{DD} = 0.7V has an EDP of $31aJ.ns$, which means that the buffer is 2.4 times less performant than when it is supplied under V_{DD} = 1V: the reduction of the supply voltage has a higher impact on the operating frequency than on the energy dissipation, which causes a higher EDP.

Table 6.1 lits different characteristics of each PFAL buffers, such as the maximum operating frequency, the optimal energy dissipation and its associated frequency, the EDP and the frequency range where the types of transistors and the supply voltage are the best options in terms of energy dissipation.

Table 6.1 – COMPARISON BETWEEN PFAL CNTFET AND CMOS BUFFERS

PFAL	Maximal operating frequency (GHz)	Optimal operating frequency (MHz)	Optimal energy dissipation (aJ)	EDP (aJ.ns)	frequency range
CNTFET, V_{DD} = 1V	2.5	400	20.8	13	$f \geq 1.25\text{GH}z$
CNTFET, V_{DD} = 0.7V	1.25	70	8.6	31	$5\text{MHZ} \geq f \leq 1.25\text{GH}z$
CMOS, V_{DD} = 0.5V	0.05	5	12.7	635	$30k\text{H}z \geq f \leq 1.25\text{GH}z$
CMOS, V_{DD} = 1V	0.1	2.5	35.5	3550	$f \leq 30k\text{H}z$

6.4 Conclusion

In this chapter, we evaluate a promising architecture for adiabatic logic: positive feedback adiabatic logic using carbon nanotubes field effect transistors, CNTFET. CNTFET is a transistor, where its gate is controlling the resistance of a carbon nanotube, CNT, instead of a doped silicon channel like the CMOS.

The aim of this chapter is to highlight the potential benefits to use CNTFETs. Thus, we develop a PFAL logic buffer using CNTFETs. Thanks to the Stanford model, we show the impact of the CNTFET width, the spacing between two CNTs, and the CNT diameter on the energy dissipation of a PFAL CNTFET buffer. In addition, we optimize these parameters in order to minimize the energy dissipation. The result of this optimisation is that we have to set the parameters to their minimum values.

Then, we compare the energy dissipation of a PFAL designing with CNTFETs with a PFAL using CMOS 45nm. As a first step, the two PFAL are supplied by the same supply voltage V_{DD} = 1V. The comparison main results are:

— CNTFET have a higher leakage current than the CMOS 45nm. Hence, the PFAL CNTFET buffer dissipates more energy than a PFAL CMOS buffer for the lowest frequencies.

— For a frequency $f \geq 18\text{MH}z$, PFAL CNTFET buffer dissipates less energy than the CMOS buffer.

— The optimal dissipation of a PFAL CNTFET buffer is $20.8a\text{J}$, which is 1.7 times lower than a CMOS buffer energy dissipation. In addition, the PFAL CNTFET optimal frequency is 160 times higher than the CMOS buffer one.

As a second step, we determine the optimal supply voltages for each buffer, which are V_{DD} = 0.5V for the CMOS and V_{DD} = 0.7V for the CNTFET. Then, we compare the energy dissipation of the two types of buffer. They benefit both from the voltage supply reduction, and the PFAL CNTFET buffer is still the buffer, which dissipates the lowest energy and have the highest optimal frequency. The PFAL CNTFET buffer dissipates $8.6a\text{J}$ per cycle for an operating frequency of $70\text{MH}z$.

We introduce a figure of merit, the energy delay product (EDP). EDP is a metric, which multiplies the energy with the delay to assess the circuit performance. With this metric, we identify the best configuration to use PFAL, which is CNTFET-based PFAL supplied by V_{DD} = 1V. With such configuration, PFAL buffer has a performance 273 times higher than a PFAL CMOS buffer. In conclusion, PFAL CNTFET is a promising architecture for adiabatic logic for high performance and low energy dissipation applications.

CHAPTER

7 Conclusion

In this chapter, we aim to conclude this thesis and to present the perspective of the future of the energy efficiency research axes. Adiabatic switching is a promising design style, which can reduce the dynamic energy dissipation in digital electronics. It decreases the energy dissipation thanks to two principles: 1) the stored energy in the gate capacitance is recovered and 2) the capacitance is charged by a ramp voltage, which is the most energy-efficient way. In order to fulfill these principles, adiabatic logic needs 4 different power signals, which are also clock signals and known as power-clock. The aim of this thesis is to study the power-clock signals. There are two objectives in this thesis: 1) Design a power-clock supply and 2) Optimize the power-clock delivery network. The rest of the chapter is organized as follows: we present conclusions on each chapter in the conclusion section. In the perspectives section, we present our perspectives for the future of adiabatic logic, then we present our perspectives for the future in the research of the energy efficiency.

7.1 Conclusion

In this section, we present the main contributions of each chapter.

Chapter 2: Principle of Adiabatic Logic and its Challenges

The second chapter presents the state of the art of the adiabatic logic and its challenges. The energy dissipation of an adiabatic logic gate is the sum of three energy dissipation: the adiabatic, the leakage, and the threshold dissipation. The adiabatic dissipation is proportional to the frequency, while the leakage dissipation is inversely proportional to the frequency. Thus, there is an optimal frequency to limit the two dissipations. The thresh-

old dissipation is a frequency-independent dissipation, which comes from the non-fully discharge of the gate capacitor.

Thanks to the state of the art, we select Positive Feedback Adiabatic Logic, PFAL, as the tested logic for our power-clock study. We optimize the PFAL buffer energy dissipation with the following parameters: the CMOS node technology, the threshold voltage and the supply voltage. The result of this optimization is that we select CMOS Low-V_{TH} 45nm to design the buffer, which ideally dissipates $13aJ$ per cycle at an optimal frequency of $5MHz$.

Chapter 3: Study of the Power-Clock Network

The third chapter presents the Power-Clock Network, PCN, which is simultaneously the power delivery network and the clock network. A state of the art on these networks points the issues a PCN may have: the power-clock signal delay, the IR drop and the power-clock noises.

We divided the study of the PCN in two steps: we study its impact on a single gate, then on multi gates.

Thanks to the study of the PCN on a single gate, we model the gate energy dissipation with respect to the gate passive, the PCN resistance and the operating frequency. In order to show the PCN impact, we derive three constraints on the PCN resistance: R_5, R_{999} and R_{CRIT}. R_5 limits the additional energy dissipation due to the PCN within 5% of the ideal gate energy dissipation. R_{999} is the highest PCN resistance, where the gate capacitance is fully charged. And R_{CRIT} is the highest PCN resistance, where the adiabatic gate dissipates less energy than an ideal classic gate. The other result of this study is that we ensure that the adiabatic dissipation can be expressed as $E_{AL} = 2\frac{RC}{T}CV_{DD}^2$ where the resistance is the sum of the gate and the PCN resistance.

The study of the impact of the PCN on multi-gates leads to a design guideline in order to size PCN to optimize the energy dissipation. From the study, we derive maximum PCN resistance and capacitance value with respect to the operating frequency, the number of gates and the additional energy dissipation tolerance. In the design guideline, we propose PCN grids parameter in order to have lower parasitic than the value we have derived.

Chapter 4: Study of the Power-Clock Supply

The fourth chapter presents the power-clock supply. The power-clock supply generates a 4 phase signal. We present a state of the art of the power-clock supply. The result of this state of the art is that they are two power-clock supplies families: capacitive-based or inductive based supplies. We choose to study inductor based power-clock supplies.

We study the power-clock supply with two cases. In the first case, the power-clock has to supply a CMOS 45nm PFAL pipeline and has a supply voltage of 0.5V and an operating

frequency of 5MHz. In the second case, the power-clock supplies a CMOS 65nm PFAL pipeline with a supply voltage of 1.2V and an operating frequency of 2.5MHz.

We propose a new inductive power-clock supplies topology. The novelty lies in the synchronization of each power-clock supply.

In the first case, we optimize the topology in order to minimize the energy dissipation. The result is that a 1-stage CMOS 45nm PFAL pipeline dissipates 167aJ per cycle at 5MHz, which is 2.9 times less energy dissipation than a CMOS 45nm classic pipeline. However, there is more direct charging than expected at the end of the evaluation phase, which detriments the energy efficiency.

We investigate on the discrepancy between the model and the simulations and the result is that the gate resistance cannot be modeled as a constant resistance when the supply voltage is not at its nominal value.

In the second case, we also optimize the topology. The result is that a 1-stage CMOS 65nm PFAL pipeline dissipates 433aJ per cycle at 2.5MHz, which is 3.23 times less energy dissipation than a CMOS 65nm classic pipeline.

Chapter 5: Design of a CMOS Adiabatic Circuit

The fifth chapter presents the realization of an adiabatic circuit, which is designed in CMOS 65nm. It is composed of a PFAL pipeline and 4 power-clock supplies and their control. The circuit is tape-out ready.

In order to evaluate the energy dissipation, we extract the parasitic of PCN and we made a model to include the dissipation of the pipeline, the PCN and the power-clock supplies. The result is that the circuit, which is composed of a 123952-stage pipeline, 4 power-clock networks and 4 power-clock supplies and their control, dissipates 59.2pJ per cycle. The pipeline represents 33.8% of the energy dissipation, power-clock supplies represent 57.9% and the power-clock networks represent 8.3%. The pipeline which has a supply voltage of 1.2V and an operating frequency of 2.5MHz dissipates 3 times less energy than an ideal classic pipeline.

Chapter 6: Adiabatic Logic Beyond CMOS

The sixth chapter presents a promising adiabatic logic family: Carbon Nanotube Field Effect Transistor, CNTFET, PFAL. We replace CMOS transistors with CNTFET ones. In order to evaluate the PFAL CNFET logic, we use the Stanford model for CNTFET. We optimize its parameters in order to minimize the energy dissipation.

We compare PFAL CNTFET buffer with PFAL CMOS 45nm buffer. The results of this comparison are: 1) PFAL CNTFET has higher leakage dissipation, thus PFAL CMOS has a better energy efficiency for lower frequency, i.e. $f \geq 18\text{M}hz$. 2) PFAL CNTFET benefits from the

supply voltage reduction. At a nominal supply voltage, i.e. V_{DD} = 1V, the maximal operating frequency of the PFAL CNTFET is 2.5GHz. At the optimal frequency f = 400MHz, the PFAL CNTFET buffer dissipates 20.8aJ. The PFAL CNTFET buffer has a higher optimal frequency and a lower energy dissipation. It follows the same trend with the reduction of the supply voltage: the PFAL CNTFET buffer dissipates 8.6aJ per cycle for an operating frequency of 70MHz.

In order to assess the performance of such adiabatic logic, we introduce the energy delay product. Thanks to this figure of merit, we show that a CNTFET-based PFAL supplied by V_{DD} = 1V has a performance 273 times higher than a PFAL CMOS buffer.

7.2 Perspectives

7.2.1 Perspectives on Adiabatic Logic

In order to increase the energy efficiency of adiabatic logic circuits, researchers can work on three main axes: develop new switch devices, design or optimize logic style and improve the energy efficiency of the power clock.

This thesis highlights the major impact on the energy efficiency of the threshold voltage. Due to the threshold voltage, the energy, which is stored in the gate in order to transmit the information, cannot be fully recovered. In addition, the threshold voltage also decreases the power-clock energy efficiency when the adiabatic circuit is supplied with a near threshold voltage. Thus, a good candidate for replacing CMOS should have a low V_{TH}/V_{DD} ratio such as CNTFET. Adiabatic principle is based on charging the gate capacitance with a ramp time at the lowest frequency possible. However, the leakage current decreases the energy frequency. Thus, the candidate device should also have low leakage current such as NEMS.

Another way to improve the energy efficiency of the adiabatic logic is to work on design logic style. In our project, researchers promote the idea that the adiabatic logic energy dissipation is increased by the switch itself. Thus, they develop a capacitive-based logic in order to improve the energy efficiency using NEMS as high ratio capacitance [53]. Further objectives are to study the impact of the NEMS scaling and to propose efficient power-clock supply for capacitive-based logic. Another research axis on the design style is to develop techniques using fully-adiabatic gate to design adiabatic circuit, i.e. an adiabatic logic, which has no threshold dissipation.

The power-clock topology we have proposed in this thesis dissipates 58% of the total circuit energy dissipation. Power-clock supplies will benefit from the improvement of the component integration such as the inductor. The main issue with power-clock energy efficiency is the synchronization. In order to ensure the functioning of an adiabatic circuit, the 4 power-clock have to be synchronized between themselves. In this thesis, the way we handle the synchronization is to add a control switch between each inductance and power-

clock networks. The problem with this solution is that the switch is in the conduction path, thus it lowers the energy efficiency. Power-clock supply energy efficiency will benefit from a synchronization solution without this switch.

7.2.2 Perspectives on the Energy Efficiency Research

Power density has become the primary concern when a digital core is designed. As in any embedded systems, each new digital core generation has more applications than the previous one and ultimately demands more power density. This is why many researchers and industrial designers have been looking into novel methods for increasing energy efficiency of digital circuit. Such efforts are concentrated into three main axes: novel technologies and devices, circuit- and system-level design and new architecture design style.

The first step to increase the energy efficiency is to propose more energy efficient switching devices. With the CMOS scaling, CMOS devices have become leakier and harder to control due to the short channel effect (SCE). In order to limits SCE, bulk CMOS have been replaced by FDSOI and FinFET for technology node below 22nm. The latest technology node is 18nm for FDSOI and 7nm for FinFET. As these technology nodes should be the last ones, the switching devices scaling should continue with other devices. Researchers have proposed new types of switching devices such as CNTFET or VeSFET. Future research should be focused on reliability, performance and scalability of such devices.

Storage data is the most energy consuming activity in embedded circuits. In order to reduce the energy dissipation, researchers have focused their studies on SRAM because it is a non-volatile memory: using SRAM reduces the dynamic dissipation. SRAM benefits from the devices scaling. Thus, using new devices, such as CNTFET, should increase the data storage density and the energy efficiency. Another axis to increase the data storage energy efficiency is to develop techniques to limit the leakage energy dissipation, which is a predominant energy dissipation for these kind of devices.

At a gate level, interconnect lowers the energy efficiency because they add parasitics, which lower the performance and increase the energy dissipation. Scientists have focused their research on replacing copper interconnect by new kind of interconnects. The two most advanced solutions are: carbon nanotube-based and optical interconnects. Researcher will focus on evaluating the performance of such interconnects and their reliability.

At circuit-level, a way to increase the energy efficiency is to use adiabatic logic. Adiabatic logic has not been taking into consideration to design digital blocks due to its lack of performance with CMOS. With the emergence of new switching devices, especially CNTFET, adiabatic logic will gain in performance as we have shown in Chapter 5. Adiabatic logic will have the same order of performance for a much lower energy dissipation, thus it should be evaluated as a potential replacement for conventional logic.

Historically, Von Neumann architecture is the main used architecture to compute data.

However, with the increased need to store data for more complex applications, the energy efficiency is impacted by the communication between the data storage and the processor. In order to limit the energy dissipation at an architecture-level, there are two main axes: 1) limit the interactions between the processor and the data storage or 2) rethink the overall architecture.

Probabilistic computing investigates the first solution. It reduces the interactions between the processor and the data storage by predicting the result of the functional block. This prediction induces error in the data processing, thus it is limited to error tolerant applications such as image processing. Probabilistic computing will gain in energy efficiency with more energy efficient devices and better predictive algorithms.

The second axis, rethink the architecture, is carried out in three main ways of computing data: the optical computing, the quantum computing and the neuromorphic computing. Optical computing replaces electronic devices by optical devices. Researcher have developed all-optical gates, optical interconnects and logic gate in order to develop a computing made with optical signals. The future on optical computing is to design new logic style and evaluate the performance and the reliability of such computing.

Brain has better performance to compute data with a higher energy efficiency than any digital circuit. The aim of neuromorphic computing is to study and replicate the way brain computes data. A neuromorphic system is composed with neurons, dendrites and synapses. Researchers have developed electronics synapses, and design styles to replicate neurons. However, the energy efficiency of such systems is lower than the brain energy efficiency. The future of neuromorphic computing is to improve the neuromorphic architecture in order to decrease the energy consumption.

Quantum computing is a promising energy efficient and high performance computing, which relies on the quantum information theory. Quantum computing relies on the quantum information theory. The quantum computing principle is to store data in the electron spin instead of storing the data with a voltage level. The data is stored in a qubit. The future of the quantum computing lies in two main things: 1) How to increase the number of qubit in quantum systems. IBM has developed a quantum computer with 5 qubits only and 2) How to read and write efficiently the data in a multiple-qubits storage systems due to the Heisenberg principle.

APPENDIX

A Curriculum Vitae

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Nicolas Jeanniot

Microelectronics Engineer, PhD

Experience

Since Nov. 2015 - 3 years, PhD student in Microelectronics
LIRMM, Montpellier, France
Design and **optimization** of a power-clock supply and its distribution network for **adiabatic circuits**. Optimization of the energy efficiency of adiabatic logic gates using PSPICE and Cadence. Study of the **impact** of the distribution network on the energy efficiency thanks to simulations and modeling. **Modeling** the control logic of the power-clock supply using VerilogA. **Realization** of an ASIC : an adiabatic pipeline and its 4 power-clock supplies in TSMC 65 nm.
Contact: aida.todri@lirmm.fr

2015 - 6 months, Research Scientist
CEA-LETI, Grenoble, France
Study of **DC-DC capacitive converter** 2:1. Optimization and comparison of this converter as a function of different technology nodes such as CMOS (180 nm, 65 nm et 28 nm FDSOI).
Contact: gael.pillonnet@cea.fr

Since Jan. 2014 - 5 years, French Community Manager
InnoGames
Managing a team of 10 persons in customer support. In charge of social networks.
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Jul. 2012 - Jun. 2013 - 1 year, Application Engineer
Analog Devices Inc., Limerick, Irlande
In charge of **testing** and **debugging** circuits using HART protocol. Conception and realization of 4 universal industrial inputs for sensors. Creation of a LabVIEW program to **test** this circuit.
Contact: michal.brychta@analog.com

Education

2015 - 2018, Microelectronics PhD
Université de Montpellier, Montpellier, France

2010 - 2015, Master of Engineering "Diplôme d'Ingénieur" CPE Lyon
CPE Lyon, Lyon, France
Major: Embedded Systems Engineering

2014 - 2015, Master of Sciences
Université Claude Bernard Lyon 1, Lyon, France
Major: Electronics and Embedded Systems

Languages

French Mothertongue

English C1 Level - CAE (Certificate of Advanced English of Cambridge) passed in 2015

Italian B2 level

Skills

Cross-functional Skills Teamwork - Autonomous - Team Management - Tact

Technical Skills Analog Design - Power Management in Integrated Circuit - Ultra Low Power Digital Electronics - Data Analysis

Word processing LaTeX - Suite Microsoft Office

Scripting Ocean - Shell

Data processing Matlab

Electrical simulations Cadence - Eldo - Pspice - Spectre - Virtuoso

Behavioral simulations VerilogA - VHDL

Test LabVIEW

Hobbies

Sports Rugby (Team Captain) and Fencing

Others Forest Harvesting

APPENDIX

B Author Publications

B.1 Journal

N. Jeanniot, R. Chen and A. Todri-Sanial, “Exploring the advantages of carbon nanotubes field effect transistors for adiabatic logic,” *in preparation target: TNANO*, 2018.

N. Jeanniot and A. Todri-Sanial, “Investigating power-clock network of adiabatic circuits,” *in preparation target: TVLSI*, 2018.

B.2 International Conference

G. Pillonnet, N. Jeanniot and P. Vivet, "3D ICs: An opportunity for fully-integrated, dense and efficient power supplies," in *2016 International 3D Systems Integration Conference (3DIC)*, 2016.

G. Pillonnet and N. Jeanniot, "Effect of CMOS Technology Scaling on Fully-Integrated Power Supply Efficiency," in *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*, pp. 1-5, 2016.

N. Jeanniot, G. Pillonnet, P. Nouet, H. Fanet, and A. Todri-Sanial, “Analyzing power-clock network parasitic on adiabatic logic,” in *2016 Workshop on Integrated Power Conversion and Power Management (PwrSoC)*, 2016.

N. Jeanniot, A. Todri-Sanial, P. Nouet, G. Pillonnet, and H. Fanet, "Investigation of the power-clock network impact on adiabatic logic," in *2016 IEEE 20th Workshop on Signal and Power Integrity (SPI)*, pp.1-4, 2016, doi: 10.1109/SaPIW.2016.7496270.

N. Jeanniot, G. Pillonnet, P. Nouet, N. Azemard, and A. Todri-Sanial, "Synchronised 4-phase resonant power clock supply for energy efficient adiabatic logic," in *2017 IEEE International Conference on Rebooting Computing (ICRC)*, pp. 1–6, Nov 2017,doi: 10.1109/ICRC.2017.8123661.

B.3 National Conference

N. Jeanniot, G. Pillonnet, P. Nouet, H. Fanet, and A. Todri-Sanial, "Impact of the power-clock network on adiabatic logic," in *Colloque 2016 du groupe de recherche System on Chip - System in Package (SOC-SIP)*, 2016.

N. Jeanniot, G. Pillonnet, N. Azemard, P. Nouet, and A. Todri-Sanial, "4-phase resonant power-clock supply for adiabatic logic," in *Colloque 2017 du groupe de recherche System On Chip, Systèmes Embarqués et Objets Connectés - System in Package (SOC2)*, 2017.

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Abstract

Power density has become the primary concern when a digital core is designed. As in any embedded systems, each new digital core generation has more applications than the previous one and ultimately demands more power density. This is why many researchers and industrial designers have been looking into novel methods for reducing power consumption of digital circuit. Adiabatic logic is a promising design style, which can reduce the dynamic energy dissipation. Adiabatic logic is different than conventional logic in two main points: 1) adiabatic gate are charged with a 4-phase power signal, and 2) the energy, which is stored in the gate, is recovered. In order to fulfill these principles, the adiabatic logic needs a special power supply. As the purpose of such supply is to act as a clock also, it is referred as power-clock supply. The aim of this thesis is to design and optimize a power-clock supply and its delivery network. This thesis has been funded by the French National Research Agency, ANR, with the project ADIANEMS2 (Grant number: ANR-15-CE24-0013).

Keywords: *adiabatic logic, energy efficiency, power-clock supply, power-clock network*

Résumé

La densité de puissance est devenue la principale préoccupation lorsqu'un circuit numérique est conçu. Comme pour tous les systèmes embarqués, chaque nouvelle génération de système numérique a plus d'applications que la précédente et exige en fin de compte une plus grande densité de puissance. C'est pourquoi de nombreux chercheurs et concepteurs industriels se sont penchés sur de nouvelles méthodes de réduction de la consommation énergétique des circuits numériques. La logique adiabatique est un style de conception prometteur qui peut réduire la dissipation d'énergie dynamique. La logique adiabatique est différente de la logique conventionnelle en deux principaux points : 1) l'alimentation d'une porte logique adiabatique est un signal à 4 phases, et 2) l'énergie stockée dans la porte est récupérée. Afin de respecter ces principes, la logique adiabatique nécessite une alimentation spéciale. Étant donné que l'objectif d'une telle alimentation est d'agir comme une horloge, elle est appelée alimentation-horloge. L'objectif de cette thèse est de concevoir et d'optimiser une alimentation-horloge ainsi que son réseau de distribution. Cette thèse a été financée par l'Agence Nationale pour la Recherche, ANR, avec le projet ADIANEMS2 (numéro de subvention : ANR-15-CE24-0013).

Mots clefs : *logique adiabatique, rendement énergétique, génération d'alimentation-horloge, réseau de distribution d'alimentation horloge*

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