Development of thermally assisted MRAMs: from basic concepts to industrialization

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Development of thermally assisted MRAMs: from basic concepts to industrialization

présentée par

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Summary

In the first part of this manuscript, I will show how thermal assistance can be implemented in field induced switched MTJ to enhance the reliability and the scalability of MRAM. A new self-referenced reading scheme can be implemented in such MTJ in order to obtain a Magnetic Logic Unit that present new logic functionalities compared to standard MRAM. In a second time, I will present the implementation of thermal assistance in MTJ with current induced switching writing scheme. In that case, no field line is required, increasing thus the storage capacity of MRAM cell and decreasing the writing consumption while keeping a satisfying data retention capacity. Ultimately, thermal assistance can be implemented in MTJ with perpendicular magnetization. In that case, thermally induced anisotropy reorientation (TIAR) can be used to decrease the switching power consumption, increase the writing reliability and further improve the scalability of TAS-MRAM down to the 22nm technological node.

The second part will be dedicated to the description of my future research projects for the forthcoming years linked mainly to applied aspects of the magnetic tunnel junctions for: sub-20nm scalable MRAMs, hybrid logical circuits and innovative magnetic field sensors.

Finally I will present my short bio, my CV, a detailed list of all the PhD supervising activity, as well as a complete list of publications after PhD.

Keywords

- Spintronics
- Tunnel magnetoresistance
- Magnetic tunnel junctions
- MRAM,
- Non-volatile memories
- Magnetic multilayers
- Thin films
- Thermal properties
- Exchange bias
- Perpendicular magnetic anisotropy

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PART I

1. INTRODUCTION

1.1 STATUS OF EMERGING NONVOLATILE MRAM MARKET

Demand for on-chip memories has been recently increasing due the growth in demand for data storage and the increasing gap between processor and off-chip memory speeds. **One of the best solutions to limit power consumption and to fill the memory gap is the modification of the memory hierarchy by the integration of non-volatility at different levels** (storage class memories, DRAM main working memory, SRAM cache memory), which would minimize static power as well as paving the way towards normally-off / instant-on computing (logic-in-memory architectures) (see *Figure 1.1*). Besides computers, today's portable electronics have become intensively computational devices as the user interface has migrated to a fully multimedia experience. To provide the performance required for these applications, the actual portable electronics designer uses multiple types of memories:

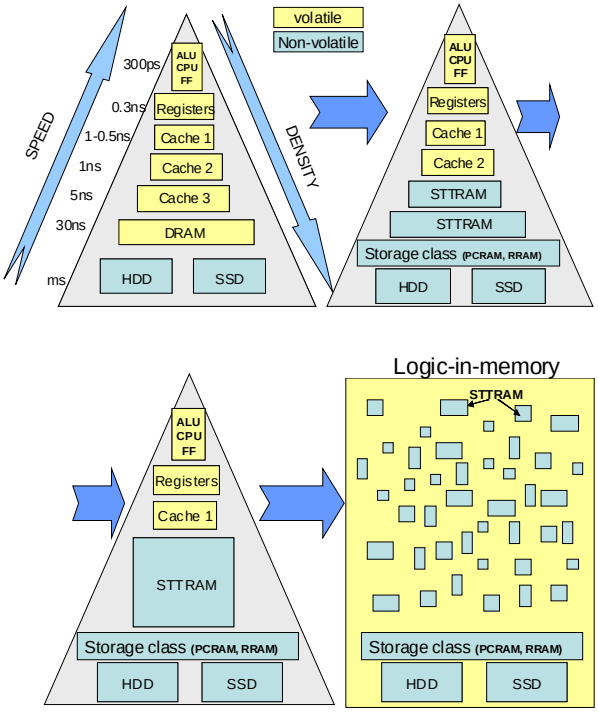


Figure 1.1: Expected evolution of memory architecture from present hierarchy to logic-in-memory architecture

- a medium-speed random access memory for continuously changing data,
- a high-speed memory for caching instructions to the CPU and
- a slower, nonvolatile memory (NVM) for long-term information storage when the power is removed.

Combining all of these memory types into a single memory has been a long-standing goal of the semiconductor industry, as computing devices would become much simpler and smaller, more reliable, faster and less energy consuming. As a result, advanced NVM chips are expected to see phenomenal growth in the forthcoming years. **MRAM is one of a number of new technologies aiming to become a "universal" memory device applicable to a wide variety of functions.** MRAMs are expected to combine nonvolatility, high speed, moderate power consumption, infinite endurance, and radiation hardness, all at moderate cost and be easy to embed in devices.

Since its inception in the late 1990s, MRAM have however not yet reached large volume applications, with only Toggle switching-based standalone products currently available from Everspin, at the 180 nm technology node [1].

The more recent advent of spin transfer torque (STT)[2], however, has shed a new light on MRAM with the promises of much improved performances and greater scalability to very advanced technology node. Indeed, in 2010, the International Technology Roadmap for Semiconductors (ITRS), Emerging Research Devices and Emerging Research Materials Working Groups **"identified spin transfer torque MRAM and redox RAM as emerging memory technologies recommended for accelerated research and development leading to scaling and commercialization of nonvolatile**

1 L. Savtchenko, B. Engels, N. Rizzo, M. Deherrera, J.A. Janesky, US6545906 (2001).

2 J. Slonczewski, "Currents and torques in metallic magnetic multilayers", J.Magn.Magn.Mater.159, L1 (1996); "Excitation of spin waves by an electric current ", 195, L261 (1999).

RAM to and beyond the 16 nm generation"[3]. Currently there is an intense research and development effort in microelectronics on these two technologies, one based on spintronic phenomena, the other based on migration of vacancies or ions in an insulating matrix driven by oxidation-reduction potentials. Both technologies could be used for standalone or embedded applications.

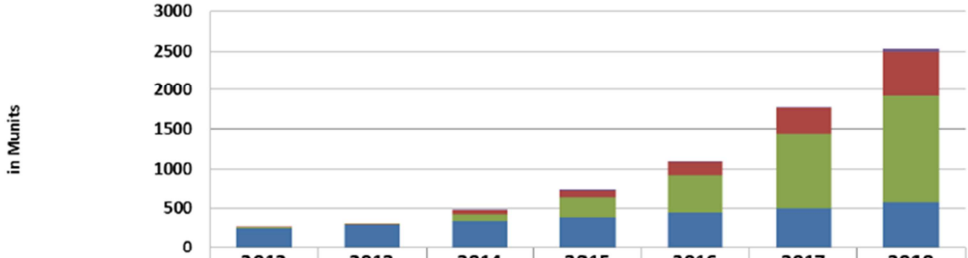
As a consequence, MRAM is now viewed as a credible replacement for existing technologies for applications where the combination of nonvolatility, speed, and endurance is key. Several start-up companies (e.g., Everspin Technologies, Grandis, Crocus Technology, Avalanche, Spin-Transfer Technology), large IC manufacturers (e.g., IBM, NEC, Toshiba, Intel, Samsung) and equipment suppliers (e.g., Canon Anelva, Singulus, Applied Materials, TEL) are now actively developing the STTRAM technology and a forthcoming launching of 64Mbit in-plane magnetized STTRAM products was recently announced by Everspin.

1.2 COMPARISON MRAM VS REDOX-RAM

The redox RAMs combine good potential for scaling below 10 nm generation, fast read and write times, (<10 ns) and relatively low write current (in the microampere range). Additionally, these nonvolatile memories should be stackable in three-dimensional architectures called cross-bar architectures and offer multilevel capabilities thanks to the possibility to control the growth/dissolution of the conducting filaments which determines the cell resistance level. However, at this point, they still suffer from a poor understanding of the underlying physical mechanisms so that no predictive model of reliability exists yet for this technology. Finally, their endurance (~10^8 cycles) is sufficient for Flash type applications but not enough for the working memory in microprocessors (which require >10^{15} cycles). Therefore, these memory elements seem to be most suited for storage class memory applications (intermediate level between hard disk drives (HDD), solid state drives (SSD) and DRAM) and memristor applications thanks to the possibility that they offer to continuously vary their resistance between a minimum and a maximum value in a hysteretic way. This may open the path to neuromorphic architectures that mimic the working principle of the human brain.

The STT-MRAM appears today as the most credible candidate for DRAM and cache replacement as it combines CMOS compatibility, high retention time (10 years), large endurance (>10^{15} cycles), and relatively fast write/read time (1-30ns depending on the architectures). However, this technology is still not yet fully mature, particularly at the smallest dimensions (sub-20 nm). The main issues remain associated with the cell-to-cell variability. This variability is mainly caused by the edge defects generated during patterning of the cells. Whenever the MgO barrier is damaged by the patterning, this yields local changes in the barrier resistance, tunnel magnetoresistance and magnetic anisotropy, i.e., cell retention. Now that the number of laboratories (including major equipment suppliers) working on this technology has substantially increased, technological progress should be faster.

3 http://www.itrs.net/Links/2010ITRS/2010Update/ToPost/ERD_ERM_2010FINALReportMemory Assessment_ITRS.pdf



	2012	2013	2014	2015	2016	2017	2018
TOTAL in M units	258	310	469	718	1103	1780	2537
RRAM	0	0	1	2	5	12	32
PCM	3	12	47	87	177	322	585
MRAM/STT MRAM	5	10	90	249	483	943	1341
FRAM	250	288	331	380	437	503	578

Figure 1.2: Emerging NVM production in Million devices will grow at a CAGR of 46% with MRAM leading the overall production in 2018. PCM will grow also rapidly. ReRAM will just start to emerge in 2017-2018.FRAM will grow at a steady state

1.3 MAIN APPLICATIONS OF MRAM

According to recent market research reports, solid-state memory constitutes a market of over $50 billion, while the nonvolatile memory (NVM) segment is much smaller. A few computers use NVMs, which retain data when the power is off, in the form of solid-state drives (SSDs) replacing traditional hard disk drives (HDDs). The now ubiquitous smart cell (mobile) phones and other handheld devices also use NVM, but there is a trade-off between cost and performance. The cheapest NVM is Flash memory, which, among other uses, is the basis of small, portable Flash memory sticks. Flash memory, however, is slow and has a limited cyclability of 10^5 cycles, sufficient for a large number of storage applications ranging from memory sticks to digital camera memory to SSDs, but much lower than that of redox-RAM or STT-MRAM.

Besides computers, today's portable electronics have become intensively computational devices as the user interface has migrated to a full multimedia experience. To provide the performance required for these applications, the portable electronics designer uses multiple types of memory: a medium-speed random-access memory for continuously changing data, a high-speed memory for caching instructions to the CPU, and a slower NVM for long-term information storage when the power is removed. Combining all of these memory types into a single memory has been a long-standing goal of the semiconductor industry. With such a memory, computing devices would become much simpler and smaller, more reliable, faster, and less energy consuming.

As a result, advanced NVM chips are expected to see phenomenal growth in the next few years, with the global market increasing from $209 million in 2012 to $2,028 million by 2018[4] - *see Figure 1.2*.

This will occur in a number of applications: embedded system-on-chip (SOC) cards; radio-frequency identification (RFID) tags used in goods transported by high-speed detection conveyors; smart airbags used in automobiles; radiation-hardened memory in aerospace and nuclear installations; printed memory platforms (such as smart cards, games, sensors, display, storage-class memory network); and high-end smart mobile phones.

MRAM is one of a number of new technologies aiming to become a "universal" memory device applicable to a wide variety of functions.

4 YOLE report on Emerging Non Volatile Memories Technologies & Markets (2013)

- As a matter of fact, MRAM can have similar performance to SRAM Cache 3 (switching time ~1 ns) but is nonvolatile.
- It has also similar density to DRAM but at much lower power consumption since there is no need to refresh and with reduced leakage since MRAM can be powered off on standby.
- Besides, it is non-volatile as Flash memory but much faster and suffers no degradation over time. It is this combination of features which makes it so attractive. Some suggest that it could replace SRAM, DRAM, some storage class memories, resulting in instant-on nonvolatile computers and tiny, super-fast and reliable portable devices.

In cell phones, handheld tablet computers, notebooks, personal digital assistants (PDAs), notebooks, and other forms of mobile computing, MRAM is an attractive alternative to deploying both Flash and DRAM since it can save money and space. With software applications residing in memory, mobile devices could rapidly power-up to exactly where they were when they were turned off. In general computing and networking, MRAM can be used to avoid boot-up delays and to provide faster access to hard drives and nonvolatile backup capabilities. At present, BIOS tend to use high cost, low density EEPROM or battery backed-up SRAM – and volatile memory is used to alleviate I/O bottlenecks. In such applications, MRAM could prove much more economical.

In factory automation systems, microcontrollers and robots typically employ both RAM and PROMs/Flash. Lower costs will be achieved by replacing these two chips with one MRAM device.

RFID tags need low-cost NVM, and a price point that makes MRAM economically viable for RFID applications will almost certainly push MRAM into other cost-sensitive areas.

For aerospace use, MRAMs are radiation-hard, meaning that they can withstand ionizing radiation in contrast to most of semiconductor memories based on the capacitor charge. This makes them suitable for use in airplanes (already in Airbus flight controllers), in satellites, and in spacecraft.

For military use, the radiation hardness makes them suitable for missiles and perhaps on battlefields where equipment could potentially be exposed to tactical weapons.

MRAM could also be used in **nuclear environment** such as nuclear power plants where conventional CMOS electronics devices fail when exposed to radiation.

1.4 Current and Future Challenges for MRAMs

MRAM technologies (*Figure 1.3*) evolved in the last years, benefiting from the progress in spintronics research, namely the tunnel magnetoresistance (TMR) of MgO magnetic tunnel junctions (MTJ)[5], the STT[6] and the spin orbit torque (SOT)[7] phenomena. The elementary cell of all these MRAM architectures is a MTJ consisting of two ferromagnetic layers separated by a thin insulating barrier and the readout (i.e. determining the magnetic state of the MTJ) is always performed by measuring the MTJ resistance. Between 1996 and 2004, most research and development focused on MRAM written by field (top line in *Figure 1.3*). Until the discovery of STT switching and its gradual implementation in MTJ after 2006, the only known way to manipulate the magnetization of a magnetic nanostructure (here the MTJ storage layer) was indeed with use of a magnetic field. The magnetic field is created by pulses of current flowing in conducting lines located below and above the MTJ. These approaches, which will be described in more detail in the next sections, actually resulted in the commercialization of the first MRAM products (1, 4, 8, and 16 Mbit MRAM chips) by Freescale Semiconductor and its spin-off Everspin Technologies in 2006. **An extension of the initial field written MRAM (*Figure 1.3a*) is**

5 S. Yuasa et al, "Giant room temperature magnetoresistance in single-crystal Fe/MgO/Fe magnetic tunnel junctions", Nature materials, (2004); S.S.P. Parkin et al, "Giant tunnel magnetoresistance at room temperature with MgO (100) tunnel barriers", Nature Materials, nmat 1256 (2004).

6 Slonczewski J C 1996, J. Magn. Magn. Mater. 159 L1-L7

7 I.M Miron. et al., Nature, 476 189 (2011)

the Thermally Assisted MRAM (TAS-MRAM)[8] (*Figure 1.3b*), proposed by Spintec and mainly developed by Crocus Technology. In TAS-MRAM, the write selectivity is achieved by a combination of temporary heating of the selected cell produced by the tunneling current flowing through the cell and a single pulse of magnetic field. The power consumption to write these memory elements is significantly reduced compared to conventional field-written MRAM thanks to the possibility of using lower magnetic fields and of sharing each field pulse among several cells so as to write several bits at once. Besides, TAS-MRAM with a soft reference allows introducing new functionalities such as the "Match In Place™", particularly promising for security and routers applications. Field-written technology is robust and is already used in a variety of applications where reliability, endurance, and resistance to radiation are important features, such as in automotive and space applications. However, **the down-size scalability provided by field-writing in conventional technology is limited to MTJ dimensions on the order of 60nm×120nm due to electromigration in the conducting lines used to generate the field.** In addition, in field-writing, the write field extends all along the conducting line where it is produced and decreases relatively gradually in space, inversely proportional to the distance to this line. As a result, unselected bits adjacent to selected bits may sense a significant fraction of the write field, which may yield accidental switching of these unselected bits.

Since the first observation of STT-induced switching in GMR metallic spin-valve pillars, the interest in using STT as a new write approach in MRAM has increased, motivated by the fact that **STT-writing (*Figure 1.3c*) offers a much better down-size scalability than field-writing as the critical current**

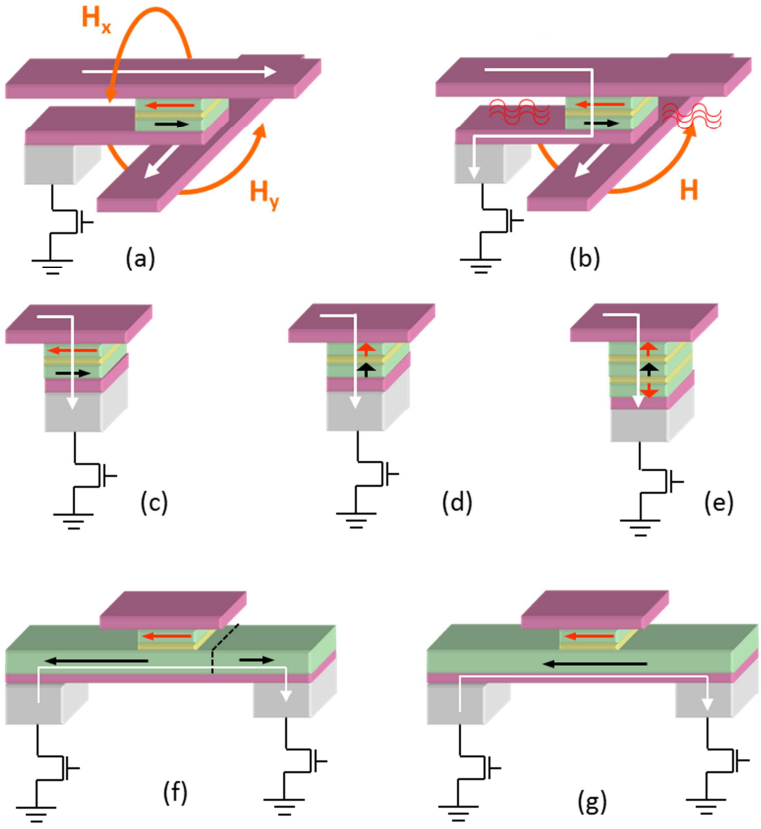


Fig.1.3 – Various MRAM technologies: toggle (a), Thermally Assisted MRAM (b), in-plane (c) and (d) out-of-plane magnetized STTRAM, p-STTRAM with double barrier(e), 3-terminal devices based on domain wall propagation (f) and SOT (g)

8 B. Dieny and O. Redon, patent FR2832542, I.L. Prejbeanu et al, IEEE Trans. Magn 40 2625 (2004); I.L. Prejbeanu, S. Bandiera, J. Alvarez-Herault, R.C. Sousa, B. Dieny and J-P Nozieres Thermally assisted MRAMs: ultimate scalability and logic functionalities J. Phys. D: Appl. Phys. 46 (2013) 074002

for writing decreases proportionally to the cell area down to a minimum value set by the retention (~15µA). Furthermore, STT provides very good write selectivity since the STT current flows through only the selected cells. The greatest interest is now focused on out-of-plane magnetized STTRAM (p-STTRAM), taking advantage of the perpendicular magnetic anisotropy which exists at the CoFeB/MgO interface (*Figure 1.3d*)[9]. **p-STT-MRAM require significantly less write current than their in-plane counterparts for a given value of memory retention and provide a better stability of the written information.** Optimized p-STTRAM stacks will likely comprise two tunnel barriers with antiparallel polarizing layers to maximize anisotropy and STT efficiency (*Figure 1.3e*). **The thermal assistance can also be combined with STT to circumvent a classical dilemma in data storage between the memory writability and its retention[10]. Recently it has been shown that assistance by an electric field may reduce the STT writing critical currents in MTJs[11].** This has been demonstrated in magnetic stacks with perpendicular magnetic anisotropy but the effect is quite weak when using metallic layers due to the electric field screening over the very short Fermi length in metals. An electrically reduced magnetic anisotropy leads to lower energy barrier that is easier to overcome for changing magnetization direction. In principle, voltage control spintronic devices could have much lower power consumption than their current-controlled counterparts provided they can operate at sufficiently low voltage (typically below 1V). Multiferroïc or ferromagnetic semiconductor materials could provide more efficient voltage controlled magnetic properties. **3-terminal MRAM cells written by domain wall propagation (*Figure 1.3f*) or SOT (*Figure 1.3g*) were also recently proposed[12] to separate write and read current paths.** This can ease the design of non-volatile logic circuits and increase the reliability of the memory. SOT-MRAM offers the same non-volatility and compliance with technological nodes below 22nm, with the addition of lower power consumption (provided the write current density can be further reduced thanks to stack optimization), cache-compatible high speed and improved endurance. The drawback is the increased cell size.

The potential benefits of spin-based memories are especially appealing when viewed in light of the exploding demand for on-chip memories. However**, spin-based devices are still in their nascent stages, particularly at the sub-20nm dimensions, and in order to realize their potential, there is a need to strengthen the technology maturity and for advances in circuit designs and innovative architectures.**

There is still a need to strengthen the technology maturity and for advances in circuit designs and innovative architectures. **The main issues remain associated with the cell to cell variability, TMR amplitude and temperature range.** Variability is mainly caused by edge defects generated during patterning of the cells. MgO damages yield local changes in the barrier resistance, TMR and magnetic anisotropy i.e. cell retention. With the increasing number of actors now working on this technology, faster technological progresses can be expected in the near future. Also, implementing self-referenced reading scheme can lead to improved tolerance to process defects. Concerning out-of-plane STTRAM, progresses are needed in the composition of the stack to minimize the write current, maximize the TMR amplitude and improve the temperature operating range. Double barrier MTJ with separately optimized interfacial and bulk properties should allow reaching the requirements for Gb STTRAM at 12nm node (Fig.1.3e). Heusler and $X_{1-x}Mn_x$ (X = Cr, V, Ge, Ga…) alloys have also already demonstrated their potential for p-STTRAM (low M_s, large perpendicular anisotropy, low damping)[13] but none of the existing alloys combine all required properties yet.

9 M. Gajek, J.J. Nowak, J.Z. Sun, P.L. Trouilloud, E.J. O'Sullivan, D.W. Abraham, M.C. Gaidis, G. Hu, S. Brown, Y. Zhu, R.P. Robertazzi, W.J. Gallagher, D.C. Worledge, Appl. Phys. Lett. 100 132408 (2012)

10 S. Bandiera, R.C. Sousa, M. Marins de Castro, C. Ducruet, C. Portemont, S. Auffret, L. Vila, I.L. Prejbeanu, B. Rodmacq and B. Dieny, Appl. Phys. Lett. 99 202507 (2011)

11 W.G. Wang et al., Nat. Mater., 11, 64 (2012)

12 I.M Miron. et al., Nature, 476 189 (2011), P.M. Braganca, J.A. Katine, N.C. Emley et al., IEEE Transactions on Nanotechnology, Volume: 8 Issue: 2 Pages: 190-195 (2009)

13 H.X. Liu et.al., Appl. Phys. Lett. 101, 132418 (2012)

Progress is also steadily being made in the composition of the stack to maximize the TMR amplitude, (now above 200 %), and in improvements in the temperature operating range (to minimize the decrease of the PMA with operating temperature). The ultimate scalability in STTRAM could be provided by combining thermally/voltage assisted switching and STT. SOT-MRAM can be viewed as a very interesting approach for non-volatile logic and MRAM of improved endurance. Voltage controlled spintronics devices may later yield devices of much reduced power consumption. As a matter of fact, there is lot of room for reducing the power consumption in MRAM technologies considering that the barrier height to insure a 10 year retention of a Gb chip is typically of $80k_BT \sim 4x10^{-4}$fJ whereas the energy presently required per STT write event is in the range 50fJ-1pJ.

1.5 HISTORICAL CONTEXT OF THIS WORK

The research of new approaches to making non-volatile memories has been a major activity of SPINTEC since its inception. SPINTEC research laboratory was established in 2000 to specifically work at valuation of upstream work in the areas of nanomagnetism and spintronics. The MRAM team in SPINTEC has proposed alternative MRAM technologies with improved performances (speed, scalability and power consumption) and avoiding problems like the write selectivity, power consumption, electromigration and thermal stability at high densities. Multiple approaches have been pursued in parallel:

- **Thermally-Assisted Switching (TAS),** as developed by our spin-off Crocus Technology which has been refined by constant materials improvements and for which lately multi-level storage has been demonstrated in a “Magnetic Logic Unit” (MLUTM).
- **Spin Transfer Torque (STT),** which has been improved by reducing the critical switching current and/or allowing reversible switching with a unipolar current.
- **The combination of TAS and STT,** which has been revisited for perpendicular magnetic tunnel junctions (viewed as the future of STT MRAM) in a new concept dubbed **Thermally-Induced Anisotropy Reorientation (TIAR)** which provides industry-record writing efficiency.
- **Precessional switching (also known as Orthogonal Spin Torque - OST)**, which was initially proposed by Spintec in 2001 and has been finally demonstrated, fulfilling its promises of ultimate speed.

Spintec has been amongst the pioneers in MRAM development and is recognized worldwide as such. Consequently, we have / have had multiple partnerships with laboratories, research centers and companies, through joint R&D projects (ANR, EU), as well as bilateral industry partnerships. A preferred relation exists with Crocus, which led to the onset of a 5 years “joint laboratory” signed in 2013.

Based on patents filed between 2001 and 2005, a new technology of non-volatile magnetic memories, thermally assisted has been demonstrated by Spintec. The originality of this technology stems from the specific writing process that combines a short heating pulse sent through the memory cell (few nanoseconds) with a magnetic field pulse or a spin polarized current. **The very convincing results obtained by SPINTEC and LETI in the framework of the NEXT European project between 2001 and 2005 enabled the launch of a start-up Grenoble, Crocus-Technology, which has managed to raise 13.5 Million Euros from venture capitals in 2006. This transaction also received the grand prize of the ANVAR innovation in 2005 and was a finalist EU Descartes Prize in 2006.**

Since the first demonstration of the TAS-MRAM concept in 2004, several improvements / variations of this technology have been proposed:

1) By **introducing "thermal barriers"** based on conductive material of low thermal conductivity, of each side of the tunnel junction, it is possible to confine the heat generated at the insulating barrier in the layers of interest. Thermal barriers allowed dividing the heating current by 2, thus improving largely the consumption of TA-MRAM.

2) **Building double tunnel junctions**, it is possible to design a memory capable of storing more than two bits per cell, thus doubling the storage density of TAS-MRAM. Furthermore, double barrier systems provide another advantage in terms of reliability; they allow reducing the voltage drop across each barrier during write, which significantly reduces the risk of electrical breakdown.
3) **The concept of heat assistance can be advantageously coupled to writing by spin-polarized current to significantly improve the thermal stability in STT-based systems**. The use of spin transfer as writing means offers much better prospects for decreasing sizes than writing magnetic field. Indeed with the spin transfer, the write current decreases as the cell size while in the field writing, the write current rather tends to increase as the size decreases. However, the STT-RAM suffers from the same problem as the MRAM standards in terms of thermal stability for small sizes. TA-STT-RAM concept (Thermally Assisted Spin Transfer Torque RAM) allows to ensure higher MRAM densities while minimizing the write current. In this concept, the same current flowing through the tunnel junction makes heats by Joule effect and exerts magnetic torque by spin transfer torque phenomenon. The concept of TA-STT-RAM was developed within the framework of a bilateral agreement between CEA and Crocus and a ANR 2007 "RAMAC," (Technology Roadmap for Advanced MRAM).
4) Recently, **the joint R&D teams from Crocus in Spintec developed a self-referenced reading concept which now serves as building block for the company's products**. This new concept makes the memory much more tolerant to process variations and very promising for security applications (smart cards, routers, biometrics). Technological advances have enabled obtained Crocus growing dramatically, as evidenced by one of the latest fund-raising 300M€ in 2011 enabling him to go live with one of the first full magnetic back-end fab worldwide.
5) In addition, the research work carried out in close collaboration with SPINTEC allowed several advances at the highest international level of research on MRAM: the ultra-low power **memories combining writing to the local heating spin polarized current TAS-STT of systems with perpendicular anisotropy.**

Spintec laboratory and Crocus Technology represent in Grenoble an excellent example of the coexistence of fundamental study and technological application based on magnetic materials. The connection with the original laboratory is kept alive through a joint Research and Development program (now joint lab) which finances among other research activities the so-called “CIFRE thesis”, a PhD with an applicative approach, closely connected with a technological application. The different joint research activities were also financed through several ANR contracts (RAMAC 2007-2010, Pathos 2010-2013, Excalyb 2014-2018)

1.6 DESCRIPTION OF THE MANUSCRIPT

The manuscript is organized in three different parts:

In the first part of this manuscript (chapters 2-7), I will show how thermal assistance can be implemented in field induced switched MTJ to enhance the reliability and the scalability of MRAM. A new self-referenced reading scheme can be implemented in such MTJ in order to obtain a Magnetic Logic Unit that present new logic functionalities compared to standard MRAM. In a second time, I will present the implementation of thermal assistance in MTJ with current induced switching writing scheme. In that case, no field line is required, increasing thus the storage capacity of MRAM cell and decreasing the writing consumption while keeping a satisfying data retention capacity. Ultimately, thermal assistance can be implemented in MTJ with perpendicular magnetization. In that case, thermally induced anisotropy reorientation (TIAR) can be used to decrease the switching power consumption, increase the writing reliability and further improve the scalability of TAS-MRAM down to the 22nm technological node.

- **Chapter 2**

In this chapter I will describe key parameters of the functioning of MRAM memories, including the storage and the read functionalities, as well as a brief description of the first MRAM proposed architectures, based on the combination of orthogonal magnetic fields, either spatially (Stoner – Wohlfarth architecture) or in a time sequence (toggle architecture)

- **Chapter 3**

In order to improve the thermal stability, the write selectivity and the power consumption for MRAM applications, we proposed a new concept, of thermally assisted writing TAS-MRAM. The working principle, the details of the heating processes in a magnetic tunnel junction and the improvements achieved in order to reduce the heating power density, to maximize the retention of the memory will be described in this chapter. **These studies have been done during the PhD thesis of Marta Kerekes, Lucien Lombard, Erwan Gapihan and during the postdoc of Cristian Papusoi.**

- **Chapter 4**

This chapter will deal with the optimization of SR-MRAM for high density storage. Two routes for achieving this will be explored. In the first one we will focus on the reduction of the patterning dimensions of the MTJ, while maintaining manageable power-consumption and data retention properties, with the experimental demonstration of the feasibility of its functionalities. We will then investigate new data encoding methods for multibit operations, from the simulation of their performances to their experimental demonstration. **These studies have been done during the PhD thesis of Quentin Stainer**

- **Chapter 5**

The problem with the field driven writing of TAS-MRAM cells is still that the magnetic field needs to be generated by a current line with current pulses of a few milliamperes. TAS-MRAM requires a single magnetic field and lower field values compared to the toggle MRAM approach, thus lowering the total power consumption. However, the write field does not scale with cell size and can be at best kept constant, unlike STT-MRAM where the write current scales with cell size. In TAS-MRAM, the heating current is not the bottleneck, since the use of thermal barriers has already demonstrated a heating current density in the $1\text{-}2\times10^{6}$A/cm² range, similar to the lowest values of spin transfer torque MRAM cells (STT-MRAM). Alternatively, it is possible to get rid of the field line by still using the thermally assisted concept but combining it with spin transfer torque (STT) to switch an exchange biased storage layer. In this case, the same current flowing through the cell is used both to heat up the cell and switch the storage layer magnetization by STT. It is thus possible to combine the added stability obtained from the exchange biasing to retain the information with the reduction of the current through cell size scaling, since the cell switching occurs at a constant current density, typically in the 10^{6}A/cm² range. **These studies have been done during the PhD thesis of Jérémy Alvarez-Hérault and Antoine Chavent**

- **Chapter 6**

One significant realization towards high density memory cells has been to assist the spin transfer switching of the magnetization of the perpendicular cell. This was achieved by a thermally induced reorientation of the free layer magnetic anisotropy from out-of-plane to in-plane. The junction temperature increase is due to the Joule dissipation around the tunnel barrier produced by the same pulse of current which generates the spin transfer torque. It allows the spin transfer torque efficiency to be maximized during write, since the spin polarization of the current is perpendicular to the magnetization of the storage layer. This reduces the STT switching current and suppresses stochastic variations in switching time. This thermal assistance scheme was demonstrated in a MRAM cell designing a magnetic electrode coupled to a Co/Pd multilayer having a strong temperature dependence of the

perpendicular anisotropy. Leading to a temperature at which the magnetization re-orientation in-plane occurs can be adjusted between 90 and 250°C by varying the Co thickness in the 0.2- 0.4nm range. These cells showed thermal stability factors of $162k_BT$ for a critical current density of 4.6MA/cm², a record write efficiency at that time. **These studies have been done during the PhD thesis of Sebastien Bandiera.**

- **Chapter 7**

Will summarize the main conclusions of all these studies and will propose a MRAM roadmap for advanced technological nodes, below 20nm.

The second part of this manuscript will be dedicated to the description of my future research projects for the forthcoming years linked mainly to applied aspects of the magnetic tunnel junctions for: sub-20nm scalable MRAMs, hybrid logical circuits and innovative magnetic field sensors.

- **Chapter 8**

This chapter will detail the perspectives of this work as well as some of my future projects, dedicated to applied aspects of the magnetic tunnel junctions for: sub-20nm scalable MRAMs, hybrid logical circuits and innovative magnetic field sensors.

Finally I will give details about my scientific career after the PhD defended end of 2001, including:

- a Curriculum Vitae,
- my main research highlights,
- a detail of the 12 PhDs (co)supervised in this period as well as
- a list of publications including 45 Journal articles, 5 chapter books and 38 patents.

2. BASICS OF MRAMS

In this chapter I will describe key parameters of the functioning of MRAM memories, including the storage and the read functionalities, as well as a brief description of the first MRAM architectures, based on the combination of orthogonal magnetic fields, either spatially (Stoner – Wohlfarth architecture) or in a time sequence (toggle architecture)

2.1 STORAGE FUNCTION: MRAM RETENTION

2.1.1 Key role of the thermal stability factor

In memory applications, a key characteristic is the retention of the memory, i.e. how long the memory chip is capable of keeping the information which has been written in it. The specification depends on the application but is, for instance, on the order of 10 years for mass storage application such as in hard disk drives (HDD). In MRAM, the information may get corrupted by unintended switching of the magnetization of the storage layer due to thermal fluctuations. The failure rate in an MRAM chip of *N* bits in standby mode can be estimated as follows. The magnetization of the storage layer of the memory cell can be described as a bistable system, the two stable states being separated by an energy barrier ΔE. ΔE is determined by the magnetic material's properties and the shape and dimensions of the magnetic element, i.e. the MTJ storage layer, as explained below. At a temperature *T*, the characteristic thermally-activated switching time is given by an Arrhenius law,

$$\tau = \tau_0 \exp\left(\frac{\Delta E}{k_B T}\right), \tag{2.1}$$

where k_B is the Boltzmann constant and τ_0 is an attempt time of the order of 1 ns. For a given bit, the probability of not having accidentally switched after a time *t* is

$$P_{noswitch}(t) = \exp(-t/\tau). \tag{2.2}$$

For *N* bits, the probability for the set of *N* bits of not having experienced any switching event after a time *t* is:

$$P^N_{noswicth}(t) = \left[P_{noswitch}(t)\right]^N = \exp(-Nt/\tau). \tag{2.3}$$

Consequently, the probability of having experienced at least one switching event after a time *t*, i.e. the failure rate in standby mode is given by:

$$F(t) = 1 - \exp(-Nt/\tau) = 1 - \exp\left[\frac{-Nt}{\tau_0}\exp\left(-\frac{\Delta E}{k_B T}\right)\right]. \tag{2.4}$$

This expression clearly shows that the factor $\Delta = \frac{\Delta E}{k_B T}$, often called thermal stability factor, plays a key role in the failure rate of MRAM chips in standby mode, i.e., memory retention failure. *Figure 2.1* shows the variation of the failure rate during 10 years in standby mode (not during a write or read operation) as a function of the thermal stability factor (Δ) for a 32 Mbit and a 1 Gbit MRAM chip. In order for the probability of experiencing one failure in time (FIT) during 10 years in standby mode to be below an acceptable level of 10^{-4} (this number depends on the whether the application is memory or logic, and on the possible use of error correction codes), the thermal stability factor must be greater than *67* for the 32 Mbit chip and greater than *66* for the 1 Gbit chip. The higher the memory capacity, the larger the thermal stability factor has to be.

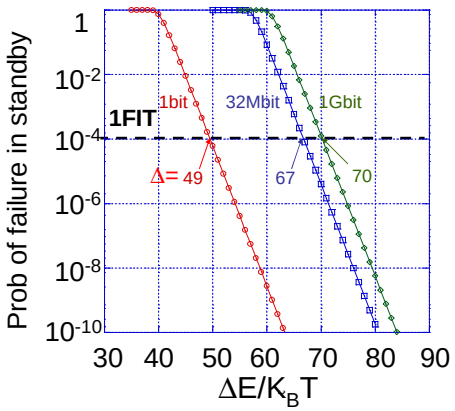


Figure 2.1: Failure rate during 10 years in standby mode for MRAM chips of 1 bit, 32 Mbit or 1 Gbit as a function of thermal stability factor.

2.1.2 Thermal stability factor for in-plane and

out-of-plane magnetized storage layer

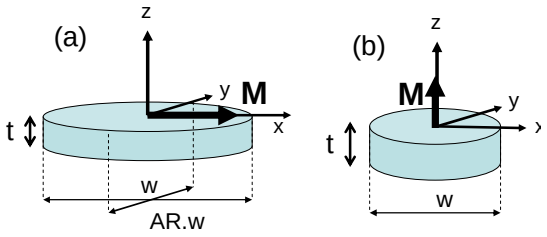


Figure 2.2: Schematic representation of a storage layer with its characteristic dimensions. (a) Case of an in-plane magnetized storage layer with an elliptical prism shape. (b) Case of an out-of-plane magnetized storage layer having the shape of a flat cylinder.

In magnetic materials, the barrier height Δ*E*, which determines the thermal stability factor, is most often created by a magnetic anisotropy which can have different origin. This anisotropy can be of magnetocrystalline origin or can be due to stress or to some electronic hybridization effects taking place at the interfaces in magnetic multilayers. It can be also due to the shape of the patterned magnetic element: a magnetic nanostructure having an elongated shape has an easy axis of magnetization along the long dimension of the structure. Whatever the origin of this anisotropy, it can generally be described by an energy per unit volume $\mathrm{E}_{anisotropy} = -K\left(\hat{n}\cdot\hat{M}\right)^2$ where $\hat{n}$ is a unit vector along the easy axis of magnetization and $\hat{M}$ is a unit vector parallel to the magnetization direction. The barrier height separating the two opposite stable states along the easy axis direction is then given by $\Delta E = KV$ where V is the volume of the magnetic nanostructure i.e. the volume of the storage layer in a considered memory cell.

Commonly used in-plane magnetized materials in MRAM have in general relatively weak magnetocrystalline anisotropy. Their magnetic anisotropy mostly originates from their shape. The MTJs, and in particular their storage layers, are patterned in the form of elliptical elements. The barrier height is then given by:

$$\Delta E = \frac{1}{2}\mu_0\left(N_y - N_x\right)M_s^2 V \qquad (2.5)$$

where N_x and N_y are the storage layer demagnetizing coefficients respectively along the short and long axis of the ellipse, M_s is the storage layer magnetization, and μ_0 is the vacuum permeability equal to $4\pi 10^{-7}$ *H/m* (SI).

There are no simple expressions for the demagnetizing coefficients N_x and N_y of an elliptical cylinder as a function of its characteristic dimensions (thickness *t*, width *w*, length $A_R w$ where A_R is the in-plane aspect ratio). These coefficients are functions of elliptic integrals and must be tabulated or numerically calculated[14][15]. Let's mention that for elliptical cylinders with small thickness *t*, the structure is often approximated as a uniformly magnetized ellipsoid, for which closed-form solutions exist. Qualitatively, for the purpose of understanding the general influence of the storage layer dimensions, the thermal stability factor Δ of in-plane magnetized storage layer can be approximated by:

$$\Delta = \frac{\Delta E}{k_B T} = \frac{\mu_0}{2}\frac{M_s^2 t^2 \left(A_R - 1\right) w}{k_B T}. \qquad (2.6)$$

The *equation (2.6)* shows that for in-plane magnetized system, Δ scales with the lateral dimension *w* (which is typically the technological node), the aspect ratio as (A_R-*1*), square of saturation magnetization M_s, and square of thickness *t*. Practically, aspect ratios between 1.5 and 2.5 are used. For larger aspect ratios, the magnetization switching no longer occurs via a coherent rotation of the

14 J.A. Osborn, *Demagnetizing factors of the general ellipsoid*, Phys.Rev.67, 351 (1945)

15 M. Beleggia, M. De Graef, Y.T. Millev, D.A. Goode and G. Rowlands, *Demagnetization factors for elliptic cylinders*, J. Phys. D: Appl.Phys. 38 (2005) 3333

magnetization (i.e., as a whole magnetic block) but proceeds via nucleation of a reversed domain and propagation of domain wall. Therefore, there is no benefit in terms of thermal stability of the magnetization in increasing the aspect ratio above ~2.5. From *equation (2.6)*, one can estimate that the smallest dimensions that an in-plane 2.5 nm thick CoFeB storage layer ($M_s \approx 10^6$A/m) can have whilst keeping a thermal stability factor above 70 is of the order of 60 nm× 150 nm.

Perpendicular-to-plane magnetized storage layer (*Figure 2.2*) can in general have better thermal stability than their in-plane counterparts at smaller dimensions because of their much larger intrinsic anisotropy. This is actually one of the reasons why the hard disk drive industry switched from in-plane magnetized magnetic media to perpendicular media in 2004. The perpendicular magnetic anisotropy (PMA) in thin film magnetic materials can have different origins. It can originate from the bulk of the material as in FePt or FePd $L1_0$ ordered alloys due to a tetragonal distortion of the lattice cell along the growth direction. This bulk anisotropy is usually described by a characteristic energy per unit volume (in J/m^3)

$$\mathrm{E}_{anisotropy}^{Bulk} = -K_V \left(\hat{n} \cdot M\right)^2 \qquad (2.7)$$

where $\hat{n}$ is a unit vector normal to the plane of the layer. The PMA may also be of interfacial origin due to interfacial electron hybridization or interfacial stress (for instance at Co/Pd, Co/Pt or CoFe/MgO interfaces). This interfacial PMA is usually expressed in terms of a volume energy (in J/m^3) as

$$\mathrm{E}_{anisotropy}^{Interface} = -\frac{K_S}{t}\left(\hat{n} \cdot \hat{M}\right)^2 \qquad (2.8)$$

where K_S is the surface energy (J/m²) and t the thickness of the storage layer. However, this PMA is partially counterbalanced by the demagnetizing energy, i.e., the cost of magnetostatic energy required to pull the magnetization of a thin film out of the plane. Indeed, from a pure magnetostatic viewpoint, the thickness of a magnetic thin film is most often its smallest dimension. The direction along the thickness is therefore usually the hard axis of magnetization (in terms of magnetostatics). If the magnetization is nevertheless pulled out of plane by other sources of anisotropy, these other sources must overcome the demagnetizing energy. For an extended thin film, the demagnetizing energy per unit volume is written:

$$\mathrm{E}_{demagnetizing} = +\frac{1}{2}\mu_0 M_s^2 \left(\hat{n} \cdot \hat{M}\right)^2 \qquad (2.9)$$

In perpendicular STT-MRAM, the MTJ and therefore its storage layer is usually patterned in the form of a flat cylinder, since there is no longer a need for in-plane shape anisotropy to insure thermal stability of the magnetization. A cylindrical shape allows an increase in areal density. If the width of the cell is larger than 50 nm, the demagnetizing energy expression in *equation (2.9)* is a sufficiently good approximation. However, for smaller dimensions, it is necessary to take into account the exact values of N_x , N_y , N_z demagnetizing coefficients. Since $N_x + N_y + N_z \approx 1$ and $N_x = N_y$ due to the cylindrical shape, the demagnetizing energy can be written as:

$$\mathrm{E}_{demagnetizing} = +\frac{1}{4}\mu_0 \left(3N_z - 1\right) M_s^2 \left(\hat{n} \cdot \hat{M}\right)^2 \qquad (2.10)$$

The total magnetic anisotropy energy per unit volume of the patterned storage layer is then the sum of these various anisotropy contributions:

$$\mathrm{E}_{anisotropy} = \mathrm{E}_{anisotropy}^{Bulk} + \mathrm{E}_{anisotropy}^{Interface} + \mathrm{E}_{demagnetizing} = -\left[K_V - \frac{1}{4}\mu_0 \left(3N_z - 1\right) M_s^2 + \frac{K_s}{t}\right]\left(\hat{n} \cdot \hat{M}\right)^2 \qquad (2.11)$$

For the storage layer magnetization to remain stable in the out-of-plane direction, the term called the effective anisotropy

$$K_{eff} = K_V - \frac{1}{4}\mu_0(3N_z - 1)M_s^2 + \frac{K_s}{t} \qquad (2.12)$$

must be positive, meaning that the bulk and interfacial perpendicular anisotropy must exceed the demagnetizing energy. To estimate the thermal stability factor of the storage layer, a cylindrical storage layer of diameter *w* in a perpendicular MTJ, one must consider which magnetization switching process prevails. In out-of-plane magnetized nanostructures of dimensions typically above 40 nm, magnetization reversal tends to proceed by nucleation of a reversed domain, most often at the edge of the nanostructures and propagation of the domain wall throughout the nanostructure. In this case, the barrier height for reversal is determined by the energy required for the nucleation of the reversed domain. In contrast, for smaller structures (typically below 30 nm in diameter), the magnetization does not have enough space to nucleate a reversed domain and consequently switches as a rigid magnetic block (often called a "macrospin"). In this macrospin approximation, which is valid for technological node below ~30 nm, the thermal stability factor of a cylindrical storage layer of diameter *w* in a perpendicular MTJ is written:

$$\Delta = \frac{\Delta E}{k_B T} = \frac{\left[\left(K_V - \frac{1}{4}\mu_0(3N_z - 1)M_s^2\right)t + K_s\right]\frac{\pi}{4}w^2}{k_B T} \qquad (2.13)$$

As an example, for a 1.2 nm thick CoFeB storage layer, with typical value of the interfacial anisotropy, a MgO barrier of $1.2.10^{-3}$ J/m², and a magnetization on the order of 1000 kA/m:

- Δ= 107 for *w* =30 nm,
- Δ= 77 for *w* = 25 nm,
- Δ= 52 for *w* = 20 nm, and
- Δ= 32 for *w* = 15 nm.

A 10 year retention for a MTJ with *w* ≤ 20 nm therefore requires an increase the interfacial anisotropy, a decrease the storage layer thickness while maintaining its TMR amplitude, or a decrease its saturation magnetization.

2.2 READ FUNCTION

2.2.1 Principle of read operation

The general principle of the read operation in MTJ-based MRAM consists in exploiting the change of resistance between P and AP magnetic configurations to determine the magnetic state of the junction and therefore the written information. This principle is illustrated in *Figure 2.3*. During read, a small reading current flows through the MTJ to sense its magnetic state from the value of the cell resistance. Usually, the output resistance value is compared to a reference cell whose resistance is the average value of the low and high resistance state (*Figure 2.3c*). To discriminate between the two possible MTJ states in a fast and reliable way, the cell-to-cell distribution of low resistance and high resistance states must be separated by at least $6(\sigma_{low} + \sigma_{high})$, where σ_{low} and σ_{high} are respectively the half-width of the distributions of low and high resistance states over an MRAM chip (*Figure 2.3b*).

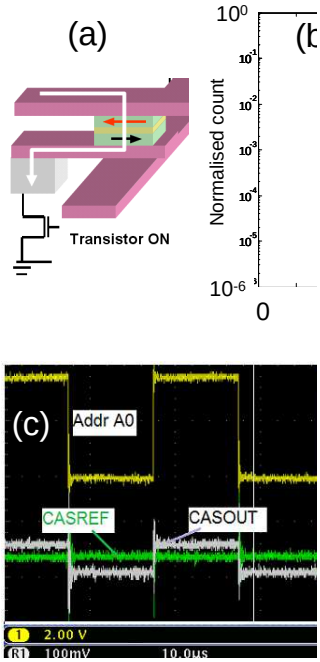


Figure 2.3: Principle of read operation: (a) During re The distributions of R_{low} corresponding to P state a fast and reliable discrimination between the two me chip in 130 nm technology. (c) Example of readou switching between two cells in opposite magnetic with a reference cell having an intermediate resistance $(R_{low}+R_{high})/2$.

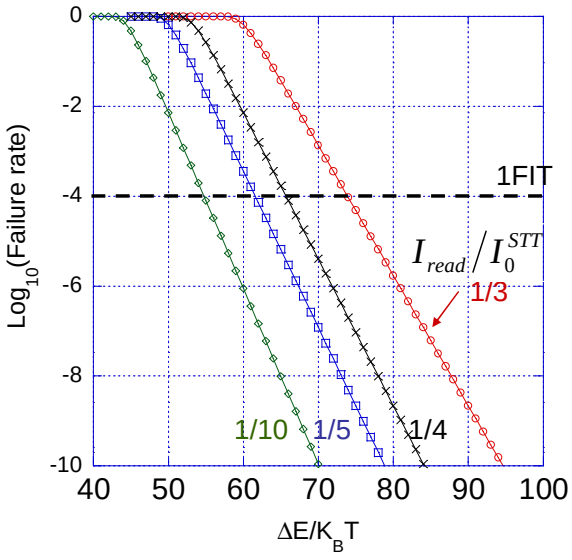


Figure 2.4: Calculated failure rate during read as a function of the thermal stability factor in standby for several values of the I_{read}/I_0^{STT} ratio. The plot assumes that 8 bits are read simultaneously during 10 % of the time for 10 years. The dashed line corresponds to an example situation where one failure in time (FIT) would happen in 10 years with a probability of 10^{-4}.

The read current is chosen so that the voltage across the MTJ during read is in the range 0.1 V to 0.2 V. This choice is motivated by two reasons:

(a) **In MTJs in general and in MgO based MTJ in particular, the TMR amplitude decreases with bias voltage.** This TMR decrease versus V is explained by a reduction of the spin polarization as the bias voltage increases due to the fact that the spin filtering mechanism associated with the symmetry of the wave becomes less effective at higher voltage. Also, hot tunneling electrons injected in the receiving electrode after tunneling generate magnetic excitations in the ferromagnetic electrodes which can contribute to depolarize the tunneling current. With read voltage in the range of 0.1 V to 0.2 V, the decrease of TMR compared to the maximum amplitude at very low voltage is no more than 10 % in relative value.

(b) **To avoid spin transfer torque disturbance of the storage layer magnetic state by the read current** as explained in the following section (2.2.2).

2.2.2 STT induced disturbance of the storage layer magnetic state during read

Very similarly to the write current in STT-MRAM, the current flowing throughout the MTJ during read, exerts a spin transfer torque effect on the storage layer magnetization. In order to avoid an unwanted writing (or disturbance) during read, the read current must be low enough compared to the STT critical current for switching. The failure rate associated with accidental STT switching of the storage layer magnetization during read can be estimated as follows. Let's consider I_0^{STT} the STT critical current. The barrier height for magnetization switching under a read current $I_{read} < I_0^{STT}$ is decreased due to the STT influence according to the following formula:

$$\Delta E = \Delta E_0 \left(1 - \frac{I_{read}}{I_0^{STT}}\right)^{\delta} \qquad (2.14)$$

where ΔE_0 is the barrier height at zero current, as given by the *equations (2.5) and (2.12)*.

This yields the following failure rate during read:

$$F(t) = 1 - \exp(-Nt/\tau) = 1 - \exp\left[\frac{-Nt}{\tau_0}\exp\left(-\frac{\Delta E}{k_B T}\left(1-\frac{I_{read}}{I_0^{STT}}\right)^{\delta}\right)\right] \qquad (2.15)$$

Figure 2.4 shows how the read current has to be adjusted with respect to the STT critical current for switching depending on the storage layer thermal stability factor and on the required failure rate. In STT-MRAM, the write voltage on the order of 0.5 V and the read voltage on the order of 0.15 V are typically used, corresponding to a ratio I_{read}/I_0^{STT} ratio between 1/3 and 1/4.

2.3 First MRAM Generations

Several large IC manufacturers (Motorola, IBM, NEC, Toshiba, Samsung, …), attracted by the potential of MRAM as a universal memory, rapidly entered the MRAM arena and started their initial developments with the same write scheme, known as "*Stoner-Wohlfarth (SW) approach*" or "*Field Induced Magnetic Switching approach*" (FIMS). Motorola[16] and IBM[17] were the two main industrial players developing in the early 2000s a MRAM architecture based on 1MTJ-1FET per cell and were exploiting this write scheme for the memory encoding.

Two categories of field-induced magnetic switching MRAM (FIMS-MRAM) are described in the following sections:

1. **MRAM based on the Stoner Wohlfarth model**
2. **The "toggle" MRAM**, an improved version, which succeeded to reach the market in 2006.

2.3.1 Stoner-Wohlfarth MRAM

The Stoner-Wohlfarth MRAM (SW-MRAM) was the first developed architecture of MTJ-based MRAM. SW-MRAM consists of an array of MTJs in which each MTJ is connected in series with a selection transistor (*Figure 2.5*). The MTJs are sandwiched between two sets of orthogonal conducting lines (called bit lines and word lines) aimed at creating local magnetic fields on the MTJs storage layer when current flows are sent through them:

- **during reading**, the selection transistor of the addressed cell is closed, a current flows through the MTJ and the magnetic state of the memory point is derived from the measured resistance of the stack.
- **during writing**, the selection transistor is open: no current flows through the MTJ.

The read operation of the MTJ based class of MRAM was greatly improved compared with all metal technologies (AMR or GMR based). However large capacity chips required both large TMR and narrow distributions of the resistance in the two states (Parallel and Antiparallel configurations). In architectures using mid-point reference cells for the detection of the information stored in the magnetic bits a minimum of 12-sigma is required for multi-megabits arrays between the centers of the distribution of the resistance of high and low resistance states. In the 4Mb demonstrator chip of Motorola published in 2005, over 20-sigma separation was demonstrated thanks to an improved process control of the bit patterning, giving ample read margin. The largest SW-MRAM chips that has

16 Tehrani S, Engel B, Slaughter JM, Chen E, De Herrera M, Durlam M, Naji P, Whig R, Janesky J, Calder J, *Recent developments in Magnetic Tunnel Junction MRAM*, IEEE trans. on Mag., 36, N°5, 2752 (2000)

17 Scheuerlein, R., Gallagher, W., Parkin, S., Lee, A., Ray, S., Robertazzi, R., Reohr, W., *A 10ns Read and Write non-volatile Mmeory Array Using a Magnetic Tunnel Junction and FET Switch in each Cell*, Digest of technical papers, IEEE International Solid State Circuits Conference, 128 (2000)

been produced was the 16Mb chip from the alliance IBM-Infineon[18], which is also the largest MRAM chip ever fabricated so far. It was built from a 0.18µm CMOS technology with three additional mask levels for the realization of the MRAM elements.

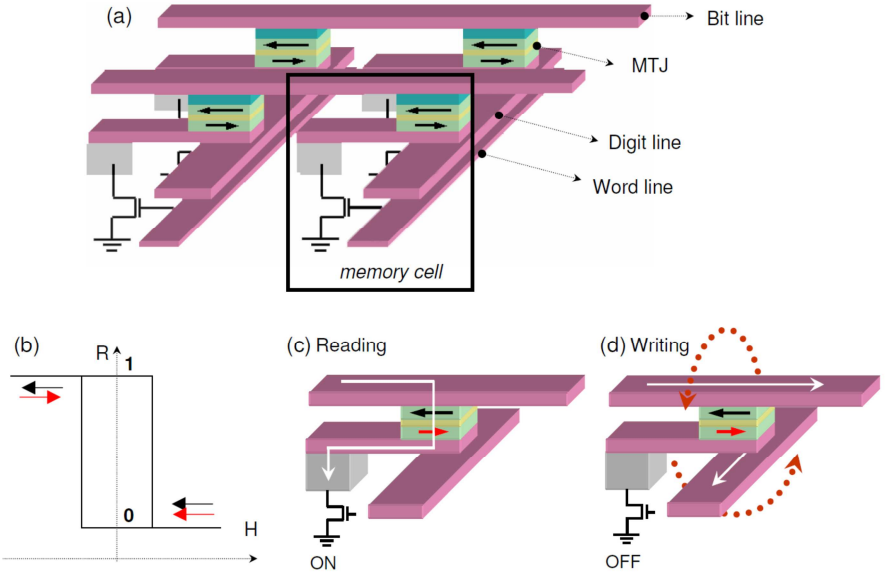


Figure 2.5: (a) Schematic representation of a conventional SW-MRAM architecture containing MTJ cells at the intersection of orthogonal lines and on top of a selection transistor The MTJ are n-plane magnetized with one layer of fixed magnetization pinned along the ellipse long axis ("reference layer," black arrow) and one layer of switchable magnetization having two stable states along the ellipse long axis ("storage layer," red arrow). (b) Typical minor hysteresis loop showing the reversal of the storage layer and two corresponding resistance levels. (c) Reading scheme: transistor is ON and a small electrical current is sent through the junction to measure its resistance (d) Writing scheme: to address the memory element located at the front left of the array, two pulses of current (represented by white arrows) are simultaneously sent in the bit line and word line which cross each other at the addressed memory point. These pulses generate two perpendicular magnetic fields (represented by orange arrows) which add as two vectors at the addressed memory point.

To write at a particular addressed cell, two simultaneous pulses of current are sent in the bit line and world line which cross each other at the addressed MTJ cell. These currents must be adjusted so that the resulting field at the addressed cell is locally large enough to switch its storage layer magnetization in the desired direction while not switching the storage layer magnetization in the other memory points located further along the same bit line or the same world line. In these SW-MRAMs, the write selectivity is thus based on the combination of two orthogonal magnetic fields, one along the easy axis of magnetization, the other along the hard axis. This write principle is based on the so-called Stoner-Wohlfarth switching astroid (*Figure 2.6* which provides a quantitative criterion for magnetization switching in a magnetic nanostructure with uniaxial anisotropy).

To review the principle, a magnetic nanostructure of magnetization M_s has a uniaxial anisotropy described by an anisotropy energy per unit volume K_u. This nanostructure is assumed to be sufficiently small so that its magnetization remains homogeneous and therefore can be described in the macrospin approximation. We now assume that the magnetization is initially oriented in one direction along the easy axis of magnetization and that we want to switch it in the opposite direction. This is achieved by applying simultaneously a field along the easy axis of magnetization (H_x) and another one in the orthogonal direction, i.e., along the hard axis of magnetization (H_y). It was demonstrated that in this situation, the condition for switching is that the total field vector of components (H_x, H_y) must fall out-of the Stoner-Wohlfarth astroid, which is defined by the relationship:

18 Gallagher, W.J. Abraham, D. Assefa, S. Brown, S.L. De Brosse, J. Gaidis, M. Galligan, E. Gow, E. Hughes, B. Hummel, J. Kanakasabapathy, S. Kaiser, C. Lamorey, M. Maffit, T. Milkove, K. Yu Lu Nowak, J. Rice, P. Samant, M. O'Sullivan, E. Parkin, S.S.P. Robertazzi, R. Trouilloud, P. Worledge, D. Wright, G. See-Hun Yang, *Recent advances in MRAM technology*, Proceedings of the IEEE International Symposium on VLSI Technology, 72 (2005)

$$H_x^{2/3} + H_Y^{2/3} = \left(\frac{2K_u}{M_s}\right)^{2/3} \quad (2.16)$$

This sets a lower limit to the amplitude of the write field in a SW-MRAM chip. Other memory cells called half-selected bits and located on the active field lines also feel the field created by the current pulse but not the two perpendicular fields simultaneously. They are. In order to avoid half-selected bits to switch, the easy axis field must be lower than the anisotropy field H_k given by $H_K = \left(\frac{2K_u}{M_s}\right)$ otherwise this field alone would switch all bits located along the corresponding word line. Thus, taking into account the lower limit set by the SW astroid and upper limit set by the anisotropy field, this defines the ideal operating window for SW-MRAM. However, in practical devices, several factors actually restrain the size of this operating window:

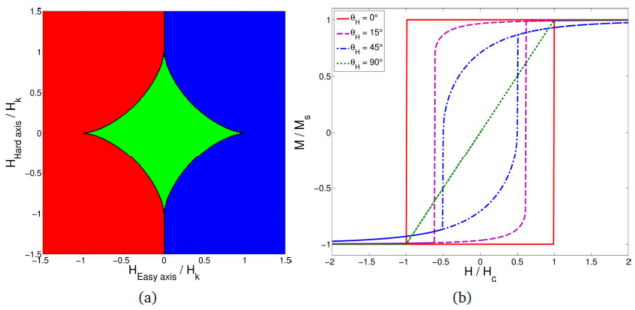


Figure 2.6: (a) Stability regions for the magnetization of a ferromagnet with an easy anisotropy axis at 0 ◦. The red and blue regions correspond to unique possible alignment directions of the magnetization along its easy axis, indicated by the white arrows, while in the green region both directions are concurrently stable. The boundaries of the bistable region constitute the Stoner-Wohlfarth astroid. (b) Normalized magnetization of a macrospin ferromagnet as a function of the external field amplitude and directions, projected on the field application axis directions of the magnetization along its easy axis, indicated by the white arrows, while in the green region both directions are concurrently stable. The boundaries of the bistable

- **The SW astroid** in elliptic MTJ of typical dimensions 100 nm × 200 nm **is often distorted due to micromagnetic distortions of the magnetization**.
- **The switching criterion given by the SW astroid is actually valid only at 0 K.** For devices operating at ambient temperature, thermal activation can significantly assist the magnetic switching so that the operating window must be pushed further away from the theoretical astroid.
- **Due to variability in the patterning process, cell-to-cell distributions in effective anisotropy field lead to cell-to-cell distribution in the shape and size of the SW astroid.** This imposes stringent conditions on the process of fabrication of the memory elements, preventing the realization of large memory arrays. This SW write scheme is efficient as long as all the bits constituting the array have identical or very similar magnetic properties.

No write conditions exist in which all bits could be properly written without writing any half-selected bits. The main parameters ruling the distribution widths are the uniformity of the chemical composition of the MTJ and the accuracy of the patterning process. Any defect or dispersion in the shape of the MTJ immediately results in a broadening of the switching field distribution. Similarly, the correct control of the shape upon scaling is very critical to tightly control the switching distribution. If the switching field of some bits gets too close to the astroid curve, its magnetic stability is reduced and it might be accidentally written due to thermal fluctuations even in the sole presence of the magnetic field along the hard axis. This problem may also occur due to some irreproducibility in the switching process in the magnetic elements. Indeed, it has been observed that upon cycling, the switching field of a single element could vary over a relatively wide range depending on the magnetization reversal mechanism that occurred. These jumps between competing mechanisms are mainly due to the thermal fluctuations that cannot be neglected at room temperature. To prevent this detrimental effect of the thermal fluctuations, specific shapes were designed that proved to yield more repeatable switching process. Element shapes with flat ends have more unpredictable switching mechanisms as either C-state, S-states or even vortex could develop due to large magnetic charges at their ends. Tapered ends are preferable to minimize magneto-static fields although too sharp ends are difficult to technologically control.

The research and development in this area has been very useful in starting the development of hybrid CMOS/MTJ technology but it did not yield a product because of write selectivity problems and poor down-size scalability. **Taking into account all these problems of switching field distributions and thermal fluctuations, the operating region of the SW-MRAM was quite reduced and often bits became inoperable.** Industrials had thus to create redundancy bits to replace the defective ones. Due to the technological difficulties to produce a reliable product based on the SW write scheme, several industrials even stepped out the MRAM arena, as Cypress or the IBM/Infineon alliance.

2.3.2 Toggle MRAM

Fortunately, a solution to this "*half select instability*" **problem was found by Savtchenko *et al.* from Freescale Technologies, architecture called "toggle writing"[19]. Similarly to SW-MRAMs,** Toggle MRAMs are also written with magnetic fields but the structure of the MTJ storage layer and the synchronization of the two orthogonal pulses of magnetic field differ from SW-MRAM. The magnetization in the MTJ ferromagnetic layers is still in-plane and the cells are patterned in elliptical shape, providing uniaxial shape anisotropy with easy axis along the long axis of the ellipse. In toggle MRAM, the ellipses are oriented at 45°[20] with respect to the bit lines and word lines to optimize the write process – *see Figure 2.7*. The storage layer consists of a compensated SAF (synthetic anti ferromagnet), i.e. two ferromagnetic layers of identical magnetic moment, antiferromagnetically coupled through a thin Ru spacer layer. For a proper choice of the Ru thickness (between 0.5 to 1nm), the RKKY coupling between the two magnetic layers is antiparallel and its strength can be adjusted by finely tuning the Ru thickness. When a moderate field is applied to such a structure, a magnetic transition takes place at a field called "*spin-flop field*" between a configuration at low fields, wherein the magnetic moments of the two layers lie antiparallel along their common anisotropy axis, and a configuration above the spin-flop field, where they lie symmetrically with respect to the field direction in a scissor configuration (*see Figure 2.8*). As a result, at low fields, the system has no net magnetic moment whereas above the spin-flop field, it acquires a net magnetic moment.

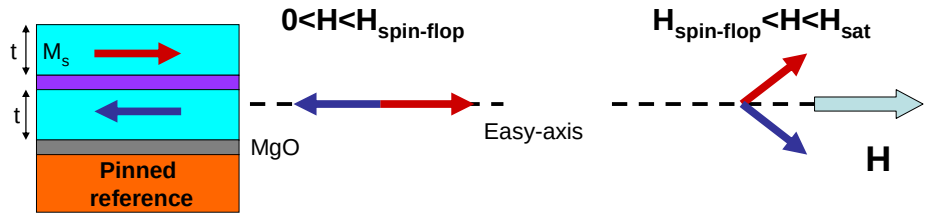


Figure 2.8: Schematic explanation of the spin-flop transition which takes place in the synthetic antiferromagnetic storage layer of a toggle MRAM cell.

The spin-flop field $H_{spin-flop}$ is given by the following expression[21]:

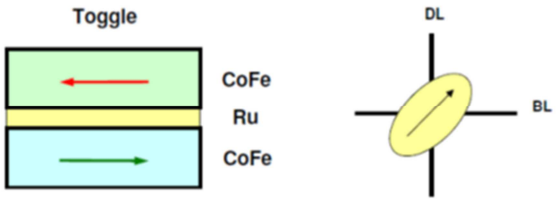


Figure 2.7: Schematic orientation of the bit with respect to the programming lines. H2 refers to the field generated by the bit line and H1 to the field generated by the digit line

19 L. Savtchenko, B. Engels, N. Rizzo, M. DeHerrera, J.A. Janesky, US6545906 (2001).

20 Engel BN, Akerman J, Butcher B, Dave RW, DeHerrera M, Durlam M, Grynkewich G, Janesky J, Pietambaram SV, Rizzo ND, Slaughter JM, Smith K, Sun JJ, Tehrani S, *A 4-Mb toggle MRAM based on a novel bit and switching method*, IEEE Trans. On Mag., 41, N°1, 132 (2005)

21 B. Dieny, J.P. Cavigan, J.P. Rebouillat, J.Phys.Condens.Matter.2, 159 (1990).

$$\mu_0 M_s H_{spin-flop} = 2\sqrt{K_{eff}\left(\frac{A}{t} + K_{eff}\right)} \qquad (2.17)$$

where M_s is the saturation magnetization of the two ferromagnetic layers (assumed here to be identical), t is their thickness, K_{eff} is their effective anisotropy per unit volume mainly of shape origin, and A is the amplitude of the interfacial antiferromagnetic coupling through the Ru spacer. Therefore, the spin-flop field can be adjusted by varying either the cell aspect ratio which determines K_{eff}, the ferromagnetic layers thickness or the Ru thickness which determines the amplitude of the antiferromagnetic coupling. Typical values of this spin-flop field in toggle MRAM are of the order of 5mT. The write toggle operation then proceeds as schematically represented in *Figure 2.9*. In the initial state, the two ferromagnetic layers are in antiparallel magnetic configuration along the long axis of the elliptical cell. At t_1, a current is sent in the x-line generating a magnetic field on the storage layer in the y-direction. This field is typically of the order of 7 to 10mT, above the spin-flop transition. The two magnetizations then scissor in the direction of this field and get in spin-flop configuration. The applied field is then gradually rotated by two steps of 45°. This is achieved by applying simultaneously a current along the x-line and y-line between t_2 and t_3 then only along the y-line between t_3 and t_4. During these steps, the spin-flop magnetic configuration rotates with the field. The y-current is then stopped. Since no more magnetic field is applied, the magnetization of the ferromagnetic magnetic layers then relax back to the antiparallel configuration along their easy axis of magnetization. In the final state, both layers have rotated by 180°. This writing process takes between 10 and 20 ns.

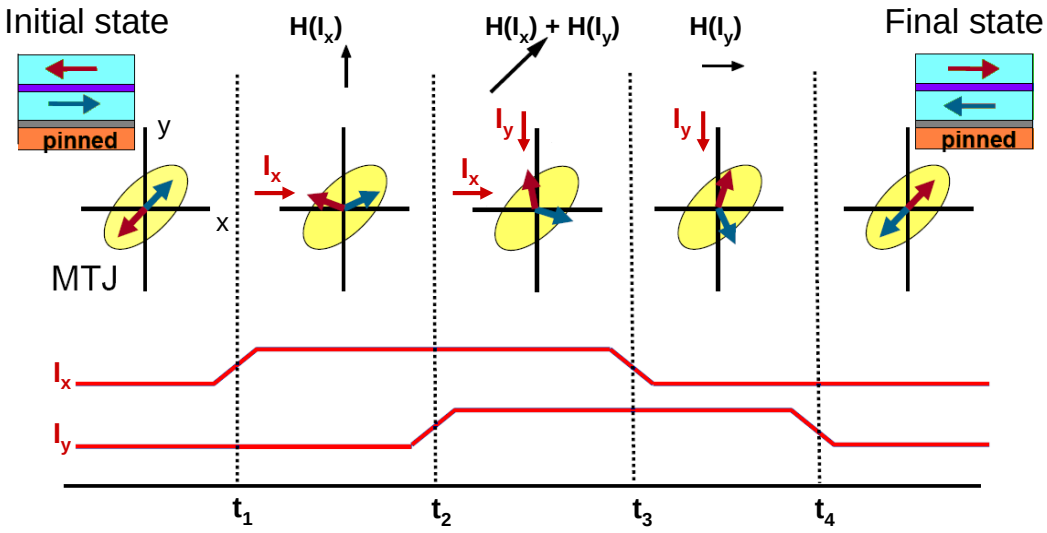


Fig. 2.9: Toggle write operation sequence

The application of this sequence of current pulses systematically rotates the storage layer magnetization by 180° whatever the initial state of the system (i.e., independently whether a “0” or a “1” is written in the memory element). **Therefore it is necessary to read before write to determine whether the magnetic state has to be changed or not.**

In order to maximize the field produced by a given current in the word and bit lines and better confine the field at the memory element, these lines are coated on their faces opposite to the memory element with a soft magnetic material (configuration called cladding)[22]. This soft magnetic material gets polarized by the magnetic field created by the current flowing in the line and helps focus the field onto the storage layer. Typically a factor 2 gain in field amplitude is obtained thanks to this cladding.

22 N.D. Rizzo, US6340085 (2001).

Toggle writing provides a much wider operation window than SW writing as illustrated in *Figure 2.10* on a 4Mbit toggle chip from Everspin Technologies. In toggle writing, the energy barrier to switch half-selected bits is many times larger than for switching fully selected bits[23].

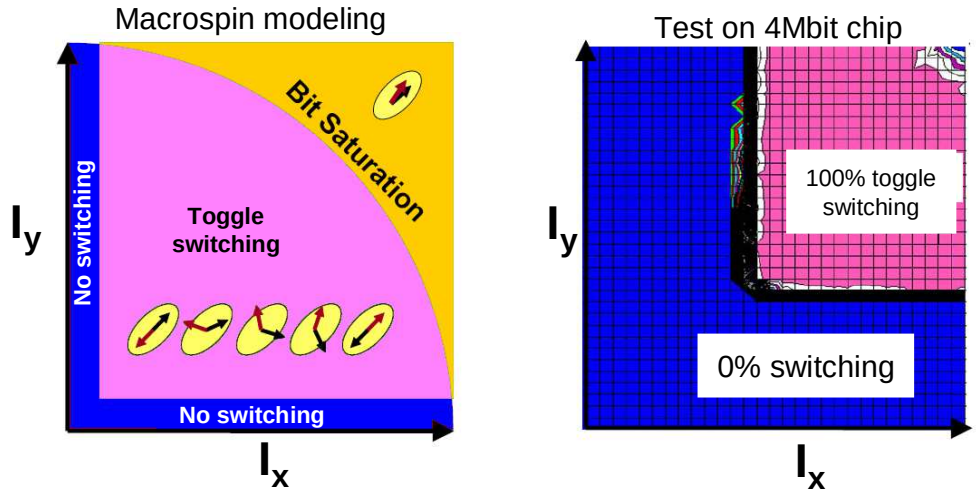


Figure 2.10: Toggle operation windows determined from macrospin modeling (left) and from testing a 4 Mbit chip from Everspin[13].

Toggle-MRAM have been extensively developed by Motorola, Freescale and then Everspin (the Spin-off of Freescale that industrialized the MRAM) and they are manufacturing actually a full family of MRAM product ranging from 256Kb to 16Mb for a large panel of applications. Toggle-MRAM has taken market shares to the conventional Flash memory in the data storage industry where its speed and unlimited endurance was appreciated for data logging or file allocation tables. It is also advantageously replacing battery backed SRAM in all systems where critical data should be rapidly stored upon power failure. Finally its historical advantage of radiation immunity makes it a natural choice for spatial and aeronautics applications[24]. **The commercialization of a 4Mbit MRAM by Everspin in 2008 was regarded as an outstanding achievement because it demonstrated that the integration of a front-end CMOS process together with a back-end magnetic process in a commercial product was possible.**

However, despite the success of the Toggle-MRAM, all MRAM technologies based on field induced switching write schemes are inherently poorly scalable. Indeed, In order to insure sufficient memory retention and to guarantee 10 years data retention, the energy barrier between the two written states has to be larger than $70k_BT$. This implies either maintaining the magnetic volume (V) of the storage layer or increasing the effective magnetic anisotropy (K^{eff}). In both cases, the switching fields for SW write or the spin flop field for the toggle write increases. Moreover, as the cross-section of the bit lines and word lines decreases, the current density then drastically increases up to the electromigration limit of the order of $10^7 A/cm^2$. Besides, the write power continuously increases which makes these concepts not viable at small technological nodes. As the feature size (F) decreases, the volume of the storage layer decreases as F^2 so that the effective anisotropy must be increased as F^{-2}. In toggle writing, the spin-flop field given by *Equation (2.17)* roughly scales as $(K_{eff})^{1/2}$, i.e., as F^{-1}. This spin-flop field is the lower limit of the write field in toggle MRAM. Because the distance between the center of the field-generating line and the storage layer does not vary significantly as the technology shrinks, the current required to generate the write field is proportional to the write field amplitude and therefore roughly scales as F^{-1}. In terms of current density, if only the width of the field generating lines decreases while their height is approximately constant, the current density in these lines increases as

23 D.C. Worledge, Appl. Phys. Lett. 84, 4559 (2004).

24 http://www.everspin.com/PDF/press/2009_sept_8_airbus.pdf

F^{-2} when F itself decreases. Since the electromigration threshold in Cu is~10^7 A/cm², this limits the MTJ width to dimensions above 100 nm. Therefore the down-size scalability of toggle MRAM and of other types of field-written MRAM is limited by this consideration. **The Toggle-MRAM is not predicted to operate at nodes smaller than 90nm**.

Different (and improved) MRAM concepts are thus needed for smaller technological nodes.

3. THERMALLY ASSISTED MRAMs

THERMALLY ASSISTED MRAM concept

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PhD THESIS

1. Yann Conraux (co-supervising 75%) – R&D engineer Crocus Technology

Préparation et caractérisation d'un alliage amorphe ferrimagnétique de GdCo entrant dans la conception de jonctions tunnel magnétiques. Résistance des jonctions tunnel magnétiques aux rayonnements ionisants
Université Joseph-Fourier, Grenoble, Oct. 10 2005 Directeur de thèse : Jean-Pierre Nozières

2. Marta Kerekes (co-supervising 25%) – passed away

Développement de nouvelles méthodes d'étude du comportement dynamique des systèmes de type vanne de spin à très hautes fréquences
Université Joseph-Fourier, Grenoble, 2006 – not defended, student died before defense Directrice de thèse : Ursula Ebels

3. Lucien Lombard (co-supervising 33%) - R&D engineer Crocus Technology

Etude et extension de la gamme de température de fonctionnement des Mémoires Magnétiques à Accès Aléatoire Assistées Thermiquement
Université Joseph-Fourier, Grenoble, Dec. 1 2010 Directeur de thèse : Alain Schuhl

4. Erwan Gapihan (co-supervising 25%) - R&D engineer Crocus Technology

Mémoire magnétique à écriture assistée thermiquement à base de FeMn
Université Joseph-Fourier, Grenoble, Jan. 11 2011 Directeur de thèse : Bernard Dieny

5. Jérémy Herault (co-supervising 33%) - R&D engineer Crocus Technology

Mémoire magnétique à écriture par courant polarisé en spin assistée thermiquement
Université Joseph-Fourier, Grenoble, Oct. 4 2010, Directeur de thèse : Alain Schuhl

6. Giovanni Vinai (co-supervising 75%) – postdoc Trieste

Scalabilité et amélioration des propriétés d'échange des TA-MRAM
Université Joseph-Fourier, Grenoble, Dec. 16 2013, Directeur de thèse : Jean-Pierre Nozières

7. Kamil Akmaldinov (co-supervising 25%) – unemployed

Ferromagnetic/antiferromagnetic exchange bias nanostructures for ultimate spintronic devices
Université Joseph-Fourier, Grenoble, February, 06, 2015, Directeur de these: Bernard Dieny

In order to improve the thermal stability, the write selectivity and the power consumption for MRAM applications, SPINTEC pioneered proposed a new concept, fundamentally different with respect to the field written MRAMs: the thermally assisted writing, called *TAS-MRAM*[25]. A current flow through the junction is used to heat the cell above a threshold temperature enabling the storage of information. The advantages are an error free selection process, simplified memory cell and lower power consumption with better thermal stability.

3.1 THERMALLY ASSISTED SWITCHING WORKING PRINCIPLE

In magnetism, it is well known that the switching of the magnetization of ferromagnetic materials can be more easily done at elevated temperature than at low temperature. Indeed, the anisotropy energy barrier height preventing spontaneous switching ($K^{eff}V$, K^{eff} effective magnetic anisotropy, V volume of magnetic element) is reduced when the temperature is increased and this increase of the thermal activation (k_BT) helps to overcome the energy barrier. The switching is thus possible the magnetization of ferromagnetic materials can be more easily switched at elevated temperature. Indeed, the anisotropy energy barrier height preventing spontaneous switching is reduced when the temperature is increased and this increase of the thermal activation helps to overcome the energy barrier.

The thermally assisted writing is actually implemented in hard disk drives (*HDD*) technology because *TAS* can help circumventing the thermal stability problem of present *HDD* technology and thereby further extend the areal storage density and the cell size reduction. In *HDD* technology, the local heating is provided by a plasmonic antenna in the immediate vicinity of the write head magnetic pole.

The thermally assisted writing scheme consists in combining a temporary heating of a memory cell (Joule heating produced by a pulse of current through the *MTJ*) with the application of a magnetic field or of a spin-transfer torque to select and write the magnetic bit. In thermally assisted writing, the data is stored at a standby temperature where the barrier height for switching is high. During the write process, the magnetic cell is temporarily heated up to a temperature close to its magnetic ordering temperature at which its magnetization can be easily switched. A magnetic field is then applied for magnetic switching. Then, the element is rapidly cooled down to the standby temperature and the magnetization subsequently remains frozen in the new direction. In thermally assisted writing, the data is stored at a standby temperature where the barrier height for switching is high providing improved retention of the information (thermal stability factor $\Delta=K^{eff}V/k_BT$ larger than 70). The heating is naturally produced by the Joule dissipation produced by the current flowing through the tunnel barrier of the magnetic tunnel junction.

An improved way to achieve this high temperature dependence - proposed by Spintec and developed at Crocus Technology[26] and represented schematically in *Figure 3.1* – is:

- **to heat directly with a current flow through the MRAM cell** and
- **to use an exchange biased storage ferromagnetic layer coupled to an antiferromagnetic layer with moderate Néel temperature**[27]. The write procedure requires heating above the storage layer blocking temperature and cooling in the presence of a magnetic field. We remind here that the blocking temperature in a ferromagnetic/antiferromagnetic bilayer is the temperature at which the loop shift induced by the exchange coupling across the interface between these two layers vanishes.

25 Dieny B and Redon O, patent FR2832542, US6385082, WO03043017,

26 Prejbeanu I L, Kula W, Ounadjela K, Sousa R C, Redon O, Dieny B and Nozières J-P 2004 IEEE Trans. Magn. 40, Prejbeanu I L, Kerekes M, Sousa R C, Sibuet H, Redon O, Dieny B and Nozières J P 2007 J. of Phys: Cond. Matter 19 165218, Sousa R C, Prejbeanu I L, Stanescu D, Rodmacq B, Redon O, Dieny B, Wang J and Freitas P P 2004 J. Appl. Phys. 95 6783, Kerekes M, Sousa R C, Prejbeanu I L, Redon O, Ebels U, Baraduc C, Dieny B, Nozières J P, Freitas P P and Xavier P 2005 J. Appl. Phys. 97 10P501, Sousa R C and Prejbeanu I L 2005, C.R. Physique 6 1013

27 Sousa R C, Kerekes M, Prejbeanu I L, Redon O, Dieny B, Nozieres J-P and Freitas P P. 2006 J. Appl. Phys. 99 08N904

The write procedure of the *TAS-MRAM* architecture requires heating above the storage layer blocking temperature and cooling down in the presence of a magnetic field. It is obvious that **the temperature increase in the *TAS-MRAM* cell is proportional to the total dissipated power density P_d**. This proportionality between the temperature increase and the power density can be observed directly from the linear decrease of the exchange-bias field both with the total heating power density and also with temperature. The total power density dissipated in the memory cell is essentially determined by the *RxA* product (Resistance x Area product) of the tunnel barrier and by the current density *j*, based on the expression $P_d = RxAj^2$. The maximum power density dissipated through the junction is limited by breakdown voltage of the tunnel barrier and by the maximum current density that can be injected through, given by the relationship: $j_{max} = V_{bd} / RxA$.

The TAS approach has multiple advantages and solves the limitations of the conventional MRAM architecture:

(i) As the selection at write is now temperature-driven, a combination of magnetic field and heating current is required to select a junction - **the addressing errors are strongly reduced**.

(ii) **Only one magnetic field is required to write, leading to reduced power consumption** (even in the presence of a heat current). Furthermore, **the write power can be further reduced, by using circular elements with no shape anisotropy**. In this case the bit orientation is defined by the cooling field that sets the direction of the AF layer. The use of a circular shape eliminates the shape anisotropy term. At the write temperature the exchange energy is cancelled and the barrier height is reduced to the magneto-crystalline anisotropy energy. In addition, each pulse of magnetic field can be shared between several bits (for instance by writing all “0”s in a 32 bit word at once).

(iii) **The exchange bias anisotropy of the storage layer ensures a good thermal stability of the information.** The energy barrier in the case of a TAS-MRAM cell has contribution not only from the shape and the uniaxial anisotropy but also from the exchange energy.

(iv) **Since the system is not anymore bistable at zero field due to the exchange bias, TAS provides good reliability under field disturbance.** Indeed, even if the resistance state of a bit is modified by external parasitic fields under standby conditions, the resistance state after the field perturbation goes back to its initial state.

(v) **TAS-MRAM presents a good scalability since the heating power density P required to heat the junction is proportional to the square of the current density** *j* ($P=RA*j^2$, RA being the resistance area product of the junction). This technology thus scales as the junction area.

In order to quantify the benefits of *TAS-MRAM* with respect to conventional *MRAM* architectures, based on field writing only, let’s calculate the total energy of the memory cell for the different types of configurations. The total energy barrier ΔE corresponding to an elliptical memory cell with in plane magnetization can be written as the sum of the magnetocrystalline, the shape and the exchange bias anisotropy:

$$\Delta E = [K + (AR - 1) \cdot (t / L) \cdot 2\pi M_S^{\,2} + (J_{eb} M_S^{\,2}) / t \cdot (1 - T / T_B)] \qquad (3.1)$$

where *K* is the magneto-crystalline energy, *AR* the aspect ratio, *t* is the thickness of the free layer, *L* is long axis dimension of the memory cell, J_{eb} is the exchange energy, M_S the saturation magnetization, *T* the functioning temperature and T_B the blocking temperature of the antiferromagnet which pins the magnetization of the ferromagnetic storage layer. The energy barrier ΔE of the elliptical MRAM memory cell, being inversely proportional to the bit length *L*, increases significantly as the cell size is reduced. Therefore the required writing field increases rapidly and consequently the write current. The evolution of the calculated write current of a conventional MRAM cell as a function of bit length *L* is represented by open circles in *Figure 3.2*. By comparing the corresponding values of the magnetic field needed for writing to the writing currents needed to heat and switch a circular *TAS-MRAM* cell

(represented by yellow dots), it results that the *TAS-MRAM* architecture becomes advantageous in terms of writing energy for cell diameters lower than 850nm. However large heating currents (represented by red triangles in the figure) needed for large cell surfaces also require a large underneath selection transistor which is detrimental for the memory density. **The region where the *TAS-MRAM* architecture cell is the most competitive is for junction sizes smaller than 250nm**, under which heating currents smaller than 500µA are obtained. I have to mention that usual selection transistors are delivering between 0.5-1 mA/µm².

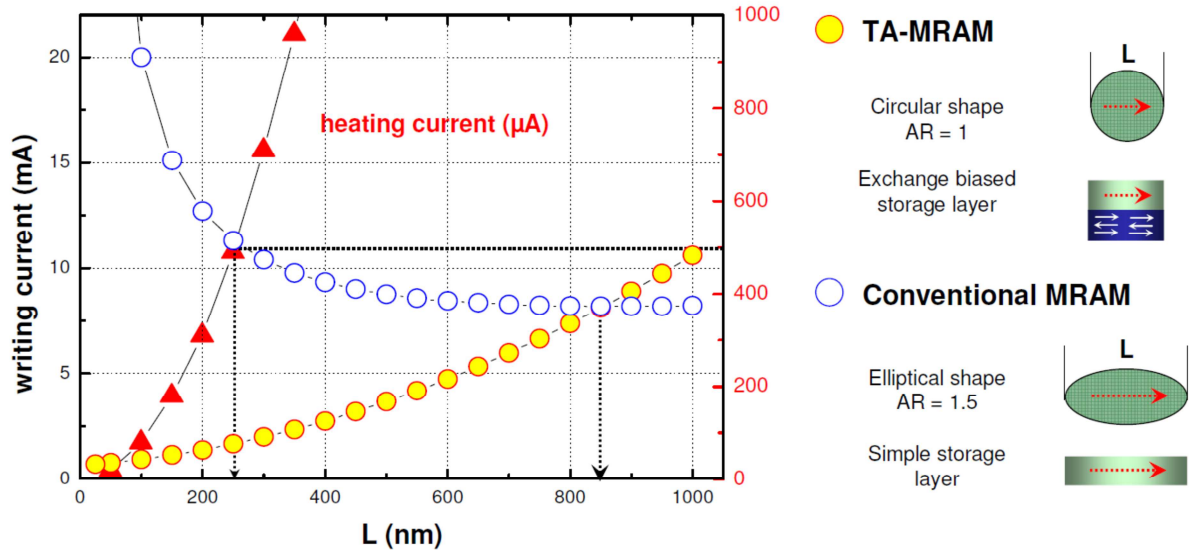


Figure 3.2: Variation of the total writing current for a memory cell versus the bit length for a conventional Stoner-Wohlfarth MRAM architecture (white circles) and a TAS-MRAM architecture (yellow circles) – left axis. For the conventional SW-MRAM, the assumption of an elliptic structure with normal (simple) storage layer was made, while for the TAS-MRAM the cell was assumed circular, with an exchange biased storage layer. The total current represents the sum of current needed to produce two orthogonal magnetic fields for SW-MRAM and the sum of the current generating the magnetic field and the heating current in the TAS-MRAM approach. The heating current is shown by red triangles (right axis). The dashed line delimitates the region in which the TA-MRAM junction is more favorable from bit density point of view. Less current is needed to write the memory cell for the TAS-MRAM approach below a bit length of 850nm. The limiting parameter is the current which can pass through the selection transistor.

In a first implementation of the *TAS-MRAM* architecture, the reference layer is pinned by an antiferromagnetic material with much higher blocking temperature (for instance PtMn with blocking temperatures of 350°C is used in the reference layer) whereas the storage layer antiferromagnet is chosen with a blocking temperature in the range 130°C-180°C depending on the requirements on the device operating temperature range. *Figure 3.3(a)* shows the temperature dependent evolution of the exchange bias field of standard storage (IrMn pinned) and reference (PtMn pinned) electrodes. The pinning properties of the IrMn layer can be tuned by varying its thickness, as shown in *Figure 3.3(b)*. A maximum exchange field of about 250Oe is obtained at 60 Å thick IrMn layer. For this particular thickness, a blocking temperature of about 180°C is obtained – see *Figure 3.3c*.

Several AFM materials are known to have Néel temperature in this range (IrMn, IrMnCr, FeMn). For example, in IrMnCr, the Néel temperature can even be continuously tuned in this range depending on the Cr content. The reference layer is also pinned by an antiferromagnetic material with much higher Neel temperature (for instance PtMn, T_N~700°C has a blocking temperature of ~380°C at 1 hour time-scale). The role of the antiferromagnetic layer is first to pin the magnetization of the adjacent ferromagnetic layer at the standby temperature and second to allow unblocking the magnetization of the storage layer when the temperature is increased above the blocking temperature of the antiferromagnetic layer. This functioning mode provides excellent thermal stability of this layer and therefore excellent retention of the memory. During writing, the cell is heated for a few ns at a temperature of 220°C enabling switching of the magnetization of the storage layer by a small pulse of magnetic field (2-5mT). At this maximum temperature, the magnetization of the reference layer still

remains pinned in the fixed reference direction. Reading is performed at about 3 times lower current density than during write so that the temperature increase during read is negligible (ΔT~10 to 20°C).

The transistor of the selected memory cell is first set in conducting state to let a heating current flow through the magnetic tunnel junction. Within nanoseconds, the inelastic relaxation of the hot tunneling electrons heats up the storage layer, enabling the switching of its magnetization. Then a weak pulse of magnetic field generated by a pulse of current in a bit line located above the selected MTJ is applied (heating plus magnetic field pulse). The heating current is then stopped so that the cell cools back to the standby temperature with the magnetization of the storage layer frozen in the new direction.

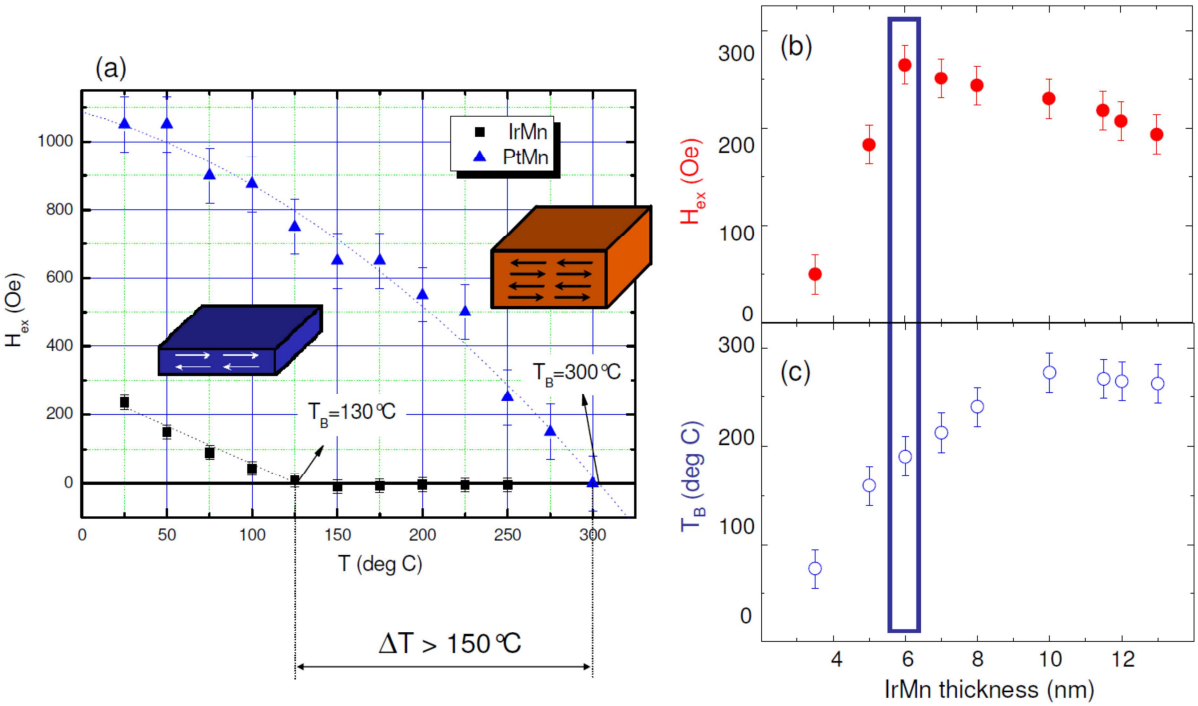


Figure 3.3: (a) Variation of the exchange bias field for the storage and reference layers pinned respectively by IrMn and PtMn antiferromagnets. A low blocking temperature of 130°C characterizes the IrMn layer while the blocking temperature of the PtMn layer is about 300°C. Plots of the exchange bias field (b) and of the blocking temperature (c) as a function of the IrMn thickness.

Figure 3.4 illustrates a TAS-MRAM bit write sequence example combining TAS with a pulse of magnetic field. The writing process starts from a given initial orientation of the magnetization of the exchange biased storage layer for instance representing a low resistance state "0". The corresponding storage layer loop is shifted around a negative field, in the hysteresis cycle before the heating pulse is applied. The reversal of the storage layer bias is achieved by heating the AF layer above its blocking temperature with a current pulse and applying simultaneously an external magnetic field H_{sw} larger than the coercive field of the storage layer. The field is applied in a direction that favors the anti-parallel alignment of the storage and reference layers. The current pulse is terminated and the system is cooled in a magnetic field. The result is a reversal of the pinning orientation of the storage layer and a bit state change to a high resistance "1". As a result the storage layer loop is now shifted towards positive values.

In zero field, only the low resistance state or the high resistance state can be stabilized depending whether a “0” or “1” has been written. This approach makes the *TAS-MRAM* concept quasi immune from magneto-electrical perturbations, which is required for consumer electronics but is also of high interest for spatial applications. Moreover, the data retention at room temperature is improved by the increased effective anisotropy of the storage layer given by coupling of the F layer with the AF one, thus largely increasing the thermal stability factor for equivalent volumes.

Nonetheless, the correct functioning of a *TAS-MRAM* memory imposes other requirements:

- The properties of the antiferromagnet pinning the magnetization of the storage layer have to be optimized such as its blocking temperature to show a very small dispersion from cell to cell and very important no overlap with the blocking temperature distribution of the reference layer.
- The exchange bias field of the storage layer has to be large enough to guarantee one single stable state at zero field, i.e. large hysteresis field shift and reduced coercivity.
- Improved heating properties, namely reduced thermal losses, both vertically in the stack and on the sidewalls

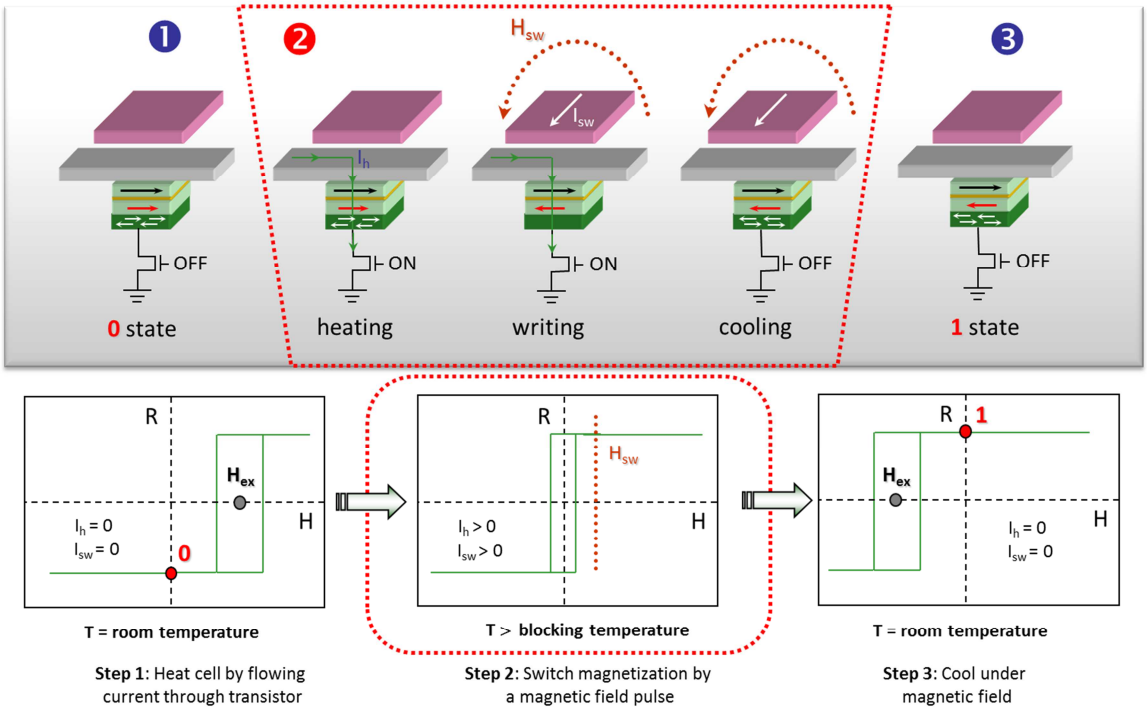


Figure 3.4: Writing steps in the Thermally Assisted TAS-MRAM architecture: Step 1: The cell is heated by flowing a current through the transistor and the memory cell; Step 2: Once the cell is heated above the blocking temperature of the antiferromagnet pinning the ferromagnetic storage layer, an external field, larger than the coercive field at the heating temperature is applied to switch the magnetization; Step 3: the system is cooled down under the applied magnetic field

3.2 HEATING IN MTJS

In magnetic tunnel junctions, the heating of the storage layer can be produced in a simple way by taking advantage of the heat dissipation around the tunnel barrier. **The principle behind the heat generation in a MTJ structure is a combination of the Joule heating in the metallic electrodes and of the inelastic scattering of tunneling hot electrons which takes place when the tunneling electrons penetrate as hot electrons in the receiving electrode after their ballistic tunneling across the tunnel barrier** – see *Figure 3.5*. Classical Joule heating produces energy per unit time equal to ρj^2 where ρ is the electrical resistivity and j is the current density. In addition the tunnelling electrons will lose their energy by inelastic scattering at the arriving electrode. This generates phonons (vibrations of the crystal lattice) and magnons (excitation mode or spin waves)[28] that macroscopically translate into a temperature increase (ΔT). The energy carried by each injected hot electron is proportional to the voltage drop V and the number of electrons that tunnel given by the current density j. The corresponding energy produced per unit time is equal to $(j\ V/\ \lambda_{inel})\ exp\ (-x/\lambda_{inel})$, where x is the

28 Zhang S., Levy P., Fert A., *Mechanisms of spin-polarized current-driven magnetization switching*, Phys. Rev. Lett., 88, 236601 (2002);

stack position, *V* the applied bias voltage, and λ_{inel} the inelastic scattering mean free path of the electrons

With these assumptions we can write a simplified one-dimensional heat equation, which includes also the heat diffusion term $K*(\partial^2 T/\partial^2 x)$ due to the heat diffusion in the leads:

$$\left[c_p d\frac{\partial T}{\partial t}\right]-\left[K\frac{\partial^2 T}{\partial^2 x}\right]=\left[\rho j^2\right]+\left[\frac{jV}{\lambda_{inel}}\exp\left(-\frac{x}{\lambda_{inel}}\right)\right] \qquad (3.2)$$

The symbols used in this equation have the following correspondence: c_p *is the* heat capacity, *d is the* mass density, *T* the temperature, *t* the time and *K* the heat conductivity. This equation has been solved for the 1D and 3D cases using a numerical finite difference method with boundary conditions. The current density is assumed to be uniform and is calculated as $j=V/(R\times A)$, where $R\times A$ is the resistance area product of the junction. As an example, in MTJs having an *RxA* product of the order of 30Ω.µm² and for heating current densities of the order of 10^6A/cm², a rise in temperature ΔT of the order of 200°C is typically achieved[29] within 5ns. One way to increase the heating efficiency and reduce the power density is to insert low thermal conductivity materials at both ends of the magnetic tunnel junction stack, serving as thermal barriers between the junction and the electrical leads. This confines the heat to the junction volume, preventing lead heating and possible thermal crosstalk[30].

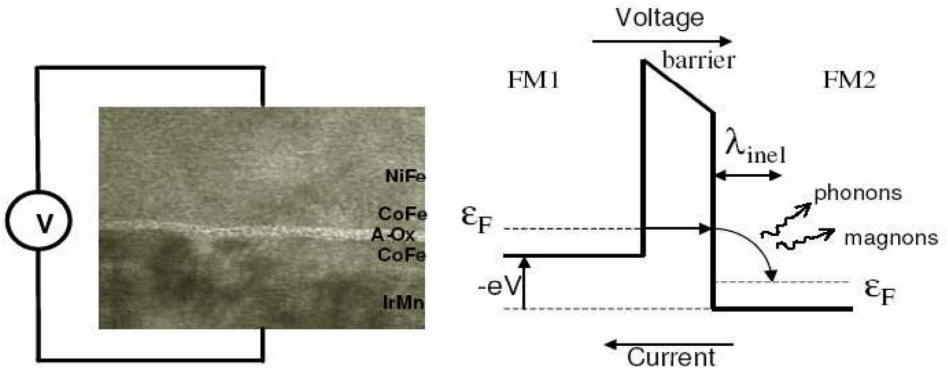


Figure 3.5: Heating process induced by a current injected through the tunnel barrier

3.2.1 Heating asymmetry vs current polarity

It is important to mention that the direction of the tunneling current in magnetic tunnel junctions can have a significant influence in the final temperature profile within the MTJ as there is an asymmetry in the heating depending on the polarity of the write pulses (flow direction). These results, demonstrated **during the PhD thesis of Erwan Gapihan**, are shown in *Figure 3.6*: on the left side, the experimental results, and on the right side finite element method thermal simulations. They are indicating that the temperature rise in the vicinity of the tunnel barrier for standard *TAS-MRAM* write conditions may vary by as much as 10%, depending on the voltage polarity/current direction. This heating asymmetry is attributed to the mechanism of energy dissipation during tunneling and particularly to the relaxation of hot electrons in the receiving electrode. In the transport of electrons tunnel there is a different energy potential between both sides of the barrier. Heat is generated in two different locations in the magnetic stack, which determines as a function of the sense of the injected current two different temperatures at the antiferromagnetic storage layer.

29 Sousa RC; Prejbeanu IL, *Non-volatile magnetic random access memories (MRAM)*, COMPTES RENDUS PHYSIQUE Volume 6, Issue 9, 1013-1021 (2005)

30 S. Cardoso et al, *Double-barrier magnetic tunnel junctions with GeSbTe thermal barriers for improved thermally assisted magnetoresistive random access memory cells*, Journal of Applied Physics 99(8) (2006)

This asymmetry could not occur if the heating was produced entirely by Joule effect because this effect is not dependent on the current direction. The effect can be advantageously used, by properly choose the sense of the injected current for write and read, to increase the heating efficiency in TAS-MRAM cells or to minimize the temperature increase of the storage layer while reading cell data.

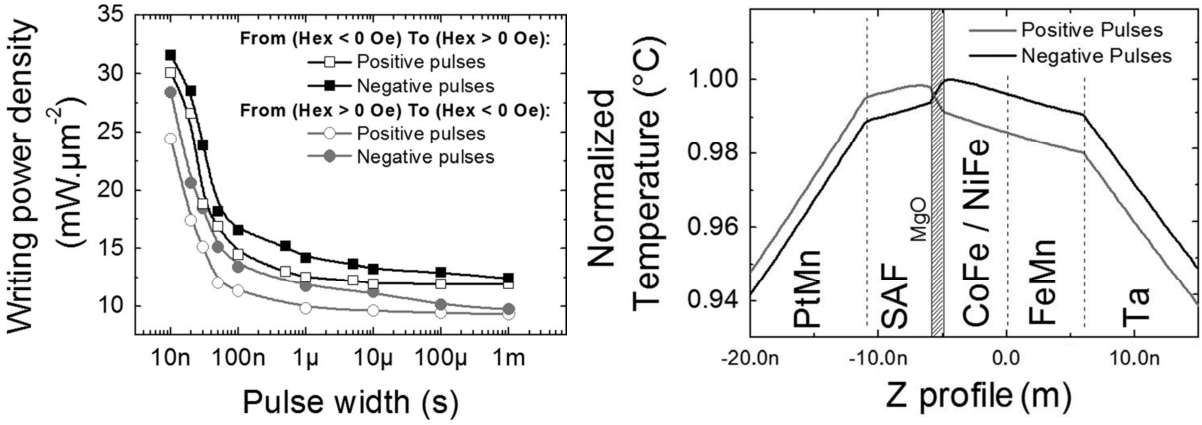


Figure 3.6 : left - Variation of the power density needed for writing with different current and magnetic field polarities; Right – Simulated temperature profile as a function of the polarity of the current injected through the junction

3.2.2 Heating and cooling dynamics

One of the requirements needed for the *TAS-MRAM* write cycle to be competitive is to have similar writing time with respect to conventional magnetic field induced switching MRAM architectures, about 3-7ns[31]. In *TAS-MRAM*, the total duration of the write cycle is determined by the heating and cooling dynamics and the speed at which cells can be re-written after an initial write. We have shown **during the postdoc of Cristian Papusoi** that the heating and cooling times can be indeed competitive, on the order of 30 ns[32].

The heating time varies inversely proportional to the heating power sent through the MTJ. A good compromise was found for heating duration of the order of 1 to 5 ns, for which the applied voltage is still not too close to the breakdown voltage of the MgO tunnel barrier.

The cooling time is determined namely by the thermal properties of the MTJ stack and of the material encapsulating the cell (specific heat, thermal conductivity). The cooling rate of *TAS-MRAM* cells has been extracted experimentally through a sequence of two applied pulses, as described in *Figure 3.7*.[33] The measurement principle is the following: an initial heating pulse applied to the magnetic tunnel junction induces a temperature rise at the blocking temperature of the antiferromagnet pinning the storage layer. A second pulse is then applied at increasing delays after the initial pulse. The second pulse also results in a temperature increase that adds to the resulting temperature increase from the first pulse. If the time interval between the two pulses is long enough for the temperature to completely decay to the initial temperature value, the second pulse requires a write power density equal to that for a single isolated pulse. If this interval is shortened, a decrease in write power density is observed. The lowest power density is obtained when both pulses are consecutive. From the write power density evolution in *Figure 3.7*, the characteristic cooling / heating time constant τ of the cell has been determined as 4-6 ns for MTJ stacks without thermal barriers and 14-16ns in MTJ stacks having a thermal barrier.

31 Koch R.E., Deak J.G., Abraham D.W., Trouilloud P.L., Altman R.A., Lu, Y., Gallagher W.J., Scheuerlein R.E., Roche, K.P., and Parkin S.S.P., *Magnetization Reversal in Micron-Sized Magnetic Thin Films*, Phys. Rev. Lett. 81, 4512 (1998).

32 Papusoi C, Conraux Y, Prejbeanu IL, Sousa RC and Dieny B J. Magn. Magn. Mater. 321 2467 (2009)

33 Papusoi C., Sousa R., Herault J., Prejbeanu I.L., Dieny B., *Probing fast heating in magnetic tunnel junction structures with exchange bias*, New J. Phys. 10, 103006, 2008

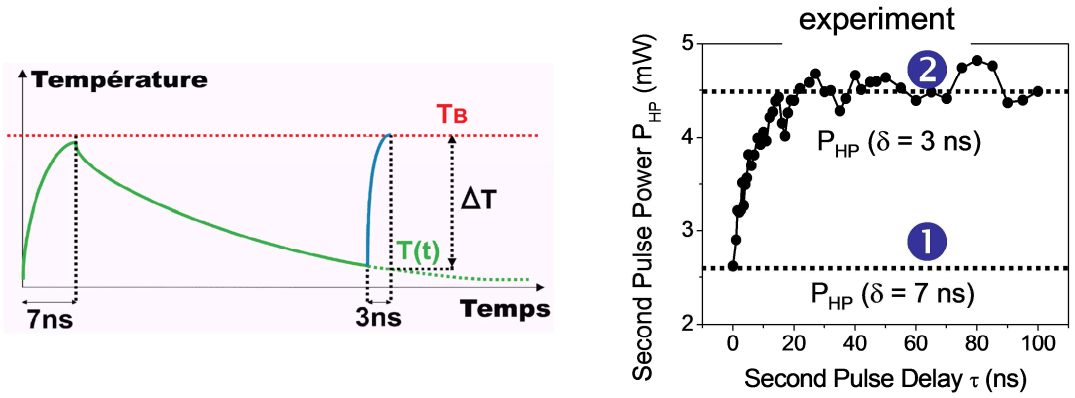


Figure 3.7: Left: Principle of the two pulses experiment for determining the cooling rate of TAS-MRAM cells. Right: Write power required for writing with a second pulse of current (3ns long) after application of a first heating pulse (7ns long), the two pulses being separated by a varying delay. The experiment was carried out on a stack with thermal barrier.

Measurements of the write power density as a function of pulse width from 300ps to 300ns (*Figure 3.8*) show the existence of four different heating regimes in this time range:

i) a sharp increase of the power density for pulses shorter than 4ns in region 1,
ii) region 2 between 5 and 10ns where the power density is almost constant,
iii) a slow decrease of the power density in region 3 between 20 and 100ns,
iv) followed by an almost constant power density in region 4, for pulses larger than 150ns.

The physical origin of the different heating mechanisms could be identified using thermodynamic numerical simulations of the time resolved heat equation. Generally, if at *t=0* a power density P_d is delivered to the tunnel junction, the temperature within the junction evolves according to the following equation: $T = T0 + \Delta T\ [1 - exp\ (-t/\tau)]$, where T_0 is the initial temperature at *t=0*, ΔT the temperature increase and τ is the characteristic heating time. Below 4ns, it is possible to write the cell at the cost of an increased power density. This is mostly an adiabatic heating regime where the heat remains confined to the junction region. The tunnel junction pillar reaches equilibrium in region 2, the bottom and top leads still remaining close to T_0. For longer heating pulses, in region 3, a gradual increase of the leads temperature takes place, as the power dissipated in the junction flows into the leads. Smaller junction sizes dissipate less power, resulting in less heating of the junction leads. Since the temperature increase of the leads adds to the temperature increase of the junction itself, larger junctions result in lower power densities because of the higher leads temperature increase. Finally in region 4 the junction pillar and also the leads both reach an equilibrium temperature.

The power density required to write the cell shows the different regions being heated during the pulse. At times <5ns only the regions adjacent to the tunnel barrier are being heated and the required write power density is rapidly increasing as the pulse duration decreases. We were able to reverse the exchange direction of our storage layer with heating pulses as short as 500ps. At 30ns thermal equilibrium in the stack is achieved creating a plateau. For larger pulse widths the

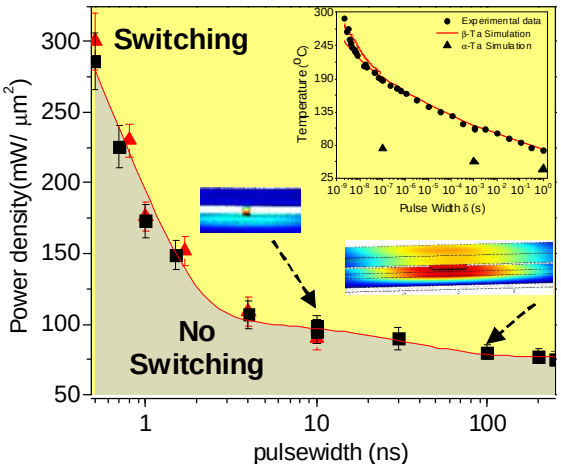


Figure 3.8: Write power density of a TA MRAM cell can be related to the temperature of the storage layer. At times <30ns the heating is mostly confined to the pillar, while for longer times the temperature increase extends to the electrical leads. Experimental data is accurately fit by 3D thermal simulation.

top and bottom electrical leads are heated. All these different regions were also confirmed in 3D thermal simulations. This shows the potential for using the AF blocking temperature as a local thermometer and gain access to thermodynamic parameters in thin patterned films.

These apects were studied in detail during the PhD thesis of Marta Kerekes and during the postdoc of Cristian Papusoi.

3.3 DEMONSTRATION OF TAS-MRAM WRITE OPERATION

The first demonstrations of *TAS-MRAM* writing procedure were realized at Spintec and INESC either statically, for DC currents[34], or dynamically, for injected current pulses down to 10ns[35]. In DC current experiments, the exchange bias field of the storage layer was reversed in micronic junctions (2x2µm²) using a heating DC power density of 3.2mW/µm² applied in the presence of a 20Oe field. The typical stack structures schematically represented on *Figure 3.8 (top)* is: buffer layer: Ta 3/ CuN 60/ Ta 3/ reference layer PtMn 20/ CoFe2 / Ru 0.8/ CoFeB 2/ tunnel barrier: MgO 1.1 +Ox / storage layer: CoFeB 2 / Ta0.2 / NiFe 3/ IrMn 6.5 (all thicknesses in nm). A Ta 0.2nm thick lamination layer was inserted inside the storage layer to decouple crystallographic structures of the MgO bcc(001) and NiFe fcc (111) – confirmed by the TEM cross section in the figure - and guarantee simultaneously high tunnel magnetoresistance and large exchange bias values[36]

Figure 3.9 also shows the evolution of the hysteresis loops of the storage layer as a function of heating current density. As the heating current increases, we observe first the decrease in the exchange bias field and second a reduction of the TMR (tunnel magnetoresistance), linked to the TMR dependence with the applied voltage. At the highest heating current density, the loop is centered, meaning that the exchange bias has vanished and low fields of a few milliteslas are then sufficient to switch the storage layer magnetization. The write sequence of the memory cell, illustrated in the bottom drawing in *Figure 3.9* starts from a given initial orientation of the magnetization of the exchange biased storage layer for instance representing a low resistance state "0". The corresponding storage layer loop is shifted around a negative field in the hysteresis cycle before the heating pulse is applied (red curve). As described in the functioning principle of the *TAS-MRAM* concept, the reversal of the storage layer bias is achieved by heating the AF layer above its blocking temperature with a current pulse and applying simultaneously an external magnetic field larger than the coercive field of the storage layer. The field is applied in the direction parallel or antiparallel to the reference layer magnetization depending whether a “0” or a “1” is to be written. In the writing example presented in *Figure 3.9*, a “1” state is written. The heating current pulse is then stopped and the system cools down in an applied external magnetic field. This maintains the storage layer magnetization in the field-cooling direction during its freezing. The result is a reversal of the pinning orientation of the storage layer magnetization and a bit state change to a high resistance "1". As a result the storage layer loop is now shifted towards positive values (blue curve in *Figure 3.9*).

34 Prejbeanu I.L., Kula W., Ounadjela K.; Sousa R.C., Redon O.; Dieny B.; Nozieres J.P., *Thermally assisted switching in exchange-biased storage layer magnetic tunnel junctions*, IEEE Transactions on Magnetics 40, No. 4, (2004)

35 J. Wang and P. P. Freitas, *Low-current blocking temperature writing of double barrier magnetic random access memory cells*, Appl. Phys. Lett. 84, 945, (2004)

36 I.L. Prejbeanu, C. Maunoury, D. Ducruet, B. Dieny, R. Sousa, Magnetic element with thermally assisted writing, 2007FR-0059584: 5/12/07 – granted FR2924851, US7898833

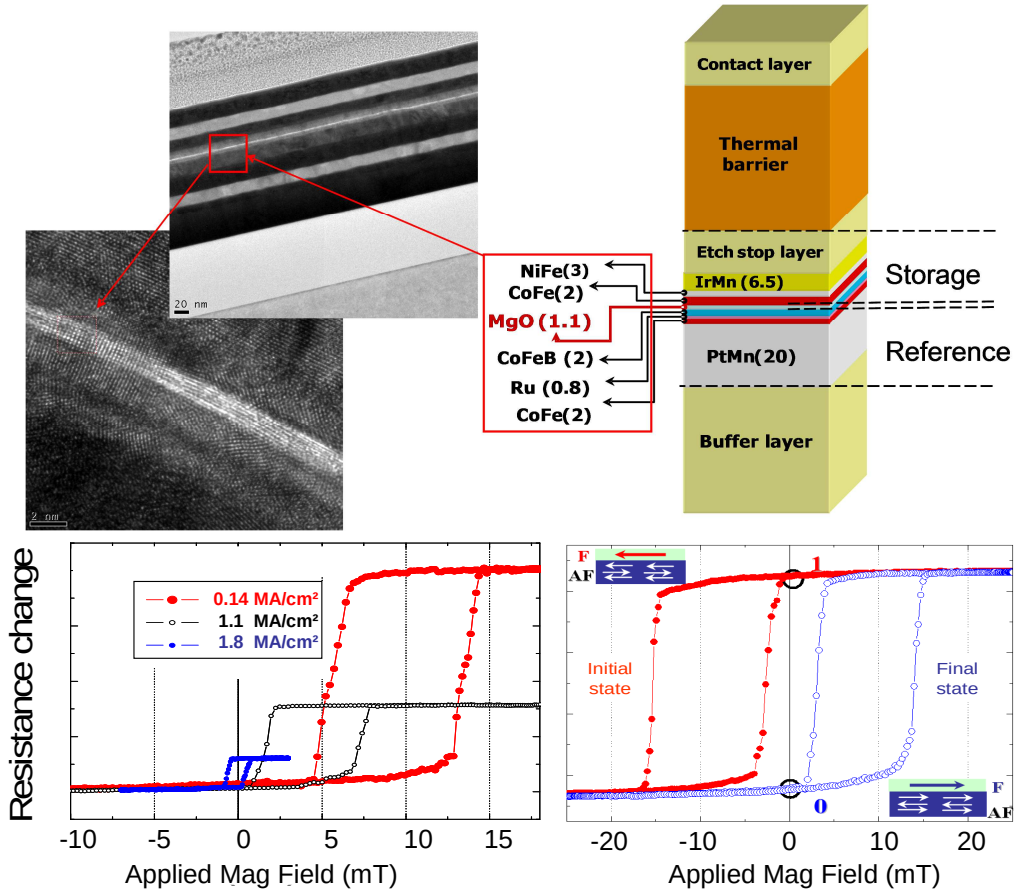


Figure 3.9: Top: Composition of the TAS-MRAM MTJ stack and cross-sectional high resolution TEM (transmission electron microscopy images) of the MTJs. Bottom left: Hysteresis loops of the storage layer as a function of heating current density showing the decrease in the pinning as the heating current increases. At the highest heating current density, the loop is centered, meaning that the exchange bias has vanished and low fields of a few milliteslas are then sufficient to switch the storage layer magnetization. Bottom right: Resistance hysteresis loops of the exchange biased storage layer before (red) and after (blue) writing, showing the inversion of the hysteresis loop shift. Note that in both cases, only one remnant state is stable at zero field: either the low or high resistance state, meaning that the memory is very stable against perturbing external fields[37].

Subsequent dynamic writing demonstrations of *TAS-MRAM* using 20ns long current pulses were realized on sub-micron junctions[38]. A power density of 20-30mW/µm² is sufficient to increase the temperature of the tunnel junction (MTJ) by about 200°C within a few ns. For *RxA* product values of 50Ω.µm² this translates into a current density of about $2x10^6$A/cm², which is of the same order of magnitude as the current densities range required for spin transfer torque induced switching.

After this initial demonstrations of the thermally assisted MRAM the goal was to optimize the heating efficiency and to reduce the overall power consumption.

37 Prejbeanu IL; Kerekes M; Sousa RC; Sibuet H; Redon O; Dieny B; Nozieres JP, Journal of Physics: Condensed Matter. 19(16) (2007)

38 J. Wang and P. P. Freitas, *Low-current blocking temperature writing of double barrier magnetic random access memory cells*, Appl. Phys. Lett. 84, 945, (2004)

3.4 REDUCING THE POWER CONSUMPTION

3.4.1 Minimization of the heating power by using thermal barriers

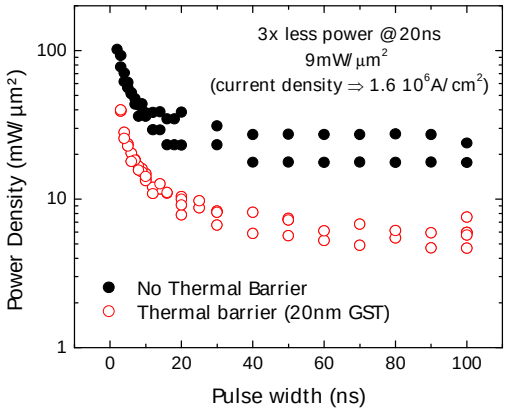


Figure 3.10: Comparison of heating power density for writing with and without in-stack thermal barriers.

One way to increase the heating efficiency and reduce the power density is to insert low thermal conductivity materials at both ends of the magnetic tunnel junction stack, serving as thermal barriers between the junction and the electrical leads (for example BiTe thermal barrier with 1.5W/mK thermal conductivity). This confines the heat to the junction volume, preventing lead heating and possible thermal crosstalk. Furthermore, using thermal barriers provides good scalability as there is no dependence of the power density needed to heat upon varying the junction size. The thermal barrier requires a thermal conductivity below 1.5W/m/K, but at the same time the material needs to be electrically conducting. Such properties can be achieved for example with chalcogenide phase change materials in their crystalline phase[39]. Electrical and magnetic properties of a tunnel junction with the integrated thermal barrier were already tested by the group at INESC from Lisbon Portugal This principle was applied to reduce the write power density by a factor of 3, when compared to cells without thermal barrier, as illustrated in *Figure 3.10*. In this case a 20nm thick layer of GeSbTe alloy was used to confine the heat, resulting in a write power density below 10mW/μm² and a current density of 1.6E^{6}A/cm² for pulse widths of only 15-20ns. **These aspects were studied in detail during the PhD thesis of Marta Kerekes**.

3.4.2 Minimization of the heating power by using AF materials with low Néel temperature

Another possibility to reduce the write power density is the use of AF materials with lower Néel temperature. Indeed, as the write pulse width decreases from the quasi-static limit to below 10ns, an increase in the required heating power density is observed. This increase is the consequence of the blocking temperature dependence on the measurement time. For longer times, the exchange loss is helped by thermal relaxation, resulting in typical blocking temperatures that are much lower than the AF Néel temperature. As the pulse width is decreased, the blocking temperature increases and become closer and closer to the Néel temperature of the AF material. This is illustrated in *Figure 3.11*, which compares the heating write power using IrMn with that for FeMn which has a much lower Neel temperature (T_{Neel}~400°C for IrMn whereas T_{Neel}~220°C). The results highlight the increase in T_B with the thickness of the IrMn AF layer (for thicknesses ranging from 4.5 to 8.5nm) while for larger thicknesses (8.5 and 10.5nm) we found similar writing power density values regardless of the heating pulsewidth. The thickness dependence of the "dynamic" results is similar to quasi-static blocking temperature. The dependency of the power density with the pulse duration has highlighted 2 important results:

1. **The thermally activated dependence of the unblocking the storage layer which increase the power density when writing time is reduced**
2. **The dependence of power density with the thickness of the AF.**

39 Cardoso, S., Ferreira, R., Silva, F., Freitas, P.P., Melo, L.V., Sousa, R.C., Redon, O., MacKenzie, M., and Chapman, J.N., *Double-barrier magnetic tunnel junctions with GeSbTe thermal barriers for improved thermally assisted magnetoresistive random access memory cells*, Journal of Applied Physics 99, 08N901 (2006)

These two results taken together are crucial from an application point of view, because they can show that if the power density required to write at short pulsewidths increases, its thickness dependence gives us a lever to adjust the heating part of the writing power density. Nevertheless any thickness reduction will also reduce the static blocking temperature, so this solution is not ideal. To put these results in the context of the temperature range, we can say that the thickness of the AF is a lever that allows either to:

- Increase the width of the operating temperature range by increasing the AF thickness but also the voltage and power needed for writing.
- Reduce the voltage and writing power by reducing the operating temperature range.

A last remark is the significant increase (3 times) in power density when the heating pulsewidth is reduced from 100ns to 10ns. T_B dependencies on the AF thickness and heating pulsewidth are in agreement with the observed behavior of the write power density. Note also that for larger IrMn thicknesses (namely 8.5 and 10.5nm), the estimated blocking temperature approaches the IrMn Néel temperature (420°C[40]). If we imagine the extreme case where the heating time tends to zero, the thermal activation has more time to act on the release of AF and the exchange coupling disappears only if we reach the temperature at which the anisotropy of AF disappears, that is to say, the Neel temperature.

The sharp increase in write power density remains an important issue from an application point of view for which solutions were required. FeMn AF layer was namely used to lower the write power densities at short pulsewidths.

In terms of application, this means that it is conceivable to control the thermal stability of the AF over long periods and therefore the operating temperature range of the memory, by adjusting structural parameters such as the thickness of AF or the size of its grains.

In addition, it is possible to set an upper bound to the write temperature devices by acting on the Neel temperature, so a priori by changing the AF material. In an attempt to verify this hypothesis, writing power density measurements as a function of pulse duration and thickness of AF were reproduced using memory cells comprising storage layers trapped by FeMn whose Neel temperature (~210°C) is lower than that of IrMn. T_B measured at 170°C for 13nm thick FeMn (estimated at 140°C for the corresponding memory cells) shows that it is possible to find a thick FeMn layer for which there is a T_B close to those measured in IrMn for thicknesses ranging between 4.5 and 8.5nm.

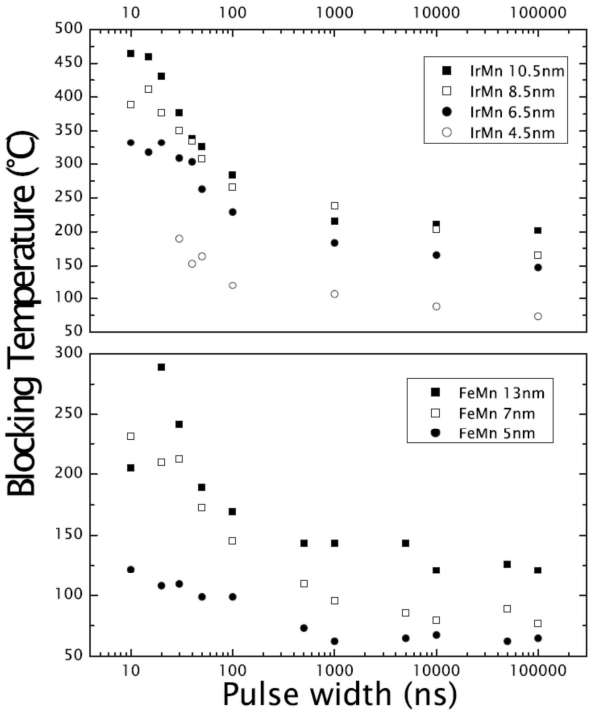


Figure 3.11: Dynamic blocking temperatures for different IrMn (a) and FeMn (b) AF thicknesses measured as a function of the heating pulsewidth

Even if similar trends are found for the FeMn layer, the maximum value of temperature calculated for achieving the shortest pulse durations is significantly lower in case of FeMn – *Figure 3.11*. For IrMn, this temperature is about 400-450 °C for the larger thicknesses, close

40 Nogués, J. & Schuller, I. K., *'Exchange bias'*, Journal of Magnetism and Magnetic Materials 192(2), 203-232. (1999)

to the Néel temperature of IrMn, while in the case of FeMn, the maximum temperatures reached are of the order 200-250°C, i.e. a temperature close to the Néel temperature of FeMn.

From an application point of view, the thermally activated character of T_B has rather negative consequences, because by reducing the blocking temperature for the longer heating time, thermal activation in AF is against the thermal stability of the memory cell and poses a problem retaining information in memory cells. Indeed, as the condition $H_{ex} > H_c$ is filled, the information is stable in the memory cell, but the destabilization of grains of AF over long durations resulting in the reduction of the exchange field, can break this condition stability. Conversely, during the writing process, the short time involved and the role reduced left to thermal activation in the unpinning of AF increase the temperature necessary to change the information in the memory cell.

The direct consequence of such dependence is to adjust the memory points operating temperature range by adjusting the thickness of AF. Nevertheless, the existence of this dependence throughout the explored heating time range is a problem for writing, because the increase in the thickness of AF leads to higher blocking temperatures both static and dynamic and therefore implies a power overhead to reach the write temperature. From a technological point of view this means the need for larger selection transistors, limiting the scalability of the memory and writing voltages that approaches the breakdown voltage of the MTJ, reducing its endurance. The difference between the limit operating temperature and the write temperature must be reduced. The comparison of results between IrMn and FeMn showed very encouraging results.

In conclusion, the initial approach of adjusting the thickness of IrMn for adjusting the *Tb* and consequently the operating temperature range without taking into account the difference between static and dynamic blocking temperatures proved limited. Comparing the results obtained for the IrMn and FeMn shows that the thermal stability of the AF over long periods of heating pulses and therefore the operating temperature range of the memory is controllable by optimizing the structural parameters of the AF such that its thickness while the relevant parameter for adjusting the write temperature is the Néel temperature. This allows considering at the same time an extension of the operating temperature range, increasing the thickness of AF, and a reduction of the write temperature, replacing the IrMn by a FeMn. By showing first that FeMn allows, by adjusting its thickness, to obtain static blocking temperatures of the same order of magnitude as those of IrMn, and second that the power densities required to write a memory point on a short time are significantly lower than those required for an IrMn layer, the FeMn was identified as a much better candidate than the IrMn for optimizing the operation of the TAS-MRAM. The conversion of the write power densities blocking temperatures in each case suggests that the characteristic mainly responsible for this improvement is the lowest Néel temperature of FeMn, which is a limit value in the blocking temperatures for the heating pulses shorter. Thus, it is through the extrinsic parameters of the AF as the thickness that can be played on static blocking temperature while it is an intrinsic parameter, the Neel temperature, which becomes relevant from the point of for writing the TAS-MRAM. **From an industrial point of view, all these results show first of all that the use of FeMn as the AF of the storage layer makes a significant improvement to the extent that it allows to maintain the temperature range of operation permitted by the IrMn while reducing the write temperature at a reasonable level from the point of view of other operating criteria such as power consumption, or write voltage which impacts the endurance of memory.**

This changes our outlook on writing memory points to consider allowing greater T_N write temperature. Indeed, as the write temperature is lower than T_N, the release of the storage layer which rests on the thermal activation of the grains of the antiferromagnetic remains a stochastic process, which is attached a writing probability that there is no guarantee as to exactly equal 1. But if writing is performed at a temperature higher than its T_N, then the antiferromagnetic becomes paramagnetic and can no longer contribute to the effective anisotropy of the storage layer. These effects of the exchange coupling disappear completely, which ensures a probability of 1 for unblocking the storage layer.

This approach makes sense when we consider the operation of the memory as a whole and not just a single memory cell. To enable the increase of the memory size by limiting the occurrence of defective memory cells or writing errors it is imperative to minimize all the dispersions of the characteristics of the memory points. In the case of writing it is necessary, not only that all the memory cells can be written, but also that the distribution of writing temperatures is as low as possible.

The use of FeMn together with thermal barriers opened a way to reduce the write power density close to 5mW/µm², and current densities in the 10^5A/cm² range. This low write density can be combined with low switching fields, with values as low as 20Oe demonstrated. In conventional field write approaches such low switching fields would result in unstable cells, but in the thermally assisted approach, it is possible to combine low writing fields once above the blocking temperature and good thermal stability of the cells.

These aspects were studied in detail during the PhD thesis of Lucien Lombard and Erwan Gapihan.

3.4.3 Minimization of the power consumption by writing strategies

Field writing combined with thermal assistance is also advantageous in terms of power consumption in MRAM chips by offering the possibility to share the pulse of magnetic field among numerous bits. Indeed, in a RAM, the bits are usually not written randomly one by one but word by word. Each word may contain 32 or 64 bits. To write a full word, only two pulses of magnetic field are required.

Figure 3.12 shows how the power consumption can be minimized by using only two pulses of magnetic field to write an entire word. In a first step, all bits in the word which have to be written to “0” are heated simultaneously by sending a heating current through the corresponding MTJ. Then the “0” field is applied, the heating currents are switched, and the heated cells cool down in the “0” magnetic field so that these cells freeze in the “0” configuration. The cells which are not heated do not switch so that they remain in their original state. In a second step, all bits which have to be written to “1” are heated simultaneously and the “1” magnetic field is applied by sending a current in the corresponding word line. The heating currents are then stopped while the “1” field is still one so that the heated cells now freeze in the “1” configuration. At the end, the whole word has been written with 32 pulses of heating current (assuming a 32-bit word) --- the corresponding energy is ~1pJ per dot --- plus two pulses of magnetic field.

Furthermore, in TAS-MRAM, since the thermal stability of the storage layer magnetization in standby is provided by exchange coupling to an adjacent antiferromagnetic layer, the cell can have a circular shape. As a result, once the writing is enabled by heating the cell above the blocking temperature of the antiferromagnetic layer, only a low field of a few millitesla (2 to 5 mT) is sufficient to switch the storage layer magnetization since the cell has no shape anisotropy.

For power consumption comparison, consider the case of toggle MRAM. Writing a bit in a toggle MRAM requires two orthogonal pulses of magnetic fields. To write a 32 bits word, one of these pulses can be shared by the 32 bits of the same word by sending a pulse of current along the corresponding word line. However, 32 pulses of magnetic fields must be independently generated along the corresponding 32 bit lines. This means that 33 pulses of magnetic field of about 10 mT each must be generated in toggle MRAM.

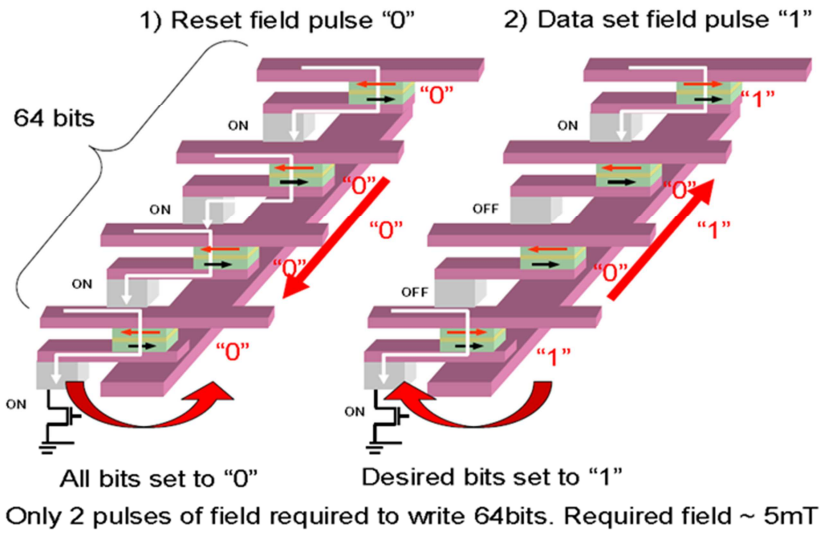


Fig. 3.12 – Power consumption optimization by using only two pulses of magnetic field to write entire words. Energy of a heating pulse~1pJ. Energy of a field pulse~35pJ. In a first step, all bits are heated and reset to "0" with a "0" field pulse. In a second step only the bit to be written "1" are heated together with application of a "1" field pulse.

3.5 IMPROVED EXCHANGE BIAS PROPERTIES

Other key parameters for *TAS-MRAM* performance improvements are:

- the control of the dispersion of exchange bias from one bit to another,
- the tuning of blocking temperature and operating temperature range,
- the optimization of exchange bias coupling itself.

The focussed Kerr measurements on patterned dots allowed having a qualitative evaluation of exchange bias variability. The study showed that both micromagnetic and microstructural properties have consequences on exchange variability. We have also shown that sandwiching an IrMn layer between two ferromagnetic layers having orthogonal anisotropy directions significantly increases the exchange bias loop shift via the improvement of the antiferromagnetic grains thermal stability. Dusting a thin Cu layer at the F/AF interface brings a concave curvature of the EB loop shift temperature dependence, which is of primary importance for MRAM cells. **These aspects were studied in detail during the PhD thesis of Giovanni Vinai**.

3.5.1 Impact of the micromagnetic configuration of the ferromagnetic layer

Local measurements directly showed that the hysteresis loops of nominally identical stacks and dots strongly vary from dot to dot. The exchange energy variability appears to be more important when the magnetization reversal in the ferromagnetic layer takes place via multidomain configuration. **Atomistic simulations showed that micromagnetic effects in the F layer are responsible for AF grain instabilities on the edges of the dot.** These effects, due to the dipolar interactions, are present for thick enough F layers and become more important when the lateral dot size is reduced. Fortunately, the variability is less pronounced when thinner magnetic layers are used which corresponds to the situation of practical interest for MR readers or MRAM.

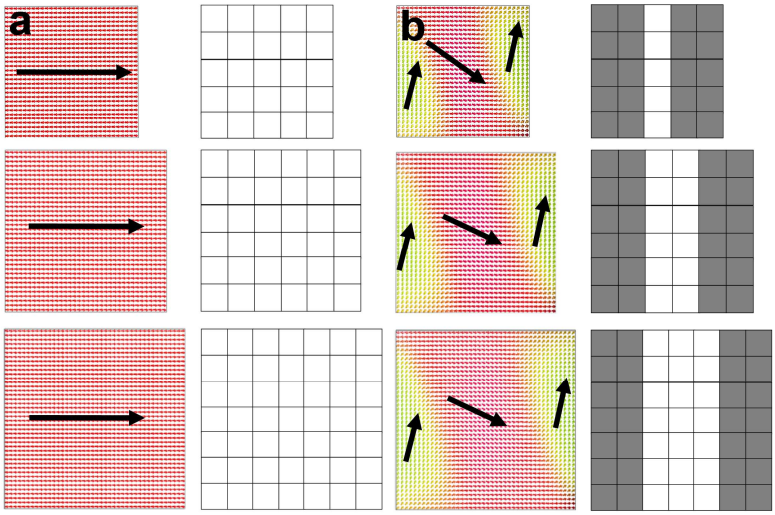


Figure 3.13 – Spin configurations at remanence and AF grain states (white or grey) at negative saturation for thin (1.6 nm) (a) and thick (12.8 nm) (b) F layer for three different dot sizes. The different grain shades distinguish their behaviors during magnetization reversal (white: the AF domain walls move reversely; grey: they go through the layer and disappear at the top surface).

Figure 3.13 shows that for thin F layers the domain walls of all the AF grains remain stable, whereas for thicker F layer the spin lattice completely switch during the loop in the AF grains located at the dot edges. This reversal is due to the different positions of the domain walls along the thickness of the AF grains. During the magnetization reversal, the grains close to the border present a domain wall that propagates deeper through the AF layer compared to the grains in the center. This is attributed to the different spin configuration in the F layer at remanence. The presence of a strong interface coupling at the F/AF interface tends to align the F spins along the easy axis direction because of the strong AF anisotropy. Whereas for thin F layers, all spins are aligned along the setting directions, this effect becomes less pronounced on thick F layers. In this case, the contribution of the dipolar field on F magnetization becomes more important, particularly along the edges of the dots. Because of the creation of a pronounced S state at remanence, the magnetization at the dot edges is already strongly distorted at remanence. As a result, the F magnetization is locally exerting earlier a torque on the AF spin lattice of the grains located at the edges than on the grains located in the bulk of the dots. The reversal process through the formation of a multidomain configuration further contributes to differentiate the behaviour of AF grains at edges and in the bulk of the dots. Note that these edge effects are only due to the micromagnetic behaviour of the F layer, induced at the surface by the dipolar interactions. It is clear that the edge effects become more and more significant when the size of the dot is reduced, as a result of the increase in the surface/volume dot ratio.

The variation of the F thickness led, because of the competition between dipolar and exchange energies, to the observation of two different mechanisms of magnetization reversal

- in the thin F regime, dots showed on MFM measurements under in-situ applied field a coherent magnetization reversal;
- in the thick F regime, dots passed through a multidomain configuration, whose spin configuration was determined by atomistic simulations.

The presence of two different micromagnetic regimes had important consequences on the exchange bias variability. Dots in the multidomain regime showed a larger exchange energy variability compared to those in the single domain regime. This increase in variability becomes even more important if the lateral size is reduced. The origin of this increased variability has been analysed by atomistic simulations. Dots in the thick F regime showed instability of the AF grains at the borders, due to the dipolar interaction with the F spins and to the earlier torque exerted by the F spins at remanence. The results of the study showed how the formation of multidomain configurations in the F layer has

detrimental effects on the exchange variability, due to an increasing instability of the AF grains in the borders. **For this reason, the F layer in the storage layer has to be sufficiently thin to avoid multidomain states. Another possibility for reducing exchange variability is the use of synthetic antiferromagnets instead of simple F layers. The reduced dipolar field would stabilize the magnetization state at remanence and reduce the detrimental dipolar coupling with the AF layer, which showed to induce an increase of grain instability during magnetization reversal.**

3.5.2 Impact of the microstructural properties of the antiferromagnetic layer

During Giovanni Vinai PhD's thesis, a second study on patterned systems concerned the effects of microstructural properties of the IrMn layer on exchange bias variability, in a coherent reversal regime. IrMn grain size distribution was varied by considering different thicknesses of buffer layer and IrMn layer. We observed an increase of grain average size and distribution width with increasing buffer and IrMn thicknesses. When patterned, samples showed similar trends to the ones of the full sheet samples and no scalability effects concerning the average exchange bias values.

Regarding exchange variability, on the other side, two main effects were observed:

- **On one side, reducing dot lateral size led to an increase of exchange variability**. This was attributed to IrMn grain cutting at the dot edges, which increases the instability of part of the dots present on the dot.
- Secondly, **variability increased with increasing grain dot size and distribution width**. This was attributed to the fact that on dots with lateral sizes below 200 nm the number of grains per dot is not sufficiently large to cover the whole grain population. Thus, in case of widely distributed grain sizes, the IrMn grain composition may vary a lot from one dot to another one, leading to an increase of exchange bias variability.

For applicative purposes, in order to reduce instabilities and increase dots magnetic properties reproducibility and reliability, multidomain configurations have to be avoided and grain size distribution has to be homogenized in order to reduce the variability of grain population from dot to dot.

3.5.3 Use of orthogonal Pt(Pd)/Co)$_3$/IrMn/Co trilayer structures

We have shown the possibility to improve the exchange bias properties in IrMn/Co structures through an additional out-of plane layer coupled with IrMn at the other interface. This second coupling reduces the critical AF thickness for which the exchange is set and increases the blocking temperature compared to equivalent IrMn/Co bilayers.

To evaluate the impact of the presence of an additional out-of plane layer coupled to the AF layer, we considered trilayer structures with the following stacks: $Ta_3/(Pt_{1.8}/Co_{0.6})_3/IrMn_x/Co_5/Pt_2$ and $Ta_3/(Pd_{1.8}/Co_{0.6})_3/IrMn_x/Co_5/Pt_2$, all thicknesses in nm, for x ranging from 2 to 15 nm.

The evolution of exchange field as a function of IrMn thickness are represented in *Figure 3.14a* for a standard IrMn/Co bilayer, as well as for 2 different trilayers, containing either a $(Pt/Co)_3$ or a $(Pd/Co)_3$ orthogonal multilayers. From this graph, we can remark two main features:

- First, a critical thickness t_C (at which exchange bias appears) appears for both $(Pt/Co)_3$ and $(Pd/Co)_3$ trilayer series, at a lower value compared to the one of the bilayer series.
- Secondly, the peak of exchange t_M is present for lower IrMn thicknesses, reaching higher values of exchange compared to the corresponding maximum exchange of the bilayer series. This increase of the exchange bias field is also associated advantageously with a reduction of the coercive field – see *Figure 3.14b*

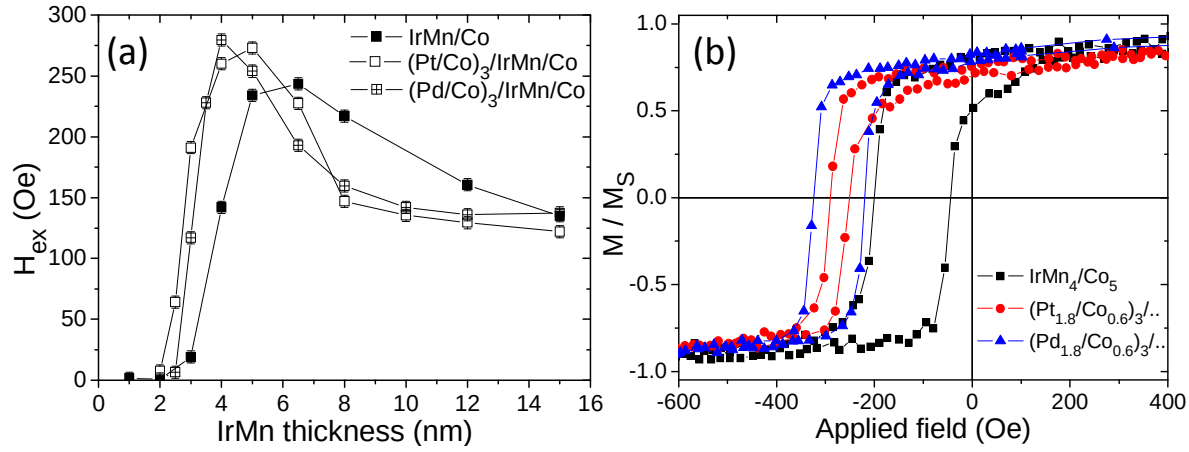


Figure 3.14 (a) Comparison of exchange bias field H_{ex} dependences as a function of IrMn thickness for the three types of structures: IrMn/Co bilayer and (Pt/Co)3/IrMn/Co or (Pt/Co)3/IrMn/Co trilayers; (b) Hysteresis loops at room temperature for the three types structures for 4 nm thick IrMn layer

In the case of thin IrMn layer, the blocking temperature is reached for higher temperatures than the ones obtained of the bilayer case – *see Figure 3.15*. Moreover, the $H_{ex}(T)$ curves for the trilayer systems show a concave (negative curvature) shape compare to the convex, quasi-linear of the bilayer case.

The possibility of increasing the blocking temperature in ultrathin AF layers and of enhancing the exchange bias field is of technological interest for TAS-MRAM applications, in particular for the retention and writing properties of the storage layer. In the range of temperature from 300 to 400 K (interesting from the application point of view), the investigated trilayer structures present, together with larger H_{ex}, a larger H_{ex}/H_C ratio compared to the corresponding bilayer. For example, for 4 nm IrMn thickness at 300 K, H_{ex}/H_C ratio is 1.6 for IrMn/Co bilayer, versus 13.6 and 5.3 for $(Pt/Co)_3$ / IrMn / Co and $(Pd/Co)_3$ / IrMn / Co trilayers. This ratio is an important quality factor for data retention and writing reliability in TAS-MRAM systems: a large exchange bias with low coercivity means a hysteresis loop with both switching field far from zero field, avoiding intermediate state issues during the writing or reading processes. Another important advantage of the trilayer structures compared to the bilayer one is the shape of the $H_{ex}(T)$ variation, concave (negative curvature) instead of convex or almost linear for the bilayer stack. A concave variation is more appropriate for TAS-MRAM application since it means that the memory retention is less degraded on the whole operating range than in the case of a linear variation and that the storage layer pinning energy sharply decreases as the writing temperature is approached. For these reasons, **this kind of trilayer structures is an excellent candidate to improve storage layer performances and reliability in TAS-MRAM.**

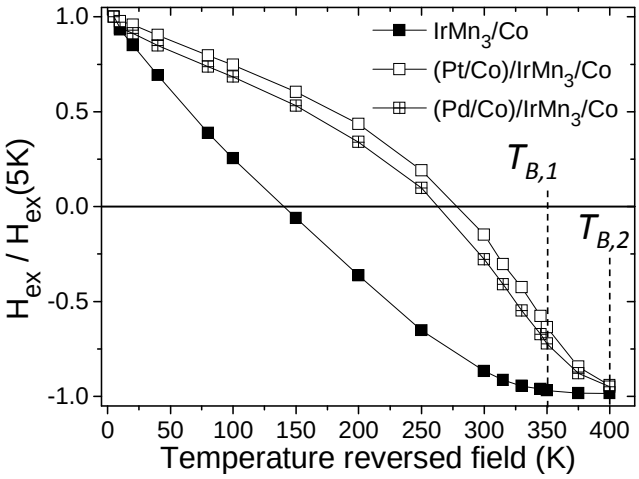


Figure 3.15 – Temperature dependence of normalized exchange bias on Ta through blocking temperature distribution measurement. Vertical dashed lines indicate the maximum blocking temperature for the bilayer (TB,1) and trilayer (TB,2) samples

The introduction of a secondary F layer with out-of-plane magnetization, coupled with the IrMn/Co bilayer, led to a series of improvements of exchange bias properties in a wide range of

temperatures. (Pt/Co) and (Pd/Co) multilayers were selected for the additional F layer (reduction of the IrMn critical thickness, shift toward thinner thickness values of the exchange bias peak, concave curvature and, for IrMn thicknesses below 5 nm, an increase of the blocking temperature). This combination of results was explained through a granular model of exchange bias. The presence of the additional F layer with out-of-plane magnetization is responsible of two effects:

- Firstly, an indirect IrMn grain coupling during the whole hysteresis loop, which creates a uniformed effective grain size more stable in temperature and a more homogeneous blocking temperature distribution.
- Secondly, a canting of the IrMn spins through its thickness because of the propagation of the out-of-plane coupling at the opposite interface of the IrMn/Co one with the (Pt(Pd)/Co)/IrMn one. This canting induces a reduction of the interface coupling, thus stabilizing grains which otherwise would have contributed to the coercivity.

The combination of these two effects leads to thermal effects which are of great interest for implementation on TAS-MRAM systems, specifically on the storage layer, specifically because the benevolent effect of the additional layer is maintained after an annealing process equivalent to those used on MTJ stacks. The concave curvature of the $H_{ex}(T)$ curves guarantee a good reliability on a large T range and the exchange drop close to T_B is ideal for a good writing process, being the whole curvature more suitable than the linear one of the initial bilayer stack. These thermal properties are moreover good for application in TMR heads, giving advantages terms of total stack thickness and stability of pinning at very small dimensions.

3.5.4 Cu dusting layer in (Pt(Pd)/Co)3/IrMn/Co trilayers

A positive impact of an ultrathin Cu dusting layer inserted at the interface between the ferromagnetic and the antiferromagnetic layers on the exchange bias field H_{ex} and on the blocking temperature T_B was already reported. A similar beneficial has been also obtained in the case of the trilayer structure, already showing positive effects given by the additional coupling with the perpendicular multilayer.

The stacks used to evaluate the impact of the Cu dusting insertion layer were (thicknesses in nm): Ta_3 / $(Pt_{1.8}/Co_{0.6})_3$ / $IrMn_4$ / Cu_x / Co_5 / Pt_2 and Ta_3 / $(Pd_{1.8}/Co_{0.6})_3$ / $IrMn_4$ / Cu_x / Co_5 / Pt_2, with x ranging from 0 to 1 nm. The dependence of the exchange bias field on the copper thickness $H_{ex}(t_{Cu})$ obtained from VSM measurements of hysteresis loops at room temperature are shown *in Figure 3.16a*. In the figure, these curves are compared with the corresponding ones obtained for the bilayer stacks. It is striking that the maximum value of exchange bias field obtained for the trilayer stacks with Cu insertion (i.e. for a Cu layer thickness of 0.1 nm), has been increased compared to the value of the IrMn/Co bilayer stack of three times, without changing the thickness of either the F or the AF layers. When a thin Cu interlayer (below 0.3 nm thick Cu, i.e. in the dusting regime) is added at the IrMn/Co interface, the exchange bias increases for all the three stacks: the effect is then confirmed also in the trilayer structure. For thicker Cu spacer, H_{ex} decreases down to vanishing for a 1 nm thick Cu interlayer. Concerning the coercivity dependence (*Figure 3.16b*), trilayer structures present reduced H_C compared to the bilayer case in absence of Cu interlayer. In the Cu dusting and continuous regime, no particular trend in H_C is observed, in contrast to the bilayer case.

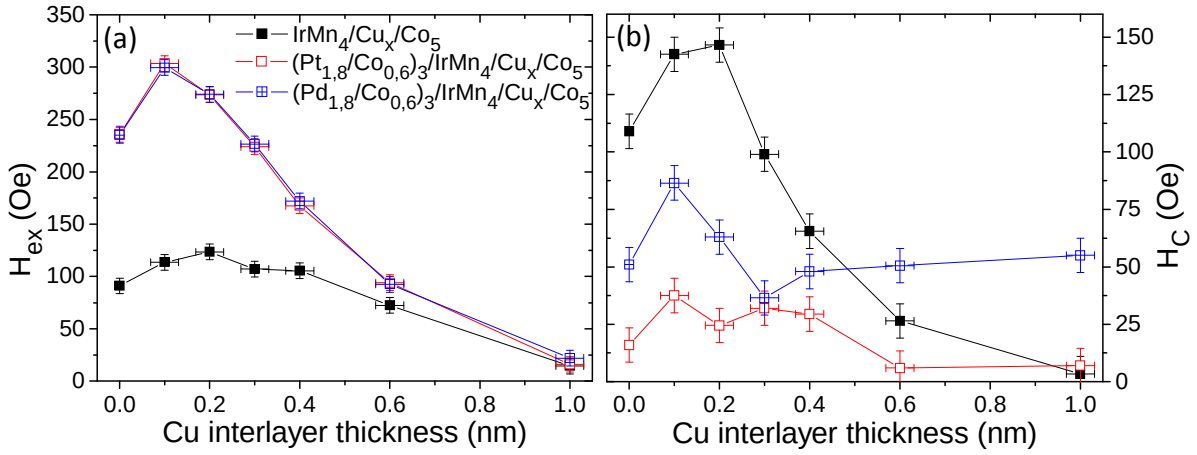


Figure 3.16 – Exchange bias (a) and coercivity (b) evolution as a function of the Cu interlayer thickness

One final important remark is that, in the dusting regime, the $H_{ex}(T)$ curve maintains its concave shape, as in the case with no Cu interlayer – see *Figure 3.17*. This characteristic in temperature is one of the key advantages of the trilayer structures, particularly interesting for technological applications. The fact that the same shape is maintained in presence of the Cu dusting layer make the implemented stack suitable for applications. When comparing trilayer and bilayer structures, the blocking temperature enhancement is confirmed for all Cu interlayer thicknesses. This means that the stabilizing effect of the out-of-plane layer is not affected by the reduced interface coupling due to the presence of the Cu spacer at the IrMn/Co interface.

In conclusion, in presence of a non-continuous interfacial layer, exchange biased samples showed an increase of exchange bias compared to the original configuration. This behaviour has been observed independently on the buffer layer thicknesses and IrMn thicknesses for the IrMn/Co bilayer structure and confirmed also on the trilayer structures $(Pt_{1.8}/Co_{0.6})_3$ / $IrMn_4$ / Cu_x / Co_5 and $(Pd_{1.8}/Co_{0.6})_3$ / $IrMn_4$ / Cu_x / Co_5. This H_{ex} enhancement was confirmed for different buffer layer thicknesses and IrMn thicknesses, which means it is independent on the IrMn microstructural properties, and also for the trilayer structures. **The combination of trilayer stack and Cu dusting layer, for 4 nm IrMn layer, led to 300% enhancement of exchange bias field at room temperature.** Both bilayer and trilayer samples confirmed their behaviour in temperature. This means that a (Pt(Pd)/Co)/IrMn/Cu/Co stack with optimized IrMn and Cu thicknesses is an exchange biased stack with maximised exchange biased value at room temperature and a concave thermal dependence, two characteristics that mark significant improvements from the initial IrMn/Co bilayer, with characteristics that are ideal for implementation on technological applications.

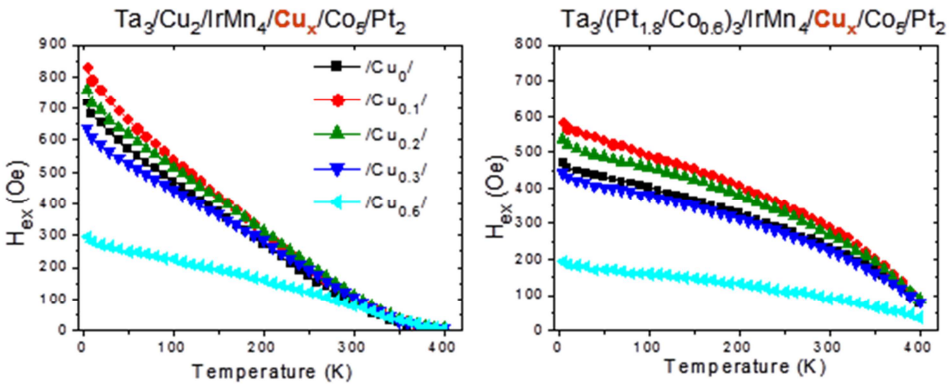


Figure 3.17 (left) Improvement of exchange bias by ultrathin Cu insertion at IrMn/Co interface. Thermal variation of exchange bias in conventional IrMn/Co structure and with Cu insertion (right) Concave variation of Hexb versus T obtained with orthogonal anisotropies.

3.6 PROTECTION AGAINST STRAY FIELDS AND WRITE SELECTIVITY

One of the important advantages of the TAS writing approaches is that the cell used in this approach has a high protection against stray field erasure.

In standby, only one state of the TAS-MRAM storage layer is stable at zero field. This means that even if the TAS-MRAM chip is exposed to a perturbation field, this field may temporary switch the magnetic configuration of the memory but the latter will spontaneously return to its original state before perturbation once the perturbation disappears[41]. This however would not be true during write. If a perturbation field that is a significant fraction of the write field is applied during write, a write error may occur. A read-after-write scheme may be used to verify that no such error has occurred during write.

The memory cell protection against magnetic erasure can be demonstrated by applying a magnetic perturbation field and then measuring the resistance state after the perturbation field is turned off. Without a heating pulse, both P and AP states are stable and insensitive to magnetic field perturbations. This offers a high protection against stray magnetic fields even in absence of any magnetic shielding. Selective writing of the memory cell can only be achieved by applying simultaneously a current pulse and a magnetic field. The memory cell then changes its resistance state each time between two well defined resistance levels corresponding to the P and AP states as illustrated in *Figure 3.18a*. Here, the protection against magnetic erasure of the thermo-magnetic write scheme is demonstrated at room temperature for a 0.45x0.2µm² size junction. The resistances of the P and AP states are shown upon cycling, using a magnetic perturbation field of +/-400Oe. The resistances are measured each time in zero magnetic fields. Without heating pulses, both zero field states are stable and insensitive to magnetic field perturbations. This unique feature of the TAS approach offers a high protection against stray magnetic fields even in absence of any magnetic shielding of the memory.

Selective writing of the memory cell is achieved, applying simultaneously a current pulse and a +/-200Oe magnetic field value. This is demonstrated in *Figure 3.18(b)* for the same junction and applying a 2V/20ns heating pulse. Each time a heating pulse a magnetic field pulse is applied to the junction, the temperature in the storage layer exceeds the Tb of the 60Å IrMn antiferromagnetic layer and the magnetization can be switched. The memory cell is correctly written as the resistance jumps each time between two well defined resistance levels corresponding to the AP or P states. This measurement highlights one important feature of the thermo-magnetic write scheme: excellent selectivity as only heated junctions can be magnetically written.

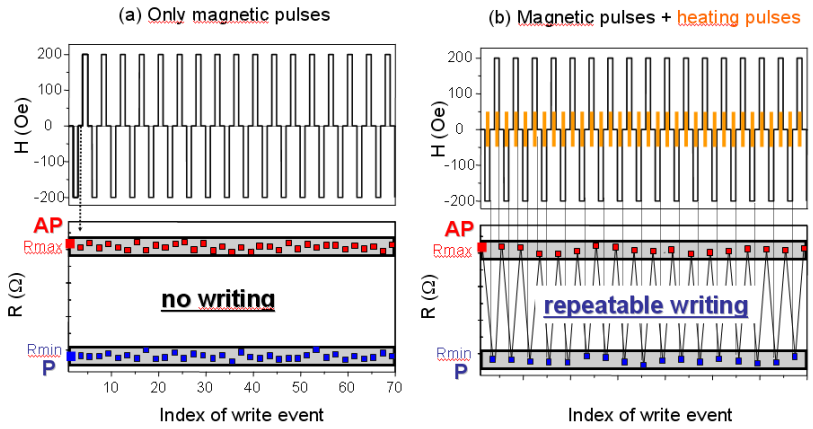


Figure 3.18: Illustration of the write selectivity in TAS-MRAM resulting from the combination of heating pulse and application of a magnetic field. (a) Application of pulses of magnetic field alone-no writing; (b) combination of heating pulse and alternating pulses of magnetic field – repeatable writing of P and AP (0 and 1) magnetic states.

41 I.L. Prejbeanu, M. Kerekes, R.C. Sousa, H. Sibuet, O. Redon, B. Dieny and J.P. Nozieres, *Thermally assisted MRAM*, J. Phys.: Condens. Matter 19 (2007) 165218.

3.7 TEMPERATURE RANGE

If the TAS-MRAM approach offers clear improvements, it nevertheless has its own constraints:

- **the operating temperature range is limited to temperatures compatible with stability of the AF of the storage layer**. If the memory point temperature increases, for example by simply increasing ambient temperature, this decreases H_{ex} which at some point can become smaller than the coercive field H_c. Moreover, if the temperature approaches or exceeds T_b, H_{ex} becomes zero. In this case, two resistance states are possible in zero field and low anisotropy resulting from the circular shape of the pins does not protect information from external magnetic fields or spontaneous reversals of the ferromagnetic layer, thermally activated. In other words, the operating temperature range that was defined in the previous generation MRAM by the superparamagnetic limit of the FM is now defined by the superparamagnetic limit of AF. This limitation defines the boundary between the operating temperature range of TAS-MRAM and write temperature range.
- **the writing method of the TAS-MRAM is based on the possibility to heat the junction to unlock the storage layer, without affecting the stability of the reference layer.** In other words the writing temperature should be higher than the T_b of the AF storage layer while remaining below the T_b of AF reference layer. The functionality of this approach is largely influenced by the choice of materials and their AF blocking temperatures.
- **The AF grain size distribution has important consequences since each grain volume will match a particular T_B.** Antiferromagnets commonly used for the reference layers are metallic and polycrystalline[42]. Their grains are magnetically decoupled and distributed in size about an average size. The idea of a single T_B should be then replaced by a blocking temperature distribution.

This changes dramatically the operating constraints associated with the TAS-MRAM, which are shown schematically in *Figure 3.19* and summarized as follows:

i) To ensure the stability of the storage layer, the operating temperature cannot exceed the minimum T_B of the AF storage layer (here IrMn) - means $T_B - 3\sigma_{T_B}$.

ii) To ensure a reliable writing, AF must be completely unlocked, so the write temperature must be greater than the maximum of the IrMn T_B (mean $T_B + 3\sigma_{T_B}$).

iii) To write without affecting the reference layer, the writing temperature range is limited by the minimum T_B of PtMn.

iv) Finally, the current pulse needed to heat the MTJ must achieve a temperature within the range of writing temperature, from any point of the operating temperature range.

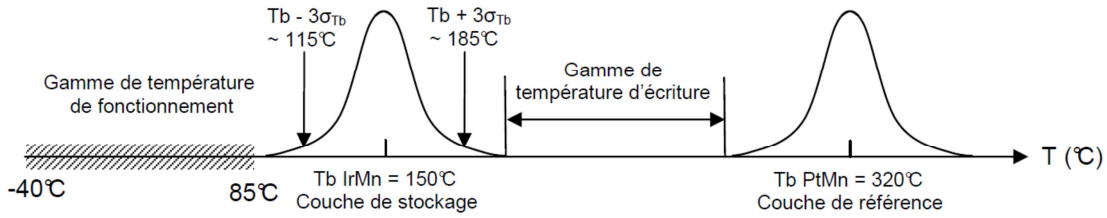


Figure 3.19: Schematic view of the functioning and writing temperatures

These four conditions have to be taken into account to set the operating temperature range of *TAS-MRAM*. From an industrial point of view, the objective of the work is to adapt the *TAS-MRAM* the growing needs of the memory market by allowing their operation temperature ranges more and more extended (*Figure 3.20*), ranging from standard use (between 0 and 70°C) to applications for automotive and aerospace (-55 to 150°C).

42 Nozieres J.P.; Jaren S.; Zhang Y.B.; Zeltser, A.; Pentek K. & Speriosu V.S., *Blocking temperature distribution and long-term stability of spin-valve structures with Mn-based antiferromagnets*, J. Appl. Phys. 87(8), 3920-3925 (2000)

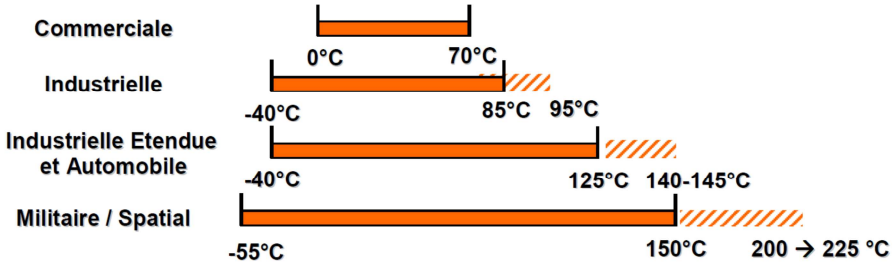


Figure 3.20: Usual functional temperature ranges for electronic devices

Moreover, the initial procedure to determine statically the temperature range by temperature dependent statical VSM measurements was reconsidered after studies showing the dependence of the blocking temperature with the heating pulsewidth. This dependence has been attributed to the role of the thermal activation on the AF grains. Fulcomer and Charap demonstrated both theoretically and experimentally the link between blocking temperature and measurement time and proposed a model of the blocking temperature based superparamagnetism AF[43]. The authors describe the behavior of a ferromagnetic layer on which are deposited AF particles distributed in sizes and shapes, exchange-coupled to the FM layer and decoupled from each other. With increasing temperature, the transition of these AF particles to the superparamagnetic state gradually reduces the exchange coupling to zero. The time dependence of the superparamagnetic limit here implies an increase in the effective blocking temperature with the reduction of heating time. Later studies done by Nishioka based on this model allowed to validate this model, namely by showing the dependence of the exchange coupling both on the lateral size of the grains [44] and on the thickness of the antiferromagnetic layer. Nevertheless all these results were obtained with static measurements of the blocking temperature.

For submicronic TAS-MRAM cells, the heating is confined in extremely small magnetic pillar volume[45]. The very small size and the local nature of the heating system provided a very low thermal inertia with respect to macroscopic heating methods involving an external heating element and thus gives access to heating and cooling of the very short time (up to several ns). It becomes thus possible to explore the exchange coupling properties with very short heating time scales and measuring dynamic T_B. Our results showed an **increase in the blocking temperature with the reduction of heating time**, which is connected to the effects of thermal activation in the AF based on the model of Fulcomer. Thus, it is necessary to take into account two blocking temperature distributions, static and dynamic:

- **The static blocking temperature distribution** gives a measure of the temperature at which the information in a cell can spontaneously disappear over long periods and sets the upper limit of the functional range of temperatures.
- **The dynamic blocking temperature distribution**, obtained by dynamic writing measurements corresponds to the temperature required to break the FM layer and write information in a very short time.

These two distributions are shown in the diagram of the *figure 3.21*. In this scheme we also included a fourth distribution of T_B (orange dashed line), representing the possible shift of the PtMn dynamic T_B to temperatures higher than those accessible by VSM measurements. Thus, **the operating temperature range is different depending on whether one considers the case of writing (dynamic) or in standby mode (static).**

43 Fulcomer, E. & Charap, S. H., *Thermal fluctuation aftereffect model for some systems with ferromagnetic-antiferromagnetic coupling*, J. Appl. Phys. 43(10), 4190-4199. (1972) Fulcomer, E. & Charap, S. H., *Temperature and frequency dependence of exchange anisotropy effects in oxidized NiFe films*, J. Appl. Phys. 43(10), 4184- 4190. (1972)

44 Nishioka, K.; Hou, C.; Fujiwara, H. & Metzger, R. D. (1996), 'Grain size effect on ferro-antiferromagnetic coupling of NiFe/FeMn systems', J. Appl. Phys. 80(8), 4528-4533.

45 Papusoi, C., Sousa, R., Herault, J., Prejbeanu, I.L., Dieny, B., Probing fast heating in magnetic tunnel junction structures with exchange bias, New J. Phys. 10, 103006, 2008

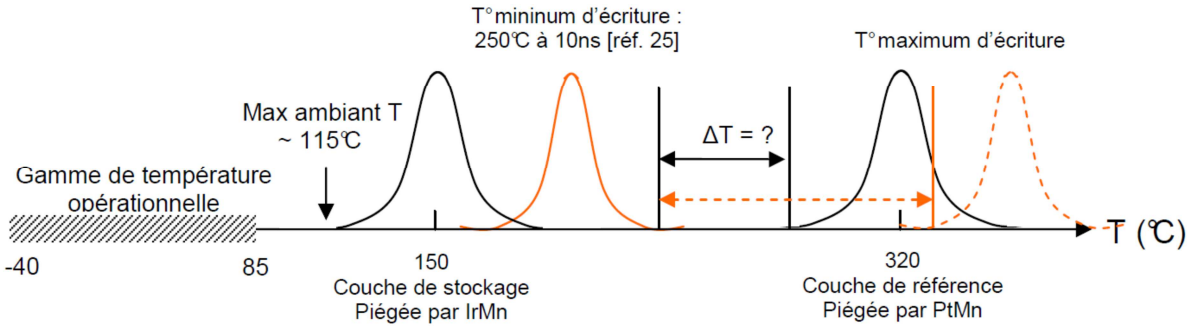


Figure 3.21: Schematic view of the functioning temperature ranges (statical measurements, black curves) and of the writing temperature ranges (dynamic measurements, orange curves)

3.8 INDUSTRIALIZATION OF THE TAS-MRAM TECHNOLOGY

Crocus Technology in collaboration with TowerJazz has produced functional 1 and 4 Mbit demonstrators using this technology in 130nm technology (*Figure 3.22*). These demonstrators are addressing shortcomings of Battery-backed SRAM solutions, have been in use for years for protecting data from power interruption. There are several drawbacks associated with these solutions; including large size, high cost, and battery reliability. TAS-MRAM based memory solutions proposed by Crocus and TowerJazz include non-volatile reliable performance, TAS programming, high data retention, high endurance, low power, and high-temperature operation. In addition, Crocus' memory products eliminate the need for battery, thus offering a cost effective green solution.

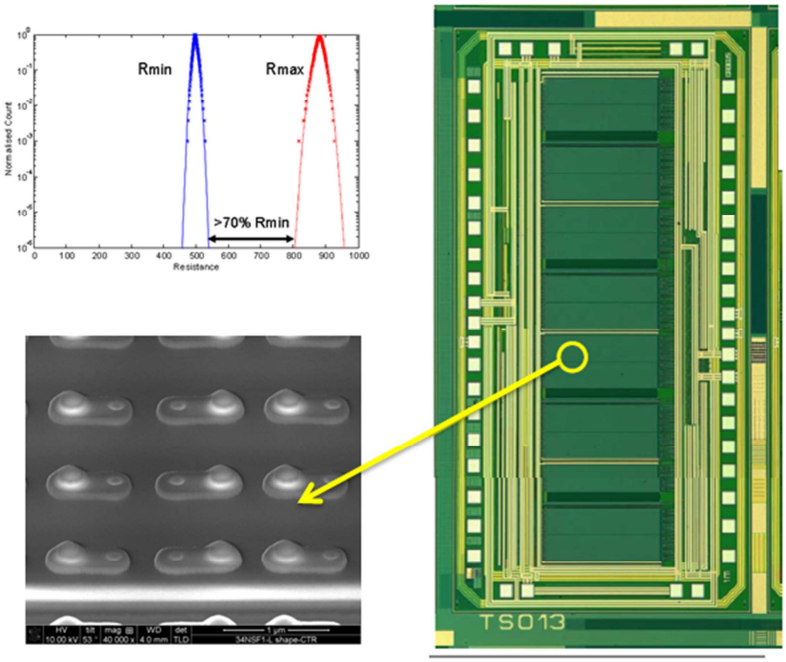
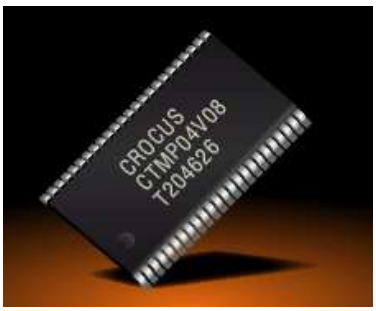


Fig. 3.22: 1 Mbit chip from Crocus Technology/Towerjazz. Zoom on the patterned MTJs connected to the via emerging from the CMOS wafer. Note the circular shape of the in-plane magnetized MTJ specific to TAS operation which allows reduced write field.

The CTMP memory (shown in *Figure 3.23*) is a low power solution for data logging, program store, data buffering and data cache applications. The Crocus Technology CTMP memory offers SRAM compatible 35ns read and 35/90/120/150 ns write cycle timing with large endurance. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltages out of specification. The CTMP memory is available in various packages: 44-pin TSOP II and 48-pin

TFBGA, compatible with similar low- power SRAM products and other non-volatile RAM products. The products are offered for commercial temperature (0 to +70°C) operation.



1. Key Features

General

- Non-Volatile Data Storage
- Automatic Data Protection on Power Loss
- Fast 35ns Read Cycle Time
- 35/90/120/150 ns Write Cycle Time
- SRAM Compatible Timing and Pinout
- Unlimited Read & Write Endurance
- Data Retention for >20 Years at Operating Temperature
- 3.3 Volt ± 10% Operation
- Commercial and Industrial Temperature Operating Range
- Small Footprint TSOP-II and TFBGA Packages(RoHS Compliant)
- Socket compatible with 128Kx8 nvSRAM and MRAM products

Benefits

- One Memory Replaces Flash, SRAM, EEPROM and BBSRAM in System for Simpler, More Efficient Design
- Uses Existing SRAM Controllers Without Redesign
- Replace Battery-Backed SRAM Solutions with MRAM to Eliminate Battery Assembly and Maintenance Costs and Improves Reliability

2. Product Brief Description

Introduction

The Crocus Technology CTMP04V08 is a 4Mbit Magnetic Random Access Memory (MRAM) device organized as 524,288 words by 8 bits. The CTMP04V08 offers SRAM compatible 35ns read and 35/90/120/150 ns write cycle timing with unlimited endurance. Data is always nonvolatile, with data retention greater than 20-years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltages out of specification.

The CTMP04V08 is the ideal low power solution for data logging, program store, data buffering and data cache applications.

The CTMP04V08 is available in the following packages: 44- pin TSOP II, and 48-pin TFBGA. These packages are compatible with similar low- power SRAM products and other non-volatile RAM products.

Crocus Technology memory devices provide highly reliable data storage over a wide range of operating temperatures. The product is offered for commercial temperature (0 to +70°C) operation. Please consult the factory for industrial temperature operation.

Fig. 3.23: Top: Picture of the 4 Mbit chip from Crocus Technology/Towerjazz. Bottom: Key features and product brief description of the 4Mbit chip (from Crocus Technology website: www.crocus-technology.com).

3.9 CONCLUSION ON TAS-MRAM

In conclusion, I have shown in this chapter that in order to improve the thermal stability, the write selectivity and the power consumption for MRAM applications, SPINTEC pioneered proposed a new concept the thermally assisted writing, called *TAS-MRAM*. A current flow through the junction is used to heat the cell above a threshold temperature enabling the storage of information. The TAS approach has multiple advantages and solves the limitations of the conventional MRAM architecture:

(i) As the selection at write is temperature-driven, the addressing errors are strongly reduced.

(ii) Only one magnetic field is required to write, leading to reduced power consumption Furthermore, the write power can be further reduced, by using circular elements with no shape anisotropy.

(iii) The exchange bias anisotropy of the storage layer ensures a good thermal stability of the information.

(iv) Since the system is not anymore bistable at zero field due to the exchange bias, TAS provides good reliability under field disturbance. Indeed, even if the resistance state of a bit is modified by external parasitic fields under standby conditions, the resistance state after the field perturbation goes back to its initial state.

(v) TAS-MRAM presents a good scalability since the heating power density P required to heat the junction is proportional to the square of the current density

The principle behind the heat generation in a MTJ structure is a combination of the Joule heating in the metallic electrodes and of the inelastic scattering of tunneling hot electrons arriving in the receiving electrode after their ballistic tunneling across the tunnel barrier. The direction of the tunneling current in magnetic tunnel junctions can have a significant influence in the final temperature profile within the MTJ as there is an asymmetry in the heating depending on the polarity of the write pulses (flow direction).

In *TAS-MRAM*, the total duration of the write cycle is determined by the heating and cooling dynamics and the speed at which cells can be re-written after an initial write. We have shown that the heating and cooling times can be indeed competitive, for a total write cycle time on the order of 30 ns

One way to increase the heating efficiency and reduce the power density is to insert low thermal conductivity materials at both ends of the magnetic tunnel junction stack. Another possibility to reduce the write power density is the use of AF materials with lower Néel temperature.

Field writing combined with thermal assistance is also advantageous in terms of power consumption in MRAM chips by offering the possibility to share the pulse of magnetic field among numerous bits.

The variation of the thickness of the ferromagnetic storage layer led, because of the competition between dipolar and exchange energies, to the observation of two different mechanisms of magnetization reversal. For this reason, the F layer in the storage layer has to be sufficiently thin to avoid multidomain states. Another possibility for reducing exchange variability is the use of synthetic antiferromagnets instead of simple F layers. The reduced dipolar field would stabilize the magnetization state at remanence and reduce the detrimental dipolar coupling with the AF layer, which showed to induce an increase of grain instability during magnetization reversal.

For applicative purposes, in order to reduce instabilities and increase dots magnetic properties reproducibility and reliability, grain size distribution has to be homogenized in order to reduce the variability of grain population from dot to dot.

The possibility of increasing the blocking temperature in ultrathin AF layers and of enhancing the exchange bias field is of technological interest for TAS-MRAM applications, in particular for the retention and writing properties of the storage layer. This kind of trilayer structures is an excellent candidate to improve storage layer performances and reliability in TAS-MRAM. The combination of trilayer stack and Cu dusting layer, for 4 nm IrMn layer, led to 300% enhancement of exchange bias field at room temperature.

If the TAS-MRAM approach offers clear improvements, it nevertheless has its own constraints:

i) the operating temperature range is limited to temperatures compatible with stability of the AF of the storage layer.
ii) the writing method of the TAS-MRAM is based on the possibility to heat the junction to unlock the storage layer, without affecting the stability of the reference layer. The functionality of this approach is largely influenced by the choice of materials and their AF blocking temperatures.
iii) The AF grain size distribution has important consequences since each grain volume will match a particular T_B. The idea of a single T_B should be then replaced by a blocking temperature distribution.
iv) Moreover, the initial procedure to determine statically the temperature range by temperature dependent statical VSM measurements was reconsidered after studies showing the dependence of the blocking temperature with the heating pulsewidth.

The thermally assisted approach offers a promising solution for the next generation of MRAM as it can solve most of the current issues: write selectivity, power consumption and thermal stability, whilst offering scalability to 65 nm node. Crocus Technology in collaboration with TowerJazz has produced functional 1 and 4 Mbit demonstrators using this technology in 130nm technology. These demonstrators are addressing namely shortcomings of Battery-backed SRAM solutions,

4. SELF REFERENCED TAS MRAM

SELF REFERENCED TAS MRAM concept

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8. Dieny, B. and **Prejbeanu, I.L.**, *MRAM basics*, To be published, Springer Verlag (2015)

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19. A. Annunziata, **I.L. Prejbeanu**, *Self-reference thermally assisted MRAM with improved write efficiency utilizing multilayer thermal barriers*, Provisional I78-0487US
20. A. Annunziata**, I.L. Prejbeanu**, *Multibit self-reference thermally assisted MRAM*, Provisional I78-0486US

PhD THESIS

1. Quentin Stainer (co-supervising 25%) - R&D engineer Crocus Technology

Development of self-referenced thermally assisted magnetic random access memory cells (MRAM)
Université Joseph-Fourier, Grenoble, defended December 19, 2014, Directeur de these: Bernard Dieny

2. Myckael Mouchel (co-supervising 50%) – PhD ongoing

Noise in MLU magnetic sensors
Université Joseph-Fourier, Grenoble, to be defended 2017, Directeur de these: Claire Baraduc

In MRAM chips, dot-to-dot variability remains a key problem. **One possible solution to solve this problem is the so called self-referenced read scheme, which is able to assess the magnetic state of an addressed cell without comparison with an external reference cell. This is achieved in self-referenced *SR-TAS-MRAM*, a second possible implementation of *TAS-MRAM*.** Besides its classical memory type applications, this self-referenced cell can be used to perform logic operations with particularly interesting applications in security. Indeed, these devices combine memory and logic functions. For this reason, self-referenced TAS-MRAMs were also called Magnetic Logic Units (MLU™)[46].

This chapter will also deal with the optimization of self-referenced *SR-TAS-MRAM* for high density storage. Two routes for achieving this will be explored:

- In the first one we will focus on the reduction of the patterning dimensions of the MTJ, while maintaining manageable power-consumption and data retention properties, with the experimental demonstration of the feasibility of its functionalities.
- We will then investigate new data encoding methods for multibit operations, from the simulation of their performances to their experimental demonstration.

4.1 WORKING PRINCIPLE

In MLUs, the reference layer (now called sense layer) is made of a soft unpinned magnetic material replacing the standard exchange biased reference layer pinned by a high Néel temperature antiferromagnet used in conventional *TAS-MRAM* architecture - *see Figure 4.1*. **This concept has been extensively studied during the PhD thesis of Quentin Stainer.**

The storage layer is exchange biased by an adjacent antiferromagnetic layer, identical to standard TAS-MRAM. **The writing of the storage layer is achieved similarly to thermally assisted MRAM cells** by the application of a combination of an external field and a heating pulse that allows the storage layer to be switched and then pinned in the opposite direction as the system cools back below its antiferromagnetic blocking temperature.

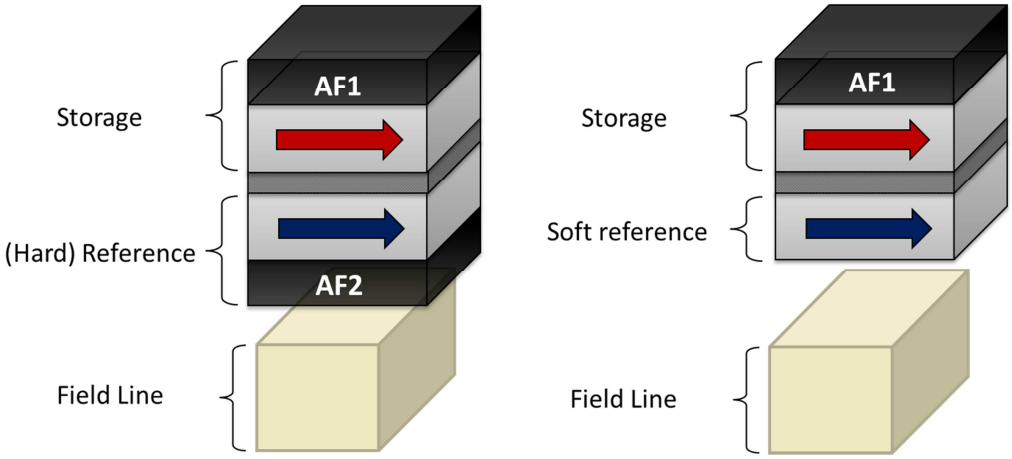


Figure 4.1: Schematic representation of a classical TAS-MRAM stack win comparison to a self-referenced TAS-MRAM stack. The main difference is the suppression in the SR-TAS-MRAM stack of the antiferromagnetic layer AF2 exchange biasing the reference layer

The reading scheme is different with respect to the classical TAS-MRAM and consists in switching the free layer in a first predetermined direction (along the stable directions of

46 http://www.crocus-technology.com/pdf/Crocus_MIP_White Paper_v6.pdf

storage layer magnetization) and then in the opposite direction[47]. This reading can be performed in a two-step quasi-static way or dynamically with an oscillation of the sense layer magnetization away from a 90° orientation, with the storage layer magnetization yielding an upward or downwards oscillation of the MTJ resistance. The quasi-static read is performed in two steps – *see Figure 4.2*:

1. **The soft reference layer is first set in a predetermined initial direction by application of a first pulse of magnetic field** (without heating pulse so as not to write the storage layer). **Then the resistance of the MRAM cell is measured**.
2. **The soft reference magnetization is then switched to the opposite direction and the new resistance is measured**.

The change of resistance associated with these two states, either increasing or decreasing, is used to infer the storage layer magnetization direction. **The resistance variation between the two measurements yields the magnetic orientation of the storage layer**. If the second resistance value is higher than the first one, this implies that the first state was the parallel magnetic configuration so that the storage layer was pointing in the first predetermined direction. On the contrary, if the second resistance is lower than the first one, this means that the magnetization of the storage layer is pointing antiparallel to the first predetermined direction of application of the field.

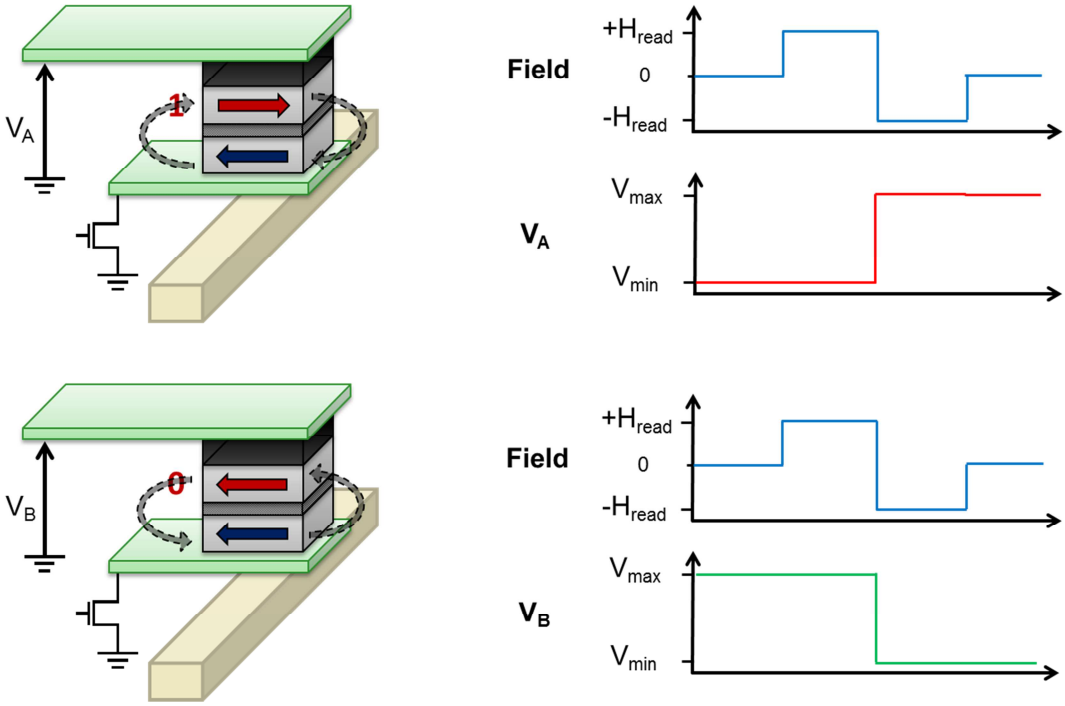


Figure 4.2: Schematic representation of the reading process in a self-referenced TAS-MRAM

The advantage, of this implementation is that the tolerance to process variation is greatly enhanced and the constraints on homogeneity of cell to cell resistance and magnetoresistance amplitude are much released – *see Figure 4.3*.

Indeed, for the standard reading scheme, the two resistance state distributions have to be well separated in order to avoid reading errors. This implies good dot size and shape control. Thanks to this self-referenced readout scheme, a major advantage of these devices is that they are much more tolerant of process variation and cell-to-cell variation. Since each cell is self-referenced, constrains on homogeneity of cell-to-cell resistance and magnetoresistance amplitude are much released. This is

47 N.Berger, and J. P. Nozières, *"Self-Referenced Magnetic Random Access Memory Cell"*, U.S. Patent 20110007561, issued January 13, 2011

particularly useful for small technological nodes where it becomes increasingly difficult to control accurately the resistance distributions.

Furthermore, **the high blocking temperature antiferromagnetic material employed in usual MRAM reference layers (i.e. PtMn) is no longer required in SR-MRAM stacks leading to a large increase of the operating temperature range.** Indeed, in TAS-MRAM using two antiferromagnets pinning layers of different blocking temperatures, the programming temperature range therefore having two boundaries. Thanks to the use of only one antiferromagnet, one of these boundaries is removed and the programming range can extend to much higher temperature since there is no more risk to unpin the reference layer during write. Antiferromagnets with higher blocking temperature may also be used to pin the storage layer magnetization for high temperature applications.

SR-TAS-MRAM **cells, aside from their storage functionality, have also been identified as technological solutions for high-temperature, multi-dimensional field sensing applications – see paragraph 4.5[48], as well as power amplification[49].**

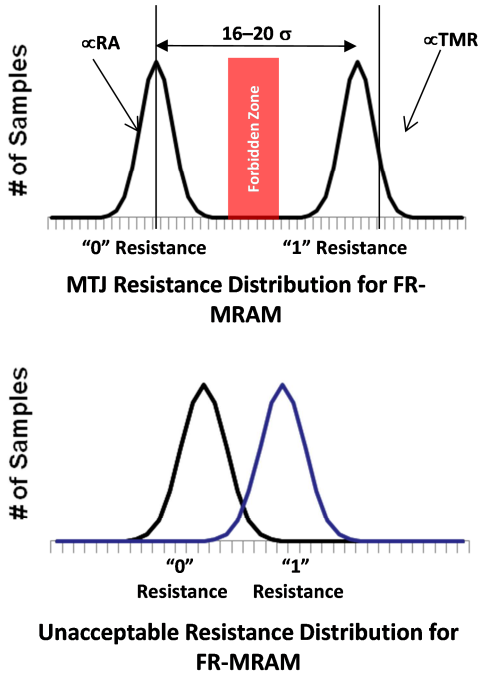


Figure 4.3 Enhanced tolerance to process variation of the SR-TAS-MRAM

4.2 DIRECT VS DIPOLAR WRITING

Although the writing sequence of a self-referenced *SR-TAS-MRAM* is identical to that of a regular TAS-MRAM (simultaneous application of a heating pulse and of a small magnetic field), the details of the magnetization switching behaviors differs significantly. **In particular, I will show that in self-referenced *SR-TAS-MRAM*, the sense layer can also be used as a magnetic lever to switch the storage layer magnetization at low fields thanks to the magnetostatic coupling between these two layers in the so called dipolar writing mode.**

As mentioned in the previous paragraph, self-referenced *SR-TAS-MRAM* stacks are obtained by replacing the pinned reference layer, representative for classical TAS-MRAM memory cells stacks, with a ferromagnetic soft free layer, henceforth referred to as the sense layer. Self-referenced *SR-TAS-MRAM* stacks also comprise an exchange biased synthetic antiferromagnet (SAF) storage layer allowing to minimize magnetostatic interactions with the sense layer, namely to reduce the offset field detrimental for the read power consumption. One of the main issues in MRAM technology is that magnetostatic couplings between ferromagnetic layers increases as the MTJ dimensions are reduced. These couplings can be responsible for an increase in field requirements and are therefore a major constraint when it comes to downward scalability, i.e. a simultaneous reduction of energy consumption and patterning dimensions.

2 strategies can be followed to minimize magnetostatic interactions:

48 B. F. Cambou, D. J. Lee, K. Mackay, and B. Hoberman. *Magnetic Logic Units Configured to Measure Magnetic Field Direction*, US Patent App. 13/787,585. September 19 2013.

49 I. L. Prejbeanu, B. Dieny, K. Mackay, and B. Cambou. *Magnetic Logic Unit (MLU) Cell and Amplifier Having a Linear Magnetic Signal*, EP Patent App. EP20,120,290,316. March 26 2014.

1. Low saturation magnetization layers both for the storage and sense layers - we refer to this configuration of magnetic layers as an F-F device.
2. using a storage layer composed of a synthetic antiferromagnet (SAF) with two ferromagnetic layers anti-coupled using RKKY exchange - we refer to this other configuration as a SAF-F device.

While the SAF-F device has better scaling properties, the F-F device is a simpler and more robust starting point for good bit yield when integrated with the high process temperatures (400 °C) used in standard back end of line (BEOL) complementary metal oxide silicon (CMOS) manufacturing. F-F devices has been mainly studied in the framework of the Crocus – IBM MRAM alliance.[50] The magnetic materials stack developed for the F-F devices satisfies the dual requirements of high temperature operation (>85 °C) and high temperature process (400 °C) compatibility.

I will present here only results obtained for the SAF-F devices. Two types of stacks have been studied in order to evaluate the writing procedure in *SR-TAS-MRAM*, They are schematically represented in *Figure 4.4*.

A first type of stack corresponds to the so called “direct” writing mode. A typical magnetic stack CoFeB 1.2 / MgO 1.4 / CoFeB 3 / Ru 0.9 / CoFe 1 / NiFe 1.5 / FeMn 9 (thicknesses indicated in nm) has 2 particularities:

- **First, the sense layer was designed to be the thinnest achievable, in order to minimize magnetostatic interactions with the storage layer, while maintaining both a sufficient TMR ratio and an in-plane magnetization** (for very thin layers there is a transition from in plane to out plane magnetized layers).
- **Second, a SyF (synthetic ferromagnetic) storage layer was employed instead of a single ferromagnetic layer in order to significantly reduce its magnetostatic coupling with the sense layer.** For this SyF storage layer, a trade-off appears between the compensation of the magnetic moment, which leads to a reduction of the magnetostatic interactions with the sense layer, thus decreasing the read field requirements, but simultaneously increases the switching field of the storage layer, therefore increasing the write field requirements.

These “direct write” *SR-TAS-MRAM MTJ* stacks were patterned to circular memory cells of various diameters, ranging from 70nm to 1200nm. The nominal, full-sheet TMR and resistance per area product (RA) values obtained by current in plane tunneling (*CIPT*) measurements, are respectively 157% and 30Ωμm². During read, a measurable resistance variation was therefore obtained by using the self-referenced read method described here above for applied fields of 100Oe. For write, we have demonstrated the possibility to unpin the exchange biased storage layer similarly to the write operation in TAS-MRAM but the write field was found to be significantly higher (about 150Oe) than the target requirement of 100Oe. Moreover, the writing fields are increasing when the cell diameter is reduced.

Thereby, while proving the feasibility of *SR-TAS-MRAM* in both read and write mode, the stack designed in this “direct write” SR-TAS-MRAM proved to be not scalable and thus unsuitable for manufacturing. An optimization of the magnetic stack is therefore mandatory.

[50] A. J. Annunziata, P. L. Trouilloud, S. Bandiera, S. L. Brown, E. Gapihan, E. J. O’Sullivan and D.C. Worledge, *Materials investigation for thermally-assisted magnetic random access memory robust against 400 °C temperatures*, J. Appl. Phys. 117, 17B739 (2015)

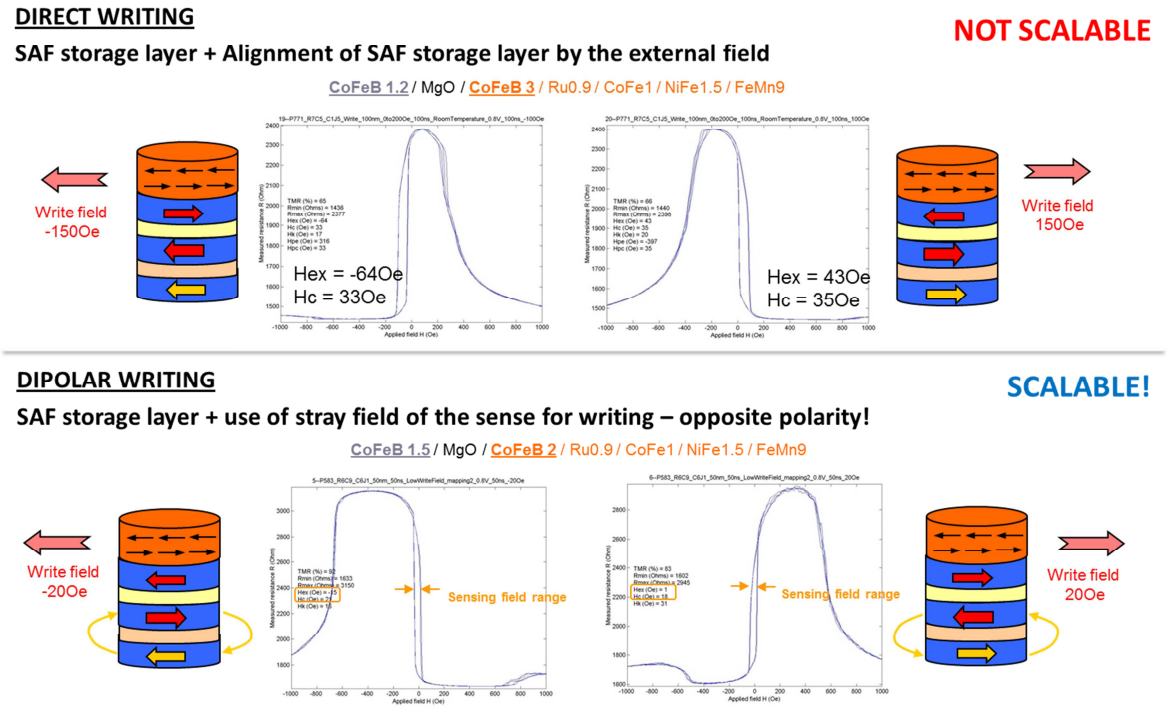


Figure 4.4 (top) Direct write mechanism for a circular dot of 120nm diameter: a 150Oe external magnetic field is required to write the memory cell in the 2 opposite directions (bottom) dipolar write mechanism for a circular dot of 120nm diameter: a 20Oe external magnetic field is required to write the memory cell in the 2 opposite directions

In order to reduce the switching fields and to improve the scalability of the ST-TAS-MRAM; a new write mode was implemented, so called "dipolar" writing mode.

- **In this "dipolar" writing concept, a thicker soft sense layer is advantageously used to locally amplify the field acting on the storage layer.** During write, the soft sense layer gets magnetized by the applied field and its stray field (much larger than the applied field) orients the storage layer magnetization in the direction antiparallel to that of the sense layer magnetization i.e. antiparallel to the applied field.
- **Moreover the synthetic ferrimagnetic storage layer is closer to compensation than in the case of a "direct" write stack, which is advantageous for the read field as the offset field of the sense layer is strongly reduced.**

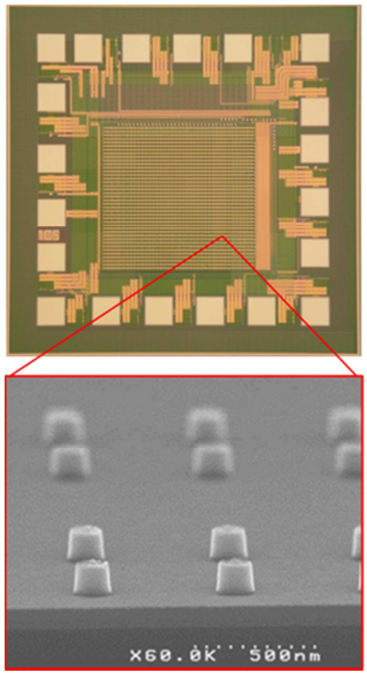


Figure 4.5 Top view of a 1kbit SR-TAS-MRAM prototype; bottom view: SEM picture of the circular pillars.

A typical *SR-TAS-MRAM* magnetic stack designed for the "dipolar" writing was CoFeB 3 / MgO 1.4 / CoFeB 2 / Ru 0.9 / CoFe 1 / NiFe 1.5 / FeMn 9 (thicknesses in nm). The MTJ were patterned on a 200 mm wafer to circles of various diameters, ranging from 70 nm to 1200 nm. The nominal, full-sheet TMR and resistance area product (RA) values were obtained by *MR-CIPT* measurements, being respectively equal to 155% and 29Ωμm². As illustrated in *figure 4.4* bottom, a sensible improvement in the read mode response has been obtained with respect to the direct write

results. **The offset field of the sense layer is also reduced from 50 to about 10Oe, which has a direct impact on the reduction of the reading field.** Moreover, the sense layer transition happens at a much lower field amplitude, namely 20Oe, while the storage layer spin-flop occurs at 600 Oe (compared to 200Oe in *figure 4.4 top*), thus **significantly extending the maximum resistance plateau, and thereby the read field margin.**

After demonstration of the proof of concept of the dipolar writing mode on SR-TAS-MRAM on individual cells, we have validated its manufacturability (the statistical reproducibility of the read and write operation on a larger number of memory cells) on 1kbit prototypes, for dots with 110nm nominal diameters – see *Figure 4.5*. In these devices, the magnetic writing fields are generated locally by flowing current in metallic field lines patterned below the MTJ.

The successful implementation of this concept on 1 kbits array is illustrated in *Figure 4.6*. Write field as low as 4mT are large enough to reach 100% writing probability. The dipolar writing regime occurs at low field values reducing the field required for switching in equivalent size cells having a standard reference layer. At higher fields, larger than the stray field from the sense layer, direct field writing is observed. The switching regimes have been confirmed both in numerical macrospin simulations, as shown in *Figure 4.5.a*. It is interesting to point out that the state diagram using easy-hard axis orthogonal fields illustrates the same critical regions as those observed for Toggle MRAM switching, which is understandable as both architectures share a similar underlying synthetic ferrimagnet switching mechanism. **We thereby confirmed the existence of a magnetostatically activated switching mechanism with significantly reduced writing / reading field requirements and opposed polarity with respect to the typical direct writing of the storage layer.**

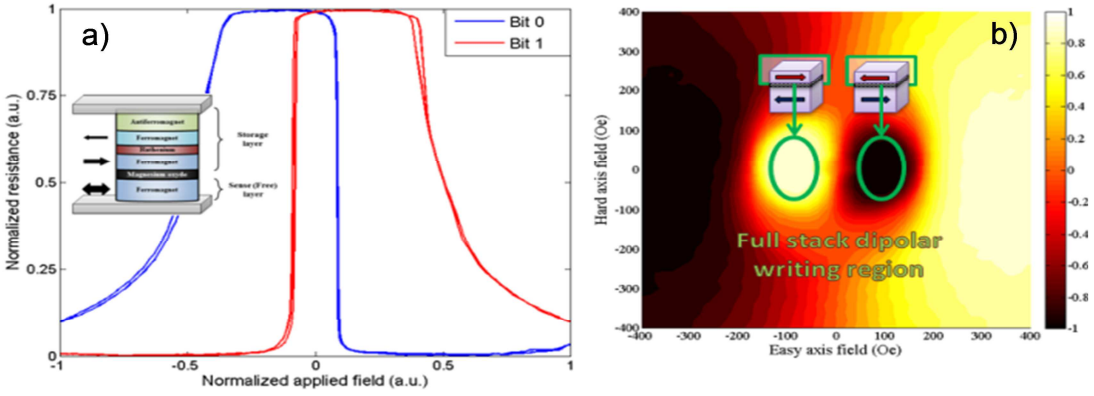


Figure 4.6 a) Self-reference layer stack and macrospin simulated sense layer loops for the 2 stored bits '1' and '0'. b) state diagram showing the low field dipolar writing regions of a 1kbit array of self-referenced MRAM cells as function of easy and hard axis field.

4.3 MULTI-BIT STORAGE

A convenient way to increase the storage density in MRAM chip is to increase the number of bits per cell instead of decreasing the cell size, which is more and more challenging from a technology point of view. While TAS-MRAM devices with multibit storage capacities have been developed[51], the presence of a free sensing layer in SR-MRAM magnetic stacks allow designing new storage paradigm.

In SR-TAS-MRAM, since the storage layer is exchange biased, its magnetization can be stabilized in any direction in the plane provided the field can be applied also in any in-plane direction. By using two orthogonal field lines and by varying the direction of the in plane

51 T. Shoto and W. Shigeyoshi. Design Method of Stacked Type Thermally Assisted MRAM with NAND Structured Cell. Contemporary Engineering Sciences, 6(4):143– 161, 2013.

applied field, multiple bits per dot could be thus stabilized. The readout is performed by rotating the magnetization of the sense layer and detecting the phase at which the resistance is minimum.

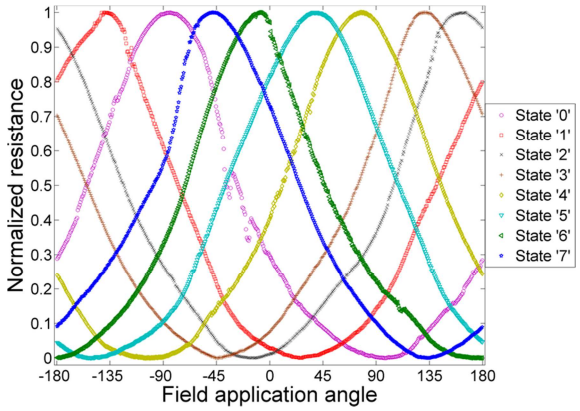


Figure 4.7: Normalized resistance as a function of the field angle (applied field = 600Oe) measured on a 110 nm wide self-referenced MRAM cell written in 8 directions, demonstrating a 3 bits per cell device feasibility

The feasibility of 3-bits per cell storage in *SR-TAS-MRAMs* was demonstrated both by macrospin simulation and experiments. The memory cell consists of a CoFe based storage layer, exchange biased with an IrMn antiferromagnetic layer and a CoFeB based sense layer. Write is performed by heating the antiferromagnet above its blocking temperature by means of a voltage pulse, with simultaneous application of an in-plane field establishing a new pinning direction. Read is then performed by applying a rotating field, inducing a coherent rotation of the CoFeB free layer, and subsequently locating the field angle associated with the minimum measured magnetoresistance. This angle corresponds to a parallel alignment of both ferromagnetic layers' magnetizations and therefore to the pinning direction established during the write operation, which is therefore carrying the information. This mechanism allows multi-bit per cell storage.

Instead of reading a resistance level, as in TAS-MRAM, or a change in resistance, as in regular self-referenced MRAM, multi-bit Self-Referenced TAS-MRAMs exploit the full resistance response obtained as the sense layer align itself with the external rotating field. During this field rotation, the resistance continuously varies as a function of the field angle, reaching a maximum (respectively minimum) value when the sense and storage layers moments become antiparallel (respectively parallel). Thus, the data, i.e. the storage layer magnetization direction can be read out from the phase of this oscillatory resistance, for instance by an external digital signal processor.

Therefore, to achieve **n**-bits per cell storage, the storage layer must be writable in at least $\mathbf{2^n}$ distinct directions. Unlike resistance-level-based multi-bit operations in MRAM, this operation does not rely on a series of predefined resistance levels. It is therefore more tolerant to process related cell to cell variability such as size or resistance per area variations, though at the expense of a more complex readout mechanism. The normalized responses during the read operation for the 110nm MTJ are plotted in *Figure 4.7* and confirm the feasibility of 3 bits functionality at that dimensions.

4.4. LOGIC FUNCTIONALITIES

***SR-TAS-MRAM*, in addition from being a storage type of device, with all described advantages in terms of tolerance to process variability and extended operating temperature range, can also address other types of applications namely due to the possibility to switch individually both sense and storage layers in the MTJ stack, rather than only the storage layer in regular MRAM architectures.** Self-referenced MRAM intrinsically allows performing logic comparison functions with particularly interesting applications in security, namely Match-in-Place Engines or Content Addressable Memories (CAM).

Magnetic Logic Unit (MLU) cells designed on the Self-referenced *SR-TAS-MRAM* technology behave as a 3 terminal device capable of performing native logical functions such as an "XOR" at the magnetic level without any transistor level CMOS logic embedded in the arrays. Considering the storage and the sense layer magnetizations as two inputs, during logic operations the field lines are

acting as control gates modulating the resistance of magnetic stacks – see *Figure 4.8*. This magnetic stack outputs the exclusive OR function of these logic inputs through the magnetoresistance level. Both inputs are set using pulses of magnetic field, with first the storage layer being written with a heating pulse and then the sense layer switched at room temperature.

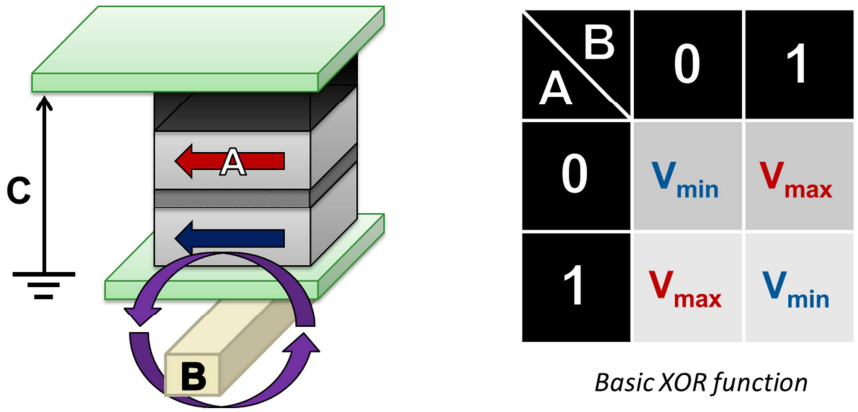


Figure 4.8: Logic gate based on a SR-TAS-MRAM cell. The logic entries are A – the orientation of the magnetization in the storage layer and B – the magnetic field in the field line. A Basic XOR function can be easily built using these logic gates

MLU cells can be used to design:

- NOR - MRAM. *Each self-referenced cell has a select transistor to read the stored bit*.
- NAND – MRAM. *Multiple cells are connected in series.*
- Match-In-Place. *The field lines drive the input patterns.*
- Table look up. *The field lines drive multiple NAND chains in parallel.*
- Various logic functions. *The field lines are acting as control gates.*

Fields of use of these new architectures include secure microcontrollers, subscriber identity module (SIM) cards, banking cards, biometric authentication chips, near-field communication and hardware acceleration. Expected benefits are enhanced security, lower cost, and faster response time.

4.4.1 Match in Place (MiP)

Match-In-Place™ engine can be created by using a set of self-referenced SR-TAS-MRAM cells connected in series to form a NAND chain, as illustrated in *Figure 4.9*. **A pattern applied to the sense layers is compared to the written pattern stored in the storage layers**[52]. The storage layers magnetizations directions correspond to a stored word, for instance a security key. In idle mode, and due to magnetostatic interactions between sense and storage layers, all the cells lie in antiparallel configurations. A reference measurement is performed as the resistance of the NAND chain will always be maximum. Current is then applied in the field lines so that the sense layers magnetization directions are switched according to an input word to compare to the stored word.

52 Cambou B, Match-In-Place™. A Novel Way to Perform Secure and Fast User's Authentication, www.crocus-technology.com website

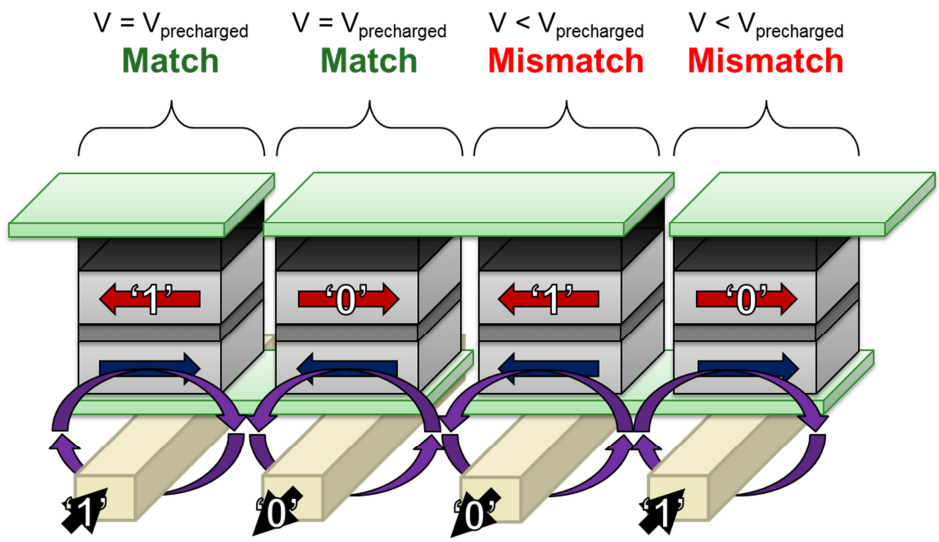


Figure 4.9: Example of a Match-In-Place™ engine made by the serial connection of 4 MLU in a NAND chain. The input binary pattern '1001' is compared to the stored binary pattern '1010'. When the input pattern does not match the stored pattern, the serial resistance of the chain is higher than its minimum level which is reached for perfect match.

The foundation of the MiP architecture is a quite sophisticated single cell that is very difficult to build economically with conventional semiconductor elements. Unlike standard memory cells that are only capable of storing, erasing, and reading individual bits, this cell can also directly compare the input bit to the stored bit, a necessary function for Match-In-Place. The single cell has to perform the Match-In-Place quickly in a native way without external circuitry.

Each cell can be viewed as a storage element represented by the storage layer intrinsically combined with a XOR gate. Multiple cells, typically 16 to 512 can be connected in series to form a NAND chain acting as a linear *Match-In-Place*^{TM} engine. Multiple NAND chains together can form a bidimensional *Match-In-Place*^{TM} matrix that matches simultaneously one input pattern with multiple stored patterns. When no current flows though the field lines the NAND chains naturally orient the sense layers in the direction that creates a match: At rest the sense layers are always oriented by their proximity to the storage layers regardless of whether a "1" or a "0" was stored. The total resistance of the chain at rest will always be n times the value of the resistance of each cell at rest. During the active matching mode, all field lines carry currents that orient each field line's associated sense layer. If all sense layers in a chain are oriented in a way that matches all the bits in the stored word, the total resistance of that chain will be exactly the same as it was when measured at rest, but any mismatched chains will have lower resistance. The differential sensing components at the end of each chain simultaneously measures the level of matching for all stored words.

An MLU-based Match-In-Place cell will retain the stored bit when power is removed. This avoids any need to reload the stored information, a step that exposes the information to hacking. An MLU-based Match-In-Place engine can handle unlimited write cycles, and a read or match cycle does not disturb the stored information. The read cycle of an individual cell is extremely fast; a compare can occur in as little as 5ns. Program cycles can be implemented through a separate path with a cycle time of about 20ns. In brief, the MLU cells are highly suitable for the fast Match-In-Place architecture. Other expected advantages of this architecture are:

- The stored patterns are never read, and never exposed to potential attacks from hackers.
- The matching cycles are very quick and can potentially be orders of magnitude faster than existing methods and use less power.
- Match-In-Place engines can act as a hardware accelerator, and simplify the overall chip.
- The cost structures of the secure chips are considerably reduced.

4.4.2 CAM memories

An interesting aspect of Match-In-Place™ engines is that they can perform simultaneously the match operation between the input and an arbitrary number of stored keys. Indeed, SR-MRAM being derived from TAS technology, field lines are shared between words by bits of the same bit address. Hence, the sense layers magnetizations in cells sharing a common field line will switch to an identical direction, and therefore input value. **This massively parallel matching functionality can be employed to develop fast associative memories and notably content-addressable memory (CAM)** that are usually very expensive to manufacture and power-consuming, yet in high demand as they are employed in most computer networking devices like switches and routers.

A design example of an 8x3 Match-In-Place check engine is presented in *Figure 4.10*. In this implementation, three NAND chains of 8 cells each are compared simultaneously. This allows fast comparison of a particular input pattern against multiple stored patterns. This concept of an 8x3 table could be extended to significantly larger look up tables. For example, a 512x10K look up table with this type of architecture could compare a 512-bit input word with 10K stored entries simultaneously in about 15ns.This simple binary CAM design can be converted into a ternary CAM by adding a “don’t care” state, a straight forward extension of the MLU architecture.

The current polarity is chosen to maintain an antiparallel alignment of the storage and sense layer magnetizations for the matching bits, so that any mismatch between the input and stored word will lead to a measurable drop in resistance. Therefore, in case of a perfect match, the resistance measured will be identical to the reference.

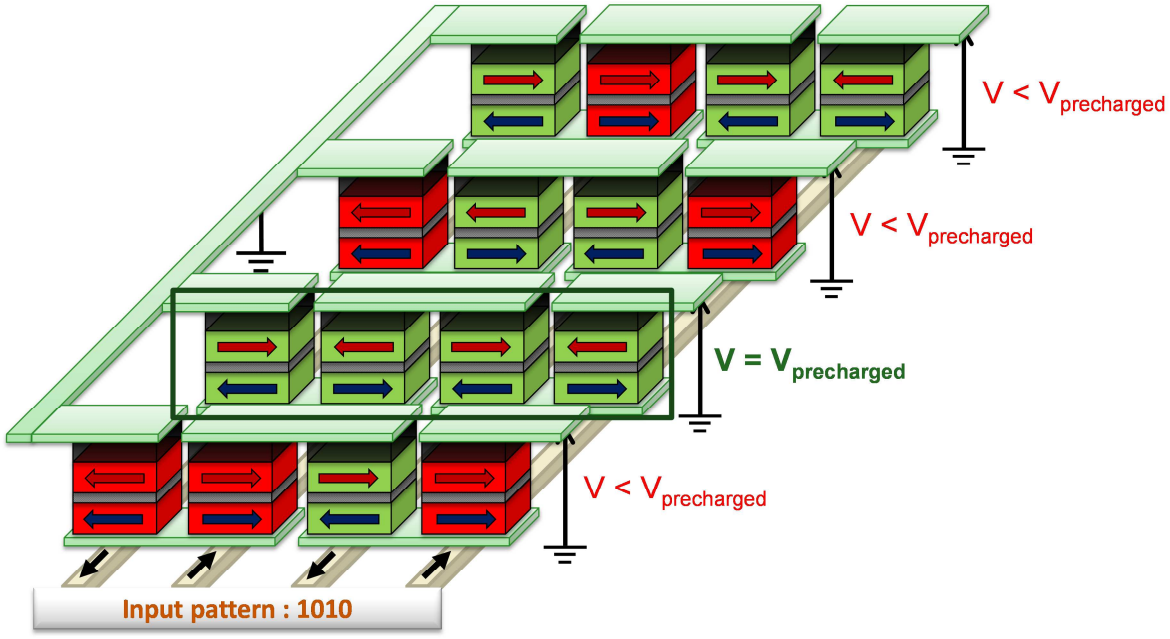


Figure 4.10: .Example of a content-addressable memory (CAM) with 4 Match-In-Place™ engines. The input binary pattern ‘1010’ is compared to the memory content and matched with the lowest voltage for a set reading current value.

4.5 MLU-BASED MAGNETIC SENSORS

Another application of the MLU based architecture is represented by 2D and 3D magnetic sensors.

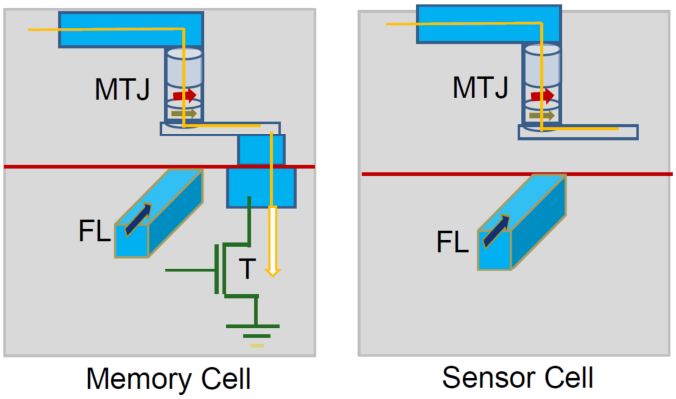


Figure 4.11: Schematic representation of the MLU memory cells (left) and of the basic magnetic sensors proposed in the IMAGSENS project (right)

The specific sensors proposed by Crocus are based on an array of many MTJs (series or parallel), aligned along multiple in-plane angles. The reference layer is typically programmed during manufacturing by using Crocus patented Differential Thermally Assisted Programming (DTAP) technology. This alignment in plane is guaranteed by the TAS technology, which allows to align independently each sensor in the array, similarly to the memory concept – see *Figure 4.11*. Indeed, the storage layer can be set individually for each magnetic cell by a standard TAS writing process. The sensing layer is under the influence of the coupling magnetic field created by the pinned storage layer as well as the magnetic field created by the field line

The output resistance of the sensor is sensitive to external magnetic fields both in magnitude and direction. During the reading cycle, the MTJ is placed at the instable point where these two fields have similar magnitudes – see *Figure 4.12. A* small external field (the field to be measured) will be enough to flip the magnetization of the sensing layer.

The actual sensor device is designed by using a large number of MTJs arranged in an array. Not only does this give and inherently robust device, this gives great flexibility in creating output resistances of magnetoresistor from several ohms to a hundred kΩs which is very useful to target different applications. Additionally such sensor devices can be directly power with relatively large voltages. A CMOS control module is measuring the output resistance, and adjust the input current in the field line in such a way that all MLU amplifiers are set at the inflection point mid-level between minimum and maximum impedance. This CMOS control module will compensate for temperature variations, and other drifts keeping the impedance at the inflexion point. Such parameter variations will produce a similar drift in all MLU amplifiers by contrast to the effect of an external field. The MLU aligned with the external field will react strongly whereas the MLU at 90° will be insensitive to it. A sensing module will read the input impedances of all MLU amplifiers located at different angles. From these measurements, the CPU will be programmed to calculate the orientation of the external field with respect to the sensor.

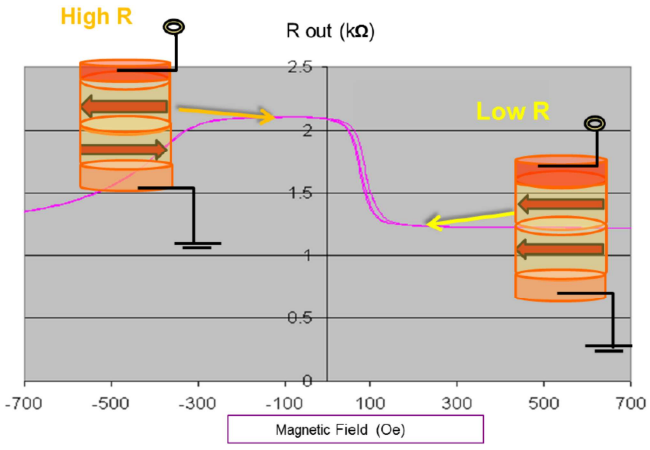


Figure 4.12: Typical R(H) loops measured for the proposed MLU based magnetic sensors

4.6 INDUSTRIALIZATION OF THE MLU TECHNOLOGY

Self-reference TAS MRAM enables a number of previously unachievable breakthroughs in magnetic technology implementation, including ultra-sensitive magnetic sensors, highly robust secure embedded memory, ultra-high-temperature non-volatile memory (NVM) operation (e.g., ~200° C), order-of-magnitude higher density hardware-based table searches (e.g., content addressable memory), high density multi-bit storage, and scaling to sub-20nm manufacturing. The MLU technology has been developed as a platform technology that serves as a base for multiple products, from magnetic sensors, to memories, to security products.

4.6.1 MLU based embedded memories

On the memory side type of applications, MLUs based memories could compete with Flash memories, having namely shorter R/W cycle and smaller footprint. In addition, Crocus' MLU™ architecture offers a highly reliable approach for building non-volatile memory capable of operating at 250°C or higher, in comparison to Flash and other technologies that are effectively limited to 150°C or lower, making it competitive for extreme environment such as automotive, energy exploration and defense.

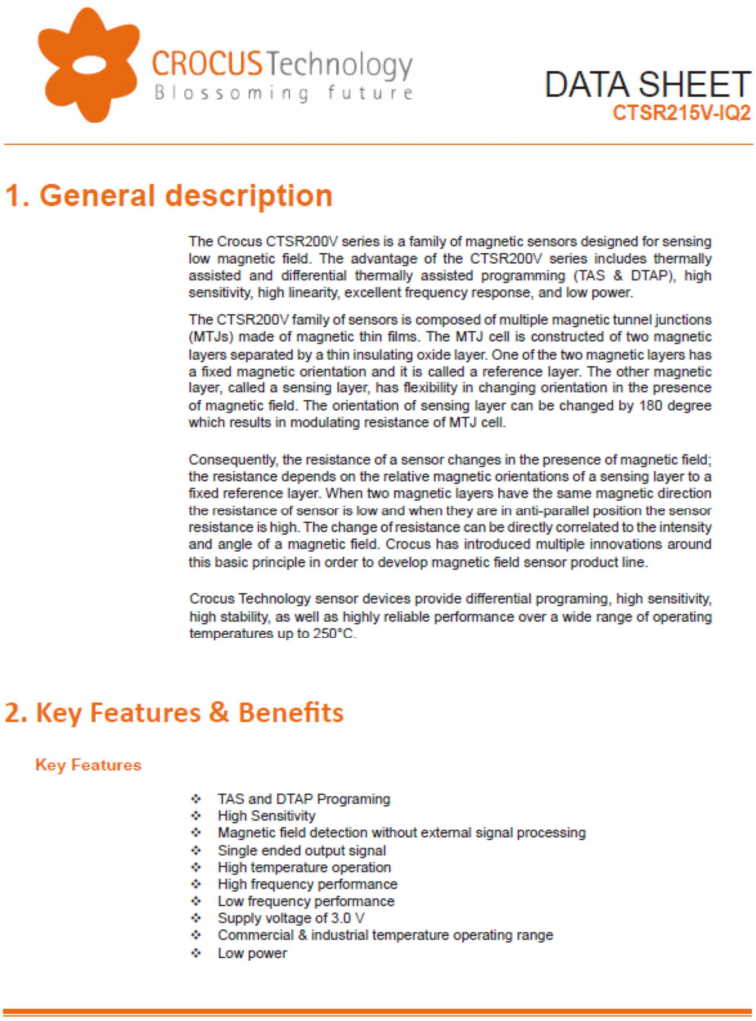
Crocus Technology MLU™ microcontroller brings unrivalled read and write performance capability in a very small footprint. CT32MLU_LTE targets GSM and LTE SIM applications. Its performances offer the best solution for secure personalization and OTA updates - see *Figure 4.13*.

Figure 4.13: Characteristics of the low-power microcontroller product based on the MLU technology (from Crocus website)

4.6.2 MLU based Magnetic sensors

The Crocus CTS series (example in *Figure 4.15*) is a family of magnetic sensors designed for sensing low magnetic field. The advantage of the CTS series includes TAS programing, high sensitivity, high linearity, excellent frequency response, and low power.

Crocus sensors for current sensing that offer significant advantages: high sensitivity, excellent linearity, high frequency performance in the MHz range, both DC and AC sensing, high reliability, a small footprint and low power consumption. Crocus magnetic sensors can also be used as effective switch products. These are ideal for replacing reed relay switches and other magnetic sensors used in switch applications.



CROCUS Technology
Blossoming future

DATA SHEET
CTSR215V-IQ2

1. General description

The Crocus CTSR200V series is a family of magnetic sensors designed for sensing low magnetic field. The advantage of the CTSR200V series includes thermally assisted and differential thermally assisted programming (TAS & DTAP), high sensitivity, high linearity, excellent frequency response, and low power.

The CTSR200V family of sensors is composed of multiple magnetic tunnel junctions (MTJs) made of magnetic thin films. The MTJ cell is constructed of two magnetic layers separated by a thin insulating oxide layer. One of the two magnetic layers has a fixed magnetic orientation and it is called a reference layer. The other magnetic layer, called a sensing layer, has flexibility in changing orientation in the presence of magnetic field. The orientation of sensing layer can be changed by 180 degree which results in modulating resistance of MTJ cell.

Consequently, the resistance of a sensor changes in the presence of magnetic field; the resistance depends on the relative magnetic orientations of a sensing layer to a fixed reference layer. When two magnetic layers have the same magnetic direction the resistance of sensor is low and when they are in anti-parallel position the sensor resistance is high. The change of resistance can be directly correlated to the intensity and angle of a magnetic field. Crocus has introduced multiple innovations around this basic principle in order to develop magnetic field sensor product line.

Crocus Technology sensor devices provide differential programing, high sensitivity, high stability, as well as highly reliable performance over a wide range of operating temperatures up to 250°C.

2. Key Features & Benefits

Key Features

- TAS and DTAP Programing
- High Sensitivity
- Magnetic field detection without external signal processing
- Single ended output signal
- High temperature operation
- High frequency performance
- Low frequency performance
- Supply voltage of 3.0 V
- Commercial & industrial temperature operating range
- Low power

Figure 4.14: Characteristics of the magnetic sensors product based on the MLU technology (from Crocus website)

4.7 CONCLUSIONS ON SR-TAS-MRAM

In addition to TAS-RAM, a new concept named Self-Reference, which is at the heart of Magnetic Logic Unit (MLU) architecture, has been proposed and developed. SR goes much further in resolving additional challenges and enabling new functionalities and capabilities. The key feature of the SR MTJ is that it does not require a fixed reference layer. This is achieved by removing the antiferromagnetic layer that pins the reference. As a result, the magnetization of this layer is free to vary and is renamed as the sense layer.

The SR memory cell operates differently from the standard fixed reference TAS memory cell. The mechanism of writing data into the memory cell in *SR-TAS-MRAM* and *TAS-MRAM* configurations is identical: A small current flows through the MTJ and heats the cell to the critical write temperature while applying a magnetic field to orient the storage layer. Then, the MTJ is cooled while write field is maintained, essentially "freezing" the magnetic state into the storage layer. Heating current was optimized by including thermal barrier inside and around the MTJ.

The read mechanisms in the standard TAS-MRAM and SR-TAS-MRAM are quite different. In the SR case, read is achieved by measuring the MTJ resistance twice. The first measurement is performed with the sense layer aligned in one direction and the second measurement in the opposite direction. The alternate alignment of the sense layer is achieved by changing the direction of the magnetic field produced by the field line. The magnitude of the field line current required to align the sense layer is roughly equal to field line current required to write sequence.

In order to optimize the read and write field requirements, we developed a macrospin model based on the Stoner-Wohlfarth model of magnetization reversal. By introducing magnetostatic, RKKY and ferromagnet / antiferromagnet exchange coupling phenomena, we calculated a general form of the energy for any type of MRAM magnetic stack.

Several improvements to MLUs have been investigated i) a decrease in the write field amplitude obtained thanks to a new write procedure which uses the sense layer as a local amplifier of the write field; ii) an increase in the storage capacity achieved in MLU thanks to multibit recording either in single domain state or in vortex state. A previously proposed highly efficient switching mode, relying on the magnetostatic interactions between the sense and the storage layer, was effectively predicted by the model and experimentally demonstrated in new samples. An excellent agreement was obtained between the model and the experimental results. Increasing the stiffness of the storage layer was found to be critical in order to minimize the read field requirements at decreasing patterning dimensions. Material developments were performed to maximize the RKKY coupling in the synthetic ferrimagnet storage layer.

In order to study the reproducibility of the write operation, the influence of thermal activation was modelled by calculating energy barriers and transition paths and compared with on-the-fly measurements of switching probabilities on the new set of samples with a stiffer storage layer. Again, an excellent agreement was obtained between the model and the experiments.

Based on the model developed, we built a roadmap describing the magnetic stack to use, that allows a downscaling of the self-referenced MRAM down to 45 nm while conserving manageable field requirements. Due to fundamental limitations in field-induced switching MRAM technology, reaching higher densities was found to require increasing the individual storage capacity of each MTJ, i.e. storing multiple bits per unit cell.

A new angle-based storage method taking advantage of the sense layer free magnetization was investigated. Using the magnetic model developed previously, suitable samples were designed and allowed to experimentally demonstrate up to 4 bits per single MTJ. The field requirements were however found to be substantially higher than those compatible with a fully functional product. A new write method, predicted by the model, was investigated and exploited in the building of a second roadmap down to 45 nm.

1kbit prototypes were used to evaluate the proof of concept and the efficiency of the SR-TAS-MRAM – see figure 4.14. With significant advantages over other field-switched MRAM technologies and a wide range of alternative applications, SR-MRAM magnetic stacks could constitute major industrial and commercial stakes for Crocus Technology.

The SR read not only enables a very robust memory cell but also allows it to be used as a logic element. Direction of the current flowing in the field line can be used as an information input. The resistance of the cell now compares the stored information and the input information - if sense and storage layers are aligned in parallel the resistance is low and if sense and storage layers are anti-parallel the resistance is high. The element acts as an XOR (exclusive OR) logic device whose output depends on the comparison of the stored information and an input information (via the field line).

Starting from MLU concept, Crocus has developed an innovative function called Match-In-Place, to authenticate users without exposing any confidential data to a security attacker. Each cell of the Match-In-Place architecture is a non-volatile memory cell combined with the virtual XOR gate of the MLU. Multiple cells are connected in series to form a NAND chain acting as a linear Match-In-Place engine. If multiple Match-In-Place NAND chains are placed in parallel, they can act in the same time to compare one pattern against many. Fields of use of this new architecture are quite wide and include secure microcontrollers, biometric devices and associative memory devices.

The MLU technology has been developed as a platform technology that serves as a base for multiple products, from magnetic sensors, to memories, to security products.

Self-reference TAS MRAM enables a number of previously unachievable breakthroughs in magnetic technology implementation, including ultra-sensitive magnetic sensors, highly robust secure embedded memory, ultra-high-temperature non-volatile memory (NVM) operation (e.g., ~200° C), order-of-magnitude higher density hardware-based table searches (e.g., content addressable memory), high density multi-bit storage, and scaling to sub-20nm manufacturing. The DTAP technology enables unique differential programming of sensors devices that leads to improved performance.

Due the possibility to program both magnetic layers individually, self-referenced MRAM can be operated as a Magnetic Logic Unit, combining in-stack the storage and exclusive-or logic functions and thereby opening new application ranges. Due to its characteristics, SR-MRAM appears as a technological solution for high-density storage and other applications like associative storage and authentication device.

5. THERMALLY ASSISTED STT-MRAM

THERMALLY ASSISTED STT-MRAM concept

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14. **IL Prejbeanu**, R Sousa, *MRAM Cell and Method for Writing to the MRAM Cell using a Thermally Assisted Write Operation with a Reduced Field Current*, 2012EP-290019: 16/01/2012

PhD THESIS

1. Jérémy Herault (co-supervising 33%) - R&D engineer Crocus Technology

Mémoire magnétique à écriture par courant polarisé en spin assistée thermiquement
Université Joseph-Fourier, Grenoble, Oct. 4 2010, Directeur de thèse : Alain Schuhl

2. Antoine Chavent (co-supervising 33%) – PhD ongoing

Bipolar TAS
Université Joseph-Fourier, Grenoble, to be defended 2015, Directeur de these: Bernard Dieny

As explained in chapter 3, there are several advantages in using a thermally assisted MRAM concept, the main one being the decoupling of the thermal stability (memory retention) and the write power consumption (writeability), since the bit can have simultaneously a low write field at the write temperature and be stable in the operating temperature range. **The problem with the field driven writing of TAS-MRAM cells is still that the magnetic field needs to be generated by a current line with current pulses of a few mA**. TAS-MRAM requires a single magnetic field and lower field values compared to the toggle MRAM approach, thus lowering the total power consumption. **However, the write field does not scale with cell size and can be at best kept constant, unlike STT-MRAM where the write current scales with cell size**. In TAS-MRAM, the heating current is not the bottleneck, since the use of thermal barriers has already demonstrated a heating current density in the 1-2×10^6A/cm² range, similar to the lowest values of spin transfer torque MRAM cells (STT-MRAM). **Alternatively, it is possible to get rid of the field line by still using the thermally assisted concept but combining it with spin transfer torque (STT) to switch an exchange biased storage layer**[53]. In this case, the same current flowing through the cell is used both to heat up the cell and switch the storage layer magnetization by STT. **It is thus possible to combine the added stability obtained from the exchange biasing to retain the information with the reduction of the current through cell size scaling, since the cell switching occurs at a constant current density, typically in the 10^6A/cm² range**. **These studies have been done during the PhD thesis of Jérémy Alvarez-Hérault.**

The STT MRAM cell is simplified since no field lines are required. Each cell only consists of a MTJ connected in series with a selection transistor. The writing is performed using bipolar pulses of current. In STT-MRAM, spin-transfer torque is used to switch the magnetization of the storage layer instead of magnetic field. The reading is performed at lower current to avoid write errors during read. The write voltage must be significantly lower than the breakdown voltage of the tunnel barriers. The main difficulty is to have the three distributions of breakdown voltage (typically around 1.2-1.7V), write voltage (typically in the range 0.5 to 0.7V) and read voltage (typically between 0.1 and 0.2V) well separated in a multi Mbit chip. Writing a “0” (i.e. a parallel configuration of the magnetization in the storage and pinned layer) can be achieved by sending a current pulse through the stack, the electrons flowing from the pinned layer to the storage layer. Writing a “1” can be achieved by sending a pulse of current of opposite polarity.

This approach clearly solves the write selectivity issues of the SW-MRAM since the write current flows only through the addressed cell so there is no risk of writing an unselected cell. Another major advantage of the STT write approach is the down-size scalability. Indeed, the critical current for which the magnetization switches due to the STT influence is determined by a critical current density so that the total current required writing a memory cell scales as the area of the cell, assuming a constant free layer thickness. **As a result, the STT writing approach offers good scalability in STT-MRAM down to cell size of the order of 45 nm. Below this dimension, there is still an issue which concerns the thermal stability of the information written in the cell.** For a storage application, it is of primary importance that once written, the magnetization orientation of the storage layer remains stable for typically 10 years, chosen for stability criterion). This actually defines the retention of the memory. As the size decreases, the volume also decreases and the storage layer magnetization becomes more and more unstable. The effective anisotropy may be increased by giving to the cell an elongated shape i.e. increasing the shape anisotropy. However, but this works only up to an aspect ratio of about 2.5. Above, the switching proceeds by nucleation/propagation of domain walls rather than coherent rotation, leading to micromagnetic states which are detrimental to the MRAM functioning. Furthermore, using materials with higher uniaxial anisotropy leads to a correlated increase in the Gilbert damping α, and correlatively to an increased writing consumption. Indeed, damping and anisotropy are often related since they have a common origin: spin-orbit coupling. An increased

53 B. Dieny and O. Redon, patent FR2832542

damping implies higher write current density which is not suitable because this means excessively large selection transistors as well as excessive electrical stress across the tunnel barrier.

5.1 SPIN-TORQUE-TRANSFER MRAM (STT-MRAM)

In STT (spin transfer torque) writing, a polarized electrical current exerts a torque called spin-transfer torque (STT) on the magnetization of the storage magnetic layer, which can switch its direction for a large enough current density. The STT-MRAM cell is simplified in comparison to FIMS-MRAM cell since no field lines are required. The STT writing is performed with bipolar pulses of current. The reading is performed at lower current to avoid write errors during read.

Writing a "0" (i.e., a parallel configuration of the magnetization in the storage and pinned layers) can be achieved by sending a current pulse through the stack, the electrons flowing from the pinned layer to the storage layer. Writing a "1" can be achieved by sending a pulse of current of opposite polarity. This approach clearly solves the write selectivity problem of the SW-MRAM since the write current flows only through the addressed cell so there is no risk of writing an unselected cell. Another major advantage of the STT write approach is the down-size scalability. Indeed, the critical current for which the magnetization switches due to the STT influence is determined by a critical current density so that the total current required writing a memory cell scales as the area of the cell, assuming a constant free layer thickness. As a result, the STT writing approach offers much better down-size scalability than FIMS-MRAM. However, at very small dimensions, there are still problems concerning the thermal stability of the information written in the cell. These limit the down-size scalability of in-plane magnetized STT-MRAM down to about 60nm × 150nm and for out-of-plane magnetized STT-MRAM to dimension of the order of 20 nm as explained further.

5.1.1 Principle of STT writing

When a spin-polarized current flows through a magnetic nanostructure, the STT effect results from the interaction between the spin of the conduction electrons and those responsible for the nanostructure magnetization. This torque is exerted on the local magnetization and tends to switch it towards a direction parallel or antiparallel to that of the spin polarizing layer depending on the current direction. The physical origin of the STT can be summarized as follows:

- each conduction electron carriers angular momentum $\frac{\hbar}{2}$. Considering that the current has a finite spin polarization (typically between 40% and 80%), the number of electrons per unit time and unit area flowing perpendicular to the plane of the layers is given by $\frac{J}{e}$ (J being the current density and e the absolute value of the electron charge) so that the corresponding flow of angular momentum per unit area is $\eta\frac{J}{e}\frac{\hbar}{2}$. When such a spin polarized incoming flow of electrons penetrates in a magnetic layer, the spin of these electrons gets reoriented in the direction parallel to the local magnetization within a thickness of about 1nm. This corresponds to an interfacial absorption of the incoming flow of transverse angular momentum. By conservation of overall angular momentum, this absorption results in a torque exerted on the local magnetization, the spin-transfer torque (STT) given by:

$$\Gamma_{STT} = -\gamma\eta\frac{J}{e}\frac{\hbar}{2}\frac{1}{\mu_0 M_s d}\hat{m}\times\left(\hat{m}\times\hat{p}\right) \qquad (5.1)$$

where $\hat{m}$ and $\hat{p}$ are unit vectors respectively along the magnetic nanostructure magnetization and incoming spin-polarization (often set by the direction of magnetization of the reference layer in a MTJ), d is the nanostructure thickness along the current direction, M_s its magnetization and γ is the

gyromagnetic ratio, μ_0 the vacuum permeability. This expression was first established by Slonczewski in 1996[54]. In magnetic tunnel junctions, it was shown that the STT also introduces a second term called field-like term but which has an amplitude of only 10 % to 25 % of the STT damping torque. This second term is considered as having a negligible role in the design of STT-MRAM[55].

The general Landau-Lifshitz-Gilbert (LLG) equation governing the dynamics of magnetization of the magnetic nanostructure is modified to include this STT term:

$$\frac{d\hat{m}}{dt} = -\gamma\left(\hat{m}\times\vec{H}_{eff}\right) + \alpha\left(\hat{m}\times\frac{d\hat{m}}{dt}\right) + \frac{\gamma\hbar}{2\mu_0 M_s}\frac{1}{d}\frac{\eta J}{e}\hat{m}\times\left(\hat{m}\times\hat{p}\right) \qquad (5.2)$$

In this equation, the first term describes a precessional motion of the magnetization around the local effective field $\vec{H}_{eff}$ which contains contributions from the applied field, the demagnetizing field, the anisotropy field, and the STT field-like term (if it is taken into account). This first term is conservative, i.e., conserves energy. The second term is the Gilbert damping term which describes the magnetic dissipation in the system, i.e., the fact that in the absence of STT influence, the magnetization tends to gradually relax towards the local effective field. This term always dissipates energy. The third term is the STT previously discussed. Interestingly, this term is also non-conservative. Furthermore, depending on the current direction through the magnetic nanostructure (e.g. the storage layer in a STT-MRAM cell), this term can absorb or dissipate energy, which means that it either behaves as a damping or antidamping term. If the current has the proper direction and the current density is large enough, the STT antidamping effect can exceed the natural Gilbert damping. Very peculiar magnetization dynamics effects then arise, such as STT-induced magnetization switching or magnetization steady-state oscillations[56]. STT-induced magnetization switching provides a new way to write the information in MRAM or logic devices. STT-induced steady-state magnetic oscillations allow the generation of RF voltage and thus new types of frequency-tunable RF oscillators.

The possibility to use the STT to switch the magnetization of a free layer in a magnetoresistive stack was first demonstrated in metallic pillars called spin-valves traversed by a current flowing perpendicular to the plane of the layers. The latter comprise a thick magnetic layer of fixed magnetization acting as a current polarizer and a second magnetic layer of switchable magnetization that reacts to the STT influence from the fixed layer magnetization. These two magnetic layers are magnetically decoupled thanks to a thin, non-magnetic, metallic spacer, typically Cu 3 to 5 nm thick. The current density required to switch the magnetization in these metallic pillars was of the order of 2.10^7 A/cm². A few years later, thanks to the progress made in the development of low RA (resistance × area product) magnetic tunnel junctions, magnetization switching induced by STT was also observed[4]. Interestingly, the current density required to write in MTJ was lower than in metallic pillars (in the range 2-6 $\times 10^6$ A/cm² in MTJ) mainly due to a higher effective spin polarization in MTJ compared to spin-valves. Since then, the interest in STT in MTJs for STT-MRAM applications has kept on increasing. STT indeed provides a powerful write scheme in MRAM for several reasons:

- In STT-MRAM there is no need to create pulses of magnetic field. Each cell is directly written by the current flowing through the stack. As a result the cells are much more compact than in field-written MRAM, as illustrated in *Figure 5.1*.

54 Slonczewski J., "*Currents and torques in metallic magnetic multilayers*", J.Magn.Magn.Mater.159, L1 (1996); "*Excitation of spin waves by an electric current*", 195, L261 (1999).

55 D.E.Nikonov, G.I.Bourianoff, G.Rowland, and I.N.Krivorotov, « strategies and tolerances of spin transfer torque switching", Journ.Appl.Phys.107, 113910 (2010).

56 W. H. Rippard, M. R. Pufall, S. Kaka, S. E. Russek, and T. J. Silva, "Direct-Current Induced Dynamics in Co90Fe10/Ni80Fe20 Point Contacts", Phys.Rev.Lett.92, 027201 (2004).

- During write of a selected cell, the corresponding selection transistor in series with the MTJ is closed so that the write current flows only through the selected cell. This provides excellent write selectivity, much better than in field-written MRAM.

In STT writing, the condition for magnetization switching is set by a critical current density j_c (actually two critical current densities, $j_c^{P\to AP}$ and $j_c^{AP\to P}$). The magnetization of the storage layer switches if the current density of proper direction exceeds j_c. This provides very good down-size scalability since the total current required to write scales like the cell area down to very small dimensions where it becomes limited by the thermal stability factor.

One can define switching voltages associated with the critical switching current densities. They are given by $V_c^{P\to AP} = (RA)_P(V)\, j_c^{P\to AP}$ and $V_c^{AP\to P} = (RA)_{AP}(V)\, j_c^{AP\to P}$ where RA is the voltage-dependent resistance × area product of the MTJ in the corresponding magnetic configuration. Interestingly, in MTJ, whereas the critical current $j_c^{P\to AP}$ can be typically twice larger than the critical current $j_c^{AP\to P}$ due to a weaker STT efficiency in P than in AP configuration, the critical voltage for switching from P to AP and from AP to P: $V_c^{P\to AP}$ and $V_c^{AP\to P}$ are very close in absolute values due to the larger RA value in the AP than in the P configuration.

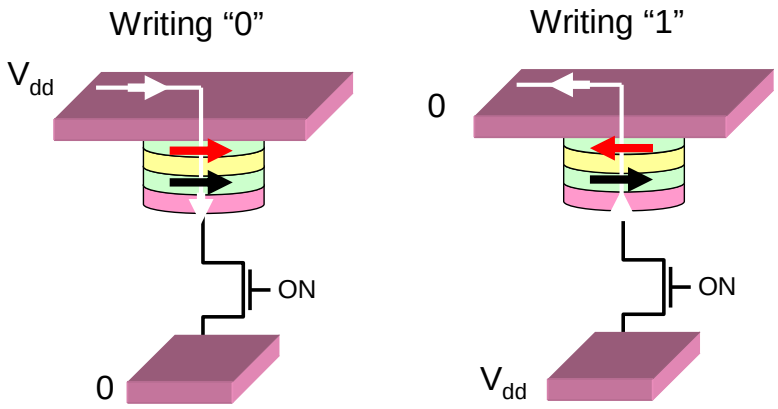

Figure 5.1: Principle of writing in STT-MRAM. Each STT-MRAM cell consists of an MTJ connected in series with a transistor. To write the parallel magnetic configuration, a current flow of density larger than jcAP→P is sent through the MTJ from the storage layer (red arrow) to the pinned reference layer (black arrow) (i.e., electrons tunnel from the pinned reference layer to the free layer). To write the antiparallel magnetic configuration, a current flow of density larger than jcP→AP is sent through the MTJ from the reference layer (red arrow) to the storage layer.

5.1.2 Considerations of breakdown, write, read voltage distributions

In conventional STT-MRAM, the write and read current paths are the same. In order to avoid write disturbance during read, the read voltage must be chosen low enough compared to the critical write voltage. **There are therefore 3 voltage cell-to-cell distributions in an MRAM chip which need to be well separated for proper functioning and reliability of the chip.** This is schematically illustrated in *Figure 5.2*. These 3 distributions are:

1. **The breakdown voltage distribution.**
   The MTJ tunnel barrier is a thin dielectric oxide layer (MgO ~1 nm thick). When exposed to an excessively large voltage, this barrier may experience dielectric breakdown. The breakdown voltage in the MTJ depends on the voltage pulse duration, the number of pulses, and even on

the delay between pulses[57]. Compared to CMOS dielectrics, these ultrathin MgO barriers are relatively resistant to breakdown. This mainly comes from the fact that the tunneling through the barrier is direct in normal working conditions, in contrast to Fowler-Nordheim tunneling as in Flash memories. As a result, upon cycling, less defects are generated in the MgO barrier than in CMOS oxides for Flash memory. For voltage pulse width in the range of 10ns, the voltage breakdown is usually larger than 1.2 V even for RA ~ 5 Ωμm².

2. **The write voltage distribution**
   At each write event (and to lesser extend read event), the tunnel barrier is exposed to an electrical stress which may cause electrical breakdown. To avoid breakdown failure, the highest write voltage in the distribution must be sufficiently low compared to the weakest MTJ in terms of breakdown. By adjusting the MTJs stack composition and their RA, one tries to get this write voltage distribution centered around 0.5 V and be as narrow as possible (typical width as illustrated in *Figure 5.2*). The distribution width mainly originates from fluctuations in the shape and particularly in edge defects associated with the patterning process.
3. **The read voltage distribution**
   The read voltage distribution originates from the variation in the resistance of the selection transistor which is connected in series with the MTJ. The read voltage across the MTJ is typically in the range 0.1 to 0.15 V. The read voltage has to be low enough compared to the write voltage in order to avoid any write disturbance during read caused by the STT from the read current. However, the lower the read voltage, the slower is the read-out process. Therefore, a trade-off has to be found.

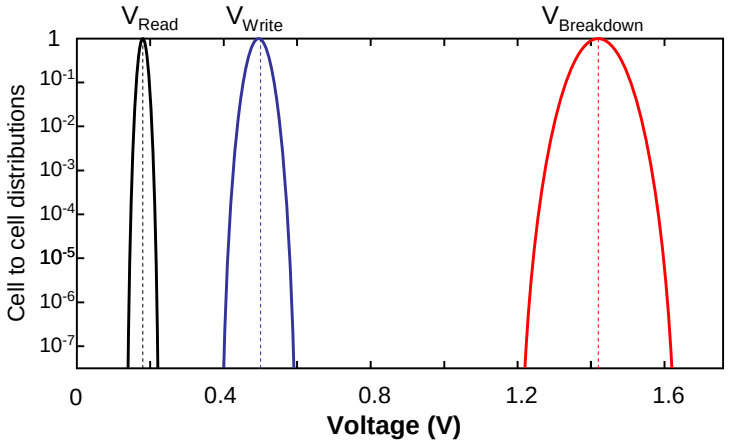

Figure 5.2: Schematic representation of the 3 voltage distributions (read, write, and breakdown) specific for STT-MRAM functioning

5.1.3 Influence of STT write pulse duration

The global picture of STT switching vs. the current pulse width is shown in Figure 5.3[58]. As commonly observed in microelectronics, the larger the voltage (i.e., the current density), the faster the operation. Two distinct switching modes have been found, namely thermal activation and precessional switching[59]. At finite temperature, thermal activation plays an important role in reducing the switching current at long current pulses (>10ns). In this slow thermally-activated switching regime, the switching

57 S. Amara-Dababi, R. C. Sousa, M. Chshiev, H. Béa, J. Alvarez-Hérault, L. Lombard, I. L. Prejbeanu, K. Mackay, and B. Dieny, "*Charge trapping-detrapping mechanism of barrier breakdown in MgO magnetic tunnel junctions*", Appl. Phys. Lett. 99, 083501 (2011).

58 J. Z. Sun, IBM J. Res. & Dev. 50, 81 (2006). A. A. Tulapurkar, T. Devolder, K. Yagami, P. Crozat, C. Chappert, A. Fukushima, and Y. Suzuki, Appl. Phys. Lett. 85, 5358 (2004).

59 Zhitao Diao, Zhanjie Li, Shengyuang Wang, Yunfei Ding, Alex Panchula, Eugene Chen, Lien- Chang Wang, and Yiming Huai, J. Phys.: Condens. Matter. 19, 165209 (2007).

current depends on the current pulse width τ and thermal stability factor $\Delta=K_uV/k_BT$ of the free layer[60,61]:

$$J_c(\tau) = J_{c0}\left[1 - \frac{k_BT}{K_uV}\ln\left(\frac{\tau}{\tau_0}\right)\right] \quad (5.3),$$

where $\tau_0 \sim 1ns$ is the inverse of the attempt frequency and K_uV is the anisotropy energy. J_{c0} is the so-called critical current which corresponds to the linearly extrapolated value of the switching current density for a pulse duration of 1 ns.

For fast precessional switching, in the nanosecond regime, the required switching current is several times greater than the critical current. In this regime, the switching time varies as

$$\tau_{switching} = \frac{(1+\alpha^2)}{\gamma H_K} J_{c0} \frac{Ln\left(\frac{\pi}{\theta_0}\right)}{\left(\frac{J}{J_{c0}} - 1\right)} \quad (5.4)$$

where α is the Gilbert damping, H_k the anisotropy field, γ the gyromagnetic ratio, and θ_0 is the angle between the storage layer magnetization and the current spin polarization at the onset of the current pulse. This initial angle is often due to random thermal fluctuations which may cause stochasticity in the magnetization switching and slow down the write process. Some particular tricks such as one with orthogonal polarizers [62] may help to improve the reproducibility (deterministic character) of the switching dynamics. *Equation (5.4)* illustrates that the larger the current density, the faster the switching, i.e., the shorter the write current pulse. In this regime, the tunnel barrier may however be exposed to a too large electrical stress which may result in accidental electrical breakdown. Typical write speeds in operation in STT-MRAM are around 5 to 10 ns, which corresponds to the intermediate regime between thermally activated and precessional switching.

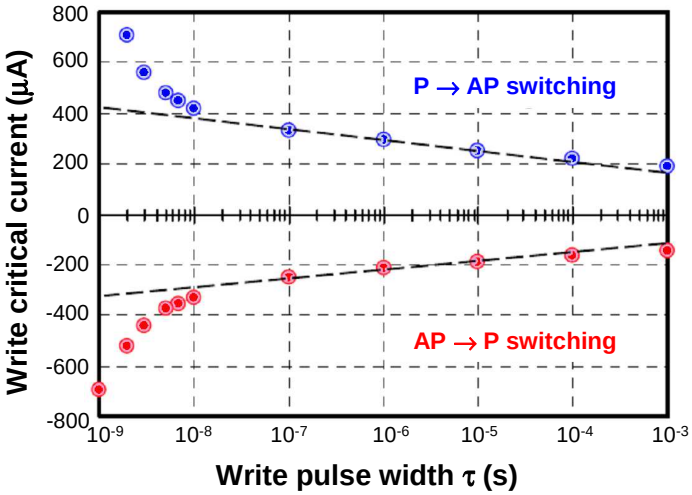

Figure 5.3: Typical values of STT switching current density (normalized by J_{c0}) as a function of write pulse width.

60 J. Z. Sun, Phys. Rev. B 62, 570 (2000).

61 R. Heindl, W. H. Rippard, S. E. Russek, M. R. Pufall and A. B. Kos, J. Appl. Phys. 109, 073910 (2011)

62 de Castro, M. Marins, Sousa, R. C., Bandiera, S., Ducruet, C., Chavent, A., Auffret, S., Papusoi, C., Prejbeanu, I. L., Portemont, C., Vila, L., Ebels, U., Rodmacq, B., Dieny, B. *Precessional spin-transfer switching in a magnetic tunnel junction with a synthetic antiferromagnetic perpendicular polarizer* Appl. Phys. Lett. 100(20), 2024 10 May 14 (2012)

5.2 IN-PLANE STT-MRAM

The first investigated MTJs for STT-MRAM were in-plane magnetized MTJ, meaning that both magnetic electrodes have in-plane magnetization. The reason is mainly historical since, besides the tunnel barrier itself, their configuration is fairly close to that of spin-valves that had been developed for hard disk drive magnetoresistive heads since 1991. However, as will be explained further, their performance and down-size scalability is not as good as for STT-MRAM based on out-of-plane magnetized MTJ.

The expression of the critical current for switching obtained in a macrospin model and at zero temperature is[63]:

$$J_{c0} = \frac{2e\alpha\mu_0 M_s t_F \left(H + H_k + \frac{M_s}{2} \right)}{\hbar\eta} \qquad (5.5)$$

where H is the applied field along the easy axis, M_S and t_F the magnetization and the thickness of the storage layer, α is the damping constant, H_k the in-plane anisotropy field (magnetocrystalline and shape), η the spin transfer efficiency. This relationship is derived by analyzing the stability of the solution of the LLG *equation (5.2)* under STT influence. When the injected current has the proper direction and is larger than $J_c(\tau)$, τ being the pulse duration, the magnetization reverses. In this expression, the term $M_s/2$ is usually larger than $(H+H_k)$ by one or two orders of magnitude. This dominant role of the demagnetizing field term $(\mu_0 M_s/2)$ comes from the fact that during the STT-induced switching of the magnetization of the in-plane magnetized layer, the magnetization has to precess out-of-plane which increases the demagnetizing energy. As a result, a good approximation of J_{c0} is given by $J_{c0} = \frac{e\alpha\mu_0 M_s^2 t_F}{\hbar\eta}$. It is also important to note that because of the dominance of the demagnetizing field term, the critical current for STT writing weakly depends on H_k, the in-plane anisotropy field which determines the thermal stability of the magnetization at rest. In other words, in in-plane magnetized MTJs, the barrier for STT switching is mainly related to the demagnetizing energy whereas the barrier for thermal stability of the magnetization, i.e., the memory retention is determined by the in-plane shape anisotropy. The first barrier is usually much larger than the second one which means that the in-plane magnetized configuration is not efficient in terms of compromise between thermal stability and writability.

5.3 IN-PLANE TAS-STT-MRAM

5.3.1 Proof of concept

Alternatively, **thermal assistance was used to extend the scalability of STT-MRAM both with in-plane and out-of-plane magnetized materials. With in-plane magnetized materials, structures similar to the exchange biased storage layer stacks used for TAS--MRAM (in chapter 3) can be used** – see *figure 5.4*. The resistance state was switched between the low resistance and high resistance states by applying current pulses of alternating polarity across the junction. Each pulse first creates a temperature increase above the antiferromagnet blocking temperature. With the ferromagnetic layer no longer pinned, the spin-polarized current simultaneously exerts a torque on the ferromagnetic storage layer reversing its magnetization direction depending on the current direction.

63 Y. Huai, AAPPS Bulletin, vol. 18, No. 6 (2008)

The write voltage is then gradually decreased to zero so that the junction cools down while STT is still on. The antiferromagnet then freezes the new storage layer magnetization direction.

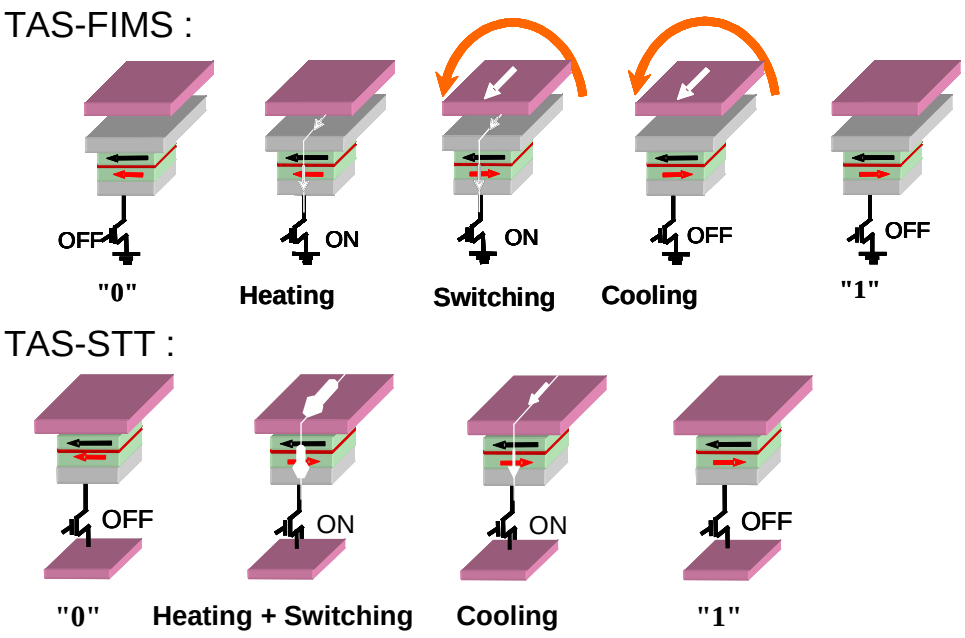

Figure 5.4 – TAS write principle combined with FIMS or STT. In TAS-FIMS, the temporary heating of the MTJ is combined with a pulse of magnetic field. In TAS-STT, the current flowing through the MTJ both heats the MTJ and exerts the magnetic torque which switches the magnetization.

Figure 5.5 illustrates the implementation of the thermal assistance combined with STT (TAS+STT) with in-plane magnetized MTJ. *Figure 5.5a and b* show the hysteresis minor loops measured before and after TAS+STT writing using pulses of bias voltage of ±1.1 V and duration of 30ns. Similarly to the TAS+FIMS approach, a change in the sign of the loop shift was produced during writing. *Figure 5.5c* indicates that by alternating the pulse polarity, the low resistance state or high resistance state could be repeatedly written. *Figure 5.5d* shows the probability of switching from P to AP and AP to P states as a function of the current density of the 30ns write pulse sent through the junction. 100% switching probability is obtained with current density in the order of 8 and 13×10^6A/cm², respectively for the antiparallel to parallel and the parallel to antiparallel transitions, which is of the same order of magnitude as in conventional in-plane STT experiments. **This implies that there is no detrimental increase in STT switching current density associated with the use of an exchange biased storage layer, while the thermal stability at stand-by temperature is greatly enhanced by the presence of exchange bias.** The thermal stability barrier can be estimated by fitting the switching probability by the theoretical Néel-Brown relaxation expression for the STT switching[64] yielding $KV/k_BT = 80$.

64 Koch, RH; Katine, JA; Sun, JZ, Phys. Rev. Let. Volume: 92 Issue: 8 088302 (2004)

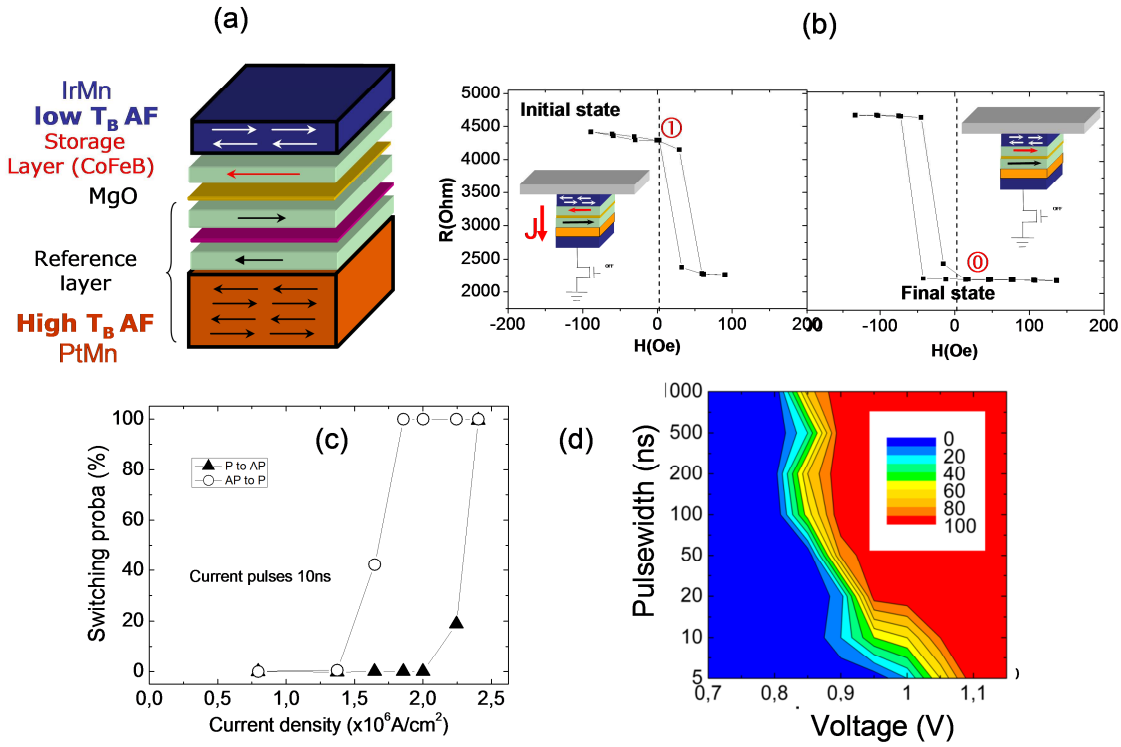

Figure 5.5: Illustration of the write scheme combining thermal assistance with spin-transfer torque. (a-b) Writing principle. Minor loops measured before (a) and after (b) applying a pulse of voltage across the MTJ of 1.1 V for 30 ns. (c) Demonstration of repeated switching between the low and high resistance state by inverting the polarity of the voltage pulse across the MTJ. (d) The probability of switching from P to AP and AP to P states.

5.3.2 Bipolar TAS

In order to use advantageously the STT effect in field driven magnetization reversal, a writing scheme has been recently proposed[65] to combine the field direction with the corresponding current direction, such that STT also favors the same final magnetization configuration, as shown in *figure 5.6a*. Depending on the heating current direction through the junction, the STT effect associated with the heating current can help or hinder the switching of the storage layer magnetization. To study the dependence of the switching field with the polarity of the injected current, field hysteresis loops have been measured **during the PhD thesis of Antoine Chavent** using constant voltage bias on the junction[6667], or by applying voltage pulses at each point along the loop[68]. Using this type of loops, it is possible to determine either the critical current for STT switching or the relationship between the injected current density and the magnetic switching field. The reported phase diagrams show that even at injected current levels below the STT critical current, we observe a reduction of the magnetic field required for switching depending on the current polarity.

65 I. L. Prejbeanu and R. Sousa, "*MRAM Cell and Method for Writing to the MRAM Cell using a Thermally Assisted Write Operation with a Reduced Field Current*," U.S. patent 20130182499, Jul. 18, 2013.

66 S. Oh, S. Park, A. Manchon, M. Chshiev, J. Han, Hyun-Woo Lee, J. Lee et al. "*Bias-voltage dependence of perpendicular spin-transfer torque in asymmetric MgO-based magnetic tunnel junctions*." Nature Physics, vol. 5, no. 12, pp. 898-902, 2009.

67 D. C. Worledge, G. Hu, David W. Abraham, J. Z. Sun, P. L. Trouilloud, J. Nowak, S. Brown, M. C. Gaidis, E. J. O'sullivan, and R. P. Robertazzi. "*Spin torque switching of perpendicular Ta/ CoFeB/ MgO-based magnetic tunnel junctions*." Appl. Phys. Lett., vol. 98, no. 2, pp. 022501, 2011.

68 L. San Emeterio Alvarez, B. Lacoste, B. Rodmacq, L. E. Nistor, M. Pakala, R. C. Sousa, and B. Dieny. "*Field-current phase diagrams of in-plane spin transfer torque memory cells with low effective magnetization storage layers*." Journ. Appl. Phys., vol. 115, no. 17, pp. 17C713, 2014.

We investigated statistically the effect of the heating current polarity on the write field values on 1kbit arrays of TAS-MRAM cells connected to bipolar selection transistors. The magnetic tunnel junction stack has a PtMn based SAF reference layer, a MgO tunnel barrier and a CoFeB/NiFe/FeMn exchange biased storage layer. The test devices used in this study are arrays of elliptical junctions of nominal size 150x300nm². The deposited stack was annealed after deposition under a magnetic field of 1T. Writing tests were performed at positive and negative current polarities at increasing the write field values until switching was obtained for every bit of the array. The writing field dependence with voltage was measured with both polarities of the injected heating current. First, all the junctions were set in the same initial state by applying, simultaneously with a heating pulse, a large external field of 200Oe – *Figure 5.6b*. Then, under an external writing field of opposite direction and increasing amplitude, a 20µs heating pulse was applied through each of the 1024 junctions of the 1kbit array.

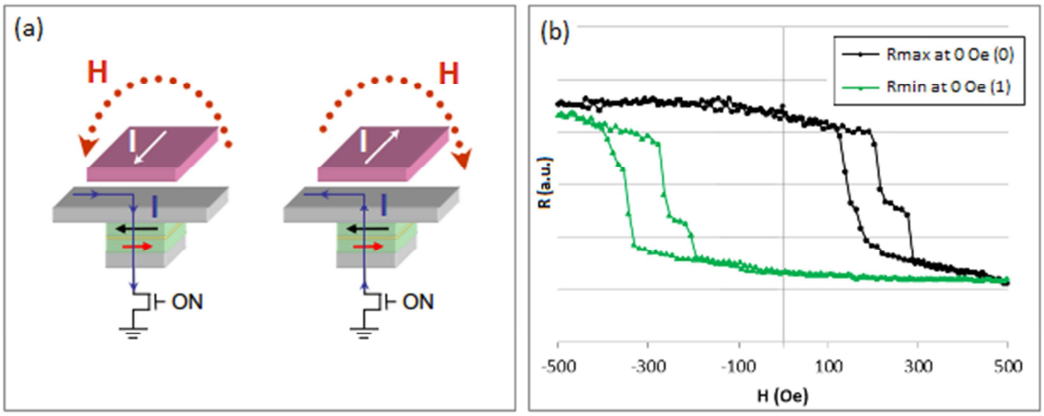

Fig.5.6: (a) Writing procedure for each state by combining the direction of the magnetic field and the polarity of the heating current in order to reduce the writing field [3]. (b) Magnetoresistance loops showing the reversal of the exchange pinning direction after applying a heating pulse with a magnetic field.

The writing test has been performed for both writing directions: from parallel to antiparallel state (P→AP) and from antiparallel to parallel state (AP→P) for positive and negative polarities. The writing results are summarized in the writing diagrams shown in *Figure 5.7a* for the AP→P switching and in Fig.5.7b for the P→AP switching. The contour lines separate regions corresponding to a given write probability: 50% - triangles, 95% - squares and 99.5% - circles. For low amplitude pulse currents (between 0.6 and 0.8mA in *Figure 5.7b*), the slope of the contour lines is steeper as they correspond to a regime where temperature induced by the heating current pulse is still below the blocking temperature of the FeMn antiferromagnet pinning the storage layer. The width of the current range required to obtain 99.5% switching at maximum field reflects essentially the dispersion in blocking temperature of the FeMn antiferromagnet. For current densities larger than 1.2MA/cm², the slope of the contour lines is reduced, approaching horizontal as the write field becomes the determining factor for successful writing. This slope however is not zero for two main reasons. First, for AP→P switching, for current densities between 1MA/cm² and 1.2MA/cm² for which the temperature raise is only slightly above the FeMn antiferromagnetic blocking temperature, the dispersion in blocking temperature determines a soft transition between pinned region and unpinned region. Second, in the unpinned region, current above 1.2MA/cm² for AP→P, the slope is due to the increased role of the thermal activation on the switching of the magnetization. When comparing the two diagrams, the slope is steeper for AP→P than P→AP for the same reason as the difference of unpinning current (0.8MA/cm² for 50% for AP→P and 1MA/cm² for 50% for P→AP): the difference of resistance of the initial state (high resistance for AP→P and low resistance for P→AP) gives rise to a temperature difference, which depends on the actual current value.

More interestingly, in this region we can observe a switching asymmetry for different pulse current polarities. For example, the mean writing field of AP→P (in *Figure 5.7a*) switching is lower with positive polarity. Such an asymmetry has previously been observed in TAS-MRAM cells (see

paragraph 3.2.1) and was attributed to a heating asymmetry, where heating is higher because the tunneling electrons energy loss occurs in the receiving electrode, which in our case is the storage layer for positive polarity. In this case the asymmetric heating cannot be distinguished from possible STT related effects, since positive polarity also favors the parallel final state. To discriminate between STT and heating asymmetry mechanisms, one must consider the P→AP switching case (*Figure 5.7b*). For P→AP switching, the mean writing field is lower for negative polarity compared to positive polarity, which in this case is not consistent simple heating asymmetry considerations. The effect could be explained by the STT effect favoring the P→AP reversal. The STT effect is observed here for a current density of 1.5 MA/cm^2, while the magnetic moment of the storage layer is 3.0x10^{-4} emu/cm². In the previous report[69], the magnetic moment of the storage layer was more than 50% larger of 4.6x10^{-4} emu/cm² whereas the heating asymmetry effect was observed for a current density of 2.2 MA/cm^2. In that case, we assumed that the larger storage layer magnetic moment masks the STT related effect, while in the present study, they become dominant because of the lower magnetic moment of the storage layer. We point out that another manifestation of STT influence associated with heating current in TAS-MRAM was the observation of steps in the switching probability versus pulse heating duration[70].

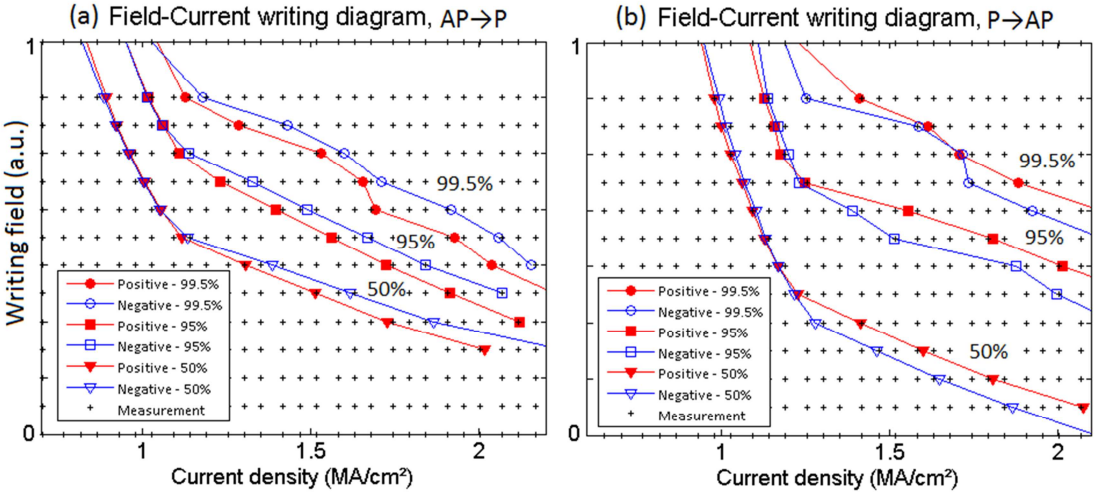

Figure 5.7: Writing diagram of a 1kbit array for three different writing rates, for both polarities of the heating current (red and blue) and for both directions of writing (P→AP and AP→P). For AP→P writing, the writing field is lower with the positive polarity whereas for P→AP writing, the writing field is lower with the negative polarity. The writing field reduction is of about 15% for a writing probability of 99.5%.

A reduction writing field in the unpinned region was evidenced by changing the polarity, which is asymmetrical with respect to the direction of writing. This is consistent with spin-transfer torque influence. The order of magnitude of the effect is in good agreement with previous work on writing field dependence with the current and compares well with numerical estimations using a Néel-Brown modified model to take into account the spin-transfer torque effect. The writing field can be reduced by 15% by advantageous polarities for a current density of 1.5MA/cm².

An estimation of the dependence of the writing field on the heating current can be made assuming a Néel-Brown model for the magnetization reversal, where the energy barrier is dependent on the field

69 E. Gapihan, J. Hérault, R. C. Sousa, Y. Dahmane, B. Dieny, L. Vila, I. L. Prejbeanu et al. "*Heating asymmetry induced by tunneling current flow in magnetic tunnel junctions*." Appl. Phys. Lett., vol. 100, no. 20, pp. 202410, 2012.

70 J. Hérault, R. C. Sousa, C. Ducruet, B. Dieny, Y. Conraux, C. Portemont, K. Mackay et al. "*Nanosecond magnetic switching of ferromagnet-antiferromagnet bilayers in thermally assisted magnetic random access memory*." Journ. Appl. Phys., vol. 106, no. 1, pp. 014505, 2009.

and also on the bias current to account for the STT contribution to the reversal. The modified energy barrier can be written as:

$$E_b = E_0\left(1-\frac{H}{H_k}\right)^a\left(1\pm\frac{I}{I_c}\right)^b \quad (5.6)$$

In *Equation 5.6*, $E_b$is the effective energy barrier and E_0 is the energy barrier in absence of external field, I_c is the critical switching current at 0K:

$$I_c = \frac{2em\alpha}{\eta\hbar}\mu_0\left(\frac{M_s}{2}+H_k-H\right) \quad (5.7)$$

And H_k is the anisotropy field at 0K. In this case, the STT related term can, from an energy point of view, be considered as an effective field ΔH:

$$E_0\left(1-\frac{H}{H_k}\right)^a = E_0\left(1-\frac{H-\Delta H}{H_k}\right)^a\left(1-\frac{I}{I_c}\right)^b \quad (5.8)$$

For $I \ll I_c$ and $\Delta H \ll H_k - H$:

$$\Delta H \approx \frac{b}{a}(H_k-H)I\frac{\eta\hbar}{\mu_0 em\alpha M_s} \quad (5.9)$$

Equation (5.9) explicitly shows the dependence of the magnetic switching field on the applied bias current, where ΔH is proportional to the current I as was previously demonstrated This equantion is valid only at currents well below the critical current and an effective field small compared to the critical field. It is important to note that the effective field is proportional to:

$$\Delta H \sim \frac{J}{tM_s{}^2} \quad (5.10)$$

Based on this relation, we can explain the writing field reduction using the switching field dependence on the STT current reported in previous works[71]. The value for the writing field dependence with pulse voltage is 50Oe/V for a 1.1nm thick CoFeB storage layer, with RA of 10Ωµm², corresponding to an STT effective field reduction of 5Oe/(MA/cm²). We can assume a saturation magnetization of 1.3x10^6 A/m for this material. The storage layer used here corresponds to a ferromagnetic material with 3nm thickness and 1x10^{6}A/m saturation magnetization by accounting for the relative contribution of CoFeB and NiFe in the storage layer. Correcting for the thickness and saturation magnetization in *equation 5.10*, the reported effect converts to 3Oe/(MA/cm²) in our case. In our samples the current density ranges from 1.3MA/cm² to2.2 MA/cm², so the actual field reduction expected is 3.9 to 6.6Oe.

In conclusion, statistical measurements of magnetization reversal were realized in thermally assisted pinned storage layer on 1kbit MRAM test devices using positive and negative current polarities.

- First, the **thermally activated nature of the reversal was confirmed by the decrease of the writing field as the current/heating is increased**.
- Second, comparing cumulative switching results for both polarities, there is a **clear effect of the current polarity on the decrease of the writing field, which is in agreement with spin transfer torque assisted switching**. When the current direction corresponds to STT favoring the same final state as field switching, there is an additional decrease of the write field, which cannot be accounted for by heating asymmetry considerations. Numerical estimations are also in good agreement with the experimental results. The reduction of the switching field was measured to be 2.5-3 Oe/(MA/cm²) for an appropriate combination of the writing field and injected current direction. **This corresponds typically to a 15% field reduction at a current density of 2MA/cm²**.

71 L. San Emeterio Alvarez, B. Lacoste, B. Rodmacq, L. E. Nistor, M. Pakala, R. C. Sousa, and B. Dieny. "*Field-current phase diagrams of in-plane spin transfer torque memory cells with low effective magnetization storage layers*." Journ. Appl. Phys., vol. 115, no. 17, pp. 17C713, 2014.

5.4 CONCLUSIONS ON TAS-STT-MRAM

We have demonstrated here a new concept of combining the memory write modes TAS and STT, STT-TA-MRAM. This memory sees its integration capacity higher although STT-RAM and TA-MRAM to target the pillars of the order of tens of nanometers. It has proved it can have the same benefits that the STT-RAM with a potentially much higher thermal stability.

The problem with the field driven writing of TAS-MRAM cells is still that the magnetic field needs to be generated by a current line with current pulses of a few mA. However, the write field does not scale with cell size and can be at best kept constant, unlike STT-MRAM where the write current scales with cell size. Alternatively, it is possible to get rid of the field line by still using the thermally assisted concept but combining it with spin transfer torque (STT) to switch an exchange biased storage layer. It is thus possible to combine the added stability obtained from the exchange biasing to retain the information with the reduction of the current through cell size scaling, since the cell switching occurs at a constant current density, typically in the 10^6A/cm² range. In order to use advantageously the STT effect in field driven magnetization reversal, a writing scheme has been recently proposed to combine the field direction with the corresponding current direction, such that STT also favors the same final magnetization configuration.

1kbit TAS-STT-MRAM prototypes were realized by the consortium including Spintec, Crocus and LETI in the framework of the ANR RAMAC project – see *Figure 5.8*.

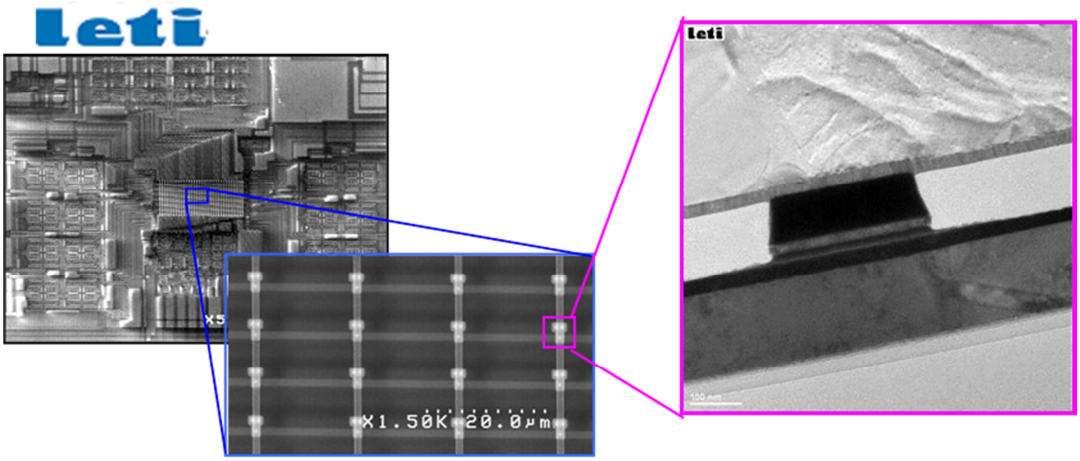

Fig.5.8: Technical realization of the 1kbit TAS-STT-MRAM prototype processed in LETI in the framework of the ANR RAMAC project

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6. ULTIMATE MRAM SCALABILITY: THERMALLY INDUCED ANISOTROPY REORIENTATION

THERMALLY INDUCED ANISOTROPY REORIENTATION (TIAR) STT-MRAM concept

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PhD THESIS

1. Sebastien Bandiera (co-supervising 33%) - R&D engineer Crocus Technology

Jonctions tunnel magnétiques à anisotropie perpendiculaire et écriture assistée thermiquement
Université Joseph-Fourier, Grenoble, Oct. 21 2011, Directeur de thèse : Bernard Dieny

6.1 MOTIVATION

MRAM has also been proposed to replace DRAM technologies below the 22nm technological node[72]. At these dimensions, it becomes increasingly difficult to achieve sufficiently large effective anisotropy with in-plane magnetized as it is necessary to fulfil the 10 years data retention criterion ($\Delta=K^{eff}V/k_BT>70$).

In order to solve this problem, i.e. to push further the superparamagnetic limit and to increase the spin-torque efficiency, it was also proposed[73] to use stacks having perpendicular-to-plane magnetization. Indeed, such materials present high effective anisotropy, up to a few 10^7erg.cm^{-3}, which potentially allows decreasing the devices lateral size below 22nm. In that case, no antiferromagnet is required, since the intrinsic effective anisotropy of the ferromagnetic material is large enough to match the 10 years data retention criterion. Such materials have already proved their efficiency to increase the storage density for hard disk drive technologies[74]. Moreover, it is useful to use this kind of material when current induced switching is used. Indeed, out-of-plane magnetization allows decreasing the write power consumption compared to in-plane magnetization when the free layer is switched by spin transfer torque[75]. **In perpendicular MTJ, the current density for switching could be significantly reduced because the two terms present in the expression of the critical current density partially cancel each other.** However, with perpendicular MTJ, current density of the order of 1 to 3x10^{6}A/cm^2 were obtained, values of the same order of magnitude than the low record values obtained for in-plane switching (~2x10^{6}A/cm2)[76]. These large values are probably related to an increase value of the Gilbert damping for the material with perpendicular anisotropy. A promising route to circumvent the issue of large damping in out-of-plane magnetized materials consists in using storage layer where the perpendicular anisotropy does not arise from a bulk contribution as in (Co/Pd) or (Co/Pt) multilayers or as in FePt ordered alloys but from a large interfacial perpendicular anisotropy which exists at the interface between the magnetic electrode and the tunnel barrier[77]. This interfacial anisotropy makes it possible to pull out-of-plane the magnetization of materials having low Gilbert damping such as CoFeB alloys (α_{CoFeB}~0.01 to be compared with $\alpha_{(Co/Pd)}$~0.2 and $\alpha_{(Co/Pt)}$~0.4[78]). Using the interfacial anisotropy therefore makes it possible to achieve simultaneously large perpendicular anisotropy required for high thermal stability of the magnetization and the weak Gilbert damping required for low switching current density.

The downsize scalability of this perpendicular STT-MRAM may however be limited by the total current required to write the memory while maintaining a sufficient thermal stability. For technological nodes below 22nm, it becomes increasingly difficult to achieve sufficiently large effective anisotropy with in-plane magnetized as it is necessary to fulfil the 10 years data retention criterion. In order to solve this, perpendicular magnetic anisotropy is of great interest. However, current induced switching still present some issues which deteriorate the reliability of the devices.

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- First, since the magnetization of the free layer is collinear to the spin polarization of the current in the initial state, **a thermal fluctuation is required to initiate the reversal of the free layer by STT, leading to a stochastic switching.**
- In addition, since the switching current is proportional to the effective anisotropy K^{eff} of the free layer, **a dilemma has to be addressed: the decrease of the lateral dimensions of the device requires an increase of K^{eff} to maintain sufficient thermal stability. However, this increase in K^{eff} also yields higher write current and correlatively larger power consumption.** This leads to a decrease of reliability since higher writing voltage reduces the existing margin to the breakdown voltage.

In order to solve these issues some assistance methods have been proposed, such as electric field [79], adding an orthogonal polarizer[80], or thermal assistance[81]. The idea is to decrease the anisotropy of the free layer under writing conditions, either by electric field or heating, so that it becomes easier to switch the junction either by field or spin transfer torque. By disconnecting the anisotropy requirements under stand-by and writing conditions, it becomes possible to scale down to the 22nm technological node limit. Electric assistance is very appealing for technological applications since it has been shown that the writing consumption can be decreased by several orders of magnitude. Moreover, unipolar switching has been demonstrated in this type of devices, simplifying the writing procedure [54][82]. However, in order to obtain significant assistance, a few tens kΩμm² barrier is required, leading to long time reading procedures, which are not desirable.

One significant realization towards high density memory cells has been to assist the spin transfer switching of the magnetization of the perpendicular cell. This was achieved by a thermally induced reorientation of the free layer magnetic anisotropy from out-of-plane to in-plane. The junction temperature increase is due to the Joule dissipation around the tunnel barrier produced by the same pulse of current which generates the spin transfer torque. It allows the spin transfer torque efficiency to be maximized during write, since the spin polarization of the current is perpendicular to the magnetization of the storage layer. This reduces the STT switching current and suppresses stochastic variations in switching time. This thermal assistance scheme was demonstrated in a MRAM cell designing a magnetic electrode coupled to a Co/Pd multilayer having a strong temperature dependence of the perpendicular anisotropy, leading to a temperature at which the magnetization reorientation in-plane occurs can be adjusted between 90 and 250°C by varying the Co thickness in the 0.2- 0.4nm range. These cells showed thermal stability factors of $162k_BT$ for a critical current density of 4.6MA/cm², a record write efficiency at that time. **<u>These studies have been done during the PhD thesis of Sebastien Bandiera.</u>**

6.2 WORKING PRINCIPLE

The efficiency of thermally assisted switching has already been demonstrated for Heat Assisted Magnetic Recording (HAMR)[83]. **This effect can be implemented easily in the case of magnetic tunnel junction by advantageously using the heat produced by the current injected in the junction to provide STT**. In that case, the MTJ resistance is compatible with fast read/write

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procedures. In such devices, the writing consumption either by field or STT can be greatly reduced. **Ultimately, thermally induced anisotropy reorientation (TIAR)[84] can be used to assist the spin transfer torque switching in perpendicular magnetic tunnel junctions. The TIAR provides a way to reorient the direction of the free layer magnetization with heating.** Indeed, the magnetization of an out-of-plane magnetized layer at room temperature can reorient in the thin film plane when heated due to the different temperature dependence of the out-of-plane anisotropy and demagnetizing energy[85].

TIAR assisted switching consists in optimizing the temperature dependence of the MTJ magnetic properties to decrease the STT critical current while keeping a satisfying thermal stability under standby conditions. In this latter case, the current is responsible of three phenomena: STT, heating, and TIAR. Such a switching method is very promising to achieve highly scalable MRAM cells with low power consumption and reliable writing.

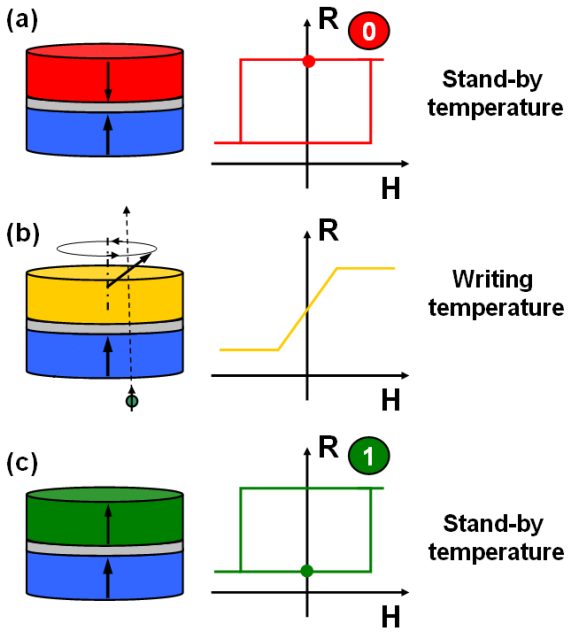

Figure 6.1: Principle of TIAR assisted switching: (a) the junction exhibits a large PMA at stand-by temperature. (b) A current is sent through the junction. The FL magnetization undergoes a TIAR due to the heating. The STT induces a large angle precessional motion of the FL magnetization and pulls it upwards or downwards depending on the current direction. (c) The FL recovers its PMA during the cooling when the current is gradually decreased to zero. Its magnetization rotates out-of-plane in the direction corresponding to the hemisphere in which it was pulled in by STT.

Figure 6.1 presents schematically the proposed writing scheme. During write, a current pulse is sent through the junction. Due to the inelastic relaxation of tunnelling electrons, heating occurs so that the PMA decreases. As a result, the free layer magnetization falls in the film plane at a critical temperature (T_K) while the reference layer is engineered so as to keep its out-of-plane magnetization. This latter electrode polarizes the current in the out-of-plane direction. The STT, due to this spin-polarized current, pulls the FL magnetization in the upper or lower hemispheres depending on the current direction and induces large angle out-of-plane precessions[86]. In such a configuration, the STT effect is highest since the spin polarization is almost perpendicular to the magnetization. It results in a more reliable switching since no thermal fluctuations are required to initiate the reversal. The injected current is then gradually decreased so that the junction cools down while STT is still effective. The free layer recovers its PMA, and its magnetization gets reoriented out-of-plane, in the direction defined by the hemisphere in which it was previously pulled in by STT. This switching approach reduces the write consumption as soon as the required current to heat the junction up to the anisotropy reorientation temperature T_K is lower than the critical switching current in a standard MTJ (typically a few 10^6A/cm^2).

In addition, as already explained in Chapter 3, the heating current density can be further reduced by adding in-stack thermal barriers on both sides of the MTJ. One should notice that heating is always occurring when a current is injected in a MTJ during writing. This heating assists STT switching, but

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materials used in MTJ are usually not optimized to use advantageously this effect. Oppositely, TIAR assisted switching consists in optimizing the temperature dependence of the MTJ magnetic properties to decrease the STT critical current while keeping a satisfying thermal stability under stand-by conditions. In that latter case, the current is responsible of three phenomena: STT, heating, and TIAR.

The voltage required to switch the junction is mainly determined by the anisotropy reorientation temperature T_K, which sets the lower limit of the writing window. T_K can be estimated theoretically by calculating K^{eff} as a function of temperature. For a cubic or uniaxial anisotropy, it can be written at first order[87] as:

$$K(T) = K_{\perp}(0)\left(\frac{M_s(T)}{M_s(0)}\right)^m - (N_{perp} - N_{plan})2\pi M_s(T)^2 \qquad (6.1)$$

where $K_{\perp}(0)$ is the perpendicular magnetic anisotropy constant at 0K, $M_S(T)$ the free layer magnetization, and $-(N_{perp}-N_{plan})2\pi M_S(T)^2$ the demagnetizing energy, N_{perp} and N_{plan} being the demagnetizing factors of the pillar. The exponent m depends on the origin of the PMA. For a single ion anisotropy, $m=i(i+1)/2$, where i denotes the anisotropy constant order, being equal to 2 at first order in most of case. From this equation, it is straightforward that K^{eff} sign changes beyond T_K, T_K being the temperature at which $K^{eff}=0$. In that situation, the in-plane anisotropy induced by the demagnetizing energy becomes higher than the PMA, and the free layer magnetization falls in the thin film plane.

In order to tune T_K, *equation (6.1)* shows that the evolution of M_S as a function of T has to be controlled. This can be achieved by tuning the Curie temperature T_C of the magnetic material. *(Co/NM)* multilayers, where *NM* is a non-magnetic metal, provide a wide range of T_C, and present *PMA* when *NM* is a noble metal such as Pt, Pd or Au[88]. In those systems, the T_C can be easily tuned by changing the *Co* or *NM* thickness, or by doping Co with Ni or non-magnetic elements[89].

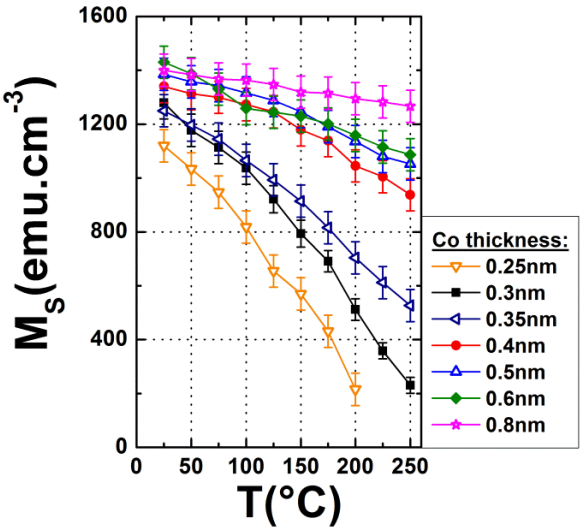

Fig. 6.2: Evolution of the magnetization of (Co tCo / Pd 1.2) multilayers as a function of the temperature for different Co thickness tCo.

This new writing scheme takes advantage of an elegant solution proposed to overcome the data retention/low consumption dilemma, and is a way to design high density and low power consumption MRAM cells below the 22nm technological node.

6.3 PROOF OF CONCEPT

Figure 6.2 illustrates such a T_C temperature control by adjusting the magnetic thickness. The magnetization of $(Pd1.2/Co\text{-}t_{Co})x5$ (thickness in nm) multilayers has been measured as a function of the temperature for different Co thicknesses t_{Co}. This figure clearly shows a decrease of the Curie temperature when the t_{Co} thickness decreases: interface Co atoms present a reduced coordination

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number compared to Co atoms, leading to an overall decrease of the exchange stiffness between magnetic atoms. Since the Curie temperature is directly related to the exchange stiffness, thin Co layers present a reduced T_C compared to bulk Co. Curie temperature can thus be tuned by adjusting the ratio of interface and volume Co atoms in the multilayer, i.e. the thickness of the Co layers. The decrease of the overall exchange stiffness can also be obtained by decreasing the RKKY coupling strength through the non-magnetic spacer, or by adding impurities in the Co layer.

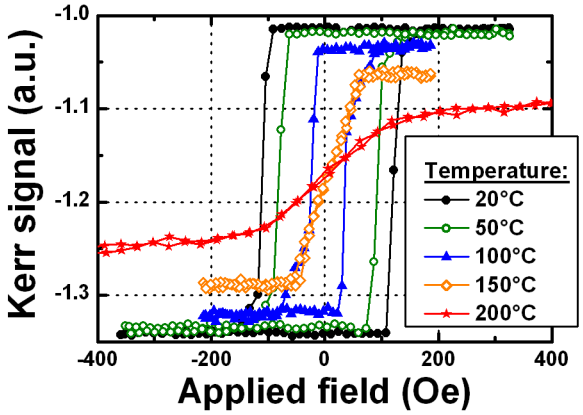

Fig. 6.3: Hysteresis loops of CoFeB1.5 / (Pd1.2/Co0.3)x3/Pd 2 as a function of the temperature with out-of-plane applied field.

However such multilayers are not suitable for MRAM applications which requires high TMR ratio. Indeed, (Co/NM) multilayers present an fcc(111) texture which does not match the bcc(001) MgO texture[90]. In magnetic tunnel junctions, it results in low TMR, which is not acceptable for high density MRAM. This problem can be solved by inserting a thin CoFeB layer at the MgO interface: the (Co/NM) multilayer provides the PMA and pulls the CoFeB magnetization out of plane while the CoFeB layer provides the appropriate texture in order to obtain large TMR ratio [91]. In such structures, TIAR can still be obtained by tuning the (Co/NM) multilayer properties.

Figure 6.3 presents the TIAR phenomenon of a MgO / CoFeB1.5 / (Pd1.2 / Co0.3)x3 (thickness in nm) multilayer. On this figure, hysteresis loops have been measured on a full sheet sample by polar magneto-optical Kerr effect as a function of the temperature, with an out-of-plane applied field. At room temperature, the loops present square and coercive behavior, indicating out-of-plane magnetization.

When the temperature increases, the coercivity decreases while the signal amplitude decreases due to the decrease of magnetization. At 150°C, perpendicular domains appear, leading to a loop with no remanence. The anisotropy reorientation occurs at 175(±20)°C. Above this temperature, the loops exhibit the reversible linear behaviour expected from a measurement

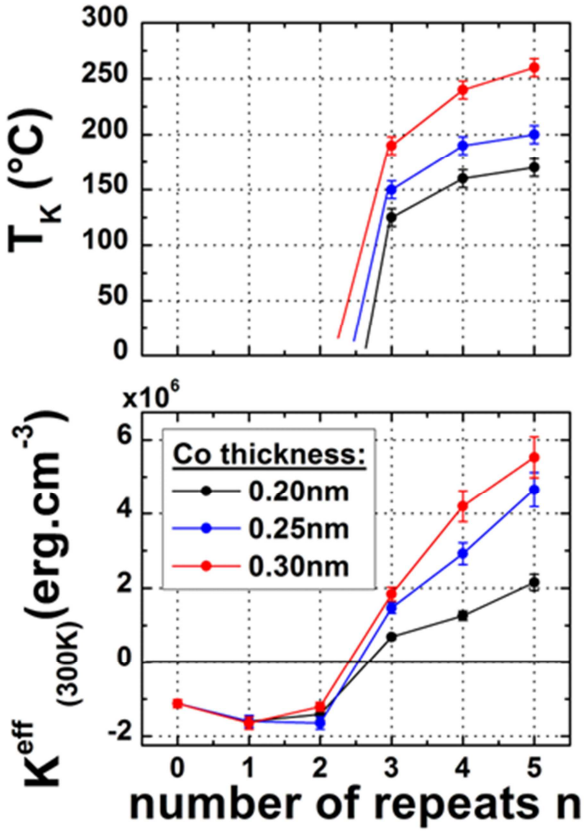

Fig. 6.4: Evolution of the reorientation temperature TK (a) and the effective anisotropy Keff (b) at room temperature of CoFeB 1.5 / (Pd 1.2 / Co tCo)xn as a function of the Co thickness tCo and the number or (Co/Pd) repeats n.

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along the hard axis direction. When the sample is cooled down, the loop recovers its squareness and coercivity, indicating that the TIAR phenomenon is reversible. In such systems, T_K is tuned by adapting the Curie temperature of the (Co/Pd)xn multilayer and the anisotropy of the stack at 300K.

Figure 6.4 shows the evolution of T_K and K(300K) measured on full sheet samples as a function of the Co thickness and the number of the (Co/Pd) multilayer repeat n. By increasing the Co thickness, the Curie temperature of the (Co/Pd) multilayer increases, resulting in higher T_K values. By increasing the number of repeat n, $K_\perp(0)$ is increased, increasing T_K as well. One can see on this graph that T_K can be tuned with these two parameters, allowing to access different applications depending on the operating temperature window.

For the reference electrode, a (Co/Pt) based synthetic antiferromagnet (SAF) has been developed. Such a SAF is important for MRAM technologies, since they create a reduced stray field on the storage layer magnetization thus avoiding different thermal stabilities Δ in the P and AP magnetic configurations as well as asymmetric P to AP and AP to P write currents[92]. Two (Co/Pt) multilayers are antiferromagnetically coupled through a Ru spacer, leading to reduced stray fields on patterned devices. The reference layer is designed to present TIAR at a temperature much higher than the writing temperature. Indeed, that electrode has to remain stable and out-of-plane magnetized under both stand-by and writing conditions.

The developed MTJ consists thus of a seed layer/SAF/MgO/FL/capping, with FL comprising 0.3nm thick Co layers and 3 (Co/Pd) repeats. The samples are subsequently annealed under vacuum at 250°C for 10min. The transition temperature T_K of the free layer in such a stack is equal to 175(±20)°C. CIPT measurements yield an *RA* product of 25Ω.µm² and a TMR ratio of 20%. The samples were then patterned into circular nanopillars with 110nm diameter using e-beam lithography and ion milling processing. When the junction is patterned, the coercive field of the free layer greatly increases from 115 to 1300Oe at room temperature, as can be seen on *Figure 6.5*, at 0V. The thermal stability of such a junction can be estimated by measuring the probability of switching as a function of applied field. For this purpose, the switching field distribution is extracted from 100 successive hysteresis loop measurements. The corresponding switching probability p_{SW} is then fitted to an expression extracted from the Néel-Brown model[93].

$$p_{sw} = \frac{f_0}{R} exp\left(-\frac{E_B(H)}{k_B T}\right) exp\left(-\frac{f_0}{R}\int_0^H exp\left(-\frac{E_B(H)}{k_B T}\right) dh\right) \quad (6.2)$$

with:

$$\mathrm{E_B(H)} = \Delta \mathrm{k_B T}\left(1 - \frac{\mathrm{H - H_{dip}}}{\mathrm{H_K}}\right)^2 \quad (6.3)$$

where f_0 is the attempt frequency (close to 1 GHz), k_B the Boltzmann constant, R the sweeping field rate, and E_B the field dependent energy barrier. H, H_{dip}, and H_K, respectively, represent the applied field, the dipolar field arising from the reference layer, and the anisotropy field.

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93 Yuasa S and Djayaprawira D D 2007 J. Phys. D : Appl. Phys. 40 R337

Using *equations (6.2) and (6.3)* to fit our data yields a thermal stability factor Δ of 167(±4) and an anisotropy field of 1950(±30)Oe at room temperature. This anisotropy field yields to $K^{eff}=1.3(\pm0.3)x10^{6}$ $erg.cm^{-3}$ on the pillar, while it was equal to $2.0(\pm0.2)x10^{6} erg.cm^{-3}$ on the full sheet sample. This decrease is probably related to damages at the edges during the junction patterning, but could be reduced by optimizing the etch process. For this value of K^{eff}, the criterion $\Delta=70$ is fulfilled down to a diameter of 36(±3)nm. At 85°C, K^{eff} is reduced to $K^{eff}=9.0(\pm1.8)x10^{5} erg.cm^{-3}$ on the pillars, the criterion $\Delta=70$ is fulfilled down to a diameter of 50(±4)nm.

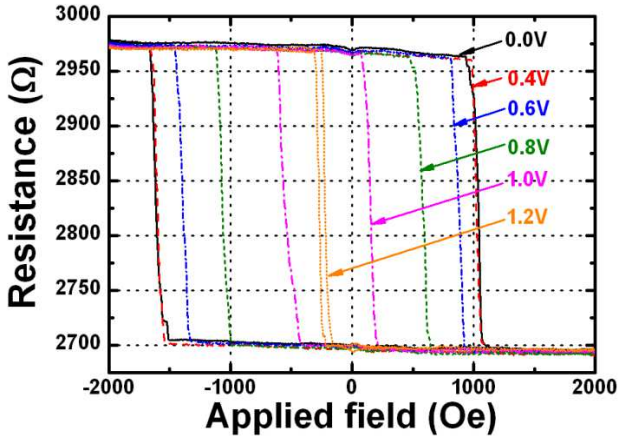

Fig. 6.5: Average of 100 hysteresis loops measured on a 110nm diameter pillar. 30ns long pulses of increasing voltage are applied at each field step. The resistance is measured after cooling.

In order to study the effect of heating, the hysteresis loops were then measured while applying 30ns long pulses of square shape of increasing voltage at each field step (2Oe), the resistance of the junction being measured after each pulse. The average of 100 loops measured with this method is plotted on *figure 6.5*. The most striking effect of the electrical pulse is to drastically decrease the FL switching field for both P to AP and AP to P transitions. Indeed, in order to achieve reliable field writing without heating pulse, a mean field of 1400 Oe has to be applied whereas only60 Oe is necessary with 1.2V pulses (the shift of the loop being subtracted). It is noticeable that above 1.1 V, AP to P and P to AP reversals occur in the same field range, indicating that the temperature in the MTJ under this voltage is higher than T_K. Since 100 loops are averaged, the remaining coercivity observed for the 1.2V loop is only due to the averaged field reversal distribution caused by thermal fluctuations. This data therefore clearly demonstrate the benefit of the TIAR for field writing in perpendicular MTJ. However, for high density MRAM, STT writing offers much better downsize scalability.

Figure 6.6 presents the switching phase diagram. The red colour denotes the region where the antiparallel state is stable, the blue one denotes the region where the parallel state is stable, and the green one denotes the bistable region. One can note that there is a 100Oe wide field window in which both P and AP region exist. This means that the junction can be switched in both directions by TIAR assisted STT at constant applied magnetic field. The switching field window is centered on -350Oe. This region is not centered on zero field due to residual stray fields arising from the reference layer. With 30ns long pulses, the switching voltage is 1.15(±0.05)V, corresponding to a current density of $j_w=4.6x10^{6} A/cm^{-2}$. This current is in the same order than the values reported in the literature using a standard Ta/CoFeB/MgO free layer and no writing assistance. However, in order to calculate the switching efficiency, the ratio j_w/Δ gives a better idea of the writing efficiency. *Table 6.1* gives a comparison between the standard current induced switching and the TIAR assisted switching.

Ref.	Material	jw (MA/cm²)	Δ(300K)	jw/Δ (MA/cm²)
[94]	Ta/CoFeB/MgO	3,8	43	0,09
[95]	Ta/CoFeB/MgO	7,4	50	0,15
[96]	CoFeB/(Pd/Co)	4,6	73	0,06

94 Ikeda S, Miura K, Yamamoto H, Mizunuma K, Gan H D, Endo M, Kanai S, Hayakawa J, Matsukura F and Ohno H 2010 Nature Mater. 9 721

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Table 6.1: comparison of writing current densities at 30ns jw, thermal stability factor Δ at 300K for 40nm large devices and efficiency jw/Δ of standard STT switching (Refs. 94, 95) and TIAR assisted STT switching (Ref 96).

This table shows reported write current densities corresponding to 30ns long pulses. The thermal stability at 300K given here is calculated for a d=40nm diameter junction. Note that:

(i) Δ (40nm) is directly measured in ref 94, 95 and extrapolated from the data at d=110nm for ref 96, assuming an identical K^{eff} at 40nm and macrospin reversal at this dimension,

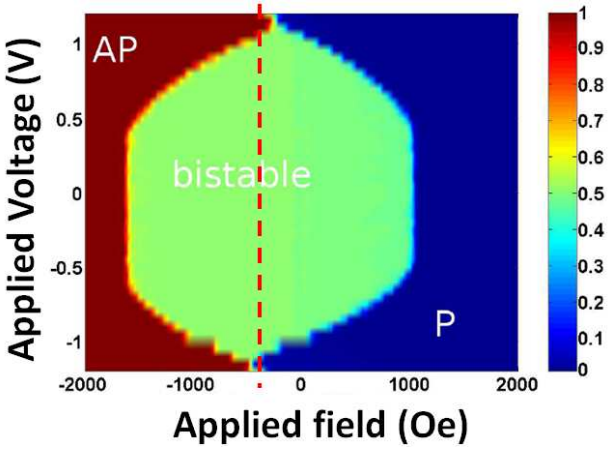


Figure 6.6: Phase diagram of a 110 nm diameter pillar with 30ns long applied pulses. The dashed red line denotes the centre of the TIAR assisted current induced switching window.

(ii) jw at 30ns is extrapolated from long pulse measurements for ref 94, and directly measured in ref 95 and 96

(iii) we assume that the writing current depends mainly on the heating in ref 96, and is thus not decreased when the dimensions are shrink down, which is a worst case.

Under these assumptions, it is clear that TIAR assisted STT switching present an improved efficiency compared to the standard STT switching. This is even more striking regarding the damping α of the different kind of FL: whereas it is equal to 0.013 to 0.03 in a Ta/CoFeB/MgO stack, it is of about 0.15 in a CoFeB/(Pd/Co) stack[97]. The efficiency of the TIAR assisted STT writing could be further optimized by implementing thermal barriers in the stack. It has been shown that with this kind of barriers, a temperature of about 200°C can be obtained with an RA product of about 30Ω.µm² and a current density of about $1x10^{6}A.cm^{-2}$[98].

Moreover, the writing field windows could be broadened by tuning the shape of the pulse during cooling: indeed the STT effect is proportional to j² while the heating is proportional to j. This would allow pulling the FL magnetization in the writing direction when it recovers its PMA during cooling, even under field or thermal fluctuations. The STT pulse shape influence has to be further investigated in future writing tests. The thermal stability Δ at operating temperature could be enhanced, keeping a constant writing consumption by controlling T_K, leading to even more scalable MTJ. Finally, decreasing the MTJ dimensions would also lead to an increased stability since it would reduce the in-plane demagnetizing energy, thus resulting in a higher effective anisotropy.

To summarize, we demonstrate here the efficiency of TIAR assisted STT switching. **This new writing scheme takes advantage of an elegant solution proposed to overcome the data retention/low consumption dilemma, and is a way to design high density and low power consumption MRAM cells below the 22nm technological node.**

96 Bandiera S, Sousa R C, Marins de Castro M, Ducruet C, Portemont C, Auffret S, Vila L, Prejbeanu I L, Rodmacq B and Dieny B 2011 Appl. Phys. Lett. 99 202507

97 Sajitha E P, Walowski J, Watanabe D, Mizukami S, Wu F, Naganuma H, Oogane M, Ando Y and Miyazaki T 2010 IEEE Trans. Magn. 46 2056

98 Gapihan E, Sousa R C, Hérault J, Papusoi C, Delaye M-T, Dieny B, Prejbeanu I L, Ducruet C, Portemont C, Mackay K and Nozières J-P 2010 IEEE Trans. Magn. 46 2486 ; Lombard L., Gapihan E, Sousa R C, Dahmane Y, Portemont C, Ducruet C, Conraux Y, Papusoi C, Prejbeanu I L, Nozières J-P, Dieny B and Schuhl A 2010 J. Appl. Phys. 107 09D728

6.4 CONCLUSIONS ON TIAR-STT-MRAM

MRAM has been proposed to replace DRAM technologies below the 22nm technological node. In order to solve this problem, i.e. to push further the superparamagnetic limit and to increase the spin-torque efficiency, it was also proposed to use stacks having perpendicular-to-plane magnetization. In perpendicular MTJ, the current density for switching could be significantly reduced because the two terms present in the expression of the critical current density partially cancel each other. The downsize scalability of this perpendicular STT-MRAM may however be limited by the total current required to write the memory while maintaining a sufficient thermal stability. One significant realization towards high density memory cells has been to assist the spin transfer switching of the magnetization of the perpendicular cell. This was achieved by a thermally induced reorientation of the free layer magnetic anisotropy from out-of-plane to in-plane. This effect can be implemented easily in the case of magnetic tunnel junction by advantageously using the heat produced by the current injected in the junction to provide STT. In such devices, the writing consumption either by field or STT can be greatly reduced. Ultimately, thermally induced anisotropy reorientation (TIAR) can be used to assist the spin transfer torque switching in perpendicular magnetic tunnel junctions. The TIAR provides a way to reorient the direction of the free layer magnetization with heating.

TIAR assisted switching consists in optimizing the temperature dependence of the MTJ magnetic properties to decrease the STT critical current while keeping a satisfying thermal stability under standby conditions. This new writing scheme takes advantage of an elegant solution proposed to overcome the data retention/low consumption dilemma, and is a way to design high density and low power consumption MRAM cells below the 22nm technological node.

7. GENERAL CONCLUSIONS

MRAM technologies evolved in the last years, benefiting from the progress in spintronics research, namely the tunnel magnetoresistance of MgO magnetic tunnel junctions, the spin transfer torque and the spin orbit torque phenomena. Between 1996 and 2004, most research and development focused on MRAM written by field. These approaches actually resulted in the commercialization of the first MRAM products by Freescale Semiconductor and its spin-off Everspin Technologies in 2006. Field-written technology is robust and is already used in a variety of applications where reliability, endurance, and resistance to radiation are important features, such as in automotive and space applications. However, the down-size scalability provided by field-writing in conventional technology is limited to MTJ dimensions on the order of 60nm×120nm due to electromigration in the conducting lines used to generate the field. In addition, in field-writing, the write field extends all along the conducting line where it is produced and decreases relatively gradually in space, inversely proportional to the distance to this line. As a result, unselected bits adjacent to selected bits may sense a significant fraction of the write field, which may yield accidental switching of these unselected bits.

An extension of the initial field written MRAM is the Thermally Assisted MRAM (TAS-MRAM), mainly developed by Crocus Technology. This basic concept can be used either with in-plane magnetized MTJ by using an exchange biased storage layer or with out-of-plane magnetized MTJ by taking advantage of the thermal variation of the perpendicular anisotropy in the storage layer. This technology is already patented by Spintec and implemented by Crocus Technology for larger features (>130nm), but process control and research on materials is still needed to take the technology to sub-20nm dimensions.

Demonstration of thermally assisted writing in MRAM with exchange biased storage layer

In TAS-MRAM, the write selectivity is achieved by a combination of temporary heating of the selected cell produced by the tunneling current flowing through the cell and a single pulse of magnetic field. The reference layer is designed so that its magnetic properties almost do not vary in the temperature operating range. In contrast, the storage layer is designed so that its magnetic switching is greatly eased when its temperature is increased to the write temperature – typically in the range 150-250°C. The power consumption to write these memory elements is significantly reduced compared to conventional field-written MRAM thanks to the possibility of using lower magnetic fields and of sharing each field pulse among several cells so as to write several bits at once. In TAS-MRAM, smaller dimensions can be reached thanks to the field sharing approach, the lower required amplitude of the write field, and the different mechanism of write selectivity.

The TAS approach has multiple advantages and solves the limitations of the conventional MRAM architecture:

- As the selection at write is temperature-driven, the addressing errors are strongly reduced.
- Only one magnetic field is required to write, leading to reduced power consumption Furthermore, the write power can be further reduced, by using circular elements with no shape anisotropy.
- The exchange bias anisotropy of the storage layer ensures a good thermal stability of the information.
- Since the system is not anymore bistable at zero field due to the exchange bias, TAS provides good reliability under field disturbance. Indeed, even if the resistance state of a bit is modified by external parasitic fields under standby conditions, the resistance state after the field perturbation goes back to its initial state.
- TAS-MRAM presents a good scalability since the heating power density P required to heat the junction is proportional to the square of the current density

The principle behind the heat generation in a MTJ structure is a combination of the Joule heating in the metallic electrodes and of the inelastic scattering of tunneling hot electrons arriving in the receiving electrode after their ballistic tunneling across the tunnel barrier. The direction of the tunneling current in magnetic tunnel junctions can have a significant influence in the final temperature profile within the MTJ as there is an asymmetry in the heating depending on the polarity of the write pulses (flow direction).

In *TAS-MRAM*, the total duration of the write cycle is determined by the heating and cooling dynamics and the speed at which cells can be re-written after an initial write. We have shown that the heating and cooling times can be indeed competitive, for a total write cycle time on the order of 30 ns

One way to increase the heating efficiency and reduce the power density is to insert low thermal conductivity materials at both ends of the magnetic tunnel junction stack. Another possibility to reduce the write power density is the use of AF materials with lower Néel temperature.

Field writing combined with thermal assistance is also advantageous in terms of power consumption in MRAM chips by offering the possibility to share the pulse of magnetic field among numerous bits.

The variation of the thickness of the ferromagnetic storage layer led, because of the competition between dipolar and exchange energies, to the observation of two different mechanisms of magnetization reversal. For this reason, the F layer in the storage layer has to be sufficiently thin to avoid multidomain states. Another possibility for reducing exchange variability is the use of synthetic antiferromagnets instead of simple F layers. The reduced dipolar field would stabilize the magnetization state at remanence and reduce the detrimental dipolar coupling with the AF layer, which showed to induce an increase of grain instability during magnetization reversal.

For applicative purposes, in order to reduce instabilities and increase dots magnetic properties reproducibility and reliability, grain size distribution has to be homogenized in order to reduce the variability of grain population from dot to dot.

The possibility of increasing the blocking temperature in ultrathin AF layers and of enhancing the exchange bias field is of technological interest for TAS-MRAM applications, in particular for the retention and writing properties of the storage layer. This kind of trilayer structures is an excellent candidate to improve storage layer performances and reliability in TAS-MRAM. The combination of trilayer stack and Cu dusting layer, for 4 nm IrMn layer, led to 300% enhancement of exchange bias field at room temperature.

If the TAS-MRAM approach offers clear improvements, it nevertheless has its own constraints:

- the operating temperature range is limited to temperatures compatible with stability of the AF of the storage layer.
- the writing method of the TAS-MRAM is based on the possibility to heat the junction to unlock the storage layer, without affecting the stability of the reference layer. The functionality of this approach is largely influenced by the choice of materials and their AF blocking temperatures.
- The AF grain size distribution has important consequences since each grain volume will match a particular T_B. The idea of a single T_B should be then replaced by a blocking temperature distribution.
- Moreover, the initial procedure to determine statically the temperature range by temperature dependent statical VSM measurements was reconsidered after studies showing the dependence of the blocking temperature with the heating pulsewidth.

The thermally assisted approach offers a promising solution for the next generation of MRAM as it can solve most of the current issues: write selectivity, power consumption and thermal stability, whilst offering scalability to 65 nm node. Crocus Technology in collaboration with TowerJazz has produced functional 1 and 4 Mbit demonstrators using this technology in 130nm technology. These demonstrators are addressing namely shortcomings of Battery-backed SRAM solutions,

Demonstration of the self-reference dipolar writing

In addition to TAS-RAM, a new concept named Self-Reference, which is at the heart of Magnetic Logic Unit (MLU) architecture, has been proposed and developed. SR goes much further in resolving additional challenges and enabling new functionalities and capabilities. The key feature of the SR MTJ is that it does not require a fixed reference layer. This is achieved by removing the antiferromagnetic layer that pins the reference. As a result, the magnetization of this layer is free to vary and is renamed as the sense layer. The reading is performed in two steps: the SR magnetization is set in a first direction, and the MTJ resistance is measured. The SR magnetization is then switched to the opposite direction and the new resistance is measured. The resistance variation between the two measurements yields the magnetic orientation of the storage layer. In this approach, the read cycle is longer (~50ns) but the tolerance to process variation is greatly enhanced. Indeed, for the standard reading scheme, the two resistance state distributions have to be well separated in order to avoid reading errors. This implies good dot size and shape control. In contrast, for the SR reading scheme, the difference of resistance between the two states is used to read the junction, and is thus not sensitive to dot size variation. This is particularly useful for small technological nodes where it becomes increasingly difficult to control accurately the resistance distributions.

The SR memory cell operates differently from the standard fixed reference TAS memory cell. The mechanism of writing data into the memory cell in *SR-TAS-MRAM* and *TAS-MRAM* configurations is identical: A small current flows through the MTJ and heats the cell to the critical write temperature while applying a magnetic field to orient the storage layer. Then, the MTJ is cooled while write field is maintained, essentially "freezing" the magnetic state into the storage layer. Heating current was optimized by including thermal barrier inside and around the MTJ.

In order to optimize the read and write field requirements, we developed a macrospin model based on the Stoner-Wohlfarth model of magnetization reversal. By introducing magnetostatic, RKKY and ferromagnet / antiferromagnet exchange coupling phenomena, we calculated a general form of the energy for any type of MRAM magnetic stack.

Several improvements to MLUs have been investigated i) a decrease in the write field amplitude obtained thanks to a new write procedure which uses the sense layer as a local amplifier of the write field; ii) an increase in the storage capacity achieved in MLU thanks to multibit recording either in single domain state or in vortex state. A previously proposed highly efficient switching mode, relying on the magnetostatic interactions between the sense and the storage layer, was effectively predicted by the model and experimentally demonstrated in new samples. An excellent agreement was obtained between the model and the experimental results. Increasing the stiffness of the storage layer was found to be critical in order to minimize the read field requirements at decreasing patterning dimensions. Material developments were performed to maximize the RKKY coupling in the synthetic ferrimagnet storage layer.

Based on the model developed, we built a roadmap describing the magnetic stack to use, that allows a downscaling of the self-referenced MRAM down to 45 nm while conserving manageable field requirements. Due to fundamental limitations in field-induced switching MRAM technology, reaching higher densities was found to require increasing the individual storage capacity of each MTJ, i.e. storing multiple bits per unit cell.

A new angle-based storage method taking advantage of the sense layer free magnetization was investigated. Using the magnetic model developed previously, suitable samples were designed and allowed to experimentally demonstrate up to 4 bits per single MTJ. The field requirements were however found to be substantially higher than those compatible with a fully functional product. A new write method, predicted by the model, was investigated and exploited in the building of a second roadmap down to 45 nm.

1kbit prototypes were used to evaluate the proof of concept and the efficiency of the SR-TAS-MRAM. With significant advantages over other field-switched MRAM technologies and a wide range of

alternative applications, SR-MRAM magnetic stacks could constitute major industrial and commercial stakes for Crocus Technology.

The SR read not only enables a very robust memory cell but also allows it to be used as a logic element. Direction of the current flowing in the field line can be used as an information input. The resistance of the cell now compares the stored information and the input information - if sense and storage layers are aligned in parallel the resistance is low and if sense and storage layers are anti-parallel the resistance is high. The element acts as an XOR (exclusive OR) logic device whose output depends on the comparison of the stored information and an input information (via the field line).

Starting from MLU concept, Crocus has developed an innovative function called Match-In-Place, to authenticate users without exposing any confidential data to a security attacker. Each cell of the Match-In-Place architecture is a non-volatile memory cell combined with the virtual XOR gate of the MLU. Multiple cells are connected in series to form a NAND chain acting as a linear Match-In-Place engine. If multiple Match-In-Place NAND chains are placed in parallel, they can act in the same time to compare one pattern against many. Fields of use of this new architecture are quite wide and include secure microcontrollers, biometric devices and associative memory devices.

The MLU technology has been developed as a platform technology that serves as a base for multiple products, from magnetic sensors, to memories, to security products.

Self-reference TAS MRAM enables a number of previously unachievable breakthroughs in magnetic technology implementation, including ultra-sensitive magnetic sensors, highly robust secure embedded memory, ultra-high-temperature non-volatile memory (NVM) operation (e.g., ~200° C), order-of-magnitude higher density hardware-based table searches (e.g., content addressable memory), high density multi-bit storage, and scaling to sub-20nm manufacturing. The DTAP technology enables unique differential programming of sensors devices that leads to improved performance.

Due the possibility to program both magnetic layers individually, self-referenced MRAM can be operated as a Magnetic Logic Unit, combining in-stack the storage and exclusive-or logic functions and thereby opening new application ranges. Due to its characteristics, SR-MRAM appears as a technological solution for high-density storage and other applications like associative storage and authentication device.

Demonstration of combined Thermally STT assisted writing in MRAM with exchange biased storage layer

The problem with the field driven writing of TAS-MRAM cells is still that the magnetic field needs to be generated by a current line with current pulses of a few mA. However, the write field does not scale with cell size and can be at best kept constant, unlike STT-MRAM where the write current scales with cell size. Alternatively, it is possible to get rid of the field line by still using the thermally assisted concept but combining it with spin transfer torque (STT) to switch an exchange biased storage layer. It is thus possible to combine the added stability obtained from the exchange biasing to retain the information with the reduction of the current through cell size scaling, since the cell switching occurs at a constant current density, typically in the 10^6A/cm² range. In order to use advantageously the STT effect in field driven magnetization reversal, a writing scheme has been recently proposed to combine the field direction with the corresponding current direction, such that STT also favors the same final magnetization configuration.

We have demonstrated here a new concept of combining the memory write modes TAS and STT, STT-TA-MRAM. This memory sees its integration capacity higher although STT-RAM and TA-MRAM to target the pillars of the order of tens of nanometers. It has proved it can have the same benefits that the STT-RAM with a potentially much higher thermal stability.

In order to use advantageously the STT effect in field driven magnetization reversal, a writing scheme proposing to combine the field direction with the corresponding current direction, such that STT also favors the same final magnetization configuration. Depending on the current direction through the junction, the STT effect associated with the heating current can help or hinder the switching of the storage layer magnetization. Statistical measurements of magnetization reversal realized on 1kbit TAS-MRAM test devices using positive and negative current polarities confirmed first the thermally activated nature of the reversal by the decrease of the writing field as the current/heating is increased and second, have shown a clear effect of the current polarity on the decrease of the writing field, in agreement with spin transfer torque assisted switching.

Demonstration of combined Thermally STT assisted writing in MRAM with perpendicular magnetization

MRAM has also been proposed to replace DRAM technologies below the 22nm technological node. In order to solve this problem, i.e. to push further the superparamagnetic limit and to increase the spin-torque efficiency, it was also proposed to use stacks having perpendicular-to-plane magnetization. In perpendicular MTJ, the current density for switching could be significantly reduced because the two terms present in the expression of the critical current density partially cancel each other. The downsize scalability of this perpendicular STT-MRAM may however be limited by the total current required to write the memory while maintaining a sufficient thermal stability. One significant realization towards high density memory cells has been to assist the spin transfer switching of the magnetization of the perpendicular cell. This was achieved by a thermally induced reorientation of the free layer magnetic anisotropy from out-of-plane to in-plane. This effect can be implemented easily in the case of magnetic tunnel junction by advantageously using the heat produced by the current injected in the junction to provide STT. In such devices, the writing consumption either by field or STT can be greatly reduced. Ultimately, thermally induced anisotropy reorientation (TIAR) can be used to assist the spin transfer torque switching in perpendicular magnetic tunnel junctions. The TIAR provides a way to reorient the direction of the free layer magnetization with heating.

TIAR assisted switching consists in optimizing the temperature dependence of the MTJ magnetic properties to decrease the STT critical current while keeping a satisfying thermal stability under standby conditions. This new writing scheme takes advantage of an elegant solution proposed to overcome the data retention/low consumption dilemma, and is a way to design high density and low power consumption MRAM cells below the 22nm technological node.

PART II

8. PERSPECTIVES – FUTURE PROJECTS

My future projects are closely related to Spintec primary targets for the next 5 years :

1. **Pursue leading-edge research in all area of spintronics,** from existing topics (e.g. spin de-pendent transport, spin dynamics, magnetic tunnel junctions,...) to emerging and unchartered territories (graphene spintronics, magnetic oxides, spin caloritronics, skyrmions and whatever may emerge in the future…). The objective here will not only be "excellence", as monitored by publications and international recognition, but also to "replenish the shelves" with new concepts, ideas, materials, etc. that may ultimately feed novel applicative projects. This works implies the convergence of theory, modeling and experimental work on materials and characterization . All can and must be done in-house in order to generate a strong and clean IP ;
2. **Choose the most promising applicative area**, whether from the expressed needs of the industry or from our own vision, and propose new and/or improved concepts for devices fulfilling a significant step forward with respect to existing solution. The objective here is to demonstrate the viability of the idea, and test the major parametrics, through "proof-of-concepts" structures that mimic real devices operations but do not have to be neither at the scale nor with all the peripherals that a product would have. All this should be preferably done in-house for IP purposes. Partnerships if requested must remain at the university level, the objective being to generate key cornerstone patents.
3. **Define a few key projects with a large potential market "value"** and push the development all the way to demonstrators at the device or system level. This implies combining experimental work, circuit design, as well as silicon implementation (e.g. clean room technology). This will require key partnerships to be established, with institutions having complementary skillset both in terms of resources (e.g. state-of-the-art materials, pilot line(s), real-life testing) and knowledge (chemists and materials scientists, process technologists, system-level designers, applications engineers, …). The ultimate objective will be to build up a coherent patent portfolio, which can later be valued through partnerships with existing corporation or through start-ups spin-off.

To reach these goals, Spintec must continue its metamorphosis from a « proof-of-concepts » laboratory, whereupon research is limited to proposing new concepts, materials, devices, and demonstrating the viability of the approach in a simple test structure with a low Technology Readiness Level (TRL), to a « demonstrators » laboratory whereupon the innovation is carried all the way to its implementation into a real-life environment with an intermediate / high TRL.

- **For memories, this means more than just a single cell demonstrating read and write parametrics. A small test chip (say 1kbit) with simplified I/O's, write drivers and sense amps, if not for full built-in test and error correction codes that would exist in a real chip, is mandatory;**
- **For sensors this implies the sensing element together with its driving electronics, even non optimized, in order to address the Signal-to-noise Ratio, which is the only relevant parameter of such devices ;**
- **For logic this means implementing the proposed chip into real, leading edge, silicon (e.g. .CMOS), fully tested, rather than simulated-only solutions.**

My scientific project for the forthcoming years are mainly related to the targets (2) and (3), more precisely being dedicated to applied aspects of the magnetic tunnel junctions for: sub-20nm scalable MRAMs, hybrid logical circuits and innovative magnetic field sensors.

8.1 SUB-20NM SCALABLE, LOW POWER MRAMS

As underlined by the ENIAC 2020 vision, our technologically-oriented society is moving steadily towards a new era of *'ambient intelligence'*, where distributed intelligent systems help to process, understand and utilize the plethora of digital information that pervades our everyday life. Since intelligence cannot exist without memory, logic, sensors and communication technologies it is clear that ultra-low power, fast and high density nanoelectronics devices of the future have a key role to play. Particularly, one major focus of ICT applications is on the future generation of technologies in which very large amounts of memory will be integrated into everyday environment, especially in portable applications, with strict power and size limitations. For instance a laptop motherboard has a power consumption of about 300mW during idle time. Of this energy, 60% are used to refresh DRAM, while just fewer than 40% are used for cache memory (SRAM). The CPU (for instance using Intel PowerGating Technology [99]consumes in idle mode only less than 1% [100] (see *Figures 8.1, 8.2*). Given that many mobile device are idle most of the time, these facts make a **low power memory device a paradigm shifting development that is pursued by major players in the memory market in the US** (Intel, Micron, HGST, etc.) and Asia (Samsung, Toshiba, NEC, etc.).

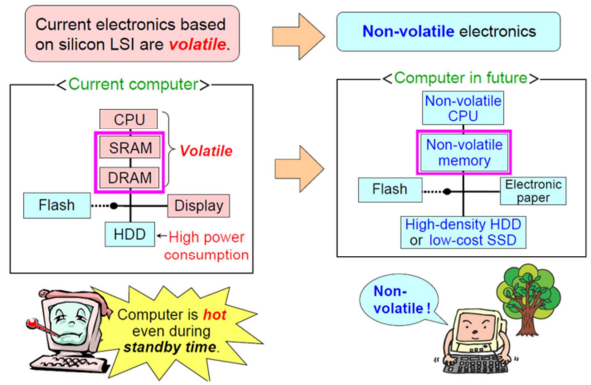


Figure 8.1: Integration of non-volatility in the future computers. Adapted from 101

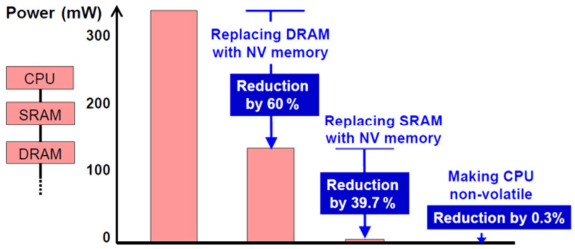


Figure 8.2: Graphical depiction of the memory consumption of a laptop motherboard. Adapted from 102

Power consumption has also become a crucial issue for mass storage in server applications that enable the storage and distribution of huge volumes of digital information. For example, the combined power consumption of the data centers in the US amount to 100 billion kWh per year, which is a percent of the total energy consumption. Overall the IT power consumption is expected to increase by a factor 10 between 2005 and 2025 with a total power consumption of 5 trillion kWh making IT a major player of electrical energy consumption (15%) (see *Figure 8.3*). To put this in perspective, it accounts for roughly the same amount of energy consumption as the whole of mobility (cars, planes, trains, etc.) showing the relevance of the field.

99 L.C. Yeo et al., "*Dynamic Power Gating Implementation*" White Paper Intel; http://www.intel.de/content/www/de/de/intelligent-systems/intel-embedded-media-and-graphics-driver/emgd-dynamic-power-gating-paper.html]

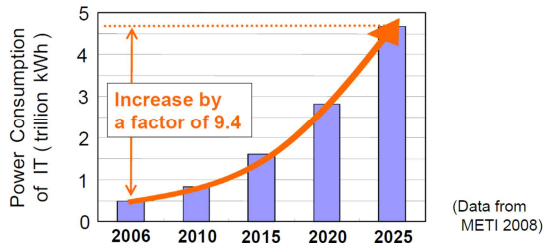
100 GreenIT promotion council presentation at the 14th world electronics forum, New Delhi]

101 (http://nanospin.agh.edu.pl/wp-content/uploads/T_Stobiecki_PM_14.pdf)

102 (http://nanospin.agh.edu.pl/wp-content/uploads/T_Stobiecki_PM_14.pdf).

Given these numbers, there is a clear case for reducing power consumption in IT devices, which will be the goal of my future projects.

The first goal is to **strengthen the STT-MRAM technology at sub-20nm nodes**, by **solving the two aforementioned remaining difficulties** in STT-MRAM development at very advanced technology nodes (<20nm) (etching of MTJ stacks and retention) thus opening the path towards very high density integration in STT-MRAM.



In 2025, global power consumption of IT appliances is expected to reach 4.6 trillion kWh. This corresponds to 15% of global power generation (6% of total energy consumption in the world).

Figure 8.3 Overall global power consumption of IT appliances by 2025 [From GreenIT Promotion Council of the Japan Electronics and Information Technology Industries Association http://www.jeita.or.jp/english/index.html].

The second goal is **to explore all possibilities and advantages of the ultra-low power MTJ-based multifunctionality for portable applications and Internet of Things (IoT).**

STT-MRAMs have a unique set of qualities that no other technology of non-volatile memories (NVM) gathers:

i) switching speed in the range 100ps-10ns,
ii) DRAM compatible density,
iii) cyclability up to 10^{16}cycles.

As a result, STT-MRAMs appear as a unique possible candidate for DRAM or SRAM L3 replacement which is the main objective of companies such as Samsung, Micron, Intel etc. However, embedded STT-MRAM are likely to first appear at relaxed dimensions (~45nm-30nm) due to two remaining difficulties

1. **Ensuring thermal stability of the magnetization (i.e. memory retention) up to 100°C for 10 years at sub-20nm node.**
2. **etching of these magnetic stacks at very small dimensions**

I propose to tackle the first point by 2 different approaches that will be described in the next paragraphs: electric field control assisted STT-MRAMs and perpendicular shape anisotropy STT-MRAMs

8.1.1 Electric field control EFE-STT-MRAMs

(in collaboration with Hélène Béa)

The main encountered limitation for the use and densification of STT-MRAMs is the large currents still necessary for controlling magnetization direction and thus switching the device. These large currents are flowing through the tunnel barrier of the MTJ to exploit STT effect that can switch the magnetization (STT writing). It thus leads to large power consumption that becomes critical at low device sizes, and that also brings endurance problems of the MTJs due to the large electrical stress applied on the ultrathin oxide tunnel barrier. The magnetic energy barrier to switch the magnetization of a magnetic element can be expressed as $E_b=KV$, where K is the magnetic anisotropy and V is the volume of the element. In order to provide thermal stability for 10 years data retention, the requirement is that $E_b \sim 80 k_B T$ in Gb size elements. As a result, the magnetic anisotropy has to increase when the bit size scales down, which leads in STT-RAM devices to higher switching current at smaller technological nodes. In general, the energy currently needed to switch a <100 nm-scale element under STT is about a few pJ and is dominated by ohmic losses of the charge current flowing. However, the magnetic energy needed to switch a magnetic element (100x100x10nm^3) having 10 year data

retention at room temperature is only in the range of fJ showing that fundamentally there is scope for an improvement in the switching efficiency by a factor 1000[103], [104].

A novel solution enabling the development of ultra-low power spintronic devices is emerging, based on electric field gating. Electric fields can be sustained without current flow and for the generation only the charging energy of the effective capacitance is needed. Along this line it has been shown that assistance by an electric field may reduce the STT writing critical currents in MTJs[105].This can be explained by an electrically reduced magnetic anisotropy which leads to lower energy barrier that is easier to overcome for changing magnetization direction. In principle, voltage control spintronic devices could have much lower power consumption than their current-controlled counterparts provided they can operate at sufficiently low voltage (typically below 1V). **This makes Electric Field gating the most important development for a paradigm shift in manipulating magnetization with ultimate efficiency.**

In order to circumvent this classical dilemma in data storage between the memory writability and its retention, EFE seems to be the most promising route (see values in *Table 8.1*). The general principle of using EFE is based on EFE induced reduction and/or reorientation of the magnetic anisotropy leading either to lower energy barrier that is easier to overcome for instance with magnetic field or STT or to full switching without any additional assistance.

	Production processes			In development	
Technology	SRAM	DRAM	NOR Flash	STT-RAM	EFE-MRAM
Energy/bit (fJ)	100	1000	10^6	100	<10
Write speed (ns)	1	20	1000	1–10	1–10
Read speed (ns)	1	30	10	1–10	1–10
Density (area in F^2)	>30	6–10	4–8	10–30	4–8
Endurance (cycles)	Very High	Very High	Low	Very High	Very High
Non-volatile	No	No	Yes	Yes	Yes
Standby power	Leakage Current	Refresh Current	None	None	None
Cost overhead versus CMOS	Large area (6T)	Separate process	Separate process	Back-end (BEOL) process	Back-end (BEOL) process
Non-volatile logic capability	No	No	No	Very limited due to power	Yes

Table 8.1. *Comparison of existing non-spintronic and emerging spintronic memory technologies, highlighting STT-RAM and EFE-RAM (voltage-controlled switching). Adapted from KL Wang et al, J. Phys. D: Appl. Phys. 46 (2013) 074003*

Recently it has been shown that assistance by an electric field through charge modulation in the dielectric barrier may slightly reduce the STT writing critical currents in MTJs[106]. The possibility of an electrical STT magnetization switching is related to the reduction of anisotropy barrier induced by the EFE, which in turn reduces the current density needed for switching by STT. For the electric field assistance to be efficient, the magnetic anisotropy of the pillar has to be very small, close to zero, to have a sizeable effect and possible electric field assisted writing. However this implies that for small pillars, the retention time is decreased, which is a problem for typical sizes of MTJs (<45nm) in MRAM. Also the anisotropy may strongly vary in temperature and the assistance may be inefficient several tens of degrees above room temperature, which can occur during operation. In order to overcome these problems, we will optimize the design of the free layer of MTJs with PMA and the properties of the tunnel barrier (RA product) to tailor the EFE induced variation of anisotropy that fulfill industrial requirements for both operating temperature range and thermal stability. We will also

103 K. L. Wang et al., J. Phys D: Appl. Phys. 46, 074003 (2013),

104 D. E. Nikonov et al., Journal of Superconductivity and Novel Magnetism 19, 497 (2006)]

105 W.G. Wang et al., Nat. Mater., 11, 64 (2012)

106 W.-G. Wang et al. Nature Materials 11,64 (2012)

investigate the possibility to develop STT-RAM devices that incorporate piezoelectric layers to assist the switching by strain induced anisotropy variations.

In order to overcome these problems, we will optimize the design of the free layer of MTJs with PMA and the properties of the tunnel barrier (RA product) to tailor the EFE induced variation of anisotropy that fulfill industrial requirements for both operating temperature range and thermal stability.

8.1.2 Perpendicular shape anisotropy (PSA) STT– MRAM

(in collaboration with Bernard Dieny, Ricardo Sousa)

Most of the STT-MRAM development efforts are nowadays focused on out-of-plane magnetized MTJ taking advantage of the perpendicular magnetic anisotropy (PMA) arising at magnetic metal/oxide interface[107,108], a phenomenon discovered at Spintec in 2002. This interfacial anisotropy allows conciliating large anisotropy required to insure a sufficient retention of the memory together with low switching current density thanks to weak spin-orbit coupling[109]. However this PMA is too weak to insure 10 year retention up to 100°C in sub-20nm devices. **For deeply sub-20nm nodes, new materials with large bulk PMA and low damping still have to be found**. Furthermore, because this PMA is an interfacial effect, it is **very sensitive** to the structural and chemical properties of the magnetic metal/MgO interfaces contributing to **dot to dot variability**.

To solve these problems in very small feature size STT-MRAM, we propose a totally novel approach. It consists in using MTJ stacks in which the storage layer **anisotropy is uniquely controlled by its out-of-plane shape anisotropy** i.e. by giving the storage layer a cylindrical shape with large enough aspect ratio (thickness/diameter typically >1)[110]. In such structure, for purely magnetostatic reasons, the storage layer magnetization lies out-of-plane. This innovative approach has several advantages:

It provides a **very robust source of PMA**, much less sensitive to defects than the interfacial PMA;

ii) it makes possible the use of materials with low damping such as Permalloy or **Heusler alloys**

it provides a **scalable approach** since the same material can be used at all sub-20nm nodes thus removing the need to find new materials with higher anisotropy at each technological node. **Thermal assistance** provided by the Joule heating around the tunnel barrier due to the write current can also be further used to assist the STT switching and reduce the write voltage.

To develop these novels **PSA-MRAM** (Perpendicular Shape Anisotropy-MRAM), different tasks will be carried out:

- Micromagnetic simulations will be performed to investigate the micromagnetic equilibrium states and STT switching dynamics of these thick out-of-plane magnetized storage layers, taking into account the combined influence of magnetostatic demagnetizing effects, magnetostatic interactions with the reference layer, magnetostatic interactions with the neighboring cells, perpendicular anisotropy at magnetic metal/oxide interface and possibly Dzyaloshinskii-Moriya (DM) interactions which may exist at the storage layer interface opposite to the MgO barrier. These simulations will allow us to evaluate the height/diameter aspect ratio that the storage layer must have to insure the desired cell retention, the influence of the micromagnetic distortions (deviations from single domain behavior) on the thermal stability factor, the relationship between STT switching speed and write current/voltage, the requirement on the control of the cells diameter to reach an acceptable variability in terms of

107 S.Ikeda et al, Nat.Mat.9, 721 (2010).

108 S.Monso, B.Rodmacq, S.Auffret, G.Casali, B.Gilles, P.Boyer and B.Dieny, Applied-Physics-Letters. 80, 4157 (2002).

109 B. Dieny et al, Proceedings of the Electron Devices Meeting (IEDM), 2011 IEEE International, 1.3.1

110 K. Metlov and YP. Lee, Appl.Phys.Lett.92, 112506 (2008)

retention (typically >10years for DRAM applications, minutes or seconds for SRAM applications) and write current/voltage (write voltage RI_{write} typically 0.45±0.03V for 1Gbit chip).

- Optimize the stack in terms of low Gilbert damping (directly proportional to the write current density) and TMR amplitude. Composite storage layer of the form CoFeB/Ta 0.2nm/NiFe will be used as well as based on Heusler alloys. The guidelines that we will follow are: use of low damping materials (NiFe, Heusler), bcc structure next to the MgO interface, B attracted away from the MgO interface upon anneal.
- In order to benchmark the properties of these PSA STT-MRAM against conventional perpendicular STT-MRAM, testchips with MTJ diameters in the range 100nm-10nm will be fabricated and tested. Particular attention will be put on retention, switching current/switching speed, variability. These results will be compared with those obtained on standard p-STT-MRAM.

8.1.3 Novel approaches to sub-20nm patterning of MTJ stacks

(in collaboration with Olivier Joubert / LTM & Bernard Dieny & Ricardo Sousa)

Sub-40nm patterning of spintronics materials and particularly MTJ remains the **main challenge** for spintronic circuits involving very small magnetic elements such as STT-MRAM. Lot of reactive ion etching (RIE) recipes were tried but failed to deliver satisfactory results due to the complexity of MTJ stacks. Ion beam etching (IBE) is still the preferred approach[111] but is difficult to implement on large wafers, yields large dot to dot variability and drift in operating conditions[112].

To **circumvent this etching problem**, we want to investigate totally new approaches for nanostructuring MTJs. It consists in **depositing the MTJ stack on conducting pillars** which have been prepatterned in the form of posts with overhanging insulated side walls. This approach was previously used with success at Spintec to make patterned media for hard disk drives (HDD)[113]. We propose to adapt it to STT-MRAM. By depositing the MTJ stack on the pre-patterned pillars, **the material gets naturally patterned during its deposition** thus **not requiring any post-deposition patterning**. One can then **play with the incidences of deposition** to create beneficial **lateral gradients of thickness or composition at the scale of each pillar**. After deposition of the MTJ stack, the trenches are filled with an insulating material (it can be a planarizing resist subsequently backed), the top contacts are opened by chemical mechanical polishing (CMP) followed by the patterning of the top electrodes.

We will take advantage of the fact that the MTJ deposition is performed on prepatterned posts to induce specific properties which will reduce the dot to dot variability. In particular, by creating a lateral MgO thickness gradient, the **current can be focused** at the center of each nanopatterned MTJ thus reducing the influence of possible edge defects. Similarly, lateral gradient of chemical composition can be induced in the storage or reference layers. Such gradient can be used to induce different properties at the edges and center of each dot in order for instance to reduce demagnetizing or nucleation effects at edges. Thus by playing with the incidence of deposition of the various layers constituting the MTJ stack, we will **minimize the role of edge defects** and thereby **reduce variability**

111 M. Gajek et al, Appl.Phys.Lett.100, 132408 (2012)

112 http://www.memorystrategies.com/report/emerging/mram.htm

113 S. Landis, B. Rodmacq, B. Dieny, Physical Review B, 62, 12271 (2000).

8.2 MTJ BASED MAGNETIC FIELD SENSORS

Spintec was originally heavily involved in read heads for disk drive, yet this activity all but vanished due to the strong consolidation of the industry, now with only two players (Seagate and WD), each with strong internal R&D capabilities. Meanwhile, the magnetic sensors market, driven by smartphones and other handheld devices, is booming with a need for low-cost multiple functions solutions (e.g. lately 9-axes MEMS devices combining an accelerometer, a gyroscope and a magnetic sensor).

Spintec has recently decided to rejuvenate an activity on sensors by pursuing new innovative concepts:

1. **A monolithic 3-D positioning sensor**, with the promised benefits of a cheap(er) manufacturing process and a simplified driving electronics. This sensor is to be deployed in consumer applications (e.g. cell phones).
2. **A high sensitivity / low noise magnetic field sensors**, combining a technology patented by Orléans University and Spintec's STT-driven noise reduction scheme. This sensor is to be first deployed in spatial environments, and could later be extended to health monitoring applications.

Magnetic field sensors are used in a wide range of applications: orientation sensors, linear and angular encoders, medical imaging (MRI), non-destructive control, current sensing, HDD read-out. Except heads for HDD which use TMR, the other sensors are not based on spintronic phenomena but rather on Hall effect, giant magneto-impedance, or field-induced variation of susceptibility of soft magnetic material (fluxgate). In this context, magnetic tunnel junctions (MTJ) based sensors may become highly competitive. MTJs are already used as field sensors working around a few 100 MHz in hard-disk drive read-heads and could be used as low magnetic field sensors for many other applications. MTJ based sensors have been essentially developed for read heads where the reduction of size requires high sensitive sensors. **However, their implementation at other large scale production has been delayed by technological issues like linearity, hysteresis free sensors, immunity against strong perturbations and integration with CMOS electronics.** The highest demand of this kind of sensors is driven by consumer desire for integrated compass devices as well in medical applications, mainly biochips, biomagnetism and MRI but there are a large number of potential applications in magnetic imaging like nondestructive evaluation.

We will propose several new innovative concepts for magnetic sensors, including 3D magnetic sensors, EFE tunable magnetic sensors and domain wall based magnetic sensors.

8.2.1 3D magnetic sensors

(in collaboration with Philippe Sabon & Bernard Dieny)

Various attempts to make **higher sensitivity 2D or 3D vectorial measurements of field (B_x, B_y, B_z) using giant magnetoresistive (GMR) sensors or TMR sensors** have been made. They were technologically complex and hardly integrable for various reasons[114]. The orientation sensors nowadays implemented in smart-phones consist of 3 independent GMR sensors assembled in 3 orthogonal directions by heterogeneous integration (soldering).

We intend to develop various schemes for 2D and 3D integrable magnetic field sensors based on low noise TMR materials.

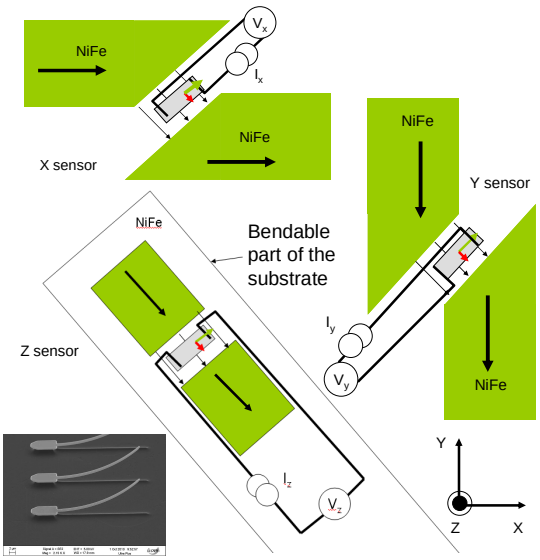


Figure 8.5 3D magnetic field sensors wherein the 3 field-components are sensed by the three identical GMR or TMR sensors. Thanks to specially designed flux concentrator, the X and Y components of the magnetic flux are rotated clockwise and anticlockwise by 45° towards the sensor. The Z-sensor is deposited on a bendable strap of the substrate bent after fabrication of the z-sensor. This part is released by etching of a sacrificial layer and bents spontaneously out-of-plane due to the internal strain.

In an approach proposed and patented at Spintec in 2014, all B_x, B_y, B_z-sensors are fabricated and biased in the same technology steps. Our "trick" is instead of having differently biased sensors for each field-component, to use **magnetic flux concentrators to deflect** the various components of the field to be sensed towards the MTJ sensors, the latter being exactly the same for the three components of the field. The concept is explained in *Figure 8.5*. Compared to the state of the art orientation sensors, the present sensors would be much more compact (50x smaller volume), more sensitive thanks to larger TMR than GMR amplitude (5x), have much reduced cost and be integrated with digital and communication function using the same baseline technology. Such sensors would be very useful for **portable applications (orientation in space), robotics, medical instrumentation** etc.

8.2.2 Tunable sensors

(in collaboration with Hélène Béa & Claire Baraduc)

In the case of magnetic field sensors based on magnetic tunnel junctions, the two magnetic layers of the junction usually have perpendicular magnetizations. One layer has its magnetization pinned, it is called the reference layer, while magnetization of the other layer may vary when a magnetic field is applied, and this is the active or the free layer. Application of a magnetic field along the hard axis of the active layer will induce rotation of its magnetization with no hysteresis. Due to TMR effect, this gives a linear variation of the junction resistance, which can be used to measure

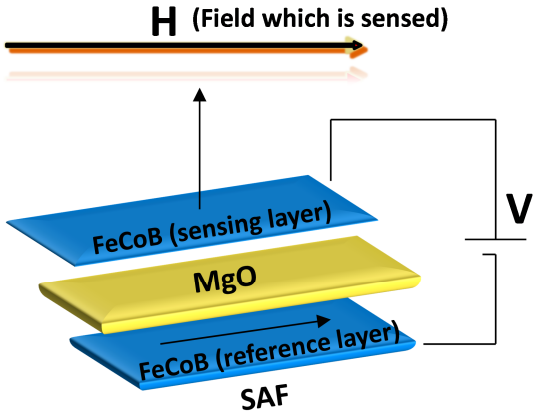


Figure 8.6 Basic principle of the functioning of the tunable magnetic sensors

114 US2008/169807 ; US2009/027048 ; WO2011/092406A1

the applied magnetic field. The range of linear behavior and the sensitivity to magnetic field are proportional to magnetic anisotropy.

Voltage controlled modification of magnetic anisotropy could be also applied in magnetic sensors to tune the sensitivity and the linear operating range, as these parameters are dependent on the magnetic anisotropy of the sensing layer. There are various issues to be addressed in realizing this type of sensor. Once optimized, this sensor could have tremendous applications in industry and could serve to reduce the cost and size of the sensing devices and would thus replace several fixed range ones with a single auto-range sensor. Usually for the in-plane MTJ based sensors, the magnetic field sensitivity is around 2%/Oe with a linear range around +/-50Oe[115]. In in-plane magnetized MTJs (initially optimized for MRAM with spin transfer torque writing), Kim et al.[116] have also shown, in the sensing mode, a tunability of the sensitivity and field range due to spin transfer torque by applying DC voltage combined with voltage pulse. In this study, when changing the DC voltage, the sensitivity varies between around 1%/Oe and 4%/Oe and the sensing field region with constant width (20Oe) is shifted from -50Oe to 100Oe. This sensor works with the field detection along the easy axis thanks to zero coercivity, which is unusual and difficult to obtain. Moreover, in this sensor, the field range is not centered at zero, contrary to what we propose.

In this project, we aim at fabricating a sensor that could detect both positive and negative fields. By choosing 90° alignment of the in-plane reference with the out-of-plane active layer (*figure 8.7*), we take advantage of the linear response of the sensor. Development of MTJs with out-of-plane active layer for sensing applications gave lower fixed sensitivities around 0.6%/Oe in the field range +/-25Oe[117]. In these structures, there is also the possibility to tune sensitivity and to symmetrically vary the field range, either by changing the thickness of the sense layer or by the EFE (electric field control). In fact, when the sensing layer magnetization is out-of-plane, the magnetic anisotropy strongly depends on the layer thickness. So the field at which the rotation of the free layer magnetization is complete, may reach large values (up to at least 1T). For instance, Wisniowski et al. have shown that a sensitivity between 0.0045%/Oe and 3.8%/Oe could be obtained depending on the CoFeB thickness[118]. In these sensors, the linear field range could thus reach large values in order to detect much larger fields than usual. However, the EFE is still not very large as it changes the sensitivity and linear field range by a factor of two only[119]. Besides the sensitivity obtained up till now in the structures presenting significant EFE is rather low due to a small TMR ratio at low bias. Therefore optimization of these structures is required to improve the sensitivity and to be able to change the detectable field range on a wider scale.

Our project aims at understanding and optimizing the structures and materials in order to optimize the functionality of the device by playing on spin transfer torque, Joule heating, resistance x area product (RA) in MTJ based voltage tunable sensors. The three main objectives are the following:

1. To optimize the RA of the MgO barrier and the thickness of CoFeB layer to make it more sensitive to the electric field and less to other effects such as STT or Joule heating.
2. To understand the role of domain walls and their contribution to TMR signal and magnetic noise.
3. To fabricate MTJs with optimized parameters, calibrate them for different applied voltages, measure sensitivity and noise and compare with usual fixed sensitivity sensors.
4. Finally, we will try to achieve a voltage tunable 2D sensor using on the same device two types of MTJs with two perpendicular in-plane reference layers.

115 J.P. Valadeiro et al., IEEE Trans Mag 51, 4400204 (2015)
116 S.I. Kim et al., J. Phys. D Appl. Phys., 47, 445004 (2014)
117 T. Takenaga et al., IEEE Trans. Mag., 49, 3878 (2013)
118 P. Wisniowski et al., IEEE Trans. Mag, 48, 3840 (2012)
119 P. Wisniowski et al., Appl. Phys. Lett., 105, 082404 (2014)

8.2.3 Domain wall based magnetic sensors

(in collaboration with Olivier Boulle & Gilles Gaudin)

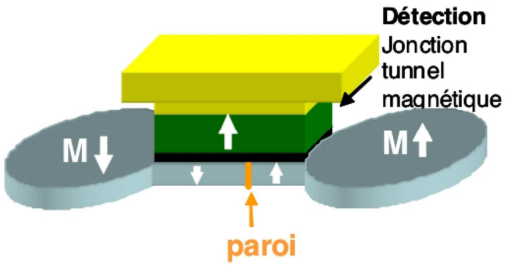


Figure 8.7 Basic principle of the functioning of the perpendicular domain wall based magnetic sensors

Magnetic sensors have invested most of our objects of common use: cars, smartphones, tablets, joystick, ... and their applications become more diversified every day. Among them, real-time spatial recognition, such as GPS assistance in a closed environment, generates a growing interest in the industrial sector. It is based on the use of a fast sensor. This fast sensor requires high sensitivity which decreases integration time. Our aim will be to achieve such perpendicular magnetic sensor with high sensitivity. The concept is based on the displacement of magnetic domain walls in a controlled and reproducible manner, and their electrical detection – see *figure 8.7*. Both aspects are now made possible thanks to recent developments in the laboratory in the field of magnetic tunnel junctions with perpendicular magnetization. We will focus initially on a one-dimensional sensor. The magnetic sensor consists of a submicron magnetic track in which the magnetization is oriented perpendicularly to the layer plane. In the presence of a perpendicular magnetic field, the wall moves in the track. This movement is converted to electric signal through a magnetic tunnel junction structured on the track and thus the measurement of the magnetic field is possible. The high mobility of the domain walls makes them sensitive to very weak magnetic fields. Our goal is to measure the Earth's magnetic field with great accuracy (accuracy on the direction <0.5 °) across ten mHz.

The development of the device includes the growth of a tunnel junction with perpendicular magnetization, nanofabrication cleanroom of the track and of the junction and the functional test performed in order to characterize its performance sensor:

1. under static field transport measurements to extract key parameters of the sensor sensitivity, linearity, magnetic field operating range
2. Sensor noise spectrum to determine its resolution and dynamic operation.
3. dependence of the temperature response. The latter should be the lowest possible for a functional device and potentially require compensation measures.

Once this basic concept demonstrated, our goal is to achieve an integrated 3D magnetometer recently patented in the laboratory.

Glossary of Acronyms

AF	Antiferromagnetic material
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DRAM	Dynamic Random Access Memory
EFE	Electric Field Control
PMA	Perpendicular Magnetic Anisotropy
IC	Integrated circuit
IoT	Internet of Things
CAM	Content-addressable memory
ITRS	International Technology Roadmap for Semiconductors
MR	Magnetoresistance
MRAM	Magnetic Random Access Memory
MLU	Magnetic logic unit
MTJ	Magnetic Tunnel Junction
NVM	Non Volatile Memory
SR-MRAM	Self-referenced magnetic random access memory.
PCRAM	Phase Change Random Access Memory
SAF	Synthetic antiferromagnet
SW-MRAM	Stoner-Wohlfarth magnetic random access memory
RA	Resistance Area product
R/W	Read and Write
SOC	System on chip
SOT	Spin Orbit Torque
SRAM	Static Random Access Memory
STT	Spin Transfer Torque
TAS	Thermally Assisted
TMR	Tunnelling MR
XOR	Exclusive-or logic function

PART III

ABOUT ME

A. CURRICULUM VITAE

Short bio

I have been conducting research on nanomagnetism and spintronics for more than 15 years. I hold a Physics degree from Babes Bolyai University in Cluj (Romania) and a PhD in Physics from Louis Pasteur University in Strasbourg where he pioneered the work on magnetic nanostructures.

After my PhD, I have joined SPINTEC research laboratory in Grenoble, where I pioneered scientific work on thermally assisted MRAM, tackling the key long-standing problem of bits stable enough for long-term storage, yet still easy to write with small magnetic fields. With my co-workers at SPINTEC, we took advantage of the temperature dependence of the magnetic properties to resolve this fundamental conflict: at operating temperature the bits would be stable, and at high temperature they would be easy to write. We pioneered experimental work in this field, establishing the basics scientific concepts and providing the first experimental proof that the thermally-assisted scheme worked. This work was reported in the well-cited paper, 'Thermally assisted switching in exchange-biased storage layer magnetic tunnel junctions'[120]. Based on this proof-of-principle of the scientific concepts, a start-up company was founded to develop and commercialize thermally assisted MRAM technology. Crocus was founded in Grenoble in 2006, and I was hired as the Research and Development Manager. In this capacity I led the research and development of this new technology, going beyond the scientific work he had done earlier in his career to now focus on solving the fundamental engineering challenges in order to make MRAM a viable product. The early success he achieved in this regard was reported in 'Thermally assisted MRAM'[121]. These two publications established both the basic science and technology of thermally assisted MRAM, and are by far the most highly cited publications in this field, with a total of more than 140 citations so far. The success achieved at this stage was enough to secure several rounds of venture capital funding for Crocus, which enabled it to grow into the successful company it is today, culminating in a $300 million financing deal in 2011 with RUSNANO to build an advanced MRAM manufacturing facility in Russia. For the work on TAS-MRAM and its successful transfer to Crocus, I have received in 2012 the SEE-IEEE Nicolas Brillouin award.

In 2013, I have returned to Spintec as deputy director, working on sub-20nm scalable MRAMs, hybrid logical circuits and magnetic sensors.

Professional experience

02/2013 – Present: Deputy Director

CEA/DSM/INAC/SPINTEC, Grenoble

- ⇨ Daily management of the laboratory (HR, finances, HCERES evaluation)
- ⇨ Management of the sensors team
- ⇨ Management of the R&D Crocus – Spintec research program (MRAMs & magnetic sensors)
- ⇨ Setup and managed several R&D projects: ANR Excalyb, joint spintronic line SPINTEC / LETI

08/2006 – 01/2013: R&D Manager

Crocus Technology, Grenoble

Management and expertise of magnetic materials for thermally assisted or STT-MRAMs

120 Prejbeanu, I. L., Kula, W, Ounadjela, K, Sousa, RC, Redon, O, Dieny, B, Nozieres, JP Thermally assisted switching in exchange-biased storage layer magnetic tunnel junctions IEEE TRANSACTIONS ON MAGNETICS 40(4) 2625 JUL 2004

121 Prejbeanu, I. L., Kerekes, M., Sousa, R. C., Sibuet, H., Redon, O., Dieny, B., Nozieres, J. P. , Thermally assisted MRAM, JOURNAL OF PHYSICS-CONDENSED MATTER 19(16) 165218 APR 25 2007

⇨ Engineering of magnetic tunnel junctions for industrial MRAMs and MLU (magnetic logic unit) - Led material development for advanced MRAM – thermally assisted with field or spin polarized current writing, self-reference concept for magnetic logic unit applications

⇨ Management of the R&D Crocus – Spintec research program

⇨ Management of the installation of a back-end magnetic processing line 200mm: deposition / magnetic anneal / characterization

⇨ Established the initial company wafer level test-chip design

⇨ Participated in company's early stage of strategic business development & planning

⇨ Built up intelligent monitoring scheme to diagnosis wafer processing defects at early stages, enabling high yields for product environment

⇨ Setup and managed several R&D projects: TIMI, R&D Crocus – INESC, ANR RAMAC, CRYSTO, CILOMAG, SPIN, PATHOS

⇨ Demonstrated the TA-STT concept

⇨ Demonstrated the self-reference cell writing adapted for logic applications and improved performances MRAM

12/2004 – 07/2006 : research engineer

CEA/DSM/DRFMC/SPINTEC, Grenoble

Magnetic logic based on extraordinary Hall effect & using domain wall movement in magnetic structures with perpendicular magnetization

Magnetic storage : STT based writing based from a near field nanometric tip

⇨ expert OMNT in nanomagnetism & spin electronics

⇨ editor of a special edition of J. Phys. C : Cond. Mat, dedicated to the spintronics

⇨ Setup an EU RTN project: SPINSWITCH

04/2003 – 11/2004 : Postdoc

CEA/DSM/DRFMC/SPINTEC, Grenoble

Thermally assisted MRAMs: first demonstration of the thermally assisted MRAMs with an exchange biased storage layer

⇨ Design and engineering of magnetic tunnel junctions, characterization, optimization of structural, electrical & magnetic properties

⇨Management of a R&D contract with CYPRESS SEMICONDUCTEUR

⇨Management of the ANR contract ECRIN (thermally inhibited memories with ferrimagnetic storage layers)

03/2002 – 03/2003: Postdoc

CNRS, Louis Néel laboratory & SPINTEC Grenoble

Magnetic storage: patterned media and writing by heating the dots by a near field nanometric AFM tip

⇨ Conception and development of the experimental setup : injection of spin polarized current

⇨ Fabrication of submicronic dots by e-beam and UV lithography and dry etching

⇨ Macroscopic magnetic characterization (Kerr, VSM), magnetic microscopy (MFM)

11/1998 – 02/2002 : PhD

IPCMS (Institut de Physique et Chimie des Matériaux de Strasbourg)

Nanomagnetism, spin electronics: domain wall magnetoresistance in nanowires & effect of

dipolar interactions on the reversal of the magnetization

- ⇨ Fabrication of nano-objects by e-beam lithography
- ⇨ Magnetotransport measurements magnetic microscopy MFM, micromagnetic simulations;
- ⇨ Local coordinator of the European contract MAGNOISE

10/1997 – 11/1998 : R&D engineer

INCDTIM (National institute for research & development of the isotopic and molecular technologies, Cluj-Napoca, Romania

Molecular Physics : multi-photonic dissociation of molecules in laser radiation field

March 1997 – July 1997 : Internship M2

LMGP (Laboratoire de Matériaux et de Génie Physique) - INPG Grenoble

Refractory materials :low temperature preparation of ultra-refractory nanocompounds

- ⇨ Structural characterization : X-ray & electronic microscopy

03/1996 – June/1996: Internship M1

Institut de recherche en physique de l'Université Babes Bolyai, Cluj Napoca, Roumanie

NdFeB permanent magnets : preparation & magnetic characterization

Education

2001 : PhD in physics – condensed matter & materials

Louis Pasteur University & Institut de Physique et Chimie des Matériaux de Strasbourg

1998 : Master of Science - condensed matter & materials

Babes-Bolyai University, Cluj-Napoca, Romania & INPG Grenoble

1997 : Bachelor in physics - condensed matter & materials

Babes-Bolyai University, Cluj-Napoca, Romania

Publications & patents

Over 60 papers in scientific journals & chapters in scientific books (Springer Verlag, NATO Science Series) ->H-index : 16

Over 35 patents filed, at different stages (granted, published, provisional pending)

Scientific reputation

Member of the organizing committee of several conferences and summer schools

- ⇨ Mesomagnetism spin dynamics and spin electronics, 11-17 September 1999, Rhodes, Greece
- ⇨ From Nanoscopic to mesoscopic magnetic systems, 28-31 august 2000, Spetses, Greece
- ⇨ « Magnétisme des systèmes nanoscopiques et structures hybrides », 1-10 september 2003, Brasov, Romania
- ⇨ French-American symposium on spin electronics, May 2006, St. Pierre en Chartreuse

Expert OMNT in nanomagnetism and spin electronics

Reviewer for several scientific journals (APL, IEEE Trans Magn, JMMM, JAP)

Editor of a special edition of J. Phys. C : Cond. Mat, dedicated to the spintronics

Several invited talks and tutorials in major international conferences (MMM, Intermag, JEMS, APS Meeting, ISAMMA, IMW) and thematic schools

Main scientific publications

1. MRAM: status and roadmap, I.L.Prejbeanu & B. Dieny, J. Phys D: Applied Physics (2014)
2. Heating asymmetry induced by tunneling current flow in magnetic tunnel junctions, E. Gapihan, J. Hérault, R. C. Sousa, Y. Dahmane, B. Dieny, L. Vila, I. L. Prejbeanu, C. Ducruet, C. Portemont, K. Mackay, and J. P. Nozières, Appl. Phys. Lett. 100, 202410 (2012)
3. Spin transfer torque switching assisted by thermally induced anisotropy reorientation in perpendicular magnetic tunnel junctions, S. Bandiera, R. C. Sousa, M. Marins de Castro, C. Ducruet, C. Portemont, S. Auffret, L. Vila, I. L. Prejbeanu, B. Rodmacq, and B. Dieny, Appl. Phys. Lett. 99, 202507 (2011)
4. Spintronic devices for memory and logic applications, Dieny, B., R.C. Sousa, J. Hérault, C. Papusoi, G. Prenat, U. Ebels, D. Houssameddine, B. Rodmacq, S. Auffret, L. Prejbeanu-Buda, M.-C. Cyrille, B. Delaët, O. Redon, C. Ducruet, J.-P. Nozières and I.L. Prejbeanu, Encyclopedia of Materials Science and Technology (2009)
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B. PHD SUPERVISING

The PhD supervising work has been done within the MRAM team at Spintec (including Ricardo Sousa, Bernard Dieny, Jean-Pierre Nozières) The objective of the MRAM team is to develop magnetic random access memories (MRAM) with improved performances (speed, scalability and power consumption) as requested by the market. Multiple approaches have been pursued in parallel. Spintec has been amongst the pioneers in MRAM development and is recognized worldwide as such. Consequently, we have / have had multiple partnerships with laboratories, research centers and companies, through joint R&D projects (ANR, EU), as well as bilateral industry partnerships. A preferred relation exists with Crocus, which led to the onset of a 5 years "joint laboratory" signed in 2013. Singulus Technologies, a German-based equipment company has been our long-lasting partner in EU projects and since 3 years we also have a partnership with Applied Materials, the leading semiconductor equipment company. More recently we also initiated projects with Samsung and Qualcomm.

Training students through research is one of SPINTEC key missions. Ensuring the highest standard of scientific and human management towards the early stage researchers (PhDs and post docs) is a commitment we share within all INAC teams. **SPINTEC students belong to 2 different doctorate schools** (School of Physics and EE School (EEATS - Ecole Doctorale Electronique, Electrotechnique, Automatique et Traitement du Signal). Over the reporting period, I co-supervised **a total number of 12 PhDs**, financed by combining a large **diversity of funding grants**: CEA grants (full or joint CFR financing), Grenoble doctoral schools grants (MESR), industrial funded PhDs (CIFRE), Nanoscience Foundation, joint grants with CNRS (BDI), co-financed with industry and other institutions (CNES, DGA) and finally direct financing by internal funds. **Diversifying and securing the funding sources is a constant challenge**, worth attempting as the number of high-quality candidates we are able to attract is larger than the number of PhD positions we are able to finance.

During their contract, we **monitor closely the scientific achievements** (publications, conferences) as well as the insertion into our ecosystem (PhD supervisor, collaborators, other PhDs). This monitoring includes **one-to-one interviews at critical stages of the PhD** (typically in the course of the 1st year, and at the beginning of 3rd year). When specific difficulties arise, the **issues are handled jointly** (when needed) by **the PhD supervisor, the group and laboratory management and the INAC human resource team**.

We dedicate a specific effort, supervised by the INAC assistant in charge of training through research, to ensure that the largest possible number of PhDs and post docs take advantage of the **specific training proposed to prepare their future careers** (such as job-interviews, knowledge of innovation models in industry…). Beyond training, we ensure that each student builds in due time a **personal career plan**. **Data carefully gathered on the professional insertion of former SPINTEC trainees** (PhDs and post docs) indicate that **almost all of them find a permanent position within 3 years, 1/3rd in the private sector (e.g. companies), 2/3rd in public research**. This is something we take a great pride of and, combined with our capacity to find funding, such figures help attract talents.

Finally, the **strong participation of SPINTEC researchers to the InMRAM and the European ESONN Schools** (teaching and training in the lab) is also worth noting. InMRAM was organized already 2 times by a local committee managed by Bernard Dieny and has attracted more than 100 participants each year.

List of PhD co-supervised

1. Yann Conraux (co-supervising 75%) – R&D engineer Crocus Technology

Préparation et caractérisation d'un alliage amorphe ferrimagnétique de GdCo entrant dans la conception de jonctions tunnel magnétiques. Résistance des jonctions tunnel magnétiques aux rayonnements ionisants

Université Joseph-Fourier, Grenoble, Oct. 10 2005, Directeur de thèse : Jean-Pierre Nozières

2. Marta Kerekes (co-supervising 25%) – passed away
Développement de nouvelles méthodes d'étude du comportement dynamique des systèmes de type vanne de spin à très hautes fréquences
Université Joseph-Fourier, Grenoble, 2006 – not defended, student died before defense, Directrice de thèse : Ursula Ebels

3. Lucien Lombard (co-supervising 33%) - R&D engineer Crocus Technology
Etude et extension de la gamme de température de fonctionnement des Mémoires Magnétiques à Accès Aléatoire Assistées Thermiquement
Université Joseph-Fourier, Grenoble, Dec. 1 2010, Directeur de thèse : Alain Schuhl

4. Erwan Gapihan (co-supervising 25%) - R&D engineer Crocus Technology
Mémoire magnétique à écriture assistée thermiquement à base de FeMn
Université Joseph-Fourier, Grenoble, Jan. 11 2011, Directeur de thèse : Bernard Dieny

5. Jérémy Herault (co-supervising 33%) - R&D engineer Crocus Technology
Mémoire magnétique à écriture par courant polarisé en spin assistée thermiquement
Université Joseph-Fourier, Grenoble, Oct. 4 2010, Directeur de thèse : Alain Schuhl

6. Maria Souza (co-supervising 25%) – Professor Brasil
Commutation précessionelle de mémoire magnétique MRAM avec polariseur à anisotropie perpendiculaire
Université Joseph-Fourier, Grenoble, Sep. 27 2011, Directrice de thèse : Ursula Ebels

7. Sebastien Bandiera (co-supervising 33%) - R&D engineer Crocus Technology
Jonctions tunnel magnétiques à anisotropie perpendiculaire et écriture assistée thermiquement
Université Joseph-Fourier, Grenoble, Oct. 21 2011, Directeur de thèse : Bernard Dieny

8. Giovanni Vinai (co-supervising 75%) – postdoc Trieste
Scalabilité et amélioration des propriétés d'échange des TA-MRAM
Université Joseph-Fourier, Grenoble, Dec. 16 2013, Directeur de thèse : Jean-Pierre Nozières

9. Kamil Akmaldinov (co-supervising 25%) –
Ferromagnetic/antiferromagnetic exchange bias nanostructures for ultimate spintronic devices
Université Joseph-Fourier, Grenoble, February, 06, 2015, Directeur de these: Bernard Dieny

10. Quentin Stainer (co-supervising 25%) - R&D engineer Crocus Technology
Development of self-referenced thermally assisted magnetic random access memory cells (MRAM)
Université Joseph-Fourier, Grenoble, defended December 19, 2014, Directeur de these: Bernard Dieny

11. Antoine Chavent (co-supervising 33%) – PhD ongoing
Bipolar TAS
Université Joseph-Fourier, Grenoble, to be defended 2015, Directeur de these: Bernard Dieny

12. Myckael Mouchel (co-supervising 50%) – PhD ongoing
Noise in MLU magnetic sensors
Université Joseph-Fourier, Grenoble, to be defended 2016, Directeur de these: Claire Baraduc

C. LIST OF PUBLICATIONS (AFTER PHD: 2002 - 2014)

1. JOURNAL ARTICLES (45)

1. I. L. Prejbeanu, S. Bandiera, Ricardo C. Sousa, Bernard Dieny

MRAM concepts for sub-nanosecond switching and ultimate scalability

Advances in Science and Technology 07/2014; 95:126-135.

2. Chavent, A., J. Alvarez-Hérault, C. Portemont, C. Creuzet, J. Pereira, J. Vidal, K. Mackay, R.C. Sousa, **I.L. Prejbeanu** and B. Dieny

Effects of the heating current polarity on the writing of thermally assisted switching-MRAM

IEEE Transactions on Magnetics 50 (2014) 3401504

3. Vinai, G., J. Moritz, G. Gaudin, J. Vogel, **I.L. Prejbeanu** and B. Dieny

Focussed Kerr measurements on patterned arrays of exchange-biased square dots

EPJ WEB of Conferences 75 (2014) 05003

4. Lacoste, B., M Marins de Castro Souza, T. Devolder, R.C. Sousa, L.D. Buda-Prejbeanu, S. Auffret, U. Ebels, C. Ducruet**, I.L. Prejbeanu**, L. Vila, B. Rodmacq and B. Dieny

Modulating spin transfer torque switching dynamics with two orthogonal spin-polarizers by varying the cell aspect ratio

Physical Review B 90 (2014) 224404

5. Stamps, R.L., S. Breitkreutz, J. Åkerman, A.V. Chumak, Y. Otani, G.E.W. Bauer, J.-U. Thiele, M. Bowen, S.A. Majetich, M. Kläui, **I.L. Prejbeanu**, B. Dieny, N.M. Dempsey and B. Hillebrands

The 2014 magnetism roadmap

Journal of Physics D: Applied Physics 47 (2014) 333001

6. Vinai, G., J. Moritz, S. Bandiera, **I.L. Prejbeanu** and B. Dieny

Large exchange bias enhancement in (Pt(or Pd)/Co)/IrMn/Co trilayers with ultrathin IrMn thanks to interfacial Cu dusting

Applied Physics Letters 104 (2014) 162401

7. Giovanni Vinai, Jerome Moritz, Gilles Gaudin, Jan Vogel, **Ioan Lucian Prejbeanu** and Bernard Dieny

IrMn microstructural effects on exchange bias variability in patterned arrays of IrMn/Co square dots

JOURNAL OF PHYSICS D-APPLIED PHYSICS, 2014

8. Akmaldinov, K., Ducruet, C., Portemont, C., Joumard, I., **Prejbeanu, I.L.**, Dieny, B., Baltz, V.

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Magnetic properties of patterned arrays of exchange-biased IrMn/Co square dots

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10. Vinai, G., Moritz, J., Bandiera, S., **Prejbeanu, I. L.**, Dieny, B.

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JOURNAL OF PHYSICS D-APPLIED PHYSICS 46(32) AUG 14 2013

11. **Prejbeanu, I. L.**, Bandiera, S., Alvarez-Herault, J., Sousa, R. C., Dieny, B., Nozieres, J-P

Thermally assisted MRAMs: ultimate scalability and logic functionalities

JOURNAL OF PHYSICS D-APPLIED PHYSICS VL 46(7) 074002 FEB 20 2013

12. **Prejbeanu, I. L.,** Sousa, R. C., Dieny, B., Nozieres, J. -P., Bandiera, S., Alvarez-Herault, J., Stainer, Q., Lombard, L., Ducruet, C., Conraux, Y., Mackay, K.

Scalability and logic functionalities of TA-MRAMs

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13. **Prejbeanu, I. L.,** Sousa, R. C., Dieny, B., Nozieres, J. -P., Bandiera, S., Mackay, K.

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15. Jabeur, K., Prenat, G., Di Pendina, G., Buda-Prejbeanu, L.D., **Prejbeanu, I.L**., Dieny, B.

Compact model of a three-terminal MRAM device based on Spin Orbit Torque switching

2013 International Semiconductor Conference Dresden - Grenoble (ISCDG)

16. Sousa, R.C., Bandiera, S., Marins de Castro, M., Lacoste, B., San-Emeterio-Alvarez, L., Nistor, L., Auffret, S., Ebels, U., Ducruet, C. , **Prejbeanu, I.L.**, Vila, L., Rodmacq, B., Dieny, B.

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17. Gapihan, E., Herault, J., Sousa, R. C., Dahmane, Y., Dieny, B., Vila, L., **Prejbeanu, I. L.**, Ducruet, C., Portemont, C., Mackay, K., Nozieres, J. P.

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Comparison of synthetic antiferromagnets and hard ferromagnets as reference layer in magnetic tunnel junctions with perpendicular magnetic anisotropy

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28. Papusoi, C., Conraux, Y., **Prejbeanu, I. L.**, Sousa, R., Dieny, B.

Switching field dependence on heating pulse duration in thermally assisted magnetic random access memories

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Pulsewidth Dependence of Barrier Breakdown in MgO Magnetic Tunnel Junctions

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31. Papusoi, C., Sousa, R., Herault, J., **Prejbeanu, I. L.,** Dieny, B.

Probing fast heating in magnetic tunnel junction structures with exchange bias

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32. Papusoi, C., Sousa, R. C., Dieny, B., **Prejbeanu, I. L.,** Conraux, Y., Mackay, K., Nozieres, J. P.

Reversing exchange bias in thermally assisted magnetic random access memory cell by electric current heating pulses

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33. Ghidini, M., Asti, G., Pernechele, C., **Prejbeanu, I. L.,** Solzi, M., Zangari, G.

Switching process in hard Co-Pt films

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34. Dieny, B., Sousa, R., **Prejbeanu, I. L.**

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35. **Prejbeanu, I. L.,** Kerekes, M., Sousa, R. C., Sibuet, H., Redon, O., Dieny, B., Nozieres, J. P.

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36. Ghidini, M., Zangari, G., **Prejbeanu, I. L.,** Pattanaik, G., Buda-Prejbeanu, L. D., Asti, G., Pernechele, C., Solzi, M.

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37. Sousa, RC, Kerekes, M, **Prejbeanu, IL**, Redon, O, Dieny, B, Nozieres, JP, Freitas, PP

Crossover in heating regimes of thermally assisted magnetic memories

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Temperature dependence of magnetic properties of AF-biased CoFe films with high FMR

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Dynamic heating in submicron size magnetic tunnel junctions with exchange biased storage layer

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Tunneling hot spots and heating in magnetic tunnel junctions

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Magnetic Random Access Memories

To be published, Springer Verlag (2015)

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Hybrid CMOS/Magnetic Memories (MRAMs) and Logic Circuits

Emerging Non-Volatile Memories, Springer US (2014)

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Magnetic memory with a magnetic tunnel junction written in a thermally assisted manner, and method for writing the same

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Magnetic tunnel junction with an improved tunnel barrier
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