Conception, modélisation et évaluation d'un convertisseur AC/DC réversible isolé

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Design,Modelling and Evaluation of a Bidirectional Highly Integrated AC/DC Converter

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Conception, Modélisation et Évaluation d'un Convertisseur AC/DC Bidirectionnel

Résumé

De nos jours, les énergies renouvelables tendent à remplacer les énergies fossiles. Pour assurer une interconnexion adéquate entre toutes ces installations électriques, l'électronique de puissance est nécessaire. Les spécifications de la prochaine génération de convertisseur de puissance sont un rendement, une fiabilité et une densité de puissance élevés, et de faibles coûts. L'intégration PCB (Printed Circuit Board) des composants actifs et/ou passifs est perçue comme une approche prometteuse, peu onéreuse et efficace. Les délais ainsi que les coûts de fabrication des convertisseurs de puissance peuvent être considérablement réduits. L'intégration permet également d'améliorer les performances des convertisseurs. Dans ce but, un concept original d'inductance 3D pliable utilisant la technologie PCB est présenté. Il permet un coût faible pour une production en série, ainsi qu'une excellente reproductibilité. Un usinage partiel de la carte PCB est utilisé, permettant le pliage et la réalisation des enroulements de l'inductance. Différents prototypes sont développés par le biais d'une procédure d'optimisation. Des tests électriques et thermiques sont réalisés pour valider l'applicabilité du concept au sein de convertisseurs de puissance. Le développement d'une procédure d'optimisation appliquée aux convertisseurs hautement intégrés utilisant l'enterrement PCB est présenté. Tous les choix importants facilitant l'intégration PCB, e.g. réduction des composants passifs, sont présentés. Cela inclut la sélection de la topologie adéquate avec la modulation associée. La procédure de design et les modèles analytiques sont présentés. Il en résulte un convertisseur comprenant quatre ponts-complets entrelacés avec des bras fonctionnant à basse (50 Hz) et haute (180 kHz) fréquences. Cette configuration autorise une variation de courant importante dans les inductances, assurant ainsi la commutation des semi-conducteurs à zéro de tension (ZVS), et ce sur toute la période du réseau. L'augmentation du volume du filtre CEM dû à la forte variation de courant sur le filtre CEM est compensé par la réduction du volume du dissipateur grâce aux faibles pertes par commutation. Deux prototypes d'un convertisseur AC/DC bidirectionnel de 3.3 kW sont présentés, les résultats théoriques et pratiques sont analysés. Dans les convertisseurs AC/DC monophasés, les condensateurs traditionnellement utilisés pour filtrer les ondulations à deux fois la fréquence du réseau sont très volumineux. Pour augmenter la densité de puissance du système, un filtre actif de type "Buck" est étudié. La procédure d'optimisation est adaptée à partir de la procédure implémentée pour le convertisseur AC/DC. L'approche utilisée, mène à un convertisseur opérant également en ZVS durant toute la période du réseau, et ce, à fréquence de commutation fixe. Les technologies sélectionnées, condensateur céramique et inductance compatible avec la technologie PCB sont favorable à l'intégration et sont implémentées sur le prototype.

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Les enjeux environnementaux encouragent le développement de l'électronique de puissance

Contexte environnemental et direction

Depuis plusieurs années maintenant, les politiques énergétiques à travers le monde se concentrent sur la réduction de l'impact de la mauvaise gestion de l'énergie sur le climat. Les énergies fossiles ont tendance à être réduites progressivement. Après le Protocole de Kyoto, le Protocole de Paris, en 2015, a été une nouvelle étape vers une protection mondiale de l'environnement. Avec les 189 plans nationaux couvrant 98 % des émissions de gaz à effet de serre, le réchauffement climatique est une préoccupation mondiale. Le principal objectif à long terme du protocole de Paris est de limiter la hausse de température moyenne en dessous de 2 °C [1].

Cependant, le dernier rapport du Groupe d'experts intergouvernemental sur l'évolution du climat (GIEC) indique que l'objectif de 2 °C n'est pas suffisant et qu'il y aurait de graves répercussions sur l'environnement. Par exemple, avec une augmentation de température d'environ 2 °C, 99 % des récifs coralliens sont menacés de disparaitre, l'augmentation du niveau de la mer de plus de 10 cm touchera plus de 10 millions de personnes et la fonte, intégrale, des glaces aura lieu tous les 10 ans. Une limitation de l'augmentation de la température de 1,5 °C peut atténuer ces problèmes [2].

Certaines méthodes sont envisagées pour réduire le réchauffement planétaire et les changements climatiques [3] :

1. Réduire ou même abandonner la production d'électricité au charbon. Le captage et la séquestration du CO2 peuvent être étudiés même s'il s'agit de solutions complexes et onéreuses [4]
2. Accroitre l'énergie nucléaire bien que la sécurité et les déchets radioactifs sont des enjeux majeurs et doivent être gérés
3. Préserver les forêts tropicales dans le monde et développer la reforestation
4. Promouvoir les énergies « vertes » (énergie éolienne, solaire, courants marin)

5. Économiser de l'énergie en produisant, en transportant, en distribuant et en consommant plus efficacement de l'électricité (objectif du réseau intelligent)
6. Remplacer les véhicules thermiques par des véhicules électriques et hybrides
7. Développer les transports électriques de masse (autobus, transport de marchandises)

Il est important de noter qu'une grande partie de ces solutions porte sur l'énergie électrique, comme l'amélioration de l'efficacité des installations électriques, le développement des énergies renouvelables et l'électrification du parc automobile. Ainsi, pour atteindre l'objectif de réduction des émissions de gaz à effet de serre de 80 à 95 % pour l'année 2050, en Europe, les deux tiers de l'énergie consommée devraient provenir de sources renouvelables. Toutes les actions et tendances sont présentées dans la « Feuille de route de l'énergie 2050 » [5]. L'énergie électrique a un rôle important à jouer, comme par exemple la dé-carbonisation des transports. 65 % de la demande énergétique, électrique, proviendra des voitures et des véhicules utilitaires. De plus, le développement des bâtiments à consommation positive, incluant les habitations individuelles, va augmenter. Ainsi, le réseau actuel, avec ses points de production centralisés, tend à évoluer vers un réseau incluant des points de production répartis.

« From grid to smart grid »

Le réseau actuel est composé d'importantes centrales électriques, généralement utilisant des combustibles fossiles (charbon, gaz et pétrole) avec une puissance nominale de 120 MW à 700 MW, d'énergie nucléaire ($>$ 1 GW) et de générateurs hydroélectriques (0.5 MW à $>$ 10 MW). Une régulation en fréquence est utilisée pour assurer une certaine tension et contrôler la puissance active et réactive en fonction de la charge (consommateurs) qui fluctue avec un facteur de puissance variable.

Compte tenu de tous les changements importants à venir mentionnés ci-dessus, la production et la distribution de l'énergie doit être mise à jour. L'association d'énormes centrales électriques, de longues lignes et de sous-stations proches du consommateur évoluera vers un réseau plus interactif (Smart Grid). La fusion

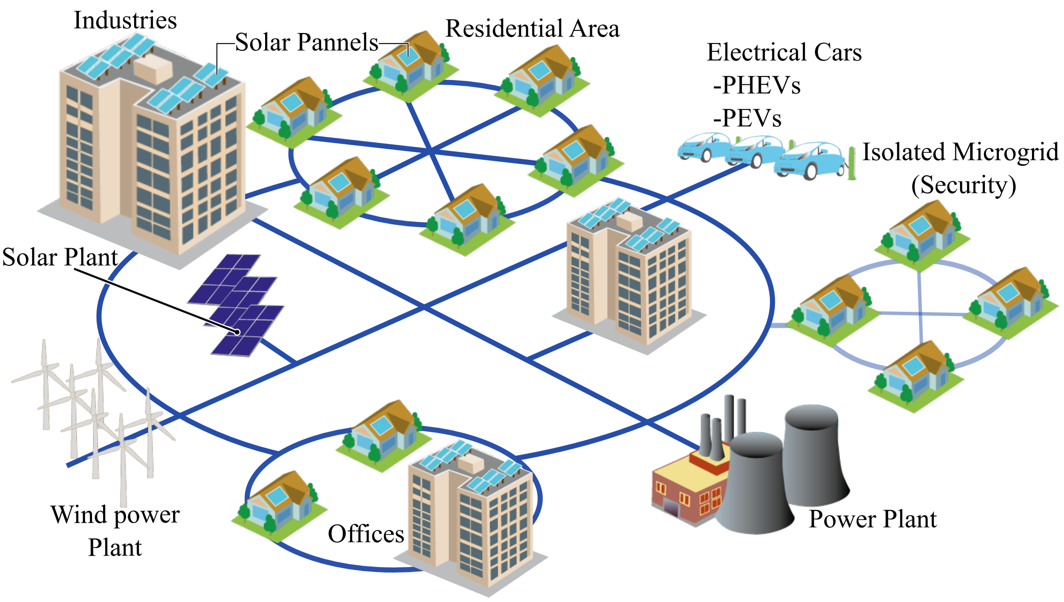


Figure 0.0.1 : « Smart grid » avec des sources distribuées

des connaissances dans les systèmes électriques, l'électronique de puissance, les communications, l'informatique et l'intelligence artificielle améliorera la fiabilité du réseau, la qualité de l'énergie électrique, l'efficacité énergétique et l'utilisation optimale des ressources de la sources vers les consommateurs [6]. Les sources d'énergie renouvelable, avec leur comportement sporadique, intègreront le réseau à plus grande échelle. Parallèlement, les sources distribuées augmenteront. Tous les acteurs, des distributeurs aux consommateurs, participeront à la sécurité et à la qualité du réseau en adaptant leur flux d'énergie à mesure que les industries, les bâtiments et les ménages seront en mesure de fournir de l'énergie au réseau. Les principes de « Home-to-Grid » (H2G), « Building-to-Grid » (B2G) et « Industry-to-Grid » (I2G) participent à la construction du futur réseau intelligent [7]. Le mouvement sera progressif étant donné que les technologies actuelles sont bien développées et profondément implantées, tandis que les nouvelles technologies prendront du temps pour intégrer pleinement le réseau actuel. Une représentation simplifiée d'un réseau intelligent et de ses acteurs est présentée dans la Figure 0.0.1.

Le développement des véhicules électriques hybrides rechargeables (VEHR) et de véhicules électriques (VE) est également concerné par cette évolution. Le concept de « Vehicle to Grid »(V2G) est étudié. Ce principe décrit un système dans lequel les VE/VEHR, considérés comme des sources et du stockage d'énergie mobiles (batterie de 20 à 50 kWh [8]), communiquent avec le réseau électrique pour vendre des services en réponse à la demande en renvoyant de l'énergie au réseau ou en limitant leur taux de recharge. Les aires de stationnement et de recharge pour les véhicules électriques peuvent être utilisées pour compenser le comportement sporadique des sources d'énergies renouvelables ou les problèmes de surcharge [9]. Ainsi, la stabilité du réseau peut être améliorée par les temps de réponse courts de ces installations. Le principe V2G et le concept de partage d'énergie sont principalement limités par le niveau de charge des batteries. La connaissance de l'heure de départ est cruciale pour assurer le niveau de charge requis avant le départ [10].

L'électronique de puissance : Un atout majeur

Parmi les solutions envisagées pour limiter le réchauffement climatique, la réduction de l'énergie gaspillée est importante et ce à chaque étape de la chaîne « production - consommation ». La mise en œuvre de l'électronique de puissance dans ces différentes étapes de la conversion énergétique peut améliorer l'efficacité [11]. Par exemple, l'utilisation ou l'amélioration de l'électronique de puissance dans le pilotage de moteurs, l'éclairage, la communication et les applications de transport peuvent représenter une économie d'énergie correspondant à 25 % de la consommation électrique de l'UE [12].

L'électronique de puissance représente le cœur des sources d'énergie renouvelables. De 1980 à 2018, la puissance maximale des éoliennes est passée de 50 kW à 10 MW et, depuis 2005, l'électronique de puissance couvre 100 % de la puissance du système [13], ce qui était déjà le cas pour le photovoltaïque (PV) depuis ses débuts. Les sources d'énergie éolienne et photovoltaïque dépendent de la météo. Par conséquent, des moyens de stockage importants sont mis en œuvre, comme par exemple, des batteries, des volants d'inertie, le stockage d'énergie grâce aux matériaux supraconducteurs [14] ou bien grâce au pompage hydroélectrique. Toutes ces techniques de stockage dépendent largement de l'électronique de puissance pour stocker puis redistribuer l'énergie sur le réseau [15].

Comme précédemment mentionné, les véhicules électriques représentent une technique de transport efficace et propre si rechargés par le biais de sources renouvelables. Le développement de tels véhicules dépend également de l'électronique de puissance. Des convertisseurs de puissance sont nécessaires pour la propulsion et la recharge, qui peut-être réalisée grâce à un chargeur embarqué de faible puissance ou bien des bornes de recharge rapide [16]. L'électronique de puissance est donc une pièce maitresse du développement du concept V2G.

En conclusion, tous ces développements conduisent à davantage d'interconnexions entre différents niveaux de puissance et types de sources (AC, DC, basse tension, haute tension). De plus, le contrôle du flux d'énergie est obligatoire dans un réseau intelligent pour des raisons de sécurité et de qualité de l'énergie, des systèmes bidirectionnels sont donc nécessaires. Les convertisseurs de puissances sont un moyen efficace et flexible pour assurer l'interconnexion des différents acteurs au sein du réseau. La possibilité de changer rapidement de mode de fonctionnement est un avantage majeur. De plus, la consommation de puissance réactive peut être facilement réduite voir même annulé grâce à un contrôle adapté [17]. Par conséquent, l'électronique de puissance est essentielle au bon développement du concept de « smart grid » et à la limitation du réchauffement climatique [18].

Optimisation multiobjectifs des convertisseurs de puissance

Depuis plusieurs années maintenant, les tendances en électronique de puissance sont dirigées vers le design de convertisseurs haute efficacité et haute densité pour faciliter l'intégration des convertisseurs dans des systèmes complexes. Un rendement élevé est intrinsèquement requis pour assurer une haute densité de puissance. Cette tendance est principalement impactée par des objectifs de volume et de réduction de coûts [19][20]. Avec les contraintes futures concernant l'amélioration de l'efficacité globale, la conception de convertisseurs hauts rendements est donc primordiale, tout en assurant d'autres objectifs. Les principaux objectifs en électronique de puissance sont :

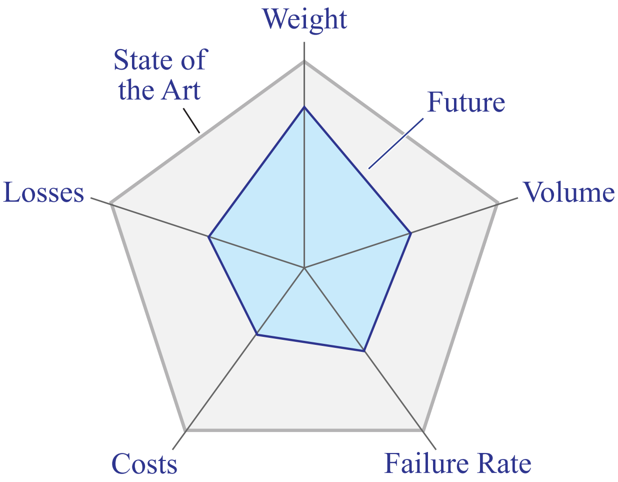


FIGURE 0.0.2 : Tendances des performances en électronique de puissance [21]

- Haut rendement (η) [%]
- Haute densité de puissance (γ) $\left[\frac{kW}{kg}\right]$
- Haute densité volumique (ρ) $\left[\frac{kW}{dm^3}\right]$
- Bas coûts [\$,€]
- Haute fiabilité

Ces objectifs sont considérés comme « Indices de performances » interdépendants. Ces indices peuvent être mesurés ou calculés, permettant ainsi une comparaison avec des produits actuels du marché afin d'évaluer l'évolution et l'amélioration des convertisseurs de puissance. Les différentes tendances liées à ces indices de performances sont présentés dans la Figure 0.0.2.

Pour atteindre ces objectifs et repousser les limites de conception des convertisseurs, une procédure d'optimisation est nécessaire, tout comme de nouvelles technologies (matériaux, composants), des topologies efficaces avec un contrôle approprié et bien sûr de nouveaux procédés de fabrication [22]. Dans l'article [23], l'optimisation de convertisseurs est mathématiquement définie comme un ensemble de quatre éléments. Le premier étant, l'ensemble des spécifications liées au projet et/ou à l'application (e.g. niveaux de tension, puissance), ici cet ensemble est représenté par le vecteur $\overrightarrow{r}$.

$$\overrightarrow{r} = (r_1, r_2, r_3, \ldots, r_n) \tag{0.0.1}$$

Le second correspond aux constantes imposées au design qui sont typiquement, les spécifications des fabricants, les propriétés des matériaux, e.g. matériaux magnétiques. Ces constantes sont définies par le vecteur $\overrightarrow{k}$.

$$\overrightarrow{k} = (k_1, k_2, k_3, \ldots, k_m) \tag{0.0.2}$$

Le troisième vecteur, $\overrightarrow{x}$, inclut toutes les variables possibles pour le design, par exemple la fréquence de commutation, la valeur de l'inductance. Ces trois vecteurs sont liés par les contraintes propres au design. Ces contraintes sont représentées par les vecteurs $\overrightarrow{g}$ et $\overrightarrow{h}$ qui peuvent présenter une égalité ou inégalité. Typiquement, les contraintes pour un convertisseur de puissance peuvent être une limitation de la température de fonctionnement, le flux maximal dans une inductance, un mode conduction, le respect d'une norme CEM, etc.

$$\overrightarrow{x} = (x_1, x_2, x_3, \ldots, x_l) \tag{0.0.3}$$

$$g_i(\overrightarrow{x}, \overrightarrow{k}, \overrightarrow{r}) = 0 \qquad i = 1, 2, 3, \ldots, p \tag{0.0.4}$$

$$h_j(\overrightarrow{x}, \overrightarrow{k}, \overrightarrow{r}) \geq 0 \qquad j = 1, 2, 3, \ldots, q \tag{0.0.5}$$

L'association de plusieurs variables conduit à une infinité de solutions possibles qui respectent les différentes contraintes ainsi que les spécifications du projet. Pour être capable de sélectionner un seul convertisseur parmi cette multitude de possibilités une fonction objectif peut être utilisée. Cette fonction $f(\overrightarrow{x}, \overrightarrow{k})$ peut être liée à n'importe quel indice de performance (p_i) présenté plus tôt, volume, coût, etc.

◇

$$p_i = f(\overrightarrow{x}, \overrightarrow{k}) \Rightarrow Max \qquad (0.0.6)$$

Comme mentionné précédemment, les différents prototypes en électronique de puissance doivent répondre à plusieurs objectifs. Par conséquent, plusieurs indices de performances se doivent d'être optimisés simultanément, e.g. rendement-volume ou bien même efficacité-volume-coût. Plusieurs fonctions objectifs doivent être simultanément respectées. Cependant, certains objectifs n'impactent pas le design de la même manière, ainsi la fonction peut être pondérée [24].

$$\sum w_i \cdot f_i(\overrightarrow{x}, \overrightarrow{k}) \Rightarrow Max \qquad (0.0.7)$$

Toutes ces définitions sont communes à n'importe quel design de convertisseurs et n'importe quelle procédure d'optimisation. La principale différence est comment la solution finale est définie et sélectionnée. Une méthode est la sélection par la procédure d'optimisation elle-même se basant sur les différents objectifs et l'erreur relative obtenue concernant ces derniers. C'est le cas de l'Algorithme Génétique (AG) proposé par Holland [25]. L'algorithme génétique est une procédure d'optimisation discrète utilisant des bases de données de composants discrets pouvant être implantés directement dans un prototype ou produit. Cette méthode de design a été largement utilisée en électronique de puissance [26, 27, 28, 29]. Elle est particulièrement intéressante lorsque certains composants discrets (semiconducteurs, noyaux magnétiques, condensateurs...) sont les variables d'optimisation. Premièrement, l'algorithme créer aléatoirement plusieurs individus, chacun représentant une solution spécifique, le tout formant une population. Chaque individu est défini par ces « gènes » dépendant des bases de données. Le nombre de gènes est équivalent au nombre de variables. Toutes les solutions sont évaluées en fonction des contraintes et des objectifs. Les designs les plus efficaces sont sélectionnés pour créer la « génération » suivante. Les solutions parentes sont combinées pour former les « enfants » ayant des caractéristiques croisées qui devraient conduire à des solutions plus performantes, comme illustré dans la Figure 0.0.3. D'autres opérateurs génétiques peuvent être appliqués, par exemple, « la mutation » qui change un ou plusieurs gènes de manière aléatoire

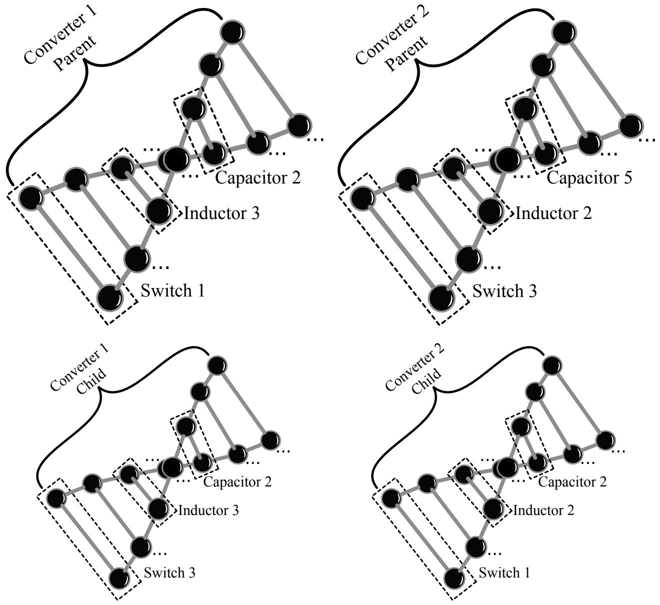


FIGURE 0.0.3 : Illustration de design de convertisseurs avec Algorithme Génétique

afin d'ouvrir vers un nouvel espace de solutions. Afin de toujours garder le meilleur design dans la boucle, les pires designs de la génération enfante sont remplacés par les meilleures de la génération parente. Cette procédure est réitérée jusqu'à que le critère de convergence soit atteint et que le design final soit sélectionné.

Malgré tout l'intérêt porté à cette méthode d'optimisation, elle présente quelques inconvénients. Dans le cas d'utilisation de variables d'optimisation continues, telles que la fréquence de commutation, des opérateurs génétiques spéciaux sont requis afin de produire la nouvelle valeur entre « parents » et « enfants ». Étant donné que cette méthode d'optimisation est basée sur des fonctionnalités aléatoires et sur un critère de convergence, il est plus difficile d'analyser l'impact des différentes variables d'optimisation.

Une autre méthode utilisant une représentation graphique des différentes possibilités peut être implémentée. Ainsi, l'espace de conception représenté par les variable $\overrightarrow{x}$ et les constantes $\overrightarrow{k}$ peut être transformé en espace de performance où certains indices de performance p_i sont les axes. Contrairement à une optimisation à objectif unique ou un résultat est placé sur l'un des axes, l'optimisation à objectifs multiples conduit à une multitude de possibilités, tout comme l'optimisation avec l'algorithme génétique. Par conséquent, le meilleur compromis, selon le

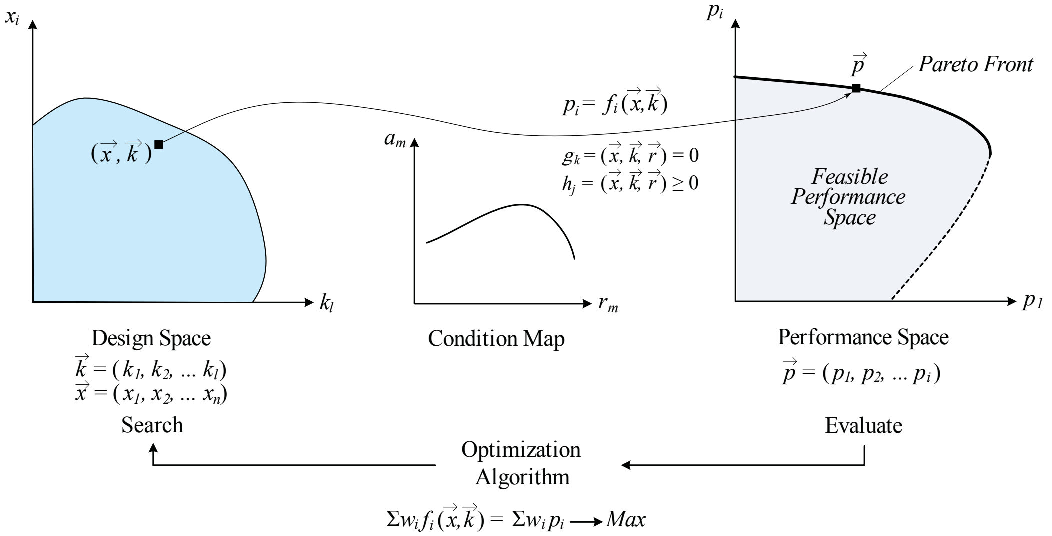


FIGURE 0.0.4 : Optimisation multiobjectif d'un espace de design multidimensionnel [21]

concepteur, doit être définie dans la représentation des solutions dans l'espace des performances. Généralement la sélection du meilleur compromis est réalisé sur la frontière les solutions réalisables. Cette frontière représente le front de Pareto. La représentation d'une optimisation à objectifs multiples est illustrée dans la Figure 0.0.4.

Habituellement, ce genre d'optimisation est réalisée pour une topologie préalablement définit avec le contrôle associé, le tout répondant aux exigences. Le fonctionnement du convertisseur est mis en équations selon les différents composants et /ou les technologies sélectionnés. Bien que les possibilités de design soient limitées par ces choix préliminaires, l'optimisation reste complexe du fait de la multitude de solutions restantes, dépendantes des semiconducteurs, noyaux magnétiques et de toutes les combinaisons de variables possibles. Afin de faciliter le design du convertisseur optimal, la procédure d'optimisation peut inclure une boucle principale, qui dépend des variables d'optimisation, et des sous parties qui correspondent aux différentes fonctions du convertisseur. Les sous-parties de l'optimisation correspondent à une étude à l'échelle du composant, comme par exemple les transistors, les inductances, les condensateurs. Cependant, ces sous-parties sont liées les unes aux autres, e.g. le choix des semiconducteurs impacte la conception du filtre CEM. Cette méthode de conception permet de comparer plusieurs solutions entre elles et d'analyser rapidement l'impact des variables. Cette méthode est donc préférée à l'algorithme génétique précédemment présenté.

L'amélioration des performances grâce à l'intégration PCB

En électronique, l'intégration consiste à regrouper dans un composant ou puce plusieurs éléments de base, habituellement des transistors, afin de créer des fonctions plus complexes. En électronique de puissance, différents composants (transistors de puissance, circuit de contrôle, inductances et condensateurs) sont essentiels pour concevoir une cellule de commutation élémentaire. Par conséquent, l'intégration en électronique de puissance consiste en l'amélioration de l'assemblage de ces composants de base afin de créer une « brique universelle » facilitant l'interconnexion pouvant ainsi répondre aux exigences de différentes applications.

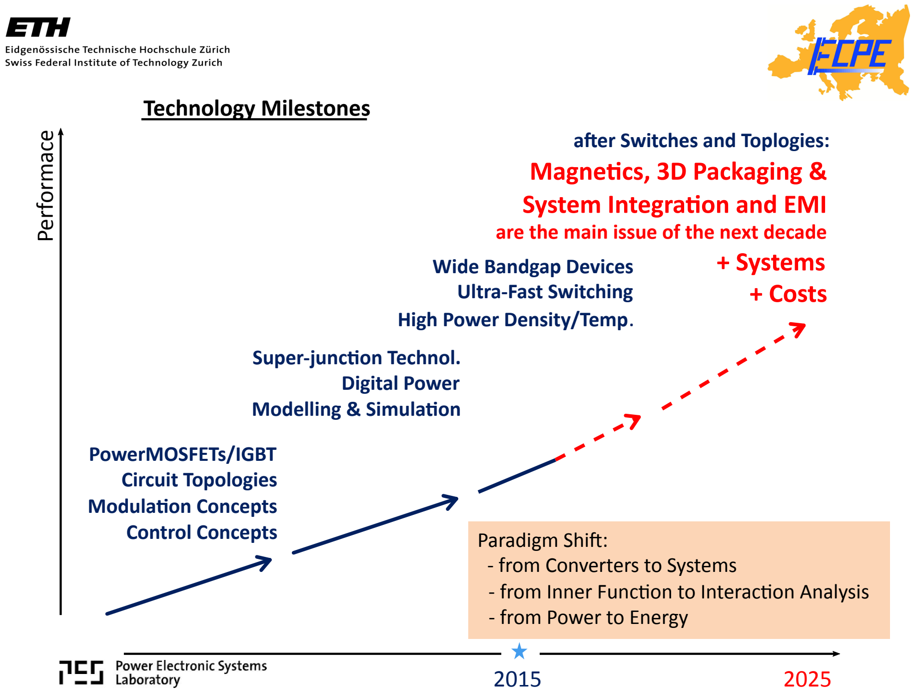
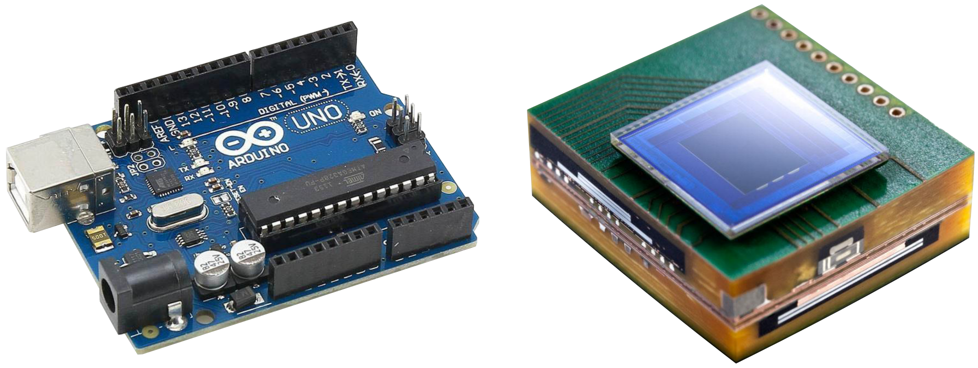


FIGURE 0.0.5 : Feuille de route d'ECPE [30]

◇



(a) Composants montés en surface (SMD) (b) PCB avec composants enterrés [31]

FIGURE 0.0.6 : Exemples d’assemblages PCB

L’intégration d’un point de vue « système » est l’une des principales préoccupations de la communauté de recherche en électronique de puissance comme il est montré sur la feuille de route des prochaines années du « European Center for Power Electronics (ECPE) », (Figure 0.0.5).

Dans le domaine de l’électronique, incluant l’électronique de puissance, l’utilisation de cartes PCB multi-couches est extrêmement courante du fait de la simplicité de fabrication sur-mesure. Le process de fabrication est complètement maîtrisé et il est peu onéreux lorsque qu’il est utilisé pour une production de masse. Habituellement, les composants électroniques sont connectés sur les couches externes de la carte PCB, comme sur la Figure 0.0.6.(a). Depuis quelques années maintenant, l’intérêt pour les composants enfouis ne cesse d’augmenter. Ce procédé permet d’utiliser l’espace interne entre les différentes couches de cuivre afin d’y placer de petits composants tels que des condensateurs, résistances et semiconducteurs. La Figure 0.0.6.(b) présente une coupe d’un module caméra de 1.6 x 1.6mm^2 incorporant des composants actifs et passifs enterrés. Le procédé d’intégration PCB répond explicitement à la demande de systèmes haute densité.

Objectifs de la thèse et spécifications

« L’intégration » est l’une des activités de recherche majeures de Mitsubishi Electric R&D Centre Europe avec le design de convertisseurs hautement intégrés.

Table 0.1 : Spécifications du PFC

Tension d'entrée	85-260 $\mathrm{V_{RMS}}$(AC)
Courant d'entrée Max.	15 $\mathrm{A_{RMS}}$(AC)
Courant de sortie Max	12 A (DC)
Tension de sortie	200V to 400 V (DC)
Puissance Max	3.3 kW
Environnement	-40 to 60°C
CEM	EN55011 Class B CEM conduite

Cela comprend des projets internes à l'entreprise et des collaborations. L'une de ces collaborations est réalisé avec le laboratoire Ampère pour l'encadrement de deux doctorants, la combinaison de ces deux thèses conduit au développement d'un convertisseur AC/DC hautement intégré avec de hautes performances. Le procédé PCB est particulièrement investigué dans ce design.

L'un des sujets traite plus particulièrement du procédé d'intégration. Ce projet de thèse est mené par Rémy CAILLAUD et est intitulé *« Integration of a 3.3 kW bidirectional AC/DC converter using PCB process »* [32]. Le travail réalisé dans cette thèse couvre l'intégration PCB des composants actifs et passifs. Concernant l'intégration des composants passifs, les inductances de puissances sont réalisées grâce à l'enterrement des noyaux magnétiques dans le substrat PCB afin de développer des inductances plates. Le management thermique par convection naturelle est aussi étudié pour les semiconducteurs et les inductances. Le procédé PCB est étroitement développé avec le fabricant (CIMULEC) pour l'intégration des puces de puissance, des composants packagés et des magnétiques.

La deuxième thèse, présentée dans ce document, étudie la topologie du convertisseur. En effet, la sélection de la topologie appropriée avec le contrôle associé est primordiale car cela affecte largement le degré d'intégration du système. La solution choisie doit induire une réduction du volume des composants passifs car ils représentent la majeure partie du volume global [33]. Une procédure d'optimisation, similaire à celle présentée précédemment, doit être développée selon la topologie sélectionnée et les contraintes ($\overrightarrow{g}$ et $\overrightarrow{h}$) impactées par l'intégration

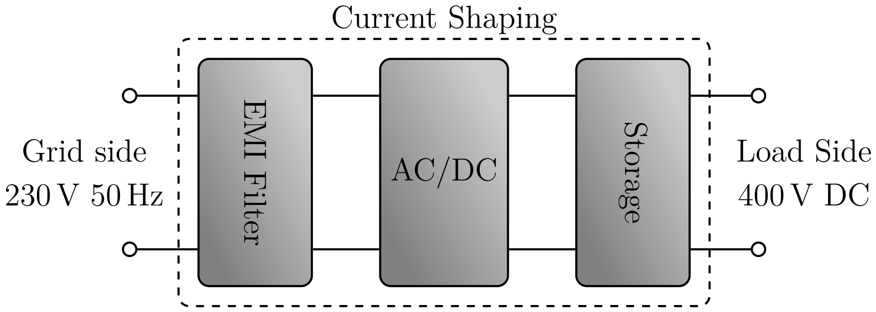
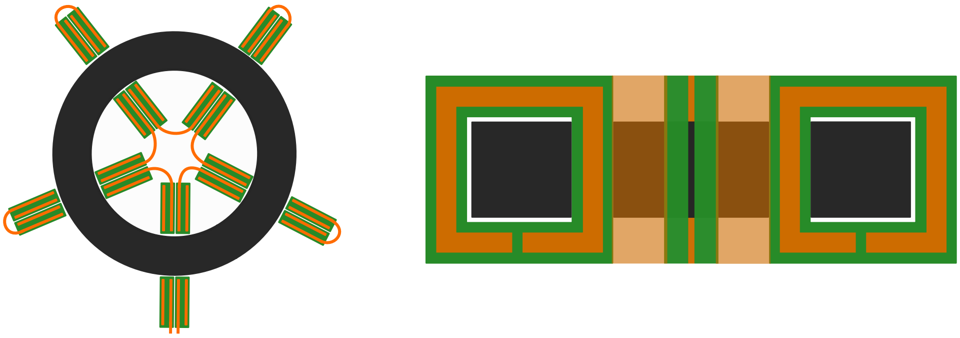


FIGURE 0.0.7 : Représentation des blocs fonctionnels du convertisseur

PCB. Elle doit inclure la conception du filtre CEM. Les variables d'optimisation ($\overrightarrow{x}$) ont besoin d'être définies. Les spécifications et contraintes ($\overrightarrow{r}$ et $\overrightarrow{g}$, $\overrightarrow{h}$ respectivement) au début du projet sont présentées dans le Tableau 0.1. Les différentes parties étudiées dans ce projet sont illustrées dans le Figure 0.0.7.

Concept d'inductance 3D pliable

Ce document présente également un nouveau concept d'inductance utilisant le procédé PCB afin de réaliser le bobinage. L'inductance est réalisée à partir d'un PCB classique. Ce concept requière l'utilisation de PCB avec au minimum 2 couches de cuivre afin de former les enroulements comme présenté dans la Figure 0.0.8.



(a) Coupe axial

(b) Coupe radial

FIGURE 0.0.8 : Concept d'inductance 3D

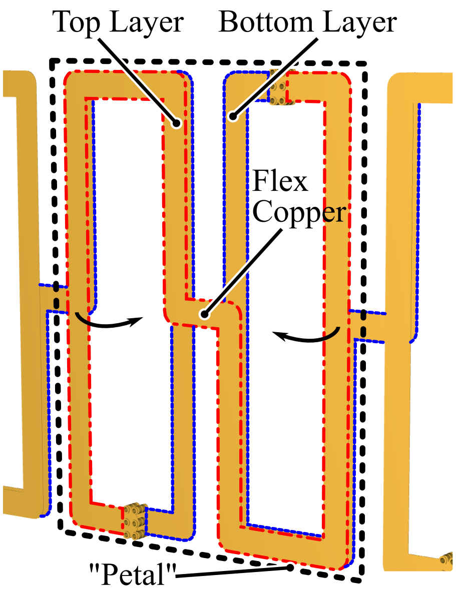


FIGURE 0.0.9 : Principe de l'inductance 3D

Ces enroulements sont composés de plusieurs parties interconnectées par du cuivre « flexible ». Par conséquent, ce design ne nécessite aucune soudure. L'inductance est obtenue en pliant les différentes parties du PCB. La forme finale est proche de celle d'une fleur, ainsi deux parties pliées sont appelées « pétale ». Les enroulements de l'inductance sont placés autour de demi-noyaux de ferrite (C). Cependant il est aussi possible d'utiliser des poudres magnétiques [34] car le matériau peut être moulé autour des enroulements. La géométrie proposée ici est principalement limitée par le diamètre interne des noyaux et l'épaisseur du PCB.

La réalisation des pétales avec un PCB deux couches est présentée dans la Figure 0.0.9. Un tour et demi est réalisé sur chaque morceaux de PCB en utilisant les couches cuivre extérieures. Ainsi chaque pétale permet de réaliser trois tours. Par conséquent, ce concept d'inductance est limité à un nombre de tours multiple de trois.

Toutes les étapes de pliage pour obtenir l'inductance 3D à partir d'un PCB plat sont présentées dans l'Annexe A.1.

Prototypage avec deux technologies PCB

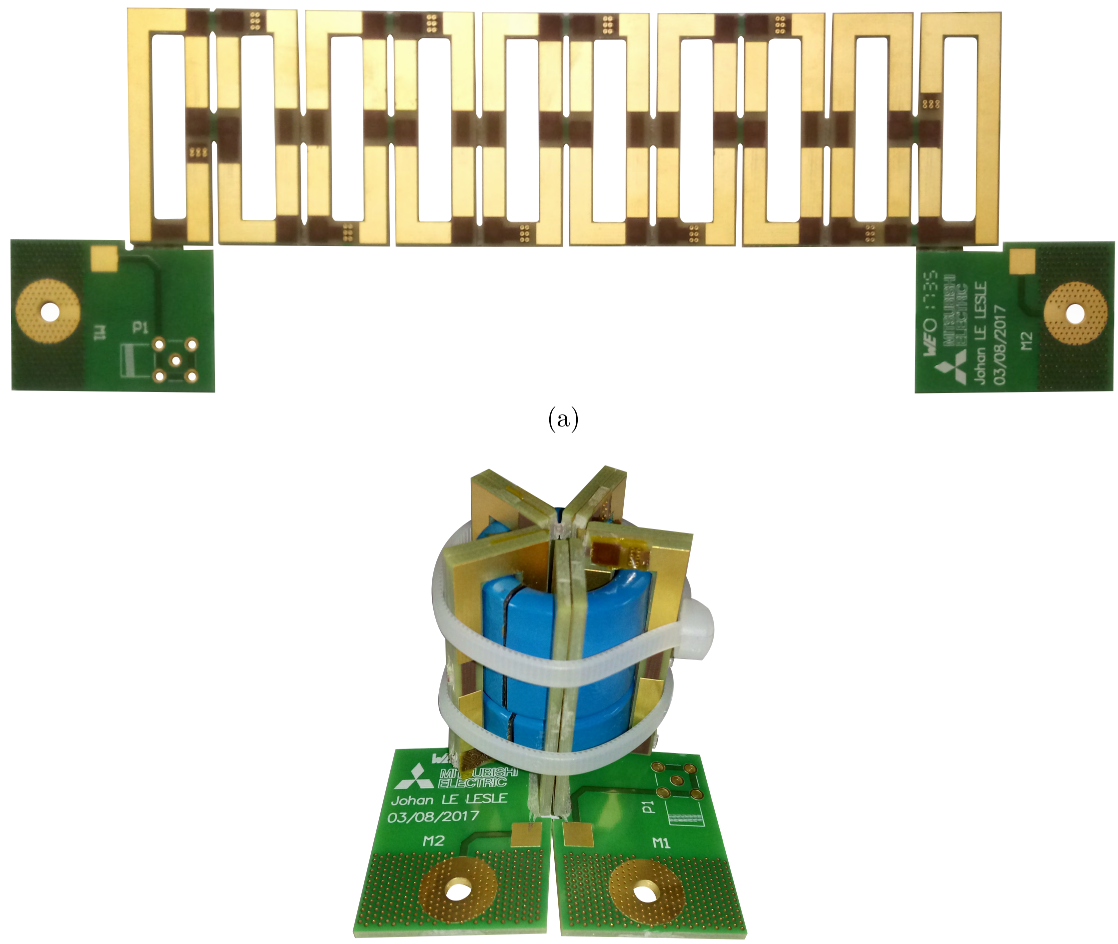
Deux prototypes sont réalisés à partir d'une procédure d'optimisation tenant compte des contraintes liées à la technologie PCB utilisée ainsi que les contraintes magnétiques et thermiques. Le prototype est réalisé avec trois noyaux empilés B64290L0626X087. Plusieurs prototypes sont réalisés avec les technologies Wirelaid et semi-flex. Chaque prototype est simulé et caractérisé avec un impédance–mètre Agilent 4294A. L'évolution de la résistance série est analysée comme indicateur de performance.

Technologie Wirelaid

Le tout premier prototype utilise la technologie Wirelaid afin de pré-évaluer la faisabilité du concept. Le PCB comprend quatre couches et présente une épaisseur de 1.5 mm. Des conducteurs épais en cuivre sont placés sur les couches internes afin de réaliser les enroulements et les interconnexions flexibles. Une fois pliée, l'inductance ne peut plus être désassemblée. Le layout de l'inductance est présenté plus en détails dans l'Annexe A.2. L'inductance une fois pliée est présentée dans la Figure 0.0.10.

Le prototype est par la suite caractérisé au moyen d'un impédance-mètre Agilent 4294A. L'inductance ainsi que la résistance équivalente sont présentées dans la Figure 0.0.11. La mesure de l'inductance est égale à 29 µH, ce qui est supérieur à ce qui était attendu. Cela peut être corrigé en jouant sur l'entrefer. Cependant la caractéristique la plus contraignante est la résistance série. Une augmentation significative de résistance pour une gamme de fréquence supérieure 10 kHz est notable. Elle est supérieure à 0.5 Ω à partir de 120 kHz. Ce design peut conduire à des pertes importantes au sein de convertisseurs opérant généralement à plusieurs centaines de kHz.

Pour bien comprendre les raisons de ce comportement, des simulations 2D par éléments finis ont été effectuées sur Flux® de CEDRAT. La géométrie simulée est une coupe transversale. Les simulations correspondent à un problème magnéto-harmonique, le maillage est automatiquement conçu par le logiciel pour inclure les effets de peau et de proximité. Avec le maillage automatique, des

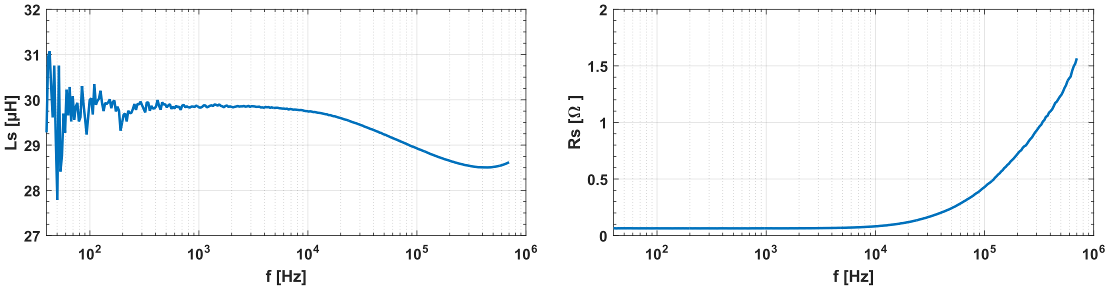


(a)

(b)

FIGURE 0.0.10 : Prototype Wirelaid

◇



(a) Inductance (b) Résistance

FIGURE 0.0.11 : Caractéristiques de l'inductance Wirelaid

triangles sont utilisés pour les surfaces. La résolution du problème est réalisée avec l'algorithme de Newton-Raphson. La simulation est réalisée en fonction de la hauteur du noyau. Il manque donc les parties supérieure et inférieure du circuit imprimé. Les zones de pliage ne sont pas incluses. Les couches de cuivre externes non connectées sont incluses dans la simulation et les entrefers sont placés de manière à s'adapter le plus possible au prototype. Ces résultats sont comparés aux mesures.

Semi-flex technologie

La seconde solution étudiée est le semi-flex. Ce procédé est bien connu et maitrisé par les fabricants, ce qui rend le prix plus attractif et réduit les délais de livraison. Cette technologie est plus adaptée à la production en série. La principale limite de la technologie provient de l'épaisseur de cuivre proposée par certains fabricants. Le cuivre utilisé pour les pièces pliées n'a qu'une épaisseur de 60 µm. Ceci est un problème lorsque des courants élevés traversent l'inducteur. Pour surmonter ce problème, des circuits imprimés multicouches sont utilisés et certaines couches sont parallélisées dans la partie rigide pour obtenir une section transversale en cuivre de 0,6 mm^2. En ce qui concerne les pièces flexibles, les grands plans en cuivre sont utilisés pour gérer les contraintes mécaniques et électriques.

Comme l'épaisseur de cuivre est plus faible, la rigidité est moindre et la technologie est plus flexible que celle utilisant du cuivre épais. Une caractéristique intéressante pour le prototypage est la possibilité de démonter l'inductance.

(a)

(b)

(c)

Figure 0.0.12 : Prototypes d'inductance Semi-flex

◇

Deux prototypes sont proposés, le premier orienté verticalement (voir Figure 0.0.12.(b)), comme le Wirelaid, et le second orienté horizontalement (voir Figure 0.0.12.(a) et (c)). Ces prototypes sont construits avec une carte de circuit imprimé de 1,2 mm d'épaisseur avec six couches de 60 µm et de 70 µm d'épaisseur de cuivre, pour les couches externes et internes, respectivement. Contrairement à Wirelaid, les couches flexibles sont les couches externes. La longueur des plans de cuivre ($\mathrm{L}_{\mathrm{flex}}$) est calculée pour obtenir un rayon de courbure de 180 °. Elle est déterminée en fonction de la largeur d'un pétale qui dépend de l'épaisseur du PCB ($\mathrm{T}_{\mathrm{PCB}}$) et du petit espace entre les deux PCB (voir Equation 0.0.8).

$$L_{flex} = \frac{\pi \cdot (2 \cdot T_{PCB} + g)}{2} \tag{0.0.8}$$

Dans ce cas, l'épaisseur du circuit imprimé est de 1,2 mm et l'espace supposé (g) est de 0,5 mm ; la longueur de la partie flexible est donc de 4 mm. Cette longueur donne le rayon de courbure le plus homogène. Dans ces modèles, à cinq pétales, les noyaux ne sont pas coupés en deux moitiés identiques, afin d'avoir les entrefers le plus loin possible des pétales.

Ces deux prototypes ont étés étudiés au travers de tests électriques et thermiques. Même si le concept est validé, des investigations supplémentaires sont nécessaires. Le point principal est la gestion thermique. Comme la surface est importante, l'inducteur 3D est très intéressant avec un flux d'air sur l'inductance elle-même. Cependant, dans le cas de la convection naturelle cela est plus compliqué en raison de la géométrie particulière. Le projet actuel considère uniquement une plaque froide refroidie naturellement. C'est la raison principale pour laquelle le nouvel inductance 3D n'est pas inclus dans les prototypes de convertisseurs suivants, même si de bonnes performances sont attendues avec ce nouveau concept.

♠

Méthodologie de conception de convertisseurs discrets et intégrés à haute efficacité

Le choix de la topologie appropriée en fonction des spécifications et le développement d'une procédure d'optimisation appropriée sont importants. Les deux améliorent les performances du convertisseur. Différentes possibilités de contrôle associées à la topologie pont-complet sont étudiées pour analyser leur impact sur l'efficacité et la densité de puissance. L'utilisation d'inductances de puissance est inhérente à l'électronique de puissance, que ce soit pour le filtrage ou pour le stockage d'énergie. Par conséquent, le développement d'une procédure d'optimisation compatible avec les convertisseurs intégrés, y compris les inductances de puissance, est obligatoire. Néanmoins, l'intégration des inductances de puissance reste un défi, car la taille de ces inductances est toujours importante. La tendance actuelle afin de réduire la taille des composants passifs est l'augmentation de la fréquence de commutation, rendue possible par le développement de composants à large bande interdite. Mais cela pose d'autres problèmes, tels que l'augmentation des pertes dans les semi-conducteurs et la CEM, qu'il convient de prendre en compte. Par conséquent, la procédure de conception présentée dans ce chapitre inclut tous ces aspects. La méthodologie utilisée pour générer toutes les formes d'ondes utiles est présentée. Ensuite, la procédure d'optimisation développée divisée en trois parties principales est détaillée. Ces trois parties correspondent au choix des semi-conducteurs, à la conception du filtre d'entrée (mode différentiel DM, mode commun CM) et à la conception magnétique. La procédure est utilisée pour les convertisseurs discrets et intégrés.

Sélection de la topologie adaptée à l'intégration

Pour améliorer les performances du convertisseur, il est possible d'associer plusieurs cellules élémentaires et de développer une approche de conception modulaire. La topologie de pont complet est sélectionnée en tant que cellule élémentaire pouvant être associée en série ou en parallèle. Cette association est ensuite utilisée pour construire le correcteur de facteur de puissance (PFC). Les avantages du pont complet sont le nombre raisonnable de semiconducteurs sur le chemin du courant,

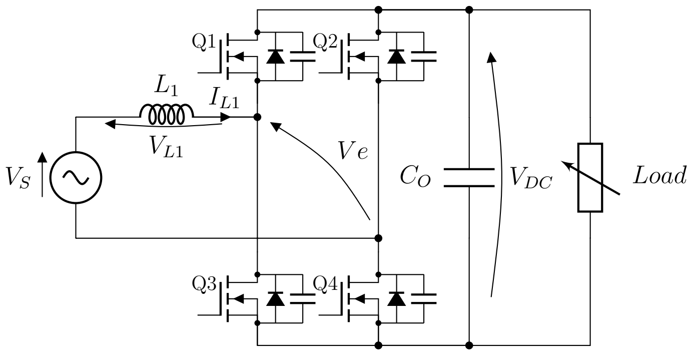


FIGURE 0.0.13 : Cellule élémentaire sélectionnée

les possibilités de contrôle étendues permettant de réduire l'inductance d'entrée et la généricité permettant de construire une seule cellule élémentaire intégrée pouvant être utilisée dans plusieurs applications. La topologie sélectionnée est illustrée dans la Figure 0.0.13.

Association Série

L'association en série, illustrée par la Figure 0.0.14, permet d'utiliser des dispositifs basse tension rendant le silicium (Si) compétitif par rapport aux composants à large bande (WBG). Le convertisseur peut donc être moins couteux. Avec ce type d'association, étant donné que le courant global circule dans plusieurs dispositifs, il est préférable de sélectionner des semi-conducteurs présentant une faible résistance à l'état passant afin de limiter les pertes de conduction. Un inconvénient de la topologie en série est le faible rendement en à faible charge, car toutes les cellules doivent rester opérationnelles. De plus, en cas de défaillance d'un composant, le convertisseur ne peut pas continuer à fonctionner, sauf en cas de défaillance court-circuit, ce qui n'est généralement pas le cas pour les dispositifs implémentés dans les applications de notre gamme de puissance.

Les différents BUS DC sont indépendants. Généralement, des convertisseurs isolés sont requis et connectés à chaque condensateur de BUS. Le secondaire du transformateur est connecté en série ou en parallèle en fonction de l'application et des exigences (courant élevé ou haute tension) [35]. Cette topologie (convertisseur

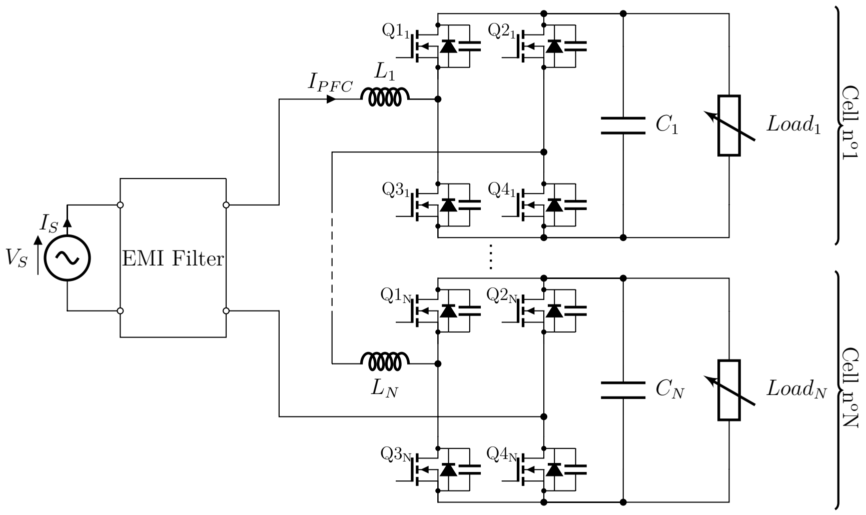


FIGURE 0.0.14 : Topologie de convertisseurs multi-niveaux composée de N cellules

multi-niveau modulaire) est envisagé pour les applications ferroviaires nécessitant de traiter avec une haute tension [36]. Par conséquent, cette configuration implique certaines contraintes du côté du contrôleur. En effet, dans le cas d'un PFC non isolé, cet assemblage n'est pas adapté.

Association Parallèle

La deuxième possibilité est l'association parallèle, voir Figure 0.0.15. Dans ce cas, la tension continue complète est appliquée aux composants. Des matrices avec de faibles pertes de commutation doivent être utilisées, e.g. composants de carbure de silicium (SiC) ou de nitrure de gallium (GaN). Les différentes cellules peuvent facilement être désactivées à faible charge pour maintenir un rendement élevé. Ce comportement est également applicable en cas de défaillance du convertisseur. Il est préférable que le composant défectueux meurt en circuit ouvert, ce qui est généralement le cas. Par conséquent, le convertisseur peut fonctionner en mode dégradé.

La Figure 0.0.16 illustre l'ondulation du courant d'entrée en fonction du nombre de cellules entrelacées (N) et du rapport cyclique (α). Toutes les courbes sont obtenues pour la même fréquence de commutation et la même inductance. La

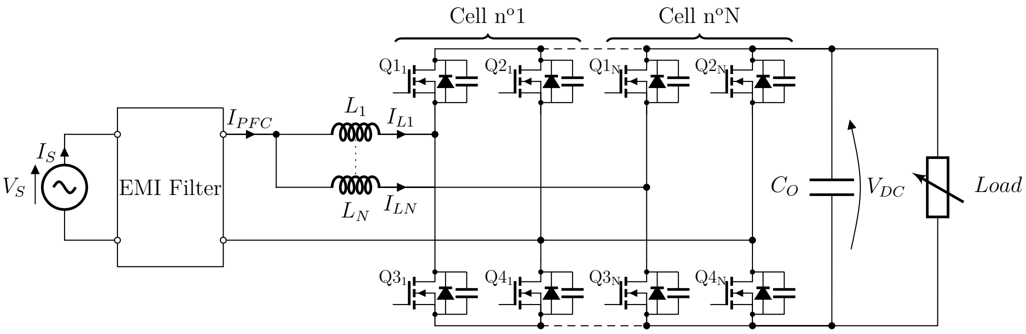


FIGURE 0.0.15 : Topologie de PFC entrelacé composé de N cellules

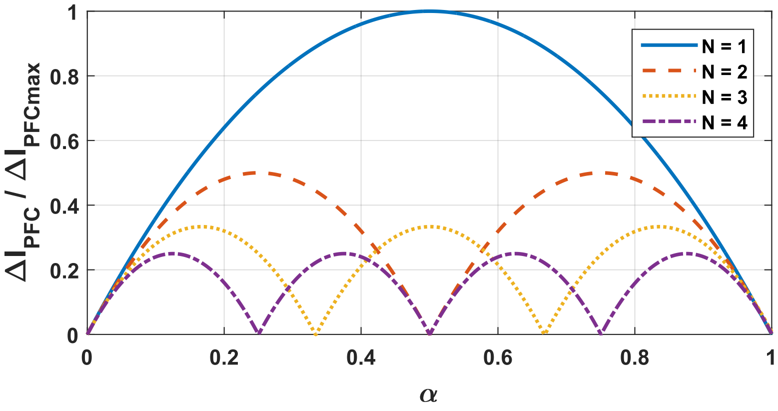


FIGURE 0.0.16 : Impact de l'entrelacement sur l'ondulation du courant d'entrée

réduction du courant d'entrée est obtenue en décalant la porteuse des différentes cellules en fonction de la période de commutation. La somme des différents courants entraine une réduction de l'ondulation globale du courant et une augmentation de la fréquence apparente.

Par conséquent, avec une valeur d'inductance d'entrée constante, l'ondulation du courant est réduite afin que le filtre CEM puisse être réduit. L'autre possibilité est de garder constante l'ondulation du courant d'entrée pour réduire la valeur de l'inductance.

Pour résumer cette partie, contrairement à l'association en série, la topologie parallèle convient mieux aux composants « WBG », les composants passifs peuvent être réduits, l'efficacité peut être améliorée même à faible charge et la disponibilité augmentée. L'association en parallèle présente un meilleur comportement que l'association série pour un fonctionnement à charge partielle. Par conséquent, pour tous ces avantages, l'association en parallèle sera utilisée pour la conception du convertisseur.

Modulation & Mode de Conduction

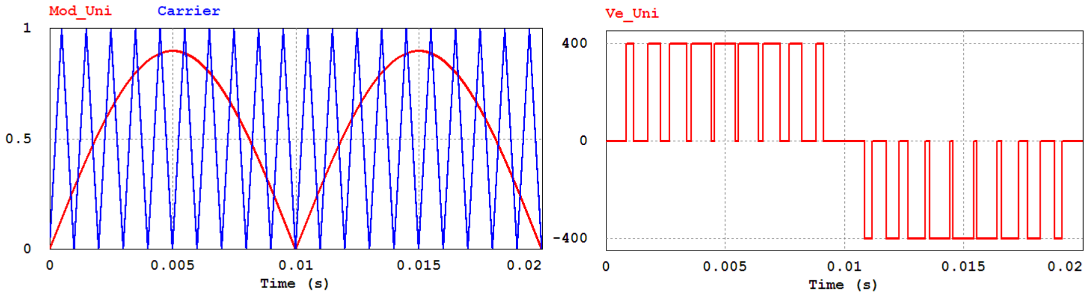
La topologie en pont complet peut être contrôlée avec différentes modulations. Le principe de contrôle influe largement sur la conception du convertisseur. La modulation affecte la taille des composants passifs tels que l'inducteur d'entrée et le filtre CEM, ainsi que les pertes. Deux schémas de modulation sont identifiés, la modulation bipolaire et la modulation unipolaire. La modulation unipolaire peut être obtenue avec deux méthodes. Dans le premier cas, tous les interrupteurs sont contrôlés avec une modulation de largeur d'impulsion haute fréquence (HF PWM). Dans le second cas, une partie des composants est contrôlée à basse fréquence (fréquence du réseau) et d'autres au moyen de HF PWM.

Modulation Unipolaire BF+HF PWM

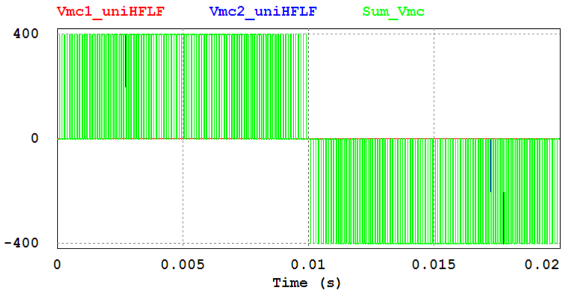
Cette modulation est une modulation à trois niveaux. Avec ce principe, un pont complet est composé de bras haute fréquence (HF) et basse fréquence (BF). Le bras BF fonctionne à la fréquence du réseau, dans ce cas 50Hz. Par conséquent, la fréquence apparente n'est pas le double de la fréquence de commutation (voire la Figure 0.0.17).

Avec ce type de contrôle, l'inductance d'entrée est deux fois plus petite que la modulation bipolaire et deux fois plus élevée que la modulation unipolaire HF. Il est nécessaire d'évaluer si l'entrelacement peut être mis en œuvre sans risquer des déséquilibres et / ou des courants de circulation trop importants. Il est possible de distinguer deux circuits équivalents en fonction du signe de la tension du réseau, voir la Figure 0.0.18.

Des équations sont également dérivées des deux configurations pour analyser l'impact de la commutation sur les courants d'inductances. Les Équations (0.0.9) & (0.0.10) correspondent à la première configuration (voir Figure 0.0.19) et les

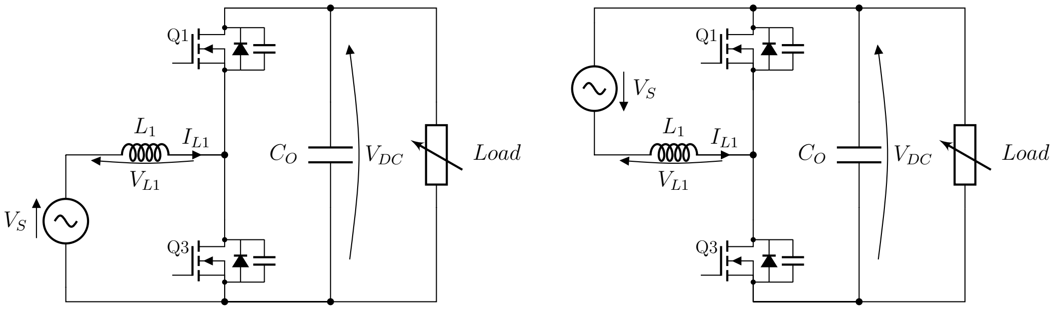


(a) Modulation & Porteuse (b) Forme d'ondes de la tension d'entrée



(c) Tension de mode commun

Figure 0.0.17 : Modulation unipolaire HF-LF



(a) Circuit équivalent pour Vs > 0 (b) Circuit équivalent pour Vs < 0

FIGURE 0.0.18 : Topologie PFC pont-complet

Équations (0.0.11) & (0.0.12) correspondent à la deuxième configuration (voir la Figure **??**).

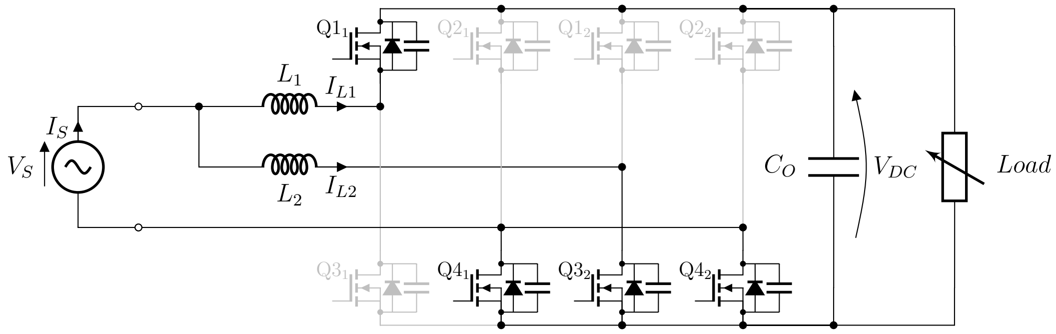
$$I\dot{L}1 = \frac{1}{L} \cdot (Vs - V_{DC}) \tag{0.0.9}$$

$$I\dot{L}2 = \frac{1}{L} \cdot Vs \tag{0.0.10}$$

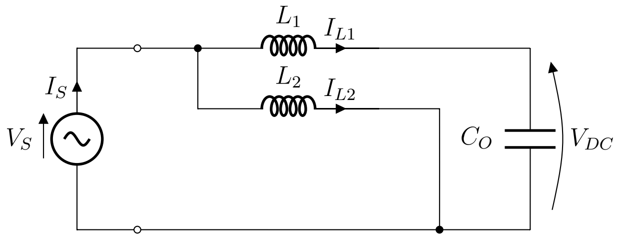
$$I\dot{L}1 = \frac{1}{L} \cdot (Vs - V_{DC}) \tag{0.0.11}$$

$$I\dot{L}2 = \frac{1}{L} \cdot (Vs - V_{DC}) \tag{0.0.12}$$

Il est possible de remarquer avec les équations précédentes pour les deux configurations de commutation qu'il n'y a pas d'impact indésirable des commutations sur le courant de l'autre bars. L'augmentation des pertes ayant un impact sur le système de refroidissement en réduisant la densité de puissance, la réduction du courant circulant est importante. Ce qui suit ne considère que cette modulation. La procédure d'optimisation est mise en œuvre conformément à ce schéma de contrôle.

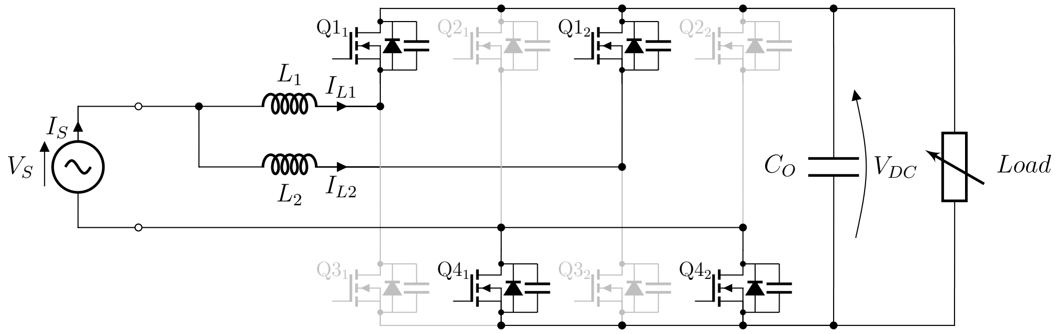


(a) Composants conducteurs

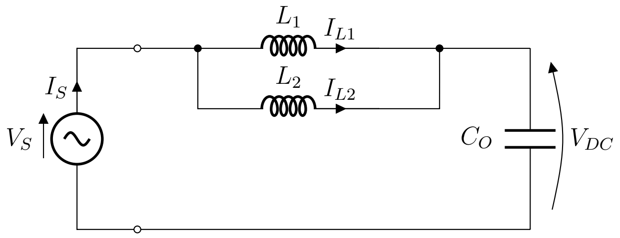


(b) Circuit équivalent

FIGURE 0.0.19 : Configuration de commutation t1 pour modulation LF+HF



(a) Composants conducteurs



(b) Circuit équivalent

FIGURE 0.0.20 : Configuration de commutation t2 pour modulation LF+HF

Mode de Conduction

La conception d'un convertisseur optimal est largement influencée par la modulation et le mode de conduction car les pertes et le volume des composants passifs sont directement impactés. Deux modes de conduction sont étudiés dans ce travail. Le premier correspond au mode de conduction continue (CCM) obtenu avec le PWM LF + HF. Le second est le mode de courant triangulaire (TCM). Ce dernier a récemment suscité de l'intérêt après le « Google little Box Challenge » [37]. Seul le mode de conduction continu est présenté dans ce résumé. Cependant dans les deux cas, le courant d'inductance d'entrée moyen est contrôlé pour être sinusoïdal.

Conduction Continue

Le CCM fonctionne à une fréquence de commutation fixe ($\mathrm{f_{SW}}$) avec un rapport cyclique variable. L'ondulation maximale du courant entrelacé HF (ΔI) est la même quelle que soit la charge. En fonction de la valeur de l'inductance et des formes d'onde présentées dans la Section 3.3.1.3, il est possible de concevoir l'inductance d'entrée (taille du noyau, matériau magnétique, nombre de spires, section de fil...). La valeur dépend de la tension du bus DC, de la fréquence de commutation, de l'ondulation du courant d'entrée et du nombre de cellules entrelacées. L'ondulation de courant maximale est obtenue pour un rapport cyclique α = 0,5. Par conséquent, la valeur de l'inductance d'entrée peut être déterminée par l'Équation (0.0.13).

$$L_{PFC_{CCM}} = \frac{V_{DC}}{4 \cdot N \cdot f_{SW} \cdot \Delta I} \tag{0.0.13}$$

Les formes d'onde typiques de ce type de conduction sont illustrées à la Figure 0.0.21. En règle générale, les pertes de conduction générées par les composants HF sont relativement faibles en raison de la faible ondulation du courant. Cependant, un inconvénient de ce type de contrôle est les pertes de commutation, une partie de la commutation correspond à une commutation dure. De plus, plus l'ondulation du courant d'entrée est faible, plus le filtre DM est

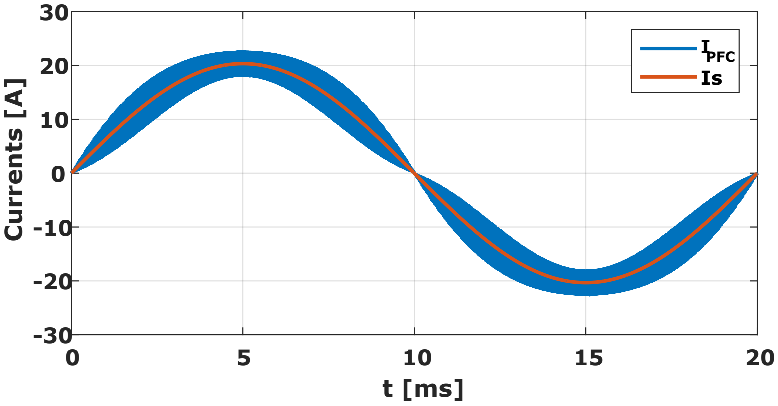


FIGURE 0.0.21 : Forme d'ondes de courant en CCM

petit, mais plus l'inductance d'entrée est élevée. En revanche, l'augmentation de la fréquence de commutation a un impact positif sur la taille de l'inductance d'entrée et du filtre CEM [38].

Par conséquent, il existe un compromis entre la taille de l'inducteur d'entrée et le filtre DM requis. Nous montrons ci-dessous que ce compromis peut être facilement géré grâce à l'entrelacement.

Cadre d'optimisation du convertisseur global

Maintenant que la modulation et la topologie sont introduites, cette partie aborde la méthodologie globale de conception du convertisseur. L'objectif de cette procédure est d'estimer le volume global et les pertes du convertisseur de manière à définir le compromis entre efficacité (η) et densité de puissance (ρ). Ces critères ont été sélectionnés en raison de l'objectif d'intégration. Cependant, cette méthodologie pourrait être adaptée à la conception avec différentes contraintes, telles que le coût ou la masse. La procédure de conception est présentée à la Figure 0.0.22 pour les deux modulations. L'organigramme est composé de trois parties principales : «Semiconducteurs», «Filtre CEM» et «Conception d'inductance». Pour les deux schémas de modulation, il est possible d'agir sur plusieurs variables présentées dans le Tableau 0.2.

Tout d'abord, les formes d'ondes importantes sont déterminées analytiquement pour un ensemble de variables en fonction de la modulation telle que présentée

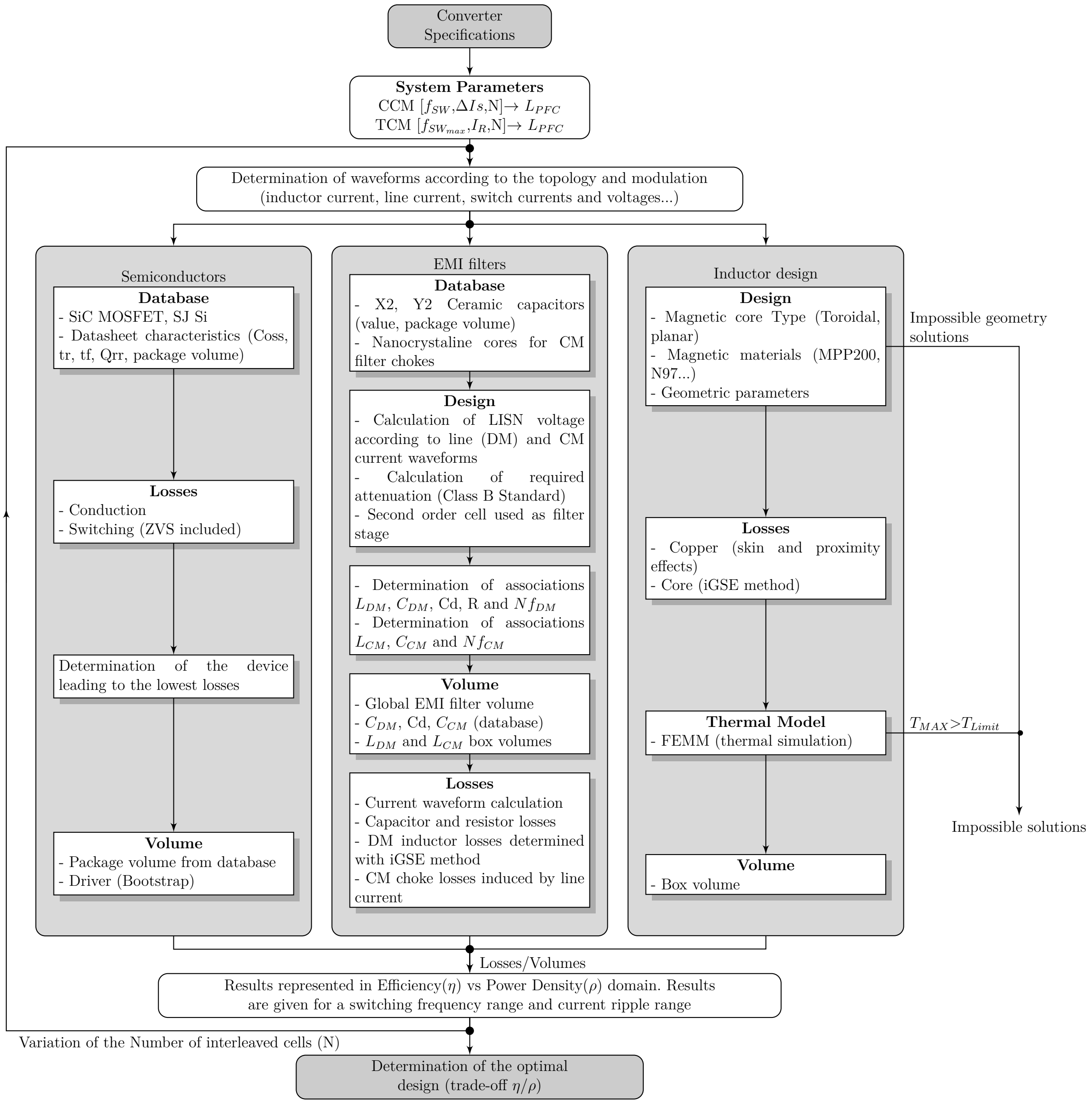


FIGURE 0.0.22 : Procédure globale de design utilisé pour le design du convertisseur

Table 0.2 : Variables d'optimisation

	CCM	TCM
Variables	Switching frequency fsw [kHz]	Maximal switching frequency $\mathrm{fsw}_{\mathrm{MAX}}$ [kHz]
	Input current ripple $\Delta\mathrm{Is}$ [A]	Maximal reverse current I_{R} [A]
	Number of interleaved Cells N	
	Maximal number of DM filter stages $\mathrm{Nf}_{\mathrm{DM}}$	
	Maximal number of CM filter stages $\mathrm{Nf}_{\mathrm{CM}}$	

Table 0.3 : Champ de variation des variables d'optimisation

CCM	TCM
$\mathrm{fsw} = [140\,\mathrm{kHz}\,;\ 300\,\mathrm{kHz}]$	$\mathrm{fsw}_{\mathrm{MAX}} = [350\,\mathrm{kHz}\,;\ 650\,\mathrm{kHz}]$
$\Delta\mathrm{Is} = [2\,\mathrm{A}\,;\ 12\,\mathrm{A}]$	$\mathrm{I}_{\mathrm{R}} = [1\,\mathrm{A}\,;\ 3\,\mathrm{A}]$

précédemment. En ce qui concerne le CCM, la fréquence de commutation et l'ondulation de courant sont utilisées comme variables d'optimisation. Les deux variables système pour le TCM sont la limite supérieure de la fréquence de commutation ($\mathrm{f}_{\mathrm{SW}_{\mathrm{MAX}}}$) et le courant inverse autorisé maximum. La plage de variation de chaque variable est présentée dans le Tableau 0.3. Ces plages de paramètres ont été définies après optimisation préliminaire.

L'optimisation de l'inductance est réalisée en fonction de la géométrie sélectionnée, toroïdale plane ou incorporée, de la valeur de l'inductance et du courant de l'inductance. Plusieurs géométries sont créées, les pertes sont ensuite calculées pour éliminer les solutions thermiquement impossibles.

La sous-partie relative à la conception des filtres CEM prend en compte les filtres à plusieurs étages, le nombre d'étages étant une variable d'optimisation supplémentaire. Les sorties de chaque partie sont les pertes et le volume qui sont utilisés pour sélectionner le convertisseur final. A la fin de la procédure, l'impact de la gestion thermique sur la densité de puissance globale est ajouté. La convection naturelle est considérée dans ce travail. Une étude préliminaire a été réalisée selon les spécifications pour déterminer le volume du dissipateur thermique en fonction des pertes globales. Un coefficient thermique de 5 cm3 / W est une valeur pertinente selon les spécifications : température ambiante de 60 °C et température maximale des composants de 125 °C. Le choix final est fait parmi plusieurs combinaisons possibles d'inductances et de filtres d'entrée.

L'optimisation a été exécutée pour un convertisseur non entrelacé afin d'évaluer la pertinence de la modulation, TCM ou CCM, dans ce type de convertisseur. Deux prototypes ont été construits et évalués. Le premier a été réalisé avec des composants standard, le second est la version intégrée, avec composants intégrés, actifs et passifs. Ces deux prototypes ont été réalisés à partir des résultats complets de la procédure d'optimisation, y compris l'entrelacement avec le mode de conduction continue.

Résultats pour convertisseurs entrelacés

Deux prototypes sont conçus. Le premier est uniquement composé de composants standard et d'inductances planars, ce qui représente une première étape dans l'intégration du circuit imprimé. Le deuxième prototype est la version intégrée. Dans ce cas, la technologie d'incorporation dans le PCB est utilisée. Les composants de puissance, les circuits de d'attaque grille et l'inductance sont intégrés. L'assemblage correspond à une pile de circuits imprimés sur le dissipateur thermique selon une approche modulaire.

Les principales différences dans la procédure d'optimisation de la conception de ces deux convertisseurs sont les technologies d'inductance considérées (planes vs incorporées dans les circuits imprimés) et les références de semi-conducteurs (composants packagés vs puces nues).

La désactivation partielle des cellules a été étudié et influe largement sur la conception du filtre CEM. Faute de temps, il n'a pas été inclus dans la conception de la contrainte de temps du convertisseur discret, mais cette fonctionnalité est incluse dans la version intégrée.

◇

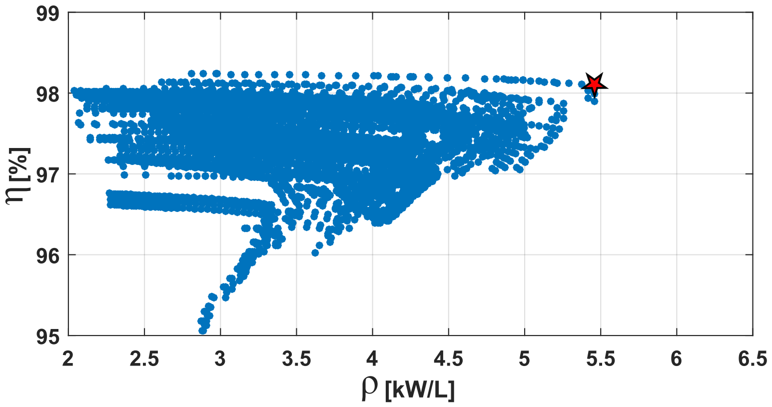
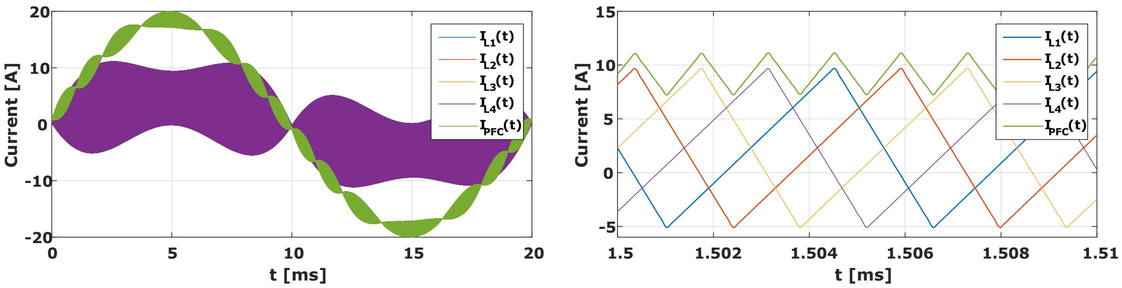


FIGURE 0.0.23 : Résultats d'optimisation du convertisseur discret

Résultats d'optimisation avec des composants discrets

La principale différence entre le convertisseur discret et le convertisseur intégré réside dans le filtre CEM. La désactivation partielles des cellules et le design du filtre CEM sont limités au cas le plus défavorable, $N = 2$. Par conséquent, le filtre CEM implémenté ne permet de se conformer à la norme qu'avec les quatre cellules opérationnelles. La Figure 0.0.23 présente les résultats de l'optimisation dans le domaine ρ vs η avec un coefficient thermique égal à 5cm^3/ W. L'impact des variables principales (N [2 ; 5], f_{SW} [140 kHz ; 300 kHz] et ΔI [2 A ; 12 A]) est analysé pour le convertisseur intégré.



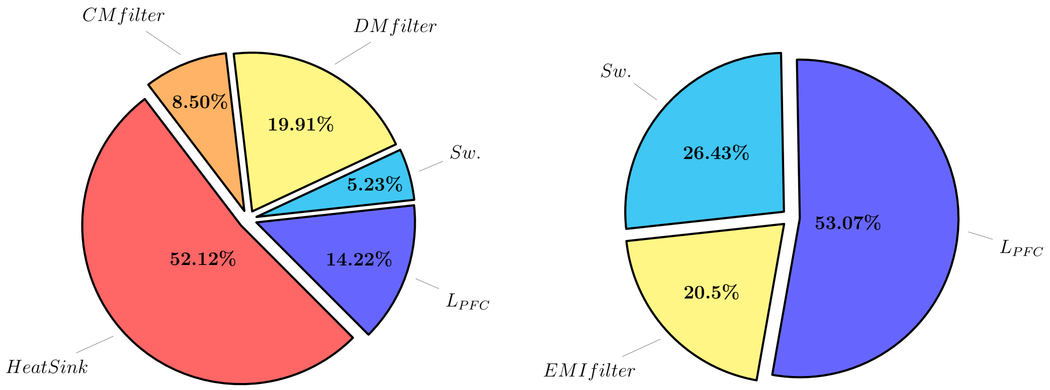
(a) Courants à la fréquence du réseau (b) Courants à la fréquence de commutation

FIGURE 0.0.24 : Formes d'ondes de courants du convertisseur discret

Le convertisseur sélectionné atteint un rendement de 98,1 % et une densité de puissance de 5,5 kW / dm^3 (somme du volume de chaque composant). Le convertisseur optimal correspond à quatre cellules entrelacées commutant à

180 kHz avec une ondulation de courant d'entrée de 4 A. Cette configuration peut être expliquée en regardant les formes d'onde obtenues (voir la Figure 0.0.24). L'augmentation du nombre de cellules entrelacées induit une réduction de la valeur requise pour l'inductance d'entrée. De plus, le courant moyen (composante 50 Hz) dans chaque cellule est réduit, ainsi les pertes sont également partagées. Plus le nombre de cellules entrelacées est élevé, plus la fréquence apparente est élevée, donc plus le filtre CEM est petit. Le deuxième facteur est la fréquence de commutation. Plus la fréquence de commutation est élevée, plus l'inducteur d'entrée est petit. Cependant, une augmentation excessive de la fréquence de commutation induit des pertes plus importantes. L'ondulation de courant a un impact sur les pertes dans les semi-conducteurs et les inductances. Une ondulation de courant élevée induit des pertes de conduction plus élevées, mais en contrepartie, les pertes de commutation sont réduites et les inductances sont plus petites.

Par conséquent, la procédure d'optimisation conduit à cette configuration particulière de convertisseur multicellulaire fonctionnant à haute fréquence avec une ondulation de courant importante. Le convertisseur sélectionné peut fonctionner en ZVS pendant toute la période du réseau. Le convertisseur avec contrôle CCM présente l'avantage d'une commutation douce, comme le TCM, mais les inconvénients du contrôle de la fréquence de commutation variable et de la détection du passage par zéro sont évités.



(a) Volume (b) Pertes

Figure 0.0.25 : Répartition volumes et pertes du convertisseur discret

TABLE 0.4 : Détails du convertisseur discret

Design for CCM @3.3kW					
General	η	98.1 %	Volume	Total	599.55 cm^3
	ρ	5.5 kW/dm^3		L_{PFC}	4 × 21.31 cm^3
	N	4		DM filter	119.43 cm^3
	f_{SW}	180 kHz		CM filter	51.02 cm^3
	ΔI	4 A		Sw.+Driver	31.36 cm^3
	L_{PFC}	34.72 µH		Heat sink	312.5 cm^3
	Devices	2//C3M0065090J			
	Nb EMI filter stages	Nf_{DM}=2, Nf_{CM}=2			
	L_{DM}	16.12 µH			
	C_{DM}/C_D	[0.5 µF, 0.33 µF]	Losses	Total	62.5 W
	R_D	[11.56 Ω, 14.32 Ω]		L_{PFC}	33.17 W
	L_{CM}	0.225 mH		Switches	16.52 W
	C_{CM}	[20.3 nF, 12.7 nF]		EMI filter	12.81 W

Les détails concernant le convertisseur sont présentés dans le Tableau 0.4 et illustrés à la Figure 0.0.25. Notez que le dispositif à semi-conducteur sélectionné correspond à deux MOSFET SiC en parallèle.

L'efficacité du convertisseur pour toute la plage de puissance est présentée dans la Figure 0.0.26. La baisse d'efficacité est significative pour une puissance inférieure à 1,5 kW. C'est la principale motivation pour implémenter la désactivation partielle des cellules dans la conception du convertisseur intégré.

Le filtre CEM est également validé en vérifiant le spectre de tension LISN obtenu par le modèle analytique et par des simulations PSIM. Les résultats obtenus pour le mode différentiel sont présentés sur la Figure 0.0.27. Le modèle analytique et les résultats des simulations PSIM sont équivalents. Les atténuations obtenues pour la fréquence de dimensionnement (720 kHz) sont les mêmes. Par conséquent, le modèle est validé par les simulations de circuit.

Résultats d'optimisation avec des composants enterrés

Les résultats obtenus avec le convertisseur intégré sont influencés par la désactivation des cellules utilisée pour maintenir un rendement élevé à faibles

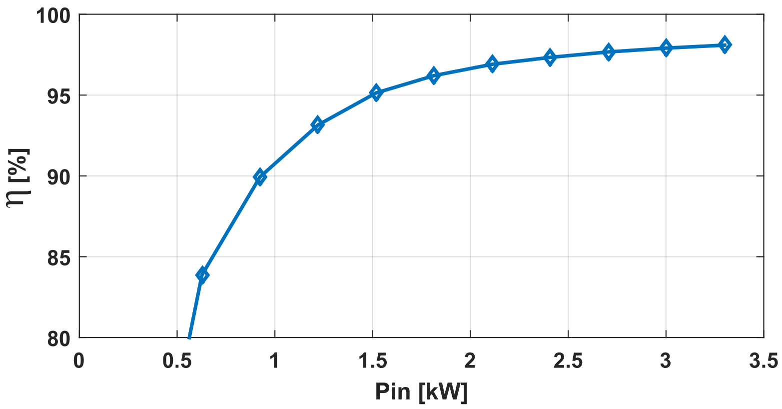
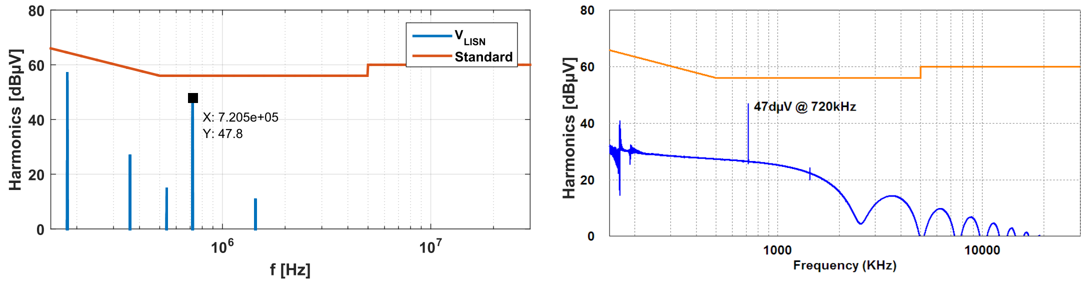


FIGURE 0.0.26 : Efficacité calculée du convertisseur discret



(a) Calculs analytique

(b) Simulation

FIGURE 0.0.27 : Spectre DM du RSIL pour un convertisseur CCM entrelacé (N = 4)

charges. Le filtre CEM d'entrée est conçu pour garantir la conformité à la norme pour toute la plage de puissance. Par conséquent, il est conçu pour le cas le plus défavorable de fonctionnement correspondant au plus petit nombre de cellules entrelacées (N = 2). Les formes d'ondes sont recalculées pour la conception du filtre EMI. La technologie à inductance mise en œuvre pour la version intégrée est du type toroïdal enfoui, car elle représente un pas en avant dans l'intégration des circuits imprimés pour cette gamme de puissance. La Figure 0.0.28 représente les résultats de l'optimisation et l'impact des différents paramètres, la gestion thermique est également incluse, le coefficient est également de 5 cm^3/W.

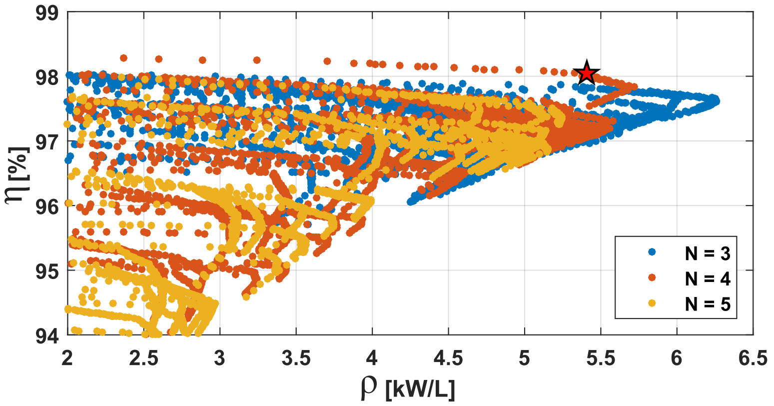
Le convertisseur sélectionné correspond à la même configuration que le convertisseur discret. Quatre cellules entrelacées fonctionnent à 180 kHz et l'ondulation de courant est égale à 4 A. Par conséquent, les formes d'onde de courant sont identiques à celles présentées dans la Figure 0.0.24. Comme mentionné

Table 0.5 : Détails du convertisseur intégré

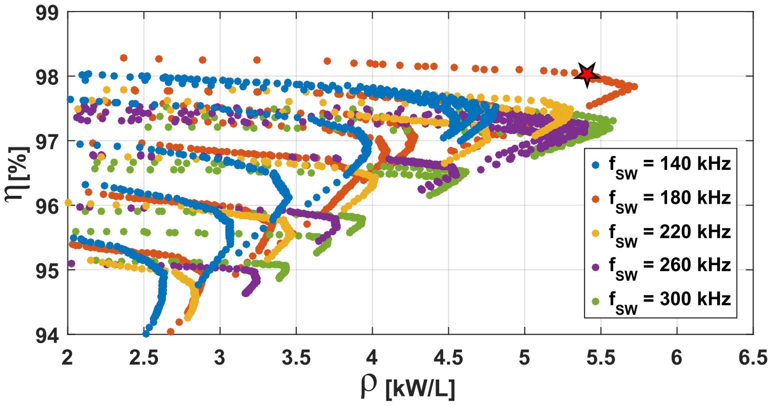
Design for CCM @3.3kW					
General	η	98.01 %	Volume	Total	609.52 cm^3
	ρ	5.41 $\mathrm{kW/dm}^3$		L_{PFC}	4 × 14.88 cm^3
	N	4		DM filter	151.36 cm^3
	f_{SW}	180 kHz		CM filter	61.61 cm^3
	ΔI	4 A		Sw.+Driver	8.04 cm^3
	L_{PFC}	34.72 µH		Heat sink	329 cm^3
	Devices	2//CPM3-0900-0065B			
	Nb EMI filter stages	Nf_{DM}=4, Nf_{CM}=3			
	L_{DM}	7.95 µH			
	C_{DM}/C_D	[0.33 µF,0.282 µF,0.188 µF,0.094 µF]	Losses	Total	65.8 W
	R_D	[10 Ω, 10.88 Ω, 13.33 Ω, 18.85 Ω]		L_{PFC}	32.99 W
	L_{CM}	0.544 mH		Switches	17.04 W
	C_{CM}	[19.2 nF, 12.7 nF, 6.5 nF]		EMI filter	15.77 W

ci-dessus, cette configuration induit un fonctionnement en ZVS pendant toute la période du réseau, réduisant ainsi les pertes dans les semi-conducteurs. En termes de densité de puissance, l'augmentation de la fréquence permet de réduire les composants magnétiques, tels que l'inducteur d'entrée et le filtre EMI. Cependant, la fréquence de commutation ne peut pas être augmentée à cause des pertes HF, par ex. effets de peau et de proximité, dans les inductances. Le Tableau 0.5 présente les détails du convertisseur. Le convertisseur sélectionné atteint une efficacité de 98,01 % et une puissance de 5,4 kW / L, ce qui est légèrement inférieur à la version discrète. Cependant, le filtre EMI pour le convertisseur intégré est conçu pour le cas le plus défavorable entrainant une augmentation de volume. Les pertes et les répartitions de volume sont présentées dans la Figure 0.0.29.

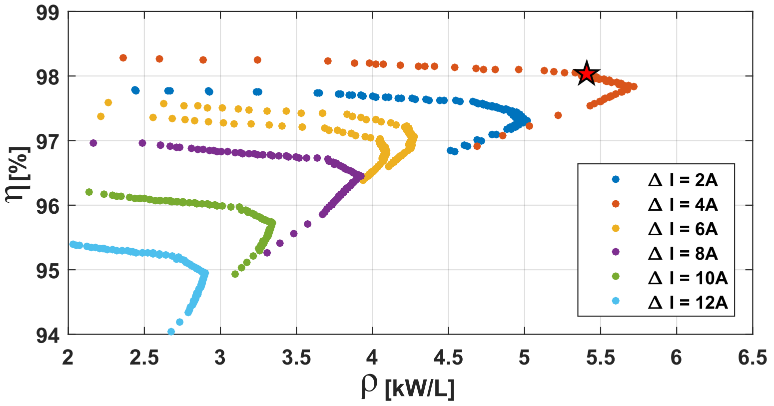
L'efficacité du convertisseur est calculée pour différents nombres de cellules en fonctionnement afin de mettre en évidence les avantages de la désactivation des cellules à faibles charges. Les courbes de rendement pour la plage de puissance allant de 10% à 100% de la charge nominale sont données dans la Figure 0.0.30.



(a) Impact de N



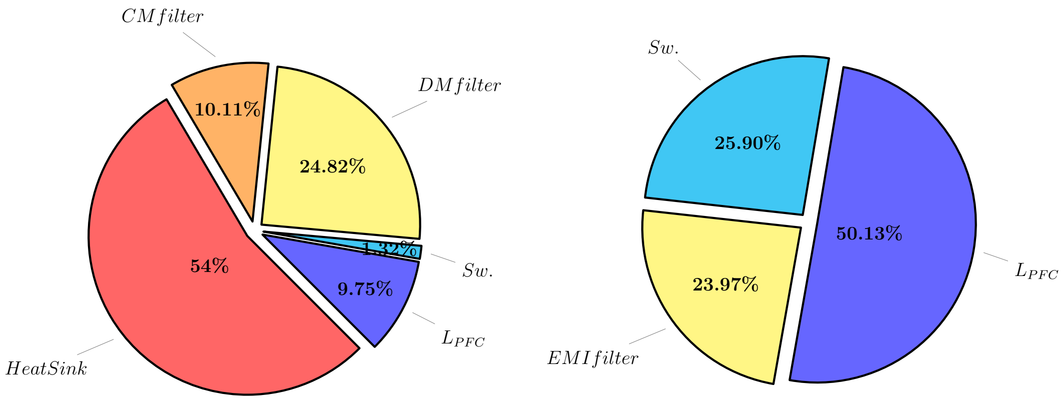
(b) Impact de f_{SW} pour $N = 4$



(c) Impact de ΔI pour $N = 4$ et $f_{SW} = 180 kHz$

FIGURE 0.0.28 : Résultats d'optimisation du convertisseur intégré

◇



(a) Volume (b) Pertes

FIGURE 0.0.29 : Répartition volumes et pertes du convertisseur intégré

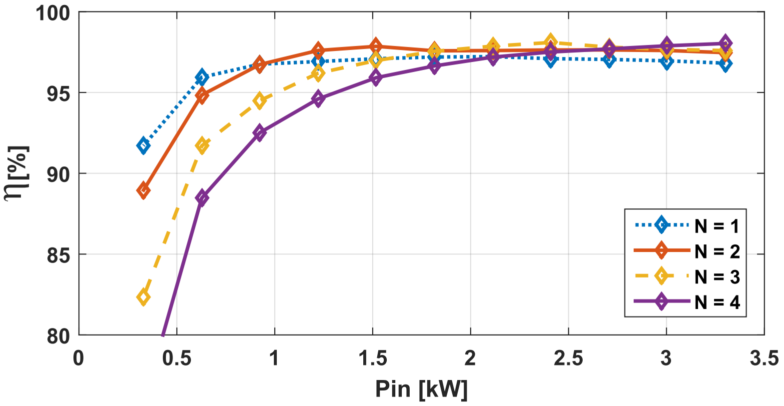


FIGURE 0.0.30 : Efficacité calculée analytiquement pour le convertisseur intégré pour un nombre différent de cellules opérationnelles

Le nombre minimal de cellules en fonctionnement sélectionné vaut deux. La configuration avec N = 2 peut être utilisée pour des puissances inférieures à 1,7 kW, puis N = 3 pour des puissances comprises entre 1,7 kW et 2,6 kW, le convertisseur complet avec les quatre cellules imbriquées est utilisé pour des puissances supérieures à 2,6 kW.

La configuration avec N = 1 est uniquement illustrée par le fait qu'il n'est pas pertinent de l'utiliser par rapport à N = 2. En effet, le gain d'efficacité n'est pas significatif pour compenser l'inconvénient induit par la perte d'entrelacement conduisant à un filtre CEM plus grand.

Par la suite deux prototypes correspondant aux résultats obtenus pour des composants discrets, et intégrés sont réalisés. Les performances de chacun des convertisseurs sont évaluées, le convertisseur discret est notamment utilisé pour valider certaines hypothèses résultant de l'optimisation, particulièrement le fait de toujours fonctionner en ZVS. Le convertisseur intégré est lui utilisé comme preuve de concept, il permet de valider la faisabilité de ce type de convertisseurs fabriqué grâce à l'enterrement de composants hétérogènes, encore trop peu étudiés.

Méthodologie de conception adaptée au PPB

Pour rappel, les principaux objectifs de ce projet sont une densité de puissance et un niveau d'intégration élevés. Comme il est présenté dans ce document, il est important de gérer la puissance pulsante du côté DC dans des application PFC monophasé. La méthode classique utilise des condensateurs électrolytiques qui ne sont pas compatibles avec l'objectif de densité de puissance élevée. Par conséquent, l'utilisation d'un condensateur électronique ou « Power Pulsating Buffer » (PPB) est presque obligatoire pour surmonter ce problème. Parmi les différentes topologies étudiées le type « Buck » est considéré comme la solution la plus appropriée pour ce projet. En effet, le condensateur requis est plus petit qu'une topologie symétrique. De plus, les mêmes interrupteurs que le PFC peuvent être utilisés car ils doivent résister à la tension du bus DC, ce qui n'est pas le cas avec une topologie Boost. Un autre point important est la similarité avec la topologie du PFC. Tout comme le PFC, le PPB est composé de deux interrupteurs et d'une inductance au point milieu. Cela correspond aux composants élémentaires de l'électronique de puissance. La procédure d'optimisation de PFC est simplement adaptée à la topologie PPB.

Adaptation de la procédure d'optimisation

Comme mentionné ci-dessus, la procédure d'optimisation PPB est similaire à l'optimisation du PFC. Il est composé de trois parties : la sélection du semi-conducteur, la conception de l'inductance et la conception du condensateur

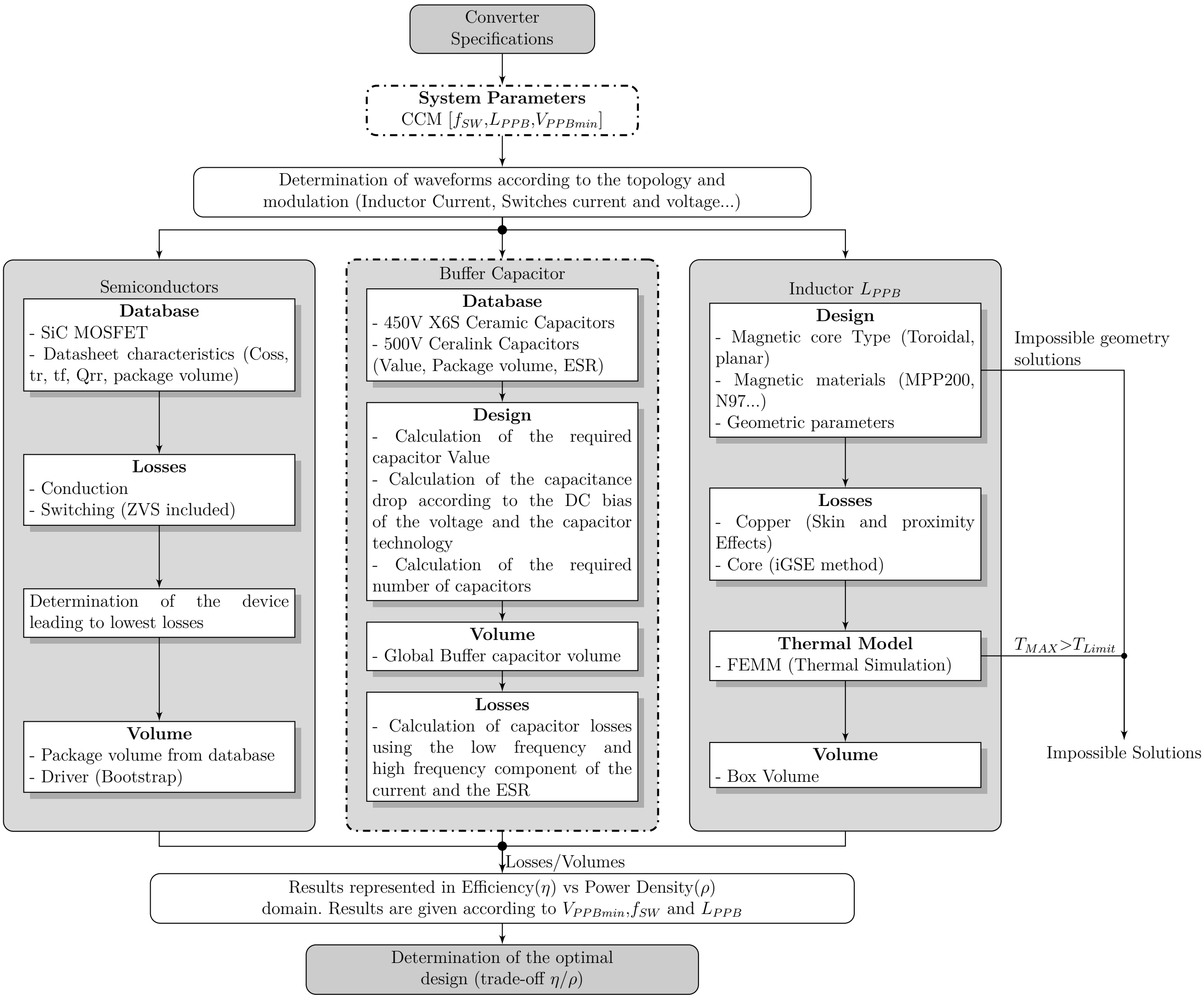


FIGURE 0.0.31 : Procédure d'optimisation implémentée pour le PPB Buck. Les parties en pointillés représentent les différences avec l'optimisation du PFC

de stockage. La figure 0.0.31 présente l'organigramme de conception. Les trois variables d'optimisation sont présentées dans le tableau 0.6. En fin de procédure, l'évaluation des pertes permet de déterminer le volume du radiateur. Cela met en évidence l'impact de la gestion thermique. Le coefficient de 5 cm^3 / W en convection naturelle est également pris en compte. La contrainte thermique est une température ambiante de 60 °C et une température maximale des puces est de 125 °C.

L'identification des variables d'optimisation est réalisée en fonction de l'application et de la topologie du convertisseur. Dans ce cas, le PPB est connecté en parallèle à un condensateur sur le bus continu (Co) de seulement 20 µF, utilisé principalement pour filtrer les composants haute fréquence. La tension continue est supposée être contrôlée par l'étage du redresseur à une valeur de 400V. Pour la procédure d'optimisation, les trois variables sont : la fréquence de commutation ($\mathrm{f_{SW}}$) du PPB, sa valeur d'inductance ($\mathrm{L_{PPB}}$) et la tension minimale du condensateur tampon ($\mathrm{V_{PPBmin}}$). La valeur de l'inductance a un impact sur l'ondulation de courant. L'ondulation actuelle a un impact sur les pertes de conduction, mais les pertes en commutation peuvent être considérablement réduites si un fonctionnement en ZVS est obtenu.

La valeur du condensateur peut être déterminée en fonction de la puissance fluctuante maximale et de l'oscillation de tension. Avec la topologie Buck, la tension aux bornes du condensateur doit toujours être inférieur à la tension continue. Par conséquent, la tension maximal ($\mathrm{V_{PPBmax}}$) est défini sur $0,93 \cdot V_{DC}$ pour éviter les problèmes de contrôle. La tension minimale permet de déterminer la valeur du condensateur, (Équation 0.0.14).

TABLE 0.6 : Plage de variation des variables d'optimisation du PPB

CCM
fsw = [40 kHz ; 280 kHz]
$\mathrm{L}_{PPB} = [10\,\mu H; 80\,\mu H]$
$\mathrm{V}_{PPB_{MIN}} = [100\,V; 350\,V]$

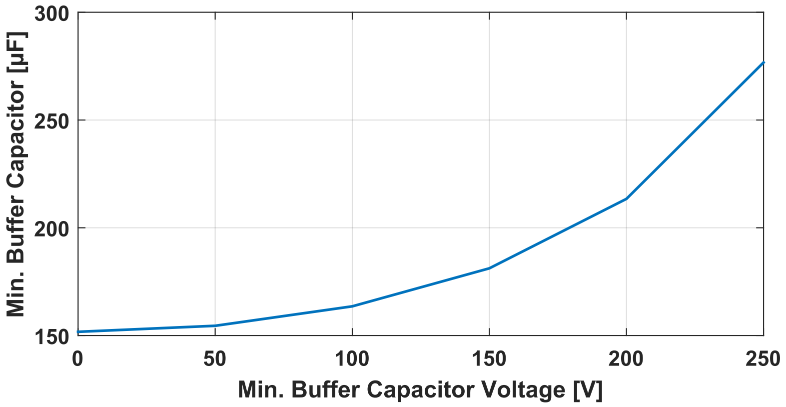


FIGURE 0.0.32 : Variation de la capacité de filtrage

$$C_{PPB} = \frac{2 \cdot P_{DC}}{\omega \cdot (V^2_{PPBmax} - V^2_{PPBmin})} \qquad (0.0.14)$$

La variation de la capacité requise en fonction de la tension minimale est présentée dans la Figure 0.0.32. Elle montre que les valeurs de condensateur pour des tensions minimales comprises entre 0 V et 100 V restent pratiquement inchangées : $\mathrm{C_{PPBmin}} = 152\,\mu\mathrm{F}$ et $\mathrm{C_{PPB}}(100\mathrm{V}) = 163\mu\mathrm{F}$. Par conséquent, le volume du condensateur est presque équivalent dans les deux cas. Cependant, il est préférable de conserver une certaine quantité d'énergie dans le condensateur, dans le cas de variations de charge. En outre, plus la variation de tension à travers le condensateur est élevée, plus le courant qui le traverse est élevé. Ce courant traverse également l'inductance, ce qui affecte négativement les pertes de conduction.

Connaissant la capacité tampon requise, les formes d'onde de tension peuvent être déterminées. La tension aux bornes du condensateur est donnée par l'Équation 5.2.8 avec “K” le facteur de sécurité sélectionné pour la tension maximale du condensateur (dans ce cas, K = 0,93). L'Équation 5.2.8 est dérivée de l'expression de l'énergie stockée dans le condensateur en supposant un comportement idéal du PFC. La puissance absorbée du PPB est égale à la puissance de pulsation.

$$W(t) = W_{init} + \int P_{Puls}(t)dt \tag{0.0.15}$$

$$W(t) = W_{init} - P_{DC} \cdot \int \cos(2\omega t)dt \tag{0.0.16}$$

$$W(t) = W_{init} - \frac{P_{DC}}{2\omega} \cdot \sin(2\omega t) \tag{0.0.17}$$

$$W_{max} = W_{init} + \frac{P_{DC}}{2\omega} \tag{0.0.18}$$

$$W_{init} = \frac{1}{2} \cdot C_{PPB} \cdot V_{PPB,max}^2 - \frac{P_{DC}}{2\omega} \tag{0.0.19}$$

$$W(t) = \frac{1}{2} \cdot C_{PPB} \cdot V_{PPB}^2(t) = \frac{1}{2} \cdot C_{PPB} \cdot V_{PPB,max}^2 - \frac{P_{DC}}{2\omega} \cdot (1 + \sin(2\omega t)) \tag{0.0.20}$$

$$V_{PPB}(t) = \sqrt{(K \cdot V_{DC})^2 - \frac{P_{DC}}{C_{PPB} \cdot \omega} \cdot (1 + \sin(2\omega t))} \tag{0.0.21}$$

La Figure 0.0.33 présente les formes d'onde de tension pour différentes valeurs de condensateur. La tension du condensateur est ensuite utilisée pour calculer le courant dans l'inductance avec la même méthode que pour le PFC. Le schéma simplifié correspondant est présenté sur la Figure 0.0.34. La tension de modulation est contrôlée selon l'équation de la tension $\mathrm{V_{PPB}(t)}$ normalisée à la tension continue, voir l'Équation 0.0.22. La loi des maille permet de déterminer la tension de l'inducteur, le courant est ensuite calculé dans le domaine fréquentiel.

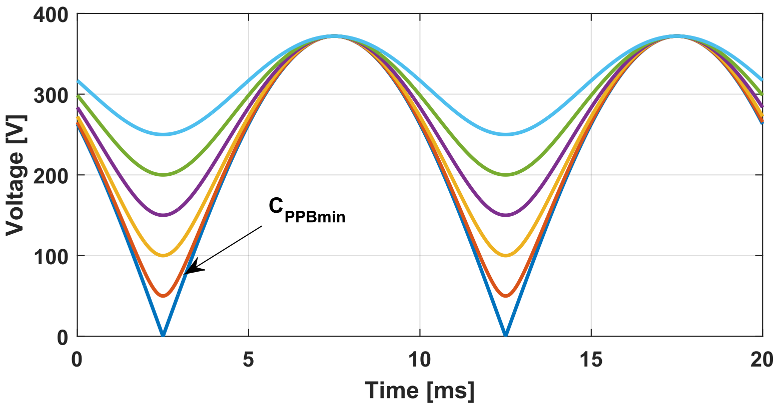


FIGURE 0.0.33 : Tension au bornes du condensateur de filtrage

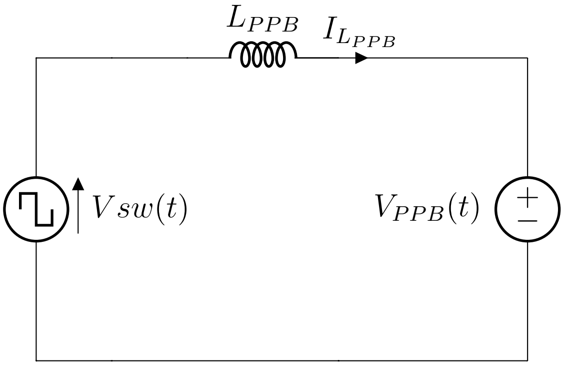


FIGURE 0.0.34 : Circuit simplifié du convertisseur PPB

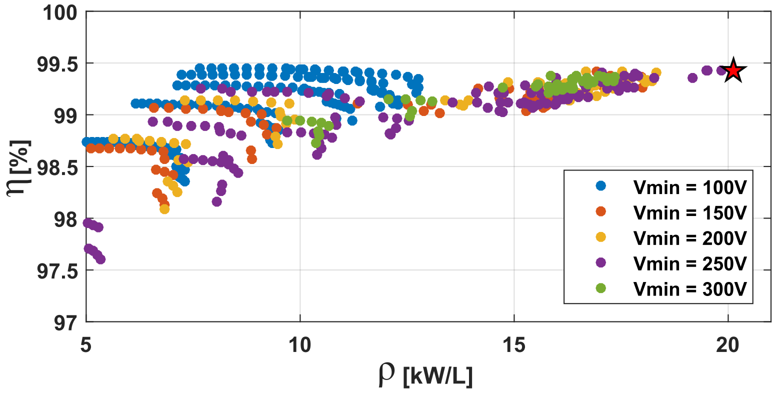
$$\alpha_{PPB}(t) = \frac{1}{V_{DC}} \cdot \sqrt{(K \cdot V_{DC})^2 - \frac{P_{DC}}{C_{PPB} \cdot \omega} \cdot (1 + \sin(2\omega t))} \tag{0.0.22}$$

Résultats de la procédure d'optimisation

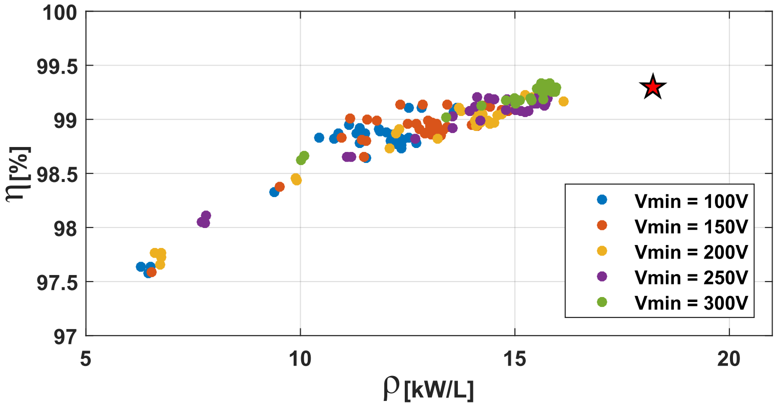
Comme pour le PFC, plusieurs configurations de convertisseur sont évaluées et les résultats sont présentés dans le domaine de la densité de puissance (ρ) par rapport au rendement (η). L'efficacité équivalente est calculée en fonction de la puissance d'entrée du PFC ($\mathrm{Pin_{PFC}}$) et des pertes calculées du PPB ($\mathrm{P_{PPB}}$), voir l'Équation 5.3.1.

$$\eta_{PPB} = \frac{Pin_{PFC} - P_{PPB}}{Pin_{PFC}} \tag{0.0.23}$$

Le convertisseur est optimisé pour la puissance nominale. Cela correspond au courant le plus élevé qui traverse les semi-conducteurs et les composants passifs. Les résultats pour les deux combinaisons possibles sont présentés dans la Figure 0.0.35. La première correspond à des condensateurs X6S associés à une inductance planaire "X6S-planar". La seconde est la combinaison de condensateurs X6S et d'une inductance avec des noyau insérés dans le PCB, «toroïdal intégré X6S-PCB». Les deux sont présentés avec le même coefficient thermique 5 cm^3 / W. Plus l'oscillation de tension est élevée plus le courant traversant le condensateur est élevé. Par



(a) Condensateurs X6S/inductance planar avec un coefficient thermique de 5 cm^3/W.



(b) Condensateur X6S/Inductance toroid enterrés dans le PCB avec un coefficient thermique de 5 cm^3/W.

FIGURE 0.0.35 : Résultats de l'optimisation présentés dans le plan densité de puissance vs. efficacité

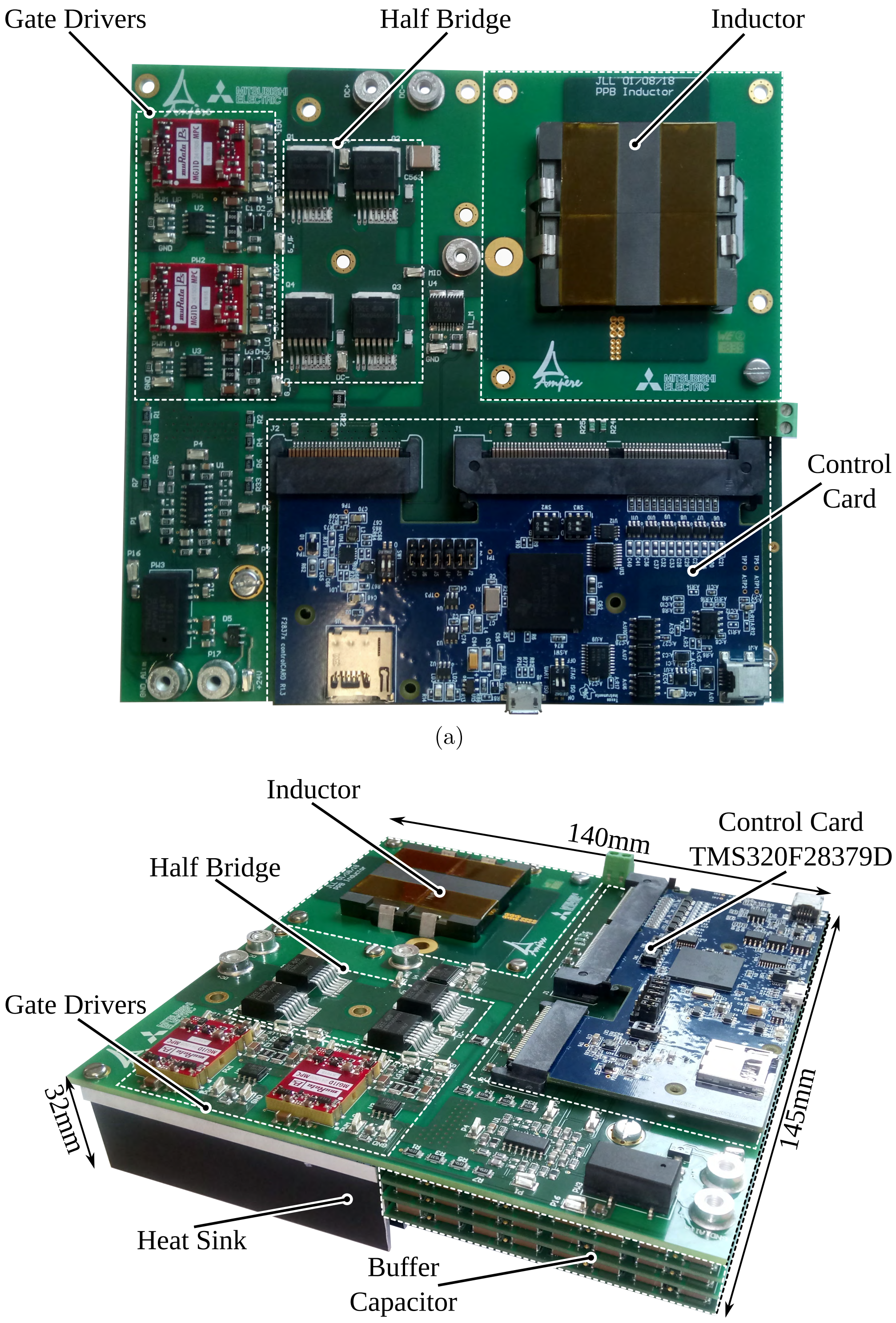
conséquent, le choix de la tension minimale du condensateur correspond à un compromis entre la taille du condensateur et les pertes globales. La fréquence de commutation et la valeur de l'inductance peuvent être considérées comme des variables d'optimisation utilisées pour compenser les pertes (principalement dans les semi-conducteurs et l'inductance) et le volume de l'inductance.

Les deux convertisseurs sélectionnés, avec les deux technologies d'inductance, correspondent aux solutions les plus denses car l'efficacité estimée est élevée, supérieure au critère minimal choisi pour le PFC (98 %). Les deux solutions atteignent une efficacité de 99.45 %, une densité de puissance de 20.12 kW/dm^3

et 99.3 %, de 18.22 kW/dm^3 pour le toroïdal plat et le toroïdal incorporé dans le circuit imprimé. L'optimum est le même dans les deux cas, la tension minimale est égale à 250 V, le condensateur est donc égal à 277 µF, la valeur de l'inductance est de 20 µF et le convertisseur commute à 140 kHz. En analysant la répartition des pertes, les pertes générées par le condensateur sont négligeables par rapport aux semi-conducteurs et à l'inductance. La principale différence entre les deux PPB provient de l'inductance. Le toroïdal PCB est plus petit que le planar, mais les pertes sont plus élevées. Ainsi, la gestion thermique est sérieusement affectée et rend la solution intégrée aux PCB plus volumineuse que la solution planar.

Réalisation du convertisseur

Le prototype de PPB utilisant la technologie Planar est construit. Malheureusement, en raison du manque de temps et des délais de fabrication assez longs, le prototype n'utilise pas l'intégration PCB. De plus, en raison de problèmes techniques rencontrés avec le gate-driver implémenté sur le PFC, une autre structure est implémentée. Il comprend des alimentations isolées de Murata (MGJ1D241505MPC) et des buffers haute vitesse de Silicon Lab (SI8271BB-IS). La mise en œuvre du convertisseur est présentée dans la Figure 0.0.37. Les analyses du volume du prototype par rapport à la procédure sont présentées dans la Figure 0.0.36. Toutes les pièces incluses dans la procédure affichent un volume plus important dans le prototype. La principale différence vient de l'utilisation de semi-conducteurs packagés et d'une autre structure de gate-driver. L'inductance est plus grosse en raison de l'utilisation de noyaux discrets qui présentent de légères différences de dimensions, en particulier de hauteur. Les interconnexions entre l'inductance, la carte principale et le condensateur augmentent également le volume. Le banc de condensateurs est composé de trois PCB empilés. Par conséquent, l'épaisseur de chaque PCB augmente le volume. La procédure d'optimisation additionne uniquement le volume de chaque composant. Avec cette réalisation, les condensateurs ne sont pas collés les uns aux autres. Un espace est ajouté pour faciliter le placement et le processus de soudage. Souder tous les condensateurs ensemble pour former un bloc unique est possible mais assez compliqué, et rend également plus difficile l'interconnexion avec d'autres parties



(a)

(b)

FIGURE 0.0.36 : Prototype du convertisseur PPB

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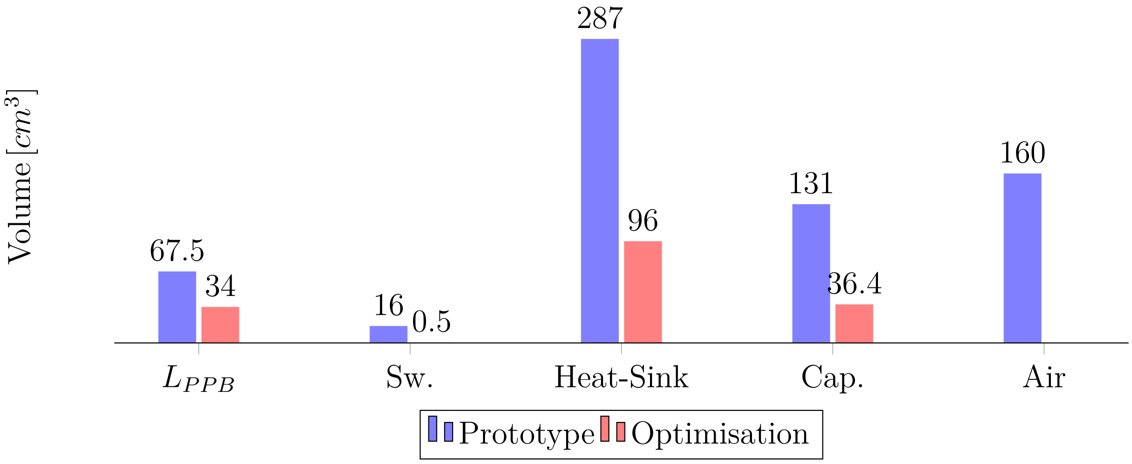

Figure 0.0.37 : Comparaison des volumes obtenus avec la procédure et le prototype

du convertisseur. La solution de circuit imprimé est l'option la plus rapide et la plus fiable. Le radiateur sélectionné est également plus grand que prévu. En effet, le choix d'un radiateur avec une épaisseur de semelle suffisante pour une opération d'usinage, associé à la longueur d'ailette souhaitée est impossible en référence standard. Par conséquent, le dissipateur sélectionné a des ailettes plus longues que prévu, ce qui entraine un volume plus important.

Ainsi conclu le résumé étendu de cette thèse. Les différents chapitres sont présentés succinctement mettant l'accent sur les points importants, comme par exemple les procédures d'optimisation ou bien la réalisation des différents prototypes.

♠

Design, Modelling and Evaluation of a Bidirectional Highly Integrated AC/DC Converter

“Il vaut mieux mobiliser son
intelligence sur des conneries
que mobiliser sa connerie sur
des choses intelligentes”"

*(Jacques Rouxel
"Les Shadocks")*

Abstract

Nowadays, the green energy sources are replacing fossil energies. To assure proper interconnections between all these different electrical facilities, power electronics is mandatory. The main requirements of next generation converters are high efficiency, high power density, high reliability and low-cost. The Printed Circuit Board (PCB) integration of dies and/or passives is foreseen as a promising, low-cost and efficient approach. The manufacturing time and cost of power converters can be drastically reduced. Moreover, integration allows the converter performances to be improved. For this purpose, an original 3D folded power inductor concept using PCB technology is introduced. It is low cost for mass production and presents good reproducibility. A partial milling of the PCB is used to allow bending and building the inductor winding. Prototypes are designed through an optimisation procedure. Electrical and thermal tests are performed to validate the applicability in power converters.

The development of an optimisation procedure for highly integrated converters, using PCB embedding, is presented. All important choices, facilitating the PCB integration, e.g. reduction of passive components, are presented. It includes the selection of the suitable converter topology with the associated modulation. The design procedure and implemented analytical models are introduced. It results in four interleaved full-bridges operating with low (50 Hz) and high (180 kHz) frequency legs. The configuration allows high current ripple in the input inductors inducing zero voltage switching (ZVS) for all the semiconductors, and for a complete grid period. The impact of high current ripple on the EMI filter is compensated by the interleaving. Two prototypes of a 3.3 kW bidirectional AC/DC converters are presented, theoretical and practical results are discussed.

To further increase the power density of the overall system, a Buck power pulsating buffer is investigated. The optimisation procedure is derived from the procedure implemented for the AC/DC converter. The result favours an original approach, where the converter also operates with ZVS along the entire main period at a fixed switching frequency. The selected technologies for prototyping are integration friendly as ceramic capacitors and PCB based inductors are implemented in the final prototype presented in this thesis manuscript.

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List of Symbols and Abbreviations

Abbreviations

B2G	Building to Grid
CCM	Continuous Current Mode
CM	Common Mode
DCM	Discontinuous Current Mode
DM	Differential Mode
DUT	Device Under Test
ECPE	European Center for Power Electronic
ESR	Equivalent Series Resistance
EVs	Electrical Vehicles
FFT	Fast Fourier Transform
GA	Genetic Algorithm
GLBC	Google little box challenge
H2G	Home to Grid
HF	High Frequency
HF PWM	High Frequency Pulse Width Modulation

I2G	Industry to Grid
IPCC	Intergovernmental Panel on Climate Change
LF	Low Frequency
LISN	Line Impedance Stabilisation Network
LTCC	Low Temperature Cofire Ceramic
MMC	Modular Multilevel Converter
MOSFET	Metal-Oxyde-Semiconductor Fiel-Effect Transistor
PCB	Printed Circuit Board
PFC	Power Factor Corrector
PHEVs	Plug-in Hybrid Electrical Vehicles
POL	Point Of Load
PPB	Power Pulsating Buffer
PWM	Pulse Width Modulation
RMS	Root Mean Square
SJ Si	Super Junction Silicon Devices
SMD	Surface Mounted Device
TCM	Triangular Current Mode
THD	Total Harmonic Distortion
V2G	Vehicle to Grid
WBG	Wide Band Gap
WBG	Wide Bandgap

Symbols

α	Duty Cycle
$\bar{IL_{TCM}}(t)$	Average current in PFC inductor for TCM [A]
ΔI	Input Current Ripple [A]
$\hat{IL_{TCM}}(t)$	Maximal current in PFC inductor for TCM [A]
φ_{car}	Carrier phase shift [°]
Esw_{OFF}	Turn OFF switching energy [J]
Esw_{ON}	Turn ON switching energy [J]
f_0	Resonance frequency
f_{SW}	Switching frequency [Hz]
fsw_{MAX}	Maximal switching frequency [Hz]
fsw_{MAX}	Maximal switching frequency for TCM [Hz]
I_R	Reverse Current [A]
P_L	Inductor losses [W]
P_{min}	Minimal power [W]
P_{SW}	Semiconductor switching losses [W]
R_{AC}	Inductor's AC resitance [Ω]
R_{DC}	Inductor's DC resitance [Ω]
S_B	Surface [m^2]
V_{DC}	DC Bus voltage [V]
$V_{DS}(t)$	Drain to Source voltage [V]
$V_{GS}(t)$	Gate to Source voltage [V]
$V_{PPB,max}$	Maximal buffer capacitor voltage [V]

V_{PPBmin}	Minimal buffer capacitor voltage [V]
Coss	Transistor Output Capacitor [F]
fs	Grid frequency [Hz]
GaN	Galluim Nitride
h	Convection factor [$W.m^{-2}.K^{-1}$]
N	Number of interleaved cells
Qrr	Transistor Body Diode Reverse Recovery Charge [C]
Si	Silicon
SiC	Silicon Carbide
tf	Transistor Fall Time [s]
tr	Transistor Rise Time [s]
Ts	Grid Period [s]
Tsw	Switching period [s]
Ve(t)	Full bridge input voltage [V]
Vs(t)	Grid voltage [V]

Chapter 1

General introduction & Preliminary studies

1.1 Environment stakes promote deployment of power electronics

1.1.1 Environmental background and direction

Since several years now, the energy policies over the world are focused on reducing the impact of the poor energy management on the environment. Fossil energies tend to be progressively avoided. In 2015, the protocol of Paris was a new step into a worldwide environmental protection, after the protocol of Kyoto. With the 189 national plans covering 98 % of the greenhouse gas emissions, global warming is a worldwide concern. The main, long-term, objective of the protocol of Paris is to limit the rises of the average temperature below 2 °C [1].

However, the last "Intergovernmental Panel on Climate Change" (IPCC) report states that the 2 °C objective is not enough and has serious impact on the environment. For examples, with an increase in temperature about 2 °C, 99 % of the reef are threatened to disappear, the increase in the sea level of 10 cm will impact more than 10 million people and the full ice melt will happen every 10 years. Hence, the limitation of an increase in temperature of 1.5 °C can mitigate these issues [2].

Some methods are foreseen to solve or reduce the global warming and climate changes [3] :

1. Reduce or even abandon coal-fired power generation. The capture and sequestration of CO_2 can be investigated even if it is a complex and expensive solution [4]
2. Increase nuclear power while security and radioactive wastes are main issues and need to be managed
3. Preserve rainforests over the world and develop forestation
4. Promote environmentally clean energies (Wind, solar, ocean current)
5. Save energy by more efficient generation, transmission, distribution and consumption of electricity (objective of smart grid)
6. Replace combustion engine vehicle by electrical and hybrid electrical vehicle
7. Develop mass electrical transportation (Bus, freight transport)

With these solutions note that a major part deals with electricity, such as improvement of electrical facilities efficiency, development of renewable energy sources and electrification of car parks. Hence, to reach the objective of a reduction of greenhouse gas emissions by 80 - 95 % by the 2050, in Europe, two-thirds of the energy should come from renewable sources. All the actions and trends are presented in the “Energy roadmap 2050”[5]. The electrical energy has an important role to play, for example the decarbonisation of the transport. Electricity will represent 65 % of the energy demand by cars and light duty vehicles. Moreover, the development of highly efficient buildings, including houses, will increase. The grid turns from centralised to decentralised energy sources.

1.1.2 From grid to smart grid

The actual grid system is composed of bulk power plants, usually mainly using fossil fuels (coal, gas and oil) with rated power from 120 MW to 700 MW, nuclear energy ($>$ 1 GW) and hydroelectric generators (0.5 MW to $>$ 10 MW). Frequency control is used to maintain the bus voltage and control the active and reactive power accordingly to the load (consumers) that fluctuate with variable power factor.

With all the major coming changes mentioned above, the actual energy distribution needs to be updated. The association of huge power plants, long power lines and substations close to loads will evolve to a more interactive network (Smart Grid). The merging of the knowledge in power systems, power electronics, communications, information, artificial intelligence will improve grid reliability, power quality, energy efficiency and optimum resource utilisation from sources to consumers [6]. Renewable energy sources, with their sporadic behaviour, will integrate the grid in a larger scale. At the same time, distributed sources will grow. All the parties in action, from the distributors to the consumers, will participate in the security and power quality of the grid by adapting their power flow as industries, buildings and households will be able to provide energy to the grid. The principles of Home-to-Grid (H2G), Building-to-Grid (B2G) and Industry-to-Grid (I2G) participate to build the future “smart” network [7]. The move will be progressive as the actual technologies are well developed while the new technologies take time to fully integrate the actual grid system. A simplified representation of a smart grid and its players is presented in the Figure 1.1.1.

The development of Plug-in Hybrid Electrical Vehicles (PHEVs) and Electrical Vehicles (EVs) is also concerned with this evolution. The concept of Vehicle-to-Grid (V2G) is investigated. V2G describes a system in which EVs/PHEVs, considered as mobile energy storages and sources (20-50 kWh battery pack [8]), communicate with the power grid to sell demand response services by either returning electricity to the grid or by throttling their charging rate. Electrical car parking lots can be used to overcome the sporadic behaviour of renewable sources or overload issues [9]. Thus, the stability of the grid can be improved by the fast response time of such installations. The V2G principle and the power sharing concept, are mainly limited by the state of charge of the batteries. Information about the departure time is crucial to ensure the required level of charge before departure [10].

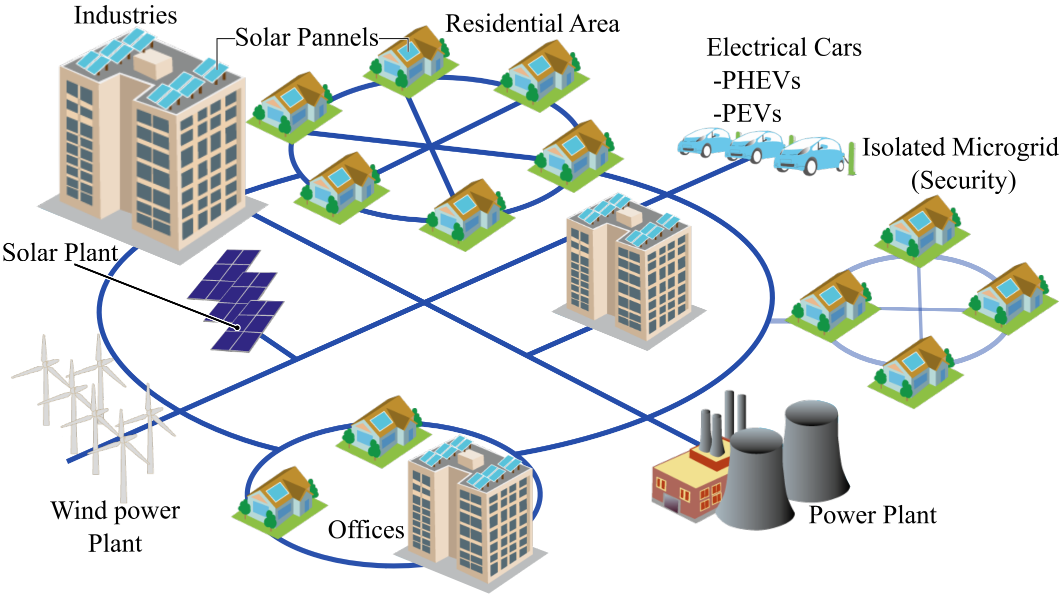


Figure 1.1.1: Smart grid with distributed power sources

1.1.3 Power electronics: the most valuable asset

Among the considered solutions to limit the global warming, the reduction of wasted energy is important at every step of the value chain. Implementation of power electronics in the different steps of the energy conversion can increase the efficiency [11]. For example, using or improving power electronics in motor drives, lighting, communication and transmission applications can represent an energy saving corresponding to 25 % of the EU electricity consumption [12].

Power electronics represents the heart of the penetrating renewable energy sources. From 1980 to 2018, the power capability of wind turbine increased from to 50 kW to 10 MW and since 2005 power electronics covers 100 % of the power rate of the system [13], which was already the case for photovoltaic (PV) since the early beginning. Wind and PV sources depend on the weather, therefore, require bulk energy storage such as battery, flywheel, superconductive energy storage [14] or pumped hydro. All these storage techniques widely depends on power electronics to store energy then to release it to the grid [15].

As mentioned, electric vehicles represent an efficient and clean transportation technique if the charging energy comes from renewable sources. The development of such vehicles also depends on power electronics. Power converters are required for the propulsion and charging, which include low power on-board charger and fast charging stations [16]. Power electronics is a centrepiece in the development of V2G.

As a conclusion, all these developments lead to more interconnections between different power levels and source types (AC, DC, low voltage, high voltage). Moreover, the control of the power flow is mandatory in a smart grid for security and power quality reasons, and thus bidirectional systems are required. Power converters are an efficient and flexible solution for the interconnection between the different grid players. The ability to quickly change the operational mode is a main advantage. Moreover, a proper control enables to easily manage the reactive power [17]. Hence, power electronics is essential for the good development of smart grids and reduction of the global warming [18].

1.2 Multi-objective optimisation design of power electronics converters

Since several years, the trend in power electronics concerns high power density and high efficiency converters to facilitate the implementation of power converters in more complex systems. High efficiency is inherently required to achieve high power density. This trend is mainly impacted by the objectives of volume and cost reduction [19][20]. With future requirements on the improvement of global efficiency, power converter design with high efficiency is mandatory, while other objectives must be reached. The most common objectives in power electronics design are :

- High efficiency (η) [%]
- High weight power density (γ) $\left[\frac{kW}{kg}\right]$
- High volume power density (ρ) $\left[\frac{kW}{dm^3}\right]$
- Low cost [$,€]
- High reliability

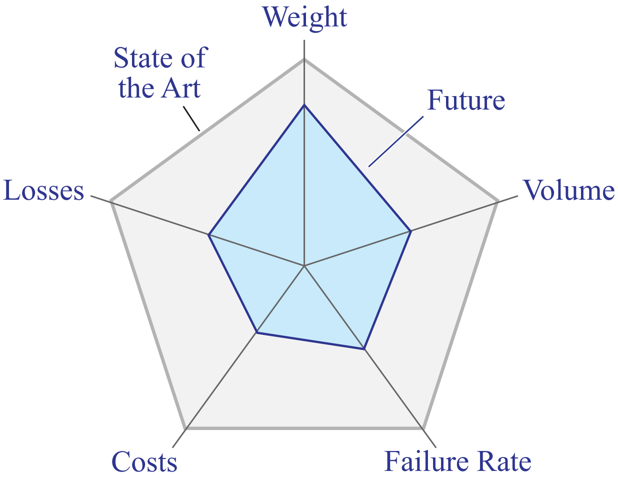


Figure 1.2.1: Performance trends of power electronic systems [21]

These objectives are identified as “Performance Indices” which are interdependent. They can be measured and compared to actual market products to evaluate the development of power converters. The trends of these different objectives in power electronics are depicted in the Figure 1.2.1.

To reach the objectives and push toward the limits of power converter design, optimisation is required, just like new technologies (materials, components), efficient converter topologies with proper control and new manufacturing processes [22]. From [23], converter optimisation is mathematically defined as four elements. The first one, a set of requirements and specifications which depends on the application and the project (e.g. voltage rating, output power) is represented by the vector $\overrightarrow{r}$.

$$\overrightarrow{r} = (r_1, r_2, r_3, \ldots, r_n) \tag{1.2.1}$$

The second one corresponds to the constants implied in the design that are basically the manufacturer specifications, the material properties, e.g. magnetic components. It is defined by the vector $\overrightarrow{k}$.

$$\overrightarrow{k} = (k_1, k_2, k_3, \ldots, k_m) \tag{1.2.2}$$

The third vector, $\overrightarrow{x}$, includes all the identified design variables, for example the switching frequency, the inductor value. All the previous vectors are linked by the design constraints represented by vector $\overrightarrow{g}$ and $\overrightarrow{h}$ which can represent equality or inequality. Basically, the constraints for power converters can be the limitation of the temperature, maximal flux density in inductors, conduction mode, EMI compliance, etc.

$$\overrightarrow{x} = (x_1, x_2, x_3, \ldots, x_l) \tag{1.2.3}$$

$$g_i(\overrightarrow{x}, \overrightarrow{k}, \overrightarrow{r}) = 0 \qquad i = 1, 2, 3, \ldots, p \tag{1.2.4}$$

$$h_j(\overrightarrow{x}, \overrightarrow{k}, \overrightarrow{r}) \geq 0 \qquad j = 1, 2, 3, \ldots, q \tag{1.2.5}$$

The association of multiple variables leads to an infinite set of virtual solutions which fulfill the constraints and the requirements. To be able to select one suitable converter among the multitude of solutions an objective function can be introduced. The objective function $f(\overrightarrow{x}, \overrightarrow{k})$ can be related to any performance indices (p_i) previously presented, volume, cost, etc.

$$p_i = f(\overrightarrow{x}, \overrightarrow{k}) \Rightarrow Max \tag{1.2.6}$$

As mentioned before, power electronic design is mainly driven by multi-objectives design. Hence, multiple performance indices need to be optimised, e.g. efficiency-volume or even efficiency-volume-cost. Several objective functions have to be simultaneously met. However, the different objectives may not impact the design in the same range, thus the objective function can be weighted [24].

$$\sum w_i \cdot f_i(\overrightarrow{x}, \overrightarrow{k}) \Rightarrow Max \tag{1.2.7}$$

All of these definitions are common to any design of power converters and related optimisation procedures. The main difference is how the final solution is defined and selected. One solution is the selection by the optimisation procedure itself based on the objectives and on relative errors. This is the case of probability based Genetic Algorithm (GA) proposed by Holland [25]. GA is a discrete optimisation procedure as component databases can be used to enable immediate prototyping. This methodology has been widely used in power electronics [26, 27, 28, 29]. It is particularly suitable when discrete components (semiconductors, inductor cores, capacitors, ...) are the optimisation variables. First, the algorithm randomly creates several individuals, each representing one specific design and forming the population. Each design is defined by its “genes” depending on the related database. The number of genes is equivalent to the number of variables. All the designs are evaluated according to the constraints and objectives. The most effective designs are selected to create the next generation. Parents are recombined to form children with crossover characteristics which should lead to more competitive designs, as illustrated in the Figure 1.2.2. Other genetic operators can be applied, for example, the mutation that randomly changes one or multiple child genes opens to new solutions. To always keep the best designs in the loop, worst converters in the child population can be replaced by the best from the parent population. This procedure is reiterated until the convergence criteria are satisfied and the final design selected.

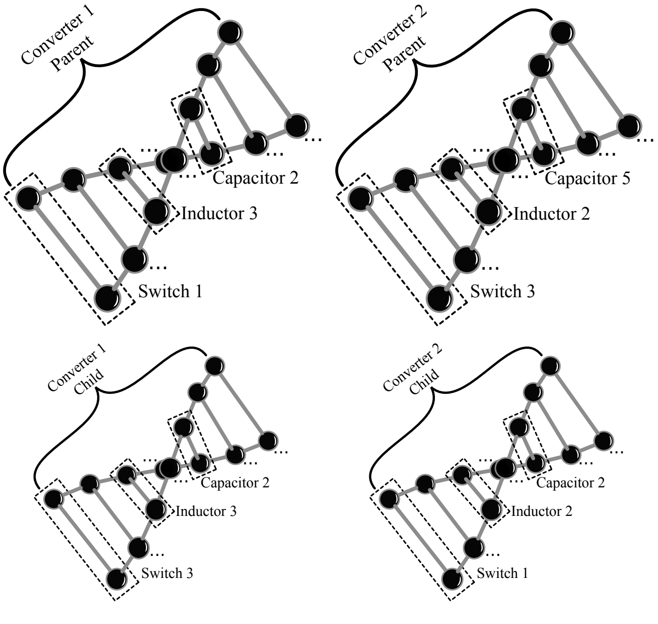


Figure 1.2.2: Illustration of converter designed with GA

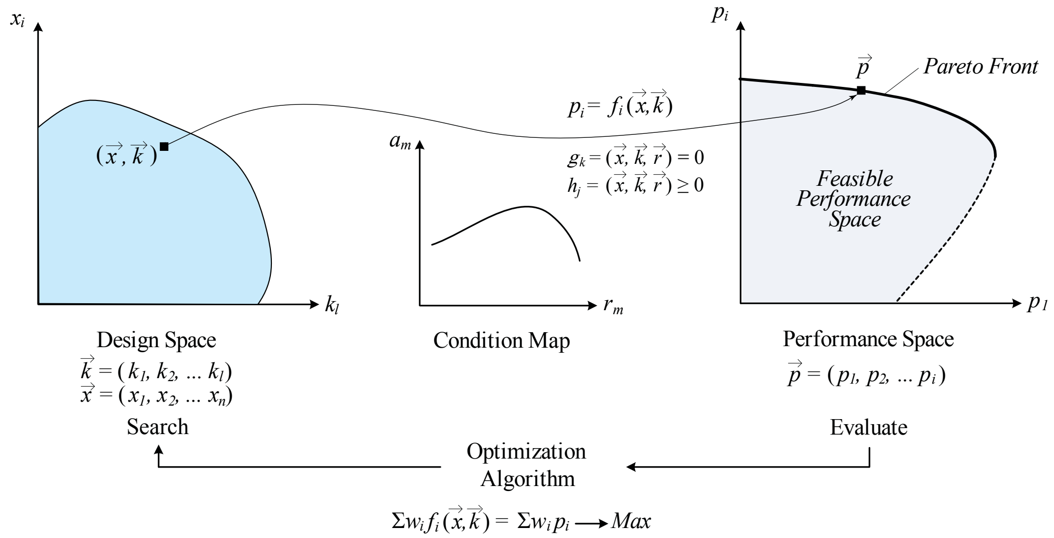


Figure 1.2.3: Multi-objectives optimisation of multi-dimensional Design space [21]

Despite the gain of interest for this optimisation method, it presents some drawbacks. In the case of continuous optimisation variables, such as switching frequency, special genetic operators are required to produce the next value from parents to children. As random features and convergence criteria are used, it is more complicated to analyse the impact of main optimisation variables.

Another method with graphical representation of the different possibilities can be implemented. Thus, the design space represented by the variable $\overrightarrow{x}$ and the constant $\overrightarrow{k}$ can be transformed in performance space where the performance indices p_i are the axis. Contrarily to single objective optimisation corresponding to one design placed on one of the axes, it results in a set of solutions, like with GA optimisation. Hence, in the representation of the performance space, the best trade-off, according to the designer, needs to be selected. The selection of the best trade-off is realised on the boundary of the feasible performance space. This represents the pareto front. The representation of multi-objectives optimisation is presented in the Figure 1.2.3.

Usually, multi-objectives optimisation is performed for a selected converter topology, corresponding to requirements with an associated control. The behaviour of the converter is put in equation according to selected components and/or technologies. Even if the variables are limited by these pre-choices, the optimisation is still complex due to the multiple possibilities depending on semiconductors, magnetic cores and the different combination of the variables. To facilitate the design of optimal converters, the optimisation can include a main optimisation loop, which depends on the main optimisation variables, and sub-parts corresponding to different functions of the converter. Therefore, sub-optimisation parts correspond to the component scale, such as semiconductors, inductors, capacitors. However, these sub-parts are still linked to each other, e.g. the selection of semiconductors impacts the EMI filter design. This design technique allows different solutions to be compared and the impact of variables quickly analysed. The latter optimisation method is then preferred than the GA optimisation procedure.

1.3 PCB integration for performances enhancement

In electronics the “integration” is merging, in one component or chip, several elementary components usually transistors to create complex functions. In power electronics different components, power transistors, gate-drivers, inductors and capacitors are required to create elementary switching cells. Therefore, integration in power electronics corresponds to an improved assembly of these basic components to create an “elementary cell” providing interconnection capabilities to meet to multiple application requirements.

System integration is one of the main concerns in the electronic community as it can be analysed from the European Center for Power Electronics (ECPE) roadmap for the coming years, see the Figure 1.3.1.

In electronic fields, including power electronics, multi-layer printed circuit board (PCB) are very common as custom designs are simple to manufacture. The manufacturing process is mastered and it is low cost for mass production. Electronic components are usually mounted on external layers of the PCBs, as presented in the Figure 1.3.2.(a). Since several years now, embedded components gained lot of interest. This process allows the free inner layers space to be used by embedding small components such as capacitors, resistors and semiconductors. The Figure 1.3.2.(b) presents a cross-section of a 1.6 x 1.6 mm^2 camera module with embedded components, actives and passives. PCB embedding process explicitly

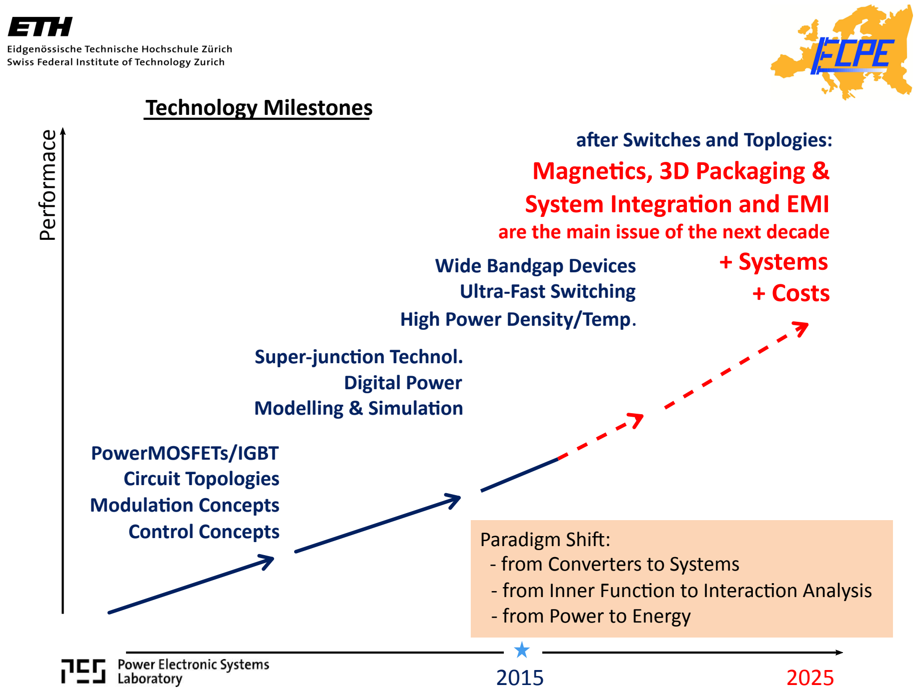
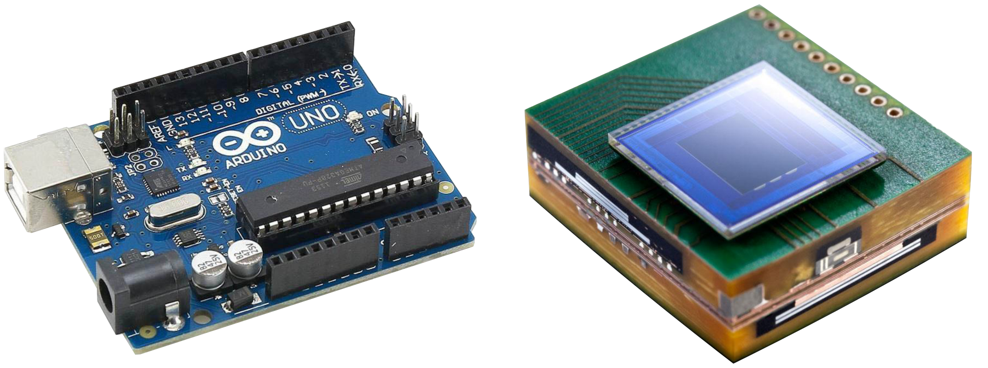


Figure 1.3.1: ECPE roadmap [30]



(a) Surface mounted devices (SMD) (b) PCB with embedded components [31]

Figure 1.3.2: Examples of PCB assemblies

responds to the high-density system demand. The following presents the benefits of PCB integration in power applications.

1.3.1 Active components

The higher switching capabilities of GaN or SiC compared to Si have been highlighted [39, 40]. However, to fully take advantage of these devices, parasitics from circuit and package must be reduced as much as possible to improve the dynamic performances [41]. The 3D packaging with power die embedding allows the parasitic elements (mainly stray inductances) to be drastically reduced. The power module presented in the Figure 1.3.3 includes four embedded SiC transistors, DC link decoupling capacitor and current measurement. The measured stray inductance is lower than 1 nH while classical half-bridge power module stray inductance is about 15-20 nH [42]. Hence, the commutations can be very fast while no ringing appears during the turn-OFF commutations, thus the switching losses are reduced [43].

The reduction of the parasitics does not only impact the losses, but also the EMI perturbations. The reduction of ringing during commutations contributes to cleaner operation of power converters as common mode perturbations are reduced. Moreover, the custom packaging capability of 3D PCB embedding allows the stray capacitances to be used favourably [44]. In the integrated power module presented

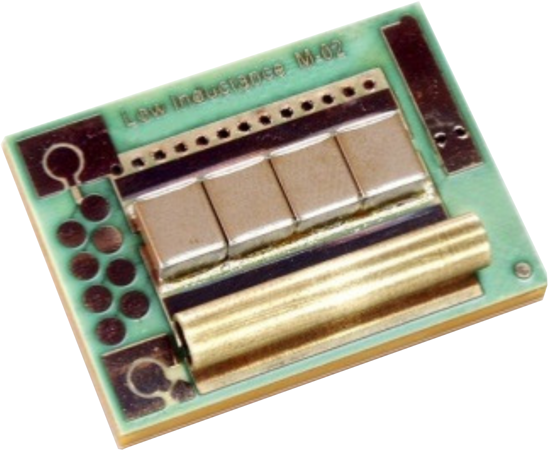
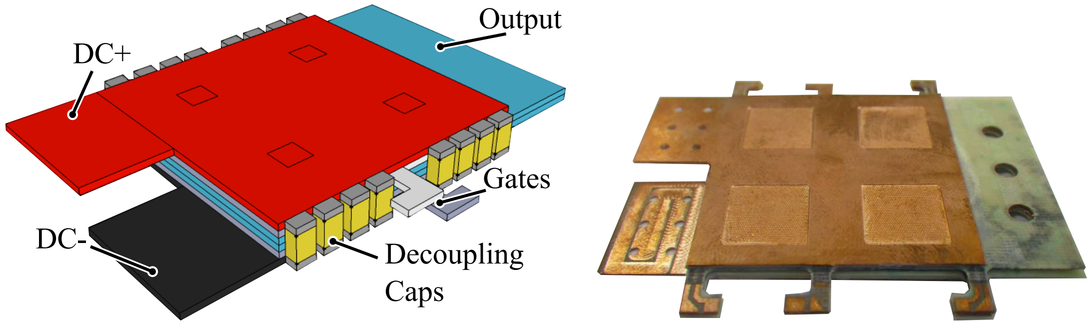


Figure 1.3.3: Integrated power module with 1 nH stray inductance [43]

in the Figure 1.3.4 the output (Mid-point) is sandwiched between the DC+ and DC- connections. This acts as a shielding. Moreover the module is a double side cooled module, thus the parasitic capacitances between earth and the two DC potentials are equivalent. With this configuration, the parasitic capacitances of the DC link help to filter the common mode noise [45]. Thus, the module has an improved common mode behaviour. In the same way, the power module designed in [46], see Figure 1.3.5, reduces as much as possible the parasitic capacitance between the mid-point and the heat-sink. This is achieved by flipping one of the chip [47]. This way the capacitances linked to the DC bus are also symmetrised. The decoupling capacitors are also very close to the semiconductors. Another new point from this example is the proximity of the gate driver allowing very fast and clean switching. Therefore, the 3D integration is not only the solution for high-density design, it is also a promising solution to improve the performances of packaging.



(a) 3D model of the integrated module [48] (b) Prototype integrated module [49]

Figure 1.3.4: Integrated power module with improved Common Mode behaviour

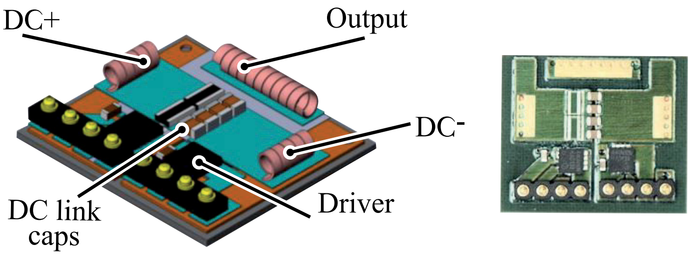


Figure 1.3.5: Power module with integrated gate drivers [46]

The embedding of active components is not limited to bare dies. It is also possible to take advantage of the interlayer space by embedding packaged devices, e.g. gate driver, Op Amp circuits, ... Packaged components embedding is preferred for circuits which does not require external cooling.

1.3.2 Passive components

The passive components (inductors, transformers, capacitors and resistors) are widely used in power electronics. The current capabilities of such components are very large, from mA to hundred of amperes, depending on the purpose, e.g. filtering for measurement circuits or energy storage components. The higher the power of the application, the bigger the component. This is an issue for PCB embedding where low profile devices are preferred.

1.3.2.1 Capacitive components

First works on embedded capacitors were focused on low power applications such as high-frequency noise filtering. In this case, one possible method is the embedding of thin capacitive films [50]. The thin capacitive film is placed between two copper layers in the stack-up to form a planar capacitor. The capacitance depends on the permittivity of the material, the surface and the thickness of the film. Performances of such capacitors are limited to few nF, even if high permittivity materials are used, e.g. $BaTiO_3$. Moreover the voltage rating of this technology is lower than 100 V which is very limiting for power converters that require capacitors in the µF range under several hundred of volts [22].

Thus, packaged capacitors (SMD) such as MLCC, are more convenient: the capacitance density is much higher than the embedded thin film. The limitation mainly comes from the thickness of the package as the PCB is from 1 to 3 mm thick. The inserted component is simply attached on a patterned board, then prepreg sheets with cavities are placed on top for the lamination of the overall PCB. This principle is also used for ICs.

1.3.2.2 Magnetic components

(a) POL converter

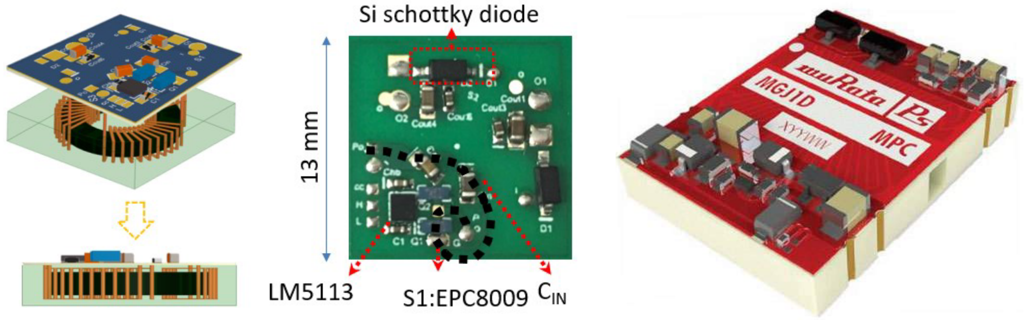
(b) LTCC inductor with surface winding

Figure 1.3.6: Integrated POL converter with LTCC inductor [51]

Similar to capacitive components, low profile thin-film inductors with a thickness lower than 3 mm are available on the market. Thus, the inductors are thin enough to be embedded, but the values are limited and the current capability is small. The integration of such low power magnetic components is particularly suitable for point-of-load (POL) converters. The Figure 1.3.6 presents a 10 A 4 MHz POL converter using the Low Temperature Cofire Ceramic (LTCC) inductor and GaN devices. The result leads to a power density of 91 kW/L.

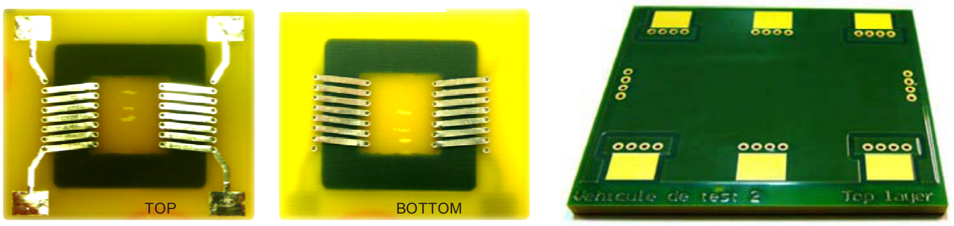
Another low power application where PCB integrated magnetics are used is gate drivers for larger power converters [52]. An integrated, 13 x 13 mm^2, 2 W dual-outputs gate-driver power supply for GaN is presented in [53]. The transformer is made by embedding a ferrite core in the PCB. The primary and the two secondary windings are formed by tracks and vias. A similar product, 15 x 20 mm^2, isolated power supply for gate drivers, is available from Murata (see Figure 1.3.7). In both cases, the embedded cores have a small outside diameter that it is preferred to handle the lamination process.

Therefore, the integration of small magnetic components for low power applications is mastered as some manufacturers use the process for mass-produced references. The work presented in [55] extends the principle close to the hundred of watts range by designing a 60 W EMI filter. The filter includes a coupled common mode choke using embedded square core. The differential mode inductors are designed by using the stray inductors of the common mode choke. The low value differential and common mode capacitors, 20 nF and two times 10 nF respectively, are formed by using embedded dielectric films. This combination of integrated



(a) Dual output power supply [53]   (b) Power supply from Murata [54]

Figure 1.3.7: Isolated power supply for gate-drivers



(a) Common Choke   (b) Complete EMI filter

Figure 1.3.8: 60 W integrated EMI filer [55]

solutions allows a low profile EMI filter of 20 cm^2 to be designed. The evaluated performances are better than an equivalent discrete EMI filter. The embedded magnetic core and the global EMI filter are presented in the Figure 1.3.8.

Hence, the development of integrated solutions, either for active and/or passive components impacts power converter optimisation procedures. The reduction of stray inductances enables the increase in switching frequency which is usually used as one of the optimisation variables. The improved EMI signature due to smart layout allowed by die embedding needs to be included in the optimisation to avoid oversized EMI filters. The design of magnetic components might be constrained by the design rules of the PCB manufacturer.

1.4 Thesis objectives and specifications

Integration is a spearhead of Mitsubishi Electric R&D Centre Europe research activities with design of highly integrated converters. It includes internal projects and collaborations. One of those collaborations includes the Laboratoire Ampère with two thesis subjects, the combination of the two work-packages results in the design of an highly integrated AC/DC converter with high performances and high level of system integration, PCB process is especially investigated.

One subject deals with the integration process. It is handled by Rémy CAILLAUD through a thesis entitled "*Integration of a 3.3 kW bidirectional AC/DC converter using PCB embedded technology*" [32]. The work realised in this thesis covers the PCB integration of active devices and passive components. The PCB integration of passive components, especially power inductor, is realised by investigating embedded magnetic cores to develop low profile inductors. The thermal management of integrated converter with natural convection cooling system is also studied, e.g. semiconductors, inductors cooling. The PCB process is developed closely with the PCB manufacturer (CIMULEC) , to embed power dies, packaged components and magnetics.

The second one, which is presented in this document, deals with the study of the converter topology. Indeed, the selection of the right topology with proper control is primordial as it widely impacts the possible level of integration. The selected topology should propose a reduction of passive component volume because

Table 1.1: PFC specifications

Input Voltage Range	85-260 V_{RMS}(AC)
Maximal Input Current	15 A_{RMS}(AC)
Maximal Output Current	12 A (DC)
Output Voltage	200V to 400 V (DC)
Maximal Output Power	3.3 kW
Working Environment	-40 to 60°C
E.M.C	EN55011 Class B conducted EMI

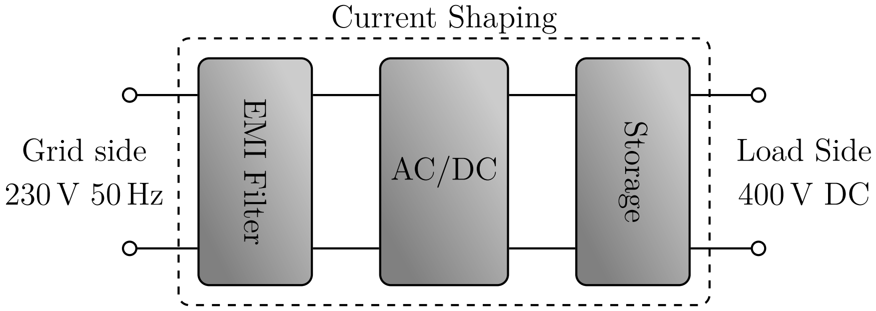


Figure 1.4.1: Functional block representation of the converter

it represents the main part of power converters [33]. An optimisation procedure, similar to the one presented in Section 1.2, must be developed according to the selected topology and the constraints ($\overrightarrow{g}$ and $\overrightarrow{h}$) impacted by the PCB integration process. It must include the EMI filter design. The optimisation variables ($\overrightarrow{x}$) need to be defined. The main specifications and constraints ($\overrightarrow{r}$ and $\overrightarrow{g}$, $\overrightarrow{h}$ respectively) of the converter at the beginning of the project are presented in the Table 1.1. The main studied parts in this project are illustrated in the Figure 1.4.1.

1.5 AC/DC converter topologies

In 2015 the Google little box challenge (GLBC) (design of a 2 kW >95 % CEC efficiency[1] photo-voltaic inverter) highlighted that high efficiency and high power density converters could be designed, as presented in the Figure 1.5.1. The analysis of the challenge shows that the selection of the right converter topology may widely impact the results [56] [57]. The development of wide band-gap components also allows the volume of power converters to be reduced. This is mainly due to lower losses and the high switching frequency capabilities of Silicon Carbide (SiC) and Gallium Nitride (GaN) [38]. Several teams used GaN for the competition [37]. The thermal management is also very important. The use of uncommon heat-sink, as

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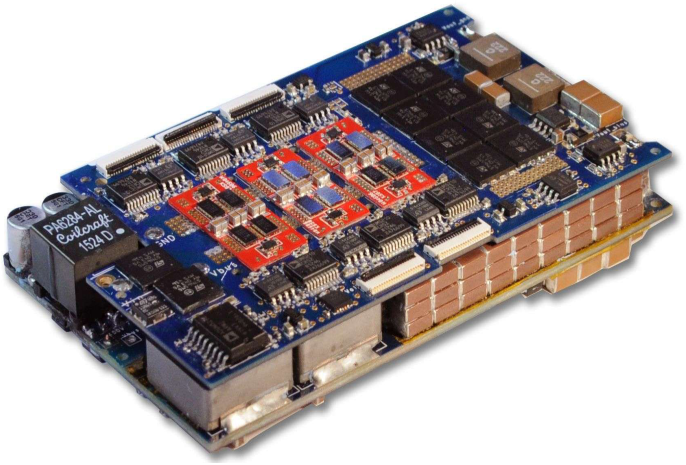
[1] CEC efficiency corresponds to a weighted efficiency measurements which depends on the power load, for example 50 %, 75 % or 100 % of the nominal power.


(a) 97.6 %, 13.2 kW/L 7 levels flying capacitors inverter [57]


(b) 96.4 %, 8.18 kW/L interleaved full-bridge inverter [37]

Figure 1.5.1: High Efficiency and High power density inverters for the GLBC

the honeycomb heat-sink used by the winner of the GLBC [58], can further reduce the volume when associated with low loss devices.

This competition point out all the critical aspects in high density converter design. The first target is the reduction of passives that are impacted by the topology, the control and the switching capabilities. Then the reduction of losses, thus the reduction of cooling, is the second point. Finally, the mechanical integration of all these elements is crucial. This final task is simplified if the integration level of active and passive components is already improved with good interconnection methods.

1.5.1 Power Factor Corrector

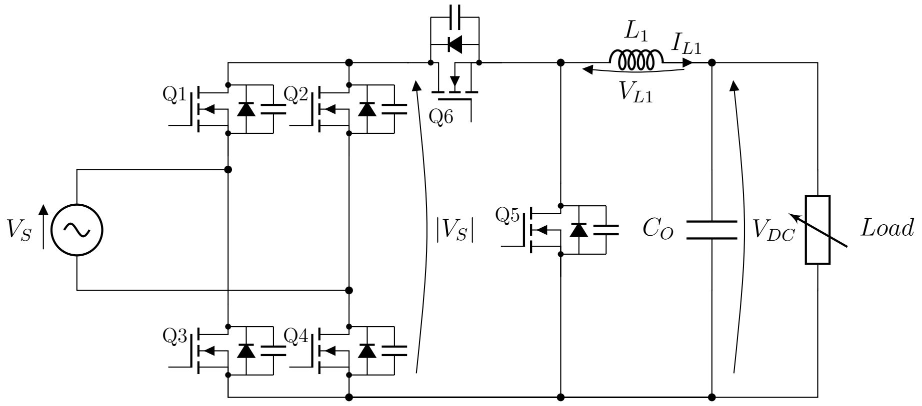
This section investigates bidirectional power factor corrector topologies. As aforementioned, the selection is based on reduction of losses and passive component volumes to facilitate the integration process. Classical PFC topologies use a diode bridge at the input that disable the load to grid power flow. This issue is easily overcome by replacing the diode bridge by switches controlled synchronously with the grid voltage (Unfolder). Moreover, these switches have to be able to push the current in the two directions. Basically, field-effect transistors are used. Hence, classical topologies as the Buck, the Boost and the Buck-Boost, all presented in the Figure 1.5.2, are studied with a low frequency bridge at the input. This three converters have a storage inductor after the rectifier bridge. Hence the current flowing through the inductor has a DC component that must be considered for the design, especially for saturation.

Buck + Unfolder

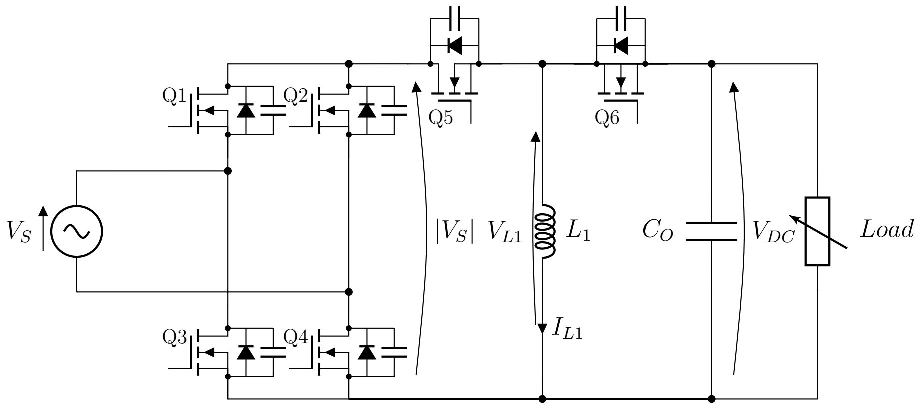
For the Buck converter, the output voltage must be always lower than the input voltage. Therefore, the regulation of the input current is not assured as soon as the rectified grid voltage is lower than the output voltage. Thus, the current presents an important distortion that is not suitable in PFC applications [59]. Concerning the design considerations, the semiconductor should withstand the maximal grid voltage. Thus, semiconductor with lower voltage rating, such as 650 V GaN, can be used without risk of over-voltage breakdown. The inductor value is calculated according to the maximal input voltages ($\hat{Vs}$), the allowed current ripple (ΔI), the switching frequency (fsw) and for a duty cycle equal to the half of the switching period (usually the current ripple is maximal for V_{DC} is half of $\hat{Vs}$), see Equation 1.5.1 .

$$L_{Buck} = \frac{\hat{Vs}}{4 \cdot \Delta I \cdot fsw} \tag{1.5.1}$$

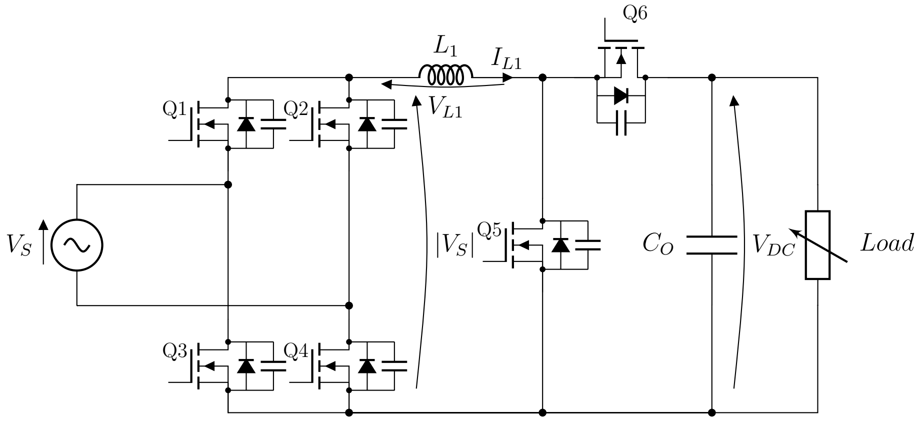
Another drawback comes from the input current. Indeed, the input current is equal to the current flowing through the top switch (Q6 in the Figure 1.5.2.a).



(a) Buck + unfolder



(b) Buck-Boost + unfolder



(c) Boost + unfolder

Figure 1.5.2: PFC topologies with low frequency unfolder

Hence, the current is discontinuous even if the conduction mode is continuous (current in the inductor). This leads to an input filter with a large volume. In the case of classical DC link capacitor bank, the required capacitance is determined with rated power of the converter and the allowed DC voltage ripple. To store the energy, the capacitor requirement must be increased as the voltage is low, thus the volume of the capacitor bank may increase depending on the voltage rating.

Due to the major drawbacks linked to this topology (high current distortion, big DC link capacitor bank), the Buck topology is not perceived as the most suitable one considering performances and integration capabilities.

Buck-Boost + Unfolder

The second converter topology is the Buck-Boost converter. The output voltage can be either higher or lower than the input voltage. As for the Boost topology grid current has almost no low frequency distortion, that make the Buck-Boost a good candidate for PFC applications. However, the main drawback of this topology is the inversion of the polarity of the output voltage compared to the rectified input voltage. The semiconductor should be selected according to worst case that depends on the desired DC voltage, higher or lower than the peak grid voltage. The storage inductor is calculated according to the maximal voltage (V_x) that could be either the input or output voltage, see Equation 1.5.2.

$$L_{Buck-Boost} = \frac{V_x}{\Delta I \cdot fsw} \tag{1.5.2}$$

As for the Buck, the injected grid current is equal to the top switch current which widely impact the design of the input filter as the current ripple to filter is large. The output capacitor also depends on the DC voltage level and allowed voltage ripple. Despite the good performance of Buck-Boost for current shaping applications [59], this topology has some drawbacks that make it less interesting than the Boost one.

Boost + Unfolder

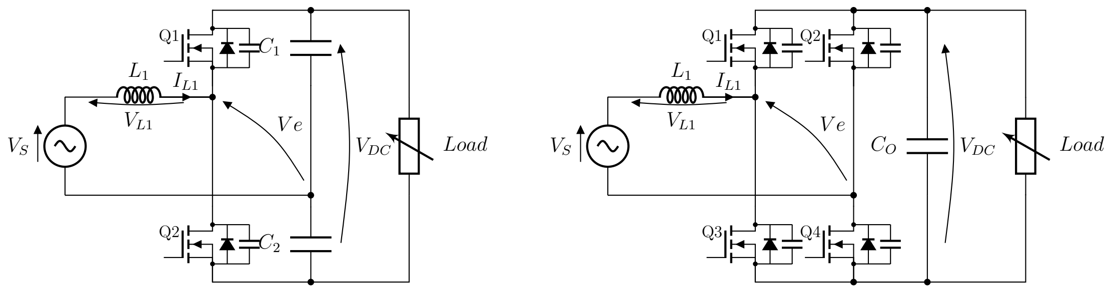
The Boost topology is widely used as a front-end converter. The Boost converter is the opposite of the Buck, the output voltage has to be always higher than the input voltage. Thereby, in the case of PFC applications the DC voltage must be higher than the peak grid voltage that is 325 V. This assures a good behaviour for current shaping, the distortion is consistently reduced compared to the Buck [59]. The semiconductors should withstand the DC voltage. Moreover the higher the blocking voltage, the higher the switching losses. Thus, as the SiC voltage rating is higher than GaN, SiC MOSFETs can be used to improve the performances. The inductor value is calculated according to the Equation 1.5.3.

$$L_{Boost} = \frac{V_{DC}}{4 \cdot \Delta I \cdot fsw} \tag{1.5.3}$$

As the inductor current corresponds to the input current, the differential mode input filter can be reduced in the case of continuous conduction mode (small current ripple). This represents a trade-off between the input inductor and the input filter sizes. With the Boost topology, the DC link capacitor can be reduced compared to the Buck, indeed the energy can be stored in lower capacitor as the voltage is higher. Hence, the effectiveness of this topology for PFC applications has already been shown. It is the most interesting topology among those that use low-frequency unfolder.

In general, these three topologies are limited, the number of active devices is large, meaning an increase in losses. The design of inductors is impacted by the DC components and the freedom degrees of control are quite limited, e.g. continuous or discontinuous conduction mode.

However, the Boost topology is identified as the most interesting. Thus, other topologies based on the Boost are investigated and reviewed [60]. In the following, two bidirectional bridge-less (without LF bridge) topologies with reduced number of devices are selected, the half-bridge with split capacitor and the full-bridge, see the Figure 1.5.3.



(a) Half-Bridge (b) Full-Bridge

Figure 1.5.3: Bridge-less PFC topologies

Half-Bridge

The half-bridge with split capacitors has the lowest number of devices. Thereby, the losses can be very low using wide band gap (WBG) components. As the topology is a Boost topology the semiconductors are selected according to the DC voltage, as for the inductor design, see Equation 1.5.4. The voltage doubler of this topology is also constraining. Indeed, the DC voltage must be, at least, twice the peak input voltage. The main drawback is the DC link composed of split capacitors. The voltage across each capacitor has to be balanced with a proper control. Moreover, the main current is flowing through the two capacitors. Hence, the size of the DC link is very large. Therefore, this topology is not particularly suitable for integration even if the losses in the semiconductors can be very low.

$$L_{HB} = \frac{V_{DC}}{4 \cdot \Delta I \cdot fsw} \tag{1.5.4}$$

Full-Bridge

The DC voltage balancing issue is overcome by the full-bridge topology. Indeed, the split capacitor bank is replaced by two switches and only one capacitor on the DC side as for the classical Boost topology. In this case the DC voltage must only be higher than the peak input voltage. The increase in number of semiconductors leads to higher losses. Nevertheless, the control possibilities also increase, e.g. bipolar, high frequency unipolar modulations and unipolar modulation with high and low frequency control. These are presented in details in Section 3.3. The modulation impacts the design of passive components, especially the input inductor (see Equations 1.5.5, 1.5.6 and 1.5.7, respectively for bipolar, HF unipolar and HF-LF unipolar modulations) and the losses. These possibilities are taken into account in the comparison between all topologies investigated.

$$L_{FB-Bip.} = \frac{V_{DC}}{2 \cdot \Delta I \cdot fsw} \tag{1.5.5}$$

$$L_{FB-Uni-HF} = \frac{V_{DC}}{8 \cdot \Delta I \cdot fsw} \tag{1.5.6}$$

$$L_{FB-Uni-HFLF} = \frac{V_{DC}}{4 \cdot \Delta I \cdot fsw} \tag{1.5.7}$$

All the topologies are compared in the Table 1.2, the selected criteria are the input inductor, DC link capacitor, control possibilities, the number of devices and the integration capabilities. Finally, the full-bridge topology is identified as the most suitable choice. The control possibilities allow the passives and the losses to be reduced, even if the number of semiconductors is not the lowest, facilitating the integration. However, the large capacitor bank on the DC side is still an issue in the design of high power density converters.

Table 1.2: Comparison of PFC topologies

	Inductor	DC Link	Control	Nb of Devices	Integration
Buck	+	−	=	6	−
Boost	=	+	=	6	=
Buck-Boost	−	=	=	6	=
Half Bridge	−	−−	=	2	−−
Full Bridge	++	+	++	4	+

1.5.2 Pulsating power management

The capacitor bank is mandatory in single-phase DC/AC or AC/DC applications such as battery charger or photo-voltaic (PV). The power at the AC side can be calculated by using the voltage and the current given by Equation (1.5.8). In these equations, it is assumed that there is no phase shift between the voltage and the current because of the Power Factor Corrector (PFC) control. From Equation (1.5.9), it is possible to identify two components in the AC power.

$$v_s(t) = \hat{V}s \cdot \sin(\omega t) \qquad i_s(t) = \hat{I}s \cdot \sin(\omega t) \tag{1.5.8}$$

$$p_s(t) = i_s(t) \cdot v_s(t) = \frac{\hat{V}s \cdot \hat{I}s}{2} \cdot (1 + \cos(2\omega t)) \tag{1.5.9}$$

The first one is the DC component used by the load and the second one is the pulsating component, as illustrated in Figure 1.5.4. In some cases, the pulsating power can be directly transferred to the load avoiding the use of buffering capacitor. This is possible with some battery technologies. Indeed, DC current with superimposed sinusoidal ripple does not affect some kind of batteries [61]. This technique can be used to design high power density converters [62].

Usually a bulky electrolytic capacitor bank is used to filter the double line-frequency power pulsation. The main drawback of electrolytic capacitors is their poor reliability [63]. Moreover, the smaller the desired voltage ripple on the DC side, the larger the capacitor bank, the larger the converter volume.

Another method using passive components, is the implementation of a notch filter . It is basically composed of one inductor and one capacitor in series. The filter resonates at the double line frequency. The main drawback of this solution comes from the inductor: as the resonance frequency is low, the inductor value is large. The addition of a large inductive component leads to higher losses compared to the full capacitive solution.

To avoid electrolytic capacitors and increase the overall power density, an additional active circuit can be used (Power Pulsating Buffer – PPB – also known as electronic capacitor). The circuit is composed of a buffer capacitor used to store and release the pulsating power, Figure 1.5.4. This decoupling method replaces

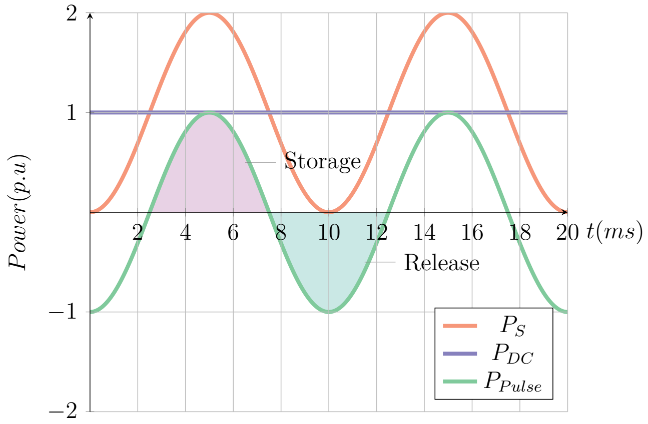


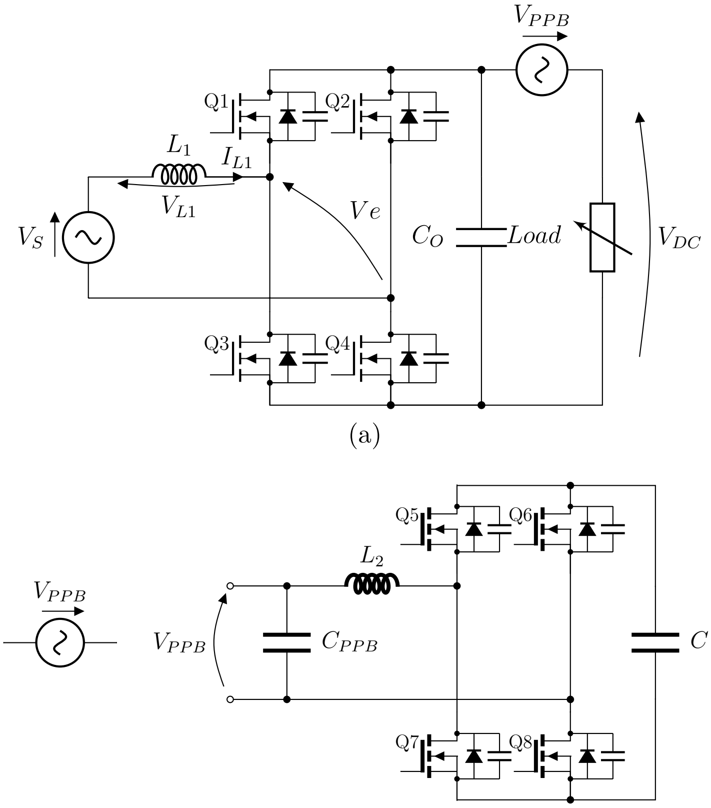
Figure 1.5.4: Typical power waveforms for an AC/DC converter. $\mathrm{P_S}$ is the power on the AC side, $\mathrm{P_{DC}}$ is the power on the DC side and $\mathrm{P_{Pulse}}$ is the power that need to be buffered by the PPB.

the bulky electrolytic capacitors by other capacitor technologies such as film or ceramic, which offer lower capacitance density, but can sustain larger current ripple, so higher voltage swing is allowed.

The literature proposes a large number of topologies [64, 65, 66, 67]. The different power decoupling techniques can be further classified into several subgroups, depending on their energy storage medium (inductive or capacitive) [68], circuit configurations and control algorithms. Firstly, it can be found independent or dependent topologies. Dependent topology means the buffer converter impacts the grid current, hence the control of the front-end converter and the electronic capacitor are linked [69]. For this project capacitive storage medium is preferred due to higher losses and volume of the inductive method. Solutions with possible independent control are investigated to avoid any cross-control issue between the PFC and the PPB. Satisfying these two criteria, two main configurations are identified, the series and the parallel connection of capacitive buffer.

1.5.2.1 Series connected power pulsating buffer

The series connected buffer is connected on one port of the PFC output, in series with the load as presented in the Figure 1.5.5.(a) [70]. The series-stacked capacitors



(a)

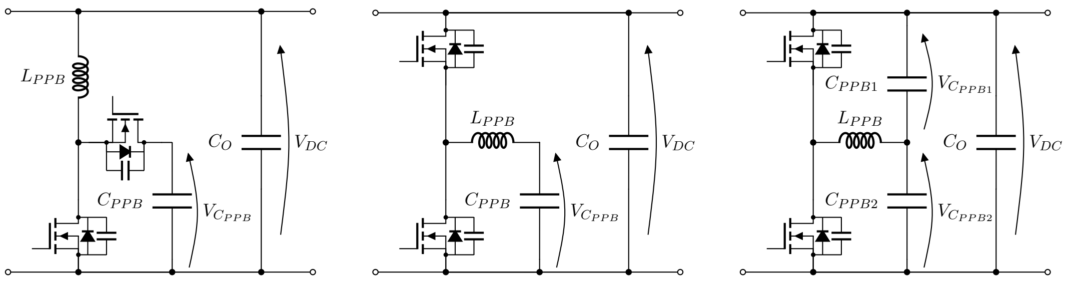
(b)

Figure 1.5.5: Series PPB principle

buffer is also included in this part [71]. The pulsating buffer placed in series is used to compensate the voltage ripple on the DC link. Therefore, the output voltage across the load is almost ripple free. A full bridge converter is usually used with this configuration (see the Figure 1.5.5.(b)).

This topology allows low voltage devices to be used as they only handle the voltage ripple of the DC link. However, lower voltage operation of the buffer converter limits the storage capabilities. Indeed, the required buffer capacitor (C) is higher compared to minimal requirement of parallel topology, especially the Buck [72]. Moreover, the full bridge topology with flying capacitor leads to a more complex implementation; e.g. all the gate drivers need to be floating. Therefore, the series connected power pulsating buffers are not selected.

1.5.2.2 Parallel connected power pulsating buffer



(a) Boost (b) Buck (c) Symmetrical Half Bridge

Figure 1.5.6: Examples of different parallel power pulsating buffers

The parallel connection is identified as the most suitable for this project. PPB stage connected in parallel on the DC bus, in a similar fashion to the electrolytic capacitor offers good characteristics in terms of power density and efficiency for a 3.3 kW highly integrated converter. Figure 1.5.6 presents a selection of possible parallel power decoupling circuits. In the following analysis, the low value inductor implemented in each topology is neglected in terms of buffering capabilities because the stored energy in the inductor is much smaller than the energy stored in the capacitor. Figure 1.5.6.(a) corresponds to a Boost topology [73] which means that the voltage across the buffer capacitor is higher than the DC voltage. A drawback is that this topology requires semiconductor devices with a higher voltage blocking capability than in the PFC stage. The voltage rating of semiconductors depends on the allowed voltage swing across the buffer capacitor. In industrial applications, the bill of material tends to be limited in a reasonable way for a given power range. Hence, this topology is not the preferred solution even if the buffer capacitor value can be reduced as the peak voltage can be high.

The Figure 1.5.6.(b) is a buck topology. In this case, the voltage across the buffer capacitor is lower than the DC Bus voltage. Consequently, the same switches can be used for the PFC and the PPB stages. For a buck PPB, the capacitor value can be determined according to the rated power of the PFC and the voltage excursion across the capacitor, see Equation (1.5.10).

$$C_{PPB} = \frac{2 \cdot P_{DC}}{\omega \cdot (V_{PPBmax}^2 - V_{PPBmin}^2)} \tag{1.5.10}$$

According to the Equation (1.5.10), the theoretical minimal value for $\mathrm{C_{PPB}}$ is obtained for $\mathrm{V_{PPBmax}} = \mathrm{V_{DC}}$ and $\mathrm{V_{PPBmin}} = 0\,\mathrm{V}$.

An alternative to the Buck topology is the symmetrical half bridge presented in [74], Figure 1.5.6.(c). The two capacitors implemented in this topology are used for the power decoupling and to build up the DC Bus voltage. However, the value of one single capacitor is twice as high as that of the buck for the same voltage rating, as it is shown in Equation 1.5.11, [74].

$$C_{PPBx} = \frac{4 \cdot P_{DC}}{\omega \cdot (V_{PPBmax}^2 - V_{PPBmin}^2)} \tag{1.5.11}$$

Thus, the total capacitor requirement for the symmetrical half bridge topology is four times higher than for the buck. Among the presented power decoupling buffers, the buck proposes the lowest buffer capacitor. Moreover, the voltage stress on semiconductors is equivalent for the rectifier stage and the buffer stage.

PPB circuit has been used by the winner of the Google little box challenge [58]. Another finalist team [72], has shown that using the buck type PPB led to a 11.3 % overall volume reduction compared to electrolytic decoupling. Thus, the advantage of PPB compared to a classical electrolytic DC Bus capacitor has attracted a large number of attention recently. However, drawbacks of any PPBs are that they require additional power switches and inductors, and generate losses. Despite, this study permits to identify the Buck power pulsating buffer as a good solution to increase the power density of the AC/DC converter.

1.6 Conclusions

The development of renewable energy sources and the evolution of the actual grid to smart grid including several types of sources increase the necessity of power electronic converters. The design of efficient and dense converters has always been a spearhead of the research community. This is all the more topical due to environmental issues. Therefore, power electronics is more important than ever to promote the development of electrical facilities.

As the development of power converters is driven by multiple-objective optimisation, the implementation of fast design procedures is mandatory to shorten the study to manufacturing time [22]. Power electronics is a multi-physics field (electronics, electromagnetism, heat sience) thus the optimisation procedure must include all these aspects. Analytical analyses of such problems are preferred as it is faster than finite element simulations.

In this project, high efficiency and high power density are the major objectives. To reach this goal, power integration is investigated, particularly PCB integration. The development of embedded active components in power electronic applications is well advanced: the PCB process is mastered and can be applied as well as for low or high power applications [75]. Beyond the gain in volume, the PCB integration is a good way to design custom packaging. The research community shows the benefits of power integration by improving the performances of power modules. It is possible to directly include other important features, such as the gate driver and the decoupling. Therefore the performances are enhanced: the parasitic elements are reduced, particularly stray inductors. The losses and the EMI signature are positively impacted. The integration of passives is more limited especially for higher power ranges. The PCB embedding of passive components for low power applications is mastered as the size of the components fits to the process. However, the design of highly integrated converters cannot be limited to the dies embedding. To reach the next level in power integration all the required features in power electronic must be included to create elementary cells that can be used in several converter designs. The elementary cell design principle in power electronics leads to a reduction of cost, losses, size and manufacturing time. Several issues are addresses with this vision: improvement of switching capabilities (reduction of stray inductances), reduction of losses, thermal management, measurements (for control and protection aspects).

Therefore, the integration-friendly full-bridge topology is selected to design the PFC. This topology allows the passive components to be reduced with an acceptable number of active devices. With the same criteria, the Buck topology is selected to design the power pulsating buffer avoiding the use of a large capacitor bank on the DC side.

1.7 Chapter overview

The **Chapter 2** introduces a new type of inductor based on 3D assembly of ferrite cores and PCB technology. This alternative solution is proposed to overcome the difficulties to embed magnetic components of such power range. Like for the embedded solution, the windings are realised with the PCB.

Chapter 3 analyses with more details the selected topology for the front-end converter (PFC). Modular configuration with series or parallel connection are compared. The different possible modulations of full-bridge converters are investigated to analyse pros and cons. The optimisation procedure of the PFC converter is presented. The three main parts of the procedure are detailed.

In **Chapter 4,** results of the optimisation are presented. Two prototypes are evaluated. The first one corresponds to a discrete PFC built with off-the-shelf components. The main assumptions on modulation are validated with this prototype. The second one is the integrated version, the converter is designed by using PCB embedded power dies, inserted components for the gate driver and embedded magnetics. The functionalities of the converter are tested.

In **Chapter** 5, the adaption of the optimisation procedure to power pulsating buffer is presented. As for the PFC, the optimisation results are presented. The impact of magnetic components on this type of converter is analysed. The last part of this chapter presents the realised prototype.

Finally, all the results obtained during this thesis are sum up and conclusions are given. Perspectives of the realised work are also discussed.

Chapter 2

New 3D PCB based inductor concept

In the recent years, PCB embedded components gained interest as presented in Chapter 1. Indeed, the PCB integration, particularly for medium power converters (1kW to 10kW), allows the performances to be enhanced, in particular efficiency and power density. Moreover, PCB process is low cost for mass production because it includes parallel manufacturing processes. Therefore it is very attractive for the industry. PCB embedding of active components is actually well known and mastered. However, it is not the case for the passives, e.g capacitor and/or inductor, especially in the kW range. Indeed, design of passives using PCB integration is more common for low power applications, reducing all the interconnection constraints. The literature review shows that most of works are dedicated to Watt-level integration. PCB integration for higher power range is still a bottleneck for the scientific community, as the size of components is too large. In the kilo-Watt power range the Planar inductor (using “E” and/or “I” cores) is widely used in the industry. It is particularly low cost and can be mass manufactured.

The inductor proposed in this chapter can be realised using toroidal ferrite core and flexible PCBs. The objectives for the inductor are high density and low losses. Nevertheless, multi-functional integration, reduction of interconnection and no requirement of manual intervention for manufacturing or cabling are expected.

2.1 3D folded power inductor concept

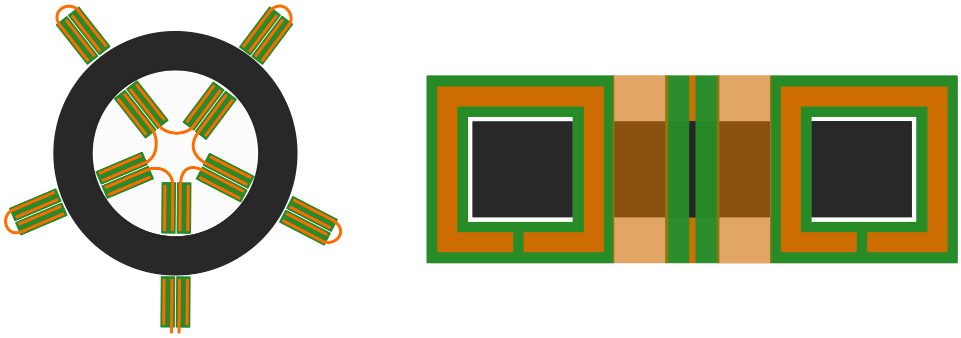

(a) Axial cross section (b) Radial cross section

Figure 2.1.1: 3D Inductor concept

The following concept of inductor has been patented (ref : EP3364428). The concept uses the PCB process to design the winding of the inductor in the planar manner, however the windings are placed around the core. The inductor is built from a classical flat PCB. The concept requires at least two copper layer PCBs for the windings, as it is presented in Figure 2.1.1. The winding is composed of several PCB parts connected by “flex” copper. Hence, it is a solder-less design. The inductor is obtained by bending the different PCB parts. The final inductor has a flower shape, so two bended PCB parts are named a “petal”. The inductor is formed with ferrite cores cut in half and the winding is threaded on the core. It could also be possible to use powder core [34], as the magnetic material can alternatively be moulded around windings. The proposed geometry is mainly limited by the inner diameter of the core and the PCB thickness.

The basic design of each petal with the associated windings for a two layers PCB is presented in Figure 2.1.2. One turn and a half is realised on each PCB part using the Top and Bottom layers. Hence each petal allows three turns to be realised. Therefore this inductor concept limits the number of turns to multiple of three.

All the bending steps from a classical flat PCB to a 3D inductor are presented in the appendix A.1.

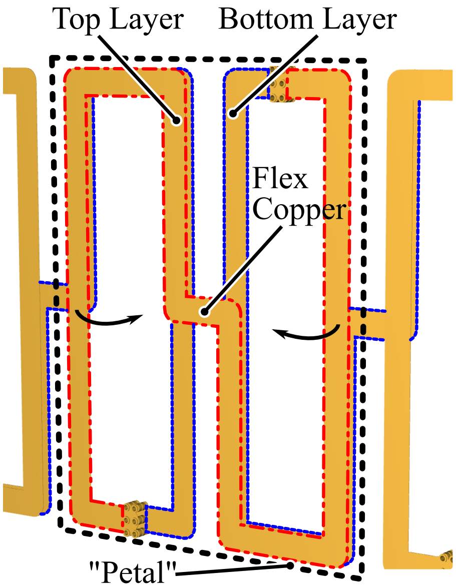


Figure 2.1.2: Basic layout of the 3D inductor

2.2 Design considerations

Before launching any optimisation, mechanical constraints need to be defined according to the PCB process. Two PCB technologies are foreseen for the realisation of the concept. The first one is the Wirelaid® technology (such as in Jumatech GmbH). It consists of thick copper wires embedded in the PCB, these copper wires are used to conduct the current and to bend the different PCB parts. The embedded wires are flat copper pieces of 1.4 mm width and 350 µm thick. The effective copper section is equal to 0.49 mm^2. Each wire is connected in parallel to a track of a at least 1.9 mm width. A pad of 3 x 3.5 mm^2 is placed at the extremities of the track for the connection with the Wirelaid. Resistance welding is used to fix the Wirelaid to the copper foil. Then, the PCB is laminated with the standard process. Therefore, according to this constraint, the track widths for the inductor windings are set to 3 mm, which also define the width of the PCB on each side of the core.

The second technology is the semi-flex, this technology uses classical process. External copper layers are used to bend the different parts. The PCB core is removed under the flexible copper and a flexible solder mask is used on top of

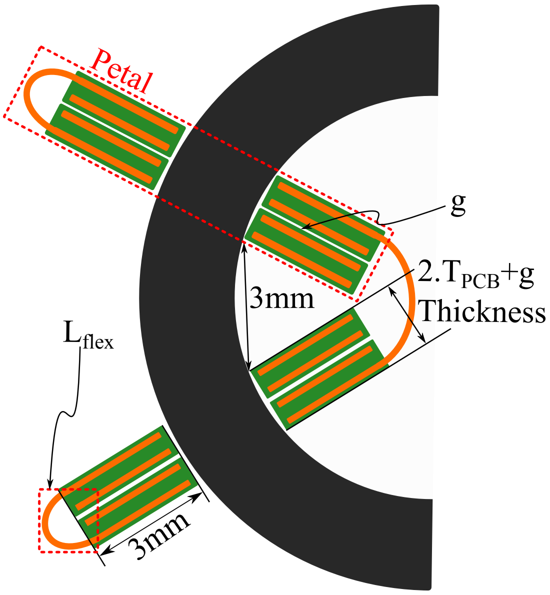


Figure 2.2.1: Determination of the maximal number of petal

the copper. With this technology the copper thickness is largely lower than the Wirelaid. The track width is also set to 3 mm but several copper layers are parallelised to assure good current capabilities and keep the copper section equivalent to the Wirelaid.

The inner diameter of the core cannot be less than 6 mm as the width of the PCB inside the core corresponds to the radius. For a selected core, the maximal number of turns depends on the number of petals. The maximal number of petals is calculated according to the PCB thickness, the minimal distance between each petals and the inner perimeter of the core, see Figure 2.2.1. For the first design the minimal distance between two petals is set arbitrarily to 3 mm for thermal concerns. Indeed, air can flow between two petals.

All mechanical constraints are defined and used in the optimisation procedure presented in the chapter 5 which concerns a power pulsating buffer. The inductor must not saturate and overheat. First, the minimal number of turns is calculated to obtain the required inductance, then rounded above to the closest multiple of three. The air gap is calculated to avoid the saturation with the redefined number of turns. The copper and the core losses are calculated separately. The copper resistance is calculated according to the copper section, the core geometry and

Table 2.1: 3D inductor optimisation results

Inductance	20 µH
Nb Turns	15
Nb Petals	5
Air Gap	2 x 800µm
Material	N87
Core outer Dia.	23 mm
Core inner Dia.	14 mm
Core Height	28 mm

the number of petals. The inductor current is the common data used for the copper and core losses. The core losses are calculated with improved generalised Steinmetz equation (iGSE), more details are presented in chapter 3. The increase in temperature is calculated according to the losses. For a first design, a simple thermal model is used. The surfaces of the corresponding box (S_B), the total losses (P_L) and a constant convection coefficient (h) are used, see Equation 2.2.1. Convection coefficient is set to 50 $\frac{W}{m^2 \cdot K}$ emulating a cooling system.

$$\Delta T = \frac{P_L}{h \cdot S_B} \tag{2.2.1}$$

The maximal temperature is fixed at 100 °C while the ambient temperature is equal to 60 °C. The optimisation results lead to inductor with fifteen turns as the optimum is five petals. The core dimensions are : 23 mm outer diameter, 14 mm inner diameter and 28 mm height. The selected core material is N87 from EPCOS. Results are summarised in the Table 2.1.

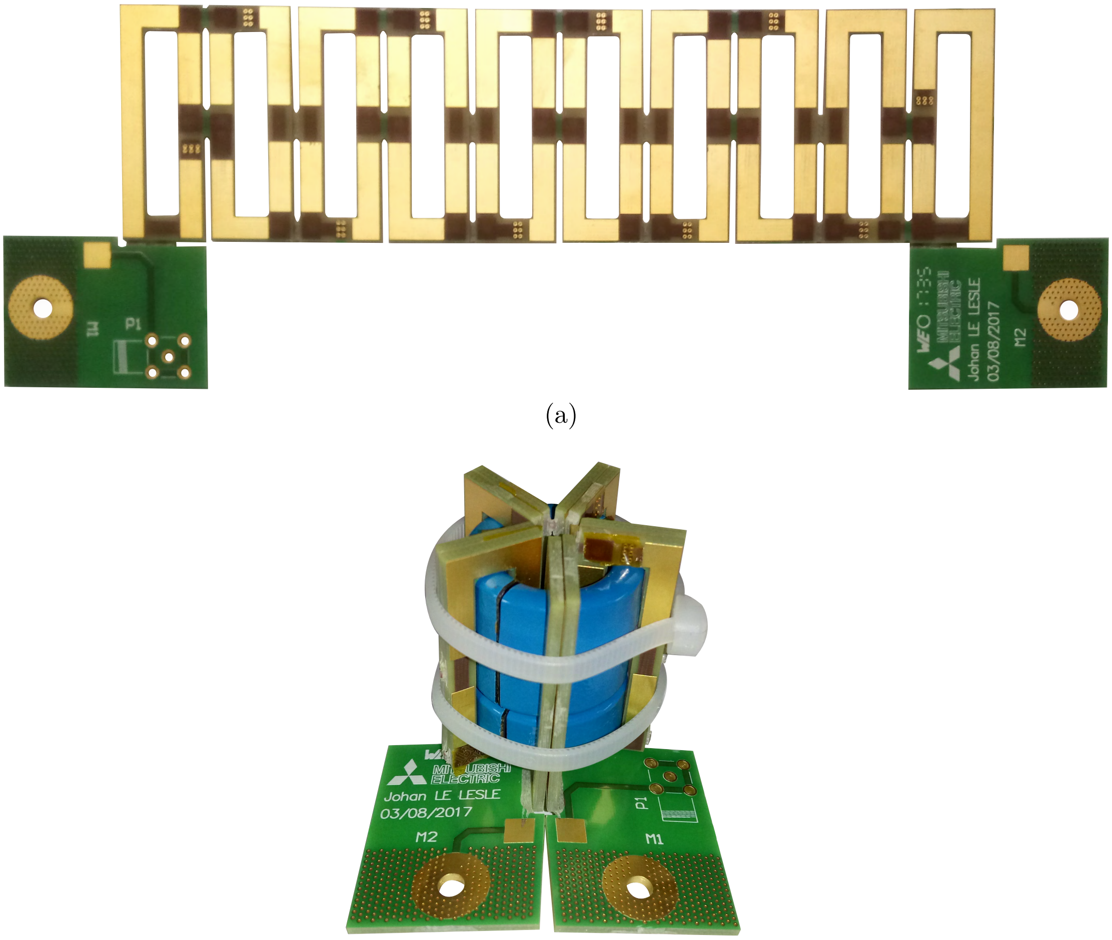
2.3 Prototyping with two PCB technologies

The optimisation results led to a quite high core. To build a prototype as close as possible to the optimum, three cores B64290L0626X087 from EPCOS are stacked. Several prototypes were built with the wirelaid technology and the semi-flex.

Each prototypes are simulated and characterised with a 4294A impedance meter from Agilent. The evolution of the series resistance is analysed as it is a good performance indicator.

2.3.1 Wirelaid technology

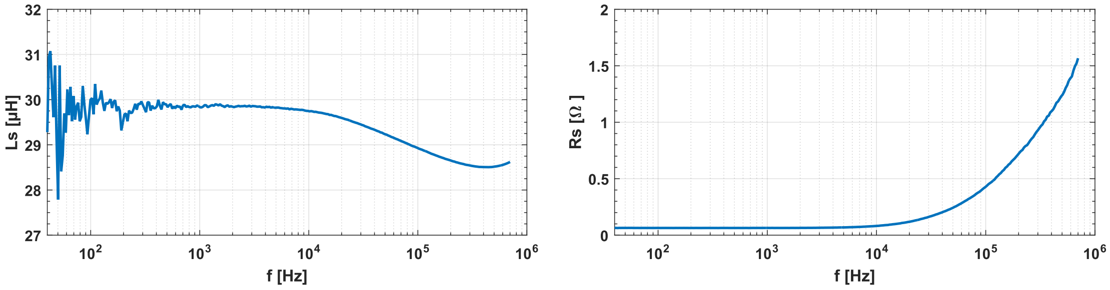
The first prototype uses the Wirelaid technology, it is used to pre-evaluate the feasibility of the concept. The PCB is 1.5 mm thick with four copper layers. The thick copper wires are connected to the internal layers. For thermal aspects, unconnected external layers are used. The first detected drawback is the weakness



(a)

(b)

Figure 2.3.1: Wirelaid prototype



(a) Series inductance (b) Series resistance

Figure 2.3.2: Wirelaid inductor characteristics

of the flexible interconnections realised with the thick copper. The inductor cannot be unfolded. The inductor layout is presented in details in appendix A.2. The bended 3D inductor using Wirelaid is shown in Figure 2.3.1.

The prototype is characterised with a 4294A impedance meter. The equivalent series inductance and series resistance are shown in the Figure 2.3.2. The measured inductance is equal 29 µH that is higher than expected. It can be adjusted through the air gap. But the most constraining characteristic is the series resistance. The increase in resistance for frequencies higher than 10 kHz is significant. It is over 0.5 Ω from 120 kHz. This design can lead to high losses in power converters that usually operate in the hundred kHz range.

To fully understand the reasons of this behaviour, 2D finite element simulations were run on Flux® from ALTAIR. The simulated geometry is a transversal cut in the XY plan. The simulations correspond to a Magneto-Harmonic problem, the mesh is automatically designed by the software to include the skin and proximity effects. With the automatic meshing, triangles are used for surfaces. The resolution of the problem is realised with the Newton-Raphson algorithm. The simulation is realised according to the core height, thus upper and lower PCB parts are missing. The folding area are not included. The external unconnected copper layers are included in the simulation and the air gaps are placed to fit as much as possible to the prototype.

Figure 2.3.3 presents the flux in the inductor. It is possible to notice that leakage flux widely interact with the conductor and the external unconnected copper tracks. The leakage flux generates eddy currents in conductors, increasing the

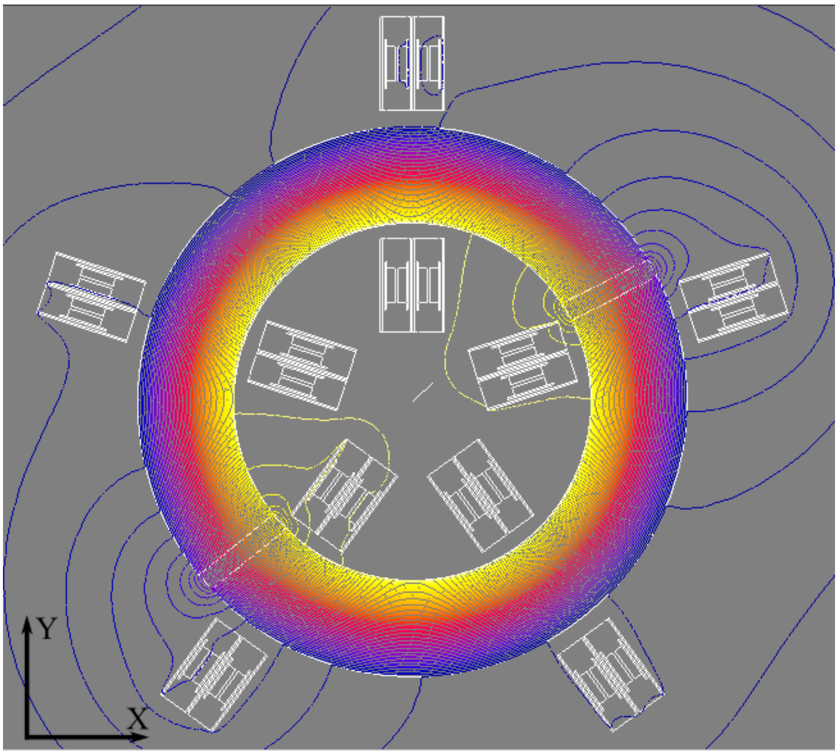


Figure 2.3.3: Flux lines in the Wirelaid inductor (Dark blue = 12 µWb / m, Yellow = 63 µWb / m)

losses. The Figure 2.3.4 presents the current density in the copper of the internal part of the petals. It highlights that induced currents are flowing through the unconnected copper. The skin effect is also very important. These issues are even more significant on the petals close to the air gaps. Notice that with the selected scale the current in the unconnected copper close to the air gaps cannot be fully displayed.

An increase of losses is regarded as resistance increase by the impedance meter. The series resistance calculated with simulation and the measure are compared in Figure 2.3.5.(a). The result obtained with the simulation are very close to measure. The high frequency behaviour is well estimated. The presented phenomena are clearly responsible of the strong increase of the resistance. Sustainable solutions can easily be provided. The first one is removing the unconnected copper that acts as shielding and sees lot of induced currents. The second one consists to place air gaps as far as possible to the petals. The best position is between two petals,

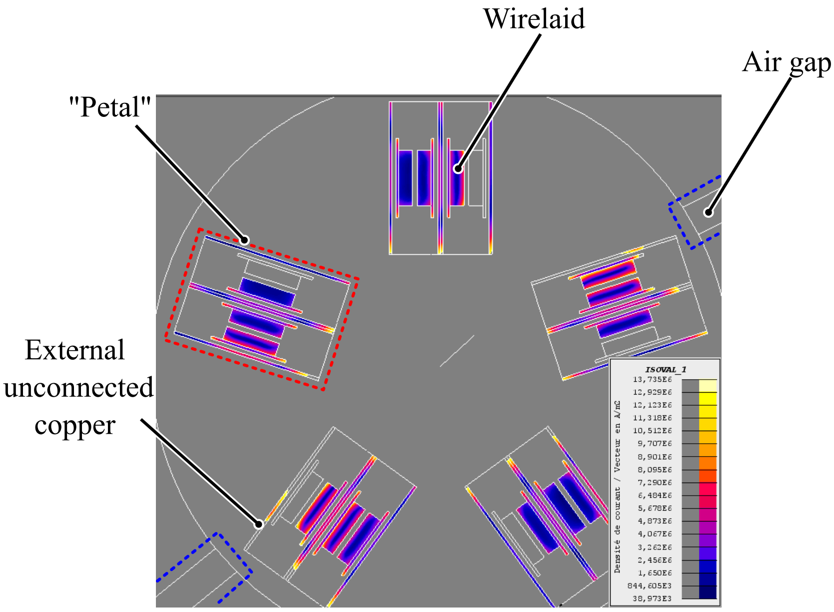


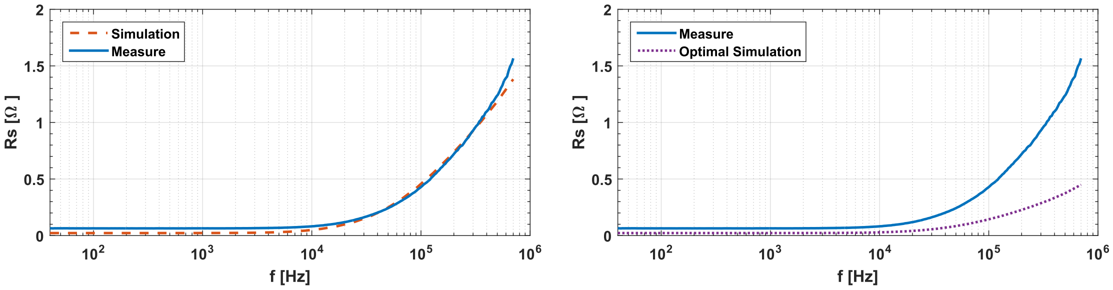
Figure 2.3.4: Current Densities in the Wirelaid inductor at 250 kHz (Dark blue = 38 kA / m^2 , Yellow = 13 MA / m^2)

equidistant from them. Indeed, the interaction of leakage flux with conductors can be consistently reduced. Simulation with optimal air gap positions and removed external copper is compared to the measurement in the Figure 2.3.5.(b). It highlights that the performances can be substantially improved by slight changes in the design. Reduction of the resistance by 50 % at 140 kHz can be achieved.

The investigations on the Wirelaid inductor are promising, the feasibility of the concept is fully validated. The simulations show possible improvements on the technology. Despite this, the Wirelaid technology is expensive and the interconnections are the weakness of the prototype. Hence, a new design using another PCB process is investigated.

2.3.2 Semi-flex technology

The studied solution in this section is the semi-flex. This PCB process is well known and mastered by PCB manufacturers making the price more attractive and also shorter delivery times. This technology is more suitable for mass-production. The main limitation of the technology comes from the copper thickness proposed



(a) Prototype configuration (b) Optimal configuration

Figure 2.3.5: Simulated series resistance vs measured

by some manufacturers, the copper used for the bending parts is only 60 µm thick. This is an issue when high currents are flowing through the inductor. To overcome this issue, multi-layer PCBs are used and some layers are parallelised in the rigid part to achieve a copper cross-section of 0.6 mm². Concerning the flex parts, large copper planes are used to handle mechanical and electrical stresses. Details on the inductor layout are presented in appendix A.3.

As the copper thickness is lower, the bending is less stressed and the technology is more flexible than the one using thick copper. Interesting feature for prototyping is the capability to disassemble the inductor.

Two prototypes are proposed, the first one is vertically oriented (see Figure 2.3.6.(b)), as the Wirelaid, and the second one is horizontally oriented (see Figure 2.3.6.(a) and (c)). These prototypes are built with 1.2 mm PCB thick with six layers 60µm and 70 µm copper thick, for outer and inner layers, respectively. Contrary to Wirelaid the flex coppers are the external layers. The length of the copper planes are calculated to obtain a 180° bending radius. It is determined according to the width of one petal that depends on the PCB thickness, and the small gap between the two PCBs (see Equation 2.3.1).

$$L_{flex} = \frac{\pi \cdot (2 \cdot T_{PCB} + g)}{2} \tag{2.3.1}$$

In this case the PCB thickness is 1.2 mm and the assumed space (g) is 0.5 mm, thus the length of the flex part is 4 mm. This length gives the most homogeneous

(a)

(b)

(c)

Figure 2.3.6: Semi-flex inductor prototypes

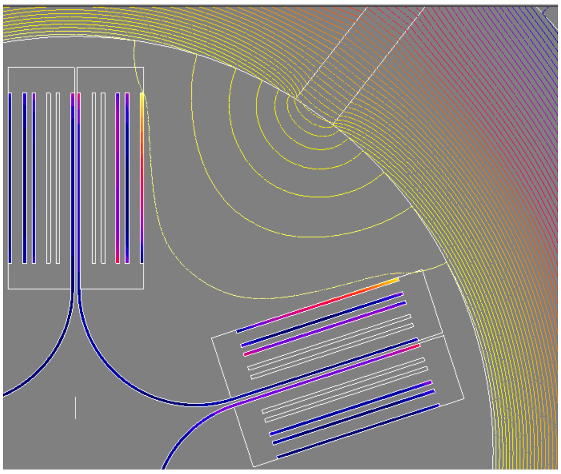
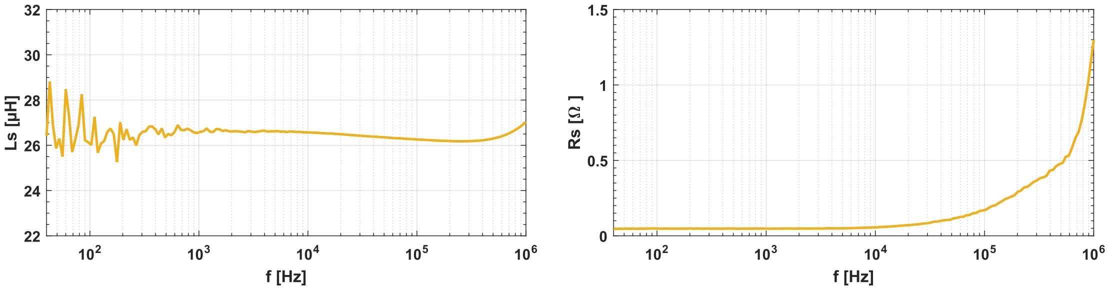


Figure 2.3.7: Flux lines in the semi-flex 3D inductor (Dark blue = 12 µWb / m, Yellow = 63 µWb / m)

bending radius. In theses designs, with five petals, the cores are not cut in two identical halves, to ensure the air gaps as far as possible from the petals.

The interactions of leakage flux with the winding are investigated for this new design. The results are presented in the Figure 2.3.7. It can be clearly seen that the deviation of the flux lines is lower than in the previous case (where air gaps were close to the petals). The proximity effects are still present but reduced. The impedance of the inductor is also measured with the impedance meter, the results are presented in the Figure 2.3.8. The inductance is still higher than the expected value. The improvement on the series resistance is discussed in the next sub-section.



(a) (b)

Figure 2.3.8: Semi-flex inductor characteristics

2.3.3 Performances comparison

This sub-section compares the performances, series resistance and volume, of the two 3D inductors to each other and to classical planar inductor. A planar inductor is designed for the operational conditions as it is the inductor used for the PPB presented in the Chapter 5. The value of the inductor is also 20 µH. The planar inductor (see Figure 2.3.9) is realised with six layers, 105 µm thick copper. The copper tracks are limited by the width of winding window of the E core. Therefore, the planar copper section is significantly larger than the flex inductor.

Firstly, the two 3D inductor are compared to each other. The improvement achieved by the investigations on the Wirelaid and the implementation on the new prototypes are very interesting. The equivalent series resistance behaviour of the two 3D inductors designed with the two PCB technologies are presented in the Figure 2.3.10. The resistance rise is consistently reduced, the high frequency behaviour is widely improved. For example, the Wirelaid resistance at 120 kHz is equal to 500 mΩ whereas the flex resistance is only 200 mΩ. This represents a reduction of 60 %. This analysis and comparison highlight the impact of possible unconnected copper close to magnetic field. The placement of air gap in magnetics is also an important point that widely impact the losses. The leakage fluxes induce eddy currents, thus, spaces are required between the air gap and the winding. This is more relevant with copper tracks, indeed the surfaces are more important than round wire and the skin/proximity effects are impacting more the design. The conduction losses can be widely reduced with the last 3D inductor design.

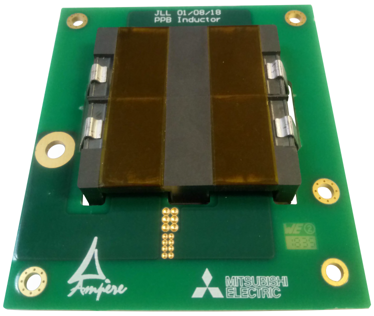


Figure 2.3.9: 20 µH planar inductor

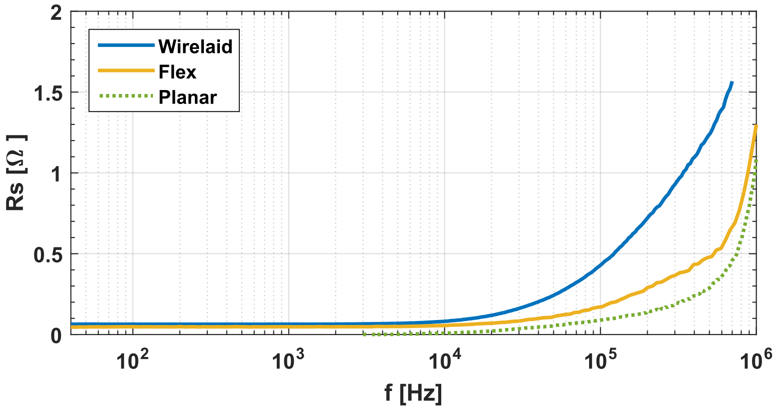


Figure 2.3.10: Comparison between Wirelaid, Semi-flex and Planar

Therefore, the new 3D inductor is a good candidate for magnetics using PCB process in the kilo-watt range. Further investigations are presented below.

Despite good improvements on the second prototype, the series resistance of an equivalent planar inductor is lower than the 3D inductor. At 120 kHz the planar resistance is only 100 mΩ that is half of the flex. However, the number of parallel layers for the flex design can be increased to reduce the series resistance to compete with the planar.

Regarding size, the horizontal-oriented flex inductor is compared to the planar. The box volume of the planar inductor is equal to 67.42 cm^3. The flex inductor has a box volume of 76.6 cm^3 if the connecting pads are included, and 50.65 cm^3 if they are not. Therefore, the volume of the proposed inductor can be significantly lower. The main advantage of the folded inductor is the use of flexible PCBs, permitting further integration freedom. The overall system (including dies, capacitors, resistors, etc) can be designed with more complex shapes without additional connectors for PCB interconnections. Analysing the foot print, the surface used by the flex inductor, 20.35 cm^2, is lower than the one used by the planar inductor, 49.6 cm^2.

2.4 Loss calculation based on calorimetric measurements

The performances of the semi-flex prototypes are evaluated as it is the 3D solution that presents the most interesting performances according to the previous tests. The designed inductor should handle a current composed of low (50 Hz) and high frequency (140 kHz and harmonics) components. Therefore, test bench dedicated to losses measurements is implemented to determine the inductor losses under such conditions.

2.4.1 Excitation circuit

The converter topology presented in the Figure 2.4.1 is used to characterise the inductor. The advantage of this kind of circuit is the possibility to use low voltage and low power DC supply. Indeed, the tests performed hereafter are realised under $30\,\mathrm{V_{DC}}$, and are compatible with any lab DC power supply. The DC supply is only used to provide the losses of the H-Bridge circuit and the inductor. Nonetheless, the current flowing through the inductor is representative of a typical current in the application. The current is composed of a low frequency component and a high frequency component. The switching frequency can be controlled either with oscillator integrated in the circuit or either from a signal generator. In the case of the oscillator, the carrier corresponds to a 140 kHz triangle. The signal generator input can be used if another switching frequency is required. The low frequency current is also controlled by a signal generator. The circuit presented in the Figure 2.4.2 is a two layer PCB with 70 µm copper thick.

2.4.2 Calorimetric methods

Losses can be estimated with electrical methods using Wattmeter or oscilloscope. However, voltage across inductors in power converters presents very high $\frac{dV}{dt}$. Thus, expensive Wattmeter with a high bandwidth is required. Inductor loss measurements with oscilloscope are also lacking of accuracy due to the requirement of a very precise phase measurement. Thus, the calorimetric method for loss

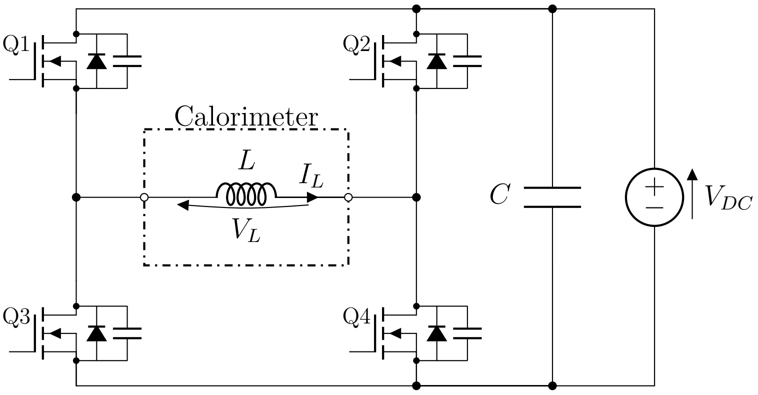


Figure 2.4.1: H-Bridge topology used for calorimetric measurements

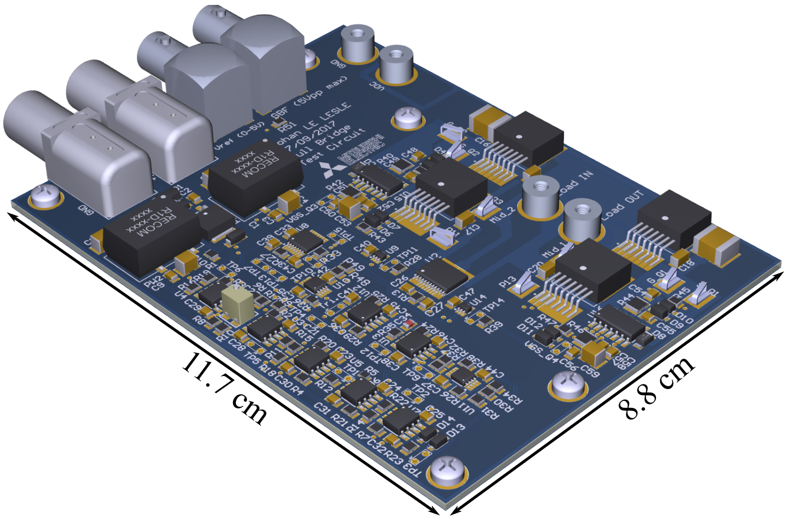
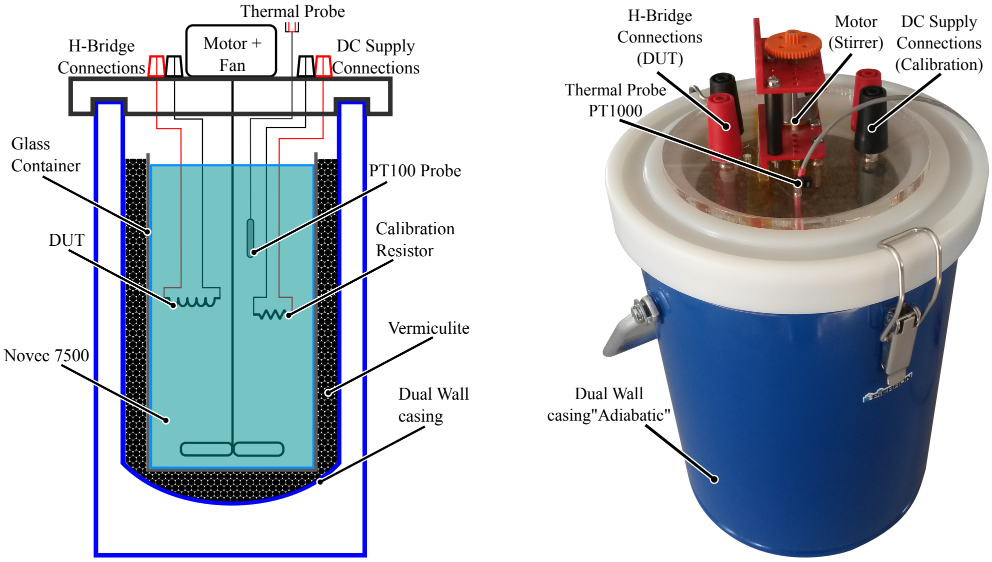


Figure 2.4.2: 3D model of the H-Bridge circuit



(a) Schematic (b) Set-up

Figure 2.4.3: Calorimeter

measurements is considered as the most simple and accurate method compared to electrical ones.

The previous circuit is associated to an inertia calorimetric set up that is used to measure the losses of the device under test (DUT), in this case the 3D inductor. All the elements used in the calorimeter are presented in the schematic of the Figure 2.4.3. The DUT is immersed in a dielectric solution inside an almost adiabatic enclosure. Usually, oil is used in such experimental set up due to good dielectric properties. However, the main drawback is the difficulty to clean up the DUT after the measure. DUT is almost unusable for other experiments. To overcome this drawback, another liquid is used: the Novec 7500 (3M). It has good dielectric properties (breakdown voltage >35kV for 2.54 mm). This liquid is usually used for immersion cooling. Moreover, the boiling temperature is 128 °C which is sufficient for experiment slightly lower than 100 °C. Finally, it is a non-oily texture, so the DUT is perfectly clean when the experiments are complete.

The temperature of the solution is automatically measured with the PT1000 connected to a Keithley 2700 precision multimeter. The data acquired with this multimeter is then uploaded on a PC running Matlab using LAN/GPIB gateway

(Agilent E5810A). The losses of the device are basically given by Equation 2.4.1, where M_i are the different masses in the system and Cp_i the different heat capacity of the different elements. With this method a calibration is required before each set of measures.

$$P_{DUT} = \sum(M_i \cdot Cp_i) \cdot \frac{dT}{t} \tag{2.4.1}$$

Before any measurement is performed, the temperature inside the calorimeter is raised to 30°C (by dissipating some power in the DUT). This ensures that the temperature of the bath is slightly above the ambient temperature and that the heat losses of the calorimeter are controlled. A stirring system ensures an homogeneous temperature in the bath (the stiring motor is kept out of the calorimeter to avoid unwanted heat dissipation). The next step is the calibration of the heat capacity of the calorimeter: a known amount of energy is dissipated in the bath (using an electric resistance, a DC power supply, and voltammetric measurements). The calibration with the resistor allows to identify $\sum(M_i \cdot Cp_i)$ (Equation 2.4.1). Once the calibration has been made, the DUT is operated for a set amount of time, and the corresponding temperature rise is measured, as presented in the Figure 2.4.4. A linear regression is determined from the temperature decreasing slope to calculate the dT. If the enclosure is well thermally insulated, the curves are parallel. The experimental procedure can be summarised as follows.

- Step 1 : Increasing of temperature with the DUT for homogenisation
- Step 2 : Rest time, decreasing of the temperature due to not perfectly adiabatic enclosure
- Step 3 : Impulse of power in the resistance for calibration
- Step 4 : Rest time
- Step 5 : Impulse of power in the DUT
- Step 6 : Rest time

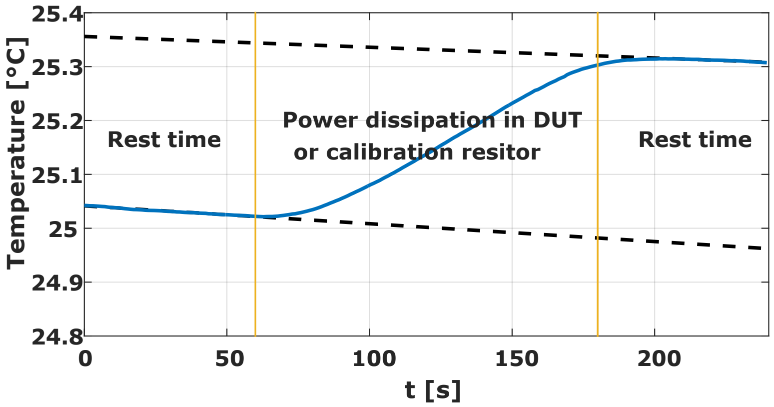


Figure 2.4.4: Typical calorimetric curve for calibration or for measurement

The precision of the set-up is calculated from all sources of errors that includes equipment uncertainty and error from the operator. Two measurements are performed, the first is the calibration and the second is the losses measurements for the DUT. Hence some errors are cumulated. For the calibration, identified errors come from the voltmeter, the amperemeter, the thermal probe and the error on the heating time as the start and stop are not automatic. The global error during the calibration can be calculated by the Equation 2.4.2. All the errors are presented in the Table 2.2. The errors from the voltmeter and amperemeter only depends on the used range, in this case 10 V and 10 A, respectively. The absolute error on the temperature measurement cancels out because temperature is measured in a relative way (final temperature minus initial temperature). Only the relative error has an effect, hence the low impact of the temperature measurement on the total measurement error. The highest source of error is on the time: the shorter heating time, the higher the error. The total error on the measurement, for the DUT, is calculated by Equation 2.4.3, including the errors on temperature and time plus the error from the calibration. For example, for a heating time of 60 s during the calibration and the measure, the final error is equal to 4.49 %. Hence, calorimetric measures are considered as a good method to determine the losses in the 3D inductor.

$$\epsilon_{calib} = \frac{\Delta V}{V} + \frac{\Delta I}{I} + \frac{\Delta t}{t} + \frac{\Delta dT}{dT} \tag{2.4.2}$$

Table 2.2: Measurement errors

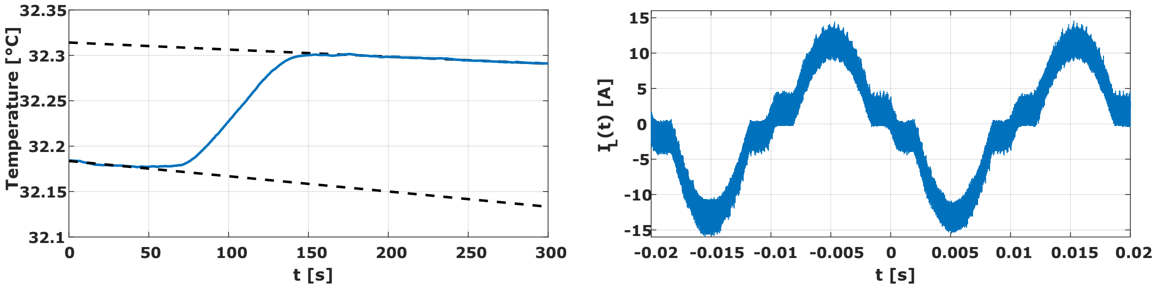
Equipment	Variable	Error	Percentage
Voltmeter U1242B	ΔV	± 11 mV/10 V	0.11 %
Ammeter U1242A	ΔI	± 65 mA/10 A	0.65 %
PT1000 Class A	ΔdT	± 0.15 °C+0.002 [T°C]	0.2 %
time estimation	Δt	± 1 s/Heating time	-

$$\epsilon_{meas} = \frac{\Delta t}{t} + \frac{\Delta dT}{dT} + \epsilon_{calib} \tag{2.4.3}$$

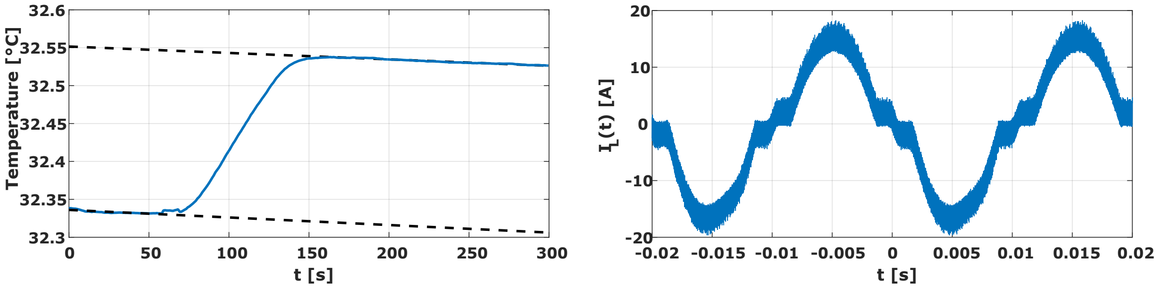
2.4.3 Results

Losses for the semi-flex inductor are determined for several current values. Three sets of measures are performed, the effective inductor current increases for each measure. The effective current values (including HF) are 7.5 $\mathrm{A_{RMS}}$, 10.3 $\mathrm{A_{RMS}}$ and 12 $\mathrm{A_{RMS}}$. The inductor nominal current is 10.25 $\mathrm{A_{RMS}}$, including LF and HF. However, the high frequency component of this current is largely higher than the high frequency component of the currents flowing through the inductor during the calorimetric measurements. All the temperature curves that are used to calculate the losses and the corresponding injected currents are presented in Figure 2.4.5. The heating time is equal to 60 s for the two phases of experiment (the calibration and the measures on the DUT). The calculated losses are equal to 3.57 W, 5.52 W and 7.18 W, respectively. All these results are presented in the Figure 2.4.6 including the uncertainty of the measure.

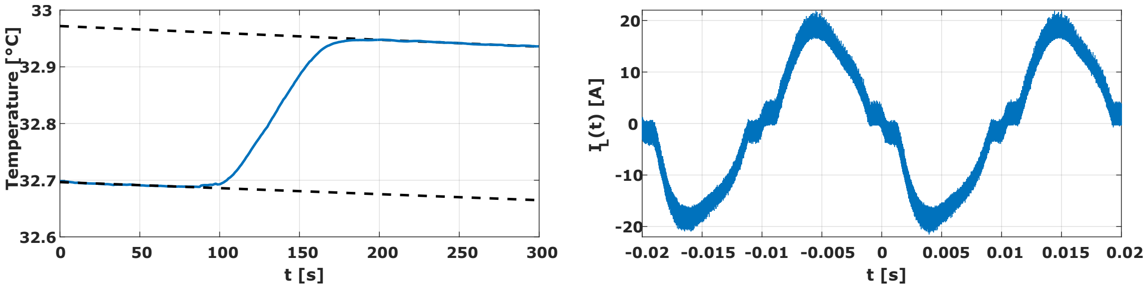
In the case of the current of 10.3 $\mathrm{A_{RMS}}$ for the calorimetric experiment the measured losses are equal to 5.52 W. The repartition of losses, copper and core losses, can be determined according the calorimetric measurements and also impedance measurements. The two components (LF and HF) of the injected current can be used to evaluate the copper losses. In the case of the 5.52 W total losses, the effective value of the low frequency component is equal to 10 $\mathrm{A_{RMS}}$ and



(a) Temperature curve at 7.5 $\mathrm{A_{RMS}}$ (b) Inductor current 7.5 $\mathrm{A_{RMS}}$



(c) Temperature curve at 10.3 $\mathrm{A_{RMS}}$ (d) Inductor current 10.3 $\mathrm{A_{RMS}}$



(e) Temperature curve at 12 $\mathrm{A_{RMS}}$ (f) Inductor curve 12 $\mathrm{A_{RMS}}$

Figure 2.4.5: Results of calorimetric measurements

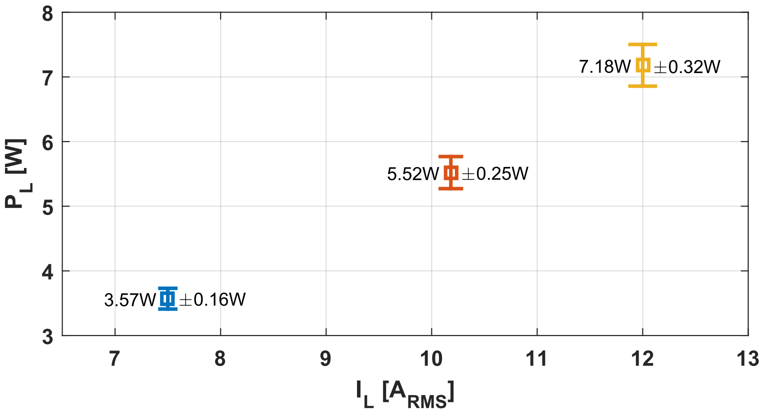


Figure 2.4.6: 3D Inductor losses according to the effective current

the effective value of the high frequency component is equal to 1.13 $\mathrm{A_{RMS}}$. The corresponding series resistance are determined from the impedance measurement (Figure 2.3.10), the 50 Hz resistance is equal to 47 mΩ and the 140 kHz series resistance is equal to 227 mΩ. The copper and core losses can be calculated according to the Equation 2.4.4 and Equation 2.4.5.

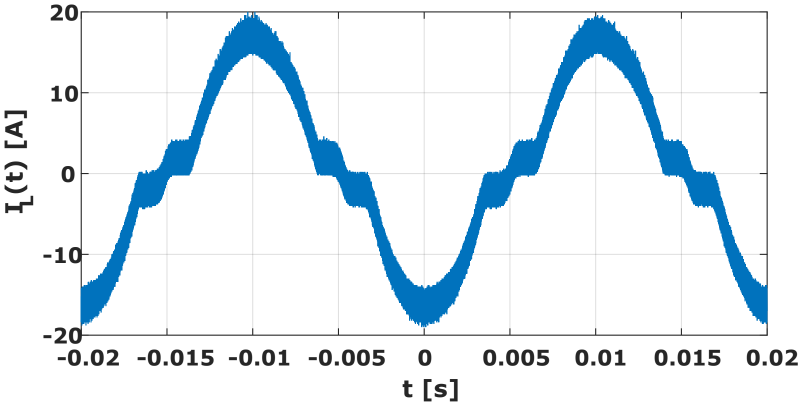
$$P_{Copper} = R_{LF} \cdot I^2_{LF_{RMS}} + R_{HF} \cdot I^2_{HF_{RMS}} \tag{2.4.4}$$

$$P_{Core} = P_L - P_{Copper} \tag{2.4.5}$$

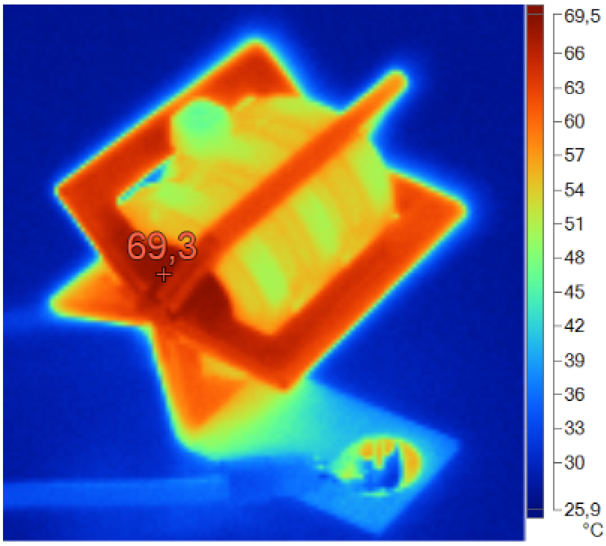
Copper losses are equal to 4.98 W. The main part comes from the low frequency current with 4.7 W, the HF losses are equal to 0.28 W. According to the calorimetric measurements, the core losses are estimated to be 0.54 W. Therefore, it can be concluded that the conduction losses are the main heat source. Indeed, the injected current is mainly pulsating at 50 Hz. The skin effect is very low and the core is not stressed.

To fully validate the optimisation model, similar tests should be performed with the same current as the optimisation. However, this is more complicated to execute.

2.4.4 Thermal measures



(a) Inductor current 10.3 $\mathrm{A_{RMS}}$



(b) Thermal measure realised after 10 min in steady state

Figure 2.4.7: Thermal behaviour investigation

One important point in power electronics is the thermal management. The lower the losses, the simpler the thermal management. With calorimetric measurements, losses are calculated for fixed current. Since the heating time is very short and the environment does not correspond to the real operational conditions, further tests are performed to analyse the thermal behaviour of the new inductor. The inductor is tested in natural convection cooling under 10 .3 A_{RMS} that corresponds to 5.52 W dissipated power. The ambient temperature is equal to 25 °C and the measures are realised with the Fluke Ti10 thermal imaging infrared IR camera, Figure 2.4.7b.The thermal image shows that the inductor windings are the hottest part, especially the flex parts, even if the length is short. Indeed, only one copper layer is used for the bending and carrying the current. In the present test conditions, the main part of the losses comes from copper, confirming the loss estimation with calorimetric measurements. The increase in temperature is about 44 °C, leading to a peak temperature of 69 °C without any cooling system. This indicates that with the appropriate cooling system, for example a direct forced air cooling, the proposed inductor is able to support higher current. The 3D PCB design increases the number of surfaces in contact with the air flow that increases the efficiency of the cooling. Thus, the volume of the inductor can be reduced.

2.5 Conclusions

The higher the power level, the bigger the components, especially the magnetics, making the PCB embedding very complicated. It requires large and thin magnetic core that can be very sensitive during the lamination process. The proposed 3D inductor overcome this issue. The PCB windings are bent around the core without risk of break. The 3D inductor concept is validated with two PCB technologies.

The first one is the Wirelaid technology, it uses thick copper wires able to handle high current and assures the flexible interconnection. The main drawback is the impossibility to unfold the inductor without breaking the winding. Hence, this is very fragile. Investigations on the first prototype using 2D simulations highlight some design rules. First, all the copper layers must be used to limit induced current. The position of the air gaps is also an important point. The leakage flux from the air gap contribute to high frequency effects such as eddy currents. The optimal position corresponds to air gap placed between two petals, at equal distance. This position involves to cut the core adequately with the number of petals. All these improvements are included in the second version of the 3D inductor.

The second prototype uses the semi-flex PCB technology that is more sustainable. The characterisation of the inductor shows a significant improvement of the series resistance. At 120 kHz the resistance is reduced by 60 %. Therefore, this new design can be used in power converters in the kW range.

Calorimetric experimental set-up is settle to further investigate the final design. The experimental conditions are close to the real operation. The current injected in the inductor is composed of low and high frequency components. For a current of $10.3\,\mathrm{A_{RMS}}$ the losses are equal to 5.52 W that is a satisfying value. The thermal behaviour is also analysed for this value of losses. The inductor is tested in natural convection. The temperature increase is 40 °C. This value can be reduced with proper thermal management. All this tests and simulations validate the concept. The proposed method to design magnetics using the PCB process is very interesting, especially for the industry as it is low cost for mass production. The manufacturing process can be simplified by using iron powder moulded around the PCB windings. Moreover, this conception method is not only limited to magnetic. More complicated designs including power dies, gate drivers, decoupling capacitors, can be considered. For example, a complete commutation cell, including magnetic, can be designed without additional connectors, keeping the advantage of mass production.

Even if the concept is validated, more investigations are required. The main point is the thermal management. As the surface is important the 3D inductor is very interesting with air flow on the inductor itself. However, in the case of natural convection associated with cold plate, it is more complicated due to the particular geometry. The actual project consider only naturally cooled cold plate. This is the main reason why the new 3D inductor is not included into following converter prototypes even if good performances are expected with this new concept.

The following presents the optimisation procedure implemented to design AC/DC converter. The procedure is adapted for discrete and also highly integrated converter. The PCB integration continue to be an important aspect of this project. Converter prototypes are built and tested.

Chapter 3

Design methodology for high efficiency discrete and integrated converters

3.1 Introduction

The selection of the suitable topology according to the specifications and the development of an appropriate optimisation procedure are important. Both enhance the converter performances. This chapter presents the selected topology. Different control possibilities associated with this topology are investigated to analyse their impact on efficiency and power density. The use of power inductors is inherent to power electronics, whether for filtering or for energy storage. Hence, the development of an optimisation procedure compatible with integrated converter, including power inductors, is mandatory. Nevertheless, the integration of power inductors is still a challenge as the size of these inductors is still large. The actual trend to reduce the size of passives is the increase in the switching frequency, made possible through the development of wide band gap components. But this leads to other issues such as the increase of semiconductor losses and EMI that need to be considered. Hence, the design procedure presented in this chapter includes all these aspects. The methodology used to generate all the useful waveforms is presented. Then the developed optimisation procedure divided into three main parts is detailed. These three parts correspond to the selection of the semiconductors, the design of the input filter (Differential Mode DM, Common Mode CM) and the magnetic design. The procedure is used for both discrete and integrated converters.

3.2 Integration-friendly topology selection

Several topologies have been presented in Chapter 1, among those and according to the project specifications, reminded in Table 3.1. To improve the performances of the converter, it is possible to associate multiple elementary cells and develop a modular design approach. The full bridge topology is selected as a building block elementary cell which could be associated in series or in parallel. This association is then used to build the Power Factor Corrector (PFC). Advantages of the full bridge are, the reasonable number of devices in the current path, extended control possibilities which allow the input inductor to be reduced, and genericity to build a single integrated elementary cell that can be used in several applications. The selected topology is illustrated in Figure 3.2.1.

Two associations are studied, the series connection, with split DC BUS, and the parallel association. With the appropriate control of each cell, both topologies allow passives to be reduced in terms of value, consequently the volume can be reduced, which is key for HiCon where passive embedding is a major challenge. The higher the number of cells, the lower the input inductor [35]. Moreover, the

Table 3.1: PFC specifications

Input Voltage Range	85-260 V_{RMS}(AC)
Maximal Input Current	15 A_{RMS}(AC)
Maximal Output Current	12 A (DC)
Output Voltage	400 V (DC)
Maximal Output Power	3.3 kW
Working Environment	-40 to 60°C
E.M.C	EN55011 Class B conducted EMI

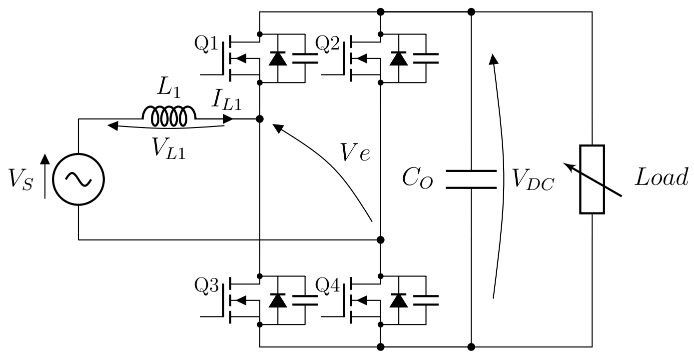


Figure 3.2.1: Selected elementary cell

multi-cell design allows the power to be spread out between the different cells, hence it simplifies the thermal management.

3.2.1 Series association

The series association, illustrated by Figure 3.2.2, allows low voltage devices to be used which make silicon (Si) competitive with Wide Band Gap (WBG) components, hence the converter can be more cost effective. With this type of association, as the overall current is flowing through several devices, it is preferable to select semiconductors with a low on state resistance in order to keep conduction losses low. A drawback of the series topology is the low efficiency at light load operation, because all the cells must be kept operational. Moreover in the case of device failure the converter cannot continue to operate, excepted if semiconductor fail to short, which is not generally the case for devices implemented in such power range applications.

DC links are independent, commonly, isolated converters are required and connected to each DC link capacitor. The secondary of the transformer is connected in series or in parallel according to the application and requirement (high current or high voltage) [35]. This topology (Modular Multilevel Converter MMC) is widely used in railway applications needing to deal with high voltage [36]. Hence, this configuration involves some constraints on the DC side. Indeed, in the case of a non-isolated PFC this assembly is not suitable.

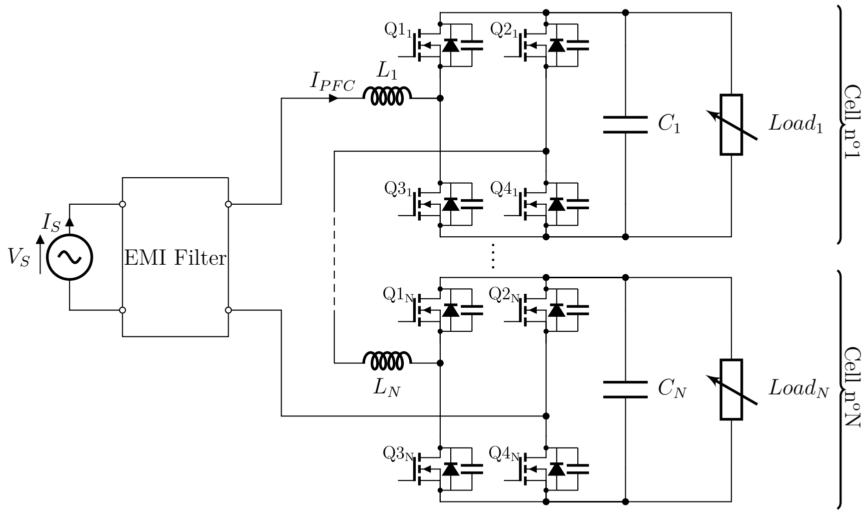


Figure 3.2.2: Topology of multilevel converter composed of N cells

3.2.2 Parallel association

The second possibility is the parallel association, see Figure 3.2.3. In this case, the complete DC voltage is applied to the devices. Dies with low switching losses must be used, e.g. Silicon Carbide (SiC) or Gallium Nitride (GaN) components. The different cells can easily be deactivated at light load to maintain high efficiency. This behaviour is also applicable in case of device failure. It is better if the defective component fails in open circuit, which is commonly the case. Hence, the converter can operate in degraded mode.

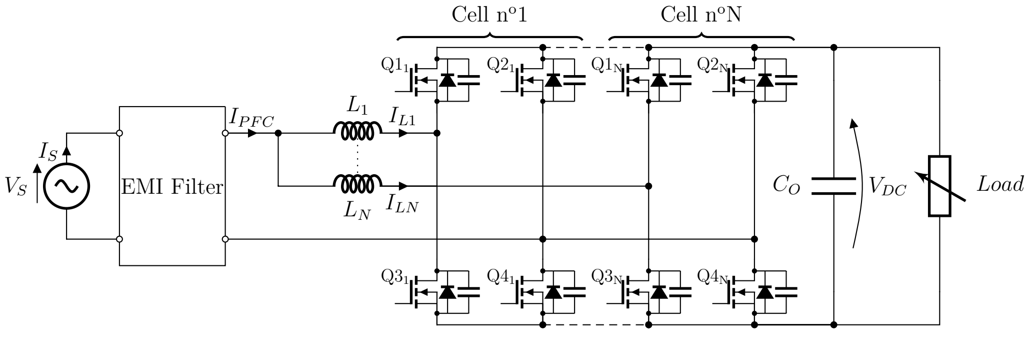


Figure 3.2.3: Topology of the interleaved PFC composed of N cells

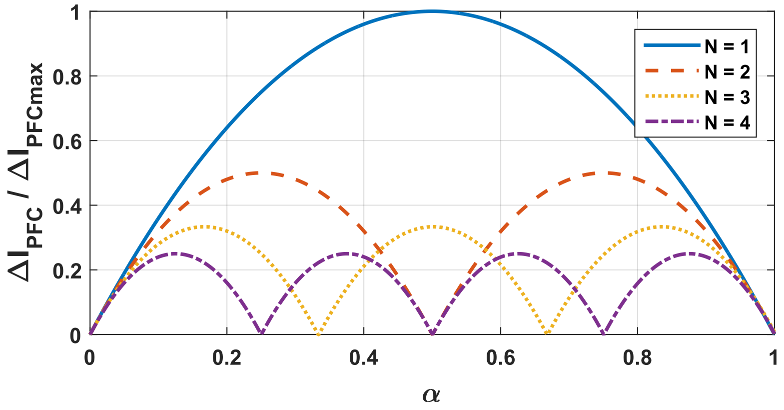


Figure 3.2.4: Impact of interleaving on the input current ripple

Figure 3.2.4 illustrates the input current ripple as a function of the number of interleaved cells (N) and the duty-cycle (α). All the curves are obtained for the same switching frequency and inductance. The reduction of input current is achieved by shifting the carrier of the different cells accordingly to the switching period. The sum of the different current leads to a reduction of the global current ripple and an increase in the apparent frequency.

Therefore, with a constant input inductor value, the current ripple is reduced so the EMI filter can be reduced. The other possibility is to keep constant the input current ripple to reduce the inductor value.

To sum up this part, contrary to series association, parallel topology is more appropriate for WBG components, the passives can be reduced, the efficiency can be enhanced even at light load and availability increased. The parallel association presents best behaviour than the series one for partial load operation. Hence, for all these advantages, the parallel association will be used for the converter design.

3.3 Modulation & conduction modes

3.3.1 Modulation

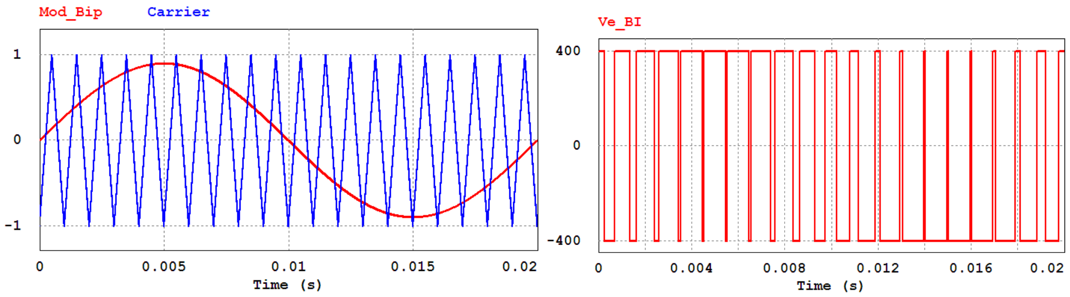
The full bridge topology can be controlled with different modulations. The control scheme widely impacts the converter design. The modulation impacts the size of passives such as input inductor and EMI filter, and also impacts the losses.

Two modulation schemes are identified, the bipolar modulation and the unipolar modulation. The unipolar modulation can be achieved with two methods. In the first one, all switches are controlled with high frequency pulse width modulation (HF PWM). In the second one, a part of devices are controlled at low frequency (grid frequency) and others are controlled with HF PWM. These three principles are presented hereafter.

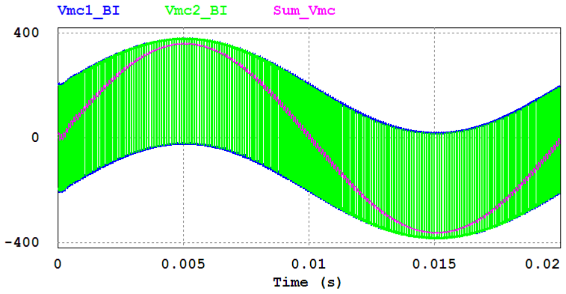
The common mode behaviour of each modulations is analysed. The results are obtained by simulating a full-bridge converter on PSIM. The global common mode voltage is obtained by summing the voltage between Mid-point and earth of each converter legs defining the common mode behaviour.

3.3.1.1 Bipolar modulation

The bipolar modulation is a two level modulation, the bridge input voltage (Ve(t) see Figure 3.2.1) can only be $\pm V_{DC}$, all devices are complementarily controlled (see Figure 3.3.1).



(a) Modulation & carrier (b) Input voltage waveforms



(c) Common Mode voltage

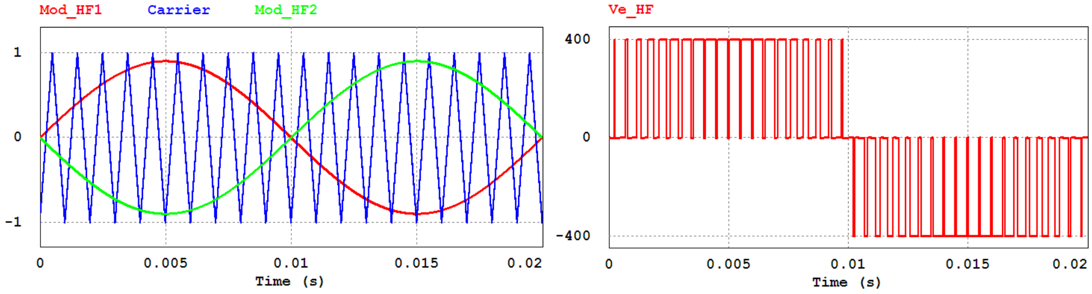
Figure 3.3.1: Bipolar modulation

Among the three principles presented here, the bipolar modulation requires the highest input inductor (see Section 1.5). However this modulation presents good behaviour for CM perturbations as the equivalent CM voltage is mainly a 50 Hz voltage [76].

3.3.1.2 HF PWM unipolar modulation

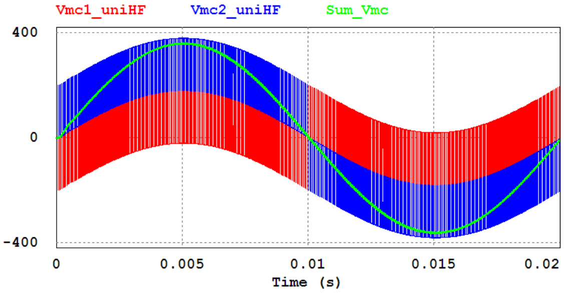
The HF unipolar modulation is obtained by using two modulations, one per leg, in phase opposition. This modulation brings a third state during which Ve(t) = 0V (see Figure 3.3.2). One advantage of this modulation is the higher apparent switching frequency. For a required current ripple the input inductor is reduced, four times lower than the bipolar modulation because the voltage variation is only 0 to V_{DC} and the apparent switching frequency is twice the switching frequency, which allows the DM filter to be significantly reduced.

The common mode behaviour with this topology is also good because the sum of the common mode voltage presents a 50 Hz component.



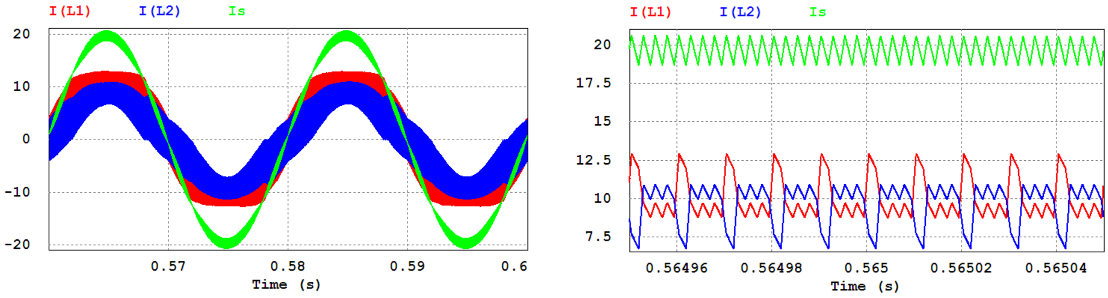
(a) Modulation & carrier

(b) Input voltage waveforms



(c) Common Mode voltage

Figure 3.3.2: HF Unipolar Modulation



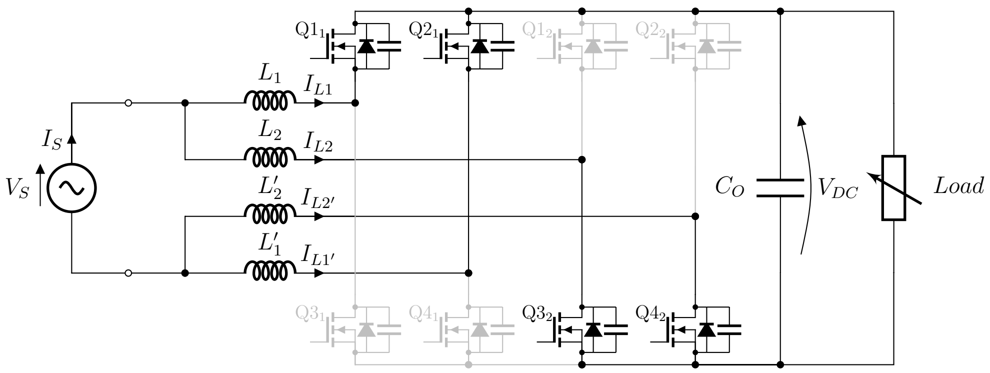
(a) Grid frequency scale (b) Switching frequency scale

Figure 3.3.3: Current waveforms for HF unipolar modulation

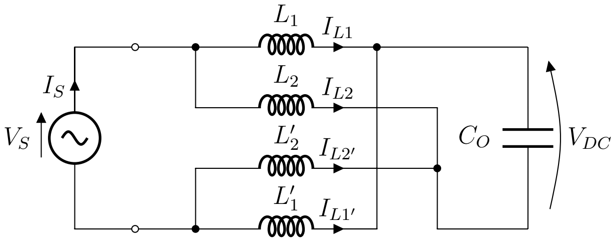
Hence, the common mode filter can also be reduced. This modulation presents clear advantages for integration. Trying to move forward the limit of passives reduction, the impact of interleaving was analysed. The interleaving is simply managed by phase shifting the carrier. With this topology the input inductor must be split to avoid short circuit between two legs, this can be illustrated by Figure 3.3.4.b); if there is only L1 and L2 the proposed configuration leads to a short-circuit of the DC link in the case of $Q2_1$ and $Q4_2$ are ON. Hence, L1' and L2' are mandatory.

PSIM simulations of the two interleaved bridges controlled with this modulation shows unbalanced inductor currents which induce more circulating current and unbalanced losses (see Figure 3.3.3). Circulating currents correspond to current flowing through the loop created by two inductors connected to different legs. These current are not useful for power transfer from the AC side to the DC side.

To obtain correct current waveforms the voltage across the two inductors of the same bridge must be similar. Moreover, the two interleaved bridges must not be impacted by commutation of the other bridge. Nevertheless, it appears that it is not the case with the present modulation. That is the reason of unbalanced currents. Hereafter, this behaviour is highlighted, Figure 3.3.4 presents an initial state, Figure 3.3.5 presents another configuration after a commutation of one leg of the second full bridge. For each configuration one equation is determined with the junction rule and three equations determined with the mesh law. The final analysis is made on the derivative of currents. In these examples, the inductor values are considered equals.



(a) Conducting devices



(b) Equivalent circuit

Figure 3.3.4: Switching configuration HF unipolar modulation t1.

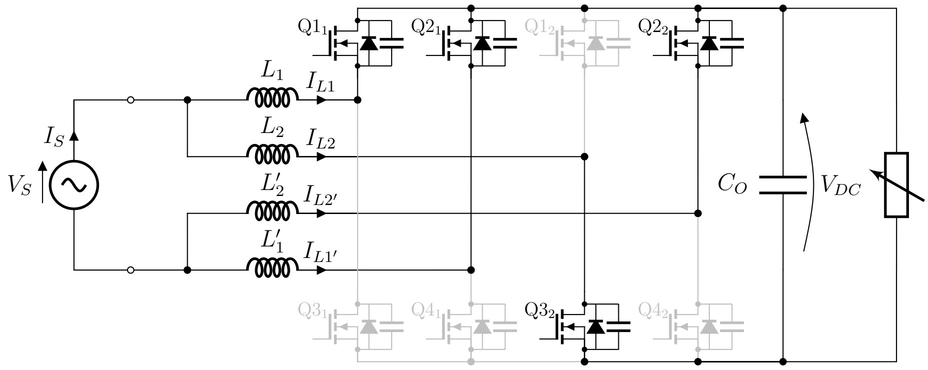
The following equations (from Equation (3.3.1) to Equation (3.3.4)) are related to the Figure (3.3.4).

$$I_s = I_{L1} + I_{L2} = -I'_{L1} - I'_{L2} \Rightarrow \dot{I}_{L1} + \dot{I}_{L2} + \dot{I}'_{L1} + \dot{I}'_{L2} = 0 \tag{3.3.1}$$

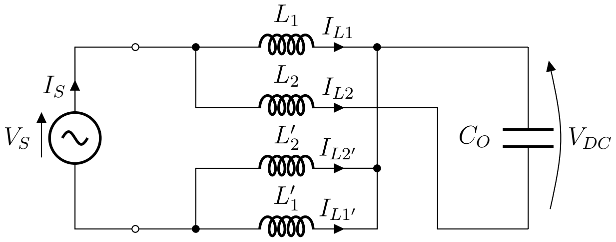
$$\dot{I}_{L1} - \dot{I}'_{L2} = \frac{1}{L} \cdot (Vs - V_{DC}) \tag{3.3.2}$$

$$\dot{I}_{L1} - \dot{I}'_{L1} = \frac{1}{L} \cdot Vs \tag{3.3.3}$$

$$\begin{pmatrix} \dot{I}_{L1} \\ \dot{I}_{L2} \\ \dot{I}'_{L1} \\ \dot{I}'_{L2} \end{pmatrix} = \begin{pmatrix} 1 & 2 & 0 & 1 \\ 1 & -2 & 4 & -3 \\ 1 & 2 & -4 & 1 \\ 1 & -2 & 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} 0 \\ Vs - V_{DC} \\ Vs \\ 0 \end{pmatrix} \cdot \frac{1}{4 \cdot L} \tag{3.3.4}$$



(a) Conducting devices



(b) Equivalent circuit

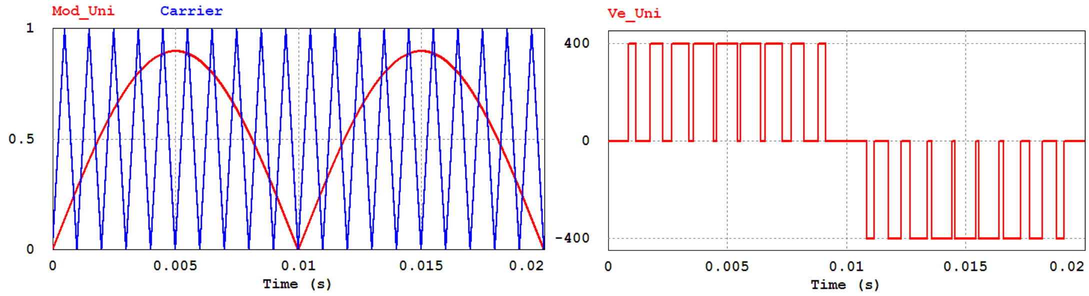
Figure 3.3.5: Switching configuration HF unipolar modulation t2.

It is possible to notice that bridge currents are different and the inductor current Ix' is not the opposite of Ix as initially expected, see Equation (3.3.4). However, the results for the second configuration (Figure (3.3.5)) show that one commutation of the second bridge will impact the current in the other bridge, see Equation (3.3.5).

$$\begin{pmatrix} \dot{I}_{L1} \\ \dot{I}_{L2} \\ \dot{I}'_{L2} \\ \dot{I}'_{L2} \end{pmatrix} = \begin{pmatrix} 1 & 2 & 1 & 1 \\ 1 & 2 & -3 & 1 \\ 1 & -2 & 1 & 1 \\ 1 & -2 & 1 & -3 \end{pmatrix} \cdot \begin{pmatrix} 0 \\ Vs \\ Vs \\ 0 \end{pmatrix} \cdot \frac{1}{4 \cdot L} \tag{3.3.5}$$

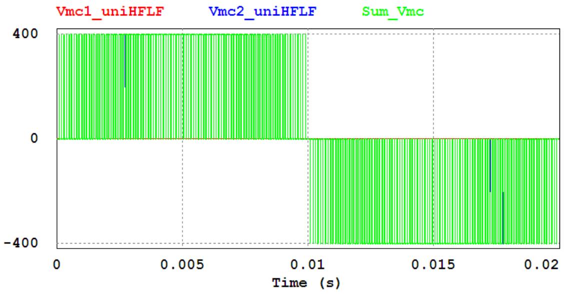
This example clearly shows that one commutation in the second bridge impacts the currents in the first bridge. These differences for associated inductors (L2 & L2') cause control issues and circulating currents which create losses. To avoid those phenomena the HF-LF unipolar modulation with only two inductors is presented in the following section.

3.3.1.3 LF + HF PWM unipolar modulation



(a) Modulation & carrier

(b) Input voltage waveforms

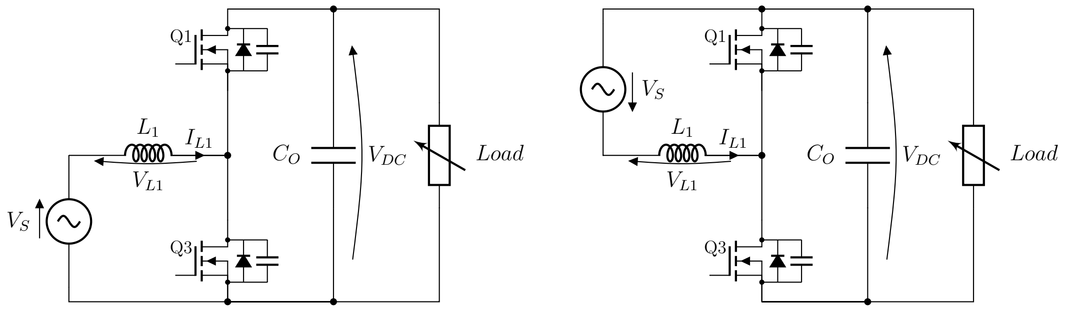


(c) Common Mode voltage

Figure 3.3.6: HF-LF unipolar modulation

This modulation is also a three level modulation. With this principle, a full bridge is composed of high frequency (HF) and low frequency (LF) legs. The LF leg operates at the grid frequency, in this case 50Hz. Hence, the apparent frequency is not twice the switching frequency. The common mode behaviour with this modulation is worst than the previous two. Indeed, there is no compensation between the legs, thus the common mode voltage varies at the switching frequency (see Figure 3.3.6).

With this type of control, the input inductor is two times smaller than the bipolar modulation and two times higher than the HF unipolar modulation. To evaluate if the interleaving can be implemented without risking too important unbalance and/or circulating currents, the same approach as previously presented is used hereafter. It is possible to distinguish two equivalent circuits according to the sign of the grid voltage, see Figure 3.3.7. Equations are also derived from the two configurations to analyse the impact of commutation on inductor currents.



(a) Equivalent circuit for Vs > 0 (b) Equivalent circuit for Vs < 0

Figure 3.3.7: PFC full-bridge topology.

Equations (3.3.6) & (3.3.7) correspond to the first configuration (see Figure 3.3.8) and Equations (3.3.8) & (3.3.9) correspond to the second configuration (see Figure 3.3.9).

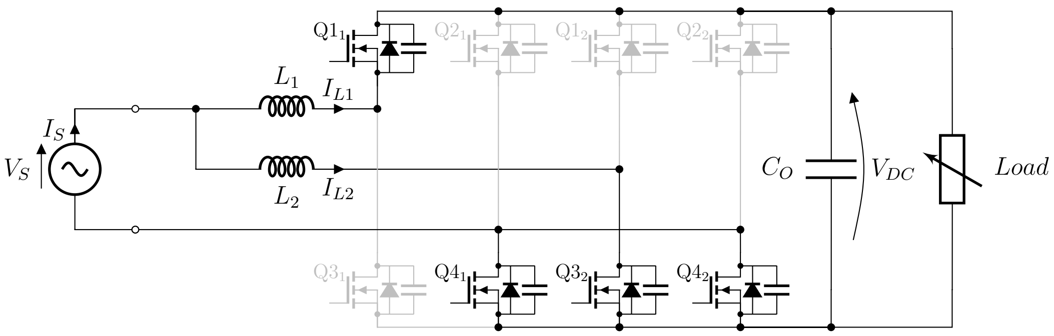
$$I\dot{L}1 = \frac{1}{L} \cdot (Vs - V_{DC}) \tag{3.3.6}$$

$$I\dot{L}2 = \frac{1}{L} \cdot Vs \tag{3.3.7}$$

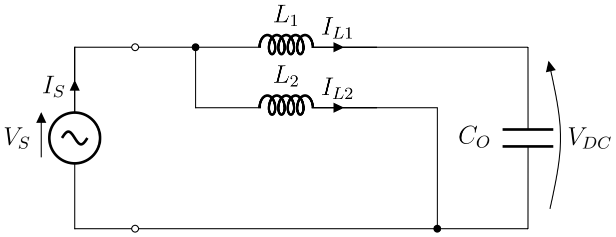
$$I\dot{L}1 = \frac{1}{L} \cdot (Vs - V_{DC}) \tag{3.3.8}$$

$$I\dot{L}2 = \frac{1}{L} \cdot (Vs - V_{DC}) \tag{3.3.9}$$

It is possible to notice with previous equations for the two switching configurations that there is no undesired impact of commutations on the different current. As an increase in the losses impacts the cooling system by reducing the power density, the reduction of circulating current is important. Then, even if the input inductor is higher than the HF unipolar modulation, the present modulation is preferred. The following only considers this modulation. The optimisation procedure is implemented according to this control scheme.

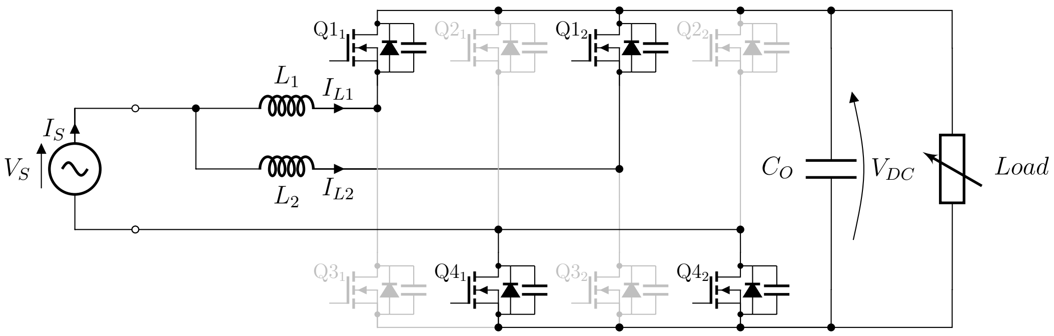


(a) Conducting devices

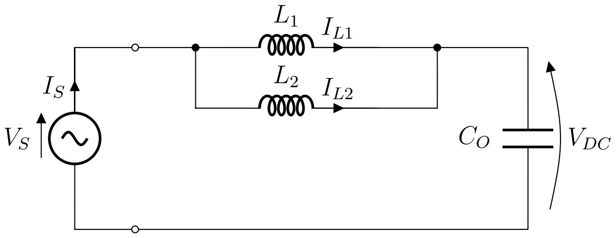


(b) Equivalent circuit

Figure 3.3.8: Switching configuration LF + HF unipolar modulation t1.



(a) Conducting devices



(b) Equivalent circuit

Figure 3.3.9: Switching configuration LF + HF unipolar modulation t2.

3.3.2 Conduction modes

The design of an optimal converter is largely influenced by the modulation and the conduction mode as losses and volume of passives are directly impacted. Two conduction modes are studied in this work. The first one corresponds to the Continuous Current mode (CCM) obtained with the LF +HF PWM. The second one is the Triangular Current Mode (TCM). The latter recently gained interest after the Google little Box challenge [37]. Both modulations are presented in details hereafter. In both cases, the average input inductor current is controlled to be sinusoidal.

3.3.2.1 Continuous current mode

CCM operates at fixed switching frequency (f_{SW}) with variable duty cycle. The maximal HF interleaved current ripple (ΔI) is the same whatever the load. According to the inductor value and the waveforms presented in section 3.3.1.3, it is possible to design the input inductor (size of core, magnetic material, number of turns, section of wire...). The value depends on the DC Bus voltage (V_{DC}), the switching frequency, the input current ripple and the number of interleaved cells (N). The maximal current ripple is obtained for a duty cycle $\alpha = 0.5$. Hence the input inductor value can be determined by Equation (3.3.10).

$$L_{PFC_{CCM}} = \frac{V_{DC}}{4 \cdot N \cdot f_{SW} \cdot \Delta I} \tag{3.3.10}$$

The typical waveforms of this type of conduction are illustrated in Figure 3.3.10. Commonly, the conduction losses generated by the HF components are relatively low due to the small current ripple. However, a drawback of this type of control is the switching losses, a part of commutation corresponds to hard switching (more details about this are presented in the sub-section 3.5.1). Moreover, the lower the input current ripple, the lower the DM filter, but the higher the input inductor. In contrast, increase the switching frequency positively impacts the size of the input inductor and the EMI filter [38].

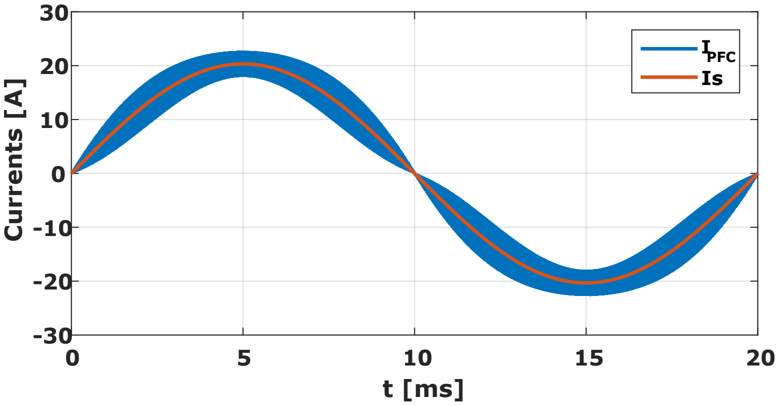


Figure 3.3.10: Current waveforms for CCM

Therefore, there is a trade-off between the size of the input inductor and the required DM filter. It is shown below that this trade-off can be easily managed thanks to interleaving.

3.3.2.2 Triangular current mode

Contrary to CCM, TCM operates at variable switching frequency [77]. Hence, the control implementation is more complicated. TCM is an extension of the discontinuous current mode (DCM); TCM allows inductor current to change its sign during each commutation and reach the defined reverse current (I_R). This reverse current is defined as the minimal current value required to achieve zero voltage switching. Indeed, the energy stored in the input inductor needs to be enough to charge and discharge the output capacitor of MOSFETs. Hence, this conduction mode is mainly used to drastically decrease the switching losses. Figure 3.3.11 represents typical current waveforms for TCM modulation at nominal power.

Some design elements are specific to TCM, such as dependency of inductor value on the maximal switching frequency (fsw_{MAX}) and the minimal power (P_{min}). The switching frequency depends on the grid voltage and the load, increasing for lighter loads and lower voltages. The maximal switching frequency must be limited and this constraint principally impacts the cell inductor value [78]. This modulation presents a higher RMS current than CCM, leading to higher conduction losses in semiconductors and passives (in particular without interleaving) e.g. input

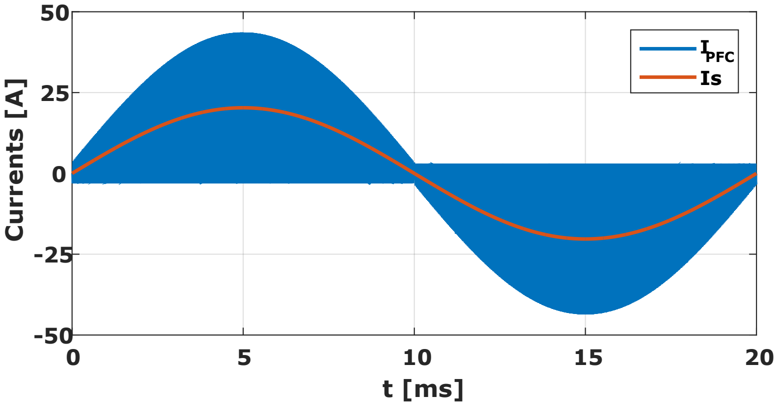


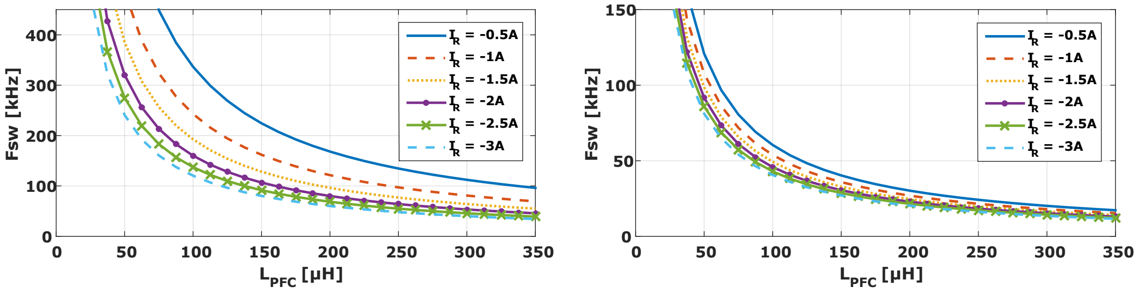
Figure 3.3.11: Current waveforms for TCM

inductor and DM filter inductors. To limit the switching frequency upper bound, we considered a minimum power equal to 10% of the nominal load (330 W). The corresponding inductor value can be calculated with Equation (3.3.11). However, the inductor design must be done for full load operation to support the higher current (cf appendix B.1).

$$L_{PFC_{TCM}} = max\left[\frac{\hat{V_S^2}\cos(2\omega t) + 2\cdot\hat{V_S}\cdot V_{DC}\sin(\omega t) - \hat{V_S^2}}{4\cdot f_{SW_{MAX}}\cdot V_{DC}\left(\frac{2\cdot Pmin}{\hat{V_S}}\sin(\omega t) + I_R\right)}\right] \tag{3.3.11}$$

Figure 3.3.12 presents the evolution of the maximum switching frequency as a function of the input inductor, reverse current and load. For the same value of L_{PFC}, the highest switching frequency at 3.3 kW is much lower than the highest switching frequency at 330 W. The method presented in [78] allows the gap between the two frequencies (maximal & minimal) to be reduced by adding a clamp circuit across the input inductor. The method can be interesting for low power converters, but is not adopted here.

Figure 3.3.13 illustrates the typical variation of the switching frequency for the TCM along the half grid period. The evolution is the same for the positive or negative half period.



(a) 10% of the rated power (330 W)

(b) Rated power (3.3 kW)

Figure 3.3.12: Evaluation of the maximum switching frequency according to the maximum reverse current.

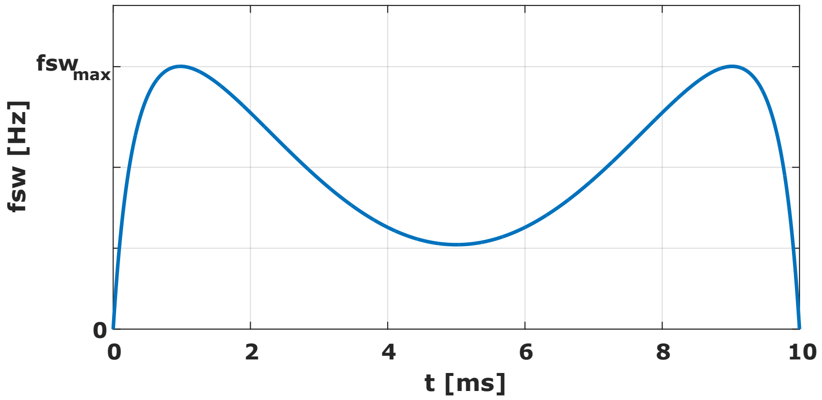


Figure 3.3.13: Switching frequency evolution for the TCM

3.4 Analytical waveforms generation

An important task to implement an optimisation procedure is the calculation of the different waveforms. Those waveforms are important to design the converter and estimate losses. The waveforms depend on the topology and on the modulation. The following presents the methodology used to obtain waveforms according to the two conduction modes previously introduced.

3.4.1 Waveforms generation for CCM

The objective of the design procedure is to ensure the compliance with harmonic standards by shaping the grid current according to the grid voltage. The average

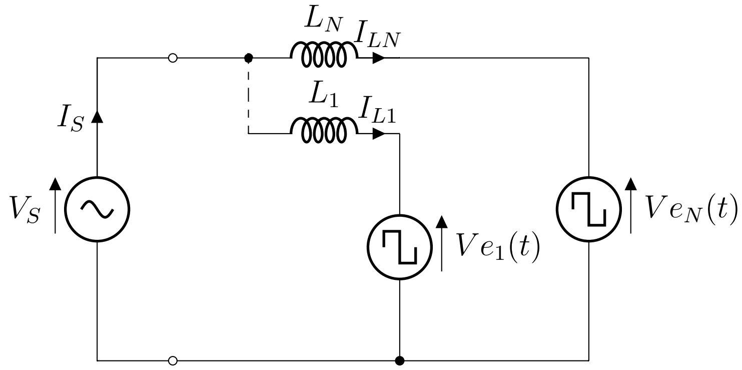


Figure 3.4.1: Note that $L_{1...N}$=L_{PFC} from Equation 3.3.10

value of the input voltage (Ve(t), see Figure 3.2.1) during one switching period of the converter is controlled to fulfill this objective. Hence the converter can be modelled by Figure 3.4.1 and Ve(t) can be expressed by Equation 3.4.1. According to the Kirchhoff's voltage law, it is possible to find the expression of the duty-cycle, assuming that the input current is sinusoidal and in phase with Vs(t), see Equation (3.4.2).

$$Ve(t) = \alpha(t) \cdot V_{DC} \tag{3.4.1}$$

$$\alpha(t) = \left| \frac{\hat{Vs}}{V_{DC}} \cdot \sin(\omega t) - \frac{L_{PFC} \cdot \omega \cdot \hat{Is}}{N \cdot V_{DC}} \cdot \cos(\omega t) \right| \tag{3.4.2}$$

The duty cycle is then compared to the carrier signal (see Figure 3.3.6.(a)) to determine the state for each devices. As it is possible to notice, the modulation depends on the interleaving, which is represented by the term "N". The carrier used for the comparison is shifted (φ_{car}) according to the switching period (Tsw) and the number of parallel cells (see Equation (3.4.3)).

$$\varphi_{car} = \frac{Tsw}{N} \tag{3.4.3}$$

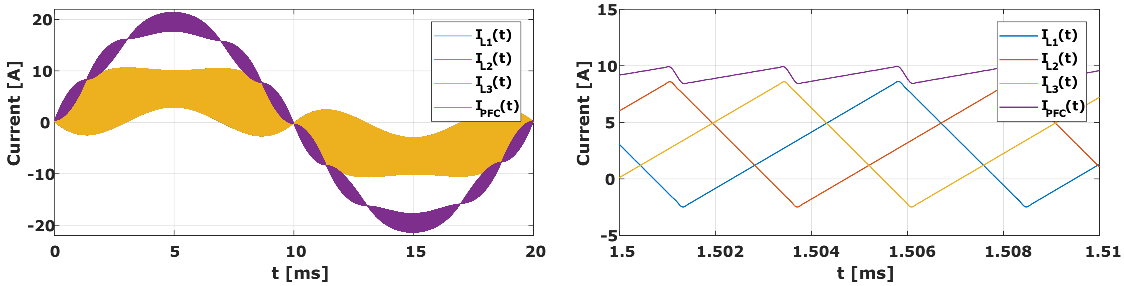
With all voltage waveforms of the switches during a grid period, the bridge input voltage is calculated, then the inductor current can be easily determined in the frequency domain using the Fast Fourier Transform (FFT). Each Harmonics of the inductor voltage is divided by the inductor impedance at the corresponding frequency to obtain the current, then the inverse FFT is applied to get the current in the time domain, as it is explained by following equations.

$$V_L(t) = Vs(t) - Ve(t) \tag{3.4.4}$$

$$I_L(\omega) = \frac{FFT(V_L(t))}{Z_L(\omega)} \tag{3.4.5}$$

$$I_L(t) = FFT^{-1}(I_L(\omega)) \tag{3.4.6}$$

This methodology has the benefit to determine all the waveforms, analytically, and realise the optimisation in the same software (Matlab). Simulation with additional software like PSIM or Simplorer is not mandatory. Indeed, the overall design time and complexity of the optimisation is reduced. Knowing the important waveforms such as, switch currents and voltages and inductor currents, the passives are designed and the losses are calculated. More details are provided on the determination of switch current and calculation of losses in sub-section 3.5.1. The typical interleaved current waveforms are presented in Figure 3.4.2.



(a) Currents at the grid frequency

(b) Currents at the switching frequency

Figure 3.4.2: CCM Current Waveforms for three interleaved cells

3.4.2 Waveforms generation for TCM

Concerning the TCM, generation of waveforms is more tricky than for CCM. Indeed, as the TCM is a variable switching frequency control, the interleaving management is more complicated because the switching period is not the same along the grid period (Ts). Once the current in one cell is calculated, the different commutation times are used to calculate the switching period to obtain the most suitable phase shift between the inductor currents, according to the number of cells [77]. The method to determine the inductor current is different than previously. This method corresponds to an hysteresis detection. The inductor current is defined by three values : the average current which corresponds to the 50 Hz current ($IL_{\bar{TCM}}(t)$), the peak current ($IL_{\hat{TCM}}(t)$) corresponding to the HF current ripple which is moving along the grid period and the maximal reverse current (see Figure 3.4.3). The peak current is calculated according to the average current, which depends on the desired input power, and the value of the reverse current, which is an optimisation variable, as it is presented in Equation 3.4.7.

$$IL_{\hat{TCM}}(t) = 2 \cdot IL_{\bar{TCM}}(t) + I_R \tag{3.4.7}$$

The HF current slope depends on the input inductor value, Equation 3.3.11, and the voltage across the inductor. Each time the current is equal or superior to one of the boundary, it is corresponding to a commutation.

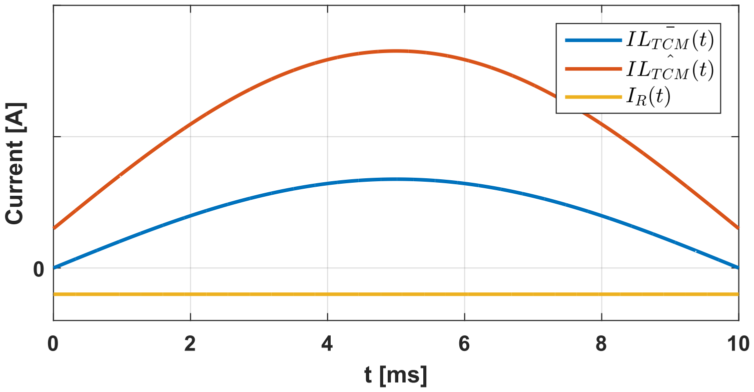
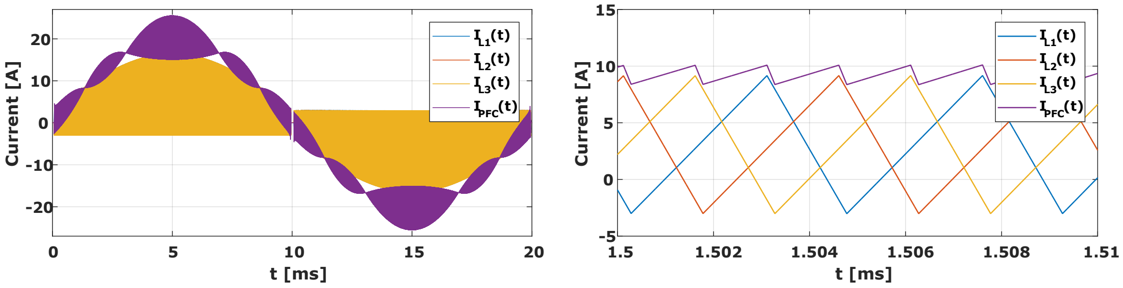


Figure 3.4.3: TCM current boundaries



(a) Current waveforms at the grid frequency (b) Current at the switching frequency

Figure 3.4.4: TCM current waveforms for three interleaved cells

Indeed, the voltage waveforms depends on the inductor value and are determined iteratively, thus taking more computing time. Since the inductor currents and switch voltages are known, the losses can be calculated. Figure 3.4.4 presents current waveforms obtained with the methodology, including interleaving.

3.5 Global converter optimisation framework

Now, both modulations and topology are introduced, this part discusses about the global methodology to design the converter. The objective of this procedure is to estimate the overall volume and losses of converters in the way to define the trade-off between efficiency (η) and power density (ρ). These criteria were selected because of the integration objective. However, this methodology could be adapted to design with different constraints, such as cost or mass. The design procedure is presented in Figure 3.5.1 for both modulations. The flowchart is composed of three main parts : "Semiconductors", "EMI filter" and "Inductor Design". For both modulation schemes, it is possible to act on several variables which are presented in Table 3.2.

First of all, important waveforms are determined analytically for a set of variables depending on the modulation as presented previously. Concerning the CCM, the switching frequency and the current ripple are used. The two system variables for the TCM are the switching frequency upper bound ($f_{SW_{MAX}}$) and the maximal allowed reverse current. The range of variation of each variable is presented in Table 3.3. These parameter ranges were defined after preliminary optimisation.

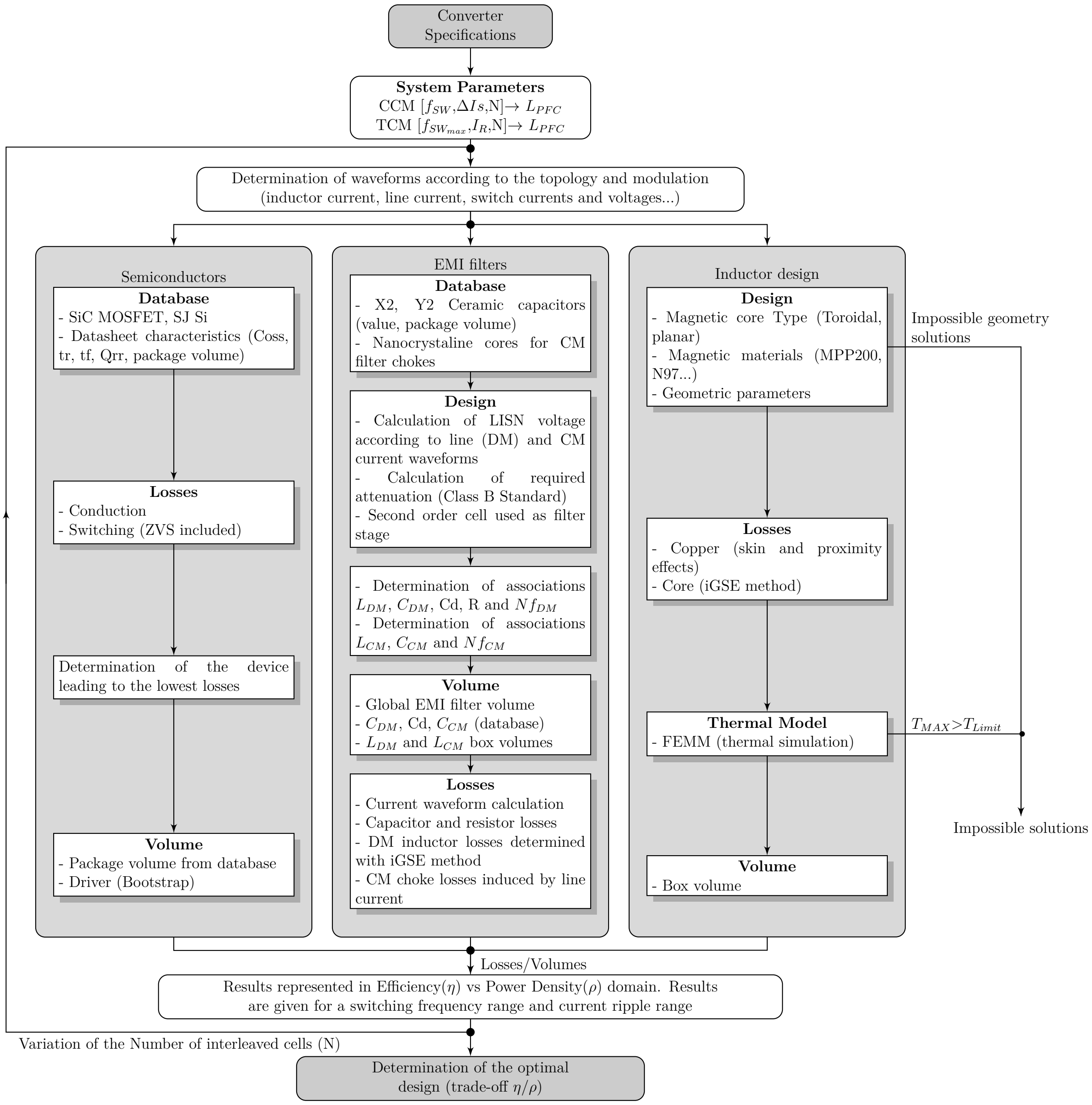


Figure 3.5.1: Flowchart of the global method used for the converter design

Table 3.2: Optimisation variables

	CCM	TCM
Variables	Switching frequency fsw [kHz] Input current ripple ΔIs [A]	Maximal switching frequency $\mathrm{fsw_{MAX}}$ [kHz] Maximal reverse current $\mathrm{I_R}$ [A]
	Number of interleaved Cells N	Number of interleaved Cells N
	Maximal number of DM filter stages $\mathrm{Nf_{DM}}$	Maximal number of DM filter stages $\mathrm{Nf_{DM}}$
	Maximal number of CM filter stages $\mathrm{Nf_{CM}}$	Maximal number of CM filter stages $\mathrm{Nf_{CM}}$

Table 3.3: Optimisation variables range

CCM	TCM
fsw = [140 kHz ; 300 kHz]	$\mathrm{fsw_{MAX}}$ = [350 kHz ; 650 kHz]
ΔIs = [2 A ; 12 A]	$\mathrm{I_R}$ = [1 A ; 3 A]

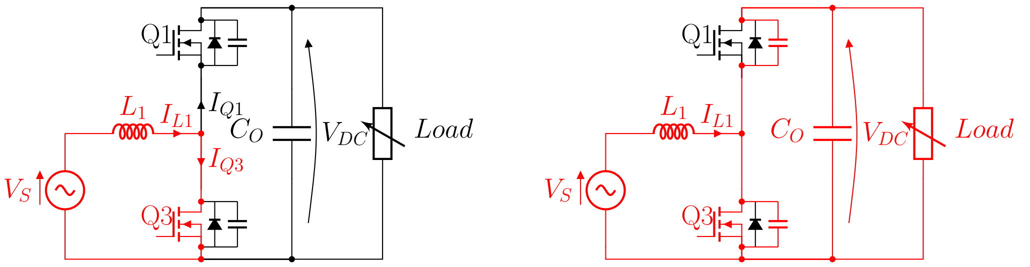
For TCM the maximal switching frequency is relatively close to the limit of SiC devices but this mode corresponds to light load operation, the switching frequency at nominal power is lower. The maximal reverse current is settled in order to limit the conduction losses. Inductor currents, grid current, device voltages and currents are used in the three different sub-parts : identification of the semiconductor which leads to the lowest losses, optimisation of the passives and design of the EMI filter.

The inductor optimisation is realised according to the selected geometry, Planar or Embedded Toroidal, inductor value and inductor current. Multiple geometries are created, losses are then calculated to eliminate thermally impossible solutions. More details on inductor geometries and losses calculations are presented in the sub-section 3.5.2

The sub-part on EMI filter design considers multistage filters, the number of stages being an additional optimisation variable. The outputs of each parts are losses and volume which are used to select the final converter. At the end of the procedure, the impact of the thermal management on the global power density is added. Natural convection is assumed in this work. A preliminary study was carried out according to specifications to determine the volume of the heat sink as a function of global losses. It was found a thermal coefficient of $5\,\mathrm{cm}^3/\mathrm{W}$ is a pertinent value according to the specifications : ambient temperature of 60°C, and the maximum devices temperature of 125°C. The final choice is made among several possible combinations between boost inductor and input filter.

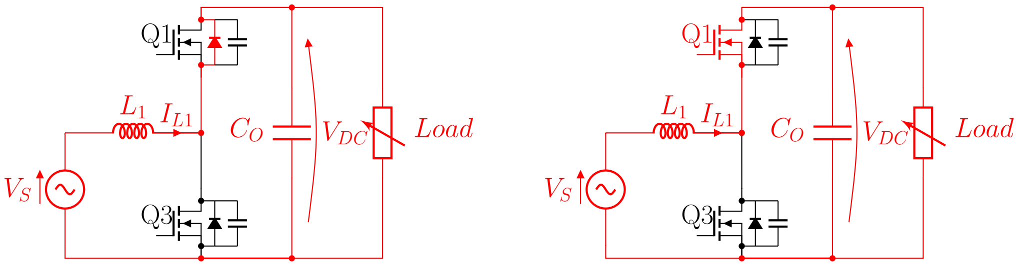
3.5.1 Semiconductors selection based on losses with ZVS recognition

The selection of suitable dies is made according to a database which is composed of 900V and 1200V SiC and Super Junction Si (SJ Si) MOSFETs. Device volume estimation includes switch packages and driver volume (bootstrap type). The estimated volume for the gate driver is equal to $0.5\,\mathrm{cm}^3$, the reference of the implemented chip is the IRS21864S. This reference was selected due to its high output current capabilities (4 A). For the integrated version the bare dies volume is considered, even if it is almost negligible compared to the gate driver. The final volume is determined after the selection of the device which results in the lowest sum of conduction and switching losses among devices included in the database. The motivation is the reduction of the impact of the cooling system on the global volume. All semiconductor parameters used to calculate losses come from datasheet. Regarding conduction losses, the on-state resistance at 150°C is considered, thus avoiding certain under-estimation of losses with the 25°C value. Even with WBG devices switching losses may represent a large part of losses at high switching frequency. A simple and fast model using datasheet parameters has been developed to quickly compare the different devices to each other. This model includes : commutation times (rise time tr, fall time tf), output capacitor (Coss) and the body diode's reverse recovery charge (Qrr). It is important to note that reverse recovery charge can generate high losses, in particular if SiC Schottky diodes are not used in parallel of MOSFETs. Synchronous rectification is assumed to limit the impact of the body diode [79]. Nevertheless, the selected topology can achieve soft-switching, zero voltage switching (ZVS), that drastically reduce the turn-ON losses. The Figures 3.5.2, 3.5.3 and 3.5.4 present the switching sequence of one HF leg. The two types of commutation (Hard and soft) are explained in details, including each conducting elements.



(a) Initial configuration Q3 ON and Q1 OFF, $\mathrm{I_{L1}}$is positive and rises

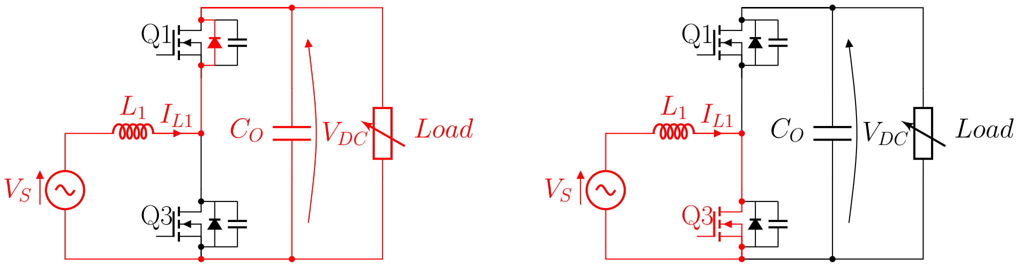
(b) Q3 turns OFF, charging and discharging Coss capacitors of Q3 and Q1 respectively.



(c) Bodydiode of Q1 starts to conduct.

(d) Q1 turns ON in ZVS.

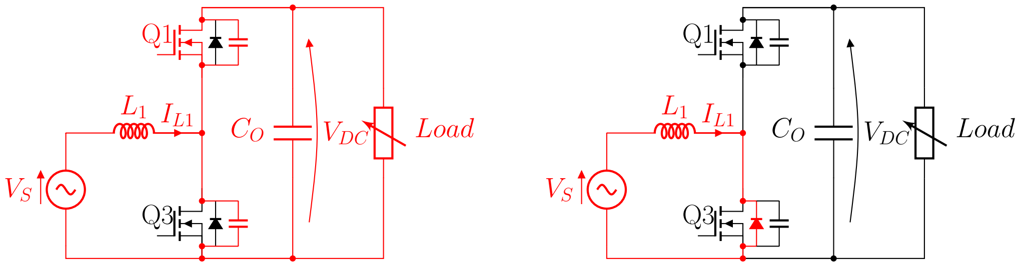
Figure 3.5.2: Switching sequences which are common to both cases: Q1 turns ON for $\mathrm{I_{L1}}$>0.



(a) Q1 turns OFF, the bodydiode starts to conduct.

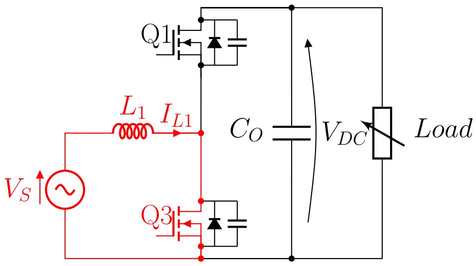
(b) Q3 turns ON, Coss capacitor is not discharged before commutation, this correspond to hard switching which involves recovery of Q1's bodydiode. Back into initial configuration.

Figure 3.5.3: Switching sequence when inductor current remains positive: Q3 turns ON for $\mathrm{I_{L1}}$>0.



(a) Q1 turns OFF, charging and discharging Coss capacitors of Q1 and Q3 respectively.

(b) Bodydiode of Q3 starts to conduct



(c) Q3 turns ON in ZVS

Figure 3.5.4: Switching sequence when inductor current changes its sign during the switching period: Q3 turns ON for $I_{L1}<0$.

Due to the AC/DC behaviour of the converter, the current switched by semiconductors is not constant. Therefore it is important to know the current at the switching time for each semiconductor to identify hard and soft commutations. In the Matlab program, the state of each device is represented by logical vector (1 → ON, 0 → OFF). Hence, it is easy to determine turning ON and OFF times with simple vector operations. The current in each device is determined with Equation 3.5.1.

$$ITx(t) = \begin{cases} IL(t) & for\, S_{Tx} = 1 \\ 0 & for\, S_{Tx} = 0 \end{cases} \tag{3.5.1}$$

for example

$$S_{Tx} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 \end{bmatrix}$$

and

$$\bar{S}_{Tx} = \begin{bmatrix} 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

It is possible to obtain two vectors applying a right and left shifting on $\bar{S}_{Tx}$, noted V_R and V_L respectively

$$V_R = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \end{bmatrix}$$

and

$$V_L = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix}$$

Now adding $\bar{S}_{Tx}$with V_R and V_L in a specific order allows to determine switching instant for turn ON and turn OFF separately. The unused values, different than 1 or 0 are indicated as “x”.

$$Sw_{ON} = V_R - \bar{S}_{Tx} - V_L = \begin{bmatrix} x & x & x & 0 & 1 & 0 & 0 & x & x & x & x & 0 & 1 & 0 & 0 & x & x \end{bmatrix}$$

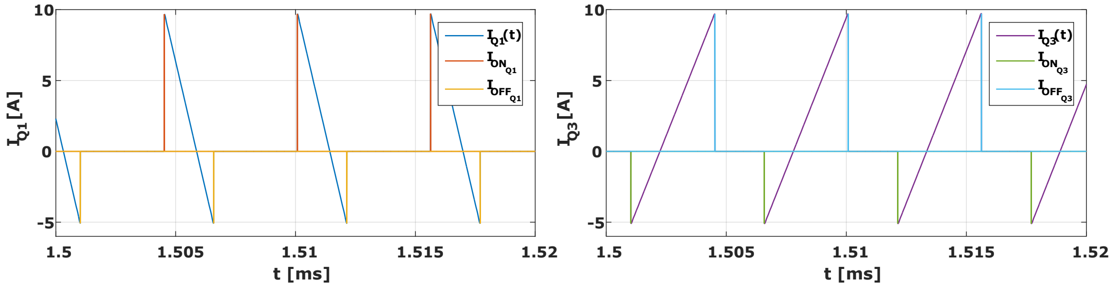
$$Sw_{OFF} = V_L - \bar{S}_{Tx} - V_R = \begin{bmatrix} x & x & x & x & x & 0 & 0 & 1 & 0 & x & x & x & x & 0 & 0 & 1 & 0 \end{bmatrix}$$

hence it is possible to determine the value of the switched current by multiplying the current $ITx(t)$ by Sw_{ON} or Sw_{OFF} (see Equations (3.5.2) and (3.5.3))

$$ITx_{ON}(t) = ITx(t) \cdot Sw_{ON} \tag{3.5.2}$$

$$ITx_{OFF}(t) = ITx(t) \cdot Sw_{OFF} \tag{3.5.3}$$

Figure 3.5.5 represents switch currents for one HF leg and their corresponding turn ON and turn OFF currents that are used to calculate switching losses. It is



(a) IQ1(t) (b) IQ3(t)

Figure 3.5.5: Switch currents with the corresponding $\mathrm{ITx_{ON}(t)}$ and $\mathrm{ITx_{OFF}(t)}$.

considered that losses generated by each full bridge (HF leg + LF leg) are equal, so losses are determined for one bridge then multiplied by the number of interleaved cells to obtain the total semiconductor losses.

In the case of hard switching, the energies ($\mathrm{Esw_{ON}}$ and $\mathrm{Esw_{OFF}}$) are calculated with Equations 3.5.5 and 3.5.6 which are derived from the Figure 3.5.6, representing simplified commutation waveforms where $\mathrm{I_{Dx}}$ represents the switched current, determined as aforementioned. The turn-ON losses are impacted by three different parameters, as it is noticeable in Equation 3.5.5. The first term corresponds to the losses in the channel which depends on the voltage across the device and the current flowing through it. The second term corresponds to the discharge of the output capacitor, as the initial state of the device is OFF, the DC voltage is applied to the parasitic output capacitor. Indeed, this stored energy needs to be transferred. Usually this energy is dissipated in the channel leading to additional losses. The last term is the reverse recovery charge. As the two devices are not perfectly synchronised due to dead time, the body diode of the second device starts to conduct. At the time of the turn-ON of the other switch, the body diode needs to be discharged and also induce additional losses. Concerning the turn-OFF losses, only losses generated in the channel are included. Then, the total switching losses ($\mathrm{P_{SW}}$) for complete grid period, for one device, are calculated with Equation 3.5.7, with fs is the grid frequency. In the case of soft-switching the turn-ON commutation is considered as lossless, the turn-OFF losses are still calculated with the Equation 3.5.6. The conduction losses for one switch, are determined with Equation 3.5.4 independently of soft or hard switching.

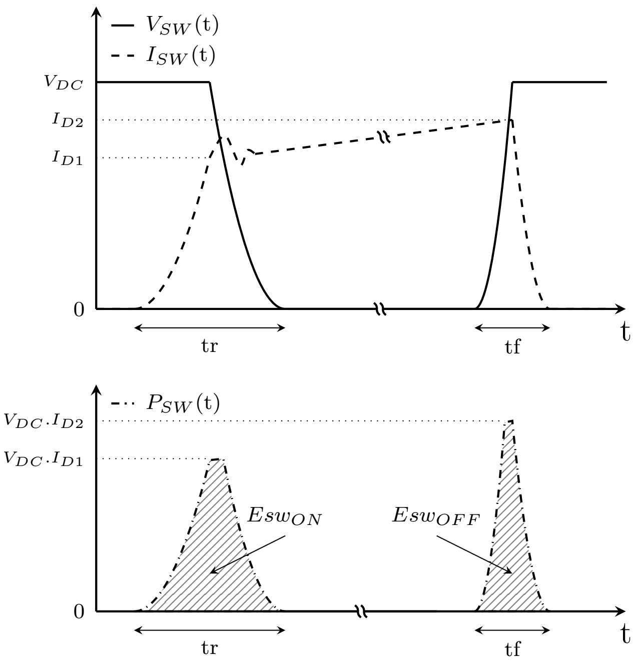


Figure 3.5.6: Simplified commutation waveforms.

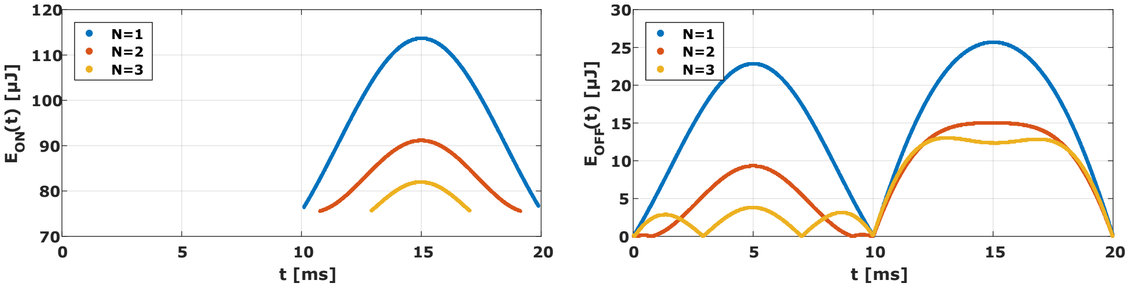
$$P_{Cond.} = R_{DSon}(150°C) \cdot I^2_{Qx,rms} \tag{3.5.4}$$

$$Esw_{ONx} = \frac{1}{2} \cdot V_{DC} \cdot I_{Dx} \cdot tr + \frac{1}{2} \cdot Coss \cdot V^2_{DC} + Qrr \cdot V_{DC} \tag{3.5.5}$$

$$Esw_{OFFx} = \frac{1}{2} \cdot V_{DC} \cdot I_{Dx} \cdot tf \tag{3.5.6}$$

$$P_{SWx} = (\sum Esw_{ONx} + \sum Esw_{OFFx}) \cdot fs \tag{3.5.7}$$

As it is explained previously, it is important to identify the commutation instants to estimate switching losses, which are more difficult to obtain than conduction losses due to inherent soft commutations. During half of the grid period, one of the HF switches achieves zero voltage switching, the second one operates in hard switching if the inductor current doest not changes its sign (Figures 3.5.2 and 3.5.3). The second switch can also achieve ZVS if the inductor current changes



(a) $\mathrm{Esw}_{\mathrm{ON}}(\mathrm{t})$ for Q1 (b) $\mathrm{Esw}_{\mathrm{OFF}}(\mathrm{t})$ for Q1

Figure 3.5.7: Switching energies for one device according to the number of interleaved cells with fsw = 180 kHz, ΔI = 4A and C3M0065090J devices

its sign before the commutation (Figures 3.5.2 and 3.5.4) which is typically the case with the TCM. Therefore all HF switches operates in soft switching for the complete grid period in TCM, which is the main advantage of this control. Figure 3.5.7 illustrates the impact of the sign of the inductor current. Indeed, with increasing number of interleaved cells and at constant ΔI, the inductor current ripple increases. Zero crossing events of the inductor current occur more frequently. Hence, the switch can turn ON in ZVS, Eon losses (Equations 3.5.5) are cancelled, as explained above. The Eoff losses (Equation 3.5.6) are also reduced because of the current sharing between the cells.

3.5.2 Design and models of inductors with different level of integration

The design of the inductors, e.g., boost inductor or input filter inductor, is a key point in the design. This sub-part of the design procedure requires the inductor value and the current waveforms to design the inductor. The inductance is determined according to the modulation. The Equations (3.3.10) and (3.3.11) are used for CCM and TCM, respectively. It is important to notice that for TCM the inductor value is impacted by the minimal load which corresponds to the highest switching frequency. Consequently the inductor value is calculated to limit the maximal switching frequency.

(a) Planar (b) Embedded toroidal

Figure 3.5.8: Inductor technologies

For the PFC, two geometries of inductor are studied, the classic planar inductor and the embedded toroidal inductor [80](see Figure 3.5.8). The toroidal PCB inductor presents a highest level of integration than the planar. Global inductor losses are composed of copper losses and core losses. Copper losses are generated by the current flowing through the PCB traces and are influenced by skin and proximity effects. The current is composed of low and high frequency harmonics. The resistance seen by each harmonic is different due to these effects. The resistance seen by low frequency harmonics is represented by the DC resistance ($\mathrm{R_{DC}}$), the equivalent AC resistance ($\mathrm{R_{AC}}$) at the fundamental of the switching frequency is determined with 3D FEM simulations. One design was simulated to obtain the ratio between DC and AC resistances. This ratio is then used in the procedure to avoid long computation times. Copper losses are calculated with the two components of the current and the corresponding resistance. The RMS value of the 50 Hz component and the HF current ripple are calculated, then copper losses are determined (see Equation 3.5.8).

$$P_{CU} = R_{DC} \cdot (I^2_{LF_{RMS}} + \frac{R_{AC}}{R_{DC}} \cdot I^2_{HF_{RMS}}) \tag{3.5.8}$$

For core losses, the improved generalised Steinmetz equation (iGSE) method is used [81]. This method decomposes the inductor current in major and minor loops. Major loops correspond to the induction created by the low frequency component (50 Hz) whereas the minor loops correspond to the induction generated by the high frequency components ($\mathrm{f_{SW}}$). Minor loops are moving along the main low

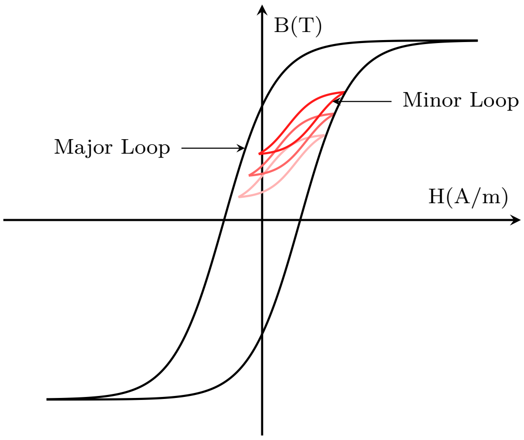


Figure 3.5.9: Typical hysteresis loop in PFC inductors.

frequency induction, hence additional losses are generated. Figure 3.5.9 presents major and minor loops and illustrates the phenomenon. More details about this method which uses the improved Generalised Steinmetz Equation (iGSE) (see Equations 3.5.9 and 3.5.10) and its implementation are presented in [80].

$$P_{vi} = \frac{1}{Ts} \int_0^T k_1 \cdot \left| \frac{dB}{dt} \right|^{\alpha} \cdot (\Delta B)^{\beta-\alpha} dt \tag{3.5.9}$$

where :

$$k_1 = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} \cdot 2^{\beta-\alpha} d\theta} \tag{3.5.10}$$

The Steinmetz coefficients correspond to k, α and β, B is the flux in the inductor and T is the period of the signal.

3.5.3 Multi-stage EMI filter design

The third part of the global design is EMI filter design. For the project, the design of EMI filter only includes conducted EMI (Differential Mode (DM) and Common Mode (CM)). Differential Mode corresponds to a current loop flowing through the two line conductors connected to an electronic system. Common Mode corresponds to a current flowing through the line conductors of the electronic system and the

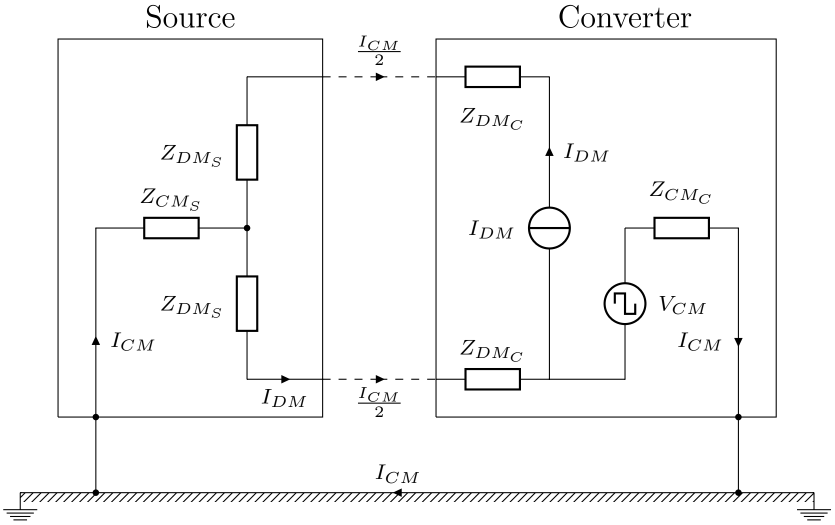


Figure 3.5.10: Conducted EMI principle.

earth connection. Schematics presented in Figure 3.5.10 illustrates conducted EMI principles. To simplify EMI filter design both types of perturbations are studied separately.

3.5.3.1 Differential Mode filter

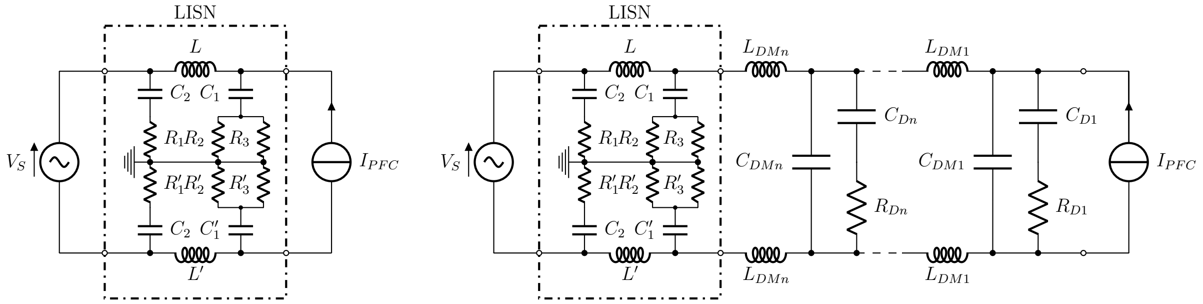
Firstly, DM filter is designed. Equivalent schematic including Line Impedance Stabilisation Network (LISN), input voltage source and PFC current is used to determine the required attenuation. Multistage LC filters are studied, it was demonstrated in [82] that multistage filter composed of identical cells induces minimal volume. Despite, this configuration presents large differences in the capacitive current density (A/µF) of each stages. The HF current flowing through the first stage (close to the converter) is higher than current flowing to last stage. To overcome this issue, only inductors are same and capacitor are different for each stage. Highest capacitance is placed close to the converter and lowest capacitance is placed at the grid side. The volume is slightly higher than filters composed of identical cells but with this principle the capacitive current density is reduced for the capacitance close to the switches.

First step in the DM filter design is calculation of required attenuation, using Kirchoff's law and superposition theorem, current and voltage in the LISN model can be determined. The needed inductor is then determined according to the attenuation, product of capacitor value and number of filter stages. Knowing current in each filter elements, calculation of losses and volume is possible. A database including package volume and serial resistance (ESR) is used for capacitors. The total capacitor value used in the filter is limited according to a minimal power factor, further details are presented hereafter. The previous mentioned method for PFC inductor is also used for filter inductors design. Different geometries can be selected based on required integration level.

Determination of the component values

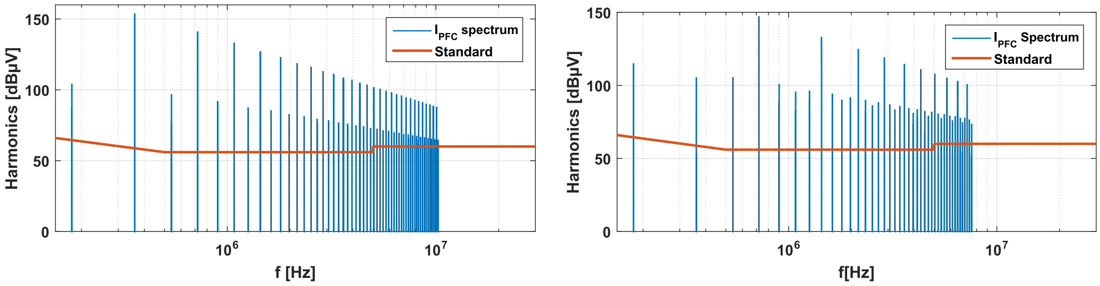
As it is aforementioned, multistage EMI filters are studied. The number of stages is a variable to define the optimal converter. Each stage is composed of a second order cell associated with R-C_d damping circuit in parallel.

The first step for DM filter design is the calculation of the required attenuation. Figure 3.5.11.(a) represents the equivalent model without DM filter and Figure 3.5.11.(b) illustrates the DM filter topology with the LISN. LISN model corresponds to a reference used for the EN55011 class B standard. All LISN voltages and currents can be determined with Kirchoff's laws and superposition theorem. FFT is used to obtain spectrum of the voltage across R3 (50Ω).



(a) Model with only LISN (b) Model with LISN and DM filter

Figure 3.5.11: Simplified model for DM filter design.



(a) N = 2, P = 330 W (b) N = 4, P = 3.3 kW

Figure 3.5.12: Comparison of line current spectrum fsw = 180 kHz, $\Delta I_{PFC} = 8A$.

The designed converter includes interleaving. The input current ripple is independent from the load. However reducing the number of interleaved cells increase this current ripple. An advantage of interleaving is high efficiency achievable at light load by disabling some cells. The negative impact of this, is the highest level of EMI perturbations. N = 2 corresponds to the minimal number of interleaved cells. Figure 3.5.12 highlights the fact that the most constraining mode corresponds to the lowest load with the minimal number of interleaved cells. The dimensioning harmonic corresponds to two times the switching frequency against four times with four interleaved cells. Hence, the DM filter is designed for worst case. The obtained spectrum is then compared with EN55011 class B average standard. The required attenuation and the dimensioning frequency are determined by Equation (3.5.11). A security margin of 6 dBµV is added to assure the compliance with the standard.

$$Att_{req} = max(FFT(V_{R3}) - Standard + Margin) \tag{3.5.11}$$

The second step corresponds to the determination of capacitors used in the filter.

Those values depends on the number of filter stages. Firstly global capacitance is calculated to achieve a certain power factor at 10% of the nominal load. At the grid frequency the impedance of DM inductor is small, hence it can be considered that all DM capacitors are connected in parallel. The power factor depends on the reactive power absorbed by filter capacitors when grid voltage is applied. This calculation also includes damping capacitors. The 10% of load corresponds to

P_{MIN}= 330W and the minimal authorised power factor is cos φ = 0.995, so the maximal reactive power is Q_{MAX}= 33VAr. The maximal global capacitor which can be implemented in the DM filter is calculated with Equation 3.5.12.

$$C_{MAX} = \frac{Q_{MAX}}{Vs_{RMS}^2 \cdot \omega s} \tag{3.5.12}$$

As it is mentioned above, damping capacitors are a part of the global capacitor, moreover the value of each capacitors are different for each filter stage. The largest capacitor is placed close to the converter and the smallest capacitor is placed at the grid side. The filtering capacitor and the damping capacitor are considered identical within each filter stage to reduce the bill of materials. The distribution of the capacitor values according to the number of filter stages is defined with the Equations 3.5.13 to 3.5.15. The factor "K" is calculated according to number of filter stage. The minimal capacitor, which corresponds to the capacitor at the grid side, is calculated. This value is then used as reference to determine the others without exceeding the global authorised capacitance.

$$K = \frac{1}{2} \cdot N_f \cdot (N_f + 1) \tag{3.5.13}$$

$$C_{DM_{N_f}} = C_{D_{N_f}} = \frac{C_{MAX}}{2K} \tag{3.5.14}$$

$$C_{DMi} = C_{Di} = i \cdot C_{DM_{N_f}} \Rightarrow i \in [1; N_f] \tag{3.5.15}$$

For known capacitor values, inductor values can be calculated according to the required attenuation, dimensioning frequency, which is presented with Equation 3.5.16. The sub-part of the flowchart "inductor design" is also used to design DM filter inductors according to the value and current waveforms.

$$L_{DM} = \frac{1}{2} \cdot \sqrt[N_f]{\frac{10^{\frac{Att_{req}}{20}}}{(2\pi f_D)^{2N_f} \cdot \prod C_{DM}}} \tag{3.5.16}$$

Middlebrook's theorem is used to determine damping resistors. The optimal damping resistor according to each filter stage elements, i.e. capacitor and inductor, can be determined with the methodology presented in [83]. The damping resistor value is calculated with Equation 3.5.17. "n" corresponds to the factor between filtering capacitor ($\mathrm{C_{DM}}$) and damping capacitor ($\mathrm{C_D}$), in this case $\mathrm{C_{DMi} = C_{Di}}$ so $\mathrm{n = 1}$.

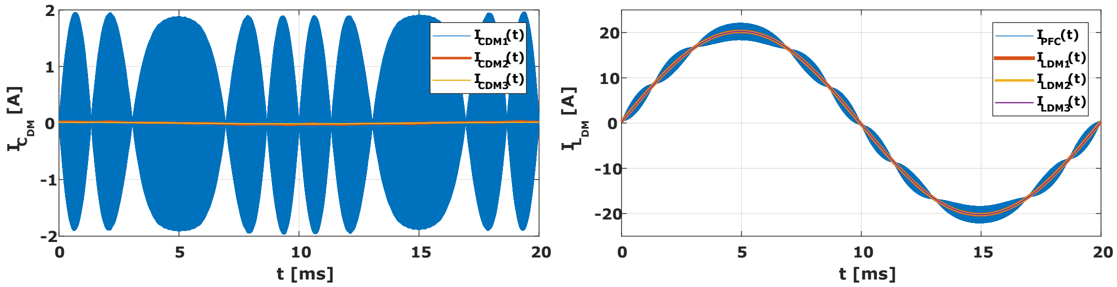
$$R_{Di} = \sqrt{\frac{2 \cdot L_{DM}}{C_{DMi}}} \cdot \sqrt{\frac{(2+n)(4+3n)}{2n^2(4+n)}} \tag{3.5.17}$$

For CCM modulation, the highest required attenuation is for harmonic at the switching frequency multiplied by the number of interleaved cells. A high switching frequency allows reducing the DM filter size, as boost inductor. As the worst case corresponds to two interleaved cells, the first high harmonic to attenuate is at $\mathrm{2.f_{SW}}$. The input filter design for the TCM needs a particular attention. As it is a variable switching frequency control, a main part of the harmonics can be out of the standard (frequency lower than 150 kHz). The Total Harmonic Distortion (THD) must be included in the DM filter design. This point is particularly important if no interleaving is used with the TCM modulation.

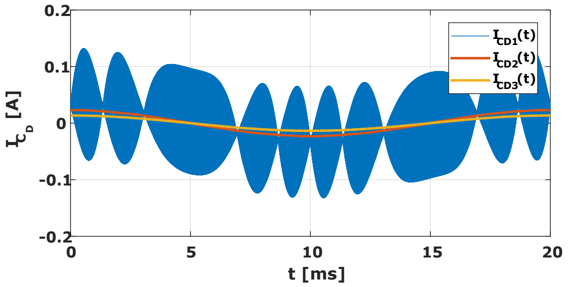
Losses calculation

For each combination of DM filter, which mainly depends on the number of stages and the inductor shape, the current in each components is calculated. These currents permit to determine the losses in the filter, which is important for the selection of the converter. Figure 3.5.13 presents typical current waveforms in a three stage EMI filter designed with the selected topology.

Losses in the filtering and damping capacitors are calculated according to the RMS current value and the equivalent series resistance (ESR). For this type of capacitor, the ESR depends on the frequency. From 100 kHz to 10 MHz, the resistance is decreasing. Hence, to avoid any underestimation of losses, the value at 100 kHz is picked in the datasheet. This value is consistent with the current flowing through the capacitor, as this current is mainly composed of switching



(a) DM capacitors (b) DM inductors



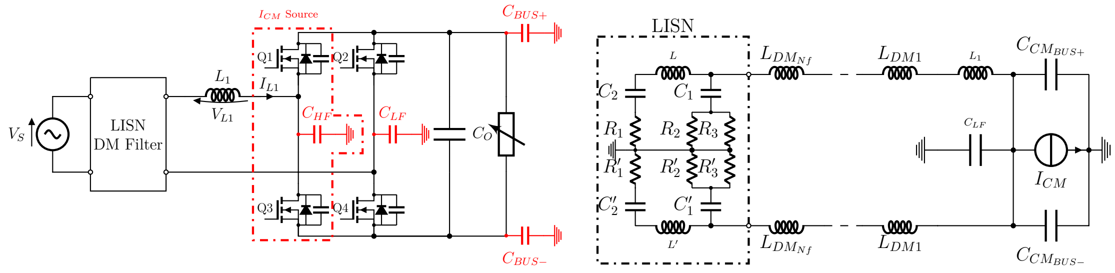
(c) Damping capacitors

Figure 3.5.13: Example of current waveforms in a 3 stage DM filter

frequency harmonics. The losses in the damping resistor are calculated in the same way. In this case the resistor value is directly used. Losses in the filtering inductor are calculated with the method presented in the sub-section 3.5.2. The inductor current is used to calculate the copper and core losses.

3.5.3.2 Common Mode filter based on ZVS-dependent transient

Secondly, CM filter is designed. Same principles as for DM filter are used, only the equivalent model changes. For CM filter, attenuation calculation depends on parasitic capacitors, selected semiconductor devices and modulation. CM perturbations are different if the commutation is in ZVS or not. CM filter capacitors are limited by maximal earth current flowing through capacitors due to grid connection. Inductors are designed with Nanocrystaline core. This material allows to obtain high inductor value with reduced winding turn. Losses in CM filter are estimated with 50 Hz current flowing through CM chokes winding.



(a) Converter and parasitic capacitors (b) Equivalent Circuit

Figure 3.5.14: CM perturbation model.

The most important point to understand in this section is the contribution of each parasitic capacitor. The converter is composed of HF and LF legs. Indeed, HF legs are switching fast with high $\frac{dV}{dt}$ which induce high common mode current in parasitic capacitors. The LF leg switch every 10 ms which is low, moreover this commutation can be done very smoothly by adding an additional gate resistor leading to low common mode current. Hence, in the pre-design, the combination of HF and LF leg commutations are considered as CM current sources. Figure 3.5.14.(a) corresponds to the converter and the associated parasitic capacitors used to develop the model of Figure 3.5.14.(b). With the model, it is noticeable that the parasitic capacitors between the earth and the DC bus (plus and minus) offer a path to the CM current reducing the current flowing through the LISN. Note that the DC link capacitor (Co) is represented as low impedance path at the considered frequency. Indeed, these capacitors contribute to filter the CM perturbations. This point must be kept in mind during the routing to try to increase these parasitic capacitor while capacitor between the mid-point connections and earth must be reduced as much as possible [44].

The common mode current depends on several parameters : parasitic capacitor, DC Bus voltage, inductor current, device parameters and modulation principle. The most critical one is the parasitic capacitor, as it is mentioned above, the higher the capacitor value, the higher the common mode current, therefore the bigger the CM filter. The common mode current is generated by the voltage variation from the commutation of the switches, see Equation 3.5.18. As presented in the Figure 3.3.6, the common mode voltage mainly depends on HF legs.

$$I_{CM} = C_{HF} \cdot \frac{dV_{MID}}{dt} \tag{3.5.18}$$

The voltage slope depends on the switch performances and characteristics such as, rise time, fall time and $\mathrm{C_{OSS}}$. It is also important to distinguish soft and hard switching. For hard switching only rise time or fall time are significant. But, in the case of soft-switching, the voltage variation depends on $\mathrm{C_{OSS}}$, and possible additional capacitors, and switched current. The design methodology includes this two cases.

For hard switching, the conducting device is turned off and the body diode start to conduct to insure the current continuity. Hence, the mid-point voltage variation is assumed when the second device is turned on, so the voltage variation is expressed as in Equation 3.5.19, where tr is given in the datasheet.

$$\frac{dV_{MID}}{dt} = \frac{\Delta V_{DC}}{tr} \tag{3.5.19}$$

For zero voltage switching the turn off of the conductive device induces a charge/discharge of $\mathrm{C_{OSS}}$(and additional parallel capacitor), as it is explained in Figures 3.5.3 and 3.5.4, this transient is mainly driven by the value of the inductor current. The higher the inductor current, the faster the charge and discharge of output capacitor. Therefore, the voltage variation is calculated with Equation (3.5.20).

$$\frac{dV_{MID}}{dt} = \frac{\Delta V_{DC}}{tf + \delta t} \tag{3.5.20}$$

with

$$\delta t = \frac{C_{OSS} \cdot V_{DC}}{IL} \tag{3.5.21}$$

Figure 3.5.15 presents the common mode current obtained with the assumptions on the voltage variation of 400 V and a parasitic capacitor of 4 pF. Figure 3.5.16 presents the LISN voltage obtained with the equivalent model used for CM perturbation estimation.

Determination of the component values

From previous results the CM filter can be designed in a similar way as DM filter. Firstly the maximal capacitor (Y2 Type Ceramic) value is determined according to maximal earth current (3.5 mA). The global capacitor is then shared according to the number of CM filter stages. Note that the capacitor close to the converter is higher than the capacitor at the grid side to favour a short pass for CM current, see Equations (3.5.22) and (3.5.23).

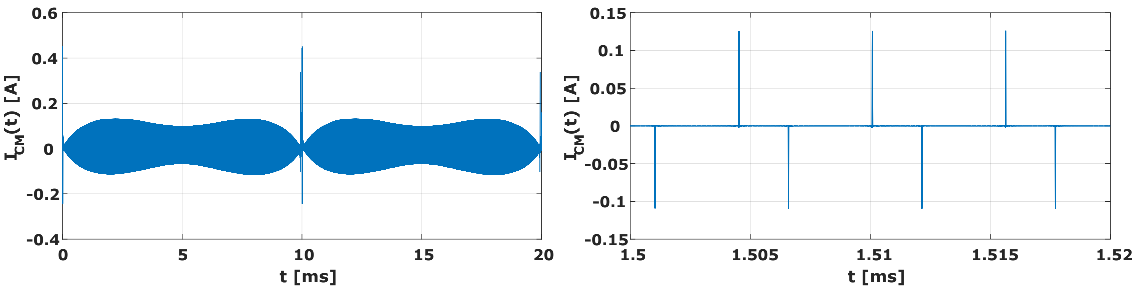
$$C_{CMtot} \leq \frac{3.5 \cdot 10^{-3}}{260 \cdot 2\pi \cdot 50} = 43\,nF \tag{3.5.22}$$

$$K = \frac{1}{2} \cdot Nf \cdot (Nf+1) \rightarrow C_{CMmin} = \frac{C_{CMtot}}{K} \tag{3.5.23}$$

Knowing the required attenuation, the dimensioning frequency and the different capacitor values, it is possible to determine the value of the CM choke, which is the same for each filter stage, as it is presented with Equation (3.5.24).

$$L_{CM} = \frac{1}{2} \cdot \sqrt[Nf]{\frac{10^{\frac{Att_{req}}{20}}}{(2\pi \cdot f_D)^{2Nf} \cdot \prod C_{CMi}}} \tag{3.5.24}$$

With the required inductance, several solutions are tested depending of core and copper sections (min = 0.88 mm^2 and max = 4.9 mm^2 for copper wires). Nanocrystaline core from Vacuumschmelze are selected because of their high



(a) During a grid period

(b) Focus on few commutations

Figure 3.5.15: Common Mode Current

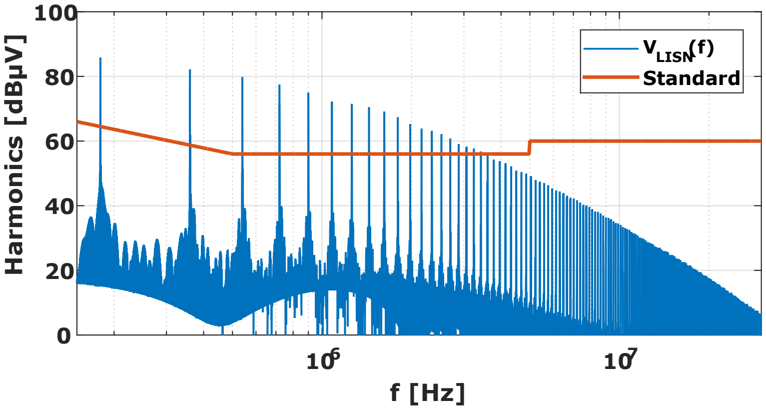


Figure 3.5.16: Example of LISN CM voltage in frequency domain

permeability. It is thus possible to reach high inductance with a reduced number of turns, which makes this technology very suitable for CM chokes.

Losses calculation

Losses generated by the CM chokes are calculated with the DM current flowing through windings. Natural convection is considered for CM chokes (no contact with the heat sink). The maximal temperature increase for chokes is limited to 40°C, every solutions with higher temperature increase are eliminated. Finally, the procedure of EMI filter returns several combinations of DM and CM filter with their respective volumes and losses.

3.6 Conclusions

In this chapter the selection of the full bridge topology with a mid-point inductor is seen as the most suitable configuration. This topology is considered as an elementary cell that can be used in more complex converters, e.g. interleaved converter, MMC or even isolated DC/DC converter. The main aspects in converter design are reduction of losses, EMI perturbations and overall volume. This is impacted by the semiconductor selection, especially WBG, the control and 3D system assembly. The assembly is a main concern in this project as highly integrated converter is investigated. Therefore the design of suitable design flow is mandatory.

The optimisation procedure presented in this chapter includes all these aspects making it suitable for integrated converter. Indeed, the increase in the switching and/or the apparent frequency, by interleaving, is considered to reduce the size of passives, in particular the inductors. In addition, the increase in the switching losses, especially Turn ON losses, is handled by investigating the modulation and conduction mode. The unipolar modulation coupled with two conduction modes is studied. The first case is the TCM that the advantage is soft switching (ZVS) operation independently of the load. But this requires a variable switching frequency control. The second case is the classical fixed frequency CCM. This chapter shows that this conduction mode is also interesting when the objective is reduction of passives and power integration. Indeed, the interleaving and the increase of current ripple allow the inductors to be reduced but also ZVS to be achieved without the variable switching frequency drawback.

These operation modes need to be considered in the EMI filter. The proposed methodology takes into account the impact of the interleaving especially for the DM filter. The high apparent frequency enables the reduction of the DM filtering even if just two cells are operating at light load. The analytical approach is suitable to pre-design the EMI filter. A possibility with this method is to optimise each EMI filter inductor separately as all the currents are known, at the expense of computation time. However, the lack of parasitic element estimation can be problematic, it is considered as major improvement. In the case of the CM filter, the impact of soft switching is analysed. Soft switching is better than hard switching concerning EMI signature. Hence, the variable transient time of ZVS commutation is included in the design. The analytical model is designed to only use the datasheet parameters and specifications of the converter. Therefore the computation time is kept low.

The results of the optimisation procedure was presented in the next chapter. The optimisation was ran for non-interleaved converter to evaluate the relevance of the modulation, TCM or CCM, in such type of converter. Two prototypes were built and evaluated. The first one was realised with off-the-shelf components, and the second one is the integrated version, with embedded components, active and passives. Both of these prototypes were realised from the complete optimisation procedure results, including the interleaving with the continuous conduction mode.

Chapter 4

Optimisation results of PFC

In the previous Chapter the optimisation procedure was presented. This Chapter presents the results obtained. Results are presented as a scatter plot in the efficiency (η) vs power density (ρ) domain. Firstly, the optimisation is performed for non-interleaved converters. In this case the densest converters are analysed. Then the interleaving is introduced. For interleaved results, the optimisation is applied to discrete and integrated converters. The final result is defined as the highest power density converter reaching the minimal efficiency criteria. Both converters are built and presented.

4.1 CCM preferred for non-interleaved converters optimisation

Most of the studies on the TCM present interleaved converters, but none of them compare the CCM and TCM in the case of non-interleaved converters. Hence, this preliminary study was performed to compare these two modulations in this particular case.

4.1.1 Highest density CCM converter reached at 140 kHz

Figure 4.1.1 presents results for CCM control at nominal power (3.3 kW). When the switching frequency varies between 140 kHz and 340 kHz, the current ripple range

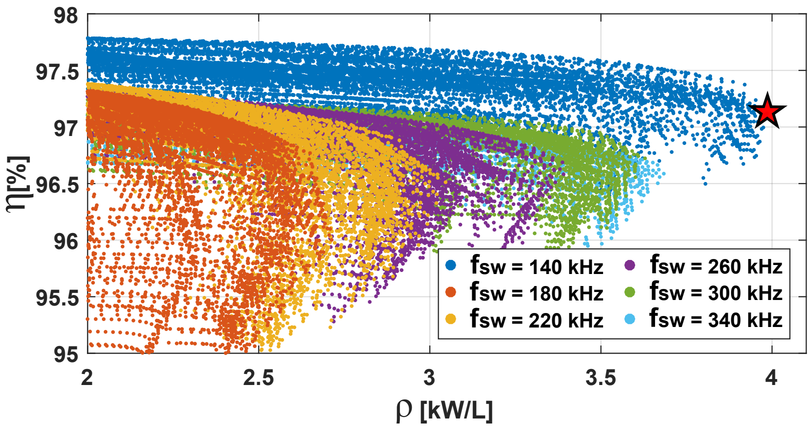
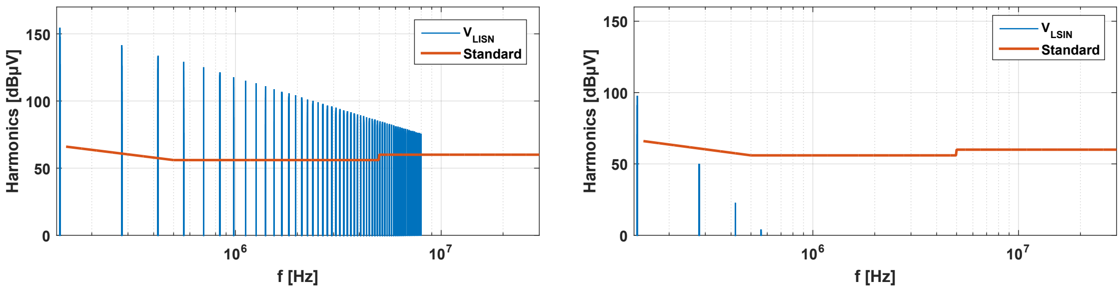
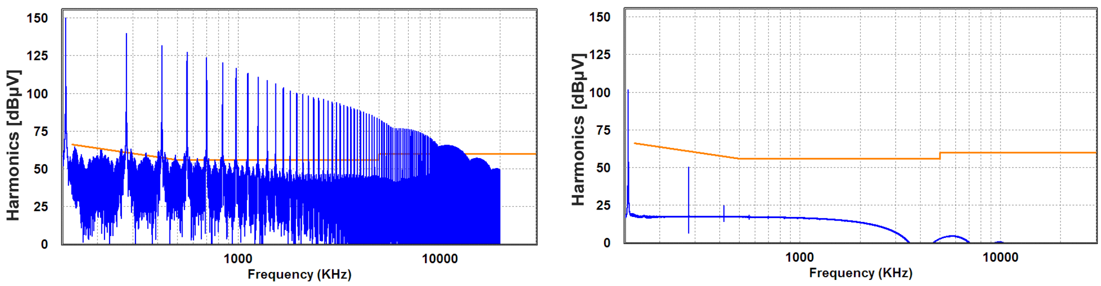


Figure 4.1.1: Optimisation results for CCM N = 1



(a) Analytical results without EMI filter (b) Analytical results with EMI filter



(c) PSIM simulation results without EMI filter (d) PSIM simulation results with EMI filter

Figure 4.1.2: DM LISN spectrum for CCM converter

is from 2 A to 12 A, the highest density point is obtained for 140 kHz switching frequency and 8 A current ripple. The switching frequency is the lowest value of the optimisation range. It can be seen that the power density is increasing continuously from 180 kHz to 340 kHz. However, the disruption of this trend at 140 kHz switching frequency can be clearly seen because first harmonic falls outside of the conducted emission frequency band. The analytical results are confirmed by PSIM simulations (see Figure 4.1.2). The design of the EMI filter is based on the second harmonic instead of the first which leads to significant filter size reduction. In the case of C.C.M, the maximum switching frequency is bound to 340 kHz because the gain on power density is not sufficient to overcome the low efficiency.

4.1.2 Highest density TCM converter reached at 650 kHz

Concerning T.C.M, the results are presented in Figure 4.1.3. The densest converter corresponds to a design with the highest switching frequency, 650 kHz at 330 W. This switching frequency is relatively close to the limitation of switching capabilities of SiC and SJ MOSFET. The value of the maximal allowed reverse current is $I_R = -3A$.

As the TCM induces variable switching frequency control, the harmonic content is densest than in the case of CCM. Moreover, the main part of these harmonics appear at frequencies lower than the minimal frequency considered in the standard

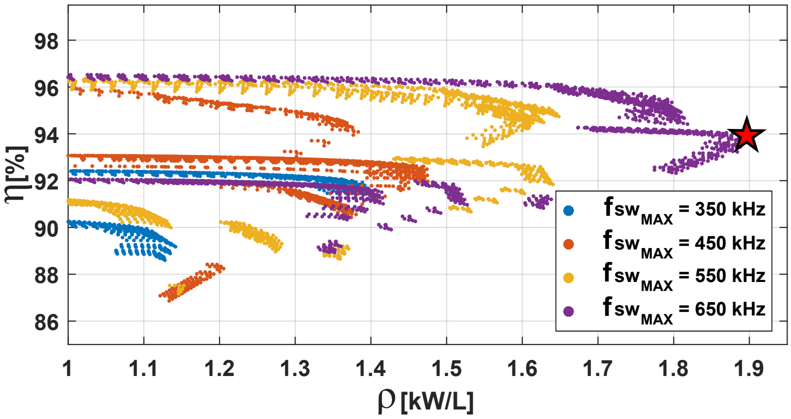
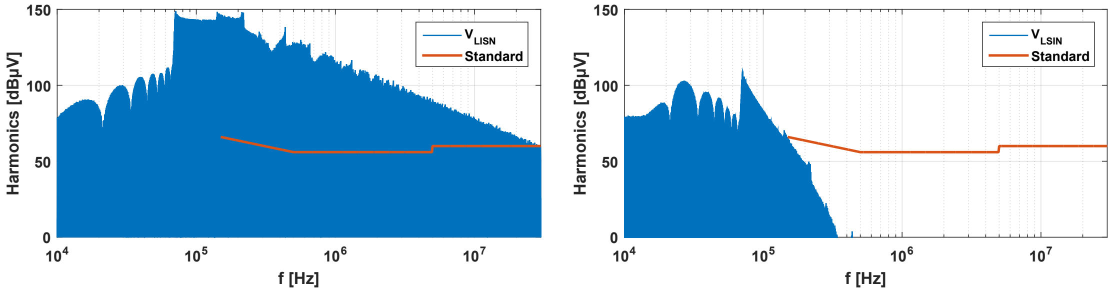


Figure 4.1.3: Optimisation results for TCM N = 1



(a) without EMI filter

(b) with EMI filter

Figure 4.1.4: LISN spectrum for TCM converter

(see Figure 4.1.4). Thus, the design of the EMI filter, in particular the DM part, is impacted by the THD. This additional criteria induces bigger EMI filter.

4.1.3 Analysis and comparison

The comparison of the two highest density converters is presented in Table 4.1. On one hand, the converter operating in CCM has a much smaller current ripple. It leads to acceptable losses in the input inductor and in the EMI filter. The volume of these parts of the converter is also acceptable. With this commutation mode the semiconductors operates in hard and soft-switching. Therefore, the optimisation tends to reduce the switching losses by selecting a SiC device with small output capacitor and recovery charge of the body diode. The overall losses are controlled to limit the impact of the cooling system design according to the thermal coefficient (natural convection $5\text{cm}^3/\text{W}$).

On the other hand, the converter designed with TCM has a very high current ripple. It widely impacts the final results. The main advantage is the reduction of the switching losses due to full ZVS operation. Therefore, the optimisation selected the device with the lowest on-state resistance, in the database, to also decrease the conduction losses. However, this high current ripple leads to higher losses in the input inductor and in the EMI filter, which is also bigger to filter all the HF noise. The thermal management needs to be bigger with the TCM to dissipate the losses in the passive components.

To conclude on this study of non-interleaved converters, the presented results show that CCM is the most interesting conduction mode in terms of efficiency and power density, even if some commutations occur in hard condition. The high current ripple in TCM widely reduces the efficiency and the power density. Power density achieved with CCM is 3.98 kW/L whereas TCM achieves only 1.9 kW/L.

The combination of poor results and high complexity of control make the TCM an irrelevant solution without interleaving. The following is mainly focused on converters controlled with Continuous Current Mode.

Table 4.1: Comparison of converters obtained for CCM and TCM for $N = 1$

		Design for CCM @3.3kW	Design for TCM @3.3kW
General	η	97.12 %	93.87 %
	ρ	3.98 kW/dm^3	1.9 kW/dm^3
	$f_{SW_{MAX}}$	140 kHz	650 kHz(@ P_{MIN})
	ΔI	8 A	-
	I_R	-	-3 A
	L_{PFC}	89.28 µH	18.51 µH
	Devices	C3M0065090J(SiC)	SCT3030AL(SiC)
	Nb EMI filter stages	3	3
	L_{DM}	21.06 µH	52.31 µH
	C_{DM}	[0.33 µF, 0.224 µF, 0.132 µF]	[0.33 µF, 0.224 µF, 0.132 µF]
	L_{CM}	0.3525 mH	0.69 mH
	C_{CM}	[19.2 nF, 12.7 nF, 6.5 nF]	[19.2 nF, 12.7 nF, 6.5 nF]
Volume	Total	813.02 cm^3	1740.08 cm^3
	L_{PFC}	84.24 cm^3	67.39 cm^3
	DM filter	186.18 cm^3	495.49 cm^3
	CM filter	77.58 cm^3	160.82 cm^3
	Switches+Driver	4.92 cm^3	5.78 cm^3
	Heat sink	460.1 cm^3	1010.6 cm^3
Losses	Total	95.02 W	202.12 W
	L_{PFC}	12.34 W	20.39 W
	Switches	53.45 W	45.45 W
	EMI filter	29.22 W	136.27 W

4.2 Interleaving for improved power converters

Two prototypes are designed. The first one is only composed of off-the-shelf components and planar inductors which represents a first step in the PCB integration. The second prototype is the integrated version. In this case the PCB embedding technology is employed. Power dies, gate drivers and inductor are embedded. The assembly corresponds to a PCB stack on the heat sink in a modular approach.

The main differences in the optimisation procedure to design theses two converters are the considered inductor technologies (planar vs PCB-embedded) and the semiconductor references (packaged devices vs bare dies)

The cell shading was investigated and widely impacts the design of the EMI filter. It has not been included in the design of the discrete converter due time constraints, but this functionality is permitted in the integrated version.

4.2.1 Optimisation results with discrete and packaged components

The main difference between the discrete and the integrated converter is the EMI filter. The decision about cell shading and EMI filter designed for the worst case of $N = 2$ has been taken after the beginning of the conception of the prototype. Hence, the implemented EMI filter allows to be compliant with the standard only with the four operational cells. Figure 4.2.1 presents the optimisation results in the ρ vs η domain with a thermal coefficient equal to $5\,\mathrm{cm}^3/\mathrm{W}$. The impact of main variables (N [2 ; 5], f_{SW} [140 kHz ; 300 kHz] and ΔI [2 A ; 12 A]) are analysed for the integrated converter.
The selected converter achieves 98.1 % of efficiency and $5.5\,\mathrm{kW/dm}^3$ power density (sum of components box volume). The optimal converter corresponds to four interleaved cells switching at 180 kHz with an input current ripple of 4A. This configuration can be explained by looking the current waveforms (see Figure 4.2.2). The increase in the number of interleaved cells induces a reduction of the required input inductor value. Moreover, the average current (50 Hz component) in each cells is reduced, thus losses are also shared. The higher the number of interleaved

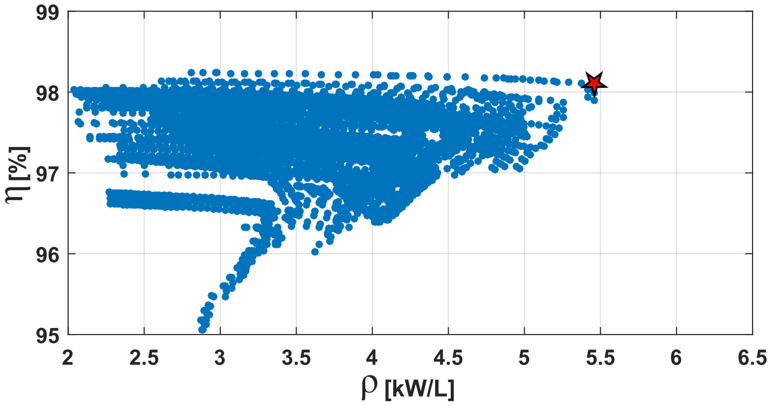
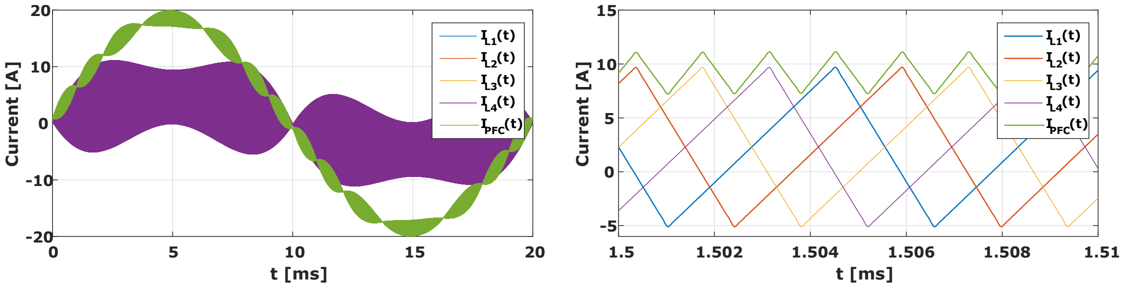


Figure 4.2.1: Results of the discrete converter optimisation



(a) Currents at the grid frequency

(b) Currents at the switching frequency

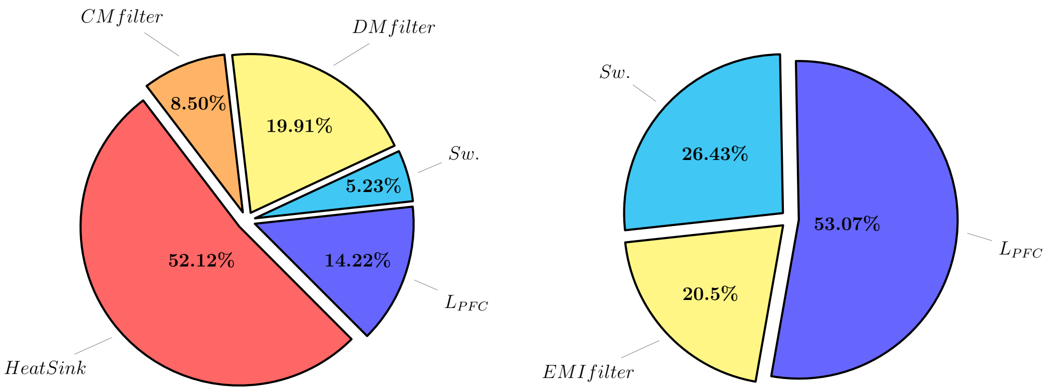
Figure 4.2.2: Discrete Converter Current Waveforms.

cells, the higher the apparent frequency, so the smaller the EMI filter. The second factor is the switching frequency. The higher the switching frequency, the smaller the input inductor. However, an excessive increase in the switching frequency induces higher losses due to high frequency effects. The current ripple impacts the losses in the semiconductors and inductors. High current ripple induces higher conduction losses, but in counter part the switching losses are reduced and the inductors are smaller.

Therefore, the optimisation procedure leads to this particular configuration of multi-cells converter operating at high frequency with an important current ripple. The selected converter can achieve ZVS for complete main period. The converter with CCM control has the advantage of soft switching , like TCM. But the variable switching frequency control and zero crossing detection drawbacks are avoided.

Table 4.2: Details about the discrete converter.

Design for CCM @3.3kW					
General	η	98.1 %	Volume	Total	599.55 cm^3
	ρ	5.5 kW/dm^3		L_{PFC}	4 × 21.31 cm^3
	N	4		DM filter	119.43 cm^3
	f_{SW}	180 kHz		CM filter	51.02 cm^3
	ΔI	4 A		Sw.+Driver	31.36 cm^3
	L_{PFC}	34.72 µH		Heat sink	312.5 cm^3
	Devices	2//C3M0065090J			
	Nb EMI filter stages	Nf_{DM}=2, Nf_{CM}=2			
	L_{DM}	16.12 µH			
	C_{DM}/C_D	[0.5 µF, 0.33 µF]	Losses	Total	62.5 W
	R_D	[11.56 Ω, 14.32 Ω]		L_{PFC}	33.17 W
	L_{CM}	0.225 mH		Switches	16.52 W
	C_{CM}	[20.3 nF, 12.7 nF]		EMI filter	12.81 W



(a) Volume (b) Losses

Figure 4.2.3: Volumes and losses repartition for discrete converter

Details about the converter are presented in Table 4.2 and illustrated in Figure 4.2.3. Note that the selected semiconductor device corresponds to two SiC MOSFET in parallel.

The efficiency of the converter for the full power range is presented in the Figure 4.2.4. The efficiency drop is significant for power lower than 1.5 kW. That

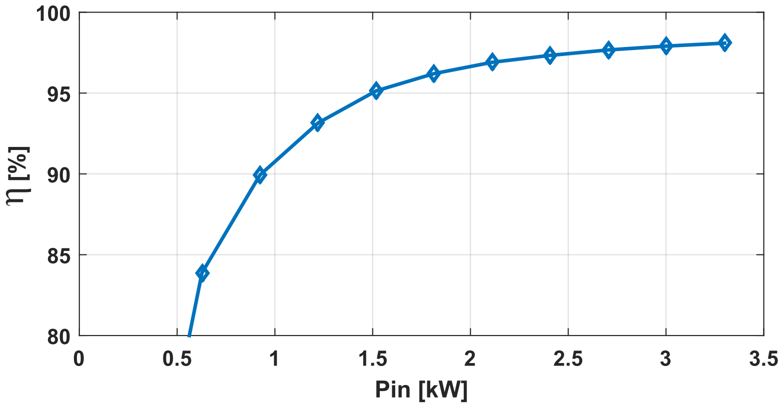
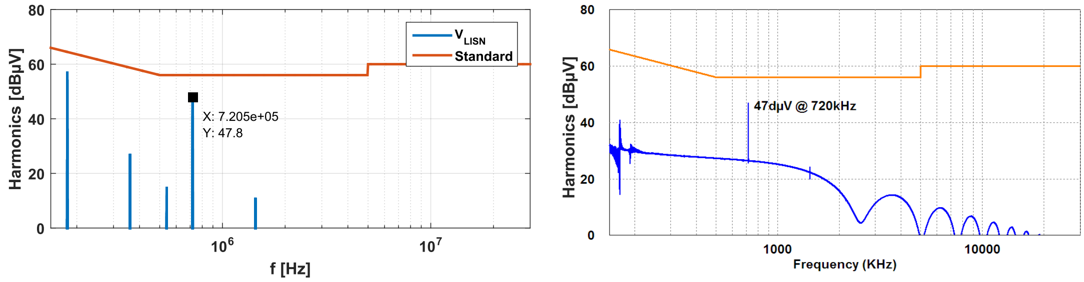


Figure 4.2.4: Calculated efficiency for the discrete converter



(a) Calculated (b) Simulation

Figure 4.2.5: DM LISN spectrum for interleaved (N = 4) CCM converter

is the main motivation to implement the cell shading in the integrated converter design.

The EMI filter is also validated by checking the LISN voltage spectrum obtained by the analytical model and by PSIM simulations. The results obtained for the differential mode are presented in the Figure 4.2.5. Analytical model and PSIM simulations results are equivalent. The attenuations obtained for the dimensioning frequency (720 kHz) are the same. Hence, the model is validated by the circuit simulations.

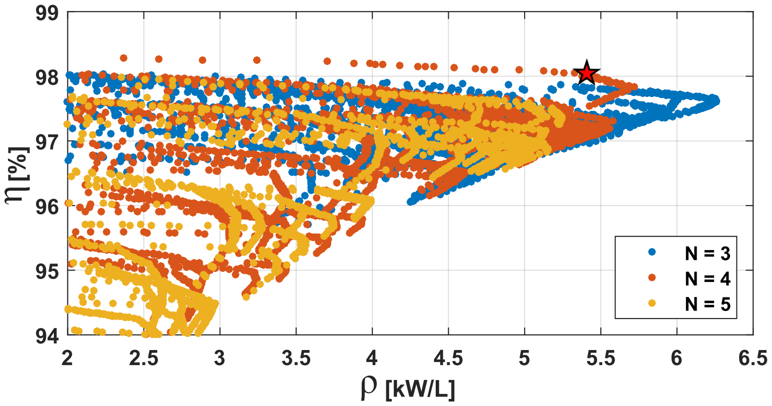
4.2.2 Optimisation results with PCB integrated components

The results for the integrated converter are impacted by the cell shading operation used to maintain high efficiency at light loads. The input EMI filter is designed to guarantee the compliance with the standard for the complete power range. Hence, it is designed for the worst case of operation corresponding to the lowest number of interleaved cells (N = 2), the waveforms are recalculated for the EMI filter design. The inductor technology implemented for the integrated version is the embedded toroidal type as it represents a step forward in PCB integration for this range of power. Figure 4.2.6 represents the optimisation results and the impact of the different parameters, the thermal management is also included, the coefficient is also 5 cm^3/W.

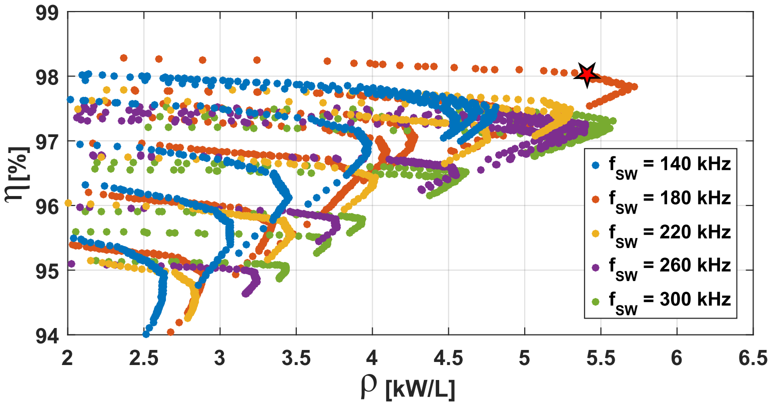
The selected converter corresponds to the same configuration as the discrete converter. Four interleaved cells are operating at 180 kHz and the current ripple is equal to 4 A. Hence, current waveforms are the same than those presented by Figure 4.2.2. As above-mentioned this configuration induces full ZVS during the complete grid period reducing semiconductor losses. In terms of power density, the increase in frequency allows the magnetic components to be reduced, such as input inductor and EMI filter. However, the switching frequency cannot be increased because of HF losses, e.g. skin and proximity effects, in the inductors. Table 4.3 presents the details of the converter. The selected converter achieves 98.01 % efficiency and 5.4 kW/L which is a bit lower than the discrete version. However, EMI filter for integrated converter is designed for the worst case leading to an increase in volume. The losses and volume repartitions are presented in the Figure 4.2.7.

The efficiency of the converter is calculated for different numbers of operating cells to highlight the benefits of cell shading at light loads. The efficiency curves for the power range of 10 % to 100 % of the nominal load are given in the Figure 4.2.8. The selected minimal number of operating cell is two. The configuration with N = 2 can be used for powers below 1.7 kW, then N = 3 for powers between 1.7 kW and 2.6 kW, the full converter with the four interleaved cells is used for powers higher than 2.6 kW.

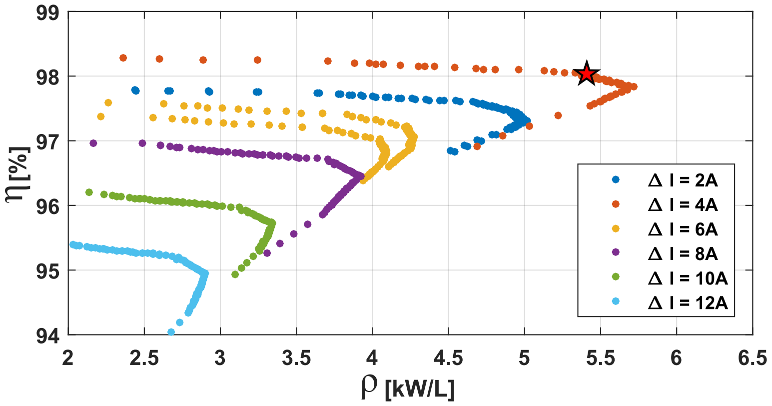
The configuration with N = 1 is represented only to highlight that it is not relevant to use it compared to N = 2. Indeed, the gain on the efficiency is not significant to compensate the drawback induced by the loss of interleaving leading to bigger EMI filter.



(a) Impact of N



(b) Impact of f_{SW} for $N = 4$

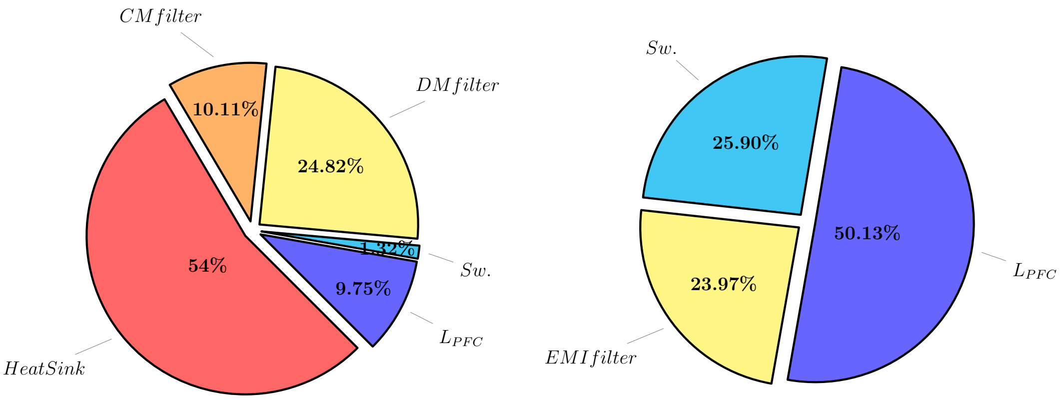


(c) Impact of ΔI for $N = 4$ and $f_{SW} = 180\text{kHz}$

Figure 4.2.6: Results of the integrated converter optimisation

Table 4.3: Details about the integrated converter.

Design for CCM @3.3kW					
General	η	98.01 %	Volume	Total	609.52 cm^3
	ρ	5.41 kW/dm^3		L_{PFC}	4 × 14.88 cm^3
	N	4		DM filter	151.36 cm^3
	f_{SW}	180 kHz		CM filter	61.61 cm^3
	ΔI	4 A		Sw.+Driver	8.04 cm^3
	L_{PFC}	34.72 µH		Heat sink	329 cm^3
	Devices	2//CPM3-0900-0065B			
	Nb EMI filter stages	Nf_{DM}=4, Nf_{CM}=3			
	L_{DM}	7.95 µH			
	C_{DM}/C_D	[0.33 µF,0.282 µF,0.188 µF,0.094 µF]	Losses	Total	65.8 W
	R_D	[10 Ω, 10.88 Ω, 13.33 Ω, 18.85 Ω]		L_{PFC}	32.99 W
	L_{CM}	0.544 mH		Switches	17.04 W
	C_{CM}	[19.2 nF, 12.7 nF, 6.5 nF]		EMI filter	15.77 W



(a) Volume (b) Losses

Figure 4.2.7: Volumes and losses repartition for integrated converter

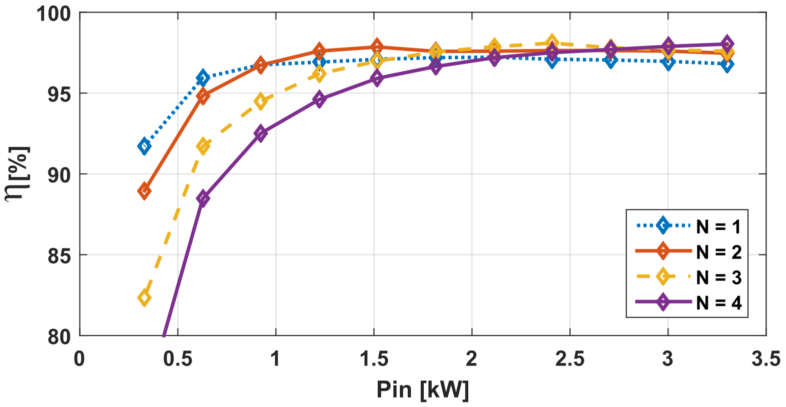


Figure 4.2.8: Analytically calculated efficiency of the integrated converter for different numbers of operating cells

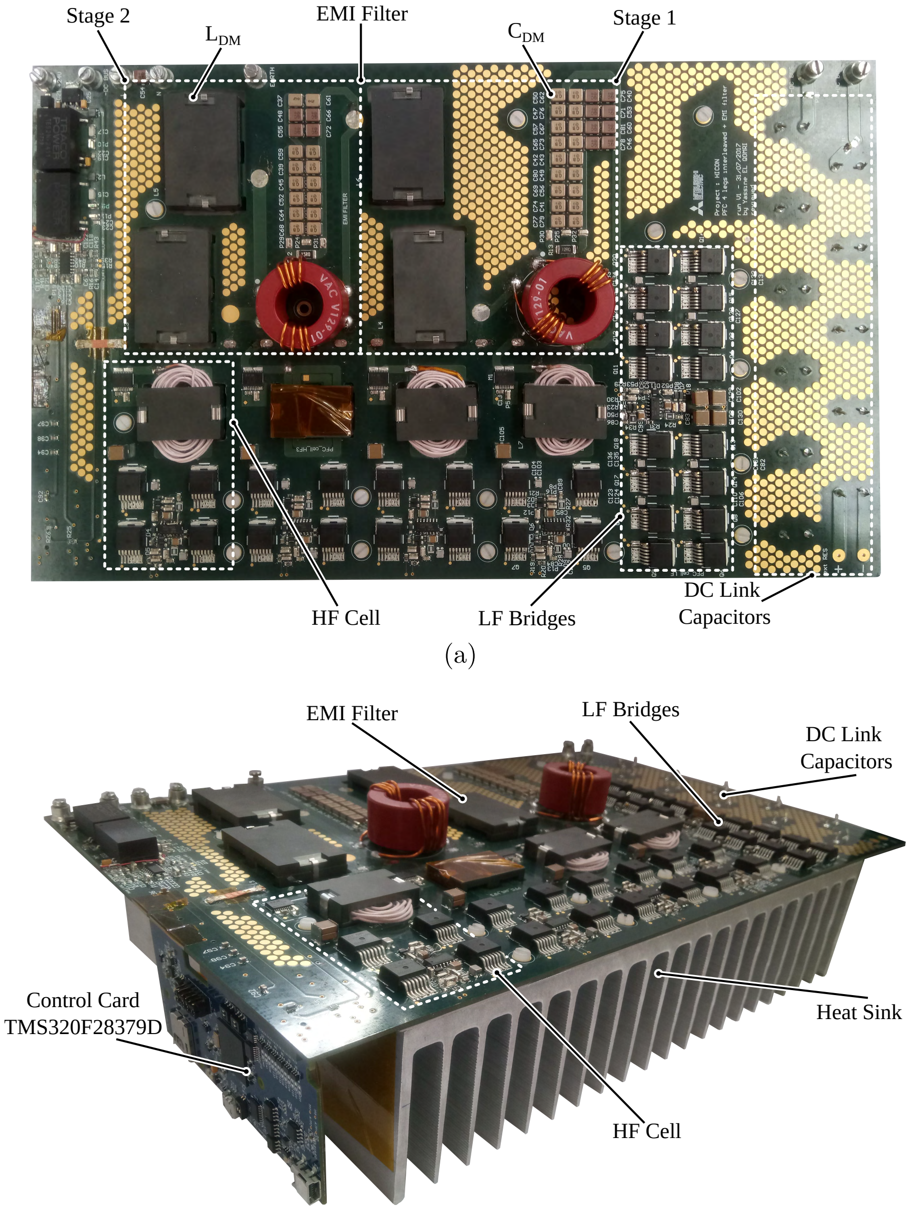
4.3 Optimised power converters evaluation

This section presents the two prototypes designed according to the optimisation results. Performances and EMC compliance are evaluated in both cases.

4.3.1 Discrete converter

The converter presented in Figure 4.3.1 was realised with off-the-shelf components and planar inductors. Some of the inductors were replaced with litz wire wound inductors because short-circuit between turns appeared during the gerber generation process. It is important to notice that the actual heat-sink is oversized with a 60 mm height. The optimal height of the heat-sink is 25 mm. The PCB is a six layers with 35 µm copper thickness. Due to time constraints, the selected PCB is a very standard one. As the manufacturing of this converter is not optimal (105 µm thick copper was expected) the performances do not correspond to the calculated ones. This first discrete prototype is mainly used to validate the control, the hardware implementation, some hypotheses such as ZVS operation and EMI filter.

The volumes obtained with the optimisation procedure correspond to the sum of each component box volume. In practice, the volume is calculated according to the surface of the investigated part of the converter (e.g. switches + gate drivers, inductors, EMI filter) and the highest components in this surface. The



(a)

(b)

Figure 4.3.1: Discrete prototype

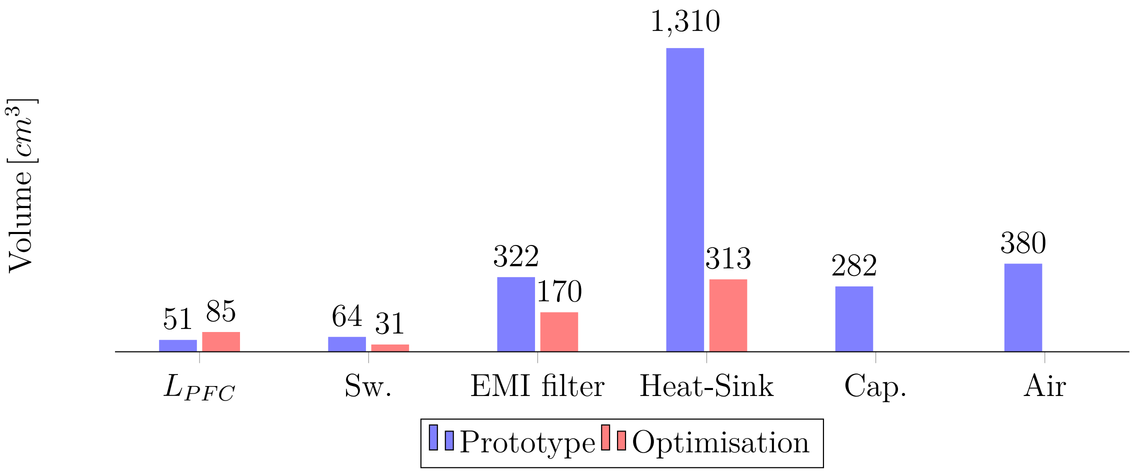
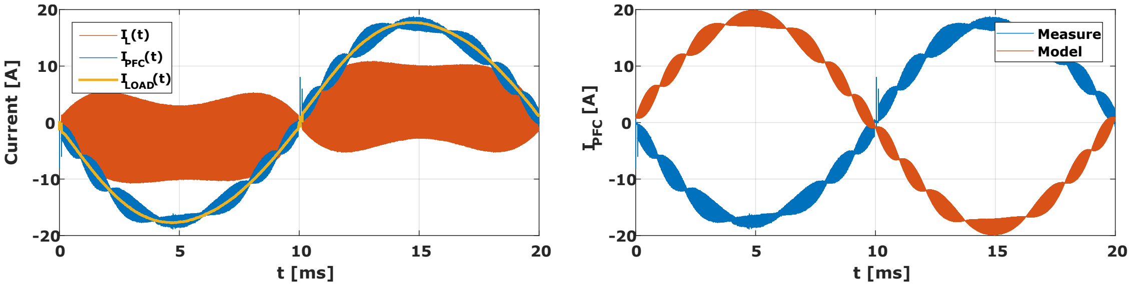


Figure 4.3.2: Volume comparison between procedure and discrete prototype

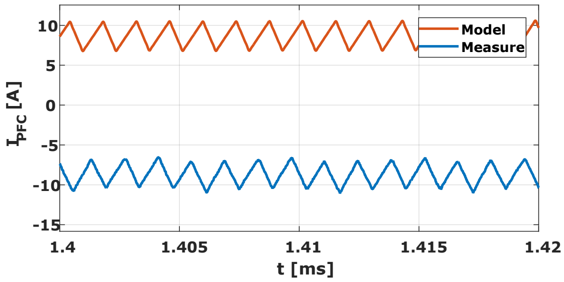
volume of the discrete converter is analysed from the prototype to compare with the optimisation. The results are presented in Figure 4.3.2. This graph shows the differences between the procedure and the hardware realisation. The prototype presents higher volume than calculated. This is mainly due to interconnections which are not included in the procedure. This is mainly noticeable for semiconductors and EMI filter. The EMI filter box volume is also impacted by the height of the common mode chokes. This could be overcome by connecting the chokes on the bottom layer and machining the heat-sink accordingly. The input inductor volume is actually lower than expected because of reduced winding head in practice. Hence, the one board mechanical integration leads to an important part of air. However this configuration facilitates measurements to validate the operation of the converter.

4.3.1.1 Waveforms validation

The optimisation procedure is mainly driven by the calculated waveforms as they directly impact the design (losses, EMI filter, inductor). As it is mentioned before, the current ripple is an optimisation variable. Hence, it is important to validate that the expected current ripple is achieved with the designed inductor, the DC voltage and the selected switching frequency. As the optimisation is realised for the nominal power (3.3 kW), the validation of current waveforms is done at nominal



(a) Measured Currents (b) Comparison during a grid period



(c) Comparison during some switching periods

Figure 4.3.3: Current waveforms of Discrete Prototype

power. The converter is operating in DC/AC mode with a resistive load on AC side and DC voltage source of 400 V. The DC source is the EA-PS 9550-20 5kW from Elektro-Automatik.

The results are presented in Figure 4.3.3. As it is possible to see, the inductor current presents high ripple. The current changes its sign for each commutation during a complete grid period. The measured interleaved current is compared, in the time domain, to the expected current. Both currents are very similar, with the same maximal current ripple.

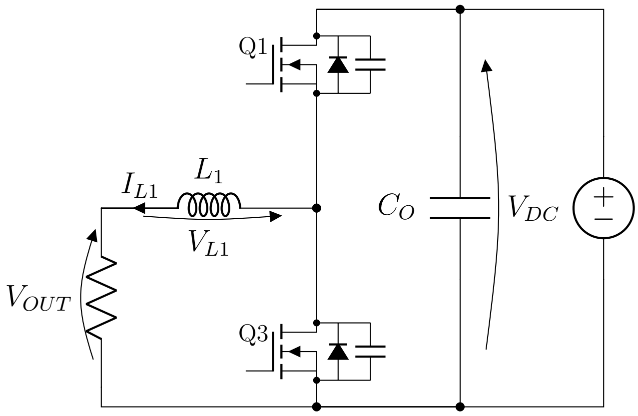
A slight difference can be observed in the interleaved current ripple, this is mainly due to the small unbalance of inductor values and dead-time implemented in the control. However, this has a very small impact on the performances, as the dead-time are selected to be short as possible. Hence, these measurements allow the inductor design and the interleaving technique to be validated.

4.3.1.2 Zero Voltage Switching

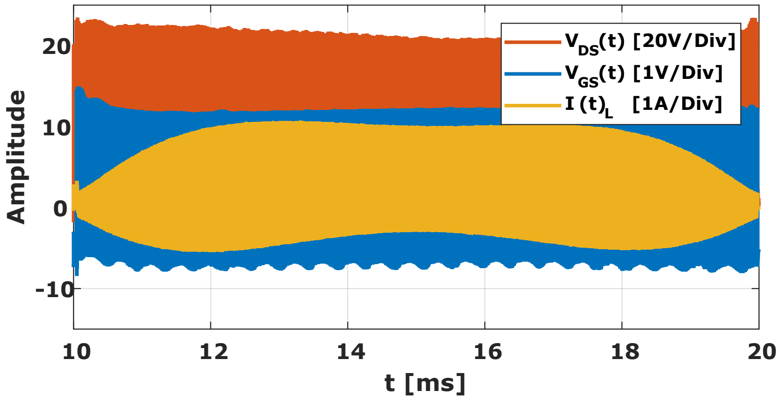
The second validation realised with the discrete converter is also related to the current waveforms. All the requirements to achieve ZVS and the different sequences are presented in the Sub-section 3.5.1. Hereafter, measurements are presented to validate the hypotheses. Usually voltage measurement are preferred than current measurements as it is less constraining for the design in particular for PCB design. For this reason, no particular setup were implemented to measure current in the different switches. To validate that all the devices achieve ZVS only Drain-Source voltage ($V_{DS}(t)$), Gate-Source voltage ($V_{GS}(t)$) and inductor current are measured. It is assumed that zero voltage switching is achieved if $V_{DS}(t)$ reaches zero before a positive $V_{GS}(t)$ is applied to the device to turn it ON. It was presented previously that at least one switch achieves ZVS during each half cycle of the grid voltage. Hence the two cases depending on the AC voltage sign are presented below. Tests are also realised in the DC/AC operation mode, the DC Bus voltage and the operating point corresponds to the nominal conditions. $V_{DC} = 400\,V$ and $P = 3.3\,kW$ correspond to the most critical operating point. A resistive load is placed at the AC output. The resistor value is selected to have the voltage corresponding to nominal voltage when the converter is connected to the grid. The validation is done during an interval were the current ripple is the lowest, which represents the worst case. In both cases the switching sequence corresponds to the top switch (Q1) turn OFF, and the bottom switch turn ON after the dead time. The ZVS validation is focused on the bottom switch (Q3).

Positive output voltage

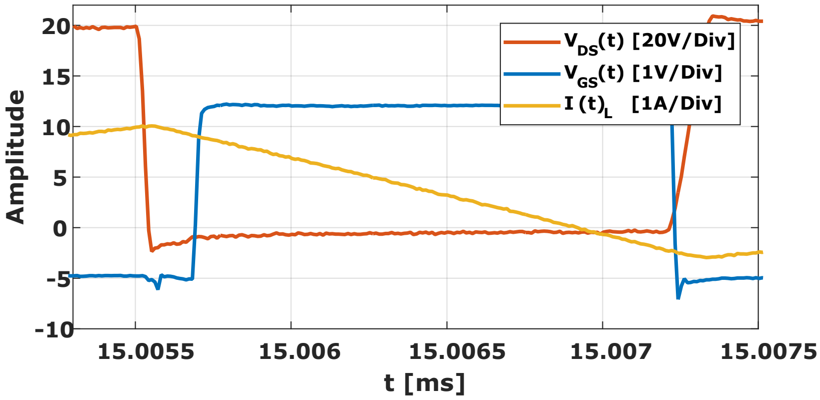
As the test is realised in DC/AC mode, the current is considered positive when it is flowing towards the resistor, therefore the output voltage is also positive. The equivalent, circuit and the waveforms are presented in the Figure 4.3.4. At $t < 15.0055\,ms$ on Figure 4.3.4.(b), the MOSFET Q1 is conducting. Hence, the inductor current increases accordingly to the inductor value, the DC bus voltage and the output voltage. Q1 turns OFF, the inductor current is still positive and will charge/discharge the output capacitor of Q1 and Q3, respectively. If the dead time is long enough, the body diode of Q3 will conduct. After the dead time,



(a) Equivalent circuit for IL(50 Hz) > 0



(b) Grid frequency scale



(c) Switching frequency scale

Figure 4.3.4: ZVS during positive half grid period. V_{DS} and V_{GS} are signals for Q3

the gate signal is applied to turn Q3 ON, the inductor current decreases. As it is possible to see on the Figure 4.3.4.(c) V_{DS} of Q3 reaches zero before the gate the signal is applied, hence it means that Q3 turns ON in ZVS.

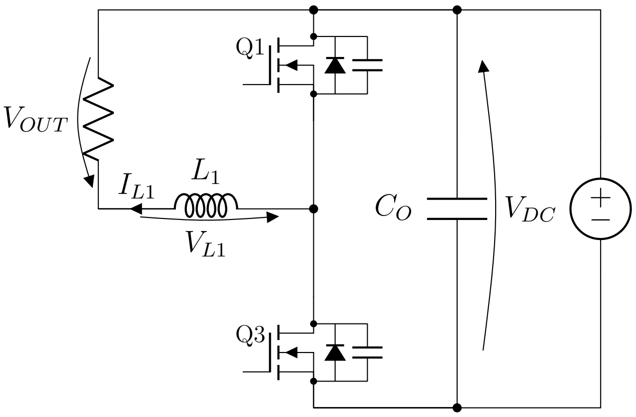
Negative output voltage

The configuration illustrated in the Figure 4.3.5 corresponds to negative output voltage. Hence, the average inductor current is negative. The analysis is still focused on Q3. The initial configuration is the same as previously, Q1 is ON, the inductor current increases from the negative peak value of the current ripple. There are two possibilities. The first one, the current ripple decreases but the value is still negative so the body diode of Q1 will conduct. The output capacitor is not discharged leading to a hard-switching of Q3. The second possibility is when Q1 is ON for a duration long enough to have the inductor current that changes its sign. Indeed, the inductor current changes from a negative to a positive value. For the designed converter, it is typically the case. Therefore, Q1 turns OFF with a positive inductor current. Same as previously, the output capacitor of Q1 will be charged and the capacitor of Q3 will be discharged. Again, the drain-source voltage of Q3 reaches zero before the gate signal is applied (see Figure 4.3.5.(c)). Hence, Q3 turn ON in ZVS because of the high current ripple allowed.

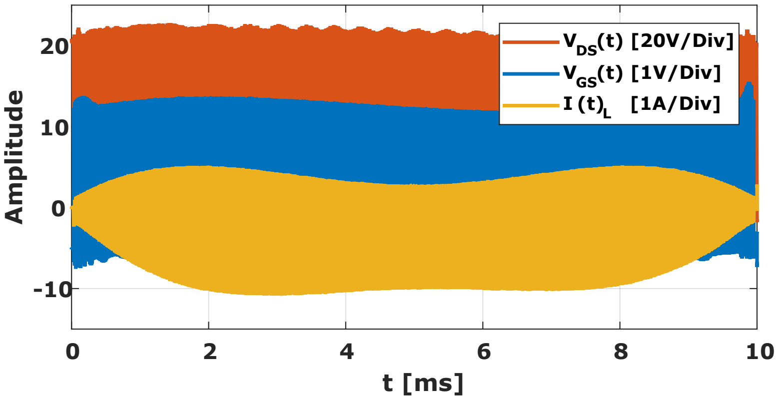
Observing the turn ON of Q3 for positive and negative half period validates the hypothesis of full ZVS operation for all HF switches. Indeed Q1 turn ON in ZVS, reciprocally to Q3, when the current ripple is negative. As the current shape in the three other cells is the same, excepting the phase shift of a quarter of the switching period, the same operation mode is achieved by all other HF switches. Thus, the converter configuration ($N = 4$, $fsw = 180\,kHz$, $\Delta I = 4\,A$) obtained with the optimisation procedure allows to achieve ZVS all along the grid period for all the HF devices and with fixed switching frequency.

4.3.1.3 Efficiency measurement

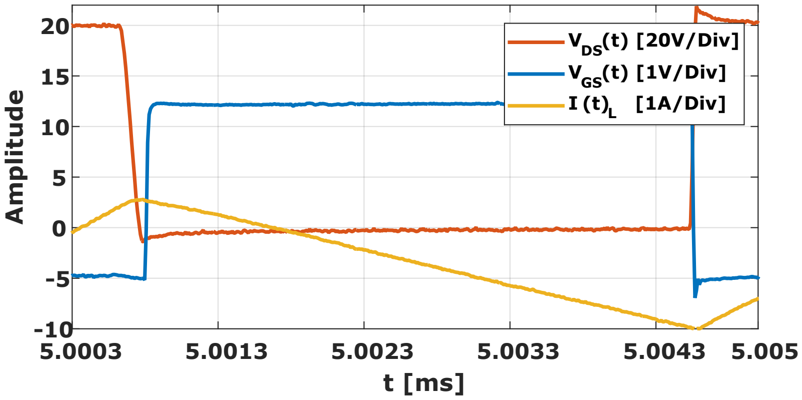
Efficiency measurement, which is one of the selected performance indices, is mandatory. The tests are also realised in DC/AC mode. As previously, the DC supply is the EA-PS 9550-20 5kW from Elektro-Automatik. Two watt-meters are



(a) Equivalent circuit for IL(50 Hz) < 0



(b) Grid frequency scale



(c) Switching frequency scale

Figure 4.3.5: ZVS during negative half grid period. V_{DS} and V_{GS} are signals for Q3

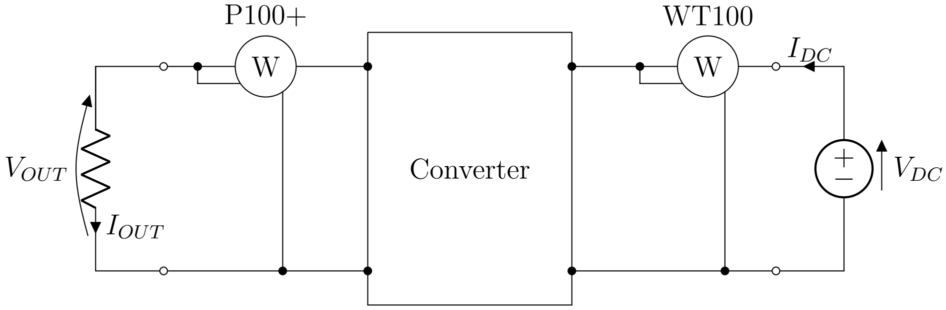


Figure 4.3.6: Schematic of efficiency measurement setup

used to measure the input and the output power. The Voltech P100+ is placed at the AC side (output) and the Yokogawa WTA100 is placed at the DC side (input), as presented in the Figure 4.3.6. The absolute error for the two watt-meters can be found in the user manual (see Equations 4.3.1 and 4.3.2). The relative errors are then used to calculate the error on the efficiency.

$$\delta_{P100+} = \pm((0.2\,\%reading + 0.1\,\%range) + 4\,mW + (\frac{0.05}{PF} \cdot f)\,\%reading) \quad (4.3.1)$$

$$\delta_{WT100} = \pm(0.3\,\%reading + 0.3\,\%range) \quad (4.3.2)$$

Figure 4.3.7 presents the efficiency of the discrete converter. The peak efficiency is equal to 95.83 % ±0.77, this efficiency is obtained for 1.92 kW input power. The efficiency at rated power (3.3 kW) is equal to 95.12 % ±0.64. The efficiency is not as high as expected, this is mainly due to the 35 µm-thick copper used for the PCB design and the replaced inductors. Indeed, the reduced copper section negatively impacts the inductor copper losses. This is highlighted by the Figure 4.3.8 which presents thermal measurements of the converter operating at nominal load. The measure is realised with the Fluke Ti10 IR camera. The hotspot corresponds to the last planar inductor realised with the PCB, high temperature means high losses. However, none of the HF switches presents high temperature.

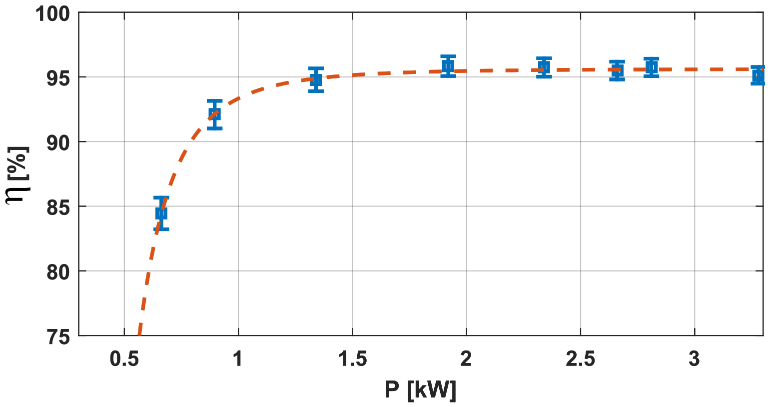


Figure 4.3.7: Discrete converter efficiency

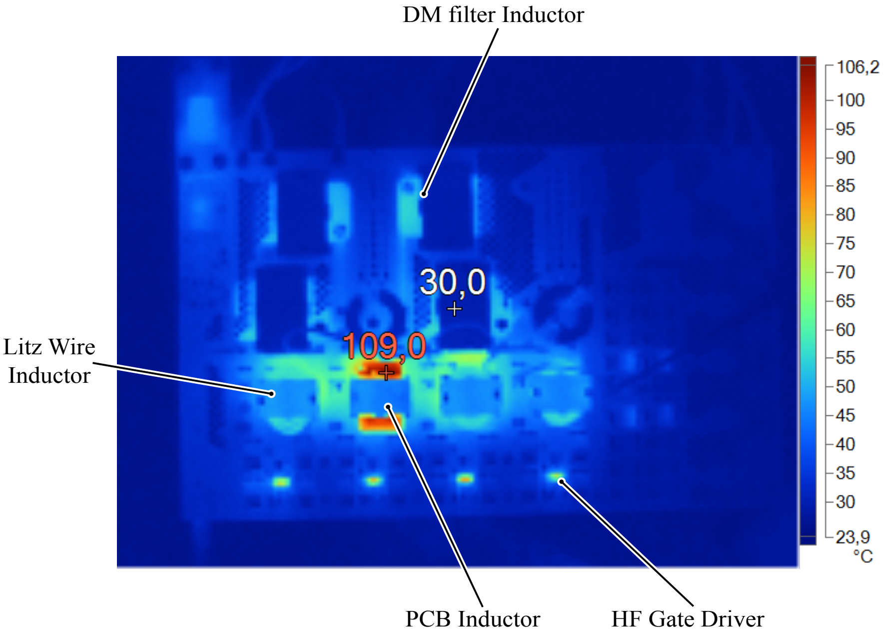
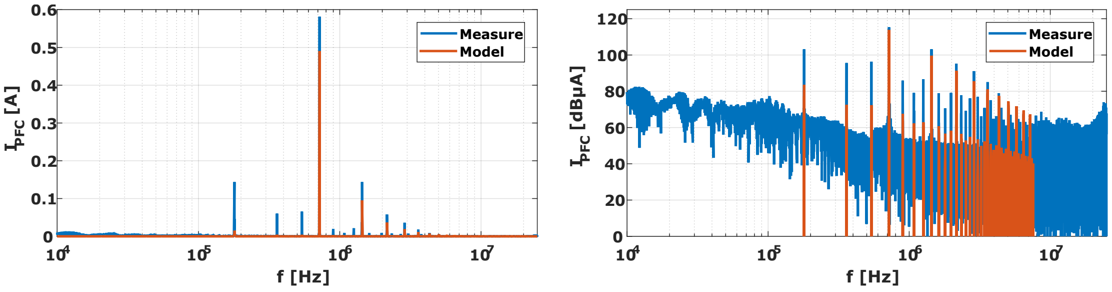


Figure 4.3.8: Thermal measure at 3.3 kW

4.3.1.4 EMC compliance

EMC compliance tests allow the EMI filter design procedure to be validated. Previously the current waveforms were compared in the time domain, no major differences were noticed. In this section, the same comparison between the model and measure is realised in frequency domain. The results of the comparison are presented in Figure 4.3.9. In both cases, the impact of the interleaving



(a) Linear scale

(b) Log scale

Figure 4.3.9: Comparison of PFC current in frequency domain

is substantial as the highest harmonic is observed at four times the switching frequency (720 kHz). At this frequency, the difference between the model and the measure is only 2 dBµA. The model prediction for higher frequency harmonic (higher than 720 kHz) is quite good, the difference is in the range of only few dBµA. The major difference occurs for first switching frequency harmonics. Indeed, the first, second and third harmonic are considerably higher for the measure than the model. The difference is in the range of 20 dB which is quite important. However, this gap can be explained. The model is analytical, so the interleaving is almost perfect because of the very small time step used for the computation (2.5 ns). Hence, the harmonics lower than $N \cdot f_{SW}$ are suppressed. In practice, slight differences between inductors and dead time implemented in the control lead to flawed interleaving. Therefore, the first switching frequency harmonics are more important than expected. Even if the dimensioning frequency is the fourth harmonic, lower harmonics can become an issue in practice. Indeed, the attenuation of the EMI filter may not be enough at these frequencies as it is designed for the dimensioning frequency. This is particularly relevant for multiple stages filter. The higher the number of stages, the higher the attenuation slope. Thus, the corner frequency might be high, slightly before the dimensioning harmonic.

Consequently, the EMC compliance with the EN55011 standard could be compromised by these undesired harmonics. One possible solution to include flawed interleaving in the model is to introduce a small phase shift between the carriers. Thus, the first harmonics will become more important, the fundamental of

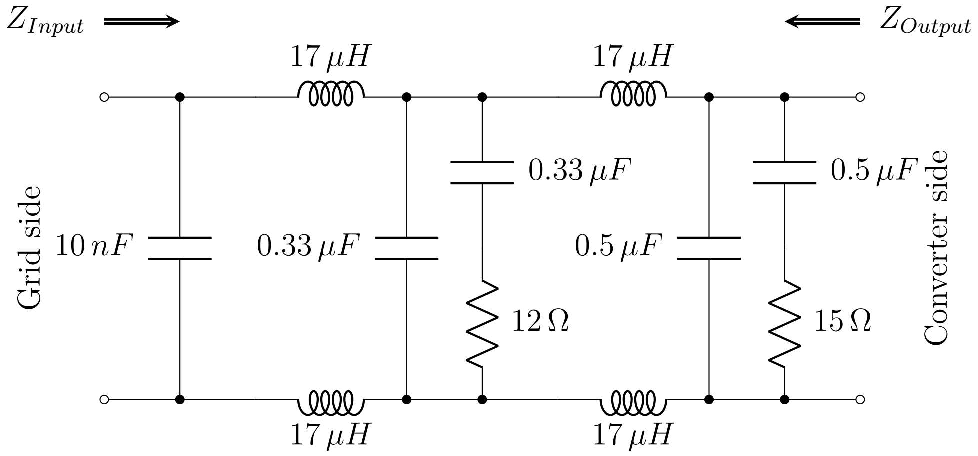


Figure 4.3.10: Discrete DM filter

the switching frequency can become the dimensioning frequency. This can widely impact the overall design, in particular the number of EMI filter stages.

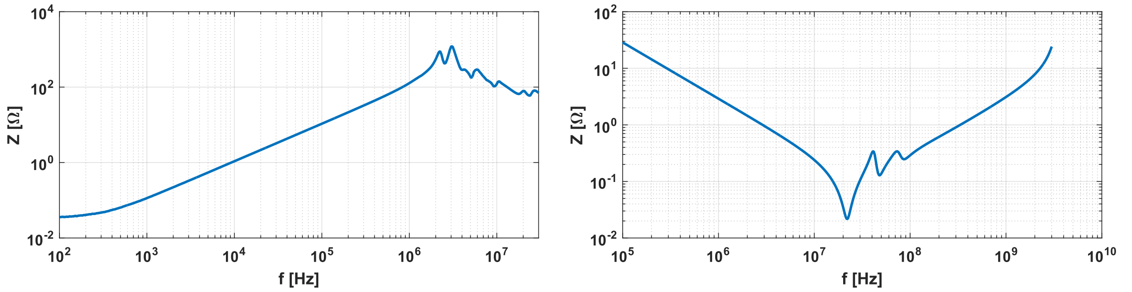
To partially validate the EMI filter model, impedances comparison is realised for the DM filter implemented on the discrete converter. The input (Z_{Input}) and the output (Z_{Output}) impedances are evaluated with a 4294A impedance meter from Agilent and the 42941A probe (Figure 4.3.13). The structure of the EMI filter and all the values practically used are reminded in Figure 4.3.10. The differential mode impedance can be measured even with the elements of the common mode filter. Indeed, the leakage inductance of common mode chokes are negligible compared to the DM inductor. The two series common mode capacitors also have a small value (nF range) compared to the DM capacitance in parallel (µF range), making their impact negligible.

The design of EMI filter is mainly impacted by the parasitics, in particular at high frequency. Therefore, the physical implementation of all the elements which compose the EMI filter can degrade the filtering performances. As the optimisation procedure is a pre-design procedure, the routing cannot be taken into account, because it is unknown when the optimisation results are obtained. Thus, the following presents the model and the improvements realised with the identification of the different parasitics.

The first EMI filter model only includes the filtering capacitor and inductor values, without any parasitics excepted the series resistance used to calculate losses. Since the EMI filter is designed, it is possible to evaluate the parasitics of each components, in particular parallel capacitance for the planar inductor. The parasitic series inductor of ceramic is very small due to the SMD package (GA355XR7GB563KW06 from Murata). However, for this first update, parasitics from packages are determined. Both parasitic elements are estimated from the impedance curve, see Figure 4.3.11. The resonance frequency (f_0) is used to calculate the value of the undesired elements, see Equation 4.3.3. The resonance frequency for the planar inductor and the capacitor are equal to 2.5 MHz and 22 MHz, respectively. Thus, the parallel equivalent capacitance and series inductance are equal to 0.24 nF and 0.93 nH. It is important to highlight that series inductance is only for one filtering capacitor. Hence, those values are added to the impedance models. The series resistance previously used for losses calculation is also added.

$$f_0 = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} \tag{4.3.3}$$

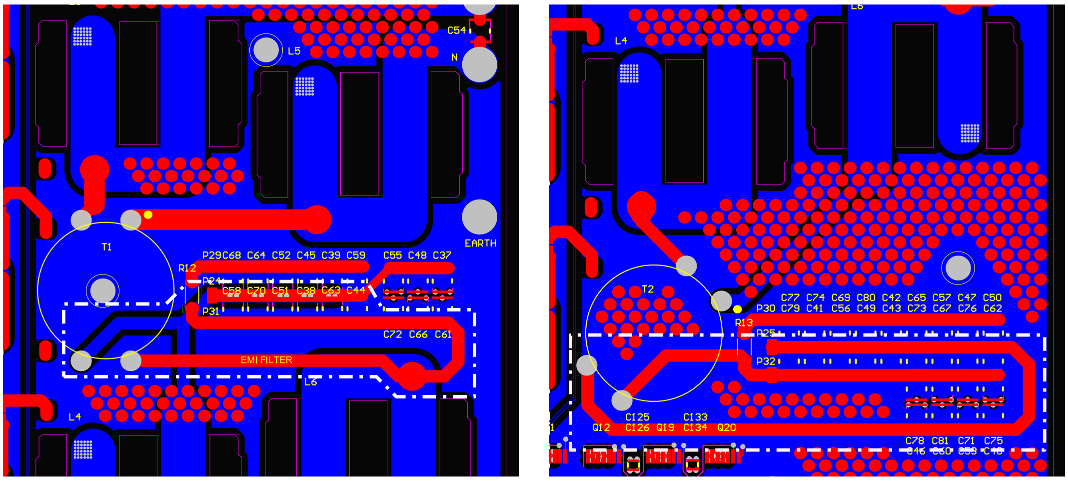
To further improve the model the routing is also analysed. It is particularly relevant for the output impedance as the tracks connecting the capacitor are long. Indeed, the total length of tracks for the first and second stage is 295 mm and 221 mm, respectively (see Figure 4.3.12). Therefore, the stray inductances brought



(a) DM inductor impedance

(b) DM capacitor package impedance measurements

Figure 4.3.11: DM filter impedances



(a) Second EMI filter stage

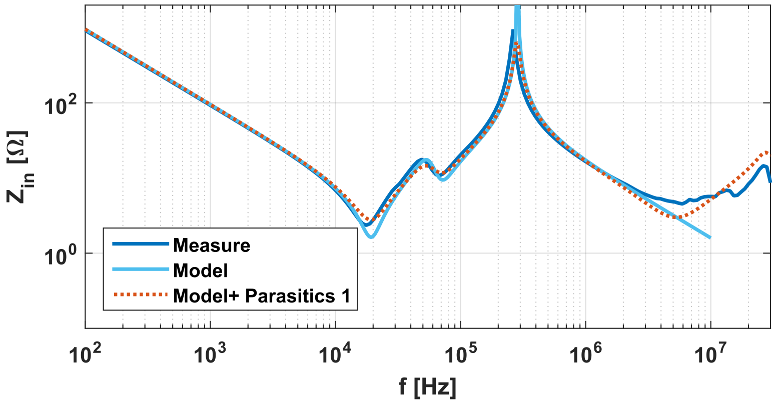
(b) First EMI filter stage

Figure 4.3.12: Additional stray inductances

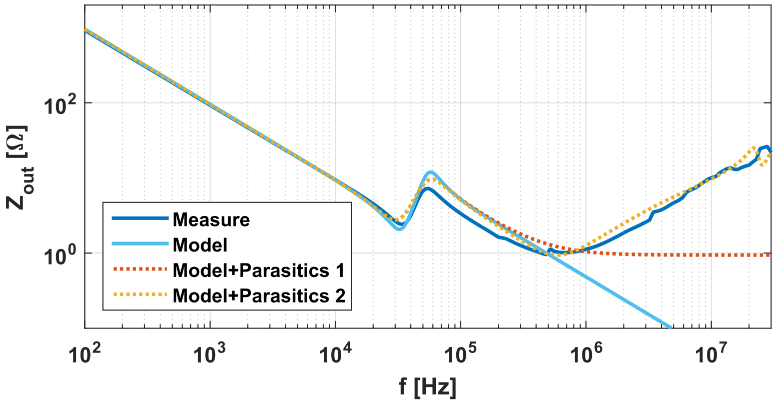
by these tracks are very important. The stray inductance of track can be calculated using the Equation 4.3.4 [84]. Thus, the inductance of tracks with the ratio length (L) vs width (W) equal to 100 is around 10 nH/cm. Hence, the additional inductor are equal to 22 nH and 29.5 nH.

$$L_{Track} = 0.2 \cdot L \cdot \left[\ln \left(\frac{2 \cdot \mathrm{L}}{W} \right) + 0.5 + 0.22 \cdot \left(\frac{W}{L} \right) \right] \tag{4.3.4}$$

The different models are compared to the measures in Figure 4.3.13. The first input impedance model fits the measure up to 3 MHz. The improved model including the parasitic of each component is sufficient to fit the measure up to 30 MHz with simple analytical model. The output impedance is very important as it is the impedance seen by the undesired harmonics (switching frequency harmonics). The deviation of the first version of the model occurs at low frequency compared to the input impedance. Indeed, the output impedance starts to increase at 500 kHz while a decrease in impedance is expected. Contrary to the input impedance, the first improvement of the model is not sufficient to explain this increase and fit the measurement. However, taking into account the layout, especially the stray inductance brought by the track, make the model accurate up to 30 MHz.



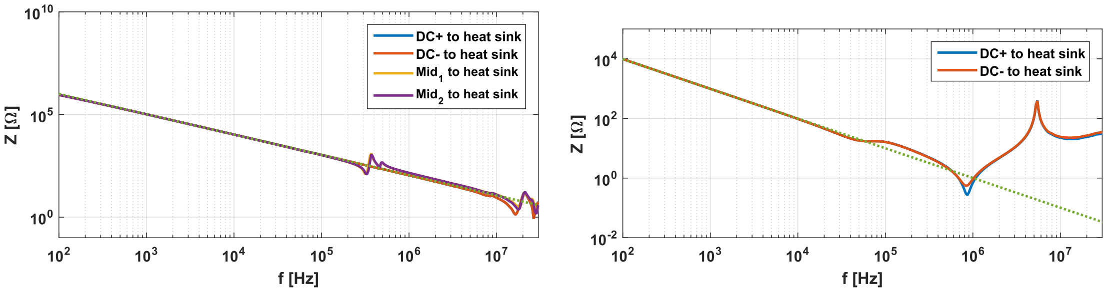
(a) Input impedance



(b) Output impedance

Figure 4.3.13: Two stages DM filter impedances

Hence, the simple analytical model used to design the EMI filter is validated up to 3 MHz and 500 kHz for the input and output impedances, respectively. It is shown that the implementation of the EMI filter is very important as the parasitic mainly depends on the layout. To avoid too high stray inductances, the interconnections must be as short as possible. Including all the parasitic elements in the filter design provides accurate attenuation prediction. This can only be realised since the layout is known. It can also be determined by 3D simulation, with Q3D Extractor for example. However, this kind of simulation is time consuming and requires the layout design. Indeed, coupling this feature in an optimisation procedure is very complex and does not allow fast design.



(a) Without DC supply connected

(b) With DC supply connected

Figure 4.3.14: Common Mode impedances

Other elements which mainly depends on the layout are the parasitic common mode capacitors, responsible of CM perturbations. Those capacitors are impacted by the PCB thickness, the thermal interface and the use of the different layers of the PCB. In the developed procedure, the values are set arbitrarily from knowledge and literature. The first set of values corresponds to non integrated design with slight overestimation to ensure a proper EMI filter design. Hence, the capacitance between the mid-points and earth, and, the DC connections and earth are 1 nF and 10 nF, respectively in the design procedure. To verify this assumption, impedance measurements are also performed. The measurements correspond to C_{HF} and $C_{BUS+/-}$ presented in the Figure 3.5.14. The results are presented in the Figure 4.3.14, two configurations are tested. The first one corresponds to the converter only. The second one corresponds to the converter plus the DC supply. The slope of the impedance curve is used to determine the equivalent capacitance.

In the case without the DC supply, the measured capacitor is equal to 1.5 nF, which is not so far from the first assumption. In the case with the DC supply, the capacitor value is equal to 150 nF. This value is very high and can leads to high common mode perturbations. Moreover, the EMI filter is not designed for such values.

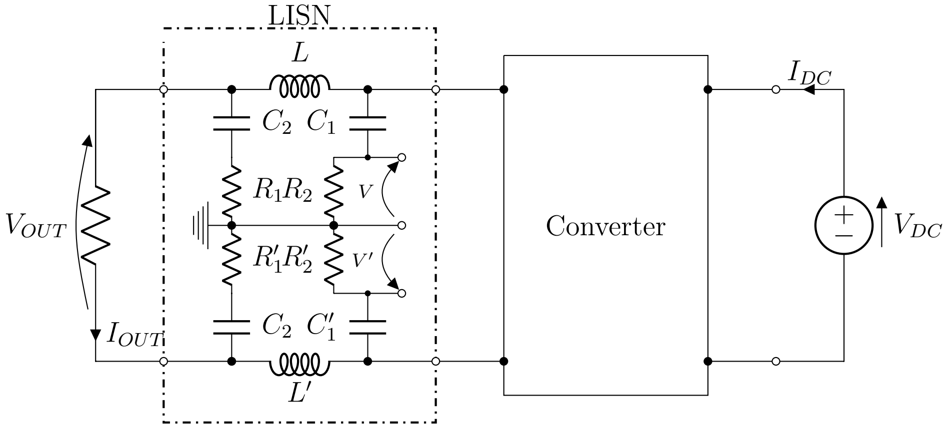
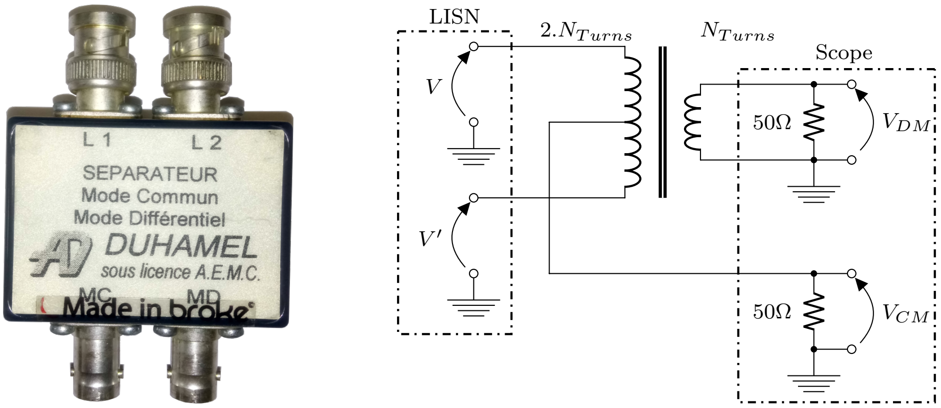


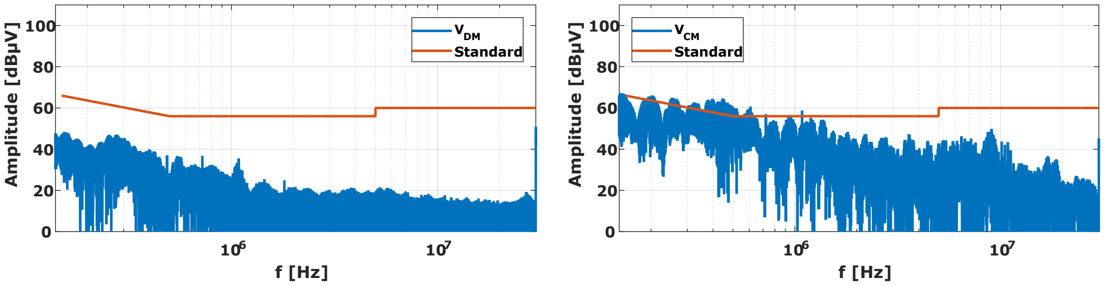
Figure 4.3.15: EMI measurements configuration



(a) Used device (b) Equivalent schematic

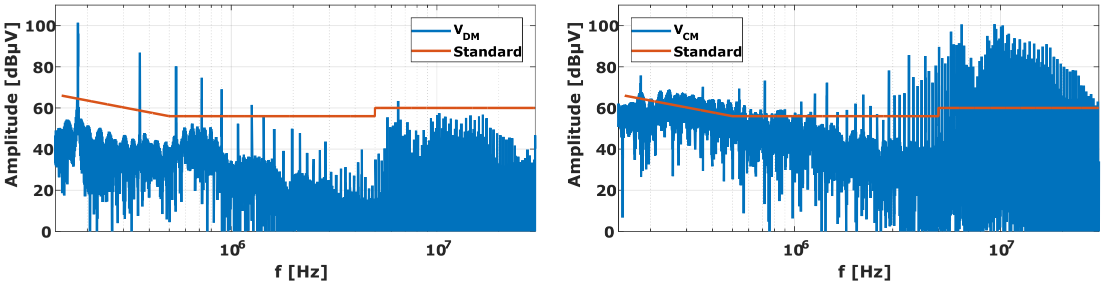
Figure 4.3.16: DM and CM noise separator device

EMI measurements were realised in DC/AC mode with LISN placed on the AC side, between the converter and the resistive load as illustrated in Figure 4.3.15. A Lecroy oscilloscope (HRO 12-bit) is used to measure the DM and CM voltages. The resistors R2 and R2' on the schematic are connected to 50 Ω inputs of the scope through noise separator. The noise separator presented in the Figure 4.3.16 is inserted between the LISN and the scope, it is used to physically separate differential mode and common mode perturbations. This equipment can speed up the design of EMI filter in the case of filters designed from measurements.



(a) DM voltage spectrum (b) CM voltage spectrum

Figure 4.3.17: DM and CM EMI measurements with standby converter



(a) DM voltage spectrum (b) CM voltage spectrum

Figure 4.3.18: DM and CM EMI measurements with operational converter

The differential mode and common mode voltages are directly visualised on the scope. The post-processing is then realised on Matlab. The FFT is performed on both signals to be compared to the standard. Two sets of measurements were realised. First, the converter is OFF, the measured DM and CM voltages depends on perturbation coming from the 24 VDC supply, the DSP used for control and the power supply maintaining the DC bus to 400 V. The results are presented in the Figure 4.3.17, these results correspond to the noise floor for next measurements realised with operational converter. The spectrum of the DM voltage is compliant with the standard. However, the difference between some harmonics and the limit is less than 20 dBµV, which should be the case for proper measurements. For CM voltage, some harmonics lower than 1 MHz are higher than the limit, impacting the measurement with the converter.

For the second set of measurements, the converter is operational and the same measurements are performed. The results are presented in the Figure 4.3.18. The combination of EMI perturbations from additional equipments and perturbations from the converter makes the whole system non-compliant with the standard. The first switching frequency harmonics are the most constraining for the differential mode. On the contrary, high frequency harmonics ($f > 1\,\mathrm{MHz}$) are the main issue for the common mode.

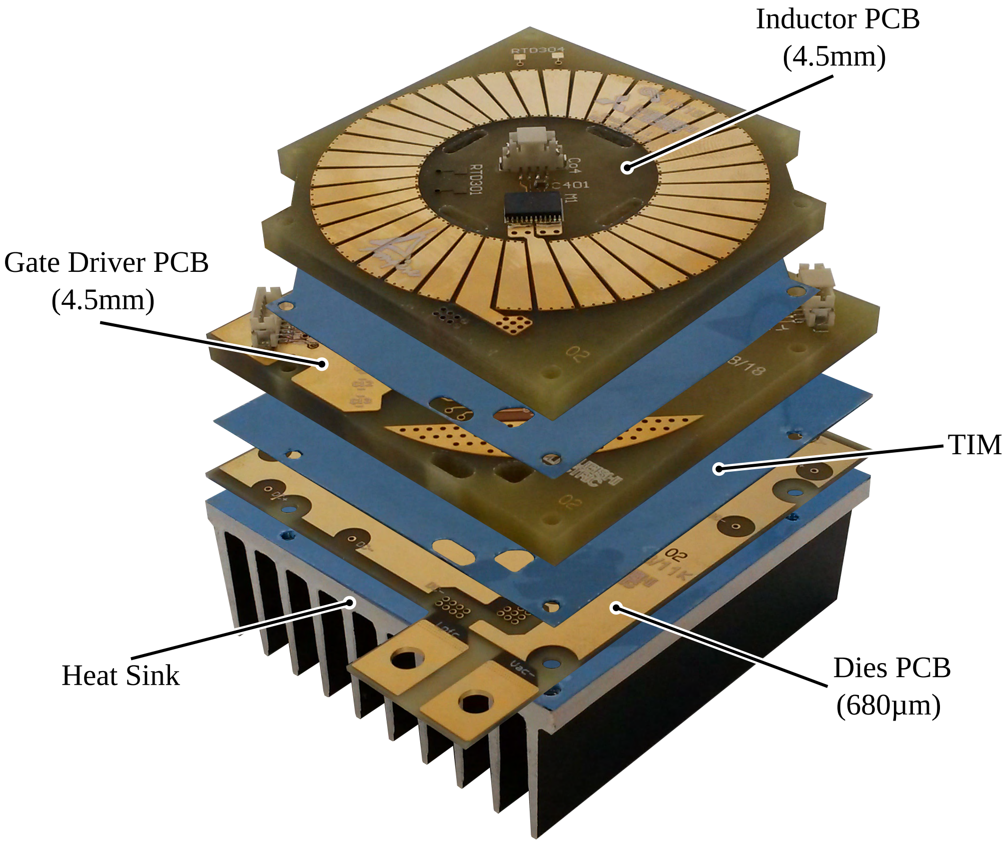
These major differences compared to analytical model or simulations are estimated coming from the test environment. Perturbations of the power DC supply are added to perturbations of the converter. Hence, the resulting spectrum is shifted up. The EMI filter design does not include all these perturbations, the attenuation of the built EMI filter is not sufficient. The filter has to be validated in AC/DC operation mode or by supplying the DC bus with a high voltage battery.

4.3.2 PCB Integrated converter

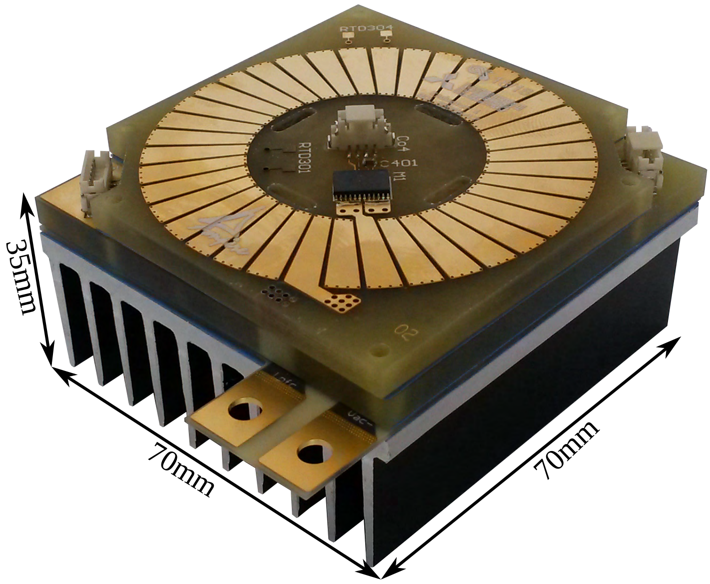
As aforementioned, the developed optimisation procedure is suitable for discrete and integrated converters. The discrete prototype has been presented in the sub-section 4.3.1. The discrete converter was built in a single PCB piece. The modular configuration is not particularly highlighted. However, this is much more relevant with the integrated version as several elementary cells can be interconnected to build the whole converter. One elementary cell is presented in Figure 4.3.19. The parallel association of four elementary cells corresponds to the complete optimised converter.

One cell is composed of three PCBs. One PCB of four 70 µm thick copper layers (after electroplating) for the low and high frequency dies, the overall thickness is 680 µm. One PCB for the gate drivers and the last one for the input inductor. These PCBs are 4.5 mm thick and composed of four 105 µm thick copper layers. More details about the stack-up and the PCB process are presented in Rémy Caillaud's thesis. In this case, the embedded toroidal inductor is used due its low profile. This kind of inductor is very interesting for stacked PCB design.

Like the discrete version, there are some differences between the optimisation results and the prototype. Figure 4.3.20 compares the elements used in the cells and the optimisation. The inductor mainly imposes the size of the cell as the dies and the gate driver are implemented in the same square boundary. The slight



(a) Exploded view



(b) Mounted cell

Figure 4.3.19: One elementary cell of the integrated PFC converter

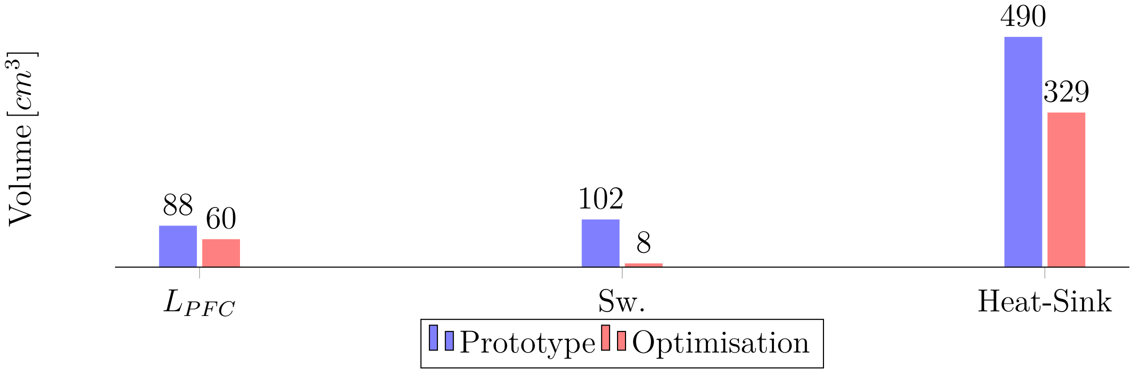


Figure 4.3.20: Volume comparison between Procedure and Integrated Prototype

difference of the realised inductor and the optimisation results come from the height of the PCB. In the optimisation procedure, the maximal PCB thickness is limited to a standard value of 3.2 mm. The volume of the switches and the gate driver are impacted by the PCB thickness and the inductor surface. Concerning the heat-sink, the height is also higher for the prototype. The equivalent thermal coefficient of 7 cm^3/W can be calculated using the volume and the calculated losses. The coefficient used in the procedure is 5 cm^3/W.

Two 65 mΩ 900 V SiC MOSFET in parallel were selected in the procedure, but the switches used in the prototype are only one 85 mΩ 1.2 kV SiC MOSFET. This is mainly due to low availability of desired bare dies and difficulties to get them metallised with thick copper. Of course this impacts the performances of the converter. However, the feasibility of such integrated converter is fully validated as all the embedded active components, including dies and gate driver circuit, are operational. The main issue of this stack-up comes from the embedded toroidal inductors. Some of the samples present core failures which may have happen during the lamination process. Even the samples with undamaged core show a strong increase in resistance with frequency, leading to high copper losses. Thus, this inductor cannot be used in nominal operation during a long time. More details about the involved phenomena are presented in Rémy Caillaud's thesis. Hence, to be able to fully test the integrated converter embedded toroidal inductor are replaced by planar inductors (see Figure 4.3.21).

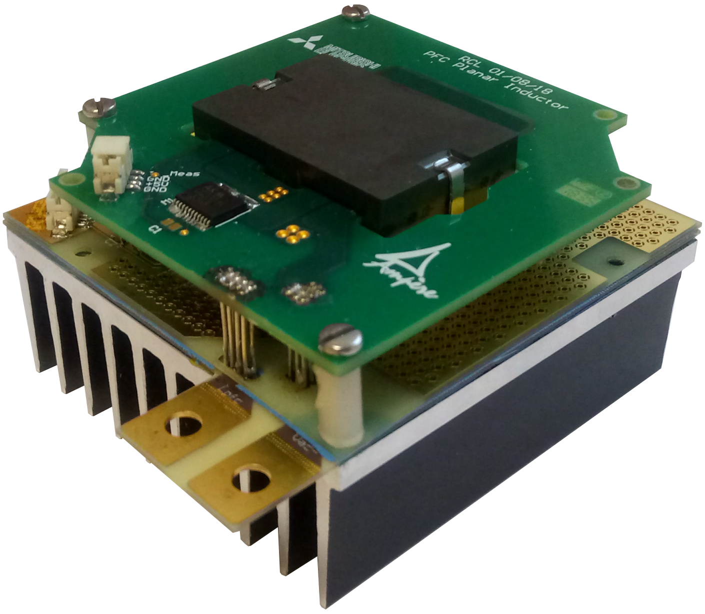


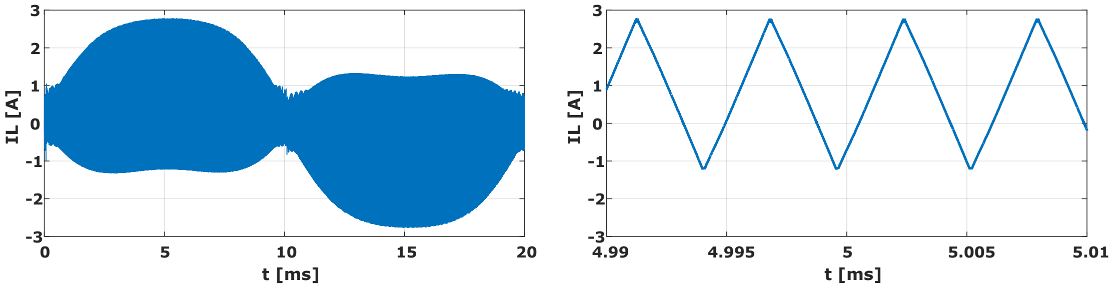
Figure 4.3.21: Integrated PFC cell with planar inductor

The overall volume of the integrated converter using the four interleaved cells and the new EMI filter (with planar inductors) is 1.5 L. Therefore, the achieved power density is 2.2 kW/L while the objective was 1 L leading to 3.3 kW/L. A new mechanical assembly could allow a power density close to the objective.

4.3.2.1 Power tests

The first operational tests performed on the integrated converter were at low power to validate the functionality of the different parts, e.g. embedded dies and embedded gate driver.

As for the discrete converter, DC/AC tests are performed. The first issue encountered is the difficulty to measure and visualise any signals. Indeed, high level of integration means limited signal access making the debugging very difficult. Unlike the discrete converter, power tests with the integrated converter led to more components breakdown. Several gate drivers became faulty during the tests. The issue appeared randomly with the increase in the DC voltage. Indeed, breaks did not happen at the same DC voltage. Even with further investigations, the phenomenon is still misunderstood. It can come from damaged components during



(a) Current at the grid frequency (b) Current at the switching frequency

Figure 4.3.22: Inductor current of the integrated converter at 100 V_{DC}

the manufacturing process or EMI issues. Therefore, power tests at nominal voltage and nominal power were not possible.

To keep operational cells, only tests at limited voltage and power were performed. The results presented in the Figure 4.3.22 are obtained under 100 V_{DC}. The inductor current waveform is very similar to the expected waveform. The current ripple is high enough to achieve ZVS as previously presented. Even if the operational conditions are curbed, it shows the feasibility of such converter, and the achievable compactness.

4.3.2.2 EMI filter evaluation

The new four stages EMI filter for the integrated converter is also realised with planar inductors (Figure 4.3.23) due to broken cores and inductance mismatch for the embedded toroidal inductors. The impedances are analysed to estimate the behaviour of the filter. These impedances are also compared to the initial model. The measures are realised with the same setup as previously. Figure 4.3.24 shows the input and output impedances. As for the two stage filter, the input impedance model fits with the measure until 5 MHz. The output impedance model does not fit as much as the input impedance. However, the measure presents better behaviour than expected with the model. Indeed, from 100 kHz to 10 MHz, the measured impedance is lower than the model. This means that the EMI filter presents a less resistive path for undesired harmonics. The increase in impedance due to parasitic elements, stray inductors, only appears at 4 MHz. The characteristics noted with

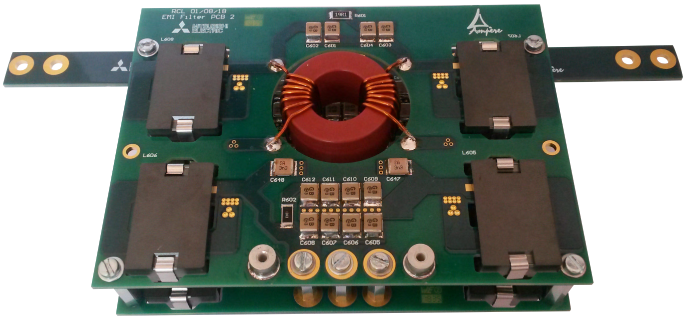
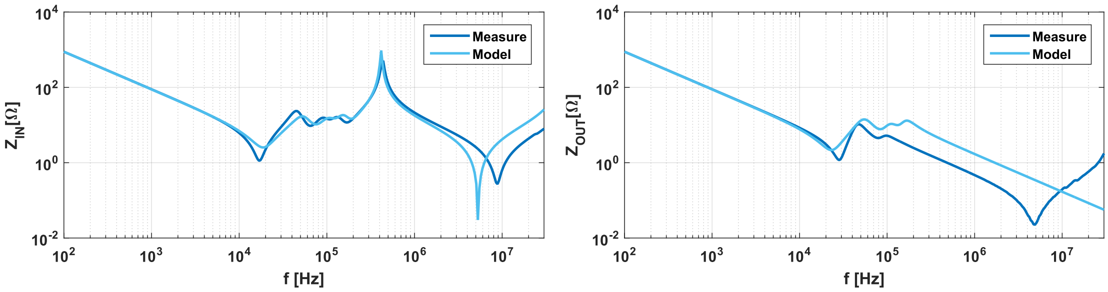


Figure 4.3.23: Four stage EMI filter with planar inductors



(a) Intput impedance (b) Output impedance

Figure 4.3.24: Four stages DM filter impedances

these measurements are largely better than the two stage EMI filter implemented on the discrete converter.

4.4 Conclusions

This chapter presents the results of the optimisation procedure introduced in the Chapter 3. First, the two considered conduction modes (CCM and TCM) were compared for non-interleaved converters. Analytical results obtained for the CCM converter were validated by PSIM simulations, particularly EMI behaviour. Results highlighted that in the studied configuration CCM proposes the best solution. Indeed, global losses and volume are smaller than converter operating in TCM, 97 % efficiency with 0.8 L compared to 93 % efficiency with 1.7 L, respectively. Thus, CCM is finally selected for the design of converters which include interleaving.

Two versions of an interleaved converter were presented. The first result comes from optimisation with off-the-shelf packaged semiconductors and planar inductors, which represents a first step in the PCB integration. The selected converter among all possibilities theoretically achieves 98 % efficiency and 5.5 kW/L power density. It includes four interleaved cells switching at 180 kHz and a two stage EMI filter. This configuration shows that all the semiconductors are operating in ZVS because of the high allowed inductor current ripple. Therefore, semiconductor losses can be kept low. The selected converter was also simulated on PSIM to validate the design of the optimisation procedure. The main drawback identified with this converter was the poor efficiency at light loads. To overcome this, cell shading was added in the integrated converter design, at the expense of a bigger EMI filter.

The integrated converter was also selected in the efficiency versus power density domain, among other converter designs based on embedded bare dies and inductors realised with embedded magnetic cores. The selected configuration is the same as for the discrete version, expected for the EMI filter which is composed of four DM stages and three CM stages. The expected efficiency and power density were 98 % and 5.41 kW/L, respectively. As for the discrete converter, semiconductors also operate in ZVS during a complete main period in the integrated version. These results highlighted the significance of soft-switching operation in highly efficient converters.

Both converters were built, first the discrete version then the integrated one. The discrete converter has been used for the first comparison with the optimisation procedure. The main difference was on the estimated volume versus the real volume. Indeed, the optimisation procedure does not include the volume of interconnections between components which represents an important part in the final design. This point is a main concern to improve the optimisation procedure. Instead of creating databases with different semiconductor references only, the database should includes different switching cells. These cells are composed of gate drivers (bootstrap, with isolated supply) and the semiconductors, the layout is known so the volume estimation is more precise.

Another improvement for discrete converter optimisation could be the limitation of the number of low frequency switches. Power tests realised on the discrete converter cannot be directly compared to the optimisation results because of several points. The first one is the low copper thickness selected to shorten the manufacturing delay. The second point concerns the faulty inductors replaced by wound planar inductors. Nevertheless, the full ZVS operation of semiconductors during a complete main period has been validated even with the mentioned issues. EMC measurements also presented some differences compared to expectations. This is explained by the use of complementary equipments impacting the measurements. The EMC compliance is expected in other operation conditions.

The integrated converter was mainly used to highlight the achievable compactness of power converter using PCB integration. The optimisation procedure can also be improved by including interconnections volume and PCB manufacturer design rules. Indeed, the main difference comes from higher PCB thickness for Gate drivers and PCB inductors. Major issue noted during the first tests realised on the integrated converter was on embedded inductors. On one hand, several samples had a broken magnetic core, certainly due to the lamination process. On the other hand, unaffected inductors present important mismatches in the values. This is most probably due to the position of the core in the cavity. Therefore, inductors with embedded core had to be replaced by planar inductors to guarantee good operation of the interleaved converter. Unfortunately, further investigations showed that the gate drivers made tests at nominal DC voltage impossible. Interleaved cells were tested under reduced voltage. The replacement of the gate drivers should be investigated to allow full power tests of integrated cells.

Chapter 5

Design methodology adapted for PPB

5.1 PPB topology for power density improvement

The main objectives of this project are high power density and power integration. As it is presented in the Chapter 1, dealing with the pulsating power in single phase PFC is important. The classical way uses Electrolytic capacitors which is not consistent with the high power density objective. Hence, the use of power pulsating buffer (PPB) is almost mandatory to overcome this issue. From the different topologies presented in the Chapter 1, the Buck solution is evaluated to be the most suitable solution for this project. Indeed, the required buffer capacitor is smaller than a symmetric topology. Moreover, same switches as the PFC can be used as they have to withstand the DC bus voltage, which is not the case with a Boost topology. Another important point is the similarity with the PFC topology. As for the PFC, the PPB is composed of two switches and one inductor at the mid-point. This corresponds to the elementary components in power electronics. The PFC optimisation procedure is simply adapted to the PPB topology. The global topology of a full bridge PFC associated to a buck PPB is illustrated in the Figure 5.1.1.

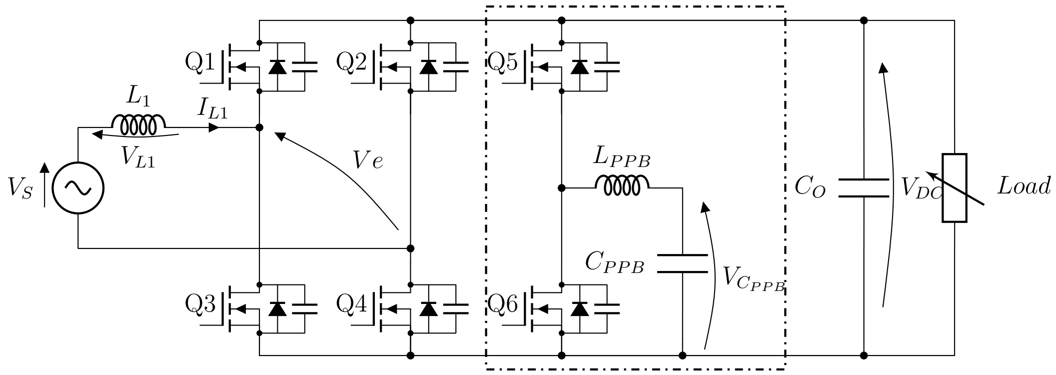


Figure 5.1.1: A full-bridge PFC stage with the considered PPB for pulsating power filtering

5.2 Adaptation of optimisation framework

As aforementioned the PPB optimisation procedure is similar to the PFC optimisation. It is composed of three parts, the semiconductor selection, the inductor design and the buffer capacitor design. Figure 5.2.1 presents the design flow-chart. The three optimisation variables are presented in the Table 5.1. At the end of the procedure, the assessment of losses allows the volume of the heatsink to be determined. This highlights the impact of the thermal management. The coefficient of 5 cm^3/W with natural convection is also considered. The thermal constraint are 60°C ambient temperature and a maximum device temperature of 125°C.

The identification of the optimisation variables is realised according to the application and the converter topology. For this case, the PPB is connected in

Table 5.1: Optimisation variables range for PPB

CCM
fsw = [40 kHz ; 280 kHz]
L_{PPB} = $[10\,\mu H; 80\,\mu H]$
$\text{V}_{PPB_{MIN}}$ = $[100\,V; 350\,V]$

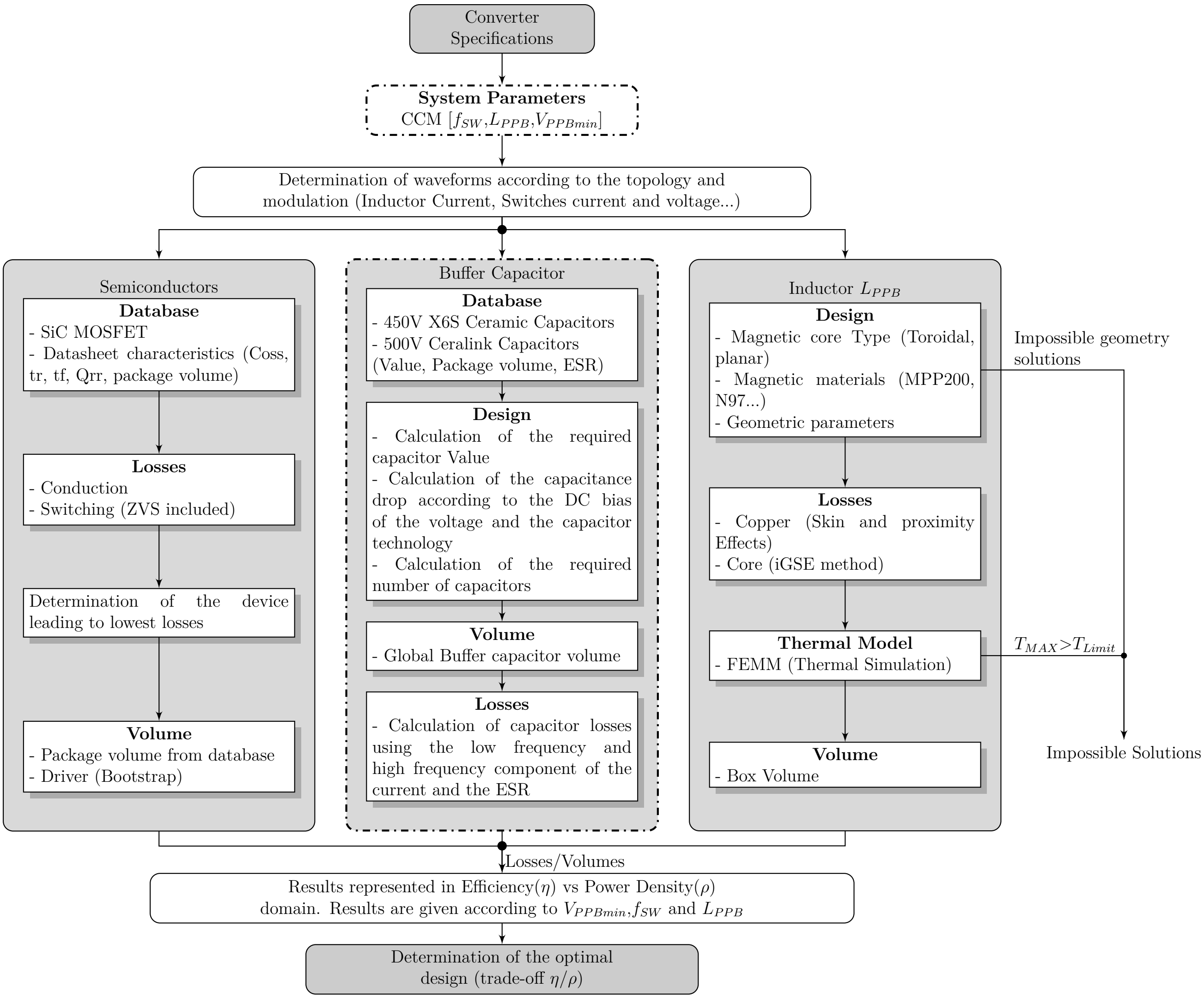


Figure 5.2.1: Design flow chart presenting the optimization procedure implemented for the Buck PPB. Dashed parts represent the changes compared to the PFC optimisation.

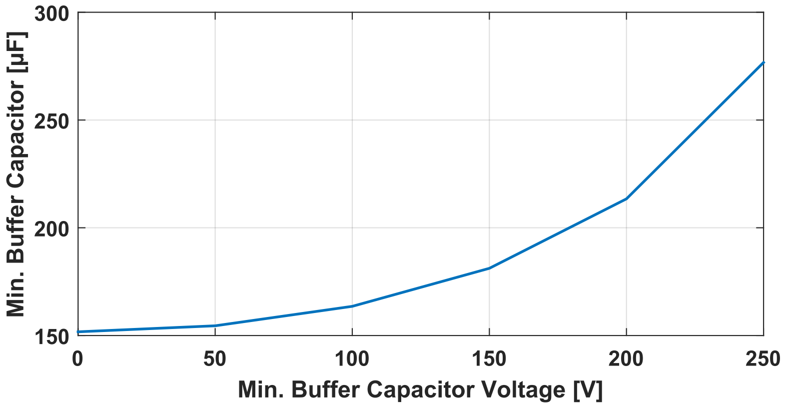


Figure 5.2.2: Buffer capacitor variation

parallel to a DC bus capacitor (Co) of only 20 µF, mainly used to filter the high frequency components. The DC voltage is assumed to be controlled by the rectifier stage to a value of 400V. For the optimisation procedure, the three variables are: the switching frequency ($\mathrm{f_{SW}}$) of the PPB, its inductor value ($\mathrm{L_{PPB}}$), and the minimum buffer capacitor voltage ($\mathrm{V_{PPBmin}}$). The inductor value impacts the current ripple. As it is highlighted in the Chapter 4, the current ripple impacts the conduction losses, but the switching losses can be drastically reduced if ZVS is achieved.

The buffer capacitor can be determined according to the maximal fluctuating power and the voltage swing. With the Buck topology, the buffer capacitor must be always lower than the DC voltage. Hence, the maximal buffer capacitor ($\mathrm{V_{PPB,max}}$) is set at $0.93 \cdot V_{DC}$ to prevent control issues. The minimal buffer capacitor voltage allows the capacitor value to be determined, see Equation 5.2.1.

$$C_{PPB} = \frac{2 \cdot P_{DC}}{\omega \cdot (V_{PPBmax}^2 - V_{PPBmin}^2)} \tag{5.2.1}$$

The variation of the required capacitance according to the minimal voltage is presented in the Figure 5.2.2. It shows that the capacitor values for minimum voltages ranging between 0 V and 100 V remain almost unchanged: $\mathrm{C_{PPBmin}} = 152$ µF and $\mathrm{C_{PPB}}(100\mathrm{V}) = 163$ µF. Consequently, the capacitor volume is almost equivalent for both cases. However, it is preferable to keep some energy stored in the capacitor, in the case of load variations. Moreover, the higher the voltage variation across the capacitor, the higher the current flowing through it. This current is also flowing through the inductor, which negatively affects the conduction losses.

Knowing the required buffer capacitance, the voltage waveforms can be determined. The voltage across the buffer capacitor is given by Equation 5.2.8 with "K" the security factor selected for the maximal capacitor voltage (in this case $K = 0.93$). Equation 5.2.8 is derived from the expression of the energy stored in the capacitor assuming an ideal behaviour of the PFC. The absorbed power of the PPB is equal to the pulsating power.

$$W(t) = W_{init} + \int P_{Puls}(t)dt \tag{5.2.2}$$

$$W(t) = W_{init} - P_{DC} \cdot \int \cos(2\omega t)dt \tag{5.2.3}$$

$$W(t) = W_{init} - \frac{P_{DC}}{2\omega} \cdot \sin(2\omega t) \tag{5.2.4}$$

$$W_{max} = W_{init} + \frac{P_{DC}}{2\omega} \tag{5.2.5}$$

$$W_{init} = \frac{1}{2} \cdot C_{PPB} \cdot V^2_{PPB,max} - \frac{P_{DC}}{2\omega} \tag{5.2.6}$$

$$W(t) = \frac{1}{2} \cdot C_{PPB} \cdot V^2_{PPB}(t) = \frac{1}{2} \cdot C_{PPB} \cdot V^2_{PPB,max} - \frac{P_{DC}}{2\omega} \cdot (1 + \sin(2\omega t)) \tag{5.2.7}$$

$$V_{PPB}(t) = \sqrt{(K \cdot V_{DC})^2 - \frac{P_{DC}}{C_{PPB} \cdot \omega} \cdot (1 + \sin(2\omega t))} \tag{5.2.8}$$

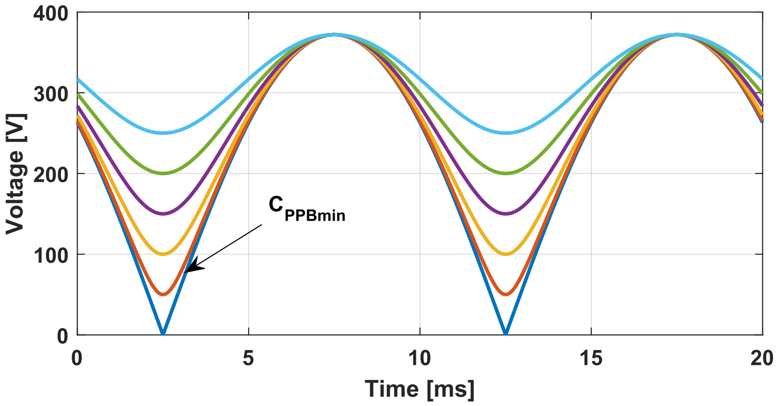


Figure 5.2.3: Buffer capacitor voltage waveforms

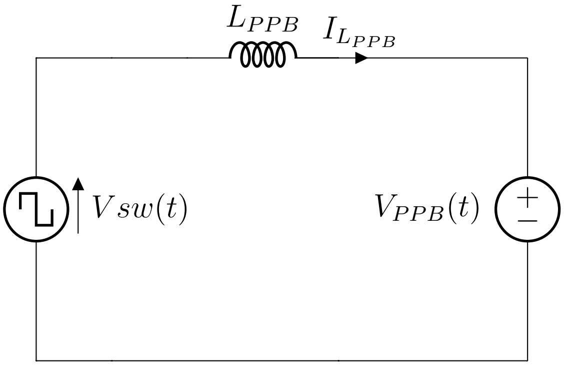


Figure 5.2.4: Simplified circuit of the PPB converter.

The Figure 5.2.3 presents the voltage waveforms for different capacitor values. The buffer capacitor voltage is then used to calculate the inductor current with the same method presented in the Chapter 3 where the grid voltage is replaced by the buffer capacitor voltage. The corresponding simplified schematic is presented in the Figure 5.2.4. The switch voltage is controlled according to buffer capacitor equation normalised to the DC voltage, see Equation 5.2.9. The mesh law allows the inductor voltage to be determined, the current is then calculated in the frequency domain (results of are presented in the Figure 5.3.3).

$$\alpha_{PPB}(t) = \frac{1}{V_{DC}} \cdot \sqrt{(K \cdot V_{DC})^2 - \frac{P_{DC}}{C_{PPB} \cdot \omega} \cdot (1 + \sin(2\omega t))} \tag{5.2.9}$$

5.2.1 Semiconductor selection

The selection of the suitable semiconductor is done among a database of SiC bare dies. As for the PFC, the volume of a die is negligible compared to the volume of the heat-sink required to dissipate the losses of the same die. Therefore, the semiconductor devices are selected solely on the criterion of losses minimisation. Both conduction and switching losses are taken into account. Conduction losses are calculated considering the on-state resistance at 150°C (extracted from the manufacturer's datasheet) and the RMS current value. Regarding the switching losses, datasheet parameters (tr: rise time, tf: fall time, Coss, Qrr) are also used and a simple analytical model is developed to facilitate the comparison between devices. The turn-ON and turn-OFF energies are reminded by Equations 5.2.10 and 5.2.11, respectively. As the buck topology can achieve soft-switching, all commutations are analysed to identify if they lead to hard or soft switching. The necessary conditions to achieve soft-switching, in particular the impact of the inductor current ripple, are explained with more details in the Chapter 3.

$$Esw_{ONx} = \frac{1}{2} \cdot V_{DC} \cdot I_{Dx} \cdot tr + \frac{1}{2} \cdot Coss \cdot V_{DC}^2 + Qrr \cdot V_{DC} \tag{5.2.10}$$

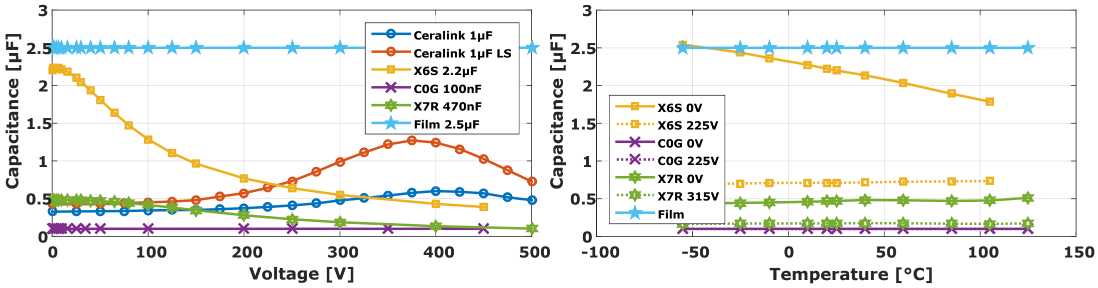
$$Esw_{OFFx} = \frac{1}{2} \cdot V_{DC} \cdot I_{Dx} \cdot tf \tag{5.2.11}$$

5.2.2 PPB inductor design

The two previously presented inductor technologies, planar and PCB-embedded toroidal, are compared for the PPB application to highlight their impact on losses and power density. The methodology is the same as for the PFC. A geometry variation is realised to fulfill the inductor value requirement. Then, the losses are calculated according to the current waveforms. This includes copper and core losses as presented in the sub-section 3.5.2. The main difference between the PFC and the PPB is the current waveform. The PFC uses interleaving techniques, so the average current value in the inductors is lower than for the single-stage PPB presented in this chapter. In fact, the average current, pulsating at twice the grid frequency, depends on the capacitor voltage swing. The higher the voltage variation the higher the current. Hence, high frequency current ripple needs to be higher in the PPB to achieve the full ZVS operation. Therefore, the losses are mainly driven by the voltage swing and the inductor value.

5.2.3 X6S ceramic capacitors for pulsating power buffering

The buffer capacitor represents an important part of the PPB. It is mandatory to evaluate several types of capacitors, and find the most suitable according to the power density and integration objectives. The three main types of capacitor are, electrolytic, film and ceramic. The first type is known for its low reliability [63].



(a) Variation according to the DC bias (b) Variation according to the temperature

Figure 5.2.5: Analysis of capacitance variations. The typical curves are given for a DC voltage corresponding to the half of the voltage rating which depends on the reference

Electrolytic capacitors tend to be replaced by other technologies. Moreover, electrolytic capacitors has a quite poor low frequency current capability. This is against the PPB operation principle as the voltage swing should be limited with such capacitor technology. The two other types, film and ceramic, are more suitable for such applications [69][71]. Both have their advantages and drawbacks. However, the comparison can be complex as the ceramic family can be sub-divided according to the dielectric material used in the manufacturing. Each material impacts the maximal capacitance, the maximal voltage rating, the capacitance variation, the thermal behaviour. The capacitance for ceramic widely depends on the DC voltage applied and the temperature, contrary to film capacitors which are constants. The Figure 5.2.5 presents the capacitance variation of several types of capacitors (film, Ceralink, X6S, C0G, X7R) according to the temperature and the DC bias. All the capacitors are picked from the same manufacturer (TDK). They are compared according to their respective datasheet.

Focusing on the impact of the DC voltage, it is possible to notice that film capacitor value stay constant. It is also the case for C0G. However the maximal capacitance is quite low with this material at this voltage rating. X6S and X7R ceramic capacitors present a drop in the value when the DC bias increases. It can represent a lost of more than 75% of the initial value. The last type of capacitor, the Ceralink, presents the opposite behaviour: the capacitance increases with the DC bias. This is particularly interesting for DC bus application. Moreover, two

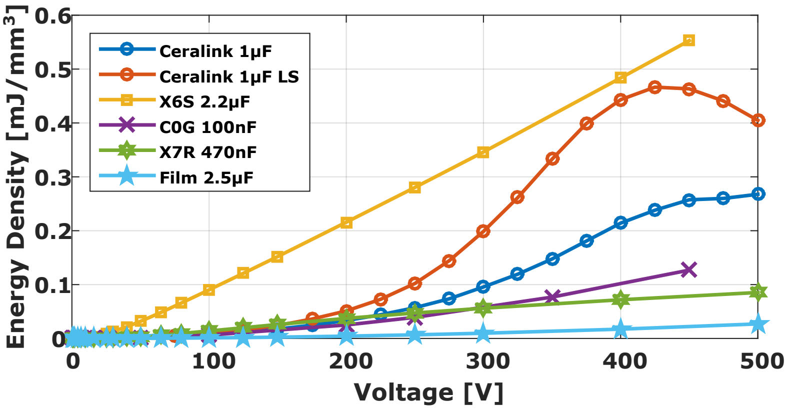


Figure 5.2.6: Analysis of energy densities

capacitance curves are presented in the datasheet. The first one corresponds to the classical "Small Signal" test, a DC voltage with a superimposed AC voltage of 0.5 V_{RMS} at 1 kHz is applied. For the second one, the "Large Signal" test is realised. The superimposed AC signal varies at low frequency. These test conditions correspond to the conditions of operation of the PPB. Hence, this particular behaviour is very interesting. It is due to the employed material, CeraLink capacitors are made with lead-lanthanum-zirconate-titanate (PLZT) ceramic. The datasheet gives two capacitor values. The nominal value that is 1 µF and the effective value that is 0.6 µF. All curves presented below are related to the effective capacitor value.

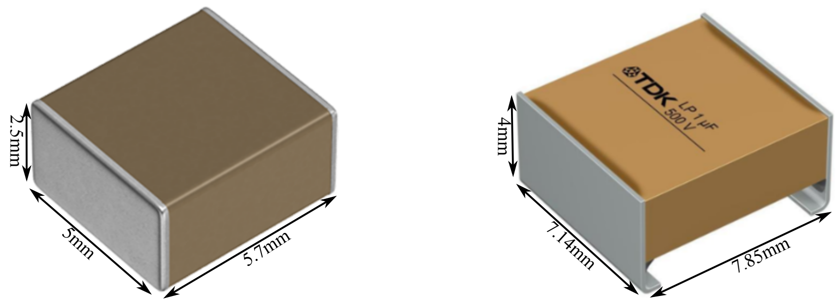
As mentioned above, the ceramic capacitor value also depends on the temperature. The Figure 5.2.5 highlights that the impact of the temperature can be neglected compared to the impact of the DC bias across the capacitor. Indeed, the DC bias induces a significant capacitance drop.

The capacitance variation is a key parameter because it directly impacts the design. However, the different capacitor types need to be compared in terms of energy density. With the power density and integration objectives, the most suitable capacitor corresponds to the smallest one with the highest capability to store energy. Hence, for this comparison, the impact of the DC voltage is taken into account. Figure 5.2.6 presents the calculated energy density stored in each capacitor for different DC voltages with the respective capacitance. The "small signal" and "large signal" characteristics of the Ceralink are also investigated.

One can clearly see that the film technology presents the poorest density when it is compared to Ceramic. Even if the capacitance is constant, the box volume is large. The two most interesting candidates for the PPB application are the X6S (C5750X6S2W225K250KA) and the Ceralink (B58031U5105M062) especially with the "large signal" variation. In spite of this interesting capacitor increase characteristic, the Ceralink is disadvantaged because of its technology and package using leads (see Figure 5.2.7). The leads added to capacitor are used to reduce the mechanical stress on the capacitor. Ceramic capacitors are known to have a strong piezoelectric behaviour [85]. The capacitor can vibrate and create acoustic noise, the leads can also be used to reduce this undesired effect.

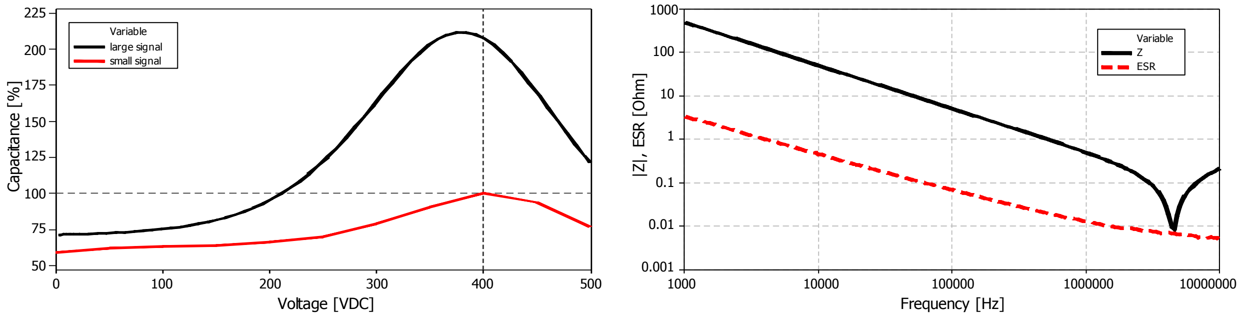
To be used in the optimisation procedure the two capacitors need to be modelled. As for the semiconductor, the capacitor models are only based on the manufacturer datasheet to facilitate the pre-design and the comparison between the two technologies. The variation of the capacitance according to the DC voltage and the variation of the ESR are mandatory to calculate the number of capacitors required and evaluate the losses, respectively. For the Ceralink, the large signal variation is selected as it corresponds to the application. The two main characteristics used in the model are presented in the Figure 5.2.8 and come from the datasheet [86].

In both cases, Ceralink and X6S, the capacitance variation in the full voltage range [0V ; 450V] is estimated with a 7th order polynomial fit (cf appendix C.1). The different parameters according to the technology are specified in the Table C.1. The calculated losses for the buffer capacitor are only conduction losses. The



(a) C5750X6S2W225K250KA (b) B58031U5105M062

Figure 5.2.7: Selected capacitor packages



(a) Capacitance variation

(b) ESR

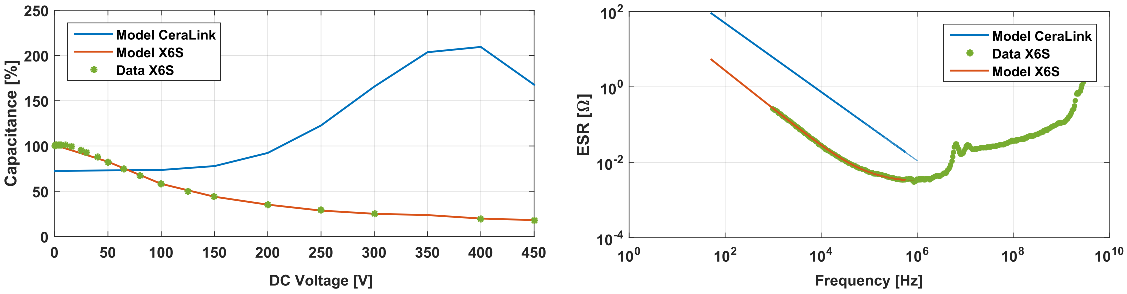
Figure 5.2.8: Ceralink capacitor behaviour from datasheet

current flowing through the capacitors is composed of a low frequency component corresponding to pulsating power, and high frequency components corresponding to the switching frequency. Hence, the corresponding losses are calculated according to the ESR value for the two main frequency components. The considered frequency range is 50 Hz to 1 MHz which is largely sufficient for the PPB application with a switching frequency lower than 500 kHz. Usually in datasheets, the frequency range starts at several kilo-Hertz and ends at several Mega-Hertz. Thus, the low frequency behaviour needs to be extrapolated from available data. The ESR variation for the Ceralink capacitor can be considered linear in a logarithmic graph in the selected frequency range, the estimation of the ESR is calculated with Equation 5.2.12. The ESR for X6S capacitor is not linear along the complete range and the linear approximation is not sufficient to estimate the ESR at the switching frequency. Consequently, the X6S ESR is modelled with a power approximation, see Equation 5.2.13.

$$ESR_{CeraLink} = 10^{(-0.911 \cdot \log(F) + 3.511)} \tag{5.2.12}$$

$$ESR_{X6S} = 285.9 \cdot F^{-1.011} + 0.00296 \tag{5.2.13}$$

All the models are presented in the Figure 5.2.9. The data for X6S, available on the manufacturer website, are directly compared to the model. Both are fitting well the variation of the capacitor and the ESR. The designed ESR model including



(a) Capacitance model (b) ESR Model

Figure 5.2.9: X6S and CeraLink models implemented in the design procedure.

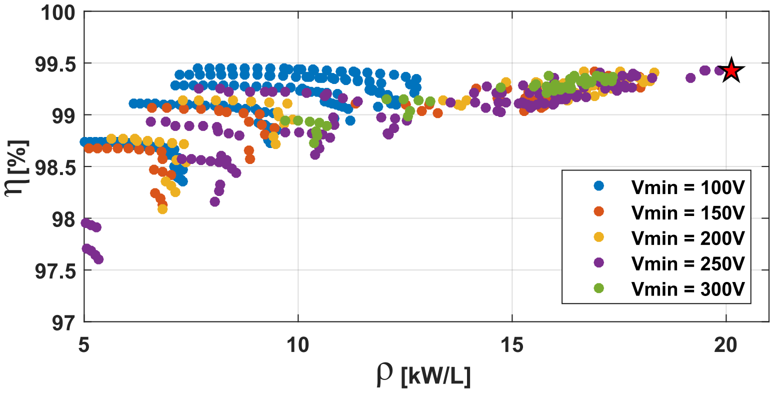
the extrapolation is used to compare the low frequency behaviour of the two technologies. Another drawback of the Ceralink is the high series resistance at low frequency. In the case of the PPB, the current flowing through the buffer capacitor is mainly pulsating at twice the main frequency, so, low-frequency ESR is a very important parameter to reduce losses. The same conclusion was also reached in [87]. Hence, the high energy density and the low frequency ESR make the X6S the most suitable technology to implement in the PPB application.

5.3 Optimisation framework results

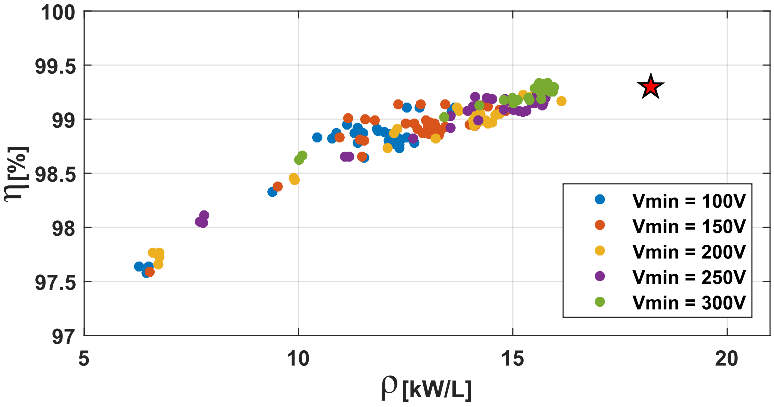
As for the PFC, several converter configurations are evaluated and the results are presented in the power density (ρ) vs efficiency (η) domain. The equivalent efficiency is calculated according to the input power of the PFC ($\mathrm{Pin_{PFC}}$) and the calculated losses of the PPB ($\mathrm{P_{PPB}}$), see Equation 5.3.1.

$$\eta_{PPB} = \frac{Pin_{PFC} - P_{PPB}}{Pin_{PFC}} \tag{5.3.1}$$

The design is realised at rated power. That corresponds to the highest current flowing through the semiconductors and passives. The results for the two possible combinations are presented in the Figure 5.3.1. The first one corresponds to X6S capacitors associated to planar inductor “X6S-planar”. The second one is the combination of X6S capacitors and PCB-embedded inductor, “X6S-PCB-embedded toroidal”. Both are presented with the same $5\,\mathrm{cm^3/W}$



(a) X6S capacitor/planar inductor with a thermal coefficient of 5 cm^3/W.

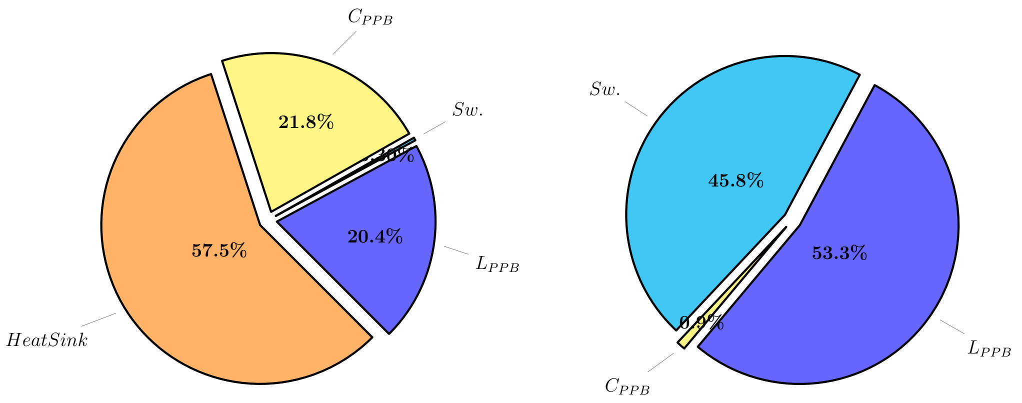


(b) X6S capacitor/PCB-embedded toroidal inductor with thermal coefficient of 5 cm^3/W.

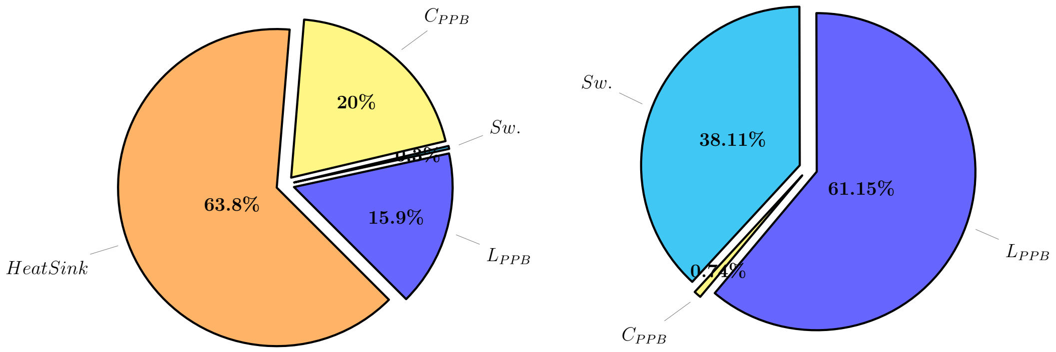
Figure 5.3.1: Results of the optimisation presented in the Power Density vs. Efficiency domain.

thermal coefficient. The impact of the minimum buffer capacitor voltage is depicted. The highest the voltage swing, the highest the buffer capacitor current, but the smallest the capacitor bank. Therefore the selection of minimal capacitor voltage corresponds to a trade-off between the size of the capacitor bank and the global losses. The switching frequency and the inductor value can be seen as optimisation variables that are used in trade-off between losses, mainly in the semiconductor and the inductor, and the volume of the inductor.

The two selected converters, with the two PCB inductor technologies, correspond to the densest solutions as the estimated efficiency is high, superior to the minimal



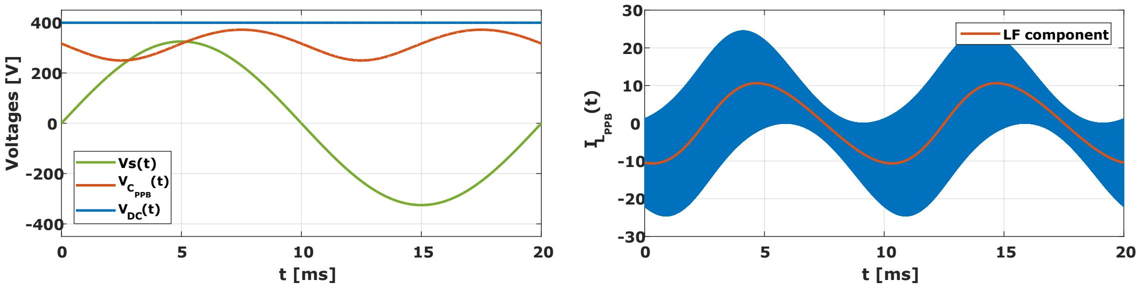
(a) Volume Planar (b) Losses Planar



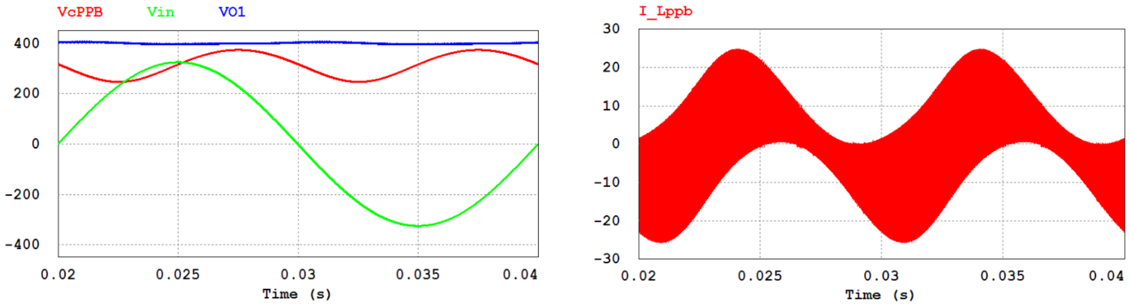
(c) Volume PCB-embed. (d) Losses PCB-embed.

Figure 5.3.2: Volumes and losses repartition for the PPBs

criteria chosen for the PFC (98 %). The two solutions achieve 99.45 % efficiency, 20.12 kW/dm^3 power density and 99.3 %, 18.22 kW/dm^3 for the planar and the PCB-embedded toroidal, respectively. The optimum is the same in both cases, the minimal voltage is equal to 250 V, so the buffer capacitor is equal to 277 µF, the inductor value is 20 µF and the converter switches at 140 kHz. The repartition of volumes and losses are analysed in the Figure 5.3.2 for both cases. Analysing the losses repartition, the losses generated by the buffer capacitor is negligible compared to semiconductors and inductor. This is one of the advantages of using ceramic capacitor with very low ESR. The work presented in [87] allows the losses to be calculated in such a capacitor by polynomial approximation and gives 0.11 W for the selected buffer capacitor in the same conditions. The polynomial equation come from experiment: a DC voltage with a superimposed AC signal is applied to



(a) Voltages Matlab (b) Current Matlab



(c) Voltage PSIM (d) Current PSIM

Figure 5.3.3: Voltages and current waveforms

the capacitor. Hence, the calculated losses only corresponds to low frequency losses. The losses calculated here are equal to 0.17 W and are based on the separation of the low and high frequency components of the current. The slight difference is due to the impact of the HF component. Therefore, more precise losses estimation are realised by separating the different frequency components. The main difference between the two PPBs comes from the inductor. The PCB-embedded toroidal is smaller than the planar however the losses are higher. Thus, the thermal management is badly impacted and make the PCB-embedded solution more bulky than the planar.

To validate the theoretical method implemented in the Matlab procedure, the selected optimised converter is simulated using the PSIM software. In the PSIM simulations, the capacitor value is kept constant to 277 µF as the non-linearity behaviour is not included. The voltage and current waveforms can be compared in the Figure 5.3.3. With this comparison, the analytical model developed in Matlab is fully validated by circuit simulations. With the selected PPB, the DC bus voltage

Table 5.2: Results Comparison. Includes only box volumes

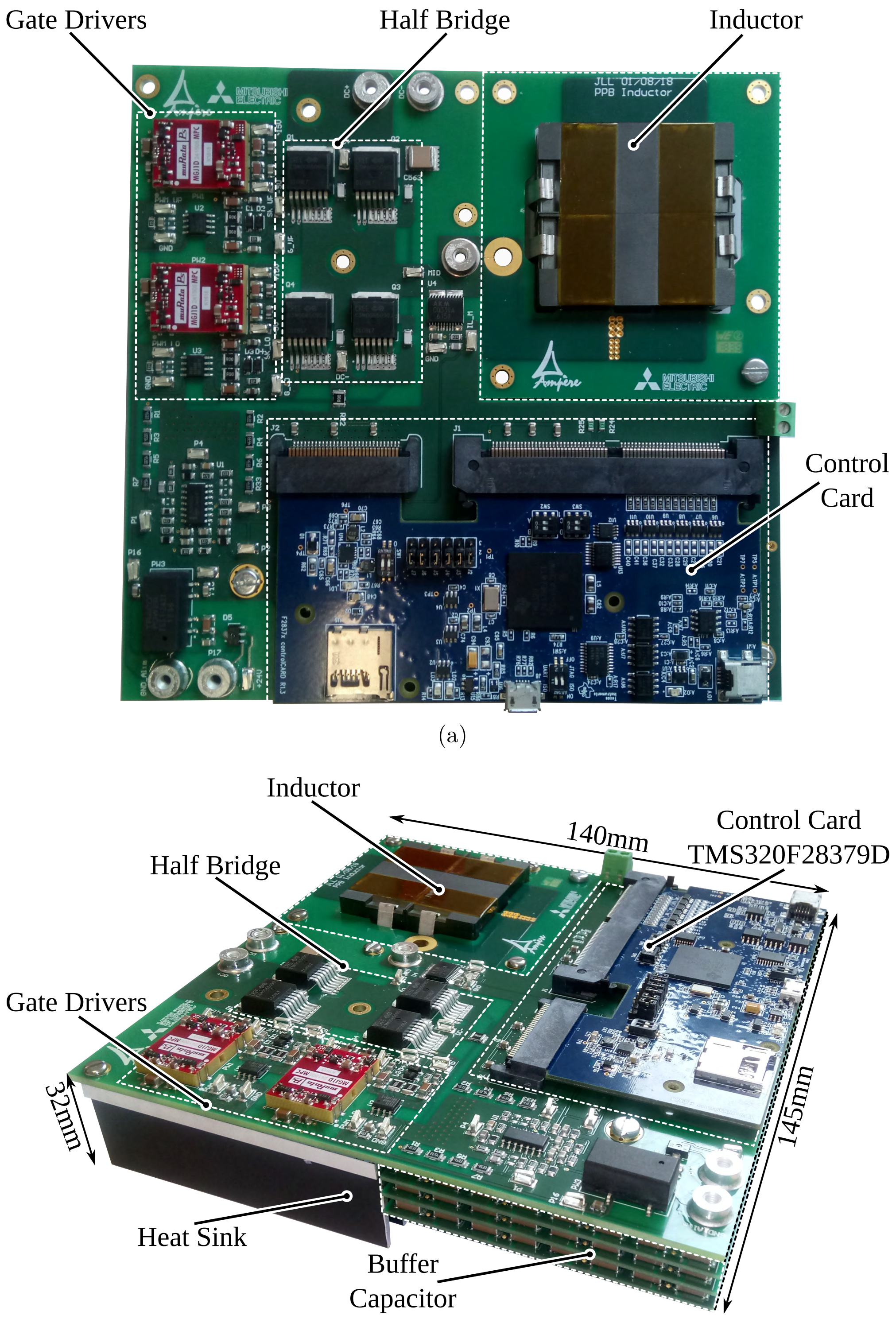
		PPB Planar	PPB PCB-emb.	Electrolytic
General	η	99.45 %	99.3 %	99.8 %
	ρ	20.12 kW/dm^3	18.22 kW/dm^3	3.5 kW/dm^3
	f_{SW}	140 kHz	140 kHz	-
	L_{PPB}	20 µH	20 µH	-
	Devices	SiC	SiC	-
	C_{PPB}	277 µF	277 µF	2.6 mF
Volume	Total	167 cm^3	181 cm^3	935 cm^3
	L_{PPB}	34.04 cm^3	28.72 cm^3	-
	C_{PPB}	36.40 cm^3	36.40 cm^3	935 cm^3
	Switches	0.505 cm^3	0.505 cm^3	-
	Heat sink	96 cm^3	115.45 cm^3	-
Losses	Total	19.2 W	23.09 W	6.5 W
	L_{PPB}	10.23 W	14.12 W	-
	Switches	8.8 W	8.8 W	-
	C_{PPB}	0.17 W	0.17 W	6.5 W

ripple is only $\pm 5\,V$ with only 20 µF on the DC link. The required electrolytic capacitor to achieve the same performance is estimated to 2.6 mF which is a very high value. A more detailed comparison between the two PPB and the classical electrolytic solution (using 47µF B43544B7476M000 from Epcos) is presented in the Table 5.2. It shows that the electrolytic capacitor generates less losses than the PPB (thus requiring no cooling system at all). However, the power density (ρ) of the PPB is much higher than the Electrolytic solution because the required capacitor value to reach the same performances is high. The efficiency for the electrolytic capacitor is calculated with the same method as the PPBs.

The same configuration (f_{SW}, L_{PPB}, $V_{PPB_{MIN}}$) for the two PPB is obtained at the end of the optimisation. It is noticeable that the selected configuration tends to limit the current flowing through the inductor and the capacitor to reduce losses by keeping a reasonable minimal voltage value. Moreover, analysing the current waveform, it can be concluded that the inductor value and the switching frequency are selected to have sufficient current ripple to achieve ZVS during the complete main period. The optimisation procedure implemented for highly integrated converter is favourable to soft-switching operation. This is an original result compared to the existing literature, in which the PPBs operating at a fixed switching frequency does not achieve ZVS the complete main period. With this two converter designs, the PFC and the PPB, the importance of soft-switching in highly integrated converter is highlighted, particularly with natural convection cooling.

5.4 PPB converter evaluation

The prototype of the optimised Planar PPB is built. Unfortunately due to the lack of time and quite long manufacturing delays, the prototype does not include PCB embedded components. Moreover, due to technical issues encountered with the gate driver implemented on the PFC another structure is implemented. It includes isolated power supplies from Murata (MGJ1D241505MPC) and high speed buffers from Silicon Lab (SI8271BB-IS). Higher robustness is expected, but the global volume is higher. The converter implementation is presented in the Figure 5.4.1. The analysis of the volume of the prototype compared to the procedure is presented in the Figure 5.4.2. All the parts included in the procedure show a bigger volume in the prototype. The main difference concerns the dies, indeed the use of packaged semiconductors and another gate driver structure widely impacts the results. The inductor is bigger because of the use of discrete cores which have slight differences in the dimensions, especially the height. The interconnections between the inductor, the main board and the capacitor also increase the volume. The buffer capacitor is composed of three stacked PCBs. Hence, the thickness of each PCB increases the volume. The optimisation procedure only sums the component volumes. With this realisation, the capacitors are not stuck to each other. Free space is added to facilitate the placement and the soldering process. Soldering all the capacitors together to form a one piece block is possible but quite complicated, and also make the interconnection to other parts of the converter harder. The PCB solution is the fastest and reliable option. The selected heat-sink is also bigger than expected. Indeed, choice of heat-sinks with sufficient base plate



(a)

(b)

Figure 5.4.1: Power Pulsating Buffer prototype

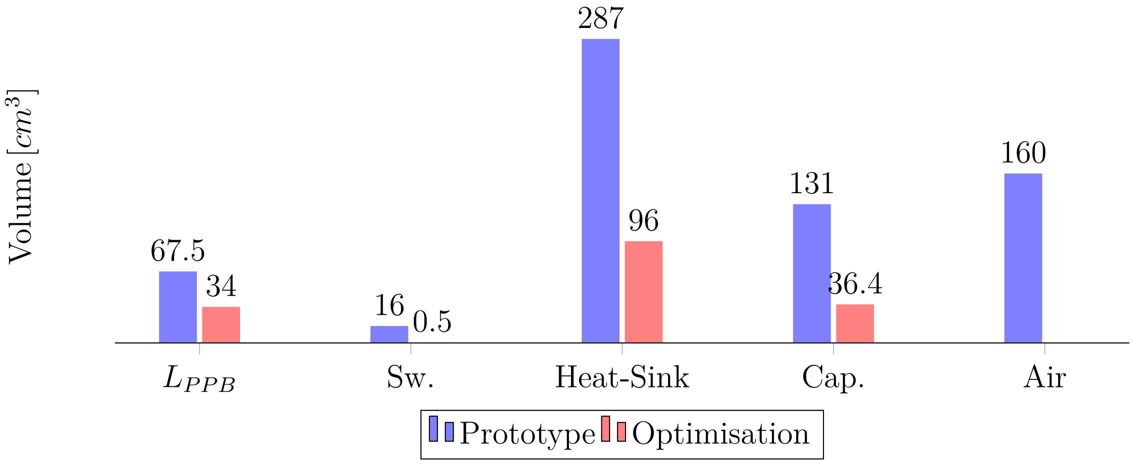


Figure 5.4.2: Volume comparison between Procedure and the PPB Prototype

thickness, for machining operation, associated to wanted fin length is impossible in standard reference. Therefore, the selected heat-sink has longer fins than expected leading to bigger volume.

5.5 Conclusions

The overall volume of power converters is mainly impacted by the passive components, inductors and capacitors. In AC/DC applications the classical method to filter the pulsating power is the use of electrolytic capacitors. However, this capacitor technology is limited by its current capabilities. To overcome this limitation, the capacitor bank can be increased to handle the current but the volume drastically raises. The scientific community also points at the poor reliability of these components. Therefore, another solution is required when the power density and power integration are the main objectives.

The integration of power pulsating buffer is a promising and efficient solution to enhance the power density of converter as it is highlighted when looking the Google little box challenge. This chapter discusses the optimisation and design of a buck power pulsating buffer. This topology is selected because of its good performances and low capacitor requirements. Moreover the PPB topology is very close to the PFC topology. That follows the concept of elementary cell design. It is confirmed by the simple adjustment realised on the PFC optimisation procedure. Semiconductor selection and inductor design is the same as previously. The main difference concerns the buffer capacitor design.

For this part of the converter, film capacitors are commonly used. However, the comparison presented in this work highlights the benefit to use ceramic capacitors. The density is substantially higher than film and the losses are lower due to low ESR of the package. The selection of the right ceramic capacitor is important. Two ceramic capacitor technologies, X6S and Ceralink, are compared to identify the most suitable one. The simple and fast modelling of the capacitance variation based on the datasheet highlights the highest density of the X6S technology. On the other hand, the ESR model, also based on the datasheet, shows the high series resistance of the Ceralink. Thus, the most suitable ceramic capacitor is the X6S on both characteristics, density and losses, that are very important when talking about power integration. Moreover, the impact of the different frequency components present in the buffer capacitor current are included. Indeed, results obtained with the proposed model are close to experimental results of the literature which only includes the low frequency aspect.

This chapter allows the two PCB inductor technologies to be compared for such applications. The planar presents the best solution as the calculated losses are lower than the PCB-embedded toroidal. The optimisation procedure is adapted for highly integrated converter. It is shown in previous chapter that soft switching is very important to achieve dense and efficient converters. This trend is also observed in this chapter. Firstly, the minimal buffer capacitor voltage is maintained to the value corresponding to the best trade-off between capacitor volume and low frequency conduction losses. Secondly, the selection of the inductor value and the switching frequency is mainly drove by the capability to achieve ZVS. As a consistent point, the optimised PPB achieves soft switching for a complete main period. Thus, the semiconductor losses are kept low, so effort on the thermal management can be reduced. This is particularly relevant for natural convection cooling.

The overall volume of the prototype is bigger than expected. The optimisation procedure only includes component volume explaining this difference. Moreover, the PCB integration is not implemented in this case, mainly because of long manufacturing delays. Despite using packaged components the PPB prototype achieves 4 kW/L power density for a 3.3 kW power converter. The overall box volume is equal to 825 cm^3. It is 110 cm^3 lower than a classical electrolytic capacitor bank, for equivalent voltage ripple on the DC link. This performance can be substantially enhanced. Indeed, the use of evaluation board for the control is not an optimal solution in terms of volume as lot of features of the board are not used and could be removed. Moreover, PCB integration with die embedding can reduce the volume. Due to lack of time, the prototype needs to be fully tested to evaluate its efficiency. Losses are expected to be higher than the electrolytic capacitors as additional active and passive components are used in PPB. All the calculated, then simulated, waveforms need to be experimentally validated.

As for the PFC design, the main lack of this procedure is the mechanical integration. The volume estimation can be more precise if the interconnections and PCB assembly are taken into account. This represents a major, but complex, improvement for future work and represents a first step to prototype design by using elementary blocks.

Chapter 6

Conclusion and perspectives

As presented in the Chapter 1, the actual economical and environmental context impose to reinforce the use of green electrical sources. To take full advantages of this trend, the performances of electrical facilities must be improved. Power electronic systems play an important role. The research community works on the reduction of power converter volume while high efficiency must be maintained.

To reach these objectives, the actual project focuses on 3D integration using PCB embedding to reduce interconnection volume and enhance the performances. Moreover, the PCB process can be automated and suitable for mass production. The embedding of active components is mastered and benefits are well known. The reduction of losses and EMI perturbations is possible due to the reduction of parasitics brought by the PCB embedding process. These improvements were noticed with the design of integrated power modules. However, the integration of large passives, e.g. magnetic components, is still challenging. Several research teams are investigating this topic. Indeed, combination of embedded active and passive components taking place in a fully integrated converter design is foreseen as a very efficient method.

Power converter design requires multi-objective optimisation to meet the specifications. Optimisation procedures needs to be adapted to the next level of converter integration including these embedded active and passive components. This is one of the main concerns in this thesis.

The objectives were to design an highly integrated bidirectional 3.3 kW single phase AC/DC converter. The design includes the topology selection, control, semiconductor evaluation and EMI filter design. The converter has to comply with the EN55011 class B standard for conducted EMI. Concerning thermal management one side natural convection cooling is considered in a thermal environment from -40 °C to 60 °C.

According to the specifications and objectives, several scientific locks were identified. Identify the suitable topology is mandatory in such a project. A proper combination of converter topology and control widely impacts the efficiency and the power density. Passive components, e.g. power inductor, EMI filter, capacitor bank, still represent the major part of converter volume. Thus, it is crucial to investigate solutions to reduce their sizes and facilitate integration, especially PCB integration.

3D Folded Power Inductor

In this sense, a new 3D folded inductor was investigated. Two PCB technologies were identified to built the inductor, the Wirelaid technology from Jumatech GmbH and the Semi-Flex from Wurth Electronik. The first prototype realised with the Wirelaid highlighted some drawbacks. The mechanical stress was a main issue as the windings were broken during the bending steps. Then, characteristics of the inductor were not satisfying: the series resistance increased significantly at low frequency. The identified reasons were a bad air gap positioning, coupled to unconnected copper layers. Fringing effects at the air gap induced eddy currents so losses were increased. These were confirmed by finite element simulations.

The second prototype using the Semi-Flex technology addressed these issues. This PCB technology was less sensitive to mechanical stress, making the prototype more reliable. The air gap placement was corrected by cutting magnetic cores into two asymmetrical parts. The characterisations of the prototype showed significant improvements between the two prototypes. Further investigations highlighted the applicability of the concept in power converters requiring custom, low cost and optimised magnetic components.

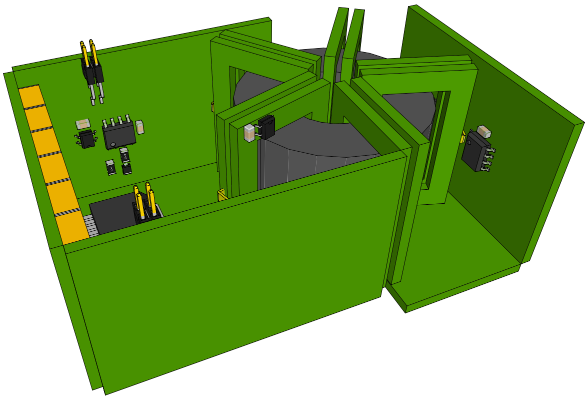


Figure 6.0.1: Switching Elementary block with Folded Power Inductor

An important possible improvement related to this design concerns the thermal model. A more accurate thermal model based on the particular shape of the 3D folded inductor can widely improve the results of the optimisation, e.g. prototype with reduced height. As a conclusion, this inductor concept presents advantages that can be used in power converter designs. The use of flexible PCBs permits further integration freedom. Overall systems (including dies, capacitors, resistors, etc) can be designed with more complex shapes without additional connectors for PCB interconnections. The PCB substrate used for the windings can also be used to solder other components, such as current sensors or even series capacitors to build a resonant tank as it is illustrated in the Figure 6.0.1.

Optimisation procedure

The presented optimisation procedure was designed according to the selected converter topology, full-bridge converter, and associated control. Implementation of interleaving was selected to enhance the performances, efficiency and power density. The impact of the modulation and the conduction mode was investigated. The unipolar modulation was considered as the most suitable control scheme due to low input inductor requirement, and reduced circulating currents in the case of interleaving.

The developed models depend on these choices. The capability of the topology to operate in soft-switching was highlighted. It reduces the semiconductor losses, especially turn-ON losses. All the necessary conditions were identified and included in the model. Therefore, a fully analytical model based on zero voltage switching recognition for all the devices was developed. The model was fed by semiconductor datasheet parameters, allowing fast comparison between several device references, reducing the computation time.

Analytical design of input filter, differential mode and common mode, has also been presented, permitting several filter solutions to be quickly compared. Multi-stage filters were investigated because of volume reduction possibilities compared to one stage filter. All the filters were designed with identical inductors but the total allowed capacitance was spread between the different stages, either for DM or CM. This was motivated by the will to balance as much as possible the capacitive current densities (A_{RMS}/µF) over the stages.

Focusing on the CM filter, impact of switching mode (hard-switching or soft-switching) on the common current was investigated. In the first case, the voltage variation depends on the switching capabilities of the semiconductor. In the second one, it depends on input inductor current and semiconductor output capacitance. So the voltage slope varies. The impact of soft-switching was included in the design as each commutation was analysed and the switching time was calculated accordingly. Thus, advantage of soft-switching on EMI perturbations, due to smoother switching transitions, was showed.

The final results of the optimisation were several combinations of semiconductor, input inductors and EMI filter. These were represented in the power density and efficiency domain to be able to select the final converter design and analyse the impact of the different optimisation variables.

All the improvements for the optimisation were identified from the feedbacks of the converter prototypes. The most important one concerned volume estimation. Large differences were observed between the procedure output and the prototypes. It was mainly due to interconnection volumes and different PCB design rules. Both should be included in the procedure to obtain more precise results.

To complete the semiconductors database GaN devices should be added. As the switching speed of GaN devices is higher than SiC, it can be used to increase further the switching frequency, to decrease magnetic component volumes. The precision of the procedure can also be improved by using characterised semiconductors in the database. However this is particularly time consuming.

According to all these possible improvements the procedure should be launch again, for discrete and integrated converters, to obtain new optimal designs which could be compared to the first prototypes.

Prototypes

Two prototypes were designed according to the optimisation procedure. The discrete converter was used to validate the optimised configuration: four interleaved cells switching at 180 kHz. It allowed to get a first feedback to compare theoretical and practical results such as volume comparison, ZVS operation, EMI behaviour. Despite manufacturing issues encountered with the discrete converter, performances were evaluated. The full ZVS operation of the converter was validated confirming the analytical results of the procedure. Low loss operation of semiconductors was also confirmed by thermal measurements. The nominal efficiency of the converter was evaluated to 95 %. The evaluation of EMI perturbations and characteristics of the input filter were divided into two phases. The first one corresponds to impedance measurements directly performed on the EMI filter. It highlighted that the routing widely impact the performances of the input filter. An increase in impedance was noticed at high frequency, reducing the attenuation. The second phase was EMI measurements realised with LISN. Measurements revealed that the converter, operating in DC/AC mode with a power DC supply placed on the DC side, did not comply with the standard. This results were mainly impacted by the DC supply.

The operation of the converter was validated, but it can still be improved. A new version should be manufactured, taking into account the issues encountered on the planar inductors, and the copper thickness which widely impact the efficiency. The power density can be improved by using multiple PCB boards and by reducing the number of LF switches which is not optimal in the case of converters using off-the-shelf components. Separating the EMI filter from the others parts of the converter can improve the overall mechanical assembly and the characteristics of the filter by reducing the parasitic elements, especially stray inductors. Finally, the volume can also be reduced by using an optimal heat-sink with shorter fins.

The results obtained with the integrated converter demonstrated the possible compactness of future power converter designed by using PCB integration. The use of the free inner space facilitate PCB stack-up and interconnections. Unfortunately, the PCB embedded inductors were replaced by planar inductors due to important mismatches between the samples. The evaluated power density of the converter, including the four interleaved cells and the second "planar" EMI filter, was 2.2 kW/L which is slightly lower than the initial objective of 3.3 kW/L. All the embedded active devices, e.g. SiC bare dies and gate drivers, were tested at low voltage ($< 50\,\mathrm{V_{DC}}$) after the manufacturing process without any issues. Tests at higher voltage ($> 100\,\mathrm{V_{DC}}$) highlighted the fragility of the implemented gate drivers. Therefore, tests at nominal voltage and power were not possible.

According to the feedbacks, the converter can be improved. Actually, the gate driver issue is a major stake. Hence, another type of gate driver should be investigated in the PCB integration context to enable full power tests. As for the discrete converter, the mechanical assembly of the integrated version can be improved to enhance the power density. New method of interconnection can be implemented to take full advantages of the "elementary cell" assembly. Indeed, multiple elementary cells can be used as plug and play elements to design larger power converters. For example, in the case of four interleaved cells, the association of the square shape and corner interconnections allows every Tetris pieces to be designed. Interconnections can simply be realised by pressing another, square or triangle, multi-layer PCB. The Tetris converter principle is illustrated in the Figure 6.0.2.

The last prototype was the power pulsating buffer implemented to answer the large electrolytic capacitor bank issue. The converter was designed in the same way as PFCs, including light changes in the procedure. As for the PFCs, the proposed solution for the PPB operated in soft-switching during the complete grid period at fixed switching frequency, reducing semiconductor losses. Due to lack of time, the prototype was only built with off-the-shelf components. The volume of 3.3 kW Buck PPB was evaluated to 0.825 L (4 kW/L) while the equivalent solution (same voltage ripple) using electrolytic capacitors was estimated to 0.935 L. Thus, the reduction of the volume by using active power buffering compared to classical method was confirmed, even if integration is required for further improvements.

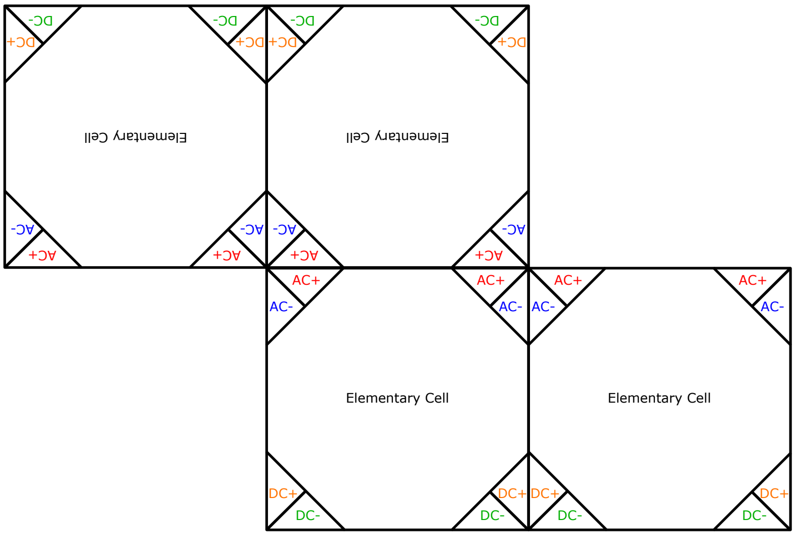


Figure 6.0.2: Tetris converter principle

All the performances of the converter need to be evaluated as the losses for the two configurations, PPB and electrolytic, are analytically obtained.

As for previous prototypes, improvements on the implementation are foreseen. With the actual design, die embedding is a good solution to improve the power density. Nevertheless, using the “elementary cell” assembly the PPB could be easily connected to the PFC. The commutation cell with the inductor can be one of the blocks while the capacitor bank another one.

A fully integrated converter including new optimal PFC and PPB coming from the updated optimisation procedures is the direct next step of this thesis project. Another possibility could be the design of a new procedure optimising both converters at the same time, including the impact of the two converters on the EMI perturbations. It can be very interesting to analyse the results of the full optimisation compared to the two independent ones.

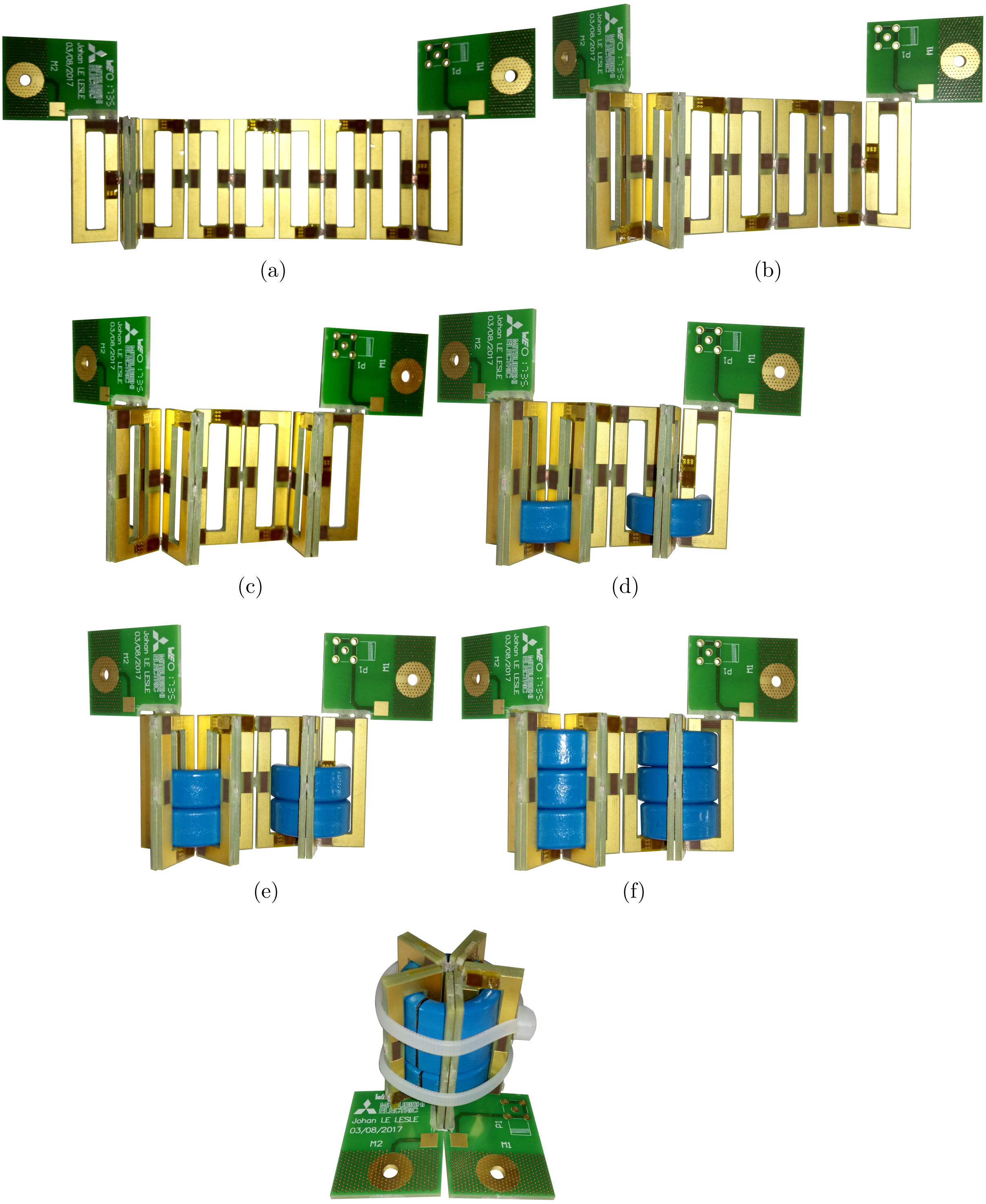
The works realised during these three years are relevant and can be used as base, complementarily with Remy Caillaud’s thesis, when high efficiency and highly integrated converters need to be designed. Lot of works remain to fully evaluate the technology and insert it into the market.

Appendices

Appendix A

Supplements to Chapter : New 3D PCB based inductor concept

A.1 Bending steps of the 3D inductor concept



(a) (b)

(c) (d)

(e) (f)

(g)

Figure A.1: Bending steps of Wirelaid inductor

A.2 Wirelaid inductor layout

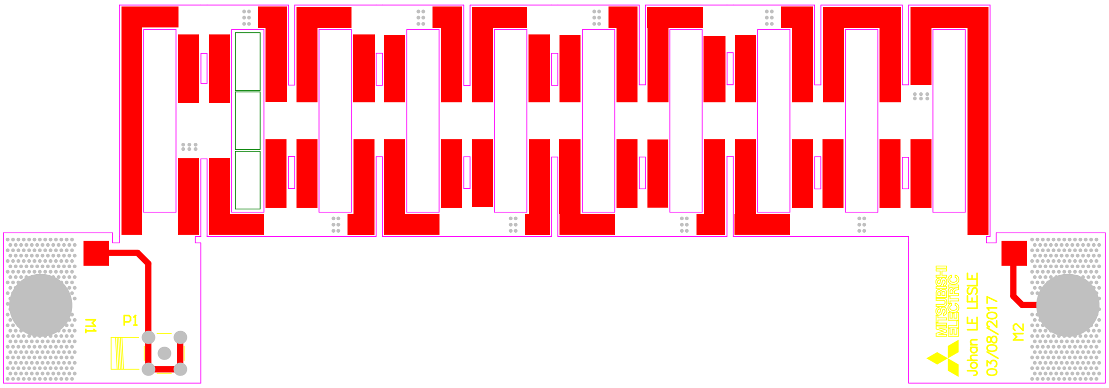


Figure A.1: Top layer

Figure A.2: Mid-layer 1

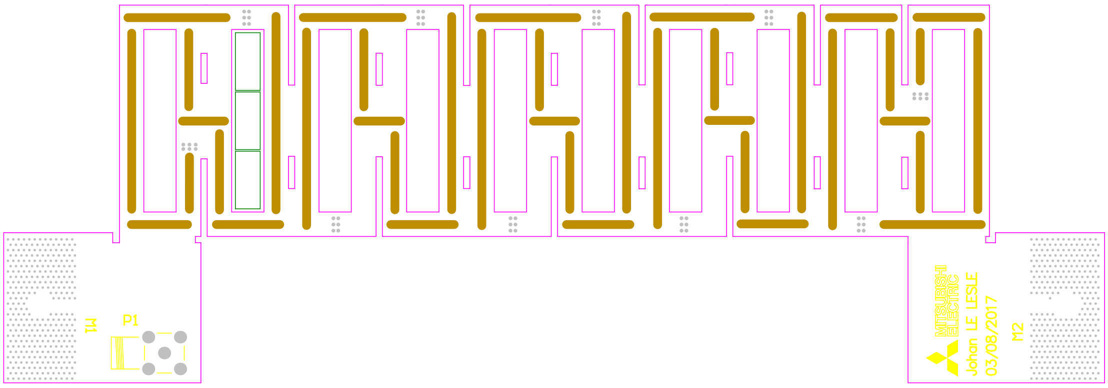


Figure A.3: Wirelaid 1 connected to Mid-layer 1

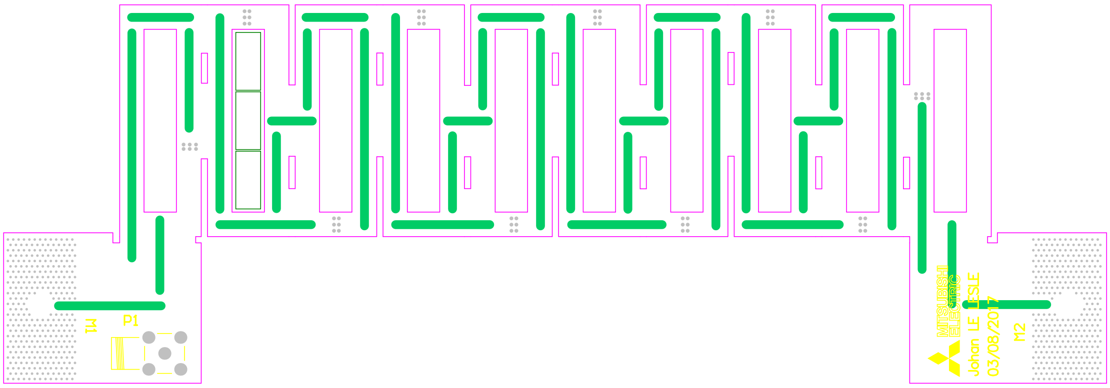


Figure A.4: Wirelaid 2 connected to Mid-layer 2

Figure A.5: Mid-layer 2

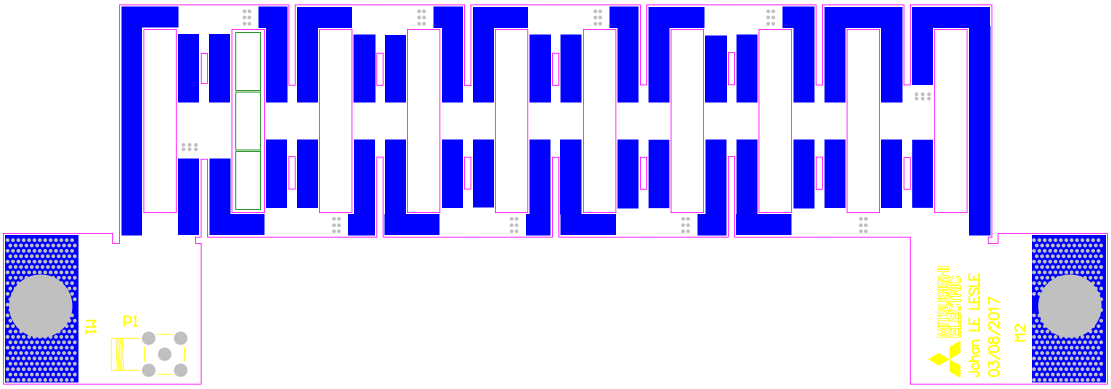


Figure A.6: Bottom layer

A.3 Flex inductor layout

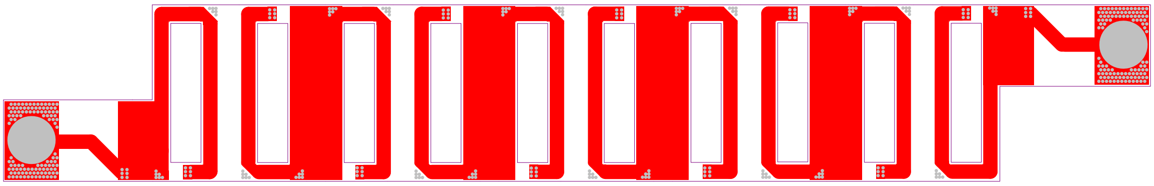


Figure A.1: Top layer

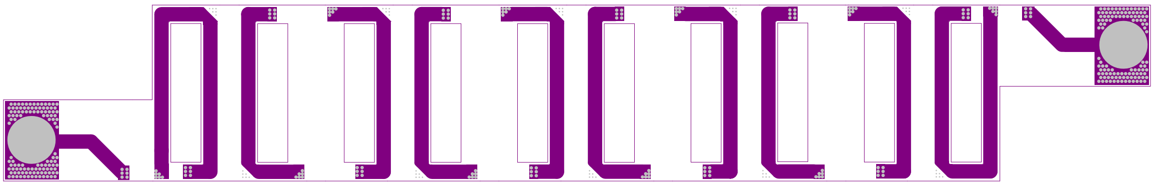


Figure A.2: Mid-layer 1 and 2 are identical

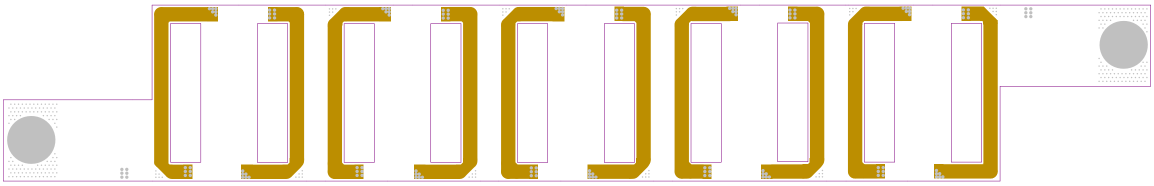


Figure A.3: Mid-layer 3 and 4 are identical

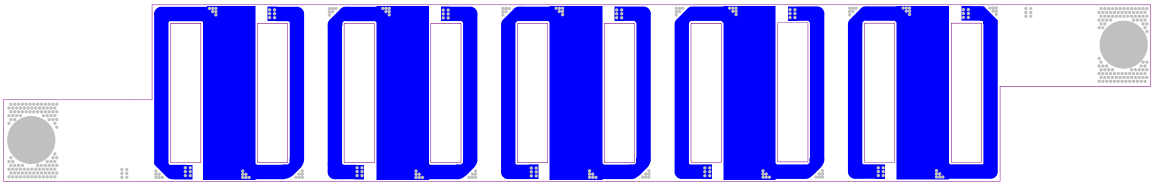


Figure A.4: Bottom layer

Appendix B

Supplements to Chapter : Design methodology for high efficiency discrete and integrated converters

B.1 Calculation of input inductor for TCM

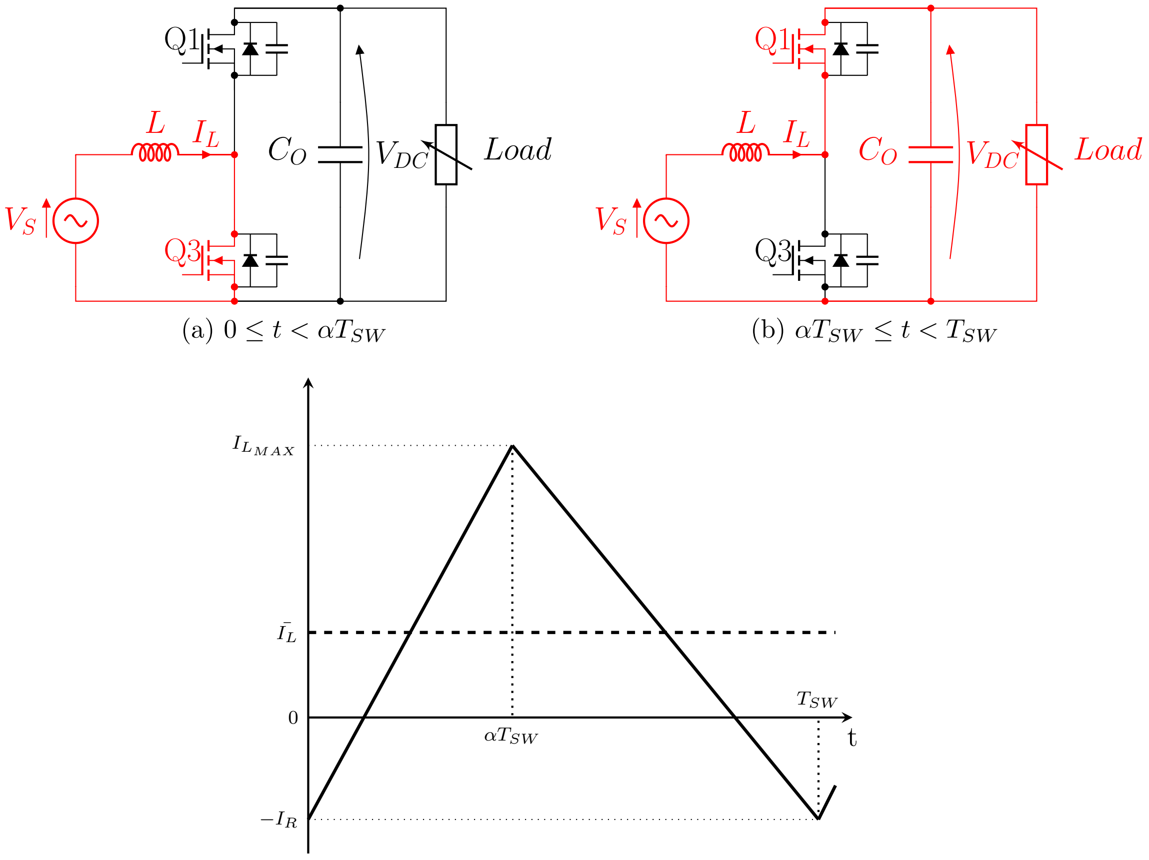
Determination of the required input inductor can be obtained according to the Figure B.1c and the following equations. The input voltage, average inductor current and the input power are given by Equations B.1.1, B.1.2 and B.1.3, respectively :

$$Vs = \hat{V}s \sin(\omega t) \tag{B.1.1}$$

$$\bar{I_L} = \hat{I_L} \sin(\omega t) \tag{B.1.2}$$

$$P = Vs \cdot \bar{I_L} = \frac{\hat{V}s \cdot \hat{I_L}}{2} \tag{B.1.3}$$

For $0 \leq t \leq \alpha T_{SW}$: Q3 is ON and Q1 is OFF



(a) $0 \leq t < \alpha T_{SW}$

(b) $\alpha T_{SW} \leq t < T_{SW}$

(c) Current waveform for one switching period

Figure B.1: Equivalent circuit for Vs > 0

$$\begin{aligned} Vs - L\frac{dI_L}{dt} &= 0 \\ Vs - L\frac{I_{L_{MAX}} + I_R}{\alpha T_{SW}} &= 0 \\ \alpha T_{SW} &= L\frac{I_{L_{MAX}} + I_R}{Vs} \end{aligned}$$

For $\alpha T_{SW} \leq t < T_{SW}$:Q3 is OFF and Q1 is ON

$$\begin{aligned} Vs - L\frac{dI_L}{dt} - V_{DC} &= 0 \\ Vs - L\frac{-I_R - I_{L_{MAX}}}{(1-\alpha)T_{SW}} - V_{DC} &= 0 \\ (1-\alpha)T_{SW} &= L\frac{-I_R - I_{L_{MAX}}}{(Vs - V_{DC})} \end{aligned}$$

Therefore,

$$\begin{aligned} T_{SW} &= L\left[\frac{I_{L_{MAX}} + I_R}{Vs} + \frac{-I_R - I_{L_{MAX}}}{(Vs - V_{DC)}}\right] \\ T_{SW} &= L \cdot \frac{(Vs - V_{DC}) \cdot (I_{L_{MAX}} + I_R) + Vs \cdot (-I_R - I_{L_{MAX}})}{Vs \cdot (Vs - V_{DC})} \\ T_{SW} &= L \cdot \frac{-V_{DC} \cdot (I_{L_{MAX}} + I_R)}{Vs \cdot (Vs - V_{DC})} \; with \; I_{L_{MAX}} = 2 \cdot \bar{I_L} + I_R \\ T_{SW} &= L \cdot \frac{-2 \cdot V_{DC}(\bar{I_L} + I_R)}{Vs \cdot (Vs - V_{DC})} \\ T_{SW} &= L \cdot \frac{4 \cdot V_{DC}(\frac{2 \cdot P}{\hat{Vs}}\sin(\omega t) + I_R)}{\hat{Vs}^2\cos(2\omega t) + 2 \cdot \hat{Vs} \cdot V_{DC}\sin(\omega t) - \hat{Vs}^2} \\ f_{SW} &= \frac{1}{T_{SW}} = \frac{\hat{Vs}^2\cos(2\omega t) + 2 \cdot \hat{Vs} \cdot V_{DC}\sin(\omega t) - \hat{Vs}^2}{4 \cdot L \cdot V_{DC}(\frac{2 \cdot P}{\hat{Vs}}\sin(\omega t) + I_R)} \end{aligned}$$

Thus, the input inductor can be determined according to the maximal switching frequency ($f_{SW_{MAX}}$) and the minimal power (P_{MIN}) :

$$L = \max\left[\frac{\hat{Vs}^2\cos(2\omega t) + 2\cdot\hat{Vs}\cdot V_{DC}\sin(\omega t) - \hat{Vs}^2}{4\cdot f_{SW_{MAX}}\cdot V_{DC}(\frac{2\cdot P_{MIN}}{\hat{Vs}}\sin(\omega t) + I_R)}\right]$$

Appendix C

Supplements to Chapter : Design methodology adapted for PPB

C.1 Polynomial fitting for Capacitance variation

$$C(\bar{V}) = p_7 \cdot \bar{V}^7 + p_6 \cdot \bar{V}^6 + p_5 \cdot \bar{V}^5 + p_4 \cdot \bar{V}^4 + p_3 \cdot \bar{V}^3 + p_2 \cdot \bar{V}^2 + p_1 \cdot \bar{V} + p_0 \quad \text{(C.1.1)}$$

Table C.1: 7^{th}order polynomial fit for the capacitance variation

	X6S	Ceralink
p_7	$5.404 \cdot 10^{-8}$	$1.122 \cdot 10^{-8}$
p_6	$-3.506 \cdot 10^{-7}$	$6.745 \cdot 10^{-8}$
p_5	$7.553 \cdot 10^{-7}$	$-7.083 \cdot 10^{-11}$
p_4	$-4.754 \cdot 10^{-7}$	$-3.456 \cdot 10^{-7}$
p_3	$-4.021 \cdot 10^{-7}$	$-3.038 \cdot 10^{-7}$
p_2	$8.668 \cdot 10^{-7}$	$3.799 \cdot 10^{-7}$
p_1	$-1.008 \cdot 10^{-6}$	$6.87 \cdot 10^{-7}$
p_0	$1.203 \cdot 10^{-6}$	$7.429 \cdot 10^{-7}$
R^2	0.9998	0.9994
RMSE	$8.5761 \cdot 10^{-9}$	$0.469 \cdot 10^{-9}$

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