Cryogenic electronics and quantum dots on silicon-on-insulator for quantum computing

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Electronique cryogénique et réalisation de boîtes quantiques sur substrat SOI pour le calcul quantique

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Résumé

Cette thèse étudie l'électronique cryogénique et la réalisation de boîtes quantiques (QD) sur substrat SOI pour le calcul quantique. Deux technologies sont proposées pour la démonstration de boîtes quantiques d'électrons (trous). La première s'appuie sur les dispositifs Trigate SOI développés au CEA-LETI et la seconde exploite la technologie FD-SOI 28 nm développée par STMicroelectronics. Dans un premier temps, les dispositifs à double-grille du LETI sont mesurés à très basse température (60 mK) pour mettre en avant le principe d'exclusion de Pauli pour les premiers trous confinés à l'intérieur des deux QD. Au travers de cette expérience réalisée sur un double QD nous étudions une brique élémentaire permettant à terme l'initialisation et la lecture d'un qubit. Cette expérience a par la suite été étendue à d'autres dispositifs possédant quatre grilles pour lesquels un protocole de mesure est proposé pour la démonstration de deux qubits de spin d'électron. Dans un second temps, nous avons adressé la question du contrôle, de la lecture et de la manipulation des qubits de spin par une électronique pouvant fonctionner à basse température. Les performances digitales et analogiques des transistors FD-SOI ont été étudiées sur une large gamme de température. La réduction de la température montre une nette amélioration de la mobilité des électrons et des trous mais également une plus faible pente sous le seuil (SS) qui s'accompagne également d'une augmentation de la tension de seuil (V_{TH}). La saturation de la SS pour les faibles températures est expliquée à l'aide d'un modèle analytique développé dans le cadre de cette thèse. En modélisant une queue étroite de densité d'états près des bords des bandes de conduction et de valence et en utilisant la statistique de Fermi-Dirac, un excellent accord est obtenu entre les mesures et le modèle. L'ajout d'une variation exponentielle dans la densité de pièges d'interface permet de reproduire l'évolution de la SS sur plus de 6 décades de courant. Par ailleurs, nous montrons que l'effet d'une polarisation face arrière qui permet d'ajuster la V_{TH} des transistors FD-SOI pour viser des applications haute performance ou basse consommation fonctionne parfaitement à basse température. La modulation de la V_{TH} reste la même

de 300 K à 4 K pour les grandes et petites longueurs de grille des transistors NMOS/PMOS. Afin de tirer avantage de la technologie FD-SOI et d'évaluer son intérêt pour l'électronique cryogénique, nous avons caractérisé plusieurs oscillateurs en anneaux (RO) jusqu'à 4 K. L'étude a été réalisée en deux temps. Dans un premier temps, l'augmentation de la V_{TH} à basse température n'a pas été corrigée. Puis, cette augmentation de la V_{TH} a été corrigée grâce à la polarisation face arrière afin de conserver la même V_{TH} que celle mesurée à 300 K. Afin de conserver les avantages tirés des plus fortes mobilités des porteurs à basse température, nous montrons que la V_{TH} doit être corrigée pour réduire significativement le délai de commutation d'une chaine d'inverseurs. Nous montrons qu'à 4 K un régime de fonctionnement optimal alliant à la fois haute performance et basse consommation peut être obtenu avec une tension d'alimentation (V_{DD}) de 0.3 V contre 1 V à 300 K. Cela permet de réduire de façon significative la dissipation statique et dynamique des RO. Un produit Energie-Délai de 6.9 fJ·ps avec un délai par étage de 37 ps sont obtenus à $V_{DD} = 0.325$ V grâce à l'utilisation de la polarisation face arrière. Pour finir, nous discutons de la dualité des transistors FD-SOI canal court qui peuvent être utilisés soit comme MOSFET ou comme transistors à électron unique. La présence de QD dans les transistors FDSOI est démontrée avec des caractéristiques proches de celles obtenues avec d'autres architectures (type nanofil) offrant ainsi des perspectives intéressantes pour une future co-intégration d'une électronique cryogénique avec des qubits de spin réalisés à partir d'une même plateforme industrielle.

Abstract

This thesis studies cryogenic electronics and quantum dots on silicon-on-insulator (SOI) for quantum computing. Different types of electron and hole quantum dots are fabricated with Leti's SOI nanowire (NW) and planar 28 nm FD-SOI technology. In the first part, Pauli Spin Blockade (PSB) is studied for the first holes down to 60 mK. We show that it is governed by a strong spin-orbit coupling (SOC). The intradot relaxation rate of 120 kHz was found for the first holes. The access barriers tunability realized with additional gates was proven to be efficient regarding the isolation of qubit from source/drain metallic leads. Following the recent demonstration of electron-dipole spin resonance (EDSR) achieved in electron quantum dots confined in the corners of silicon nanowire (CDs), we deeply investigated quantum dots in several n-type samples under different body-biasing conditions. Based on preliminary cryogenic transport measurements, an operation protocol for a compact two electron spin qubit gate has been proposed.

Regarding cryogenic electronics required for efficient control, manipulation and read-out of a large number of qubits, the low temperature digital and analog performance of 28 nm FD-SOI MOSFETs were analyzed from room temperature down to 4 K. Significant improvements in transistor performance are achieved with a clear enhancement of carrier mobility and a strong reduction of subthreshold swing (SS), even for short-channel devices with gate length down to 28 nm. The saturation of the subthreshold swing at low temperature is explained with a new analytical model developed in this thesis. By introducing a narrow tail in the density of states at the edges of the conduction and valence bands and using the Fermi-Dirac statistics, an excellent agreement of SS is achieved between experiments and modeling. The analysis of the $SS - I_{DS}$ metric under different forward body-biasing (FBB) conditions has revealed that the increased density of interface traps cannot be responsible for the SS saturation at low temperature. By adding a slight exponential variation in the interface trap density, we show that the $SS - I_{DS}$ curve can be well reproduced over more than 6 decades, paving a way for an efficient cryogenic design of CryoCMOS. In a

second time, the cryogenic performance of Ring Oscillators (RO) down to 4 K was investigated. We have shown that the optimal supply voltage can be reduced down to 0.3 V. This allows to efficiently reduce the dynamic and static power dissipations. At the same time, a small Energy-Delay product of 6.9 fJ·ps with a delay per stage of 37 ps was achieved at $V_{DD} = 0.325$ V under aggressive FBB.

Finally, in the last chapter, the duality of short-channel FD-SOI transistors operation as FETs or SETs is demonstrated at 4 K. By benchmarking the QDs with respect to the common silicon platforms, we show that 28 nm FD-SOI technology has a great potential for both cryogenic electronics and qubits.

Thesis outline

This thesis consists of six chapters and is organized as follows. In Chapter 1, the current challenges towards silicon-based large scale quantum computing are reviewed. We first start with a brief introduction into the physics of quantum bits (qubits) and list the major achievements recently obtained in the silicon spin qubit progress. This includes the realization of a robust silicon electron qubits in purified silicon as well as the demonstration of CMOS compatible electron and hole qubits fabricated on 300 mm silicon substrates using Leti's silicon-on-insulator (SOI) nanowire technology. Then, more sophisticated few-quantum bits experiments are mentioned and the challenges towards many-qubits system regarding the requirements for long-range coupling, advanced solutions for qubit's readout, scalable architectures, purification of natural silicon to improve the spin qubit performance, the optimal temperature of qubit operation and the need of cryogenic electronics to efficiently control qubits. Indeed, a particular attention to cryogenic electronics (CryoCMOS) based on advanced CMOS technologies was a driving force of this thesis.

Then, low temperature experiments on multi-gate nanowire transistors are described in the next chapter 'Silicon Nanowire Technology for Qubits'. First, the fabrication of SOI nanowire multi-gate devices is briefly described. Pauli Spin Blockade (PSB) for the first holes is studied and the role of the spin-orbit coupling is analyzed down to 60 mK. Moreover, electrostatic tunability of access barriers using a p-type device with four gates in series is demonstrated and its importance regarding improvements in hole spin qubit performance is discussed. Then, the electron quantum dots confined in the corners of nanowire (corner dots) are reviewed for all-electrical electron spin control using electron-dipole spin resonance (EDSR). The importance of using a special design with split-gates (Face-to-Face) is emphasised. We study electron corner dots in several n-type devices and discuss the role of disorder and dopants in the channel using addition energy values as the main metric. Our analysis of low temperature stability diagrams is supported with realistic simulations. Finally, by investigating different double

quantum dot (DQD) regimes in a n-type device with four gates, we propose an operation principle for the demonstration of CMOS two-qubit gate, the building block of quantum computers.

The next chapter summarises the digital and analog performance of 28nm FD-SOI MOSFETs from room temperature down to 4 K. It begins with a description of key features of this commercially available technology and room temperature analysis. Then, transfer $I_{DS} - V_{GS}$ and output $I_{DS} - V_{DS}$ characteristics of a large number of isolated devices are given and the low temperature behaviour of FD-SOI is discussed. We investigate the low temperature evolution of the effective mobility μ_{EFF} for NMOS and PMOS devices with different gate oxide thickness using the C-V split technique. The effect of channel doping on $\mu_{EFF}(T)$, the shift of threshold voltage (V_{TH}) at low temperature, the subthreshold behaviour in terms of $SS-I_{DS}$ metric are discussed. A variability analysis of long-channel devices is presented and the variability issues associated to a cryogenic operation are mentioned. The overdrive drain currents I_{ODLIN} and I_{ODSAT} are discussed for a large set of NMOS and PMOS transistors with short- and long gate length. Then, the body-biasing capability is analyzed down to 4 K. The low temperature behaviour of effective currents of short-channel NMOS and PMOS are reviewed as well as the extended window of body-biasing at low temperature are discussed. An excellent efficiency of body-biasing is demonstrated down to 4 K. The analog performance at 4 K is analyzed.

In Chapter 4, the low-temperature saturation of the subthreshold swing (SS) in FD-SOI MOSFETs is discussed. First, we show the saturation of $SS(T)$ for a set of different samples and review the existing theories and approaches used to explain the saturation. Then, by introducing a narrow tail close to the edges of the conductance and valence bands and using the Fermi-Dirac statistics to describe charge carriers, we develop a physics-based model explaining the saturation of SS below 35 K in FD-SOI devices.

Cryogenic performance of 28 nm FDSOI Ring Oscillators (ROs) is analyzed down to 4 K in Chapter 5. The chapter starts with a description of the circuit, its principle of operation as well as room temperature characterization. Then, a thorough analysis of cryogenic performance of ROs fabricated with different technologies and the existing solutions for optimization of low temperature performance are presented. Two different modes of operation are reviewed. Within the first one the measurements are done without body-biasing having the V_{TH}-shift attenuating the impact of low temperature mobility enhancement on RO performance. In the second approach, forward body-biasing (FBB) is used to keep $V_{TH} = V_{TH}(296K)$ of NMOS and PMOS transistors down to 4 K. Then, several metrics are used to analyze the cryogenic performance of ROs, such as the dynamic and static

currents $I_{DYN,STAT}$ (power $P_{DYN,STAT}$), the delay per stage (τ_P), the energy per transition (EPT), the energy-delay product (EDP) under different FBB conditions. We find a good agreement between the low-temperature gain in τ_P obtained from the measurement of ROs and the gain estimated using the effective current I_{EFF} from isolated NMOS and PMOS transistors from 296 K down to 4 K. By exploring very aggressive FBB voltages (V_{FBB}) up to ± 5.8 V, we show that the performance-power tradeoff can be efficiently managed at 4 K and the supply voltage can be reduced down to $V_{DD} = 0.325$ V while keeping an excellent performance. We present the low-field mobility (μ_0) comparison between 296 K and 4 K and show that, even for the shortest $L_G = 28$ nm, the short-channel $\mu_0(4K)$ is enhanced as compared to room temperature. Then, by comparing the key metrics of ROs with $L_G = 28$ and 46 nm, we demonstrate that comparable performance can be achieved for these devices thanks to FBB. The variability analysis of short-channel NMOS and PMOS devices is discussed and the choice of optimal temperature for the cryogenic electronics of control based on FD-SOI of 4 K is justified.

The last chapter describes the duality of short-channel FD-SOI transistors. Here by measuring wide ($W = 200 - 300$ nm) and short-channel transistors, we show that the same NMOS and PMOS devices can be operated either as field-effect transistors (FETs) or single electron transistors (SETs) depending on the drain voltage V_{DS} and body-biasing. In two similar NMOS devices, we find almost the same features in 4 K stability diagrams with high addition energies as well as an excellent electrostatic control. By benchmarking different silicon platforms currently used to fabricate robust and efficient quantum dots, we demonstrate the interest of FD-SOI technology for qubit applications. In addition, PMOS short-channel devices were deeply analyzed and the effect of boron dopants diffused from Source/Drain regions is illustrated by using the Coulomb spectroscopy. The chapter ends with a description of a prototype cryogenic circuit recently fabricated using 28 nm FD-SOI which integrates both cryoelectronics and quantum devices.

Finally, we outline the main conclusions and perspectives of this thesis in terms of different silicon quantum dots for spin qubits and cryogenic electronics based on industrial FD-SOI technology.

Contents

Short list of frequent acronyms

Qubit - Quantum bit.

SOI - Silicon-on-Insulator.

FD-SOI - Fully-Depleted Silicon-on-Insulator.

28nm FD-SOI - STMicroelectronics commercial planar process technology.

PSB - Pauli Spin Blockade.

SOC - Spin-orbit coupling.

SS - Subthreshold Swing.

EDSR - Electron-dipole spin resonance.

QD - Quantum dot.

DQD - Double quantum dot.

CD - Corner dot.

FBB/RBB - Forward and reverse body-biasing.

V_{FBB} **,** V_{RBB} - Forward and reverse body-biasing voltages.

CryoCMOS - Cryogenic digital and analog electronics specially designed to control, measure and read-out large-scale qubit systems.

RO - Ring oscillator.

FET or MOSFET - Field-effect transistor

SET - Single electron transistor.

I_{ODLIN} **and** I_{ODSAT} - Overdrive drain current extracted at typically $V_{GS} - V_{TH} = 0.5$ V and $V_{DS} = 50$ mV and $V_{DS} = 1$ V respectively.

NMOS / PMOS - n- and p-type MOSFETs.

V_{TH} - Threshold voltage of a MOSFET.

V_{TH-LIN} **,** V_{TH-SAT} - Linear and saturation MOSFET threshold voltages extracted at low and high drain voltage (typically at 50 mV and 1 V).

I_{DYN} **,** P_{DYN} - Current and power of a ring oscillator in the dynamic (oscillating) mode.

I_{STAT} **,** P_{STAT} - Current and power of a ring oscillator in the static (stand-by) mode.

τ_P - Measured delay per stage of a ring oscillator accounting for the number of inverter stages and the frequency divider.

I_{EFF} - Effective current calculated using transfer and output characteristics of N- and PMOS transistors.

V_{DD} - Supply voltage of a ring oscillator.

μ_{EFF} - Effective mobility of a MOSFET measured using the C-V split technique.

μ_0 - Low-field mobility of a MOSFET extracted using the Y-function method

Face-to-face, F-to-F - A specially designed Leti nanowire transistors with two spilt gates partially covering the channel and placed in front of each other.

RCS - Remote Coulomb Scattering.

SR - Surface roughness.

PS - Phonon scattering.

SPS - Soft phonon scattering.

I_{ON} **,** I_{OFF} - Drain current of a MOSFET at high drain voltage (typically $V_{DS} = 1V$) and $V_{GS} = V_{DS}$ and $V_{GS} = 0$ V respectively.

E_{ADD} - Additional energy required to add an additional electron (hole) in a quantum dot.

BOX - Buried oxide separating bulk silicon from the channel in the silicon-on-insulator wafer.

V_{BACK} - Backgate voltage. For electrons, $V_{BACK} > 0$ V becomes V_{FBB} and $V_{BACK} < 0$ V is V_{RBB}.

EOT - Equivalent oxide thickness of the $SiO_2/high - \kappa$ gate oxide of Leti and STMicroelectronics transistors which both use high-κ metal gate technology.

DIBL - Drain-Induced Barrier Lowering.

RT - Room temperature.

RVT / LVT - Regular and low V_{TG} architectures of 28 nm FD-SOI transistors.

GO1 , GO2 - Thin and thick EOT transistors.

C_{OX} - Gate capacitance defined by the geometrical dimensions.

C_{Si} - Semiconductor capacitance.

Chapter 1

Current challenges towards Si-based large scale quantum computing

In this chapter a brief review of main ideas behind quantum computing is given. The progress in silicon-based spin qubits with close to conventional CMOS fabrication route is presented. The difficulties associated with scaling up, i.e. increasing the number of qubits with respect to main constraints are mentioned. The interest of co-integration of the qubit layer with cryogenic electronics is justified. Finally, the correspondence between the results presented in this thesis with the challenges of silicon CMOS large-scale quantum computing is established.

1.1 Towards large-scale silicon quantum computing

The necessity of quantum computers (QCs) to simulate 'physics' by exploiting the problem of many-particle quantum wavefunction was first foreseen by Richard Feynman in the 80ties [1]. Quantum computing is fundamentally different from the classical binary logic where the information is encoded into bits storing either logical "1" or "0 [2]. This principle is illustrated in Fig.1.1 (a) using a simple inverter. Indeed, the quantum computer composed of quantum bits (qubits) can store exponentially more information than the one using classical binary logic [3]. For instance, to represent n-qubit system one needs to have n quantum and 2^n classical bits. A large number of new quantum algorithms for resolving problems not accessible by standard computers (SCs) has been proposed [4]. The

following algorithms are of particular interest : (i) Shor's algorithm [5] for integer factorisation (running time $O(logN)^3$ for QC and exponentially larger $exp(O(logN)^{1/3}(O(log\ logN)^{2/3}))$ for SC [6]); (ii) Grover's algorithm [7] for unstructured search problem (nearly quadratic speedup for QC [4]), to calculate dynamical properties by resolving the Schrodinger equation of (interacting) many-body systems which is currently a topic of active research in the fields of quantum chemistry[8], quantum field theory[9], etc. Finally, quantum computing can be efficiently applied for solving large systems of linear [10] and differential equations [11], data fitting [12], and machine learning [13].

Similarly to the binary classical logic, a qubit can be characterized by two states : $|0\rangle$ (ground state) and $|1\rangle$ (exited state) as shown in Fig.1.1 (b). However, the difference lays in the quantum nature of qubits systems. The qubit can be in the linear combination of computational basis states leading to the superposition: $|\psi\rangle = \alpha|0\rangle + \alpha|1\rangle$. Thus, the qubit can exist in a continuum of states until is measured and α^2, β^2 give the probability of finding $|0\rangle$ or $|1\rangle$ after the measurement. A convenient way to represent a two-level quantum system is to use the Block sphere. Then, the pure states $|0\rangle$ and $|1\rangle$ (spin-up and spin-down for spin qubits) point towards the north and south poles of the Block sphere whereas the interior points correspond to the mixed states (see Fig.1.1 (b)).

The famous paper on the requirement for the physical implementation of quantum computation [15] (so-called DiVincenzo criteria) describe a list of necessary condition for realizing the QC: (1) a scalable physical system with well-characterized qubits (few-electron/hole regime, cryogenic temperature, static magnetic field); (2) the ability to initialize the state of the qubits (3) long relevant decoherence (T_1 to corresponding the relaxation from excited to ground state and T_2 describing the dephasing time), much longer than the gate operation time; (4) A universal set of quantum gates (quantum 'XOR' or 'CNOT' gate will be discussed in details); (5) A qubit-specific measurement capability (read-out through spin-to-charge conversion or using a reflectometry technique); (6) The ability of interconvert stationary and flying qubits; (7) The ability to faithfully transmit flying qubits between specified locations. The last two conditions (6-7) are additional to (1-5) and are required for quantum communication protocols and will only partially be addressed in this chapter.

The principle of qubit operation is given in Fig.1.1. A very simplified operation sequence consists in: (i) initializing the qubit in the ground state $|0\rangle$ (a static magnetic field B_0 splits the lowest energy level by lifting the spin degeneracy), (ii) sending both DC (few mV) and AC (typically from 1 to 10 GHz for silicon spin qubits) signals to detune the quantum dot system

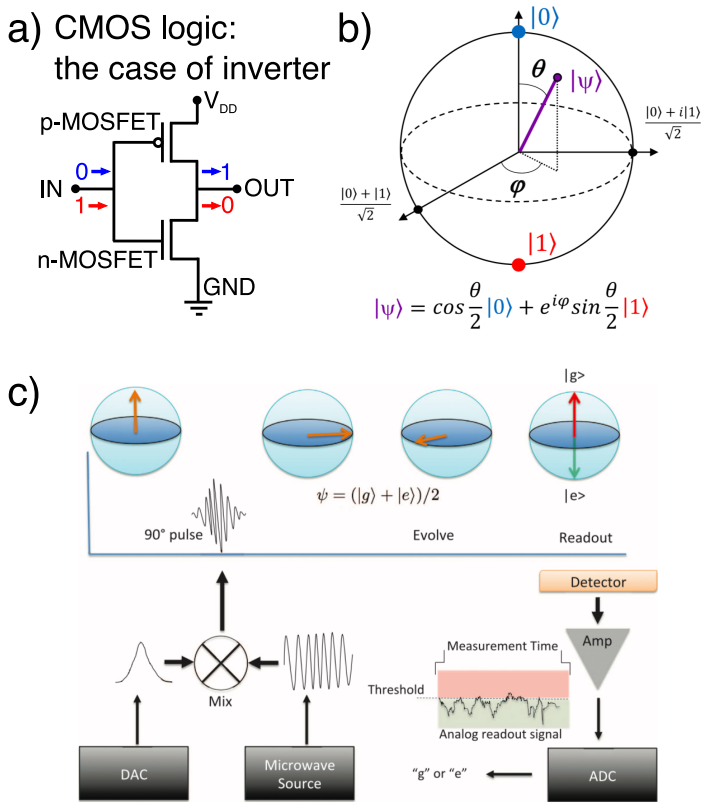


Figure 1.1: (a) Illustration of classical binary logic using an inverter. (b) Qubit representation with a Block sphere formalism. (c) Principle of operation of a qubit. Taken from [14]

and to coherently drive the qubit between $|0\rangle$ and $|1\rangle$, (iii) waiting for the system located in a dephasing environment to evolve, (iv) reading-out the final output and thus determining the Rabi frequency and dephasing times [14]. Finally, typical key parameters used to benchmark different qubit realization are : clock speed, coherence time, the fidelity and speed of single- and two-qubit logic gates, read-out time, susceptibility to crosstalk between qubits, footprint for scalability, architectural complexity (how many gates to define a single qubit, the number of levels of metal gates, etc), the constraints imposed on the control and read-out hardware [14].

Regarding quantum computation with superconducting qubits, this platform uses superconducting Josephson junctions which are usually realized as tunnel junctions in which two superconductors (typically made of aluminum) are separated by an insulating region (oxide layer). Tremendous progress has been achieved in the field of superconducting qubits [16, 17].

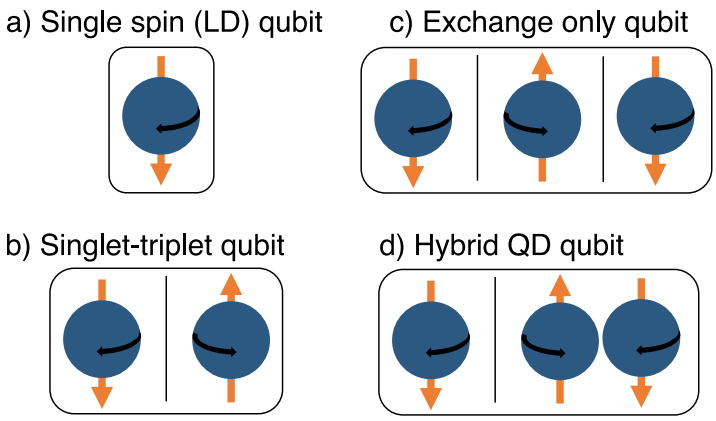


Figure 1.2: Different quantum dot spin qubits.

But, given the possible issues with large scaling-up of macroscopic superconducting systems, we will focus our attention on the semiconductor spin qubits. Furthermore, since there exist several limitations for the gate fidelity and spin coherence times in III-V systems due to a high percentage of nuclear spins in the host material [18, 19], in this section we will focus on silicon-based quantum dot system realizations.

Indeed, tremendous work has been done to make these silicon-based systems compatible with industrial CMOS technology characterized by high-yield, reproducibility and cleanliness [20]. Although initially solid-state quantum qubits were realized through manipulation of a single charge in quantum dot systems [21], it was found advantageous to encode the information into a spin degree of freedom since spin qubit coherence times are much less impacted by charge noise. Particularly long coherence times and high fidelity were recently reported for silicon spin qubits [22–24].

There exist several types of implementations of semiconductor spin qubits based on gate-defined quantum dot systems. For instance, a single spin (Loss-DiVincenzo) qubit is the most compact architecture which is realized with only one quantum dot [25] as shown in Fig.1.2 (a). It requires magnetic manipulation (AC B-field for electrons [22]) or electron-dipole spin resonance EDSR-manipulation with AC E-field only for holes [26] or electrons (depending on the strength of spin-orbit coupling SOC) [27]. Other common qubit implementations schematically shown in Fig.1.2 (b - d) are the following:

- a singlet-triplet qubit which consists of realizing a spin qubit with two quantum dots controlled using one gate voltage, thus having one electric and one magnetic axis [28];

- an exchange only qubit is obtained with three dots and controlled with two gate voltages, having two electric axes [29];

- a hybrid quantum dot qubit which uses two dots controlled with one gate voltage having two electric axes [30].

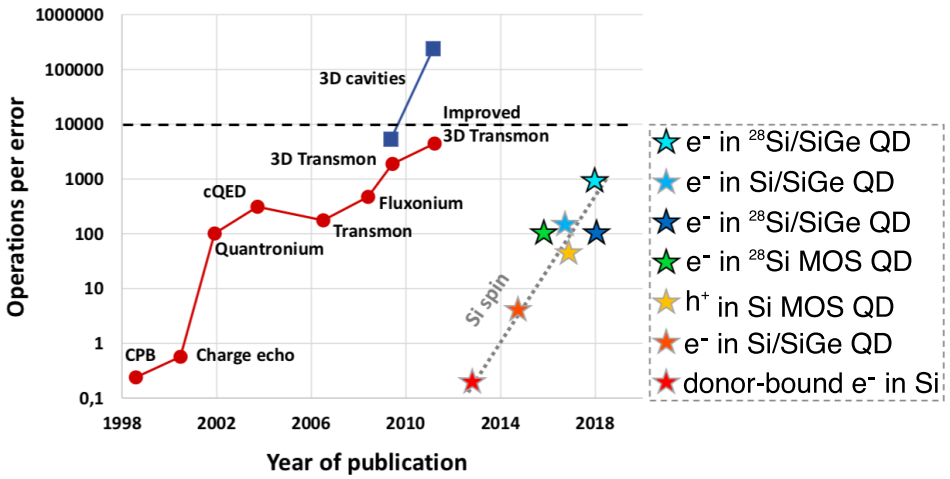


Figure 1.3: Graph adapted from [16], showing the number of operations per error for various implementations of superconducting qubits versus publication year. The added star symbols represent recent demonstrations of Si spin qubits in electrostatically-defined quantum dots. The figure of merit was estimated as the dephasing time T_2^* divided by the time needed to induce a π-rotation of the spin. Taken from [31].

While Google, IBM and a number of other companies and academic labs have achieved considerable progress in superconducting systems as large as 50 qubits [32], more recently silicon-based electron (hole) spin qubits were demonstrated to operate close to the operation per error threshold or 'Q'-factor as shown in Fig.1.3. Maximizing the Q-factor is crucial for performing robust calculations since it sets an upper bound to the number of operations that can be sequentially performed on a number of qubits for the implementation of quantum error detection protocols [31]. Thus, owing to the silicon spin qubit compatibility with state-of-the-art technologies continuously improved over several decades by the IC manufacturing industry, the stage of the superconducting qubit progress will possibly be achieved and overpassed in the near future.

In Fig.1.4 three recent demonstrations of silicon spin qubit architecture are shown. All these architectures were used for electron spin qubit experiments. In Fig.1.4 (a) a single electron was trapped in a natural Si/SiGe

quantum well and a quantum dot was electrostatically formed with gate voltages [33]. Vandersypen and colleagues performed the electron spin manipulation using EDSR-mechanism thanks to an on-chip micromagnet generating an inhomogeneous B-field across the quantum dot. A high fidelity exceeding 99% and long inhomogeneous dephasing time T_2^* during free-evolution as well as relatively fast qubit manipulation rate were found. In contrast, using isotopically purified ^{28}Si in MOS structure with a microwave antenna close to the quantum dot (as shown in Fig.1.4 (b)), Veldhorst and colleagues could achieve much longer T_2^* and higher fidelity rate [22] due to reduced impact of hyperfine interaction with nuclear spins since approximatively 4.7% of non-zero nuclear spin ^{29}Si is usually present in natural silicon. The manipulation of spin was performed through electron spin resonance (ESR) induced thanks to the microwave antenna generating AC B-field. Finally, Muhonen and colleagues found even larger T_2^* [34] by using a single electron spin bound to a phosphorus dopant in isotopically purified ^{28}Si, see (as shown in Fig.1.4 (c). The same mechanism of ESR-manipulation using an on-chip microwave antenna was used. In all cases, the spin read-out was performed using a single electron transistor (SET) capacitively coupled to the quantum dot. A common feature of all above-presented architectures is the use of 'planar' geometry, many gates and several layers of metal gates to realize a single qubit. Although these qubit experiments have confirmed the expectation that individual electron spins in silicon can be highly decoupled from their environment and can be controlled coherently with high accuracy, regarding the scalability issues and problematic integration into common CMOS technologies, these architectures are not optimal.

An alternative route based on the fabrication of industry-standard CMOS transistors was proposed to obtain devices with qubit functionality. Fig.1.5 (a) shows a p-type double gate nanowire transistor fabricated on a 300 mm Silicon-on-Insulator wafer. Using hole double quantum dot (DQD) in Pauli Spin Blockade (PSB) configuration, a fast, all-electrical, two-axis control of the first hole spin qubit was demonstrated (see Rabi oscillations in 1.5 (b)). Regarding a common CMOS silicon nanowire fabrication high-κ metal gate (HKMG) process [36], the only additional step is the use of electron-beam lithography to obtain sub-100 nm gate pitch and thick 20 nm spacers isolating the DQD from Source/Drain regions. The main difference here is that due to the strong SOC for holes in silicon, no additional micromagnet or microwave lines are needed to produce EDSR-manipulation. Another distinct feature of this architecture lays in its compactness: one gate-confined quantum dot can provide a qubit and the adjacent one can be used for PSB read-out [37]. Despite the obvious advantage regarding the device yield, variability, and reproducibility due to the well-established fabrication pro-

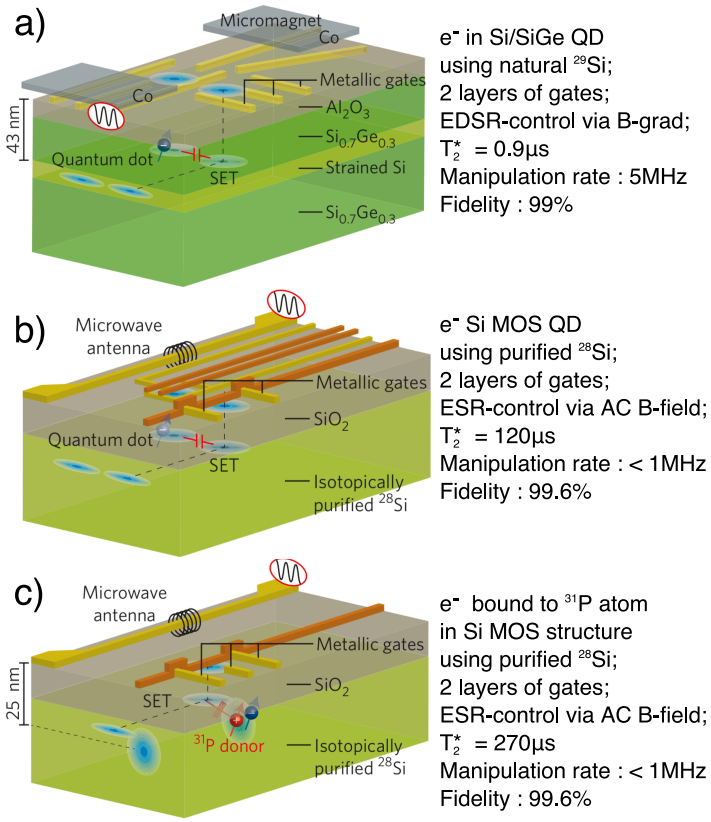


Figure 1.4: Three breakthrough, proof-of-concept electron spin qubit experiments demonstrated in 2014. Adapted from [35]

cess, the qubit functionality was demonstrated in the many-hole regime. However, the first hole-regime which is very difficult to achieve was observed in similar nanowire devices in [38, 39] and in planar Si MOS QDs [40].

Nevertheless, an ultra-compact and very promising hole spin qubit platform was successfully demonstrated with remarkably high manipulation frequency $f_{RABI} = 85$ MHz and rather moderate dephasing time from Ramsey experiment $T_2^* = 60$ ns (due to the many-hole region and the presence of boron dopants in the channel).

More recently, an experimental demonstration of electric-dipole, spin-valley resonance mediated by intrinsic spin-orbit coupling (SOC) in a silicon electron double QD has been reported [27]. Although SOC is intrinsically weak in silicon, its effect can be enhanced in the corner QDs of an etched SOI device, owing to their reduced symmetry. Then, SOC enables EDSR

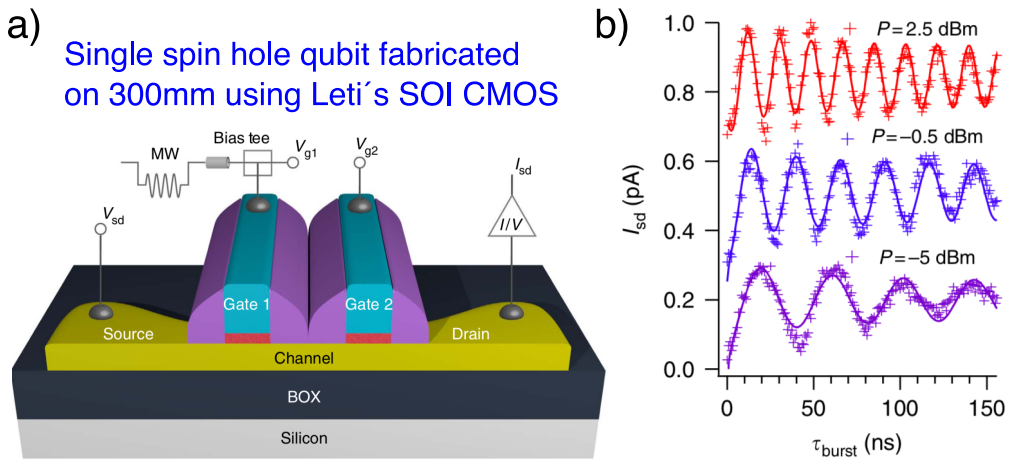


Figure 1.5: (a) Simplified 3-dimensional schematic of an SOI nanowire field- effect transistor with two gates (Gate1 and Gate2). Using a bias-T, Gate 1 is connected to a low-pass-filtered line, used to apply a static gate voltage V_{g1}, and to a 20-GHz bandwidth line, used to apply the high-frequency modulation necessary for qubit initialization, manipulation, and read-out. (b) Rabi oscillations for different microwave power as a function of microwave bursts demonstrating controlled spin rotations. Taken from [26].

on the spin-split doublet of the first, lowest energy valley by mixing the up-spin state of this valley with the down-spin state of the second valley. Importantly, the EDSR Rabi frequency is strongly enhanced near the corresponding anti-crossing, namely when the valley and Zeeman splittings are close enough [27, 41]. In turn, the valley splitting can be efficiently electrically-tuned via body-biasing in such nanowire devices [42]. This tuning is essential in order to enhance the above-described EDSR mechanism for electrons [27]. A signature of Rabi oscillations and thus of the coherent control can be found in [43].

Thus, all-electrical control of a hybrid electron spin/valley qubit, as well as the first hole spin qubit using the same SOI CMOS nanowire technology, have marked an important step towards large-scale quantum computing.

Similarly to the classical binary logic build up from the NOT and AND gates, arbitrary quantum logic can be generated from a small set of quantum gates. Two different realizations of controlled-NOT (CNOT) quantum gates using exchange interaction are shown in Fig.1.7 (a - b). Whereas the demonstration of an efficient CNOT gate for spins in silicon opens a path for multi-qubit algorithms in silicon-based quantum computing (in [44], the

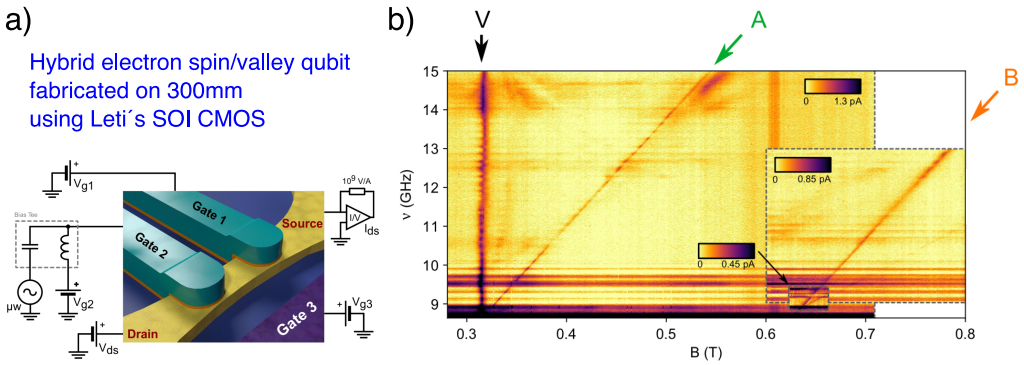


Figure 1.6: (a) Sketch of the sample and measurement setup consisting in the silicon nanowire with the source/drain extensions colored in yellow, the two top gates in green, and the side gate in purple. The gate oxides are colored in orange and the buried oxide (BOX) of the SOI in blue. (b) Color plot of the measured drain current I_{ds} as a function of the magnetic field B and microwave frequency ν. The gates are biased in the spin-blockade regime. Three different measurements are gathered for clarity. EDSR transitions are revealed by oblique straight lines, labeled with letters A and B. Adapted from [27].

resonantly driven gate operation of 200 ns is much shorter than the qubit dephasing time), the complexness of the architecture is significantly increased as compared to the single spin qubits described above.

Alternatively to the spin read-out using single electron transistors (SETs) or quantum point contacts (QPCs) challenging for scalability, gate-coupled radio-frequency (RF) reflectometry has been recently proposed as an alternative approach to qubit read-out [47]. In this read-out technique, the qubit sensing is accomplished by measuring the dispersive response of an electromagnetic RF resonator connected to one of the qubit gates and excited at its resonance frequency. Very recently, significant improvements in RF-based read-out were reported using Si MOS design [48] (average fidelity 73%), dopant-based architecture [49] (average fidelity 83%). In these experiments, resolving the qubit state within single-shot (single measurement) was demonstrated marking another step towards viable read-out method for spin qubits in silicon. A major improvement in RF-based read-out was also reported for the SOI CMOS nanowire platform (using a similar multi-gate device as those used for hole and electron qubits) [50].

In addition to the single qubit and CNOT gate demonstration, a dynamic random access architecture for efficient read-out of complex quan-

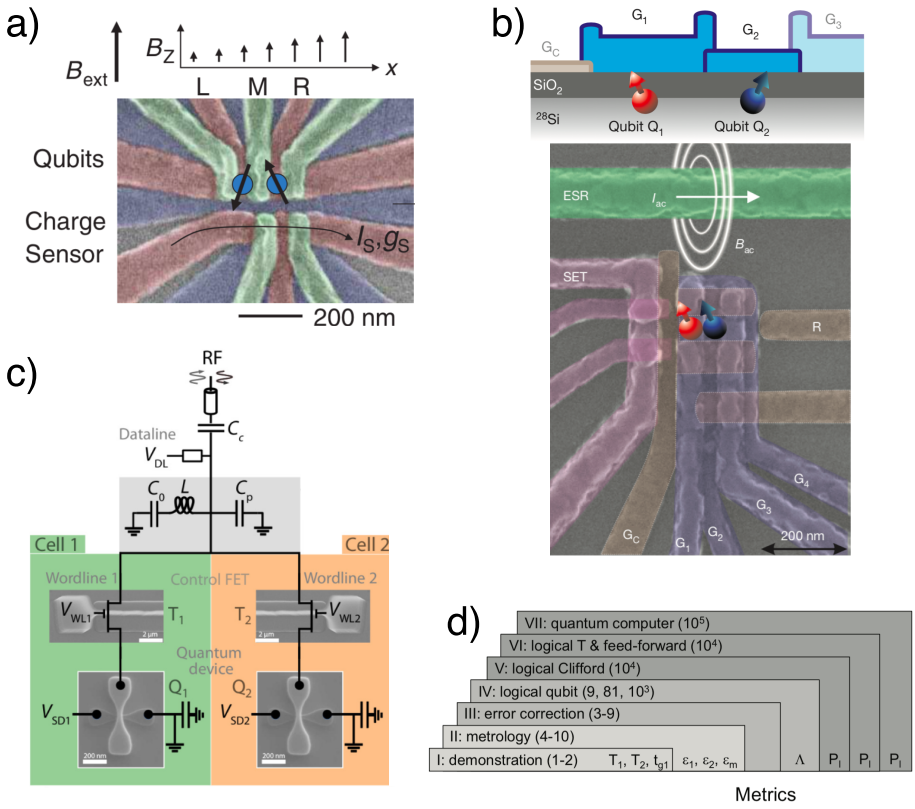


Figure 1.7: (a - b) Implementation of CNOT gates within electron spin qubit architectures using Si/SiGe and Si MOS platforms. Taken from [44] and [23]. (c) An example of a CMOS dynamic random access architecture for radio-frequency read-out of qubit devices. Taken from [45]. (d) Main steps from single qubit demonstration up to the realization of quantum computer with the number of qubits necessary to fulfil each stage's requirements. Taken from [46].

tum circuits was demonstrated at millikelvin temperatures using Leti's SOI CMOS nanowire technology [45]. The circuit divided into cells containing a CMOS quantum dot (QD) and a field-effect transistor that enables selective readout of the QD, as well as charge storage on the QD gate is shown in Fig.1.7 (c). This is analogous to the 1 transistor - 1 DRAM cell approach used in CMOS technologies. Using an RF-resonator, the dynamic read-out of two cells was successfully reported thus paving the way for reducing the number of input lines per qubit and enabling addressing large-scale device arrays.

Fig.1.7 (d) shows the roadmap towards a quantum computer illustrat-

ing the increasing complexity of qubit experiments, described by technology levels I to VII. Numbers in parenthesis show approximate qubit numbers. Errors for 1 qubit, 2 qubits and measurement are described by ϵ_1, ϵ_2, ϵ_m which leads to an error suppression factor Λ. The fault-tolerant error correction is achieved when $\Lambda > 1$ [46]. Here, it is worth mentioning that contrarily to the classical logic where each physical bit corresponds to a single logic bit, in order to achieve high computational tolerance by correcting different type of errors occurring during CNOT operation [51, 52], a quantum logic bit typically consists of several physical qubits (the actual number depends on a particular technology used as well as the error-correcting code and can reach 10^3).

Although a classical computer can compete up to about 50 qubits, solving relevant problems in quantum chemistry or code-breaking using known quantum algorithms and error correction methods require a large number of physical qubits $10^6 - 10^8$ [20, 53, 54]. Thus, adoption of well-established, mature CMOS technologies for fabrication of high-quality, reproducible single qubits seems to be one of the most promising paths towards large-scale quantum computation.

In order for a functional quantum computer to become a reality, different architectures integrating many qubits are currently investigated. In Fig.1.8 (a), a 12-quantum-dot device (for potentially 9 qubits and 3 charge sensors) fabricated on an undoped Si/SiGe heterostructures as a proof of concept for a scalable, linear gate architecture for silicon QDs is shown.

Using this design, similar quantum dots were obtained with approximatively 20% of relative variation of single quantum dot parameters (charging and orbital energies) [56]. Whereas it has marked a major achievement, it is not clear whether such variability is acceptable for large-scale quantum computing. Thus, top-down close-to-industrial CMOS fabrication process with several additional e-beam lithography steps was recently developed at Leti (in theory, the same gate pitch can be achieved using extreme UV lithography which will be brought into production fabrication for the most advanced technological nodes [57]). The left array of 8 Face-to-Face gates can be used to electrostatically define QDs in the corners of nanowire whereas the right array is used for RF read-out [58].

As we already discussed previously, silicon spin qubits in isotopically purified ^{28}Si present remarkably longer, by more than two orders of magnitude, T_2^* as compared to their natural silicon counterparts. For instance, $T_2^* = 120\mu$s for qubits based on Si MOS quantum dots [22], $140 - 270\mu$s for qubits based on phosphorus donors [34], 20μs for qubits based on ^{28}Si/SiGe heterostructures [24] for 99.92% ^{28}Si were reported.

Two-qubit CNOT gates fabricated using isotopically purified 99.92%

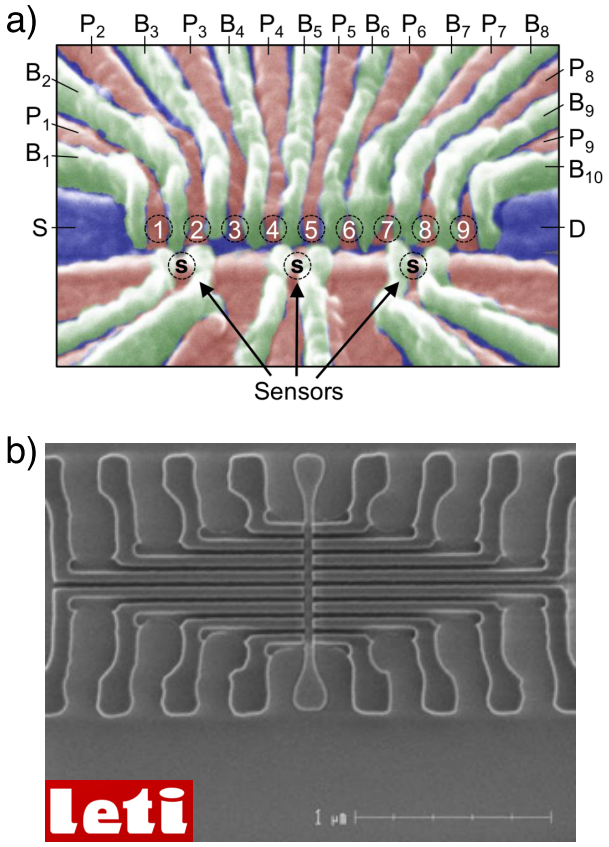


Figure 1.8: (a) False-color SEM image of a typical overlapping gate design for Si/SiGe electron QDs architecture. A linear array of 9 QDs is formed under plunger gates P1 - P9 and the tunnel couplings are controlled using barrier gates B1 - B10. Quantum dot charge sensing is realized using sensors formed under S1 - S3. Taken from [55] (b) An SEM image after gate etching of one-dimensional array of qubits along Si nanowire using 'Face-to-face' (F-to-F) devices in series recently fabricated on 300 mm wafers by Leti.

^{28}Si also have been demonstrated with high fidelities [24, 23], much better than those based on natural silicon [33, 60]. Recently, qubits based on isotopically purified Si MOS structures on 300 mm wafers covered with a 100 nm thick layer ^{28}Si purified at 99.92% have been reported and long spin relaxation time $T_1 = 145$ ms has been measured [61].

In Fig.1.9, SIMS analysis of ^{28}Si CVD-grown on 300 mm bulk Si substrates demonstrating 99.992% percentage of ^{28}Si is shown [59]. The level of ^{28}Si enrichment reported in this work is larger than in all previous reports concerning silicon qubits and hits the record purification for large-area sili-

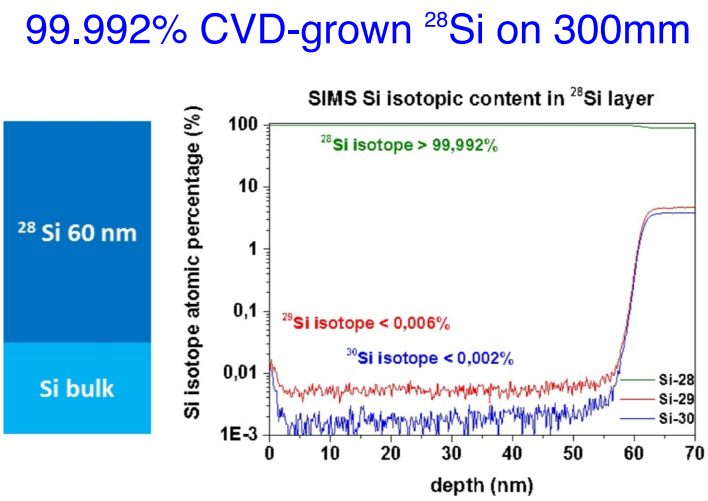


Figure 1.9: Secondary ion mass spectrometry measurements of 300 mm wafers fabricated by Leti. Left panel: targeted layer composition. Right panel: SIMS depth profiles of the Si isotopes in the resulting layer. The concentration of the ^{29}Si isotope which contains a nuclear spin 1/2 is less than 0.006% in the top layer and the concentration of the nuclear spin-free ^{30}Si isotope lower than 0.002%. Taken from [59].

con films. In addition, a detailed investigation of the isotopic concentration profile as a function of annealing temperature is given in [59] which allowed to identify the thermal budget range for the successful qubit fabrication on 300 mm using standard CMOS foundries.

Having discussed different single qubit and CNOT gate architectures as well as advanced read-out techniques, another important brick towards large-scale quantum computing is to achieve long-range coupling. There exist a great variety of different strategies to fulfill this long-range coupling requirement. We will focus on the two most promising approaches which are spin-photon coupling with on-chip microwave cavity [62–64] and extended Heisenberg exchange interaction using a quantum mediator [65].

A silicon spin qubit coupled to a superconducting $NbTiN$ resonator reported in [62] is shown in Fig.1.10 (a). In this work, the authors demonstrated that an electron spin can be efficiently coupled to a microwave photon from the resonator. Given large μm-dimensions of the resonator, the coupling of distant qubits separated by less than 100 nm was argued to be possible. Indeed, using this approach, multiple qubits can possibly interact through the same resonator thus providing a route towards scalable networks of spin qubit registers [62, 20].

Another scalable strategy for long-range qubit interactions is to use intermediate quantum dots to accomplish the coupling between neighboring qubits. In [65], this approach was applied to QDs electrostatically defined in GaAs two-dimensional electron gas and separated by more than 200 nm as shown in Fig.1.10 (b). In theory, the same method can be adopted for silicon QDs if the gate pitch is reduced below 100 nm [20]. Malinowski and colleagues have shown that a many-electron quantum dot (mediator) can be efficiently used for long-range exchange interaction providing another path for scaling large quantum-dot based qubit circuits.

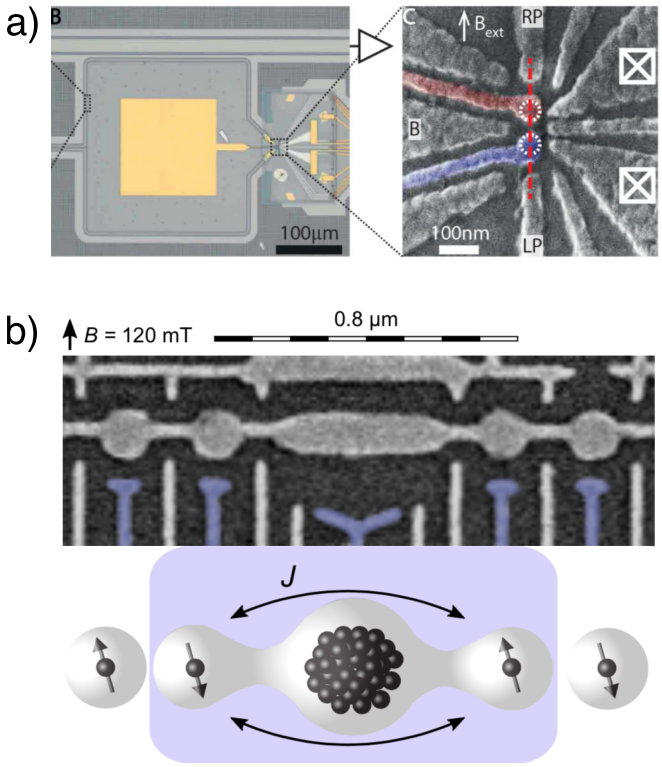


Figure 1.10: Long-range qubit coupling using (a) spin-photon coupling with on-chip superconducting resonator (taken from [62]) and (b) extended Heisenberg exchange interaction via an intermediate quantum dot (taken from [65]).

Finally, the qubit control signals and the wiring solutions as explained in [14, 20] require local electronics for running a large number of qubits in parallel. Indeed, connecting $10^6 - 10^8$ qubits from sub-100 mK to room temperature voltage source via wires or coaxial lines is hardy achievable as it conflicts with Rent's rule in classical systems and the total number

of pins on a chip [66]. Thus, the most straightforward strategy for CryoElectronics meeting the necessary requirements for qubits (clock speed, resolution, frequency range, memory, power dissipation) [67, 20] is to adopt an existing advanced sub-100 nm CMOS technology (typically $1-10$ GHz frequencies are needed to run silicon spin qubits) to balance cryogenic constraints. In addition, contrarily to III-V semiconductor qubits, in order to be able to couple/decouple adjacent qubits through exchange interaction, silicon spin qubits are denser with a typical $20-100$ nm pitch. Thus, if the co-integration of hot spin qubits working at $1-4$ K [61] with local electronics is carried out on the same chip, the density requirement imposes using very advanced CMOS technologies [20]. Depending on the actual qubit requirements regarding functionality, power budget, the spacing between qubits different complexity of classical electronics can be realized [68]. Importantly, special attention should be paid to the thermal power dissipation from cryoelectronics defining at which temperature stage the local electronics should reside.

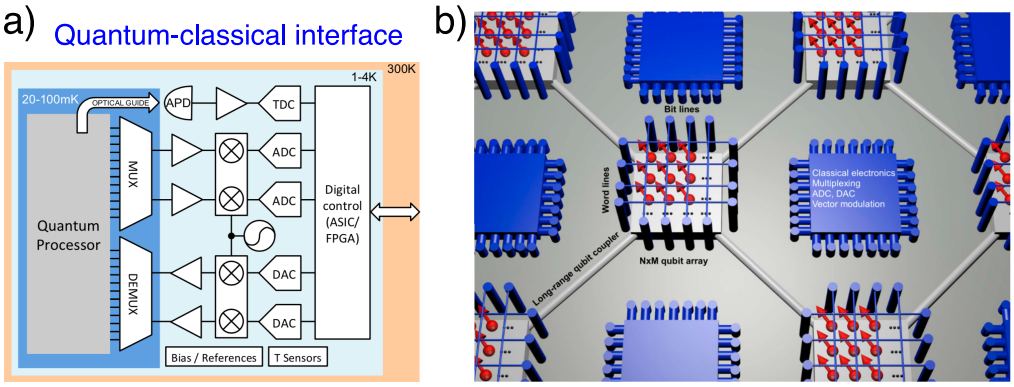


Figure 1.11: (a) A sketch showing the co-integration of qubit physical level and the control and read-out cryogenic electronics. Taken from [67]. (b) An example of qubit arrays with corresponding local electronics placed in the qubit plane for simplicity. Taken from [20].

1.2 Results presented in this thesis with respect to the challenges of silicon CMOS quantum computing

From the progress in Si-based quantum computing presented in the previous section, it seems to be clear that a thorough analysis of multi-gate Leti's qubit close-to-industrial architecture with an eventual benchmarking with the most common Si architectures is crucial for advancing towards many-qubit arrays. This is why in Chapter 2 we give a detailed analysis of both n- and p-type quantum dots of different flavor (usual quantum dots centered in the nanowire and corner dots confined in the corners of nanowire) using Leti's SOI nanowire technology. Moreover, the tunability of quantum dots in multi-gate devices using body-biasing is presented. Pauli Spin Blockade for the first holes in a double quantum dot is studied as it is commonly used in qubit read-out schemes. The role of intentionally placed and diffused dopants in the channel is discussed and the main results are supported with tight-binding simulations.

In Chapter 3, the requirements of CMOS cryogenic electronics are discussed. The digital and analog performance of 28 nm FD-SOI isolated transistors is analyzed from 300 K down to 4 K. The saturation of subthreshold swing and threshold voltages are explained by physical modeling in Chapter 4. Chapter 5 is dedicated to the analysis of low-temperature performance of Ring Oscillators fabricated within the FD-SOI technology. Several important conclusions regarding power-performance management at low temperatures are drawn. Finally, a review of the FD-SOI technology for qubit applications is given in Chapter 6 by an extensive analysis of single quantum dots electrostatically defined in conventional short-channel transistors.

Chapter 2

Silicon Nanowire Technology For Qubits

This chapter begins with a brief introduction on the fabrication of SOI nanowire multi-gate devices followed by room temperature characterization of a large number (many thousands) of samples.

Then, Pauli Spin Blockade (PSB) for the first holes is studied at different temperatures and the dip-behavior of the leakage current is explained by the spin-orbit interaction mechanism.

Moreover, by measuring a p-type device with four gates in series at low temperature, we demonstrate the electrostatic tunability of access tunnel barriers required to couple/decouple an inner double quantum dot (DQD) from the Source/Drain regions which can be used to improve the hole spin qubit performance.

We study quantum dots in using split-gate or the so-called Face-to-Face (F-to-F) geometry and analyze the first electrons confined either in the dots located in the edges of silicon nanowire or on a cluster of dopants under aggressive forward back-biasing (for the device with channel doping).

Our analysis of Face-to-Face devices is supported by realistic simulations based on the effective mass approximation used to compute the electron wavefunctions and addition energies E_{ADD} as well as the constant interaction method. All the simulations of n-type F-to-F samples were performed by Leo Bourdet (CEA-INAC).

Finally, we propose a four-gate geometry for the realization of a CMOS two-qubit logic gate and investigate different quantum dot configuration within this system.

The results presented in this chapter were partially published in [38, 69–71].

2.1 Brief description of Leti's SOI nanowire technology and 300K systematic characterization

The fabrication of multigate nanowire transistors on 300 mm SOI substrate starts with active area patterning. The whole process flow is adopted from [36, 72] with few unconventional fabrication steps such as the use of thick spacers to enhance quantum dot confinement at very low temperature and electron-beam lithography to achieve $30-40$ nm spacing between adjacent gates [70]. In the following, the front-end-of-line (FEOL) process is briefly reviewed. [110]-oriented nanowire field-effect-transistors (N- and PMOS) with high-κ/metal gate stack were fabricated on (100) SOI wafers with BOX (buried oxide) thickness of 145 nm. The silicon layer is patterned to create nanowires by mesa isolation technique. Each transistor is isolated from each other with the SiO_2 buried oxide of the SOI substrate. Nanowire patterns are defined by deep-UV (193 nm) optical lithography and followed by a resist trimming process in order to shrink the dimensions of nanowires. After the active patterning, a high-κ/metal gate is deposited. The high-κ oxide is 1.9 nm HfO_2 deposited by chemical vapour deposition technique (CVD) onto thermally-grown SiO_2 of 2.5 nm. This gives the equivalent oxide thickness (EOT) of 2.9 nm. Note that the 2.5 nm of SiO_2 is larger than the usual sub-1 nm value used in advanced CMOS, since we infer a large impact of Remote Coulomb Scattering (RCS) on the low-field mobility [73]. Indeed, in order to improve the stability of quantum dots at very low temperature, pushing this SiO_2/HfO_2 interface further away could be an important point for qubit applications. The atomic layer deposition (ALD) of 5 nm of TiN as the metal gate is followed by doped poly-Si of 50 nm. The gate is wrapped around the channel in the Trigate configuration [36] which guarantees an excellent electrostatic control of field-effect transistors (FETs) including high I_{ON}, low I_{OFF}, close-to-60 mV/dec subthreshold swing at room temperature, etc., and single electron transistors (SETs) with high charging energies, close-to-1 lever arm parameter, etc. The silicon film thickness is approximately 10 nm. In practice, nanowire width down to 10 nm can be achieved after active patterning [36], however, for the devices presented in this chapter, a typical width is $25-50$ nm.

The role of the silicon nitride (SiN) spacers formed on the sidewalls of the gate is crucial. The first spacer is mainly used to protect the channel during low dose (LD) ion implantation (II) used to form LDD regions providing low access resistances and avoiding semiconductor-metal junctions (Schottky diodes). In addition, to improve access resistance, Si raised

Source/Drain ($t = 18$ nm) are realized by CVD. Finally, the second spacer consisting of a tetraethyl orthosilicate (TEOS) liner and a nitride layer was fabricated before Source/Drain high dose (HD) implantations, activation spike anneal (to activate the dopants) and silicidation ($NiPtSi$ silicide to obtain low contact ohmic resistances). The FEOL process flow with the main fabrication steps is summarized in Fig.2.1.

To complete the fabrication, tungsten contact and standard Cu back-end-of-the-line process flows were used [70]. Thus, the interconnections, the bonding pads were created and the devices were encapsulated in a protective glass.

Some of architectures developed for different qubit experiments are summarized in Fig.2.2. An important progress towards CMOS quantum computing has been recently achieved using Leti's SOI nanowire technology:

- Fig.2.2 (a) - using the double gate in series, the first CMOS hole qubit

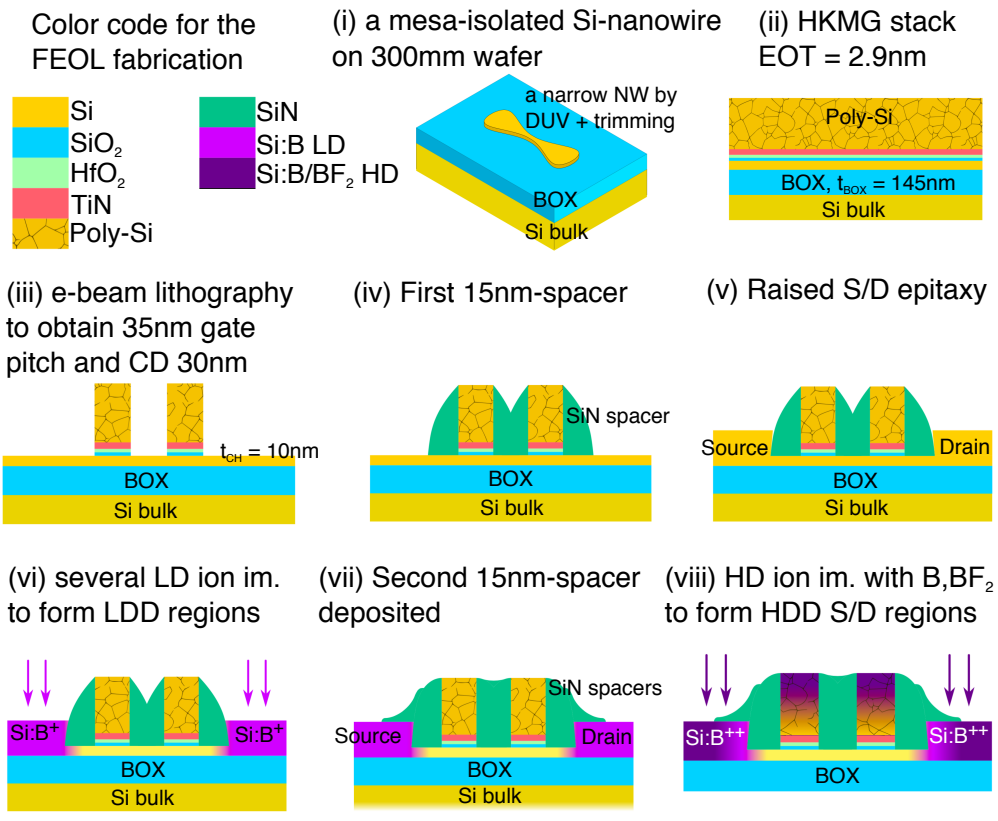


Figure 2.1: Simplified FEOL process flow for a double gate PMOS with the key fabrication steps schematically shown. Adapted from [43].

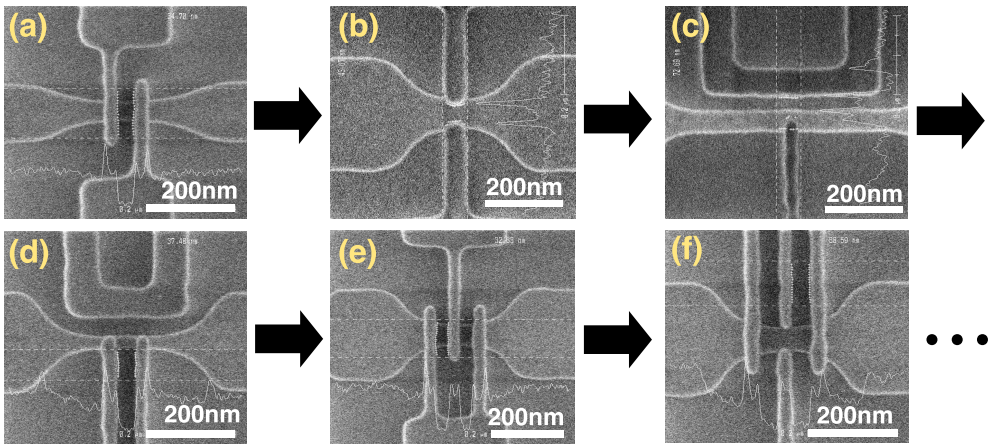


Figure 2.2: (a - f) SEM images of different multi-gate NW transistors used as quantum devices at low temperature. The images were taken after gate patterning (before the first spacer deposition).

was demonstrated [26] as well as the double gate reflectometry technique for an efficient qubit read-out [47]; Pauli Spin Blockade in the few-hole regime at 4 K and 15 mK will be presented in this chapter.

- Fig.2.2 (b) - the quantum dots (QDs) formed in the top corners of nanowire, also called Corner Dots (CDs) were extensively characterized at low temperature under different body-biasing conditions [71, 74]. In the light of recent theoretical models of all-electrical control through Electron Dipole Spin Resonance (EDSR) over the spin of electron, these unusual QDs are of great importance for scalable CMOS electron qubits [27, 41]; A thorough analysis of CDs regarding the addition energies E_{ADD}, lever arm α and the backgate tunability will be presented in this thesis.

- Fig.2.2 (d) Electrically driven electron spin resonance mediated by spin-valley-orbit coupling in a corner dot was demonstrated [27] as well as Rabi oscillations using PSB spin-selective read-out technique [43].

- Fig.2.2 (e) high-fidelity (above 99% for 1 ms integration time) gate-based spin read-out was demonstrated in [50] using the latched spin blockade mechanism [75]. In addition, low temperature characterization and tunability of similarly fabricated 4-gates-in-series devices (not shown) will be presented in this chapter.

- Fig.2.2 (f) the F-to-F geometry with additional access gates to locally couple/decouple corner dots (electron spin qubits) will be discussed in this chapter.

One of the key features of our close-to-industrial CMOS fabrication is

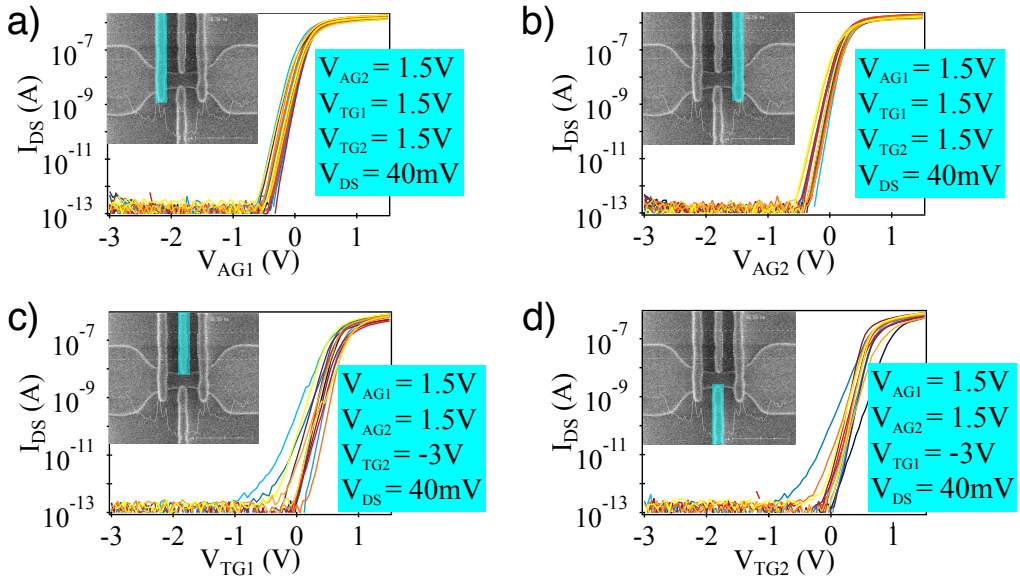


Figure 2.3: Probe station characterization over a 300 mm wafer at 300 K. Statistics over 20 random samples with $I_{DS}-V_{GS}$ at V_{DS} = 40 mV is shown. A low degree of variability is demonstrated for both access (a, b) and F-to-F (c, d) gates in terms of V_{TH} and SS.

that, at the end, a large amount of quantum devices is available for room temperature (RT) analysis with 300 mm probe station. This preliminary testing at RT allows us to verify the proper operation of different gates and their symmetrical operation.

In Fig.2.3 the transfer characteristics $I_{DS} - V_{GS}$ of a four gate NMOS device at 300 K is shown. The channel width is relaxed to 60 nm as it is required for devices that can host CDs. The gate length L_G is 40 nm for all four gates and the spacing between gates along the channel and for F-to-F gates is 35 nm. We note, that special measurement sequences were developed in order to have a better understanding of performance of F-to-F or Access gate. For instance, we open all the gates by applying a positive voltage and consecutively sweep the Access gates, see Fig.2.3 (a - b). Testing of the F-to-F gates consists in setting positive voltages to the Access gates and trying to close the channel with one F-to-F gate while sweeping the second one as shown in Fig.2.3 (c - d).

Then, despite the complexness of multi-gate device fabrication, for a set of 20 quantum devices we find a relatively low dispersion in terms of single device variation and an excellent electrostatic control comparable to the single-gate devices [36]. Due to an unintentional misalignment, we observe

a slightly higher degree of variability for F-to-F gates. It should be noted that this variability can be reduced by further optimizing the fabrication process.

2.2 Low temperature characterization of PMOS devices: PSB and the QD tunability

2.2.1 Brief review of charge transport through double quantum dot

When a double gate devices (see Fig.2.2 (a)) are cooled down to 4 K and below, the so-called stability diagram are typically recorded to probe transport through quantum dots [77]. They are obtained by sweeping the gate voltages and recording the drain current I_{DS}. In our case, artificial atoms or QDs with discrete energy spectrum are formed due to structural

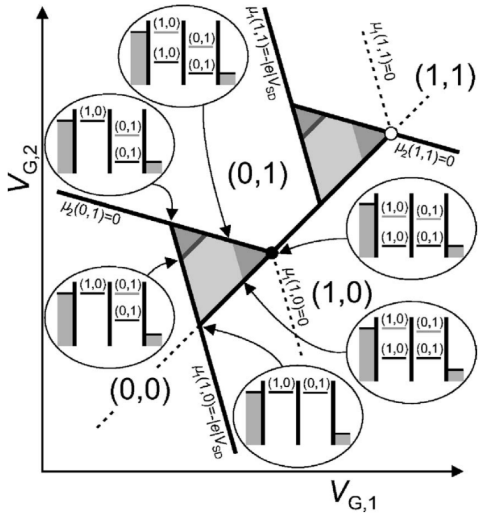


Figure 2.4: A triple points appearing in a DQD system at low temperature for a small V_{DS}. A triangle is formed from each triple point. Transport through the dot is energetically allowed only within this bias triangle and Coulomb blocked outside. Gray lines and regions in the triangles illustrate ($V_{G,1}$,$V_{G,2}$) at which transitions excited-state levels play a role. Electrochemical potentials corresponding to transitions involving an excited state are shown in gray in the level diagrams. Taken from [76].

and electrical confinement. The gate spacers provide the isolation from Source/Drain regions and serve as tunnel barriers and QDs are capacitively coupled to the gates [76]. Then, at low temperature, the phenomenon of Coulomb blockade determines the properties of transport (typically when the thermal energy is much smaller compared to the charging energy). Indeed, the Coulomb repulsion between charge carriers on the QD leads to an energy cost for adding an extra electron/hole to the dot and a precise control over the QD population can be achieved. Due to this charging energy, the charge carriers need to pay in order to tunnel from metallic leads onto a QD. The drain current becomes blocked if the electrochemical potentials within the double quantum dot system are not aligned as shown in Fig.2.4.

In Fig.2.4, a typical signature of transport through a double quantum dot in series is shown. At V_{DS} of few mV, resonant current through aligned electrochemical potentials results in pairs of triangles outside of which the transport is Coulomb blocked. It should be noted that upon increasing V_{DS}, the triangle tend to overlap, finally forming a single triangle at sufficiently high drain voltages. When decreasing V_{DS}, the triangles evolve into triple points.

Moreover, from the stability diagram analysis, the strength of coupling between two quantum dots can be deduced [76]. This coupling is parametrized by the mutual capacitance C_{12}. Generally, it is important to be able to finely tune this coupling in order to tune two adjacent quantum dots.

2.2.2 Theory of Pauli Spin Blockade in the presence of strong SOC

The Pauli exclusion principle leading to a spin blockade in semiconductor QDs was proven to be a powerful tool for read-out of the spin degree of freedom of single electrons [78, 79, 18]. More recently, PSB read-out technique was successfully used for CMOS electron [43] and hole [26] spin qubits fabricated with Leti's nanowire technology.

When a DQD is electrostatically tuned in the regime with the $(0, 2)$ occupation of QDs (or equivalent charge occupation such as $(m, n + 2)$ where m and n are integers) and the transition to $(1, 1)$ is probed, depending on whether V_{DS} is negative or positive, the spin blockade phenomenon might occur when external magnetic field is applied. It can be understood from Fig.2.5 (b): the transition from the energy lowest triplet state $T(1, 1)$ to the energetically allowed singlet state $S(0, 2)$ is forbidden and the resulting transport is blocked. However, depending on the hosting semiconductor

material, type of charge carriers (electrons, holes), and other parameters, the blockade can be lifted via different relaxation mechanisms. Indeed, depending on the dominant mechanism for mixing of blocked and allowed spin states, one can distinguish different manifestation of PSB. For PSB governed by hyperfine coupling, at zero magnetic field B_{ext}, a peak in leakage current appears. This is due to nuclear-field induced mixing between the unblocked singlet and the blocked triplet states [80]. Then, the current can be suppressed when a relatively small B_{ext} of typically few mV is applied. Another well-studied PSB mechanism is so-called spin-flip cotunneling which also manifests a peak at $B_{ext} = 0$ T. In this case, the second-order tunneling process allowing to exchange an electron with the source reservoir can result in an effective spin flip [81]. This spin relaxation mechanism is also suppressed at finite B_{ext}. In this case, however, typical critical field can reach few hundreds of mT since it is related to the electronic temperature in the source reservoir [37]. The third commonly reported mechanism of PSB is due to strong spin-orbit coupling (SOC). This mechanism will be studied for the first holes in silicon in the next subsection. Contrarily to electrons in III-V materials [82], electrons in silicon have weak SOC and PSB for them is typically governed either by hyperfine interaction or spin-flip cotunneling. A dip in current at zero B_{ext} for PSB governed by SOC mechanism can be understood in the following way [83]: by applying external magnetic field, the blocked triplet states start to mix with singlet $S(0,2)$ state and thereby the spin blockade is lifted via relaxation of different triplet states into $S(0,2)$ if magnetic field mixing blocked and unblocked states is applied as shown in Fig.2.5 (c). Another type of relaxation occurs between the blocked states (note that there are four blocked states due to the splitting of $T_{\pm}(1,1)$ in magnetic field) and is described by Γ_{rel} (relaxation to the ground state) [83].

2.2.3 Pauli Spin Blockade for the first holes: Experiment

In this section, we will investigate PSB for the first holes observed at 60 mK and 4 K using a p-type device with double gate in series as shown in Fig.2.2 (a). All the measurements for this samples were done with $V_{BACK} = 0$ V.

To achieve the base temperature T_{base} of 60 mK, we cooled down the device in an Air Liquide dilution refrigerator. This cryostat does not have the 1 K pot and the lowest temperature is reached when ^{4}He is pumped. We used home-made opto-isolated voltage sources to DC bias gates and

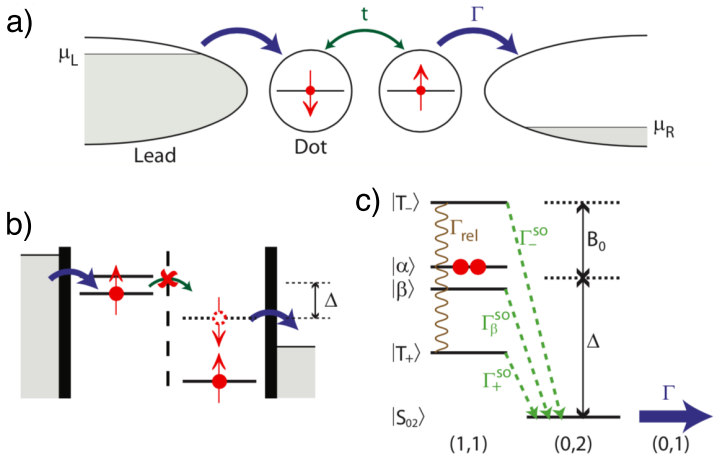


Figure 2.5: Double quantum dot in the Pauli Spin Blockade regime. (a) Illustration of transport through a DQD characterized by the strength of the tunnel interdot coupling t and the decay (relaxation) rate of the $S(0,2)$ Γ in PSB. (b) Due to the Pauli exclusion principle, the transport is blocked for $S(0,2) - T(1,1)$ transition. (c) Different energy levels and transition rates for non-spin-conserving interdot coupling. Taken from [83].

transimpedance amplifier to convert current into voltage and then read-out using a commercial digital multimeter. Typical electronic temperature T_{el} is somewhat higher that T_{base}. By fitting the Coulomb blockade resonance in similar nanowire devices, T_{el} was previously found to be around 200 mK. More details on the dilution refrigerator can be found in [84].

Since the proposal of Loss and DiVincenzo in 1998 [25] to make quantum bits based on spins confined in semiconductor quantum dots, substantial progress has been made. First, in III-V materials, where the maturity of growth techniques has allowed the emergence of top-down qubits based on the confinement of a two-dimensional electron gas in GaAs/AlGaAs heterostructures [76], but also bottom-up qubits made from nanowires (InAs or InSb) [85, 86]. In all III-V qubits, the dephasing time is limited by the interaction of the electron spin with the nuclear spins present in the host material [87, 88]. In contrast, silicon presents a low natural abundance of nuclear spins and can even be isotopically purified. It can be used to make electron spin qubits with extremely long dephasing time [89, 90, 33, 22]. An all-electrical control of single dot spin qubit by a single gate voltage microwave signal without the need of local magnetic field gradient would be a clear asset for future developments. Fast and local electrical manipulation using spin-orbit interactions has already been demonstrated in III-V

materials [85, 86]. Thus focusing on holes in silicon appears as an appealing strategy since holes present a limited hyperfine interaction [91] as well as a strong spin-orbit interaction (SOC) due to their p-orbital nature. Recent experiments [92, 93] have indeed revealed SOC-related spin properties and a hole spin qubit has even been demonstrated [26]. Here, we present a silicon hole double quantum dot based on the Leti nanowire technology. The device is tunable in the few hole regime in which we investigate Pauli spin blockade, the key ingredient for spin qubits initialization and readout in several qubit implementations [76]. More specifically, we focus on the magnetic field evolution of the leakage current through the device in the PSB regime. It reveals a dip around zero magnetic field linked to spin-orbit mixing [83]. The spin relaxation rates determined from the PSB are comparable with the values extracted for electrons in InAs nanowire double quantum dots [82] and are compatible with the operation of a hole spin-orbit qubit in silicon [26].

Our devices are nanowire field-effect transistors fabricated in a 300 mm CMOS facility on silicon-on-insulator wafers with 145 nm-thick buried oxide. The 11nm-thick Si channel is doped with $4 \cdot 10^{24}$ Boron m^{-3}. Regarding the previously described FEOL process flow, the low-dose channel implantation was done before patterning the active area as described in [72]. Nanowire width down to 18nm is achieved after patterning. Two gates (G1 and G2) in series are patterned by electron-beam lithography and are isolated from the channel by 2.5 nm of SiO_2 and 1.9 nm of HfO_2. Silicon nitride spacers are then deposited and etched on the sidewalls of the gates (see Fig.2.6 (a-b)). The spacers effectively protect the inter-gate spacing from the silicidation and dopant implantation used to reduce the access resistances [70]. The resulting structure, sketched in Fig.2.6 (c), yields a compact DQD with optimal gate control. At low temperature, two quantum dots, QD1 and QD2, are formed by accumulation below G1 and G2 respectively (see Fig.2.6 (c-d)). The same process has been used to produce n-type DQD [94].

The stability diagram shown in Fig.2.7 (a) reveals overlapped bias triangles [95] with vertical and horizontal edges. This is a characteristic of an excellent electrostatic control of each dot by one gate. The gate capacitances associated to G1 and G2, C_{G1} and C_{G1} are therefore the dominant capacitances and the lever arm parameters $\frac{C_{G1}}{C_{\Sigma 1}}$ and $\frac{C_{G2}}{C_{\Sigma 2}}$ are close to 1 ($C_{\Sigma 1} = C_{G1} + C_S + C_{12}$ and $C_{\Sigma 2} = C_{G2} + C_D + C_{12}$ are the total capacitances for QD1 and QD2, C_{12} being the capacitance between QD1 and QD2 and C_S (C_D) being the source to QD1 (drain to QD2) capacitance).

In order to precisely know (n, m)-the charge state with $n(m)$ the ex-

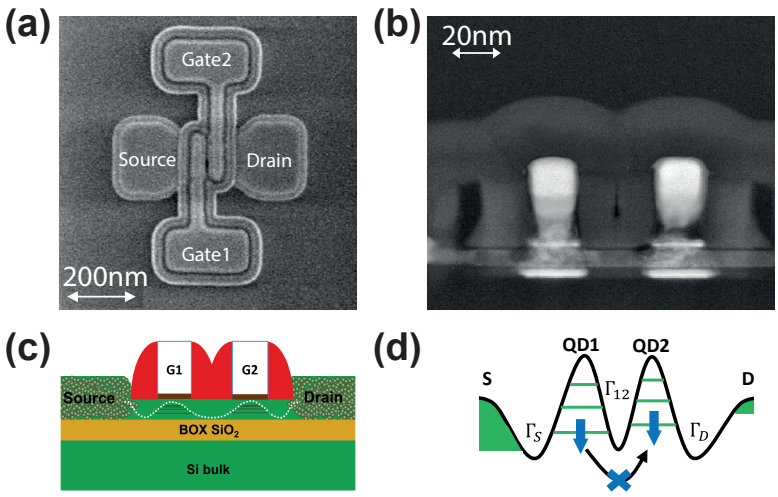


Figure 2.6: (a) Top view scanning electron micrograph of a typical DQD device after spacer etching, featuring the gates with the length of 30 nm separated by 35 nm. (b) Transmission electron micrograph along the source-drain axis. (c) Schematics of the DQD made by hole accumulation below G1 and G2. (d) Schematic Pauli spin blockade for the (1h,1h)→(0,2h) transition at reverse bias $V_{DS} \leq 0$, analogue to the (3h,3h)→(2h,4h) transition in the inset of Fig.2.9 (c). The black line is the top of the valence band. The green regions indicate the hole reservoirs in the source and drain.

cess holes in QD1(QD2), a large V_{DS} has been applied. Even if transitions $(1, m) \rightarrow (0, m + 1)$ and $(n, 1) \rightarrow (n + 1, 0)$ have not been detected at $V_{DS} = 20$ mV, they appear above $\mid V_{DS} \mid \approx 100$ mV thanks to the enhanced tunneling through the barriers under the spacers: the latter are markedly tilted at highV_{DS} so that the tunnel transparencies Γ_S, Γ_D increase significantly. In Fig.2.7 (a), the drain current recorded at $V_{DS} = -100$ mV is shown in a region where no current is detected at $V_{DS} = 20$ mV. This row of triangles corresponds to the second (1→2) transition in dot 2. The conducting parts of the triangles are replicated as a result of the ionization of dopants near the channel at large bias [96].

Interestingly, the charging energies are significantly larger in the few holes regime (up to 70 meV) than in the many holes regime ($\simeq$ 20 meV). We have, therefore, performed tight-binding calculations [97] in a realistic geometry in order to understand the nature of the very first low-lying hole states. The first few holes do not localize in edge states as in [74] because the channel is doped with Boron atoms and the back gate is grounded.

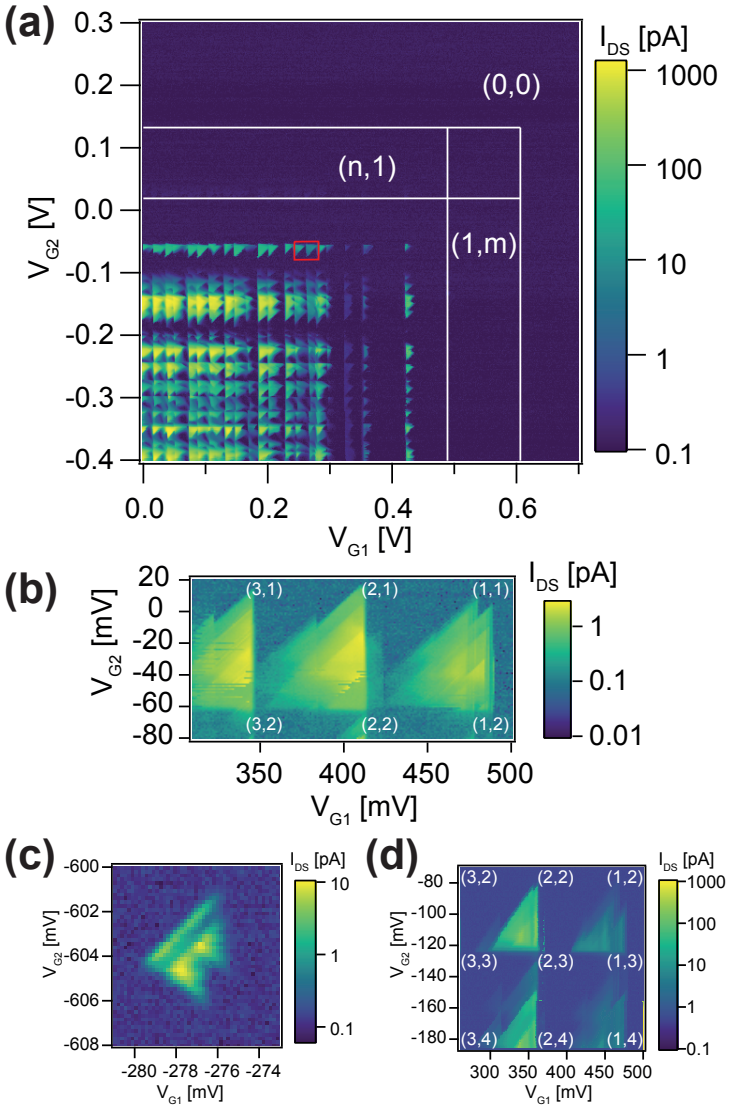


Figure 2.7: Stability diagrams obtained by sweeping V_{G1}, V_{G2} and recording I_{DS} at $T = 60$ mK. (a) $V_{DS} = 20$ mV. White lines indicate the position of four lines of current detected at larger bias (see b). The absolute hole occupation numbers are indicated for the few hole region. The red square indicates the region studied in Fig.2.8 (a). (b) $V_{DS} = -100$ mV. The region where no current was detected at $V_{DS} = 20$ mV ($(n, 1) \rightarrow (n, 2)$ transition line). (c) A typical pair of triangles obtained at $V_{DS} = -3$ mV in the many hole regime. (d) $V_{DS} = -70$ mV. The region where PSB was studied (see Fig.2.9) is shown. The absolute hole occupation numbers are indicated.

Therefore the holes are not pulled in the upper corners. They might rather be bound to clusters of two or more nearby Boron impurities which exist in the doped channel. Assuming a random distribution of Boron atoms, there is indeed $> 50\%$ (resp. $> 95\%$) chance of having at least two impurities closer than $d = 1.5$ nm (resp. $d = 2.5$ nm) under the gate. Configuration interaction calculations [74] show that such clusters show larger binding and charging energies E_c than single impurities ($E_c \sim 75$ meV at $d = 1.5$ nm and $E_c < 60$ meV when $d > 2.5$ nm). The charging energy decreases once the deepest clusters are filled and the confinement gets dominated by the structure and gate fields. Despite doping, the SOC is mostly mediated by the silicon matrix as the probability that the holes sit on the Boron atoms is always small.

Once the first holes are added in the channel, the DQD is defined by the geometry of the sample. We have simulated the stability diagram in the $(n, m) \geq (5, 3)$ regime with the orthodox Coulomb blockade theory. We solved the master equation for transport [98] with the parameters given in Table 2.1. In addition to the capacitances defined above, we set the electronic temperature T_e, as well as the tunneling rates Γ_S, Γ_D and Γ_{12} associated to C_S, C_D and C_{12}, respectively. The simulation shown in Fig. 2.9 (b), reproduces the shape of the measured bias triangles.

The value for C_{12} is deduced from the gate voltage separation ΔV_G between the triple points [95] observed at small V_{DS} (see Fig.2.7 (c)): $\Delta V_G = eC_{12}/C_{G1}C_{G2} \simeq 1.8$ mV. In addition, from Fig.2.7 (c) the first excited state is observed approximately 1 meV above the ground state similarly to what was reported for a similar n-type DQD device [94].

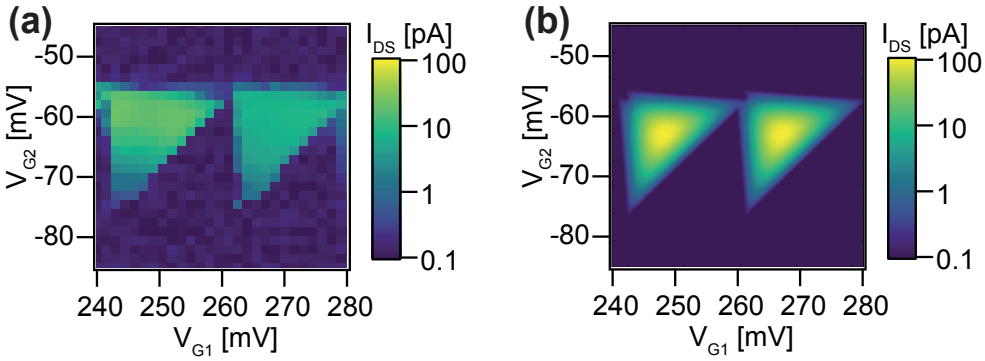


Figure 2.8: (a) I_{DS} versus V_{G1} and V_{G2} measured with $V_{DS} = 20$ mV at $T = 60$ mK (region highlighted in red in Fig.2.7 (a)). (b) Electrostatic simulations with the parameters given in table 2.1.

$T_e = 150$ mK
$C_{G1} = C_{G2} = 7.6$ aF
$C_S = C_D = 0.15$ aF
$C_{12} = 0.65$ aF
$\Gamma_S = \Gamma_D = \Gamma_{12} = 10^{-4}\ e^2/h$

Table 2.1: Numerical values used in the simulation of Fig.2.8 (b)

We now turn to the investigation of PSB. Spin blockade in a DQD arises when the current follows a transport cycle equivalent to $(0,1) \rightarrow (1,1) \rightarrow (0,2) \rightarrow (0,1)$ [99]. Since the $(0,2)$ ground state is a spin singlet, the cycle stops as soon as the DQD enters in a $(1,1)$ triplet state. The remaining leakage current results from spin relaxation or spin-orbit mixing mechanisms. Depending on the relevant mechanism, the leakage current will behave differently as a function of the magnetic field and detuning [83, 82].

Fig.2.9 (a - b) present current triangles in which PSB has been evidenced at $T = 60$ mK thanks to the magnetic field dependence of the drain-source current. As expected, a reduced current is detected at the base of the bias triangles [76] corresponding to the $(1,3) \rightarrow (2,2)$ transition in Fig.2.9 (a) and to the $(3,3) \rightarrow (2,4)$ transition in Fig.2.9 (b), respectively. Fig.2.9 (c - d) displays the leakage current as a function of the out-of-plane magnetic field, B_{ext}, and of the detuning axis in the PSB regime of Fig.2.9 (a) and Fig.2.9 (b), respectively (detuning axis are indicated by white arrows in Fig.2.7 (a) and (d). The leakage current decreases around $B_{ext} = 0$ in both cases. The current does not depend on magnetic field for the reverse polarity ($V_{DS} < 0$) as well as for the two other triangles shown in Fig.2.7 (d), i.e. for $(3,2) \leftrightarrow (2,3)$ and $(2,3) \leftrightarrow (1,4)$ transitions. Note here that the $(1,1) \rightarrow (0,2)$ transition - at which PSB is also expected - was not caught even at large bias.

A cut at zero detuning taken in Fig.2.9 (c) and 2.9 (d) is shown in Fig.2.9 (e) and in Fig.2.9 (f), respecively. It reveals a current dip which can be fitted to a Lorentzian function, in line with a model assuming both strong SOC [83]:

$$I = I_{max}(1 - \frac{8}{9}\frac{B_C^2}{B_C^2 + B^2}) + I_0 \tag{2.1}$$

with $I_{max} = 4e\Gamma_{rel}$ the dip height, where Γ_{rel} is the spin relaxation rate among the $(1,1)$ states, B_C is the dip width and I_0 is a B-independent background current [92] (0.15 pA for the (1,3)$\rightarrow$(2,2) transition and 1.3 pA

for the (3,3)→(2,4) transition). B_C accounts for the cross-over between leakage currents resulting from spin relaxation at small field and spin-orbit mixing at higher field. The rate Γ_{SO} of spin-orbit mixing between $(1,1)$ states and the $(0,2)$ singlet can be estimated with:

$$g\mu_B B_C \simeq h\sqrt{\Gamma_{rel} \times \Gamma_{SO}} \tag{2.2}$$

Contrarily to what has been reported in [100, 92], we always see a dip of current at a low magnetic field that we attribute to the dominance of spin-orbit mixing over hyperfine [82] or spin-flip cotunneling mechanisms [100, 37]. We also observe two current peaks at $B = \pm 20$ mT and $T = 60$ mK (see Fig.2.9 (c) and (e)). Peaks of current at finite magnetic field, whose origin remains unclear, are also reported in references [101, 100, 102]. Recently, Zarassi and the colleagues developed a theory explaining a double-peak structure in the magnetic field [103]. With simulations and experiment, they argued that this complex structure might appear for a given DQD configuration depending on Γ_{rel} and Γ_{SO}. The dip observed at zero magnetic field extends in detuning up to several meV, which indicates that the $(0,2)$ singlet-triplet splitting in our QDs - as other orbital splittings - is large. As a result, PSB can be seen even at $T = 4.2$ K which will be shown later.

Γ_{rel} and Γ_{SO} can be estimated from the above experiments. For two QDs in series, Γ_{SO} mainly depends on the interdot coupling. The hole g-factor was found to be anisotropic in similar nanowire transistors [93], with g =1.5 - 2.6. Then, Eq. (2.2) yields $\Gamma_{SO} = 1.4-4.3$ meV for the (1,3)→(2,2) transition and $\Gamma_{SO} = 0.6 - 1.8$ meV for the (3,3)→(2,4) transition. The spin relaxation is dominated by the spin-orbit coupling in our DQD rather than by hyperfine effects. Indeed, we estimate a fluctuating Overhauser field [104] $B_{nuc} \approx 20\mu$T, which is much smaller than the current dip width of $10-20$ mT [100, 93]. Γ_{SO} is larger than in previous reports [82, 92] while the critical field B_C is comparable to that of refs. [82, 100] (for electrons) and smaller than in refs. [102, 92] (for holes). This can be attributed to the small value of Γ_{rel}. A large Γ_{SO} can limit qubit readout fidelity through unwanted transitions from $(1,1)$ triplet to $(0,2)$ singlet [105] and it would be favorable to reduce the interdot coupling.

$\Gamma_{rel} = 120$ kHz (resp. 2.0 MHz) for the (1,3)→(2,2) (resp. (3,3)→(2,4)) transition is smaller than in previous reports [82, 100, 102, 92] where it ranges between 0.8 [100] and 6 MHz [105] (3 MHz in ref. [92], $I_{DS} = 6$ pA for $B \geq B_C$ in [102]). Γ_{rel}, which limits the inelastic relaxation time T_1, should be primarily minimized for hole spin-orbit qubits. Contrarily to Γ_{SO}, Γ_{rel} cannot be adjusted by changing the interdot coupling and its optimization is material and process dependent.

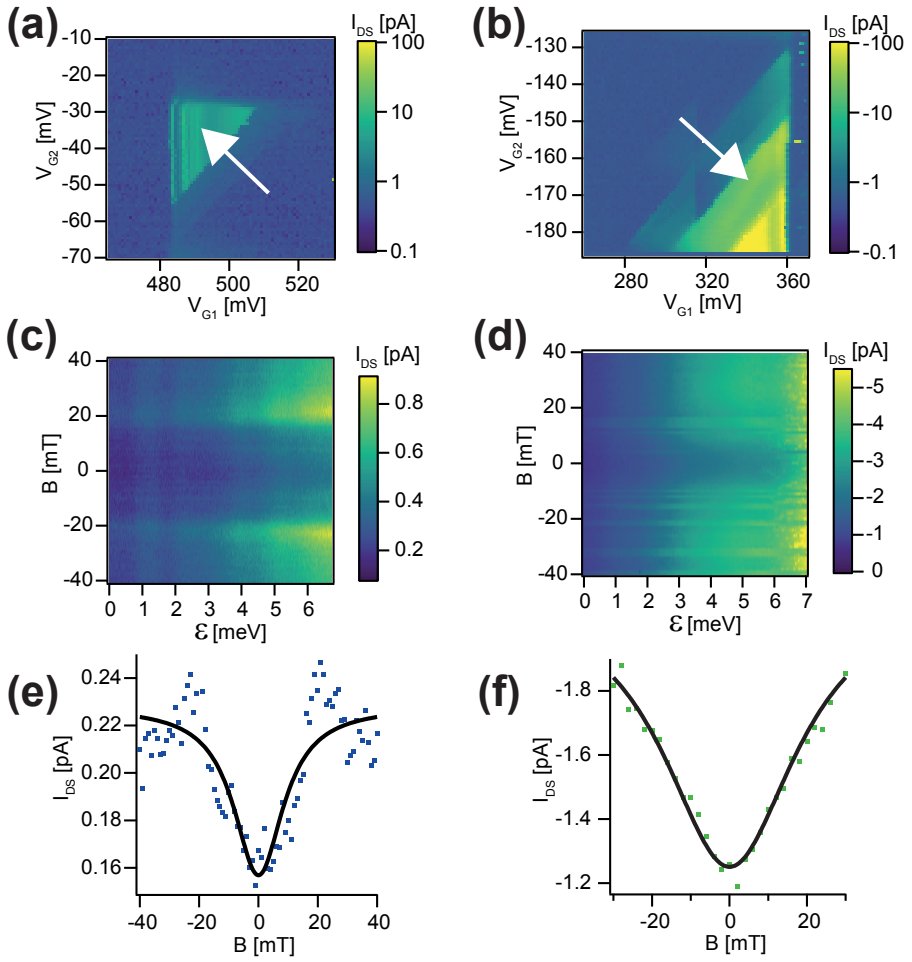


Figure 2.9: Current in the PSB regime as a function of detuning and out-of-plane magnetic field B_{ext} at $T = 60$ mK. (a) Drain current versus V_{G1} and V_{G2} at $V_{DS} = 70$ mV and $B_{ext} = 0$. (b) Same as in (a) except for $V_{DS} = -70$ mV. (c) Current versus detuning energy ϵ and magnetic field for the (1,3)→(2,2) transition (white arrow in a)). (d) Same as in (c) but for the (3,3)→(2,4) transition (white arrow in b)). (e) and (f) are cuts of the (1,3)→(2,2) and (3,3)→(2,4) transitions at $\epsilon = 0$. The curves are fitted (black lines) assuming that PSB is spin-orbit mediated [83].

Given that it is desirable to have silicon spin qubits operating at a higher temperature (ideally above 1 K), we measured the same (1,3)→(2,2) transition at $T = 4$ K. The same dip-behavior but this time with no double-peak structure is shown in Fig.2.10 (a - b). By fitting the cut at $\epsilon = 0$ in the

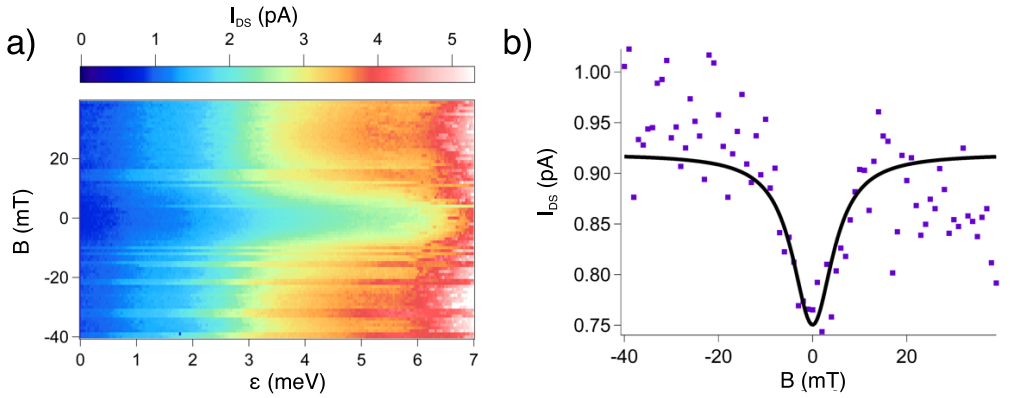


Figure 2.10: (a) Current in the spin blockade regime as a function of detuning and out-of-plane magnetic field B_{ext} for the (1,3)→(2,2) transition at $T = 4$ K. The dip in the current near zero magnetic field can be seen. Two symmetric peaks at ±20 mT observed for this transition at 60mK have disappeared. (b) Current at zero detuning versus magnetic field. The black line represents the fit.

same way as it was done previously, we find the set of parameters given in table 2.2. As the temperature is increased it is expected an increase of Γ_{rel}. Nevertheless, its value is well below few MHz obtained for silicon DQD in the many hole regime at $20 - 50$ mK temperature [26, 92]. In addition, the decay rate Γ_{SO} is reduced at 4 K due to narrower dip and lower B_C. It can be explained by the temperature-increased Γ_{rel} competing with Γ_{SO} [83].

To conclude, the few-hole regime has been reached in a silicon CMOS DQD and Pauli spin blockade has been observed at different charge transitions. We found that this blockade is dominated by the SOC. By analyzing the magnetic field evolution of the leakage current in the blockade regime we deduced a small intradot spin relaxation rate (≈120 kHz for the first

(1,3)→(2,2)	$T = 60$ mK	$T = 4$ K
I_0	0.15 pA	0.73 pA
B_C	10.23 mT	5.23 mT
Γ_{rel}	0.49 neV (120 kHz)	1.23 neV (297 kHz)
Γ_{SO}	1.5 meV (363 GHz)	0.168 meV (40.6 GHz)

Table 2.2: Parameters of PSB for the (1,3)→(2,2) transition at $T = 60$ mK and 4 K obtained by fitting the current dip at $\epsilon = 0$ using Eq.2.1

holes), an important step towards a robust hole spin-orbit qubit.

2.2.4 P-type quantum dots with electrostatically controlled tunnel coupling

An effective way to improve the coherence time of the hole spin qubit demonstrated in [26] consists in reducing the coupling to Souce/Drain regions by tuning the access tunnel barriers. In addition, decoupling from S/D has been proven to be an efficient technique for similar 3-gate-in-series devices to reduce Γ_S and Γ_D and isolate the DQD [50].

This decoupling mechanism has been achieved by adding two additional access gates (G1 and G4) as shown in Fig.2.11 (a). The sample consists in four gates in series with the same channel doping as in the previous section. The geometrical parameters are given in Fig.2.11 (a). The tunability of the corresponding potential barriers is demonstrated in Fig.2.11 (b - d) where the resonant current through the central DQD confining holes is plotted as a function of gate voltages (V_{G2},V_{G3}) for different values of V_{G1} and V_{G4}. A stability diagram for the DQD created with G2, G3, was recorded at 4 K and was found to be similar to the double gate p-type device presented in the previous subsection (not shown here). Again, the first holes regime was not accessible at low V_{DS}. For the chosen triple point in the many holes regime which also exhibits PSB (not shown), the tunability analysis was performed. The current level decreases upon increasing the voltages V_{G1} and V_{G4}, following enhancement of the access tunnel barriers. Varying V_{G1} and V_{G4} does not affect the (V_{G2},V_{G3}) position of the current resonance, indicating that the electrostatically defined DQD is not affected by parasitic cross-capacitances.

Although only symmetrical $V_{G1} = V_{G4}$ are shown in Fig.2.11 (c - d), we analyzed asymmetric barrier lowering by separately biasing V_{G1} and V_{G4}. Very weak dependence on Γ_S of resonant current through DQD was found. It can be explained by the theory of resonant tunneling via two discrete states explained in [106]. Basing on this theory, I_{DS} is given by:

$$I_{DS} = et^2\Gamma_D/(t^2(2 + \Gamma_D/\Gamma_S) + \Gamma_D^2/4 + (\epsilon - \Delta E)^2/\hbar^2) \qquad (2.3)$$

where t is the interdot coupling, ϵ the detuning, ΔE the energy splitting between the ground and the excited states. Thus, from Eq.2.3 it is obvious that the major decay rate governing the drain current is imposed by the decay rate to escape from QD2 to Drain.

Additionally, we could achieve similar DQD configurations using G1, G2, and G1, G3 and stability diagrams revealed an excellent electrostatic

gate control (not shown). The last configuration is of particular interest as the intermediate gate can be used to control the exchange coupling between adjacent qubits as explained in Chapter 1.

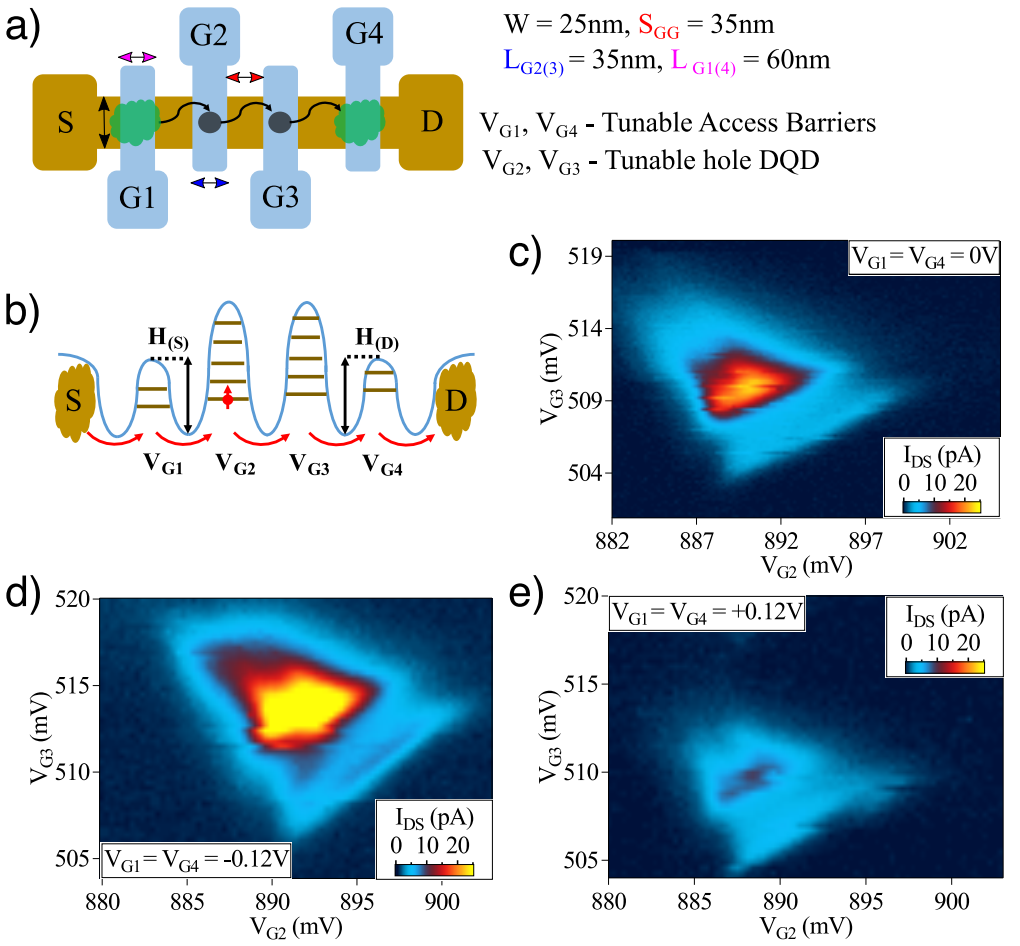


Figure 2.11: PMOS NW MOSFETs with four gates in series: (a) 2D sketch of the device (b) Operation principle based on the access gates (G1, G4) tuning the access barriers (H_S, H_D) of a hole double quantum dot created with the inner gates (G2, G3). The tunability of the same triple point at 1.4 K is shown. The triple point without any voltages applied on Access Gates is given on (c). (d) Access barriers are symmetrically lowered by applying $V_{G1} = V_{G4} = -0.12$ V and as a result higher I_{DS} is observed. (e) Access barriers are symmetrically raised by applying $V_{G1} = V_{G4} = 0.12$ V and then I_{DS} is suppressed.

2.3 Back-gate tunable QDs and Coulomb spectroscopy of the first electrons

2.3.1 N-type Corner Dots under zero and reverse body-biasing

In this subsection, we will demonstrate electron quantum dots confined in the edges of silicon nanowire within the Face-to-Face geometry (see Fig.2.2 (b)). First, the potential of such QDs for electron spin qubits with all-electrical control through EDSR will be presented. Then, low-temperature characterization of CDs of different samples and supported by simulations will be presented.

The quantum dots defined in the edges of n-type silicon nanowire MOSFETs with F-to-F geometry were already reported in [74]. Most recently, such electron QDs have gained an increased interest due to the possibility to explore EDSR mechanism for coherent control of the electron spin despite weak SOC for electrons in silicon [27].

Here, the EDSR-experiment for electrons (reported in [27]) using the geometry shown in Fig.2.2 (d) is described in [31]. As shown in [74], electron localization occurs along the upper edges of the mesa (silicon nanowire). We consider two QDs, QD1 and QD2 confined in the corners' defined by the gates G1 and G2. If both electrons are in the same spin state (e.g. parallel spins, which is the ground state in a finite magnetic field B), PSB prevents charge movement from QD1 to QD2. However, a spin rotation obtained by applying a resonant RF electrical field to G1 will lift PSB and thus will induce a non-zero current. Yet for electrons in Si, the additional valley degree of freedom needs to be considered. The conduction band of bulk Si features six degenerate Δ valleys. Structural and electrical confinement in our device, however, leaves two lowest energy valleys ν_1 and ν_2, separated by an energy $\Delta\nu$. From these two valleys, four distinct states can be resolved upon applying a static magnetic field B: $|\nu_1,\downarrow\rangle$, $|\nu_1,\uparrow\rangle$, $|\nu_2,\downarrow\rangle$, $|\nu_2,\uparrow\rangle$.

Then, the two states $|\nu_1,\uparrow\rangle$ and$|\nu_2,\downarrow\rangle$ can be mixed if the inter-valley spin-orbit coupling coefficient $C_{\nu_1\nu_2}$ in the Hamiltonian is non-zero. As illustrated in Fig.2.12 (a), this criterion is fulfilled if the mirror symmetry of the electron wavefunction with respect to the (XZ) plane is broken [107, 27]. The partially overlapping top gate leading to the 'Corner Dot' confinement is, therefore, the key to spin-valley-orbit mixing in this case.

As magnetic field is increased and the spin splitting $E_Z = |g|\mu_B B$ approaches the valley splitting Δ_V, the $|\nu_1,\uparrow\rangle$ and $|\nu_2,\downarrow\rangle$ energies may either cross ($C_{\nu_1\nu_2} = 0$) or anticross ($C_{\nu_1\nu_2} \neq 0$). In the case of anticrossing shown

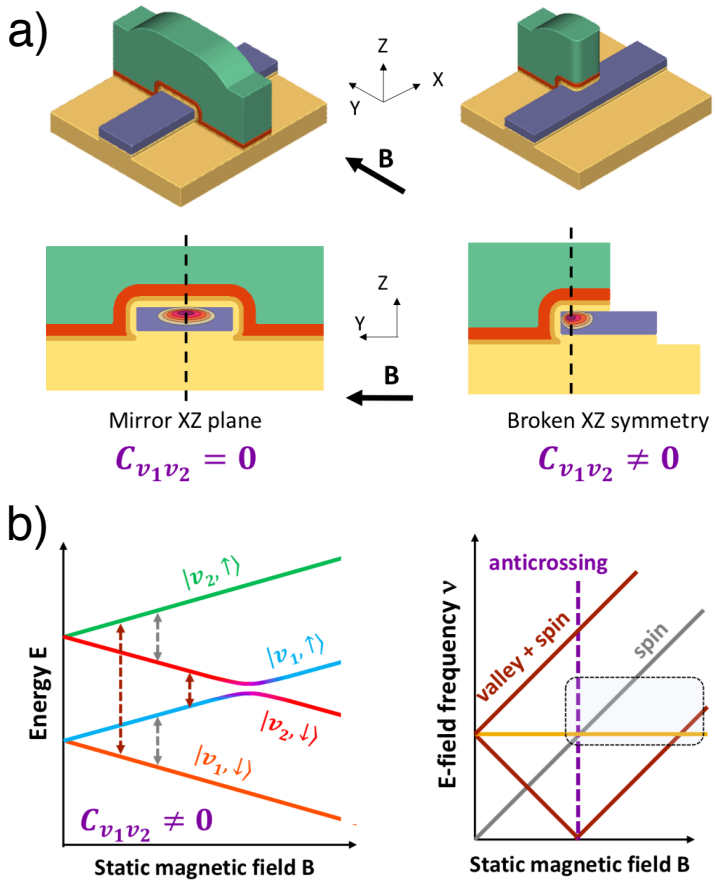


Figure 2.12: (a) Impact of device geometry on inter-valley SOC. The coupling term $C_{\nu_1\nu_2}$ is non-zero if the symmetry of the electron wavefunction with respect to the (XZ) plane is broken. This condition is fulfilled in the case of Corner Dots. (b) Zeeman splitting from ν_1 and ν_2 when the inter-valley SOC exists and states anticross is shown on the left and the EDSR spectrum on the right. The dotted frame highlights the region experimentally measured in [27]. Adapted from [31].

in Fig.2.12 (b), due to states mixing near the anticrossing, B-dependent spin/valley transition diagonals due to RF E-signal can be seen. They result in EDSR-driven electron spin resonance [27].

Therefore, in this thesis, we studied the corner dots in the Face-to-Face geometry under different body-biasing conditions. Two similar samples without (F-to-F #1) and with (F-to-F #2) channel doping were cooled down to 4.3 K. Both devices have the same $W = 45$ nm and $S_{FF} = 30$ nm and slightly different gate length : $L_G = 50$nm for the undoped device and

70nm for As-doped channel device (2×10^{18} cm^{-3}) (see Fig.2.13 (a)).

In this section, to simulate CDs, we used the effective mass approximation to compute the wavefunctions and the addition energies. The potential in the system was computed using a 3D Poisson solver, including surface roughness (SR), individual dopants and remote Coulomb scattering (RCS). We then took into account electrons interactions using the Configuration Interaction method [108], to compute the many-particles energies. From this, the average number of electrons in the system was calculated using the grand canonical ensemble.

In Fig.2.13 (b), the electron wavefunction calculated for the geometry of F-to-F #2 is shown. It should be mentioned that although we analyze CDs under reverse body-biasing with $V_{BACK} = -8$ V, a similar behavior of quantum dots confined in the corners was also observed at zero V_{BACK} as reported in [69].

4 K stability diagrams for both devices are shown in Fig.2.13 (c - d) featuring two uncoupled corner dots beneath G1 and G2 (no anticrossing between parallel vertical and horizontal lines of resonant current, close to zero C_{12}). An important feature of these NMOS devices is that the first electrons at 4 K start to populate CDs at gate voltages close to $V_{TH}(300K)$.

In Fig.2.13 (e - f), Coulomb diamonds of corner dots are shown for both devices. Large addition energies can be visible in both cases. For the doped channel device, the energy to add the first additional electron is surprisingly high and exceeds 35 meV.

To understand such high E_{ADD}, we introduced different types of disorder in the simulations and we analyzed the following cases:

- No disorder (ref.): maximal E_{ADD} up to 24.5 meV;

- Surface Roughness (SR): for Si/SiO_2 interface with realistic correlation length $L_c = 1.5$nm and rms $\Delta_{SR} = 0.35$ nm [42] calibrated on 300 K mobility measurements [109], E_{ADD} can reach 32 meV;

- Surface Roughness and Remote Coulomb Scattering (SR+RCS). We found slightly higher $E_{ADD} = 34$ meV by considering the same parameters for SR and accounting for 2×10^{13} cm^{-2} positive charges at the SiO_2/HfO_2 interface [109, 110].

- Dopants in the channel without SR and RCS: addition energies up to 60 meV can be found due to the dopant-assisted confinement as explained in the section on PSB for the first holes;

The simulated stability diagram with up to 3 additional electrons put on each CDs shown in Fig. 2.14 (a), agrees the experiment. From the Coulomb-spectroscopy, we could extract the addition energies for the first electrons as well as the lever arm parameters for both devices. A remarkable conclusion from the experimental data is : (i) very large E_{ADD} for both

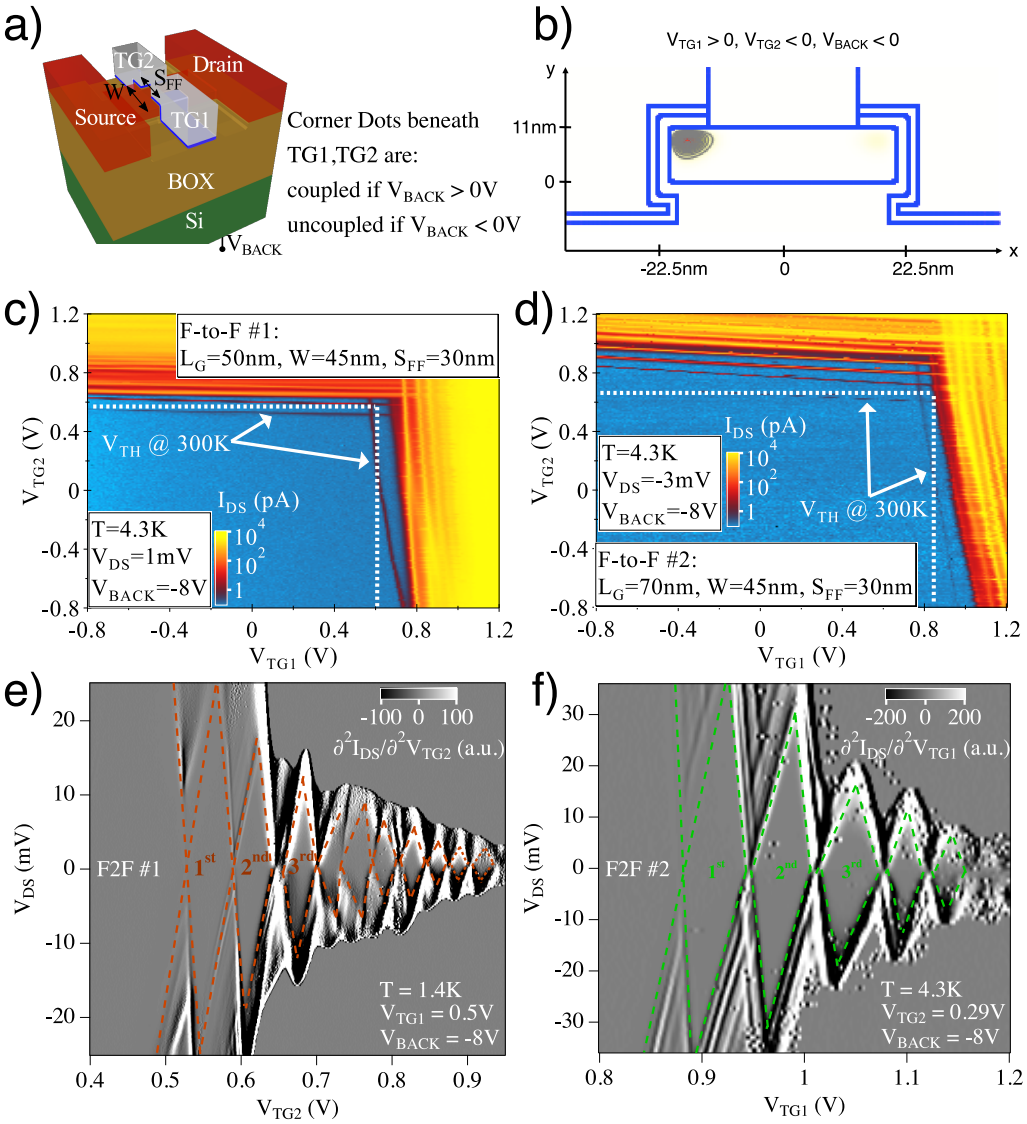


Figure 2.13: (a) A 3D sketch of n-type F-to-F device. (b) The wavefunction for a corner dot defined below G1 at $V_{BACK} = -8$ V obtained from realistic simulations accounting for the real device geometry. (c)-(d) Stability diagrams for two F-to-F devices with doped and undoped channel recorded at 4.3 K. Geometrical dimensions are given in the inserts. (e)-(f) Coulomb spectroscopy for the first electrons. $V_{DS} - V_{TG1,2}$ are plotted as a function of $\partial^2 I_{DS}/\partial^2 V_{TG2,1}$.

devices, (ii) for the undoped device, the experimental value is close to the one obtained from simulations without the disorder. It means that the first

electrons are very likely to be confined thanks to the electrostatic and are not imposed by stochastically distributed disorder in the channel. In case of the doped channel device, E_{ADD} for the first electron is above the reference value and those obtained with SR+RCS. It probably signifies that the first two additional electrons are confined due to the dopants close to the edges of the nanowire.

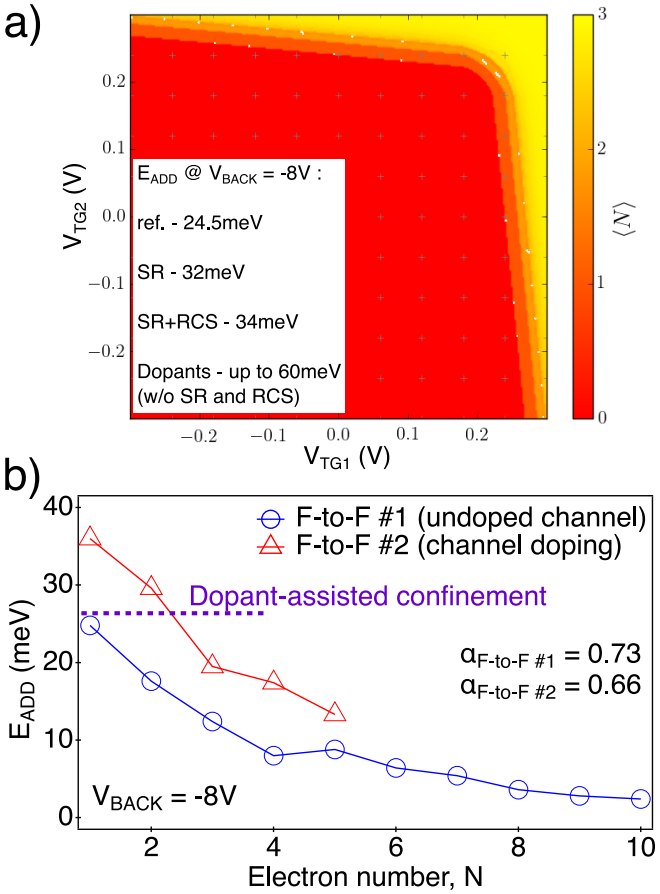


Figure 2.14: (a) Simulated stability diagram for the geometry of F-to-F #2 for $V_{BACK} = -8$ V. The shape reproduces well the experimentally observed pattern. The insert shows E_{ADD} for different types of disorder introduced in the system. (b) The addition energies are extracted for the undoped and doped channel devices from Fig.2.13 (e - f). The threshold value indicating the energy above which the electrons are most likely confined on the dopant-assisted QDs from the simulations results in (a).

2.3.2 Dopant-assisted QDs under forward body-biasing

In order to capacitively couple the QDs created in F-to-F n-type devices, we decided to apply forward body-biasing in order to bring close the wavefunctions of electrons defined by G1 and G2 as it was suggested with simulations in [69]. Indeed, the possibility of tuning the interdot coupling would be a great asset for large-scale parallel arrays of F-to-F gates [69]. In addition, the tunability of CDs with body-biasing is crucial for all-electrical manipulation of electron spin qubits based on spin-valley mixing [41] as valley splitting was demonstrated to be tunable with V_{BACK} in similar nanowire devices [42].

Here we will explore the regime of FBB when the electron wavefunctions are pulled towards Si/BOX interface and a CD transforms into a usual QD. For F-to-F #1 with arsenic-doped channel, several stability diagram evolution steps happen when V_{BACK} is increased from +12 to +30 V as

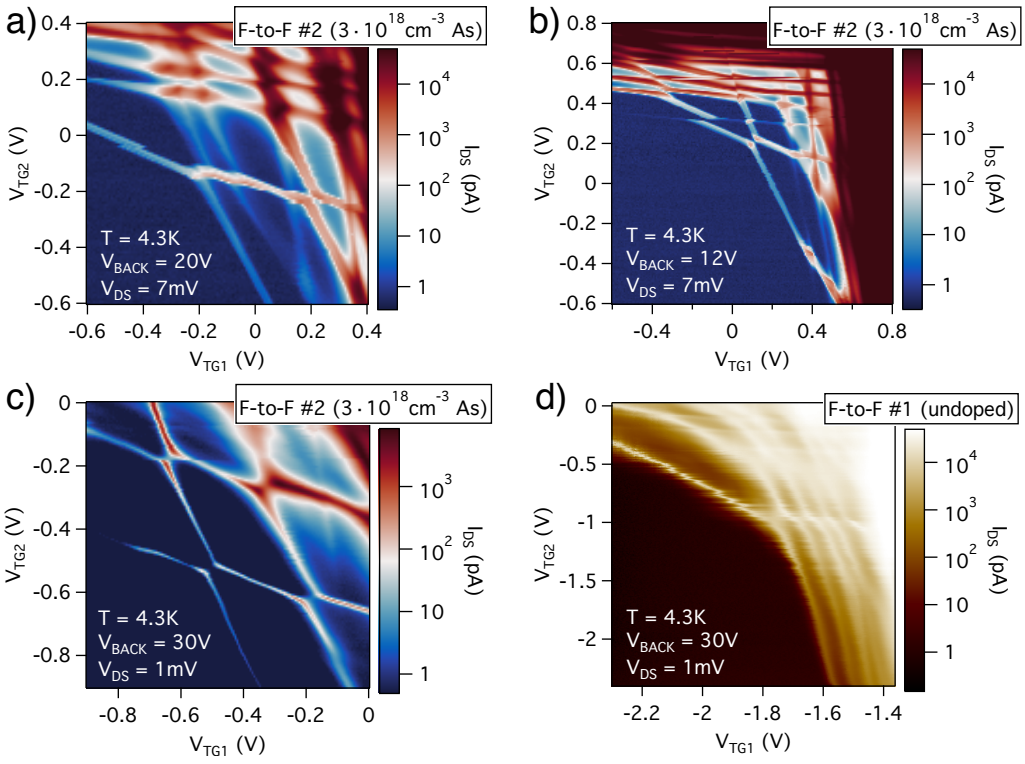


Figure 2.15: (a) - (c) Evolution of 4 K stability diagrams for different FBB voltages up to +30 V in the case of doped channel F-to-F device. (d) Stability diagrams for the undoped channel device at $V_{BACK} = +30$ V.

shown in Fig.2.15 (a - c):

- for intermediate $V_{BACK} = +12$ and $+20$ V different multi-dots in the channel are created featuring double or triple quantum dots due to the dopants.

- at $V_{BACK} = +30$ V the desirable DQD configuration is obtained. The DQD can be populated up to $(2, 2)$ charge configuration.

However, at the highest FBB voltage, the addition energies for the first electrons are very high and reaches 58 meV as deduced from the Coulomb spectroscopy in Fig.2.16 (b). Such degree of confinement cannot be explained by our simulations including a different type of disorder and must be related to confinement on dopants as it was reported for a cluster of six phosphorus dopants in STM-defined silicon QD [111]. In addition, a different signature for initially undoped F-to-F #2 was observed with asymmetric quantum dots below G1 and G2 as shown in Fig.2.16 (d). In this case, under G1, a quantum dot with addition energy close to the values reported for CDs are observed whereas a similar E_{ADD} for the QD under G2 can be visible.

To gain a better understanding of such unexpected behavior, since the confinement on a single dopant cannot give such high charging energies and it is unlikely to achieve the double occupation of the same arsenic atom, we performed simulations of stability diagram for $V_{BACK} = +30$ V. In these simulations, two clusters of four As dopants were put at the Si/BOX interface. The electron wavefunction is pulled towards this interface when FBB is applied. For such artificial clusters separated by 28 nm and located symmetrically in the channel, we could obtain a similar stability diagram revealing E_{ADD} up to 100 meV for the first electrons as shown in Fig.2.16 (a).

Therefore, now we can associate the patterns observed for the channel-doped device to the confinement on the clusters of arsenic at very aggressive FBB ($V_{BACK} = +30$ V). For the undoped device in Fig.2.15 (d), we conclude that one of the QDs (below G2) is also linked to the confinement due to residual/diffused dopants from S/D regions. We conclude that for reproducible and similar NMOS F-to-F devices which are building blocks for electron spin qubits, particular care of residual channel doping and thermal budget must be taken.

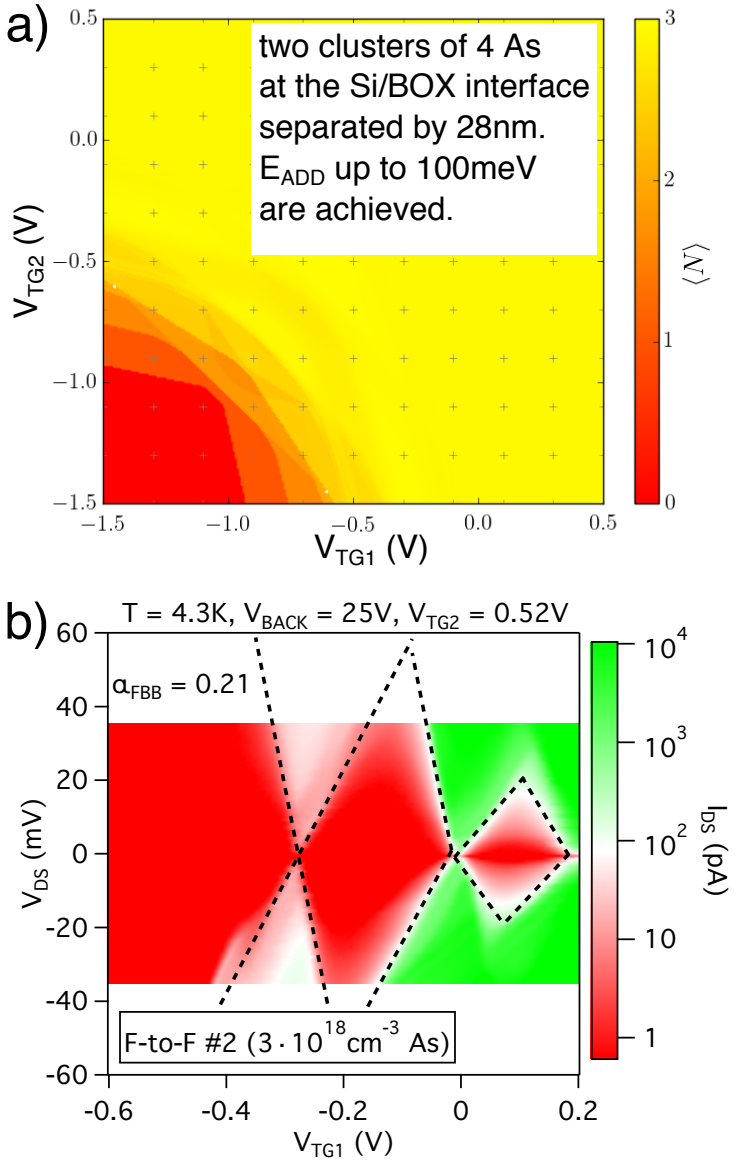


Figure 2.16: (a) Simulated stability diagram at $V_{BACK} = +30$ V. To achieve DQD pattern, two artificial As-clusters were put in the channel allowing us to reproduce both the shape of experimental stability diagram in Fig.2.16 (c) and the high E_{ADD} in (b). (b) The Coulomb spectroscopy analysis for high FBB voltage revealing $E_{ADD} = 58$ meV which is consistent with the confinement on a cluster of dopants. Note that the lever arm parameter is much lower as the strength of coupling to the front gates is reduced.

2.4 Towards scalable electron spin qubits with Corner Dots

In this section, we present low-temperature characterization of a 4 gate n-type F-to-F device with two additional access gates. The SEM image after gate patterning is shown in Fig.2.2 (f). The geometrical dimensions of the device are: $L_{AG1,2} = L_{TG1,2} = 40$ nm, $W = 60$ nm, $S_{GG} = S_{FF} = 35$ nm as shown in the sketch in Fig.2.17 (a). The sample was measured at $V_{BACK} =$ 0 V at low temperature using a Cryoconcept wet dilution refrigerator with $T_{base} = 15$ mK.

By adding two additional 'access' gates to the Face-to-Face geometry (see Fig.2.2 (a)), we obtain a good candidate for a two-qubit logic whose possible operation principle can be the following:

- Corner dots defined with TG1 and TG2;

- Coupling between two CDs is modulated by back-biasing;

- Both CDs are manipulated via EDSR [27] and then read using AG2 through Pauli Spin Blockade;

- Two qubits can be coupled/uncoupled from the source region using AG1;

In order to validate the proposed approach, we demonstrate two distinct regimes of operation with the access gates used to create artificial S/D reservoirs (Fig.2.17 (c) and (e)) or read-out QD (Fig.2.17 (d) and (f)) depending on the applied voltages.

Indeed, when the source access barrier is open with $V_{AG2} = 1V$, $V_{AG2} >$ 0.58 V, and $V_{TG2} = 0$, a corner dot is formed below TG1 by applying positive V_{TG1}. In this scenario, we artificially obtain transport through a single quantum dot coupled with semi-metallic dots below AG1 and AG2 (see the regime (I) in Fig.2.17 (f)). Similarly, the same operation can be achieved for a CD below TG2, thus resulting in a usual F-to-F stability diagram as shown in Fig.2.17 (e).

However, if $V_{AG2} < 0.58$ V and $V_{AG2} = 1V$, we obtain a DQD configuration with a small CD below TG1 coupled to large quantum dot accumulated with AG2 (see the regime (II) in Fig.2.17 (f)). Coupling down the device to 15 mK in this voltage configuration, we observe a well-resolved pair of triangles indicating transport through two dots in series.

Finally, in this section, we demonstrated the versatility of multi-gate geometry for which different QD configurations can be achieved and a two-qubit gate can be demonstrated.

2.5 Conclusions

In this chapter, we described the fabrication of SOI nanowire multi-gate devices fabricated with conventional high-κ metal gate and present room temperature characterization of multi-gate architecture for silicon spin qubit applications.

Using a p-type double gate transistor used to demonstrate the hole spin qubit functionality in the many hole regime [26], we studied Pauli spin blockade (PSB) for the first holes and compared its behavior at 4 K and 60 mK. We find that PSB is mediated by spin-orbit coupling as expected for holes in silicon. By analyzing the magnetic field evolution of the leakage current in the blockade regime, we observed a small intradot spin relaxation rate ($\approx$120 kHz for the first holes) which limits T_1 relaxation time.

For the four gates in series PMOS device, we demonstrated an efficient electrostatic tunability allowing to couple/decouple an inner DQD from the Source/Drain regions.

Regarding the importance of the electron quantum dots confined in the corner edges (CDs) of the silicon nanowire, we analyzed and quantified CDs in terms of addition energies (E_{ADD}) and lever arm parameter for the first electrons in different n-type samples. Our analysis is supported by realistic simulations based on the effective mass approximation used to compute the electron wavefunctions and E_{ADD} as well as the constant interaction method to estimate the average number of electrons (up to three additional electrons) in the system. We found a good agreement between the experimentally observed addition energy and the simulations without the disorder, thus we argued that the CDs are electrostatically defined and not due to disorder. By performing forward body-biasing analysis, we revealed a double quantum dot occupation on clusters of arsenic dopants for the sample with channel doping and reproduce the experimental stability diagrams with simulations.

Within a more elaborated F-to-F geometry upon adding two additional access barriers, we showed the versatility of this geometry allowing to have several DQD configurations. Based on these results, we proposed a protocol for a two-qubit logic gate using this geometry.

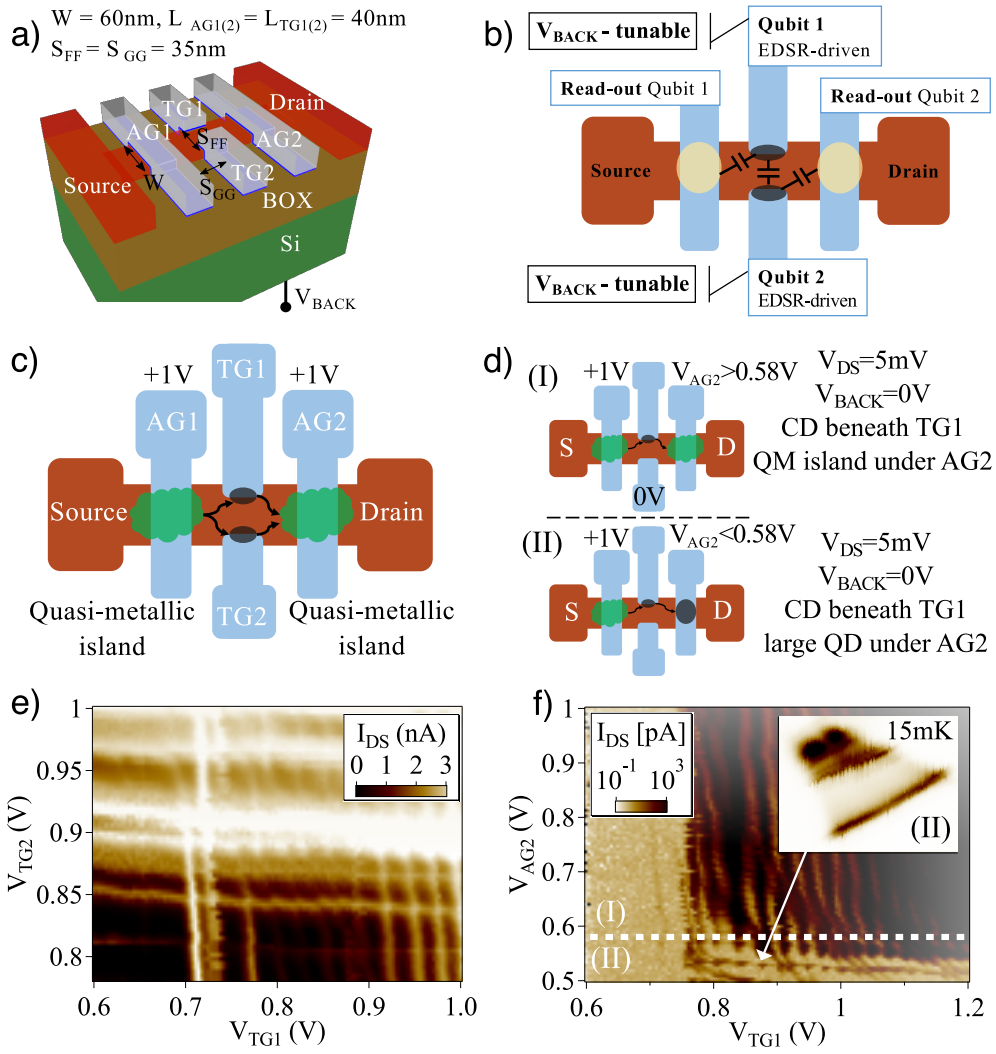


Figure 2.17: (a) 3D sketch of an electron Face-to-Face with tunable Access Gates. (b) The operation principle of using this geometry for CMOS two-qubit gate.(c) Sketch of a system with two CDs defined beneath TG1 and TG2 and surrounded by two quasi-metallic islands formed when V_{AG1} and V_{AG2} are positive enough. The corresponding 4 K stability diagram is shown in (e). (d) Illustration of two different regimes depending on V_{AG2} experimentally observed in (f) at 4 K: if V_{AG2} is positive enough, we have a metallic island next to the CD, otherwise transport through a double quantum dot in series occurs. The insert of (f) demonstrates two partially overlapped triangles which are a typical signature of transport through DQD at finite bias voltage at $T = 15$ mK.

Chapter 3

Digital and Analog performance of 28 nm FD-SOI MOSFETs down to 4 K

In this chapter, a simplified process flow for the fabrication of high-κ metal gate 28 nm FD-SOI MOSFETs is given and an excellent room temperature (RT) variability is demonstrated for short-channel devices. Two different well architectures for regular (RVT) and low (LVT) threshold voltages are reviewed in this thesis.

Then, analysis of transfer and output characteristics of short- and long-channel NMOS and PMOS devices with different equivalent oxide thickness (EOT) is performed. Reduced subthreshold swing (SS) and increased threshold voltages (V_{TH}) are discussed down to 4.3 K. The body-biasing capability to compensate the shift of V_{TH} at low temperature and thus to highly improve NMOS and PMOS performance is used by keeping V_{TH} constant down to 4.3 K thanks to forward body-biasing (FBB).

Using the C-V split technique, long-channel mobility of NMOS and PMOS transistors with different EOT is analyzed down to 4.3 K. The main scattering mechanisms impacting the effective mobility (μ_{EFF}) such as phonon scattering (PS), Coulomb scattering (CS), Soft phonon scattering (SPS) due to the presence of HfO_2 are discussed down to 4.3 K. The effect of body-biasing on $\mu_{EFF}(T)$ is reported. Finally, we show that the overdrive current in the linear regime at $V_{OVER} = 0.5$ V and $V_{DS} = 50$ mV (I_{ODLIN}) is well correlated to the gain in effective mobility from room temperature down to 4.3 K for different body-biasing voltages (V_{BACK}).

By comparing identical long-channel PMOS devices with undoped and intentionally doped channel, we observe a highly unstable subthreshold behavior for the doped channel device below 77 K. It results from the channel

doping impacting the effective mobility (highly reduced μ_{EFF} for the case of the doped channel) and the cryogenic shift of V_{TH} (more than twice larger shift for the doped channel).

Then, we demonstrate an excellent 4 K long-channel variability which is comparable to room temperature. For both low and high $V_{DS} = 50$ mV and 0.9 V, a low degree of variability in terms of 4 K threshold voltages and $SS - I_{DS}$ metric is demonstrated.

The analysis of the cryogenic shift in V_{TH} is given for short-channel devices with variable L_G and W. In addition, Drain-Induced Barrier Lowering ($DIBL$) quantifying the short-channel effects is analyzed down to 4.3 K. For the shortest $L_G = 28$ nm, the overdrive current at $V_{OVER} = 0.5$ V and $V_{DS} = 0.9$ V (I_{ODSAT}), we show that I_{ODSAT}/W is almost the same for W between 80 nm and 1μm for both NMOS and PMOS. Additionally, we show an important enhancement in I_{ODLIN} and I_{ODSAT} at 4 K due to the increased short-channel mobility even for $L_G = 28$ nm.

We also explore the 4 K body-biasing capability in a large range of voltages ($-5.8...+5.8$ V) for both long-and short-channel devices and study the cryogenic evolution of N- and PMOS effective currents used to model an elementary logic gate.

Finally, cryogenic analog performance is given using different metrics. The importance of V_{BACK} is demonstrated for both NMOS and PMOS devices.

The results presented in this section were partially published in [112–114].

3.1 Introduction in 28nm Fully Depleted Silicon-on-Insulator technology

Fully-Depleted Silicon-on-Insulator (FD-SOI) technology is a promising candidate for the development of advanced ultra-scaled CMOS transistors. It allows using back-gate voltage (V_{BACK}) in parallel to the top gate voltage (V_G) to modulate the threshold voltage. Moreover, the buried oxide (BOX) below the channel limits the current coming from the bulk Si region and offers excellent isolation of adjacent transistors [115]. In addition, the electrostatic control is much better than in bulk Si transistors owing to steeper Source and Drain junctions and smaller depletion regions. Also the fact that the channel is undoped results in very low variability in terms of technological parameters such as the threshold voltage (V_{TH}), on-current (I_{ON}), off-current (I_{OFF}), subthreshold swing (SS), etc. [116, 117].

Main interest of using 28nm FD-SOI technology for low-temperature applications lays in its intrinsic properties among which the already mentioned undoped channel, the presence of back-gate enabling modulation of V_{TH} (an essential requirement for low-temperature circuits made out of transistors designed for room temperature (RT) operation), and an excellent electrostatic control in terms of subthreshold swing (SS).

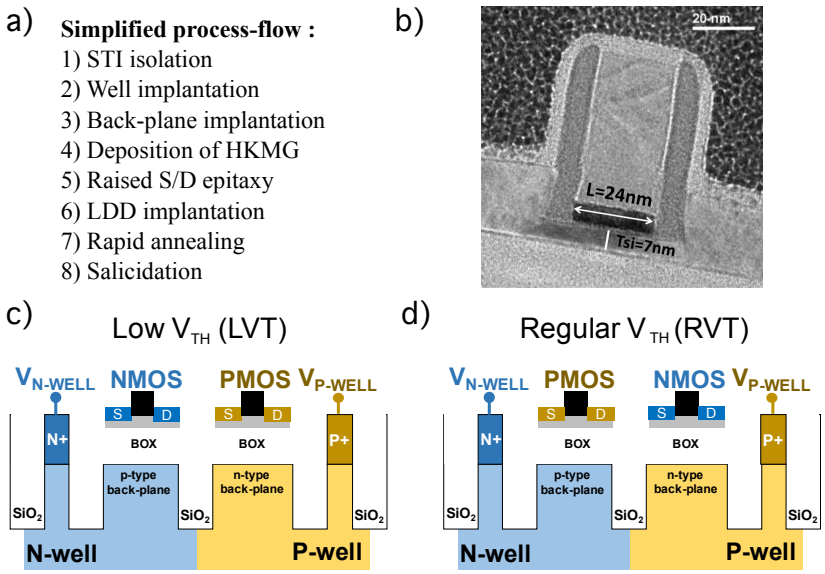


Figure 3.1: (a) Simplified process-flow adapted from [116]. (b) TEM image taken from [116] showing the cross-section of NMOS device with $L_G = 24$ nm and a channel thickness of 7 nm. (c) Low V_{TH} (LVT) architecture designed for high-performance applications with a possibility to apply forward back biasing up to $+3V/-3V$ for NMOS/PMOS at room temperature. (d) Regular V_{TH} (RVT) architecture used for ultra low-power applications with a possibility to apply reverse back biasing up to $-3V/+3V$ for NMOS/PMOS at room temperature.

Planar FDSOI transistors are fabricated on 300 mm Silicon-on-Insulator (SOI) wafers with the buried oxide (BOX) thickness of 25 nm. The device fabrication starts with shallow trench isolation (STI) done in order to isolate MOSFET devices. It is a different approach comparing to the mesa isolation used in the silicon nanowire technology. Then, well and back-plane implantations are performed to be able to address either NMOS or PMOS through a dedicated back-biasing. Afterward, high-κ metal gate is formed using a combination of SiO_2, HfO_2 and TiN layer deposition and etching. Raised silicon source and drain are epitaxially grown. Then, LDD ion im-

plantation to reduce access resistance is followed by rapid thermal annealing in order to activate the dopants. The front-end fabrication ends with salicidation during which low resistance contacts are achieved.The 7 nm-thick channel is undoped. LDD doping below 9 nm-thick SiN spacers results in a low access resistance. A simplified process-flow is shown in Fig.3.1 (a) and a transversal TEM image of resulting device is given in Fig.3.1 (b).

Two different types of transistors with thin (GO1) and thick (GO2) gate oxides were studied. In table 3.1, the corresponding EOTs are given.

	GO1	GO2
EOT_{NMOS} (nm)	1.55	3.7
EOT_{PMOS} (nm)	1.7	3.7

Table 3.1: Two different families of equivalent oxide thickness (EOT) transistors measured at low temperature.

Throughout this chapter, RVT and LVT architectures were explored as shown in Fig.3.1 (c - d). The room temperature limitations for forward (FBB) and reverse (RBB) body-biasing are mainly due to the N-well/P-well diode which must be maintained in the reverse biasing [117]. In addition, the range of RBB and FBB at 300 K is defined by the breakdown voltage and the threshold voltage of the N-well/P-well diode. Importantly, since thin BOX can result in strong coupling from the drain through the lightly doped substrate and thus degrade the gate control over the channel [118], a special backplane low doping (N/P-type for LVT NMOS/PMOS for FBB and P/N-type for RVT NMOS/PMOS for RBB) is introduced below the channel [119].

Typical example of 300 K transfer characteristics $I_{DS} - V_{GS}$ over 30 identical NMOS RVT GO1 samples with $L_G = 28$ nm and $W = 210$ nm is shown in Fig.3.2.

3.2 Transfer and output characteristics down to 4 K

There exist many different approaches to extract MOSFET's threshold voltage [120]. Throughout this thesis, we use the constant current method with different criteria for NMOS and PMOS devices commonly used for this technology by STMicroelectronics engineers:

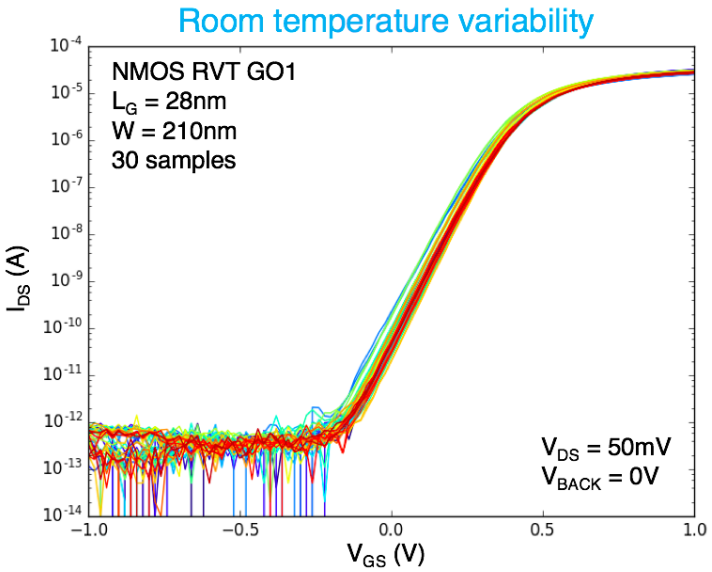


Figure 3.2: Room temperature short-channel $I_{DS} - V_{GS}$ characteristics over 30 samples.

$$V_{TH}(NMOS) = V_{GS}\ at\ I_{DS} = 10^{-7}\ W/L_G\ (A) \tag{3.1}$$

$$V_{TH}(PMOS) = V_{GS}\ at\ I_{DS} = 2 \cdot 10^{-8}\ W/L_G\ (A) \tag{3.2}$$

Concerning SS-values discussed in this chapter, we will always give the values extracted in the very weak inversion for $I_{DS} = 1 - 10$ pA. For some short-channel PMOS devices having irregular subthreshold behavior, we will give the minimal value of SS extracted using the $SS - I_{DS}$ metric.

In Fig.3.3 and 3.4, transfer characteristics $I_{DS} - V_{GS}$ for $V_{BACK} = 0$ V are shown for GO1,GO2 long/short channel NMOS and PMOS transistors. Main features common for both GO1,GO2 long/short channel devices are:

- Increased V_{TH-LIN} ($|V_{DS}| = 50$ mV) and V_{TH-SAT} ($|V_{DS}| = 0.9$ mV) due to low temperature. Indeed, reducing the temperature results in a steeper Fermi function [121] and thus the threshold voltages increase as shown with simulations in Chapter 4.

- Subthreshold swing at both $|V_{DS}| = 50$ mV (SS_{LIN}) and $|V_{DS}| = 0.9$ V is highly reduced but the values $SS(4.3K)$ are much higher than 0.8 mV/dec predicted from $ln10\ k_BT/e$ as reported in [112, 114]. The low temperature saturation of SS will be explained and modeled in Chapter 4;

- Mobility enhancement for long-channel devices can clearly be seen at low temperature. A detailed analysis of the long-channel effective mobility

evolution for different devices will be presented later;

- Almost the same (especially for long-channel devices) SS_{LIN} and SS_{SAT} are observed down to 4.3 K. In addition, for all NMOS and PMOS transistors given in Fig.3.3 and Fig.3.4, a saturation of SS_{LIN}, SS_{SAT} is observed at low temperature. The curves at 10 K and 4.3 K are almost superimposed;

- Classical, oscillationless transfer characteristics are observed down to 4.3 K for all NMOS long- and short-channel devices. However, an irregular subthreshold behavior for short channel PMOS devices can be seen in Fig.3.4 (c,e,f). We attribute these oscillations below V_{TH} (Fig.3.4 (c - f)) to the impact of enhanced boron diffusion from source/drain regions for the shortest $L_G = 28$ nm [122] and a thorough analysis of dopant-assisted transport is given in Chapter 6. Nevertheless, when L_G is relaxed to 46 nm, a stable subthreshold behavior can be obtained for PMOS devices at 4 K as demonstrated in Chapter 6.

- The V_{TH-LIN}, V_{TH-SAT} variations between 296 K and 4.3 K are very similar for long-channel NMOS and PMOS devices for GO1 and GO2 as shown in Fig.3.3 (a - d) and Fig.3.4 (a - b).

- Whereas the zero temperature point (ZTP) [121] at which the V_{TH}-shift is fully compensated with the increase in mobility can be observed for all NMOS devices, no clear ZTP is observed for PMOS devices.

- Although not shown in this chapter, the gate current is highly reduced at low temperature and is close to zero for long-channel devices and typically in the sub-100 pA range for the short-channel devices.

Note that in this section we will refer V_{BACK} to V_{N-WELL}, V_{P-WELL} for LVT NMOS,PMOS and V_{P-WELL}, V_{N-WELL} for LVT NMOS,PMOS. Although the NMOS and PMOS mobility increases at low temperature due to suppression of phonon scattering, the V_{TH} shift, as the temperature is reduced, is partially canceling the improvement of performance of FD-SOI transistors shown in Fig.3.3 and Fig.3.4. Indeed, from the output characteristics recorded at $V_{BACK} = 0$ V of NMOS LVT GO1 transistor with $L_G = 34$ nm and $W = 210$ nm shown in Fig.3.5 (a) it can be observed that $I_{ON}(4.3K)$ measured at $V_{GS} = V_{DS} = 1$ V is increased only by +12%. However, for $V_{GS} = V_{DS} = 0.5$ V (V_{GS} is below ZTP), I_{ON} at 4.3 K is reduced by -51%.

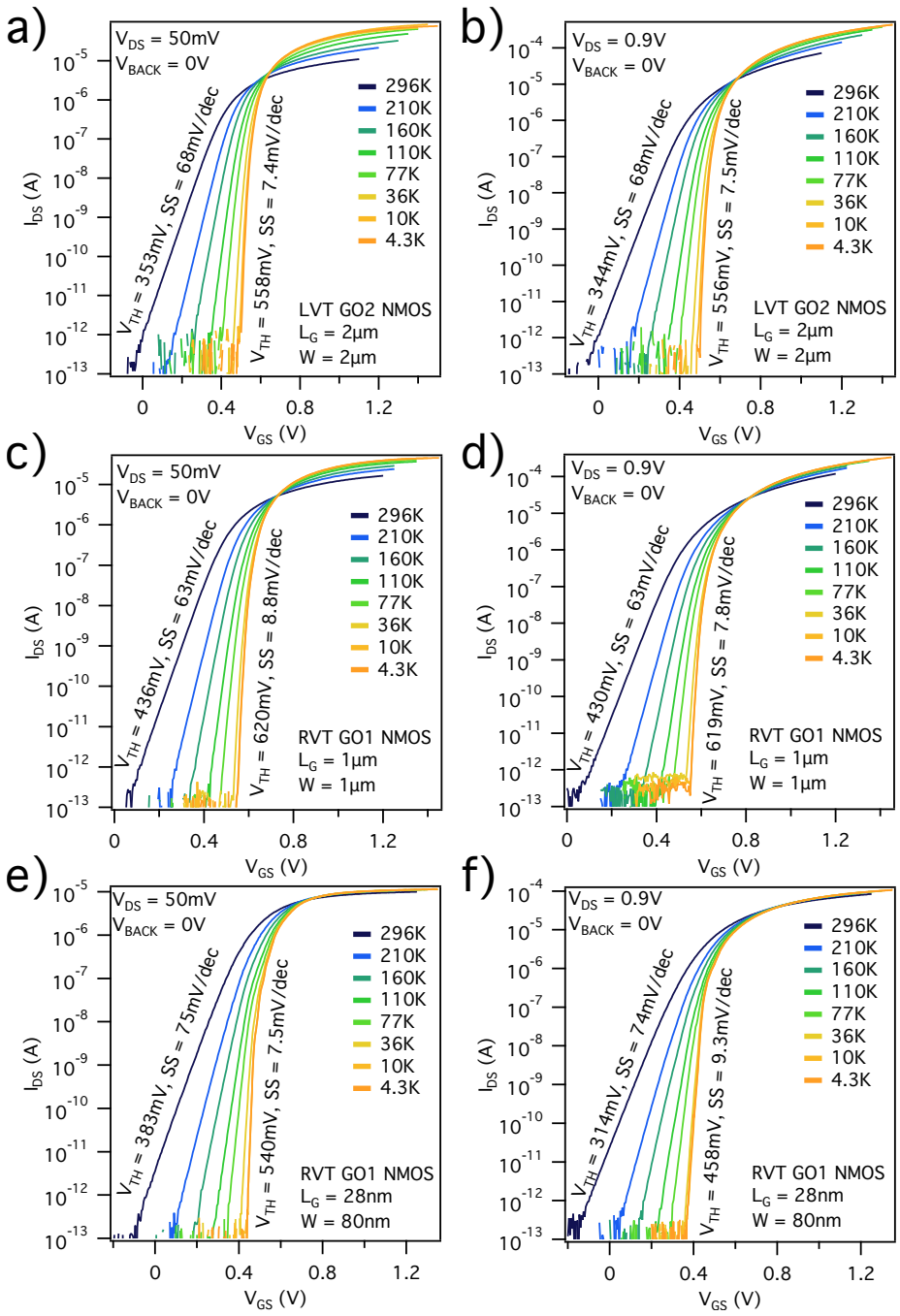


Figure 3.3: Transfer characteristics $I_{DS} - V_{GS}$ of GO1,GO2 long- and short channel NMOS devices at $V_{DS} = 50$ mV/0.9 V from RT down to 4.3 K.

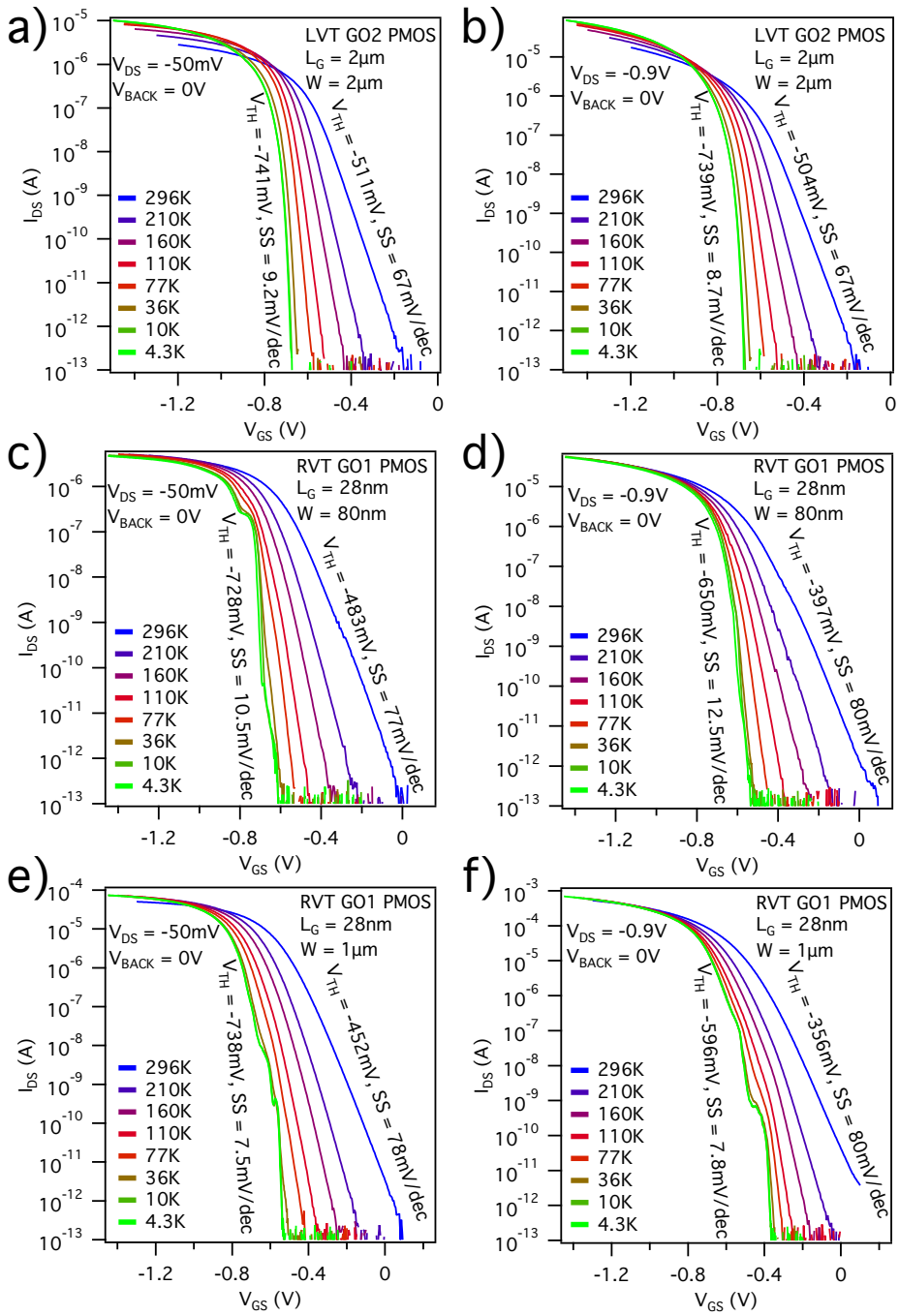


Figure 3.4: Transfer characteristics $I_{DS} - V_{GS}$ of GO1,GO2 long- and short channel PMOS devices at $V_{DS} = -50$ mV/-0.9 V from RT down to 4.3 K.

Thus, it seems to be unlikely to reduce significantly V_{DS} for a low-power cryogenic operation which is imposed by the thermal budget [20, 14]. The difference in $I_{DS} - V_{DS}$ at low temperature in the absence of body-biasing is even more drastic for PMOS LVT GO1 transistor of the same $L_G = 34$ nm shown in Fig.3.6 (a), (c) due to higher V_{TH}. We observed almost unchangeable I_{ON} at $V_{GS} = V_{DS} = -1$ V. The PMOS device cannot be used at $V_{GS} = V_{DS} = -0.5$ V as temperature is reduced down to 4.3 K due to $V_{TH}(4K) < -0.5$ V.

Then, when FBB voltages are systematically applied to keep $V_{TH-NMOS}$ and $V_{TH-PMOS}$ constant in temperature (see Fig.3.3 (e) and Fig.3.4 (e)), a significant improvement in NMOS and PMOS output characteristics was observed at low temperature. For NMOS/PMOS short-channel device, the gain in I_{ON} at $|V_{GS}| = |V_{DS}| = 1$ V at 4.3 K was found to be +32.5% and +50% as shown in Fig.3.3 (b) and Fig.3.4 (b).

Much higher gain was found at $|V_{GS}| = |V_{DS}| = 0.5$ V with +83% and +211% for NMOS (Fig.3.3 (d)) and PMOS (Fig.3.4 (d)). Note that in order to compensate V_{TH}-shift at 4.3 K by approximatively $160 - 170$ mV for NMOS and $250 - 280$ mV for PMOS , FBB voltages up to $1.6 - 1.7$ V for NMOS and $-2.9 - 3.1$ V for PMOS were applied. Importantly, the forward body-factor given by $\gamma = \Delta V_{TH}/\Delta V_{BACK}$ was found to be almost unchanged down 4.3 K indicating that the backplane doping of FD-SOI transistors is not frozen-out [123].

From the analysis of I_{ON} currents for NMOS (Fig.3.3 (f-g)) and PMOS (Fig.3.4 (f-g)) devices, another important conclusion can be derived. The measured total resistance ($R_M = V_{DS}/I_{ON}$) reveals a pronounced saturation behavior below 100 K (as well as threshold voltages of short-channel devices which will be discussed later). This result can be explained by a partial freeze-out of LDD regions [124] possessing a relatively low concentration of dopants designed to have good access resistances at RT.

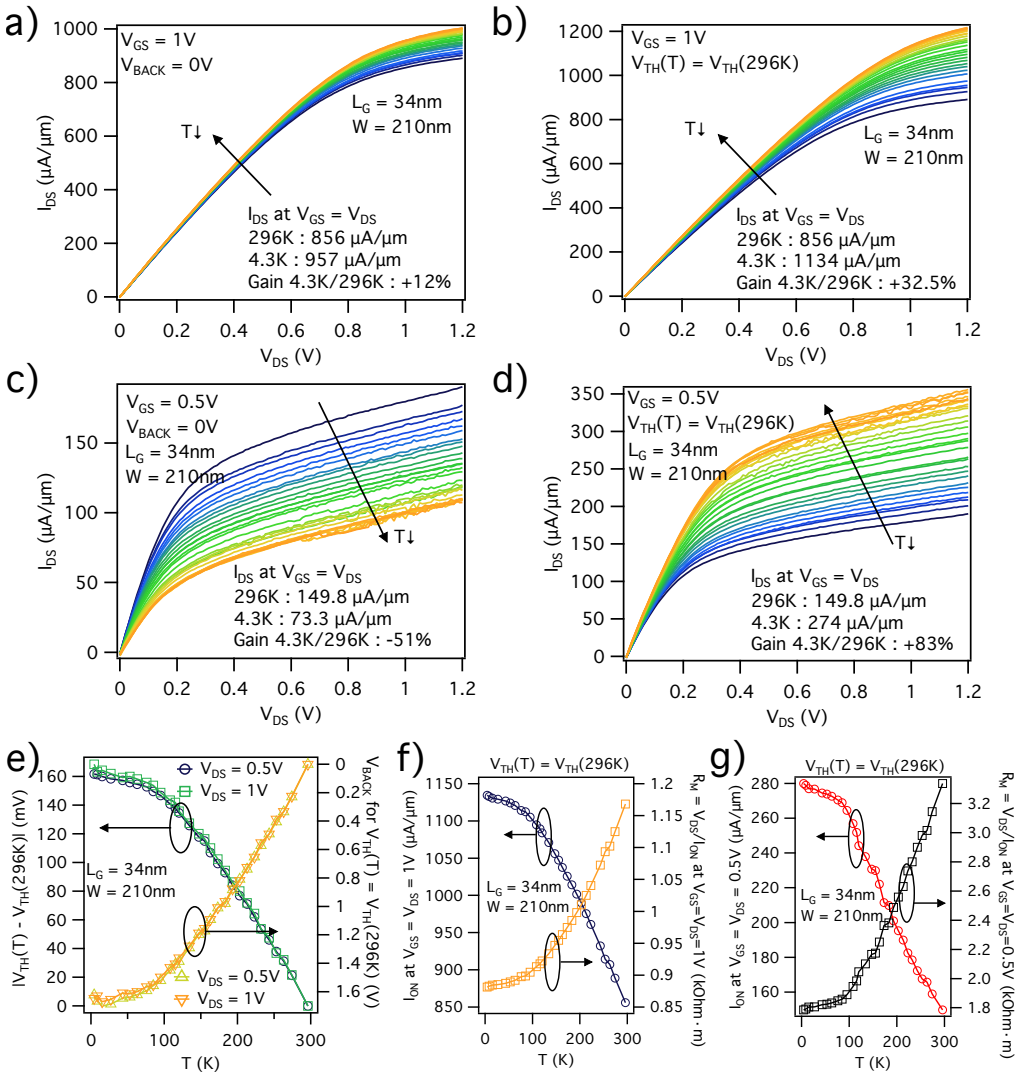


Figure 3.5: Output characteristics $I_{DS} - V_{DS}$ of NMOS LVT GO1 transistor with L_G = 34nm and W = 210 nm recorded approximatively every 10 K from RT down to 4.3 K. (a),(c) the case of V_{BACK} = 0 V for V_{GS} above (V_{GS} = 1 V) and below (V_{GS} = 0.5 V) ZTP. (b),(d) $I_{DS} - V_{DS}$ for temperature-constant V_{TH} achieved using FBB-compensation at each temperature. (e) The temperature dependence of V_{TH} for V_{DS} = 0.5 V and 1 V and the FBB values deduced from $I_{DS} - V_{GS}$ required to have $V_{TH}(T) = V_{TH}(296K)$. (f),(g) On-current I_{ON} and measured resistance R_M for V_{DS} = 0.5 V and 1 V plotted for $V_{TH}(T) = V_{TH}(296K)$. Note that for both $V_{DS} = V_{GS}$, the measured resistance is saturating approximatively below 100 K.

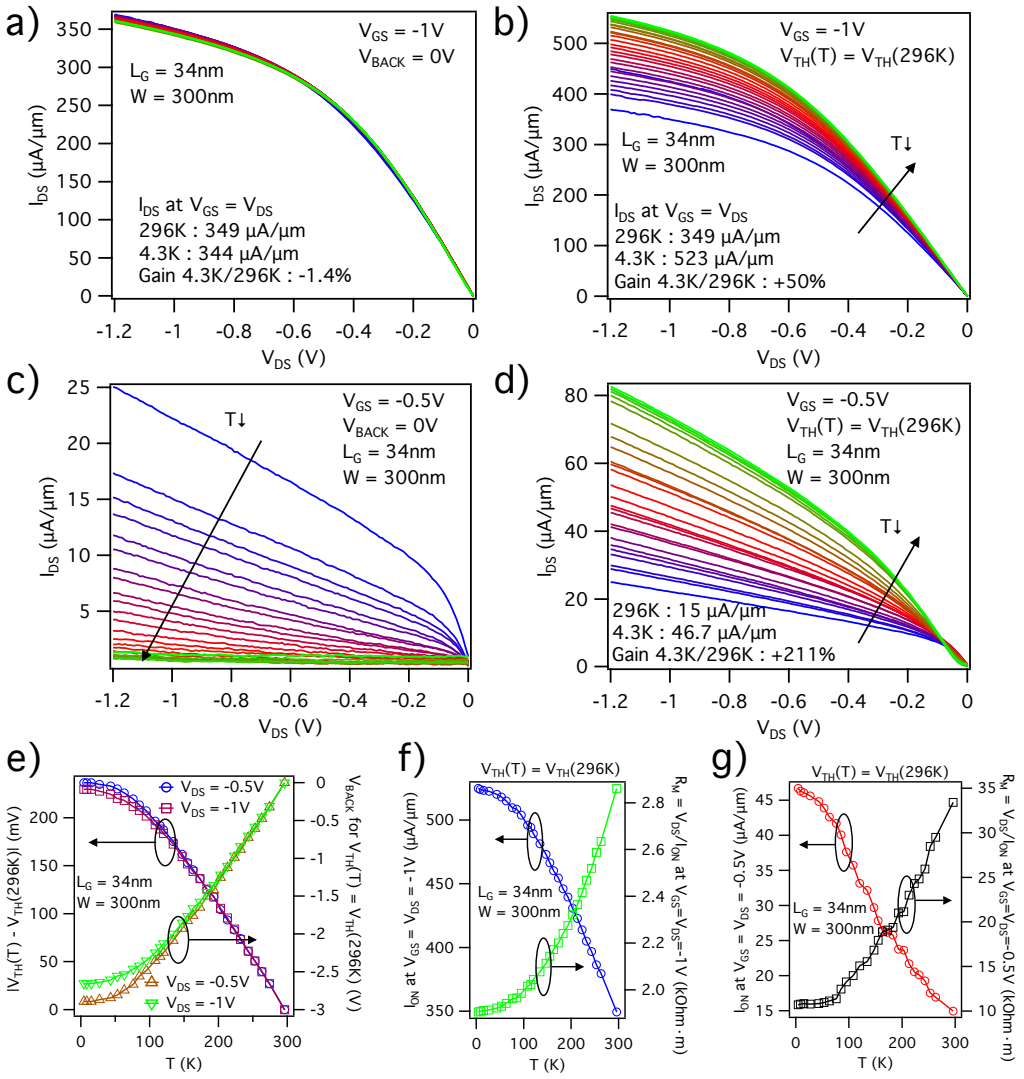


Figure 3.6: Output characteristics $I_{DS}-V_{DS}$ of PMOS LVT GO1 transistor with L_G = 34nm and W = 300 nm recorded approximatively every 10 K from RT down to 4.3 K. (a),(c) the case of V_{BACK} = 0 V for V_{GS} = −1 V and −0.5 V. (b),(d) $I_{DS}-V_{DS}$ for temperature-constant V_{TH} achieved using FBB-compensation at each temperature. (e) The temperature dependence of V_{TH} for V_{DS} = −0.5 V and −1 V and the FBB values deduced from $I_{DS}-V_{GS}$ required to have $V_{TH}(T) = V_{TH}(296K)$. (f),(g) On-current I_{ON} and measured resistance R_M for V_{DS} = −0.5 V and −1 V plotted for $V_{TH}(T) = V_{TH}(296K)$. Note that for both $V_{DS} = V_{GS}$, the measured resistance is saturating approximatively below 100 K.

3.3 Long-channel mobility down to 4 K

The mobility of charge carriers in the channel is one of the key parameters of MOSFET that is continuously optimized and improved by the microelectronics industry for the most advanced CMOS technologies. It can be defined as a factor of proportionality between the charge carrier velocity and the applied electric field. Typically, the drain current in the linear regime is given by [125]:

$$I_{DS}(V_{GS}) = (W/L_G)\ \mu_{EFF}\ N_{INV}(V_{GS})\ e\ V_{DS} \tag{3.3}$$

where μ_{EFF} is the effective mobility and N_{INV} is the inversion charge carrier density. Depending on the technology, it is important to determine both the value of μ_{EFF} as well as its dependence on the effective electric field or the inversion charge density.

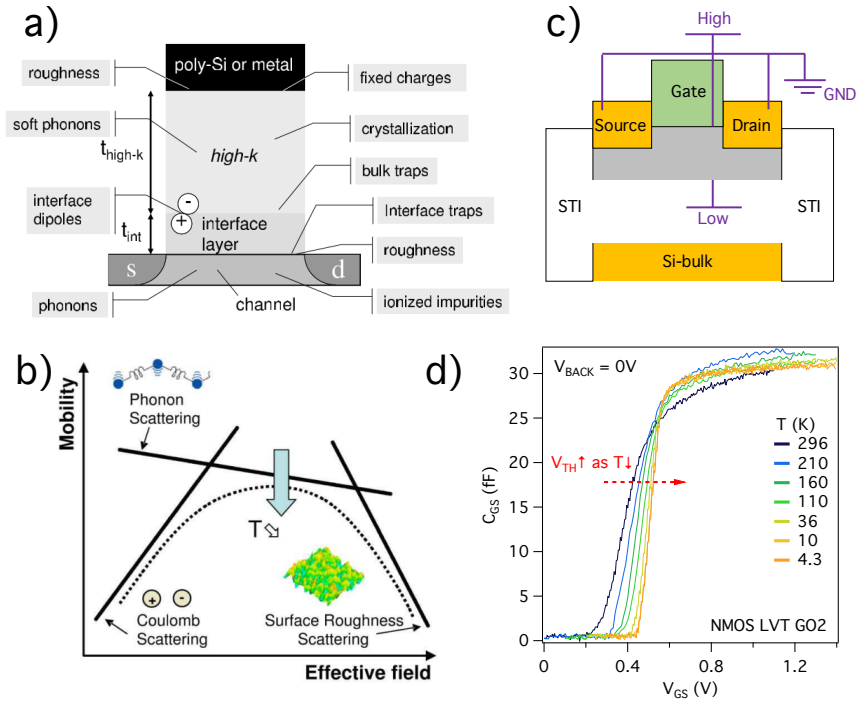


Figure 3.7: (a) Different mechanism affecting the effective mobility. Taken from [73]. (b) An electrical scheme for the C-V split long-channel mobility measurement. (c) Three main sources of scattering and their evolution as temperature is decreased. Taken from [73]. (d) An example of the measured gate capacitance $C_{GS}-V_{GS}$ of NMOS LVT GO2 as a function of temperature measured at $V_{AC} = 20\mu$V and 100 kHz.

Although there exist a large variety of scattering mechanisms defining the effective mobility, especially in the presence of high-κ material HfO_2 in the gate stack (see Fig.3.7 (a)), the following sources of scattering essentially define μ_{EFF}:

- Phonon Scattering (PS): interactions between charge carriers and acoustic phonons [73];

- Coulomb Scattering (CS): Coulomb interactions with charges located in the channel [126];

- Surface Roughness (SR): mobility degradation due to the finite roughness at the Si/SiO_2 interfaces [126].

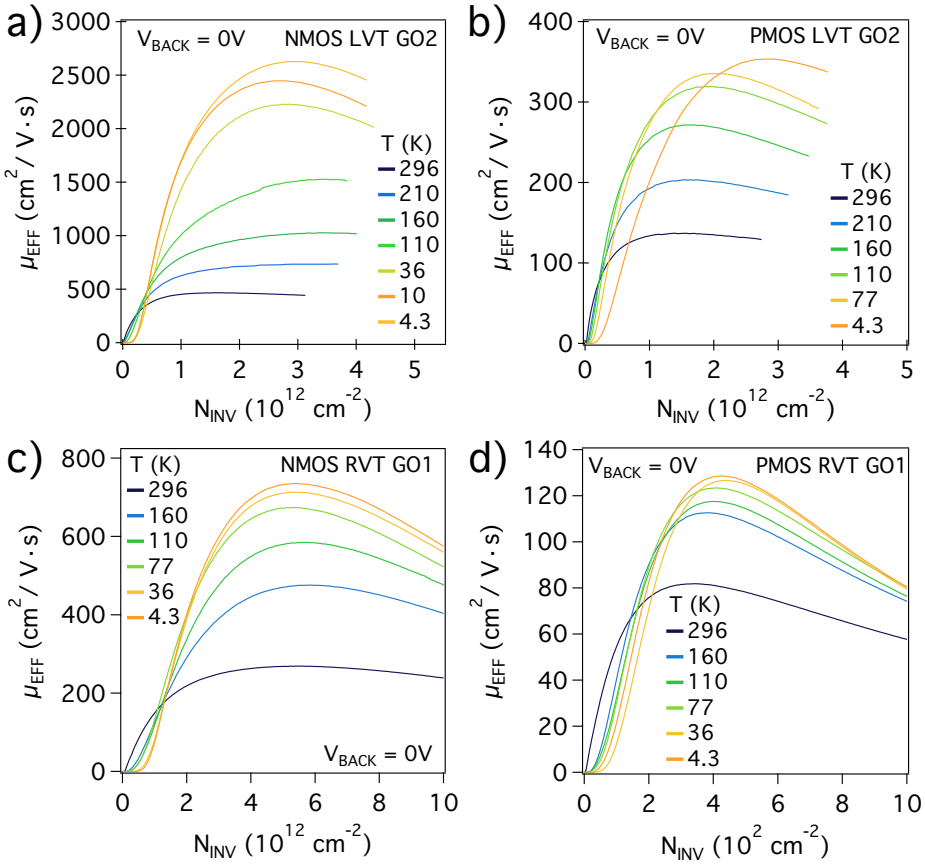


Figure 3.8: Effective mobilities from RT down to 4.3 K for GO2 NMOS (a), PMOS (b) and GO1 NMOS (c) and PMOS (d) long-channel transistors obtained using the C-V split technique.

Additionally, given that there is a thin layer of HfO_2 in the gate stack of FD-SOI transistors, two additional mechanisms should be considered [73]:

- Remote Coulomb Scattering (RCS) due to the charges at the SiO_2/HfO_2 interface [127, 128];

- Soft optical Phonon Scattering (SPS) induced by the use of HfO_2 [129, 130].

At low temperature, acoustic phonon scattering (PS) decreases as lattice vibrations become weaker and are almost suppressed at 4 K. Coulomb Scattering (CS), however, is strengthened at a cryogenic temperature which can be understood by a slower thermally-activated motion of charge carriers resulting in larger deflections by residual dopants in the channel, charges trapped in the oxide and finally smaller scattering time. Regarding Surface Roughness (SR), this scattering mechanism is dominant in the strong inversion regime and has almost no temperature dependence. The temperature dependence of these three mechanisms is summarized in Fig.3.7 (c). At room temperature, the low field mobility in the weak/intermediate inversion regime (for example $N_{INV} = 5 \cdot 10^{12}$ cm^{-2}) is mainly governed by PS whereas at low-temperature CS becomes the dominant mechanism.

A commonly used technique for measuring the effective mobility is the so-called C-V split [131] which is well suitable for the measurement of long gate length devices. It is based on the measurement of inversion charge Q_{INV} (or the charge density often normalized by area $N_{INV} = Q_{INV}/eL_GW$) at small excitation AC voltage and $f = 100$ kHz when source/drain are grounded and a capacitance meter is used to record gate capacitance C_{GS} as V_{GS} is swept (see Fig.3.7 (b)). Then, by integrating the measured C_{GS} with respect to V_{GS}, Q_{INV} is derived and the effective mobility can written as :

$$\mu_{EFF}(N_{INV}) = (L_G\ I_{DS})/(e\ W\ N_{INV}\ V_{DS}),\ at\ V_{DS} = 50mV \qquad (3.4)$$

All the effective mobilities measured using the C-V split technique presented in this chapter were measured at 100 kHz. In Fig.3.7 (d), the temperature evolution of $C_{GS} - V_{GS}$ for NMOS LVT GO2 long-channel transistor is shown at $V_{BACK} = 0$ V. Two main features of low-temperature curves can be observed: (i) the maximal value of C_{GS} in the strong inversion regime is almost independent on temperature and (ii) the overall profile $C_{GS} - V_{GS}$ is shifted and becomes steeper at low temperature. Having a limited resolution of the capacitance meter, it thus becomes impossible to apply this mobility measurement technique to short-channel devices because of the small area. That is why for short-channel device another technique is commonly used to derive (low-field) mobility, the so-called Y-function method [132]. This technique will be used for extraction of low-field mobility down to $L_G = 28$ nm in Chapter 5.

In Fig.3.8, the effective mobility as a function of inversion charge density is plotted from 296 K down to 4.3 K. An important mobility enhancement is observed for all GO1 and GO2 devices since phonon mobility is sufficiently weak and can be neglected at a very low temperature. It can also be noted that thick gate oxide (GO2) weakens remote Coulomb and soft-optical phonon scattering (the SiO_2/HfO_2 interface is displaced further from the silicon channel). It, therefore, leads to an improved carrier mobility [133, 134]. Thus, the low-temperature mobility enhancement is much stronger for GO2 devices, especially in the weak/intermediate inversion regime. This is illustrated in Fig.3.9 (a), where the peak of μ_{EFF} is plotted as a function of temperature for GO1 and GO2 devices.

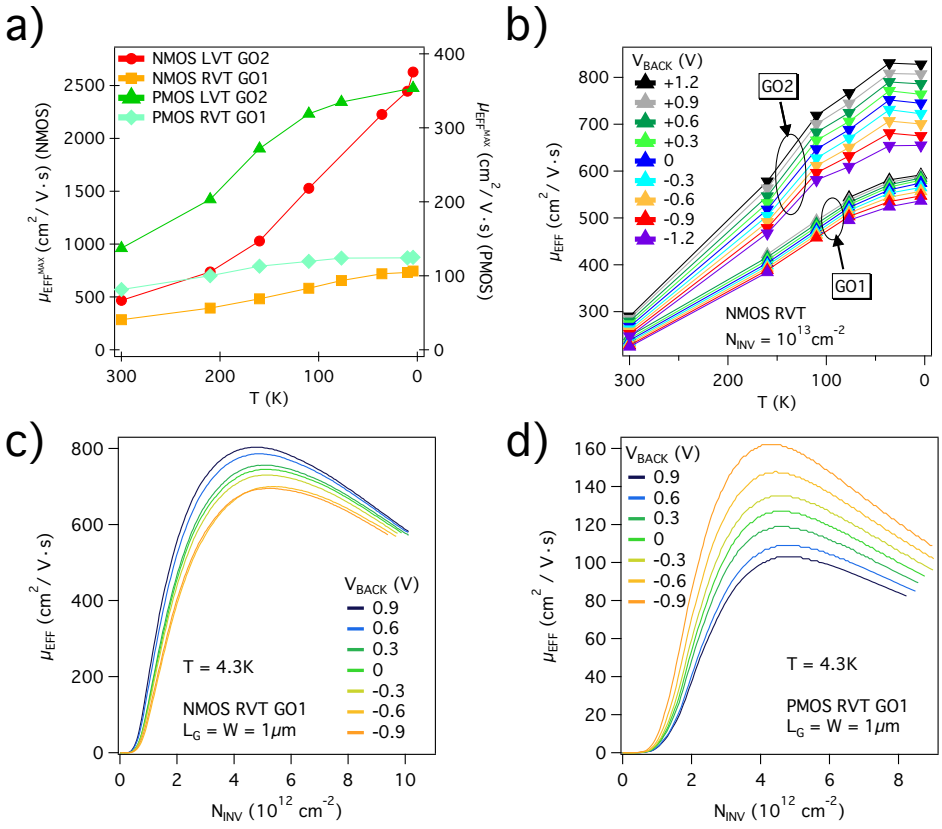


Figure 3.9: (a) Maximal effective mobility as a function of temperature for long-channel GO1 and GO2 transistors at $V_{BACK} = 0$ V. (b) The effect of body-biasing on μ_{EFF} extracted at $N_{INV} = 10^{13}$ cm^{-2} for GO1 and GO2 NMOS. (c),(d) An illustration of the effect of moderate body-biasing on effective mobility for GO1 NMOS and PMOS 4.3 K.

Importantly, as we already discussed in the previous section, the compensation of the V_{TH}-shift with body-biasing is essential at low temperature to keep the advantage of high charge carrier mobility. In Fig.3.9 (b) we show an example of the body-biasing capability to modulate the mobility at low temperature in the strong inversion regime at $N_{INV} = 10^{13}$ cm^{-2} for NMOS GO1 and GO2 devices (the same holds for PMOS devices not shown here). Much higher modulation of μ_{EFF} for GO2 devices can be explained by thicker EOT and the fact that the SiO_2/HfO_2 interface is further away from the channel. Indeed, at 4.3 K, it is still possible to greatly improve the effective mobility by bringing the conductive channel towards the bottom Si/BOX interface for both NMOS and PMOS devices as shown in Fig.3.9 (c) and (d) (the same holds for GO2 devices not shown here). In addition, the back-interface scattering is expected to be lower than the front interface one [134]. The density of interface traps at back-interface in FD-SOI transistors is typically at least ten times lower than the front one, for instance, 3×10^{10} against 5×10^{11} $traps/cm^2/eV$ was reported in [135].

Given the low-temperature shift in V_{TH}, in order to quantify MOSFET's performance, the overdrive current can be used instead of I_{ON} extracted at a given V_{GS} as it was done in Fig.3.5 and 3.6.

In this chapter, we will use the following expressions for the overdrive drain current:

$$I_{ODLIN}(T) = I_{DS}\ at\ |V_{TH}(T) + 0.5V|\ at\ V_{DS} = 50mV \tag{3.5}$$

$$I_{ODSAT}(T) = I_{DS}\ at\ |V_{TH}(T) + 0.5V|\ at\ V_{DS} = 0.9V \tag{3.6}$$

At low temperature, we can observe a clear improvement of I_{ODLIN} and I_{ODSAT} for both NMOS and PMOS, GO1 and GO2 devices as shown in Fig.3.10 (a - b). Furthermore, according to 3.3, the gain in $\mu_{EFF}(T)$ should be directly correlated to the gain in $I_{ODLIN}(T)$. Indeed, we show in Fig.3.10 (c - d) an excellent correlation between the $I_{ODLIN}(T)$ and $\mu_{EFF}(T)$ improvements. The same trend was observed for PMOS GO1 and GO2 devices not shown here.

3.4 Comparison between intentionally doped and undoped long-channel PMOS

In this work, PMOS RVT GO2 devices were highly doped during the poly-Si ion implantation (II). Due to the increased dose of II of poly-Si,

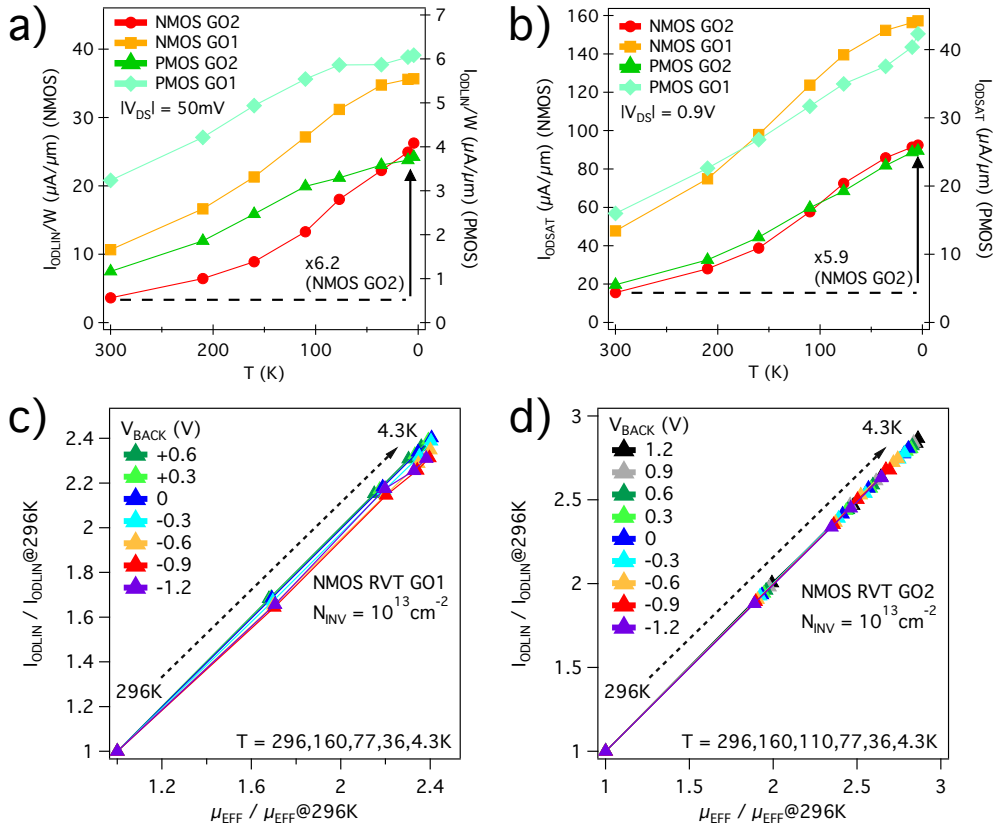


Figure 3.10: (a),(b) The overdrive current for $V_{DS} = 50$ mV (I_{ODLIN}) and 0.9 V (I_{ODSAT}) for NMOS and PMOS GO1/GO2 devices for $|V_{OVER}| = 0.5$ V. (c),(d) The correlation between the gain in effective mobility in the strong inversion regime and the corresponding I_{ODLIN},I_{ODSAT} for the same $N_{INV} = 10^{13}$ cm^{-2}.

PMOS RVT GO2 are likely to contain a non-negligible amount of dopants in the gate stack down to the Si/SiO_2 interface. Here, such PMOS devices are compared with the behavior of undoped channel device (residual impurities concentration in FD-SOI transistors is typically as low as 10^{15} cm^{-3}).

When cooled down, the first important observation from the experiment is that below 100 K (see Fig.3.11 (a - b), the subthreshold current becomes irregular displaying an oscillating behavior previously observed in short-channel PMOS. It is consistent with the freeze-out of boron atoms below 100 K highly impacting the subthreshold transport. Indeed, whereas for the identical but undoped PMOS device (see Fig.3.6 (a - b)) SS_{LIN}, SS_{SAT} reached $8 - 9$ mV/dec at 4.3 K and shown regular $SS - I_{DS}$ behaviour,

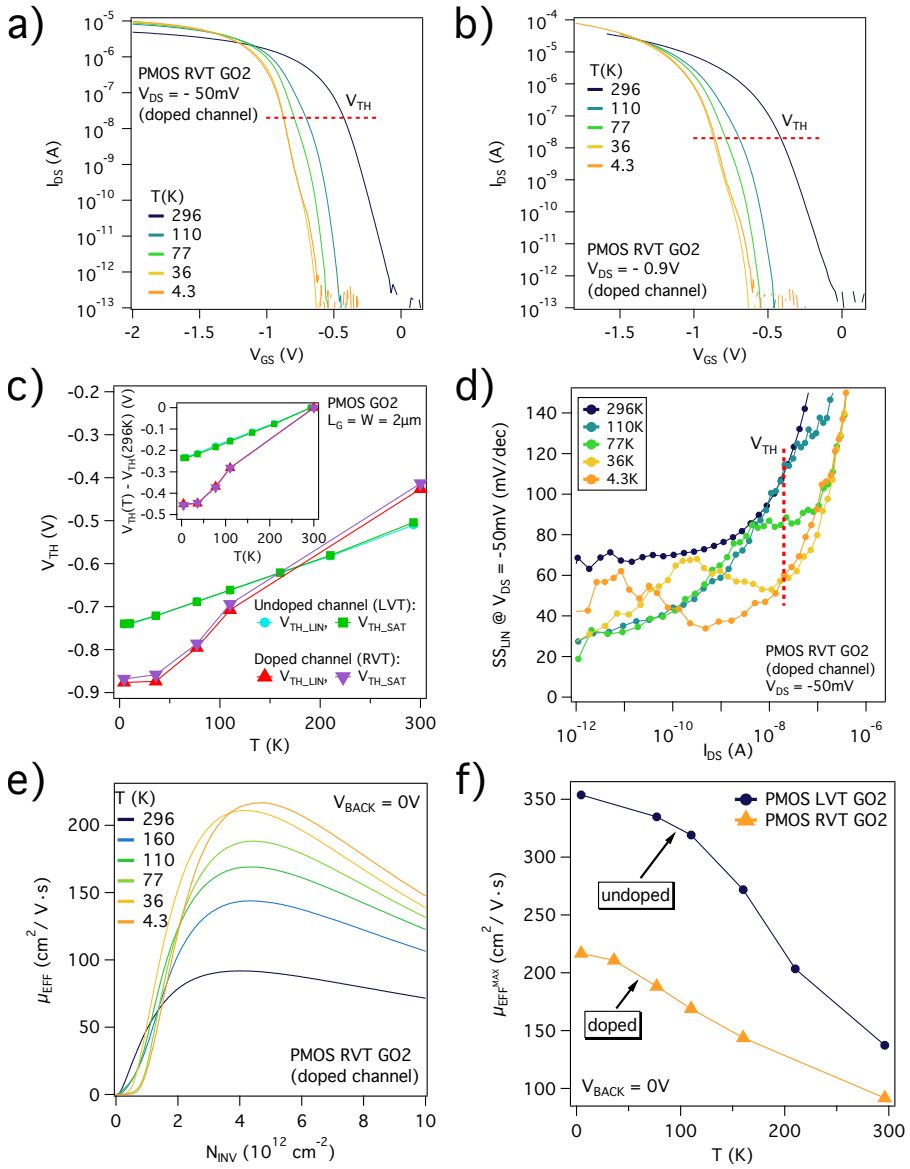


Figure 3.11: (a),(b) $I_{DS} - V_{GS}$ measured at low and high V_{DS} for the doped channel PMOS RVT GO2 device at low temperature. (c) Comparison between the evolution of V_{TH} for the PMOS transistor with $L_G = W =$ 2 µm for the doped and undoped channel down to 4.3 K. (d) The irregular behaviour of $SS - I_{DS}$ for the doped channel PMOS transistor. (e) The effective mobility for the doped channel PMOS transistor. (f) Comparison between the low temperature behaviour of the peak of μ_{EFF} for the doped and undoped PMOS of the same dimensions and EOT.

here it is not the case as shown in Fig.3.11 (d). Similar SS-values of $20-40$ mV/dec at 4.3 K for long-channel PMOS devices fabricated in conventional $160,40$ nm bulk Si technology were already reported in [67, 136]. However, the irregular $SS-I_{DS}$ behavior and large long-channel variability were not discussed.

In addition, much larger V_{TH}-shift is obtained at low temperature up to 0.5 V for the doped device as shown in Fig.3.11 (c) (similar $V_{TH}-T$ curve and the value of V_{TH}-shift were reported for conventional bulk Si PMOS devices in [137]).

At room temperature the difference in low and high field mobility for doped and undoped channel is not as significant as at low temperature due to the effect of CS and RCS drastically impacting the doped channel PMOS as shown Fig.3.11 (e) (to be compared with Fig.3.8 (b)). Indeed, the difference can be clearly observed from Fig.3.8 (d) where the peak of μ_{EFF} as a function of temperature is plotted for the doped and undoped channel PMOS devices of the same dimensions and EOT. The gain in the maximal (peak) mobility for the undoped and doped channel devices is +64% at 4.3 K.

Finally, FD-SOI technology seems to be much more advantageous comparing due to much steeper SS, regular behavior in $SS-I_{DS}$, more than twice lower shift of V_{TH} (as shown in this section and reported in [138]), much higher effective mobility due to lower CS and RCS, and potentially much lower V_{TH}-variability.

3.5 Long-channel device variability at 4 K

Regarding the requirements of CryoCMOS, the question of device variability of MOSFETs at very low temperature is of great importance for the successful design of cryogenic circuits. If there is a large variability at low temperature for FD-SOI transistors, it becomes difficult to achieve the optimal power-performance tradeoff at 4 K. Indeed, once the V_{TH}-shift is compensated, further reduction of V_{DS} to obtain lower power dissipation requires applying more FBB in order to have higher driving current (lower switching resistance of a CMOS inverter [2]) and thus higher circuit's speed (typically frequencies between $1-10$ GHz are required for driving silicon spin qubits [20]). However, if the low-temperature device variability is large, the close-to-zero-V_{TH} operation may result in non-negligible off-current thus making it challenging to further reduce the operational point.

In Fig.3.12 (a - b), $I_{DS}-V_{GS}$ characteristics of 5 identical NMOS RVT GO1 devices with $L_G = W = 1$ µm are shown at room temperature and

4.3 K. Almost the same variability at 4.3 K compared to 296 K can be seen in terms of V_{TH} and I_{ON} (not shown) as expected for undoped channel. More importantly, a regular subthreshold behavior with a low degree of variability was observed using $SS - I_{DS}$ metric as shown in Fig.3.12 (c - d).

The same behavior was observed for a series of PMOS LVT GO2 devices showing a low degree of variability at both low and high V_{DS} by comparing $I_{DS} - V_{GS}$ and $SS - I_{DS}$. The analysis of short-channel NMOS and PMOS device variability can be found in Chapter 5.

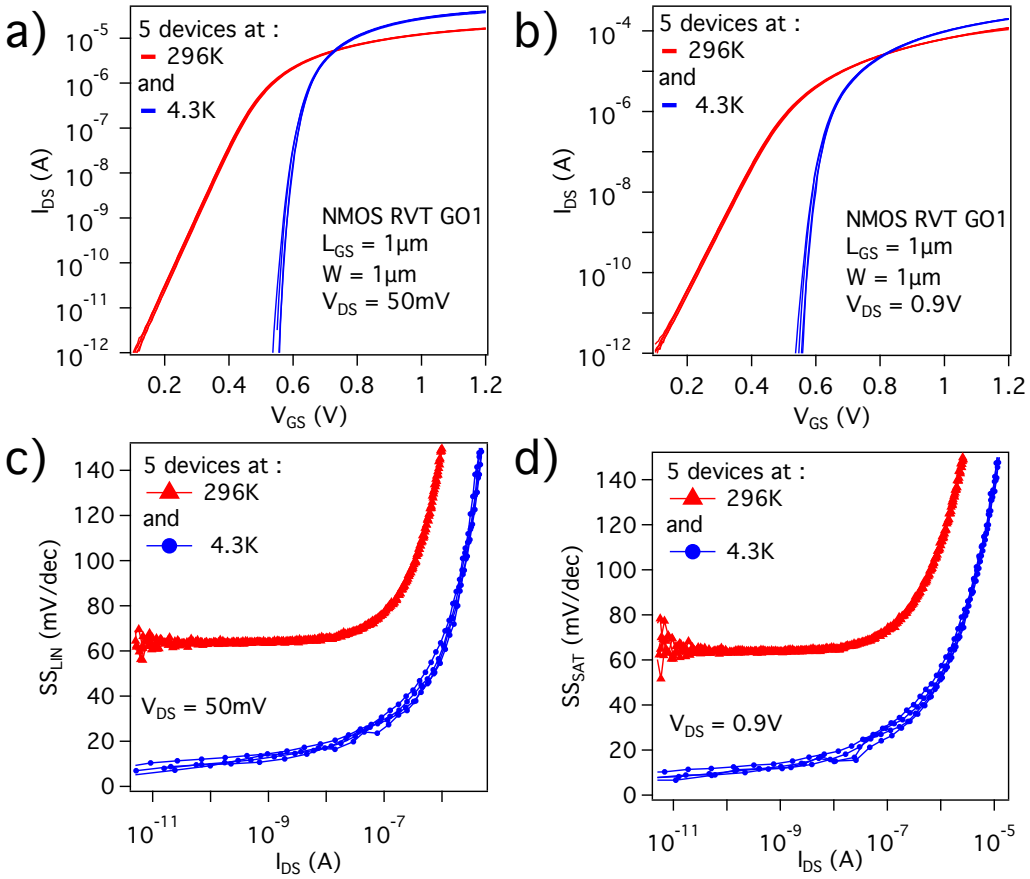


Figure 3.12: (a),(b) Transfer characteristics at RT and 4.3 K at low and high V_{DS} for 5 long-channel NMOS RVT GO1 devices. (c),(d) SS_{LIN} and SS_{SAT} as a function of I_{DS} for these 5 identical devices in (a-b) at 296 K and 4.3 K.

3.6 Short-channel devices: the effect of W

In the first section of this chapter, the increase of V_{TH-LIN}, V_{TH-SAT} was already evidenced with cryogenic transfer characteristics down to 4.3 K. In Fig.3.13 (a, c) and 3.14 (a, c), the evolution of V_{TH-LIN} and V_{TH-SAT} as a function of temperature is plotted for long- and short-channel devices. The following conclusions can be drawn.

For long channel GO1 and GO2 NMOS and PMOS devices, V_{TH-LIN} and V_{TH-SAT} vary almost linearly with temperature as expected from the low-temperature behavior of the Fermi function. However, for NMOS and PMOS RVT GO1 a small V_{TH} saturation occurs at low temperature. For short-channel NMOS and PMOS devices with $L_G = 28$ nm and W varying between 80 nm and 1 µm, a deviation from the linear law below approximatively 100 K can be observed.

To better understand this unexpected V_{TH} behaviour of short-channel devices, we calculated the relative shifts $V_{TH}(T) - V_{TH}(296K)$ at low and high V_{DS} which are shown in Fig.3.13 (b,d) and 3.14 (b,d). In both cases, we

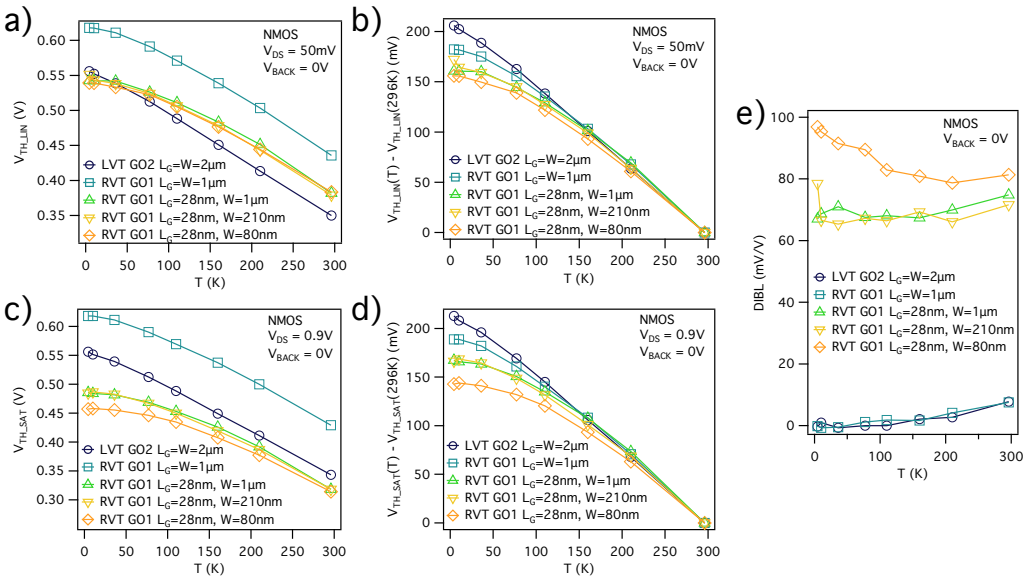


Figure 3.13: (a),(c) V_{TH-LIN} and V_{TH-SAT} as a function of temperature for two long-channel NMOS RVT GO1 and LVT GO2 devices and three RVT GO1 transistors with $L_G = 28$ nm of different W measured at $V_{BACK} = 0$ V. (b),(d) The same analysis but for $V_{TH-LIN}(T) - V_{TH-LIN}(296K)$ and $V_{TH-SAT}(T) - V_{TH-SAT}(296K)$ showing the V_{TH}-shift at low temperature. (e) $DIBL$ as a function of temperature.

observe less saturation for wider W. Although, a saturation behavior of V_{TH} for short-channel devices at low temperature was reported and an analytical BSIM modeling was proposed for bulk Si devices [137], this phenomenon is still not fully understood. Dao and colleagues in [137] explained the short-channel V_{TH} saturation by the charge sharing effect (which depends on the depletion layer width). However, to understand the saturation of V_{TH} in short-channel devices with fully-depleted and undoped channel, more statistical data are required. It also should be noted that for RVT NMOS devices with $L_G = 28$ nm, V_{TH-SAT} is more impacted by the saturation at low temperature than V_{TH-LIN} as it can be seen by comparing Fig.3.13 (b) and (d).

By analyzind the Drain-induced barrier lowering ($DIBL = |V_{TH-LIN} - V_{TH-SAT}|/(V_{DS-SAT} - V_{DS-LIN})$) as a function of temperature, we observe that at 4.3 K an initially low value ($5-10$ mV/V at 296 K) drops to almost zero for short-channel devices as it can be seen in Fig.3.13 (e) and 3.14 (e). For NMOS devices with $W = 210, 1000$ nm, $DIBL$ seems to be weakly

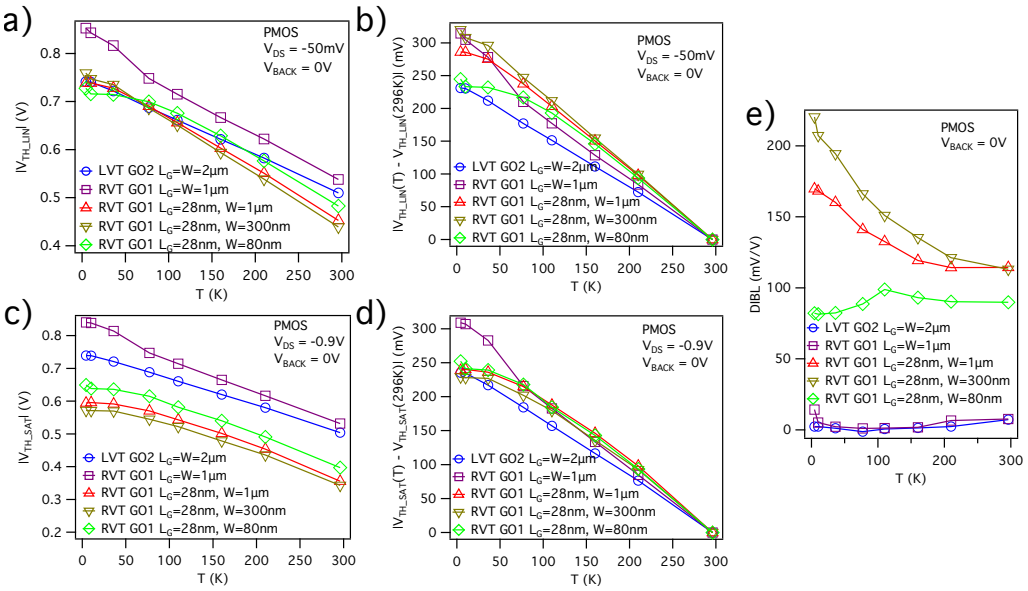


Figure 3.14: (a),(c) V_{TH-LIN} and V_{TH-SAT} as a function of temperature for two long-channel PMOS RVT GO1 and LVT GO2 devices and three RVT GO1 transistors with $L_G = 28$ nm of different W measured at $V_{BACK} = 0$ V. Not that the absolute values of $|V_{TH}|$ are plotted. (b),(d) The same analysis but for $V_{TH-LIN}(T) - V_{TH-LIN}(296K)$ and $V_{TH-SAT}(T) - V_{TH-SAT}(296K)$ showing the V_{TH}-shift at low temperature. (e) $DIBL$ as a function of temperature.

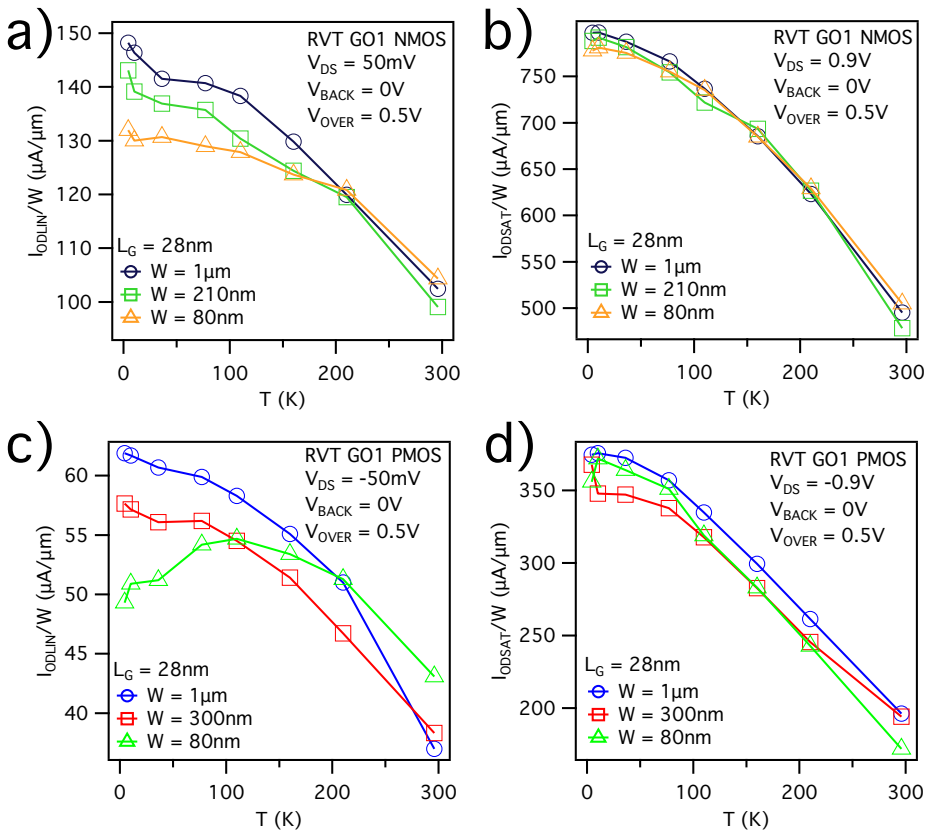


Figure 3.15: (a),(c) I_{ODLIN} and (b),(d) I_{ODSAT} as a function of T for NMOS and PMOS devices with $L_G = 28$ nm and diffrent W.

dependent on temperature. No significant difference in terms of electrostatic control between different W was observed by analyzing $SS(T)$ down to 4.3 K. The DIBL situation is different for short-channel PMOS devices as shown in Fig.3.14 (e). Here, for wider W, $DIBL(T)$ increases significantly at low temperature. It should be mentioned that short-channel PMOS devices are highly impacted by enhanced diffusion of boron atoms from Source/Drain regions and thus it is expected to have irregular, oscillatory behavior in the subthreshold regime (see Fig.3.4 (c - f)).

In Fig.3.15, I_{ODLIN} and I_{ODSAT} normalized by W as a function of temperature are plotted for NMOS and PMOS transistors with $L_G = 28$ nm and variable W. Importantly, for both NMOS and PMOS devices, an important enhancement of I_{ODLIN} is observed down at 4.3 K. It is a clear indication that contrarily to what has been reported for short-channel 14 nm FD-SOI transistors, there is an improvement in short-channel mobility. As the mobility is expected to be higher for larger W in planar devices [139],

we observe this trend for all NMOS devices (shown in Fig.3.15 (a)) and for PMOS with $W = 300, 1000$ nm plotted in Fig.3.15 (b). The reason for a drop in I_{ODLIN} for the PMOS with $W = 80$ nm is probably due to the highly irregular oscillatory behaviour around $V_{GS} = V_{TH}$ as shown in Fig.3.4 (c). Importantly, the low-temperature enhancement of I_{ODSAT}/W is almost the same for both short-channel NMOS and PMOS device for $W = 80...1000$ nm. This observation will be used later in Chapter 5 to correlate the cryogenic performance of RO with the effective currents of a CMOS inverter [2].

3.7 Short-channel devices: the effect of L_G

After having studied the effect of W for a given short L_G, here we compared the cryogenic performance of GO1 NMOS and PMOS transistors from room temperature to 4.3 K. The overdrive drain currents at $|V_{DS}| =$ 50 mV and 0.9 V at 4.3 K were found to increase as L_G was reduced from 1 µm to 28 nm as shown in Fig.3.16 (a, b) and 3.17 (a, b).

In [140] the charge carrier mobility in 14 nm FD-SOI devices was studied down to 77 K. By comparing the low-field mobility extracted using the Y-function method as a function of temperature for different L_G, it was argued that neutral defect scattering (defects originating from the fabrication of source/drain regions [141]) becomes the dominant mobility limiting factor below typically $L_G = 50$ nm and is independent on the gate stack. In our case, using a well-optimized 28 nm FD-SOI technology we expect that the short-channel mobility is not completely saturated below a certain temperature. By plotting $I_{ODLIN}/(W/L_G)$ and $I_{ODSAT}/(W/L_G)$ at 4.3 K for different L_G, we observed a non-negligible gain in the overdrive currents as compared to 296 K for both NMOS and PMOS devices as shown in Fig.3.16 (c, d) and 3.17 (c, d).

Then, given that the linear drain current is proportional to $(W/L_G)\,\mu_{EFF}$ according to 3.3, we obtained a usual increase of mobility (or I_{ODLIN}) as the gate length is reduced [139]. We already demonstrated that the gain in I_{ODLIN} current is directly proportional to the gain in the long-channel mobility. Thus, we expect the same behavior for the short-channel NMOS and PMOS devices. For the case of $L_G = 28$ nm, a gain at $4.3K$ as compared to room temperature in terms of $I_{ODLIN}(L_G/W)$ of approximatively +45% for NMOS and +63% for PMOS devices is achieved.

In Chapter 5 we will show that the low-field mobility for the case of $L_G = 28$ nm extracted using the Y-function method, increase by almost a

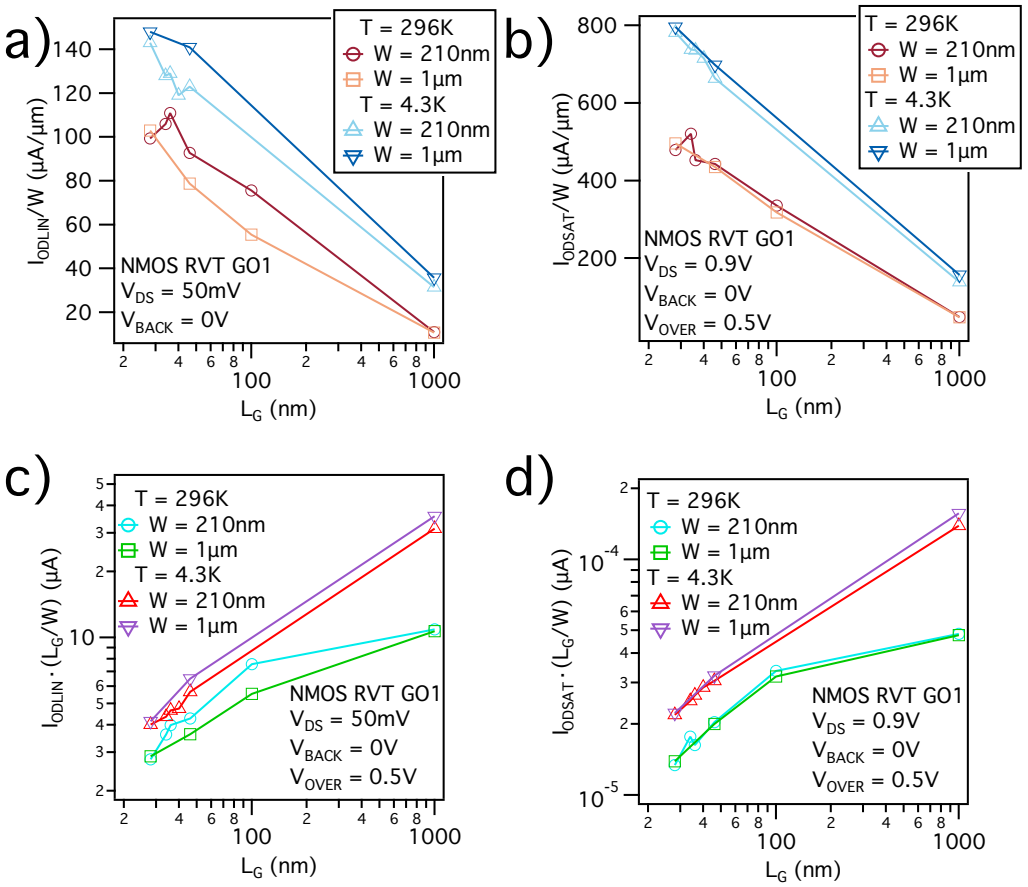


Figure 3.16: NMOS RVT GO1 transistors at 296 K and 4.3 K. (a),(b) I_{ODLIN}/W and I_{ODSAT}/W as a function of L_G for $W = 210, 1000$ nm. (c,)(d) Normalized by L_G, $I_{ODLIN}/(W/L_G)$ and $I_{ODSAT}/(W/L_G)$ as a function of L_G for $W = 210, 1000$ nm.

factor of 2 at 4.3 K compared to RT and an efficient power-performance tradeoff for Ring Oscillators can be performed.

3.8 Body-biasing at low temperature

It will be shown that in order to at least maintain the RT performance of ROs, especially for reduced V_{DS}, it is essential to compensate the cryogenic shift of V_{TH}.

The effective currents of NMOS and PMOS devices shown in Fig.3.18 (a - c), can be calculated as following [2]:

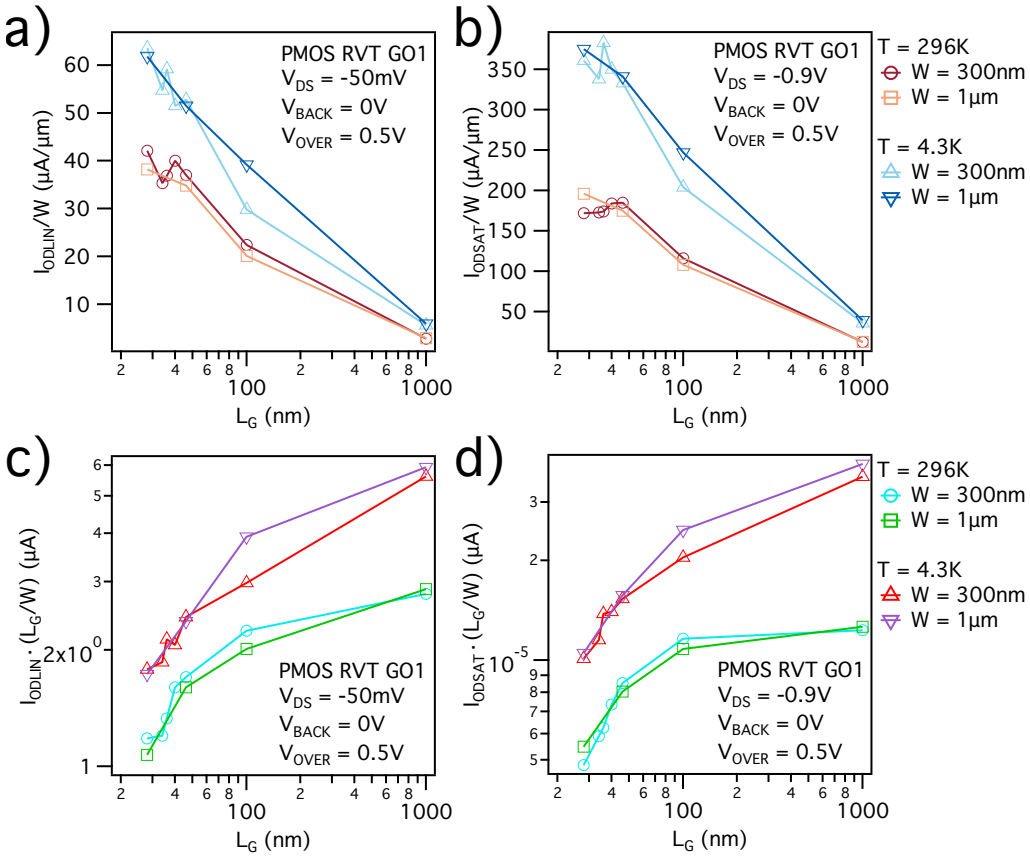


Figure 3.17: PMOS RVT GO1 transistors at 296 K and 4.3 K. (a),(b) I_{ODLIN}/W and I_{ODSAT}/W as a function of L_G for $W = 300, 1000$ nm. (c,)(d) Normalized by L_G, $I_{ODLIN}/(W/L_G)$ and $I_{ODSAT}/(W/L_G)$ as a function of L_G for $W = 300, 1000$ nm.

$$I_{EFF-N(P)} = (I_H + I_L)/2 \tag{3.7}$$

$$I_{EFF} = 1/(1/I_{EFF-N} + 1/I_{EFF-P}) \tag{3.8}$$

where $I_H = I_{DS}$ extracted at $V_{GS} = V_{DD}, V_D = V_{DD}/2$ and $I_L = I_{DS}$ extracted at $V_{GS} = V_{DD}/2, V_D = V_{DD}$. V_{DD} is the supply voltage. By analyzing the effective currents of the NMOS and PMOS devices shown in Fig.3.18 (a - b), we realize that without the compensation of V_{TH}-shift with FBB, I_{EFF} is drastically reduced at low temperature, especially for the PMOS device as it was already shown from the analysis of I_{ON} currents in the first section of this chapter.

We demonstrate that at 4.3 K, I_{EFF-N} and I_{EFF-P} can be efficiently controlled with body-biasing as shown in Fig.3.18 (d).

In Fig.3.19, we demonstrate the extended body-biasing capability at 4.3 K for GO2 devices with $L_G = 100$ nm and GO1 devices with $L_G = 34$ nm. Regular transfer characteristics for FBB voltages up to ± 5 V are observed for both GO2 devices and the GO1 NMOS transistor for low V_{DS} as shown in Fig.3.19 (a, b, d). An oscillatory behaviour in the subthreshold current of short-channel PMOS device shown in Fig.3.19 (e) can be reduced by relaxing L_G.

In Fig.3.19 (c), the 4 K V_{TH} tunability for $|V_{BACK}|$ up to 5 V is shown for GO2 devices. Almost the same body-factor γ for both NMOS and PMOS devices was found at 4.3 K. The measured GO2 body-factors at 4.3 K are

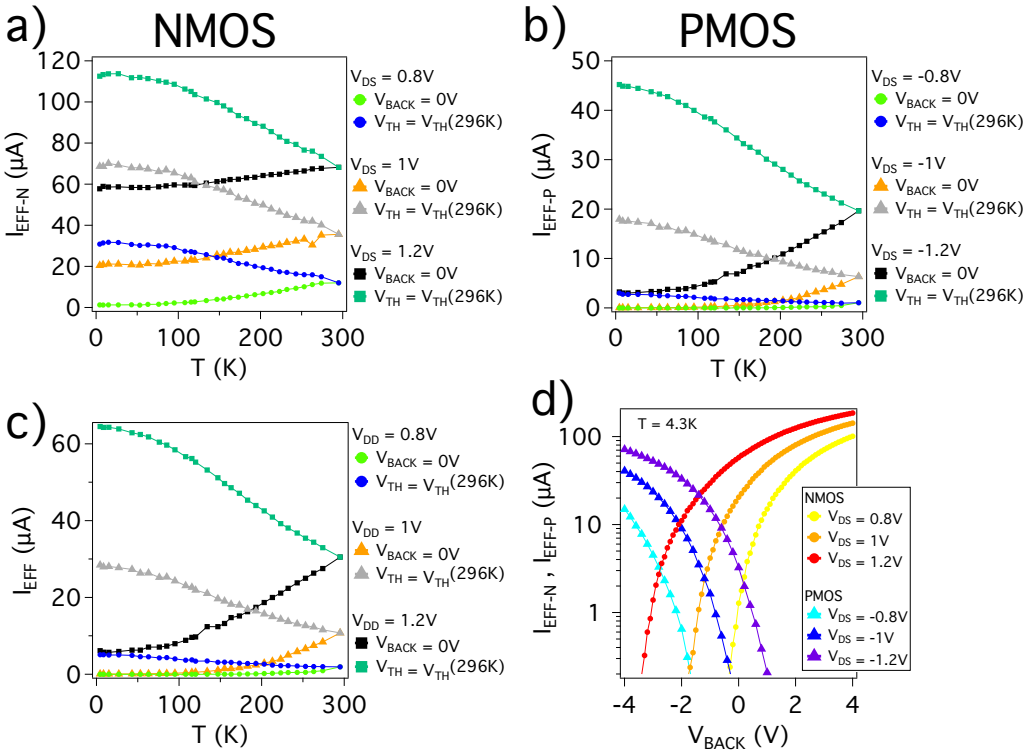


Figure 3.18: (a), (b) Effective currents for NMOS and PMOS LVT GO1 devices with $L_G = 34$ nm and $W_{NMOS} = 210$ nm, $W_{PMOS} = 300$ nm from 296 K down to 4.3 K. (c) The total I_{EFF} calculated from (a),(b) as a function of temperature for the case of $V_{BACK} = 0$ V and with the threshold voltage compensation $V_{TH}(T) = V_{TH}(296K)$. (d) The 4 K tunability of I_{EFF-N} and I_{EFF-P} as a function of V_{BACK}.

close to the room temperature values: 183 and 178 mV/V for NMOS and PMOS, respectively. The situation is similar for GO1 devices. Due to the difference in back-plane doping 95 mV/V for NMOS and 69 mV/V for PMOS GO1 devices were observed at 4.3 K. Supporting our assumption of the body-biasing effect not altered by freeze-out of back-plane dopants, these values are close to what was observed at room temperature: 89 mV/V for NMOS and 73 mV/V for PMOS.

3.9 Analog performance at 4 K

The analog performance of 28 nm FD-SOI NMOS devices was reported down to 77 K in [142]. Here we extend the analysis down to 4.3 K by measuring the normalized drain current I_{DS} (L_G/W) and the normalized transconductance G_M (L_G/W) for different V_{DS}. Furthermore, the G_M/I_{DS} vs I_{DS} (L_G/W) metric is discussed from room temperature down to 4.3 K.

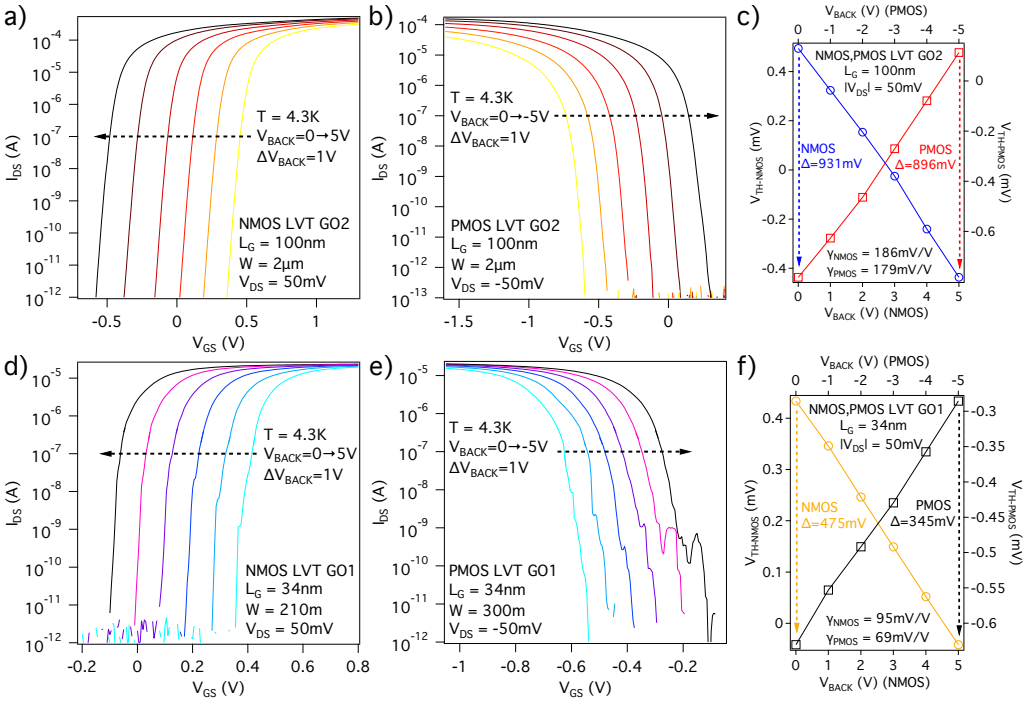


Figure 3.19: (a - b) the effect of V_{BACK} on NMOS and PMOS GO2 devices with $L_G = 100$ nm and (c) the tunability of V_{TH} at 4.3 K. (a - b) the effect of V_{BACK} on NMOS and PMOS GO1 devices with $L_G = 34$ nm and (c) the tunability of V_{TH} at 4.3 K.

The effect of L_G and V_{BACK} regarding G_M/W vs A_{v0} metric (where A_{v0} is the intrinsic voltage gain) is shown at 4.3 K.

First, we start the analysis of analog performance by comparing the I_{ON} currents from I_{DS} (L_G/W) vs V_{GS} for NMOS LVT GO1 device with $L_G = 34$ nm and $W = 210$ nm as shown in Fig.3.20 (a). That is why in this section we will also analyze the analog performance at $V_{DS} = V_{GS} = 0.3$ V. By comparing the $4.3K/296K$ gain at $V_{GS} = V_{DS} = 0.3, 1$ V after the V_{TH}-

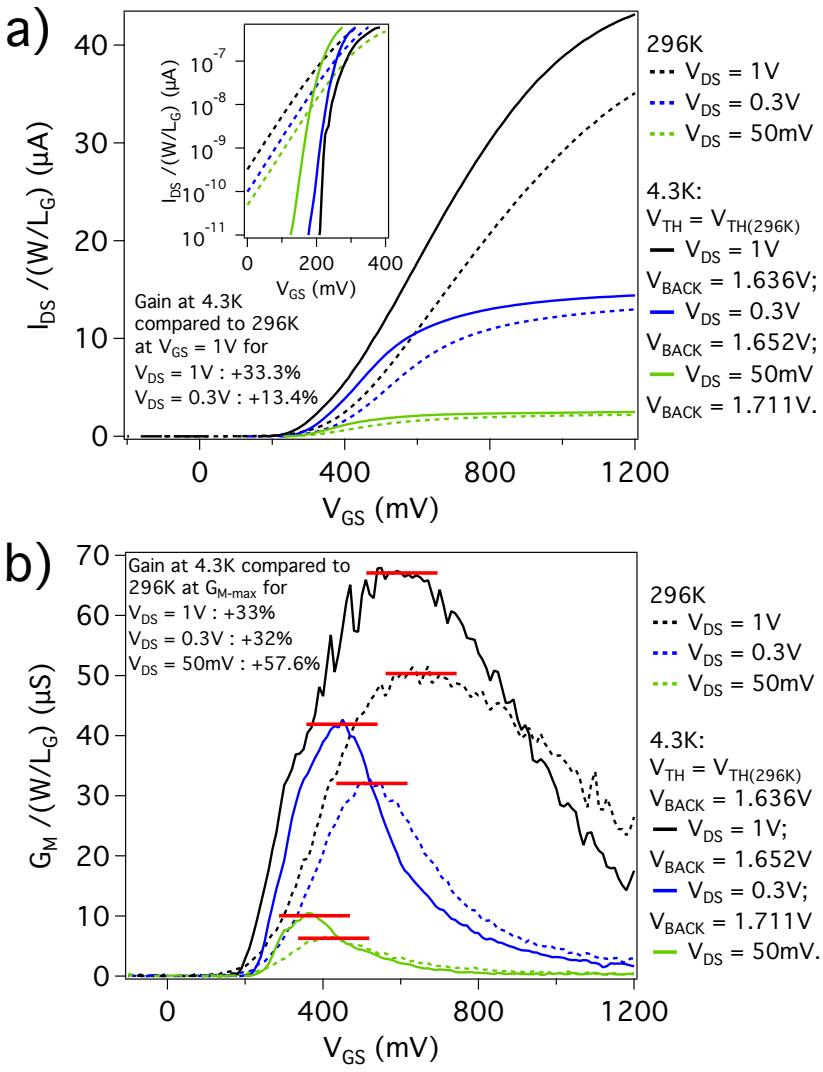


Figure 3.20: (a) I_{DS} (L_G/W) and (b) G_M (L_G/W) as a function of V_{GS} for different V_{DS} with $V_{BACK} = 0$ V and V_{BACK} applied to keep $V_{TH}(4.3K) = V_{TH}(296K)$.

compensation, we found an I_{ON} (L_G/W) increased by +33% for $V_{DS} = 1$ V

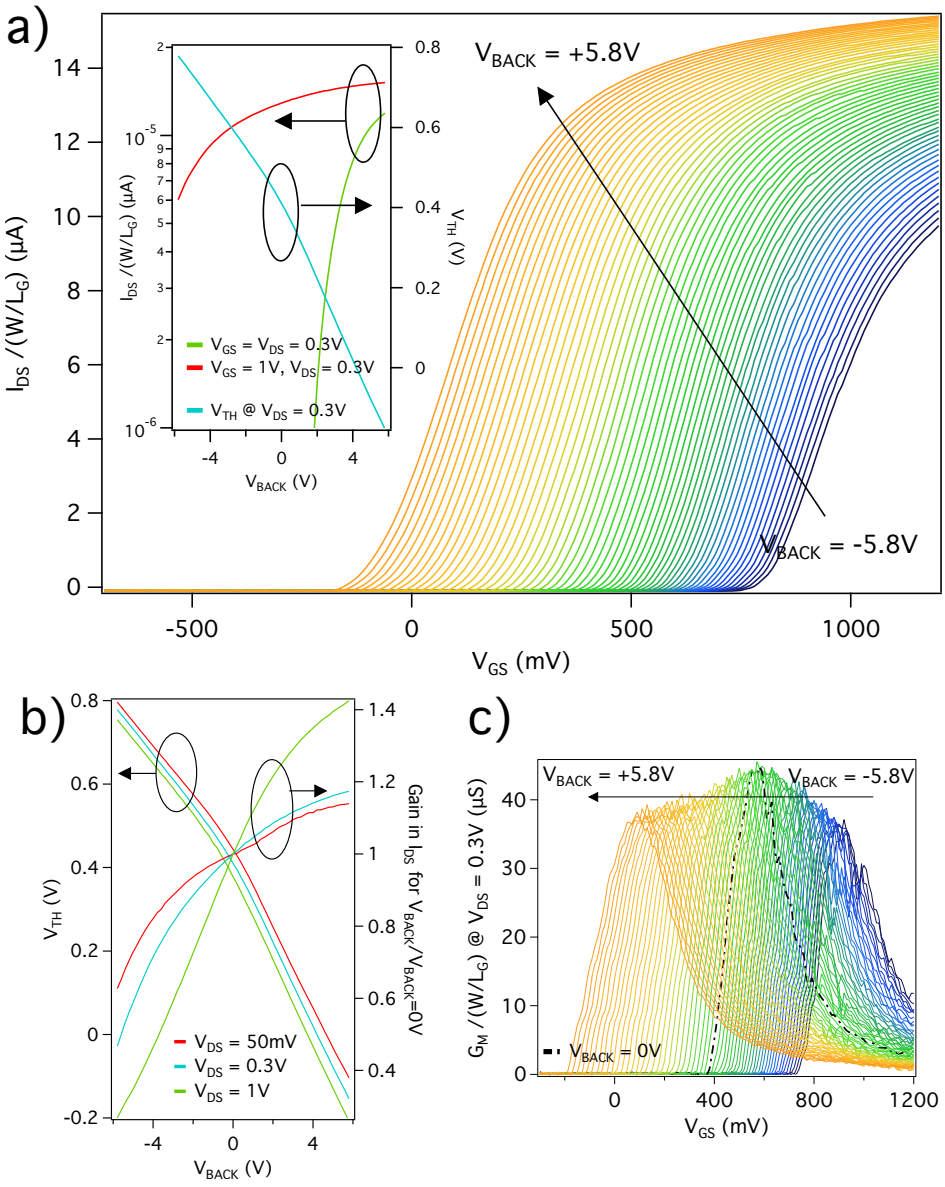


Figure 3.21: NMOS LVT GO1, L_G = 34 nm and W = 210 nm: (a) I_{DS} (L_G/W) and (b) G_M (L_G/W) as a function of V_{GS} for different V_{BACK} at $V_{DS} = 0.3$ V at 4.3 K. The inset shows the normalized I_{ON} current as a function of V_{BACK} for different V_{GS} at $V_{DS} = 0.3$ V. (b) The tunability of the I_{ON} gain under body-biasing and the corresponding V_{TH}. (c) G_M (L_G/W) as a function of V_{GS} for different V_{BACK} at $V_{DS} = 0.3$ V at 4.3 K.

and by +13.4% for $V_{DS} = 0.3$ V respectively due to the improved low temperature mobility as shown in Fig.3.20 (a). Then, by plotting I_{DS} (L_G/W) vs V_{GS} for the same NMOS device (see Fig.3.20 (b)), an increase of the

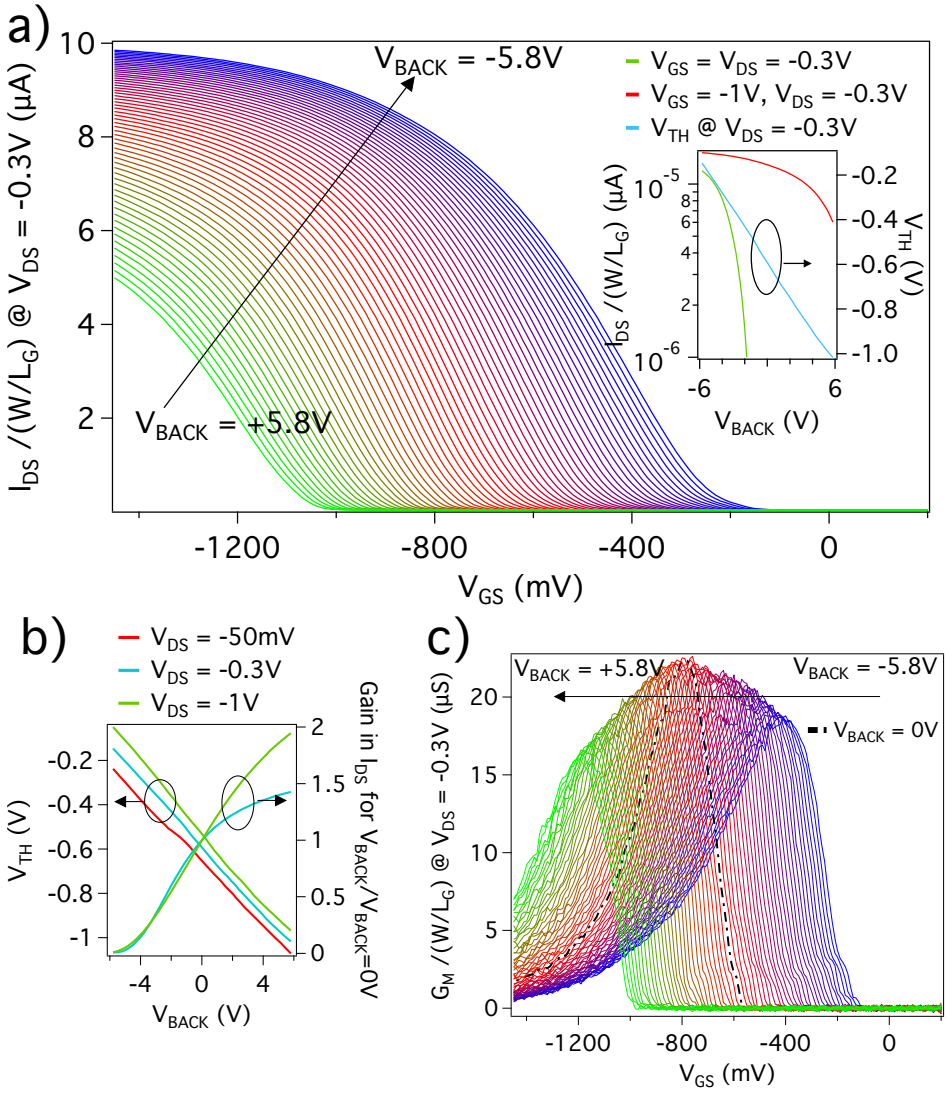


Figure 3.22: PMOS LVT GO1, $L_G = 34$ nm and $W = 300$ nm: (a) I_{DS} (L_G/W) and (b) G_M (L_G/W) as a function of V_{GS} for different V_{BACK} at $V_{DS} = -0.3$ V at 4.3 K. The inset shows the normalized I_{ON} current as a function of V_{BACK} for different V_{GS} at $V_{DS} = -0.3$ V. (b) The tunability of the I_{ON} gain under body-biasing and the corresponding V_{TH}. (c) G_M (L_G/W) as a function of V_{GS} for different V_{BACK} at $V_{DS} = -0.3$ V at 4.3 K.

normalized G_M at 4.3 K can be observed. At 77 K in FD-SOI devices, G_{M-max} was found to be increased by 28% and 42% for V_{DS} = 1 V and 50 mV respectively [142]. In our case, an improvement of G_{M-max} by 33% at V_{DS} = 1 V and 57.6% at V_{DS} = 50 mV is obtained due to the higher mobility. Similarly, for PMOS LVT GO1 devices with L_G = 34 nm and W = 300 nm, we found G_{M-max} at 4.3 K enhanced by 53% at $V_{DS} = -1$ V and 86% at $V_{DS} = -50$ mV.

It is worth mentioning that the gain in G_{M-max} for NMOS and PMOS devices can be logically correlated with the gain in low-field mobility extracted using the Y-function method in Chapter 5. It results in similar enhancement at 4.3 K as compared to RT, thus, we present another prove of the improvement in short-channel FD-SOI NMOS and PMOS mobilities at low temperature.

The extended body-biasing capability was already discussed in the previous section. Here, using $|V_{DS}|$ = 0.3 V, we demonstrate that a significant gain in normalized I_{ON} can be achieved under aggressive FBB for both short-channel NMOS and PMOS devices as shown in Fig.3.21 (a) and Fig.3.22 (a). Actually, in Chapter 5 we will demonstrate that the optimal supply voltage of 28 nm FD-SOI transistors (at which the energy per cycle is spent in the most efficient way [2]) can be reduced down to 0.3 V. That is why in the insets of Fig.3.21 (a) and Fig.3.22 (a), we plotted the I_{ON} for two different configurations with $|V_{DS}|$ = 0.3 V, $|V_{GS}|$ = 1 V and $|V_{DS}| = |V_{GS}|$ = 0.3 V. From these graphs, it can be concluded that body-biasing can be efficiently used to improve the device performance for the reduced power dissipation.

In Fig.3.21 (b) and 3.22 (b) the gain in the I_{ON} at $|V_{DS}|$ = 0.3 V is shown for NMOS and PMOS devices with respect to the current at V_{BACK} = 0 V.

Finally, the study of transconductance as a function of V_{BACK} is presented in Fig.3.21 (c) and 3.22 (c) for NMOS and PMOS devices. An interesting feature of the dependence of G_{M-max} as a function of V_{BACK} can be observed from these graphs. For both NMOS and PMOS devices, the maximum of G_{M-max} is obtained at V_{BACK} = 0 V.

In this section, the device analog performance is assessed down to 4 K through the key parameters such as the transconductance G_M, the output conductance G_D and the intrinsic gain $A_{v0} = G_M/G_D$. The figure of merit G_M/I_{DS} vs $I_{DS} \cdot L_G/W$ for NMOS and PMOS RVT GO1 transistors is shown in Fig.3.23 (a - b). Given that G_M/I_{DS} being inversely proportional to the subthreshold swing (in weak inversion) and proportional to μ_{EFF} (in strong inversion), the 'G_M/I_{DS} vs I_{DS}' metric at 4.3 K is strongly improved compared to room temperature. Indeed, we found a gain by 5.5 and 4.5 times for NMOS and PMOS devices with L_G = 28 nm for low/intermediate

currents suitable for base-band applications, where high gain and high precision are required [143]. A non-negligible gain for high currents as compared to 296 K can also be visible. This is suitable for high-frequency applications where high drive currents are needed [2]. Note, that a slightly irregular behavior for the lowest drain currents for PMOS shown in Fig.3.23 (b) is explained by the impact of dopants and can potentially be made more stable when L_G is slightly relaxed and the regular subthreshold behavior in $SS - I_{DS}$ is achieved.

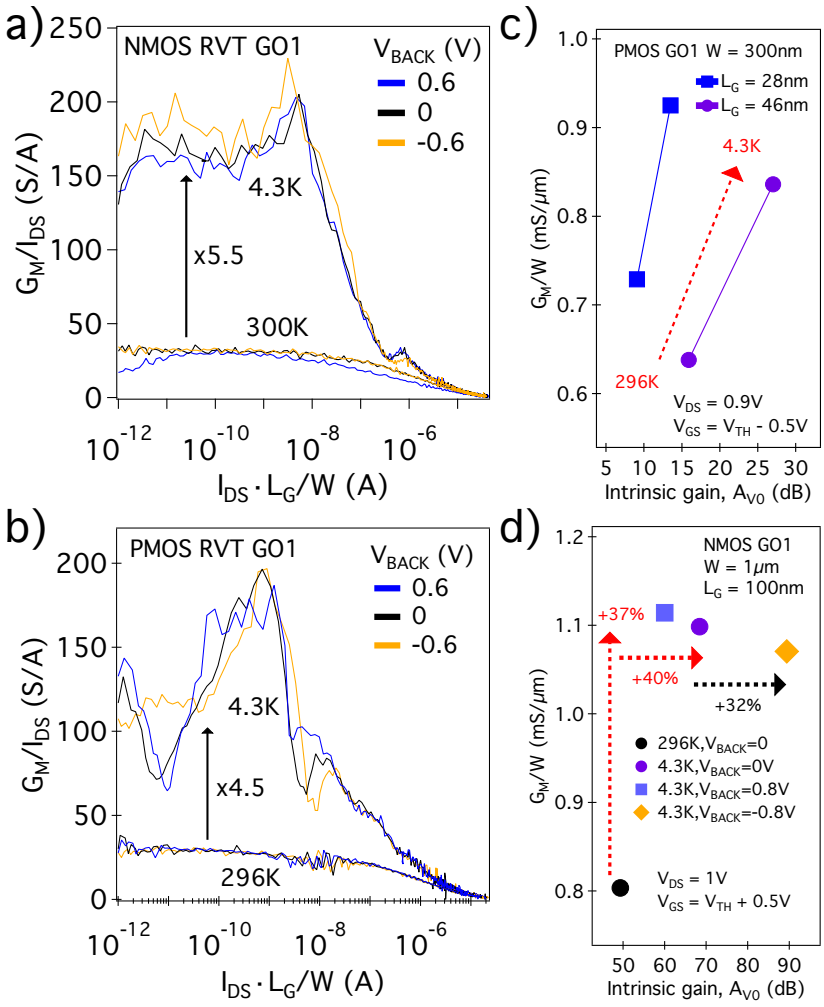


Figure 3.23: (a),(b) G_M/I_{DS} as a function of $I_{DS}(L_G)/W$ at 296 K and 4.3 K for NMOS and PMOS RVT GO1 devices with L_G = 28 nm and W = 80 nm at $|V_{DS}|$ = 0.9 V. (c),(d) G_M/W vs A_{v0} for different T, W, L_G and V_{BACK} for NMOS and PMOS GO1 transistors.

Finally, G_M/W as a function of the intrinsic voltage gain A_{v0} is shown in Fig.3.23 (c - d). It is demonstrated that low temperature and body-biasing significantly improve the transconductance G_M/W (due to increased μ_{EFF}) and A_{v0} (due to reduced G_D). All these metrics used to quantify the analog performance of 28 nm FD-SOI transistors are highly improved at 4.3 K as compared to 77 K [142].

3.10 Conclusions

Main conclusions of low-temperature study of digital and analog performance over a large number of different FD-SOI transistors are given below.

At low-temperature long-channel NMOS and PMOS transistors have a regular and stable subthreshold behavior suitable for both analog and digital applications. More precisely, SS_{LIN}, SS_{SAT} falls down to $7-12$ mV/dec and the effective mobility is highly improved.

Short-channel NMOS devices are much more stable in the subthreshold regime than PMOS. The later suffer at low temperature from the enhanced boron diffusion from Source/Drain regions leading to oscillatory, irregular behavior in the $SS-I_{DS}$ characteristics.

Using forward body-biasing modulate V_{TH} for NMOS and PMOS transistors is crucial to modulate in order to benefit from the low-temperature enhancement of mobility.

The low-temperature effective mobility extracted using the C-V split technique is greatly enhanced due to the suppression of phonon scattering for both thick (GO2) and thin gate oxide (GO1) transistors. It is higher for the thick gate oxide (GO2) devices due to the reduced impact of remote Coulomb scattering and soft-optical phonon scattering as the SiO_2/HfO_2 interface is located further from the channel. In addition, an efficient tuning of effective mobility with moderate FBB is demonstrated for all GO1, GO2 NMOS, and PMOS transistors.

By analyzing the doped channel PMOS device in terms of the cryogenic shift of V_{TH}, μ_{EFF} and subtreshold behavior, we emphasize on the importance of the undoped channel to improve device performance at cryogenic temperature.

The analysis of long-channel device variability revealed almost the same degree of variability in terms of V_{TH-LIN}, V_{TH-SAT} and I_{ON} at 4.3 K as compared to room temperature. Moreover, a very regular 4 K cryogenic behavior was demonstrated using $SS-I_{DS}$ metric.

Regarding the overdrive currents, we observed an important increase of I_{ODLIN} and I_{ODSAT} for short/long channel devices with a set of different

L_G and W. It was shown that I_{ODSAT}/W for $L_G = 28$ nm is the same for $W = 80...1000$ nm for NMOS and PMOS RVT GO1 devices.

We have argued that at low temperature the short-channel mobility is not completely dominated by the scattering on neutral defects from Source/Drain regions. An important improvement is found at 4.3 K for both NMOS and PMOS even for the shortest $L_G = 28$ nm.

We demonstrated the efficiency of body-biasing in tuning V_{TH} and I_{ON} currents within an extended range $-5.8... + 5.8$ V of V_{BACK} at 4.3 K.

The potential of 28 nm FD-SOI technology for cryogenic analog applications was also analyzed using different metrics.

Chapter 4

Low-temperature Saturation of the Subthreshold Swing in FD-SOI MOSFETs

A new model which explains the low-temperature behavior of subthreshold swing (SS) of FD-SOI MOSFETs is presented in this chapter. The modeling introduces a disorder-induced tail in the density of states at the conductance and valence band edges which (with Fermi-Dirac statistics) are used to calculate the mobile charge density and the current in the subthreshold regime.

In the first approach describing an energy-independent distribution of interface traps, for a set of MOSFETs with different gate oxide thicknesses and gate lengths, we were able: to (i) reproduce the saturation of SS at cryogenic temperatures in the weak inversion regime commonly observed in both bulk Si and FD-SOI transistors and (ii) to obtain the saturation of the threshold voltage (V_{TH}) below typically 40 K. Then, by accounting for the energy dependence of interface-trap distribution within the silicon bandgap, we qualitatively reproduce the tailing in $SS-I_{DS}$ characteristics which affects the subthreshold operation of MOSFETs at cryogenic temperatures.

By displacing the conductive channel from the top Si/SiO_2 to the bottom Si/BOX interface via forward back-biasing (FBB), we show that the disorder is not solely due to the defects on the interfaces since the same saturation of SS is observed for both N- and PMOS devices.

Moreover, dynamic threshold MOS (DTMOS) operation is successfully demonstrated for short channel NMOS transistor at 4.3 K. Indeed, a very steep SS below 3 mV/dec over more than 4 decades of I_{DS} and highly reduced V_{TH} by more that 250 mV compared to the case of $V_{BACK} = 0$ V are demonstrated under DTMOS operation with $V_{GS} = 16V_{BACK}$. Thus,

despite the limitations for minimal SS due to disorder, we demonstrated that thanks to body biasing, SS can be further reduced at 4.3 K. We discuss a potential interest of using such outstanding transistor's sharpness for both digital and analog applications at 4.3 K.

Finally, the outcomes of the physical modeling presented in this chapter capture most of the features of the subthreshold current at cryogenic temperatures and provide an in-depth understanding of the role of disorder in MOSFETs. Furthermore, our results might be of great interest for their implementation into existing compact models for the design of cryogenic circuits. A part of experimental data together with the model's description has been submitted for a publication in IEEE Electron Device Letter.

4.1 Experimental evidence of the saturation of SS in FD-SOI devices

The saturation of SS that occurs at temperatures below approximatively 40 K was already pointed out in Chapter 3. In this chapter, we develop a novel physical model, explaining the temperature dependence of SS from room temperature down to 4.3 K. Although the SS-saturation was observed at both low and high drain voltages, the experimental data and the correlation with the developed model will be shown only for the case of $V_{DS} = 50$ mV. Actually, almost no difference between SS_{LIN} ($V_{DS} = 50$ mV) and SS_{SAT} ($V_{DS} = 0.9$ V) was experimentally observed for long-channel transistors, as it has been demonstrated in Chapter 3, since the subthreshold current is mainly governed by the diffusive transport [125]. Considering only the case of low V_{DS} simplifies the analysis allowing us to avoid the problems of short-channel effects such as drain-induced-barrier-lowering ($DIBL$). Indeed, to describe the operation of short-channel MOSFET at high V_{DS}, $DIBL$ should be included in the calculation of SS [139] since the channel-to-drain capacitance can become comparable to the gate capacitance. The gate capacitance per unit area imposed by the transistor's geometry can be expressed as $C_{OX} = k\epsilon_0/t_{EOT}$, where $k = 3.9$ - is the relative dielectric constant of SiO_2, ϵ_0 the free-space permittivity and t_{EOT} the equivalent oxide thickness. To support the generality of our modelling, two cases of thin (GO1, $t_{EOT} = 1.55$ nm) and thick (GO2, $t_{EOT} = 3.7$ nm) gate oxide will be addressed.

The subthreshold drain current is well known to have an exponential gate-voltage dependence because of the diffusive nature of transport in the weak inversion regime (at higher inversion charge density N_{INV}, the drift

component of transport due to the transverse electrical field should be taken into account). The $I_{DS} - V_{GS}$ relation can be expressed as $I_{DS} \sim e^{eV_{GS}/k_BT}$ [125], where e is the elementary charge, k_B is the Boltzmann's constant, and T is the temperature. Then, the expression for SS can be obtained by taking the derivative of V_{GS} with respect to $\log I_{DS}$:

$$SS(T) = dV_{GS}/d\log I_{DS} = \ln 10 \; k_BT/e \tag{4.1}$$

It should be noted that (4.1) is valid for an ideal, defectless transistor. This equation gives 60 mV/dec at 300 K which is the well know thermal activation limit for the transistor's sharpness at room temperature. However, with a few hundred fabrication process steps, a transistor is very likely to contain various kinds of defects resulting from a crystalline disorder, interface traps, residual impurities and strain, charges in the oxide, surface roughness etc. Despite the existence of different types of disorder, the interface traps density (D_{IT}) is the main parameter used to quantify the degradation of SS for FD-SOI transistors (considering bulk Si MOSFETs, one should also take into account the depletion capacitance) [139]. The interface traps located at the Si/SiO_2-interface act as a parasitic capacitance connected in series with C_{OX}. Moreover, the semiconductor capacitance (C_{Si}) [139] arising from the inversion charge layer connected in series with C_{OX} should also be taken into account. We will discuss the potential drops over both C_{OX} and C_{Si} and how they contribute to V_{GS} in section 'First approach to model $SS(T)$: disorder-induced tail below band edges and $m = 1$'. Finally, for an FD-SOI transistor, one obtains the following expression for SS [139]:

$$SS(T) = ((C_{OX} + C_{IT} + C_{Si})/C_{OX}) \ln 10 \; k_BT/e = m \ln 10 \; k_BT/e \tag{4.2}$$

where C_{Si} is very small compared to C_{OX} in the weak inversion region and thus m is mainly given by the value of C_{IT} with respect to C_{OX}. A more complete $SS(T)$ description can be obtained by connecting the BOX capacitance C_{BOX} in series to the previously mentioned ones and considering C_{IT} at the Si/BOX interface [144]. However, the additional term due to the presence of the back interface (Si/BOX) is canceled out in the weak inversion regime and (4.2) can be used (see the equation for the case of single sheet conductivity and equal trap density for top and back interfaces in [145]).

One of the numerous advantages of FD-SOI is that close-to-one values of m give an excellent SS(300 K) thanks to good electrostatic control over the undoped and fully-depleted channel [115]. Finally, we should note that

whereas for long-channel devices a finite C_{IT} ($C_{IT} = e^2 D_{IT}$) is responsible for m slightly higher than 1, short-channel devices also suffer from short-channel effects which cause more degradation of SS and higher m.

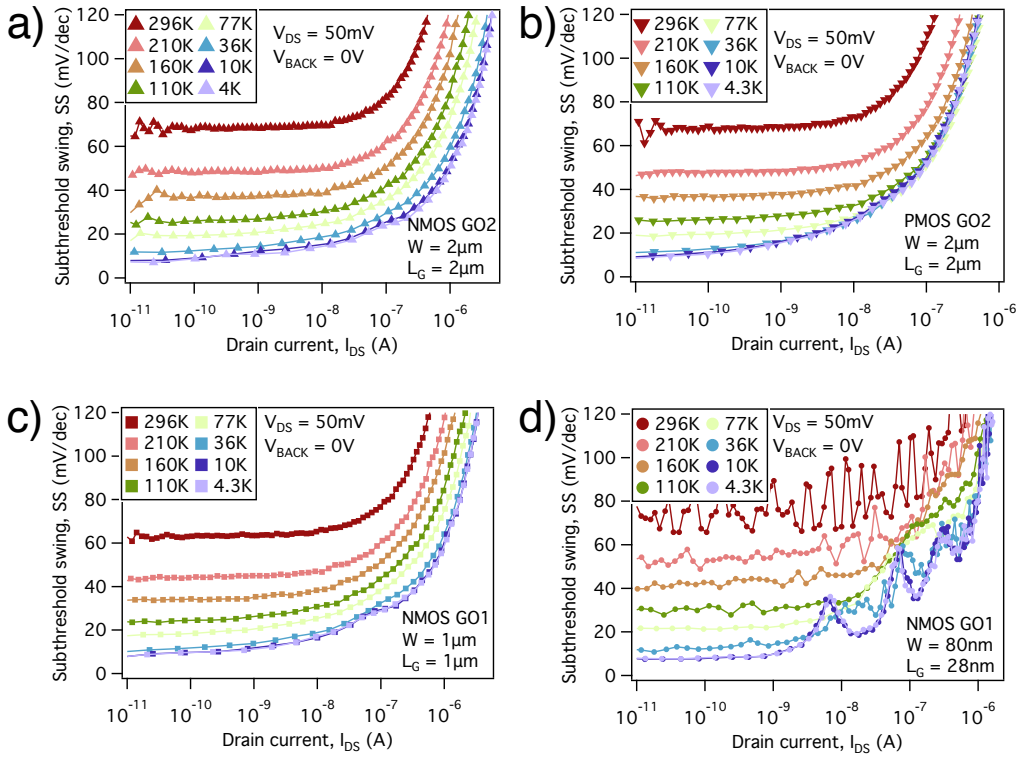


Figure 4.1: Cryogenic behaviour of different MOSFETs at $V_{DS} = 50$ mV using the $SS - I_{DS}$ - metric (a)-(b) Long-channel, thick EOT (GO2) LVT N-, and PMOS transistors. (c) Long-channel RVT NMOS with thin EOT (GO1). (d) Short-channel, GO1 RVT NMOS transistor with relatively stable subthreshold behaviour at low temperature.

The transfer characteristics of MOSFETs down to 4.3 K analyzed in this chapter were already presented in Chapter 3. The $SS - I_{DS}$ curves will be the main metric used in this chapter for a better understanding of low-temperature behavior of MOSFETs in the subthreshold regime. In Fig.4.1, the evolution of $SS - I_{DS}$ down to 4.3 K is shown for four different long and short-channel transistors. Each successive data point corresponds to the change of V_{GS} by 5 mV. We also note that these measurements were performed in the absence of body-biasing ($V_{BACK} = 0$ V). For all the transistors presented in Fig.4.1, the saturation of SS can be clearly observed:

for instance, the curves corresponding to 10 K and 4.3 K are superimposed. Oscillatory behaviour above few nA for the short channel NMOS with $L_G = 28$ nm and $W = 80$ nm can be seen in Fig.4.1(d). It is explained by the very small geometrical dimensions which would lead to the formation of single electron transistor (SET) due to mesoscopic fluctuations and quantum confinement effects for ultra-small devices [125, 139]. The SET-behaviour and analysis of quantum dots in 28 nm FD-SOI N- and PMOS short-channel devices will be discussed in Chapter 6. The boron dopants diffused from source/drain regions hinder a stable and oscillationless cryogenic operation of FD-SOI PMOS with $L_G = 28$ nm [122, 112, 114] at low V_{DS}. Actually, the subthreshold operation of short-channel PMOS becomes much more stable when L_G is relaxed to 46 nm but for such devices, we could not perform the measurements within the whole temperature range but only at room temperature and 4.3 K. This is the reason why we do not address short-channel PMOS devices. In this section, we restrict our analysis only to short-L_G NMOS devices. Another important observation from the data in Fig.4.1 is an increased 'curving' in $SS - I_{DS}$ at low temperatures. Contrarily to the 'flat' behavior of SS(296 K) with very small dependence on I_{DS} (or V_{GS}), this is no longer the case at low temperatures. We will give an explanation for such behavior of $SS - I_{DS}$ in terms of energy-dependent interface traps later in section 'Second approach to model $SS(T)$: disorder-induced tail below band edges and $m = m(E)$'.

In this chapter, the quantitive comparison between the model and experimental data is performed only for the very weak inversion regime. The values of SS for all samples were extracted at $I_{DS} = 10$ pA and are shown in Fig.4.2. A clear deviation from the temperature dependence derived in (4.2) can be observed below 40 K. The values of m_{2-4} were extracted at room temperature by comparing the measured SS with the theoretical 60 mV/dec value. m_1 was extracted at 160 K due to parasitic noise presented in the room temperature data (see Fig.4.1(d)). In the legend of Fig.4.2, the notations NMOS/PMOS GO2 long correspond to the transistor's dimensions given in Fig.4.1 (a-b) and the NMOS GO1 long/short devices correspond to Fig.4.1 (c-d)

The subthreshold swing at 4.3 K for both long and short channel devices reaches $7 - 8$ mV/dec which is much higher than the theoretical prediction from (4.2) giving a value below 1 mV/dec. It is worth mentioning that by analyzing more than 50 samples with different dimensions and EOT, we always observed the saturation of SS. This suggests that this phenomenon is of 'universal' nature. Moreover, almost the same SS(4.3 K,10 pA) were observed with a statistical variation of $\pm$ 1 $-$ 2 mV/dec for long-channel devices and a slightly higher variation for short channel devices.

In addition, although the case of high V_{DS} is not discussed in this chapter, as previously mentioned, the same $SS(4.3\ \mathrm{K})$ at $V_{DS} = 0.9$ V were found for long-channel devices and a slightly higher value of SS (12 mV/dec) for the short-channel NMOS with $L_G = 28$ nm.

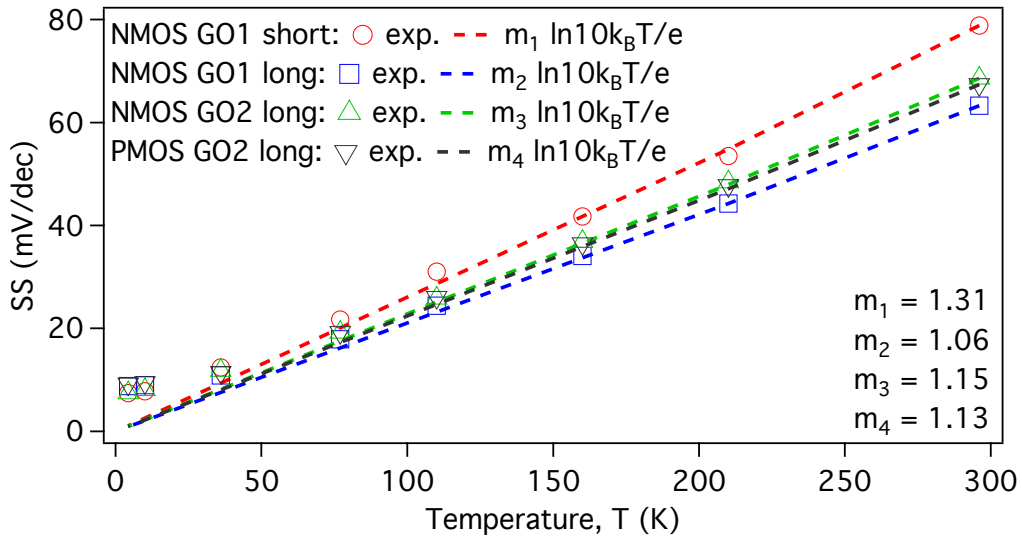


Figure 4.2: $SS(T)$ extracted in the weak inversion regime at $I_{DS} = 10$ pA for samples presented in Fig.4.1. Using $\ln 10\, k_B T/e$ with different m-factors, the experimental data down to roughly 40 K can be reproduced. Below this temperature, the data points deviate from the classical $SS(T)$ dependence.

Finally, to sum up the experimental data presented in this section, we emphasize the fact that the saturation of $SS(T)$ was generally observed in all characterized samples and up to now, there exists no theory explaining this behavior for temperatures ranging from 300 K down to 4.3 K. A value of 7 mV/dec was recently reported also at 20 mK in FD-SOI devices at $V_{BACK} = 0$ V [145] which reinforces the hypothesis of complete saturation of SS at very low temperatures. Also, the stronger V_{GS} dependence of $SS(T)$ at low temperature is another important general observation from experimental data. Finally, we need to be able to explain and numerically describe these both phenomena which can be crucial for cryogenic compact modeling and further design of robust CryoCMOS circuits based on 28 nm FD-SOI technology.

4.2 Existing theories and approaches to explain $SS(T)$ in bulk Si and SOI technologies

The temperature dependence of the subthreshold current was a very studied topic of research back in the 90ties. For instance, a physics-based model for the subthreshold current in µm bulk Si MOSFETs with $m = m_0\ (1/2C_{OX})\sqrt{q\epsilon_0\kappa_{SiO_2}/\psi_B}$ (ψ_B is the bulk potential and m_0 is the SS-degradation measured at room temperature) was successfully used for compact modelling and design of cryogenic circuits [146, 121]. However, for the sub-µm technologies, such modeling failed to predict the values of SS at deep cryogenic temperatures down to 4.3 K [121].

Recently, due to the growing interest in cryogenic electronics to run efficiently large qubit-systems [67, 14, 20], more advanced CMOS technologies have been carefully studied at temperatures as low as 20 mK. Standard 160 nm and 40 nm technologies were studied down to 100 mK in [136] and $SS(1\text{ K}) = SS(100\text{ mK}) = 10$ mV/dec were reported for long-channel devices. This saturation was explained by a rapid increase of the depletion capacitance C_{DEP} due to the freeze-out of dopants in the channel below a certain temperature (note that highly doped and degenerate source/drain regions do not suffer from the freeze-out phenomenon down to 4 K [124]). Then, the saturation of SS was transformed into a temperature-dependent parameter m reaching very large values at 100 mK with $m = 500$ [136]. Similar results were reported by the group of TU Delft for Si bulk transistors fabricated in 160 nm technology [147]. They are shown in Fig.4.3 (a). A clear saturation below approximatively 100 K is also observed in the dynamic threshold voltage MOSFET (DTMOS). Another experimental observation from this work was that standard bipolar transistors fail below roughly 77 K (see Fig4.3 (a)) as it is logically expected for a bipolar transistor with a strong reduction of minority carrier lifetime at low temperature [148]. Therefore, MOSFET transistors appear to be the best choice for cryogenic circuits fabricated with standard semiconductor technologies that operate at 4 K and below. The same approach of temperature-dependent m was also applied for cryogenic characterization of 28 nm bulk Si resulting in $m = 10 - 20$ for long channel ($SS = 10 - 20$ mV/dec) and $m = 20 - 30$ for short channel devices ($SS = 20 - 30$ mV/dec) at 4 K [149]. Furthermore, an analytical temperature $m(T)$ was incorporated in a cryogenic compact model for 160 nm bulk Si [150]. But again, in all herein mentioned references, only analytical description of $SS(T)$ were proposed without any

rigorous physical explanation.

More recently, the $SS(T)$ of 28 nm bulk Si long channel transistors measured at 300 and 4 K has been argued to be strongly related to interface trap density [151]. In Fig. 4.3 (b), the effect of 4 traps (arbitrarily located in the silicon band-gap and separated by k_BT) on the mobile charge density (which is proportional to the subthreshold current) is shown. Although the model allowed to fit the 300 and 4 K data, this choice of D_{IT}-energy distribution and the inability to reproduce the SS-behaviour for intermediate temperatures between 300 and 4 K make this theory suitable only for analytical modelling at a given temperature without a complete physical justification.

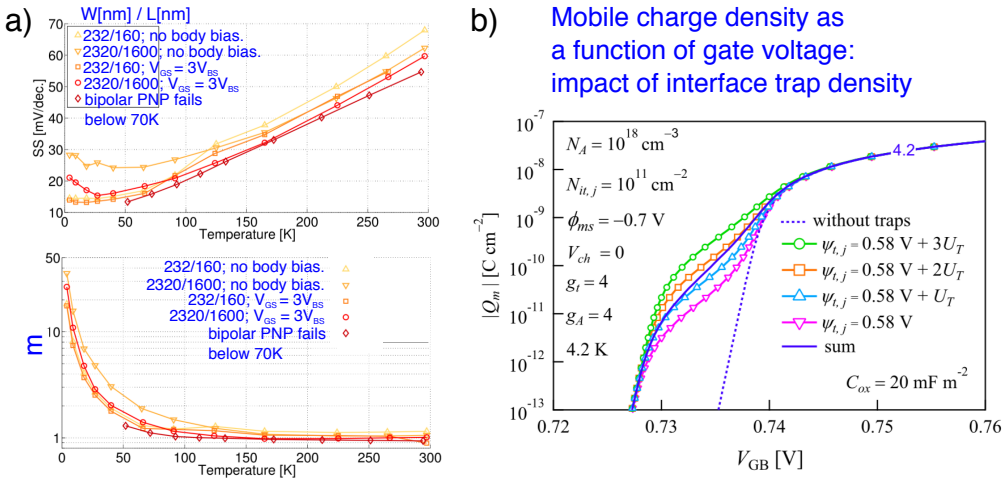


Figure 4.3: (a) Subthreshold swing of standard 0.16 μm bulk Si: non-ideality factor m strongly depends on temperature. The same saturation of $SS(T)$ is also observed for DTMOS. Adapted from [147]. (b) Standard 28 nm bulk Si: interface trap density is introduced in the silicon band-gap with an energy spacing $U_T = k_BT$ to model the mobile charge. A clear increase of $SS(4.2\text{ K})$ is observed as the interface trap density is considered. Adapted from [151].

In partially-depleted SOI (PD-SOI) technologies with channel doping, much higher SS values than these given by (4.2) were measured at 10 K [138] (10 – 30 mV/dec). A strong inhomogeneity of the energy profile of interface states in the band-gap was put forward to explain $SS(T)$. The authors proposed the following explanation: given that at low temperature the Fermi level approaches the band edges and the energy dependence of D_{IT} rapidly increases close to the band edges (at 4 K, $10^{13} - 10^{14}\ cm^{-2}eV^{-1}$

[152]), an increase of C_{IT} is responsible for the large SS values. Due to low channel doping in PD-SOI, the role of C_{DEP} was not considered to be crucial in the $SS(T)$ dependence.

Even though cryogenic characterization of 14 nm FD-SOI devices provided SS values close to the theoretical limit $SS = 15.3$ mV/dec at 77 K with rather weak D_{IT}-dependence in [140], the temperatures below 77 K were not addressed.

Similarly to 28 nm FD-SOI devices, $SS(4K) = 8$ mV/dec was reported for short-channel silicon nanowire transistors fabricated with Leti's Trigate technology [153].

There exist several techniques commonly used to evaluate D_{IT} : (i) by studying the temperature dependence of SS which takes into account fast traps located at the Si/SiO_2 interface and ignores the slower traps due to, for instance, parasitic charges in oxide (as we discussed previously); (ii) by doing low- and high-frequency capacitive sensing [125]; (iii) by measuring transconductance as a function of frequency [152]; by using spectroscopic charge pumping where a pulse is applied to the transistor's gate (it means filling the interface traps with electron and holes) and then measuring the recombination current flowing in a specific design of gated diode [154]. All these techniques show an important increase of D_{IT} close to the band edges.

In Fig.4.4 (a), the D_{IT} profiles within the silicon band-gap for electrons and holes are shown for planar SOI devices [154]. An important increase of D_{IT} close to the band edges is observed.

Finally, 28 nm FDSOI NMOS devices were recently measured down to 20 mK with the extraction of D_{IT} from the $SS(T)$-behavior [145]. The SS-model dependent on the density of interface traps at the top and bottom interfaces was taken from [144]. The results are shown in [154]. We note the anomalously high D_{IT} values below 4 K reaching few $10^{17} eV^{-1} cm^{-2}$ at 20 mK. Such unrealistic values (much larger than the silicon free-electron 2D density of states available in the channel) were explained by the use of Maxwell-Boltzmann statistics to describe the subthreshold current.

Summarizing the experimental results of $SS(T)$ for different technologies mentioned in this section, we would like to emphasize that although some of the models could give an acceptable correlation with experiment, no one could physically explain the complete temperature dependence $SS(T)$ from 300 K down to sub-K temperatures. In the next two sections, we will demonstrate a new physical model based on a narrow tail in the DOS close to the band edges and m moderately depending on energy. The increased gate-voltage dependence in $SS - I_{DS}$ (see Fig.4.1) is also captured by our theory. Finally, our modeling approach also reproduces another important experimental observation in both bulk and SOI transistors: the saturation

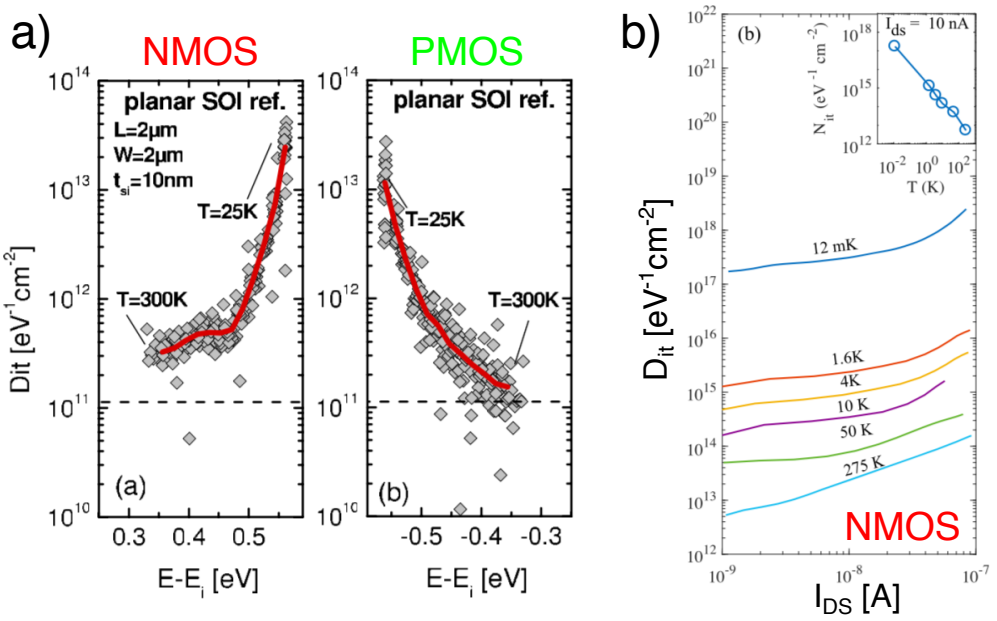


Figure 4.4: (a) Energy distribution of interface traps (symbols) for planar FD-SOI devices. E_i stands for the intrinsic Fermi level. The profiles are obtained by scanning temperature from 300 K down to 25 K with $\delta T = 25$ K. The bold red line represents the mean value $D_{IT}(E)$. The dashed black line is the directly measured mean value of $D_{IT}(E)$ over the full energy range at 300 K. Adapted from [154]. (b) $D_{IT} - I_{DS}$ in the inversion regime measured in long-channel 28nm FD-SOI NMOS devices. $SS(T)$ is used to extract the $D_{IT}(T)$ dependence. Adapted from [145].

of threshold voltages at cryogenic temperatures [123].

4.3 First approach to model $SS(T)$: disorder-induced tail below band edges and constant m

The model presented in this section will be developed for the case of NMOS with thick EOT (GO2), although we will see that the same approach can also be applied to all NMOS and PMOS samples presented in the first section.

First, in our approach, we assume that the subthreshold current is given only by diffusive transport (with a constant diffusion parameter or constant

mobility) and the drift component dependent on the transverse electric field (or V_{DS}) is neglected [125]. Thus, I_{DS} becomes proportional to the mobile charge density $n(\Psi_S)$, where Ψ_S is the surface potential, i.e. the electrostatic potential in the semiconductor [125] (see Fig.4.5 (b)). The discretization of the energy in the direction perpendicular to the interface charge layer results in the formation of 2D subbands [124]. Then, the total sheet electron density can be found by summing the contribution from each subband and neglecting the intervalley scattering (following the Kubo-Greenwood formalism) [155]. In our modeling of FD-SOI, we assume that only the lowest subband is occupied which is a reasonable assumption for a very thin channel and relatively widely spaced subband energies [139]. Then, using the Fermi-Dirac statistics for the occupation of electron states [139, 156], n can be expressed as a function Ψ_S in the following way:

$$n(\Psi_S) = \int_{-\infty}^{\infty} f(E) N_c^{2D}(E) dE \tag{4.3}$$

with the Fermi function $f(E) = 1/(e^{(E-E_F)/k_BT} + 1)$ and a step function for the two-dimensional density of states $N_c^{2D}(E)$ from zero to $N_c^{2D} = g_v m^*/\pi\hbar^2$ [139] at the conductance band edge which we define as $E_c = E_c^0 - e\Psi_S$.

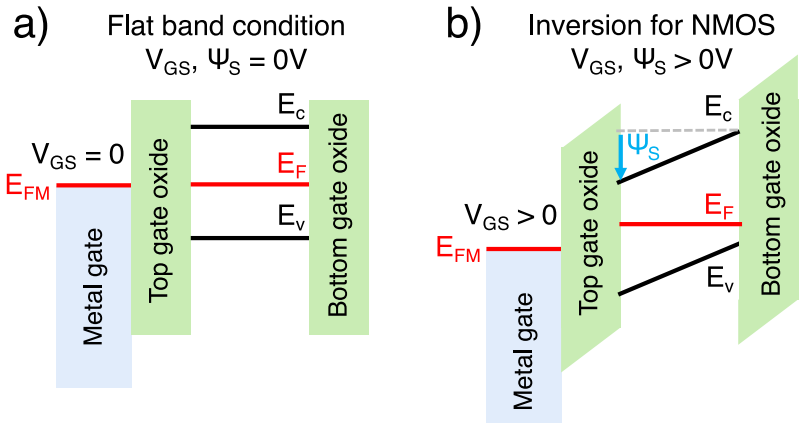


Figure 4.5: (a) Flat band condition when no gate voltage is applied. It is assumed that there is no band bending and the Fermi level in the metal gate (E_{FM}) and in the channel (E_F) are aligned. (b) The inversion regime for fully-depleted NMOS when a positive gate voltage is applied. Note that both schematics are simplified, i.e. we do not consider the bulk silicon located below BOX and there is only one surface potential at the top interface.

For the flat-band condition where no gate voltage is applied and $\Psi_S = 0$, the Fermi level is taken at mid band-gap with $E_c^0 = 0.55$ eV (see Fig.4.5 (a)) which is a reasonable assumption since for non-defective undoped semiconductors the Fermi level (see E_F in Fig.4.5) must be positioned close to mid-gap to satisfy the charge neutrality in the material [125]. m^* is the effective electron mass in the direction perpendicular to transport and in our case is equal to $m^* = 0.19\ m_0$ [139] with m_0 the free-electron mass. $g_v = 2$ is the silicon valley degeneracy factor. Note that we neglect the weak-temperature dependence of silicon band-gap, changing from 1.125 at room temperature to 1.17 eV at 4 K [157] and consider 1.1 eV for the whole temperature range. Then, by applying the Gauss's law at the Si/SiO_2 interface to relate the drop of potential over gate oxide to the inversion charge density [139], the equilibrium electron density $n(\Psi_S)$ can be transposed to $n(V_{GS})$ as :

$$V_{GS} = \Psi_S + n(\Psi_S)e/C_{OX} \tag{4.4}$$

In (4.4) we neglect the C_{IT} contribution ($m = 1$) and throughout this section suppose that m does not depend on temperature.

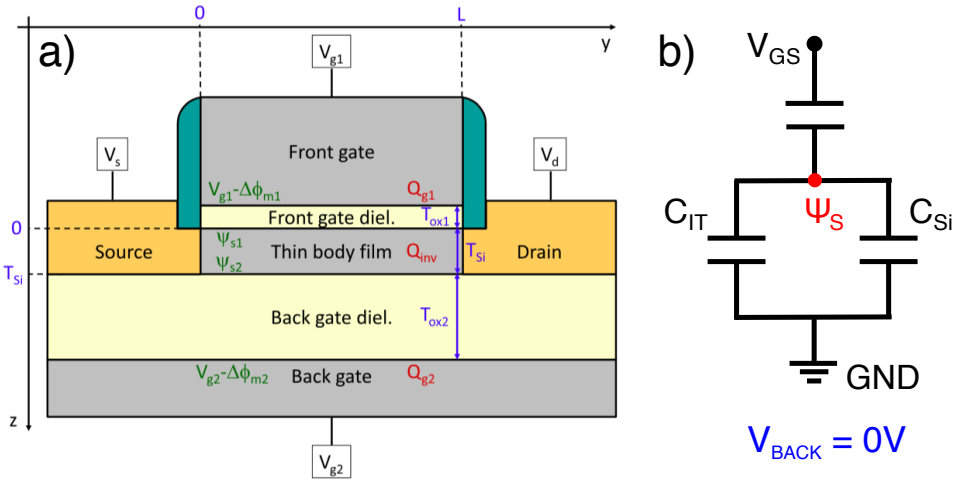


Figure 4.6: (a) A sketch from [158] giving the ensemble of complex parameters used in FD-SOI compact modelling. (b) A simplified equivalent circuit used for the modelling in this work.

Actually, a realistic FD-SOI compact modeling reproducing all transistor's characteristics (V_{TH}, SS, I_{ON}, effects of body-biasing, etc.) takes into account several other MOSFET parameters as it can be seen from Fig.4.6 (a). Among the parameters that should be considered, there is the metal

workfunction for the top and back gate and the density of fixed charges at the interfaces and in the oxides that define V_{TH}, the surface potential at the bottom interface due to the back-gate connected to the channel via the BOX capacitance, etc. [158, 159]. Since the aim of our model is to explain the saturation of $SS(T)$, we will assume that there is no difference between the Fermi levels E_{FM} and E_F at $V_{GS} = 0$ V. In our case, we fix the zero-level energy at the mid-gap. Therefore, the equivalent circuit considered for the zero body-biasing regime is given in Fig.4.6 (b).

Using (4.3) and (4.4), the calculated $n(V_{GS})$ data for a sharp band edge shown in Fig.4.7 (a), reveal the exponential dependence $I_{DS} \sim e^{eV_{GS}/k_BT}$ reported in Fig.4.7 (b). This rather simplified model description confirms the linear dependence of $SS(T)$ given in (4.1). However, taking into account only the Fermi-Dirac statistics does not explain the saturation of SS experimentally observed at low temperatures in Fig.4.2. The calculated SS continuously decreases giving 1 mV/dec at 5 K and 0.4 mV/dec at 2 K as it can be seen in Fig.4.7 (c). It should be noted that I_{DS} in Fig.4.7 is given in arbitrary units on a wide range of drain current to match the experimental data as shown in Fig.4.1.

Thus, to describe the saturation of SS at low temperatures, a broadened band edge was added to the density of states in the form $N_c^{2D} e^{(E-E_c)/k_BT_0}$ for $E < E_c$ (see Fig.4.7(d)) where k_BT_0 represents the extend of the exponential tail resulting from, e.g., crystalline disorder, residual impurities, strain, surface roughness, etc. To find the experimentally observed saturation at approximatively 7 mV/dec, we set T_0 to 35 K ($k_BT_0 = 3$ meV).

Actually, the exponential tail close to the of band edges in disordered materials was firstly introduced by Lifshitz in the 60ties [160]. It was considered important to explain the DOS in the band-gap for heavily doped semiconductors [161, 162]. The tail of localized states leading to a non-zero density of states in the band gap depending on the dimensionality of disordered material can take many different forms such as exponential, Gaussian, power laws, etc [163]. The localized states can contribute to the mobile charge density via Mott variable-range hopping (tunneling of carriers despite the presence of potential barrier) [164].

Although we do not know the exact nature of the complex disorder in FD-SOI, we chose an exponential tail of $k_BT_0 = 3$ meV width that is much narrower than the D_{IT} - profiles shown in Fig.4.4 (a). The latter extends over more than 100 meV.

Finally, by putting the density of states in the form of $N_c^{2D} e^{(E-E_c)/k_BT_0}$ in (4.3) (Fig.4.7 (d)), we calculated the subthreshold current shown in Fig.4.7 (e). The saturation of SS at low temperatures can be clearly observed. Also, such modeling predicts the saturation of threshold voltage generally

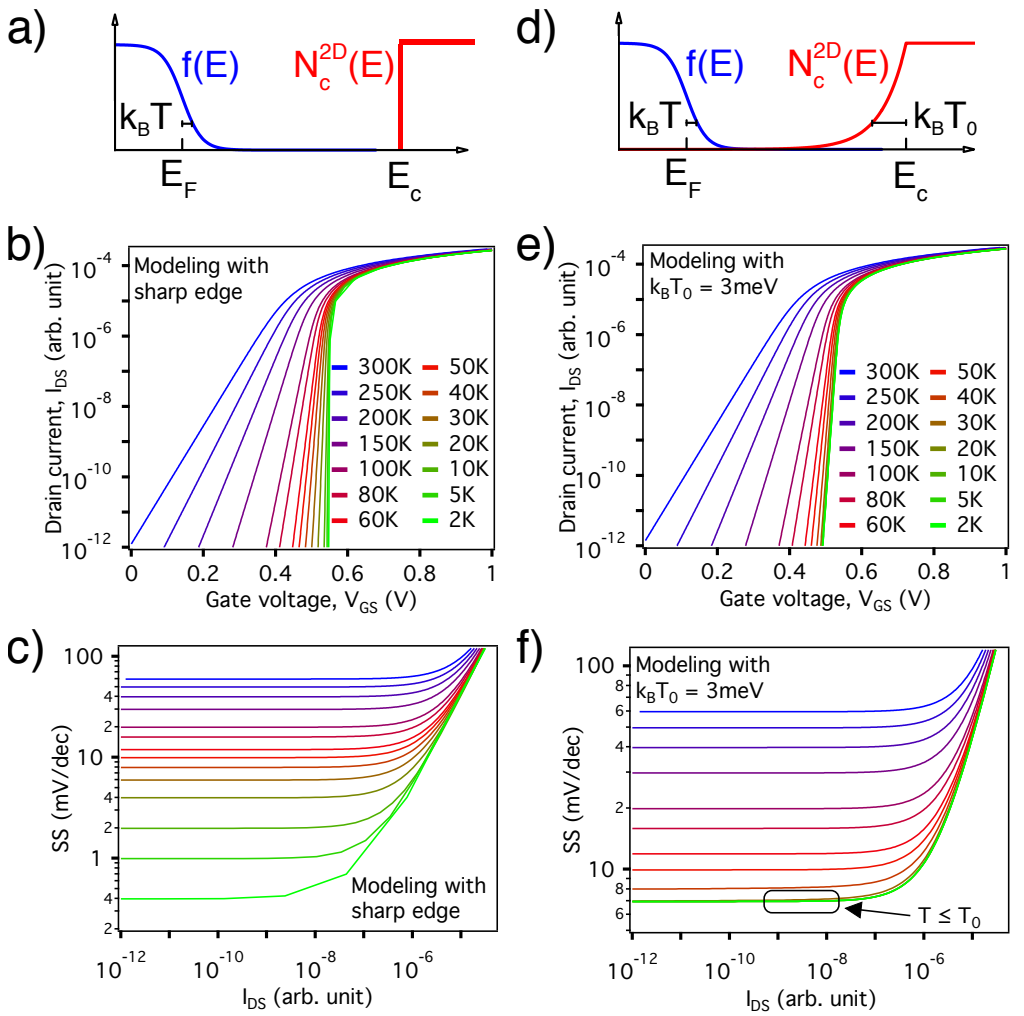


Figure 4.7: (a) Schematic representation of the exponential tail of the Fermi function $f(E)$ for $E > E_F$ and of the sharp conduction band edge. (b) Calculated I_{DS} as a function of V_{GS} for different temperatures from 300 to 2 K. (c) $SS - I_{DS}$ extracted from (b) plotted in log scale : no saturation of SS occurs. (d) Schematic representation for a tail in the DOS $N_c^{2D}(E)$ for $E < E_c$. (e) same as (b) but calculated with $k_BT_0 = 3$ meV. Note that the saturation of V_{TH} can also be observed. (f) $SS - I_{DS}$ for different temperatures: $SS(T)$ saturates to 6.94 mV/dec below 35 K. Note that the gate voltage dependence of SS is flat up to V_{TH} which is not the behavior observed in the experiment.

observed for long- and short-channel FD-SOI devices (see Chapter 3).

$SS - I_{DS}$ plotted in log scale for the case of k_BT_0 shows the saturation

of SS for $T < T_0$ as it can be seen from Fig.4.7 (f).

Now, our model can be compared with the experimental data shown in Fig.4.2. In Fig.4.8, the experimental data are normalized by m estimated from the deviation of SS from 60 mV/dec at room temperature. Even though the model was derived for NMOS GO2 devices, we note an excellent agreement for PMOS GO2 and NMOS GO1 long and short-channel devices. The gate oxide thickness does not play an important role in the modeling of subthreshold current since in the weak inversion regime $C_{Si} \ll C_{OX}$ and V_{GS} drops mainly on C_{Si}. Since no difference in the metal gate workfunction was considered at $V_{GS} = 0$ V (see the flat band condition shown in Fig.4.5 (a)), we conclude that the same modeling can be applied to PMOS devices with the same band tailing at the valence band edge.

Finally, we remind that only diffusive transport is considered in our model. To model the current above V_{TH}, a complex carrier mobility dependence on temperature (which we already discussed in Chapter 3) should be taken into account.

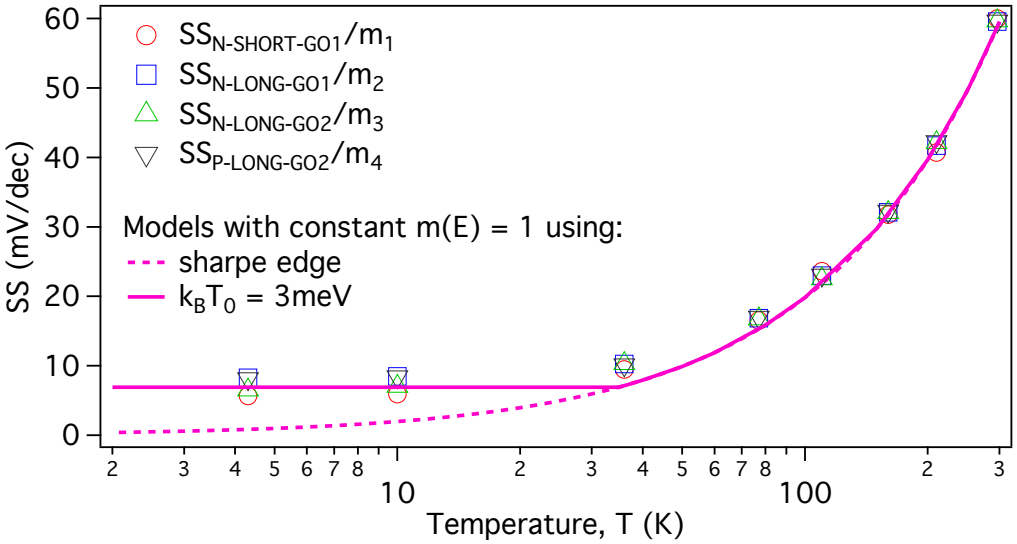


Figure 4.8: Two modelling approaches for $SS(T)$ compared to experimental data normalized by m: (i) sharp edge resulting in $(ln10\ k_BT/e)$ - dependence for $SS(T)$ and (ii) the narrow bandtailing with $k_BT_0 = 3$ meV at the conduction/valence band edges giving the saturation of SS for $T < T_0 = 35K$. Note that in these models we do not consider the D_{IT}-contribution to m $(m = 1)$.

4.4 Second approach to model $SS(T)$: disorder-induced tail below band edges and $m = m(E)$

In our previous approach, we could reproduce both the saturation of $SS(T)$ and V_{TH} at low temperatures. However, the gate dependence of $SS - I_{DS}$ in the subthreshold regime (the effect of 'curving-up' at low temperatures) was not captured by such simplified model. Inspired by the exponentially decreasing profiles of D_{IT} shown in Fig.4.4 (a), we have included an energy dependence into the m parameter in the following way:

$$V_{GS} = m\Psi_S + n(\Psi_S)e/C_{OX} \ , \ m = m_{max}e^{(E_c-E)/E_{m-ext}} \tag{4.5}$$

In Fig.4.9 (a) a rather sligth increase of m up to 1.2 with an exponential tail is shown. It already drastically affects the subthreshold current for both cases with the sharp edge and $k_BT_0 = 3$ meV as shown in Fig.4.9 (b).

Two important conclusions can be drawn: (i) for the case of $k_BT_0 = 3$ meV, only a 20% variation in m already gives the effect of the curving-up in $SS - I_{DS}$ and (ii) including $m = m(E)$ for the sharp model leads to unreasonably high threshold voltages (the saturation of $V_{TH}(T)$ was demonstrated in Chapter 3) and a weaker tailing in $SS - I_{DS}$.

To understand the role of the energy extension and the magnitude in $m = m(E)$ (see 4.5), we modeled several configurations with different E_{m-ext} and m_{max} values. First, for a given $E_{m-ext} = 20$ meV we calculated $SS - I_{DS}$ for different m_{max} values as shown in Fig.4.9(c). Then, for $m_{max} = 1.2$ by varying E_{m-ext} from 0 to 20 meV, the analysis of $SS - I_{DS}$ was performed (see Fig.4.9(d)). From these results, we conclude that both parameters can highly affect $SS - I_{DS}$ dependencies at a low temperature.

The results of energy-dependent m with $m_{max} = 1.2$ and $E_{m-ext} = 20$ meV for the cases of sharp edge and $k_BT_0 = 3$ meV for temperatures between 300 K and 2 K are given in Fig.4.10. For the sharp edge model (Fig.4.10 (a)) with $m = m(E)$, we observe that V_{TH} does not saturate at low T as it was the case for $m = 1$ in Fig.4.7 (b). Regarding the $SS - I_{DS}$-behavior in Fig.4.10 (b), a saturation of SS occurs when the Fermi level, shifted to the edge of the conduction band, intersects the tail in $m(E)$ for temperature between 100 and 20 K. However, when the temperature is further lowered below $T < 20$ K, SS rapidly decreases. This effect is due to the decaying exponential dependence we have taken for $m = m(E)$.

For the case of $k_BT_0 = 3$ meV, $I_{DS} - V_{GS}$ and $SS - I_{DS}$ down to 2 K are shown in Fig.4.10 (c-d). Besides the saturation of SS extracted in the

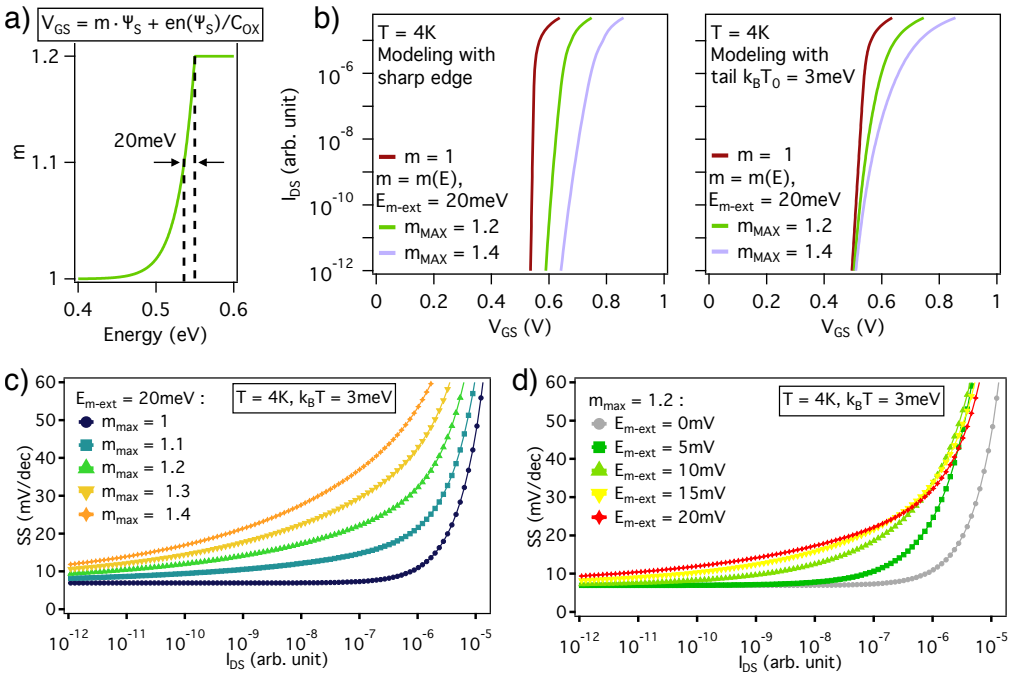


Figure 4.9: (a) Exponential decrease of $m = m(E)$ from the conductance band edge in the form of $m = m_{max}e^{(E_c-E)/E_{m-ext}}$ with $m_{max} = 1.2$ and $E_{m-ext} = 20$ meV. (b) The effect of $m(E)$ with $m_{max} = 1,\ 1.2,\ 1.4$ on the subthreshold current calculated at 10 K. (c) $SS - I_{DS}$ for different m_{max} and $E_{m-ext} = 20$ meV. (d) $SS - I_{DS}$ for different E_{m-ext} and $m_{max} = 1.2$.

weak inversion regime, we observe the curving-up (strong V_{GS} - dependence) of $SS - I_{DS}$ experimentally reported in Fig.4.1. It is worth mentioning that from the D_{IT} profiles shown in Fig.4.4 (a) we observe that the energy tailing from the band edge is rather narrower for NMOS compared to PMOS transistors. Another observation is that $m_{max} = 1.2$ and $E_{m-ext} = 20$ meV at below 30 K lead to slightly increased SS: $SS(30\text{ K}) = 9.8$ mV/dec and $SS(2\text{ K}) = 10.5$ mV/dec. We will see later that a correct calibration of m_{max} and E_{m-ext} allows us to accurately reproduce the experimental profile of $SS - I_{DS}$.

The modelling approaches with and without $m = m(E)$ are compared in Fig.4.11 (a). We already provided the arguments why the sharp edge with $m = m(E)$ cannot be used to explain the subthreshold swing at low temperature. Then, by using a tail in the DoS with $k_BT_0 = 3$ meV and considering $m = 1$ and $m = m(E)$ (data extracted at 10 pA from Fig.4.10 (d)) we conclude that both theories capture the saturation of $SS(T)$ ex-

perimentally observed. Less abrupt transition below $T < T_0 = 35$ K seen in experimental data can be reproduced by adjusting the magnitude or the energy tailing in $m = m(E)$ and T_0.

To validate the improved model with $m = m(E)$ presented in this section, a quantitive comparison between experiment and simulations is shown in Fig.4.11 (a) for NMOS GO2 long device. For the modeling with $k_BT_0 = 3$ meV, we accounted for $m > 1$ at room temperature (1.15 for this transistor) and introduced $m = m(E)$ with $m_{max} = 1.35$ and $E_{m-ext} = 10$ meV. The simulation curve was shifted to the lower gate voltages to match the real threshold voltage defined by the TiN metal gate (typical TiN work function is $0.43 - 0.465$ eV depending on the process pa-

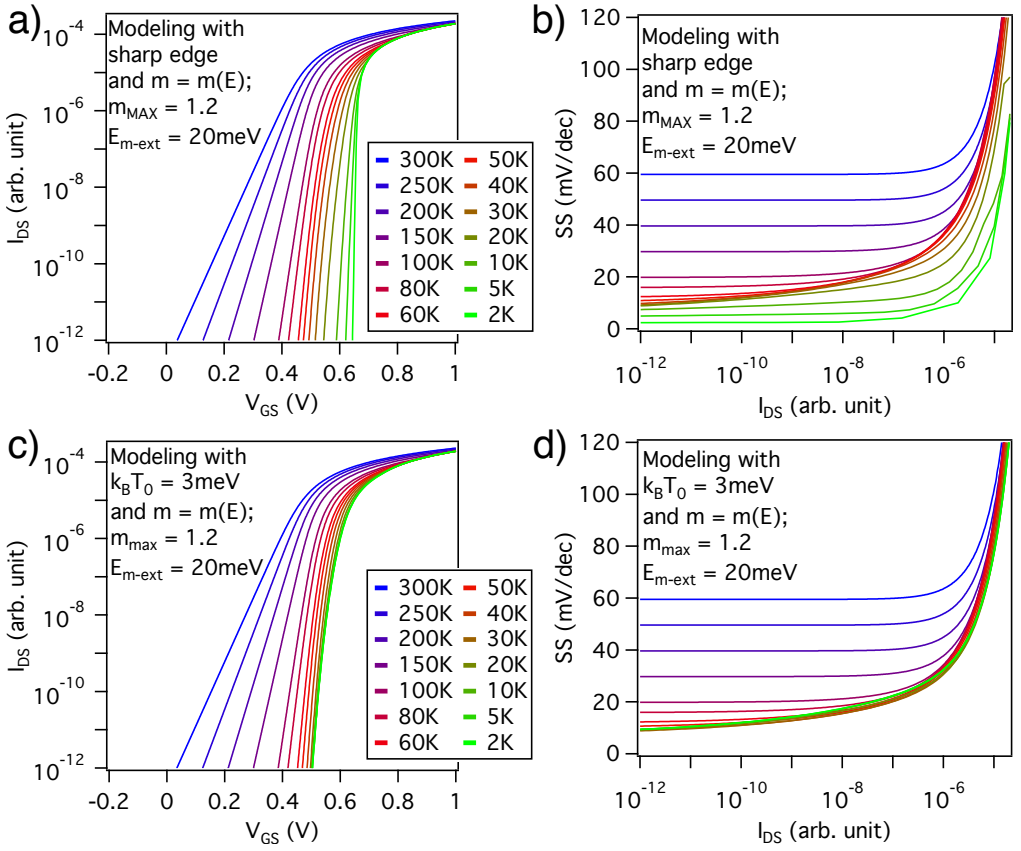


Figure 4.10: The effect of $m = m(E)$ with $m_{max} = 1.2$, $E_{m-ext} = 20$ meV extension for the cases of sharp edge (a-b) and $k_BT_0 = 3$ meV (c-d). For data in (a-b) we do not observe the saturation of V_{TH} and SS whereas the modelling with $m = m(E)$ and $k_BT_0 = 3$ meV shown in (c-d), reproduces the gate voltage dependence of $SS - I_{DS}$ observed in experiment.

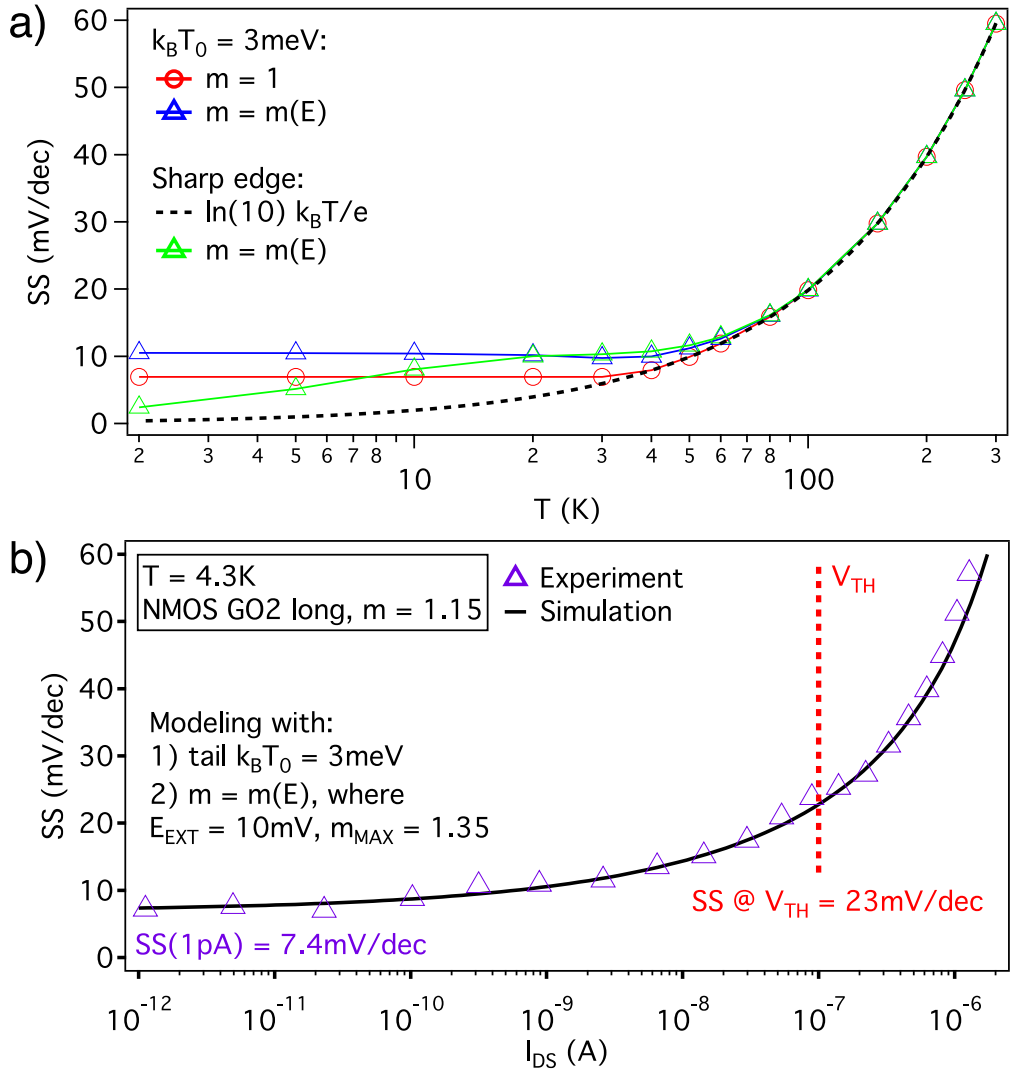


Figure 4.11: (a) $SS(T)$ calculation with different approaches of modeling : sharp edge and $k_BT_0 = 3$ meV - cases with a constant and energy-dependent $m(E)$ with $m_{max} = 1.2$ and $E_{m-ext} = 20$ meV. (b) Quantitive comparison between the simulation with $k_BT_0 = 3$ meV and $m = m(E)$ with $m_{max} = 1.35$ and $E_{m-ext} = 10$ meV at 4.3 K. Note that the experimental $SS - I_{DS}$ is not normalized. $m = 1.15$ is deduced from the room temperature characteristic is used.

rameters [165]). An excellent agreement with experimental data was found up to V_{TH} @ $I_{DS} = 0.1$ μA. It should be noted, that for the first time, we present a model which captures the 'curving-up' in $SS - I_{DS}$ at cryogenic

temperatures. At 4.3 K we obtain $SS(1\text{ pA}) = 7.3$, $SS(1\text{ nA}) = 10.9$, $SS(0.1\ \mu\text{A}) = 23$, and $SS(1\ \mu\text{A}) = 51.2$ mV/dec. Therefore, for realistic cryogenic compact modeling, such strong V_{GS} - dependence must obviously be taken into account. For $I_{DS} > 0.6\ \mu$A, the simulation starts to deviate from experiment due to the drift component of current which is neglected in our modeling.

Finally, the main outcomes of this section are : (i) the density of states with a sharp edge at the conduction band edge cannot adequately describe the experimentally observed saturation of $SS(T)$ and V_{TH} neither with constant m nor with $m = m(E)$. (ii) Introducing a narrow tail in the density of states of 3 meV close to the band edges captures both the saturation of $SS(T)$ and V_{TH}. (iii) the tailing observed in $SS - I_{DS}$ characteristics can be modelled by introducing a energy-dependent $m(E)$ with the magnitude changing by typically 20% ($m_{max} = 1.2$) at the band edges and exponentially decaying away from the band edges with a typical characteristic width of $E_{m-ext} = 10 - 20$ meV.

4.5 Cryogenic behavior of SS under body-biasing

At low temperature, due to the shift of threshold voltages, forward body-biasing is needed to recover $V_{TH}(300\text{ K})$ and then to improve the performance of MOSFETs. In the case of 28 nm FD-SOI transistors, we have already shown in Chapter 3 that the slope of subthreshold current is rather weakly dependent on body-biasing (at least for the top-gate operation). $SS - I_{DS}$ curves for GO2 NMOS and PMOS transistors with $L_G = 150$ nm are shown in Fig.4.12 (a) and (b) for different FBB. For NMOS, $SS - I_{DS}$ does not change up to $V_{BACK} = 3$ V indicating more uniformly distributed disorder. A slightly higher tailing in $SS - I_{DS}$ for FBB up to $V_{BACK} = -5$ V for PMOS is observed. This difference might be explained by different disorder for PMOS with lower energy extension of $m = m(E)$ for the back interface (note that the minimum value does not change). Thus, our analysis of SS vs V_{BACK} shows that the variation of interface trap density between the top and back interfaces [135] cannot be used to explain the saturation of SS.

Finally, using the dynamical threshold MOSFET (DTMOS), for which the top gate and back gates are biased at the same time, is a particularly interesting operation for achieving high performance at low supply voltages and highly reduced I_{OFF} at room temperature [166, 167]. At low tempera-

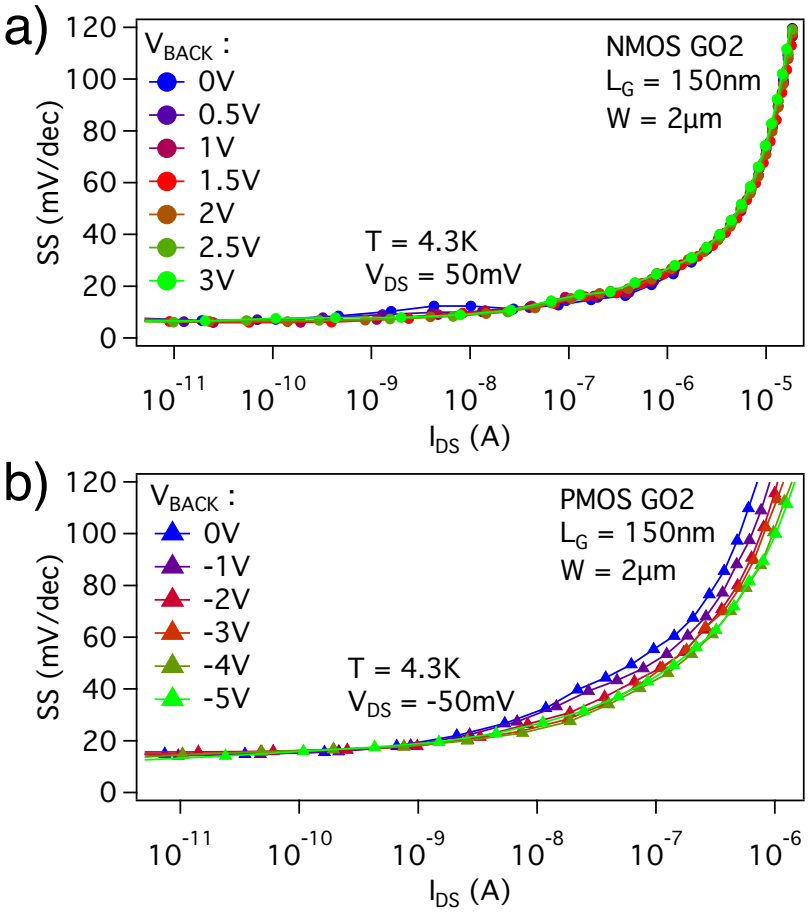


Figure 4.12: $SS - I_{DS}$-analysis under different forward body biasing conditions for (a) GO2 NMOS and (b) GO2 PMOS with $L_G = 150$ nm and $W = 2$ µm.

ture, the ability to effectively compensate the V_{TH}-shift via body-biasing is of particular importance for optimizing power-performance tradeoffs which will be discussed in details in Chapter 5. The $SS - I_{DS}$ dependence for a short-channel NMOS transistor at 4.3 K and $V_{DS} = 0.5$ V is shown in Fig.4.13. Each data point corresponds to the increase of V_{GS} by 0.5 mV and V_{BACK} by 8 mV. Such configuration was chosen to approach the ideal dual-gate mode [139] of DTMOS operation by choosing $V_{GS} = 16 \times V_{BACK}$ where 16 is the ratio between the EOT of top gate and t_{BOX}.

For the first four decades, we observed an average SS less than 3 mV/dec. Highly reduced $V_{TH-DTMOS}$ which can be estimated from Fig.4.13 is below 140 mV at $V_{DS} = 0.5$ V, whereas in the absence of body-biasing V_{TH}(4.3 K)

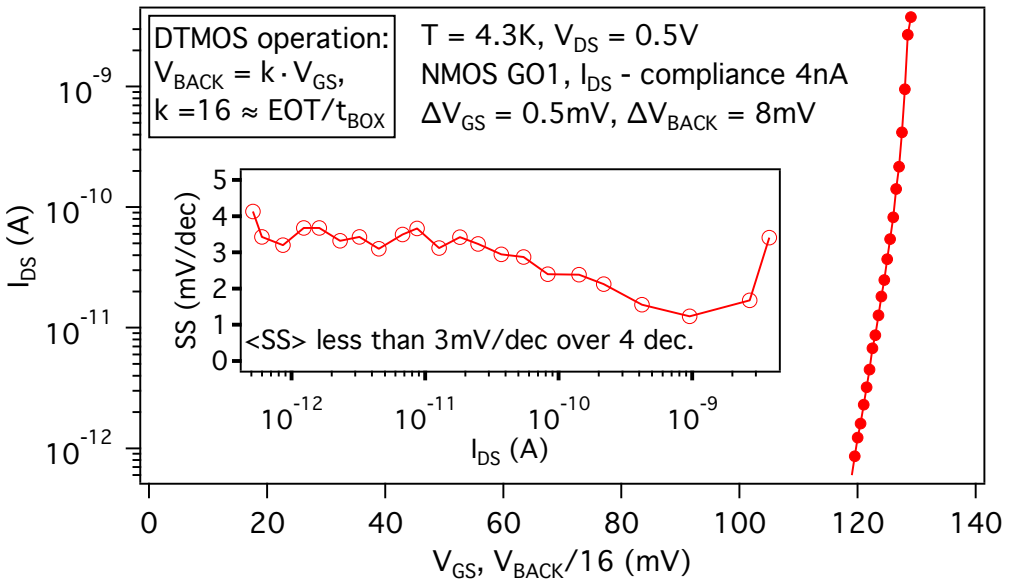


Figure 4.13: DTMOS operation of a short-channel GO1 NMOS transistor with EOT = 1.55 nm. An average SS measured over the first 4 decades is less than 3 mV/dec. The current compliance of 4 nA prevented us from measuring SS for higher currents.

= 0.4 V. Moreover, the steepness of SS of DTMOS is highly reduced compared to an average SS of 11 mV/dec for the first four decades when FBB up to +5.8 V is applied. Therefore, this outstanding sharpness of FD-SOI DTMOS transistors at 4 K is of great potential for low-power and very-high-performance cryogenic circuits. Another interest in using DTMOS lays in its excellent analog performance: very high transconductance G_M and low output conductance G_{DS} in the strong inversion regime can be achieved [168]. The improved values of G_M and G_{DS} under DTMOS operation also result in higher oscillation frequency (f_{max}) [169].

Thus, our results provide an additional knob (unavailable for standard bulk Si technologies) to boost the low-temperature performance of 28 nm FD-SOI transistors (in addition to the V_{TH}-compensation with FBB approach given in Chapter 5) for both digital and analog cryogenic circuits.

4.6 Conclusion

In this chapter, a new physical model is proposed to explain the low-temperature behavior of the subthreshold current and the saturation of

threshold voltage (discussed in Chapter 3). For the first time, the saturation of subthreshold swing is explained from room temperature down to 4 K. Our model also predicts the saturation of $SS(T)$ at deep sub-K temperatures (down to 20 mK) observed in both bulk Si and FD-SOI transistors.

By introducing The model initially developed for GO2 NMOS long-channel transistors, gives an excellent correlation with the experimental data for both NMOS and PMOS transistors of different gate lengths and gate oxide thicknesses. Therefore, despite the transistor's dimensions and type of charge carriers, the universality of our approach based on the disorder-induced tail at the band edges is emphasized.

In addition to the narrow 3 meV tail, when a very small variation (by only 20%) of the density of interface traps was included in the modeling, we were able to explain another important phenomenon of the tailing in $SS - I_{DS}$ characteristics at cryogenic temperatures. Then, the model was validated using experimental $SS - I_{DS}$ data and an excellent agreement over six decades of I_{DS} was demonstrated.

Forward body biasing analysis demonstrated that, by solely considering the effect of interface trap density at the top and bottom interfaces, the saturation of $SS(T)$ cannot be explained.

By performing dynamic threshold MOSFET characterization of a short-channel NMOS, we found an average SS(4 K) below 3 mV/dec over four decades of I_{DS}. Then, the importance of such outstanding transistors sharpness for both digital and analog applications was discussed.

Finally, our analysis allowed a direct determination of the technology-dependent band-tail extension and an energy-dependent $m = m(E)$ which could form a crucial element in future compact modeling and design of cryogenic circuits.

Chapter 5

Cryogenic Performance of 28 nm FD-SOI Ring Oscillators

In this chapter, the performance of Ring Oscillators (ROs) is characterized from room temperature down to 4.3 K for different gate lengths 28, 34 and 46 nm. The speed of RO is evaluated in terms of delay per stage while keeping the same threshold voltages within the $296 - 4.3$ K temperature range. The relative gain in terms of RO's speed-up is correlated with the effective current calculated from isolated NMOS and PMOS transistors and thus, the low-temperature behavior of load capacitance is addressed. The extended body-biasing window at 4.3 K and its potential use for CryoCMOS design are discussed. Thanks to aggressive forward body-biasing (up to 6 V), we observe no minimum in Energy-Delay product as a function of supply voltage down to $V_{DD} = 0.325$ V, proving that 28nm FD-SOI technology provides a unique solution for low-supply voltage cryoelectronics. The impact of gate length on the cryogenic performance of ring oscillators is discussed. We have demonstrated that the same performance with highly reduced power dissipation can be achieved when the gate length is relaxed from 28 to 46 nm. The variability of short-channel devices at low temperature is analyzed as well as the zero-threshold-voltage mode of operation. Finally, we conclude with some reflexions on the choice of the optimal (lowest) temperature of operation for the cryoelectronics based on the 28 nm FD-SOI technology. Some of the results presented in this chapter were published in [113].

5.1 Setup used for cryogenic measurements of ring oscillators

The ring oscillator devices cleaved from a 300 mm wafer have been provided by R&D department of STMicroelectronics. They were mounted onto a printed circuit board (PCB) and wet bonded. DC polarizations were provided by state-of-the-art electronics for low-temperature measurements using the IVVI-DAC-rack designed at TU Delft [170]. Currents were measured using a transimpedance amplifier, converted to voltage and recorded using a commercial digital multimeter (Agilent 34401A). The sample holder was placed inside a vacuum tube with a small amount of exchange gas and loaded into a helium dewar. Precise temperature control for measurements between 296 K and 4.3 K was achieved thanks to a small amount of exchange gas providing long cooling-down times. Pulling the sample insert up and down in a helium dewar allowed us to fix a given temperature. The temperature of the sample was monitored with an ultra-precise temperature controller TRMC2 developed at Neel Institute [171]. Although we use only standard DC lines, we have verified that AC signals can be detected without much degradation for the frequencies of interest (up to 500 kHz). To visualize the output AC signal and to measure the frequency, a digital oscilloscope (TBS1064) was used. The Python-based data acquisition framework Qcodes [172] was used with several additional driver developments.

5.2 Principle of operation and room temperature performance of RO

To evaluate the performance of given CMOS technology, especially in terms of relative speed and power consumption, in addition to the characterization of isolated MOSFETs, basic circuits such as Ring Oscillators are often measured. An RO is a device which gives an AC signal at the output when it is polarized using only DC voltages. The circuit is composed of a chain of elementary logic gates, inverters (IV). The number of IVs is crucial: for an odd number of IV (101) attached to the enabling AND gate as in our case (see Fig.5.1 a), the signal at the output of any IV will oscillate with the period being 101 times larger than the elementary propagation delay of IV (also called delay per stage or τ_P). The principle of operation can be briefly formulated as following: given that a finite time is needed to charge the gate capacitance before the MOSFETs start to conduct, the

output of every IV provides either the logical state "0" or "1" after a finite delay [173]. Therefore, we will have an AC signal with a magnitude set by the supply voltage V_{DD}. ROs fabricated using advanced CMOS technology are characterized by a delay per stage τ_P lower than 20 ps [2]. Therefore, to be able to measure such a high frequency with conventional electronics, a chain of inverters with a frequency divider at the output are usually used (in our case having the highest frequency of about 500 kHz at the output, we could use classical low-frequency DC lines for measurements). In our devices, we have 101 invertors and a frequency divider by 1024. Considering an average equal pull-up and pull-down times of the AC signal, the delay per stage can be expressed as $\tau_P = 1/(f_{OUT} \times 2 \times 101 \times 1024)$ [2], where f_{OUT} is the measured output frequency.

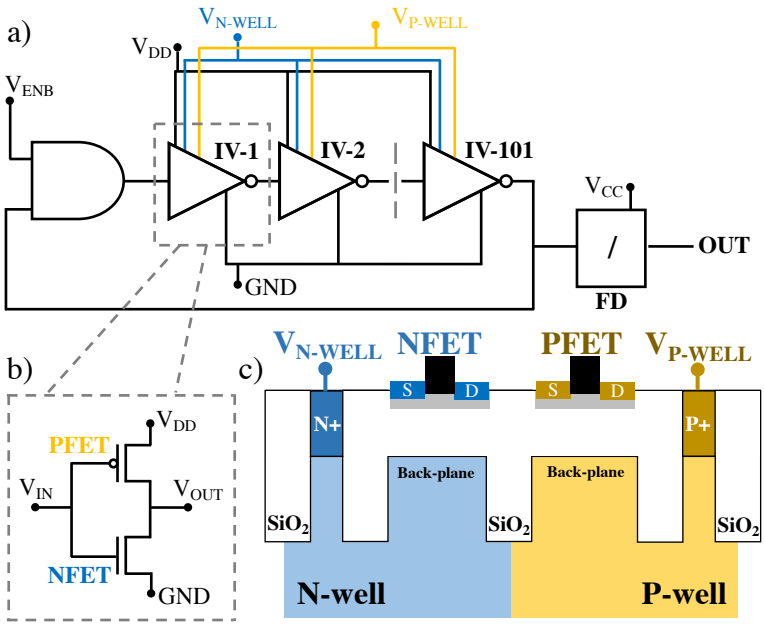
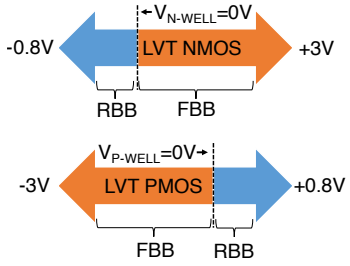


Figure 5.1: LVT Ring Oscillator characterized at low temperature. (a) Schematic layout of 101-stages ring oscillator with 1024-frequency divider (FD). The circuit starts to oscillate when ENABLE (V_{ENB}), Supply voltage (V_{DD}), and Frequency Divider (V_{CC}) are polarized. The measurement protocol is given in the table of Fig.5.2. (b) Single inverter stage composed of n- and p-MOS. V_{N-WELL} (V_{P-WELL}) attached to n-MOS (p-MOS) are not shown. (c) Illustration of LVT transistors in the flip-well configuration designed for forward body-biasing. The allowed range of body-biasing at room temperature is shown in Fig.5.2

In contrast to usual bulk technology, LVT FD-SOI architecture enables

an extended body-bias range from −0.8 V (reverse body-biasing RBB for NMOS, +0.8 V for PMOS) up to +3 V (forward body-biasing FBB for NMOS, −3 V for PMOS) as shown in Fig. 5.2 [117, 116, 115]. In order to compensate the increase of V_{TH} at low-temperature already discussed in Chapter 3, LVT transistors are used to provide a strong improvement in the switching delay thanks to FBB (a typical body factor is around $V_{TH}/V_{BACK} = 85$ mV/V at room temperature) at the cost of a higher leakage current. When no input is provided on the AND logic gate, static current I_{STAT} and then static power P_{STAT} consumption occurs due to leakage current from supply to ground. If V_{ENB} is applied, dynamic current I_{DYN} and dynamic power P_{DYN} can be analyzed.

a)



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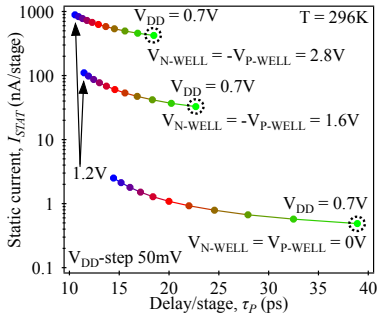


c)

Parameter	*Unit*	*Description*	*Measurement protocol*
f	Hz	RO frequency	V_{ENB}=V_{DD}, V_{CC} = 1V and measure OUT.
τ_P	ps	RO delay per stage	= 1/(f×2×101×1024).
I_{DYN}	µA/ stage	Dynamic current per stage in oscillating state	V_{ENB}=V_{DD}, V_{CC} = GND and measure OUT.
I_{STAT}	nA/ stage	Static current per stage in non-oscillating state	V_{ENB} = V_{CC} = GND and measure OUT.
P_{DYN}	µW/ stage	Dynamic power per stage in oscillating state	= I_{DYN} × V_{DD}
P_{STAT}	nW/ stage	Static power per stage in non-oscillating state	= I_{STAT} × V_{DD}
I_{EFF}	µA	Effective drive current of FD-SOI transistor	I_{EFF} = 1/(1/ $I_{EFF\text{-}N}$ + 1/ $I_{EFF\text{-}P}$) $I_{EFF\text{-}N(P)}$ = (I_H+ I_L)/2 where I_H = I_{DS} (V_{GS} = V_{DD}, V_D = V_{DD}/2) I_L = I_{DS} (V_{GS} = V_{DD}/2, V_D = V_{DD}) where V_{GS}, V_{DS}, and I_{DS} are MOSFET gate voltage, drain voltage and drain current.
$G(I_{EFF})$	%	I_{EFF} enhancement at low temperature	= [I_{EFF} (T) - I_{EFF} (296K)] / I_{EFF} (T)
$G(\tau_P)$	%	τ_P enhancement at low temperature	= [τ_P (T) - τ_P (296K)] / τ_P (T)
EPT	fJ	Energy per transition	=101 × τ_P × (I_{DYN} - I_{STAT}) ×V_{DD}
EDP	fJ×ps	Energy Delay product	= τ_P × EPT

Figure 5.2: (a) Body-biasing limitations at room temperature (b) Static current vs delay per stage for a set of V_{DD} from 0.7 to 1.2 V ($\delta V_{DD} = 50$ mV). Three different FBB voltages are considered. I_{STAT} is significantly increased at high V_{FBB} illustrating that ROs are well optimized at room temperature with $V_{FBB} = 0$ V. (c) Definitions of the RO parameters used in this work and their measurement protocol.

Throughout this chapter, we will use RO delay, static and dynamic currents (power) normalized by the number of inverters as it is commonly done

to benchmark different technologies [2]. Other important parameters used in this work to evaluate the low-temperature performance of ring oscillators are Energy Per Transition (EPT) and Energy-Delay product which will be discussed later. For the details on measurement procedures of τ_P, I_{DYN}, and I_{STAT} and other parameters see the table in Fig. 5.2.

In Fig.5.2, we show I_{STAT} as a function of τ_P measured at room temperature for different V_{DD} ranging from 0.7 V to 1.2 V. As supply voltage is increased, we observe the RO speeding up due to higher overdrive current and lower threshold voltages of MOSFETs. For instance, in the case of $V_{FBB} = 2.8$ V, τ_P is reduced by 33% at $V_{DD} = 1$ V. We characterized the RO under three symmetric FBB conditions: $V_{N-WELL} = -V_{P-WELL} = 0, 1.6, 2.8$ V. Under forward body biasing, static current is increased mainly due to non-negligible leakage currents at $V_{GS} = 0$ V because of reduced threshold voltages. Thus, we can conclude that even though the LVT architecture is designed for high-performance applications, static power dissipation may become a limiting factor at room temperature if an aggressive forward body-biasing is applied.

5.3 Existing solutions for the optimization of cryogenic performance using standard silicon technologies

For a long time, standard [174, 121, 123] and specially designed [175] CMOS ring oscillators fabricated in bulk Si have been characterised at low temperature for high-performance cryogenic circuits. Despite an improvement in switching time (typically few ns per stage) obtained in μm-technologies at low temperature down to $4-10$ K [175, 123] and a possibility to reduce supply voltage, these circuits operated at typically $V_{DD} = 5-15$ V [174]. Hence, it might be problematic to use the μm-technologies for low power and high-performance CryoCMOS applications. Indeed, typical requirements for the use of cryoelectronics for large qubit arrays [176] are: much less than 2 mW/qubit power dissipation, deep sub-μm technology for scalability, noise budget less than 0.1 nV Hz$^{-1.2}$, bandwidth for frequency multiplexing $1 - 12$ GHz and avoidance of non-ideal kink behaviour and hysteresis in the MOSFET's characteristics as observed in bulk Si [121].

It has been believed for a long time that standard CMOS technologies are not suitable for low-temperature circuits due to the above-mentioned non-idealities. This is why hybrid technologies were extensively characterized at low temperature for high-performance applications. For the gen-

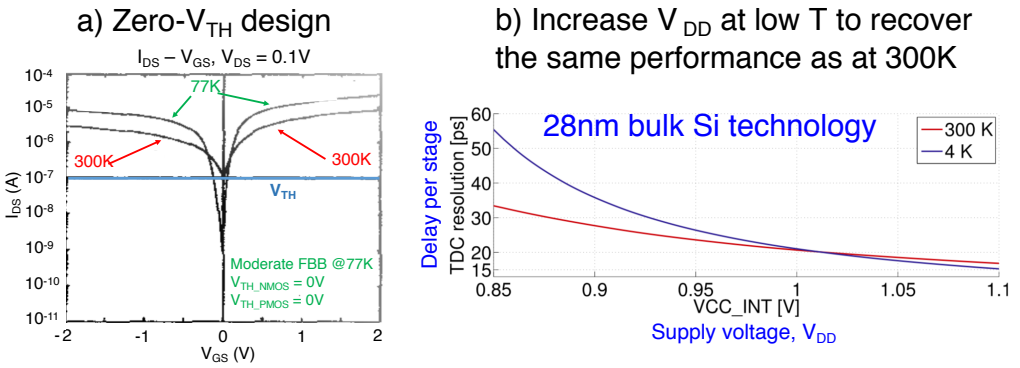


Figure 5.3: Two common strategies for optimization of low temperature performance if wide-range body-biasing is not available (as in case of bulk Si technologies): (a) To design NMOS and PMOS transistors with V_{TH} close to zero at low temperature by adjusting the channel doping, adapted from [175]; (b) To increase V_{DD} (VCC_INT) at low temperature in order to have higher driving currents and thus to obtain the room temperature performance. Note that at 4 K, the relative speed of FPGA (fabricated in standard 28 nm bulk Si) plotted in this graph is increased by 260% when V_{DD} is lowered only from 1 V to 0.85 V, adapted from [147]. The TDC resolution stands for the delay of a single carry element of FPGA which is equivalent to the inverter's delay per stage.

eral references see [121, 123] and for more recent results, see the cryogenic performance of a ring oscillator fabricated in silicon-germanium (SiGe) hetero-junction bipolar transistor (HBT) technology with τ_P of only 2.3 ps at 25 K [177]. More recently, the cryogenic characterization of advanced CMOS technologies (28, 40, 160 nm technology nodes [136, 149, 178]) was performed in view of the arising need of CryoElectronics for qubits, and also other applications such as low temperature sensors, low power neuromorphic computing (to replace superconducting circuits [179]), and extreme environment electronics (Aerospace, Space Exploration, etc.). The general drawback of the above-mentioned bulk Si technologies regarding low-temperature operation is the inability to reduce the supply voltage to optimize the power-performance. For these technologies there is no means to compensate the low temperature V_{TH}-shift and then the supply voltage must be increased [136] which is not consistent with the low-power consumption requirement.

Typical strategies for optimization of cryogenic RO performance are the already-discussed increase of V_{DD} as used in [147] (see Fig.5.3(b)) or

a special design of MOSFETs accounting for the low-T shift of threshold voltages and thus resulting in close-to-zero V_{TH} operation as demonstrated in [175] (see Fig.5.3(a)).

In addition to standard bulk Si devices, low-temperature characterization of 45 nm partially-depleted silicon-on-insulator (PD-SOI) RO has revealed promising results at a temperature as low as 2.8 K. As compared to 300 K, a decrease of τ_P by 15% and a static power reduction by 15 times were achieved [180]. However, the low-temperature body-biasing was not addressed probably due to its low efficiency in PD-SOI.

Finally, the co-integration of ring oscillators fabricated using Leti's FD-SOI Trigate technology (with MOSFETs of $L_G = 60$ nm, $W = 1000$ nm) and the single-electron transistors featuring Coulomb blockade at low temperature ($L_G = 40$ nm, $W = 25$ nm) was recently demonstrated marking an important step toward hybrid Quantum-CMOS circuits [181]. It is worth mentioning that a similar device was used for the recent demonstration of the first CMOS hole spin qubit [26, 182]. Regarding the RO performance at 4 K reported in [181], the body-biasing capability for the $V_{TH-PMOS}$ compensation was demonstrated at 4 K resulting in a +14% increase of the output frequency at $V_{BACK} = -8$ V (RBB for NMOS and FBB for PMOS) comparing to the case of zero body-biasing. However, having a 145 nm-thick BOX and the unique body-biasing for both N- and PMOS, an efficient performance-power optimization couldn't be performed.

To sum up, in this chapter, we will show that commercially available planar 28 nm FD-SOI technology with addressable body-biasing to NMOS and PMOS (FBB can be applied for both separately) and much thinner BOX of 25 nm provides significant opportunities toward optimizing highly-efficient and ultra-low-power cryogenic circuits for large-scale quantum computing.

5.4 RO performance at low temperature without V_{TH} compensation

Operation of FD-SOI transistors at cryogenic temperature was already reported in [114, 183, 112]. Since the scattering of charge carriers with phonons is sufficiently weak and can be neglected at liquid helium temperature, electron and hole mobilities are strongly enhanced and should lead to a smaller τ_P at low temperature for a given V_{DD}. Mobility enhancement of short-channel NMOS and PMOS transistors at low temperature will be quantitatively addressed in the section 'Boosting the RO performance with relaxed L_G'.

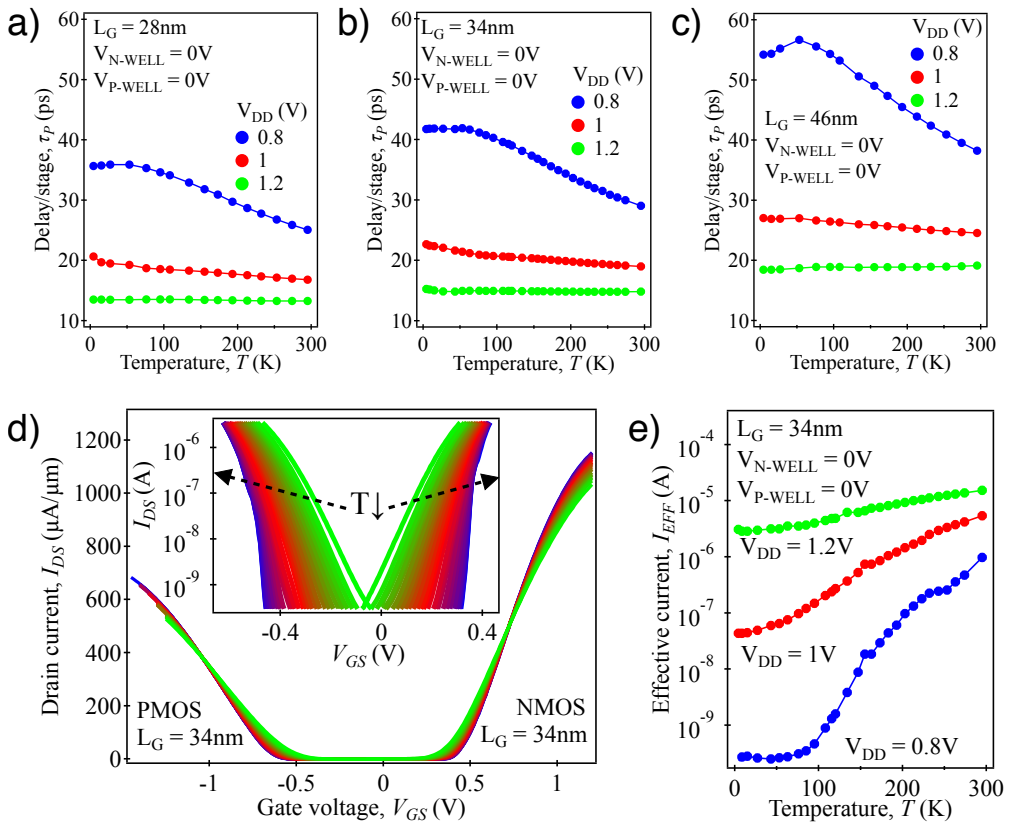


Figure 5.4: (a) - (c) Ring oscillator performance in terms of τ_P from 296 down to 4.3 K with $V_{N-WELL} = V_{P-WELL} = 0$ V for $L_G = 28, 34$, and 46 nm ($W_{NMOS} = 420$ nm and $W_{PMOS} = 600$ nm). All the ROs slow down due to the increase of V_{TH} at low temperature for $V_{DD} = 0.8$ V and $V_{DD} = 1$ V. (d) Transfer characteristics $I_{DS}-V_{GS}$ at $V_{DS} = 1$ V recorded every 5−15 K from 296 K to 4.3 K illustrating the effect of V_{TH}-shift at low temperature. Inset shows the subthreshold behaviour with subthreshold swing greatly reduced at low temperature. The dimensions of LVT GO1 NMOS and PMOS are $L_G = 34$ nm, $W_{NMOS} = 210$ nm, and $W_{PMOS} = 300$ nm. (e) The decrease of effective current (inversely proportional to the inverter delay) extracted from (d) explains the increase of τ_P observed in (a - c).

However, despite a significant increase of drive current expected at low temperature [112], the ROs of different $L_G = 28, 34, 46$ nm slow down as it can be seen in Fig.5.4 (a)-(c). This effect is especially pronounced for longer L_G (having higher V_{TH}) and when V_{DD} is reduced. This increase of delay per stage is explained by the V_{TH}-shift at low temperature for both N- and

PMOS transistors as shown for the case of $L_G = 34$ nm in Fig.5.4(d). As the ON-currents at $V_{GS} = V_{DS} = V_{DD}$ are smaller for longer L_G because of higher V_{TH}, it explains why the delay-degradation at low temperature is more important for $L_G = 46$ nm (see Fig.5.4(c)) than for devices with shorter L_G as shown in Fig.5.4 (a - b). Note that when the supply voltage was set to $V_{DD} = 1.2$ V for all gate lengths, τ_P remained unchanged within the whole $296 - 4$ K window. This can be explained by higher driving currents in the strong inversion regime at $|V_{GS}| = 1.2$ V (see Fig.5.4(d)) making the ROs less sensitive to the V_{TH}-shift.

Apart from directly measuring the RO delays, another common practice in CMOS modeling is to predict the single inverter delay by measuring the following currents: first from N-, PMOS transfer/output characteristics $I_{EFF-N(P)} = (I_H + I_L)/2$ where $I_H = I_{DS}(V_{GS} = V_{DD}, V_{DS} = V_{DD}/2)$ and $I_L = I_{DS}(V_{GS} = V_{DD}/2, V_{DS} = V_{DD})$ are measured.Then the effective current of a single inverter can be calculated as $I_{EFF} = 1/(1/I_{EFF-N} + 1/I_{EFF-P})$ as specified in the table of Fig.5.2. Then, the delay of an inverter modeled with one NMOS and PMOS transistor can be linked to I_{EFF} using the load capacitance C_{LOAD} including the inversion capacitance, the parasitic capacitances and the wiring capacitance of back-end-of-line as $\tau_P = C_{LOAD} \times V_{DD}/I_{EFF}$ [2]. This so-called two-point model for I_{EFF} used for the inverter delay modeling has been proven to be very efficient for deep sub-μ technologies [2, 184].

Finally, we should mention that to link τ_P measured from ring oscillators to I_{EFF} of isolated N-, and PMOS transistors, the same physical dimensions must be taken. In our case of $L_G = 34$ nm shown here, the width of NMOS and PMOS are twice smaller for isolated transistors used to estimate I_{EFF}. To be able to link the RO to the isolated transistors we have first verified that the V_{TH}-shift and I_{ODSAT}/W (at $|V_{GS}| = |V_{TH}| + 0.5V$ and $V_{DS} = V_{DD}$) remained almost unchanged for W between 80 and 1000 nm for temperatures down to 4.3 K (see Chapter 3). This is why we could directly relate the decrease of I_{EFF} shown in Fig.5.4(e) to the variation in τ_P (Fig.5.4(b)) as done in a quantitative analysis in the next section.

Finally, we conclude that without forward-body-biasing used to compensate the V_{TH}-shift, it seems to be unlikely to achieve an optimized cryogenic digital control electronics combining high-performance and low-power consumption.

5.5 Forward body-biasing compensation of the V_{TH}-shift down to 4.3 K

In order to preserve the benefit of higher carrier mobility and hence, higher driving current at low temperatures, the V_{TH}-shift must be compensated. The ability to adjust V_{TH} through body-biasing was successfully demonstrated down to 4.3 K using 28nm FD-SOI transistors [112]. Moreover, we already discussed the forward and reverse body-biasing efficiency for long- as well as for short-channel transistors in Chapter 3. Here, the measurements were done in three steps.

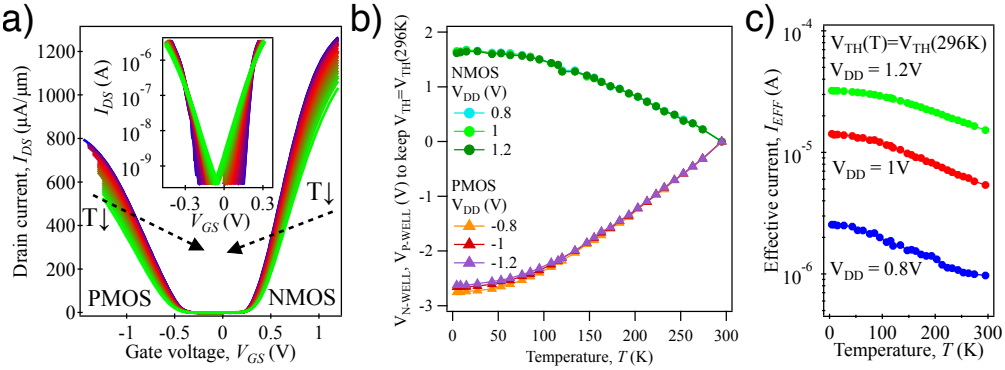
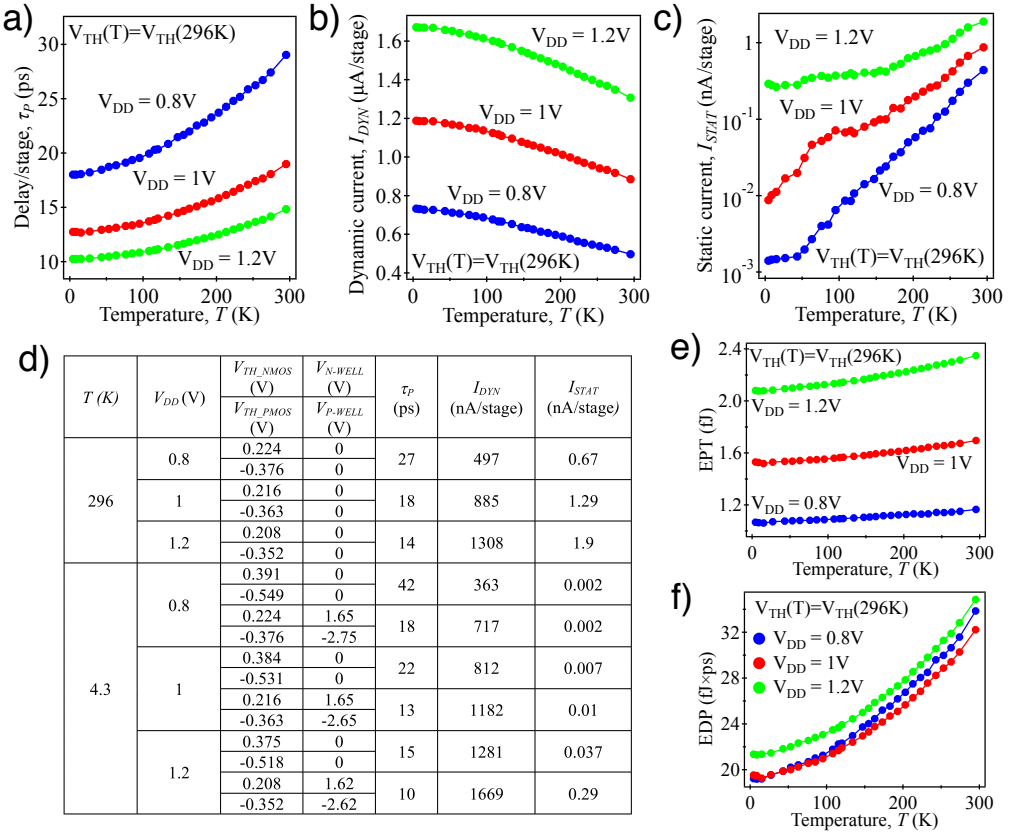


Figure 5.5: The V_{TH} compensation performed on LVT GO1 transistors with $L_G = 34$ nm, $W_{NMOS} = 210$ nm, and $W_{PMOS} = 300$ nm. (a) Transfer characteristics from room temperature down to 4.3 K. Note that the threshold voltages are kept constant through FBB within the whole temperature range as can be seen in the inset. (b) V_{N-WELL} and V_{P-WELL} applied at each temperature to keep V_{TH} constant for different supply voltages. (c) I_{EFF} for $V_{DD} = 0.8,\ 1,\ 1.2$ V corresponding to the case of constant V_{TH} shown in (a). The effective current increases as the temperature is reduced leading to a shorter τ_P.

First, isolated transistors of the same dimensions as the ring oscillator were measured down to 4.3 K with V_{FBB} varying from 0 to $-3(+3)$ V for PMOS (NMOS). Then, the body factor was deduced at each temperature. It turned out to be almost independent on temperature down to 4.3 K. Afterward, once again we measured the same transistors by applying V_{N-WELL} and V_{P-WELL} to keep constant the $V_{TH-NMOS}$ and $V_{TH-PMOS}$ (see Fig.5.5(a-b)). Threshold voltages were calculated using the constant current method [2]. In the case of 28 nm FD-SOI, we define $V_{TH-NMOS}$ as V_{GS} @ $I_{DS} = 0.1\mu A \times W_{NMOS}/L_G$ and $V_{TH-PMOS}$ as

V_{GS} @ $I_{DS} = 0.02\mu A \times W_{PMOS}/L_G$ as explained in Chapter 3. The threshold voltages and V_{FBB} applied for the compensation at 4.3 K are given in Fig.5.6 (d).



T (K)	V_{DD} (V)	V_{TH_NMOS} (V) / V_{TH_PMOS} (V)	$V_{N\text{-}WELL}$ (V) / $V_{P\text{-}WELL}$ (V)	τ_P (ps)	I_{DYN} (nA/stage)	I_{STAT} (nA/stage)
296	0.8	0.224	0	27	497	0.67
		-0.376	0			
	1	0.216	0	18	885	1.29
		-0.363	0			
	1.2	0.208	0	14	1308	1.9
		-0.352	0			
4.3	0.8	0.391	0	42	363	0.002
		-0.549	0			
		0.224	1.65	18	717	0.002
		-0.376	-2.75			
	1	0.384	0	22	812	0.007
		-0.531	0			
		0.216	1.65	13	1182	0.01
		-0.363	-2.65			
	1.2	0.375	0	15	1281	0.037
		-0.518	0			
		0.208	1.62	10	1669	0.29
		-0.352	-2.62			

Figure 5.6: FBB compensation of the ring oscillator down to 4.3 K with L_G = 34 nm. (a) - (c) τ_P, dynamic and static currents as a function of temperature for the case of $V_{TH}(T) = V_{TH}(296K)$. (d) Table comparing room temperature and 4.3 K performance with and without compensation including τ_P, I_{DYN}, I_{STAT}, threshold voltages, and V_{N-WELL} and V_{P-WELL} needed for the 4.3 K compensation. (e) Energy per transition $EPT = 101 \times \tau_P \times (I_{DYN} - I_{STAT}) \times V_{DD}$ decreasing at low temperature due to the τ_P-reduction (f) Energy-Delay product $EDP = \tau_P \times EPT$ showing that V_{DD} = 0.8 V is more optimal than V_{DD} = 1 V at low temperature.

Finally, as it can be easily guessed from Fig.5.5(a), the effective currents for different V_{DD} were found to be significantly improved due to highly increased carrier mobility at low temperature. For instance, a relative gain in I_{EFF} of approximatively 62% was achieved for V_{DD} = 0.8 V.

In contrast to the previous results without FBB, a significant speedup for different V_{DD} is observed when threshold voltages were settled to $V_{TH}(T) = V_{TH}(296K)$ within the full temperature range (Fig.5.6 (a)). Indeed, by reducing the temperature from 296 K down to 4.3 K, the delay per stage is decreased by 38% at V_{DD} = 0.8 V, 33% at V_{DD} = 1 V, and 31% at V_{DD} = 1.2 V. The τ_P-reduction is explained by the increase of I_{EFF} shown in Fig.5.5 (c). Obviously, dynamic currents are also increased at low temperature (Fig.5.6 (b)). Furthermore, as compared to room temperature, greatly reduced static currents resulted in static power ($P_{STAT} = I_{STAT} \times V_{DD}$) decreased by a factor of 1600 (V_{DD} = 0.8 V), 100 (V_{DD} = 1 V), and 6.5 (V_{DD} = 1.2 V) at 4.3 K. This demonstrates the uniqueness of the FD-SOI technology in achieving ultra-low power dissipation at cryogenic temperatures.

The Energy Per Transition (EPT), also called Power-Delay metric, is commonly used to compare different technologies [2]. It is proportional to the active power dissipation during the RO switching and the delay per stage $EPT = 101 \times \tau_P \times (P_{DYN} - P_{STAT})$. Smaller EPT values are desirable to have either lower active (switching) power dissipation $P_{DYN} - P_{STAT}$ or shorter time to propagate a signal when carrying out a logic operation. In Fig.5.5 (e) a decrease of EPT for all supply voltages is observed proving that despite the P_{DYN}-increase (Fig.5.5(b)), the RO becomes more efficient in terms of power-performance tradeoff. However, EPT-metric has a major drawback: it does not differentiate between changes in switching power ($P_{DYN} - P_{STAT}$) and τ_P. To perform a more accurate power-performance evaluation, the Energy-Delay metric can be used [2]. The Energy-Delay product (EDP) is written as $EPT \times \tau_P$. It is well known that for a given technology, a transistor should work at the minimum energy point (MEP) in terms of V_{DD}, thus allowing a logic circuit to spend the lowest energy per operation for a given switching delay [185, 186]. MEP gives an optimal V_{DD} for a given technology and can be obtained by minimizing EDP. For instance, for the 28 nm FD-SOI technology, the optimal V_{DD} at room temperature is close to 1 V as shown in Fig.5.6(f). However, at 4.3 K, an optimal operation point is obtained for V_{DD} = 0.8 V thanks to the delay reduction via FBB. Having observed this reduction of V_{DD} at 4.3 K, we will study in the next section different aggressive forward body-biasing configurations to further optimize the cryogenic operation of RO.

Generally, to reduce RO delay and reach minimum power consumption, the desirable properties of NMOS and PMOS transistors are: high driving current (I_{DS} at $V_{GS} = V_{DS} = V_{DD}$), low leakage currents (I_{OFF} at V_{GS} = 0 V and $V_{DS} = V_{DD}$), low intrinsic capacitances (C_{INV}, C_{IT}, C_{DEP}, etc.), and low parasitic resistances and capacitances mainly related

to the interconnections and back-end-of-line. In the case of 28 nm FD-SOI technology, C_{INV} in the strong inversion regime, where ROs are operated, was already reported to be unchanged down to 4.3 K [112]. Consideration of C_{DEP} can be neglected because of the fully-depleted channel. From the SS-analysis presented in the previous chapter, we could conclude that C_{DIT} also does not play a crucial role at low temperatures. Moreover, regarding the low-κ Cu metal lines used in interconnections, it is worth mentioning that recent cryogenic studies of low-κ materials revealed their temperature insensitivity (no significant increase in capacitance and effective series resistance) down to 4.3 K [147].

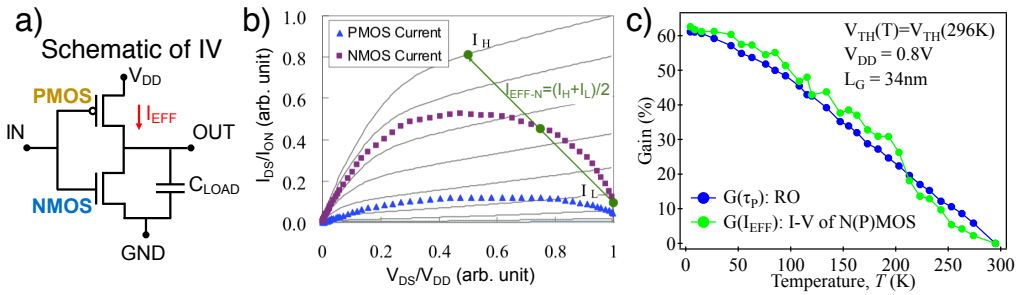


Figure 5.7: (a) Schematic of a single inverter modeling with I_{EFF} and C_{LOAD} used to calculate the delay $\tau_P = C_{LOAD} \times V_{DD}/I_{EFF}$. (b) Example of well-designed pair of NMOS and PMOS for which $I_{EFF-N} \gg I_{EFF-P}$, adapted from [187]. (c) Relative enhancement of I_{EFF} and τ_P at $V_{DD} = 0.8$ V for temperatures between 296 and 4.3 K. FBB is applied to compensate the increase of V_{TH} at low temperatures. Note that both relative gains are well correlated within the whole temperature range.

In Fig.5.7(a) the modeling of a single inverter is illustrated with a unique C_{LOAD} accounting for all the capacitances discussed above. Taking into account the cryogenic behavior of intrinsic and parasitic capacitances discussed above, one would suppose that cryogenic variation of τ_P can be mainly explained by I_{EFF}. A typical estimation of effective current using $I_{DS} - V_{DS}$ curves for a well-designed inverter is shown in Fig.5.7(b). It is interesting to note that in such case I_{EFF-N} should be higher than I_{EFF-P} which will lead to symmetric $V_{IN} - V_{OUT}$ voltage characteristic and thus in almost the same pull-up and pull-down times of the AC signal from the Ring Oscillator [2]. Finally, a good correlation between the relative gains in τ_P measured from RO and I_{EFF} deduced from isolated MOSFETs assuming temperature-independent C_{LOAD} are shown in Fig.5.7(c). This correlation supports the above-mentioned assumptions about C_{LOAD} being very weakly

dependent on temperature down to 4.3 K. The possibility to directly link I_{EFF} to τ_P without taking into account the complex dependences of capacitances at low temperature is of great importance for CryoCMOS designers.

5.6 Maximal performance and body-biasing limitations at 4.3 K

We already demonstrated the body-biasing efficiency within $-6...+6$ V for short-channel LVT NMOS and PMOS at 4.3 K in Chapter 3. Fig.5.8 (a) shows what happens if V_{N-WELL} of an LVT NMOS GO1 transistor with $L_G = 34$ nm and $W_{NMOS} = 210$ nm is increased above +6 V. By fixing $V_{GS} = -150$ mV, we were able to probe the subthreshold region of $I_{DS} - V_{N-WELL}$. Importantly, we can observe that in the strong inversion region the current suddenly starts to decrease above approximately $V_{N-WELL} = 6.1$ V. This sets the upper boundary of FBB at +6 V. Above this upper boundary, current leakage through BOX is most probably the reason for the decrease of I_{DS}.

In Fig.5.8 (b) the static current appears only for the body-biasing region where the RO oscillates as shown in Fig.5.8 (c). From the static current analysis, we can directly observe that due to the V_{TH}-shift at low temperature, much higher FBB can be applied compared to room temperature before the transistors reach the zero-V_{TH} regime. To be able to apply even higher FBB, the room temperature V_{TH} might be increased by changing the gate stack or increasing L_G. It will result in higher charge carrier mobilities for the close-to-zero V_{TH} operation and thus better power-performance tradeoffs as it will be shown later.

Having identified FBB boundaries at 4.3 K, we will apply them to the case of an LVT ring oscillator. For instance, as shown in Chapter 3, by applying $V_{N-WELL} = -V_{P-WELL} = 5.8$ V to the LVT transistors with $L_G = 34$ nm, $W_{NMOS} = 210$ nm, and $W_{PMOS} = 300$ nm, we reached the near-zero-V_{TH} condition with $V_{TH-NMOS} = -24$ mV and $V_{TH-PMOS} = -49$ mV. This result was obtained for $V_{DS} = 1$ V. Then, the best FBB configuration at the lowest $V_{DD} = 0.325$ V was found to be $V_{N-WELL} = 4$ V and $V_{P-WELL} = -5.8$ V (see Fig.5.9 (a - c)). From Fig.5.9 (a) no minimum in Energy-Delay product versus V_{DD} for this FBB case can be observed down to 0.325 V. Although we recorded reasonably high I_{DYN} for even lower supply voltages, below $V_{DD} = 0.3$ V, the ROs stop to oscillate. Such behavior observed on 7 different samples with different L_G probably indicates that the design of the RO circuits was done to operate at $V_{DD} > 0.3$ V. Nevertheless,

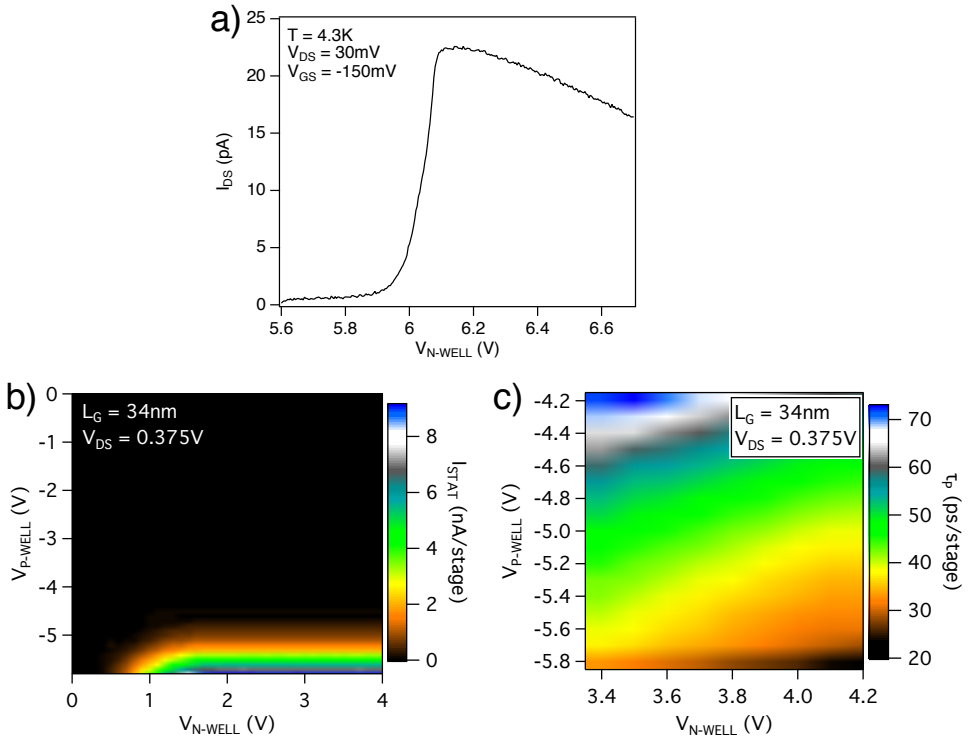
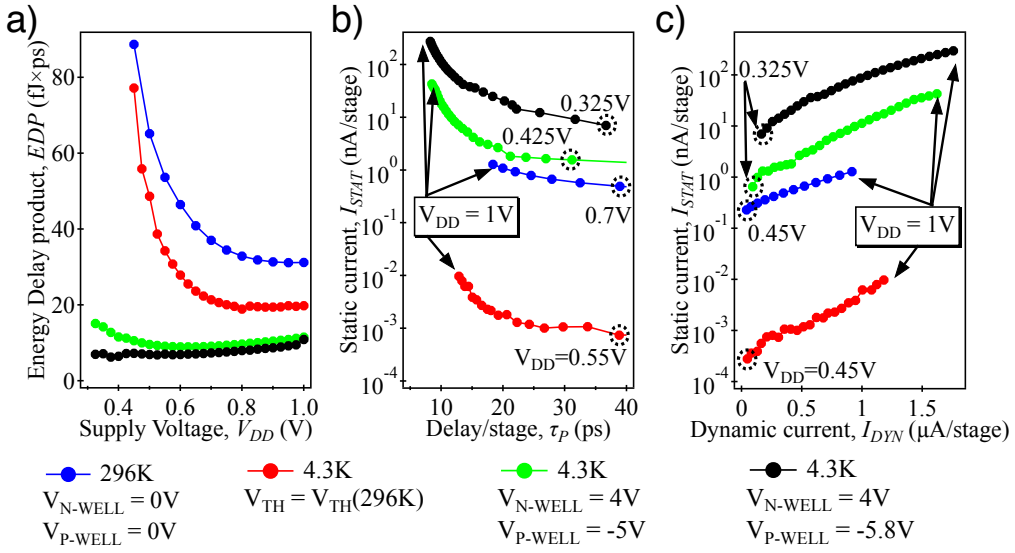


Figure 5.8: (a) $I_{DS} - V_{N-WELL}$ characteristic at $V_{DS} = +30$ mV and $V_{GS} = -150$ mV for LVT NMOS with $L_G = 34$ nm and $W_{NMOS} = 210$ nm recorded at 4.3 K. (b) I_{STAT}-analysis for a RO with $L_G = 34$ nm under high forward body-biasing. (c) A zoomed region of τ_P-analysis as a function of V_{N-WELL} and V_{P-WELL} where the RO approaches the close-to-zero V_{TH} mode of operation.

by comparing the blue and black curves of $EDP(V_{DD})$ in Fig.5.9(a), we demonstrate that the optimal V_{DD} can be reduced by the factor 3.1 at 4.3 K. Then, having the power proportional to V_{DD}^2 [2], we are able to reduce the power consumption by the factor 10 at 4.3 K. Note that at such reduced $V_{DD} = 0.325$ V, the delay per stage is found to be reasonably high as shown in Fig.5.9 (b)). Indeed, we obtained $\tau_P = 37$ ps/stage due to lowered threshold voltages and highly increased effective currents under aggressive FBB.

Some examples of power-performance improvement at 4.3 K are given in Fig.5.9 (d). The data in this table illustrate the tremendous versatility of 28 nm FD-SOI technology for both ultra-low power and high performance applications with highly reduced supply voltages at 4.3 K. They highlight the possible tradeoffs between delay and static/dynamic power dissipation.

If the specifications of a CryoCMOS circuit would require to have very low dynamic power consumption with increased τ_P (we do not need to have all the circuits working in the $10 - 100$ GHz-range), the 28 nm FD-SOI technology can provide very efficient solutions as illustrated in Fig.5.9(c).



d)

V_{DD} (V)	V_{N-WELL} (V) / V_{P-WELL} (V)	τ_P (ps)	P_{DYN} (nW/stage)	P_{STAT} (nW/stage)
0.325	4 / -5.8	37	55.25	2.275
	4 / -4.8	71	29.9	0.227
0.5	4 / -5.8	17	259	15
	4 / -4.8	21	213	0.8

Figure 5.9: (a) Comparison of Energy-Delay product vs V_{DD} at room temperature and 4.3 K with different forward body-biasing conditions. Note that for the case of very high V_{FBB} ($V_{N-WELL} = 4$ V and $V_{P-WELL} = -5.8$ V) no minimum is observed down to $V_{DD} = 0.325$ V. (b) Static current vs Delay/stage metric measured at RT and 4.3K for different V_{DD} (initial and final values for the studied V_{DD} interval are given). (c) Static current vs dynamic current for different V_{DD} at 296 K and 4.3 K. Note that depending on FBB voltage, I_{DYN} between 30 nA/stage and 1760 nA/stage can be achieved. Initial and final values for the studied V_{DD} interval are given. (d) Typical examples in terms of RO performance-power estimation at 4.3 K for highly reduced V_{DD}.

Indeed, dynamic power dissipation of only $10-15$ nW/stage can be achieved in the sub-GHz range as it can be guessed from Fig.5.9 (b - c).

5.7 Boosting the RO performance with relaxed L_G

Even though the mobility in the strong inversion regime is higher for longer L_G, the threshold voltage difference may result in lower driving currents and thus longer τ_P for ring oscillators [2]. Thus, for room temperature applications, the shortest possible L_G with the lowest threshold voltages enabling high performance while keeping low power consumption is usually chosen. In this section, it will be demonstrated that, at 4.3 K, by increasing L_G from 28 to 46 nm, we are able to achieve the same performance at highly reduced power dissipation due to the possibility to apply more FBB.

In Fig.5.10 the low field mobilities for NMOS and PMOS transistors are extracted using the well-known Y-function method [132] which consists in fitting $I_{DS}/G_m^{0.5}$ vs V_{GS} in the linear regime (V_{DS} = 50 mV). As already discussed in Chapter 3, an important mobility enhancement is expected at low temperatures due to the suppression of phonon scattering. In contrast to previous data reported on 14 nm FD-SOI transistors [183, 140], where short-channel mobilities were only slightly improved at low temperature,

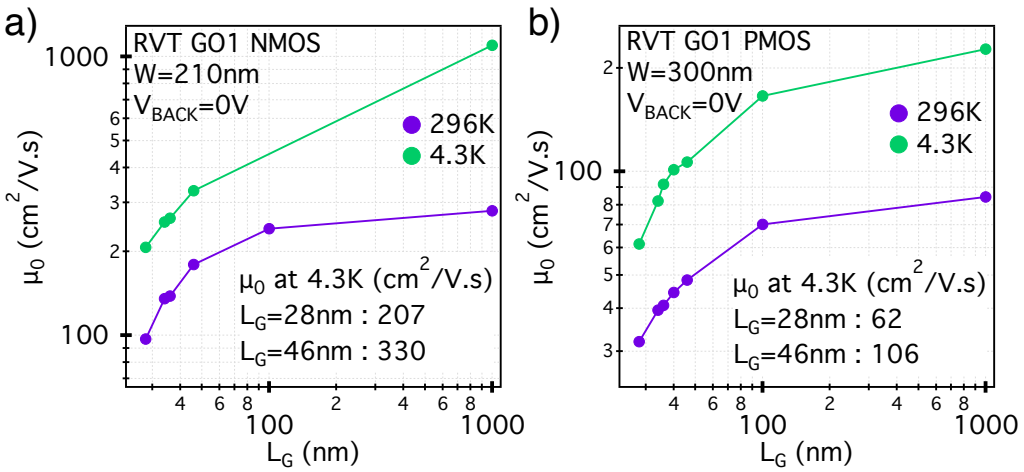


Figure 5.10: Low field μ_0 mobilities extracted using the Y-function method for gate lengths between 28 nm and 1 µm. (a),(b) room temperature and 4.3 K low field mobilities for RVT transistors (W_{NMOS} = 210 nm, W_{PMOS} = 300 nm) for different L_G extracted for $V_{N-WELL} = V_{P-WELL} = 0$ V.

here we found an important low field mobility enhancement at 4.3 K even for L_G as short as 28 nm as shown in Fig.5.10(a),(b). For the shortest gate length of 28 nm, the low field mobility is almost doubled at 4.3 K for both N- and PMOS transistors. At the same time, increasing L_G from 28 to 46 nm, μ_0(4.3 K) increases by 59% for NMOS and 71% for PMOS transistors for the same width. Similarly, using the recently developed Jazaeri mobility-extraction method [188], the maximal mobility was found more than two times higher at 4.3 K compared to 296 K for an NMOS transistor with $L_G = 46$ nm and $W = 80$ nm [114].

In Fig.5.11, the delay and static/dynamic power dissipation are shown for $L_G = 28$ nm and $L_G = 46$ nm. Note that the same FBB range is used for both ROs. The first important observation by comparing Fig.5.11(c) and (f) is that P_{STAT} measured at high FBB is much higher for $L_G = 28$ nm. This can be explained by the difference in threshold voltages between both L_G. The effect of gate length is discussed by using different metrics to compare the performance of ROs [2] such as: the same τ_P, P_{DYN}, P_{STAT}, and V_{N-WELL} / V_{P-WELL}.

For different benchmarking conditions, we used the data from Fig.5.11 recorded at $V_{DD} = 0.5$V. In Fig.5.12 (a) active and static power consump-

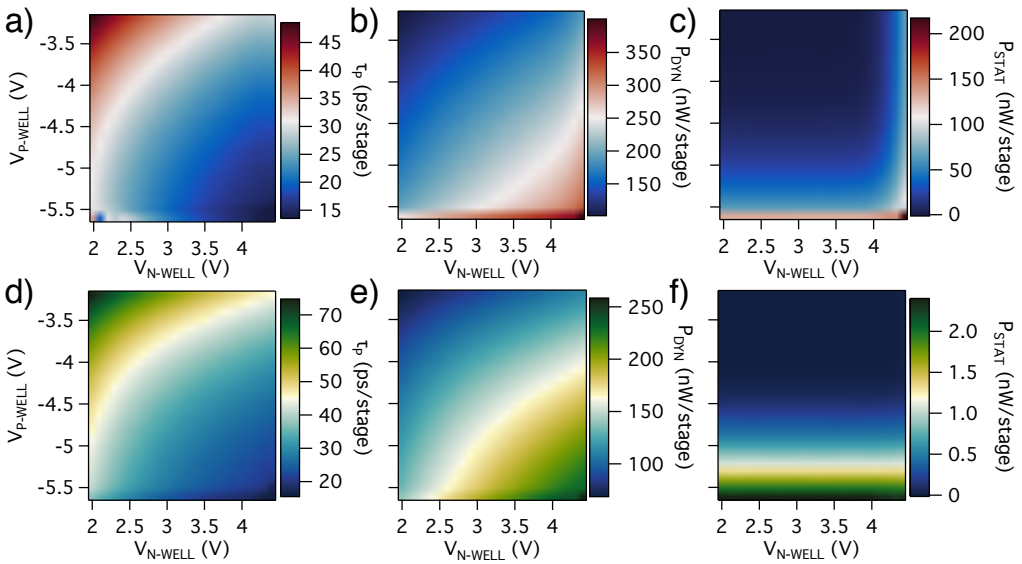


Figure 5.11: Performance of ROs at $T = 4.3$ K and $V_{DD} = 0.5$ V in terms of τ_P, P_{DYN}, and P_{STAT} for the same forward body biasing ranges. (a - c) $L_G = 28$ nm. (d - f) $L_G = 46$ nm. For both ROs $W_{NMOS} = 420$ nm and $W_{NMOS} = 600$ nm.

tion for the same τ_P of ROs (15.8, 18.2, and 23 ps/stage) are plotted as well as the FBB voltages applied for each case. Here, analysis of P_{ACT} (P_{DYN} - P_{STAT}) [2] instead of P_{DYN} is easier to understand since P_{STAT} highly increases under aggressive FBB for $L_G = 28$ nm. For $L_G = 46$ nm, C_{LOAD} increases because of higher gate capacitance. Then, to achieve the same τ_P as for $L_G = 28$ nm, higher I_{EFF} is needed. However, the active (switching) power is lower for $L_G = 28$ nm due to non-negligible P_{STAT}: 58.1 nW/stage at the lowest τ_P. This is why, despite a higher P_{DYN} for $L_G = 28$ nm, both RO have the same performance. Even though much higher FBB voltages are applied for $L_G = 46$ nm to achieve the same performance, due to higher threshold voltages, P_{STAT} remains very low even for $\tau_P = 15.8$ ps/stage.

On the other side, by keeping a constant dynamic power dissipation (124, 200, and 257 nW/stage) shown in Fig.5.12 (b), we also found that $\tau_P(P_{DYN} = 257$ nW/stage) is lower for $L_G = 46$ nm due to higher active power (see the difference in P_{STAT} in the last graph). Finally, P_{STAT} of the RO with longer L_G is at least 10 times lower despite higher FBB voltages applied to achieve the same P_{DYN}.

Then, by keeping constant the static power dissipation shown in Fig.5.11 (c), it can be concluded that the RO with longer L_G is much faster. This difference in τ_P is correlated with higher P_{ACT} obtained for more aggressive FBB in the case of $L_G = 46$ nm.

By probing the ROs under the same body-biasing conditions, we find that as FBB voltages are increased, the difference in speed becomes less and less important (at $V_{N-WELL} = 4.4$ V and $V_{P-WELL} = -5.6$ V less than 15%). Also, static power consumption is much higher for the shorter L_G (at $V_{N-WELL} = 4.4$ V and $V_{P-WELL} = -5.6$ V, we have 87 times lower P_{STAT} for the longer L_G). Therefore, the effect of higher P_{DYN} for shorter L_G is highly reduced regarding P_{ACT} and very similar τ_P are obtained for $V_{N-WELL} = 4.4$ V and $V_{P-WELL} = -5.6$ V.

Finally, it can be concluded that despite an increase of C_{LOAD}, it might be potentially useful to relax the gate length due to: (i) higher mobility for longer L_G, even for sub-100 nm L_G; (ii) higher threshold voltages for longer L_G allow to apply more FBB without having P_{STAT} highly increased in contrast to $L_G = 28$ nm. Then, P_{ACT} will be much higher for longer L_G and the effect of increased load capacitance can be overcome. Another argument for using longer L_G will be discussed in details in Chapter 6 where we compare the subthreshold regime of PMOS transistors with $L_G = 28$ and 46 nm and find a lot of oscillations and non-idealities degrading the average subthreshold swing below V_{TH} for the shorter device.

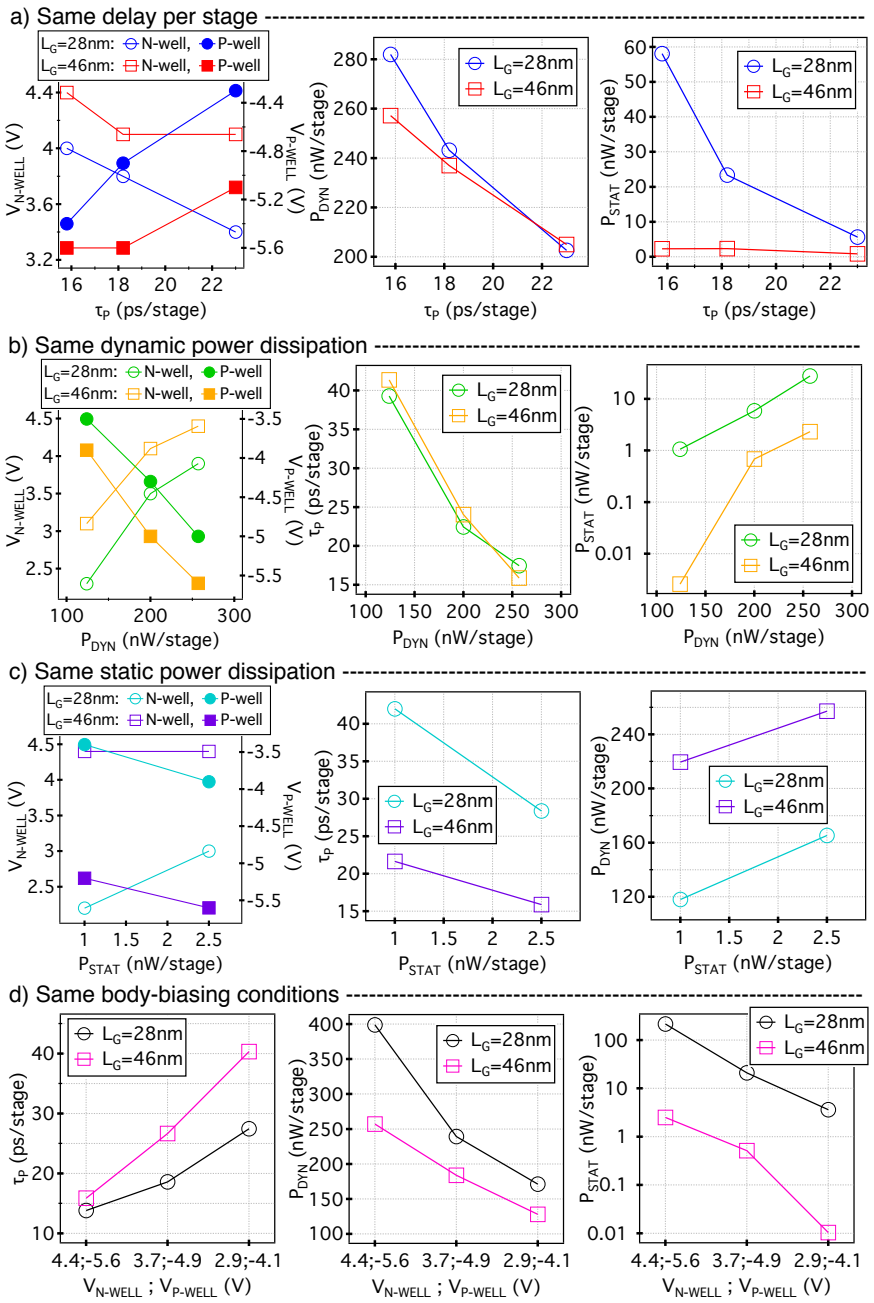


Figure 5.12: Analysis of ROs performance with $L_G = 28$ and 46 nm using different metrics: the same τ_P, P_{DYN}, P_{STAT}, and V_{N-WELL} / V_{P-WELL}. For (a-c), first graph shows the FBB configurations used for the calculations of τ_P, P_{DYN}, P_{STAT}.

5.8 Variability, zero-V_{TH} regime, and the optimal temperature of operation

A typical V_{TH}-shift induced by low temperature is presented in Fig.5.13 (a). Generally, it is almost the same for long- and short-channel transistors for high V_{DS} as we already discussed in Chapter 3. This assumption of the universal shift of V_{TH} allowed us to apply the compensating FBB for the LVT $L_G = 34$ nm RO with $W_{NMOS} = 420$ nm and $W_{PMOS} = 600$ nm.

A great concern for reliable operation of circuits is the device variability at low temperatures. Often, cryogenic characterization of the single device is only addressed due to the complexity of measurements [121, 123]. Moreover, in most of the recent cryogenic performance analysis, only long-channel and rarely short-channel NMOS are studied leading to a possible deduction that short-channel bulk PMOS transistors are problematic at cryogenic temperatures. [136, 149, 178, 183, 151, 189, 67].

The device variation in terms of threshold voltages recorded at $|V_{GS}| = 0.9$ V for short-channel NMOS and PMOS with $L_G = 28$ nm is shown in Fig.5.13(b)-(c).

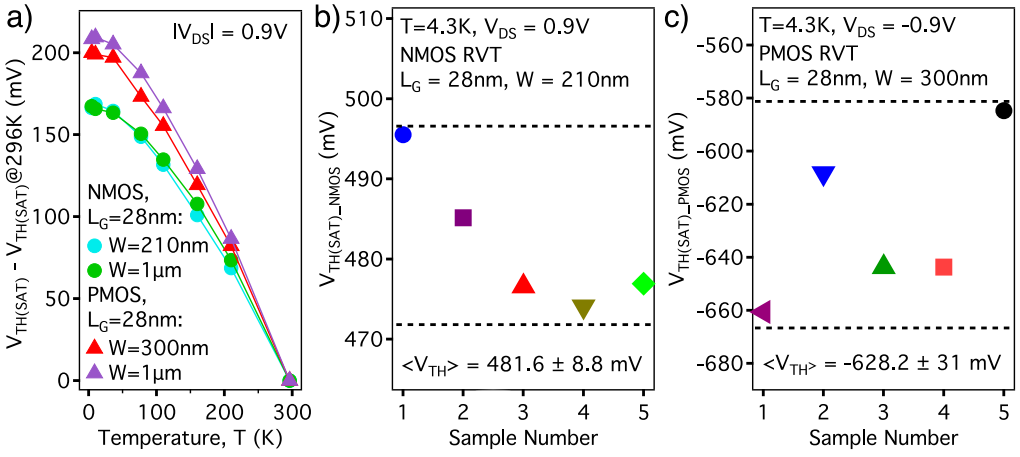


Figure 5.13: (a) Typical V_{TH}-shift at low temperatures for RVT GO1 NMOS and PMOS transistor with $L_G = 28$ nm and different widths for $|V_{DS}| = 0.9$ V. (b)-(c) V_{TH-SAT} variation between 5 identical samples giving a standard deviation of 8.8 mV for NMOS and 31 mV for PMOS at 4.3 K.

Although only 5 different samples of each type of device were measured, from these results we show that short-channel PMOS transistors have larger variability at low temperature: a standard deviation of 31 mV is achieved against 8.8 mV for NMOS at 4.3 K. Actually, the short-channel PMOS

variability could be explained by the presence of dopants diffused from the Source/Drain regions [122, 190]. The diffusion of dopants will be further discussed in Chapter 6. Moreover, oscillations and instabilities in $I_{DS}-V_{GS}$ for short-channel 28 nm FD-SOI PMOS in the subthreshold region should also be carefully taken into account as discussed in [114, 112]. Summarizing the variability analysis, we can conclude that the average $V_{TH-NMOS}$ can be brought closer to 0 V without an important increase in P_{STAT} whereas reducing $V_{TH-PMOS}$ close to zero would result in non-negligible static leakage because of their unstable subthreshold behavior and a larger average subthreshold swing below V_{TH}.

A mode of operation with highly reduced threshold voltages ($V_{TH-NMOS}$ = 0 V, $V_{TH-PMOS}$ = −110 mV) at 4.3 K is demonstrated in Fig.5.14(a) for LVT N-, and PMOS with L_G = 34 nm, W_{NMOS} = 210 nm, and W_{PMOS} = 300 nm at V_{N-WELL} = 4.04 V and V_{P-WELL} = −5.8 V. Some instabilities in the transfer characteristic of PMOS can be observed even for V_{DS} = 0.5 V. The static power dissipation of a RO with L_G = 34 nm was found to be 15.5 nW/stage. To understand the source of static leakage we made a hypothesis that NMOS transistors are mainly responsible for P_{STAT} due to lower $V_{TH-NMOS}$. Then, by decreasing V_{N-WELL} to 3.2 V the threshold voltage is increased and P_{STAT} is reduced to 2.5 nW/stage.

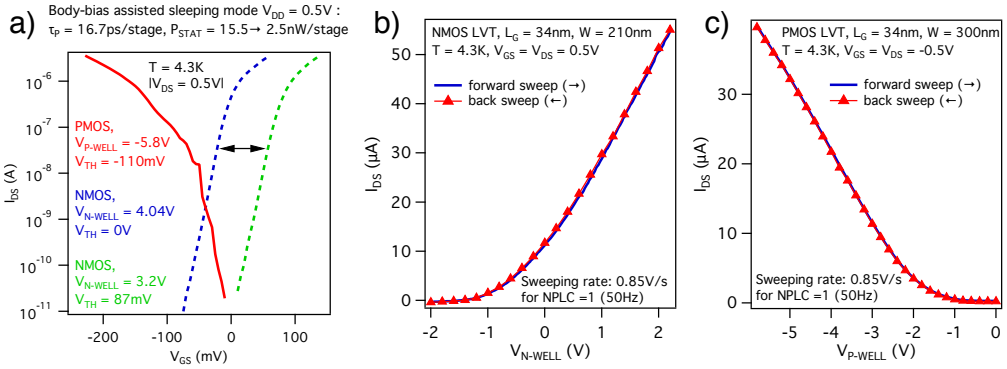


Figure 5.14: (a) Transfer characteristics for L_G = 34 nm NMOS and PMOS transistors with highly reduced V_{TH}. Note that despite much higher variability for short-channel PMOS, by reducing V_{FBB} of NMOS and hence increasing $V_{TH-NMOS}$, P_{STAT} of a RO with the same L_G is reduced from 15.5 nW/stage (blue curve with the corresponding τ_P = 16.7 ps/stage) to 2.5 nW/stage. (b),(c) Opening the channel of NMOS and PMOS LVT transistors with L_G = 34 nm at 4.3 K. For both transistors, there is no hysteresis for fast forward and back sweep with V_{N-WELL} and V_{P-WELL}.

Contrarily to large hysteresis loops observed at 20 mK while sweeping back and forward transistors with body-biasing fabricated [145] (due to highly increased freeze-out of the backplane doping as explained in [121]), no hysteresis was observed at 4.3 K in our samples when opening and closing the transistors at a high sweeping rate of FBB voltages 0.85 V/s as shown in Fig.5.14 (b - c). The time of read-out by digital multimeter at standard integration time NPLC = 1 (16.7 ms per measurement point) is taken into account. Thus, we conclude that an ultra-efficient body biasing of the technology can be fully exploited down to 4.3 K. Moreover, the thermal budget or the total power of the CryoCMOS circuits that can be dissipated is limited to a few watts at 4.3 K [191]. For a sub-Kelvin temperature, this restriction is even strongly increased: a state-of-the-art dilution cryostat can manage only a 25 µW-power dissipation at 20 mK [192]. Then, we can conclude that 4 K is the most suitable temperature for cryoelectronics build with 28 nm FD-SOI technology because of: i) manageable power dissipation of a few watt and ii) an efficient body biasing which is essential for the V_{TH}-shift compensation to drastically improve the circuit's performance.

Finally, having demonstrated a very stable and efficient body biasing capability, we can consider a dynamically-assisted RO mode of operation at 4.3 K. The principle described in [193, 194], consists in dynamically reducing FBB voltages applied to the circuit in the sleeping mode to further decrease static power dissipation. In our case, we can simply apply small AC-voltages on V_{N-WELL} and V_{P-WELL} when the circuit is in the sleeping mode to effectively reduce static power consumption as can be seen in Fig.5.11(c) when, for instance, V_{P-WELL} is changed from -5.8 to -5.5 V. In addition, DTMOS regime demonstrated in Chapter 4 might be of great potential for low-power and high-performance cryoelectronics at 4.3 K [166]. However, the impact of DTMOS operation regarding the dynamical variability of V_{TH} at low temperature due to low frequency and random telegraph noises should be carefully considered as it was done for 28nm FD-SOI at room temperature in [195].

5.9 Conclusions

In this chapter, for the first time, electrical characterization of 28 nm FD-SOI ring oscillators down to 4.3 K has been demonstrated. The unique capability of body-biasing being fully efficient at 4.3 K in the development of fast power-efficient peripheral circuitry has been shown through the analysis of the delay per stage, static and dynamic current (power) of ROs with different gate lengths. Also, the tradeoffs between energy consumption and

delay per stage have been discussed for a large range of supply voltages. We have demonstrated that by properly balancing power and performance, the maximum benefit in terms of speed and energy consumption can be derived at a very low supply voltage of only $V_{DD} = 0.325$ V.

At 4.3 K and close-to-zero-V_{TH} operation, a very small Energy-Delay product of 6.9 fJ×ps with $\tau_P = 37$ ps have been achieved at $V_{DD} = 0.325$ V. Moreover, at 4.3 K, we have found the upper and lower boundaries of body-biasing between $-6... + 6$ V.

We could correlate the behavior of isolated transistors to that of RO down 4.3 K and thus conclude that, for 28 nm FD-SOI technology, C_{LOAD} of a single inverter is only weakly dependent on temperature.

Contrarily to the common strategies of increasing supply voltage and/or re-designing V_{TH} for low-temperature circuits, we have shown that thanks to body-biasing, the 28 nm FD-SOI is fully suitable for CryoCMOS requiring both ultra-low power dissipation and high performance.

It has been demonstrated that an improved power-performance tradeoff can be met with relaxed L_G thanks to higher electron and hole mobilities, and higher V_{TH} allowing to apply more FBB.

While discussing the variability issues of short-channel transistors, it has been argued that despite a stronger $V_{TH-PMOS}$-variability at 4.3 K, it is still possible to achieve an effective RO power management in the close-to-zero-V_{TH} mode of operation.

Finally, the absence of hysteresis loops when opening the transistor through body-biasing at a high sweeping rate at 4.3 K and the thermal budget constraint led us to the conclusion that the optimal temperature for 28 nm FD-SOI cryoelectronics will be probably limited to 4.3 K.

Chapter 6

Duality of short-channel FD-SOI transistors: from FETs to SETs

In this chapter, the current progress in using conventional CMOS transistors for quantum computing applications (mostly oriented towards dopant-based physics) is presented. Unexpectedly, we demonstrate a very high degree of confinement in NMOS and PMOS short-channel devices with $W \gg L_G$ when V_{DS} is reduced typically below 20 mV leading to the transition FET-to-SET at 4.3 K. We thoroughly characterize the quantum dot parameters such as the addition, charging and orbital energies; gate, source and drain capacitances, lever arm parameter, etc. From our estimation based on C_G, the size of QDs is found to be much smaller than the one expected from lithographically-imposed geometry. The evolution of quantum dots under wide-range body-biasing is presented at 4.3 and 1.4 K. In addition, the benchmarking of the QDs obtained in standard FD-SOI transistors with respect to the most common Si-based devices is given. From cryogenic characterization of PMOS with short-L_G at low V_{DS}, the issues related to the diffusion of boron atoms from Source/Drain regions mentioned in Chapters 3-5 are explained. Finally, possible solutions to achieve stable and tunable quantum dots as well as 'classical'-behavior FETs at higher V_{DS} are proposed for the PMOS devices. We finish this chapter by presenting a hybrid (cryoelectronics and quantum devices) circuit recently designed using 28 nm FD-SOI and discuss the future of this technology regarding the implementation of a qubit and its further co-integration with CryoCMOS within the same FD-SOI platform.

6.1 Setups used for low-temperature measurements

The FD-SOI transistor cryogenic measurements down to 1.4 K presented in this chapter were done using an 'Orange cryostat' [196]. To achieve temperatures below 4.3 K while using ^4He as a cryogenic liquid, we used an additional pumping system to lower the temperature below 2.2 K (temperature at which ^4He changes its state and becomes superfluid) [197]. The programs for fast data acquisition using Labview-interface were developed by Andrea Corna. Similarly to the setup description given in the previous chapters, we also had home-made optoisolated DC sources to feed the voltages and a transimpedance amplifier (TIA) for current-to-voltage conversion which then was recorded using a digital multimeter.

6.2 Conventional CMOS and Si-based MOS structures for quantum computing

The interest of low-temperature characterization of CMOS and Si-based MOS structures for quantum computing applications has grown up after the famous $Loss - DiVincenzo$ proposal of quantum computation with quantum dots [25]. Even more, starting from the proposal of a silicon-based nuclear spin quantum computer [198], different qubit platforms using silicon as a host material were demonstrated, such as: $Si/SiGe$ heterostructures (scalabe 1D architecture [56], single spin qubits [33, 89, 60]), two-gate-levels Si MOS structures (quantum dot characterization [199], the first two-qubit logic gate [23]) and qubits using impurities to encode information (see single/coupled atom transistors using phosphorous [111, 200] and arsenic [201] in silicon lattice, and moreover, demonstrating donor and nuclear spins qubits [34]).

Recently, as discussed in Chapter 2, a close-to-industrial CMOS nanowire technology was used to demonstrate the first hole spin qubit [26, 182] and an electrically driven electron spin (opening the way towards the electron spin-valley qubit) [27].

The same nanowire platform was also successfully used to develop and study new techniques of spin read-out [47, 202, 203]. Having already explained in Chapter 1 the advantages of using impurities to encode and store quantum information, the dopant's physics in MOSFETs has been largely addressed. In [204], the spin lifetime of 30 s was reported and the coherent electrical control of two dopants [205, 206] was also demonstrated.

To reinforce the importance of dopants in the MOSFET's channel, within the dopants-based quantum computing paradigm, it is worth mentioning that the high-selectivity of donor-based Pauli Spin Blockade (PSB) read-out was demonstrated with planar Si MOS structure [207] as well as with a nanoscale SOI PMOS fabricated with 0.13 μm bulk technology [208].

However, the main drawback of the dopants-based large-scale quantum computer remains scalability and reliability issues: indeed, depending on the dopant's position in the silicon channel, the experiment will give every time high-fidelity and very performant qubits which are, however, unique regarding gate voltages needed to achieve the quantum confinement to isolate spins.

Therefore, the most straightforward approach we follow in this chapter is to: first, demonstrate the transition from field-effect-transistor (FET) to single-electron-transistor (SET) as it was already shown for SOI nanowire transistors in [153] and then to characterise the typical addition energies E_{ADD} (the energy needed to add an additional electron by overcoming Coulomb interactions and accounting for orbital spacing [77]) and lever-arm parameters α (an equivalent of subthreshold swing in usual MOSFET devices [77]) of quantum dots created in FD-SOI transistors at 4.3 K and below. Hence, in this chapter, we will argue that industrial-level 28 nm FD-SOI technology, in addition to its excellent suitability for cryoelectronics demonstrated in Chapter 5, can be used to create single electron and hole quantum dots with an excellent electrostatic control and large addition energies and thus, be of interest for qubit applications.

6.3 FET-to-SET transition in NMOS at 4.3 K

In Chapter 5, we have shown that supply voltage of ring oscillator can be drastically reduced down to 0.3 V while keeping high performance and low power consumption. However, at a low supply voltage, advanced CMOS technologies operating at cryogenic temperature often suffer from dopant- or disorder-induced non-idealities which result in non-predictable V_{TH}-shifts and highly irregular behavior in $SS - I_{DS}$ metric in the subthreshold region [121, 123]. In Fig.6.1 (a) an excellent subthreshold behaviour of LVT transistors (previously used for the characterization of ring oscillators) is demonstrated at $V_{DS} = 100$ mV only. Importantly, when V_{DS} of the same transistor is reduced to 5 mV, we observe a typical SET behavior with Coulomb Oscillations due to the discrete energy spectrum of a quantum

dot [125, 77] (see Fig.6.1 (b)).

To be able to define a QD or SET, two main conditions must be fulfilled. Firstly, the temperature of operation must be lower than typical addition energy [77]

$$E_{ADD} = E_C + E_{ORB} \gg k_B T, \tag{6.1}$$

where E_C is the charging energy required to overcome the Coulomb repulsion and put the second electron (hole) with the opposite spin (as required by the Pauli Exclusion Principle) on the same orbital of QD. E_{ADD} is the energy to be paid to populate a higher energy orbital once the lowest energy one is populated. This condition is well fulfilled in our case for both hole and electrons with E_{ADD} of $15-20$ meV whereas the thermal energy at 4.3 K is only 0.37 meV.

Secondly, the tunnel barriers modeled as the access resistances connected in parallel with the Source/Drain capacitances (see Fig.6.1 (c-d)) must be high enough to ensure a sufficient confinement [209]. Thus, the access resistances should be much higher than the quantum of resistance :

$$R_{ACC} \gg R_Q = \hbar/e^2 = 25\ kOhm \tag{6.2}$$

If the condition given in 6.2 is not met, the peaks of current are induced by the universal conductance fluctuations in the diffusive regime and, being poorly sensitive to the temperature, they do not evolve into sharp resonances (meaning a precise control over the number of electrons/holes in a QD) at lower temperatures [190]. In case of a LVT NMOS transistor in Fig.6.1 (b), for $V_{DS} = 5$ mV at $V_{GS} = 0.385$ V (where the first clear resonant peak can be seen), we obtain the access resistances $R_{ACC}(4.3\text{ K}) = 1.45$ MOhm which is lower than typically $4-5$ MOhm observed in quantum dots designed with Leti's nanowire technology which uses $20-40$ nm-thick spacers (see Chapter 2 and [108]). The latter is explained by well optimized LDD doping and the use of thin spacers. Indeed, 9 nm-thick spacers are used in the case of 28 nm FD-SOI as shown in Fig.6.1 (c). By accounting for the relative cryogenic V_{TH}-shift of 0.2 V ($V_{GS} = 0.385 - 0.2 = 0.185$ V), we have found a lower access resistance $R_{ACC}(296\text{ K}) = 0.47$ MOhm. The higher access resistance at 4.3 K can be explained by a partial freeze-out of LDD regions [209, 138].

To model a SET, we use the constant interaction method [76] where the following assumptions are considered: (i) the Coulomb interactions among electrons in the dot, and between electrons(holes) in the dot and those in the environment, are parametrized by a single, constant capacitance C_{TOT}. This capacitance is the sum of capacitances between the dot and the source

C_S, the drain C_D, and the gate C_G. Thus, the total capacitance can be described as : $C_{TOT} = C_S + C_D + C_G$. The ratio C_G/C_{TOT} is the lever arm parameter α characterizing the effectiveness of the gate control. Secondly, we suppose that the single-particle energy-level spectrum is independent of interactions with electrons(holes) already put in the QD and therefore of the number of electrons(holes).

After having identified that the first electrons can be electrostatically confined at low V_{DS}, high-resolution $V_{GS} - V_{N-WELL}$ scans (stability diagrams) were recorded for two LVT NMOS transistors with $L_{GS} = 28$ (Fig.6.2(a)) and 34 nm (Fig.6.2(b)) with $W = 300$ nm. Note that although the use of a charge detector is required in order to make sure that we measure the first electrons, by consequently increasing V_{DS} above 30mV up to 1 V, no new states in DC transport measurements were detected.

When carefully comparing the stability diagrams in Fig.6.2, one can notice a very similar behavior of the resonant current peaks for reverse body biasing ($V_{N-WELL} < 0$) with the line of resonant current corresponding to the first electron in the quantum dot clearly visible. It means that we are able to tune the transistors in the SET regime. Another observation is that when V_{GS} is lowered, the channel remains empty below the first electron line for a large window of body biasing. This illustrates the advantage of the undoped channel to anticipate and control the few-electron quantum dots. Analyzing the stability diagrams becomes much more complicated in the forward body-biasing regime. For instance, for $V_{N-WELL} > 0$ V one can observe additional states with a different slope. It can be attributed to the local density of states due to disorder (as discussed in Chapter 4) or dopant-assisted confinement as the wavefunction is extended over the Si/BOX interface [69, 41] and hence, the first electrons are more affected by the proximity to the Source/Drain regions.

6.4 Evolution of n-type quantum dots under different body biasing

Before analyzing the Coulomb diamonds observed in the LVT NMOS devices presented in Fig.6.2, let us comment on Typical widths of QDs defined in Si nanowires shown in Chapter 2 was $40 - 80$ nm whereas in this section, the quantum dots with comparable addition energy (relative size) will be shown for $W = 210$ nm. Actually, in [190], the phenomenon of Coulomb blockade was reported for nanoscale MOSFET transistors with $L_G = 50, 100$ nm and $W = 1000, 400$ nm. The authors demonstrated that

in the dielectric regime (silicon at low temperature in the very weak inversion regime) for short-channel transistors with channel width up to µm and $W \gg L_G$, the total conductance (current) can be dominated by a single contribution from a square conductance of size $L_G \times L_G$ in MOSFETs in

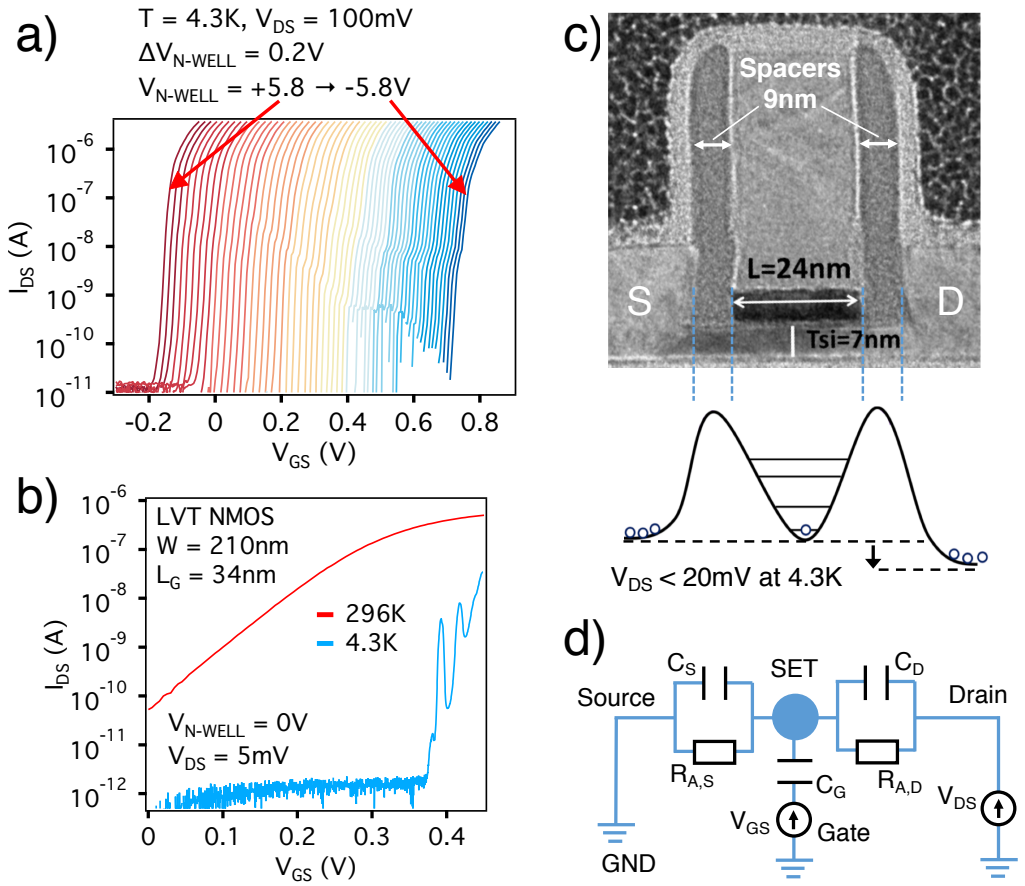


Figure 6.1: FET-SET duality at 4.3 K in LVT NMOS depending on V_{DS}. (a) $I_{DS} - V_{GS}$ characteristics for different V_{N-WELL} of a short-channel LVT NMOS transistor at $V_{DS} = 100$ mV fully suitable for ultralow-V_{DD} cryogenic electronics applications. (b) Transfer characteristics at 296 and 4.3 K at $V_{DS} = 5$ mV. (c) An illustration of SET regime where the spectrum quantization at low V_{DS} typically below 20 mV can be observed (TEM image taken from [116]). (d) Constant interaction model [76] to describe a SET (QD). The QD is capacitively coupled to the gate (C_G) and the connection to the Source/Drain is modeled with tunnel junctions (the access resistances $R_{A,S}$, $R_{A,D}$ with the corresponding capacitances C_S, C_D in parallel). Note that the back-gate capacitively coupled to the SET is not shown.

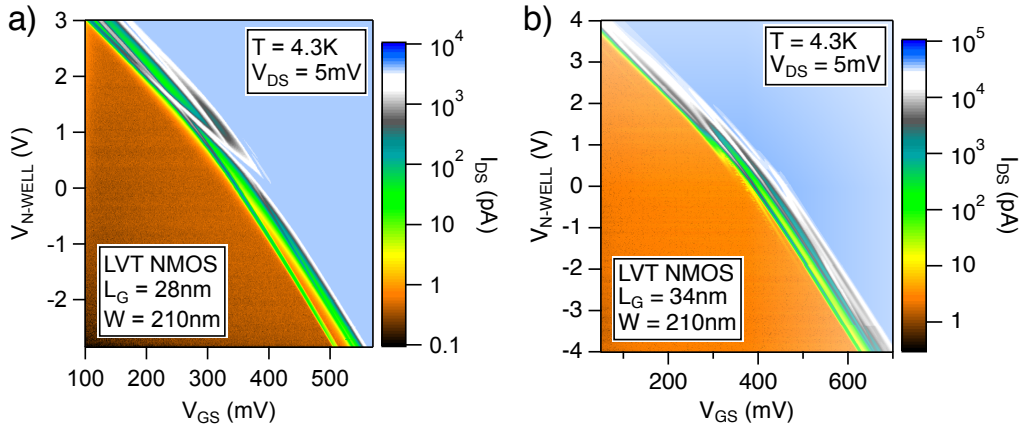


Figure 6.2: Stability diagrams $V_{GS} - V_{N-WELL}$ for two LVT NMOS with $L_G = 28$ (a) and 34 nm (b). Note that the Coulomb oscillations can be clearly observed despite $W \gg L_G$ in both cases. For these high-resolution scans, the current compliance was limited to 4 and 40 nA to achieve sub-pico current resolution by setting high gains of 10^9 and 10^8 of TIA.

spite of $L_G \ll W$. Then, the QDs of a very small 2D size with 25×25 nm^2 for $L_G = 50$ nm, $W = 1$µm and 50×50 nm^2 for $L_G = 100$ nm, $W = 400$ nm were reported. Thus, it was concluded that at low temperature a disorder-induced single quantum dot can be created in relatively wide-channel geometries. We have tested several short-channel LVT NMOS samples with $W = 1$µm at 4.3 K but the Coulomb blockade with distinct resonant peaks was not observed.

For the NMOS samples with $W = 210$ nm, we performed a detailed analysis of the stability diagrams shown in Fig.6.2 by recording Coulomb diamonds $V_{DS} - V_{GS}$ at different V_{N-WELL} from reverse body biasing (RBB) to forward body biasing (FBB).

For the shorter device with $L_G = 28$ nm, when changing V_{N-WELL} from 0 V to negative values (Fig.6.3(b - d)) we observed the tuning of QDs with respect to V_{GS} with quasi-constant addition energies for adding the first additional electron $E_{ADD-1} = 19.5$ meV. Having observed no extra feature appearing below the first resonance up to $V_{DS} = 40$ mV, we suppose that the first electrons in the channel have been observed. For the case of $V_{N-WELL} = -2.8$ V shown in Fig.6.3 (b), we see that while the first diamond size is similar to the case of $V_{BACK} = 0$ V (see Fig.6.3 (d)), the second one becomes larger under FBB ($E_{ADD} = 10.2$ meV against 5.6 meV at $V_{BACK} = 0$ V). This change of the size of the second diamond means that the orbital splitting increases. Therefore, the QD size doesn't change under

FBB but at $V_{N-WELL} = 0$ V it is more shallow than at $V_{N-WELL} = -2.8$ V. It is consistent with the effect of RBB, e.g pushing the electron wavefunction towards the upper Si/SiO_2 interface and thus enhancing the quantum confinement. This demonstrates an excellent tunability of QDs with body biasing. However, in the case of FBB with $V_{N-WELL} > 0$ V shown in Fig.6.3 (e - f), an additional quantum dot having a different slope (coupling) with respect to the backgate can be observed. Such double quantum dot configuration under FBB can be used for the qubit demonstration (one QD to store and manipulate the spin and another for PSB read-out as it was done in [208]).

Then, the same kind of analysis was performed for the sample with a larger gate length $L_G = 34$ nm and the results are shown in Fig.6.4. A similar large $E_{ADD} = 15.9$ meV for adding the first electron was found up to strong RBB with $V_{N-WELL} = -5.8$ V as can be seen from Fig.6.4(b - d).

Upon increasing RBB, the QD levels become deeper. Indeed, at $V_{N-WELL} = -5.8$ V shown in Fig.6.4 (b), we can put up to 3 additional electrons whereas at lower RBB, after 2 electrons, the Coulomb-blocked region almost vanishes, see Fig.6.4 (c-d). Finally, contrarily to the case of $L_G = 28$ nm, at high FBB ($V_{N-WELL} = 5.8$ V), by analyzing the stability diagram shown in Fig.6.4 (f), it can be seen that the Coulomb blockade region becomes highly suppressed similarly to QDs defined in SOI nanowires reported in [153].

In Table 6.1, the main parameters of QDs for the NMOS samples analyzed previously are given for the case of intermediate RBB ($V_{N-WELL} = -1.8$ V). A notable result is that the gate capacitance C_G (which is similar to the semiconductor capacitance C_{Si} discussed in Chapter 4) deduced from the Coulomb peak spacing is much smaller than C_{OX} calculated from $EOT_{NMOS} = 1.55$ nm. This observation is in line with the fact that in the weak inversion regime (characterized by a very low charge density in the silicon channel) $C_{OX} \gg C_{Si}$. Source-to-gate C_S and drain-to-gate C_D capacitances estimated from the slopes of the first Coulomb diamond (see Fig.6.5 (a)) are much smaller than C_G which gives an excellent gate-control with α close to 1 for both samples. Thus, the advantage of using an ultra-thin EOT is highlighted. Then, the 2D size of the quantum dots can be estimated from C_G. This gives 17.1×17.1 nm^2 and 17.6×17.6 nm^2 for respectively $L_G = 28$ nm and $L_G = 34$ nm.

We can note that the QD size is much smaller than the gate surface $L_G \times W$. Although, it is difficult to explain the reason for such a high degree of confinement and where the quantum dots are located in the channel, if it turns out that similar E_{ADD} can be obtained for all such samples, the 28 nm FD-SOI platform might be of great interest for qubit applications. Indeed, given the high addition energies (compared to the thermal energy)

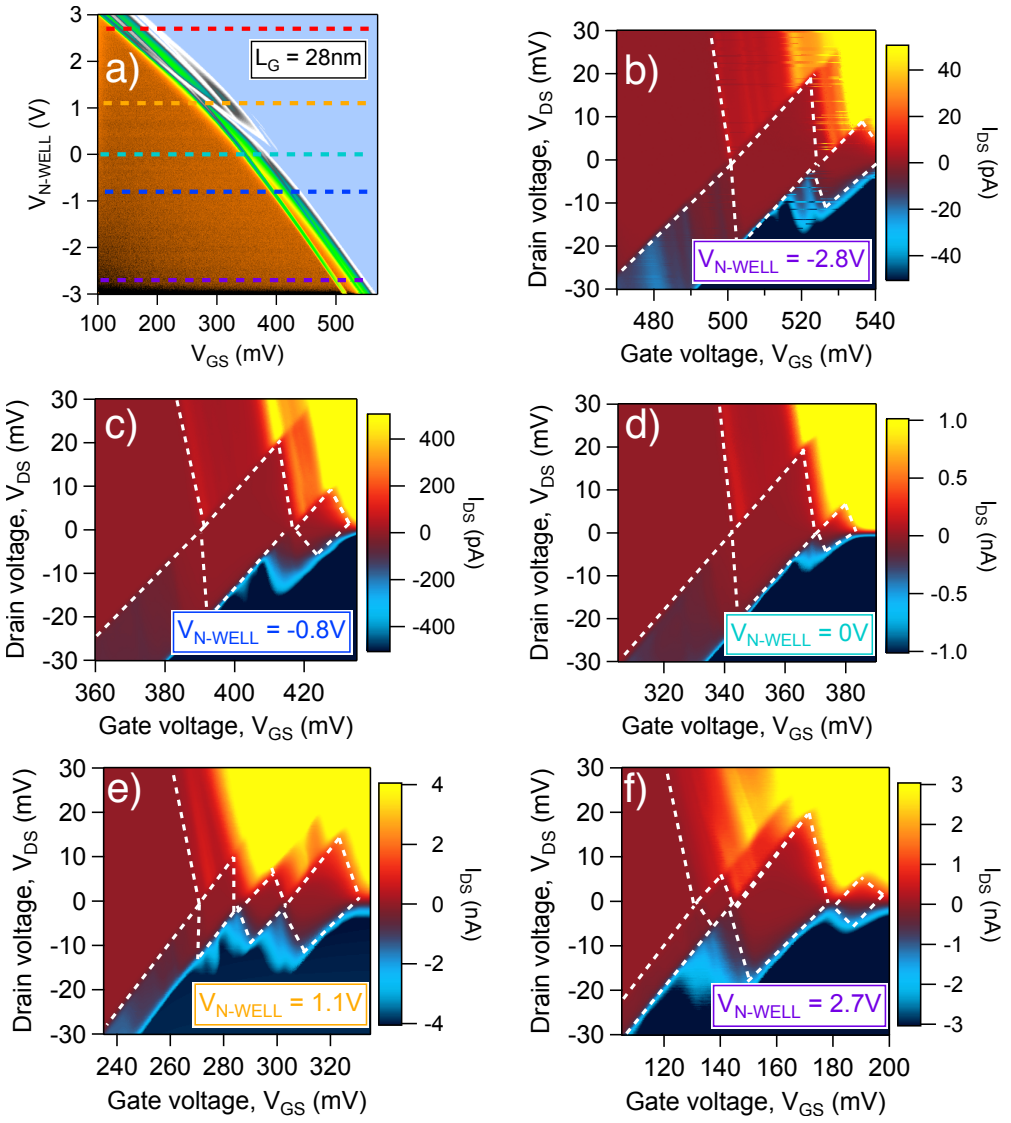


Figure 6.3: (a) Stability diagram from Fig.6.2 (a) for a LVT NMOS with $L_G = 28$ nm, $W = 210$ nm at 4.3 K. (b)-(f) Coulomb spectroscopy analysis $V_{DS} - V_{GS}$ for different V_{N-WELL} shown in (a) with dashed lines of different colour.

in Si-based quantum dots and typical spin relaxation times at $1 - 4$ K [20], it would allow us to fabricate both the cryoelectronics of control and qubits using the same industrial-level platform.

Finally, we benchmarked the quantum dots observed in FD-SOI transistors with respect to the most commonly used structure for Si-based qubits:

$Si/SiGe$ heterostructures [56], Si MOS QDs [199] and dopant-based QDs [111]. In Fig.6.5 (b) the effectiveness of gate-control in terms of α is demonstrated for both 28 nm FD-SOI and SOI nanowire QDs. Regarding the typical charging energies for $Si/SiGe$ heterostructures and Si MOS QDs, we obtain much higher E_{ADD-1} for the first additional electron. In addi-

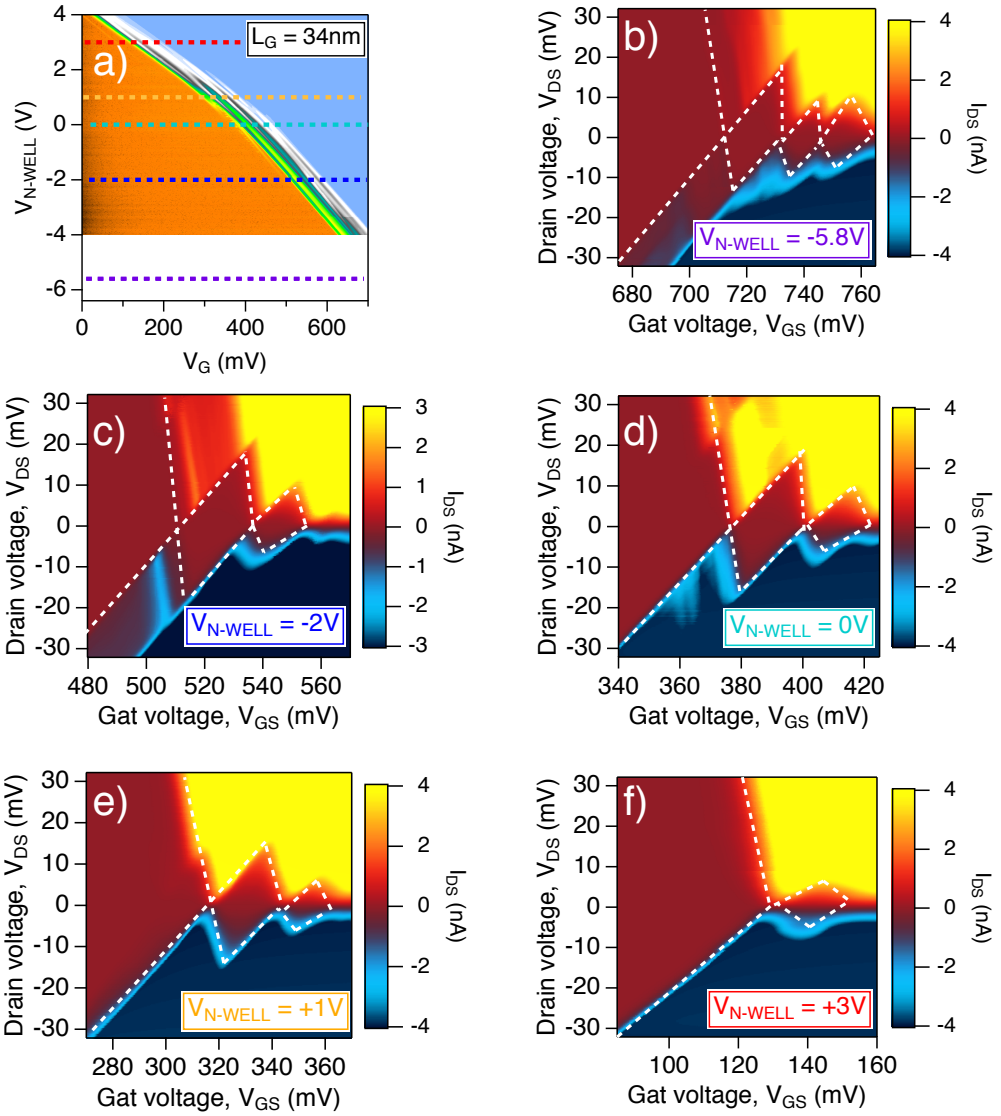


Figure 6.4: (a) Stability diagram from Fig.6.2 (b) for a LVT NMOS with $L_G = 34$ nm, $W = 210$ nm at 4.3 K. (b)-(f) Coulomb spectroscopy analysis $V_{DS} - V_{GS}$ for different V_{N-WELL} shown in (a) with dashed lines of different colour.

L_G(nm)	C_{OX}(aF)	C_G(aF)	C_S(aF)	C_D(aF)	$E_{ADD-1}(meV)$	α
28	131	6.55	0.89	1.11	19.5	0.77
34	159	6.93	1.11	1.25	15.9	0.75

Table 6.1: 4 K quantum dots parameters for two NMOS samples with $L_G = 28$ nm and 34 nm and $W = 210$ nm at $V_{N-WELL} = -1.8$ V. E_{ADD-1} stands for the addition energy of the first additional electron.

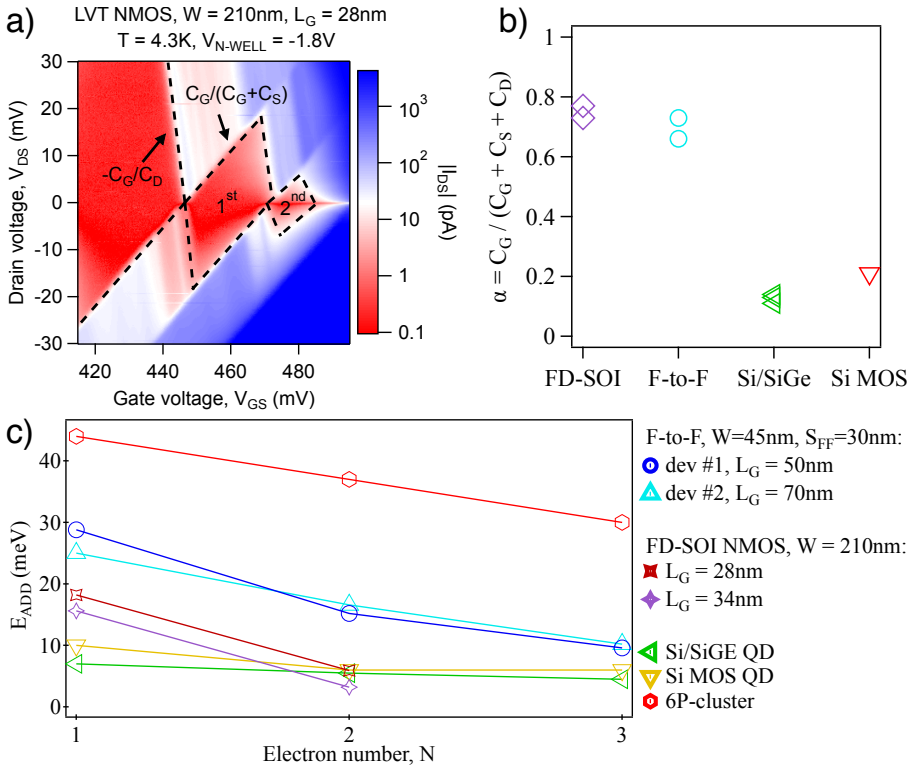


Figure 6.5: (a) Typical Coulomb diamonds observed in short-channel NMOS. (b),(c) Benchmarking of FD-SOI quantum dots with respect to the Corner Dots observed in F-to-F devices (see Chapter 2), $Si/SiGe$ QDs [56], Si MOS QDs structures with two levels of gates [199], and six-phosphorus-based QDs [111].

tion, they are similar to E_{ADD-2} for F-to-F devices. Note, that E_{ADD-1} between $25 - 30$ meV for SOI nanowire QDs are most likely due to the dopant-assisted confinement as discussed in Chapter 2. Even though E_{ADD} can be as high as 40 meV for STM-defined phosphorous-based cluster of dopants in silicon, it should be noted that each additional electron is added

on a different dopant.

6.5 Problems with short-L_G PMOS at 4.3 K and possible solutions

In previous chapters, we already mentioned the crucial role of dopants regarding the cryogenic behavior of short-channel PMOS, especially in the subthreshold region. In Fig.6.6 (a) a 4 K stability diagram recorded at $V_{DS} = -5$ mV for a LVT PMOS with $L_G = 34$ nm is shown.

When V_{DS} is increased to -100 mV, contrarily to the case of short-channel NMOS (see Fig.6.1 (a)), we observe in Fig.6.6 (b) a highly irregular behaviour in the subthreshold region with more and more oscillations when negative (FBB) voltage is applied.

The hypothesis about boron atoms highly impacting short-channel transport is now supported with the stability diagram analysis. Indeed, in Fig.6.6 (c - d) we can see very irregularly-shaped diamonds with the additional energy for first holes ($30-40$ meV) reaching this of boron clusters coupled with disorder-induced surface states as demonstrated with simulations in Chapter 2. It is worth mentioning, that despite ultra-thin $EOT_{PMOS} = 1.7$ nm, the presence of high-κ material and spacers (both of which are likely to contain positive/negative charges and thus affecting low-temperature transport) we have not observed such replicas and switching behaviour for the NMOS transistors ($EOT_{PMOS} > EOT_{NMOS}$) as it can be seen from Fig.6.5 (a). Hence, we can conclude that the issues with low-temperature transport in short-channel PMOS widely mentioned in Chapter 3-5, are likely due to boron dopants diffused from Source/Drain regions.

Given a reduced impact of dopants when the gate length is increased (the hole effective mass is higher than the electron one and thus holes are more sensitive to the disorder which impacts the confinement of hole wavefunction), an important improvement in the subthreshold region at higher V_{DS} is expected. In Fig.6.7, a comparison using the $SS - I_{DS}$ metric between two PMOS transistors with $W = 300$ nm and different L_G is shown. In case of $L_G = 28$ nm (Fig.6.7 (a)) for both low and high V_{DS}, strong oscillations can be observed below V_{TH} thus, partially cancelling the effect of reduced SS.

These oscillations visible even at $V_{DS} = -0.9$ V would likely introduce non-negligible instabilities in a cryoelectronics circuit built using CMOS logic. Nonetheless, when L_G is increased to 46 nm, much more regular subthreshold behavior even for $V_{DS} = -50$ mV is observed Fig.6.7 (b) which

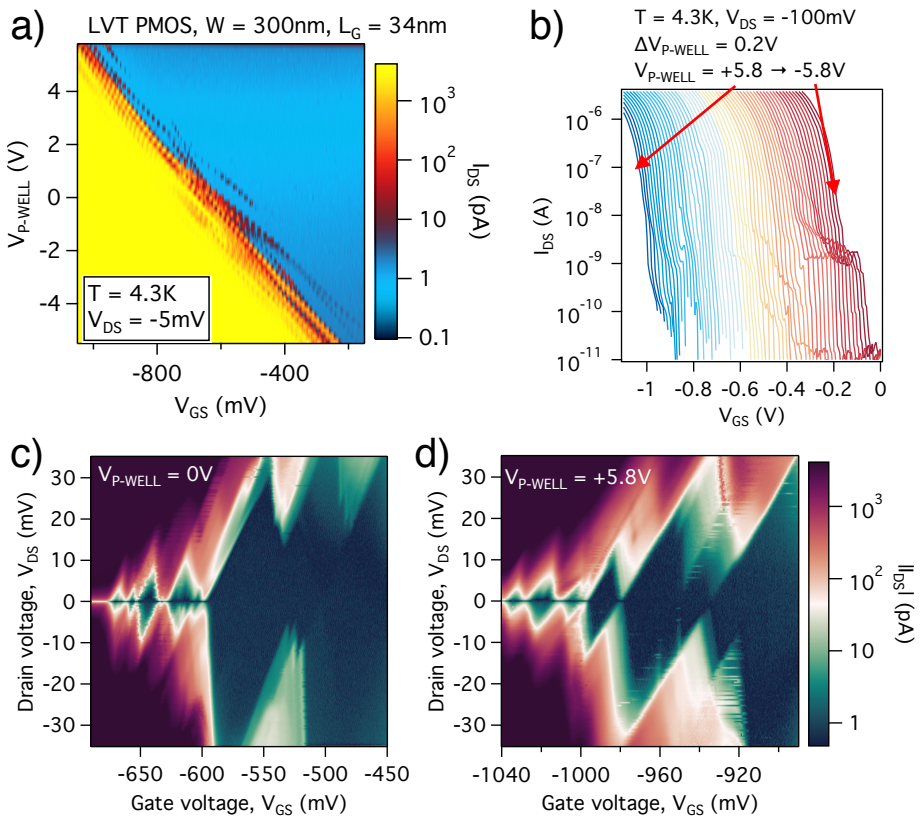


Figure 6.6: LVT PMOS with $L_G = 34$ nm and $W = 300$ nm at 4.3 K (a) Stability diagram $V_{GS} - V_{P-WELL}$ recorded at $V_{DS} = -5$ mV. (b) Transfer characteristics under different body-biasing at $V_{DS} = -100$ mV of the same device as shown in (a). Strong non-idealities in the subthreshold region can be observed. (c) Coulomb spectroscopy at $V_{P-WELL} = 0$ V revealing irregular diamonds as well as huge E_{ADD} of $30 - 50$ meV for the first holes which are consistent with the confinement on clusters of boron mixed with surface states as discussed in Chapter 2. (d) The first holes observation at strong RBB.

confirms that such transistors can be used for a robust digital cryoelectronics circuit working at ultra-low supply voltages.

1.4 K stability diagrams for PMOS transistors with $L_G = 46$ nm and $W = 80$ nm and 300 nm are respectively shown in Fig.6.8 (a - b). Here, for a relaxed L_G, we do not see additional states appearing under body-biasing. Moreover, comparing to NMOS devices, here the resonant peaks corresponding to the first holes are in the form of doublets. Such behavior of quantum dots can be understood from Fig.6.8 (c). Indeed, for $E_{ORB} > E_C$,

the first two holes are added on the same orbital paying the corresponding charging energy. However, to add an additional hole, one need to take into account the additional orbital spacing contribution [77].

The PMOS quantum dots parameters extracted from Fig.6.8 (d - e) are summarised in Table 6.2.

W(nm)	C_{OX}(aF)	C_G(aF)	E_{ORB}(meV)	E_C(meV)
80	74.7	7.7	20.9	7.1
300	280	8.2	19.6	3.9

Table 6.2: 1.4 K quantum dots parameters for two PMOS samples with $W = 80$ nm and 300 nm and $L_G = 46$ nm at $V_{N-WELL} = 0.8$ V. $\alpha = 0.75$ is used for the voltage-to-energy conversion.

Given that we did not perform $V_{GS} - V_{DS}$ measurements to extract the lever arm parameter, herein we used a typical value observed in NMOS devices $\alpha = 0.75$ for the voltage-to-energy conversion. Basing on the estimated orbital spacing, we can estimate the 2D size of p-type QDs using C_G. It leads to 20×20 nm^2 and 19.4×19.4 nm^2 for respectively $W = 80$ nm and $W = 300$ nm. Note the relative size deduced from the energy level spacing, is similar for both n- and p-type QDs. It is worth mentioning that $E_{ORB} = 20.9$ meV is almost the same as the one observed for the first holes in a p-type SOI nanowire QDs reported in [93]. However, for the QDs

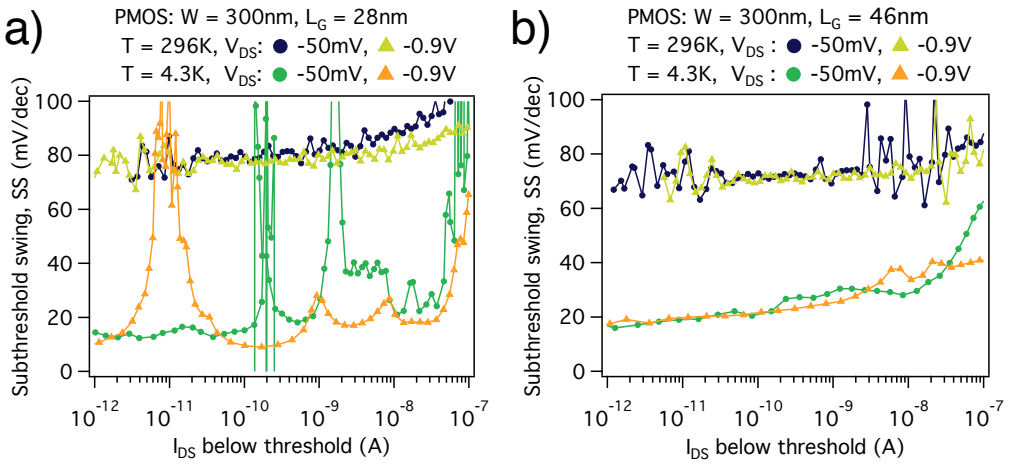


Figure 6.7: Comparison the subthreshold swing for PMOS with $L_G = 28$ nm (a) and $L_G = 46$ nm (b) at zero body biasing using the $SS - I_{DS}$ metric.

defined in the undoped nanowire, the geometrical dimensions were only $L_G = 25$ nm and $W = 10$ nm. Therefore, the reason for such enhanced quantum confinement in PMOS samples remains unclear. Recently, low temperature characterization of a p-type Si MOS structure with two levels of gates was reported in the first hole regime [40]. $E_{ADD} = 12$ meV and $\alpha = 0.17$ were found for the first additional hole.

Finally, both p-type and n-type quantum dots observed in relatively wide FD-SOI transistors are characterized by an excellent tunability under

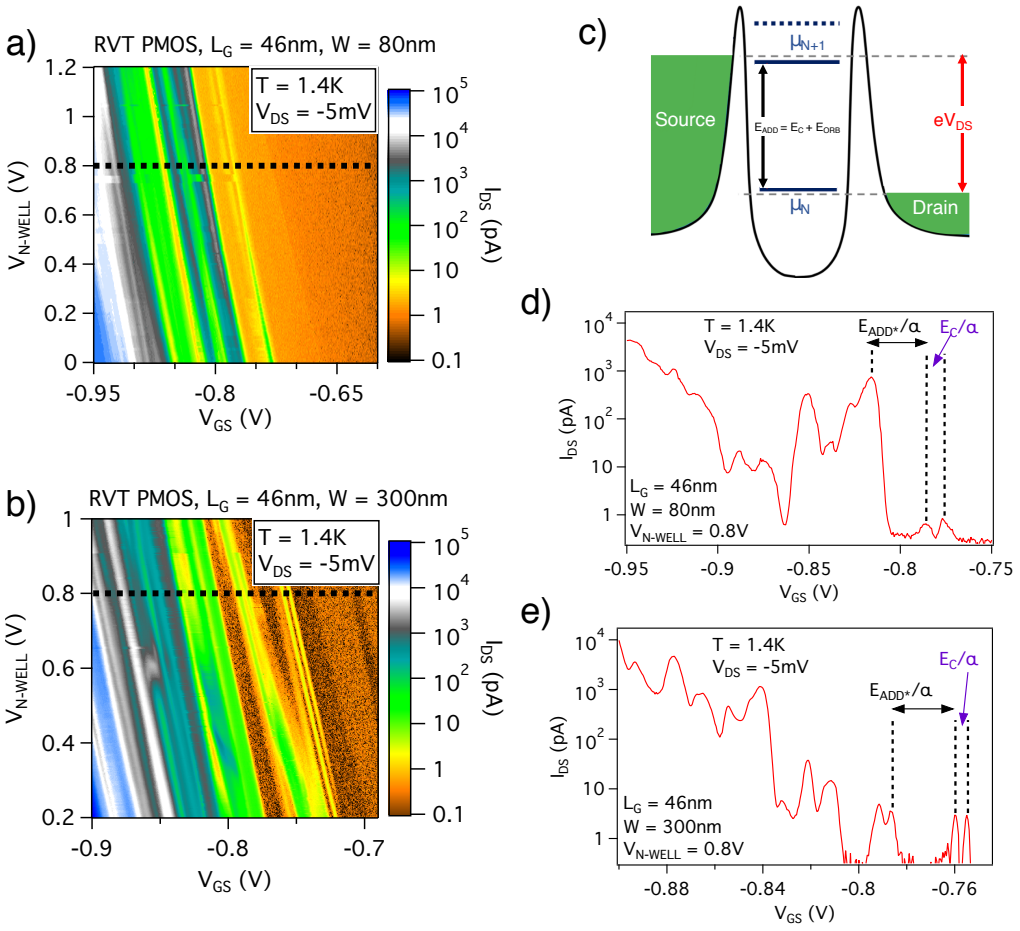


Figure 6.8: Stability diagrams for RVT PMOS transistors with $L_G = 46$ nm and $W = 80$ nm (a) and $W = 300$ nm (b) recorded at 1.4 K. (c) The p-type QD energy spectrum which explains the peak doublets observed for both devices. (d), (e) Coulomb oscillations for the first holes from the cuts shown with black dashed line in (a - b). Note that the energies and voltages are related through the level arm parameter.

body-biasing, surprisingly high addition energy, and very small size as compared to the lithography defined geometry. A statistical characterization over many NMOS and PMOS devices of the same dimensions is still necessary to understand the nature of such confinement in FD-SOI transistors.

6.6 Towards FD-SOI based circuits with quantum devices

A cryogenic hybrid circuit combining a ring oscillator and an SET fabricated using Leti's SOI nanowire has already been demonstrated at 1.1 K [181]. In this circuit, the finite DC current flowing through SET when the AC signal from the RO was sent to the SET was observed. Following the low-temperature characterization of isolated FD-SOI transistors presented in Chapter 3 and having observed an excellent cryogenic performance of ROs in Chapter 5, a first prototype to validate the use of FD-SOI analog and mixed-signal circuits for quantum device control was designed by L. Le Guevel. The schematic of a typical cryo-circuit is shown in Fig.6.9.

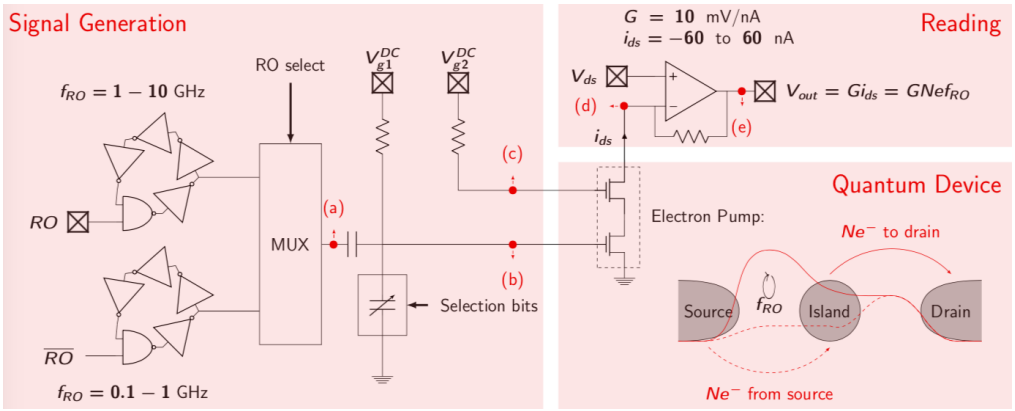


Figure 6.9: On-chip analog and mixed signal circuits for quantum device control (electron pump) fabricated with standard 28 nm FD-SOI technology. High and/or low-frequency AC signals from ROs are send to the multiplexor and then depending on the capacitive divider to the electron pump. The quantum device consists of two SETs tunable with the RF signal. Then, the read-out is performed with a cryogenic TIA. Taken from [210]

By measuring this circuit, DC/AC control of an electron pump composed of two gates in series (L_G = 40 nm with heavily doped integrate

spacing 136 nm) will be soon performed. Electron pump is typically a device which consists of two SETs (with metallic-like equidistant spectrum) connected in series and controlled with RF signals [211]. Such devices have been widely fabricated and characterized at low temperature in order to better define the fundamental value of Ampere for metrology needs [212, 213]. In addition, cryogenic measurements of several important devices such as the variable capacitive divider and the transimpedance amplifier fabricated using FD-SOI technology will allow us to validate the cryogenic operation of hybrid circuits containing both cryoelectronics and quantum devices. Another probable follow-up of the on-going work based on the results presented in this thesis will be to modify/decrease the intergate spacing (using either an additional e-beam lithography or advanced patterning techniques) in order to create two quantum dots in series. Then, it will be possible to perform a qubit experiment using industrial-level FD-SOI devices as it was done for the first CMOS hole spin qubit in [26].

6.7 Conclusions

The main conclusion of this chapter is that standard 28 nm FD-SOI transistors can host very small quantum dots at cryogenic temperature when drain voltages are sufficiently lowered. Indeed, we demonstrated the FET-to-SET transition for both N- and PMOS short-channel devices.

For the case of short-channel NMOS devices , large addition energies for the first electrons are found : $E_{ADD-1} = 19.5$ meV and $E_{ADD-1} = 15.9$ meV for the samples with $W = 210$ nm and $L_G = 28$ nm and 34 nm respectively. Similarly, for the PMOS devices we observed $E_{ORB} = 20.9$ and 19.6 meV for the first holes in samples with $L_G = 46$ nm and $W = 80$ nm and 300 nm, respectively. Moreover, we have shown an excellent gate control with the lever arm parameter $\alpha = 0.75 - 0.8$ deduced from the Coulomb diamonds.

By analyzing NMOS devices with different L_G under forward and reverse body biasing, For the case of $L_G = 34$ nm, we demonstrated that the effect of quantum confinement can be highly decreased and thus, when V_{DS} was increased to 100 mV, we showed a close-to-ideal subthreshold behaviour which is fully suitable for ultralow-power cryogenic electronics as discussed in Chapter 5. However, it was found that using the shorter $L_G = 28$ nm and forward body biasing and, thus pushing the electron wavefunction toward the back interface, will result in new complex states most probably due to the coupling to disordered source/drain regions. We suggest that further modeling can bring more light on the nature of such enhanced quantum confinement at cryogenic temperature and low bias voltages.

For short-channel PMOS transistors, the effect of boron diffusion For the p-type device with $L_G = 34$ nm, Furthermore, the addition energies exceeding $30 - 40$ meV were extracted in the few holes regimes. We could relate these states to the boron clusters mixed with disorder as discussed in Chapter 2. Finally, a proposed solution to achieve both FETs and SETs for PMOS can be to slightly increase the gate length. Indeed, at $L_G = 46$ nm both regular quantum dot states and very stable subthreshold FET-behaviour already at $V_{DS} = -50$ mV were observed.

The 2D size of both p- and n-type quantum dots estimated from C_G has been found to be much lower than C_{OX} imposed by the geometrical consideration. Whereas the reason for such enhanced quantum confinement in standard FD-SOI transistors remains unclear, the possibility to co-integrate CryoCMOS and qubits on the same FD-SOI platform seems to be very advantageous for large-scale silicon quantum computing.

We concluded the chapter by presenting recently designed on-chip analog and mixed-signal circuits for quantum device control (electron pump) fabricated with standard 28 nm FD-SOI technology.

Chapter 7

General conclusions and Perspectives

In this thesis, two major axes of quantum computing research are considered. First, we studied different types of quantum dots using close-to-industrial Leti's nanowire technology and the 28nm FD-SOI planar technology from the perspective of silicon quantum computing. Second, the potential of 28 nm FD-SOI technology for CryoCMOS was investigated.

In Chapter 1, we discussed the choice and the advantages of CMOS-compatible technologies for building large qubit systems. It was shown that within the paradigm of electron spin qubit driven by EDSR, a special design corner dots must be realized. Finally, the importance of cryogenic electronics to efficiently drive qubits is emphasized.

Main results from Chapter 2 are the following. The Pauli Spin Blockade in the few holes regime is demonstrated in a p-type double gate device governed by strong spin-orbit coupling with a small intradot spin relaxation rate (limiting T_1) of 120 kHz for the (1,3)→(2,2) transition. Then, as the hole spin qubit performance is impacted by the closeness of Source/Drain regions, a p-type device with four gates was used to efficiently tune the access barriers of a double quantum dot. It can improve the coherence times of the hole spin qubit by electrostatically decoupling the DQD used for the qubit from the metallic leads. Regarding electron QDs, we extensively study QDs under different body-biasing conditions. In the weak coupling regime under zero V_{BACK} or RBB, we find that the experimental addition energies describing the relative size of QDs (up to 25 meV for the first additional electron) can be obtained by realistic electrostatic simulation without any disorder. For the FBB regime, we have found that depending on the channel doping, a DQD in series can be obtained due to the cluster of dopants. Finally, we have shown that either a CD or a DQD in series can be obtained

in a geometry with two F-to-F gates and two access gates. It was demonstrated that depending on the access barrier voltages, either a semi-metallic island or quantum dot can be accumulated below the access barriers. The promising results obtained from transport measurements serve as a basis for using this geometry to demonstrate a two-electron spin qubit gate in the future experiments.

The outcomes of the digital and analog performance analysis of 28 nm FD-SOI MOSFETs down to 4 K have shown to be of great potential for cryogenic electronics applications. First, we have found that at low temperature the currents above V_{TH} are greatly increased due to the mobility enhancement even for $L_G = 28$ nm for both NMOS and PMOS. In terms of electrostatic control, it was demonstrated that this technology not only offers the best $SS - I_{DS}$ characteristics below V_{TH} but it also provides the capability to compensate the cryogenic V_{TH}-shift by keeping $V_{TH}(T) = V_{TH}(296K)$. By comparing the same long-channel PMOS device with and without channel doping, we argued that in terms of variability, the $SS - I_{DS}$ metric, the effective mobility and the V_{TH}-shift, it is crucial to keep an undoped channel. Then, long-channel device variability has been discussed. We have shown that the 4 K variability is comparable to room temperature and that almost identical $SS_{LIN,SAT} - I_{DS}$ were measured over 5 samples. In-depth analysis of the V_{TH}-shift on short-channel devices together with the measurement of the access resistance, revealed that the saturation in the $V_{TH}(T)$ dependence is probably due to a partial freeze-out of low doping LDD Source/Drain regions. However, it was shown that the normalized overdrive current I_{ODSAT}/W is the same for NMOS and PMOS with W ranging between 80 nm and 1 µm. By analyzing the $I_{ODLIN}(L_G/W)$ (proportional to the low field mobility) for the case of shortest $L_G = 28$ nm down to 4 K, a 4.3 K gain compared to 296 K of approximatively +45% for NMOS and +63% for PMOS devices was found. Also, it was shown that an efficient body-biasing capability is kept down to 4 K and the body-biasing window is greatly enlarged. Finally, by addressing the cryogenic analog performance using the key parameters such as the transconductance G_M, the output conductance G_D and the intrinsic gain $A_{v0} = G_M/G_D$, we have shown a great potential of 28 nm FD-SOI technology for both base-band applications (requiring high precision and low currents) and high frequency applications (where high gain and currents are needed). As a possible follow-up of this section, more variability analysis should be done on a larger amount of samples and the role of high-κ dielectric in the gate stack (introducing additional RCS and SPS) on the stability of $SS - I_{DS}$ characteristics should be clarified. Moreover, the low-temperature study of noise and the dynamic measurements have to

be performed in order to be able to design an efficient cryogenic circuit.

In Chapter 4, we have developed a physics-based model explaining the low-temperature saturation of $SS(T)$ below typically 35 K. By introducing a narrow 3 meV tail at the edges of the conduction and valence bands and using the Fermi-Dirac statistics, we have well reproduced the saturation of $SS(T)$ from the experiment. Although SS values dropping down to $7-10$ meV were observed at 4 K which already presents great improvements in $SS-I_{DS}$, we were able, for the first time, to explain the low-temperature behavior of the subthreshold current over more than 6 decades in FD-SOI transistors. By analyzing the $SS-I_{DS}$ metric under different FBB conditions, we have argued that the increased density of interface traps cannot be responsible for the $SS(T)$ saturation. The DTMOS operation of short-channel devices has shown that even lower SS can be obtained reaching less than 3 mV/dec over more than four decades. Finally, by introducing a slight exponential variation in the interface trap density by typically $10-20\%$, we could qualitatively reproduce the $SS-I_{DS}$ behavior thus paving a way for an efficient cryogenic design of CryoCMOS. In the future, the developed model should be adapted to deal with the saturation of $V_{TH}(T)$ in short-channel devices.

Regarding the cryogenic performance of ROs down to 4 K, it was shown that the optimal supply voltage can be reduced down to 0.3 V thereby reducing the dynamic and static power dissipations. At the same time, a small Energy-Delay product of 6.9 fJ×ps with $\tau_P = 37$ ps were achieved at $V_{DD} = 0.325$ V under aggressive FBB. Moreover, we could correlate the behavior of isolated transistors to that of RO down 4.3 K and thus conclude that the load capacitance of a single inverter is only weakly dependent on temperature. Additionally, the variability issues of short-channel transistors in terms of V_{TH} variations were discussed. It was shown that despite a stronger $V_{TH-PMOS}$-variability at 4.3 K, it is still possible to achieve an effective RO power management in the close-to-zero-V_{TH} mode of operation. Finally, the absence of hysteresis loops when operating the transistor with V_{BACK} at a high sweeping rate at 4 K and the thermal budget constraint led us to the conclusion that the optimal temperature for 28 nm FD-SOI cryo-electronics will be probably close to 4 K to limit the freeze-out of backplane doping. The next logical step after having analyzed the isolated transistor performance and ROs down to 4 K would be to measure other basic circuits such as SRAM and analyzing the device circuit variability. Moreover, the power dissipation limits for the 4 K should be precisely quantified.

Finally, in the last chapter, we have demonstrated the duality of short-channel FD-SOI transistors operation as FETs or SETs depending on V_{DS} and V_{BACK} at 4 K. Although the exact mechanism of the electrostatic con-

finement in channel-wide ($200 - 300$ nm) still needs to be further investigated, very stable and high-E_{ADD} (up to 20 meV) electron QDs were reported in the planar FD-SOI devices. By benchmarking these QDs with respect to the common Si-platforms, we have shown that 28 nm FD-SOI technology has a great potential for qubits. Indeed, it would be of great importance for scalable quantum computing to have both CryoCMOS and qubits designed within the same technological platform and then fabricated on 300 mm wafers as a single circuit. The role of enhanced boron diffusion from S/D regions on the short-channel device stability in the subthreshold regime was explained with Coulomb spectroscopy at 4 K. In this case, we have shown that the first holes are most likely to be confined on dopants for the shortest $L_G = 28$ nm which can be problematic for both SET and FET operations. Then, by relaxing L_G to 46 nm, we have demonstrated that a stable $SS - I_{DS}$ behavior can be achieved and electrostatically confined hole QDs are found when V_{DS} is reduced to 20 mV. Finally, as a future work towards the co-integration, we presented a prototype design for electron pumps driven with ROs and read-out with a cryogenic transimpedence amplifier within the same technological platform. If a small intergate pitch ($30-40$ nm) between two gates in series can be achieved either using e-beam lithography, EUV or advanced gate patterning, a similar circuit containing 'qubits + CryoCMOS' can potentially be realized using the 28 nm FD-SOI technology.

References

[1] R. P. Feynman. Simulating physics with computers. *International Journal of Theoretical Physics*, **21** 467, 1982.

[2] M. Bhushan and M. B. Ketchen. *CMOS Test and Evaluation: A Physical Perspective*. Springer-Verlag New York, 2015.

[3] M. A. Nielsen and I. L. Chuang. *Quantum Computation and Quantum Information: 10th Anniversary Edition*. Cambridge University Press, 2011.

[4] A. Montanaro. Quantum algorithms: an overview. *Npj Quantum Information*, **2** 15023, 2016.

[5] P. W. Shor. Polynomial-time algorithms for prime factorization and discrete logarithms on a quantum computer. *SIAM J. Comput.*, **26** 1484, 1997.

[6] J. P. Buhler, H. W. Lenstra, and C. Pomerance. Factoring integers with the number field sieve. In A. K. Lenstra and H. W. Lenstra, eds., *The development of the number field sieve*, pp. 50–94. Springer Berlin Heidelberg, Berlin, Heidelberg, 1993.

[7] L. Grover. Quantum mechanics help in searching a needle in a haystack. *Phys. Rev. Lett. 79, 325-328*, 1997.

[8] M. B. Hastings, D. Wecker, B. Bauer, and M. Troyer. Improving quantum algorithms for quantum chemistry. *Quantum Info. Comput.*, **15** 1, 2015.

[9] S. Jordan, K. Lee, and J. Preskill. Quantum algorithms for quantum field theories. *Science 336, 1130-1133*, 2012.

[10] A. W. Harrow, A. Hassidim, and S. Lloyd. Quantum algorithm for linear systems of equations. *PRL*, **103** 150502, 2009.

[11] D. W. Berry. High-order quantum algorithm for solving linear differential equations. *Journal of Physics A: Mathematical and Theoretical*, **47** 105301, 2014.

[12] N. Wiebe, D. Braun, and S. Lloyd. Quantum algorithm for data fitting. *Phys. Rev. Lett.*, **109** 050505, 2012.

[13] S. Aaronson. Read the fine print. *Nature Physics*, **11** 291, 2015.

[14] D. J. Reilly. Engineering the quantum-classical interface of solid-state qubits. *Npj Quantum Information*, **1** 15011, 2015.

[15] D. P. DiVincenzo. The physical implementation of quantum computation. *Fortshritte der Physik 48, 771-783*, 2000.

[16] M. H. Devoret and R. J. Schoelkopf. Superconducting circuits for quantum information: An outlook. *Science*, **339** 1169, 2013.

[17] J. M. Gambetta, J. M. Chow, and M. Steffen. Building logical qubits in a superconducting quantum computing system. *npj Quantum Information*, **3** 2, 2017.

[18] J. R. Petta, A. C. Johnson, J. M. Taylor, E. A. Laird, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hanson, and A. C. Gossard. Coherent manipulation of coupled electron spins in semiconductor quantum dots. *Science*, **309** 2180, 2005.

[19] E. A. Chekhovich, M. N. Makhonin, A. I. Tartakovskii, A. Yacoby, H. Bluhm, K. C. Nowack, and L. M. K. Vandersypen. Nuclear spin effects in semiconductor quantum dots. *Nature Materials*, **12** 494, 2013.

[20] L. M. K. Vandersypen, H. Bluhm, J. S. Clarke, A. S. Dzurak, R. Ishihara, A. Morello, D. J. Reilly, L. R. Schreiber, and M. Veldhorst. Interfacing spin qubits in quantum dots and donors–hot, dense, and coherent. *npj Quantum Information*, **3** 34, 2017.

[21] J. R. Petta, A. C. Johnson, C. M. Marcus, M. P. Hanson, and A. C. Gossard. Manipulation of a single charge in a double quantum dot. *PRL*, **93** 186802, 2004.

[22] M. Veldhorst, J. C. C. Hwang, C. H. Yang, A. W. Leenstra, B. de Ronde, J. P. Dehollain, J. T. Muhonen, F. E. Hudson, K. M. Itoh, A. Morello, and A. S. Dzurak. An addressable quantum dot

qubit with fault-tolerant control-fidelity. *Nature Nanotechnology*, **9** 981, 2014.

[23] M. Veldhorst, C. H. Yang, J. C. C. Hwang, W. Huang, J. P. Dehollain, J. T. Muhonen, S. Simmons, A. Laucht, F. E. Hudson, K. M. Itoh, A. Morello, and A. S. Dzurak. A two-qubit logic gate in silicon. *Nature*, **526** 410, 2015.

[24] J. Yoneda, K. Takeda, T. Otsuka, T. Nakajima, M. R. Delbecq, G. Allison, T. Honda, T. Kodera, S. Oda, Y. Hoshi, N. Usami, K. M. Itoh, and S. Tarucha. A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9 %. *Nature Nanotechnology*, **13** 102, 2018.

[25] D. Loss and D. P. DiVincenzo. Quantum computation with quantum dots. *PRA*, **57** 120, 1998.

[26] R. Maurand, X. Jehl, D. Kotekar-Patil, A. Corna, Bohuslavskyi, H., R. Laviéville, L. Hutin, S. Barraud, M. Vinet, M. Sanquer, and S. De Franceschi. A cmos silicon spin qubit. *Nature Communications*, **7** 13575, 2016.

[27] A. Corna, L. Bourdet, R. Maurand, A. Crippa, D. Kotekar-Patil, Bohuslavskyi, H., R. Laviéville, L. Hutin, S. Barraud, X. Jehl, M. Vinet, S. De Franceschi, Y.-M. Niquet, and M. Sanquer. Electrically driven electron spin resonance mediated by spin-valley-orbit coupling in a silicon quantum dot. *Npj Quantum Information*, **4** 6, 2018.

[28] J. Levy. Universal quantum computation with spin-1/2 pairs and heisenberg exchange. *PRL*, **89** 147902, 2002.

[29] D. P. DiVincenzo, D. Bacon, J. Kempe, G. Burkard, and K. B. Whaley. Universal quantum computation with the exchange interaction. *Nature*, **408** 339, 2000.

[30] Z. Shi, C. B. Simmons, J. R. Prance, J. K. Gamble, T. S. Koh, Y.-P. Shim, X. Hu, D. E. Savage, M. G. Lagally, M. A. Eriksson, M. Friesen, and S. N. Coppersmith. Fast hybrid silicon double-quantum-dot qubit. *Phys. Rev. Lett.*, **108** 140503, 2012.

[31] L. Hutin, L. Bourdet, B. Bertrand, A. Corna, Bohuslavskyi, H., A. Amisse, A. Crippa, R. Maurand, S. Barraud, M. Urdampilleta,

C. Bäuerle, T. Meunier, M. Sanquer, X. Jehl, S. De Franceschi, Y.-M. Niquet, and M. Vinet. All-electrical control of a hybrid electron spin/valley quantum bit in soi cmos technology. *IEEE Transactions on Electron Devices*, **65** 5151 , 2018.

[32] D. Castelvecchi. Silicon gains ground in quantum-computing race. *Nature news*, 10 January 2018.

[33] E. Kawakami, P. Scarlino, D. R. Ward, F. R. Braakman, D. E. Savage, M. G. Lagally, M. Friesen, S. N. Coppersmith, M. A. Eriksson, and L. M. K. Vandersypen. Electrical control of a long-lived spin qubit in a si/sige quantum dot. *Nature Nanotechnology*, **9** 666, 2014.

[34] J. T. Muhonen, J. P. Dehollain, A. Laucht, F. E. Hudson, R. Kalra, T. Sekiguchi, K. M. Itoh, D. N. Jamieson, J. C. McCallum, A. S. Dzurak, and A. Morello. Storing quantum information for 30 seconds in a nanoelectronic device. *Nature Nanotechnology*, **9** 986, 2014.

[35] L. R. Schreiber and H. Bluhm. Silicon comes back. *Nature Nanotechnology*, **9** 966, 2014.

[36] S. Barraud, R. Coquand, M. Casse, M. Koyama, J. . Hartmann, V. Maffini-Alvaro, C. Comboroure, C. Vizioz, F. Aussenac, O. Faynot, and T. Poiroux. Performance of omega-shaped-gate silicon nanowire mosfet with diameter down to 8 nm. *IEEE Electron Device Letters*, **33** 1526, 2012.

[37] N. S. Lai, W. H. Lim, C. H. Yang, F. A. Zwanenburg, W. A. Coish, F. Qassemi, A. Morello, and A. S. Dzurak. Pauli spin blockade in a highly tunable silicon double quantum dot. *Scientific Reports*, **1** 110, 2011.

[38] Bohuslavskyi, H., D. Kotekar-Patil, R. Maurand, A. Corna, S. Barraud, L. Bourdet, L. Hutin, Y.-M. Niquet, X. Jehl, S. De Franceschi, M. Vinet, and M. Sanquer. Pauli blockade in a few-hole pmos double quantum dot limited by spin-orbit interaction. *Applied Physics Letters*, **109** 193101, 2016.

[39] B. Voisin, R. Maurand, S. Barraud, M. Vinet, X. Jehl, M. Sanquer, J. Renard, and S. De Franceschi. Electrical control of g-factor in a few-hole silicon nanowire mosfet. *Nano Lett.*, **16** 88, 2016.

[40] S. D. Liles, R. Li, C. H. Yang, F. E. Hudson, M. Veldhorst, A. S. Dzurak, and A. R. Hamilton. Spin and orbital structure of the first

six holes in a silicon metal-oxide-semiconductor quantum dot. *Nature Communications*, **9** 3255, 2018.

[41] L. Bourdet and Y.-M. Niquet. All-electrical manipulation of silicon spin qubits with tunable spin-valley mixing. *PRB*, **97** 155433, 2018.

[42] D. J. Ibberson, L. Bourdet, J. C. Abadillo-Uriel, I. Ahmed, S. Barraud, M. J. Calderón, Y.-M. Niquet, and M. F. Gonzalez-Zalba. Electric-field tuning of the valley splitting in silicon corner dots. *Appl. Phys. Lett.*, **113** 053104, 2018.

[43] A. Corna. *Single spin control and readout in silicon coupled quantum dots*. Ph.D. thesis, CEA-INAC, University of Grenoble, 2017.

[44] D. M. Zajac, A. J. Sigillito, M. Russ, F. Borjans, J. M. Taylor, G. Burkard, and J. R. Petta. Resonantly driven cnot gate for electron spins. *Science*, **359** 439, 2018.

[45] S. Schaal, A. Rossi, S. Barraud, J. J. L. Morton, and M. F. Gonzalez-Zalba. A cmos dynamic random access architecture for radio-frequency readout of quantum devices. *arXiv:1809.03894v1 [cond-mat.mes-hall]*, 2018.

[46] J. M. Martinis. Qubit metrology for building a fault-tolerant quantum computer. *Npj Quantum Information*, **1** 15005, 2015.

[47] A. Crippa, R. Maurand, D. Kotekar-Patil, A. Corna, Bohuslavskyi, H., A. O. Orlov, P. Fay, R. Lavieville, S. Barraud, M. Vinet, M. Sanquer, S. De Franceschi, and X. Jehl. Level spectrum and charge relaxation in a silicon double quantum dot probed by dual-gate reflectometry. *Nano Letters*, **17** 1001, 2017.

[48] A. West, B. Hensen, A. Jouan, T. Tanttu, C. H. Yang, A. Rossi, M. F. Gonzalez-Zalba, F. E. Hudson, M. Morello, D. J. Reilly, and A. S. Dzurak. Gate-based single-shot readout of spins in silicon. *arXiv:1809.01864v1 [quant-ph]*, 2018.

[49] P. Pakkiam, A. V. Timofeev, M. G. House, M. R. Hogg, T. Kobayashi, M. Koch, S. Rogge, and M. Simmons. Single-shot single-gate rf spin readout in silicon. *arXiv:1809.01802v1 [cond-mat.mes-hall]*, 2018.

[50] M. Urdampilleta, D. J. Niegemann, E. Chanrion, B. Jadot, C. Spence, P. A. Mortemousque, C. Bäuerle, L. Hutin, B. Bertrand, S. Barraud, R. Maurand, M. Sanquer, X. Jehl, S. D. Franceschi, M. Vinet, and

T. Meunier. Gate-based high fidelity spin read-out in a cmos device. *arXiv:1809.04584v1 [cond-mat.mes-hall]*, 2018.

[51] S. J. Devitt, W. J. Munro, and K. Nemoto. Quantum error correction for beginners. *Reports on Progress in Physics*, **76** 076001, 2013.

[52] B. M. Terhal. Quantum error correction for quantum memories. *Rev. Mod. Phys.*, **87** 307, 2015.

[53] D. Wecker, B. Bauer, B. K. Clark, M. B. Hastings, and M. Troyer. Gate-count estimates for performing quantum chemistry on small quantum computers. *Phys. Rev. A*, **90** 022305, 2014.

[54] R. Van Meter and C. Horsman. A blueprint for building a quantum computer. *Commun. ACM*, **56** 84, 2013.

[55] A. R. Mills, D. M. Zajac, M. J. Gullans, F. J. Schupp, T. M. Hazard, and J. R. Petta. Shuttling a single charge across a one-dimensional array of silicon quantum dots. *arXiv:1809.03976v1 [cond-mat.mes-hall]*, 2018.

[56] D. M. Zajac, T. M. Hazard, X. Mi, E. Nielsen, and J. R. Petta. Scalable gate architecture for a one-dimensional array of semiconductor spin qubits. *PRAPPLIED*, **6** 054013, 2016.

[57] https://spectrum.ieee.org/semiconductors/nanotechnology/euv-lithography-finally-ready-for-chip-manufacturing.

[58] L. Hutin, B. Bertrand, R. Maurand, M. Urdampilleta, B. Jadot, Bohuslavskyi, H., L. Bourdet, Y. . Niquet, X. Jehl, S. Barraud, C. Bäuerle, T. Meunier, M. Sanquer, S. D. Franceschi, and M. Vinet. Soi cmos technology for quantum information processing. In *IEEE International Conference on IC Design and Technology*, pp. 1–4. 2017.

[59] V. Mazzocchi, P. G. Sennikov, A. D. Bulanov, M. F. Churbanov, B. Bertrand, L. Hutin, J. P. Barnes, M. N. Drozdov, J. M. Hartmann, and M. Sanquer. 99.992integration of silicon spin qubits. *arXiv:1807.04968v1 [cond-mat.mtrl-sci]*, 2018.

[60] K. Takeda, J. Kamioka, T. Otsuka, J. Yoneda, T. Nakajima, M. R. Delbecq, S. Amaha, G. Allison, T. Kodera, S. Oda, and S. Tarucha. A fault-tolerant addressable spin qubit in a natural silicon quantum dot. *Sci Adv*, **2**, 2016.

[61] L. Petit, J. M. Boter, H. G. J. Eenink, G. Droulers, M. L. V. Tagliaferri, R. Li, D. P. Franke, J. Singh, J. S. K. J. Clarke, R. N. Schouten, V. V. Dobrovitski, L. M. K. Vandersypen, and M. Veldhorst. Spin lifetime and charge noise in hot silicon quantum dot qubits. *arXiv:1803.01774v2 [cond-mat.mes-hall]*, 2018.

[62] N. Samkharadze, G. Zheng, N. Kalhor, D. Brousse, A. Sammak, U. C. Mendes, A. Blais, G. Scappucci, and L. M. K. Vandersypen. Strong spin-photon coupling in silicon. *Science*, 2018.

[63] A. J. Landig, J. V. Koski, P. Scarlino, U. C. Mendes, A. Blais, C. Reichl, W. Wegscheider, A. Wallraff, K. Ensslin, and T. Ihn. Coherent spin-photon coupling using a resonant exchange qubit. *Nature*, **560** 179, 2018.

[64] X. Mi, M. Benito, S. Putz, D. M. Zajac, J. M. Taylor, G. Burkard, and J. R. Petta. A coherent spin-photon interface in silicon. *Nature*, **555** 599, 2018.

[65] F. K. Malinowski, F. Martins, T. B. Smith, S. B. Bartlett, A. C. Doherty, P. D. Nissen, S. Fallahi, G. S. Gardner, M. J. Manfra, C. M. Marcus, and F. Kuemmeth. Fast spin exchange between two distant quantum dots. *arXiv:1808.09736v1 [cond-mat.mes-hall]*, 2018.

[66] D. P. Franke, J. Clarke, L. Vandersypen, and M. Veldhorst. Rent's rule and extensibility in quantum computing. *arXiv:1806.02145v1 [quant-ph]*, 2018.

[67] E. Charbon, F. Sebastiano, A. Vladimirescu, H. Homulle, S. Visser, L. Song, and R. M. Incandela. Cryo-cmos for quantum computing. In *2016 IEEE International Electron Devices Meeting (IEDM)*, pp. 13.5.1–13.5.4. 2016.

[68] J. M. Hornibrook, J. I. Colless, I. D. Conway Lamb, S. J. Pauka, H. Lu, A. C. Gossard, J. D. Watson, G. C. Gardner, S. Fallahi, M. J. Manfra, and D. J. Reilly. Cryogenic control architecture for large-scale quantum computing. *PRAPPLIED*, **3** 024010, 2015.

[69] S. D. Franceschi, L. Hutin, R. Maurand, L. Bourdet, Bohuslavskyi, H., A. Corna, D. Kotekar-Patil, S. Barraud, X. Jehl, Y. M. Niquet, M. Sanquer, and M. Vinet. Soi technology for quantum information processing. In *IEEE International Electron Devices Meeting*, pp. 13.4.1–13.4.4. 2016.

[70] S. Barraud, R. Lavieville, L. Hutin, Bohuslavskyi, H., M. Vinet, A. Corna, M. Clapera, P.and Sanquer, and X. Jehl. Development of a cmos route for electron pumps to be used in quantum metrology. *Technologies*, **4**, 2016.

[71] Bohuslavskyi, H., S. Barraud, L. Bourdet, A. Crippa, B. Bertrand, A. Amisse, R. Ezzouch, R. Maurand, X. Jehl, B. Jadot, M. Urdampilleta, T. Meunier, C. Bauerle, Y.-M. Niquet, S. D. Franceschi, M. Sanquer, and M. Vinet. Nanowire soi quantum dots with electrostatically controlled tunnel coupling. In *2018 Silicon Nanoelectronics Workshop (SNW), to appear in proceedings*. Honolulu, 2018.

[72] S. Barraud, M. Berthome, R. Coquand, M. Casse, T. Ernst, M. . Samson, P. Perreau, K. K. Bourdelle, O. Faynot, and T. Poiroux. Scaling of trigate junctionless nanowire mosfet with gate length down to 13 nm. *IEEE Electron Device Letters*, **33** 1225, 2013.

[73] M. Casse. *Caracterisation Electrique et Modelisation du Transport dans les Dispositifs CMOS Avances (in french), HDR*. University of Grenoble, 2014.

[74] B. Voisin, V.-H. Nguyen, J. Renard, X. Jehl, S. Barraud, F. Triozon, M. Vinet, I. Duchemin, Y.-M. Niquet, S. de Franceschi, and M. Sanquer. Few-electron edge-state quantum dots in a silicon nanowire field-effect transistor. *Nano Lett.*, **14** 2094, 2014.

[75] P. Harvey-Collard, B. D'Anjou, M. Rudolph, N. T. Jacobson, J. Dominguez, G. A. Ten Eyck, J. R. Wendt, T. Pluym, M. P. Lilly, W. A. Coish, M. Pioro-Ladrière, and M. S. Carroll. High-fidelity single-shot readout for a spin qubit via an enhanced latching mechanism. *PRX*, **8** 021046, 2018.

[76] R. Hanson, L. P. Kouwenhoven, J. R. Petta, S. Tarucha, and L. M. K. Vandersypen. Spins in few-electron quantum dots. *Rev. Mod. Phys.*, **79** 1217, 2007.

[77] F. A. Zwanenburg, A. S. Dzurak, A. Morello, M. Y. Simmons, L. C. L. Hollenberg, G. Klimeck, S. Rogge, S. N. Coppersmith, and M. A. Eriksson. Silicon quantum electronics. *RMP*, **85** 961, 2013.

[78] F. H. L. Koppens, C. Buizert, K. J. Tielrooij, I. T. Vink, K. C. Nowack, T. Meunier, L. P. Kouwenhoven, and L. M. K. Vandersypen. Driven coherent oscillations of a single electron spin in a quantum dot. *Nature*, **442** 766, 2006.

[79] K. C. Nowack, F. H. L. Koppens, Y. V. Nazarov, and L. M. K. Vandersypen. Coherent control of a single electron spin with electric fields. *Science*, **318** 1430, 2007.

[80] F. H. L. Koppens, J. A. Folk, J. M. Elzerman, R. Hanson, L. H. W. van Beveren, I. T. Vink, H. P. Tranitz, W. Wegscheider, L. P. Kouwenhoven, and L. M. K. Vandersypen. Control and detection of singlet-triplet mixing in a random nuclear field. *Science*, **309** 1346, 2005.

[81] F. Qassemi, W. A. Coish, and F. K. Wilhelm. Stationary and transient leakage current in the pauli spin blockade. *Phys. Rev. Lett.*, **102** 176806, 2009.

[82] S. Nadj-Perge, S. M. Frolov, J. W. W. van Tilburg, J. Danon, Y. V. Nazarov, R. Algra, E. P. A. M. Bakkers, and L. P. Kouwenhoven. Disentangling the effects of spin-orbit and hyperfine interactions on spin blockade. *Phys. Rev. B*, **81** 201305, 2010.

[83] J. Danon and Y. V. Nazarov. Pauli spin blockade in the presence of strong spin-orbit coupling. *PRB*, **80** 041301, 2009.

[84] M. Hofheinz. *Coulomb blockade in silicon nanowire MOSFETs*. Ph.D. thesis, CEA-INAC, University of Grenoble, 2006.

[85] S. Nadj-Perge, S. M. Frolov, E. P. A. M. Bakkers, and L. P. Kouwenhoven. Spin-orbit qubit in a semiconductor nanowire. *Nature*, **468** 1084, 2010.

[86] J. W. G. van den Berg, S. Nadj-Perge, V. S. Pribiag, S. R. Plissard, E. P. A. M. Bakkers, S. M. Frolov, and L. P. Kouwenhoven. Fast spin-orbit qubit in an indium antimonide nanowire. *Phys. Rev. Lett.*, **110** 066806, 2013.

[87] H. Bluhm, S. Foletti, I. Neder, M. Rudner, D. Mahalu, V. Umansky, and A. Yacoby. Dephasing time of gaas electron-spin qubits coupled to a nuclear bath exceeding 200us. *Nat. Phys.*, **7** 109, 2011.

[88] G. de Lange, Z. H. Wang, D. Ristè, V. V. Dobrovitski, and R. Hanson. Universal dynamical decoupling of a single solid-state spin from a spin bath. *Science*, **330** 60, 2010.

[89] B. M. Maune, M. G. Borselli, B. Huang, T. D. Ladd, P. W. Deelman, K. S. Holabird, A. A. Kiselev, I. Alvarado-Rodriguez, R. S. Ross, A. E. Schmitz, M. Sokolich, C. A. Watson, M. F. Gyure, and A. T.

Hunter. Coherent singlet-triplet oscillations in a silicon-based double quantum dot. *Nature*, **481** 344, 2012.

[90] X. Wu, D. R. Ward, J. R. Prance, D. Kim, J. K. Gamble, R. T. Mohr, Z. Shi, D. E. Savage, M. G. Lagally, M. Friesen, S. N. Coppersmith, and M. A. Eriksson. Two-axis control of a singlet-triplet qubit with an integrated micromagnet. *Proc. Natl. Acad. Sci.*, **111** 11938, 2014.

[91] C. Testelin, F. Bernardot, B. Eble, and M. Chamarro. Hole-spin dephasing time associated with hyperfine interaction in quantum dots. *Phys. Rev. B*, **79** 195440, 2009.

[92] R. Li, F. E. Hudson, A. S. Dzurak, and A. R. Hamilton. Pauli spin blockade of heavy holes in a silicon double quantum dot. *Nano Lett.*, **15** 7314, 2015.

[93] B. Voisin, R. Maurand, S. Barraud, M. Vinet, X. Jehl, M. Sanquer, J. Renard, and S. De Franceschi. Electrical control of g-factor in a few-hole silicon nanowire mosfet. *Nano Lett.*, **16** 88, 2016.

[94] D. Kotekar-Patil, A. Corna, R. Maurand, A. Crippa, A. Orlov, S. Barraud, L. Hutin, M. Vinet, X. Jehl, S. De Franceschi, and M. Sanquer. Pauli spin blockade in cmos double quantum dot devices. *Phys. Status Solidi B*, **254** 1600581, 2016.

[95] W. G. van der Wiel, S. De Franceschi, J. M. Elzerman, T. Fujisawa, S. Tarucha, and L. P. Kouwenhoven. Electron transport through double quantum dots. *Rev. Mod. Phys.*, **75** 1, 2002.

[96] V. N. Golovach, X. Jehl, M. Houzet, M. Pierre, B. Roche, M. Sanquer, and L. I. Glazman. Single-dopant resonance in a single-electron transistor. *Phys. Rev. B*, **83** 075401, 2011.

[97] Y. M. Niquet, D. Rideau, C. Tavernier, H. Jaouen, and X. Blase. Onsite matrix elements of the tight-binding hamiltonian of a strained crystal: Application to silicon, germanium, and their alloys. *PRB*, **79** 245201, 2009.

[98] M. Pierre, M. Hofheinz, X. Jehl, M. Sanquer, G. Molas, M. Vinet, and S. Deleonibus. Background charges and quantum effects in quantum dots transport spectroscopy. *Eur. Phys. J. B*, **70** 475, 2009.

[99] K. Ono, D. G. Austing, Y. Tokura, and S. Tarucha. Current rectification by pauli exclusion in a weakly coupled double quantum dots system. *Science*, **297** 1313, 2002.

[100] G. Yamahata, T. Kodera, H. O. H. Churchill, K. Uchida, C. M. Marcus, and S. Oda. Magnetic field dependence of pauli spin blockade: A window into the sources of spin relaxation in silicon qunatum dots. *Phys. Rev. B*, **86** 115322, 2012.

[101] A. Pfund, I. Shorubalko, K. Ensslin, and R. Leturcq. Suppression of spin relaxation in an inas nanowire double quantum dot. *Phys. Rev. Lett.*, **99** 036801, 2007.

[102] S. V. Pribiag, S. Nadj-Perge, S. M. Frolov, J. W. G. van den Berg, I. van Weperen, S. R. Plissard, E. P. A. M. Bakkers, and L. P. Kouwenhoven. Electrical control of single hole spins in naowire quantum dots. *Nat. Nanotechnol.*, **8** 170, 2013.

[103] A. Zarassi, Z. Su, J. Danon, J. Schwenderling, M. Hocevar, B. M. Nguyen, J. Yoo, S. A. Dayeh, and S. M. Frolov. Magnetic field evolution of spin blockade in ge/si nanowire double quantum dots. *Phys. Rev. B*, **95** 155416, 2017.

[104] L. V. C. Assali, H. M. Petrilli, R. B. Capaz, B. Koiller, X. Hu, and S. Das Sarma. Hyperfine interactions in silicon quantum dots. *PRB*, **83** 165301, 2011.

[105] S. Nadj-Perge, V. S. Pribiag, J. W. G. van den Berg, K. Zuo, S. R. Plissard, E. P. A. M. Bakkers, S. M. Frolov, and L. P. Kouwenhoven. Spectroscopy of spin-orbit quantum bits in indium antimonide nanowires. *Phys. Rev. Lett.*, **108** 166801, 2012.

[106] T. H. Stoof and Y. V. Nazarov. Time-dependent resonant tunneling via two discrete states. *PRB*, **53** 1050, 1996.

[107] X. Hao, R. Ruskov, M. Xiao, C. Tahan, and H. Jiang. Electron spin resonance and spin-valley physics in a silicon double quantum dot. *Nature Communications*, **5** 3860, 2014.

[108] B. Voisin. *Control of electrons and uniques dopants in silicon transistors*. Ph.D. thesis, CEA-INAC, University of Grenoble, 2013.

[109] Z. Zeng, F. Triozon, S. Barraud, and Y. Niquet. A simple interpolation model for the carrier mobility in trigate and gate-all-around silicon nwfets. *IEEE Transactions on Electron Devices*, **64** 2485, 2017.

[110] L. Bourdet, J. Li, J. Pelloux-Prayer, F. Triozon, M. Cassé, S. Barraud, S. Martinie, D. Rideau, and Y.-M. Niquet. Contact resistances

in trigate and finfet devices in a non-equilibrium green's functions approach. *Journal of Applied Physics*, **119** 084503, 201.

[111] M. Fuechsle, J. A. Miwa, S. Mahapatra, H. Ryu, S. Lee, O. Warschkow, L. C. L. Hollenberg, G. Klimeck, and M. Y. Simmons. A single-atom transistor. *Nature Nanotechnology*, **7** 242, 2012.

[112] Bohuslavskyi, H., S. Barraud, M. Cassé, V. Barrai, B. Bertrand, L. Hutin, F. Arnaud, P. Galy, M. Sanquer, S. D. Franceschi, and M. Vinet. 28nm fully-depleted soi technology: Cryogenic control electronics for quantum computing. In *Silicon Nanoelectronics Workshop*, pp. 143–144. Kyoto, 2017.

[113] Bohuslavskyi, H., S. Barraud, V. Barral, M. Casse, L. Le Guevel, L. Hutin, B. Bertrand, A. Crippa, X. Jehl, G. Pillonnet, L. Jansen, F. Arnaud, P. Galy, R. Maurand, S. De Franceschi, M. Sanquer, and M. Vinet. Cryogenic characterization of 28nm fdsoi ring oscillators with energy efficiency optimization. *IEEE Transactions on Electron Devices*, **65** 3682 , 2018.

[114] A. Beckers, F. Jazaeri, Bohuslavskyi, H., L. Hutin, S. D. Franceschi, and C. Enz. Design-oriented modeling of 28 nm fdsoi cmos technology down to 4.2 k for quantum computing. In *Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon*, pp. 1–4. 2018.

[115] B. Doris, B. DeSalvo, K. Cheng, P. Morin, and M. Vinet. Planar fully-depleted-silicon-on-insulator technologies: Toward the 28nm node and beyond. *Solid-State Electronics*, **117** 37, 2016.

[116] N. Planes, O. Weber, V. Barral, S. Haendler, D. Noblet, D. Croain, M. Bocat, P. O. Sassoulas, X. Federspiel, A. Cros, A. Bajolet, E. Richard, B. Dumont, P. Perreau, D. Petit, D. Golanski, C. Fenouillet-Béranger, N. Guillot, M. Rafik, V. Huard, S. Puget, X. Montagner, M. A. Jaud, O. Rozeau, O. Saxod, F. Wacquant, F. Monsieur, D. Barge, L. Pinzelli, M. Mellier, F. Boeuf, F. Arnaud, and M. Haond. 28nm fdsoi technology platform for high-speed low-voltage digital applications. In *2012 Symposium on VLSI Technology (VLSIT)*, pp. 133–134. 12-14 June 2012.

[117] D. Jacquet, F. Hasbani, P. Flatresse, R. Wilson, F. Arnaud, G. Cesana, T. D. Gilio, C. Lecocq, T. Roy, A. Chhabra, C. Grover, O. Minez, J. Uginet, G. Durieu, C. Adobati, D. Casalotto, F. Nyer,

P. Menut, A. Cathelin, I. Vongsavady, and P. Magarshack. A 3 ghz dual core processor arm cortex tm -a9 in 28 nm utbb fd-soi cmos with ultra-wide voltage range and energy efficiency optimization. *IEEE Journal of Solid-State Circuits*, **49** 812, April 2014.

[118] T. Skotnicki, C. Fenouillet-Beranger, C. Gallon, F. Boeuf, S. Monfray, F. Payet, A. Pouydebasque, M. Szczap, A. Farcy, F. Arnaud, S. Clerc, M. Sellier, A. Cathignol, J. Schoellkopf, E. Perea, R. Ferrant, and H. Mingam. Innovative materials, devices, and cmos technologies for low-power mobile multimedia. *IEEE Transactions on Electron Devices*, **55** 96, 2008.

[119] C. Fenouillet-Beranger, P. Perreau, L. Tosti, O. Thomas, J. Noel, O. Weber, F. Andrieu, M. Cassé, X. Garros, T. Benoist, S. Haendler, A. Bajolet, F. Bœuf, K. K. Bourdelle, F. Boedt, and O. Faynot. Low power utbox and back plane (bp) fdsoi technology for 32nm node and below. In *2011 IEEE International Conference on IC Design & Technology*, pp. 1–4. 2011.

[120] A. Ortiz-Conde, F. J. Garcıia Sanchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue. A review of recent mosfet threshold voltage extraction methods. *Microelectronics Reliability*, **42** 583, 2002.

[121] E. D. Gutierrez, J. Deen, and C. Claeys. *Low Temperature Electronics: Physics, Devices, Circuits, and Applications*. Academic Press, 2001.

[122] R. Wacquez, M. Vinet, M. Pierre, B. Roche, X. Jehl, O. Cueto, J. Verduijn, G. C. Tettamanzi, S. Rogge, V. Deshpande, B. Previtali, C. Vizioz, S. Pauliac-Vaujour, C. Comboroure, N. Bove, O. Faynot, and M. Sanquer. Single dopant impact on electrical characteristics of soi nmosfets with effective length down to 10nm. In *2010 Symposium on VLSI Technology*, pp. 193–194. 2010.

[123] F. Balestra and G. Ghibaudo. *Device and Circuit Cryogenic Operation for Low Temperature Electronics*. Springer Science+Business Media Dordrecht, 2001.

[124] F. Balestra and G. Ghibaudo. Brief review of the mos device physics for low temperature electronics. *Solid-State Electronics*, **37** 1967, 1994.

[125] S. M. Sze and K. K. Ng. *Physics of Semiconductor Devices, 3rd edition*. Wiley, 2006.

[126] S. Takagi, A. Toriumi, M. Iwase, and H. Tango. On the universality of inversion layer mobility in si mosfet's: Part i-effects of substrate impurity concentration. *IEEE Transactions on Electron Devices*, **41** 2357, 1994.

[127] S. Saito, D. Hisamoto, S. Kimura, and M. Hiratani. Unified mobility model for high-/spl kappa/ gate stacks [misfets]. In *IEEE International Electron Devices Meeting 2003*, pp. 33.3.1–33.3.4. 2003.

[128] S. M. Thomas, M. J. Prest, T. E. Whall, D. R. Leadley, P. Toniutti, F. Conzatti, D. Esseni, L. Donetti, F. Gámiz, R. J. P. Lander, G. Vellianitis, P.-E. Hellström, and M. Östling. On the role of coulomb scattering in hafnium-silicate gated silicon n and p-channel metal-oxide-semiconductor-field-effect-transistors. *Journal of Applied Physics*, **110** 124503, 2011.

[129] M. V. Fischetti, D. A. Neumayer, and E. A. Cartier. Effective electron mobility in si inversion layers in metal-oxide-semiconductor systems with a high-k insulator: The role of remote phonon scattering. *Journal of Applied Physics*, **90** 4587, 2001.

[130] S. Datta, G. Dewey, M. Doczy, B. S. Doyle, B. Jin, J. Kavalieros, R. Kotlyar, M. Metz, N. Zelick, and R. Chau. High mobility si/sige strained channel mos transistors with hfo/sub 2//tin gate stack. In *IEEE International Electron Devices Meeting 2003*, pp. 28.1.1–28.1.4. 2003.

[131] C. G. Sodini, T. W. Ekstedt, and J. L. Moll. Charge accumulation and mobility in thin dielectric mos transistors. *Solid-State Electronics*, **25** 833, 1982.

[132] G. Ghibaudo. New method for the extraction of mosfet parameters. *Electronics Letters*, **24** 543, 1988.

[133] M. Casse, L. Thevenod, B. Guillaumot, L. Tosti, F. Martin, J. Mitard, O. Weber, F. Andrieu, T. Ernst, G. Reimbold, T. Billon, M. Mouis, and F. Boulanger. Carrier transport in hfo/sub 2//metal gate mosfets: physical insight into critical parameters. *IEEE Transactions on Electron Devices*, **53** 759, April 2006.

[134] V. Nguyen, Y. Niquet, F. Triozon, I. Duchemin, O. Nier, and D. Rideau. Quantum modeling of the carrier mobility in fdsoi devices. *IEEE Transactions on Electron Devices*, **61** 3096, Sept 2014.

[135] L. Brunet, X. Garros, F. Andrieu, G. Reimbold, E. Vincent, A. Bravaix, and F. Boulanger. New method to extract interface states density at the back and the front gate interfaces of fdsoi transistors from cv-gv measurements. In *2009 IEEE International SOI Conference*, pp. 1–2. 2009.

[136] R. M. Incandela, L. Song, H. A. R. Homulle, F. Sebastiano, E. Charbon, and A. Vladimirescu. Nanometer cmos characterization and compact modeling at deep-cryogenic temperatures. In *2017 47th European Solid-State Device Research Conference (ESSDERC)*, pp. 58–61. 2017.

[137] N. C. Dao, A. E. Kass, M. R. Azghadi, C. T. Jin, J. Scott, and P. H. W. Leong. An enhanced mosfet threshold voltage model for the 6-300k temperature range. *Microelectronics Reliability*, **69** 36, 2017.

[138] T. Elewa, F. Balestra, S. Cristoloveanu, I. M. Hafez, J. . Colinge, A. . Auberton-Herve, and J. R. Davis. Performance and physical mechanisms in simox mos transistors operated at very low temperature. *IEEE Transactions on Electron Devices*, **37** 1007, 1990.

[139] M. Lundstrom. *Fundamentals of Nanotransistors: 6 (Lessons from Nanoscience: A Lecture Notes Series)*. World Scientific Publishing Company, 2017.

[140] M. Shin. *Electrical Characterization and Modeling of advanced FD-SOI transistors for sub-22nm nodes*. Ph.D. thesis, Korea University (Seoul, South Korea) and Grenoble INP (Grenoble, France), 2015.

[141] M. Mouis, J. W. Lee, D. Jeon, M. Shi, M. Shin, and G. Ghibaudo. Source/drain induced defects in advanced mosfets: what device electrical characterization tells. *Phys. Status Solidi C*, **11** 138, 2011.

[142] B. K. Esfeh, M. Masselus, N. Planes, M. Haond, J. . Raskin, D. Flandre, and V. Kilchytska. 28 fdsoi analog and rf figures of merit at cryogenic temperatures. In *2018 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, pp. 1–3. 2018.

[143] V. Kilchytska, S. Makovejev, S. Barraud, T. Poiroux, J.-P. Raskin, and D. Flandre. Trigate nanowire mosfets analog figures of merit. *Solid-State Electronics*, **112** 78, 2015.

[144] Z. Lun, D. S. Ang, and C. H. Ling. A novel subthreshold slope technique for the extraction of the buried-oxide interface trap density in the fully depleted soi mosfet. *IEEE Electron Device Letters*, **21** 411, Aug 2000.

[145] P. Galy, J. C. Lemyre, P. Lemieux, F. Arnaud, D. Drouin, and M. Pioro-Ladrière. Cryogenic temperature characterization of a 28-nm fd-soi dedicated structure for advanced cmos and quantum technologies co-integration. *IEEE Journal of the Electron Devices Society*, **6** 594, 2018.

[146] R. S. Murphy. *Prospects for the MOS transistor as a high frequency device*. Ph.D. thesis, INAOE, Puebla, Mexico, 1997.

[147] H. Homulle, S. Visser, B. Patra, and E. Charbon. Design techniques for a stable operation of cryogenic field-programmable gate arrays. *Review of Scientific Instruments*, **89** 014703, 2018.

[148] B. Lengeler. Semiconductor devices suitable for use in cryogenic environments. *Cryogenics*, **14** 439, 1974.

[149] A. Beckers, F. Jazaeri, and C. Enz. Characterization and modeling of 28 nm bulk cmos technology down to 4.2 k. *IEEE Journal of the Electron Devices Society*, pp. 1–1, 2018.

[150] A. Akturk, M. Holloway, S. Potbhare, D. Gundlach, B. Li, N. Goldsman, M. Peckerar, and K. P. Cheung. Compact and distributed modeling of cryogenic bulk mosfet operation. *IEEE Transactions on Electron Devices*, **57** 1334, June 2010.

[151] A. Beckers, F. Jazaeri, and C. Enz. Cryogenic mos transistor model. *IEEE Transactions on Electron Devices*, pp. 1–9, 2018.

[152] I. M. Hafez, G. Ghibaudo, and F. Balestra. Assessment of interface state density in silicon metal-oxide-semiconductor transistors at room, liquid-nitrogen, and liquid-helium temperatures. *Journal of Applied Physics*, **67** 1950, 1990.

[153] B. Roche, B. Voisin, X. Jehl, R. Wacquez, M. Sanquer, M. Vinet, V. Deshpande, and B. Previtali. A tunable, dual mode field-effect or single electron transistor. *Appl. Phys. Lett.*, **100** 032107, 2012.

[154] M. Cassé, K. Tachi, S. Thiele, and T. Ernst. Spectroscopic charge pumping in si nanowire transistors with a high-/metal gate. *Appl. Phys. Lett.*, **96** 123506, 2010.

[155] G. Ghibaudo. Transport in the inversion layer of a mos transistor: use of kubo-greenwood formalism. *Journal of Physics C: Solid State Physics*, **19** 767, 1986.

[156] N. Ma and D. Jena. Carrier statistics and quantum capacitance effects on mobility extraction in two-dimensional crystal semiconductor field-effect transistors. *2D Materials*, **2** 015003, 2015.

[157] W. Bludau, A. Onton, and W. Heinke. Temperature dependence of the band gap of silicon. *Journal of Applied Physics*, **45** 1846, 1974.

[158] T. Poiroux, O. Rozeau, P. Scheer, S. Martinie, M. Jaud, M. Minondo, A. Juge, J. C. Barbé, and M. Vinet. Leti-utsoi2.1: A compact model for utbb-fdsoi technologies–part ii: Dc and ac model description. *IEEE Transactions on Electron Devices*, **62** 2760, Sept 2015.

[159] D. Kitamaru, Y. Uetsuji, N. Sadachika, and M. Miura-Mattausch. Complete surface-potential-based fully-depleted silicon-on-insulator metal-oxide-semiconductor field-effect-transistor model for circuit simulation. *Japanese Journal of Applied Physics*, **43** 2166, 2004.

[160] I. M. Lifshitz. The energy spectrum of disordered systems. *Advances in Physics*, **13** 483, 1964.

[161] A. Gold, J. Serre, and A. Ghazali. Density of states in a two-dimensional electron gas: Impurity bands and band tails. *PRB*, **37** 4589, 1988.

[162] P. Van Mieghem. Theory of band tails in heavily doped semiconductors. *RMP*, **64** 755, 1992.

[163] S. Yaida. Instanton calculus of lifshitz tails. *PRB*, **93** 075120, 2016.

[164] N. Mott and E. A. Davis. *Electronic processes in non crystalline materials*. Clarendon Press, Oxford, 1979.

[165] S. A. Vitale, J. Kedzierski, P. Healey, P. W. Wyatt, and C. L. Keast. Work-function-tuned tin metal gate fdsoi transistors for subthreshold operation. *IEEE Transactions on Electron Devices*, **58** 419, 2011.

[166] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Bokor, P. K. Ko, and C. Hu. Dynamic threshold-voltage mosfet (dtmos) for ultra-low voltage vlsi. *IEEE Transactions on Electron Devices*, **44** 414, 1997.

[167] H. Soeleman, K. Roy, and B. C. Paul. Robust subthreshold logic for ultra-low power operation. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **9** 90, 2001.

[168] V. Kilchytska, A. Neve, L. Vancaillie, D. Levacq, S. Adriaensen, H. van Meer, K. D. Meyer, C. Raynaud, M. Dehan, J. . Raskin, and D. Flandre. Influence of device engineering on the analog and rf performances of soi mosfets. *IEEE Transactions on Electron Devices*, **50** 577, 2003.

[169] T. Tanaka, Y. Momiyama, and T. Sugii. Fmax enhancement of dynamic threshold-voltage mosfet (dtmos) under ultra-low supply voltage. In *International Electron Devices Meeting. IEDM Technical Digest*, pp. 423–426. 1997.

[170] http://qtwork.tudelft.nl/ schouten/ivvi/index-ivvi.htm.

[171] http://neel.cnrs.fr/spip.php?article149.

[172] https://github.com/qcodes/qcodes.

[173] C. H. Chenming. *Modern Semiconductor Devices for Integrated Circuits*. Pearson, 2009.

[174] J. Laramée, M. J. Aubin, and J. D. N. Cheeke. Behavior of cmos inverters at cryogenic temperatures. *Solid-State Electronics*, **28** 453, 1985.

[175] J. B. Burr. Cryogenic ultra low power cmos. In *1995 IEEE Symposium on Low Power Electronics. Digest of Technical Papers*, pp. 82–83. 9-11.

[176] E. Charbon, F. Sebastiano, A. Vladimirescu, H. Homulle, S. Visser, L. Song, and R. M. Incandela. Cryo-cmos for quantum computing. In *Presentation given during 2016 IEEE International Electron Devices Meeting (IEDM)*, pp. 13.5.1–13.5.4. 2016.

[177] J. Yuan, K. A. Moen, J. D. Cressler, H. Rücker, B. Heinemann, and W. Winkler. Sige hbt cml ring oscillator with 2.3-ps gate delay at cryogenic temperatures. *IEEE Transactions on Electron Devices*, **57** 1183, 2010.

[178] H. Homulle, L. Song, E. Charbon, and F. Sebastiano. The cryogenic temperature behavior of bipolar, mos, and dtmos transistors in standard cmos. *IEEE Journal of the Electron Devices Society*, **6** 263, 2018.

[179] M. L. Schneider, C. A. Donnelly, S. E. Russek, B. Baek, M. R. Pufall, P. F. Hopkins, P. D. Dresselhaus, S. P. Benz, and W. H. Rippard. Ultralow power artificial synapses using nanotextured magnetic josephson junctions. *Sci Adv*, **4**, 2018.

[180] I. V. Vernik, T. A. Ohki, M. B. Ketchen, and M. Bhushan. Performance characterization of pd-soi ring oscillators at cryogenic temperatures. In *2010 IEEE International SOI Conference (SOI)*, pp. 1–2. 2010.

[181] P. Clapera, S. Ray, X. Jehl, M. Sanquer, A. Valentian, and S. Barraud. Design and cryogenic operation of a hybrid quantum-cmos circuit. *PRAPPLIED*, **4** 044009, 2015.

[182] L. Hutin, R. Maurand, D. Kotekar-Patil, A. Corna, Bohuslavskyi, H., X. Jehl, S. Barraud, S. D. Franceschi, M. Sanquer, and M. Vinet. Si cmos platform for quantum information processing. In *IEEE Symposium on VLSI Technology*, pp. 1–2. Honolulu, 2016.

[183] M. Shin, M. Shi, M. Mouis, A. Cros, E. Josse, G. T. Kim, and G. Ghibaudo. Low temperature characterization of 14nm fdsoi cmos devices. In *2014 11th International Workshop on Low Temperature Electronics (WOLTE)*, pp. 29–32. 2014.

[184] M. H. Na, E. J. Nowak, W. Haensch, and J. Cai. The effective drive current in cmos inverters. In *Digest. International Electron Devices Meeting,*, pp. 121–124. 2002.

[185] B. Zhai, L. Nazhandali, J. Olson, A. Reeves, M. Minuth, R. Helfand, S. Pant, D. Blaauw, and T. Austin. A 2.60pj/inst subthreshold sensor processor for optimal energy efficiency. In *2006 Symposium on VLSI Circuits, 2006. Digest of Technical Papers.*, pp. 154–155. 2006.

[186] B. Zhai, S. Pant, L. Nazhandali, S. Hanson, J. Olson, A. Reeves, M. Minuth, R. Helfand, T. Austin, D. Sylvester, and D. Blaauw. Energy-efficient subthreshold processor design. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **17** 1127, 2009.

[187] J. Hu, J. E. Park, G. Freeman, and H. S. P. Wong. Effective drive current in cmos inverters for sub-45nm technologies. In *NTSI Nanotech, Boston, June 1-5*. 2008.

[188] F. Jazaeri, A. Pezzotta, and C. Enz. Free carrier mobility extraction in fets. *IEEE Transactions on Electron Devices*, **64** 5279, December 2017.

[189] F. Sebastiano, H. Homulle, B. Patra, R. Incandela, J. van Dijk, L. Song, M. Babaie, A. Vladimirescu, and E. Charbon. Cryo-cmos electronic control for scalable quantum computing. In *2017 54th ACM/EDAC/IEEE Design Automation Conference (DAC)*, pp. 1–6. 2017.

[190] M. Sanquer, M. Specht, L. Ghenim, S. Deleonibus, and G. Guegan. Coulomb blockade in low-mobility nanometer size si mosfet's. *PRB*, **61** 7249, 2000.

[191] J. P. G. van Dijk, E. Kawakami, R. N. Schouten, M. Veldhorst, L. M. K. Vandersypen, M. Babaie, E. Charbon, and F. Sebastiano. The impact of classical control electronics on qubit fidelity. *arXiv:1803.06176v1*, Fri, 16 Mar 2018.

[192] https://www.oxford-instruments.com/products/cryogenic-environments/dilution-refrigerator/cryogen-free-dilution-refrigerators/tritonxl.

[193] S. Kamohara, N. Sugii, K. Ishibashi, K. Usami, H. Amano, K. Kobayashi, and C. Pham. A perpetuum mobile 32bit cpu on 65nm sotb cmos technology with reverse-body-bias assisted sleep mode. In *2014 IEEE Hot Chips 26 Symposium (HCS)*, pp. 1–1. 2014.

[194] N. Sugii, Y. Yamamoto, H. Makiyama, T. Yamashita, H. Oda, S. Kamohara, Y. Yamaguchi, K. Ishibashi, T. Mizutani, and T. Hiramoto. Ultralow-power sotb cmos technology operating down to 0.4 v, 2014.

[195] E. G. Ioannidis, S. Haendler, C. G. Theodorou, N. Planes, C. A. Dimitriadis, and G. Ghibaudo. Statistical analysis of dynamic variability in 28nm fd-soi mosfets. In *2014 44th European Solid State Device Research Conference (ESSDERC)*, pp. 214–217. 2014.

[196] https://www.isis.stfc.ac.uk/Pages/Orange-MAXI-50mm Cryostats.aspx.

[197] J. Ekin. *Experimental Techniques for Low-Temperature Measurements: Cryostat Design, Material Properties and Superconductor Critical-Current Testing*. Oxford university press, Oct 2006.

[198] B. E. Kane. A silicon-based nuclear spin quantum computer. *Nature*, **393** 133, 1998.

[199] W. H. Lim, F. A. Zwanenburg, H. Huebl, M. Möttönen, K. W. Chan, A. Morello, and A. S. Dzurak. Observation of the single-electron regime in a highly tunable silicon quantum dot. *Appl. Phys. Lett.*, **95** 242102, 2009.

[200] X. Jehl, B. Voisin, B. Roche, E. Dupont-Ferrier, S. D. Franceschi, M. Sanquer, M. Cobian, Y.-M. Niquet, B. Sklénard, O. Cueto, R. Wacquez, and M. Vinet. The coupled atom transistor. *Journal of Physics: Condensed Matter*, **27** 154206, 2015.

[201] G. P. Lansbergen, R. Rahman, C. J. Wellard, I. Woo, J. Caro, N. Collaert, S. Biesemans, G. Klimeck, L. C. L. Hollenberg, and S. Rogge. Gate-induced quantum-confinement transition of a single dopant atom in a silicon finfet. *Nature Physics*, **4** 656, 2008.

[202] M. Urdampilleta, A. Chatterjee, C. C. Lo, T. Kobayashi, J. Mansir, S. Barraud, A. C. Betz, S. Rogge, M. F. Gonzalez-Zalba, and J. J. L. Morton. Charge dynamics and spin blockade in a hybrid double quantum dot in silicon. *Phys. Rev. X*, **5** 031024, 2015.

[203] A. C. Betz, R. Wacquez, M. Vinet, X. Jehl, A. L. Saraiva, M. Sanquer, A. J. Ferguson, and M. F. Gonzalez-Zalba. Dispersively detected pauli spin-blockade in a silicon nanowire field-effect transistor. *Nano Lett.*, **15** 4622, 2015.

[204] T. F. Watson, B. Weber, Y.-L. Hsueh, L. C. L. Hollenberg, R. Rahman, and M. Y. Simmons. Atomically engineered electron spin lifetimes of 30 s in silicon. *Sci Adv*, **3**, 2017.

[205] E. Dupont-Ferrier, B. Roche, B. Voisin, X. Jehl, R. Wacquez, M. Vinet, M. Sanquer, and S. De Franceschi. Coherent coupling of two dopants in a silicon nanowire probed by landau-zener-stückelberg interferometry. *Phys. Rev. Lett.*, **110** 136802, 2013.

[206] B. Roche, R.-P. Riwar, B. Voisin, E. Dupont-Ferrier, R. Wacquez, M. Vinet, M. Sanquer, J. Splettstoesser, and X. Jehl. A two-atom electron pump. *Nature Communications*, **4** 1581, 2013.

[207] P. Harvey-Collard, N. T. Jacobson, M. Rudolph, J. Dominguez, G. A. Ten Eyck, J. R. Wendt, T. Pluym, J. K. Gamble, M. P. Lilly, M. Pioro-Ladrière, and M. S. Carroll. Coherent coupling between a quantum dot and a donor in silicon. *Nature Communications*, **8** 1029, 2017.

[208] K. Ono, G. Giavaras, T. Tanamoto, T. Ohguro, X. Hu, and F. Nori. Hole spin resonance and spin-orbit coupling in a silicon metal-oxide-semiconductor field-effect transistor. *Phys. Rev. Lett.*, **119** 156802, 2017.

[209] X. Jehl, M. Sanquer, G. Bertrand, G. Guegan, S. Deleonibus, and D. Fraboulet. Silicon single electron transistors with soi and mosfet structures: the role of access resistances. *IEEE Transactions on Nanotechnology*, **2** 308, 2003.

[210] L. L. Guevel, G. Billiot, Bohuslavskyi, H., S. Barraud, L. Hutin, M. Vinet, S. D. Franceschi, M. Sanquer, X. Jehl, L. Jansen, and G. Pillonnet. Fdsoi cryogenic electronics for quantum computing. In *Poster session presented at the JMC ('les Journée de la Matière Condensée')*. Grenoble, 2018.

[211] X. Jehl, B. Voisin, T. Charron, P. Clapera, S. Ray, B. Roche, M. Sanquer, S. Djordjevic, L. Devoille, R. Wacquez, and M. Vinet. Hybrid metal-semiconductor electron pump for quantum metrology. *PRX*, **3** 021012, 2013.

[212] L. P. Kouwenhoven, A. T. Johnson, N. C. van der Vaart, C. J. P. M. Harmans, and C. T. Foxon. Quantized current in a quantum-dot turnstile using oscillating tunnel barriers. *PRL*, **67** 1626, 1991.

[213] L. J. Geerligs, V. F. Anderegg, P. A. M. Holweg, J. E. Mooij, H. Pothier, D. Esteve, C. Urbina, and M. H. Devoret. Frequency-locked turnstile device for single electrons. *PRL*, **64** 2691, 1990.