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Hanqing Wang

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**THESE DE DOCTORAT DE L'ETABLISSEMENT UNIVERSITE BOURGOGNE
FRANCHE-COMTE
PREPAREE A UNIVERSITE DE TECHNOLOGIE DE BELFORT-MONTBELIARD**

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École Doctorale Sciences Pour l'Ingénieur et Microtechniques

Doctorat de Spécialité **Génie électrique**

Par

Hanqing WANG

**Design and control of a 6-phase Interleaved Boost Converter based on
SiC semiconductors with EIS functionality for Fuel Cell Electric Vehicle**

Thèse présentée et soutenue à Belfort, le 7 juin 2019

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Nomenclature

Abbreviation

BC	Boost Converter
CCM	Continuous Conduction Mode
DC-IBC	6-phase Interleaved Boost Converter based on Direct Coupled inductors of cyclic cascade structure
DFT	Discrete Fourier Transform
EIS	Electrochemical Impedance Spectroscopy
EREV	Extended Range Electric Vehicle
EV	Electric Vehicle
FC	Fuel Cell
FCEV	Fuel Cell Electric Vehicle
FIBC	Floating Interleaved Boost Converter
FPGA	Field Programmable Gate Array
GaN	Gallium Nitride
HEV	Hybrid Electric Vehicle
HIL	Hardware In the Loop
IBC	Interleaved Boost Converter
IC-IBC	6-phase Interleaved Boost Converter based on Inverse Coupled inductors of cyclic cascade structure
PEMFC	Proton Exchange Membrane Fuel Cell
PHEV	Plug-in Hybrid Electric Vehicle
PI	Proportional-Integral control
PWM	Pulse-Width Modulation
RMS	Root-Mean-Square
Si	Silicon
SiC	Silicon Carbide

SMC	Sliding-Mode Control
UC-IBC	6-phase Interleaved Boost Converter based on uncoupled inductors
WBG	Wide-Band Gap

Symbol

B_{pk}	Half of the AC flux swing (Tesla).
B_{sat}	Saturation flux density (Tesla).
C_{dl}	The capacitance property in the catalyst layer (F).
D	Duty cycle of driving signal.
E	The nerst voltage in standard state (V).
f_s	Switching frequency of converter (kHz).
I_{FC}	Fuel cell current (A).
I_L	Inductor current (A).
I_{sin}	Inductor current reference's sinusoidal disturbance signal.
i_{FC_AC}	AC response of FC current (A).
$i_{M,sat}$	Maximum magnetizing current (A).
K_g	Core geometrical constant (cm ⁵).
K_u	Winding factor
k	Coupling coefficient of coupled inductor
L_s	Self-inductance of coupled inductor (H).
M	Mutual inductance of coupled inductor (H).
N	Number of interleaved phases
N_{cell}	Number of cells
N_t	Number of turns of each winding
N_x	The quantity of paralleled MOSFET and Schottky diode per phase.
P_{losses}	Total power losses of N-phase IBC (W).
P_{on_mos}	MOSFET conduction losses (W).
P_{switch}	MOSFET switching losses (W).
P_{gate_driver}	MOSFET gate driver losses (W).
P_{on_diode}	Diode conduction losses (W).
P_{rev_diode}	Diode reverse recovery losses (W).

P_{copper}	Inductor copper losses (W).
P_{core}	Inductor core losses (W).
$P_{core_density}$	Inductor core losses density (W).
P_N	Nominal power of converter (kW).
p_{H2}	Hydrogen partial pressure against the standard atmosphere pressure (bar(g)).
p_{H2O}	Water vapor partial pressure against the standard atmosphere pressure (bar(g)).
p_{O2}	Oxygen partial pressure against the standard atmosphere pressure (bar(g)).
R_c	The resistance against the charge transfer around the catalyst layer (Ω).
R_m	The resistance against the proton transfer through the membrane (Ω).
$S_{L,n}$	Sliding surface of phase-n
T_{delay}	Phase delay between each control signal (μ s).
$T_{ambient}$	Ambient temperature ($^{\circ}$ C).
T_{dio_j}	Schottky diode junction temperature ($^{\circ}$ C).
T_{mos_j}	MOSFET junction temperature ($^{\circ}$ C).
T_{fc}	The temperature of FC (Kelvin).
T_0	The standard-state temperature (Kelvin).
V	Lyapunov candidate
V_{in}	Input voltage of converter (V).
V_{out}	Output voltage of converter (V).
v_{FC_AC}	AC response of FC voltage (V).
v_{cell}	The cell terminal voltage (V).
v_{act}	The cell activation loss or activation overvoltage (V).
v_{cons}	The cell concentration loss or concentration overvoltage (V).
v_{ohm}	The cell ohmic loss (V).
$Z_{mos_j_c}$	Thermal resistance of MOSFET from junction to case ($^{\circ}$ C/W).
$Z_{mos_c_h}$	Thermal resistance of MOSFET from case to heat-sink ($^{\circ}$ C/W).

$Z_{mos_h_a}$	Thermal resistance of MOSFET's heat-sink ($^{\circ}\text{C}/\text{W}$).
$Z_{dio_j_c}$	Thermal resistance of Schottky diode from junction to case ($^{\circ}\text{C}/\text{W}$).
$Z_{dio_c_h}$	Thermal resistance of Schottky diode from case to heat-sink ($^{\circ}\text{C}/\text{W}$).
$Z_{dio_h_a}$	Thermal resistance of Schottky diode's heat-sink ($^{\circ}\text{C}/\text{W}$).
Δi_{FC}	Fuel cell input current ripple of converter (A).
Δi_L	Inductor current ripple (A).
ΔV_{out}	Output voltage ripple of converter (V).
$\langle x(t) \rangle_{T_s}$	Average value of $x(t)$ in one period T_s
$\hat{x}(t)$	Small disturbance around the steady state value
ρ_{cu}	Wire effective resistivity ($\Omega \cdot \text{m}$).

General Introduction

During the last decade, the global warming caused by the greenhouse effect is becoming more and more seriously. The increase of anthropogenic carbon dioxide emissions is treated as the main factors of greenhouse effect and is becoming unendurable. The use of fossil fuels, which is closely related to the carbon emissions, supplies almost eighty percent of the world energy consumption. As the fossil fuels are non-renewable resources, the promotion of upgrading present energy structure is the common objective of the whole world.

Since the vehicle inventory is growing year by year, the greenhouse gas emission due to the conventional fossil fuel based vehicle has become one of the most serious contaminations for our living environment. Pollution emissions caused by classical internal combustion engine is increasing with a high ratio. In the general trend towards increasing engine efficiency and decreasing pollutant emissions, clean energy based technologies are more and more regarded as perfect solutions. The hydrogen, as a new energy vector, is drawing increasing attention of the world as it can be transformed to electric energy by a fuel cell (FC) and can be used as a new energy source to power the vehicle which is well known as Fuel Cell Electric Vehicle (FCEV). The development of this technology is increasing in the last decade. The initial and service costs of FCEV are higher while compared with Electric Vehicle (EV), Hybrid Electric Vehicle (HEV) and Plug-in Hybrid Electric Vehicle (PHEV). However, relatively long-driving range, fast-charging time and true zero emission are gained by this type of vehicles. Thus, FCEV is treated as an extremely promising and environmentally friendly technology to promote the current transportation mode.

Proton Exchange Membrane Fuel Cell (PEMFC) is the most suitable type of fuel cell for automotive applications because of their operating temperature range and quick response compared with other types of fuel cells. As a current intensive source, the output voltage of a PEMFC must be increased to approximately a few hundred volts (400V~700V) to be suitable for the motor drive system. Hence, a DC/DC step-up converter is required to connect with PEMFC with the DC bus of the vehicle. The commonly used DC/DC step-up converters can be divided into the non-isolated converters and the isolated converters. Both two types of converters possess both

advantages and disadvantages. The selection of suitable topology should be depended on the specific applications. On account of FCEV application, the FC connected DC/DC converter is requested to own low volume, low weight, high efficiency and good thermal performance. The FC current ripple connected to the DC/DC converter is also required to be kept at a low level which is closely related to FC lifespan. Although the isolated DC/DC boost converter owns the galvanic isolation and high voltage gain ratio, the drawback is that a magnetic transformer exists and its size depends of the switching frequency of converters. The intermediate AC stage can lead to the decrease of compactness. Even high-frequency transformer or planar transformer is interesting to reduce the volume and weight, the design complexity and the price will be high. In this case, the non-isolated DC/DC boost converter, which owns simple construction, high compactness, low cost and simplified control, seems to be more relevant for practical FCEV application.

So far, the general lifespan of PEMFC cannot reach the expectation of commercial application. For example, a typical life expectancy of the PEMFC under actual transportation constrains is around 3000 hours, whereas transportation applications require at least 5000 hours. Hence, the primary assignment to be solved for universal application of PEMFC is to increase its reliability and durability. Indeed, the manufacture of PEMFC is mainly depending on high cost noble materials (platinum catalyst, acid membrane, etc.) with limited durability especially in unstable operations and cyclic stress operation. Concerning these limitations, various faults such as short-circuit, starvation, CO poisoning, membrane flooding and drying can occur to PEMFC during operating condition. According to the literatures, the existed PEMFC fault diagnosis strategies can be formulated generally with model-based diagnosis approaches and non-model ones. The model-based diagnosis approaches rely on the deeply study of PEMFC's model and the non-model diagnosis methods depend on huge amounts of data sets that acquired on a system in day-to-day use or on a dedicated laboratory test bench. Electrochemical Impedance Spectroscopy (EIS) is treated as an effective characterization tool to reveal diverse failure mechanisms in the FC system. However, the achievement of EIS always relies on impedance meter equipment and FC test station. Concerning FCEV applications, the additional equipment and sensor cause the increase of volume, weight and price; furthermore, the risk of failure caused by the additional components will increase, too. In order to apply EIS functionality on-line, the integration between EIS detection and FC

connected DC/DC boost converter's control strategy is drawing the increasing attentions of researchers. This provides a favorable strategy for the FC system diagnosis without any other additional equipment to respect the limited space in a FCEV.

The objective of this thesis is firstly to propose a DC/DC boost converter combined with low input current ripple, high efficiency and compact structure for FCEV application. Then, integrate EIS functionality with the control strategy of the proposed converter.

In the first chapter, the state-of-the-art of DC/DC converter for FCEV application is analyzed. A comparative analysis of FCEV development is given. The characteristics of different manufactures' FCEVs are generally compared. Then, power converters based on the interleaved structure, Wide-Band Gap (WBG) semiconductors, coupled magnetic components and auxiliary voltage-boost circuit are reviewed. After that, the literatures that focus on on-line EIS detection based on DC/DC converter connected to FC are reviewed. At last, the requirements for a DC/DC converter focused on FCEV application combined with EIS on-line detection functionality are summarized.

In chapter 2, firstly the specifications of the proposed DC/DC boost converter, namely 6-phase Interleaved Boost Converter based on Silicon Carbide semiconductors and inverse coupled inductors of cyclic cascade structure (IC-IBC), are presented. Then, the input current ripple of IC-IBC is evaluated and compared with other two related topologies: 6-phase IBC based on uncoupled inductors (UC-IBC) and 6-phase IBC based direct coupled inductors of cyclic cascade structure (DC-IBC). After that, the magnetic component design process is explained. The theoretical analysis of power losses caused by each component is addressed. Then, the converters' efficiencies are estimated theoretically. In order to improve the efficiency of IC-IBC, the proposed converter based on multi-device in parallel construction is also discussed. At last, thermal analysis of the proposed IC-IBC and the derived configurations are evaluated together. The most suitable configuration is determined at the end of this chapter.

Chapter 3 is devoted to designing the Sliding-Mode Control (SMC) strategy for the proposed IC-IBC. Also, the Proportional-Integral (PI) control strategy for UC-IBC is also developed to make a comparison. Firstly, the design process of each control strategy is explained and the state-space representation of each topology is derived.

Then, the electrical simulation analysis of UC-IBC and IC-IBC is addressed. At last, the thermal simulation analysis of IC-IBC based on different configurations (single active device per phase and two in-parallel per phase) is discussed.

Chapter 4 is dedicated to developing EIS detection strategy of PEMFC based on the proposed IC-IBC. Firstly, EIS fundamentals such as the validity conditions and FC equivalent circuit models are studied. Then, the process of disturbance injection into the control strategy of the proposed IC-IBC is mainly discussed. The flowchart of on-line EIS detection procedure is presented and each step is detailed. After that, the sampling processes of FC voltage and current are illustrated to explain the AC impedance measurement. The calculation of FC impedance is based on Discrete Fourier Transform (DFT). At last, the membrane drying fault and flooding fault, which are based on man-assumed parameters, are both evaluated with simulation and theoretical calculation.

Following the work of previous chapters, chapter 5 is devoted to further verify the proposed topology with real-time Hardware in the loop (HIL) validation. The real-time platform (MicroLabBox) and necessary softwares (Real-Time Interface to Simulink and Xilinx System Generator) are presented and illustrated. Then, the modeling processes of each component, such as PEMFC, Pulse-Width Modulation (PWM) generator, converter and controller, are explained in detail. In order to reduce the use of computing resource, the pipeline structure is applied during the modeling procedure of converter. At last, three DC/DC boost converters are compared in real-time HIL environment: the conventional Boost converter, 6-phase UC-IBC and the proposed 6-phase IC-IBC.

The main contributions of this thesis work are summarized in the conclusion. Some new directions for future works are also presented.

Chapter 1: State of the art

1.1.Introduction

During the last decade, transportation-related air pollution emissions have reached increased consideration from the political, technical and scientific communities. In the general trend towards decreasing crude oil dependence, hydrogen-energy based technologies and fuel cell systems are more and more treated as indispensable parts in the upcoming next-generation environmentally friendly vehicle [1-1]. Indeed, they are enhancing performances and lowering fabrication costs; owing to the actual duality between hydrogen-energy and electricity, fuel cell electric vehicles (FCEV) present the advantages of a high efficiency and a (in-situ) zero pollutant emission relative to classical internal combustion engine vehicle. Moreover, their refueling time is quite similar to that of conventional oil-fueled automotive. Proton Exchange Membrane Fuel Cell (PEMFC), which owns the advantages such as low operating temperature, quick start-up and rapid load following, is seen as the most suitable type of fuel cell for transportation applications.

Nevertheless, before the mass marketization of FCEV, there are still technical and scientific issues to be solved. The most urgent subject is the limited lifespan of the existing PEMFC systems, especially when considering hard operating constraints. Depending on recent publications from the U.S. department of energy, the maximum life expectancy of an existing fuel cell system under transportation operating conditions is around 3000 hours; however, at least 5000 hours are demanded to reach the “standard” lifetime of internal combustion engines [1-2]. In order to achieve this purpose, not only studies on materials, bipolar plates, catalytic layers, and electrolytic membranes must be in progress, but also research towards extending the lifespan and increasing the reliability must be done from the overall perspective. Hence, diagnostic approaches and state-of-health management strategies are essential to be developed to increase the durability, the efficiency and the reliability of the fuel cell stack and the fuel cell system obviously [1-3]. Furthermore, in order to increase the dynamic performances of the fuel cell system, the mixed use of the fuel cell stack and auxiliary power sources such as electrochemical or electrostatic electricity storage devices must

be considered [1-3].

Taking into consideration of PEMFC's inherent characteristic (low voltage and high current) and voltage requirement of motor drive system, power converter is essential to be connected between PEMFC and the motor drive system in order to realize power conditioning. Generally, power converters can be classified as non-isolated converters and isolated converters. The former achieves a simple structure and high compactness, but voltage gain ratio is relatively low; the latter can obtain high voltage ratio, however, intermediate AC stage, which is composed of transformer and inverter, will reduce the compactness. Magnetic components based on coupled structure are attractive to reduce volume and weight and to gain compactness and space for the fuel cell system. To be emphasized, depending on the study of [1-4], the fuel cell current ripple can influence the fuel cell lifespan. In other words, a power converter which can reduce the input current ripple and the volume and weight will be more suitable for FCEV application. Nowadays, Wide-Band Gap (WBG) semiconductors have been commercialized and applied in actual FCEV [1-5]. This new generation semiconductor is much suitable for high power and high switching frequency applications; and better thermal performance, lower power losses, and higher compactness will be reached. Thus, the reliability, energy efficiency and power density of the fuel cell system will also be enhanced.

Electrochemical impedance spectroscopy (EIS) is established as a powerful characterization tool to detect different failure mechanisms occurring in the fuel cell [1-6]. As fuel cell systems should be able to enter the market at competitive prices, hence, the use of a minimal number of actual sensors is demanded. Besides, this requirement will also reduce complexity within the system and increase reliability. Thus, the integration between EIS and control strategy of the necessary power converter provides the possibility to realize on-line diagnosis of the fuel cell stack without any additional sensor or equipment [1-7].

This chapter is organized as follow. Section 1.2 will provide some recalls about fuel cell technology and fuel cell systems. The fuel cell electric vehicle's development will be compared in details. Then, section 1.3 will be devoted to the power converter development for FCEV application. The approaches to increase voltage gain ratio and the development of WBG semiconductors are separately commented. In section 1.4, online EIS detection process of PEMFC integrated with power converter is mainly discussed. Relevant studies are summarized; the advantages and disadvantages of

each method are demonstrated. Finally, this chapter will be concluded in section 1.5. A general suggestion will be proposed to achieve a proper power converter for FCEV application, which can not only realize power conversion with high performances, but also accomplish online diagnosis of the fuel cell stack without any additional equipment.

1.2. Fuel cell electric vehicle development

Nowadays, researchers of the automotive field devote themselves to developing economic and environment-friendly vehicles. Among these clean energy based vehicles, all-electric vehicles (EVs), plug-in hybrid electric vehicles (PHEVs), hybrid electric vehicles (HEVs) and fuel cell electric vehicles (FCEVs) are playing dominant roles. The researches of EVs, PHEVs and HEVs have been started early, the technologies are more mature, and have already realized large-scale marketization.

EVs are propelled by one or more electric motors powered by a rechargeable battery and achieve several performance benefits such as quiet operation, quick acceleration ability, regenerative braking, and less requirement of maintenance than internal combustion engines. PHEVs are hybrids that can be charged both by plugging them into an electrical outlet or charging station. Both PHEVs and HEVs are classified by two configurations: series PHEVs/HEVs which are also called Extended Range Electric Vehicles (EREVs), and parallel or blended PHEVs/HEVs. The electric motor of series PHEVs/HEVs is the only power source that turns the wheels; the gasoline engine only generates electricity. For the parallel PHEVs/HEVs, both the engine and electric motor are mechanically connected to the wheels, and both may propel the vehicle. HEVs combine the best features of the internal combustion engine with an electric motor and can significantly improve fuel economy. They are primarily propelled by an internal combustion engine; they also use regenerative braking to convert energy normally wasted during coasting and braking into electricity [1-8].

However, EVs, PHEVs and HEVs have several disadvantages. Firstly, the charging times of EVs and PHEVs still requires several hours (except fast charging phases). Secondly, the driving ranges of EVs are still quite limited; moreover, it is more sensitive to driving style, driving conditions, and accessory use. Thirdly, PHEVs and HEVs still rely on the crude oil which means cannot realize real “zero” pollutant emission. Briefly, FCEVs have many advantages (fast refueling, long driving range, zero pollutant emission, etc.) over the other types of clean energy vehicles. Different

fuel cell electric vehicles and fuel cell technologies are firstly discussed below.

Since the occurrence of first modern fuel cell electric vehicle around 1959 [1-9], many car manufacturers have focused on the study of FCEV. In 2000, Ford Motor Company has presented a two-wheel drive compact car which was powered by a fuel cell stack and electrochemical batteries. In 2005, a four-wheel drive model of a fuel cell vehicle has been rolled out by Ford and the driving range was 200 miles. Mercedes-Benz has also rolled out two models of its FCEV, the F-Cell, separately in 2002 and 2010. The power level and driving range of the former were 65kW and 100 miles, while 100kW and 190 miles have been achieved by the latter [1-10].

In today's market, commercial fuel cell electric vehicles proposed by Toyota Motor Corporation, Honda Motor Company, and Hyundai Motor Company have taken the major part of the market. By year-end 2017, a total of 6,364 FCEVs have been sold globally since 2013 when FCEVs first became available commercially [1-11]. Over 50% of FCEVs were sold in California of the U.S. Japan takes second place over 30% sales [1-11]. Among the manufactures, Toyota Motor Corporation accounts for over 76% of the sales. Honda Motor Company gains around 13% of the market share and Hyundai Motor Company accounts for around 11% [1-11]. A global comparison analysis of the commercialized FCEV from these three companies has been presented in Table.1.1. According to this table, obviously PEM fuel cell is the common choice of these companies.

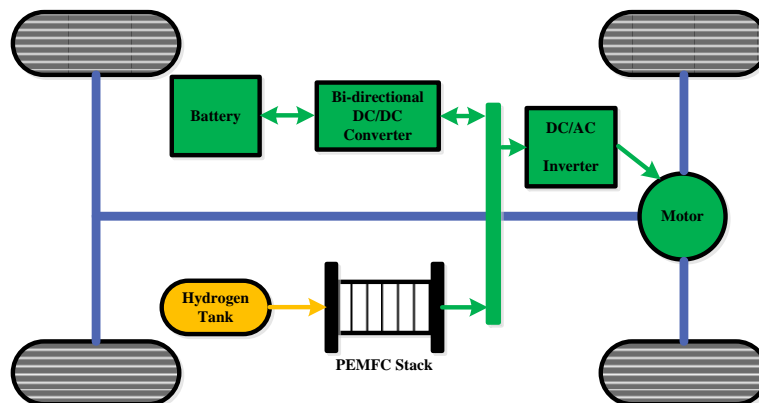
Table.1.1.Overall comparison analysis of the commercialized FCEV [1-10]

		Toyota FCHV-adv	Toyota Mirai	Honda FCX-Clarity	Honda Clarity Fuel Cell	Hyundai Tucson ix35 FCEV	Hyundai Nexo
Year		2008	2015	2008	2016	2014	2018
Vehicle class		Sport Utility Vehicle 2WD	Subcompact car	Midsized car	Midsized car	Small Sport Utility Vehicle 2WD	Small Sport Utility Vehicle 2WD
Fuel cell	Type	PEM	PEM	PEM	PEM	PEM	PEM
	Cell quantity	400 cells (dual line stacking)	370 cells [1-12] (single line stacking)	--	--	434 cells (250~450V)	440 cells [1-18] (255~450V)

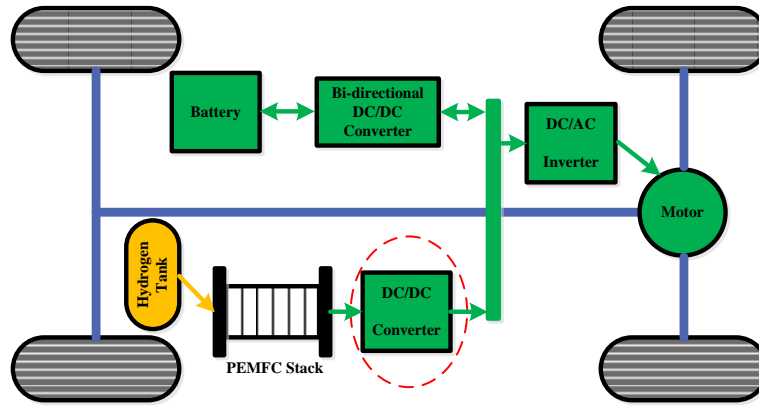
	Power density	1.4kW/L 0.83kW/kg	3.1kW/L [1-13] 2.0kW/kg	2.0kW/L 1.0kW/kg	3.1kW/L [1-15] 2.0kW/kg	1.65kW/L [1-17]	3.1kW/L [1-18]
Fuel	Type	Hydrogen	Hydrogen	Hydrogen	Hydrogen	Hydrogen	Hydrogen
	Storage pressure (nominal)	--	70MPa	35MPa	70MPa	70MPa	70MPa
	Storage volume	156L	122.4L	171L	141L	144L	156.6L
	Fuel storage mass	--	5.0kg	3.6kg	5.0kg	5.64kg	6.33kg
	Refueling time	--	3 minutes	--	3 minutes	3 minutes	3 minutes
DC/DC converter for fuel cell		No	Yes [1-14]	No	Yes [1-15]	No	No [1-18]
DC bus voltage		--	650V [1-14]	330V	500V [1-15]	400V	400V [1-18]
HV battery	Type	Ni-MH	Ni-MH	Li-Ion	Li-Ion	Li-Ion	Li-Ion
	Voltage	288V	245V	288V	358V	180V	240V
Motor	Type	AC Synchronous Motor	AC Synchronous Motor	DC Brushless Motor	PMSM	AC Induction Motor	PMSM
	Power	90kW-260Nm	113kW	100kW	130kW	100kW	120kW
Driving range (miles)		--	312	240	366	265	354
Fuel economy: Miles per Kilogram (city/highway)		--/--	66/66	60/60	68/66	48/50	58/53

For the new generation FCEVs of Toyota Motor Corporation and Honda Motor Company, the fuel cell power densities have been increased compared with previous models. The PEMFC of Toyota Mirai has been redesigned and resulted in lower concentration overvoltage, lower resistance overvoltage and lower activation overvoltage. Then, the Mirai stack increased the current density by a factor of 2.4 compared to the stack of Toyota FCHV-adv, and the cell volume has been reduced by

24%. As a result, the FC system of Toyota Mirai increased the power density by more than twice that of the conventional stack [1-13]. The new generation FCEV of Honda Motor Company, Honda Clarity Fuel Cell, employed Honda's unique 2-cell cooling structure. As a result, new cell thickness has been reduced by 20% compared with previous cell, and electricity generation for each cell has been improved by 1.5 times which allows the decrease of the number of cells by 30%. Thus, the Clarity fuel cell system also increased the power density. However, the thinner gas flow path require a higher pressure operating point than before [1-15]. Considering the hydrogen storage system, higher storage pressure is preferred to reduce storage volume and gaining inner space. The powertrain structures of these commercialized FCEV are presented in Fig.1.1. In Fig.1.1.(a), PEMFC is connected to DC bus directly without power converter. This structure has been selected by Toyota FCHV-adv (2008), Honda FCX-Clarity (2008), Hyundai Tucson ix35 FCEV (2014) and Hyundai Nexu (2018). The power control unit of this structure is simple. However, the output voltage of a single cell is quite low ($<1V$) and the voltage requirement of the motor drive system is high (at least 330V according to Table.1.1), which means whether quantities of single cells are requested to be connected in series or multi-stack structure is requested. This leads to air, hydrogen, cooling water issues in the stack or increased control complexity. At the same time, the power density of fuel cell system can be decreased. The new generation FCEV, Toyota Mirai and Honda Clarity Fuel Cell, have changed their powertrain structure to Fig.1.1 (b). The improvement is that a DC/DC converter is connected between PEMFC stack and DC bus. The output voltage of the PEMFC stack will be boosted to higher level. Meanwhile, according to Table.1.1, when the motor's maximum drive voltage is increased, the motor's maximum output and maximum torque will also be increased.



(a) Uncontrolled FC combined with controlled Battery

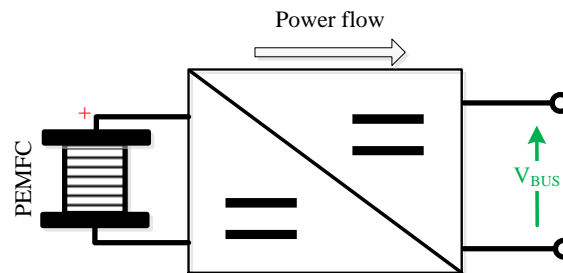


(b) Controlled FC combined with controlled Battery

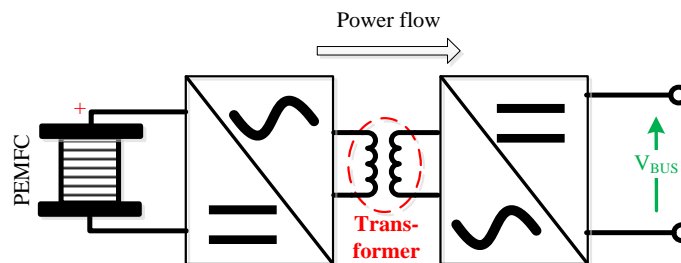
Fig.1.1. The powertrain structures of the commercialized FCEV

1.3. DC/DC converter for FCEV application

As discussed in the previous section, using power converter as an interface between the fuel cell system and DC bus shows great advantages such as increasing DC bus voltage level and reducing FC current ripple. DC/DC power converters are always classified as non-isolated DC/DC converters and isolated DC/DC converters [1-20] [1-21]. The schematic representation of these two kinds of power converters is shown by Fig.1.2.



(a) Non-isolated DC/DC converter



(b) Isolated DC/DC converter

Fig.1.2. Schematic representations of DC/DC converters

The non-isolated DC/DC converters are widely used due to their simple structure, high compactness, low cost and simplified control. Some non-isolated topologies as Boost converter, Buck-Boost converter, Cuk converter, and Sepic converter are well-known. Unlike the other three topologies, in whole duty cycle range (from zero to one), the voltage gain ratio of a Boost converter is always higher than one; and the output voltage is positive with respect to the input voltage [1-22] [1-23].

Due to the existence of a magnetic transformer, the isolated DC/DC converters are more suitable for the application that requests a high voltage gain ratio. Another characteristic of the isolated DC/DC converters is the galvanic isolation. However, magnetic transformer leads to bigger volume, higher weight and more complex design. The isolated power converters are a combination of two stages: the primary DC/AC stage (Half-bridge inverter, Full-bridge inverter, etc.) and the secondary AC/DC stage (controlled or uncontrolled rectifier). Other well-known isolated topologies are as: Push-pull converter, Forward converter, and Flyback converter.

Towards the FCEV application, the following criteria are essential to be satisfied to design or select a proper power conditioning unit:

- High efficiency, which is closely related to the fuel economy and the design process of the powertrain cooling system [1-35][1-36][1-37][1-40];
- High voltage gain ratio, which is required by the inherent characteristics of the FC stack [1-55][1-60][1-65];
- High compactness, low weight and volume are essential due to the limited inner space of the FCEV [1-43][1-45];
- Low input current ripple is requested to extend the FC stack's lifespan [1-4];
- Low cost and high reliability are mandatory to ensure commercialization [1-3][1-74].

Non-isolated DC/DC boost converters based on the interleaved structure are helpful to reduce the FC current ripple and the weight and size of the FC system [1-14]. Wide-Band Gap (WBG) semiconductors-based power switches have been commercialized and are a better choice than conventional Si semiconductors-based ones to improve thermal performance and efficiency of a power converter [1-15]. Power converters based on coupled magnetic components are possible to increase compactness, reduce weight and increase voltage gain [1-24]. Meanwhile, auxiliary circuits that focus on increasing voltage gain ratio are also attractive for FCEVs application [1-25]. Power converters for FCEVs applications, based on these

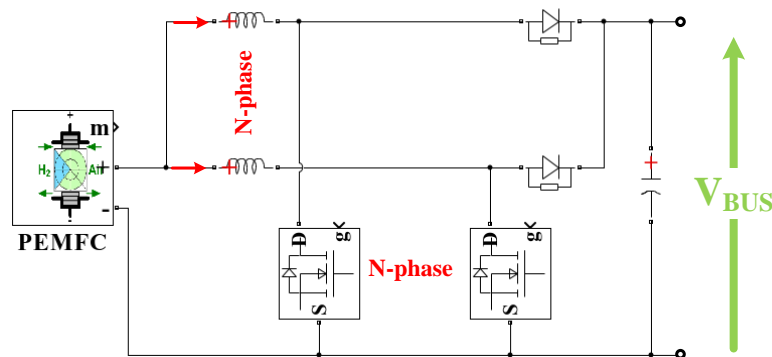
technologies, will be analyzed in the following subsections.

1.3.1. Power converters based on the interleaved structure

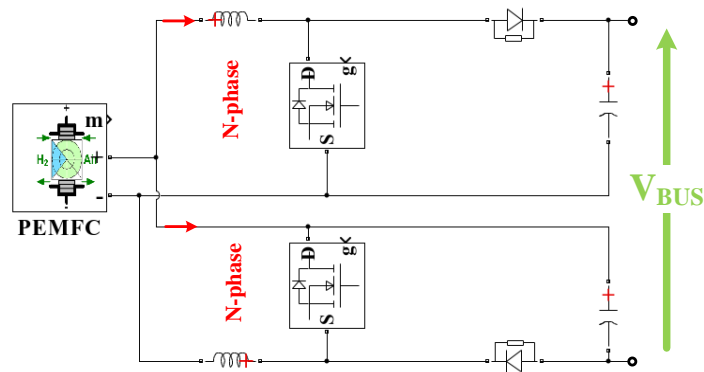
Interleaved Boost Converter (IBC), as presented in Fig.1.3 (a), has been developed focusing on reducing power source current ripple while retaining the same voltage gain ratio as the conventional Boost converter [1-26]. Benefiting from the specific structure, the input current is shared by multiple parallel power switches, hence, current stress of each power switch can be reduced and total efficiency of the converter can be increased. Concerning the real FCEVs applications, Wen et al. [1-27] have presented a 150kW, 2-phase hybrid-mode IBC. A 500W 3-phase IBC prototype based on Maximum Power Point Tracking (MPPT) controller has been analyzed by Benyahia et al. [1-28]. A 4-phase IBC has been adopted by Toyota Mirai [1-14] to increase the voltage of the motor and to reduce the number of fuel cell stack cells.

Floating Interleaved Boost Converter (FIBC), as presented in Fig.1.3 (b), has also been widely studied for FCEVs application due to its ability that can not only reduce the power source current ripple but also increase the voltage gain ratio [1-29] [1-30]. However, the control design is more complex than for IBC.

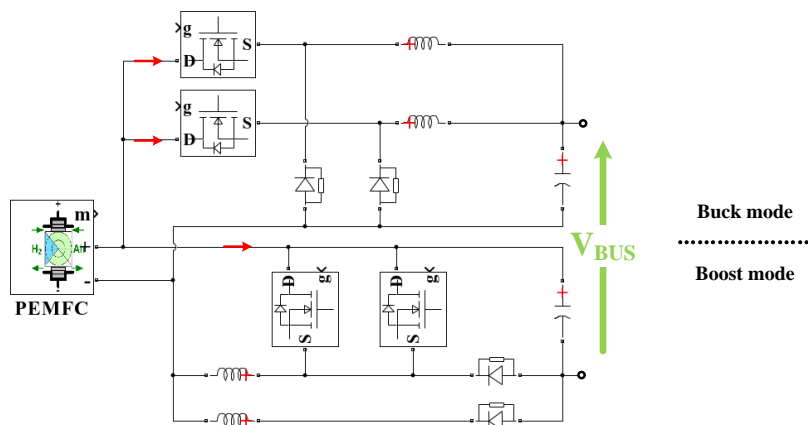
According to a recent study, a novel 50kW prototype Floating Interleaved Buck-Boost Converter (FIB-BC) for fuel cell electric vehicle applications has been proposed by Gao et al. [1-31] and shown in Fig.1.3 (c). The proposed topology provided significant mitigation of the boost module and buck module with switching between the step-up and step-down modes, lowering input current ripple and improving efficiency and reliability. High efficiencies have been achieved which were kept above 95% (Si-based IGBT).



(a) N-phase IBC [1-27] [1-28]



(b) N-phase FIBC [1-29] [1-30]



(c) 4-phase FIB-BC [1-31]

Fig.1.3.Schematics of non-isolated DC/DC converters for FCEVs application based on the interleaved structures

1.3.2.Power converters based on WBG semiconductors

Nowadays, the new generation Wide Band-Gap (WBG) semiconductors that feature high power density, high efficiency, and good thermal performance are quite suitable for FCEV applications. Silicon Carbide (SiC) and Gallium Nitride (GaN) are the most promising candidates to replace Silicon (Si) in the next generation of power switches [1-32]. Fig.1.4 presents the material properties of Si, SiC, and GaN [1-33]. The high critical field of both GaN and SiC is a property which allows these devices to operate at high voltages and low leakage currents. Higher electron mobility and electron saturation velocity allow for a higher frequency of operation. Higher thermal conductivity means that the material is superior in conducting heat efficiently. Higher

thermal conductivity combined with wide bandgap and high critical field gives SiC semiconductors an advantage when high power is a key device feature.

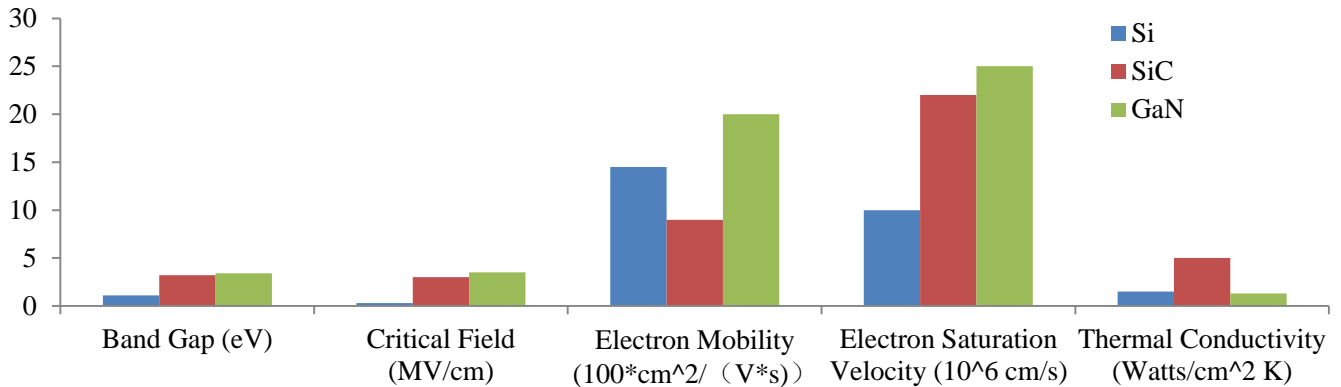


Fig.1.4. The material properties of Si, SiC and GaN

According to [1-34], the SiC semiconductor-based power switches have been identified as a prime option for the FCEV applications, which is benefited by the characteristics of the specific material. Though the Si-IGBT are chosen for the high power design, the low switching frequency, relatively low maximum operating temperature, and high switching losses are the limits for the application in high frequency, high power fields. According to [1-15], SiC power module [1-16] has been used for the first time in a production vehicle, and the size of the FC voltage converter unit has been reduced.

Table.1.2 presents the WBG semiconductors based power converters/inverters for transportation applications. Among these studies, some of them focused on the fuel cell powered more electric aircraft (MEA) application [1-35] [1-36] and military electric vehicle application [1-37], where the operating conditions are much extreme than the daily transportation applications. Meanwhile, in order to make a more comprehensive presentation of the WBG semiconductors applications, fuel cell connected DC/DC power converters [1-35] [1-36] [1-38], battery connected bi-directional DC/DC power converters [1-39] [1-37], and motor drive system's inverters [1-40] [1-41] are presented.

These power converters and inverters are all realized and verified by experiments. Obviously, high switching frequencies (50~200kHz) have been used by the SiC/GaN MOSFET based power converters and inverters. In some applications, only SiC semiconductors are used [1-39] [1-36]; in others, different types of semiconductors are used mixed. All of these topologies have very high efficiencies which are commonly over 98%. Benefiting from this advantage, better thermal performances

have been achieved, and the requirements for the heat dissipation systems have been reduced. Hence, the compactness and the reliability of power conditioning units have been increased.

Table.1.2. Power converter/inverter based on WBG semiconductors for transportation applications

Topology	Ref	Power level	Switching frequency	Max Efficiency	Semiconductor		Application field
					Type	Part No.	
Bi-directional DC/DC Half-Bridge converter	[1-39]	2kW	150kHz, 200kHz	98.8%	SiC MOSFET	1200V 24A CMF20120D (CREE)	EV; HEV; Plug-in EV; FCEV.
					SiC SBD	1200V 54A C4D40120D (CREE)	
6-phase IBC	[1-35]	15kW (6 parallel fuel cell)	--	~97%	SiC MOSFET	--	FC powered MEA
					No information of diodes.		
Bi-directional DC/DC Half-Bridge converter	[1-37]	100kW (continuous), 150kW (peak)	--	98% at 100 ambient temperature	Si IGBT	--	Military EV
					SiC diode	--	
Three-phase Half-Bridge inverter	[1-40]	30kW	20kHz	99%	SiC MOSFET power module	1200V 300A CAS300M12-BM2 (CREE)	EV; HEV; Plug-in EV; FCEV.
					No information of diodes.		

Three-phase Half-Bridge inverter	[1-41]	30kW (continuous)	20kHz	98.9%	SiC MOSFET power module	1200V 444A CAS325M12- HM2 (CREE)	EV; HEV; Plug-in EV; FCEV.
		55kW (peak)			Schottky barrier diode	--	
Floating-Output Interleaved-Input boost	[1-36]	60kW (2kV V_{in})	50~ 100kHz	98.7%	SiC MOSFET	3.3 kV XPM3-3300-0 040-ES (CREE)	FC powered MEA
					SiC schottky diode	CPW3-3300-Z 045B (CREE)	
Three level boost	[1-38]	1.1kW & 1.3kW	100kHz	--	GaN MOSFET	GS66508T E-HEMTs (GaN Systems)	FCEV
					SiC schottky diode	C3D10065E (CREE)	

1.3.3. Power converters based on coupled magnetic components

As studied previously, power converters based on the interleaved structure are quite suitable for FCEVs application. However, the increase in the number of branches will lead to an increase in the quantity of magnetic components. Since the fuel cell connected power converter has to constantly pass the high power generated by the fuel cell, the inductors require high heat dissipation performance. For example, the 4-phase IBC of Toyota Mirai used liquid loop cooling (LLC) to improve the heat dissipation capacity by reducing the thermal resistance [1-14]. In contrast, the extra liquid coolant is required, and the global structural design of the power converter is

much more complicated.

Magnetic components based on the coupled structure can contribute a lot to reduce size and weight, to decrease quantities, and to reduce power losses [1-42]. Thus, the coupled inductors can lead to less heat dissipation and the cooling system can be simplified accordingly. The number of interleaved branches, the method of coupling, and the shape of a magnetic core influence the performances of power converters strongly. Table.1.3 presents the interleaved power converters based on different types of coupled inductors. In order to present a full comparison, the application fields are not limited to FCEVs; power conditioning units for EVs/HEVs/PHEVs applications are also studied.

Table.1.3 Interleaved power converters combined with coupled inductors for electric vehicles

Basic topology	Ref	Power level	Magnetic component			Max Efficiency	Application field
			Coupling method	Shape	Material		
2-phase IBC	[1-43]	3.6kW	Inverse coupled; 2 windings for a single core.	CCTT	--	--	FCEV
		72kW				~96.7%	
2-phase IBC	[1-44]	450W	Inverse coupled; 4 windings for a single core.	E-E (E42/21/15)	3C92	~96%	FCEV
2-phase IBC	[1-45]	1kW	Uncoupled	EE90	--	--	FCEV
			Loosely inverse coupled; 2 windings for a single core.	EE60	--	~98%	
			Integrated inverse coupled; 2 windings for	EE50	--	~97.61%	

			a single core.				
2-phase IBC	[1-46]	1kW	Inverse coupled; 2 windings for a single core.	--	--	--	FCEV
2-phase IBC	[1-47]	1kW	Inverse coupled; 2 windings for a single core.	EC70	PC40	--	FCEV
2-phase IBC	[1-48]	500W	Direct coupled; 2 windings for a single core.	--	--	~95.5%	FCEV
3-phase IBC	[1-50]	545W	3 windings for each core	E-E	--	~97%	FCEV
2-phase IB-BC	[1-49]	360W	Inverse coupled; 2 windings for each core.	Toroid	--	--	FCEV
2-phase BIB/BC	[1-53]	--	Inverse coupled; 2 windings for a single core.	U-I	3F45	~98.5%	EV/HEV/P HEV/FCEV

4-phase BIB/BC	[1-54]	120W (buck)	Inverse coupled; 4 windings for a single core.	Customer design	DMR50B	~94.1%	EV/HEV/P HEV/FCEV
		36W (boost)				~90.33%	
Interleaved forward-flyback	[1-52]	2kW	Direct coupled; 3 windings for each core.	Toroid	--	~96.5%	FCEV

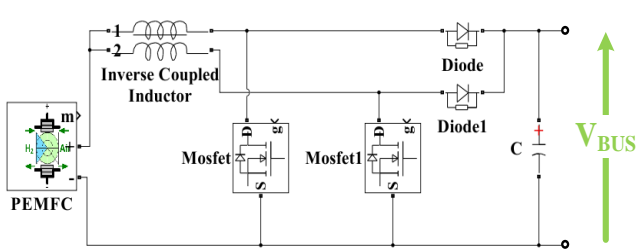
Obviously, N-phase IBCs are mostly used for FCEVs application. Both the inverse coupled structure [1-43] [1-45] [1-46] [1-47] and the direct coupled structure [1-48] have been integrated with this specific topology. H. Liu et al. [1-44] proposed a 2-phase inverse coupled IBC (IICIB) without right half-plane zeros. Besides, B.C. Barry et al. [1-49] and Tseng, K. C et al. [1-52] also separately proposed a 2-phase inverse coupled Interleaved Buck-Boost Converter (IB-BC) and a direct coupled Interleaved Forward-Flyback converter for FCEVs application. Towards EV/HEV/PHEV applications, a bi-directional buck/boost converter is essential as the interface between the energy storage system and the DC bus. Huang, X. et al. [1-53] and Yang, Y. et al. [1-54] have proposed a 2-phase and a 4-phase Bi-directional Interleaved Buck/Boost Converters (BIB/BCs), respectively.

According to the comparative studies, most of the topologies use the magnetic cores which are widely commercialized and easy to be obtained, for example, the E-E shaped cores and the toroid cores. Martinez, W. et al. [1-45] have made an overall comparative study of 2-phase IBC based on different coupling manners. According to this research, although the Integrated Winding Coupled Inductor (IWCI) can reduce the size, it can lead to a magnetic loss increase. On the other hand, this research suggests that the Loosely Coupled Inductor (LCI) converter is effective for reducing the size and improving the efficiency.

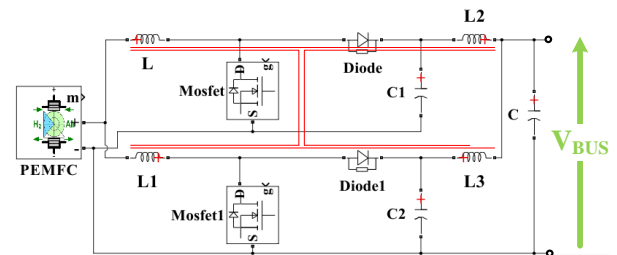
When the number of interleaved phases is bigger than two, there are more coupling manners to be selected such as symmetrical cascade association [1-54], cyclic cascade association [1-50], symmetrical parallel association, and cyclic parallel association [1-51]. Concerning different methods, the number of magnetic cores and the complexity of coupling is quite different.

A 4-phase magnetic core with the monolithic structure is used for the proposed

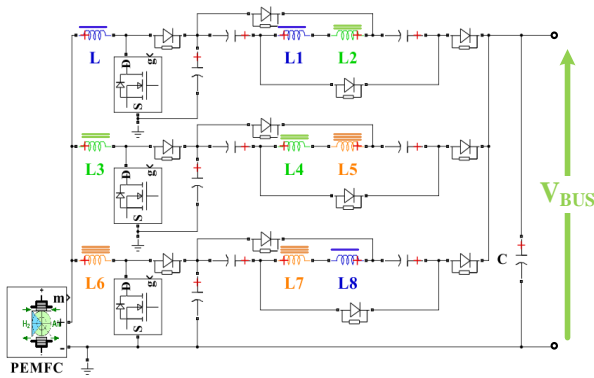
converter in [1-54]. Although the number of magnetic component has been reduced, the redundancy of the converter is decreased, and the manufacturing difficulty and cost of the specific-made magnetic core are increased which are unfavorable for commercialization. The structure of multi-magnetic cores has been selected in the study of [1-50] where a 3-phase IBC based on coupled inductors has been proposed. Each two neighbor branches are coupled by a single E-E magnetic core and then the three independent E-E magnetic cores are coupled based on the cyclic cascade association. Hence, the redundancy of the proposed converter in [1-50] is higher than the one of [1-54]. The topologies mentioned in Table.1.3 are presented in Fig.1.5.



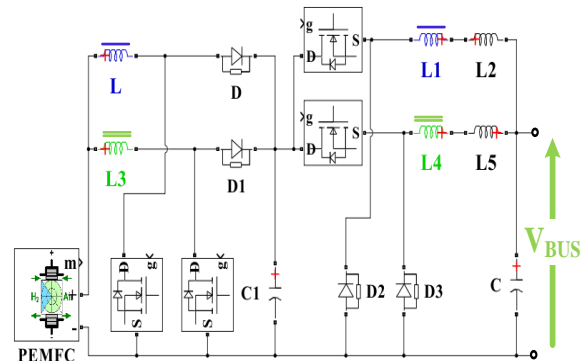
(a) 2-phase inverse coupled IBC
by [1-43] [1-45] [1-46] [1-47]



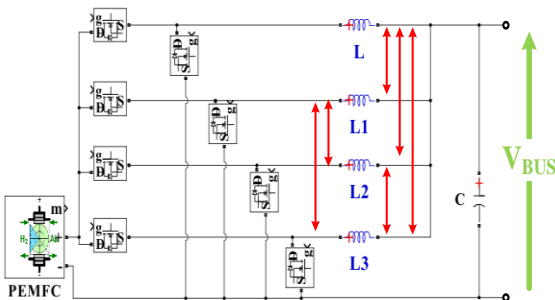
(b) IICIB by [1-44]



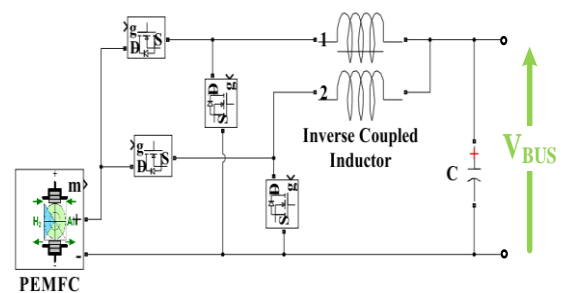
(c) 3-phase coupled IBC
with voltage multiplier circuit by [1-50]



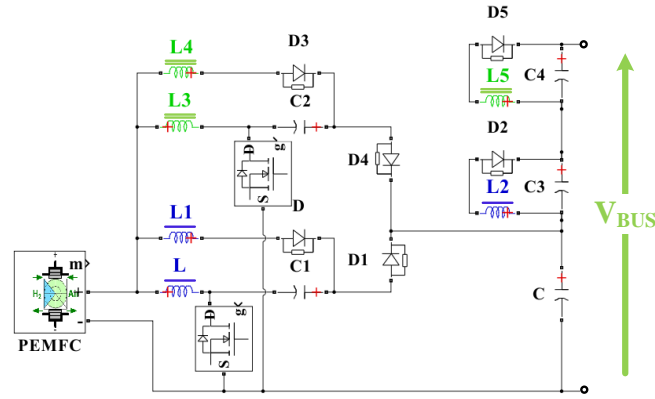
(d) 2-phase IB-BC by [1-49]



(e) 4-phase BIB/BC by [1-54]



(f) 2-phase BIB/BC by [1-53]



(g) Interleaved forward-flyback by [1-52]

Fig.1.5. Schematics of non-isolated DC/DC converters for FCEVs application

1.3.4. Power converters based on auxiliary voltage-boost circuit

In purpose of increasing the voltage gain ratio of conventional non-isolated converters, different kinds of auxiliary circuits are widely applied to this type of topologies. Table.1.4 presents the comparisons of non-isolated DC/DC converters integrated with the auxiliary voltage-boost structure; the topologies are presented in Fig.1.6 respectively.

Table.1.4 Comparisons of non-isolated DC/DC converters with auxiliary voltage-boost structure

Ref.	Voltage gain	Power level	V _{in}	V _{out}	Efficiency	Special characteristic
[1-55]	$2/(1-D)$	1.6kW	50~120V	400V	~96.6%	Input-parallel Output-series boost converter.
[1-57]	$1/[(1-D_1)*(1-D_2)]$	200W	40V	300V	~90%	New Cascade boost converter.
[1-64]	$[(1+D)/(1-D)]^2$	--	12V	100V	<90%	3-Z-Network based boost converter.
[1-60]	$2/(1-D)$	3kW	20~35V	250V	~94%	2-phase IBC combined with switched capacitor.

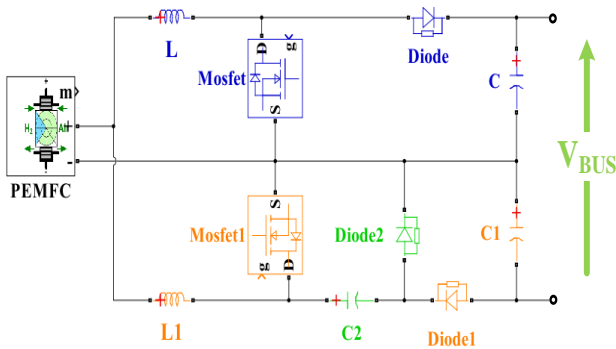
[1-61]	2/(1-D)	1.2kW	26~43V	200V	~95%	2-phase IBC combined with voltage doubler circuit.
[1-62]	2/(1-D)	1kW	24V	250V	--	2-phase IBC combined with voltage double circuit.
[1-58]	2/(1-D)	100W	24V	240V	~95.8%	High step-up converter.
[1-65]	2/(3-4*D)	1.2kW	60~150V	400V	~95.66%	Three level Q-Z source boost converter.

The Input-Parallel Output-Series structure is interesting to be considered by the conventional Boost converter according to the study of Wang et al. [1-55]. An interleaved structure based on two inductors is chosen on the input side of this structure to reduce input current ripple. In addition, the two capacitors at the output side are connected in series to obtain a high voltage gain. Cascade Boost converter is another solution to achieve a high voltage gain ratio when the galvanic isolation is not necessary [1-56]. Nejad et al. [1-57] proposed a new cascade Boost converter; it can not only retain the advantages of the conventional cascade Boost converter but also reduce the conduction losses of semiconductors. Al-Saffar et al. [1-58] proposed a new single-switch step-up DC/DC converter which was derived from the conventional Boost converter integrated with self-lift Sepic converter for providing high voltage gain without extreme switch duty cycle.

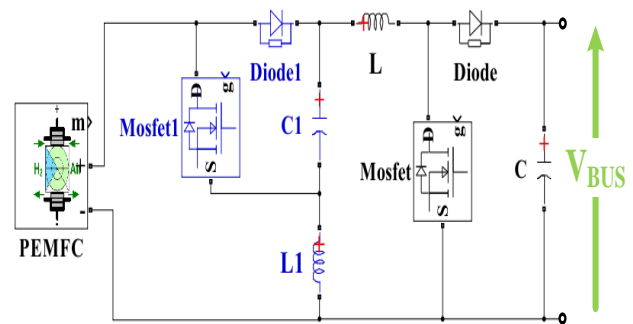
Voltage Doubler Circuit (VDC) is well known due to its simple structure and principle. The basic operation of VDC has been discussed in detail by [1-59]. As presented in [1-60] [1-61] [1-62], some studies have integrated VDC with interleaved DC/DC converters in order to increase the voltage gain ratio. Fuzato et al. [1-62] analyzed the effect of the parasitic resistances on the static voltage gain of the 2-phase IBC combined with VDC using the final value theorem. Cardenas et al. [1-60] proposed a 3-kW DC-DC-AC power electronic interface for PEMFC application. A relatively high voltage gain (higher than 10 times) without transformer has been achieved. Wu et al. [1-61] proposed a power electronic interface based on a DC/DC converter and a DC/AC inverter which focused on grid-connected fuel cell generation

system. In this study, the DC bus voltage has been set to 200V while the maximum input voltage was only 40V.

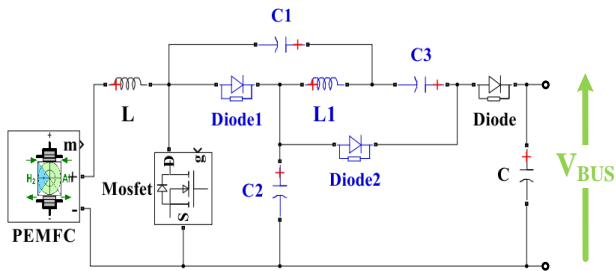
To realize a high voltage gain in DC/DC converters, Z-Source Impedance (ZSI) networks are also applied to boost the voltage due to the possibility of working in the shoot-through mode [1-63]. Zhang et al. [1-64] proposed a 3-Z-Network Boost converter that only utilized a single power switch; therefore easy to be controlled. The voltage gain could be higher than 9 times. Whereas, the maximum efficiency of the proposed converter was below 88% due to the high reverse recovery losses which are introduced by the high quantity of Si schottky diodes. A Boost Three Level DC/DC Synchronous Rectification Q-Z source converter (BTL-SRqZ) has been proposed by Zhang et al. [1-65]. The advantages such as lower voltage stress for the power semiconductors, the common ground between the input and output sides, as well as the wide range of voltage-gain with modest duty cycles [0.5, 0.75] for the power switches have been achieved. In order to compare the voltage gains of each topology more clearly, the voltage gain ratios are calculated as the function of duty cycles as presented in Fig.1.7.



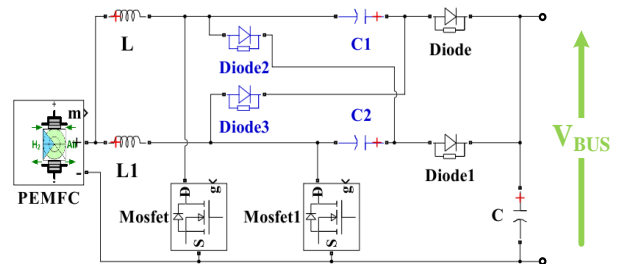
(a) Input-Parallel Output-Series DC/DC Boost converter by [1-55]



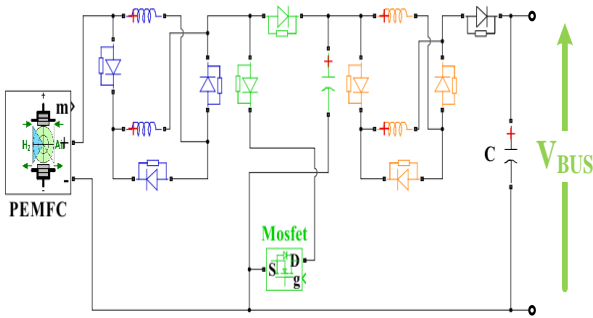
(b) Novel Cascade Boost converter by [1-57]



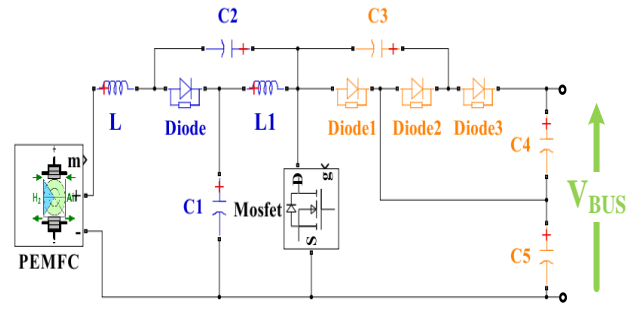
(c) Single-switch high step-up converter by [1-58]



(d) IBC combined VDC by [1-60] [1-61] [1-62]



(e) 3-Z Network based Boost converter by [1-64]



(f) Three level quasi-Z source based Boost converter by [1-65]

Fig.1.6 Schematics of non-isolated DC/DC converters for FCEVs application

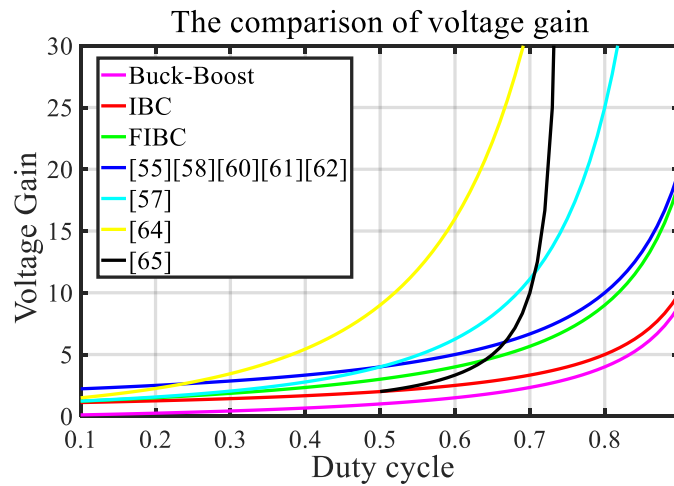


Fig.1.7. The comparison of voltage gain ratio of the power converters combined with auxiliary voltage-boost circuit in an ideal case (without taking into account the internal resistance of inductors)

1.3.5. Summary

Generally, for the fuel cell electric vehicle applications, the input current ripple is closely related to the lifespan of a fuel cell stack. DC/DC converters based on interleaved structure (IBC, FIBC, etc.) can reduce the current ripple of the power source. Benefiting from these specific topologies, the lifespan of fuel cell stack can be extended [1-4][1-66]. Furthermore, the electric stresses of each component can be reduced. The new hybrid system of Toyota Mirai has currently a 4-phase interleaved boost converter between the fuel cell system and the motor drive system to step up the

voltage from the fuel cell stack [1-14]. Benefiting from the developed converter, the voltage of the motor has been increased, the number of fuel cell single cells has been reduced, and the size and weight of the system have also been reduced. Therefore, the non-isolated DC/DC Boost converter based on interleaved structure is well-suited for FCEVs application.

Due to the limited inner space of a vehicle, a compact and light power conversion system is much more attractive. Generally speaking, the magnetic components (transformer and inductor) influence the total volume and weight significantly. High power application requires big transformers; however, the geometric sizing, the wound coil size and the difficulty of manufacturing will increase. Planar transformer technique is an attractive method to achieve a compact structure. Nevertheless, their prices are often very high, not really competitive for automotive applications. Towards non-isolated converters, to satisfy the requirement of low current ripple, big inductors are required. Interleaving structure is meaningful to reduce the current flowing through each inductor, thus the current ripple of inductor can be decreased. Another attractive approach is the coupled structure. A coupled inductor is a filter inductor having multiple windings and benefiting from this technique, the geometric sizing can be reduced and can induce the miniaturization of the heat dissipation system.

High switching frequency is also an effective method to reduce the magnetic component's volume. However, when the conventional Si semiconductor operates with high switching frequency ($>20\text{kHz}$), high switching loss and high reverse recovery losses will be separately introduced by MOSFET and diode. IGBT is possible for high current operating conditions, but to respect its inherent characteristics, the high switching frequency is not acceptable in many actual applications. SiC semiconductors have been developed rapidly in the last decade and already achieved commercialization. Low weight, small package, and interesting thermal performances made them attractive for FCEVs application. SiC MOSFET, which obtains high blocking voltage with low on-resistance and high speed switching with low capacitances, makes it possible to achieve higher system efficiency, reduce cooling requirements and increased power density. SiC Schottky diode, which features high repetitive peak reverse voltage, zero reverse recovery current and high-frequency operation ability, makes it available to achieve high efficiency, zero switching losses and reduction of heat sink requirements. In general, the selection of

SiC semiconductors can not only lead to a compact system but also increase system efficiency.

In consideration of the fuel cell characteristic (low-voltage high-current power source), a power converter which owns a high voltage gain ratio is more attractive. The isolated DC/DC boost converter can reach high voltage gains as discussed previously. However, compactness could be reduced. The conventional boost converter owns a medium voltage gain ratio. Different auxiliary circuits can be selected to increase the voltage gain significantly. Whereas a big quantity of additional components makes the system complicated, meanwhile the reliability of the system will be decreased by active components.

Efficiency is also an important factor to evaluate the performance of a power converter. Generally, power losses are mainly introduced by semiconductors and magnetic components. As analyzed previously, SiC-based semiconductor is an attractive approach to decrease power losses. GaN is another promising solution to improve the performances of semiconductors. Lower conduction resistance and higher switching frequency can be achieved by GaN semiconductor compared with the one based on SiC. However, the limitation of GaN semiconductor is that its blocking voltage is relatively low (<1000V) while higher cost is supported. Thus, currently, SiC semiconductor presents more advantages. On another side, core losses and copper losses are the dominating factors which decrease the efficiency of the magnetic component. Core loss is closely related to the core volume, the core material, and the geometric construction. High frequency is in favor of decreasing the core volume; hence, core loss can be reduced. Litz wire is suitable for high-frequency applications. Skin effect, which is an electromagnetic inherent characteristic, can be avoided by this special technique and thereby the copper losses can be reduced.

1.4.On-line EIS detection based on DC/DC converter connected to FC

Load cycling is the main characteristic that affects PEMFC lifespan in FCEVs applications [1-67]. During the load changing process, the current density of fuel cell stack changes frequently. As a complex electrochemical power device, relative humidity, temperature, gas flow rate, partial pressure, and other factors can influence the fuel cell system performance significantly, and various faults possibly occur to

PEMFC during the operating period. Short-circuit, which leads to the membrane and catalyst layer degradation, occurs in the microsecond or millisecond time range and is irreversible on-site [1-68]. Fuel starvation occurs in the millisecond or second time range, and will lead to the catalytic layer degradation [1-69]. Flooding and drying, which occur most commonly during operations, can lead to the performance reduction of the fuel cell system. Flooding can increase the fuel cell system degradation as a result of starvation and material alteration [1-70]; drying can result in pinhole degradation of the polymer membrane [1-71]. Both flooding and drying are entirely reversible by timely treatments. CO poisoning also leads to fuel cell system performance losses, and the reversibility closely relates to the exposure time, temperature and in-channel gas composition [1-72]. Fig.1.8 presents a schematization of the most frequent faults in a PEMFC based on different response times. Therefore, fault diagnostic methods are important to be developed in order to expand fuel cell lifespan. Different fault diagnostic methods for the fuel cell system are discussed in the subsections, and available studies of the on-line EIS detection are reviewed. A design guideline of the on-line EIS detection integrated with the fuel cell connected DC/DC converter is proposed.

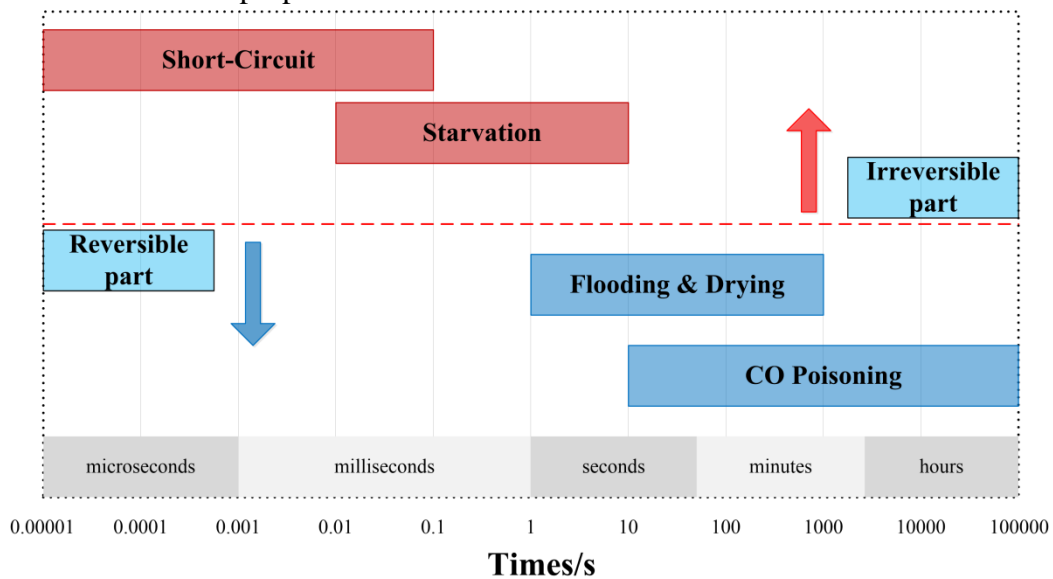


Fig.1.8. Illustration of the most common faults of a PEMFC based on response times [1-106]

1.4.1. Fault diagnostic methods of the fuel cell system

In recent years, diverse techniques and methods have been developed for PEMFC's diagnosis. These diagnostic approaches are generally classified into two types: model-based ones [1-73] and non-model based ones [1-74].

The model-based diagnosis is based on the development of a model which is capable of reflecting the status of the monitored system. Regarding the model-based approach, the fault diagnosis is commonly accomplished by residual evaluation where a residual inference is used for possible fault occurrence detection [1-75]. Hence, such a method is also referred to as the residual-based diagnosis. The physical multidimensional models are presented as a series of algebraic and/or differential equations. A high computational effort is required to obtain the solution, which means a near impossibility for real-time or on-line application [1-76]. The “black-box” model, which is directly derived from experiments, requests low computational efforts and is attractive for non-linear monitoring applications. However, this kind of model is strongly depending on available experiments which can reduce its genericity [1-77]. Therefore, the combination of these two model-based methods can simplify the characterization of a system, replace some complex mathematical equations, and reduce the requirement of computational effort [1-78].

Compared with model-based approaches, non-model based methods could be divided into knowledge-based and signal-based. The objective of this kind of methods is to detect, isolate, and classify different types of faults based on signal processing or heuristic knowledge or a combination of both. Artificial Intelligence (AI) methods have attracted a lot of attention in the field of diagnosis because they are effective in the identification of fault patterns without system structure knowledge. Neural network (NN), Fuzzy logic (FL), and Neural-fuzzy method are mostly used in this field. NN achieves the ability to handle noisy data [1-79] while FL is possible to handle the uncertainty in the system [1-80]. A neural-fuzzy method combines the advantages of NN and FL, and better generalization capability is obtained compared with NN [1-81]. Statistical methods such as Principle Component Analysis (PCA), Fisher Discriminant Analysis (FDA), Bayesian network (BN) and others are the most frequently used variable dimension-reduction methods to extract the most discriminating features from a huge amount of data [1-82]. Signal processing methods are effective to analyze oscillations of the detected signals. Fast Fourier Transform (FFT) and Wavelet Transform (WT) are commonly used and they can provide a view of signals in the frequency domain [1-83]. However, the main drawback of non-model-based methods is the requirement of huge amounts of data sets that originally acquired on a system in day-to-day use or on a dedicated laboratory test bench. Moreover, these data sets must be acquired under both normal and targeted

fault conditions [1-3].

Towards FCEVs applications, the requirement of the fuel cell diagnostic method can be summarized as high accuracy, high robustness, quick response, high sensitivity, and good versatility. At the same time, the diagnostic method is also requested to have the possibility of on-line or onboard application, and with minimum dependence of sensor or other additional equipment.

1.4.2. The applications of EIS

Electrochemical impedance spectroscopy (EIS) is established as a powerful characterization tool to detect different failure mechanisms occurring in the fuel cell system. Impedance spectra can help to characterize a cell in a much more efficient mode than just analyzing the polarization curve [1-84]. Many works highlight the use of the EIS technique for the fuel cell parameter identification, which is a kind of model-based diagnosis method and is effective for both fault detection and isolation [1-85]. EIS technique is also treated as an efficient means for non-model based diagnosis method because it helps a lot for pre-processing the original data sets and for decreasing the misclassification rate [1-86]. Some typical applications of the EIS technique as a fault diagnostic approach for the fuel cells are presented in Table.1.5.

Table.1.5 Applications of EIS technique as a fault diagnostic method for the fuel cells

Ref.	Description of the method	Fault types	EIS achievement	On/off-line
[1-87]	Use EIS estimate the high-frequency impedance data and the parameters characterizing the cathode reaction of H ₂ /air fed PEMFC.	No information.	Labview program based.	Off-line & In-lib
[1-88]	Use EIS technique as the diagnostic approach to two PEMFC failures associated with low-frequency current ripple.	Cathode flooding; Membrane drying.	EIS spectrometer (Zahner, IM6ex). Range from 2kHz to 0.03Hz.	Off-line & In-lib
[1-89]	Use EIS study impacts of operating conditions on the effects of chloride contamination on PEMFC.	Increase charge transfer resistance and mass transfer resistance.	EIS spectrometer (Teledyne test station). Range from 3kHz to 0.1Hz.	Off-line & In-lib
[1-90]	Use EIS study DMFC's electrochemical process and degradation reasons.	Ru's dispersing; MEA's swelling;	VMP2 electrochemical	Off-line & In-lib

		Cathode's water flooding.	workstation (Bio-logic).	
[1-91]	Combine EIS and SANS techniques to study water management of PEMFC in operando at sub-zero temperatures.	Member dehydration.	Bio-Logic VSP impedance meter.	Off-line & In-lib
[1-92]	Use EIS reveal the degradation phenomena caused by cell polarity reversal due to fuel starvation of PEMFC.	Fuel starvation.	Frequency response analyzer from Solartron Model 1250.	Off-line & In-lib
[1-93]	Use spatial EIS and current distribution model study the effect of low concentration CO poisoning of Pt anode in PEMFC.	Anode CO poisoning.	Hawaii Natural Energy Institute's (HNEI) segmented cell system.	Off-line & In-lib
[1-94]	Use EIS study the influence of CO and methanol vapor contamination of the anode gas in a HT-PEMFC.	Anode poisoning (CO and methanol vapor).	Gamry Reference 3000 instrument.	Off-line & In-lib
[1-95]	Use EIS assess the effect of different MEA conditionings for PEMFC performance.	In fact, different operating conditions of PEMFC have been studied in this paper. But they can't be called as faults.	Fuel cell test station: Scribner, 850e	Off-line & In-lib
[1-96]	Use EIS analyze geometrical features of PEMFC based on computational fluid dynamics.	No information.	Electronic load CHROMA 63600. Range from 20kHz to 0.05Hz.	Off-line & In-lib

Mainka et al. [1-87] made a discussion on the estimation of impedance parameters of H₂/air fed PEMFC. The parameters characterizing charge separation and transport process at the cathode can thus be estimated with the high-frequency impedance data, independently of the oxygen transport model. Consequently, even in the absence of fully validated oxygen transport impedance, EIS can be used as an alternative method for the estimation of the parameters characterizing the cathode reaction. Kim et al. [1-88] dealt with a diagnosis of cathode flooding and membrane drying associated with a low-frequency ripple current of a PEMFC based on EIS analysis. In this study, it has been shown that a low-frequency ripple current more accelerates the PEMFC degradation with these two PEMFC failures. Li et al. [1-89] used EIS as a diagnostic tool in purpose of exploring changes in cell component resistances during the contamination tests because the chloride contaminated fuel

and/or air streams in an operating PEMFC can cause significant adverse effects on fuel cell performance and durability. Wang et al. [1-90] have successfully investigated direct methanol fuel cell's (DMFC's) electrochemical process in situ using the EIS method. The results showed that Ru's dispersing, membrane's swelling and water flooding were the main reasons resulting in performance decline. Morin et al. [1-91] combined Small-Angle Neutron Scattering (SANS) and EIS techniques to study the water management in an operating PEMFC at sub-zero temperatures. It was shown that the fuel cell operation at sub-zero temperature can be conducted in operando by SANS meanwhile the variation of membrane water content can be confirmed by EIS technique with different current density. Travassos et al. [1-92] used the EIS technique to report the degradation phenomena caused by cell polarity reversal due to the fuel starvation of an open cathode membrane electrode assembly. Reshetenko et al. [1-93] studied the effects of CO on PEMFC performance with a segmented cell by the spatial EIS technique. The spatial EIS data were analyzed using the equivalent electric circuits approach. A current distribution model and the EIS interpolation method were applied for detailed analysis. Jeppesen et al. [1-94] have presented a comprehensive mapping of electrochemical impedance measurements under the influence of CO and methanol vapor contamination of the anode gas in a high-temperature PEMFC (HT-PEMFC), at varying load current. Zhiani et al. [1-95] have studied the effects of three different commonly used on-line membrane-electrode assembly (MEA) conditioning procedures on the final MEA performance, and the performance of activated PEMFCs was investigated under different operation conditions (low and high relative humidity, low and high cell pressure and low and high oxidant concentration) by EIS technique. Baricci et al. [1-96] have made use of EIS for the design of PEMFC's flow field geometry because EIS allows separating the effect of electric resistance due to contact between Gas Diffusion Layer (GDL) and bipolar plates, electrode kinetics oxygen transport under the rib. Advanced understanding of EIS features that has been detailed in this work could be also beneficial for the implementation of EIS as a diagnostic measurement on-board to manage the operating conditions and detect faults.

Although EIS has already been widely applied for the fuel cell in-lab/off-line applications, the acquisition of data-sets is mainly based on impedance meter equipment and fuel cell test station which are impossible for onboard/on-line applications. Thus, the realization of on-line EIS detection is quite important and

urgent nowadays for FCEVs application.

1.4.3. On-line EIS realization based on the power converter

Classically, a DC/DC converter is considered for the connection between the fuel cell stack and the DC bus, in order to realize the power conversion. The ripple frequency of a DC/DC converter is just the same as the switching frequency of the power switching semiconductors such as power MOSFET. This provides a favorable crucible for the fuel cell system diagnosis without any other additional equipment to respect the limited space in a FCEV [1-99]. Table.1.6 presents a review of the realizations of EIS detection based on actual power converters. As common electrochemical and electrostatic energy storage devices, battery and super-capacitor are also be analyzed with this approach.

Table.1.6 Comparisons of EIS detection based on the practical converter connected to the power source

Application field	Converter type	Ref.	Control strategy & Controlled object	Input current ripple	Perturbation injection method
PEMFC	Boost	[1-98]	PID controller.	High	--
		[1-101]	Dual-loop PI controller. DC bus voltage and input current.		Injected current or voltage perturbation.
		[1-102]	Dual-loop PI controller.		--
	IBC	[1-24]	Sliding-Mode controller. DC bus voltage and inductor current.	Low	Injected current perturbation.

	Full bridge	[1-99]	PI controller. DC bus voltage.	High	Injected current perturbation.
		[1-7]	PI controller. DC bus voltage.		Injected current perturbation.
Battery	Boost	[1-103]	--	High	Injected duty cycle perturbation.
	Full bridge	[1-100]	Dual-loop PI controller. Output voltage and output current.		--
PEMFC & EDLC	Boost	[1-104]	Dual-loop PI controller. DC bus voltage and source voltage.		Injected voltage perturbation.
DC Capacitive Network	Buck-Boost	[1-105]	Dual-loop PI controller. DC bus voltage and battery current.	--	Injected current perturbation.

Narjiss et al. [1-99] and Depernet et al. [1-7] consisted of on-line detection of fuel cell dysfunction thanks to the selected full bridge converter without additional hardware component. The switching frequency was relatively high (50kHz), but the semiconductors were conventional Si material which increased switching losses at this operating condition. Doan et al. [1-100] have designed an intelligent charger which was a full bridge converter combined with a controlled rectifier, and the on-line battery diagnosis function has been realized. The relationship between the perturbation signal frequency and the control loop bandwidth was mentioned. The nonlinear least square fitting algorithm was utilized to estimate battery parameters.

Conventional Boost converter was selected by [1-98] [1-101] [1-103] and [1-102] to realize EIS detection of electrochemical sources. The method utilized by Hinaje et al. [1-98] relied on the estimation of the internal resistance calculated from the voltage and current ripples, thus, on-line humidification diagnosis of PEMFC was realized.

However, the real and imaginary parts of the AC impedance cannot be analyzed separately. Bethoux et al. [1-101] have studied the stability of the control system during EIS detection. Relied on this study, injection of the perturbation signal into the fuel cell current reference or the DC bus voltage reference is depending on its frequency. Hong et al. [1-102] detected EIS of PEMFC based on two parallel Boost converters and a battery was connected to DC bus directly. To control the input current, a control scheme of two-degrees of freedom was put forward. In the outer control loop, a PI controller and a look-up table were used to set the reference value of the output current. The look-up table got the output power of the stack according to the reference output current. In the inner loop, the output current was controlled based on the state space model of the converter. To decrease the input current overshoot, the feedforward control was added to the duty cycle. The output voltage of this converter was determined by the battery. Varnosfaderani et al. [1-103] presented an on-line impedance estimation approach for the battery application. A small component representing a low-frequency component was directly imposed to the duty cycle when the system operated under steady state. The ripple and harmonics of battery voltage and current were separately analyzed.

Depending on the study of Katayama et al. [1-104], the diode of the conventional Boost converter was replaced by a MOSFET. The proposed circuit was based on two power sources: PEMFC and EDLC. Each power source was connected with its own Boost converter. The control strategy of EDLC converter is DC bus voltage control. The control strategy of PEMFC converter is dual loop voltage control: the outer loop is EDLC voltage control, and the inner loop is FC voltage control. During the diagnosis mode, a sinusoid signal with a certain frequency and amplitude is injected to the FC converter reference. However, the perturbation of the DC bus voltage has been introduced while the input current ripple was high. Depernet et al. [1-105] integrated the EIS detection functionality of lead-acid batteries with a Buck-Boost converter for storage management of standalone power plant.

As discussed previously, input current ripple influences fuel cell stack's lifespan a lot. However, among these references, conventional DC/DC (Boost, Buck-Boost) or DC/AC/DC (Full-Bridge) converters were mainly considered. Thus, the fuel cell current ripple was still kept at a high level. Furthermore, Si semiconductors were utilized which means poor performances under high switching condition, especially high switching losses of MOSFET and high reverse recovery losses of Schottky diode.

In [1-99], [1-105], [1-103] and [1-7], open loop control were applied during EIS detection process. The stability of DC bus voltage cannot be ensured during this period.

Wang et al. [1-24] currently proposed on-line detection of impedance spectroscopy for PEMFC application based on connected electric power converter. The proposed converter based on high switching frequency, SiC semiconductors and inverse coupled inductors is an innovative solution to settle the problem of regulating PEMFC voltage to satisfy the voltage requirement of the fuel cell electric vehicle DC bus. Compared with the existing studies, the proposed strategy has been verified by FC stack Randles model in a wide range of frequencies (maximum 10kHz). Besides, the selected Sliding-Mode Control can well regulate the fuel cell current and DC bus voltage and realize close loop control either under nominal operating conditions or disturbed conditions.

In general, these features are presented in Table.1.7 are essential for a DC/DC converter, which is focused on FCEV application meanwhile integrated with EIS detection ability. Therefore, this study focus on the design and control of a non-isolated DC/DC boost converter combined with low input current ripple, low volume, low weight, high efficiency and good thermal performance for FCEV application. Furthermore, on-line EIS detection method based on FC connected power converter will also be studied.

Table.1.7 Requirements for a DC/DC converter focused on FCEV application combined with EIS on-line detection functionality

Required feature	Approaches
High reliability	<ul style="list-style-type: none"> ● Use proper topology to reduce input current ripple in purpose of extending fuel cell stack's lifespan; ● Select proper semiconductor which achieves good thermal performance; ● Realize closed loop control during EIS detection period to ensure the stability of DC bus voltage.
High power density	<ul style="list-style-type: none"> ● Optimize magnetic component structure to minimize total volume and weight; ● Select high switching frequency to minimize magnetic component; ● Replace power IGBT module by advanced power MOSFET to reduce semiconductors' volumes, meanwhile compact heat sink can be utilized.

High energy efficiency	<ul style="list-style-type: none"> ● Semiconductor based on SiC material is attractive to reduce power losses; ● Auxiliary soft-switching circuit can be selected to reduce switching losses; ● Magnetic component with compact structure is promising to decrease core losses.
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1.5. Conclusion

In this chapter, a review focusing on the integration of EIS detection functionality in DC/DC converter for FCEV applications is presented.

The non-isolated DC/DC converter and the isolated DC/AC/DC converter are commonly considered. The characteristics like high compactness, simple structure and low cost are achieved by the non-isolated topologies. However, the voltage gain ratio of this type of topology is relatively low. Although different auxiliary circuits can be selected to increase the voltage gain ratio, the complexity of the converter will be increased while the reliability will be decreased due to the application of additional components. High voltage gain ratio can be achieved easily by the isolated converters due to the magnetic transformer. The voltage gain ratio of this kind of topology is closely related to the turn ratio of transformer. But the compactness of the converter will be decreased.

Depending on the study of literatures, non-isolated DC/DC boost converter based on the interleaved structure is attractive to reduce the input current ripple while the lifespan of the power source can be extended. The redundancy of the converter can also be improved by this specific structure. In order to increase voltage gain ratio and gain volume and weight, the magnetic component based on coupled structure is attractive to be applied. To decrease the power losses introduced by the semiconductors, the ones manufactured by Wide Band-Gap (WBG) materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are treated as a promising solution. According to existed commercialized power MOSFETs based on WBG materials, SiC-based one owns the ability for high voltage (900V~1700V) applications compared with power MOSFET based on GaN (<650V). Better thermal performance, lower switching losses and lower conduction losses can be obtained by using power switches based WBG materials. The efficiency can be improved and the cooling system can be simplified.

As discussed in the previous section, fault diagnosis is essential for the fuel cell system both in the laboratory and in actual applications. Electrochemical Impedance Spectroscopy (EIS) is one of the most promising diagnostic approaches to handle this issue. Due to the limited inner space of a vehicle, on-line EIS detection functionality integrated with the DC/DC converter which is connected to the fuel cell stack is a promising approach. Benefiting from this method, no additional equipment is required. Some efforts have been done by others to realize this diagnostic method as demonstrated in this paper. Nevertheless, the topologies utilized in these researches were the conventional ones which didn't achieve the ability to reduce the input current ripple. Meanwhile, in some studies, the converters were in open-loop control mode during on-line EIS detection processes. The stability of DC bus voltage can't therefore be ensured.

Therefore, concerning the fuel cell electric vehicle applications, a DC/DC boost converter which achieves low input current ripple, compact structure, high voltage gain ratio, high efficiency and high redundancy is attractive for the practical application. After the power conversion has been realized, the integration of the EIS detection process with the proposed power conditioning unit is a promising approach to realize on-line water management of the fuel cell stack without any additional equipment.

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Chapter 2: Interleaved Boost Converter for FCEV

2.1. Introduction

Fuel Cell Electric Vehicles (FCEV) have physical constraints such as volume and weight under limited cost and expected lifetime. There is a need of high voltage ratio for the DC/DC converter connected between the FC and the electric motor drive on the DC bus because typically battery packs are around of 400~600 volts. Although the isolated DC/DC converter owns high voltage gain, this kind of converter is not quite suitable for FCEV application as the requirement of magnetic transformer can lead to the increase of weight and volume. In addition, it is necessary to have a low input current ripple at the DC/DC converter in order to maximize the FC lifetime [2-1]. The average power of EV is much lower than a peak power during accelerating or braking. Therefore, the converter must provide a high efficiency over a wide load range. Multi-phase interleaved Boost Converter (IBC) may have a physical volume and weight lower than single-phase converter, like a Boost Converter (BC) for example. Adding more phases increases the benefits of interleaving but at a certain number of phases, the benefits are limited with increasing converter complexity and cost. In this chapter, a 6-phase IBC based on SiC semiconductors with inverse coupled inductors is proposed. This topology will be contrasted and compared to the conventional IBC solution, aiming to improve performance figures related to the inductor and capacitor volume versus weight, input current ripple, DC bus voltage ripple, as well as efficiency. This analysis will permit to evaluate the benefits of increasing phases and choose the most suitable topology among other proposed ones in order to achieve desired objectives from specifications.

2.2. System specifications and proposed topology

Compared with conventional BC, IBC is more attractive for FCEV application benefiting from the interleaved input structure. The current stress of each power switch can be decreased significantly while the input current ripple can be reduced importantly which is closely related to the lifespan of FC stack. The N -phase IBC

with uncoupled inductors and the N -phased IBC based on inverse or direct coupled inductors of cyclic cascade structure are separately presented in Fig.2.1.

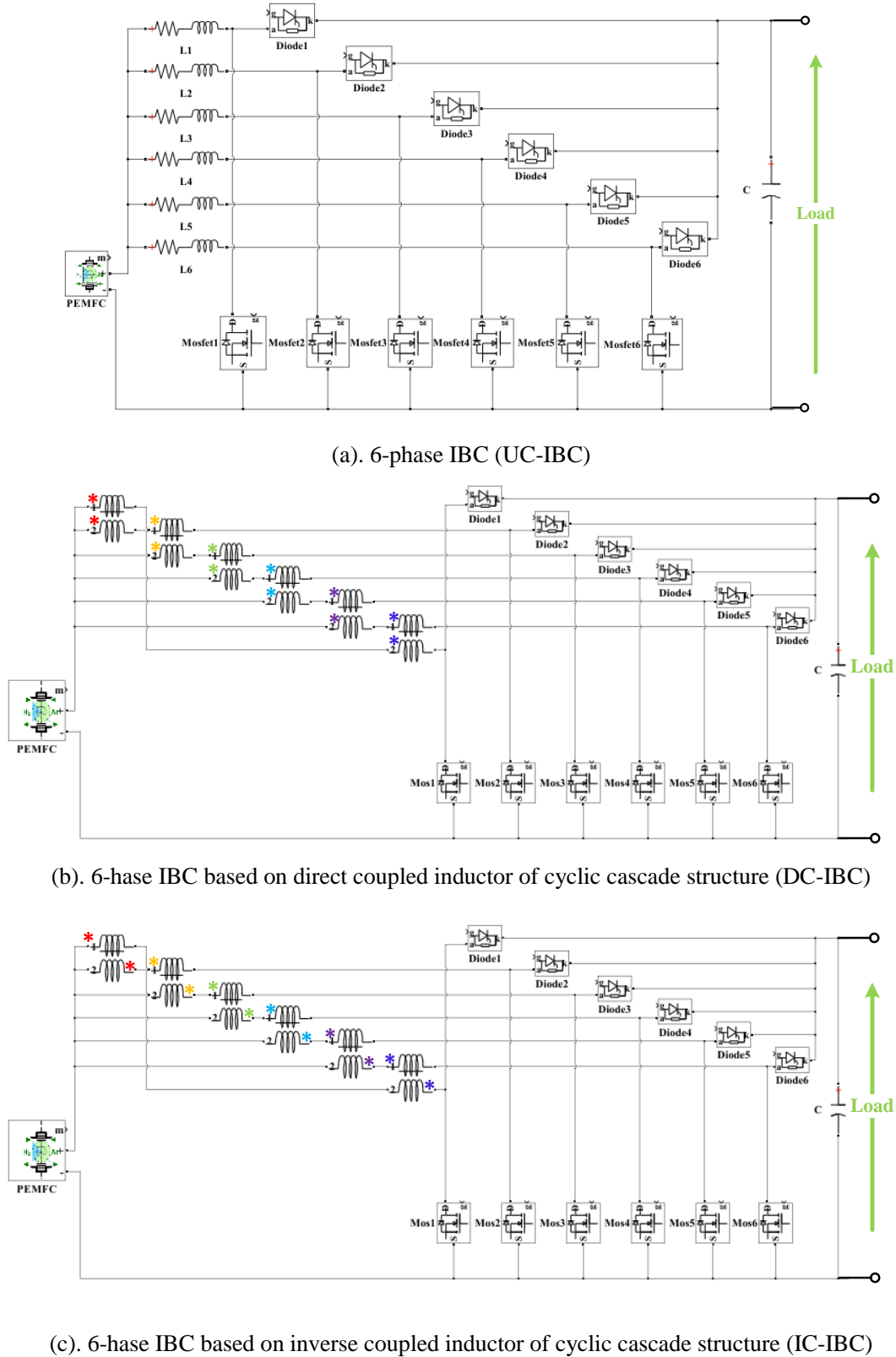


Fig.2.1 Topologies of IBC based on different structures of inductors

Another aspect of the current ripple is that it not only affects the FC lifespan, but also its capacity and fuel consumption [2-2]. It has been suggested that the current ripple should be limited to less than 10% of the nominal FC current [2-3]. In our study, the system specifications are presented in Table.2.1.

Table.2.1 Specifications of a DC/DC power converter unit for FCEV

Parameter	Symbol	Value	Unit	
Input voltage	V_{in}	70	V	
Nominal power	P_N	21	kW	
Output voltage	V_{out}	350	V	
Output voltage ripple	ΔV_{out}	$<10\% * V_{out}$	V	
Inductor current ripple	Δi_L	$<20\% * I_L$	A	
Switching frequency	UC-IBC	f_{s1}	100	kHz
	DC-IBC	f_{s2}	100	
	IC-IBC	f_{s3}	100	

2.3. The fuel cell current evaluation

The mathematical expressions for input current ripple and DC bus voltage ripple of the proposed topology are based on the following assumptions:

1. Resistances of inductor and capacitor are negligible;
2. Stray inductor and capacitor are negligible;
3. Power switches are ideal;
4. Passive components are identical;
5. The phase shift for the control order of power switches is $360^\circ/N$;
6. The converter operates in continuous conduction mode (CCM).

The duty cycle of N -phase IBC equals to conventional BC and can be expressed by (2.3.1).

$$D = \frac{V_{out} - V_{in}}{V_{out}} \quad (2.3.1)$$

The input FC current dynamic response of N -phase IBC is given by (2.3.2).

$$\frac{di_{FC}}{dt} = \frac{di_{L1}}{dt} + \frac{di_{L2}}{dt} + \dots + \frac{di_{Ln}}{dt} \quad (2.3.2)$$

Depending on some other studies [2-4] [2-5], the ratio of the input current ripple to the inductor current ripple of N -phase UC-IBC as a function of duty cycle can be expressed by (2.3.3).

$$\frac{\Delta i_{FC}}{\Delta i_L} = \frac{[N \times D - (x-1)] \cdot [x - N \times D]}{N \times D \times (1-D)}, \quad \frac{x-1}{N} < D < \frac{x}{N}, \quad x=1,2,\dots,N \quad (2.3.3)$$

Here, only five groups of IBC (from 2-phase to 6-phase) are presented. According to these five groups' equations, the relationships between I_{FC} and I_L as the function of duty cycle are achieved for different topologies as detailed in Fig.2.2.

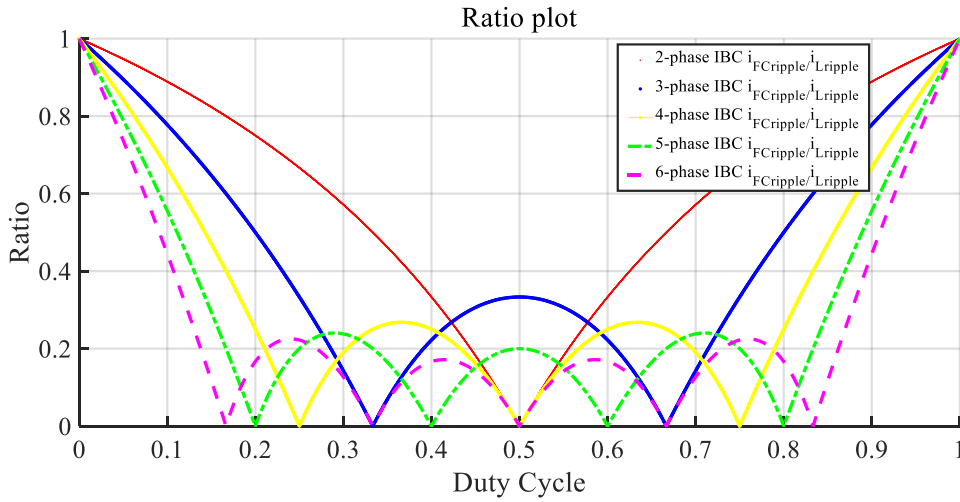


Fig.2.2 he relationship between I_{FC} and I_L for N -phase IBC with uncoupled inductors

The operating principle of IBC with coupled inductors as proposed previously is much more complicated than the conventional one. The highly non-linear characteristic of coupled inductors introduces more processes. In fact, during each condition, the state equations are not the same to each other's. In other words, it is essential to obtain these state equations between each turning point in purpose of better understanding the operating processes of coupled inductor meanwhile the relationship between the input current and the inductor current.

The relationships between FC current ripple and inductor current ripples for IBC based on coupled inductors (from 2-phase to 6-phase) are presented below. The coupled inductors are combined by cyclic cascade structure. In these equations [2-6] [2-7], k stands for the coupling coefficient which equals to M/L_s (M is the mutual inductance and L_s is the self-inductance).

- 2-phase IBC based on coupled inductor as (2.3.4):

$$\frac{\Delta i_{FC}}{\Delta i_L} = \begin{cases} 2 - \frac{(1+k)}{(1-D(1-k))}, 0 < D < \frac{1}{2} \\ \frac{(2D-1)(1-k)}{k(1-D)+D}, \frac{1}{2} < D < 1 \end{cases} \quad (2.3.4)$$

- 3-phase IBC based on coupled inductor as (2.3.5):

$$\frac{\Delta i_{FC}}{\Delta i_L} = \begin{cases} \frac{(1-3D)(2-k)}{(2+k)-D(2-k)}, 0 < D < \frac{1}{3} \\ \frac{(2-k)(3D-2)(1-3D)}{k(2-3D)+3D^2(k-2)+6D}, \frac{1}{3} < D < \frac{2}{3} \\ \frac{(3D-2)(2-k)}{2k+D(2-k)}, \frac{2}{3} < D < 1 \end{cases} \quad (2.3.5)$$

- 4-phase IBC based on coupled inductor as (2.3.6):

$$\frac{\Delta i_{FC}}{\Delta i_L} = \begin{cases} \frac{(4D-1)}{(D-1)}, 0 < D < \frac{1}{4} \\ \frac{(16D^2-8D)}{(4D^2-11D-1)}, \frac{1}{4} < D < \frac{2}{4} \\ 4 - \frac{(18D-8)}{((2D-1)(D+2))}, \frac{2}{4} < D < \frac{3}{4} \\ 4 - \frac{12}{(4D+3)}, \frac{3}{4} < D < 1 \end{cases} \quad (2.3.6)$$

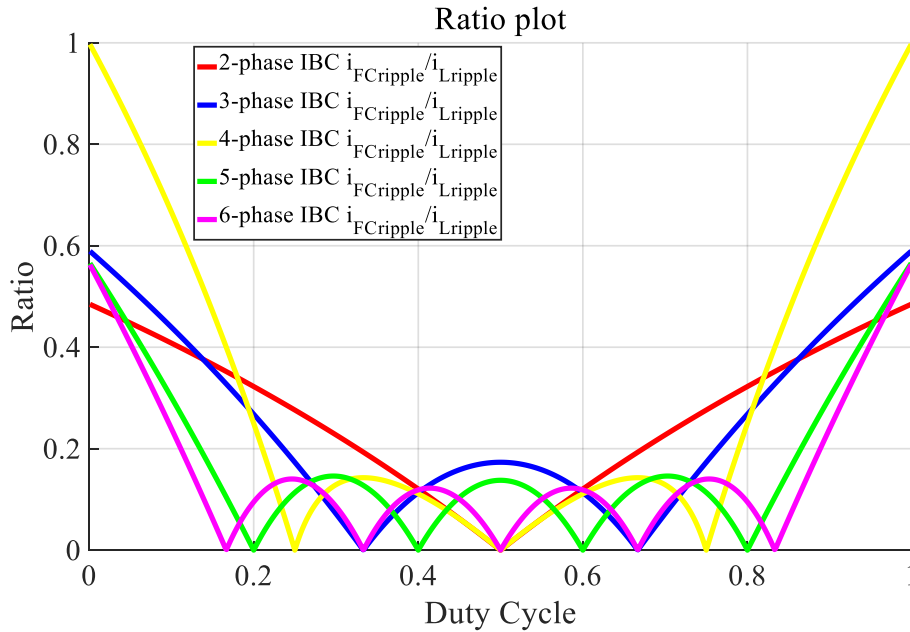
- 5-phase IBC based on coupled inductor as (2.3.7):

$$\frac{\Delta i_{FC}}{\Delta i_L} = \begin{cases} \frac{(5D-1)(k^2+2k-4)}{(k+2)(k-2)(D-1)+2k(D+1)}, 0 < D < \frac{1}{5} \\ \frac{(-25D^2+15D-2)k^2+(-50D^2+30D-4)k+100D^2-60D+8}{(-5D^2+15D-2)k^2+(-10D^2+10D-4)k+20D^2-20D}, \frac{1}{5} < D < \frac{2}{5} \\ \frac{(-25D^2+25D-6)k^2+(-50D^2+50D-12)k+100D^2-100D+24}{(-5D^2+15D-2)k^2+(-10D^2+10D-4)k+20D^2-20D}, \frac{2}{5} < D < \frac{3}{5} \\ \frac{(-25D^2+35D-12)k^2+(-50D^2+70D-24)k+100D^2-140D+48}{(-5D^2+15D-2)k^2+(-10D^2+10D-4)k+20D^2-20D}, \frac{3}{5} < D < \frac{4}{5} \\ \frac{(4-5D)k^2+(8-10D)k+20D-16}{(-D) \cdot k^2+(4-2D)k+4D}, \frac{4}{5} < D < 1 \end{cases} \quad (2.3.7)$$

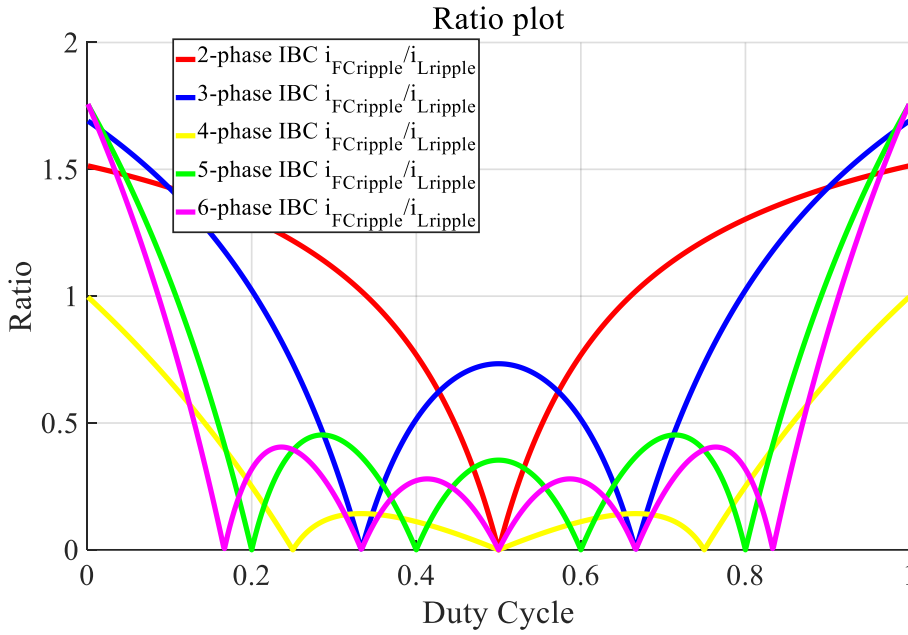
- 6-phase IBC based on coupled inductor as (2.3.8):

$$\frac{\Delta i_{FC}}{\Delta i_L} = \begin{cases} \frac{(6D-1)k^3 + (1-6D)k^2 + (4-24D)k + 24D-4}{Dk^3 + (3-D)k^2 - 4Dk + 4D-4}, 0 < D < \frac{1}{6} \\ \frac{(18D^2-9D+1)k^3 - (18D^2-9D+1)k^2 - 4(18D^2-9D+1)k + 72D^2-36D+4}{(3D^2-6D+1)k^3 - (3D^2-9D)k^2 - (12D^2-12D+2)k + 12D^2-12D}, \frac{1}{6} < D < \frac{2}{6} \\ \frac{(18D^2-15D+3)k^3 - (18D^2-15D+3)k^2 - (72D^2-60D+12)k + 72D^2-60D+12}{(3D^2-6D+1)k^3 - (3D^2-3D-2)k^2 - (12D^2-12D+2)k + 12D^2-12D}, \frac{2}{6} < D < \frac{3}{6} \\ \frac{(18D^2-21D+6)k^3 - (18D^2-21D+6)k^2 - (72D^2-84D+24)k + 72D^2-84D+24}{(3D^2-2)k^3 - (3D^2-3D-2)k^2 - (12D^2-12D+2)k + 12D^2-12D}, \frac{3}{6} < D < \frac{4}{6} \\ \frac{(18D^2-27D+10)k^3 - (18D^2-27D+10)k^2 - (72D^2-108D+40)k + 72D^2-108D+40}{(3D^2-2)k^3 - (3D^2+3D-6)k^2 - (12D^2-12D+2)k + 12D^2-12D}, \frac{4}{6} < D < \frac{5}{6} \\ \frac{(6D-5)k^3 + (5-6D)k^2 + (20-24D)k + 24D-20}{(D-1)k^3 - (2+D)k^2 + (4-4D)k + 4D}, \frac{5}{6} < D < 1 \end{cases} \quad (2.3.8)$$

Obviously, compared with conventional N -phase IBC, the operating processes of N -phase IBC based on cyclic cascade coupled inductors are much more complicated. Depending on these analyses, Fig.2.3 (a) and (b) stand for the ratios between FC current ripples and inductor current ripples separately for direct and inverse coupled inductors. According to these figures it is shown that the maximum ratio of 4-phase IBC whether based on direct coupled inductors or inverse coupled inductors equals to one. For the other IBCs, their maximum ratios change along with the coupling ways. DC-IBC has a maximum ratio lower than one while IC-IBC's maximum ratio is higher than one.



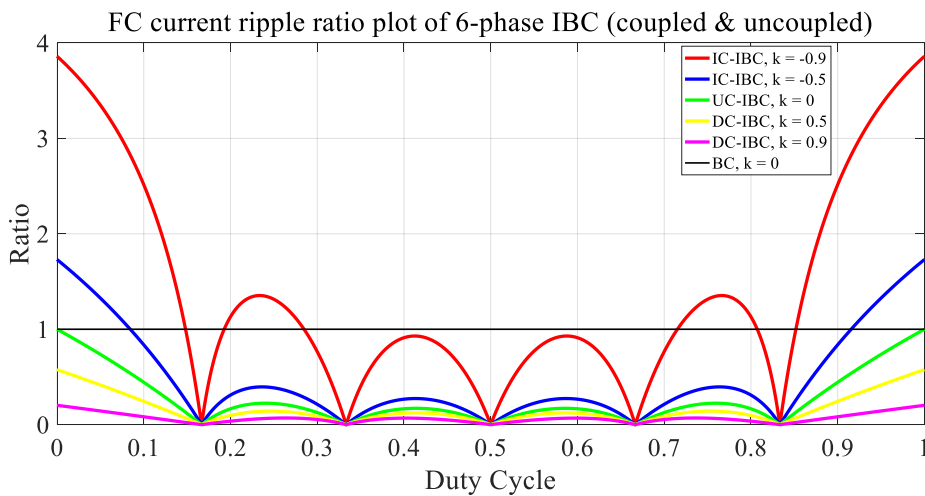
(a). $\Delta i_{FC}/\Delta i_L$ of N -phase DC-IBC



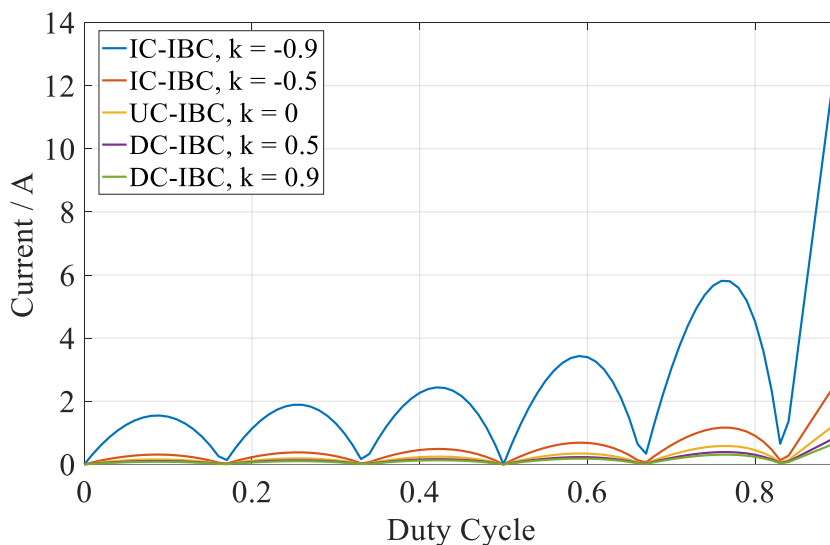
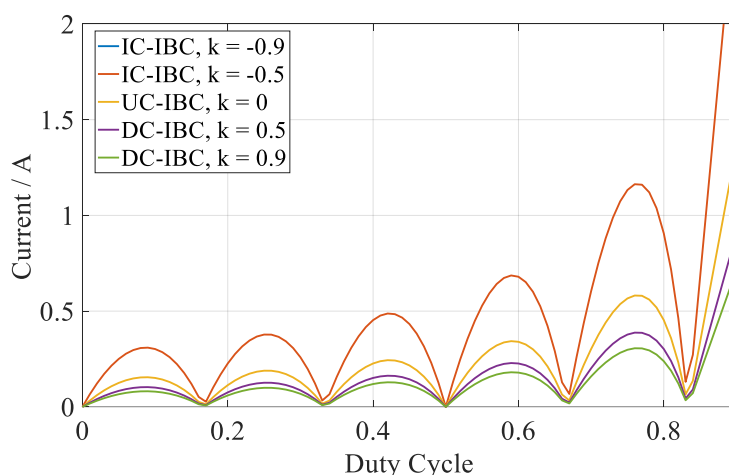
(b). $\Delta i_{FC}/\Delta i_L$ of N -phase IC-IBC

Fig.2.3 The ratios between FC current ripple and inductor current ripples for coupled IBC topologies

In this study, the 6-phase IBCs are mainly focused as discussed in previous chapter. As the current ripple ratio changes along with both duty cycle and coupling coefficient, it is quite important to find out the influence that can be led by these two factors. The analysis results are illustrated in Fig.2.4. Fig.2.4 (a) presents the change of ratio caused by different duty cycle and coupling coefficient. Fig.2.4 (b) presents the change of FC current ripple based on different duty cycle and coupling coefficient. The theoretical analysis is done under the nominal operating point.



(a). Ratio plot of 6-phase UC-IBC, DC-IBC, and IC-IBC

(b). I_{FC} ripple of 6-phase UC-IBC, DC-IBC, and IC-IBC

(c). Zoom of (b)

Fig.2.4 The comparison analysis of input current ripple among UC-IBC, DC-IBC, and IC-IBC

based on different duty cycle and coupling coefficient

According to Fig.2.4 (a), UC-IBC is treated as the special condition that the coupling coefficient equals zero as the green curve. The ratio of BC always keeps at one due to its construction's inherent characteristic. Two different coupling coefficients (0.5 and 0.9) have been selected both for DC-IBC and IC-IBC. Obviously, we can find that the ratio of IC-IBC is always bigger than the ratio UC-IBC while the ratio of DC-IBC changes just in opposite tendency. The most significant result is that the ratio of IC-IBC can be bigger than one. In this way, the FC current ripple can be bigger than the inductor current ripple in specific condition. However, the ratio can

only reflect the relationship between FC current ripple and inductor current ripple. In order to obtain the actual value of FC current ripple, Fig.2.4 (b) is given. The FC current ripple of UC-IBC and DC-IBC can be kept below 5A while the one of IC-IBC can reach 15A when the duty cycle equals 0.9 and the coupling coefficient equals 0.9. Nevertheless, it is also possible for IC-IBC to achieve a low FC current ripple once the duty cycle is kept below 0.85.

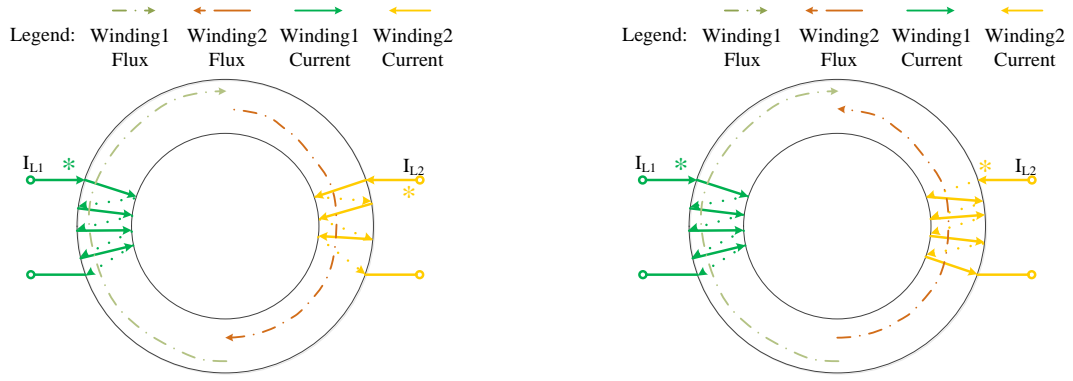
Hence, it can be concluded that DC-IBC's FC current ripple is lower than the one of UC-IBC and IC-IBC; but, the FC current ripple of IC-IBC is still acceptable if suitable coupling coefficient and duty cycle values are selected.

2.4. Inductor design process

In actual FCEV application, the volume and weight of a power converter have to be reduced due to the limited inner space and the requirement of energy efficiency. The magnetic component can influence a lot the total volume and weight of a converter. Hence, in this section, the inductor design process of UC-IBC, DC-IBC, and IC-IBC will be addressed. Taking the volume, weight, complexity of installation and core material specification (saturation magnetic flux, core loss, etc.) into consideration, toroid magnetic cores based on the iron powder material are selected.

The physical structure and electrical structure of DC-IBC and IC-IBC are illustrated in Fig.2.5 (a) and (b). Due to different winding configurations, the magnetic fluxes flow in different ways inside these two coupled inductors. For the direct coupled inductor, the magnetic fluxes of two windings flow in same direction; on the other hand, the magnetic fluxes flow inversely inside the inverse coupled inductor. That is to say, it is possible to cancel DC magnetic flux by the inverse coupled inductor and only AC magnetic flux exists. In this way, a significant core losses' reduction will be obtained, and the magnetic core's volume can also be decreased.

In this section, the comparative analysis of magnetic core's volume is mainly addressed. Meanwhile, the design process of magnetic core is also proposed for UC-IBC, DC-IBC, and IC-IBC.



(a) Inductor's physical structure of DC-IBC (left) and IC-IBC (right)



(b) Inductor's electrical structure of DC-IBC (left) and IC-IBC (right)

Fig.2.5 The coupled inductor of DC-IBC and IC-IBC

The inductor volume is closely related to inductor value, current value, current ripple level and maximum flux density. According to [2-8], the core geometrical constant K_g is a figure-of-merit that describes the effective electrical size of magnetic cores. The minimum K_g (K_{gmin}) can be used to decide the required minimum core geometrical constant. (2.4.1) and (2.4.2) are the design formulas of K_{gmin} for coupled magnetic core and uncoupled magnetic core, separately. The necessary parameters are presented in Table.2.2.

$$K_{g \min_coupled} = \frac{\rho_{cu} \times L_M^2 \times i_{M,sat}^2 \times (I_{L1rms} + I_{L2rms})^2}{B_{sat}^2 \times K'_u \times P'_{cu_tot}} \quad (2.4.1)$$

$$K_{g \min_uncoupled} = \frac{\rho_{cu} \times L^2 \times I_{Lmax}^2}{B_{sat}^2 \times K'_u \times R'_L} \quad (2.4.2)$$

Table.2.2 The necessary parameters to calculate K_{gmin}

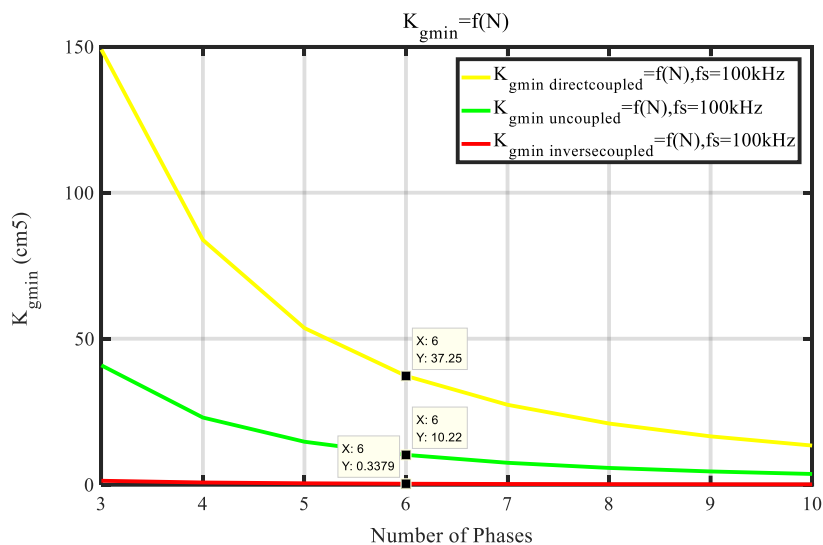
Symbol	Parameter	UC-IBC	DC-IBC	IC-IBC	Unit
ρ_{cu}	Wire effective resistivity	1.724*10 ⁻⁸			$\Omega \cdot m$
B_{sat}	Saturation flux density	0.2			T
K'_u	Assumed winding factor	0.4	0.4	0.4	--
L	Inductor value	56*10 ⁻⁶	--	--	H
L_M	Magnetizing inductance	--	28*10 ⁻⁶	56*10 ⁻⁶	H
$i_{M,sat}$	Maximum magnetizing current	--	110	5	A
$I_{L,max}$	Maximum inductor current	55	--	--	A
I_{L1rms} I_{L2rms}	Winding current RMS value	--	50	50	A
$P'_{cu,tot}$	Assumed copper losses	--	50	50	W
R'_L	Assumed inductor resistance	10*10 ⁻³	--	--	Ω
K_{gmin}	Calculated K_{gmin}	10.2216	41.0227	0.3390	cm ⁵

In Table.2.2, B_{sat} is set as 0.2T to satisfy the worst case. K'_u , $P'_{cu,tot}$, and R'_L are assumed value and after the inductor's design, the actual values will be obtained. For DC-IBC, the DC component of magnetizing current equals the sum of two windings' DC currents. The magnetizing current ripple sets as 20% DC magnetizing current. For IC-IBC, as the DC fluxes are canceled, the DC magnetizing current can be neglected. Here, the AC magnetizing current is set as AC component of winding current. The magnetizing inductance can be obtained as (2.4.3).

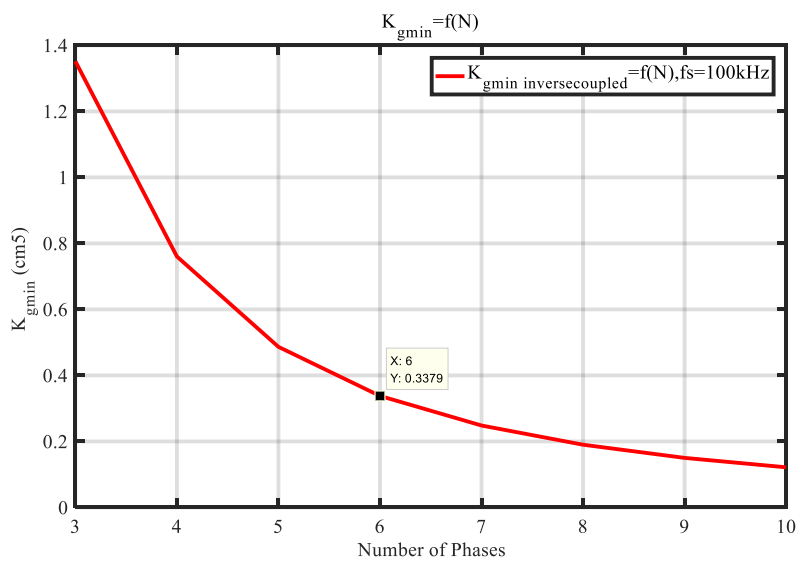
$$L_M = \frac{V_{in} \times D}{i_{M,sat} \times f_s} \quad (2.4.3)$$

Thus, the K_{gmin} of these three converters under the nominal operating conditions can be calculated and are given in Table.2.2. Although only 6-phase IBC is studied in this thesis, the relationship between number of interleaved phases (N) and magnetic core geometric constant is also required to be analyzed. Fig.2.6 illustrates the influence caused by N to K_{gmin} for UC-IBC, DC-IBC, and IC-IBC.

According to Fig.2.6, obviously the minimum core geometrical constant of single inductor decreases while the number of interleaved phase increases. DC-IBC obtains the highest K_{gmin} while IC-IBC possesses the lowest in the whole range. The K_{gmin} of UC-IBC situates between these two limitations. The zoom of K_{gmin} for IC-IBC has been presented in Fig.2.6 (b).



(a). Relationship between K_{gmin} and N



(b) Zoom of K_{gmin} for IC-IBC

Fig.2.6 Comparison of minimum core geometric constant among each topologies

The flow diagram for magnetic core design procedure of UC-IBC, DC-IBC, and IC-IBC is presented as Fig.2.7. Then, the magnetic core of each topology is designed according to these steps.

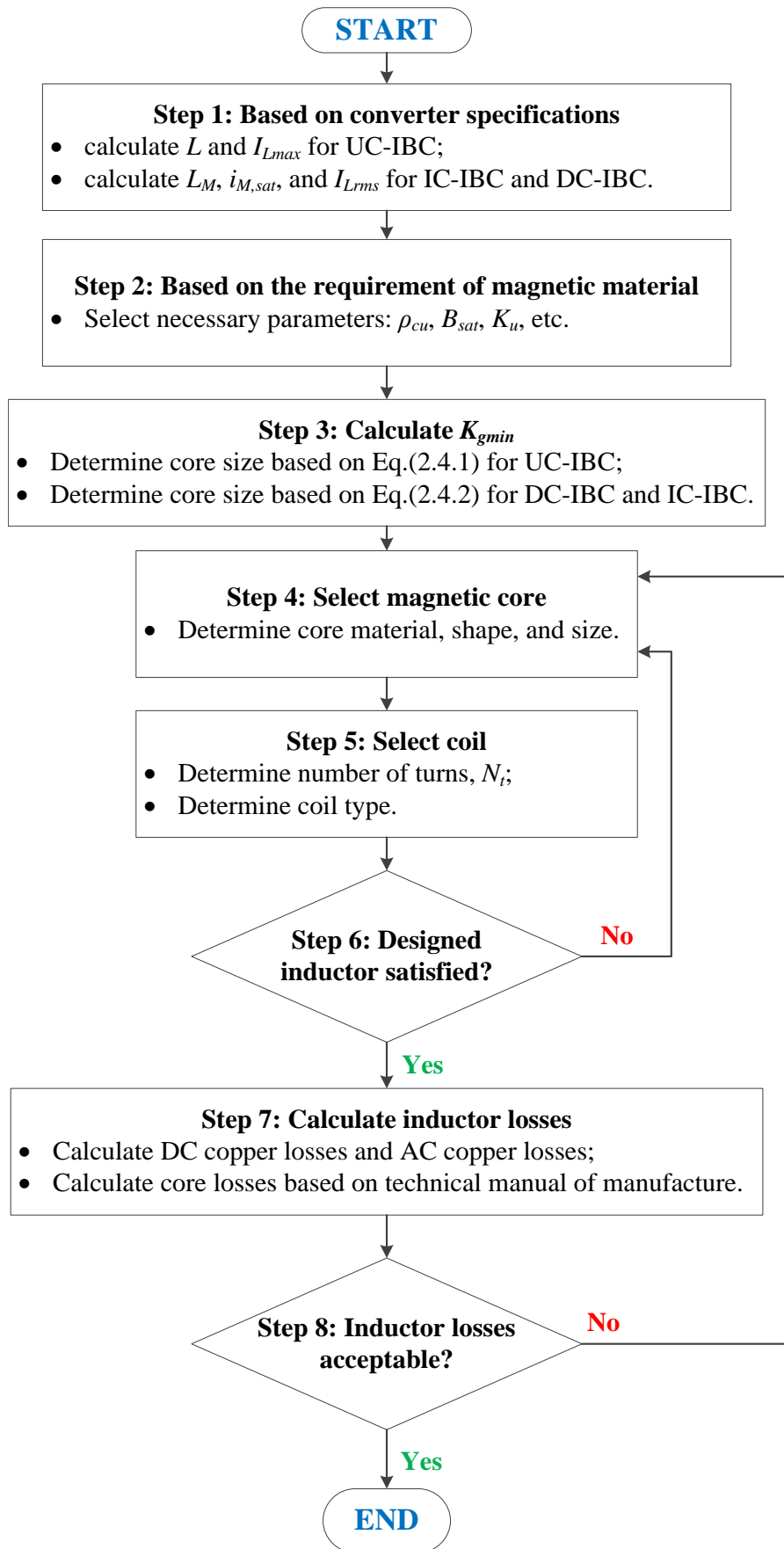


Fig.2.7 Flow diagram of magnetic core's design procedure

Some important parameters of the designed inductors are summarized in Table.2.3. Firstly, the core quantity, volume, and weight are compared. Here the inductor's parameters of DC-IBC are treated as the reference. For DC-IBC, four toroid cores are required to increase the effective area. The cost is that the volume and weight are increased compared with other twos. For UC-IBC and IC-IBC, the magnetic core's volume is reduced by 75% and 94.17% while the magnetic core's weight is reduced by 75% and 94.30% compared with DC-IBC respectively. Hence, from the side of inductor's volume and weight, IC-IBC can be much more attractive than DC-IBC and UC-IBC for FCEV application. The power losses analysis of the proposed inductors will be addressed in the following section.

Table.2.3 The comparison of designed inductors for three converters

Parameter	DC-IBC	IC-IBC	UC-IBC	Unit
Core type	Toroid	Toroid	Toroid	--
Manufacturer	Magnetics	Magnetics	Magnetics	--
Ordering code	55735	55439	55737	--
Core material	MPP	MPP	MPP	--
Permeability	26u	60u	60u	--
Quantity of core	4	1	1	--
Single core volume	91400	21300	91400	mm ³
Core volume reduction compared to DC-IBC	--	94.17%	75%	--
Core weight	790	180	790	g
Core weight reduction compared to DC-IBC	--	94.30%	75%	--
Coil	AWG 7	AWG 7	AWG 7	--
Number of turns	10	8	31	--
Actual winding factor	0.11	0.42	0.22	--
Effective area	497	199	497	mm ²
Winding area	1550	427	1550	mm ²
Mean length per turn	110	77.6	117	mm
Effective length	184	107	184	mm
Actual K_{gmin}	124.5302	0.2835	16.0150	cm ⁵
K_g of selected core	139.2233	2.1791	32.7234	cm ⁵

2.5. Converter's efficiency analysis

The efficiency of converter is closely related to power losses of each electrical element. Theoretical analysis is essential during the design process of converter. Normally, power losses of converter are caused by semiconductors and passive components. The power losses of 6-phase UC-IBC, DC-IBC, and IC-IBC are evaluated from efficiency point of view.

2.5.1. The power losses caused by MOSFET

The power losses caused by MOSFET consist of two parts:

- 1) Conduction losses (P_{on_mos});
- 2) Switching losses (P_{switch}).

When the control order is sent to the gate driver of the MOSFET, the power switch will operate under on-off states. During the on-state, the current flows through drain-source of MOSFET. According to the inherent characteristic of the MOSFET, the drain-source on-state resistance (R_{on_mos}) cannot be neglected and this is the source of conduction losses P_{on_mos} which can be expressed as (2.5.1):

$$\begin{cases} P_{on_mos} = I_{mos_rms}^2 \times R_{on_mos} \\ I_{mos_rms} = \sqrt{D \times I_{L_dc}^2 + D \times \frac{\Delta i_L^2}{12}} \end{cases} \quad (2.5.1)$$

According to the specification, the inductor current ripple equals 20% of the DC component. Thus, the power losses caused by current ripple cannot be neglected. I_{mos_rms} stands for the Root-Mean-Square (RMS) value of current that flows through MOSFET, I_{L_dc} stands for the DC component of inductor current.

The switching losses of MOSFET are introduced in two periods, turn-on and turn-off transitions respectively. In actual application, even the switching period of MOSFET is extremely small regarding the high switching frequency; however, the voltage across drain-source and the current flowing through drain-source are not equal to zero. Hence, switching losses occur during these two switching periods. The evaluation processes are as (2.5.2):

$$\begin{cases} P_{turnon_mos} = f_s \times \frac{E_{test_on} \times V_{switch}}{V_{sw_test_on} \times I_{sw_test_on}} \times I_{switch} \\ P_{turnoff_mos} = f_s \times \frac{E_{test_off} \times V_{switch}}{V_{sw_test_off} \times I_{sw_test_off}} \times I_{switch} \end{cases} \quad (2.5.2)$$

E_{test_on} , E_{test_off} , $V_{sw_test_on}$, $V_{sw_test_off}$, $I_{sw_test_on}$ and $I_{sw_test_off}$ respectively stand for turn-on and turn-off switching energies and the test conditions. These parameters are closely depending on the datasheet of power MOSFET. f_s stands for the switching frequency. The presented two equations can be utilized to estimate switching losses. The calculation process has been simplified and treated the relationship as linear among switching energy, test voltage and test current.

Power losses which are introduced by MOSFET gate driver (P_{gate_driver}) should be considered during the evaluation of total power losses of power converters. The total gate charge, the switching frequency and the voltage across gate-source influence a lot the gate driver losses and can be expressed by (2.5.3). Q_{gate_mos} and V_{gs} stand for the total gate charge and the gain-source drive voltage of MOSFET, respectively.

$$P_{gate_driver} = Q_{gate_mos} \times V_{gs} \times f_s \quad (2.5.3)$$

2.5.2. The power losses caused by Schottky diode

Diode has conduction losses which are proportional to the forward voltage (V_F) multiply by the RMS current through the diode (I_{dio_rms}). The conduction losses contain also the losses due to the resistance in the turn-on state of the diode (R_{on_diode}).

$$\begin{cases} P_{on_diode} = I_{L_dc} \times (1-D) \times V_F + (I_{dio_rms})^2 \times R_{on_diode} \\ I_{dio_rms} = \sqrt{(1-D) \times I_{L_dc}^2 + (1-D) \times \frac{\Lambda i_L^2}{12}} \end{cases} \quad (2.5.4)$$

Another source of power losses is due to the diode reverse recovery time. When the diode is reverse biased in period the series inductance within the circuit continues to force current through the diode. The forward voltage V_F will remain approximately constant as the current reaches zero. In period the stored charges within the diode PN junction are depleted, resulting in a large negative current which peaks at a value of reverse current (I_{rev}). The diode acts as an energy source and delivers energy to the circuit. When the stored charge is depleted across the junction, the voltage drop across the diode snaps in the direction of the reverse bias and after a brief overshoot will settle at the steady-state reverse biased value. The diode reverse recovery losses can be calculated as (2.5.5). In this equation, Q_{rr} stands for the total capacitive charge of Schottky diode.

$$P_{rev_diode} = 0.5 \times V_{rev} \times Q_{rr} \times (I_{dio_dc} / I_{rev}) \times f_s \quad (2.5.5)$$

To be emphasized, (2.5.5) can only be used to estimate the reverse recovery losses of Silicon (Si) based Schottky diode. The Wide-Band Gap (WBG) materials based Schottky diode, such as Silicon Carbide (SiC) and Gallium Nitride (GaN) based ones, can obtain almost zero reverse recovery losses [2-12]. Thus, only the conduction losses exist in this new generation Schottky diode, and the power losses of diode can be reduced significantly.

2.5.3. The power losses caused by inductor

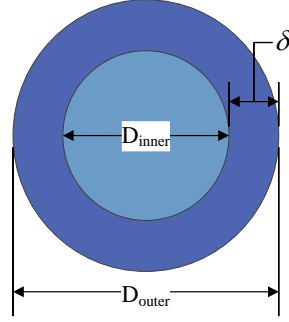
The power losses caused by inductor include copper losses (P_{copper}) which are introduced by the skin effect and proximity effect, and core losses (P_{core}) which are introduced by the hysteresis and eddy current effects. These losses depend on the core material and on the wire gauge used. The calculation processes of P_{copper} and P_{core} in this study are presented as following subsections.

2.5.3.1. Copper losses analysis

Estimation of the copper losses is necessary for the power converter efficiency analysis. These losses are generated by the DC resistance of the total winding and the AC resistance affected by the skin-effect and the proximity effect. The copper losses are derived as (2.5.6). I_{L_dc} stands for the average value of inductor current; Δi_{L_rms} stands for the RMS value of inductor current ripple; R_{L_dc} and R_{L_ac} stand for the DC resistance and AC resistance of winding separately.

$$P_{copper} = I_{L_dc}^2 \times R_{L_dc} + \Delta i_{L_rms}^2 \times R_{L_ac} \quad (2.5.6)$$

In order to explain the distribution and estimation of R_{L_dc} and R_{L_ac} inside winding, the cross section of wire is illustrated in Fig.2.8. According to the design process of inductor explained previously, the round wire which respects American Wire Gauge (AWG) is selected. In this figure, the DC component of inductor current flows through the inner part colored by light blue; and the AC component of inductor current flows through the outer part which is an annulus and colored by dark blue. D_{inner} stands for the diameter of the part which the DC inductor current flows through; D_{outer} stands for the outer diameter of the wire.


 Fig.2.8 $R_{L_{dc}}$ and $R_{L_{ac}}$ distribution inside winding

Once the wire model is confirmed, the area of annulus is determined by the skin depth which can be calculated as (2.5.7). δ is the skin depth; ρ_{cu} is the resistivity of the winding material; μ_0 is the permeability of free space; f_s is the switching frequency.

$$\delta = \sqrt{\frac{\rho_{cu}}{\pi \cdot \mu_0 \cdot f_s}} \quad (2.5.7)$$

The wire area (A_w) can be calculated by (2.5.8).

$$A_w = \pi \cdot \left(\frac{D_{outer}}{2} \right)^2 \quad (2.5.8)$$

Thus, the inner part area (A_{dc}) and the annulus area (A_{ac}) can be obtained by (2.5.9).

$$\begin{cases} A_{dc} = \pi \cdot \left(\frac{D_{inner}}{2} \right)^2 = \pi \cdot \left(\frac{D_{outer} - 2 \times \delta}{2} \right)^2 \\ A_{ac} = A_w - A_{dc} \end{cases} \quad (2.5.9)$$

Finally, the DC resistance ($R_{L_{dc}}$) and AC resistance ($R_{L_{ac}}$) can be obtained as (2.5.10). l stands for the length of each winding.

$$\begin{cases} R_{L_{dc}} = \rho_{cu} \cdot \frac{l}{A_{dc}} \\ R_{L_{ac}} = \rho_{cu} \cdot \frac{l}{A_{ac}} \end{cases} \quad (2.5.10)$$

2.5.3.2. Core losses analysis

The core losses are mainly dependent on the eddy currents and the hysteresis process, and they can be calculated by the well-known Steinmetz equation. However, this estimation method is limited because it is valid only under a sinusoidal excitation condition.

In this study, the selected magnetic cores are fabricated by the manufacturer Magnetics [2-9]. Depending on its manual, the estimation method of core losses' density has been given. The core losses density is calculated depending on the DC magnetization curve fitting formula ((2.5.11)) and the core losses density curve fitting formula ((2.5.12)). a_1, b_1, c_1, d_1, e_1 , and x_1 are the given parameters depending on the magnetic material. B_{pk} is half of the AC flux swing as (2.5.13), f_s is the switching frequency, and a, b, c are the given parameters depending on the magnetic material.

$$B = \left(\frac{a_1 + b_1 \cdot H + c_1 \cdot H^2}{1 + d_1 \cdot H + e_1 \cdot H^2} \right)^{x_1} \quad (2.5.11)$$

$$P_{core_density} = a \cdot B_{pk}^b \cdot f_s^c \quad (2.5.12)$$

$$B_{pk} = \frac{\Delta B}{2} = \frac{B_{AC\ max} - B_{AC\ min}}{2} \quad (2.5.13)$$

The magnetic field strength (H) can be obtained as (2.5.14). N_t is the number of turns of each winding, and l_e is the length of effective magnetic circuit.

$$\begin{cases} H_{AC\ max} = \frac{N_t}{l_e} \cdot \left(I_{L_dc} + \frac{\Delta i_L}{2} \right) \\ H_{AC\ min} = \frac{N_t}{l_e} \cdot \left(I_{L_dc} - \frac{\Delta i_L}{2} \right) \end{cases} \quad (2.5.14)$$

2.5.4. Total power losses and efficiency analysis of each converter

According to the analysis from 2.5.1 to 2.5.3, total power losses of N -phase IBC (P_{losses}) are presented as (2.5.15) and (2.5.16). The current of each phase decreases when the quantity of phases increases. Therefore, the total power losses of this kind of converter are decreased by increasing the quantity of phase.

$$P_{losses} = N \times (P_{mos} + P_{diode} + P_{inductor}) \quad (2.5.15)$$

$$\begin{cases} P_{mos} = P_{on_mos} + P_{turnon_mos} + P_{turnoff_mos} + P_{gate_driver} \\ P_{diode} = P_{on_diode} + P_{rev_diode} \\ P_{inductor} = P_{copper} + P_{core} \end{cases} \quad (2.5.16)$$

The WBG technology is more and more attractive in the application of high frequency, high power and high temperature areas during recent years. Compared with the classical Si-based semiconductors, ones based on SiC material have lower

on-state resistance, lower switching losses, better thermal capacities, and higher reverse voltage capabilities [2-10].

In consideration of SiC Schottky barrier diodes (SiC-SBDs), SiC-SBDs allow system designers to improve efficiency and increase switching frequency to lower the cost and size of passives and heat sinks in high voltage (600V+) applications that far exceed the upper limit of Si-SBDs.

While Si-SBDs have the advantage of low forward and negligible switching losses, the narrow band-gap of silicon limits their use to a maximum voltage of ~200V. For breakdown voltages above 200V, silicon fast, super-fast and ultra-fast recovery diodes (FRDs) are used. However, compared to silicon FRDs, SiC-SBDs feature significantly lower reverse recovery current and recovery time, which dramatically reduces recovery loss and noise emission. And unlike Si-FRDs these characteristics do not change significantly over current and operating temperature ranges.

Si-FRDs also have high transient current at the moment the junction voltage switches from the forward to the reverse direction, resulting in significant switching loss. This is due to minority carriers stored in the drift layer during conduction phase when forward voltage is applied. The higher the forward current (or temperature), the longer the recovery time and the larger the recovery current.

In contrast, since SiC-SBDs are majority carrier (unipolar) devices that use no minority carriers for electrical conduction, they do not store minority carriers. The reverse recovery current in SiC-SBDs is present only to discharge junction capacitance. Therefore, the low reverse recovery current in SiC-SBDs leads to substantially lower switching losses compared to Si-FRDs.

Towards SiC MOSFETs, IGBTs (Insulated Gate Bipolar Transistors) are the most common silicon power transistors for high-voltage (>600V), high-current applications. However, the IGBT's advantage of low resistance at high breakdown voltages is achieved at the expense of switching performance.

IGBTs provide lower on-resistance than MOSFETs by injecting minority carriers into the drift region, a phenomenon called conductivity modulation. However, when the IGBT is turned off, it takes time for these minority carriers to recombine and "dissipate", thus generating a tail current and increasing switching time and power compared with MOSFETs (which in principle do not generate tail current).

In contrast, SiC devices do not need conductivity modulation to achieve low on-resistance since they have much lower drift-layer resistance than Si devices. As a result, SiC-MOSFETs feature much lower switching loss than IGBTs.

As analyzed in previous sections, IC-IBC, DC-IBC and UC-IBC have been comparative studied from the view of magnetic cores' constructions, volumes, and weights. Meanwhile, the influences to the input current ripple caused by different inductor structures have also been compared. In order to find out the advantages and disadvantages of each converter, it is necessary to make a global efficiency and power losses analysis. SiC-based MOSFET and Schottky diode are used in this study depending on the specifications of converters. High switching frequency and high current are requested. So the selection of SiC-based semiconductors can help these converters to gain good thermal performance and reduce power losses while satisfy the requirements of specifications. Here, these three converters are presented more precisely by the following Table.2.4.

Table.2.4 Explanation of converters

Converter	Basic topology	SiC MOSFET	SiC Schottky diode	Coupled inductor
IC-IBC	6-phase IBC	✓	✓	✓ Inverse coupled
DC-IBC	6-phase IBC	✓	✓	✓ Direct coupled
UC-IBC	6-phase IBC	✓	✓	

According to the specifications, the maximum inductor current (I_{Lmax}) equals 55A and the maximum DC bus voltage (V_{out_max}) equals 367.5V. Hence, the minimum continuous drain current (I_D) of the selected SiC MOSFET and the minimum continuous forward current (I_F) of the selected SiC Schottky diode must be bigger than I_{Lmax} ; the drain-source voltage (V_{DS}) of the selected SiC MOSFET and the repetitive peak reverse voltage (V_{RRM}) of the selected SiC Schottky diode must be bigger than V_{out_max} .

Discrete SiC power MOSFETs C2M0025120D from CREE[®] (Wolfsped group) has been selected in order to gain volume and weight for the converter [2-11]. The important parameters of this SiC MOSFET are summarized in Table.2.5. Obviously,

V_{DSmax} is 1200V which can satisfy the requirement of $V_{out_max} \cdot I_D$ under the worst case ($T_c=100\text{ }^\circ\text{C}$) is 60A which can also satisfy the requirement of I_{Lmax} .

The SiC Schottky diodes C4D40120D produced by CREE[®] (Wolfspeed group) have been selected [2-12]. The important parameters of this SiC Schottky diode are summarized in Table.2.6. Obviously, V_{RRM} is 1200V which can satisfy the requirement of $V_{out_max} \cdot I_F$ under the worst case ($T_c=150\text{ }^\circ\text{C}$) is 40A per device and 54A when T_c is $135\text{ }^\circ\text{C}$. To be emphasized, the ambient temperature of actual FCEV is around $70\text{ }^\circ\text{C}$. In other words, the limitation of I_F will not be reached in actual application. Hence, the selected SiC Schottky diode is possible to be used in FCEV.

Table.2.5 The parameters of SiC MOSFET used in IC-IBC, DC-IBC and UC-IBC

Symbol	Parameter	Value	Unit	Test Conditions	
V_{DSmax}	Drain-Source Voltage	1200	V	$V_{GS}=0V, I_D=100\mu A$	
I_D	Continuous Drain Current	1) 90 2) 60	A	1) $V_{GS}=15V, T_c=25\text{ }^\circ\text{C}$ 2) $V_{GS}=15V, T_c=100\text{ }^\circ\text{C}$	
T_J, T_{stg}	Operating Junction and Storage Temperature	-55 to +150	$^\circ\text{C}$		
$R_{DS(on)}$	Drain-Source On-State Resistance	1) 25 2) 43	mOhm	1) $V_{GS}=15V, I_D=15A$ 2) $V_{GS}=15V, I_D=15A, T_J=150\text{ }^\circ\text{C}$	
E_{ON}	Turn-On Switching Energy (Body Diode FWD)	1.6	mJ	$V_{DS}=800V,$ $V_{GS}=-4V/15V,$ $I_D=50A,$ $R_{G(ext)}=2.5\text{ohm},$ $L=142\mu H,$	$T_J=25\text{ }^\circ\text{C}$
		1.49			$T_J=150\text{ }^\circ\text{C}$
E_{OFF}	Turn-Off Switching Energy (Body Diode FWD)	0.75			$T_J=25\text{ }^\circ\text{C}$
		0.9			$T_J=150\text{ }^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.24	$^\circ\text{C/W}$		

Table.2.6 The parameters of SiC Schottky diode used in IC-IBC, DC-IBC and UC-IBC

Symbol	Parameter	Value	Unit	Test Conditions
V_{RRM}	Repetitive Peak Reverse Voltage	1200	V	
I_F	Continuous Forward Current (Per Leg/Device)	1) 56.5/113 2) 27/54 3) 20/40	A	1) $T_c=25\text{ }^\circ\text{C}$ 2) $T_c=135\text{ }^\circ\text{C}$ 3) $T_c=150\text{ }^\circ\text{C}$
T_J	Operating Junction Temperature	-55 to +175	$^\circ\text{C}$	
T_{stg}	Storage Temperature	-55 to +135	$^\circ\text{C}$	
V_F	Forward Voltage	1) 1.5	V	1) $I_F=20A, T_J=25\text{ }^\circ\text{C}$

		2) 2.2		2) $I_F=20A, T_J=175\text{ }^\circ\text{C}$	
I_R	Reverse Current	35	uA	$V_R=1200V$	$T_J=25\text{ }^\circ\text{C}$
		65			$T_J=175\text{ }^\circ\text{C}$
Q_C	Total Capacitive Charge	99	nC	$V_R=800V, I_F=15A$ $di/dt=200A/us$ $T_J=25\text{ }^\circ\text{C}$	
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.29	$^\circ\text{C/W}$		

The total power losses and efficiency of these converters are shown in Table.2.7. As the parameter value of SiC MOSFET and SiC Schottky diode changes a lot with the semiconductor's junction temperature, it is important to know the maximum power losses of each component under the worst case. Here, T_J of 150°C is selected as the worst case for both SiC MOSFET and SiC Schottky diode according to the datasheet.

In actual application, the efficiency will be higher than the calculated minimum efficiency for each converter. The power losses and efficiencies are calculated under nominal power.

Table.2.7 Power losses and efficiency @ $P_{FC}=21\text{kW}$ & $T_J=150^\circ\text{C}$

Junction Temperature	Converter Type	Power	Total Power Losses	Efficiency
$T_J=150^\circ\text{C}$	IC-IBC	21kW PEMFC	1653W	92.12%
	DC-IBC		1844W	91.20%
	UC-IBC		1745W	91.68%

According to Table.2.7, the highest efficiency is obtained by IC-IBC as 92.12% under the worst condition. The total power losses of IC-IBC are 1650W. The minimum efficiency is obtained by DC-IBC as 91.20% and its total losses are 1842W. The power losses and efficiency of UC-IBC is between the result range of IC-IBC and DC-IBC as presented.

In order to understand how the power losses of each component influence converter's efficiency, the power losses distribution of single phase for these three converters is illustrated in Fig.2.9.

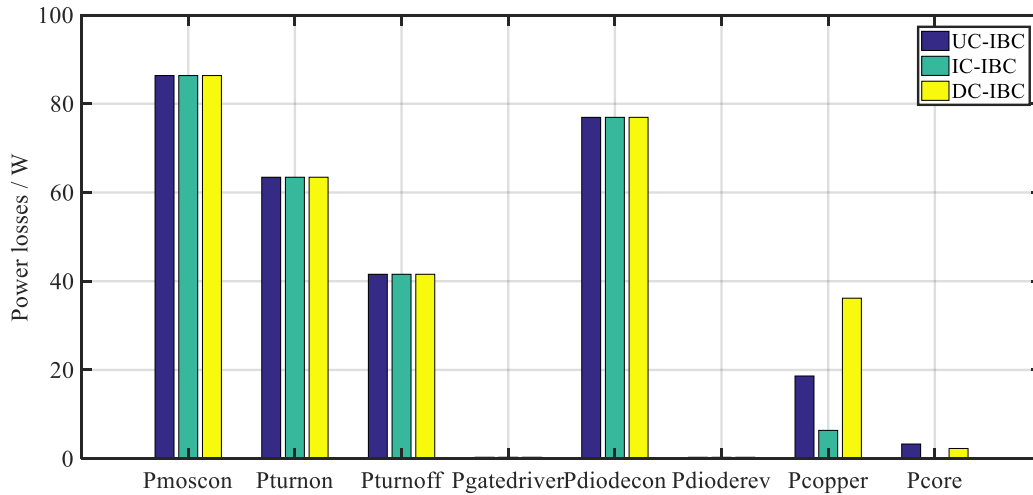


Fig.2.9 Single phase power losses @ $P_{FC}=21\text{kW}$ & $T_j=150^\circ\text{C}$

The useful information from Fig.2.9 is explained as follow:

- 1) The power losses of SiC MOSFET of IC-IBC, DC-IBC and UC-IBC are the same. The same model of SiC MOSFET is chosen for these three converters as they own the same topology. The currents that flow through power switch of each topology are the same. Although the magnetic components are not the same, the power losses of SiC MOSFET will not be influenced. The power losses values of selected SiC MOSFET are given in Table.2.8.
- 2) The power losses of SiC Schottky diode of IC-IBC, DC-IBC and UC-IBC are the same. The reason is the same as explained in 1). The power losses values of selected SiC Schottky diode are given in Table.2.8.
- 3) According to Fig.2.9, the conduction losses of power switch, whether SiC MOSFET or SiC Schottky diode, can influence total power losses of converter significantly. Thus, it is attractive to use multi power switch in parallel to reduce the conduction resistance. Meanwhile, the redundancy of converter can be increased. However, too many power switches lead to big volume and high price, and the requirement of gate driver is also increased. In the following subsection, this issue will be addressed.
- 4) The power losses of inductors are different. IC-IBC obtains the minimum copper losses and core losses. The copper losses of DC-IBC are the highest because multiple cores are request to be constructed in parallel depending on the design process. In this way, the length of winding increases, thus, P_{copper} of DC-IBC increases. However, the magnetic core's material of DC-IBC is different for

UC-IBC. Therefore, P_{core} of DC-IBC is reduced a little compared to UC-IBC. A zoom of inductor losses of these three converters is presented by Fig.2.10.

Table.2.8 Semiconductor’s power losses distribution of Fig.2.9

	Symbol	Parameter	Value
SiC MOSFET	P_{moscon}	Conduction losses	86.36W
	P_{turnon}	Turn-on losses	63.44W
	$P_{turnoff}$	Turn-off losses	41.56W
	$P_{gatedriver}$	Gate drive losses	0.322W
SiC Schottky diode	$P_{diodecon}$	Conduction losses	76.94W
	$P_{diode rev}$	Reverse recovery losses	0.3158W

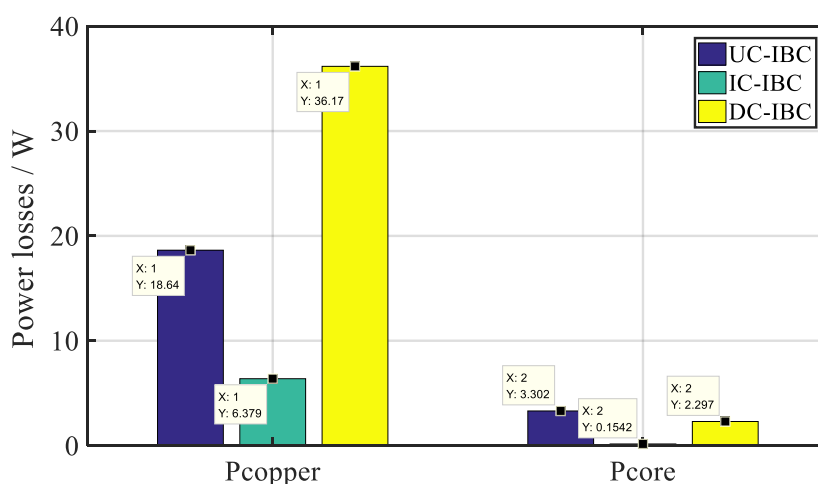


Fig.2.10 Inductor power losses @ $P_{FC}=21kW$ & $T_J=150^\circ C$

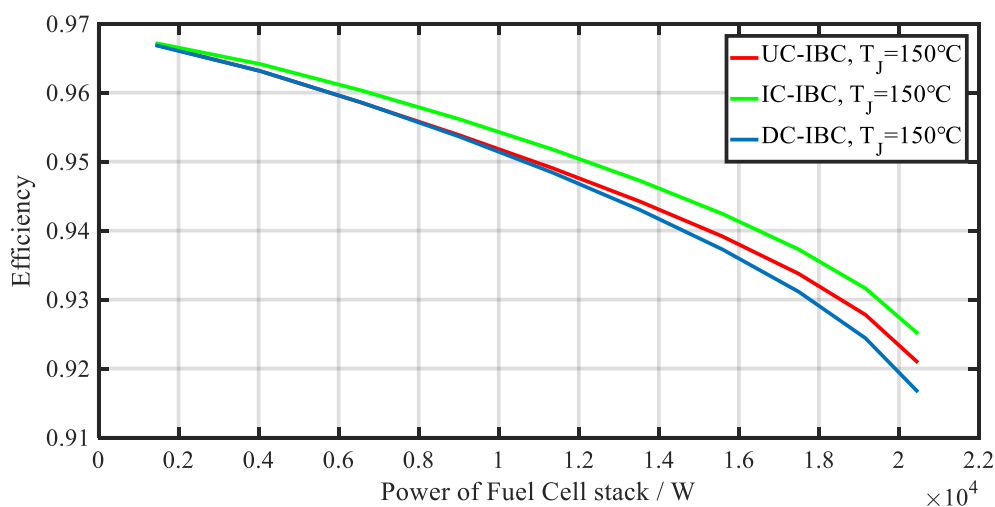


Fig.2.11 Efficiency curves of UC-IBC, IC-IBC and DC-IBC @ $T_J=150^\circ C$

The efficiency of each converter under different power level has been calculated as presented in Fig.2.11. The result is also obtained at the worst case ($T_j=150^\circ\text{C}$). Obviously, the efficiency of IC-IBC is the highest in the whole power range. The efficiency of nominal power is 92.12% as presented in Table.2.7. The maximum efficiency of IC-IBC can be over 96.5%. The efficiency of UC-IBC is higher than DC-IBC. However, when the FC power is lower than 10kW, UC-IBC and DC-IBC almost own the same efficiency.

Therefore, the inverse coupled magnetic core helps a lot decrease the copper losses and core losses of IC-IBC, then, the efficiency increases.

2.5.5. Analysis of IC-IBC based on multi-device in parallel construction

As analyzed previously, the conduction losses of SiC-based MOSFET and Schottky diode have a major effect on the total power losses of converter for FCEV application. This condition is due to the high input current of a fuel cell. Even the input current has already shared by the interleaved branches of IBC, the current which flows through MOSFET and Schottky diode still keeps at a high level. For example, the average inductor current equals 50A depending on the specifications and topologies in this study.

IC-IBC gains more attraction than DC-IBC and UC-IBC from the view of efficiency and power losses. Hence, only IC-IBC is addressed in section to study the influence caused by multi-semiconductor in parallel to the converter's power losses and efficiency.

Here, the quantity of paralleled MOSFET and Schottky diode is symbolized as N_x . With multi-semiconductor in parallel structure, the conduction losses of single SiC MOSFET and SiC Schottky diode are given as (2.5.17). And single phase total conduction losses of SiC MOSFET and SiC Schottky diode are given as (2.5.18). According to these two equations, the total phase conduction losses can be reduced as the existence of N_x 's quadratic component.

$$\begin{cases} P'_{on_mos} = \left(I_{mos_rms} \times \frac{1}{N_x} \right)^2 \times R_{on_mos} \\ P'_{on_diode} = I_{L_dc} \times \frac{1}{N_x} \times (1-D) \times V_F + \left(I_{dio_rms} \times \frac{1}{N_x} \right)^2 \times R_{on_diode} \end{cases} \quad (2.5.17)$$

$$\begin{cases} P_{on_mos}'' = N_x \times \left(I_{mos_rms} \times \frac{1}{N_x} \right)^2 \times R_{on_mos} \\ P_{on_diode}'' = N_x \times \left[I_{L_dc} \times \frac{1}{N_x} \times (1-D) \times V_F + \left(I_{dio_rms} \times \frac{1}{N_x} \right)^2 \times R_{on_diode} \right] \end{cases} \quad (2.5.18)$$

Depending on (2.5.18), total power losses of IC-IBC based on different quantity of SiC MOSFET and SiC Schottky diode in parallel are presented by Fig.2.12. Obviously, total power losses of IC-IBC decrease along with the increase of paralleled component's quantity. Compared with single MOSFET and single diode per phase, the power losses are reduced by 419W when two MOSFETs and two diodes are constructed in parallel per phase. And when three MOSFETs and three diodes are constructed in parallel per phase, total power losses is reduced by 556W compared with single component per phase. When N_x increases from four to ten, the reduction of IC-IBC's total power losses is not significantly.

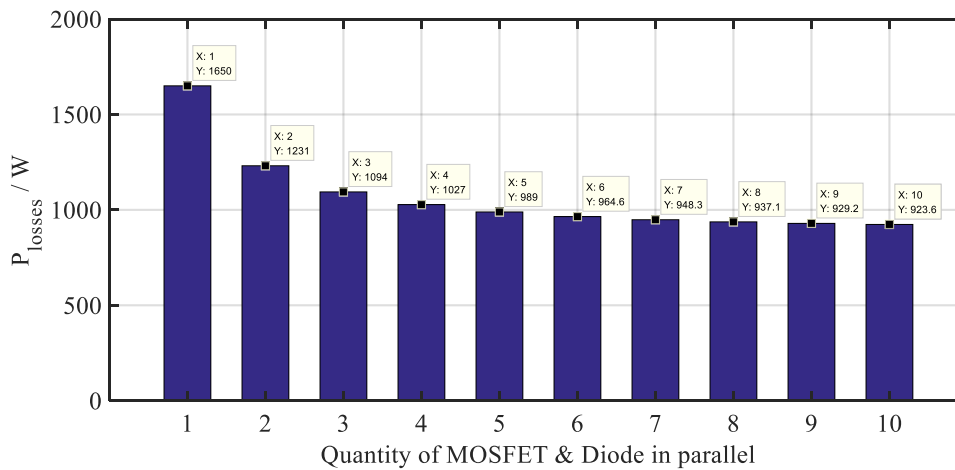


Fig.2.12 Total power losses of IC-IBC based on different quantities of semiconductors in parallel

@ $P_{FC}=21kW$ & $T_j=150^\circ C$

Relying on the calculation of total power losses with different quantity of paralleled component, IC-IBC's efficiency is obtained and illustrated by Fig.2.13. The efficiency of IC-IBC increases along with the increase of paralleled component's quantity. The efficiencies are calculated under the nominal power at the worst case ($T_j=150^\circ C$). The efficiency of IC-IBC can reach 94.8% when three MOSFETs and three diodes are constructed in parallel per phase while only 92% is obtained by IC-IBC with single component per phase.

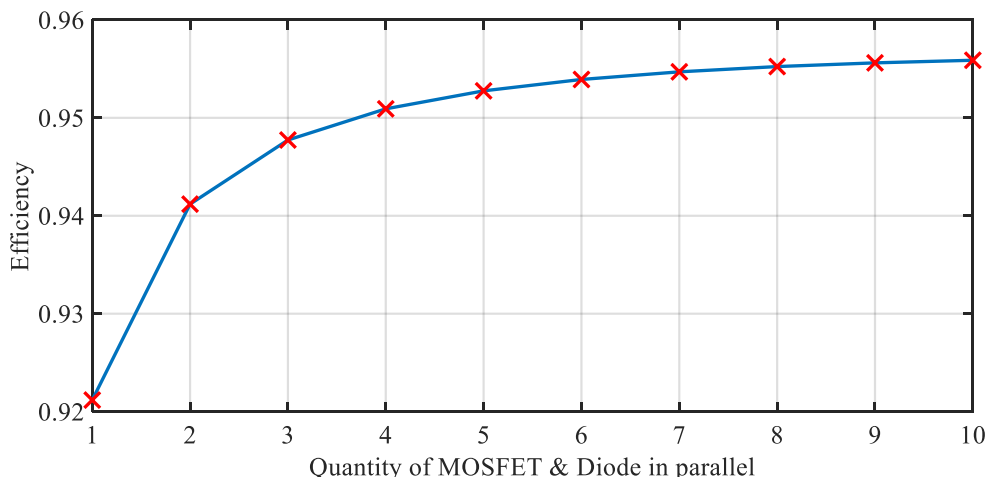


Fig.2.13 Efficiency of IC-IBC based on different quantities of semiconductors in parallel

@ $P_{FC}=21kW$ & $T_j=150^{\circ}C$

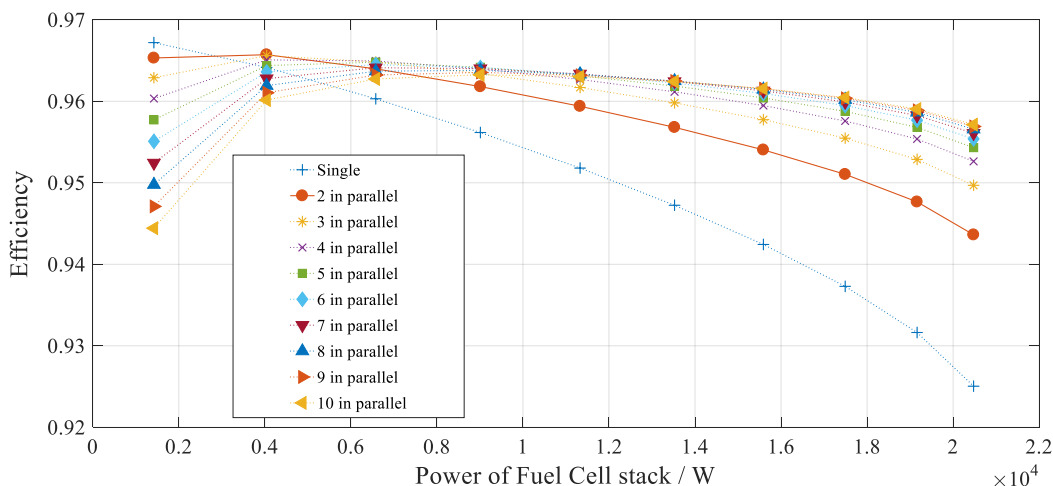


Fig.2.14 Efficiency curves of IC-IBC based on different quantity of semiconductor in parallel

under different FC power levels @ $T_j=150^{\circ}C$

The efficiency curves of IC-IBC based on different quantity of SiC MOSFET and SiC Schottky diode constructed in parallel are illustrated in Fig.2.14. The efficiencies are calculated under different FC power levels at the worst case ($T_j=150^{\circ}C$). The efficiency under nominal power increases along with the increase of paralleled component's quantity. Nevertheless, the maximum efficiency of each condition decreases along with the increase of paralleled component's quantity. Therefore, it is necessary to make comprise between the quantity of paralleled component and the efficiency of IC-IBC. Two or three SiC MOSFETs and SiC Schottky diodes in parallel per phase can be a good choice compared with others.

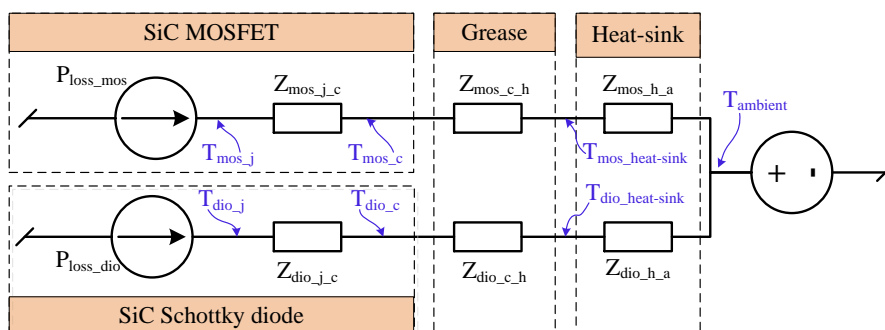
2.6. Thermal analysis of IC-IBC

The reliability of power converter is strongly related to the thermal performance of semiconductor. High power losses can lead to the drastic thermal shock and can even shorten the lifespan of semiconductor. Moreover, the ambient temperature of FCEV' powertrain is always around 70~80°C in practice while the junction temperature limitation of semiconductor (no matter Si or SiC) is 150°C. Hence, in order to keep the junction temperature in an acceptable range, normally we have the following solutions:

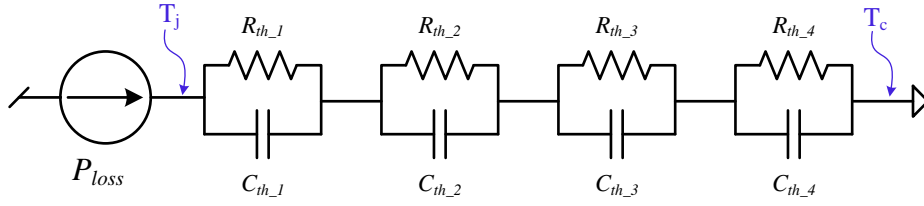
- Use the semiconductor which owns low thermal resistance;
- Use the semiconductor which owns low power losses;
- Use the bulky heat sink which owns low thermal resistance;
- Add the forced (or natural) cooling system (air or liquid) to converter.

Semiconductor power module can obtain low thermal resistance and low conduction resistance. However, compared with the discrete semiconductor, the volume and weight of power module are both its drawbacks. On the other hand, although the bulky heat sink can optimize the thermal performance of semiconductor, it can lead to a converter with large size and big weight. Commonly, there are two kinds of forced cooling system: forced air cooling system and liquid cooling system. The former has a simple construction which only relies on the cooling fans. The latter requires the cooling liquid and the additional pipe network, but these can lead to weight and volume increment and the system will be more complicated.

In order to analyze the semiconductor's thermal performance, semiconductor's thermal model is required. Fig.2.15 presents the used thermal model of semiconductor in this study [2-13].



(a) Thermal model of single SiC MOSFET and SiC Schottky diode from junction to ambient



(b) Equivalent Foster RC thermal network of power device from junction to case

Fig.2.15 The thermal model of power devices in this study

In Fig.2.15 (a), P_{loss_mos} and P_{loss_dio} are the power losses of single SiC MOSFET and SiC Schottky diode of IC-IBC. $Z_{mos_j_c}$ and $Z_{dio_j_c}$ are the thermal resistance of MOSFET and diode from junction to case; $Z_{mos_c_h}$ and $Z_{dio_c_h}$ are the thermal resistance of MOSFET and diode from case to heat-sink (usually neglected due to it is very small value [2-14]); $Z_{mos_h_a}$ and $Z_{dio_h_a}$ are the thermal resistances of heat-sinks. T_{mos_j} and T_{mos_c} are the junction temperature and case temperature of SiC MOSFET separately. T_{dio_j} and T_{dio_c} are the junction temperature and case temperature of SiC Schottky diode separately. $T_{mos_heat-sink}$ and $T_{dio_heat-sink}$ are the temperatures of heat-sinks and $T_{ambient}$ is the ambient temperature. In Fig.2.15 (b), $R_{th_1} \sim R_{th_4}$ stand for the thermal resistances and $C_{th_1} \sim C_{th_4}$ are the thermal capacitances. The parameters are determined by manufacture's datasheet as presented in Table.2.9.

Table.2.9 Thermal parameters of selected SiC MOSFET and SiC Schottky diode [8] [9]

	R_{th_1}	R_{th_2}	R_{th_3}	R_{th_4}	C_{th_1}	C_{th_2}	C_{th_3}	C_{th_4}
C2M0025120D	0.0318	0.0741	0.0499	0.113	0.00689	0.0193	0.0767	0.235
C4D40120D	0.01526	0.061	0.1667	0.0458	0.004736	0.01201	0.02028	1.292
Unit	°C/W				J/°C			

The thermal impedance can be obtained by (2.6.1), and the junction temperature can be obtained by (2.6.2).

$$Z_{j_c}(t(i)) = \sum_{i=1}^4 R_{th_i} \times \left(1 - \exp\left(-\frac{t(i)}{R_{th_i} \times C_{th_i}}\right) \right) \quad (2.6.1)$$

$$\begin{cases} T_{mos_j}(t) - T_{ambient}(t) = P_{loss_mos} \times (Z_{mos_j_c}(t) + Z_{mos_c_h} + Z_{mos_h_a}) \\ T_{dio_j}(t) - T_{dio_c}(t) = P_{loss_dio} \times (Z_{dio_j_c}(t) + Z_{dio_c_h} + Z_{dio_h_a}) \end{cases} \quad (2.6.2)$$

The heat-sink is necessary for a converter in order to improve the rate of thermal dissipation and increase the thermal performance. Thus, it is necessary to estimate the

thermal resistance of heat-sink (R_{h_a}) to select a suitable model. According to Fig.2.15, R_{h_a} is related to T_j , $T_{ambient}$, P_{loss} , and $R_{th_j_c}$ of MOSFET and diode. Benefiting from the use of SiC-based power device, low power losses are obtained and the discrete heat-sink can be selected for each component. Here, the ambient temperature is set as 70°C, and the maximum junction temperatures of SiC MOSFET and SiC Schottky diode are selected as 125°C. The thermal resistance can be obtained as (2.6.3) for the discrete heat-sink. The maximum thermal resistances of heat-sinks for each configuration are presented in Table.2.10. The thermal grease's thermal resistance is selected as 0.1°C/W.

$$\begin{cases} R_{h_a_mos} = \frac{T_{mos_j_max} - T_{ambient}}{P_{loss_mos}} - R_{th_mos_j_c} - R_{th_mos_c_h} \\ R_{h_a_dio} = \frac{T_{dio_j_max} - T_{ambient}}{P_{loss_dio}} - R_{th_dio_j_c} - R_{th_dio_c_h} \end{cases} \quad (2.6.3)$$

Table.2.10 Heat-sink's thermal resistance estimation of converter based on different configurations

@($P_{FC}=21\text{kW}$, $T_a=70^\circ\text{C}$)

	R_{h_a} of Discrete heat-sink		Unit
	SiC MOSFET	SiC Schottky diode	
Config.1	0.0054	1.0013	°C/W
Config.2	0.5730	3.4965	
Config.3	1.1726	6.2670	

In Table.2.10, Config.1 stands for IC-IBC based on single SiC MOSFET and single SiC Schottky diode per phase. Config.2 stands for IC-IBC based on two SiC MOSFETs and two SiC Schottky diodes per phase. Config.3 stands for IC-IBC based on three SiC MOSFETs and three SiC Schottky diodes per phase. According to the estimation results, for Config.2 and Config.3, the power losses of single active component decrease, thus, the thermal dissipation of each component is reduced. Compared with Config.2, R_{h_a} of Config.3 is bigger which means a smaller size of heat-sink can be selected. Discrete heat-sink can be chosen for these two configurations based on the obtained maximum thermal resistance limitation.

The thermal performance of IC-IBC (Config.2 and Config.3) is evaluated as follow. For Config.2, $R_{h_a_mos}$ is 0.5°C/W and $R_{h_a_dio}$ is 3.4°C/W. For Config.3, $R_{h_a_mos}$ is 1.1°C/W and $R_{h_a_dio}$ is 6.2°C/W.

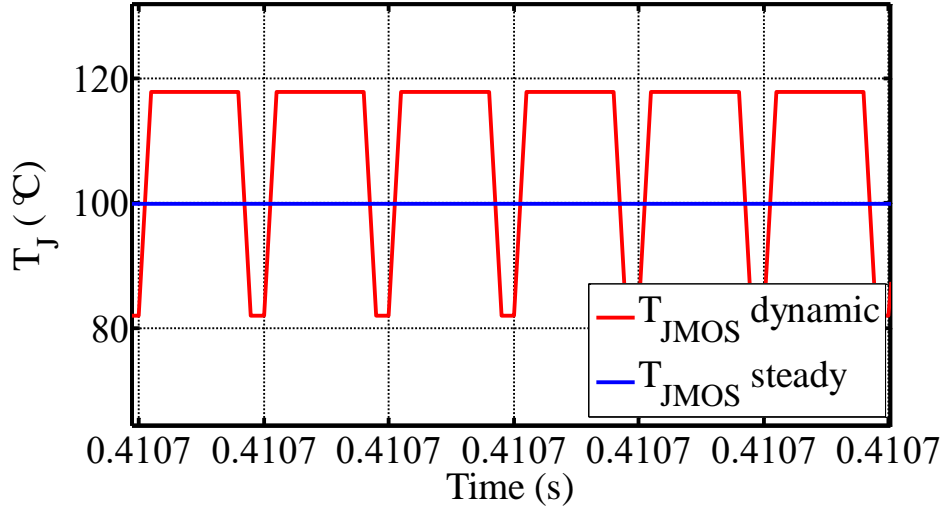


Fig.2.16 SiC MOSFET junction temperature of IC-IBC, Config.2 (@ $P_{FC}=21\text{kW}$ & $T_a=70^\circ\text{C}$)

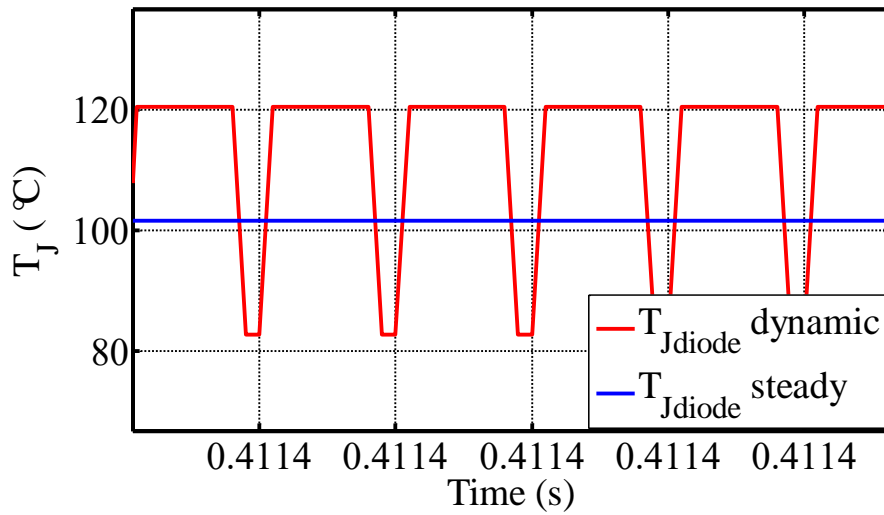


Fig.2.17 SiC Schottky diode junction temperature of IC-IBC, Config.2 (@ $P_{FC}=21\text{kW}$ & $T_a=70^\circ\text{C}$)

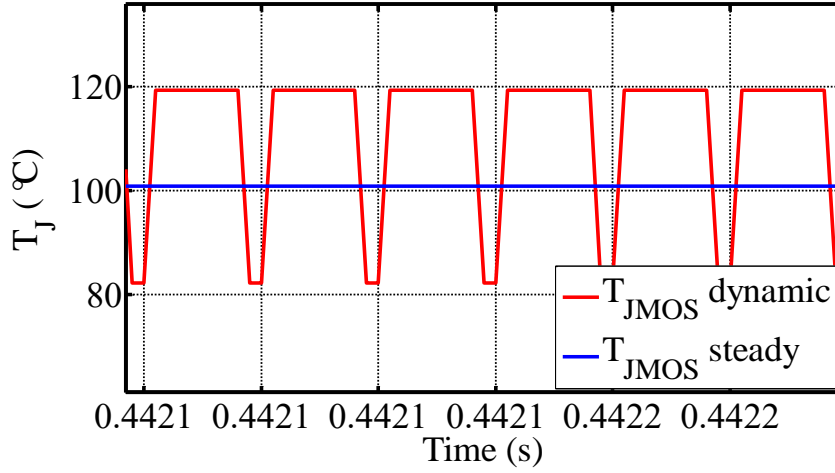


Fig.2.18 SiC MOSFET junction temperature of IC-IBC, Config.3 (@ $P_{FC}=21kW$ & $T_a=70^\circ C$)

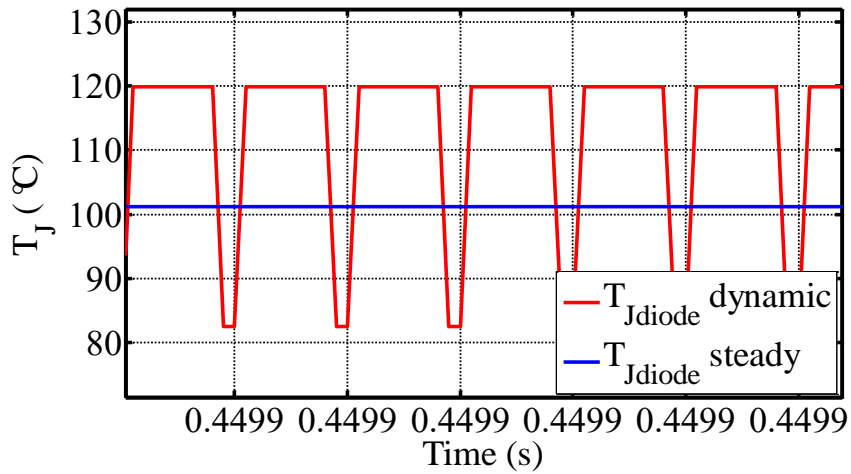


Fig.2.19 SiC Schottky diode junction temperature of IC-IBC, Config.3 (@ $P_{FC}=21kW$ & $T_a=70^\circ C$)

The useful information in Fig.2.16~ Fig.2.19 is summarized in Table.2.11.

Table.2.11 Comparison of thermal behaviors among IC-IBC based on different configurations

@($P_{FC}=21kW$, $T_a=70^\circ C$)

	Parameter	Config.2	Config.3	Unit
SiC MOSFET T_{mos_j}	Steady state temperature	100	101	$^\circ C$
	Maximum of dynamic temperature	119	119	$^\circ C$
	Temperature ripple of dynamic process	35.9	37	$^\circ C$
SiC Schottky Diode T_{dio_j}	Steady state temperature	101	102	$^\circ C$
	Maximum of dynamic temperature	120	119	$^\circ C$
	Temperature ripple of dynamic process	37.9	38	$^\circ C$
Component per phase	MOSFET	2	3	--
	Diode	2	3	--
Total component per converter		24	36	--

At first, the calculation method of junction temperature for the dynamic process is explained. For SiC MOSFET, the power losses consist of three parts (P_{on_mos} , P_{turnon_mos} and P_{gate_driver}) during the conduction state and only $P_{turnoff_mos}$ exists during the off-state. Hence, the difference of junction temperature between theoretical steady state and dynamic process exists. For SiC Schottky diode, P_{on_diode} exists during the conduction state and P_{rev_diode} exists during the off-state. Due to the characteristic of SiC Schottky diode, P_{rev_diode} is extremely small and can be neglected. Hence, the maximum dynamic junction temperature almost equals the theoretical steady state junction temperature.

The thermal performances of these three configurations are evaluated under the nominal FC power and the ambient temperature is set as $70^\circ C$. The junction temperatures of SiC MOSFET and SiC Schottky diode are all lower than the limitation $125^\circ C$ for each configuration of IC-IBC. According to Table.2.11, the junction temperatures of SiC MOSFETs for Config.2 and Config.3 are at the same level ($100^\circ C$). And for SiC Schottky diodes of each configuration, the tendency is the same. To be emphasized, although the semiconductor junction temperature of the Config.2 is the same level as Config.3, its heat-sink's thermal resistance is much bigger than Config.3. Therefore, smaller heat-sink is possible to be selected for Config.2 and the total volume and weight of IC-IBC is also possible to be reduced.

Thus, according to the thermal analysis, IC-IBC based on the configuration of two SiC MOSFETs and two SiC Schottky diodes constructed in parallel per phase can reduce the semiconductor's junction temperature significantly. The specific configuration is attractive for the actual FCEV application.

2.7. Conclusion

In this chapter, a 21kW 6-phase IBC based on SiC semiconductors and inverse coupled inductors (IC-IBC) is proposed. To make a comparative analysis, 6-phase IBC (UC-IBC) and 6-phase IBC based on direct coupled inductors (DC-IBC) are also studied. Firstly, the input current ripple of these three converters is researched. Then, the inductors' design processes are presented. After that, each converter's efficiency is also evaluated. In order to increase the efficiency, the configuration that use multi-semiconductor in parallel is proposed and analyzed for IC-IBC. At last, the thermal analysis is addressed for IC-IBCs which are based on multi-semiconductor in parallel structure. In conclusion, IC-IBC based on two SiC MOSFETs and two SiC Schottky diodes in parallel per phase achieves more advantages such as compact magnetic component, high efficiency, and good thermal performance than UC-IBC and DC-IBC. Although IC-IBC presents higher input current ripple than UC-IBC and DC-IBC, it is also possible to reduce ΔI_{in} below ten percents of average input current with the change of duty cycle and inductor's coupling coefficient. The proposed IC-IBC will be verified based on simulation analysis in chapter 3. Meanwhile, the design process of corresponding controller will also be studied.

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Chapter 3: Control strategy design process

3.1. Introduction

In the previous chapter, the proposed 6-phase IBC based on inverse coupled inductors which are constructed by cyclic cascade structure (IC-IBC) has been studied, analyzed and compared from these aspects: FC current ripple, volume of the magnetic component, power losses of each component and total efficiency of converter at different operating conditions. The conclusion is that the proposed 6-phase IC-IBC tends to be the solution with the best compromise in terms of efficiency and compactness. In this chapter, the small signal AC model of a 6-phase IC-IBC using an averaged PWM switch method will be developed to support the feedback controller design process. Although the inverse coupled inductor is introduced to decrease the core losses and achieve a more compact system, its high non-linear characteristic cannot be neglected. Hence, Sliding Mode Control (SMC) is utilized to satisfy the strict control requirements of the inverse coupled inductors' currents and regulate a stable DC bus voltage both under steady state and transient state [3-1].

In section 3.2, the design process of the control strategy for the 6-phase IBC based on the uncoupled inductors (UC-IBC) and for the 6-phase IC-IBC will be separately addressed. The average models of these two topologies are analyzed and compared. The state-space representations are presented separately for both topologies. In section 3.3, the simulation results of two converters will be demonstrated to verify the correctness and accuracy of proposed control strategy. A conclusion will be given at the last section.

3.2. Design process of the control strategy

The aims of the control are necessary to be established for the purpose of defining the control strategy:

1) Output voltage regulation under load uncertainty. To avoid load damages, it is necessary to regulate the DC bus voltage and maintain it constantly.

2) Equal current sharing between each phase of coupled inductors. The current waveforms should be equal in order to avoid overloading one of the phases, especially

when supplying heavy loads. Also the currents must be interleaved in order to reduce the current ripple which is undesirable in fuel cell stack.

3) Asymptotic stability of the closed loop system. Global asymptotic stability is required to avoid imposing restrictions on the allowed initial conditions.

In this study, the power sources of the FCEV are both PEMFC and battery. The PEMFC plays the constant power supply role while the battery focuses on the dynamic power requirements. The battery is connected to the DC bus through a Buck/Boost converter. The PEMFC and the battery are connected to the DC bus, or the load, through the proposed boost converter and a Buck/Boost converter respectively. In this research, only the design and control of the PEMFC connected Boost converter are studied. Considering FCEV application, firstly the DC bus voltage is essential to be regulated at a constant value to satisfy the requirements; secondly, the input current of the PEMFC is required to be settled at a required value.

3.2.1 Dual-loop PI control for 6-phase UC-IBC

Proportional-Integral (PI) regulator is widely utilized for DC/DC converter and a good control can be obtained. In order to satisfy the control requirements both of DC bus voltage and phase currents, a dual-loop regulator is much more attractive than a single loop regulator. The dual-loop regulator of a BC is composed by outer loop and inner loop regulators which are separately responsible for the regulation of DC bus voltage and phase current. The output of outer loop regulator will act as the reference value of inner loop regulator. Because an integration element exists at the outer loop, the response speed of inner loop regulator is faster than the outer loop. The diagram of dual-loop regulator for a BC is presented in Fig.3.1.

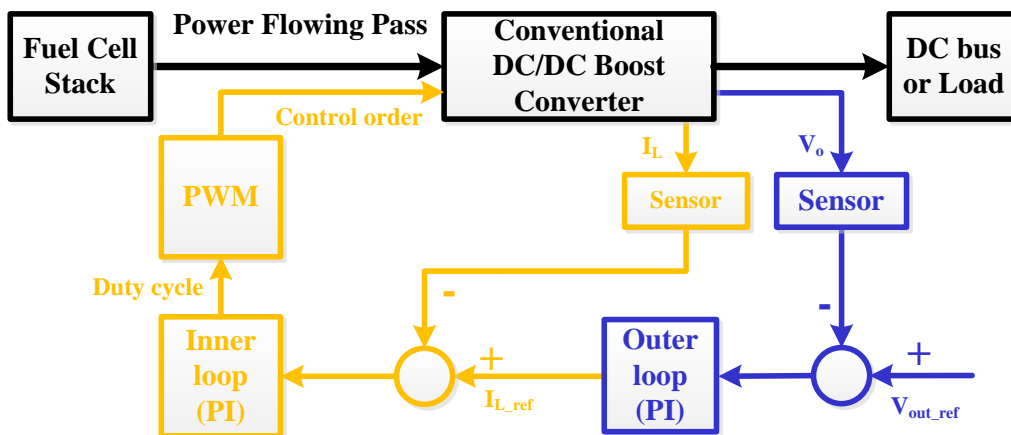


Fig.3.1 Diagram of dual-loop regulator for a BC

However, when the BC is replaced by a 6-phase UC-IBC, the previously presented dual-loop regulator is required to be modified. Due to existing 6-phases and to the fact that the currents flowing through each phase are essential to be regulated, the inner loop regulator has to be applied to each phase to regulate the inductor current. There is a phase shift (T_{delay}) existing between the PWM signal of each phase. Its duration is depending on the quantity of phases and the switching time ($T_{delay}=T_s/N$). By this way, the interleaving control strategy can be realized. Even though the voltage gain ratio will not change compared with the BC, the FC current ripple can be reduced significantly depending on this control strategy. The diagram of dual-loop regulator for the 6-phase UC-IBC is presented in Fig.3.2.

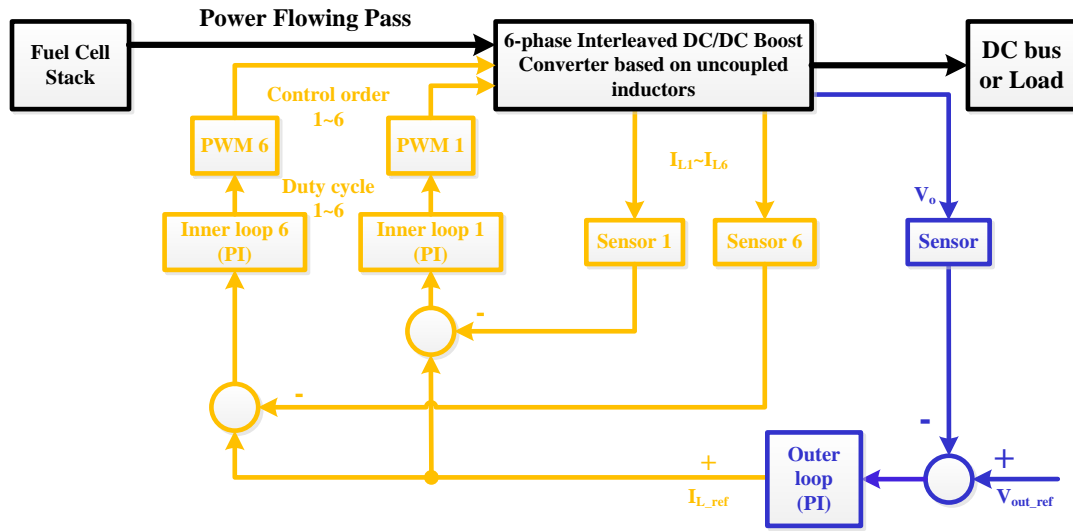


Fig.3.2 Diagram of dual-loop regulator for an 6-phase IBC

In order to design the controls, appropriate dynamic models of the topology are required. In a first step, the equations for the converter are given for the two represented operating sequences. During the analysis, the parasitic resistance of the inductance R_L and the MOSFET conduction resistance R_{on} are both taken into consideration. For the sequence of operation ($0 < t < DT_s$), the equations are given as (3.2.1):

$$\begin{cases} L \frac{di_{L_n}(t)}{dt} = v_{in}(t) - (R_L + R_{on}) \times i_{L_n}(t), n = 1 \sim 6 \\ C \frac{dv_o(t)}{dt} = -i_o(t) \end{cases} \quad (3.2.1)$$

For the sequence of operation ($DT_s < t < T_s$), the equations are given as (3.2.2):

$$\begin{cases} L \frac{di_{L-n}(t)}{dt} = v_{in}(t) - (R_L + R_{on}) \times i_{L-n}(t) - v_o(t), n=1 \sim 6 \\ C \frac{dv_o(t)}{dt} = i_{L1}(t) + i_{L2}(t) + i_{L3}(t) + i_{L4}(t) + i_{L5}(t) + i_{L6}(t) - i_o(t) \end{cases} \quad (3.2.2)$$

Subsequently, the average modeling, well known as averaged circuit models, was applied to equations presented previously. The average model of the 6-phase UC-IBC is given as (3.2.3):

$$\begin{cases} L \frac{d\langle i_{L-n}(t) \rangle_{T_s}}{dt} = \langle v_{in}(t) \rangle_{T_s} - (R_L + R_{on}) \times \langle i_{L-n}(t) \rangle_{T_s} - (1 - d_n(t)) \times \langle v_o(t) \rangle_{T_s}, n=1 \sim 6 \\ C \frac{d\langle v_o(t) \rangle_{T_s}}{dt} = \sum_{n=1}^6 (1 - d_n(t)) \times \langle i_{L-n}(t) \rangle_{T_s} - \langle i_o(t) \rangle_{T_s} \end{cases} \quad (3.2.3)$$

From this modeling, the small signal modeling, commonly called averaged small signal model is deduced. This modeling makes it possible to take into consideration the steady-state and transient operation modes of the system. Therefore, (3.2.4) can be obtained:

$$\langle x(t) \rangle_{T_s} = X + \hat{x}(t) \quad (3.2.4)$$

where $\langle x(t) \rangle_{T_s}$ represents the average value of $x(t)$ in one period T_s , X represents the steady state value of $x(t)$ and finally $\hat{x}(t)$ represents a small disturbance around X . Thus, the following relations can be achieved.

$$\begin{cases} \langle i_{L-n}(t) \rangle_{T_s} = I_{L-n} + \hat{i}_{L-n}(t) \\ \langle v_{in}(t) \rangle_{T_s} = V_{in} + \hat{v}_{in}(t) \\ \langle v_o(t) \rangle_{T_s} = V_o + \hat{v}_o(t) \\ \langle d_n(t) \rangle_{T_s} = D_n + \hat{d}_n(t) \end{cases}, n=1 \sim 6 \quad (3.2.5)$$

The average small signal model of the 6-phase UC-IBC is given as (3.2.6):

$$\begin{cases} L \frac{d\hat{i}_{L-n}(t)}{dt} = \hat{v}_{in}(t) - (R_L + R_{on}) \times \hat{i}_{L-n}(t) - (1 - D_n) \times \hat{v}_o(t) + V_o \times \hat{d}_n, n=1 \sim 6 \\ C \frac{d\hat{v}_o(t)}{dt} = \sum_{n=1}^6 [(1 - D_n) \times \hat{i}_{L-n}(t) - \hat{d}_n \times I_{L-n}] - \hat{i}_o(t) \end{cases} \quad (3.2.6)$$

Assuming that the steady state value ($D_1 \sim D_6$) are identical, the different transfer functions of this UC-IBC with a resistive load R_{out} are given as (3.2.7):

$$\left\{ \begin{array}{l} G_{di_L(s)} = \frac{\hat{i}_L(s)}{\hat{d}(s)} \Big|_{\hat{v}_o(s)=0} = \frac{V_o \cdot C \cdot s + \left[(1-D) \times I_L + \frac{V_o}{R_{out}} \right]}{L \cdot C \cdot s^2 + \left(R_L \cdot C + \frac{L}{R_{out}} \right) \cdot s + \left[\frac{R_L}{R_{out}} + (1-D)^2 \right]} \\ G_{dv_o(s)} = \frac{\hat{v}_o(s)}{\hat{d}(s)} \Big|_{\hat{i}_L(s)=0} = \frac{-I_L \cdot L \cdot s + \left[(1-D) \times V_o - R_L \times I_L \right]}{L \cdot C \cdot s^2 + \left(R_L \cdot C + \frac{L}{R_{out}} \right) \cdot s + \left[\frac{R_L}{R_{out}} + (1-D)^2 \right]} \end{array} \right. \quad (3.2.7)$$

The second order transfer functions can be in following canonical form as given in (3.2.8):

$$\left\{ \begin{array}{l} G_{di_L(s)} = \frac{\hat{i}_L(s)}{\hat{d}(s)} \Big|_{\hat{v}_o(s)=0} = \frac{K_{di_L} \times (T_{di_L} \cdot s + 1)}{\left(\frac{s}{\omega_n} \right)^2 + \frac{2\xi}{\omega_n} \cdot s + 1} \\ G_{dv_o(s)} = \frac{\hat{v}_o(s)}{\hat{d}(s)} \Big|_{\hat{i}_L(s)=0} = \frac{K_{dv_o} \times (T_{dv_o} \cdot s + 1)}{\left(\frac{s}{\omega_n} \right)^2 + \frac{2\xi}{\omega_n} \cdot s + 1} \end{array} \right. \quad (3.2.8)$$

where:

$$\left\{ \begin{array}{l} K_{di_L} = \frac{R_{out} \times I_L \times (1-D) + V_o}{R_L + R_{out} \times (1-D)^2} \\ T_{di_L} = \frac{R_{out} \times V_o \times C}{R_{out} \times I_L \times (1-D) + V_o} \end{array} \right. \quad (3.2.9)$$

$$\left\{ \begin{array}{l} K_{dv_o} = \frac{R_{out} \times V_o \times (1-D) - R_{out} \times R_L \times I_L}{R_L + R_{out} \times (1-D)^2} \\ T_{dv_o} = \frac{I_L \times L}{R_L \times I_L - V_o \times (1-D)} \end{array} \right. \quad (3.2.10)$$

$$\left\{ \begin{array}{l} \omega_n = \frac{1}{\sqrt{LC}} \times \sqrt{\frac{R_L + R_{out} \times (1-D)^2}{R_{out}}} \\ \xi = \omega_n \times \frac{L + R_L \times R_{out} \times C}{2 \times \left[R_L + R_{out} \times (1-D)^2 \right]} \end{array} \right. \quad (3.2.11)$$

The transfer functions are second-order systems with a double pole with a cutoff frequency and with a zero. The cutoff frequency and also the zeros are a function of the duty cycle D . In a closed loop system, the system elements will change as the duty cycle changes, which mean that the transfer function also changes. This therefore makes the controller design for this converter complex form a point of view of stability and bandwidth.

First, the block diagram of the control incorporating the two closed loop control loops for one phase are shown in the following figure Fig.3.3.

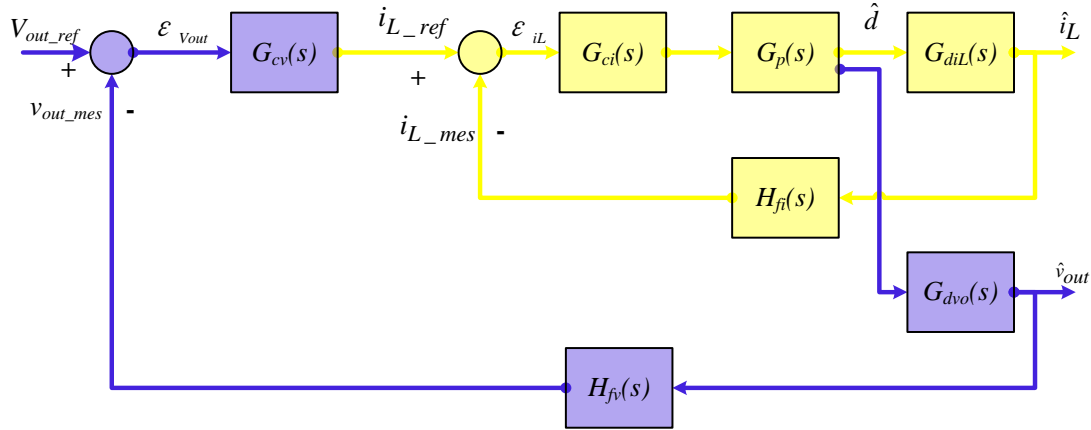


Fig.3.3 Dual loop controller structure

The open loop transfer function of the internal current loop is given as (3.2.12):

$$G_{i_L_open}(s) = G_{ci}(s) \cdot G_p(s) \cdot G_{dil}(s) \cdot H_{fi}(s) \quad (3.2.12)$$

The open loop transfer function of the external voltage loop is given as (3.2.13):

$$G_{v_o_open}(s) = G_{cv}(s) \cdot (1 - G_{i_L_close}(s) \cdot H_{fi}(s)) \cdot G_{ci}(s) \cdot G_{dvo}(s) \cdot H_{fv}(s) \quad (3.2.13)$$

In the presented figure, $G_{cv}(s)$ is the PI controller for obtaining the phase current reference from the difference between the references of the DC bus voltage and the measured DC bus voltage. $G_{ci}(s)$ is the PI controller for obtaining the duty cycle from the difference between the reference and measured currents. $G_p(s)$ is the transfer function of the Pulse Width Modulator (PWM) (i.e. shift of control signals), which can initially be considered equal to one (for the amplitude of the saw tooth signal equal to one). $G_{dil}(s)$ and $G_{div}(s)$ are the transfer functions defined respectively with presented equations. $H_{fi}(s)$ and $H_{fv}(s)$ are the transfer functions of the measurement filters for phase currents and DC bus voltage.

The $G_{cv}(s)$ and $G_{ci}(s)$ correctors were designed using the SISO tool available in Matlab/Simulink software.

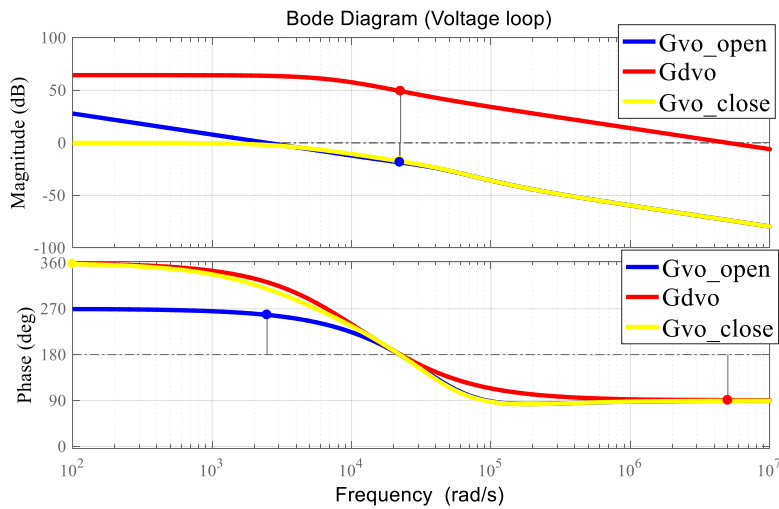
The corrector parameters have been optimized to meet design requirements such as phase margin and magnitude margin, stabilization time, commonly known as settling time. The transfer functions $G_{cv}(s)$ and $G_{ci}(s)$ are as (3.2.14):

$$\begin{cases} G_{ci}(s) = K_{pi} \times \frac{s + K_{ii}/K_{pi}}{s} \\ G_{cv}(s) = K_{pv} \times \frac{s + K_{iv}/K_{pv}}{s} \end{cases} \quad (3.2.14)$$

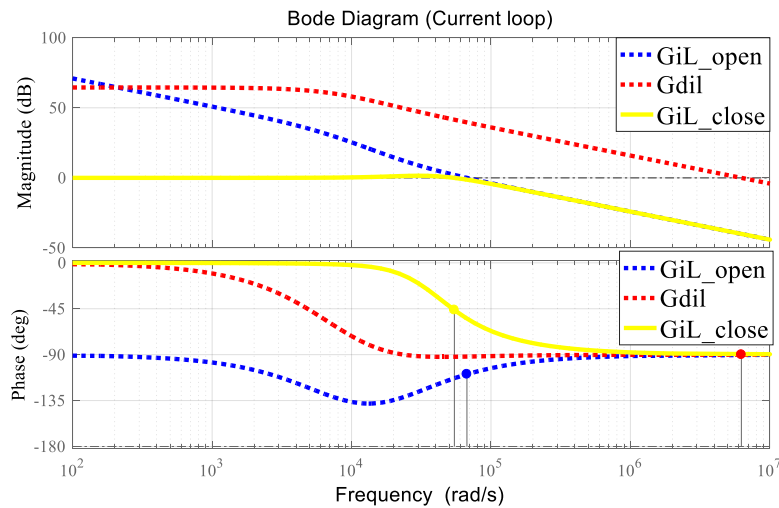
The values of the parameters of the two correctors are given as follow:

$$K_{pi}=0.01, K_{ii}=210; K_{pv}=1/3500, K_{iv}=225$$

The frequency domain analysis results of the proposed dual-loop controller are presented in Fig.3.4. Fig.3.4.(a) illustrates the voltage loop's Bode diagram. In the output voltage control loop, the phase margin is 80° and the magnitude margin is 18.7dB; the crossover frequency is 3kHz. Fig.3.4.(b) illustrates the current loop's Bode diagram. In the current control loop, the phase margin is 68° and the crossover frequency is 7kHz.



(a) Bode plot of voltage loop



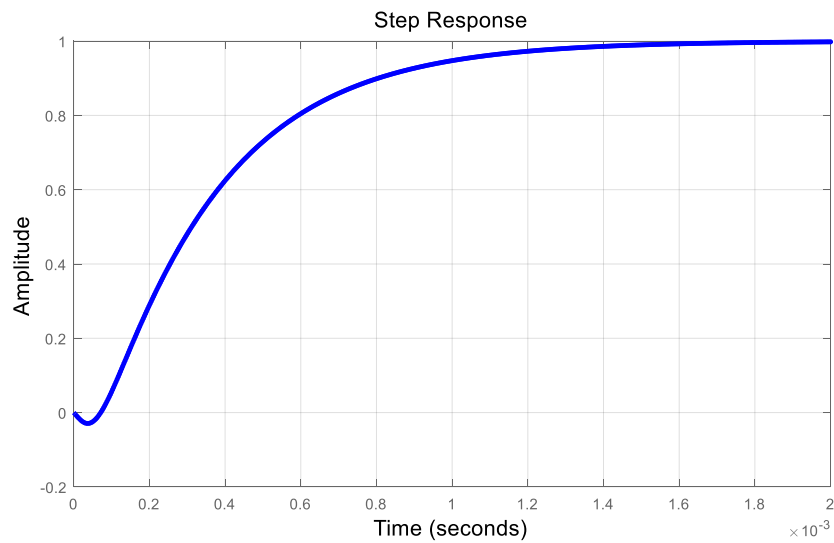
(b) Bode plot of current loop

Fig.3.4 Frequency domain analysis of the proposed dual-loop controller

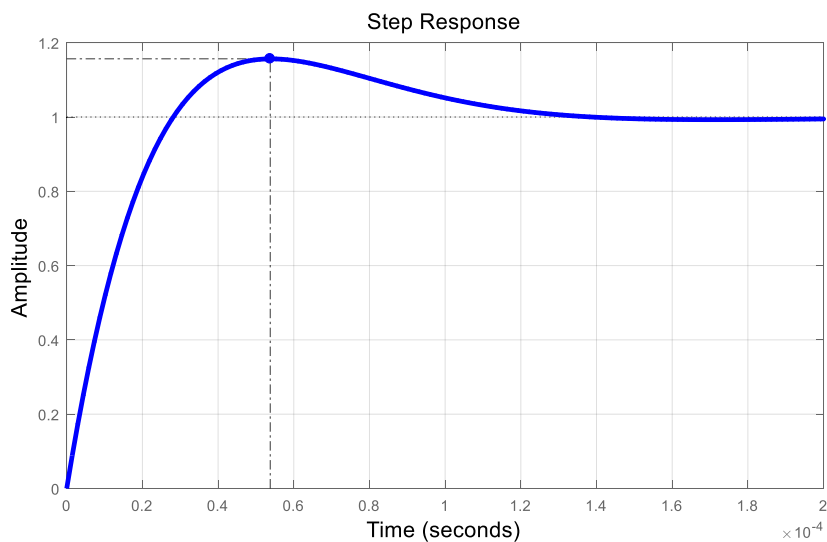
Fig.3.5 presents the time domain analysis of the proposed dual-loop controller.

Fig.3.5.(a) illustrates the step response of DC bus voltage control loop. The settling time equals $2ms$. As Boost converter is not a minimum phase system, it can be found that the response curve decreases at the initial phase and then the curve increases in Fig.3.5.(a). Fig.3.5.(b) illustrates the step response of inner current control loop. The settling time is $0.117ms$. The peak response equals 1.15.

Thus, the proposed dual-loop PI controller for UC-IBC has been verified based on both frequency domain analysis and time domain analysis. UC-IBC combined with the controller can obtain good stability margin and fast response time.



(a) Voltage close loop step response



(b) Current close loop step response

Fig.3.5 Time domain analysis of the proposed dual-loop controller

3.2.2 Sliding-Mode Control for the proposed 6-phase IC-IBC

As demonstrated previously, the Proportional-Integral (PI) controller is well known and widely applied in industrial application fields to optimize the steady-state performance as it is easy to implement PI controller in a real-time processor. The proportional gain contributes to reduce the current error value while the integral gain accelerates the dynamic in order to reduce the time response of the process towards set point and eliminates the residual steady-state error that occurs with a pure proportional controller [3-2]. Nonetheless, an obvious drawback faced with PI controller is that it is linear. Hence, the performance of PI controller in non-linear system is variable. Concerning the design process of PI compensator, it relies on the small signal model of the converter. In order to utilize small signal model, the premise is that the converter operates under static work point. In such a condition, AC small signal analysis can be preceded.

Unfortunately, on account of the strongly non-linear characteristic of coupled inductor, classical PI control strategy does not satisfy the requirements, especially when dynamic changes occur to the electric loads. The DC components of inductor currents are strictly required to be kept to the current reference in our study. DC magnetic bias must be avoided to guarantee the magnetic components operating under non-saturation area. This requirement is needed to be satisfied whether under static work point or dynamic processes. Further, the operating processes of coupled inductor are strongly related to duty cycle and number of interleaved phases. Different number of interleaved phases can lead to different coupling relationship of each phase. Hence, the working process of inductor current also changes as the quantity of branches change. Meanwhile, duty cycle, which is closely related to load level, can influence the regulating process of inductor currents significantly. Supposing significant differences occurring between inductor currents, magnetic saturation could be introduced. In other words, well controlled inductor currents can lead to desirable performance of magnetic components. The most interesting point of inverse coupled inductor is that the DC magnetic fluxes are almost cancelled inside the core, thus compact structure can be obtained in our proposed topology by utilization of inverse coupled inductors compared with uncoupled ones.

Sliding-Mode Control (SMC), which has been proposed by [3-3], is theoretically robust to parameter variations, insensitive to disturbance and can achieve a zero steady-state error [3-9]. More importantly, the design process of SMC depends on the

large signal model of the IBC [3-6]. Its stability is not restricted by variations around operating point, which contributes to an overall improved controller performance [3-7]. The diagram of SMC for proposed 6-phase IC-IBC based on inverse coupled inductors of cyclic cascade structure is presented in Fig.3.6 [3-8]:

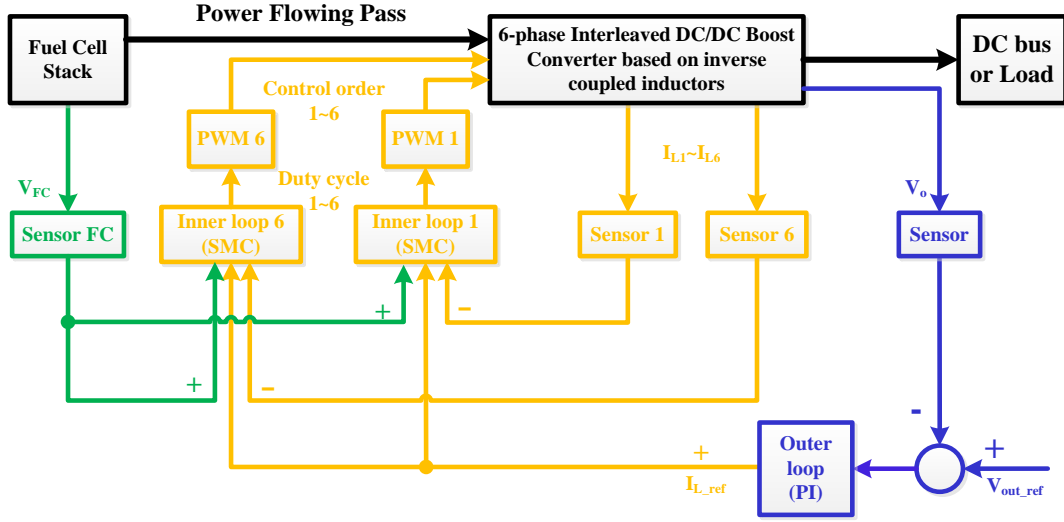


Fig.3.6 Diagram of combination between PI outer voltage loop and Sliding-Mode inner loop for proposed 6-phase IC-IBC

The sliding surface in our study is defined by the following expression.

$$S_{L_n} = (I_{L_n} - I_{L_n_ref}) + K_{L_n} \times \int_0^t (I_{L_n} - I_{L_n_ref}) d\tau \quad (3.2.15)$$

In (3.2.15), n and I_{L_n} respectively stand for the sequence number and average current of each inductor. $I_{L_n_ref}$ is the reference current and K_{L_n} is a coefficient that defines the dynamic of convergence to zero of the static error.

The Lyapunov control function is used to test whether a system is feedback stabilizable [3-4]. A characteristic method is applying a Lyapunov candidate function to test the stability of the dynamic system.

Hence, ε , which equals to I_{L_n} minus $I_{L_n_ref}$, is defined as the error between actual and desired inductor current. Thus, (3.2.15) can be re-written as (3.2.16)

$$S_{L_n} = \varepsilon + K_{L_n} \times \int_0^t \varepsilon d\tau \quad (3.2.16)$$

A Lyapunov candidate is presented in (3.2.17), which is positive definite for all $I_{L_n_ref} \neq 0$, $d(I_{L_n_ref})/dt \neq 0$.

$$V = \frac{1}{2} S_{L_n}^2 \quad (3.2.17)$$

The purpose is to achieve the time derivative to be

$$\dot{V} = -\lambda V, \quad \lambda > 0 \quad (3.2.18)$$

which is globally exponentially stable if V is globally definite.

The convergence dynamic of the sliding surfaces to zero is defined by (3.2.19), which can be proved by (3.2.16), (3.2.17) and (3.2.18). This control law will guarantee global exponential stability.

$$S_{L_n}' = -\lambda_{L_n} \times S_{L_n} \quad (3.2.19)$$

λ_{L_n} , the convergence factors, are positive real numbers. The larger convergence factors are, the faster the system reaches its steady state. However, due to the limitations of the system, it is not possible to increase the value beyond a certain value.

Because the inductors are inverse coupled and based on cascade cyclic structure, the influences of mutual inductance cannot be neglected. Here Phase-1 of 6-phase IC-IBC is taken as an example to explain the coupling relationship more clearly. Phase-1 is inverse coupled with Phase-2 and Phase-6. For the co-owned inductor between Phase-1 and Phase-2, L_{12} stands for the self-inductance of Phase-1 and L_{21} stands for the self-inductance of Phase-2. M_{21} denotes the mutual-inductance caused by Phase-2's current inside the magnetic core and acts to Phase-1. M_{12} is just the opposite. The case is the same for the co-owned inductor between Phase-1 and Phase-6. The coupling relationship of other phases is analogous. Hence, different from the average model of UC-IBC as (3.3), the average model of the 6-phase IC-IBC is given in (3.2.20):

$$\left\{ \begin{array}{l} \left(L_{12} \cdot \frac{di_{L1}}{dt} - M_{21} \cdot \frac{di_{L2}}{dt} \right) + \left(L_{16} \cdot \frac{di_{L1}}{dt} - M_{61} \cdot \frac{di_{L6}}{dt} \right) = v_{in} - (1-d_1) \times v_o - i_{L1} \times (R_L + R_{on}) \\ \left(L_{23} \cdot \frac{di_{L2}}{dt} - M_{32} \cdot \frac{di_{L3}}{dt} \right) + \left(L_{21} \cdot \frac{di_{L2}}{dt} - M_{12} \cdot \frac{di_{L1}}{dt} \right) = v_{in} - (1-d_2) \times v_o - i_{L2} \times (R_L + R_{on}) \\ \left(L_{34} \cdot \frac{di_{L3}}{dt} - M_{43} \cdot \frac{di_{L4}}{dt} \right) + \left(L_{32} \cdot \frac{di_{L3}}{dt} - M_{23} \cdot \frac{di_{L2}}{dt} \right) = v_{in} - (1-d_3) \times v_o - i_{L3} \times (R_L + R_{on}) \\ \left(L_{45} \cdot \frac{di_{L4}}{dt} - M_{54} \cdot \frac{di_{L5}}{dt} \right) + \left(L_{43} \cdot \frac{di_{L4}}{dt} - M_{34} \cdot \frac{di_{L3}}{dt} \right) = v_{in} - (1-d_4) \times v_o - i_{L4} \times (R_L + R_{on}) \\ \left(L_{56} \cdot \frac{di_{L5}}{dt} - M_{65} \cdot \frac{di_{L6}}{dt} \right) + \left(L_{54} \cdot \frac{di_{L5}}{dt} - M_{45} \cdot \frac{di_{L4}}{dt} \right) = v_{in} - (1-d_5) \times v_o - i_{L5} \times (R_L + R_{on}) \\ \left(L_{61} \cdot \frac{di_{L6}}{dt} - M_{16} \cdot \frac{di_{L1}}{dt} \right) + \left(L_{65} \cdot \frac{di_{L6}}{dt} - M_{56} \cdot \frac{di_{L5}}{dt} \right) = v_{in} - (1-d_6) \times v_o - i_{L6} \times (R_L + R_{on}) \end{array} \right. \quad (3.2.20)$$

According to the operating process, the state space model of the proposed

converter can be obtained as described by (3.2.21). The duty cycle of each phase as a function of time, which is presented by (3.2.22), can be achieved based on the equations mentioned previously.

$$\frac{d}{dt}[I_{L_n}] = [L]^{-1} \times ([V_{in}] - [1-D_n] \times V_o - [i_{L_n}] \times (R_L + R_{on})) \quad (3.2.21)$$

$$[D_n(t)] = 1 - \frac{1}{V_o} \times \begin{pmatrix} [V_{in}] + (R_L + R_{on}) \times [I_{L_n}] \\ + [L_A] \times [-\lambda_{L_n} \times S_n + I_{L_n_ref}' - K_{L_n} \times \varepsilon_n] \end{pmatrix} \quad (3.2.22)$$

The matrixes $[L]$ and $[L_A]$ are separately the inverse coupled inductor matrix and the similar matrix of its inverse matrix. They are presented as follow. Due to (3.2.22), the control inputs are independent and will not be influenced by the disturbance of loads.

$$[L] = \begin{bmatrix} 2L & -M & 0 & 0 & 0 & -M \\ -M & 2L & -M & 0 & 0 & 0 \\ 0 & -M & 2L & -M & 0 & 0 \\ 0 & 0 & -M & 2L & -M & 0 \\ 0 & 0 & 0 & -M & 2L & -M \\ -M & 0 & 0 & 0 & -M & 2L \end{bmatrix}_{6 \times 6}$$

$$[L_A] = \begin{bmatrix} \frac{1}{2(L-M)} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{2(L+M)} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{2L-M} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{2L-M} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{2L+M} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{2L+M} \end{bmatrix}_{6 \times 6}$$

Combining (3.2.15), (3.2.19) and (3.2.22) together, (3.2.23) can be obtained:

$$\varepsilon' + \varepsilon \times (\lambda_{L_n} + K_{L_n}) + \lambda_{L_n} \times K_{L_n} \times \int_0^t \varepsilon d\tau = 0 \quad (3.2.23)$$

The time derivative of (3.2.23) is

$$\varepsilon'' + \varepsilon' \times (\lambda_{L_n} + K_{L_n}) + \lambda_{L_n} \times K_{L_n} \times \varepsilon = 0 \quad (3.2.24)$$

This equation is independent regarding the topology parameters, which means a high robustness for the controller. The classical tuning method for second-order systems can be used to determine the coefficients K_{L_n} and the convergence factors

λ_{L_n} to achieve the desired performance. According to the specifications and parameters of 6-phase IC-IBC, K_{L_n} and λ_{L_n} have been obtained as -2000 and 5000.

3.2.3 The state-space representations of 6-phase UC-IBC and IC-IBC

Here, the state-space representations for 6-phase UC-IBC and the proposed 6-phased IC-IBC are presented separately.

$$\begin{cases} K \cdot \frac{dx(t)}{dt} = A \cdot x(t) + B \cdot u(t) \\ y(t) = C \cdot x(t) + E \cdot u(t) \end{cases} \quad (3.2.25)$$

$u(t)$ stands for the input variables; $y(t)$ stands for the output variables; $x(t)$ stands for the state variables which contains the inductor current and capacitor voltage. A , B , C and E are the constant matrix and the coefficient matrix K consists the inductor value, capacitor value and mutual inductor value. According to the analysis done previously, the difference between UC-IBC and IC-IBC is the coefficient matrix. This phenomenon is depending on the inherent characteristics of each topology. The parameters of State-Space Representation for each topology are presented as follow:

1) 6-phase UC-IBC

a. the input variables, the output variables and the state variables are respectively presented as follow:

$$x(t) = \begin{bmatrix} i_{L_1}(t) \\ i_{L_2}(t) \\ \dots \\ i_{L_n}(t) \\ v_o(t) \end{bmatrix}_{(n+1) \times 1} \quad u(t) = \begin{bmatrix} v_{in}(t) \\ 0 \end{bmatrix} \quad y(t) = i_{in}(t)$$

b. the constant matrixes are respectively presented as follow:

$$B_1 = \begin{bmatrix} 1 & -D' \\ 0 & 0 \end{bmatrix} \quad C_1 = [1 \quad 1 \quad \dots \quad 1 \quad 0]_{1 \times (n+1)} \quad E_1 = [0 \quad 0]$$

$$A_1 = \begin{bmatrix} -(R_L + D \times R_{on})_1 & 0 & \dots & 0 & -D'_1 \\ 0 & (R_L + D \times R_{on})_2 & \dots & 0 & -D'_2 \\ \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & \dots & (R_L + D \times R_{on})_n & -D'_n \\ -D'_1 & -D'_2 & \dots & -D'_n & -\frac{1}{R_o} \end{bmatrix}_{(n+1) \times (n+1)}$$

c. the coefficient matrix is presented as follow:

$$K_1 = \begin{bmatrix} L_1 & 0 & \dots & 0 & 0 \\ 0 & L_2 & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & \dots & L_n & 0 \\ 0 & 0 & \dots & 0 & C \end{bmatrix}_{(n+1) \times (n+1)}$$

2) 6-phase IC-IBC

a. the input variables, the output variables and the state variables are respectively presented as follow:

$$x(t) = \begin{bmatrix} i_{L_1}(t) \\ i_{L_2}(t) \\ \dots \\ i_{L_n}(t) \\ v_o(t) \end{bmatrix}_{(n+1) \times 1} \quad u(t) = \begin{bmatrix} v_{in}(t) \\ 0 \end{bmatrix} \quad y(t) = i_{in}(t)$$

b. the constant matrixes are respectively presented as follow:

$$B_2 = \begin{bmatrix} 1 & -D' \\ 0 & 0 \end{bmatrix} \quad C_2 = [1 \quad 1 \quad \dots \quad 1 \quad 0]_{1 \times (n+1)} \quad E_2 = [0 \quad 0]$$

$$A_2 = \begin{bmatrix} -(R_L + D \times R_{on})_1 & 0 & \dots & 0 & -D'_1 \\ 0 & (R_L + D \times R_{on})_2 & \dots & 0 & -D'_2 \\ \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & \dots & (R_L + D \times R_{on})_n & -D'_n \\ -D'_1 & -D'_2 & \dots & -D'_n & -\frac{1}{R_o} \end{bmatrix}_{(n+1) \times (n+1)}$$

c. the coefficient matrix is presented as follow:

$$K_2 = \begin{bmatrix} 2L_1 & -M & 0 & \dots & -M & 0 \\ -M & 2L_2 & -M & \dots & 0 & 0 \\ 0 & -M & 2L_3 & \dots & 0 & 0 \\ 0 & 0 & \dots & 2L_{n-1} & -M & \dots \\ -M & 0 & \dots & -M & 2L_n & 0 \\ 0 & 0 & 0 & \dots & 0 & C \end{bmatrix}_{(n+1) \times (n+1)}$$

3.3. Analysis of simulation results

In order to verify the control strategies designed previously, some simulations have been realized for both topologies discussed in the previous sections (6-phase UC-IBC and 6-phase IC-IBC). The PLECS software from Plexim [3-5], which

focuses on simulation of electrical engineering, has been utilized. This software is very useful and very well-known for the simulation in power electronics.

3.3.1 Comparison of electrical part simulation

The electrical part simulation results of UC-IBC and IC-IBC are presented and compared in the following subsection. The purpose of this comparative analysis is to evaluate the correctness of each converter's electrical model and the stability of corresponding control strategy. The performances of DC bus voltage, inductor current, input voltage and input current will be mainly focused. Each variable will be verified under both loading and unloading operation. The important parameters are summarized as Table.3.1.

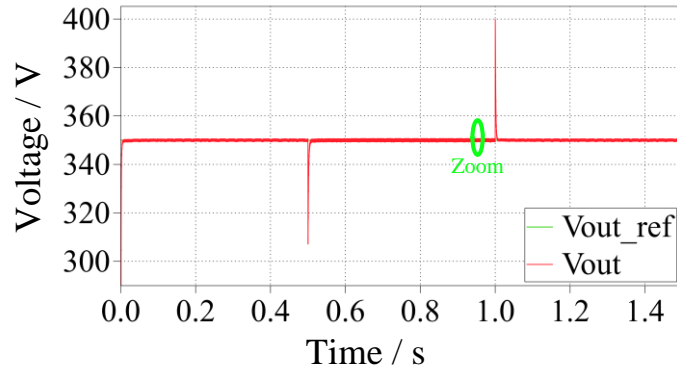
Table.3.1 Simulation parameters of UC-IBC and IC-IBC

Symbol	Parameter	UC-IBC	IC-IBC	Unit
L	Inductor	$56*10^{-6}$	--	H
L_s	Self-inductor	--	$37*10^{-6}$	H
M	Mutual-inductor	--	$19*10^{-6}$	H
k	Coupling coefficient	--	-0.51	--
R_L	Winding resistance	$10*10^{-3}$	$10*10^{-3}$	Ω
R_M	Mutual resistance	--	$5*10^{-3}$	Ω
R_{mos_on}	MOSFET conduction resistance	$43*10^{-3}$	$43*10^{-3}$	Ω
t_r	Rising time of MOSFET	$32*10^{-9}$	$32*10^{-9}$	s
t_f	Falling time of MOSFET	$28*10^{-9}$	$28*10^{-9}$	s
V_F	Forward voltage of diode	1.5	1.5	V
R_{dio_on}	Diode conduction resistance	$12.5*10^{-3}$	$12.5*10^{-3}$	Ω
C	Capacitor	$10*10^{-6}$	$10*10^{-6}$	F
R_{ESR}	Capacitor equivalent series resistance	$10*10^{-6}$	$10*10^{-6}$	Ω

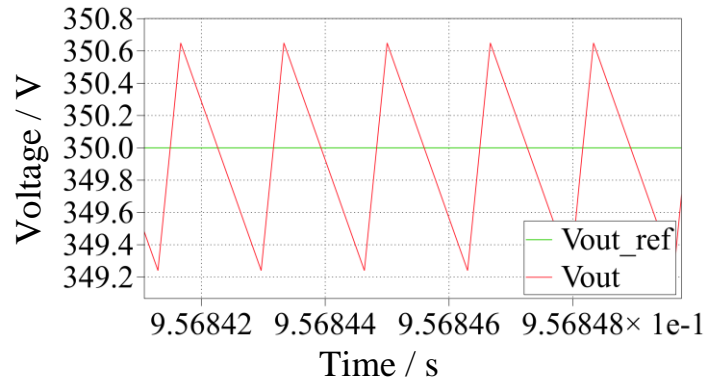
3.3.1.1 The verification of DC bus voltage

The DC bus voltage's waveforms (V_{out}) of UC-IBC and IC-IBC are separately presented in Fig.3.7 and Fig.3.8. In order to clearly observe the operating details, zooms of V_{out} have been made for each result under the nominal condition. As analyzed previously, the DC bus voltages of both converters are all regulated based on PI controllers. According to the results, the DC bus voltage of each converter has been well controlled around the V_{out} reference (350V) no matter under loading condition or unloading condition. The DC bus voltage's ripples are all at extremely low level: 0.4% for UC-IBC and 0.43% for IC-IBC. Thus, the DC bus voltage's closed loop control of

each converter has been realized.

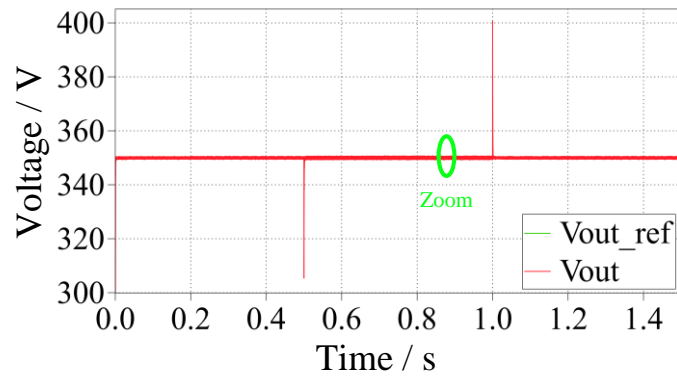


(a) V_{out_UC-IBC}

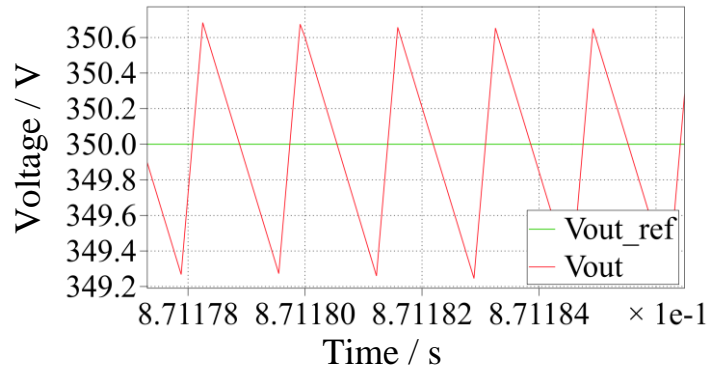


(b) Zoom of (a)

Fig.3.7 Simulation results of UC-IBC's DC bus voltage (V_{out_UC-IBC}) and zoom



(a) V_{out_IC-IBC}

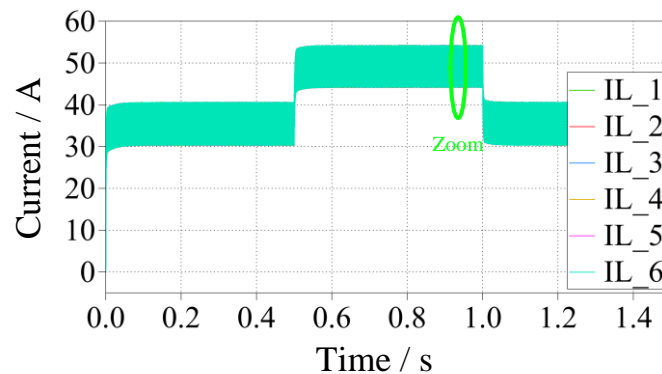


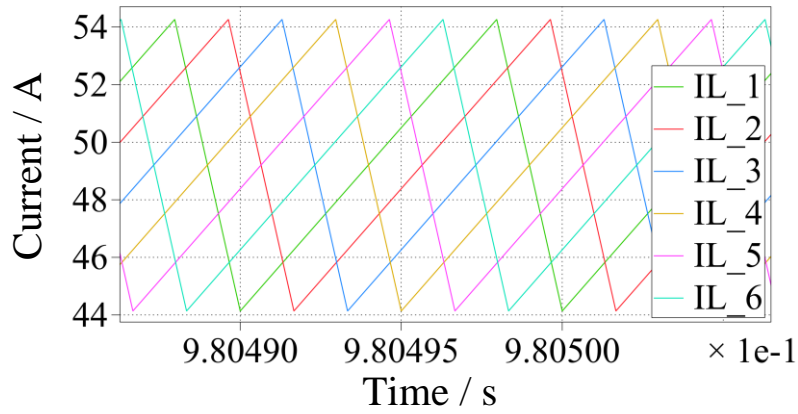
(b) Zoom of (a)

Fig.3.8 Simulation results of IC-IBC's DC bus voltage (V_{out_IC-IBC}) and zoom

3.3.1.2 The verification of inductor current

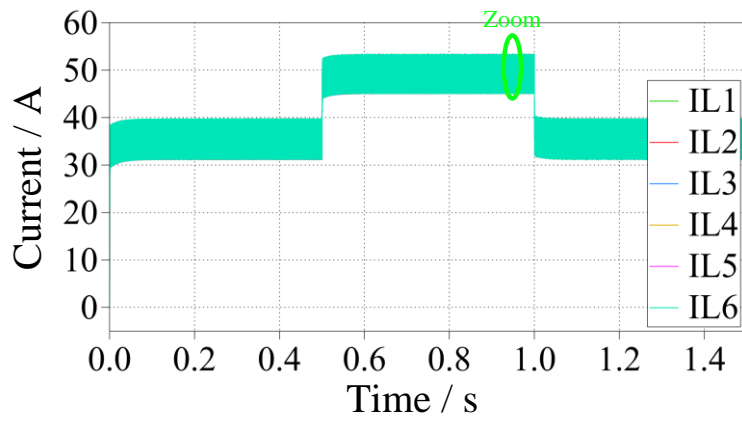
The inductor current's waveforms (I_L) of UC-IBC and IC-IBC are separately presented in Fig.3.9 and Fig.3.10. In order to clearly observe the operating details, zooms of I_L have been made for each result under the nominal condition. As analyzed previously, the inductor currents of UC-IBC and IC-IBC are separately controlled by PI controller and SMC controller. Obviously, a delay exists between adjacent phases according to the interleaved control strategy. According to the results, the inductor current of each converter has been well controlled around I_L 's reference no matter under loading condition or unloading condition. The inductor current's ripples are 20% and 16% for both UC-IBC and IC-IBC separately. To be emphasized, the inductor's current ripple of inverse coupled inductor is influenced by the self-inductance (L_s) and the mutual-inductance (M). For IC-IBC, L_s equals 37 μ H and M equals 19 μ H. The coupling coefficient is set to -0.51 to obtain lower input current ripple. Thus, the inductor current's closed loop control of each converter has been realized.

(a) I_{L_UC-IBC} , phase 1~6

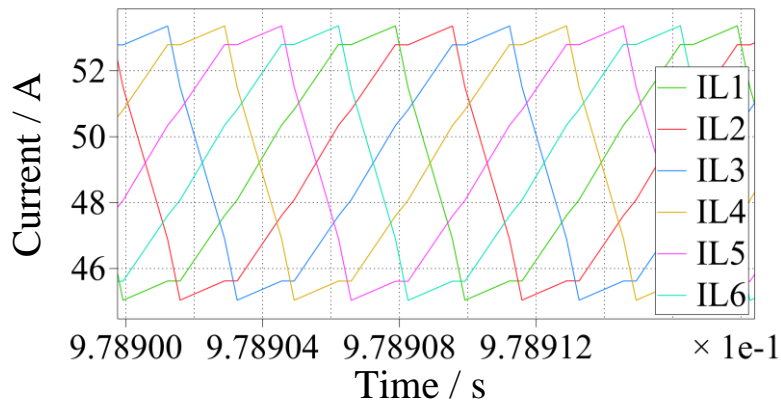


(b) Zoom of (a)

Fig.3.9 Simulation results of UC-IBC's inductor currents ($I_{L_{UC-IBC}}$) and zoom



(a) $I_{L_{IC-IBC}}$, phase 1~6

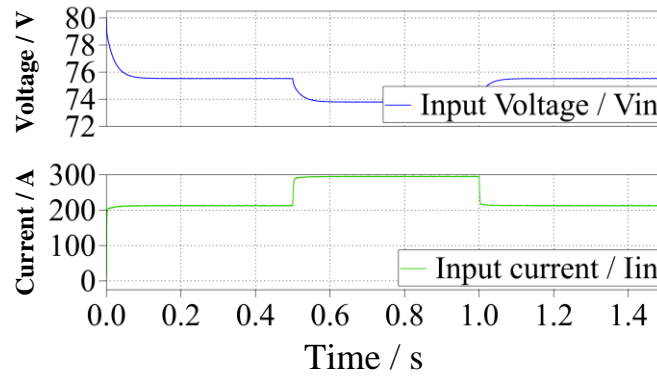
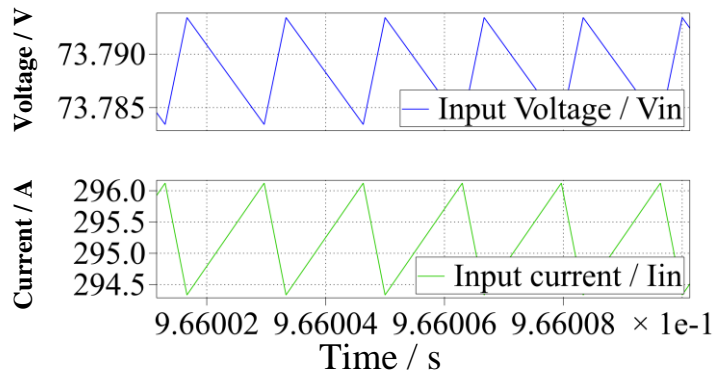


(b) Zoom of (a)

Fig.3.10 Simulation results of IC-IBC's inductor currents ($I_{L_{IC-IBC}}$) and zoom

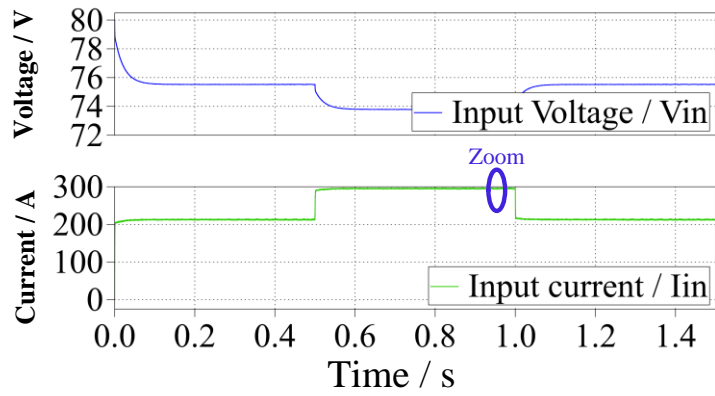
3.3.1.3 The verification of input current and input voltage

The Randles circuit is used as the FC model during the simulation. Unlike a constant voltage source, the Randles circuit's output voltage and current change during loading and unloading period, as presented in Fig.3.11 and Fig.3.12. Obviously, the input voltages of both converters are not constant values. According to the results, the input current ripples of both converters are quite small: 1.5A for UC-IBC and 2.5A for IC-IBC. As analyzed in chapter. 2, the FC current ripple of UC-IBC is only relied to the duty cycle. For IC-IBC, not only the duty cycle but also the coupling coefficient will also influence the FC current ripple. When a good coupling coefficient is selected, the FC current ripple of IC-IBC can also be kept at a low level. The simulation results of both converters' DC bus currents are also presented in Fig.3.13 and Fig.3.14.

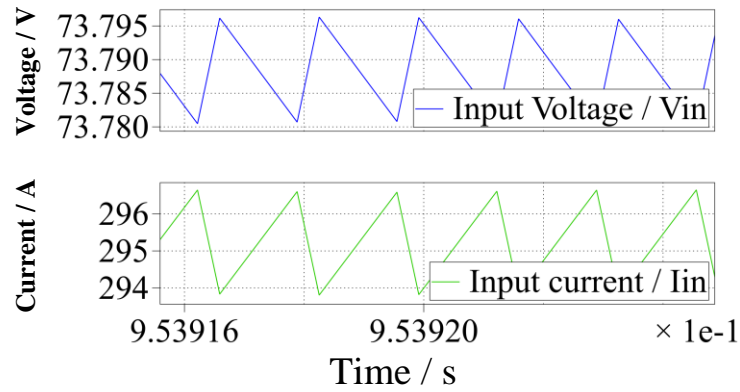
(a) V_{in} and I_{in} of UC-IBC

(b) Zoom of (a)

Fig.3.11 Simulation results of UC-IBC's input voltage (V_{in}), input current (I_{in}) and zooms

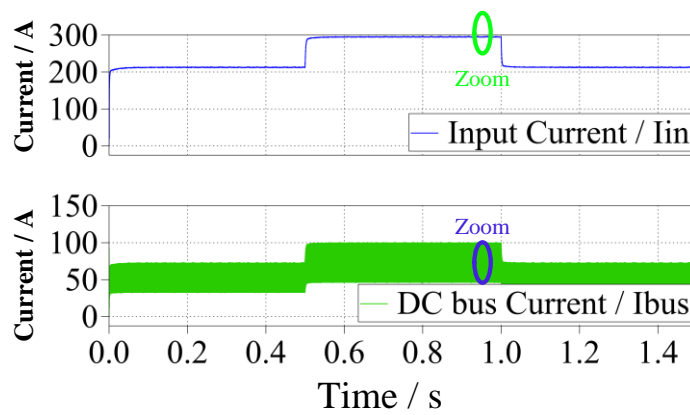


(a) V_{in} and I_{in} of IC-IBC

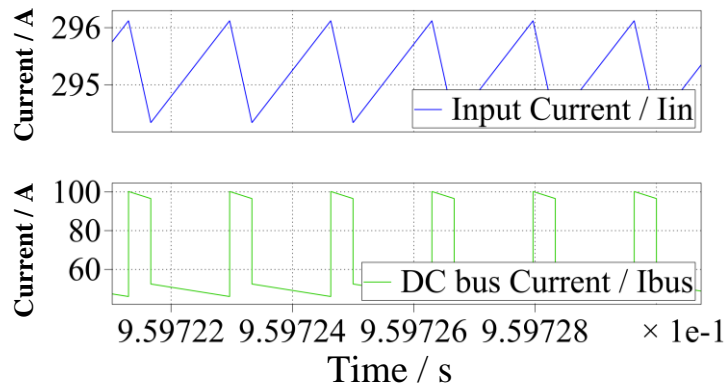


(b) Zoom of (a)

Fig.3.12 Simulation results of IC-IBC's input voltage (V_{in}), input current (I_{in}) and zooms

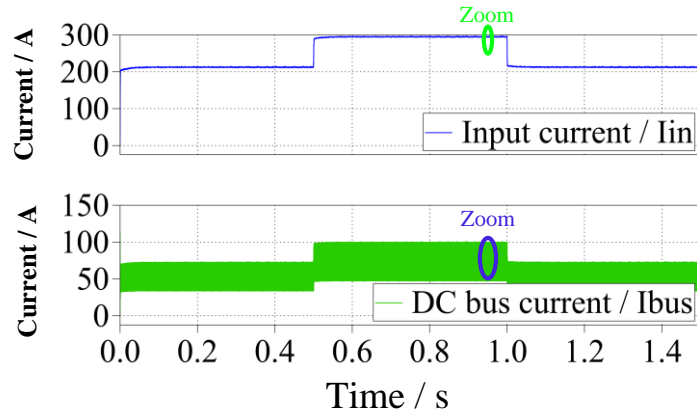


(a) I_{in} and I_{DC_bus} of UC-IBC

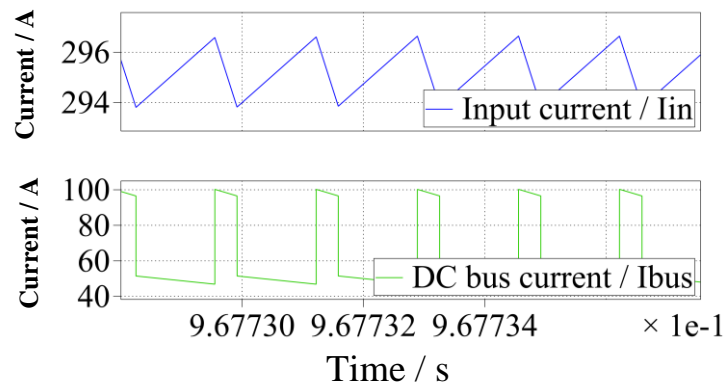


(b) Zoom of (a)

Fig.3.13 Simulation results of UC-IBC's input current (I_{in}), DC bus current (I_{DC_bus}) and zooms



(a) I_{in} and I_{DC_bus} of IC-IBC



(b) Zoom of (a)

Fig.3.14 Simulation results of IC-IBC's input current (I_{in}), DC bus current (I_{DC_bus}) and zooms

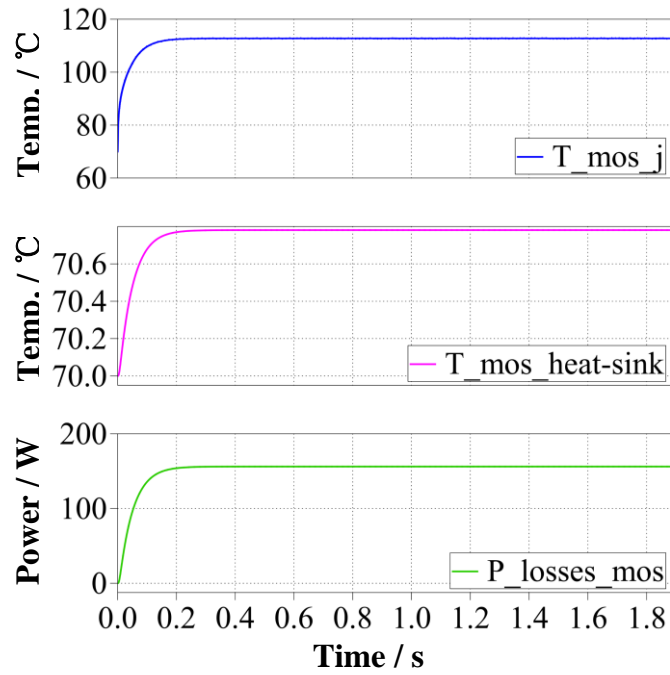
3.3.2 Comparison of thermal part simulation

PLECS provides the blocksets to implement thermal analysis for MOSFET and Schottky diode based on their thermal parameters from datasheets. In chapter.2, it has been concluded that for IC-IBC, multiple MOSFETs and Schottky diodes that are constructed in parallel can reduce total power losses and increase thermal performance. Depending on the study, two MOSFETs and two Schottky diodes constructed in parallel per phase is the best comprise for the efficiency, power losses, volume, thermal performance and price. Here, the thermal evaluations of IC-IBC are implemented. Single MOSFET and Schottky diode per phase (Config.1) and two of each contrasted in parallel per phase (Config.2) are all carried out. The SiC MOSFET's part number is C2M0025120D from CREE[®] (Wolfspeed group) and the SiC Schottky diode's part number is C4D40120D produced by CREE[®] (Wolfspeed group). Their thermal parameters can be obtained based on the datasheets.

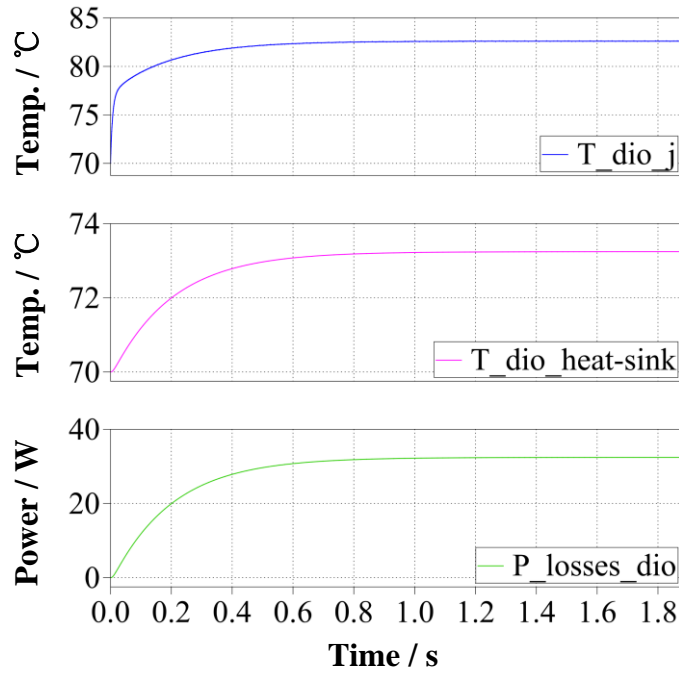
The ambient temperature is set to 70°C. The heat-sink's initial temperature is set to 70°C. Here, the discrete heat-sink is selected for MOSFET and diode to reduce the volume and weight. For Config.1, the heat-sink' thermal resistance is set as 0.005°C/W (SiC MOSFET) and 0.1°C/W (SiC Schottky diode); for Config.2, the heat-sinks' thermal resistances are set as 0.5°C/W for both SiC MOSFET and SiC Schottky diode. The thermal performances at the nominal power are analyzed in Fig.3.15 and Fig.3.16. When constructed singly, SiC MOSFET's junction temperature reaches 110°C while SiC Schottky diode's junction temperature reaches 82.5°C at the steady state. For the construction that features two SiC MOSFETs and two SiC Schottky diodes in parallel per phase, MOSFET's junction temperature reaches 102°C while diode's junction temperature reaches 78°C. The semiconductor junction temperature comparison of two configurations is presented in Table.3.2.

Table.3.2 Junction temperature comparison

	Config.1	Config.2
T_{ambient}	70°C	70°C
T_{mos_j}	110°C	102°C
$T_{\text{mos_heat-sink}}$	70.8°C	90°C
T_{dio_j}	82.5°C	78°C
$T_{\text{dio_heat-sink}}$	73°C	74.8°C

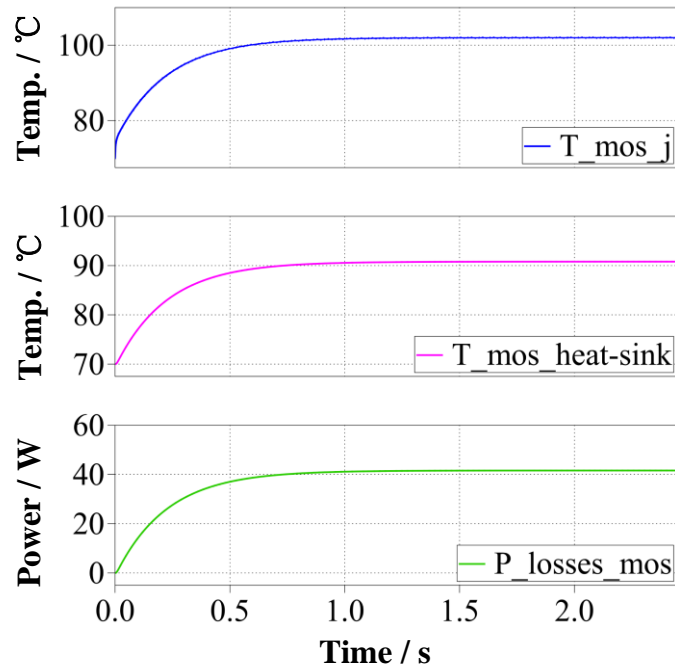


(a) SiC MOSFET

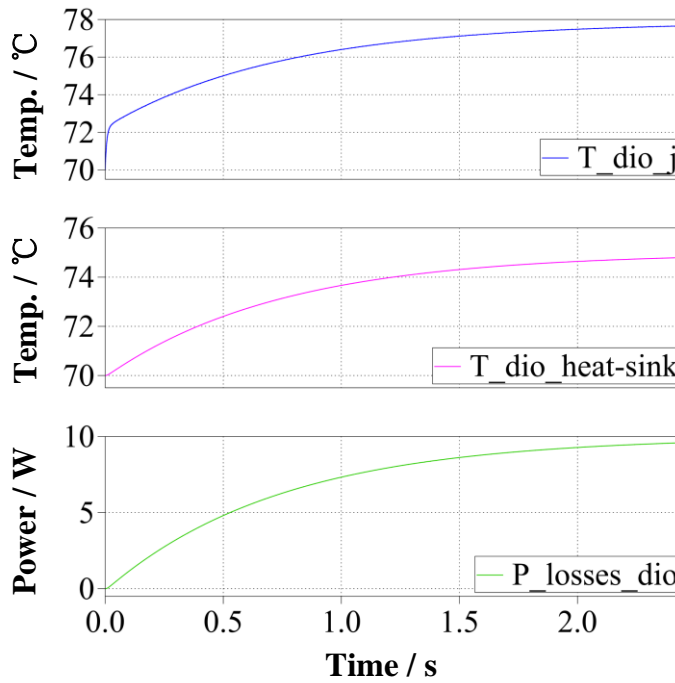


(b) SiC Schottky diode

Fig.3.15 Steady state thermal performance of IC-IBC at the nominal power (single active device per phase)



(a). SiC MOSFET



(b). SiC Schottky diode

Fig.3.16 Steady state thermal performance of IC-IBC at the nominal power (two active devices in parallel per phase)

3.4. Conclusion

In this chapter, the design process of control strategy for the proposed 6-phase IC-IBC has been studied. In order to make a comparison, 6-phase UC-IBC has been addressed to well explain the procedures. Firstly, the dynamic models of both UC-IBC and proposed IC-IBC have been analyzed. Dual loop PI controller has been applied to UC-IBC while Sliding-Mode Control has been adopted by the proposed IC-IBC. Hence, the high non-linear characteristic of inverse coupled inductors, which have been utilized by the proposed topology, have been satisfied. The general State-Space Representations of both topologies have also been presented. Some typical simulation results of both topologies have been given and analyzed to verify the performance of the proposed control strategy. Finally, closed loop control has been realized and the required specifications of the converter have been satisfied.

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Chapter 4: On-line Electrochemical Impedance Spectroscopy

4.1. Introduction

So far, general lifespan of PEMFC cannot reach the expectation of commercial application. For example, a typical life expectancy of the PEMFC under actual transportation constraints is around 3000 h, whereas transportation applications require at least 5000 h [4-1]. Hence, one of the primary assignment to be solved for universal application of PEMFC is to increase its reliability and durability. Indeed, the manufacturing of PEMFC is mainly depending on high cost materials (platinum catalyst, acid membrane, etc.) with limited durability especially in unstable operations and cyclic stress operation.

Concerning these limitations, various faults can occur on PEMFC during operating condition. Short-circuit, whose response time is relatively short (10^{-6} ~ 10^{-2} s), can lead to membrane and catalyst layer degradation [4-2]. Starvation, which can cause catalytic layer degradation, has been defined as an undersupply of reactants that could occur either at local or global level [4-3]. CO poisoning owns a relative long response time (10^1 ~ 10^5 s) and can issue in performance losses and then starvation of PEMFC [4-4].

Actually, presence of liquid water inside PEMFC can impede performance and durability of the system. Thus, the water management inside cells is one of the key problems needed to be better understood. Under normal operation, the membrane of PEMFC is required to be wet. However, improper operating temperatures, high air flow rates, and humidity can lead to inappropriate water content inside the membrane. These variations separately result in membrane drying or electrode flooding. Longstanding operation during these two states decreases the output power of the FC. Considering for example membrane drying out, it can be linked to low current demand, high gas flow rates, high operating temperature, poor humidified incoming gases, etc. As the membrane of the cell dries out, the voltage gradually drops. An increase in humidification improved the cell performance at high cell temperature due

to higher membrane conductivity but decreased the cell performance at low cell temperature and high current density due to cathode flooding [4-5].

The operating conditions of PEMFC are essential to be monitored and controlled for the purpose of extending lifespan of power source. Electrochemical Impedance Spectroscopy (EIS) is established as a powerful characterization tool to detect different failure mechanisms occurring in a FC. Impedance spectra can help to characterize a cell in a much more complete mode than just analyzing the polarization curve [4-6].

As analyzed in the previous chapters, PEMFC system's output voltage must be increased to 400V~700V by FC connected DC/DC boost converter to satisfy the requirement of motor drive system [4-7][1-15][1-18]. Based on this fact, harmonics generated by the FC power converter could be used to perform online diagnostic of the FC stack, without any additional device and thus, respecting the limited space available in a FCEV. This idea will be developed in this chapter. It is organized as follow. In section 4.2, the validity condition of EIS is demonstrated while the considered equivalent circuit model for the FC stack is given. The proposed on-line EIS detection process based on the proposed 6-phase IBC with inverse coupled inductors (6-phase IC-IBC) is analyzed in section 4.3. Some typical simulation results are also illustrated in this section. Several conclusions are drawn in the last section.

4.2. EIS fundamental

4.2.1. EIS validity conditions

According to the literature, linearity, causality, stability and finiteness are essential qualifications for an effective EIS measurement. Herein, linearity and stability are emphatically considered for EIS implementation [4-10].

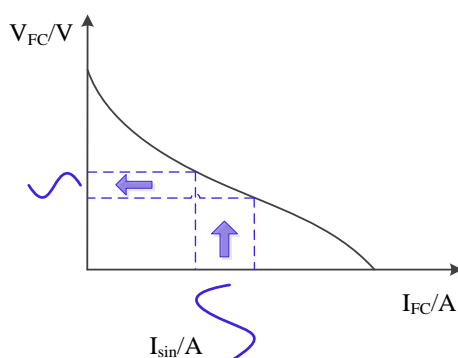


Fig.4.1 EIS achievement by injecting sinusoidal perturbation to IFC in the linear operating range

A linear system should satisfy the properties of superposition and scaling. To guarantee the linearity, the FC stack should work in a linear or quasi-linear region. In terms of the impedance, the acquired impedance should be irreverent to the amplitude of the perturbation signal when the linearity condition is met. However, certain cautions should be noted: firstly, in order to guarantee a good signal-to-noise ratio, the amplitude of the perturbation should be larger than the system noises; secondly, the amplitude should not be too large for not disturbing the operating point of the stack. A suggested range for the AC current's amplitude in galvanostatic mode is classically about 5%~10% of the stack DC current [4-11].

The stability condition requires that the system works in the same stable state before and after the perturbation. The stable operating state is usually characterized by a steady-state stack voltage and stack temperature. The EIS measurements should also be stationary, which means it is time-independent. This condition can be easily verified by repeating the measurements and check the consistency of the obtained Nyquist plot.

4.2.2. Equivalent circuit model of the FC stack

Electrical characteristic of a FC can be represented by an equivalent circuit model. The most common equivalent circuit is the Randles circuit proposed by Randles [4-12]. As presented in Fig.4.2, membrane resistance R_m is connected in series with a parallel combination of the double layer capacitor C_{dl} and the catalyst resistance R_c .

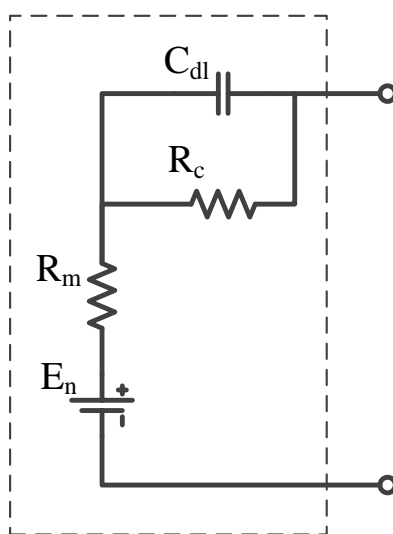


Fig.4.2 FC simple model based on Randles circuit

According to principles described in [4-10], the resistance R_m stands for the resistance against the proton transfer through the membrane (note that water content in the membrane has much influence on this proton transfer property. As for the double layer capacitor C_{dl} , it stands for the capacitance property in the catalyst layer where electrochemical reactions happen. Of course, the resistance R_c stands for the resistance against the charge transfer around the catalyst layer. In addition, the Nernst voltage of the FC is defined as [4-13]. E , p_{H_2} , p_{H_2O} , and p_{O_2} are the Nernst voltage in standard state, hydrogen partial pressure, water vapor partial pressure and oxygen partial pressure against the standard atmosphere pressure respectively.

$$E_n = E + \frac{RT}{2F} \ln \left(\frac{p_{H_2} \times p_{O_2}^{0.5}}{p_{H_2O}} \right) \quad (4.2.1)$$

For this equivalent circuit, the total impedance can be defined as (4.2.2)

$$Z_\omega = R_m + \frac{R_c}{jC_{dl}R_c\omega + 1} \quad (4.2.2)$$

where ω stands for the angular frequency. According to (4.2.2), the impedance Z_ω is equal to $(R_m + R_c)$ approximately when the frequency f is close to zero.

4.3.on-line EIS detection process based on 6-phase IC-IBC

In consideration of the limited effective volume of FCEV, the integration of EIS functionality in control strategy of converter is a promising technique in purpose of realizing on-line monitoring the state of health of FC [4-10]. The strategy of EIS integration in SMC consists in injecting a current perturbation I_{sin} around the polarization current I_{FC} as presented in Fig.4.3. In this figure, a time delay (T_{delay}) exists between neighbor phases drive signals (PWM Phase N). This value depends on the number of phases (N) and the cycle period (T_s). In our case, N and T_s separately equal to 6 and 10 μs . Thus, T_{delay} can be achieved as $(10/6) \mu s$.

At nominal conditions, DC bus voltage (V_o) will be compared with the reference voltage (V_{ref}), and then the difference will be transferred to a PI controller (out loop controller) to obtain the current reference (I_{L_ref}) for each phase. After that, I_{L_ref} , FC voltage (V_{FC}), FC current (I_{FC}) and inductor current (I_L) of each phase will be sent into the Sliding Mode Controller (SMC), which is an inner loop controller. After the calculation process, PWM control orders can be obtained and will be sent to corresponding power MOSFET as drive signal.

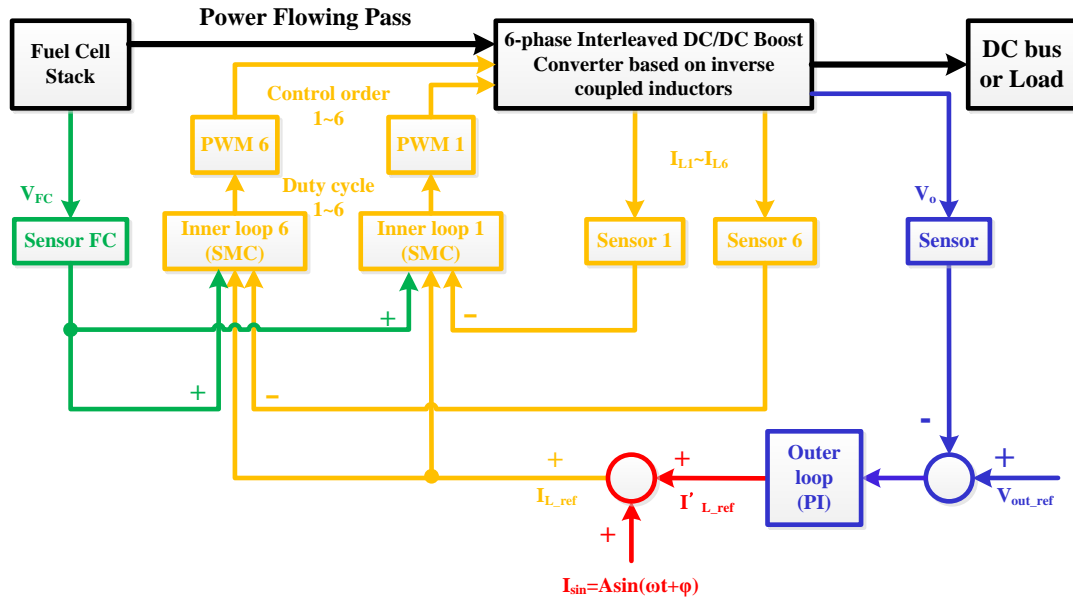


Fig.4.3 The strategy of EIS integration in SMC

According to the existed literatures, on-line EIS functionality has been integrated with the conventional Boost converter [4-14] [4-15] [4-16] and the full bridge converter [4-17]. In these studies, normally the PI and PID controllers are used. However, depending on [4-15], the perturbation inserting based on PI control strategy is strongly depending on the bandwidth of control loop. In [4-15], the conventional Boost converter is selected and the dual-loop (inner current loop, outer voltage loop) PI control strategy is developed. As a matter of fact, when a low frequency AC perturbation signal is superimposed directly to the current reference, it can also induce a perturbed power flow from FC to the DC bus through the converter. The DC bus voltage will also fluctuate. This fluctuation is detected by voltage sensor and the voltage loop controller is devoted to cancel it and produce the appropriate FC current reference. In other words, the injected low frequency AC perturbation signal will be compensated by the outer loop. The perturbation inserting is ineffective. Therefore, as summarized in [4-15], when PI controller is used for on-line EIS detection based on FC connected converter, high frequency perturbation is suitable to be injected in the current reference directly while low frequency perturbation is appropriate to be injected in the voltage reference.

In this thesis, SMC controller is developed to satisfy the high non-linear characteristic of the proposed 6-phase IC-IBC. The AC perturbation is injected to the

inductor current reference directly no matter the signal's frequency is high or low. This strategy relies on SMC's high robust to parameter variations and inherent insensitivity to the disturbance. Thus, the injected AC perturbation will not be compensated.

4.3.1. Detection process analysis

On-line detection of EIS based on the 6-phase IBC is presented by Fig.4.4. The process can only be handled when the FC stack operates at stable state, which is usually characterized by a steady-state stack voltage and stack temperature [4-10]. When the EIS monitoring is required, a controlled sinusoidal perturbation will be superimposed to the output signal of the PI controller (I_{L_ref}). According to the process of SMC, the current of each phase will track this new reference value. Thus, the sinusoidal perturbation can be superimposed successfully to the FC stack current. Owing to operate at linear range, the FC voltage will also be perturbed by a sinusoidal signal obtained at the same frequency as the current perturbation. Under this condition, the mean values of the FC stack output voltage and current can be obtained separately. These two parameters are essential for the measurement of AC impedance. Meanwhile, benefiting from the high robustness of this control strategy, the output voltage of the IBC can still be maintained relatively constant and for sure under the required constraints (<20% of average value).

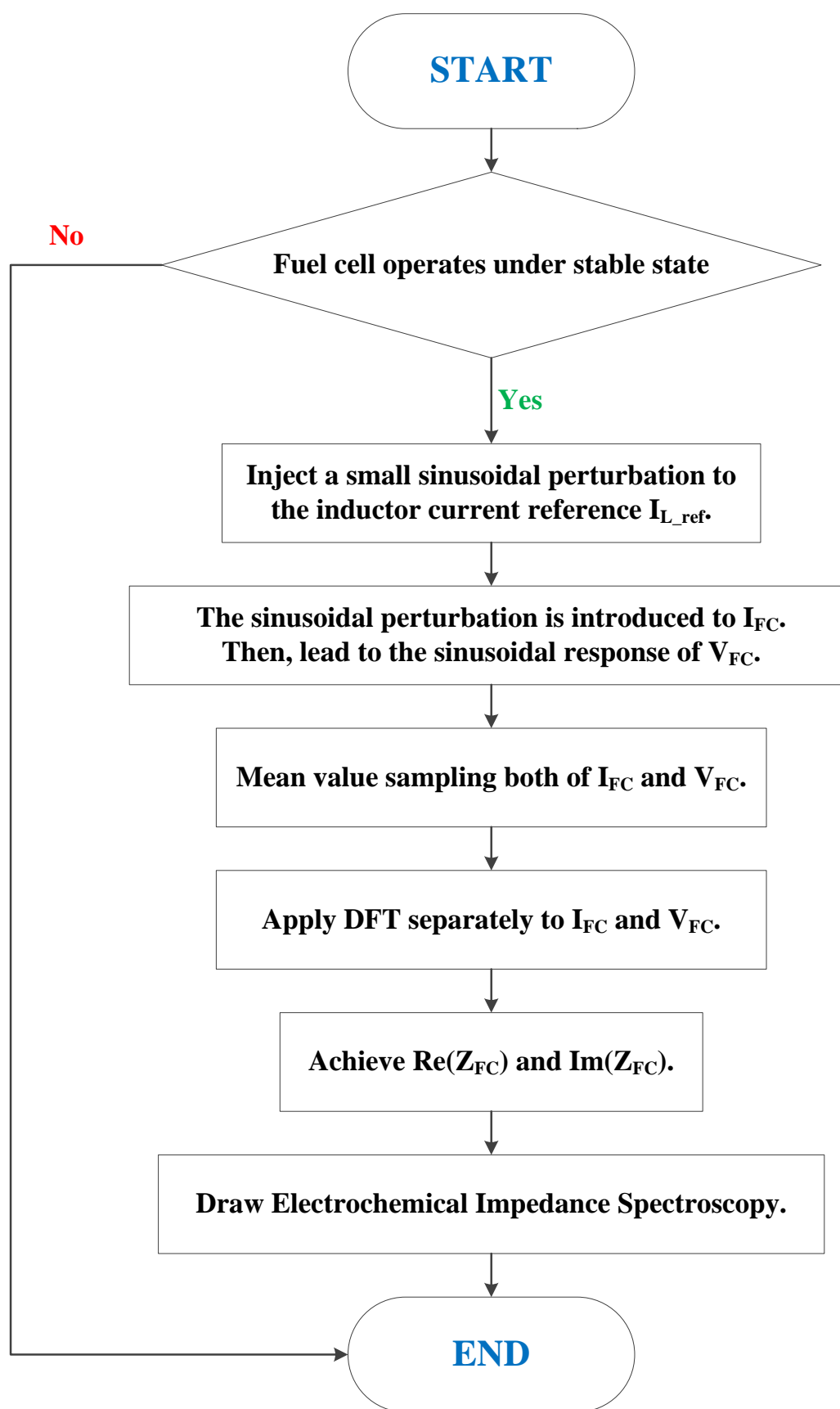


Fig.4.4 The process flow diagram of on-line detection of EIS based on 6-phase IBC

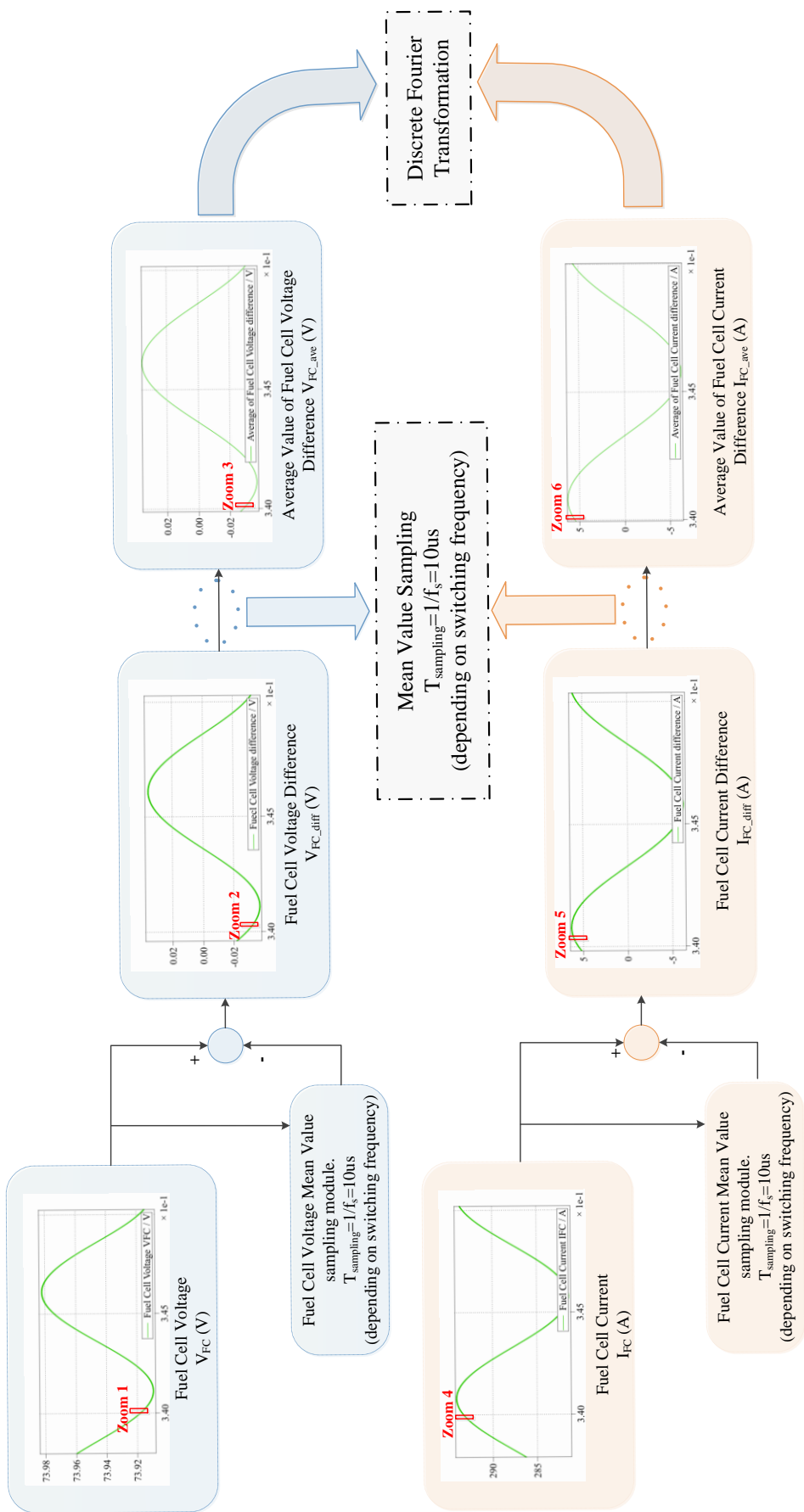
In order to illustrate the principle of AC impedance measurement, hence, the sampling process of FC stack current is taken as an example. The sampling processes both for V_{FC} and I_{FC} are shown in Fig.4.5. Given from (b) to (g) are the zooms of typical signals, either FC voltage or current, which are essential during the procedures of the proposed strategy. A sinusoidal perturbation combined with frequency of 100Hz and amplitude of $\pm 1A$ is taken as an example in these figures.

The difference between FC current mean value and perturbation FC current is an AC component. The AC component is composed by the FC current ripple under steady state and a sinusoidal perturbation. The frequency of the FC current ripple equals to the switching frequency. Thus, the mean value of the AC component in each switching period can be calculated. A sinusoidal wave based on the same frequency as the perturbation signal, can be achieved.

This signal is the exact extracted signal, i_{FC_AC} , which is caused by the injected sinusoidal perturbation, I_{sin} . Perturbations combined with different frequencies can let to different responses of FC current and corresponding responses of FC voltage. These independent responses can be utilized to plot impedance spectrums.

Discrete Fourier Transform (DFT) is utilized to separate the real part and imaginary part of i_{FC_AC} . The sampling frequency (f_e) is set at ten times the value of the perturbation signal frequency. Thus, the number of samples (N_s) in one cycle of perturbation signal equals ten. In this study, i_{FC_AC} is a sine signal and the fundamental frequency component is the dominant part, hence, the highest order harmonic is selected as twenty-time harmonic which is enough to guarantee the precise of calculation result. The real part and imaginary part will be utilized to calculate the AC impedance of the FC stack.

With regards to the sampling process of the FC stack voltage under perturbed conditions, the principle is the same as illustrated in foregoing paragraphs.



(a) Sampling processes of V_{FC} and I_{FC} for EIS functionality

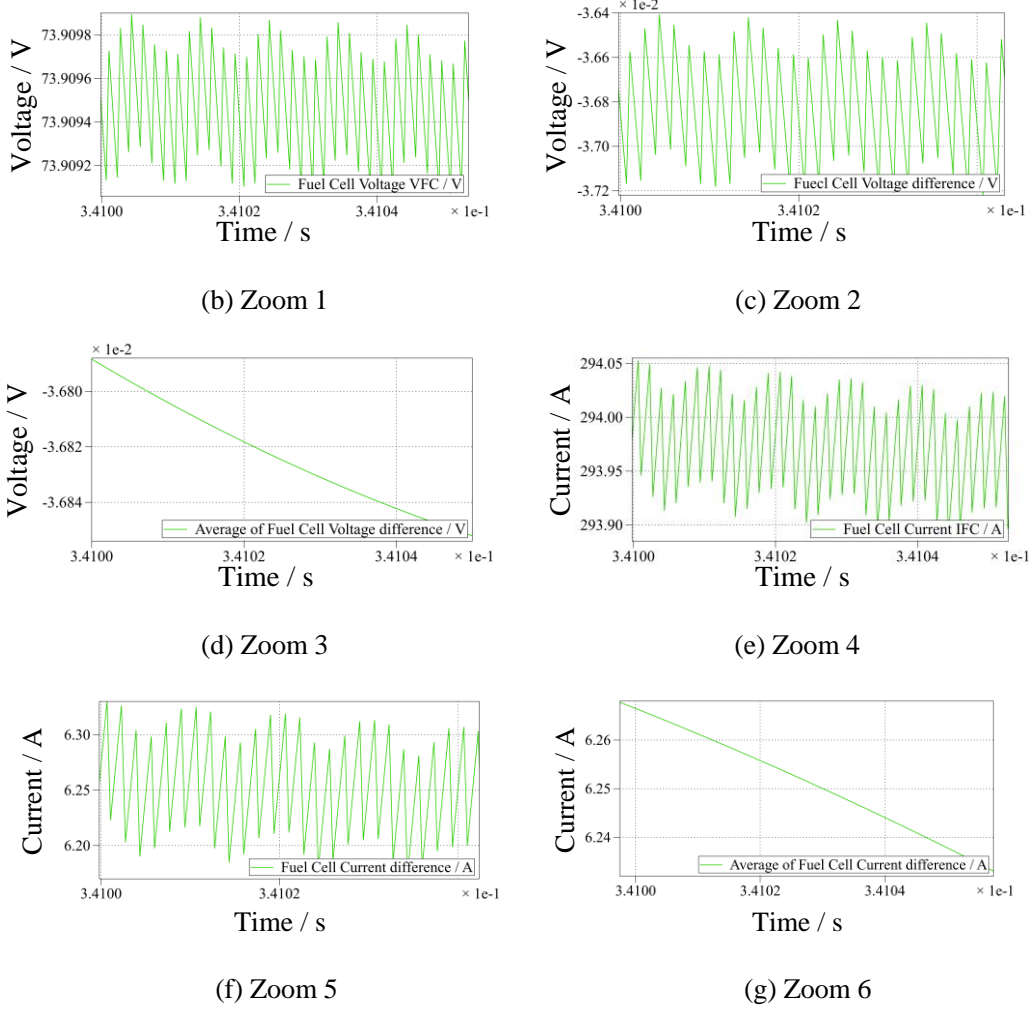


Fig.4.5 The processes of FC voltage and FC current sampling in purpose of the realization of EIS functionality.

Combining DFT and Euler's formula, the impedance of FC stack can be expressed as (4.3.1), (4.3.2) and (4.3.3) [4-18].

$$\begin{cases} \text{Re}(V_{FC}) = \sum_{n=0}^{N-1} V_{FC}(n) \times \cos\left(-\frac{2\pi}{N}nk\right) \\ \text{Im}(V_{FC}) = \sum_{n=0}^{N-1} V_{FC}(n) \times \sin\left(-\frac{2\pi}{N}nk\right) \end{cases}, k = 0, 1, \dots, N-1 \quad (4.3.1)$$

$$\begin{cases} \text{Re}(V_{FC}) = \sum_{n=0}^{N-1} V_{FC}(n) \times \cos\left(-\frac{2\pi}{N}nk\right) \\ \text{Im}(V_{FC}) = \sum_{n=0}^{N-1} V_{FC}(n) \times \sin\left(-\frac{2\pi}{N}nk\right) \end{cases}, k = 0, 1, \dots, N-1 \quad (4.3.2)$$

$$\left\{ \begin{array}{l} \bar{Z}_{FC} = \frac{V_{FC}}{I_{FC}} = \frac{\text{Re}(V_{FC}) + j \cdot \text{Im}(V_{FC})}{\text{Re}(I_{FC}) + j \cdot \text{Im}(I_{FC})} = \text{Re}(\bar{Z}_{FC}) + j \cdot \text{Im}(\bar{Z}_{FC}) \\ \text{Re}(\bar{Z}_{FC}) = \frac{\text{Re}(V_{FC}) \times \text{Re}(I_{FC}) + \text{Im}(V_{FC}) \times \text{Im}(I_{FC})}{\text{Re}^2(I_{FC}) + \text{Im}^2(I_{FC})} \\ \text{Im}(\bar{Z}_{FC}) = \frac{\text{Im}(V_{FC}) \times \text{Re}(I_{FC}) - \text{Re}(V_{FC}) \times \text{Im}(I_{FC})}{\text{Re}^2(I_{FC}) + \text{Im}^2(I_{FC})} \end{array} \right. \quad (4.3.3)$$

Normally, there is no limitation for the minimum frequency of the perturbation signal, but the maximum frequency shall be smaller than f_s/N_s . N_s stands for the number of samples and it is selected as 10 in our case in consideration with the sampling precision [4-18]. An impedance spectrum can be formed by a series of the stack impedances at discrete frequency points within a wide range of frequencies. The proposed converter, which is based on SiC semiconductors, makes it possible to obtain impedances at high frequency due to the ability of operating at high switching frequency. The frequency of stimulus signal is here designed from 1Hz to 10kHz.

Compared with the converters based on the classical Si semiconductors [4-14] ~ [4-18], the proposed 6-phase IC-IBC is based on SiC semiconductors and high switching frequency (100kHz) is selected. Thus, during on-line EIS detection, the perturbation signal can own high frequency. The maximum perturbation signal's frequency ($f_{\text{per_max}}$) is limited to one-tenth of the converter switching frequency (f_s) to avoid signal aliasing. Therefore, the frequency of perturbation signal is here designed from 1Hz to 10kHz. Thanks to this advantage, the high frequency impedance of FC which is associated with the pseudo-inductance part due to all connections of the complete FC stack [4-19] is possible to be detected.

4.3.2. The verification of perturbation signal injecting process

The required specifications are mandatory to be achieved both under nominal condition and disturbed condition. Naturally, nominal condition is tested firstly to verify the reliability of the control strategy.

Fig.4.6 presents the obtained simulation results of the proposed converter under nominal operating conditions. Clearly, both load and no-load tests are realized. Due to the high robust characteristics of SMC, the proposed DC/DC converter operates at steady state. DC bus voltage is stabilized at 350V. DC components of inductor current are totally maintained at the identical value. AC components are successfully regulated in a small range. Meanwhile, FC current and voltage are likewise well

controlled within the linearity range. Especially, due to the interleaved structure of the converter and the use of coupled inductor, current ripple of FC stack is rather small, which is effective for the purpose of extending the FC lifespan.

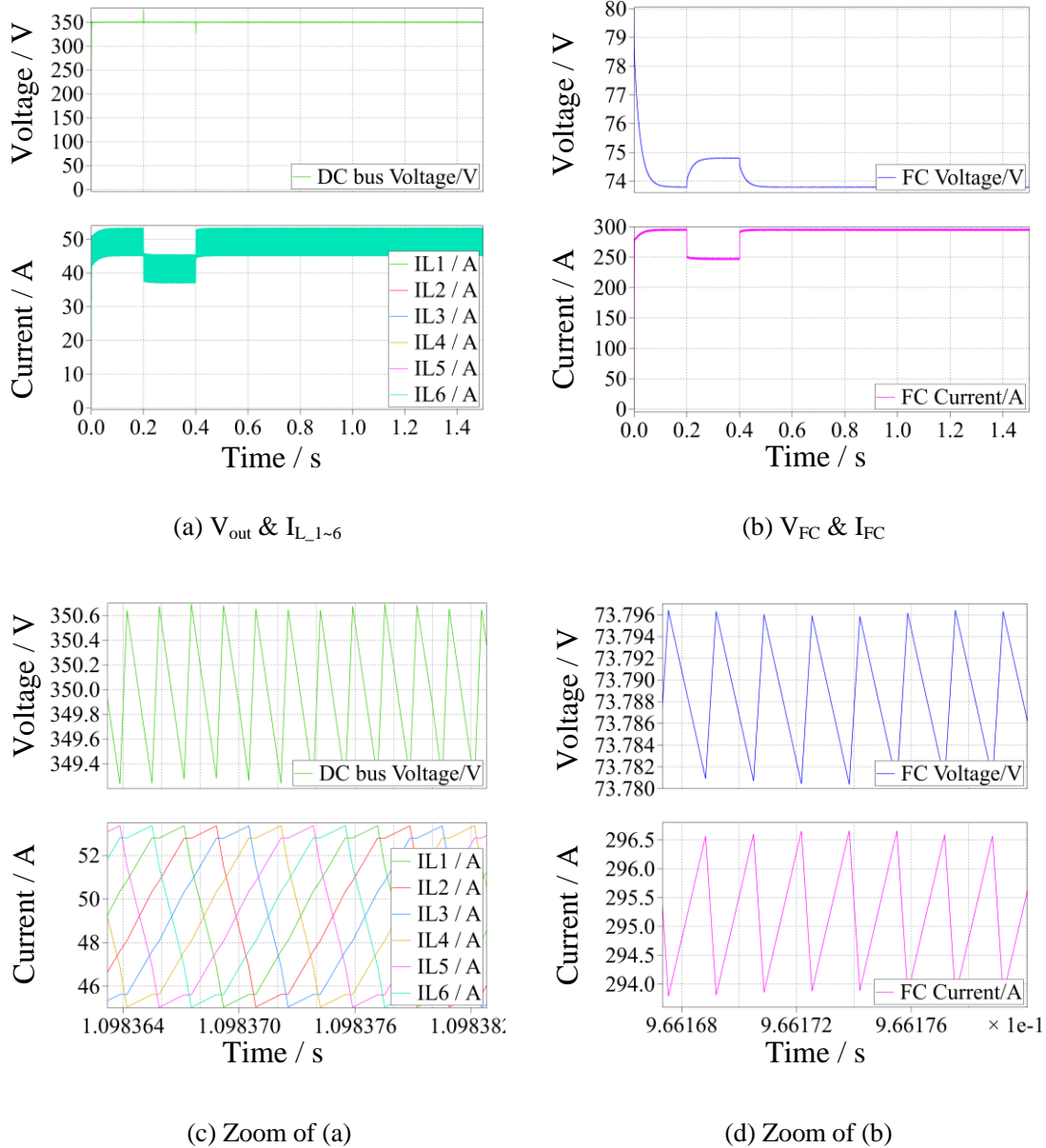


Fig.4.6 Nominal condition, without perturbation.

Hereby, in purpose of verifying the proposed detection strategy, perturbations possessing different frequencies are separately presented by Fig.4.7, Fig.4.8 and Fig.4.9. Some important information of these figures is summarized in Table.4.1.

Table.4.1 Comparison of IC-IBC's performances with different perturbation signals

		Fig.4.6	Fig.4.7	Fig.4.8	Fig.4.9
Perturbation frequency		Normal condition	10kHz	1kHz	1Hz
I_L	I_{L_ave}	49.2A	49.2A	49.2A	49.18A
	Δi_L	8.3249A	8.7A	10.2151A	8.6702A
	Ratio	16.9%	17.7%	20.7%	17.63%
V_{out}	V_{out_ave}	350V	349.9V	350.0V	349.9V
	ΔV_{out}	1.458V	2.97V	8.905V	2.54V
	Ratio	0.42%	0.85%	2.54%	0.73%
V_{FC}	V_{FC_ave}	73.8V	73.8V	73.8V	73.79V
	ΔV_{FC}	0.0163V	0.0322V	0.0906V	0.593V
	Ratio	0.022%	0.043%	0.12%	0.81%
I_{FC}	I_{FC_ave}	295.2A	295.2A	295.3A	295.1A
	Δi_{FC}	2.876A	5.783A	16.232A	4.948A
	Ratio	0.97%	1.96%	5.50%	1.68%

According to Fig.4.7~Fig.4.9, the perturbations have been successfully injected in the FC currents and the sinusoidal responses have also been introduced to the FC voltages. To be emphasized, close loop control has been achieved even during the process of perturbation injection. The average values of inductor current (I_L), the DC bus voltage (V_{out}), the FC voltage (V_{FC}) and FC current (I_{FC}) are all well regulated under both steady state and dynamic state. In Table.4.1, only the steady state information under the nominal power is presented. Each parameter's average value, ripple and ripple ratio are summarized. Regarding to the inductor current of each condition, it has been well controlled around the reference. The inductor current ripple is also kept below 20% even the perturbation is superimposed. Although perturbation has been injected to the system, the current ripples on the FC stack are still kept at low level (<10%). The effect of current ripple on the FC stack lifespan will thus be very limited.

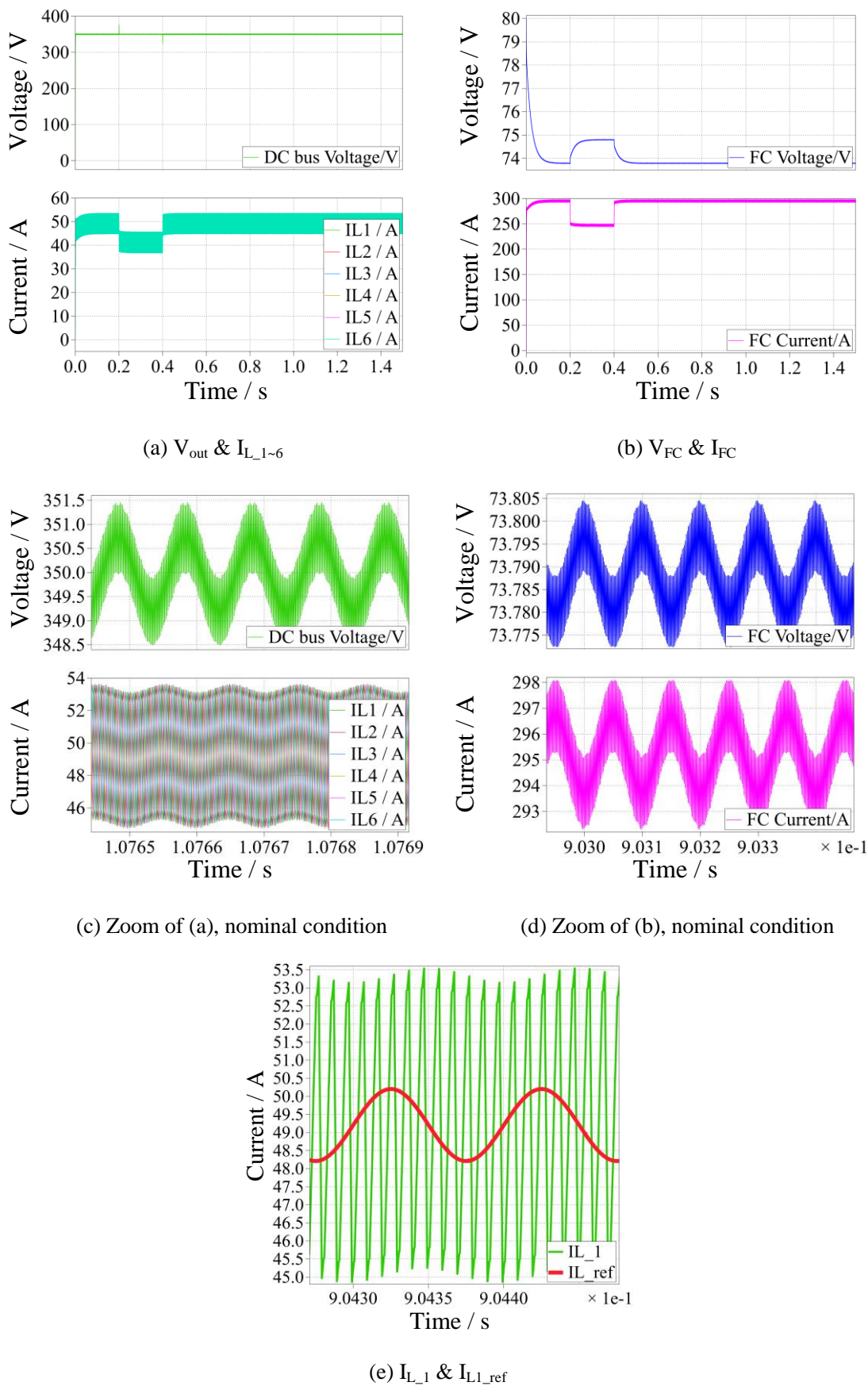
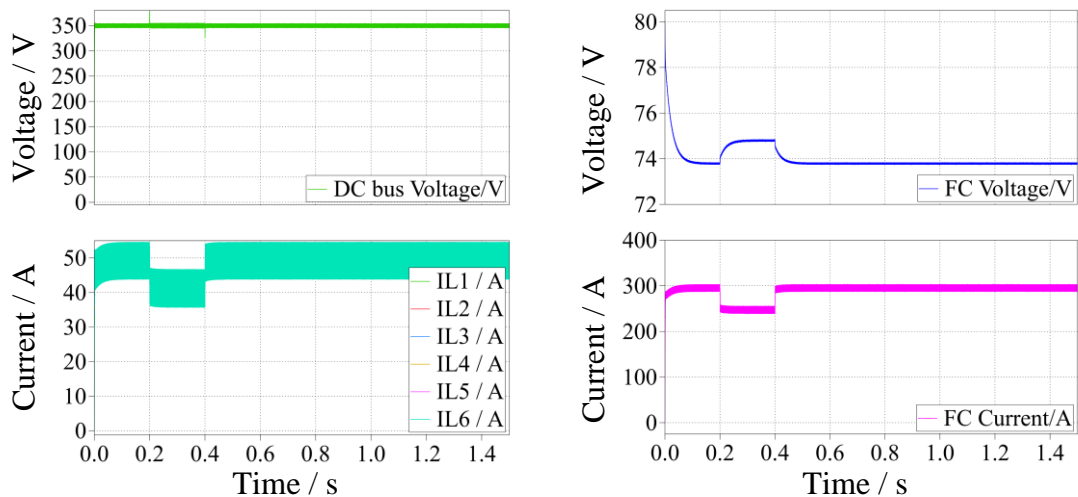
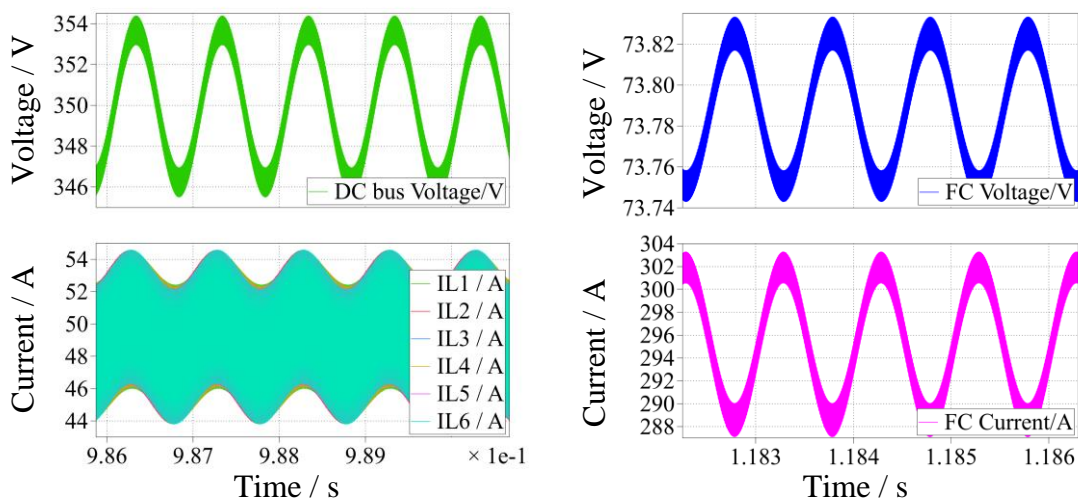


Fig.4.7 Perturbation of 10 kHz condition, sinusoidal signal.



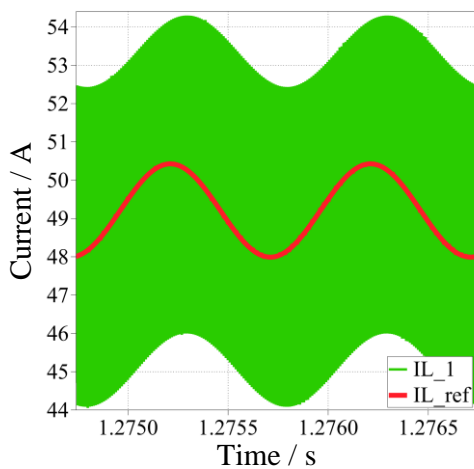
(a) V_{out} & I_{L1-6}

(b) V_{FC} & I_{FC}



(c) Zoom of (a), nominal condition

(d) Zoom of (b), nominal condition



(e) I_{L1} & I_{L1_ref}

Fig.4.8 Perturbation of 1kHz, sinusoidal signal.

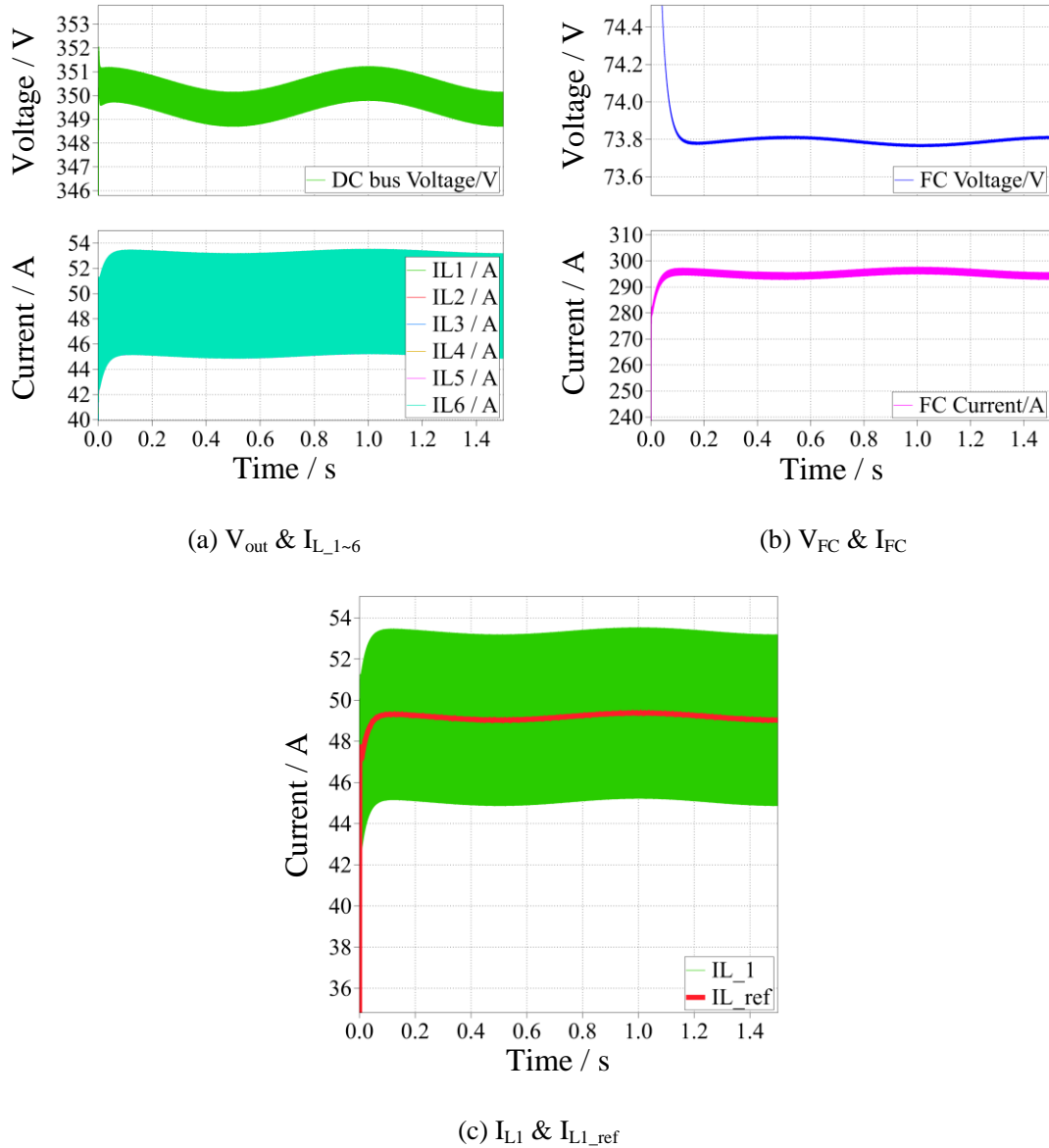


Fig.4.9 Perturbation of 1Hz, sinusoidal signal.

As analyzed previously, when an AC signal of known amplitude and frequency is sent to the inductor current reference of the proposed DC/DC converter, the amplitude responses of the FC stack's voltage and current can be recorded separately. This process can be repeated at different frequencies, thus, a Nyquist impedance spectrum can be formed by a series of stack impedances at discrete frequency points to get useful information regarding the FC stack state-of-health.

4.3.3. The verification of EIS achievement

Under nominal condition, Nyquist plot is obtained as presented by Fig.4.10 (the blue curve). Due to the characteristics of Randles model, only one arc can here be

exhibited in the Nyquist plot. Hence, three feature points, R_m , R_c and ϕ , which reflect the operating condition of FC stack, have been illustrated as follow [4-10].

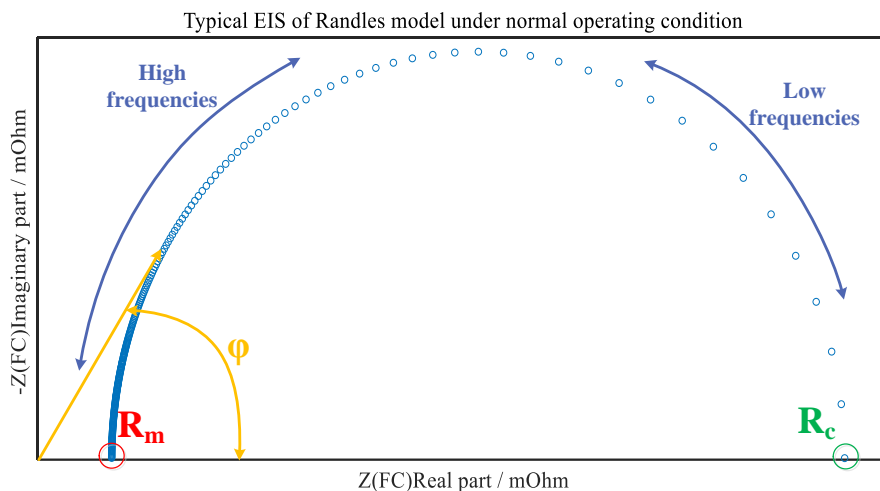
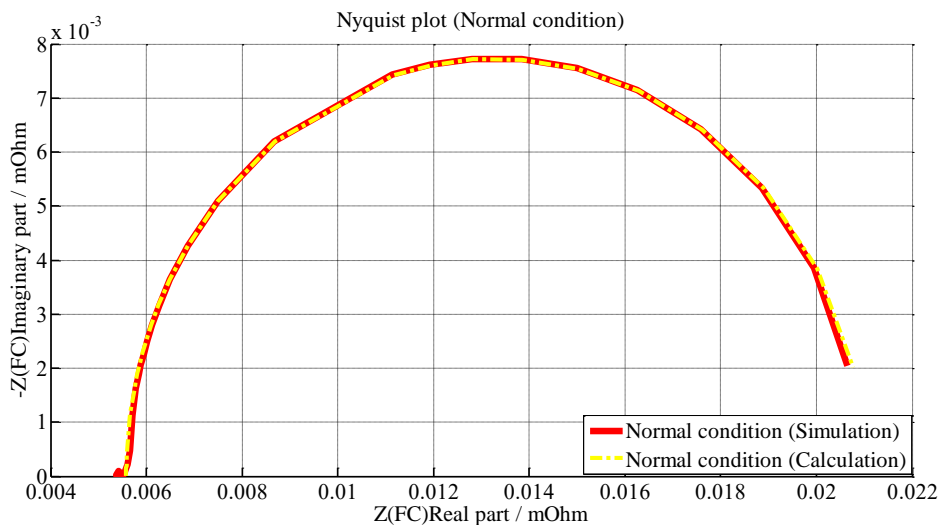


Fig.4.10 Typical EIS of Randles model of PEMFC

R_m , which is the left intercept of the curve and real axis, indicates the total Ohmic resistances of FC stack. The humidification degree of the membrane can especially be reflected by the parameter.

R_c , which can be achieved when the perturbation frequency approaches zero and it is actually the low frequency intercept of the impedance arc. This value provides also an idea about the polarization resistance of the FC stack.

ϕ , which corresponds to the maximal phase in the Phase plot and indicates the size of low frequency diffusion arc. A bigger ϕ represents a large arc diameter and reflects a difficult mass transport process.



(a) Normal operating condition

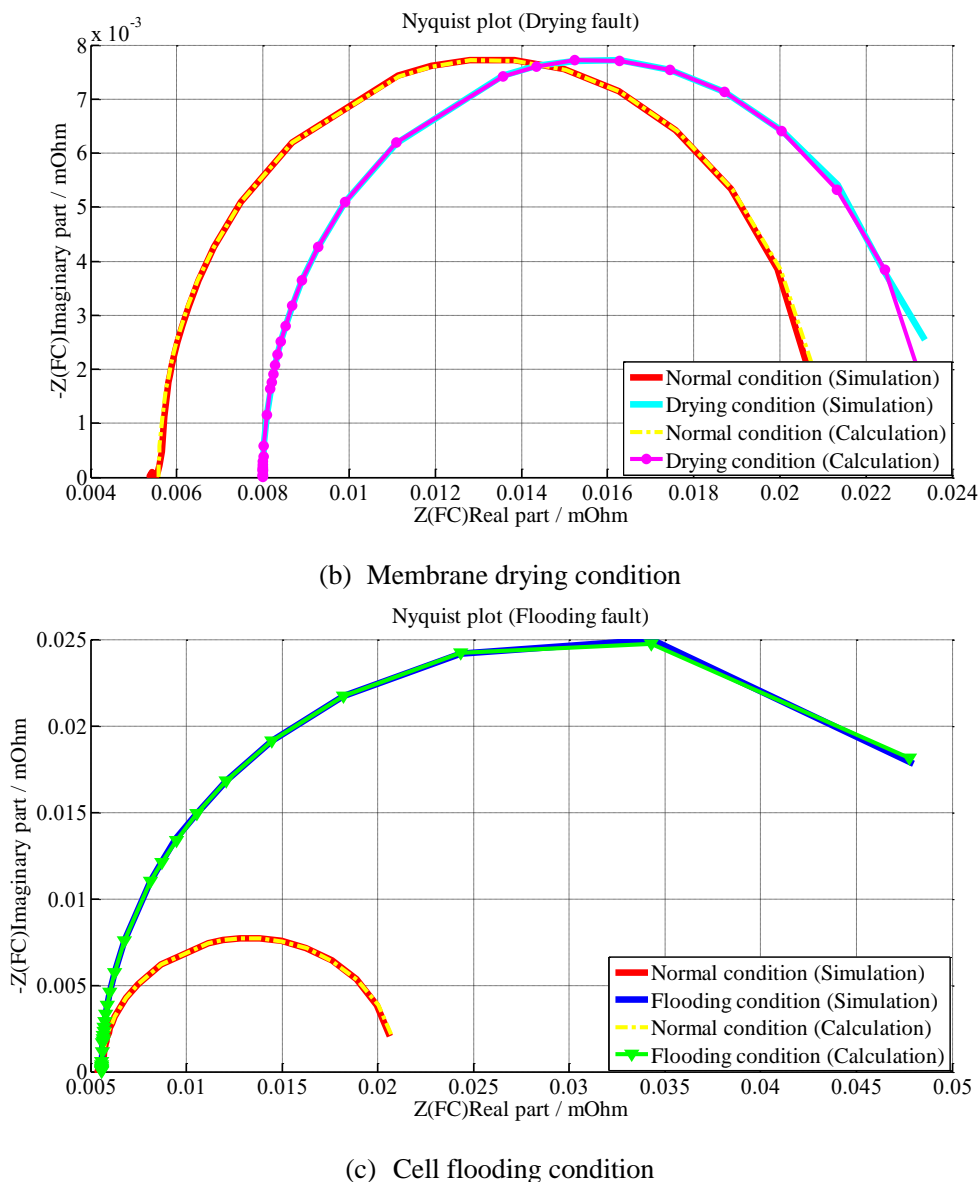


Fig.4.11 Electrochemical Impedance Spectrums of PEMFC under normal operating condition, drying faults and flooding faults are separately by (a), (b) and (c).

In Fig.4.11.(a), the other curve constructed by yellow points represent theoretical calculations of impedance spectrum in nominal operating conditions. The simulation results fit well with the calculation results. The proposed strategy is verified under nominal operating conditions based on Randles model.

In order to verify the proposed detection method, some parameters of the simplified FC stack model are modified to simulate different faults. Efficient water management inside the FC stack is essential to avoid breakdown or damages. Different types of fault (flooding or drying) can be indicated by different impedance spectrums as a result of variations of FC model parameters [4-20]. Therefore,

according to the obtained variations introduced to impedance curves when these faults are brought into existence, EIS is an effective diagnosis tool for these situations. Table.4.2 presents different FC parameters considered for different operating states. These parameters are man-set values and just considered in purpose of verifying the validity of the proposed diagnostic strategy.

Table.4.2 EMFC parameters for the assumption of different man-set faults to verify proposed EIS detection functionality

State of Health (SOH)	$R_m/m\Omega$	$R_c/m\Omega$	C_{dl}/F
Normal	5.58	15.46	1.37
Drying	8	15.46	1.37
Flooding	5.58	50	1.37

1) Simulating membrane drying (R_m increased)

Drying can be caused if the membrane is not sufficiently hydrated, or the inlet gases are insufficiently humidified. The inlet gases' temperature is below the FC operating one can be another reason. Drying out can lead to an increase of membrane resistance. Hence, this fault can be detectable by any increase of cell resistance [4-21].

R_m is replaced by a bigger value to simulate drying fault occurring to the FC stack. Both theoretical analyses and simulation results are presented in Fig.4.11.(b). Distinctly, the impedance spectrums achieved by simulation are visibly different from nominal condition. In Nyquist plot, the left intersection of the curve and real axis moves to the right of positive axis which indicates the increase of R_m , or the occurring of drying fault. The waveform doesn't change nevertheless, only a translation of the curve is obtained.

2) Simulating cell flooding (R_c increased)

Flooding, which is one of the most recurrent PEMFC's faults, is defined as an accumulation of liquid water in the gas channels or electrodes, impeding the access of reactive gases to the active layers, and therefore decreasing the reaction rate [4-22].

The flooding probability increases the difficulty of mass transport process. The lower the O_2 diffusion rate is, the more severe the flooding will be. Difficult mass transport leads to an arc owing a bigger diameter in Nyquist plot.

R_c is replaced by a bigger value to emulate flooding fault occurring in the FC stack. Both theoretical analyses and simulation results are presented in Fig.4.11.(c). Obviously, the impedance spectrums obtained by simulation are visibly different from nominal condition. In Nyquist plot, due to the untouched membrane resistance, the left intersections of the curves and real axis are the same. An arc combined with a bigger diameter is achieved by the flooding conditions.

Hence, according to the comparison analyses between theoretical and simulated results, the proposed strategy, which focuses on integration of EIS functionality with sliding-mode control on the considered DC/DC power converter, is effective to be applied for monitoring the state of health of a FC stack. Both drying and flooding modes are detectable from the achieved impedance spectrums. On-line diagnosis of the FC stack is realized; meanwhile DC bus voltage is well regulated even during detection procedure. To be emphasized, the proposed on-line diagnosis approach is accomplished without any additional equipment which is highly attractive for practical FCEV applications due to the limited space inside a vehicle.

4.4. Conclusion

In this chapter, on-line detection of EIS for PEMFC application based on 6-phase IBC with coupled inductors is verified by calculation and simulation. The 6-phase IBC is based on SiC semiconductors and inverse coupled inductors. A 21kW FC stack is selected as the power source. Compared with the existing studies, the selection of IBC is meaningful for the reduction of the FC current ripple and the extension of the FC lifespan. Thanks to the selection of SiC semiconductors and coupled inductor technique, the total volume and weight of the power converter have been reduced significantly. Besides, SMC has been selected to satisfy the constrained requirements of current control for coupled inductor. Furthermore, EIS implementation (without any additional devices) has been realized and verified by a simple model Randles of a FC stack in a wide range of frequencies. DC bus voltage has been well-controlled either under nominal operating conditions or disturbed conditions. Benefiting from the proposed strategy, additional equipment is not required which is meaningful due to the limitation of inner space in a FCEV and much compactness can be achieved.

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Chapter 5: Hardware in the Loop real-time validation

5.1. Introduction

During these last years, Hardware-In-Loop (HIL) real time rapid prototyping has been an advanced research topic in many engineering fields such as power electronics and AC drive applications. Most of the developed simulators are applied in the context of Hardware-In-Loop (HIL) testing of digital controllers in order to validate them in many operating conditions, which would not be easily possible using only experimental tests.

The main issue of this chapter is to define how to develop HIL real time validation able to accurately reproduce our system dynamics and transients. High performance digital simulation platforms are now commercialized, covering a wide range of system complexities and operating at very short simulation time-steps. They integrate powerful and scalable multi-core processor boards combined with Field Programmable Gate Array (FPGA) boards. In fact, these FPGA platforms are deployed to address the demand of very fast system dynamics, thus very short simulation time-steps.

The 6-phase IBC based on inverse coupled inductors has been verified by HIL simulation in real time. The system MicroLabBox from dSPACE has been used as the platform [5-1]. According to this process, not only the proposed topology but also the control strategy can both be validated based on high switching frequency before experimental tests on a small-scale test bench.

This chapter is organized as follow. In section 5.2, the platform and corresponding softwares used in this study for HIL are presented. In section 5.3, the modeling process of the converter and the realization of the control strategy are explained. The off-line simulation results and HIL real time validation results are compared respectively. This chapter will be concluded in section 5.4.

5.2. MicroLabBox and required softwares

MicroLabBox, which is proposed by dSPACE GmbH, has been selected as the HIL platform to verify the control strategies of the 6-phase IBC with inverse coupled inductors. In this section, MicroLabBox and the required softwares are briefly introduced.

5.2.1. MicroLabBox

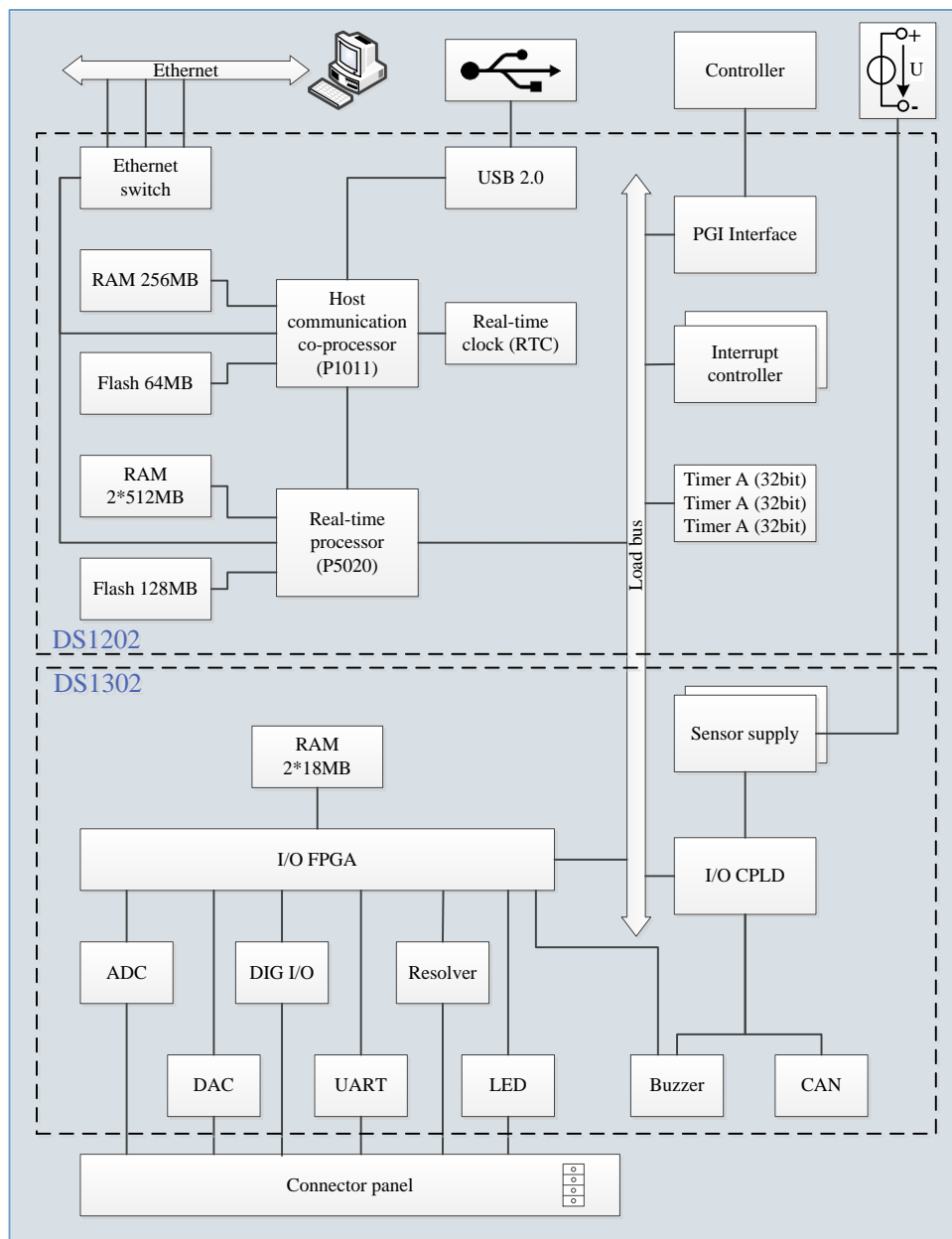


Fig.5.1 MicroLabBox block diagram [5-1]

As presented in Fig.5.1, MicroLabBox is a compact all-in-one development system for the laboratory purpose that combines compact size and cost-effectiveness with high performance and versatility [5-1]. Dual-core real-time processor at 2GHz and one user-programmable FPGA are integrated inside. More than 100 I/O channels of different types make MicroLabBox a versatile system that can be used in mechatronic research and development areas, such as robotics, medical engineering, electric drives control, renewable energy, vehicle engineering, or aerospace. Typical technical details of MicroLabBox are given in Table.5.1.

Table.5.1 Technical details of MicroLabBox[5-1]

Parameter		Specification
Processor	Real-time processor	NXP (Freescale) QorIQ P5020, dual-core, 2GHz
	Host communication co-processor	NXP (Freescale) QorIQ P1011 800MHz for communication with host PC
Memory		1GB DRAM; 128MB flash memory.
Programmable FPGA		Xilinx Kintex-7 XC7K325T FPGA
Analog input	Resolution and type	<ul style="list-style-type: none"> ● 8 14-bit channels, 10 Msps, differential; ● 24 16-bit channels, 1 Msps, differential.
	Input voltage range	-10 ... 10 V
Analog output	Resolution and type	16 16-bit channels, 1 Msps, settling time: 1 μ s
	Output voltage range	-10 ... 10 V
	Output current	\pm 8 mA
Digital I/O		<ul style="list-style-type: none"> ● 48 bidirectional channels, 2.5/3.3/5 V (single-ended); functionality: bit I/O, PWM generation and measurement, etc. ● 12 bidirectional channels (RS422/485 type) to connect sensors with differential interfaces.

In reality, the time and cost of project development are needed to be reduced. MicroLabBox is a great choice for the design and optimization of control systems for power electronics application. The typical illustration of MicroLabBox-based system in this study is presented in Fig.5.2.

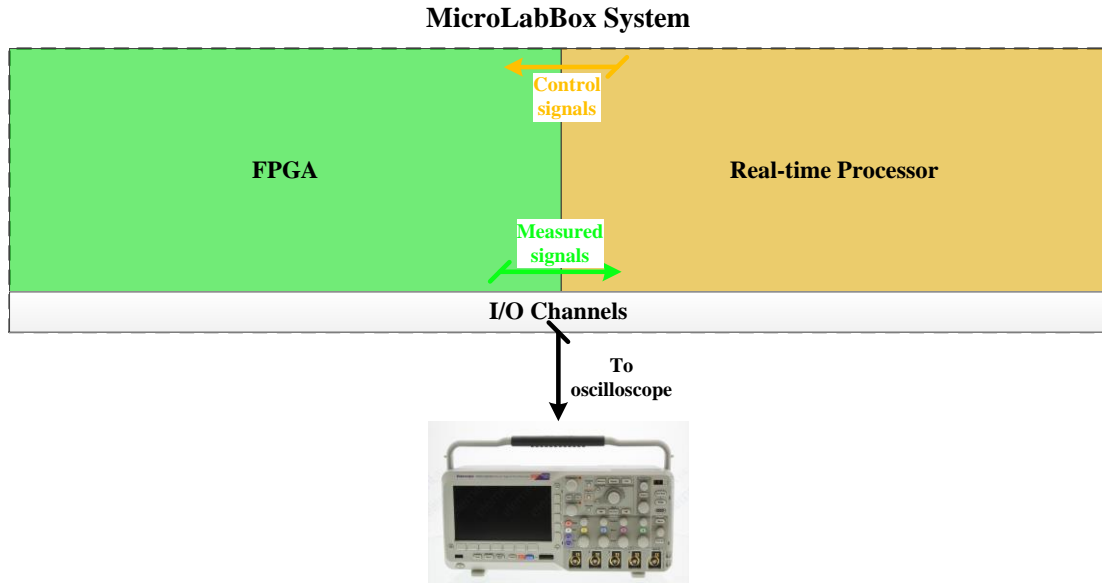


Fig.5.2 Illustration of the system structure based on MicroLabBox

The developed control strategy is based on Real-Time Interface (RTI) block-set to Simulink, and downloaded to MicroLabBox. Then, the measured signals are sent to I/O channels of MicroLabBox by various sensors. After the calculation process of developed control strategy, corresponding control signals will be sent out to the target device (here is a DC/DC converter for example). The control can be monitored and optimized in real-time in ControlDesk software.

The composition and connections of MicroLabBox are illustrated in Fig.5.3. The transmission of data sets among the host PC, external device, and MicroLabBox during real-time application can be well understood.

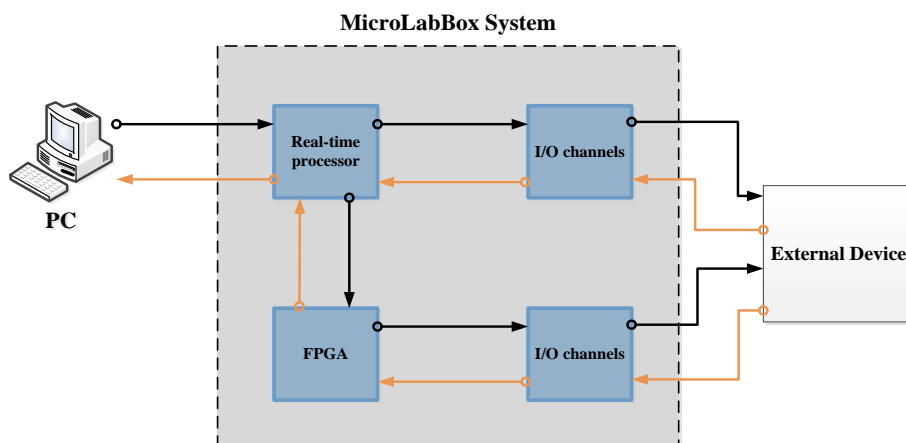


Fig.5.3 Components of MicroLabBox and their connections

The host PC can load programs of the processor and FPGA for real-time

experiments. The real-time processor not only executes the processor application but also initiates sending and receiving data to/from the FPGA via a board-specific bus. External devices such as an electric control unit can be connected to MicroLabBox. The real-time processor and FPGA can also be connected to their own I/O channels to provide I/O functionality independently.

5.2.2. Real-Time Interface to Simulink

The Real-Time Interface (RTI) Programming Blockset is a Simulink blockset that allows programming a FPGA in a dSPACE system. Benefiting from the modular design, the programming process is simplified. The overview of RTI FPGA programming blockset is shown in Fig.5.4 [5-2].

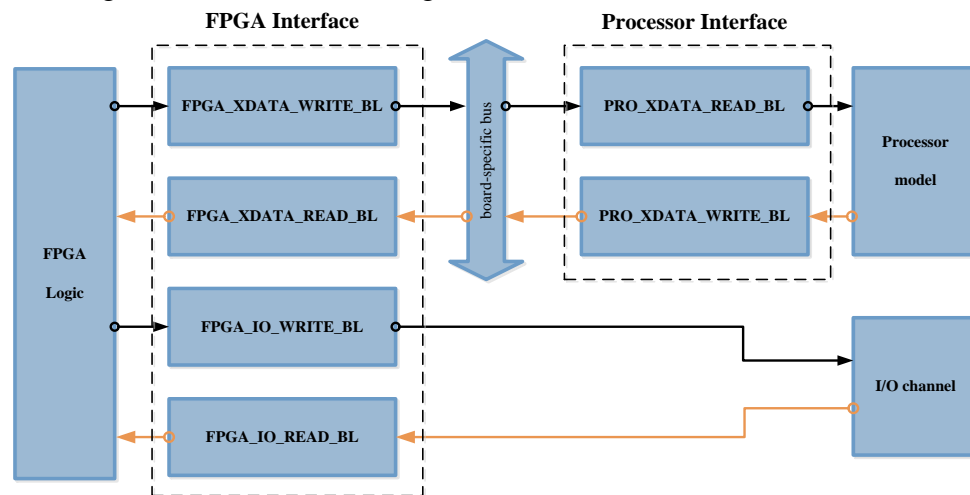


Fig.5.4 Overview of RTI FPGA programming blockset

To be able to exchange data, the FPGA and processor interfaces provide different data storages: register, register group, and buffer. Only the processor application can initiate data exchange between the real-time processor and the FPGA. The FPGA executes its operations in parallel because the FPGA application is a logic implementation which obtains a much faster execution time than the real-time processor. The FPGA is able to operate (read and write) several processor tasks with different task periods at different points in time. These read and write requests are executed by the FPGA in parallel.

5.2.3. Xilinx System Generator

The embedded FPGA inside MicroLabBox is the production of Xilinx Kintex-7 series. RTI programming blockset is required to co-operate with two special

development tools from Xilinx: Xilinx Vivado and Xilinx System Generator (XSG) [5-3]. As XSG is mainly used as the compiler and configuration tool of FPGA, it is mainly focused here.

XSG is a system-level modeling tool that facilitates FPGA hardware design. It allows device-specific hardware designs to be constructed directly in a flexible high-level system modeling environment. In a XSG design, signals are not just bits. They can be signed and unsigned fixed-point numbers, and changes to the design automatically translate into appropriate changes in signal typed. Blocks are not just stand-ins for hardware. They respond to their surroundings, automatically adjusting the results they produce and the hardware they become.

Most Xilinx blocks are polymorphic, i.e., they are able to deduce appropriate output types based on their input types. This characteristic allows the designer to set the output type for a block and to specify how quantization and overflow should be handled. Therefore, Xilinx System Generator tool provides more flexibility to the designer.

5.3.HIL real time validation

As studied in previous chapters, the 6-phase interleaved boost converter based on inverse coupled inductors (IC-IBC) has been compared with 6-phase interleaved boost converter (UC-IBC) and the conventional boost converter (BC). The simulation results based on PLECS have been presented and analyzed. In this section, to verify and analyze the proposed topology in real time and to reproduce the dynamic response, HIL real time validation analysis based on MicroLabBox will be addressed. The modeling process of each part will be detailed; both off-line simulation results and HIL real time validation results of these three topologies will be carried out.

5.3.1.PEMFC modeling process

As the main power source of FCEV, the fuel cell stack directly converts chemical energy to electrical energy. Electrochemical reactions happen at the surface of the catalyst at the interface between the electrolyte and the membrane. The fuel cell stack voltage can be obtained as a function of stack current, cathode pressure, reactant partial pressures, fuel cell temperature, and membrane humidity using a combination of physical and empirical relationships [5-4]. Here, the electrochemical model has been built depending on the manual of selected PEMFC, a 21kW PEM

FCvelocity[®]-9SSL module from Ballard[®] Company [5-5]. As the inherent characteristics of this specific PEMFC module, the output FC current is high (300A) while the FC voltage is comparatively low (70V). The fuel cell stack specifications are presented in Table.5.2.

Table.5.2 PEMFC specifications of Ballard[®] FCvelocity[®]-9SSL

Parameter	Symbol	Value	Unit
Rated Power (beginning of life)	P _N	21.0	kW
Rated Current	I _{FC_N}	300	Amps
Voltage	V _{FC_N}	70.2	volts
Number of Cells	N _{cell}	110	--
Fuel Pressure	p _{H2}	1.2	bar(g)
Oxidant Pressure	p _{O2}	1.0	bar(g)
Ambient Temperature (operating)	T _{amb}	-25~+75	°C

The cell terminal voltage (v_{cell}) and the fuel cell stack voltage (v_{FC}) are presented in (5.3.1), separately. E is called the reversible open circuit voltage or “Nernst” voltage of a hydrogen fuel cell; v_{act} is called the cell activation loss or activation overvoltage; v_{ohm} is called the cell ohmic loss and v_{cons} is called the cell concentration loss of concentration overvoltage. N_{cell} stands for the number of fuel cells [5-6].

$$\begin{cases} v_{cell} = E - v_{act} - v_{ohm} - v_{cons} \\ v_{FC} = v_{cell} \times N_{cell} \end{cases} \quad (5.3.1)$$

The cell Nernst voltage E can be obtained by (5.3.2) in which T_{fc} stands for the temperature of the fuel cell; T_0 stands for the standard-state temperature. T_{fc} and T_0 are expressed in Kelvin. The partial pressure p_{H2} and p_{O2} of hydrogen and oxygen, respectively, are expressed in bars.

$$E = 1.229 - 0.85 \times 10^{-3} \times (T_{fc} - T_0) + 4.3085 \times 10^{-5} \times T_{fc} \times \left[\ln(p_{H_2}) + \frac{1}{2} \cdot \ln(p_{O_2}) \right] \quad (5.3.2)$$

The cell activation loss can be obtained by (5.3.3). v_0 is the voltage drop at zero current density; i_{fc} is defined as the cell current density, and v_a and c_1 are constants [5-4].

$$v_{act} = v_0 + v_a \times \left(1 - e^{-c_1 \times i_{fc}} \right) \quad (5.3.3)$$

The cell ohmic loss can be obtained by (5.3.4). Rohm is the internal electrical

resistance which depends strongly on the membrane humidity and the cell temperature. t_m is the thickness of the membrane and σ_m is the membrane conductivity [5-4].

$$\begin{cases} v_{ohm} = i_{fc} \times R_{ohm} \\ R_{ohm} = t_m / \sigma_m \end{cases} \quad (5.3.4)$$

The concentration loss can be obtained by (5.3.5). The constants c_2 and c_3 , which depend on the temperature and the reactant partial pressure, can be determined empirically. The parameter i_{max} is the current density that causes precipitous voltage drop [5-6].

$$v_{conc} = i_{fc} \times \left(c_2 \times \frac{i_{fc}}{i_{max}} \right)^{c_3} \quad (5.3.5)$$

Hence, according to the fuel cell stack specifications and the modeling process of stack voltage, the polarization curve has been obtained as Fig.5.5.

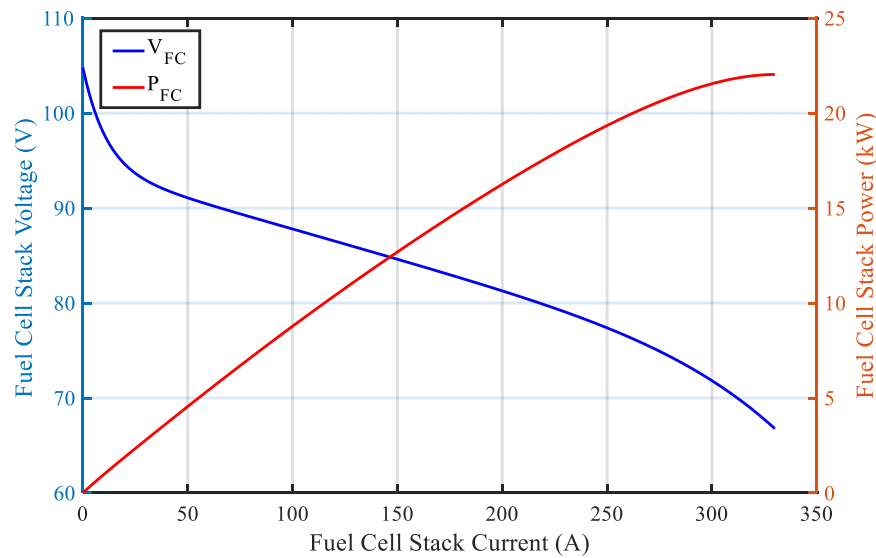


Fig.5.5 Ballard® FCvelocity®-9SSL polarization curve

5.3.2. Modeling of the converter

The DC/DC converters based on high switching frequency are implemented in FPGA. The average converter model is used aiming to verify the control strategy.

5.3.2.1. PWM signal generation

In this part, the PWM technique is used to control the turn-on and turn-off of

power switch of DC/DC converter.

According to construction of the proposed DC/DC boost converter, there are six parallel phases in this topology. Each phase requests its own PWM drive signal and due to the interleaved control strategy, a fixed phase shift exists between each phase control order as studied previously. In our case, high switching frequency (100kHz) has been chosen. Hence, the PWM generators can only be built inside the embedded FPGA of MicroLabBox.

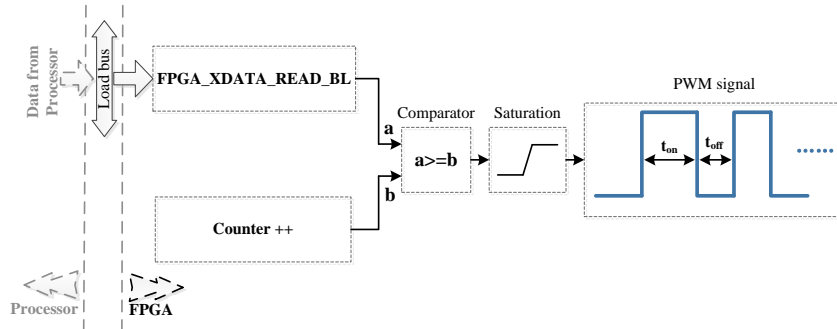


Fig.5.6 PWM signal generation based on FPGA of MicroLabBox

Fig.5.6 presents the PWM signal generation's process based on the embedded FPGA of MicroLabBox. The data sets of modulated wave are sent by the real-time processor through load bus, and received by the blockset "FPGA_XDATA_READ_BL". The carrier wave is generated by the blockset "Counter ++". These two waves will be compared by a comparator and then generate the PWM signal. Here, the generation procedure of carrier wave based on "Counter ++" blockset is explained. Two counter types can be selected: free running and count limited. The free running type means no upper limit and in contrast, when the count limited type is selected, the counter will recount from the given initial value once the upper limit value is reached. The count step and the explicit period can both be configured. The count step must be a positive integer and the explicit period mustn't be smaller than the clock period of FPGA.

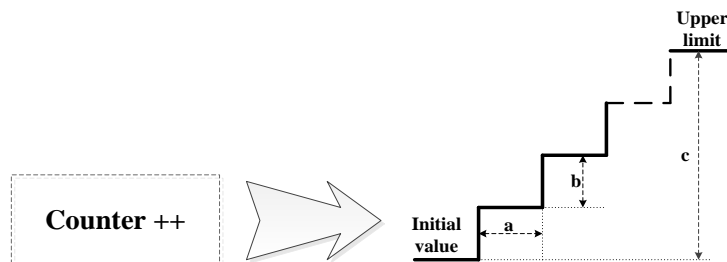


Fig.5.7 Illustration of Counter ++ modular

In Fig.5.7, “a” stands for the step size which must be a positive integer, “b” stands for the explicit sample period which can be user defined and its minimum value equals the clock period, and “c” stands for the difference between the upper limit and initial value. The counting accuracy and rate are determined by these parameters. The count period is given as (5.3.6) in unit of second. Therefore, the switching period equals to the count period $T_{counter++}$. For example, to obtain a carrier wave combined with frequency of 100kHz, the step size “a” can be set as one, the sample period “b” can be selected as 10ns and the upper limitation is 999. Here, the initial value equals zero and $T_{counter++}$ can be obtained as 10 μ s. Therefore, the requested carrier wave is obtained.

$$T_{counter++} = (c+1) \times b \times a \quad (5.3.6)$$

5.3.2.2. Output voltage modeling process

The output voltage model consists of two components: the output voltage state equation and the integrator. As analyzed in Chapter.3, the state-space equations of each converter have been given. Then, the change rate of V_{out} with respect to time can be obtained as (5.3.7).

$$\frac{dv_{out}}{dt} = \frac{1}{C} \times \left(\sum_{n=1}^N i_{L_n} \times (1-d_n) - \frac{v_{out}}{R_o} \right) \quad (5.3.7)$$

In this equation, “N” stands for the total number of phases (N equals “1” for Boost and “6” for UC-IBC and IC-IBC). Here, the right part of (5.3.7) is called Eq.(V_{out}). The integral of Eq.(V_{out}) is the output voltage as illustrated in Fig.5.8.

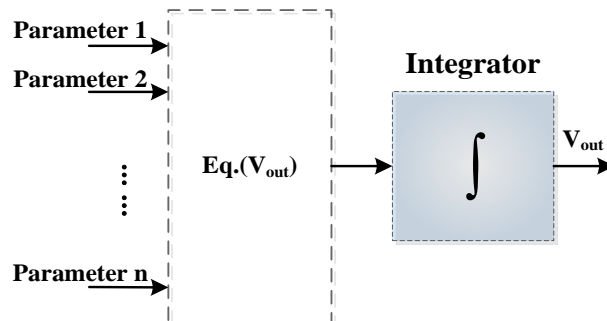
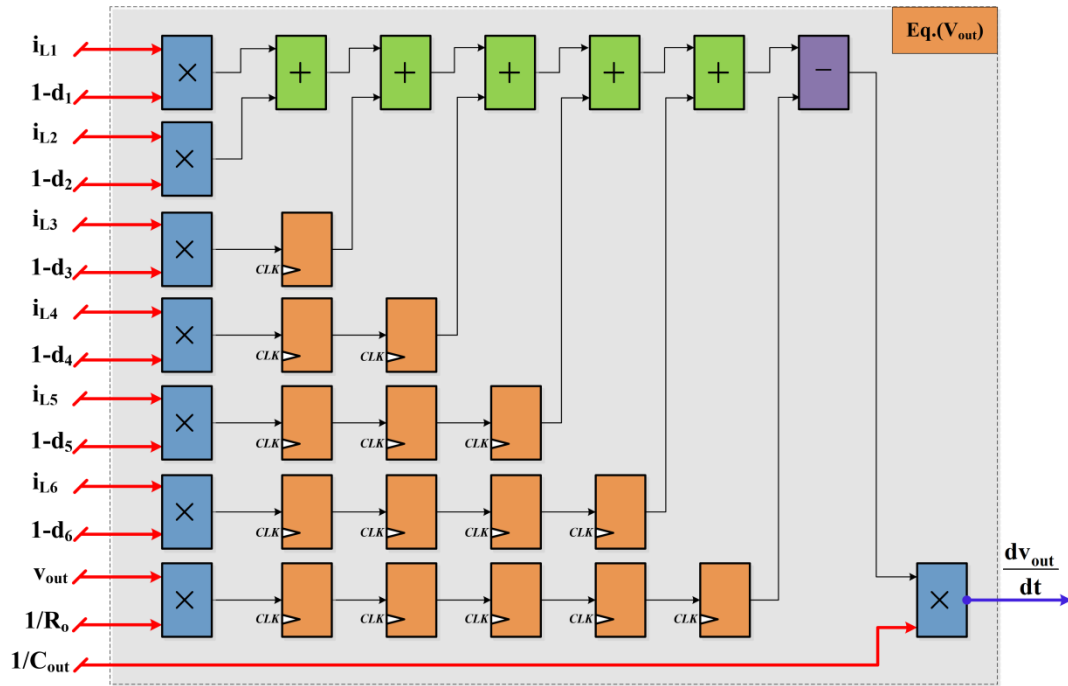


Fig.5.8 Diagram of output voltage model

Fig.5.9 Eq.(V_{out}) detail

The detail of Eq.(V_{out}), which was realized in FPGA, is illustrated as Fig.5.9. In this diagram, multiplier is represented as the blue rectangle, adder is represented as the green rectangle, subtracter is represented as the purple rectangle, and register is represented as the orange rectangle. The utilization of plenty registers focus on the realization of pipeline structure which can improve response frequency of the program [5-7]. Meanwhile, it is also the requirement of timing synchronization. The quantity of register is depending on the latency of operations and data length. The mathematical operations require more operating period than the logical operation. In Fig.5.9, the latency of multiply operation equals three clock periods. The latency of add operation is one clock periods. Regarding to Fig.5.9, $i_{L1}*(1-d_1)$, $i_{L2}*(1-d_2)$ and $i_{L3}*(1-d_3)$ are implemented at the same time in parallel. Then, the sum of $i_{L1}*(1-d_1)$ and $i_{L2}*(1-d_2)$ will be added to $i_{L3}*(1-d_3)$. As the add operation takes one clock period, one register is inserted to the loop of $i_{L3}*(1-d_3)$ to “wait for” the sum of $i_{L1}*(1-d_1)$ and $i_{L2}*(1-d_2)$.

In FPGA, a set of operations can be divided into several branches, and these branches operate in parallel. Each branch consists of different operators, mathematical or logical. As the execution duration (latency) of each operator is quite different and the computational complexity of each branch is not the same, there are great differences among the operational durations. Therefore, the optimization of timing

sequence is essential to avoid operational error. In simple terms, the branches which own short operational durations are requested to “wait” other long operational duration-based branches. So, registers can be used to realize this purpose. Although the overall delay may be increased when registers are inserted, the waiting time can be shortened significantly. The data utilization rate and the operational efficiency can thus be improved.

In the numerical system, the integral operation of functions is treated as the accumulative operation of functions. The diagram of integrator is detailed in Fig.5.10.

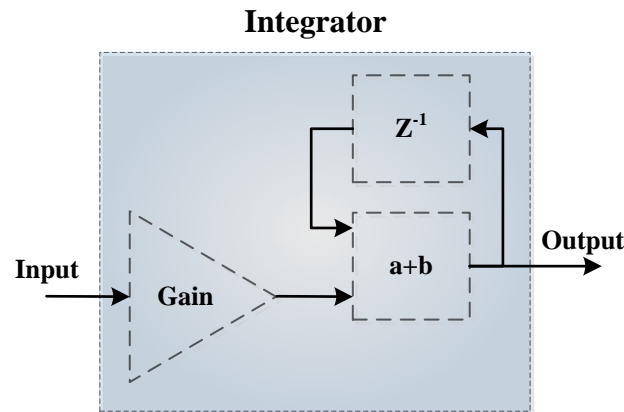


Fig.5.10 Integrator of FPGA

The modular “a+b” is the adder, the modular “Z⁻¹” is the register, and the modular “Gain” is the coefficient which can be treated as the integral time. In order to gain the accuracy and meet the error requirement, the “Gain” must be a very small value. The numerical integrator can be explained by (5.3.8).

$$Output_{(t+1)} = Gain \times Input_{(t+1)} + Output_{(t)} \quad (5.3.8)$$

5.3.2.3. Inductor current modeling process

The inductor current model also consists of two components: the inductor current state-equation and the integrator. The operating principle of integrator has been explained previously. The quantity of integrator is depending on the number of interleaved phases. Similarly, the change rate of inductor current with respect to time of BC and 6-phase UC-IBC is presented as following (5.3.9).

$$\frac{di_{L-n}}{dt} = \frac{1}{L} (v_{in} - R_L \times i_{L-n} - (1-d_n) \times v_{out}), n=1 \sim N \quad (5.3.9)$$

“N” stands for the number of phases which equals “1” for BC and “6” for 6-phase UC-IBC.

The change rate of I_L of 6-phase IC-IBC is given as following (5.3.10). The matrix $[L]$ is the inverse matrix of inductance matrix; “ M ” stands for the mutual inductance.

$$\frac{d}{dt}[i_{L_n}] = [L]^{-1} \times ([v_{in}] - [1-d_i] \times v_{out} - [i_{L_n}] \times R_L), n=1 \sim 6 \quad (5.3.10)$$

$$[L] = \begin{bmatrix} 2L & -M & 0 & 0 & 0 & -M \\ -M & 2L & -M & 0 & 0 & 0 \\ 0 & -M & 2L & -M & 0 & 0 \\ 0 & 0 & -M & 2L & -M & 0 \\ 0 & 0 & 0 & -M & 2L & -M \\ -M & 0 & 0 & 0 & -M & 2L \end{bmatrix}_{6 \times 6}$$

Here, the right parts of (5.3.9) and (5.3.10) are called Eq.(I_L). The integral of Eq.(I_L) is the inductor current as illustrated in Fig.5.11.

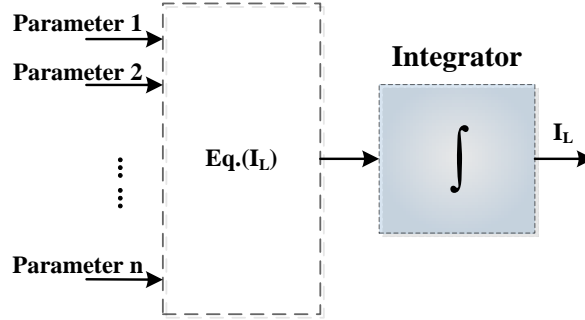


Fig.5.11 Diagram of inductor current model

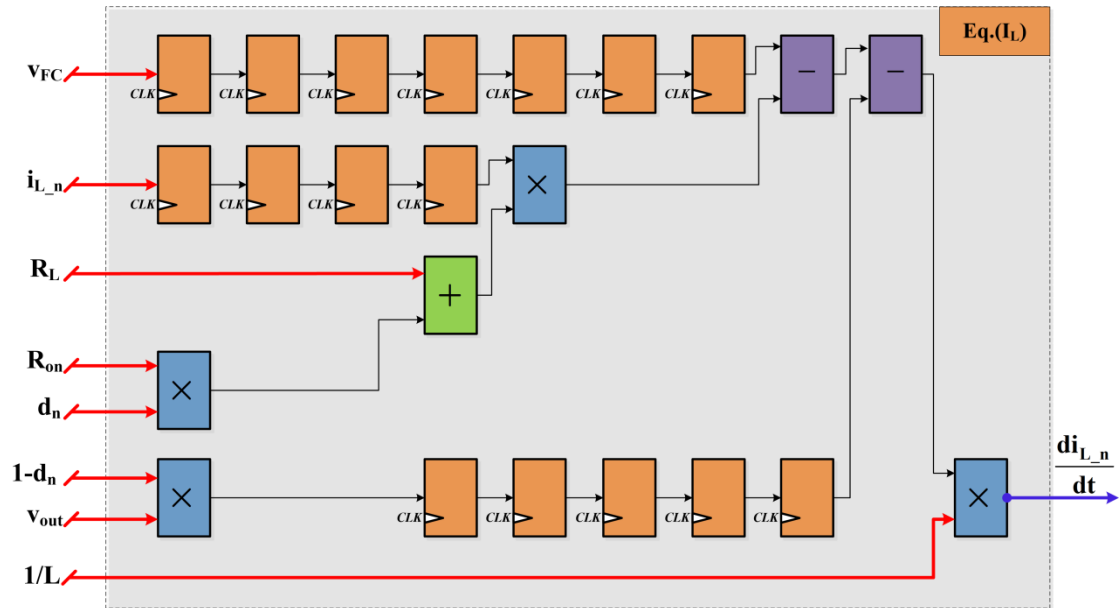
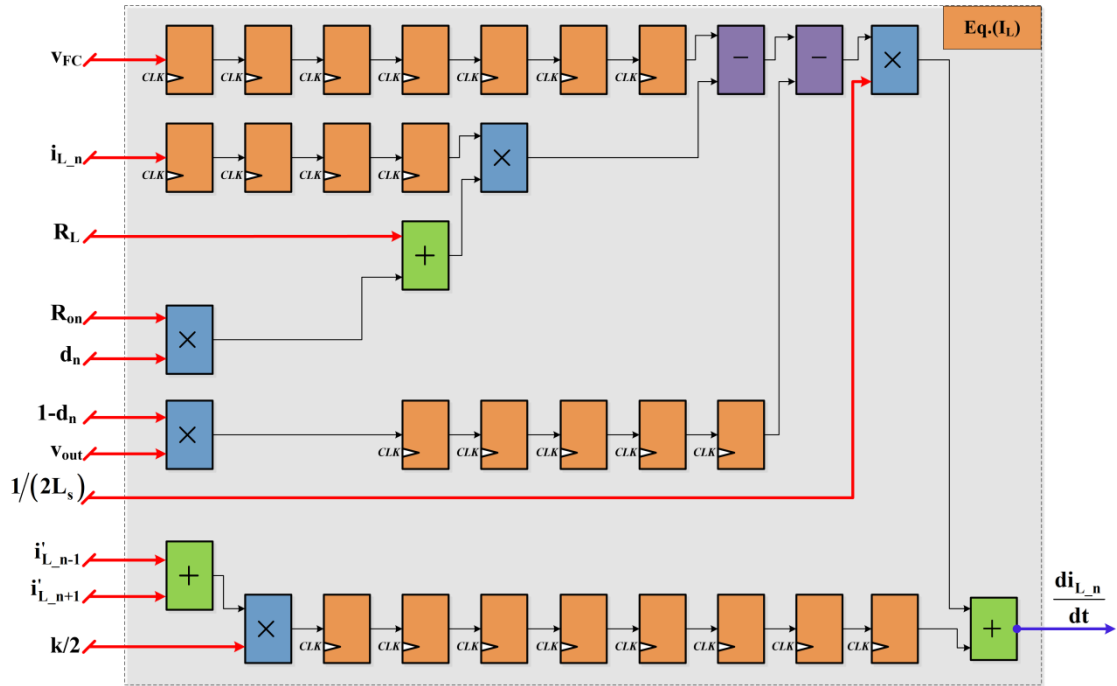


Fig.5.12 Eq.(I_L) detail BC and 6-phase UC-IBC

Fig.5.13 Eq.(I_L) detail the proposed 6-phase IC-IBC

The Eq.(I_L) of BC and 6-phase UC-IBC is illustrated in Fig.5.12. In this figure, “i_{L_n}” represents the inductor current of phase-n. For the BC, only one Eq.(I_L) exists. Depending on the topology’s structure, six Eq.(I_L) are constructed in interleaved structure for the 6-phase UC-IBC. Due to the existence of inverse coupled inductors, the Eq.(I_L) of the proposed 6-phase IC-IBC is more complicated than the other two as illustrated in Fig.5.13. The coupling coefficient (k), the self-inductance (L_s), and the change rate of neighbor phase’s current (i’_{L_{n-1}} and i’_{L_{n+1}}) are taken into consideration. Similarly, the pipeline structure has also been used for Eq.(I_L) of three topologies in order to increase data throughput and response frequency.

5.3.2.4. Controller modeling process

The controller of DC/DC boost converter is built in the real-time processor, and it consists of two loops: outer loop for DC bus voltage control and inner loop for inductor current control. The principle of each control loop is the same that apply PI correction to the difference between detected signal and corresponding reference in order to make the system reach the desired steady point rapidly. The output of outer loop is used as the reference of inner loop. For the multi-phase interleaved boost converter, there is a single output voltage controller and the number of inductor current controller is corresponding to the number of phases. The parameter calculation

process has been analyzed in Chapter.3. Fig.5.14 presents the diagram of dual-loop PI controller for DC/DC boost converters in this study.

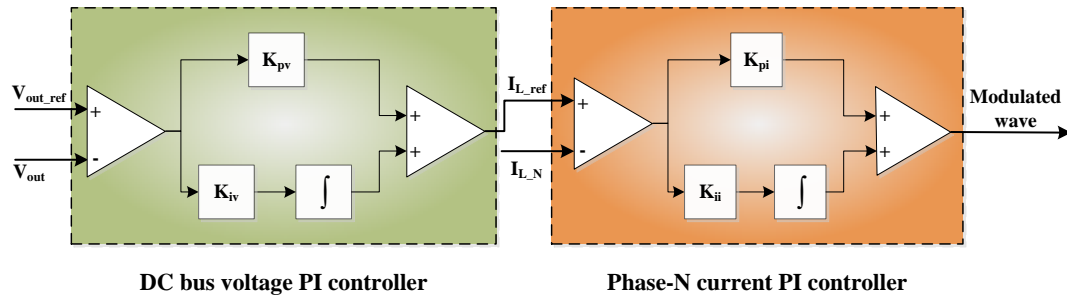


Fig.5.14 Diagram of controller

5.3.3.HIL verification

The real-time HIL validation, which consists of real time implementation of the real part into the FPGA and the control part in the microprocessor of the MicroLabBox has been proved as an efficient and powerful means to verify new topologies and their corresponding control strategies before the hardware implementation. In this study, real time HIL validation based on MicroLabBox and relevant softwares has been implemented. As illustrated before, the power source model and the controller are built in the real-time processor, and the converter model is implemented in FPGA. During the real-time HIL validation, the oscilloscope can be used to monitor the signals sent out by MicroLabBox through its I/O interfaces.

The diagram of MicroLabBox for real time HIL validation in our study is given in Fig.5.15. Obviously, the implementation has been divided into two parts as explained previously. These two parts realize data-sets transmission by the “Load bus” inside MicroLabBox. In this diagram, “N” stands for the number of phase of a boost converter. “Eq.(V_{out})” and “Eq.(I_L)” have been analyzed in detail previously.

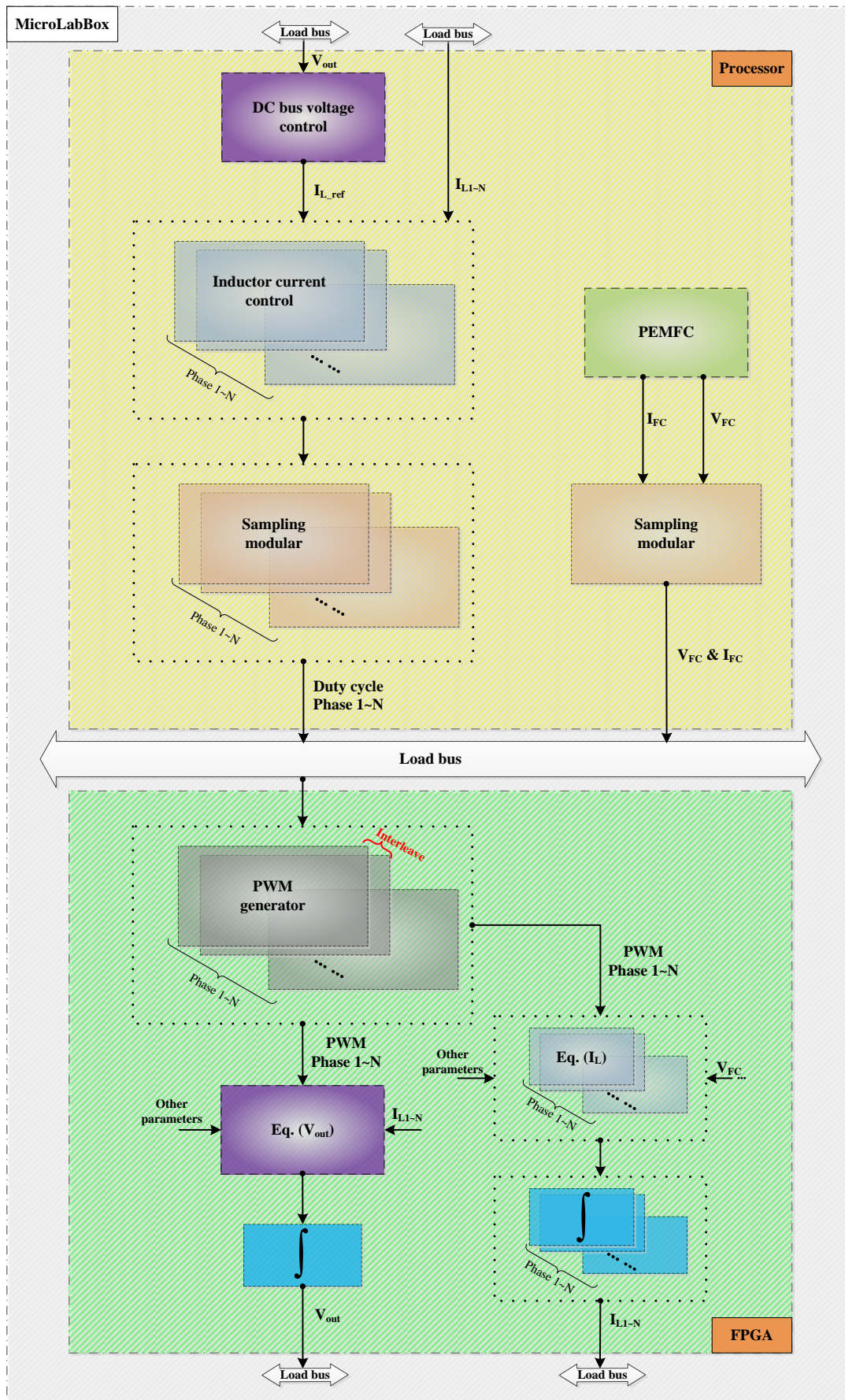


Fig.5.15 Implementation of controller and DC/DC converter models inside the MicroLabBox



Fig.5.16 Signal flow diagram from FPGA of MicroLabBox to external device

Fig.5.16 presents the signal flow diagram from the embedded FPGA to external device. Due to there is a limitation input/output voltage range of the I/O channel ($\pm 10V$), the “FPGA_IO_WRITE_BL” owns a factor around 1/3300 to maximum limit possible damage. This factor is obtained based on several times comparative tests between the input and output values of the blockset. Hence, a “Gain” is required to be added to make the sent out signal be suitable for monitoring. Different values of “Gain” have been chosen for different input signals, as given in Table.5.3.

Table.5.3 Selected “Gain” of each signal sent out through I/O channel

Converter	Input signal	Original value (nominal condition)	“Gain”	Total gain	Output signal value
Boost	I_L/A	300	30	30/3300	2.73
	I_{FC}/A	300	30	30/3300	2.73
	V_{out}/V	350	30	30/3300	3.18
	V_{in}/V	70	30	30/3300	0.64
UC-IBC & IC-IBC	I_L/A	50	300	300/3300	4.55
	I_{FC}/A	300	30	30/3300	2.73
	V_{out}/V	350	30	30/3300	3.18
	V_{in}/V	70	30	30/3300	0.64

In the following subsections, both off-line simulation and real time HIL results of BC, 6-phase UC-IBC, and the 6-phase IC-IBC are presented. Even the specifications of each converter have been given in previous chapter, here they are still be emphasized as Table.5.4. In the case of BC, high current will pass through the power switch which means IGBT is required to be used. Due to IGBT’s inherent characteristic, the switching frequency is selected as 20kHz.

Table.5.4 The specifications of converters

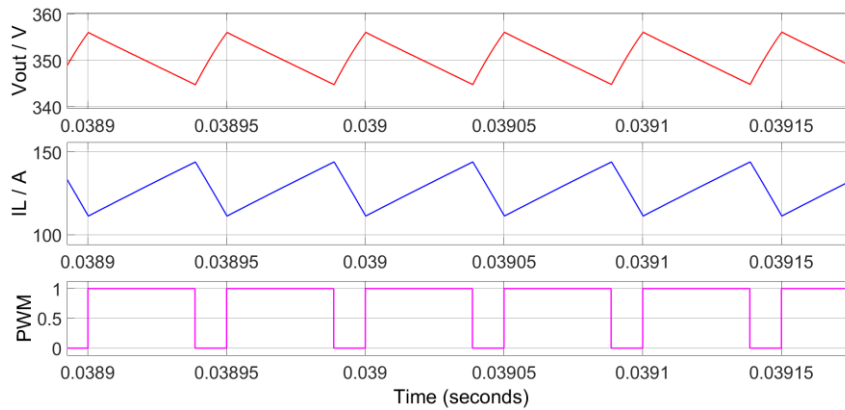
Parameter (@ nominal condition)	Symbol	BC	6-phase UC-IBC	6-phase IC-IBC
Power	P_N	21kW	21kW	21kW
Input voltage	V_{in_N}	70V	70V	70V
Output voltage	V_{out}	350V	350V	350V
Input current	I_{in_N}	300A	300A	300A
Inductor current	I_{L_N}	300A	50A	50A
Inductor current ripple	ΔI_{L_N}	<10%	<10%	<10%
Switching frequency	f_s	20kHz	100kHz	100kHz

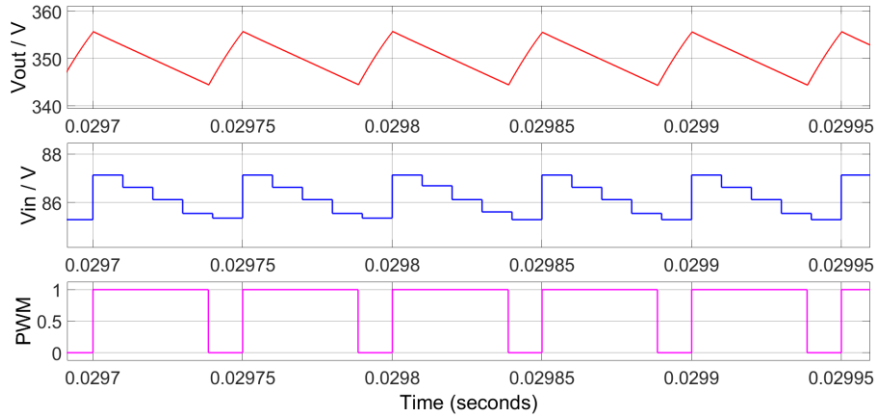
During the off-line simulation, the simulation period is selected as 10ns. The switching period equals $10\mu s$ for UC-IBC and IC-IBC. Thus, one thousand times sampling will be implemented during one switching period. The details of current can be well presented. Meanwhile, the frequencies of FC current, FC voltage and the DC bus voltage are six times of the switching frequency, thus, a short off-line simulation period is necessary. The light load condition has been used to verify the control strategy of each converter during off-line simulations. The full load condition will be verified during HIL.

5.3.3.1. BC verification

The off-line simulation and real time HIL results of BC are separately presented in *part.1* and *part.2* in this subsection.

part.1 Off-line simulation

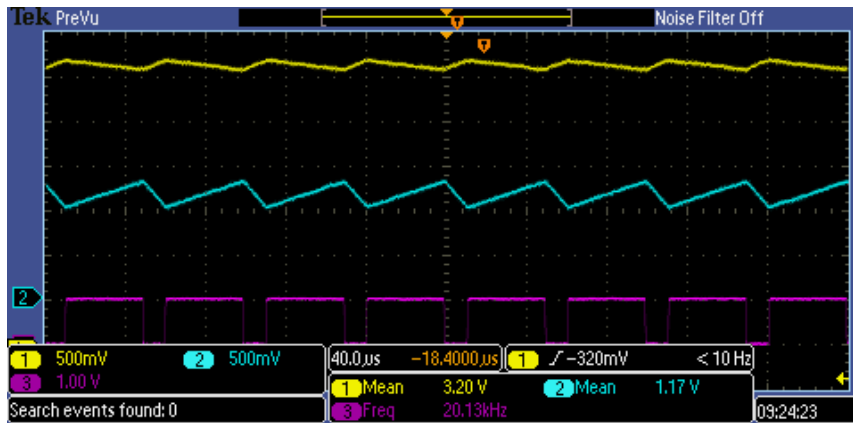
(a) V_{out} , I_L , and PWM signals



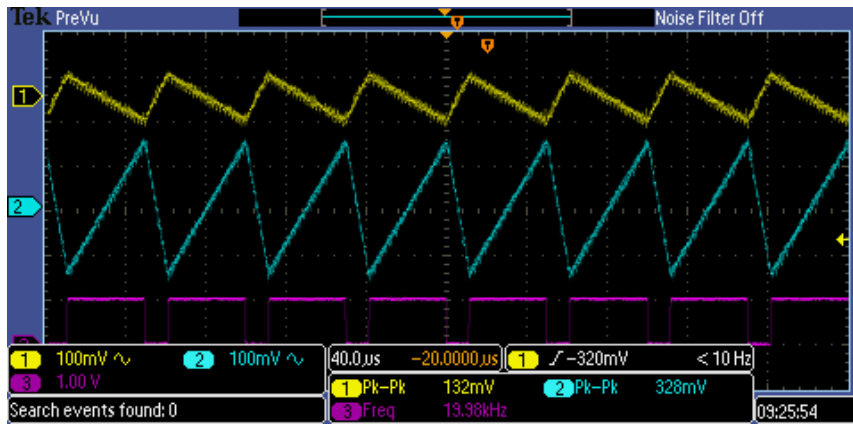
(b) V_{out} , V_{in} , and PWM signals

Fig.5.17 Off-line simulation results of Boost converter at light load condition.

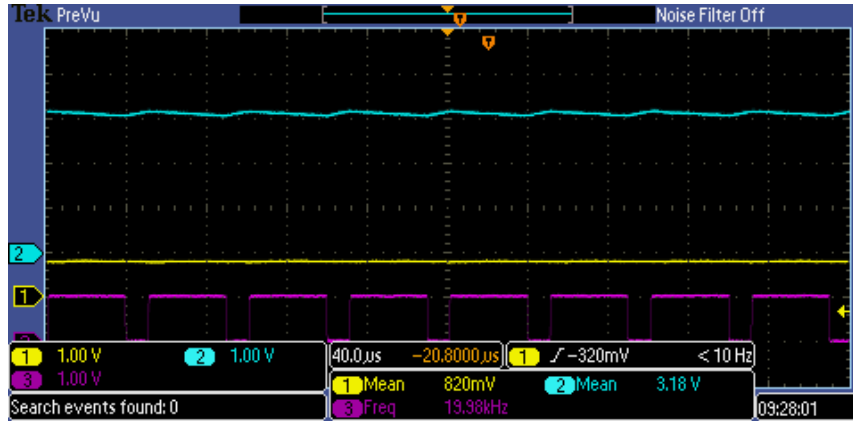
part.2 Real time HIL



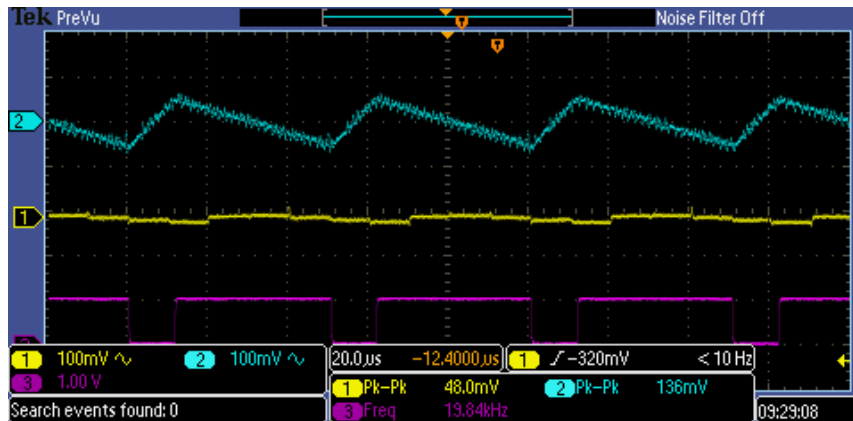
(a) V_{out} (yellow, 500mV/div is equivalent to 55V/div) and I_L (blue, 500mV/div is equivalent to 55A/div) signals.



(b) AC component of V_{out} (yellow, 100mV/div is equivalent to 11V/div) and I_L (blue, 100mV/div is equivalent to 11A/div) signals' peak-peak values.



(c) V_{in} (yellow, 1.00V/div is equivalent to 110V/div) and V_{out} (blue, 1.00V/div is equivalent to 110V/div) signals' mean values.



(d) AC component of V_{in} (yellow, 100mV/div is equivalent to 11V/div) and V_{out} (blue, 100mV/div is equivalent to 11V/div) signals' peak-peak values.

Fig.5.18 HIL results of Boost converter at light load condition.

According to the results in Fig.5.17, off-line simulation of BC has been realized. The switching frequency is 20kHz according to the PWM signal. The output voltage and the inductor current both reach the steady point.

The On-line HIL results of BC are presented in Fig.5.18. In order to observe the ripple of each signal clearly, signals' reference has been set as AC coupling (except PWM signal) and their waveforms are given as (b) and (d). Table.5.5 listed all of the useful information in Fig.5.17 and Fig.5.18. Depending on this comparative analysis, the Boost converter's model in FPGA operates well. However, depending on Table.5.5, differences exist between Off-line simulation and HIL. One possible incentive is that during the period of HIL, the clocking period in the real-time processor is 10µs while the clocking period in FPGA is 10ns. These operating periods are inherent properties

which are determined by hardware performances. Hence, the AC component of each signal can be influenced by the non-synchronized clocking period and acceptable difference will be generated during HIL period.

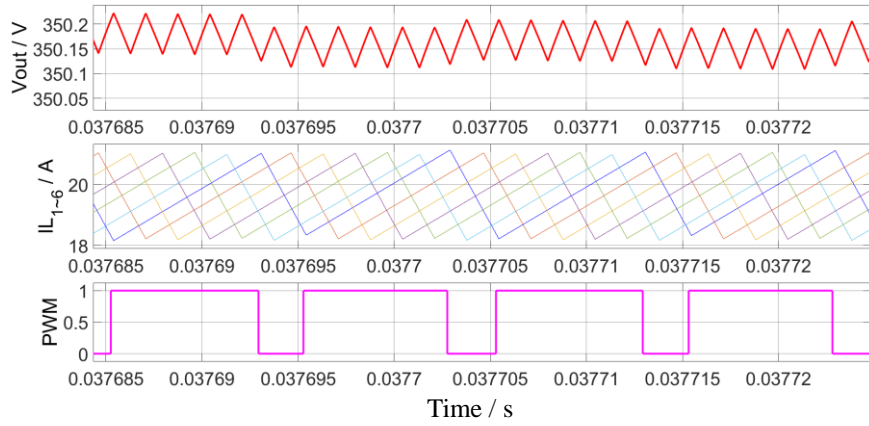
Table.5.5 Off-line simulation and HIL results comparison of BC

	Off-line simulation	HIL	
		I/O output value	Multiplied by total gain
Load condition	Light load	Light load	
Switching frequency	20kHz	20kHz	
V_{out}	350V	3.20V	352V
ΔV_{out}	11.82V	0.132V	14.52V
V_{FC}	86V	0.82V	90.2V
Voltage gain	4	3.9	3.9
I_L	128A	1.17A	128.7A
ΔI_L	35A	0.328A	36.08A
$\Delta I_L/I_L$	27.3%	28.0%	28.0%
I_{FC}	128A	1.17A	128.7A
ΔI_{FC}	35A	0.328A	36.08A
$\Delta I_{FC}/I_{FC}$	27.3%	28.0%	28.0%

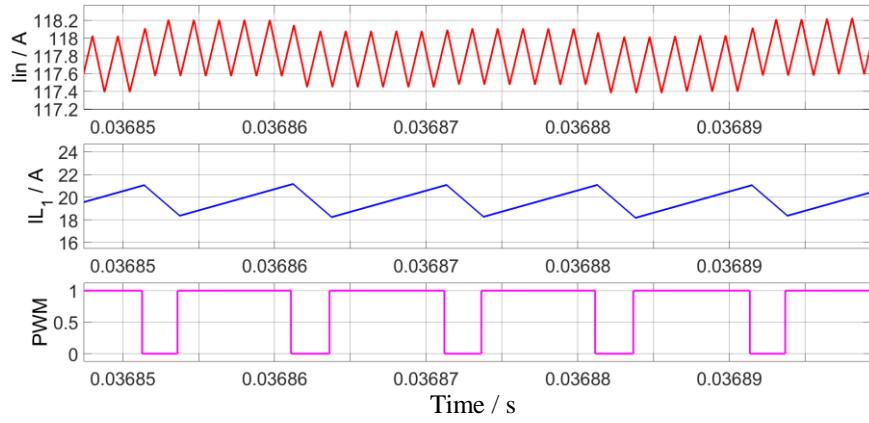
5.3.3.2. 6-phase UC-IBC verification

The off-line simulation and real time HIL results of 6-phase UC-IBC are separately presented in *part.1* and *part.2* in this subsection.

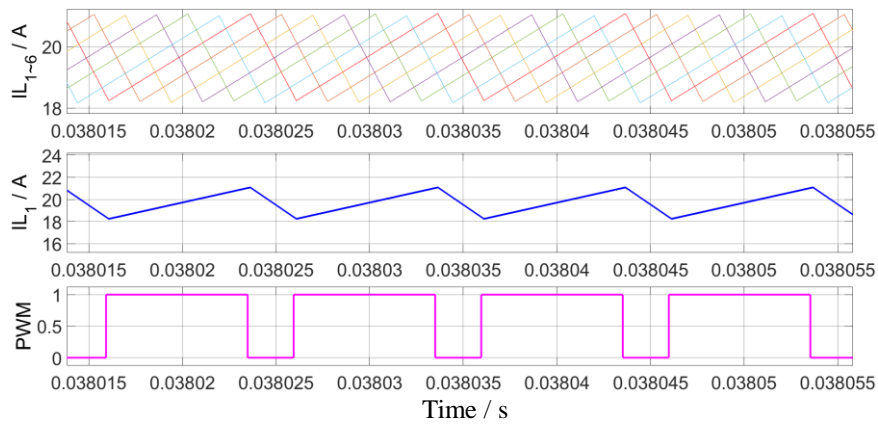
part.1 Off-line simulation



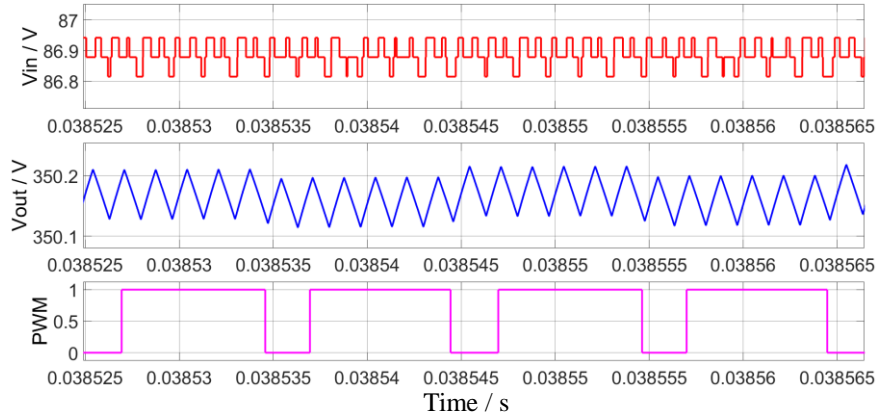
(a) V_{out} , I_{L1-6} , and PWM signals



(b) I_{FC} , I_{L1} , and PWM signals



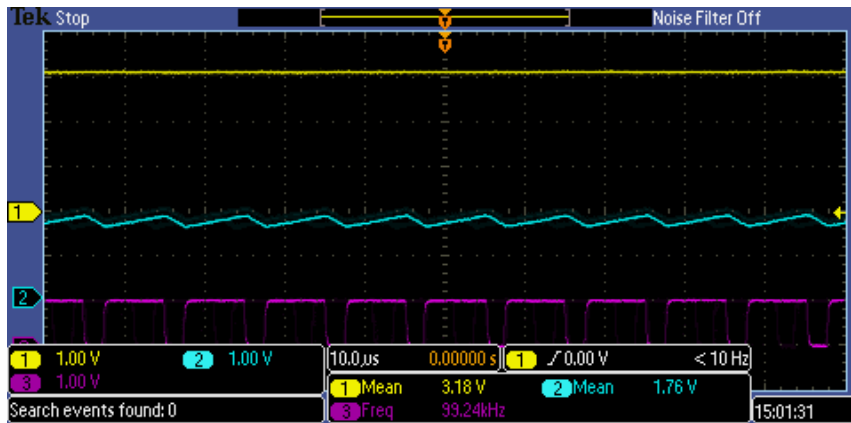
(c) I_{L1-6} , I_{L1} , and PWM signals



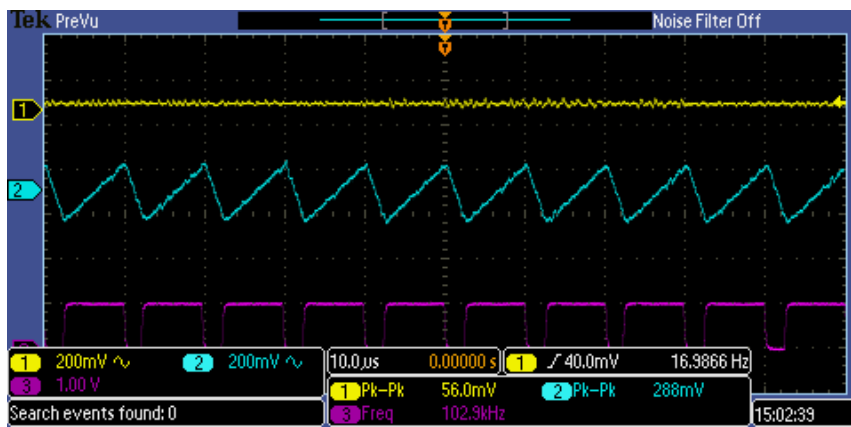
(d) V_{in} , V_{out} , and PWM signals

Fig.5.19 Off-line simulation results of 6-phase UC-IBC at light load condition.

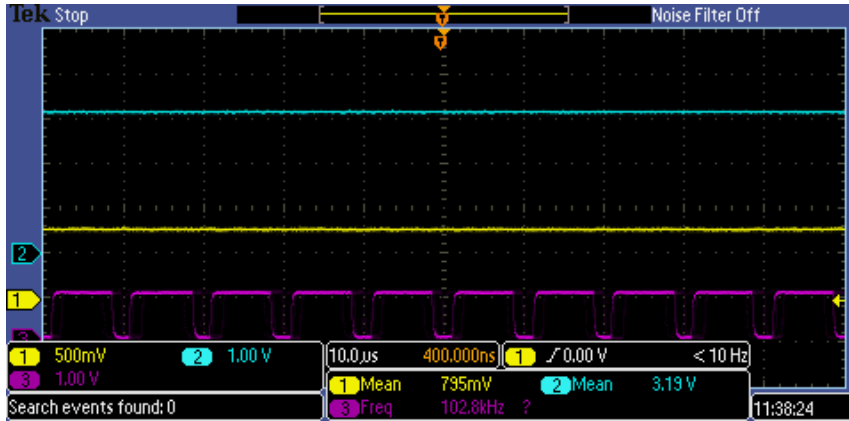
part.2 Real time HIL



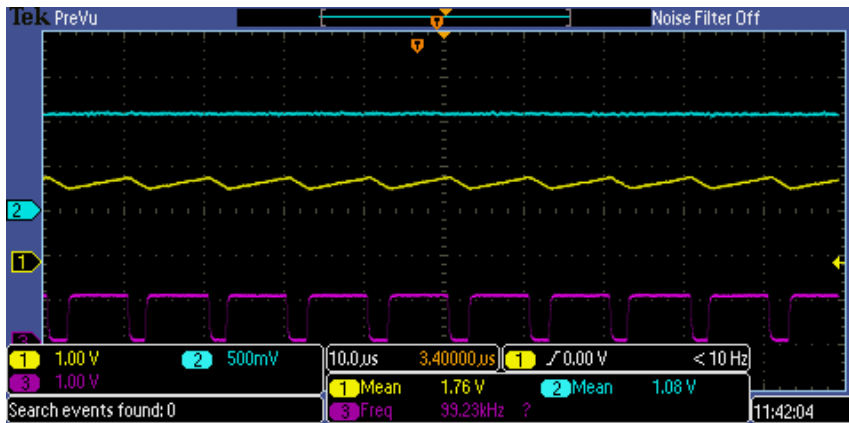
(a) V_{out} (yellow, 1.00V/div is equivalent to 110V/div) and I_{L1} (blue, 1.00V/div is equivalent to 11A/div) signals' mean values.



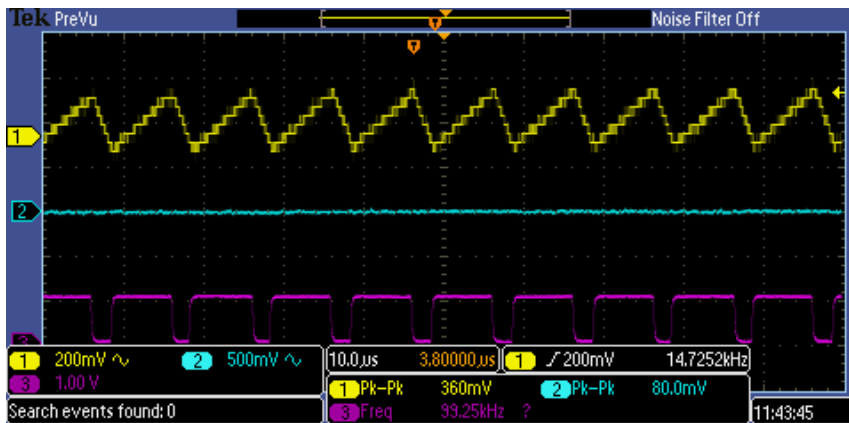
(b) AC component of V_{out} (yellow, 200mV/div is equivalent to 22V/div) and I_{L1} (blue, 200mV/div is equivalent to 2.2A/div) signals' peak-peak values.



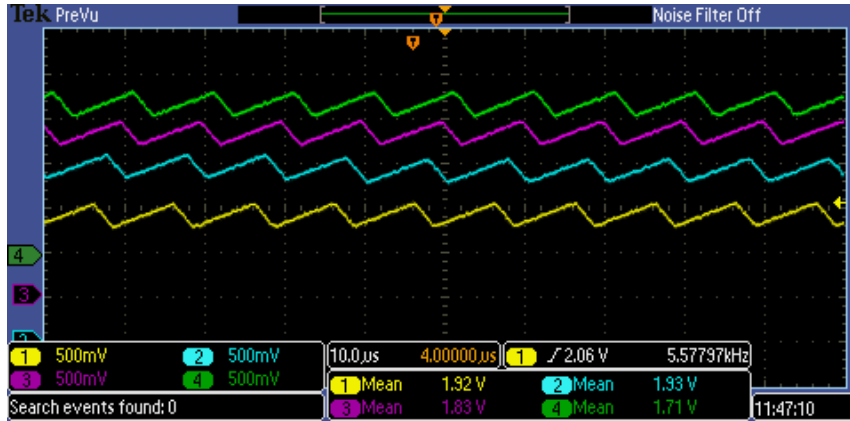
(c) V_{in} (yellow, 500mV/div is equivalent to 55V/div) and V_{out} (blue, 1.00V/div is equivalent to 110V/div) signals' mean values.



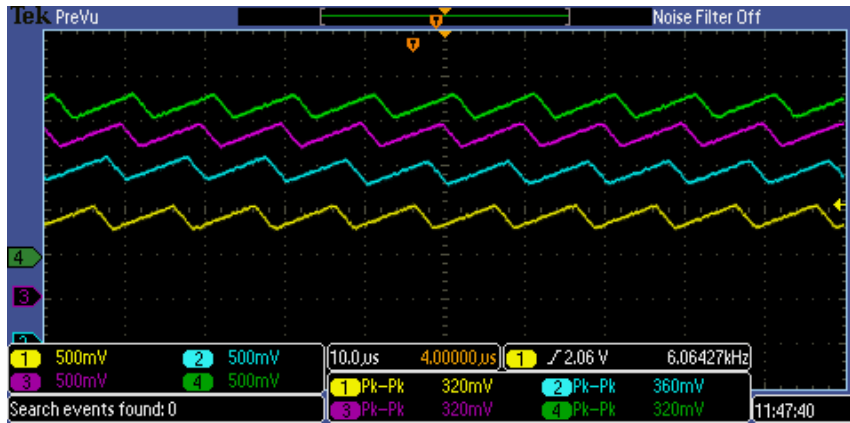
(d) I_{L1} (yellow, 1.00V/div is equivalent to 11A/div) and I_{FC} (blue, 500mV/div is equivalent to 55A/div) signals' mean values.



(e) AC component of I_{L1} (yellow, 200mV/div is equivalent to 2.2A/div) and I_{FC} (blue, 500mV/div is equivalent to 55A/div) signals' peak-peak values.



(f) I_{L1} (yellow, 500mV/div is equivalent to 5.5A/div), I_{L2} (blue, 500mV/div is equivalent to 5.5A/div), I_{L3} (purple, 500mV/div is equivalent to 5.5A/div), and I_{L4} (green, 500mV/div is equivalent to 5.5A/div) signals' mean values.

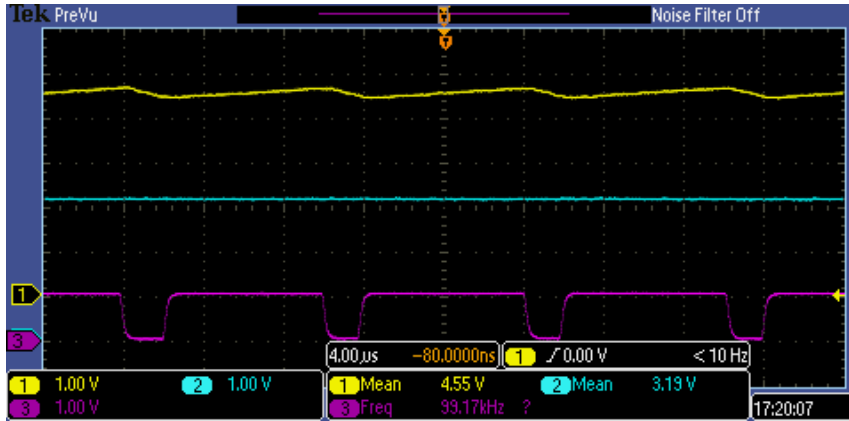


(g) I_{L1} (yellow, 500mV/div is equivalent to 5.5A/div), I_{L2} (blue, 500mV/div is equivalent to 5.5A/div), I_{L3} (purple, 500mV/div is equivalent to 5.5A/div), and I_{L4} (green, 500mV/div is equivalent to 5.5A/div) signals' peak-peak values.

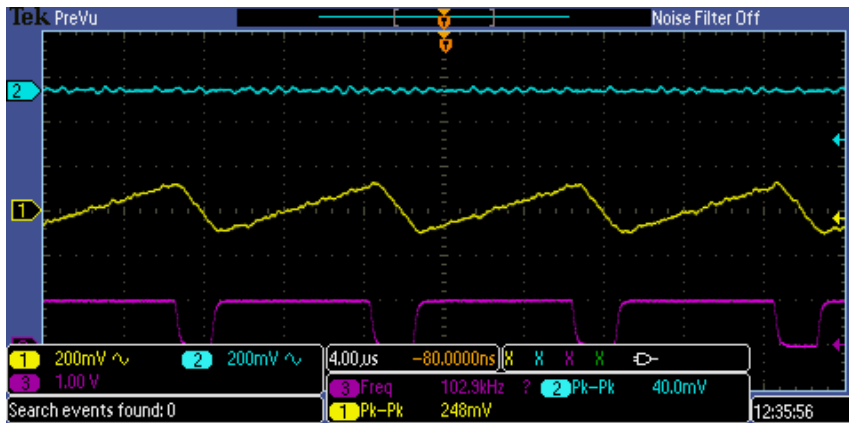


(h) AC component of I_{L1} (yellow, 200mV/div is equivalent to 2.2A/div), I_{L2} (blue, 200mV/div is equivalent to 2.2A/div), I_{L3} (purple, 200mV/div is equivalent to 2.2A/div), and I_{L4} (green, 200mV/div is equivalent to 2.2A/div) signals' frequencies.

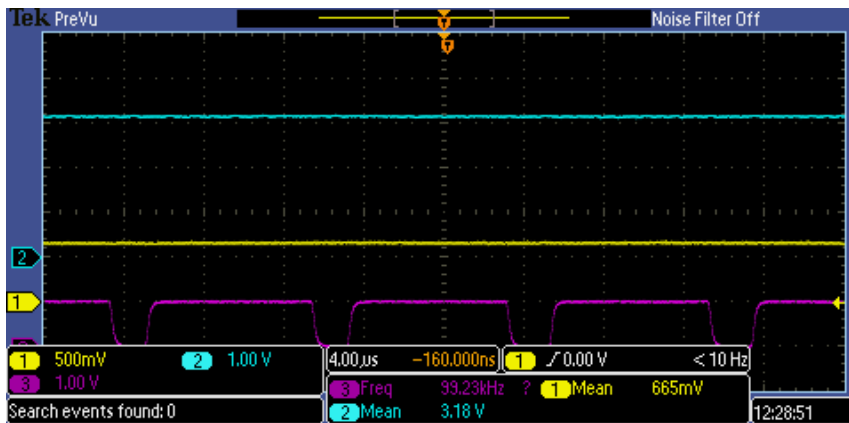
Fig.5.20 On-line HIL results of 6-phase UC-IBC at light load condition.



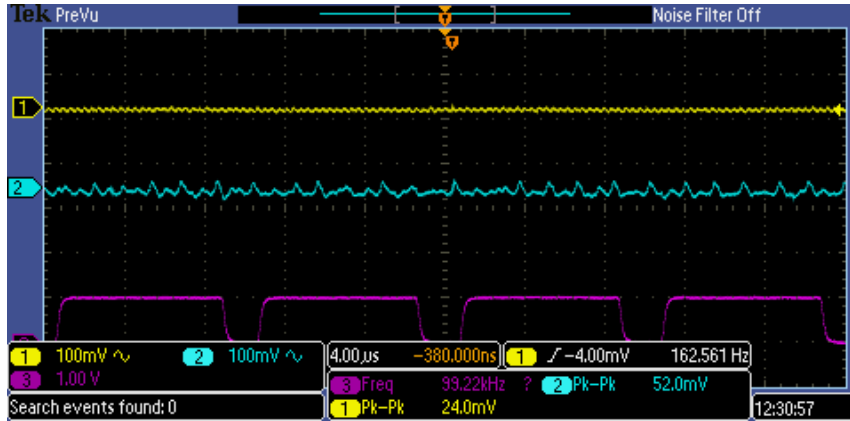
(a) I_{L1} (yellow, 1.00V/div is equivalent to 11A/div) and V_{out} (blue, 1.00V/div is equivalent to 110V/div) signals' mean values.



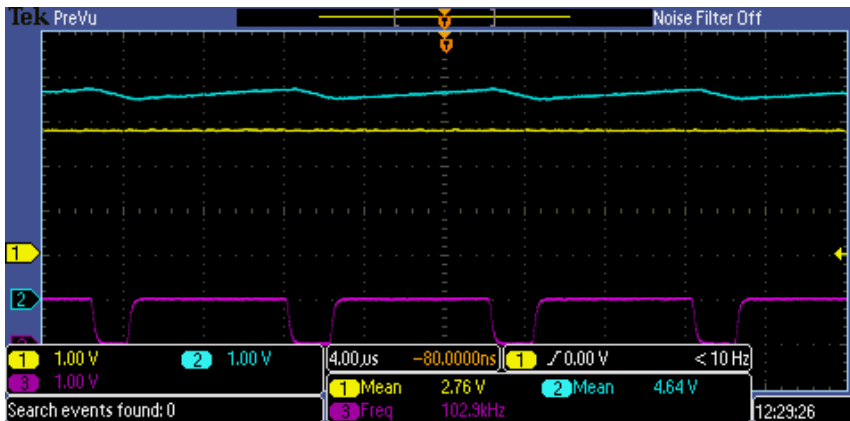
(b) AC component of I_{L1} (yellow, 200mV/div is equivalent to 2.2A/div) and V_{out} (blue, 200mV/div is equivalent to 22V/div) signals' peak-peak values.



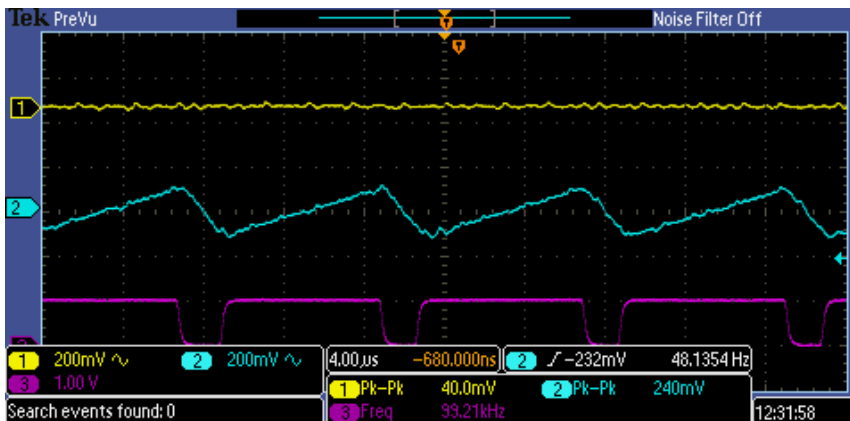
(c) V_{in} (yellow, 500mV/div is equivalent to 55V/div) and V_{out} (blue, 1.00V/div is equivalent to 110V/div) signals' mean values.



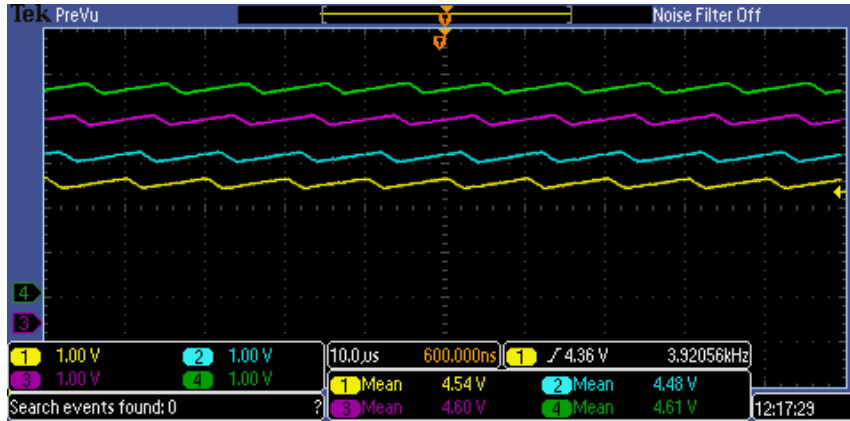
(d) AC component of V_{in} (yellow, 100mV/div is equivalent to 11V/div) and V_{out} (blue, 100mV/div is equivalent to 11V/div) signals' peak-peak values.



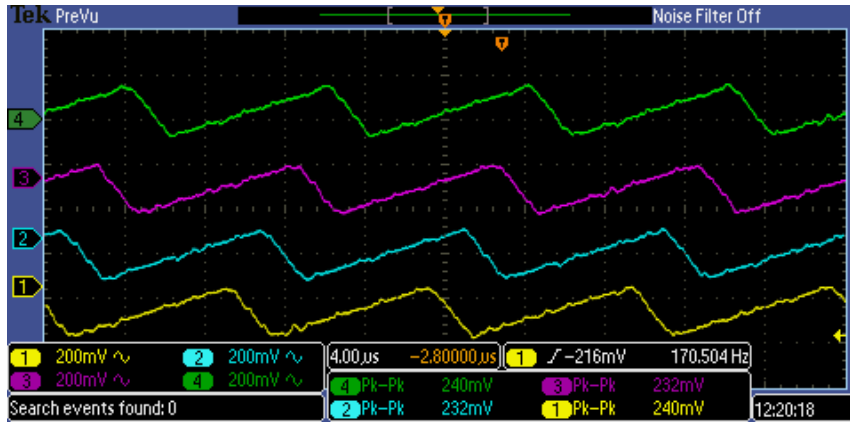
(e) I_{FC} (yellow, 1.00V/div is equivalent to 110A/div) and I_{L1} (blue, 1.00V/div is equivalent to 11A/div) signals' mean values.



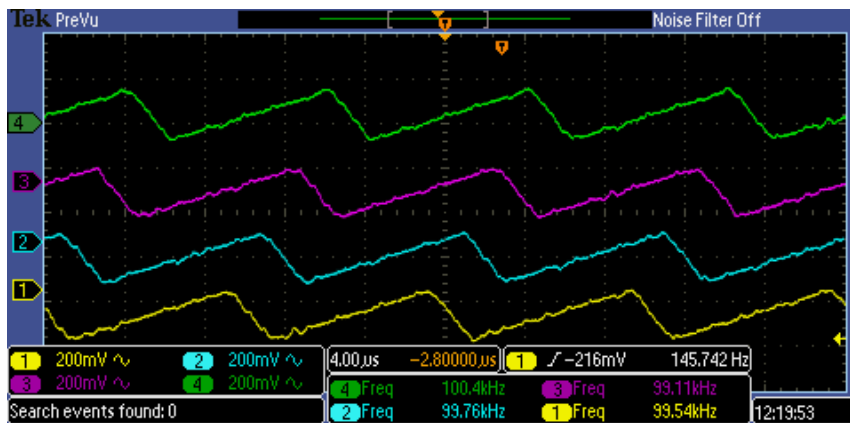
(f) AC component of I_{FC} (yellow, 200mV/div is equivalent to 22A/div) and I_{L1} (blue, 200mV/div is equivalent to 2.2A/div) signals' peak-peak values.



(g) I_{L1} (yellow, 1.00V/div is equivalent to 11A/div), I_{L2} (blue, 1.00V/div is equivalent to 11A/div), I_{L3} (purple, 1.00V/div is equivalent to 11A/div), and I_{L4} (green, 1.00V/div is equivalent to 11A/div) signals' mean values.



(h) AC component of I_{L1} (yellow, 200mV/div is equivalent to 2.2A/div), I_{L2} (blue, 200mV/div is equivalent to 2.2A/div), I_{L3} (purple, 200mV/div is equivalent to 2.2A/div), and I_{L4} (green, 200mV/div is equivalent to 2.2A/div) signals' peak-peak values.



(i) AC component of I_{L1} (yellow, 200mV/div is equivalent to 2.2A/div), I_{L2} (blue, 200mV/div is equivalent to 2.2A/div), I_{L3} (purple, 200mV/div is equivalent to 2.2A/div), and I_{L4} (green, 200mV/div is equivalent to 2.2A/div) signals' frequencies.

Fig.5.21 On-line real time HIL results of 6-phase UC-IBC at full load condition.

According to the results in Fig.5.19, off-line simulation of 6-phase UC-IBC has been realized. The switching frequency is 100kHz according to the PWM signal. The output voltage and the input current both reach the steady point. The inductor currents are kept around 20A. The interleaved control strategy has been realized successfully. The input current and the DC bus voltage are ideal triangle waves combined with the frequency of 600kHz.

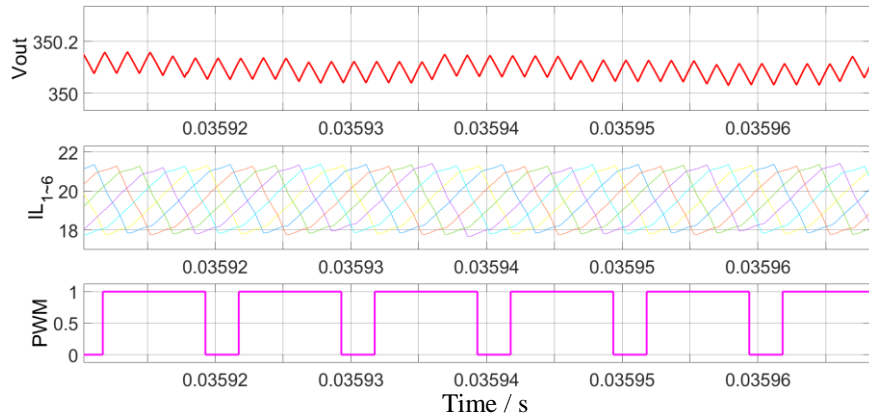
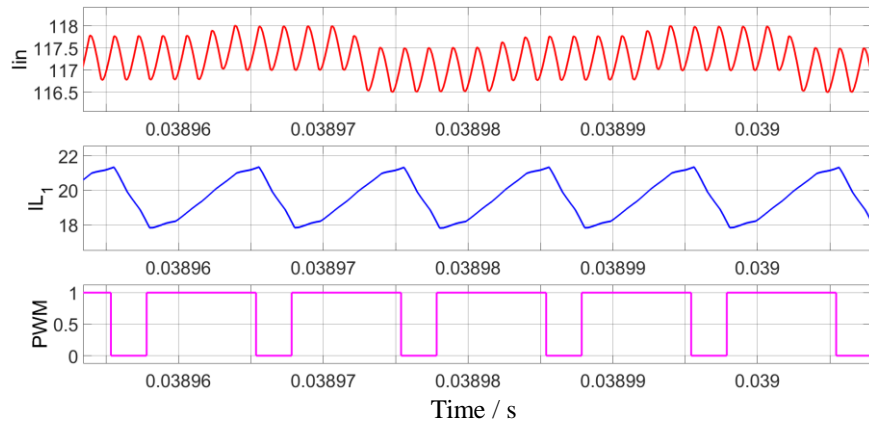
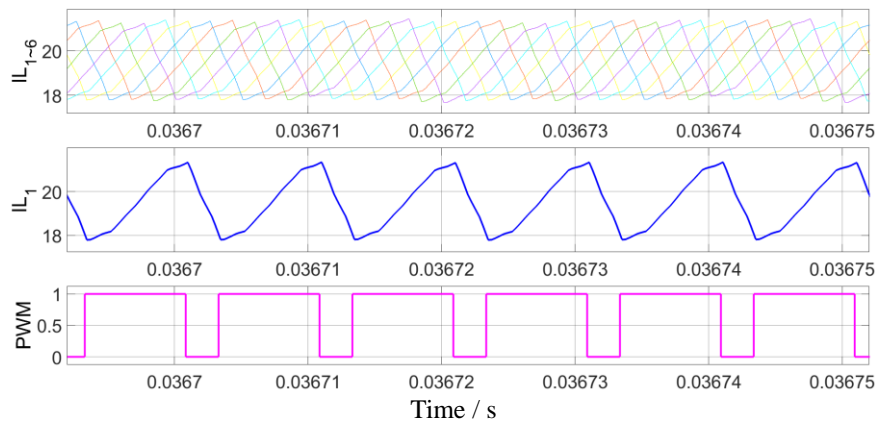
The On-line HIL results of 6-phase UC-IBC at light load condition are presented in Fig.5.20. Then, the On-line HIL at full load condition have also been tested and the results are given as Fig.5.21. Depending on this comparative analysis, the 6-phase UC-IBC's model in FPGA operates well. Table.5.6 listed all of the useful information in Fig.5.19, Fig.5.20 and Fig.5.21. Obviously, the FC current ripple has been reduced below ten percent no matter under light load or full load operating condition. In Fig.5.20 and Fig.5.21, only four inductor currents (from I_{L1} to I_{L4}) have been detected due to the limited channels of the oscilloscope, Tektronix MSO2024B.

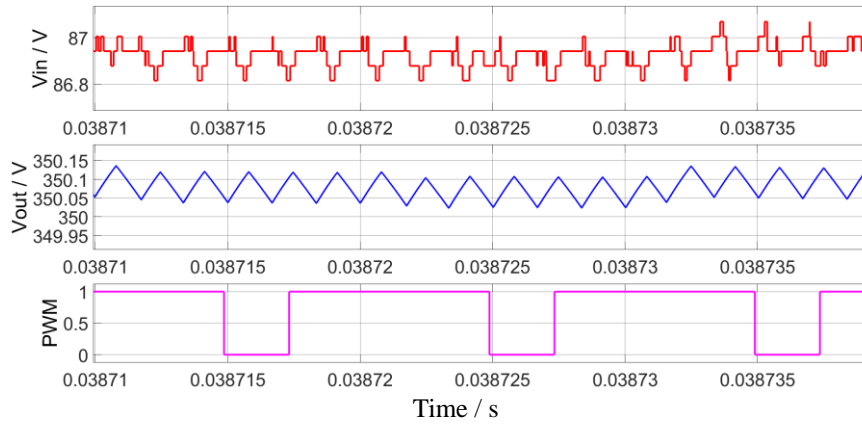
Table.5.6 Off-line simulation and HIL results comparison of 6-phase UC-IBC

	Off-line simulation	HIL			
		I/O output value	Multiplied by total gain	I/O output value	Multiplied by total gain
Load condition	Light load	Light load		Full load	
Switching frequency	100kHz	100kHz			
V_{out}	350.155V	3.18V	349.8V	3.18V	349.8V
ΔV_{out}	0.06V	0.056V	6.16V	0.052V	5.72V
V_{FC}	86.9V	0.795V	87.45V	0.665V	73.15V
Voltage gain	4.03	4	4	4.78	4.78
I_L	19.8A	1.76A	19.36A	4.64A	51.04A
ΔI_L	3A	0.288A	3.168A	0.24A	2.64A
$\Delta I_L/I_L$	15.2%	16.4%	16.4%	5.17%	5.17%
I_{FC}	117.8A	1.08A	118.8A	2.76A	303.6A
ΔI_{FC}	0.6A	0.08A	8.8A	0.04A	4.4A
$\Delta I_{FC}/I_{FC}$	0.5%	7.4%	7.4%	1.45%	1.45%

5.3.3.3. 6-phase IC-IBC verification

The off-line simulation and real time HIL results of the proposed 6-phase IC-IBC are separately presented in *part.1* and *part.2* in this subsection.

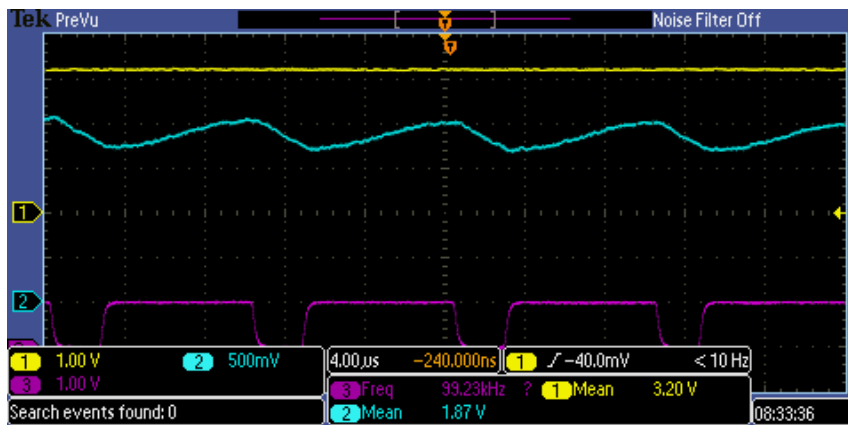
part.1 Off-line simulation(a) V_{out} , I_{L1-6} , and PWM signals(b) I_{FC} , I_{L1} , and PWM signals(c) I_{L1-6} , I_{L1} , and PWM signals



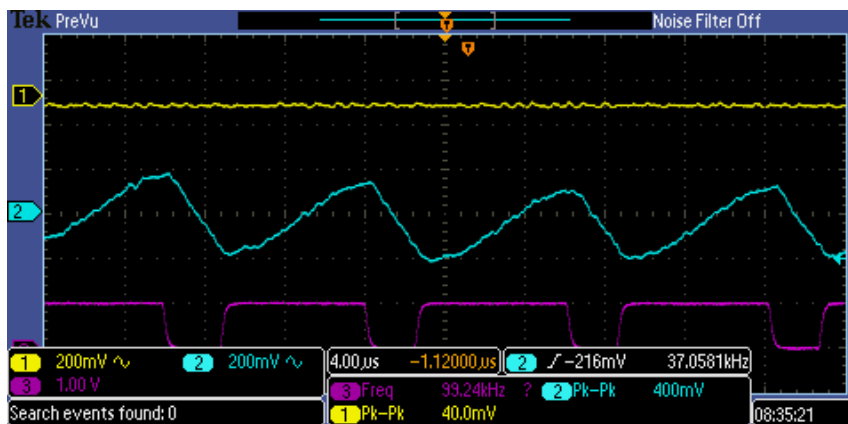
(d) V_{in} , V_{out} , and PWM signals

Fig.5.22 Off-line simulation results of 6-phase IC-IBC at half load condition.

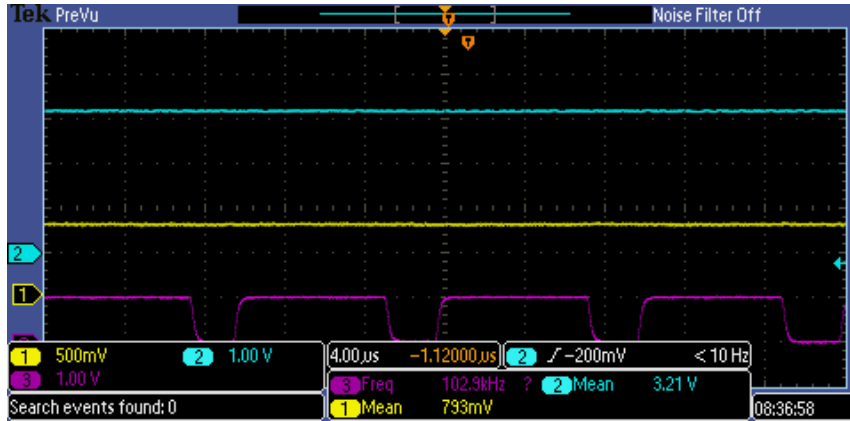
part.2 Real time HIL



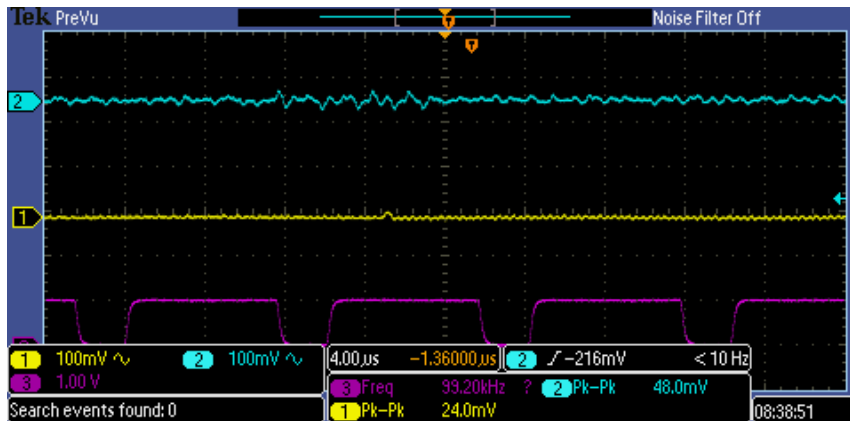
(a) V_{out} (yellow, 1.00V/div is equivalent to 110V/div) and I_{L1} (blue, 500mV/div is equivalent to 5.5A/div) signals.



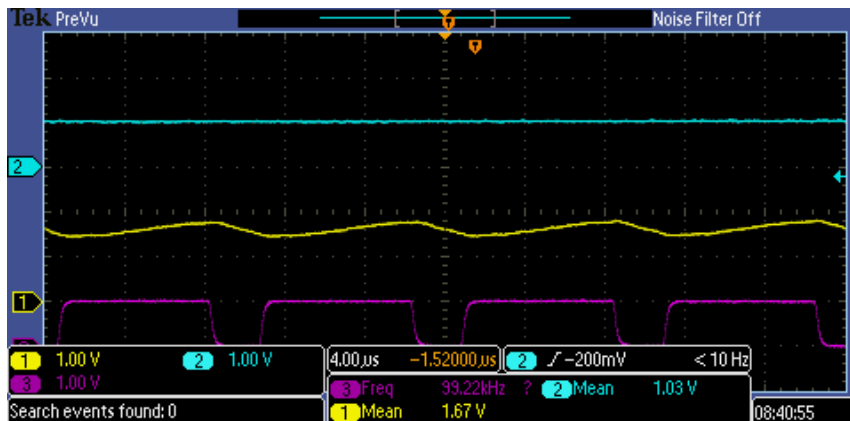
(b) AC component of V_{out} (yellow, 200mV/div is equivalent to 22V/div) and I_{L1} (blue, 200mV/div is equivalent to 2.2A/div) signals' peak-peak values.



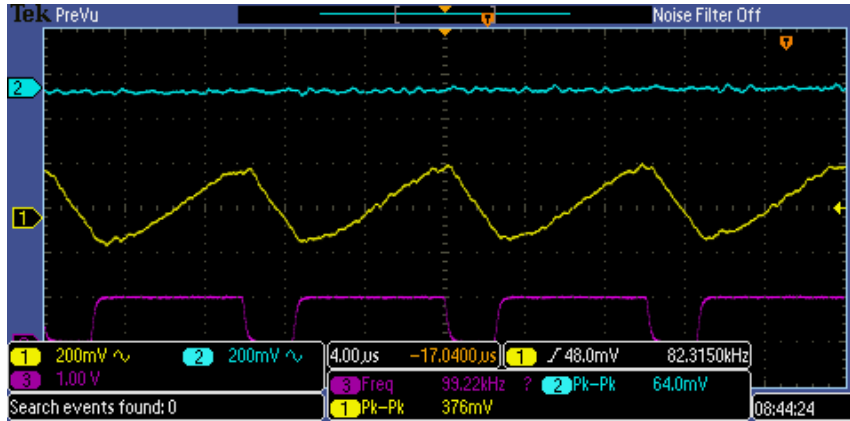
(c) V_{in} (yellow, 500mV/div is equivalent to 55V/div) and V_{out} (blue, 1.00V/div is equivalent to 110V/div) signals.



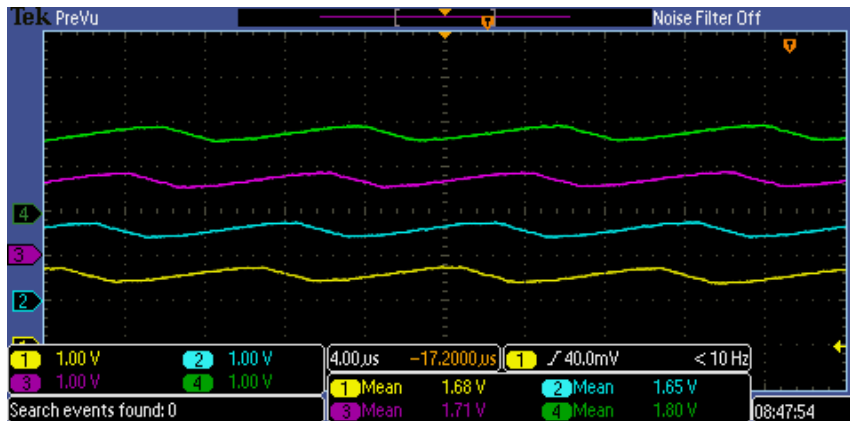
(d) AC component of V_{in} (yellow, 100mV/div is equivalent to 11V/div) and V_{out} (blue, 100mV/div is equivalent to 11V/div) signals' peak-peak values.



(e) I_{L1} (yellow, 1.00V/div is equivalent to 11A/div) and I_{FC} (blue, 1.00V/div is equivalent to 110A/div) signals.



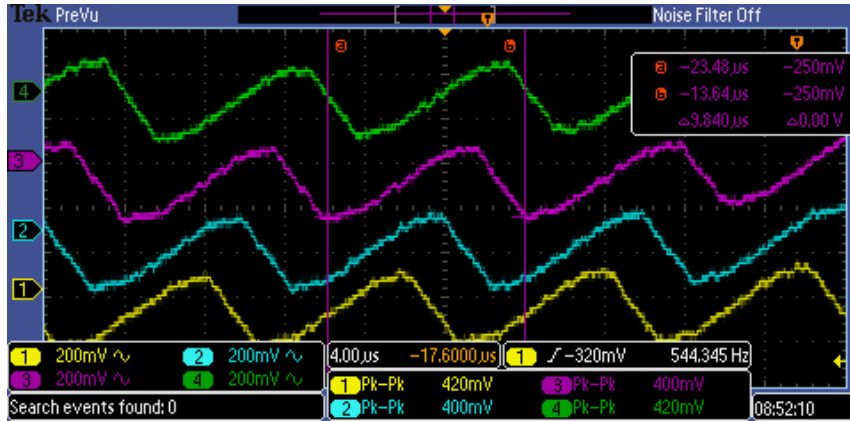
(f) AC component of I_{L1} (yellow, 200mV/div is equivalent to 2.2A/div) and I_{FC} (blue, 200mV/div is equivalent to 22A/div) signals' peak-peak values.



(g) I_{L1} (yellow, 1.00V/div is equivalent to 11A/div), I_{L2} (blue, 1.00V/div is equivalent to 11A/div), I_{L3} (purple, 1.00V/div is equivalent to 11A/div), and I_{L4} (green, 1.00V/div is equivalent to 11A/div) signals.

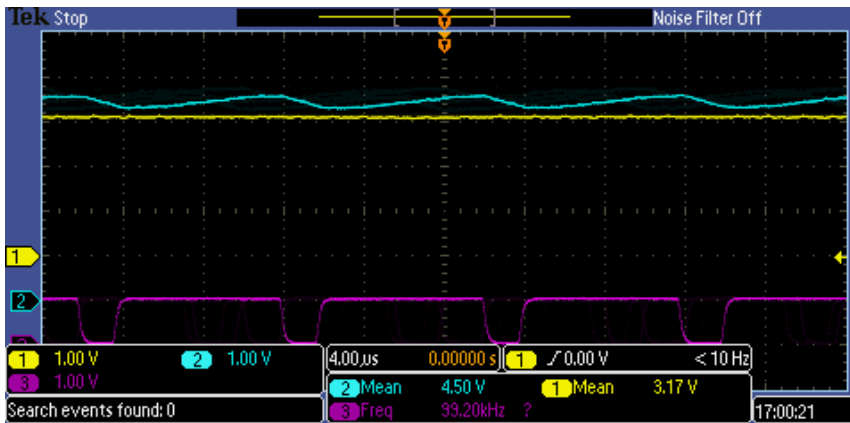


(h) I_{L1} (yellow, 1.00V/div is equivalent to 11A/div), I_{L2} (blue, 1.00V/div is equivalent to 11A/div), I_{L3} (purple, 1.00V/div is equivalent to 11A/div), and I_{L4} (green, 1.00V/div is equivalent to 11A/div) signals' frequencies.

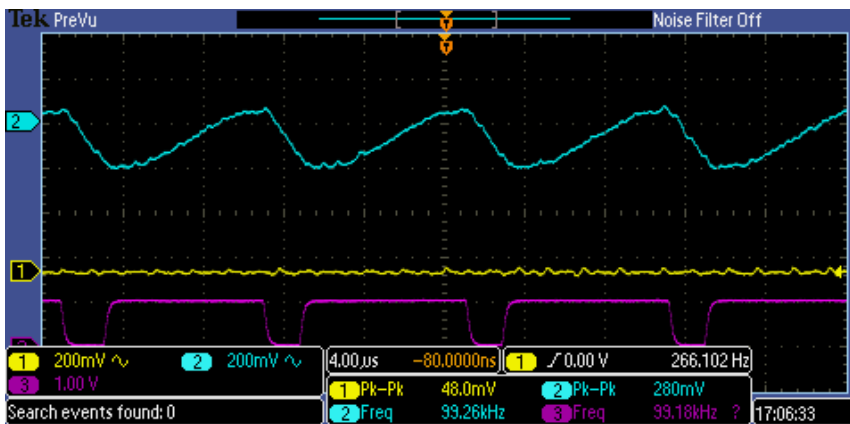


(i) AC component of I_{L1} (yellow, 200mV/div is equivalent to 2.2A/div), I_{L2} (blue, 200mV/div is equivalent to 2.2A/div), I_{L3} (purple, 200mV/div is equivalent to 2.2A/div), and I_{L4} (green, 200mV/div is equivalent to 2.2A/div) signals' peak-peak values.

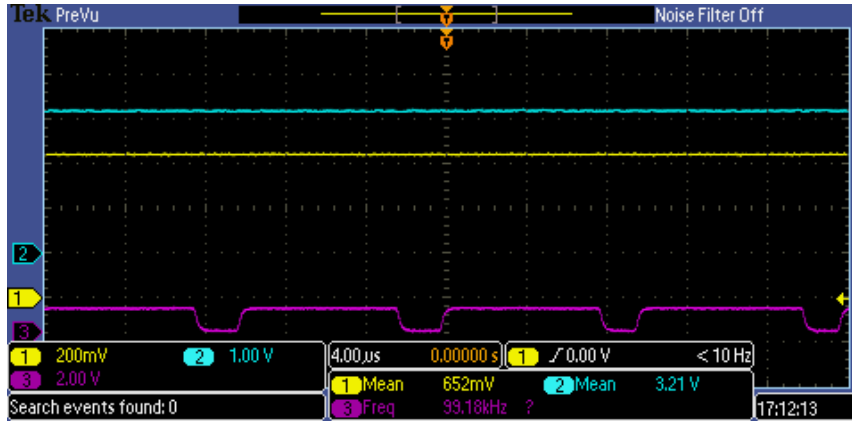
Fig.5.23 On-line HIL results of 6-phase IC-IBC at light load condition.



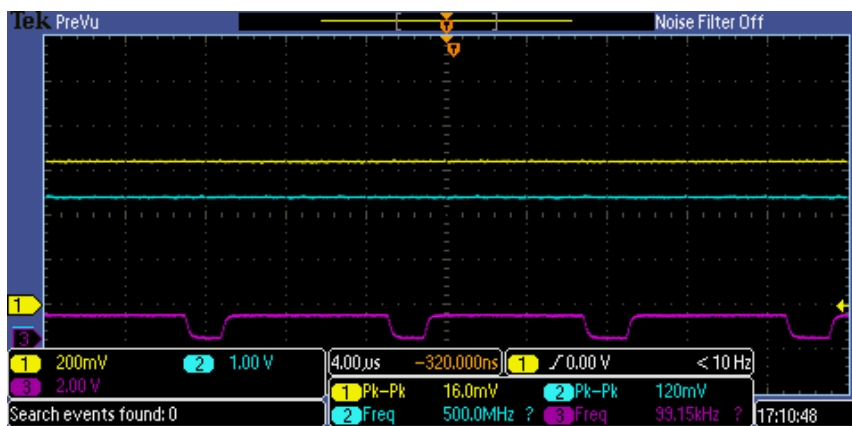
(a) V_{out} (yellow, 1.00V/div is equivalent to 110V/div) and I_{L1} (blue, 1.00V/div is equivalent to 11A/div) signals' mean values.



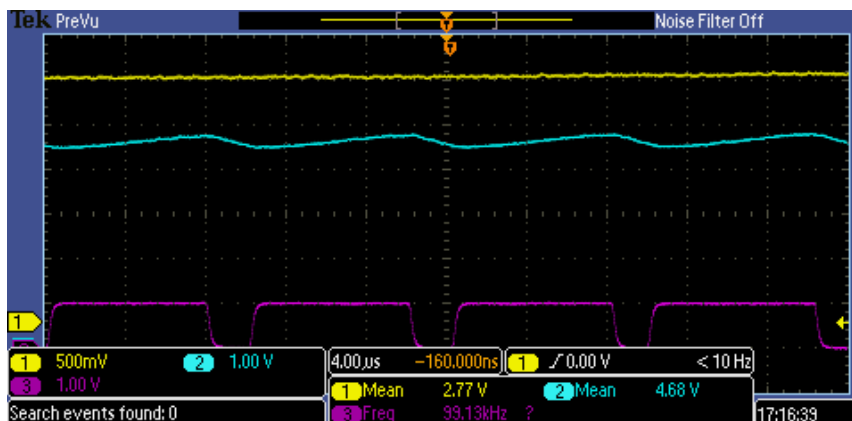
(b) AC component of V_{out} (yellow, 200mV/div is equivalent to 22V/div) and I_{L1} (blue, 200mV/div is equivalent to 2.2A/div) signals' peak-peak values.



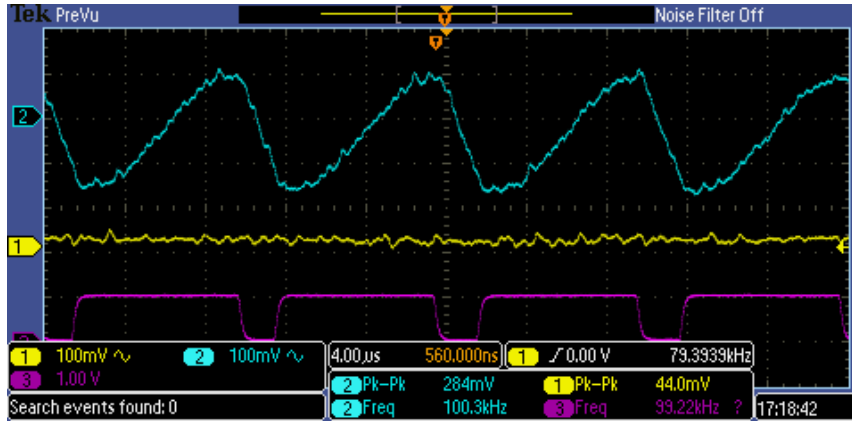
(c) V_{in} (yellow, 200mV/div is equivalent to 22V/div) and V_{out} (blue, 1.00V/div is equivalent to 110V/div) signals.



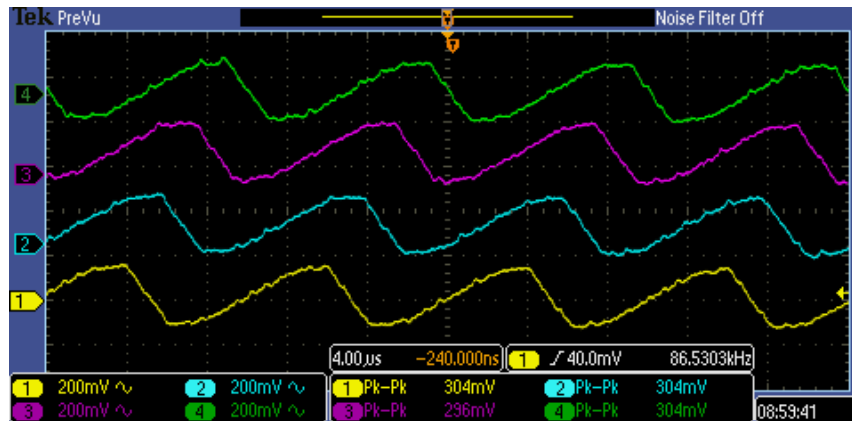
(d) AC component of V_{in} (yellow, 200mV/div is equivalent to 22V/div) and V_{out} (blue, 1.00V/div is equivalent to 110V/div) signals' peak-peak values.



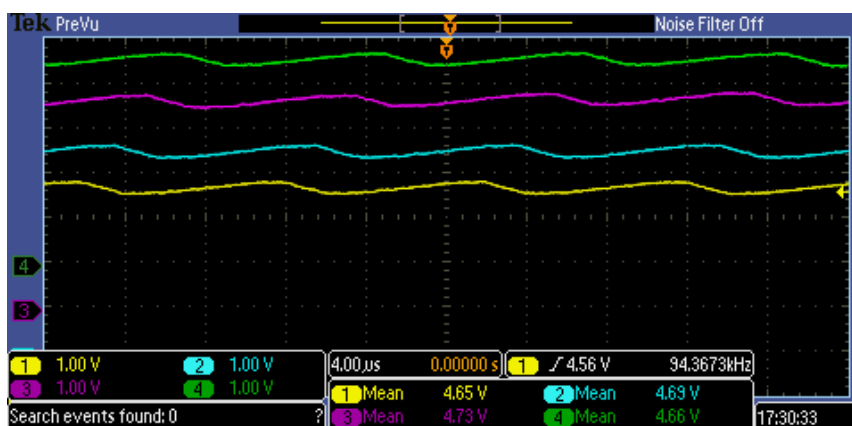
(e) I_{FC} (yellow, 500mV/div is equivalent to 55A/div) and I_{L1} (blue, 1.00V/div is equivalent to 11A/div) signals.



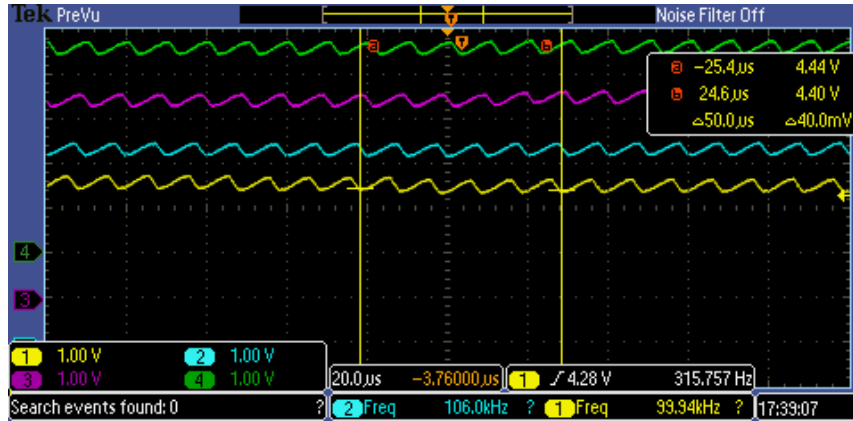
(f) AC component of I_{FC} (yellow, 100mV/div is equivalent to 11A/div) and I_{L1} (blue, 100mV/div is equivalent to 1.1A/div) signals' peak-peak values.



(g) I_{L1} (yellow, 200mV/div is equivalent to 2.2A/div), I_{L2} (blue, 200mV/div is equivalent to 2.2A/div), I_{L3} (purple, 200mV/div is equivalent to 2.2A/div), and I_{L4} (green, 200mV/div is equivalent to 2.2A/div) signals.



(h) I_{L1} (yellow, 1.00V/div is equivalent to 11A/div), I_{L2} (blue, 1.00V/div is equivalent to 11A/div), I_{L3} (purple, 1.00V/div is equivalent to 11A/div), and I_{L4} (green, 1.00V/div is equivalent to 11A/div) signals' mean values.



(i) I_{L1} (yellow, 1.00V/div is equivalent to 11A/div), I_{L2} (blue, 1.00V/div is equivalent to 11A/div), I_{L3} (purple, 1.00V/div is equivalent to 11A/div), and I_{L4} (green, 1.00V/div is equivalent to 11A/div) signals' frequencies.

Fig.5.24 On-line HIL results of 6-phase IC-IBC at full load condition.

According to the results in Fig.5.22, off-line simulation of the proposed 6-phase IC-IBC has been realized. The switching frequency is 100kHz according to the PWM signal. The output voltage and the input current both reach the steady point. The inductor currents are kept around 20A and satisfy the requirements. The interleaved control strategy has been realized successfully. Obviously, there are more stages of inductor current during one operating period than BC and 6-phase UC-IBC. As the input current presented here is the sum of inductor current of each phase, its frequency is six times the switching frequency. Similarly, the DC bus voltage is also a triangle wave combined the frequency of 600kHz.

The On-line real time HIL results of the proposed 6-phase IC-IBC at light load condition are presented in Fig.5.23. Then, the On-line HIL at full load condition have also been tested and the results are given as Fig.5.24. Depending on this comparative analysis, the 6-phase IC-IBC's model in FPGA operates well. To be emphasized, the inductor current operating process has more stages. Due to the limitation of XSG I/O blockset's sampling capacity, the detail can't be very well presented during On-line HIL period. Table.5.7 listed all of the useful information in Fig.5.22, Fig.5.23 and Fig.5.24. Obviously, the FC current ripple has been reduced below ten percent no matter under light load or full load operating condition.

Table.5.7 Off-line simulation and HIL results comparison of 6-phase IC-IBC

	Off-line simulation	HIL			
		I/O output value	Multiplied by total gain	I/O output value	Multiplied by total gain
Load condition	Light load	Light load		Full load	
Switching frequency	100kHz	100kHz			
V_{out}	350.15V	3.20V	352V	3.17V	348.7V
ΔV_{out}	0.1V	0.04V	4.4V	0.048V	5.28V
V_{FC}	86.9V	0.793V	87.23V	0.652V	71.72V
Voltage gain	4.03	4.04	4.04	4.86	4.86
I_L	19.8A	1.87A	20.57A	4.5A	49.5A
ΔI_L	3.3A	0.4A	4.4A	0.28A	3.08A
$\Delta I_L/I_L$	16.7%	21.4%	21.4%	6.2%	6.2%
I_{FC}	117.5A	1.03A	113.3A	2.77A	304.7A
ΔI_{FC}	1A	0.064A	7.04A	0.044A	4.84A
$\Delta I_{FC}/I_{FC}$	0.85%	6.21%	6.21%	1.6%	1.6%

5.4. Conclusion

The real-time HIL validation is a powerful and effective method for the verification of topology and control strategy in power electronics application. In this chapter, BC, 6-phase IBC, and the proposed 6-phase IC-IBC are validated by real-time HIL. MicroLabBox, which is the production of dSPACE, has been used as the HIL platform. A real-time processor and an FPGA are embedded inside MicroLabBox. The load bus is performed as data-set transmission interface. The modeling processes of different modules have been illustrated in this chapter. Both off-line and on-line HIL results of these three converters are presented and compared. Obviously, these results coincide with the theoretical analysis. The input current ripples of 6-phase IBC and IC-IBC are much smaller than the one of BC. Therefore, the successfully executed HIL helps verify the principle, accuracy, and correctness of the proposed topology. As HIL is based on Hardware Description Language (HDL), it can get much closer to actual operation of a converter than the simulation only based

on PC. Hence, the design and verification of hardware platform can be more effective.

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- [5-6] Pukrushpan, J. T., Stefanopoulou, A. G., & Peng, H. Control of fuel cell power systems: principles, modeling, analysis and feedback design [M]. Springer Science & Business Media. 2004.
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Conclusion and perspectives

In today's Fuel Cell Electric Vehicle (FCEV), DC/DC converter is required to boost the output voltage of PEMFC to high level (400~700V). Towards this target, the main aim of this thesis is to design a DC/DC boost converter with high efficiency, high compactness and high voltage gain ratio.

To promote the utilization and commercialization of FC technologies, the reliability and durability have to be improved. Electrochemical Impedance Spectroscopy (EIS) is widely used for PEMFC's diagnosis. To remove additional equipment and sensor, on-line EIS detection functionality integrated with the control strategy of the proposed PEMFC connected to the DC/DC boost converter is also addressed.

The main contributions of this thesis work are summarized as follow.

1. The current development status of FCEV is comparative analyzed. Different DC/DC boost converters for FCEV application are studied. The on-line EIS strategy integrated into PEMFC connected converter is reviewed. At last, the requirement of multi-functional DC/DC boost converter for FCEV application is proposed.
2. A 6-phase Interleaved Boost Converter based on SiC semiconductors and inverse coupled inductors of cyclic cascade structure (IC-IBC) is proposed.
 - 2.1. The interleaved structure contributes to decrease the FC current ripple and the FC lifespan can be extended. Meanwhile, the high input current is shared by multi-phase. The electrical stress of power switch is decreased; the reliability and redundancy of converter are increased.
 - 2.2. The SiC-based semiconductors contribute to increase switching frequency and decrease power losses. These new components are possible operating with high frequency (100kHz in this study) while good thermal performances can be obtained. At the same time, high frequency helps to reduce the magnetic component's volume and weight. Meanwhile, SiC-based power MOSFET's switching loss and SiC-based power Schottky diode's reverse recovering loss are much lower than that of Si-based power semiconductors. Hence, the efficiency of the proposed converter is promoted and the

requirement of thermal dissipation is reduced.

- 2.3. The inverse coupled inductor based on cyclic cascade structure contributes to decrease volume and weight of the magnetic component. Two phases are inversely coupled by one magnetic core. The magnetic fluxes flow in opposite direction inside the magnetic core; hence, the DC components are almost canceled. Therefore, there are only magnetic flux's AC component exists and the volume of the magnetic core is reduced significantly.
3. Sliding-Mode Control (SMC) strategy is applied to the proposed converter. Due to SMC's great robustness, the DC component of inductor's current is well controlled. No significant difference exists between two neighbor phases' current. The magnetic saturation is avoided.
4. On-line EIS detection functionality is integrated with SMC of the proposed DC/DC boost converter. Both membrane drying and flooding, which are most common during actual application, are estimated based on PEMFC's equivalent electric circuit model. According to the comparative analysis between theoretical and simulated results, the proposed diagnostic method is effective for different kinds of PEMFC faults. No additional equipment and sensor are needed for the proposed method. The complexity of PEMFC system can be decreased and the reliability can be increased.
5. The real-time HIL validation of the proposed converter is realized. MicroLabBox, which owns the embedded real-time processor and FPGA, is used as the real-time platform. A 21kW PEMFC's voltage model is developed as the power source. HIL platform provides the advantage to observe the converter's dynamic operating process in real-time which is not possible for the off-line simulation.

A summary of related research interests, which deserve future investigation, is presented here.

1. Finish the hardware development of the proposed IC-IBC. The prototype will be a reduced power scale converter around 1kW. The actual PEMFC will be used as the power source. The control strategy of converter and the proposed on-line EIS detection functionality will be developed inside the real-time processor of MicroLabBox. The PEMFC, MicroLabBox, and the prototype converter will be tested corporately in FCLAB platform.

2. Develop the fault control strategy for the proposed IC-IBC. The most common fault is short circuit and power switch failure. Once the fault occurs in one phase or more, the current of each inductor winding will be different a lot from the normal condition. The magnetic saturation will occur inside the magnetic core. Therefore, it is essential to propose the fault control strategy to keep IC-IBC operating even under fault conditions and to improve the reliability of the system.
3. As the detection period of EIS can be relatively long, especially for the low frequency injected signals, it is significant to improve the proposed strategy with new signal processing method which can shorten the calculation period of impedance.
4. The real-time model of SiC-based semiconductor is attractive to be developed. The average model of converter has been studied in this research for the real-time HIL validation. However, the switching process of SiC MOSFET and SiC Schottky cannot be detected. Although the manufacture has provided devices' models, they can only be applied in off-line simulation. The development of SiC-based power switch's real-time model can depend on the component datasheet or the experiment obtained datasets, or the combination of both. In this way, the operating process of power switch can be detected and evaluated in real-time. The development cost and period will be reduced especially for the high power application.
5. HIL validation of whole traction system of FCEV based on real driving cycle is necessary to be addressed. The proposed DC/DC converter can be constructed in series or in parallel to satisfy the total power requirement of FCEV for real application. Based on HIL platform, high power level verification can be addressed easily. Meanwhile, the proposed EIS strategy is also necessary to be verified based on real driving cycle.

Personal Publications

Journal Articles

- 1 Hanqing WANG, Arnaud GAILLARD, and Daniel HISSSEL. "Online electrochemical impedance spectroscopy detection integrated with step-up converter for fuel cell electric vehicle [J]." *International Journal of Hydrogen Energy* 44.2 (2019): 1110-1121. (doi.org/10.1016/j.ijhydene.2018.10.242).
- 2 Hanqing WANG, Arnaud GAILLARD, and Daniel HISSSEL. "A review of DC/DC converter-based electrochemical impedance spectroscopy for fuel cell electric vehicles [J]." *Renewable Energy*, 2019. (doi.org/10.1016/j.renene.2019.03.130).

International Conferences

- 1 Hanqing WANG, Arnaud GAILLARD, and Daniel HISSSEL. "6-Phase Soft-Switching Interleaved Boost Converter Based on SiC Semiconductor for Fuel Cell Vehicles [C]." *2016 IEEE Vehicle Power and Propulsion Conference (VPPC)*. IEEE, Oct.2016. (Oral).
- 2 Hanqing WANG, Arnaud GAILLARD, and Daniel HISSSEL. "Six-Phase Soft-Switching Interleaved Boost Converter Based on SiC Semiconductor and Coupled Inductor for Fuel Cell Vehicles [C]." *2017 IEEE Vehicle Power and Propulsion Conference (VPPC)*. IEEE, Dec.2017. (Poster).
- 3 Hanqing WANG, Arnaud GAILLARD, and Daniel HISSSEL. "Theoretical analysis of six-phase interleaved boost converter based on SiC semiconductor and inverse coupled inductor for fuel cell electric vehicle application [C]." *2019 ELECTRICMACS*. May.2019. (Paper accepted and oral presentation).

National Conferences

- 1 Hanqing WANG, Arnaud GAILLARD, and Daniel HISSSEL. "DC/DC converter based on SiC semiconductors combined with online EIS detection functionality for Fuel Cell Electrical Vehicles [C]." *Symposium de Génie Electrique (SGE 2018) Nancy, France*. Jul.2018. (Oral).

- 2 Hanqing WANG, Arnaud GAILLARD, and Daniel HISSSEL. “DC/DC converter based on SiC semiconductors combined with online EIS detection functionality for Fuel Cell Electrical Vehicles [C].” *GdR Hydrogène, Systèmes et Piles à Combustible (2018) / Grenoble, France*. May.2018. (Oral).

Symposiums

- 1 Hanqing WANG, Arnaud GAILLARD, and Daniel HISSSEL. “Efficiency and Thermal Comparison between Fuel Cell Electric Vehicle Powertrains based on Silicon or Silicon Carbide Power Converters.” *Réunion d’équipe SHARPAC de D département Energie de FEMTO-ST Belfort, France*. Jun.2017. (Oral)
- 2 Hanqing WANG, Arnaud GAILLARD, and Daniel HISSSEL. “Multi-phase Soft-Switching Interleaved Boost Converter based on SiC semiconductor and Coupled Inductor technique for Fuel Cell Electric Vehicles.” *FEMTO-ST en Séminaires Scientifique à Besançon, France*. Jun.2017. (Poster)

Titre: Etude et contrôle d'un hacheur élévateur à 6 phases entrelacées basé sur des composants SiC intégrant la fonctionnalité EIS pour véhicule électrique à pile à combustible

Mots clés: Véhicule électrique, Pile à combustible, Convertisseur DC/DC, Carbure de silicium, Spectroscopie d'impédance électrochimique, Validation HIL.

Résumé Cette thèse traite l'étude et le contrôle d'un hacheur élévateur à 6 phases entrelacées basé sur des semi-conducteurs en carbure de silicium (SiC) et des inductances couplées inverses pour véhicules électriques à pile à combustible (FCEV). L'ondulation du courant dans la pile à combustible est considérablement réduite et la durée de vie de celle-ci peut être prolongée. Les semi-conducteurs en SiC, en raison de leurs faibles pertes, permettent de meilleures performances thermiques et une fréquence de commutation plus élevée. Les volumes des composants passifs (inductances et condensateurs) sont ainsi réduits. Grâce aux inductances à couplage inverse, les pertes du noyau magnétique et du bobinage sont réduites.

La stratégie de contrôle par mode glissant est développée en raison de sa grande robustesse face aux variations de paramètres. La fonctionnalité de détection en ligne de spectroscopie d'impédance électrochimique (SIE) est intégrée avec succès à l'algorithme de contrôle par mode glissant. La validation HIL (Hardware In the Loop) en temps réel du convertisseur proposé est obtenue en implémentant la partie puissance dans le FPGA et la partie commande dans le microprocesseur du système de prototypage MicroLabBox de dSPACE. La comparaison entre la simulation hors ligne et la validation HIL a démontré le comportement dynamique du convertisseur proposé et validé la mise en œuvre du contrôle dans un contrôleur en temps réel avant de futurs tests sur un banc d'essai expérimental à échelle réduite.

Title: Design and control of a 6-phase Interleaved Boost Converter based on SiC semiconductors with EIS functionality for Fuel Cell Electric Vehicle

Keywords: Electric vehicle, Fuel cell, DC/DC converter, Silicon carbide, Electrochemical Impedance Spectroscopy, HIL validation.

Abstract: The objective of this thesis work is devoted to the design and control of a DC/DC boost converter for Fuel Cell Electric Vehicle (FCEV) application. A 6-phase Interleaved Boost Converter (IBC) based on Silicon Carbide (SiC) semiconductors and inversed coupled inductors of cyclic cascade structure is proposed. The input current ripple is reduced significantly and the lifespan of Polymer Electrolyte Membrane Fuel Cell (PEMFC) can be extended. Low power losses, good thermal performance and high switching frequency have been gained by the selected SiC-based semiconductors. The volumes of passive components (inductors and capacitors) are reduced. Thanks to the inverse coupled inductors, the core losses and copper losses are decreased and the compact magnetic component is achieved.

Sliding-Mode Control (SMC) strategy is developed due to its high robust to parameter variations. on-line Electrochemical Impedance Spectroscopy (EIS) detection functionality is successfully integrated with SMC. No additional equipment and sensor is required.

The real-time Hardware In the Loop (HIL) validation of the proposed converter is achieved by implement the power part into the FPGA and the control into the microprocessor in the MicroLabBox prototyping system from dSPACE. The comparison between off-line simulation and HIL validation demonstrated the dynamic behavior of the proposed converter and validated the implementation of the control into a real time controller before future tests on experimental test bench.