Design by Mathematics

Francois Rivet

HABILITATION À DIRIGER DES RECHERCHES

présentée à

L'UNIVERSITÉ BORDEAUX

Ecole doctorale des Sciences Physiques et de l'Ingénieur

par **François RIVET**

SPÉCIALITÉ : ÉLECTRONIQUE

DESIGN BY MATHEMATICS

Soutenue le : 27 Juin 2019

Après avis de :

M.	**Ramesh** HARJANI	Professeur	University of Minnesota	Rapporteur
	Stefan HEINEN	Professeur	RWTH Aachen University	Rapporteur
	Ricardo REIS	Professeur	Universidade Federal do Rio Grande do Sul	Rapporteur

Devant la commission d'examen formée de :

M.	**Asad** ABIDI	Professeur	University of California Los Angeles	Président
	Yann DEVAL	Professeur	Bordeaux INP	Examinateur
	Ramesh HARJANI	Professeur	University of Minnesota	Rapporteur
	Stefan HEINEN	Professeur	RWTH Aachen University	Rapporteur
	Eric KERHERVÉ	Professeur	Bordeaux INP	Examinateur
	Stefano PELLERANO	Principal Engineer	Intel Corporation	Examinateur
	Ricardo REIS	Professeur	Universidade Federal do Rio Grande do Sul	Rapporteur

”Quand les téléphones étaient attachés à un fil, les Hommes étaient libres”.

Remerciements

A ma mère qui nous a quittés trop tôt. Tu me manques chaque jour. Tu aurais été, je pense, fière de moi,
à mon père, à sa compagne, à mes soeurs et à ma famille,
à mes amis et à ma « famille australienne ».

A l'équipe Circuits And Systems,
aux docteurs Veyrac, Bouassida et Tlili,
à mes collègues du laboratoire IMS.

A l'ENSEIRB-MATMECA et Bordeaux INP,
le service des Relations Internationales,
à mes collègues et aux étudiants.

To the jury members, Asad, Ramesh, Stefan, Ricardo, Stefano and Eric,
à Yann, pour toutes ces années de complicité scientifique et d'amitié.

Contents

List of Figures

List of Tables

List of Abbreviations

5G	5th Generation
A2F	Analog to Feature converter
A2I	Analog to Information
A/D	Analog-to-Digital
AC	Alternating Current
ADC	Analog-to-Digital Converter
AI	Artificial Intelligence
AM	Amplitude Modulation
ASIC	Application-Specific Integrated Circuit
BER	Bit Error Rate
BPSK	Binary Phase Shift Keying
CAGR	Compound Annual Growth Rate
CDMA	Code Division Multiple Access
CMOS	Complementary MOS
CS	Compressed Sensing
DAC	Digital-to-analog converter
DbM	Design by Mathematics
DC	Direct Current
DFT	Discrete Fourier Transform
DR	Dynamic Range
DSP	Digital Signal Processor
DUT	Device Under Test
EDGE	Enhanced Data for GSM Evolution
ENOB	Effective Number of Bits
EVM	Error Vector Magnitude
FFT	Fast Fourier Transform
FM	Frequency Modulation
FSK	Frequency Shift Keying

GMSK	Gaussian Minimum Shift Keying
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HSDPA	High-Speed Downlink Packet Access
IBC	Intra-Body Communications
IC	Integrated Circuit
IF	Intermediate Frequency
IFFT	Inverse FFT
IoT	Internet of Things
ISSCC	International Solid-State Circuits Conference
LC-ADC	Level-Crossing ADC
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MEMS	Micro Electro Mechanical Systems
MOS	Metal Oxide Semiconductor
NSR	Noise Shaping Riemann
OFDM	Orthogonal Frequency Division Multiplexing
OSR	Over Sampling Ratio
PA	Power Amplifier
PCB	Printed Circuit Board
PLS	Post Layout Simulation
PSK	Phase Shift Keying
QPSK	Quadrature PSK
QAM	Quadrature AM
RF	Radio-Frequency
SASP	Sampled Analog Signal Processor
SDR	Software-Defined Radio
SFDR	Spurious-Free Dynamic Range
SoA	State of the Art
SR	Software Radio
SNR	Signal-to-Noise ratio
T/H	Track-and-Hold
UWB	Ultra-Wideband
WCDMA	Wideband CDMA

Introduction

"It's Difficult to Make Predictions, Especially About the Future" (Niels Bohr). For sure, the future will be more digital than the present as we all agree that the size of the digital universe will double every two years at least, to support an exponential data growth toward 2020 and beyond. Human- and machine-generated data is experiencing an overall 10x faster growth rate than traditional business data, and machine data is increasing even more rapidly at 50x the growth rate. We are ready to enter to the 5th generation of mobile communication with trillions of device connected.

Our lives are digital.

This development puts the pressure on research to satisfy more and more stringent requirements. The field of electronics, and more specifically the one of integrated circuit design is facing many challenges to support this fast evolution. My research activities at the IMS laboratory are in line with those challenges. They are focused on the design of radio-frequency (RF) systems to enhance the spectrum access, reduce the power consumption using mass market technologies. This paradigm has guided my thoughts during a decade by pioneering in RF architectures. This document summarizes my research work and is structured as follows.

Chapter 1 presents an overview of the RF transceivers design. We analyse the evolution of the telecommunication market with a focus on 5G standard. Then, a brief state of the art of RF architectures research work is presented. Finally, we introduce our Design by Mathematics methodology.

Chapter 2 details the research work in RF systems with 4 different architectures designed for Software Radio or arbitrary waveform generation purpose. All of them jeopardize the classical way of converting signals and revisit either the receiving or the transmitting chain by illustrating the concept of Design by Mathematics. Circuits have been designed and their performances have been evaluated in terms fo spectrum access, power consumption and integration cost.

Chapter 3 is focused on architectures for health applications. We present 3 aspects of research on bio-electronics, respectively a RF interface for a blood pressure sensor, a LC-ADC for ECG conversion and a study of ultrasounds propagation within the Human body. The main goal of this work is to understand how a communication system can be customized for a given application.

Chapter 4 concludes on a research project in analog circuit design for the coming years. I propose 3 directions of research: RF systems design, ad-hoc Intra-Body Communications network and analog signal processing for edge computing. Those directions are open to discussions as it foresees more or less long term activities.

CHAPTER

1

RADIO FREQUENCY TRANSCEIVERS

Sommaire

Chapter 1 presents the Radio Frequency Transceivers design facing with the evolution of standards since the last two decades. In a first part, we analyse the evolution of the telecommunication market by exhibiting figures of the exponential increase of data exchange and the need of new network to support it. A focus on 5G standard is given to provide a concrete example of our research work. In a second part, Radio-Frequency architectures research work is presented thanks to a brief state of the art to highlight directions taken by the community to tackle issues raised in the first part. Finally, we conclude on our proposed methodology to design RF transceivers based on a mathematical approach to identify the most relevant way to convert information into RF signals.

Key words: radio-frequency, telecommunications, 5G, conversion, software radio, integrated circuits, Design by Mathematics.

> "The very small value of 10^{-16} of negentropy required per bit of information plays a very important role in our modern life and it makes possible to communicate information at a negligible cost."
> Leon Brillouin, Science and Information theory, 1956, quoted by Dr. Yoan Veyrac in [2]

In the 50s, Leon Brillouin stated that modern life relies on the possibility to deal with large quantities of information for a minimal cost. In the same decade, the development of the transistor in Bell laboratories led to a physical media allowing to get closer to the theoretical cost of information described by Brillouin. Since then, the electronic industry followed the Moore's law by developing standalone devices that can exchange billions of bits per second for various applications that are now the backbone of our society and to some extent of our civilization. However, conventional transceiver architectures cannot support the pressure of the exponential increase of exchanged digital information while satisfying customer expectations in terms of quality of service, device cost and battery life.

RF designers are faced to technological issues such as collecting data, converting them into digital, processing them and transporting them along heterogenous network. Conversion and transport are the key of the system when hardware is concerned. Brillouin statement is challenging us on the efficiency of data exchange by lowering its cost in terms of power consumption, device price, and spectrum ressources. This chapter introduces the trade-off of wireless circuit design and proposes research directions.

1.1 Wireless Communications Challenges

Mass market radio-frequency (RF) transceivers have emerged during the 90's with GSM as the technology driver. Since then, we can observe a continuous evolution of demand to design products wireless systems which either integrate more and more applications at the lowest price or answer specific needs such as Internet of Things (IoT). This constant growth can be seen in the mobile data traffic forecast presented in Fig. 1.1. It will be mainly supported by the 5th Generation (5G) mobile technology.

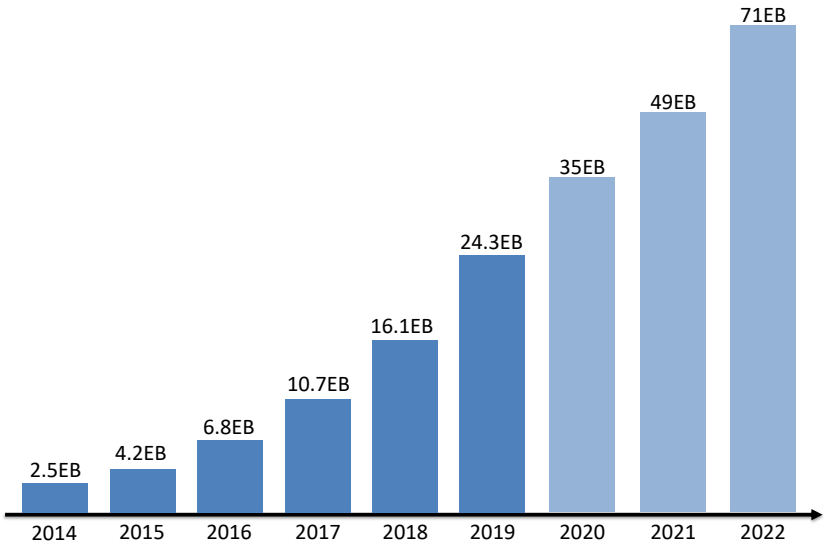


Figure 1.1 – Exabytes per month. Cisco VNI: Global Mobile Data Traffic Forecast Update 2016-2022. February 2017

What is 5G ? It is said to be disruptive compared to the previous mobile networks. The change is evident but it is too soon to know what the future may hold. Analysts are projecting the expected results from 5G technology even if at this day, deployments are just beginning and commercial 5G deployment is clearly on the horizon:

— 5 Billion people forecast to be accessing the internet via mobile by 2025,
— 5G coverage will roll out rapidly to cover more than 40 percent of the global population by 2025,
— 5G will account for almost 1 in 7 connections (14 percent) by 2025,
— 9 Billion mobile connections with 5.9 Billion unique subscribers in 2025,
— 25 Billion Internet of Things devices globally in 2025,
— Global Mobile Annual Revenue of 1.1 Trillion in 2025.

The transformation to 5G will also transform everyone lives, our economy, our jobs and our industries. The early signs are beginning to show, such as wearables with self-contained mobile computing devices (Apple Watch or connected glasses), the connected car (autonomous vehicles), the healthcare system (remote monitoring and robotic surgery), drones (used for transportation and surveillance) and finally robots and Artificial Intelligence (AI) will result in a new relationship for both humans and machines.

The wireless industry has its game to play by providing new mega-networks of connecting billions of things, billions of connected people with a major shift in network operations and management. For instance by 2023, more than 30 billion connected devices are forecast with 2 main observations:

— Mobile video traffic is forecast to grow by around 50 percent annually through 2023, when it should account for nearly three-quarters of all mobile data traffic (Fig 1.2). Social networking is forecast to grow by 34 percent annually over the coming six years. The trend is accentuated by the growing use of embedded video in social media and web pages, which is considered video traffic in this context, fueled by larger device screens, higher resolution and new platforms supporting live streaming.

— 20 billion of the 30 billions of devices will be related to the IoT. Connected devices include connected cars, machines, meters, sensors, point-of-sale terminals, consumer electronics and wearables. Between 2017 and 2023, connected IoT devices are expected to increase at a Compound Annual Growth Rate (CAGR) of 19 percent, driven by new use cases and affordability.

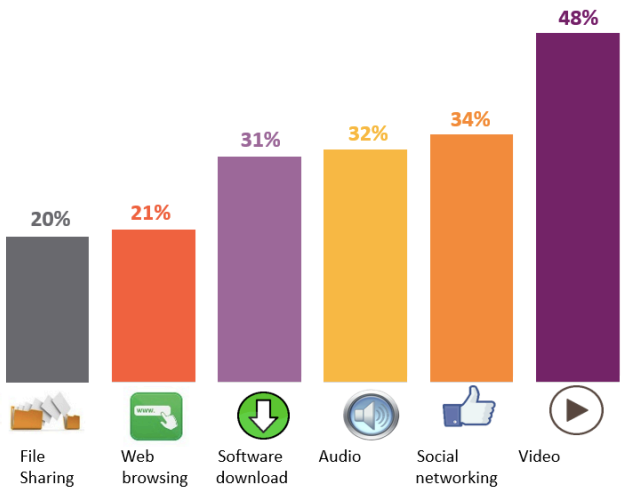


Figure 1.2 – Mobile Traffic by Application Category - CAGR 2017-2023 - Ericsson Mobility Report, November 2017

The 5G infrastructures would rely on an heterogeneous, densified network. As for frequency resources, 5G is expected to use as much spectrum as possible, divided into 3 main frequency ranges for different applications (Fig. 1.3):

— Sub-6 GHz band: this frequency range offers less losses for a transmission in the air; a data rate higher than 1 Gbps can be achieved on this band thanks to carrier aggregation, based on an extension of the LTE standard (cf. Fig. 1.4),

— The mmW band: it has a limited range because of attenuation but gives access to wider bandwidths,

— The Internet of Things (IoT): it will be deployed in the same time, using the sub-GHz frequency band. Those devices will be equipped with low-power transceivers.

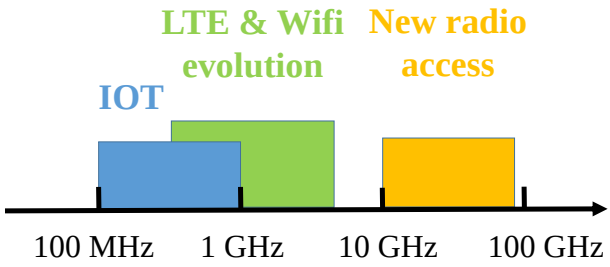


Figure 1.3 – Technology tracks of 5G era

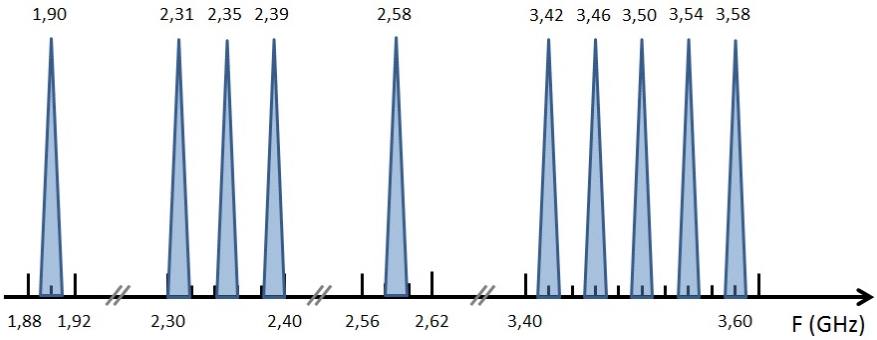


Figure 1.4 – Spectrum allocation for sub-6GHz 5G standard

RF Transceivers are the hardware implementation of those various techniques to access the spectrum. It necessitates a high flexibility as the demand of spectrum access is large in terms of frequency ranges and number of users. For instance, sub-6GHz claim for a carrier-aggregated signal which cover frequencies from 1.8GHz up to 3.6GHz and then 6GHz.

As depicted in Fig 1.5, RF Transceivers design is thus more and more constrained by:

- **Power consumption**: mobile handsets are limited by their battery and as a matter of consequence, the power consumption has to be as low as possible with the highest efficiency
- **Data rate**: as data traffic is increased mainly by video applications, data rate is getting higher (from 10x to 100x from one generation mobile communication to another) and asks for higher carrier frequencies, not necessarily compatible with an efficient propagation (mmW frequencies)
- **Technology**: mass market imposes the use of a low cost technology, such as CMOS. Nevertheless, this technology is not suited for analog RF electronics.
- **Propagation environment**: wireless signal propagate more or less depending of the environment and their frequencies. The air is very a good medium for sub-6GHz signals in a non-dense area. New challenges are raised by mmW frequencies in dense area (such as urban) or new propagation media such as human body.

Our research work is to design radio-frequency integrated circuits to challenge this paradigm.

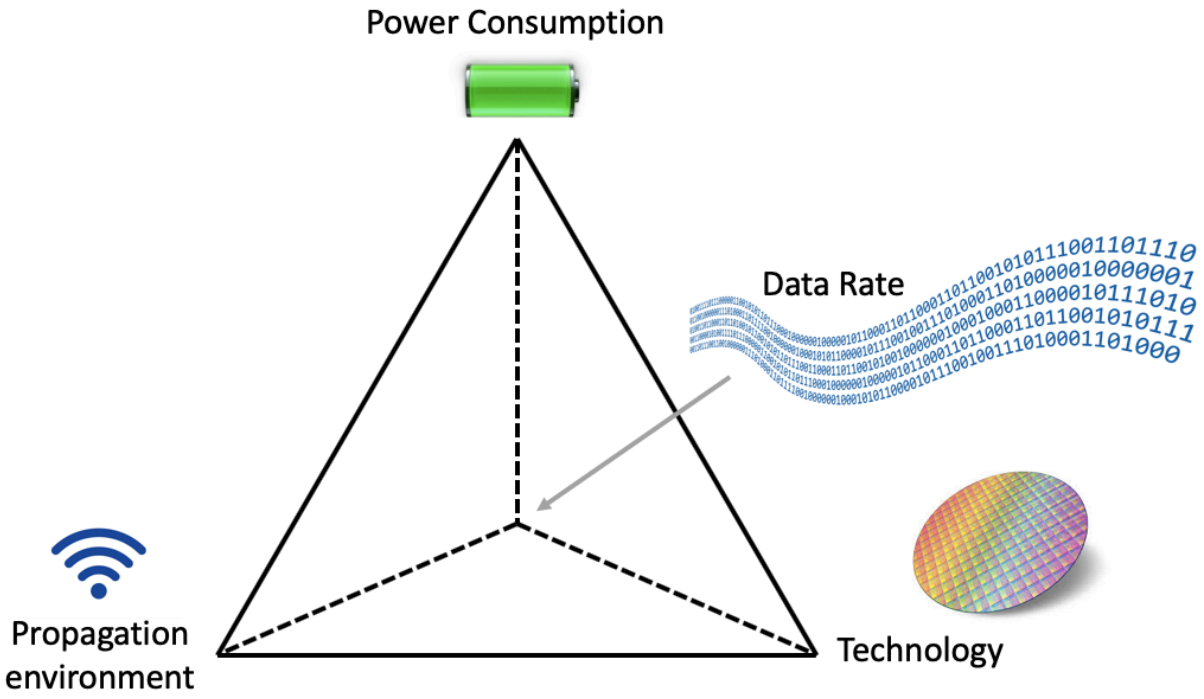


Figure 1.5 – Paradigm of RF Transceivers design

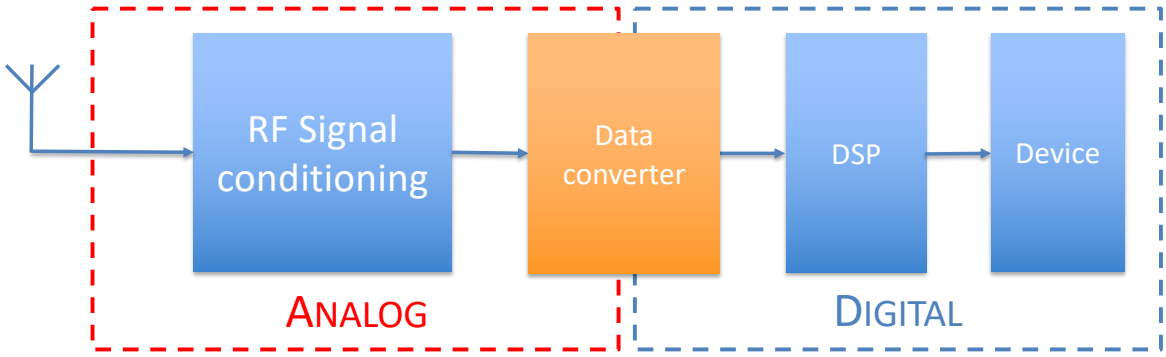


Figure 1.6 – Transceiver Architecture

A wireless communication system transmits and receives information at high frequencies. Fig. 1.6 summarizes the transceiver architecture with 3 main parts:

- RF signal conditioning: RF signals are amplified, filtered and up or down-converted into baseband,
- Data converter: signals are converted from analog to digital or digital to analog,
- Digital signal processing: the signal is processed digitally to recover the information contained in the data stream to be displayed by the device.

Our research aim is to adapt or invent techniques to design transceivers for new wireless communication protocols. We have to deal with CMOS technologies, high frequencies and data rate, low power consumption and system integration.

1.2 Radio-Frequency architecture

RF architectures have to challenge the evolution of wireless transmission requirements as presented before. Since 20 years, a lot of researches are oriented in the direction of RF flexible solutions. Many terms are associated to those architectures, such as multi-standards, Software Defined Radio (SDR), Software Radio (SR), Cognitive Radio, adaptative radio with an updated terminology now including artificial intelligence in adaptative RF front-end design.

Fig 1.6 illustrates how a transmitter architecture can gain in flexibility. Digital conversion is brought as close as possible to the antenna to alleviate reconfigurability or adaptative RF signal processing. Nevertheless, the analog front-end is struggling with RF requirements over a wider band of operation. This depicts the technological bottleneck of the analog-to-digital conversion the scientific community is fighting against. Boris Murmann's ADC Performance Survey keeps an updated trend of ADC or DAC evolution

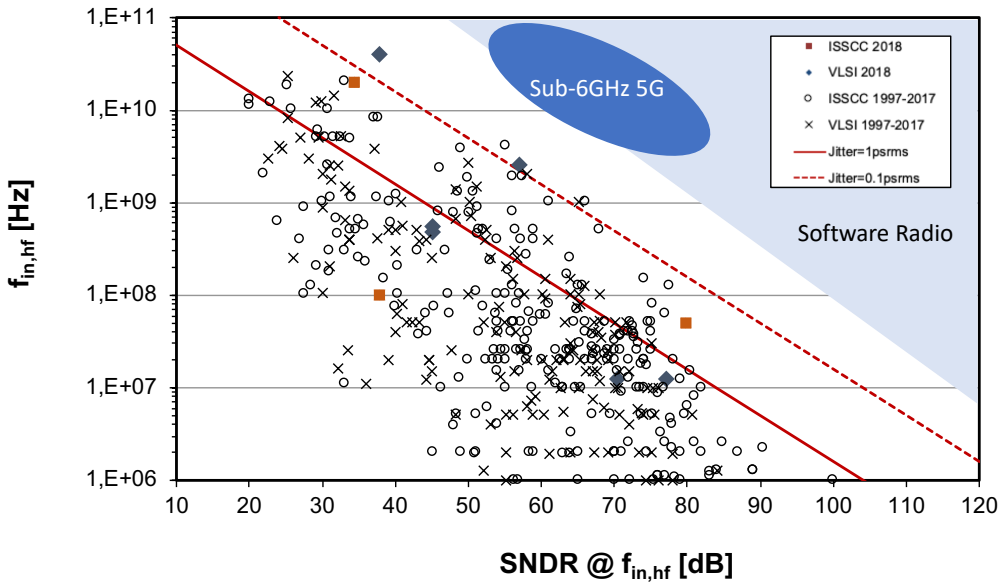


Figure 1.7 – Boris Murmann's ADC Performance Survey [1]

over the 2 last decades and shows clearly that a universal ADC or DAC for RF applications is not for today or tomorrow. Fig 1.7 presents how challenging could be an ADC for either SDR or sub-6GHz 5G applications. There is clearly a wall to break and recent evolution cannot fight against physics where aperture time is struggling with the jitter. That is why, research is focused on proposing solutions at the system level instead of keeping on running to the wall.

1.2.1 State of the Art

Some researches provides solutions at the system level, either for the receiving or the transmitting path. The philosophy is to give flexibility at a RF system while respecting RF requirements:

— High-order modulation scheme,
— Large frequency range or wide-band,
— High resolution requirements (Signal-to-Noise Ratio (SNR)),
— Low latency.

Receivers trends

RF receiver state of the art depicts a wide range of research on new RF receivers. The following one is not exhaustive but presents a selection of circuits that highlight some interesting features. They all achieve good performance in terms of Dynamic Range (DR) or rejection, power consumption but exhibit how to challenge limited instantaneous bandwidth and concurrent reception (i.e. their potential to perform

	Nauta [3]	Kinget [4]	Pamarti [5]	Abidi [6]	Andrews [7]	Harjani [8]
Tuning range	0.1-1GHz	0.2-1GHz	0.1-1GHz	0.08-2.7GHz	0.1-2.4GHz	0-2.5GHz
Instantaneous Bandwidth	35MHz	2MHz	2.5-40MHz			312.5MHz
Gain / Rejection	NA / 70dB	36dB / 52dB	23dB / 45dB	72dB/42dB	40-70dB/-	47dB
Power Consumption (mA)	1.6 to 13	26		27	31	0.76
Technology	65nm	65nm	65nm	40nm	65nm	65nm

Table 1.1 – RF receiver State of the Art

a direct carrier aggregation). Nevertheless, ideas presented by the state of the art in Tab. 1.1 pave the way to revamped approach such as N-path filters [3] [4], time-interleaved (i.e. convolution) [5], noise cancellation [6], digitally assisted systems [7] or analog signal processing [8]. We can detail 2 approaches of interest:

— Prof. Bram Nauta proposes in [3] to achieve filtering thanks to N-path filter. Despite this technique is not new, he was a pioneer to integrate it in a RF Front End. He demonstrated that we can reach very good performances such as selecting a narrow channel within a wide frequency range with a good selectivity. His work inspired many researchers and was a starting point to several improvements at the system level to enhance it as depicted by Prof. Peter Kinget in [4] and by Prof. Bram Nauta himself in [9],

— Prof. Ramesh Harjani proposes in [8] a disruptive system to select several bands in a wide range of frequency using analog signal processing thanks to a discrete Fourier Transform. This approach has demonstrated a low power and highly linear application which is well suited to RF. This work has been improved by being integrated in a receiver to sense a wide spectrum and to perform beamforming [10].

Transmitters trends

Tab. 1.2 presents a selected state of the art of transmitters that aim at achieving software radio purpose. It follows the various type of architectures in function of their flexibility as depicted in Fig. 1.8 extracted from [2]. A multi-standard transmitter detailed in [11], [12] and [13] plays on direct conversion with a carrier frequency configuration. [14] exposes a SDR transmitter supporting intra-band dual carrier aggregated signals. The trend is to generate several bands in parallel and counteract inter-modulation products by harmonics rejection techniques. Amplification itself is still a main technological bottleneck if one considers it targets wide band with high efficiency in CMOS technologies.

	Craninckx [12]	Sakamoto [11]	Hashemi [13]	Wang [14]
Tuning range	0.15-6GHz	0.7-2.7GHz	0.05-6GHz	0.1-6GHz
Bandwidth	16MHz	20MHz	40MHz	100MHz
Power Consumption (mW)	100	200	900	103
Technology	130nm	90nm	130nm	65nm

Table 1.2 – RF transmitter State of the Art

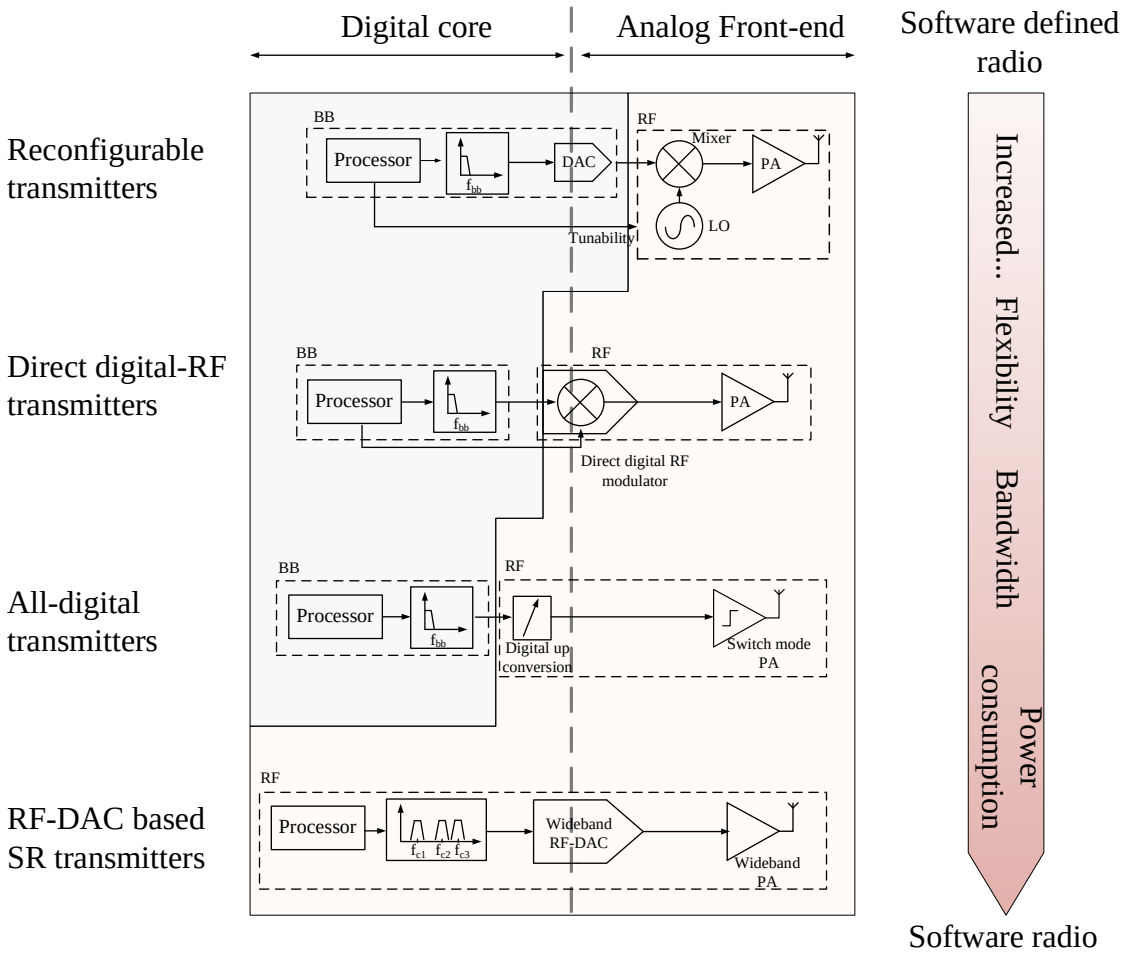


Figure 1.8 – Transmitter digital versus analog composition for flexible RF applications

1.2.2 RF Transceiver design

Going digital at the earliest possible stage is no more the trend. Designing a RF transceiver is first to face with many circuits such as Power Amplifiers, Oscillators, Filters, Clocks, Analog-to-Digital and Digital-to-Analog Converters, Modulators (Amplitude, Phase, Frequency Modulation), Demodulators, Mixers, PLL, Multiplexers, etc... As said before, it becomes very complex to consider a complete paradigm between power, frequency, cost and bandwidth with such a diversity of standards. Software Radio is not necessarily the grail to get. We believe that RF designers have still their role to play to propose the most suited circuit for each application. The grail might not be the circuit but the methodology to design it.

When considering the RF system in its whole, we can identify a trade-off in RF circuit design. Fig. 1.9 illustrates the compromise between classical RF architectures and the general purpose one:

— Classical RF architectures: they use well-known techniques such as homodyne, heterodyne, super-heterodyne architecture. RF designers work actively to integrate the FE efficiently with the most relevant technology. The methodology is limited in terms of risks but the architecture is not necessarily optimized for power consumption, die area or over-loaded in calibration apparatus,

— General purpose RF architecture: it is the ultimate Software Radio system but we can consider that intermediate SDR systems can be included in. RF constraints are relaxed to the price of intensive digital signal processing and A/D conversion cost. The system is not optimized for power consumption and signal processing efficiency.

We envision a trade-off between classical and general purpose RF architectures. The most relevant one is a full custom RF architecture based on the wireless application. It will determine the power consumption budget, the standard (i.e. modulation), the frequency range, the bandwidth and all the inherent RF requirements. The underlying goal is to integrate Compressed Sensing (CS) as a matter to receive or transmit only the relevant information directly at the RF stage to avoid waste of power and time due to complex signal analysis.

The concept of "relevant information" is about to convert only signal information rather than its full representation. Under these conditions, Nyquist rate sampling may no longer offer the optimal digitization scheme. The trend is to reduce the sampling bandwidth as closely as possible to the signal's information rate while the new class of feature-sampling ADCs called Analog to Information (A2I) converter or Analog to Feature converter (A2F) reduce the dimensionality of the waveform through analog analytics to retain only application relevant signal features, with the intention of classifying these features instead of representing the original waveform.

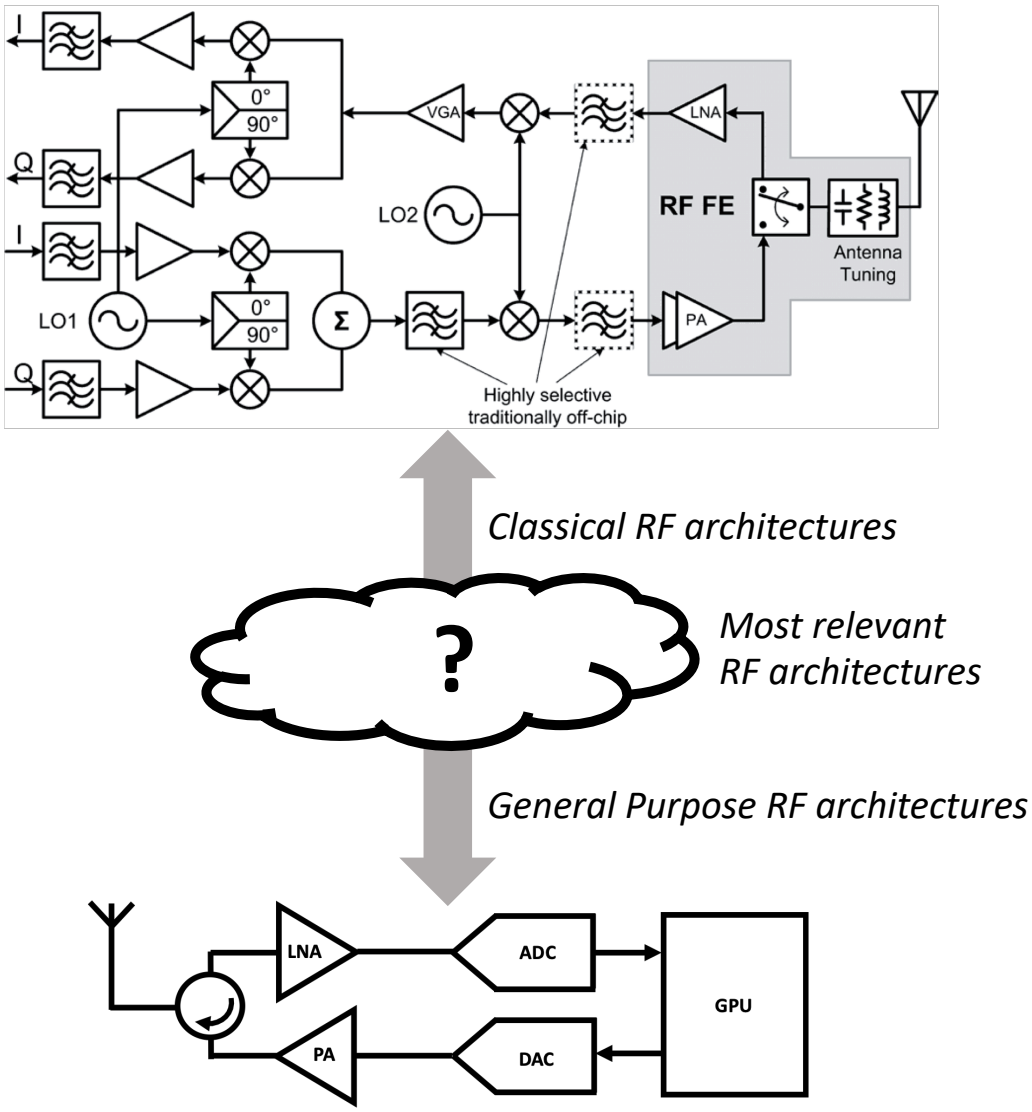


Figure 1.9 – Representation of trade-off between classical and general purpose RF architectures

Our design methodology is called **Design by Mathematics (DbM)**. It is divided into 2 parts:

1. A holistic consideration of the circuit:
   — IEEE standard (frequency range, bandwidth, modulation scheme, etc ...),
   — wireless propagation medium and its properties (attenuation, distance).
2. The signal is converted in the most adequate mathematical base, ideally orthonormal:
   — the base is the analog Front End,
   — only coefficients are converted and projected in the base.

Fig. 1.10 presents the differences between a classical and the DbM approaches in the case of 5G and SDR-like transceivers:

— Wide-band RFFE are similar in both approaches,
— The conversion circuitry is no more a multiple carrier up/down converter but a base implemented in silicon in which coefficients are projected. The frequency generator can be seen as the family generator in the mathematical meaning,
— Data are no more considered as a digital signal but as information encoded or decoded in coefficients extracted from or converted in a RF signal thanks to the base.

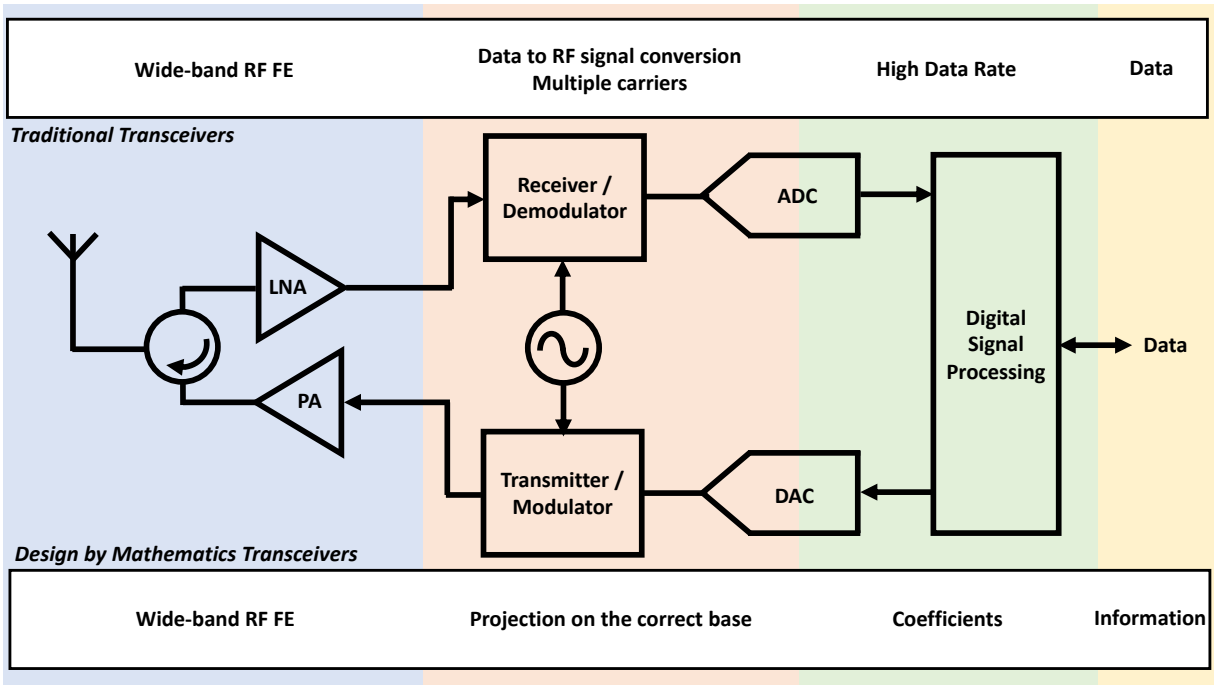


Figure 1.10 – Transceivers architecture difference between traditional and DbM approaches

The base is the key to choose the most adequate circuitry. Mathematically: it should be orthonormal and build by a family provided by the frequency generator. Following algebra rules, we need to define Odd signals O(x) and Even signals E(x) with a scalar product to orthonormalize the base. Then, we have to demonstrate the density and verify the Dirichlet theorems to ensure that any “pseudo” periodic function can be written as the limit of a sum of O(x) and E(x). This will be the confirmation that any RF signal can be generated using this base. Thus, the base can be implemented in silicon and RF signals will be converted only thanks to their coefficients.

1.3 Conclusion

Telecommunication industry claims for new RF architectures. It is faced with a huge diversity of standards and a constant evolution that impose a design of new RFIC. A decade ago, a concept called Software Radio was said to be the grail to reach by proposing a universal circuit to access to large band of the RF spectrum by moving to digital all the flexibility. This concept arrived to a dead end. The upcoming 5G standard pushes RF designers to develop wide band, low power, high resolution architectures. The boom of IoT strives RF designers to develop ultra low-power RF circuits. Last but not least, new trends such as Intra-Body Communications and up-100GHz spectrum access also push RF designers to develop new RF architectures.

In this chapter, we have discussed about the relevancy of **RF architecture design**, from its classical way to the SR one. We assume that there is a trade-off between frequency, either the carrier or the bandwidth, the power consumption, the technology and the resolution to design the most relevant architecture. A/D and D/A conversion is still the technological bottleneck to counteract because it cannot support the increasing amount of data, either on the RF or on the digital signal processing sides, or the limited power at its disposal to be performed.

This is why we propose to revisit the design methodology of RF circuits by introducing the **Design by Mathematics approach**. It consists in considering the conversion from baseband to RF in the projection of coefficients in an orthonormal base. The RF circuit is the orthonormal base and the coefficients represent the information. Each application will find the most relevant pair of bases and coefficients, which will give the most appropriate circuit displaying the **best performance at the least cost**.

CHAPTER

2 DESIGN BY MATHEMATICS FOR RADIO-FREQUENCY IC

Sommaire

Chapter 2 presents the research led in RF systems during the last decade. It started as an investigation focused on Software Radio receiver. Then, it was extended to arbitrary waveform generation. 4 kind of architectures were proposed and divide into 2 families: frequency domain and time domain ones. Each of it proposes a receiver and a transmitter solution. We have evaluated their efficiency in terms of spectrum access, power consumption and integration cost. The first family is about Fourier transform: the receiver implements a Discrete Fourier Transform using analog voltage samples to carry out an instantaneous image of the RF spectrum. The transmitter is based on a "digital" Fourier transform using Walsh series in order to investigate on the best trade-off between analog and digital to generate amplified wide-band signals. The second family is a time domain solution based on derivatives and integrals of a RF signal. The transmitter, called Riemann Pump, proposes to discretize the integral of a signal by encoding it thanks to a high-data rate digital stream. The receiver is about to shape the quantification noise using a feedback loop, called Delta Riemann, to display a direct RF conversion of a signal.

Key words: Sampled Analog Signal Processing, Walsh series, Software Radio, Arbitrary Waveform Generator, Carrier Aggregation

2.1 Design by Mathematics principles

A RF signal is by nature a sine-wave that varies in amplitude, frequency and phase in time. This sine-wave is modulated to carry information. It is done by changing its amplitude, its frequency or its phase thank to slow variations compared to the sine-wave one. Assuming that, we consider that only the envelope carries information and the carrier is useless to convert information to radio-frequency.

In mathematics, an algebra over a field (simply called an algebra) is a vector space equipped with a bilinear product. Thus, an algebra is an algebraic structure, which consists of a set, together with operations of multiplication, addition, and scalar multiplication by elements of the underlying field, and satisfies the axioms implied by "vector space" and "bilinear". We consider that RF signal and signal processing is an algebra. The vector space is the RF transceiver.

A vector space is a collection of objects called vectors, which may be added together and multiplied by numbers, called scalars. An orthonormal family of vector forms a base. With given properties, this base can describe pseudo-periodic RF signals. Scalars are then called coefficients.

We propose a methodology to convert RF signals to base-band by representing it in the most adapted base thanks to a set of coefficients. In electronics, we consider that those coefficients carry the information and the base is the mean of conversion from RF to base-band.Fig. 2.1 depicts how Tx can generate a signal based on coefficients conversion in a base or how Rx can project RF signal in a base and recover coefficients.

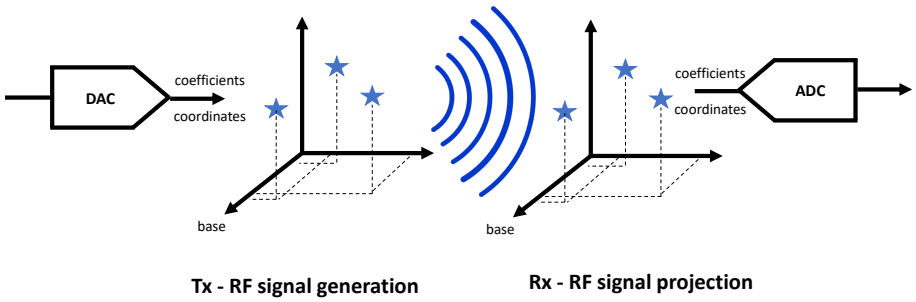


Figure 2.1 – Symbolic representation of the DbM methology

We can identify some relations between the mathematical description of a RF signal and its RF properties. It can be listed as follows:

— density: it is the accuracy of the signal description based on the size of the base and its ability to represent any kind of functions. It will play on the bandwidth, i.e. the wide-band capability,
— coefficient quantification: coefficients are converted from digital to analog. Their resolution will play on properties such as SNR, SFDR, BER.

The 2 following sections present 4 kind of circuits developed during the last decade as a research prospective. They are divided in 2 categories: frequency domain and time domain, and each one presents a transmitter and a receiver. Each solution is detailed by:

— its concept,
— its architecture,
— its simulation,
— its measurements,
— its perspectives.

2.2 Frequency domain

2.2.1 Sampled Analog Signal Processor Receiver - SASP Rx

This work was initiated in the trend of Software Radio receivers and was the subject of my PhD thesis. The objective was to design and measure a Sampled Analog Signal Processor (SASP). Its purpose is to carry out analog operations on discrete voltage samples at RF frequencies. My idea was to relax ADC constraints and coherently the DSP constraints by decreasing their working frequency as it was and it is still the main technological bottleneck as both resolution, power consumption and large bandwidth cannot be achieved at the same time.

We have proposed to interface the antenna and the A/D conversion with an analog signal processor (cf. Fig. 2.2). Its goal was to work in the frequency domain at RF frequencies to perform operations in the frequency domain instead of the time domain. Those operations are much easier and thus, less costly (filtering, mixing, carrier aggregation, ...).

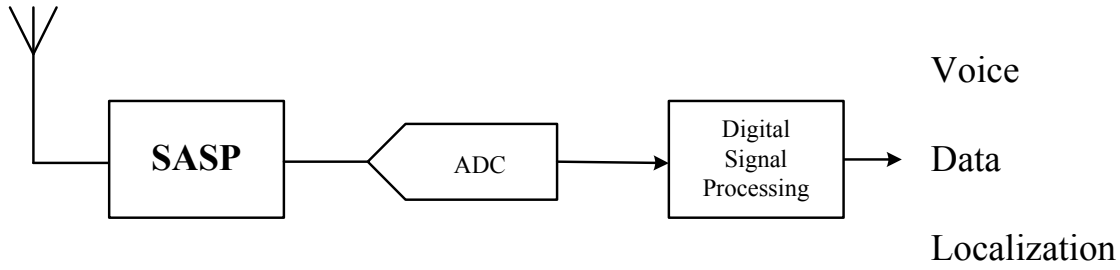


Figure 2.2 – SASP receiver system

Concept

Every sampled signal can be expressed using Fourier coefficients by Eq. 2.1.

$$x(k) = \sum_{n=-\infty}^{+\infty} c_n(f).\exp\left(jnk\frac{2\pi}{T}\right) \tag{2.1}$$

The SASP processes an analog Discrete Fourier Transform (DFT). Output carries out the Fourier coefficients that compose the input signal as described in Eq. 2.2.

$$X(n_{\text{sample}}) = \sum_{k=0}^{N-1} x(k)\exp\left(\frac{-j2\pi n_{\text{sample}}k}{N}\right), \qquad n_{\text{sample}} = 0,1,\cdots,N-1 \tag{2.2}$$

The SASP works as follows (Fig. 2.3):

— RF signals are sampled,

— Voltage samples carries out analog FFT,

— Among thousands of them, only the ones representing the desired RF signal envelope are selected,

— Selected voltage samples represent the instantaneous in-band cartesian coordinates of signal envelope.

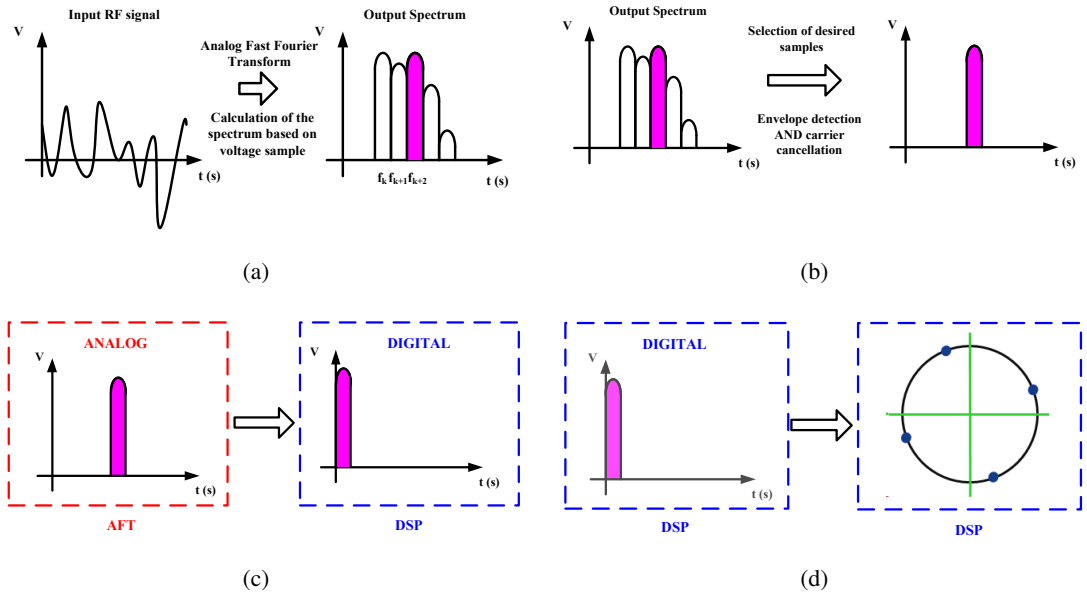


Figure 2.3 – Concept of the SASP, analog FFT (a), sample selection (b), A/D conversion (c), constellation processing (d)

The SASP emphasizes two applications:

— The frequency demodulation: as only the sample contains both phase and amplitude information, a direct demodulation of the constellation can be performed [15],

— A native carrier aggregation: the sample selection is not limited to one sample and several samples, i.e. channels, can be processed at the same time.

Architecture

We have designed a generic architecture to implement the FFT algorithm on a given number of samples N. Sampling frequency f_s is the only parameter to scale FFT accuracy and range. We limit our study to $N = 64$ voltage samples, i.e. three stages of analog calculation (Fig. 2.4). This architecture was sufficient to demonstrate the feasibility, the application and the technological limitations. High level simulation results have been published in [16] [17] [18] [19] [20].

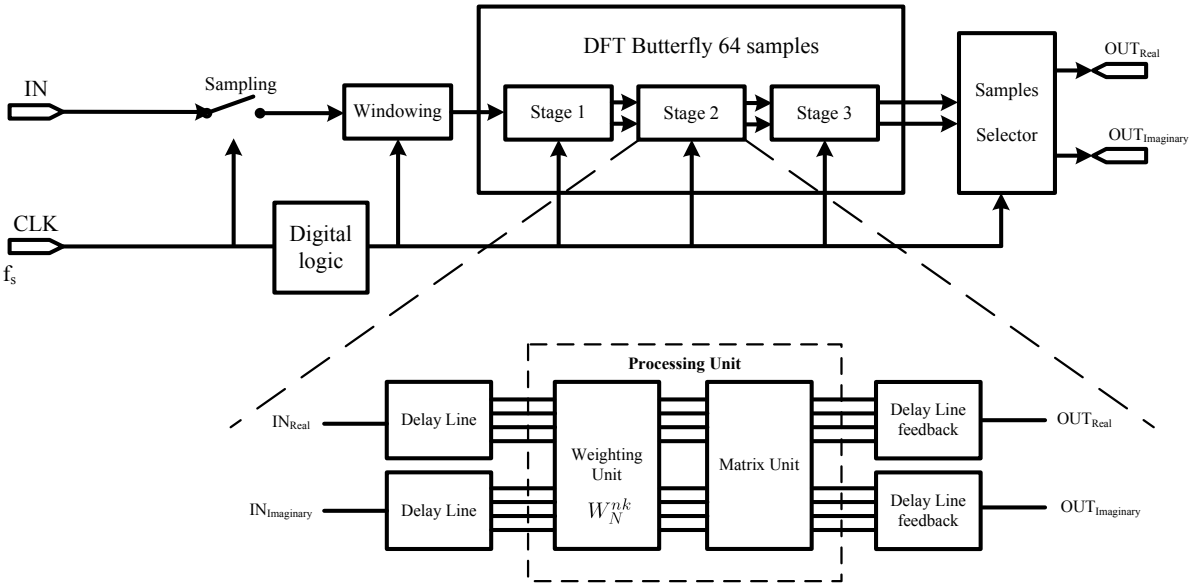


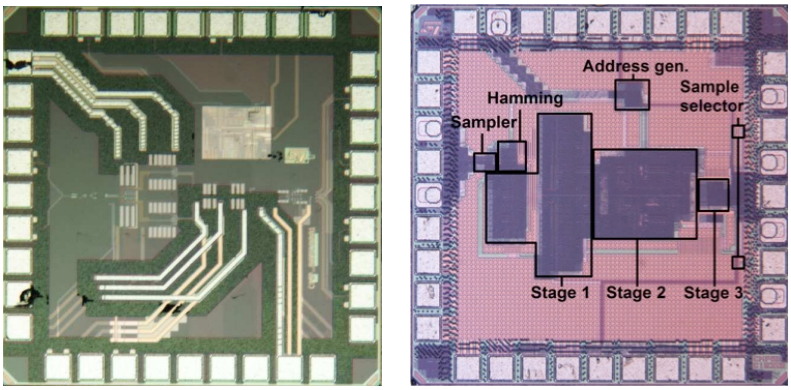
Figure 2.4 – SASP Architecture

The demonstration has exhibited main constraints in analog signal processing building blocks such as:

- The Track and Hold (T/H) sampler: it samples the signal and transfers the voltage samples to the FFT circuit. Sampling is the most important part of the system because the resolution of the calculation depends on its accuracy,
- Windowing: the range of the data processing is limited by the number of stored samples N and has an undesired effect on the spectrum. This effect is reduced thanks to a weighting function called *window*, here a Hamming window which was hard-wired but would be reprogrammable for more flexibility,
- Analog operations: delaying, adding and weighting operations on voltage samples bring inaccuracy such as:
  - Delay suffers from leakage in storing capacitors,
  - Adding and weighting suffers from distortion because of voltage-to-current conversion.

Measurements

Two demonstrators of the SASP were fabricated respectively in 2008 and 2013. They were using the 65nm CMOS technology from STMicroelectronics. Their die area was pad limited to $1.44mm^2$ with an active area of $0.13mm^2$ (Fig. 2.5). The circuits have been fully characterized and their main characteristics are given by Table 2.1.



(a) (b)

Figure 2.5 – Frequency demodulation, SASPEPA-2008 (a), NIKITA-2013 (b)

Characteristics	SASPEPA	NIKITA
Technology	65nm CMOS STM	65nm CMOS STM
Die area	$1.44mm^2$	$1.44mm^2$
Maximal f_s	1 GHz	2 GHz
RF spectrum covered	0-500 MHz	0-6 GHz
Instantaneous BW	0-500 MHz	0-1 GHz
Power consumption	360mW	97mW

Table 2.1 – SASP performances

Measurements have demonstrated that frequency demodulation can performed using:

— Frequency Modulation (FM): defined by a frequency deviation of $f_{deviation} = 1kHz$ around a central frequency of $f_{carrier} = 160.001MHz$ (Fig. 2.6(a)). f_{out} varies a frequency range from 0 to $2kHz$,

— BPSK modulation: bits are encoded through a phase shift of 180° with a bit rate of $1Mbps$. The output samples representing a '0' are reversed compared to a '1', thus we can read directly bits (Fig. 2.6(b)),

— 2-level Frequency Shift Keying (FSK) modulation: bits are encoded at 2 different frequencies $f_1 = 160.002MHz$ and $f_2 = 160MHz$ with a bit rate of $1ksps$. '1' is a $2kHz$-signal and '0' is a DC signal (Fig. 2.6(c))

— Amplitude Shift Keying (ASK): either the signal is the RF signal or a zero-signal to encode bits with a $1kHz$-data rate ASK signal (Fig. 2.6(d)).

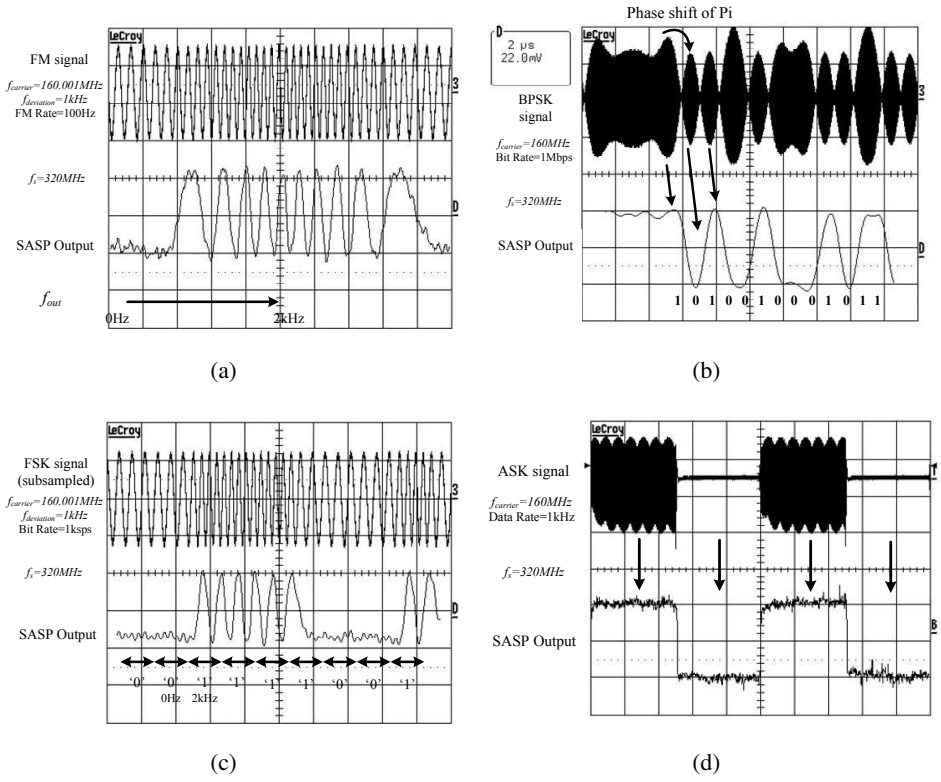


Figure 2.6 – Frequency demodulation, FM modulation (a), BPSK modulation (b), FSK modulation (c), ASK modulation (d)

Fig. 2.7 presents the principle and the measurement of a concurrent reception which is applied to carrier aggregation. A 2-frequencies signal is carried out by samples $n_s = 28$ and $n_s = 30$. We can notice interferences in samples $n_s = 27$, $n_s = 29$ and $n_s = 31$ due to the input windowing. All the others samples are null. Measurements results have been published in [21] [22] [23] [24].

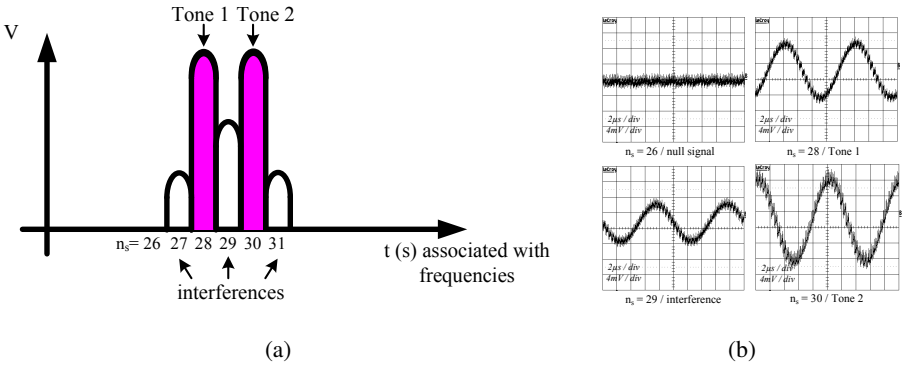
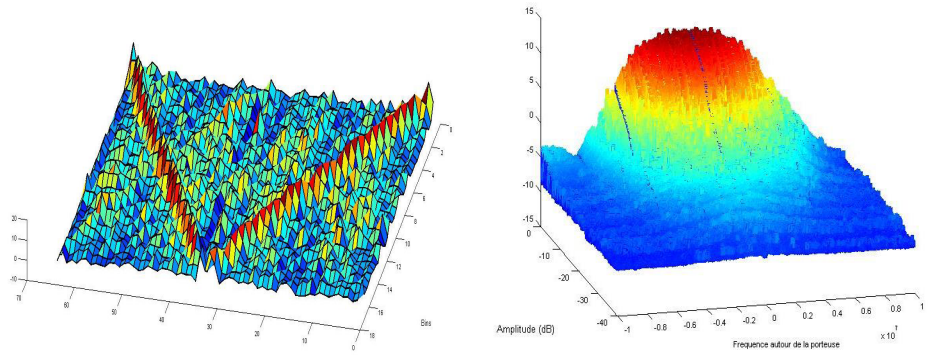


Figure 2.7 – Concurrent reception, principle (a), measurements (b)

Fig. 2.8 presents the complete characterization of bins and in a bin in particular. It was measured using millions of sets thanks to an automatic bench developed for this purpose. It validates the correct addressing and behavior of every bin. It was completed with a characterization in temperature (Fig. 2.9). As one can see, SNR decreases with temperature increasing.



(a) (b)

Figure 2.8 – Characterisation of a bin, addressing of all bins (a), frequency behavior in a bin (b)

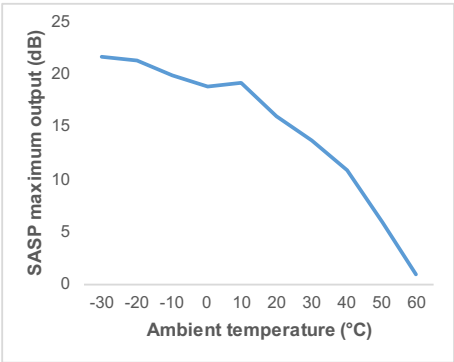


Figure 2.9 – SASP characterization in temperature

Perspectives

At this day, we can identify several research works in the line of this one such as [8] and [10] used as systems for instantaneous reception of signal within very large bands.

The work has been pursed with 2 applied scenarii:

— Civil applications: ST Microelectronics has kept financing the investigations on the SASP performances improvements. 5G is a standard that requires carrier aggregation. The SASP can receive several channel at the same time within large bandwidth [25]. Some improvement works on the design of the circuitry have been done to optimize the signal processing [26],

— Defense applications: Thales Group has financed research work on RADAR application. [27] [28] [29] [30] present the principle of a frequency detection for this purpose. The goal is to cancel any interfering signal from 0 to 20GHz+ frequencies, i.e. to localize a signal, identify its frequency, its magnitude and its modulation scheme as quickly as possible. Analog signal processing is the relevant answer to low-latency systems as no-conversion and digital signal processing are avoided to waste time.

2.2.2 Walsh Transmitter - Walsh Tx

This work was initiated in the trend of Software Radio transmitters and was the subject of Dr Nassim Bouassida's PhD thesis [31]. The objective was to propose a new type of RF transmitter with very wide band capabilities such as carrier aggregation purpose.

Concept

The spectral representation of a signal is a sum of harmonics. Thus, one can think that a sum of harmonics can generate arbitrary waveforms. For instance, 3 harmonics are sufficient to approximate a square wave as depicted in Fig 2.10. Nevertheless, this is hardly feasible in RFIC, such as proposed in Fig. 2.11, because it would consume a lot of power, surface and would face with various parasitic effects. However, we thought that a square signal also has a fundamental harmonic and odd harmonics. In integrated circuits, square signals are relatively straightforward to manage. We decided to investigate on how to generate a RF signal based on a square signals generation.

Joseph Walsh has proposed a base of square signals to describe any pseudo-periodic signals. This theory is described in [32]. It is based on Walsh series that are discrete trigonometric functions. It is generated following an iterative pattern given by Eq. 2.3 where $W_0 = 1$ and n is the order of Walsh.

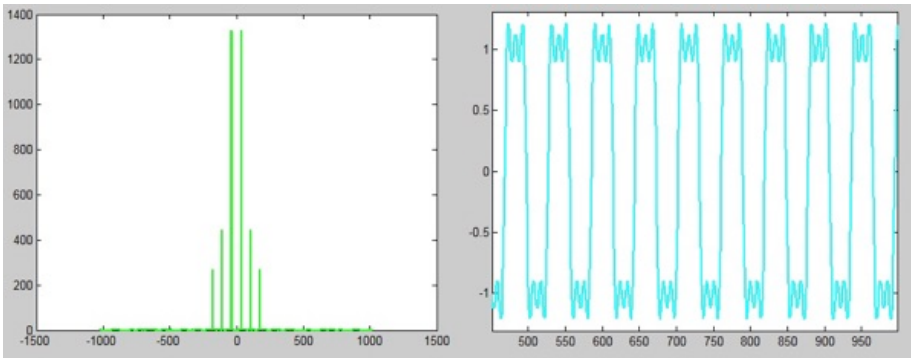


Figure 2.10 – square signal generated with 3 harmonics

$$W_n = \begin{pmatrix} W_{n-1} & -W_{n-1} \\ W_{n-1} & W_{n-1} \end{pmatrix} \tag{2.3}$$

Square signals sequences are given by each line of the matrix. We can represents those sequences in time with every line corresponding to a Walsh function. Those functions are named $Wal(i)$, with $i = 0 \ldots 2^{Order_{Walsh}}$. They are orthonormal and can be splitted into 2 kinds, *Cal* and *Sal*, representing the cosinus and the sinus for Walsh functions. Thus, we can describe any signal under its Walsh form based Eq. 2.4. a_n and b_n are the coefficients. Those coefficients represent the signal and are consequently refreshed no more than the envelope frequency, i.e. the data rate.

$$x(t) = Wal(0) + \sum_{n=1}^{N} a_n.Cal(n,t) + b_n.Sal(n,t) \tag{2.4}$$

with $N = \frac{Order_{Walsh}}{2}$.

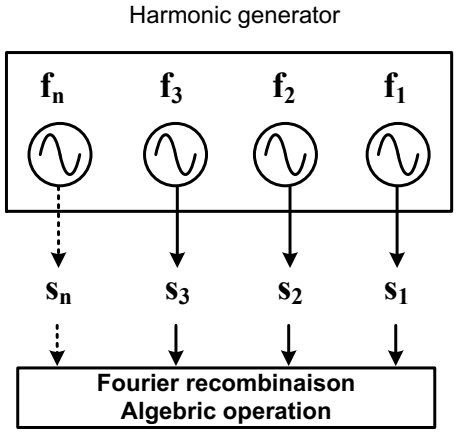


Figure 2.11 – Harmonics recombination

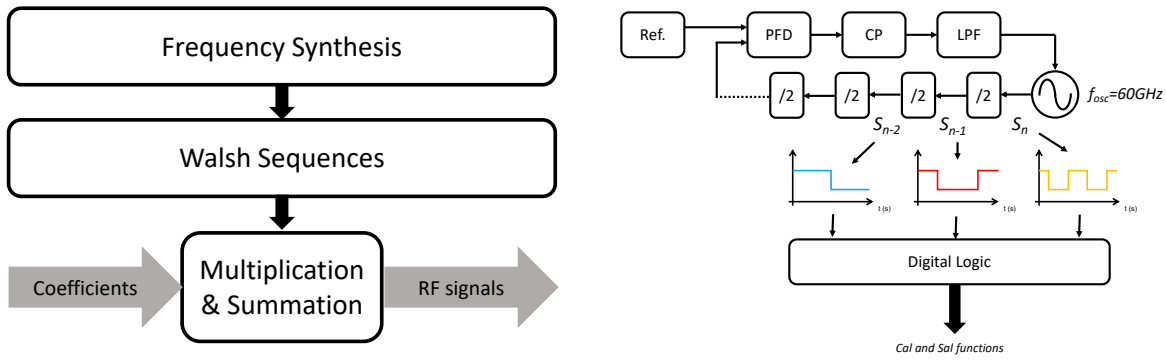
Architecture

Fig. 2.12(a) presents the system as it is described in details in [33]. It is composed of 3 main parts:

— Squares signal are provided by a mmW frequency synthesis from a PLL. It is a fundamental block in RF transmission / reception and can therefore be re-used as it is. Square signals are associated together thanks to logic gates to provide every Walsh function (cf. Fig. 2.12(b)),

— Coefficients are converted from digital to analog and multiplied to Walsh functions,

— Summation of all sequences are performed by differential pairs weighted by their tail-current sources.



(a) (b)

Figure 2.12 – Walsh system (a), and its associated sequences generation (b)

Compared to classical transmitter architectures, the signal is arbitrary generated which means that in the case of carrier aggregation, every channel is synchronized to each other. The non-dependence to a dedicated local oscillator for every channel offers first a robust architecture to asynchronicities and also a lower silicon footprint.

Our research work was to establish the trade-off between Walsh order, the number of coefficients and spectrum mask (i.e. modulated signal resolution such as SNR, EVM, etc.). We have demonstrated that the SNR is similar to the one of a regular DAC and based on the coefficients conversion one. But, the system is wide band and the coefficients refreshment is the main bottleneck as there are numerous and only a few are relevant. Thus, the tradeoff lies on identifying the "good" coefficients to convert with high resolution and the "bad" coefficients with a low impact on signal quality.

The main question is to identify how to address those coefficients. We decide to consider a limited number of parameters:

— Walsh order: it has to be as low as possible to reduce dimensions of logic glue and number of coefficients,

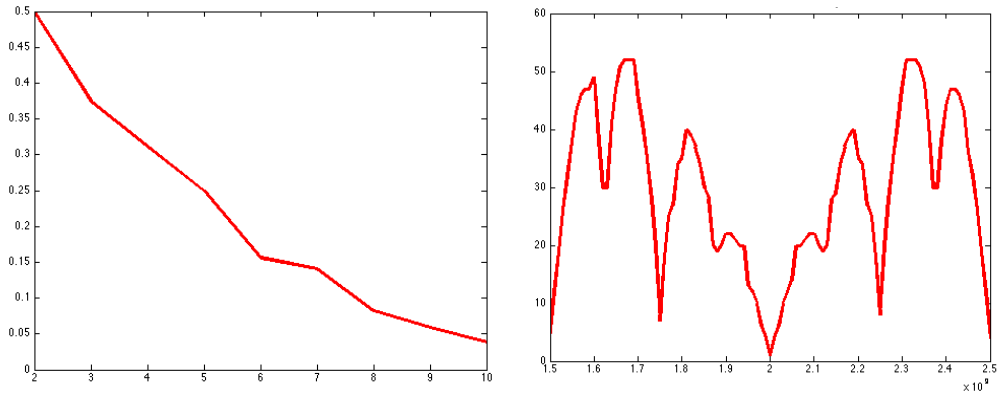
— Coefficient binary order: a truncature of coefficient binary code, i.e. a limited resolution for insignifiant ones.

For instance, simulations have been performed to evaluate the number of coefficients to be addressed versus the Walsh order in Fig. 2.13. We can assume that:

— Walsh order: Fig. 2.13(a) depicts the percentage of coefficients used in relation with the Walsh order (here given in $\log_2$). Te higher the order is, the lower the percentage is, which means

that the number of coefficients is relatively constant whatever the order for given specification. We decide that after an order of 6, i.e. 64 Walsh sequences, resolution is sufficient for our applications,

— a non-linear behavior in terms of frequency: Fig. 2.13(b) presents the number of coefficients required among 64 to generate a CW signal at a given frequency. Within a frequency band from 1.5GHz to 2.5GHz, this number can vary from 1 to 52. Some investigations have demonstrated that all those coefficients are not necessarily relevant as some of them have small value compared to others. Quantification would determine a LSB and thus, a truncature threshold that would reduce the number of active coefficient.



(a) (b)

Figure 2.13 – Percentage of coefficients used versus the Walsh order (a), number of coefficients used within a large frequency band based on a 64 Walsh sequence architecture (b)

Simulations

The Walsh generator circuit has been designed in the 28nm FD-SOI CMOS technology from STMicroelectronics. [31] presents the discussion about the trade-off between the Walsh order, the number of coefficients and their resolution. We have decided the most relevant number of Walsh functions is 64 with a 6-bit coefficients coding. We have simulated its behavior in a 5G scheme presenting its spectrum and associated eye diagram and EVM as depicted in Fig. 2.15).

The 3 signals are respectively:

— QAM-16 modulated signal at 2.31GHz with a bit rate of 10MS/s,

— QAM-64 modulated signal at 2.33GHz with a bit rate of 10MS/s,

— QPSK modulated signal at 3.58GHz with a bit rate of 25MS/s.

As one can see, Walsh Tx can convert very close bands while keeping very good EVM under 1% despite the limited number of coefficients.

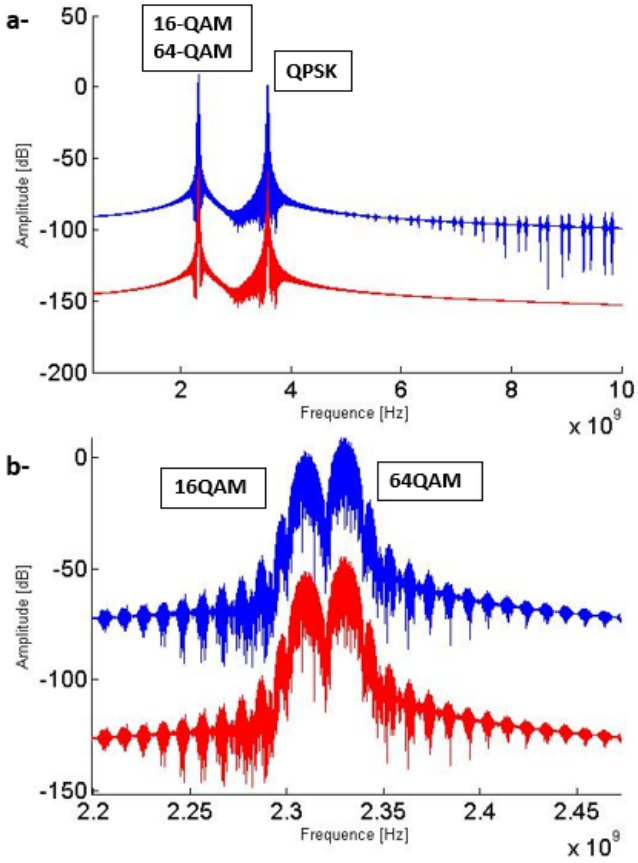


Figure 2.14 – Carrier aggregation done by Walsh Tx in frequency

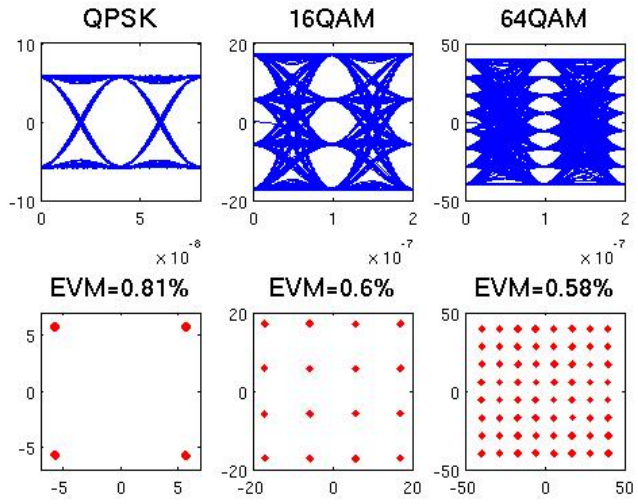


Figure 2.15 – Associated eye diagram and EVM

Based on the design work, we estimate that:

— The core system would consume around $25mW$ and has an estimated size of $0.35mm^2$,

— The Walsh DAC would consume $13.62mW$ under 1V and its estimated size is $0.2mm^2$.

Perspectives

At this day, we propose to integrate the Walsh generator in a complete transceiver and investigate on the relevancy of Walsh base to undergo all the signal processing, such as RF filtering for Rx and pre-distortion techniques for Tx. The project is detailed in section 4.1.1.

2.3 Time domain

2.3.1 Riemann Pump Tx

An arbitrary waveform generator (AWG) architecture was the subject of Dr Yoan Veyrac's PhD thesis [2]. We proposed to generate a signal based on its piecewise linear approximation, resulting from the use of a differential digital coding associated with a suited digital-to-analog converter (DAC), named here the Riemann Pump. A first version was designed in a GaN technology [34], suited for power applications and a second version was designed in 65nm CMOS technology, suited for 5G applications [35].

Concept

The purpose of the presented system is to generate arbitrary waveforms up to the GHz range with a low cost and low consumption solution. The wanted signal is available in a high resolution digital representation. It is converted in its Riemann form with a specific coding, and then converted in the analog domain thanks to a pre-determined set of slopes such as presented in Fig. 2.16.

The generation process is implemented as shown in Fig. 2.17. A Digital Signal Processor (DSP) computes the Riemann code (i.e. the slopes index sequence) from the theoretical signal we want to generate. This code controls switched current sources, in order to generate current steps that are integrated into an output capacitor, producing a piecewise linear approximation of the wanted signal.

The Riemann Pump principle is detailed in [35]. We have demonstrated that the SNR for a full scale sine wave is calculated as:

$$SNR_{dB} \approx 6.02N + 9.03r - 7.78 + 10log_{10}(1 - \frac{1}{2^{N-1}} + \frac{1}{2^{2N}}) \tag{2.5}$$

In the Eq. 2.5, the dependence of the SNR on the OSR has a double origin. The main effect comes from the differential coding; any doubling of the sampling frequency divides by 2 the range to be covered by

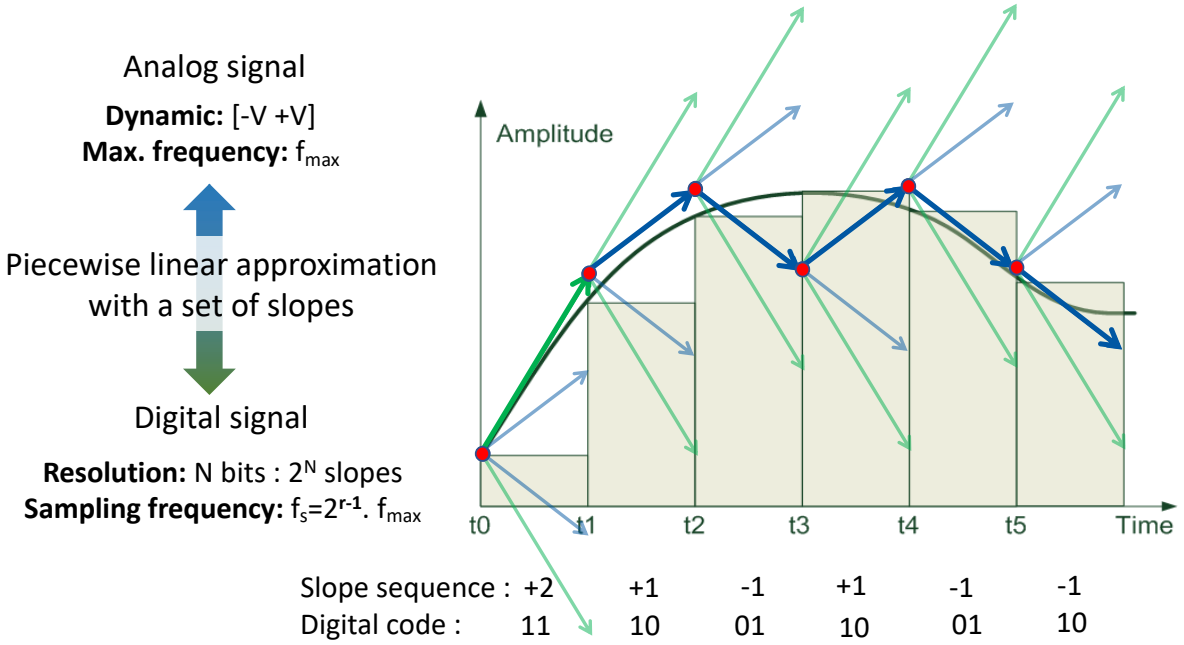


Figure 2.16 – Riemann Pump Architecture Principle.

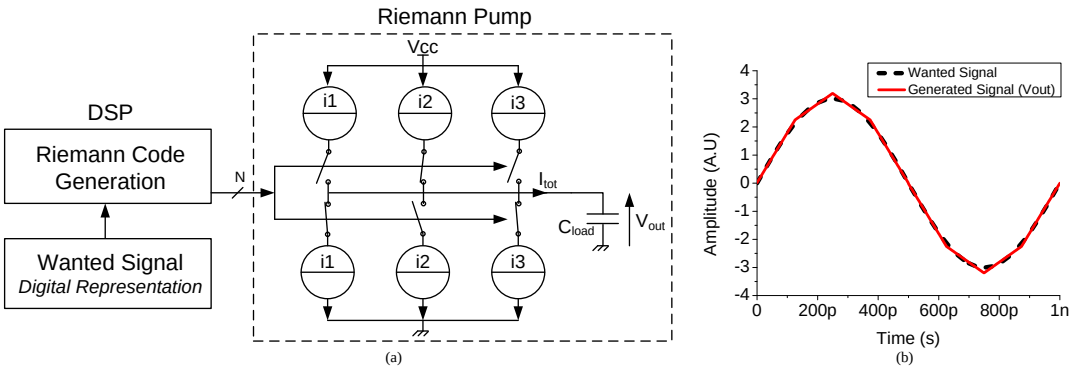


Figure 2.17 – Riemann Pump Architecture (a) and theoretical signal generation (MATLAB) (b).

the quantizer, as well as the quantum. Thus, it generates a factor $6.02r$ in the SNR, corresponding to a decrease of the total quantization noise generated. The additional factor $3.01r$ comes from the filtering out of the noise lying on the band $[f_{max}, \frac{f_s}{2}]$. Considering our application, the OSR is inherently low and its effect does not mainly depend on the filtering of the out of band quantization noise. The requirements on the analog output filter are thus relaxed. This topology of digital to analog conversion is optimized for low OSR applications, in order to cover a large frequency band without a complex and resource intensive architecture. An optimized noise shaping was proposed in [36], named Noise Shaping Riemann (NSR).

Architecture

The signal generation process can be formalized as shown in Fig. 2.18. A bandwidth limited analog signal of maximum frequency f_{max} can be perfectly described by an ideal digital signal sampled at the Nyquist frequency ($f_s = f_{nyq}$) which is worth twice f_{max} (Nyquist-Shannon theorem). That is to say the original analog signal can be recovered without any additive noise; provided the digital signal has a perfect accuracy and the sampling images are ideally filtered. This is theoretically achievable with an infinite number of bits to code the sampled analog levels. Such a signal would exhibit an infinite signal to noise ratio (SNR). An actual DA conversion obviously involves a digital signal with a limited number of bits N to drive the DAC. The overall DA conversion can thus be split into two distinct parts:

— a digital-to-digital (DD) conversion that transforms the ideal digital signal into a resolution-limited digital signal (which produces quantization noise),

— a DAC together with an additional low pass filter.

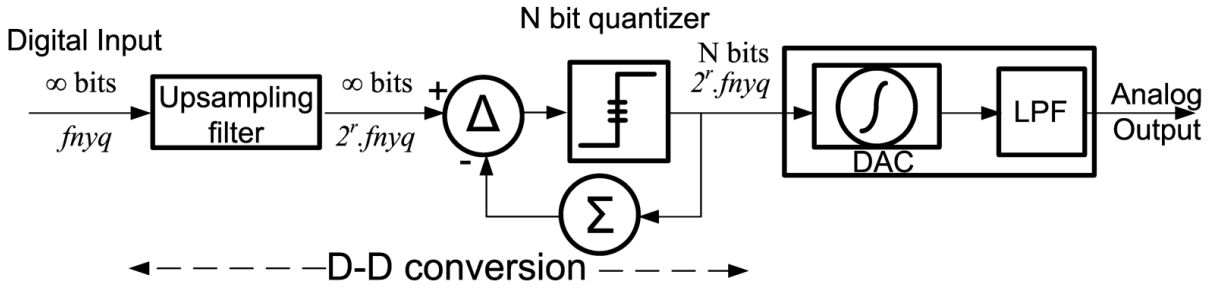


Figure 2.18 – Riemann DAC topology.

Schematic

The number of bits of the prototype designed for our research work is limited to 3 bits for measurement purposes. The maximal switching frequency of this DAC core is 25 GHz, which gives a bandwidth (BW) larger than 3 GHz with an oversampling factor r of 2 ($2.r = f_s/2.BW$). Provided the multi-gigahertz target bandwidth and the typical picofarad range of integrated circuit capacitances, the full scale current is limited to several hundreds of microamperes to generate output voltages of hundreds of millivolts. Considering a complete transmitter topology, the Riemann Pump can directly drive an amplifier whose input impedance is capacitive, which is most often the case in CMOS technology. It provides an inherent wide-band operation while avoiding any cumbersome matching network at the input of the amplifier. A prototype of the Riemann Pump was designed in a 65 nm CMOS technology from TSMC. A simplified version of the transistor-level schematic view of the circuit is presented in Fig. 2.19.

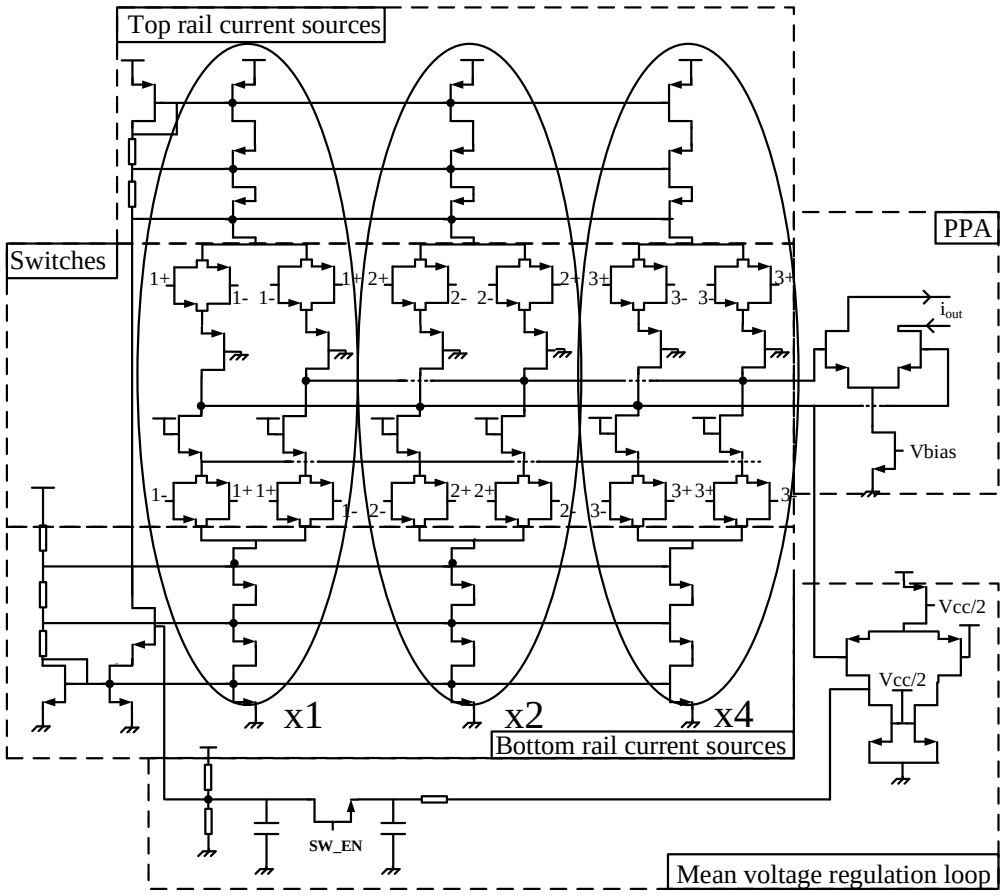


Figure 2.19 – Riemann Pump schematic

Simulations

The ability of the system to handle concurrent transmission is demonstrated with a combination of 3 modulated signals distributed over the [0 - 3 GHz] band corresponding to several standards with their characteristics

— QPSK modulated signal at 900MHz with a bit rate of 10Mbps.
— QPSK modulated signal at 2.45GHz with a bit rate of 20MS/s,
— QAM-16 modulated signal at 2.6GHz with a bit rate of 40MS/s,

The spectra of the composite signals corresponding to the sum of the 3 modulated signals reconstructed with respectively the Riemann and the NSR coding scheme are displayed in Fig. 2.20 [36]. One can notice that for the Riemann conversion, the noise floor is flat over the whole band. Nevertheless, the noise floor exhibits a high pass characteristic for the NSR; it is not uniformly distributed over the whole band but it turns out lower than the Riemann case in the band of interest. The 3 signals are demodulated independently for the two conversions. We only observe their respective eye diagram and EVM

in Fig. 2.21. The obtained EVM values for the Riemann conversion are around 1%, which is far below the requirements for the most common standards. There is room for the command circuit and the power amplification imperfections.

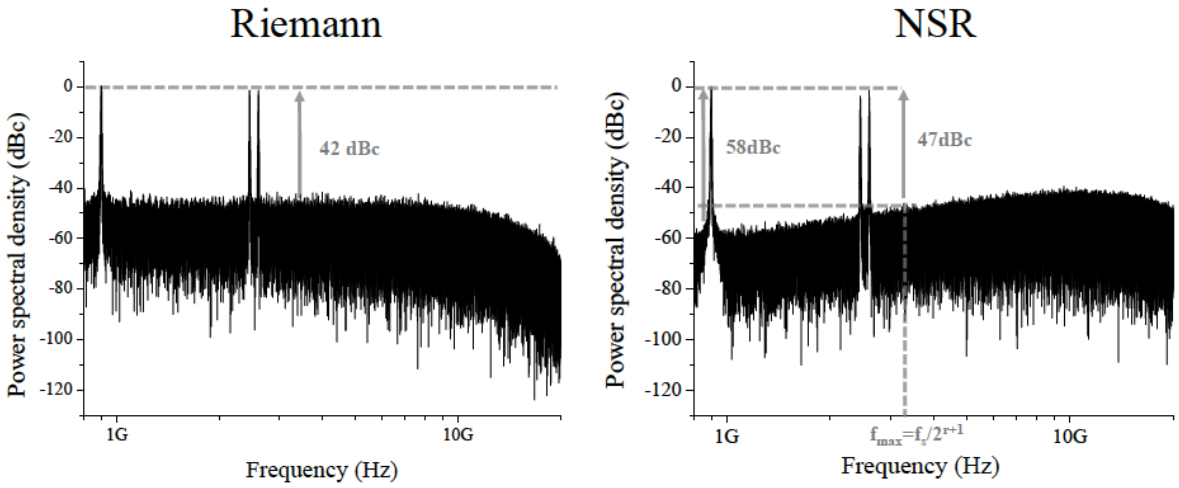


Figure 2.20 – Carrier aggregation: spectrum

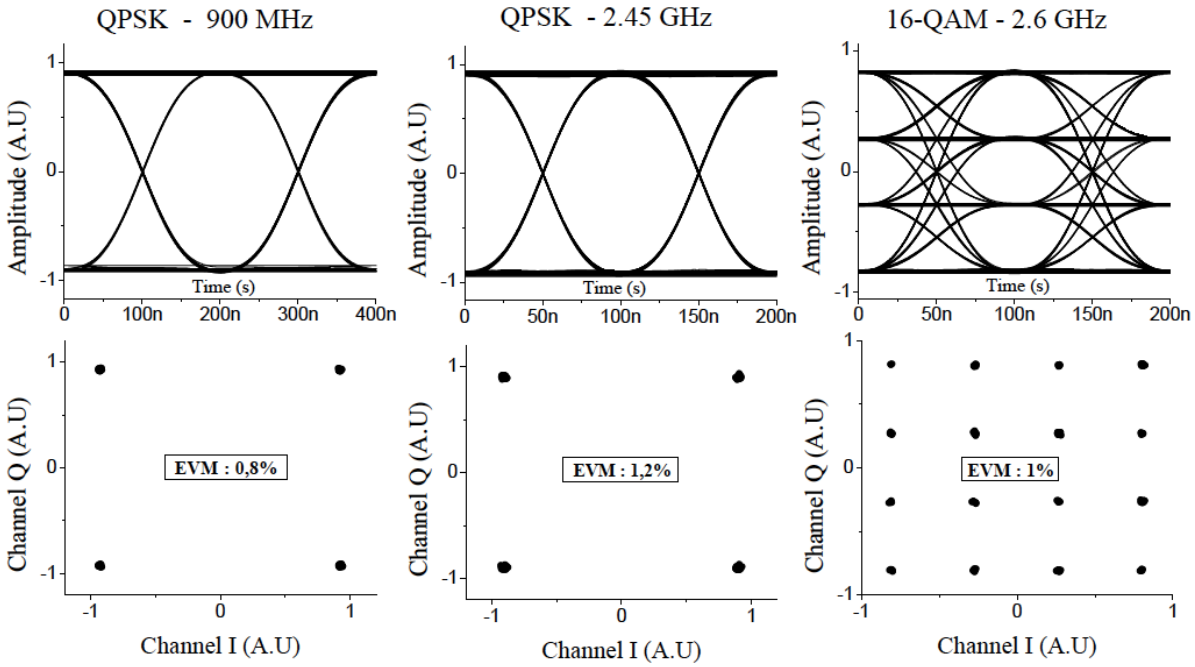


Figure 2.21 – Carrier aggregation: eye diagram

Measurements

Several campaigns of measurements have been performed such as in [37]. Our target was to demonstrate the ability to generate a multi-carrier signal over a large bandwidth. Device under test (DUT) is shown in Fig. 2.22. We present here a limited number of relevant measurements.

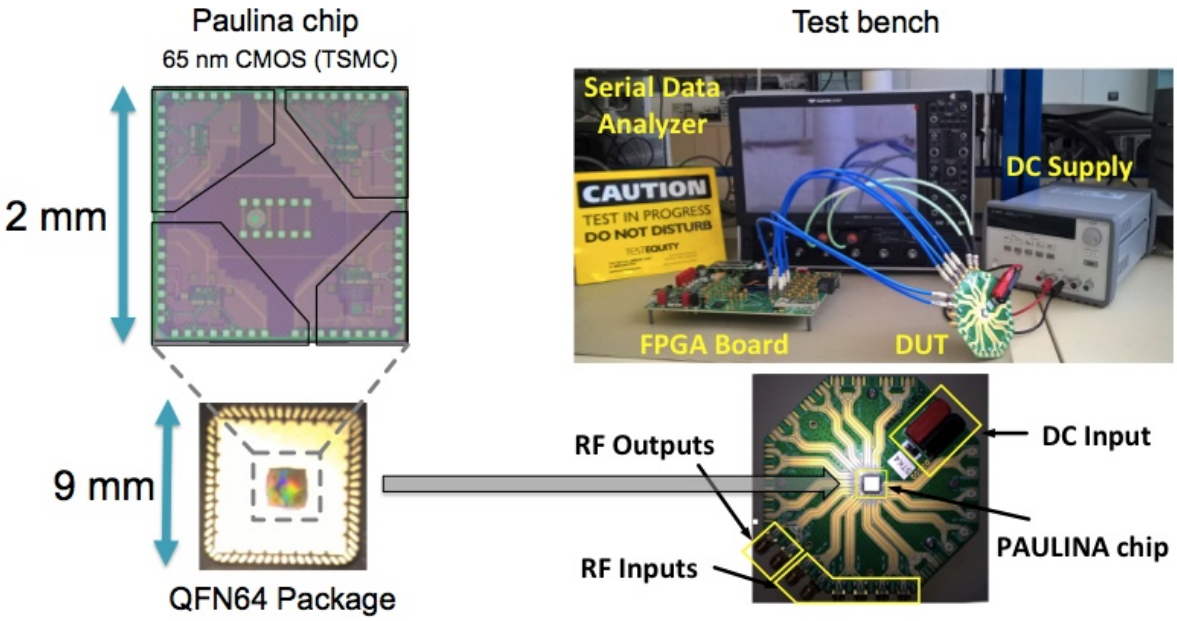


Figure 2.22 – Device Under Test from chip to bench

We generate various signals from 700MHz to 2.68GHz to demonstrate the feasibility of four different carriers with three modulation schemes. The Fourier Transform of this multi-carrier signal is depicted in Fig. 2.23. The 4 signals are respectively:

- A: Continuous sine-Wave (CW) at 623MHz,
- B: GMSK modulated signal at 700MHz with a bit rate of 1MS/s,
- C: QAM4 modulated signal at 2.12GHz with a bit rate of 10MS/s,
- D: QAM16 modulated signal at 2.68GHz with a bit rate of 50MS/s.

5G standard implies to reach data rate of several hundred of MS/s. QAM4 represents the kind of modulation scheme used for 5G which will be by extension QAM64 to QAM256. We decide to limit our measurements to QAM4 because of a limited size of FPGA memory which is not compatible with higher complexity of modulation scheme.

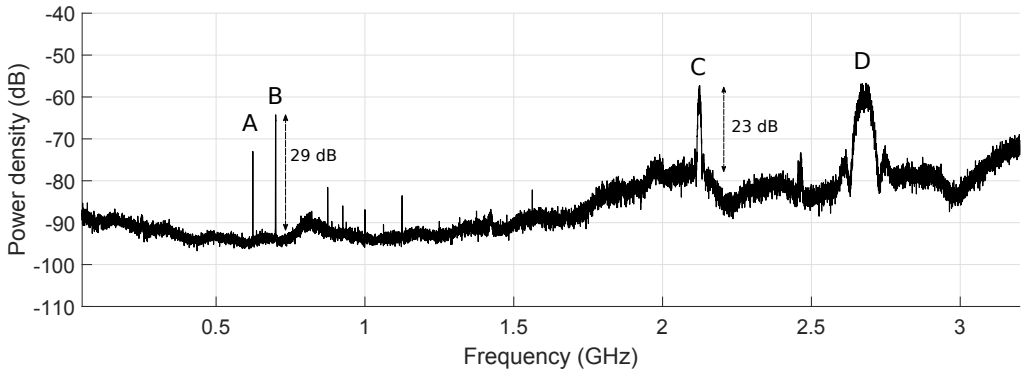


Figure 2.23 – Fourier Transform of a multi-carrier signal with (A) sinusoidal signal, (B) GMSK, (C) QAM4 and (D) QAM16 modulated signals

A characterization of frequency behavior of QAM4 for several data rate is depicted in Fig. 2.24 with a carrier frequency of 2.6GHz. The bandwidth increases with the data rate from several MHz to hundreds of MHz. Spurs located at 500 MHz around the carrier frequency are artefacts due to post digital signal processing and has no link with any chip imperfection.

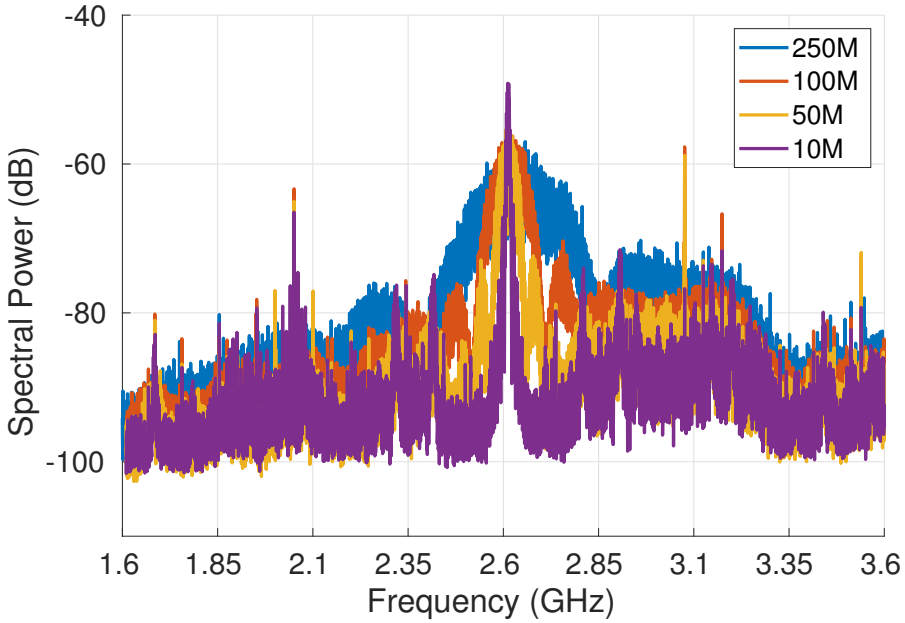
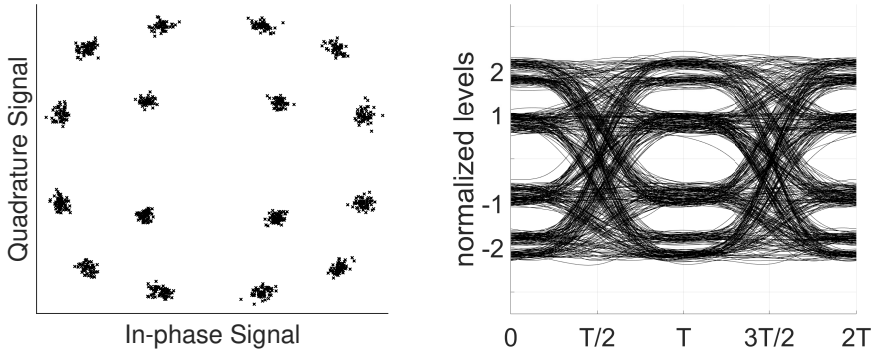


Figure 2.24 – Fourier Transform of QAM4 modulated signal using different data rates

A focus is made on a QAM16 measurements at 2.6GHz in Fig. 2.25(a) and 2.25(b). As one can see, eye diagram exhibits good shape and EVM remains acceptable under 16%.



(a) (b)

Figure 2.25 – Constellation associated with eye diagram of QAM16 modulated signal at 2.6GHz with a data rate of 50MS/s (a) (b).

Perspectives

At this day, we have made the complete demonstration and characterization of this architecture. Its transfer to the industry is supported by the University of Bordeaux with a proposition to extend investigations to a complete integration of the digital and the analog part. The digital part would sustain dedicated digital-to-digital conversion and a high-data rate conversion based on multiplexing to control the Riemann Pump. Last but not least, those research opened the way for a receiver solution detailed in section 2.3.2.

2.3.2 Delta Riemann - Breda Rx

.

This work was proposed in the continuity of the Riemann Pump Tx. This idea was to investigate on a receiver using the same conversion scheme, which was named Delta-Riemann Rx and nicknamed Breda. There is no PhD thesis nor project associated to it but preliminary results have been published in [38].

Concept

The circuit quantifies the RF signal derivative. We code the derivative by comparing a sampled input signal with a limited set of slopes like for the Riemann Pump. For instance, if we consider 2 input samples, $x(k)$ and $x(k+1)$, that correspond to the interval $t = [x(k), x(k+1)]$. The derivative is calculated as follows in Eq. 2.6:

$$D(k) = \frac{y(k+1) - y(k)}{x(k+1) - x(k)} \tag{2.6}$$

Then, we discretize the slope by quantifying it. It leads to convert into digital the derivative as depicted in Fig. 2.26 where the slope will be approximated among a set of predetermined values representing the meaningful slopes that compose the derivative signal.

This concept is depicted in Fig. 2.27. It exhibits the original signal, the quantized derivative and the reconstructed signal. It is possible to observe that the reconstructed signal is close to the original one.

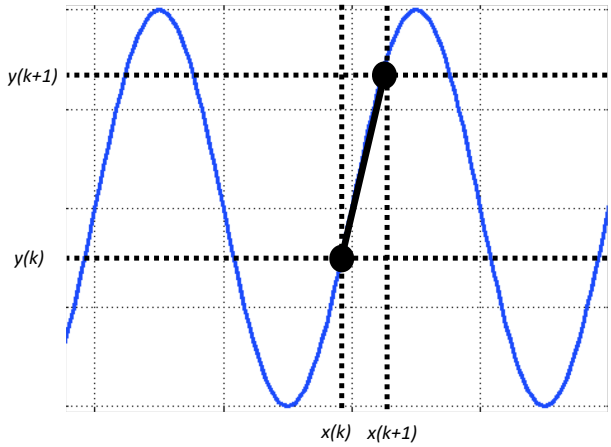


Figure 2.26 – Basic Delta-Riemann ADC

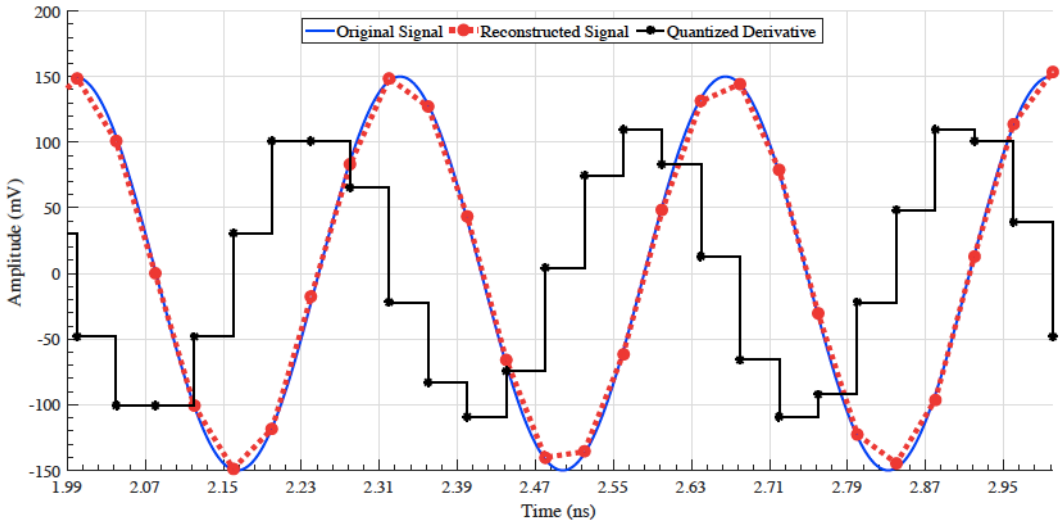


Figure 2.27 – Basic Delta-Riemann ADC

Architecture

Fig. 2.28 presents the architecture. First, the reference signal $R(t)$ is subtracted from the input signal $A(t)$ resulting in a differentiated signal $D(t)$. Next, this differentiated signal is quantized into a N-bit code $Q(t)$. Then, at a sampling clock transition, this signal is then latched as $L[k]$. The latch works as a sample and hold stage and at the sampling clock transition, its output changes switching the Riemann Pump internal current sources to the new sampled code. Finally, the Riemann Pump capacitive load will then integrate the new resulting internal current i($L[k]$) for a whole sampling period (here T_s) generating a new reference value $R(t)$. At the new sampling clock transition, the reference value $R(t+Ts)$ will be close to the value of input signal $A(t)$ at the beginning of the previous sampling period. Those five septs are performed within a whole sampling period T_s: delta signal generation, quantization, latching, Riemann Pump switching and Riemann Pump integration. Due to the high GHz sampling frequencies, the sampling period is very short (for instance, 40 ps for a 25GHz sampling frequency).

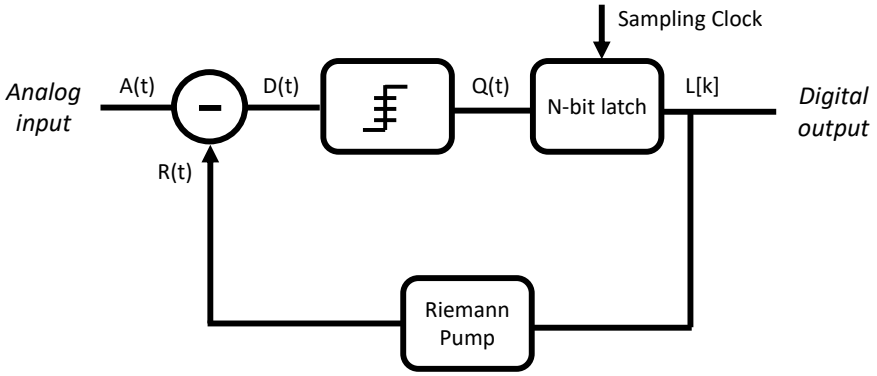


Figure 2.28 – Basic Delta-Riemann ADC

As the Delta-Riemann Rx integrates a Riemann Pump, we have decided to keep the same parameters as the ones chosen in the prototype presented here below, i.e. 3-bit encoding and a sampling frequency at 25GHz.

Simulations

The Delta-Riemann is simulated in MATLAB using the sub-6GHz 5G standard with 10 carriers, each of it modulated with a bandwidth of 20MHz. The bit sequences of each carrier were then demodulated and the quality of signal in each channel evaluated. The resulting reconstructed signal power spectrum is shown in Fig. 2.29. Some spectral leakage is present due the non-coherent sampling resulting in a non flat noise floor. The noise floor is between -40 dB and -50 dB. Since the carrier frequencies present a power spectral density close to 0 dB, the minimal SFDR is near 40 dB.

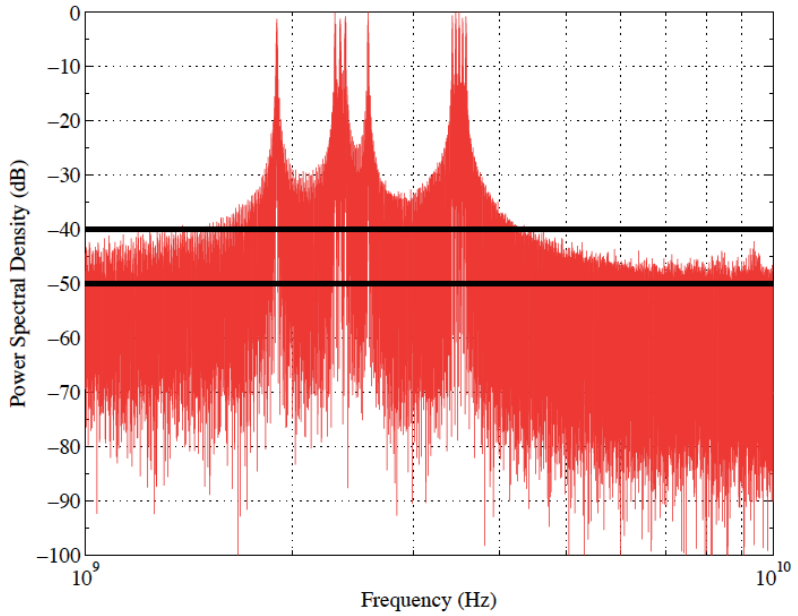


Figure 2.29 – Spectrum of Reconstructed signal - 10 aggregated channels

Since the Delta-Riemann Rx degrades as the overall internal delay increases, it may produce demodulation errors. A QAM16 signal composed of a bit sequence for 256 symbols at a data rate of 10 MS/s was tested for different internal delays. The demodulated constellation is then normalized, rotated and scaled. The results in terms of error vector magnitude (EVM) are presented in Fig. 2.30 for 2 delays, respectively 20ps and 30ps. The EVM for dispersion was obtained in reference of the mean constellation IQ values received for each symbol. According the results, the Delta-Riemann Rx produces a distortion that increases as the internal delay increases.

Perspectives

At this day, there is no demonstration of the Delta Riemann - Breda Rx. As for the Riemann Pump, a complete integration of both the analog and the digital part would motivate investigation either in circuit design or in signal processing.

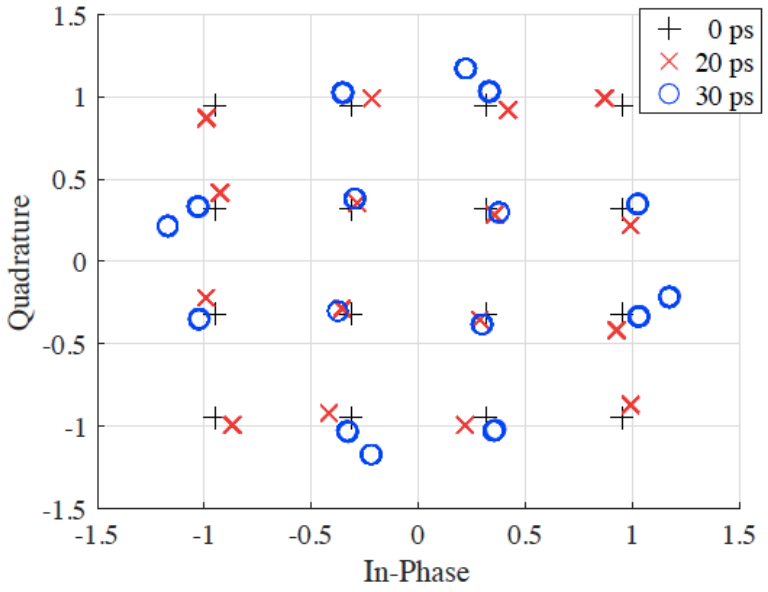


Figure 2.30 – Normalized constellations after rotation and scaling

2.4 Conclusion

This chapter presented the concrete application of the concept of Design by Mathematics. It has been applied in 2 domains, frequency and time ones, with both a receiver and a transmitter solution. For each of them, our investigations focused on the proposition of an architecture and its integration. The architecture illustrates the principle of a base integrated in a chip and the use of coefficients converting the information to RF. We have demonstrated some potential applications listed as follows:

— **Sampled Analog Signal Processor (SASP)**: carrier aggregation for 5G standard and RADAR application with low-latency signal processing,
— **Walsh Tx**: direct carrier aggregation and amplification for 5G standard,
— **Riemann Pump Tx**: arbitrary waveform generator for IoT application and 5G standard,
— **Delta Riemann - Breda Rx**: wide-band ADC for IoT application and 5G standard.

Perpectives of research would be to carry those demonstrators to a more-advanced development such as a more detailed modeling, simulation and demonstration to reach RF specifications. This could be done by adding noise considerations, especially in very advanced technologies, and interferer rejection, especially when very wide band are concerned. Last but not least, as the point of view changed from traditional way of conversion to a coefficient-based one, it could be interesting to propose a dedicated digital signal processing using the coefficient and not necessarily a conventional one.

CHAPTER

3

DESIGN BY MATHEMATICS FOR BIO-RELATED IC

Sommaire

Chapter 3 presents our research work on architecture dedicated to health applications. It starts with the design of a MEMS interface, called Corona Tx, for blood pressure measurement from sensing to transmission using IBC standard. The chip has been designed to sense a capacitive variation and encode and transmit it by RF thanks to a full analog circuit. The second work, called WiBio Rx, was performed to convert ECG signals with an investigation on the sparsity to adapt the converter architecture. The choice of an LC-ADC was made to design and simulate the system. The last work is about a new technique of communication within the human body using ultrasounds. Our research purpose is to analyze the relevancy of ultrasounds as a mean of wireless link within the body to setup a complete network. As demonstrated, it is twice more efficient and paves the way to explore the design of circuits dedicated to this new communication scheme.

Key words: analog interface, health monitoring, LC-ADC, sparsity, ultrasounds, intra-body communications.

The work on Intra-Body Communications (IBC) has been initiated in 2013. The purpose was to jeopardize what was commonly found in the literature by redefining the paradigm of communication of the Human body by taking into account its nature. Ultra-low power electronics is mandatory and thus, dedicated integrated circuits must be designed. We investigate solutions that adapt the analog-to digital conversion or avoid completely this conversion. Last but not least, the propagation medium is not necessarily relevant for RF and its specificity must be taken into account leading to the use of ultrasounds.

3.1 Wireless Sensor Interface - Corona Tx

This work was initiated in partnership with Monash University in Prof. Jean-Michel Redoute research group. Our goal was to develop an ultra low-power integrated interface for capacitive and resistive MEMS and sensors, intended for use in biomedical applications. Medical implant technologies are increasingly used in routine medical monitoring of patients health and performance: indicators such as blood pressure, pulse rate and temperature provide useful information to medical practitioners, leading to real-time patient diagnoses. Monash University has developed a MEMS to measure blood pressure and we need to convert information from the MEMS to transmit it using RF.

Concept

The design of wireless biomedical implants is subject to strict constraints on power consumption, size and reliability. Many designs for biomedical sensor interfaces utilise an architecture requiring input instrumentation amplifiers, analog to digital converters, and a clock, carrier and modulation generating circuits [39]. The wireless transmission in an implant is the most power hungry component. For this reason, we wanted to improve the efficiency of data transmission in implant's power performance. We started by prototyping a system in COTS presented in [40].

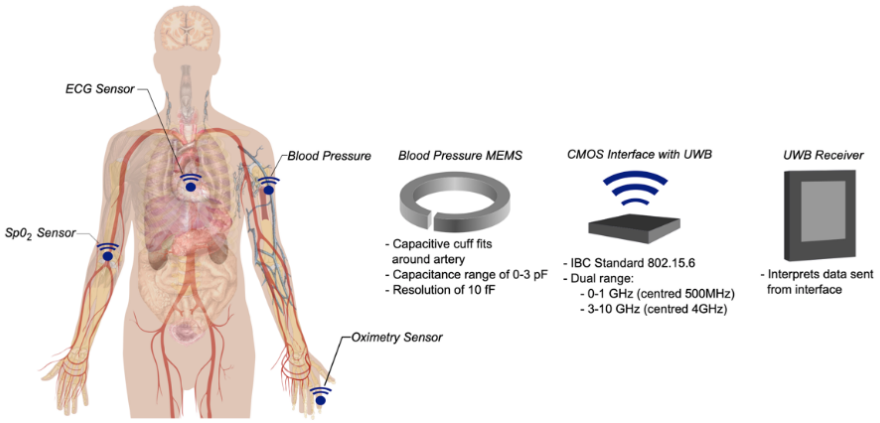


Figure 3.1 – Corona System View

The interface encodes sensed data from a MEMS blood pressure sensor and transmits UWB (Ultra Wide-Band) pulses without any analog to digital conversion. This reduces dramatically the power consumption. We have decided to convert the capacitive and resistive variations of the MEMS pressure sensor to pulses using UWB communication link respecting standard [41].

Architecture

The system achieves a capacitance to time conversion with 10fF resolution. A DC current source I_{BIAS} is used to create a linear voltage ramp (V_{in}) across a capacitive sensor C_{sensor} such as depicted in Eq. 3.1 and in Fig. 3.2. When the ramp crosses a reference voltage (V_{REF}), the capacitor is discharged and the comparator switches states. The discharge time of the capacitor can be varied using a delay circuit controlled by a voltage input 'Switching Time Control' (SWT in Fig. 3.2). As the value of C_{sensor} changes (ΔC_{sensor}), the time taken by each voltage ramp also changes (Δt).

$$\Delta V_{in} = \frac{I_{BIAS}.\Delta t}{C_{sensor} + \Delta C_{sensor}} \tag{3.1}$$

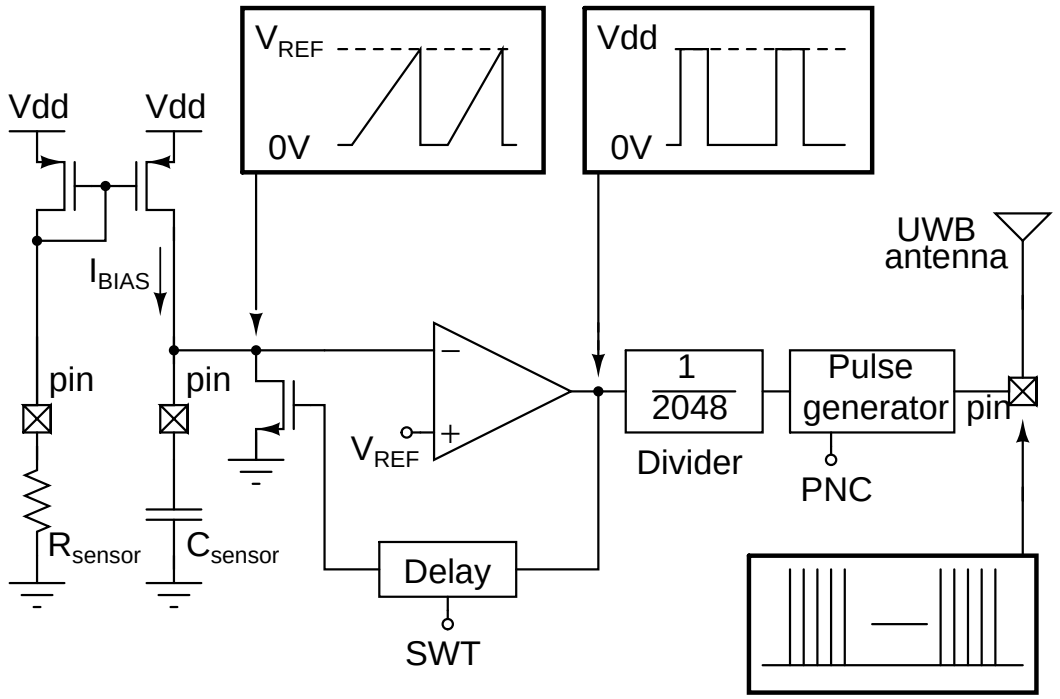


Figure 3.2 – Proposed architecture

I_{BIAS} has been designed equal to 500nA with V_{REF} equal to 1V for a time difference between samples (i.e. edges between when the comparator has switched) equal to 90.4ns corresponding to a MEMS capacitance variation of 45.2fF. Those choices corresponds to 1mmHg as described in the literature. We add a clock divider, constructed by chaining D-flip-flops, to increase the reliability of measurement by allowing the output to switch only once for several charge/discharge cycles. This reduces the transmitted power and averages the capacitance and current source and reducing the effect of high frequency noise. The value of the divider chosen equal to 2048, resulting in a chain of 11 D-flip-flops.

A UWB signal must have either a bandwidth higher than 500 MHz, or more than 20 % of the centre frequency [41]: the presented interface has been tuned to operate in the low band channel 1 (i.e. below 1 GHz). An UWB signal is transmitted at every edge on the output of the divider. A delay module controlled by the voltage 'Pulse Number Control' (PNC in Fig. 3.2) is used to alter the length of the UWB transmission. At all other times the UWB circuitry is off. The UWB pulses are produced with a current starved ring oscillator (Fig. 3.3). The frequency and width of the individual pulses are controlled by the input voltages 'Pulse Frequency' (PF) and 'Pulse Width' (PW). These voltage inputs control the bandwidth of the output, and can be used to minimize the power consumption of the system. The UWB signal is then buffered and driven to the off-chip antenna.

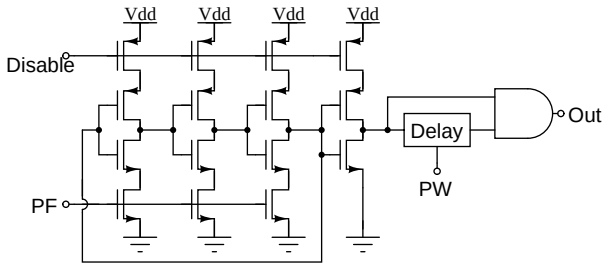


Figure 3.3 – Schematic of the pulse train generator

Measurements

The circuit was designed and fabricated in the UMC 0.18 μm CMOS process such as depicted in Fig. 3.4 and published in [42]. In order to replicate a capacitive MEMS pressure sensor, a digitally controlled internal capacitor bank was integrated on-chip. It has a resolution of 9 bits, with 10fF as the LSB, giving it a range of 0-5.12 pF. The circuit area including the capacitor bank occupies 230 $\times$ 230 μm^2: the circuit without the capacitor bank occupies 215 $\times$ 50 μm^2.

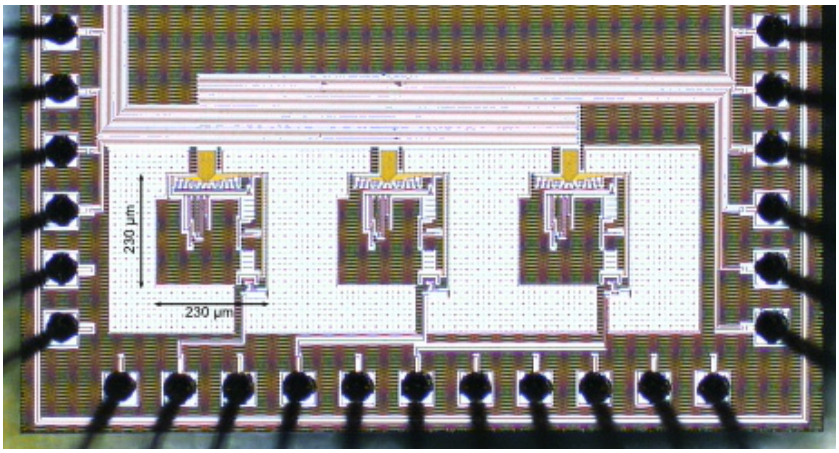
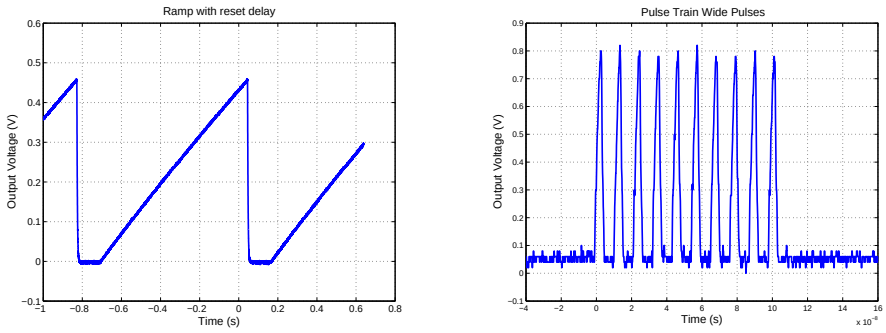


Figure 3.4 – Photograph of the die

Fig. 3.5(a) shows the measured voltage ramp across the sensor capacitance: the figure shows that the system behaves as expected, by discharging the sensor capacitance during a configurable delay time once the voltage across C_{sensor} exceed the reference voltage. The linearity of the system was obtained by measuring the effect of changes in capacitance on the time between pulses at the output of the divider. This measurement combined non-linearities in the voltage ramp and in the capacitor bank. On average, the time between pulses increased by 5.146μs for every 10fF difference in capacitance. The initial offset of 489.85μs corresponds to the residual capacitance formed by the bondpad, bondwire and IC pin. The measured integral non-linearity (INL) of the system was 70.3uS, corresponding to an error of 136.6fF

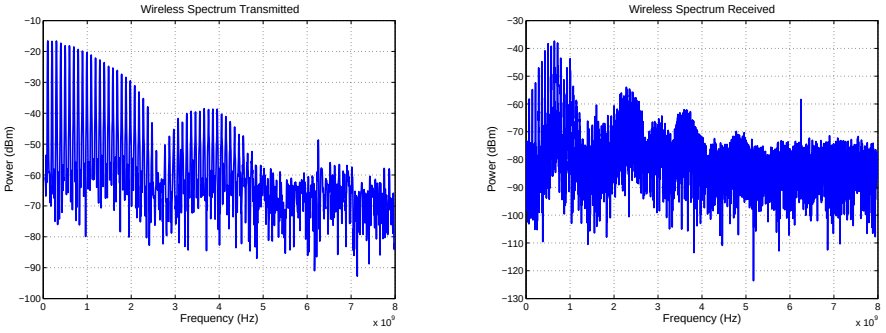
(13.66LSBs). This value is less relevant than the differential non-linearity (DNL), as it can be eliminated by calibrating the input values based on the known variation in capacitance. The maximum differential non-linearity of the system was 8.87μs, or 1.73LSBs. This corresponds to an error of 17.3fF. As the sensitivity for the implantable capacitive pressure sensor is 45.2fF/mmHg, the error is within an acceptable range. The corresponding effective number of bits (ENOB) for this system is 8.1.

The pulse frequency and pulse width of the system were tuned to produce a wide spectrum (Fig. 3.5(b)). Measurements at the output of the circuit showed significant frequency components up to 4.5 GHz (Fig. 3.6(a)). The UWB transmission capability was tested by connecting matched UWB antennas, separated by 5 cm (Fig. 3.6(b)). With filtration, the transmitted signal complies with IEEE standard 802.15.6-2012 [41], low band channel 1 (center frequency 3993.6 MHz).



(a) (b)

Figure 3.5 – Measured voltage ramp across the sensor capacitance, (a), Measured pulse train tuned to have a wide spectrum, (b)



(a) (b)

Figure 3.6 – Frequency spectrum at the output of the circuit, (a), Frequency spectrum of the received wireless signal, (b)

The average power consumption of the system was 200nW at the minimum sample rate of 8.2Hz. At 37Hz, the system consumed 1.04μW. At a higher sample rate of 105Hz, the system consumed 4.75μW. At the maximum sample rate of 575Hz, the system consumed 59.8μW.

Perspectives

A second circuit was fabricated using a new sampling scheme related to the one used in section 2.3.2 in order to reduce more the power consumption. The results are presented in [43]. Nevertheless, the chip was never co-integrated with the sensor to fully experiment its application to blood pressure in-vivo measurement.

3.2 ECG Converter - WiBio Rx

This work aimed at investigating on the conversion of electrocardiogram (ECG) signals for its wireless transfer. We have designed a system by optimizing the conversion based on the signal properties to alleviate the energy cost of information transfer, as a biosignal-dependent design methodology for the LC-ADC. We performed this work in collaboration with SUPCOM (Tunis, Tunisia) with the PhD thesis of Dr Mariam Tlili [44].

Concept

Many efforts focus on reducing power consumption of non-invasive measurement systems such as:

- Realizing architectural optimizations of the analog front-end design such as turning on the ADC by means of a low-power control strategy or using ultra-low power miniaturized electrodes to save energy [45, 46],
- the digital ECG compression and encoding after analog-to-digital conversion [47]. Transform methods [48, 49], are among the most commonly used compression techniques. Optimized parameters benefit from time-domain sparsity to provide accurate compressed representation of original data,
- an hybrid solution realizing architectural optimizations by means of sampling methods that rely on the sampled signal sparsity [50].

We propose an alternative solution based on designing a level-crossing ADC (LC-ADC) to efficiently sample analog ECG signals. According to Nyquist theorem, the uniform sampling rate should be higher than twice the maximal frequency of the signal bandwidth. Thus, with slow ECG amplitude variations in time domain, as depicted in Table 3.1, redundant data are acquired when the signal is uniformly sampled at the Nyquist frequency. In contrast, the level-crossing analog-to-digital converter (LC-ADC) is inactive in slow-changing intervals which avoids unnecessarily acquired data.

Wave/Segment	**Amplitude** (mV)	**Duration** (s)
P	0.2 - 0.25	0.08 - 0.1
QRS	Q : 0.05 , R : 2.5	0.04 - 0.1
T	0.1 - 0.5	0.35 - 0.43
PR	-	0.12 - 0.2
ST	-	0.05 - 0.15

Table 3.1 – Normal ECG temporal and amplitude waves characteristics.

Architecture

Fig. 3.7 depicts the LC-ADC architecture. It is composed of two comparators, two DACs, a window-update stage, an output-selection stage and a time-tracking stage. The input signal, ECG_{in}, is compared to voltage levels, V^+ and V^-, at continuous time. Meanwhile, the time duration between two consecutive level-crossing events is computed at a constant counter clock frequency, F_C. As long as ECG_{in} is between V^- and V^+, the outputs of both comparators are low and the LC-ADC elementary circuits, at the exception of the time-tracking stage, are inactive. Once the input signal moves outside this range, one of the comparators' outputs, *INC* for increment or *DEC* for decrement, is set to the logical value $'1'$ and the entire circuit is active. Consequently, the window-update stage modifies the digital values $S1$ and $S2$ of V^+ and V^- using two identical accumulators. Precisely, when V^+ level is crossed, accumulators' outputs are incremented by 1. Therefore, V^+ and V^- are also shifted by a factor q defined in (3.2) where FS is the LC-ADC full scale and M is the DAC's resolution. In the opposite situation, accumulators' outputs and the reference levels are decreased by 1 and q, respectively.

$$q = \frac{FS}{2^M} \tag{3.2}$$

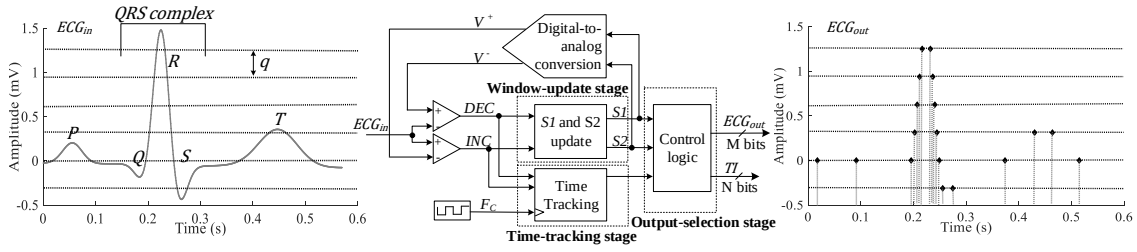


Figure 3.7 – LC-ADC architecture.

The *SNR* expression of the LC-ADC is given in (3.3) where $P(ECG_{in})$ is the power of the input signal, $P(dECG_{in}/dt)$ is the power of the input signal's derivative with respect to time t, and F_C is the counter clock frequency [51].

$$SNR = 10log_{10}\left(\frac{12P(ECG_{in})}{P(\frac{dECG_{in}}{dt})}\right) + 20log_{10}(F_c) \tag{3.3}$$

In this expression, the *SNR* is a function of the properties of the input signal and the counter clock frequency and does not depend on the LC-ADC resolution unlike conventional ADCs. Doubling F_C leads to a 6-dB increase of the *SNR*. Ideally, infinite increase of the counter clock frequency leads to an infinite increase of the *SNR* ...

We mainly focused on the LC-ADC design parameters for ECG sampling. It is based on the choice of the full scale, FS, the counter clock frequency, F_C, the counter resolution, N, and the quantization step, q. The quality of the reconstructed ECG was our metrics. We used temporal signal-to-distortion ratio (S/D) which is widely used in this application [52] as given in (3.4) or the percentage root-mean-square difference (PRD) as in (3.5).

$$S/D = 10log_{10}\left(\frac{\sum_{n=1}^{L}\left(ECG_{in}(n) - \overline{ECG_{in}}\right)^2}{\sum_{n=1}^{L}\left(ECG_{in}(n) - \widehat{ECG}_{out}(n)\right)^2}\right) \tag{3.4}$$

where ECG_{in} is the vector of L samples which models the input analog signal, $\overline{ECG_{in}}$ is the mean of ECG_{in} vector and $\widehat{ECG}_{out}$ is the reconstructed signal.

$$PRD = 10^{-\frac{S/D}{20}+2} \tag{3.5}$$

Signals with *PRD*s lower than 9 %, respectively with S/Ds higher than 21 dB, are good quality signals and can be medically interpreted. Thus, the optimal choice is the 8-bit resolution and using equation (3.2), the quantization step is equal to 39.1 μV. Specifications are detailed in Table 3.2. We designed the LC-ADC as presented in Fig. 3.8 following the methodology presented in Fig. 3.9.

Specification	**Value**
Maximal slope	290.6 mV/s
Minimal slope	0.0962 mV/s
Dynamic range	[-5,5] mV
Bit resolution	8 bits
Counter clock frequency	10 kHz
Counter resolution	12 bits

Table 3.2 – LC-ADC design parameters.

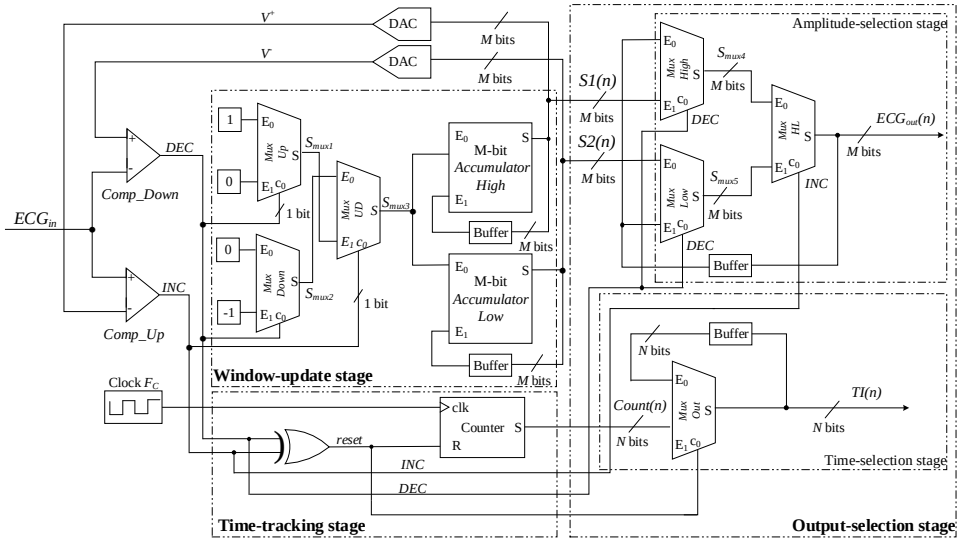


Figure 3.8 – Block diagram of the LC-ADC.

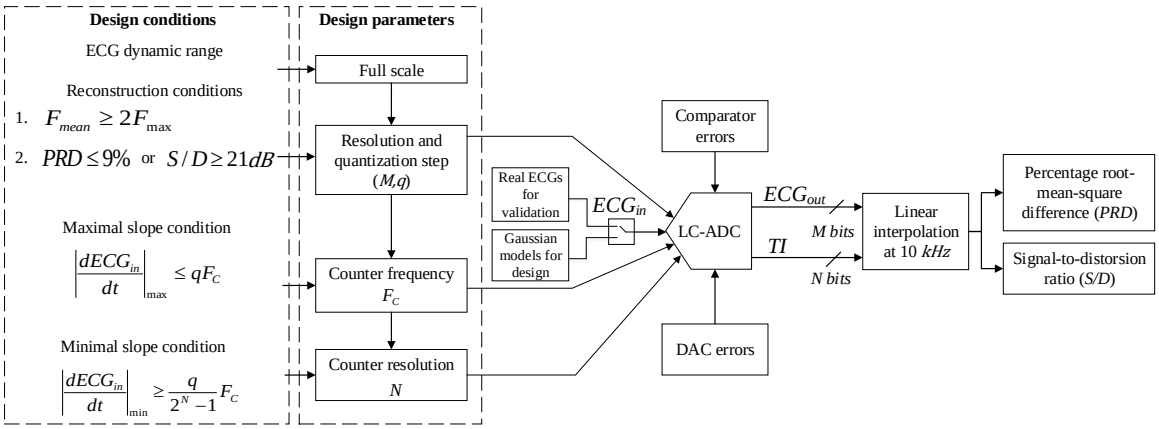
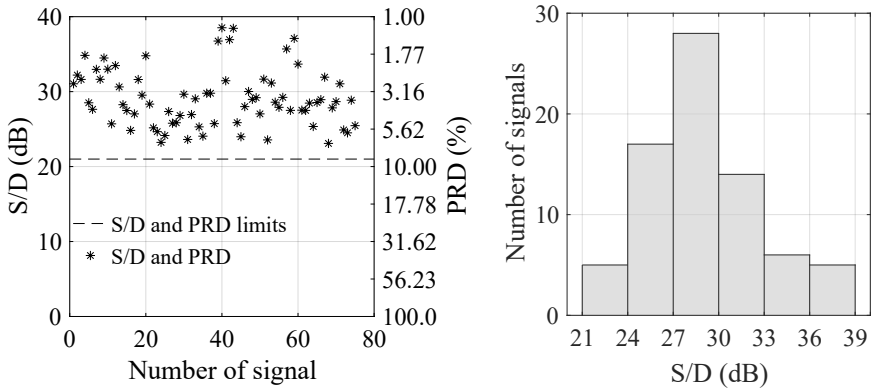


Figure 3.9 – LC-ADC design and evaluation methodology.

Simulations

The designed LC-ADC model was simulated by evaluating 75 real ECG records from Physionet databases. The test signals are chosen with different shapes, amplitude ranges, slopes and pathologies to assess robustness of the LC-ADC against ECG waveforms variations [44]. Fig. 3.10.a gives simulation results. The converter achieves S/D and PRD values that vary from 23 dB to 38.52 dB and from 1.18 % to 7 %, respectively, which reflect good signals' quality. Furthermore, the distribution density of these results, given in Fig 3.10.b, shows that 71 % of the converted signals have S/D at least 6 dB higher than 21 dB.



(a) S/D and equivalent PRD variations.

(b) Histogram of S/D values.

Figure 3.10 – LC-ADC simulation results using 75 real ECG records.

We have included analog components' errors in the LC-ADC model and simulated using the same ECG signals. The highest degradations in terms of S/D and its equivalent *PRD* are obtained for the highest simulated offset voltages when added to both comparators as summarized in Table 3.3. As a matter of fact, good signal quality is maintained with values of the S/D and *PRD* ranging between 23.74 dB to 34.47 dB and from 1.89 % to 6.5 %, respectively.

We have enriched the LC-ADC model with DACs non-linearities using a polynomial function of degree, d, which generates voltages shifted by at most $\pm mq$ from the ideal values with m equal to 1. The polynomial function was defined in [53], with the extraction of the maximal and minimal errors, INL_{max} and INL_{min}. The function was designed as accurate but minimized as possible to lower the complexity of the DAC's model. Finally, the retained degree to model the non-linear function of the DAC is d=8.

We analyzed the impact of non-linearity errors on LC-ADC performances for identical DACs by measuring the maximal differential non-linearity, $|DNL|_{max}$. Table 3.4 summarizes the highest computed S/D and *PRD* degradations regarding the time-quantization based LC-ADC model results. S/D degradations

Signal	**S/D** (dB)	**S/D degradation** (dB)	**PRD** (%)	**PRD degradation** (%)
ECG3	29.05	2.45	3.53	0.87
ECG9	32.85	1.65	2.27	0.39
ECG27	23.74	1.76	6.50	1.20
ECG42	34.47	2.46	1.89	0.47
ECG52	32.58	4.19	2.35	0.90
ECG63	26.09	2.41	4.96	1.20

Table 3.3 – LC-ADC simulation results with offset voltage errors equal to 0.25 of q.

Signal	S/D (dB)	S/D degradation (dB)	PRD (%)	PRD degradation (%)	$\|DNL\|_{max}$ (mV)
ECG3	27.30	4.20	4.30	1.64	0.182 q
ECG9	25.17	9.33	5.51	3.63	0.159 q
ECG27	20.11	5.39	9.87	4.47	0.182 q
ECG42	32.50	4.43	2.37	0.95	0.36 q
ECG52	31.35	5.42	2.70	1.25	0.182 q
ECG63	21.54	6.96	8.37	4.61	0.182 q

Table 3.4 – LC-ADC simulation results with non-linearity errors in the interval $\pm q$.

vary from 4.2 dB to 9.33 dB which are equivalent to PRD degradation values from 0.95 % and 4.61 % where $|DNL|_{max}$ is lower than 0.36 q. Only one tested signal has almost good quality due to non-linearity errors with S/D approximately 1 dB below the minimal limit of S/D and a PRD value slightly above 9 %.

Perspectives

All the blocks have been designed using 0.18μm CMOS technology from UMC but the circuit was not fabricated. The evaluated performances in simulation pave the way to relevant real measurements of ECG signals with a low power consumption and robustness against analog components' errors.

3.3 IBC using Ultrasounds - UTRx

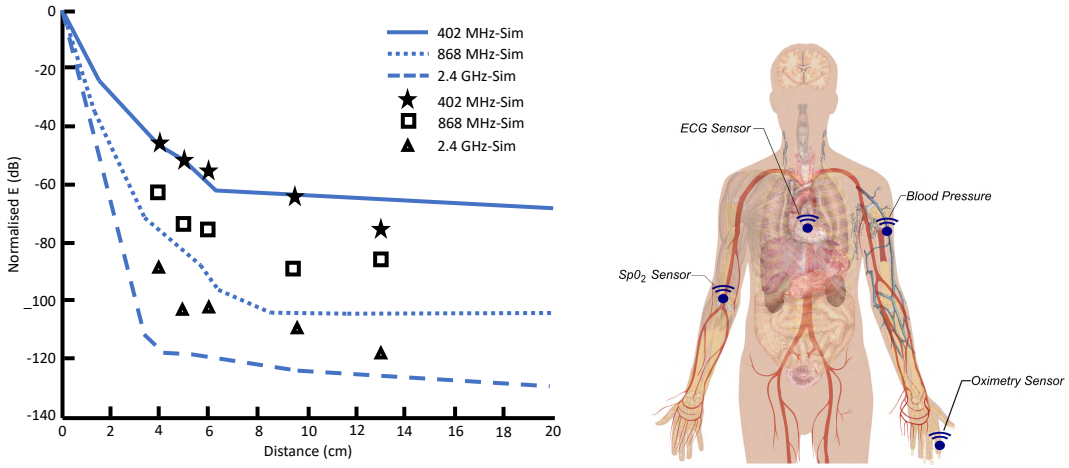
This work was initiated by remarks on Wireless Body Area Network (WBAN). It is used for wireless health monitoring and WBAN technology envisions a network of continuously operating sensors, which measure critical physical and physiological parameters such as heart rate or glucose concentration. Wireless connectivity in WBAN technology is key to its success and despite RF technology has been successfully deployed in most WBAN implementations, the latter consume a lot of battery power and have security issues, and the frequencies of interest are not at all suited to propagate in a body.

Thus, we jeopardize RF communications for health monitoring and we have started investigating ultrasounds has a good candidate for wireless communication in the body. We propose to design an ultrasound transceiver (UTRx) for IBC. This work has been initiated in collaboration with Victoria University in Australia [54] [55] [56].

Concept

We propose IBC as an alternative to WBAN. The human body is composed of 60 to 70% of water. Water is not at all compliant for propagation of neither high frequency electro-magnetic waves nor light waves as depicted in Fig 3.11(a). Human body modeling covers various levels of heterogeneous modeling. The granularity found in the literature starts from the skin to complex models involving muscles,

bones, veins. It presents experimental measurements of the frequency and time domain responses in order to investigate the transmission characteristics of the human body as a conductor. On the other hand solely high frequencies are considered, as they are known to efficiently propagate in the air, while they are unsuited to propagate within the body. That is why we propose ultrasounds as IBC in the human body as the signal propagation medium to create a network of sensors (cf. Fig. 3.11(b)). This network could collect data from all sensors and send it to a unique RF gateway node. This node will act as a 'hub', concentrating IBC and offering a wireless interface to the external world, thanks to a Near Field Communication (NFC) link or any other approach suited to the issue. Therefore, the channel used for ultrasounds wireless communications will rely on a physical vector made of flesh, blood and bones, and no longer with air, which is disruptive for telecommunications behaviors.



(a) (b)

Figure 3.11 – Electromagnetic waves absorption within human body, (a), IBC sensor network (b)

Our research aimed at investigating IBC by determining, modeling and using at its best the medium in the case of ultrasonic wave for such a link in terms of frequency, bandwidth, power consumption, and radiated power to the set up of a global in-vivo ultrasounds network.

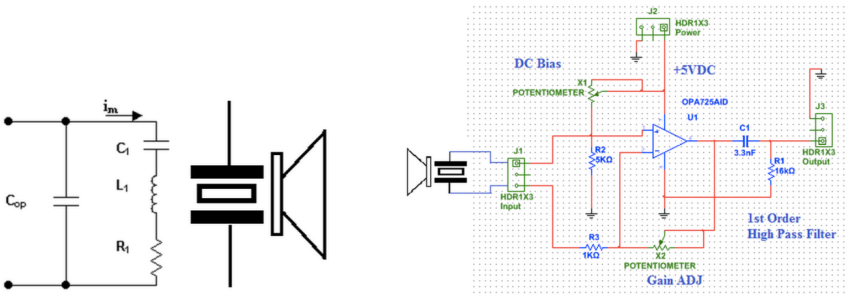
First experimental measurements

We have started our first experimentation by characterizing experimentally the propagation of ultrasounds in biological medium such as meat or cheese to better understand the paradigm IBC ultrasounds communications. We have selected several transducers in a wide frequency range, from 40 kHz to 5 MHz and then develop our test bench with a transmitter, a receiver, a meat coupler and all the required measurement tools.

Material	Density (Kg/m^3)	Speed of propagation (m/s)
Air	1.225	343.99
Water	1000	1500
Fat	937	1479
Bone (Skull)	1738	2770
Muscle	1070	1566

Table 3.5 – Speed of propagation in different material

Measurement of the speed of a wave through a biological medium requires the animal meat specimens to be cut to particular dimensions using two ultrasonic transducers placed at each of the narrow ends, Set one end as the transmit transducer (source) (cf. Fig.3.12(a)) and the other as a receive transducer (point) (cf. Fig. 3.12(b)), connect the source to a signal generate trigger monostable (pulse mode), then connect the point receive transducer to a fast recording device such as a digital storage scope.



(a) (b)

Figure 3.12 – Resonant circuit, (a), Ultrasonic Receiver circuit (b)

Fig. 3.13 exhibits the measurement setup. First measurements are performed only trough air to validate the functionality of the setup. Fig. 3.14(a)) displays the flight time measured between the transmitter and the receiver. The experiment is repeated with different distance. The average propagation speed extracted from those measurements is 343.05m/s (cf. Fig.3.14(b)), which is consistent to wave propagation through air (343.99m/s, cf. Table 3.5).

The experimental comparisons between ultrasonic and RF wave propagation involved comparing the propagation time and attenuation between the two technologies. Propagation time was taken as a measure of flight time between the leading edges of the source and point pulses through a prepared cut of pork 30x30x150mm.

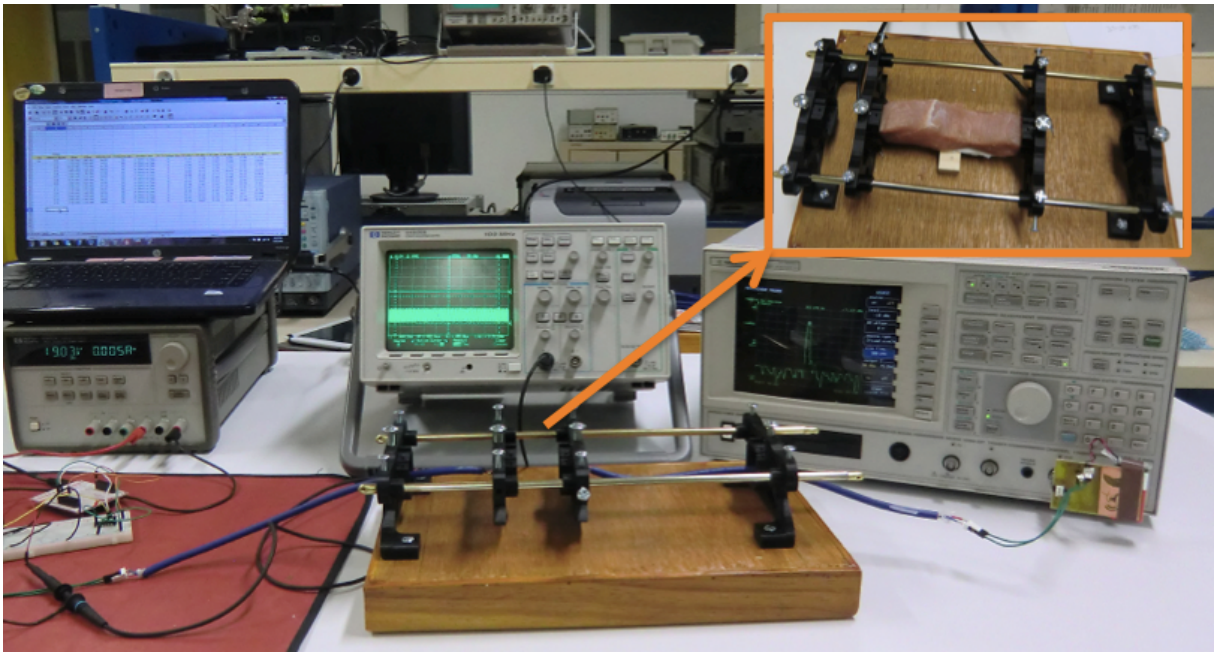
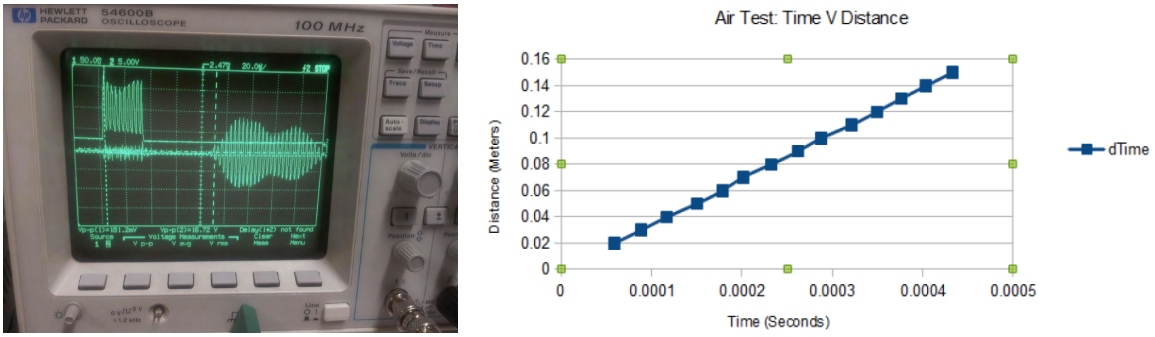


Figure 3.13 – Picture of meat in the setup measurement platform for both RF and Ultrasonic propagation analysis

The average speed of ultrasonic signal propagation of the pork meat sample was $C = 1465.91m/s$. From the published figures, the speed of propagation indicates the sample had a composition near fat $1479m/s$ and muscle $1560m/s$. Variations can be explained by the mix of fat and muscle in the meat sample.



(a) (b)

Figure 3.14 – Flight time measurement between Transmitter and Receiver (a), Extrapolation of Speed of Propagation in Air (b).

The plotted data RF vs Ultrasonic comparison is presented in Fig. 3.15). It indicates that ultrasonic transmission suffers considerable less signal attenuation than RF at 300KHz, due to the water content of the meat sample.

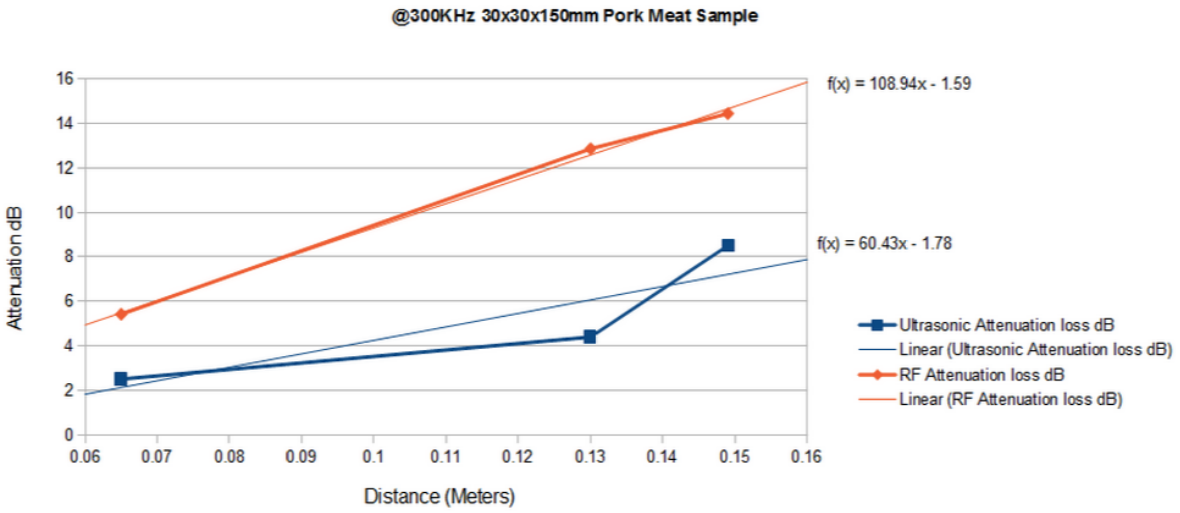


Figure 3.15 – RF vs Ultrasonic attenuation in human body in function of distance

Ultrasounds Modeling in Human Body

After measurement, we tried to find a theoretical model of a non-linear ultrasonic wave propagation to apply to Human body. We have introduced mathematical tools required to understand theoretically a non-linear ultrasonic wave propagation and detailed parameters required to simulate an ultrasonic wave propagation in biological medium with muscle as case of study.

Ultrasounds are mechanical and elastic waves. There are two types of waves:

— Longitudinal bias or compression wave: this bias corresponds to a particles displacement along the propagation axis.

— Transverse polarisation or shear wave: this bias corresponds to a particles displacement perpendicular to the propagation axis.

We have decided to only consider longitudinal waves as explained in [57]. By solving and understanding waves propagation equations, we have extracted the acoustic pressure and a specific acoustic impedance. Consequently, two fields of wave propagation can be identified: the far field and the near field such as depicted in Fig. 3.16).

Simulation results provided in Fig. 3.17 allow to identify the near field and the far field. The location of the last maximum of this curve is usually taken as the limit between the near field and the far field. We have assumed that it is the most suited trade-off in terms of distance to receive or transmit a signal because of its maximum of magnitude. In the far field, fluctuations vanish and side lobes appear (cf Fig. 3.18). We can deduce the propagation channel width which is, for a 10MHz transmitter with $1cm$ radius, $2.3cm$.

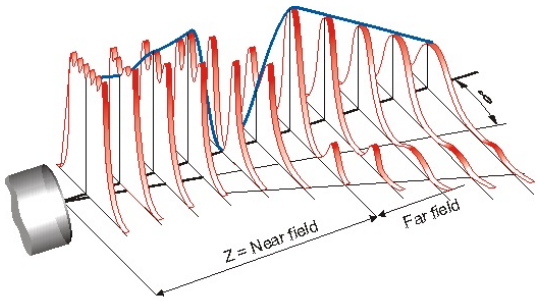


Figure 3.16 – Near Field and Far Field

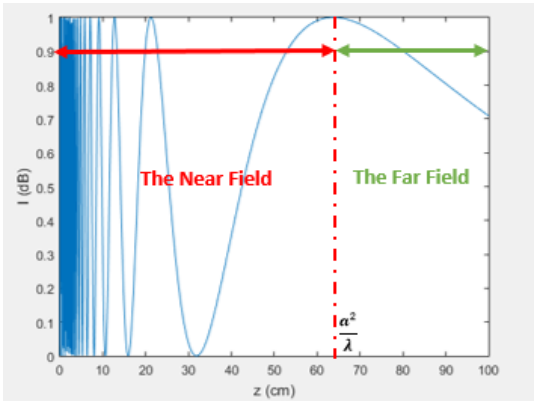


Figure 3.17 – The axial intensity as a function of distance in the vicinity of a vibrating transmitter

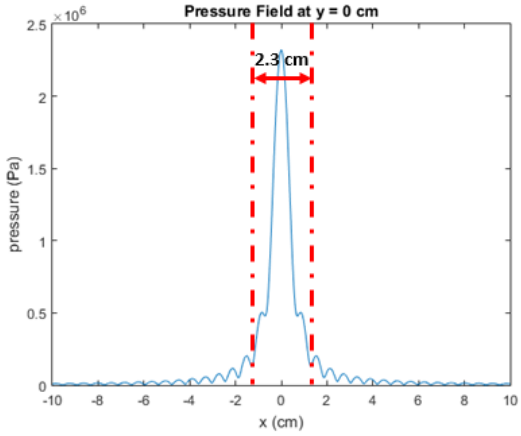


Figure 3.18 – Modeling of side lobes of ultrasonic wave in the far field ($f = 10MHz$, $\beta = 1.09$, $a = 1cm$, $c = 1569m.s^{-1}$, $z = 50cm$)

We have enriched the model by considering a propagation in homogeneous and isotropic medium with the case of study of muscle. Muscle is characterized by different parameters such as velocity, absorption coefficient and volumetric mass density. The transducer is defined by its radius, its form and its bend. All of these parameters are defined in Table 3.6.

Most modeling software suffer from errors and mismatching in the near field and especially at the transducer interface. The Michigan State University has developed a software, FOCUS, which performs calculation very quickly with the same accuracy than the other softwares [58]. Simulation results are exhibited in Fig. 3.19. FOCUS allows us to identify easily near field and far field in muscle and depict the presence of side lobes.

Emitter		Medium	
shape	circular	**c**	$1569 m.s^{-1}$
radius	$6.5 mm$	α	$1.09 dB.cm^{-1}.MHz^{-1}$
bend	0	ρ	$1.184 kg.m^{-3}$

Table 3.6 – Characteristics of the transmitter and muscular medium

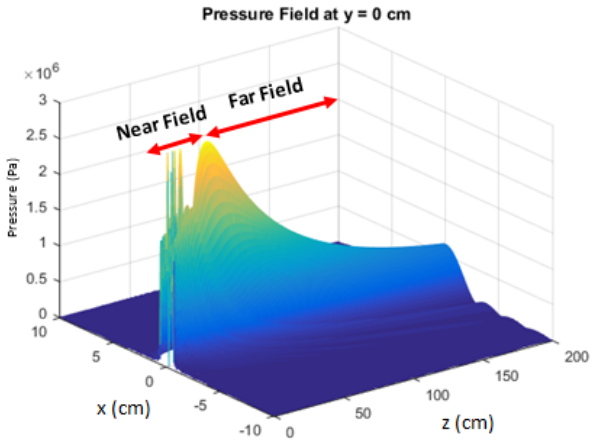


Figure 3.19 – Modeling of ultrasonic wave propagation in muscle ($f = 10MHz$, $radius = 1cm$)

Second experimental measurements

An experimental protocol has been established in order to measure near field and far field in muscle (here a piece of meat used as phantom). We have designed a bench with a transmitter placed in a fixed position and a receiver placed on a mobile platform, which can be adjusted in the X and Z directions (cf. Fig. 3.20). This platform can move by step of $1\mu m$. Measurements are performed through air to validate the correct operability of the setup (cf. Fig. 3.21). We used a $40kHz$-transmitter and receiver. The frequency of $40kHz$ was chosen to highlight easily the exponentially attenuation of the pressure. The measurements results are plotted in Fig. 3.22. It shows the frontier between the two fields and the presence of side lobes in the far field.

Perspectives

At this day, we have gathered a sufficient amount of data to setup more advanced research. A PhD work is under its way to design a Transmitter-Receiver front-end for an integrated ultrasonic transducer. It will be part of a project detailed in section 4.2.

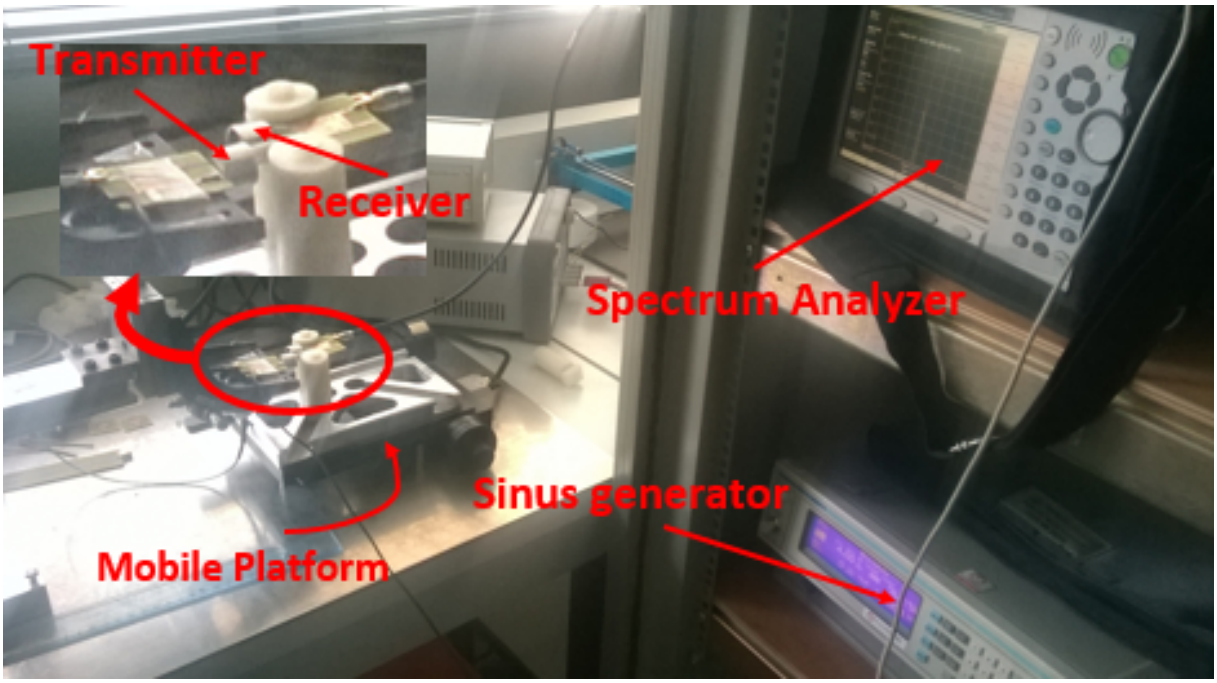


Figure 3.20 – Setup measurement platform for Ultrasonic propagation analysis

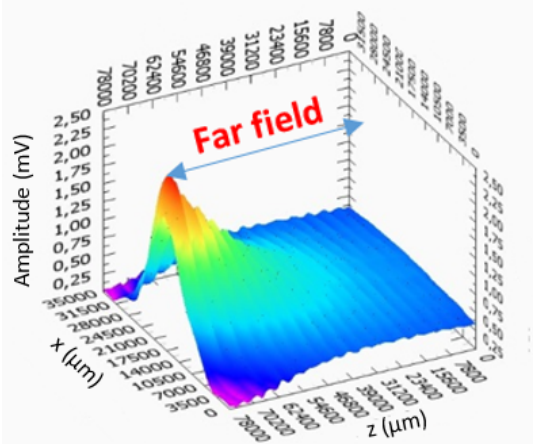


Figure 3.21 – Experimental measurements of an ultrasonic wave propagation in air ($f = 40kHz$, $radius = 6.5mm$)

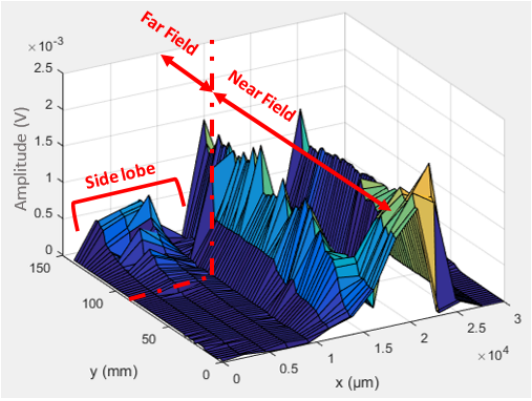


Figure 3.22 – Experimental measurements of an ultrasonic wave propagation in muscle ($f = 40kHz$, $radius = 6.5mm$)

3.4 Conclusion

This chapter presented our research on IBC. We have investigated several parts of electronics that are brought into play in the Human body. First, an interface for an embedded sensor was designed to achieve the conversion from the bio-signal to its transmission by RF. We have reduced the power consumption by proposing a pure analog system for a direct conversion, avoiding any digital signal processing. Then, we worked on ECG and its mathematical representation to adapt an analog-to-digital architecture to the sparsity nature of this signal. It allowed us to optimize the power consumption while keeping good performances. Finally, we jeopardized the RF link itself for communications within the body. We have demonstrated that ultrasounds are a relevant solution for in-vivo communication. Altogether, the 3 sides of electronics for IBC have been covered: **bio-signal properties, conversion and propagation**. It paves the way of disruptive systems investigations applied to **health monitoring**.

CHAPTER

4

RESEARCH PROJECT

Sommaire

Chapter 4 presents a research project in analog circuit design for the coming years. In a first part, we propose to keep on investigating in RF systems design with 2 main focus: a complete transceiver using the Walsh generator and a transmitter dedicated to high frequencies using Hilbert Transform. In a second part, we propose to work on the miniaturization of an ultrasound implant to can communicate within the Human body and be part of a ad-hoc IBC network. Finally, we propose directions to longer term researches on analog signal processing for edge computing with the example of IoT (or any low-power communicating device) or image sensors.

Key words: Walsh generator, wide-band N-path filters, Hilbert transform, mmW direct conversion, digital pre-distortion, IBC network, ultrasonic transducers.

4.1 New perspectives in RF systems design

RF circuits are limited by the technology when one can consider integrating in a downscaled technology or an optimized one. The idea is to keep on investigating on system level innovation. Our goal is to propose systems that achieve:

— frequency agility. We are looking for a dynamic and instantaneous access to several bands in a very wide spectrum, from DC to several GHz, whatever the repartition, the number and the width of the bands.

— high frequency bandwidth. We are looking to access to high part of the spectrum, over 100GHz, without relying on complex architectures.

4.1.1 Versatile RF transceiver solution

5G communication will offer to users' high peak data rate by accessing more and more carrier frequencies in the 1.8 – 3.6GHz bands and then in the 1.8 – 6GHz bands. The mmW bands will be a complementary solution to get higher data rate transfer but will not replace the sub-6GHz bands. For sub-6GHz bands, the solution to give high peak data rate users' experience will be an efficient carrier aggregation. The main challenge is to keep power consumption reasonable for mobile handsets. Analog-Digital (AD or DA) interfaces are the technological bottlenecks in a transceiver system when considering multi-standards, resolution, speed, integration and power consumption constraints. Nyquist AD and DA

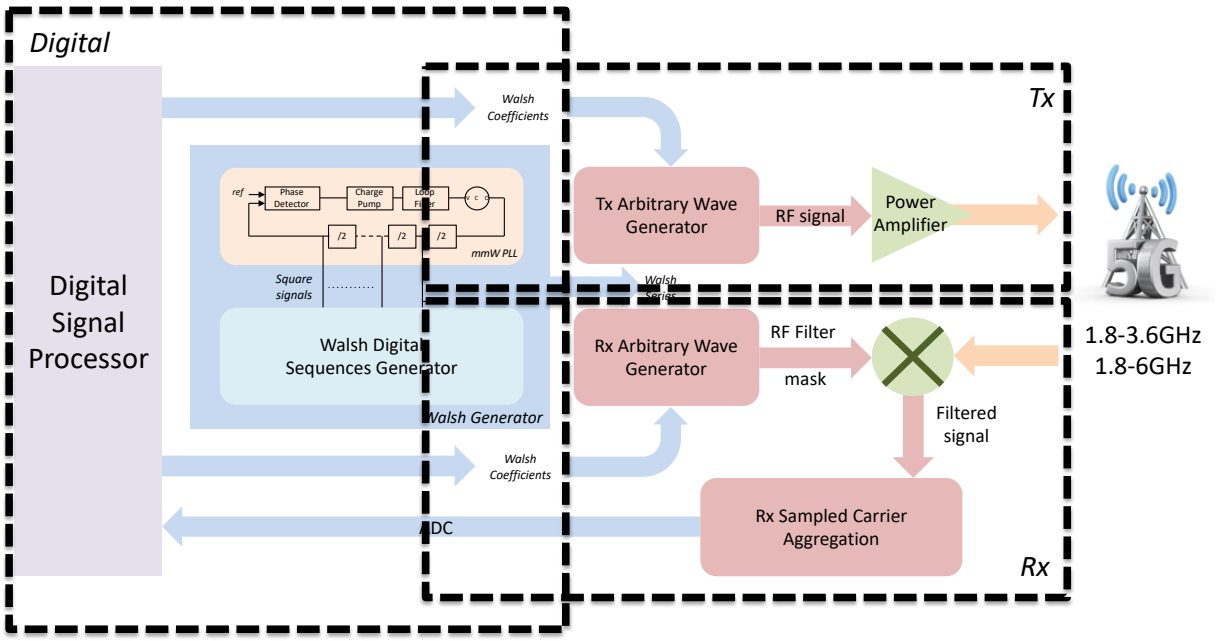


Figure 4.1 – 5G Transceiver using Walsh generator as a core

converters and RF conditioning are the functions to stay focused on even if the high-speed digital signal processing and medium access processor remain hard to design with a low-power budget while FDSOI technologies offer a new CMOS scaling opportunity and leakage management.

We propose to develop a low-power high-data rate transceiver integrated in nanoscale FDSOI CMOS technology to answer to 5G requirements discussed above (large frequency range; multi-carrier; high resolution; high speed; integration and low-power consumption) using Walsh series and compressed sensing approaches. It will be used to redefine the conversion, the amplification and the reception of RF signals at the system level.

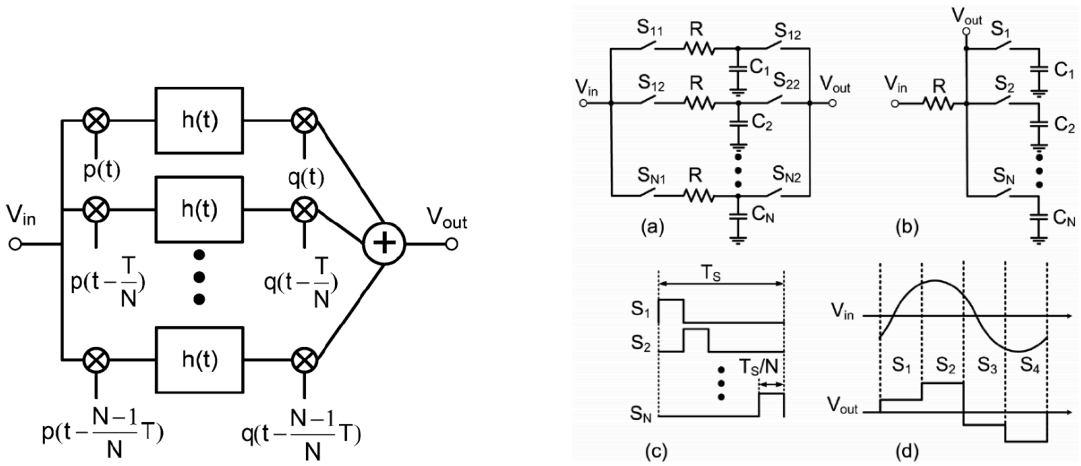
This system is composed of a Walsh generator as a core used either for transmission (Tx) or reception (Rx). We propose the design of a 5G RF transceiver using Walsh series to release the best performances provided by the 28nm FDSOI CMOS technology as depicted in Fig. 4.1.

Receiver: N-path Walsh Rx

Our goal is to select several channels at a time in a very wide spectrum. We need to filter the desired signals and to reject the strong signals in order to avoid blocking of the receiver. It can be compared to a bank of filters with very high linearity, very high compression point and very high Q (e.g. for 10 MHz bandwidth around 500 MHz). Although off-chip passive filters provide these properties, the trend is to

integrate it in CMOS alternatives for reasons of size and cost. LC filters cannot be considered as they provide a limited tuning range and low Q.

Alternative tunable filters without inductors based on periodically time variant networks have been investigated in literature under different names such as N-path filters, sampled data filters, commutated capacitors such as in [59] and depicted in Fig. 4.2(a). Prof. Bram Nauta and Prof. Eric Klumperink have revamped the concept in the 2010's by integrating continuous-time switched capacitor N-path filters for RF applications detailed in [3] and [60] following the basic schematic depicted in Fig. 4.2(b). They have kept on improving the concept over the years [9] to reach excellent performances in terms of blocker rejection, NF, power consumption. Their work inspired the RF community all over the world. Nevertheless, the concept remained limited to a single band without any degree of flexibility.



(a) (b)

Figure 4.2 – (a), Architecture of an N-path filter (p and q are the mixing functions and T is the period of the mixing frequency). (b), (a) Switched-RC N-path filter. (b) Single port, single ended N-path filter. (c) Multiphase clocking. (d) Typical (in-band) input and output signal.

We propose to investigate a tunable filter that display an on-demand mask. It relies on both N-path filter concept and Walsh series. Fig. 4.3 presents the principle of filtering using a mask in both time and frequency domain.

— In the frequency domain, filtering is the multiplication between a mask and an input RF signal,
— In the time domain, the mask is considered as a pseudo periodic signal, thus, this signal is convolved with the input RF signal. The result of the convolution is the RF filtered signal.

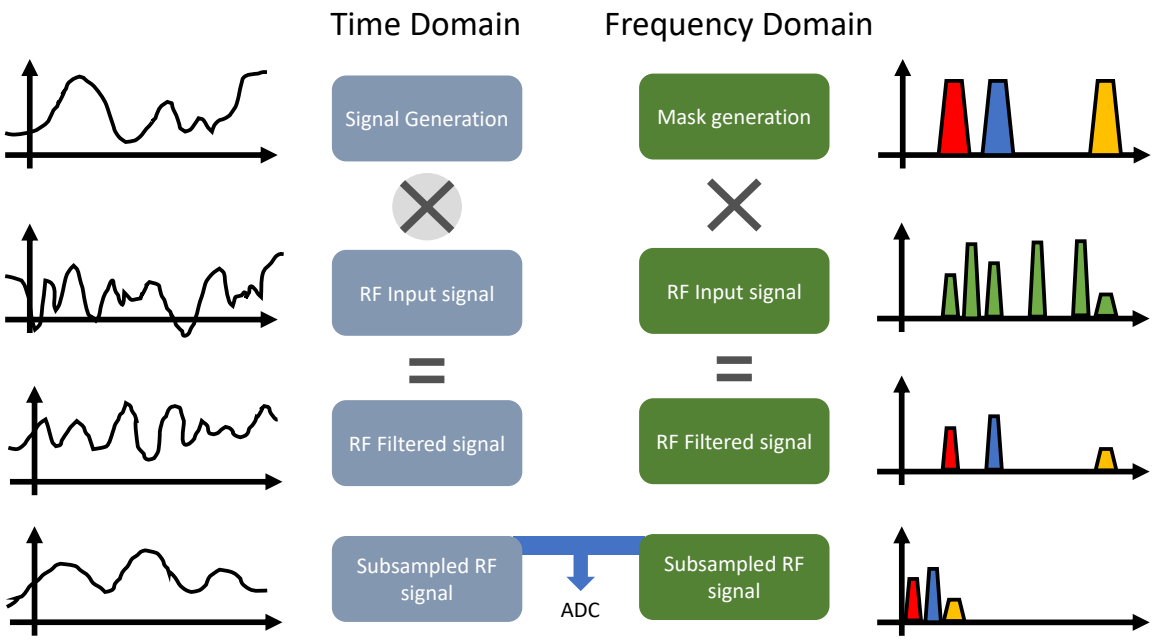


Figure 4.3 – Time and Frequency domain principle of on-demand filtering

The concept is to generate the mask using Walsh series. Fig. 4.4 presents the system that perform the convolution. It is composed of 3 parts:

— The Mask generator. It is based on a Walsh generator which uses Walsh sequences controlled by a PLL as in described in Chapter 2.2.2. The Walsh series are used to switch a set of N-path filters,

— The N-path filters. We display a series of N-path filters. Each of them receive a Walsh series that is delayed by one period from one N-path to the other one. At each period, every N-path filter load a capacitor or not, that means that each N-path filter will reproduce a frequency mask of every Walsh series,

— Mask coefficients. All the Walsh series masks applied to N-path filters are added together and weighted. It os controlled by binary words that can be set to adjust the mask on demand. The coefficients are similar to the Walsh ones and thus finalize the filtering operation.

We have performed high level simulations using MatLab to validate the architecture. We focus our simulations around a central frequency (here $f_c = 2\ GHz$). Fig. 4.5(a) presents the Fourier transform of the mask, i.e. the selected channel. Fig. 4.5(b) presents the RF filtered signal with a sweep of RF input signal frequency from 1.95 GHz to 2.05 GHz with a 10 MHz-span. We can notice they are all filtered following the mask which means that only the channel is selected. Also, some out-of-band side-lobes frequencies are amplified at $2 - GHz$ but remain at a low and acceptable level.

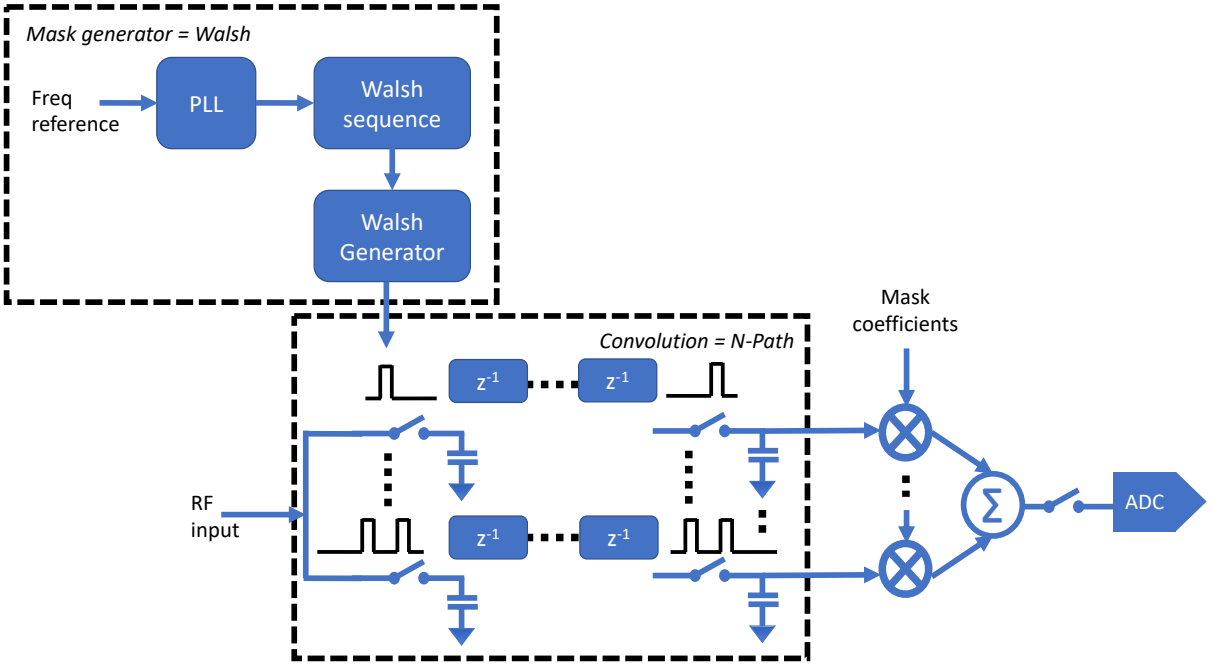
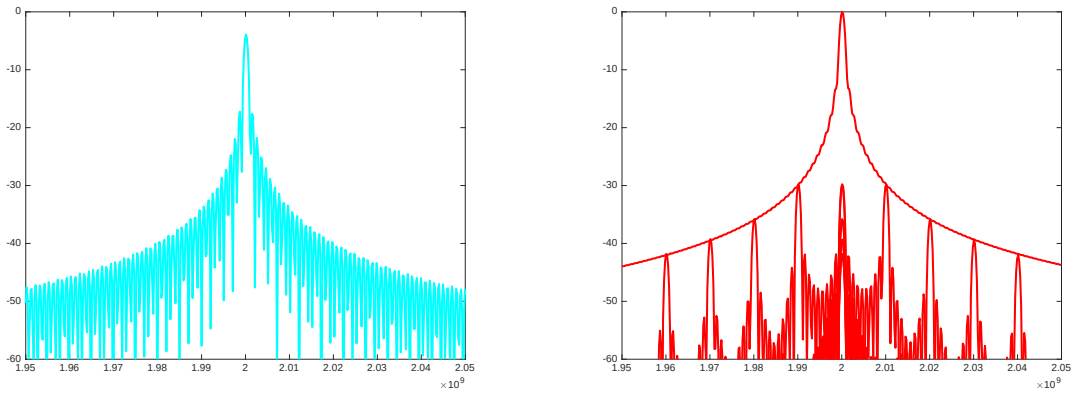


Figure 4.4 – Principle of a Walsh N-path filter



(a) (b)

Figure 4.5 – (a), Mask used for a single channel at 2 GHz (b), RF filtered signal with a swept RF input signal from 1.95 GHz to 2.05 GHz with a 10 MHz-span

Transmitter: Walsh-enhanced Power Amplifier

A collaboration with the Hyper-Frequency Circuits and Systems (CSH) would be the best way to investigate the use of Walsh series in PA design. We target to design a fully integrated transmitter using the Walsh generator and a RF PA. The research will be about the design methodology and the architecture to address the principle presented in Fig. 4.6 and detailed as follows:

— The Walsh generator delivers digital sequences to a digital beamformer to adjust dynamically the phase of the generated signal,
— The Walsh generator delivers the coefficients to weight every Walsh series during their amplification within a set of broadband drivers. A digital pre-distortion can be done on the coefficients to improve the RF PA performances,
— Sequences pre-amplified by the broadband drivers using the coefficients are summed together and amplified by a Power Stage.

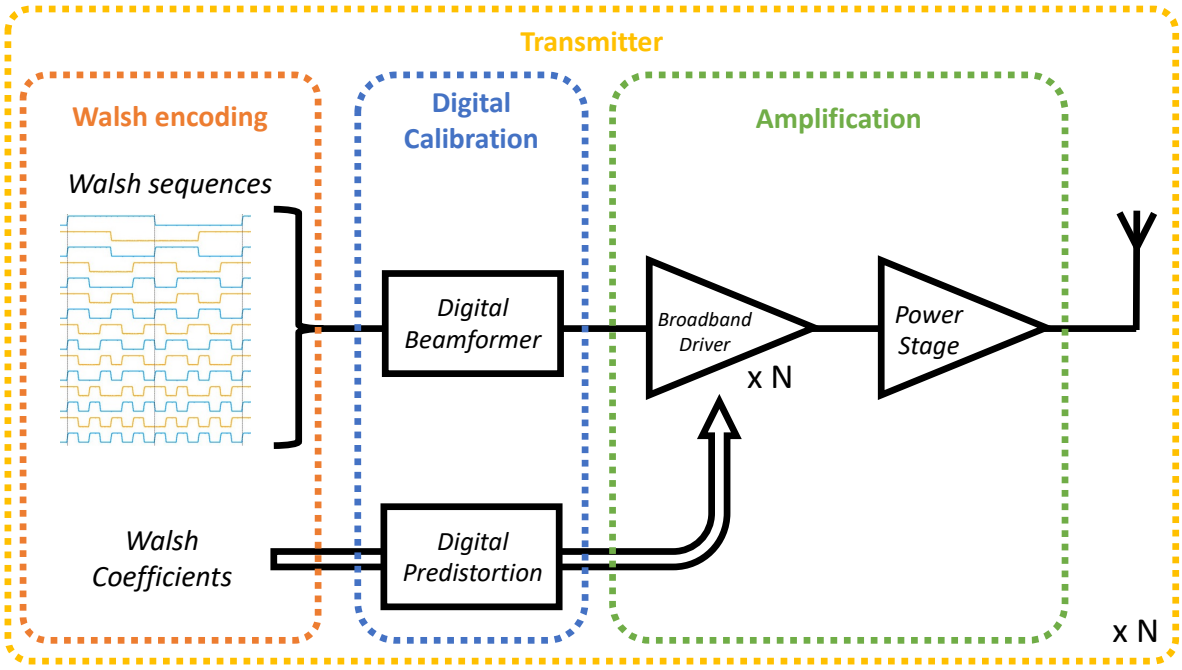


Figure 4.6 – Walsh-enhanced Power Amplifier

Modeling would be an interesting part of this research as Walsh series impose to re-visit the PA behaviour model to then work on the pre-distortion. Our target is to implement the digital pre-distortion (DPD) directly in the generator to modify the Walsh coefficients to improve the linearity of the non-linear RF PA. That solution permits to enhance the efficiency and the power consumption of the PA working in a non-linear operating class, and also strongly improves the linearity required for the 5G complex modulation. To do so, the non-linear behavior of the PA is modeled to then update the Walsh coefficients.

This innovative solution can highly decrease the power consumption comparing with the classical DPD existing solutions. We could improve by 33% the Tx amplification (linearized PA) consumption. An intersting idea would be to determine if it can be done dynamically. Thus, we need to work on a PA

model by identifying the non-linearities and then determine how the Walsh coefficients can be corrected in the generator (Walsh generator + PA co-integration). The Walsh coefficient correction could be done dynamically in function of the PA variation over the time such as a calibration step to determine a first set of coefficients (initialization step) and then, the Walsh predistortion associated with a DPD or/and a feedback loop to adjust dynamically the Walsh coefficient (Walsh Flexible Predistorsion PA).

4.1.2 Access to high frequencies: Hilbert Tx

Accessing to high frequencies is facing to system level technological bottleneck. It requires upconverting large bandwidth from base band (GHz wide) to frequencies above 100 GHz. We believe that next generations of telecommunications will be local, short range and high data rate. The concept is to bring data by wireline access up not only to its last mile but its last hundred of meters. Thus, the most adequate part of the spectrum (cf. Fig. 4.7) is between 118 GHz (O_2 absorption frequency) and 183 GHz (H_2O absorption frequency) with a minimum at 150 GHz. mmW architectures would use mixers, filters and various analog, digital or mixed building blocks to achieve specifications. We propose a disruptive point of view with a direct conversion from base-band to mmW frequencies with a reduced analog circuitry.

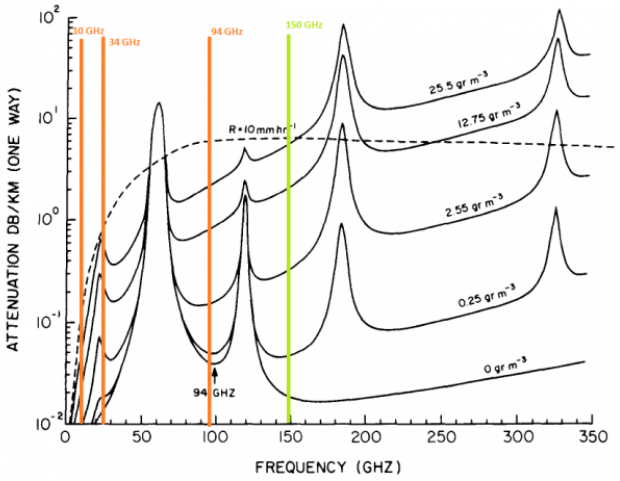


Figure 4.7 – Attenuation in dB/km from 0 to 350 GHz

Our conversion scheme is to consider generating an negative-frequency-less base-band signal so upconversion won't require any more filter or dedicated circuitry to reject its image frequencies. The Hilbert Transform is the mathematical operation (cf Eq. 4.1 and Eq. 4.2) that displays a signal without any negative frequency. For instance, if we consider a pure sine-wave, such as $x(t) = cos(2.\pi.f_c.t)$, the Hilbert transform is $H(t) = sin(2.\pi.f_c.t)$ and analytical signal is consequently $X(t) = cos(2.\pi.f_c.t) + j.sin(2.\pi.f_c.t)$. Fig. 4.8 associates the signal to its Fourier transform and as one can see, the analytical signal has no negative frequency.

$$Z(t) = x(t) + j.H(x(t)) \tag{4.1}$$

$$H(t) = x(t) * \frac{1}{\pi.t} = \frac{1}{\pi}\int_{-\infty}^{+\infty} x(t).\frac{1}{(t-\tau)}\,d\tau \tag{4.2}$$

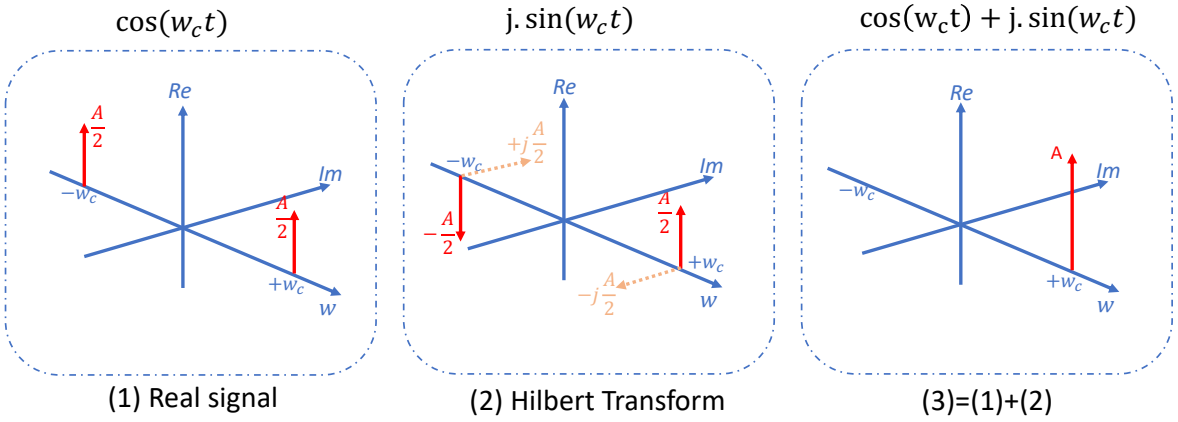


Figure 4.8 – Illustration of a Hilbert Transform

Based on the Hilbert Transform operation, we propose the system depicted in Fig. 4.9 for its the analog version. It works as follows:

— a base-band signal is generated digitally. It is converted from digital to analog,

— the signal is loaded in a sampled delay line with a given lengh of N samples and a sampling period of T_s,

— the stored samples in the delay line are convoluated with the discretized function $\frac{1}{\pi.t}$ and out of phase of $\pi/2$,

— both signals are summed to give the complex representation of the analytical signal. Both real and imaginary part are splitted in phase and amplitude to control a mixer. The mixer also receives the mmW carrier frequency provided by a Local Oscillator.

Fig. 4.10 presents the digital version where all the signal processing is performed digitally and the mixer is monitor digitally by both converted phase and amplitude. The architecture was simulated in MatLab for a proof of concept. Fig. 4.11(a) depicts the Hilbert transform on a single band. One can notice the rejection of $-30dB$. Fig. 4.11(b) depicts the same transform but using a 5G scheme with 3 channels to demonstrate the image rejection over large bandwidth.

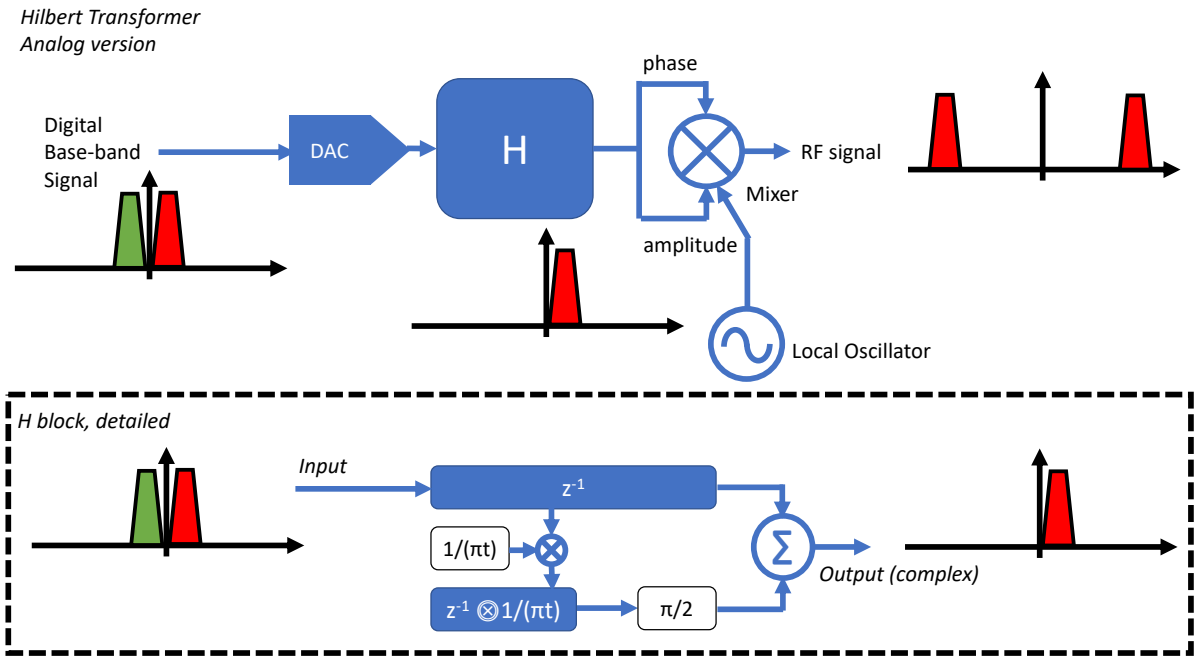


Figure 4.9 – Principle of the Hilbert generator (analog version)

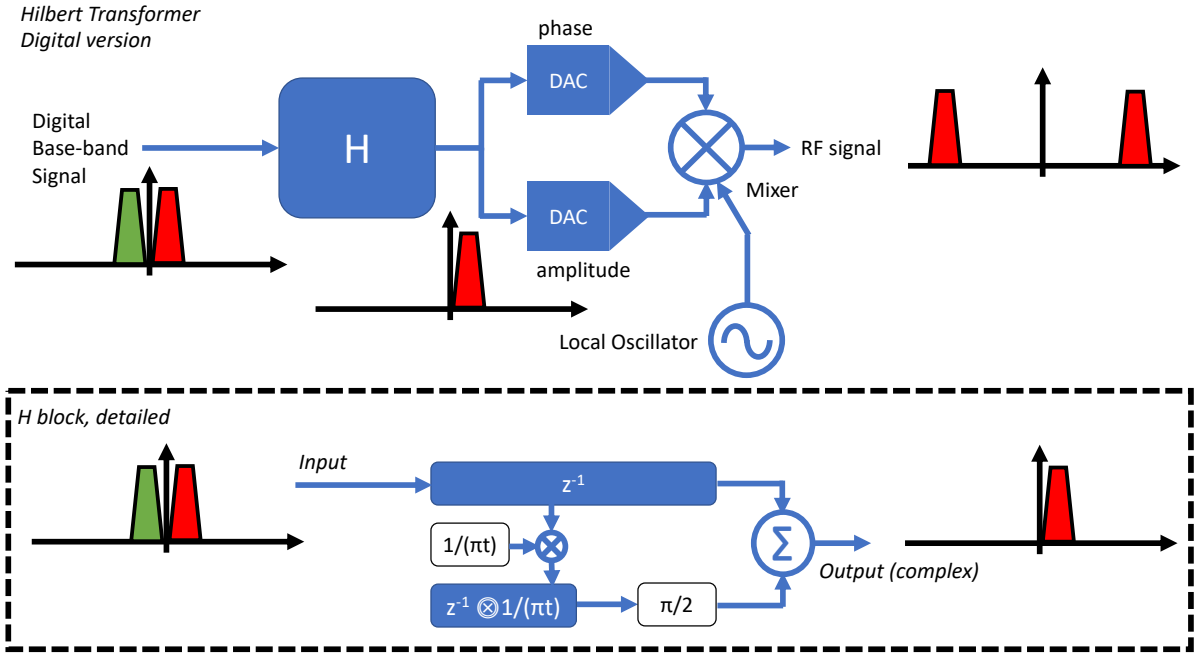
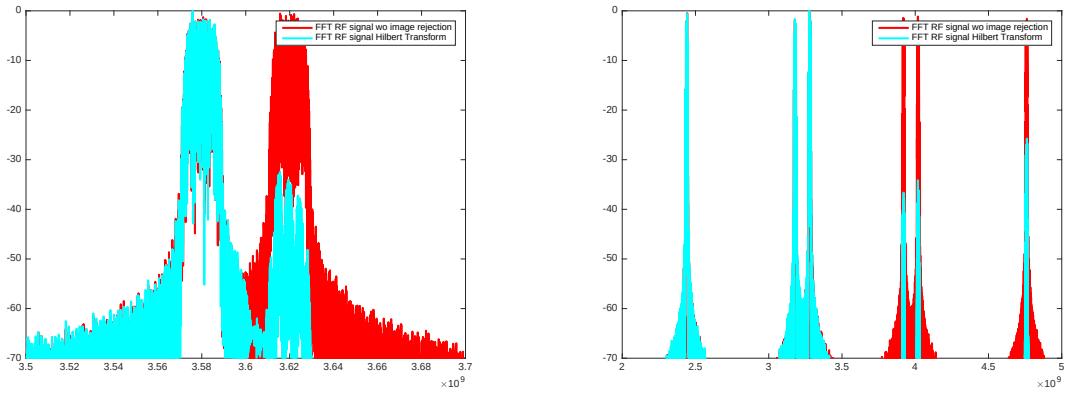


Figure 4.10 – Principle of the Hilbert generator (digital version)



(a) (b)

Figure 4.11 – (a), RF spectrum of an upconverted 5G scheme without image rejection and with Hilbert transform (b), RF spectrum of an upconverted 5G scheme with Hilbert transform

The rejection will depend on the accuracy of the Hilbert transform. It is defined by the length of the delay line and thus, by the discretized function $\frac{1}{\pi.t}$. It is determined by the minimum value that can be used for this function as depicted in Fig. 4.12. Based on the quantum q, we can extrapolate the N voltage samples required for the transform and depending on the frequency to address, the time required to process the transform. This time must be compatible with the maximum latency of the system, i.e. $\leq 1\mu s$.

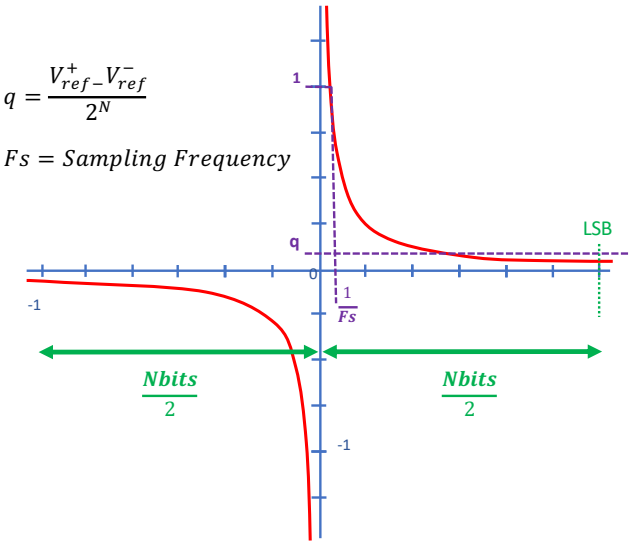


Figure 4.12 – Trade-off between image rejection and Hilbert transform length

Our investigations will be first at the system level to determine the most relavant architecture integration (digital, analog or mixed). Then, once the principle is physically demonstrated, for instance at lower frequencies compared to the hundreds of GHz ones, we will focus on the analog building block such as the frequency synthesis and the mixer. This work will be done within the Circuits and Systems (CAS) research team that gathers all the required expertise.

4.2 An ultrasound-based network for Intra-Body Communications

We have demonstrated that ultrasonic communications in a biological media is twice as effective as radio-frequency links. We propose to develop a miniaturized system to form a communication network in the Human body. This system consists of integrated devices with dimensions less than one millimeter, limited to frequencies below the MHz with dedicated modulations and with a very low power consumption (less than the hundred of μW). This system is composed of several parts as depicted in Fig. 4.13:

- an ultrasonic transducer, known as Micromachined Ultrasound Transducer (MUT),
- a dedicated integrated circuit (ASIC) for conversion and signal processing,
- a dedicated modulation technique to encode the information of a sensor, here full duplex and robust enough to body noise,
- a dedicated power supply, either mechanical, chemical or electrical,
- a sensor that will be customized depending of the desired functionality.

Several questions are tackled to lead those investigations on the 3 levels: MUT, ASIC and modulation.

We need to determine the MUT specifications: its type, either pMUT (piezzo) or cMUT (capacitive), its resonance frequency, the bandwidth, the necessary transmitted pressure, the reception sensitivity and the resolution. We found that advanced research are led by CEA-LETI, in France. A collaboration with them iwould be fruitful as they have expertise in chip biocompatibility and the realization of flexible miniature chips. These two aspects are fundamental for an in-vivo integration and still very little discussed in the state of the art. They propose to seek the realization of ultrafine cMUT chips (<100 microns), integrated in a polymer material (total thickness 200 microns), passivated with biocompatible layers.

An ASIC will integrate the architecture for the signal conversion carried out by a sensor. It must be very low power and modulated to be transmitted. We will follow a flow of design with a particular work on architecture and the choice of integration technology to reduce consumption. We estimate that a $1mm^2$ integrated circuit will be sufficient to perform the information-to-ultrasound conversion.

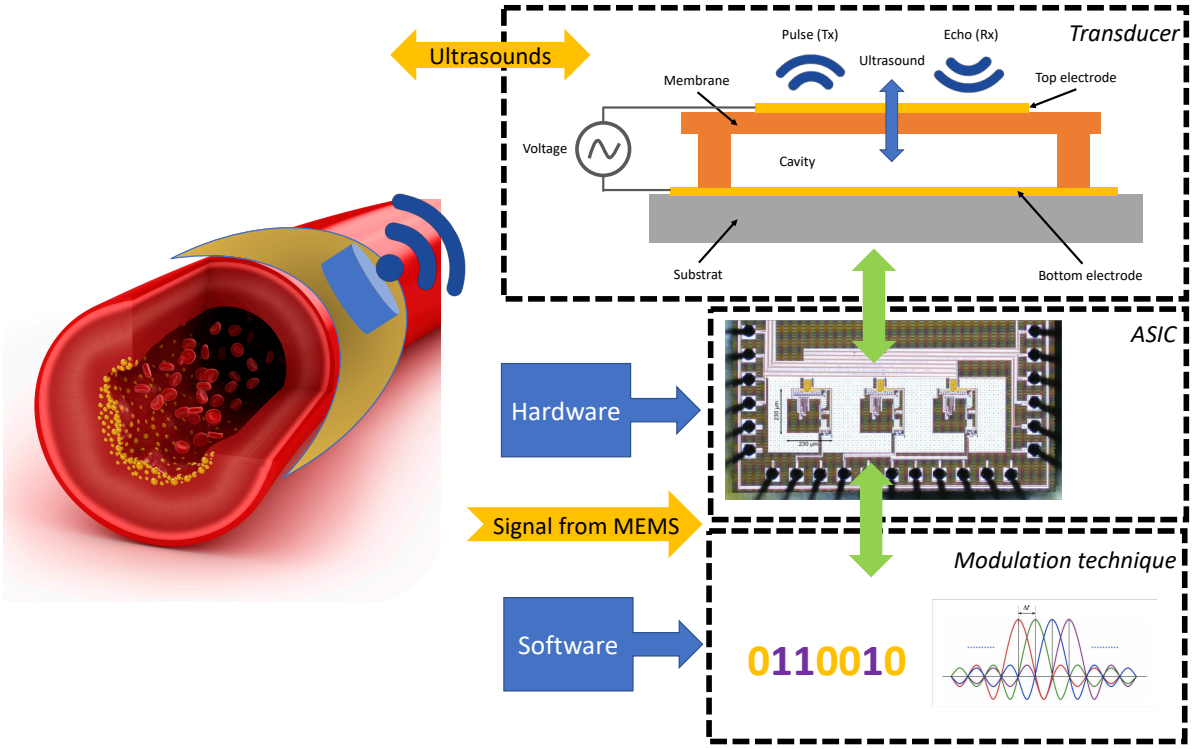


Figure 4.13 – View of the integrated system for ultrasonic communication

A dedicated signal processing has to be proposed. Ultrasonic transmission must be robust to interference to ensure the integrity of the information (Signal-Noise Ratio, SNR) on multidirectional propagation with reflection (bone, muscle, fat, blood circulation). We have identified a company specialized in ultrasonic communication (COPSONIC) which is currently working on the development of CODECs specific to ultrasonic communications to ensure the integrity of propagation in constrained environments. We will work with them on the modeling of the Human body with the simulation of a channel to evaluate the propagation of modulated signals and we will apply their modulation techniques. Signal processing will be integrated into the ASIC.

The purpose of those investigations are to make a proof of concept to provide a complete building block for a device in the field of e-health, telemedicine and medical research. The use of this technology, driven by the development of dedicated MUT, might enable breakthrough innovation:

— in medical research: this will open to a “big data” of the Human body to understand body mechanism at the deeper scale and over a large and diverse population. For example, research in hematology has a strong interest in digitizing the body’s bloodstream in real time over a long period of time.

— in e-health: we seek to develop a predictive health on-the-fly: from the optimization of everyone's hygiene, with a continuous surveillance to trigger some alerts on our behaviors. The goal is a drastic reduction in the costs of the health system.

4.3 Analog Signal Processing for Edge Computing

Analog Signal Processing is a solution for optimized transceivers architectures as said in section 1.2.2. The key drivers for its uses is the power consumption, the high resolution and the low-latency of the signal processing. Thus, possible investigations for an application to Design by Mathematics in electronics systems could be IoT or imagers. It is, to some extent, edge computing using analog signal processing. This processing will operate as close as possible to the transceiver device (antenna, photodiode, ...) to perform information-to-signal conversion.

IoT

IoT will connect more than a trillion of objects, with a majority limited to sensing one data over a long lifetime. The power consumption is crucial, not only for the battery but also at a global level when considering ressources available on Earth. IoT cannot use a standard architecture. We can estimate that an ASIC dedicated to edge computing from a sensor or a group of sensors to RF Tx in an object can reduce its power consumption by a factor of 10 when digital signal processing is avoided at its maximum. By moving some processing in front of the ADC, an order-of-magnitude reduction in signal chain power consumption can be achieved, because the desired data can be extracted and digitized while the undesired data are discarded. Thus, analog processing can improve battery life and sensor intelligence. I propose to investigate on full custom solution at the system level. The system will include analog sensing, analog or mixed-signal edge computing and low-power RF transmitter.

Image sensor

Image sensors are now smart sensors that allow embedded systems to analyze our environment without any transmission of raw data, which consumes a lot of power because of the high amount of data involved. That is why image sensor are required to integrate image processing tasks as close as possible to the sensor which consist in a matrix of pixels composed of a photosensitive area. The trend is a macropixel approach with the merge of processing elements between several pixels and processing tasks between several processing elements. The application is a direct adaptation of spatial and temporal filtering. As the processing element is an analog switched capacitor circuit, there is room to investigate on analog signal processing dedicated to image sensors. The target would be to optimize the accuracy, reduce the power consumption and increase the edge computing possibilities within image sensors such as initiated in [61].

4.4 Conclusion

This chapter presented **3 directions** for research activities in the coming years. First, I proposed to keep on investigating on **optimized RF systems** either to give them more flexibility (carrier aggregation, wide band, ...) or to access to higher frequency band such as over 100GHz. Then, I would like to participate to the integration of a full **ultrasound transceiver for IBC**. This implies the research of new techniques to efficiently propagate ultrasound not only in terms of power but also in terms of modulation. Last, I try to envision which kind of analog electronics will be required on a long term basis. ASICs and thus, analog designers, have still their role to play to optimize each circuit as trillions of them would be concern in the case of IoT and imagers. I believe that **edge computing** can be analog and be done at a low power with relevant resolution.

Conclusion

This document summarizes my research work over the past decade since my PhD work in June 2009 until today. I have presented activities in analog circuit design applied to communications.

My first research topic is the design of RF systems. I have made the demonstration of 4 disruptive architectures that could be used for sub-6GHz communications. They all use a dedicated design methodology called **Design by Mathematics**:

- in the frequency domain: using Fourier and Walsh theories,
- in the time domain: using Riemann integral theory.

Circuits have been designed, measured and published in close collaboration with industrial partners such as STMicroelectronics and Thales.

My second research topic is Intra-Body Communications. I have started this activity 6 years ago by proposing:

- new approach in interface sensor design: a full analog circuit to convert sensor data to RF signal,
- using the sparsity of ECG signal to design an ADC,
- new approach of propagating information within the Human body by using ultrasounds.

This work allowed me to consider my projects and prospects for the next coming years organized in 3 main directions:

- advanced RF systems for wide band of high frequency access,
- an ultrasound-based network for Intra-Body Communications,
- the use of analog signal processing for edge computing.

Some of these projects have already started thanks to Master or PhD thesis work. These perspectives within the Circuits and Systems research team have a great potential with several academic or industrial partners involved. The support of our industrial partners, our institutional partners, our involvement in European projects allow us to maintain these activities at a very high level.

We strongly believe that analog circuit design has a lot to offer for years to come.

Bibliography

[1] "B. murmann, adc performance survey 1997-2018," http://web.stanford.edu/~murmann/adcsurvey.html, [Online] 2018.

[2] Y. Veyrac, "Contribution à l'étude et à la réalisation d'un générateur de signaux radiofréquences analogiques pour la radio logicielle intégrale," Ph.D. dissertation, 2015, thèse de doctorat dirigée par Deval, Yann et Rivet, François Electronique Bordeaux 2015. [Online]. Available: http://www.theses.fr/2015BORD0444

[3] A. Ghaffari, E. A. M. Klumperink, M. C. M. Soer, and B. Nauta, "Tunable high-q n-path band-pass filters: Modeling and verification," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, May 2011.

[4] Y. Xu, J. Zhu, and P. R. Kinget, "A blocker-tolerant rf front end with harmonic-rejecting *n* -path filter," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 2, pp. 327–339, Feb 2018.

[5] S. Hameed and S. Pamarti, "Design and analysis of a programmable receiver front end with time-interleaved baseband analog-fir filtering," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 11, pp. 3197–3207, Nov 2018.

[6] D. Murphy, H. Darabi, A. Abidi, A. A. Hafez, A. Mirzaei, M. Mikhemar, and M. F. Chang, "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2943–2963, Dec 2012.

[7] C. Andrews and A. C. Molnar, "A passive mixer-first receiver with digitally controlled and widely tunable rf interface," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2696–2708, Dec 2010.

[8] B. Sadhu, M. Sturm, B. M. Sadler, and R. Harjani, "A 5gs/s 12.2pj/conv. analog charge-domain fft for a software defined radio receiver front-end in 65nm cmos," *2012 IEEE Radio Frequency Integrated Circuits Symposium*, pp. 39–42, June 2012.

[9] E. A. M. Klumperink, H. J. Westerveld, and B. Nauta, "N-path filters and mixer-first receivers: A review," in *2017 IEEE Custom Integrated Circuits Conference (CICC)*, April 2017, pp. 1–8.

[10] Q. Meng and R. Harjani, "An easily extendable fft based four-channel, four-beam receiver with progressive partial spatial filtering in 65nm," *ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference*, pp. 359–362, Sep. 2016.

[11] O. Oliaei, M. Kirschenmann, D. Newman, K. Hausmann, H. Xie, P. Rakers, M. Rahman, M. Gomez, C. Yu, B. Gilsdorf, and K. Sakamoto, "A multiband multimode transmitter without driver amplifier," pp. 164–166, Feb 2012.

[12] J. Craninckx, M. Liu, D. Hauspie, V. Giannini, T. Kim, J. Lee, M. Libois, B. Debaillie, C. Soens, M. Ingels, A. Baschirotto, J. van Driessche, L. van der Perre, and P. Vanbekbergen, "A fully reconfigurable software-defined radio transceiver in 0.13m cmos," *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, pp. 346–607, Feb 2007.

[13] B. Analui, T. Mercer, S. Mandegaran, A. Goel, and H. Hashemi, "A 50 mhz–6 ghz, 2 2 mimo, reconfigurable architecture, software-defined radio in 130nm cmos," *2014 IEEE Radio Frequency Integrated Circuits Symposium*, pp. 329–332, June 2014.

[14] Y. Yin, B. Chi, Z. Sun, X. Zhang, and Z. Wang, "A 0.1–6.0-ghz dual-path sdr transmitter supporting intraband carrier aggregation in 65-nm cmos," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 5, pp. 944–957, May 2015.

[15] A. Fouque, F. Rivet, F. Fadhuile, Y. Deval, J.-B. Begueret, and D. Beloty, "A low power digitally-enhanced sasp-based receiver architecture for mobile dvb-s applications in the ku-band (10.7-12.75 ghz)," *2011 IEEE Radio and Wireless Week, RWW 2011 - 2011 IEEE Radio and Wireless Symposium, RWS 2011*, pp. 275–278, 2011.

[16] F. Rivet, Y. Deval, J.-B. Begueret, D. Dallet, and D. Belot, "A universal radio frequency receiver architecture based on sampled analog signal processing," *2007 IEEE North-East Workshop on Circuits and Systems, NEWCAS 2007*, pp. 1449–1452, 2007.

[17] ——, "A software-defined radio based on sampled analog signal processing dedicated to digital modulations," *Proceedings of the 2007 Ph.D Research in Microelectronics and Electronics conference, PRIME 2007*, pp. 121–124, 2007.

[18] F. Rivet, Y. Deval, J. Begueret, D. Dallet, and D. Belot, "A disruptive software-defined radio receiver architecture based on sampled analog signal processing," *Digest of Papers - IEEE Radio Frequency Integrated Circuits Symposium*, pp. 197–200, 2007.

[19] F. Rivet, Y. Deval, J.-B. Begueret, D. Dallet, P. Cathelin, and D. Belot, "A disruptive receiver architecture dedicated to software-defined radio," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 4, pp. 344–348, 2008.

[20] ——, "65nm cmos circuit design of a sampled analog signal processor dedicated to rf applications," *2008 Joint IEEE North-East Workshop on Circuits and Systems and TAISA Conference, NEWCAS-TAISA*, pp. 233–236, 2008.

[21] ——, "The first experimental demonstration of a sasp-based full software radio receiver," *Digest of Papers - IEEE Radio Frequency Integrated Circuits Symposium*, pp. 25–28, 2009.

[22] ——, "From software-defined to software radio: Analog signal processor features," *RWS 2009 IEEE Radio and Wireless Symposium, Proceedings*, pp. 348–351, 2009.

[23] ——, "The experimental demonstration of a sasp-based full software radio receiver," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 5, pp. 979–988, 2010.

[24] F. Rivet, A. Mariano, Y. Deval, D. Dallet, J.-B. Begueret, and D. Belot, "Sampled analog signal processing: From software-defined to software radio," *Lecture Notes in Electrical Engineering*, vol. 2021 LNEE, pp. 249–264, 2010.

[25] F. Rivet and Y. Deval, "A 97mw 0-4ghz 65nm cmos concurrent receiver," *Proceedings - 2014 IEEE 12th International Conference on Solid-State and Integrated Circuit Technology, ICSICT 2014*, 2014.

[26] Y. Abiven, F. Rivet, Y. Deval, D. Dallet, D. Belot, and T. Taris, "A low-power 2 ghz discrete time weighting system dedicated to sampled analog signal processing," *2011 18th IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2011*, pp. 57–60, 2011.

[27] F. Rivet, F. Fadhuile, Y. Deval, and T. Taris, "Wide-band rejection of interfering signals," *Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems*, pp. 767–770, 2013.

[28] O. Holstensson, F. Rivet, N. Regimbal, Y. Deval, P. Garrec, and T. Taris, "Adaptive interferer cancellation using a sampled analog signal processor," *2014 International Radar Conference, Radar 2014*, 2014.

[29] F. Rivet, Y. Veyrac, Y. Deval, and P. Garrec, "Adaptive interference cancellation using a sampled analogue signal processor," *IET Radar, Sonar and Navigation*, vol. 10, no. 1, pp. 43–49, 2016.

[30] J. Orlando, F. Rivet, and Y. Deval, "A radio-frequency real-time spectrum sensor based on an analog signal processing magnitude calculator," *Proceedings - 30th Symposium on Integrated Circuits and Systems Design: Chip on the Sands, SBCCI 2017*, pp. 7–10, 2017.

[31] N. Bouassida, "Design of a full software transmitter based on walsh sequences," Theses, Université de Bordeaux, Dec. 2016. [Online]. Available: https://tel.archives-ouvertes.fr/tel-01497771

[32] N. J. Fine, "On the walsh functions," *Transactions of the American Mathematical Society*, vol. 65, no. 3, pp. 372–414, 1949.

[33] N. Bouassida, F. Rivet, Y. Deval, D. Duperray, and A. Cathelin, "A concurrent transmitter in cmos 28nm fdsoi technology based on walsh sequences generator," *14th IEEE International NEWCAS Conference, NEWCAS 2016*, 2016.

[34] Y. Veyrac, F. Rivet, Y. Deval, D. Dallet, P. Garrec, and R. Montigny, "The riemann pump: A concurrent transmitter in gan technology," *2014 21st IEEE International Conference on Electronics, Circuits and Systems, ICECS 2014*, pp. 594–597, 2015.

[35] ——, "A 65-nm cmos dac based on a differentiating arbitrary waveform generator architecture for 5g handset transmitter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 1, pp. 104–108, 2016.

[36] Y. Veyrac, F. Rivet, and Y. Deval, "Noise shaping riemann: an energy efficient data conversion scheme," *Analog Integrated Circuits and Signal Processing*, vol. 92, no. 2, pp. 189–197, 2017.

[37] ——, "Experimental demonstration of a riemann pump rf-dac in 65 nm cmos," *2016 IEEE International Conference on Electronics, Circuits and Systems, ICECS 2016*, pp. 241–244, 2017.

[38] F. Rivet, E. Fiawoo, R. Montigny, P. Garrec, and Y. Deval, "An ultra wide band analog-to-digital converter based on a delta-riemann architecture," *Proceedings - SBCCI 2016: 29th Symposium on Integrated Circuits and Systems Design: Chip on the Mountains*, 2016.

[39] D. Yoon, C. Jeong, J. Cartwright, H. Kang, S. Han, N. Kim, D. Ha, and S. Lee, "A new approach to low-power and low-latency wake-up receiver system for wireless sensor nodes," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 10, pp. 2405–2419, Oct 2012.

[40] A. Aldaoud, C. Laurenson, F. Rivet, M. R. Yuce, and J. Redouté, "Design of a miniaturized wireless blood pressure sensing interface using capacitive coupling," *IEEE/ASME Transactions on Mechatronics*, vol. 20, no. 1, pp. 487–491, Feb 2015.

[41] "Ieee standard for local and metropolitan area networks - part 15.6: Wireless body area networks," *IEEE Std 802.15.6-2012*, pp. 1–271, Feb 2012.

[42] C. Laurenson, F. Rivet, M. Yuce, and J.-M. Redoute, "A 1.04 μw wireless integrated mems interface in umc 0.18?m cmos," *Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society, EMBS*, vol. 2015-November, pp. 889–892, 2015.

[43] ——, "A 180 nm cmos analog adaptive sampler for blood pressure feature extraction," *Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society, EMBS*, vol. 2016-October, pp. 4841–4844, 2016.

[44] M. Tlili, "Contribution à la conception d'un système d'acquisition de signaux biomédicaux pour la télésurveillance médicale," Ph.D. dissertation, 2018, thèse de doctorat dirigée par Dallet, Dominique et Rebai, Chiheb Electronique Bordeaux 2018. [Online]. Available: http://www.theses.fr/2018BORD0159

[45] S. Yim, Y. Park, H. Yang, and S. Kim, "Power efficient SAR ADC adaptive to input activity for ECG monitoring applications, IEEE International Symposium on Circuits and Systems (ISCAS), 2017," pp. 1–4.

[46] I. A. A. Al-Darkazly and S. R. Hasan, "Optimized low-power CMOS active-electrode-pair for low-frequency multi-channel biomedical stimulation," *Elsevier Microelectronics Journal*, vol. 66, pp. 18–24, 2017.

[47] S. Mukhopadhyay, S. Mitra, and M. Mitra, "An ECG signal compression technique using ASCII character encoding," *Elsevier Measurement Journal*, vol. 45, no. 6, pp. 1651–1660, 2012.

[48] M. Brajović, I. Orović, M. Daković, and S. Stanković, "On the parameterization of Hermite transform with application to the compression of QRS complexes," *Elsevier Signal Processing Journal*, vol. 131, pp. 113–119, 2017.

[49] Z. Peng, G. Wang, H. Jiang, and S. Meng, "Research and improvement of ECG compression algorithm based on EZW," *Computer Methods and Programs in Biomedicine*, vol. 145, pp. 157–166, 2017.

[50] E. Allier, G. Sicard, L. Fesquet, and M. Renaudin, "Asynchronous level crossing analog to digital converters," *Elsevier Measurement Journal*, vol. 37, no. 4, pp. 296–309, 2005.

[51] M. Tlili, A. Maalej, M. Ben-Romdhane, M. C. Bali, F. Rivet, D. Dallet, and C. Rebai, "Level-crossing ADC modeling for wireless electrocardiogram signal acquisition system, IEEE International Instrumentation and Measurement Technology Conference Proceedings (I2MTC)," pp. 1–5. , 2016.

[52] Y. Zigel, A. Cohen, and A. Katz, "The weighted diagnostic distortion (WDD) measure for ECG signal compression," *IEEE* T*ransactions on* B*iomedical* E*ngineering*, vol. 47, no. 11, pp. 1422–1430, 2000.

[53] M. Tlili, M. Ben-Romdhane, A. Maalej, F. Rivet, D. Dallet, and C. Rebai, "Level-crossing adc design and evaluation methodology for normal and pathological electrocardiogram signals measurement," *Measurement*, vol. 124, pp. 413 – 425, 2018.

[54] F. Rivet, N. Owen, D. Lai, and Y. Deval, "Intra-body communications - radio-frequency versus ultrasonic," *2014 21st IEEE International Conference on Electronics, Circuits and Systems, ICECS 2014*, pp. 347–350, 2015.

[55] M. Seyedi, Z. Cai, D. Lai, and F. Rivet, "An energy-efficient pulse position modulation transmitter for galvanic intrabody communications," *Proceedings of the 2014 4th International Conference on Wireless Mobile Communication and Healthcare - "Transforming Healthcare Through Innovations in Mobile and Wireless Technologies", MOBIHEALTH 2014*, pp. 192–195, 2015.

[56] F. Rivet, N. Owen, D. Lai, and Y. Deval, "Intra-body communications: radio-frequency versus ultrasonic," *Analog Integrated Circuits and Signal Processing*, vol. 87, no. 2, pp. 289–299, 2016.

[57] F. Rivet, S. Redois, and Y. Deval, "Characterization of ultrasonic wave propagation for intra-body communication," Sept. 2016. [Online]. Available: https://hal.archives-ouvertes.fr/hal-01377964

[58] R. McGough and M. W. Urban, "Calculations of intensities for radiation force modeling with the software package focus," *Proceedings of Meetings on Acoustics*, vol. 9, no. 1, p. 020006, 2010.

[59] L. E. Franks and I. W. Sandberg, "An alternative approach to the realization of network transfer functions: The n-path filter," *The Bell System Technical Journal*, vol. 39, no. 5, pp. 1321–1350, Sep. 1960.

[60] A. Ghaffari, E. Klumperink, and B. Nauta, "Tunable n-path notch filters for blocker suppression: modeling and verification," *IEEE journal of solid-state circuits*, vol. 48, no. 6, pp. 1370–1382, 6 2013, eemcs-eprint-23470.

[61] J. Le hir, "Mixed co-design for an integrated smart image sensor with massively parallel local image processing," Theses, Université Paris-Saclay, Dec. 2018. [Online]. Available: https://tel.archives-ouvertes.fr/tel-02015255