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# Wide Bandgap Semiconductor Components Integration in a PCB Substrate for the Development of a High Density Power Electronics Converter

Thèse de doctorat de l'Université Paris-Saclay  
préparée à l'Université Paris-Sud

École doctorale n°575 : Electrical, Optical, Bio: Physics and  
Engineering (EOBE)

Spécialité de doctorat: Génie électrique

Thèse présentée et soutenue à Gif-sur-Yvette de soutenance, le 30 Novembre 2018, par

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**Titre :** Intégration dans un substrat PCB de composants à semi-conducteur Grand Gap pour le développement d'un convertisseur d'électronique de puissance à forte densité

**Mots clés :** Technologie de PCB, Gestion thermique, Modélisation 3D, Modélisation électrothermique

**Résumé :** Les nouveaux composants à semi-conducteur de type grand gap ont été développés pour des applications de conversion de puissance en raison de leurs hautes fréquences de commutation (de centaine kHz à quelques MHz) et pertes faibles. Afin de bien profiter ses avantages, la technologie des circuits imprimés (PCB) est intéressante pour une intégration à haute densité de puissance grâce à sa flexibilité et son faible coût. Cependant, à cause de la mauvaise conductivité thermique du matériau FR-4 utilisé pour le substrat PCB et la haute densité de puissance réalisée, il est primordial de trouver des solutions thermiques pour améliorer les performances thermique de la structure de PCB.

Dans cette thèse, trois solutions thermiques pour les structures de PCB ont été proposées, y compris des solutions avec des vias thermiques, de cuivre épais sur le substrat PCB ainsi que des dispositifs de refroidissement thermoélectrique (TEC). Nos études sont basées sur la modélisation électrothermique et la méthode d'éléments finis en 3D.

Tout d'abord, l'optimisation des paramètres des vias (diamètre, épaisseur de placage, surface formée par des vias, la distance entre des vias etc.) a été réalisée pour optimiser l'effet de refroidissement.

Ensuite, on constate que les performances thermiques des structures de PCB peuvent être améliorées en utilisant cuivre épais sur le substrat de PCB. Cuivre épais augmente le flux thermique lateral dans la couche de cuivre. Les influences de l'épaisseur de cuivre (35 à 500  $\mu\text{m}$ ) ont été étudiées. Cette solution est facile à réaliser et peut être combinée à d'autres solutions de refroidissement.

Enfin, le dispositif thermoélectrique comme les modules Peltier est une technologie de refroidissement local. Les influences des paramètres de Peltier (Propriétés du matériau thermoélectrique, nombre d'éléments Peltier, distance entre la source de chaleur et les dispositifs Peltier, etc.) ont été identifiées. Il est démontré que des modules Peltier ont l'application potentielle pour le développement d'intégration de PCB attendu que son active contrôle des températures.

**Title :** Wide Bandgap Semiconductor Components Integration in a PCB Substrate for the Development of a High Density Power Electronics Converter

**Keywords :** PCB technology, Thermal management, 3D FE Modeling, Electro-thermal modeling

**Abstract :** The emerging wide bandgap (WBG) semiconductor devices have been developed for power conversion applications instead of silicon devices due to higher switching frequencies (from few 100 kHz to several MHz) and lower on-state losses resulting in a better efficiency. In order to take full advantage of the WBG components, PCB technology is attractive for high power density integration thanks to its flexibility and low cost. However, due to poor thermal conductivity of the commonly used material Flame Retardant-4 (FR4), efficient thermal solutions are becoming a challenging issue in integrated power boards based on PCB substrates. So it is of the first importance to seek technological means in order to improve the thermal performances.

In this thesis, three main thermal management solutions for PCB structures have been investigated including thermal vias, thick copper thickness on the PCB substrate as well as thermoelectric cooling (TEC) devices. Our studies are based on the electro-thermal modeling and 3D finite element (FE) methods.

Firstly, optimization of the thermal via parameters (via diameter, via plating thickness, via-cluster surface, via pattern, pitch distance between vias etc.) has been realized to improve their cooling

performances. We presented and evaluated thermal performances of the PCB structures by analyzing the thermal resistance of the PCB substrate with different thermal vias.

Secondly, it is found that thermal performances of the PCB structures can be enhanced by using thick copper thickness on top of the PCB substrate, which increases the lateral heat flux along the copper layer. Influences of the copper thickness (35  $\mu\text{m}$  to 500  $\mu\text{m}$ ) has been discussed. This solution is easy to realize and can be combined with other cooling solutions.

Thirdly, thermoelectric cooler like Peltier device is a solid-state cooling technology that can meet the local cooling requirements. Influences of Peltier parameters (Thermoelectric material properties, number of Peltier elements, distance between the heating source and the Peltier devices etc.) have been identified. All these analyses demonstrate the potential application of Peltier devices placed beside the heating source for PCB structures, which is a benefit for developing the embedding technology in such structures.

## REMERCIEMENTS

Sur cette page dédiée aux remerciements je souhaite m'adresser à toutes les personnes qui m'ont aidé à agrandir dans l'univers des sciences et des technologies durant ces trois années de thèse.

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# RÉSUMÉ EN FRANÇAIS

## I- Contexte de l'étude

Au cours des dernières années, la technologie de l'électronique de puissance a connu une évolution rapide grâce au concept « plus électrique ». Récemment, de nombreuses applications de l'électronique de puissance se sont développées dans les environnements industriels, commerciaux, résidentiels, de transport, utilitaires, aérospatiaux et militaires en raison de la réduction des coûts, de la taille et de l'amélioration des performances [1].

Comme les caractéristiques des composants de puissance à base de Silicium ont atteint ou sont très proches leurs limites physiques, les composants à grand gap en Nitrure de Gallium (GaN) ou Carbone Silicium (SiC) ont récemment émergé. Ils permettent d'atteindre de plus hautes fréquences de commutation tout en offrant une plus faible résistance à l'état passant. La capacité de ces composants grand gap en matière de montée en fréquence est liée à leurs vitesse de commutation ce qui implique que des fronts d'onde  $dv/dt$  et  $di/dt$  extrêmement élevés sont générés. Les connexions de ces composants avec le reste du circuit et donc leur packaging sont donc des points cruciaux pour permettre de bénéficier pleinement des performances en vitesse de commutation. L'augmentation des performances électriques permet par ailleurs de réduire les dimensions de la partie active du composant grand gap pour un cahier des charges donné. Les contraintes thermiques découlant de la réduction de la surface de ces composants devient alors un problème important, d'autant plus si l'on souhaite travailler à plus haute température, ce que sont censés pouvoir permettre de tels composants.

L'augmentation de la densité de puissance et les avancées des semi-conducteurs à grand gap nécessitent des améliorations en matière d'intégration, de technologie d'assemblage ainsi que des solutions de gestion thermique. En effet, la plupart des technologies d'assemblage commerciales sont élaborées pour les composants à base de Silicium pour lesquels, la température de fonctionnement est en particulier plus faible. Or, dans de nombreuses applications, par exemple dans les domaines de l'aérospatiale et de l'aéronautique, une capacité de fonctionnement fiable dans des environnements difficiles (de  $-55\text{ °C}$  à  $250\text{ °C}$ ) est fortement souhaitée. Les composants à grand gap offrent l'avantage de pouvoir fonctionner à plus haute température. Cependant, les technologies d'assemblage, les composants passifs, les composants périphériques disponibles, les matériaux de brasure, les considérations de fiabilité et les coûts limitent actuellement les températures de jonction à environ  $175\text{ °C}$ , même si les semi-conducteurs à grand gap peuvent fonctionner principalement à températures de jonction beaucoup plus élevées [7-9].

Afin d'atténuer les effets induits par une plus grande rapidité de commutation et une densité de puissance plus importante, il est nécessaire de proposer et développer des solutions d'assemblage avancées avec des systèmes de refroidissement efficaces de manière à tirer pleinement avantage des composants à grand gap.

Parmi les technologies matures utilisées dans le domaine de l'électronique de puissance, la technologie des circuits imprimés (Printed Circuit Board : PCB) répond aux contraintes techniques pour les petites et moyennes puissances (quelques centaines de Watts jusqu'à quelques kW). La technologie DBC (Direct Bonded Copper) est pour sa part utilisée dans le cas de densité de puissance et de puissances élevées [10]. Entre autres avantages, la technologie PCB permet de réaliser l'intégration 3D des composants de puissance en supprimant l'utilisation des fils de bonding. Toutefois le substrat de PCB en matériau de FR-

4 a une mauvaise conductivité thermique ( $<1.5 \text{ W/mK}$ ), ce qui rend difficile la gestion des flux thermiques et la maîtrise de la température des composants.

Cette thèse est donc consacrée au développement de solutions de refroidissement destinées à des assemblages à base de PCB. Trois méthodes de refroidissement ont été étudiées :

- La première solution est basée sur le concept de vias thermiques créés dans le substrat PCB. L'objectif est pour cette partie de définir des règles de design permettant de choisir les paramètres des vias pour atteindre les performances thermiques souhaitées ;
- La seconde solution consiste à augmenter l'épaisseur de la couche de cuivre sur le dessus de substrat de PCB. Cette solution permet d'augmenter la diffusion latérale de la chaleur et ainsi d'augmenter la surface de dissipation thermique ;
- La troisième solution propose et analyse des solutions de refroidissement basées sur des technologies thermoélectriques (TEC).

Le mémoire de thèse est divisé en quatre parties, hors conclusion et perspectives, présentant successivement :

- Dans le premier chapitre, un bref aperçu du développement des systèmes électroniques de puissance et du contexte général de ce travail est présenté afin d'introduire les concepts de base de la gestion thermique, concepts utilisés tout au long de la thèse. Nous discuterons ensuite de l'état de l'art des techniques d'assemblage actuels utilisés en électronique de puissance et des différentes solutions de gestion des aspects thermiques. Ce chapitre sera également consacré à la comparaison des certaines méthodes de modélisation basées sur différents logiciels issues de la littérature ;
- Le deuxième chapitre présentera les aspects instrumentaux utilisés dans le banc d'essai destiné à la mesure des flux de puissance et des températures. Le banc d'essai est décrit ainsi que le processus d'étalonnage de certains dispositifs tels que les capteurs de température à résistance (RTD). Les principes de réalisation des échantillons sont également présentés ;
- Le troisième chapitre couvre deux méthodes de refroidissement : La solution de refroidissement par vias thermiques et par augmentation de l'épaisseur de cuivre du substrat PCB. Différentes méthodes de modélisation : analyse électrothermique en 1D et méthode d'éléments finis en 3D ont été utilisées pour analyser l'impact sur refroidissement des différents paramètres des vias, notamment le diamètre, le nombre des vias, l'épaisseur du cuivre, la distance entre deux vias, etc. ;
- Le quatrième chapitre, décrit et analyse une solution de refroidissement basée sur des modules thermoélectriques (TEC) utilisant l'effet Peltier. Dans ce chapitre, des modèles sont proposés et utilisés pour dimensionner et optimiser cette solution en fonction des propriétés thermiques recherchées.



## II- Les principaux résultats

### ✧ Optimisation des vias thermiques

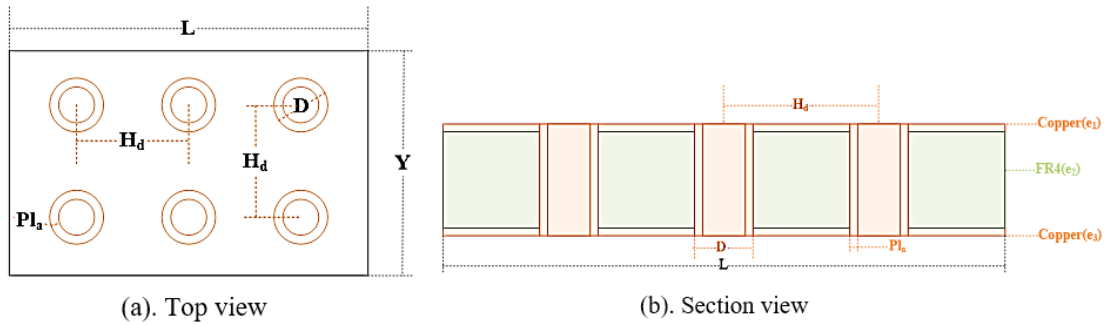


Figure 1: Vue de dessus (a) et vue en coupe (b) des vias thermiques créés dans un substrat PCB

D'après l'hypothèse de conduction thermique en 1D, les paramètres des vias thermiques sont exprimés sous la forme de grandeurs adimensionnelles dans (1) et (2). Ces paramètres sont utilisés pour définir la résistance thermique d'une structure PCB avec vias thermiques.

$$R_{oa} = \frac{1}{1 + \pi \cdot R_{o1} \cdot R_{o2}^2 \cdot \left( \sigma_r \cdot \frac{R_{o3} - 1}{R_{o2}} \right)} \quad (1)$$

$$R_{oa} = \frac{R_{a\_N}}{R_{board}}, R_{o1} = \frac{N \cdot H_d^2}{S_1}, R_{o2} = \frac{D}{H_d}, R_{o3} = \frac{Pl_a}{H_d} \quad (2)$$

Avec

$R_{oa}$  : le rapport de la résistance thermique du substrat de PCB avec et sans  $N$  vias thermiques ;

$R_{a\_N}$  (W/mK) : la résistance thermique du substrat de PCB avec  $N$  vias thermiques ;

$R_{board}$  (W/mK) : la résistance thermique du substrat de PCB sans vias thermiques ;

$R_{o1}$  : le rapport de la surface formée par des vias thermiques à la surface disponible ;

$R_{o2}$  : le rapport du diamètre du via thermique  $D$  (mm) à la distance entre deux vias  $H_d$  (mm) ;

$R_{o3}$  : le rapport de l'épaisseur de cuivre dans le via  $Pl_a$  (mm) à la distance entre deux vias  $H_d$  (mm) ;

$S_1$  : la surface normale à la direction de transfert de chaleur  $L \times Y$  (mm $\times$ mm) ;

$\sigma_r$  : le rapport de la conductivité thermique entre les matériaux : cuivre et FR-4 ;

On a proposé deux motifs différents formés par des vias thermiques (Voir Figure 2). La différence entre les deux motifs réside dans le nombre des vias qu'on peut créer pour la même surface disponible.

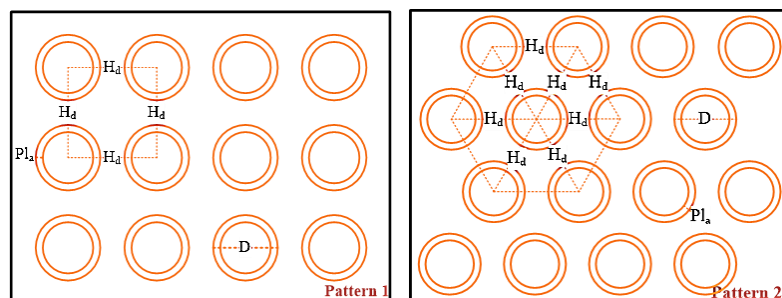
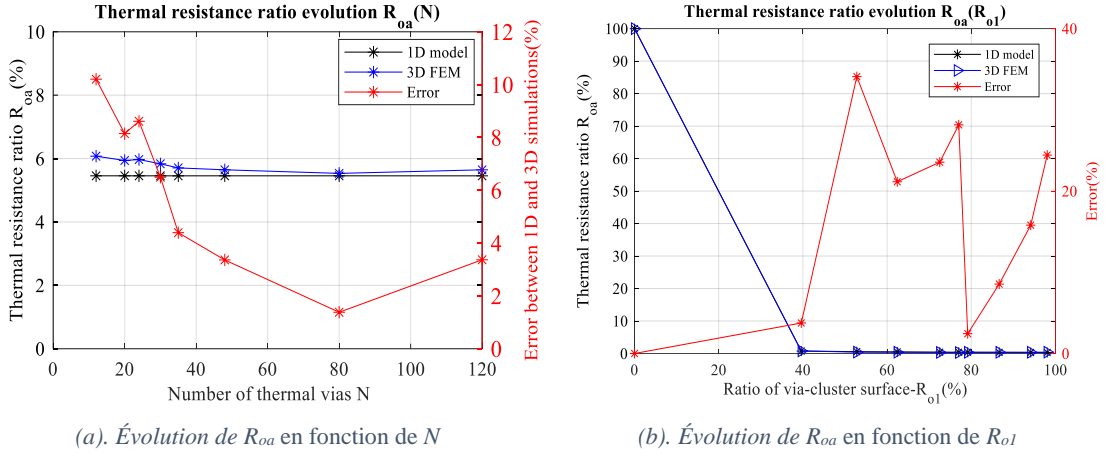


Figure 2: Vue de dessus des deux motifs (Pattern\_1 et Pattern\_2) utilisés pour créer des vias thermiques dans un substrat PCB

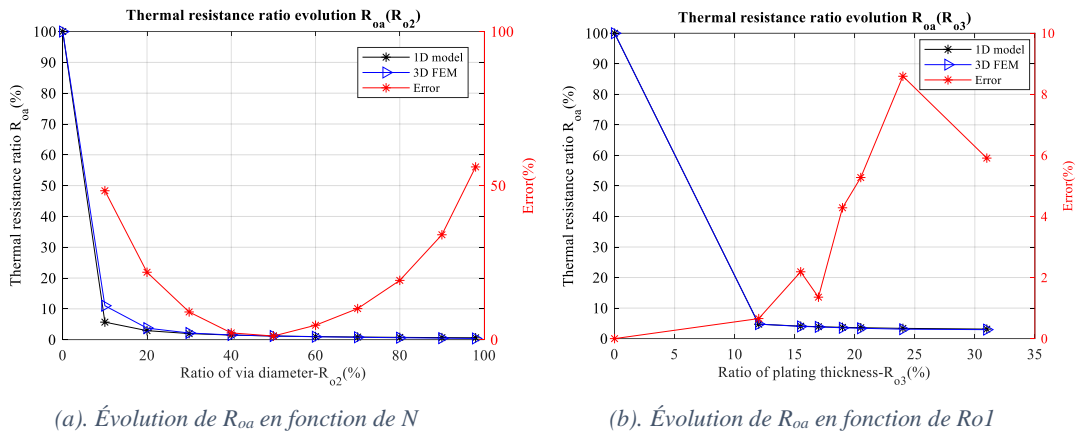
Les effets sur la résistance thermique du substrat des différents paramètres précédents (le nombre des vias  $N$ , le rapport de surface des vias  $R_{o1}$ , le rapport de diamètre du via  $R_{o2}$ , le rapport d'épaisseur de placage du via  $R_{o3}$  et le motif formé par des vias) sont résumés dans Figure 3, Figure 4 et Figure 5 :



(a). Évolution de  $R_{oa}$  en fonction de  $N$

(b). Évolution de  $R_{oa}$  en fonction de  $R_{o1}$

Figure 3: Évolution du rapport de résistance thermique du substrat PCB avec des vias thermiques  $R_{oa}(N)$ ,  $R_{oa}(R_{o1})$



(a). Évolution de  $R_{oa}$  en fonction de  $R_{o2}$

(b). Évolution de  $R_{oa}$  en fonction de  $R_{o3}$

Figure 4: Évolution du rapport de résistance thermique du substrat PCB avec des vias thermiques  $R_{oa}(R_{o2})$ ,  $R_{oa}(R_{o3})$

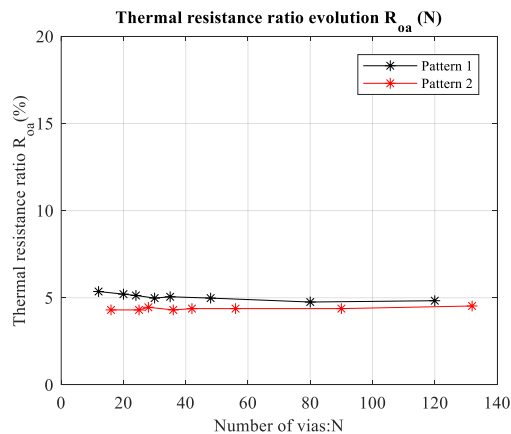


Figure 5: Évolution de rapport de résistance thermique du substrat PCB avec des vias thermiques  $R_{oa}(N)$  pour deux motifs différents

Les prédéterminations du comportement thermique de cette solution sont réalisées par simulation sur un modèle 1D en utilisant le logiciel Matlab Simulink. Les simulations 3D sont réalisées avec le logiciel COMSOL Multiphysics.

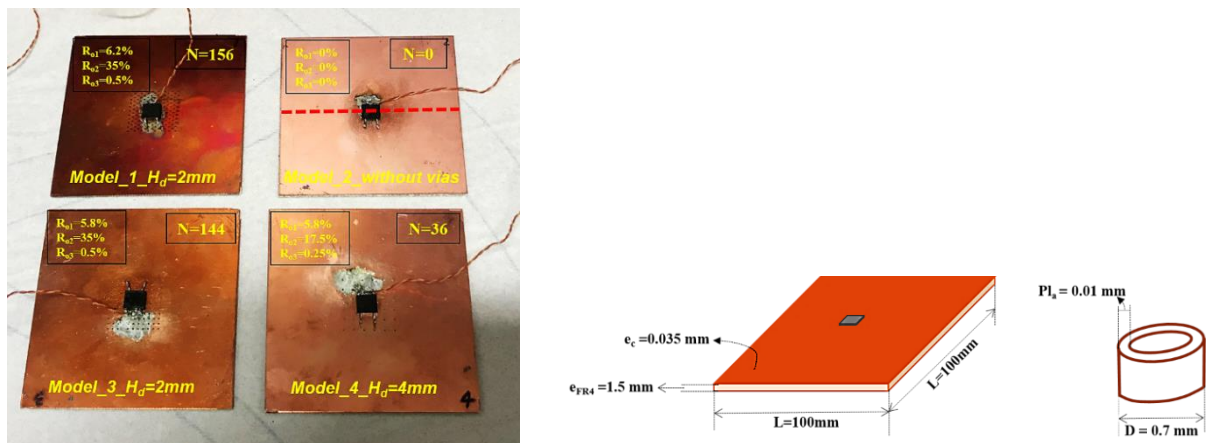


Figure 6: Les différents échantillons avec vias thermiques créés sur un substrat PCB. L'élément chauffant est une résistance brasée. les vias thermiques sont placés au-dessous de la résistance. Un thermocouple est soudé sur la semelle de la résistance pour mesurer sa température au plus près de l'élément chauffant

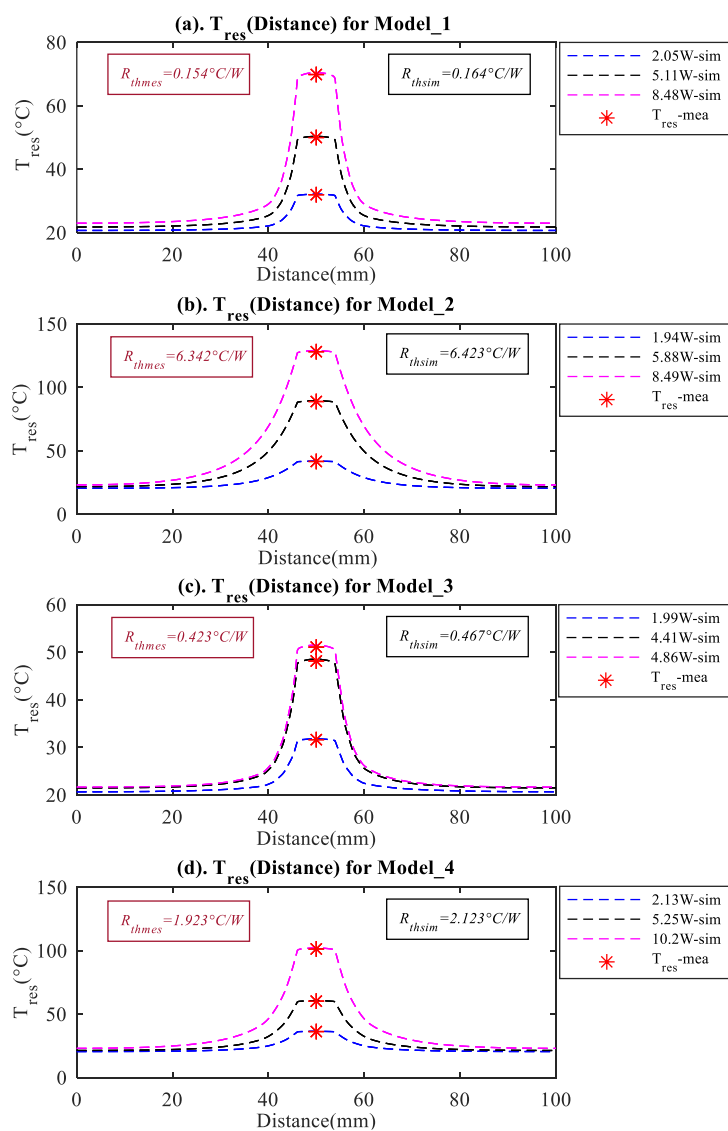


Figure 7: Comparaisons des résultats de simulation et des résultats d'expérimentation. Les températures au milieu de la surface de PCB sont obtenues par simulation thermique 3D. La température de l'élément chauffant est mesurée par thermocouple.

L'étude conduite a permis de relier la valeur de la résistance thermique du substrat aux valeurs des différents paramètres  $R_{o1}$ ,  $R_{o2}$ ,  $R_{o3}$ . De façon qualitative, la résistance thermique

diminue lorsque la valeur de ces paramètres augmente. Il est également démontré que le motif *Pattern\_2* donne de meilleures performances à surface de PCB occupée identique.

Les résultats des températures obtenues par simulations et expérimentalement sont donnés à la Figure 6 et la Figure 7. Un bon accord entre les expérimentations et les simulations nous a permis de valider les modèles proposés et ainsi de valider ces modèles comme outil de conception de vias thermiques.

#### ❖ Refroidissement par des modules de Peltier

L'agencement du mode de refroidissement par modules thermoélectriques d'un assemblage sur PCB est proposé à la Figure 8. Cet agencement permet de drainer le flux de chaleur généré par l'élément chauffant en face avant via la couche supérieure de cuivre du PCB. Les modules de Peltier jouent le rôle de pompe à chaleur et absorbent le flux de chaleur de côté froid  $Q_c$  (W) pour l'évacuer côté chaud  $Q_h$  (W).

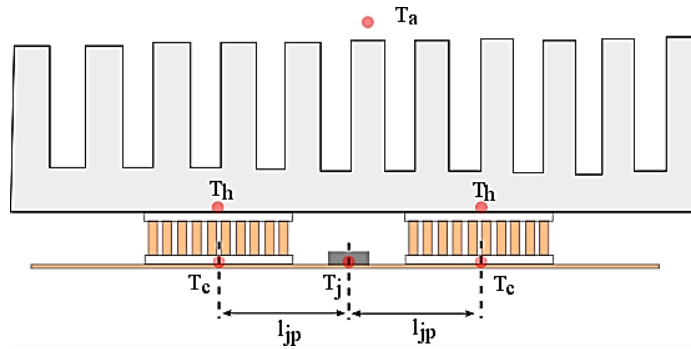


Figure 8: Agencement du refroidissement d'un assemblage PCB par modules Peltier montés en face avant du PCB

L'un des avantages de cette solution réside dans le fait qu'elle permet de contrôler la température de jonction  $T_j$  (K) dynamiquement en fonction de la puissance à dissiper  $P_{heat}$  (W). L'ajustement est réalisé par l'intermédiaire du courant électrique parcourant les modules Peltier et donc par modulation de la puissance électrique consommée. La puissance électrique nécessaire pour réaliser ce pompage d'énergie thermique est un point clé de ce mode de refroidissement. Le design de la solution doit être optimisé pour minimiser cette puissance.

En considérant que le flux thermique est 1D dans l'essentiel de la structure, un modèle thermique simplifié a été proposé. Ce modèle intègre un modèle analytique des modules Peltier [161-166]. Le schéma électrique correspondant à ce modèle est donné ci-dessous :

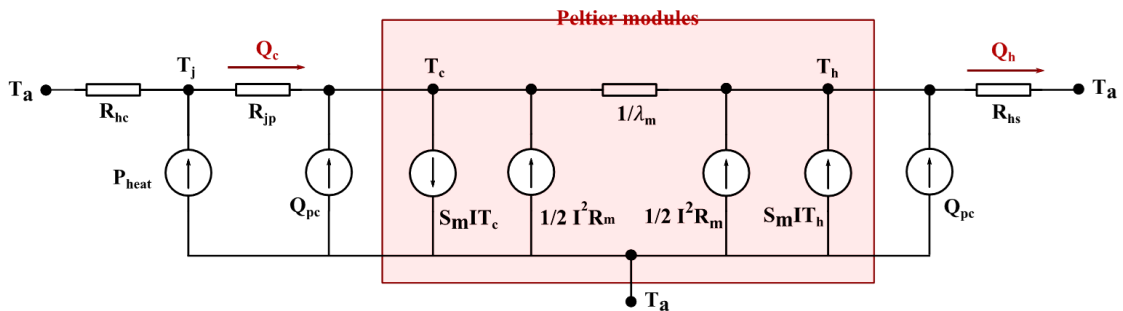


Figure 9: Modèle électrothermique de la structure de refroidissement proposée.  $T_a$  (K) est la température ambiante ;  $T_j$  (K) représente la température de jonction ;  $R_{hc}$  (K/W) est la résistance thermique correspondant à l'effet de convection entre la source de chaleur et la périphérie ;  $R_{jp}$  (K/W) est la résistance thermique latérale entre les modules Peltier et la source de chaleur ;  $R_{hs}$  (K/W) est la résistance thermique du radiateur ;  $Q_{pc}$  (W) représente des pertes supplémentaires dans la structure. Les autres composants ( $Q_c$ ,  $S_m$ ,  $\lambda_m$  et  $R_m$ ,  $Q_h$ ) sont des paramètres du modèle des modules de Peltier.

Le modèle 1D proposé permet de prédire les performances thermiques de la structure de refroidissement de faire un bilan de puissance au niveau des modules Peltier. Ce modèle

léger permet de tester différentes options et d'évaluer le coefficient de performance ( $COP=Q_c/Q_{ed}$ ) de la structure étudiée.

Le modèle 1D a été validé par des expérimentations en utilisant le banc d'essai montré à la Figure 10 et la Figure 11. La méthode calorimétrique mise en œuvre permet de mesurer le flux de chaleur total évacué par l'une des faces des modules Peltier  $Q_h$  (W). Les modules Peltier CP39236 [188], CP30238 [189] et CP 60133 [190] testés dans ce travail expérimental sont distribués par CUI Inc.

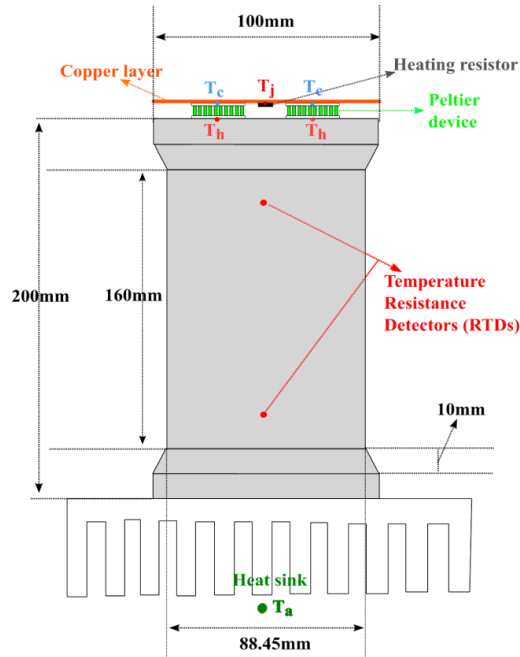


Figure 10: Schématique de principe du banc d'essai permettant la mesure de flux de chaleur par une méthode calorimétrique

Dans notre travail expérimental, nous sommes assurés que la majorité des pertes de puissance générées par l'élément chauffant et par le module Peltier passe par la colonne de mesure. La température de l'élément chauffant est mesurée par un thermocouple et  $Q_h$  est obtenue via la mesure de la différence de température entre deux résistances Platine (La résistance thermique de la colonne en duralumin est de  $0.187 K/W$  a été calibrée au préalable). Différents courants (variant de 0 à 2.5A pour les produits CP39236 et CP30238, de 0 à 4A pour le produit CP60133) sont injectés dans les modules Peltier afin d'évaluer les performances de refroidissement.

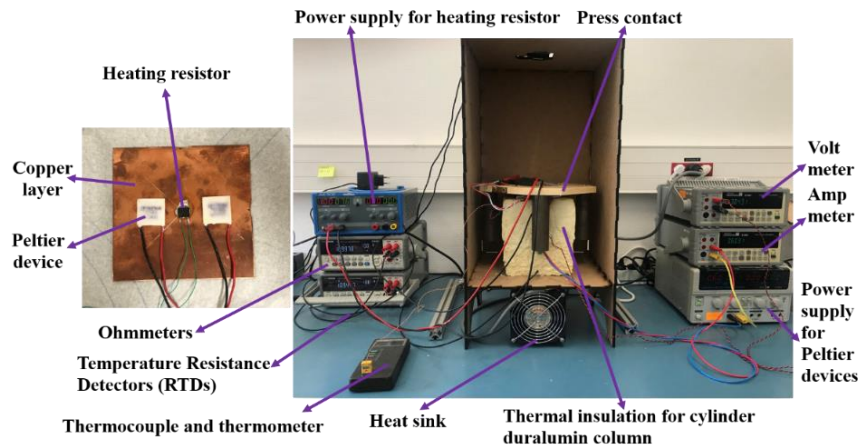


Figure 11: Banc d'essai permettant de mesurer le flux de chaleur par une méthode calorimétrique

Tout d'abord, le modèle 1D proposé a été validé par comparaisons des résultats de simulation avec les résultats expérimentaux (Voit Figure 12).

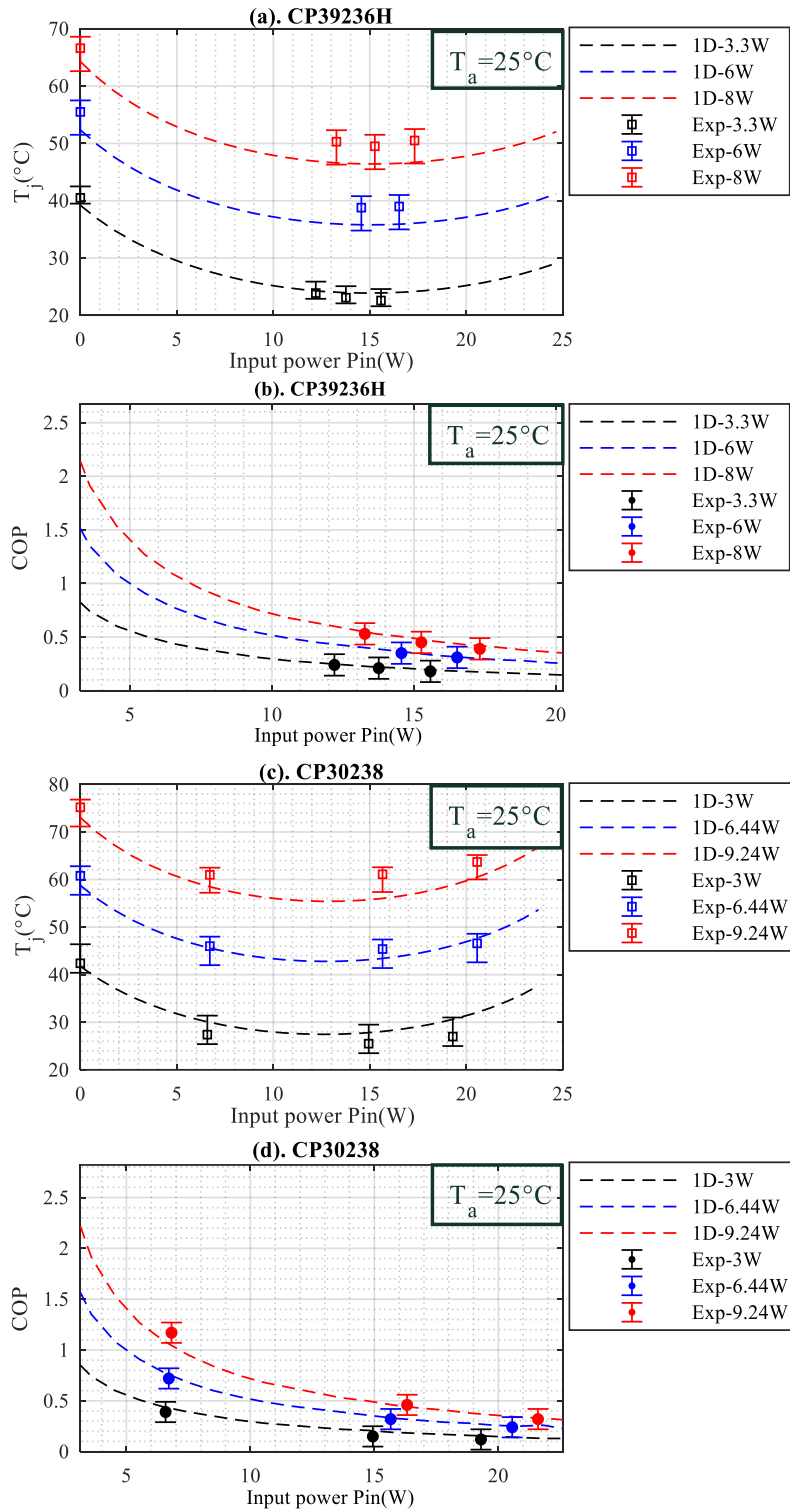


Figure 12: Comparaisons des résultats des simulations avec les résultats expérimentaux. (a). Évolution de la température de jonction  $T_j$  ( $P_m$ ) en utilisant des modules CP39236H ; (b). Évolution du COP des modules Peltier CP39236H ; (c). Évolution de la température de jonction  $T_j$  ( $P_m$ ) en utilisant des modules CP30238 ; (d). Évolution du COP des modules Peltier CP30238. La température ambiante  $T_a$  est de  $25^\circ\text{C}$ .

Le modèle 1D est ensuite utilisé pour prédire les performances thermiques de la structure d'assemblage proposée. Comme montré dans Figure 13, l'effet de refroidissement des modules Peltier est lié à la puissance électrique  $P_{in}$  injectée et à la puissance thermique à

drainer. On peut donc montrer qu'il est possible de contrôler la température de jonction de l'élément chauffant et mettre en œuvre une stratégie permettant de maintenir la température de cet élément à une valeur fixe sur une certaine plage de puissance injectée. Il est également possible d'opter pour une stratégie limitant la température maximum et réduisant la consommation électrique des modules Peltier lorsque les flux de chaleur à dissiper sont faibles.

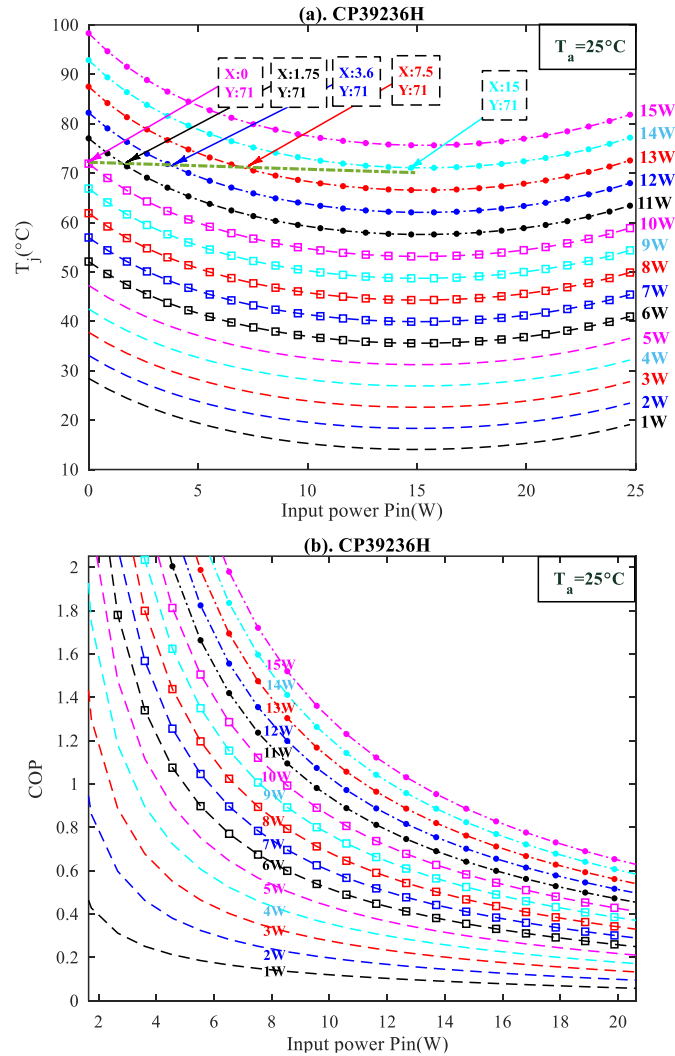


Figure 13: Résultats prédits à partir du modèle 1D en utilisant les modules Peltier CP39236H. (a). Profil de la température de jonction  $T_j(P_{in})$  ; (b). Profil du COP ( $P_{in}$ ). La température ambiante  $T_a$  est de  $25^\circ\text{C}$ .

L'influence du nombre d'éléments des modules Peltier  $N$  a également été étudié comme montré dans la figure 14.

On constate que la puissance thermique soutirée par les modules augmente avec le nombre d'éléments. Pour illustrer ceci, la diminution maximale de la température  $\Delta T_{jmax}$  ( $^\circ\text{C}$ ) obtenue pour différents nombres d'éléments est donnée dans le tableau ci-dessous :

Tableau 1: La diminution maximale de la température  $\Delta T_{jmax}$  ( $^\circ\text{C}$ ) des trois scénarios de refroidissement

N	$P_{heat} = 4\text{W}$	$P_{heat} = 6\text{W}$	$P_{heat} = 8\text{W}$	$P_{heat} = 10\text{W}$
128	15.2	16.1	17.1	18.3
192	21	22.3	23.9	25.7
256	23.6	25.1	26.7	28.7

De plus, le COP est amélioré lorsqu'on augmente le nombre d'éléments des modules Peltier pour le même effet de refroidissement. Par exemple, pour une température de

l'élément chauffant souhaitée  $T_j$  de  $55\text{ }^\circ\text{C}$ , les valeurs des coefficients COPs sont indiquées dans le tableau ci-dessous :

Tableau 2: Valeurs des coefficients COPs des trois scénarios pour maintenir  $T_j$  à  $55\text{ }^\circ\text{C}$

Pheat (W)	COP		
	N=128	N=192	N=256
4	Infinity (Pin=0)	Infinity	Infinity
6	5.5	16.21	Infinity
8	0.26	1.27	3.84
10	Inability	Inability	0.88

Ce résultat démontre que l'efficacité du système de refroidissement s'accroît lorsque le nombre d'éléments Peltier augmente pour une température de l'élément chauffé donnée.

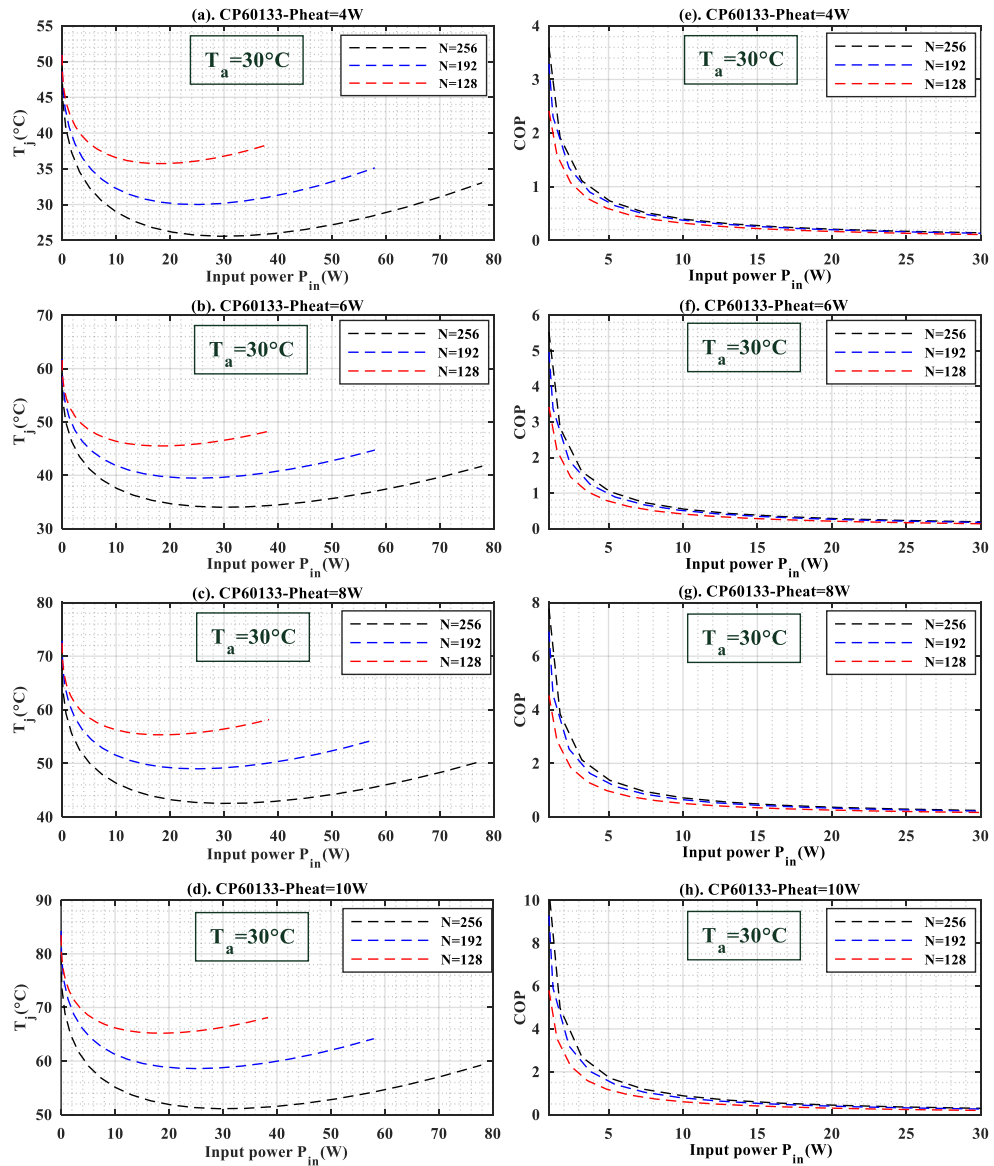


Figure 14: Résultats estimés par le modèle électrothermique pour les structures avec différents  $N$ . (a). Profil  $T_j(P_{in})$  pour évacuer 4 W de flux de chaleur ; (b). Profil  $T_j(P_{in})$  pour évacuer 6 W de flux de chaleur ; (c). Profil  $T_j(P_{in})$  pour évacuer 8 W de flux de chaleur ; (d). Profil  $T_j(P_{in})$  pour évacuer 10 W de flux de chaleur ; (e). Profil d'efficacité COP ( $P_{in}$ ) pour évacuer 4 W de flux de chaleur ; (f). Profil d'efficacité COP ( $P_{in}$ ) pour évacuer 6 W de flux de chaleur ; (g). Profil d'efficacité COP ( $P_{in}$ ) pour évacuer 8 W de flux de chaleur ; (h). Profil d'efficacité COP ( $P_{in}$ ) pour évacuer 10 W de flux de chaleur. La température ambiante  $T_a$  est de  $30\text{ }^\circ\text{C}$ .



# TABLE OF CONTENTS

<b>Remerciements .....</b>	<b>I</b>
<b>Résumé en français.....</b>	<b>II</b>
<b>List of figures .....</b>	<b>XIV</b>
<b>List of tables.....</b>	<b>XVIII</b>
<b>General Introduction .....</b>	<b>1</b>
<b>CHAPTER 1. State of The Art .....</b>	<b>3</b>
1.1. Introduction .....	3
1.2. Power Converters .....	3
1.2.1. Semiconductor Components.....	3
1.2.2. Multilevel Converters .....	6
1.3. Power Packaging .....	8
1.3.1. Introduction .....	8
1.3.2. 2D Packaging with Direct Bonded Circuit (DBC) Technology .....	8
1.3.3. 3D Packaging with Printed Circuit Board (PCB) Technology.....	9
1.3.4. Conclusion .....	11
1.4. Thermal Analysis of Power Electronics Systems .....	11
1.4.1. Introduction .....	11
1.4.2. Thermal Measurement Methods.....	15
1.4.3. Thermal Management Solutions.....	25
1.5. Summary .....	34
<b>CHAPTER 2. Thermal Instrumentations .....</b>	<b>36</b>
2.1. Introduction .....	36
2.2. Test Bench.....	36
2.2.1. Establishment.....	36
2.2.2. RTD Sensor (PT 100) Calibration .....	36
2.2.3. Thermal Conductivity of Duralumin $\lambda_{\text{dura}}$ (W/mK).....	38
2.2.4. Temperature Measurement Equipments .....	39
2.2.5. Applied Softwares .....	40
2.3. Chip Attachment on The PCB Substrate.....	43
2.3.1. Preparation of PCB Substrate .....	43
2.3.2. Chip Soldering.....	44
2.4. Through-Hole Electroplating .....	45
2.5. Summary .....	45
<b>CHAPTER 3. Optimization of thermal vias .....</b>	<b>47</b>
3.1. Introduction .....	47
3.2. Analytical Analysis .....	47

3.2.1.	PCB Substrate with One Individual Thermal Via .....	47
3.2.2.	PCB Substrate with Two Thermal Vias .....	48
3.2.3.	PCB Substrate with Multiple Vias.....	49
3.3.	3D FEM Analysis.....	51
3.3.1.	Number of Thermal Vias N.....	52
3.3.2.	Via-Cluster Surface Ratio $R_{o1}$ .....	53
3.3.3.	Via Diameter Ratio $R_{o2}$ .....	54
3.3.4.	Via Plating Thickness Ratio $R_{o3}$ .....	54
3.3.5.	Via Pattern .....	55
3.3.6.	Copper Thickness on The PCB Substrate.....	57
3.4.	Experimental Results and Discussions.....	59
3.5.	Conception of The Inverse Thermal Model .....	63
3.5.1.	Introduction .....	63
3.5.2.	Steady State Inverse Heat Conduction Model (IHCM).....	63
3.5.3.	Dissipated Power Prediction.....	65
3.5.4.	Dissipated Power and Thermal Conductivity Prediction .....	67
3.6.	Summary .....	69
<b>CHAPTER 4. Thermoelectric Cooling .....</b>		<b>71</b>
4.1.	Introduction .....	71
4.2.	3D FEM Analysis.....	72
4.2.1.	Placement of The Peltier Device $d_{gp}$ and Number of Peltier Elements $N_p$ .....	73
4.2.2.	Copper Thickness on The PCB Substrate.....	75
4.2.3.	Modeling of The Peltier Device CP39236H.....	76
4.3.	1D Electro-Thermal Modeling .....	80
4.3.1.	1D Modeling of The Cooling Structure.....	81
4.3.2.	1D and 3D Simulation Results and Discussions .....	83
4.4.	Experimental Validation .....	85
4.4.1.	Test Bench .....	85
4.4.2.	Results and Discussions.....	87
4.4.3.	Influences of Number of Peltier Elements N.....	89
4.5.	Summary .....	93
<b>Conclusions and Perspectives.....</b>		<b>95</b>
<b>References .....</b>		<b>97</b>
<b>Annex A.....</b>		<b>107</b>
<b>Annex B .....</b>		<b>109</b>
<b>Annex C.....</b>		<b>112</b>
<b>Annex D.....</b>		<b>116</b>

## LIST OF FIGURES

Fig.1. Power density and costs evolution [2] .....	1
Fig.1-1. Summary of Si, SiC and GaN relevant material properties [14] .....	4
Fig.1-2. Normally-on GaN device built on a silicon substrate (Source: MOUSER ELECTRONICS [15]) .....	5
Fig.1-3. (a) Three-level NPC featuring IGCTs; (b) Three-level FC featuring MV-IGBTs; (c) Five-level CHB featuring LV-IGBTs [11] .....	6
Fig.1-4. Switching process of an IGBT with several commutation cycles [30].....	7
Fig.1-5. Schematic view of a power module and example of 2D packaging inverter arm [10] .....	9
Fig.1-6. Thin 60-W offline converter with PCB integrated transformer and capacitors [40] .....	10
Fig.1-7. Thermal simulation results for different GaN prototypes [10] .....	11
Fig.1-8. Bounded spatial thermal region .....	12
Fig.1-9. The Foster (top) and Cauer (bottom) canonic forms of thermal networks .....	13
Fig.1-10. Calculation results for Si structures by Cauer modeling [48].....	13
Fig.1-11. Layered approach adopted for the electro-thermal modeling of integrated power electronics modules [49].....	14
Fig.1-12. Heat convection .....	14
Fig.1-13. Heat radiation.....	15
Fig.1-14. Schematic of high power IGBT module modeled in ANSYS Icepak for FEM analysis [65].....	17
Fig.1-15. Electro-thermal model in Saber [71] .....	18
Fig.1-16. Schematic for measurement of power losses with the electrical method [84].....	20
Fig.1-17. Double pulse waveform [86] .....	20
Fig.1-18. SiC MOSFET switch on and switch off transient [88].....	21
Fig.1-19. Schematic open, single-cased closed and double cased closed type [107].....	23
Fig.1-20. Overview of different implemented calorimeters and their reached accuracy [107] .....	23
Fig.1-21. Block diagram of calorimeter [95].....	23
Fig.1-22. Schematic of calorimetric method with heat-flux sensors PT100 [115] .....	24
Fig.1-23. Schematic of proposed apparatus.1: DUT; 2: Inner Al cover; 3: Outer Al cover; 4: Al base plate I; 5: Al base plate II; 6: Heat sink; 7: Heater; 8: Thermocouple; 9: Fins; 10: Insulated material; 11: Heat flux sensor; 12: TE module.[110] .....	25
Fig.1-24. Thermal management - a continuous process during system engineering [117].	26
Fig.1-25. Different air cooling systems design with heat sinks [119].....	27
Fig.1-26. Different liquid cooling solutions [122] .....	28
Fig.1-27. Thermal resistance of commercial available cold plates as a function of water flow [124] .....	28
Fig.1-28. Section view of main heat transfer path for a 2 layer PCB with thermal vias [131] .....	29
Fig.1-29. Curves of ZT versus temperature for different materials [144].....	31
Fig.1-30. Schematic of thermoelectric module operation in cooling mode .....	31
Fig.1-31. Pyrolytic graphite sheet from Panasonic PGS product datasheet [155] .....	33
Fig.1-32. Hybrid solid- and liquid-cooling designs for IGBT isothermalization [116] .....	33
Fig.1-33. Embedded thermal solutions for PCB structures using PGS and heat pipe techniques [126] .....	34

Fig.2-1. Power loss measurement test bench.....	36
Fig.2-2. RTD sensor PT 100 (Online source: flukecal.com).....	37
Fig.2-3. Test bench for calibrating RTD sensors .....	37
Fig.2-4. Temperature differences between two RTDs following temperature of forced-air oven .....	38
Fig.2-5. Temperature differences between two RTDs after calibration .....	38
Fig.2-6. Measured relationship between input power and temperature difference between two RTDs.....	39
Fig.2-7. Thermography camera FLIR T450sc [157] .....	39
Fig.2-8. Thermal imaging of a simple PCB structure .....	40
Fig.2-9. K&T type thermocouple (ANSI MC96.1) [159] and thermometer .....	40
Fig.2-10. 3D model of the PCB structure with soldered Si chip (dimensions in mm).....	41
Fig.2-11. Top and section view of lumped parameter model for the PCB structure.....	42
Fig.2-12. Steady-state thermal network for the PCB structure .....	42
Fig.2-13. 3D Thermal simulation of the PCB structure .....	43
Fig.2-14. Fabrication process of PCB [160].....	44
Fig.2-15. Prepared PCB substrate for chip soldering .....	44
Fig.2-16. Chip soldering process.....	45
Fig.2-17. Electroplated vias in the standard PCB substrate .....	45
Fig.3-1. Typical PCB structure with a single thermal via .....	47
Fig.3-2. Analytical model for one single via PCB structure .....	48
Fig.3-3. Top and Section view of the PCB substrate with two thermal vias.....	49
Fig.3-4. Analytical thermal model for PCB structure with two thermal vias.....	49
Fig.3-5. Top and section view of the PCB substrates with multiple thermal vias in pattern 1 .....	50
Fig.3-6. Two typical via-cluster patterns.....	50
Fig.3-7. Top and Section view of the studied PCB assembly .....	51
Fig.3-8. Evolution of thermal resistance ratio $R_{oa}$ following the number of vias .....	52
Fig.3-9. 3D FEM simulations with different number of thermal vias but the same ratios of $R_{o1}$ , $R_{o2}$ , $R_{o3}$ .....	53
Fig.3-10. Evolution of thermal resistance ratio $R_{oa}$ following the ratio of via-cluster surface $R_{o1}$ .....	54
Fig.3-11. Evolution of thermal resistance ratio $R_{oa}$ following the ratio of via diameter $R_{o2}$ .....	54
Fig.3-12. Evolution of thermal resistance ratio $R_{oa}$ following the ratio of via plating thickness $R_{o3}$ .....	55
Fig.3-13. 3D FEM simulations with different ratio of via plating thickness .....	55
Fig.3-14. 3D FEM simulations with different via patterns .....	56
Fig.3-15. Arrangement of thermal vias in two patterns with the same available via-cluster surface.....	56
Fig.3-16. Evolution of the average thermal resistance ratio in two patterns .....	56
Fig.3-17. Section view of the 3D model for DBC or PCB structure.....	57
Fig.3-18. Thermal resistance evolution following the copper thickness.....	58
Fig.3-19. 3D thermal simulation results for PCB structures having 10kV breakdown voltage .....	58
Fig.3-20. Structure of double-sides cooling solution for the PCB .....	59
Fig.3-21. Thermal resistance evolution following the copper thickness for the same breakdown voltage 10kV.....	59

Fig.3-22. Four PCB structures with different via patterns .....	59
Fig.3-23. PCB dimensions and via parameters .....	60
Fig.3-24. 3D FEM simulations for PCB structures with different via parameters.....	60
Fig.3-25. Temperature measurements of the heating source and comparisons with 3D FEM simulations.....	62
Fig.3-26. PCB structure with embedded GaN chip.....	64
Fig.3-27. Parameters estimation step for DHCM.....	64
Fig.3-28. Input power estimation step for IHCM.....	64
Fig.3-29. Power prediction with 5 temperature sensors (Annex A).....	65
Fig.3-30. Power prediction with 10 temperature sensors (Annex B).....	66
Fig.3-31. Temperature measurements on the top surface of PCB structure by 3D FEM simulations.....	66
Fig.3-32. Power predictions in 2 embedded GaN dies with 5 temperature sensors (Annex C) .....	67
Fig.3-33. Power prediction for IHCM with two unknown system parameters (Annex D). 68	
Fig.3-34. Prediction of thermal conductivity of the PCB substrate for IHCM with two unknown system parameters (Annex D) .....	68
Fig.3-35. Power prediction with less temperature sensors (Annex D).....	69
Fig.3-36. Thermal conductivity prediction with less temperature sensors (Annex D) .....	69
Fig.4-1. PCB structure with Peltier modules.....	71
Fig.4-2. One element of a TEC device .....	71
Fig.4-3. Working mode of the Peltier device .....	72
Fig.4-4. Examples of 3D FEM simulations for PCB structures with different distance between the chip and the Peltier devices. A heat dissipation of 1 W in the chip, an equivalent convection heat-transfer coefficient of 15 W/(m <sup>2</sup> K) from all external surfaces (except the bottom layer and the top TEC plate) to the ambient, a copper thickness $e_c$ of 500 $\mu$ m on the top of the PCB substrate and an optimum input electric power of 0.4 V in the Peltier modules are applied. The ambient temperature is at 25 °C.....	74
Fig.4-5. Thermal resistance evolution following the distance $d_{gp}$ . A heat dissipation of 1 W in the chip, an equivalent convection heat-transfer coefficient of 15 W/(m <sup>2</sup> K) from all external surfaces (except the bottom layer and the top TEC plate) to the ambient and a copper thickness $e_c$ of 500 $\mu$ m on the top of the PCB substrate are applied. The ambient temperature is at 25 °C.....	75
Fig.4-6. Thermal performance comparison between PCB and DBC structures. A heat dissipation of 1 W in the chip, an equivalent convection heat-transfer coefficient of 15 W/(m <sup>2</sup> K) from all external surfaces (except the bottom layer and the top TEC plate) and an ambient temperature of 25 °C are applied. ....	76
Fig.4-7. 3D model of Peltier device CP39236H.....	76
Fig.4-8. A simulated example for the 3D FEM model of product CP39236H built in COMSOL with the input current $I$ equaling 1.56 A, the temperature of the cold side $T_c$ equaling 20 °C, the temperature of the hot side $T_h$ equaling 50 °C. ....	77
Fig.4-9. Simulation results of the input voltage versus temperature difference.....	78
Fig.4-10. Simulation results of the heat absorbed versus temperature difference.....	78
Fig.4-11. Simulation results of the relationship between COP and input current.....	78
Fig.4-12. CP39236H performances from datasheet [172].....	79
Fig.4-13. Cooling performances of Peltier modules for PCB structures.....	80
Fig.4-14. Schematic of proposed cooling structure with Peltier devices beside the heating source.....	80
Fig.4-15. Thermal resistance network of the studied structure .....	82

Fig.4-16. Top view for heating resistor and Peltier devices.....	83
Fig.4-17. An example of 3D FEM simulation for the designed cooling structure and its section view. The PCB structure is put on a duralumin column for power loss measurement. The bottom side of the column is set at 25 °C. Heat power in the heat source $P_{\text{heat}} = 7.6\text{W}$ and the input current in each Peltier device is 1.5 A. ....	83
Fig.4-18. 1D electro-thermal model of the cooling structure built by Matlab Simulink.....	84
Fig.4-19. Thermal simulations for 1D analytical and 3D FE models. (a). Junction temperature profile $T_j$ (I) when dissipating 5 W from the heating source; (b). Cooling efficiency profile COP (I) when dissipating 5 W from the heating source; (c). Junction temperature profile $T_j$ (I) when dissipating 7.6 W from the heating source; (d). Cooling efficiency profile COP (I) when dissipating 7.6 W from the heating source. The ambient temperature is 25 °C. ....	85
Fig.4-20. Test bench for validating the thermal models of the PCB structure with Peltier devices .....	86
Fig.4-21. Power loss measurement based on calorimetric method with duralumin column	86
Fig.4-22. Experimental and estimated results with Peltier devices CP39236H. (a). Junction temperature profile $T_j$ (I) when dissipating 5 W from the heating source; (b). Cooling efficiency profile COP (I) when dissipating 5 W from the heating source; (c). Junction temperature profile $T_j$ (I) when dissipating 7.6 W from the heating source; (d) Cooling efficiency profile COP (I) when dissipating 7.6 W from the heating source. The ambient temperature is 25 °C. ....	87
Fig.4-23. Experimental and estimated results with Peltier devices CP39236H and CP30238. (a). Junction temperature profile $T_j$ ( $P_{\text{in}}$ ) with CP39236H; (b). Cooling efficiency profile COP ( $P_{\text{in}}$ ) with CP39236H; (c). Junction temperature profile $T_j$ ( $P_{\text{in}}$ ) with CP30238; (d) Cooling efficiency profile COP ( $P_{\text{in}}$ ) with CP30238. The ambient temperature is 25 °C..	88
Fig.4-24. Estimated results with Peltier device CP39236H. (a). Junction temperature profile $T_j$ ( $P_{\text{in}}$ ). (b). Cooling efficiency profile COP ( $P_{\text{in}}$ ). The ambient temperature is 25 °C. ....	89
Fig.4-25. Experimental and estimated results with Peltier devices CP60133. (a). Junction temperature profile $T_j$ (I); (b). Cooling efficiency profile COP (I); (c). Junction temperature profile $T_j$ ( $P_{\text{in}}$ ); (d) Cooling efficiency profile COP ( $P_{\text{in}}$ ). The ambient temperature is 30 °C. ....	90
Fig.4-26. Estimated results with Peltier devices CP60133. (a). Junction temperature profile $T_j$ (I) for dissipating 4 W; (b). Junction temperature profile $T_j$ (I) for dissipating 6 W; (c). Junction temperature profile $T_j$ (I) for dissipating 8 W; (d). Junction temperature profile $T_j$ (I) for dissipating 10 W; (e). Cooling efficiency profile COP (I) for dissipating 4 W; (f). Cooling efficiency profile COP (I) for dissipating 6 W; (g) Cooling efficiency profile COP (I) for dissipating 8 W; (h). Cooling efficiency profile COP (I) for dissipating 10 W. The ambient temperature is 30 °C. ....	91
Fig.4-27. Estimated results with Peltier devices CP60133. (a). Junction temperature profile $T_j$ ( $P_{\text{in}}$ ) for dissipating 4 W; (b). Junction temperature profile $T_j$ ( $P_{\text{in}}$ ) for dissipating 6 W; (c). Junction temperature profile $T_j$ ( $P_{\text{in}}$ ) for dissipating 8 W; (d). Junction temperature profile $T_j$ ( $P_{\text{in}}$ ) for dissipating 10 W; (e). Cooling efficiency profile COP ( $P_{\text{in}}$ ) for dissipating 4 W; (f). Cooling efficiency profile COP ( $P_{\text{in}}$ ) for dissipating 6 W; (g) Cooling efficiency profile COP ( $P_{\text{in}}$ ) for dissipating 8 W; (h). Cooling efficiency profile COP ( $P_{\text{in}}$ ) for dissipating 10 W. The ambient temperature is 30 °C. ....	92

## LIST OF TABLES

Table 1.1. Physical characteristics of Si and main wide band gap semiconductors [13] .....	4
Table 1.2. Ceramic materials used for DBC substrate [38].....	9
Table 1.3. Different loss-calculation models concerning IGBT devices in literatures [73] 19	
Table 2.1. Thermal to electrical analogy .....	41
Table 3.1. Dimensions of the assembly and material properties .....	51
Table 3.2. Pitch distance and number of vias for different thermal models.....	52
Table 3.3. Via parameters used to create different 3D FE models.....	53
Table 3.4. Dimensions and thermal properties of each layer for the PCB structures with thermal vias .....	61
Table 3.5. Comparisons between simulation and experimentation results .....	62
Table 4.1. Peltier element parameters .....	73
Table 4.2. Peltier element parameters and ceramic substrate dimensions of each side .....	76
Table 4.3. Dimensions and calculated parameters of Peltier devices.....	81
Table 4.4. Thermoelectric material properties .....	81
Table 4.5. Thermal to electrical analogy .....	82
Table 4.6. Maximum decrease of the junction temperature $\Delta T_{jmax}$ ( $^{\circ}C$ ) .....	91
Table 4.7. COP values of the three cooling scenarios when keeping $T_j$ at $55^{\circ}C$ .....	92

# GENERAL INTRODUCTION



# GENERAL INTRODUCTION

In last four decades, power electronics technology has gone through dynamic evolution due to the “more electric” concept. “Recently, its applications are fast expanding in industrial, commercial, residential, transportation, utility, aerospace, and military environments primarily due to reduction of cost, size, and improvement of performance” [1]. As shown in Fig.1 [2], power converters are constantly trending towards lower cost, higher efficiency, and higher power density.

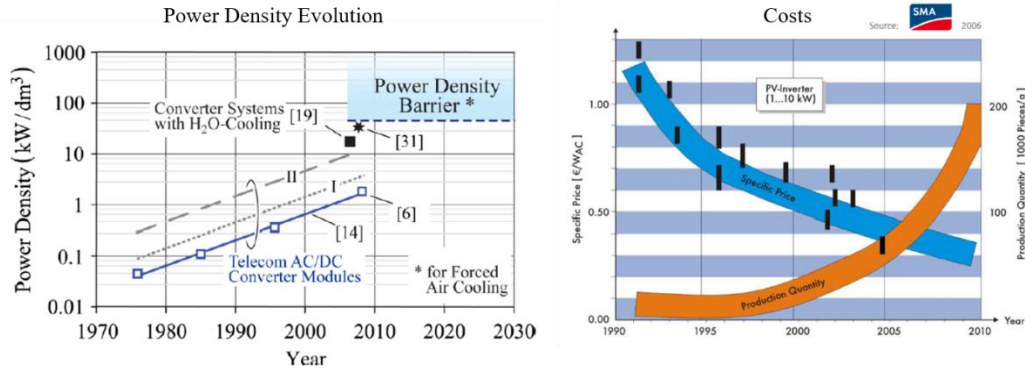


Fig.1. Power density and costs evolution [2]

In addition, since characteristics of Si devices have reached its natural limitation, Wide Band Gap (WBG) components in Gallium Nitride (GaN) or Silicon Carbide (SiC) with lower on-state resistance ( $R_{on}$  ( $\Omega$ )) and higher switching frequency have recently emerged. Accompanied with the fast switching speed benefit of WBG devices, inevitably there is higher  $dv/dt$  and  $di/dt$  introduced at the same time, which can hardly be observed in comparatively slow Si Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Current carrying capability is ultimately a thermal issue. In a power module, the package itself generates conduction losses in the metal interconnections, power terminals, wire bonds, and solder interfaces. Power semiconductors offer conduction losses as well as switching losses resulting from turn-on, turn-off, and diode reverse recovery energies. A well optimized system will work to reduce the magnitude of the generated losses as well as to provide an effective method for heat removal purpose [3-5].

Increased power density and advances in Wide Band Gap (WBG) semiconductors require improvements in the integration technology, packaging technology as well as thermal management solutions to adapt to their high temperature operation advantage. Today, in many applications such as aerospace and aircraft, desired reliable operating temperature is from  $-55\text{ }^{\circ}\text{C}$  to  $250\text{ }^{\circ}\text{C}$  [6]. However, available packaging technologies, passives and peripheral components, solder materials, reliability considerations and cost presently limit the junction temperatures to  $\sim 175\text{ }^{\circ}\text{C}$  even though the WBG semiconductor devices can, in principle, operate at much higher junction temperatures [7-9].

In order to mitigate these side effects and thus fully utilize the benefits of these unique devices, advanced module packaging and efficient cooling systems are needed.

“Among the mature technologies used in power electronics domain, usually, the Printed Circuit Board (PCB) technology addresses today small and medium power (a few hundreds of Watts up to a few kW), and Direct Bonded Copper (DBC) based technology is used for medium and high power” [10]. To avoid the use of wire bondings, PCB technology is preferred to realize 3D integration of power components by embedding technologies. But

PCB substrate in material of FR4 has poor thermal conductivity ( $<1.5 \text{ W/mK}$ ), which brings us big challenges in thermal dissipation of the total structure.

Therefore, this research work will be devoted to develop cooling solutions for embedded PCB structures. Three different cooling methods have been studied.

- The first one allows to optimize the classical solution of creating thermal vias in the PCB substrates. The main goal here is to develop a referenced criterion of thermal via parameters for manufacturing.
- The second solution is to increase the thickness of copper layer on the top of the PCB substrate. This solution could enhance lateral heat spreading effect along the copper layer, thus increase the heat dissipation surface.
- The third one is a recent solution in use of thermoelectric cooling (TEC) devices. Compared to DBC structure with the same dielectric strength, this solution is dedicated to develop a competitive PCB structure in thermal aspects.

This thesis is organized as follows in five parts:

- In the first chapter, a brief overview concerning the development of power electronics systems and general context of this work will be presented to introduce basic concepts of thermal management needed throughout this thesis. Then, the state-of-art of power packaging, thermal measurement of the power systems as well as different thermal management solutions will be discussed. In particular, this chapter will be devoted to compare various modelling methods based on different softwares in literatures;
- The second chapter will present all used instrumentations in the process of establishing the test bench for temperature and power loss measurement. Schematic of the test bench, calibration process of some devices such as Resistance Temperature Detector (RTD) sensors, as well as chip soldering process will be introduced;
- The third chapter covers two cooling methods: the optimization of thermal vias and increasing the copper thickness of PCB. Different modeling methods: analytical and 3D Finite Element (FE) methods have been used to analyze the cooling effect of different via parameters including via diameter, number of vias, via pattern, plating thickness of copper and pitch distance between two vias etc.;
- In the fourth chapter, thermoelectric (TEC) cooling devices of Peltier modules based on Peltier effect will be described. Influences of different Peltier parameters will be discussed to optimize their thermal cooling performances.
- The last chapter dedicated to the general conclusion gives also some perspectives.

## CHAPTER 1. STATE OF THE ART

- 1.1. Introduction
- 1.2. Power Converters
- 1.3. Power Packaging
- 1.4. Thermal Analysis of Power Electronics Systems
- 1.5. Summary



# CHAPTER 1. STATE OF THE ART

## 1.1. INTRODUCTION

For completeness and better understanding of the reasons and recent advances in thermal management solutions, it is necessary to cover the concerned power converters' topologies. Firstly, different components of power converters and well-established packaging technologies for power converters will be briefly introduced and referred to existing literatures. Then, principle of different thermal management solutions will be discussed.

## 1.2. POWER CONVERTERS

Generally, power converters consist of the totality of the equipments between source and load. The main objective is to convert currents form (AC, DC), or the voltage magnitude, or the frequency range, or a combination of that and also to control electromagnetic energy flow between an electric source and load.

Power converters are a combination of power devices which can be divided into active components and passive components. In a power converter, active components are made by association of a power transistor and its driver. By association of such elementary power switches many conversion functions can be achieved. This structure is a natural interface between digital controllers and the world of power conversion and play the role of amplifier to boost power. But they are mainly used in power converters to format the voltages and the currents by removing some unwanted frequency components. Basic passive components include capacitors and inductors.

### 1.2.1. Semiconductor Components

Evolutions of the power converter topologies in order to improve power ratings, efficiency, reliability, performance and costs are directly related to the evolution of power semiconductor devices, which constitute the heart of power converters. In the last decades, Silicon (Si) devices (diodes, Insulated Gate Bipolar Transistors (IGBTs), MOSFETs, etc.) dominate the market because of its mature and well-established technology. However, Si devices approach theoretical limitations of the Si material. For example, Si-based device cannot sustain temperature higher than 200 °C as well as very high voltage (Si IGBT are limited to 6.6 kV). *“Generally speaking, the medium-voltage range is considered in the power converter industry from 2.3 kV to 6.6 kV for high power in the range of 1-50 MW”* [11]. So, Wide Band Gap (WBG) semiconductors like Gallium Nitride (GaN) and Silicon Carbide (SiC) have emerged because their intrinsic performances exceed those of Silicon [12, 13].

#### 1.2.1.1. Materials

Some of the main characteristics for WBG materials that can be compared to those of Si are shown in Fig.1-1 [14] and Table 1.1 [13]. These materials have superior electrical characteristics compared to Si. These properties lead to improve the power devices characteristics in several domains as they allow to lower the conduction and the switching losses. It is also possible to operate at a higher maximum junction temperature and, since the thermal properties of the WBG semiconductors are better than those of Si, the thermal management of the power dissipation can be facilitated.

These advantages allow to operate at higher frequencies and theoretically to higher ambient temperature. The emergence of new power electronics devices based on WBG semiconductor materials will result in substantial improvements in the performances of

power systems in terms of faster switching speed, higher blocking voltages, higher efficiency, and higher reliability as well as higher temperature tolerance.

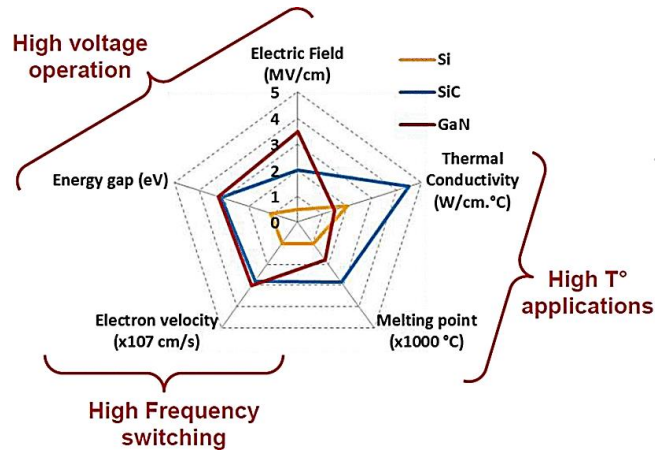


Fig.1-1. Summary of Si, SiC and GaN relevant material properties [14]

Table 1.1. Physical characteristics of Si and main wide band gap semiconductors [13]

Property	Si	6H-SiC	4H-SiC	GaN
Bandgap, $E_g$ (eV)	1.12	3.03	3.26	3.45
Dielectric constant, $\epsilon_r$	11.9	9.66	10.1	9
Electric breakdown field, $E_c$ (kV/cm)	300	2500	2200	2000
Electron Mobility, $\mu_n$ (cm <sup>2</sup> / V.s)	1500	500	1000	1250
Thermal conductivity, $\lambda$ (W/m.K)	150	490	490	130
Saturate Electron Drift Velocity, $v_{sat}$ (x 10 <sup>7</sup> cm/s)	1	2	2	2.2

### 1.2.1.2. GaN Devices

GaN devices have a lateral structure because they are based on the high electron mobility transistor (HEMT) structure. As we can see in Fig. 1-2 [15], a GaN HEMT is built on a silicon substrate, with a lateral two-dimensional electron gas (2DEG) channel formed on an AlGaN/GaN hetero-epitaxy structure [15, 16]. Like a Si MOSFET, a GaN transistor has source, drain and gate terminals, and the key figures of merit are  $R_{on}$  and the breakdown voltage.

Compared to Si devices, GaN devices have three main advantages:

- **Lower  $R_{on}$ :** theoretically about three orders of magnitude smaller than conventional Si devices because of the high critical electric field which allows to minimize the device length and the high concentration 2DEG with high carrier mobility [17], thus reducing a major source of static losses and inefficiency when at on-state.
- **Faster on/off switching:** switching hundreds of volts in nanoseconds, supporting the design of supplies that can switch large currents at rates of several megahertz (some latest-generation devices can operate in the hundreds of MHz) [15].
- **Smaller die size:** this gives us the potential to develop integrated circuits with high power density. For example, the eGaN transistor provided by EPC (40 V-33 A) has a very small die size of  $4075 \times 1602 \times 685 \mu\text{m}$  [18].

There are two types of GaN transistors available on the market:

- **Those operating in depletion mode:** such GaN transistors are normally on. To turn them off, a negative voltage between the drain and the source electrodes is needed. To work around this apparent drawback (for the most popular power converters) and have it in a normally off configuration, they are often packaged

in a cascode configuration with a low-voltage Si MOSFET that reverses this situation [19].

- **Those operating in enhancement mode:** such GaN transistors are normally off (for example when the gate drive voltage is set to zero: left image in Fig.1-2) and are turned on when a positive voltage exceeding the threshold voltage is applied to the gate turned on by positive voltage applied to the gate (center and right images in Fig.1-2).

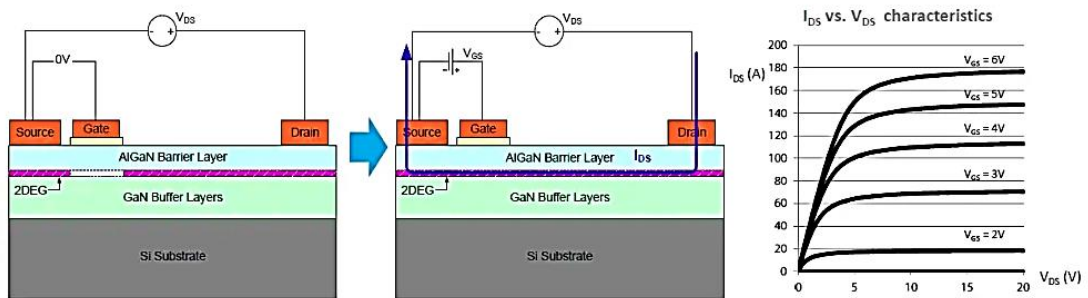


Fig.1-2. Normally-on GaN device built on a silicon substrate (Source: MOUSER ELECTRONICS [15])

### 1.2.1.3. SiC Devices

Those wide bandgap transistors are different from GaN devices. Indeed, the structure of SiC devices is usually vertical like Si power devices. Fast development of SiC technology in recent years is bringing solutions to the many barriers that Si devices have encountered. Besides the same advantages as GaN devices, authors in [20] have summarized following compelling advantages of SiC devices as following:

- **Higher critical electrical field:** It's  $\sim 8$  times higher than that of Si, thus a SiC device is much thinner due to its high dielectric strength and is doped to a much higher level, leading to lower losses.
- **Higher thermal conductivity:** It's  $\sim 3$  times higher than that of Si and heat dissipation by the losses can be conducted with a much lower temperature drop across the semiconductor material.
- **Higher operating temperature:** SiC devices can operate well over  $400^\circ\text{C}$  ( $\sim 150^\circ\text{C}$  for standard Si devices) which allows to increase the possible power density and enables applications in harsh environments.

Today, main commercial available SiC power devices are Schottky diodes, MOSFETs and Bipolar Junction Transistors (BJTs). Authors or manufacturers in [20-22] have characterized these SiC components. Advantages of these components have also been reviewed by authors in [20]:

- **SiC Schottky Diode:** It's the first successfully commercialized SiC power device and has extended the breakdown voltage of a Schottky diode above 1000 V, which had ever been limited below 200 V with Si technology [20].
- **SiC MOSFET:** It's attractive since it is voltage controlled and normally off. And it does not require continuous driving current to maintain the conduction state. Today several components from different manufacturers are available on the market for 1.2 and 1.7 kV and devices with higher breakdown voltage (until 10 kV) have been demonstrated.

- **SiC BJT:** *It can provide the lowest specific  $R_{on}$  that results in the smallest chip size and the smallest parasitic capacitance for a given voltage and current rating, allowing higher switching speed than other SiC switching devices. In addition, SiC BJT has no oxide layer and can operate at higher temperatures than the SiC MOSFET.*

Compared to the best Si IGBTs, SiC devices will improve system efficiency up to 20 % and operate at 2-5 times the switching frequencies [2].

### 1.2.2. Multilevel Converters

The converter topologies can be divided into two main groups: direct and indirect converters. Direct converters are topologies without any energy storage elements. Indirect converter is made of several stages with an energy storage link between them [23]. Besides, according to the nature of the dc link (inductive or capacitive, respectively), converters can be divided into Current Source Converters (CSCs) and Voltage Source Converters (VSCs). *“In addition, VSCs can also be classified into two-level and multilevel converters depending on the number of voltage levels generated at the output”* [23, 24].

Classic multilevel converter topologies (one phase) are shown in Fig.1-3 [11]. They are well established topologies namely the Neutral Point Clamped (NPC), the Cascaded H-Bridge (CHB) and the Flying Capacitor (FC). Operating principles, multilevel waveform generation, special characteristics, modulation schemes and more details as advantages and disadvantages related to the NPC, FC and CHB can be found in [25-29] and will not be covered in this thesis devoted to the present thermal management topics. Generally, multilevel converters have their own potential advantages thanks to their lower output harmonic distortion and also the lower device voltage rating requirements, which can provide a lighter, more efficient and more reliable power converter.

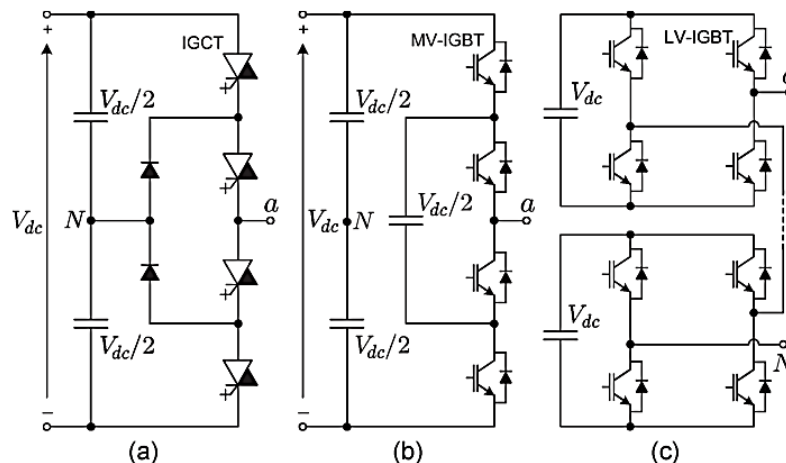


Fig.1-3. (a) Three-level NPC featuring IGCTs; (b) Three-level FC featuring MV-IGBTs; (c) Five-level CHB featuring LV-IGBTs [11]

#### 1.2.2.1. Power Losses Distribution

Power-supply efficiency is a critical criterion for power converters. The efficiency of the chosen power solutions relates to system power losses and thermal performances of switching cells and other components. An ideal switch implies zero losses, thus offering 100 % efficiency. However, components are not ideal, and the topology of converters plays an important role in the power loss distribution as it defines the way the switches are operated [30]. For example, for a 2-level three-phase inverter, it is possible to apply eight different

switching states [31] and some of them give the same differential voltages on a star-connected load.

The losses in a device can be mainly classified as switching losses, conduction losses and reverse recovery losses (for diode).

#### ❖ *Switching Losses*

Switching losses reduce the efficiency of power converters, particularly at low power ranges and force the designer to include large cooling devices. Typical switching losses are generated during the turn-on and turn-off transitions due to internal device capacitance, stored charges for bipolar components and stray inductances:

- **Device Capacitance:** It is the internal output capacitance ( $C_{oss}$ ) that comes in parallel with the switch such as IGBT and MOSFET when the switch comes in turning-on state. The energy stored by this capacitance in the off-state is vanished during the turning-on transition.
- **Stray Inductances:** These are inductances that appear effectively in series with the switch. The stored energy by these inductances during the on-state is vanished during the turn-off transition.

In fact, each connection in converters is associated with a parasitic resistance, inductance, and capacitance. These parasitic elements created by the interconnections are also undesirable sources of losses. More details concerning the parasitic elements have been described in [2]. Besides, all these switching energies can be added together and multiplied by the switching frequency to give the total switching losses. The efficiency of a converter decreases with the increase of the switching frequency.

A switching process of an IGBT with several commutation cycles is shown in Fig.1-4 [30]. Both turn-on and turn-off processes dissipate energy  $E$ , which is calculated by integrating the power of  $p(t)$ . The high reverse-recovery current generates a fast current peak during turn-on, while the current peak is lower but longer during turn-off. And this energy increases in steps at each commutation cycles (ON and OFF) [30].

Switching loss is a part of the junction temperature rising in the power semiconductor, forcing the use of cooling devices. One possible approach to reduce switching losses is to enhance the switching process by improving the gate drive circuit [32].

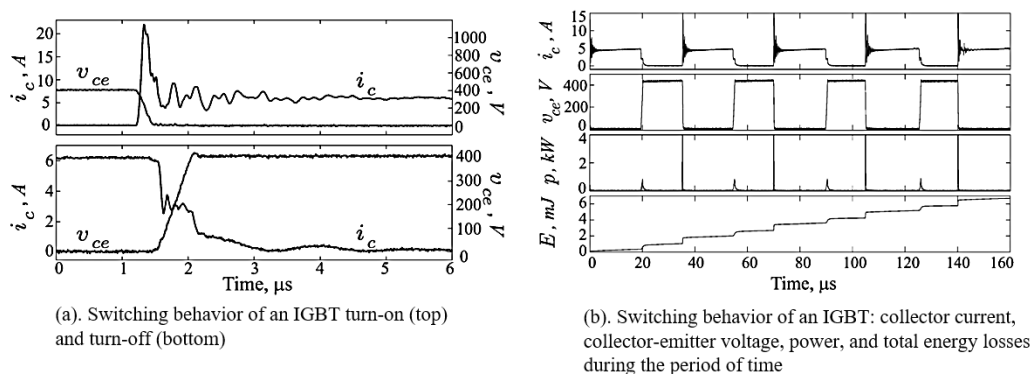


Fig.1-4. Switching process of an IGBT with several commutation cycles [30]

#### ❖ *Conduction Losses*

In contrast to the switching losses during transition period, the conduction losses are the product of the current flowing and the on-state voltage over the conducting period. In Pulse Width Modulation (PWM) applications, the conduction losses must be multiplied by the duty factor to obtain average power dissipation [33]. This means that the conduction losses



are dependent on the duty cycle. In addition, the conduction losses are related to the  $R_{on}$  of the semiconductor (in case of a unipolar device) and conduction losses can be reduced with lower  $R_{on}$  value.

❖ *Reverse Recovery Losses* [33]

A diode allows current to pass in one direction at conduction state, but blocking current in the reverse direction. When turning off the diode, it needs a discharge process to remove the stored charges. So there exists a discharge time known as the reverse recovery time. During this reverse recovery time, the diode current flows in reverse direction. This phenomenon generates an increase of switching losses called recovery losses in the diode.

#### 1.2.2.2. Heat Dissipation Issues

All power sources generate heat due to inefficiency, and all components must dissipate some heat. Thermal cycling can shorten power components lifetime and decrease the mean time to failure, which makes it a long-term reliability consideration of the cooling system.

There are two main heat dissipation issues in a power system [34]:

- **Local cooling requirement:** an individual component (heating source) is overheating due to excess self-dissipation capability.
- **Total system cooling requirement:** the entire system needs a cooling system design to ensure the system reliability to avoid thermal failures caused by thermal cycles.

Thermal paths of a power system are related to the applied components, packaging technologies, as well as the designed cooling devices. Usually a cooling system is designed for the total power system, but special local cooling can help us to remove the heat more fast from the heating source.

### 1.3. POWER PACKAGING

#### 1.3.1. Introduction

Electronic packaging is an important discipline in the field of electronic engineering and it contributes to assemble the power components and cooling systems in order to distribute signal and power, dissipate the heat power, protect the power systems from mechanical damage, and ensure reliable operation environment of the components. Usually, requirements for the power electronics packaging for harsh environment operation are summarized as follows [35-37]:

- **Thermal:** Low thermal resistance from junction to case; high junction temperature operation ability; high thermo-mechanical robustness for large temperature excursion.
- **Electrical:** Small parasitic inductance; symmetric layout; small footprint.
- **Manufacture:** Simple fabrication process; precise interconnection of small pads on the dies.

Generally, electronic packaging could be divided into two big categories as 2D packaging and 3D packaging. In the following part, discussions will be concentrated to the differences between these two packaging technologies, especially in the thermal aspects.

#### 1.3.2. 2D Packaging with Direct Bonded Circuit (DBC) Technology

##### 1.3.2.1. Structures

As shown in Fig.1-5 [10], power electronics interconnection technique realized by wire bondings is usually based on the DBC substrate. The DBC substrate has two copper layers

separated by an insulated ceramic layer, which is preferred for medium to large power packages (from kW to MW). Its role is to provide a plane space dedicated to assembly by soldering process the active electronics components in a 2D package.

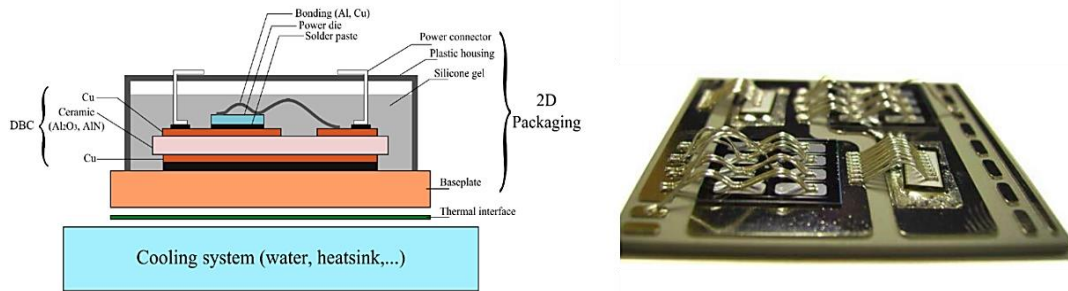


Fig.1-5. Schematic view of a power module and example of 2D packaging inverter arm [10]

### 1.3.2.2. Materials

Available ceramic materials are listed in Table 1.2 [38]. Thermal performances of power systems are related to the material properties of chosen components. For high performance requirements, the Aluminum Nitride (AlN) is preferred for its better thermal conductivity than traditional alumina (Al<sub>2</sub>O<sub>3</sub>). Silicon Nitride (Si<sub>3</sub>N<sub>4</sub>) is an interesting material with a high flexural strength of 932 MPa. That means, it can be used without any baseplate to reduce the total packaging size. The last material of Beryllium oxide (BeO) is usually avoided because of its toxicity when its powder is inhaled [10, 38]. Besides, Coefficient of Thermal Expansion (CTE) is indicative of the extent to which a material expands upon heating and due to CTE mismatch between materials of an assembly, detrimental internal stress or shear stress will be generated in some parts of the structure [39]. These differences of thermal expansion coefficients between materials of components, solders and substrates are usually the reasons of delamination phenomena after certain thermal cycling.

Table 1.2. Ceramic materials used for DBC substrate [38]

Ceramic	Thermal Conductivity (W/m·K)	CTE (ppm/°C)	Flexural Strength (MPa)	Dielectric Strength (kV/mm)	Relative Cost
Al <sub>2</sub> O <sub>3</sub> (96%)	24	6.0	317	12	1
Al <sub>2</sub> O <sub>3</sub> (99%)	33	7.2	345	12	2
AlN	150 to 180	4.6	360	15	4
Si <sub>3</sub> N <sub>4</sub>	70	3.0	932	12	2.5
BeO	270	7.0	250	10	5

### 1.3.2.3. Limiting Points

2D Packaging with wire-bondings has many drawbacks, namely high stray inductances (several nH); non-negligible area; time-consuming to manufacture as all wire bonds have to be placed successively [10, 38]. In addition, this 2D packaging structure has limitations in thermal dissipation because it does not offer the possibility of double-side cooling due to the presence of wire-bondings, which causes such problems as increased interconnect delays, power consumption, and temperatures.

### 1.3.3. 3D Packaging with Printed Circuit Board (PCB) Technology

#### 1.3.3.1. Structures

PCB substrates are primarily used to connect components together for 3D packaging technologies with a variety of interconnect possibilities. Usually, this PCB technology makes use of flexible or rigid PCB substrates. Besides, PCBs are very favorable for use in power conversion products as they make the manufacturing process easier.

Flex PCB substrate is usually used to realize interconnections in order to reduce the interconnect lengths formed by wire bondings. Hence to reduce the switching losses caused by stray inductances.

In addition, PCB technologies may also be used to realize 3D assemblies. Compared to 2D packaging, 3D packaging allow to create higher power density converters by using vertical interconnections and PCB embedding technology with multiple layers rather than spread out over a large surface area. For example, as shown in Fig.1-6, authors in [40] proposed a converter integrating passive components into PCB substrates to form an “embedded Passive Integrated Circuit” (emPIC). And it is demonstrated that 82% efficiency can be achieved of their 3D embedding application.

3D packaging by PCB substrates indicate the trends of power modules development in miniaturization and higher power density. However, one of the biggest challenges in using PCB technology lies in thermal problems. Since heat has further travel to reach ambient because of the additional integration layers, and insulating materials used during fabrication between layers also impedes heat dissipation.

#### 1.3.3.2. Materials

Most available PCB substrates are in material of typical epoxy-based Flame Retardant (FR-4) for its low cost. However, FR-4 possesses significantly poor thermal conductivity ( $<1.5$  W/mK) which contributes to the overall thermal resistance of the PCB structure [41]. Besides, the significant increase of thermal resistance and the resulting temperature gradient may lead to delaminate the interfacial layer material attached to the PCB. But, the dielectric strength of FR-4 PCB substrate is  $54$  kV/mm, which is more than 4 times higher than that of ceramic (from  $10$  to  $15$  kV/mm as shown in Table 1.2). In other words, PCB substrates may be thinner than DBC substrates for the same insulation rating. However, from a thermal point-of-view, this reduction in the thickness of PCB substrates is not sufficient to cover up its worse thermal performances than DBC.



Fig.1-6. Thin 60-W offline converter with PCB integrated transformer and capacitors [40]

#### 1.3.3.3. Limiting Points

PCB technology is attractive to realize 3D integration structures because of its available integration density, flexibility and comparatively low costs. However, higher temperatures caused by higher power densities (usually  $100$  W/cm<sup>2</sup> [42]) and greater thermal resistances in use of the PCB substrates could decrease system performances and generate reliability issues.

In [10, 18], Yu has compared the thermal performances of different GaN prototypes, GaN transistors are mounted on PCB ( $70$   $\mu$ m) and DBC ( $635$   $\mu$ m) substrate for the same dielectric strength. As shown in Fig.1-7 [10], for a dissipated power of  $10$  W in GaN chip, DBC

structures have much better thermal performances than that of PCB because of its higher thermal conductivity with ceramic substrate.

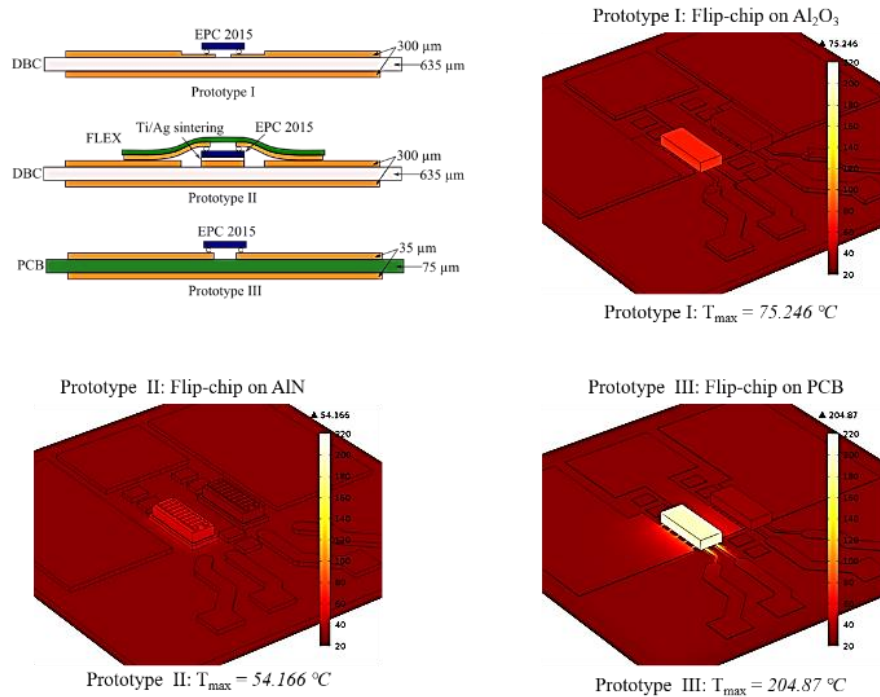


Fig.1-7. Thermal simulation results for different GaN prototypes [10]

#### 1.3.4. Conclusion

The pros and cons of 3D packaging technology and of 2D packaging technology have been discussed in this section based on the realized structures and used materials, especially from a thermal point-of-view. In a word, “*power electronics packaging has been saddled with five key complaints with the advent of WBG components: packages have too much electrical resistance; they have too much stray inductance; they take up too much space and they have poor thermal properties*” [43]. All these weak points will turn into unexpected power losses and finally the problems of heat dissipation.

In order to take advantages of the benefits of 3D integration and of WBG devices, thermal problems of PCB substrates must be firstly overcome and suitable cooling solutions should be found.

## 1.4. THERMAL ANALYSIS OF POWER ELECTRONICS SYSTEMS

### 1.4.1. Introduction

Higher voltage, higher current levels and higher operating frequencies induce higher thermal losses in power electronics [44] and the continued miniaturization trend leads to growing high power densities. In other words, this induces higher dissipation heat flux densities and, subsequently, higher device operating temperatures. Consequently, thermal modeling and management of power electronics systems are nowadays one of the most important research areas since a vast majority of system malfunctions or failures are due to thermal reasons.

Heat transfer may take place by one or more of three modes: thermal conduction, thermal convection, and thermal radiation.

#### ❖ Thermal Conduction (Heat Diffusion)

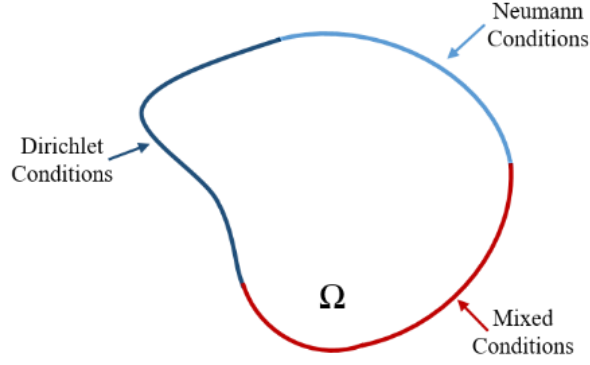


Fig.1-8. Bounded spatial thermal region

In a bounded spatial region  $\Omega$  for multi-port dynamic thermal networks, the relation between the power density  $P(\mathbf{r}, t)$  and the temperature rise  $T(\mathbf{r}, t)$  with respect to ambient temperature, functions of the position vector  $\mathbf{r}$  and of the time instant  $t$ , is ruled by the heat conduction equation [45, 46]:

$$\nabla \cdot (-k(\mathbf{r})\nabla T(\mathbf{r}, t)) + c(\mathbf{r})\frac{\partial T}{\partial t}(\mathbf{r}, t) = P(\mathbf{r}, t) \quad (1.4-1)$$

Where  $c(\mathbf{r})$  is the volumetric heat capacity and  $k(\mathbf{r})$  is the thermal conductivity Eq (1.4-1) is completed by conditions on the boundary of  $\Omega$ ,  $\partial\Omega$ , and by initial condition for the temperature rise  $u(\mathbf{r}, t)$ . The boundary conditions, assumed of Robin's type, are:

$$-k(\mathbf{r})\frac{\partial T}{\partial v}(\mathbf{r}, t) = h(\mathbf{r})u(\mathbf{r}, t) \quad (1.4-2)$$

In which  $h(\mathbf{r})$  is the heat transfer coefficient and  $v(\mathbf{r})$  is the outward unit vector normal to  $\partial\Omega$ . Here  $h(\mathbf{r})$  is not assumed to be identically zero over  $\partial\Omega$ , that is pure Neumann's boundary conditions are excluded. The initial condition is assumed to be zero.

$$T(\mathbf{r}, 0) = 0 \quad (1.4-3)$$

At steady state, heat conduction within a chip can be described by the following differential equation:

$$k_x\frac{\partial^2 T}{\partial x^2} + k_y\frac{\partial^2 T}{\partial y^2} + k_z\frac{\partial^2 T}{\partial z^2} + P(x, y, z) = 0 \quad (1.4-4)$$

Where  $k_x, k_y, k_z$  are the thermal conductivities, and  $P$  is the heat generated per unit volume. Unique solution exists when convective, isothermal, and insulating boundary conditions are appropriately applied, and the nature of the packaging and heat sink determines these boundary conditions.

Solutions of Eqs (1.4-1)(1.4-2)(1.4-3) could be expressed as Eq (1.4-5) by the Laplace transform [45]:

$$T(s) = Z_{th}(s)P(s) \quad (1.4-5)$$

In which  $Z_{th}(s)$  is the thermal impedance matrix of the multi-port dynamic thermal networks. By analogy with electrical solutions, dynamic thermal networks have canonical representations of passive lumped RC (resistor-capacitor) networks [46, 47]. In particular, Foster canonical form is equivalent to the time-constant representation and the generalized Cauer canonical form is a passive multi-conductor RC transmission line.

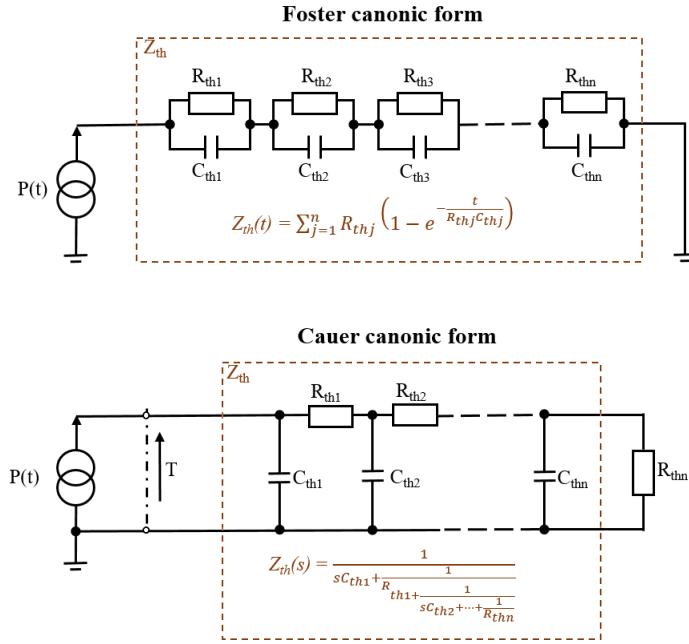


Fig.1-9. The Foster (top) and Cauer (bottom) canonic forms of thermal networks

Thermal component models are shown in Fig.1-9, Foster canonic form is represented by series connection of multiple elements of parallel resistance  $R_{thj}$  and capacitance  $C_{thj}$ . To represent the physical structure of the thermal system, it has been converted into Cauer canonic form [44]. And in the Cauer form, one pair of thermal impedance  $R_{thj}$  and  $C_{thj}$  represent one element of the thermal stack from chip to ambient. An example of Cauer canonic form is shown in Fig.1-10. In this figure, calculation of Cauer form elements are done with Matlab for a simple power die assembly and compared to 3D FE simulations [53].

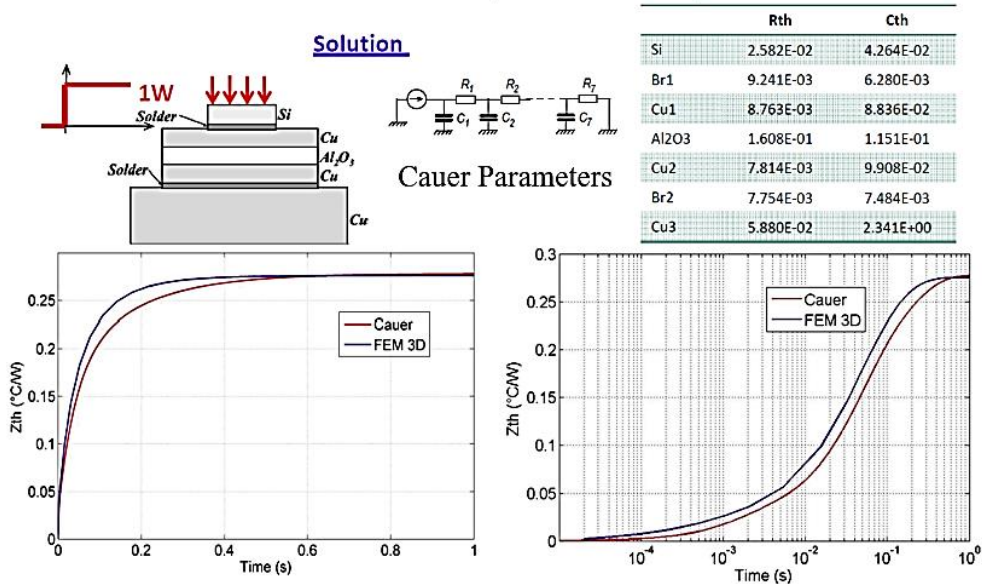


Fig.1-10. Calculation results for Si structures by Cauer modeling [48]

Foster and Cauer canonic forms are common representations of thermal networks by equivalent RC circuits. They are usually used in dynamic analysis of power systems to simulate their thermal behaviors. For example, two abstraction layers that are synthesized as PSpice netlists have been designed to represent respectively the electrical and thermal behaviors as shown in Fig.1-11. This approach allows reducing a multi-physic electrical-thermal problem to a single-domain electro-thermal one [54].

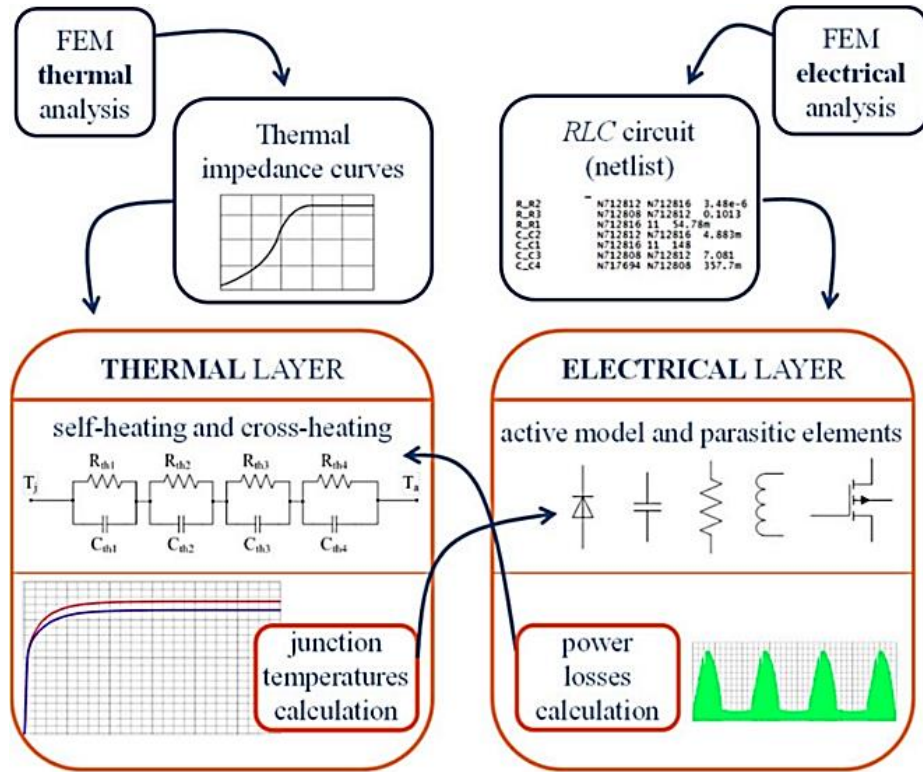


Fig.1-11. Layered approach adopted for the electro-thermal modeling of integrated power electronics modules [49]

❖ Thermal Convection

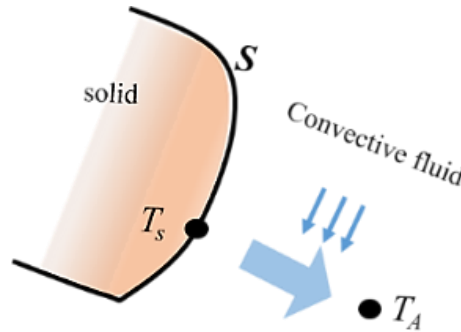


Fig.1-12. Heat convection

Physical mechanism of convection is related to the heat conduction through the thin layer of fluid adjacent to the heat-transfer surface. When a fluid (air or liquid) is heated and then moves away from the heat source, it carries the thermal energy away as shown in Fig.1-12. This type of heat transfer is called convection. The fluid above a hot surface expands, becomes less dense, and rises. The equation for convection rates is calculated as follows:

$$Q_{con} = h_c A (T_s - T_A) \quad (1.4-6)$$

Where  $Q_{con}$  is the heat transferred per unit time;  $h_c$  is the convective heat transfer coefficient;  $A$  is the heat transfer area of the surface;  $T_s$  is the temperature of the surface; and  $T_A$  is the temperature of the fluid.

❖ Thermal Radiation

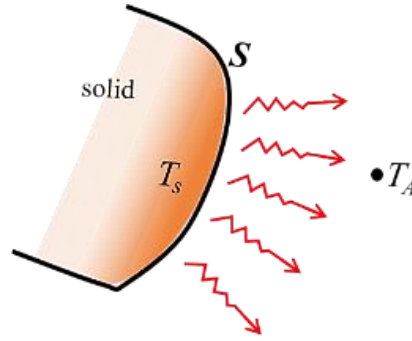


Fig.1-13. Heat radiation

“Fourier’s law is applicable for both conduction and convection, although fluid mechanics must be brought into play in the convection problem in order to establish the temperature gradient. But radiation heat transfer involves a different physical mechanism: electromagnetic radiation-propagation of electromagnetic energy” [50].

“Thermodynamic considerations show that an ideal thermal radiator, or blackbody, will emit energy at a rate proportional to the fourth power of the absolute temperature of the body and directly proportional to its surface area” [50]. Heat radiation relationship called the Stefan-Boltzmann law is described in Eq (1.4-7).

$$Q_{\text{rad}} = \varepsilon S \sigma (T_s^4 - T_A^4) \quad (1.4-7)$$

Where  $\varepsilon$  ( $0 < \varepsilon < 1$ ) is emissivity,  $S$  is heat radiation area of the surface,  $\sigma$  is Stefan-Boltzmann constant with the value of  $5.669 \times 10^{-8} \text{ W}/(\text{m}^2 \cdot \text{K}^4)$ .

For example, in [51], authors investigate a new thermal technique that controls thermal radiation spectrum using 2-D periodic microstructure. It suggests that thermal radiation is effective for thermal management of electronic devices in small spaces.

#### 1.4.2. Thermal Measurement Methods

Driven by recent advances toward integration, high densities, and high operating frequencies in power electronics systems, accurate estimates of junction temperature and power losses have become more important for proper thermal management and ensuring reliable operation. Because “Power wall” is a critical performance limitation or thermal limits of integrated circuit, especially for the PCB substrates with poor power thermal conductivity of FR4 material ( $< 1.5 \text{ W}/\text{m}^2 \cdot \text{K}$ ) and excessive power dissipation of GaN chip will reduce its life time [52]. An overview of temperature and power losses measurement methods will be presented in the following part.

##### 1.4.2.1. Temperature Measurement

Temperature variations in power components cause a considerable change in power loss dissipation. Thermal properties and temperature dependency of semiconductor parameters are well-known phenomena. If the temperature exceeds the materials' melting temperature, the package would fail or even blast. Moreover, due to the significant mismatch of coefficient of thermal expansion (CTE) between the bond wire, die, die attach solder and lead frame, the high temperature gradient would induce high thermal strain, and stress, which would lead to cracks and delamination, which may also lead to final failure. Therefore, it is important to investigate the thermal performance of high power electronic package and thus find an effective solution to enhance the thermal dissipation ability, thus improving its reliability. Temperature evolution of component could lead to a better control and utilization of the component. Temperature measurement methods may be discussed by divided into direct and indirect methods.



❖ *Direct Methods*

There are mainly three direct methods for temperature measurement:

1) Infrared camera

The most common direct method based on Eq (1.4-7) is to measure the surface radiation of the component chip and calibrate it with the temperature, i.e. by using the infrared camera. Besides, a sophisticated acquisition and exploitation software is coupled with the infrared microscope to minimize measurement errors.

There are several factors which complicate the measurement of surface temperature of objects from the intensity of their emitted infrared radiation. As mentioned previously, the intensity of emitted radiation is dependent upon the nature of the surface of the emitting material. And a perfect radiation emitter is known as a black body. Advantages of using infrared camera include that they can have very high spatial resolution, can often measure rapid variations in temperature, and are non-contacting. Besides, detailed surface temperature distribution is possible without technical difficulties. To collect similar information, using arrays of thermocouples or thermistors should be used.

2) Thermocouple

Thermocouple is a widely used type of temperature sensor. A thermocouple is consisted of two dissimilar electrical conductors that can measure temperatures in a wide range of temperatures (-250 °C to 2,000 °C) [53]. In contrast to most other methods of temperature measurement, thermocouples are self powered and require no external form of excitation. The main limitation is that the measurement errors of less than 1 °C can be difficult to achieve [54].

3) Resistance Temperature Detectors (RTDs)

RTDs, also called Resistance thermometers, are used to measure temperature. Most RTD elements have a length of fine wire wrapped around a ceramic or glass core. The RTD wire is usually created by a pure material such as platinum, nickel, or copper. Besides, principle of temperature indication is based on the accurate resistance/temperature relationship of the used material. Platinum is the best metal for RTDs due to its very linear and stable resistance-temperature relationship, highly repeatable over a wide temperature range [55].

The important feature of the direct method is that it gives the spatial temperature distribution of the component chip instead of only the averaged value obtained by the indirect method.

❖ *Indirect Methods (Electrical Methods)*

Because that many electrical properties of semiconductor devices can vary with the temperature, principal of the indirect methods is to calibrate the variation of a temperature sensitive parameter of the component with temperature variations. These time-dependent Temperature-Sensitive Parameters (TSP) are presented as follows [56, 57]:

- 1) On-state voltage drop
- 2) Off-state leakage (direct or reverse) current
- 3) Direct or reverse avalanche voltage
- 4) Threshold voltage of their gate controlled devices.

The first step in using these parameters as a temperature indicator is to calibrate them with known temperatures and derive a calibration curve for the specified component. In

order to measure small variation of these parameters with temperature, measurement devices should be very precise.

#### 1.4.2.2. Power Loss Measurement

It is self-evident that we need a quantitative knowledge of power loss in any power electronics system. Power loss measurement with high accuracy is important to assess system performance and optimize the characteristics of the designed systems [58].

Commonly used methods to measure power losses are sophisticated modeling, electrical methods and calorimetric methods. Their pros and cons concerning various techniques will be discussed in the following part.

#### ❖ *Sophisticated Modeling*

Thermal component models are parameterized in terms of structural and material properties so they can be readily used to develop a library of component models for any available power module.

##### 1) Numerical 3-Dimension (3-D) modeling

Common numerical methods for thermal analysis are 3-D Finite Element Methods (FEM) and 3-D Finite Difference Methods (FDM) by 3D simulations in use of softwares such as ANSYS [59], SOLIDES-ise [60], SALOME [61], COMSOL Multiphysics [62], FloTHERM [63] etc. There are a lot of research work depending on FEM or FDM simulations to calculate the 3D thermal behaviors in power modules as in [64, 65].

For example, in [66], a simplified boundary-dependent thermal model for high power insulated-bipolar transistor IGBT modules has been developed as presented in Fig.1-14. The simulation conditions applied by the authors are heat sources (power losses) and the heatsink (cooling system). Thermal distributions are acquired in critical points and the 3D FEM simulation results could be used for accurate life-time estimation of the used IGBT module.

However, 3-D FEM or FDM simulations has limitation due to computation time in arbitrary load cycles and computer memory for fine meshes. Moreover, it may also lead to divergence in case of very high dynamic operations.

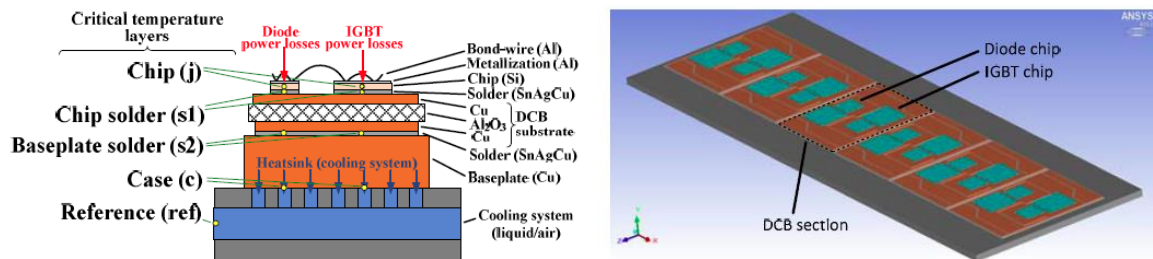


Fig.1-14. Schematic of high power IGBT module modeled in ANSYS Icepak for FEM analysis [66]

##### 2) Analytical 2-Dimension (2-D) modeling: Electro-thermal analysis

The most widely used method for thermal behavioral modeling of power modules involves curve fitting RC cell networks from data sheet or from 3-D FEM solvers to provide thermal transient curves [67]. This kind of electro-thermal model is usually a full analytical Fourier series-based model as previously described in part I.4.1 for heat conduction analysis with Foster or Cauer canonic forms. Traditional softwares for electro-thermal modeling and simulations are Saber [68], PSpice [69], Matlab [70], T3Ster Master Software tool [71], etc.

In these cases, additional synthesis step is required from measurement or numerical 3-D FEM analysis. For example, the extracted thermal part of the total system is coupled with an electronic system part in the circuit simulator Saber as shown in Fig.1-15 [72]. Based on the

numerical results, the temperatures at defined positions of the 3-D FEM result are used to generate a set of RC components for the thermal network. This thermal network is inserted and implemented into the circuit simulator to analyze the electro-thermal behavior of power electronics systems, simultaneously. The RC circuits can quickly offer an insight into the physical layers of the components and provides useful information in a few minutes for arbitrary or periodic power waveforms.

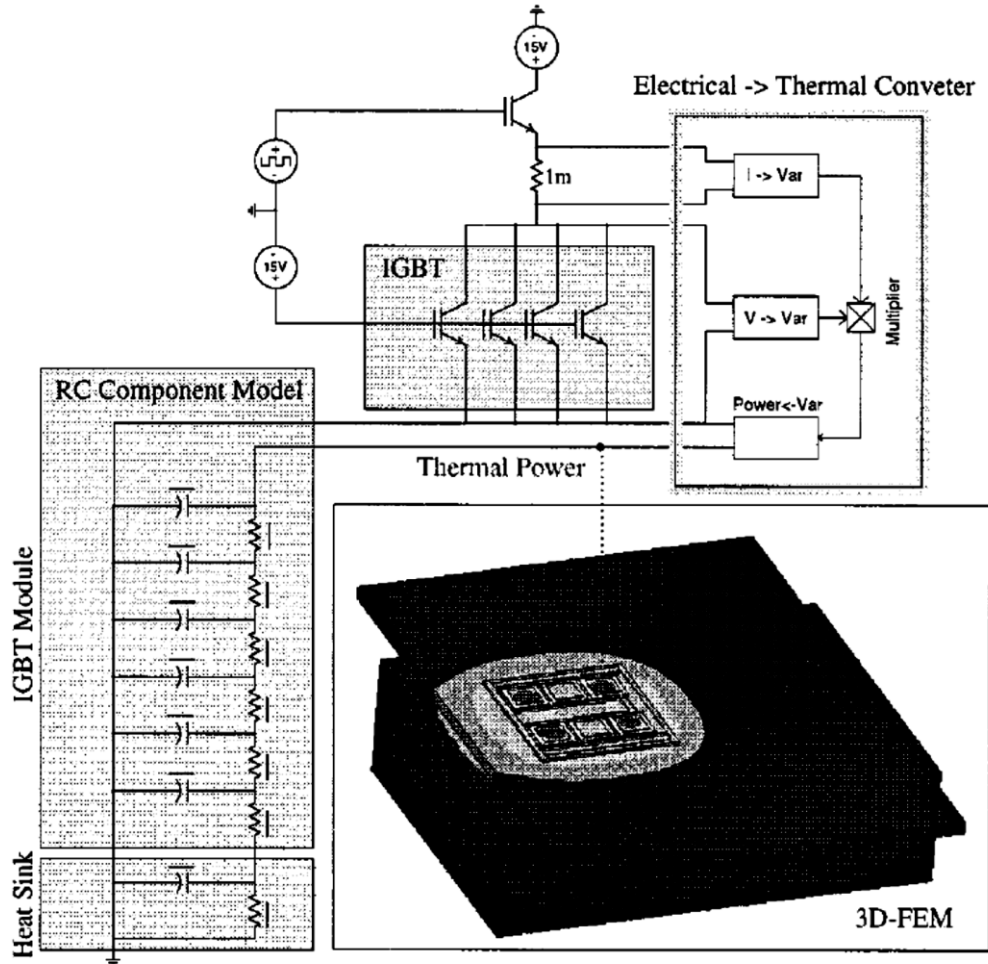


Fig.1-15. Electro-thermal model in Saber [72]

### 3) Mathematical calculations: Functions to estimate power losses

Since the insulated-bipolar transistor (IGBT) is the most widely used power transistor in the medium and high-voltage range [73], most models in literature focus only on the IGBT. But with little modifications, these models can be made suitable to other devices as well.

Different loss-calculation models in literatures are summarized in Table 1.3, which have been reviewed by authors in [74]. According to these listed literatures, power losses could be estimated as functions of one or more of the following parameters: device currents  $I_c$ , DC-link voltages  $V_{dc}$ , junction temperatures  $T_j$ , gate-resistance  $R_g$ , the gate-voltage  $V_g$ , the IGBT chip area  $S_I$  and diode chip area  $S_D$  etc. The coefficients  $A-K$ ,  $A_{11}-D_{43}$  are obtained by fitting calculated curves to measured values of  $V_{ce}$  or  $P$  function of  $I_c$ . So, these models need step-by-step procedure to experimentally determine the model coefficients. Usually these equation models are used to simulate the losses for automotive inverter applications and give about 15% error over a wide operating range for standard models making it unsuitable for efficiency calculations [74]. More accurate models need to be developed in the next future.

Table 1.3. Different loss-calculation models concerning IGBT devices in literatures [74]

Literatures	Voltage: $V_{ce}$ (V)	Losses: $P$ (W)
1989 [75]	$V_{ce} = V_{ce0} + R_c \cdot I_c$	$P = P_{nom} \frac{I_c}{I_{cnom}} \frac{V_{dc}}{V_{dcnom}}$
1991 [76]		
1994 [77]		
1995 [78]	$V_{ce} = V_{ce0} + R_c \cdot I_c^K$	$P = P_{nom} \left( \frac{I_c}{I_{cnom}} \right)^A$
1996 [79]	$V_{ce} = (V_{ce0} + A \cdot T_j) + (R_c + B \cdot T_j) \cdot I_c^K$	$P = P_{nom} \left( \frac{I_c}{I_{cnom}} \right)^A \left( \frac{V_{dc}}{V_{dcnom}} \right)^B \left( \frac{T_j}{T_{jnom}} \right)^C$
2004 [80]	$V_{ce} = V_{ce0} + R_c \cdot I_c$	$P = P_{nom} \frac{I_c}{I_{cnom}} \frac{V_{dc}}{V_{dcnom}}$
2005 [81]		$P = P_{nom} (A \cdot I_c^2 + B \cdot I_c + C) \frac{V_{dc}}{V_{dcnom}}$
2013 [82]		$P = P_{nom} \frac{I_c}{I_{cnom}} \left( \frac{V_{dc}}{V_{dcnom}} \right)^K$
Infineon [74]	$V_{ce} = (V_{ce0} + A \cdot T_j + B) + (R_c + C \cdot T_j + D) \cdot I_c$	$P = P_{nom} \left( \frac{I_c}{I_{cnom}} \frac{V_{dc}}{V_{dcnom}} \right) \cdot (E \cdot T_j + F)^G$
ABB [83]	$V_{ce} = V_{ce0} + R_c \cdot I_c$	$P = P_{nom} (A \cdot I_c^2 + B \cdot I_c + C) \frac{V_{dc}}{V_{dcnom}} \cdot (D \cdot T_j + F)^G$
Semikron [84]	$V_{ce} = (V_{ce0} + A \cdot T_j + B) + (R_c + C \cdot T_j + D) \cdot I_c$	$P = P_{nom} \left( \frac{I_c}{I_{cnom}} \right)^A \left( \frac{V_{dc}}{V_{dcnom}} \right)^B (C \cdot T_j + D)^K$
2016 [74]	$V_{ce} = V_{ce0} + R_c \cdot I_c$	$P = (A_{11} \cdot I_c^2 + A_{12} \cdot I_c + A_{13})(B_{21} \cdot T_j^2 + B_{22} \cdot T_j + B_{23})(C_{31} \cdot V_{dc}^2 + C_{32} \cdot V_{dc} + C_{33})(D_{41} \cdot S_D^2 + D_{42} \cdot S_D + D_{43})$

Generally, sophisticated numerical modeling methods are often available and efficient to predict power losses, but validity of the models need to be verified experimentally.

#### ❖ Electrical Methods

This method is applicable to steady state as well as transient conditions. It is common to determine power losses through conventional input-output procedure by taking the difference between the measured input and output power in use of electronic equipments: voltmeters for voltage measurements and ammeters for current measurements, or a combined measurement using a wattmeter, especially in DC and low frequency AC circuits [58]. For example, a test platform for the electrical input-output based method described as Fig.1-16 [85] is built. The inverter is connected to a 3-phase inductive load. The power analyzer measures the input DC power  $P_{in}$  and the output AC power  $P_{out}$ , and the difference is equal to the power loss  $P_{loss}$ , from the basic definition  $P_{loss} = P_{in} - P_{out}$ .

However for high frequency systems, conventional meters are no longer suitable because of their limited bandwidth and dynamic frequency response [86]. So, the second common electrical method to estimate losses digitally is based on the high frequency sampling of voltage and current waveforms. For periodical power signals with a period of  $T$ , the instantaneous average power  $P_a$  can be calculated by Eq (1.4-8) [58]:

$$P_a = \frac{1}{T} \int_0^T v(t) \cdot i(t) dt \quad (1.4-8)$$

Where voltage  $v(t)$  and current  $i(t)$  waveforms are simultaneously sample at a sampling rate  $f_s = 1/T_s$ , and converted to digital values. If  $v(t_i)$  and  $i(t_i)$  are the instantaneous samples

of the voltage and current at time  $t_i = i \cdot T/N$ , then the average power  $P_a$  can be approximated by Eq (1.4-9)[58]:

$$P_a = \frac{1}{N} \sum_{n=0}^{N-1} v(t_i) \cdot i(t_i) \quad (1.4-9)$$

Power losses in power switching devices are mainly the combination of the conducting and switching losses. As mentioned previously, conducting losses are the dissipation that occurs while the semiconductor is in the on-state and conducting current. Switching losses are the power dissipation during turn-on ( $E_{on}$ ) and turn-off ( $E_{off}$ ) switching transitions. The conduction losses are computed by multiplying the on-state saturation voltage by the on-state current. In case of high-frequency switching (>100 kHz) systems, switching losses are unneglectable [87] and the switching energy losses have to be calculated by integrating the instantaneous dissipated power.

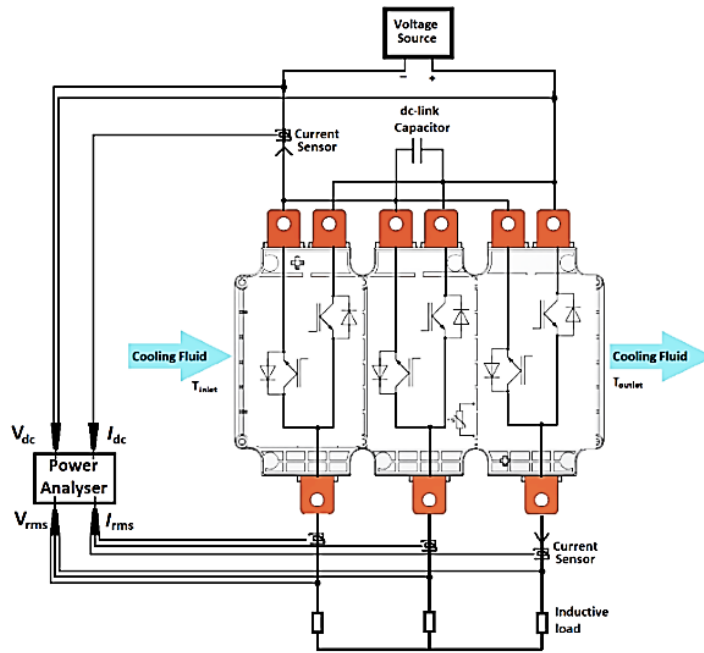


Fig.1-16. Schematic for measurement of power losses with the electrical method [85]

The well-known double pulse test (DPT) method allows to determine switching losses at different junction temperature by controlling case temperature of the device under test (DUT). It could limit self heating effects by the use a “double pulse” [88] that produces very short test pulses ( $<8 \mu s$ ) and does not heat up the DUT. As shown in Fig.1-17, the turn-off waveform can be recorded after the first pulse. And the turn-on waveform can also be recorded until the transistor is turned on again [87].

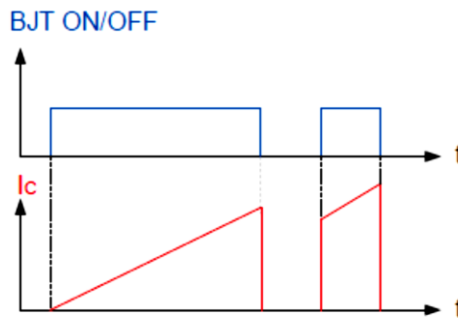


Fig.1-17. Double pulse waveform [87]

An example of DPT result is shown in Fig.1-18 [89]. Switching loss equals to the addition of turn-on energy  $E_{on}$  and turn-off energy  $E_{off}$ . The total dissipated power is obtained by adding conducting losses and switching losses.

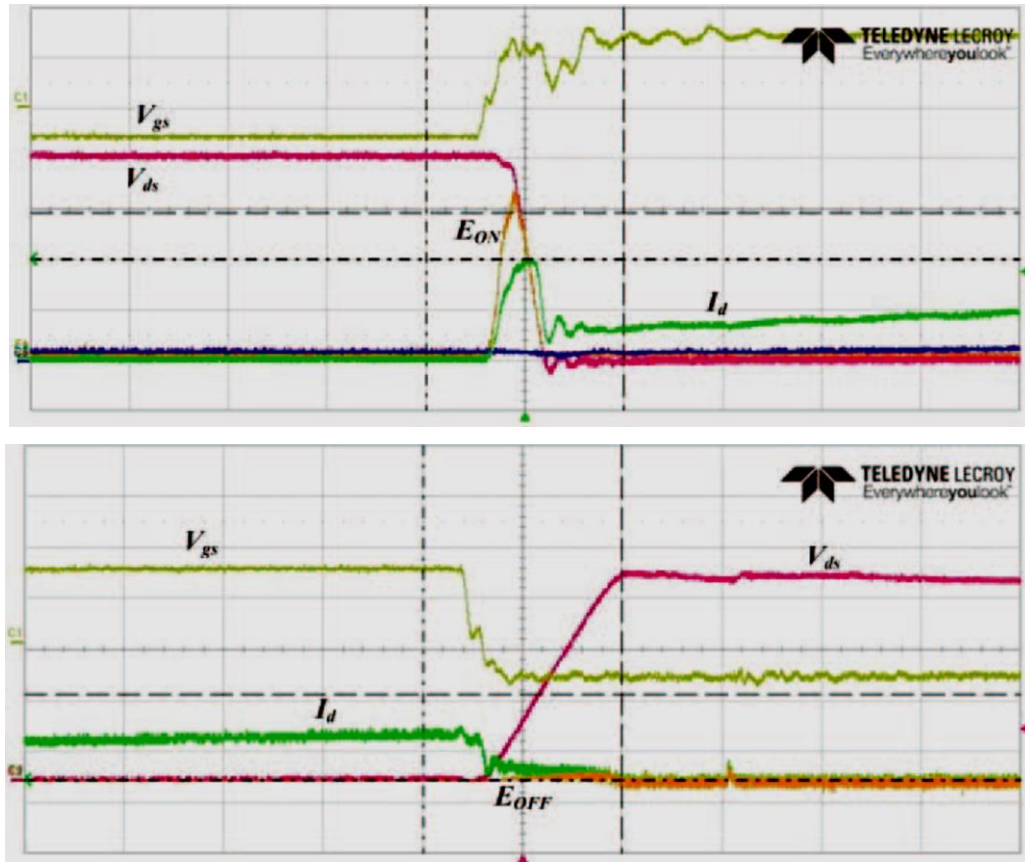


Fig.1-18. SiC MOSFET switch on and switch off transient [89]

However, the accuracy of digital measurement is affected by the delays introduced between probes, phase shifts between sampling channels of digitizer, sampling errors and non-linearity of A/D converter. Firstly, different propagation delays due to the different construction of voltage and current probes are noticeable for MHz signals [90]. Secondly, the bandwidth and rise time of oscilloscope/probe system also affects measurement accuracy [91]. Moreover, the radio frequency interferences (RFI) and electromagnetic interferences (EMI) emanating from the high  $di/dt$  and  $dv/dt$  are prevailed in hard switching power converters [58]. A common solution to this problem is to add a sine output filter, which produces additional measurement errors. When  $dv/dt$  is very high, no instrument can today accurately record the waveforms of the hard-switched output voltage [92]. Despite accuracy compromise, electrical method is still a preferred method for measuring losses in power electronics because of its simplicity.

By the way, in order to further increase power densities within multichip power modules containing single-phase and three-phase inverter bridges, soft switching techniques are required along with dense packaging. Technique such as turning on a device under zero voltage switching (ZVS) allows the reduction or elimination of switching loss.

#### ❖ *Calorimetric Methods*

Calorimetric methods allow to measure with high accuracy the power losses under normal operating conditions and this method is independent of voltage and current waveforms of the device under test (DUT). This method based on direct loss measurement is applicable to steady state conditions. Since the power losses are dissipated as heat, the effect caused by

the heat could be measured to determine the losses [85]. It has been widely used in power electronics to measure power losses of magnetic components [93-97], capacitors [98], switching semiconductors [99], power converters [100] and electrical machines [101-106].

Adiabatic walls are needed for an ideal calorimetric measurement system to ensure that the total power loss from the DUT can be detected by the increase of temperature inside the measurement chamber [107]. “Power dissipation  $P_{loss}$  of the DUT is then determined as a function of the temperature rise  $\Delta T$  between the inlet ( $T_{in}$ ) and the outlet ( $T_{out}$ ) fluid medium temperature, the mass density  $\rho$  and the flow rate  $\dot{v}$  of the coolant as described in Eq (1.4-10):

$$P_{loss} = c_p \cdot \rho \cdot \dot{v} \cdot \Delta T \quad (1.4-10)$$

where  $c_p$  is the specific heat capacity of the fluid” [108].

There are mainly three basic calorimeters as following [85, 108, 109]:

- 1) Open-type calorimeter
- 2) Closed-type calorimeter: single-cased and double-cased
- 3) Calorimeter based on heat flux sensor

The common used fluid is surrounding air or water, for ‘open’ calorimeter or ‘closed’ calorimeter, which are sorted by authors in [108] as shown in Fig.1-19. The difference is that the open type exchanges heat directly with the surrounding air, whereas a heat exchanger is employed for the closed type. Water is usually chosen as coolant for the closed system. Heat leakage through the walls  $P_{wall}$  is the major error source of all calorimeter types. The closed-type calorimeter has proved to be far more accurate than the open one [107]. For example, the double-cased closed type calorimeter can improve the measurement accuracy of the calorimeter system by minimizing  $P_{wall}$  through an active control of the air temperature in the  $T_{gap}$ .

Comparisons between their accuracies shown in Fig.1-20 are summarized by authors in [108]. They indicated that “the open type calorimeters are used for high power measurements of several hundred watts, the closed type calorimeters are used for lower power measurements”. For example, power calorimeters have an accuracy better than 0.4 W with a measurement range lower than 50 W [110, 111]; In [112], authors designed a calorimeter which is capable of measuring power losses of several mW with an accuracy of  $\pm 1.3$  mW at losses of 24 mW. According to [113], the combined (calorimeter and dc power measurement) standard uncertainties for the calorimeter is about  $\pm 0.7$  % with a confidence level of 95 % for power between 2 and 7 kW. Other calorimeters with high accuracy have been contributed by authors in [105, 114, 115] for power losses of 500 W.

For example, the dielectric fluid FC-40 coolant is chosen by authors in [96] for the closed cooling system as presented in Fig.1-21. A delta-T thermocouple pile is used in this system for measuring the temperature difference, and a flowmeter is used for measuring the liquid-flow rate. It’s important to maintain a constant flow rate through the chamber, to minimize the heat leakage through the walls of the chamber, and to control the temperature of the FC-40 fluid in the reservoir [96].

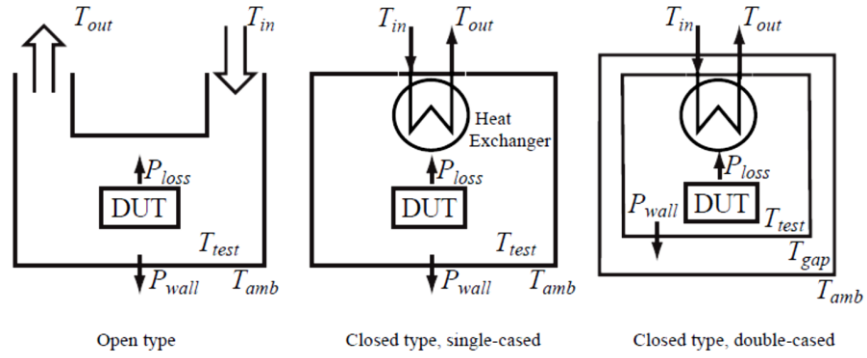


Fig.1-19. Schematic open, single-cased closed and double cased closed type [108]

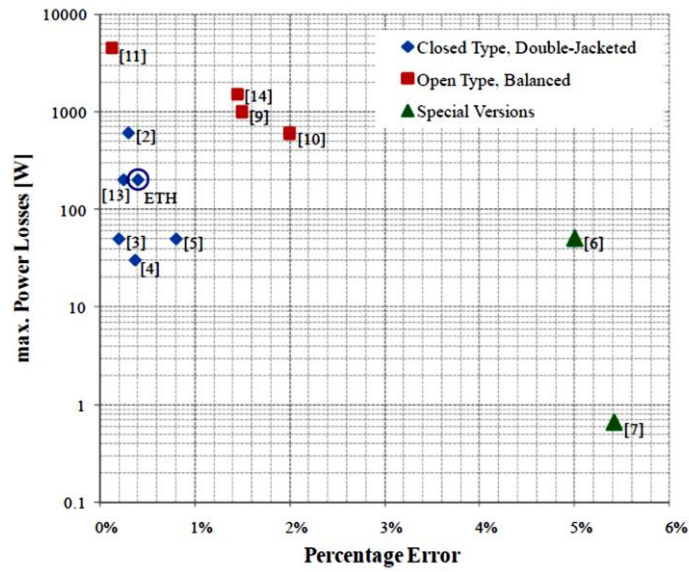


Fig.1-20. Overview of different implemented calorimeters and their reached accuracy [108]

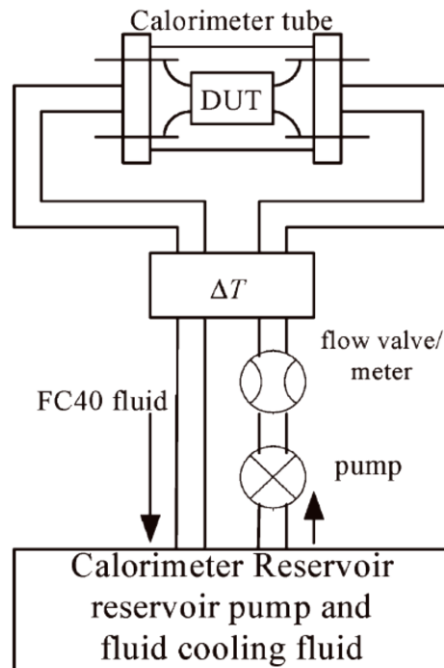


Fig.1-21. Block diagram of calorimeter [96]



The “dry” calorimeter based on heat flux sensors is an effective and simple construction. Fewer accessories are required as compared to the other calorimeters, and the testing time can be reduced because of small time constants. As shown in Fig.1-22 [116], a schematic of proposed apparatus with aluminum pedestal has been designed. Heat passing through the sensors  $P_{loss}$  will generate temperature difference  $\Delta T$  between them, which could be measured by these two sensors. The temperature difference  $\Delta T$  is proportional to the heat flux through the sensor and is converted to a resistance difference signal. A-class PT100 temperature sensors (Platinum resistance thermometer) with four-wire compensation circuits are applied to measure the temperatures. According to Eq (1.4-11), power losses may be calculated.

$$P_{loss} = \frac{\Delta T}{R_{th}}, R_{th} = \frac{e}{\lambda_{th} \cdot S} \quad (1.4-11)$$

Where  $R_{th}$  corresponds to the thermal resistance of the aluminum column between two sensors;  $e$  corresponds to the length between the two positions of the sensors;  $\lambda_{th}$  is the thermal conductivity of the aluminum material;  $S$  corresponds to the cross-section of the aluminum pedestal.

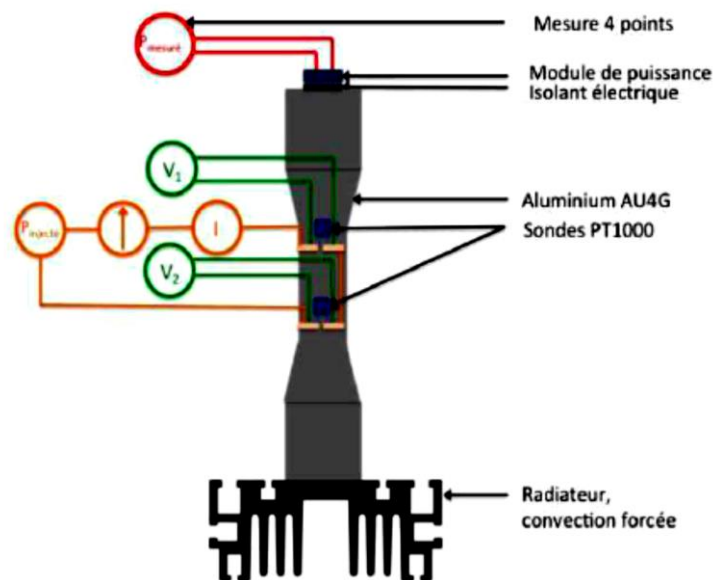


Fig.1-22. Schematic of calorimetric method with heat-flux sensors PT100 [116]

In summary, the open-type calorimeter uses air as a coolant to avoid the risk of leaking fluids. In other words, its cooling system is natural and simple. However, the air properties as density and specific heat are easily affected by ambient temperature, pressure and humidity. Air as coolant is also more prone to uneven temperature distributions inside the chamber. These problems are addressed in [104].

The closed-type calorimeter may be used for a direct calorimetric measurement or a balance test with better accuracy than that of the open-type calorimeters. Since the density and specific heat of coolants as water or another fluid are much higher and less environment dependent than those of air. But the need for a liquid coolant and a heat exchanger make this system complex and expensive. The calorimetric method based on heat-flux sensor is easier to implement and operate without liquid bath or liquid flow system, and the thermal time constants are significantly shorter [93].

A calorimeter combining the advantages of double-jacked closed-type calorimeter and calorimeter based on heat flux sensor is presented in Fig.1-23 [111]. The DUT is placed

inside the internal enclosure of the double-jacked calorimeter. The temperature difference between two polished covers is controlled to minimize the heat escaping through the two covers. A heat flux sensor placed under the conductive pedestal measures the total heat generated in the DUT. A pair of thermoelectric (TE) modules are introduced and used to keep the plate II at constant temperature. The heat generated in the DUT flows down through a heat flux sensor. The heater, the TE modules, and the heat flux sensor together replace the liquid cooling system necessary in other types of calorimeter. This proposed calorimeter is easy to setup and operate, and less than 5 % error in 50 W loss measurements can be achieved [111].

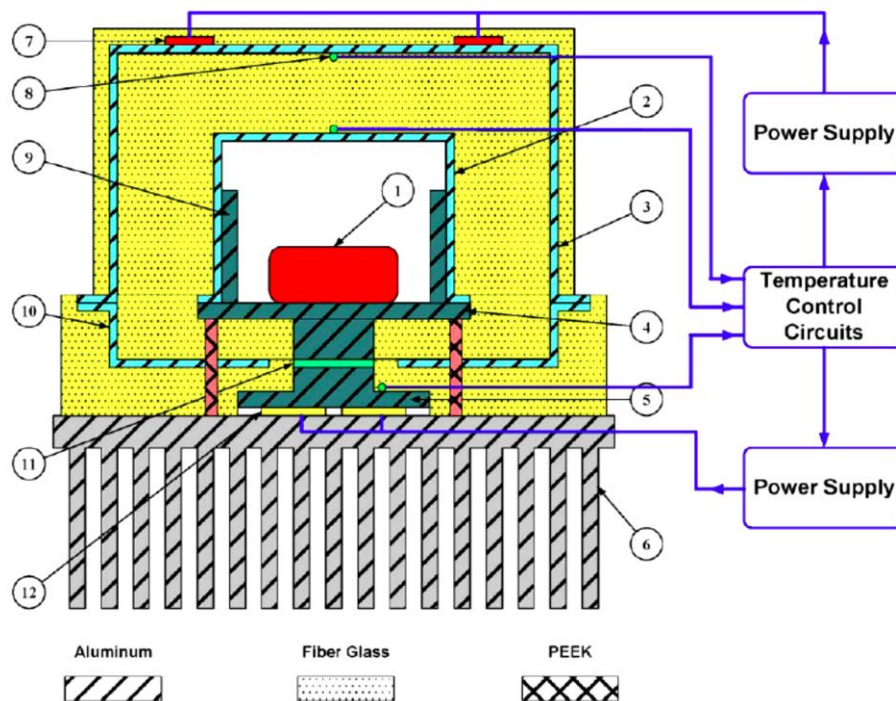


Fig.1-23. Schematic of proposed apparatus.1: DUT; 2: Inner Al cover; 3: Outer Al cover; 4: Al base plate I; 5: Al base plate II; 6: Heat sink; 7: Heater; 8: Thermocouple; 9: Fins; 10: Insulated material; 11: Heat flux sensor; 12: TE module.[111]

Thermal analysis can be regarded as a fundamental step to design the power conversion systems. Along with the thermal analysis, thermal management of power electronics systems and cooling solutions are the next requirement.

#### 1.4.3. Thermal Management Solutions

As mentioned previously, with the increase of power densities and harsh operating environments, thermal management becomes more and more a central issue in power electronics. For example, “the heat flux of power electronic device for hybrid electric vehicles is currently at the level of 100-200 W/cm<sup>2</sup> and is projected to increase up to 500 W/cm<sup>2</sup> in next generation vehicles” [117]. This kind of high heat fluxes will bring us higher but less uniform junction temperature of the chip, which is a critical issue of degrading the performance and reliability of power systems.

So as shown in Fig.1-24 [118], the objective of thermal management is to control the junction temperature of power components to avoid thermal fatigue, short lifetime and irreversible destruction. The main efforts have to be focused on minimizing overall thermal resistance of the power electronics systems. Most cooling technologies rely on heat spreading and convection.

Here in this part, conventional concepts as air cooling, liquid cooling, as well as cooling by thermal vias are reviewed and recent concepts as thermoelectric cooling and hybrid cooling by Peltier modules are described. Their advantages and disadvantages will be given and compared.

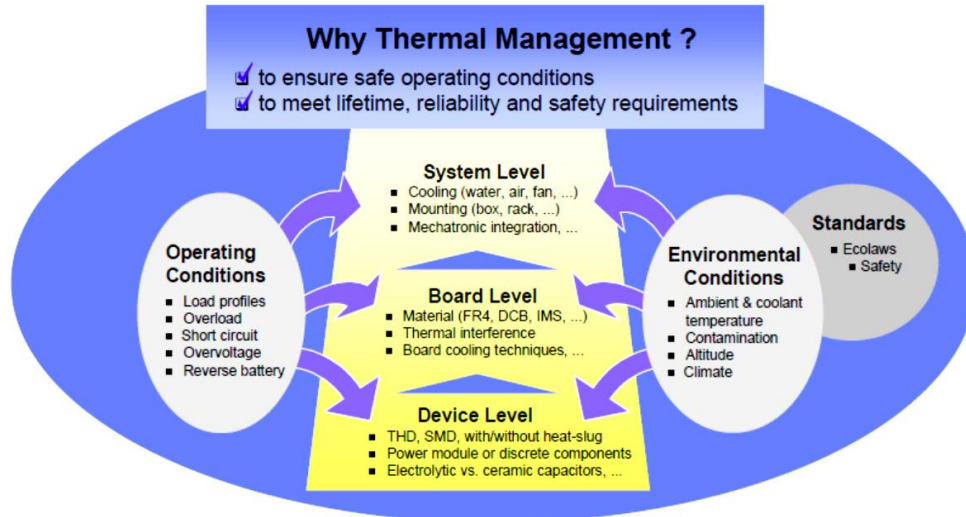


Fig.1-24. Thermal management - a continuous process during system engineering [118]

#### 1.4.3.1. Air Cooling

Systems with air cooled heat sinks dissipate heat directly into the air that flows through the system either by natural or forced convection. They are commonly made of well-known standard materials like Aluminum and Copper and are made of several fins placed on a base plate.

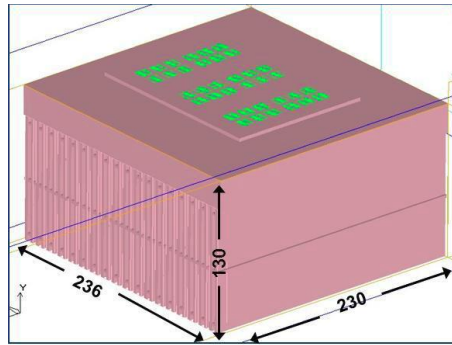
“Heat sink thermal resistance can be expressed through the following equation commonly used in heat exchanger design literature” [119, 120].

$$R_{sa} = \frac{1}{\dot{m}c_p \left(1 - e^{-\frac{hA}{\dot{m}c_p}}\right)} \quad (1.4-12)$$

where  $R_{sa}$  is the heat sink to air thermal resistance ( $W/mK$ ),  $\dot{m}$  is the mass flow rate ( $m^3/s$ ) of fluid through the heat sink (e.g. forced convection rather than natural convection),  $c_p$  is the heat capacity ( $J/kg$ ) of the fluid,  $h$  is the heat transfer coefficient ( $W/m^2K$ ) on the heat sink surface and  $A$  is the effective heat transfer area ( $m^2$ ).

According to Eq (1.4-12), heat sink thermal resistance can be reduced by increasing the mass flow rate  $\dot{m}$  (e.g. forced convection rather than natural convection), the heat capacity  $c_p$  (e.g. a liquid versus a gas), the heat transfer coefficient  $h$  (e.g. using smaller channel dimensions like micro-channels) and the effective heat transfer area  $A$  (e.g. using closely spaced fins) [120].

As shown in Fig.1-25 [120-122], authors have compared thermal performances of different heat sinks. It is demonstrated that a copper base would enable an ~40 % reduction in the spreading resistance and an ~60 % reduction in the spreading resistance could be achieved by using heat sink with heat pipes. They can significantly improve heat spreading in air cooled heat sinks.

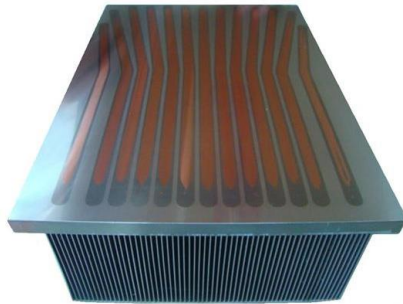


(a). Aluminum press-fin forced air cooled heat sink



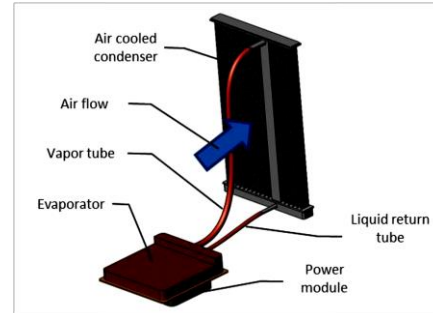
Courtesy Aavid

(b). Air cooled heat sink with copper base



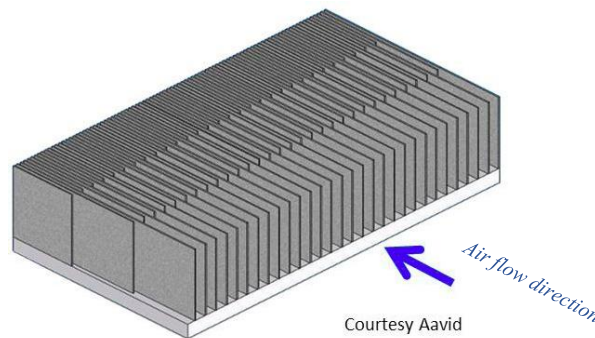
Courtesy Aavid

(c). Air cooled heat sink with embedded heat pipes



Courtesy Aavid

(d). Air cooled heat sink using loop thermosiphon



Courtesy Aavid

(e). Advanced heat sink with increasing fin density along air flow direction

Fig.1-25. Different air cooling systems design with heat sinks [120]

However, standard modules with air cooled aluminum heat sinks are not suitable for moving platforms, they are too heavy and voluminous for automotive uses.

#### 1.4.3.2. Liquid Cooling

Compared to air cooling with heat sinks, liquid cooling enables greater levels of integration and major reductions in the volume and weight. In liquid cooling systems, heat is transferred to a liquid which then flows to a remote heat exchanger and dissipate the heat to air or to another liquid in a secondary cooling system. As we can see in Fig.1-26 [123], existing and emerging liquid cooling solutions were extensively reviewed by the authors including:

- 1) Tube type and fin type Liquid Cold Plates (LCPs)
- 2) Single and double sided cooling using liquid jet impingement (SCJ and DCJ)
- 3) Micro-channel LCPs.

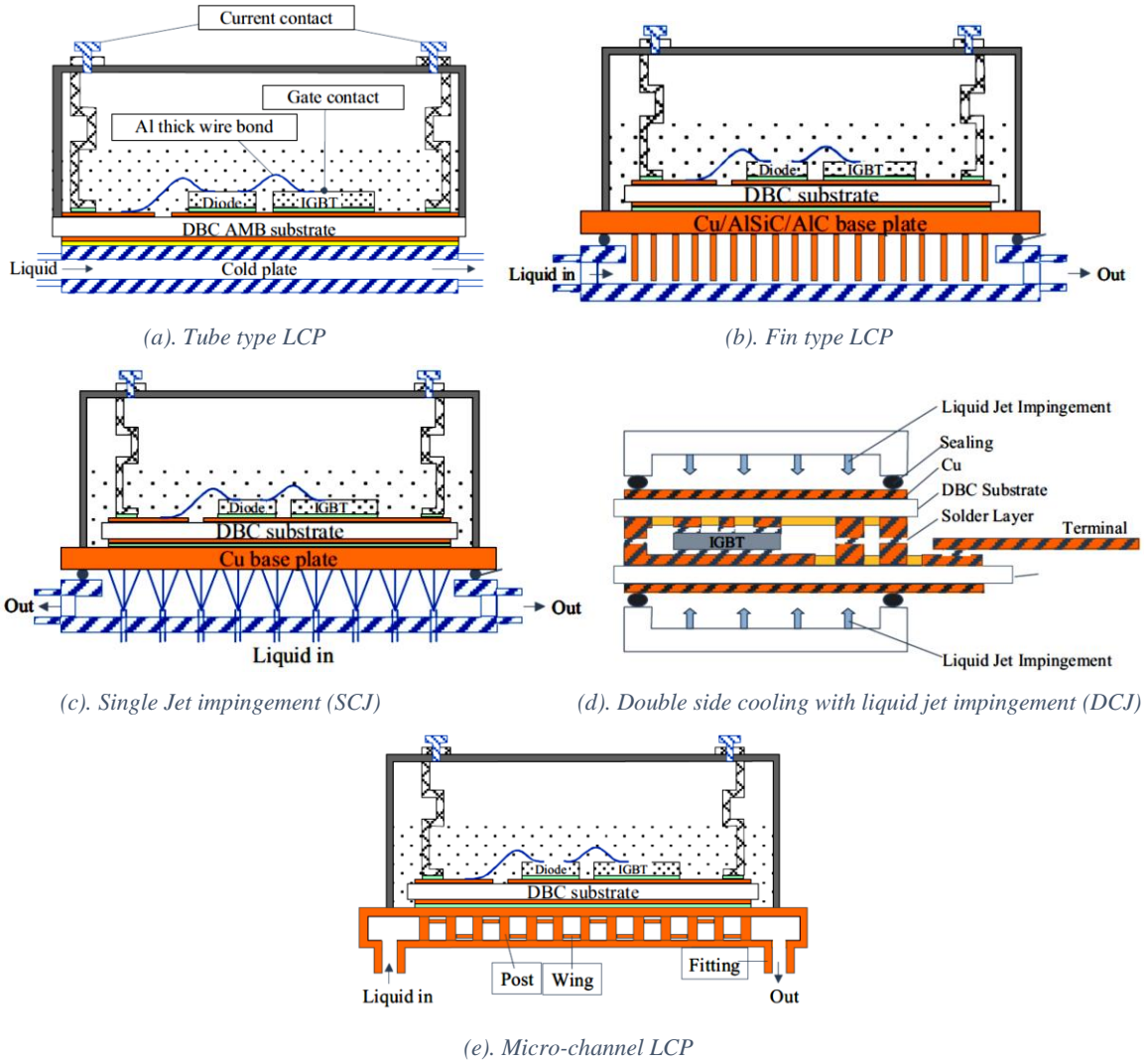


Fig.1-26. Different liquid cooling solutions [123]

Thermal resistance of cold plates depends on materials as copper or aluminum and internal structures [123-125]. According to the data extracted from [125] for commercial available cold plates, as shown in Fig.1-27 [123], it is obvious that the minimum values can be achieved by using micro-channeled copper based cold plates, usually offered by companies as Lytron, Mikros and Curamik.

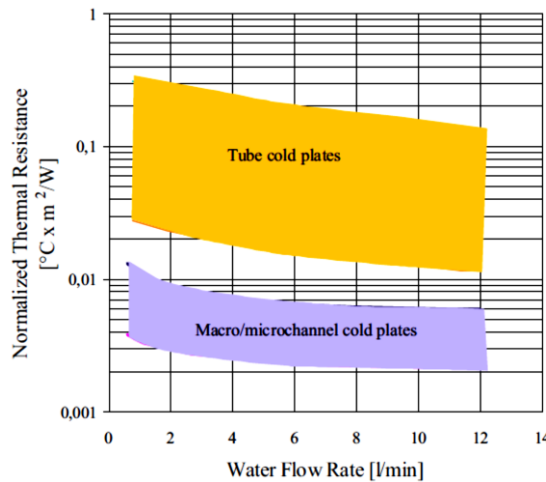


Fig.1-27. Thermal resistance of commercial available cold plates as a function of water flow [125]

For example, authors in [126] used double-sided cooling with micro-channels and direct surface contact with the IGBT die to achieve  $312 \text{ W/cm}^2$  per side and  $624 \text{ W/cm}^2$  at the base. The junction-to-case thermal resistance was reduced from  $0.312 \text{ K/W}$  to  $0.087 \text{ K/W}$ .

The DCJ have unique thin profile to the design which makes it an ideal choice for the embedded thermal management material for power electronics. Benefits of DCJ reduced volume requirement, reduced power requirement and increased life. Due to the design features of DCJ it proves to be the right choice for lower power electronics cooling in automotive, portable electronics etc. [127]. Besides, liquid cooling technology has better cooling performances than conventional fans for heat sink cooling.

#### 1.4.3.3. Solid Cooling

Conventional assemblies used in industrial applications based on standard modules with air cooled aluminum heat sinks are too heavy and voluminous, especially for automotive uses. Besides, the heat conduction capability of the cooling system or the thermal path of the structure is always the dominant factor of its thermal performances. So many efforts such as developing new semiconductor materials with higher thermal conductivities or improving packaging technologies, have been contributed in order to reduce the thermal resistances of the total structure with less additional components.

Recently, besides traditional solid-technologies of thermal vias, advanced thermoelectric solid-state cooling technology, based on polycrystalline miniaturized TE cooler [128], nanostructured superlattice TEC [129], mini-contact enhancement technology [130], and silicon and germanium substrate self-cooling [131] have received great attention and considerable progress has been made at the research level for high flux thermal management for microprocessors and electro-optic components. These solid-state techniques have compact structure, offer high reliability, can be locally applied, provide high cooling flux, and can be integrated with IC processing.

#### ❖ Thermal Vias

A thermal via is a plated through hole (PTH) plated with copper and is used to transfer the heat from one side of the PCB to the other side. PTH is a promising way of mitigating thermal issues by lowering the effective-thermal resistance of the structure. With thermal vias, the PCB acts as a pathway for the heat energy to reach the main heatsink, rather than serving as the heatsink itself. For example, main heat transfer path for a 2 layer PCB with thermal vias is shown in the Fig.1-28 [132].

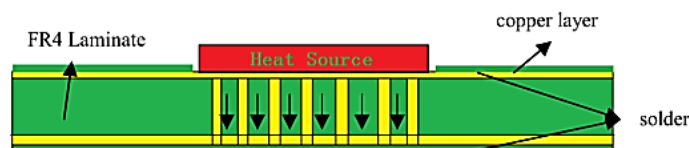


Fig.1-28. Section view of main heat transfer path for a 2 layer PCB with thermal vias [132]

Besides, Lee *et al.* studied arrangements of thermal vias in the packaging of multichip modules and found that as the size of thermal-via islands increased, more heat removal was achieved but less space was available for routing [133]. Relationships between via design parameters and the thermal resistance of thermal-via clusters have been presented in [134]. For these relationships, one-dimension theory for via-cluster was assumed to neglect the lateral effect of heat paths on the PCB copper surface between vias as the heat transfer is much more efficient vertically through the thickness than laterally from heat spreading.

Although these papers have limited application for the placement of thermal vias, the basic use and properties of thermal vias are demonstrated. But it is important to realize that

there is a tradeoff between routing and space and heat removal path, indicating that thermal vias should be used sparingly.

In addition, a significant temperature difference between the two sides of the vias limits the number of thermal cycles before the mechanical stress causes vias to start failing. In order to reduce the temperature rise on the PCB, the thermal resistance of the PCB to the heatsink should be designed to be as low as possible. This value is highly dependent on the thermal via pattern design of PCB. Thus, there is a need to properly design the thermal via pattern for high power application. Thermal via pattern optimization will be realized in the Chapter III.

#### ❖ *Thermoelectric Cooling (TEC) Devices*

The application of thermoelectric modules to cool electronics systems has been firstly discussed in 1965 by Kraus [135] in the book devoted to cooling electronic equipment. TEC is a thermal instrument used to transfer heat based on Peltier effect. The device transfers heat when there is a DC power applied, and as an application, it is widely used in different fields of science and technology, such as computer chips and CPU cooler [136], laser diode temperature stabilization [137], small refrigerator [138], semiconductor chip manufacturing [131], as well as the temperature management for Polymerase Chain Reaction (PCR) in biomedical and genetic field [139, 140]. Typically, the cold side of the TEC device is in contact with the chip to maintain the chip temperature below its designed temperature with natural or forced convection at the hot side of the TEC. The TEC module transports the heat from the chip to the ambient [141].

Although the principle of thermoelectricity dates back to the discovery of the Peltier effect in 1834, there was little practical application of the phenomenon until the middle 1950s because of the poor thermoelectric properties of known materials which made them unsuitable for use in a practical refrigerating device [142]. Refrigeration capacity of a semiconductor material is dependent on a combined effect of the material's Seebeck voltage, electrical resistivity, and thermal conductivity between the cold and hot side over the operational temperature range. Therefore, various TE materials are compared by an efficiency basis which is expressed in terms of a dimensionless figure of merit  $ZT$  [143, 144] as calculated by Eq (1.4-18).

$$ZT = \frac{S_e^2}{\rho \cdot \lambda_{th}} \quad (1.4-13)$$

This figure of merit represents the relationship between thermal conductivity  $\lambda_{th}$  ( $W/(m \cdot K)$ ), electrical resistivity  $\rho$  ( $\Omega \cdot m$ ), and Seebeck coefficient  $S_e$  ( $V/K$ ) of the thermoelectric material. The operating temperature is the most significant factor when choosing a TE material as shown in Fig.1-29 [145]. A larger  $ZT$  leads directly to a higher conversion efficiency. Maximizing  $ZT$  is the major objective in the selection and optimization of thermoelectric materials [143]. Today, bismuth telluride is commonly used as commercial TEC pellet material for refrigeration in the temperature range of  $-120$  °C to  $230$  °C.

A typical TEC device consists of multiple n-type and p-type elements soldered electrically in series but thermally in parallel between two dielectric plates. Thermoelectric refrigeration is achieved when a direct current flows through one or more pairs of n- and p-type semiconductor materials as shown in Fig.1-30.

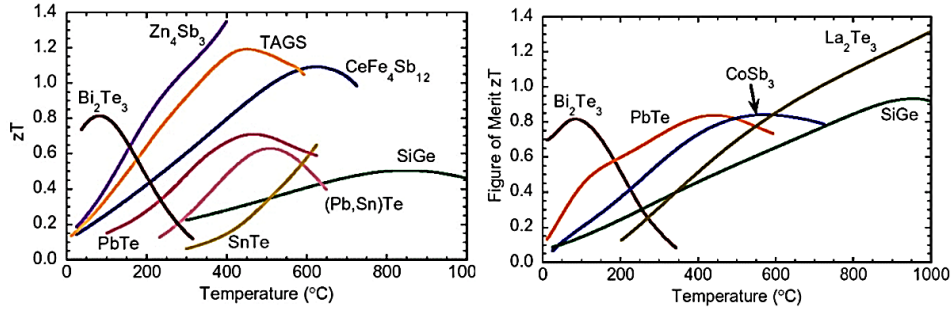


Fig.1-29. Curves of  $zT$  versus temperature for different materials [145]

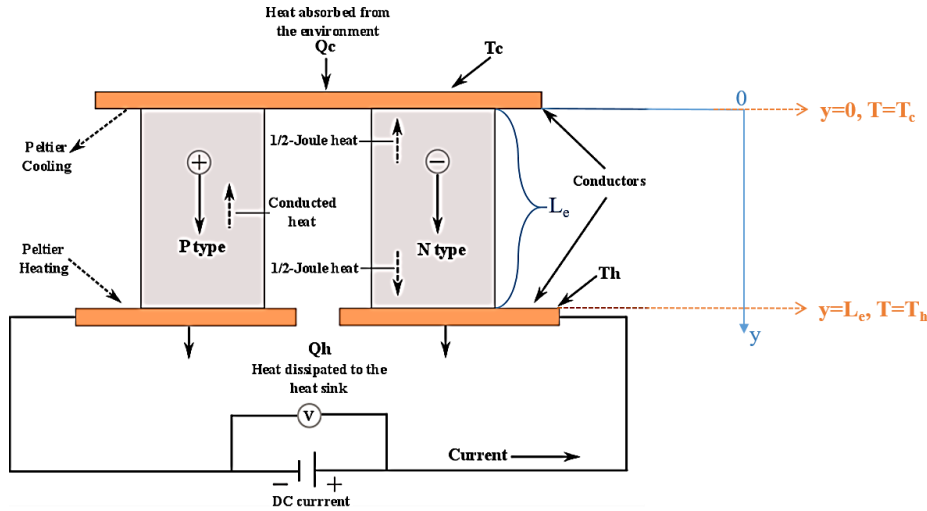


Fig.1-30. Schematic of thermoelectric module operation in cooling mode

In fact, five energy-conversion processes take place in a thermoelectric module: *Conductive heat transfer*, *Joule heating*, *Peltier cooling/heating*, *Seebeck power generation* and *the Thomson phenomenon* [146, 147]. All these processes account for the interrelations between thermal and electrical energies.

Thermal energy may be reversibly converted to electrical energy and vice versa in electrically conducting materials by thermoelectric effects. The Seebeck effect is a bulk effect that generates an electric potential gradient in a conductor subjected to a temperature gradient under open circuit conditions. It arises because thermal diffusion causes a flow of charge carriers (electrons or holes) along or against temperature gradients in conducting materials thereby generating an electric potential gradient  $dV$ . In an open circuit at equilibrium, the flow of charge carriers due to electrostatic forces balances that due to thermal diffusion. The Seebeck effect is described by  $dV = S_e dT$ . Thus heat is evolved or absorbed when current  $I$  flows through the interface between two conductors. This is known as the Peltier effect: the rate of reversible heat absorption at the interface ( $Q$ ) equals  $2 \cdot I \cdot S_e \cdot T$ . And the Thomson effect is usually a secondary effect that heat is also liberated or absorbed due to it when current flows through a conducting material in the presence of a temperature gradient. The irreversible effects of Joule heating and heat conduction leak must also be considered in the analysis of thermoelectricity [148-151].

The net rate of heat conducted out of a differential control volume normal to the  $y$ -direction defined in Fig.1-30 equals the rate of ohmic heat generation inside it [152]. Hence the form of the heat equation governing conduction inside the pellets is:

$$\frac{d^2T}{dy^2} + \frac{I^2 \rho}{\lambda_{th} A_e^2} = 0 \quad (1.4-14)$$



The boundary conditions on the heat equation at the two sides (cold and hot side) are  $T = T_c$  at  $y = 0$  and  $T = T_h$  at  $y = L_e$ , respectively. Thus, the temperature distribution  $T$  in the pellets is:

$$T = -\frac{I^2 \rho}{2\lambda_{th} A_e^2} y^2 + \left( \frac{I^2 \rho L_e}{2\lambda_{th} A_e^2} + \frac{T_h - T_c}{L_e} \right) y + T_c \quad (1.4-15)$$

Physically, the rate of heat transfer from the cold side  $q_c$  (for  $N = 1$ ) equals the rate of energy absorbed by the Peltier effect  $Q$  plus the rate of heat transfer by conduction into the pellets ( $-2\lambda_{th} \cdot A_e \cdot dT|_{y=0 \text{ or } L_e}$ ). Hence, for  $N=1$ :

$$q_c = 2 \cdot I \cdot S_e \cdot T_c - 2 \cdot \lambda_{th} \cdot A_e \cdot \frac{dT}{dy} \Big|_{y=0} = 2 \cdot S_e \cdot I \cdot T_c - \frac{I^2 \rho}{G} - 2 \cdot \lambda_{th} \cdot G \cdot \Delta T \quad (1.4-16)$$

$$q_h = 2 \cdot I \cdot S_e \cdot T_c - 2 \cdot \lambda_{th} \cdot A_e \cdot \frac{dT}{dy} \Big|_{y=L_e} = 2 \cdot S_e \cdot I \cdot T_c + \frac{I^2 \rho}{G} - 2 \cdot \lambda_{th} \cdot G \cdot \Delta T \quad (1.4-17)$$

Therefore, one-dimensional thermal balance equations of the TECs are summarized as Eq (1.4-18) to (1.4-22)(1.4-19).

$$Q_c = 2N \left( \underbrace{S_e \cdot I \cdot T_c}_{\text{Electron Heat Pumping}} - \underbrace{\frac{I^2 \rho}{2G}}_{\text{Joule Heating}} - \underbrace{\lambda_{th} \cdot G \cdot \Delta T}_{\text{Conduction Heat Leak}} \right) \quad (1.4-18)$$

Electron Heat Pumping      Joule Heating      Conduction Heat Leak

$$Q_{ed} = 2N \left( \underbrace{S_e \cdot I \cdot \Delta T}_{\text{Electron Heat Pumping}} + \underbrace{\frac{I^2 \rho}{G}}_{\text{Joule Heating}} \right) \quad (1.4-19)$$

Electron Heat Pumping      Joule Heating

$$Q_h = Q_c + Q_{ed} = 2N \left( S_e \cdot I \cdot T_h + \frac{I^2 \rho}{2G} - \lambda_{th} \cdot G \cdot \Delta T \right) \quad (1.4-20)$$

$$\Delta T = T_h - T_c, \quad G = \frac{A_e}{L_e} \quad (1.4-21)$$

$$V_{in} = 2 \cdot N \cdot \left( S_e \cdot \Delta T + \frac{I \cdot \rho}{G} \right) \quad (1.4-22)$$

$$COP = Q_c / Q_{ed} \quad (1.4-23)$$

where,

- $Q_c$  (W) is the power absorbed at the cold side;
- $Q_{ed}$  (W) is the electrically driven TEC power;
- $Q_h$  (W) is the heat generated at the hot side;
- $V_{in}$  (V) is the TEC voltage;
- $COP$  is the coefficient of performance of the TEC device;
- $\Delta T$  (K) is the temperature difference between two sides of Peltier
- $N$  is the number of PN pellets;
- $I$  (A) is the input current;
- $T_c$  (K) is the temperature of the cold side of TEC device;
- $T_h$  (K) is the temperature of the hot side of TEC device;
- $A_e$  (m<sup>2</sup>) is the section area of Pellet leg;
- $L_e$  (m) is the leg length of the pellet.

As a solid-state technology, TEC devices have fast and precise temperature control as no moving parts and no working fluids exist, which involves simple integration, little maintenance, silent operation, and excellent reliability [153]. In other words, TEC provides an active cooling of a chip to keep its operating temperature below the designed point. Along with the advantages that TEC brings in, some existing issues should be considered including

extra power loss due to Joule heat, design optimization in terms of temperature control and overall efficiency etc. These limitations of TEC systems lie in their low system coefficient of performance (COP usually less than one), but recent studies have shown that TEC can operate with a COP greater than one [150, 151, 154, 155], making it an attractive candidate for thermal management.

❖ *Pyrolytic Graphite Sheets (PGS)*

Pyrolytic graphite sheets are made of synthetic graphite material with better thermal conductivity in x and y plane (from 700 to 1950 W/mK for density of 0.85 to 2.13 gm/cm<sup>3</sup>) in comparison to the standard metals, 2 to 5 times higher than copper and 3 to 8 times higher than aluminum, which is almost close to the naturally available diamond [156, 157].

As shown in Fig.1-31, PGS is very thin, flexible and could be cut into customizable shapes. It is ideal for thermal management as a thermal interface material (TIM). Thanks to its thermal spreading properties, it is proposed in [127] that PGS can be used as bonding agent between the heat pipes and the power devices to transfer heat for multiple layers of PCB structures. Today, there are also many applications of PGS in smart phones, tablet PCs and peripherals, LED devices, etc.

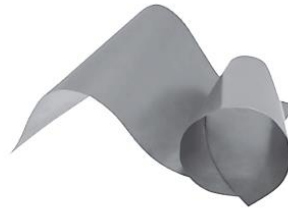


Fig.1-31. Pyrolytic graphite sheet from Panasonic PGS product datasheet [156]

1.4.3.4. Hybrid Cooling

More and more advanced technologies focus on the hybrid cooling solutions for purpose of uniform cooling and better cooling effect. That means, it is attractive to improve the external heat convection capacity and the dominant heat conduction ability at the same time for better thermal performances of electronics systems.

As presented in Fig.1-32 [117], authors have designed a cooling system for a 10×10 mm<sup>2</sup> IGBT chip by combining cold plate with a TE solid-state cooling, which is a hybrid solid- and liquid-cooling design. It is demonstrated that thin-film superlattice TEC can successfully isothermalize IGBT chip and eliminate 94 % of the temperature non-uniformity for the 100W/cm<sup>2</sup> IGBT chip and 91 % for a 200 W/cm<sup>2</sup> IGBT chip.

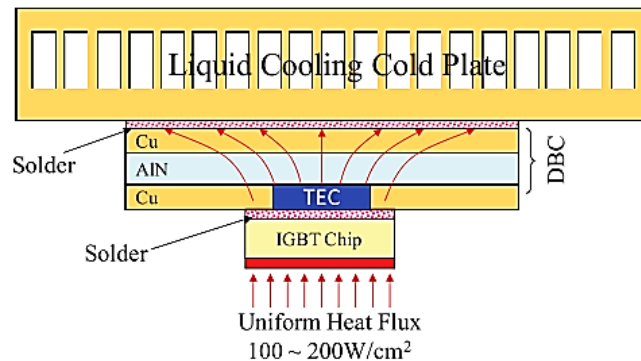


Fig.1-32. Hybrid solid- and liquid-cooling designs for IGBT isothermalization [117]

Recently, a concept of embedded thermal management has been proposed as shown in Fig.1-33 [127] for PCB structures using 3D integration technologies. A heat pipe and PGS layer could be assembled between two PCB dielectric layers. Thermal dissipation between layers could be improved and also the space consumed by heat sinks can be minimized. Although this idea has not been realized yet due to current technology limits of the PCB 3D printers, authors have demonstrated the feasibility of this proposed concept by separately validating the cooling effects of DCJ and PGS at the first time.

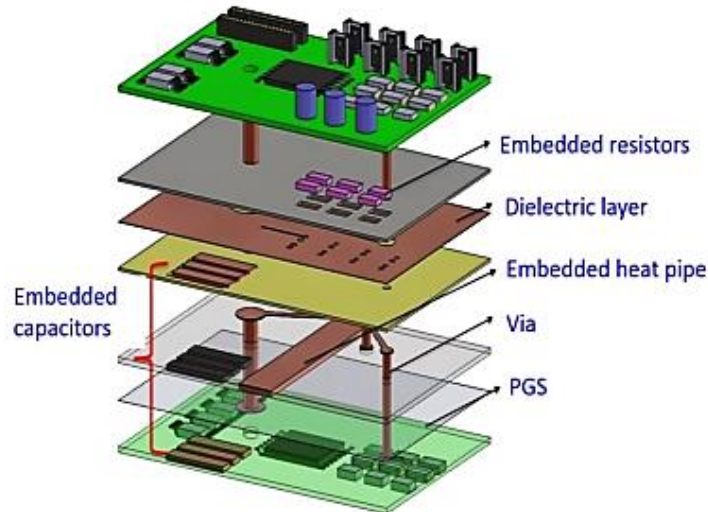


Fig.1-33. Embedded thermal solutions for PCB structures using PGS and heat pipe techniques [127]

#### 1.4.3.5. Conclusion

Different cooling methods for power systems, especially for PCB structures have been reviewed and described. Pros and cons of each solution have been analyzed depending on their principals, cooling efficiency, applications, etc. All these reviewed research work give us basic heating flow possibilities based on the two main heat runways, especially the heat conduction and convection process. This will help us to develop our own suitable cooling methods for certain PCB structures.

In a word, cooling system should be appropriate and efficient to keep the cell temperature low as well as uniform, but should also be simple and reliable.

## 1.5. SUMMARY

In this chapter, some important features of the power converters and different thermal management solutions for PCB structures are presented. The active components, the converter topologies and their power losses are introduced at the first place.

Then, DBC technology and PCB technology have been compared in terms of material properties and thermal performances. With DBC technology, heat dissipation can be realized vertically to the heatsink and ceramic substrate of DBC has much higher thermal conductivity than that of PCB made of FR4 ( $<1.5 \text{ W/mK}$ ) material. But, with PCB technology, 3D integration can be achieved and heat can be evacuated through both the upper side and the bottom side of the packaging.

The third part of this chapter focuses on the thermal measurement and management of PCB structures based on heat conduction. For thermal prediction purpose, different methods are introduced including analytical, 3D FE modelling methods. For thermal measurement purpose, electrical methods and calorimetric methods are described. Calorimetric methods

are preferred in this thesis because of its high precision without any signal distortions of electrical probes.

At the end of this chapter, different thermal management solutions in literature have been reviewed including air cooling methods with heatsink, liquid cooling methods with heat pipes, solid cooling methods with thermal vias or TEC devices, as well as hybrid cooling methods for high cooling demanding cases. In fact, suitable cooling methods should be chosen depending on the cooling requirements in consideration of their pros and cons. Different from conventional cooling methods, TEC cooling devices are attractive for their silent operation and fast dynamic response.

## CHAPTER 2. THERMAL INSTRUMENTATIONS

- 2.1. Introduction
- 2.2. Test Bench
- 2.3. Chip Attachment on The PCB Substrate
- 2.4. Through-Hole Electroplating
- 2.5. Summary



# CHAPTER 2. THERMAL INSTRUMENTATIONS

## 2.1. INTRODUCTION

This chapter will be devoted to describe all used instrumentations regarding to the established test bench serving as experimental platform. This platform is based on the temperature measurement methods and calorimetric method presented in the first chapter. At the same time, calibration process of certain equipments such as Resistance Temperature Detector (RTD) sensor will be discussed. In addition, general descriptions concerning applied softwares for analytical calculation and 3D FE Modeling will be presented. For example, Solidworks, COMSOL Multiphysics, Matlab, etc. Besides, typical chip soldering procedure and hole plating process will be presented in respect to the PCB technology.

## 2.2. TEST BENCH

### 2.2.1. Establishment

According to previous studies of power loss measurement principles presented in part 1.4.2.2 of chapter 1, the schematic and pictures of the proposed test bench based on the open type calorimetric method is shown in Fig.2-1. The power loss measurement method is based on the heat conduction theory given in (1.4-11) for which it is assumed that the power loss of the heating source under test will pass vertically through the duralumin cylinder to the radiator.

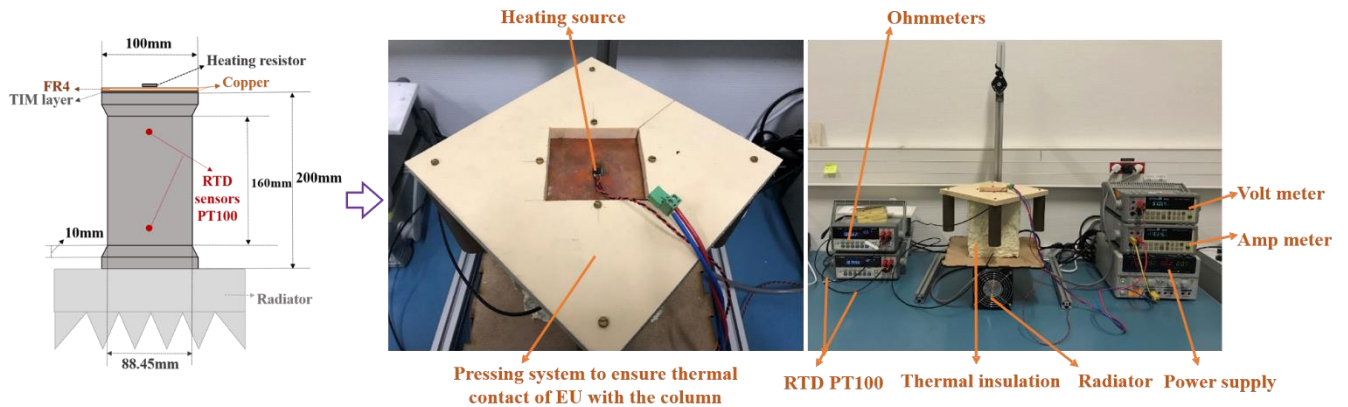


Fig.2-1. Power loss measurement test bench

To obtain precise measured value of power loss  $P$  (W) passing through the duralumin column, the temperature difference between two RTD sensors  $\Delta\theta_{RTD}$  (°C) and the knowledge of the thermal resistance of duralumin column for the length between the two RTD sensors  $R_{th\_du}$  (W/mK) are essential.

### 2.2.2. RTD Sensor (PT 100) Calibration

Empirically, PT 100 (Fig.2-2) has a resistance  $R$  ( $\Omega$ ) of  $100 \Omega$  at  $0^\circ\text{C}$  and the fundamental interval between  $0^\circ\text{C}$  and  $100^\circ\text{C}$  is  $0.385 \Omega$ . So the temperature measured by RTD  $\theta_{RTD}$  (°C) could be expressed as in Eq (2.2-1).

$$\theta_{RTD}(\text{°C}) = \frac{R-100}{0.385} \quad (2.2-1)$$

Two sensor probes are inserted in an aluminum cuboid in order to evaluate their resistance difference for the same temperature point. The cuboid is then placed into a forced-air oven (Fig.2-3), providing temperature  $T_{oven}$  (°C) that may vary from  $20^\circ\text{C}$  to  $60^\circ\text{C}$ .

Resistances of the two sensors are measured by Kelvin (4-wire) resistance measurement method when the system has reached its stable state (one hour per measurement).



Fig.2-2. RTD sensor PT 100 (Online source: flukecal.com)

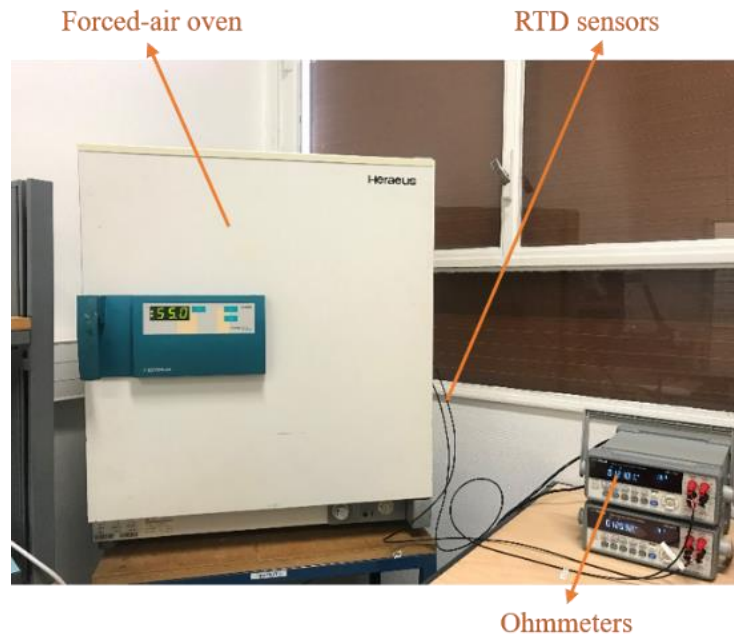


Fig.2-3. Test bench for calibrating RTD sensors

After ten times of measurement for each fixed air-oven temperature, average resistance difference and the corresponding theoretical temperature difference for each point has been calculated as shown in Fig.2-4. Ideally,  $\Delta\theta_{RTD}$  should be zero when the relationship in Eq (2.2-1) is applied for temperature calculations of the two sensors.

For calibration purpose, the RTD sensor at the bottom of cylinder column is considered as reference and the relationship between  $\theta_{RTD}$  and  $R$  in (2.2-1) is applied for this sensor. The relationship between  $\theta_{RTD}$  and  $R$  for the top sensor is then modified to suppress the offset and gain error. The proposed relationship for the top sensor is given in (2.2-2).

$$\theta_{RTD} = \frac{R - 99.945}{0.3856} \quad (2.2-2)$$

With this new relationship between the top sensor temperature and the top sensor resistance, the temperature differences between the two sensors ( $\Delta\theta_{RTD}$ ) is recalculated and

shown in Fig.2-5. From this figure, we can verify that average intrinsic errors between the two RTD sensors could be considered as null.

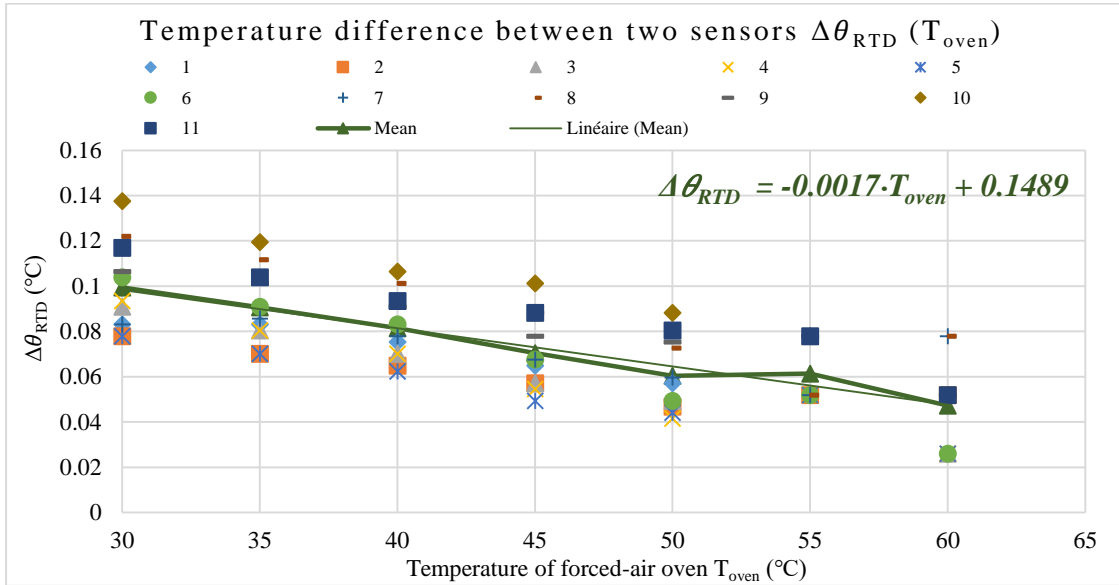


Fig.2-4. Temperature differences between two RTDs following temperature of forced-air oven

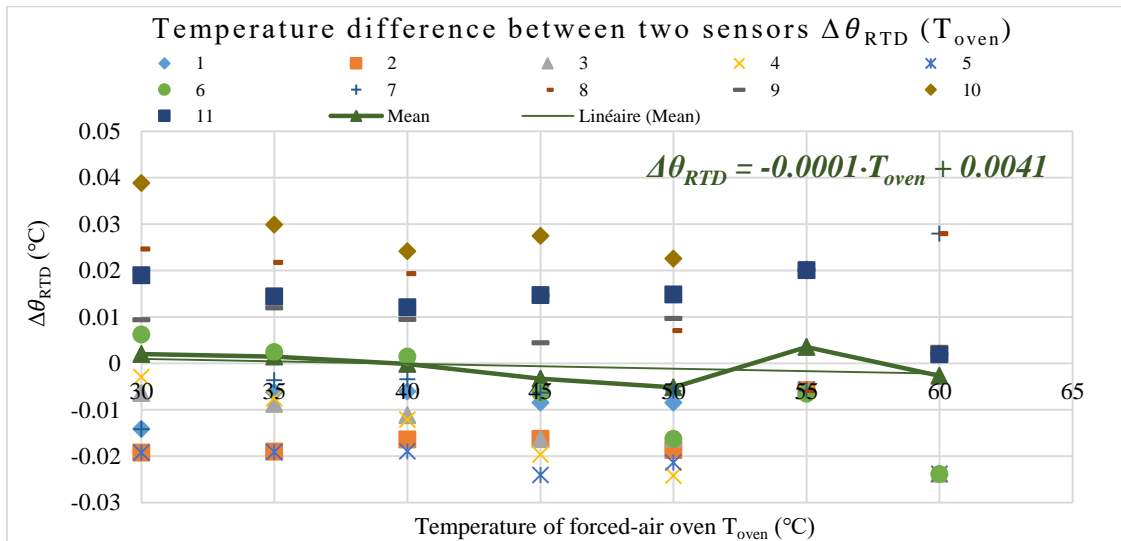


Fig.2-5. Temperature differences between two RTDs after calibration

### 2.2.3. Thermal Conductivity of Duralumin $\lambda_{dura}$ (W/mK)

The two RTDs (with the corrected relationship) have been used to determine the precise thermal conductivity of duralumin  $\lambda_{dura}$  (W/mK). As shown in Fig.2-1, a heating resistor is mounted on the PCB substrate and a piece of glass wool for thermal insulation is applied to cover the top side of the PCB module to avoid heat convection between the heating resistor and the air. So, the dissipated power of the heating resistor will mainly pass through the duralumin column by neglecting the heat convection and heat radiation effects. Based on (1.4-11), the thermal resistance of the duralumin column between the two RTDs  $R_{th\_du}$  could be obtained by inputting a heating power and measuring the temperature difference  $\Delta\theta_{RTD}$ .

Measurement has been performed 5 times to obtain the average value of  $R_{th\_du}$ . It is assumed that the ambient temperature for these measurements is constant. Relationship between temperature difference  $\Delta\theta_{RTD}$  and input power  $P$  has been drawn in Fig.2-6. So, the



thermal resistance between two RTDs is obtained as  $0.187$  °C/W. Then the thermal conductivity of the duralumin  $\lambda_{dura}$  can be calculated by using (1.4-11). It is equal to  $130.45$  W/(mK). This values is postulated to be independent of temperature and kept constant to be applied for power loss calculations.

The obtained value of  $R_{th\_du}$  will be used for the power loss measurement and the deduced  $\lambda_{dura}$  will be applied for 3D FE simulations in the following sections.

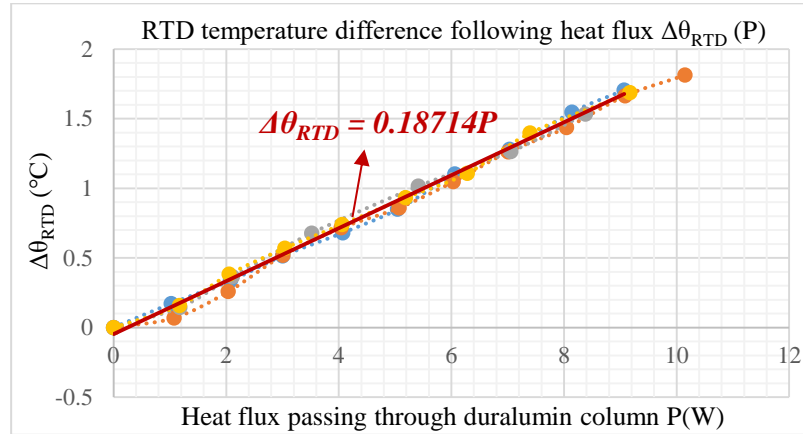


Fig.2-6. Measured relationship between input power and temperature difference between two RTDs

#### 2.2.4. Temperature Measurement Equipments

Besides the RTD sensor, this part will list other temperature measurement equipments applied for this thesis including the infrared camera and the thermocouples.



Fig.2-7. Thermography camera FLIR T450sc [158]

#### ❖ Infrared Camera (IR camera)

Thermography camera FLIR T450sc (Fig.2-7 [158]) has a rotating optical block and touch screen interface. It can produce thermal images of  $320 \times 240$  pixels. And it works seamlessly with FLIR ResearchIR Max software, allowing us to control the camera in order to view, acquire, analyze, as well as record the thermal data. Besides, it can capture thermal data directly into MathWorks® Matlab software for advanced image analysis and processing.

For example, a thermal imaging of a PCB structure with a soldered Si diode has been shown in Fig.2-8. Before measuring with the IR camera, the surface of the PCB module has been painted in black in order to avoid the reflection effect. From the imaging interface, it can be identified that the maximum surface temperature is  $42.4$  °C and the ambient temperature is  $26.4$  °C.

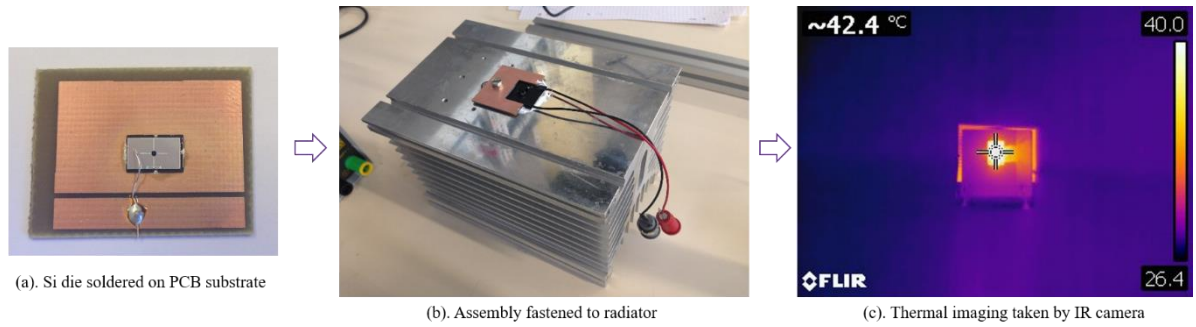


Fig.2-8. Thermal imaging of a simple PCB structure

#### ❖ Thermocouple

As previously mentioned, a thermocouple is an electrical device consisting of two dissimilar electrical conductors forming electrical junctions at different temperatures. A thermocouple is widely used as a type of temperature sensor. It produces a temperature-dependent voltage as a result of the thermoelectric effect, and this voltage can be interpreted to measure temperature [159].

The K&T type thermocouple and the thermometer used in this thesis is presented in Fig.2-9. It's easy to apply with fast response and welded exposed junction. According to the product datasheet, the temperature range of this kind of thermocouple is between  $-75\text{ }^{\circ}\text{C}$  to  $+250\text{ }^{\circ}\text{C}$ .

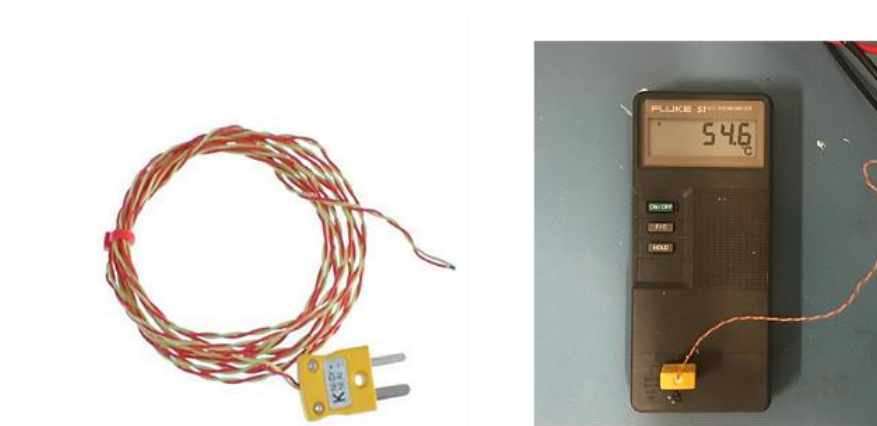


Fig.2-9. K&T type thermocouple (ANSI MC96.1) [160] and thermometer

#### 2.2.5. Applied Softwares

The main methods used for thermal performances analysis are analytical (2D) and 3D FE methods. On the one hand, analytical methods are based on thermal theories as heat convection, heat conduction and heat radiation. Analytical models will be created with the help of Matlab Simulink. On the other hand, 3D FEM is a numerical method allowing to solve problems in some area of physics as for simulation of dielectric, magnetic, thermal, mechanic etc. Here in this thesis, software COMSOL Multiphysics has been used mainly for 3D thermal simulations.

This part is devoted to introduce the modelling process with the two softwares (Matlab, COMSOL) in case of a simple PCB structure shown in Fig.2-8 (a). The structure dimensions are shown in Fig.2-10. The purpose is to estimate the maximum chip temperature  $T_c$  ( $^{\circ}\text{C}$ ). Power of  $1\text{ W}$  is input in the chip for all simulations. Heat convection and heat radiation effect have been neglected to simplify the simulations here.

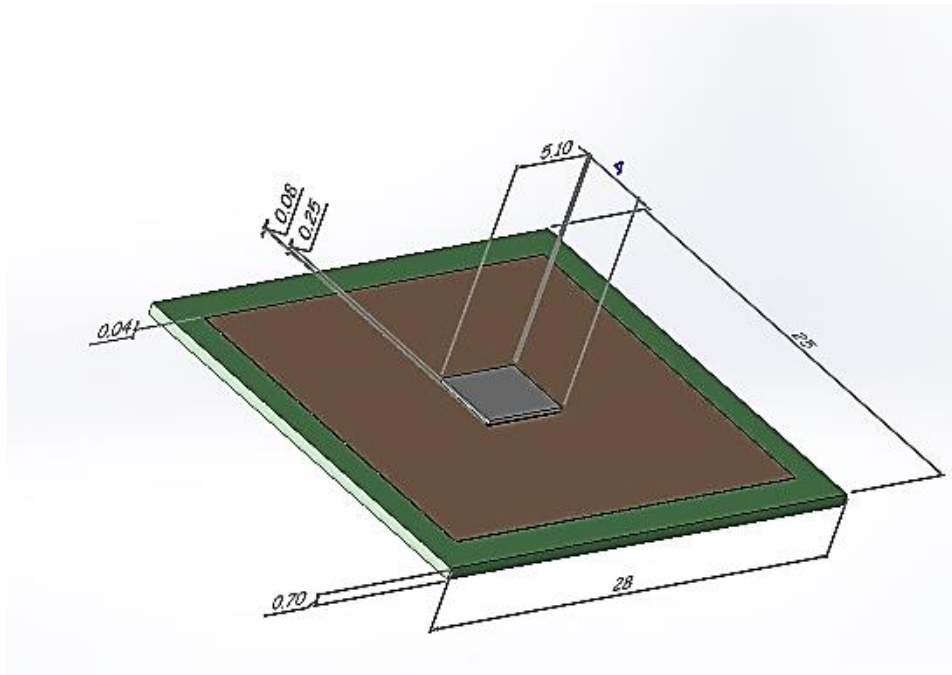


Fig.2-10. 3D model of the PCB structure with soldered Si chip (dimensions in mm)

✧ Analytical Modeling (2D) with Matlab Simulink

Analytical model or thermo-electric model is based on the analogy of thermal elements to those in electrical circuit. Thermal to electrical analogy is summarized in Table 2.1.

Table 2.1. Thermal to electrical analogy

Thermal quantities	Units	Analogous electrical quantities	Units
Heat Q	W	Current I	A
Temperature T	K	Voltage V	V
Thermal resistance $R_{th}$	K/W	Resistance R	$\Omega$
Heat capacity $C_{th}$	J/K	Capacity C	F
Absolute zero	0 K	Ground	0 V

The analytical model can be realized in four steps:

- Step 1: Choosing appropriate physical model for analyzing the PCB structure to be modeled.
- Step 2: Calculating equivalent thermal resistances or thermal capacitances of the total thermal path according to different components properties of the system.
- Step 3: Drawing corresponding thermo-electric circuit with predefined thermal components in Matlab Simulink interface.
- Step 4: Executing the 2D simulation to get desired value or evolution of certain parameters such as junction temperature.

For example, as presented in Fig.2-11, model of the PCB structure (Fig.2-10) has been built by using lumped parameters method. Here, the heat flux flows both laterally along the copper layer and vertically through the PCB substrate.  $R_{sith}$  (W/mK) represents the thermal resistance of the chip,  $R_{sth}$  (W/mK) is the thermal resistance of the solder. Besides,  $R_{li}$  ( $R_{l1}, R_{l2}, R_{l3}...$ etc.) and  $R_{vi}$  ( $R_{v1}, R_{v2}, R_{v3}...$ etc.) represent the lateral and vertical thermal resistances of lumped elements. Ambient temperature  $T_{ambient}$  equals to 300 K.

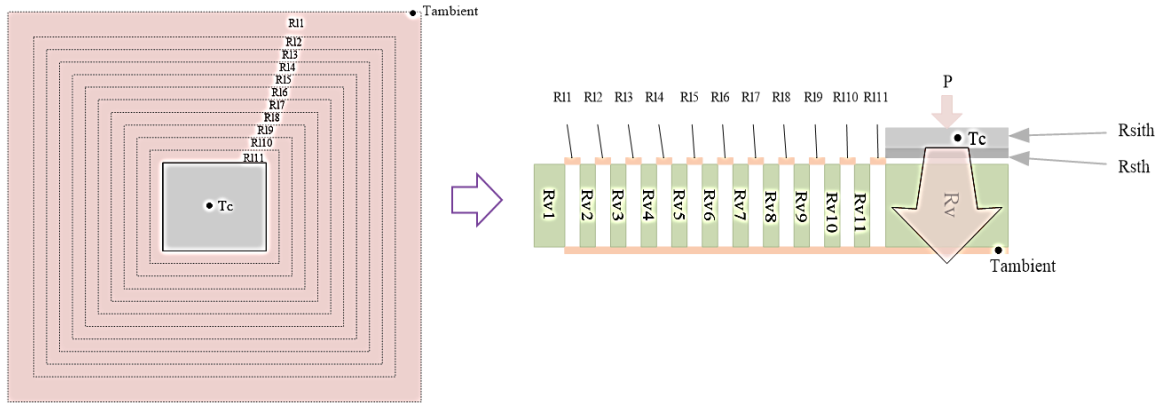


Fig.2-11. Top and section view of lumped parameter model for the PCB structure

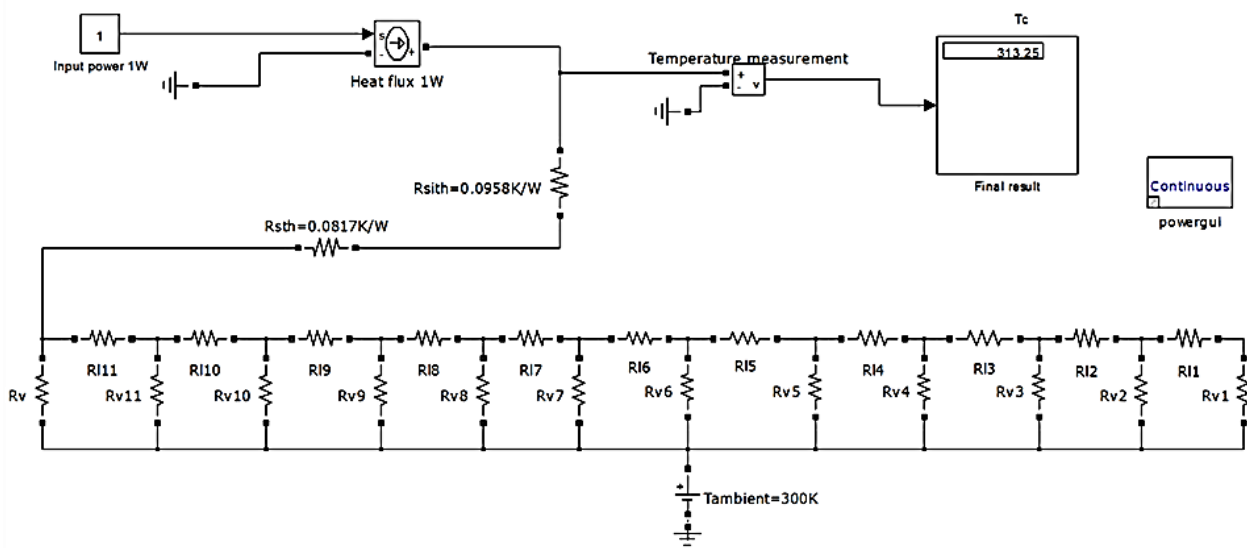


Fig.2-12. Steady-state thermal network for the PCB structure

Then the corresponding thermal model has been created in Simulink.  $R_{li}$  ( $R_{l1}, R_{l2}, R_{l3}...$ etc.) and  $R_{vi}$  ( $R_{v1}, R_{v2}, R_{v3}...$ etc.) are calculated according to the module dimensions (Fig.2-10) and the thermal resistance equation (1.4-11). As we can see in Fig.2-12, the analytical maximum chip temperature is **313.25 K** for an ambient temperature equal to **300 K**.

#### ❖ FE Analysis (3D) with COMSOL Multiphysics

Different from analytical models which need complex pre-calculations depending on the structure geometry, 3D FEM can provide us more precise and intuitive simulated results by applying reasonable boundary conditions.

The 3D simulations can be realized in five steps:

- Step 1: Creating a 3D model of the structure to be simulated.
- Step 2: Choosing appropriate modules or ‘physics’ according to the problems needed to be solved.
- Step 3: Describing the structure with boundary conditions.
- Step 4: Creating meshes of the domain.
- Step 5: Executing simulations and visualizing the 3D simulation results.

The geometry of the 3D model could not only be created by COMSOL itself, but also by SolidWorks, AutoCad or Matlab, etc.

For example, 3D thermal simulation results of the PCB structure (Fig.2-10) is presented in Fig.2-13.  $1\text{ W}$  is applied in the Si chip as heating source. The PCB module is attached to a heat sink and the bottom surface is assumed to be at ambient temperature of  $300\text{ K}$ . Heat convection effect is neglected. Complete mesh consists of  $63007$  domain elements,  $20720$  boundary elements, and  $1096$  edge elements. The estimated maximum chip temperature is  $313.36\text{ K}$ .

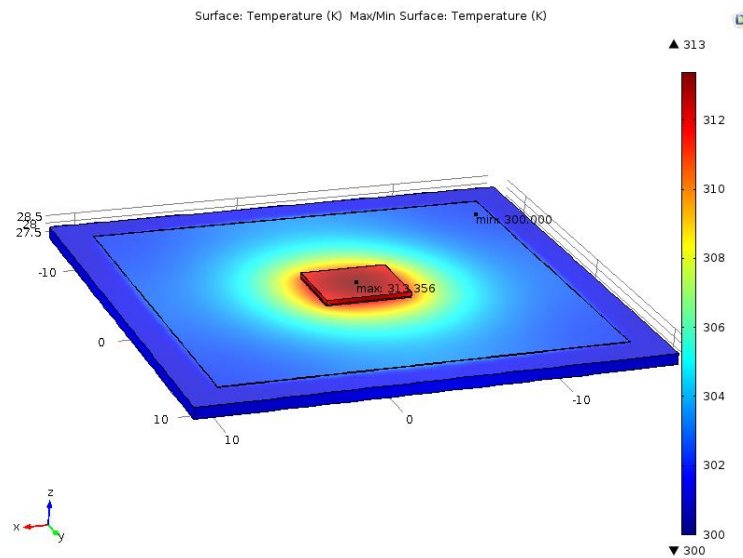


Fig.2-13. 3D Thermal simulation of the PCB structure

Comparing simulation results with those obtained by experimentations ones (Fig.2-8 (c)) shows that both methods give a correct estimated temperature despite the errors caused by wire bonding impact (not modeled) and heat convection ignorance in both methods. Material properties for thermal simulations are the same as listed in Table 3.1 (Chapter 3).

## 2.3. CHIP ATTACHMENT ON THE PCB SUBSTRATE

This part mainly focuses on the fabrication technology of PCB structure. Based on a soldering procedure of Si chip on the PCB substrate, preparation process of PCB as well as the realization of the chip attachment will be presented in order to introduce the materials and equipments used for manufacturing a PCB structure.

### 2.3.1. Preparation of PCB Substrate

A full fabrication process of PCB is shown in Fig.2-14 [161]. The typical processes to prepare the PCB substrate as shown in Fig.2-15 are described in the following five steps:

- Step 1: Creating the substrate by lamination technology with prepreg, which is a glass fabric pre-impregnated in resin. More details could be found in [161].
- Step 2: Substrate cleaning. Before covering the substrate by resin or photosensitive film, this cleaning step is important to avoid yielding a poor coating by the resin. That means, the particles or the residues left on the surface may create small holes in the deposited layer.
- Step 3: Photolithography. Firstly, coating or marking the substrate with liquid photoresist which aims to protect the copper part of the circuit. Then it is exposed to an ultraviolet radiation so that the exposed areas become soluble for positive resin. Here the etch mask with ink pattern can be created by Eagle or Altium

softwares. Lastly, the development step is realized by dipping the PCB substrate in a developer. The exposed area of the photoresist will be dissolved for the positive resin.

- Step 4: Etching. The copper etching is made directly in ferric chloride solution or with an etchant spray system. And it's necessary to do this step repeatedly until the exposed copper part is fully cleaned.
- Step 5: Stripping. This last step is to clean the substrate with chemical reagent before the chip soldering.

More details of applied materials and fabrication technologies of PCB are described in the thesis of YU [2].

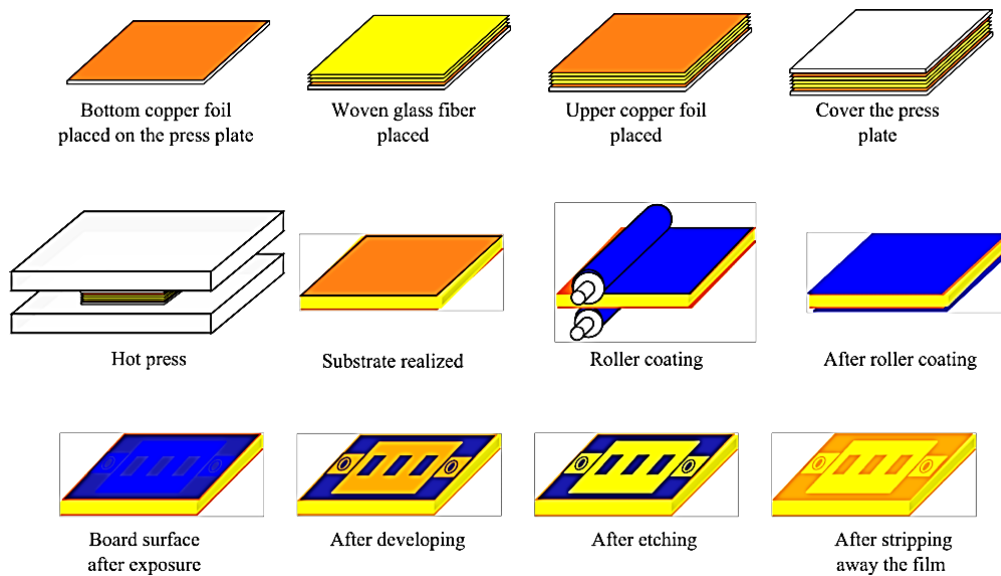


Fig.2-14. Fabrication process of PCB [161]

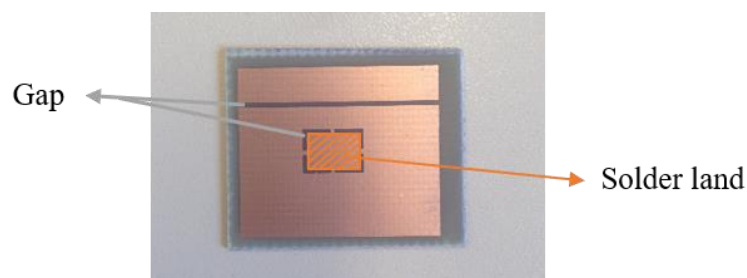


Fig.2-15. Prepared PCB substrate for chip soldering

### 2.3.2. Chip Soldering

Once the PCB substrate has been prepared, chip can be soldered by reflow method summarized in Fig.2-16. Before the procedure of soldering, the PCB substrate has been put on a polishing machine with a grit paper in order to smooth the copper surface layer. Then, the selected paste (Sn62-Pb36-Ag2) has been applied on the PCB by screen printing. The solder thickness depends on the thickness of the applied screen printing.

After mounting the chip on the paste, the whole substrate is put in a preheated reflow oven (preheated temperature: 110 °C). The temperature used for soldering depends on the PCB reflow profile, which is generally determined by the melting temperature of the solder,

the heat resistance of the components, and the characteristics of the PCB. Here, the reflow profile used for the PCB (Fig.2-15) is  $160\text{ }^{\circ}\text{C}$  during  $90\text{s}$  followed by  $250\text{ }^{\circ}\text{C}$  during  $120\text{s}$ .

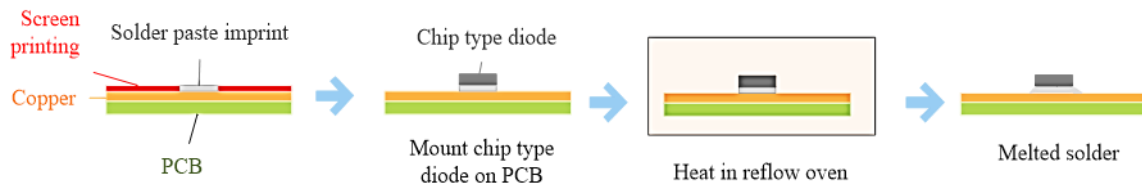


Fig.2-16. Chip soldering process

## 2.4. THROUGH-HOLE ELECTROPLATING

Electrolytic copper solution is widely used in many industrial applications like anticorrosion and decorative coatings, etc. Copper is electrodeposited over a surface of wafer such as through holes. And aqueous sulfuric acid baths are usually used for filling the through holes [162]. Here, the through holes are metallized with copper to behave as the thermal vias for heat power dissipation but without any electrical interconnection purpose.

A typical copper plating solution contains copper sulfate, sulfuric acid, chloride ions, and organic additives that control the deposition process and the quality of the plated coatings.

The via metallization process for the PCB substrate (Fig.2-17) is mainly based on the five following steps:

- Step 1 : Surface preparation by chemical acid cleaning. The purpose is to remove the fingerprints and oxides.
- Step 2 : Hole cleaning with  $10\%$  soda at  $70\text{ }^{\circ}\text{C}$  during 4 minutes and rinsing with water.
- Step 3 : 7 minutes for the deposit of colloidal palladium (4 minutes for preparation).
- Step 4 : Rinsing with water and drying.
- Step 5 : 30 minutes for plating process with copper sulfate solution.

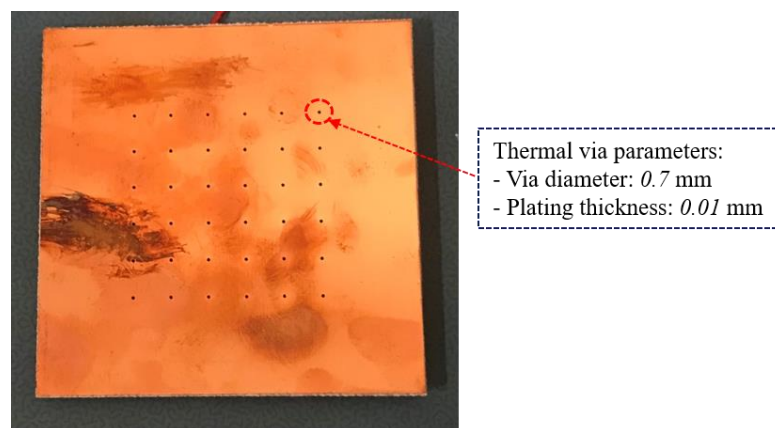


Fig.2-17. Electroplated vias in the standard PCB substrate

## 2.5. SUMMARY

In this chapter, a test bench for power loss measurement by calorimetric method has been firstly presented as well as the measurement equipments such as RTD sensors, thermocouples and IR camera, etc. Simulation softwares have been discussed in case of

thermal simulation of a simple PCB structure. The purpose is here to briefly illustrate the analysis steps for creating thermal models corresponding to the real PCB structure by using analytical or 3D FE methods.

In addition, concerning the PCB technology, the chip soldering process has been presented to show the total fabrication procedure of a PCB structure as well as hole electroplating technology used to create thermal vias.



## CHAPTER 3. OPTIMIZATION OF THERMAL VIAS

- 3.1. Introduction
- 3.2. Analytical Analysis
- 3.3. 3D FEM Analysis
- 3.4. Experimental Results and Discussions
- 3.5. Conception of The Inverse Thermal Model
- 3.6. Summary



## CHAPTER 3. OPTIMIZATION OF THERMAL VIAS

### 3.1. INTRODUCTION

In many cases, addition of thermal vias yields an alternative thermal management solution that may potentially eliminate the need for separate heat sink parts [134]. Related modeling studies on the via network exist in literature for typical packaging applications [133, 163]. Optimization of the thermal via design is an important issue in thermal performance management engineering due to the complexity of their structure. Questions about thermal via parameters such as via diameter, via plating thickness, number of vias as well as via pattern are often expected to be answered. Therefore, this chapter addresses a design guideline on thermal via parameters for the PCB structures.

The most common material to fill the thermal vias is copper and one can imagine that thermal vias are located in a relatively large domain and isolated by the board material of FR4 with a worse thermal conductivity. Small vias in the PCB substrates close to each other can form a cluster with relatively large dimension. So, the heat flow will across vertically the substrate with negligible lateral heat spreading effect. Therefore, one-dimensional (1D) heat conduction can be proposed for analytical simplification by considering the thermal vias and the PCB substrate as parallel thermal networks [134]. This 1D heat conduction assumption will be applied for the following discussions.

In this chapter, thermal performances in steady state of the PCB structures with thermal vias will be studied by analytical and 3D FEM analysis in order to optimize the cooling effects of thermal vias. Experimental validation will be executed to verify the simulation predictions. In addition, concerning the power loss measurement method, the conception of inverse thermal models will also be discussed.

### 3.2. ANALYTICAL ANALYSIS

Firstly, to figure out the cooling mechanism of thermal vias as well as the significant via parameters of the thermal resistance path, thermal performances with one via, two vias as well as multiple vias will be discussed based on numerical analysis approaches.

#### 3.2.1. PCB Substrate with One Individual Thermal Via

Fig.3-1 depicts a typical structure of a single via. To simplify the analysis process, it is postulated that the individual via has isothermal boundary conditions on its top and bottom and adiabatic condition on its surrounding surfaces. Here,  $e_i$  ( $mm$ ) ( $i = 1,2,3$ ) represents the thickness of each layer, and  $\sigma_i$  ( $W/mK$ ) is the corresponding thermal conductivity.  $D$  ( $mm$ ) stands for the via diameter.  $Pl_a$  ( $mm$ ) is the plating thickness of thermal via. The thermal resistance of each layer  $R_{th,i}$  ( $K/W$ ) can be obtained by (1.4-11).

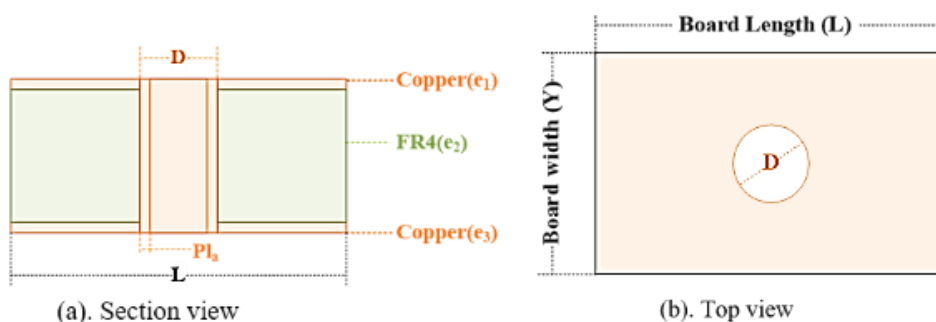


Fig.3-1. Typical PCB structure with a single thermal via

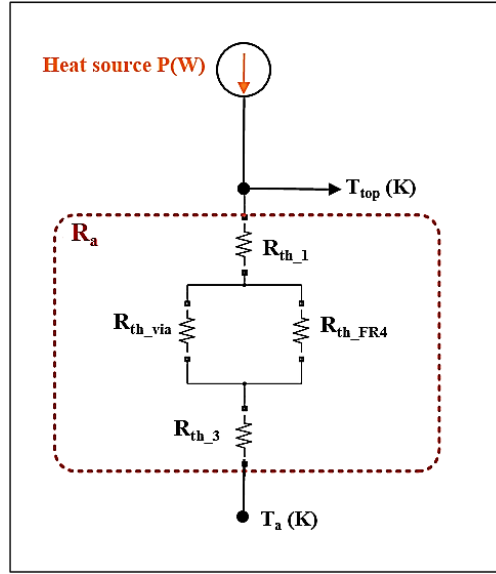


Fig.3-2. Analytical model for one single via PCB structure

The analytical thermal model for the one single via structure has been drawn in Fig.3-2 by the analogy between thermal path and electrical circuit. Based on the 1D heat conduction assumption, the thermal via is considered in parallel with the remaining FR4 material in the second layer. So, the thermal resistance of each part of the structure can be obtained by equations (3.2-1)(3.2-2)(3.2-3).

$$R_{board} = \frac{e_2}{\sigma_2 \cdot S_1} \quad (3.2-1)$$

$$R_{th\_via} = \frac{e_2}{\sigma_1 \cdot (\pi \cdot D \cdot Pl_a)}, R_{th\_FR4} = \frac{e_2}{\sigma_2 \cdot (S_1 - \frac{\pi \cdot D^2}{4})} \quad (3.2-2)$$

$$R_a = R_{th\_2} = \frac{1}{\frac{1}{R_{th\_via}} + \frac{1}{R_{th\_FR4}}} = \frac{R_{board}}{1 + \frac{\pi \cdot D^2}{S_1} \cdot (\sigma_r \cdot \frac{2 \cdot Pl_a}{D} - \frac{1}{2})}, \text{ with } \sigma_r = \frac{\sigma_1}{\sigma_2} \quad (3.2-3)$$

where,  $R_{board}$  ( $K/W$ ) is the thermal resistance of the PCB substrate without any vias;  $R_a$  ( $K/W$ ) stands for the total thermal resistance of the PCB structure with one single via;  $R_{th\_2}$  ( $K/W$ ) is the thermal resistance of the FR4 substrate with one single via;  $S_1$  ( $mm \times mm$ ) is the heat across area or the pad surface on the PCB substrate equaling to  $L \times Y$  ( $mm \times mm$ ). Here,  $R_a$  equals to  $R_{th\_2}$  since that  $R_{th\_1}$  and  $R_{th\_3}$  (thermal resistances of the copper plates, see Fig.3-1 and Fig.3-2) can be omitted because of the small thickness value of the copper layers, for example,  $35 \mu m$  for standard PCB. And (3.2-2) can be used to calculate the approximated thermal resistance of the thermal vias when  $Pl_a$  is far less than  $D$ .

As we can see in Fig.3-1 and Fig.3-2, for the substrate with one single thermal via, the significant via parameters related to its thermal resistance include via diameter  $D$  ( $mm$ ), via plating thickness  $Pl_a$  ( $mm$ ) and pad surface of PCB substrate  $S_1$  ( $mm \times mm$ ).

### 3.2.2. PCB Substrate with Two Thermal Vias

In the case of two thermal vias in PCB substrate, one more parameter is needed to be considered as shown in Fig.3-3: the pitch distance  $H_d$  ( $mm$ ) between two thermal vias. As  $H_d$  is usually smaller than  $1 mm$ . Analytical thermal model corresponding to this structure by analogy to electrical circuit is drawn in Fig.3-4.

In the same way as for the one thermal via case, the two thermal vias and the remaining FR4 substrate are in parallel according to the 1D heat conduction assumption. It is postulated that the two-vias structure has isothermal boundary conditions on its top and bottom and

adiabatic condition on its surrounding surfaces. Thus, the influence of the pitch distance  $H_d$  is neglected by omitting the lateral conduction effect. Then the thermal resistance of the total PCB substrate  $R_a$  can be obtained by (3.2-4)(3.2-5)(3.2-6). Impact of the pitch distance  $H_d$  will be analyzed in the case of multiple vias.

$$R_{th\_via\_2} = \frac{e_2}{\sigma_1 \cdot 2 \cdot (\pi \cdot D \cdot Pl_a)} , R_{th\_FR4\_2} = \frac{e_2}{\sigma_2 \cdot (S_1 - 2 \cdot \frac{\pi \cdot D^2}{4})} \quad (3.2-4)$$

$$R_{a\_2} = R_{th\_2} = \frac{1}{\frac{1}{R_{th\_via\_2}} + \frac{1}{R_{th\_FR4\_2}}} \quad (3.2-5)$$

$$R_{a\_2} = \frac{R_{board}}{1 + \pi \cdot \frac{D^2}{S_1} \cdot (\sigma_r \cdot \frac{2 \cdot Pl_a}{D} - \frac{1}{2})} \quad (3.2-6)$$

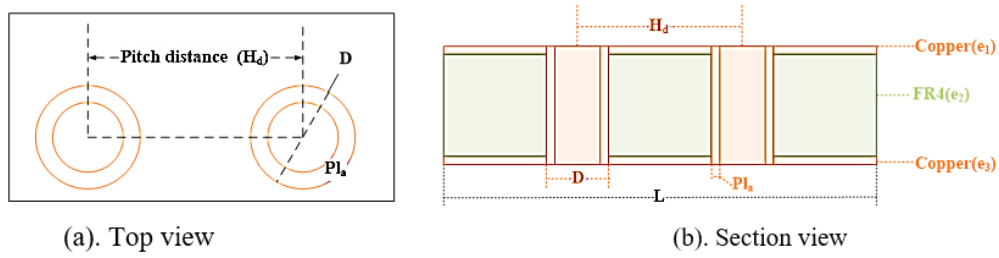


Fig.3-3. Top and Section view of the PCB substrate with two thermal vias

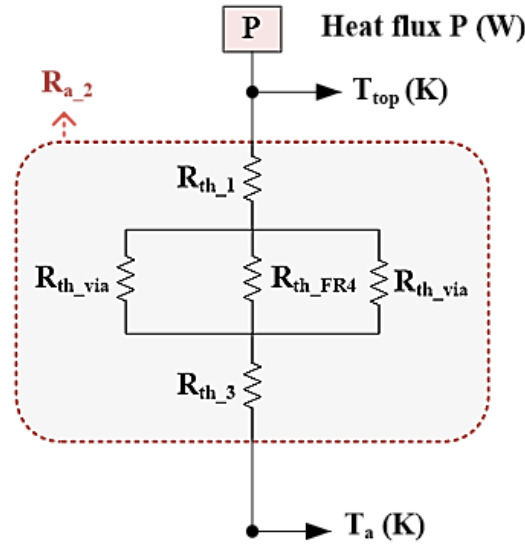


Fig.3-4. Analytical thermal model for PCB structure with two thermal vias

### 3.2.3. PCB Substrate with Multiple Vias

After figuring out the significant via parameters according to the cases where PCB substrates have one and two thermal vias, it is much easier to analyze the common case with multiple thermal vias. As shown in Fig.3-5, via-cluster is formed by multiple vias, each individual via would function separately. In other words, all thermal vias are considered as parallel thermal resistances based on the 1D heat conduction assumption. Two typical sketches of multiple-via pattern are presented in Fig.3-6. The difference between these two patterns is related to the higher via design density allowed by pattern 2.

To simplify the analysis procedure, it is assumed that there are  $N$  ( $m \times n$ :  $m$  rows,  $n$  columns) thermal vias with a pitch distance  $H_d$  between each other and these vias form a via-cluster area  $L_{via} \times Y_{via}$  ( $mm \times mm$ ), with via-cluster length  $L_{via}$  equivalent to  $n \times H_d$  and via-

cluster width  $Y_{via}$  equivalent to  $m \times H_d$ . It is postulated that this multiple-via structure has isothermal boundary conditions on its top and bottom and adiabatic condition on its surrounding surfaces.

The total thermal resistance  $R_{a\_N}$  (K/W) of the PCB substrate is then obtained by following equations.

$$R_{th\_via\_N} = \frac{e_2}{\sigma_1 \cdot N \cdot (\pi \cdot D \cdot Pl_a)} , R_{th\_FR4\_N} = \frac{e_2}{\sigma_2 \cdot (S_1 - N \cdot \frac{\pi \cdot D^2}{4})} \quad (3.2-7)$$

$$R_{a\_N} = \frac{1}{\frac{1}{R_{th\_via\_N}} + \frac{1}{R_{th\_FR4\_N}}} \quad (3.2-8)$$

$$R_{a\_N} = \frac{R_{board}}{1 + \pi \cdot \sigma_r \cdot \frac{D}{H_d} \cdot \frac{Pl_a}{H_d} \cdot \frac{L_{via} \times Y_{via}}{L \times Y} - \frac{1}{4} \cdot \pi \cdot \frac{D^2}{H_d^2} \cdot \frac{L_{via} \times Y_{via}}{L \times Y}} \quad (3.2-9)$$

According to (3.2-9), it is complex to analyze the influences of all significant parameters independently. Therefore, it is proposed to normalize these via parameters in dimensionless form as shown in (3.2-10) and (3.2-11).

$$R_{oa} = \frac{1}{1 + \pi \cdot R_{o1} \cdot R_{o2}^2 \cdot \left( \sigma_r \cdot \frac{R_{o3} - 1}{R_{o2}} \right)} \quad (3.2-10)$$

$$R_{oa} = \frac{R_{a\_N}}{R_{board}} , R_{o1} = \frac{N \cdot H_d^2}{S_1} , R_{o2} = \frac{D}{H_d} , R_{o3} = \frac{Pl_a}{H_d} \quad (3.2-11)$$

where  $R_{oa}$  is the ratio of  $R_{a\_N}$  to  $R_{board}$ ;  $R_{o1}$  is the ratio of the via-cluster surface to the total available board area;  $R_{o2}$  is the ratio of via diameter  $D$  to the pitch distance  $H_d$ ;  $R_{o3}$  is the ratio of the plating thickness of copper  $Pl_a$  to the pitch distance  $H_d$ ;  $S_1$  is the total board surface normal to the heat transfer direction  $L \times Y$ ;  $\sigma_r$  is the ratio of thermal conductivity of copper to that of FR4; Therefore, the ratio of  $R_{oa}$  is the objective function in via design optimization.

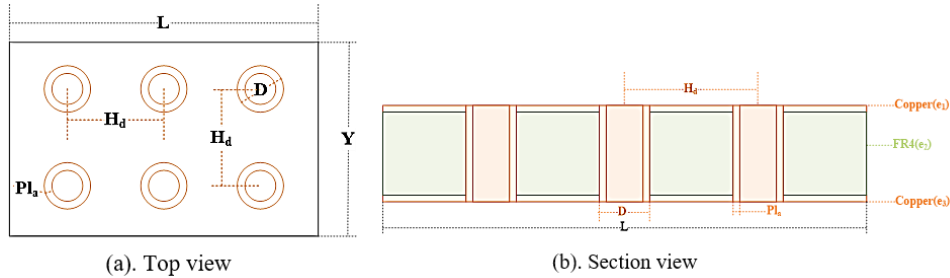


Fig.3-5. Top and section view of the PCB substrates with multiple thermal vias in pattern 1

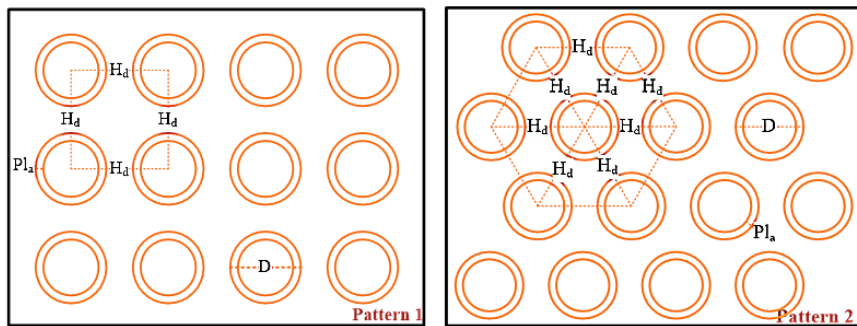


Fig.3-6. Two typical via-cluster patterns

As we can see in (3.2-10), the value of  $R_{oa}$  is within the range from 0 to 1. And an increase of  $R_{oa}$  means the augmentation in thermal resistance. Equation (3.2-10) also involves that

increase of ratios  $R_{o1}$ ,  $R_{o2}$ ,  $R_{o3}$  leads to a reduction of  $R_{oa}$  and, therefore, of the equivalent thermal resistance of the PCB substrate with multiple vias  $R_{a_N}$ .

In addition, it can be noticed that the absolute value of via design parameters is no longer critical because of their dimensionless normalized form. This means that the significant issue of thermal via design regarding their thermal behavior mainly depends on the vias arrangement in the via-cluster, which is related to their formed via pattern and via-cluster surface.

Theoretical analysis of the PCB substrate with thermal vias provides us concise form of the relationships between its total thermal resistance and the different via design parameters. Evolution of the equivalent thermal resistance ratio  $R_{oa}$  with the via parameters and the cooling effects of this solution with thermal vias will be discussed in next part.

### 3.3. 3D FEM ANALYSIS

In fact, 1D analytical thermal models can offer a fast estimation of the cooling effect tendency, but they have limitations in terms of accuracy because of the 1D hypothesis about the heat conduction dimensions as well as the omitted heat convection effect. In this section, cooling effects with thermal vias in the PCB substrates have also been analyzed in steady state by 3D FEM analysis. Analytical thermal resistances of different PCB substrates will be compared to the results obtained by 3D FEM simulations. The purpose is to identify the influences of different via parameters and also to figure out the model errors between the two methods.

All thermal simulations are based on the PCB assembly shown in Fig.3-7. A Silicon chip is attached to the PCB substrate and the chip is considered as the heating source. Multiple thermal vias will be created in the FR4 substrate to evaluate their cooling effect. Dimension parameters and material properties used for thermal simulations are listed in Table 3.1. For all thermal simulations, the heat flux  $P$  is supposed to be  $1W$  and the bottom of the PCB substrate is supposed to be attached to a heat sink, the convection heat transfer coefficient between the module surface and the ambient equals  $15 W/(m^2K)$ , and the ambient temperature  $T_a$  is  $20\text{ }^\circ\text{C}$ .

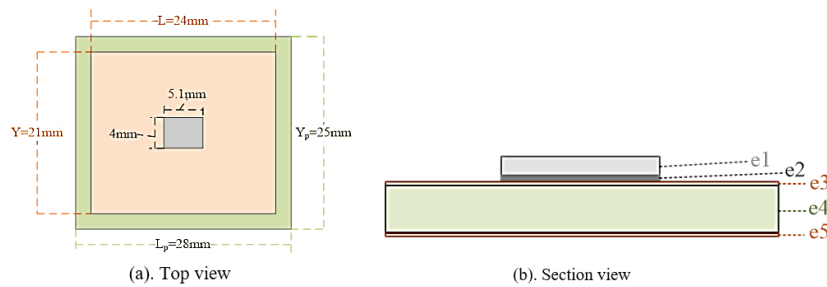


Fig.3-7. Top and Section view of the studied PCB assembly

Table 3.1. Dimensions of the assembly and material properties

Layer	Material	Layer thickness ( $\mu\text{m}$ )	Vertical heat cross area ( $\text{mm} \times \text{mm}$ )	Thermal conductivity $\text{W}/(\text{mK})$
Chip	Silicon	$e_1=245\mu\text{m}$	$S_c = 5.1 \times 4$	130
Solder	62Sn-36Pb-2Ag	$e_2=75\mu\text{m}$	$S_c$	50
Top-PCB	Copper	$e_3=38\mu\text{m}$	$S_1 = 24 \times 21$	400
PCB	FR4	$e_4=0.7\text{mm}$	$S_2 = 28 \times 25$	0.3
Bottom-PCB	Copper	$e_5=38\mu\text{m}$	$S_2$	400

Multiple thermal vias are created beneath the chip. Influences of normalized via parameters including the ratio of via-cluster surface  $R_{o1}$ , the ratio of via diameter  $R_{o2}$ , the ratio of via plating thickness  $R_{o3}$ , the number of thermal vias  $N$  as well as the via pattern will be discussed in following parts. In the following sections, the available pad surface is assumed to be  $S_c$  and the thermal vias are created right beneath the chip component.

### 3.3.1. Number of Thermal Vias $N$

According to the normalized form described in (3.2-10), the thermal resistance of the PCB substrate should be constant when the ratios of  $R_{o1}$ ,  $R_{o2}$  and  $R_{o3}$  are all kept at certain values. Both 1D electro-thermal and 3D FEM analysis have been carried out to verify this prediction with  $R_{o1}$  equaling to 0.8,  $R_{o2}$  equaling to 0.8 and  $R_{o3}$  equaling to 0.1. In other words, the via-cluster surface is 80 % of the pad surface for the Si chip  $S_c$ ; the via diameter  $D$  is 80 % of the pitch distance  $H_d$  and the via plating thickness is 10 % of the pitch distance  $H_d$ . Values of  $H_d$  and number of vias  $N$  used for creating different thermal models are summarized in Table 3.2.

Table 3.2. Pitch distance and number of vias for different thermal models

$H_d$ (mm)	0.369	0.452	0.583	0.683	0.738	0.825	0.903	1.166
$N$	120	80	48	35	30	24	20	12

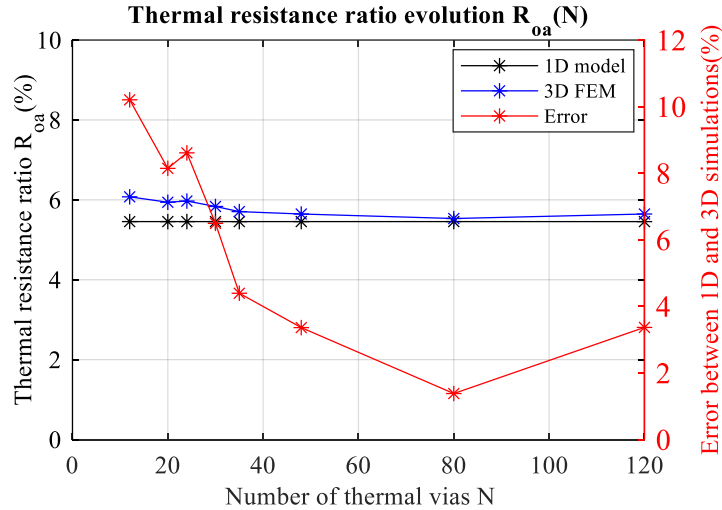


Fig.3-8. Evolution of thermal resistance ratio  $R_{oa}$  following the number of vias

Thermal vias are beneath the chip. Fig.3-8 depicts the impact of the number of thermal vias  $N$  on the 1D thermal resistance model. In all these configurations, the theoretical thermal resistance is constant. 3D FEM simulations have also been realized for 3D models with different number of vias but with the same via-cluster area to maintain the same via geometric ratios. For example, thermal performances of assemblies with different number of vias are shown in Fig.3-9. It is noted that the same cooling effect with different thermal vias ( $N=12$  and  $N=80$ ) can be achieved when they have fixed via geometric ratios.

It is discovered that the difference between the 3D FE and 1D thermal simulations is lower than 7 % when  $N$  is more than 35. This means that, for such configuration, the 1D heat conduction assumption is valid and gives results similar to 3D FEM simulations. In general, this will be the case when the via-cluster surface is relatively large in comparison with the diameter of thermal vias. Besides, the main error between the 1D thermal resistance networks and the 3D FE models is due to the finite lateral thermal conduction of the top copper layer. In the 1D models, the heat spreading effect over the copper layer has been omitted. In 3D FEM cases, the heat source is localized in the Si chip and the heat flux

laterally spread over the PCB surface by the top copper layer. The finite thermal conduction of the top copper layer leads to a difference between the two models.

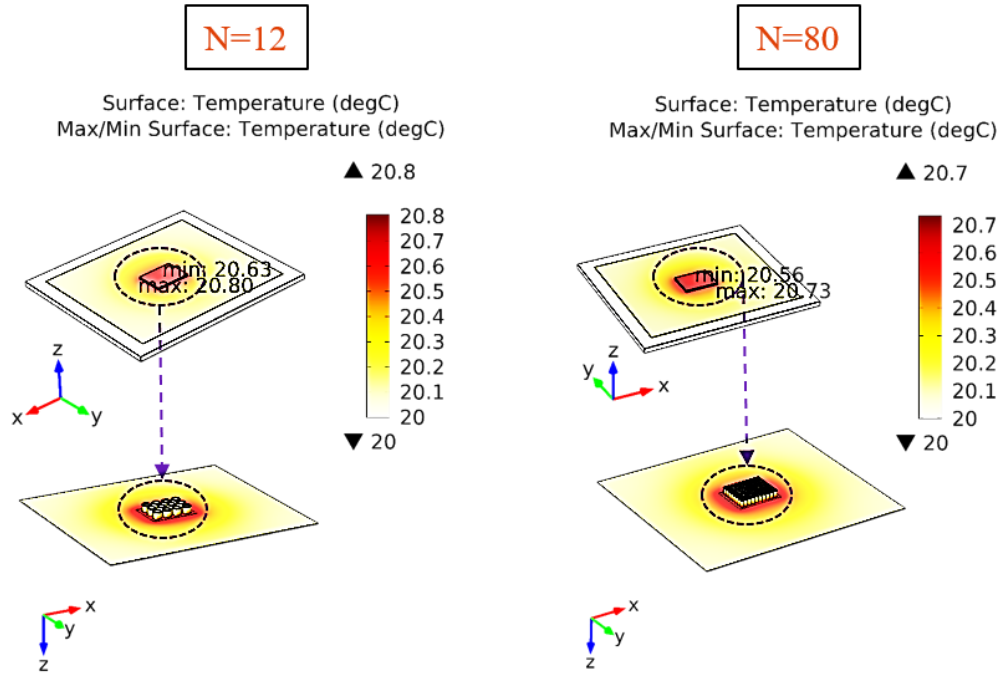


Fig.3-9. 3D FEM simulations with different number of thermal vias but the same ratios of  $R_{o1}$ ,  $R_{o2}$ ,  $R_{o3}$

### 3.3.2. Via-Cluster Surface Ratio $R_{o1}$

Then,  $R_{o2}$  (0.8) and  $R_{o3}$  (0.1) are fixed to observe the impact of via-cluster surface  $R_{o1}$ . Different via parameters applied to create the 3D models are listed in Table 3.3. Thermal vias are created beneath the chip component.

Table 3.3. Via parameters used to create different 3D FE models

Via Parameters		$H_d$ (mm) ( $D < H_d < L-D$ )	$N$ ( $m \times n, m \leq \frac{Y}{H_d}, n \leq \frac{L}{H_d}$ )	$R_{o1}$ (%)
$D$ (mm), $R_{o2} = 0.8$	$Pl_a$ (mm), $R_{o3} = 0.1$			
0.40	0.05	0.50	8×10	98.04
0.64	0.08	0.80	5×6	94.12
0.376	0.047	0.47	8×10	86.63
0.464	0.058	0.58	6×8	79.15
0.536	0.067	0.67	5×7	77.02
0.688	0.086	0.86	4×5	72.51
0.824	0.103	1.03	3×4	62.41
1.072	0.134	1.34	2×3	52.81
1.608	0.201	2.01	1×2	39.61

Evolution of the thermal resistance ratio  $R_{oa}$  following  $R_{o1}$  is presented in Fig.3-10. We can see that the thermal resistance ratio  $R_{oa}$  decreases dramatically in the range  $0 < R_{o2} < 40\%$ , and then, the curves level off. The via-cluster surface formed by multiple vias should be as large as possible. This can be obtained by increasing the number of vias  $N$  for the same pitch distance or by increasing the pitch distance  $H_d$  while maintaining the ratios of  $R_{o2}$  and  $R_{o3}$ , this means increasing the size of the vias proportionally to the pattern surface increase.



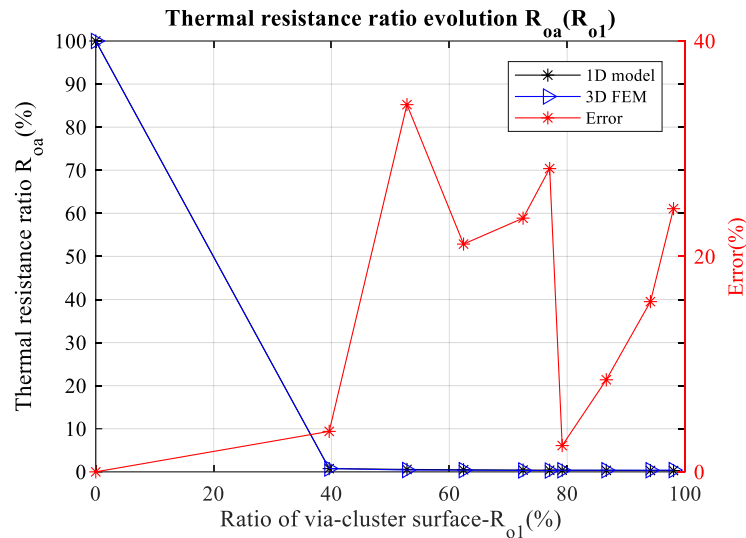


Fig.3-10. Evolution of thermal resistance ratio  $R_{0a}$  following the ratio of via-cluster surface  $R_{01}$

### 3.3.3. Via Diameter Ratio $R_{02}$

Influences of the via diameter have been simulated with fixed via-cluster surface ratio  $R_{01}$  (0.8) and also fixed plating thickness ratio  $R_{03}$  (0.1). Evolution of the total thermal resistance of the PCB substrate is presented in Fig.3-11. The curve giving the evolution of the  $R_{0a}$  as a function of via diameter ratio decreases dramatically in the range  $0 < R_{02} < 30\%$ , then, the tendency levels off. Obviously, the thermal resistance of the PCB substrate becomes smaller when the ratio of the via diameter increases.

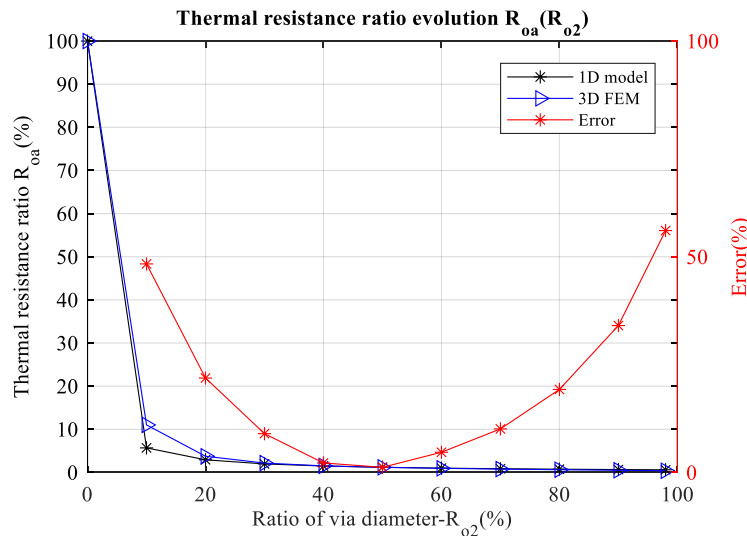


Fig.3-11. Evolution of thermal resistance ratio  $R_{0a}$  following the ratio of via diameter  $R_{02}$

### 3.3.4. Via Plating Thickness Ratio $R_{03}$

In this part, the via-cluster surface ratio  $R_{01}$  (0.8) and the via diameter ratio  $R_{02}$  (0.8) are fixed, via plating thickness ratio  $R_{03}$  ( $0 < R_{03} < 0.5 \times R_{02}$ ) is changed to observe its influences on the thermal performances.

As we can see in Fig.3-12, the plating thickness has also a huge influence on the thermal resistance, especially when the ratio  $R_{03}$  is lower than 10%. For example, Fig.3-13 depicts the 3D thermal simulation results of the structure when  $R_{03}$  equals 0 and 0.31, respectively. Thermal vias should be filled as much as possible.

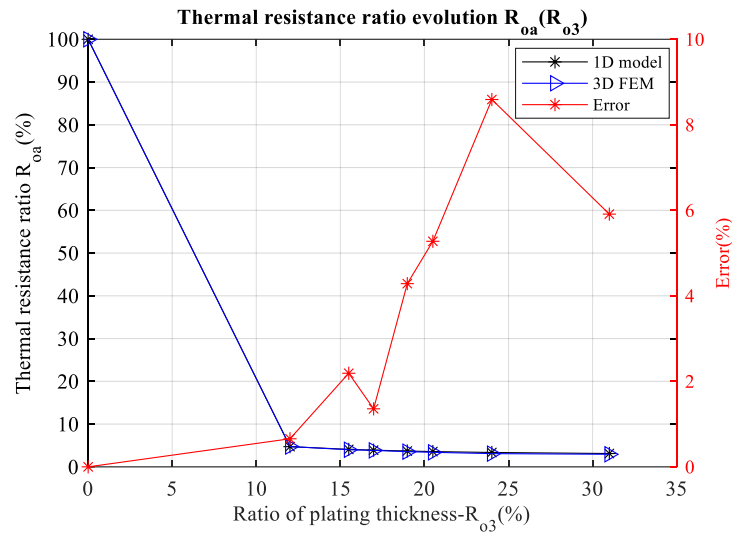


Fig.3-12. Evolution of thermal resistance ratio  $R_{0a}$  following the ratio of via plating thickness  $R_{03}$

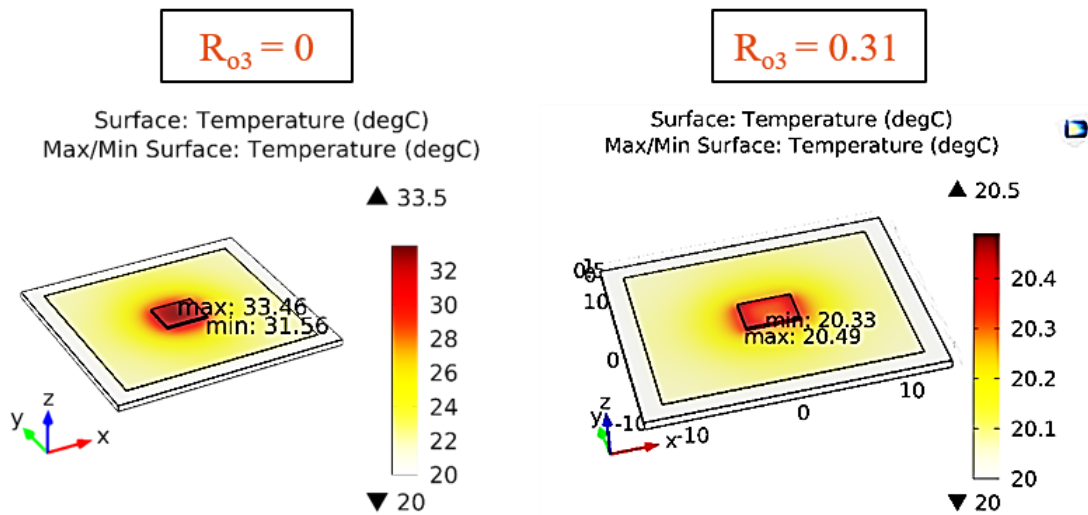


Fig.3-13. 3D FEM simulations with different ratio of via plating thickness

### 3.3.5. Via Pattern

Fig.3-6 describes two typical via patterns formed by multiple vias. As previously mentioned, their difference lies in the number of vias for the same via parameters of via-cluster surface, via diameter and via plating thickness. It has been demonstrated in part 3.3.1 that the cooling effect while increasing the number of thermal vias  $N$  is almost the same if via parameters  $R_{01}$ ,  $R_{02}$ ,  $R_{03}$  remain the same. For example, Fig.3-14 depicts the 3D thermal simulation results for two models created with the two different patterns. We can note that the temperature distributions are similar.

In fact, pattern 2 can make fill a large part of the available via-cluster surface  $L_{via} \times Y_{via}$  as shown in Fig.3-15. Besides, to simplify the theoretical analysis, the via-cluster surface of the two patterns is assumed to be  $N_{pattern1} \times H_d^2$ . But it exists a deviation between the real via-cluster surface formed by multiple vias and the assumed one. That means that the real via-cluster surface of pattern 2 ( $\frac{\sqrt{3}}{2} N_{patter2} \times H_d^2 + \frac{\sqrt{3}}{4} \times m_{pattern2} \times H_d^2$ ) is larger than that of pattern 1. For example, pattern 2 in Fig.3-15 ( $N=42$ ) has a real via-cluster surface ratio  $R_{01}$  of 85.73%. By contrast, pattern 1 in Fig.3-15 ( $N=35$ ) has a via-cluster surface ratio of 77%.

This explains the cooling effect difference between the two patterns shown in Fig.3-16. Therefore, pattern 2 is preferred for its slightly better cooling effect related to a higher number of vias for a given via-cluster surface.

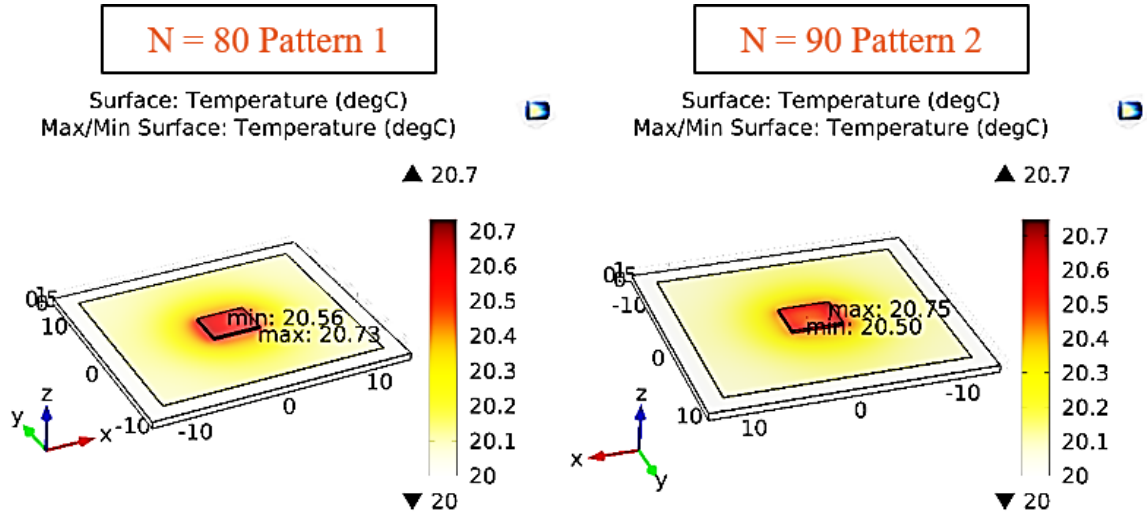


Fig.3-14. 3D FEM simulations with different via patterns

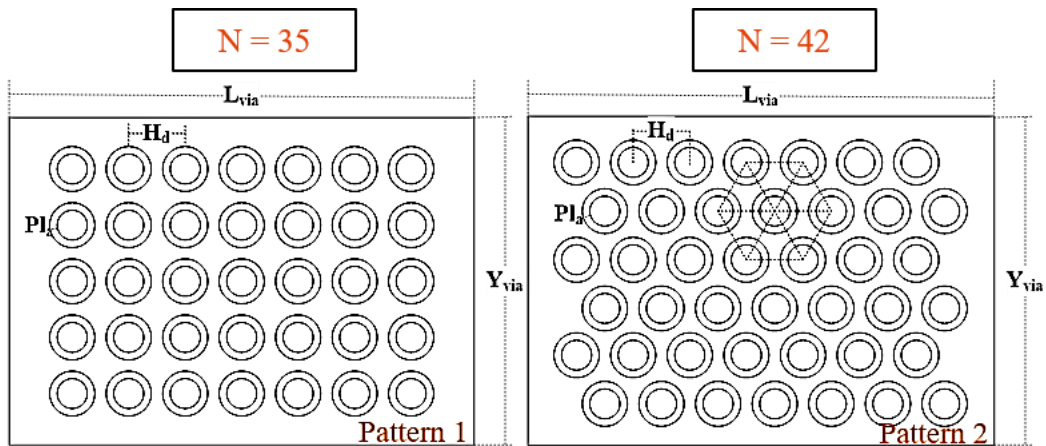


Fig.3-15. Arrangement of thermal vias in two patterns with the same available via-cluster surface

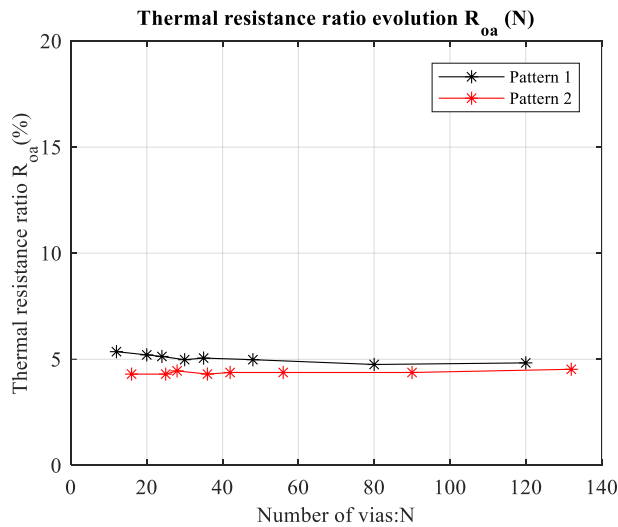


Fig.3-16. Evolution of the average thermal resistance ratio in two patterns

In a word, the creation of thermal vias in the PCB substrate should be optimized with larger geometric ratios of via parameters such as via-cluster surface, via diameter, via plating thickness. Thermal resistance from the proposed 1D model is correlated with the results obtained from the 3D FEM analysis. Besides, though without satisfactory accuracy of the 1D models, the emphasis at layout design stage is to know the design direction within a short time.

### 3.3.6. Copper Thickness on The PCB Substrate

PCB substrate has been chosen for its better electrical properties and mechanical soundness compared to DBC. But DBC substrate has much better thermal performance. In order to be competitive with DBC, one solution is to increase the PCB copper thickness  $e_c$  (mm) on the top layer in order to increase heat spreading. For comparison purpose, 3D models with a chip attached to PCB or DBC substrate are created as shown in Fig.3-17.



Fig.3-17. Section view of the 3D model for DBC or PCB structure

For DBC ( $\text{Al}_2\text{O}_3$ ) substrate, the available ceramic thickness range is:  $0.25 \sim 1.00\text{mm}$  and the corresponding breakdown voltages are in the range:  $2.5 \sim 10\text{kV}$ . The available copper thickness on DBC substrate are in the range:  $0.127 \sim 0.4\text{mm}$  [164]. For the same breakdown voltages, PCB (FR4) substrates are thinner:  $0.046 \sim 0.185\text{mm}$  as FR4 has a higher breakdown voltage (FR4:  $54\text{kV/mm}$ ,  $\text{Al}_2\text{O}_3$ :  $10 \sim 15\text{kV/mm}$ ). Usually, the standard PCB substrate has a copper thickness of  $35\mu\text{m}$  or  $38\mu\text{m}$ .

Using the material properties in Table 3.1, simulations have been carried out to identify the effects of increasing copper thickness. A heat dissipation of  $1\text{W}$  was used for the chip, and an equivalent convection heat-transfer coefficient of  $15\text{ W}/(\text{m}^2\text{K})$  from all external surfaces (except the bottom layer) to the ambient was applied. The bottom copper layer is assumed to be attached to heat sink, and the ambient temperature is supposed to be  $20\text{ }^\circ\text{C}$ . The thermal resistance evolution versus the top layer copper thickness is presented in Fig.3-18 for DBC and PCB substrates. As shown in this figure, the thermal resistance  $R_{thc}$  (K/W) of the PCB assembly is much higher than that of DBC. But, it can be noticed that the thermal resistance depends a lot on the copper thickness, especially in the range of  $35\mu\text{m} < e_c < 300\mu\text{m}$ . On the other hand, increasing DBC copper thickness is not as efficient. The reason of such fast decrease for PCB structures can be explained from the results shown in Fig.3-19. Due to the huge difference of thermal conductivity between FR4 and copper, the lateral heat flux is reinforced in the copper layer before it crosses vertically through the FR4 layer. This spreading effect of a thicker top copper layer reduces a lot the thermal resistance of the structure.

However, despite this improvement, PCB cannot compete with DBC technology regarding the thermal performances, for the same breakdown voltage. Therefore, the method of double-sided cooling by combining the effects of thermal vias and the use of thick copper layer has been proposed as shown in Fig.3-20. As previously, a heat dissipation of  $1\text{W}$  was used for the chip, and an equivalent convection heat-transfer coefficient of  $15\text{ W}/(\text{m}^2\text{K})$  from all external surfaces (except the bottom layer) to the ambient was applied. The bottom copper layer is assumed to be attached to heat sink, and the ambient temperature is supposed to be  $20\text{ }^\circ\text{C}$ . And the thermal simulation results for such design are presented in Fig.3-21. As we can see in Fig.3-21, the double-sided cooling method is only effective when the top copper layer is attached to a heat sink. However, in practical implementation, adding a heat sink to the top layer is difficult as this layer should be dedicated to decoupling capacitors and to

drivers that have both to be placed close to the power semiconductor device. This is especially required in case of GaN technology, for example.

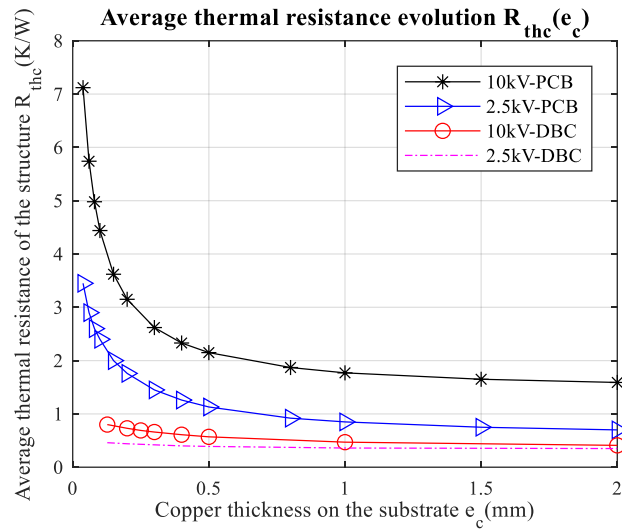
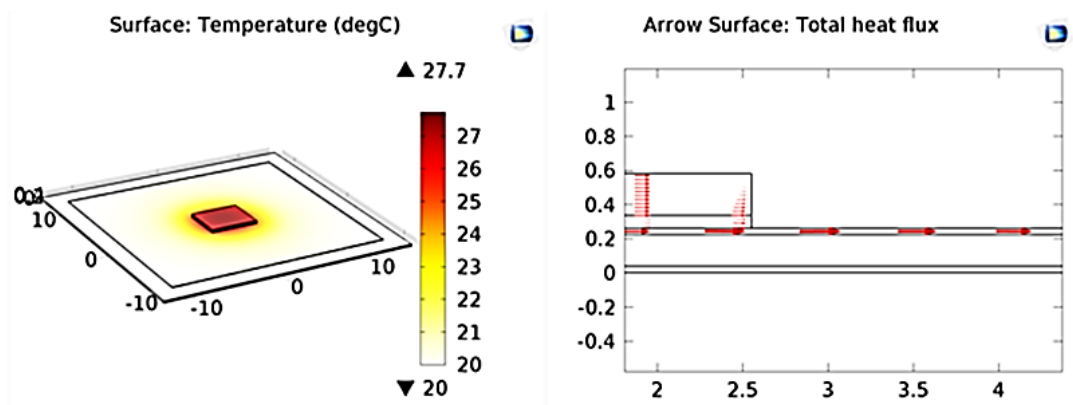
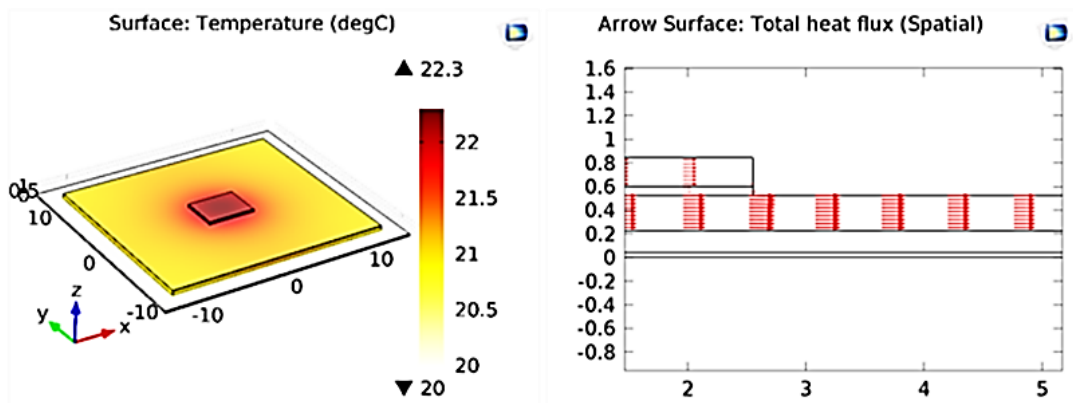


Fig.3-18. Thermal resistance evolution following the copper thickness



(a). Copper thickness  $e_c = 38 \mu\text{m}$  and section view of heat flux



(b). Copper thickness  $e_c = 300 \mu\text{m}$  and section view of heat flux

Fig.3-19. 3D thermal simulation results for PCB structures having 10kV breakdown voltage

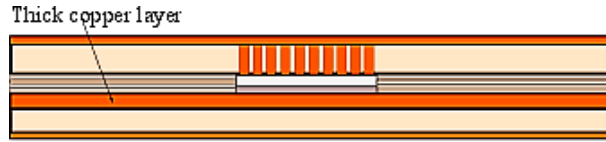


Fig.3-20. Structure of double-sides cooling solution for the PCB

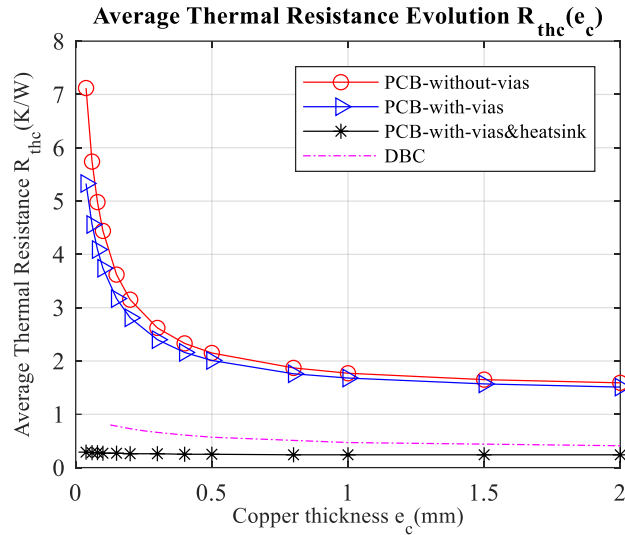


Fig.3-21. Thermal resistance evolution following the copper thickness for the same breakdown voltage 10kV

### 3.4. EXPERIMENTAL RESULTS AND DISCUSSIONS

In this part, experimentations have been carried out to validate previous simulation predictions of the thermal via design. As shown in Fig.3-22, four models of the PCB structures with different thermal vias have been fabricated to demonstrate the cooling performances of thermal vias. A heating resistor ( $7.87\text{ mm} \times 8.51\text{ mm} \times 0.81\text{ mm}$ ) is attached to the PCB substrate. Thermal vias are placed below the heating resistor. Physical dimensions of the PCB substrate and via parameters are presented in Fig.3-23.

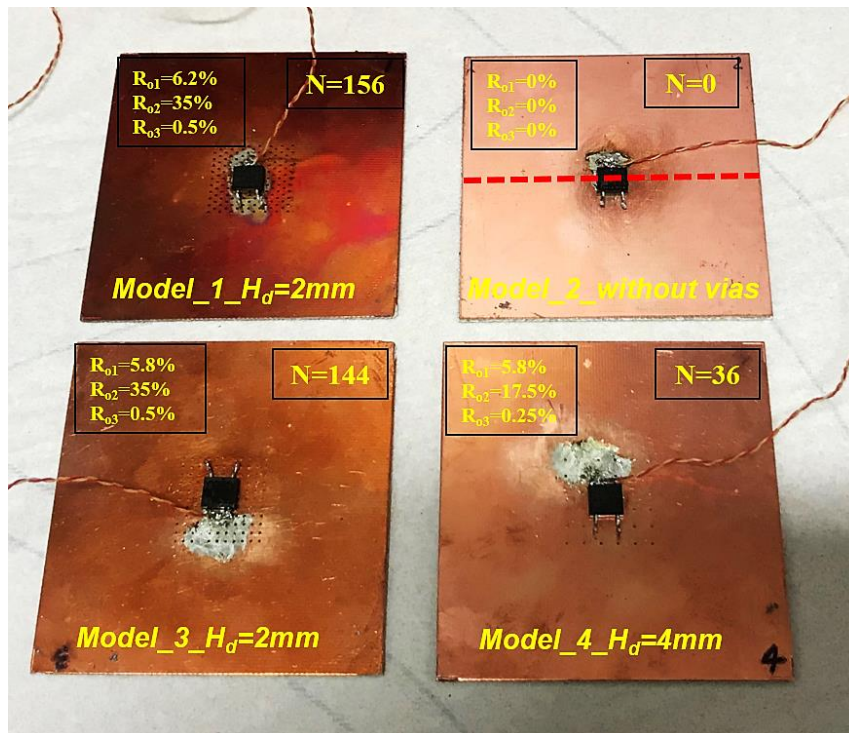


Fig.3-22. Four PCB structures with different via patterns

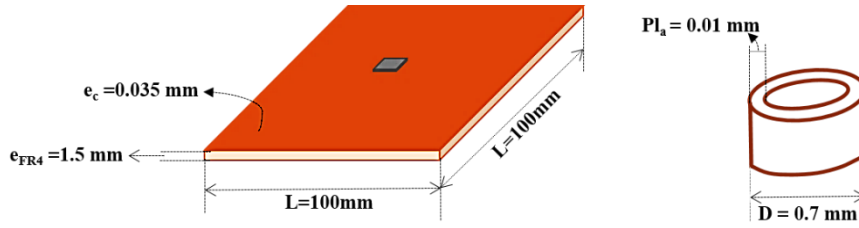


Fig.3-23. PCB dimensions and via parameters

Firstly, 3D FEM models have been created according to the real PCB structures with different via parameters. Differences between the four models are related to the pitch distance  $H_d$ , the number of vias  $N$ , and the formed via-cluster surface. 3D thermal simulations are calculated with COMSOL Multiphysics. Material properties in Table 3.1 have been applied for the 3D FEM simulations. Simulation results are presented in Fig.3-24. A heat dissipation of  $10\text{ W}$  is applied in the heating resistor, the bottom copper layer of the PCB is assumed to be attached to a heat sink, and the ambient temperature is supposed to be constant at  $20\text{ }^\circ\text{C}$ . Here, model\_2 without any thermal vias is considered as the reference for cooling effects comparisons.

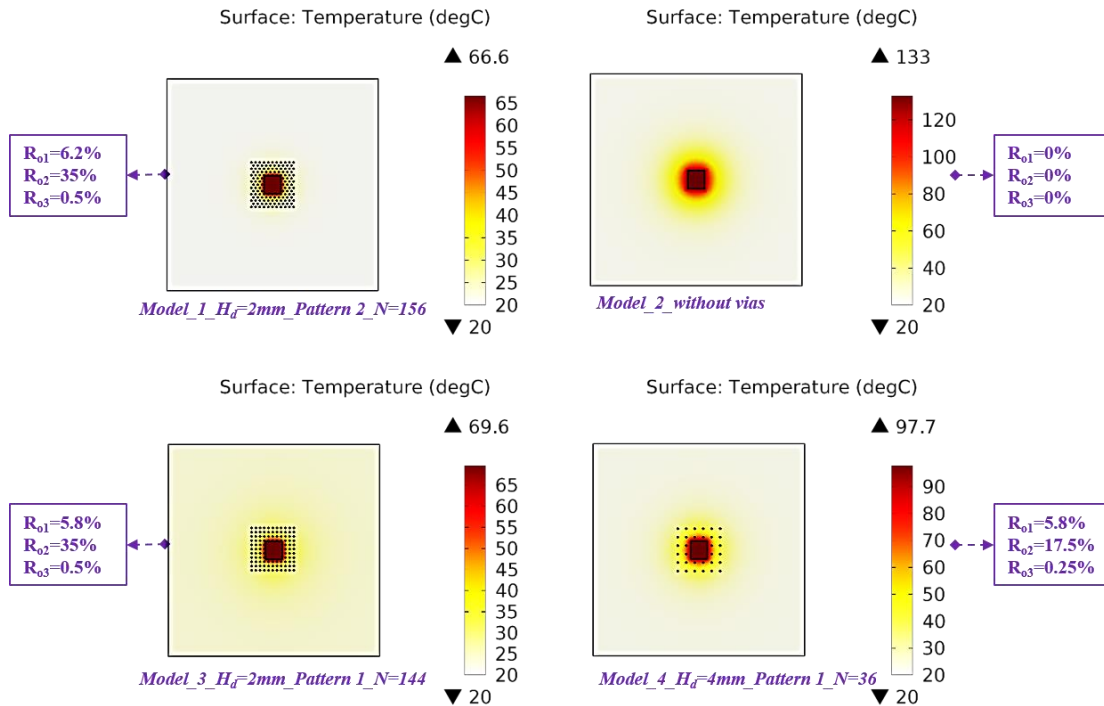


Fig.3-24. 3D FEM simulations for PCB structures with different via parameters

According to the relationship between temperature and thermal resistance described previously in (1.4-11), equivalent thermal resistances of PCB substrates  $R_{thsim}$  ( $^\circ\text{C}/\text{W}$ ) for each model could then be obtained:  $0.164\text{ }^\circ\text{C}/\text{W}$  for model\_1 (156 vias in pattern 2);  $6.422\text{ }^\circ\text{C}/\text{W}$  for model\_2;  $0.467\text{ }^\circ\text{C}/\text{W}$  for model\_3 (144 vias in pattern 1);  $2.123\text{ }^\circ\text{C}/\text{W}$  for model\_4 (36 vias in pattern 1). Obvious thermal resistance reduction could be observed, which is already sufficient for many applications. Therefore, thermal vias could reduce the thermal resistance of the PCB structure by increasing the thermal conductivity of the PCB substrate. By comparing model\_1 to model\_3, it is found that cooling effect is better when more thermal vias could be created with larger via-cluster surface for the same available pad surface ( $S_I=10\text{cm} \times 10\text{cm}$ ), equivalent to larger  $R_{o1}$ . So, for limited space on the PCB substrate, pattern 2 with more thermal vias should be chosen. In addition, by comparing

model\_3 to model\_4, it is demonstrated that better cooling effect can be achieved when with larger ratio of via diameter  $R_{o2}$  and via plating thickness  $R_{o3}$ .

Then, the test bench introduced in Fig.2-1 has been used for power loss measurement in order to experimentally estimate the thermal resistance of the PCB substrates with thermal vias. As we can see in Fig.3-22, a thermocouple is soldered on the heatsink mounting tab of each heating resistor to measure its inner temperature  $T_{res}$  ( $^{\circ}C$ ). It is postulated that the mounting tab is uniform and isothermal. So the measurement error between the real inner temperature and that of the side mounting tab has been omitted because of the small distance ( $\sim 4\text{ mm}$ ) between them. The thermal resistance of the total system from the resistor base plate to the PT100 sensor of the duralumin column  $R_{thto}$  ( $^{\circ}C$ ) can be obtained based on (1.4-11). From this value, the thermal resistance of PCB substrate  $R_{thmes}$  ( $^{\circ}C/W$ ) can be calculated by (3.4-12).

$$R_{thmes} = R_{thto} - R_{thres} - R_{thTIM} - R_{thcol} \quad (3.4-12)$$

Where  $R_{thres}$  ( $^{\circ}C/W$ ) is the thermal resistance from the resistor element to the case of the heating resistor. This resistance equals to  $5.2\text{ }^{\circ}C/W$  according to the product datasheet [165];  $R_{thTIM}$  ( $^{\circ}C/W$ ) is the thermal resistance of TIM layer, equaling to  $0.02\text{ }^{\circ}C/W$  when PCB substrate has no thermal vias but equaling to  $0.16\sim 0.21\text{ }^{\circ}C/W$  respect to the four different via-cluster surface according to the thermal spreading effect;  $R_{thcol}$  ( $^{\circ}C/W$ ) is the thermal resistance of the duralumin column, equaling to  $0.225\text{ }^{\circ}C/W$ . And the thermal resistances of solder layer and copper layers are neglected because of their relatively small values. Details of each layer are summarized in Table 3.4.

Table 3.4. Dimensions and thermal properties of each layer for the PCB structures with thermal vias

Layer		Thickness (mm)	Heat cross section (mm×mm)	Thermal conductivity (W/mK)	Thermal resistance ( $^{\circ}C/W$ )
$R_{thTIM}$	Model_1 (N=156)	0.51	25×25	5 in Z direction	0.16
	Model_2 (N=0)		80×80		0.02
	Model_3 (N=144)		22×22		0.21
	Model_4 (N=36)		22×22		0.21
$R_{thcol}$ (Duralumin)		180	$\pi \times \left(\frac{88.45}{2}\right)^2$	130.45	0.225
Solder		0.030	7.87×8.51	50.9	--
Copper		0.038	100×100	400	--
$R_{thres}$ (Chip)		--	--	--	5.2

From 3D simulations, the temperature profile according to the distance from the heating resistance on the top copper layer along the red line (see Fig.3-22) were calculated. The results are presented in Fig.3-25 for each model. In these figures, the position of the heating resistor is at  $50\text{ mm}$  on the X-axis.

Compared to model\_2 (no via model), other models with thermal vias have highly reduced thermal resistance. As summarized in Table 3.5, the simulated results are in good agreement with experimental ones materialized by the temperature of the case of the heating resistor measured by the thermocouple. These results also validate previous analytical studies giving the thermal vias impact on the thermal equivalent resistances for the models with different via parameters ( $R_{o1}$ ,  $R_{o2}$ ,  $R_{o3}$ ).



Table 3.5. Comparisons between simulation and experimentation results

<b>R<sub>th</sub> of PCB</b>	<b>Model_1 (N=156)</b>	<b>Model_2 (N=0)</b>	<b>Model_3 (N=144)</b>	<b>Model_4 (N=36)</b>
R <sub>thmes</sub> (°C/W)	0.154	6.342	0.423	1.923
R <sub>thsim</sub> (°C/W)	0.164	6.423	0.467	2.123
Error	6.5%	1.3%	10%	10%

For further cooling effect improvements, one can fill the vias to reduce thermal resistance of the PCB substrate or increase the copper thickness  $e_c$  (mm) of the top PCB layer to improve the lateral heat flux dissipation.

However, using classical thermal vias will lead to lose the benefit of electrical insulation between the board and the heatsink. Today, one available solution is to use a kind of insulating glued joint realized either with special double-sides adhesive tape or by using a glue containing a small amount of glass balls. These balls ensure a well-defined thickness of the glue layer and insure reproducible thermal and electrical insulation properties. Thermally enhanced glue, filled, for example, with ceramic powder, are also available [118].

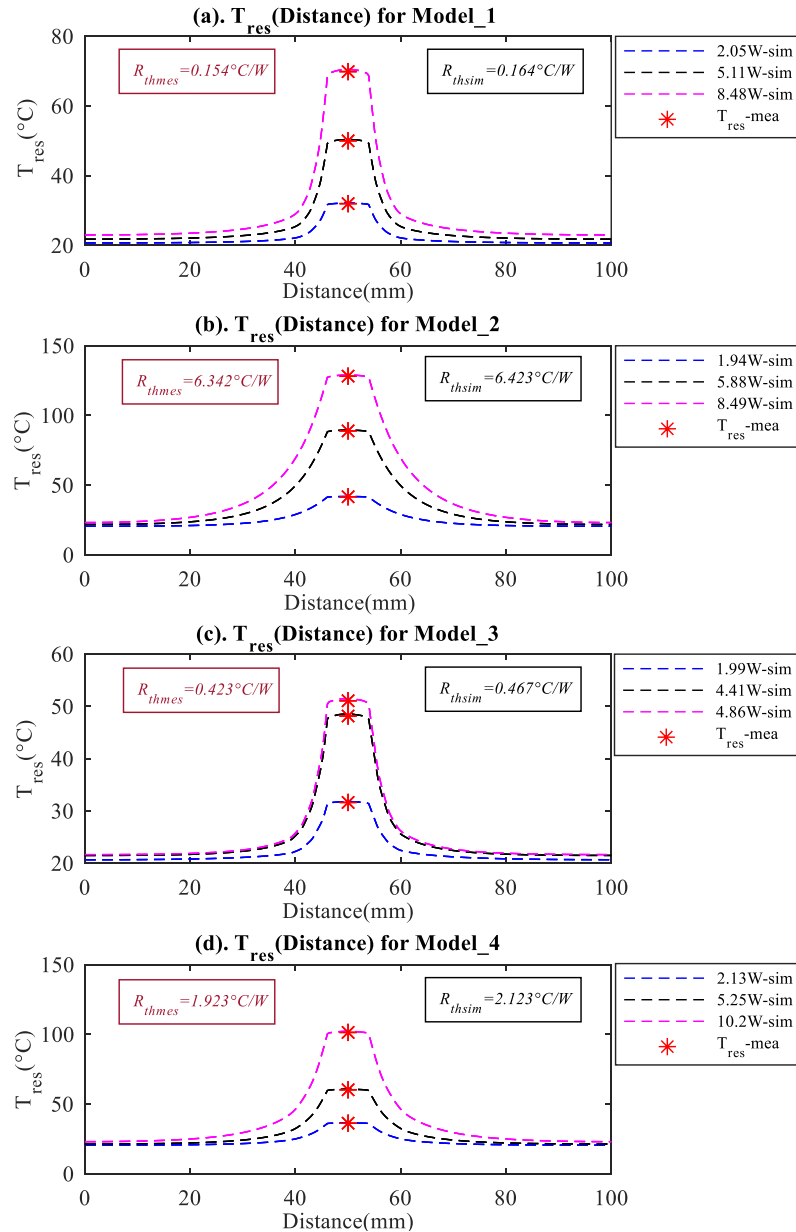


Fig.3-25. Temperature measurements of the heating source and comparisons with 3D FEM simulations

### 3.5. CONCEPTION OF THE INVERSE THERMAL MODEL

As previously mentioned, the calorimetric method used for power loss measurement takes a lot of time to stabilize the total thermal system. And the almost impossibility to measure the current under the penalty of adding parasitic inductances incompatible with the switching speeds of those WBG components. For this purpose, this part investigates the conception of the steady-state inverse heat conduction model (IHCM) developed from thermal simulations. The main objective is to derive the power dissipation in a chip, for example, GaN chip mounted on or embedded in a PCB from the surface temperature measured by infrared thermography or thermal sensors.

In this problem, the power devices losses are the solutions of the inverse problem of the temperature-to-power mapping. IHCM here is based on simple observations from real PCB structures with GaN chip embedded in PCB substrates. The error of the resultant power map with thermal noises is minimized by Least-Square Optimization, which transforms the direct inverse problem into a constrained optimization problem.

#### 3.5.1. Introduction

Inverse methods are defined as methods which allow to discover causes and unknown measureable variables by observing the consequences of a problem [166]. So IHCM is a possible approach to obtain dissipated power without actual power measurement, which is based on the thermal simulations of direct heat conduction model (DHCM). Compared to direct power measurements which are very difficult in the case of GaN transistors, temperature measurement by infrared cameras or thermal sensors is more achievable with high accuracy. So far, however, there has been very few discussions about the inverse thermal modelling of electronic systems [167-170]. This is the motivation behind the present study.

In the first part, the principals of IHCM will be presented and formulated. Then, prediction accuracy of the results will be discussed and optimized by Least-Square Method (LSM). Besides, effects of temperature measurement points on the surface and variable parameters such as the dissipated power in GaN  $P$  (W) and the thermal conductivity of PCB substrate  $\lambda_{FR4}$  ( $W/m^2K$ ) will be discussed and analyzed.

#### 3.5.2. Steady State Inverse Heat Conduction Model (IHCM)

Inverse modelling is a method to reconstruct an unmeasurable heating source for embedded PCB structure from its easily observable surface temperature distributions [169]. It has its own advantages especially when high harmonics in digital systems or power converters can cause measurement devices to operate improperly. Hence temperature measuring can serve as a direct indicator of power losses and through inverse source reconstruction, losses in some inaccessible electronic parts can be determined from temperatures at some places. The relationship between power loss  $P$  (W) and temperature rise at some places of an assembly  $dT$  ( $^{\circ}C$ ) in steady state can be established and can be written as a discrete equation (3.5-13).

$$[dT] = F(a, b)[P] + \alpha \quad (3.5-13)$$

where  $\alpha$  is the additive noises and  $F$  a matrix depending on some known or unknown system parameters  $(a, b)$ . If  $[P]$  and  $F(a, b)$  are known,  $[dT]$  calculation is the direct problem (DHCM). If  $[dT]$  and  $F(a, b)$  are known, calculating  $[P]$  is the inverse problem (IHCM). If  $[dT]$  is known, calculating  $[P]$  and parameters  $(a, b)$  is the inverse blind problem.

In the following, IHCM is used to predict the power dissipated by a GaN chip embedded in a PCB substrate as described in Fig.3-26. The 3D FE model of the PCB structure has been created and is used as the real system reference in the proposed methodology.

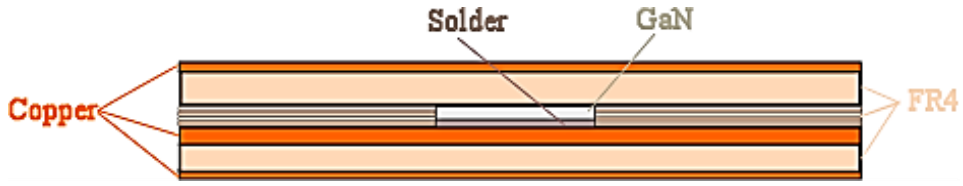


Fig.3-26. PCB structure with embedded GaN chip

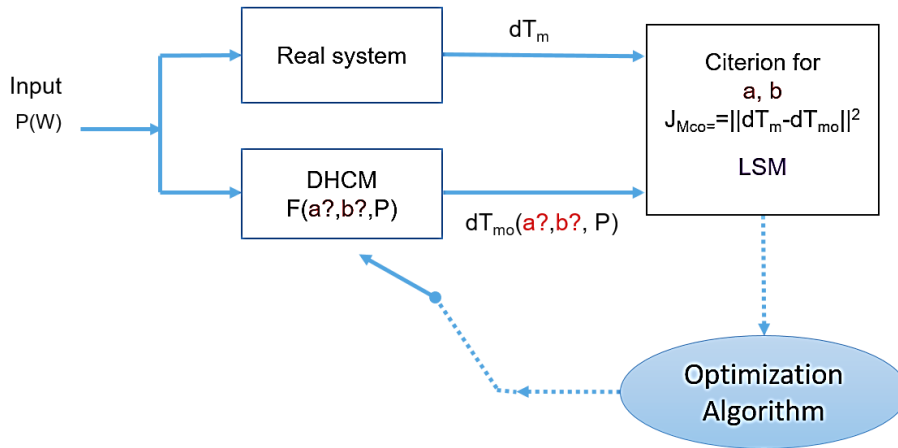


Fig.3-27. Parameters estimation step for DHCM

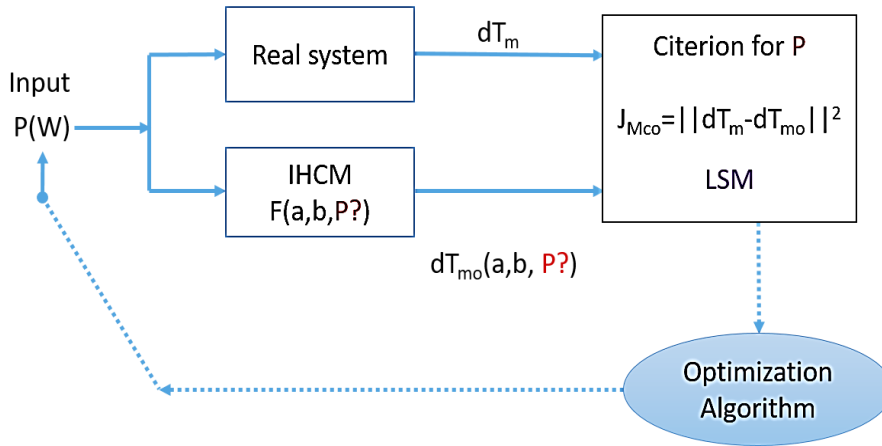


Fig.3-28. Input power estimation step for IHCM

Direct inverse of the problem is not possible for two main reasons: First the problem is not square, the output vector  $[dT]$  has a dimension higher than that of  $[P]$ ; Secondly, even if the sizes are identical, the noise added to measurements leads to high error when using a direct inversion method. The best way to proceed is to use the following method.

In a first step, as presented in Fig.3-27,  $F(a, b)$  is identified by injecting in real system and in the model defined by (3.5-14) a set of known input powers.

$$[dT_{mo}] = F(a, b)[P] \quad (3.5-14)$$

LSM used to calculate the best function  $F(a, b)$  minimizes the sum of square of deviations  $J_{Mco}$  calculated from the difference between temperature variations calculated with (3.5-14)

and those given by the real system. The optimal solution is obtained by a Matlab least square solver which uses the interior-point algorithm, with the method of Lagrange multipliers for determining the solution convergence.

In a second step, corresponding to the inverse problem, injected powers are calculated from temperature measurement on the real system. To realize such inversion, despite the noise on measurements, input powers are also identified by using a LSM as shown in Fig.3-28. The main objective of the algorithm is here to find the vector  $[P]$  that minimize  $J_{Mco}$  while the model is defined by the previous defined  $F(a,b)$ .

In this problem, additional linear constraints were imposed to the solution so that the heat dissipated in GaN device is only supposed to change between  $1W$  and  $10W$ . Our real system model is perfectly known as it is a 3D numerical one.

To evaluate the robustness accordingly to temperature measurement noises in a real system, temperatures obtained from the 3D FE models were corrupted with additive normally distributed random noise with zero mean and maximum deviation of  $0.1^\circ C$ . More sophisticated models are required when the deviation is larger than  $0.1^\circ C$ .

### 3.5.3. Dissipated Power Prediction

Simple linear IHCM could be used when only one parameter such as the value of the dissipated power of a heat source  $P(W)$  has to be estimated.

Firstly, the 3D FE model of PCB structure is built. In this 3D model, the temperature measurements are located at different distances of the die on the top layer of the PCB. A first step as described in Fig.3-27 gives the direct model relationship between  $[dT_{mo}]$  and  $P$  for our system. A known injected power used in the direct model identification is imposed (namely  $1.73W$  in the following figures) and temperature  $[dT_{mes}]$  on 5 or 10 points of the top layer are extracted from the 3D model. As previously explained, a normally distributed random noise with zero mean and maximum deviation of  $0.1^\circ C$  is added to each temperature. The model of LSM is shown in (3.5-15).

$$J_{Mco} = \sum(|[dT_{mo}] + \alpha - [dT_{mes}]|)^2 \quad (3.5-15)$$

From this set of data, inverse problem methodology described in Fig.3-28 is then applied. This problem inversion is realized 1000 times, with new noises values for each trial.

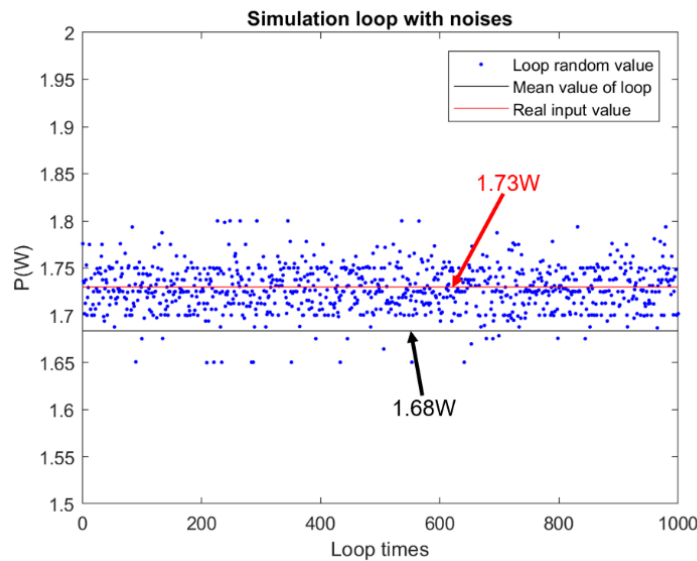


Fig.3-29. Power prediction with 5 temperature sensors (Annex A)

Fig.3-29 and Fig.3-30 give the power calculated by inverting the problem for 5 and 10 measurement points on the PCB top layer, respectively. According to curve fitting tools and LSM in Matlab,  $F(a,b) = [3.917 \ 0.014 \ 0.008 \ 0.004 \ 1.604]$  for the chosen 5 points of interest and equals to  $[3.917 \ 0.014 \ 0.008 \ 0.004 \ 1.604 \ 0.807 \ 0.425 \ 1.972 \ 0.998 \ 2.263]$  for the chosen 10 points of interest.

3D FEM simulation results as references are presented in Fig.3-31. Dissipated power in the embedded GaN chip is 1.73 W. Heat convection coefficient between the top surface of the structure and the air is considered as  $15 \text{ W}/(\text{m}^2\text{K})$ . The bottom of this PCB structure is assumed to be attached to a heatsink and the ambient temperature  $20 \text{ }^\circ\text{C}$ . For example, five chosen points on the top of the PCB structure for measuring temperatures  $[dT_{mes}]$  are indicated in red color.

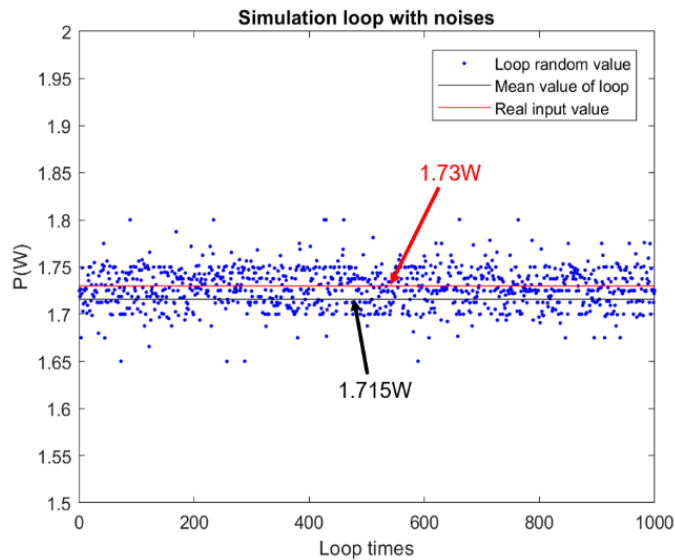


Fig.3-30. Power prediction with 10 temperature sensors (Annex B)

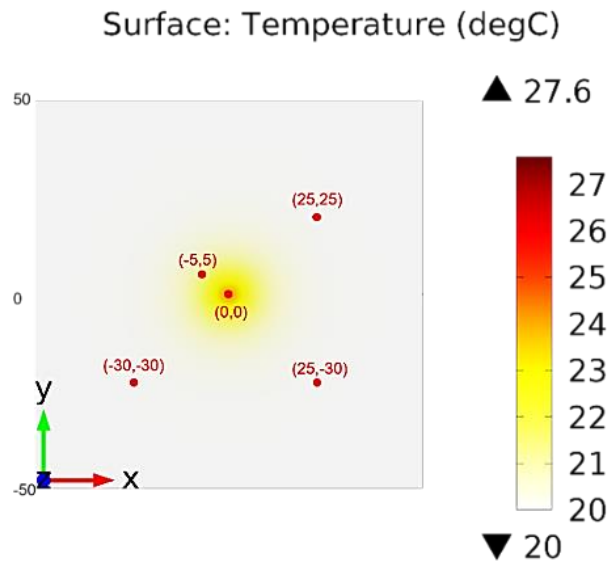


Fig.3-31. Temperature measurements on the top surface of PCB structure by 3D FEM simulations

Comparison between the predicted input power and the really injected one in the 3D simulations reveals a good agreement with an acceptable error within 5 %. It is noticed that the average power calculated over the 1000 trials is closer to the real one when the number

of measurement points is higher:  $1.715\text{ W}$  instead of  $1.68\text{ W}$  compared to the  $1.73\text{ W}$  really injected.

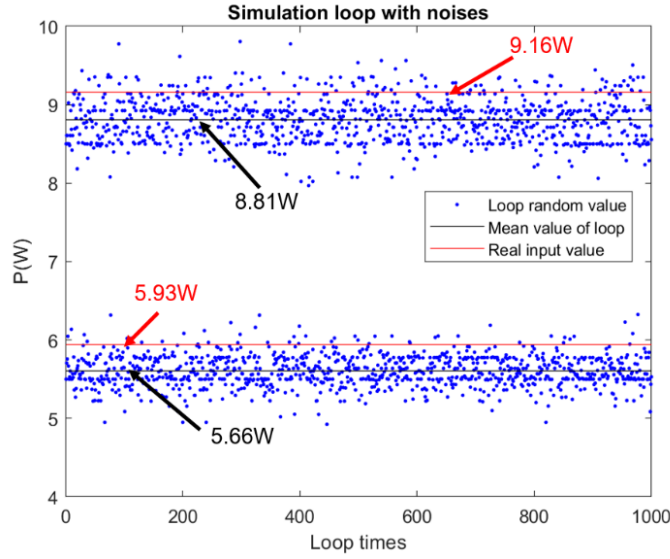


Fig.3-32. Power predictions in 2 embedded GaN dies with 5 temperature sensors (Annex C)

The methodology could also be used to predict the dissipated powers of more than one heat source. For example, Fig.3-32 depicts the results for a PCB structure with two heating GaN chips embedded in the PCB substrate. In this new configuration, errors on the two injected power are less than  $10\%$  for a 5 sensors temperature measurement.

Benefit of this power prediction method is that it can provide a quick estimation of dissipated power even for embedded devices. The prediction accuracy could be improved by increasing the number of temperature measurement points or by developing more sophisticated DHCMs and IHCMs. For example, one can increase the number coefficient parameters such as structure dimensions, relative chip position and material properties of different components when creating the models with higher accuracy.

#### 3.5.4. Dissipated Power and Thermal Conductivity Prediction

According to (1.4-11), temperature variation depends not only on the dissipated power, but also on the thermal conductivity of the PCB substrate fabricated by woven fiberglass or laminated cotton paper. But its value is not provided by manufacturers. Therefore, estimation of the substrate thermal conductivity could help to identify the thermal resistance of PCB substrate and to choose appropriate thermal management solutions.

For this purpose, the determination of DHCM parameters algorithm described in Fig.3-27 is used with two input parameters which are the input power and the material thermal conductivity. In this first step, a collection of values for  $P$  and  $\lambda_{FR4}$  are applied and  $F$  is defined as a function of  $\lambda_{FR4}$  and  $P$ . Due to the inverse proportionality of the thermal resistance with  $\lambda_{FR4}$ , the chosen fitting function over this parameter is non-linear. Developed relationship between  $P$  and  $\lambda_{FR4}$  for LSM calculations in Matlab is described in (3.5-16).

$$dT_{m0} = a_0 + a_1 \cdot (\log P) + b_1 \cdot (\log \lambda_{th}) + a_2 \cdot (\log P)^2 + c_1 \cdot (\log P)(\log \lambda_{th}) + b_2 (\log \lambda_{th})^2 \quad (3.5-16)$$

where  $a_0$ ,  $a_1$ ,  $a_2$ ,  $b_1$ ,  $b_2$  and  $c_1$  are unknown model coefficients. With the function resulting from the first stage, the inverse problem methodology described in Fig.3-28 is applied. As previously, a known injected power chosen to be different from the set of power used in the direct model identification is imposed (namely  $5.79\text{ W}$ ), and the thermal

conductivity of the PCB substrate is fixed in the 3D model to  $0.62 \text{ W/mK}$ . This problem inversion is done  $1000$  times with new noises values added to the temperature measurement for each trial.

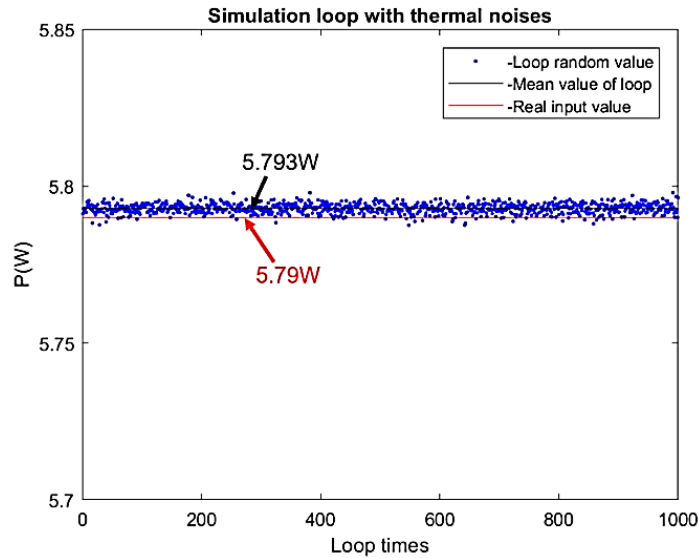


Fig.3-33. Power prediction for IHCM with two unknown system parameters (Annex D)

Results are presented in Fig.3-33 and Fig.3-34. Ten points on the surface in the region of interest have been chosen for temperature measurements. The results demonstrate a high accuracy on the predicted value of the dissipated power in the GaN chip as well as on the thermal conductivity of the PCB.

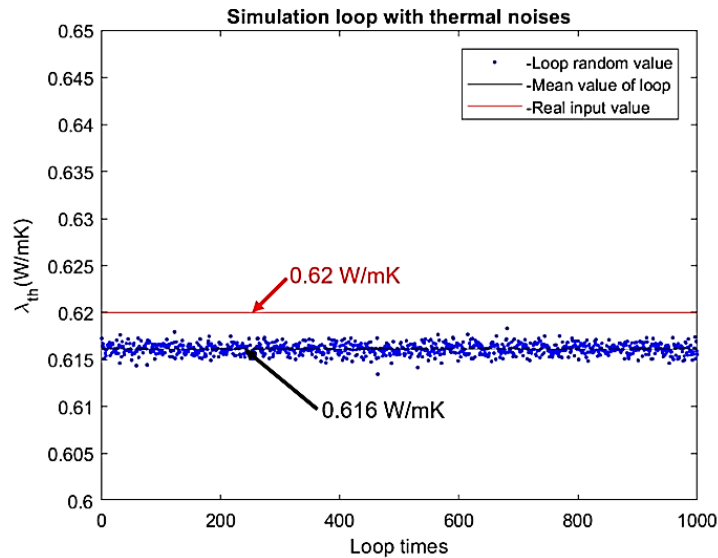


Fig.3-34. Prediction of thermal conductivity of the PCB substrate for IHCM with two unknown system parameters (Annex D)

To save unnecessary cost by using less temperature sensors or less data collections by infrared thermography, inverse model calculation with just 6 points of interest on the top layer of the PCB were realized. The results are presented in Fig.3-35 and Fig.3-36.

It is shown here that IHCMs could accurately predict system parameters even with less points of measurement in the region of interest. This can lead to the simplification of thermal measurements in a test bench.

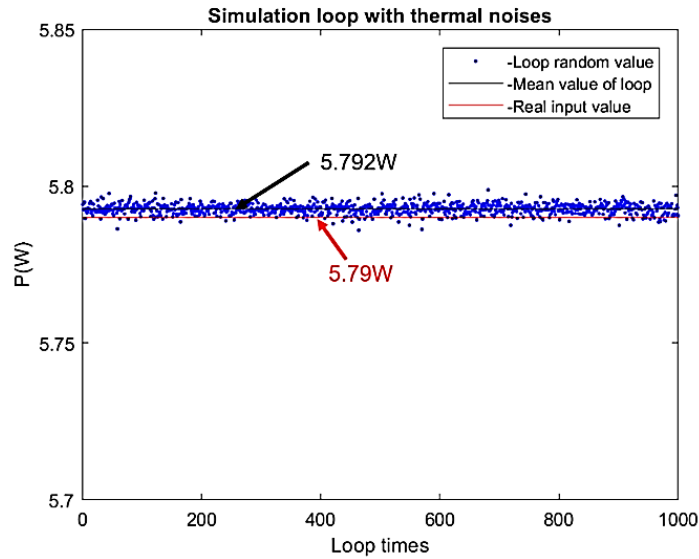


Fig.3-35. Power prediction with less temperature sensors (Annex D)

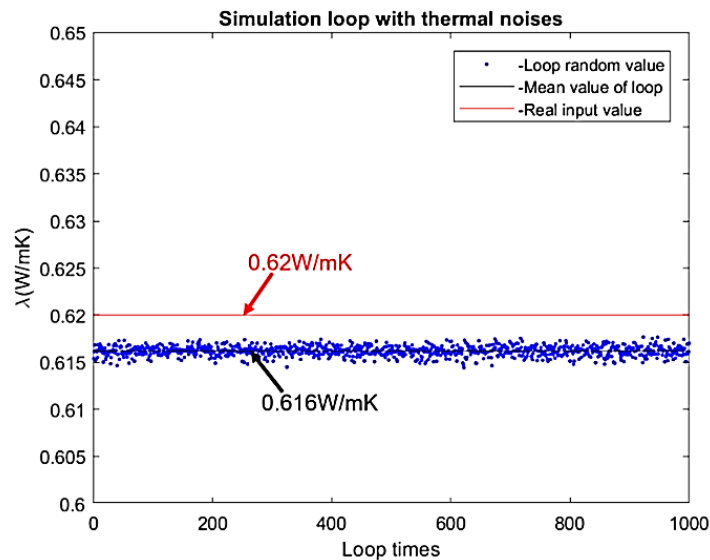


Fig.3-36. Thermal conductivity prediction with less temperature sensors (Annex D)

### 3.6. SUMMARY

In this chapter, a manufacture guideline of the thermal vias has been proposed and the design of thermal via has been optimized by the via parameters. This optimization is based on the theoretical analysis of the thermal resistance of the total PCB structure. The assumption of one-dimension heat conduction provides us the basis to develop the function of the total thermal resistance and then to normalize the via parameters into dimensionless form. This normalization procedure facilitates the discussions about the influences of each via parameter on the cooling effects.

Then according to the 3D FEM, impact of each via parameter such as the ratio of via-cluster surface, the ratio of via diameter, the ratio of via plating thickness as well as the via pattern formed by multiple vias has been analyzed to observe the reduction of the total thermal resistance. And the test bench has been established to validate simulation predictions. It is found that this cooling solution by creating thermal via is efficient to enhance the thermal performances of the PCB structures by increasing the thermal conductivity of the PCB substrate. For limited pad surface, in order to obtain smaller thermal path, larger via-



cluster surface ratio, via diameter ratio as well as larger ratio of via plating thickness are preferred. And for further thermal performance improvement, PCB copper thickness could be increased to enhance the lateral heat flux along the copper layer at the same time.

In addition, in consideration of the long time cost for power loss measurement, the conception of inverse thermal models for power loss prediction have been proposed. The purpose is to give a fast power loss estimation of the heat source embedded in the PCB substrates so that we can choose appropriate thermal management solutions according to the dissipated power. 3D simulations based on a simple PCB structure have proved that this conception is feasible by the temperature distribution on the structure surface to realize a temperature-to-power mapping.

## CHAPTER 4. THERMOELECTRIC COOLING

- 4.1. Introduction
- 4.2. 3D FEM Analysis
- 4.3. 1D Electro-Thermal Modeling
- 4.4. Experimental Validation
- 4.5. Summary



# CHAPTER 4. THERMOELECTRIC COOLING

## 4.1. INTRODUCTION

Creating thermal vias is an effective method in cooling down the total PCB structures as demonstrated in previous studies. But in consideration of their drawback due to their electrical conducting property, as well as the decrease of available electrical routing spaces of the pad layer, another solution by using thermoelectric cooling devices has been proposed due to its operation facility.

As shown in Fig.4-1 and Fig.4-2, the cooling solution with Peltier devices beside the heating source for the PCB structures has been proposed. Thermoelectric cooling (TEC) by Peltier modules differs from thermal vias in the way of cooling electronic components directly by forcing lateral heat flux along the top PCB copper layer in certain configurations, and the heat will be drawn by the TEC devices, and then transferred into environment.

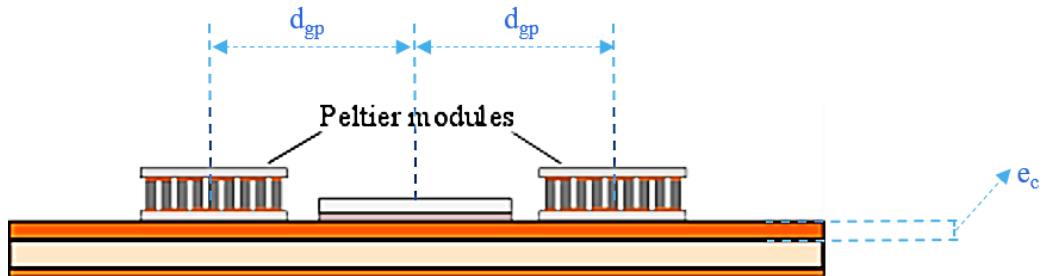


Fig.4-1. PCB structure with Peltier modules

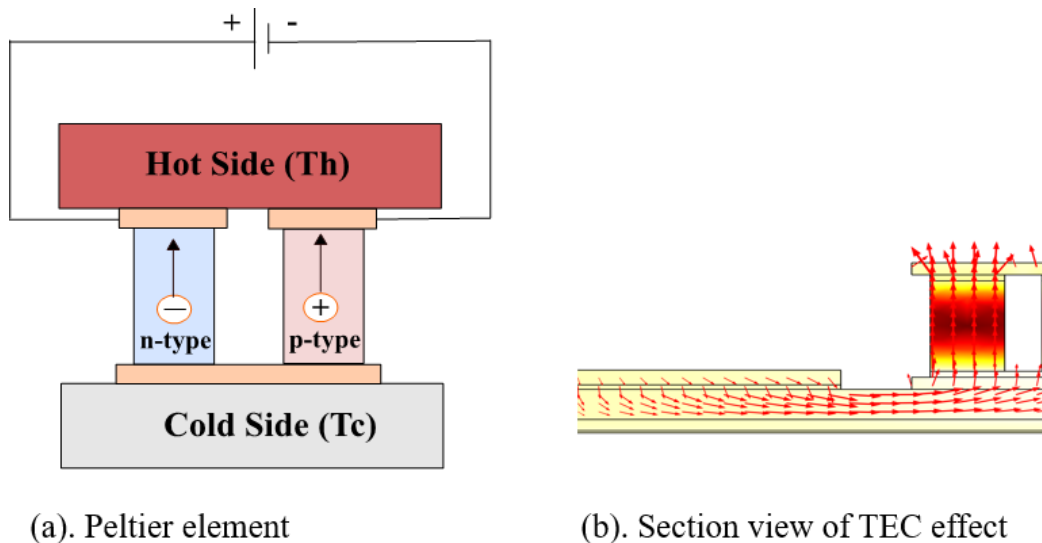


Fig.4-2. One element of a TEC device

According to the thermoelectric theory previously described in (1.4-18) to (1.4-22), it exists two working possibilities for Peltier devices: *heat pump mode* and *heat engine mode* [171]. Their difference lies in the electric power sign. An electric power is supplied to the Peltier device during the heat pump mode, and an electric power is generated during the heat engine mode. The comparisons of the two operating modes concerning the direction of energy flow are drawn in Fig.4-3.  $Q_h$  (W) is the heat pumped into or flowing out of the hot reservoir,  $Q_c$  (W) is the heat pumped out of or flowing into the cold reservoir,  $Q_{ed}$  (W) corresponds to the work done by the Peltier or by the heat engine, depending on its working mode.

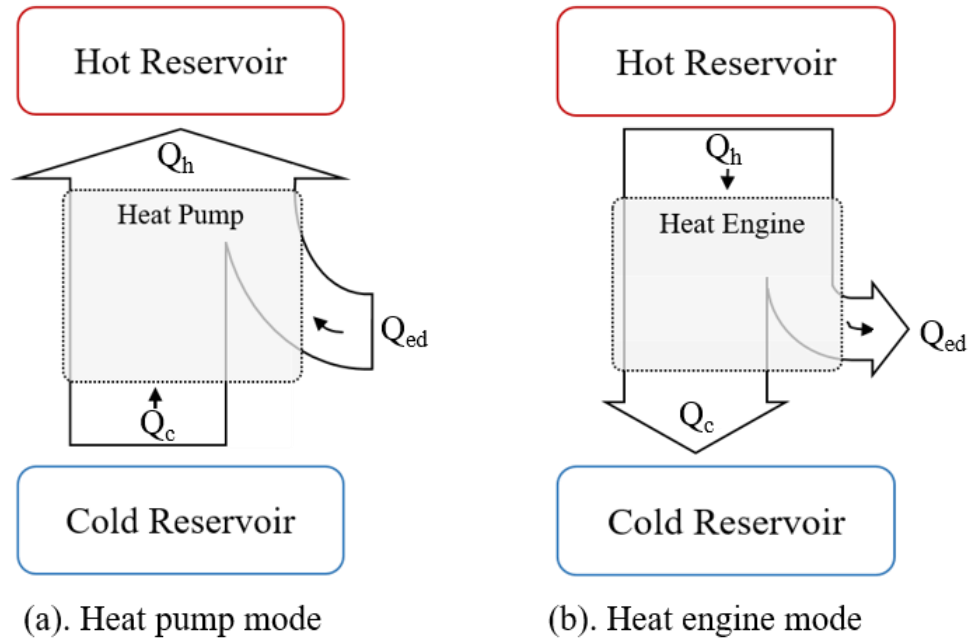


Fig.4-3. Working mode of the Peltier device

In heat pump phase, electrical power is supplied into the Peltier device. This input power equals the rate at which the Peltier does work to pump heat out of the cold reservoir and into the hot one. By contrast, in heat engine phase, heat flows out of the hot reservoir and part of it is converted to electrical energy. This generated power equals to the rate at which the Peltier does work on the electric load.

Here, in cases of cooling the PCB substrates, heat pumping mode will be applied. In fact, the input power  $Q_{ed}$  gives the heat pump rate. The cold reservoir absorbs heat energy of the structure and releases it by flowing into the hot side, then into the environment. Therefore, an important criterion called Coefficient of Performance (COP) can be derived as in (4.1-1). This coefficient enables to choose a suitable Peltier device and to assess its cooling efficiency. Maximum power dissipation of TEC devices is limited to several tens of watts, and the COP is usually less than one in applications.

$$COP = \frac{Q_c}{Q_{ed}} \quad (4.1-1)$$

This chapter is dedicated to evaluate the cooling performances of Peltier devices applied for PCB structures. Firstly, the influences of different Peltier parameters will be studied based on the 3D FEM analysis. Then, a 1D electro-thermal resistance network of the cooling structure according to the heat conduction assumption will be developed in order to give a fast estimation of the junction temperature and also of the cooling efficiency. Thirdly, the experimentations have been carried out to validate the 3D and 1D thermal models. Finally, the cooling performances of the TEC devices will be discussed to optimize their usage so that we can maximize the COP values for designed junction temperature.

## 4.2. 3D FEM ANALYSIS

The cooling performances of the TEC devices are related to their input current, number of Peltier element in series  $N_p$  and their placement on the PCB surface. The optimum applied current,  $N_p$ , and the size of the TEC device are usually fixed by manufacturers and can be found in the datasheet of the product.

In this part, influences of different Peltier parameters such as the number of Peltier elements  $N_p$ , their position beside the chip  $d_{gp}$  (mm) as well as the copper thickness  $e_c$  (mm) on the PCB substrate will be discussed at first based on the 3D FE models of the cooling structure (Fig.4-1).

3D FEM simulations are performed with COMSOL Multiphysics which allow to build models coupling thermal and electrical domains based on the thermoelectric effects. This 3D FEM is used to solve the system of thermoelectric equations providing values for temperature distribution, thermal flux, temperature gradient, and voltage distribution. For the following simulations, Peltier element parameters (Fig.4-2(a)) are defined in Table 4.1. For the PCB substrate, material properties are the same as in previous sections (see Table 3.1). A heat dissipation of  $1\text{ W}$  in the chip and an equivalent convection heat-transfer coefficient of  $15\text{ W}/(\text{m}^2\text{K})$  from all external surfaces (except the bottom layer and the top TEC plate) to the ambient are applied. The ambient temperature is supposed to be  $25\text{ }^\circ\text{C}$ . The bottom copper layer and the TEC top plate are assumed to be attached to heatsinks and are considered as isothermal.

Table 4.1. Peltier element parameters

Part	Material	Height (mm)	Width (mm)	Depth (mm)
Hot or Cold Side	Alumina	0.2	3	2.5
PN Junction	$\text{Bi}_2\text{Te}_3$	1.5	1	1
Copper-Hot side	Copper	0.1	1	1
Copper-Cold side	Copper	0.1	2.5	1

It is known that large temperature rise produces thermomechanical stresses in components due to the differences in the Coefficient of Thermal Expansion (CTE) of the different used materials [172], which may lead to cracks at interfaces of materials with different CTE. Two TEC devices are applied beside the GaN chip to guarantee a temperature uniformity over the chip attachment surface.

#### 4.2.1. Placement of The Peltier Device $d_{gp}$ and Number of Peltier Elements $N_p$

It is a common sense that the cooling device should be as close as possible to the heating component. But the sensitivity of the thermal performances to TEC modules position is unknown. So, it is important to identify the influence of the distance between GaN transistor and TEC device to see whether it is a critical design parameter or not. Thermal simulation results for a 3D model with 3 pairs of Peltier elements per module are presented in Fig.4-4. It is obvious that the temperature distribution on the PCB substrate around the heating source is more uniform with lower temperature when  $d_{gp}$  is smaller. Fig.4-5 depicts the evolution of the average thermal resistance of the PCB substrate  $R_{thc}$  (K/W), which is calculated as the ratio of the temperature difference between the GaN bottom surface and the ambient temperature divided by the GaN dissipated power.

It is seen that the distance  $d_{gp}$  between GaN and Peltier modules greatly affects the equivalent thermal resistance. This can be explained because the heat flux drawn by the TEC modules flows laterally in the top copper layer. As the distance  $d_{gp}$  increases, the lateral thermal resistance of this path increases as well. This means that for dissipating the same heat flux from the heat source, without consideration of the heat spreading effect, the temperature difference between the GaN bottom surface and the TEC bottom plates will be increased with larger distance  $d_{gp}$ .

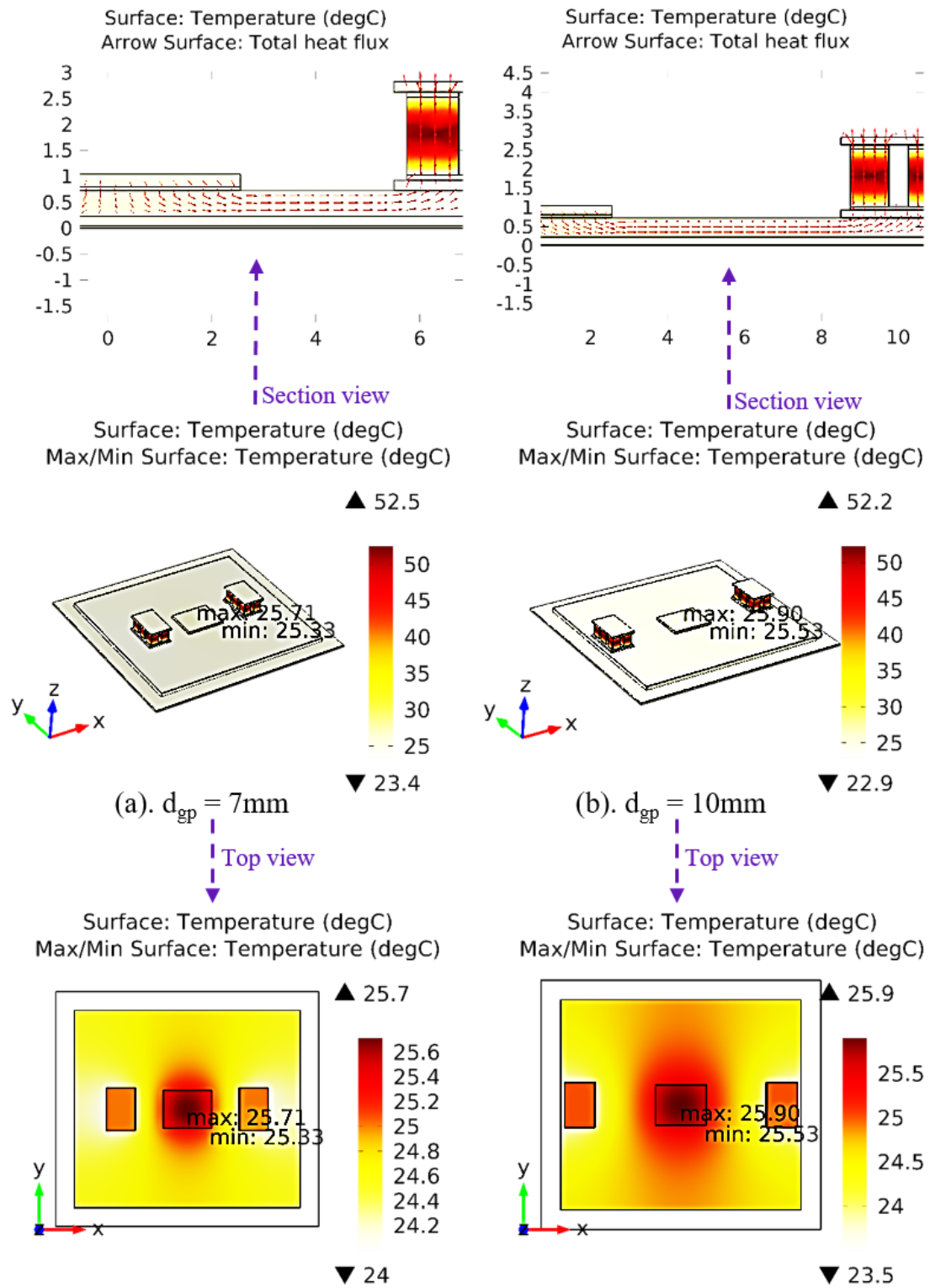


Fig.4-4. Examples of 3D FEM simulations for PCB structures with different distance between the chip and the Peltier devices. A heat dissipation of 1 W in the chip, an equivalent convection heat-transfer coefficient of 15 W/(m<sup>2</sup>K) from all external surfaces (except the bottom layer and the top TEC plate) to the ambient, a copper thickness  $e_c$  of 500 $\mu$ m on the top of the PCB substrate and an optimum input electric power of 0.4 V in the Peltier modules are applied. The ambient temperature is at 25 °C.

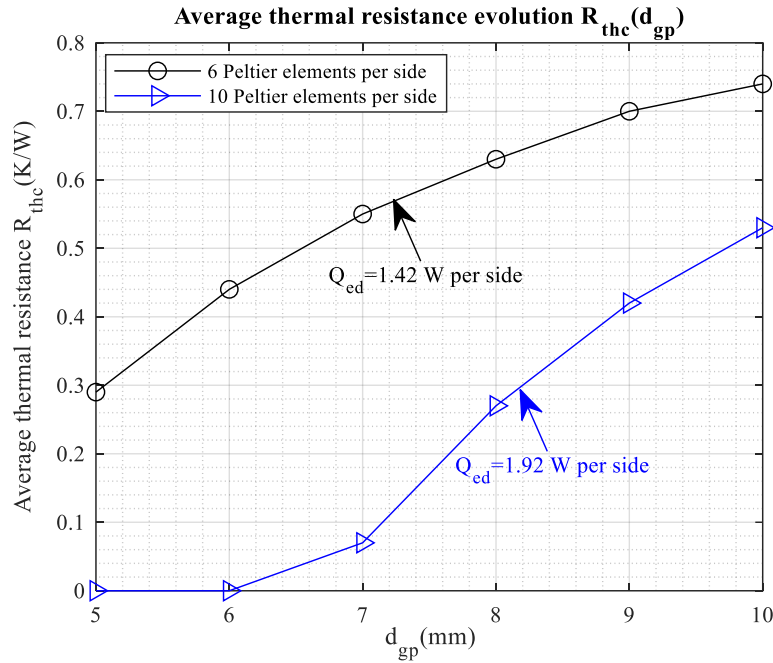


Fig.4-5. Thermal resistance evolution following the distance  $d_{gp}$ . A heat dissipation of 1 W in the chip, an equivalent convection heat-transfer coefficient of 15 W/(m<sup>2</sup>K) from all external surfaces (except the bottom layer and the top TEC plate) to the ambient and a copper thickness  $e_c$  of 500 $\mu$ m on the top of the PCB substrate are applied. The ambient temperature is at 25  $^{\circ}$ C.

In addition, it can be noticed that the number of Peltier elements is a critical parameter regarding the equivalent thermal resistance value as it defines the maximum heat flux that can be drawn by the TEC module. But more electrical power is consumed when the optimum cooling effect is achieved with more Peltier elements.

#### 4.2.2. Copper Thickness on The PCB Substrate

Then, effect of top copper layer thickness for the PCB assembly with TEC modules (6 Peltier elements per side,  $d_{gp}$  equals 7 mm) is analyzed. As we can see in Fig.4-6, the equivalent thermal resistance varies significantly with the copper thickness. But we can also notice that the variation is less for higher copper thickness.

Besides, it has been proven in chapter 3 that the well-known via technology could not compete with DBC substrate in thermal performances even if the lateral thermal diffusion is increased in PCB by using thicker copper layers (Fig.3-21). Here, TEC devices provide a way to reach the DBC thermal performances by combining their cooling effect with that of the high top layer copper thickness. This is shown in Fig.4-6, where a PCB and DBC structures with the same breakdown voltages are compared. In this example, it is found that an enhanced PCB substrate with 6 Peltier elements demonstrates higher thermal performances than DBC when its copper thickness is beyond 300  $\mu$ m.

In a word, the design of PCB substrate with thermoelectric cooling is therefore an optimization between the TEC number of elements  $N_p$ , the placement of these modules  $d_{gp}$  and the top layer copper thickness  $e_c$ . Indeed, optimization of TEC modules is difficult to achieve as the dimensions and the number of Peltier elements are fixed by the manufacturers. The optimization is therefore largely constrained.

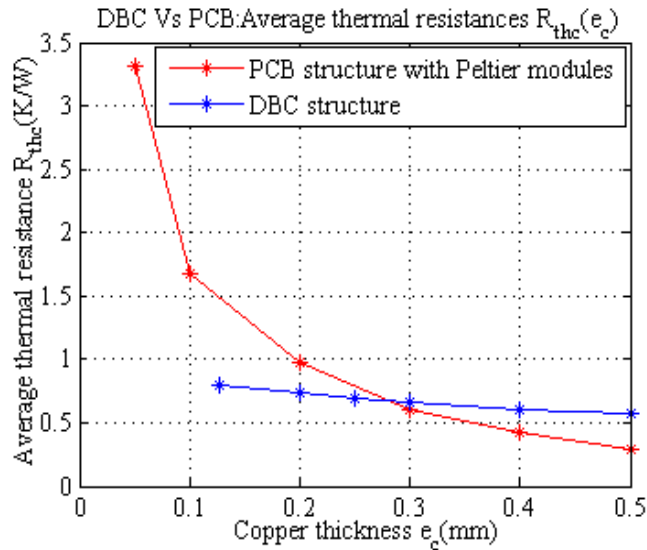


Fig.4-6. Thermal performance comparison between PCB and DBC structures. A heat dissipation of 1 W in the chip, an equivalent convection heat-transfer coefficient of 15 W/(m<sup>2</sup>K) from all external surfaces (except the bottom layer and the top TEC plate) and an ambient temperature of 25 °C are applied.

#### 4.2.3. Modeling of The Peltier Device CP39236H

Previous concise analysis of the Peltier parameters gives us a general conscience of the influences of each part on the total cooling structure. The Peltier device CP39236H provided by CUI Inc. has been applied in the PCB cooling. Device dimensions and Peltier parameters to create the 3D FE models are presented in Fig.4-7 and Table 4.2.

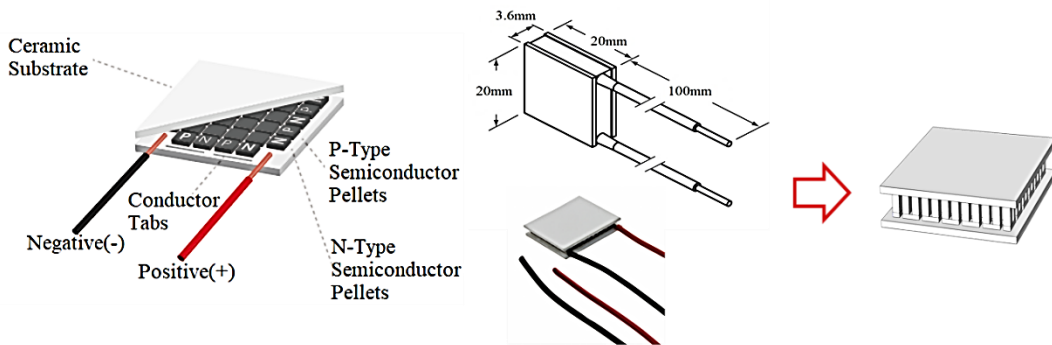


Fig.4-7. 3D model of Peltier device CP39236H

Table 4.2. Peltier element parameters and ceramic substrate dimensions of each side

Part	Material	Height (mm)	Width (mm)	Depth (mm)
PN Pellet	Bi <sub>2</sub> Te <sub>3</sub>	1.6	1	1
Hot side	Copper	0.4	1	1
Cold side	Copper	0.4	2.5	1
Substrates	Al <sub>2</sub> O <sub>3</sub>	0.6	20	20

3D FEM simulations have been executed as shown in Fig.4-8. It depicts an example of simulated result for the 3D model of the product CP39236H.



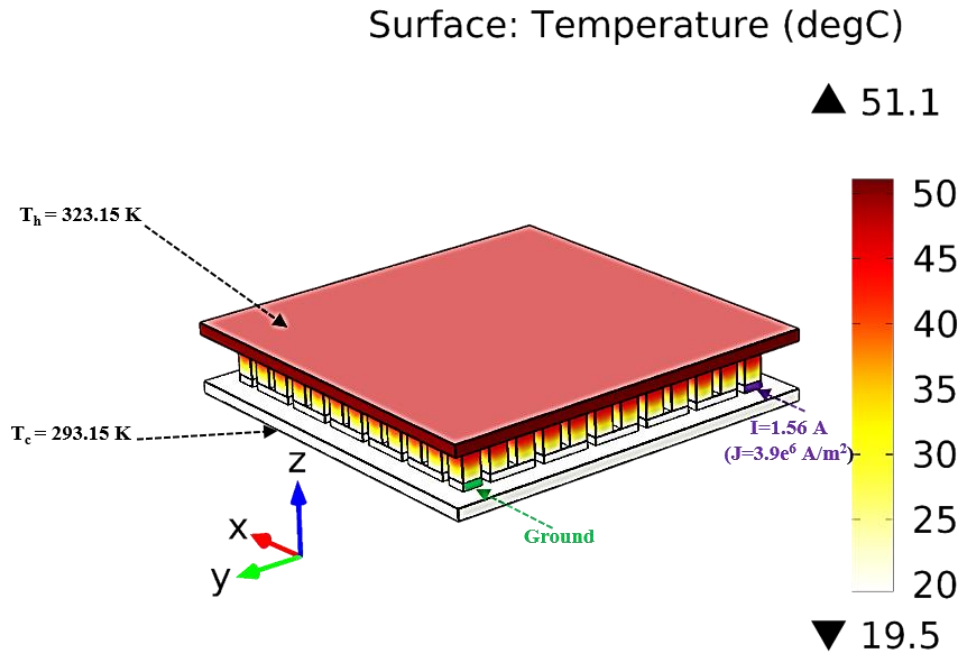


Fig.4-8. A simulated example for the 3D FEM model of product CP39236H built in COMSOL with the input current  $I$  equaling 1.56 A, the temperature of the cold side  $T_c$  equaling 20 °C, the temperature of the hot side  $T_h$  equaling 50 °C.

For designed cooling structures, absorbed heat  $Q_c$  (W) of the Peltier modules depends on the input electrical power  $Q_{ed}$  (W), and also on the temperature difference  $dT$  (°C) between hot and cold reservoirs. For example, the relationship between input power,  $dT$  and absorbed heat  $Q_c$  is presented in Fig.4-9 and Fig.4-10. Fig.4-11 depicts the relationship between the COP and the input current for fixed temperature  $T_h$  of the hot side. And these 3D FEM simulation results correspond to the datasheet (see in Fig.4-12) given by the manufacturer [173]. For certain input power, the heat absorption  $Q_c$  could be calculated or found according to the function diagrams in Fig.4-9 and Fig.4-10 by measuring the temperature  $T_h$  and  $T_c$ .

The good agreement between the datasheet characteristics (Fig.4-12) and the 3D FE models of the product CP39236H (Fig.4-9 and Fig.4-10) have been considered sufficiently to be used in the following cooling structure 3D FE model. The cooling effect of Peltier modules for the same previous PCB structure (Fig.3-23) is shown in Fig.4-13. Here, heat source in the bare die is 10 W. The ambient temperature is 25 °C. Compared to the cooling effect shown in Fig.3-24, Peltier modules are more efficient with the appropriate electrical current  $I_{in}$  (A). With TEC devices, the equivalent thermal resistance of the total PCB structure is controllable and changeable depending on  $I_{in}$  according to the desired cooling effect. For higher heat dissipation, one solution is to apply more powerful Peltier modules with more Peltier elements. Another solution is to increase the top PCB copper thickness  $e_c$  when using Peltier devices.

However, Peltier modules consume a lot of electrical power to reach the required power dissipation. Such high power flow corresponds to low values of COP of such devices. COP performances of the studied device according to  $I_{in}$  and  $dT$  are shown in Fig.4-11. For example, when  $T_h$  is 50 °C and  $dT$  equals 50 °C, an electrical power of 18.33 W is required to get 4 W of heat power pumped from the cold side corresponding to a performance factor COP of 0.22. Besides, it is found that there is an optimum value of COP and the COP is maximum at the lowest temperature difference  $dT$ . Therefore, from the point-of-view of an optimum performance of the cooling system, temperature difference between the object and the heat sink should be kept as low as possible.

In addition, the 3D FEM simulations are time consuming due to the coupling effects between the thermal and electrical domain. For each simulation, it takes at least half an hour even though with a coarse mesh of the structure. Therefore, it is proposed to develop a 1D thermal resistance network of the designed cooling structure in steady state so that we can quickly assess the TEC cooling efficiency in order to provide a guideline for active junction temperature control with optimum COP value.

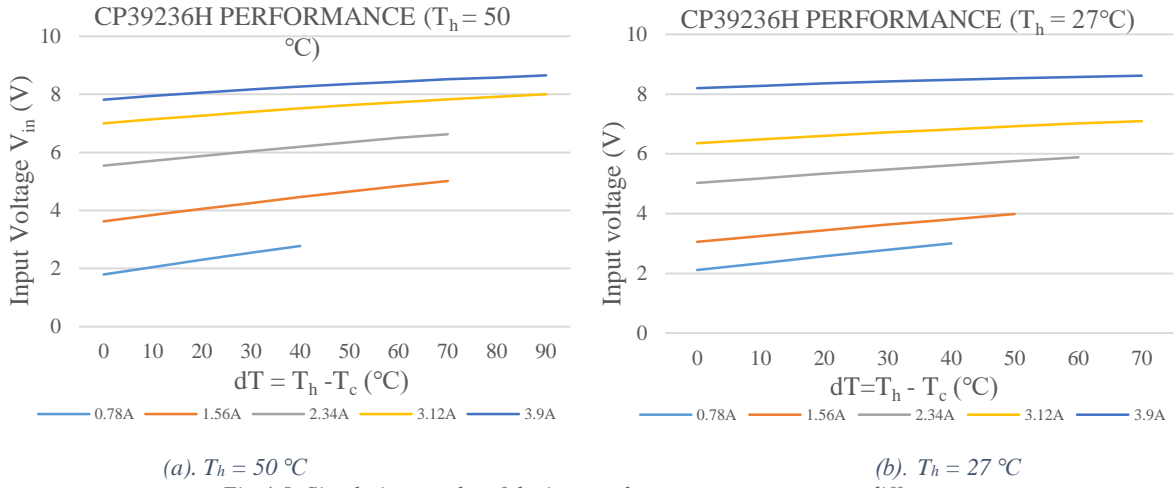


Fig.4-9. Simulation results of the input voltage versus temperature difference

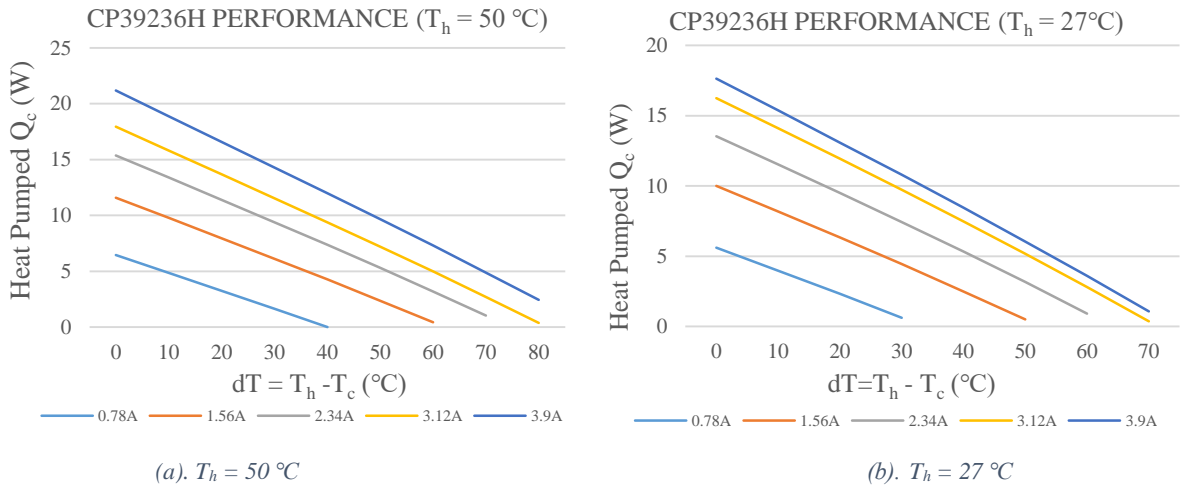


Fig.4-10. Simulation results of the heat absorbed versus temperature difference

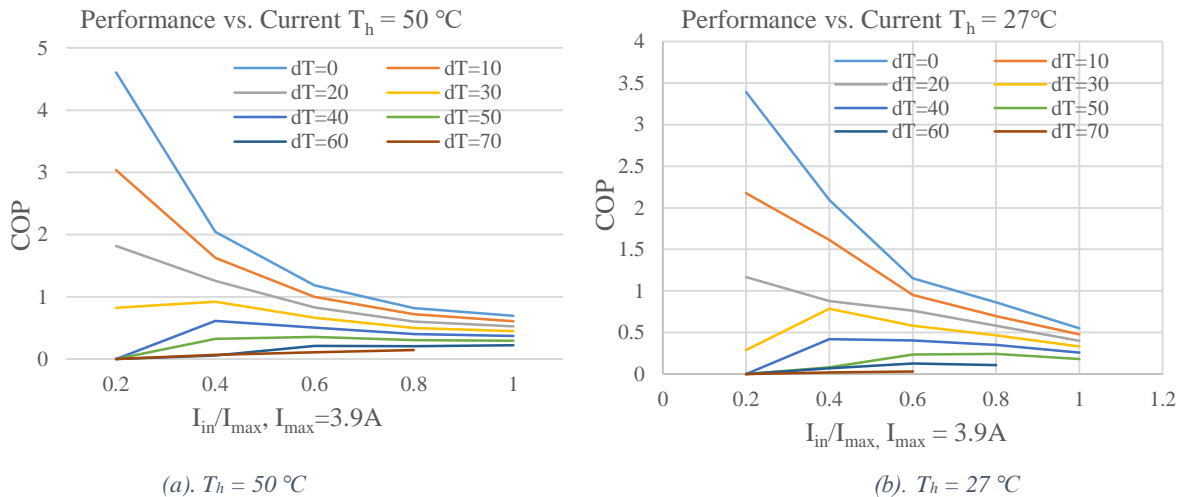
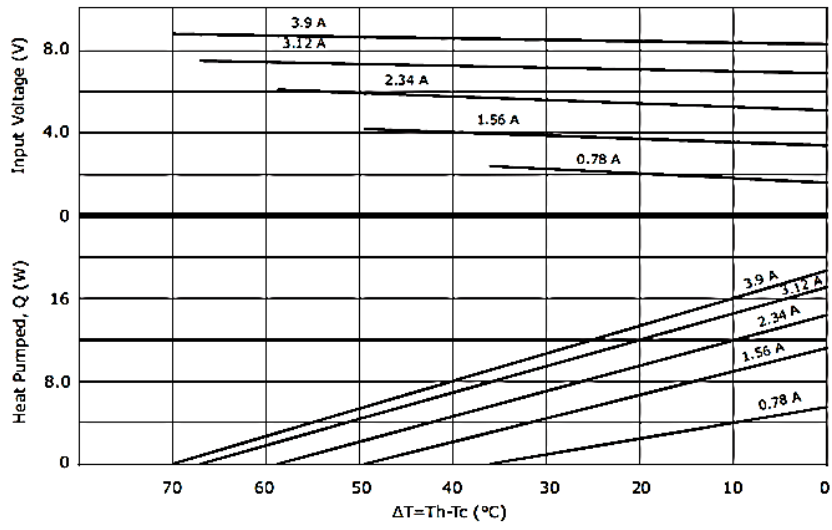


Fig.4-11. Simulation results of the relationship between COP and input current

**CP39236H PERFORMANCE (Th=27°C)**



**CP39236H PERFORMANCE (Th=50°C)**

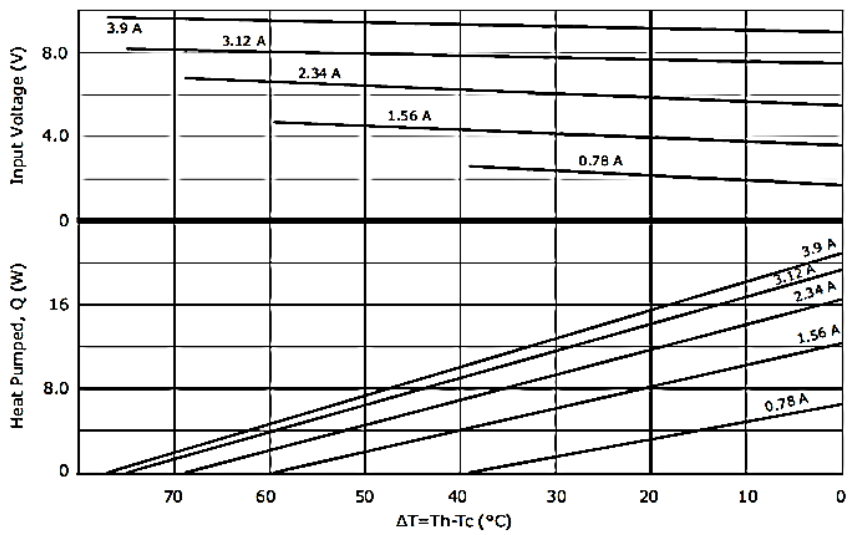


Fig.4-12. CP39236H performances from datasheet [173]

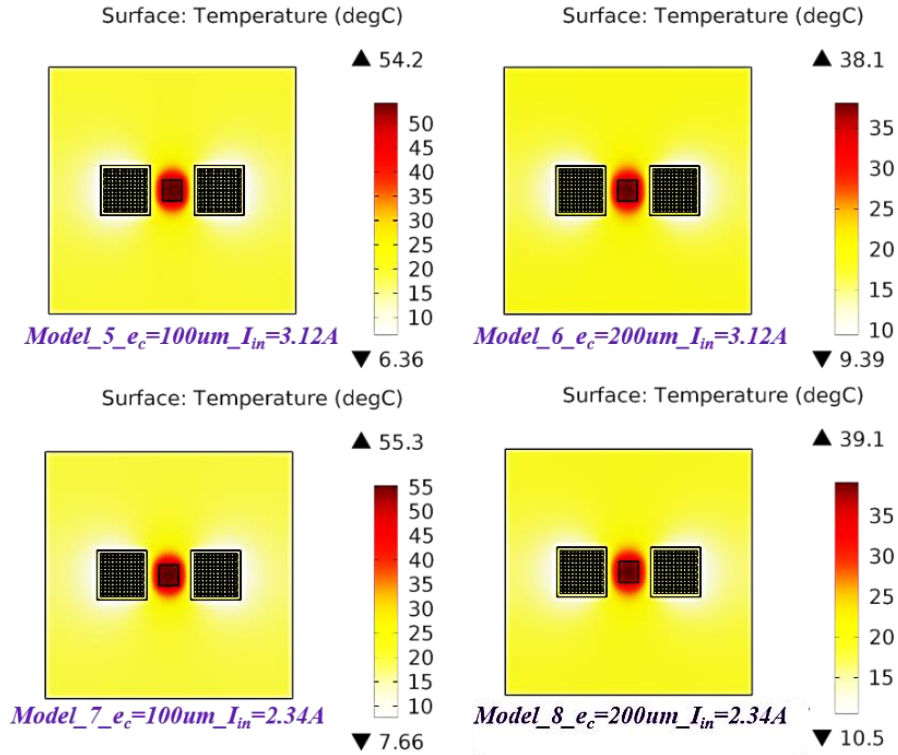


Fig.4-13. Cooling performances of Peltier modules for PCB structures

### 4.3. 1D ELECTRO-THERMAL MODELING

The schematic of the proposed cooling configuration is shown in Fig.4-14. Peltier devices are put beside the heating source with a distance  $l_{jp}$  (mm). Based on the cooling mechanism of the Peltier effect, heat flux will be firstly forced along the copper layer on the PCB substrate, then passing through the Peltier devices, finally into the ambient. So almost all the heat flux will be evacuated upward due to the poor thermal conductivity of the material FR4. To facilitate the thermal analysis, a heating resistor ( $7.9mm \times 8.5mm \times 2.8mm$ ) and only the copper layer ( $100mm \times 100mm \times 300\mu m$ ) on the top of the PCB substrate will be applied. Power supply for the heating resistor will represent the total power loss of certain power modules needed to be dissipated. In this case with thick copper layer, the PCB substrate layer in FR4 is omitted here because of its worse thermal conductivity compared to copper, as well as the upward thermal path for the designed cooling structure.

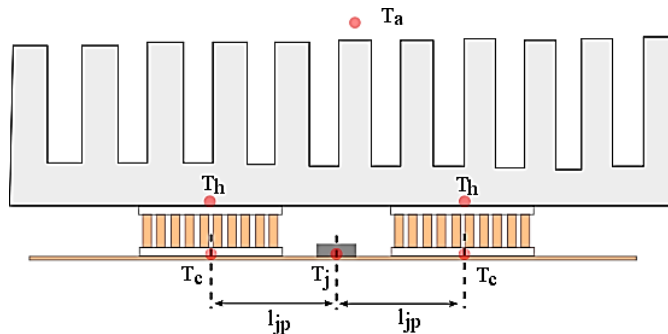


Fig.4-14. Schematic of proposed cooling structure with Peltier devices beside the heating source

Three different Peltier device products provided by CUI Inc. have been applied with Peltier element array of  $12 \times 12$  for CP39236H and CP30238 [173, 174],  $8 \times 8$  for CP60133 [175], respectively. As previously mentioned, the commonly used material for Peltier elements is Bismuth Telluride ( $Bi_2Te_3$ ) and the material thermoelectric properties vary with carrier concentration depending on manufacture process [176]. However, the detailed

thermoelectric properties of Seebeck coefficient  $S_e$  (V/K), electrical resistivity  $\rho$  ( $\Omega \cdot m$ ), thermal conductivity  $\lambda_{th}$  (W/mK) and geometric factor  $G$  are difficult to obtain directly from the datasheet. Fortunately, device parameters of equivalent Seebeck coefficient  $S_m$  (V/K), equivalent electrical resistance  $R_m$  ( $\Omega$ ) and equivalent thermal conductance  $\lambda_m$  (W/K) are obtainable with product specifications on the datasheet such as  $\Delta T_{max}$ ,  $I_{max}$ ,  $V_{max}$ ,  $Q_{max}$  and  $T_h$  [147, 176]. According to the datasheet,  $\Delta T_{max}$  (K) is the largest temperature between  $T_c$  and  $T_h$ ;  $I_{max}$  (A) is the maximum input current at  $\Delta T_{max}$ ;  $V_{max}$  (V) is the voltage at  $\Delta T_{max}$  and  $I_{max}$ ;  $Q_{max}$  (W) is the maximum amount of the heat absorbed by the cold side at  $I_{max}$  and  $\Delta T = 0$  °C. Equations (4.3-2) to (4.3-7) give us the correlations of equivalent device parameters.

$$R_m = \frac{2 \cdot N \cdot \rho}{G} \quad (4.3-2)$$

$$\lambda_m = 2 \cdot N \cdot \lambda_{th} \cdot G \quad (4.3-3)$$

$$S_m = 2 \cdot N \cdot S_e \quad (4.3-4)$$

$$R_m = \frac{(T_h - \Delta T_{max}) \cdot V_{max}}{T_h \cdot I_{max}} \quad (4.3-5)$$

$$\lambda_m = \frac{(T_h - \Delta T_{max}) \cdot V_{max} \cdot I_{max}}{2 \cdot T_h \cdot \Delta T_{max}} \quad (4.3-6)$$

$$S_m = \frac{V_{max}}{T_h} \quad (4.3-7)$$

Details of the applied Peltier devices in this work are listed in Table 4.3. Thermoelectric material properties of  $\text{Bi}_2\text{Te}_3$  such as thermal conductivity  $\lambda_{th}$ , Seebeck coefficient  $S_e$  and electrical conductivity  $\sigma$  (S/m) are then obtainable with geometric parameters (Table 4.2). The material properties are presented in Table 4.4. These device parameters and material properties will be applied into the 1D and 3D thermal simulations in the following sections.

Table 4.3. Dimensions and calculated parameters of Peltier devices

Parameters	CP39236H	CP30238	CP60133
Dimensions	20×20×3.6	20×20×3.8	15×15×3.3
Peltier	144	144	64
$\Delta T_{max}$ (K)	70	72	72
$I_{max}$ (A)	3.9	3	6
$V_{max}$ (V)	8.8	8.6	3.8
$Q_{max}$ (W)	18.7	16.7	13.6
$T_h$ (K)	300.15	323.15	323.15
$S_m$ (V/K)	0.0293	0.0266	0.0118
$R_m$ ( $\Omega$ )	1.73	2.23	0.49
$\lambda_m$ (W/K)	0.188	0.139	0.123

Table 4.4. Thermoelectric material properties

Material	Thermal conductivity (W/mK)	Electrical conductivity (S/m)	Seebeck coefficient (V/K)
Copper	400	--	--
$\text{Al}_2\text{O}_3$	238	--	--
$\text{Bi}_2\text{Te}_3$	2.1	$1.33e^5$	$2.1e^{-4}$

#### 4.3.1. 1D Modeling of The Cooling Structure

Based on (4.3-2)(4.3-3)(4.3-4), previous Peltier equations (1.4-18) to (1.4-22) can be recast into the following form as (4.3-8)(4.3-9)(4.3-10)(4.3-11). Here,  $Q_{pc}$  (W) represents

unexpected Joule loss of the designed structure in wire bondings, solder, etc. In fact,  $Q_{pc}$  is a coefficient to compensate the thermal model.

$$Q_c = S_m \cdot I \cdot T_c - \frac{1}{2} \cdot I^2 \cdot R_m - \lambda_m \cdot \Delta T - Q_{pc} \quad (4.3-8)$$

$$Q_{ed} = S_m \cdot I \cdot \Delta T + I^2 \cdot R_m \quad (4.3-9)$$

$$Q_h = S_m \cdot I \cdot T_h + \frac{1}{2} \cdot I^2 \cdot R_m - \lambda_m \cdot \Delta T + Q_{pc} \quad (4.3-10)$$

$$V_m = S_m \cdot \Delta T + I \cdot R_m \quad (4.3-11)$$

By thermal to electrical analogy shown in Table 4.5, a representative thermal resistance network in steady state for the total structure with Peltier devices (Fig.4-14) has been created with Matlab Simulink as shown in Fig.4-15.

Table 4.5. Thermal to electrical analogy

Thermal quantities	Units	Electrical quantities	Units
Heat Q	W	Current I	A
Temperature T	K	Voltage	V
Thermal resistance $R_{th}$	K/W	Resistance R	$\Omega$

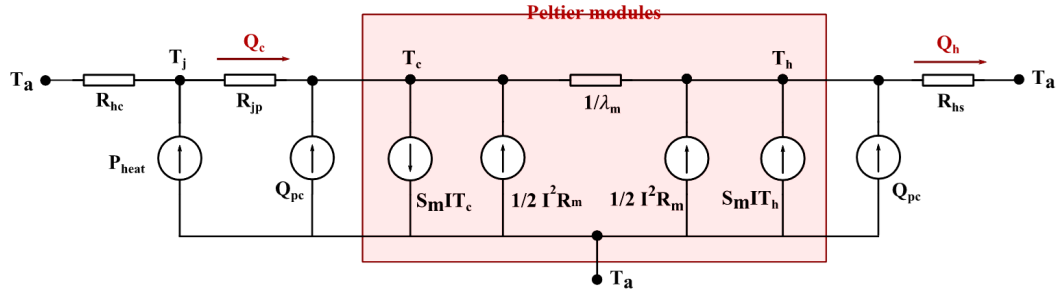


Fig.4-15. Thermal resistance network of the studied structure

where,  $T_a$  (K) is the ambient temperature;  $T_j$  (K) is the junction temperature;  $R_{hc}$  (K/W) is the thermal resistance representing the heat leakage due to heat convection effect;  $R_{jp}$  (K/W) is the lateral thermal resistance between the Peltier devices and the heating source;  $R_{hs}$  (K/W) is the thermal resistance of the heat sink and the cylinder duralumin column for power loss measurement.

As previously mentioned, thermal resistance for heat conduction can be derived by (4.3-12)(4.3-11).

$$R_{th} = \frac{\Delta T}{Q} = \frac{e}{\lambda_{th} \cdot A} \quad (4.3-12)$$

where,  $\Delta T$  is the temperature difference between the studied object or layer;  $e$  (m) is the thickness or length of material as heat flow path;  $A$  ( $m^2$ ) is the cross-section area, perpendicular to the heat flow path.

Based on (4.3-12),  $R_{hs}$  equals to  $0.21 \pm 0.05$  K/W. The lateral thermal resistance  $R_{jp}$  depends on the distance between the Peltier devices and the heating source  $l_{jp}$ . As shown in Fig.4-16,  $l_{jp}$  has been separated into lumped elements  $e_1$  (mm),  $e_2$  (mm) and  $e_3$  (mm) in consideration of the heat spreading effect. Empirically, the constant spreading angle is assumed to be  $45^\circ$  [177]. By calculation based on (4.3-12),  $R_{jp}$  varies approximately from 4 K/W to 8 K/W respect to the distance from 18 mm to 25 mm.

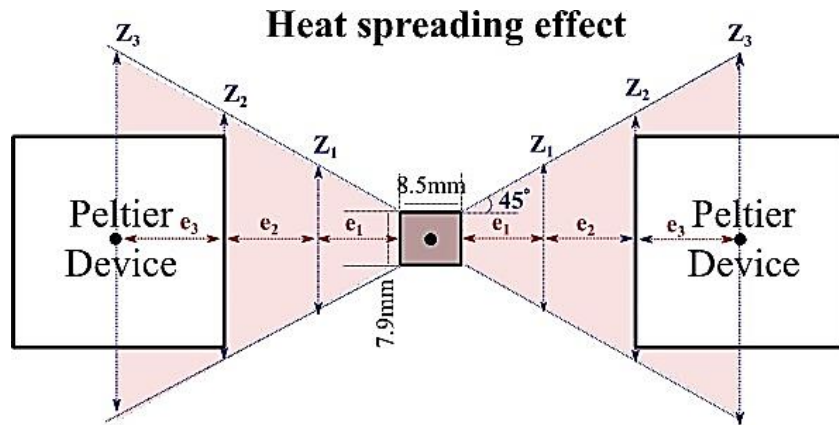


Fig.4-16. Top view for heating resistor and Peltier devices

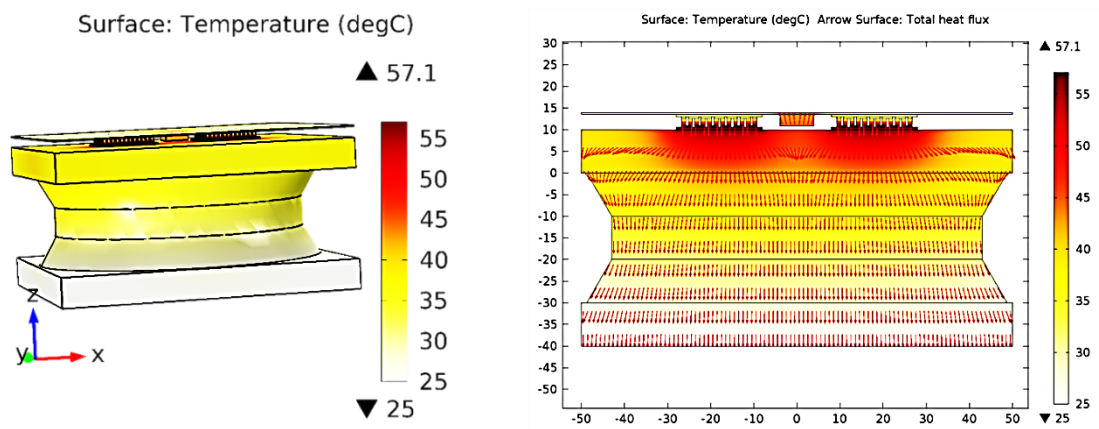


Fig.4-17. An example of 3D FEM simulation for the designed cooling structure and its section view. The PCB structure is put on a duralumin column for power loss measurement. The bottom side of the column is set at 25 °C. Heat power in the heat source  $P_{heat} = 7.6W$  and the input current in each Peltier device is 1.5 A.

Then, in order to define the thermal network components  $R_{hc}$  and  $Q_{pc}$ , comparisons of the simulation results between 1D and 3D have been carried out for the same cooling structure. 3D FE models of the proposed cooling structure have been built with COMSOL as shown in Fig.4-17. Same geometric Peltier parameters in Table 4.2 and material properties in Table 4.4 have been applied.

#### 4.3.2. 1D and 3D Simulation Results and Discussions

Sophisticated 3D models are precise but time-consuming for 3D FEM simulations due to the relative small meshes for the Peltier elements and the coupling effects between thermal and electrical domains. In contrast, simplified 1D thermal resistance network is fast and concise. However, there exists a trade-off between the fast 1D calculations and its simulation accuracy. Therefore, by comparing simulation results in use of the two methods, this section is dedicated to find out the undefined values of the thermal components  $R_{hc}$  and  $Q_{pc}$  in order to complete the previous built analytical model (Fig.4-15). The purpose is to develop a 1D thermal resistance network so that we can carry out a fast estimation of the thermal performances as well as the cooling efficiency in steady state. Fig.4-18 represents the 1D thermal model of the total cooling structure (Fig.4-15) built with Simulink.

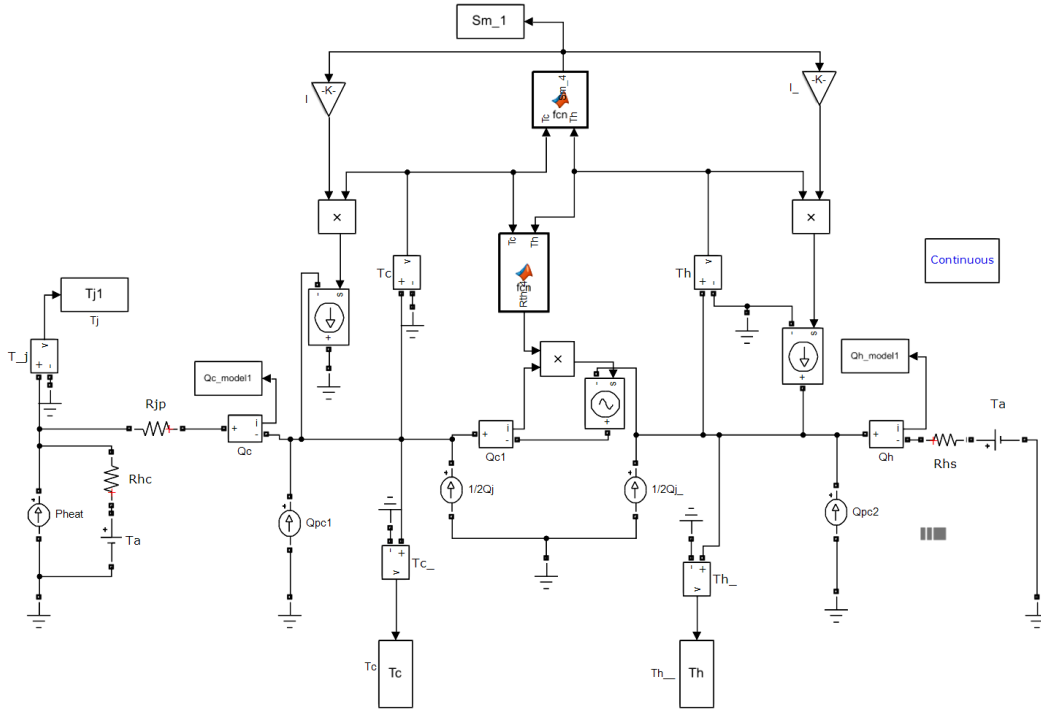


Fig.4-18. 1D electro-thermal model of the cooling structure built by Matlab Simulink

Thermoelectric material properties listed in Table 4.4 are firstly considered as constant for thermal simulations. With the same boundary condition of the ambient temperature  $T_a$  equaling to  $25\text{ }^\circ\text{C}$ , simulation results of estimated junction temperatures for different dissipated power are shown in Fig.4-19.

Firstly, as we can see in Fig.4-19.(a) and Fig.4-19.(c), junction temperature  $T_j$  of the heating resistor can be reduced by  $20\text{ }^\circ\text{C}$  when feeding the Peltier modules with a proper input current. These figures show that junction temperature is controllable with quick and silent operation of Peltier devices. In other words, from the point view of cooling power modules, the Peltier devices provide the possibility to control the thermal resistance of the total structure, especially for PCB structures.

Secondly, modeling errors for junction temperature predictions between 1D and 3D are less than  $10\%$  ( $\pm 4\text{ }^\circ\text{C}$ ) when heat leakage due to the thermal resistance  $R_{hc}$  is equal to 5 times  $R_{jp}$  and unexpected Joule loss  $Q_{pc}$  equals to 0.65 times the Joule heating of Peltier devices  $I^2 R_m$  (W). Meanwhile, errors for cooling efficiency estimations of COP between two models are smaller than 0.2 as shown in Fig.4-19.(b) and Fig.4-19.(d). From these results, the 1D thermal network of the total cooling structure as shown in Fig.4-15 can be completed with pre-calculations ( $R_{jp}$ ,  $R_m$ ,  $\lambda_m$ ,  $S_m$ ) and approximate components values ( $R_{hc}$ ,  $Q_{pc}$ ) according to the 3D thermal simulations.

Thirdly, the cooling efficiency of Peltier device is represented by its COP value, defined as the ratio of the absorbed heat power  $Q_c$  to the input electrical power  $P_{in}$ . It decreases as the applied DC current increases. And COP value depends on the desired junction temperature as well as the heat power loss to be dissipated. For example, for dissipating  $5\text{ W}$  from the heating source and keeping  $T_j$  at  $30.4\text{ }^\circ\text{C}$ , COP is about 1.45, consuming  $3\text{ W}$  of electrical power. But for keeping  $T_j$  at  $21\text{ }^\circ\text{C}$  when dissipating the same  $5\text{ W}$  heat power from the heating source, COP equals 0.27, consuming  $18\text{ W}$  of electrical power, which is more than 3 times the dissipated power. This is the main drawback of Peltier devices with low COP.



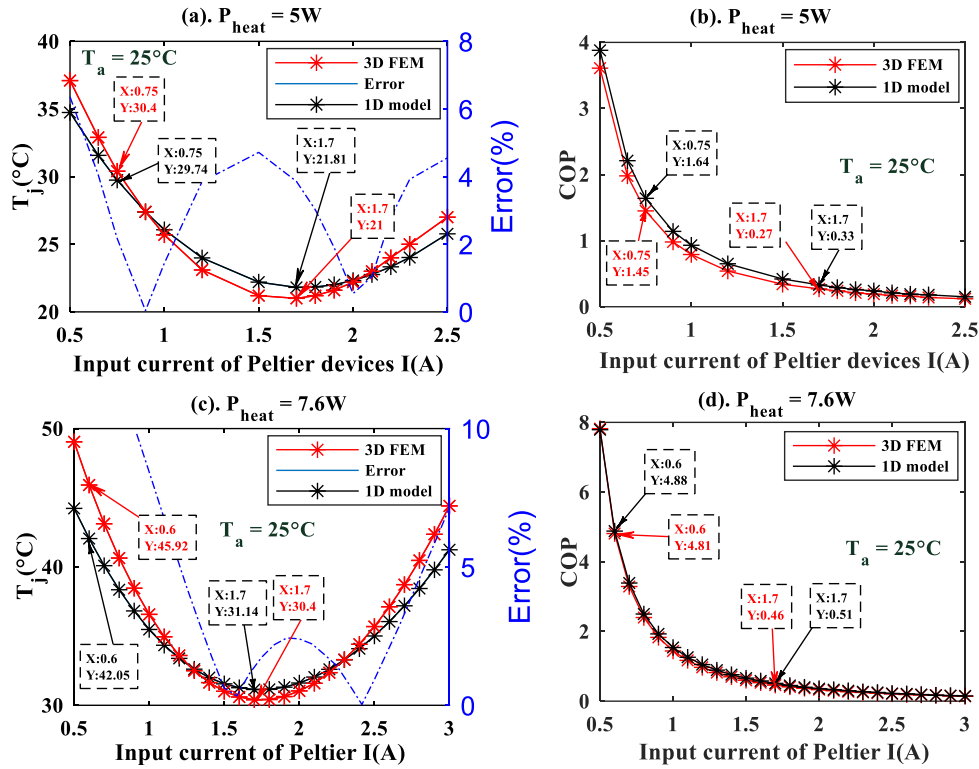


Fig.4-19. Thermal simulations for 1D analytical and 3D FE models. (a). Junction temperature profile  $T_j(I)$  when dissipating 5 W from the heating source; (b). Cooling efficiency profile COP ( $I$ ) when dissipating 5 W from the heating source; (c). Junction temperature profile  $T_j(I)$  when dissipating 7.6 W from the heating source; (d). Cooling efficiency profile COP ( $I$ ) when dissipating 7.6 W from the heating source. The ambient temperature is 25 °C.

In addition, for each input current  $I$  (A), 3D FE model needs at least 25 minutes for calculation. By contrast, the 1D thermal resistance network requires at most 5 minutes for all values of input current  $I$  varying from 0 A to 3 A. Despite the limited accuracy of the 1D thermal model, its simplicity is useful to provide fast estimations.

Here, as the same material  $\text{Bi}_2\text{Te}_3$  is used for fabricating all different Peltier devices, only 3D simulation results for CP39236H have been compared to validate the 1D thermal resistance network in order to avoid repeating long time-consuming simulations. Therefore, for the following sections, the approximated relations between  $R_{hc}$  and  $R_{jp}$ , as well as the relationship between  $Q_{pc}$  and  $I^2 R_m$  will be applied in the 1D models for the different Peltier devices. More studies in the next sections will be devoted to optimize the application of Peltier devices to obtain a desired junction temperature for different dissipated heat power.

## 4.4. EXPERIMENTAL VALIDATION

### 4.4.1. Test Bench

Based on the schematic of the total cooling structure (Fig.4-1), a test bench has been established as shown in Fig.4-20 to validate previous thermal models, especially the 1D thermal models. The heat is firstly forced along the copper layer from the heating resistor to the Peltier devices and then dissipated to the duralumin column by thermal conduction and finally to the ambient by natural convection. The top side of this cooling structure is covered with a glass wool to avoid the heat convection with the air. Junction temperature  $T_j$  is measured by using a thermocouple and column temperatures with two PT100 platinum resistance (RTD). In order to obtain the cooling efficiency COP of the Peltier device by (1.4-17), its pumped power  $Q_{ed}$ , equivalent to its consumed electrical power  $P_{in}$ , and also the total evacuated heat power  $Q_h$  are needed.  $P_{in}$  is measured by voltmeter and amp meter and  $Q_h$  is measured based on the calorimetric method.

It is assumed that all power loss will pass through the column by heat conduction. Fig.4-21 depicts the calorimetric method used for power loss measurement in this case. So  $Q_h$  is obtained by measuring temperature difference between the two RTDs  $\Delta T_{RTD}$ . The thermal resistance between the two RTDs  $R_{th\_du}$  has been previously determined and is equal to  $0.187 K/W$ .

Different current  $I$  varying from  $0 A$  to  $2.5 A$  has been input into the Peltier devices CP39236H to obtain the variation tendency of the junction temperature and to assess their cooling performances. It is noted that each measurement should be carried out when the thermal system achieves its steady state. Note that it takes one hour to stabilize each measurement.

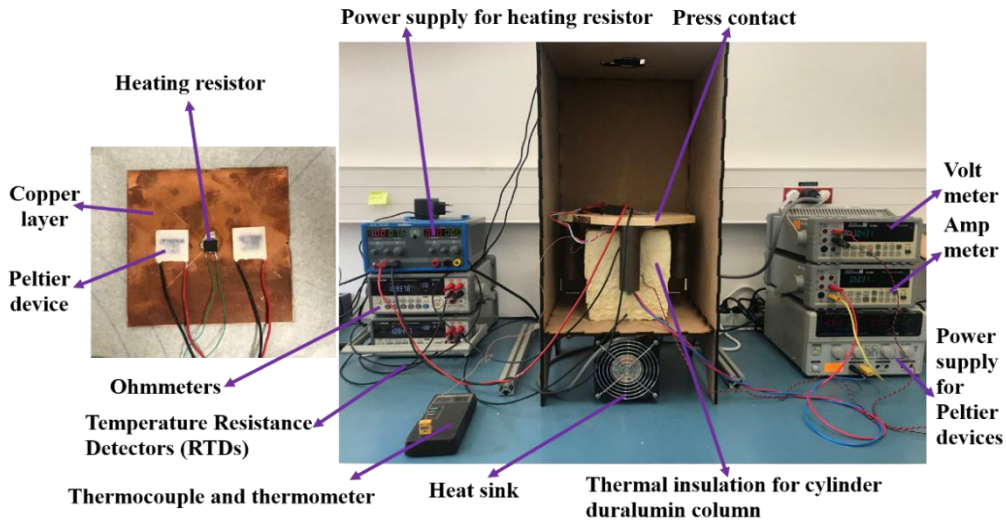


Fig.4-20. Test bench for validating the thermal models of the PCB structure with Peltier devices

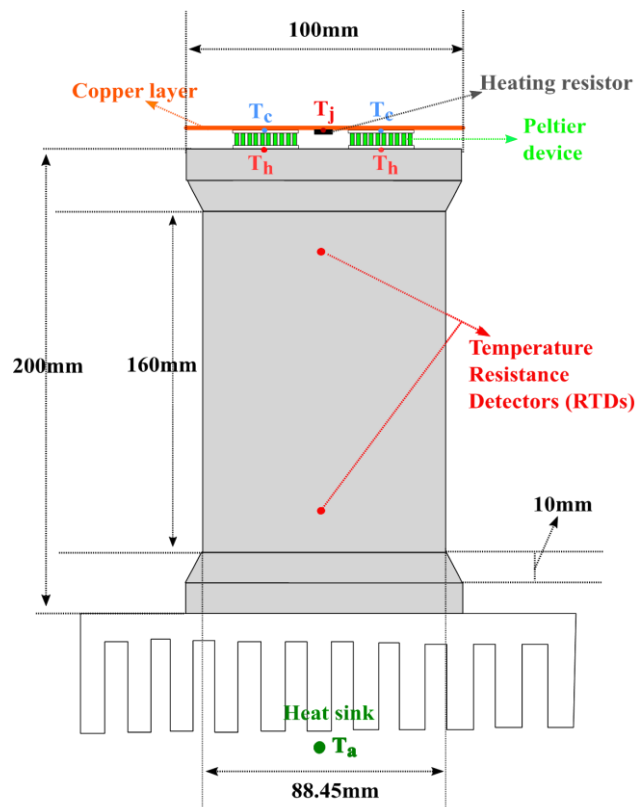


Fig.4-21. Power loss measurement based on calorimetric method with duralumin column

## 4.4.2. Results and Discussions

In fact, thermoelectric properties such as Seebeck coefficient  $S_e$ , thermal conductivity  $\lambda_{th}$  and electrical resistivity  $\rho$  are temperature interdependent. Besides, the three properties have also been proved to be tightly coupled with each other [143, 144]. Therefore, previous constant values calculated from the product datasheet are no longer reasonable to be applied for comparing the estimated responses with the experimental ones. Due to the lack of real values of the three properties from the product datasheet, here in our cases for thermal estimations, the Peltier figure-of-merit  $ZT$  value is fitted by a second degree polynomial using Matlab, from 0.5 to 2 for a temperature interval from 300 K to 400 K.

Variations of junction temperature  $T_j$  and COP profile for CP39236H, CP30238 modules are shown in Fig.4-22 and Fig.4-23, respectively. For 1D and 3D model, ambient temperature is assumed to be constant equal to 25 °C. The plotted curve corresponding to the measured values are calculated by averaging five measurements. It is noted that 3D FEM simulation gives predictions of the junction temperature with an error less than 1 % ( $\pm 1^\circ\text{C}$ ). By contrast, the 1D thermal resistance model gives a higher prediction error which is less than 10 % ( $\pm 4^\circ\text{C}$ ) on the whole current interval. This difference is mainly attributed to the errors between 3D and 1D models as observed from Fig.4-19. Besides, the errors of COP values between the 1D model and experimentations are also less than 10 % ( $\pm 0.1$ ). Therefore, with an accuracy tolerance of 10 % for the predictions of the junction temperature as well as the COP values, 1D thermal models can be validated and applied.

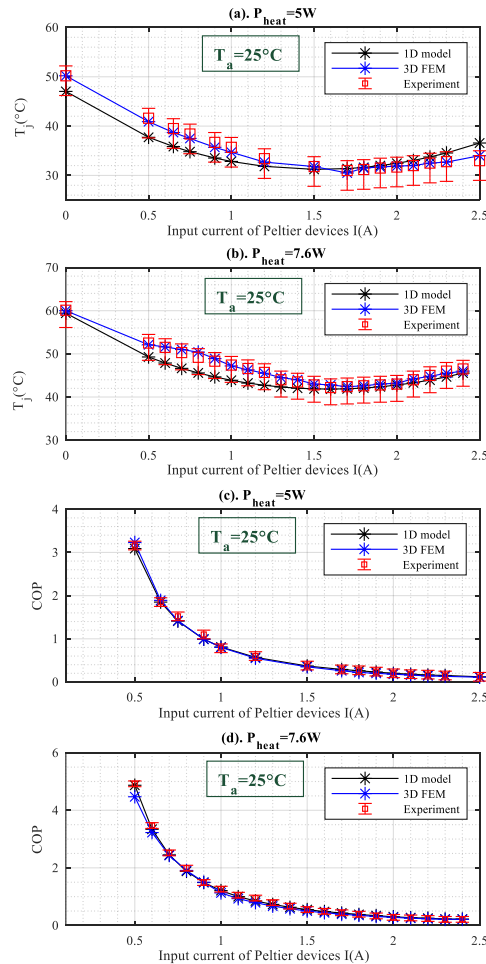


Fig.4-22. Experimental and estimated results with Peltier devices CP39236H. (a). Junction temperature profile  $T_j(I)$  when dissipating 5 W from the heating source; (b). Cooling efficiency profile COP ( $I$ ) when dissipating 5 W from the heating source; (c). Junction temperature profile  $T_j(I)$  when dissipating 7.6 W from the heating source; (d). Cooling efficiency profile COP ( $I$ ) when dissipating 7.6 W from the heating source. The ambient temperature is 25 °C.

As we can see in Fig.4-23.(a), for the Peltier device CP39236H with 72 pairs of Peltier elements ( $N = 288$ ), the optimum cooling effect is achieved when  $P_{in}$  is about  $15\text{ W} (\pm 1\text{ W})$ . The junction temperature  $T_j$  decreases from  $66.6\text{ }^\circ\text{C}$  to  $46.6\text{ }^\circ\text{C}$  when dissipating  $8\text{ W}$  from the heating source, from  $55.5\text{ }^\circ\text{C}$  to  $35.8\text{ }^\circ\text{C}$  when dissipating  $6\text{ W}$  and from  $40.5\text{ }^\circ\text{C}$  to  $23\text{ }^\circ\text{C}$  when dissipating  $3.3\text{ W}$ , respectively. The junction temperature can be reduced by  $20\text{ }^\circ\text{C}$  at the optimum point.

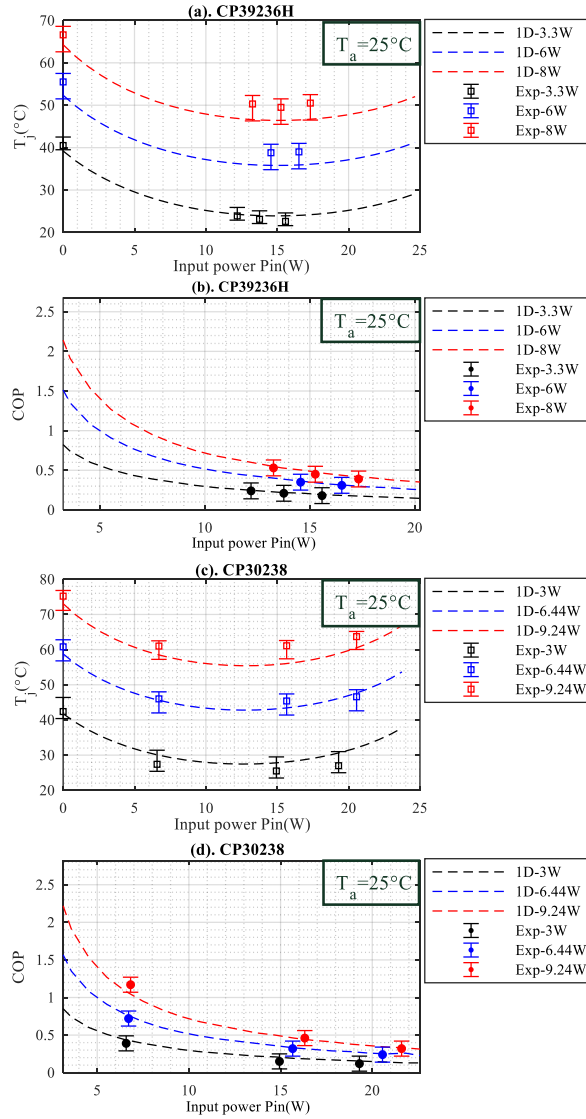


Fig.4-23. Experimental and estimated results with Peltier devices CP39236H and CP30238. (a). Junction temperature profile  $T_j$  ( $P_{in}$ ) with CP39236H; (b). Cooling efficiency profile COP ( $P_{in}$ ) with CP39236H; (c). Junction temperature profile  $T_j$  ( $P_{in}$ ) with CP30238; (d) Cooling efficiency profile COP ( $P_{in}$ ) with CP30238. The ambient temperature is  $25\text{ }^\circ\text{C}$ .

By contrast, for CP30238 also having 72 couples of Peltier elements ( $N = 288$ ), the optimum cooling effect is achieved when  $P_{in}$  is approximately  $13\text{ W} (\pm 1\text{ W})$ . At this optimum point, Fig.4-23.(c) depicts that the junction temperature  $T_j$  is decreased from  $75.2\text{ }^\circ\text{C}$  to  $55.4\text{ }^\circ\text{C}$  when dissipating  $9.24\text{ W}$  from the heating source, from  $60.8\text{ }^\circ\text{C}$  to  $42.8\text{ }^\circ\text{C}$  when dissipating  $6.44\text{ W}$ , and from  $42.4\text{ }^\circ\text{C}$  to  $27.5\text{ }^\circ\text{C}$  when dissipating  $3\text{ W}$ , respectively.

The two products CP39236H and CP30238 have almost the same cooling effects because they are fabricated with the same material and they have the same number of Peltier elements. The small difference between them is attributed to their internal electrical resistance.

Fig.4-24 depicts the temperature profile  $T_j$  ( $P_{in}$ ) calculated for different heat power dissipated by the heating resistor with CP39236H. First of all, the 1D thermal model can

provide fast estimations of the junction temperatures regarding different dissipated heat power. Secondly, the junction temperature is controllable with Peltier devices. For example, if  $T_j$  is required to be kept less than or equal to  $71^\circ\text{C}$ , an electric power of  $1.75\text{ W}$  needs to be applied for dissipating a heating power of  $11\text{ W}$ ;  $3.6\text{ W}$  is needed to dissipate  $12\text{ W}$ ;  $7.5\text{ W}$  is needed for  $13\text{ W}$  and  $15\text{ W}$  for  $14\text{ W}$ . Obviously, more electrical power is demanded to maintain the junction temperature as the heat power loss increases. The ratio between electrical power and drawn power deteriorates as the power increases due to the deterioration of the COP values with the level of electrical power injected.

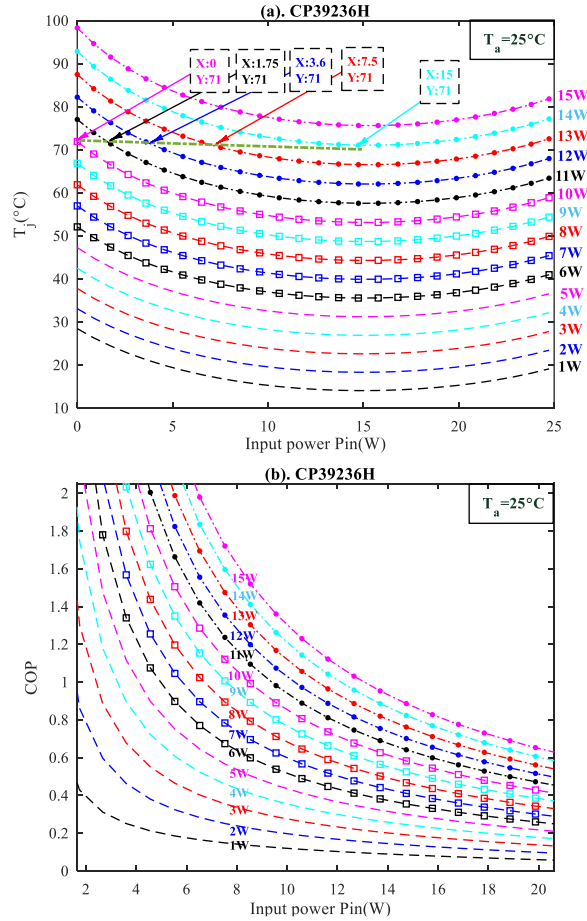


Fig.4-24. Estimated results with Peltier device CP39236H. (a). Junction temperature profile  $T_j$  ( $P_{in}$ ). (b). Cooling efficiency profile COP ( $P_{in}$ ). The ambient temperature is  $25^\circ\text{C}$ .

In addition, no electrical power is needed when the heat power is equal or less than  $10\text{ W}$ . In this case, the Peltier devices can be shut down to economize electrical energy. It means that the electrical feeding power of Peltier devices could be controlled a depend on the designed junction temperature and the heat power loss to be dissipated. This is the second big benefit of using Peltier devices in PCB structures. However, when the dissipated power is more than  $14\text{ W}$ , the applied Peltier devices are no more able to control the junction temperature at less than  $71^\circ\text{C}$ . In this case, it is suggested that more powerful Peltier devices should be applied. Otherwise, extra cooling methods to enhance the cooling effects are required. In [117], WANG has proposed a package design of a hybrid cooling solution which combines a thin-film superlattice TEC device with a cold plate liquid cooling to reduce the temperature of the high-power IGBT chip with a maximum power dissipation of  $200\text{ W}/\text{cm}^2$ .

#### 4.4.3. Influences of Number of Peltier Elements N

As previously, a 1D thermal model to predict the thermal performances of a cooling structure using two Peltier devices CP60133 beside the heating resistor has been validated.

As shown in Fig.4-25, the optimum cooling effect for this module is achieved when  $P_{in}$  is  $13\text{ W}$  ( $\pm 1\text{ W}$ ). As we can see in Fig.4-25.(c), the junction temperature  $T_j$  can be decreased from  $58\text{ }^\circ\text{C}$  to  $41\text{ }^\circ\text{C}$  when dissipating  $5.12\text{ W}$  from the heating resistor, from  $62\text{ }^\circ\text{C}$  to  $46\text{ }^\circ\text{C}$  when dissipating  $6\text{ W}$ , and from  $70\text{ }^\circ\text{C}$  to  $55.5\text{ }^\circ\text{C}$  when dissipating  $8\text{ W}$ , respectively.  $T_j$  can be reduced by  $17\text{ }^\circ\text{C}$  at the optimum point. The cooling performance is not as good as that of CP3926H or CP30238 when dissipating the same heat power. In other words, less heat power can be pumped when there are less Peltier elements ( $128$  instead of  $288$ ).

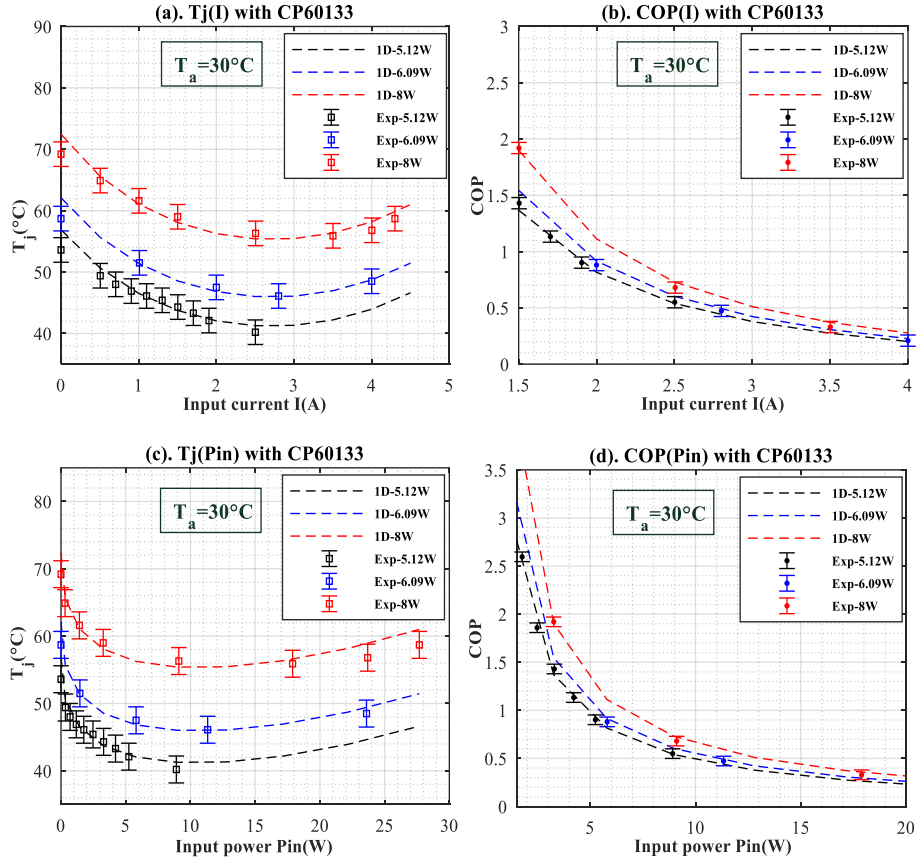


Fig.4-25. Experimental and estimated results with Peltier devices CP60133. (a). Junction temperature profile  $T_j(I)$ ; (b). Cooling efficiency profile  $\text{COP}(I)$ ; (c). Junction temperature profile  $T_j(\text{Pin})$ ; (d) Cooling efficiency profile  $\text{COP}(\text{Pin})$ . The ambient temperature is  $30\text{ }^\circ\text{C}$ .

To further study the impact of  $N$ , the cooling scenarios with two ( $N = 128$ ), three ( $N = 192$ ) and four ( $N = 256$ ) CP60133 Peltier devices have been simulated to compare their thermal performances when dissipating the same heat power from the heating source. Based on the 1D thermal model (Fig.4-15) and the heat spreading effect (Fig.4-16), it is assumed that the thermal resistance  $R_{jp}$  decreases but the thermal resistance  $R_{hc}$  increases when using more Peltier devices. For example, compared to the structure with 2 CP60133 Peltier devices,  $R_{jp}$  is halved and  $R_{hc}$  is doubled in the cases of using 4 Peltier devices. The estimated junction temperature  $T_j$  and also the corresponding cooling efficiency COP are presented in Fig.4-26 and Fig.4-27. COP is calculated by (4.1-1) and absorbed heat power at the cold sides of Peltier modules  $Q_c$  is the difference between the measured heat power passing through the duralumin column  $Q_h$  and the input electric power  $P_{in}$  ( $Q_{ed}$ ).

Firstly, as we can see in Fig.4-26.(a) to Fig.4-26.(d), the junction temperature can be reduced when the input current is in the range  $0$  to  $2.5\text{ A}$ . Then it rises again when the input current exceeds  $2.5\text{ A}$ . We also find that the COP value don't change a lot with the number of Peltier elements  $N$  as observed in Fig.4-26.(e) to Fig.4-26.(h) as it is mainly an intrinsic characteristic of each Peltier device. The Joule losses increase for a given current

proportionally to the number of elements of the structure but the power with drawn from the cold plate also increases proportionally. The maximum decrease of junction temperature  $\Delta T_{jmax}$  achieved by the three cooling scenarios is summarized in Table 4.6. From these results we can conclude that cooling performance can be enhanced by more  $N$  with the same product CP60133.

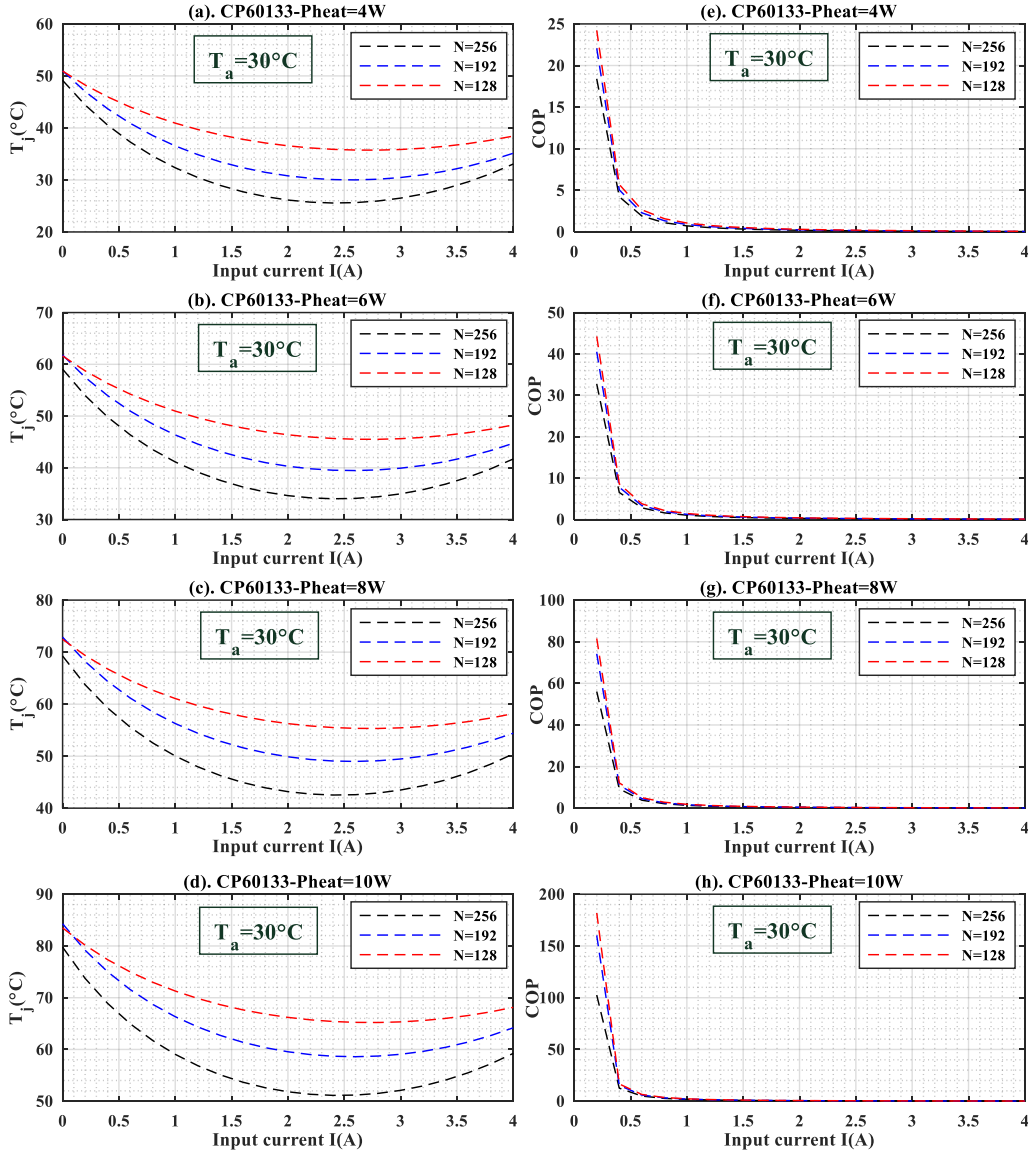


Fig.4-26. Estimated results with Peltier devices CP60133. (a). Junction temperature profile  $T_j(I)$  for dissipating 4 W; (b). Junction temperature profile  $T_j(I)$  for dissipating 6 W; (c). Junction temperature profile  $T_j(I)$  for dissipating 8 W; (d). Junction temperature profile  $T_j(I)$  for dissipating 10 W; (e). Cooling efficiency profile  $COP(I)$  for dissipating 4 W; (f). Cooling efficiency profile  $COP(I)$  for dissipating 6 W; (g). Cooling efficiency profile  $COP(I)$  for dissipating 8 W; (h). Cooling efficiency profile  $COP(I)$  for dissipating 10 W. The ambient temperature is 30 °C.

Table 4.6. Maximum decrease of the junction temperature  $\Delta T_{jmax}$  (°C)

N	$P_{heat} = 4W$	$P_{heat} = 6W$	$P_{heat} = 8W$	$P_{heat} = 10W$
128	15.2	16.1	17.1	18.3
192	21	22.3	23.9	25.7
256	23.6	25.1	26.7	28.7

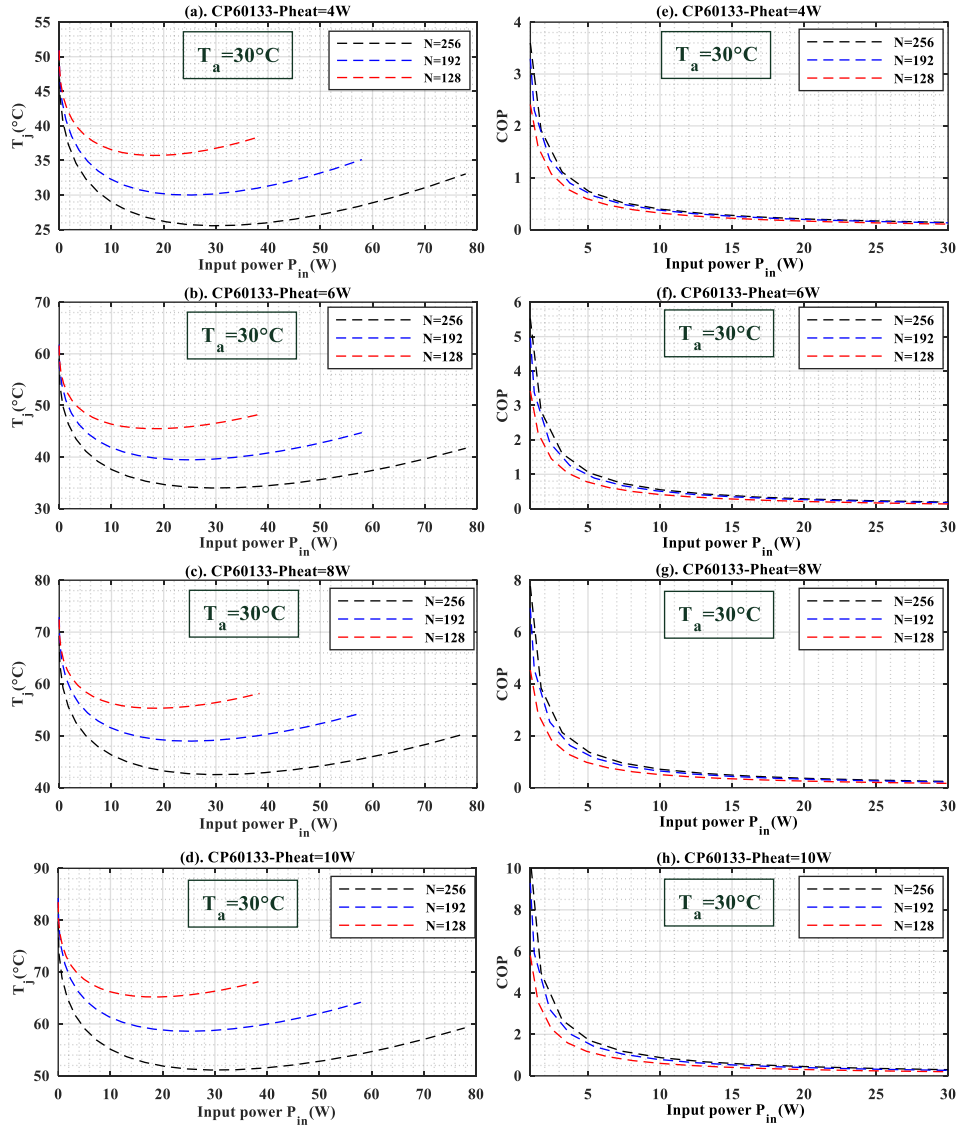


Fig.4-27. Estimated results with Peltier devices CP60133. (a). Junction temperature profile  $T_j$  ( $P_{in}$ ) for dissipating 4 W; (b). Junction temperature profile  $T_j$  ( $P_{in}$ ) for dissipating 6 W; (c). Junction temperature profile  $T_j$  ( $P_{in}$ ) for dissipating 8 W; (d). Junction temperature profile  $T_j$  ( $P_{in}$ ) for dissipating 10 W; (e). Cooling efficiency profile COP ( $P_{in}$ ) for dissipating 4 W; (f). Cooling efficiency profile COP ( $P_{in}$ ) for dissipating 6 W; (g). Cooling efficiency profile COP ( $P_{in}$ ) for dissipating 8 W; (h). Cooling efficiency profile COP ( $P_{in}$ ) for dissipating 10 W. The ambient temperature is 30 °C.

Table 4.7. COP values of the three cooling scenarios when keeping  $T_j$  at 55 °C

Pheat (W)	COP		
	N=128	N=192	N=256
4	Infinity ( $P_{in}=0$ )	Infinity	Infinity
6	5.5	16.21	Infinity
8	0.26	1.27	3.84
10	Inability	Inability	0.88

In addition, the cooling efficiency COP is enhanced for the same cooling performance of the three different cooling scenarios. For designed junction temperature  $T_j$  of 55 °C, according to the junction temperature evolutions in Fig.4-27.(a) to Fig.4-27.(d), COP values and consumed electrical power of the three cooling scenarios are summarized in Table 4.7. For example, in the case of dissipating 8 W heating power, COP equals 3.84 when  $N$  is 256 but 0.26 when  $N$  is 128. In other words, less electrical power is consumed when using more



Peltier devices for the same cooling performance. The cooling structure with more Peltier devices is more efficient for a given heat power while keeping the junction temperature at an identical temperature.

Ideally, as described in (4.3-8),  $S_m$  can be increased with more  $N$  leading to enhance the capability of absorbing the heat power. However, the Joule heating and heat conduction leakage due to  $R_m$  and  $\lambda_m$  have also been increased at the same time because of the interdependent thermoelectric properties between Peltier parameters  $S_e$ ,  $\lambda_{th}$ , and  $\rho$ . For example, for the two Peltier devices of CP60133 beside the heating resistor,  $S_m$  equals  $0.0236$  V/K,  $R_m$  equals  $0.98$   $\Omega$ ,  $\lambda_m$  equals  $0.246$  W/K. By contrast, when four devices of CP60133 are applied,  $S_m$ ,  $R_m$  and  $\lambda_m$  are doubled to  $0.0472$  V/K,  $1.96$   $\Omega$  and  $0.492$  W/K, respectively. This explains the phenomenon of the cooling performances when increasing  $N$  as shown in Fig.4-26 and Table 4.6. The increased Joule heating and heat conduction leakage due to  $R_m$  and  $\lambda_m$  will militate against further enlargement of the heat pump ability influenced by Peltier effect  $S_m$ . This explains also the small difference of the cooling performances between CP60133 (Fig.4-25) and CP30238 (Fig.4-23) because their Peltier elements have almost the same  $ZT$  value. A higher  $ZT$  leads directly to a higher conversion efficiency. But the main challenge lies in the decoupling of the interdependent thermoelectric parameters [143]. There are also people working to optimize the geometrical factor  $G$  to increase the conversion efficiency. Authors in [178] found that the optimum Peltier module length is between  $0.612$  mm and  $1.76$  mm and the maximum heat dissipation density should be  $3.70$  to  $5.52$  W/cm<sup>2</sup> with a  $ZT$  of  $0.8$  to  $3.0$ .

Here, for cooling the PCB structures, it is proposed to apply the devices according to the desired junction temperature with minimum consumed electrical power.

#### 4.5. SUMMARY

In this chapter, thermal management solution with Peltier devices beside the heating source for PCB structures has been proposed. A 1D thermal resistance network has been developed to represent the total cooling system and predict its cooling performances. Compared to the 3D FE Model, this electro-thermal model is a good compromise between calculation time and estimation accuracy.

Benefit of using Peltier devices lies in that they provide a local cooling capability with the ability to control the junction temperature control. But it exists a trade off between the junction temperature control and the cooling efficiency. Design of such solutions requires an optimization stage in order to obtain the maximum cooling effect and the maximum cooling efficiency according to the designed junction temperature and dissipated heat power.

The results of the study demonstrate that the thermal performance of the system is heavily dependent on the Peltier parameters and on the rated temperature and dissipated power. Both input current and  $ZT$  of the chosen Peltier device should be carefully considered to arise an optimum cooling effect.

How such devices could be used for cooling integrated power boards? The main questions concern the cost of such solid state solutions and its low energetic efficiency. In fact, the initial cost of such solutions can be balanced by many new possibilities offered to Power Electronics and Thermal designers. Indeed, Peltier modules offer the possibility of dynamically controlling the temperature on a semiconductor die or a part of an assembly. In a long-term point of view, using such technological solution may decrease the thermal constraints due to thermal cycling in power converters and the cost of using Peltier devices could be covered by saving system maintenance cost. If a dynamic thermal control is applied to the thermal assembly using PCB and Peltier devices, such base plate can be seen as an

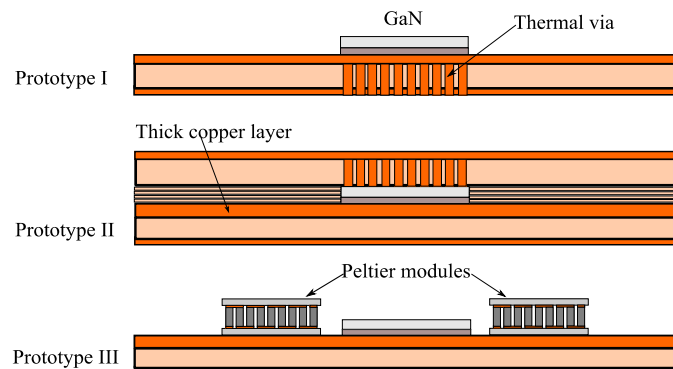
active substrate with a controlled thermal resistance that can reach the thermal performances of DBC substrates.

## CONCLUSIONS AND PERSPECTIVES

## CONCLUSIONS AND PERSPECTIVES

PCB technology is attractive for high power density integration thanks to its flexibility and low cost. 3D integration by PCB technology without wire bondings can improve the electrical interconnections as well as reduce the parasitic loop inductances because of its multilayer and its ability of embedding devices. In this 3D integration context, it indicates the tendency in power integration technologies toward use of PCB technology. However, the poor thermal conductivity of PCB substrate ( $< 1 \text{ W/mK}$ ), which is usually in glass-reinforced epoxy laminate material of Flame Retardant-4 (FR4), brings big challenges for the thermal management of the total power system. Besides, the emerging of high switching speed wide bandgap (WBG) devices brings out more severe operating environment. So thermal management is an important design to ensure the system reliability as well as its final performance efficiency.

The current researches focus on the development of thermal management solutions for PCB structures adapted to new wide-bandgap power devices and more severe operating environment. Three types of assemblies based on PCB technology have been proposed and discussed regarding cooling performances as shown in the following figure. In the first configuration (Prototype I), the thermal vias are created in the PCB substrate to increase the thermal conductivity of the complete structure. In the second configuration (Prototype II), influence of the PCB copper thickness ( $35 \mu\text{m}$  to  $500 \mu\text{m}$ ) has been discussed. Moreover, a double-sided cooling configuration has been introduced by combining the effects of thermal vias and the use of thick copper. In the third configuration (Prototype III), Peltier devices have been applied for local cooling of the heating source. The studies of the thermal performances are mainly based on 1D analytical and 3D FEM analysis to identify the influences of different significant parameters of each structure such as via parameters (via diameter, via plating thickness, via-cluster surface formed by multiple vias, via pattern, pitch distance between vias etc.), Peltier parameters (Thermoelectric material properties, number of Peltier elements, distance between the heating source and the Peltier devices etc.).



The solution by creating thermal vias in the PCB substrate has been optimized to improve their cooling performances. It has been demonstrated according to the normalized relationships between the thermal resistance of the total structure and the via parameters that thermal vias are more efficient when the number of vias are more than 35 with larger via-cluster surface ratio, plating thickness ratio, as well as via diameter ratio in pattern 2. This optimization gives us a guideline for fabricating the thermal vias.

The second solution has enhanced the thermal performances of the PCB structures by increasing the lateral heat flux along the thick copper layer on the PCB substrate instead of the standard thickness of  $35 \mu\text{m}$  or  $38 \mu\text{m}$ . It is efficient for PCB substrate because of the

much better thermal conductivity of the copper material than that of FR4. In addition, this solution is easy to realize and can be combined with other cooling solutions.

The third solution by using the thermoelectric cooler (TEC) like Peltier devices is a solid-state cooling technology that can meet the local cooling requirements. Two previous cooling solutions focus on dissipating heat towards the gravity direction for the total structure. By the upward thermal path, TEC device addresses the thermal challenge that exists near the junction of the power module. They have advantages of simple integration, little maintenance, silent operation and excellent reliability. Besides, TEC devices have fast and accurate temperature control without neither moving parts nor working fluids. Moreover, for the same dielectric strength, the PCB substrate with TEC devices and thick copper layer can be competitive with the DBC substrate. Along with the advantages that TEC brings in, there are existing issues that should be considered including design optimization and overall efficiency of the system due to extra electrical consumption by the device itself. This is related to its low efficiency COP, usually less than one. Here, it is demonstrated that we can apply the Peltier devices according to the designed junction temperature as well as the dissipated heat power from the heat source in order to lower the consumed electrical power. In addition, it has been proven that TEC can quickly decrease the junction temperature even below the designed temperature with more input power. In other words, by controlling the temperature distribution on the surface of PCB substrate, TEC cooling technology provides also a method to control the thermal resistance of the total PCB substrate. All these analyses demonstrate the potential application of Peltier devices placed beside the heating source for PCB structures, which is a benefit for developing the embedding technology in such structures.

In the long term, Peltier device has fast thermal dissipation and active operation which makes it possible to set up an active control of the temperature thus making it possible to limit the negative impacts of thermal cycling on an assemblies.

This thesis focuses mainly on the thermal management of PCB structures. In experiments, a heating resistor instead of the WBG device has been applied to simplify the thermal analysis. The next step should be the application of these cooling solutions to an integrated PCB structures with WBG components and even with some passive components. In addition, mechanical stress analysis caused by different Coefficient of Thermal Expansion (CTE) of the materials should be realized to avoid the crack of each laminated layer. Moreover, concerning the reasons of thermal problems of the PCB structures such as switching losses, parasitic losses and interconnection losses etc., electrical and magnetic problems accompanied with the packaging technologies should be analyzed and designed to improve the reliability and robustness of the total structure.

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# ANNEXES



## ANNEX A

**%%Inverting the problem for 5 measurement points on the PCB top layer**

```

A=[];
b=[];
Aeq=[];
beq=[];
lb=0;
ub=[];
x1=lsqlin(P,dT1,A,b,Aeq,beq,lb,ub);
x2=lsqlin(P,dT2,A,b,Aeq,beq,lb,ub);
x3=lsqlin(P,dT3,A,b,Aeq,beq,lb,ub);
x4=lsqlin(P,dT4,A,b,Aeq,beq,lb,ub);
x5=lsqlin(P,dT5,A,b,Aeq,beq,lb,ub);
a1=x1;%dT1=a1*P
a2=x2;%dT1=a2*P
a3=x3;%dT1=a3*P
a4=x4;%dT1=a4*P
a5=x5;%dT1=a5*P
%Fitting coefficient for determined physic model Ymp=P/kmp*Cmp
Cmp1=lsqlin(P/kmp,dT1);
Cmp2=lsqlin(P/kmp,dT2);
Cmp3=lsqlin(P/kmp,dT3);
Cmp4=lsqlin(P/kmp,dT4);
Cmp5=lsqlin(P/kmp,dT5);
%Function of inverse model %Inverse model for calculating the input power P=1.73W
global dTme1
dTme1=[3.917 0.014 0.008 0.004 1.604];%Measurement temperatures for 5 surface points
Pin=fmincon('myLsq_MM',[1],[],[],[0,10)
%One thousand loop times with random noises
n=1000;
options = optimset('TolFun',1e-3);
Mat=zeros(1,n); %empty matrix
for i=1:n
[Pin,FVAL,EXITFLAG]=fminsearch('myLsq_MM',[1]);%options);
    Mat(i)=Pin; %save loop results in matrix Mat
    EXIT(i)=EXITFLAG;
end
Re_IM=mean(Mat)%Average value of inverse model with noises
figure (1)
plot([1:1000],Mat,'b.',[1,1000],[Re_IM,Re_IM],'-k') %tracer courbe de proximité
hold on
plot([1,1000],[1.73,1.73],'-r')
ylim([1.5 2]);
xlabel('Loop times');ylabel('P(W)');
legend('Loop random value','Mean value of loop','Real input value')
title('Simulation loop with noises')
Er_I_E=(1.73-Re_IM)/1.73*100
errmax=(max(Mat)-1.73)/1.73*100
errmin=(min(Mat)-1.73)/1.73*100
%%Inverting the problem for 5 measurement points on the PCB top layer
%%Calling function 'myLsq_MM'

function [Er]=myLsq_MM(Pin) %Least square for calculating the error between measurement and
modelling

```

## ANNEX A – CONCEPTION OF THE INVERSE THERMAL MODEL

```
%global dTme1 %dTme2 dTme3 dTme4 dTme5
Bruit=0.05*randn(1,5);%(rand(1,5)-0.5)*0.05;%distributed noise with mean 0 and standard
deviation 1
dTme1=[3.917 0.014 0.008 0.004 1.604]+Bruit;%Measurement temperatures for 5 surface points
Amo=[2.2642 0.0081 0.0044 0.0025 0.9272];%Precious obtained fitting coefficients
dTmo1=Pin.*Amo;
Er=sum((dTmo1-dTme1).^2);
end
```

## ANNEX B

### %%Inverting the problem for 10 measurement points on the PCB top layer

% Dix points de mesure

%%

%%Estimation des paramètres d'un modèle par la méthode moindres carrés

P=[0; 1; 2; 3; 4; 5; 6; 7; 8; 9; 10;]; %Puissance dissipée par puce GaN

P1=[0 1 2 3 4 5 6 7 8 9 10];

Ta=20;%Temperature ambient

dT1=[0 2.264 4.528 6.793 9.057 11.321 13.585 15.849 18.114 20.378 22.642];%Température d'un point (0,0,0.86)mm sur la surface du système

dT2=[0 0.008 0.016 0.024 0.032 0.040 0.049 0.057 0.065 0.073 0.081];%Température d'un point (0,0,0.86)mm sur la surface du système

dT3=[0 0.004 0.009 0.013 0.018 0.022 0.027 0.031 0.035 0.040 0.044];%Température d'un point (0,0,0.86)mm sur la surface du système

dT4=[0 0.003 0.005 0.008 0.010 0.013 0.015 0.018 0.020 0.023 0.025];%Température d'un point (0,0,0.86)mm sur la surface du système

dT5=[0 0.927 1.854 2.781 3.709 4.636 5.563 6.490 7.417 8.344 9.272];%Température d'un point (0,0,0.86)mm sur la surface du système

dT6=[0 0.467 0.933 1.400 1.866 2.333 2.799 3.266 3.733 4.199 4.666];

dT7=[0 0.246 0.491 0.737 0.982 1.228 1.473 1.719 1.964 2.210 2.455];

dT8=[0 1.140 2.280 3.420 4.560 5.700 6.840 7.980 9.120 10.260 11.400];

dT9=[0 0.577 1.154 1.731 2.308 2.885 3.462 4.039 4.616 5.193 5.770];

dT10=[0 1.308 2.616 3.925 5.233 6.541 7.849 9.157 10.465 11.774 13.082];

%%

%Least Squares with Linear Inequality Constraints

A=[];

b=[];

Aeq=[];

beq=[];

lb=0;

ub=[];

x1=lsqlin(P,dT1,A,b,Aeq,beq,lb,ub);

x2=lsqlin(P,dT2,A,b,Aeq,beq,lb,ub);

x3=lsqlin(P,dT3,A,b,Aeq,beq,lb,ub);

x4=lsqlin(P,dT4,A,b,Aeq,beq,lb,ub);

x5=lsqlin(P,dT5,A,b,Aeq,beq,lb,ub);

x6=lsqlin(P,dT6,A,b,Aeq,beq,lb,ub);

x7=lsqlin(P,dT7,A,b,Aeq,beq,lb,ub);

x8=lsqlin(P,dT8,A,b,Aeq,beq,lb,ub);

x9=lsqlin(P,dT9,A,b,Aeq,beq,lb,ub);

x10=lsqlin(P,dT10,A,b,Aeq,beq,lb,ub);

a1=x1;%dT1=a1\*P

a2=x2;%dT1=a2\*P

a3=x3;%dT1=a3\*P

a4=x4;%dT1=a4\*P

a5=x5;%dT1=a5\*P

a6=x6;%dT1=a1\*P

a7=x7;%dT1=a2\*P

a8=x8;%dT1=a3\*P

a9=x9;%dT1=a4\*P

a10=x10;%dT1=a5\*P

```

Acf=[a1 a2 a3 a4 a5 a6 a7 a8 a9 a10];
%%
%Function of inverse model %Inverse model for calculating the input power P=1.73W
global dTme1
dTme1=[3.917 0.014 0.008 0.004 1.604 0.807 0.425 1.972 0.998 2.263];%Measurement
temperatures for 5 surface points
n=1000;
options = optimset('TolFun',0.5e-2, 'MaxFunEvals',100000,'MaxIter',10000);
Mat=zeros(1,n); %empty matrix
for i=1:n
    [Pin,FVAL,EXITFLAG]=fminsearch('myLsq_MM_10p',[1],options);%,options)
    Mat(i)=Pin; %save loop results in matrix Mat
end
Re_IM=mean(Mat)%Average value of inverse model with noises
Bande=max(Mat)-min(Mat)
Re_re=1.73;
plot([1:1000],Mat,'b.',[1,1000],[Re_IM,Re_IM],'-k',[1,1000],[Re_re,Re_re],'-r')%tracer courbe de
proximité
ylim([1.5 2]);
xlabel('Loop times');ylabel('P(W)');
legend('Loop random value','Mean value of loop','Real input value')
title('Simulation loop with noises')
Er_I_E=(1.73-Re_IM)/1.73*100
Errmax_min=max(Mat)-min(Mat)

```

**%%Inverting the problem for 10 measurement points on the PCB top layer**  
**% Calling function 'myLsq\_MM\_10p'**

```
function [Er]=myLsq_MM_10p(Pin) %Least square for calculating the error between measurement
and modelling
global dTme1
Bruit=0.05*randn(1,10);%(rand(1,5)-0.5)*0.01;%distributed noise with mean 0 and standard
deviation 1
dTme1=[3.917 0.014 0.008 0.004 1.604 0.807 0.425 1.972 0.998 2.263]+Bruit;%Measurement
temperatures for 10 surface points
Amo=[2.2642 0.0081 0.0044 0.0025 0.9272 0.4666 0.2455 1.14 0.577 1.3082];%Precious obtained
fitting coefficients
dTmo1=Pin.*Amo;
Er=sum((dTmo1-dTme1).^2);
end
```

## ANNEX C

### %%Power predictions in 2 embedded GaN dies with 5 temperature sensors

```

clear all;
%% Estimation des paramètres d'un modèle par la méthode moindres carrés
P=[0; 1; 2; 3; 4; 5; 6; 7; 8; 9; 10;]; % Puissance dissipée par puce GaN
P1=[0 1 2 3 4 5 6 7 8 9 10];
Ta=20;% Temperature ambiante
kmp=0.3;% thermal conductivity of the FR4 substrate
dT1=[0 2.264 4.528 6.793 9.057 11.321 13.585 15.849 18.114 20.378 22.642];% Temperature d'un
point (0,0,0.86)mm sur la surface du système
dT2=[0 0.008 0.016 0.024 0.032 0.040 0.049 0.057 0.065 0.073 0.081];% Temperature d'un point
(0,0,0.86)mm sur la surface du système
dT3=[0 0.004 0.009 0.013 0.018 0.022 0.027 0.031 0.035 0.040 0.044];% Temperature d'un point
(0,0,0.86)mm sur la surface du système
dT4=[0 0.003 0.005 0.008 0.010 0.013 0.015 0.018 0.020 0.023 0.025];% Temperature d'un point
(0,0,0.86)mm sur la surface du système
dT5=[0 0.927 1.854 2.781 3.709 4.636 5.563 6.490 7.417 8.344 9.272];% Temperature d'un point
(0,0,0.86)mm sur la surface du système

%%
n=1;% one degree for each fitting curve
f1=polyfit(P1,dT1,n);
f2=polyfit(P1,dT2,n);
f3=polyfit(P1,dT3,n);
f4=polyfit(P1,dT4,n);
f5=polyfit(P1,dT5,n);
% Least Squares with Linear Inequality Constraints
A=[];
b=[];
Aeq=[];
beq=[];
lb=0;
ub=[];

x1=lsqmin(P,dT1,A,b,Aeq,beq,lb,ub);
x2=lsqmin(P,dT2,A,b,Aeq,beq,lb,ub);
x3=lsqmin(P,dT3,A,b,Aeq,beq,lb,ub);
x4=lsqmin(P,dT4,A,b,Aeq,beq,lb,ub);
x5=lsqmin(P,dT5,A,b,Aeq,beq,lb,ub);

a1=x1;% dT1=a1*P
a2=x2;% dT2=a2*P
a3=x3;% dT3=a3*P
a4=x4;% dT4=a4*P
a5=x5;% dT5=a5*P

%%
% Fitting coefficient for determined physic model Ymp=P/kmp*Cmp
Cmp1=lsqmin(P/kmp,dT1);
Cmp2=lsqmin(P/kmp,dT2);
Cmp3=lsqmin(P/kmp,dT3);
Cmp4=lsqmin(P/kmp,dT4);
Cmp5=lsqmin(P/kmp,dT5);

```

```
%TwoGaN chips attached to PCB substrate
```

```
Pin1=[1 2 3 4 5 6 7 8 9 10];
```

```
Pin2=[1 2 3 4 5 6 7 8 9 10];
```

```
%Five points' temperatures on model surface
```

```
dTme1_2GaN=[0.214 0.321 0.428 0.534 0.641 0.748 0.854 0.961 1.068 1.174;0.322 0.429 0.535
0.642 0.749 0.855 0.962 1.069 1.175 1.282;0.430 0.536 0.643 0.750 0.856 0.963 1.070 1.176 1.283
1.390;0.537 0.644 0.751 0.857 0.964 1.071 1.177 1.284 1.391 1.497;0.645 0.752 0.858 0.965 1.072
1.178 1.285 1.392 1.498 1.605;0.753 0.859 0.966 1.073 1.179 1.286 1.393 1.499 1.606 1.713;0.860
0.967 1.074 1.180 1.287 1.394 1.500 1.607 1.714 1.820;0.968 1.075 1.181 1.288 1.395 1.501 1.608
1.715 1.821 1.928;1.076 1.183 1.289 1.396 1.502 1.609 1.716 1.822 1.929 2.036;1.184 1.290 1.397
1.504 1.610 1.717 1.824 1.930 2.037 2.143];
```

```
dTme2_2GaN=[0.007 0.011 0.014 0.018 0.021 0.025 0.029 0.032 0.036 0.039;0.011 0.014 0.018
0.021 0.025 0.029 0.032 0.036 0.039 0.043;0.014 0.018 0.021 0.025 0.029 0.032 0.036 0.039 0.043
0.047;0.018 0.021 0.025 0.029 0.032 0.036 0.039 0.043 0.047 0.050;0.021 0.025 0.029 0.032 0.036
0.039 0.043 0.047 0.050 0.054;0.025 0.029 0.032 0.036 0.039 0.043 0.047 0.050 0.054 0.057;0.029
0.032 0.036 0.039 0.043 0.047 0.050 0.054 0.057 0.061;0.032 0.036 0.039 0.043 0.047 0.050 0.054
0.057 0.061 0.064;0.036 0.039 0.043 0.047 0.050 0.054 0.057 0.061 0.064 0.068;0.039 0.043 0.047
0.050 0.054 0.057 0.061 0.064 0.068 0.072];
```

```
dTme3_2GaN=[0.249 0.498 0.747 0.995 1.244 1.493 1.742 1.990 2.239 2.488;0.249 0.498 0.747
0.996 1.244 1.493 1.742 1.991 2.239 2.488;0.250 0.498 0.747 0.996 1.245 1.493 1.742 1.991 2.240
2.488;0.250 0.499 0.748 0.996 1.245 1.494 1.742 1.991 2.240 2.489;0.250 0.499 0.748 0.997 1.245
1.494 1.743 1.992 2.240 2.489;0.251 0.499 0.748 0.997 1.246 1.494 1.743 1.992 2.241 2.489;0.251
0.500 0.748 0.997 1.246 1.495 1.743 1.992 2.241 2.490;0.251 0.500 0.749 0.998 1.246 1.495 1.744
1.993 2.241 2.490;0.252 0.500 0.749 0.998 1.247 1.495 1.744 1.993 2.242 2.490;0.252 0.501 0.749
0.998 1.247 1.496 1.744 1.993 2.242 2.491];
```

```
dTme4_2GaN=[0.249 0.249 0.250 0.250 0.250 0.250 0.251 0.251 0.251 0.252;0.497 0.498 0.498
0.498 0.499 0.499 0.499 0.500 0.500 0.500;0.746 0.746 0.747 0.747 0.747 0.748 0.748 0.748 0.749
0.749;0.995 0.995 0.995 0.996 0.996 0.996 0.997 0.997 0.997 0.997;1.243 1.243 1.244 1.244 1.244
1.245 1.245 1.245 1.246 1.246;1.492 1.492 1.492 1.493 1.493 1.493 1.494 1.494 1.494 1.495;1.740
1.741 1.741 1.741 1.742 1.742 1.742 1.743 1.743 1.743;1.989 1.989 1.990 1.990 1.990 1.990 1.991
1.991 1.991 1.992;2.237 2.238 2.238 2.238 2.239 2.239 2.239 2.240 2.240 2.240;2.486 2.486 2.487
2.487 2.487 2.488 2.488 2.488 2.489 2.489];
```

```
dTme5_2GaN=[0.007 0.011 0.014 0.018 0.021 0.025 0.029 0.032 0.036 0.039;0.011 0.014 0.018
0.021 0.025 0.029 0.032 0.036 0.039 0.043;0.014 0.018 0.021 0.025 0.029 0.032 0.036 0.039 0.043
0.047;0.018 0.021 0.025 0.029 0.032 0.036 0.039 0.043 0.047 0.050;0.021 0.025 0.029 0.032 0.036
0.039 0.043 0.047 0.050 0.054;0.025 0.029 0.032 0.036 0.039 0.043 0.047 0.050 0.054 0.057;0.029
0.032 0.036 0.039 0.043 0.047 0.050 0.054 0.057 0.061;0.032 0.036 0.039 0.043 0.047 0.050 0.054
0.057 0.061 0.064;0.036 0.039 0.043 0.047 0.050 0.054 0.057 0.061 0.064 0.068;0.039 0.043 0.047
0.050 0.054 0.057 0.061 0.064 0.068 0.072];
```

```
p00=[-3e-5 -9e-5 -1.333e-5 -4e-5 -9e-5];
```

```
p11=[0.1067 0.003587 0.2487 0.0003212 0.003587];
```

```
p22=[0.1077 0.003587 0.00032 0.2486 0.003587];
```

```
% %One thousand loop times with random noises
```

```
n=1000;
```

```
options = optimset('TolFun',0.5e-3,'MaxFunEvals',10000000,'MaxIter',10000);
```

```
alpha=1:n;
```

```
Mat2=zeros(2,n); %empty matrix
```

```
for ii=1:n
```

```
PP0=[5.5;8.5];
```

```
Pin=fminsearch(@myLsq_Two,PP0);
```

```
Mat2(:,ii)=Pin; %save loop results in matrix Mat
```

```

%EXIT(ii)=EXITFLAG;
end

Pin_one=mean(Mat2(1,:))% Average value of first line of matrix
Pin_two=mean(Mat2(2,:))% Average value of second line of matrix
Ermaxmin1=max((Mat2(1,:)))-min((Mat2(1,:)))%Error between Pin1max and Pin1min
Ermaxmin2=max((Mat2(2,:)))-min((Mat2(2,:)))%Error between Pin2max and Pin2min
figure(1)
plot([1:1000],Mat2(1,:),'b',[1,1000],[Pin_one,Pin_one],'-k',[1,1000],[5.94,5.94],'-r',
[1:1000],Mat2(2,:),'b',[1,1000],[Pin_two,Pin_two],'-k')
hold on
plot([1,1000],[9.16,9.16],'-r')
xlabel('Loop times');
ylabel('P(W)');
legend('Loop random value','Mean value of loop','Real input value')
title('Simulation loop with noises')

```



**%%Power predictions in 2 embedded GaN dies with 5 temperature sensors**  
**% Calling function @myLsq\_Two**

```
function [Err]=myLsq_Two(Pin) %Least square for calculating the error between measurement and
modelling
global dTme1_Two dTme2_Two
Bruit=0.1*randn(1,5);%(rand(1,5)-0.5)*0.01;%distributed noise with mean 0 and standard deviation
1
dTme1_Two=[1.162 0.039 2.113 0.594 0.039]+Bruit;%Measurement temperatures for 5 surface
points
dTme2_Two=[1.617 0.054 2.280 1.479 0.054]+Bruit;
p00=[-3e-5 -9e-5 -1.333e-5 -4e-5 -9e-5];%fitting coefficients
p11=[0.1067 0.003587 0.2487 0.0003212 0.003587];%fitting coefficients
p22=[0.1077 0.003587 0.00032 0.2486 0.003587];%fitting coefficients
dTmo1_Two=p00+p11*Pin(2)+p22*Pin(1); %fitting curves
dTmo2_Two=p00+p11*Pin(2)+p22*Pin(1);
Err=sum((dTmo2_Two-dTme2_Two).^2);
end
```

## ANNEX D

### %%Power and thermal conductivity predictions with 10 temperature measurement sensors

%Inverse model with input power and variable thermal conductivity of PCB

clear all;

%e=220e-6;%thickness from top surface of total structure to top surface of GaN chip

%A=1e-8;%section surface of the structure

P=[1 2 3 4 5 6 7 8 9 10];%Input power

lambda=[0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1];%Thermal conductivity of FR4

ln\_P=log(P);

ln\_lambda=log(lambda);

%Temperature measurements for five points on the surface of the structure:

dT1=[2.27 4.541 6.811 9.082 11.352 13.623 15.893 18.164 20.434 22.704;2.302 4.604 6.906 9.209  
11.511 13.813 16.115 18.417 20.719 23.021;2.264 4.528 6.793 9.057 11.321 13.585 15.849 18.114  
20.378 22.642;2.209 4.419 6.628 8.838 11.047 13.257 15.466 17.676 19.885 22.094;2.151 4.302  
6.453 8.604 10.755 12.906 15.057 17.208 19.359 21.510;2.093 4.186 6.280 8.373 10.466 12.559  
14.652 16.745 18.839 20.932;2.038 4.075 6.113 8.151 10.188 12.226 14.263 16.301 18.339  
20.376;1.985 3.970 5.955 7.940 9.925 11.910 13.894 15.879 17.864 19.849;1.935 3.870 5.805 7.740  
9.676 11.611 13.546 15.481 17.416 19.351;1.888 3.776 5.664 7.553 9.441 11.329 13.217 15.105  
16.993 18.882];

dT2=[0.089 0.178 0.266 0.355 0.444 0.533 0.622 0.711 0.799 0.888;0.023 0.046 0.068 0.091 0.114  
0.137 0.159 0.182 0.205 0.228;0.008 0.016 0.024 0.032 0.040 0.049 0.057 0.065 0.073 0.081;0.003  
0.007 0.010 0.014 0.017 0.020 0.024 0.027 0.031 0.034;0.002 0.003 0.005 0.006 0.008 0.010 0.011  
0.013 0.014 0.016;0.001 0.002 0.002 0.003 0.004 0.005 0.006 0.007 0.007 0.008;0 0.001 0.001 0.002  
0.002 0.003 0.003 0.004 0.004 0.004;0 0 0.001 0.001 0.001 0.001 0.002 0.002 0.002 0.002;0 0 0  
0.001 0.001 0.001 0.001 0.001 0.001 0.001;0 0 0 0 0.001 0.001 0.001 0.001 0.001];

dT3=[0.063 0.126 0.188 0.251 0.314 0.377 0.439 0.502 0.565 0.628;0.014 0.028 0.041 0.055 0.069  
0.083 0.097 0.111 0.124 0.138;0.004 0.009 0.013 0.018 0.022 0.027 0.031 0.035 0.040 0.044;0.002  
0.003 0.005 0.007 0.009 0.010 0.012 0.014 0.015 0.017;0.001 0.001 0.002 0.003 0.004 0.004 0.005  
0.006 0.007 0.007;0 0.001 0.001 0.001 0.002 0.002 0.002 0.003 0.003 0.004;0 0 0.001 0.001 0.001  
0.001 0.001 0.001 0.002 0.002;0 0 0 0 0.001 0.001 0.001 0.001 0.001;0 0 0 0 0 0 0.001;0 0 0  
0 0 0 0 0];

dT4=[0.046 0.092 0.138 0.184 0.230 0.276 0.322 0.368 0.414 0.460;0.009 0.018 0.026 0.035 0.044  
0.053 0.061 0.070 0.079 0.088;0.003 0.005 0.008 0.010 0.013 0.015 0.018 0.020 0.023 0.025;0.001  
0.002 0.003 0.004 0.004 0.005 0.006 0.007 0.008 0.009;0 0.001 0.001 0.001 0.002 0.002 0.003 0.003  
0.003 0.004;0 0 0.001 0.001 0.001 0.001 0.001 0.001 0.002;0 0 0 0 0 0.001 0.001 0.001 0.001;0  
0 0 0 0 0 0 0;0 0 0 0 0 0 0 0;0 0 0 0 0 0 0 0];

dT5=[1.365 2.729 4.094 5.459 6.823 8.188 9.553 10.917 12.282 13.647;1.111 2.221 3.332 4.442  
5.553 6.663 7.774 8.884 9.995 11.106;0.927 1.854 2.781 3.709 4.636 5.563 6.490 7.417 8.344  
9.272;0.790 1.581 2.371 3.162 3.952 4.743 5.533 6.324 7.114 7.904;0.685 1.369 2.054 2.739 3.423  
4.108 4.793 5.477 6.162 6.847;0.600 1.201 1.801 2.402 3.002 3.602 4.203 4.803 5.404 6.004;0.532  
1.064 1.595 2.127 2.659 3.191 3.722 4.254 4.786 5.318;0.475 0.950 1.425 1.899 2.374 2.849 3.324  
3.799 4.274 4.749;0.427 0.854 1.281 1.708 2.135 2.562 2.989 3.416 3.843 4.270;0.386 0.772 1.158  
1.545 1.931 2.317 2.703 3.089 3.475 3.862];

dT6=[1.758 3.515 5.273 7.030 8.788 10.545 12.303 14.06 15.818 17.575;1.605 3.209 4.814 6.418  
8.023 9.627 11.232 12.836 14.441 16.045;1.462 2.924 4.386 5.849 7.311 8.773 10.235 11.697  
13.159 14.622;1.341 2.683 4.024 5.365 6.707 8.048 9.389 10.731 12.072 13.414;1.239 2.478 3.717  
4.956 6.194 7.433 8.672 9.911 11.150 12.389;1.51 2.302 3.453 4.604 5.755 6.906 8.057 9.208 10.359  
11.510;1.075 2.150 3.224 4.299 5.374 6.449 7.524 8.598 9.673 10.748;1.008 2.016 3.024 4.032  
5.040 6.048 7.056 8.064 9.072 10.080;0.949 1.898 2.847 3.796 4.745 5.694 6.642 7.591 8.540  
9.489;0.896 1.792 2.689 3.585 4.481 5.377 6.274 7.170 8.066 8.962];

ANNEX D – CONCEPTION OF THE INVERSE THERMAL MODEL

```

dT7=[0.125 0.251 0.376 0.502 0.627 0.752 0.878 1.003 1.129 1.254;0.037 0.073 0.110 0.147 0.184
0.220 0.257 0.294 0.331 0.367;0.014 0.029 0.043 0.057 0.071 0.086 0.100 0.114 0.129 0.143;0.006
0.013 0.019 0.026 0.032 0.039 0.045 0.052 0.058 0.064;0.003 0.006 0.010 0.013 0.016 0.019 0.022
0.026 0.029 0.032;0.002 0.003 0.005 0.007 0.008 0.010 0.012 0.014 0.015 0.017;0.001 0.002 0.003
0.004 0.005 0.006 0.007 0.008 0.009 0.009;0.001 0.001 0.002 0.002 0.003 0.003 0.004 0.004 0.005
0.005;0 0.001 0.001 0.001 0.002 0.002 0.002 0.003 0.003 0.003;0 0 0.001 0.001 0.001 0.001 0.001
0.002 0.002 0.002];
dT8=[0.686 1.372 2.057 2.743 3.429 4.115 4.801 5.486 6.172 6.858;0.411 0.822 1.233 1.644 2.056
2.467 2.878 3.289 3.700 4.111;0.272 0.545 0.817 1.090 1.362 1.634 1.907 2.179 2.451 2.724;0.192
0.383 0.575 0.766 0.958 1.149 1.341 1.533 1.724 1.916;0.140 0.281 0.421 0.561 0.702 0.842 0.982
1.123 1.263 1.403;0.106 0.212 0.318 0.424 0.530 0.635 0.741 0.847 0.953 1.059;0.082 0.164 0.245
0.327 0.409 0.491 0.573 0.655 0.736 0.818;0.064 0.129 0.193 0.258 0.322 0.386 0.451 0.515 0.580
0.644;0.051 0.103 0.154 0.206 0.257 0.309 0.360 0.412 0.463 0.515;0.042 0.083 0.125 0.167 0.208
0.250 0.292 0.333 0.375 0.417];
dT9=[0.268 0.535 0.803 1.071 1.338 1.606 1.873 2.141 2.409 2.676;0.108 0.217 0.325 0.433 0.542
0.650 0.758 0.867 0.975 1.083;0.054 0.107 0.161 0.215 0.268 0.322 0.376 0.429 0.483 0.537;0.030
0.059 0.089 0.119 0.148 0.178 0.208 0.238 0.267 0.297;0.018 0.035 0.053 0.071 0.088 0.106 0.124
0.141 0.159 0.177;0.011 0.022 0.033 0.044 0.055 0.066 0.078 0.089 0.100 0.111;0.007 0.014 0.022
0.029 0.036 0.043 0.051 0.058 0.065 0.072;0.005 0.010 0.015 0.020 0.024 0.029 0.034 0.039 0.044
0.049;0.003 0.007 0.010 0.014 0.017 0.020 0.024 0.027 0.030 0.034;0.002 0.005 0.007 0.010 0.012
0.014 0.017 0.019 0.022 0.024];
dT10=[0.168 0.336 0.504 0.672 0.839 1.007 1.175 1.343 1.511 1.679;0.056 0.112 0.168 0.224 0.281
0.337 0.393 0.449 0.505 0.561;0.024 0.048 0.072 0.097 0.121 0.145 0.169 0.193 0.217 0.241;0.012
0.024 0.036 0.048 0.059 0.071 0.083 0.095 0.107 0.119;0.006 0.013 0.019 0.026 0.032 0.038 0.045
0.051 0.058 0.064;0.004 0.007 0.011 0.015 0.018 0.022 0.026 0.029 0.033 0.037;0.002 0.004 0.007
0.009 0.011 0.013 0.015 0.018 0.020 0.022;0.001 0.003 0.004 0.005 0.007 0.008 0.010 0.011 0.012
0.014;0.001 0.002 0.003 0.004 0.004 0.005 0.006 0.007 0.008 0.009;0.001 0.001 0.002 0.002 0.003
0.004 0.004 0.005 0.005 0.006];
ln_dT1=log(dT1);
ln_dT2=log(dT2);
ln_dT3=log(dT3);
ln_dT4=log(dT4);
ln_dT5=log(dT5);
ln_dT6=log(dT6);
ln_dT7=log(dT7);
ln_dT8=log(dT8);
ln_dT9=log(dT9);
ln_dT10=log(dT10);
%%
%custom equation for curve fitting: z=f(x,y)= f(x,y) = p00 + p10*x + p01*y + p20*x^2 + p11*x*y
+ p02*y^2
p00=[0.6374 -8.953 -9.779 -10.55 -0.9444 -0.1066 -8.181 -3.164 -5.985 -7.309];
p10=[1 0.8977 0.8007 0.7836 1 1 0.8289 1.001 0.9884 0.9707];
p01=[-0.2286 -4.166 -4.319 -4.57 -0.9242 -0.5319 -4.099 -1.937 -3.139 -3.658];
p20=[-1.943e-005 -0.009812 0.03921 0.02953 2.466e-005 -0.0001232 0.02139 -0.0002026
0.001184 -0.003295];
p11=[-2.227e-005 -0.07716 -0.05874 -0.06763 1.591e-005 7.902e-005 -0.08164 0.0003083 -
0.005951 -0.02435];
p02=[-0.06509 -0.5925 -0.552 -0.5712 -0.1654 -0.1049 -0.6481 -0.3171 -0.4863 -0.5547];

%%
%Inverse model for input power P=5.79W, lambda=0.62W/(m.K)
%One thousand loop times with random noises
n=1000;
options = optimset('TolFun',0.4e-2, 'MaxFunEvals',1000000000,'MaxIter',100000);

```

```

alpha=[1:n];
Mat2=zeros(2,n) ; %empty matrix
for ii=1:n

    PP0=[1.5;-0.5];
    Qin=fminsearch(@myLsq_Pin_loglamta_10points_polynomial,PP0,options);
    Mat2(:,ii)=Qin; %save loop results in matrix Mat
end

Pin_logP=Mat2(1,:);%Average value of first line of matrix
Pin_loglambda=Mat2(2,:);%Average value of second line of matrix
Pin_P=exp(Pin_logP);
Pin_lambda=exp(Pin_loglambda);
Pmean_P=mean(Pin_P)
Pmean_lambda=mean(Pin_lambda)
Ermaxmin1=max(Pin_P)-min(Pin_P)%Error between Pin1max and Pin1min
Ermaxmin2=max(Pin_lambda)-min(Pin_lambda)%Error between Pin2max and Pin2min
Pin_real=5.79;
lamta_real=0.62;

figure(1)
plot(alpha,Pin_P,'b',[1,1000],[Pmean_P,Pmean_P],'-k',[1,1000],[Pin_real,Pin_real],'-r')%tracer
courbe de proximité
ylim([5.7 5.85]);
xlabel('Loop times');ylabel('P(W)');
legend('-Loop random value','-Mean value of loop','-Real input value')
title('Simulation loop with thermal noises')

figure(2)
plot(alpha,Pin_lambda,'b',[1,1000],[Pmean_lambda,Pmean_lambda],'-
k',[1,1000],[lamta_real,lamta_real],'-r')%tracer courbe de proximité
ylim([0.6 0.65]);
xlabel('Loop times');ylabel('\lambda_t_h(W/mK)');
legend('-Loop random value','-Mean value of loop','-Real input value')
title('Simulation loop with thermal noises')

```

**%%Power and thermal conductivity predictions with 10 temperature measurement sensors**  
**% Calling function @myLsq\_Pin\_loglamta\_10points\_polynomial**

```
function [Err]=myLsq_Pin_loglamta_10points_polynomial(Qin) %Least square for calculating the
error between measurement and modelling
global dTmea_Pin_lamta
Bruit=0.1*randn(1,10);%(rand(1,5)-0.5)*0.01;%distributed noise with mean 0 and standard
deviation 1
dTmea_Pin_lamta=[12.054 0.004 0.002 0.001 3.390 6.571 0.009 0.581 0.059
0.019]+Bruit;%Measurement temperatures for 5 surface points
p00=[0.6374 -8.953 -9.779 -10.55 -0.9444 -0.1066 -8.181 -3.164 -5.985 -7.309];
p10=[1 0.8977 0.8007 0.7836 1 1 0.8289 1.001 0.9884 0.9707];
p01=[-0.2286 -4.166 -4.319 -4.57 -0.9242 -0.5319 -4.099 -1.937 -3.139 -3.658];
p20=[-1.943e-005 -0.009812 0.03921 0.02953 2.466e-005 -0.0001232 0.02139 -0.0002026
0.001184 -0.003295];
p11=[-2.227e-005 -0.07716 -0.05874 -0.06763 1.591e-005 7.902e-005 -0.08164 0.0003083 -
0.005951 -0.02435];
p02=[-0.06509 -0.5925 -0.552 -0.5712 -0.1654 -0.1049 -0.6481 -0.3171 -0.4863 -0.5547];
ln_dTmo_Pin_lamta=p00+p10*Qin(1)+p01*Qin(2)+p20*Qin(1)*Qin(1)+p11*Qin(1)*Qin(2)+p02
*Qin(2)*Qin(2);
dTmo_Pin_lamta=exp(ln_dTmo_Pin_lamta);
Err=sum((dTmea_Pin_lamta-dTmo_Pin_lamta).^2);
end
```

**%%Power and thermal conductivity predictions with 6 temperature measurement sensors**

```
%Inverse model with input power and variable thermal conductivity of PCB
```

```
clear all;
```

```
%e=220e-6;%thickness from top surface of total structure to top surface of GaN chip
```

```
%A=1e-8;%section surface of the structure
```

```
P=[1 2 3 4 5 6 7 8 9 10];%Input power
```

```
lambda=[0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1];%Thermal conductivity of FR4
```

```
ln_P=log(P);
```

```
ln_lambda=log(lambda);
```

```
%Temperature measurements for five points on the surface of the structure:
```

```
dT1=[2.27 4.541 6.811 9.082 11.352 13.623 15.893 18.164 20.434 22.704;2.302 4.604 6.906 9.209  
11.511 13.813 16.115 18.417 20.719 23.021;2.264 4.528 6.793 9.057 11.321 13.585 15.849 18.114  
20.378 22.642;2.209 4.419 6.628 8.838 11.047 13.257 15.466 17.676 19.885 22.094;2.151 4.302  
6.453 8.604 10.755 12.906 15.057 17.208 19.359 21.510;2.093 4.186 6.280 8.373 10.466 12.559  
14.652 16.745 18.839 20.932;2.038 4.075 6.113 8.151 10.188 12.226 14.263 16.301 18.339  
20.376;1.985 3.970 5.955 7.940 9.925 11.910 13.894 15.879 17.864 19.849;1.935 3.870 5.805 7.740  
9.676 11.611 13.546 15.481 17.416 19.351;1.888 3.776 5.664 7.553 9.441 11.329 13.217 15.105  
16.993 18.882];
```

```
%dT2=[0.089 0.178 0.266 0.355 0.444 0.533 0.622 0.711 0.799 0.888;0.023 0.046 0.068 0.091 0.114  
0.137 0.159 0.182 0.205 0.228;0.008 0.016 0.024 0.032 0.040 0.049 0.057 0.065 0.073 0.081;0.003  
0.007 0.010 0.014 0.017 0.020 0.024 0.027 0.031 0.034;0.002 0.003 0.005 0.006 0.008 0.010 0.011  
0.013 0.014 0.016;0.001 0.002 0.002 0.003 0.004 0.005 0.006 0.007 0.007 0.008;0 0.001 0.001 0.002  
0.002 0.003 0.003 0.004 0.004 0.004;0 0 0.001 0.001 0.001 0.001 0.002 0.002 0.002 0.002;0 0 0  
0.001 0.001 0.001 0.001 0.001 0.001 0.001;0 0 0 0 0 0.001 0.001 0.001 0.001 0.001];
```

```
%dT3=[0.063 0.126 0.188 0.251 0.314 0.377 0.439 0.502 0.565 0.628;0.014 0.028 0.041 0.055 0.069  
0.083 0.097 0.111 0.124 0.138;0.004 0.009 0.013 0.018 0.022 0.027 0.031 0.035 0.040 0.044;0.002  
0.003 0.005 0.007 0.009 0.010 0.012 0.014 0.015 0.017;0.001 0.001 0.002 0.003 0.004 0.004 0.005  
0.006 0.007 0.007;0 0.001 0.001 0.001 0.002 0.002 0.002 0.003 0.003 0.004;0 0 0.001 0.001 0.001  
0.001 0.001 0.001 0.002 0.002;0 0 0 0 0 0.001 0.001 0.001 0.001 0.001;0 0 0 0 0 0 0 0.001;0 0 0  
0 0 0 0 0 0];
```

```
%dT4=[0.046 0.092 0.138 0.184 0.230 0.276 0.322 0.368 0.414 0.460;0.009 0.018 0.026 0.035 0.044  
0.053 0.061 0.070 0.079 0.088;0.003 0.005 0.008 0.010 0.013 0.015 0.018 0.020 0.023 0.025;0.001  
0.002 0.003 0.004 0.004 0.005 0.006 0.007 0.008 0.009;0 0.001 0.001 0.001 0.002 0.002 0.003 0.003  
0.003 0.004;0 0 0 0.001 0.001 0.001 0.001 0.001 0.001 0.002;0 0 0 0 0 0.001 0.001 0.001 0.001;0  
0 0 0 0 0 0 0 0;0 0 0 0 0 0 0 0;0 0 0 0 0 0 0 0];
```

```
dT5=[1.365 2.729 4.094 5.459 6.823 8.188 9.553 10.917 12.282 13.647;1.111 2.221 3.332 4.442  
5.553 6.663 7.774 8.884 9.995 11.106;0.927 1.854 2.781 3.709 4.636 5.563 6.490 7.417 8.344  
9.272;0.790 1.581 2.371 3.162 3.952 4.743 5.533 6.324 7.114 7.904;0.685 1.369 2.054 2.739 3.423  
4.108 4.793 5.477 6.162 6.847;0.600 1.201 1.801 2.402 3.002 3.602 4.203 4.803 5.404 6.004;0.532  
1.064 1.595 2.127 2.659 3.191 3.722 4.254 4.786 5.318;0.475 0.950 1.425 1.899 2.374 2.849 3.324  
3.799 4.274 4.749;0.427 0.854 1.281 1.708 2.135 2.562 2.989 3.416 3.843 4.270;0.386 0.772 1.158  
1.545 1.931 2.317 2.703 3.089 3.475 3.862];
```

```
dT6=[1.758 3.515 5.273 7.030 8.788 10.545 12.303 14.06 15.818 17.575;1.605 3.209 4.814 6.418  
8.023 9.627 11.232 12.836 14.441 16.045;1.462 2.924 4.386 5.849 7.311 8.773 10.235 11.697  
13.159 14.622;1.341 2.683 4.024 5.365 6.707 8.048 9.389 10.731 12.072 13.414;1.239 2.478 3.717  
4.956 6.194 7.433 8.672 9.911 11.150 12.389;1.51 2.302 3.453 4.604 5.755 6.906 8.057 9.208 10.359  
11.510;1.075 2.150 3.224 4.299 5.374 6.449 7.524 8.598 9.673 10.748;1.008 2.016 3.024 4.032  
5.040 6.048 7.056 8.064 9.072 10.080;0.949 1.898 2.847 3.796 4.745 5.694 6.642 7.591 8.540  
9.489;0.896 1.792 2.689 3.585 4.481 5.377 6.274 7.170 8.066 8.962];
```

```
%dT7=[0.125 0.251 0.376 0.502 0.627 0.752 0.878 1.003 1.129 1.254;0.037 0.073 0.110 0.147 0.184  
0.220 0.257 0.294 0.331 0.367;0.014 0.029 0.043 0.057 0.071 0.086 0.100 0.114 0.129 0.143;0.006  
0.013 0.019 0.026 0.032 0.039 0.045 0.052 0.058 0.064;0.003 0.006 0.010 0.013 0.016 0.019 0.022
```

ANNEX D – CONCEPTION OF THE INVERSE THERMAL MODEL

```

0.026 0.029 0.032;0.002 0.003 0.005 0.007 0.008 0.010 0.012 0.014 0.015 0.017;0.001 0.002 0.003
0.004 0.005 0.006 0.007 0.008 0.009 0.009;0.001 0.001 0.002 0.002 0.003 0.003 0.004 0.004 0.005
0.005;0 0.001 0.001 0.001 0.002 0.002 0.002 0.003 0.003 0.003;0 0 0.001 0.001 0.001 0.001 0.001
0.002 0.002 0.002];
dT8=[0.686 1.372 2.057 2.743 3.429 4.115 4.801 5.486 6.172 6.858;0.411 0.822 1.233 1.644 2.056
2.467 2.878 3.289 3.700 4.111;0.272 0.545 0.817 1.090 1.362 1.634 1.907 2.179 2.451 2.724;0.192
0.383 0.575 0.766 0.958 1.149 1.341 1.533 1.724 1.916;0.140 0.281 0.421 0.561 0.702 0.842 0.982
1.123 1.263 1.403;0.106 0.212 0.318 0.424 0.530 0.635 0.741 0.847 0.953 1.059;0.082 0.164 0.245
0.327 0.409 0.491 0.573 0.655 0.736 0.818;0.064 0.129 0.193 0.258 0.322 0.386 0.451 0.515 0.580
0.644;0.051 0.103 0.154 0.206 0.257 0.309 0.360 0.412 0.463 0.515;0.042 0.083 0.125 0.167 0.208
0.250 0.292 0.333 0.375 0.417];
dT9=[0.268 0.535 0.803 1.071 1.338 1.606 1.873 2.141 2.409 2.676;0.108 0.217 0.325 0.433 0.542
0.650 0.758 0.867 0.975 1.083;0.054 0.107 0.161 0.215 0.268 0.322 0.376 0.429 0.483 0.537;0.030
0.059 0.089 0.119 0.148 0.178 0.208 0.238 0.267 0.297;0.018 0.035 0.053 0.071 0.088 0.106 0.124
0.141 0.159 0.177;0.011 0.022 0.033 0.044 0.055 0.066 0.078 0.089 0.100 0.111;0.007 0.014 0.022
0.029 0.036 0.043 0.051 0.058 0.065 0.072;0.005 0.010 0.015 0.020 0.024 0.029 0.034 0.039 0.044
0.049;0.003 0.007 0.010 0.014 0.017 0.020 0.024 0.027 0.030 0.034;0.002 0.005 0.007 0.010 0.012
0.014 0.017 0.019 0.022 0.024];
dT10=[0.168 0.336 0.504 0.672 0.839 1.007 1.175 1.343 1.511 1.679;0.056 0.112 0.168 0.224 0.281
0.337 0.393 0.449 0.505 0.561;0.024 0.048 0.072 0.097 0.121 0.145 0.169 0.193 0.217 0.214;0.012
0.024 0.036 0.048 0.059 0.071 0.083 0.095 0.107 0.119;0.006 0.013 0.019 0.026 0.032 0.038 0.045
0.051 0.058 0.064;0.004 0.007 0.011 0.015 0.018 0.022 0.026 0.029 0.033 0.037;0.002 0.004 0.007
0.009 0.011 0.013 0.015 0.018 0.020 0.022;0.001 0.003 0.004 0.005 0.007 0.008 0.010 0.011 0.012
0.014;0.001 0.002 0.003 0.004 0.004 0.005 0.006 0.007 0.008 0.009;0.001 0.001 0.002 0.002 0.003
0.004 0.004 0.005 0.005 0.006];
ln_dT1=log(dT1);
%ln_dT2=log(dT2);
%ln_dT3=log(dT3);
%ln_dT4=log(dT4);
ln_dT5=log(dT5);
ln_dT6=log(dT6);
%ln_dT7=log(dT7);
ln_dT8=log(dT8);
ln_dT9=log(dT9);
ln_dT10=log(dT10);
%%
%custom equation for curve fitting: z=f(x,y)= f(x,y) = p00 + p10*x + p01*y + p20*x^2 + p11*x*y
+ p02*y^2
p00=[0.6374 -0.9444 -0.1066 -3.164 -5.985 -7.309];
p10=[1 1 1 1.001 0.9884 0.9707];
p01=[-0.2286 -0.9242 -0.5319 -1.937 -3.139 -3.658];
p20=[-1.943e-005 2.466e-005 -0.0001232 -0.0002026 0.001184 -0.003295];
p11=[-2.227e-005 1.591e-005 7.902e-005 0.0003083 -0.005951 -0.02435];
p02=[-0.06509 -0.1654 -0.1049 -0.3171 -0.4863 -0.5547];

%%
%Inverse model for input power P=5.79W, lambda=0.62W/(m.K)
%One thousand loop times with random noises
n=1000;
options = optimset('TolFun',0.4e-2, 'MaxFunEvals',100000,'MaxIter',100000);
alpha=[1:n];
Mat2=zeros(2,n) ; %empty matrix
for ii=1:n

PP0=[1.5;-0.5];

```

```

Qin=fminsearch(@myLsq_Pin_loglamta_6points_polynomial,PP0,options);
Mat2(:,ii)=Qin; %save loop results in matrix Mat
%EXIT(ii)=EXITFLAG;
end

Pin_logP=Mat2(1,:);%Average value of first line of matrix
Pin_loglambda=Mat2(2,:);%Average value of second line of matrix
Pin_P=exp(Pin_logP);
Pin_lambda=exp(Pin_loglambda);
Pmean_P=mean(Pin_P)
Pmean_lambda=mean(Pin_lambda)
Ermaxmin1=max(Pin_P)-min(Pin_P)%Error between Pin1max and Pin1min
Ermaxmin2=max(Pin_lambda)-min(Pin_lambda)%Error between Pin2max and Pin2min
Pin_real=5.79;
lamta_real=0.62;

figure(1)
plot(alpha,Pin_P,'b',[1,1000],[Pmean_P,Pmean_P],'-k',[1,1000],[Pin_real,Pin_real],'-r')
ylim([5.7 5.85]);
xlabel('Loop times');ylabel('P(W)');
legend('-Loop random value','-Mean value of loop','-Real input value')
title('Simulation loop with thermal noises')

figure(2)
plot(alpha,Pin_lambda,'b',[1,1000],[Pmean_lambda,Pmean_lambda],'-k',[1,1000],[lamta_real,lamta_real],'-r')%tracer courbe d'approximate
ylim([0.6 0.65]);
xlabel('Loop times');ylabel('\lambda(W/mK)');
legend('-Loop random value','-Mean value of loop','-Real input value')
title('Simulation loop with thermal noises')

```



**%%Power and thermal conductivity predictions with 10 temperature measurement sensors**  
**% Calling function @myLsq\_Pin\_loglamta\_6points\_polynomial**

```
function [Err]=myLsq_Pin_loglamta_6points(Qin) %Least square for calculating the error between
measurement and modelling
global dTmea_Pin_lamta
Bruit=0.1*randn(1,6);%(rand(1,5)-0.5)*0.01;%distributed noise with mean 0 and standard deviation
1
dTmea_Pin_lamta=[12.054 3.390 6.571 0.581 0.059 0.019];%+Bruit;%Measurement temperatures
for 5 surface points
Coe_a=[0.6782 -0.8407 -0.02357 -2.964 -5.717 -7.02];
Coe_b=[1 1 0.9915 1 1.008 0.9893];
Coe_c=[-0.08569 -0.561 -0.2998 -1.24 -2.087 -2.49];
ln_dTmo_Pin_lamta=Coe_a+Coe_b*Qin(1)+Coe_c*Qin(2);
dTmo_Pin_lamta=exp(ln_dTmo_Pin_lamta);
Err=sum((dTmea_Pin_lamta-dTmo_Pin_lamta).^2);
end
```