FD-SOI technology opportunities for more energy efficient asynchronous circuits

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THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITÉ GRENOBLE ALPES

Spécialité : **Nano Électronique & Nano Technologies**

Arrêté ministériel : 25 mai 2016

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dans **l'École Doctorale Electronique, Electrotechnique, Automatique & Traitement du Signal (E.E.A.T.S)**

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Thèse soutenue publiquement le **21 Janvier 2019**,
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To my beloved family: Selma, Ana, Gilson, and Maíra

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Abstract

Keeping the fast evolving pace of embedded systems of portable devices require ameliorations of power management techniques, without compromising the circuit performance and robustness. In this context, this thesis studies novel energy management schemes, and how to implement them, by using two main design approaches: asynchronous logic and adaptive body biasing (ABB) techniques. Four main contributions have been done, thus enabling the design of more energy efficient asynchronous circuits. 1) We contributed with the design of a Quasi-delay Insensitive (QDI) asynchronous ALU architecture, used in a comparative analysis of asynchronous versus synchronous systems. This first study has demonstrated the energy efficiency and robustness of QDI circuits, especially if operating at low power supply (V_{dd}). 2) We proposed a new body built-in cell for implementing ABB schemes by tuning the circuit threshold voltage (Vth) on-the-fly; and detecting short-duration and long-duration transient faults (TF) caused by environmental radiation. The proposed cell is a key building block to fully benefit from body biasing features of the FD-SOI technology while enhancing system's reliability. 3) We assessed three different ABB strategies - based on automatic activity detection and multiple body-biasing domains (BBDs) - for QDI asynchronous circuits. Furthermore, a methodology for analyzing energy efficiency of ABB strategies in QDI asynchronous circuits is also proposed in this work. 4) We developed a standard cell-based IC design flow to apply ABB strategies with multiple BBDs by using the proposed body built-in cells. A testchip has been designed and fabricated to validate the developed design flow and the efficacy of the body built-in cell.

Keywords: Quasi-delay-insensitive Asynchronous Circuits, Adaptive Body Biasing, Energy Efficiency, FD-SOI.

Résumé

Afin de suivre le rythme effréné des évolutions des systèmes embarqués et des dispositifs portables, il s'avère aujourd'hui indispensable d'optimiser la gestion de l'énergie sans pour autant compromettre la performance et la robustesse des circuits. Dans ce contexte, cette thèse étudie de nouveaux dispositifs de gestion de l'énergie ainsi que leur mise en œuvre, en combinant deux approches: la logique asynchrone et les techniques de polarisation du substrat (*Adaptive Body Biasing* - ABB). Cette thèse comporte quatre contributions permettant la conception de circuits asynchrones énergétiquement plus efficaces. 1) Une unité arithmétique et logique (UAL) asynchrone quasi insensible aux délais (*Quasi Delay Insensitive* - QDI) a été conçue et utilisée pour mener une analyse comparative entre systèmes synchrones et asynchrones. Cette étude démontre notamment la meilleure efficacité énergétique et la plus grande robustesse des circuits asynchrones QDI, surtout lorsqu'ils fonctionnent à basse tension. 2) Une cellule standard a été spécialement développée pour mettre en œuvre nos schémas d'adaptation dynamique du substrat (ABB) qui ajustent la tension de seuil (V_{th}) des transistors. En outre, cette cellule s'est révélée très utile pour la détection de fautes transitoires causées par des radiations environnementales. Cette cellule est en outre un élément clé pour exploiter la polarisation du substrat, un des intérêts majeurs de la technologie FD-SOI, et d'améliorer la fiabilité du système. 3) Trois stratégies de polarisation de substrat ont été évaluées. Ces stratégies reposent sur la détection automatique de l'activité des circuits asynchrones QDI et de la polarisation de multiples domaines dans le substrat (*Body Biasing Domains* - BBD). De plus, une méthode pour analyser l'efficacité énergétique des stratégies de polarisation pour les circuits asynchrones QDI a également été proposée dans le cadre de cette thèse. 4) Enfin, un flot de conception de circuits numériques intégrés a été proposé et développé. Ce flot, basé sur des cellules standards, permet d'exploiter des stratégies de polarisation (ABB) avec plusieurs domaines (BBD) en utilisant la cellule standard spécialement développée. Un testchip a été conçu et fabriqué pour valider notre flot de conception et évaluer l'efficacité de la cellule proposée.

Mots-clés : Circuits Asynchrones Quasi-Insensibles aux Délais, Polarisation Adaptative du Substrat, Efficacité Énergétique, FD-SOI.

Chapter 1

Introduction

The rapid technological advances of recent years have induced a massive spread of electronic circuits to almost every apparatus that surround our environment. From smartphones to smartwatches and even personal health monitoring systems, nowadays most devices have embedded integrated circuits (ICs). We entered an era of boundlessly greater connectivity, the Internet of Things (IoT), in which these ubiquitous electronic devices exchange information between them and with the cloud. The popularity of IoT has been increasing at a incredibly fast pace. Intel Corporation has estimated that the number of connected devices was 2 billion in 2006 and reached 15 billions by 2015. Extrapolating these numbers, they projected a total of 200 billions devices to be connected to each other by 2020 [8].

This massive proliferation of connected "things" has been rapidly increasing the demand for energy. For instance, the Semiconductor Industry Association has estimated that the computer devices will require more energy than what the entire world is capable of generating by 2040 [132]. Thus, the law of the more performance the better, the predominant design theory in past years, is no longer acceptable. Instead, the systems designed for IoT applications, especially wireless sensor networks, need to prioritize energy efficiency. The result is not only batteries that last longer and increased autonomy, but also the preservation of natural resources for the sake of a greener world.

Attaining the aforementioned energy efficiency has been sought in three different research axis: technology, architectural design, and power management techniques. In the first axis, enhancing the manufacturing technology to shrink the transistors gate length has historically allowed decreasing the power consumption required for maintaining a certain performance. For instance, in [101] authors have reported that scaling the technology node of a microprocessor from 0.75 μm to 0.35 μm resulted in a power reduction by a factor of approximately two with an equivalent performance. Reducing the power consumption while maintaining a similar performance implies a higher energy efficiency was achieved with technology scale down. This energy gain with transistors scale down has been possible until the 100 nm node. Beyond this node, several fundamental physics limitation previously neglected, for example short channel effects, have slowed down the energy efficiency enhancement traditionally achieved with simple scale down of conventional bulk technology [128]. To overcome the 100 nm manufacturing barrier, alternative technologies, based on thin film, have been proposed. The two main alternatives proposed by the industry were: the Fully depleted Silicon on Insulator (FD-SOI) [136] and the Fin Field Effect Transistor (FinFET) [35], technologies in which the electrostatic control in the channel has been improved to enable the pursuit of power consumption and performance improvements with downscale.

Furthermore, the second axis of research towards more energy efficiency is the architectural design approach. Asynchronous circuits, systems with local synchronization instead of global synchronization, has been shown to be a promising solution for low power and high energy efficient applications [19]. In this type of circuit, a local handshake protocol controls data propagating through the system instead of a global clock signal. In the absence of the clock signal, the power consumed by the clock tree circuitry is eliminated. Additionally, the event-driven nature of the asynchronous logic automatically turns the inactive blocks to standby mode. Only blocks with data to be processed will be activated, thus the dynamic power of the system is reduced if compared to a synchronous counterpart [18, 50]. There are different methods to design asynchronous circuits that differ from each other in the number of timing assumptions used to implement sequencing. The class of Quasi-Delay Insensitive (QDI) asynchronous circuits, the design approach explored in this thesis, can operate correctly with only a few assumptions on certain forks [86]. The reduced number of timing assumptions makes QDI asynchronous circuits very robust and appropriate for low-power operation.

Another possibility for enhancing energy efficiency is implementing existing power management techniques, e.g. voltage scaling and body biasing [26, 98]. The former consists in reducing V_{dd} in order to decrease the dynamic power consumption at the cost of increased gate delays, a technique imposing a permanent trade-off between power and performance. Complementarily, applying a voltage to the body of the transistors - a technique known as body biasing - artificially changes transistors threshold voltage (V_{th}) in order to decrease static power consumption or boost performance for achieving optimum energy efficiency [157]. Moreover, adaptive body biasing (ABB) allows further enhancing energy efficiency by adaptively decreasing V_{th} during computation, in order to improve performance, and increase V_{th} at idle periods to mitigate leakage [109, 165]. The use of ABB schemes is perfectly suitable for IoT applications, in which long periods of idleness between two calculations is a key characteristic.

In this context, we focused on merging these three research axis to design more energy efficient nano-electronic systems, as proposed by Hamon et al [56]. The extended body biasing range - achievable with the FD-SOI technology - enable the implementation of efficient ABB strategies in asynchronous circuits, systems in which the application of the aforementioned power management techniques is straightforward. The asynchronous handshake signals are directly exploited to detect the periods of activity and idleness - necessary for implementing ABB. Moreover, the local synchronization nature of asynchronous circuits allows ABB-induced on-the-fly delay variation with a minimal risk of timing violations.

This thesis brings four main contributions to enable the design of more energy efficient asynchronous circuits. The first one is the design of a QDI asynchronous ALU architecture, used in a comparative analysis of asynchronous versus synchronous systems. This first study has demonstrated the energy efficiency and robustness of QDI circuits, especially if operating at low V_{dd}. The second contribution is a new level-shifter based body biasing generator (BBG) that enables applying ABB schemes by tuning the circuit Vth on-the-fly. The proposed BBG is a key building block to fully benefit from the body biasing features of the FD-SOI technology. It is also capable of detecting short-duration and long-duration transient faults (TF) caused by environmental radiation, thus enhancing system reliability.

The third contribution of this thesis is the evaluation of three different ABB strategies for QDI asynchronous circuits. The objective of this study was to determine the optimal granularity for implementing multiple body-biasing domains (BBDs) with automatic biasing activation depending on circuit activity. Furthermore, a methodology for analyzing energy efficiency of ABB strategies in QDI asynchronous circuits is also proposed.

Finally, as a final contribution of this thesis, a standard cell based IC design flow has been proposed. It uses the proposed architecture of level-shifter based BBG to implement ABB strategies with multiple BBDs in QDI asynchronous circuits. In order to validate the IC design flow, a testchip has been designed and fabricated in FD-SOI 28 nm technology, which also showed the efficacy of the developed level-shifter based BBG and gains of implementing ABB strategies in QDI asynchronous systems.

This thesis is organized as follows. Chapter 2 introduces the state of the art on the FD-SOI technology, comparing it to conventional bulk and FinFET technologies. In the sequel, the basic concepts of asynchronous circuits is presented in chapter 3, highlighting their advantages over synchronous circuits. A case study comparison of synchronous versus asynchronous circuits, the results of the first contribution, is presented in chapter 4. In chapter 5, a methodology for analyzing energy efficiency of ABB strategies in QDI asynchronous circuits is presented. It establishes the criteria for assessing three different ABB strategies based on automatic activity detection and multiple body-biasing domains (BBDs), with the goal of determining optimal use cases for each strategy. Chapter 6 presents a novel level-shifter based BBG, which is the key for implementing the strategies investigated in chapter 5. Additionally, the proposed cell enables transient fault detection, which contributes for improving the robustness of the system. Subsequently, the proposed dedicated IC design flow for implementing ABB strategies with multiple BBDs by using the proposed body built-in cells is presented and validated with the preliminary results obtained with the fabricated test-chip. Finally, chapter 8 concludes this thesis, summarizing the main contributions and presenting the conclusions and future perspectives of this work.

Chapter 2

The Fully Depleted Silicon on Insulator technology

2.1 Introduction

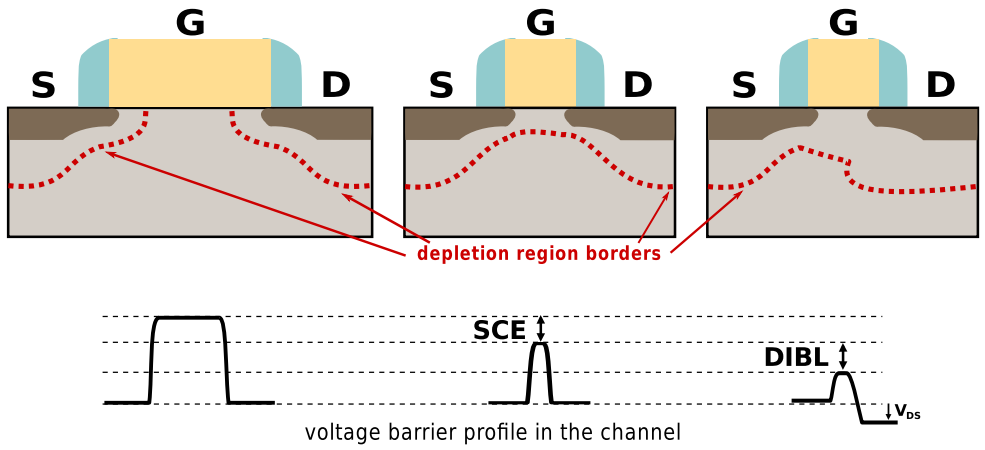
Historically, the continuous scale down of semiconductor nodes has relied on doubled integration density and significant performance gains for each new technology node, as foreseen by Moore's law [102]. Additionally, the reduction of the cost per transistor has also been seen as a key parameter that enables advances in the semiconductor industry [65]. Although the improvements with scaling have been consistent for technology nodes until 90 nm, a number of fundamental physics limitation, previously neglected, have decreased the attractiveness of conventional bulk technology scaling beyond the referred node. The main physics limitations are Short Channel Effects (SCE), reduced carrier mobility, increased gate tunneling current and increased p-n junction leakage [128]. Moreover, according to the study published in [65], for nodes below 28 nm, using conventional bulk transistor techniques will increase the cost per gate by approximately 1.6%, mainly due to process complexity and unfeasible effective gate length reduction.

In this context, alternative manufacturing technologies, based on thin film, have been proposed to overcome the issues encountered by shrinking conventional MOS transistors, thus enabling to cross the 32 nm technology node barrier. The two main alternatives proposed by the industry were: the Fully depleted Silicon on Insulator (FD-SOI) [96, 136] and the Fin Field Effect Transistor (FinFET) [35, 38]. Both technologies use an undoped thin silicon film between source and drain, which enables a much better electrostatic control of the channel by the gate. As a result, the so called short channel effect and the sub-threshold leakage are greatly reduced [35, 136]. Furthermore, the undoped silicon also substantially reduce the variation of transistor's threshold voltage (V_{th}) induced by the fabrication process, thus enabling circuit's operation at lower supply voltages (V_{dd}). The FD-SOI and FinFET technologies are presented and compared to the conventional bulk technology in the sequel of this chapter.

2.2 The problem with scaling down conventional MOS transistors

Many parasitic effects have appeared when shrinking conventional MOS transistors bellow 100 nm. In fact, the so called short channel effects (SCE) arise when the distance between

the source and the drain reaches the order of magnitude of the depletion region. In this case, the voltage barrier in the channel drops, as depicted in Fig. 2.1 b, causing a decrease in V_{th}. In addition, biasing the drain/source terminal also influences the depth of the depletion region in a short channel transistor, as in Fig. 2.1 c. Therefore, the short channel effect is intensified by the polarization of the drain, an effect known as Drain Induced Barrier Lowering (DIBL).



a) Long chanel, $V_{DS} = 0$ b) Short chanel, $V_{DS} = 0$ c) Short chanel, $V_{DS} \neq 0$

Fig. 2.1: Lowering of the voltage barrier caused by the reduction of transistor's gate length.

In addition to short-channel effects, another phenomenon that also degrades electrical characteristics of short channel MOS transistors is the variation of the number of dopants in the channel, known in the literature as Random Dopant Fluctuation (RDF). In fact, RDF has become today the main source of variability of V_{th} [12]. Indeed, a MOS transistor fabricated in conventional 100 nm technology has an average of approximately 100 dopant atoms in its channel [73]. Since V_{th} is directly affected by variations in the channel's dopant concentration, the impact of RDF is magnified as the gate length shrinks. The result is a limited reduction of the nominal V_{dd} as technology nodes scale down, which also limits the reduction of the consumed static power from node to node.

To overcome the insufficient power and performance gains caused by the arising of the aforementioned parasitic effects, many improvements in the fabrication process have been proposed [13, 14, 41]. Despite all the advances in the conventional bulk manufacturing process, the short channel effects continued to degrade the gate electrostatic control over the channel as technology nodes scaled down. Hence, the industry was forced to search alternative manufacturing technologies to continue the scale down of transistors.

2.3 Alternatives to conventional bulk technology

2.3.1 Silicon on insulator

One of the alternatives to advance beyond the 32 nm technology node was adding a layer of oxide insulator in the substrate (buried insulator or BOX), as depicted in Fig. 2.2a. Thus, the source, drain and channel are separated from the substrate (also known as body or back plane). The addition of a BOX enabled reducing the junction parasitic capacitances, increasing the

electrostatic control of the channel, and also reducing SCE. Hence, the performance is improved while decreasing the dynamic consumption [20], what enabled the crossing of the technological barrier imposed by short channel effects.

There are several types of manufacturing technologies that use silicon on insulator [20, 34]. The basic difference between each one of them is the thickness of the silicon film on the top of the BOX (t_{si}), and the thickness of the BOX itself (t_{BOX}). One of the first proposed technologies was the Partially Depleted Silicon on Insulator (PD-SOI), illustrated in Fig. 2.2b. It contains a thick top silicon layer, t_{si} is larger than the depth of the depletion region [20]. Thus, the channel is only partially occupied by the depletion region, what explains its denomination. Although PD-SOI transistors have been the focus of many scientific publications [10, 104, 129], the fluctuation of V_{th} caused by the circuit switching history made PD-SOI a deprecated technology.

The problem with PD-SOI was solved by reducing t_{si} to the same order of magnitude of the depletion region. In this case, the channel is fully occupied by the depletion region, which explains the reason for the name Fully Depleted Silicon on Insulator (FD-SOI). A thinner top silicon layer has shown to improve SCE, increase transconductance, improve sub-threshold

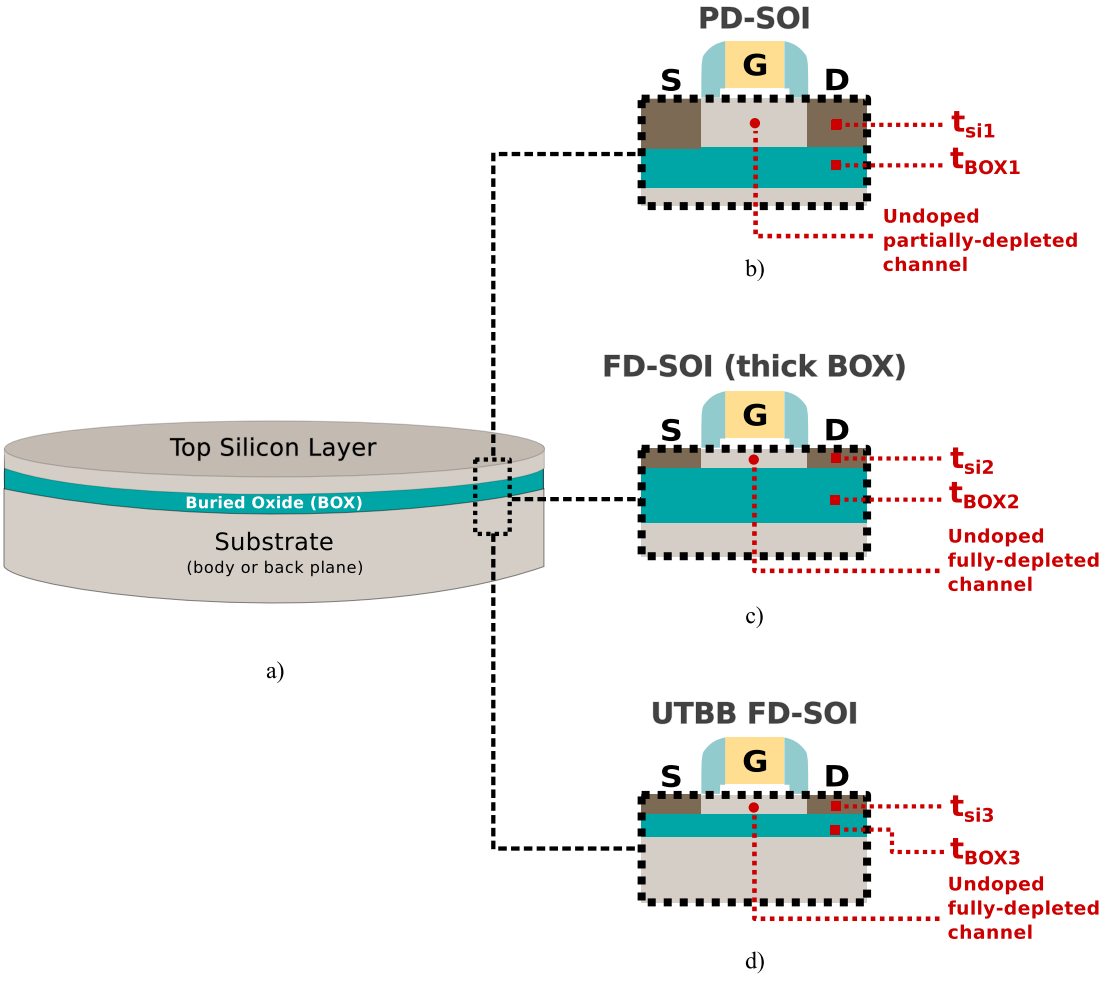


Fig. 2.2: Cross section of PD-SOI (b), FD-SOI (thick box) (c) and UTBB FD-SOI (d) transistors built from silicon-on-insulator base waver (a). t_{si} represents the thickness of the top silicon layer and t_{BOX} represents the thickness of BOX. $t_{si1} > t_{si3}$; $t_{si2} = t_{si3}$; $t_{BOX1} > t_{BOX3}$; $t_{BOX2} > t_{BOX3}$. Figure based on information available in [139].

slope, and increase soft errors tolerance [32, 43, 140, 142].

Once t_{si} is reduced to the point of generating a fully depleted channel, two technologies flavors are achievable by adjusting t_{BOX}: The FD-SOI with thick BOX, depicted in Fig. 2.2c and the Ultra Thin Body and BOX FD-SOI (UTBB FD-SOI), shown in Fig. 2.2d. As illustrated Fig. 2.2, the top silicon layer of FD-SOI and UTBB FD-SOI have the same thickness: $t_{si2} = t_{si3}$; and the BOX of the UTBB FD-SOI is thinner: $t_{BOX3} < t_{BOX2}$. As a result previous experimental and simulation work has shown that, not only the UTBB FD-SOI has been proven to have considerably reduced SCE [34,64,113,142,150,155,167], but also a thin BOX allows calibrating transistors V_{th} by gate biasing [108, 151].

Thanks to these advantages and the advances the technique for manufacturing SOI wafers, the UTBB FD-SOI technology prevails as the SOI alternatives to replace conventional bulk. Further details on UTBB FD-SOI will be given in the next section.

2.3.2 Fin field-effect transistors

The other alternative adopted by the industry to continue scaling down transistors beyond 32 nm was developing the Fin Field-Effect Transistor (FinFET) technology. This solution was largely supported by Intel corporation [87]. In this 3D manufacturing technology, the drain and the source are raised out of the substrate, forming a shape known as fin. The gate surrounds the fin in a perpendicular axis, as depicted in Fig. 2.3 a. A nitrided hard mask isolates the top part of fin. Consequently, the channel is formed in the XX' direction and the carriers move in the YY' direction. With this configuration, a better electrostatic control of the depletion region is obtained compared to regular SOI transistor. Furthermore, the influence of the drain electric field on the channel is reduced, thus reducing SCE [35].

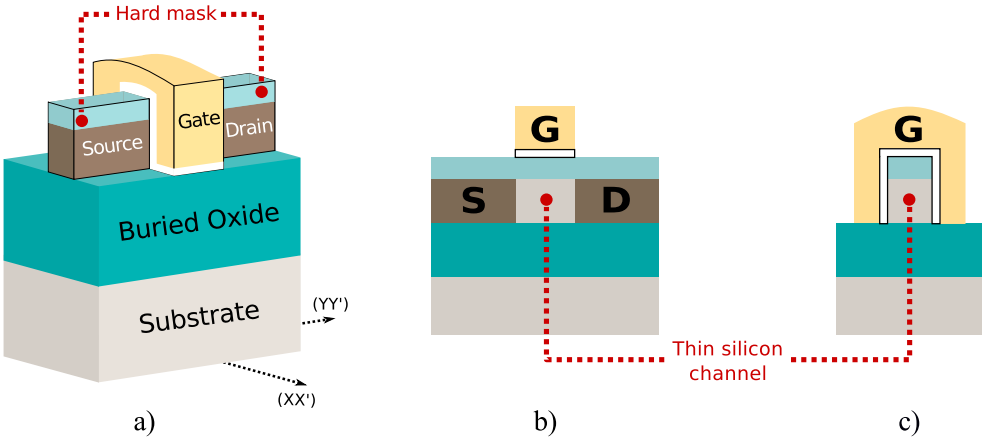
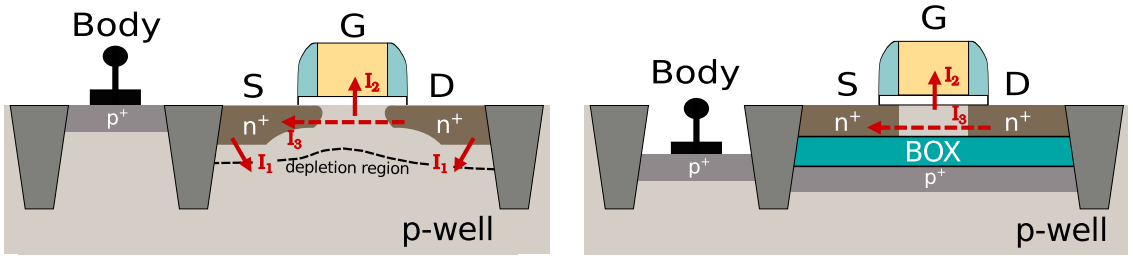


Fig. 2.3: 3D schematic (a) and cross sections YY' (b) and XX' (c) of a FinFET transistor.

From an electrostatic point of view, FinFET transistors are better than FD-SOI transistors. The former has also shown to have better performance results [60, 168]. However, they are much more difficult to manufacture [60]. The simplified planar manufacturing process of FD-SOI transistors allow reducing the fabrication time if compared to FinFET. In addition, the structure of FD-SOI transistors is very close to that of conventional bulk. Therefore, adapting existing circuit designs from conventional bulk to FD-SOI technology is simpler than adapting it to FinFET.

2.4 The UTBB FD-SOI transistor

A typical cross section of an UTBB FD-SOI transistor is shown in Fig. 2.4b and compared to a cross section of a conventional bulk transistor, in Fig. 2.4a. As explained in the previous section, the main difference between these technologies is the insertion of the ultra thin BOX in the UTBB FD-SOI, separating the thin silicon film that forms source, drain and the channel from the substrate of the transistor (p-well in Fig. 2.4b).



(a) (b)

Fig. 2.4: Classical Bulk (a) and FD-SOI (b) NMOS transistor cross sections. The red arrows represent the main leakage current components: I_1 is the junction leakage; I_2 is the gate leakage; and I_3 is the subthreshold leakage. In UTBB FD-SOI technology, the path for junction leakage is eliminated, and the gate and subthreshold leakages are considerably reduced.

2.4.1 Advantages of a thin silicon film

The extremely thin top silicon layer of UTBB FD-SOI transistors provides a much better electrostatic control than conventional bulk [69]. For achieving optimal electrostatic behavior, t_{si} is kept in the order of one third of the gate length value [97, 135]. For instance, $t_{si} \cong 12$ nm in UTBB FDSOI 28 nm technology [137]. As a result, two major advantages: the first one is a reduced subthreshold slope [82]. This parameter reflects the capability of the gate to effectively control the current flow through the channel. The closer the subthreshold slope is to the theoretical minimum value of 60 mV/dec, the higher is the gate control over the channel what consequently reduces the gate leakage (I_2 in Fig. 2.4a) [69].

The second major advantages of a better electrostatic control is the reduction of short-channel effects, especially DIBL [69, 97]. According to its theoretical equation [135], the value of the DIBL is directly proportional to the depth of the source and drain junctions. Since in UTBB FD-SOI the depth of the junctions is t_{si}, which is considerably smaller than the corresponding depth in conventional bulk, the value of DIBL is considerably reduced in UTBB FD-SOI. The experimental demonstration of reduction of DIBL is depicted in Fig. 2.5, extracted from [16].

In [16], a comparison with different DIBL values obtained for the conventional bulk (circles), FD-SOI (squares) and FinFET (stars) technologies is presented, as depicted in Fig. 2.5. The presence of a thin top silicon layer make the FD-SOI and FinFET DIBL values smaller than the measurements obtain in conventional bulk technology, for every gate length shown in Fig. 2.5. Additionally, the measurements obtained with FinFET are slightly smaller than the corresponding FD-SOI measurements due to the improved electrostatic control obtained with the former, as mentioned in section 2.3.2.

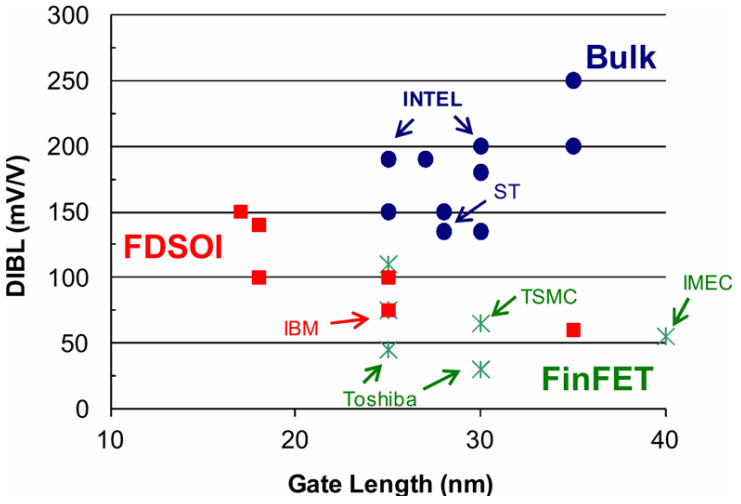


Fig. 2.5: Measurements of the DIBL for different gate lengths obtained for in conventional bulk, FD-SOI and FinFET technologies [16].

Finally, the combination of reduced short-channel effects and reduced subthreshold slope achieved in the UTBB FD-SOI induces a reduction in the subthreshold leakage (I_3 in Fig. 2.4a).

2.4.2 Advantages of an undoped channel

The isolation provided by the BOX free the UTBB FD-SOI technology from the obligation of doping the channel, as is the case for the conventional bulk technology. An undoped channel brings two major improvement: removing the random dopants fluctuation (RDF) of the channel and reducing the V_{th} variability, which are considered as two of the most critical challenges for continuing the scale down in CMOS technology [12, 161]. Therefore, for the same gate length, an UTBB FD-SOI transistor has a coefficient of variability of threshold voltage (AV_t) approximately three times lower than an equivalent transistor in conventional bulk technology [29,116]. The values of AV_t for conventional bulk, FD-SOI, and FinFET technology are depicted in Fig. 2.6 [16]. The smaller values obtained with the FD-SOI technology demonstrates that it is less subject to local V_{th} variations than conventional bulk technology.

Less variability means less power and performance differences between process corners fast-fast (FF) and slow-slow (SS). Thus, less margin needs to be added by the logical synthesis and place and route tools to guarantee timing closure. Therefore, the circuits designed in UTBB FD-SOI technology operate in a faster frequency than an equivalent circuit designed in the same technology node in conventional bulk.

Another advantage of an undoped channel is limiting the Gate induced Drain leakage (GIDL), one of the components of current leakage in MOSFET transistors. Previous studies show that the GIDL is very low in UTBB FD-SOI technology, in the order of a few $pA/\mu m$ [22, 28, 29].

2.4.3 Advantages of the isolation with a BOX

The presence of the BOX, that completely isolates the source/drain from the substrate imposes certain advantages. The most straightforward one is the complete elimination of the current leakage from source/drain to the substrate, marked as I1 in Fig. 2.4a. Eliminating one of the

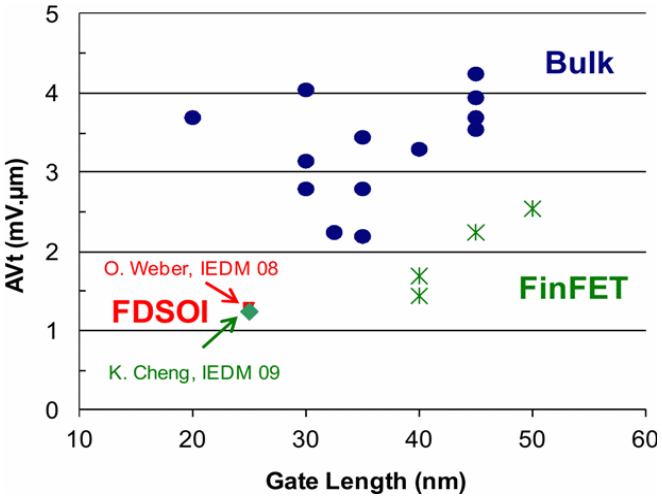


Fig. 2.6: Measurements of the V_{th} variation for different gate lengths obtained for conventional bulk, FD-SOI and FinFET technologies [16].

sources of leakage that exists in conventional bulk technology allows reducing the static power consumption in FD-SOI technology [33].

Furthermore, the insertion of the BOX limits the depth of source and drain, which allows reducing the diffusion surface. As a consequence, a reduced parasitic junction capacitance is achieved [97]. Considering that the source/drain terminals of transistors are connected to each other to form logic gates, and considering that the output capacitance seen by a certain logic gate is the equivalent of all junction capacitances of all source/drain terminals connected to the output of that logic gate, reducing the junction capacitance directly reduces the energy required to switch a logic gate state. Therefore, the dynamic power consumption in an UTBB FD-SOI circuit is considerably lower if compared to an equivalent in conventional bulk operating at the same frequency [97].

Another positive effect of the BOX addition is the elimination of the latch-up [128]. This phenomenon occurs in conventional bulk technology, under some specific situations. A parasitic thyristor based structure forms between adjacent transistors, thus inducing a large current to flow from V_{dd} to Gnd. The latch-up generally has a destructive effect to CMOS circuits and is a major problem in CMOS systems [61]. In FD-SOI, thanks to the BOX and the Shallow Trench Isolation (STI depicted in Fig. 2.4b), the adjacent transistors are electrically isolated from each other. Consequently, the parasitic bipolar transistors, formed in conventional bulk by the juxtaposition of n-wells and p-wells, are suppressed. The latch-up effect is thus eliminated in the FD-SOI technology.

2.4.4 Advantages of an ultra thin BOX

In UTBB FD-SOI technology, as its acronym suggests, an ultra thin BOX is used. In the 28 nm node, for instance, $tbox \cong 25$ nm [137]. It has been demonstrated that a thinner BOX strengthens the electrostatic control over the channel by reducing the DIBL [107]. The short channel effects are also decreased with a thin BOX due to the suppression of the lateral electrostatic coupling that exists between source, drain and channel of transistors with a thick BOX [97, 150]. As a result, the reduction of $tbox$ enhances the scalability of UTBB FDSOI transistors down to

the 11 nm node with an almost constant tsi [97].

2.5 Modulating the V_{th} of UTBB FD-SOI transistors

In order to meet the tight power and performance constraints of nowadays complex systems, the use of transistors with different V_{th} is mandatory. In high performance designs, for instance, low V_{th} transistors are commonly used in critical paths to increase the performance of the overall system, whereas high V_{th} transistors are preferred for non-critical paths, so that the static power consumption is reduced. Thus tuning V_{th} is necessary for the establishment of any CMOS technology in the deep sub-micro era.

2.5.1 Modulating V_{th} through manufacturing techniques

The conventional bulk technology proposes three levels of Vth, high; regular; and low [11,148]. In order to create these variants, the V_{th} is modified either by controlling the doping of the channel, or by changing the gate stack used [11]. These two options were not kept in the UTBB FD-SOI. Indeed, as described in previous sections, the channel in UTBB FD-SOI is undoped to reduced variability. Thus, doping the channel would increase the variability of the transistors. Moreover, the second method considerably raises the manufacturing cost and complexity.

Thus, in UTBB FD-SOI technology a third method for creating a multi V_{th} platform have been used. The substrate underneath the BOX is doped to a high level concentration [46, 107], illustrated by the p+ layer in Fig. 2.4b, also known as back plane. Therefore, adjusting V_{th} of the transistors is done by modulating only the type and doping levels of the back plane while keeping the same gate metal type. This technique was initially used to improve the electrostatic integrity of the channel [45]. It is nowadays used to generate transistors with different V_{th} levels. Depending on the type of dopants used in the back plane, two V_{th} level possibilities are used in UTBB FD-SOI: a low V_{th} option (LVT), and a higher V_{th} option, which is known as regular V_{th} (RVT).

In the RVT configuration, the back plane dopant type is the opposite of source and drain dopants, which causes an increase in transistors V_{th}. A cross section schematic of a NMOS and a PMOS RVT transistors is depicted in Fig. 2.7. In this case, the p-well and n-well disposition is equal to the conventional bulk technology: the NMOS lies over a p-well and the PMOS lies over a n-well. Due to the similarity with the conventional bulk, this architecture is known as conventional well.

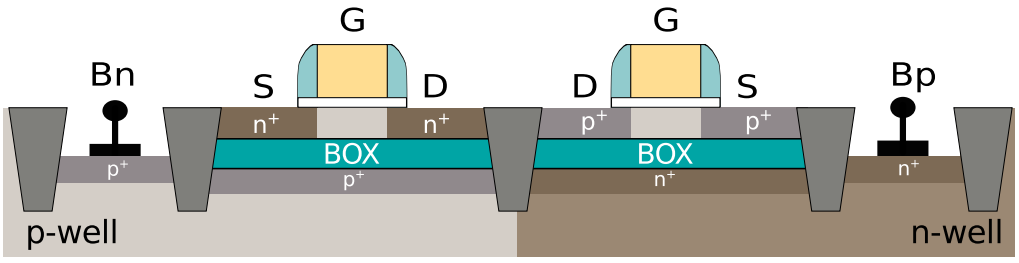


Fig. 2.7: Cross section of NMOS and PMOS UTBB FD-SOI transistors with conventional well configuration (RVT transistors).

Conversely, in the LVT configuration, the back plane dopant type is the same of source and drain dopants, which causes an decrease in transistors V_{th}. A cross section schematic of a NMOS

and a PMOS RVT transistors is depicted in Fig. 2.8. Thus, the p-well and n-well dispositions are flipped if compared to the conventional bulk technology: the NMOS lies over a n-well and the PMOS lies over a p-well. This disposition of n-wells and p-wells are only possible since the BOX provides electrical isolation between source/drain and the back plane. It is commonly referred to as flip-well.

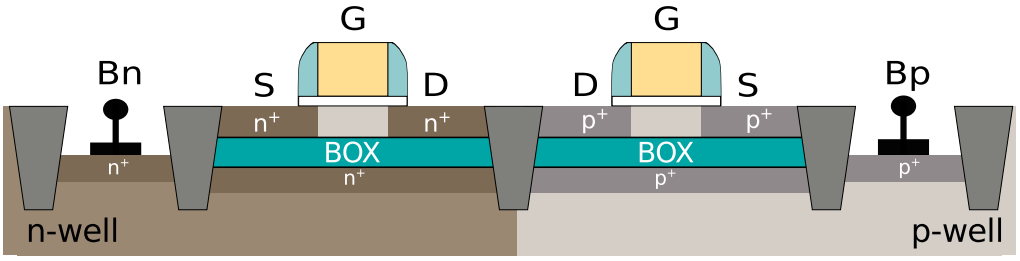


Fig. 2.8: Cross section of NMOS and PMOS UTBB FD-SOI transistors with flip well configuration (LVT transistors).

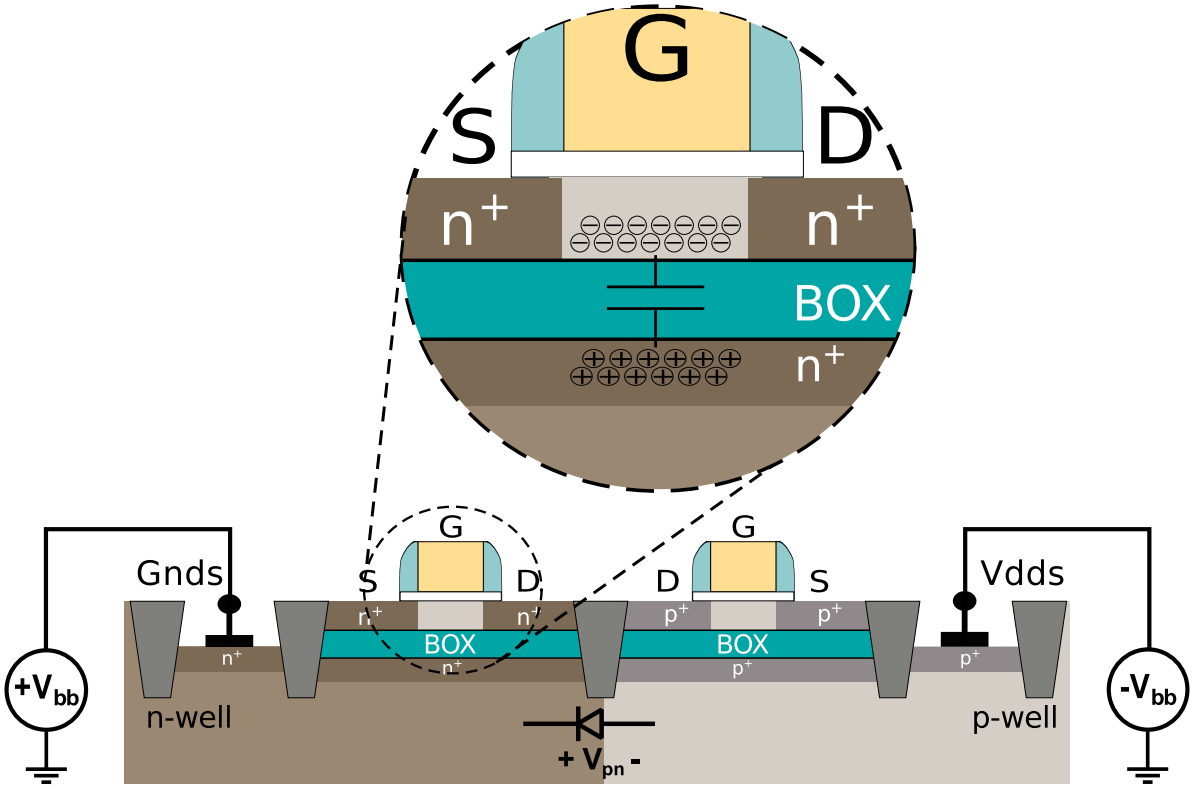
2.5.2 Modulating V_{th} post manufacturing: Body Biasing

Once the transistors are fabricated, the V_{th} achieved by adjusting the back plane doping, as mentioned in the previous section, is fixed and can not be modified during circuit operation. However, the UTBB FD-SOI technology provides yet another knob for modulating the V_{th} post manufacturing. Thanks to the ultra thin BOX, applying a voltage to the back plane modifies the V_{th} of the transistors, a technique known as body biasing [81]. Therefore, V_{th} can be adjusted even during circuit operation, thus increasing the frequency of the circuit or reducing its static power consumption [9, 26, 40, 93, 144]. Body biasing has been also used to compensate process variation, since the biasing voltage is applied post manufacturing [51, 143, 146].

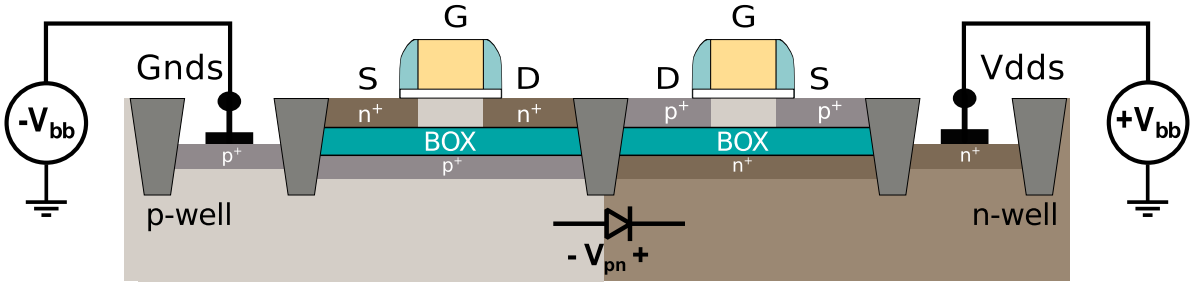
Boosting the performance of a target system is done by applying a positive voltage to the n-well (+V_{bb}) and a negative voltage to the p-well (-V_{bb}), as depicted in Fig. 2.9a. The result is the accumulation of negative charges in the channel of the NMOS transistor, as illustrated in the zoom of Fig. 2.9a. Analogously, positive charges are accumulated in the channel of the PMOS transistor. Since the induced excess of charges facilitates transistors switching, the V_{th} decreases. As V_{bb} increases, so does the concentration of charges in both PMOS and NMOS, thus further decreasing V_{th}. Thus, the operation speed increases and so does the subthreshold leakage. The aforementioned body biasing scheme is known as forward body biasing (FBB).

Conversely, reducing the system's static consumption is done by applying a negative voltage to the n-well (-V_{bb}) and a positive voltage to the p-well (+V_{bb}), as depicted in Fig. 2.9b. The result is the accumulation of positive charges in the channel of the NMOS transistor, and negative charges in the channel of the PMOS transistor. Since the induced excess of charges makes transistors switching more difficult, the V_{th} increases. As V_{bb} increases, so does the concentration of charges in both PMOS and NMOS, thus further increasing V_{th}. Thus, the static power consumption decreases and so does the operation speed. The aforementioned body biasing scheme is known as reverse body biasing (RBB).

Body biasing is also used in conventional bulk technology. Nonetheless, body biasing a conventional bulk transistor with a voltage higher than the range of $\pm$ 0.3 V cause undesired effects [76]. For instance, FBB is done by applying a positive voltage to the p-well of an NMOS transistor, which directly bias the substrate/source PN junction. The drawbacks are the increase of the junction leakage consumption (I_1 in Fig. 2.4) and the augmented risk of latch-up.



(a)



(b)

Fig. 2.9: Cross section view of UTBB FD-SOI NMOS and PMOS LVT (a) and RVT (b) transistors. The LVT transistors are body biased with a FBB scheme (a), while the RVT transistors are biased with a RBB scheme (b); the body biasing scheme in which V_{bb} is wider in both cases. The zoom in (a) shows the carriers accumulation induced by V_{bb}.

Conversely, RBB is done by applying a negative voltage to the n-well of a conventional bulk PMOS, thus directly biasing its substrate/source PN junction at the cost of an increased GIDL.

In UTBB FD-SOI technology the isolation provided by the BOX eliminate theses drawbacks, since there is no junction leakage (I_1 in Fig. 2.4) nor latch-up in UTBB FD-SOI. Additionally, the increased body factor provided by the insertion of the BOX indicates a better control of V_{th} by applying a biasing voltage (V_{bb}) to the substrate. It has been shown that the body factor is approximately 85 mV/V in UTBB FD-SOI and 25 mV/V in conventional bulk for the 28 nm node [34]. The BOX also increases the voltage range of body biasing to approximately $\pm$ 3 V. In fact, the maximum V_{bb} is imposed by the diode formed between p-well and n-well, shown in Fig. 2.9a and Fig. 2.9b and replicated in Fig. 2.10. If this diode is inversely

biased, the preferred scenario, the maximum voltage that can be applied to the p-n junction (V_{pn} in Fig. 2.10) that do not generate undesired effects is the diode's breakdown voltage. A higher V_{pn} would significantly increase the leakage by avalanche breakdown. This ideal scenario is achieved in UTBB FD-SOI by implementing an FBB scheme in LVT transistors or with RBB in RVT transistors. For the 28 nm node, the breakdown voltage is approximately 7 V. Thus, the maximum allowed V_{pn} is 7 V, which enables a body biasing of $V_{bb} = \pm$ 3 V.

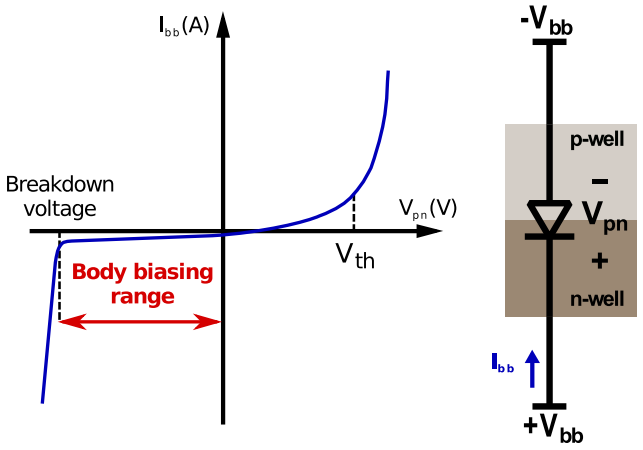


Fig. 2.10: Range of body biasing in FD-SOI technology. The diode formed by the p-well and n-well junction needs to be reverse biased to limit current leakage.

On the other hand, directly biasing the diode is also allowed though with a very reduced voltage range. In this case, the maximum V_{pn} is the diode's V_{th} (approximately 0.6 V in the 28 nm node), as depicted in the right-hand side of the graph in Fig. 2.10. Higher V_{pn} values would bring the diode to the forward region, exponentially increasing the leakage. This non ideal scenario is achieved in UTBB FD-SOI by implementing an RBB scheme in LVT transistors or with FBB in RVT transistors.

2.5.2.1 Performance and power gains

Many studies have shown the efficacy of using body biasing schemes to enhance performance or reduce power consumption [16, 31, 40, 156]. In [16], different IP blocks, including an ARM Cortex-A9 CPU, were electrically simulated with RC extracted models. As depicted in the left side graph of Fig. 2.11, if operation at V_{dd} = 1.3 V a gain of 40 % in operation frequency is achievable by implementing a FBB scheme with a V_{bb} = 1.0 V in UTBB FD-SOI 28 nm LVT transistor compared to an equivalent circuit implemented in conventional bulk technology. The gains are further enhanced to a factor of 5X at V_{dd} = 0.45 V.

Conversely, if the RBB scheme is implemented in UTBB FD-SOI technology, a significant leakage reduction is achievable compared to an equivalent implementation in conventional bulk. In the right side graph of Fig. 2.11, a leakage current reduction by a factor of 10X is reported for a V_{bb} = 1.5 V. These results motivates the use of body biasing in UTBB FD-SOI, especially for circuits operating at low supply voltage.

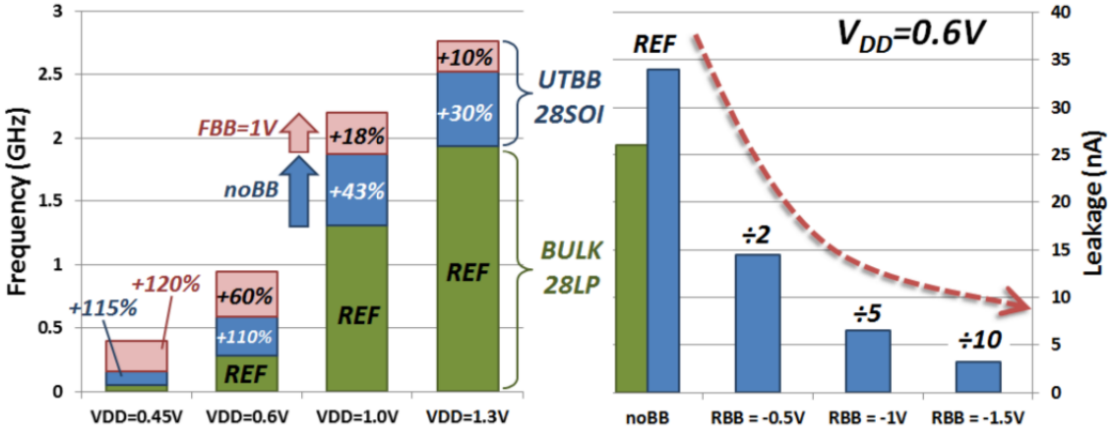


Fig. 2.11: Performance gains for various V_{dd} obtained with FBB scheme and LVT transistors (left); and leakage reduction for different V_{bb} values and V_{dd} = 0.6 V, obtained with RVT transistors with RBB scheme (right) [16].

2.6 Overall Analysis

Table 2.1 compares the UTBB FD-SOI, conventional bulk and FinFET technologies in terms of the parameters discussed in this section: manufacturing cost, short channel effects containment, power efficiency and performance. The evaluation levels (good, fair and poor) are comparative to other technologies in the same node. For instance, the body biasing range of the conventional bulk technology is poor if compared to the UTBB FD-SOI at the same technology node (28 nm).

The UTBB FD-SOI technology show good results in all the evaluated parameters. Compared to the conventional bulk, it is superior in every aspect, except for the manufacturing cost, in which both conventional bulk and UTBB FD-SOI are similar. The FinFET technology presents a good overall evaluation, especially in the performance parameter. The main draw-

Table 2.1: Comparison of manufacturing cost, power consumption and performance on conventional bulk, UTBB FD-SOI and FinFET technologies.

Good Fair Poor	Conventional Bulk	UTBB FD-SOI		FinFET
	28 nm	28 nm	14 nm	14 nm
Manufacturing Cost	☺	☺	☺	☹
SCE Containment	😐	☺	☺	☺
DIBL Containment	😐	☺	☺	☺
Ultra Low Voltage Capability	😐	☺	☺	☺
Power efficiency	😐	☺	☺	😐
Body Biasing Range	☹	☺	☺	☺
Performance	😐	😐	😐	☺
Latch-Up Immunity	☹	☺	☺	☺

back of this technology is the extremely high manufacturing cost and complexity. Hence, the UTBB FD-SOI technology emerges as a key solution for the 28 and 14 nm nodes, especially for low power applications.

2.7 Conclusion

In this chapter, the UTBB FD-SOI technology has been deeply analyzed and compared to the conventional bulk and FinFET technologies. The UTBB FD-SOI has shown to be a good candidate to replace the conventional bulk technology in the in the deep sub-micron era, and a very suitable alternative for the FinFET technology. Thanks to a very thin top silicon layer and the insertion of a very thin BOX, a better electrostatic control is achieved, greatly reducing short channel effects; the dynamic power consumption and the leakage are reduced; and the variability is controlled. Moreover, the body biasing voltage range is considerably increased, which opens new perspectives for performance boosting, static power consumption and post silicon variability control.

Chapter 3

The Asynchronous Circuits

3.1 The limitations of synchronous circuits

Synchronous circuits are architectures in which the data flow is governed by a global synchronization signal: the clock. This periodic signal is connected to all memory elements of a system, as depicted in Fig. 3.1, to indicate the correct moment to memorize the input data. Therefore, in order to avoid the propagation of incorrect data, the clock needs to be slow enough to let data propagate through the slowest path of the system, known as critical path (the bottleneck of the system performance). Thanks to the simplicity of the global clock synchronization, the synchronous circuits have dominated the microelectronics design industry since the 1960s [15].

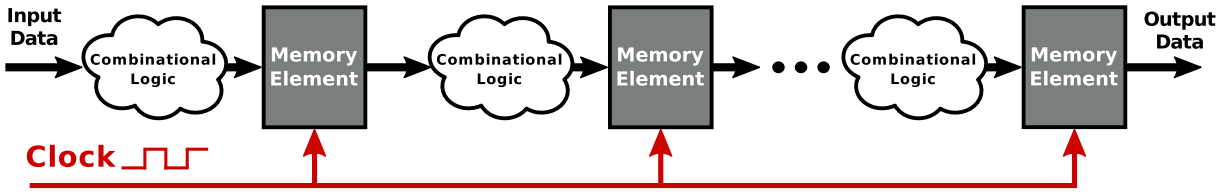


Fig. 3.1: Abstraction of a synchronous system.

However, the increasing integration density imposed by the newest manufacturing technologies have significantly increased the complexity of designing synchronous circuits. Most of the limitations faced are related to intrinsic restrictions of the global synchronization:

- The circuit frequency is limited by the critical path. Thus, even if some pipeline stages have already generated their outputs, the results will only be propagated once the critical path has finished calculating.
- Ideally, the clock must simultaneously reach all the memory elements. A small difference in the arrival time of the clock in different parts of the circuit, known as clock skew, may cause a malfunction of the system. Thus, the correct distribution of this signal throughout a large system is nowadays a very challenging task.
- The circuitry required to properly distribute the clock, namely the clock tree, consumes between 20 - 45% of the total energy consumed by a circuit [134].

- Each pipeline stage of the system consumes dynamic power on both edge of the clock, even if the system is not processing any new data.

- The modularity, an important aspect for reusing already synthesized IPs, is a major problem in the integration of synchronous systems. It is not guaranteed that an IP already designed to a target frequency will correctly function if integrated to a system designed to operate at a different clock frequency.

- Significant electromagnetic radiations are emitted at the clock frequency, since the activity of synchronous circuits is concentrated close to the positive edge of the clock [121].

Therefore, due to the aforementioned limitations, the development of complex systems as well as the high performance requirements have steered designers towards new design approaches based on asynchronous logic. The idea is replacing the global clock by a local communication protocol. The clock suppression is able to overcome the aforementioned limitations, thus increasing the attractiveness of asynchronous circuits in recent years.

3.2 The asynchronous circuits principle

Asynchronous circuits are locally synchronized systems. They are composed of functional blocks that are activated by the presence of data at their inputs and/or outputs. A typical abstraction of this type of system is depicted in Fig. 3.2. Compared to the synchronous system of Fig. 3.1, the global clock signal has been replaced by local request and acknowledgement signals. They implement a local handshake protocol that must be respected between the adjacent blocks. The block N+1, for instance, will start processing its input data ($Data_{N+1}$) only if the signal $request_{N+1}$ is received, indicating that $Data_{N+1}$ is valid. Once $Data_{N+1}$ is memorized by the block N+1, the $acknowledgement_{N+1}$ signal indicates to the block N that it is now allowed to start processing new data. The result of the calculation done in the block N+1 will then be transmitted to the block N+2 via $Data_{N+2}$ and $request_{N+2}$.

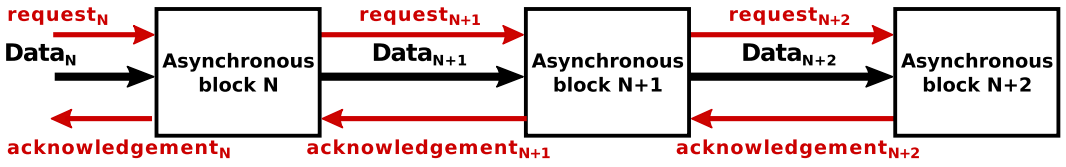


Fig. 3.2: Typical representations of an asynchronous systems.

This succession of requests and acknowledgements are implemented in each block interface of an asynchronous system, and governs the data flow throughout the system. The result of such data transfer sequence is: 1) the system latency is minimal and equal to the time required for the module to perform the calculation and generate its output [37, 163]. The latency may vary for different calculations; 2) the throughput of the system is maximum and it corresponds to the maximum possible speed for processing the received data [163].

The aforementioned data transfer sequence is one of the possibilities of communication protocol that is used in asynchronous circuits. A more detailed description of the most commonly used protocols will be given in the sequel this chapter.

3.3 Data encoding and signaling

In asynchronous circuits, as describe in the previous section, there is no global clock to define instant in which an input data is considered valid. Therefore, it is the duty of request and acknowledgement signals to indicate data validity. The former indicates the arrival of new data, and the latter mark the end of the calculation. Thus, to ensure a correct synchronization between different blocks, a request signal must be associated to every data signal of the system. This concept requires a special encoding of information in asynchronous circuits. The two most popular ones are bundle data encoding and delay insensitive encoding, to be described in details in the following subsection [122, 141].

3.3.1 Bundled-data encoding

In bundled-data encoded systems, data validity is signaled by a dedicated request signal, as depicted in Fig. 3.2. Therefore, the transmitted data is encoded in a traditional way as the encoding scheme used in synchronous circuits: each bit is encoded by a single wire. A small amount of required wires and logic gates leads to an area efficient implementation of bundle-data encoded asynchronous circuits [122].

Moreover, in bundled-data encoding the request signals operate as local clocks for each asynchronous block, indicating the moment in which the data signal is valid [141, 170]. Consequently, the request must be implemented with the adequate delay to ensure that it wont be asserted before the respective data signal is effectively valid [50, 68, 106]. This timing assumption forces the request signal to be delayed from the sender to the receiver in order to match the sender's worst case computation delay (plus margin). Hence, the speed of data propagation from block to block is bounded by the local worst case delay.

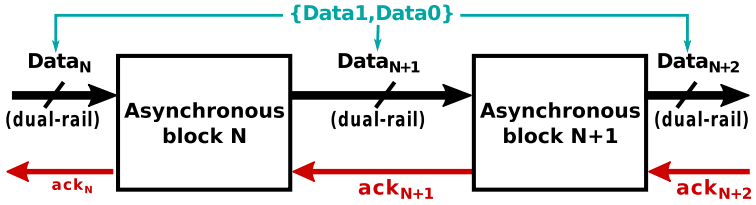
3.3.2 Delay insensitive encoding

A more sophisticated alternative to bundled-data encoding is done by merging data information and validity in the same signal. In delay insensitive encoding, the request signal is eliminated and the data signal is implemented in a multi-rail encoding: each bit of information is encoded by multiple wires. This approach enables detecting a new data as soon as it has arrived at the input channel of an asynchronous block and simultaneously ensure its validity. Therefore, there are no temporal assumptions between data and request, which explains the name delay insensitive encoding.

Many multi-rail encoding schemes exist [48, 120]. They are know as M-of-N encoding, in which M indicates the number of wires that needs to be asserted simultaneously to indicate a new input data, and N represents the total number of wires used to transmit a single bit of information. The most used M-of-N encoding is the 1-of-2, also known as dual-rail encoding. An abstraction of a typical dual-rail encoded system is shown in Fig. 3.3a. Unlike the bundled-data system depicted in Fig. 3.2, the dual-rail system of Fig. 3.3a has no request signal and two wires to represent each data bit: $Data1$ and $Data0$.

Fig. 3.3b shows the information carried by the tuple $\{Data1, Data0\}$. In dual-rail encoding, the net 0 ($Data0$) caries the information of a 0 bit, and the net 1 ($Data1$) caries the information of a 1 bit. Therefore a 0 bit is encoded by $\{Data1, Data0\}$ = 01 and a 1 bit is encoded by $\{Data1, Data0\}$ = 10. To properly detect two consecutive bits with the same value, a different code word needs to be send between every valid information bit, a step of the asynchronous

data exchange known as return-to-zero. It is encoded by the word $\{Data1,Data0\} = 00$. The steps to successfully transmit a data between adjacent asynchronous blocks is defined by the implemented communication protocol, which will be detailed in the next section.



(a)

Data1	Data0	State
0	0	invalid
0	1	valid 0
1	0	valid 1
1	1	not used

(b)

Fig. 3.3: Typical representations of a dual-rail encoded asynchronous systems (a). The information encoded by the tuple $\{Data1,Data0\}$ is depicted in (b).

3.4 Communication protocols

A synchronization protocol, also referred to as handshake protocol, is a set of rules that governs data exchange between the blocks of an asynchronous circuit. Each block of the asynchronous system must be implemented with the same communication protocol. Two basic characteristics differentiate the protocols: 1) the data encoding used; and 2) the data transfer sequence. Based on these two properties, the different communication protocols proposed in the scientific literature are classified in two categories: two-phase protocols, in which a complete data transfer is done in two steps; and four-phase protocols, in which the data transfer is done in four steps. The choice on the protocol to be used is essential to the design of asynchronous circuits and determines the system total area, performance, power consumption and robustness [111, 112, 138, 153].

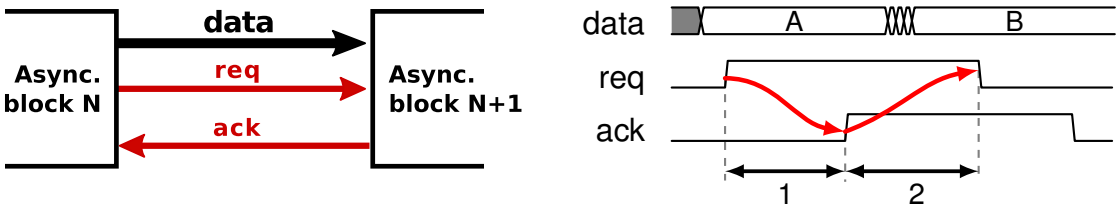
3.4.1 Two-phase protocols

The waveforms of a two-phase protocol for a single data transfer between asynchronous blocks is depicted in Fig. 3.4 and Fig. 3.5. The former shows the implementation of the protocol in a bundled-data encoded system while the latter represent the implementation in a dual-rail encoded system. The two-phase protocol is the minimal sequence allowing data exchange between two blocks.

In phase 1: the sender (Async. block N in Fig. 3.4 and Fig. 3.5) inputs a valid data to the receiver (Async. block N+1 in Fig. 3.4 and Fig. 3.5). The latter detects the data, process it and then sends the acknowledgment signal to the sender, indicating that the communication channel is free and new data can be now send. In phase 2: the sender detects the acknowledgement. This phase ends with the arrival of a new valid data.

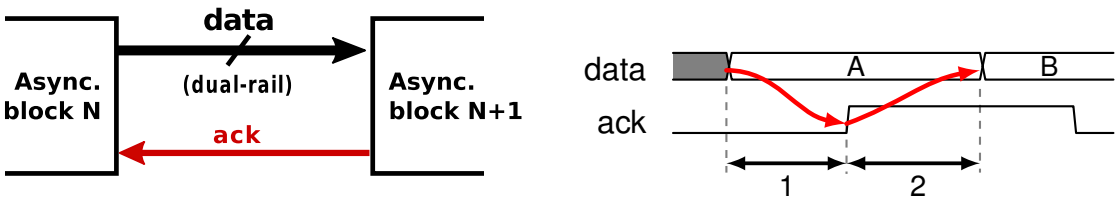
3.4.2 Four-phase protocols

The waveforms of a four-phase protocol in a bundled-data encoded system and dual-rail encoded system are depicted in Fig. 3.6 and Fig. 3.7 respectively. This protocol is also know as Return



(a) (b)

Fig. 3.4: Two-phase protocol implemented in a bundled-data encoded asynchronous system (a). The red arrows in the waveform (b) highlight the 2 phases of a complete transfer of data A. The transfer finishes when a second valid data (B) arrives.



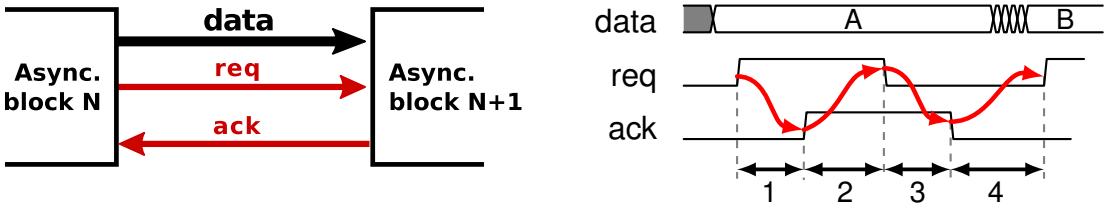
(a) (b)

Fig. 3.5: Two-phase protocol implemented in a dual-rail encoded asynchronous system (a). The red arrows in the waveform (b) highlight the 2 phases of a complete transfer of data A. The transfer finishes when a second valid data (B) arrives.

to zero (RTZ), since the request and acknowledgment signals must be reseted before a new data transfer. In a dual-rail encoded system, the data channel need to be set to the invalid state before beginning a new data transfer. This is done by setting $\{Data1, Data0\} = 00$, as explained in section 3.3.2.

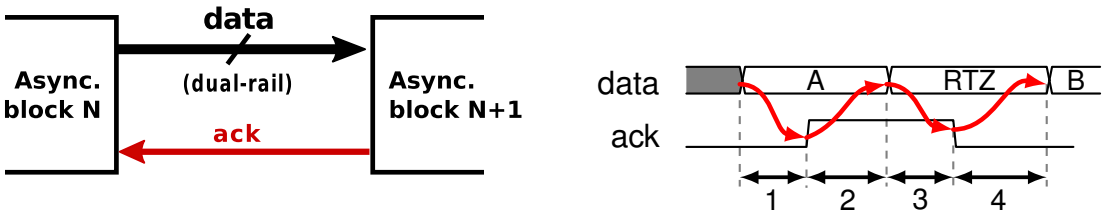
The phase 1 starts when the sender requests a new data transfer by asserting the req signal, as soon as data A is available. The receiver then detects the req, processes the received data and assert the ack signal. In phase 2, the sender detects the ack signal and resets the req signal. In a dual-rail encoded system (Fig. 3.7), this phase is also known as RTZ. In phase 3 the receiver detects the reset of req and also resets ack. Finally, phase 4 finishes when the sender detects the ack reset, thus the communication channel is ready to receive data B.

At a first glance, since fewer transitions are needed for transferring data with a two-phase protocol, its implementation seems to generate faster asynchronous circuits that even consume



(a) (b)

Fig. 3.6: Four-phase protocol implemented in a bundled-data encoded asynchronous system (a). The red arrows in the waveform (b) highlight the 4 phases of a complete transfer of data A. The transfer finishes when a second valid data (B) arrives.



(a) (b)

Fig. 3.7: Four-phase protocol implemented in a dual-rail encoded asynchronous system (a). The red arrows in the waveform (b) highlight the 4 phases of a complete transfer of data A. The transfer finishes when a second valid data (B) arrives.

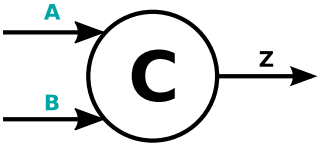
less dynamic power than a four-phase implementation. However, according to most of the reported cases, this impression is usually false. In fact, the circuits implemented with a two-phase protocol are faster than their four-phase counterpart [15]. On the other hand, designing edge sensitive circuitry (needed for the two-phase protocol implementation) is more complex, leading to larger circuits that consume more power [15]. Therefore, a two-phase protocol is preferred for designing fast circuits, in which the performance is a critical issue. Conversely, the four-phase protocol is widely used if the designer has some freedom degree to balance the latency components in order to enhance the circuit performance [15, 125].

3.4.3 The Muller gate

To implement the communication protocols of asynchronous circuits, basic logic gates are not sufficient. A different gate, capable of properly synchronizing the various protocol signals, is then required. Moreover, designing asynchronous architectures require special circuitry other than conventional logic gates and flip-flops, e.g. fork, join and merge circuits, and metastability filters. Implementing such circuitry with conventional gates is possible but is an inefficient solution.

In this context, the logic gate proposed by David Eugene Muller, known as Muller gate or C-element [103], has the appropriate behavior to address all these issues. The symbolic representation and the truth table of a 2 input symmetric C-element is shown in Fig. 3.8. If both inputs (A and B) are equal, the output (Z) is equal to the inputs. On the other hand, if A and B are different, Z keeps its last value. In other words, the output of a C-element copies the value of its inputs when they are identical, otherwise it memorizes its previous state. The peculiar behavior of the C-element has made it an essential building block for asynchronous circuit design [138].

Other architectures of C-elements have been also proposed. For instance, the generalized C-element, also known as asymmetric C-element, has been proposed in [88]. In such gate, the inputs that need to be equal to 1 to change the output to 1 is different than the inputs that need to be equal to 0 to change the output to 0. Despite the behavioral differences with the conventional C-element, the asymmetric and all the other different types of C-elements are also considered to be a state retention device.



A	B	z
0	0	0
0	1	z^{-1}
1	0	z^{-1}
1	1	1

(a) (b)

Fig. 3.8: 2 input symmetric C-element symbol (a) and truth table (b).

3.5 Classification of asynchronous circuits

The characterization of asynchronous systems is not limited to the choice of communication protocol to be implemented. Depending on the signaling and data encoding conventions, the asynchronous circuits are classified in different classes [71]. Fig. 3.9 shows the classification of asynchronous circuits in the classes most cited in the literature: Delay insensitive (DI); Quasi-delay-insensitive (QDI); Speed Independent (SI); and Micropipeline. Synchronous circuits are also shown in the graph for the sake of comparison.

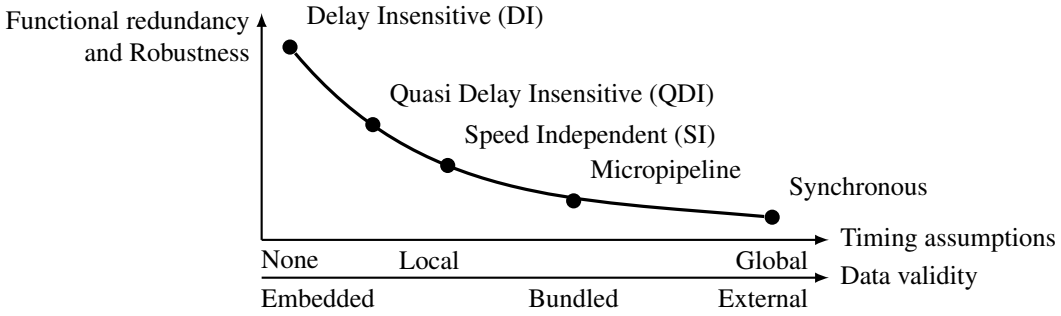


Fig. 3.9: Classification of asynchronous circuits in terms of functional redundancy and robustness. The graph shows how data validity and timing assumptions vary from class to class. Adapted from [71].

The communication protocol and data encoding conventions, that are specific of each class, impose some requirements such as no hazard or local timing assumptions [138]. The global assumptions impose more circuit restrictions to guarantee a correct behavior than the local assumptions. Thus, the architectures operating under global timing assumptions are less robust than a circuit class operating with local assumptions. In other words, the class of circuits that have global timing assumptions are more susceptible to failure due to environmental events such as aging, temperature and voltage variations.

The price to pay for robustness is functional redundancy. To ensure a correct operation under environmental events, larger architectures, with special circuitry such as metastability filters and completion detection elements need to be designed. The result is that local timing assumptions generally require bigger circuits and global assumption generally implies smaller circuits [15, 138]. For instance, a QDI asynchronous circuit has almost no timing assumptions, which makes it more robust but larger than its synchronous counterpart [15, 138].

The data validity axis of Fig. 3.9 classifies each asynchronous circuit class based on the data

signaling convention (embedded, bundled and external data validity), as explained in section 3.3. More details on each class are given in the following subsections.

3.5.1 Micropipeline

The concept of micropipeline circuits was introduced in 1989 by Ivan Sutherland [141]. This is the class of asynchronous circuits that has more similarities with the synchronous circuits, as depicted in Fig. 3.10. Compared to its synchronous equivalent (Fig. 3.1), the datapath is kept identical and the global clock is replaced by asynchronous controllers that interact with each other thanks to request and acknowledgement signals. Thus a bundled-data encoding is used in micropipeline circuits.

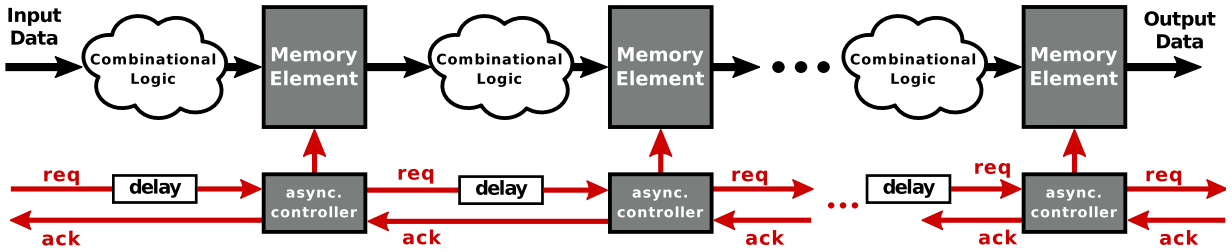


Fig. 3.10: Abstraction of a micropipeline asynchronous system.

The data propagation throughout the system depends on the state of each stages (occupied or free). Thus, the data propagates in the micropipeline as long as they do not encounter occupied memory elements [15, 138]. Delay lines need to be inserted in the req signals between blocks, as depicted in Fig. 3.10, in order to avoid that the output request signal from one asynchronous controller arrives to the following memory block before the corresponding combinational logic block has finished its calculation. Hence, the speed of data propagation throughout the system is bounded by the local critical path delay of the combinational logic between memory elements.

3.5.2 Speed Independent

The Speed Independent (SI) circuits were initially described by [100]. In this class of asynchronous circuits, the delay in logical gates are arbitrary while all the interconnect delay are considered to be negligible [100]. Unfortunately, in recent CMOS manufacturing technologies, the interconnect delay is becoming increasingly critical. Thus, a model that neglects the delays in the wires is no longer desirable.

3.5.3 Delay Insensitive

The delay insensitive circuits (DI) [30,152] do not impose any timing restriction neither on logic gate delays nor on wire delays. Thus, the DI circuits behave according to their specification regardless of the delays of logic gates and interconnects. The only requirement for correct operation is respecting the chosen communication protocol. This is the most robust class of asynchronous circuits, as depicted in Fig. 3.9. Unfortunately, it is not always possible to design DI circuits. The robustness required by this class impose the use of only inverters and C-elements as building blocks to design asynchronous DI architectures. With only these logic gates available, the set of achievable circuits is very limited [90].

3.5.4 Quasi Delay Insensitive

The Quasi Delay Insensitive (QDI) class is a subset of the SI class in which the notion of isochronic fork has been inserted [86, 89]. The definition of fork is a wire that connects a single sender block to at least two receivers. The fork is considered to be isochronic if the delays between the sender and all the receivers are identical (or very close to identical). In [89], Alain Martin has shown that the timing assumption of the isochronic fork is the weakest constraint to be added to DI circuits in order to make them feasible with single output gates. Complex QDI asynchronous circuits are therefore feasible by using standard cells of synchronous circuits, which increases the attractiveness of this class of asynchronous circuits for industrial applications [44].

In QDI circuits, data propagates through logic gates and wires with arbitrary delays with no risk for the system correct behavior. This makes them extremely robust to temperature, aging, process and supply voltage variations [91]. Both two-phase and four-phase protocols are feasible, but implementing architectures with such robustness require delay insensitive encoding. The reduced number of timing assumptions makes QDI asynchronous circuits very well-suited for low-power operation and on-the-fly V_{th} tuning, subject that will be explored in details in the following chapters of this thesis.

3.6 The advantages of asynchronous circuits

The absence of a clock signal results in a functional behavior of asynchronous circuits that is comparable to a synchronous circuit with a local clock for each block of the asynchronous circuit. The period of these local clocks are determined by the block latency and they are not in phase with each other. Moreover, a fine-grain clock gating mechanisms is an intrinsic property of asynchronous circuits: memory elements are only clocked when needed [138]. The result of such intrinsic properties of asynchronous circuits are the benefits listed below.

3.6.1 High performance

The processing delay in asynchronous circuits is bounded and varies with the variation of the inputs. Indeed, different inputs may activate distinct paths of the system, which cause the input to output latency to change. The end of a calculation is locally detected by a certain block of the circuit, and data propagates to the following blocks of the system as soon as the previous block is done calculating. Therefore, the circuit operating speed is determined by averaging the local latencies rather than the global worst-case latency [92, 162].

3.6.2 Low power consumption

In the absence of a global clock signal, all the power consumed by the clock tree circuitry is then eliminated. Additionally, the event-driven nature of asynchronous logic automatically set the inactive block to standby mode. Only the blocks of the system that have data to process will be activated, thus the total dynamic power consumption of the system is reduced if compared to its synchronous counterpart [18, 50].

Moreover, using voltage scaling schemes to further reduce the power consumption is easily implementable in asynchronous systems. Lowering V_{dd} is a well-know technique for reducing the dynamic power consumption at the cost of a reduced performance. Implementing voltage

scaling in synchronous circuits requires adjusting the clock frequency accordingly to avoid timing violations, which increases the design complexity. In asynchronous circuits, on the other hand, this scheme is easily implemented since varying the voltage just changes the blocks propagation delays but does not affect the correctness of the operations. The use of asynchronous circuit at low V_{dd} for low power applications is the focus of this thesis. Their behavior under such conditions will be analyzed in details in the following chapters.

3.6.3 Modularity

The block-to-block communication protocol implemented in asynchronous circuits and thus locality of synchronizations increases the modularity in asynchronous systems. Indeed, complex systems can be build by connecting pre-existing asynchronous blocks in a plug and play manner [88, 141]. Moreover, the local nature of synchronization in asynchronous systems enables data activity sensing in a rather fine granularity by using only the request and acknowledgment signals [147]. The impact of local activity detection will be analyzed in details in chapter 5.

3.6.4 Low electromagnetic emissions

The communication protocol signals (request and acknowledgement) that control data propagation in asynchronous systems can be seen as local clocks. They can occur at any moment in time, solely depending on the latency of the successor and the predecessor blocks and the availability of new data to be processed. Therefore, these local clocks tend to be randomized over time, which results in supply current curves [138], without the large di/dt spikes of synchronous circuits. Consequently, the asynchronous circuits emit less electro-magnetic noise [19, 115].

3.7 Conclusion

In this chapter, an alternative solution to the conventional synchronous design approach has been presented: the asynchronous circuits. In this case, the global timing synchronization performed by the clock signal is replaced by a local synchronization mechanism, implemented through a bidirectional signaling that guarantees an event-driven processing of data. Following the analysis of asynchronous principles, the most used communication protocols and data encoding have been presented. Subsequently, the asynchronous circuits have been classified in terms of robustness and timing assumptions, the convention mostly used by the scientific literature. At the end of this chapter, the advantages of asynchronous circuits have been highlighted.

Despite all the presented benefits and potential gains of removing the global clock, the increased design complexity of asynchronous systems limits the industry from widely adopting this promising solution. However, the event-driven intrinsic operation of asynchronous circuits and the facility to implement power management schemes have impulsed the used of such circuits for applications with critical energy efficiency and robustness. This type of application is the focus of this thesis, and will be analyzed in detail in chapters 4, 5 and 6.

Chapter 4

Comparing Voltage Scaling in Synchronous and Asynchronous FD-SOI Circuits

Among state-of-the-art power management techniques, reducing the operation voltage (V_{dd}) of circuits is a traditional method to decrease power consumption. However, low V_{dd} makes circuits more vulnerable to process, voltage, and temperature (PVT) variations [171], causing timing uncertainties leading to clock assumption violations in synchronous circuits.

In this context, asynchronous circuits appear as an alternative solution for addressing power consumption issues and ensuring high system reliability at lower V_{dd} levels. As their own data flow is used to locally synchronize information between parts of the system, delay variations are much more tolerable. Thus, asynchronous circuits are intrinsically more robust to PVT variations, especially the quasi-delay insensitive (QDI) class that enables operation at very low V_{dd} [126].

The data driven processing between asynchronous blocks makes the system more modular, and the inclusion of local voltage scaling techniques is much easier. In addition, extended low-power features are exploitable from the recent Fully-Depleted Silicon On Insulator (FD-SOI) process. Thanks to a more efficient control of the body biasing effects on the transistor channel [17], the FD-SOI technology provides the option of setting different threshold voltages (Vth) even during system operation. Therefore, local synchronization signals can be used to control biasing of asynchronous block substrates, which enables power reductions or speed improvements [56].

The power consumption reduction strategy on QDI asynchronous circuits with body biasing features in FD-SOI technology has been analyzed in [56]. The same strategy, however, was neither studied at low operation voltages nor compared with their synchronous equivalent. The work in [25] compares an asynchronous architecture to its synchronous counterpart, but in a classical CMOS 130 nm technology, in which body biasing effects are not efficiently controllable. In order to apply voltage scaling techniques to decrease V_{dd} of integrated systems and to profit the full low-power potential of the FD-SOI body biasing features, additional work to [40, 85] is still required, especially to define and compare the minimum operation voltages in synchronous and asynchronous FD-SOI case-study circuits. In this chapter, we present a comparison of an asynchronous arithmetic logic unit (ALU) with its synchronous version, both designed in FD-SOI 28 nm. The results in terms of data throughput, power consumption and energy per bit are analyzed at different V_{dd} levels. The work of this chapter was presented in the

international conference PATMOS 2016.

The following sections of this chapter is organized as follows: section 4.1 discusses how QDI features are exploitable for saving power; section 4.2 describes the case-study circuits analyzed in this work; and in sections 4.3 and 4.4 comparative results and final conclusions are highlighted.

4.1 Exploiting intrinsic features of QDI asynchronous circuits for saving power

Asynchronous circuits, particularly QDI circuits, are well suited for operating in a wide V_{dd} range. As detailed in chapter 3, the intrinsic data-driven operation characteristic indeed enables correct behavior under several voltage levels, with no need for extra circuitry or additional precautions, even in the scenario of dynamically modifying V_{dd} during the circuit operation. Extremely low V_{dd} is also tolerated, not requiring architectural changes, as discussed in [126].

Traditional power saving strategy for integrated systems simply applies lower operation voltages rather than the nominal one. For the FD-SOI technology, low voltage operation was demonstrated in [40, 85] for saving power. Low voltages, on the other hand, increase the delay of system components, making timing violations more probable in clock-based circuits.

QDI asynchronous circuits present three intrinsic features that allow low operation voltages and the power management of integrated systems:

1. the absence of a clock eliminates several related timing assumptions
2. the tolerance to any delay variation on their gates and on majority of their wires
3. the modularity by using data-based request and acknowledgement signals between blocks.

Hence, at the expense of a delay increase on their gates, QDI circuits are able to operate with low voltages for saving power. Furthermore, the biasing advantages of FD-SOI technology associated with the previously mentioned properties of QDI circuits is also exploited to speed up components operating at low voltages, thus increasing the energy per operation ratio, as is analyzed in details in chapter 5.

4.2 Target Case-Study Circuits: Synchronous and Asynchronous ALU

As previously mentioned in the introduction of this chapter, an 8-bit ALU was used in this work as a case-study. This circuit has been specifically chosen since it is one of the most important blocks in modern processors. The designed architecture can compute either addition, subtraction, or bitwise logic operations. Fig. 4.1 depicts the proposed ALU architecture. It is composed of three stages of pipeline. The first one is the input stage, with de-multiplexers for selecting between either arithmetic or logic operations; the second stage is the execution stage, in which the logic and arithmetic units compute their corresponding output; and the third stage of pipeline is the output selection stage. Both synchronous and asynchronous circuits were equally pipelined and have logic blocks with the same functionality. Thus, both circuits are composed of:

- One 8-bit Sklansky Adder, which computes the operations of addition and subtraction;
- One 8-bit Logic Unit for computing AND, OR and XOR logic operations;
- Several multiplexers and de-multiplexers necessary to correctly select the required operations.

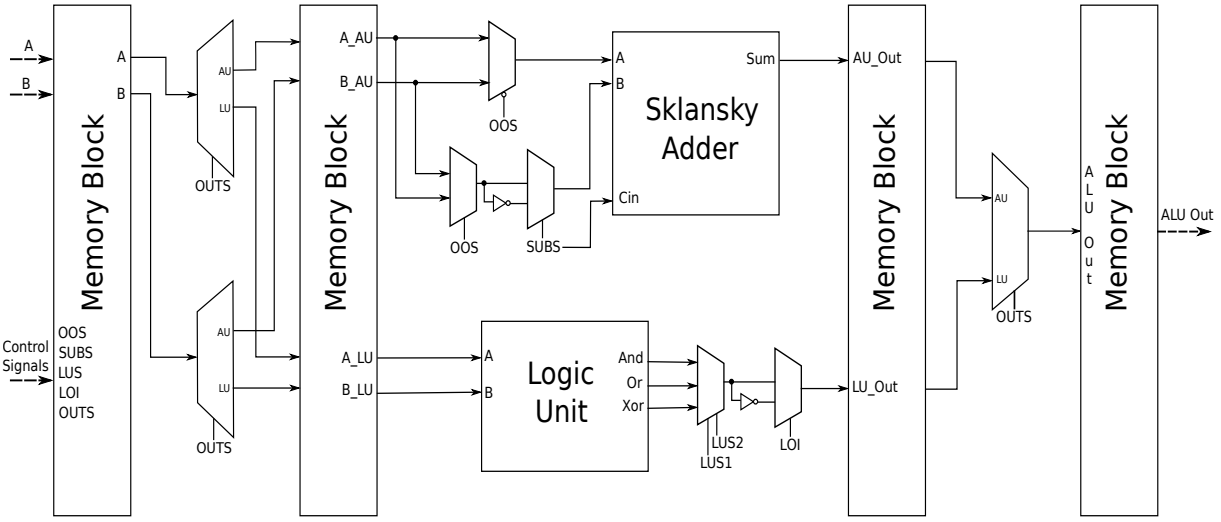


Fig. 4.1: ALU general architecture, designed in synchronous and asynchronous versions.

The difference between the synchronous and asynchronous implementation of the proposed architecture is that the former has registers as memory blocks and is entirely composed of standard cells. The latter, on the other hand, has half-buffers as memory blocks, which memorize data between pipeline stages and implement a 4-phase Weak-Conditioned Half-Buffer (WCHB) communication protocol [80]. The asynchronous logic blocks of Fig. 4.1 were designed by using the Delay Insensitive Min-terms Synthesis (DIMS) technique [138]. This design method allows generating QDI basic logic gates by only using conventional OR gates and C-elements (the special cell described in chapter 3). Complex QDI systems are then achieved by combining these basic QDI logic gates in exact same way as when designing combinational circuits for a synchronous system [138]. The systems design with DIMS are very robust, thus they are suitable for low V_{dd} operation.

The synchronous ALU has been described in VHDL, at a structural level, with the same blocks used in the asynchronous circuit. The hardware description was then synthesized for a target voltage of 1 V. Subsequently, the generated verilog gate level netlist was converted to a SPICE netlist, so that electrical simulations could be performed. On the other hand, for the asynchronous design, the same blocks previously described were directly designed at Spice level, using a QDI dual-rail 4 phase asynchronous encoding. Details on the simulation environment will be given in section 4.3.

It is widely known that QDI designs present a considerable area overhead if compared to a synchronous equivalent, as reported by [25]. In fact, to cope with the extra robustness, the asynchronous ALU present a significant area overhead compared to the synchronous circuit. In this study-case, the functional blocks of the asynchronous circuit are 1.8x to 2.5x larger than the synchronous functional blocks, which leads to a total of approximately 2.3x area overhead of the asynchronous ALU.

4.3 Comparison of Synchronous and Asynchronous ALU Results

4.3.1 Simulation Environment

The synchronous and asynchronous ALU spice netlists, obtained as detailed in section 4.2, were simulated with Regular Threshold Voltage (RVT) transistors of FD-SOI 28nm technology. Each netlist was connected to a Linear Feedback Shift Register (LFSR) so that it could generate the input vectors. Afterwards, electrical simulations were performed with the circuit, ALU and LFSR, for a fixed amount of time with different levels of V_{dd}, ranging from nominal 1.0 V down to 0.4 V. This procedure was the same for both circuits, synchronous and asynchronous. Some precautions needed to be taken into account in simulations with the synchronous design though. For each simulation scenario, it was necessary to adjust the clock frequency to prevent timing violations. Moreover, to allow a fair comparison with the asynchronous counterpart, the clock frequency was adjusted to the fastest possible for each V_{dd}, ensuring maximum performance of the synchronous ALU through all simulations. A script was used to automatically tune the clock frequency for each simulation.

With the asynchronous design, however, no special adjustment needed to be done to ensure correct behavior and maximum performance at each V_{dd}. In fact, as previously mentioned in section 4.1, QDI circuits are intrinsically robust to voltage variations. Furthermore, the local handshake protocol, used by the asynchronous counterpart, ensures that it will always operate at its maximum speed. Fig. 4.4 depicts the results of energy per bit for synchronous and asynchronous designs. A lower value of energy per bit represents a better efficiency.

4.3.2 Results

After performing the simulations described in subsection 4.3.1, results in terms of power consumption, data throughput and energy efficiency were obtained. Fig. 4.2 shows the average power consumption of the synchronous and asynchronous designs, for different V_{dd} levels under three corner conditions: typical-typical (TT), fast-fast (FF) and slow-slow (SS). Fig. 4.3 illustrates the measured throughput of both circuits at the same V_{dd} levels. The throughput has been chosen as figure of merit for performance comparison between the designs since it can be easily measured in both synchronous and asynchronous designs. Notice that the throughput of the synchronous circuit is directly determined by the clock frequency. Hence the importance of implementing a clock frequency scaling mechanism, as described in section 4.3.1.

The figures illustrate the trade-off between power and performance in FD-SOI technology. Comparing Fig. 4.2 and 4.3, it can be noticed that the throughput is reduced when V_{dd} is decreased. For instance, when V_{dd} is decreased from 1 V to 0.8 V, there is a reduction of approximately 30% and 44% in the synchronous and asynchronous architectures performance, respectively.

In Fig. 4.2 it can be seen that the asynchronous ALU has a lower average power consumption, if compared to the synchronous one, in every simulated operation voltage. For instance, if operating at V_{dd} = 0.4 V, the TT asynchronous ALU consumes approximately 86% less power than its synchronous counterpart. This result can be explained by the intrinsic QDI asynchronous properties, which ensures switching activity only in blocks that are processing some data. In synchronous designs, however, inadvertent transistors also switch, which increases the dynamic power consumption. Additionally, the curves of SS and FF synchronous corners are

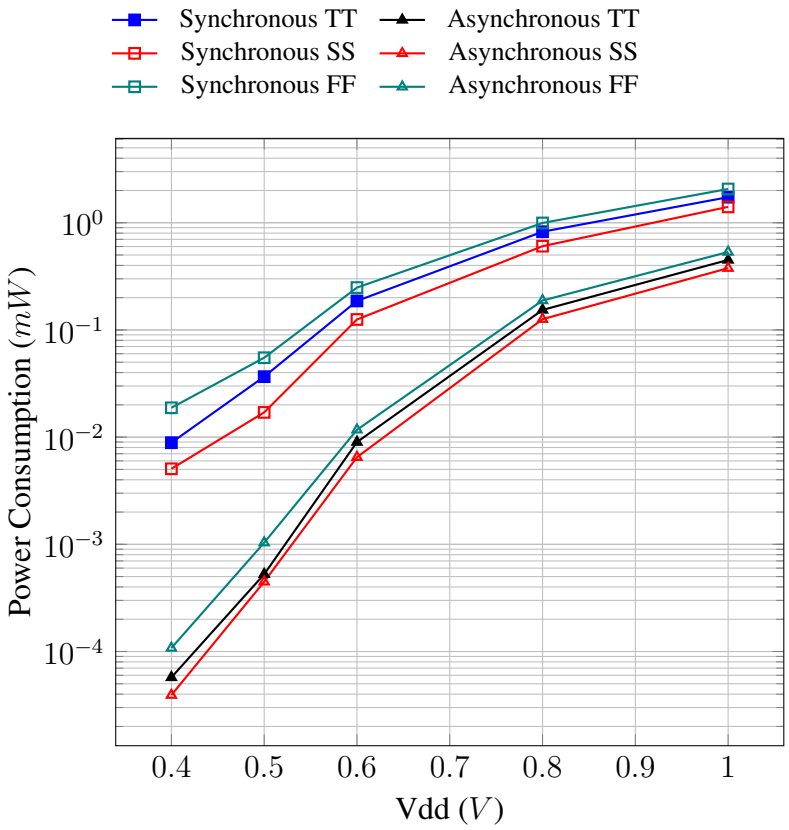


Fig. 4.2: Average power consumption of synchronous and asynchronous ALU in different V_{dd} conditions and corners typical-typical (TT), slow-slow (SS), and fast-fast (FF).

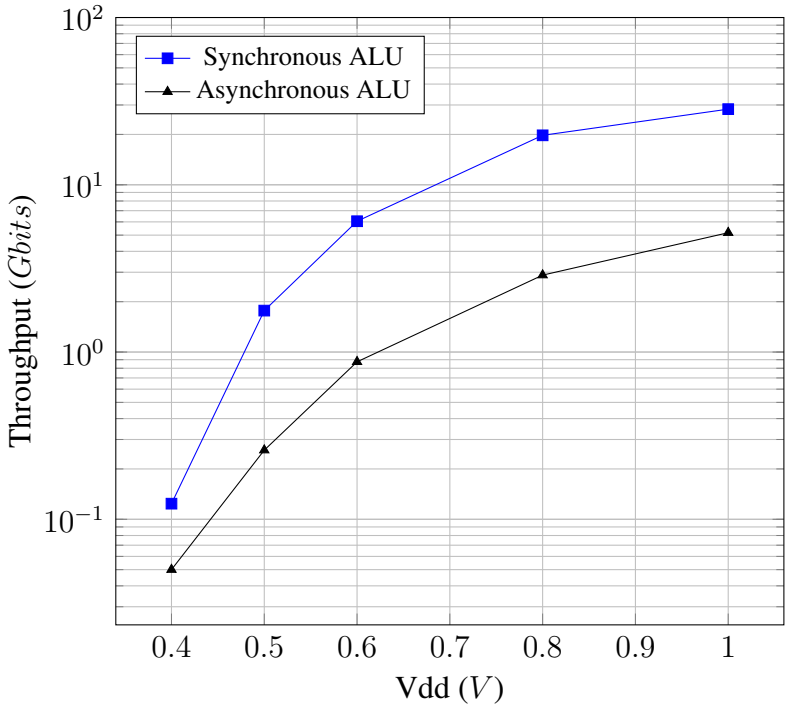


Fig. 4.3: Data throughput of synchronous and asynchronous ALU in different V_{dd} conditions.

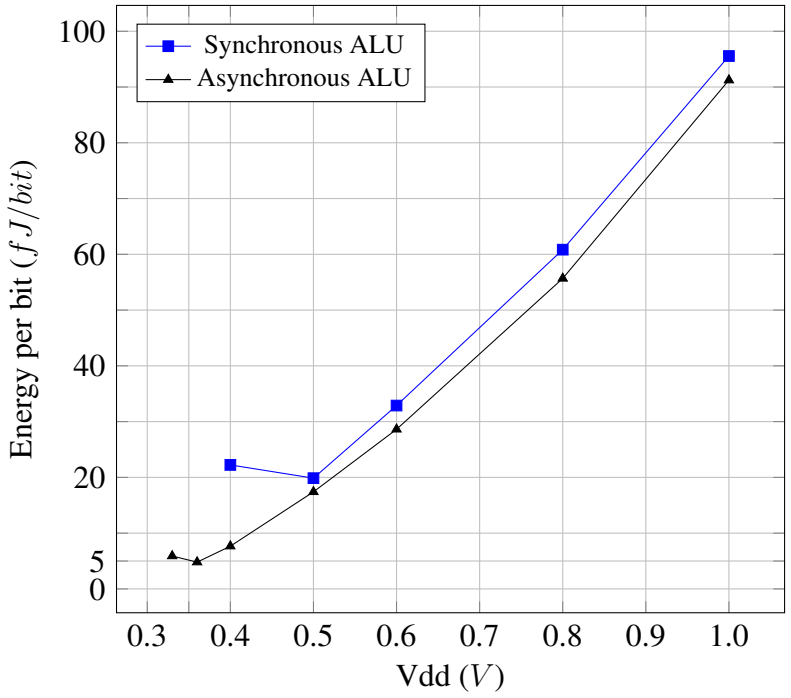


Fig. 4.4: Energy per bit of the synchronous and asynchronous ALU in different V_{dd} conditions.

more widely spaced than asynchronous ones, indicating that the synchronous circuit is more sensitive to process variations. Comparing both architecture operating at V_{dd} = 1.0 V, the synchronous circuit power consumption varies approximately 10% more with the process variation than the asynchronous counterpart.

On the contrary, Fig. 4.3 shows that the performance of the synchronous ALU is better for values close to the nominal voltage, but it gets closer to asynchronous performance if V_{dd} decreases. Also, the synchronous circuit performance is more sensitive to V_{dd} changes if compared to its asynchronous counterpart, since it has a steeper slope in the throughput curve of Fig. 4.3. For instance, decreasing V_{dd} from 0.5 to 0.4 V cause a reduction of approximately 80% in the asynchronous circuit performance, which is 13% less than the performance degradation that occurs in the synchronous counterpart considering the same V_{dd} interval.

Finally, if energy efficiency is analyzed, as depicted in Fig. 4.4, the energy per bit ratio is lower in the asynchronous circuit for all simulated V_{dd} scenarios. In the case of operation voltage bellow 0.5 V, the throughput degradation becomes quite severe in the synchronous design. Its energy per bit ratio thus starts growing, indicating that the throughput degradation overcomes the power consumption reduction trade-off. Therefore, the minimum energy operating point (MEOP) is achieved with the synchronous circuit operating at 0.5 V, in which the energy consumption per bit is approximately 20 fJ/bit. The MEOP of the asynchronous ALU is achieved at 0.36 V, in which the energy per bit is approximately 5 fJ/bit, 75% less than the synchronous counterpart. The main reason for that, is the enormous amount of timing margin that has to be added to the clock at very low V_{dd}, which makes the circuit leaks power for a much longer interval of time. The same behavior is not observed in the asynchronous counterpart for V_{dd} equals to 0.4 V. Hence, for V_{dd} levels lower than 0.5 V, the usage of the QDI asynchronous ALU instead of classical synchronous architecture is very well-suited for applications requiring high energy efficiency.

4.4 Conclusions

This chapter compares a synchronous and an asynchronous ALU circuits in FD-SOI 28 nm. The goal was to analyze the behavior of these circuits at very low operation voltages. Thanks to the natural asynchronous properties, the asynchronous ALU presents a better energy efficiency in all simulated Vdd conditions. Furthermore, at V_{dd} lower than 0.5 V, the asynchronous architecture becomes predominantly much more power efficient. Although QDI asynchronous design leads to almost the double of area than its synchronous counterpart, it has been noticed that it is very robust, and thus suitable for applications requiring high reliability and security. The synchronous design, otherwise, must be adapted by receiving extra circuitry that may make it more robust. The results shown in this chapter allows to define new voltage scaling strategies in FD-SOI 28 nm, and in addition thanks to the body biasing features of this technology, more power savings can be envisioned.

Chapter 5

Assessing Adaptive Body Biasing Strategies in Asynchronous Circuits

Power consumption is nowadays one of the main concerns for nano-electronic systems [158]. The increasing popularity of Internet of Things demands CMOS devices able to adapt their energetic behavior to the environmental requests by exploiting several power modes such as low-power, low-leakage or high-performance modes. In this context, supply voltage scaling and body biasing (BB) are well-known effective techniques to address this issue [26, 98]. Voltage scaling consists in reducing the supply voltage (V_{dd}), thus quadratically decreasing dynamic consumption and consequently increasing gate delay. Therefore a permanent trade-off has to be managed between power and performance. Another way of diminishing power consumption is applying BB, which artificially changes the transistors threshold voltage (V_{th}). Two configurations can be applied, as described in chapter 2. The first one increases V_{th} thus decreasing the leakage and the performance. This technique is denominated Reverse Body Biasing (RBB). The second, known as Forward Body Biasing (FBB), decreases V_{th} for improving the performance of transistors at the price of higher leakage consumption. The attractiveness of BB has been enhanced in the Fully Depleted Silicon on Insulator (FD-SOI) technology. A wide range of body bias voltages (V_{bb}) is available in FD-SOI thanks to a layer of insulator, inserted between body and channel, allowing fine V_{th} tuning [109, 117], as discussed in chapter 2.

Over the last few years, various techniques have been devised to enhance BB effectiveness, especially by splitting the target system into body biasing domains (BBD) [51, 74, 77]. Each BBD is set to an independent V_{bb} at runtime, which adds flexibility to address variability issues or enhance the power-performance tuning. To implement such schemes, special cells are required to control the V_{bb} of each BBD, commonly known as body bias generators (BBG), capable of changing the biasing voltage of the n-well and p-well during circuit operation.

For biasing large BBDs, with a size comparable to IPs such as processors, the proposed body bias generators use digital-to-analog converters and/or charge pumps to generate V_{bb} with a fine resolution [21, 66, 95, 99]. Although this is a good solution for charging systems split into large BBDs, the complexity and high area overhead of such body bias generators make them inappropriate for smaller BBDs. Therefore, when dealing with tiny BBDs, a different strategy is adopted to limit the complexity and area overhead. V_{th} hopping is commonly used [56, 109, 165], since it is simply implementable with level shifters. The idea of this type of adaptive body biasing (ABB) scheme is decreasing V_{th} during active periods of the circuit, in order to guarantee performance, and increase it during idle periods, thus preventing unnecessary leakage consumption. In this case the required body bias generators is a simple level shifter that

adjusts V_{bb} for high performance or low leakage mode, depending on the circuit activity. Such approach is presented and analyzed in this chapter.

Asynchronous circuits are the perfect candidate for implementing the aforementioned technique. As the local handshake signals control data propagation through the system [138], they are perfectly suitable to indicate if a BBD is active or idle. Moreover, the intrinsic robustness properties of asynchronous circuits make them more favorable for on-the-fly V_{th} changes than their synchronous counterparts, thus avoiding timing violations when transitioning from high to low performance mode. Body biasing strategies using asynchronous circuits have been previously investigated by Hamon et al. [56]. Authors presented the benefits of adaptive body biasing in asynchronous circuits for high performance applications with a fine grain BBD partition strategy. However, their study was not focused on the BBD partitioning, which is a parameter that along with circuit's activity rate directly impact the performance and energy efficiency of a system.

This chapter proposes assessing three different BBD partitioning strategies for implementing adaptive body biasing schemes in asynchronous circuits: one coarse-grain, one fine-grain and one medium-grain. A case-study circuit based on ALUs is chosen as base system for evaluating performance and energy efficiency of the three proposed body biasing strategies. In order to evaluate the optimal use case for each strategy, a methodology for analyzing energy efficiency of adaptive body biasing strategies in asynchronous circuits is also proposed. The work of this chapter was submitted for publication in the Microprocessors and Microsystems journal 2018.

The following sections of this chapter are organized as follows: section 1 presents how to build different ABB schemes by exploiting asynchronous features and BBD partitioning. The following section proposes a methodology for analyzing the energy efficiency of adaptive body biasing strategies implemented in asynchronous circuits. Finally, sections 3 and 4, respectively, analyzes simulation results for a case-study in FD-SOI 28 nm technology and concludes this chapter.

5.1 Body biasing strategies for asynchronous circuits

5.1.1 Implementing ABB schemes

The attractiveness of implementing RBB and FBB schemes is increased by applying an ABB scheme. The V_{th} is decreased during active periods, to enhance circuit's performance, and increased during idle periods to prevent unnecessary leakage. This thesis is focused on applying ABB in sub-circuits of an integrated system, therefore, the complexity and area overhead of BBGs need to be minimized. Thus, a strategy based on V_{th} hopping [110, 165] is used. The idea is to reduce the resolution of V_{bb} by setting only two possibilities: one voltage level for decreasing V_{th} and another one for increasing it, a strategy easily implemented with level shifters.

Fig. 5.1 depicts an abstraction of the ABB strategy used. The level shifter block controls the tuning of the transistors V_{th} depending on the target system's activity. Whenever the activity signal is 1, indicating that the target system is active, the body of the transistors will be set to V_{act_n} and V_{act_p}, voltage levels that decrease V_{th}, thus increasing the performance. Conversely, if the activity signal is 0, which indicates that the target system is idle, the body of transistors are biased to V_{idle_n} and V_{idle_p}, a configuration that increases V_{th}, consequently decreasing the leakage.

The body biasing strategy shown in Fig. 5.1 applies to both RBB and FBB schemes. In fact, what differentiates these strategies is the choice of voltage levels of V_{idle_n}, V_{idle_p}, V_{act_n}

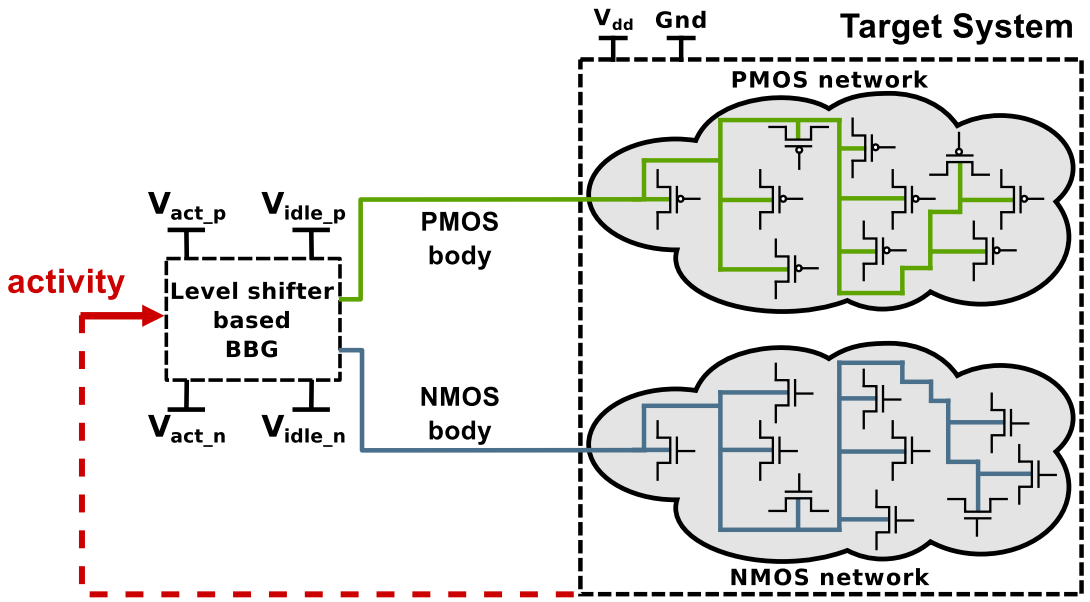


Fig. 5.1: Abstraction of a level-shifter based BBG controlling the V_{th} tuning of a generic target system. The activity signal indicates if the Target System is active or idle. The former is indicated by a logic value 1, which sets PMOS and NMOS body outputs V_{act_p} and V_{act_n} respectively. If the Target system is idle, the activity signal is 0, which sets PMOS and NMOS body outputs V_{idle_p} and V_{idle_n} respectively.

and V_{act_p}. For instance, in order to implement FBB $V_{idle\_n} = 0$; $V_{idle\_p} = 0$; $V_{act\_n} > 0$; and $V_{act\_p} < 0$. The experiments described in the rest of this chapter were performed with FBB. The procedure to perform simulations with a RBB scheme is analogous to what is described in the following sections. In this chapter, the level-shifter based BBG will be treated as a black box. Its architecture and detailed behavior are analyzed in depth in chapter 6.

5.1.2 ABB schemes for QDI asynchronous circuits

Implementing an effective ABB scheme requires changing the V_{bb} of the circuit during its operation. For instance, implementing an FBB approach requires biasing the circuit as soon as data is available for processing, and turning off the biasing as soon as the circuit becomes idle. Changing the operation mode to high performance requires charging the body capacitance (C_b), which requires an energy consumption (E_{Cb}) of:

$$E_{Cb} = C_b V_{bb}^2 \tag{5.1}$$

The extra energy cost E_{Cb} has to be compensated with energy savings during a sufficiently long idle period. Therefore, precisely sensing the circuit activity is crucial for switching from high performance to low leakage mode as soon as possible, thus increasing the energy savings and the attractiveness of adaptive body biasing schemes.

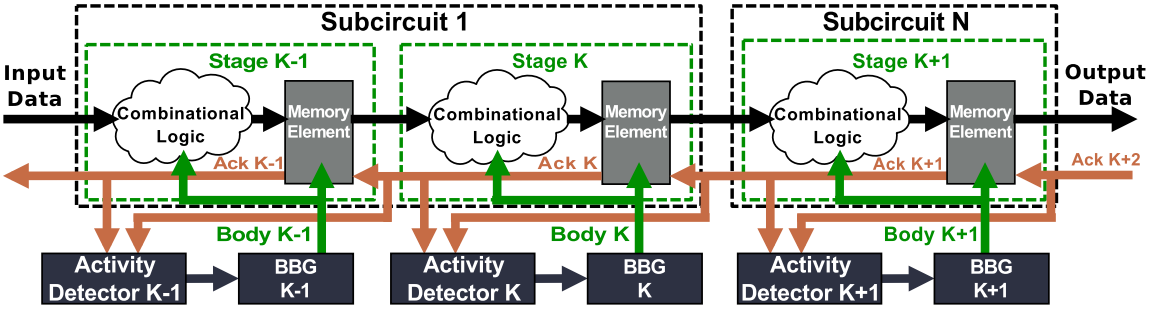
In QDI asynchronous architectures, as previously discussed in chapter 3, the acknowledgement signals can be directly used for generating the activity signal of Fig. 5.1. Logically processing a combination of consecutive acknowledgements allow controlling body-biasing activation. Fig. 5.2 shows the logic blocks responsible for detecting activity of QDI asynchronous

circuits for different granularity levels, called activity detectors. The differences between the strategies depicted in Fig. 5.2 will be detailed in the following subsection.

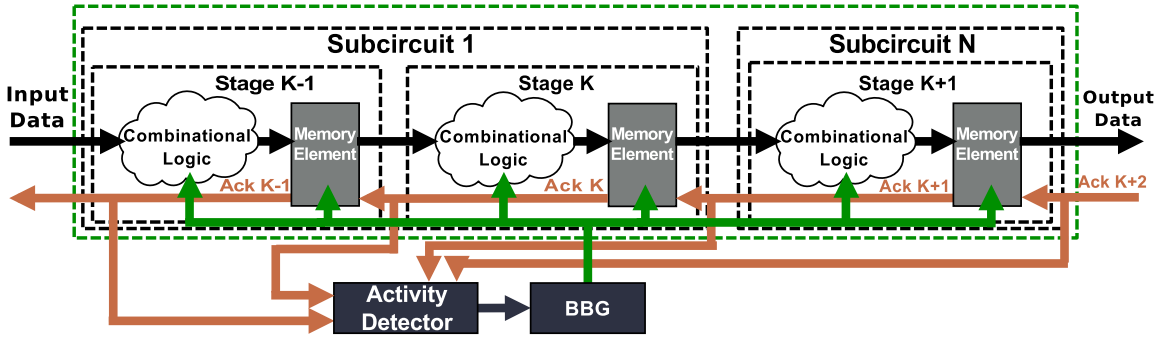
Once the activity signals have been generated by activity detectors, the level shifter based BBGs in Fig. 5.2 drive V_{bb} to the back plane of PMOS and NMOS transistors necessary to set a FBB or a noBB scheme, as described in section 5.1.1.

5.1.3 BBD granularity

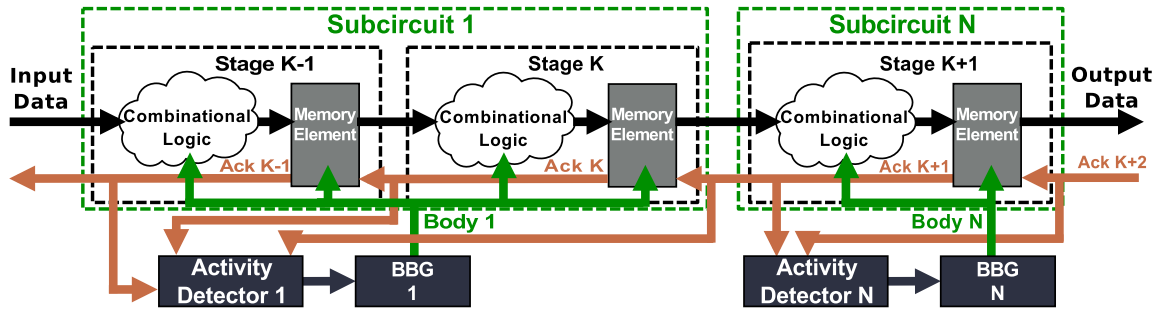
In this work, each BBD is a sub-circuit of the Target System. It is composed of a single activity detector that control the activation of a level shifter based BBG independently of the other BBDs. For the asynchronous circuits, the discussion of BBD granularity is closely related to the way the system is pipelined. In fact, exploiting the locality of communication protocol



(a)



(b)



(c)

Fig. 5.2: Abstraction of adaptive body biasing strategies at fine (a), coarse (b), and medium (c) grain. The green dashed squares represent the BBDs of each strategy.

signals to indicate circuit activity limits the minimum size of BBD to a pipeline level. Smaller BBDs would be possible by redesigning the system with more pipeline stages. A high level abstraction of such fine body biasing strategy is depicted in Fig. 5.2a. In this case, each pipeline stage belongs to a separate BBD. The acknowledgement signals of input and output memory blocks are used to indicate activity. For instance, if the logic value of Ack_{K-1} is different than Ack_K, new data has been stored in the memory block of stage K-1, thus it will be processed by stage K. At this moment, body biasing should be turned on. Conversely, if Ack_{K-1}, Ack_K and Ack_{K+1} have the same logic value, there is no data to be processed by stage K, then body bias can be turned off. Several activity detection approaches for asynchronous circuits have been proposed for fine granularities [56, 62]. In this work, it is implemented by a single 3-input NAND gate.

An alternative body biasing strategy, the coarser possibility for an asynchronous circuit, is a system-level approach, as depicted in Fig. 5.2b. In this case, all pipeline stages are grouped in the same BBD. Hence, the activity detector is a circuit that checks the pipeline emptiness. It signalizes activity if at least one stage is processing data (at least 2 Ack signals different from each other). Conversely, body biasing is turned off if the pipeline is completely empty: all acknowledgements have the same logic value.

Yet another body biasing strategy, intermediate to the already presented ones, is shown in Fig. 5.2c. Here each BBD is a sub-circuit of the target circuit composed of one or more pipeline stages. The activity detection proposed in this case is a simplified version of the emptiness detector of the system-level approach.

5.2 Energy efficiency of ABB strategies with asynchronous circuits

There will be advantages on applying one of the body biasing strategies discussed in section 5.1.3 if the energy they consume (E_{ABB}) is smaller than the energy consumption of an always biased counterpart (E_{alwaysBB}), a system that is always connected to de the same V_{bb} potentials, independently of the circuit activity. In eq. (5.2), E_{ABB} represent any of the strategies discussed in section 5.1.3. Changing from low to high performance modes leads to energy overheads (E_{Cb}), as described in section 5.1.2. Therefore, satisfying eq. (5.2) requires energy saving during idle periods to be greater than E_{Cb}.

$$E_{\text{ABB}} < E_{\text{alwaysBB}} \tag{5.2}$$

5.2.1 Analyzing a coarse-grain strategy

Fig. 5.3b shows the activation and deactivation of body biasing when input vectors are processed by a system with a single BBD (body biasing strategy depicted in Fig. 5.2b. The system is active during the period Δt_{BB} and idle during Δt_{noBB}. As shown by the green curve in Fig. 5.3b, the complete circuit is biased at the arrival of the first input vector and unbiased only when the pipeline is completely empty. Therefore, the total energy (E_{ABB}) consumed during Δt_{BB} and Δt_{noBB} is:

$$E_{\text{ABB}} = E_{\text{BB}} + E_{\text{noBB}} + 2E_{\text{Cb}} \tag{5.3}$$

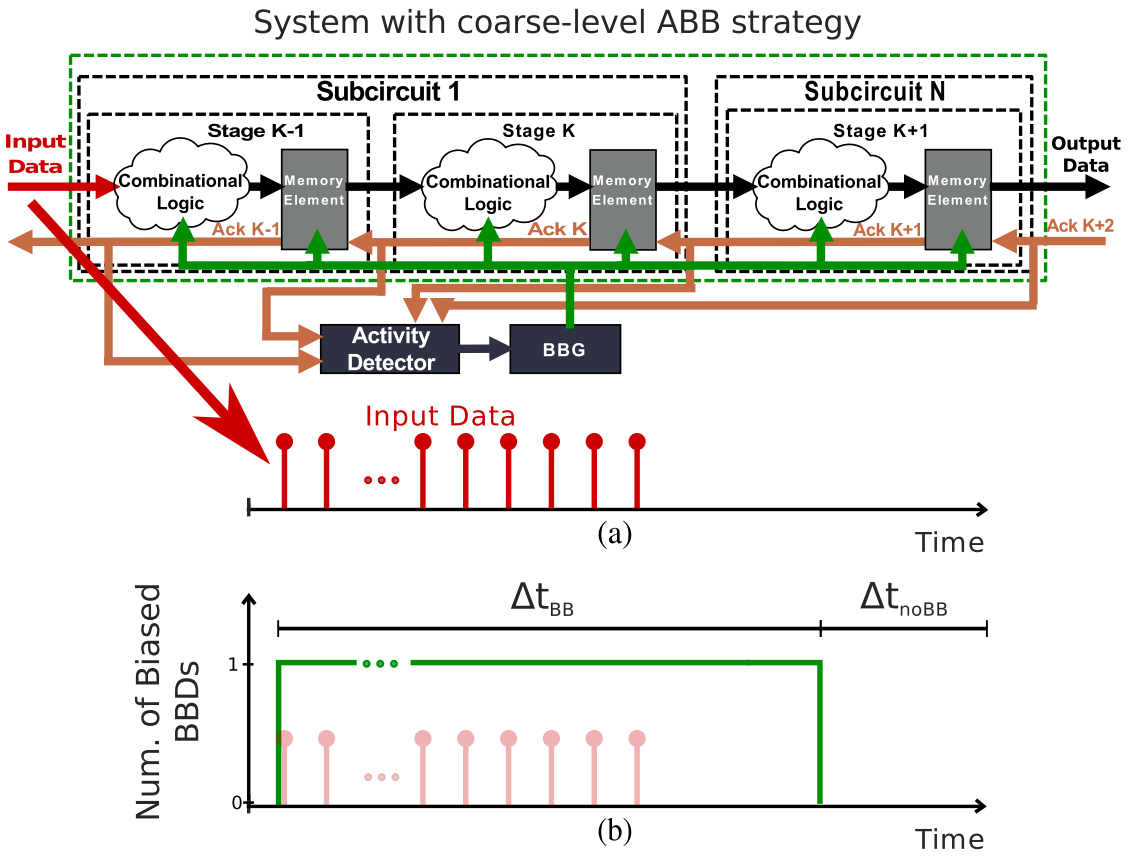


Fig. 5.3: Variation of the number of body biased BBDs with time (b) in a system split into a single BBD - implementation of a coarse-grain ABB strategy - as a burst of input vectors (a) is processed by the system.

$$E_{\mathrm{BB}} = \Delta t_{\mathrm{BB}}(P_{\mathrm{sys}} + P_{\mathrm{ad}} + P_{\mathrm{bc}}) \tag{5.4}$$

$$E_{\mathrm{noBB}} = \Delta t_{\mathrm{noBB}}(P^0_{\mathrm{L}} + P^0_{\mathrm{L,ad}} + P^0_{\mathrm{L,bc}}) \tag{5.5}$$

P_{sys} corresponds to the total power consumption of the target system, including dynamic and leakage power consumption. Thus, it varies with the values chosen for V_{dd} and V_{bb}. P_{bc} corresponds to the power spent by the BBGs; and P_{ad} represents the total power consumed by the activity detection circuitry. E_{Cb} is required for charging the back plane capacitances to the chosen V_{bb} as the system becomes active and, as it turns idle, E_{Cb} is once again consumed to switch the circuit to low performance mode. Consequently a factor 2 appears in equation (5.3).

During Δt_{noBB}, the power consumption in the system and in the activity detection circuitry (P^0_{L} and $P^0_{\mathrm{L,ad}}$ respectively) solely correspond to leakage, since there is no power dissipation due to switching. Moreover, as the system has been switched to low performance mode, the values of P^0_{L} and $P^0_{\mathrm{L,ad}}$ are considerably smaller than the corresponding leakages in the active mode ($P^{V_{\mathrm{bb}}}_{\mathrm{L}}$ and $P^{V_{\mathrm{bb}}}_{\mathrm{bc,L}}$, respectively).

In this context, the total energy overhead (E_{o}) caused by implementing the body biasing strategy described in Fig. 5.2b) and the energy saved (E_{s}) by turning off FBB during Δt_{noBB}

are:

$$E_{\mathrm{o}} = \Delta t_{\mathrm{BB}}(P_{\mathrm{ad}} + P_{\mathrm{bc}}) + 2E_{\mathrm{Cb}} \tag{5.6}$$

$$E_{\mathrm{s}} = \Delta t_{\mathrm{noBB}}(P_{\mathrm{L}}^{V_{\mathrm{bb}}} - P_{\mathrm{L}}^{0} - P_{\mathrm{L,ad}}^{0} - P_{\mathrm{L,bc}}^{0}) \tag{5.7}$$

Finally, the inequality in eq. (5.2) will only be true if the saved energy is greater than E_{o}.

$$E_{\mathrm{ABB}} < E_{\mathrm{alwaysBB}} \iff E_{\mathrm{s}} > E_{\mathrm{o}} \tag{5.8}$$

Substituting equations (5.6) and (5.7) in eq. (5.8) enable deriving the relation between Δt_{BB} and Δt_{noBB} for which eq. (5.2) is true. By expanding this equation and considering that the power consumption (dynamic and static) of the activity detection and BBGs are negligible if compared to the total power consumption of the target circuit, equation (5.8) is simplified to the following relation that determines the minimum Δt_{noBB} that equals the energy overhead with the energy savings, commonly known as minimum idle time (MIT) [165].

$$\Delta t_{\mathrm{noBB}} > \frac{2C_{\mathrm{b}}(V_{\mathrm{bb}})^2}{P_{\mathrm{L}}^{V_{\mathrm{bb}}} - P_{\mathrm{L}}^{0}} \tag{5.9}$$

As previously mentioned in section 5.1.2, C_{b} is a technology dependent factor that represents the back plane capacitance, which is proportional to the area being biased, thus the BBD size.

5.2.2 Analyzing a fine-grain strategy

The same target system analyzed in section 5.2.1 is now considered to be composed of N BBDs, one BBD per pipeline stage (body biasing strategy depicted in Fig. 5.2a). Fig. 5.4b illustrates the variation of the number of biased pipeline stages as vectors are inputted to the system. Differently from what is shown in Fig. 5.3b, now the number of biased stages progressively increases during pipeline loading until the whole system is biased, when the pipeline is full.

For instance, during Δt_{BB1}, data is only being processed in the first pipeline stage. Consequently it is the only part of the circuit that is on high performance mode, thus having a high leakage consumption ($P_{\mathrm{leak,1}}^{Vbb}$). Conversely, the following N-1 pipeline stages are not yet biased, thus the leakage power they consume during Δt_{BB1} is equivalent to no biased ($P_{\mathrm{L,j}}^{0}$). Hence, compared to a coarse-grain strategy (the case analyzed in section 5.2.1), the energy saved during Δt_{BB1} ($E_{\mathrm{s,1}}$) is determined by:

$$E_{\mathrm{s,1}} = \Delta t_{\mathrm{BB1}} \sum_{j=2}^{N} (P_{\mathrm{L,j}}^{Vbb} - P_{\mathrm{L,j}}^{0}) \tag{5.10}$$

The same analysis is done to the following time intervals in pipeline loading. Therefore compared to a coarse-grain strategy, the total energy saved during pipeline loading ($E_{\mathrm{s,pl}}$) is a summation of the individual savings in each interval of pipeline loading:

$$E_{\mathrm{s,pl}} = \sum_{i=1}^{N-1} \Delta t_{\mathrm{BBi}} \Big(\sum_{j=i+1}^{N} (P_{\mathrm{L,j}}^{Vbb} - P_{\mathrm{L,j}}^{0}) \Big) \tag{5.11}$$

As the analyzed target system is an asynchronous circuit, Δt_{BBi} corresponds to the latency of the corresponding pipeline stage (δ_i), which varies with the chosen values of V_{dd} and V_{bb}.

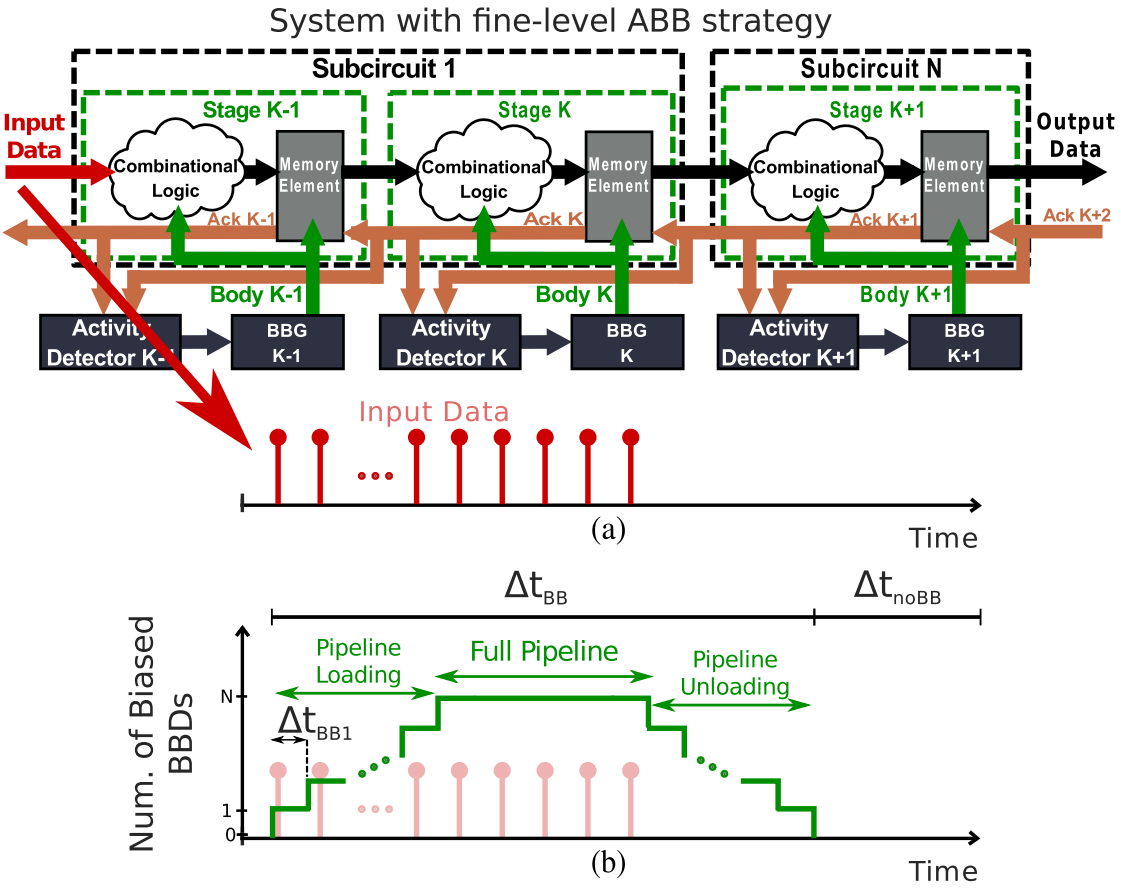


Fig. 5.4: Variation of the number of body biased BBDs with time (b) in a system split into N BBDs - implementation of a fine-grain ABB strategy - as a burst of input vectors (a) is processed by the system.

As soon as each pipeline stage has no data to process, it is switched back to low performance mode, causing the number of biased stages to progressively decrease during pipeline unloading, as shown in Fig. 5.4b. The analyses to evaluate the amount of saved energy during pipeline unloading ($E_{\text{s,pu}}$) is similar to the case of pipeline loading. By following the same reasoning, the energy saved during pipeline unloading is defined by the summation of the individual savings in each interval of the pipeline unloading:

$$E_{\text{s,pu}} = \sum_{j=1}^{N-1} (P_{\text{L,j}}^{Vbb} - P_{\text{L,j}}^{0})(\sum_{i=j+1}^{N} \Delta t_{\text{BBi}}) \tag{5.12}$$

With some algebraically manipulation, it is straightforward to derive that equations 5.12 and 5.11 are equivalent for a balanced pipeline. Thus, for the sake of simplicity, they will be considered equal from now on.

Repeating the energy analysis done in section on the target system 5.2.1, the total energy (E_{fine}) consumed by a fine-grain strategy during Δt_{BB} and Δt_{noBB} is:

$$E_{\text{fine}} = E_{\text{BBfine}} + E_{\text{noBB}} + 2\sum E_{\text{bias,i}} \tag{5.13}$$

$$E_{\text{BBfine}} = E_{\text{BB}} - 2E_{\text{s,pl}} \tag{5.14}$$

$$E_{\text{bias,i}} = C_{\text{b,i}}(V_{\text{bb}})^2 \tag{5.15}$$

Compared to equation (5.3), the total energy consumption during Δt_{BB} (E_{BBfine}) has been updated with the component of saved energy from equation (5.11). The value of E_{noBB} is kept as defined in eq. (5.5) since during Δt_{noBB} the energy consumed by the system is equivalent to a coarse-grain strategy. Moreover, as the area of each BBD of the target system has been reduced, the value of back plane capacitance ($C_{\text{b,i}}$) is now different for each BBD and smaller than C_{b}. Consequently, the energy required to switch the system from low to high performance mode ($E_{\text{bias,i}}$) has been split into smaller components. Equations (5.6) and (5.7) are now rewritten for the case of a fine-grain strategy:

$$E_{\text{o,fine}} = \Delta t_{\text{BB}}(P_{\text{ad}} + P_{\text{bc}}) + 2\sum E_{\text{bias,i}} \tag{5.16}$$

$$E_{\text{s,fine}} = \Delta t_{\text{noBB}}(P_{\text{L}}^{V_{\text{bb}}} - P_{\text{L}}^{0} - P_{\text{L,ad}}^{0} - P_{\text{L,bc}}^{0}) + 2E_{\text{s,pl}} \tag{5.17}$$

Finally, with similar manipulation as done in section 5.2.1, equation (5.9) is derived for a fine-grain strategy:

$$\Delta t_{\text{noBB}} > \frac{2((V_{\text{bb}})^2 \sum C_{\text{b,i}} - E_{\text{s,pl}})}{P_{\text{L}}^{V_{\text{bb}}} - P_{\text{L}}^{0}} \tag{5.18}$$

The MIT for a fine-grain body biasing strategy differs from the one in equation (5.9) by a term $E_{\text{s,pl}}$, determined by equation (5.11). Therefore, the more cycles of pipeline loading and unloading, the smaller is the MIT and consequently more energy savings are achieved compared to a coarse-grain strategy.

5.3 Simulation Results and Analysis

To demonstrate the energy efficiency and performance gains of adaptive body biasing strategies, a case-study circuit was used as target system for the implementation of the 3 different body biasing strategies depicted in Fig. 5.2. The layout of the 3 strategies have been designed using low threshold voltage transistors in FD-SOI 28nm technology. Electrical simulations with post-layout netlists have been done to generate the power consumption and performance results.

5.3.1 Case-Study: 8-bit QDI asynchronous ALU chain

The QDI asynchronous 8-bit ALU proposed in [1] is the base architecture for the implementation of this case-study. It is a 3-stage pipelined circuit, as depicted in Fig. 5.5a, summing a total of 506 logic gates. It has been replicated 5 times, and connected in chain, as depicted in Fig. 5.5b, in order to create a more complex system, more suitable for the implementation of different body biasing strategies. The input of the ALU chain is connected to a Linear Feedback Shift Register (LFSR) that provides pseudo-random input vectors. A completion detection circuit (End Plug in Fig. 5.5b) is connected to the chain output, generating the acknowledgement for the last pipeline stage, thus guaranteeing the correctness of the asynchronous communication protocol at the output of the last ALU of the chain.

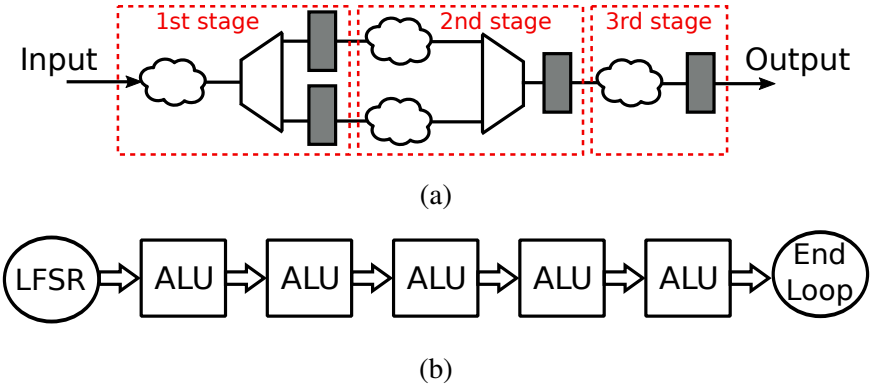


Fig. 5.5: Representation of the pipeline stages of the QDI asynchronous ALU used as base architecture (a), and its connection in chain (b) to serve as case-study of adaptive body biasing strategies. In (a) the clouds represent combinational logic and the grey rectangles represent memory elements. In (b), the input vectors are generated by a LFSR, connected to the first ALU of the chain. A handshake interface (End Loop) is connected to the last ALU of the chain to implement the communication protocol in the system's output stage.

The chain of ALUs is the base for the implementation of three different adaptive body biasing strategies: 1) a coarse-grain strategy, in which all ALUs belong to the same BBD (as shown in Fig 5.2b); 2) a fine-grain strategy, with 1 BBD per pipeline stage of each ALU, summing a total of 15 BBDs (the strategy depicted in Fig 5.2a); and 3) a medium-grain strategy, in which each ALU of the chain belongs to a separate BBD, summing a total of 5 BBDs (the strategy shown in Fig. 5.2c). Additionally, for the sake of comparison, an always biased system was also designed. It is a version of the ALU chain in which the body biasing is always on, independently of circuit activity. Thus, the always biased versions have no BBGs nor activity detection circuitry. The body terminal of all transistors of the target system are connected to V_{bb} from the beginning until the end of each simulation.

5.3.2 Description of experiments

Each simulation, in this work, is characterized by three parameters: 1) V_{dd}; 2) V_{bb}; and 3) activity ratio. In the conducted experiments, the circuits were simulated under nominal voltage (V_{dd} = 1.0 V) and in near-threshold voltage region (V_{dd} = 0.6 V), voltage operation regions that are commonly used for high performance and low power applications respectively. The used V_{bb} values are: V_{bb} = 0 V, a no body biasing scenario; V_{bb} = 1.0 V, an intermediate biasing level; and V_{bb} = 1.5 V, a strong biasing scenario. The third parameter, the activity ratio, is the proportion between active interval (Δt_{BB}) and the following idle period (Δt_{noBB}), previously shown in Fig. 5.3 and Fig. 5.4. It is mathematically defined as:

$$Activity\ \ ratio = \frac{\Delta t_{BB}}{\Delta t_{BB} + \Delta t_{noBB}} \tag{5.19}$$

As the idle period tends to 0, the activity ratio tends to 1, indicating that the system is always processing data. On the other hand, as Δt_{noBB} tends to a large number, the activity ratio tends to 0, indicating that the system is almost always idle.

For each V_{dd}, Δt_{BB} was chosen to minimize the full pipeline time, depicted in Fig. 5.4. A large Δt_{BB} create a long full pipeline time, and consequently decreases the influence of the

savings during pipeline loading and unloading, described by equation 5.11. Therefore, in the experiments conducted in this section, Δt_{BB} is set to approximately the latency of a single ALU, which is 0.5 ns at V_{dd} = 1.0 V and 2.4 ns at V_{dd} = 0.6 V. Δt_{noBB} is then changed accordingly to create the desired activity ratios. For instance, at a V_{dd} = 1.0 V, knowing that Δt_{BB} is 0.5 ns, Δt_{noBB} needs to be equal to 2 ns in order to generate an activity ratio of 0.2.

5.3.3 Results and Analysis

Tables 5.1 and 5.2 show the results obtained from electrical simulations performed with always biased, coarse, medium, and fine strategies. For generating each table, the activity ratio and V_{dd} are kept fixed while V_{bb} varies as shown in the table. In each scenario, the results of total power, operation frequency and energy per operation for each strategy were measured.

If operating at nominal voltage, as shown in table 5.1, the operation frequency of the adaptive body biasing strategies (coarse, medium and fine) is approximately the same as the always biased strategy, which shows the effectiveness of the proposed biasing strategy based on BBGs and activity detection circuitries. The reason for the slight performance gap between the always strategy and the other ones is the latency between detecting activity and fully biasing each BBD. Since both activity detection circuities and the area being biased are particular to each strategy, as described in section 5.1.3, there are slight variations between the performance of coarse, medium and fine strategies. As the number of BBDs increase, so does the biasing activation latency, thus slightly reducing the performance, as shown in table 5.1. If operating at V_{dd} = 0.6 V, as depicted in table 5.2, the performance gap between always biased and the other strategies significantly increases. For instance, the performance of the coarse strategy is approximately 50% of the always biased considering a V_{bb} = 1.5 V. This increased gap is caused by the increase of the latency of the BBGs when operating at low V_{dd}.

The power consumption results, conversely, show significant improvements as the number

Table 5.1: Electrical simulation results for V_{dd} = 1.0 V and activity ratio of 0.1. The values of total power, operation frequency and energy per operation were normalized to the respective values of the always biased strategy for a V_{bb} = 0.0 V and a V_{dd} = 1.0 V.

Vbb (V)	BB strategy	Total Power (normalized)	Operation Frequency (normalized)	Energy per Operation (normalized)
0.0	coarse	1.02	1.003	1.01
	medium	1.02	1.001	1.02
	fine	1.03	0.998	1.03
	always	1.00	1.000	1.00
1.0	coarse	1.49	1.189	1.31
	medium	1.39	1.167	1.19
	fine	1.38	1.168	1.18
	always	1.65	1.191	1.39
1.5	coarse	2.11	1.271	1.73
	medium	1.85	1.255	1.48
	fine	1.81	1.254	1.44
	always	2.79	1.289	2.17

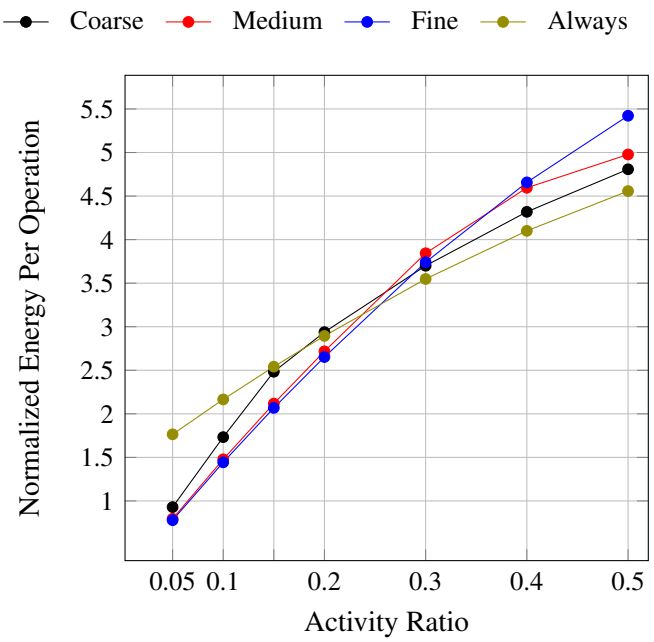
of BBDs and V_{bb} increase. For instance, for the scenario represented in table 5.1, if the target circuit is body biased at V_{bb} = 1.5 V, the fine strategy consumes approximately 14% less power than the coarse one and 35% less than the always biased strategy. The improvement in total power consumption achieved by increasing the number of BBDs (moving from a coarse to a fine strategy) is explained by the savings during pipeline loading and unloading quantified by equations (5.11) and (5.12). The total power consumption results shown in table 5.1 includes the power overhead required for implementing each ABB strategy, i.e. the power consumed by activity detectors (P_{ad}), BBGs (P_{bc}) and the extra power required to change the operation mode (describe by equation 5.1). In table 5.1, in the case of V_{bb} = 1.5 V, this power overhead is approximately 19%, 21%, 24% of the total power consumption for the coarse, medium and fine strategies, respectively.

Reducing the operation V_{dd} to 0.6 V reduces the total power consumption differences between coarse, medium and fine strategies, as shown in table 5.2. In this scenario, the maximum reduction between the power consumption of the fine strategy if compared to the coarse is approximately 8% at V_{bb} = 1.5 V. However, if compared to the always biased strategy, the fine and med strategies power consumption are reduced by a factor of more then 3, which clearly show the advantages of implementing adaptive body biasing strategies with low V_{dd}.

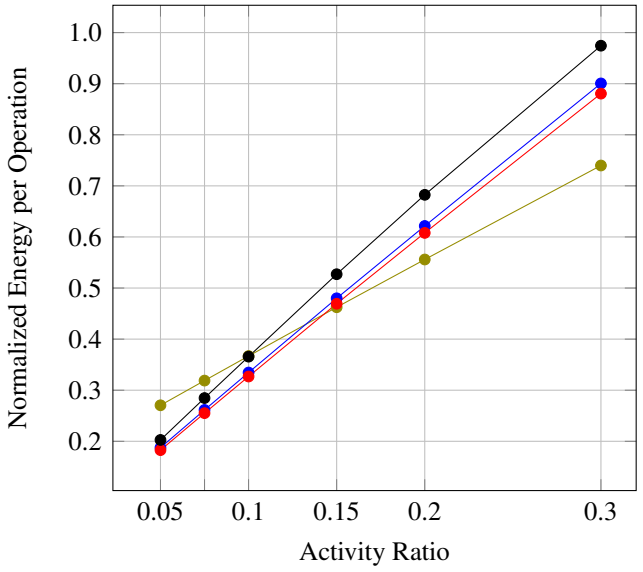
The lower power consumption and relative high performance of the proposed adaptive body biasing strategies, close to the performance of the always strategy if V_{dd} = 1.0 V, make them more energy efficient than the latter. As depicted in tables 5.1 and 5.2, the values of energy per operation of coarse, medium and fine strategies are smaller than the always strategy for any V_{bb} value superior than 0 V. For instance, for V_{dd} = 0.6 V and V_{bb} = 1.5 V the value of energy per operation of the medium strategy is reduced by approximately 52% if compared to the always biased. Moreover, considering the scenarios of table 5.2, applying a V_{bb} = 1.0 V allow keeping the same energy per operation in the medium strategy while increasing the operation frequency by approximately 56% if compared to not applying body biasing (V_{bb} = 0 V).

Table 5.2: Electrical simulation results for V_{dd} = 0.6 V and activity ratio of 0.05. The values of total power, operation frequency and energy per operation were normalized to the measurements of the always biased strategy for a V_{bb} = 0.0 V, a V_{dd} = 1.0 V and activity ratio of 0.1.

Vbb (V)	BB strategy	Total Power (normalized)	Operation Frequency (normalized)	Energy per Operation (normalized)
0.0	coarse	0.05	0.266	0.18
	medium	0.05	0.264	0.18
	fine	0.05	0.265	0.18
	always	0.05	0.264	0.18
1.0	coarse	0.08	0.401	0.20
	medium	0.08	0.412	0.18
	fine	0.08	0.404	0.19
	always	0.18	0.674	0.27
1.5	coarse	0.13	0.476	0.27
	medium	0.11	0.487	0.23
	fine	0.12	0.423	0.29
	always	0.40	0.829	0.48



(a)



(b)

Fig. 5.6: Energy per operation variation with activity ratio of fine, medium, coarse and always biased strategies for a V_{dd} = 1.0 V, V_{bb} = 1.5 V in (a); and V_{dd} = 0.6 V, V_{bb} = 1.0 V in (b). The measurements in (a) and (b) were normalized to the same reference as tables 5.1 and 5.2, i.e. the energy per operation result of the always biased strategy for a a V_{dd} = 1.0 V, V_{bb} = 0.0 V and activity ratio of 0.1.

Finally, Fig. 5.6 depicts the energy per operation variation with activity ratio. In this set of experiments, the V_{bb} and V_{dd} are kept fixed while the activity ratio varies as shown in the x-axis of Fig. 5.6. From these graphs the value of minimum idle time defined by equations (5.9) and (5.18) can be determined. It determines the region of activity ratio in which the coarse, medium and fine body biasing strategies are more energy efficient than the always biased circuit. Out of this region, implementing an always biased strategy consumes less energy per operation, thus

the attractiveness of implementing an adaptive body biasing strategy is diminished.

As depicted in Fig. 5.6a, if the target system is operating at V_{dd} = 1 V and V_{bb} = 1.5 V, the always biased circuit spends less energy per operation than any of the other approaches for activity ratios bigger than 0.3. The calculated values of minimum idle time for fine, medium and coarse strategies in this operation condition are 1.38 ns, 1.23 ns and 2.12 ns respectively. These values determines that for activity ratios bigger than 0.3, the implementation of the coarse, medium or fine strategies are less energy efficient than simply always biasing the target system. As seen in Fig. 5.6a, the always curve is lower than the other curves for any activity ratio bigger than 0.3. In fact, in such cases, the energy overhead described by equation (5.6) and (5.16) are greater than the energy savings of equations (5.7) and (5.17), since Δt_{noBB} is not sufficiently high.

If the target system is operating at V_{dd} = 0.6V and V_{bb} = 1.0 V though, longer idle times are required. From simulation results depicted in Fig. 5.6b, the calculated values of minimum idle time for fine, medium and coarse strategies in this operation condition are 15.64 ns, 14.32 ns and 21.6 ns respectively. In this operation scenario, longer idle times since the energy savings for a smaller V_{bb} are also smaller. Therefore, as depicted in Fig. 5.6b, for activity ratios bigger than 0.15, the implementation of the coarse, medium or fine strategies are less energy efficient than simply always biasing the target system.

The results presented in this section would be further enhanced by improving the architecture of the BBGs. Reducing the BBG activation latency would improving the operation frequency of fine and medium strategies and increase the energy saved during pipeline loading and unloading, described by equation (5.11), especially if the target circuit is operating in low V_{dd}. Moreover, assigning different V_{bb} levels to each BBD, as presented in [74], would further enhance the energy efficiency of medium and fine strategies.

5.4 Conclusions

This chapter analyzed the energy efficiency and performance gains of three different adaptive body biasing strategies on asynchronous circuits. The aim of this work was evaluating the optimum granularity for implementing adaptive body biasing in asynchronous circuits. Therefore, each analyzed strategy partitions a target case-study circuit in a different BBD configuration. Results show that implementing adaptive body biasing strategies allow maintaining the performance gains featured by body biasing while reducing its drawback, the significant power consumption increase, by approximately 35%. Therefore, lower energy per operation is achieved by implementing adaptive body biasing strategies, especially if the target system is partitioned into small BBDs (the fine strategy in this work).

Moreover, this study provided a methodology for analyzing the energy efficiency of adaptive body biasing strategies. Therefore, by evaluating the activity rate of the target system, we delimited the regions of operation in which implementing each strategy is feasible. Future works will include improving energy and performance results obtained with low V_{dd} by enhancing the architecture of the level-shifter based BBGs.

Chapter 6

A body built-in cell for body biasing subcircuits of integrated systems and detecting transient faults

Besides energy efficiency, reliability is also nowadays one of the main concerns for nanoelectronic systems. Although in the past the dynamic energy has been the dominant source of consumption, in the deep sub-micron era the significantly increased sub-threshold leakage is making the static power comparable to the dynamic consumption [127]. Therefore, guaranteeing high energy efficiency in advanced technology nodes requires the use of techniques to mitigate leakage. In this context, tuning V_{th} through body biasing has been shown to be an effective alternative to overcome this issue [26, 51]. As described in chapter 2, by artificially increasing transistors threshold voltage (V_{th}) the leakage is reduced, a scheme known as RBB. Alternatively, decreasing V_{th}, a technique known as FBB, increases transistors performance. The attractiveness of body biasing is increased by applying an ABB scheme, as presented in chapter 5. Implementing it requires special cells, commonly known as body bias generators (BBG), that need to be embedded to the system thus properly controlling the V_{bb} during circuit operation, as shown in chapter 5. Th implementations based on level-shifters represent a promising solution, specially for fine-grain body biasing, as demonstrated in chapter 5.

Another major challenge faced by nanoelectronic systems is reliability, especially for applications in which failure is critical, e.g. satellites, aircrafts, nuclear power plant robots. The harsh environment in which such devices are inserted are susceptible to high radiation exposure or environmental variations, that may induce parasitic transient currents. These transient faults (TF), which are indeed temporary voltage level modifications, affect the circuits for a short duration of time, and their occurrence are not predictable. Consequently, TFs need to be detected and corrected at run-time to avoid the occurrence of soft errors. Among the existing design strategies, the Body Built-In Current Sensors (BBICS) are a promising solution for detecting TFs, and are perfectly suitable to be integrated in IC standard-cell based design flows [54, 105, 133].

In fact, the robustness of a system is strongly related to its frequency of operation, power supply voltage (V_{dd}), and V_{bb} [49]. Thus, power management and fault tolerance techniques need to be jointly considered. Studies have shown that FBB reduces the soft error rate induced by radiation, while applying RBB increases it [57, 67]. Furthermore, both ABB and transient fault detection techniques require special cells to provide the appropriate V_{bb} for transistors.

This chapter presents a novel cell that merges the functionalities of BBICS and level-shifters based BBGs. Therefore, the proposed architecture is capable of: 1) detecting short-duration, or

long-duration TFs; 2) controlling transistor's V_{th} thus compensating alterations induced by aging or PVT variations; 3) optimizing the system trade-off between low-power and high performance. The design of a single cell with multiple purposes allows to further reduce the already low area overhead imposed by the elements of the BBICS and level-shifter circuitry. It also facilitates the cell insertion in a standard design flow. The work of this chapter was published in the Microelectronic Reliability journal 2018.

The following sections of this chapter are organized as follows: section 2 presents the fundamental on detecting TFs with BBICS and briefly recapitulates how to implement ABB schemes. The following section describes the architecture and the behavior of the proposed body built-in cell, and precises how it is used for both body biasing and TF detection. Section 4 explains the experiments conducted and the results obtained with the proposed architecture inserted into a target circuit, and section 5 concludes this chapter.

6.1 Fundamentals

6.1.1 Implementing ABB schemes

As previously explained in chapter 5, the attractiveness of RBB and FBB is increased by implementing ABB schemes. The idea is to decrease V_{th} during active periods, to enhance circuit performance, and increase it during idle periods to prevent unnecessary leakage. Implementing such ABB schemes requires special cells, known as BBGs. Since this work is focused on applying ABB in sub-circuits of an integrated system, level-shifter based BBG architectures are preferred, thus less area overhead is achieved by reducing the BBG complexity. Fig. 6.1 depicts an abstraction of the ABB strategy used in this work, as previously shown in chapter 5.

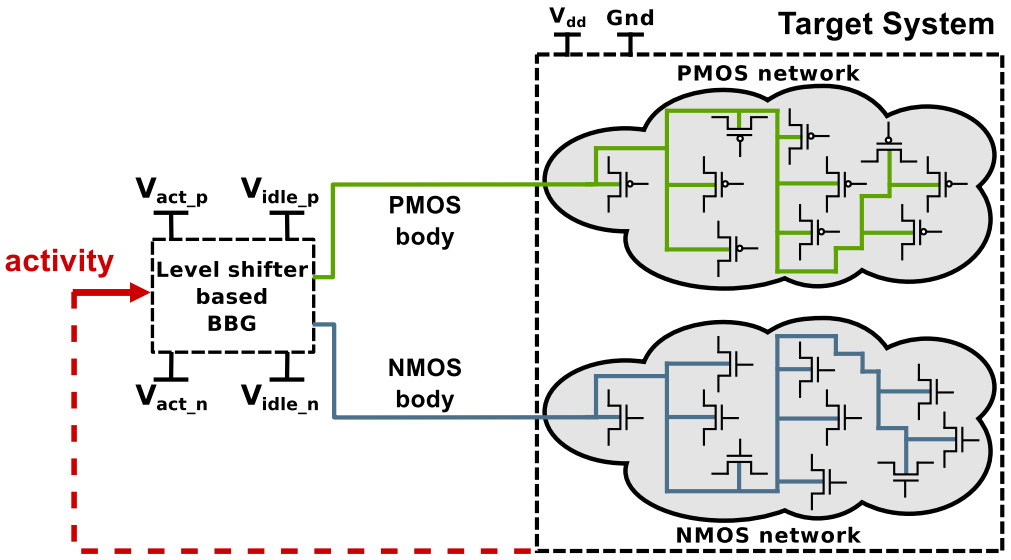


Fig. 6.1: Abstraction of a level-shifter based BBG controlling the V_{th} tuning of a generic target system.

The body biasing strategy shown in Fig. 6.1 applies to both RBB and FBB schemes. In fact, what differentiates these strategies is the choice of voltage levels of V_{idle_n}, V_{idle_p}, V_{act_n} and V_{act_p}. For instance, in order to implement FBB $V_{idle\_n} = 0$; $V_{idle\_p} = 0$; $V_{act\_n} > 0$; and $V_{act\_p} < 0$.

The experiments described in section 6.3 were performed with FBB. The procedure to perform simulations with a RBB scheme is analogous to what is described in section 6.3.

The feasibility of level-shifter based BBGs for ABB relies on: 1) low delay, rapidly switching from low-leakage to high-performance mode and vice versa; 2) very low power consumption, in order to minimize the power overhead; 3) proper operation at low V_{dd}, in which minimum energy is reachable [159]. Therefore, these parameters are used in the experiments described in section 6.3 to evaluate the efficiency of the proposed body built-in cell for implementing ABB schemes.

6.1.1.1 State-of-the-Art level shifter architectures

The fundamental purpose of a level shifter is converting an input signal V_{in} from a certain voltage level (V_{DDL}) to another voltage level (V_{DDH}) in the output V_{out}. It is used for implementing ABB schemes since the voltage levels of V_{bb} is generally higher than the target system V_{dd} in order to increase the energy efficiency, as demonstrated in the experiments of chapter 5.

Many level shifter architectures have been proposed by the scientific community. They have been classified in this section into five categories defined according to the presence of the following particular internal structures: (I) cross-coupled PMOS transistors; (II) diode-connected transistors; (III) pass transistors; (IV) current mirrors; and (V) dynamic logic.

(I) **Cross-type level shifters**: several architectures have been proposed using the principles of the differential cascode voltage switch (DCVS) CMOS logic [58] to mitigate static current overheads [149, 154, 160, 169]. Fig. 6.2 and Fig. 6.4 illustrates DCVS structures (inside dashed boxes), which are cross-coupled PMOS pairs forming two pull-up networks (PUNs) complemented by two pull-down networks (PDNs). A basic DCVS-based level shifter architecture is shown in Fig. 6.2.

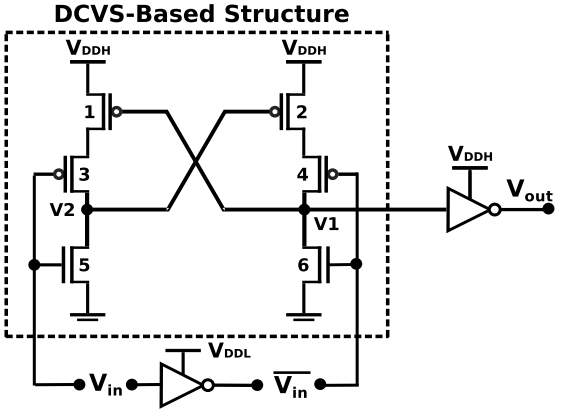


Fig. 6.2: State-of-the-art cross-type level shifter [149].

(II) **Diode-type level shifters**: adding diode-connected transistors, in order to limit the current in a typical DCVS structure, has been proposed by several architectures [36, 52, 70, 78,79,119,130,164,172]. Recently, Lanuzza et al. [78] have proposed the level shifter depicted in Fig 6.3. Additionally, a self-adapting boost circuit increases the strength of each level shifter branch during their charging phase, and weakening them in the discharging phase.

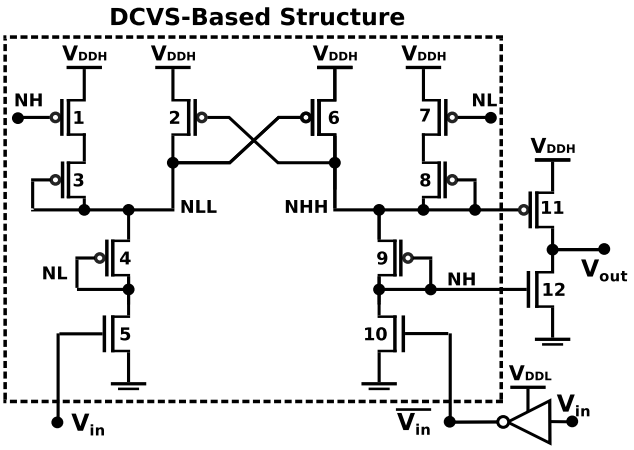


Fig. 6.3: State-of-the-art diode-type level shifter [78].

(III) **Pass-type level shifters**: in the early 2000s, architectures employing pass transistors and other complementary structures were presented in [55, 75, 119, 131, 145] to improve classic level shifter structures.

(IV) **Mirror-type level shifters**: architectures based on current mirrors have been proposed to feature wider input voltage range at Vin. [23, 27, 59, 72, 83, 84, 94, 114, 173]. Fig. 6.4 illustrates a level shifter architecture using two Wilson current mirrors connected to a conventional level shifter structure [23].

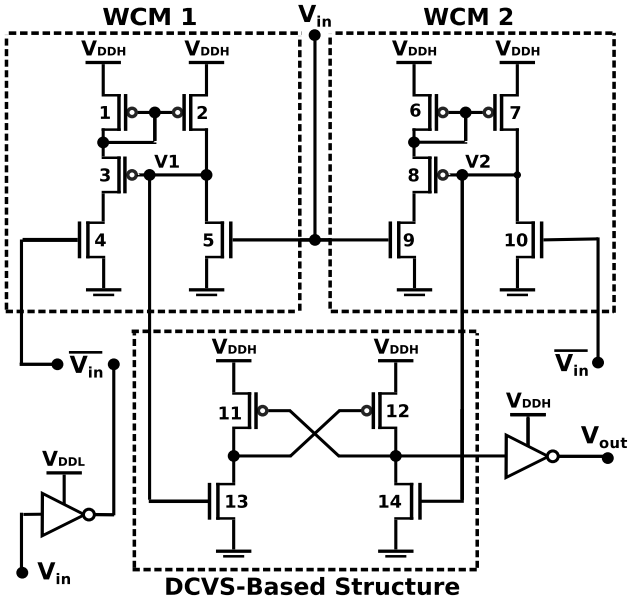


Fig. 6.4: State-of-the-art mirror-type level shifter [23].

(V) **Dynamic-type level shifters**: another type of LS architecture was proposed in [63] and [24] by exploiting dynamic logic to operate at lower voltage levels. The dynamic-type LS architectures require a circuitry for the precharge phase of the dynamic logic.

6.1.2 Detecting TFs with BBICS

The so-called body or bulk built-in current sensors (BBICS) are used to detect abnormal transient currents flowing from the body to the drain (or vice versa) of sensitive transistors (reverse-biased PN junctions) of a design under test (DUT) [105]. Fig. 6.5 depicts an abstraction of a BBICS monitoring a target system. It shows a current source (I_{FaultN}), that models a transient fault (TF) occurring in one of the NMOS transistors of the target system. As shown in Fig. 6.5, the voltages that bias the body of the NMOS and PMOS transistors (V_n and V_p respectively) are provided by the BBICS. Thus, there is no direct connection between the body terminals of the target system and the power rails, as depicted in Fig 6.5. Whenever an atypical current is detected, an output flag is raised (Flag signal in Fig 6.5), indicating the occurrence of a TF. The threshold at which the BBICS is capable of detecting a TF is defined as the BBICS sensitivity and it is determined by the number of transistors in the target system and the architecture of the BBICS [118]. Therefore, two strategies are used to calibrate the range of TF detectable by a BBICS: 1) splitting the target system into sub-circuits, each one of them monitored by an independent BBICS, thus reducing the number of monitored transistors per sensor; 2) changing the size and drive strength of some specific transistors of the BBICS. In this work, for the sake of simplicity, only the NMOS sensor is analyzed. The analyses of the PMOS case is analogous.

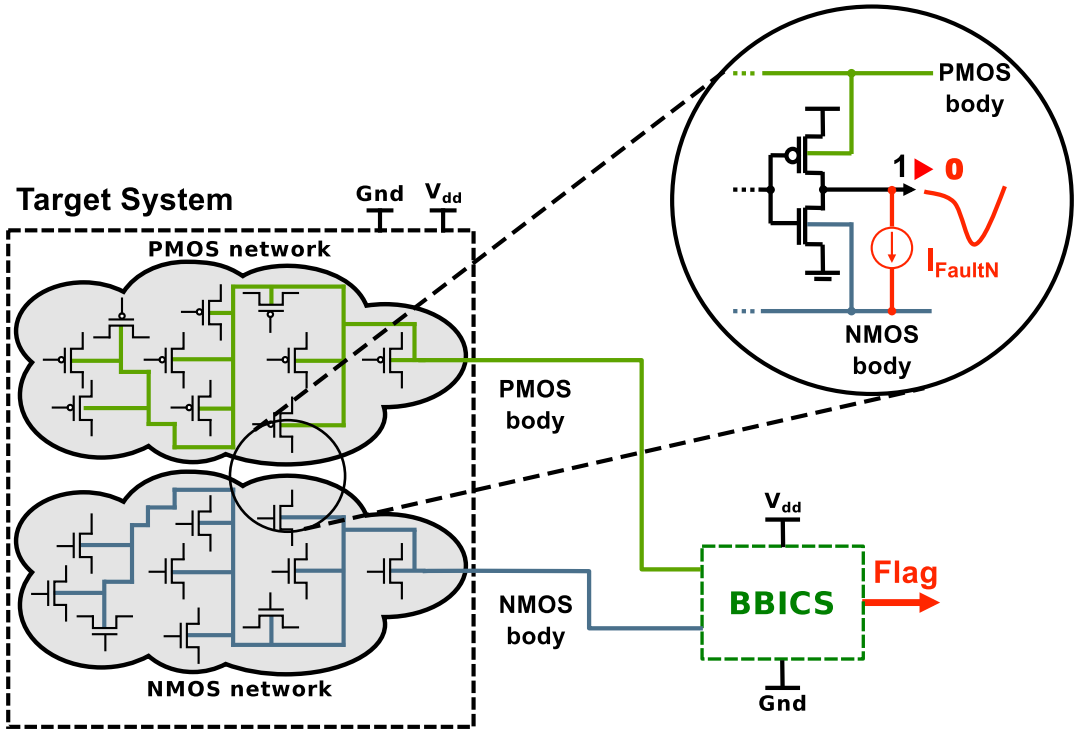


Fig. 6.5: Abstraction of BBICS monitoring a generic target system. A zoom in an arbitrary part of the system details the occurrence of a TF, modeled as a current source, temporarily changing the output of an inverter from 1 to 0.

6.2 Proposed body built-in architecture

The body built-in cell proposed in this work unites the strategies described in sections 6.1.2 and 6.1.1. Therefore, the proposed architecture is composed of two parts: a level-shifter based

structure, depicted in Fig. 6.6 inside a dashed black box; and a current sensor based structure, shown inside the dashed green box of Fig. 6.6. The body built-in cell described in the sequel corresponds to the circuitry necessary for biasing and monitoring the NMOS transistors of a target system. The architecture for the PMOS network is analogous.

6.2.1 Level-shifter structure

This part of the proposed body built-in cell ensures a proper implementation of the ABB strategy described in section 6.1.1. The functionality of the level shifter of Fig. 6.1 is implemented by the circuitry inside the dashed black box of Fig. 6.6. Therefore, if the input signal boost of Fig. 6.6 changes from 0 to 1, indicating that body biasing should be activated, the node V2, previously set to $V_{\text{act\_n}}$, will discharge to logical 0 through the transistor 5. After discharging, V2 will activate the transistor 2, thus enabling the node V1 to charge (the transistor 4 was already activated by the signal FB). Finally, the body biasing voltage $V_{\text{act\_n}}$ is provided to the body of NMOS transistors of the target system through the terminal NMOS Body, output of the transmission gate formed by transistors 9 and 10.

Once V1 has reached $V_{\text{act\_n}}$, forcing $\overline{FB}$ to 0, the transistor 3 will be activated, and the signal FB will deactivate transistor 4, preparing the pull-up branches of the Level-Shifter based structure for the next input transition of the boost signal. The signals FB and $\overline{FB}$ ensure that transistors 3 and 4 change their voltage levels only after V1 has changed. The delay of these feedback signals has to be controlled to certify that the nodes V1 and V2 have fully switched to $V_{\text{act\_n}}$ or 0 before affecting transistors 3 and 4. The level-shifter based structure has an analogous behavior when the boost signal changes from 1 to 0, indicating that body biasing should be deactivated.

The implemented level shifter architecture is an amelioration of the classical cross-type

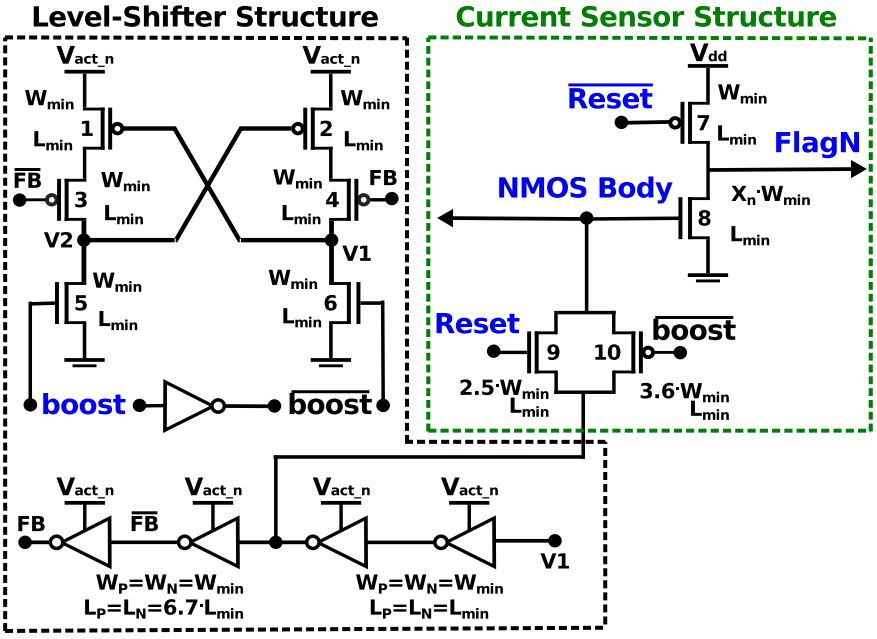


Fig. 6.6: The proposed body built-in cell architecture. The inputs and outputs are marked in blue. X_n is a design factors used for calibrating the sensitivity of the sensor in detecting transient faults.

architecture, the weak contention level shifter presented in [7]. Its feedback signals FB and $\overline{FB}$ help reducing the cell leakage, even under ultra-low voltage operation [7].

6.2.2 Current sensor structure

The role of this part of the proposed body built-in cell is to detect TFs. If an abnormal transient current occurs, it will be signaled through the output FlagN. Its architecture is based on dynamic BBICS. Instead of the conventional latch of the static BBICS architectures, that requires a feedback to maintain the output flag voltage level, a dynamic memory cell is used (transistors 7 and 8 in Fig. 6.6). With no feedback circuit wired to FlagN, the sensitivity of the sensor in detecting TFs is increased and its transistor count is reduced.

As in any dynamic CMOS circuit, a periodic signal ($Reset$ and $\overline{Reset}$ in Fig. 6.6) is required to periodically refresh the sensor memory node. It is mandatory to remove accumulative leakage effects on the sensor output, thus preventing consequent false indications of fault. The results in [118] show that a dynamic BBICS designed in a bulk CMOS 65-nm technology is able to properly function by using a short reset pulse with a period of 50 ns. The transistors 9 forces the NMOS bulk node to a temporary floating state, in order to facilitate the switching of transistor 8 in the case of TFs. Thanks to the large channel-width of transistor 8, the dynamic output FlagN is a steady voltage signal that lasts long enough to be dealt by other system blocks, applying corrective actions if a transient fault occurs.

6.3 Simulation Results and Analysis

The operation of the proposed body built-in cell was electrically simulated in FD-SOI 28 nm technology with low threshold voltage transistors. The NMOS Body terminal (shown in Fig. 6.6) was connected to the body of the NMOS transistors of three different target systems: 2, 4 and 6 chains of 10 standard inverters of minimum size. The performed experiments have the purpose of: 1) evaluating the effectiveness of the cell in providing multiple body biasing voltage levels, for different target systems; 2) determining how the cell sensitivity to TFs change with the variation of the size of the target system; and 3) determining how the process and temperature variations influence the sensitivity of the proposed cell towards TFs. Since the activation of body biasing directly affects the cell sensitivity towards TFs (setting NMOS Body to $V_{\text{act\_n}}$ triggers the output FlagN), body biasing and TF detection schemes are evaluated separately. To isolate the influence of body biasing in the activation of the output FlagN, a simple AND gate with inputs boost and FlagN is sufficient. In all performed simulations, the parasitic capacitances and resistances have been included.

6.3.1 Body biasing efficiency

For analyzing the effectiveness of the proposed cell in providing body biasing voltage levels to a target system, a periodic pulse with frequency of 20 MHz has been applied to the boost input. A FBB scheme was set up, thus $V_{\text{idle\_n}}$ = 0 V; $V_{\text{idle\_p}}$ = 0 V; $V_{\text{act\_n}}$ = 1 V; and $V_{\text{act\_p}}$ = -1 V. To verify the limits of correct operation of the cell, in which the level-shifter based structure needs to convert near-threshold into nominal voltage levels, a parametric analysis simulation was performed varying the voltage level of the boost input signal. The simulated voltage levels of boost are depicted in the x-axis of Fig. 6.7. Each curve in the graphs of Fig. 6.7 represents the response of the proposed body built-in cell when connected to a different target system. While

evaluating the body biasing functionality, no TF was injected since FBB drastically reduces the probability of TF occurrence [57, 67].

For each simulation, the following three figures of merit were considered: delay, transition energy and static power, shown in Fig. 6.7a, Fig. 6.7b and Fig. 6.7c respectively. The delay is the latency of the cell to charge NMOS Body to V_{act_n}/V_{idle_n} after the rising/falling of the boost input signal. The transition energy is defined as the energy consumed by the proposed cell when converting the output NMOS Body from V_{idle_n} to V_{act_n} and vice-versa; and the static power is the leakage of the cell when NMOS Body has reached a stable voltage (there is no switching of its transistors). Each figure of merit value in the graphs of Fig. 6.7 is the average of a simulation

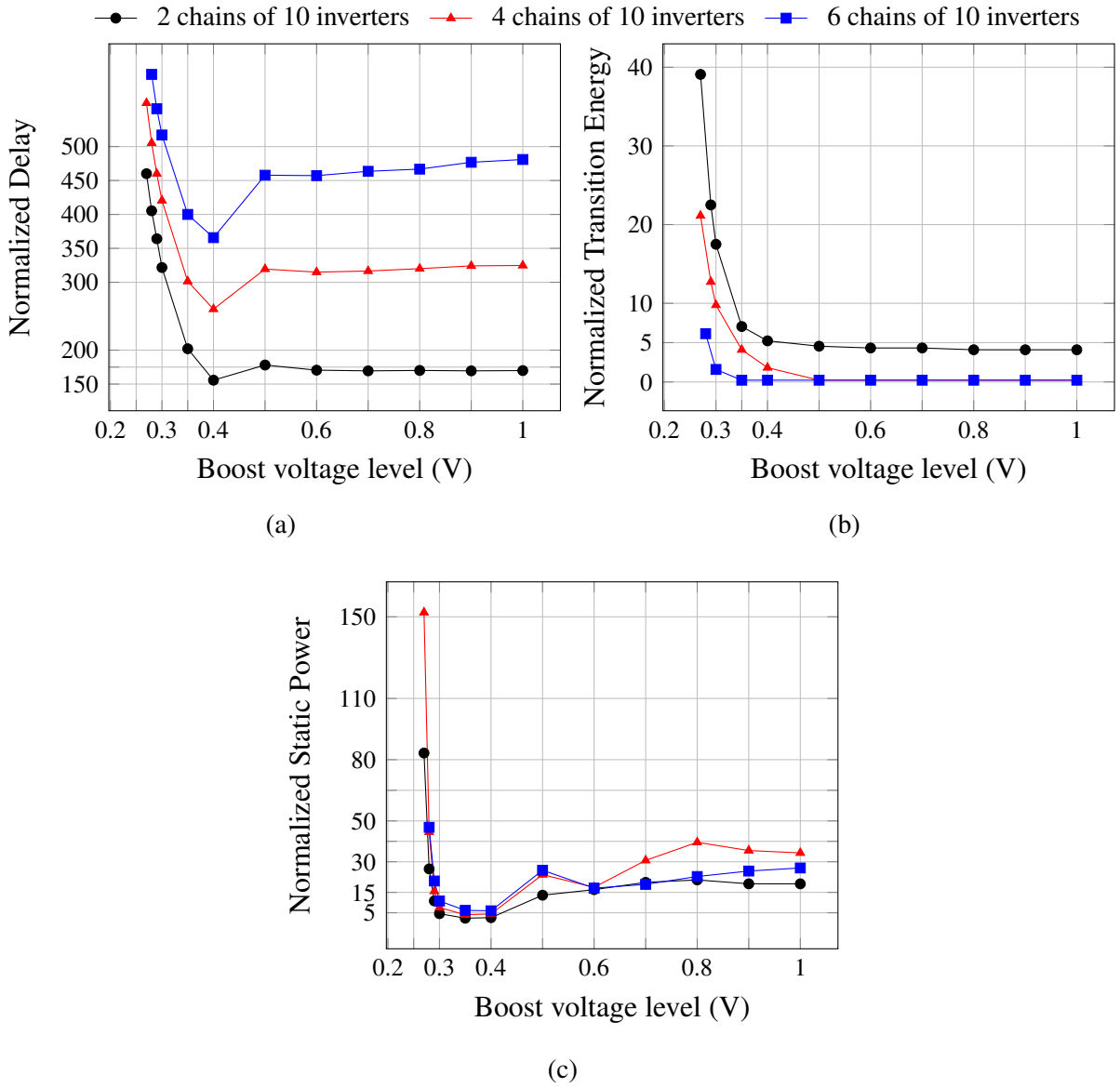


Fig. 6.7: Normalized average results of delay, transition energy and static power consumption of the proposed body built-in cell biasing 2, 4 and 6 chains of 10 inverters, with fixed V_{act_n} = 1 V. All points of these graphics are normalized to the results of the technology standard LVT inverter with minimal drive operating at V_{dd} = 1 V, and a temperature of 27^{o}C. The reference values used in the normalization are: 4.88 ps, 0.43 fJ and 4.35 nW for graphs a), b), and c) respectively.

result obtained during body biasing activation (when the NMOS Body output passes from V_{idle_n} to V_{act_n}) and the results during its deactivation (when the NMOS Body output passes from V_{act_n} to V_{idle_n}). All simulation results shown in the graphs of Fig. 6.7 has been obtained with feasible boost voltage inputs, which is defined, in this work, as an input capable of changing the output node NMOS Body voltage from V_{idle_n} to V_{act_n} in a maximal delay of 5 ns.

The proposed body built-in cell shows a very stable operation for a boost signal voltage level ranging from 0.4 V to 1.0 V. In this region of operation, the delay and the transition energy remain practically unchanged, for the 2,4 and 6 inverter chain curves, certifying the proposed cell capacity of providing a wide range of body biasing voltages with almost constant delay and low energy overhead. In the same operation region, the static power consumption significantly decreases for the three target circuits depicted in Fig. 6.7c. For instance, for the 2 inverter chains circuit, there is a reduction of approximately 3x in the static consumption between 1 V and 0.4 V.

The significant delay difference between the three curves of Fig. 6.7a, for this operation interval, is mainly due to the sizing of transistors 9, 10 and the inverter connected to the output of the level-shifter based structure. The sizing was optimized for a target system equivalent to 2 chains of 10 inverters. Better delay results are easily obtained by resizing these transistors to other target systems.

As the boost voltage decreases below 0.4 V, the figures of merit for all simulated target systems exponentially increase. For instance, if the cell is biasing 2 inverter chains, its static power consumption at 0.27 V (higher point of the black curve of Fig. 6.7c) is approximately 16x higher than its value at 0.4 V, while the delay is approximately 3x higher. The proposed cell does not properly operate with a 6 inverter chains for a boost voltage level smaller than 0.28 V (the highest points in the blue curves of Fig. 6.7). The extremely high power and energy overheads make the cell usage bellow 0.35 V impractical.

Subsequently, a Monte Carlo (MC) simulation has been done to evaluate the robustness of the proposed architecture against process variations and device mismatch. The graphs in Fig. 6.8a and Fig. 6.8b respectively show the measures of the transition energy and the static power consumption versus the delay of the 1000 runs of the performed MC simulation. The closer the points are to the lower-left corner of the scatter plot, the better they are, since it represents a low consumption and high performance cell. The obtained normalized standard deviations (σ/μ) of the energy and power consumption are respectively 0.05 and 0.39, which are comparable to those obtained by similar level-shifter architectures [7]. The high concentration of the points of Fig. 6.8 in the x-axis indicates a rather low performance variation with process, mainly due to the absence of pull-up network contention in the level-shifter based structure of the proposed cell. The point dispersion in the y-axis of Fig. 6.8b indicates a slight variation of power consumption with process.

6.3.2 Detecting TFs

For evaluating the sensitivity of the proposed body built-in cell towards TFs, the target system is set to the biasing scenario that is more susceptible to TFs: a no body biasing [67]. Therefore, during this experiment the boost input was set to 0, forcing the NMOS Body terminal of the proposed cell is to V_{idle_n} = 0 V. A single TF is then injected between the 5th and the 6th inverter of one of the monitored chains. Different profiles of single transient faults were investigated. Each TF was modeled as a double exponential current source with short rise time and a longer fall time, the classical transient fault model for CMOS circuits [42, 47]. The rise time of every

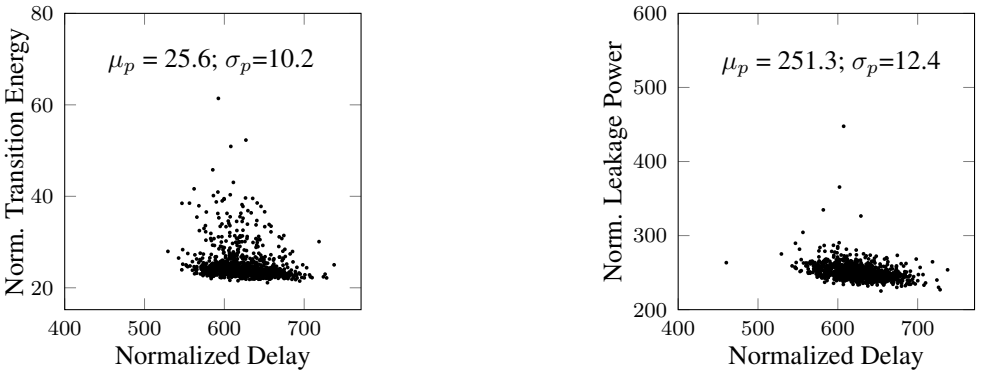


Fig. 6.8: Monte Carlo simulation for 1000 runs ($V_{\text{act\_n}}$ = 1 V, V_{dd} = 0.6 V, frequency of 20 MHz and temperature of 27^{o}C). The simulated results were normalized to the equivalent values obtained for a standard LVT inverter with minimal drive. The reference values used in the normalization were: 4.88 ps, 0.43 fJ and 4.35 nW.

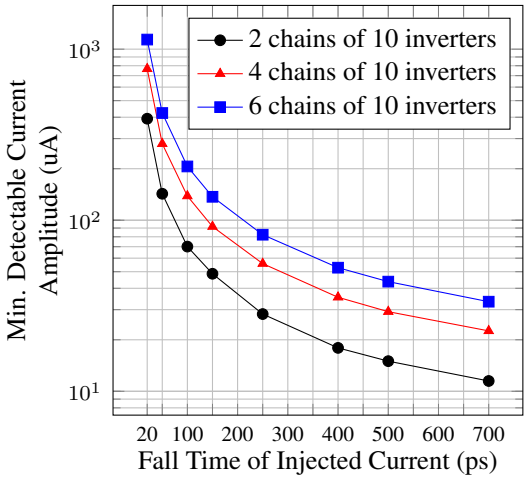
simulated current was fixed to 5 ps while the fall time vary from TF to TF, as depicted on the x-axis of Fig. 6.9a and Fig. 6.9b. Moreover, as the shape of a transient fault is technology dependent, the sweep of the injected current was limited to not create voltage amplitudes higher than 100% of Vdd in any node of the target system. This strategy prevents the injection of voltage peaks leading to permanent damage to the circuit or behaviors out of the technology's specifications.

For each considered fall time, the amplitude of the injected transient current is adjusted to the smallest value capable of triggering the output *FlagN* of the proposed cell with a maximal delay of 3 ns. For instance, if the transient current is injected 10 ns after the simulation started, the TF is considered to be detected if the output node FlagN is set to logic 0 at 13 ns. The obtained minimum detectable current amplitudes for each selected fall time are depicted in y-axis of Fig. 6.9a and Fig. 6.9b.

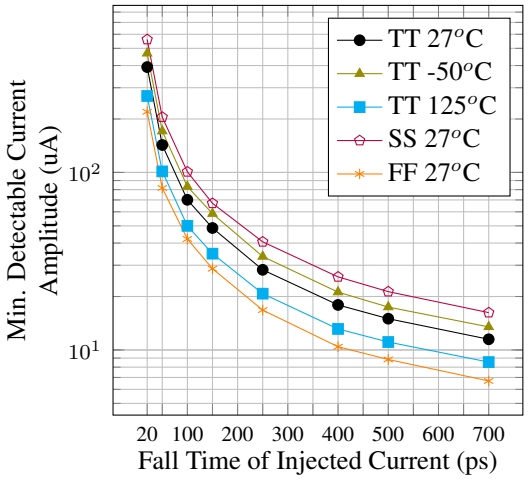
The aforementioned simulation procedure have been repeated for different target systems, in order to investigate the influence of the number of monitored transistors (target system size) to the sensibility of the current sensor structure of the proposed body built-in cell. The obtained results are shown in Fig. 6.9a. Each curve represents the simulation results for the proposed cell monitoring a different number of inverter chains, for a reference temperature of 27 ^{o}C and a typical process corner.

In all the simulated scenarios, the proposed cell was able to detect both short and long transient faults, with fall times ranging from 20 ps to 700 ps (x-axis of Fig. 6.9a). For instance, with a TF of 5 ps of rise time and 100 ps of fall time, any transient current with amplitude greater than 70 μA are detected, if the proposed cell is monitoring 2 inverter chains (black curve). For the same TF profile (5 ps rise time and 100 ps fall time), increasing the number of monitored transistors also increases the minimum detectable current. It increases to approximately 150 μA and 200 μA, if the cell is monitoring 4 and 6 inverter chains, respectively. This behavior is expected since increasing the number of monitored transistors also increase the equivalent capacitance tied to the node NMOS Body of the proposed cell (shown in Fig. 6.6), thus making the switching of transistor 8 more difficult.

To show the resilience of the proposed cell against environmental effects and how the cell sensitivity varies with different operation scenarios, the experiment was repeated for multiple process corners and temperatures, considering a target system of 2 inverter chains. The obtained



(a)



(b)

Fig. 6.9: Minimum current amplitudes detectable by the proposed body built-in cell with the injection of a single TF with rise time of 5 ps. In a) the cell sensitivity is being compared for a varying number of monitored transistors, in a typical process and temperature of 27^{o}C. In b), the cell is monitoring 2 chains of 10 inverters in multiple process corners: typical (TT), fast-fast (FF) and slow-slow (SS); and multiple temperatures.

results are shown in Fig. 6.9b. The black curve is the same in both Fig. 6.9a and Fig. 6.9b. The temperature has an inverse impact on the cell sensitivity: as it decreases, the minimum detectable current increases. This behavior is depicted by the black, olive and blue curves of Fig. 6.9b. The reason is mainly the inverse relation between transistors V_{th} and temperature [39], which facilitates the switching of transistor 8 at higher temperatures. For instance, the minimum detectable current drops from 70 μA to approximately 50 μA if the temperature increases from 27^{o}C to 125^{o}C (black and cyan curves, respectively, in Fig. 6.9b).

The proposed body built-in cell was also robust against process variations, as shown by the orange and purple curves in Fig. 6.9b. Analyzing the same TF profile, a variation of process from TT to SS causes an increase of the minimum detectable current of approximately 30 μA. Conversely, a fast-fast (FF) corner variant cause a decrease of roughly 20 μA.

6.4 Conclusions

In this chapter a novel body built-in cell has been presented and analyzed. It is capable of: 1) detecting short-duration (20 ps fall time) and long-duration (700 ps fall time) TFs, even under temperature and process variations, showing its resilience against environmental effects; 2) efficiently implementing ABB schemes with a wide biasing voltage range: the cell shows a very stable operation for a boost signal voltage ranging from 0.4 V to 1.0 V for target systems simulated in FD-SOI 28-nm technology. A chip, described in details in chapter 8, has been fabricated to validate the proposed cell. The testing of the chip will begin in the next months. Future works will include adapting the proposed architecture for detecting TFs that occur during body biasing, an operation scenario that needs to be studied in more details. Moreover, considering that current sensors have been previously used for detecting hardware Trojans [53], future research will also include evaluating the use of the proposed cell for detecting hardware Trojans.

Chapter 7

An ASIC Design flow adapted for asynchronous systems with multiple BBDs

Manufacturing QDI asynchronous ICs exploiting the energy efficiency gains of ABB presented in chapter 5 is a challenging task. The viability of designing such type of circuits relies on the development of a dedicated standard-cell based IC design flow, since the required steps for achieving the analyzed ABB schemes depend on non-standard design steps. Moreover, the use of standard CAD tools provided by the major EDA vendors is crucial to convince the industry to take advantage of the demonstrated gains of ABB strategies for asynchronous circuits.

This chapter is focused on adapting a standard-cell based IC design flow to exploit the body-biasing features of the FD-SOI technology and the locality of data synchronization of asynchronous circuits to implement ABB systems. All the necessary building blocks for assembling a dedicated flow have already been presented in previous chapters of this thesis. The first one is the architecture of level-shifter based BBG, an issue that has already been addressed in chapter 6. It is a fundamental element for changing transistors V_{th} during circuit operation, especially for small BBDs. Another crucial building block for the implementation of the analyzed ABB schemes is the circuitry that detects activity, signaling the correct moment to switch between low-leakage to high-performance mode ans vice versa, an issue addressed in details in chapter 5. A detailed description of the necessary place-&-route steps for enabling the creation of multiple BBDs is presented in this chapter.

Finally, in order to validate the designed BBG architecture and the proposed design flow, a testchip prototype has been designed, fabricated and tested. The top architecture is composed of multiple IPs implementing the different ABB strategies described in chapter 5. By the end of this chapter the preliminary measurements obtained with the testchip are presented.

7.1 The proposed standard-cell based IC design flow

Fig 7.1 depicts the steps of the proposed standard-cell based IC design flow for exploiting the asynchronous synchronization locality to implement ABB strategies in FD-SOI technology. The red rectangles represent the steps of the proposed design flow that have been modified from or added in an IC standard flow. The asynchronous synthesis step was achieve thanks to the collaboration with our partners Tiempo Secure and STMicroelectronics, which provided the specialized synthesis tool ACC (Asynchronous Circuit Compiler) and the asynchronous standard-cells library necessary for the synthesis of QDI circuits.

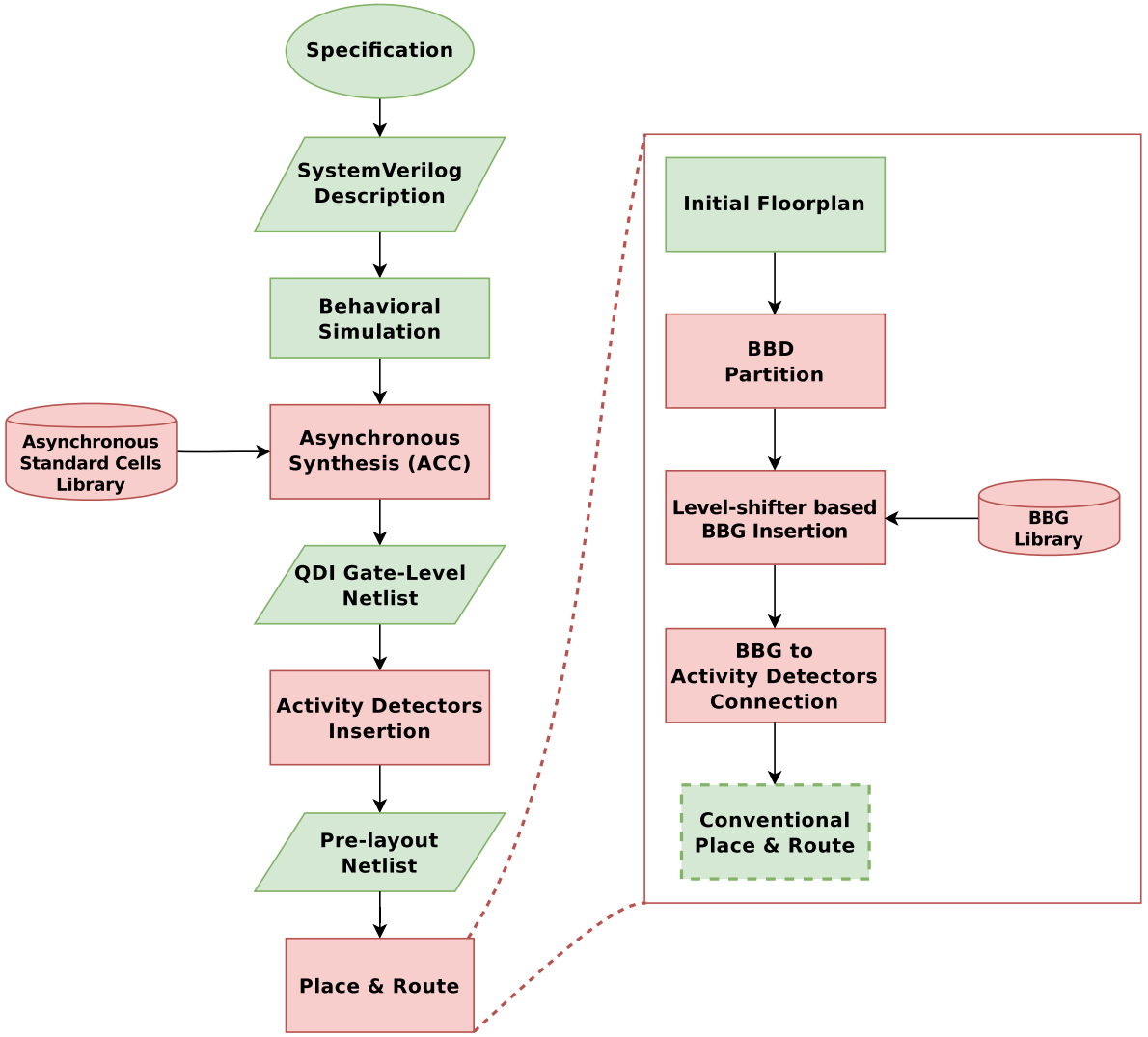


Fig. 7.1: Proposed standard-cell based IC design flow implementing multiple BBDs in QDI asynchronous circuits. The red rectangles represent the steps that have been modified from or inserted in a standard IC design flow.

7.1.1 System description, simulation and asynchronous synthesis

The first steps, as in a standard IC design flow, is specifying and modeling the target system in a hardware description language. These steps are represented in Fig. 7.1 by the Specification ellipse and the square right below it. This part of the proposed design flow have been done by our partner Tiempo Secure [124]. The asynchronous system model is written on a Transaction Level Model (TLM), by using the standard IEEE-1800 SystemVerilog language. This format provides a direct compatibility with the standard verification platforms of the main EDA vendors, thus allowing the designers to use any required debug tool to solve the probable design mistakes. The following behavioral simulation, depicted in Fig. 7.1, ensures that the generated SystemVerilog model corresponds to the system specification. It is exactly done as a standard IC design flow, with conventional simulation tools.

Once the hardware description is considered to be functionally correct, it is converted in a gate-level netlist, the step represented by the Asynchronous Synthesis square. However, as the

SystemVerilog code describes an asynchronous circuit, the conventional tools are not qualified for synthesizing it. Such synthesis tools are deeply optimized for the synchronous architectures, but are insufficiently effective for synthesizing QDI asynchronous designs. Therefore, the synthesis step of the proposed design flow is based on a specific synthesis tool called ACC developed by Tiempo Secure. It performs fully-automated synthesis of QDI asynchronous circuits starting from a standard SystemVerilog hardware description [166]. Fig. 7.2 shows ACC main output (the verilog gate-level netlist) and the auxiliary output files (area, timing reports and SDC constraints) that enable its interoperability with commercial CAD tools.

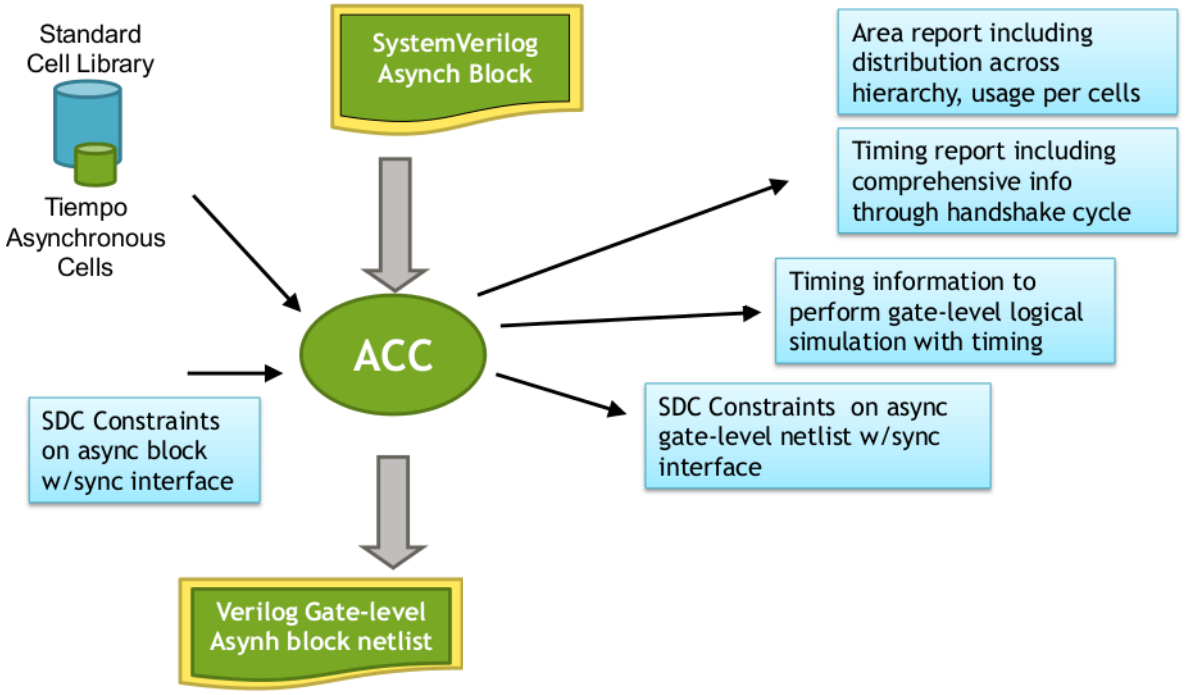


Fig. 7.2: Required inputs of ACC synthesis tool and generated output files. Adapted from [166].

To properly implement the data encoding and communication protocol required by QDI circuits, as described in chapter 3, a library of asynchronous standard-cells is provided to ACC. The input standard design constraint (SDC) file shown in Fig. 7.2 describes not only conventional specifications for the target netlist, but notably constraints for the handshake protocol signals.

7.1.2 Activity detectors insertion

Once the gate-level netlist has been generated, the activity detection circuitry is inserted. This step of the flow is represented in Fig. 7.1 by the "Activity Detection Insertion" rectangle. As explained in chapter 5, changing from high-performance to low-power mode and vice-versa during circuit operations, the basic principle of ABB, requires detecting the target system activity. In QDI asynchronous circuits specifically, the acknowledgment signals are used for this purpose. The choice of activity detectors depends on the implemented strategy, as discussed in chapter 5. Fig. 7.3 depicts how a part of the gate-level netlist is modified to insert an activity detector for implementing a fine-grain ABB strategy. In this case, as discussed in the chapter 5, the activity detector is a simple nand gate, depicted in red in Fig. 7.3. The choice of circuitry to

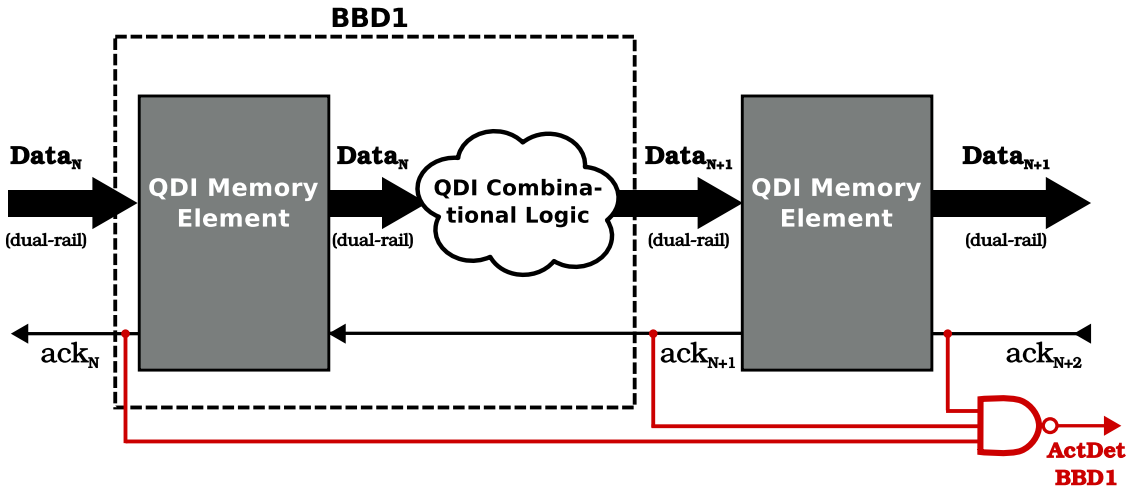


Fig. 7.3: Inserting an activity detector (NAND gate) for monitoring BBD1. The red gate and nets correspond to the modifications done to the QDI gate-level netlist.

be used as an activity detector depends on the chosen ABB strategy, as described in chapter 5. The output of the activity detector (*ActDetBBD1*) is let floating at this point of the flow as it will be the input of a BBG, which has not yet been inserted into the netlist.

7.1.3 Place & Route strategies

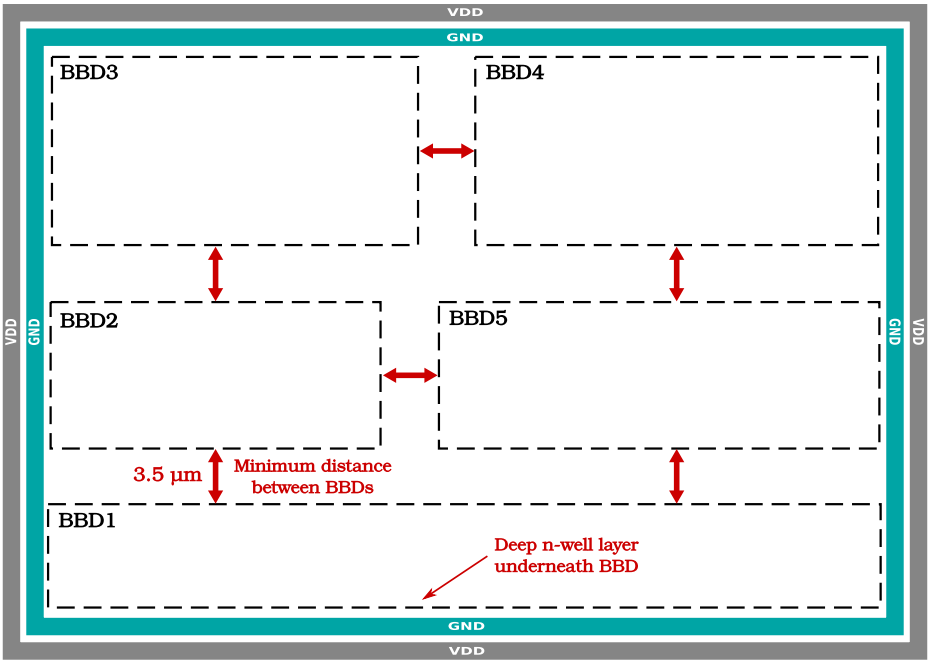
At this point of the flow, the gate-level netlist is ready to be placed and routed.

7.1.3.1 Body biasing domain partitioning

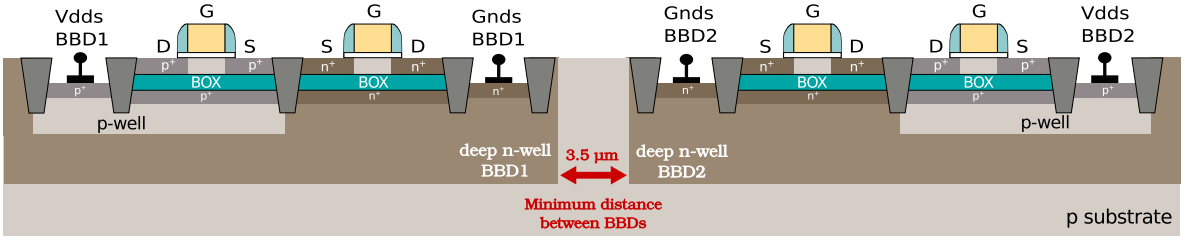
The core area, defined in the initial floorplan, is split into several BBDs according to the specified ABB strategy. At this point of the flow, all the standard-cells that compose the IC gate-level netlist are assigned to a BBD according to the previously defined strategy. Fig. 7.4a shows an example of the partition of a floorplan into five BBDs. The size of each BBD, delimited by the dashed rectangles in Fig. 7.4a, varies with the number of standard-cells composing each BBD. Thus, the area of each BBD depend on the chosen ABB strategy, as explained in chapter 5, and it does not need to be equal to the area of the other BBDs, as shown in Fig. 7.4a and previously in Fig. 5.2. The dashed rectangles in Fig. 7.4a also represent the layer of deep n-well that needs to be added underneath all the standard-cells composing each BBD. This extra layer electrically isolates the p-well and n-well of the standard-cells that compose each BBD (as depicted in Fig. 7.4b), thus guaranteeing the application of different V_{bb} to each BBD.

7.1.3.2 Level shifter based BBG insertion

Once the BBDs have been delimited in the core area, each of them will receive the appropriated level-shifter based BBG. The criteria for choosing the sizing of BBGs to be placed in each BBD is similar to the dimensioning procedure done in chapter 6. In fact, achieving a higher energy efficiency with ABB requires BBGs with low latency, capable of rapidly switching from low-leakage to high-performance mode and vice versa. Additionally, they need to have very low leakage, in order to minimize the power overhead due to inserting extra circuitry. Moreover, the



(a)



(b)

Fig. 7.4: Partition of the core (area surrounded by the GND and VDD rings) into BBDs (a). The required minimum distance between adjacent BBDs is highlighted in a cross section of transistors that belong to different BBDs (b)

BBGs need to properly function at low V_{dd}, the operation region in which minimum energy is reachable. These constraints need to be taken into account by the designers in order to define the optimal BBG for the defined ABB strategy. For instance, if the BBG chosen for a specific BBD is very large, it will have a very small latency, thus quickly switching from high-performance to low-leakage mode and vice versa. However, the drawbacks of this choice are high area and power overheads. On the other hand, considering the same BBD area, a smaller BBG reduce the power and area overheads at the cost of a higher latency, which risks to diminish the energy efficiency gains of implementing an ABB scheme, as shown in chapter 5.

Taking the aforementioned considerations into account, the necessary BBGs for each BBD is selected from the BBG library that has been developed by our research group, shown in Fig. 7.1. The base architecture of each cell has been analyzed in details in chapter 6. In the proposed design flow, multiple BBGs are placed in each BBD to guarantee a better distribution of V_{bb}, as depicted in Fig. 7.5. The *Vdds* and *Gnds* power nets are interconnected within each BBD to uniform the body biasing distribution inside each BBD and to guarantee that switching

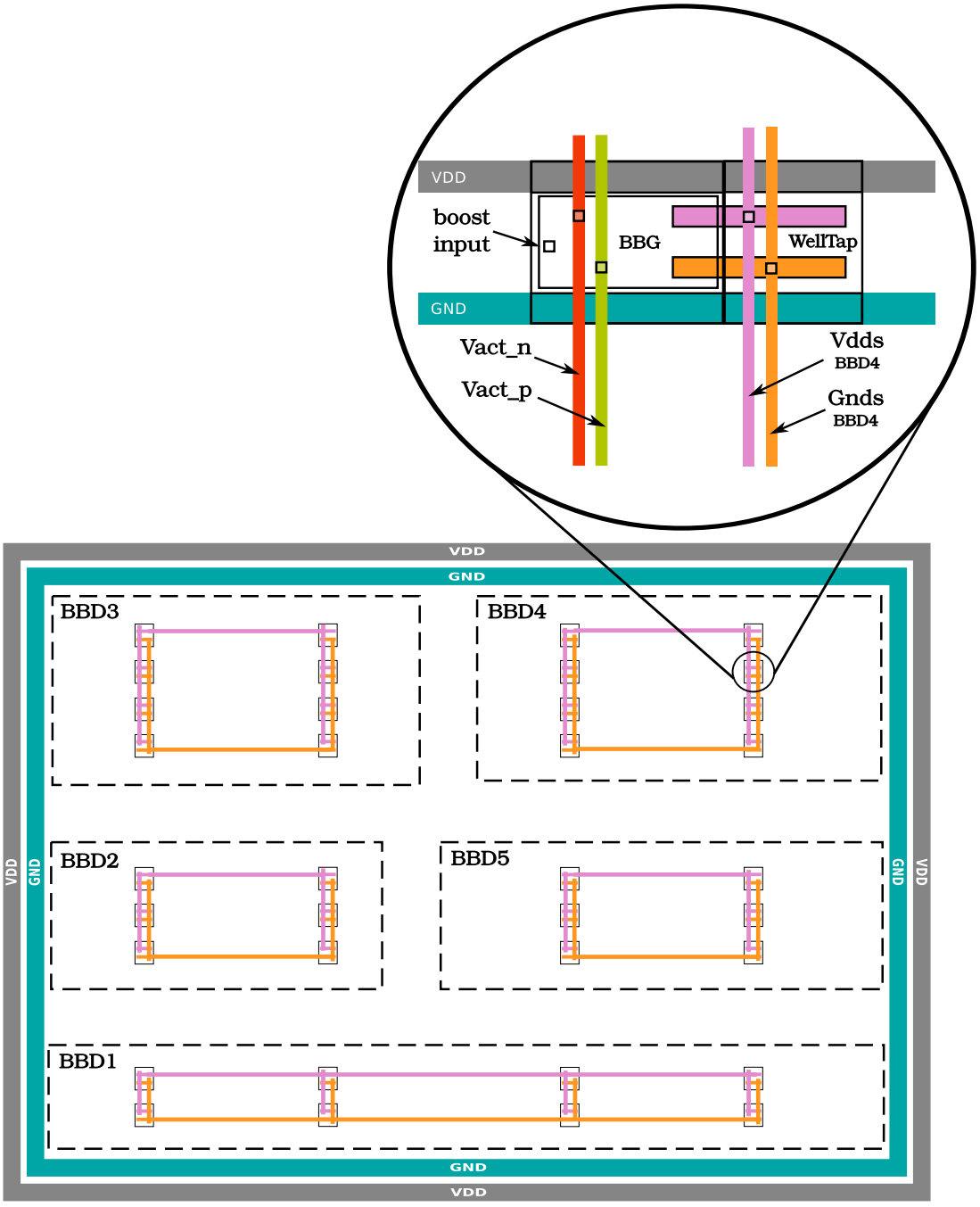


Fig. 7.5: Distribution of BBGs in each BBD. The *Vdds* and *Gnds* - outputs of the BBGs - are connected through well taps to the PMOS and NMOS body of transistors belonging to the same BBD respectively. $V_{\text{act\_n}}$ and $V_{\text{act\_p}}$, shown in the zoom, are input power nets common to every BBG, therefore they are the same for all BBDs.

between high-performance and low-leakage modes is done even if one BBG fails.

The BBGs need to be connected to their necessary power input nets. As shown in chapter 6, besides V_{dd} and Gnd, these special cells have two supplementary power nets: $V_{\text{act\_n}}$ and $V_{\text{act\_p}}$. They are created during the initial floorplan as power stripes covering all the core area. Therefore, the placement of every BBG in all BBDs needs to be aligned with the $V_{\text{act\_n}}$ and $V_{\text{act\_p}}$,

as shown in the zoom of Fig. 7.5. The correct alignment optimizes the metal use consequently reducing the routing effort, since there is less metal wires placed in the core area before the routing begins.

In the FD-SOI technology, the connection with n-well and p-well is done through a standard-cell called well taps, shown in the zoom circle of Fig. 7.5. To simplify the connection and minimize the area overhead, the well taps are placed right beside each BBG, as depicted in the referred figure. To finalize this step of the proposed design flow, the output of the activity detectors (*ActDet BBD1* in Fig. 7.3) are connected to the input (boost in Fig. 7.5) of the BBGs of each BBD by using the engineering change order (ECO) commands, available in any place&route tool. The following placing and routing steps are equivalent to the ones of a standard IC design flow, with the only restriction of placing the standard-cells that has been assigned to a specific BBD in the partition step into its rightful place.

7.2 Validating the proposed IC design flow

To validate the proposed design flow, a testchip was designed and fabricated in FD-SOI 28 nm technology in collaboration with Tiempo Secure and STMicroelectronics. In fact, manufacturing a prototype has also allowed validating the proposed BBG architecture described in chapter 6 and evaluating the ABB strategies analyzed in chapter 5.

7.2.1 The testchip

The main architecture, shown in Fig. 7.6, is composed of six IPs (TIEMPO ASYNC 1, TIMA ASYNC 1, TIMA ASYNC coarse, TIMA ASYNC medium, TIMA ASYNC fine, and TIMA SYNC 4) connected to each other through an asynchronous communication network called Asynchronous Link (ASL), represented in green in Fig. 7.6. It is described with more details in the sequel. In order to enable a more standard access interface, similar to what is used in industrial silicon test equipments, an IEEE 1149.3 JTAG interface has been added. Since internally all the IPs are interconnected through the ASL network, the block JTAG2ASL has been added

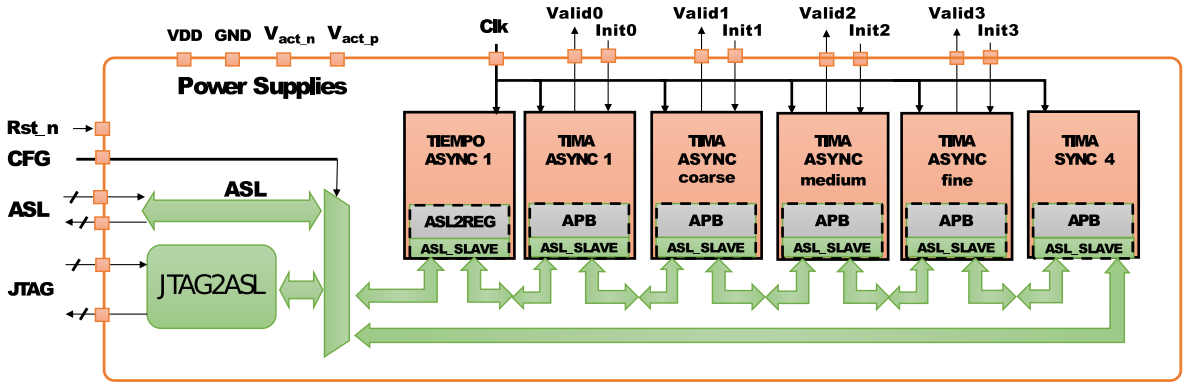


Fig. 7.6: High-level abstraction of the testchip architecture. The blocks and arrows in green belong to the Asynchronous link (ASL) and the salmon rectangles represent the IPs embedded in the testchip.

to convert the JTAG format to the asynchronous communication protocol implemented by the ASL and vice-versa. A selection input (CFG) allows selecting which protocol will be used to access the IPs: ASL or JTAG.

The analyses carried out in this chapter is focused on the IPs developed in the context of this thesis: TIMA ASYNC coarse, TIMA ASYNC medium, TIMA ASYNC fine. They were designed following the steps described in section 7.1. The other three IPs (TIEMPO ASYNC 1, TIMA ASYNC 1 and TIMA SYNC 4) were developed by partners of the project for their on use and will not be discussed in this work.

7.2.1.1 The interconnection between IPs: the ASL

The ASL is a PVT variation tolerant communication network developed by Tiempo Secure. By using QDI logic, the ASL implements a delay insensitive single bit asynchronous serial protocol, called ASPIC, greatly simplifying the complex timing constraints required by signals crossing physical and voltage domains [123].

A crucial feature of the ASL network is its plug and play characteristics. Independently of the physical position in the die, controlling and accessing each IP is done by simply integrating the ASL_SLAVE block, shown in Fig. 7.6. This is enabled by the following technical reasons: 1) the ASL is asynchronous, so there is no clock distribution issues or clock domain crossing at the chip top level; 2) the ASL is delay insensitive, so there is no timing constraint to be considered during placement of its constituting blocks or routing of its interconnects; 3) the IPs are connected to the ASL through a standard APB interface, grey boxes in Fig. 7.6, which enables the designers to re-use the ASL infrastructure with other IPs that communicate with this widely used interface [123].

7.2.1.2 Testing ABB strategies: the TIMA ASYNC IPs

A high level representation of the TIMA ASYNC IPs is depicted in Fig 7.7. The three blocks represented in the lower part of the figure (LFSR, ABB ALU Chain and Performance Measurement) are the main part of the IPs. The LFSR and ABB ALU Chain are the same circuitry previously described in chapter 5. The LFSR generates pseudo-random inputs to the ALU chain,

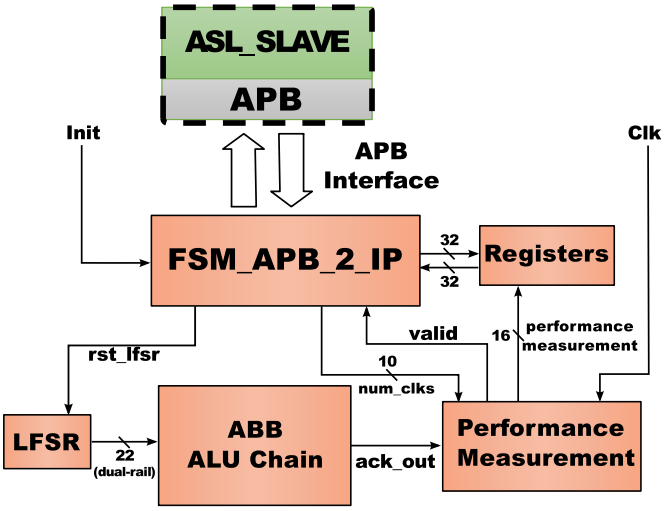


Fig. 7.7: Architecture of the TIMA ASYNC IPs.

and the Performance Measurement block, as its name suggests, is an on-chip performance measurement circuitry, added to simplify the post-silicon test procedure. It counts the number of output acknowledgment signals (*ack_out*) generated by the ALU chain in a reference time window, which is defined by the reconfigurable value *num_clks* and the frequency of the reference clock (*Clk* in Fig 7.7).The output measurements are stored in registers, depicted in Fig 7.7, that holds the historic of ten performance measurements.

Both LFSR and Performance Measurement blocks are exactly the same in the three TIMA ASYNC IPs represented in Fig. 7.6. The ABB ALU Chain, however, varies from IP to IP as described in the section 5.3.1 of chapter 5. They have the same chain of five ALUs, which are exactly the same in all the IPs, but each TIMA ASYNC IP implements a different ABB strategy: in TIMA ASYNC coarse the ABB ALU Chain has a coarse-grain ABB strategy, in which all the ALUs belong to the same BBD (as shown in Fig 5.2b); in TIMA ASYNC fine it has a fine-grain strategy, with 1 BBD per pipeline stage of each ALU, summing a total of 15 BBDs (the strategy depicted in Fig 5.2a); and in TIMA ASYNC medium it has a medium-grain ABB strategy, in which each ALU of the chain belongs to a separate BBD, summing a total of 5 BBDs (the strategy shown in Fig. 5.2c).

In order to interface the main part of the TIMA ASYNC IPs with the ASL network, a synchronous finite state machine (FSM_APB_2_IP in Fig 7.7) has been added to the IPs. It controls the start/stop of the LFSR according to the predefined measurement time window; configures the Performance Measurement block; and manage the read and write operations of the registers. Three operation modes have been configured to enable the measurement of performance and power consumption. The first one is the idle mode. As its name suggest, in this mode of operation the IPs do not perform any calculation. This mode is crucial for avoiding interference of one IP over the others, especially when measuring power consumption. Whenever the testchip is reset, all the IPs are set to idle mode until the FSM of each IP receives a command from the APB interface. As soon as an IP goes out of the two other operation modes, it is immediately set back to idle.

The second operation mode, called "single measurement mode", is used for producing a single performance measurement, which is then stored in the registers block. In this operation mode, the ALU Chain processes the inputs generated by the LFSR during the pre-configured measurement time window. In other words, the performance measurement block counts the number of *ack_out* cycles generated before reaching *num_clks* reference *Clk* cycles, which is indicated by the valid signal. The number of counted *ack_outs* is then stored in the registers block as one performance measurement.

The other operation mode that has been designed is called "continuous operation" and is used for measuring the average power consumption of each IP. In this operation mode, the ALU Chain processes the inputs generated by the LFSR continuously, independently of the pre-configured measurement time window. In order to avoid the interference of other IPs, this mode has to be set to only one TIMA ASYNC IP at a time. Therefore, considering that the target IP is the only one functioning while it is in continuous operation mode, its average power consumption is measured directly from the testchip power supply pads (VDD and GND in Fig. 7.6). In this operation mode, the valid signal stays low and no measurement is stored in the registers. The FSM only goes back to idle mode if it detects an edge (positive or negative) of the *init* signal.

7.3 Circuit testing and preliminary results

The designed layout of the testchip is shown in Fig. 7.8. The fabricated die size is approximately 1.5 mm^2. Table 7.1 shows the number of BBGs and the area overhead required to implement the three ABB strategies in the TIMA ASYNC IPs. The Reference IP in table 7.1 was added as a base for comparing the extra area requirements of each IP. In fact, the Reference IP has not been added to the testchip. It is an hypothetical circuit exactly equal to the other TIMA ASYNC IPs in terms of datapath, but with no ABB strategy implemented. Therefore there is no BBG, nor activity detection circuitry added, thus the area required for placing it is smaller. Moreover, no minimum space between BBDs is considered since there are no BBDs in this reference circuit.

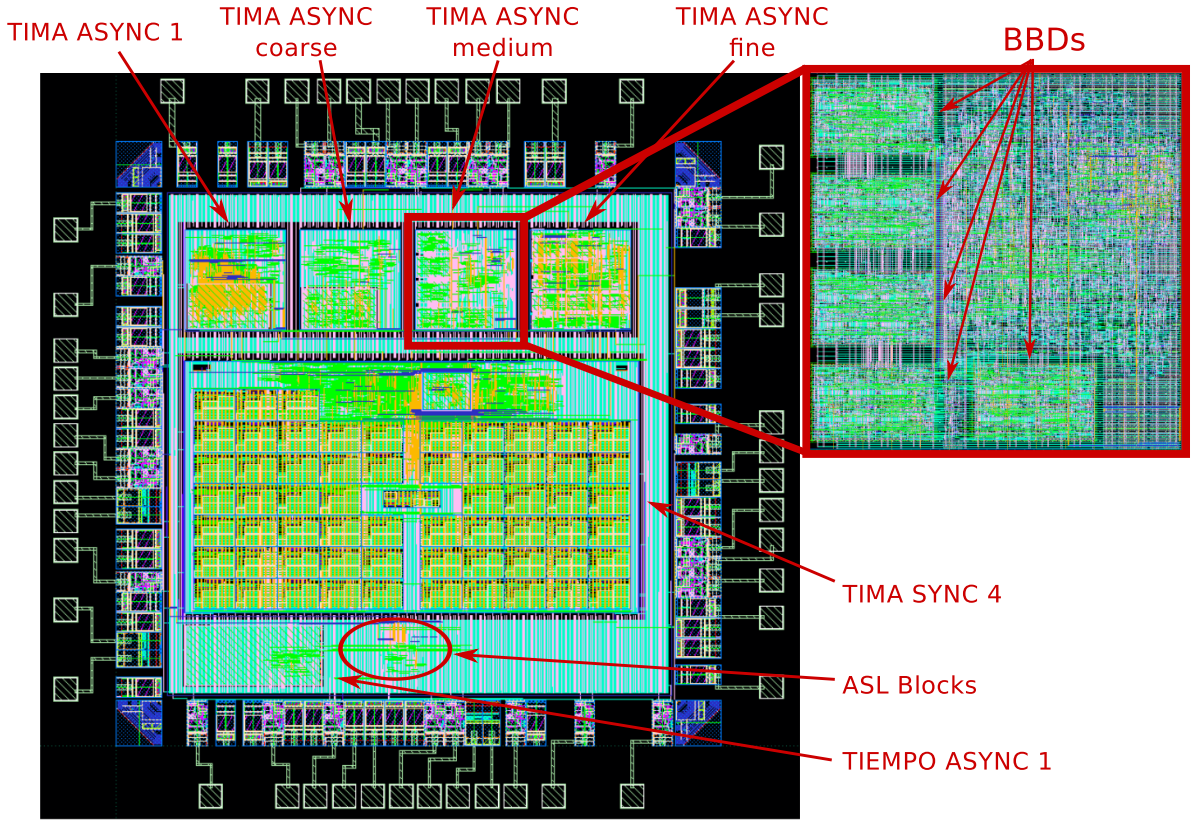


Fig. 7.8: Testchip top layout.

Table 7.1: Area overhead and number of BBGs required to implement coarse, medium and fine grain ABB strategies.

IP name	ABB strategy	number of BBDs	BBGs per BBD (min - max)	Total number of BBGs	Area Overhead (%)
TIMA ASYNC coarse	coarse	1	24-24	24	37.64
TIMA ASYNC medium	medium	5	6-6	30	59.55
TIMA ASYNC fine	fine	15	1-3	30	86.32
Reference	none	0	0-0	0	0.00

As the number of BBDs increase, more empty spaces need to be added to the final IP area to avoid violations of the minimal space between BBDs. The result is a considerable increase in the area overhead comparing to the Reference IP. For instance, increasing the number of BBD

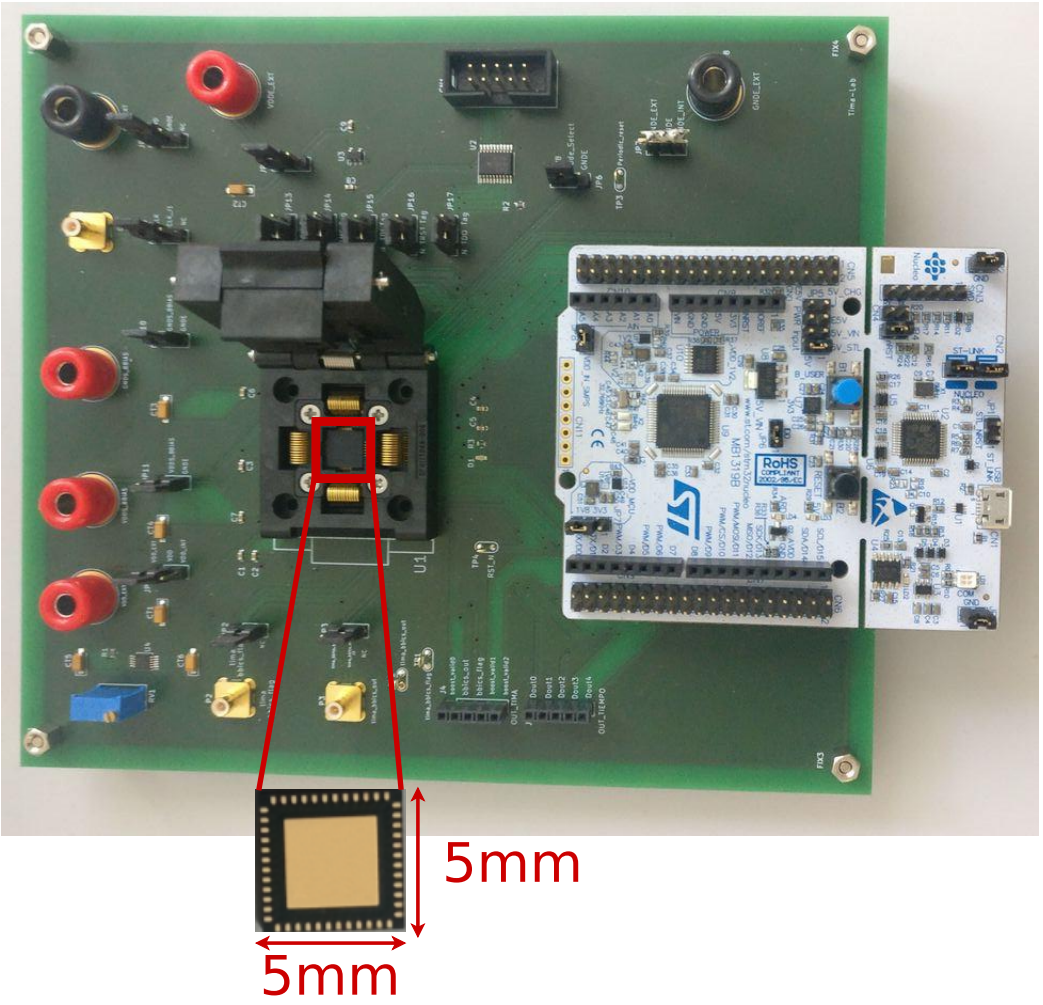


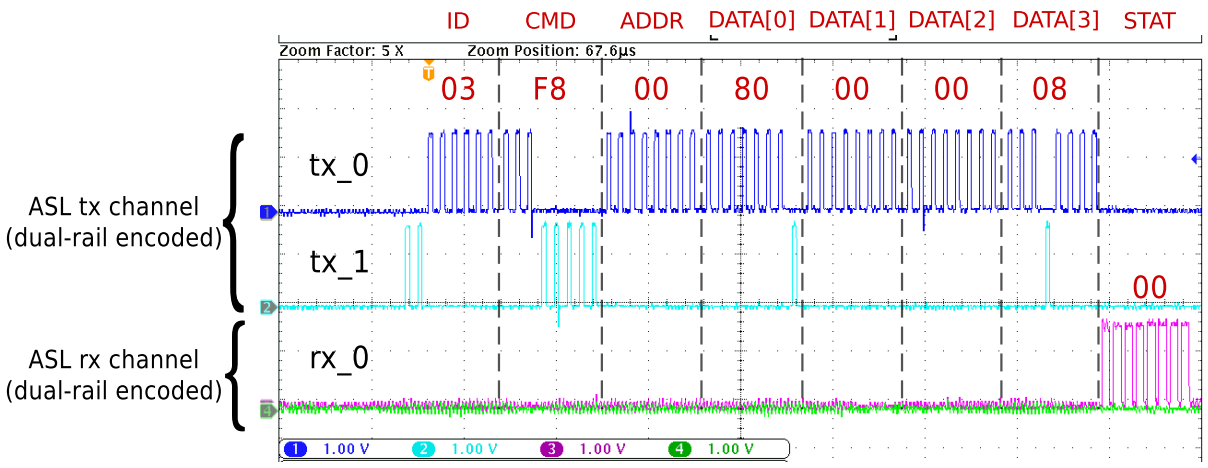
Fig. 7.9: Printed circuit board developed to simplify the testing of the testchip. It is connected to the ST32 Nucleo (white board on the left). A zoom into the socket shows the back face of the testchip and the dimensions of the packaging.

from 5 to 15 increases the total area overhead in 26.77% (difference between area overheads of TIMA ASYNC medium and fine), as depicted in table 7.1.

In order to simplify the test of the prototype, a printed circuits board (green board in Fig. 7.9) has been designed. It integrates all necessary resources to run the validation routines: power supplies connectors, potentiometers to vary the voltage supplied to the testchip, switches to drive the input ports, pins or LEDs to monitor the output ports, and a socket to place the testchip. Moreover, a ST32 Nucleo (white board in Fig. 7.9) has been added to the testing environment to allow a quick creation of test routines implementing the ASPIC communication protocol and/or the JTAG standard.

7.3.1 Accessing the TIMA ASYNC IPs

Before testing the designed IPs themselves, it is necessary to certify that they are being accessed correctly through the ASL interface. Therefore, write and read operations to the registers of each TIMA ASYNC IP has been executed in the first test campaign. The result of this test is



(a)

ID	Target IP
CMD	Nature of the operation (read/write, byte enable)
ADDR	Address inside IP
DATA	Payload (to be written into IP)
STAT	Status of the operation (succes = 0 or error = 1)

(b)

Fig. 7.10: Oscilloscope waveform of dual-rail encoded tx and rx channels of the ASL interface (a). The meaning of each byte necessary for composing a write operation is presented in (b). The numbers in red are the hexadecimal representation of each dual-rail byte.

shown by the oscilloscope waveforms of the ASL tx and rx channels in Fig. 7.10a. It shows two dual-rail encoded signals: the dark blue and light blue waveforms are the signals *tx_0* and *tx_1*, respectively, which represent the serial input channel of the ASL interface. The pink and green waveforms are the signals *rx_0* and *rx_1*, that represent the serial output channel of the ASL interface. At first, 7 bytes are sent through the tx channel respecting a 4-phase dual rail protocol. To simplify the understanding of the obtained waveform, a table describing the information carried by each byte is shown in Fig. 7.10b. Therefore, interpreting the hexadecimal numbers of Fig. 7.10a, the presented waveform corresponds to a write operation (F8) to the register 0 of the TIMA ASYNC coarse IP, which received the ID 03 in the top architecture. Four bytes have been written to this address: 80, 00, 00, and 08. The target IP then responds through the rx channel with a zero byte, indicating that no error occurred during the write operation, thus DATA has been successfully stored in the TIMA ASYNC coarse IP. An explanation with further details of the ASPIC protocol is done in [123].

Correctly writing into the registers of each IP is crucial since it allows selecting the operation mode of each IP. For instance in the aforementioned writing test, the payload written to the

configuration register (address 0) of the target IP configures the TIMA ASYNC coarse IP to operate in single measurement mode for a time window of 8 reference *Clk* cycles. The writing test shown in Fig. 7.10 has been repeated for IPs TIMA ASYNC medium and fine, followed by a read operation of the same register address of each IP. Executing a read operation through the ASL interface also allows verifying if the written value has been correctly stored in the specified register. It is similar to the write operation, the only differences being: 1) After sending the ID byte, followed by CMD and ADDR, no DATA bytes are send through the tx channel; 2) the target IP responds through the rx channel with the STAT byte, followed by four DATA bytes that corresponds to the value stored in the requested register.

At the end of this preliminary write/read test campaign, no read nor write operation problems were detected, thus all the TIMA ASYNC IPs were considered fully accessible.

7.3.2 Testing the TIMA ASYNC IPs: evaluating ABB strategies

Assessing the effectiveness of ABB strategies requires measuring both performance and power consumption. To measure performance, the IPs need to be configured to single measurement mode, as described in section 7.2.1.2. This is done by writing the value 0x80000008 to the configuration register (ADDR 0). After the defined measurement time window, the performance result is stored in the IP output register (ADDR 1). A subsequent reading of the register ADDR 1 allows obtaining the measured performance. This procedure was repeated for all the TIMA ASYNC IPs operating at V_{dd} = 0.6 V and activity ratio of 1. The obtained results are depicted in table 7.2.

The activity ratio is a parameter that represents the proportion between active interval (Δt_{BB}) and the following idle period (Δt_{noBB}), previously used in the analysis of chapter 5. The values stored in the output registers of the three TIMA ASYNC IPs are shown in the Perf. measurement column. These values were obtained with a reference clock of 14.27 MHz (directly available in the Nucleo board) and a *num_clks* of 8. This means that, in a time window of 560.62 ns ($8 * T_{Clk}$), the ALU chain of IP TIMA ASYNC coarse has successfully generated 55 outputs when operating at V_{dd} = 0.6 V and V_{bb} = 0 V. Knowing the frequency of *Clk* and the performance measurement value read from the registers of each IP, the average frequency of operation is easily calculated. Table 7.2 also shows the results of simulation obtained at the same operation conditions: V_{dd} = 0.6 V and activity ratio of 1.

The obtained simulation values are coherent with the testchip measurements. In both cases the TIMA ASYNC coarse IP has the highest average frequency, a result explained by the lower latency in the body biasing activation of each BBD in this ABB strategy. As demonstrated by the simulation experiments of chapter 5, in a coarse-grain ABB strategy, all the system

Table 7.2: Testchip results of performance measurement compared with simulation at a V_{dd} = 0.6 V and activity ratio of 1.

IP name	Vbb (V)	Perf. measurement (# of *ack_outs*)	Measured average frequency (MHz)	Simulated average frequency (MHz)
TIMA ASYNC coarse	0.0	55	98.10	134.97
	1.0	93	165.88	227.34
TIMA ASYNC medium	0.0	54	96.30	125.87
	1.0	90	160.53	218.95
TIMA ASYNC fine	0.0	50	89.18	118.33
	1.0	84	149.82	215.21

pipeline stages are switched to high performance mode as soon as the first input arrives at the first stage, and the whole system only changes back to low leakage mode once the pipeline is completely empty. Since the complete system stays in high performance mode for a longer time, coarse-grain ABB strategy has slightly better performance. Analyzing the impact of the ABB, applying V_{bb} = 1 V in the testchip causes a performance boost of approximately 69% in the TIMA ASYNC coarse IP compared to applying a V_{bb} = 0 V. Additionally, there are performance reductions between 26% and 30% in the testchip obtained results if compared to their corresponding simulation values. An inadvertent reset issue on the FSM design of the testchip impedes the variation of the activity ratio. Thus, the results shown in table 7.2 corresponds to an activity scenario in which a coarse ABB strategy is favorable.

Table 7.3 shows the measured average power consumption of each IP compared to the simulation results considering the same operation conditions: V_{dd} = 0.6 V and activity ratio of 1. As described in section 7.2.1.2, in order to obtain such results, each IP is configured to operate in continuous mode, which forces the activity in the ALU chain to be constant, a scenario suitable to perform power consumption measurements on the testchip. This is done by writing the value 0xC0000008 to the register ADDR 0. Before each measurement, the testchip is reseted to guarantee that all the other IPs enter in idle mode. The average power consumption of each IP is then measured from the voltage source that provides V_{dd} to the testchip core by using a hall-effect probe.

Table 7.3: Testchip results of average power consumption compared with simulation at a V_{dd} = 0.6 V and activity ratio of 1.

IP name	Vbb (V)	Measured power consumption (mW)	Simulated power consumption (mW)
TIMA ASYNC coarse	0.0	1.30	1.08
	1.0	2.00	2.08
TIMA ASYNC medium	0.0	0.90	1.05
	1.0	2.00	2.02
TIMA ASYNC fine	0.0	1.20	0.70
	1.0	2.10	2.11

At such a high activity ratio, the average power consumption of fine, medium and coarse grain ABB strategies are very similar. In fact, is has been demonstrated in chapter 5 that a high activity ratio is a favorable case for implementing coarse-grain ABB strategies, an affirmation consistent with the obtained testchip measurements. At a V_{bb} = 1 V, the TIMA ASYNC coarse IP consumes approximately 5% less power than the TIMA ASYNC fine IP. The obtained simulation results follow the same tendency.

Although the inadvertent reset issue on the testchip FSM impedes a proper control of the activity ratio, the similarity between simulation results and testchip measurements - shown in tables 7.2 and 7.3 - demonstrates the consistence of the obtained measured values and consequently validates the implemented IP architectures. Therefore, the testchip behavior at lower activity ratios is also expected to be similar to the simulation results, shown in chapter 5.

Finally, more experiments still need to be performed at V_{dd} = 1.0 V. At this operation condition, the obtained performance measurements of the TIMA ASYNC medium IP is approximately two times higher than the results obtained with the TIMA ASYNC coarse IP, even with V_{bb} = 0 V, a scenario in which the performances of all IPs should be very similar. The causes for this unexpected behavior need to be further investigated. Some possible reasons are: the

activity detection circuitry is not responding fast enough; or the level shifter based BBGs are not properly functioning at V_{dd} = 1.0 V. Nevertheless, further tests and investigation need to be done with the testchip operating at V_{dd} = 1.0 V before driving concrete conclusions.

7.4 Conclusion

In this chapter, a standard-cell based IC design flow has been proposed. It has been designed to exploit the body-biasing features of the FD-SOI technology and the locality of data synchronization of asynchronous circuits to implement more energy efficient ABB systems, from the initial specification until the final layout. The proposed flow integrates the level shifter based BBG architecture presented in chapter 6 to build asynchronous systems with multiple BBDs. The proposed IC flow has been afterwards validated with the design and fabrication of a testchip in FD-SOI 28 nm technology. The preliminary results obtained with the measurements of the testchip have demonstrated the efficacy of the BBG architecture; the advantages of implementing ABB strategies, especially if operating at low V_{dd}; and, finally, have validated the proposed standard-cell based IC design flow. Further tests on the testchip operating on nominal V_{dd} are still required to complete the study showing the efficacy of the BBGs and the advantages of using ABB strategies in asynchronous circuits.

Chapter 8

Conclusions and Perspectives

Keeping the fast evolving pace of electronic portable devices require reducing power consumption without compromising the circuit performance or robustness. QDI asynchronous circuits have demonstrated to be an excellent solution to accomplish the high energy efficiency required in the IoT era. Their local synchronization makes them the perfect fit for fully exploiting dynamic power management techniques, such as ABB, in an advanced technology such as the FD-SOI. The circuit activity is directly detected by using the already existing handshake signals, enabling the application of different ABB strategies with almost no modification to the original QDI asynchronous architecture. Additionally, the timing properties of QDI circuits are very well-suited for changing transistors V_{th} on-the-fly, a requirement for applying ABB schemes.

We detailed in this thesis all the necessary steps for understanding a complete design - from specification to final layout - of QDI asynchronous circuits, fully exploiting body biasing features of FD-SOI technologies by implementing ABB schemes with multiple BBDs. The chapter 2 presents the fundamentals of UTBB FD-SOI technology, one of the candidates to enable the scale down in the deep sub-micron era. It has been compared to the conventional bulk, showing the main manufacturing innovations that make FD-SOI technologies an interesting alternative for nodes beyond 32 nm. The benefits of body biasing and its extended voltage range is emphasized in this chapter since it is the FD-SOI key factor used in this thesis, opening new perspectives for performance boosting and static power reduction.

Another crucial element for fully understanding the contributions of this thesis is the concept of asynchronous circuits, presented in chapter 3. In these circuits, a local communication protocol synchronizes data transfers between blocks instead of a global clock signal. The advantages of asynchronous circuits compared to their synchronous counterpart is highlighted, illustrating the facility to include power management techniques in order to achieve higher robustness and energy efficiency.

Chapter 4 compares a QDI asynchronous 8-bit ALU architecture with a synchronous counterpart, both designed in FD-SOI 28 nm technology. The behavior of these circuits at very low operation voltages was analyzed, showing that the asynchronous approach intrinsically made the designed ALU more energy efficient than its synchronous counterpart. This study also demonstrated that the QDI ALU has its minimum energy point at a lower V_{dd} and it is intrinsically more robust to power and voltage variations and thus more suitable for applications requiring high reliability and security. Results show the QDI asynchronous ALU capacity of operating in a wide V_{dd} range with no need for extra circuitry, unlike its synchronous counterpart.

In the sequel, chapter 5 analyzes the energy efficiency and performance gains of three dif-

ferent adaptive body biasing strategies on asynchronous circuits. This study investigates the optimum granularity for applying ABB with different BBD configurations in QDI asynchronous circuits. Results show that ABB strategies allow maintaining the performance gains featured by body biasing while reducing the power consumption increase by approximately 35%. Therefore, lower energy per operation is achieved by applying ABB strategies, especially if the target system is partitioned into small BBDs (the fine-grain strategy). Moreover, a methodology is presented to analyze the energy efficiency of ABB strategies, which allows delimiting the activity ratios in which implementing each strategy is feasible.

In chapter 6, we devise a novel body built-in cell for enabling the application of ABB strategies. The performed experiments show that the proposed cell is capable of function as a BBG, efficiently applying ABB schemes with a wide biasing range. The cell has a very stable operation for input signal voltage variations between 0.4 V and 1.0 V when simulated with target systems in FD-SOI 28-nm technology. Additionally, it is capable of detecting short-duration (20 ps fall time) and long-duration (700 ps fall time) transient faults caused by radiation exposure or environmental perturbations, even under temperature and process variation, improving the system resilience against environmental effects. The proposed cell is an essential building block for the successful implementation of ABB strategies in asynchronous circuits.

Finally, chapter 7 proposes a standard-cell based IC design flow, necessary for designing QDI asynchronous systems including ABB schemes with multiple BBDs. It exploits the body-biasing features of FD-SOI technologies and the locality of data synchronization of asynchronous circuits to generate more energy efficient ABB systems, from the initial specification until the final layout. The proposed flow merges the contributions explored in chapters 5 and 6. Moreover, a testchip has been designed and fabricated in FD-SOI 28 nm technology in order to validate the IC flow and body built-in cell. The preliminary results obtained with the measurements of the testchip demonstrate the efficacy of the BBG cells, and the advantages of applying ABB strategies in QDI asynchronous circuits, especially if operating at low V_{dd}.

Having the automated IC design flow (chapter 7); the level-shifter based BBG (chapter 6); and the knowledge of how to include ABB strategies in QDI asynchronous circuits (chapter 5), IC designers have all the necessary tools to build more energy efficient systems in FD-SOI technologies.

In order to further optimize the obtained results, additional experiments and optimizations are still required:

1. In a near future, the BBG effectiveness and the advantages of using ABB strategies in asynchronous circuits will be completely validated by performing more experiments with the testchip at nominal V_{dd}, since further investigations are still needed at this operation point. Moreover, one of the IPs of the testchip (TIMA ASYNC 3) has not yet been assessed. We have inserted in this IP a circuitry to detect TFs occurring in a QDI asynchronous ALU chain with an ABB strategy. Evaluating the behavior of this IP under radiation exposure allows better understanding the impact of TFs to the system output and how ABB strategies influence the robustness of QDI asynchronous circuits, a topic not yet deeply investigated in the literature.

2. Optimizing the architecture of the level-shifter based BBG (proposed in chapter 6) allows further improving the energy and performance results presented in chapter 5. Reducing the BBGs latency enables a faster response to the activity detection, thus speeding-up the transition between high-performance to low-leakage mode and vice-versa. As a result:

- The energy savings during pipeline loading and unloading would considerably increase, especially with operations at low V_{dd}.
- The performance difference between fine-grain and coarse-grain ABB strategies (detailed in chapter 5 and observed in table 7.2), would be considerably reduced.

3. ABB strategies would be more energy efficient by setting BBDs with high activity to a fixed V_{bb}, independently of circuit activity. In fact, it has been demonstrated in chapter 5 the existence of an activity ratio above which implementing ABB strategies is not profitable. Identifying BBDs in which the activity is higher than this threshold allows:

   - Avoiding unnecessary energy consumption overheads necessary for implementing an ABB strategy (described in details in section 5.2);
   - Simplifying the final system layout by removing the design flow steps of activity detectors and BBG insertion for the selected BBDs.

Future works will also include adapting the proposed body-built in cell for detecting TFs that occur during body biasing, an operation scenario that needs to be studied in more details. Furthermore, considering that current sensors have been previously used for detecting hardware Trojans [53], future research will also include evaluating the use of the proposed cell for detecting hardware Trojans.

Considering the projections of exponential growth of the number of IoT devices and the consequent expectation of insufficient power to supply all the electronic devices [8, 132], it is crucial to find alternative solutions to overcome these issues. The results and conclusions of this thesis highlight the benefits of aligning asynchronous circuits with the ABB strategies for FD-SOI technologies, a very promising solution to build the next generation of high energy efficient systems of the deep sub-micron era.

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La technologie FD-SOI, une opportunité pour la conception de circuits asynchrones énergétiquement efficients

Cette thèse étudie de nouveaux dispositifs de gestion de l'énergie ainsi que leur mise en œuvre, en combinant deux approches: la logique asynchrone et les techniques de polarisation du substrat (Adaptive Body Biasing - ABB). Cette thèse comporte quatre contributions permettant la conception de circuits asynchrones énergétiquement plus efficaces. 1) Une unité arithmétique et logique (UAL) asynchrone quasi insensible aux délais (Quasi Delay Insensitive - QDI) a été conçue et utilisée pour mener une analyse comparative entre systèmes synchrones et asynchrones. Cette étude démontre notamment la meilleure efficacité énergétique et la plus grande robustesse des circuits asynchrones QDI, surtout lorsqu'ils fonctionnent à basse tension. 2) Une cellule standard a été spécialement développée pour mettre en œuvre nos schémas d'adaptation dynamique du substrat (ABB) qui ajustent la tension de seuil (Vth) des transistors. En outre, cette cellule s'est révélée très utile pour la détection de fautes transitoires causées par des radiations environnementales. Cette cellule est en outre un élément clé pour exploiter la polarisation du substrat, un des intérêts majeurs de la technologie FD-SOI, et d'améliorer la fiabilité du système. 3) Trois stratégies de polarisation de substrat ont été évaluées. Ces stratégies reposent sur la détection automatique de l'activité des circuits asynchrones QDI et de la polarisation de multiples domaines dans le substrat (Body Biasing Domains - BBD). De plus, une méthode pour analyser l'efficacité énergétique des stratégies de polarisation pour les circuits asynchrones QDI a également été proposée dans le cadre de cette thèse. 4) Enfin, un flot de conception de circuits numériques intégrés a été proposé et développé. Ce flot, basé sur des cellules standards, permet d'exploiter des stratégies de polarisation (ABB) avec plusieurs domaines (BBD).

Keywords: Circuits Asynchrones Quasi-Insensibles aux Délais, Polarisation Adaptative du Substrat, Efficacité Énergétique, FD-SOI

FD-SOI technology opportunities for more energy efficient asynchronous circuits

This thesis studies novel energy management schemes, and how to implement them, by using two main design approaches: asynchronous logic and adaptive body biasing (ABB) techniques. Four main contributions have been done, thus enabling the design of more energy efficient asynchronous circuits. 1) We contributed with the design of a Quasi-delay Insensitive (QDI) asynchronous ALU architecture, used in a comparative analysis of asynchronous versus synchronous systems. This first study has demonstrated the energy efficiency and robustness of QDI circuits, especially if operating at low power supply (V_{dd}). 2) We proposed a new body built-in cell for implementing ABB schemes by tuning the circuit threshold voltage (Vth) on-the-fly; and detecting short-duration and long-duration transient faults (TF) caused by environmental radiation. The proposed cell is a key building block to fully benefit from body biasing features of the FD-SOI technology while enhancing system's reliability. 3) We assessed three different ABB strategies - based on automatic activity detection and multiple body-biasing domains (BBDs) - for QDI asynchronous circuits. Furthermore, a methodology for analyzing energy efficiency of ABB strategies in QDI asynchronous circuits is also proposed in this work. 4) We developed a standard cell-based IC design flow to apply ABB strategies with multiple BBDs by using the proposed body built-in cells. A testchip has been designed and fabricated to validate the developed design flow and the efficacy of the body built-in cell.

Keywords: Quasi-delay-insensitive Asynchronous Circuits, Adaptive Body Biasing, Energy Efficiency, FD-SOI.