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# Exploration of carbon nanotube and copper-carbon nanotube composite for next generation on-chip energy efficient interconnect applications

Jie Liang

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**THÈSE POUR OBTENIR LE GRADE DE DOCTEUR  
DE L'UNIVERSITÉ DE MONTPELLIER**

**En Microélectronique**

**École doctorale : Information, Structures, Systèmes**

**Unité de recherche LIRMM**

**Exploration of Carbon Nanotube and  
Copper-Carbon Nanotube Composite for Next  
Generation On-chip Energy Efficient Interconnect  
Applications**

**Présentée par Jie LIANG**

**le 17 Juin 2019**

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**UNIVERSITÉ  
DE MONTPELLIER**



*I dedicate my dissertation work to my family and many friends. A special feeling of gratitude to my loving parents, whose words of encouragement and push for tenacity ring in my ears.*



# Résumé

Dans les sociétés modernes, le style de vie rapide et efficace nécessite un échange d'informations rapide, précis et sûr. Cette masse d'information est acquise par le biais de divers dispositifs reposant en grande majorité sur des réseaux électroniques complexes ainsi que sur Internet. La ville intelligente, l'Internet des objets (IoT) et l'intelligence artificielle des objets (AIoT) sont actuellement des tendances essentielles du développement technologique futur. L'informatique quantique et neuro-morphique à très grande vitesse laisse entrevoir la possibilité de reprendre les architectures de Von Neumann. Cependant, tous ces évolutions consomment une énorme quantité d'énergie. Satisfaire à la fois les hautes performances et les ultra-basses consommation est au centre des défis posés aux technologies de la prochaine génération. Afin de répondre à la demande en termes de quantité de données et d'efficacité énergétique, la miniaturisation des produits microélectroniques, plus précisément des transistors, couplée à une amélioration des fonctionnalités et un coût réduit, ouvre la possibilité de répondre aux demandes susmentionnées.

Cependant, l'amélioration seule des performances des transistors des prochaines générations de puce n'est pas suffisante. Malgré leurs importances, les puces en elles-mêmes ne représentent qu'une petite partie du très vaste et complexe puzzle de la technologie de l'information. Ainsi, pour façonner l'avenir du monde numérique, nous devons également examiner la situation dans son ensemble. Les performances des transistors ne valent que dans le système dans lesquels ils sont intégrés. Les microprocesseurs les plus rapides sont inutiles si la capacité des lignes de données n'est pas augmentée en conséquence. C'est là que les interconnexions électriques en cuivre (Cu) actuelles approcheront leurs limites physiques et pourraient ne plus être en mesure de suivre le débit de données d'un processeur. En fait, la fréquence de fonctionnement des processeurs d'aujourd'hui est déjà régie par les retards d'interconnexion et, en cours de fonctionnement, la plus grande partie de leur puissance est dissipée dans les interconnexions. Par conséquent, le manque d'interconnexions améliorées est à l'origine de la tendance actuelle à une simple réduction de la taille des circuits sans mise à l'échelle simultanée des performances de la technologie CMOS, contrairement aux décennies précédentes.

Parallèlement à la forte augmentation de la résistance des câbles d'interconnexion induite par la diminution des dimensions, les performances globales d'une puce se trouve dominées par les interconnexions pour la région submicronique. Parallèlement à la miniaturisation de la taille caractéristiques des dispositifs, le délai intrinsèque de porte diminue et le délai d'interconnexion augmente considérablement et devient dominant pour les performances globales. Obéissez à la loi de Moore [110] indique que les transistors sur puce seront réduits et doublés tous les deux ans afin

d'améliorer les performances et la production en volume. Toutefois, l'augmentation des performances des puces risque de se voir entravée si seuls les périphériques sont optimisés mais que ceux-ci ne disposent pas des interconnexions appropriées. Par conséquent, l'exploration et la recherche de matériaux alternatifs pour conducteurs d'interconnexion sur puce sont essentielles et nécessaire pour les futures puces hautes performances et faible consommation.

Pendant plusieurs décennies, l'aluminium (Al) a été utilisé pour les interconnexions sur puce. En raison des contraintes de mise à l'échelle des fils et de faible résistances des fils, le cuivre, avec sa faible résistivité, son faible coût et moins d'oxydation que l'aluminium, a été jusqu'à présent la solution privilégiée pour les fils d'interconnexion. Cependant, avec la réduction continue de la largeur de ligne des interconnexions en Cu, les performances et la fiabilité des conducteurs d'interconnexion requièrent une attention particulière pour suivre la mise à l'échelle des transistors. L'avancement de la photolithographie par fil métallique est également une composante importante du défi posé, la rugosité de la surface augmentant avec la largeur de raie du métal. Une densité de courant élevée entraînera la rupture du matériau d'interconnexion le long du chemin conducteur, ce qui provoquera également un dysfonctionnement du circuit et accélérera le délai de la puce. Les deux problèmes principaux des interconnexions actuelles en Cu sont la résistivité considérablement accrue et l'effet d'électromigration important, qui posent les limites physique des interconnexions en Cu.

Le cuivre en tant qu'interconnexion sur puce suivant un procédé damascène afin de réduire davantage la réduction d'échelle. Cependant, l'existence d'une couche barrière de tranchées d'interconnexion en Cu est nécessaire et ne peut être réalisée en dessous d'une certaine épaisseur ( $\sim 2$  nm); par conséquent, la fraction effective des lignes de Cu diminue considérablement si des lignes très minces avec une barrière induisent une augmentation importante de la résistance, encore moins de résistance à l'électromigration (EM) et en conséquence une dégradation des performances encore plus sévère. Par conséquent, il est proposé que des métaux alternatifs tels que le Ruthenium (Ru) et le Cobalt (Co) remplacent le Cu en conservant le procédé de Damas. Même si Ru et Co ont une résistivité supérieure à celle de Cu, du fait qu'ils ne possèdent pas de barrière, la résistance effective à la tranchée est inférieure à celle du Cu.

Le Graphène a été découvert en 2004 [116]. Le graphène est un arrangement en réseau hexagonal monocouche d'atomes de carbone. En raison de sa nature semi-métalliques et des propriétés particulières qui en découlent, où la bande de conduction et la bande de valence se croisent au point de Dirac, ses électrons se comportent comme des fermions de Dirac sans masse qui produisent du graphène ayant une vitesse de transport et une densité de courant élevées. Par conséquent, de nombreuses recherches sur le graphène sont conduites pour des applications ciblant les dispositifs micro-électroniques et les interconnexions. Une bande étroite de graphène, connue sous le nom de graphène nanoribbon (GNR), a été étudiée comme candidat prometteur pour remplacer les canaux de transistors [11, 117] et les interconnexions [130] pour les circuits intégrés de très grande taille de prochaine génération (VLSI). Le GNR présente de nombreux avantages sur les propriétés électriques [107], mécaniques et thermiques [10, 12]. Le GNR a une grande mo-

bilité des porteurs et une conductivité thermique [134]. Le libre parcours moyen des électrons dans du GNR peut atteindre plusieurs micromètres [15] et sa conductivité thermique est dans la gamme de 5300 W/mK. Cependant, Le GNR a des propriétés métalliques ou semi-conductrices en fonction de la disposition des atomes de bord. Un GNR à bords en zigzag se comporte de manière métallique et à "bord de fauteuils" est semi-conducteur [112]. Il reste encore difficile de fabriquer des GNR entièrement métalliques de haute qualité pour les applications d'interconnexion à grande échelle. Cependant, en raison de la quantification 2D et de la bande interdite étroite du GNR semi-conducteur, à la température ambiante ou au-dessus, la transition des électrons induite par les effets thermiques peut rendre la bande interdite étroite négligeable. Les GNR deviennent l'une des alternatives intéressantes et prometteuses pour les futures applications d'interconnexions sur puce.

Le nanotube de carbone (CNT) a été découvert sous la forme de parois multiples (MWCNT) en 1999 [63] par le chercheur japonais S. Iijima. Les CNT à paroi simple (SWCNT) sont découverts deux ans après en 1993 [64, 17]. Le CNT peut être vu comme enveloppant une ou plusieurs feuilles de graphène dans un fil cylindrique à une dimension, la distance entre les coquilles est définie par la distance de Van der Waals (0,34 nm) [45, 46]. Le diamètre des SWCNT peut varier de 0,4 nm à 4 nm (le diamètre typique est de 1,4 nm). Le diamètre de coque le plus à l'extérieur de MWCNT peut aller jusqu'à 100 nm. Le CNT en tant que fil quantique 1-D, possède une très forte liaison covalente entre atomes de carbone [166], ce qui lui confère un très bon confinement des électrons dans la direction uniaxiale. Les CNT ont également des propriétés physiques uniques: un tiers d'entre eux sont métalliques et les autres sont semi-conducteurs en fonction de leur chiralité [165, 131]. Les CNT métalliques ont de très bonnes propriétés pour les applications d'interconnexion, telles que le transport balistique, le chemin libre moyen des électrons (jusqu'à plusieurs), résistance mécanique élevée ( $\sim 1$  TPa) [132, 88], ampoule élevée (jusqu'à  $10^9$ ); ) [161, 171] et à haute conductivité thermique (de 2000 W/mK à 7500 W/mK) [66]. Cependant, les CNT ont toujours des problèmes de fiabilité en ce qui concerne les processus de fabrication et la conception. Au cours des dernières décennies, des chercheurs ont étudié les phénomènes de basse température (densité, intégrité), de densité élevée ( $>10^{13}$  cm $^{-2}$ ) [151, 44, 118], processus de croissance de haute qualité. Les contrôles de l'orientation des CNT [151, 44, 145] Néanmoins, la sélectivité de la chiralité [160, 59, 170] des CNT avec un processus développé par CVD à basse température reste un défi important pour les intégrations en bout de ligne (BEOL) compatibles avec les processus silicium.

L'objectif de cette thèse est d'explorer le potentiel des nanotubes de carbone et des composites de nanotubes de carbone pour les interconnexions faible consommation de la prochaine génération. Sur la base des modèles compacts physiques de pointe pour les CNT immobiles en SW et MW, nous avons tout d'abord développé un modèle compact amélioré basé sur la physique électrique en tenant compte de l'effet de dopage et de la variabilité des CNT autonomes pour une utilisation en tant qu'interconnexions locales. Deuxièmement, nous avons exploré le dopage des CNT, qui était l'un des principaux objectifs pour comprendre comment contrôler indirectement l'incertitude de la chiralité des CNT et améliorer davantage leurs conductivités et atténuer les défauts des contacts critiques. Nos modèles établis dans cette

thèse visaient à corrélérer les CNT réalistes cultivés par CVD à basse température. Troisièmement, nous avons étudié les propriétés électrothermiques composites des CNT et des CNT-Cu pour les utilisations d'interconnexions intermédiaires et globales. En raison de la densité de courant élevée fournie, l'effet thermique des interconnexions (auto-échauffement) est l'un des principaux facteurs des problèmes d'électromigration et de la défaillance des interconnexions. Enfin, nous avons intégré nos modèles électriques à des points de référence de circuits afin d'évaluer leurs performances et leurs efficacités énergétiques, que nous avons ensuite comparé avec des interconnexions en Cu. Cette thèse fait partie de et a été financée par la Commission européenne. Le projet européen Horizon 2020 CONNECT est financé par la subvention 688612. Le projet CONNECT est une collaboration entre l'Université de Glasgow (UoG), Royaume-Uni; LIRMM-CNRS, France; CEA Leti / Liten, France; Fraunhofer (FhG), Dresde, Allemagne; Synopsys, Royaume-Uni; AIXTRON Ltd., Cambridge, Royaume-Uni; et IBM Suisse.

Cette thèse porte principalement sur la modélisation compacte et les simulations au niveau du circuit en prenant des entrées à partir des résultats de la simulation au niveau atomistique fondamental (UoG) et en fournissant des retours aux partenaires expérimentaux (CEA et FhG) pour le guidage des expériences et la validation des modèles. Un autre aspect majeur consiste à fournir des directives de conception de niveau de circuit pour l'utilisation des interconnexions à base de CNT.

Au chapitre 2, nous décrivons les modèles compacts primitifs de résistance ( $R$ ) et de capacitance ( $C$ ) des CNT basés sur des travaux de littérature. Nous constituons une base solide en étudiant des modèles de base RC à CNT à une seule paroi (SW) et à plusieurs parois (MW). EN complément, nous proposons une étude approfondie des variations de processus et de leur impact sur les performances d'interconnexion du réseau MWCNT.

Au chapitre 3, nous évaluons la performance et la variabilité des interconnexions du réseau MWCNT tout en tenant compte de l'impact du dopage. Nous introduisons le paramètre nombre de canaux conducteurs ( $N_C$ ) et l'intégrons dans notre modèle compact amélioré de MWCNT décrit au chapitre 2. En calculant théoriquement  $N_C$  en fonction du décalage de niveau de Fermi  $E_f$  - nous évaluons chaque source de variation (diamètre, chiralité, défauts) et toutes sources en utilisant des simulations de Monte Carlo (MC). Les résultats de la simulation sont ensuite comparés aux résultats expérimentaux et une bonne cohérence est trouvée entre eux.

Au chapitre 4, nous avons commencé par étudier séparément les propriétés thermo-électriques des Cu, SWCNT, MWCNT, SWCNT-Cu composite et MWCNT-Cu composite. Nous construisons des modèles thermoélectriques pour chacun des cas en incluant des effets d'auto-échauffement, de diffusion de la chaleur vers le substrat. Un système d'équation différentielle à conduction thermique à composition automatique est résolu pour extraire le profil de température pour chaque cas d'interconnexion. De plus, nous avons déduit leurs caractéristiques I-V et leurs variations de résistance sous diverses tensions. L'ampacité est calculée à la fin afin de comprendre les propriétés thermoélectriques du matériau. Cette étude nécessite des validations supplémentaires avec des données expérimentales.

Dans le chapitre 5, nous cherchons à mieux comprendre les performances au niveau du circuit des interconnexions MWCNT dopées et le potentiel des technolo-

gie carbone, en comparant *CNTFET + MWCNT* et *FinFET + Cu*, présenté en tant qu'étude de cas pour les technologies avancées. Les modèles d'interconnexion MWCNT, CNTFET, 7 nm FinFET et PTM Cu model sont utilisés pour effectuer des simulations au niveau circuit. Le retard de circuit global, le produit de retard de puissance et d'énergie sont étudiés pour les deux cas d'étude. De plus, un circuit logique (additionneur/Full-Adder) est pris en exemple pour étudier et comparer différents choix d'interconnexions: interconnexions idéales, interconnexions en Cu et interconnexions MWCNT.

Une ouverture sur les nouvelles perspectives d'investigation des technologie à base de nano-tubes de carbones terminent le présent manuscrit de thèse



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# Chapter 1

## Introduction

### 1.1 Overview of On-Chip Interconnects

In today's modern society, fast and efficient lifestyle requires rapid, accurate, and safe information exchange. Enormous information and data acquired through various electronic devices. Different activities rely on complex electronic networks and the internet. Smart city, internet of things (IoT), and artificial intelligence of things (AIoT) become the essential trend for future technology development. Super-speed neuromorphic and quantum computing indicate the prospects of taking over the Von Neumann architectures. However, all these developments and evolutions consume a huge amount of energy. Satisfying high-performance and at the same time ultra-low power are the center of the interest for the next generation technologies. In order to meet the demand of data abundant workloads and its energy efficiency, miniaturization of microelectronic products, more precisely, the transistors, with enhanced functionality and decreased cost open the possibility to meet the aforementioned requests.

Nevertheless, improving only the transistor performance of future chip isn't sufficient. Chips are only one small part of the very large and complex information technology puzzle, albeit a very important one. Thus, to shape the future of the digital world, we also have to look at the bigger picture. Transistors are only as good as the system in which they are embedded. The fastest microprocessors are useless if the capacity of the data lines is not increased accordingly. This is where current electrical copper (Cu) interconnects will approach their physical limitations and may no longer be able to keep pace with a processor's data throughput. In fact, the operation frequency of today's CPUs is already governed by interconnect delays, and, during operation, most their power is dissipated in the interconnects. Therefore, the lack of improved interconnects is responsible for today's trend towards merely size-scaling without concurrent performance scaling of CMOS, unlike previous decades of scaling.

On-chip interconnects include global, intermediate and local interconnects. In Fig. 1.1 [1], it shows the on-chip interconnect structure. For global interconnects, vias are used for signal and power delivery. Large amount of current passes through global interconnects can generate severe electromigration (EM) issues. Metals with low resistivity and being strong against electromigration effect become the priority

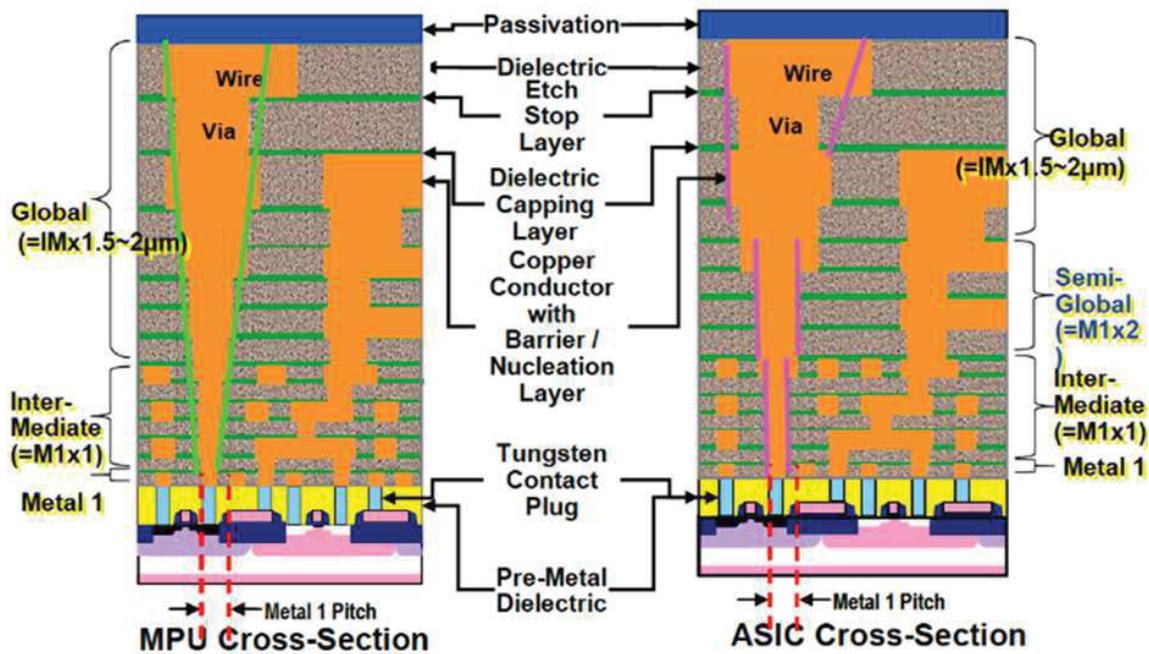


Figure 1.1: On-Chip hierarchical cross-sectional interconnect structure [1].

choices. Scaling of global interconnects is not as critical as intermediate and local interconnects. However, it still remains necessary to find solutions for electromigration problem and interconnects reliability. Intermediate interconnects are the metal wires connecting between cells and cores/modules. The module complexity leads to a rapid increase of wire resistances and capacitances when we scale the intermediate interconnects. Air gaps can be used to reduce capacitance effects, but the increase of resistance is critical. Local interconnects are short connections between cells and are the most sensible interconnects to the transistor miniaturization. As transistors size shrinks and density increases, there requires a huge amount of local interconnect, thus wire congestion and resistance become detrimental for future technology nodes. New materials and components with barrier-less and ballistic transport are widely investigated.

On-chip delay becomes dominating by interconnects when the minimum on-chip feature size scales to submicron region (Fig. 1.2). Accompanying with the miniaturization of device feature size, intrinsic gate delay decreases while interconnect RC delay increases and becomes dominant for overall performance. Moore's law [110] indicates that on-chip transistors double its number for every two years in order to meet the request for better performance and higher volume production. Due to the area limitation of the chip, integrating two times of transistors need to scale down each of them. Scaling of transistors increases their performances and further aims to improve the chip overall performance. However, the increase of the chip performance cannot be guaranteed if only devices are optimized but without interconnects. Therefore, exploring and investigating alternative on-chip interconnect conductor materials are critical for future high performance and energy efficient chips.

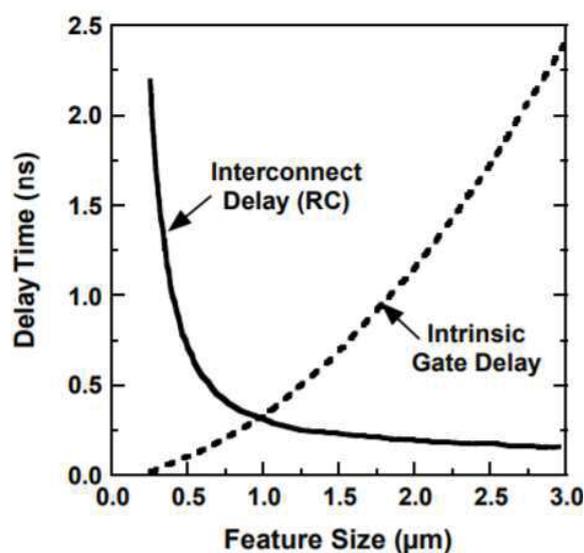


Figure 1.2: Interconnect delay becomes dominant for submicron region [100].

## 1.2 Copper Interconnects

Accelerated technology scaling has aggravated Copper (Cu) resistivity increase due to electron scattering and even more severely, it introduced electromigration issues. Mass transport along interfaces and grain boundaries in state-of-the-art Cu interconnects is one of the most important issues to be solved for future technology nodes according to the International Roadmap for Devices and Systems (IRDS) [2].

During several decades, aluminium (Al) has been used for on-chip interconnect wires. Due to the demands of wire scaling and lower wire resistivity, copper with its low resistivity, low cost and less oxidation than Aluminium and scalability has been considered for the suitable interconnect wires until nowadays. However, with the continuous downscaling of Cu interconnect linewidth, performance and reliability of interconnect conductors become severe issues to follow the transistors scaling. The advancement of thin metal wire photo-lithography is also an important factor for realization challenge, surface roughness increases with metal linewidth gets thinner. High current density will lead the interconnect material breakdown along the conducting path, which will further cause circuit malfunction and accelerate the chip's time to failure. Two main issues of current Cu interconnects are 1) exponential increased resistivity and 2) occurrence of electromigration effect, which indicate the physical bottleneck of Cu interconnects for further performance improvement.

### 1.2.1 Copper Interconnects - Resistivity

For Cu interconnects structure, there are not only the metal conductor itself but accompanying with barrier layer to prevent Cu diffusion into the surrounding dielectric, nucleation layer on the barrier material to enable metal film growth, and then metal conductor filling inside [143]. While interconnects are downscaled, thickness and volume of each layer will be reduced. This is causing the increase of Cu electri-

cal resistivity where rising of electron scattering at metal grain boundaries and at metal surface and interfaces. Figure 1.3 (a) illustrates the scattering phenomena for an interconnect structure, and increase of Cu resistivity due to grain boundaries and scattering effects is shown in (b).

Other important factors are also contributing to the interconnect total resistance, such as the contact resistance and interconnects geometry. With shrinking of linewidth, contact resistance is increasing as contacting area is reduced, thus the overall interconnect performance degrades. Inter-metal capacitance is also governing the interconnect performance, which is geometry and inter-metal dielectric dependent. Air gap [113] and low- $k$  (dielectric constant) insulating materials are studied recently in order to reduce the effective dielectric constant.

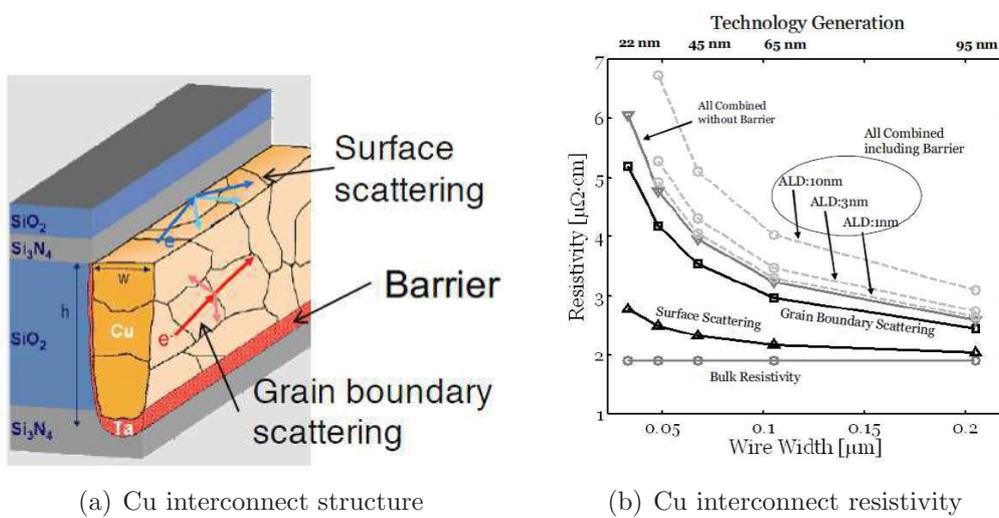


Figure 1.3: (a) Copper interconnects suffer from grain boundary and surface scattering effects. (b) Grain boundary and scattering effects increase Cu interconnects resistivity with shrinking of Cu width [77].

## 1.2.2 Copper Interconnects - Electromigration

Apart from increase of resistivity and degradation of performance, another critical metric for interconnects is the reliability, which determines how an interconnect conductor can maintain charge flow that goes through it without damaging the metal conductor and degrading performance, or even causing interconnect material breakdown. Downscaling of interconnects indicates the reduction of wire cross-sectional area and maximizing the current density  $J$ , in A/cm<sup>2</sup> [97]. Once the maximum current density approaches the conductor material current-carrying capacity, the moving electrons with associated electric field have enough energy to displace atoms from their original lattice sites where voids and hill-hocks can happen in the thin conductor material. This is due to a combination of the electron wind force, the temperature gradient induced force, the stress gradient induced force and the surface tension force. This phenomenon is known as electromigration (EM). EM is a

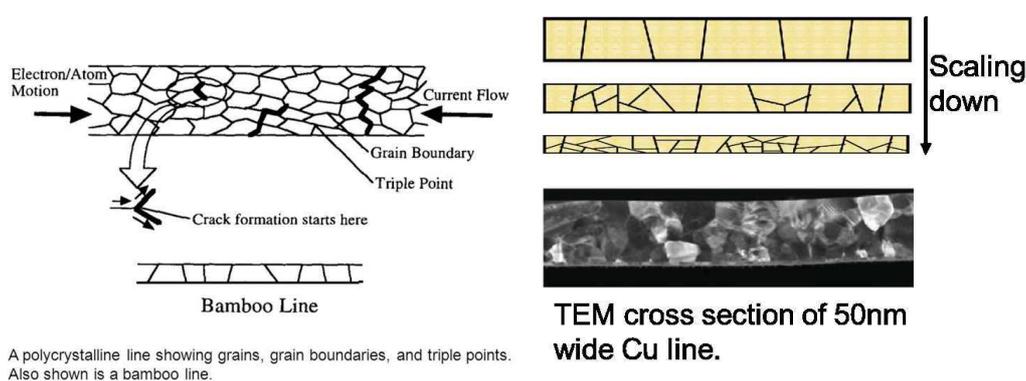
severe issue leading the chip failure and malfunctions. The maximum current density projected for interconnects in future technology nodes is  $J_{\max} \geq 2\text{MA}/\text{cm}^2$  [97] from 2014 on. Cu bulk material maximum current-carrying capacity is  $2\text{MA}/\text{cm}^2$ , that clearly cannot meet the requirements for future technology nodes. In Fig. 1.4 (a), a polycrystalline line showing grains, grain boundaries and triple points and structure cracks happen at those interfaces are shown. TEM (Transmission Electron Microscopy) image in (b) shows the cross section of 50 nm wide Cu line with EM issues. This material intrinsic property limitation shows the bottleneck of Cu for further on-chip interconnects implementation due to its severe reliability issue.

## 1.3 Emerging Interconnects for Advanced Technology Node

### 1.3.1 Metal Interconnects: Cobalt and Ruthenium

On-chip interconnects integration requires a Damascus process where Cu metal is surrounded by liner/barrier layers and then dielectrics. Existence of barrier layer of Cu interconnect trenches is necessary and can not be scaled less than certain thickness ( $\sim 2$  nm). Hence the effective fraction of Cu lines is shrinking such that thin Cu lines with a barrier will induce an important resistance increase and performance degradation, and even more prone to electromigration (EM). Therefore, the alternative metals Ruthenium (Ru) and Cobalt (Co) are investigated to replace Cu with the same Damascus integration process. Even-though, Ru and Co have higher resistivity than Cu, but being barrierless makes the effective trench resistance less than that of Cu.

Recently, the major semiconductor industries have investigated alternative metals for advanced technology nodes. Table 1.1 summarizes the state-of-the-art alter-



(a) Polycrystalline line interconnect structure (b) Cu interconnect EM phenomenon under TEM observation

Figure 1.4: (a) Formation of electromigration for a bulk metal interconnect. (b) Scaling induced more electromigration effects, voids and breaks are dominant for Cu interconnects performance and lifetime.

native materials for future interconnects. For 14 nm node, Cu and W (tungsten) [3, 182] are being investigated for process and barrier materials by Intel. Co will be mainly explored by Intel and Global Foundries due to its barrierless advantages [40, 154] for 10/7 nm nodes. Further scaling to 5/3 nm nodes, IMEC is stretching out the possibility of Ru thanks to its weak thickness dependent resistivity [155, 40, 178, 4]. When technology node scales to beyond 3 nm, new materials need to be explored. Such as carbon nanotube, graphene nanoribbon and other composite materials. TSMC is considering the carbon based materials, more precisely multi-layered graphene nanoribbon [159]. Ballistic transport and high thermal and electrical conductivity in carbon based materials and its composite indicate its suitability for interconnects, however, contact resistance and integration process are still big challenges.

Table 1.1: Alternative interconnects for future technology node.

Technology	14nm	10/7nm	5/3nm	<3nm
Interconnect metals	Cu / W [3, 182]	Co [155, 40, 154]	Ru [155, 40, 178, 4]	New compound: CNT, GNR [159, 176], composite material [144]
Advantages	Low resistivity	No barrier	Weak thickness dependent resistivity	Ballistic transport
Limitations	Barrier effect	High resistivity	Surface scattering	Integration / Contact resistance
Industries	Intel	Intel / Global Foundries	IMEC	TSMC

### 1.3.2 Graphene Nanoribbon Interconnects

Graphene has been discovered in 2004 [116]. Graphene is a monolayer hexagonal lattice arrangement of carbon atoms. Due to its special nature of semi-metallic properties, where conduction band and valence band cross at Dirac point, its electrons behave like massless Dirac fermions that makes graphene having a high carrier velocity and current density. Hence, many researches on graphene are driven for electronic devices and interconnects applications. A narrow stripe of graphene, known as graphene nanoribbon (GNR) has been investigated for promising candidate to replace the transistor channels [11, 117] and interconnects [130] for next-generation very large scale integrated (VLSI) circuit. GNR has many advantages on electrical [107], mechanical [83] and thermal [10, 12] properties. GNR has high carrier mobility and thermal conductivity [134]. The electron mean free path in GNR can reach several micrometers [15] and its thermal conductivity is in the range of 5300 W/mK. However, GNR has metallic or semiconducting properties depending on the edge atoms arrangement. A zigzag-edged GNR behaves metallic and armchair-edged GNR is semiconducting [112]. It still remains challenge to fabricate high quality and fully metallic GNRs for large scale interconnect applications. However, due to the 2D quantization and narrow bandgap of semiconducting GNR, at room temperature or above, thermal effects induced electrons transition can make the narrow bandgap negligible. GNRs become one of the interesting and promising alternatives for future on-chip interconnects applications [159, 176].

### 1.3.3 Carbon Nanotube Interconnects

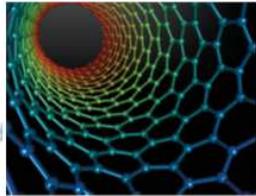
Carbon nanotube (CNT) is discovered as multi-walled (MWCNT) in 1999 [63] by Japanese researcher S. Iijima. Single-walled CNT (SWCNT) is discovered two years after in 1993 [64, 17]. CNT can be seen as wrapping up one or multi graphene sheets into a 1-dimension cylindrical wire, the inter-shell distance is defined by Van der Waals distance (0.34 nm) [45, 46]. Diameter of SWCNT can vary from 0.4 nm to 4 nm (typical diameter is  $\sim 1.4$  nm). The outermost shell diameter of MWCNT can be up to 100 nm. CNT as 1-D quantum wire, has a very strong  $sp^2$  covalent bonding between carbon atoms [166], hence having a very good electron confinement in uni-axial-direction. CNTs also have unique physical properties that one third of them are metallic and the rest are semiconducting depending on their chirality [165, 131].

Metallic CNTs have very good properties for interconnect applications, such as ballistic transport [76, 135, 9], large electron mean free path (up to several  $\mu\text{m}$ ) [164, 90, 105, 129, 53, 172, 89, 5], high mechanical strength ( $\sim 1$  TPa) [148, 132, 88], high ampacity (up to  $10^9$  A/cm<sup>2</sup>) [161, 171, 162] and high thermal conductivity (from 2000 W/mK to 7500 W/mK) [14, 21, 66]. However, CNTs still have reliability challenges on fabrication process and design aspect. For the past decades, researchers have investigated on low temperature [157, 173, 92], high density ( $>10^{13}$  cm<sup>-2</sup>) [151, 44, 181, 118], high quality growth process. CNTs orientation control [151, 44, 145, 179, 22, 72] and high metal-CNT contact resistance [103, 32, 169, 31] were also been studied for nano- and micro- electronics applications. Nevertheless, chirality selectivity [160, 59, 170] of CNTs with low temperature CVD grown process still remain

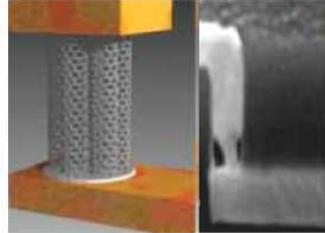
big challenge for silicon process compatible back-end-of-line (BEOL) integrations.

CNTs have been well investigated in the past thirty years. A brief history of essential achievements of CNTs on electronic applications is shown in Fig. 1.5. Ten years after the discovery of CNTs, IBM has demonstrated the possibility of CNT based transistor. Semiconducting CNT has been used as transistor channel under back-gated. One year after, in 2002, Kreupl from Infineon has first proposed CNTs with metallic properties for interconnect usage. In 2013, first CNT based computer were demonstrated by Shulaker et al. in Stanford University [136]. With further technology development, in 2015, 7 nm p-channel SWCNT based channel transistor using p-type end contacts are shown by IBM. In 2016, employing CNTs mechanical properties, the company NANTERO have developed a CNT based non-volatile random access memory (RAM) for molecular computing. In 2017, Stanford University built a CNT based chip by using three-dimensional integration of nanotechnologies for computing and data storage [137]. This chip has integrated silicon logic, CNT-FET logic, RRAM (resistive random access memory) and CNTFET based logic and sensors.

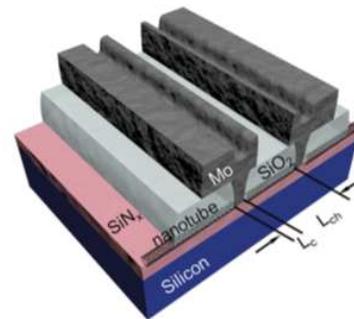
# A brief History of CNT



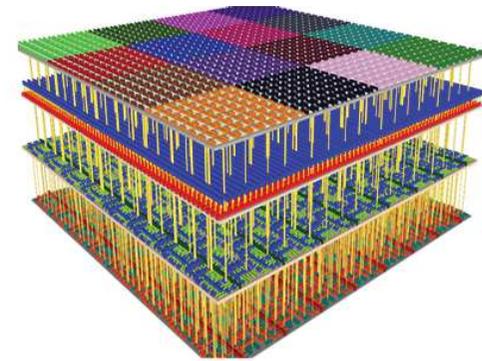
Nanotubes discovered by Dr. S. Iijima (NEC) 1991



CNT interconnects (Kreupl, Infineon) 2002



7nm p-channel SWCNT transistor using p-type end contact (IBM) 2015

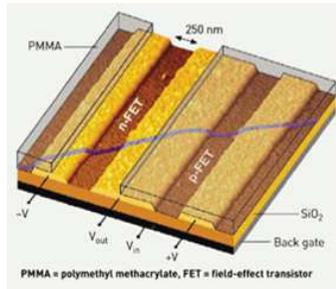


A 3D stack of silicon logic, resistive RAM, nanotube circuits, and sensors uses new architecture and devices to save energy (Stanford) 2017



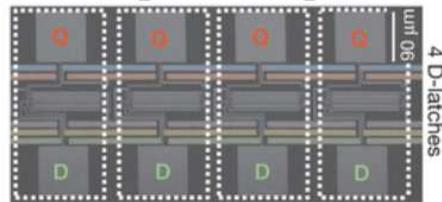
2001

Carbon nanotube transistor (IBM)



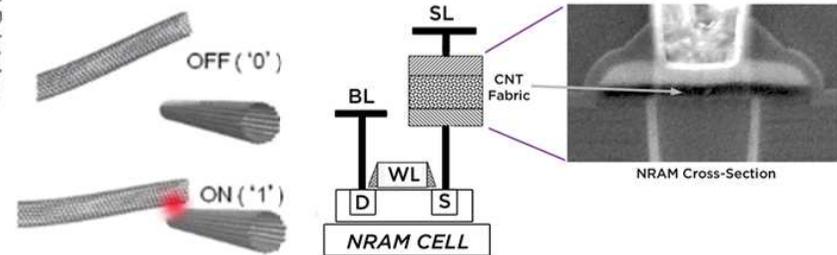
2013

First Carbon nanotube computer (Shulaker et al. Stanford)



2016

Carbon nanotube-based non-volatile random access memory for molecular computing (NANTERO - NRAM)



MRAM™ cell with CMOS select transistor and CNT resistive change memory element shown in SEM cross-section

Figure 1.5: A brief history of Carbon Nanotube.

## 1.4 Structure of the Thesis

The focus of this thesis is to explore the potential of carbon nanotubes and carbon nanotube composite for next generation energy efficient on-chip interconnects. Based on the state-of-the-art physical compact models for pristine SW and MW CNTs, we firstly developed models by taking into the account the doping effect, variability impacts, and thermal effect. Secondly, we explored doping of CNTs to indirectly control CNTs chirality uncertainty, enhance its conductivity, and mitigate defects and high contact drawbacks. Our models are based on experimental grown low temperature CVD CNTs. Thirdly, we studied CNTs and CNT-Cu composite electrical-thermal properties for intermediate and global interconnects usage. Due to high current density, interconnects thermal effect (self-heating) is one of the main factor for electromigration issues and interconnect breakdown. Finally, we integrated our electrical models into circuit benchmarks in order to understand its performance and energy efficiency, in addition, comparing with Cu interconnects.

This thesis is part of and has been funded by European Commission H2020 CONNECT Project under Grant 688612. CONNECT project is a collaboration among University of Glasgow (UoG), UK; LIRMM-CNRS, France; CEA Leti/Liten, France; Fraunhofer (FhG), Dresden, Germany; Synopsys, UK; AIXTRON Ltd., Cambridge, UK; and IBM Switzerland.

This thesis is mainly working on compact modeling and circuit level simulations by taking inputs from fundamental atomistic level simulation results (UoG), and providing feedbacks to experimental partners (CEA and FhG) for experiment guidance and model validations. In addition, providing circuit level design guidelines for CNT based circuit.

This thesis is organized as follows:

- **Chapter 2: Pristine Carbon Nanotube**

In this chapter, we describe the pristine CNT electrical resistance (R) and capacitance (C) compact models based on literature works. We started by investigating basic pristine single-walled (SW) and multi-walled (MW) CNTs RC models. Furthermore, we performed a thorough study on process variations and their impact on MWCNT interconnect performance.

- **Chapter 3: Doping of Carbon Nanotube**

In this chapter, we evaluate MWCNT interconnects performance and variability while considering the impact of doping. We introduce a new parameter, the number of conducting channels ( $N_C$ ) and incorporate it into our enhanced MWCNT compact model described in Chapter 2. By theoretically calculating  $N_C$  as a function of Fermi level shift  $E_f$  - we evaluate each source of variation (diameter, chirality, defects) and all-sources using Monte Carlo (MC) simulations. Simulation results are subsequently compared with experimental results, and a good consistency is found between them.

- **Chapter 4: Copper-Carbon Nanotube Composite**

In this chapter, we started by investigating the electrical-thermal properties for Cu, SWCNT, MWCNT, SWCNT-Cu composite and MWCNT-Cu composite separately. We build electrical-thermal model for each of the cases by including self-heating, heat diffusion to substrate effects. A self consist heat conduction differential equation system is solved to extract temperature profile along the interconnect. In addition, we derived their I-V curves and resistance variations under various voltage supply. Ampacity is calculated in order to understand the material reliability. This study needs further validations with experimental data.

- **Chapter 5: Circuit Level Analysis of Carbon Nanotube Interconnects**

In this chapter, we investigated circuit-level performance of doped MWCNT interconnects and the potential of all carbon technology. we compared CNT based field effect transistor connecting by our standalone MWCNT interconnect (*CNTFET + MWCNT line*) with FinFET connecting by conventional Cu interconnect (*FinFET + Cu line*) as two advanced technology testcases. CNTFET, 7nm FinFET and PTM Cu interconnect models are used to perform circuit-level simulations. Overall circuit delay, power and energy delay product are computed for both testcases. Furthermore, a full-adder benchmark is employed to study and compare different interconnect choices: ideal interconnects, Cu interconnects and standalone MWCNT interconnects.

- **Conclusion and Perspective**

In conclusion, we summarised the main achievements from each chapter and give takeaway key messages. We described next steps and further investigation perspectives.

The main contributions of this thesis are summarised in the Table 1.2.

Table 1.2: Main Contributions in this Thesis

Chapter	Main Contributions	Assessment
Chapter 2	1) We present a compact shell-level model of MWCNT to include the defects, chirality, end-contact resistance and shell connectivity to end-contacts. 2) We perform Monte Carlo (MC) or best/worst cases simulations to study variations in diameter, chirality, the presence of defects (defect density) and contacts.	We provide the first shell-to-shell MWCNT distributed models including variability sources.
Chapter 3	We investigated doping of CNTs by introducing Fermi-Level shift related number of conducting channels $N_C$ as physical key parameter for doped CNT models. 1) Analytical calculations of $N_C$ vs. $E_F$ shift. 2) Enhanced doped CNT electrical compact models and simulations. 3) Experimental results correlation and comparison.	For the first time, a systematic investigations are realized by including theoretical modeling and experimental measurements for doped standalone CNT interconnect. Good consistency is found between them.
Chapter 4	1) We investigated the electro-thermal properties and modeling on SW/MW CNTs and CNT-Cu composite. 2) Temperature profile, I-V and resistance variations are evaluated based on our electro-thermal models. 3) CNT-Cu composite ampacity and conductivity are extracted for state-of-the-art results comparison.	A macroscopic physical based electro-thermal model for CNT-Cu composite for interconnects. We explored for the first time compact modeling of CNT-Cu composite for intermediate and global interconnects.
Chapter 5	1) We investigated circuit-level benchmarking and simulations for all carbon based circuit (CNTFET + CNT lines), and comparing to conventional Cu technology. 2) Full-adder circuit is employed to evaluate the performance and energy of CNT interconnects.	We evaluated our models in circuit-level to provide useful insights for future CNT interconnect design guideline.



# Chapter 2

## Pristine Carbon Nanotubes

### 2.1 Introduction

As technology scales down, the transistor performance continues to improve. However, for interconnect, scaling leads to higher current density and more substantial resistance. The transition of interconnect material from Aluminum (Al) to Copper (Cu) a few decades ago enabled further scaling of interconnects. Nevertheless, Cu interconnects resistance rises rapidly as its dimensions scale and become comparable to the order of electron mean free path ( $\sim 40$  nm at room temperature) [65], [143]. Compared with Cu, carbon nanotube (CNT) has attractive properties such as ballistic transport, high thermal conductivity, and ampacity [146],[98]. Because of strong  $sp^2$  bonding between carbon atoms, CNT is much more resistant to electromigration (EM) and can sustain significantly larger current densities than Cu [162]. Furthermore, self-heating problem is a concern on deeply scaled Cu interconnects whereas CNTs have long ballistic electronic transport length  $\sim 1$   $\mu\text{m}$ , making them have higher electrical and thermal conductivities and thus capable of carrying high current density with virtually no heating thanks to its 1D electronic structure [147, 13, 57].

Carbon nanotubes are currently being investigated as potential replacement of back-end-of-line interconnect copper material for integrated circuits. Carbon nanotubes have a semiconducting or metallic property due to their special Dirac energy band structure and open a field for nano- or micro-electronic devices and interconnect applications. Compared with Cu line process, the fabrication of CNT requires different processing steps and much higher temperature (up to  $900^\circ\text{C}$  [121]) to achieve good quality CNT growth. However, achieving back-end-of-line process compatible with CNTs would require to grow them at a lower temperature such as  $450^\circ\text{C}$  to  $500^\circ\text{C}$ . Growing CNTs at such temperatures introduces several variations, i.e., diameter, chirality. Furthermore, at such temperatures defects are omnipresent, and the most typical types are vacancies, interstitials, non-hexagonal rings and grain boundaries [38], [177]. Defects can trap or scatter carriers and thus ultimately impact CNT interconnect performance.

Good contacts between the CNTs and metal electrodes are very challenging. Poor contacts induce a significant contact resistance or might be even disconnected as in the case of inner shells on MWCNTs [122, 149]. This can be a significant

concern for vertical interconnects where the electrode acts as a support for the catalytic growth of CNT and also as an electrical contact [50]. Currently, there are two types of contacts with CNTs - side-contacts and end-contacts [23]. The side-contact has the metal deposited on top of the CNT, enabling the electrons to flow along the length of the metal-CNT tube interface and the contact resistance depends on the overlap length between the metal and CNT tube. End-contacts are formed between the end of CNT tube and metal. The interface between electrode and CNT for the end-contact is covalent metal-carbon bonds while it is Van der Waals bond for the side contact as discussed and described in [23]. As a result, the end-contact tends to have smaller contact resistance than the side-contact. Whereas, end-contacts in MWCNT may suffer from disconnected shells to the electrodes which ultimately also increases the contact resistance.

In this chapter, we describe the pristine CNT electrical resistance (R) and capacitance (C) compact models based on literature works. We would like to start our work with a solid base by investigating basic pristine single-walled (SW) and multi-walled (MW) CNTs RC models. Furthermore, we perform a thorough study on process variations and their impact on MWCNT interconnect performance.

We investigate the CNT quantum transport property and use the number of conducting channels  $N_C$  as a figure of merit for computing the change in CNT conductance due to process variations. On SWCNTs (with the diameter less than 10 nm) the variations in diameter have been shown to have little impact on its conductance [91]. However, on MWCNTs, the diameter variations may change the total number of shells and  $N_C$ ; thus, the MWCNT conductance can vary significantly. Chirality determines the property of the CNT, which can be either metallic or semiconducting. Metallic and semiconducting CNT conductivities are significantly different, especially for small diameter CNT [111]. Shell connection to the end-contact also impacts overall MWCNT resistance, and even more so for MWCNT with many shells [89].

To understand how CNT interconnect performance is impacted by these variations, we develop a compact shell-level model capable of combining the MWCNT physical properties with process variations. Such a model is essential for circuit-level simulation and circuit design space exploration with MWCNT interconnects.

The contents in this Chapter have been published on:

[96]: *Jie Liang* et al. "Physical description and analysis of doped carbon nanotube interconnects", in IEEE International Workshop on Power and Timing Modeling, Optimization and Simulations (PATMOS) (2016), pp. 250-255.

[29]: Rongmei Chen, *Jie Liang*, et al. "Variability Study of MWCNT Local Interconnects Considering Defects and Contact Resistances - Part I: Pristine MWCNT", in IEEE Transactions on Electron Devices 65.11 (2018), pp. 4955-4962.

## 2.2 Physical Description of Carbon Nanotube

Carbon nanotube, known as 1-D quantum material which can be obtained by rolling up a mono-layered graphene sheet. Rolling direction of graphene impacts directly the physical properties of carbon nanotube. For a graphene mono-layered sheet,

we define two unit vectors  $\vec{a}_1$  and  $\vec{a}_2$  that represent the minimum unit cell vectors based on material crystallography physics. From vectors  $\vec{a}_1$  and  $\vec{a}_2$ , we define the carbon nanotube chiral vector  $\vec{C} = n\vec{a}_1 + m\vec{a}_2$ , which indicates the graphene rolling direction. Different  $n$  and  $m$  indices will provide a kind of rolling thus a type of carbon nanotube. There are typically three types of chirality for carbon nanotube: chiral, zigzag and armchair. As shown in Fig. 2.1, chiral nanotube has the end sides with unregulated shapes. For nanotubes having end sides shaped as zigzag form are named zigzag nanotube. And for armchair tubes, the end sides have flat up and down shapes, so called armchair. Carbon nanotubes are not only single walled (SW) but also multi walled (MW). For multi-walled carbon nanotube (MWCNT), there are coaxial single shell nanotubes formed together with different diameters as shown in Fig. 2.2. Shell to shell distance is 0.34 nm, so called Van der waals distance. Each shell of MWCNT has different chirality, thus different electrical properties. Therefore, a SWCNT or MWCNT is formed with various sources of variability that can impact nanotubes electrical properties. Impacts of different sources of variability are studied separately in the following sections of this chapter.

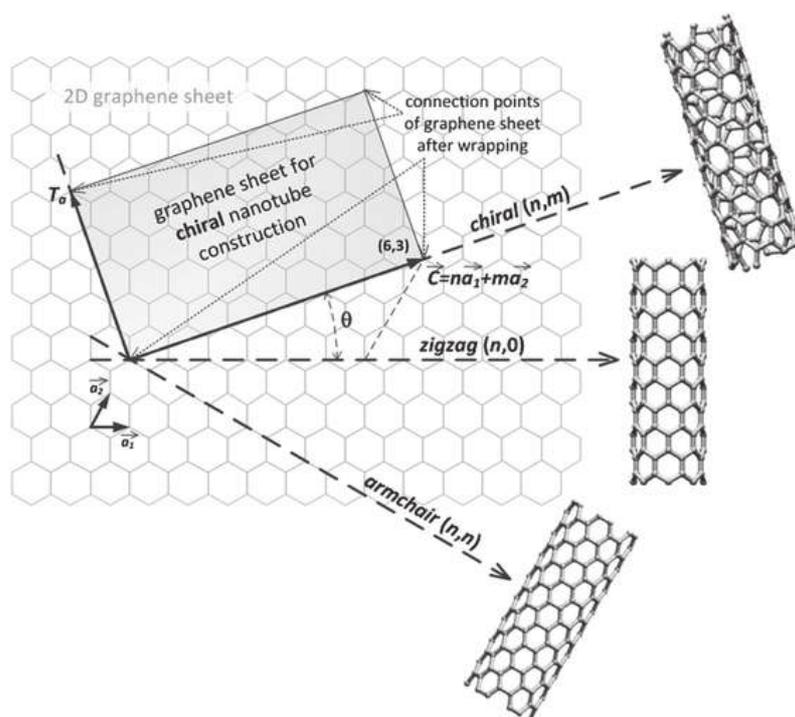


Figure 2.1: Carbon nanotube, based on different rolling direction, can have three types of chirality: chiral, armchair and zigzag. Chirality of carbon nanotube is defined by chiral vector  $\vec{C}$  which composed by indices  $n$ ,  $m$  and unit vector  $\vec{a}_1$  and  $\vec{a}_2$ .

Beside defining carbon nanotubes by different chirality, we can as well define them by different electrical properties, either metallic or semiconductor nanotubes. Important parameters to define the metallic or semiconductor properties are given by chiral vectors indices  $n$  and  $m$ . If the difference  $(n-m)$  between  $n$  and  $m$  is a multiple of 3 and  $n \neq m$  and  $nm \neq 0$ , then this type of carbon nanotube has a

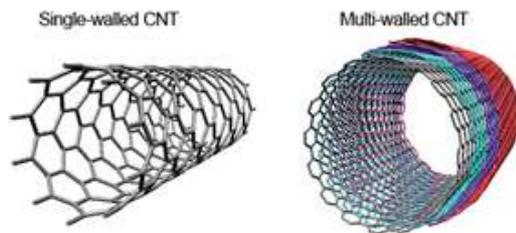


Figure 2.2: Carbon nanotubes can be formed as single-walled (SWCNT) or multi-walled (MWCNT). MWCNT can be seen as coaxial SWCNT shells with different diameters.

quasi metallic property with bandgap nearly 0. Otherwise, nanotube is a moderate semiconductor tube [79]. In Fig. 2.3, it illustrates the typical energy band structure of metallic and semiconductor carbon nanotubes, where in (a), a Dirac point band structure is shown for metallic nanotube, and a clear bandgap is observed in (b) for semiconductor nanotube.

Another interesting properties of carbon nanotube is the diameter dependent electrical property. As the carbon nanotube diameter increases, tube metallic properties increases, and large diameter MWCNT often shows a metallic property.

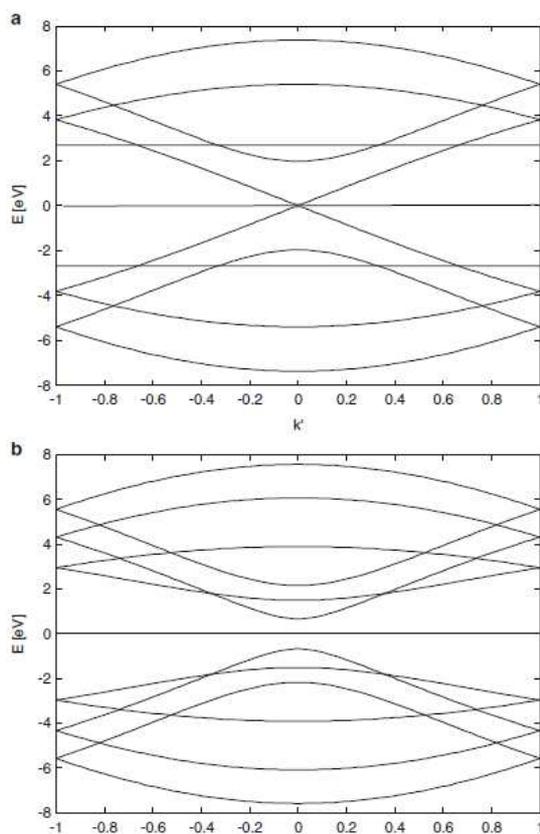


Figure 2.3: Typical Energy Band Structure of (a) metallic and (b) semiconductor carbon nanotube.

## 2.3 Pristine CNT Resistance and Capacitance

A novel material used as back-end-of-line (BEOL) requires a good understanding on how fundamental physical effects can impact the macroscopic electrical and thermal properties. Modeling novel quantum materials such as graphene, graphene nano ribbon (GNR) or carbon nanotube for on-chip interconnect material requires the modeling of its equivalent resistance and capacitance. We do not consider the inductance in this thesis. From the electrical point of view, CNTs are modelled as an RC circuit, which allows to devise analytical formulas to describe the CNT as an interconnect [141, 146]. Here, we concentrate on the resistance and capacitance variance for different type of CNTs.

### 2.3.1 Pristine SW/MW CNT resistance

The resistance of an isolated SWCNT includes intrinsic quantum resistance and scattering resistance, which are due to the quantum transport and electron-phonon scattering [114]. CNTs could be considered as a quantum wire transport where the conductance is evaluated using the two-terminal Landauer-Buttiker formula [80]. This states that, a 1-D system with  $N$  channels in parallel, the conductance is as  $G = (Ne^2/h)T$ , where  $h$  is the plank constant and  $T$  is the transmission coefficient for electrons pass through the CNT. Due to electron spin degeneracy and two effective atoms per unit cell in graphene, pristine SWCNT has four conducting channels in parallel ( $N = 4$ ), ballistic transport in SWCNT assumes perfect contacts ( $T = 1$ ), the intrinsic SWCNT conductance is given by  $G_0 = 4e^2/h$  which yields a resistance about 6.45 k $\Omega$ . For the length of CNT longer than the electron mean free path (here we take  $L_{MFP} = 1 \mu\text{m}$ ) [68], scattering resistance becomes important and need to be taken into account. Equation 2.1 shows the total SWCNT resistance with scattering resistance as:

$$R_{SWCNT} = \frac{h}{4e^2} \left( 1 + \frac{L}{L_{MFP}} \right) + R_C \quad (2.1)$$

where  $R_c$  is the contact resistance for interconnect. Also from the tight-binding (TB) calculation, mean free path (MFP) of electrons in metallic and semiconducting CNT are given as:

$$L_{MFP}^{Metallic} = \frac{D\sqrt{3}\psi^2}{2\sigma_\epsilon^2 + 9\sigma_\psi^2} \quad (2.2)$$

$$L_{MFP}^{S-C} = \frac{D\vartheta_F}{\alpha T} \quad (2.3)$$

where  $\psi$  is the nearest neighbor tight-binding parameter,  $\epsilon$  is the on-site energies, and  $\sigma_\epsilon$  and  $\sigma_\psi$  are the variances of  $\epsilon$  and  $\psi$ , respectively. For pristine CNT, we chose  $\sigma_\epsilon = 0.04$  eV and  $\sigma_\psi = 0$  (for doped CNT,  $\sigma_\epsilon = 0$  and  $\sigma_\psi = 0.06$  eV) [69].  $\vartheta_F$  is the Fermi velocity of CNTs ( $\sim 8 \cdot 10^5$  m/s),  $\alpha$  is the coefficient of scattering rate, and  $T$  is the temperature. Quantum resistance  $1/G_0$  is a material property which is evaluated by the two-terminal Landauer-Buttiker formula. Scattering resistance depends on the electron mean free path (MFP), MFP is mostly depending on CNT diameter,

but for semiconducting CNT, temperature is also a dependency. An example result (Fig. 2.4) illustrates an individual pristine SWCNT resistance variation due to SWCNT diameter (D) and length (L). We observe a sharp decrease of resistance with large diameter and a strong resistance for a long narrow SWCNT. Table 2.1 shows resistance values for different L and D of SWCNT. A decrease of resistance can be observed by increasing the diameter from 1 to 20 nm for a long length (L = 5  $\mu\text{m}$ ), while there are less length impacts on resistance for greater diameter (i.e., D > 5 nm). We note that for longer SWCNT, larger diameters have greater impact on reducing resistance. 80% of resistance is reduced by a 5  $\mu\text{m}$  SWCNT with D = 20 nm.

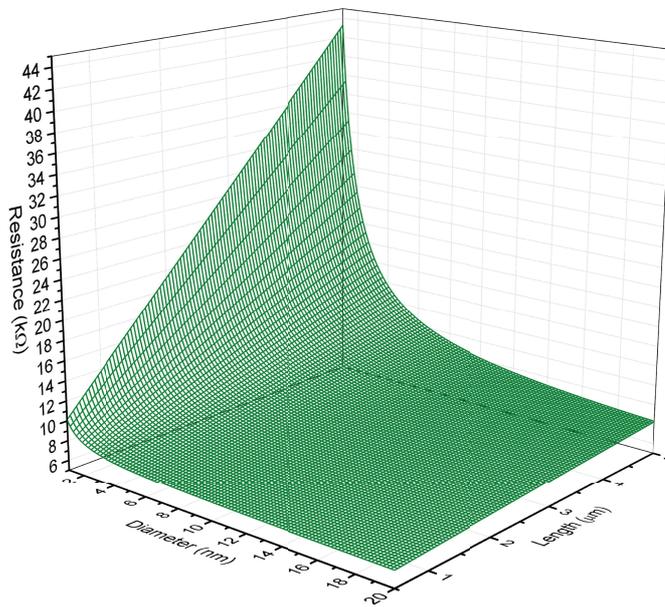


Figure 2.4: Resistance of pristine SWCNT varies with its diameter and length (diameter varying from 1 nm to 20 nm; length varying from 0.5  $\mu\text{m}$  to 5  $\mu\text{m}$ ).

Table 2.1: Values of pristine SWCNT Resistance for various length and diameter

L	D=1nm	D=20nm	Reduction in %
1 $\mu\text{m}$	13.8 k $\Omega$	6.8 k $\Omega$	50.7 %
1.6 $\mu\text{m}$	18.2 k $\Omega$	7.04 k $\Omega$	61.3 %
2 $\mu\text{m}$	21.2 k $\Omega$	7.2 k $\Omega$	66 %
5 $\mu\text{m}$	34.3 k $\Omega$	8.3 k $\Omega$	80.8 %

For a pristine multi-walled carbon nanotube (MWCNT), the widely used total conductivity [111] and total resistance are given as equations 2.4 and 2.5, respec-

tively. Shell-to-shell distance (van der waals distance) is  $\delta = 0.34$  nm.

$$\sigma_{MWCNT} = \frac{G_0 l}{2\delta} \left[ \left(1 - \frac{d_{min}^2}{d_{max}^2}\right) \frac{a}{2} + \left(b - \frac{l}{l_0} a \times \left( \left(\frac{1}{d_{max}} - \frac{d_{min}}{d_{max}^2}\right) - \frac{l}{d_{max}^2 l_0} \ln \frac{d_{max} + \frac{l}{l_0}}{d_{max} + \frac{l}{l_0}} \right) \right] \quad (2.4)$$

$$R_{MWCNT} = \frac{4L}{\sigma_{MWCNT} \pi D_{max}^2} \quad (2.5)$$

Inter shell tunnelling conductance is given as equation 2.6 [91]:

$$G_T = \sigma \pi D \quad (2.6)$$

which depends on the shell diameter. We compare MWCNT conductivity with and without inter shell tunnelling based on analytical formulas (equations 2.4 and 2.6) shown in Fig. 2.5. We noticed that almost no difference with and without tunnelling. This result shows a standalone MWCNT conductivity. However, when contacting MWCNTs with perfect end-contact, tunnelling effects will be strongly enhanced and all walls are assumed to be connected.

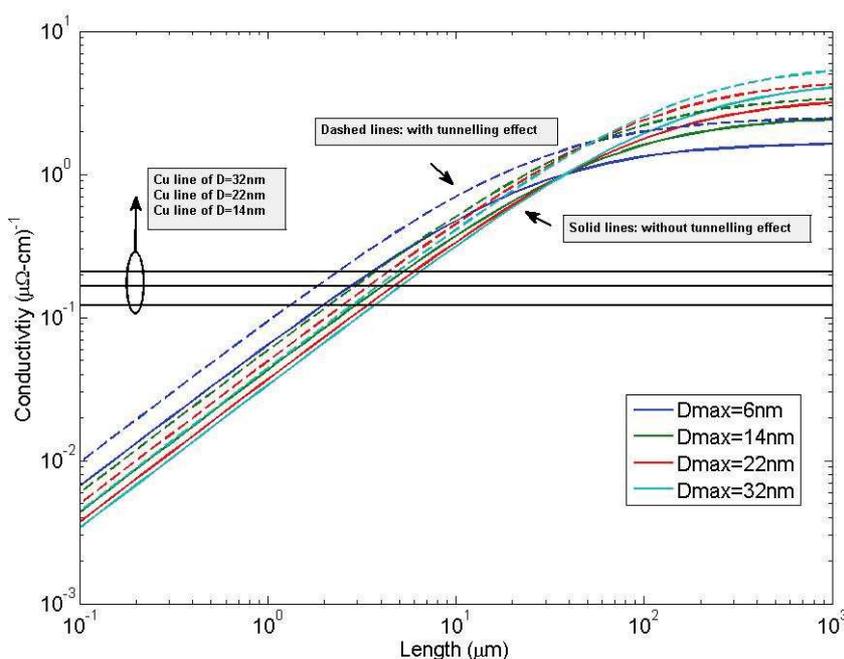


Figure 2.5: MWCNT conductivity with and without tunnelling effect.

### 2.3.2 Pristine SW/MW CNT capacitance model

The capacitance of an isolated SWCNT is composed of two parts. Intrinsic quantum capacitance  $C_Q$  and electrostatic resistance  $C_E$  [20]. Quantum capacitance is defined by the capability of energy storing for a quantum material, which is mostly related to the number of conducting channels in this material. Equations 2.7 - 2.9 show the

mathematical formulas for  $C_Q$ ,  $C_E$  and total capacitance ( $C_{SWCNT}$ ) of an isolated pristine SWCNT.

$$C_Q = 4 \frac{2e^2}{h\nu_F} \quad (2.7)$$

$$C_E = \frac{2\pi\varepsilon}{\ln(\frac{H}{D})} \quad (2.8)$$

$$C_{SWCNT} = \frac{C_Q C_E}{C_Q + C_E} \quad (2.9)$$

$\varepsilon$  here is related to dielectric constant of the CNT surrounding environment. For a standalone SWCNT, length will be the main dominant factor for its capacitance.

For an individual pristine MWCNT, the total capacitance of MWCNT ( $C_{Q-MWCNT}$ ) is given as equation 2.10:

$$C_{Q-MWCNT} = L \cdot N_{channel} \cdot C_{Q,1-channel} \quad (2.10)$$

Theoretical value of quantum capacitance for 1 conducting channel is  $C_{Q-1channel} = 96.5 \text{ aF}/\mu\text{m}$  [20].

## 2.4 Sources of Variability on MWCNT

Relying on current CNT growth technology, it is difficult to have ideal pristine CNTs but often CNTs have defects, diameter, chirality variations. Additional, for interconnect application, connection of each shell of MWCNT to metal contacts is also an important variation. In the following sections, four sources of variations are considered. They are based on observations either from experimental measurements or atomistic-level simulations.

### 2.4.1 Diameter Variations

For MWCNT, both CNT diameter and number of shells can fluctuate during the fabrication process. Typically, the diameter variation of fabricated CNT shows a Gaussian or normal ( $N$ ) distribution [93, 8].

By the catalytic CVD method, MWCNT forests in our CONNECT project, which typically exhibit Gaussian distributed outermost diameters ( $D_{CNTmax}$ ) with relative variations of  $\sim 20\%$  (standard deviation = 20% of the mean  $D_{CNTmax}$ ), as shown in Fig. 2.6. However, preliminary experimental results suggest that if each catalyst nanoparticle is confined in a nanoscale via hole [93], the relative diameter variation of individually grown MWCNT can be reduced below 10%. It is believed that this variation, which includes both catalyst size variation and intrinsic CNT growth variation, can be further reduced by improving the nanoscale via hole fabrication process. In this work, to trade off the current achieved diameter variation data and possibly optimized results, we make the assumption that the  $D_{CNTmax}$  variation on MWCNTs is a Gaussian distribution with the  $\sigma_{D_{CNTmax}} = 15\%$  of the  $\mu_{D_{CNTmax}}$ , namely  $N(\mu_{D_{CNTmax}}, (15\% \times \mu_{D_{CNTmax}})^2)$ . The 15% relative variation is

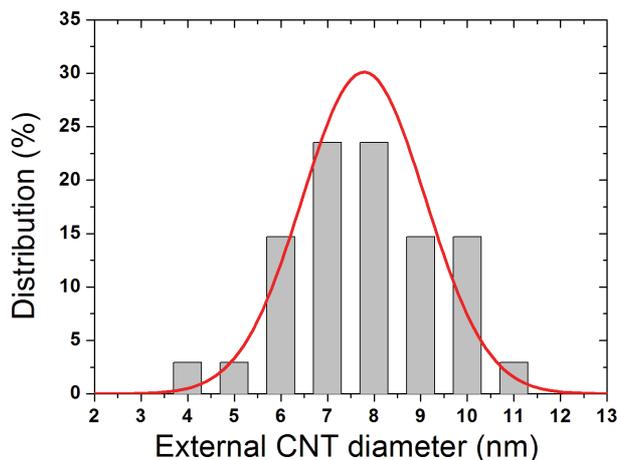


Figure 2.6: Experimental results of MWCNT  $D_{CNTmax}$  variation. Mean and standard deviation of  $D_{CNTmax}$  are 7.8 nm and 1.6 nm, respectively.

an average of the current obtained 20% and the potentially optimized 10% relative variation aforementioned. Furthermore, the total number of CNT shells is  $p$  and each shell diameter is  $D_{CNTi}$ , which are calculated by taking that the shell-to-shell distance is the van der Waals gap  $d = 0.34$  nm and  $D_{CNTmin}/D_{CNTmax} = 1/2$ , in which  $D_{CNTmin}$  and  $D_{CNTmax}$  are the innermost and outermost CNT shell diameters respectively [91], as shown in Equations (2.11) and (2.12) below where “Floor[]” means only the integer part is taken into account.

$$p = 1 + \text{Floor} \left[ \frac{(D_{CNTmax} - D_{CNTmin})}{2d} \right] \quad (2.11)$$

$$D_{CNTi} = D_{CNTmax} - 2d(i - 1), \quad 1 \leq i \leq p \quad (2.12)$$

To support the analytical formulation, we incorporated high-resolution TEM analysis of CNTs from our partners in the project. There are 38 growth experiments were realized by our partners under various conditions (catalyst thickness, sample temperature, pressure, hot filament temperature) to grow CNTs with different structures. A systematic TEM analysis was performed, and the diameter and number of shells of about 60 CNTs were measured for each growth condition (i.e., 2300 different CNTs were measured in total). Experimental results on numbers of shells for MWCNT and calculation results based on Equation (2.11) are presented in Fig. 2.7. It should be highlighted that Fig. 2.7 does not represent the variability of CNT structures for a given growth process but instead illustrates the overall trend observed for hot filament CVD-grown MWCNTs. A similar trend was also reported for thermal CVD grown MWCNTs [33]. From Fig. 2.7, we can tell that Equation (2.11) is accurate when  $D_{CNTmax}$  is around 11 nm and the equation over-estimates and under-estimates the number of shells before and after  $\sim 11$  nm  $D_{CNTmax}$ .

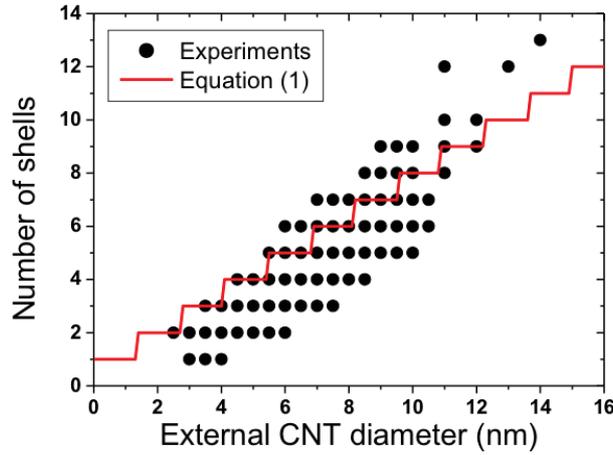


Figure 2.7: Experimental results of numbers of shells for MWCNTs of different outermost (external) diameters. Also shown are the calculation results of Equation (2.11).

## 2.4.2 Defect Occurrence

Experimental results show that defects in CNT could severely degrade CNT electrical properties through conductivity reduction [18]. In this chapter, we use vacancy defect as a representation of all defects by assuming that other types of defects may have a similar impact on CNT resistance. Vacancy defect density will be varied to assess the effect of defect density on MWCNTs.

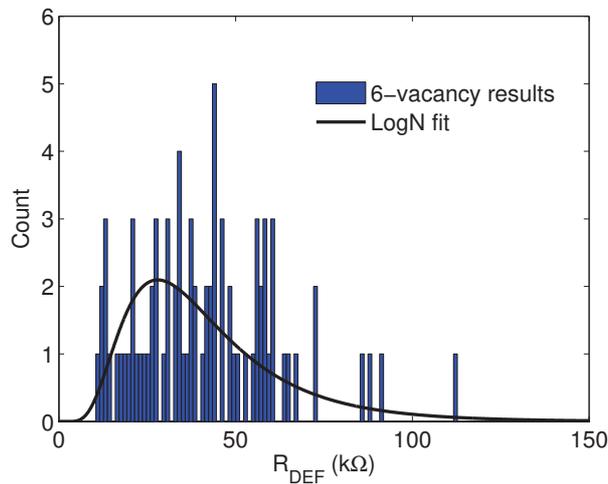


Figure 2.8: Atomistic-level simulation results of defect-induced resistance of a SWCNT (24, 0) with 6 vacancies. The SWCNT length is set to be about 42 nm corresponding to a vacancy density of 0.143 /nm. Also shown is the corresponding LogN fit result.

Atomistic-level simulations [85] show that vacancies in a SWCNT induce resis-

tance fluctuation behaving like an Ohmic-like principle, which is proportional to the defect density. Furthermore, due to the statistical distribution of vacancies inside the SWCNT, the resistance induced by the defects  $R_{Def}$  can be fit by a Lognormal (LogN) distribution with mean and standard deviation  $10.5117 \Omega$  and  $0.5226 \Omega$ , respectively (i.e.  $\ln(R_{Def}) \sim N(10.5117, 0.5226^2)$ ) as shown in Fig. 2.8. In this chapter, we assume that defect-induced resistance variation complies with a LogN distribution with the ratio of LogN parameters mean and standard deviation being  $0.5226/10.5117 = 0.0497$ . For different defect densities, the average of  $R_{Def}$  (Equation (2.15)) can be used to calculate LogN mean value of  $R_{Def}$  [61]. In this way, the LogN distribution of  $R_{Def}$  can be obtained under different defect densities.

### 2.4.3 CNT Chirality

Without any particular separation technique, in theory, the probability of a fabricated CNT to be metallic (semiconducting) is  $1/3$  ( $2/3$ ) [166]. For a MWCNT, the chirality of each shell is also statistically distributed. CNT chirality plays an essential role on CNT parasitics and ultimately its performance [104]. Up to date, there are no experimental data available for distribution of chirality of shells in MWCNT even though chirality can statistically fluctuate during the CNT growth process. In this chapter, the chirality of each shell in a MWCNT is assumed to be independent and comply with a Bernoulli distribution (or 0-1 distribution) with each shell of  $1/3$  (or  $2/3$ ) probability to be metallic (or semiconducting).

### 2.4.4 Shells Connection to Contacts

A good contact between CNTs and metal electrodes ensures a low resistance. Due to multiple shells in MWCNT, it could happen that some of the shells (i.e., inner shells) may not be connected to the contact. Disconnected shells do not contribute to the overall MWCNT conductance and can detriment its performance. Each CNT shell resistance  $R_i$  is shown in Equations (3.9) and (3.10) [91].  $R_Q$ ,  $N_C$  and  $\lambda_i$  represent quantum resistance, number of conducting channels and mean free path (MFP) in the CNT shell  $i$  respectively.  $h/2e^2 \sim 12.9 \text{ k}\Omega$  and  $L$  is the CNT shell length. As shown in these equations, the scattering-induced shell resistance  $R_{Si}$  is inversely proportional to the CNT shell diameter  $D_{CNTi}$ , which means the outer CNT shells have lower resistance than the inner shells. Thus, the MWCNT electrical performance is more susceptible when outer shells are disconnected rather than the inner shells. The calculation of  $N_C$  at different shell diameters for both metallic and semiconducting CNTs is based on a Transmission Coefficients method [140], which is detailed in chapter III 3.2.4.

$$R_i = R_Q + R_{Si}L = \frac{h}{2e^2 N_{Ci}} + \frac{h}{2e^2 N_{Ci}} \frac{L}{\lambda_i} \quad (2.13)$$

$$\lambda_i \approx 1000 D_{CNTi} \quad (2.14)$$

In this chapter, we consider various scenarios of disconnected shells from contacts. On a  $p$ -shell MWCNT (i.e., the total number of shells is  $p$ ), different shell numbers

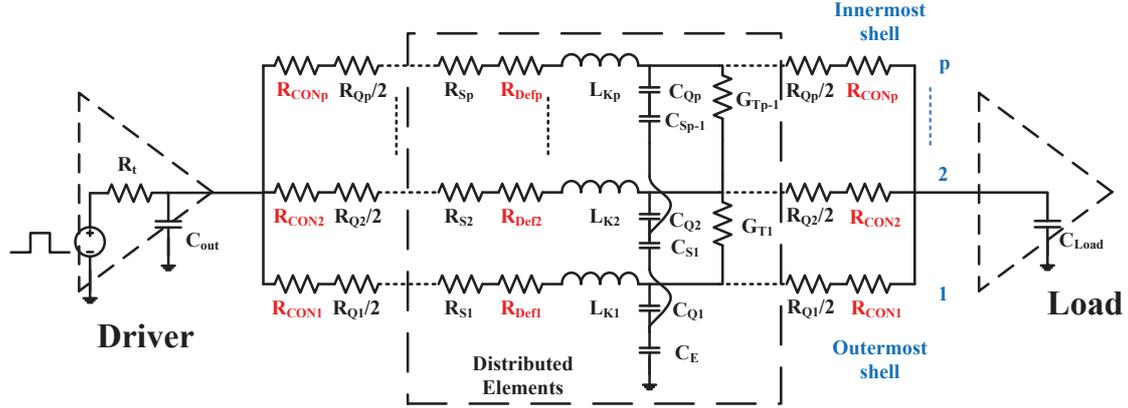


Figure 2.9: Enhanced distributed  $p$ -shell MWCNT compact model proposed in this chapter based on the original compact model by [91]. New parameters are contact resistance  $R_{CON}$  and defect-induced resistance  $R_{Def}$  in each shell. Except  $R_{CON}$  and lumped quantum resistance  $R_Q$ , each shell has intra-shell distributed parameters including  $R_{Def}$  and scattering resistance  $R_s$ , kinetic inductance  $L_K$ , and quantum capacitance  $C_Q$ . Inter-shell parameters include tunneling conductance  $G_T$  and shell-to-shell capacitance  $C_S$ . Intra-shell parameters have  $p$  components while inter-shell parameters have  $p-1$  components. Only the outermost shell has electrostatic capacitance  $C_E$  with the ground.  $R_t$  and  $C_{out}$  are the effective resistance and output capacitance of the driver, respectively, and  $C_{load}$  is the input capacitance of the load [91].

ranging from 1 to  $p$  can be disconnected from the contacts. Depending on the number of shells disconnected and their locations, the MWCNT performance will vary accordingly. For  $n$  shells disconnected, the largest performance degradation of MWCNT corresponds if the outermost  $n$  shells are disconnected while the least performance degradation corresponds if the innermost  $n$  shells are disconnected. For example, if the shells from the outermost to the innermost are labeled as 1, 2,  $\dots$ ,  $p$ , then the disconnections of 1, 2,  $\dots$ ,  $n$  shells correspond to the *worst case* of MWCNT performance degradation. Meanwhile, the disconnections of the  $p$ ,  $p-1$ ,  $\dots$ ,  $p-n+1$  shells correspond to the *best case* of performance degradation due to disconnection of  $n$  shells. Any other combinations of disconnected  $n$  shells degrade the MWCNT performance by an amount in between the *worst* and *best* cases.

## 2.5 Enhanced MWCNT Model

### 2.5.1 Original MWCNT Distributed Compact Model

The original distributed MWCNT compact model of  $p$ -shell was proposed by [91]. Calculations of each parameter can be referred to [91] including intra-shell parameters such as scattering resistance  $R_S$  and inter-shell parameters such as shell-to-shell

capacitance  $C_S$ . Deriving the number of shells and diameter of each shell is shown in Equations (2.11) and (2.12).

## 2.5.2 Enhanced MWCNT Distributed Compact Model

Based on the original model, we develop an enhanced distributed MWCNT compact model considering defects and contact resistances as shown in Fig. 2.9. In the enhanced distributed model, the defect-induced resistance of each shell is distributed uniformly in the shell similar to the scattering CNT resistance. Different from the original model, the contact resistance of each shell is included which is diameter dependent. Furthermore, in the enhanced distributed compact model, the contribution of semiconducting CNT shells to the MWCNT overall performance is ignored. This is because the conductance of semiconducting CNT shells is several orders less than that of metallic CNT shells and thus negligible. Besides, the contact resistance between a semiconducting CNT and electrode is also several orders larger than the contact resistance between a metallic CNT and electrode.

### Defect Resistance

In [85], atomistic-level simulations showed that vacancy-type defects induced resistance  $R_{Def_i}(\Omega)$  in metallic CNTs is on average proportional to the defect density  $N_{Def_i}$  (/nm) and is inversely dependent on the shell diameter  $D_{CNT_i}$  (Å) as shown in Equation (2.15), where  $L$  is the CNT shell length. It should be noted that  $R_{Def}$  is introduced to represent the impact of defects on the resistance of MWCNT and it could physically result from an increase in  $R_s$  [85]. This defect-induced resistance is distributed uniformly along each MWCNT shell as shown in Fig. 2.9. Furthermore, we assume that the density of defect vacancies is not dependent on the diameter of each shell. As a result,  $N_{Def_i}$  is the same for each shell and the difference of  $R_{Def_i}$  between each shell results from their diameter difference.

$$R_{Def}(N_{Def_i}, D_{CNT_i})_i = 2.67 \times 10^5 \times N_{Def_i} \times L \times D_{CNT_i}^{-1.27} \quad (2.15)$$

### Contact Resistance

Atomistic-level simulations were performed by our partners for a metallic armchair CNT with Density Function Theory (DFT) [19], [139]. The simulation temperature is fixed at 300 K. After fitting the atomistic-simulation data, we obtain that end-contact resistance of Pd-SWCNT is inversely dependent on the cross-sectional area of SWCNT as shown in Fig. 2.10, although different slopes are found and some fluctuation exists. We believe that the fluctuation is due to discretization of atom positions during DFT simulation, which leads to diameter dependent variation. For large diameters (such as diameter  $D_{CNT} = 0.8 \text{ nm} \sim 1.3 \text{ nm}$ ), a good linear fit is obtained by setting the reciprocal of CNT area ( $A_i$  (nm<sup>2</sup>)) as a variable while contact resistance  $R_{CON_i}$  changes with it. We obtain the coefficient of determination

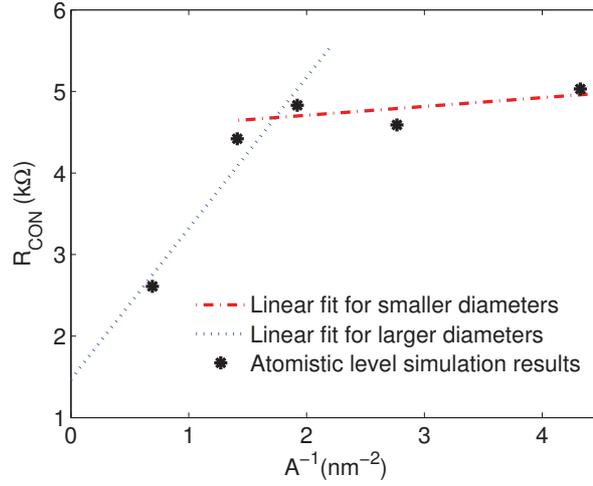


Figure 2.10: Dependence of Pd-SWCNT end-contact resistance on cross-sectional area of SWCNT.

$R^2 = 0.9384$ . As we study MWCNT with shell diameter  $\geq 1$  nm, it is reasonable to use the linear fitting results for large diameters by extrapolation and derive the end-contact resistance as in Equation (2.16).

$$R_{CON_i} = 1.8514A_i^{-1} + 1.4685 \quad (\text{k}\Omega) \quad A_i = \frac{\pi D_{CNT_i}^2}{4} \quad (2.16)$$

Although, the equation is based on the metallic armchair SWCNT simulation, the metallic zigzag CNT is assumed to have an identical contact resistance with Pd for the same shell diameter. Furthermore, the MWCNT contact resistance can be computed by considering each MWCNT shell as a SWCNT. Thus, according to this equation, the contact resistance of each shell can be calculated and introduced at the two contact-ends as shown in Fig. 2.9.

### 2.5.3 Enhanced MWCNT Lumped Compact Model

To simplify the enhanced distributed MWCNT compact model, we develop a respective lumped model as shown in Fig. 2.11. Compared with the distributed model in Fig. 2.9, the lumped model replaces the distributed parameters such as  $R_S$  with lumped parameters by multiplying the distributed values with the MWCNT length. Tunneling parameters and shell-to-shell capacitance are eliminated as they are relatively negligible. Circuit level simulations using the simulation setup in Section 2.6 show that for local interconnect application (such as MWCNT length  $\leq 20$   $\mu\text{m}$ ) the lumped model represents well the distributed model without any accuracy loss but significantly improves simulation efficiency. Thus, in our following simulations, we use the lumped model.

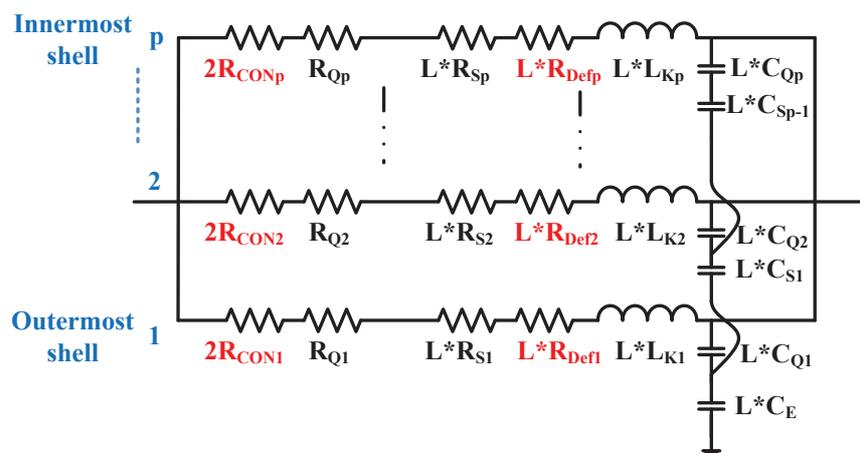


Figure 2.11: Enhanced lumped  $p$ -shell MWCNT compact model proposed based on the enhanced distributed compact model in Fig. 2.9. Driver and load are not shown for clarity.

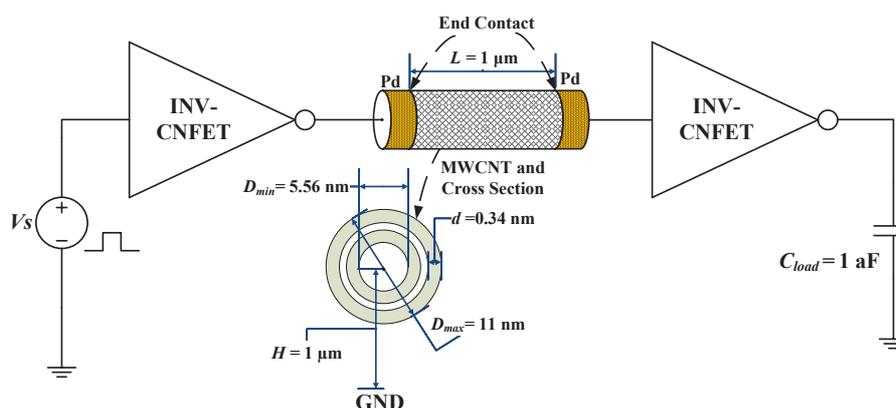


Figure 2.12: Simulation setup schematic of MWCNT as an interconnect. MWCNT connects two inverters composed of CNTFET devices.

## 2.6 MWCNT Variability Evaluations

### 2.6.1 Simulation setup

The simulation setup schematic is shown in Fig. 2.12. The circuit benchmark consists of two inverters connected through either an ideal wire or a MWCNT interconnect. Inverter gates are built with carbon nanotube field effect transistors (CNTFETs), but other types of devices can also be used. Here, we use CNTFETs as devices with MWCNT interconnects to assess the performance benefits of a possible all carbon-based technology. We use CNTFET compact models proposed by [81]. The key parameters of both N-type and P-type CNTFET are 11.7 nm, 1  $\mu\text{m}$ , 10 nm for gate length, gate width and the distance between CNTs underneath the gate region, respectively. Other parameters are the default values recommended by [81]. The input stimulus is a square wave of 5 ps rising and falling time. The

period of the square wave is 100 ps. The supply voltage is 0.7 V. The delay, power consumption, and product of power and delay (PDP) of the MWCNT interconnect are calculated by subtracting from the circuit respective values with an ideal connection from those with MWCNT interconnect. The outermost MWCNT diameter  $D_{CNTmax}$  is 11 nm with length  $L$  of 1  $\mu\text{m}$ .

We perform Monte Carlo (MC) simulations for diameter, defects, chirality and all-sources variations. The all-sources variation refers to the case that diameter, defects and chirality variations are simultaneously considered. The diameter, defect and chirality variations are randomized respectively as follows:  $D_{CNTmax}$  (Gaussian distribution  $N(11 \text{ nm}, 1.65^2 \text{ nm}^2)$ ),  $R_{Def}$  (LogN distribution,  $\ln(R_{Def}) \sim N(\mu_{LogN}, (\mu_{LogN} \times 0.0497)^2)$ ),  $\mu_{LogN}$  can be calculated based on the mean of  $R_{Def}$  in Equation (2.15), and each CNT shell chirality (0-1 distribution, 1/3 to be metallic). The all-sources variation has the above all parameters randomized simultaneously. For each run of MC simulation, 1000 samples are collected to obtain a reasonable confidence level for the respective simulation results. Defect density in the MWCNT is assumed to be 10 defects per  $\mu\text{m}$  (10 / $\mu\text{m}$ ) for each shell of MWCNT by default. The chirality variation that may generate all semiconducting MWCNT shells ( $\sim 2.6\%$  probability) can make MWCNT interconnect non-conducting and is thus not considered in the following simulation results.

## 2.6.2 Diameter, Defects, Chirality and All-sources Variations

Results of MWCNT resistance variations are shown in Fig. 2.13 (a)-(d). For each source of variation, distributions of delay, power, and power-delay-product (PDP) are found to be similar to their respective resistance variation and are thus not shown in detail. The similarity is due to the relatively negligible influence of MWCNT capacitance variation on these performance because MWCNT capacitance is  $\sim 3$  orders smaller than the inverter parasitic capacitance (found by DC parasitic parameters extraction). Diameter variations can lead to either an increase or a decrease in the number of the MWCNT shells, which also makes MWCNT conductance change discretely as in Fig. 2.13 (a). There are nine clusters in diameter variation which also corresponds to the total number of shells. Chirality variation is not continuous resulting from different combinations of metallic and semiconducting CNT shells in the MWCNT. Because metallic and semiconducting shells have significantly different conductance, chirality variation is significant as shown in Fig. 2.13 (c). Defect and all-sources variations continuously change MWCNT conductance as shown in Fig. 2.13 (b) and (d).

We find that LogN distributions can fit different sources variations. MWCNT resistance for diameter variation is not symmetrically varied around its mean value despite the Gaussian distribution of diameter variation as the change of resistance with decreasing diameters is larger than the change of resistance with increasing diameters. The chirality variation is also varied asymmetrically due to the asymmetrical variation of the portion of metallic CNT shells in MWCNT. Defect variation complies also with a LogN distribution due to the input of LogN distributed defect-induced resistance. The all-sources variation is impacted by these three sources of

variations and also shows a LogN type distribution as in Fig. 2.13 (d).

Additionally, we show mean ( $\mu$ ) and standard deviation ( $\sigma$ ) of MWCNT resistance for each source variation in Fig. 2.13 (a)-(d). We observe that the chirality is the most dominant source of variation, then diameter variation followed by defects as the least dominant source of variation. This can also be seen in Fig. 2.14 (a)-(d) where the fitted probability density functions (PDFs) of each source of variation for resistance, delay, power and PDP are presented. The reason why chirality variation dominates is that chirality variation changes the portion of metallic CNT shells from  $\sim 0$  to  $\sim 1$ , and hence significantly impacts resistance and performance of MWCNT. Diameter variation is also large because  $D_{CNTmax}$  not only impacts  $N_C$  but also influences the contact resistance and defect-induced resistance.

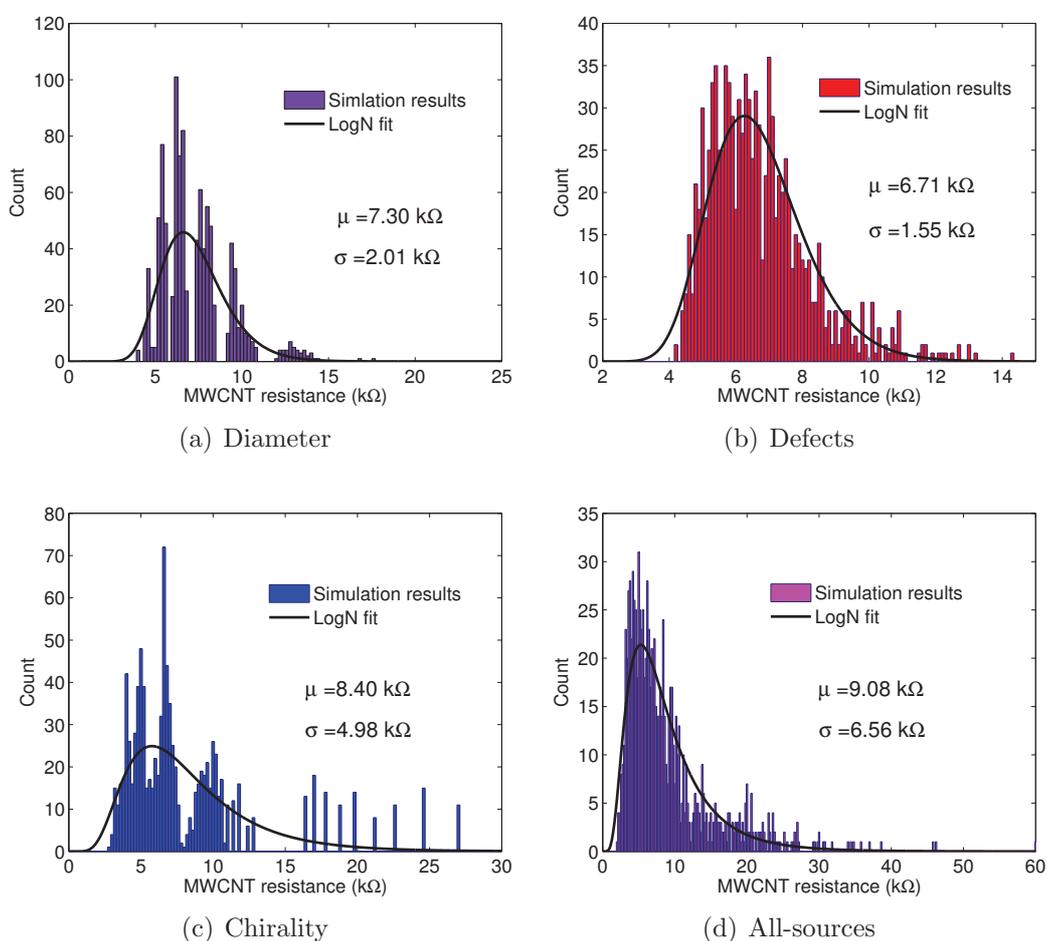


Figure 2.13: (a)-(d) are distributions of resistance variation of the pristine MWCNT interconnect with input diameter, defects, chirality and all-sources variations respectively.

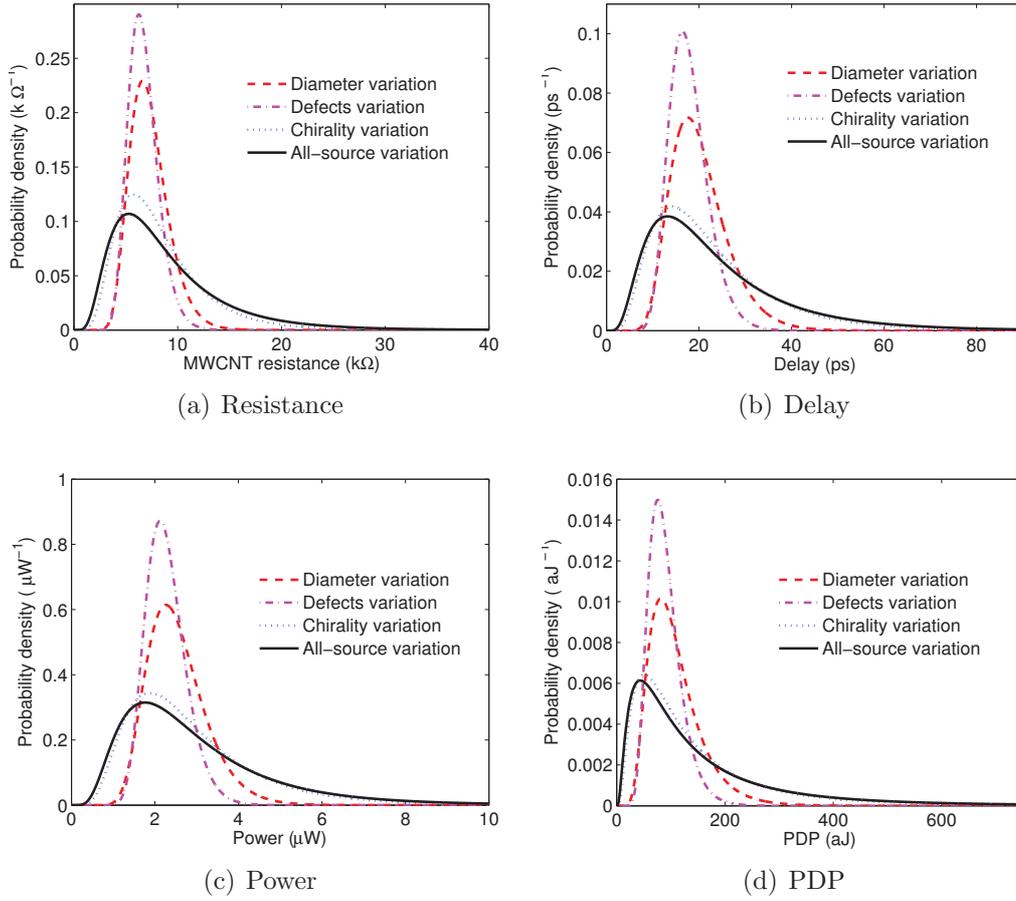


Figure 2.14: (a)-(d) are PDFs of resistance, delay, power and PDP of the pristine MWCNT interconnect respectively with input diameter, defects, chirality and all-sources variations.

### 2.6.3 Impact of Defect Density

To investigate further the impact of defects, we vary defect densities ranging from  $5/\mu m$  to  $100/\mu m$ . Please note that in previous subsection the defect density was set to  $10/\mu m$ . As shown in Fig. 2.15,  $\mu$  and  $\sigma$  of MWCNT resistance for each source of variation are increased linearly with defect density at slightly different rates. The increase in defect density leads to larger metallic CNT resistance and further the  $\mu$  of MWCNT resistance. The increase in defect resistance  $\sigma$  with defect density is as expected while the increase in diameter resistance  $\sigma$  can be explained by Equation (2.15) where defect-induced resistance is dependent on both diameter and defect density. Additionally, the chirality variation  $\sigma$  increases as each shell resistance increases with defect density.

The  $3\sigma$  percentage variation ( $3\sigma/\mu \times 100\%$ ) (or relative variation) [115] for each variation source also increases with defect density at different rates particularly for small defect densities ( $5/\mu m - 50/\mu m$ ), as shown in Fig. 2.15. We observe that defect variation starts to surpass diameter variation for defect density of  $\sim 15/\mu m$ ,

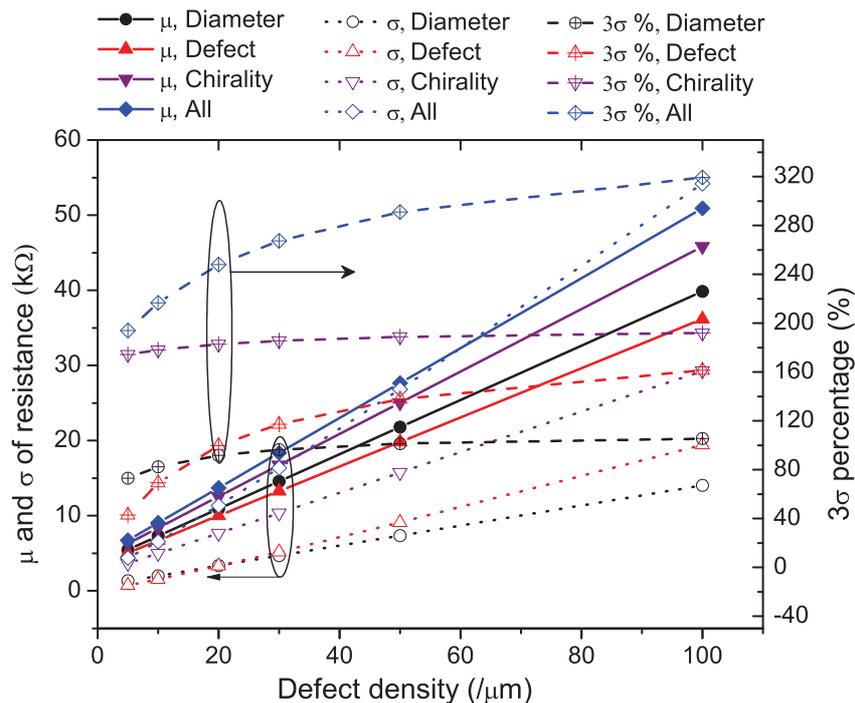


Figure 2.15: Change of resistance while varying defect density on pristine MWCNT interconnects with diameter, defect, chirality and all-sources variations.

but they are still less significant than the chirality variation. As defect density continues to increase, the  $3\sigma$  percentage variation seems to saturate for different sources of variations. As a result, the chirality variation remains the most dominant source. Such observations suggest that chirality is the most dominant source of variations among all sources despite the large defect density.

#### 2.6.4 Improvement on MWCNT Variations

Here, we investigate the scenario of an improved CNT growth method that can reduce MWCNT process variations. We consider improvements in defect and diameter variability whereas chirality variability remains unchanged as there is no trivial method to control chirality during growth. We investigate resistance variability as shown in Fig. 2.16 with different improvement levels of diameter and defect variations. The x-axis indicates the percentage improvement in both defect density and diameter variability. We observe that resistance  $\mu$ ,  $\sigma$  and  $3\sigma$  percentage are reduced with the improvements on defect and diameter variability. However, the  $3\sigma$  percentage for chirality variation remains almost unchanged. This is because the resistance  $\mu$  and  $\sigma$  of chirality variation change at the same pace with the variability improvement. We notice, that when the percentage improvement reaches around 80%, the chirality variation starts to be almost the only source of variation. We deduce that if process variations (such as diameter and defect) can be well controlled and reduced, then the chirality will be the only source of MWCNT variation that limits the improvement of MWCNT variability.

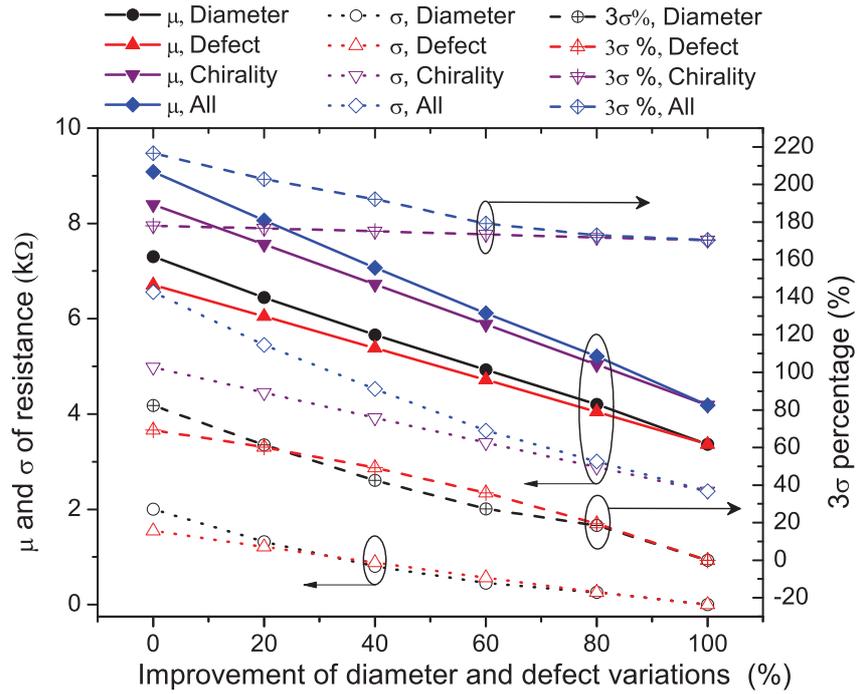


Figure 2.16: Minimizing resistance variation of the pristine MWCNT interconnect by reducing the contribution of diameter and defect variations.

### 2.6.5 MWCNT Shell to Contact Variations

As described in Section 2.4, we also investigate the connectivity between MWCNT shells and contacts. Good contacts between shell and metal electrodes are essential for achieving a low resistance contact. In this chapter, we studied as example case that MWCNT interconnect has up to nine shells. We study the cases where the number of shells  $n$  ranging from zero to nine can be disconnected from metal electrodes, which can lead to resistance variations and performance degradations. The case of all nine shells disconnected to contact would lead to conduction failure and is not considered here. Simulation results in Fig. 2.17 show the MWCNT resistance, delay, power and PDP with respect to the number of disconnected shells. We observe significant (more than one order of magnitude) increases in resistance and performance degradations as the number of disconnected shells increases, especially for PDP. Depending on the positions of the disconnected shells (such as innermost or outermost), the performance degradation is also different. There are the best and the worst cases of performance degradation, which corresponds to all  $n$  innermost shells disconnected and all  $n$  outermost shells disconnected, respectively. We find that the difference between the two extreme cases gets larger with the number of disconnected shells.

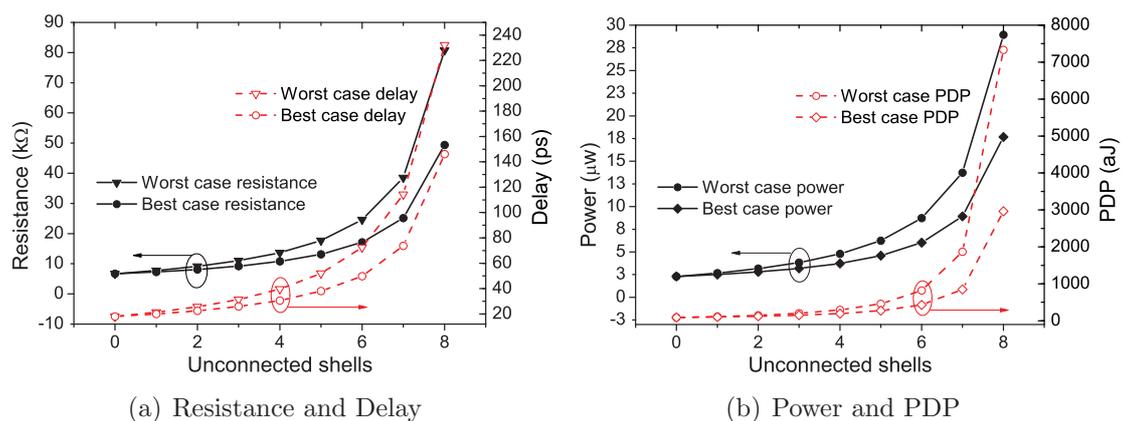


Figure 2.17: Change of (a) resistance and delay, (b) power and PDP of MWCNT with disconnected CNT shells from contact. In this example, there are total nine shells in the MWCNT.

## 2.7 Conclusion

In this chapter, we provide firstly physical description on pristine CNTs electrical properties and present the widely used models in the literature to be our starting foundations. Secondly, an enhanced compact model of MWCNT interconnect is presented where diameter dependent contact resistance and defect-induced resistance for each MWCNT shell are included. Based on the proposed enhanced compact model, MWCNT interconnect resistance and performance variations (including delay, power, and PDP) are analyzed including variations on diameter, defect densities, chirality, and shell-to-contact connectivity. We identify that the diameter, defects, chirality, and all-sources variations all produce Lognormal resistance and performance distributions. We find that defect variation is increased with defect density at a larger rate than diameter variation and surpasses diameter variation at defect density of  $\sim 15 / \mu\text{m}$ . The chirality variation is always the most dominant source of variation even at large defect densities. We also consider the case of significantly reduced MWCNT diameter and defect variations due to improving the quality of MWCNT growth, where the chirality remains as the only source of variation.



# Chapter 3

## Doping of Carbon Nanotubes

### 3.1 Introduction

Atomically thin, ballistic transport, large electron MFP and highly conductive carbon-based materials such as carbon nanotubes (CNTs) provide compelling advantages for the next generation of on-chip interconnects [146, 147]. CNTs are also listed as one of the future materials for advanced technology nodes based on IRDS 2017 report [2]. There are different types of CNTs, single-wall (SW) and multi-wall (MW), according to the number of carbon shells. Different shell rotation indicates the chirality property of shells as either semiconducting or metallic CNTs. Stand-alone metallic CNTs are good candidates for advanced low dimensions interconnect applications [37]. However, individual metallic SWCNT is limited by the intrinsic quantum resistance ( $\sim 6.45 \text{ k}\Omega$ ) [53, 164] for lengths longer than its MFP, hence the total resistance further increases with phonon scattering [105]. Moreover, using a single shell as interconnect is prone to connections issues during the fabrication process, defects, and highly resistive contacts, thus, overall they can be less reliable. Consequently, multi-wall CNTs (MWCNT) with numerous parallel shells are considered to enhance the CNT conductivity by increasing the number of possible conducting paths. For interconnect applications, it is essential that shells are metallic to obtain high conductivity, hence, raises the importance of MWCNT chirality control.

Doping of MWCNT can be a suitable solution to overcome the random shell chirality. MWCNT semiconducting shells can be converted to metallic-like behavior through doping. Furthermore, the resistance of CNT interconnects can be reduced by applying doping such as charge transfer internal or external doping. Doping improves CNT conductivity through the Fermi level,  $E_f$  shift to increase the density of charge carriers (by either holes for p-type doping or electrons for n-type doping) [183, 96, 109, 175]. It was also experimentally demonstrated that doping could improve CNT conductivity regardless of CNT diameter and type (either metallic or semiconducting) as in [183]. In [60], it was shown that the addition of MoOx, which forms a composite material with CNT, makes the improved conductivity of doped CNT stable in air at the temperatures up to 390 °C. Similar stable doping has also been achieved by utilizing a single electron oxidant to efficiently dope CNT films by [27].

However, the BEOL processing of CNTs is not yet streamlined or CMOS compatible. CNTs require much higher temperature (up to 900 °C) compared to Cu [121] to achieve good quality CNT growth. Nevertheless, to achieve CMOS BEOL process compatibility, CNTs need to grow at lower temperatures such as 450 °C to 500 °C. However, at such temperatures CNTs have many defects, variations in diameter and chirality, which currently limit the practical application of CNTs as BEOL interconnects. Contacts are also a serious challenge for both reliability (good contact) and performance (high resistance). Metal electrodes might not be connected to all MWCNT shells, which detracts MWCNT interconnect performance.

While there is an extensive body of work on various methods for doping CNTs, there is not yet a systematic study of doping impact on MWCNT interconnects and their variability. Doping is capable of changing semiconducting CNTs into metallic CNTs concerning their electrical performance, and thus it is possible to reduce chirality variation and overall MWCNT resistance variation. In [93], we showed by atomistic-level simulation and experimental results how doping alters CNT chirality. However, there is still a need for further investigations to understand the impact of doping in the presence of various sources of variations such as defects, diameter, chirality, and connectivity.

In this Chapter, we evaluate MWCNT interconnects performance and variability while considering the impact of doping. We introduce the parameter number of conducting channels ( $N_C$ ) to represent doping effect. Experimental doping process and electrical measurements are realized in our CONNECT project. We evaluate doping impacts from both our theoretical lumped compact model and experimental data. In addition, we incorporate  $N_C$  into our enhanced MWCNT compact model described in Chapter 2. By theoretically calculating  $N_C$  as a function of Fermi level shift  $E_f$  - we evaluate each source of variation (diameter, chirality, defects) and all-sources using Monte Carlo (MC) simulations. Simulation results are subsequently compared with experimental results, and a good consistency is found between them.

The contents in this Chapter have been published on:

[94]: **Jie Liang**, et al. "A physics-based investigation of Pt-salt doped carbon nanotubes for local interconnects." 2017 IEEE International Electron Devices Meeting (IEDM). IEEE, 2017.

[95]: **Jie Liang**, et al. "Investigation of Pt-Salt-Doped-Standalone-Multiwall Carbon Nanotubes for On-Chip Interconnect Applications." IEEE Transactions on Electron Devices (2019).

[30]: Rongmei Chen, **Jie Liang**, et al. "Variability Study of MWCNT Local Interconnects Considering Defects and Contact Resistances—Part II: Impact of Charge Transfer Doping." IEEE Transactions on Electron Devices 99 (2018): 1-8.

## 3.2 Electrical Compact Models

CNT interconnect electrical models have already been established by [141] and [91] where pristine SWCNTs and MWCNTs for on-chip interconnects were investigated. In contrast to these works, we consider modeling of charge-based doped MWCNT interconnects. We perform both atomistic- and circuit-level simulation to understand

the impact of doping on Fermi-level shift and MWCNT parasitics.

### 3.2.1 Doping of MWCNT

Doping of CNTs with electron donor (n-type)/acceptor (p-type) presents a practical solution to overcome variations on random chirality and shell variability in MWCNTs. Doping shifts the material Fermi-Level, thus enhancing metallic properties for semiconducting tubes and reducing the metallic tube resistivity by introducing additional electron transport channels. One doping mechanism of CNTs is substitutional doping. Substitutional doping introduces foreign atoms into carbon atom site either by removing an original carbon atom or filling into a default carbon vacancy. However, substitutional doping in CNTs forms a Bamboo-like morphological deformation [119] due to different atom lattice parameters, where more defects and variability sources can be additionally generated, which are not advantageous for on-chip interconnect applications. Another possible doping mechanism is through charge transfer doping. In this thesis, we investigate charge transfer doping as a viable method to control MWCNT chirality. In the charge transfer doping, dopants do not form covalent bonds, but rather Van der Waals interactions take place, hence there is no structural modification. Doping can be either n- or p-type, while due to interactions with the ambient environment, pristine CNTs behave lightly p-type doped [39], hence introducing a p-type dopant is practically more feasible. There exists various kinds of p-type dopant such as  $\text{NO}_2$ [75],  $\text{H}_2\text{SO}_4$  and  $\text{SOCl}_2$ [138], and the combination of  $\text{HNO}_3$  and  $\text{SOCl}_2$  [120], etc. [175]. Recently, iodine [180],  $\text{MoO}_3$ [49] and  $\text{PtCl}_4$  [43], [94] based p-type charge transfer doping have been presented. In this chapter, our models are based on  $\text{PtCl}_4$  charge transfer p-type doping.

### 3.2.2 Atomistic model - DFT Calculation

Density Functional Theory (DFT) simulations have been performed by our partners in the project, which is implemented in the Atomistix Tool Kit (ATK) [7] to investigate the electrical properties of Pt-salt doped CNTs. The generalized gradient approximation (GGA) is applied to the exchange-correlation energy function. We have compared the formation energies with atomic structures using  $\text{PtCl}_4$  as a dopant agent as shown in Fig. 3.1. When  $\text{PtCl}_4$  is located inside the CNT (Fig. 3.1 (b)), the structure is most stable. Fig. 3.2 (a) shows the band structure and density-of-states (DOS) of pristine and doped metallic CNT (15,0). It is found that Pt-salt is a good p-type dopant. Thanks to the Fermi-level ( $E_f$ ) shift, the doped CNT has a larger DOS near  $E_f$ . The band structure and DOS of the semiconductor CNT (16,0) are shown in Fig. 3.2 (b). Due to  $E_f$  shift, the semiconductor CNT can have a metallic behavior. The value of  $E_f$  shifts in double-wall CNTs (DWCNTs) is also calculated, and the results are shown in Table 3.1. To summarize, doping of CNTs reduces the chirality variability of shells by degenerating semiconducting shells, which acquire metallic properties.

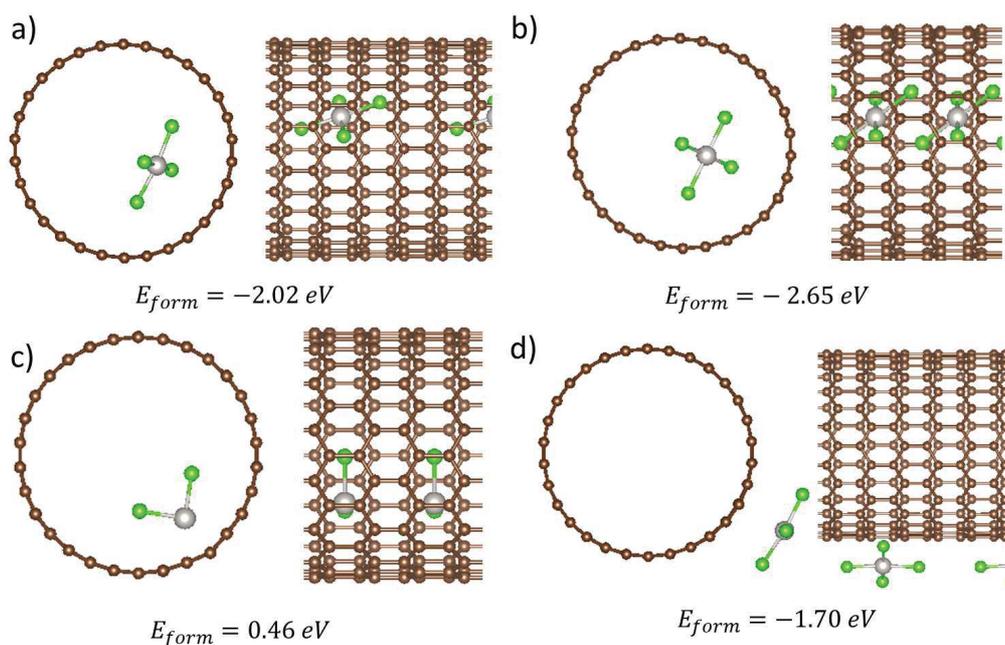


Figure 3.1: Comparison of the formation energy ( $E_{form}$ ) for the  $\text{PtCl}_4$  doped  $\text{CNT}(15,0)$ . Grey, white, and green spheres are carbon, platinum, and chlorine, respectively [93].

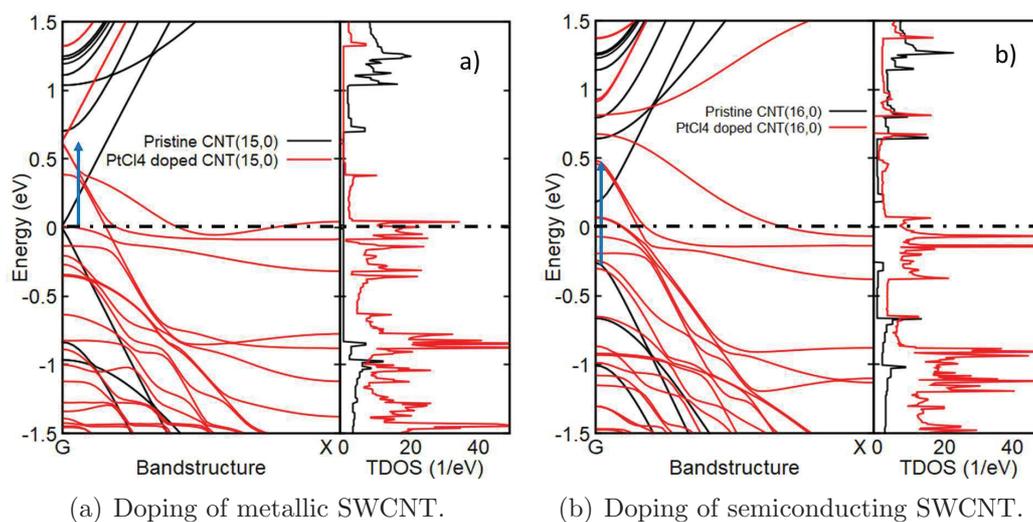


Figure 3.2: Band structure and total DOS of pristine and  $\text{PtCl}_4$  doped (a)  $\text{CNT}(15,0)$  (See Fig 1. b)). Fermi-level ( $E_f$ ) is set to 0.0 eV. Due to the dopant,  $E_f$  is shifted by -0.6 eV, and DOS near  $E_f$  has increased. (b)  $\text{CNT}(16,0)$ .  $E_f$  shifts by dopants, semiconductor  $\text{CNT}(16,0)$  has become a metal [93].

Table 3.1: Summary of  $E_f$  shift of double-wall CNTs (DWCNTs).  $E_f$  shift is calculated based on the valence band edge [93].

	Fermi-level shift (inner shell)	Fermi-level shift (outer shell)
CNT(15,0)(24,0),MM	0.509 eV	0.444 eV
CNT(15,0)(25,0),MS	0.554 eV	0.502 eV
CNT(14,0)(24,0),SM	0.586 eV	0.503 eV
CNT(14,0)(23,0),SS	0.556 eV	0.428 eV

M and S indicate the metallic and semiconducting of each shell respectively.

### 3.2.3 Electrical RC model

#### Number of conducting channels

Each MWCNT shell has a different number of conducting channels due to shell chirality and diameter. We introduce  $N_C$  to represent the number of conducting channels per shell and as a parameter for controlling chirality variability knowing that doping alters semiconducting shells to acquire metallic properties. The number of conducting channels per shell can be theoretically expressed as [89]:

$$N_C = \int T(E) f'(E_{occ}^i, E_f) dE / (k_B T) \quad (3.1)$$

$$f' = \frac{1}{e^{|E_{occ}^i - E_f|/k_B T} + 1} \quad (3.2)$$

where  $f'$  is the Fermi distribution function, which is used to evaluate the probability of electrons contributing to total CNT conductance.  $E_{occ}^i$  is the energy of highest occupied sub-bands below Fermi-level ( $E_f$ ),  $k_B T \sim 0.0258$  eV for  $T=300$  K. With doping, shifting of  $E_f$  can tune the energy distance to the occupied sub-bands  $E_{occ}^i$ , thus further increase the probability of electrons to contribute to electrical transport, hence more conducting channels are available with doping of CNTs. From analytical computations of Equation (3.1), we assume a pristine metallic shell with a diameter less than 10nm has two conducting channels,  $N_C = 2$ . After doping, when a semiconducting shell acquires a  $N_C \geq 2$ , we interpret such increase of conducting channels as a conversion of shell property from semiconducting to metallic [30]. To illustrate the relation between the number of conducting channels  $N_C$  and Fermi shift  $E_f$ , for a single semiconducting shell of 7 nm diameter, it requires 0.08 eV Fermi shift to convert the semiconducting shell to metallic behaviour (or reach  $N_C = 2$ ).  $E_f$  shifts of 0.2 eV and 0.198 eV are necessary for semiconducting and metallic shells (with  $D = 7$  nm) to reach  $N_C = 5$ , respectively.

**Doped MWCNT Resistance**

For a single conducting channel, its conductance is derived as:

$$G_{1channel} = G_0 / (1 + L/L_{MFP}) \quad (3.3)$$

where  $G_0$  is the quantum conductance ( $\sim 1/12.9 \text{ k}\Omega$ ) and  $L_{MFP}$  is the CNT electron mean free path. CNT mean free path depends on the CNT diameter and an experimental based derivation of CNT mean free path is provided in [91] as:

$$L_{MFP} \approx 1000D_{MWCNT} \quad (3.4)$$

Hence, the total doped MWCNT resistance  $R_{MWCNT}$  is derived as:

$$R_{MWCNT} = \frac{1}{N_C N_s G_{1channel}} \quad (3.5)$$

where  $N_s$  is the number of shells and is derived as *diameter-1* based on experimental statistical measurements [33].

**Doped MWCNT Capacitance**

CNT has quantum ( $C_Q$ ) and electrostatic capacitance ( $C_E$ ). Quantum capacitance per channel  $C_{Q/channel}$  is  $\sim 96.5 \text{ aF}/\mu\text{m}$  [91].  $C_Q$  depends on number of conducting channels ( $N_C$ ) and MWCNT shells ( $N_s$ ), as the CNT quantum capacitance refers to the capability of storing electron energy [20]. Doped MWCNT total quantum capacitance is derived as:

$$C_Q = N_C N_s C_{Q/channel} \quad (3.6)$$

$N_C$  linearly increases the total quantum capacitance.  $C_E$  is geometry dependent [91] and does not change with doping.

In Fig. 3.3, we show the resistivity of 7 nm diameter MWCNT with lengths up to 10  $\mu\text{m}$  while varying  $N_C$ . We compare the resistivity of copper (Cu) lines with line widths of 32, 22 and 14 nm [91]. We observe that doping improves CNT resistivity and achieves even lower resistivity than pristine CNTs and Cu lines. We notice that resistivity of pristine CNTs becomes advantageous to Cu lines for lengths beyond 3  $\mu\text{m}$ . With doping, CNTs become favorable at even shorter lengths, which indicates the suitability of doped CNTs for local short on-chip interconnects where Cu line performance significantly degrades with scattering. We obtain up to 90% improvement in resistivity with doping at  $N_C = 5$ , which applies as well on resistance improvement.

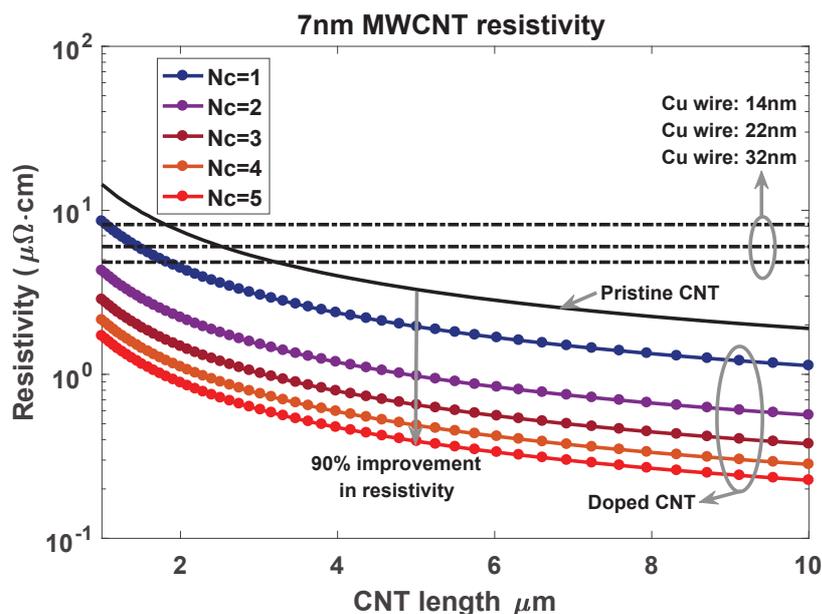


Figure 3.3: 7nm diameter MWCNT conductivity with different doping levels where the increase of  $N_C$  indicates more doping concentration).

### 3.2.4 Analytical Method for Computing the Impact of Doping

Here, we present the analytical method for computing the impact of doping on  $N_C$  via the Fermi level shift  $E_f$ . The band structure of a zigzag CNT with chirality of  $(m, 0)$  can be described by Equation (3.7) [140]:

$$E(k_x) = \pm \frac{3ta_0}{2} \sqrt{k_x^2 + \left( \frac{1}{D_{CNT}} \left( 2v - \frac{4}{3}m \right) \right)^2} \quad (3.7)$$

where  $D_{CNT}$  is the CNT diameter,  $k_x$  is the wave vector in the  $x$  direction,  $t$  is the hopping parameter,  $a_0$  is the carbon-carbon distance, and  $v$  is an integer less than  $m$ .  $E_f$  is assumed to be 0.0 eV for pristine zigzag CNT although manufactured CNTs tend to be slightly p-doped by the oxygen in the air under ambient conditions [102] and have some downshift of  $E_f$ . From Equation (3.7), we can calculate the transmission coefficients ( $T(E)$ ), and then  $N_C$  can be obtained as in Equation (3.8) [140]. It should be noted that the  $N_C$  of metallic armchair CNT can be calculated similarly [41].

$$N_C = \int T(E) f'(E, E_f) dE / (k_B T) \quad (3.8)$$

where  $f'$  is the derivative of the Fermi function,  $k_B$  is the Boltzmann constant, and  $T$  is the temperature.  $N_{C_i}$  of the CNT shell  $i$  in MWCNT modifies its intrinsic resistance  $R_i$  as Equations (3.9) and (3.10) [91] where  $h/(2e^2) \sim 12.9$  k $\Omega$  and  $R_{S_i}$ ,  $R_Q$  and  $\lambda_i$  represent scattering and quantum resistances, and mean free path (MFP)

of the CNT shell  $i$ , respectively.  $L$  is the MWCNT length.

$$R_i = R_Q + R_{Si}L = \frac{h}{2e^2 N_{Ci}} + \frac{h}{2e^2 N_{Ci}} \frac{L}{\lambda_i} \quad (3.9)$$

$$\lambda_i \approx 1000 D_{CNTi} \quad (3.10)$$

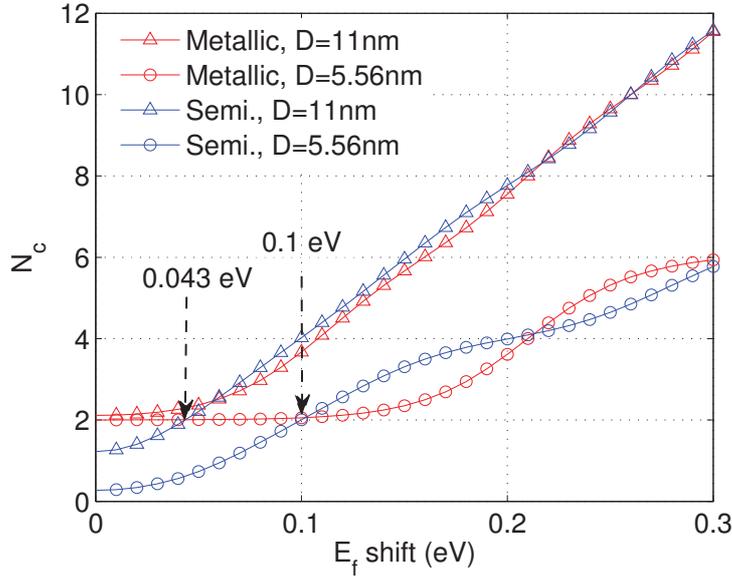
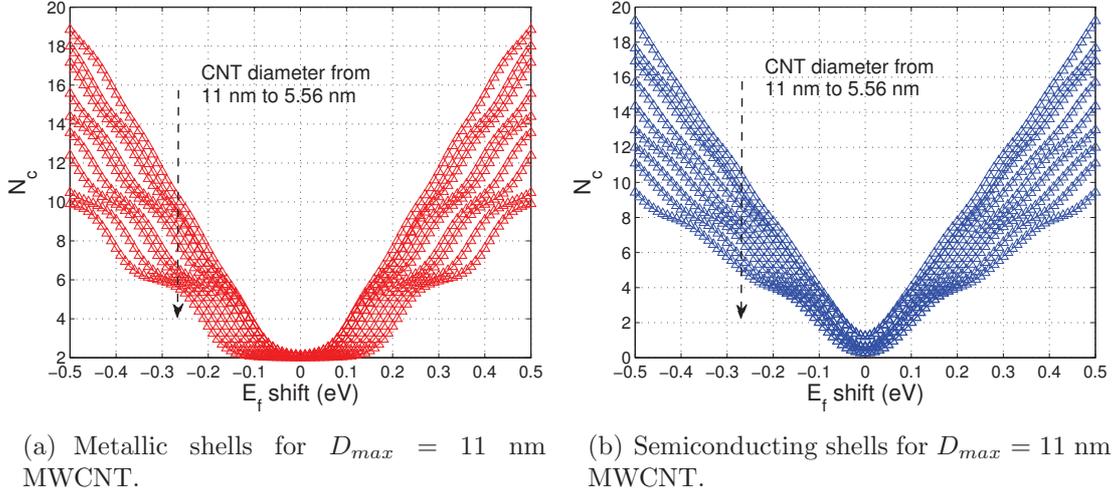


Figure 3.4: a)  $N_C$  of metallic shells and b)  $N_C$  of semiconducting shells with the  $E_f$  shift for the MWCNT with 11 nm outermost diameter, and c)  $N_C$  of metallic and semiconducting shells of the outermost (11 nm) and the innermost (5.56 nm) shells before and after the  $E_f$  shift (similar for the negative  $E_f$  shift).

Calculated results for metallic and semiconducting CNTs of various diameters

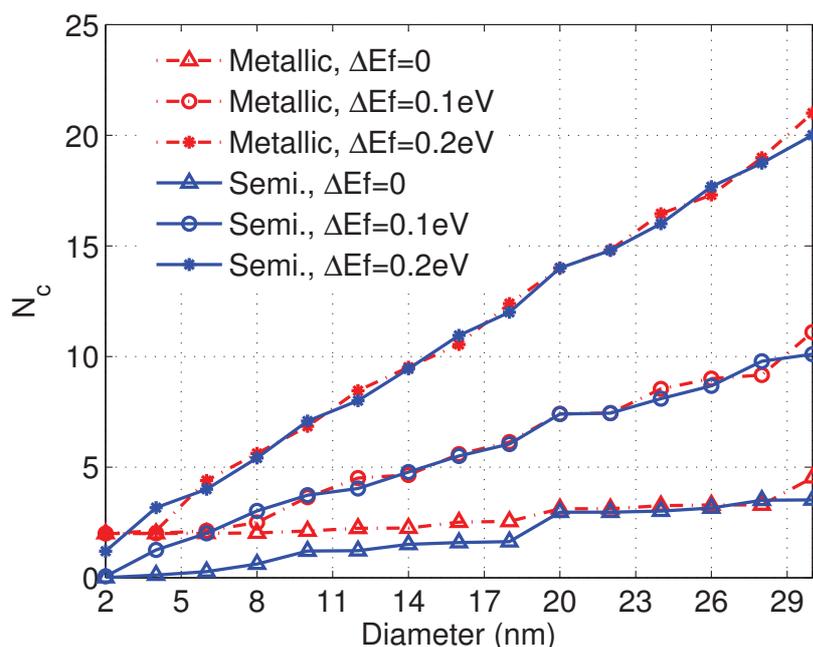


Figure 3.5: Change of  $N_C$  with diameter for metallic and semiconducting CNTs before and after the  $E_f$  shift.

before and after the  $E_f$  shift are shown in Fig. 3.4. It shows that the increase in  $N_C$  is more significant for larger diameter CNTs than for smaller diameter CNTs. Moreover, metallic and semiconducting CNTs have almost the same  $N_C$  when their diameters are larger than 20 nm. The increase in  $N_C$  leads to increase in both conductance and quantum capacitance of MWCNT [91] and can change the performance of MWCNT interconnect.

In Fig. 3.4 we show the calculated results for different shells of an MWCNT with 11 nm outermost diameter. The negative shift of  $E_f$  corresponds to the p-type doping while the positive shift corresponds to the n-type doping. There are in total nine shells based on the shell number calculation equations (in Chapter 2). The smallest or innermost diameter is 5.56 nm. Furthermore, we note from Fig. 3.4(c) that when  $E_f$  is shifted to 0.043 eV and 0.1 eV, the outermost and the innermost semiconducting CNT shells start to have  $N_C = 2$ , respectively.

Interestingly, pristine metallic CNTs also have  $N_C = 2$  when their diameters are small ( $\leq 11$  nm, see Fig. 3.5). Hence, we deduce that a semiconducting CNT of a small diameter ( $\leq 11$  nm) becomes equivalent to a pristine metallic CNT when its  $N_C$  reaches 2 ( $N_C = 2$ ) by shifting  $E_f$ . Additionally, we assume that the  $E_f$  shift is the same for both metallic and semiconducting CNT shells because no hint of doping selectivity for semiconducting and metallic CNTs is observed [183]. Furthermore, doping is assumed to have no impact on defect and contact resistance. Based on these assumptions and the simulations shown in Fig. 3.4(c), one can predict that a MWCNT with 11 nm outer diameter starts to degenerate semiconducting shells and increase metallic behavior when  $E_f$  is shifted by 0.043 eV with doping. All shells start behaving as metallic when  $E_f$  is shifted by 0.1 eV.

Table 3.2: Representative  $E_f$  shifts for MWCNT with  $D_{max} = 11$  nm and the  $N_C$  for metallic ( $N_{Cm}$ ) and semiconducting ( $N_{Cs}$ ) CNT shells. Also shown are the ratios of metallic CNT shells at different  $E_f$  shifts.

$E_f$ shifts (eV)	0	0.043	0.1	0.2	0.3
11 nm $N_{Cs}$	1.2	2.0	4.0	7.8	11.6
11 nm $N_{Cm}$	2.1	2.3	3.7	7.6	11.5
5.56 nm $N_{Cs}$	0.27	0.61	2.0	4.0	5.8
5.56 nm $N_{Cm}$	2.0	2.0	2.1	3.6	5.9
Metallic shell ratio after doping	1/3	1/3	1	1	1

It is important to note that chirality which represents the carbon nanotube rotation angle does not change with doping - it is the  $N_C$  or electrical conductance of semiconducting shells that changes to metallic-like shell properties. Detailed information of  $N_C$  and the ratios of metallic CNT shells in the MWCNT at some specific  $E_f$  shifts are shown in Table 3.2.

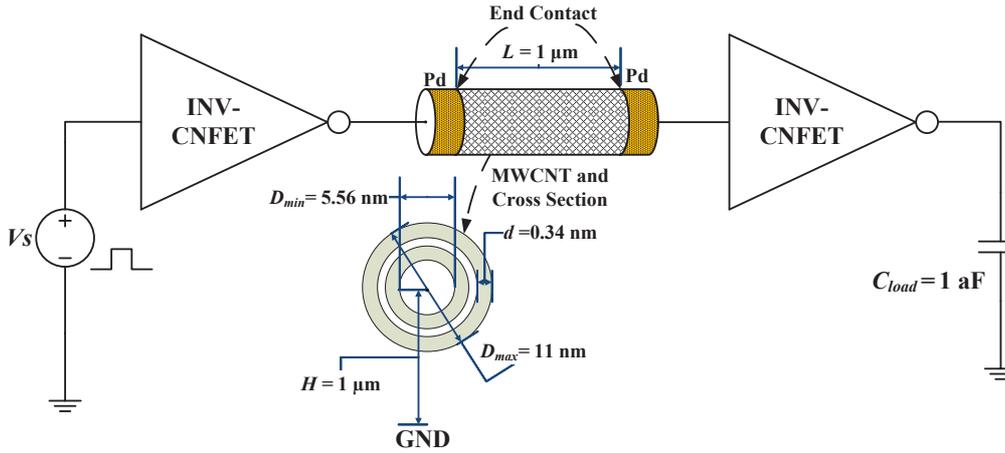


Figure 3.6: Simulation setup schematic of MWCNT as interconnect. MWCNT is connected between two inverters composed of CNTFETs.

### 3.3 Evaluations of Variability with Doping

#### 3.3.1 Simulation Setup

The simulation setup schematic is shown in Fig. 3.6. The circuit benchmark consists of two inverters connected through either an ideal wire or a MWCNT interconnect. Inverter gates are created with carbon nanotube field effect transistors (CNTFETs) based on compact models as in [81]. The key parameters of both n-type and p-type CNTFET are 11.7 nm, 1  $\mu$ m, 10 nm for gate length, gate width and the distance between CNTs, respectively where other parameters are the default values recom-

mended by [81]. We compute the MWCNT interconnect delay, power consumption, and power-delay product (PDP).

We conduct MC simulations for diameter, defects, chirality and all-sources variations. A detailed description of each variation source can be found Chapter 2 of this thesis. One thousand samples are collected to obtain a good confidence level for each simulation condition. We investigate MWCNT doping by considering the five representative  $E_f$  shifts as listed in Table 3.2. For any given Fermi shift  $E_f$  (or doping concentration), the MWCNT compact model (described in Chapter 2) is updated to take into account the  $N_C$  of each shell (either metallic or semiconducting). We also assume a defect density on each shell as  $10 / \mu\text{m}$ .

### 3.3.2 Impact of MWCNT Doping

In this section, we explore charge transfer doping as a means for reducing resistance variability. As described in Section 3.2.4, doping shifts the  $E_f$  and introduces additional  $N_C$  for both metallic and semiconducting MWCNT shells (see Table 3.2). We perform MC simulations for each source of variation (diameter, defects, and chirality) with different levels of  $E_f$  for doping. Results are shown in Fig. 3.7 (a)-(c). The all-sources variation results are shown in Fig. 3.8. Foremost, we observe that doping lowers MWCNT resistance and narrows the distributions, particularly for the  $E_f$  shift from 0.043 eV to 0.1 eV. Similar trends are also obtained for MWCNT performance (delay, power, and PDP) and are not shown here.

We also calculated the mean value ( $\mu$ ), standard deviation ( $\sigma$ ) and  $3\sigma$  percentage ( $3\sigma/\mu \times 100\%$ , used to estimate the largest possible percentage deviation from  $\mu$  [115], [128]) of MWCNT resistance and performances with the  $E_f$  shift and are presented in Fig. 3.9 and Fig. 3.10 (a)-(c), respectively for each source and the all-sources of variations. Based on our analytical method from Section 3.2.4 (Fig. 3.4 (c)), we know that doping of  $E_f \geq 0.043$  eV starts to increase  $N_C$  for metallic CNTs, whereas semiconducting CNTs begin to behave as metallic-like shells as  $N_C \geq 2$ . Hence, it is not until  $E_f$  reaches 0.043 eV that we start to observe improvements in MWCNT resistance and performances  $\mu$  and  $\sigma$  as in Fig. 3.9 and 3.10. On the contrary, the  $\sigma$  and  $3\sigma$  percentage of diameter variation increase to some extent when the  $E_f$  shift increases beyond 0.043 eV. This is because the outermost semiconducting shell of MWCNT at these  $E_f$  shifts can behave like metallic CNT shell when its diameter is larger than 11 nm as a result of diameter variation (see Table 3.2 and Fig. 3.4). The co-existence of metallic and semiconducting CNT shells makes the diameter variation more predominant. Due to the increase in diameter variation, the all-sources variation also slightly increases with  $E_f$  beyond 0.043 eV.

But, as  $E_f$  reaches 0.1 eV, all semiconducting shells behave as metallic, thus improving significantly MWCNT resistance  $\mu$  and  $\sigma$ . As more doping is applied with  $E_f$  from 0.1 eV to 0.3 eV, slight reductions in  $\mu$  and  $\sigma$  are observed. This can be mainly explained due to two doping attributes: (1) significant CNT shell resistance reduction is obtained at  $E_f = 0.1$  eV as all semiconducting shells behave as metallic shells, and (2) with more doping  $E_f \geq 0.1$  eV the  $N_C$  increases, however, resistance reductions is less drastic as in (1). Additionally, the change in the ratio of metallic to semiconducting CNT shells makes the chirality variation reduced (both

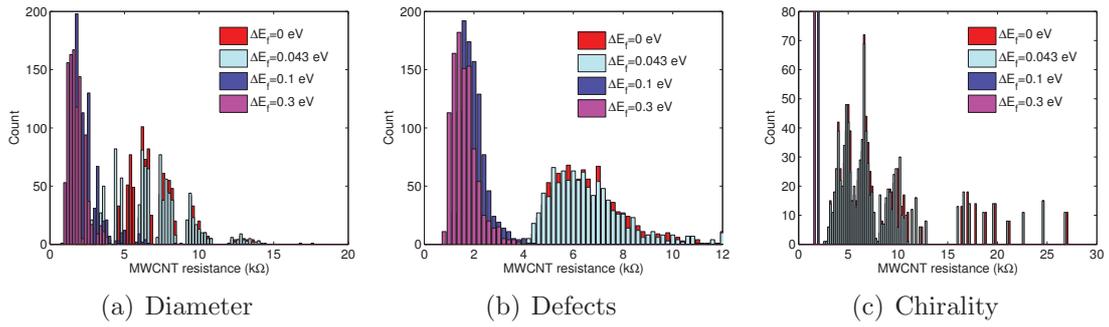


Figure 3.7: (a)-(c) are distributions of resistance variation of the MWCNT interconnect at different  $E_f$  shifts with input diameter, defects, and chirality variations respectively.

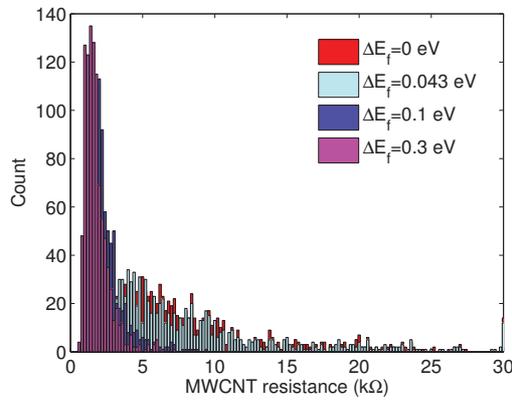


Figure 3.8: Distributions of resistance variation of the MWCNT interconnect at different  $E_f$  shifts with input all-sources variation.

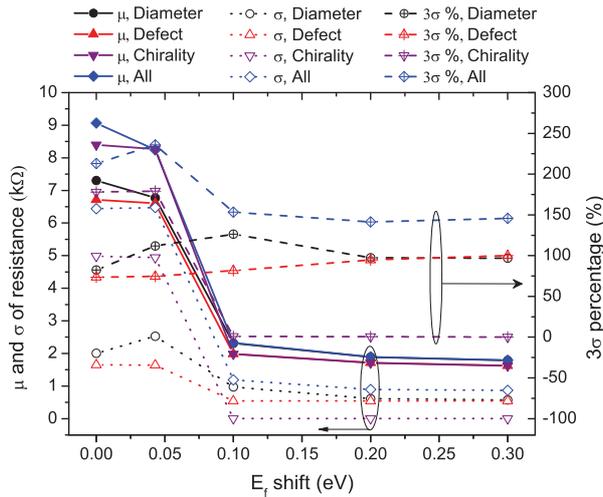


Figure 3.9: Change of resistance of the MWCNT interconnect with the  $E_f$  shift for diameter, defect, chirality and all-sources variations.

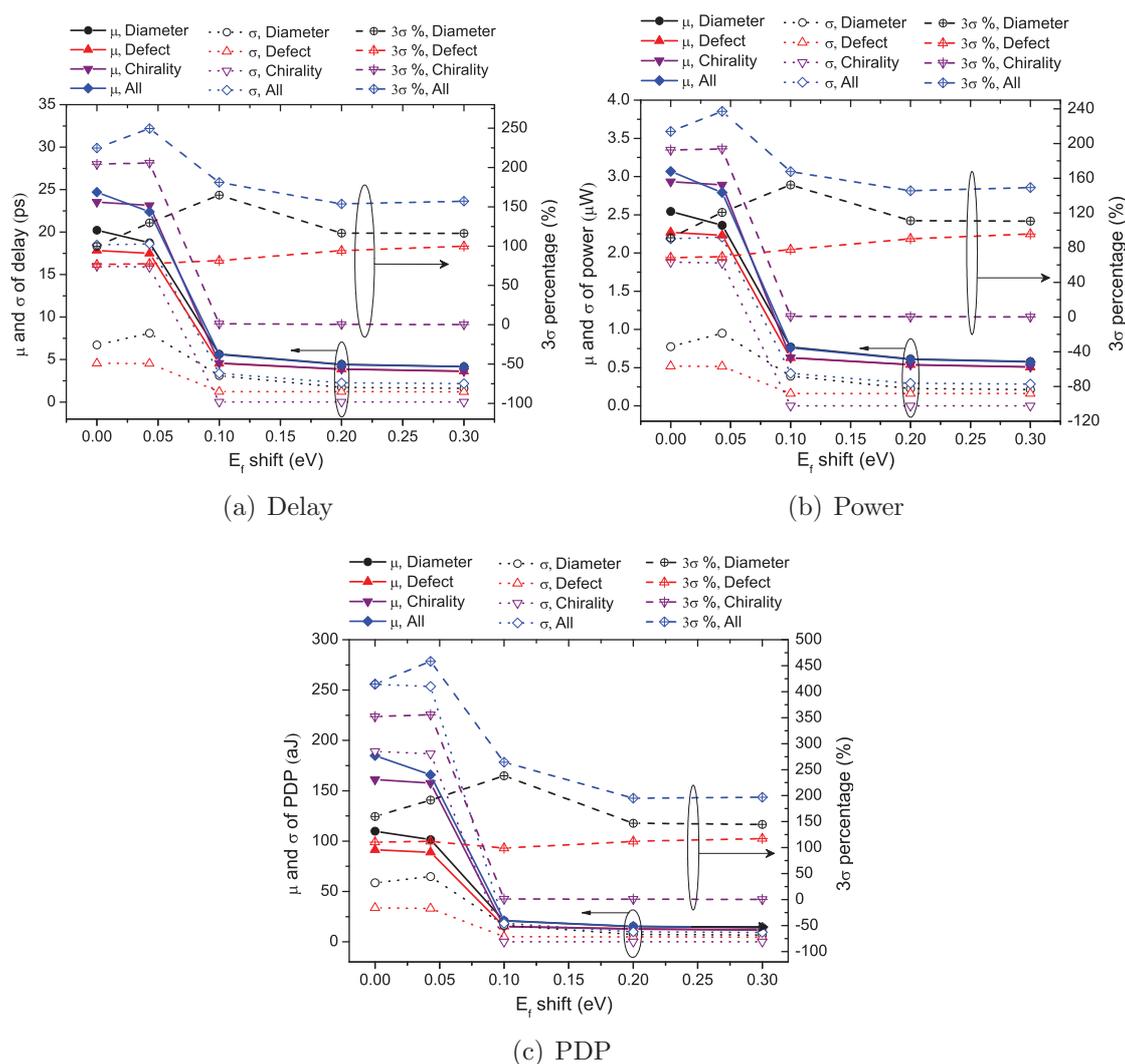


Figure 3.10: (a)-(c) are change of delay, power and PDP variations of the MWCNT interconnect, respectively with the  $E_f$  shift for diameter, defect, chirality and all-sources variations.

$\sigma$  and 3 $\sigma$  percentage). It approaches zero when  $E_f$  reaches 0.1 eV. We also note that although the  $\sigma$  of diameter and defects variation reduce with  $E_f$  of 0.1 eV, the 3 $\sigma$  percentage does not improve due to their respectively similarly decreasing rate of  $\mu$ . Both diameter and defect variations remain present as  $E_f$  shifts beyond 0.1 eV because they are not directly related to  $E_f$  or  $N_C$  and furthermore contact and defect resistances (contribute to diameter and defects variations) are assumed to be not impacted by doping in this work. Hence, their impact cannot be canceled out by doping.

All-sources variation shows a similar trend in resistance and performances  $\sigma$  to that of chirality variation with the  $E_f$  up to 0.1 eV as shown in Fig. 3.9 and 3.10. Beyond  $E_f$  of 0.1 eV, the contribution of chirality to overall variation is negligible, but the variations of diameter and defects dominate. We can deduce that

doping helps to reduce overall MWCNT variation by decreasing the contribution of chirality variation mainly due to the degeneration of semiconducting shell properties to metallic. Doping has limited impact on defects and diameter (including contact resistance variation) variations, especially for the  $3\sigma$  percentage variation.

### 3.3.3 Comparisons with Experimental Data

As described in [93], our partners in the project developed a CNT integration process to grow individual MWCNTs at predefined locations on a silicon wafer by hot filament assisted CVD, and to individually contact them with Palladium (Pd) electrodes for electrical characterization. External doping of the MWCNT by  $\text{PtCl}_4$  salt was then developed. To estimate the impact of doping under various conditions, similarly to [93], we assume the contact resistance is much smaller than MWCNT intrinsic resistance and compare the distributions of linear resistance before and after doping. In [93], a 40% reduction of the linear resistance was obtained by dipping the connected MWCNTs in  $\text{PtCl}_4$  solution. For this work, our partners used a different doping process and instead sprayed the  $\text{PtCl}_4$  solution on the connected MWCNTs to better control the amount of dopant on the CNTs. It is found that both mean value and variations of MWCNT resistance are significantly reduced after doping. In addition, higher doping efficiencies can be obtained with the spray doping process and that the Fermi-level shift can be controlled by the amount of dopant deposited on the CNTs. TEM and STEM pictures of MWCNT before and after doping are shown in Fig. 3.11.

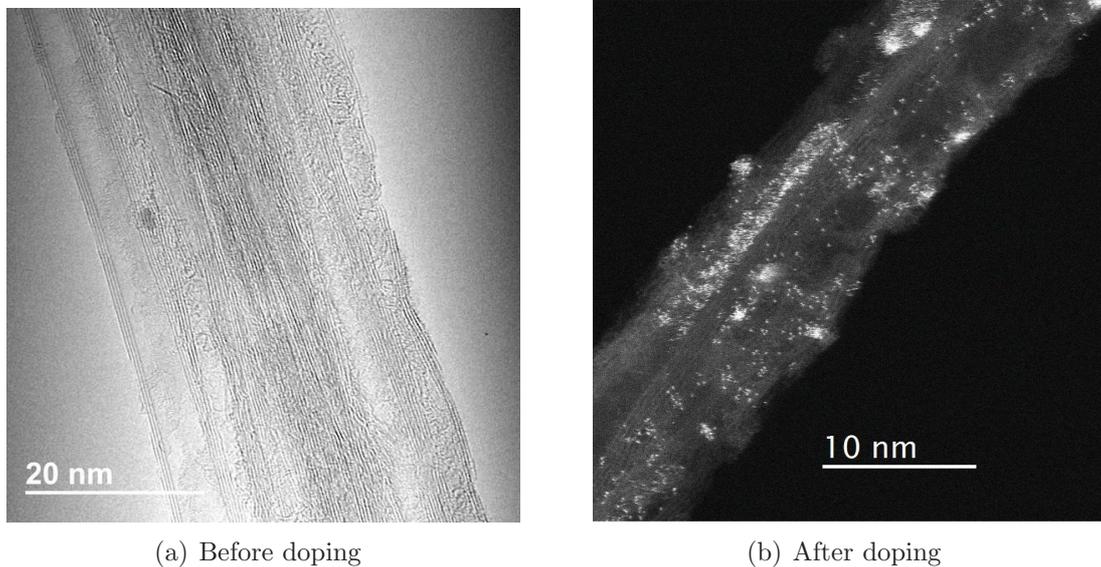


Figure 3.11: TEM and STEM pictures for MWCNT before and after doping with  $\text{PtCl}_4$ , respectively.

The measured average  $D_{max}$  of the experimentally doped MWCNTs was 6.5 nm. Because the defect density and MFP of these doped CNTs are not measurable, direct comparisons of  $\mu$  and  $\sigma$  of MWCNT resistance between experiments and simulation (all-sources variation) are difficult and meaningless. Instead, we compare relative

Table 3.3: Comparisons of doping efficiency in reducing MWCNT resistance between the all-sources simulation results and the experimental data in this work or that from [93].

Doping process	Non doped[93]	Dipping	Spray dopant 1	Spray dopant 2
Estimated $E_f$ shifts (eV)	0.00	0.104	0.122	0.250
$\sigma$ , simulation	0%	-19.6%	-42.6%	-77.2%
$\sigma$ , experiments	0%	-18.6%	-59.3%	-77.2%
$\mu$ , simulation	0%	-41.2%	-55.1%	-73.1%
$\mu$ , experiments	0%	-41.4%	-55.5%	-73.3%
$3\sigma\%$ , simulation	0%	38.9%	24.4%	-16.6%
$3\sigma\%$ , experiments	0%	39.0%	-8.5%	-14.5%

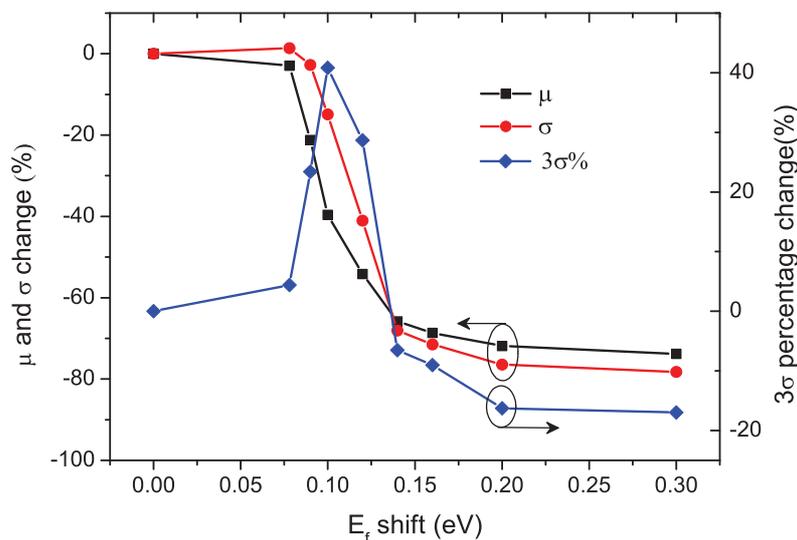


Figure 3.12: Change of MWCNT resistivity and its variability from the all-sources simulation results with the  $E_f$  shift for the MWCNT of  $D_{max} = 6.5$  nm (other parameters are the same to previous simulations).

change (or doping efficiency) in MWCNT resistance  $\mu$  and  $\sigma$ , and the  $3\sigma$  percentage variations with  $E_f$  shift for MWCNTs of  $D_{max} = 6.5$  nm. Fig. 3.12 shows the simulation results of MWCNT doping efficiency with  $E_f$  shift. In Table 3.3, we show doping efficiency of  $\mu$  and  $\sigma$ , and  $3\sigma$  percentage variations before and after doping for experimental results (obtained in this work or those from [93]). By comparing these simulation results and experimental results we can further predict the Fermi shift due to experimental doping, as presented in the table. For comparisons, the corresponding  $\mu$ ,  $\sigma$  and  $3\sigma$  relative percentage reductions extracted from Fig. 3.12 are shown in Table 3.3 as well. The most significant deviation between the simulation results and experimental data is the relative change in  $3\sigma$  percentage variation at the  $E_f$  shift of 0.122 eV. This can be attributed to the abrupt change in  $3\sigma$  percentage

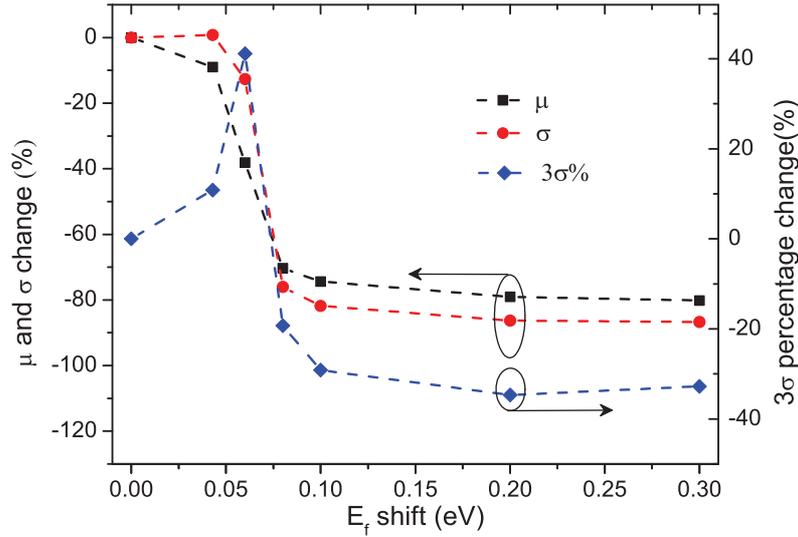


Figure 3.13: Change of MWCNT resistivity and its variability from the all-sources simulation results with the  $E_f$  shift for MWCNT of  $D_{max} = 11$  nm (MFP =  $1000D_{CNT}$ ).

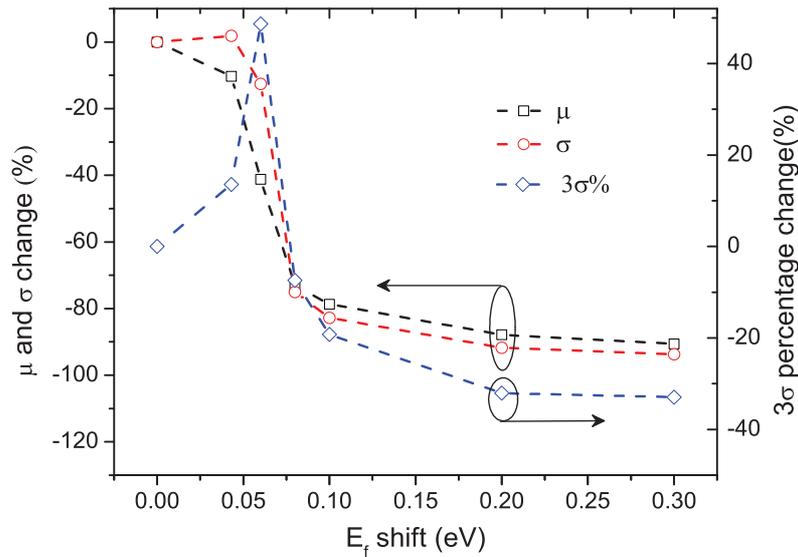


Figure 3.14: Change of MWCNT resistivity and its variability from the all-sources simulation results with  $E_f$  shift for MWCNT of  $D_{max} = 11$  nm (MFP =  $10D_{CNT}$ ).

variation as shown in Fig. 3.12 and the assumed  $E_f = 0$  eV for pristine CNTs (before doping operation) which may be incorrect because p-doped CNTs have an  $E_f$  downshift which can be expected during fabrication [183], [102].

Except for the  $3\sigma$  percentage deviation, an overall good match between experimental data and simulation results is observed, which strongly demonstrates the capability of the MWCNT compact model to quantitatively predict relative change in MWCNT performance and the doping efficiency.

### 3.3.4 Doping Efficiency

#### Impact of MWCNT diameter

It is worth noting that the required level of the  $E_f$  shift (or effective  $E_f$  shift) to achieve a significant improvement of MWCNT resistance is dependent on the MWCNT dimensions though the overall change of doping efficiency with doping is similar. For example, by decreasing  $D_{max}$  from 11 nm to 6.5 nm, the effective  $E_f$  shift is increased from  $\sim 0.1$  eV to  $\sim 0.16$  eV but the overall change of doping efficiency with doping is similar, as shown in Fig. 3.12 and Fig. 3.13.

#### Impact of MFP

CNTs are of interest due to their ballistic transport and long mean free path (MFP). In this work, we assume that the default value of MFP in each shell of MWCNT is 1000 times the CNT shell diameter [91]. However, MFP is dependent on MWCNT fabrication process and thus may change from process to process. For instance, based on the scattering resistance of CVD-grown MWCNTs measured in [93] and in this work - it appears that MFP is shorter than 100 nm ( $\sim 10-20 \times D_{CNT}$ ), which is also in agreement with other literature reports [158]. So, it is worth investigating the impact of MFP on doping efficiency by considering different MFPs. Simulation results of doping efficiency for MFP of  $10 \times D_{CNT}$  are presented in Fig. 3.14 and compared with the default case (MFP of  $1000 \times D_{CNT}$ ) in Fig. 3.13. It shows that despite the 100 times difference in MFP, doping efficiency is similar. This is because doping increases  $N_C$  of CNT shells and further improves conductance of MWCNT, which is impacted by MFP proportionally under different  $N_C$  as shown in Equations (3.9) and (3.10). As a result, we deduce that the MFP does not significantly impact the relative change of MWCNT resistance and performance improvements obtained from doping.

#### Impact of Pristine MWCNT chirality

As demonstrated in Section 3.3.2, the improvement of MWCNT performance and variability with doping is mainly attributed to chirality variation reduction. Because the chirality variation results from the change of metallic and semiconducting CNT shell portions, it is reasonable to deduce that the doping efficiency can be degraded if the original MWCNT is more metallic, namely a larger portion of metallic CNT shells. For example, Fig. 3.15 shows the simulation results of entirely metallic MWCNT, namely metallic chirality 1 (other parameters are the same as the default one) with the  $E_f$  shift. Compared with the default MWCNT (1/3 of metallic CNT shells) as shown in Fig. 3.13, the doping efficiency is reduced for the entirely metallic MWCNT. Instead of the abrupt reduction in  $\mu$  and  $\sigma$  of MWCNT resistance for the default MWCNT from the  $E_f$  shift of 0.043 eV to 0.1 eV, a continuous and slow reduction is observed for the entirely metallic MWCNT up to 0.3 eV. Moreover, different from the default case where  $3\sigma$  percentage can finally be reduced by doping up to 0.1 eV, the  $3\sigma$  percentage is continuously increased with doping for the entire metallic MWCNT case.

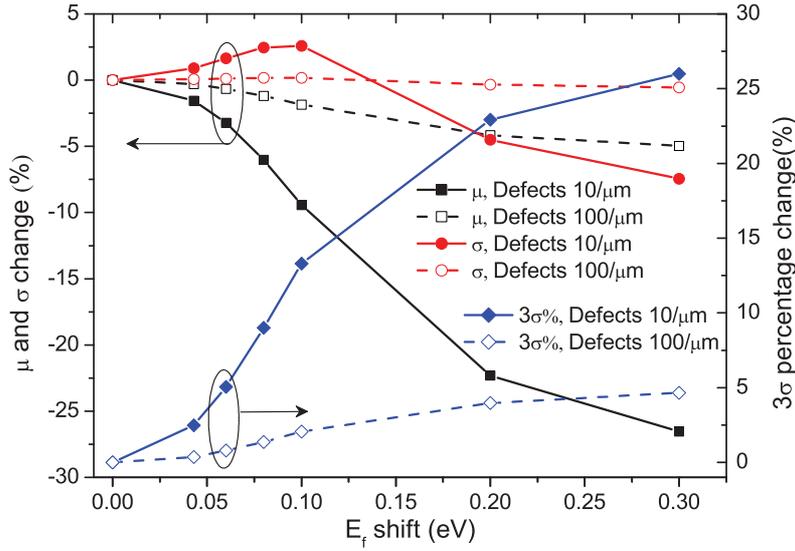


Figure 3.15: Change of metallic MWCNT resistivity and its variability from the all-sources simulation results with the  $E_f$  shift for defect density of 10 / $\mu\text{m}$  (the default) and 100 / $\mu\text{m}$ .

### Impact of Defect Density

We study the impact of defect density and in Fig. 3.15 we show the simulation results of doping efficiency for the entire metallic MWCNT. We observe that with the increase in defect density, doping effectiveness is significantly reduced for the entire metallic MWCNT. For example, the doping efficiency of  $\mu$  and  $\sigma$  of MWCNT resistance at the 0.3 eV  $E_f$  shift is 26.5%/7.3% and 5.0%/0.7% for defect density of 10 / $\mu\text{m}$  and 100 / $\mu\text{m}$ , respectively. The  $3\sigma$  percentage is increased relatively by 26.1% and 4.5%, respectively. This is because the role of diameter and defect variations are relatively more important as defect density is increased for the case of entirely metallic MWCNT. However, it is found that for the default case of 1/3 metallic chirality, the defect density impact on doping effectiveness is negligible (less than 2% and 4% difference are observed at the  $E_f$  of 0.1 eV and 0.3 eV, respectively). This is due to the dominant impact of chirality variation on the overall variation response with  $E_f$  shift for the default case.

### 3.3.5 MWCNT Shell to Contact Variations

Here, we study the impact of doping on MWCNT shells connectivity to contact. In Fig. 3.16, we show the relative worst case (the outermost shells disconnected, as discussed in Chapter 2 of this thesis) resistance degradation (similar to  $\sigma$ ) versus a different number of disconnected shells for different  $E_f$  shift levels compared to all shells connected case. No significant improvements with doping are observed till  $E_f = 0.043$  eV and significant improvements are observed for  $E_f \geq 0.1$  eV. When normalizing the relative worst resistance degradation to the case with all shells connected resistance (similar to  $\sigma/\mu$ , namely relative variation), it is found that there is not an obvious impact from doping up to five disconnected shells (out of

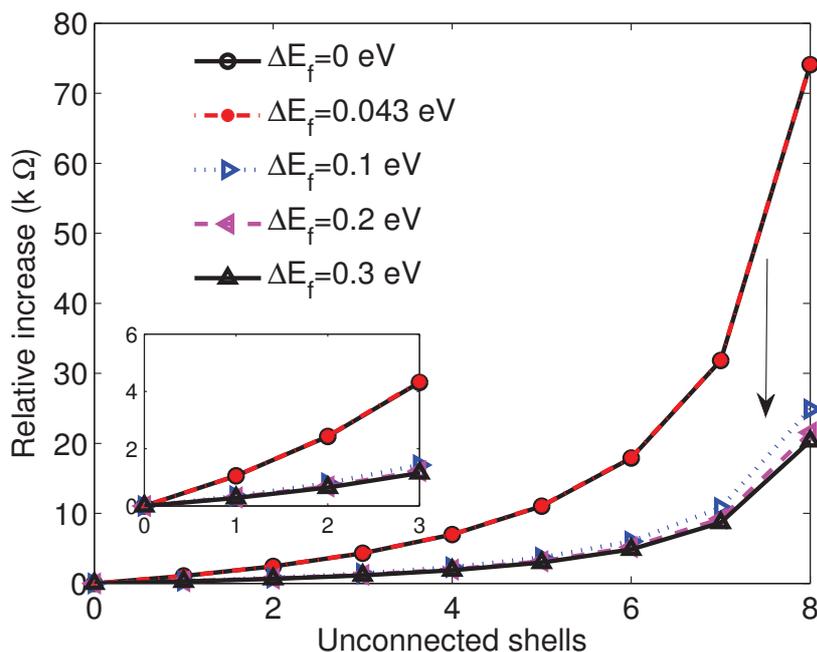


Figure 3.16: Relative increase in the worst case MWCNT delay with several disconnected shells and  $E_f$  shift levels compared to the case of all (nine) connected shells. The inset is the simulation result of unconnected shells from 0 to 3 after zooming in.

nine shells total) and increases slightly as more shells are disconnected. MWCNTs performances with disconnected shell have a similar response to doping and are not shown here. Hence, we deduce that doping improves MWCNT resistance and then performances, which allows mitigating the effect of disconnected shells without increasing relative variation significantly.

### 3.4 Experimental vs. Simulation Results

In our project, our partners have developed the process of chemical vapor deposition (CVD) grown CNTs in relatively low temperatures ( $\sim 600^\circ C$ ) for on-chip interconnect applications and compatibility with CMOS BEOL process line.  $PtCl_4$  charge based doping process is developed as well, and CNT/Palladium side contacts are realized for electrical characterization. Figure 3.17 presents the individual CVD grown MWCNT and the distribution of CNT diameter is  $6.5 \text{ nm} \pm 1 \text{ nm}$ . Figure 3.18 shows the HAADF-TEM image of the CNT opened with oxygen plasma process and doped with Pt-Cl network of dopants. The three different CNTs are highlighted with doped dotted purple lines. The Pt and Cl elements within the doped-CNT were verified using Energy-Dispersive X-ray spectroscopy (EDX) mapping. The difference in concentration between neighboring CNTs is due to partial amorphization induced by plasma treatment. Finally, both side-contact and end-contact were realized on individual MWCNT as shown in Fig. 3.19.

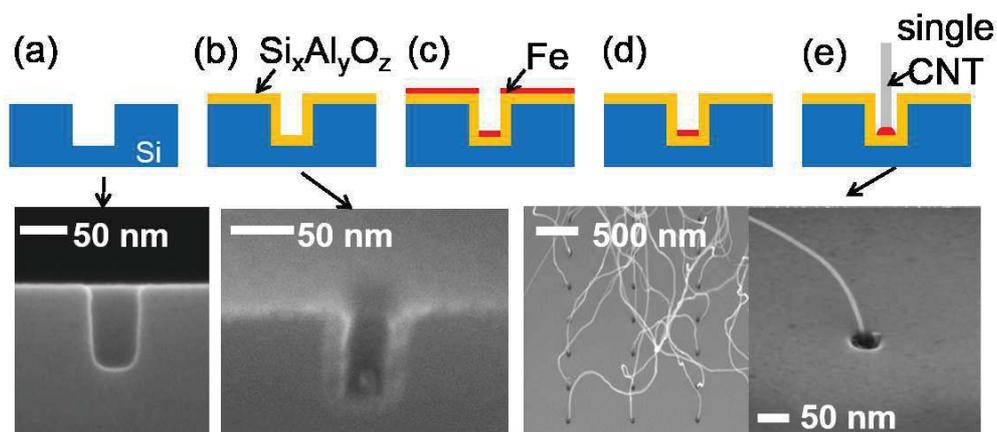


Figure 3.17: Localized growth of a single MWCNT from a via hole.

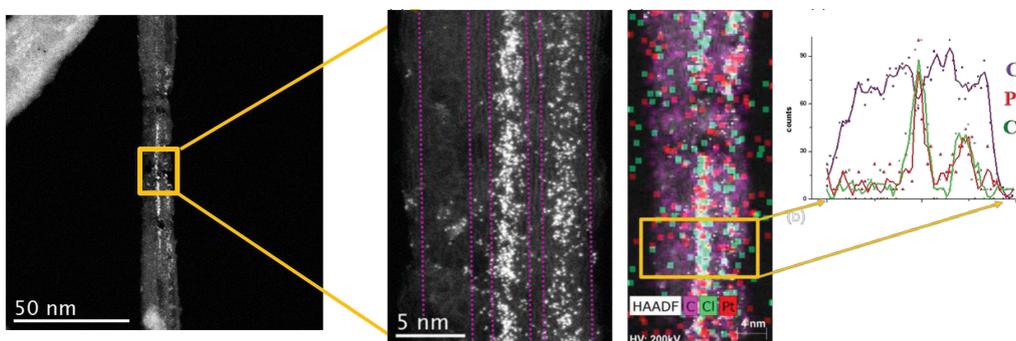


Figure 3.18: HAADF-TEM image of CNTs with different concentration of dopant is shown in the left side. EDX mapping of Pt-Cl doped CNTs and line scan of EDX mapping across doped CNT are shown in the middle and right sides. Purple, red, green color represents Carbon, Platinum and Chlorine respectively.

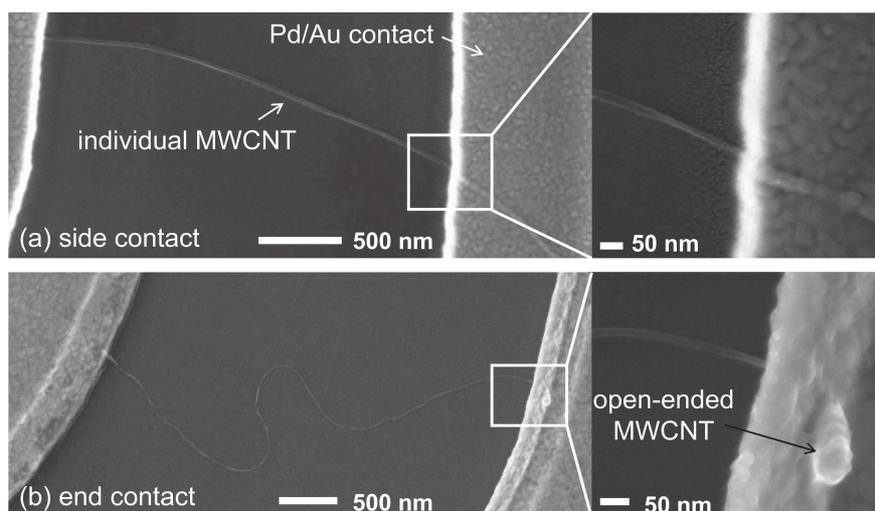


Figure 3.19: SEM images of electrically connected individual MWCNT with (a) side and (b) end contacts made out of Pd (40nm) and Au (150nm).

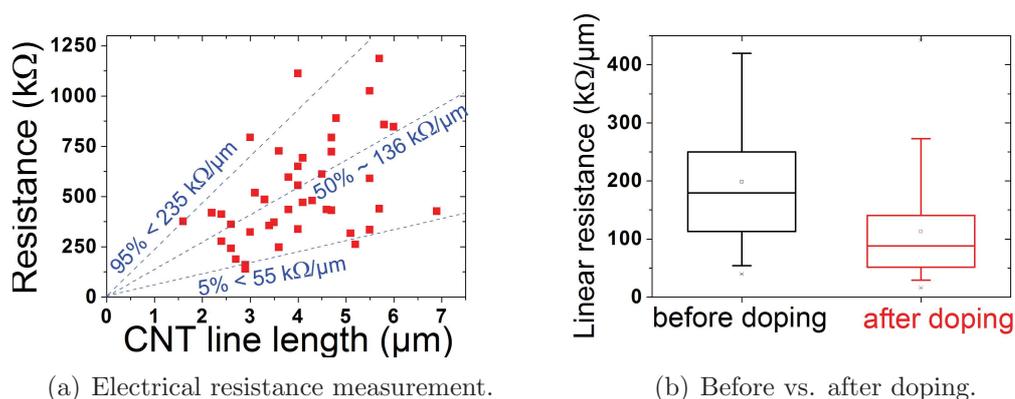


Figure 3.20: (a) Two points probe resistance measurement for a collection of individual CNTs. (b) 50% improvement of linear resistance with external  $\text{PtCl}_4$  doping.

A set of individual MWCNT interconnect fabricated in parallel on the same sample was electrically characterized. Two-point-probe current-voltage characteristics were systematically recorded to extract the electrical resistance (CNT resistance + CNT/Pd side contact resistance). Fig. 3.20 (a) displays the measured resistance as a function of the CNT length. It is observed that resistance increases with CNT length in the 1-10  $\mu\text{m}$  range, which is expected for diffusive transport in CVD-grown, hence, defective CNTs. However, a large scatter in the data is observed, thus revealing variability in MWCNT conductivity and contact resistance. The origin of the variability may be the variability in the diameter, the number of shells of each CNT, the random repartition of metallic versus semiconducting shells, the presence of defects, or variability in the contact fabrication technology. Assuming the measured resistance is dominated by the resistivity of MWCNT, linear resistance is spread between 55 and 235  $\text{k}\Omega/\mu\text{m}$  (90% envelope). Preliminary electrical results of doped CNTs by  $\text{PtCl}_4$  were obtained by using external doping of side-contacted single CNT interconnects. Fig. 3.20 (b) displays the measured linear resistance (resistance divided by CNT length) for the same set of CNTs before and after external doping. It is observed that, on average, the resistance of externally doped MWCNTs is reduced up to 50%. The scatter of data is also reduced, which suggests variability improves with doping.

As described shown previously, doping is an efficient method to enhance MWCNT conductivity and reduce shell variability. However, there is a discrepancy between the theoretical predictions (i.e., up to 90% improvement in resistivity) versus experimental measurements (i.e., up to 50% improvement of linear resistance). We presume that such discrepancy is due to contact resistance and defects on MWCNT which reduce its mean free path. As MWCNTs are grown in low-temperature ( $\sim 450^\circ\text{C}$ ) CVD, it is challenging to obtain high-quality CNTs. Various types of defects are introduced during the growth process, such as vacancies (missing atoms), interstitials, non-hexagonal carbon atom rings [38, 177], which result in shortening the ballistic transport (or electron mean free path). The reduction in mean free path leads to higher MWCNT resistance [18]. Additionally, the contact between

metal and CNTs can be of considerable resistance. The DOS of pristine CNTs is not comparable with bulk metals. For metal-to-metallic CNT junctions, nearly zero DOS of pristine metallic CNTs indicates a relatively high contact resistance. There are commonly two types of contacts, end-contact [28] and side-contacts [54]. We introduce two fitting parameters to our MWCNT model: defect-related mean free path [156] and contact resistance,  $R_C$  as:

$$L_{MFP}^D \approx \alpha \cdot D_{MWCNT} \quad (3.11)$$

$$\begin{aligned} R_{MWCNT}^D &= \frac{1}{N_C N_s G_{1channel}} + 2R_C \\ &= \frac{1 + L/L_{MFP}^D}{N_C N_s G_0} + 2R_C \end{aligned} \quad (3.12)$$

where equation 3.11 represents the mean free path with defects. Smaller  $\alpha$  means shorter CNT mean free path, and highly defective the CNT is. Equation 3.12 represents the defective MWCNT resistance together with contact resistances. These equations indicate that MWCNT resistance increases with defects (or decrease of mean free path  $L_{MFP}^D$ ) and contact resistance,  $R_C$ . When doping is applied, the number of conducting channels  $N_C$  increases which helps to reduce MWCNT resistance and alleviate some of the detrimental impacts of defects.

We update our model to include different mean free path.  $L_{MFP}^D = \alpha \cdot D_{MWCNT}$  represents different defects density impacts on CNT mean free path, the smaller  $\alpha$  is the higher defect density presents in CNT and shorter the electron mean free path becomes.  $L_{MFP} = 1000D_{MWCNT}$  represents the defect-free MWCNT. In Fig. 3.21, we show a doped ( $N_c = 5$ ) 7 nm MWCNT without contact resistance. Comparing to the pristine CNT, doping efficiency (left y-axis) is evaluated with defects. It shows a decrease in doping efficiency with defects, as defects are worsening CNT total resistance which is opposite to doping effect. For right y-axis, we present the tolerated contact resistance if we want to make doped defective MWCNT total resistance remain unchanged to pristine MWCNT. Doping efficiency and tolerated contacts become very small when the CNT is highly defective ( $L_{MFP} \sim 20D_{MWCNT}$ ).

We also consider various contact resistances  $R_C$  to represent contact type (side-/end-contacts) and contact metal. In Fig. 3.22 we show the MWCNT doping efficiency in a realistic interconnect system while varying contact resistance and defects in MWCNTs. In this case, we would like to show the importance of contact resistance. While contact resistances are included both for pristine and doped defective MWCNTs. Contacts are reducing the doping efficiency as doping does not directly impact the contact resistance but improves the tube resistance. Hence the total MWCNT resistance is reduced by doping but increased by contacts and defects. For pristine CNT with  $L_{MFP} = 1000D_{MWCNT}$ , 10 times increase in contacts (2 k $\Omega$  to 20 k $\Omega$ ) causes 3.7 times reduction of doping efficiency. And with 10 times decrease in defects related mean free path (1000D to 100D), there are 1.22 and 1.25 times doping efficiency degradation for contact resistance of 2k $\Omega$  to 20 k $\Omega$  respectively. Hence, when we introduce contact resistance to the interconnect system, it

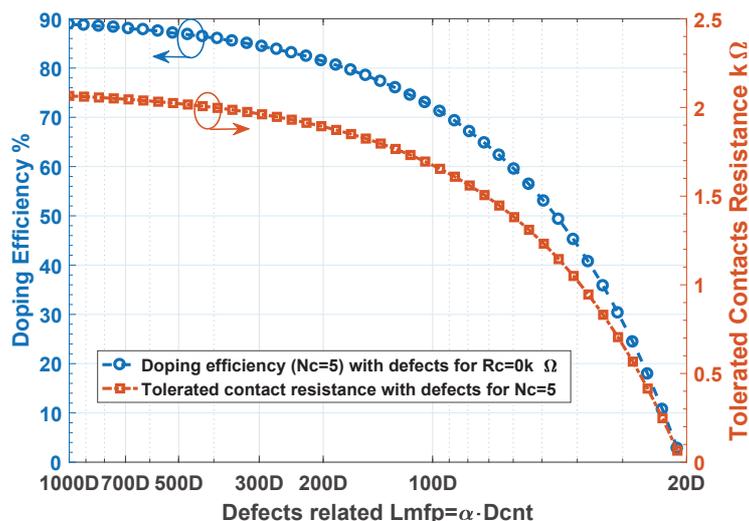


Figure 3.21: For MWCNT of diameter 7 nm, it is shown in the left Y-axis that doping efficiency of  $N_c = 5$  varies with defects and no contact resistance. With doping of  $N_c = 5$ , tolerated contact resistance to remain the total resistance unchanged for various defect scenarios is shown in the right Y-axis. Each tolerated contact resistance is derived with corresponding doping efficiency for each defect scenario.

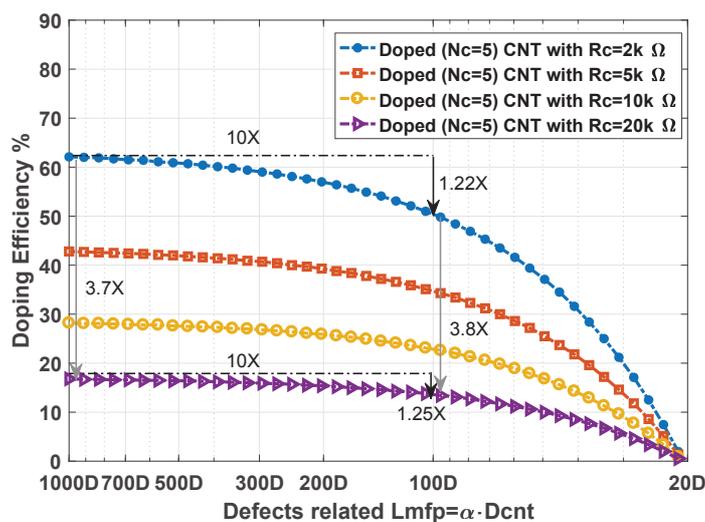


Figure 3.22: Doping efficiency of MWCNT of diameter 7nm. Doping concentration is fixed as  $N_c = 5$ . The presence of contact resistance decreases the doping efficiency for various defects concentration.

becomes the dominant factor comparing to defects. Doping efficiency reduces with high contacts and defects.

It is known from experimental measurements that distribution of linear resistances of pure MWCNTs are centred at  $136 \text{ k}\Omega/\mu\text{m}$  and 50% of linear resistance is improved by doping (Fig. 3.20 (a) and (b)). As aforementioned, both contacts and defects can impact the MWCNT resistance and doping efficiency. Therefore,

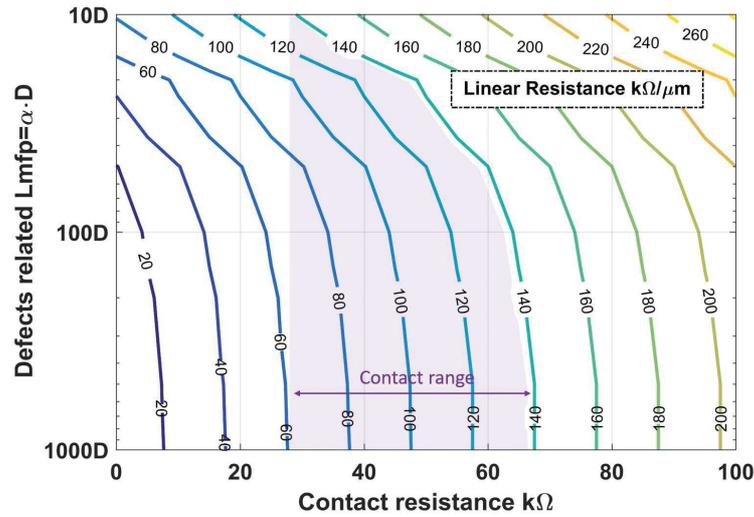


Figure 3.23: Theoretical prediction of linear resistance for a defective pure MWCNT with contact resistances, similar conditions to the experimental measurements. 1000D means defects free and 10D represents highly defective.

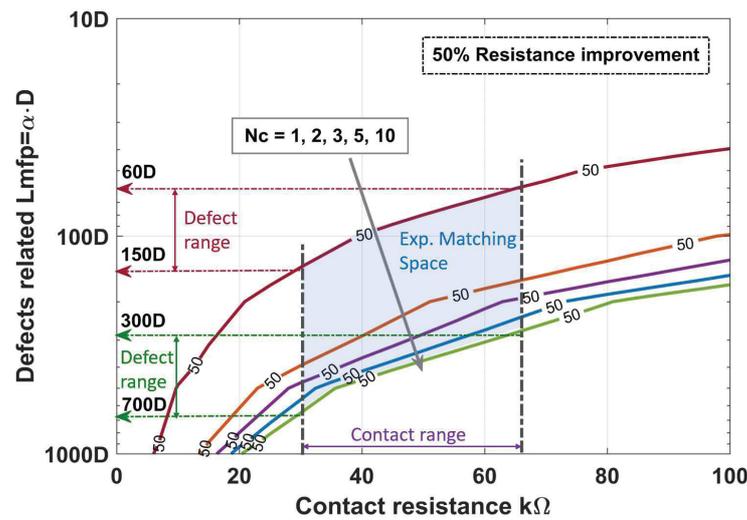


Figure 3.24: 50% of resistance improvement after doping with different  $N_c$  (red line:  $N_c = 1$ ; green line:  $N_c = 10$ ). Resistance improvement has also dependence on contact resistance and defects related CNT mean free path. 1000D means defects free and 10D represents highly defective.

we performed a variability simulations by varying contact resistance and defects related CNT mean free path for pure MWCNTs with results shown in Fig. 3.23. Both contacts and defects are increasing the pure MWCNT resistance. If we look into the linear resistance of  $140 \text{ k}\Omega/\mu\text{m}$ , we find a range of contact resistance of  $30 \text{ k}\Omega$  to  $67 \text{ k}\Omega$  for various defect related CNT mean free paths.

To further decorrelate the impact of contacts and defects during before and after doping experimental measurements, we consider different levels of doping by

varying  $N_c$  from 1 to 10. The goal is to assess the possible combination of contact resistances, quality of grown CNTs (regarding defects) and doping process efficiency for our experimental results. In Fig. 3.24, 50% resistance improvements are shown with variations of contacts and defects. We notice that doping from  $N_c = 5$  to  $N_c = 10$  has much less impact than doping from  $N_c = 1$  to 2, hence we predict that for 7 nm MWCNT, heavily doping ( $N_c > 5$ ) will not have additional significant impacts. Combining with the  $140 \text{ k}\Omega/\mu\text{m}$  linear resistance (with contact resistance of  $30 \text{ k}\Omega$  to  $67 \text{ k}\Omega$ ) shown in Fig. 3.23, after different doping, defects related mean free paths can be derived. For lightly doping of  $N_c = 1$ ,  $L_{\text{MFP}}$  of 60D to 150D are found (dashed red arrows) and with heavily doping of  $N_c = 10$ ,  $L_{\text{MFP}}$  can vary from 300D to 700D.

From Fig. 3.23 and 3.24, we would like to propose some possible understanding of our low temperature CVD grown MWCNT quality and evaluate the contact and doping process. Knowing the average linear resistance of  $136 \text{ k}\Omega/\mu\text{m}$  and 50% of linear resistance improvement, our MWCNTs have relatively high contact resistance and with different doping levels and defects related CNT mean free path can vary from 60D to 700D. Further four points and six points measurements should be investigated to fully decorrelate the relationship among doping efficiency, contact resistance and defects for standalone MWCNT interconnects.

## 3.5 Discussion

In this chapter, we show that by doping ( $E_f$  shift to 0.1 eV) on a MWCNT of  $D_{\text{max}} = 11 \text{ nm}$  significant improvements on performance and variability can be obtained. However, we also show that for MWCNT of smaller diameters, more doping or  $E_f$  shift is required to achieve these improvements. Hence, as technology scales, the local interconnect sizes also decrease [167], which implies that MWCNT interconnects for advanced technology node applications may need higher doping levels to improve their performance and variability efficiently. Moreover, the  $N_C$  of semiconducting CNT shells decrease with their diameter and technology scaling, hence, increasing the importance of applying doping to local interconnects with small geometries to improve MWCNT resistance and chirality variation. Other sources of variations such as diameter and defects will require further improvement on CNT process growth to exploit the potentials of MWCNTs for interconnect application.

In this chapter, we propose an enhanced compact model for MWCNT interconnects to take into account variability including diameter, defects, chirality and connectivity and also the impact of doping as a countermeasure to large resistance variability. Based on the analytical formulations, the change of MWCNT resistance and performance variation (including delay, power, and PDP) with  $E_f$  shift can be calculated while including variations on diameter, defect densities, chirality, and shell-to-contact connectivity. We identify that chirality variation (both  $\sigma$  and  $3\sigma$  percentage) can be significantly reduced to almost zero when the doping induced  $E_f$  shift enables to degenerate all semiconducting shells to equivalent metallic like shell conductivity. Also, the diameter and defect variations  $\sigma$  can be reduced up to  $\sim 80\%$  while the  $3\sigma$  percentage is slightly increased. The efficiency of doping is compared with experimental data, and an overall good match is obtained, which

demonstrates the validity of computing doping efficiency and simulation methodology. We observe that MFP has a minor effect on doping efficiency. However, doping efficiency can be significantly reduced and degraded if the original portion of metallic CNT shells increases. Overall, we have established the analytical methods and simulation framework to study charge based doping impact on MWCNT interconnects performance and variability.

## 3.6 Conclusion

In this chapter, we investigate Pt-salt doped CNT for BEOL interconnects. By combining atomistic to circuit-level simulation and measurement results, we explain the impact of doping on enhancing MWCNT metallic properties. Both experimental data and simulations show that the  $\text{PtCl}_4$  represents an efficient doping strategy to reduce MWCNT resistivity through conversion of semiconducting shells to metallic. Doping can also be a likely solution to overcome the detrimental impacts of defects and contact resistances for a realistic interconnect system. This represents a milestone result, which could enable the success of MWCNTs as a candidate for future back-end-of-line technology nodes interconnects.

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analytical methods and simulation framework to study charge based doping impact on MWCNT interconnects performance and variability.



# Chapter 4

## Copper-Carbon Nanotube Composite

### 4.1 Introduction

The back-end-of-line (BEOL) metallization technology for high-performance and low-power microelectronics, Cu is the material of choice. With scaling of devices, for logic and memory applications up to 14 nm node, the increased current density and reliability requirements still have known material and integration solutions. Such as thinner barrier and adhesion layers, doping of secondary metals to enhance grain boundary electromigration resistance, and integration concepts of selective cappings, that can be some of the adopted solutions for 14 nm node. However, for dimensions below 7 to 10 nm nodes, the decreased volume of available conducting material will force innovative material and integration approaches towards novel interconnect architectures. On the other hand for power and high-performance applications the most critical challenges are high ampacity, thermal conductivity and electromigration resistance. Far away from bulk, Cu conductors can withstand  $10^7 \text{ A/cm}^2$  due to good heat dissipation through thermal contact to the surrounding material. Besides this elementary current carrying capacity, the reliability of state of the art interconnects is closely linked to effects like electromigration (EM). This adverse effect describes the material transport and consequently void formation especially in thin metal lines by a combination of the electron wind force, the temperature gradient induced force, the stress gradient induced force and the surface tension force (Fig. 4.1 (a)). Depending on the design of the interconnect layout and the used metallization scheme, the dominance of each driving force can differ. Even at the current scaling node of CMOS technology, current carrying capacity and reliability are among the main reasons for the trend that the continuous scaling of transistors no longer automatically leads to “performance scaling” (i.e., increased performance per transistor). In this chapter, we address these issues by proposing the copper-carbon nanotube composite as a potential candidate for global interconnects. To this end, the electrical-thermal effect of copper-carbon nanotube composite is characterized after putting forward a physical based electrical-thermal modeling of the composite.

Figure 4.1 (b) shows the electrical performances of different materials, includ-

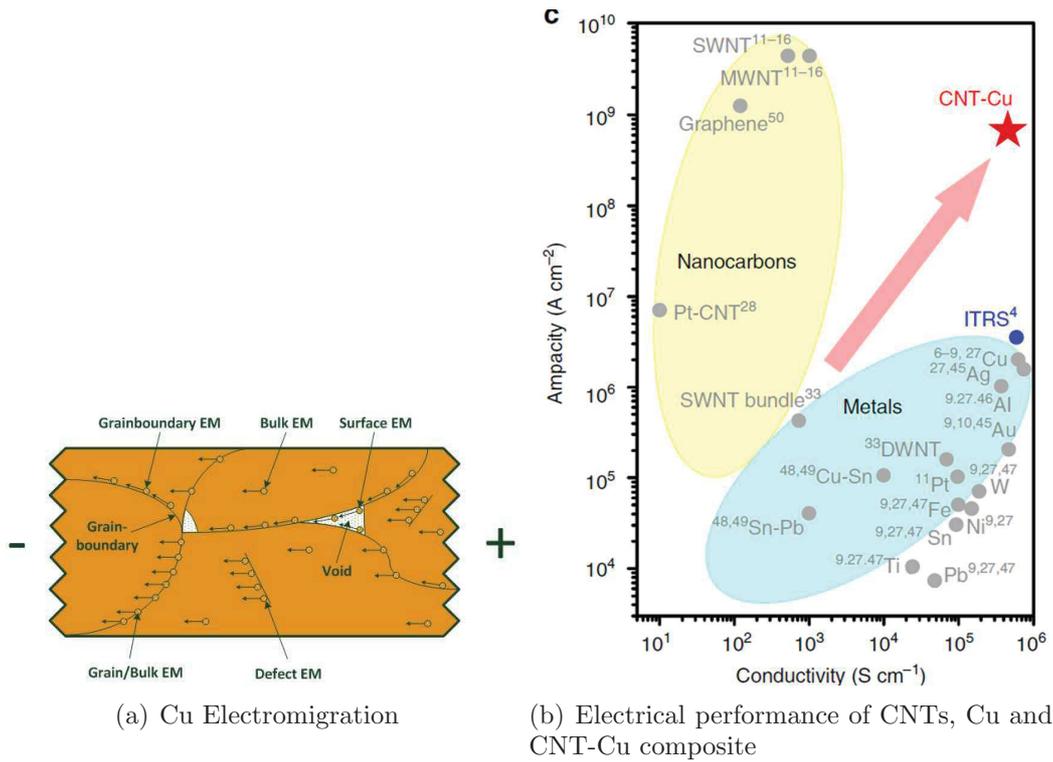


Figure 4.1: (a) Cu electromigration: 1) Bulk EM, 2) Grain boundary EM, 3) Grain/Bulk EM, 4) Defect EM, 5) Surface EM. (b) Performances of Cu-CNT composite from [144].

ing CNT-Cu composite from [144]. CNTs has been studying as a potential Cu replacement owing to their excellent electrical properties in terms of conductivity, ampacity and high frequency characteristics. However, compared with the nearly perfect CNTs studied at the fundamental level, the CNTs integrated with functional device in the system level show much lower performance improvement. As a consequence, combinations of CNTs with copper were envisioned [47]. Initial experimental realizations focused on a “bulk” approach where a mixture of CNTs and Cu is deposited from a solution on the target substrate [99, 174, 6]. This approach demonstrated mitigated performances for interconnect, such that focus is now almost exclusively on composite materials where the CNTs are aligned with respect to the current flow (referred to as aligned CNT-Cu composite).

Chai et al [24, 25, 26] first demonstrated the fabrication of vertical interconnects using aligned CNT-Cu composite materials in 2007 by first growing vertically aligned CNTs before filling the voids between CNTs with Cu through an electroplating method. It was shown that this material could reach low, Cu-like, resistivity but was more resistant to electromigration than Cu. More recently, a renewed interest for this material was generated by the work of Hata group [144] claiming a 100 fold increase in current carrying capacity of aligned CNT-Cu material compared to pure Cu (Fig. 4.1 (b)). Several groups are now working worldwide on the integration of aligned CNT-Cu composite materials in interconnect structures [51, 52, 106, 70].

Apart from the CNT-Cu formation process development, theoretical physics based compact modeling needs to be investigated as fundamental support and understood for further pushing this technology as viable solution for next generation conventional Cu replacement interconnects. In this chapter, we study the electrical-thermal properties for pure Cu and standalone SW and MW CNTs. We explore the electrical-thermal behaviours of SWCNT-Cu and MWCNT-Cu composite by constructing physical based electrical-thermal models.

## 4.2 Copper, and CNT Electrical-Thermal Properties

In this section, we present electrical-thermal properties for copper and CNT with their various temperature dependent physical parameters.

### 4.2.1 Copper electrical-thermal transport

#### Copper electrical-thermal resistivity

Copper interconnect resistivity is often defined by the wire geometries as bulk metal materials. With the wire size shrinking and limitations of photo-lithography technology, finer copper lines resistivity becomes even more sensitive to the size effect [142] as important line edge roughness (LER) become more dominant. New Cu interconnect resistivity model including LER effects has been proposed and measured experimentally in [101]. This model has been well used to estimate the resistivity for advanced technology nodes of Cu interconnect.

$$\rho_{eff} = \frac{\rho_0}{\sqrt{1 - (u/W)^2}} \cdot (GB_{scat} + 0.45(1 - p) \frac{\lambda}{W} (W/T + (1 - (u/W)^2))) \quad (4.1)$$

$$GB_{scat} = \frac{1}{3} \left[ \frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln \left( 1 + \frac{1}{\alpha} \right) \right]^{-1} \quad (4.2)$$

$$\alpha = \frac{\lambda}{d} \frac{R}{1 - R} \quad (4.3)$$

In equation 4.1,  $u/W$  represents the LER, where  $u$  is the edge roughness and  $u = 0$  indicates the perfect line without roughness.  $W$  and  $T$  are width and thickness of interconnects respectively.  $\rho_0$  is the Cu bulk resistivity.  $\lambda$  is the Cu electron mean free path ( $\lambda_{Cu} \sim 40\text{nm}$ ). Sidewall boundary scattering is related to the specularity parameter,  $p$ , a fitting parameter, which represents the portion of electrons that are scattered specularly at the wire sidewall.  $p$  can vary from 0 to 1. A specularity of 1 means all electrons have a specular reflection at the conductor surface / sidewall. This means elastic collisions of electrons and their momentum are conserved in their original travelling direction. If  $p = 0$ , all electrons colliding at the conductor surface experience a diffusive scattering process. Grain boundary scattering is shown in equations 4.2 and 4.3, which capture the quantum mechanical barrier impact on

conducting electrons encountering at the conductor material grain boundaries.  $R$  is the reflectivity parameter, indicates the fraction of electrons scattered at the grain boundaries due to the quantum mechanical barrier effect.  $R = 1$  and  $0$  represent the complete scattering and total transmission at grain boundaries respectively.  $d$  denotes the average distance that an electron can travel between grain boundaries. For temperature dependent thermal-resistivity, we use a linear approximation as below:

$$\rho_{Cu}(T) = \rho_{eff}(1 + \mu(T - T_0)) \quad (4.4)$$

where,  $\rho_{eff}$  for 7 nm node is taken as  $11.7 \cdot 10^{-8} \Omega \cdot m$ .  $\mu$  is the temperature coefficient of Cu resistance, and equals  $0.003862 \text{ K}^{-1}$ .  $T_0$  is set to be 300 K.

Copper under high bias or current supply, has self-heating effects, also known as joule heating. Joule heating is the process that a current flowing through a conductor can produce heat on the conductor. The heat production is an ohmic effect or resistive effect. On the one hand, high resistance metals have more joule heating under the same current input. On the other hand, for metal conductor, high thermal effect (i.e., joule heating) will increase the metal conductor resistivity. Therefore, interconnect lines with high current density always suffer from self-heating issues. Cu has a measured thermal conductivity of  $401 \text{ W/m/K}$  [48]. Equation 4.5 describes the joule heating per unit length of Cu. There is also contact resistance  $R_{cont}$  of Cu. The  $R_{cont}$  is used for current calculation (when bias voltage is provided) but is not considered for thermal heating calculation. In this chapter, we focused on material intrinsic properties and we did not consider the impact of contacts.

$$p'_{Cu} = I^2 R_{cu} / L \quad (4.5)$$

## 4.2.2 Thermal transport in CNT

### Temperature dependent CNT electron Mean Free Path

Carbon nanotube as 1D quantum wire, is known for having a good thermal conductivity. Measured CNT thermal conductivity varies from  $1750 \text{ W/m/K}$  to  $5800 \text{ W/m/K}$  [62]. In the previous chapters, we have presented pristine and doped SW/MW CNT electrical models. In this chapter, we incorporate the thermal effect into our electrical models. Temperature-dependent electrical resistance of CNT relationship is described as in equation 4.6:

$$R_{CNT-tot}(T) \sim (R_{cont}(T), R_{Quantum}(T), R_{scattering}(T)) \quad (4.6)$$

where  $R_{cont}$  is the contact resistance. As metallic CNTs have limited electron density of states(DOS) due to its 1D quantization, hence contacting CNTs with metal that has much higher DOS that can cause high contact electrical and electrical-thermal resistance. High contact resistance can significantly increase the CNT interconnect total resistance, thus altering total current flowing through CNT that induce joule heating effect. Fundamental first principle simulations need to be performed in order to understand clearly the electrical-thermal effect at the CNT-metal interfaces. However, as our focus is to develop a macroscopic compact electrical-thermal model,

we therefore set contact resistance as a numerical variable without providing more physical explanation.  $R_{Quantum}$  is the quantum resistance of CNTs, which is the intrinsic resistance of CNTs that is a constant used throughout this work.  $R_{scattering}$  plays an important role in determining the CNT thermal behaviour because thermal effect can induce additional scattering in the conductors. For CNTs, we include mean free path (MFP) approximation that describes different scattering mechanisms in CNT. For CNT mean free path calculation, Matthiessen's rule [124, 108, 123] is widely used in the literature, as shown in equation 4.7:

$$\lambda = \left( \frac{1}{\lambda_{ac}} + \frac{1}{\lambda_{op,ems}^{fld}} + \frac{1}{\lambda_{op,ems}^{abs}} + \frac{1}{\lambda_{op,abs}} \right)^{-1} \quad (4.7)$$

where  $\lambda_{ac}$  is the mean free path due to acoustic phonon scattering;  $\lambda_{op,ems}^{fld}$  is the mean free path from optical phonon emission after the electrons gain enough energy from electric field;  $\lambda_{op,ems}^{abs}$  is the mean free path due to optical phonon emission after absorption and  $\lambda_{op,abs}$  is from optical phonon absorption. All these mean free paths are temperature dependent and can be calculated by following equations:

$$\lambda_{ac} = 400460 \times \frac{D_{CNT}}{T} \quad (4.8)$$

$$\lambda_{op,abs} = 56.4 \times D_{CNT} \frac{N_{op}(300) + 1}{N_{op}(T)} \quad (4.9)$$

$$\lambda_{op,ems}^{abs} = \lambda_{op,abs} + 56.4 \times D_{CNT} \frac{N_{op}(300) + 1}{N_{op}(T) + 1} \quad (4.10)$$

$$\lambda_{op,ems}^{fld} = \frac{\hbar\omega_{op} - \kappa T}{qV/L_{CNT}} + 56.4 \times D_{CNT} \frac{N_{op}(300) + 1}{N_{op}(T) + 1} \quad (4.11)$$

$$N_{op}(T) = \frac{1}{\exp((\hbar\omega_{op})/(\kappa T)) - 1} \quad (4.12)$$

where  $N_{op}(T)$  is the average number of optical phonons defined by Bose-Einstein distribution. Optical phonon energy is given by  $\hbar\omega_{op}$ , and  $\hbar$  is the plank constant, equal to  $6.582 \cdot 10^{-16}$  eV/s.  $\omega_{op}$  is the phonon frequency equal to  $0.027 \cdot 10^{16}$  s<sup>-1</sup> and  $\kappa$  is Boltzmann constant equal to  $8.617 \cdot 10^{-5}$  eV/K. We can see that the phonon scatterings (and its mean free path) of CNT depends on temperature, applied bias and CNT diameter.

We incorporate aforementioned temperature-dependent MFP into our models. And CNT joule heating is derived in equation 4.13:

$$p'_{CNT} = I^2 R_{CNT} / L \quad (4.13)$$

Meanwhile, CNT thermal conductivity is also temperature dependent. Hence, to improve the accuracy of our model, we employed a relatively complete thermal conductivity [125] in our model. CNT thermal conductivity is length and temperature dependent as described in equation 4.14. Similarly to previous Cu joule heating relationship, the  $R_{cont}$  is used for current calculation (when bias voltage is provided) but is not considered for joule heating calculation and we did not focus on the impact

of contact resistance for CNTs joule heating in this chapter.

$$k(L, T) = [3.7 \times 10^{-7}T + 9.7 \times 10^{-10}T^2 + 9.3(1 + 0.5/L)T^{-2}]^{-1} \quad (4.14)$$

this equation can be approximated by  $1/T$  when temperature is above room temperature but when temperature is approaching the breaking-down point,  $1/T^2$  also needs to be included.

## 4.3 Electrical-thermal Modeling and Simulation results

### 4.3.1 Electrical-thermal model & simulation results in Cu

#### Copper electrical-thermal model

In order to study in the next sections the Cu-CNT composite electrical-thermal effect, we started by modeling only Cu on a substrate, with the sketch shown in Fig. 4.2. Copper has current flowing through, then induces self-heating and has heat diffusion to the substrate.

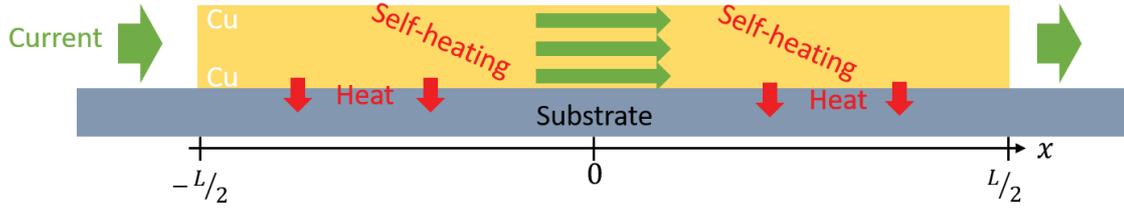


Figure 4.2: Pure copper electrical-thermal modeling sketch.

To understand the thermal effect of copper, we need to solve the heat conduction equation for copper.

$$A_{cu} \nabla(k_{cu} \nabla T_{cu}) + p'_{cu} - g_{cu-sub}(T_{cu} - T_{sub}) = 0 \quad (4.15)$$

where the Cu thermal conductivity variations with temperature, self-heating and heat diffusion to the substrate are all included. For heat diffusion coefficient  $g$ , it is dielectric substrate material dependent [16] and described as in equation 4.16 for a cylindrical geometry conductor lying on substrate [123]. For a thin Cu metal line on substrate we can approximately replace the cylinder conductor diameter  $d$  by the width of narrow bulk metal lines.

$$g_{ox} = \frac{\pi k_{ox}}{\ln(8t_{ox}/\pi d)} \quad (4.16)$$

We developed a self consistent models which are solved by using a numerical

shooting method [127], and the boundary conditions, namely temperatures at contacts and substrate are set to be 300 K. For  $g$ , we have chosen numerically 0.1, 0.2 and 0.3 W/m/K based on the experimental results in [123]. The simulation flow is shown in Fig. 4.3. We employ this flow for all the electrical-thermal simulations in this chapter.

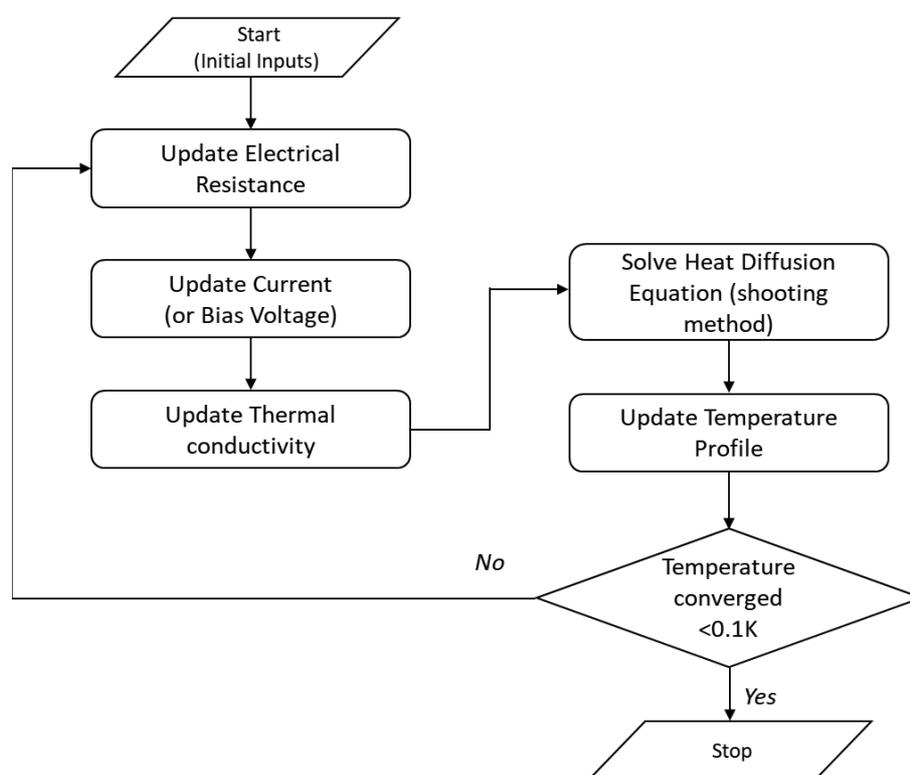


Figure 4.3: Interconnect (includes Cu, CNT, and Cu-CNT) unit cell heat conduction self consistent simulation flow.

## Simulation results

We first started by studying the copper interconnect for different metal level dimensions for 7 nm technology node. Detailed dimensions data are shown in the Table 4.1 [146]. In this chapter, we have chosen interconnect sizes for intermediate (M2:M3) and semi-global (M4:M6) metal layers based on 7 nm technology node.

Figures 4.4 and 4.5 present the temperature profiles of 7 nm node Cu line interconnects for metal level 2-3 and 4-6, respectively. We notice that when Cu dimensions remain unchanged, as  $g$  increases, there is better heat diffusion to substrate, hence, making Cu have a lower temperature profile. As  $g$  increase from 0.1 W/m/K to 0.3 W/m/K, Cu maximum temperature can be decreased more than 1000 K to less than 650 K for applied voltage of 0.9 V. The heat diffusion to the substrate is more important when the applied voltage is increased. Thus, if high electrical bias is applied on the interconnect, it will be important to optimize the heat diffusion to substrate and environment. If we look into the same heat diffusion coefficient to substrate (i.e., the same  $g$ ), we find that as Cu dimension increases, Cu resistance

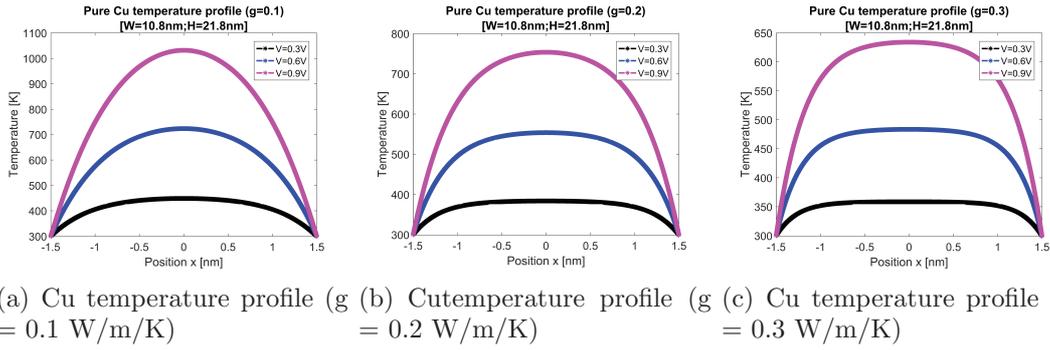


Figure 4.4: Pure Cu interconnect metal temperature profile for 7 nm node metal level 2-3 with heat diffusion coefficient to the substrate (a)  $g = 0.1$  W/m/K. (b)  $g = 0.2$  W/m/K. (c)  $g = 0.3$  W/m/K.

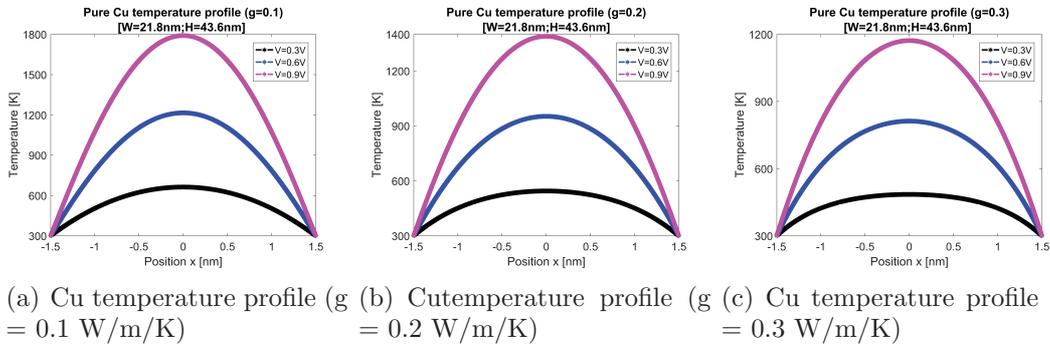


Figure 4.5: Pure Cu interconnect metal temperature profile under various electrical bias for 7 nm node metal level 4-6 with heat diffusion coefficient to the substrate (a)  $g = 0.1$  W/m/K. (b)  $g = 0.2$  W/m/K. (c)  $g = 0.3$  W/m/K.

decreases, thus more current flowing through the Cu metal, and hence, Cu metal joule heating increases which causes higher temperature profile.

In Fig. 4.6 and Fig. 4.7, we show the I-V variations and resistance variations as a function of applied voltage. For an ideal conductor, current increases with applied voltage. After taking into the account the self-heating effect, conductor resistance increases with temperature. Therefore, current of the realistic conductor is no more linearly varied with applied voltage but showing a saturated trend, or even drops down when self-heating is dominating the conductor resistance. In Fig. 4.6, the saturation trend of I-V curves are shown for Cu lines in (a) metal layer 2-3 and (b) metal layer 4-6. Even though larger Cu lines have less resistance and higher current flowing, however, we deduce from Fig. 4.4 and 4.5, larger metal lines have higher temperature profiles, hence we can not easily conclude that larger metal lines suffered less self-heating issues. We extract the maximum current carrying density (Ampacity) of these two case studies. We obtained  $1.49 \cdot 10^8$  A/cm<sup>2</sup> and  $8.42 \cdot 10^7$  A/cm<sup>2</sup> current carrying ampacity for metal 2-3 and metal 4-6, respectively under applied voltage 1.8 V, which is partly because metal 4-6 have larger cross section

area.

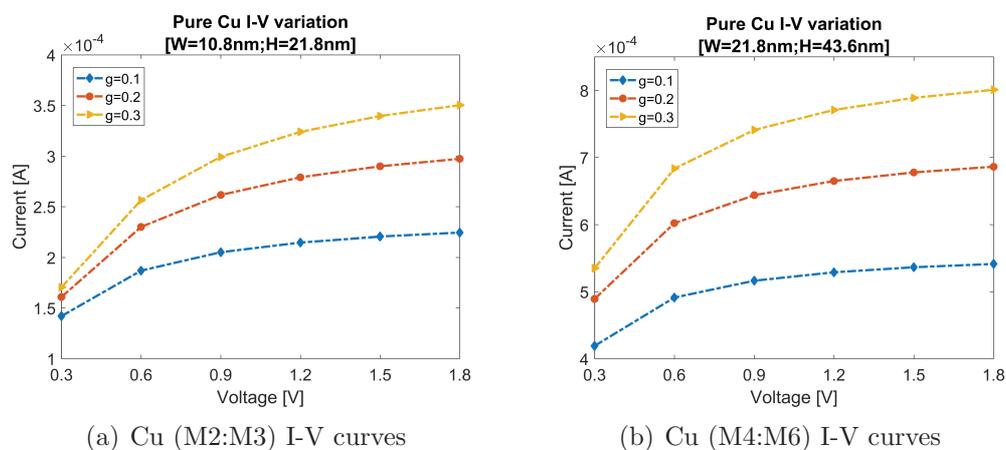


Figure 4.6: Pure Cu interconnect metal I-V variations under different heat diffusion coefficient to the substrate for (a) Metal level 2-3. (b) Metal level 4-6. The unit of heat diffusion coefficient  $g$  is W/m/K.

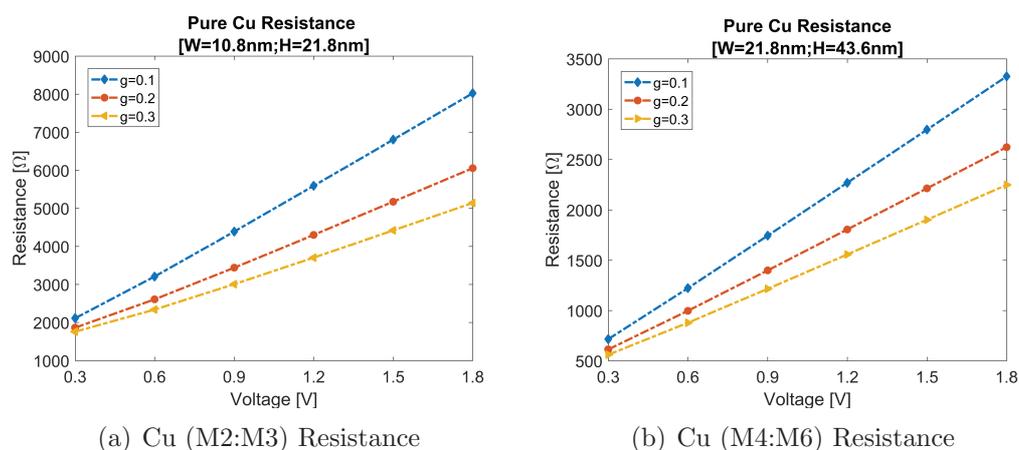


Figure 4.7: Pure Cu interconnect metal Resistance variations under different heat diffusion coefficient to the substrate for (a) Metal level 2-3. (b) Metal level 4-6. The unit of heat diffusion coefficient  $g$  is W/m/K.

In Fig. 4.7, we observed that with the increase of applied voltage from 0.3 V to 1.8 V, Cu line resistances are increased by  $\sim 4X$  and  $\sim 5X$  for metal level 2-3 and 4-6 respectively.

### 4.3.2 Electrical-thermal model & simulation results in CNTs

In this section, we present the electrical-thermal transport model in standalone SWCNT and MWCNT on a substrate.

### Electrical-thermal model

We employ a similar modeling strategy as that for Cu lines. We have the SWCNT or MWCNT lying on a substrate. Electrical bias (or current) is applied on CNT line. CNT has self-heating along the tube and heat diffusion to substrate. CNT electrical-thermal model sketch is shown in Fig. 4.8.

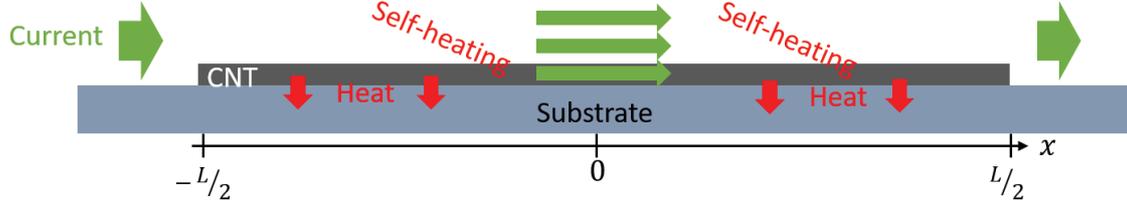


Figure 4.8: Standalone CNT electrical-thermal modeling sketch.

$$A_{CNT} \nabla(k_{CNT} \nabla T_{CNT}) + \dot{p}_{CNT} - g_{CNT-sub}(T_{CNT} - T_{sub}) = 0 \quad (4.17)$$

We solve the heat conduction equation for both SWCNT and MWCNT. Self-heating, temperature dependent thermal conductivity and heat diffusion terms are aforementioned in equations 4.13, 4.14 and 4.16. We solve the heat conduction equation by the same self consistent numerical method as that for Cu model. We also update CNT resistance calculation as shown in equation 4.18 which has temperature, applied voltage and length dependencies.

$$R_{CNT}(V, T) = R_c + \frac{h}{4q^2} \left\{ 1 + \int_{-L/2}^{L/2} \frac{dx}{\lambda_{eff}[V, T(x)]} \right\} \quad (4.18)$$

### Simulation results

Based on the electrical-thermal models, we performed simulations for both SWCNT and MWCNT with diameter of 3 nm and 6 nm respectively. The reason that we selected 6 nm for MWCNT is based on experimental measurements in our H2020 CONNECT project. However, due to the timelines of this project and the thesis, we were not able to compare our simulation results to experimental data at the time thesis submission.

In the following sections, we present temperature profiles, I-V and resistance variations for both SWCNT and MWCNT.

- Standalone SWCNT Temperature profile & I-V & Resistance variations

In Fig. 4.9, we notice that the increase in temperature with applied voltage is much lower than that of Cu. For example, under 1 V of applied voltage, SWCNT maximum temperature varies from 360 K to 320 K when  $g$  changes from 0.1 W/m/K to 0.3 W/m/K. We expect little increase in SWCNT temperature when small bias

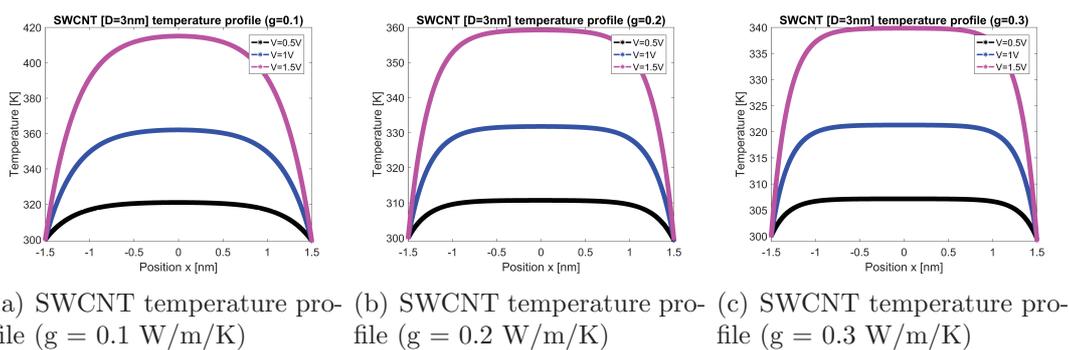


Figure 4.9: SWCNT ( $D = 3$  nm) interconnect temperature profile with heat diffusion coefficient to the substrate (a)  $g = 0.1$  W/m/K. (b)  $g = 0.2$  W/m/K. (c)  $g = 0.3$  W/m/K.

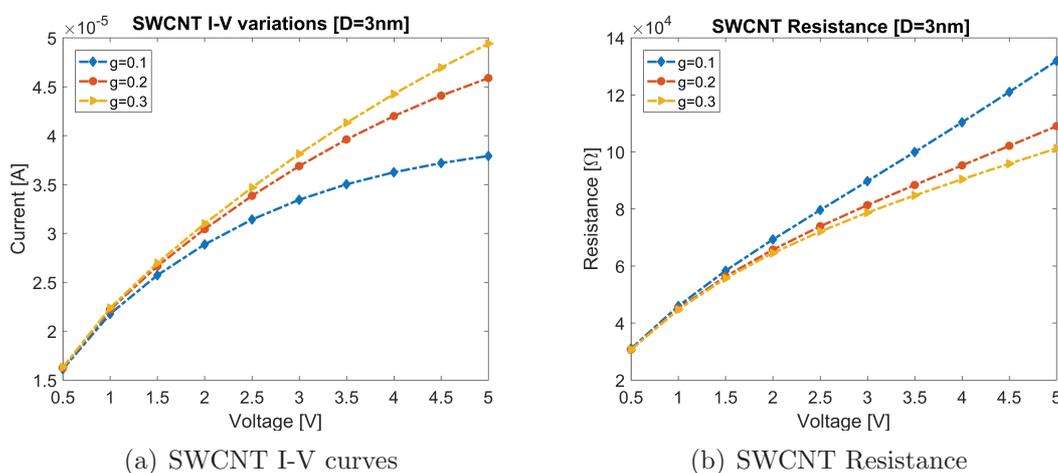


Figure 4.10: SWCNT interconnect (a) I-V variations (b) resistance variations under different heat diffusion coefficient  $g$  values (W/m/K) to the substrate.

is applied for  $g = 0.3$  W/m/K. Similar to Cu, large  $g$  values will directly improve the SWCNT thermal dissipation. We further analyse SWCNT I-V variations and resistance changes as shown in Fig. 4.10 (a) and (b), respectively. In (a), we notice that the current flowing in SWCNT is one order of magnitude lower than that in Cu, and this is due to the high resistance of SWCNT, as shown in (b). SWCNT has only one single conducting shell and high quantum resistance which induce significant self heating effect. Even though the effective resistance of SWCNT is very high, meaning less current passing through, due to its small cross sectional area, we can still extract a  $3.8 \cdot 10^8$  A/cm<sup>2</sup> of ampacity and a conductivity of  $8.6 \cdot 10^4$  S/cm under applied voltage of 1 V.

- Standalone MWCNT Temperature profile & I-V & Resistance variations

We continue to analyse the MWCNT electrical-thermal effects. From Fig. 4.11, we notice that the maximum temperatures are higher than that in SWCNT cases with different  $g$  values, and MWCNTs have still better thermal dissipation than that for Cu lines. For  $g = 0.3$  W/m/K, under 0.3 V applied bias, only 10 K of maximum temperature is found. We observed that CNTs (SW and MW) have in general better temperature dissipation than Cu lines, which can be explained by their better thermal conductivities. Concerning the I-V and resistance variations for MWCNT, they are shown in Fig. 4.12 (a) and (b), respectively. MWCNT has higher current than SWCNT and is similar to that in Cu lines. In this case study, MWCNT shows a more obvious trend of current saturation than what is shown in SWCNT case. We observed a current drop on MWCNT when  $g = 0.1$  W/m/K after applying a voltage more than 0.5 V. For a small heat diffusion coefficient to substrate, self heating becomes dominant under high bias, while for lower bias ( $<0.2$  V), there is not obvious distinction of current for different  $g$  values. This is also shown in the resistance variation where the resistances are increased in the same manner under lower bias. However, when bias voltage is 0.8 V, resistance has been increased by almost 5X for  $g = 0.1$  W/m/K. We have calculated the ampacity and conductivity for MWCNT under 0.8 V and  $8.2 \cdot 10^8$  A/cm<sup>2</sup> and  $3 \cdot 10^5$  S/cm are obtained respectively.

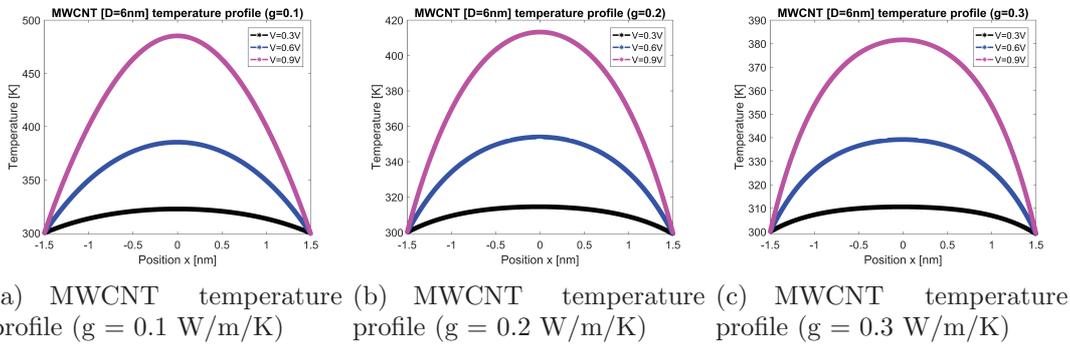


Figure 4.11: MWCNT ( $D = 6$  nm) interconnect temperature profile with heat diffusion coefficient to the substrate (a)  $g = 0.1$  W/m/K. (b)  $g = 0.2$  W/m/K. (c)  $g = 0.3$  W/m/K.

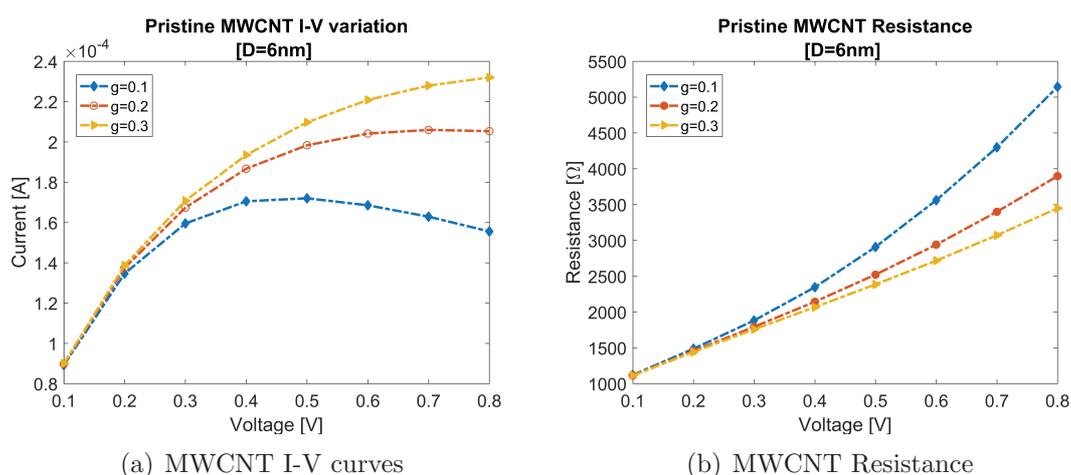


Figure 4.12: MWCNT ( $D = 6 \text{ nm}$ ) interconnect (a) I-V variations, (b) Resistance variation under different heat diffusion coefficient  $g$  ( $\text{W/m/K}$ ) to the substrate.

### 4.3.3 Electrical-thermal model in Cu-CNT composite

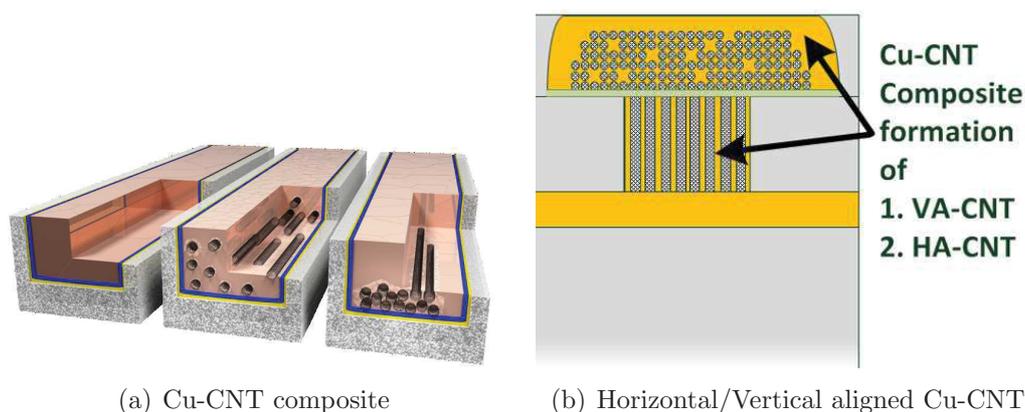


Figure 4.13: (a) Cu-CNT composite for global interconnects (b) Horizontally and vertically aligned Cu-CNT composite for global interconnects.

Figure 4.13 illustrates the sketch of Cu-CNT composite interconnects using vertically and horizontally aligned CNTs deposited by Copper. Cu-CNT composite material formation process is challenging and here we only investigate its electrical-thermal properties by theoretical modeling. To have a compact model for Cu-CNT composite, we start by looking into a unit cell of composite material, composed by a standalone SW or MW CNT and surrounded by copper. As shown in Fig. 4.14, the unit composite cell lies on a substrate.

When we apply a current or electrical bias to the composite interconnect, current passes through both copper and CNT (see Fig. 4.15). Here, we do not consider the heat exchange between the Cu and CNT based the assumption that the thermal re-



Figure 4.14: Cu-CNT composite unit cell geometry sketch.

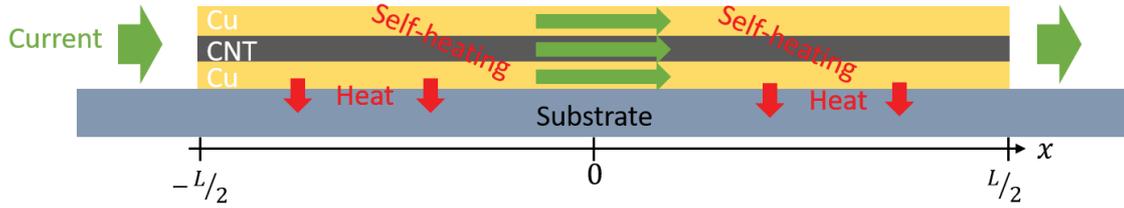


Figure 4.15: Cu-CNT composite unit cell electrical-thermal modeling sketch.

sistance between Cu and CNT is relatively ignorable compared with that between Cu and the substrate. Similarly, we assume that there is no current exchange between CNT and Cu on the same cross section because the CNT and Cu are in parallel and have identical voltage distribution along the current flowing direction. The reasons that we did not consider more in depth the electrical and thermal exchanges are 1) more fundamental physical mechanisms need to be studied by using first principle based modeling and simulations and 2) much more complex numerical models need to be developed. These reasons are out of the scope of this thesis. Hence, in other words, in this thesis, the CNT and Cu are perfectly thermally coupled and exchange heat with the substrate and electrodes of the interconnect. Furthermore, the equivalent resistance directly affects the total current flowing into both parts. In the near future, we would like to investigate more in depth the electrical and thermal exchange at the interface of Cu and CNTs, which can be an important complement to this model.

$$\begin{aligned}
 A_{CNT} \nabla(k_{CNT} \nabla T_{CNT}) + p'_{CNT} &= 0 \\
 A_{Cu} \nabla(k_u \nabla T_{Cu}) + p'_{Cu} - g_{Cu-sub}(T_{Cu} - T_{sub}) &= 0
 \end{aligned}
 \tag{4.19}$$

For Cu-CNT composite, we need to simultaneously solve both the heat conduction equations for CNT and Cu (see equation 4.19). In this case, only outer copper will have the heat diffusion term and CNT will only remain the self-heating term. We solve the two differential equations self consistently by updating each time their temperature profiles and resistances. Updating equivalent total resistance will update the total current in the composite, then update the self-heating on each

of them. When the temperature has a convergency of  $T < 0.1$  K, the simulation iteration stops. Simulation flow is basically the same to that in Fig. 4.3.

#### 4.3.4 Thermal effect simulation results of Cu-CNT composite

We first study the temperature variation of Cu-CNT under different electrical bias applied, as well as different heat diffusion coefficients to substrate. Composite unit cell dimensions have the same dimensions as Cu metal level 2-3 and 4-6 for 7 nm technology node as shown in Table 4.1. CNTs dimensions are 3 nm and 6 nm for SWCNT and MWCNT respectively as in previous sections.

##### SWCNT-Cu composite

In Fig. 4.16 and 4.17, we show the temperature variations of SWCNT-Cu composite. We notice that the composite has similar temperature profiles as SWCNT and much lower than that of Cu. SWCNT-Cu composite has maximum temperatures slightly higher than those of SWCNT, which is due to the additional Cu in parallel, leading to larger current under the same bias voltage. Thanks to the higher SWCNT thermal conductivity than that of Cu, the composite has thus much smaller temperature profile. Comparing Fig. 4.16 and 4.17, we find the same trend that larger dimension of composites has higher temperature due to more current flowing through and induce higher self heating. We also notice that SWCNT-Cu composite is relatively more sensitive to the applied bias than the standalone SWCNT. For standalone SWCNT, there is 50 K of the maximum temperature increased (from 310 K to 360 K) when applied voltage increases from 0.5 V to 1V for  $g = 0.2$  W/m/K. Nevertheless for SWCNT-Cu composite, with the same  $g$  value, the maximum temperatures are increased by 70 K and 220 K with a very small voltage change (from 0.1 V to 0.3 V) for dimensions corresponding to metal level 2-3 and 4-6 respectively. (4.16 (b) and 4.17 (b)).

I-V and resistance variations are shown in Figs. 4.18 and 4.19. We notice that the currents are similar to that in SWCNT and the resistances are much lower. This is due to the parallel conductors between SWCNT and Cu, indicating that the equivalent total resistance is limited by the smaller one. And the total SWCNT-Cu resistance is the lowest resistance compared to Cu and SWCNT knowing that composite dimensions are the same as Cu dimensions taking as in Table 4.1 and SWCNT has a diameter of 3 nm.

We extract the ampacity and conductivity of SWCNT-Cu composite for those two dimension of metal level cases. For dimensions corresponding to metal level 2-3, the composite has ampacity of  $1.4 \cdot 10^8$  A/cm<sup>2</sup> and conductivity of  $2.8 \cdot 10^4$  S/cm for applied voltage of 1 V and  $g = 0.3$  W/m/K. For metal level 4-6,  $V = 1$  V and  $g = 0.3$  W/m/K, the ampacity and conductivity are calculated as  $8 \cdot 10^7$  A/cm<sup>2</sup> and  $2.4 \cdot 10^4$  S/cm. We notice that, in larger dimensions SWCNT-Cu composite, there is lower ampacity and conductivity. The main reasons for this phenomenon are that: 1) ampacity and conductivity are cross sectional area related. Even though the current and conductance is higher, the corresponding cross sectional area is larger as well,

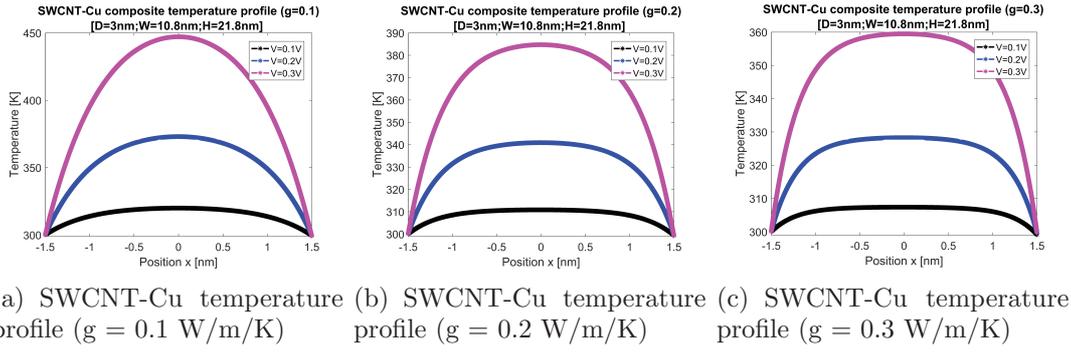


Figure 4.16: SWCNT-Cu composite interconnect temperature profile.  $D_{\text{swcnt}} = 3\text{nm}$ , and surrounding Cu dimensions are taken for 7 nm node metal level 2-3. Temperature variations under different heat diffusion coefficients to the substrate (a)  $g = 0.1$  W/m/K. (b)  $g = 0.2$  W/m/K. (c)  $g = 0.3$  W/m/K.

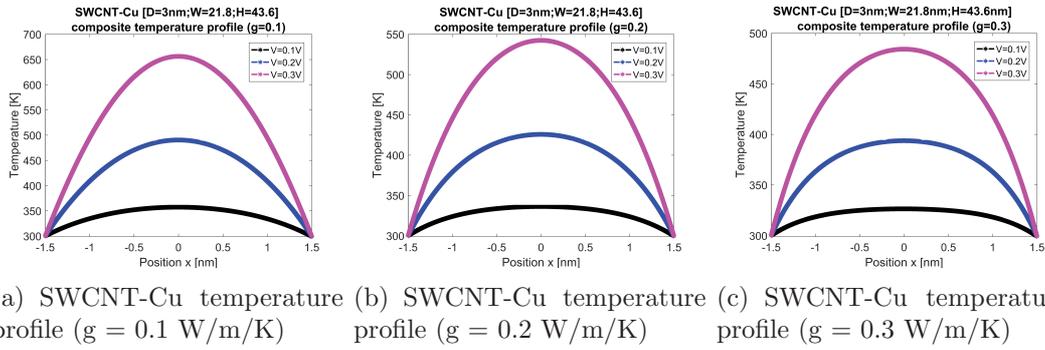


Figure 4.17: SWCNT-Cu composite interconnect temperature profile.  $D_{\text{swcnt}} = 3\text{nm}$ , and surrounding Cu dimensions are taken for 7 nm node metal level 4-6. Temperature variations under different heat diffusion coefficients to the substrate (a)  $g = 0.1$  W/m/K. (b)  $g = 0.2$  W/m/K. (c)  $g = 0.3$  W/m/K.

leading to smaller ampacity and conductance. 2) due to thermal effect, current and resistance under increased applied voltages are not in linear relationship with dimensions. Hence, we can not simply conclude that larger dimension composite cell should have better ampacity or conductivity. 3) in our simulations,  $g$  is not varied with the cross section or transverse size, such as the diameter of CNT. This can bring some inaccuracy as the  $g$  is expected to be larger when the interconnect has larger surface interacted with the substrate. To summarize, there are five factors playing a role in determining the interconnect ampacity and conductivity, such as dimensions, resistance, current, self heating and heat diffusion to environment. So, contradictory with the traditional electrical performance of a conductor with its transverse size relationship, the interconnect conductivity is not increased with its transverse size but may show the opposite trend after taking the self heating thermal effect into consideration.

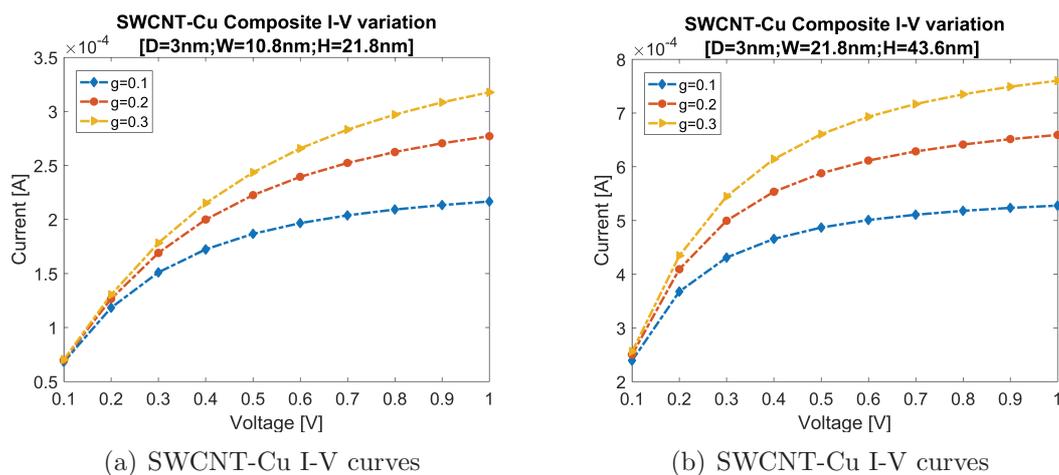


Figure 4.18: SWCNT-Cu composite interconnect I-V variations under different heat diffusion coefficient to the substrate for (a) surrounding Cu with dimension of metal level 2-3. (b) surrounding Cu with dimension of metal level 4-6. SWCNT with its diameter of 3 nm. The unit of heat diffusion  $g$  coefficient is W/m/K.

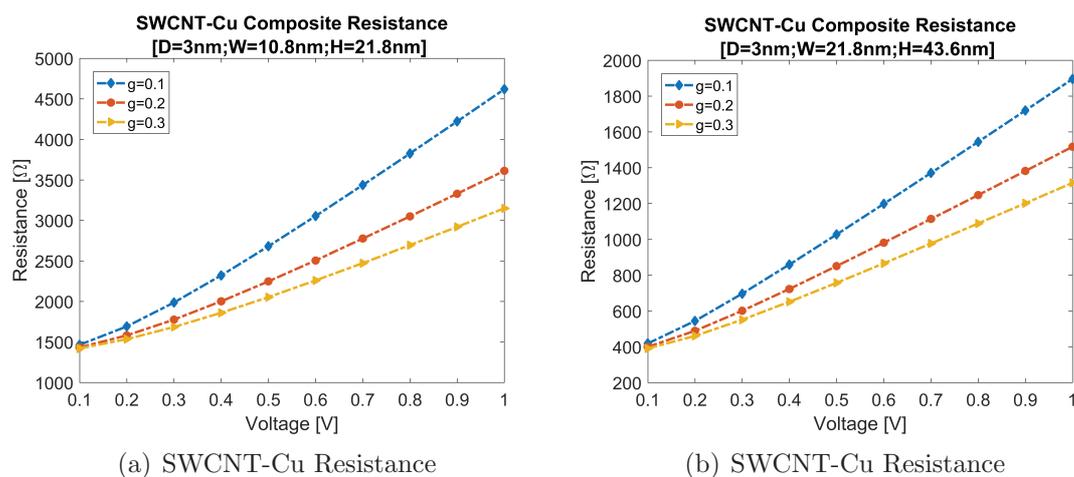


Figure 4.19: SWCNT-Cu composite interconnect Resistance variations under different heat diffusion coefficient to the substrate for (a) surrounding Cu with dimension of metal level 2-3. (b) surrounding Cu with dimension of metal level 4-6. SWCNT with its diameter of 3 nm. The unit of heat diffusion  $g$  coefficient is W/m/K.

### MWCNT-Cu composite

For MWCNT-Cu composite, we show the temperature profiles in Figs. 4.20 and 4.21 for composite dimensions corresponding to metal level 2-3 and 4-6 respectively. We observe MWCNT-Cu composite has lower magnitude of temperature increase than that in MWCNT. However, if we compare MWCNT-Cu to SWCNT-Cu composite temperature profiles (Fig. 4.16), for  $g = 0.1$  W/m/K, MWCNT-Cu has slightly lower

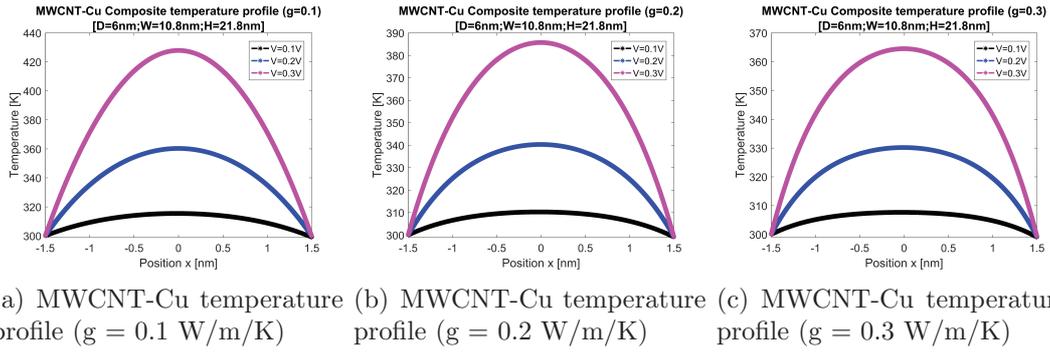


Figure 4.20: MWCNT-Cu composite interconnect temperature profiles.  $D_{\text{mwcnt}} = 6\text{nm}$ , and surrounding Cu dimensions are taken for 7 nm node metal level 2-3. Temperature variations under different heat diffusion coefficients to the substrate (a)  $g = 0.1 \text{ W/m/K}$ . (b)  $g = 0.2 \text{ W/m/K}$ . (c)  $g = 0.3 \text{ W/m/K}$ .

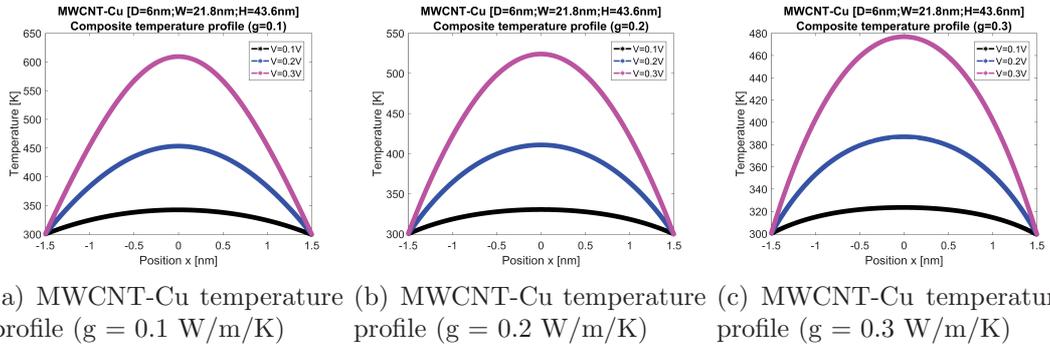


Figure 4.21: MWCNT-Cu composite interconnect temperature profiles.  $D_{\text{mwcnt}} = 6\text{nm}$ , and surrounding Cu dimensions are taken for 7 nm node metal level 4-6. Temperature variations under different heat diffusion coefficients to the substrate (a)  $g = 0.1 \text{ W/m/K}$ . (b)  $g = 0.2 \text{ W/m/K}$ . (c)  $g = 0.3 \text{ W/m/K}$ .

temperature, but for  $g = 0.2 \text{ W/m/K}$  or larger, MWCNT-Cu has a little bit higher maximum temperature than that in SWCNT-Cu under the same applied bias. This can be qualitatively explained as follows: compared with MWCNT-Cu, SWCNT-Cu composite has relatively smaller electrical and thermal conductance, meaning smaller current (and thus self-heating) but also worse heat dissipation in the current flowing direction. So, depending on the mutual competition between the self-heating and heat dissipation, SWCNT-Cu can be of smaller or larger temperature profile than that of MWCNT-Cu. When the  $g$  is small like  $0.1 \text{ W/m/K}$  here, indicating limited heat dissipation into the substrate, the overall interconnect heat dissipation will be more degraded for the SWCNT-Cu than MWCNT-Cu, leading to larger temperature profile for SWCNT-Cu. If  $g$  is increased, such as  $0.2 \text{ W/m/K}$ , then the opposite phenomenon will show, as observed in the simulations. Similar phenomena are also observed for larger dimension composite wires if we compare Figs. 4.21 and 4.17.

Moreover, we show the I-V and resistance variations for MWCNT-Cu composite

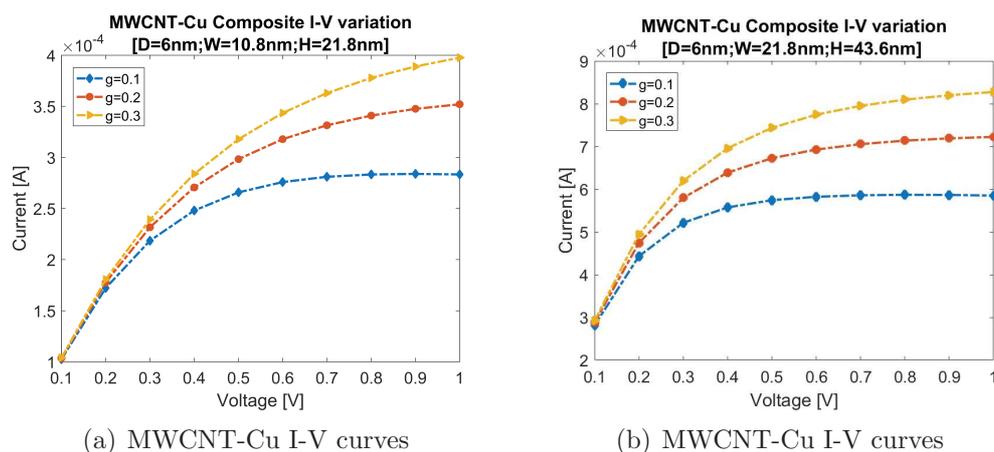


Figure 4.22: MWCNT-Cu composite interconnect I-V variations under different heat diffusion coefficients to the substrate for (a) surrounding Cu with dimensions of metal level 2-3. (b) surrounding Cu with dimensions of metal level 4-6. MWCNT has a diameter of 6 nm. The unit of heat diffusion  $g$  coefficient is W/m/K.

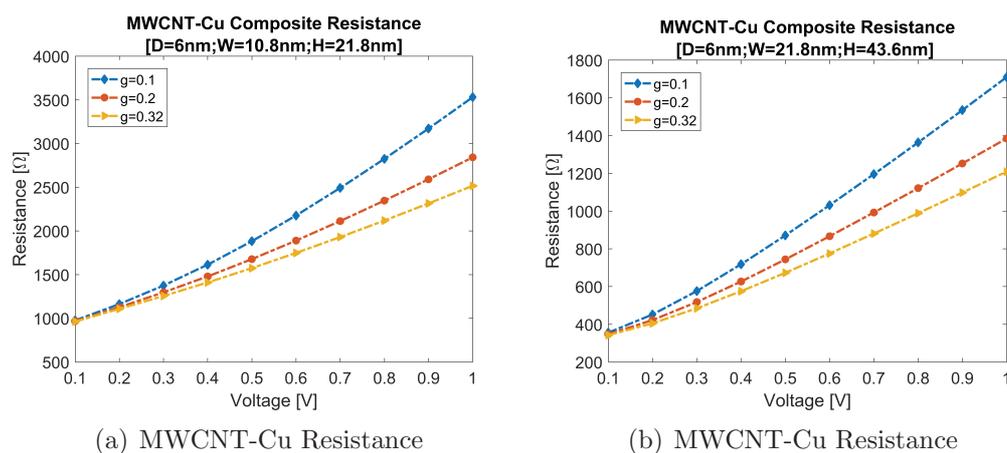


Figure 4.23: MWCNT-Cu composite interconnect Resistance variations under different heat diffusion coefficients to the substrate for (a) surrounding Cu with dimensions of metal level 2-3. (b) surrounding Cu with dimensions of metal level 4-6. MWCNT has diameter of 6 nm. The unit of heat diffusion  $g$  coefficient is W/m/K.

in Figs. 4.22 and 4.23. MWCNT-Cu has higher current and lower resistance for both low level intermediate (metal level 2-3) and global (metal level 4-6) interconnect dimensions than SWCNT-Cu. We calculate the ampacity and conductivity for MWCNT-Cu composite. For intermediate level wire, ampacity of  $1.7 \cdot 10^8$  A/cm<sup>2</sup> and conductivity of  $5.1 \cdot 10^4$  S/cm are found. For global level, the extracted ampacity and conductivity are  $8.6 \cdot 10^7$  A/cm<sup>2</sup> and  $2.6 \cdot 10^4$  S/cm, respectively. We find the same observations as previous for SWCNT-Cu, that dimensions, resistance, current, self heating and heat diffusion coefficient will all impact the finally observed electrical-

thermal performance. Self heating and resistance are not linearly decreased when the interconnect transverse dimensions are increased. This can be understood as that for SWCNT-Cu. Hence, lower ampacity and conductivity can be obtained in larger dimension MWCNT-Cu composite wire as well.

## 4.4 Discussion

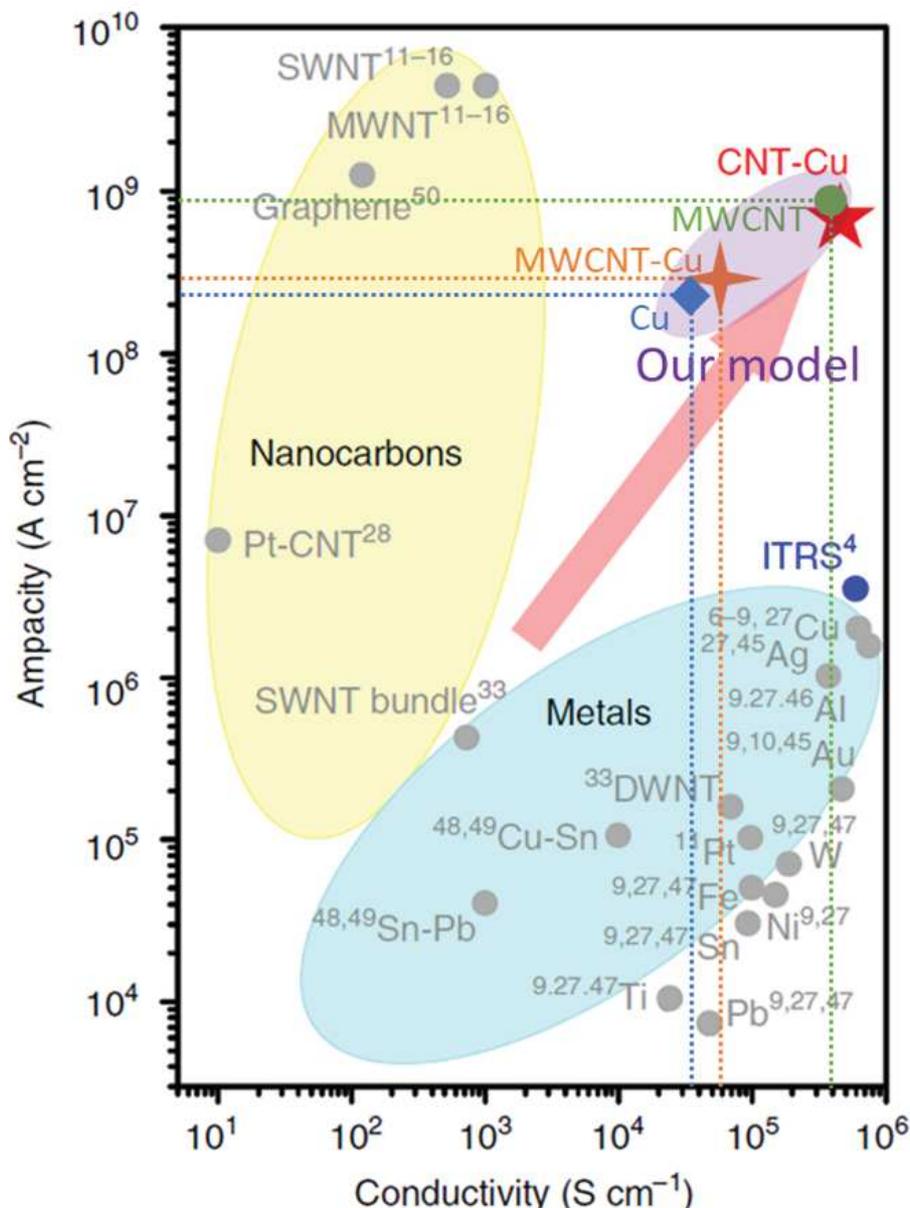


Figure 4.24: Ampacity vs. Conductivity [144].

We develop and evaluate self-consistent electrical-thermal models for different types of Cu, CNTs and CNTs-Cu composite. We have extracted their ampacity and conductivity to understand their potential for interconnects applications. Due

to the lack of our proper experimental measurements, we compare our models to the state-of-the-art literature experimental results in [144] even though there exist many process variations in the experimental measurements such the measurement setup and quality of interconnects, etc. This comparison aims to further propose possible investigations in order to optimize our models.

In Fig. 4.24, it shows the ampacity and conductivity results on various metals and CNT based materials for possible interconnect applications. Our model for MWCNT-Cu composite, with the Cu dimensions of width  $W = 10.8$  nm and height  $H = 21.8$  nm corresponding to on-chip low level intermediate interconnect metal level 2-3 and MWCNT diameter of 6 nm which is chosen based on the individual CVD grown MWCNT process in our project, shows an ampacity of  $1.7 \cdot 10^8$  A/cm<sup>2</sup> and conductivity of  $5.1 \cdot 10^4$  S/cm. We compare this result to the best experimental measurements in [144], and find that the ampacity is in the same order of magnitude while conductivity is less one order of magnitude lower. In [144], the measurements are based on MWCNT bundles which we can expect higher conductivity when the composite is in form of large bundles of CNTs while in our case it is an standalone MWCNT surrounded by Cu. Knowing that, in our test case, the quantum resistance is not involved in self-heating but it does reduce the overall current of the CNT-Cu interconnect. By increasing the number of CNTs in parallel as in the experiments, the equivalent quantum resistance is reduced while the thermal performance are not simultaneously increased. This could be the reason why the experimentally measured CNT-Cu composite has much better conductivity but comparable thermal performance. In addition, in our model, our heat diffusion coefficient to substrate  $g$  is not dependent on the transverse size of the interconnect. In addition, the electrical-thermal performance of composite is strongly dependent on the  $g$ , which is not possible to be extracted by experiments and thus can be very different for the simulation and experiments. Hence, find the conservative results of the composite in this thesis. Furthermore, in [144], deposited Cu materials can be a sort of dopant that results in doping effect to CNTs bundles, which may enhance the composite material conductivity as in the experiments but is not considered in the simulation study.

We also look into our MWCNT electrical-thermal model. Our MWCNT model shows ampacity and conductivity of  $8.2 \cdot 10^8$  A/cm<sup>2</sup> and  $3 \cdot 10^5$  S/cm which are very close to the MWCNT-Cu composite measurement results. This comparison motivates us to further investigate the possible coupling mechanisms between Cu and CNTs which is not considered in our models. In addition, we show our 7 nm technology node Cu interconnect (metal level 2-3) line ampacity and conductivity under high applied voltage (1.8 V) with thermal effects. We find higher ampacity and lower conductivity.

Therefore, we propose more investigations on the Cu and CNTs interface coupling mechanisms, such as thermal exchange and electrical exchange (i.e., doping effect). We also need to look into fundamental atomistic simulations to understand the metal-CNT interface contact thermal diffusions, as well as including surface dependent heat diffusion coefficient to environment. Additionally, for experiments, large amount of CNTs are deposited by Cu seeds for growing Cu materials. In this case, Cu may has different electrical-thermal behaviours to bulk metal properties.

And there would be some portions of the composite are fully filled by Cu without CNTs. Aforementioned reasons could all change the composite electrical-thermal properties.

In this chapter, we showed an exploration of CNT-Cu composite electrical-thermal properties for the potential usage for interconnect applications. This exploration is the first time to establish a systematically macroscopic electrical-thermal model for CNT-Cu composite. There are still lots of physical mechanisms to be understood and integrated to this composite model.

## 4.5 Conclusion

In this chapter, we proposed a systematic study on the electrical-thermal effects of carbon based nanotubes and composite materials for interconnect applications. Based on our previous electrical based models of CNTs, we incorporated thermal effect into electrical performance modeling (i.e., thermal based scattering and self heating) of CNTs and CNT-Cu composite. Temperature profiles along the carbon based interconnect wires, I-V and resistance variations are evaluated. We extracted their ampacity and conductivity from our simulations in order to compare with state-of-the-art literature measurements. The comparison indicates and encourages us to further investigate the coupling effects, doping effects, contact effects and heat diffusion effects in order to have accurate physics based compact models for possible and potential circuit level simulations.

Table 4.1: Width, thickness, and effective Cu resistivity values normalized to the bulk resistivity of  $1.8 \mu\Omega\cdot\text{cm}$  for interconnect layers at the 45-, 22-, 11-, and 7-nm technology nodes based on the Nangate open cell library interconnect stack and assuming a dimensional scaling factor of 0.7X at each new technology generation. [146]

		Width (nm)	Thickness (nm)	$\rho_1$	$\rho_2$	$\rho_3$	$\rho_4$	$\rho_5$
				p = 0, R = 0.43	p = 0, R = 0.43	p = 0.2, R = 0.3	p = 0.25, R = 0.13	
M1	45 nm	70	130	-	2.81	2.3	1.94	1.68
	22 nm	35	65	5.1	4.49	3.44	2.7	2.14
	11 nm	17.4	32.5	12.98	7.75	5.63	4.13	3.01
	7 nm	10.8	20.2	29.47	13.29	9.36	6.58	4.52
M2:M3	45 nm	70	140	-	2.79	2.29	1.93	1.67
	22 nm	35	70	5.05	4.44	3.41	2.67	2.12
	11 nm	17.4	35	12.8	7.67	5.56	4.07	2.96
	7 nm	10.8	21.8	28.97	13.13	9.24	2.35	4.44
M4:M6	45 nm	140	280	-	1.84	1.62	1.46	1.35
	22 nm	70	140	2.67	2.53	2.09	1.77	1.54
	11 nm	35	70	4.73	3.85	2.98	2.35	1.89
	7 nm	21.8	43.6	7.75	5.75	4.26	3.2	2.41



# Chapter 5

## Circuit Level Analysis of Carbon Nanotube Interconnects

### 5.1 Introduction

Along with device scaling and ultra dense integration, interconnects become critical and important for improving overall circuit performance and power dissipation. Conventional copper (Cu) interconnects have reached its physical bottleneck due to high resistivity with surface scattering and grain boundary effect [65, 143]. Scaling limitations and electromigration issues [87, 150] motivate us seeking for new component and materials for future interconnects. Carbon nanotubes (CNTs) based local interconnects become a promising candidate thanks to the ballistic electrical transport [89], high thermal conductivity [14, 98] and high scalability [71]. However, chirality controllability and contact resistance are still considerable issues for CNT interconnects [59, 78]. Hence, doping of CNTs has been investigated as a way to overcome the CNTs variability [109], convert semiconducting shells to metallic behaviour [94] and mitigate contact resistance drawback.

Physical understanding and compact modeling of CNT interconnects provide us a meaningful and practical way to integrate CNT interconnects into circuit level and analyse the overall benchmark performance and energy delay product. Knowing various advantages of CNT interconnects, it is necessary to combine them with highly performed and advanced devices in the circuit benchmark. Carbon nanotube field effect transistor (CNTFET) [58] as one of the promising emerging technologies with additionally carbon based feature can be of interest and potential possibility for future all carbon technology. Moreover, in 2017, more than one million resistive random-access memory (RRAM) cells and more than two million CNTFETs were integrated in a single chip by vertical stacking [137] for energy efficient digital logic circuit [55, 163] and dense data storage [168]. Conventional Cu interconnects are used in [137].

In order to further understand circuit level performance of doped MWCNT interconnects and the potential of all carbon technology, we compare CNT based field effect transistors with standalone MWCNT interconnect (*CNTFET + MWCNT line*) with FinFET and conventional Cu interconnect (*FinFET + Cu line*) as two advanced technology testcases. CNTFET, 7nm FinFET and PTM Cu interconnect

Table 5.1: Experimental contact resistance realized with different contact materials and contact structure

Contact material	Rc (Ohm cm <sup>2</sup> )	Comments	References
Silver	2E-2	SWCNT film side contact	Jackson and Grahama [67]
Pt	1.1E-6	SWCNT film side contact	Koechlin et al. [74]
Pd	3.49E-9	Individual SWCNT side contact	Franklin and Chen [54]
Pd/Au	3.9E-8	CNT line end contact	Chiodarelli et al. [32]
Ti/Au	5E-7	Via end contact (bottom + top)	Chiodarelli et al. [42]
Ti/Al	1.4E-8	Via end contact (bottom + top)	Lee et al. [86]
CNT	1.4E-7	MW/MW side contact	Santini et al. [133]
Carbon EBID*	4.1E-10	Individual MWCNT end contact	Kim et al. [73]
Carbon EBID*	9E-9	Individual MWCNT side contact	Kim et al. [73]

\*Electron beam induced deposition (EBID) of carbon nanotube.

models are used to perform circuit level simulations. Overall circuit delay, power and energy delay product are studied for both testcases.

Furthermore, based on our established CNT electrical compact models, we integrated our model into larger scaled benchmark: Full-adder in order to analyse the overall circuit level performances. Our CNT interconnect models will be compared with conventional Cu model and ideal interconnect models for the usage in the same benchmark. More circuit level analysis will be driven in the last section of this chapter.

Some of the contents in this Chapter will be submitted to:

*Jie Liang*, et al. and A. Todri-Saniai, “Circuit Level Analysis of Pt-Salt Doped Multi-Wall Carbon Nanotubes with Contacts for Local Interconnect Applications”. (to be submitted for IEEE Transactions on Nanotechnology).

## 5.2 Contacts of CNTs Interconnects

Using CNTs for local on-chip interconnects will have to consider contact resistance of CNTs. Contacting CNTs is challenging and varies a lot for different process and applications. Table 5.1 summarize contact resistance for different contact types with various contact metals. From Table 5.1, we notice that, Palladium and Palladium/Gold are the most suitable metals for side- and end- contacts respectively. In this section, we discuss CNT end- and- side contacts and incorporate analytical Palladium end contact resistance into our circuit-level simulations.

### 5.2.1 Different Contacts for MWCNT

The contact between metal and CNTs can be of considerable resistance. When connecting two metals, thanks to the significant electron density of states (DOS) of metals, the interface contact resistance is much smaller than what one can obtain while metal connecting to CNTs. The DOS of pristine CNTs is not comparable with bulk metals due to its 1D quantization. For metal connecting to semiconductor CNTs, the contact resistance is very high due to the large Schottky barrier and no

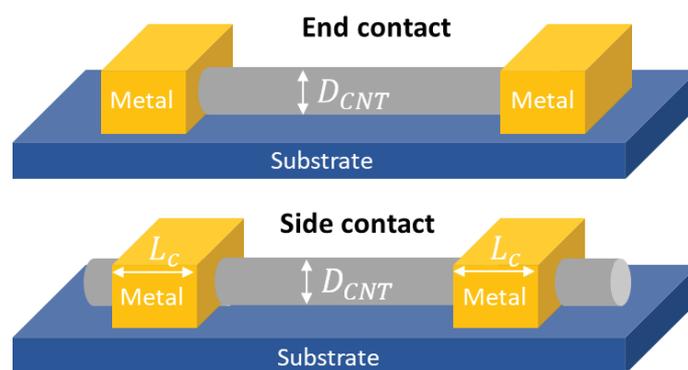


Figure 5.1: Illustration of end and side contact for CNT interconnect.

conducting channels (no DOS at Fermi-level) at the junction interface. For metal to metallic CNT junctions, there is no bandgap for metallic CNTs, but small DOS of CNTs indicates a relatively high contact resistance as well. Therefore, the contact resistance will play a critical role in CNT interconnect performance. In this section, we discuss different types of metal-CNT contacts including end contact and side contact. Fig. 5.1 illustrates a sketch of end- and side- contact.

### Metal-CNT end contact

End contacts are contacts only to the end edges of CNTs. Here, the metal to CNT covalent bonding dominates the contact resistance. In [28], the contact resistance can be reduced by two orders of magnitude for metallic CNT end contacted with TiC instead of Ti. TiC - CNT end contact resistance is shown to be around 6.8 k $\Omega$ . End contact resistance also varies with CNT diameters and contact metal types. End contact resistance decreases with CNT diameter as larger diameter CNT could provide more covalent bondings. In [29], an analytical equation is extracted from DFT (Density Functional Theory) simulations for Palladium end contact. Equation 5.1 shows the relationship between end contact resistance of each shell with contacting shell area  $A_i$ .

$$R_{con_i}^{end} = 1.8514A_i^{-1} + 1.4685 \quad (\text{k}\Omega), \quad A_i = \frac{\pi D_{CNT_i}^2}{4} \quad (5.1)$$

### Metal-CNT side contact

Side contacts are contacting CNT outermost shell with a certain contact length. There is no covalent bonding but van der waals interactions for metal-CNT side contact. In [54], an experimental formula for side contact resistance was derived as below shown in equation 5.2:

$$R_{con}^{side} = \frac{\rho_c^{side}}{\pi L_c D_{CNT}} \quad (5.2)$$

where  $L_c$  is the contact length,  $D_{CNT}$  is the CNT diameter, and  $\rho_c^{side}$  is the resistivity of side-contact which differs from metal resistivity or CNT resistivity. For MWCNT,

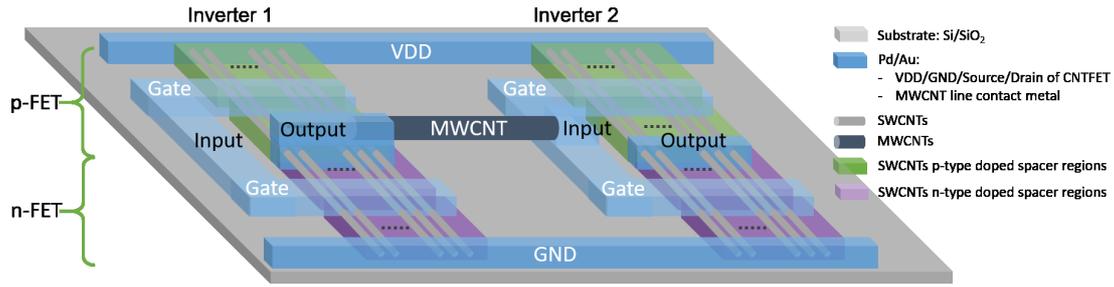


Figure 5.2: Sketch of CNTFET based Inverter - MWCNT Interconnect - Inverter.

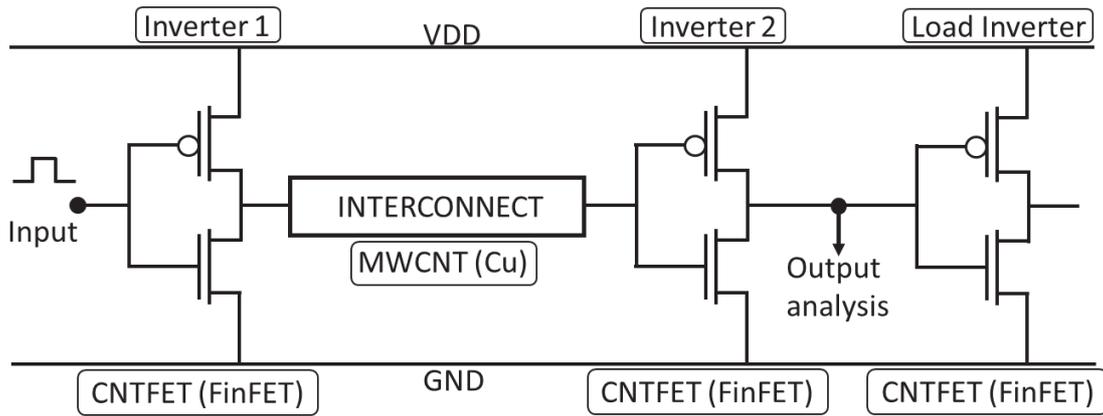


Figure 5.3: Circuit level simulation schematic of Inverter - Interconnect - Inverter for two testcases: *CNTFET device + MWCNT line* and *FinFET device + Cu line*.

$D_{CNT}$  is the outermost shell diameter  $D_{max}$  as there is no side contacts for inner shells. In [54], a Palladium side contact resistance of about 3.3 k $\Omega$  ( $\sim$  6.6 k $\Omega$  for 2Rc) was reported for 100 nm contact length.

### Simulation setup

In our simulations, we first consider end contact resistance between CNTFET and MWCNT interconnect. Equation 5.1 is included in MWCNT interconnect compact model for each shell (Fig. 5.4). We have also chosen several values from 0k $\Omega$  to 5k $\Omega$  for ideal and realistic contact resistances regardless of the contact type and contact metal, as contact resistance is very dependent on process variation. These values can represent different metal-CNT contact scenarios.

## 5.3 CNT Interconnects in Simple Test Benchmark: Inverter to Inverter

In this section, we describe different device and interconnect models employed for circuit level benchmarking and simulations. We investigate a Inverter - Interconnect - Inverter benchmark for circuit level analysis. CNTFET (FinFET) based inverter with MWCNT (Cu) interconnect are used for testcase. Simulation schematic is

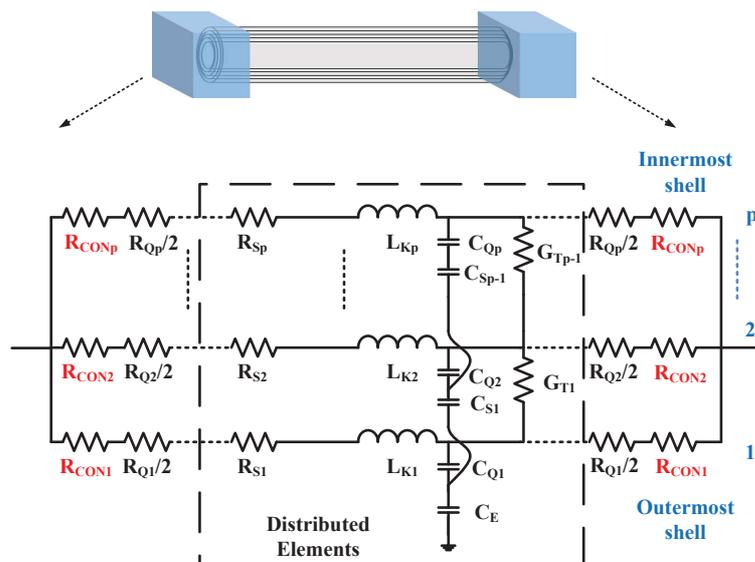
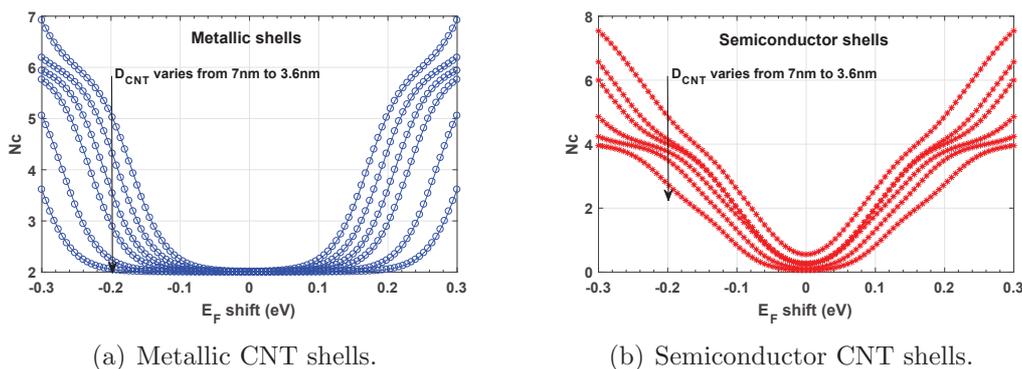


Figure 5.4: MWCNT interconnect electrical compact model [29].



(a) Metallic CNT shells.

(b) Semiconductor CNT shells.

Figure 5.5: (a) and (b) shows the number of conducting channels varies with  $E_f$  shift for metallic and semiconductor shells with respect to different CNT diameters.

shown in Fig. 5.3. We study on two different testcases represent two different technologies as listed below:

- CNT Tech: *CNTFET + MWCNT line*
- CMOS Tech: *FinFET + Cu line*

A sketch of *CNT tech* is shown in Fig. 5.2. MWCNT interconnect is placed between gate level. CNT-metal end contact is considered in this sketch. CNTFET based inverter structure is based on [56] which is advantageous for CNTFET alignment and better chirality selection. This sketch is simply an illustration of our test bench but not a circuit layout design.

### 5.3.1 Testcase I: CNTFET devices with MWCNT interconnect

#### VS-CNTFET Compact Model

We use the VS-CNTFET (Virtual-Source Model for Carbon Nanotube FETs) device models developed by Stanford University [82, 84]. All model parameters are used based on the user manual suggestions (i.e., 11.7 nm and 12,9 nm for gate length and contact length respectively, SWCNT diameter = 1.2 nm, etc). Suggested parameter values are optimized for CNTFET gate delay based on the 2023 node of the ITRS 2013 projections ( $L_{Gatepitch} = 28.1\text{nm}$ ,  $L_{M1} = 25.2\text{nm}$  and  $L_{pitch} = 31.1\text{nm}$ ) [1] for 5-nm technology node. We performed our simulations with different values of gate width (W) and tube to tube spacing (s) in order to analyze overall circuit level energy delay produce (EDP) by varying number of SWCNT tubes in the device.

#### MWCNT Interconnect

We employ the pristine/doped MWCNT distributed model as described in [29] and shown in Fig. 5.4. End contact resistance is calculated for each shell with respect to the equation 5.1. We do not consider defects at the time. MWCNT interconnect doping concentration is represented by CNT Fermi-level shift  $E_f$  based on semiconductor physics. By shifting CNT Fermi-level, electron density of state (DOS) will be increased, thus introducing additional conducting channels and further enhancing CNT interconnect conductivity. The relation between number of conducting channels  $N_C$  and  $E_f$  is shown in Fig. 5.5. Doping of CNT is also a mean of reducing CNT variability [94, 30].

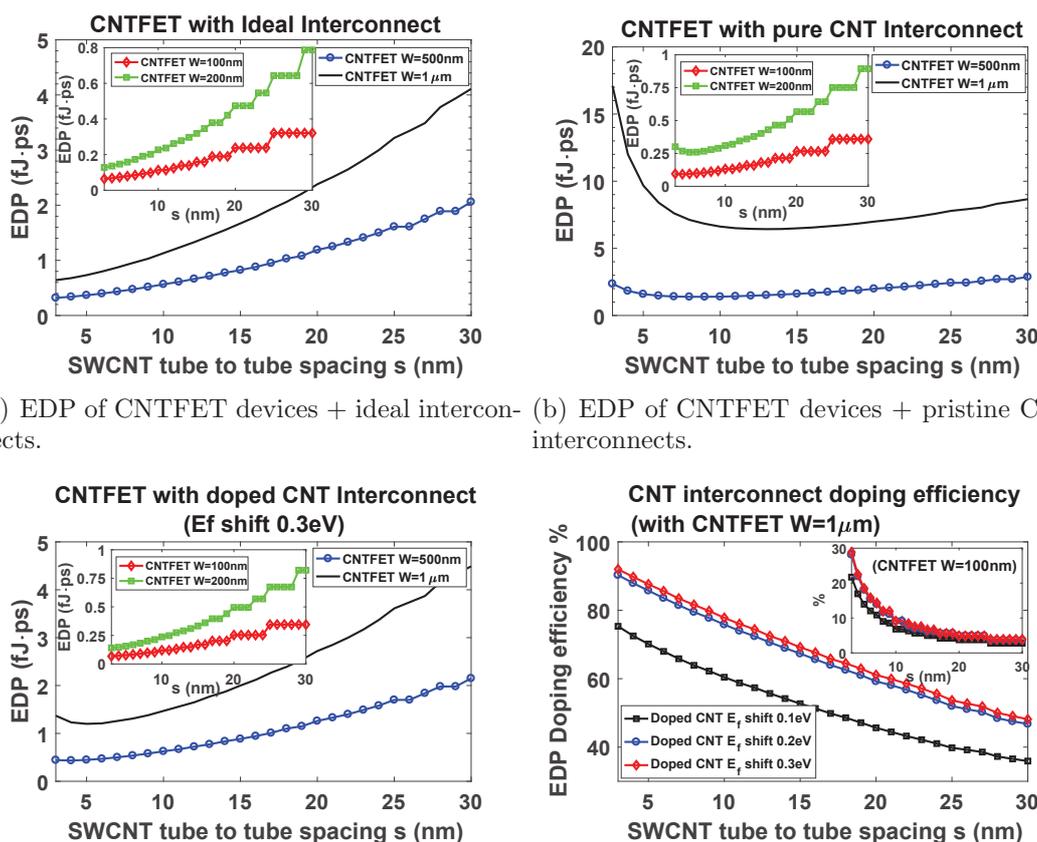
### 5.3.2 Testcase II: FinFET devices with Cu interconnect

#### ASAP 7nm FinFET Model

ASAP7 is a 7-nm FinFET predictive process design kit developed in collaboration between Arizona State University and ARM Ltd. [35, 36, 152, 153, 34]. In our simulations, we apply the original FinFET model as described in ASAP7. We choose FinFET model with TT (regular) mode and vary number of fins. Hspice simulations are performed for FinFET devices connected with Cu interconnect with respect to the benchmark shown in Fig 5.3.

#### Cu Interconnect PTM Model

In this section, we consider Cu metal lines connecting with Cu vias, where no additional metal contact resistance for Cu interconnect. We use Predictive Technology Model (PTM) developed by the Nanoscale Integration and Modeling (NIMO) Group at ASU for copper interconnect [126]. As this model is limited for Cu dimensions, we employed the PTM model with resistance and capacitance analytical formula and thus introduced a resistivity value fitting from [91] (Table. 1). Fitting resistivity is  $11.4 \mu\Omega\text{-cm}$  for 7 nm line width of Cu.



(a) EDP of CNTFET devices + ideal interconnects. (b) EDP of CNTFET devices + pristine CNT interconnects.

(c) EDP of CNTFET devices + doped CNT interconnects. (d) EDP improvement with doped CNT interconnects with various doping concentration + CNTFET devices  $W=1\mu\text{m}$  (and  $W=100\text{nm}$  for inset figure).

Figure 5.6: (a)-(d) are simulation results relating to Testcase A: CNT based technology. (a) represents energy delay product (EDP) as varying CNTFET width ( $W$ ) and tube to tube spacing ( $s$ ) with ideal interconnects. (b) shows the circuit level EDP variation when including pristine MWCNT interconnect between CNTFET based Inverter 1 and Inverter 2. (c) shows the overall EDP variation with doped MWCNT interconnects ( $E_f$  shifts 0.3 eV) under different  $W$  and  $s$ . (d) illustrates the overall circuit EDP improvement by introducing different doping to the MWCNT interconnects.

### 5.3.3 Variability Evaluations of CNTs in test benchmarks

#### Carbon based technology

In order to have meaningful understanding of MWCNT interconnect impacts on the circuit level, it is necessary to optimize firstly CNTFET device. We investigate in terms of energy delay product (EDP) of CNTFET devices with ideal and different types of CNT interconnects. We vary CNTFET gate width ( $W$ ) and tube-to-tube spacing ( $s$ ) by keeping the rest of parameters unchanged as provided by the model.

In Fig. 5.6 (a), we consider ideal interconnects where no additional parasitics

from interconnect. We notice that CNTFET EDP is increasing with  $s$  and decreasing with CNTFET gate width. This can be understood as larger  $s$  (less tubes (channels)) will improve the device power consumption by reducing driven current, but less ballistic transport channels are worsening the delay. And we also learn that variations of CNTFET  $W$  and  $s$  have more impacts on circuit level delay than power consumption.

In Fig. 5.6 (b), 7 nm diameter of pristine MWCNT interconnects are included between CNTFET inverter 1 and 2 (see Fig. 5.3 and 5.2 (a)). We vary CNTFET  $W$  and  $s$ . End contact resistance is included in the MWCNT interconnect compact model. Comparing to (a) with ideal interconnect, circuit level EDP for  $W = 1 \mu\text{m}$  has more than one order of magnitude increased due to interconnect with small  $s$  and about 2X increase for large  $s$ . For  $W = 500 \text{ nm}$ , there are 10X and 1.25X EDP increased for small and large  $s$  respectively. And we observed very few EDP increase for  $W = 100$  and  $200 \text{ nm}$ . Additionally, we notice that for  $s = 13 \text{ nm}$ , there is a minimum EDP on overall circuit level for CNTFET  $W = 1 \mu\text{m}$  with pristine MWCNT interconnect. Important notice from (a) and (b) is the critical impact of local interconnect on the overall circuit level energy efficiency, especially for CNTFET with larger  $W$  and smaller  $s$ , where interconnects have comparable impacts as CNTFET devices on overall circuit level.

In Fig. 5.6 (c), we introduce heavily doping ( $E_f$  shift = 0.3 eV) into MWCNT interconnect. With doped MWCNT interconnect, we can see that overall circuit level EDP is very close to that with ideal interconnect in (a). In this case, interconnects performances are very much improved and devices become again dominant for the overall circuit level energy efficiency. In Fig. 5.6 (d), we present the circuit level EDP improvement with different doping concentration on MWCNT interconnect. Doping has much more impacts for large CNTFET ( $W=1\mu\text{m}$ ) than that of small CNTFET ( $W = 100 \text{ nm}$ ). Comparing with pristine CNT interconnect, overall EDP can be improved by more than 90% and 75% with lightly ( $E_f$  shifts 0.1 eV) and heavily ( $E_f$  shifts 0.3 eV) doping for circuit benchmark with large width ( $W=1\mu\text{m}$ ) CNTFET with small tube spacing (large amount of SWCNT channels). For CNTFET width of 100nm with small tube spacing, 30% overall EDP can still be obtained with heavily doping. Moreover, less than 4% EDP is improved when few SWCNT channels existing in CNTFET (small  $W$  and large  $s$ ). Furthermore, we notice that doping with  $E_f$  shift of 0.2 eV and 0.3 eV has no much difference on overall EDP improvement. Hence, there is not necessary to have very heavily doping when the doping process is still challenging.

### Advanced CMOS technology

We perform simulations to analyse advanced CMOS technology: *FinFET + Cu interconnect* in terms of delay, average power and energy delay product (EDP). We have varied the number of fins for 3, 5 and 10. For each fin number, we introduce ideal interconnect and various Cu interconnects with different aspect ratio (A/R) of 3, 5 and 10. Detailed values are summarised in Table 5.2.

For FinFET devices connecting with ideal interconnects, power consumption increases with number of fins as more fins induce higher output capacitance  $C_{out}$ , hence more power consumption. Constant delay is due to the proportionally increase

Table 5.2: 0.9T *Testcase I*: FinFET + Cu interconnects

Cu Aspect Ratio (A/R)	3 Fins			5 Fins			10 Fins		
	Delay (ps)	Power (uW)	EDP (fJ·ps)	Delay (ps)	Power (uW)	EDP (fJ·ps)	Delay (ps)	Power (uW)	EDP (fJ·ps)
Ideal Interconnect	12.08	0.50	0.08	12.08	0.84	0.12	12.08	1.68	0.25
A/R = 3	27.49	1.66	1.25	22.36	1.98	0.99	17.73	2.85	0.90
A/R = 5	22.35	1.16	0.58	18.77	1.47	0.52	15.22	2.31	0.53
A/R = 10	15.95	0.78	0.20	15.11	1.12	0.26	13.50	1.95	0.36

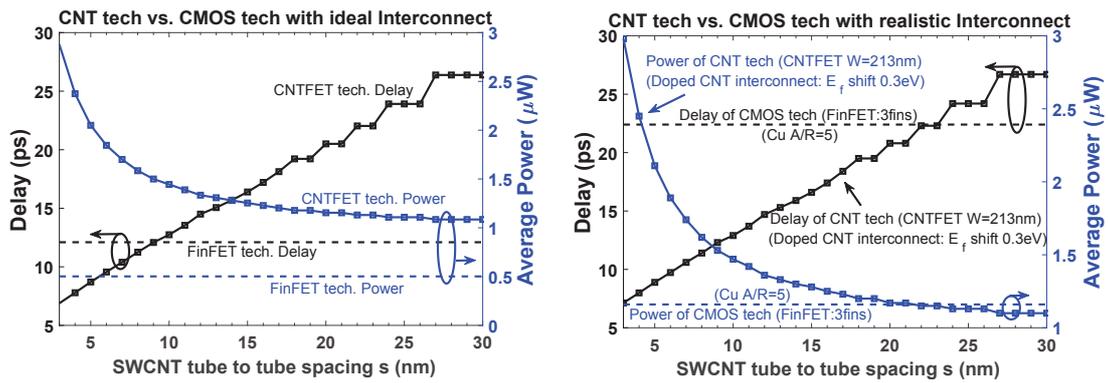
in output capacitance and driving current  $I$  (delay  $\sim C_{out} \cdot V_{dd}/I$ ). Hence, EDP is increased as well with number of fins. We then employ realistic Cu interconnects with varied Cu aspect ratio into *FinFET + Cu line* testcase with respect to the circuit benchmark shown in Fig. 5.3. By increasing number of fins, we observed an overall trend of increase in power and EDP, and decrease in delay. With the increase of the Cu interconnect aspect ratio, the overall circuit level delay, power and EDP are improved. And this shows again the importance of local interconnects for advanced CMOS technology. However, considering reliability of advanced technology node, high Cu interconnect aspect ratio remains big challenge. Results shown in table 5.2 are used for further comparison with carbon based technology (*CNTFET + MWCNT line*).

### Carbon based vs. Advanced CMOS technologies

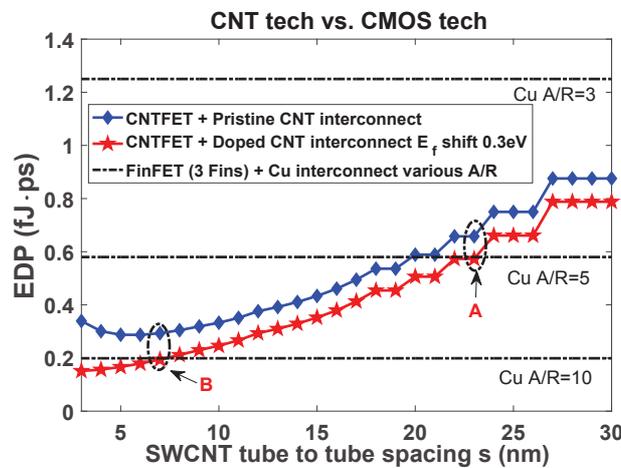
Figure 5.7 shows comparisons between CNT technology and advanced CMOS technology. In order to have fair comparison, we optimized the CNTFET gate width ( $W$ ) to 213 nm, as we would like to compare with tri-gate 3fins FinFET where effective channel width  $3W_{eff} = 3 \times (2H_{fin} + T_{fin}) = 213\text{nm}$ [35].

In Fig. 5.7 (a), we compare CNT technology with CMOS technology with ideal interconnects in terms of delay and power consumption. We can see that the FinFET benchmark circuit always has better power consumption, and CNTFET testcase can have better performance when CNTFET is inferior to 9 nm (including  $\sim 25$  SWCNTs in the CNTFET). In Fig. 5.7 (b), we introduce heavily doped MWCNT interconnect with  $E_f$  shift = 0.3 eV. In this case, we compare to 3 fins FinFET with Cu interconnect of aspect ratio 5. It is noticed that the CNT based testcase (*CNTFET + MWCNT line*) can have better overall circuit performance than advanced CMOS testcase (*FinFET + Cu line*) when CNTFET is smaller than 23 nm ( $\sim 9$  SWCNTs inside CNTFET), and power consumption gets better than CMOS testcase when  $s$  is greater than 23 nm. It is interesting to find that a trade-off point for delay and power in CNT based testcase when CNTFET has  $s \sim 9$  nm connecting with heavily doped MWCNT interconnect. This observation is also shown in Fig. 5.7 (c) that the circuit level EDP comparison of two testcases. We can also find that for CNTFET is inferior to 7 nm, with heavily doped MWCNT interconnect, *CNTFET + MWCNT line* is having better EDP than *FinFET + Cu line* with Cu interconnect aspect ratio is 10. Therefore, two interesting trade-off areas A ( $s = 23$  nm) and B ( $s = 7$  nm) are observed and shown in (c).

In Fig. 5.8 (a) and (b), we further analyse the impact of CNT-metal contact resistance and doping concentration on the trade-off area A and B (see Fig. 5.7 (c)). In this case, we varied contact resistance from 0 to 5 k $\Omega$  and Fermi-level shift from 0 (pristine) to 0.3 eV (heavily doped). In Fig. 5.8 (a), which corresponds to trade-off area A, EDP ratio can remain inferior to 1 for contact resistance of 3 k $\Omega$  with heavily doped ( $E_f$  shifts 0.3 eV) MWCNT interconnect. In Fig. 5.8 (b) - trade-off area B, comparing to the best case of advanced CMOS test (FinFET + Cu line A/R = 10), carbon based testcase overall circuit level EDP can still remain comparable when having heavily doped MWCNT interconnect with contact resistance less than 2.8 k $\Omega$ . From these two cases, we can learn that doping of CNT interconnect can also further mitigate contact resistance drawback, however, high contact resistance



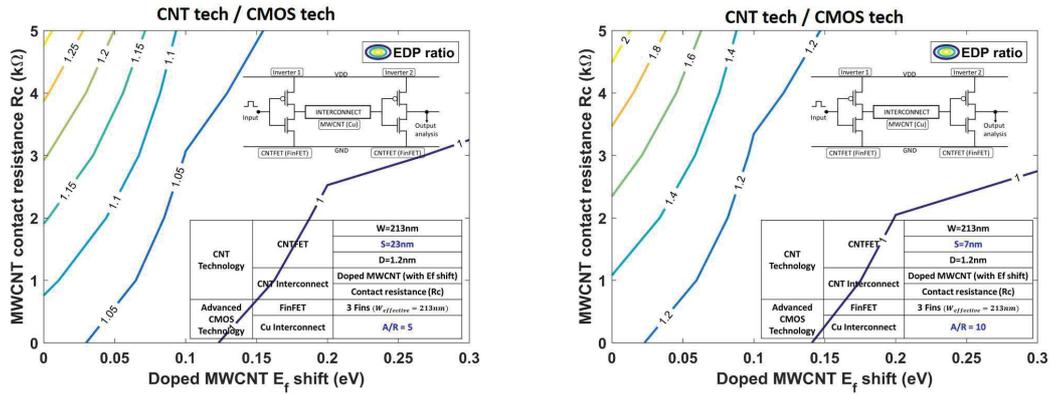
(a) Delay and Power comparison for CNT tech and CMOS tech with ideal interconnects. (b) Delay and Power comparison for CNT tech and CMOS tech with realistic interconnects.



(c) EDP comparison between CNT tech and CMOS tech with different interconnect configurations.

Figure 5.7: (a)-(c) are simulation analysis to compare carbon based technology and advanced CMOS technology. (a) and (b) represent overall circuit level delay, power consumption for devices (CNTFET and FinFET) with ideal and realistic (doped MWCNT and Cu) interconnects respectively. (c) shows the circuit level energy delay product (EDP) for CNT tech and CMOS tech with different interconnect configurations. Pristine and heavily doped MWCNT interconnects are included for CNTFET devices; and for FinFET devices, Cu interconnects with various aspect ratio ( $A/R$ ) are considered for comparison.

is still the critical factor for CNT local interconnects.



(a) EDP ratio of CNT tech vs. CMOS tech with different CNT-metal contact resistance and doping concentration for area A. (b) EDP ratio of CNT tech vs. CMOS tech with different CNT-metal contact resistance and doping concentration for area B.

Figure 5.8: Energy delay product ratio between CNT tech and CMOS tech for specified area A and B (in Fig. 5.7 (c)). (a) and (b) corresponds to area A and B respectively. MWCNT interconnect contact resistance and doping level are varied based on different given parameters (inset tables).

## 5.4 CNT Interconnects in Larger Test Benchmark: Full-adder

In order to compare the impact of CNT interconnect in the local level, ideal, copper or MWCTN/SWCNT interconnect is placed at the output node of each gate, making the circuit connection equivalent to the Fig. 5.9. Thus, three versions of CNFET standard library are available, i.e. with ideal interconnect, copper interconnect or MWCTN/SWCNT interconnect. Furthermore, to make fair and meaningful comparisons between copper and CNT interconnect, the placement of interconnect, geometrical parameters and equations of calculating the parasitic capacitance for them should be carefully considered as shown schematically in Fig. 5.10. In addition, due to the increase in resistivity of copper interconnect at high scaled technology nodes, the predicted resistivity should be calculated as well, which is shown in Fig. 5.11. The resistance calculation for CNT interconnect is based on the compact model proposed previously.

### 5.4.1 Full-adder characterization

To evaluate the impact of technology node scaling on the integrated circuits with copper and CNT interconnects at the local level, a full-adder is used as a typical circuit. Pristine MWCNT without defects and doping is used for CNT interconnect. The characterization results are presented in Fig. 5.12. The results show that without any improvement or optimization of MWCNT interconnect, such as doping techniques and contact resistance reduction, the CNT interconnect performance is overall worse than that of the copper interconnect at the perspective of circuit level.

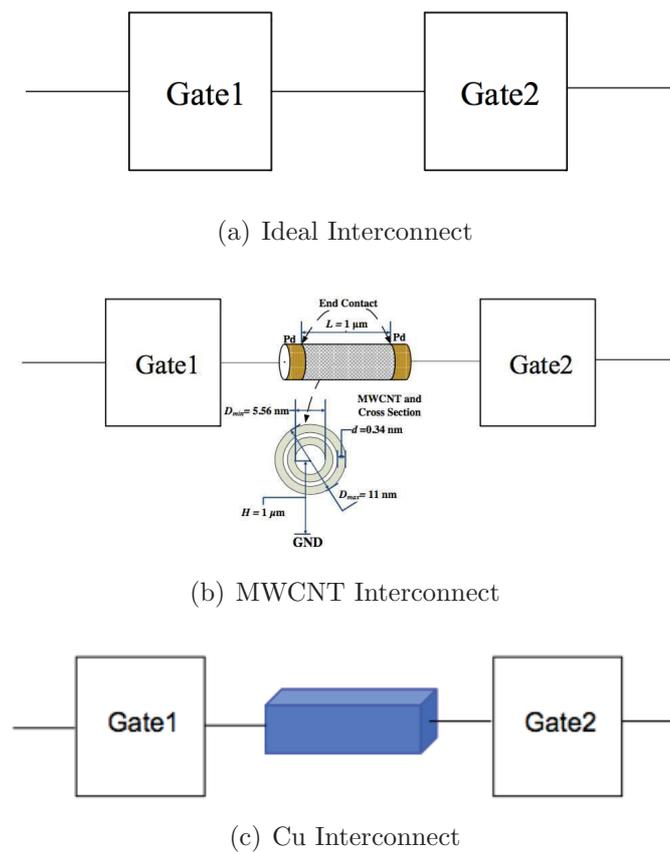


Figure 5.9: Schematic of circuit gates connection of various interconnect scenarios including the MWCNT interconnect case (a), ideal interconnect case (b) and the copper interconnect case (c).

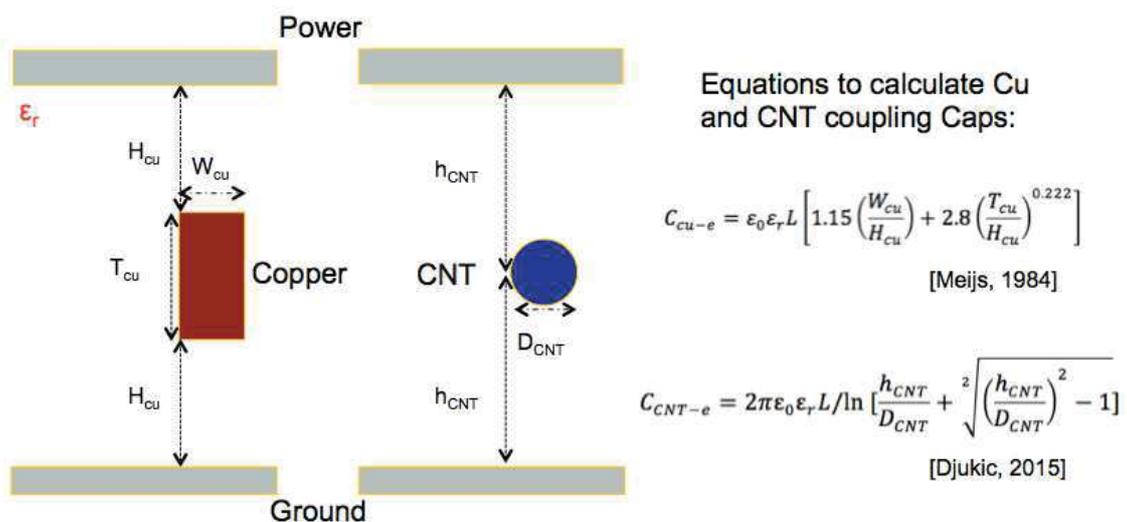


Figure 5.10: Corresponding Copper and CNT interconnect placement.

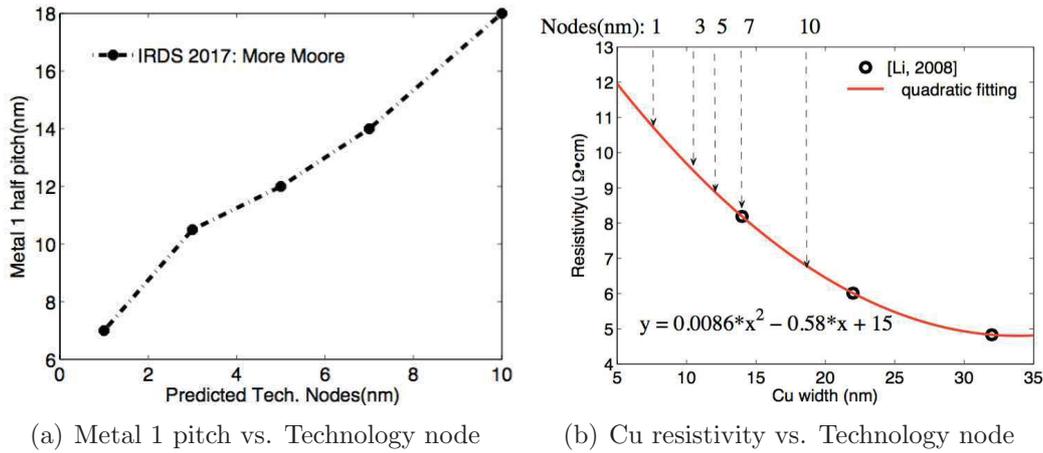


Figure 5.11: (a) Metal 1 pitch for different technology nodes from IRDS 2017. (B) Prediction of resistivity of copper interconnect under different technology nodes according the IRDS 2017 and that from [2].

But the disadvantage is disappearing when the technology nodes is highly scaled such as that of 1 nm node. Thus, if the MWCNT is improved by doping and contact resistance reduction, it can be expected that it will be of some advantages to some extent. Fig. 5.13 shows the impact of doping by the means of Fermi level shift on the performance of CNT interconnect (@ 5 nm node) at the full-adder circuit level. It clearly shows that doping can enable the CNT interconnect to become better when the doping level induced Fermi level shift is up to 0.2 eV, which however is also technology node dependent. Also shown in Fig. 5.13 is the doping impact on MWCNT interconnect with chirality of 1/3 which is an average value for large number of CNTs after growth, i.e. statistical result. By doping technique, the performance of the 1/3 chirality MWCNT can be significantly improved as the full-adder overall characterization results show. This is because of the degeneration of semiconducting CNT shells to metallic CNT shells after doping.

Defects can induce additional delay (similar for power) for the full-adder significantly, as shown in Fig. 5.14. Despite of the significant improvement for the 1/3 chirality MWCNT interconnect by the doping technique, for metallic MWCNT interconnect, the defect will dominate the impact of CNT interconnect on the circuit performance at various doping levels.

## 5.5 Discussion

In this chapter, we performed circuit level simulations by integrating standalone doped MWCNT into gate level. Carbon based technology (*CNTFET + MWCNT line*) and advanced CMOS technology (*FinFET + Cu line*) have been used as test benchmarks. From our simulation result of 1  $\mu\text{m}$  CNTFET width, important impacts of interconnects on overall circuit level performance have been shown up to one order of magnitude higher EDP after including pristine MWCNT interconnects with CNTFET. By scaling down CNTFET width to 100 - 200 nm, this correspond-

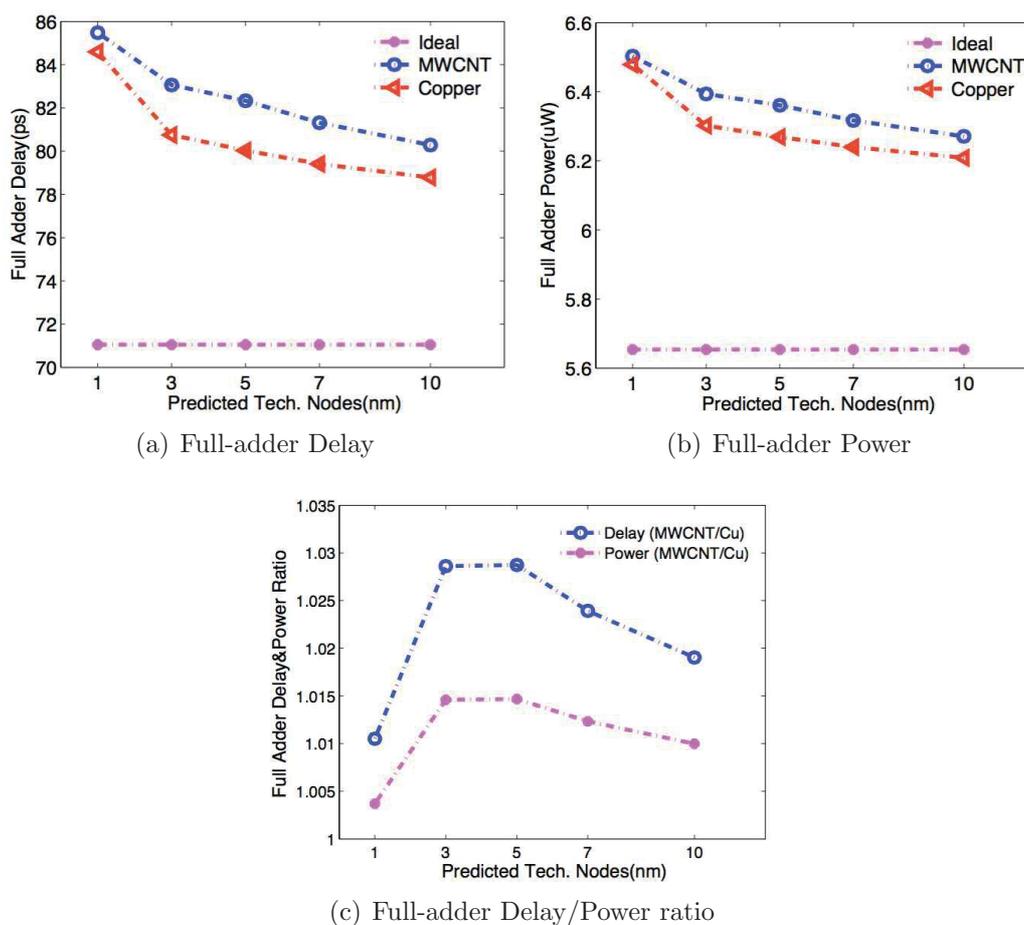


Figure 5.12: Delay (a) and power (b) characterization results of a full-adder at different technology nodes. The ratio of these two interconnects and its with technology nodes is also shown in (c).

ing increase of overall circuit level EDP is reduced to very few, as the device load capacitance and power dissipation are much decreased.

With lightly and heavily doped MWCNT interconnects and CNTFET devices, the overall EDP can be improved by up to 75% and 90% with CNTFET  $W = 1 \mu\text{m}$ . After CNTFET device scales down to 100 nm width, improvement on overall EDP can still be up to 30%. This is because as the number of SWCNTs inside the device is reduced by one order of magnitude, the device has already performance improvement, and hence doping on interconnects gets less efficient on the overall circuit level performance improvement.

Cu interconnects also have significant impacts on the overall circuit level performance regarding the test bench *FinFET + Cu line*. More than 15X higher EDP is observed comparing with ideal interconnects for 3 fins and Cu aspect ratio of 3. With increase of number of fins on FinFET, the overall delay, power and EDP get improved. And Cu interconnects can improve the circuit level delay, power and EDP by increasing the aspect ratio. However, for advanced 7 nm FinFET technology with

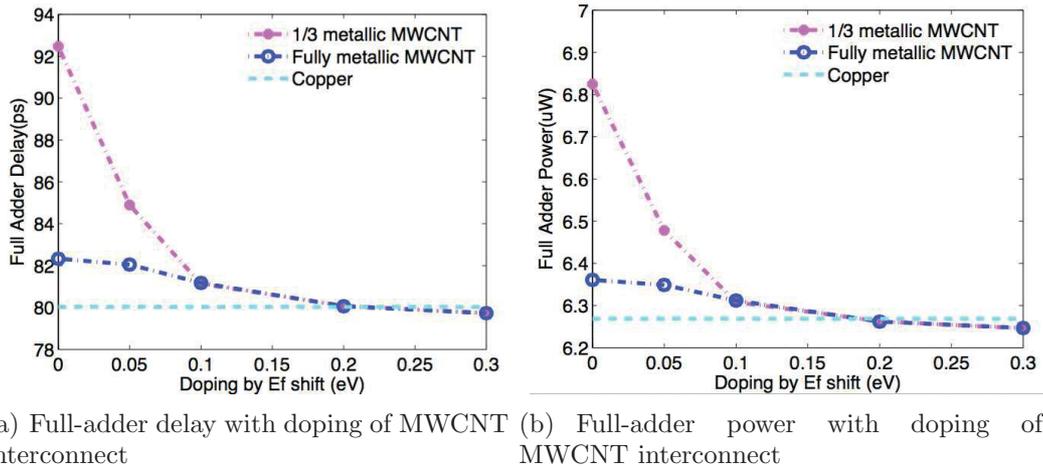


Figure 5.13: Impact of doping on MWCNT interconnect performance at the full-adder circuit level. Both total metallic CNT and CNT of 1/3 metallic chirality are concerned and compared with copper interconnect. The study case is at the 5 nm technology node.

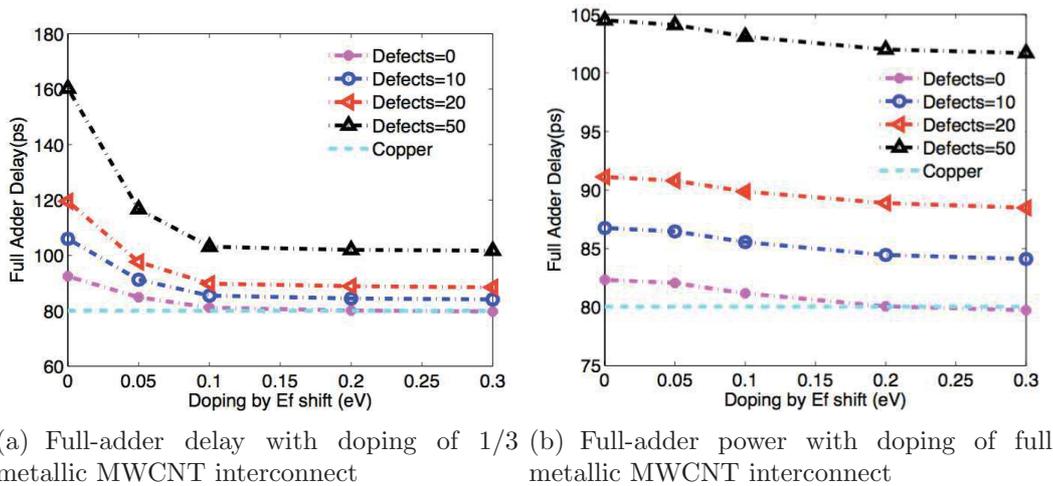


Figure 5.14: Impact of CNT interconnect defects on the full-adder performance (delay) under different Fermi levels or doping. Both 1/3 chirality MWCNT (a) and fully metallic MWCNT are shown (b). Power results are similar changed and thus not shown here..

Cu interconnects, we can not only scale the device but also the interconnects and high Cu interconnect aspect ratio relies on the process reliability. Therefore, with conventional interconnects, performance, reliability and physical scaling limitation remain critical issues and challenges.

Comparing the two advanced technologies, *FinFET + Cu line* can have less power consumption, and *CNTFET + MWCNT line* has better performance and energy efficiency for certain CNTFET tube spacing ( $s$ ) choices. By doping of MWCNT

interconnects, we have found two interesting trade-off areas for  $s \sim 23$  nm and  $\sim 7$  nm, where *CNTFET + doped MWCNT line* can have comparable or better energy efficiency than *FinFET + Cu line* with Cu A/R is 5 and 10. We also notice that doping of MWCNT interconnect can mitigate local interconnect contact resistance drawbacks. However, high contact resistance remains critical problem to be solved in the further research.

## 5.6 Conclusion

In this chapter, we investigate standalone doped MWCNT interconnect into circuit level. We analyse gate-level performances of two advanced technologies (CNTFET and FinFET) with its accompanied interconnects (MWCNT and Cu). Circuit-level analysis for both *CNTFET + MWCNT line* and *FinFET + Cu line* indicate the importance of improving interconnect performance. Doping of MWCNT shows a good potential to be one of the promising solutions with respect to improve the overall circuit scalability while remaining high performance and energy efficiency. Two cross areas are observed of circuit level EDP between these two technologies by employing doped MWCNT interconnect and selecting proper CNT interconnect contact resistance. This also illustrates a potential possibility of an all carbon-based circuit for future generation of ultra-large scale integrated (ULSI) circuit.



# Chapter 6

## Conclusion and Perspective

In this thesis, we have explored the potential of carbon nanotube and carbon nanotube - copper composite for next generation energy efficient interconnects. Based on the state-of-the-art interconnects development, we aimed to contribute in terms of electrical / physical compact models for carbon nanotube based interconnect models. We have studied in different kinds of carbon nanotube interconnects, namely pristine SWCNT and MWCNT, doped SWCNT and MWCNT, SWCNT-Cu composite and MWCNT-Cu composite. We provided a physics based systematic research on this topic with additional experimental validations.

In the following of this chapter, we conclude each of the chapter by summarizing the main contributions and giving takeaway key messages on each research item. We finish by highlighting possible research steps to complete this thesis and give future research perspectives.

### 6.1 Conclusion

In the following, we conclude each of the chapter in this thesis.

- Chapter 2: Pristine Carbon Nanotubes

In this chapter, an enhanced compact model of MWCNT interconnect is presented where diameter dependent contact resistance and defect-induced resistance for each MWCNT shell are included. Based on the proposed enhanced compact model, MWCNT interconnect resistance and performance variations (including delay, power, and PDP) are analyzed including variations on diameter, defect densities, chirality, and shell-to-contact connectivity. We identify that the diameter, defects, chirality, and all-sources variations all produce Lognormal resistance and performance distributions. We find that defect variation is increased with defect density at a larger rate than diameter variation and surpasses diameter variation at defect density of  $\sim 15 / \mu\text{m}$ . The chirality variation is always the most dominant source of variation even at large defect densities. We also consider the case of significantly reduced MWCNT diameter and defect variations due to improving the quality of MWCNT growth, where the chirality remains as the only source of variation.

- Chapter 3: Doping of Carbon Nanotubes

In this chapter, we investigate Pt-salt doped CNT for BEOL interconnects. By combining atomistic to circuit-level simulation and measurement results, we explain the impact of doping on enhancing MWCNT metallic properties. Both experimental data and simulations show that the  $\text{PtCl}_4$  represents an efficient doping strategy to reduce MWCNT resistivity through conversion of semiconducting shells to metallic. Doping can also be a likely solution to overcome the detrimental impacts of defects and contact resistances for a realistic interconnect system. This represents a milestone result, which could enable the success of MWCNTs as a candidate for future back-end-of-line technology nodes interconnects. Overall, we have established the analytical methods and simulation framework to study charge based doping impact on MWCNT interconnects performance and variability.

- Chapter 4: Copper-Carbon Nanotube Composite

In this chapter, we proposed a systematic study on the electro-thermal effects of carbon based nanotubes and composite materials for interconnect applications. Based on our previous electrical based models of CNTs, we integrated thermal effects (i.e., thermal based scattering and self heating). Temperature profiles along the carbon based interconnect wires, I-V and resistance variations are evaluated. We extracted their ampacity and conductivity from our models in order to compare with state-of-the-art literature measurements. The comparison indicates and encourages us to further investigate the coupling effects, doping effects and contact effects in order to have compact physical models for possible and potential circuit level simulations.

- Chapter 5: Circuit Level Analysis of Carbon Nanotube

In this chapter, we integrate standalone doped MWCNT interconnect into circuit level. We analyse gate-level performances of two advanced technologies (CNTFET and FinFET) with its accompanied interconnects (MWCNT and Cu). Circuit level analysis for both *CNTFET + MWCNT line* and *FinFET + Cu line* indicate the importance of improving interconnect performance when we look for a highly integrated and performing circuit. Doping of MWCNT shows a good potential to be one of the promising solutions with respect to improve the overall circuit scalability while remaining high performance and energy efficiency. Two cross areas are observed of circuit level EDP between these two technologies by employing doped MWCNT interconnect and selecting proper CNT interconnect contact resistance. This also illustrates a potential possibility of an all carbon-based circuit for future generation ultra-large scale integrated (ULSI) circuit.

In addition, we have performed circuit level simulations by employing larger scaled benchmark: Full-adder for different interconnects usage. Performance, power consumption and energy efficiency are analysis for ideal, Cu interconnects and MWCNT interconnects for advanced technology node.

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## 6.2 Research Perspectives

### 6.2.1 To complete this thesis

In this thesis, we have achieved to build compact models for pristine and doped carbon nanotubes for on-chip local interconnects by taking into the account different variability sources (i.e., diameter, defects, chirality, shell connections to contact) and how doping impacts the CNT performance and power consumptions. We have investigated in depth the doping of CNTs from fundamental physics to macroscopic compact modeling. Our models have been compared with experimental data and showed its accuracy. Furthermore, we have studied the electro-thermal effects of CNT and CNT based composite as potential candidates for intermediate and global interconnects. In this study, we have considered the thermal effect on composite materials by introduce thermal scattering, self heating and heat diffusion to the substrate. However, in order to be robust and compact to accurate circuit design and simulations, it is needed to investigate in depth the thermal coupling between CNT and Cu in composite material. More investigations should be done on possible thermal exchanges at the interface of CNT and Cu, charge transfer doping effect between Cu and CNT, contacts thermal impacts and heat diffusion coefficient of composite material to the environment.

### 6.2.2 Perspectives relating to Carbon Nanotube

#### All carbon based processor

Based on this thesis, we have shown carbon nanotube as viable solutions for future interconnect applications from theoretical compact modeling. Some of the experimental measurements also demonstrated the potential of doping of CNTs to mitigate the variability impacts and enhance its electrical properties. However, relating to the topic of future energy efficient interconnects, there are still more research needed. Most of the industries prefer to keep the Damascus integration process by finding new metal conductors with optimized liner and dielectric layers. This is due to the big challenges of developing a totally innovative integration process for an all carbon based technology. Even though the carbon based transistors are well studied during the past decades, but integration of carbon nanotubes for all interconnects is still to be developed and remain a lot of experimental investigations.

#### Carbon nanotube for memory applications

As introduced in the introduction part of this thesis, carbon nanotubes have been used for non-volatile random access memory (NRAM) thanks to its mechanical properties. Carbon nanotubes were often used for memory devices level. However, for nowadays memory requirements, fast, stable, energy efficient and area minimizations are highly demanding. A lot of research are focusing on new devices for memories, such as spin torque transfer magnetic RAM (STT-MRAM), phase change memory (PCM), resistive switching RAM (RRAM) and conductive bridge RAM (CBRAM). Based on this thesis, we have found carbon nanotubes having very good electrical

performances and energy efficient, as well as with tunable dimensions. Combining carbon nanotubes interconnects with emerging memory devices would be an interesting research topic.

### **Carbon nanotube for biosensing applications**

During this thesis, we came to know the imperfectness of grown CNTs. Even though with high temperature CVD growth or arc-discharge growth, we can have high quality CNTs. But looking into the defects on CNTs, instead of removing them, we can use the defects for biosensing applications. For most of the chemistry and biology researches, functionalisation of materials are necessary and important. Existence of defects in CNTs can be a good nature of being easily functionalized by different chemical or biological elements. The functionalized CNTs can be used as mobile probe for sensing target.

Beside of using as mobile probe for sensing, CNT based transistors can also be used for field effect sensing. Semiconducting CNT channels in a transistor can be tuned their energy bandgap by different virtual applied gates. Instead of an bulk metal gate, we can use chemical or biological liquids as tunable gates. Different molecular concentration in the liquid gate will directly impact the CNT electrical properties and then change the transistor device behaviour.

### **Carbon nanotube for thermal interface**

Based on the good thermal conductivity of carbon nanotubes, carbon based film or forest can be used for thermal interface and integrated in possible thermal related devices. Carbon nanotube forest or carbon nanotube bundles with metal composite can be of interest for thermal conduction and heat dissipation elements.

## **6.2.3 Perspectives relating to Energy Efficiency**

### **Photonic interconnects**

Photonic interconnects as one of the high performance and energy efficient technology has been used often for off-chip interconnects due to the emitter and receiver size and cost limitations. However, on-chip photonics started to be widely investigated while the conventional on-chip interconnects reach their physical limitations. Besides finding new materials for novel interconnects, photonics on-chip also drives a lot of attention for future interconnects applications research. There are lots of interesting topics require further investigations and development. Such as different laser sources with a silicon-based substrate, laser source compatible modulator developments, energy efficient waveguide, and photo-detectors. Developing silicon integration compatible photonic devices become a trend in the optoelectronics field. Integration of a large number of photonic interconnects needs more investigations and cost optimizations. New circuit design needs also to be also investigated to adopt a novel on-chip photonic interconnects environment.

## Emerging energy efficient devices

In the past five decades, semiconductor industry has experienced from the geometry based scaling (i.e., conventional MOSFET scaling) to effective performance scaling with new device structures (i.e., FinFET, CNTFET, and nanowire-based transistors). Based on the continuous scaling and energy efficiency request, different hyper-performance electronic devices have attracted lots of interest. Various researches have been driven for future sub-Boltzmann or beyond-Boltzmann field effect transistors. Such as negative-capacitance ferroelectric field effect transistor (FeFET) can reduce the subthreshold swing without modifying their transport physics, negative-capacitance field-effect transistor (NCFET) can amplify the applied gate voltage electrostatically, and phase transition FET (PFET) exploits the negative differential resistance induced across the correlated material as the abrupt phase transition takes place. This phase transformation amplifies the free-carrier concentration and rises its conductivity. Looking into the beyond-Boltzmann limits transistors indicates a new era of future on-chip electronics with much higher performance and energy efficiency.

## Neuromorphic computing

Neuromorphic computing describes using a VLSI electronic analog circuits to mimic neuro-biological architectures present in the nervous system. Neuromorphic computing is a non Von Neumann architectures. In neuromorphic computing, novel algorithm in software, new circuit architecture design, and novel devices developments are of huge interest. As a mimic of neuro-biological nervous system, it is expected to be hyper-performance and energy efficient. Neuromorphic computing opens a room where lots of inter-disciplinary research need to be studied and developed.

## Quantum computing

Another non Von Neumann architecture computing is quantum computing. Quantum computing uses Qubits with its superposition and entanglement of different quantum states for its computations. Qubits are fundamental to quantum computing and can be analogous to bits in a classical computer. Qubits can be in a 1 or 0 quantum state. But they can also be in a superposition of the 1 and 0 states. Quantum computing can be potentially used for quantum cryptography, quantum simulations, quantum annealing and adiabatic optimizations, solving complex biological equations, and solve problems that classical computing can not practically achieve (also known as quantum supremacy). However, for quantum computing, there is still a big challenge of noise and error corrections, implementation in mobile devices, and operation in room temperature or beyond.



# Appendix

## Verilog-A SW CNT compact models

- CNRS - Carbon Nanotube Interconnect RC Model

### *Description*

Our carbon nanotube interconnect compact model is developed with fundamental physics understanding and electrical modeling. Single Wall Carbon Nanotube (SWCNT) RC electrical model takes into the account the quantum resistance and capacitance, as well as electrostatic capacitance. A doped SWCNT interconnect model by introducing a doping enhancement factor  $N_c$  has also included in this model. SWCNT dimension (L and D) and contacting resistance  $R_c$  can be varied in our models.

We have published our models with detailed Verilog-A codes on *NanoHUB*. If you are interested in looking more in detail or would like to download our model for your usage, please visit <https://nanohub.org/publications/200/1>.

## Verilog-A MW CNT compact models

- Multi-walled/Single-walled Carbon Nanotube (MWCNT/SWCNT) Interconnect Lumped Compact Model Considering Defects, Contact resistance and Doping impact

### *Description*

Currently, CNT is considered as one of the primary candidates to outperform Cu concerning performance and reliability as future back-end-of-line (BEOL) interconnect material due to its properties such as ballistic transport, high thermal conductivity, ampacity and strong sp<sup>2</sup> bonding between carbon atoms.

Good contacts between CNT and metal electrodes are very challenging. Poor contacts generate significant contact resistance, which severely degrades the performance of CNT as interconnects. Basically, there are two kinds of contacts such as side-contact and end-contact. The side-contact relies on Van der Waals bond while the end-contact has covalent metal-carbon bonds as an interface. In this manual, we use and describe the end-contact. The selected metal electrode is Pd. It should be noted that SWCNT is a particular case of MWCNT and so in the following introduction and discussion, MWCNT is regarded as a representative of CNT interconnect.

On CVD grown CNTs, defects are omnipresent and may impact its performance. The most typical types include vacancies, interstitials, non-hexagonal rings and grain boundaries. Defects can trap or scatter carriers and thus, ultimately impact CNT interconnect performance. Furthermore, CNT diameter, chirality, and defect variations are found to play an essential role in determining the CNT performance as interconnects. So, a MWCNT/SWCNT compact model capable of evaluating the impact of the defects, diameter and chirality variations on its performance is of high interest.

We present SWCNT and MWCNT interconnect compact models. These models consider the impact of CNT defects, the chirality and contact resistance between CNT-electrode (Pd) on CNT interconnect performances and power consumption. Variabilities of diameter, defect resistance and chirality are also considered in these models by enabling Monte Carlo simulation. Furthermore, the increase in charge based doping of CNT with PtCl<sub>4</sub> is evaluated by Fermi level shift which changes the conducting channel of CNT and then impact the performance, power consumption and variability of CNT interconnect.

We have published our models with detailed Verilog-A codes on *NanoHUB*. If you are interested in looking more in detail or would like to download our model for your usage, please visit <https://nanohub.org/publications/243/1>.

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### EDUCATION

- 09/2016-06/2019 **Ph.D.**, Electrical Engineering. Department of Microelectronics, University of Montpellier, CNRS-LIRMM, Montpellier, France.
- 09/2014-07/2016 **M.S.**, Quantum Devices. Department of Physics, University of Paris7 Denis Diderot, Paris, France.
- 09/2011-07/2014 **B. S.**, Physics. Department of Physics, University of Paris7 Denis Diderot, Paris, France.

### TECHNICAL SKILLS

- **IC design and test:** HSPICE, Cadence
- **Device modeling:** Compact model development with Verilog-A, COMSOL
- **Programing:** MATLAB, Python
- **Experimental skills:** AFM, SEM, TEM, Raman Spectroscopy, UV-Lithography, E-Beam Lithography, RIE, Optical Microscope, Low-Temperature (80K) Measurements
- **Other skills:** EXCEL, Origin, PowerPoint, Word, Latex

### THEORETICAL TRAINING

- **Physics:** Electrons and Phonons in Nanostructures, Quantum Theory of Light, Advanced Solid State Physics, Introduction to Photonic Quantum Devices, Introduction to Electronic Quantum Devices, Nanomaterials for Nanomedicine, Imaging Nano-objects, Quantum Optoelectronics, Devices and Quantum Information, Nanomagnetism and Spintronics
- **Mathematics:** Advanced Numerical Analysis, Advanced Calculus, Mathematical Equations and Special Functions, Probability & Mathematical Statistics
- **Electronics:** Semiconductor Devices and Physics

### RESEARCH INTERESTS

- Nano-electronic devices and interconnects (CNT, Cu-CNT) modeling and variability/reliability
- Novel electronic devices physical compact modeling, fabrication and characterization
- Nano-electronic devices for healthcare and bio-sensing applications
- III-V semiconductor based electronic/optoelectronic devices and detectors
- 1D/2D material based electronic/optoelectronic devices

### RESEARCH EXPERIENCE

- 09/2016-present PhD program Under EU H2020 CONNECT project. Grant agreement: No. 688612  
University of Montpellier, CNRS-LIRMM. *Under the supervision of Dr. Aida Todri-Sanial.*  
(Defense planning in June 2019)  
**Thesis Title: Exploration of Carbon Nanotube and Copper/Carbon Nanotube Composite for Next Generation On-chip Energy Efficient Interconnect Applications**

- Physical understanding of CNT and Cu-CNT composite as possible candidates for local and global interconnect applications.
- Physical understanding and electrical/electro-thermal compact modeling for pristine/doped CNTs, Copper-CNT composite.
- Hierarchical modeling. From atomistic-level simulations (ab-initio) to extract physical parameters which are using for electrical/electro-thermal compact modeling.
- CNT interconnect variability studies.
- Circuit level benchmarking and AC/DC simulations for CNT interconnects with advanced CMOS device (FinFET) and CNTFET.

03-07, 2016 Internship “**Physical modeling on Carbon nanotube based devices and interconnect applications for on-chip integrated circuit.**” CNRS-LIRMM, University of Montpellier, Montpellier, France. *Under the supervision of Dr. Aida Todri-Sanial.*

09-10, 2015 Master Training Project “**Fabrication of Carbon Nanotube Field Effect Transistor (CNTFET) in clean room and electrical characterization**”, Laboratory of Matériaux et Phénomènes Quantiques (MPQ) UMR 7162, University of Paris7 Denis Diderot, Paris, France. *Under the supervision of Dr. Maria Luisa Della Rocca.*

05-07, 2015 Internship “**Process development and clean room experimental test on Nanosphere (Gold / Latex) Lithography**”, Laboratory of Matériaux et Phénomènes Quantiques (MPQ) UMR 7162, University of Paris7 Denis Diderot. *Under the supervision of Dr. Maria AMANTI.*

05-07, 2014 Internship “**Characterization of Quantum Well Inferred Photodetector (QWIP)**”, Laboratory of Matériaux et Phénomènes Quantiques (MPQ) UMR 7162, University of Paris7 Denis Diderot. *Under the supervision of Dr. Maria AMANTI.*

## JOURNAL PUBLICATIONS

1. **J. Liang**, et al. and A. Todri-Sanial, “Investigation of Pt-Salt Doped Stand-Alone Multi-Wall Carbon Nanotubes for On-Chip Interconnect Applications,” **IEEE TRANSACTIONS ON ELECTRON DEVICES**, 2019. doi: **10.1109/TED.2019.2901658**.
2. **J. Liang**, J. Lee, S. Berrada, V. Georgiev, R. R. Pandey, R. Chen, A. Asenov, A. Todri-Sanial, “Atomistic to Circuit-Level Modeling of Doped SWCNT for On-Chip Interconnects,” **IEEE Transactions on Nanotechnology**, 2018, doi: **10.1109/TNANO.2018.2802320**.
3. R. Chen, **J. Liang**, J. Lee, V. P. Georgiev, R. Ramos, H. Okuno, D. Kalita, Y. Cheng, L. Zhang, R. R. Pandey, S. Amoroso, C. Millar A. Asenov, J. Dijon, A. Todri-Sanial, “Variability Study of MWCNT Local Interconnects Considering Defects and Contact Resistances - Part I: Pristine MWCNT”, accepted at **IEEE Transactions on Electron Devices**, 2018, doi: **10.1109/TED.2018.2868421**.
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#### **JOURNAL PAPERS UNDER PREPARATION**

1. **J. Liang**, et al. and A. Todri-Sanial, "Circuit Level Analysis of Pt-Salt Doped Multi-Wall Carbon Nanotubes with Contacts for Local Interconnect Applications". (**to be submitted for IEEE Transactions on Nanotechnology**).

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## Abstract

Improving only the performance and energy efficiency of transistors is not sufficient for future systems-on-chip. On-chip interconnects have become equally critical to transistors and can detriment system's performance and energy efficiency. Copper (Cu) is the state-of-the-art interconnect material and is reaching its physical limit due to scaling. Barrier and scattering effects induce high resistivity and electromigration exacerbates interconnect reliability. Carbon Nanotubes (CNTs) and Copper-Carbon Nanotube (Cu-CNT) composite materials are of interest due to ballistic transport, high scalability, high thermal conductivity and high current density. We investigate from fundamental atomistic level to macroscopic level the physical understanding and electrical compact modelling on CNT and Cu-CNT composite for on-chip local and global interconnect applications. We evaluate and assess the different sources of variations and its impacts on CNT interconnect performance and energy efficiency. Charge transfer based doping of CNT is also investigated as an alternative method to further reduce its resistivity, mitigate CNT chirality variations and contact resistance drawbacks. Experimental measurement results are used to demonstrate the validity and accuracy of our established models. The interconnect models are finally applied to gate- and circuit- level studies as local and global interconnects to evaluate their performance.

**Keywords:** *Carbon nanotube, Interconnect, Energy efficient, Nanotechnology, Modeling*

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## Résumé

Améliorer uniquement les performances et l'efficacité énergétique des transistors n'est pas suffisant pour les futurs systèmes sur puce. Les interconnexions sont également essentielles et ont de graves répercussions sur les performances globales du circuit et l'efficacité énergétique. Le cuivre (Cu) est le matériau d'interconnexion conventionnel qui a aujourd'hui atteint ses limites par suite de l'effet de la miniaturisation. Les effets de barrière et de dispersion induisent une résistivité élevée et une forte électromigration aggravent la fiabilité d'interconnexion. Les Nanotubes de carbone (CNT) et les composites de Cuivre et Nanotube de carbone (Cu-CNT) sont intéressants grâce à leur transport balistique, à la grande évolutivité, à la conductivité thermique élevée et à la densité de courant élevée. Dans ce travail, nous étudions les propriétés physiques fondamentales et électriques des CNT et des composite de Cu-CNT de l'échelle atomique à l'échelle macroscopique pour les applications d'interconnexions locales et globales. Nous évaluons les différentes sources de variabilité et leurs impacts sur les performances d'interconnexion des CNT et l'efficacité énergétique. Le dopage basé sur le transfert de charge des CNT est également étudié en tant que moyen important de réduire davantage sa résistivité et d'atténuer les variations de chiralité des CNT ainsi que d'alléger les effets sur la résistance de contact. Les résultats des mesures expérimentales sont utilisés pour démontrer la validité et la précision de nos modèles établis. Les modèles d'interconnexion sont enfin appliqués aux études à l'échelle de portes et de circuits en tant qu'interconnexions locales et globales pour évaluer leurs performances.

**Mots clefs:** *Nanotube de carbone, Interconnexion, Efficacité énergétique, Nanotechnologie, Modélisation*