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# A DC-DC power converter study for High Voltage Direct Current (HVDC) grid: Model and control of the DC-DC Modular Multilevel Converter (M2DC)

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CENTRALE LILLE

## THESE

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En

Spécialité : Génie électrique

Par

**Yafang LI**

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**Etude d'un convertisseur DC-DC pour les réseaux haute tension à courant continu (HVDC) : modélisation et contrôle du convertisseur DC-DC modulaire multiniveaux (M2DC)**

**A DC-DC power converter study for High Voltage Direct Current (HVDC) grid: Model and control of the DC-DC Modular Multilevel Converter (M2DC)**

Soutenue le 11 Juillet 2019 devant le jury d'examen :

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*To the future*





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# *Résumé étendu*

## **Contexte**

Lors du siècle précédent, les développements technico-économique de l'énergie électrique se sont basés sur les énergies fossiles (charbon, gaz naturel, pétrole et nucléaire). L'exploitation de ces énergies a provoqué une augmentation des émissions de gaz à effet de serre avec les conséquences que nous connaissons actuellement. Suite à une prise de conscience mondiale, des protocoles ont été signés et des démarches ont été mises en œuvre pour limiter les dégâts. L'une des principales actions consiste à limiter progressivement les sources d'énergies fossiles en les remplaçant par des sources d'énergies plus propres, (solaire et/ou éolien). Le potentiel du gisement éolien en Europe est très fort et un grand nombre de projet sont en développement.

En Europe, ces sources d'énergies renouvelables à haut gisement sont plutôt disponibles sur des sites en mer, en général au large. La localisation de ces sites, nécessite des câbles sous-marins (et/ou sous terrain). L'utilisation de la transmission en régime alternatif (sous acronyme anglophone : AC) est non faisable d'un point de vue technique. De plus, pour des raisons environnementales, d'acceptabilité de la société, des décisions politiques ont limité le développement de nouvelles lignes aériennes. Les investissements se sont donc orientés vers de liaisons enterrées, engendrant les mêmes contraintes que précédemment. De ce fait, la migration vers des liaisons en courant continu (sous acronyme anglophone : DC) pour les réseaux électriques en haute tension devient une nécessité face aux défis actuels.

Un défi majeur de ces dernières décennies était de proposer un système d'interfaçage entre les réseaux AC existant et les réseaux DC proposés. Cette interface a été dans un premier temps réalisée par des convertisseurs de puissance à base de thyristors appelés LCC (convertisseurs commutés par la ligne or Line Commutated Converter). Cette technologie permet de transiter une grande quantité de puissance (plusieurs GW) mais nécessite un gros dispositif de filtrage et de compensation de la puissance réactive. De plus, elle possède une dynamique relativement lente nécessitant l'inversion de polarité du câble.

L'émergence des convertisseurs de type source de tension (Voltage Source Converter, VSC) s'est faite suite aux développements technologiques et pour répondre aux exigences des cahiers des charges. Le recours à cette technologie se justifie en partie par le fait que les flux de puissance peuvent être commandés dans les deux sens sans changer la polarité de la tension continue et facilite l'intégration de sources d'énergies renouvelables tout en équilibrant les puissances sur des grandes étendues. Dans la littérature, il existe de nombreuses topologies de convertisseurs de type VSC, néanmoins une topologie sort du lot

pour l'application des réseaux électriques continus en haute tension. Connue dans le domaine, sous la dénomination de Convertisseur Modulaire Multi-niveaux (Modular Multilevel Converter, MMC), cette topologie a été largement présentée dans la littérature, avec beaucoup de succès, par Dr. Lesnicar et Prof. Marquardt. Les avantages majeurs de cette topologie sont d'être modulaire (en terme de tension, puissance, etc.) tout en apportant la possibilité de travailler avec des fréquences de commutation assez faibles (limitant les pertes) et garantissant une meilleure performance harmonique suffisamment élevée pour limiter les filtres.

Cette technologie est, depuis sa 1<sup>ère</sup> publication, devenue mature et industriellement utilisée dans les liaisons HVDC (mentionnées précédemment comme les réseaux continus en haute tension) comme TRANSBAY, INELFE, Zhoushan Multi-terminal DC Interconnection et Nan'ao.

L'augmentation de la fiabilité du réseau DC se fera comme pour le réseau AC au travers du maillage du réseau. Basé sur ce constat, le concept de réseau Continu Multi-Terminaux (MTDC) émerge depuis une dizaine d'années permet aussi d'assurer une meilleure continuité de service, de renforcer les interconnexions entre différentes zones de l'Europe voire de plusieurs continents avec le concept de SuperGrid dans la mer du nord.

La multitude de projets de liaison HVDC indique que les premiers réseaux MTDC se feront par l'interconnexion de plusieurs liaisons. L'interconnexion directe de plusieurs liaisons HVDC ne sera assurément pas possible dans une grande partie des cas. En effet, il n'est pas certain que les niveaux de tension, le système de mise à la terre de ces réseaux et/ou que le propriétaire/constructeur de ces liaisons soient identiques. Il s'avère donc nécessaire d'introduire des convertisseurs statiques DC/DC pour assurer l'interfaçage de ces différents réseaux comme le montre la figure ci-dessous (fig. i).

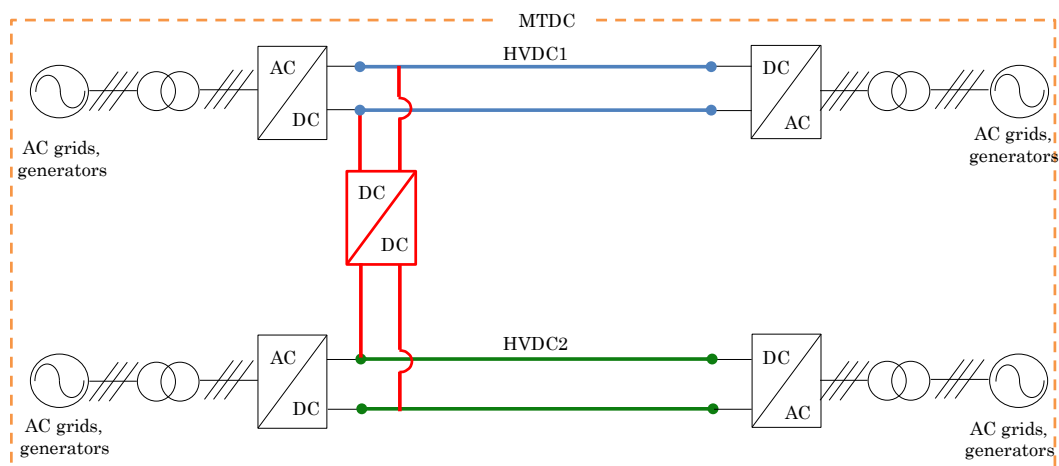


fig. i. Réseau DC Multi-Terminaux

La technologie de convertisseur DC/DC haute tension et haute puissance pour le réseau HVDC n'est pas encore suffisamment développée pour être proche de l'industrialisation dont les principaux défis liés au convertisseur DC/DC sont la difficulté de monter en tension et la protection du défaut. Cette thèse se focalise sur l'étude et le contrôle de ces convertisseurs existants de la littérature et plus particulièrement sur la topologie du convertisseur DC-DC Modulaire Multiniveau (M2DC).

### Plan de la thèse

Le Chapitre 1 de cette thèse introduit dans un premier temps le contexte de cette l'étude et confirme la nécessité de développer des topologies de convertisseur DC/DC pour les réseaux HVDC. Dans un second temps, un état de l'art des convertisseurs DC/DC passera en revue les topologies existantes de la littérature. Deux familles de convertisseurs peuvent être définies, les convertisseurs classiques et modulaires. Cette deuxième partie est constituée de deux types de conversion, direct ou indirect. Le direct a un seul étage tandis que l'indirect en a au moins deux, car ce dernier se réalise par au moins un DC/AC et un AC/DC. Parmi les propositions, le convertisseur DC-DC modulaire multiniveau (M2DC) est sélectionné pour sa structure potentiellement intéressante. Ce convertisseur est présenté dans fig. ii.

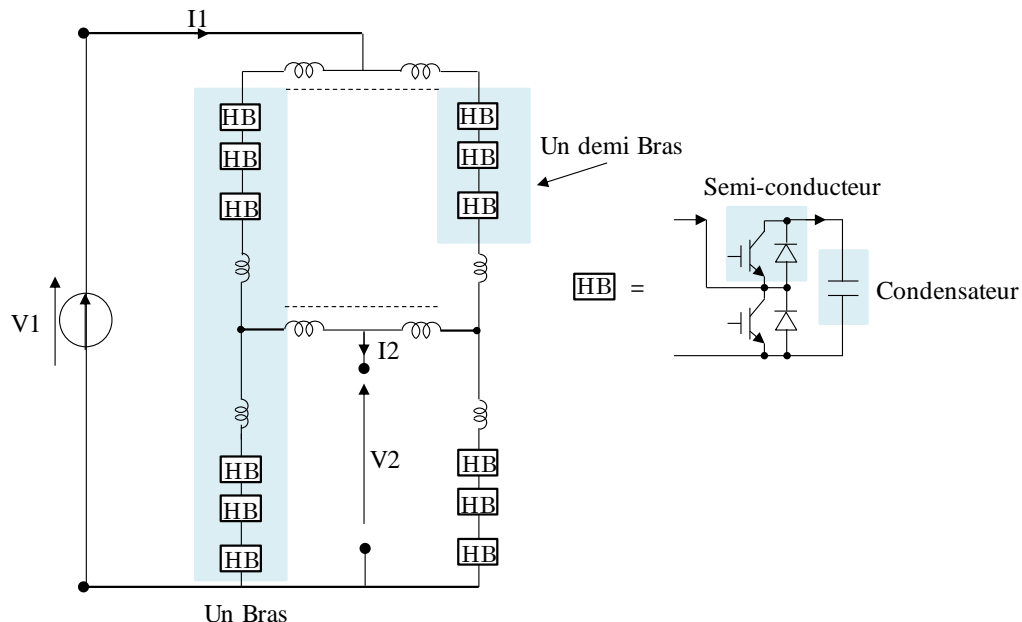


fig. ii. Convertisseur DC-DC modulaire multiniveaux

Le Chapitre 2 présente la topologie du convertisseur M2DC et son principe de fonctionnement. Ce chapitre commence par une analyse générale de l'architecture du convertisseur. La topologie est composée de sous-modules (demi-pont ou pont complet) identiques à ceux nécessaires aux MMCs. Comme ce dernier, le M2DC bénéficie donc des

pertes par commutation assez faibles, d'une modularité d'une évolutivité forte. De plus, le M2DC hérite directement d'une maturité relative, provenant de l'industrialisation du MMC, plus importante que d'autre topologie. Le principe de fonctionnement du convertisseur M2DC et sa conception sont centrés sur la topologie de sous-modules en demi-pont. La première partie établit le modèle moyen équivalent des bras du M2DC. Le modèle de bras permet d'identifier le comportement global du convertisseur en régime établi en négligeant la commutation des semi-conducteurs.

L'étude du comportement global se poursuit par la présentation du moyen d'équilibrer l'énergie stockée dans les condensateurs des sous-modules. Le modèle moyen du convertisseur permet d'étudier et d'illustrer le principe de fonctionnement, les caractéristiques et les contraintes électriques du convertisseur.

Dans le Chapitre 3, une stratégie de contrôle du convertisseur est passée en revue. Le premier objectif est de confirmer les comportements statiques analysés dans le chapitre précédent. Le second est d'étudier les comportements dynamiques du M2DC au travers des énergies stockées internes. Le contrôle de l'énergie comprend deux boucles en cascade, une boucle de courant qui est la boucle interne et une boucle d'énergie (ou boucle de tension) qui est la boucle externe. Étant donné que chaque branche du convertisseur doit fonctionner de la même manière (avec les courants/tensions déphasés pour ne pas avoir de composante AC dans les réseaux DC), le contrôle présenté dans ce chapitre s'applique à n'importe quel nombre de branches. Une opération de découplage du modèle est nécessaire pour fiabiliser la commande. Le chapitre commence par la proposition d'un modèle découplé obtenu par un changement de variables. Ce découplage modifie également le cadre de référence sur lequel le modèle de convertisseur a été construit dans le chapitre. Sur la base du modèle découplé, des boucles de contrôle sont développées pour valider l'analyse en régime permanent du chapitre précédent et permettre une meilleure compréhension du comportement dynamique du convertisseur. Une étude des performances dynamiques du convertisseur permet de comprendre les avantages et les limitations du contrôle proposé.

Le quatrième chapitre se focalise sur la validation de l'implantation du contrôle développé précédemment sur un DSP cible de type Texas Instrument TMS320F28377D. La validation de ce contrôle est réalisée à l'aide des outils de simulation temps réel et avec un environnement de test HIL (Hardware in the Loop). Cette validation se base sur les paramètres non modifiables du convertisseur MMC présent au laboratoire L2EP (Laboratoire d'électrotechnique et de puissance de Lille) mis au point lors de précédents projets (nombre de sous modules, sous-modules en demi-pont, valeur des condensateurs). Ce chapitre commence par une description des cas d'étude se basant sur le prototype MMC associé au cas test du groupement CIGRE B4.76 travaillant sur ce type de convertisseur. La méthodologie de développement du contrôle est ensuite présentée en commençant par

la partie simulation temps réel du convertisseur M2DC se basant sur un système de technologie OPAL-RT puis sur la partie simulation HIL. Le modèle instantané du convertisseur et du contrôle rapproché des sous-modules est présenté. Ce dernier a pour vocation de maintenir l'équilibrage des tensions flottantes des condensateurs des sous-modules dans un bras tout en générant la tension de référence que lui demande le contrôle éloigné. Ce chapitre se termine par la comparaison sur les résultats entre la simulation Matlab (dite hors ligne), la simulation temps réel et le test HIL aussi bien sur le régime statique que dynamique. Ces conclusions montrent que le prototype actuel du MMC ne peut pas être utilisé dans certains cas test car la capacité interne des sous-module est trop faible pour l'application M2DC. La partie HIL montre aussi qu'il est nécessaire d'améliorer la stratégie de contrôle à puissance nulle pour des raisons de stabilité numérique qui n'ont jamais été mise en évidence en simulation hors ligne ou temps réel.

### **Les conclusions de la thèse**

Les réseaux à Courant Continu (HVDC) représentent une solution fiable et moins chère pour transmettre l'électricité haute tension et forte puissance sur de longues distances. Pour augmenter la flexibilité de ces réseaux, les réseaux Continus Multi-Terminaux (MTDC) sont proposés pour interconnecter différentes liaisons DC. Dans les interconnexions, des convertisseurs DC/DC de puissance sont nécessaires au cas où les liaisons DC ne sont pas identiques. Donc, l'objectif de cette thèse est d'étudier un convertisseur DC/DC haute tension et forte puissance.

En réponse à la problématique liée au convertisseur DC/DC « haute tension forte puissance », le premier chapitre révise les structures proposées dans la littérature. En comparant leur volumes et rendements, le convertisseur « DC-DC modulaire multiniveaux » (M2DC) a été choisi pour les applications HVDC.

Le chapitre 2 propose le modèle moyen et explique le fonctionnement du convertisseur M2DC. Pendant les analyses, il observe que le M2DC a besoin des composants alternatif qui sont limités par la structure du convertisseur. La fin de ce chapitre propose les dimensionnements des inductances des demi-bras et des condensateurs des sous-modules.

Les analyses théoriques du chapitre 2 sont validées dans le troisième chapitre. Ces validations sont réalisées par un simple contrôle du convertisseur en inversant le modèle moyen. Les simulations sous Matlab ont également validé la capacité de la haute tension et forte puissance du convertisseur par le cahier des charges du CIGRE.

Dans le chapitre 4, un dimensionnement du M2DC en utilisant le MMC existant du L2EP est proposé, tout d'abord, basé sur les analyses théoriques du deuxième chapitre. Le chapitre propose ensuite une méthodologie d'implémentation de contrôle sous HIL. La fin du chapitre valide le dimensionnement et le contrôle du convertisseur par des



comparaisons de trois types de simulation : simulation hors ligne, simulation en temps réel et simulation HIL.

Sur le M2DC, il est aussi possible d'en conclure que ce convertisseur est plus adapté pour un ratio  $\alpha > 0.5$  du aux moindres courants alternatives internes, donc moins de pertes.

Toutefois, pour avoir une vision plus complète sur les structures proposées dans la littérature, il est nécessaire de comparer le M2DC avec les autres structures qui ne sont pas étudiées dans la thèse.

En plus, certaines perspectives concernant le M2DC sont proposées pour améliorer sa performance. Ces perspectives concernent le dimensionnement, le contrôle éloigné, le contrôle rapproché et l'intégration du M2DC dans le MTDC.

**Mots-clés :**

MTDC, DC/DC, M2DC, modélisation, analyse en régime établi, contrôle, Simulation en Temps Réel, Hardware-In-the-Loop (HIL)

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# Nomenclature

Lists of symbols used in this work are found in the following descriptions.

## Acronyms

AC	Alternative Current
ADC	Analog-to-Digital Converter
CBA	Control Balancing Algorithm
CIGRE	Conseil International des Grands Réseaux Electriques
CPU	Central Processing Unit
CSC	Current Source Converter
DAB	Dual Active Bridge converter
DC	Direct Current
DQ transformation	Direct-Quadrature transformation
DSP	Digital Signal Processor
FB	Full Bridge
FC	Flying Capacitors converter
FPGA	Field-Programmable Gate Array
FTBO	Fonction Transfer en Boucle Ouverte (open loop transfer function)
FTBF	Fonction Transfer en Boucle Fermée (closed loop transfer function)
HB	Half Bridge
HIL	Hardware In-the-Loop
HuT	Hardware under Test
HVDC	High-Voltage Direct Current
IEA	International Energy Agency
IGBT	Insulated Gate Bipolar Transistor
L2EP	Laboratoire d'Electrotechnique et d'Electronique de Puissance de Lille
LCC	Line Commutated Converter
NLC	Nearest Level Control
NPC	Neutral-Point-Clamped converter
NVC	Nearest Vector Control
M2DC	DC-DC Modular Multilevel Converter
MMC	Modular Multilevel Converter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTDC	Multi-Terminal Direct Current
Mtoe	Million tons of oil equivalent energy
PI	Proportional Integral
PID	Proportional Integral Differential

PR	Proportional Resonance
PLL	Phase-Locked Loop controller
PWM	Pulse Width Modulator
RoS	Rest of System
RT	Real-Time
SACOI	Sardinia-Corsica-Italy
SM	Submodule
SHE	Selective Harmonic Elimination
SVM	Space-Vector Modulation
TWENTIES	Transmission system operation with a large penetration of wind and other renewable electricity sources in electricity networks using innovative tools and integrated energy solutions
VSC	Voltage Source Converter
XLPE	cross-linked polyethene insulation

#### Subscripts, circumflexes and prefixes

*	Complex conjugate
$\Sigma$	Sum
$\Delta$	Difference
$\hat{\cdot}$	Peak value
$\underline{\cdot}$	Vector
$\langle \cdot \rangle$	Average value
$\bar{\cdot}$	Opposite
$u, l$	Upper/lower arm
ref	Reference
$DC, dc$	$DC$ components
$AC, ac$	$AC$ components

#### Converter and grid parameters

$V1$	High pole-to-ground DC voltage side
$V2$	Low pole-to-ground DC voltage side
$I1$	DC current of high DC voltage side
$I2$	DC current of low DC voltage side
$P1$	Transmission power seen from high DC voltage side
$P2$	Transmission power seen from low DC voltage side
$P_{ref}$	Transmission power reference
$P1_{ref}$	Power reference of high DC voltage side
$P2_{ref}$	Power reference of low DC voltage side
$\alpha$	DC voltage ratio
$M$	Number of legs
$N$	Number of submodules per arm
$C$	Submodule capacitance

$C_{tot}$	Capacitance of equivalent arm model
$l$	Arm inductance
$r$	Parasitic arm resistance
$L_s$	Secondary inductance
$R_s$	Parasitic secondary resistance
Variables	
$m$	Modulation index
$n$	Inserted number of submodules
$t$	Time
$i_{u,l}$	Current of upper and lower arms
$i_s$	Secondary current
$v_{mu,l}$	Voltages of upper and lower arms
$i_{diff}$	Average current of two arm currents
$v_{diff}$	Average voltage of two arm voltages
$v_v$	Half of difference of two arm voltages
$v_c$	Submodule capacitor voltage
$v_{ctot}$	Capacitor voltage of equivalent arm model
$i_m$	Current of capacitor of equivalent arm model
$W_C$	Stored energy of equivalent arm model
$W_{u,l}$	Stored energy in upper and lower arms
$W_c^\Sigma$	Stored capacitor energy per leg
$W_c^\Delta$	Imbalanced capacitor energy
$P_{DC}$	Average value of power of DC component
$p_{DC}$	Instantaneous power of DC component
$P_{AC}$	Active power of AC component
$p_{u,l}$	Arm instantaneous power
$P_{u,l}$	Arm average power
$\lambda$	Phase angle between $i_u$ and $i_l$
$\varphi$	Phase angle between $i_u$ and $v_{mu}$
$\varphi_1$	Phase angle between $i_{diff,ac}$ and $v_{diff,ac}$
$\varphi_2$	Phase angle between $i_{s,ac}$ and $v_{v,ac}$
$\theta$	Phase angle between $v_{mu}$ and $v_{ml}$
$\theta'$	Phase angle between $v_{diff}$ and $v_v$
$f$	Fundamental AC frequency
$\omega$	Fundamental angular frequency / pulsation
Controller parameters and transfer functions	
$K_p$	Proportional Gain
$K_i$	Integral Gain
$G(s)$	Canonical form of second order system
$T_r$	Response time
$\omega_n$	Natural Frequency



$\xi$	Damping ratio
$H_{diff}(s)$	Transfer function of the subsystem $i_{diff}$
$H_s(s)$	Transfer function of the subsystem $i_s$
$H^\Sigma(s)$	Transfer function of the energy $W_c^\Sigma$
$H^\Delta(s)$	Transfer function of the energy $W_c^\Delta$

# Introduction

More and more energy is required to satisfy our daily electricity demand. Facing climate change and preserving at the most environment, modern electricity production is changing from burning fossil fuels to clean renewable energy (solar/hydro/biomass/wind/ocean/geothermal energy, etc.).

Electrical energy can be transmitted in two ways: AC transmission or DC transmission. Historically, AC transmission is the most used electricity transportation thanks to its low losses and low costs, but limited by the line capacitance in long distance transportation. Nowadays, DC transmission used for dozens of years has been proved more suitable and reliable for long distance transmission thanks to its no reactive power and no need of compensation. Thereby, as renewable energy generators are usually far from consumers, DC transmission is deemed more suitable than AC transmission.

So far, most DC links are “Point to Point” with electricity transmitted from one converter station to another. To improve the power flow control and connect different existing DC links, MTDC grids are necessary with three or more converter stations. The first industrially realized MTDC grids has parallel connections using thyristor technology DC links with the same DC voltage on each converter stations. With the escalated number of DC links, DC voltage of each link can be different, as well as the converter technology. HVDC DC/DC converters are mandatory to connect these different DC voltage links together.

An example of these requirements is illustrated in the CIGRE test case, where each DC/DC converter should have more than 100kV of voltage capability, more than 100MW of power capability and bi-directional power transmission. The converter satisfying these requirements is still unknown due to voltage and power level regarding the semiconductor technology. Thereby, with high voltage and high power issue, Chapter 1 reviews existing potential DC/DC topologies. These existing topologies are presented in two categories: classical DC/DC converters and modular DC/DC converters. The classical DC/DC converters are conventional non modular topologies, such as buck, double buck and flying capacitors DC converters. In modular DC/DC converters, a series connection of Dual Active Bridges and Modular Multilevel DC Converters using Modular Multilevel Converter are presented. Among these topologies, DC-DC Modular Multilevel Converter (M2DC) has been selected as an investigation subject.

Focusing on M2DC, Chapter 2 proposes a mathematical model and investigates its operation principle in steady state to understand the converter limitations. This analysis will be helpful for the converter design and is the central part of the thesis.

Based on the converter model, a basic control algorithm is proposed in Chapter 3 to validate the analysis presented in Chapter 2. The principle is to maintain energy of each capacitor of the converter. Using the proposed control, the converter theoretical analysis is confirmed with Matlab simulations.

Once the converter is analyzed theoretically (Chapter 2) and confirmed with simulations (Chapter 3), its implementation in an existing smaller scaled laboratory MMC mock-up is investigated in Chapter 4. Firstly, a design method of an M2DC based on MMC is proposed. Then, this chapter develops a methodology of control implementation in Hardware-In-the-Loop (HIL) simulation, which is a preparation for a safe and secure M2DC practical test.

Finally, a conclusion for the realized work is presented and perspectives are discussed, which includes a necessary performance comparison between other topologies and M2DC, and also propositions to improve M2DC performances.

# I Context and state of the arts for HVDC DC/DC converters

## I.1 Background

According to the International Energy Agency (IEA) statement, global energy demand grew by 2.1% in 2017, which is more than twice the growth rate in 2016. It reached an estimated 14 gigatonnes of oil equivalent energy (Mtoe), in which fossil fuels are the principal growth (70%) [1], [2]. At the same time, IEA states also that global energy related CO<sub>2</sub> emission grew by 1.4% in 2017 than 2016, reaching a historical high of 32.5 gigatonnes, which contrasts with the demand of Paris Agreement established in December 2015.

However, it is hopeful to see that emissions dropped in some countries in 2017, such as United States, United Kingdom, Mexico and Japan, thanks to coal-to-gas switching, higher renewable based electricity generation and nuclear generation [1]. Moreover, China, which is the “first” country for carbon emissions, has increased its emission increased just by 1% in 2017 than their 2014 level, thanks to a continued renewable deployment and a coal-to-gas switching [1].

These reports confirm positively that renewable energy generation is possible and efficient to reduce carbon emissions. But there are still a lot of works and efforts to do to cope with climate change and meet the Paris Agreement.

The renewable energy mentioned above includes solar/hydro/biomass/wind/ocean/geothermal energy [2]. The thesis focuses on High Voltage Direct Current (HVDC) transmission, which is the technology trend to integrate renewable energy in power systems.

### I.1.1 AC transmission versus DC transmission

Alternative Current (AC) transmission (Fig 1) is the most used transmission technique. The three-phase alternative current allows the direct use of electrical machine as power generator and transformers ensuring voltage adaptation in a low losses and low cost way.

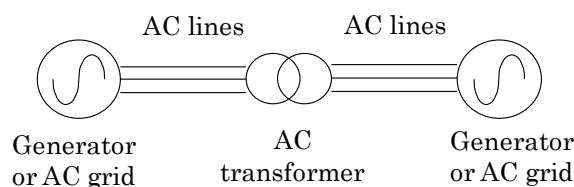


Fig 1. AC grid or transmission

However, the limitation of AC transmission is linked to the capacitance value of long cable in great power transmissions [3] creating reactive power, which greatly increases cable currents and definitely limits power transmission. It can be solved by two methods explained in [3]: using shunt inductive reactors along the cable line to compensate reactive power or using DC transmission instead of AC transmission.

Fig 2 shows AC line performance with and without compensation. Transmission distance decreases when delivered power and line voltage increase. To transmit more power in high voltage, inductive compensation is mandatory to extend the transmission distance. However with reactors, a higher cost is necessary. This solution is also ineffective for undersea transmissions where numerous offshore substations are needed.

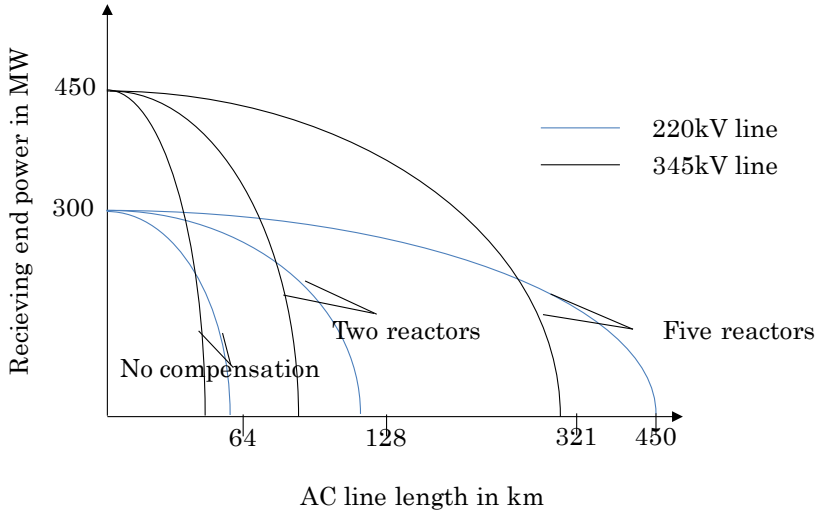


Fig 2. AC line performance [3]

Thereby, DC transmission (Fig 3) is a solution to deliver the high power from remote generator plants without reactive power compensators.

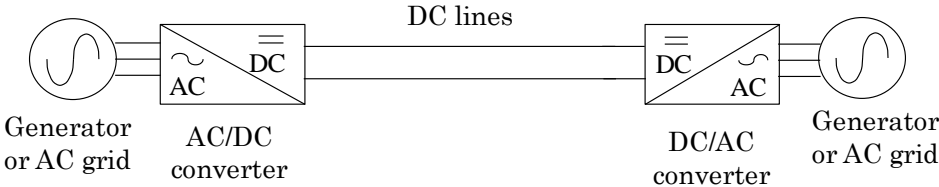


Fig 3. DC grid or transmission

Some advantages of DC transmission over AC are described as follows:

- Low costs for long distance:

DC transmission shows lower costs over the critical distances (Fig 4), according to power and voltage (approx underground: 600-800km, undersea: 50km), than AC even though DC terminal stations are more expensive [5]. It is linked to the huge cost of compensators increasing according to the line distance.

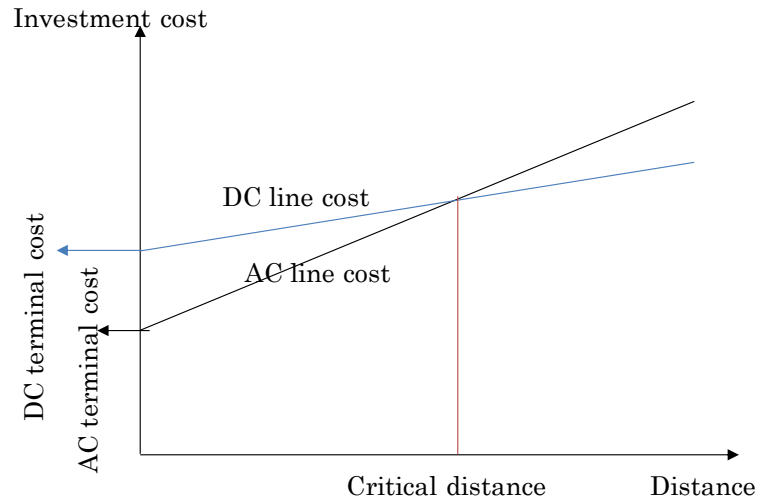


Fig 4. Comparison of AC and DC investment costs [5]

- Interconnection of asynchronous grids:

If two AC grids need to be connected, their frequency, voltage and phase must be identical. However, the interconnection can be realized by DC transmission thanks to AC/DC and DC/AC converters [6].

- No skin effect:

Skin effect exists in AC conductors where current frequency is high. DC transmission avoid the skin effect using direct current which reduces conductor losses compared to AC transmission.

These advantages make DC transmission the preferred solution for long distance, high voltage and great power transmission. However, several disadvantages should be also taken into account to minimize costs and losses:

- Expensive:

Fig 4 shows DC transmission economic benefits for long distance. However, it is also true that DC/AC and AC/DC converter stations are more expensive than AC substations. Therefore, converter design criteria has small footprint and low cost.

- Harmonics:

Power converters are sources of harmonics [7]. These harmonics spread to DC and AC grids, impacting power quality. To reduce high-frequency harmonics, filters are needed to improve power quality which increases costs and weight, especially for high voltage and high power applications. Therefore, efficient high power converters are necessary.

- DC short circuit protection:

Unlike AC grids, DC grids are more vulnerable for short circuit at DC sides. Then, most of DC grids are protected actually from the AC side by AC breaker or protected by control algorithms. A research trend is now to develop DC circuit breakers demonstrators to protect directly DC grid at DC side.

Despite the disadvantages described above, a hundred of DC lines ( around 139 projects reported by ABB and Siemens in 2019 [8]-[11] ) have been commissioned.

## I.1.2 Existing and future installation equipment for HVDC grids

### I.1.2.1 Existing installation equipment

A DC link is created by the connection of two AC/DC converter stations to AC generators transmitting power in DC cables (Fig 5). Regarding the converter stations, two main types of stations exist: Line Commutated Current Source Converter (LCC or CSC) and Voltage Source Converter (VSC).

The LCC is the converter topology after mercury-arc valve industrially confirmed to be suitable for high voltage and power application thanks to high blocking voltage of Thyristor [12].

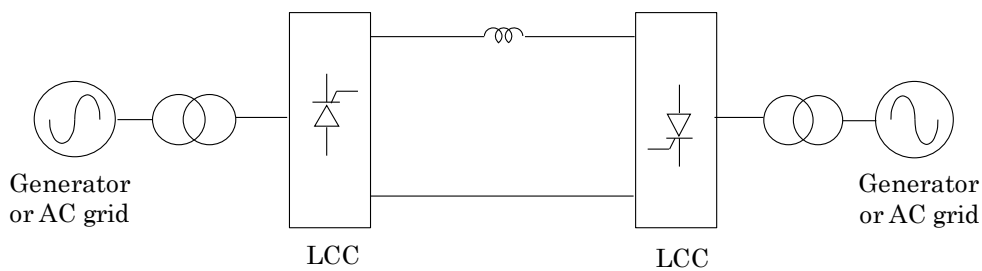


Fig 6. LCC DC link [12]

This converter technology is spread all over the world. Fig 7 shows the example of LCC converter installation at Sellindge side built in 1985 [13] used in the cross-Chanel DC link Britain-France from Sellindge to Les Mandarins (in Bonnigues-Les-Calais).



Fig 7. Sellindge LCC converter station [13]

But due to the LCC technology based on thyristor control, harmonics in AC currents are important. To increase converter performances, VSC DC link is used instead of LCC DC link Fig 8. (a). The VSC DC link uses new VSC multilevel (2 or 3 level) converter technology, Modular Multilevel Converter (MMC) Fig 8. (b). The MMC solution, with its multilevel output voltage, ensures current quality, high efficiency (low frequency switching) and interesting electric performances.

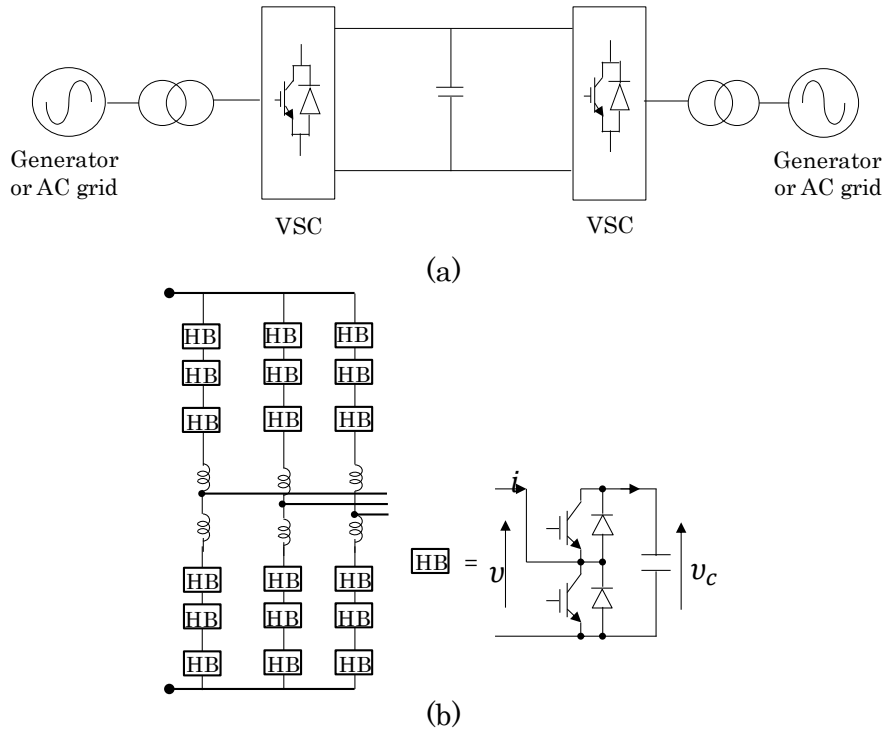


Fig 8. (a) VSC DC link [12] (b) MMC VSC converter

A VSC DC link is used in Baixas-Santa Llogaia Fig 9. (a), where MMC converter station Fig 9. (b) and (c) was built in 2015.



(a)



(b)



(c)

Fig 9. (a) Baixas-Santa Llogaia VSC DC link (b) MMC converter station outside view [15] (c) inside view [18]



Regarding DC transmission cable, Fig 10. (a) and (b) show the extruded dielectric cable with cross-linked polyethene insulation (XLPE) used in Baixas-Santa Llogaia to ensure electrical and mechanical properties.



(a)



(b)

Fig 10. (a) DC cable [16] (b) cable installing in Baixas – Santa Llogaia [15]

**I.1.2.2 Future equipment**

New technologies are proposed for future project installation, for example DC breakers. The potential solution (Fig 11) is able to achieve a DC current breaking in a 320kV/2kA DC grid. It is currently the first high voltage and high current DC breaker. The tested DC breaker is shown in Fig 12.

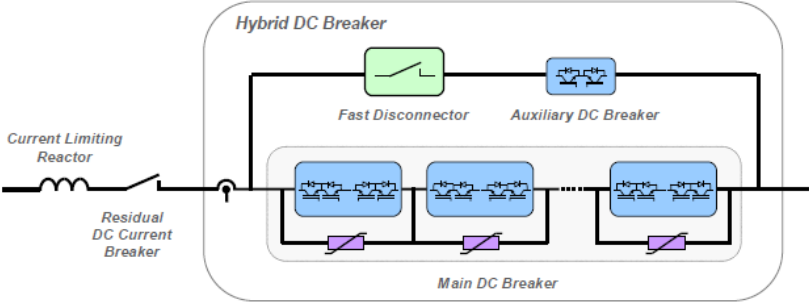


Fig 11. DC breaker [19]



Fig 12. Installation [21]

Besides, robots (Fig 13) are also proposed for monitoring the installed equipment, such as for converter stations.



Fig 13. Monitoring robots (a) Rope robotics [22] (b) ANYmal [23]

These equipment aim to prove the future development of HVDC grids. Along with this development, it is expected to connect different DC links, as it has been done in the past for AC grids in order to assure a high power flexibility.

### 1.1.3 Multi-Terminal DC transmission

Similarly to massively interconnected AC grid, existing point to point DC links are expected to be interconnected to realize the power control. The pre-mentioned DC links with two converter stations are “point to point” DC links. Energy is transmitted from one station to another. To increase power flexibility, future DC grid should be Multi-Terminal DC grid with power exchanged between three or more converter stations.

The Multi-Terminal DC (MTDC) grid is a basic concept proposed in 1956 [24]. The realized MTDC configuration was a parallel connection with the same DC voltage using LCC converter technology (Fig 14).

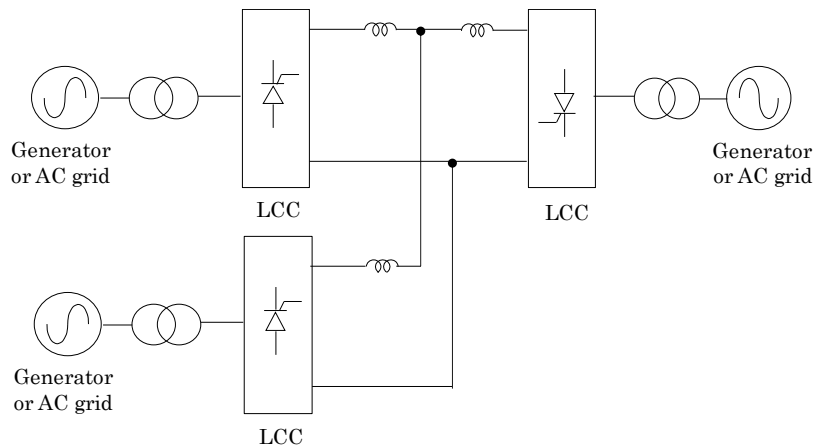


Fig 14. Three terminal LCC DC grid principle

Fig 15. (a), (b), (c) show respectively the commissioned MTDC project Sardinia-Corsica-Italy (SACOI) in 1967, Nelson River project in 1972 and Hydro-Quebec – New England project in 1983.

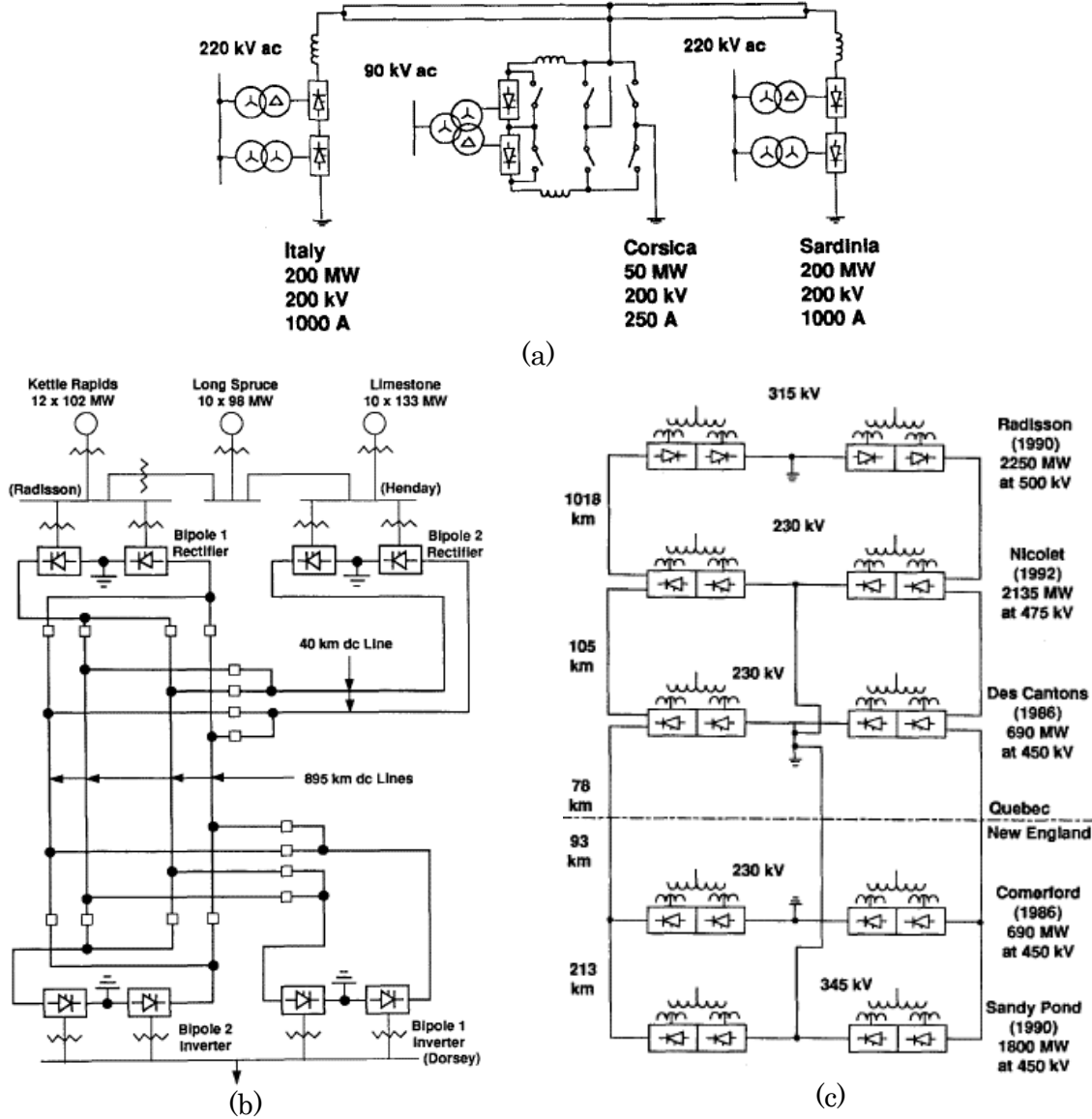


Fig 15. Basic parallel connection (a) in SACOI [25] (b) Nelson River [25] (c) Hydro-Quebec – New England [25]

Due to their parallel configuration, the essential role of those MTDCs was the control of power flow between each station [25]. However, with the escalated number of DC lines, voltage levels or converter technologies can be different in each DC links. Thereby, the parallel configuration is no longer suitable in the general MTDC concept.

To overcome voltage differences, DC/DC converters could be a potential solution to manage the voltage adaptation. The MTDC concept is illustrated in Fig 16.

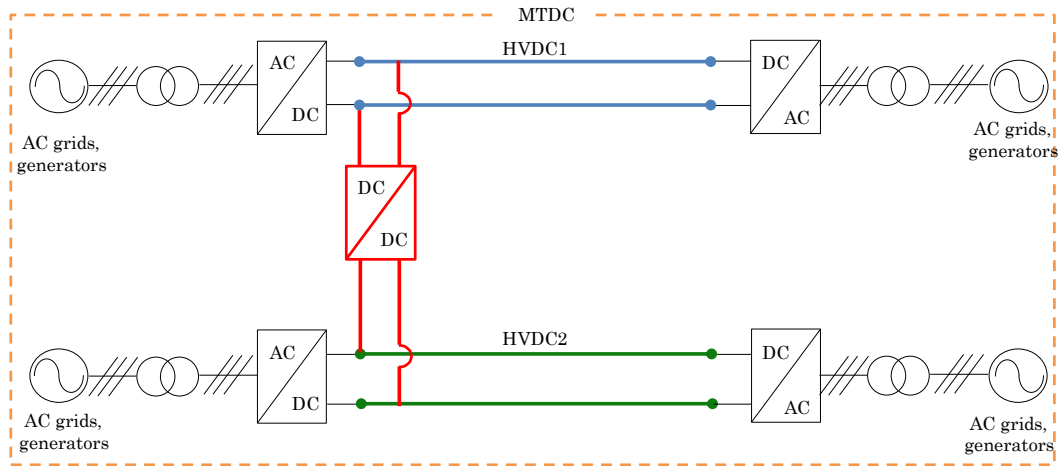


Fig 16. Multi-Terminal DC grid basic principle

DC/DC converters are usually used in Switch Mode Power Supplies with low voltage, but rarely in HVDC applications due to high voltage and high power value. Thereby, five main requirements are expected for the future DC/DC converters:

- High voltage and power: The converter should be able to stand for hundreds kilo volts and hundreds kilo watts.
- Voltage regulation: The converter should be able to step down or up a DC voltage to avoid voltage conflicts between different links.
- Power regulation: The converter should be able to easily control and change the power flow in both directions.
- DC current fault blocking capability: It is better to have self DC current fault protection, as the new DC circuit breaker is not mature.

#### 1.1.4 CIGRE test case analysis

To illustrate the previous requirements, the test case proposed by CIGRE Group B4.76 (Conseil International des Grand Réseaux Electriques) is presented and used in our future simulations. A Multi-Terminal DC grid test case provided by CIGRE B4 group in [26] in 2013 is shown in Fig 17.

From right to left, the test case consists of offshore AC grids, AC/DC conversion, MTDC grid, DC/AC conversion, onshore AC grids and, from up to low, three transmission systems, DCS1, DCS2 and DCS3 with different voltage levels and power ratings.

DCS1 is a point to point DC link with rated voltage  $\pm 200$  kV and power 800 MVA. It connects directly an offshore generator to an onshore consumer via submarine DC cables.

DSC2 is a five sources MTDC system with rated voltage  $\pm 400$  kV. Connections of the five sources are planned by six headlines (solid line) and four submarine cables (dashed line). Five DC/AC converter stations are designed with power rating 1200 MVA for Cb-A1, 1200 MVA for Cb-B1, 1200 MVA for Cb-B2, 400 MVA for Cb-C2 and 800 MVA for Cb-D1.

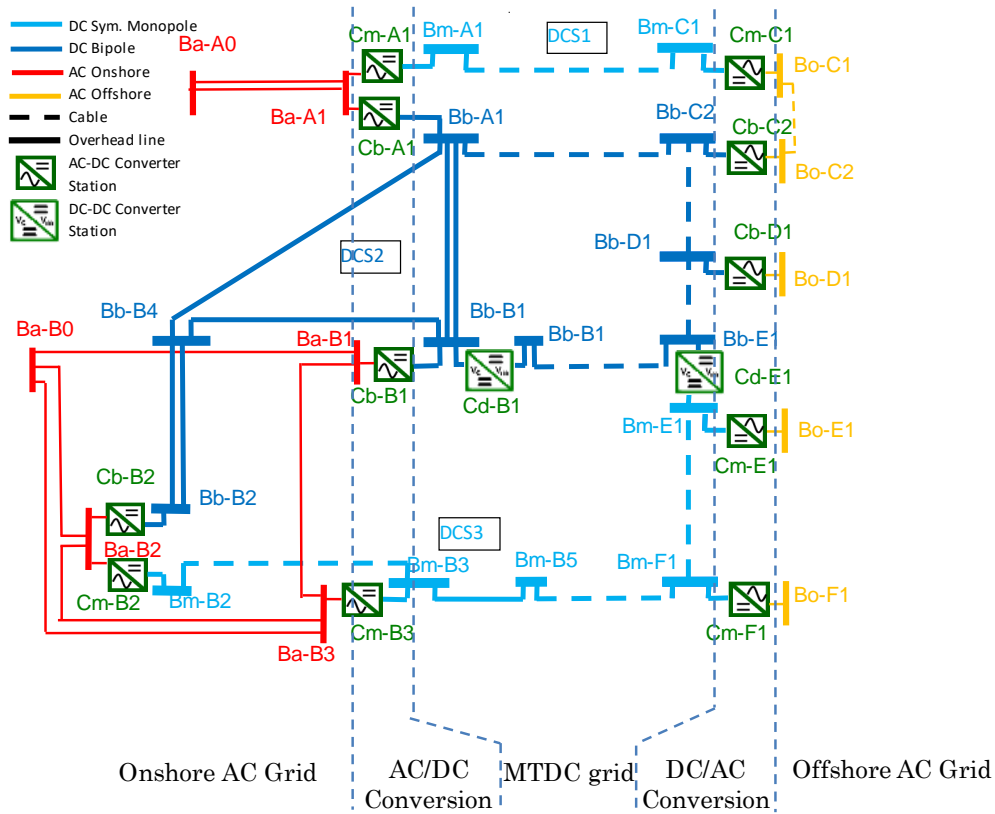


Fig 17. CIGRE B4 DC Grid Test System [26]

DSC3 is a four sources MTDC system. Its rated voltage is  $\pm 200$  kV. It needs three submarine cables (dashed line) and one headline (solid line). Its four converter stations have a rated power of 800 MVA for Cm-B2, 1200 MVA for Cm-B3, 200 MVA for Cm-E1 and 800 MVA for Cm-F1.

To connect DC grids DSC2 and DSC3, the DC/DC converter station Cd-E1 is mandatory to adapt to DC voltages between  $\pm 400$  kV and  $\pm 200$  kV. This converter participates in the power control with a rating power of 1000 MW.

Moreover, in the DSC2 DC grid, a DC/DC converter Cd-B1 is shown in the plan. Depending on CIGRE, Cd-B1 needs a power rating of 2000 MW between two similar sides voltage  $\pm 400$  kV. Its principal role is to control the power flow.

Regarding the positions of two DC converters, Cd-B1 can be an onshore station or an offshore station. But Cd-E1 can only be an offshore station, which is connected with two submarine cables (dashed line).

To conclude, the requirements of MTDC DC/DC converter are described in Table 1. It confirms the demand for DC/DC converters in MTDC grids.

Table 1 DC/DC converter stations Cd-B1, Cd-E1 requirement [26]

Stations	Cd-B1	Cd-E1
Rated voltage	$\pm 400kV/\pm 400kV$	$\pm 400kV/\pm 200kV$
Power rating	2000MW	1000MW
Position	Onshore or offshore	Offshore

Following parts of the thesis will take the requirements described in Table 1 as criteria for DC/DC converter selection, design reference and simulations.

### *1.1.5 Problem statement*

As shown previously, several DC links have been developed to deliver great power in high voltage range. Most existing links are point to point DC links with power exchanged between two converter stations. To increase system flexibility, it is envisaged to build MTDC grids, where the power is exchanged between three or more converter stations. The existing MTDC grids are parallel connections of DC links where each link has the same voltage and converter technology. To adapt to the differences between different DC links, DC/DC converters are mandatory for several hundreds of kilovolts and several hundreds of megawatts. The high voltage and power range are actually the difficulties of DC/DC converter topology.

To deal with the difficulties and answer CIGRE requirements, the main existing DC/DC converter topologies are reviewed in order to extract or propose innovative solutions for MTDC grid connections.

## **1.2 State of the arts for DC/DC converters**

Topologies presented in this section are principally selected with two imposed criteria:

- DC voltage regulation
- and bidirectional power flow

However, the most encountered issues of these topologies are their low voltage and current range. Thereby, this section intends to increase their range to HVDC applications, regarding to CIGRE requirements. Then, the possibility and difficulties of extending voltage and current range are discussed.

The topologies are classified according to their potential modularity. In each class, topologies are also distinguished with their “multilevel” and eventually with their “galvanic isolation” possibilities.

### I.2.1 Classical DC converters

The classical DC converters are non-modular DC converters. They are principally Buck (or boost), Double buck and Flying Capacitors converters (Fig 18). Due to the low voltage and power applications, this part reviews the possibility of extending their voltage and current range.

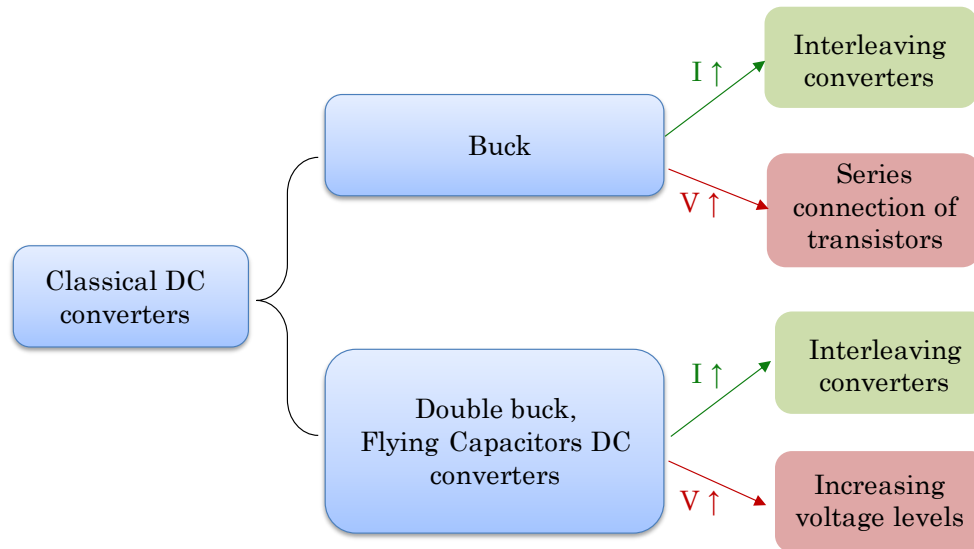


Fig 18. Classical DC converters

#### I.2.1.1 Buck

The Buck converter (shown in Fig 19) is widely used in the low voltage industry such as Switched-Mode Power Supply (SMPS) with two alternative power semiconductors (Transistor/diode). DC power and voltage are stored by only one semiconductor at each time, thereby power and voltage range of the converter are determined by the semiconductor technology.

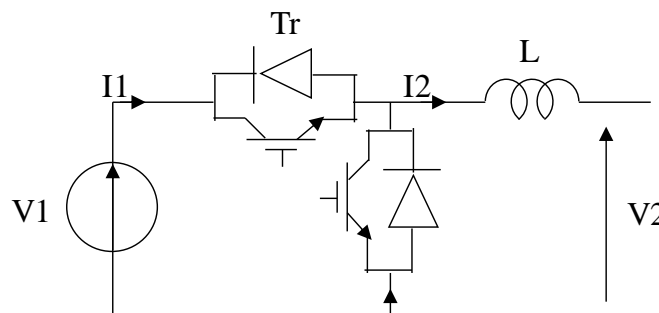


Fig 19. Buck converter

So far available commercial semiconductors can barely support a few kilo volts and a few kilo amperes, which is far from the CIGRE requirements. Thereby, one semiconductor is not sufficient to operate buck converter in MTDC grid.

To raise the voltage and current range, two solutions are:

- using parallel connection and interleaved control to increase the power range
- series connection of transistors to increase the voltage range.

### I.2.1.2 Interleaved converters

Interleaved converters use a parallel connection of converters to increase current range and are modulated with an interleaved control. Fig 20 shows interleaving technique used in two buck converters. The number of buck converters ( $N$ ) can be still increased until satisfying MTDC grids current requirement.

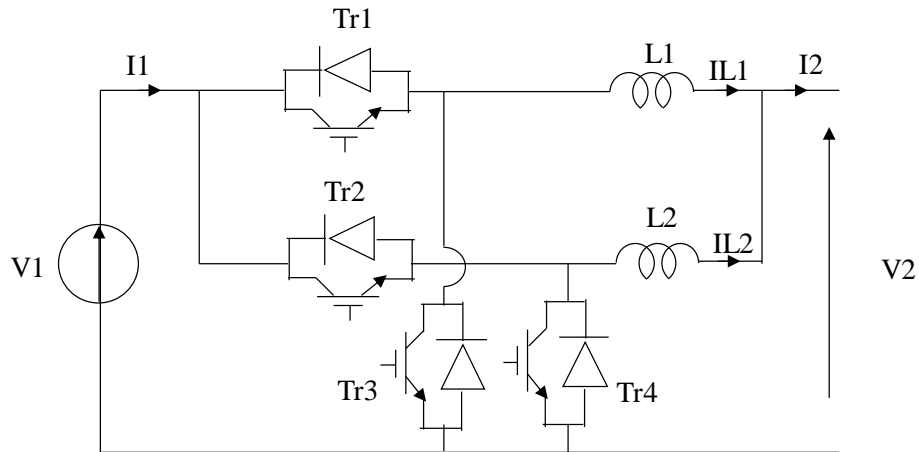


Fig 20. Interleaved buck converter

The interleaving technique is an operation of transistors with phase shift  $2 \cdot \pi/N$  to produce phase shifted current in the inductors. As shown in Fig 21,  $I_{L1}$  and  $I_{L2}$  are phase shifted by  $\pi$  radian during Tr1 and Tr2 alternatively turning-on and off.

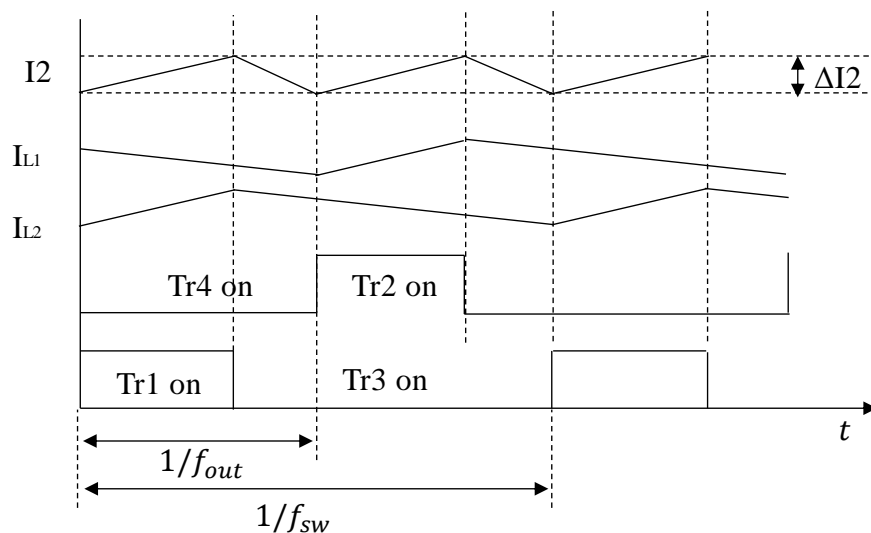


Fig 21. Current waveforms of the converter control

In the case of  $N = 2$ , the frequency ( $f_{out}$ ) of output current ripple ( $I_2$ ) is twice the switching frequency ( $f_{sw}$ ). The increased frequency in the output implies the possibility of reduction of inductance footprint using coupled inductance and a reduction of current ripple  $\Delta I_2$ . Thereby the interleaved converters are proved to be suitable for low voltages and high currents applications, e.g. voltage regulator modules (VRMs) [28].



### I.2.1.3 Series connection of transistors

To increase the voltage range, a series connection of transistors has been used and investigated in the literature. Fig 22 shows an example of the series connection of transistors applied in a Buck converter.

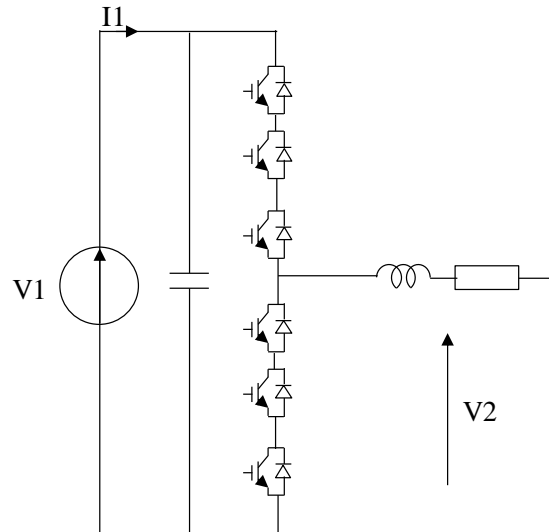


Fig 22. Series connection of transistors applied to Buck converter [29]

The direct series connection of transistors is not as easy as it looks like. According to [30], several issues prevent the spread of the technique as:

- Unequal voltage sharing across transistors due to different delay times of driving circuits.
- Unequal voltage sharing across transistors due to small parameter deviation amongst different devices.
- Unequal voltage sharing across the freewheeling diodes due to different reverse recovery behavior.
- Increase of  $dv/dt$  with the number of series connected devices at the terminals of the converter.

[29], [30] have had also solutions to overcome these pre-mentioned issues using complex controls to keep the same collector-emitter-voltage of each transistor, same transient voltage ( $dv/dt$ ) and current ( $di/dt$ ) of each transistor and the same gate voltage of each transistor at each moment to avoid destructing transistors. Due to the high accuracy demand, extreme complex control and lack of component failure management, the series connection of semiconductors are finally deemed as difficult to be realized for HVDC applications.

### I.2.1.4 Double Buck and Flying Capacitor DC converter

A second potential solution are the multilevel converter topologies, as shown in Fig 23. (a) Double buck converter [32] (b) flying capacitor DC converter [33].

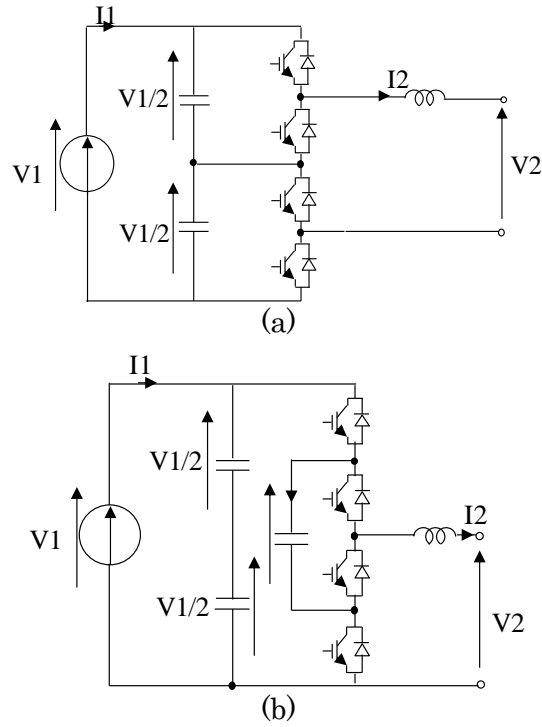


Fig 23. (a) Double bucks (b) Flying capacitor DC converter

Those topologies reduce the voltage of each switch to  $V_1/2$  instead of  $V_1$  in buck. The output frequency is also increased to twice the fundamental switching frequency, thereby the output inductor footprint can be reduced thanks to the reduced voltage and increased frequency. With these advantages, these converters are widely used for applications in electric vehicle (EV) [31], [32].

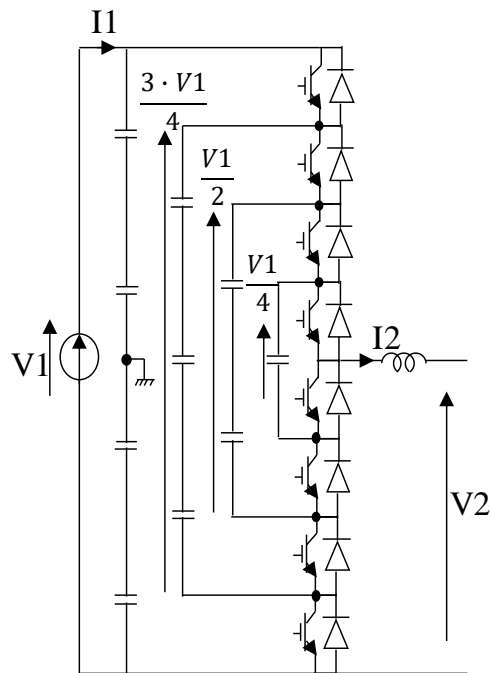


Fig 24. 5 levels Flying Capacitor DC converter

However, it is difficult to apply those topologies in HVDC grids due to the difficulty of balancing capacitors voltage in extending their voltage levels, even though the pre-mentioned interleaving technique can be used to raise the current range. So far as shown in the literature, five levels are the most level numbers for the topologies, e.g. Fig 24 is the extension of FC to five levels.

The increased number of levels is helpful to decrease the voltage of each switches and increase the output switching frequency, thereby reducing inductor filter footprint. In response to the CIGRE requirements ( $V > 100kV$  and  $1kA < I < 10kA$ ), the maximum five voltage levels are far from the almost hundreds of levels needed according to the semiconductor technology. Moreover, the topologies have capacitors concentrate connection in which energy is stored. The great energy stock could involve a danger if a short circuit occurs in the circuit.

In conclusion, multilevel converters are not suitable for HVDC applications due to the issue of raising voltage range of converters. To overcome this obstacle, a last solution is using topologies with high modularity, called hereby “modular converters”.

*1.2.2 Modular DC converters*

DC converters with high modularity (Fig 25) are the series connection of Dual Active Bridge (DAB) and Modular Multilevel DC converters based on the Modular Multilevel Converter (MMC). The Modular Multilevel DC converter topologies are also classified by their converting methods: two stage conversion and single stage conversion.

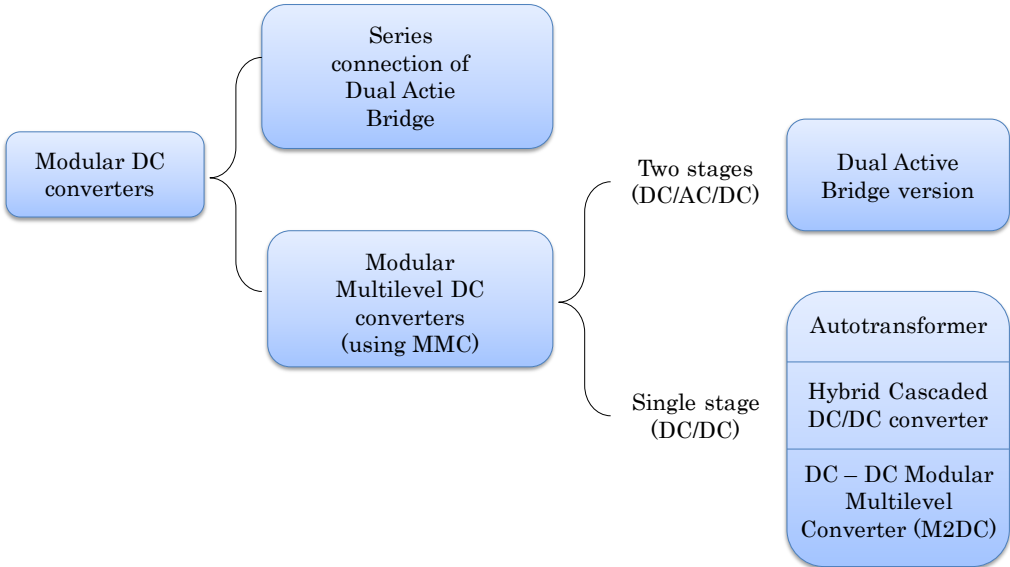


Fig 25. Modular DC converters

### I.2.2.1 Series connection of Dual Active Bridge

The series connection of Dual Active Bridge (DAB) converter is shown in Fig 26, which consists of several DAB converters interconnected (output and input).

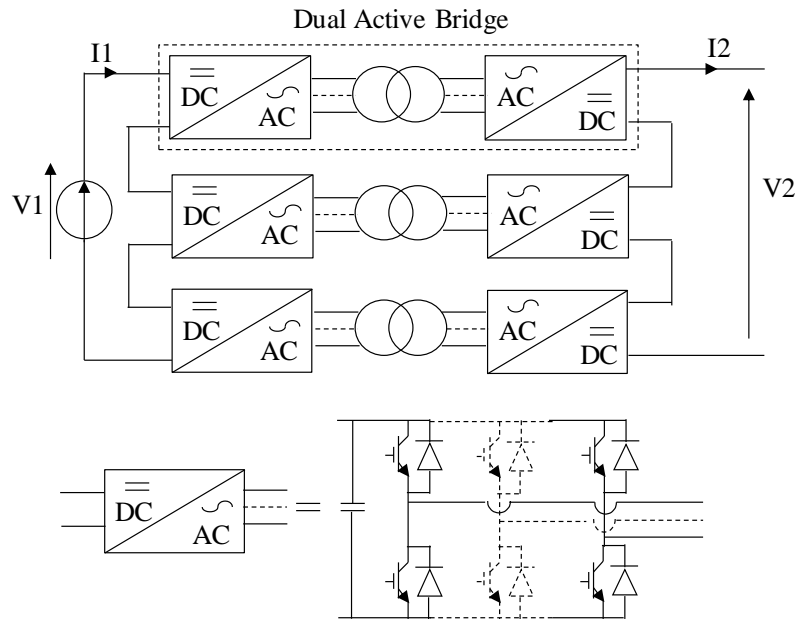


Fig 26. Series connection of Dual Active Bridge

A single Dual Active Bridge (DAB) is a DC/DC bidirectional power converter containing two DC/AC converters interconnected through an AC transformer. The DAB can be three phases or single phase depending on the current range. More phases are, higher DC current is. The transformer is mandatory to isolate current from the primary to secondary. Its volume can be reduced by a higher frequency, which involves potentially more semiconductor losses.

DABs are connected in series to raise the voltage range (Fig 27). The modular topology prevents the issues existed in the pre-mentioned topologies. However, in HVDC applications, the number of modules could be in the hundreds, thereby hundreds of transformers. This great number increases physically the converter volume and technical difficulties of control, e.g. synchronization of different DABs.

As a result, the series connection of DABs succeeds in overcoming the voltage level raising obstacle with the modular topology, but is still deemed unsuitable in HVDC applications due to the great number of transformers.

### I.2.2.2 Modular Multilevel DC Converter (DC-DC MMC)

To reduce the number of transformers, thereby prevent synchronization issues and losses from transformers, a fourth potential solution is Modular Multilevel Converter (MMC) topology based DC/DC converters.

The MMC (Fig 28) has modular topology with basically Half Bridge (HB) submodule which allows raising easily voltage levels. Numerous of Half Bridge submodules are connected in series that the number depends on the semiconductor technology.

Meanwhile, the power range is determined by the number of legs same as the pre-mentioned interleaving technique. With the two characteristics, MMC has been confirmed suitable for HVDC applications and already installed in several links, for example, interconnection Baixas - Santa Llogaia.

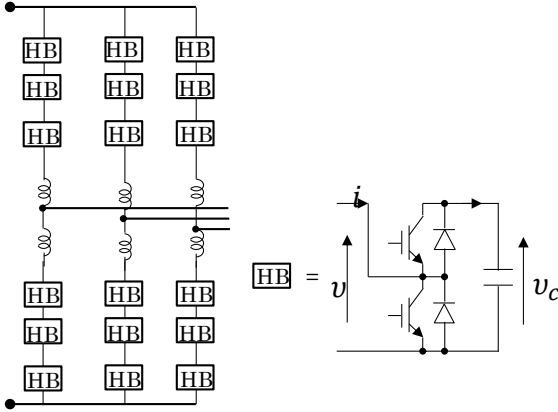


Fig 28. Modular Multilevel Converter

Recently, different submodule topologies are emerged, e.g. Full Bridge (FB) submodule used in Alternative Arm Converter (AAC) (Fig 29).

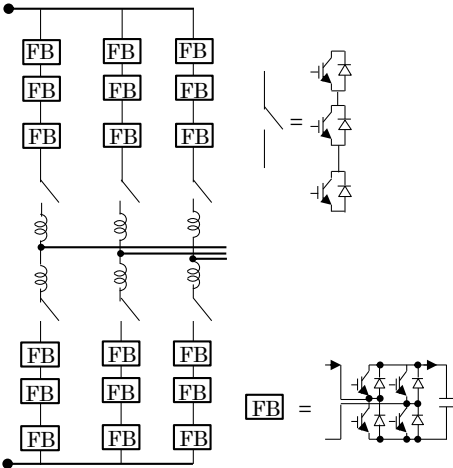


Fig 29. Alternative Arm Converter

Thanks to the reliability and efficiency of the MMC confirmed by numerous projects, DC/DC topologies proposed in the literature are mostly based on the MMC toward the same advantages, e.g. the DC-DC MMC. It is a DC/DC converter which associates directly two MMCs with a transformer in their AC sides as shown in Fig 30.

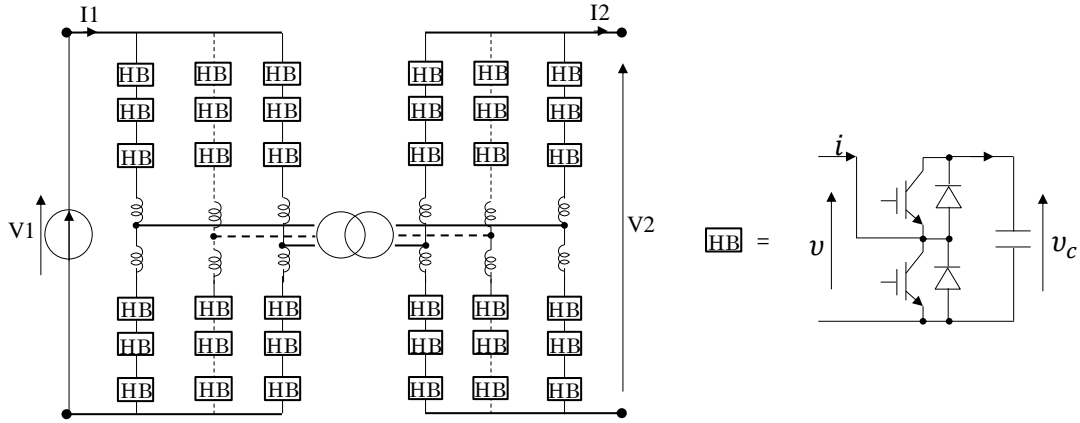


Fig 30. Modular Multilevel DC Converter (DC-DC MMC)

For a DC/DC converter application, two DC sides connect directly to different DC grids and the transformer can isolate current from primary to secondary and help voltage regulation. However, the general hypothesis toward the MMC and transformer is no power dissipation, which implies the two MMCs and the transformer have approximately same power. Regarding the power range of an HVDC grid and the installed MMC volume, the DC-DC MMC could have twice the MMC volume.

In another side, this topology reduces the number of transformers comparing the previous topology with Series connection of DABs. The transformer is an intermediate stage without connections to grid. Thereby, a higher frequency than the grid frequency is possible to reduce the transformer volume. However, losses due to high frequency and volume are always a compromise during the converter design.

Some studies have already been realized on this topology until 2019. For example, [38] studied DC current fault on the converter. [39] proposes a control strategy involving different phase numbers. An overview of the converter losses is shown in [40] and [41]. Then, [42] presents an integration of the converter in MTDC grid to test its dynamic behavior.

The DC-DC MMC is a DC/DC converter with galvanic isolation thanks to the intermediate transformer. However, the transformer is only an option that two MMCs can also be directly connected, as shown in Fig 31.  $L$  represents a small value line inductors. In this case, the DC-DC MMC converter has no galvanic isolation, but benefits of a smaller volume.

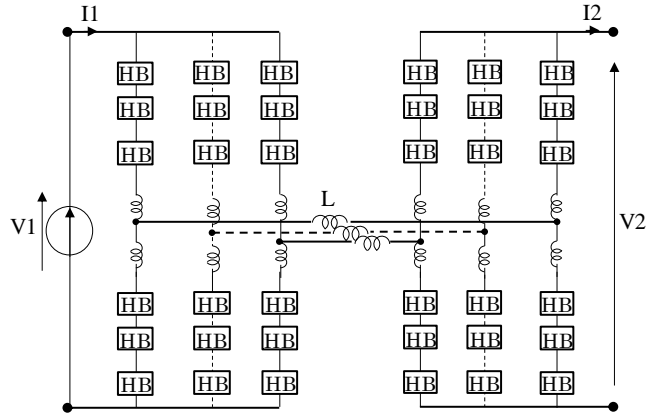


Fig 31. Modular Multilevel DC Converter without transformer (DC-DC MMC)

Otherwise, the AC side of two MMCs can also be replaced by an LCL circuit (Fig 32) to reduce the volume. According to [43], the circuit allows also blocking DC current fault, but eliminates galvanic isolation.

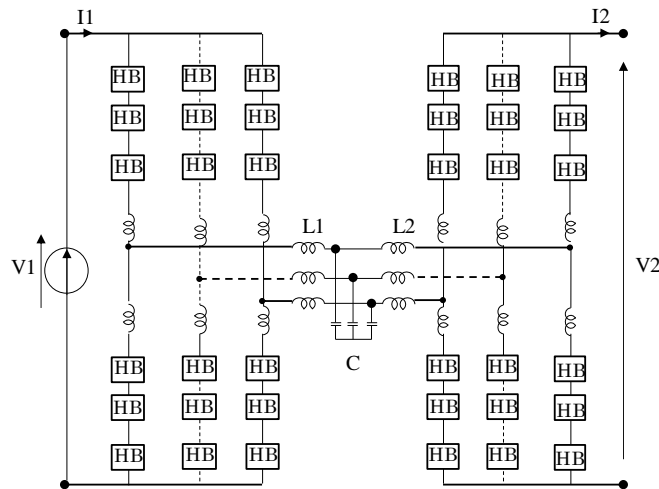


Fig 32. Modular Multilevel DC Converter without transformer (DC-DC MMC)

In any case, these topologies use directly MMC which are currently developed for HVDC DC/AC conversions.

### I.2.2.3 Modular Multilevel DC converter (Autotransformers)

The second possibility to convert an MMC to a DC/DC is based on autotransformers (MMC-AT or HVDC/DC AT) and shown in Fig 33 [45], which is a DC/DC direct conversion converter inspired from autotransformers.

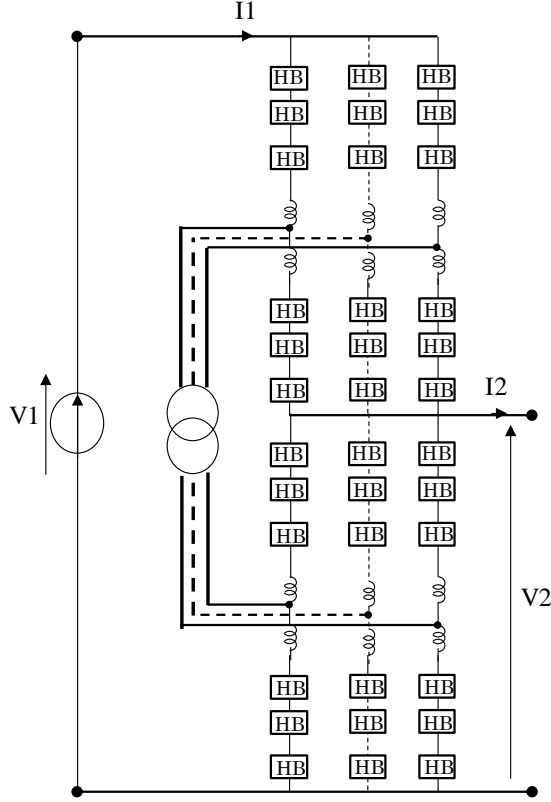


Fig 33. Modular Multilevel DC Converter (Autotransformer 1) [45]

The topology has a series connection of two MMCs, one on the top and another on the bottom. The AC sides of MMCs are always connected by a transformer, but alters to participate in energy balancing instead of galvanic isolation. Compared to the DC-DC MMC, MMC-AT aims to reduce the transformer volume and the number of submodules in MMCs according to [45].

Since the power in the transformer is lower than the grid power (I.2.1) [45], transformer footprint of the MMC-AT is smaller than isolated DC-DC MMC.

$$P_{transformer} = P_{DC} \cdot (1 - \alpha) \quad (I.2.1)$$

where  $P_{transformer}$  indicates power of the transformer.  $P_{DC}$  is the power in DC grid.  $\alpha = V2/V1$  is the DC voltage ratio.  $V1$  and  $V2$  are the two HVDC voltages.

Moreover, the top and bottom MMCs can have different numbers of submodules in terms of different voltage ratios. As a result, these two MMCs will have less submodules than the DC-DC MMC, thereby lower volume.

Another MMC-AT topology proposed in the literature is Fig 34 with monopole symmetrical configuration, which is different from monopole asymmetrical configuration in Fig 33.



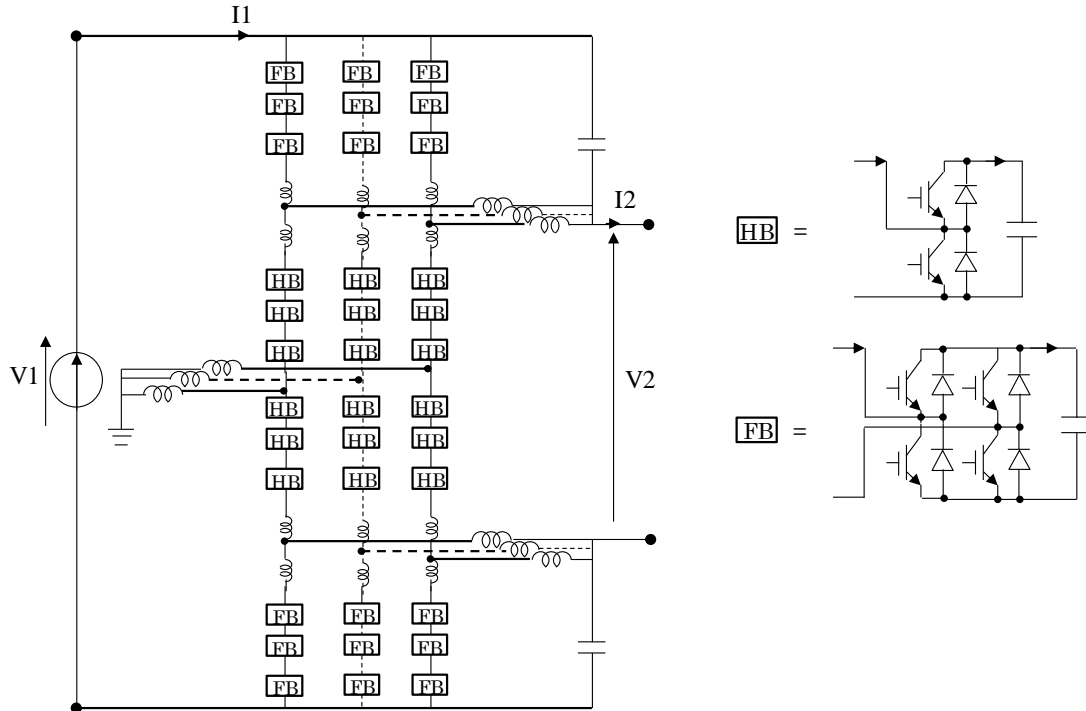


Fig 34. Modular Multilevel DC Converter (Autotransformer 2) [46]

Submodules in the topology are Full Bridge and Half Bridge. The DC voltage is obtained from AC side, thereby output LC filters are mandatory. Thanks to half of Full Bridges utilization, Fig 34 can step down and up a DC voltage without flipping two DC sides that only half bridge cannot afford.

In conclusion, the two topologies of MMC-AT have smaller footprint thanks to their reduced number of submodules and smaller transformer. The transformer is used as power transmission and current filter, thereby lack of galvanic isolation.

Moreover, both converters have DC current fault blocking function from either the internal AC sides or utilization of Full Bridge submodules. With different submodule topologies, MMC-AT could have monopole asymmetrical configuration or monopole symmetrical configuration.

Finally, the phase leg numbers are always an option to raise current range, according to the interleaving technique principle.

Some recent work in 2018 and 2019 about these two topologies [47] , [48] analyzed respectively a multi-frequency operation and DC current fault blocking. In [49], authors proposed a new multiport DC/DC converter (Fig 35).

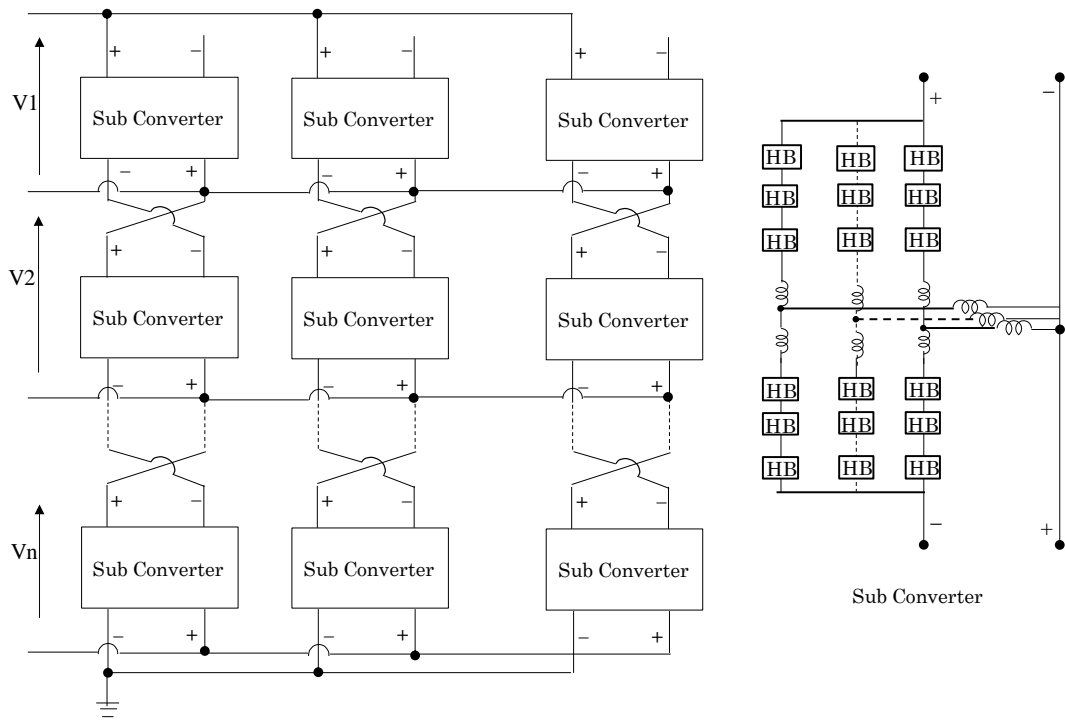


Fig 35. Multiport DC/DC converter [49]

**I.2.2.4 Modular Multilevel DC Converter (Hybrid cascaded DC/DC converter)**

A third DC/DC topology based on MMC is the Hybrid cascaded DC/DC converter shown in Fig 36 [50].

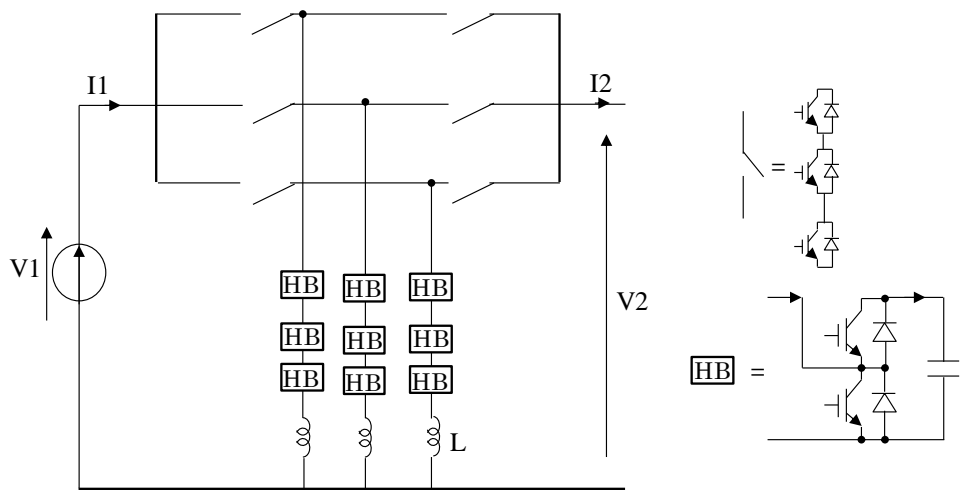


Fig 36. Hybrid cascaded DC/DC converter [50]

This solution is similar to the “Direct series connection of transistors applied in Buck Boost converter”. The principle operation is using inductors to stock energy. However, instead of using single inductors, MMC submodules with capacitors are connected in series with the inductors to provide a zero current and zero voltage switching.

Due to the submodule capacitors, the energy discharge of capacitors could take time to get the desired DC voltage. Thereby, this proposition is considered as a low voltage ratio

DC/DC converter, that two DC sides have similar voltages. Finally, the direct series connection of transistors could make the control complicated to maintain voltage of each transistor.

**I.2.2.5 Modular Multilevel DC Converter (M2DC)**

The last DC/DC topology is Modular Multilevel DC converter (M2DC), which is a direct conversion topology without transformer shown in Fig 37 , more compact than the DC-DC MMC constituted of two MMC connected through their AC side.

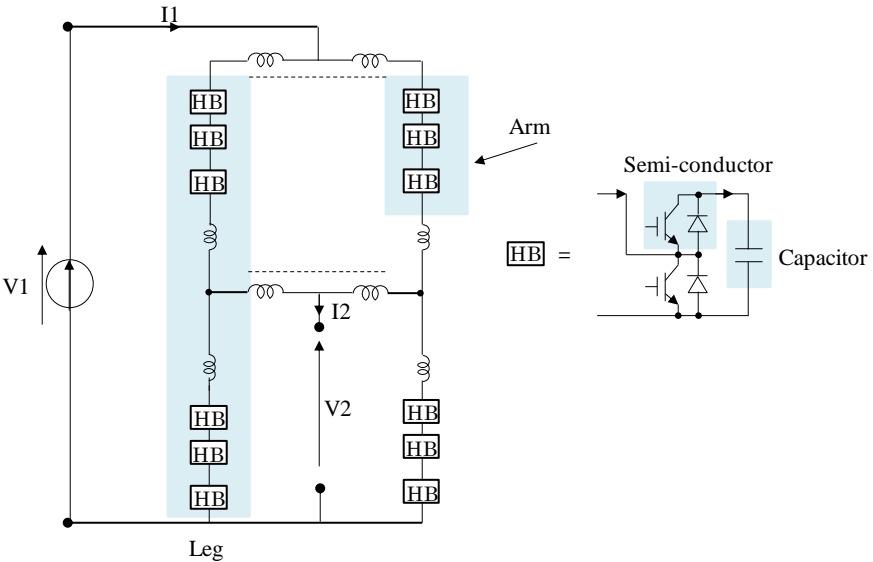


Fig 37. M2DC topology [51]

The topology has four arms, two upper arms and two lower arms. Each arm composed by Half Bridge submodules has the same function as an arm in MMCs, thereby to stock energy in the submodule capacitors. Energy balancing is crucial.

Compared to the MMC-ATs, M2DC eliminates the transformer, then no transformer volume during the converter design. The number of submodules can also be regulated in terms of different voltage ratios. Thereby, the M2DC seems to be the simplest DC/DC topology with most benefits of converter volume.

Some recent work on M2DC are [52], [53] and [56]. In their analysis, methods for converter modelling, design and control are presented. [54], [55] proposed also different methods for DC current fault blocking (Fig 38 and Fig 39) in 2018 and 2019, respectively.

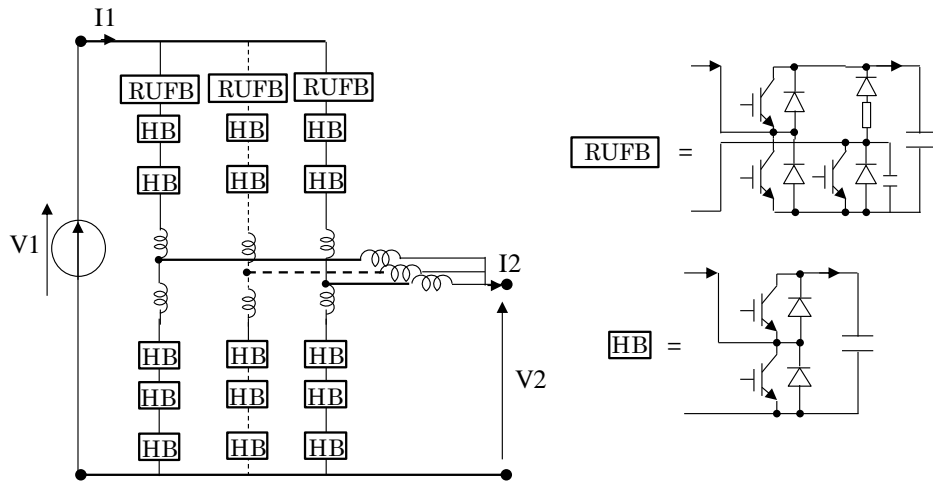


Fig 38. DC fault current blocking structure [54]

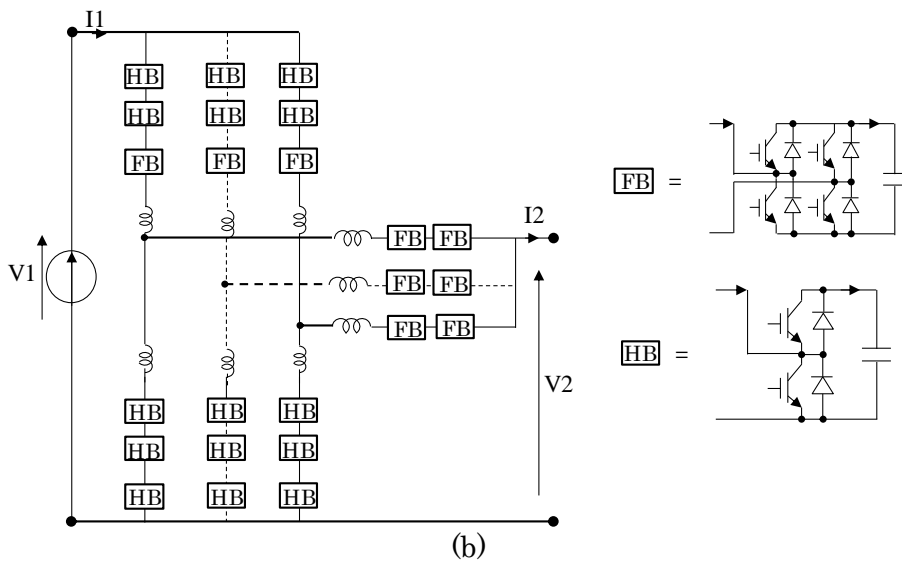


Fig 39. DC fault current blocking structure [55]

### I.3 Conclusion

This chapter reviews four types of HVDC DC/DC converters. Each topology is able to realize a voltage regulation and bi-directional power flow control. Table 2 synthesizes their advantages and disadvantages.

Table 2 Review of existing DC/DC converters

Topologies	Classical DC converters		Modular DC converters	
	Buck/boost	Double buck, three or five levels FC	Series connection of DABs	MMC based
<b>High voltage (&gt;100kV)</b>	No, (Need series connection of transistors)	No, (Need voltage levels extension more than five)	Yes, (Important number of transformers)	Yes
<b>High current (&gt;1kA)</b>	No, (Need interleaving converters)	Yes, (with more than one leg)	Yes	Yes
<b>Modularity</b>	Low	Low	High	High

The first topologies are based on Buck topology. Due to the semiconductor technology, it is mandatory to interleave several Buck converters to raise the current range and connect transistors in series to increase the voltage range. But series connection of transistors has met the difficulty of control and protection of each semiconductor and lack failure management. Thereby, Buck converters are deemed unsuitable in HVDC applications due to their low stand-by voltage.

The second topologies are multilevel converters, increased in voltage range thanks to their multilevel topologies. However, the increased voltage range is still insufficient in HVDC applications due to their low modularity and difficulty of energy balance, thereby these topologies are usually applied in electrical vehicle applications.

The high voltage range obstacle is overcome by series connection of DABs and topologies based on MMC using a high modularity. The series connection of DABs is able to raise the voltage range increasing the number of DAB. Each DAB can have single or three phases in AC side adapting different current range. But transformers are mandatory for each

DAB to avoid short circuit, thereby transformer numbers become important in high voltage applications.

To decrease the number of transformers, four DC/DC topologies based on MMC are presented, DC-DC MMC, MMC-ATs, Hybrid cascaded DC/DC converter and M2DC. They are deemed more suitable for HVDC applications thanks to high modularity and reduced transformer number. Based on the MMC topology, Table 3 shows a qualitative comparison of potential active and passive components necessary in different presented topologies. These table has to be deepened in the future, but gives the trend of our research work.

Table 3 Comparative potential components used in different MMC based DC/DC converters

Topology	Two stage conversion (DC/AC/DC)		Single stage (DC/DC)	
	DC-DC MMC	MMC-ATs	Hybrid Cascaded DC/DC converter	M2DC
Active components	2 × MMC	2 × MMC	N × Half bridge + N × transistors	1 × MMC
Passive components	1 × transformer or 1 × LCL or No passive components	1 × transformer	-	1 × L

As it can be seen, hybrid cascaded DC/DC converter and M2DC seems to need less active components, thereby fewer transistors and lower losses than Dual Active Bridge MMC and MMC-ATs, that both need two MMCs involving more submodules and losses. However, due to the series connection of transistors, Hybrid cascaded DC/DC converter is less feasible and lower modularity than the M2DC. As the results, the M2DC has been selected as the central research in order to confirm the trend given in Table 3.

Some studies on the M2DC have already been realized. However, this report aims to clarify basic operation principles and limitations of the M2DC converter. The analysis will show the differences between MMC and M2DC control. Its control principle will be presented and validated in the following chapters. Firstly, the second chapter will theoretically explain the principle operation and limitation of the topology. Then, the third chapter will show a basic control to validate the theory explored in the second chapter.

The HIL validation will be shown in the fourth chapter, which will involve the validation methodology and a MMC based design.

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# II DC-DC Modular Multilevel Converter (M2DC)

## II.1 Introduction

The DC-DC Modular Multilevel Converter (M2DC) is a DC/DC converter based on the Modular Multilevel Converter topology which is able to achieve high power and high voltage conversion. Series connection of submodules is the key feature of the M2DC. It is effectively possible to change its voltage level by increasing the numbers of submodules. The main difference of the M2DC converter amid MMC variations is its direct DC/DC voltage conversion. M2DC converter is therefore equivalent to a DC transformer and is proposed for High Voltage Direct Current (HVDC) grids.

The purpose of this chapter is to explain the M2DC converter topology and its operating principle. The chapter starts with a general analysis of the converter architecture. During the analysis, the author shows also the possibility of using two different topologies of submodules (half bridge or full bridge). After the discussion on the different submodule topologies, the converter operating principle and its design are focused on the half-bridge submodule topology. Using half-bridge submodule, investigations on the operating principle are described.

The first part establishes a specific M2DC average arm model useful for its simplified study. This arm model allows us to identify the global behavior of the converter in steady state by omitting the high switching frequency of semiconductors.

Then the investigation of the global behavior is realized by a discussion on why and how to balance capacitor energies of submodules. Capacitor energy balancing is an issue for the MMC family converter. With the balancing capacitor energy method, the leg model illustrates the operating principle of the converter, which is helpful to obtain the characteristics of the converter and its electrical constraints. These constraints reveal the converter capability used for the converter design.

Finally, the end of the chapter shows the inductance and capacitance design made possible by the analysis of the converter.

## II.2 Topology of the DC-DC Modular Multilevel Converter

The electrical circuit of the DC-DC Modular Multilevel Converter (M2DC) is drawn in Fig 40. In the original proposition [57], the author uses coupled inductors to reduce inductors volume. Mutual inductance occurs when magnetic flux created by an inductor go through another inductor nearby. With the aim of comprehension of the converter operating principle, mutual inductances are not desirable due to the difficulties of the analysis. Therefore, the electrical circuit drawn in Fig 40 replaces the coupled inductors by simple inductors. These inductors have their self-inductances ( $l$  for arm inductance,  $L_s$

for secondary inductance) and their parasitic resistance ( $r$  for arm inductor,  $R_s$  for secondary inductor) which simulate the inductance losses.

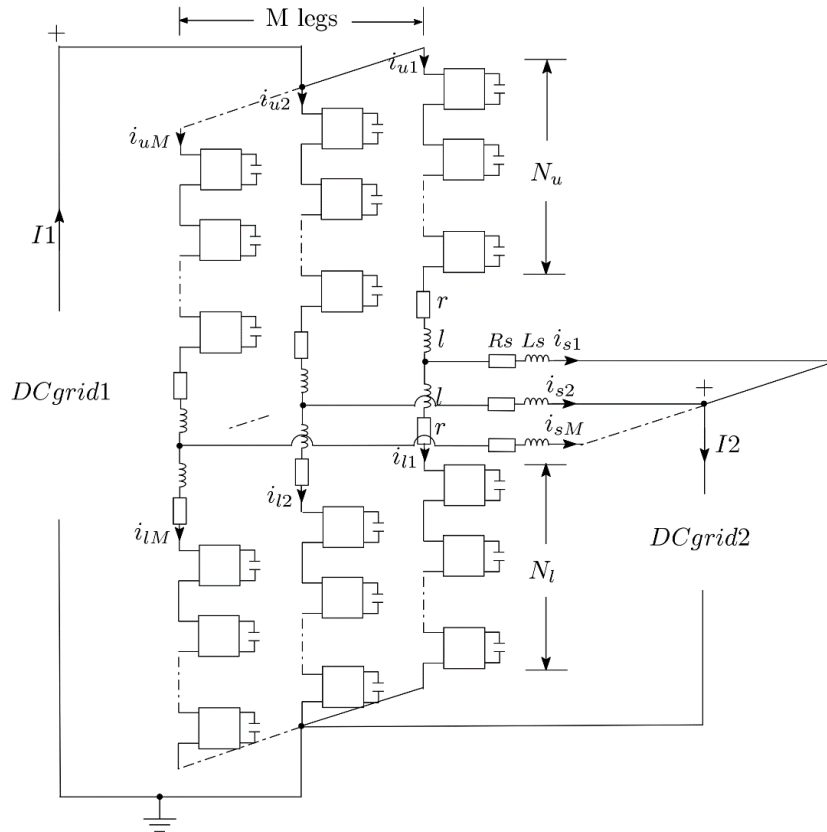


Fig 40. The electrical circuit of the M2DC converter

The M2DC converter has  $M$  symmetric legs with the same components and the same number of submodules for each leg. However,  $M = 2$  is the minimal configuration to obtain the DC/DC conversion in order to naturally filter AC components on DC sides. This principle will be detailed later. Then, the interest of extending the leg number  $M$  (where  $M > 2$ ) is only to increase the power transmission capability of the converter. For the continuity of analysis, the study focusses on the behavior of one leg (Fig 41. (a)).

One leg of the converter consists of two arms, the upper one and the lower one. Each arm is a string of submodules connected to an arm inductor  $l$  represented by a  $l$ - $r$  circuit, where  $r$  represents the inductor losses. The scope of arms inductors is to support instantaneously different voltages between high DC voltage  $V_1$  and the sum of the two arms voltages. Arms inductors play also an important role to limit gradient of current in case of DC fault occurred in DC grid, which will be taken into account in designing the arm inductance  $l$  of the M2DC converter at the end of the chapter.

A string of submodules is a sequence of submodules in series. Each submodule (SM) can use a half-bridge converter (Fig 41. (b)) or a full bridge converter (Fig 41. (c)). Each submodule has a capacitor to store energy and maintain the submodule voltage. Charge and discharge of the capacitor energy are realized by switching semiconductors (e.g. MOSFETs, IGBTs) regarding on arms currents direction and submodule voltage control.

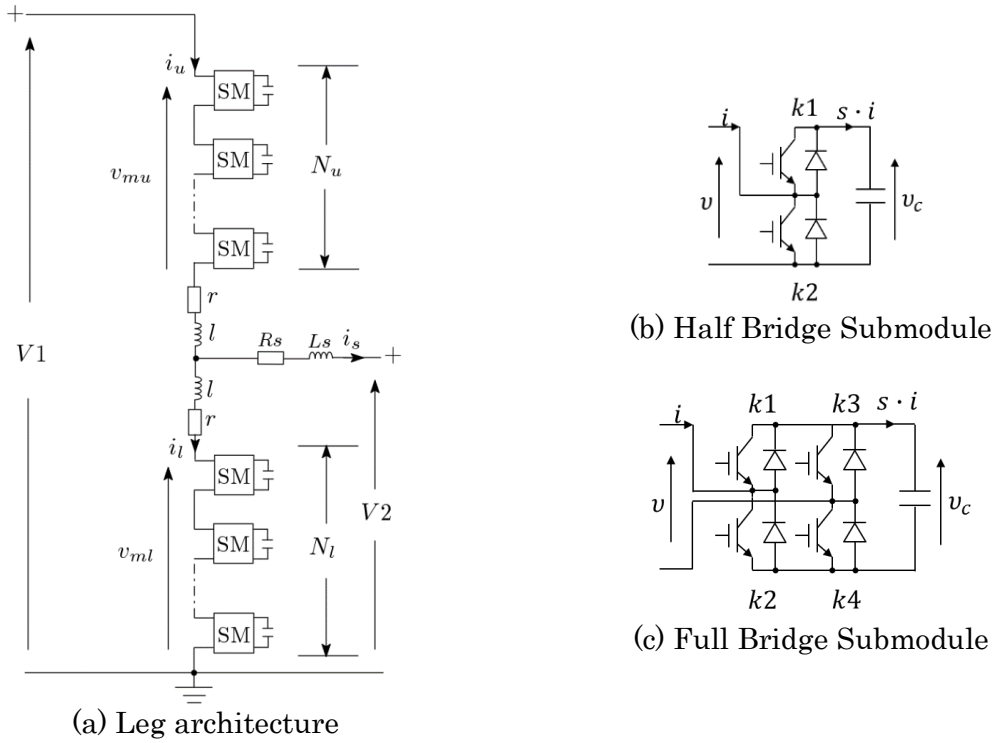


Fig 41. M2DC leg and its submodules

Submodules connected in series make the converter leg step-up or step-down the DC grids voltages according to submodule topologies. With half-bridge submodules, the converter leg step-down DC voltage. Regarding the architecture of the converter leg (Fig 41. (a)),  $V1$  has necessarily a higher value than  $V2$ .

To step up a DC voltage, there are two possibilities. One possibility is to turn over the two DC sides of the half-bridge M2DC. The other is using full-bridge submodules, which accepts negative voltage. If an arm voltage ( $v_{mu}, v_{ml}$ ) is negative, the sum of two arms voltages can be lower than the voltage of a single arm, which is not possible when the leg is constituted by half-bridge submodules. Then in Fig 41. (a), the voltage  $V1$  of the converter leg can be lower than the  $V2$  voltage with full-bridge submodules.

Another possibility exist to step up a DC voltage. Turning over two DC sides of the half-bridge M2DC is simpler and more reliable than using full-bridge submodules. For future HVDC applications, voltage ratio  $V2/V1$  will be quasi-fixed (with a certain tolerance) which allows to simplify the choice of input and output of the M2DC converter. Moreover, a half-bridge submodule has less losses than a full bridge submodule. Therefore, the objective of this work is a study of the operation principle of the half-bridge submodule.

Notably, analysis afterwards does not take into account full-bridge submodules. Therefore, DC grid fault and prevention of the M2DC will not be studied, because the full bridge submodules are necessary.

Another difference between the M2DC topology and the MMC is due to the fact that M2DC converter leg can have an asymmetric topology. It is possible to have different numbers of submodules in the upper and the lower arms of an M2DC. As presented in Fig 41. (a),  $N_u$  is noted as the number of submodules of upper arm ( $N_l$  for the lower arm). These numbers of submodules are selected depending on two sides DC voltage values  $V1$

and  $V_2$ . The two arms can have different DC voltages, then, different numbers of submodules in the upper and lower arm. However, it is always possible to use the same number of submodules for upper arms and lower arms regardless of DC voltage values. In the last case, one of the two arms should be oversized.

### II.3 Submodule topologies

This section presents the two submodule topologies (half-bridge and full bridge) and their differences.

#### II.3.1 Half Bridge Submodule

A half bridge submodule (Fig 41. (b)) has two complementary semi-conductors switching the output voltage  $v$  between 0 and  $v_c$ . Therefore, there are two switching states.

- One is called the “insert” state. In this state, arm current go through the capacitor charging or discharging energy. The output voltage  $v$  of the submodule is the voltage of the capacitor  $v_c$ .
- The other one is the “bypass” state. The capacitor of the submodule is isolated from arm current and maintain its capacitor voltage. Voltage and current of the submodule can be defined as eq. (II.3.1) [59].

$$\begin{aligned} v &= s \cdot v_c \\ s \cdot i &= C \cdot \frac{dv_c}{dt} \end{aligned} \tag{II.3.1}$$

where  $s$  is the switching state of  $k_1$ . Its value can be 1 or 0, to indicate respectively turn-on or turn-off of switch  $k_1$ . The switch  $k_2$  takes all over the opposite state ( $\bar{s}$ ) of the switch  $k_1$ .

When  $k_1$  is turned on ( $s = 1$ ) and  $k_2$  is turned off, the capacitor  $C$  is inserted. The voltage of the submodule  $v$  is equal to the voltage of the capacitor  $v_c$ . The current  $i$  goes through the capacitor. When  $k_1$  is turned off ( $s = 0$ ) and  $k_2$  is turned on, the capacitor  $C$  is bypassed. The current of the capacitor is zero. The voltage across the capacitor is maintained. Table 1 shows the voltage and current of a half bridge submodule.

Table 4 Output voltage and current of Half-Bridge Submodule

	$s = 0$	$s = 1$
$v$	0	$v_c$
$C \cdot \frac{dv_c}{dt}$	0	$i$

The series connection of modules (Fig 42) allows easily extending an arm voltage of the converter. The arm voltage  $v_m$  is the sum of submodules voltages at “insert” state. This modularity has made the success of MMC converters for HVDC applications, which is also

expected for the M2DC. The value of the arm voltage depends on the number of submodules in the “insert” state.

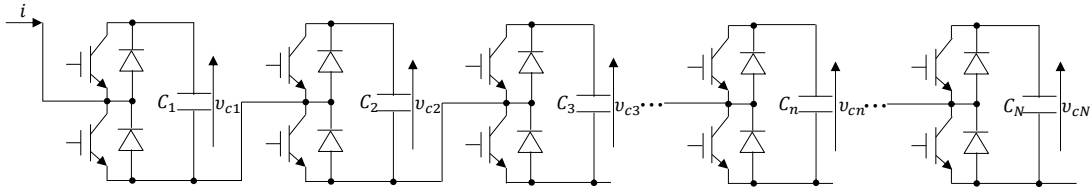


Fig 42. A string of Half-Bridge Submodules

Eq. (II.3.2) describes the “arm voltage”  $v_m$  of a string of submodules as shown in Fig 42 in terms of capacitors voltages  $v_{cx}$ .

$$v_m = \sum_{x=0}^n v_{cx} \quad (\text{II.3.2})$$

where  $n \in [0, N]$  is the number of inserted submodules.  $N$  is the total number of submodules in a string.

If no capacitor is inserted in an arm,  $v_m$  is equal to zero. On the contrary, with  $N$  submodules inserted ( $N$  is the total number of submodules in a string), the voltage is maximum:  $\sum_{x=0}^N v_{cx}$ . As a result, a string of  $N$  half bridge submodules can take a value between zero and  $\sum_{x=0}^N v_{cx}$ . When the leg is in operation, the average voltage value of a half bridge submodules string is consequently positive, as shown in Fig 43.

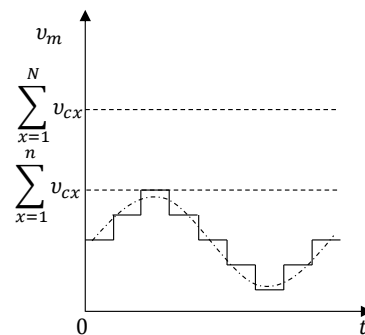


Fig 43. Arm voltage  $v_m$  with a string of Half Bridge Submodules: voltage levels

The number of voltage levels depends on the number of inserted submodules. If the number of submodules is large enough, the voltage of a submodule string  $v_m$  can approach to a pure sine wave, as shown by the dash-dotted line of Fig 43. If the reference voltage of the arm is sinusoidal, increasing the submodules number reduces therefore the harmonic contents in the voltage. At the same time, it increases the complexity of the solution.



### II.3.2 Full-Bridge Submodule

A full-bridge submodule (Fig 41. (c)) consists of two half-bridges and a capacitor. The output voltage of the submodule is carried out with the middle potentials of two half bridges. Unlike the half-bridge, the polarity of a full-bridge output voltage alternates thanks to the switches complementarily controlled, as shown by eq. (II.3.3).

$$\begin{aligned} v &= (s1 - s2) \cdot v_c \\ (s1 - s2) \cdot i &= C \frac{dv_c}{dt} \end{aligned} \quad (\text{II.3.3})$$

where  $s1$  is the switching state of  $k1$ . Its value is 0 or 1 to indicate the turn-off or the turn-on state. The switch  $k2$  has an opposite state ( $\overline{s1}$ ) to  $k1$ . In the same way,  $s2$  is the switching state of  $k3$ .  $k4$  has an opposite state ( $\overline{s2}$ ) to  $k3$ .

Table 5 explains the operating principle of a full-bridge [60]. When  $k1$  and  $k4$  are turned on ( $s1 = 1, s2 = 0$ ), the capacitor  $C$  is inserted and the output voltage of submodule is  $v_c$ . When  $k2$  and  $k3$  are turned on ( $s1 = 0, s2 = 1$ ), the capacitor  $C$  is inserted and the output voltage of submodule  $-v_c$ . The third situation is when  $k1$  and  $k3$  are turned on (or  $k2$  and  $k4$ ), the capacitor is bypassed.

Table 5 Output voltage and current of Full-Bridge Submodule

	$s1 = 1, s2 = 0$	$s1 = 0, s2 = 1$	$s1 = 1, s2 = 1$	$s1 = 0, s2 = 0$
$v$	$v_c$	$-v_c$	0	0
$C \frac{dv_c}{dt}$	$i$	$-i$	0	0

As with half bridge submodules, an arm as a string of full-bridge submodules, needs also to increase its number of submodules to extend its voltage level (Fig 44).

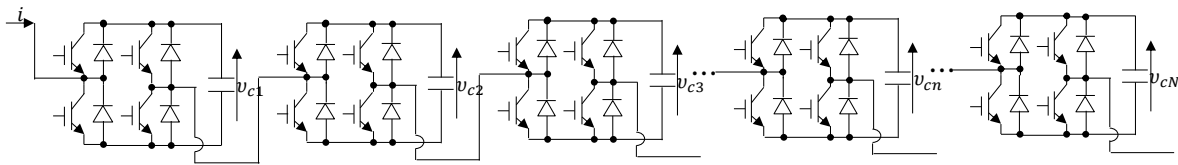


Fig 44. String of Full-Bridge Submodules

Summing voltages of active submodules, the voltage of a string of full-bridge submodules is done by (II.3.4).

$$v_m = \sum_{x=0}^{n^+} v_{cx} + \sum_{y=0}^{n^-} (-v_{cy}) \quad (\text{II.3.4})$$

where  $n^+ \in [0, N]$  is the number of submodules inserted with a submodule voltage of  $v_c$ .  $n^- \in [0, N - n^+]$  is the number of submodules inserted with a submodule voltage of  $-v_c$ .  $N$  is the total number of submodules in a string.

Depending on the number of active submodules, two extreme cases mark the boundaries of voltages of a full-bridge submodules string. When all submodules are inserted with a submodule voltage  $v_c$ , the arm voltage of a submodules string  $v_m$  reach the maximum positive value  $\sum_{x=0}^N v_{cx}$ . When all submodules are inserted with a submodule voltage  $-v_c$ , the arm voltage of a string has the minimum negative value  $\sum_{y=0}^N (-v_{cy})$ . A string of full bridge submodules provides, therefore, all voltage levels between  $\sum_{x=0}^N v_{cx}$  and  $\sum_{y=0}^N (-v_{cy})$ . Its average value can be positive, zero or negative with different switch combinations as shown in Fig 45 in solid line. The dash dotted line shows the voltage of a string of submodules when the number of submodules is large enough and can reach its sinusoidal reference.

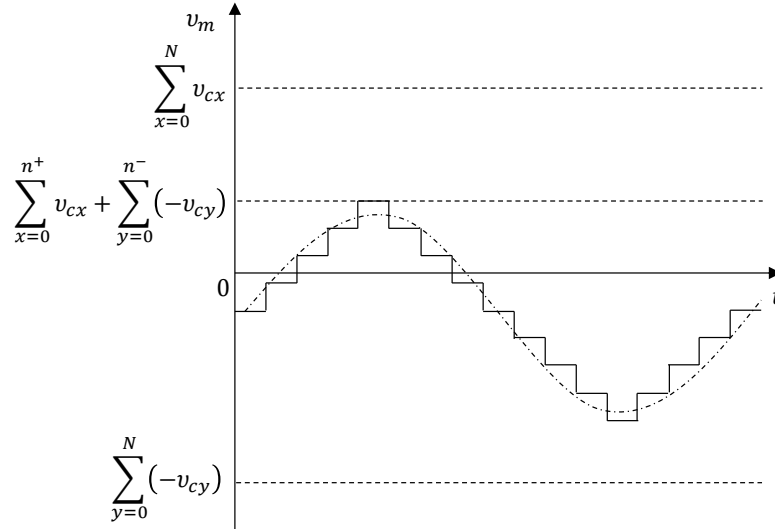


Fig 45. Arm voltage  $v_m$  with a string of Full-Bridge Submodules: voltage levels

## II.4 Average model of a string of submodules

Different submodule topologies make the converter more flexible and with more capabilities. However, this section discusses an average model of a string of submodule based on half bridge submodule, which is the topology studied in this work. This model is also the average model of an arm of M2DC.

An average model describes the global behavior of an element without taking into account the states of each submodule at each moment. For an arm of the M2DC which has a huge number of semiconductors, the average model simplifies the analysis by neglecting the voltages ripples and the interactions of semiconductors.

Due to the high voltage of an HVDC grid, a large number of submodules is generally required, which determines directly the submodule voltage and the levels number of an

arm. The number of voltage levels is, therefore, high enough to allow the discretized voltage signal be approached by a continuous voltage signal. This model concerns the global behavior of the converter where the high switching frequency behavior of the arm is ignored. Therefore, neglecting the high order harmonics caused by the switching frequency is a condition for establishing the average model of an arm.

To build this average model, a necessary assumption is that an algorithm balances perfectly the submodule capacitors voltages. All capacitors are then supposed to have the same voltage (II.4.1). This assumption is assured by an algorithm, which is the “Nearest Level Control” algorithm [62]-[64] studied and used in a lot of academic research as well as industrial projects.

$$v_{c1} = v_{c2} = v_{c3} = \dots = v_{cN} = v_c \quad (\text{II.4.1})$$

#### II.4.1 Voltage relations for a string of submodules

Since the capacitor voltage of submodules have the same value, the sum of all capacitors voltages of an arm called  $v_{ctot}$  is proportional to the capacitor voltage of one submodule  $v_c$  (II.4.2):

$$v_{ctot} = v_{c1} + v_{c2} + v_{c3} + \dots + v_{cN} = N \cdot v_c \quad (\text{II.4.2})$$

where  $N$  is the number of submodules of an arm. It can be replaced by  $N_u$  to indicate the number of submodules of the upper arm or  $N_l$  to indicate the number of submodules of the lower arm.

Arm voltage  $v_m$  (II.3.2) is the voltage of a string of submodules (II.4.3) as a part of the maximal voltage  $v_{ctot}$ .

$$v_m = n \cdot v_c \quad (\text{II.4.3})$$

where  $n$  is the number of inserted submodules.  $n_u$  and  $n_l$  designate respectively the number of inserted submodules of the upper arm or lower arm.

Comparing the two voltages  $v_m$  and  $v_{ctot}$ , their difference comes from the inserted number of submodules ( $n$ ) and the number of submodules of an arm ( $N$ ).

$$\frac{v_m}{v_{ctot}} = \frac{n}{N} \quad (\text{II.4.4})$$

By (II.4.4), a string of submodules can be considered as a voltage source. The voltage of the source  $v_m$  follows the ratio  $n/N$ . This ratio is called modulation arm index  $m$  (II.4.5). Regarding half-bridge submodules,  $m$  is ranged from 0 to 1.

$$m = \frac{n}{N} \quad (\text{II.4.5})$$

The arm voltage  $v_m$  is, therefore, a voltage source controlled by a modulation index  $m$  (II.4.6).

$$v_m = m \cdot v_{ctot} \quad (\text{II.4.6})$$

#### II.4.2 Current relations of a submodule string

Deriving each term of the relation (II.4.2) of time  $t$  and multiplying by capacitance value  $C$  yields:

$$C \frac{dv_{ctot}}{dt} = C \frac{dv_{c1}}{dt} + C \frac{dv_{c2}}{dt} + C \frac{dv_{c3}}{dt} + \dots + C \frac{dv_{cN}}{dt} \quad (\text{II.4.7})$$

Since submodules are connected in series, arm current  $i$  is the current flowing through the inserted capacitors, on the contrary of bypassed capacitors. The right side of equation (II.4.7) explains, therefore, an addition of currents of  $n$  inserted submodules in (II.4.8).

$$C \frac{dv_{ctot}}{dt} = n \cdot i \quad (\text{II.4.8})$$

Dividing this expression (II.4.8) by  $N$  (submodules number of an arm):

$$\frac{C}{N} \cdot \frac{dv_{ctot}}{dt} = \frac{n}{N} \cdot i \quad (\text{II.4.9})$$

The left side of (II.4.9) explains a current of an equivalent capacitor  $C/N$  charged to the voltage  $v_{ctot}$ . This current named  $i_m$  in Fig 46.(b) has the expression of (II.4.10).

$$i_m = \frac{C}{N} \cdot \frac{dv_{ctot}}{dt} \quad (\text{II.4.10})$$

The equivalent capacitor with the value of  $C/N$  is named  $C_{tot}$  (II.4.11).

$$C_{tot} = \frac{C}{N} \quad (\text{II.4.11})$$

Notably, the equivalent capacitor  $C_{tot}$  is not a series connection of submodule capacitors. Its value is independent from time  $t$  and numbers of submodules active  $n$ . A series connection of capacitors causes a capacitance value variable in terms of time  $t$  and numbers of submodules active  $n$ .

(II.4.9) illustrates also the relation between the current  $i_m$  and the current  $i$ . It can be, therefore, rewritten in (II.4.12).

$$i_m = m \cdot i \quad (\text{II.4.12})$$

Combining the voltage relation (II.4.6) and the current relation (II.4.12), the average arm model of a string of submodules Fig 46.(b) describes Fig 46.(a) with a new variable  $m$ .



Fig 46. (a) String of submodules, (b) Arm average model

Following this model, the average model of the converter leg is described in Fig 47.

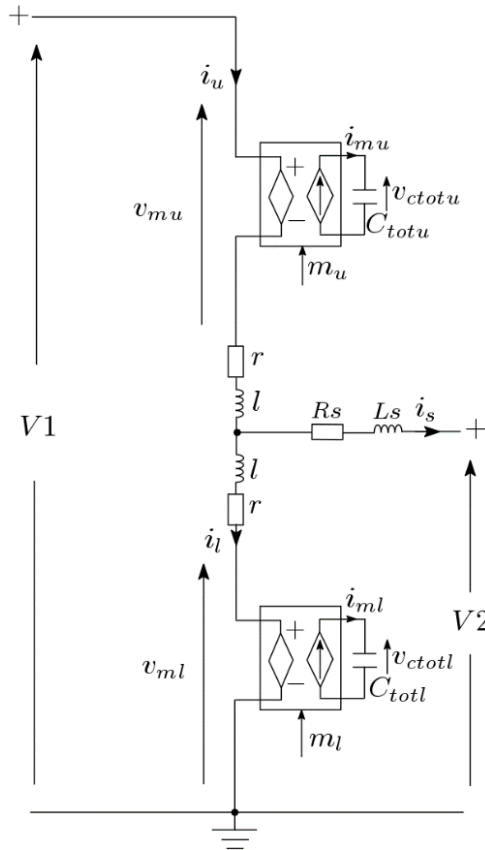


Fig 47. Leg average model

### II.4.3 Energy relations of a string of submodules

Balancing energy is an issue for converters with floating capacitors to assure its safety and the defined conversion same as the M2DC. To find the energy model of the M2DC, some definitions are shown at first.

For a string of submodules modeled by its average model, energy definition is (II.4.13).

$$W_C = \frac{1}{2} \cdot C_{tot} \cdot v_{ctot}^2 \quad (\text{II.4.13})$$

Capacitor power is then found by taking the time derivative of the energy.

$$\frac{dW_C}{dt} = C_{tot} \cdot v_{ctot} \cdot \frac{dv_{ctot}}{dt} \quad (\text{II.4.14})$$

As discussed above, the equivalent capacitor  $C_{tot}$  and total voltage of capacitors  $v_{ctot}$  correspond to a number of submodules  $N$  in each arm. Using different numbers of submodules in upper and lower arms make equivalent capacitances different between the upper arm  $C_{totu}$  and lower arm  $C_{totl}$  (II.4.15). Also, the differences make total arm voltage different as explained by  $v_{ctotu}$ ,  $v_{ctotl}$  in (II.4.16).

$$C_{totu} = \frac{C}{N_u} \quad (\text{II.4.15})$$

$$C_{totl} = \frac{C}{N_l}$$

$$v_{ctotu} = N_u \cdot v_c \quad (\text{II.4.16})$$

$$v_{ctotl} = N_l \cdot v_c$$

where  $N_u$ ,  $N_l$  are submodule number of upper arms and lower arms, respectively.  $C_{totu}$ ,  $C_{totl}$  are equivalent capacitances of the upper arm and lower arm, respectively.  $v_{ctotu}$  and  $v_{ctotl}$  are total capacitors voltages in upper and lower arms, respectively.

At the same time, the capacitor energy of the upper arm and lower arm are different and proportional to their submodule number  $N_u$ ,  $N_l$  (II.4.17).

$$W_{CU} = \frac{1}{2} \cdot C \cdot N_u \cdot v_c^2 \quad (\text{II.4.17})$$

$$W_{CL} = \frac{1}{2} \cdot C \cdot N_l \cdot v_c^2$$

## II.5 Steady state analysis

Regarding the average model of a string of submodules, the energy study is a fundamental aspect of the M2DC converter leg. As the classical Modular Multilevel Converter (MMC) topology, balancing capacitor energy in a pure DC condition is impossible for the M2DC converter.

For this reason, this section resolves firstly the issue of balancing capacitor energy by static analysis. The solution different from the MMC one is used for investigating the

converter leg operating principle afterwards, which includes voltages, currents, and power analysis.

An assumption kept all along this section is that the converter losses are ignored. Also, energy is conserved. The input power is either transferred to the output or stored in arms.

### II.5.1 Static analysis of an M2DC leg

Before studying the converter's behavior, some definitions make the analysis easier and more readable. The voltage ratio  $\alpha$  is defined as the ratio between the two DC voltages  $V1$  and  $V2$  in (II.5.1). Using half bridge submodule, the converter steps down DC voltage. The voltage of  $V2$  side is lower than the voltage of  $V1$  side. The range of  $\alpha$  is  $\alpha \in [0,1]$ .

$$\alpha = \frac{V2}{V1} \quad (II.5.1)$$

Ignoring the converter losses, power  $P1$  of  $V1$  side is equal to the power  $P2$  of  $V2$  side when the average energy of leg is controlled. Then, DC currents of both sides of the converter have the relation (II.5.2).

$$I1 = \alpha \cdot I2 \quad (II.5.2)$$

where  $I1$  and  $I2$  are currents at  $V1$  side and  $V2$  side respectively.

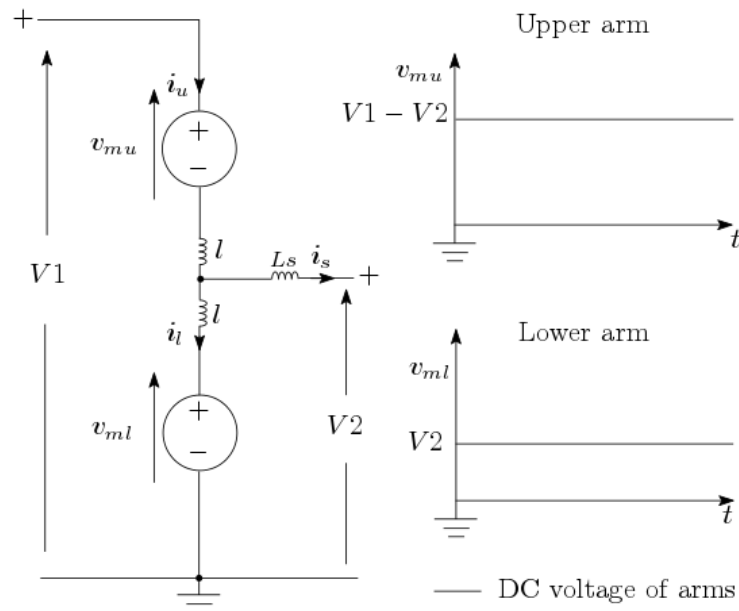


Fig 48. Equivalent leg circuit with DC arm voltages

DC grids provide DC voltages in the converter leg, which create DC components of currents. These arms voltages supplied in DC cannot stabilize capacitor voltages. Considering only DC voltages in the converter leg, the average model of the leg becomes

as shown in Fig 48, where  $V1$  is the high DC voltage and  $V2$  is the low DC voltage.  $i_u$  is the current of the upper arm.  $i_s$  is the output current in the middle branch.

Regarding the leg topology,  $i_u$  as the current of the upper arm is also the current of high voltage side  $I1$ .  $i_s$  as the current of the middle branch is the current of low voltage side  $I2$ . Their difference is  $i_l$ , the lower arm current.

$$\begin{aligned} i_u &= I1 \\ i_s &= I2 \\ i_l &= I1 - I2 \end{aligned} \tag{II.5.3}$$

The DC voltage of the lower arm  $v_{ml}$  is  $V2$ , as inductor  $Ls$  voltage is null in steady state. The upper arm takes the voltage difference between the two DC grids (II.5.4). So, for the DC voltage components, we have:

$$\begin{aligned} v_{mu} &= (1 - \alpha) \cdot V1 \\ v_{ml} &= \alpha \cdot V1 \end{aligned} \tag{II.5.4}$$

Instantaneous powers of the upper arm  $p_{u,DC}$  and lower arm  $p_{l,DC}$  (II.5.5) are found by multiplying voltage and current. Then,  $P_{u,DC}$  and  $P_{l,DC}$  are average arm powers during a period of operation.

$$\begin{aligned} P_{u,DC} &= \langle p_{u,DC}(t) \rangle = \langle (1 - \alpha) \cdot P1 \rangle \\ P_{l,DC} &= \langle p_{l,DC}(t) \rangle = \langle (\alpha - 1) \cdot P1 \rangle \end{aligned} \tag{II.5.5}$$

Both average powers have the same value with a different sign (II.5.6). In other words, an arm generates the power and the other arm absorbs it.

$$P_{u,DC} = -P_{l,DC} \tag{II.5.6}$$

For a DC converter, the main objective is to have DC voltage  $V1 \neq V2$ . Then, the voltage ratio  $\alpha$  is different from 1. For any voltage ratio different from 1, the average power  $P_{u,DC}$  and  $P_{l,DC}$  are different from 0 depending on (II.5.5). This issue causes the energy variation of both arms.

The solution suggested in this section is to introduce an AC component in each arm. These AC components produce the active power  $P_{u,AC}$  and  $P_{l,AC}$  to compensate the active power of arms due to DC components of voltages defined earlier,  $P_{u,DC}$  and  $P_{l,DC}$  (II.5.7).

$$\begin{aligned} P_{u,AC} &= -P_{u,DC} \\ P_{l,AC} &= -P_{l,DC} \end{aligned} \tag{II.5.7}$$

The introduction of AC components has many possibilities regarding its frequency. More frequencies implicate in signals, more complicated will be the control. To simplify



the study, this work uses a single frequency, as shown in Fig 49. The operating principle of a converter leg is analyzed based on a DC component and a sinusoidal AC component in an arm.

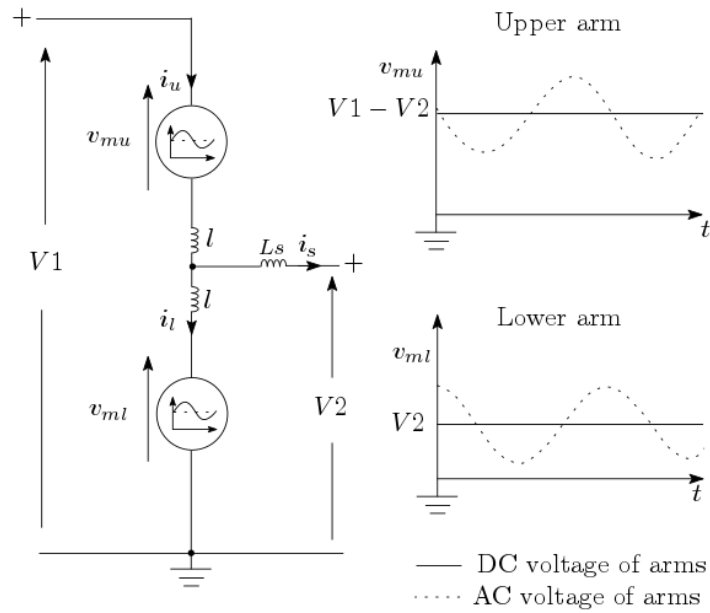


Fig 49. Equivalent leg circuit with DC and AC voltages

AC components have to create power in opposition to the power of DC components in each arm. Therefore, AC average power  $P_{u,AC}$ ,  $P_{l,AC}$  and DC average power  $P_{u,DC}$ ,  $P_{l,DC}$  should be the same. Fig 50 explains  $P_{u,AC}$ ,  $P_{l,AC}$  in terms of voltage ratio  $\alpha$  and rated power  $P1$ . When the voltage ratio  $\alpha$  is zero, the converter leg needs maximum power from AC components, that the value should be  $P1$ . AC average power decrease when ratio  $\alpha$  increases if  $P1$  is constant.

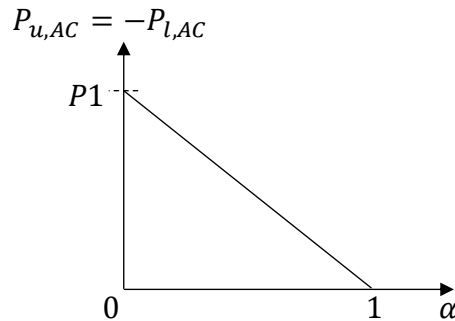


Fig 50.  $|P_{u,AC}|$  and  $|P_{l,AC}|$  with a transmitted power  $P1$

### II.5.2 DC buses currents

With the integration of AC components, AC currents are present in each branch of the converter leg. To suppress AC currents in DC buses, it is necessary to multiply the number of legs in parallel. Each AC leg current is shifted of  $2\pi/M$  rad, where  $M$  is the number of legs.

The average model of a multi-leg M2DC converter is finally drawn in Fig 51. The configuration is similar to the MMC converter [69].

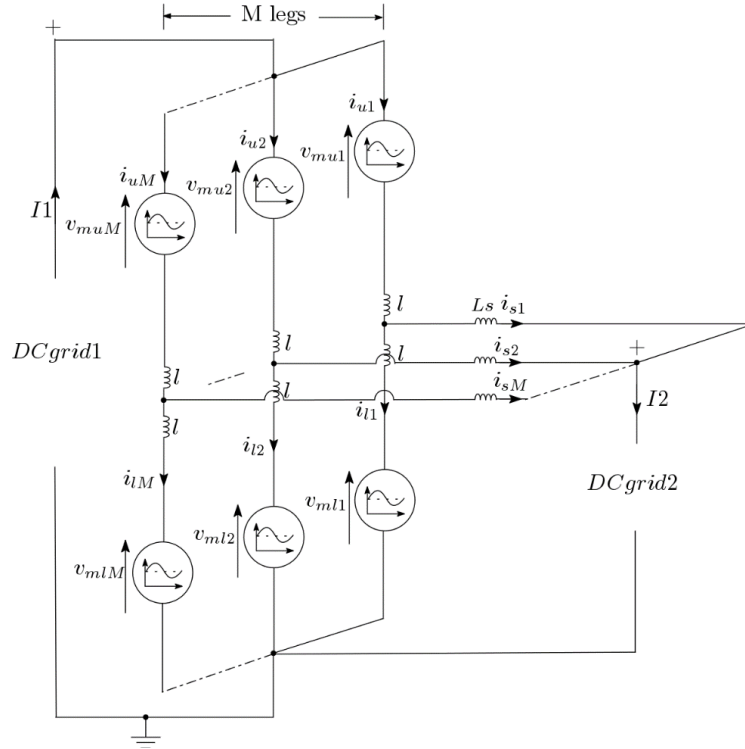


Fig 51. Average model of the M2DC converter

Leg number  $M$  does not have a theoretical limit. For a rating power, more legs are inserted in the converter, less currents (or power) flow through each leg. This is convenient for semi-conductor rating in terms of current. But increasing the leg number involves more material and components. An economic and efficient compromise has to be taken into account during the design process to choose the right number  $M$  according to converter constraints.

Regarding the converter structure,  $M$  upper arms are connected at the positive pole, whereas  $M$  lower arms at the ground. The sum of the upper arms currents must be equal to the DC bus current  $I1$ .

$$\sum_{x=1}^M i_u^x = I1 \quad (\text{II.5.8})$$

The middle point of the branches are connected to the second DC bus positive pole. The sum of currents in the middle branches is required to be equal to DC bus current  $I2$ .

$$\sum_{x=1}^M i_s^x = I2 \quad (\text{II.5.9})$$

(II.5.8) and (II.5.9) imply the sum of AC currents should be zero.

$$\sum_{x=1}^M I_{u,ac}^x = \underline{0}$$

$$\sum_{x=1}^M I_{s,ac}^x = \underline{0}$$
(II.5.10)

A symmetric set of AC currents in each leg is necessary to have only DC current in both DC buses.

### II.5.3 Operating principle

Unlike low voltage converter, an M2DC leg needs AC components to balance capacitor energy between the upper and lower arm. The next issue is to determine arms voltages and currents with DC and AC components. These arms voltages and currents are firstly expressed in the time domain. Then AC components are extracted and rewritten in phasor form to clarify phase angles shift. The phasor form is also useful for following mathematical modeling of the converter leg. Finally, the study concerns power relations in the steady state.

#### II.5.3.1 Arm voltages

Modulation arm index  $m$  (II.4.5) depends on arm voltages defined as (II.5.11).

$$v_{mu}(t) = V_{mu,dc} + \hat{V}_{mu,ac} \cos(\omega t)$$

$$v_{ml}(t) = V_{ml,dc} + \hat{V}_{ml,ac} \cos(\omega t + \theta)$$
(II.5.11)

where  $V_{mu,dc}$  and  $V_{ml,dc}$  are DC voltage component of upper arms and lower arms respectively.  $\hat{V}_{mu,ac}$  and  $\hat{V}_{ml,ac}$  are magnitudes of AC voltage component of upper and lower arms respectively.

$\theta$  is the phase angle of AC voltages between the upper arm and lower arm. Taking upper arm voltage as a reference, lower arm voltage leads or lags the reference having an impact on the power flow direction. Angle  $\theta$  and amplitudes of arm voltages will be dependent of each other, as will be explained later.  $\omega$  is the fundamental frequency of AC voltages of upper and lower arm inserted to balance DC powers.

In terms of phasors, arms voltages in the time domain are written as (II.5.12) and Fig 52.

$$\underline{V}_{mu,ac} = \hat{V}_{mu,ac} \cdot e^{j0} = \hat{V}_{mu,ac}$$

$$\underline{V}_{ml,ac} = \hat{V}_{ml,ac} \cdot e^{j\theta}$$
(II.5.12)

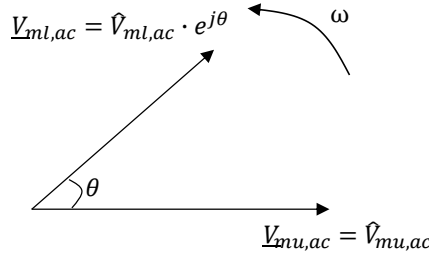


Fig 52. Representation of AC arms voltages in the phasor diagram

### II.5.3.2 Arm currents

Currents are the consequences of arms voltages and passing in both arms (II.5.13).

$$\begin{aligned} i_u(t) &= I_{u,dc} + \hat{I}_{u,ac} \cos(\omega t + \varphi) \\ i_l(t) &= I_{l,dc} + \hat{I}_{l,ac} \cos(\omega t + \lambda + \varphi) \end{aligned} \quad (\text{II.5.13})$$

where  $I_{u,dc}$  and  $I_{l,dc}$  are DC currents of arms.  $\hat{I}_{u,ac}$  and  $\hat{I}_{l,ac}$  are magnitudes of AC currents.  $\varphi$  represents the phase shift between an upper arm voltage and an upper arm current due to inductances  $l$  and  $L_s$ .  $\lambda$  is the phase shift between an upper arm current and a lower arm current.  $\varphi$  and  $\lambda$  depend on passive elements values.

(II.5.14) is AC arm currents described in the phasor domain.

$$\begin{aligned} \underline{I}_{u,ac} &= \hat{I}_{u,ac} \cdot e^{j \cdot \varphi} \\ \underline{I}_{l,ac} &= \hat{I}_{l,ac} \cdot e^{j \cdot (\lambda + \varphi)} \end{aligned} \quad (\text{II.5.14})$$

Fig 53 expresses AC currents in the phasor diagram.

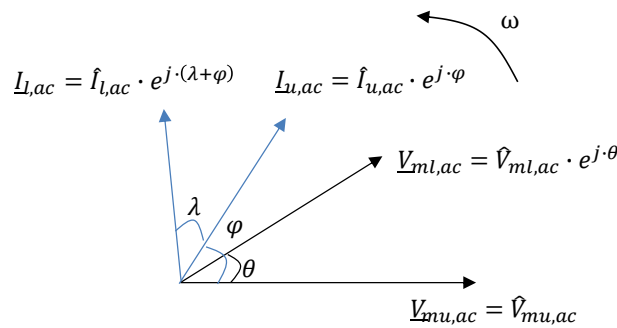


Fig 53. Representation of AC arm currents in the phasor diagram

### II.5.3.3 Arm power expressions

By definition, the instantaneous power is the product of instantaneous voltages and currents. (II.5.15) describes the instantaneous power of the upper arm.

$$\begin{aligned}
p_u = v_{mu} \cdot i_u &= \left( V_{mu,dc} \cdot I_{u,dc} + \frac{1}{2} \cdot \hat{V}_{mu,ac} \cdot \hat{I}_{u,ac} \cdot \cos(\varphi) \right) \\
&+ \hat{V}_{mu,ac} \cdot I_{u,dc} \cdot \cos(\omega t) + V_{mu,dc} \cdot \hat{I}_{u,ac} \cdot \cos(\omega t + \varphi) \\
&+ \frac{1}{2} \cdot \hat{V}_{mu,ac} \cdot \hat{I}_{u,ac} \cdot \cos(2\omega t + \varphi)
\end{aligned} \tag{II.5.15}$$

(II.5.16) shows the instantaneous power flowing in the lower arm.

$$\begin{aligned}
p_l = v_{ml} \cdot i_l &= \left( V_{ml,dc} \cdot I_{l,dc} + \frac{1}{2} \cdot \hat{V}_{ml,ac} \cdot \hat{I}_{l,ac} \cdot \cos(\theta - \varphi - \lambda) \right) \\
&+ \hat{V}_{ml,ac} \cdot I_{l,dc} \cdot \cos(\omega t + \theta) + V_{ml,dc} \cdot \hat{I}_{l,ac} \cdot \cos(\omega t + \varphi + \lambda) \\
&+ \frac{1}{2} \cdot \hat{V}_{ml,ac} \cdot \hat{I}_{l,ac} \cdot \cos(2\omega t + \theta + \varphi + \lambda)
\end{aligned} \tag{II.5.16}$$

Active power of each arm resulting from voltages and currents are the mean values of each instantaneous power. The first observation of the two equations (II.5.15) and (II.5.16) is that the constant terms have to be zero, which is the objective of introducing AC voltages (II.5.17).

$$\begin{aligned}
P_u = \langle p_u \rangle &= P_{u,DC} + P_{u,AC} = V_{mu,dc} \cdot I_{u,dc} + \frac{1}{2} \cdot \hat{V}_{mu,ac} \cdot \hat{I}_{u,ac} \cdot \cos(\varphi) = 0 \\
P_l = \langle p_l \rangle &= P_{l,DC} + P_{l,AC} = V_{ml,dc} \cdot I_{l,dc} + \frac{1}{2} \cdot \hat{V}_{ml,ac} \cdot \hat{I}_{l,ac} \cdot \cos(\theta - \varphi - \lambda) = 0
\end{aligned} \tag{II.5.17}$$

By definition, the active power of an AC system is the real part of the complex power. Their active power can be formulated in phasor form as (II.5.18).

$$\begin{aligned}
P_{u,AC} &= \Re \left\{ \frac{1}{2} \cdot \underline{V}_{mu,ac} \cdot \underline{I}_{u,ac}^* \right\} \\
P_{l,AC} &= \Re \left\{ \frac{1}{2} \cdot \underline{V}_{ml,ac} \cdot \underline{I}_{l,ac}^* \right\}
\end{aligned} \tag{II.5.18}$$

Furthermore, each instantaneous AC power has two oscillation frequencies. One is at the fundamental frequency  $\omega$ , the other is at  $2\omega$  which is the second harmonic term. As power is the derivative of stored energy, the charge or discharge of capacitors energy is realized by the power oscillations, which influences greatly the size and the cost of capacitors.

## II.6 Model of M2DC Converter and parameters design

Previous discussions have explained how using AC components to balance capacitors energies and investigated the operating principle in steady state. In this section, a mathematical model is proposed under two assumptions:

- Algorithm “Nearest Level Control” works perfectly and capacitor voltages are equal;
- Converter losses continue to be ignored.

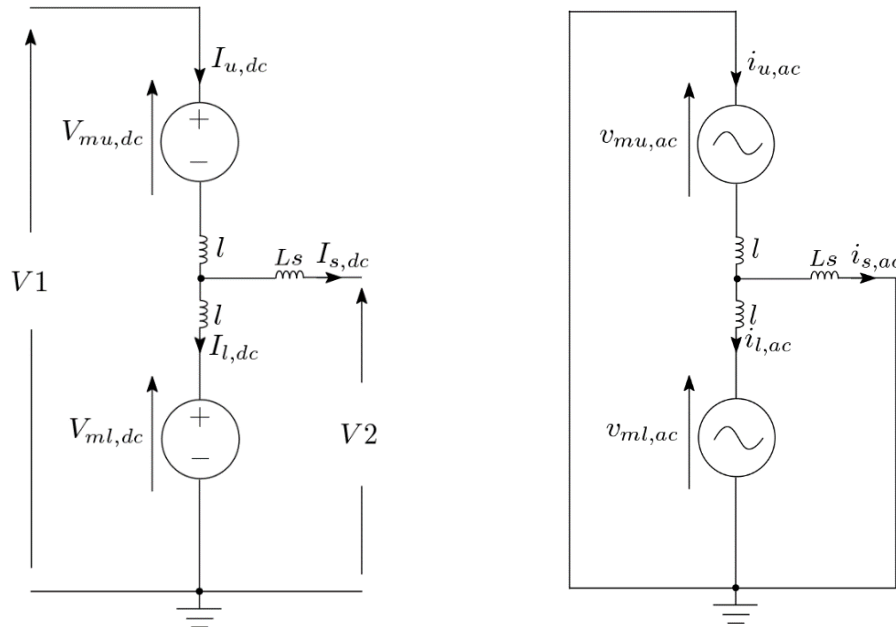
With these two assumptions, this part defines dynamic models of a leg in the time and phasor domains. Time-domain models show variables forms over time. They will be used to establish the control algorithms in the next chapter. Phasor domain models clarify the amplitude, frequency, and phase of variables, which is the foundation of the converter characterizing and design.

### II.6.1 DC and AC behavior modeling

Applying Kirchhoff's circuit law on Fig 49, voltage and current equations of a leg are written as (II.6.1).

$$\begin{aligned}
 V1 &= v_{mu} + v_{ml} + l \cdot \left( \frac{di_u}{dt} + \frac{di_l}{dt} \right) \\
 V2 + L_s \cdot \frac{di_s}{dt} &= v_{ml} + l \cdot \frac{di_l}{dt} \\
 i_s &= i_u - i_l
 \end{aligned}
 \tag{II.6.1}$$

These equations, governing the converter behavior, contain DC and AC components. Then, decoupling DC and AC part is convenient for analyzing the operation of the leg. The decoupling is realized in Fig 54. The leg behavior is seen from DC point of view (Fig 54.(a)) and AC point of view (Fig 54. (b)), pointing out the circulation path of DC and AC currents.



(a) Equivalent average DC circuit      (b) Equivalent average AC circuit  
 Fig 54. Equivalent DC and AC average leg circuits

#### II.6.1.1 Leg model of DC components

Considering Fig 54. (a), DC equations are (II.6.2):

$$\begin{aligned}
V1 &= V_{mu,dc} + V_{ml,dc} + l \cdot \frac{d(I_{u,dc} + I_{l,dc})}{dt} \\
V2 + L_s \cdot \frac{dI_{s,dc}}{dt} &= V_{ml,dc} + l \cdot \frac{dI_{l,dc}}{dt} \\
I_{s,dc} &= I_{u,dc} - I_{l,dc}
\end{aligned} \tag{II.6.2}$$

Since DC grids impose DC voltages, it is evident that DC currents run through each branch of the converter. But DC grids currents may contain some slight ripples due to DC power or DC voltage variations. These variations cause that the derivative terms of DC currents exist in the expression (II.6.2).

### II.6.1.2 Leg model of AC components

Electrical relations of AC components are described in (II.6.3) according to Fig 54 (b). Both DC voltage sources are short-circuited.

$$\begin{aligned}
0 &= v_{mu,ac} + v_{ml,ac} + l \cdot \left( \frac{di_{u,ac}}{dt} + \frac{di_{l,ac}}{dt} \right) \\
L_s \cdot \frac{di_{s,ac}}{dt} &= v_{ml,ac} + l \cdot \frac{di_{l,ac}}{dt} \\
i_{s,ac} &= i_{u,ac} - i_{l,ac}
\end{aligned} \tag{II.6.3}$$

To understand the relations of amplitudes, frequency, and phases of AC components, the model in the time-domain (II.6.3) is transformed to the phasor domain (II.6.4). These equations illustrate relations between AC currents and AC voltages, where AC currents are consequences of AC arm voltages introduced in the M2DC.

$$\begin{aligned}
\underline{I}_{u,ac} &= - \frac{(l + L_s) \cdot \underline{V}_{mu,ac} + L_s \cdot \underline{V}_{ml,ac}}{j \cdot \omega \cdot (2 \cdot l \cdot L_s + l^2)} \\
\underline{I}_{l,ac} &= - \frac{L_s \cdot \underline{V}_{mu,ac} + (l + L_s) \cdot \underline{V}_{ml,ac}}{j \cdot \omega \cdot (2 \cdot l \cdot L_s + l^2)} \\
\underline{I}_{s,ac} &= \frac{-\underline{V}_{mu,ac} + \underline{V}_{ml,ac}}{j \cdot \omega \cdot (2 \cdot L_s + l)}
\end{aligned} \tag{II.6.4}$$

where  $\underline{I}_{u,ac}$  and  $\underline{I}_{l,ac}$  are vectors of arm currents.  $\underline{V}_{mu,ac}$  and  $\underline{V}_{ml,ac}$  are vectors of arm voltages.  $j$  is the imagine part of a complex.  $\omega$  is the angular frequency of AC voltages expressed in rad/s.

To achieve DC power compensation, active powers produced by AC components in arms have to be defined in (II.6.5). These active power are obtained by substituting the equations (II.5.12) and (II.6.4) into (II.5.18).

$$P_{u,AC} = -P_{l,AC} = -\frac{1}{2} \cdot \frac{Ls \cdot \hat{V}_{mu,ac} \cdot \hat{V}_{ml,ac} \cdot \sin(\theta)}{\omega \cdot (2 \cdot l \cdot Ls + l^2)} \quad (\text{II.6.5})$$

where  $\hat{V}_{mu,ac}$  and  $\hat{V}_{ml,ac}$  are amplitudes of AC voltages.  $\theta$  is the angle between two AC voltages.  $P_{u,AC}$  and  $P_{l,AC}$  are active powers of AC components of upper and lower arm respectively.

Active power of AC components must satisfy the condition (II.5.17) to keep the energy balanced in arms to compensate DC powers. Replacing the relation between rated power  $P1$  and AC active powers explained in Fig 50 into (II.6.5), an expression of the rated power of a leg is obtained in (II.6.6).

$$\frac{P1}{M} = \frac{1}{1-\alpha} \cdot \frac{1}{2} \cdot \frac{Ls \cdot \hat{V}_{mu,ac} \cdot \hat{V}_{ml,ac} \cdot \sin(\theta)}{\omega \cdot (2 \cdot l \cdot Ls + l^2)} \quad (\text{II.6.6})$$

The rated power  $P1/M$  is dependent on AC voltages and values of inductances. As a consequence, the choice of both (AC voltages and the design of inductances values) are degrees of freedom for the converter leg. Such numerous degrees of freedom are neither convenient for characterizing the converter, nor for the control design. To distinguish these AC variables, global impacts of AC voltages will be analyzed.

### II.6.2 Degrees of freedom

There are six degrees of freedom that influence the converter power flow  $P1$ . The influences can be explained by rewriting equation (II.6.6) in another form (II.6.7) and Fig 55.

$$\frac{1}{2} \cdot \frac{\hat{V}_{mu,ac} \cdot \hat{V}_{ml,ac} \cdot \sin(\theta)}{l \cdot \omega \cdot \left(2 + \frac{l}{Ls}\right)} = \frac{P1}{M} \cdot (1 - \alpha) \quad (\text{II.6.7})$$

Four degrees of freedom are linked to AC voltages. They are two AC voltage amplitudes ( $\hat{V}_{mu,ac}$ ,  $\hat{V}_{ml,ac}$ ), angle  $\theta$  and angular frequency  $\omega$ .

Two degrees of freedom are linked to inductors design: arm inductor  $l$  and secondary inductor  $Ls$ .

All degrees of freedom have different impacts on the converter operation.

- Higher AC voltages increase power transmission capability.
- The phase  $\theta$  between an upper arm and a lower arm voltage has the same effect as amplitudes. When  $\sin(\theta)$  approaches to unity, the converter transmits the highest power.
- Angular frequency  $\omega$  has an inverse consequence to the transmission power. But its choice has an important impact on AC current amplitudes and sizing of passive components.



- Finally, choosing carefully inductances is critical for increasing the converter performance as well. They resist alternative currents flow. Less AC currents pass through, less power is transmitted.

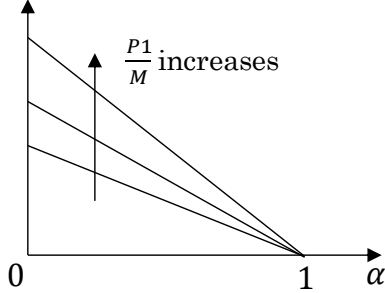
$$|P_{u,AC}| = |P_{l,AC}| = \frac{1}{2} \cdot \frac{\hat{V}_{mu,ac} \cdot \hat{V}_{ml,ac} \cdot \sin(\theta)}{l \cdot \omega \cdot \left(2 + \frac{l}{L_s}\right)}$$


Fig 55. Impacts of six degrees of freedom

This general analysis of the converter covers all possibilities brought by the converter. Degrees of freedom on AC voltages and inductances have consequences on the converter performance. Selecting suitable AC voltages becomes a great issue. To resolve the issue, the next part presents the analysis.

## II.7 AC voltage components analysis

The objective of this section is to investigate the four degrees of freedom of AC voltages regarding a rated power  $P1$ . The power transmission of a leg is  $P1/M$ .

Firstly, some choices are made to reduce the number of degrees of freedom. These choices limit the converter to work in certain conditions. Then, investigations are based on these choices with limited conditions. It consists of an investigation of AC voltages, total arm voltages, and operating frequency. Their analysis is described by their limits which characterize the converter behavior in terms of voltage and also in power capacity.

### II.7.1 Choices of angle $\theta$ and amplitudes of AC voltages

The main idea of our choices is to minimize the amplitudes of two AC arms voltages in order to limit AC currents with a fixed frequency. The equation (II.6.6) is rewritten as (II.7.1).

$$\frac{1}{2} \cdot \hat{V}_{mu,ac} \cdot \hat{V}_{ml,ac} \cdot \sin(\theta) = \frac{P1}{M} \cdot (1 - \alpha) \cdot l \cdot \omega \cdot \left(2 + \frac{l}{L_s}\right) \quad (\text{II.7.1})$$

where the term  $\frac{P1}{M} \cdot (1 - \alpha) \cdot l \cdot \omega \cdot \left(2 + \frac{l}{L_s}\right)$  is considered constant.

This relation (drawn in Fig 56) is a symmetrical function with respect to  $\sin(\theta) = 0$ . Depending on the angle definition in Fig 52, the AC voltage of the upper arm  $v_{mu,ac}$  is lagging the AC voltage of the lower arm  $v_{ml,ac}$  by the angle  $\theta$ . This angle describes the

direction of power transmission. Assuming the positive power transmission is from  $V1$  (high DC voltage) to  $V2$  (low DC voltage), angle  $\theta$  will be positive. On the contrary, if the power transmission is from the low voltage  $V2$  to the high voltage  $V1$ , angle  $\theta$  will be negative.  $v_{mu,ac}$  leads  $v_{ml,ac}$  by angle  $\theta$ .

With the transmission power  $P1/M$ , voltage ratio  $\alpha$  is different from 1. The product of the two AC amplitudes and  $\sin(\theta)$  show an inverse relation between each of them. An opposite phase means that  $\sin(\theta)$  equal to zero. Then, AC amplitudes will be infinite if power is not zero. A minimum value for  $\theta$  is, therefore, required to transmit power.

Finally, the minimum value of  $\hat{V}_{mu,ac} \cdot \hat{V}_{ml,ac}$  occurs when  $\sin(\theta)$  is  $\pm 1$  according to the sign of the rated power  $P1$ .

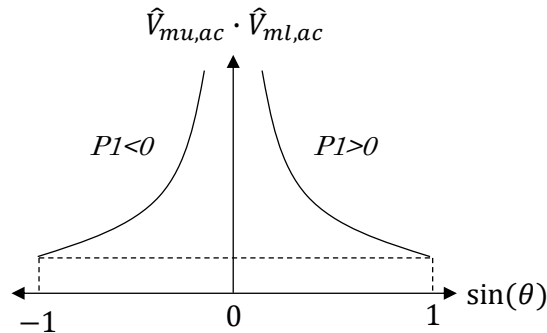


Fig 56. Evolution of AC amplitude in terms of angle  $\theta$

To have minimum amplitudes for the two AC voltages,  $\hat{V}_{mu,ac}$  and  $\hat{V}_{ml,ac}$  are set to be equals. Thus, AC voltages are described in (II.7.2) and Fig 57. ***This particular choice of AC components is then applied and kept throughout this manuscript.***

$$\begin{aligned} \underline{V}_{mu,ac} &= \hat{V}_{mu,ac} \cdot e^{j \cdot 0} = \hat{V}_{mu,ac} \\ \underline{V}_{ml,ac} &= \hat{V}_{mu,ac} \cdot e^{j \frac{\pi}{2}} = j \cdot \hat{V}_{mu,ac} \end{aligned} \quad (\text{II.7.2})$$

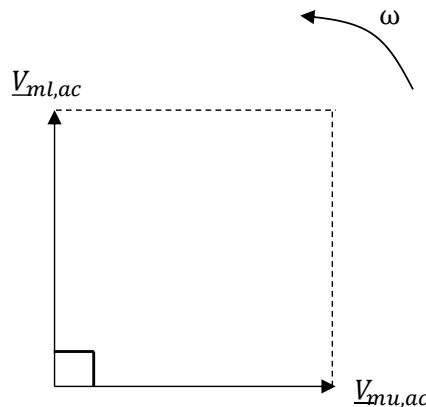


Fig 57. Voltage phasor with minimized AC amplitudes

## II.7.2 Limits of operation

A leg needs DC and AC components to transmit power in which DC grids impose DC components. Regarding AC components which are added to balance the internal leg energy, choices of AC components are restricted by the type of submodule and DC components. Changing the submodule type changes the limits of the leg.

Our work studies half bridge submodule. These limitations indicate the leg potential capability in voltage.

### II.7.2.1 Limits of AC voltage components

Submodule topology and DC voltages impose AC voltage limits. For half bridge submodules, negative arm voltage is unrealizable as explained in Fig 43. Regarding DC voltages, amplitudes of AC voltages have to be inferior to the DC voltage components (II.7.3) drawn in Fig 58.

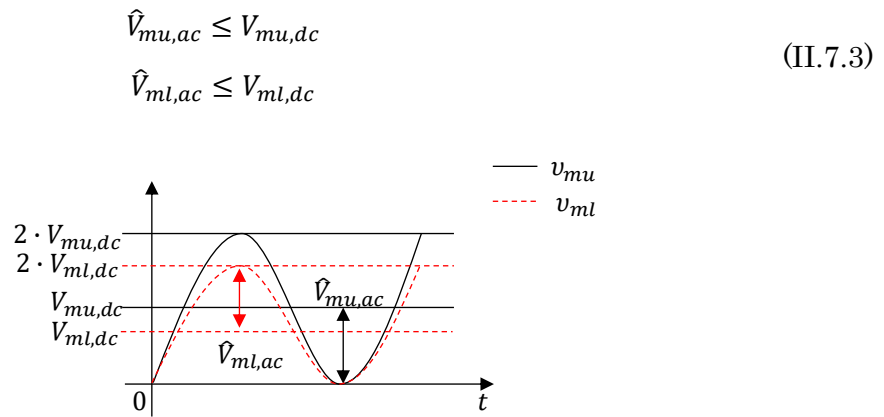


Fig 58. AC and DC voltage component of the upper and lower arm

According to (II.5.4), the relation (II.7.3) is described in (II.7.4) to illustrate AC voltages limitations in terms of  $\alpha$ . It is shown graphically in Fig 59.

$$\begin{aligned}\hat{v}_{mu,ac} &\leq (1 - \alpha) \cdot V1 \\ \hat{v}_{ml,ac} &\leq \alpha \cdot V1\end{aligned}\tag{II.7.4}$$

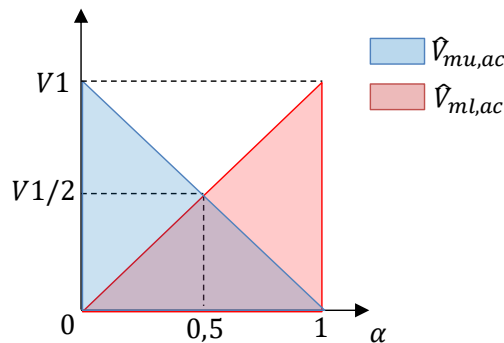


Fig 59. Upper limits of AC voltages for the upper and lower arm

Upper and lower arms have different limitations on AC components due to their different DC voltage components. The limitation is the same, only when  $\alpha$  is equal to 0.5, since the partition of DC bus voltage  $V1$  between the two arms is identical.

Taking into account the choices made in the previous section, the amplitudes of upper and lower arms voltages are set to be equal to minimize their amplitudes. To ensure positive voltages for the two arms, AC voltages should take minimum value of them (II.7.5).

$$\hat{V}_{mu,ac} = \hat{V}_{ml,ac} \leq \min (V_{mu,dc}, V_{ml,dc}) \quad (\text{II.7.5})$$

This equation is illustrated in Fig 60.

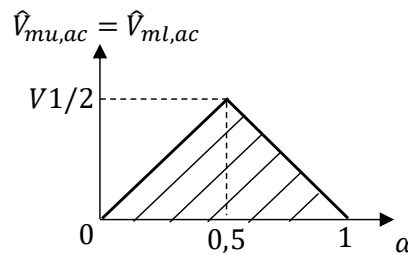


Fig 60. Upper limitation of AC voltages with the condition  $\hat{V}_{mu,ac} = \hat{V}_{ml,ac}$

The AC voltages limitations are symmetric around  $\alpha = 0.5$ . At  $\alpha = 0.5$ , the leg is able to carry an amplitude of  $V1/2$  which is the greatest AC component value. Otherwise, AC amplitude reduces when voltage ratio approaches both extremities. The Fig 60 shows the AC voltage component that a leg is able to create.

### II.7.2.2 Limit of total arm voltage $v_{ctot}$

The total arm voltage  $v_{ctot}$  (II.4.2) is the voltage of a string of submodules, which defines the voltage that an arm can handle. It is calculated as the sum of DC voltage and AC voltage components. Taking into account the choice that  $\hat{V}_{mu,ac}$  is equal to  $\hat{V}_{ml,ac}$ , both total arm voltages are described in (II.7.6).

$$\begin{aligned} v_{ctotu} &\geq V_{mu,dc} + \hat{V}_{mu,ac} \\ v_{ctotl} &\geq V_{ml,dc} + \hat{V}_{ml,ac} \end{aligned} \quad (\text{II.7.6})$$

As discussed earlier, an arm should be able to hold a minimum voltage to create DC and AC voltage components. Therefore, total arm voltages should be superior or equal to the maximum voltage to satisfy the demand of the converter control. However, if the total arm voltage is superior to the sum of two components, the supplementary parts expect more submodules or higher capacitor voltage rating. For the final design, efficiency and economic reasons must be taken into account.

Considering of AC voltage components (Fig 60), their upper limitations give us an estimated view of total arm voltages. If AC voltages are selected by their maximum values, the minimum values of total arm voltages are drawn in Fig 61. The upper and lower arm have different total arm voltages. The difference provided by AC voltages involves a potential difference in submodules number. Therefore, it is not necessary to design the total arm voltage of upper arms and lower arms in the same way and with same submodules number. Moreover, to minimize the submodules number, it is on the contrary benefit to design the two arms with suitable different submodule numbers.

Only if the voltage ratio is a half, both arms share equally the voltage of the DC grid  $V1$ . Then, the minimum value of total arm voltages is the same for the upper and lower arm. In this case, the submodules number of both arms should be equal, just like the MMC converter topology.

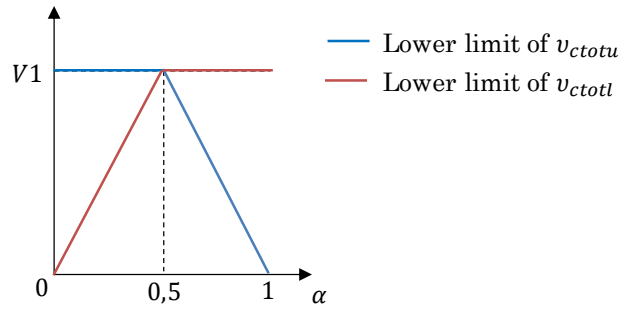


Fig 61. Lower limits of total arm voltages  $v_{ctot}$  with maximum AC voltage components

In any case, since AC voltages change in terms of voltage ratio and power, DC voltages are therefore the minimum voltages that total arm voltage must be able to create (II.7.7).

$$\begin{aligned} v_{ctotu} &\geq V_{mu,dc} = (1 - \alpha) \cdot V1 \\ v_{ctotl} &\geq V_{ml,dc} = \alpha \cdot V1 \end{aligned} \quad (II.7.7)$$

To conclude, total arm voltages can take any value in the range of  $(V_{mu,dc}, +\infty)$  and  $(V_{ml,dc}, +\infty)$  for the upper and lower arm, respectively (II.7.7). AC components play an important role for the total arm voltages design. Depending on the different AC components, the voltage that an arm should be able to hold is not fixed.

But the voltage  $v_{ctot}$  is expected to be greater than the lower limitation (defined in Fig 61) to perform the maximal transmission power per leg in the condition of no other limitation (current value, voltage variations, etc.).

### II.7.2.3 Limit of operating angular frequency

Another degree of freedom is the operating angular frequency  $\omega$ . The MMC must be synchronized to the frequency of AC grids, 50Hz. For M2DC, the frequency is a degree of freedom that influences greatly the operation of the M2DC converter. The objective of this part is to discuss how to select it and to define its limitation.

For one operating setpoint, transmission power and voltage ratio are determined by DC grids. Depending on (II.6.6), internal energies balancing depends on the frequency and the amplitude of AC voltages. Rewriting the relation (II.6.6) and taking into account the choices discussed previously, (II.7.8) is obtained.

$$\omega = \frac{1}{1-\alpha} \cdot \frac{1}{2} \cdot \frac{Ls \cdot (\hat{V}_{mu,ac})^2}{\frac{P1}{M} \cdot (2 \cdot l \cdot Ls + l^2)} \quad (\text{II.7.8})$$

The relation shows that the angular frequency is limited by AC voltages. Increasing the frequency makes the amplitude of AC voltages higher. Taking into account the maximum value of the AC voltage component (II.7.4), the limit of frequency is described in terms of voltage ratio in (II.7.9) and drawn in Fig 62.

$$\begin{cases} 0 \leq \alpha \leq 0.5, & \omega \leq \frac{\alpha^2}{1-\alpha} \cdot \frac{1}{2} \cdot \frac{Ls \cdot V1^2}{\frac{P1}{M} \cdot (2 \cdot l \cdot Ls + l^2)} \\ 0.5 \leq \alpha \leq 1, & \omega \leq (1-\alpha) \cdot \frac{1}{2} \cdot \frac{Ls \cdot V1^2}{\frac{P1}{M} \cdot (2 \cdot l \cdot Ls + l^2)} \end{cases} \quad (\text{II.7.9})$$

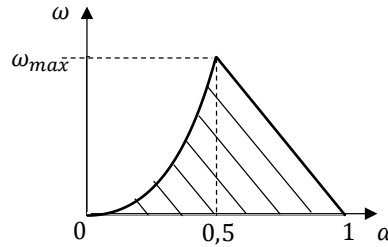


Fig 62. Upper limitation of operating angular frequency

The frequency is divided into two parts,  $\alpha < 0.5$  and  $\alpha > 0.5$ , according to the limitation of AC voltages (Fig 60). If  $\alpha < 0.5$ , the maximum frequency increases with  $\alpha$ . When  $\alpha > 0.5$ , the maximum frequency decreases linearly in terms of the voltage ratio. The maximum frequency is at  $\alpha = 0.5$  where a leg is able to create maximum AC voltages. This point is called  $\omega_{max}$ . It has the expression (II.7.10).

$$\omega_{max} = \frac{1}{4} \cdot \frac{Ls \cdot V1^2}{\frac{P1}{M} \cdot (2 \cdot l \cdot Ls + l^2)} \quad (\text{II.7.10})$$

$\omega_{max}$  is the maximum angular frequency that a leg can theoretically achieve due to the maximum amplitude of AC voltages. This maximal value is also limited by semiconductors, passive components, and converter performances. So it will be necessary to validate this value during the design of the converter according to application constraints and technology.

Furthermore, in practice, extremely low frequencies are considered ineffective to the converter operation, e.g. 1Hz, 10Hz, 20Hz, etc. There is, therefore, a lower limit of the frequency  $\omega_{min}$  defined by applications of the converter.

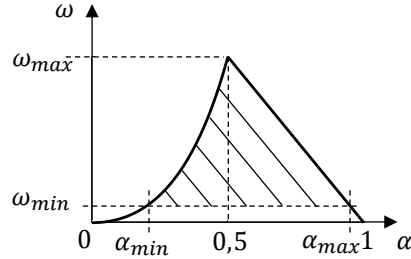


Fig 63. The upper and lower limit of operating angular frequency

The lower limit  $\omega_{min}$  (in Fig 63) illustrates that voltage ratios approaching to 0 or 1 are uninteresting.  $\alpha_{min}$  and  $\alpha_{max}$  indicate the limitations of the voltage ratio defined by the lower limit of frequency.

For a specific voltage ratio, if the rated power  $P1$  is reduced, it will be possible to increase the frequency (in its practical limits) to optimize the performances of the converter. On the contrary, increasing power reduces the frequency, which is generally the case of MTDC grids.

In conclusion, energy balancing relations (II.6.6) are crucial to define degrees of freedom and limitations of AC components in voltage and frequency.

#### II.7.2.4 Consequences of the limits for power transmission

The M2DC can operate thanks to AC components. Four degrees of freedom on AC voltages are reduced to two, which are the amplitude of AC voltage and its frequency by fixing  $\theta = 90^\circ$  and  $\hat{V}_{mu,ac} = \hat{V}_{ml,ac}$ . However, the amplitude of the AC voltages and the frequency are limited by the type of submodule and energy balancing principle. To conclude the analysis on the limitations of AC components, an estimation of power transmission of the converter leg is investigated.

Fixing a frequency and respecting its upper and lower limit, the converter power is proportional to the amplitude of AC voltages. More the converter is able to increase the amplitude of AC voltages, more power can be transmitted. The influence of AC voltages on the converter power is described in (II.7.11) and Fig 64 where the choices made earlier are always available.

$$\begin{cases} 0 \leq \alpha \leq 0.5, & \frac{P1}{M} \leq \frac{\alpha^2}{1-\alpha} \cdot \frac{1}{2} \cdot \frac{Ls \cdot V1^2}{\omega \cdot (2 \cdot l \cdot Ls + l^2)} \\ 0.5 \leq \alpha \leq 1, & \frac{P1}{M} \leq (1-\alpha) \cdot \frac{1}{2} \cdot \frac{Ls \cdot V1^2}{\omega \cdot (2 \cdot l \cdot Ls + l^2)} \end{cases} \quad (II.7.11)$$

Comparing the upper limit of AC voltages (Fig 60) with the upper limit of the power (Fig 64), the converter transmits the highest power (II.7.12) at  $\alpha = 0.5$  thanks to the maximum AC voltage ( $V1/2$ ) created by an arm.

$$\left\{\frac{P1}{M}\right\}_{max} = \frac{1}{4} \cdot \frac{Ls \cdot V1^2}{\omega \cdot (2 \cdot l \cdot Ls + l^2)} \quad (\text{II.7.12})$$

where  $\left\{\frac{P1}{M}\right\}_{max}$  is the maximum power of a leg.

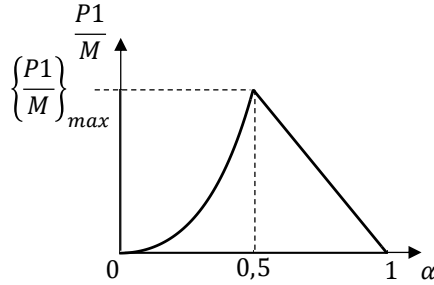


Fig 64. Upper limitation of power transmission

The increased amplitude of AC voltages improves the capability of transmittable power. However, the increased tendency is not always linearly dependent on DC voltages, such as  $0 < \alpha < 0.5$ . If  $0.5 < \alpha < 1$ , a linear relation between power and amplitude of AC voltage is true. As a consequence, with the same amplitude of AC voltage, a leg transmits more power at  $0.5 < \alpha < 1$  than  $0 < \alpha < 0.5$ . This makes the converter more attractive if  $\alpha$  is superior to 0.5, and stays inferior to  $\alpha_{max}$  due to the lower limitations of frequency.

In the condition of keeping the frequency constant, the converter power has also an influence on the active power of AC components, since they are used for balancing the internal energy.

The influence is shown in Fig 65, which is a comparison of the active power of AC components (red line) and the converter transmittable power (black line). The active power of AC components is expressed mathematically in (II.7.13) by varying the constant power  $P1/M$  of Fig 50 to the  $\alpha$  variable power (Fig 64).

$$\left\{ \begin{array}{l} 0 \leq \alpha \leq 0.5, \quad |P_{u,AC}| = |P_{l,AC}| \leq \alpha^2 \cdot \frac{1}{2} \cdot \frac{Ls \cdot V1^2}{\omega \cdot (2 \cdot l \cdot Ls + l^2)} \\ 0.5 \leq \alpha \leq 1, \quad |P_{u,AC}| = |P_{l,AC}| \leq (1 - \alpha)^2 \cdot \frac{1}{2} \cdot \frac{Ls \cdot V1^2}{\omega \cdot (2 \cdot l \cdot Ls + l^2)} \end{array} \right. \quad (\text{II.7.13})$$



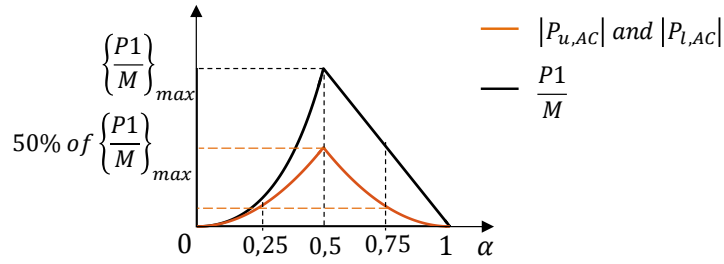


Fig 65. Active powers of AC components  $|P_{u,AC}|$  and  $|P_{l,AC}|$

With a constant frequency, the AC power  $|P_{u,ac}|$  and  $|P_{l,ac}|$  inherit the symmetry of AC voltage components. Therefore, at 0.5, the AC power has the maximum value.

However, compared to the transmittable power, for  $\alpha < 0.5$ , the AC power occupies more than 50 percent of the transmittable power to balance the internal energy. On the contrary for  $\alpha > 0.5$ , the converter uses less power from the transmittable power to balance the energy.

In another way, if the demand of the transmittable power is determined and kept constant, most of the power would be transformed to AC for  $\alpha < 0.5$  instead of  $\alpha > 0.5$  to balance the energy. (This point has been illustrated in Fig 50.) Thus, the great AC power at  $\alpha < 0.5$  has an impact on the converter design.

## II.8 AC currents analysis with $L_s \gg l$

The objective of this section is to investigate the degree of freedom of inductor  $L_s$  and show the leg currents with a constant transmission power.

The investigation on inductor  $L_s$  is firstly realized to facilitate the analysis on the AC current components. Then, the reason of analyzing currents of the converter are:

- AC currents of M2DC converter leg are extremely different from conventional converters.
- AC currents give a global vision of semi-conductor rating, which is helpful to evaluate semiconductor losses and to define the minimum number of converter legs  $M$ , according to the maximal transmission power.

### II.8.1 Minimized AC currents

Instead of investigating an exact value of inductance  $L_s$ , the aim of this part is to show the best case in terms of AC currents for the M2DC converter. Therefore, the inductor  $L_s$  sizing method is not presented here.

As mentioned in the part II.6.2,  $l/L_s$  and power are inversely proportional. The lower the value of  $l/L_s$  is, the higher the power. Before talking about AC currents, the first element is therefore the choice of inductance value  $L_s$ .

Physically, inductor  $L_s$  can be considered as a low pass filter in the middle branch to prevent AC currents pass through DC source  $V_2$ . The advantage of a great inductance  $L_s$  value is the increase of the power of a leg (II.6.6).

Therefore, for the M2DC converter, this inductor cannot be suppressed, which is different from MMC converters. To have a better effect of the filter, each leg of the converter needs a large inductance  $L_s$  to reduce amplitudes of AC currents in the middle branch. Depending on Kirchhoff current law, the reduced AC currents in the middle branch decrease also AC currents in the upper and lower arm.

For this,  $l/L_s$  has necessarily a small value. Of course, in practice, the inductor  $L_s$  must have a limited value to reduce its size and the volume of the converter. A compromise has to be found according to the arm inductor  $l$  value.

Mathematically, minimized AC voltages as from the choice (II.7.2) are expected to produce minimized AC currents  $i_{u,ac}$  and  $i_{l,ac}$ . General expressions of AC currents in the phasor domain are described in (II.8.1) by replacing (II.7.2) into (II.6.4).

$$\begin{aligned} \underline{I}_{u,ac} &= \frac{\sqrt{L_s^2 + (l + L_s)^2}}{(2 \cdot l \cdot L_s + l^2)} \cdot \frac{\hat{V}_{mu,ac}}{\omega} \cdot e^{j \cdot \arctg\left(-\frac{l+L_s}{L_s}\right)} \\ \underline{I}_{l,ac} &= \frac{\sqrt{L_s^2 + (l + L_s)^2}}{(2 \cdot l \cdot L_s + l^2)} \cdot \frac{\hat{V}_{mu,ac}}{\omega} \cdot e^{j \cdot \arctg\left(-\frac{L_s}{l+L_s}\right)} \end{aligned} \quad (\text{II.8.1})$$

To minimize AC currents, which is convenient to reduce arms losses, a maximum frequency is necessary. This frequency increases the impedances of arms which reduces AC currents. Since the first terms of expression (II.8.1) can be considered as admittances, to have minimum AC currents, it is better to select small admittances with inductor  $L_s$  much greater than  $l$ . Thus, for an extreme case that the inductance  $L_s$  is considered as infinite, the middle branch is an open circuit for the AC side. Then, AC current of arms have their minimum values described by (II.8.2). These values are obtained by considering  $L_s = \infty$  in the expressions (II.8.1).

$$\begin{aligned} \underline{I}_{u,ac} &\cong \frac{1}{\sqrt{2} \cdot l} \cdot \frac{\hat{V}_{mu,ac}}{\omega} \cdot e^{j \cdot \arctg(-1)} \\ \underline{I}_{l,ac} &\cong \frac{1}{\sqrt{2} \cdot l} \cdot \frac{\hat{V}_{mu,ac}}{\omega} \cdot e^{j \cdot \arctg(-1)} \end{aligned} \quad (\text{II.8.2})$$

The simplification does not only make amplitudes of AC currents reduced but also change the arguments of AC arm currents. By resolving  $\arctg(-1)$  of expression  $\underline{I}_{u,ac}$  and  $\underline{I}_{l,ac}$ , the argument of the current of each arm has two possibilities ( $-45^\circ, 135^\circ$ ). But only the argument  $135^\circ$  satisfies the energy balancing relation (II.5.17). Therefore the AC current of upper arm should lead AC voltage with  $\varphi = 135^\circ$  (Fig 66). Then, both arm currents are in phase, i.e.  $\lambda \cong 0$ .

$$\begin{aligned} \underline{I}_{u,ac} &\cong \frac{1}{\sqrt{2} \cdot l} \cdot \frac{\hat{V}_{mu,ac}}{\omega} \cdot e^{j \cdot \frac{3\pi}{4}} \\ \underline{I}_{l,ac} &\cong \frac{1}{\sqrt{2} \cdot l} \cdot \frac{\hat{V}_{mu,ac}}{\omega} \cdot e^{j \cdot \frac{3\pi}{4}} \end{aligned} \quad (\text{II.8.3})$$

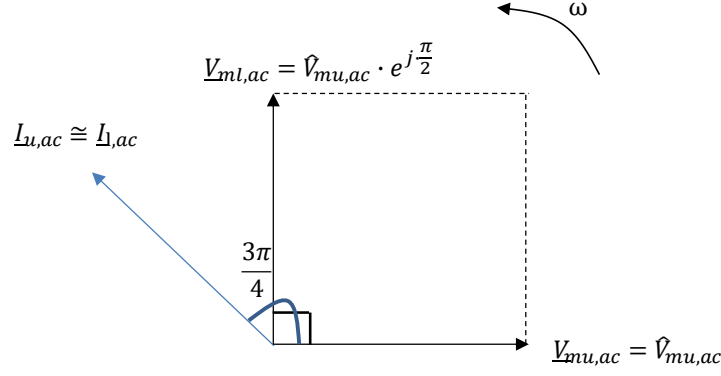


Fig 66. AC voltages and AC currents (with  $L_s = \infty$ ) in the phasor diagram

### II.8.2 Analysis of arm currents

This part discusses two specific currents in the arm: AC current components and arm currents (DC+AC components). AC current components allow justifying the choices made on AC voltages strategy. Analysis of total arm currents draws a global situation on the converter design.

It is notable that for a constant power, manipulating frequency changes the amplitudes of AC voltages. The discussion hereafter on AC currents is based on an operating power and maximum AC voltages (Fig 60) according to the voltage ratio  $\alpha$ .

It implies that the frequency is not constant and has its maximum value corresponding to each maximum AC voltages at each voltage ratio (Fig 62).

Analysis afterwards is based on the conditions:

- The rated grid power  $P_1$  is constant;
- The value of  $L_s$  is great to have minimum AC currents;
- The voltage ratio is changed in an interval  $(0,1)$  where 0 and 1 are not included.

#### II.8.2.1 Analysis of AC currents relative values

AC currents are studied by the relation (II.5.17) where AC currents are in terms of AC voltages, DC voltages, and DC currents.

Taking into account the choices of previous sections, AC voltages are set to be equals and angle  $\theta$  is set to  $\pm 90^\circ$  to ensure minimum amplitudes.  $L_s$  is great enough that both AC currents are phase shifted  $135^\circ$  from  $v_{\mu,ac}$ . Considering (II.5.17), the proportions of DC and AC currents of arms are obtained in (II.8.4). If the power transferred by an arm is constant, AC currents ( $\hat{I}_{u,ac}$ ,  $\hat{I}_{l,ac}$ ) have an inverse relation of AC voltages ( $\hat{V}_{\mu,ac}$ ,  $\hat{V}_{ml,ac}$ ). Notably, the frequency is variable in this section.

$$\frac{\hat{I}_{u,ac}}{I_{u,dc}} = -\frac{2 \cdot V_{\mu,dc}}{\hat{V}_{\mu,ac} \cdot \cos\left(\frac{3\pi}{4}\right)} \quad (II.8.4)$$

$$\frac{\hat{I}_{l,ac}}{I_{l,dc}} = -\frac{2 \cdot V_{ml,dc}}{\hat{V}_{ml,ac} \cdot \cos\left(\frac{\pi}{4}\right)}$$

By substituting AC voltages (II.7.5), DC voltages (II.5.4) and DC currents (II.5.2), (II.5.3) into (II.8.4), AC current components are finally described in equation (II.8.5). As AC voltages have maximum limitations due to half bridge submodule application, then AC currents have their lower limitations.

$$\begin{cases} 0 < \alpha \leq 0.5 & \frac{\hat{I}_{u,ac}}{\frac{I1}{M}} = \frac{\hat{I}_{l,ac}}{\frac{I1}{M}} > 2 \cdot \sqrt{2} \cdot \left(\frac{1}{\alpha} - 1\right) \\ 0.5 \leq \alpha < 1 & \frac{\hat{I}_{u,ac}}{\frac{I1}{M}} = \frac{\hat{I}_{l,ac}}{\frac{I1}{M}} > 2 \cdot \sqrt{2} \end{cases} \quad (II.8.5)$$

These lower limitations are shown graphically in Fig 67, which considers the limitation of  $\alpha$  due to the frequency.

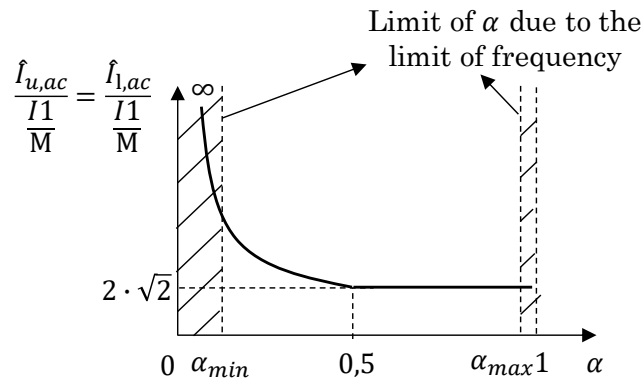


Fig 67. Lower limitations of AC currents

The amplitude of AC current components is more important at  $\alpha < 0.5$  than  $\alpha > 0.5$ . This result can be explained by comparing AC and DC powers (Fig 65) and AC voltage (Fig 60).

The AC current resulted by the power and voltage is therefore great for  $\alpha < 0.5$ . Following the decreased AC power and increased AC voltage, the AC current decreases exponentially until  $\alpha = 0.5$ .

The AC current finds its minimum value for  $\alpha \geq 0.5$ . Then, the decrease of AC power has the same tendency as the AC voltages. As a result, AC currents keep constant for  $\alpha > 0.5$ .

In Fig 67, two limitations of  $\alpha$  ( $\alpha_{min}$ ,  $\alpha_{max}$ ) are also considered due to the limitation of frequency. They can be adjusted to avoid overcurrent for  $\alpha < 0.5$ .

In conclusion, M2DC converter needs AC components, which limits the converter performance. For a rated transmission power, AC components change in terms of  $\alpha$  (Fig 67). The converter is more restrictive by the AC current at  $\alpha_{min} < \alpha < 0.5$  and by the AC voltage at  $\alpha = 0.5$ . Table 6 summarizes the important limits due to AC constraints. If the converter must operate at  $\alpha < 0.5$ , an analysis of arm currents (DC+AC components) is mandatory to adjust the  $\alpha_{min}$  and avoid overcurrent.

Table 6 AC components of Half-Bridge M2DC converter leg

Voltage ratio	$\alpha = 0.5$
Maximum AC voltage (Amplitude value)	$V/2$
Minimum AC current (Amplitude value)	$2 \cdot \sqrt{2} \cdot \frac{I_1}{M}$
Active power of AC components	$\frac{P_1}{2 \cdot M}$

It is notable that the analysis of AC currents is based on the choices made on AC voltages and constant power. If these choices are changed, a review of this analysis will be necessary.

### II.8.2.2 Analysis of total arm currents

To resolve the semiconductors rating issue and find  $\alpha_{min}$  by a limitation of arm current, the DC current component is taken into account. The maximum values of currents for an arm are, therefore, calculated by summing AC and DC current components in (II.8.6).

$$\begin{aligned}\hat{I}_u &= |I_{u,dc}| + \hat{I}_{u,ac} \\ \hat{I}_l &= |I_{l,dc}| + \hat{I}_{l,ac}\end{aligned}\tag{II.8.6}$$

where  $\hat{I}_u$  is the maximum value of current for the upper arm.  $\hat{I}_l$  is the maximum value of current for the lower arm.

As DC components of the upper and lower arm are different. Maximum values of arms currents are expressed separately in (II.8.7) for the upper arm

$$\begin{cases} 0 < \alpha \leq 0.5 & \frac{\hat{I}_u}{I_1/M} > 1 + 2 \cdot \sqrt{2} \cdot \left(\frac{1}{\alpha} - 1\right) \\ 0.5 \leq \alpha < 1 & \frac{\hat{I}_u}{I_1/M} > 1 + 2 \cdot \sqrt{2}\end{cases}\tag{II.8.7}$$

and in (II.8.8) for the lower arm.

$$\begin{cases} 0 < \alpha \leq 0.5 & \frac{\hat{I}_l}{I_1/M} > (1 + 2 \cdot \sqrt{2}) \cdot \left(\frac{1}{\alpha} - 1\right) \\ 0.5 \leq \alpha < 1 & \frac{\hat{I}_l}{I_1/M} > \left(\frac{1}{\alpha} - 1\right) + 2 \cdot \sqrt{2}\end{cases}\tag{II.8.8}$$

Both currents are shown in Fig 68. The upper arm current has the same form as its AC component. Their difference is the DC current  $I_1/M$ . The lower arm current has a different form from its AC component due to the variable DC current  $I_2/M$  in terms of  $\alpha$ .

For  $\alpha < 0.5$ , the lower arm takes more current stresses than the upper arm. This situation is changed for  $0.5 < \alpha < \alpha_{max}$  where the upper arm has more currents. It is only at  $\alpha = 0.5$  that both arms share the same currents stress. Otherwise, two arms have always different currents, then different constraints.

To avoid overcurrent in the arms, the limitation of  $\alpha_{min}$  is adjusted for  $\alpha < 0.5$  in Fig 68 by the limitation of arm current (red dashed line).

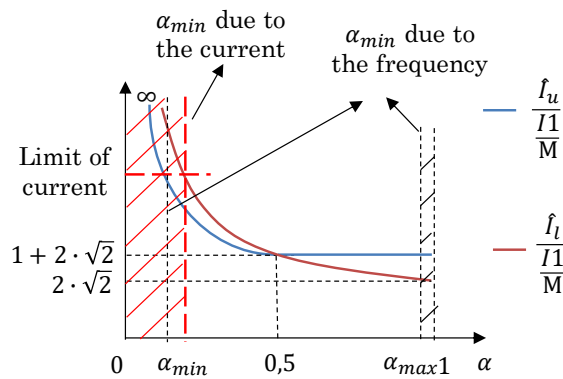


Fig 68. Lower limitations of arms currents

In conclusion, to transfer a certain rated power, the leg has different constraints for the upper and lower arm. With different voltage ratio, three main parameters are designing the converter: total arm voltages  $v_{ctot}$ , arm currents and frequency (Table 7).

Table 7 Other electrical parameters for the converter design

Voltage ratio	$\alpha_{min} < \alpha < 0.5$	$\alpha = 0.5$	$0.5 < \alpha < \alpha_{max}$
Total arm voltage	-	$\geq 2V_1$	-
Arm current	< limit of current	$\hat{I}_u \cong (1 + 2\sqrt{2}) \cdot \frac{I_1}{M}$ $\hat{I}_l \cong (1 + 2\sqrt{2}) \cdot \frac{I_1}{M}$	$\hat{I}_u \cong (1 + 2\sqrt{2}) \cdot \frac{I_1}{M}$ $\hat{I}_l > 2\sqrt{2} \cdot \frac{I_1}{M}$
Frequency	$> \omega_{min}$	$\omega_{max}$	$> \omega_{min}$

Regarding voltage results, the converter needs the higher number of submodules at  $\alpha = 0.5$ . Then, converter cost and losses in semiconductors could be important.

Regarding current results, the converter is more efficient for low tap conversion, with voltage ratio superior to 0.5 since current, and then losses are reduced.

The third parameter is the frequency. Increasing the operating frequency reduces inductance and capacitance value, but its maximal value is limited by technological

constraints. Therefore a compromise has to be taken into account during the converter design.

## II.9 Arm inductance design and Capacitance design

This section intends to show design methods of arm inductance and submodule capacitance. The first part concerns the design of arm inductors which is the same as the design concept of arm inductance of MMC converter. The submodule capacitance is designed to reduce capacitor voltage ripple. Since the two arms of a leg have different constraints, the capacitance of the upper and lower arm are designed separately.

### II.9.1 Arm inductance design

For MMC converters, arm inductance is designed for different applications [70]-[73], [77]. For the M2DC converter, a practical interest of the arm inductor is to limit fault current rise rate on high DC voltage side  $V1$ . Therefore, the arm inductance is designed to ensure the fault current stay under a threshold level in case of a short circuit occurred at high DC voltage side (Fig 69).

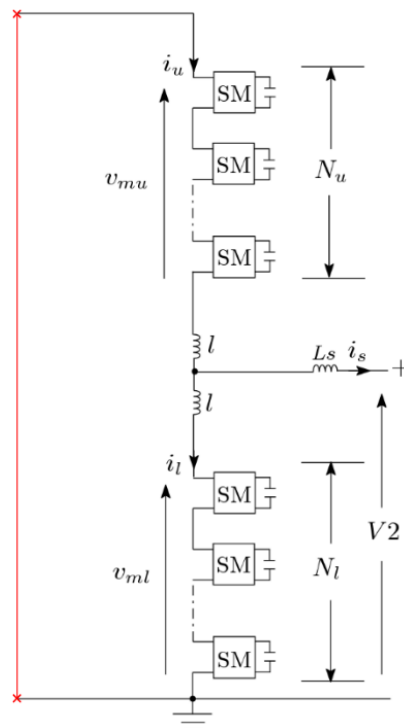


Fig 69. Short circuit occurred on the high voltage side  $V1$

Even though large inductances allow the system to have more time to react in case of a fault, arm inductance is expected to have a minimum value for three reasons.

Firstly, minimum inductances are convenient for high power transmission (II.6.7). Increasing arm inductances reduces power transmission and arms currents.

Secondly, a great value of arm inductance increases the amplitude of AC voltages required to create the AC power.

The third reason is that the minimum arm inductance is more convenient for the design of the inductance  $L_s$ . To reduce the currents of the leg,  $L_s$  should be greater than arm inductance from the discussion of part “II.8.1 Minimized AC currents”. In consequence, a minimum value of arm inductance is necessary to avoid a huge inductance  $L_s$ .

The design of arm inductance assumes also that during short-circuit capacitors of submodules don't have enough time to discharge. For the instant, the sum of voltages of the upper and lower arm has the value around high DC grid voltage  $V1$  (II.9.1).

$$v_{mu} + v_{ml} = V1 \quad (\text{II.9.1})$$

According to Kirchhoff Circuit law, the current relation is (II.9.2).

$$V1 + l \cdot \frac{di_u}{dt} + l \cdot \frac{di_l}{dt} = 0 \quad (\text{II.9.2})$$

Assuming the current rise rate is the same in the upper arm and in the lower arm at the fault moment (II.9.3).

$$\frac{\Delta i_u}{\Delta t} = \frac{\Delta i_l}{\Delta t} \quad (\text{II.9.3})$$

where the maximal fault current rise rate can be tolerated by a DC circuit [70], with the unit of A/s.

Therefore arm inductor design formulation is described in (II.9.4) that indicates the minimum arm inductance to make the system react in time.

$$l \geq \frac{V1}{2 \cdot \frac{\Delta i_l}{\Delta t}} \quad (\text{II.9.4})$$

### II.9.2 Capacitance design

The capacitance of submodules is designed based on the arm average model Fig 46 (b). The value of equivalent capacitance is, therefore, the objective instead of submodule capacitance.

Equivalent capacitance is designed to reduce the voltage ripples. To avoid using a huge capacitance, the design seeks the minimum value of capacitances. The design method has already been proposed for MMC converter in [74]-[77]. In this part, they are applied for the M2DC converter. Moreover, the M2DC leg has different characteristics for upper and lower arms. The capacitance expressions are therefore different between upper arms and lower arms.

In any case, it is an approximate design as it uses simplifications for calculating capacitance value. Inductor  $L_s$  is assumed much greater than  $l$ . The real value of  $L_s$  should be taken into account to have an exact capacitance value.



Current-voltage relation of equivalent capacitance is described in (II.9.5).

$$i_m = C_{tot} \cdot \frac{dv_{ctot}}{dt} \quad (\text{II.9.5})$$

Multiplying  $v_{ctot}$  on both side yields

$$i_m \cdot v_{ctot} = C_{tot} \cdot v_{ctot} \cdot \frac{dv_{ctot}}{dt} \quad (\text{II.9.6})$$

As the energy stored in the equivalent capacitance is the energy in the arm, instantaneous power in equivalent capacitance is the same as the power in the arm.

$$i \cdot v_m = i_m \cdot v_{ctot} \quad (\text{II.9.7})$$

The energy fluctuation (II.9.8) is described by integrating capacitance power.

$$W_C(t) = \int i \cdot v_m dt \quad (\text{II.9.8})$$

Taking into account relations (II.5.15), (II.5.16), and considering that inductor  $L_s$  is much greater than  $l$ , the energy expression of the upper arm is obtained in (II.9.9)

$$\begin{aligned} W_{CU}(t) &= \int i_u \cdot v_{mu} dt \\ &= \left( \frac{\hat{V}_{mu,ac} \cdot I_{u,dc}}{\omega} + \frac{\sqrt{2}}{2} \cdot \frac{V_{mu,dc} \cdot \hat{I}_{u,ac}}{\omega} \right) \cdot \sin(\omega t) + \frac{\sqrt{2}}{2} \cdot \frac{V_{mu,dc} \cdot \hat{I}_{u,ac}}{\omega} \cdot \cos(\omega t) \\ &\quad + \frac{\hat{V}_{mu,ac} \cdot \hat{I}_{u,ac}}{4 \cdot \omega} \cdot \cos\left(2\omega t + \frac{\pi}{4}\right) \end{aligned} \quad (\text{II.9.9})$$

and then the energy expression of the lower arm in (II.9.10).

$$\begin{aligned} W_{CL}(t) &= \int i_l \cdot v_{ml} dt \\ &= \left( -\frac{\hat{V}_{ml,ac} \cdot I_{l,dc}}{\omega} + \frac{\sqrt{2}}{2} \cdot \frac{V_{ml,dc} \cdot \hat{I}_{l,ac}}{\omega} \right) \cdot \cos(\omega t) + \frac{\sqrt{2}}{2} \cdot \frac{V_{ml,dc} \cdot \hat{I}_{l,ac}}{\omega} \cdot \sin(\omega t) \\ &\quad - \frac{\hat{V}_{ml,ac} \cdot \hat{I}_{l,ac}}{4 \cdot \omega} \cdot \cos\left(2\omega t + \frac{\pi}{4}\right) \end{aligned} \quad (\text{II.9.10})$$

Energy variations in a period are therefore the differences between maximum energy and minimum energy. The differences of energy  $\Delta W_{CU}$  and  $\Delta W_{CL}$  are described as the peak to peak value of the energy fluctuation in (II.9.11). This energy fluctuation definition has been presented in [74].

$$\begin{aligned}\Delta W_{CU} &= \max\{W_{CU}(t)\} - \min\{W_{CU}(t)\} \\ \Delta W_{CL} &= \max\{W_{CL}(t)\} - \min\{W_{CL}(t)\}\end{aligned}\quad (\text{II.9.11})$$

where  $\Delta W_{CU}$  and  $\Delta W_{CL}$  are the peak to peak energies.  $\max\{W_{CU}(t)\}$  and  $\max\{W_{CL}(t)\}$  are maximum energy of the upper and lower arm, respectively.  $\min\{W_{CU}(t)\}$  and  $\min\{W_{CL}(t)\}$  are the minimum energy of the upper arm and lower arm, respectively.

The voltage of equivalent capacitances of the upper and lower arm are balanced around their average voltages  $\langle v_{ctotu} \rangle$  and  $\langle v_{ctotl} \rangle$  with voltage ripples  $\Delta V_{ctotu}$  and  $\Delta V_{ctotl}$ . According to [74], it has assumed that average voltages are in the middle of their voltage. The maximum voltages and the minimum voltage are therefore calculated by summing and subtracting the same ripple value. (II.9.12) [74] are the approached expression of the maximum and minimum value of the upper arm.

$$\begin{aligned}\max\{W_{CU}(t)\} &= \frac{1}{2} \cdot C_{totu} \cdot (\langle v_{ctotu} \rangle + \Delta V_{ctotu})^2 \\ \min\{W_{CU}(t)\} &= \frac{1}{2} \cdot C_{totu} \cdot (\langle v_{ctotu} \rangle - \Delta V_{ctotu})^2\end{aligned}\quad (\text{II.9.12})$$

(II.9.13) [74] are the approached expressions of the maximum and minimum value of the lower arm.

$$\begin{aligned}\max\{W_{CL}(t)\} &= \frac{1}{2} \cdot C_{totl} \cdot (\langle v_{ctotl} \rangle + \Delta V_{ctotl})^2 \\ \min\{W_{CL}(t)\} &= \frac{1}{2} \cdot C_{totl} \cdot (\langle v_{ctotl} \rangle - \Delta V_{ctotl})^2\end{aligned}\quad (\text{II.9.13})$$

Energy variations in the upper and lower arm are therefore described in (II.9.14) similar to [74] for MMC.

$$\begin{aligned}\Delta W_{CU} &= 2 \cdot C_{totu} \cdot \langle v_{ctotu} \rangle \cdot \Delta V_{ctotu} \\ \Delta W_{CL} &= 2 \cdot C_{totl} \cdot \langle v_{ctotl} \rangle \cdot \Delta V_{ctotl}\end{aligned}\quad (\text{II.9.14})$$

The general design of the equivalent capacitance is (II.9.15).

$$\begin{aligned}C_{totu} &= \frac{\Delta W_{CU}}{2 \cdot \langle v_{ctotu} \rangle \cdot \Delta V_{ctotu}} \\ C_{totl} &= \frac{\Delta W_{CL}}{2 \cdot \langle v_{ctotl} \rangle \cdot \Delta V_{ctotl}}\end{aligned}\quad (\text{II.9.15})$$

For an M2DC leg, the energy fluctuation has two main frequencies, the fundamental frequency and the second harmonic. To simplify the energy expressions, only the first term of (II.9.9) and (II.9.10) are taken into account.

Substituting the peak to peak value of expressions (II.9.9) and (II.9.10), the formulas of equivalent capacitors are extracted in (II.9.16).

$$C_{totu} = \frac{1}{2 \cdot \langle v_{ctotu} \rangle \cdot \Delta V_{ctotu}} \cdot 2 \cdot \left( \frac{\hat{V}_{mu,ac} \cdot I_{u,dc}}{\omega} + \frac{\sqrt{2}}{2} \cdot \frac{V_{mu,dc} \cdot \hat{I}_{u,ac}}{\omega} \right) \quad (II.9.16)$$

$$C_{totl} = \frac{1}{2 \cdot \langle v_{ctotl} \rangle \cdot \Delta V_{ctotl}} \cdot 2 \cdot \left( -\frac{\hat{V}_{ml,ac} \cdot I_{l,dc}}{\omega} + \frac{\sqrt{2}}{2} \cdot \frac{V_{ml,dc} \cdot \hat{I}_{l,ac}}{\omega} \right)$$

Using the choices made previously and equations (II.5.5) and (II.8.4), (II.9.17) shows the minimum required values for the equivalent capacitances of each arm.

$$C_{totu} \geq \frac{(1-\alpha) \cdot \frac{P1}{M}}{\omega \cdot \langle v_{ctotu} \rangle \cdot \Delta V_{ctotu}} \cdot \left( \frac{\hat{V}_{mu,ac}}{V_{mu,dc}} + 2 \cdot \frac{V_{mu,dc}}{\hat{V}_{mu,ac}} \right) \quad (II.9.17)$$

$$C_{totl} \geq \frac{(1-\alpha) \cdot \frac{P1}{M}}{\omega \cdot \langle v_{ctotl} \rangle \cdot \Delta V_{ctotl}} \cdot \left( \frac{\hat{V}_{ml,ac}}{V_{ml,dc}} + 2 \cdot \frac{V_{ml,dc}}{\hat{V}_{ml,ac}} \right)$$

Since AC voltages depend on the power (II.7.11), the capacitance formula can be rewritten in (II.9.18), where  $\hat{V}_{mu,ac}$  and  $\hat{V}_{ml,ac}$  are substituted by  $P1/M$  using the energy balancing relation (II.6.6). To have the best performance, the choice of  $\theta$ ,  $\hat{V}_{mu,ac} = \hat{V}_{ml,ac}$  and  $Ls \gg l$  are always considered.

$$C_{totu} \geq \frac{(1-\alpha) \cdot \frac{P1}{M}}{\omega \cdot \langle v_{ctotu} \rangle \cdot \Delta V_{ctotu}} \cdot \left( \frac{2 \cdot \sqrt{\frac{P1}{M} \cdot (1-\alpha) \cdot \omega \cdot l}}{V_{mu,dc}} + 2 \cdot \frac{V_{mu,dc}}{2 \cdot \sqrt{\frac{P1}{M} \cdot (1-\alpha) \cdot \omega \cdot l}} \right) \quad (II.9.18)$$

$$C_{totl} \geq \frac{(1-\alpha) \cdot \frac{P1}{M}}{\omega \cdot \langle v_{ctotl} \rangle \cdot \Delta V_{ctotl}} \cdot \left( \frac{2 \cdot \sqrt{\frac{P1}{M} \cdot (1-\alpha) \cdot \omega \cdot l}}{V_{ml,dc}} + 2 \cdot \frac{V_{ml,dc}}{2 \cdot \sqrt{\frac{P1}{M} \cdot (1-\alpha) \cdot \omega \cdot l}} \right)$$

After simplification, the formula of equivalent capacitances is finally as (II.9.19).

$$C_{totu} \geq \frac{\sqrt{\frac{P1}{M} \cdot (1-\alpha) \cdot \omega \cdot l} \cdot \left( 2 \cdot \frac{P1}{M} \cdot (1-\alpha) \cdot \omega \cdot l + (1-\alpha)^2 \cdot V1^2 \right)}{\omega^2 \cdot l \cdot \langle v_{ctotu} \rangle \cdot \Delta V_{ctotu} \cdot (1-\alpha) \cdot V1} \quad (II.9.19)$$

$$C_{totl} \geq \frac{\sqrt{\frac{P1}{M} \cdot (1-\alpha) \cdot \omega \cdot l} \cdot \left( 2 \cdot \frac{P1}{M} \cdot (1-\alpha) \cdot \omega \cdot l + \alpha^2 \cdot V1^2 \right)}{\omega^2 \cdot l \cdot \langle v_{ctotl} \rangle \cdot \Delta V_{ctotl} \cdot \alpha \cdot V1}$$

These expressions conclude that high power increases the value of equivalent capacitances. But increasing the angular frequency ( $\omega$ ) under its limitations helps to reduce the great value of capacitance. Moreover, the capacitance value depends on the voltage ratio, and then to HVDC grids specifications. Therefore, it can be pre-dimensioned

by the formulas (II.9.19), once the specifications of the converter are determined, (power, voltage ratio and one DC voltage). The pre-dimensioning of the equivalent capacitance can be adjusted and validated by simulations of the converter system considering the final value of  $L_s$ .

## II.10 Conclusion

In this chapter, the converter topology has been studied on the base of a leg model, and the leg components design has been approached. M2DC converter is a flexible DC/DC converter thanks to its modular architecture. Especially for high voltage application, its maximum voltage can be easily extended or decreased by adding or suppressing submodules. This is convenient for adapting two HVDC voltages. Multiple legs allow increasing power transmission. Since each leg has a current phase shifted of  $2\pi/M$  with each other, the converter is investigated by one leg study, each leg having the same behavior than the others.

From the static analysis, it is known that this converter is different from conventional low voltage DC/DC converters, as additional AC components are mandatory. Numerous degrees of freedom of AC components make the analysis complex and with a lot of solutions. For this reason, the study shows the limitations of degrees of freedom which are the conditions for a leg to work. These limitations are discussed under our specific choice of equaling amplitudes of AC voltage components of arms with a phase shift of  $\pi/2$  between upper and lower arms. These limitations are useful to show the leg characteristics, its efficiency and to design passive components.

The arm inductance is calculated by fault current rise rate, which is the conventional method for MMC converter. For the capacitance of submodules, the pre-design determines the equivalent capacitance, defined in the average model of arms. The capacitance formula shows the great influence of specifications of the conversion (rated power, voltage ratio, the frequency, etc.).

In conclusion,  $\alpha \geq 0.5$  is convenient for the leg in terms of losses and components sizing. It is not recommended to design and operate the converter for  $\alpha < 0.5$  due to the high current constraints. If operating the converter at  $\alpha < 0.5$  is necessary, the current limitation and  $\alpha_{min}$  must be monitored. The converter global performance is synthesized in Table 8 by the number of submodules, losses, and power transmission capability, according to different voltage ratio  $\alpha$ .

The low number of submodules and low losses shows us the best performance of the converter at  $0.5 < \alpha < \alpha_{max}$ . For  $\alpha_{min} < \alpha < 0.5$ , other converter solutions should be explored and compared in performances.

Furthermore, at  $\alpha > 0.5$ , to differentiate the number of submodules in upper and lower arms, it should be necessary to evaluate the converter losses (semiconductor losses and passive components losses) and to design arm capacitances. This study is not presented in this work, but is necessary to optimize the design of the M2DC converter for a specific voltage ratio according to HVDC networks to be connected. The transmission power decreases when  $\alpha$  increases, but remains consequent when  $\alpha$  is not too far from 1/2.

Table 8 Performance of the converter leg

Voltage ratio	$\alpha_{min} < \alpha < 0.5$	$\alpha = 0.5$	$0.5 < \alpha < \alpha_{max}$
Number of submodules	<b>Low</b>	High	<b>Low</b>
Losses	High	Low	<b>Low</b>
Transmission Power	Low	<b>High</b>	Low

The next chapter proposes to detail the control strategy on M2DC converter, using the investigations of average models and choices on degrees of freedom defined in this chapter.

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# III Converter control strategy and dynamics

## III.1 Introduction

This chapter focuses on the control strategy of the converter, using the model obtained in the previous chapter. The objective is to confirm static behaviors analyzed in the previous chapter and to study dynamic behaviors of the converter.

A great number of capacitors are present in the M2DC converter. The power transferred between the two DC grids involves naturally unbalance between equivalent capacitors or between each submodule capacitors. Therefore, as for the MMC, the main control design is the stability of internal energy stored in equivalent capacitors to secure the converter and to be able to control the DC power transfer. This control is named capacitor energy-based control.

The energy-based control includes two cascaded loops: a current loop which is the inner loop and an energy loop (or voltage loop) which is the outer loop. Since each leg of the converter is expected to act in the same way, with phase-shifted currents, the control presented in this chapter is applicable for any number of legs.

As an operation to decouple the current model is necessary to increase the control precision, this chapter starts with the proposition of a decoupled model using a change of variables. This decoupling changes also the frame of reference used in the previous chapter for the converter model.

Based on the decoupled model, control loops are developed to validate the steady-state analysis of the previous chapter and to get a better comprehension of converter behavior. The study of the converter dynamic performances allows understanding the advantages and disadvantages of the proposed control.

Then, to demonstrate the high voltage and great power endurance, the simulation is explored at the condition of voltage rating and power rating of CIGRE Group (Conseil International des Grands Réseau Electrique).

## III.2 Control architecture

Fig 70 is an overview of the control for a leg. It includes two levels of control:

- high-level control which includes current loop and energy loop
- low-level control which is the Control Balancing Algorithm (CBA).

The high-level control aims to regulate the energy transfer between the two DC grids and the stability of the stored energy in each arm. It gives modulation references to low-level control. The low-level control balances the energy of each submodule in an arm and provides gate signals for each submodule transistor.

This chapter is focused on high-level control. The low-level control (CBA) is not studied here, as the well-studied Nearest Level Control (NLC) developed for the MMC converter



[78]-[81] is used in the M2DC. This algorithm has been studied and used in L2EP laboratory as [82], [83]. Since submodule selection of M2DC converter is the same as the MMC, NLC algorithms developed for MMC is applied for the M2DC. This submodule selection limits high switching frequency in high voltage high power systems compared to PWM control [84].

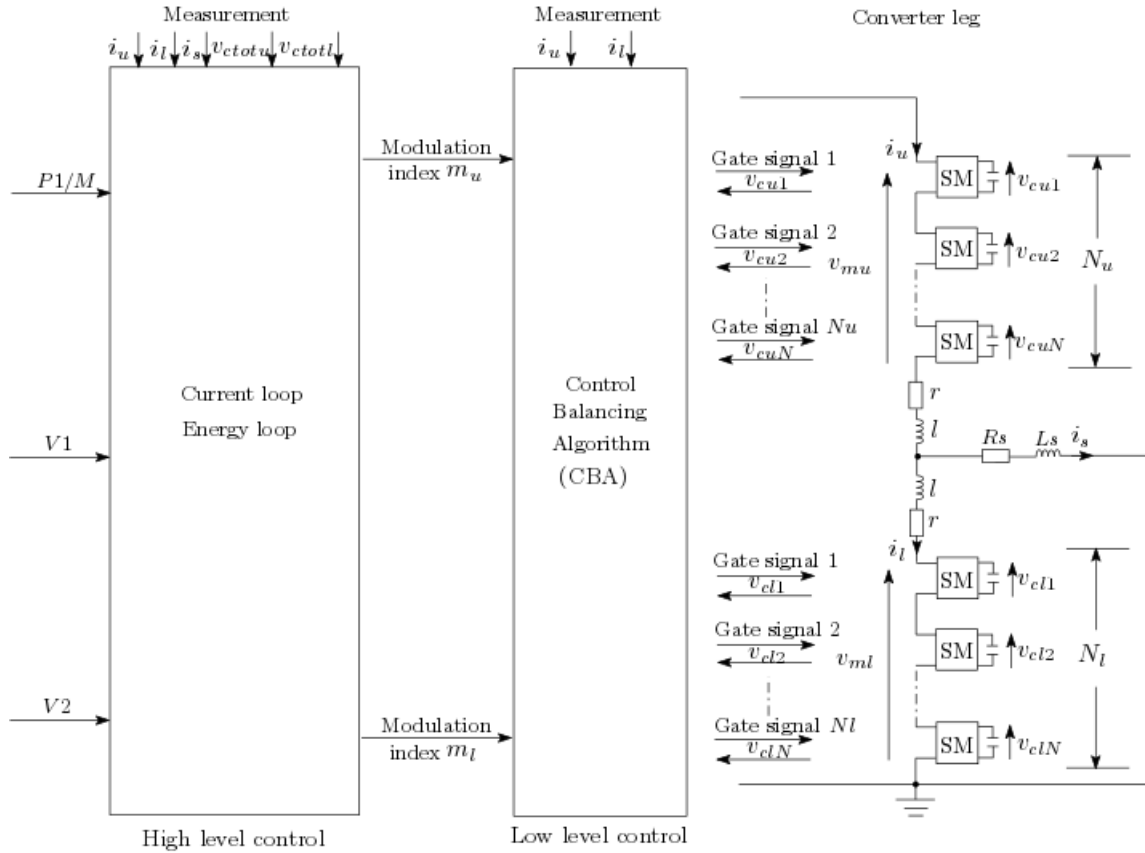


Fig 70. Overview of energy based control for a leg

The high-level control is designed by reversing the average converter model. This implies that Control Balancing Algorithm (CBA) is supposed to work well. The control has a classical cascade structure built with an energy loop and an internal current loop (Fig 71).

The energy loop aims to balance the energy of the upper and lower arm and give references to the current loop. The target is the average value of capacitor voltage obtained by filtering voltage measurements. A low pass filter is therefore presented for measurements of total arm voltage signals  $v_{ctotu}$  and  $v_{ctotl}$ .

The current loop regulates arm currents which include DC and AC components. Both components of each current are controlled by one controller instead of two different controllers since the controller design is the same for each component. Outputs of the current loop are the two modulation indexes sent directly to the low-level control.

As presented in the previous chapter, the frequency and phase of AC components are degrees of freedom for the control of M2DC. The converter does not need Phase-Locked Loop (PLL) controllers to synchronize its AC components to any signals. Therefore

frequency and phase of AC currents of Fig 71 are imposed independently. Their values are designed and based on investigations and choices detailed in the previous chapter.

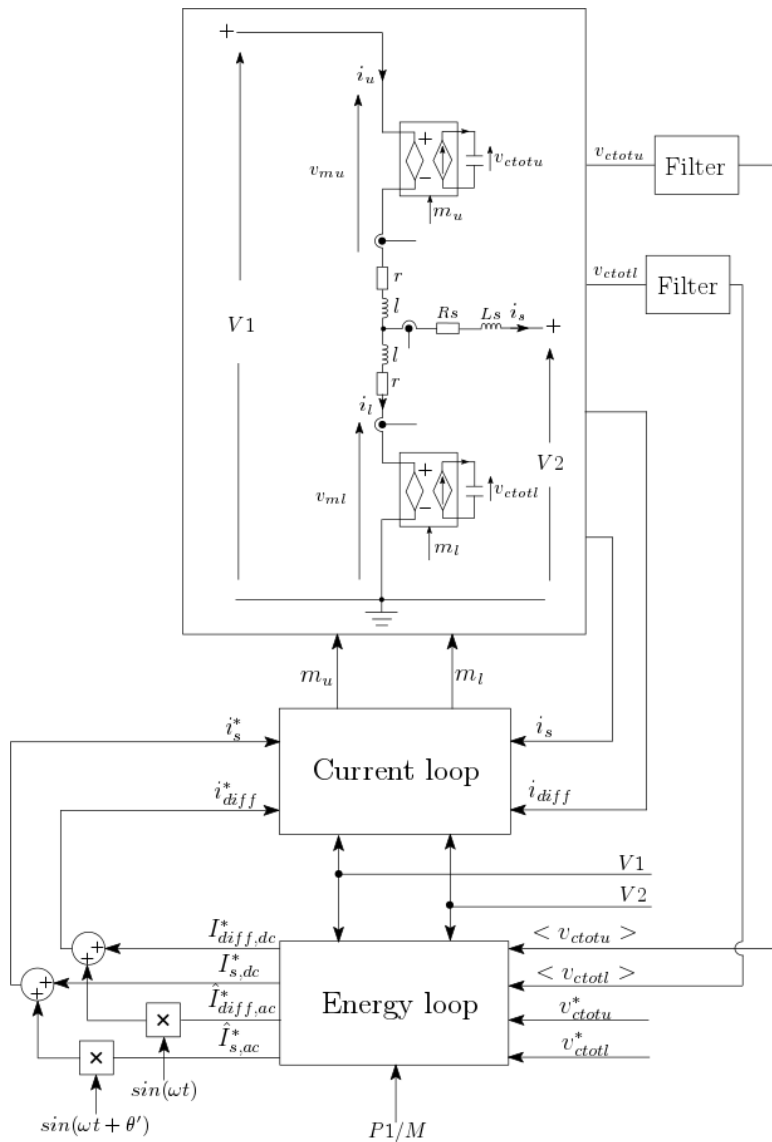


Fig 71. High-level control and average model of M2DC leg

### III.3 Decoupling average current model

A decoupling method allows controlling currents independently but needs to change the controlled variables. This method is already used to design the current control loop of the MMC converter [85]-[86]. M2DC converter has a current model similar than the MMC, also the same decoupling method is applied.

### III.3.1 Decoupled average model

#### III.3.1.1 Change of variables

To control currents of the upper arm and the lower arm, it requires that both currents are independent. However, depending on the current model (III.3.1) obtained from the previous chapter, the two arms currents are coupled by  $v_{mu}$  and  $v_{ml}$ . The coupled terms make impossible to obtain the control design by reversing model (Fig 72), and a decoupling method is therefore necessary.

$$\begin{aligned} \frac{di_u}{dt} &= -\frac{Ls+l}{(2 \cdot Ls+l) \cdot l} \cdot v_{mu} - \frac{Ls}{(2 \cdot Ls+l) \cdot l} \cdot v_{ml} + \frac{Ls+l}{(2 \cdot Ls+l) \cdot l} \cdot V1 - \frac{1}{2 \cdot Ls+l} \cdot V2 \\ \frac{di_l}{dt} &= -\frac{Ls}{(2 \cdot Ls+l) \cdot l} \cdot v_{mu} - \frac{Ls+l}{(2 \cdot Ls+l) \cdot l} \cdot v_{ml} + \frac{Ls}{(2 \cdot Ls+l) \cdot l} \cdot V1 + \frac{1}{2 \cdot Ls+l} \cdot V2 \end{aligned} \quad (III.3.1)$$

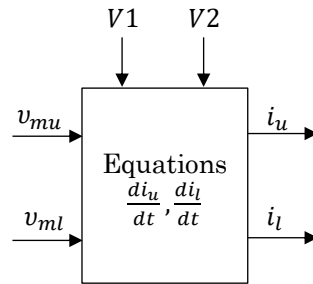


Fig 72. Coupled current model

The change of variables is described in (III.3.2) [85]-[86]:

$$\begin{aligned} v_{diff} &= \frac{v_{mu} + v_{ml}}{2} \\ v_v &= \frac{v_{mu} - v_{ml}}{2} \\ i_{diff} &= \frac{i_u + i_l}{2} \\ i_s &= i_u - i_l \end{aligned} \quad (III.3.2)$$

This method changes the control target from the state variables  $i_u$  and  $i_l$  to the state variables  $i_{diff}$  and  $i_s$ , where  $i_{diff}$  and  $i_s$  are two decoupled currents. They can be regulated independently unlike  $i_u$  and  $i_l$ .

Arm voltages  $v_{mu}$ ,  $v_{ml}$  are changed to  $v_{diff}$ ,  $v_v$ .

$v_{diff}$  is the average voltage of the upper arm and lower arm.  $v_v$  is half of the voltage difference between the upper and the lower arm.

$i_{diff}$  is the average current of the upper and lower arm, and  $i_s$  is the current in the middle branch.

### III.3.1.2 Decoupled average model

Thanks to the change of variables, the model (III.3.1) is separated into two independent models (III.3.3) and (III.3.4) by summing and subtracting equations of (III.3.1).

$$\frac{di_{diff}}{dt} = -\frac{1}{l} \cdot v_{diff} + \frac{1}{2 \cdot l} \cdot V1 \quad (III.3.3)$$

$$\frac{di_s}{dt} = -\frac{2}{2 \cdot Ls + l} \cdot v_v + \frac{1}{2 \cdot Ls + l} \cdot V1 - \frac{2}{2 \cdot Ls + l} \cdot V2 \quad (III.3.4)$$

Each model represents a subsystem. “Subsystem  $i_{diff}$ ” has the state variable  $i_{diff}$  (III.3.3), whereas the “subsystem  $i_s$ ” has the state variable  $i_s$  (III.3.4).

Both decoupled current models and change of variables are shown in Fig 73.

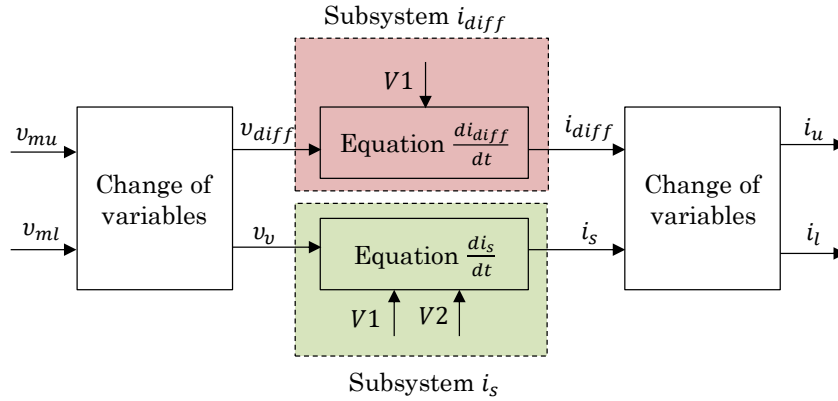


Fig 73. Decoupled current model of M2DC leg

These subsystems can also be represented in circuits (Fig 74), where DC and AC components are included in each circuit. In the subsystem  $i_{diff}$  (Fig 74.(a)), DC source  $V1/2$  provides powers to  $v_{diff}$  and an equivalent inductor  $l$ . For the subsystem  $i_s$  (Fig 74.(b)), DC source  $(V1/2 - V2)$  creates current  $i_s$  in the circuit of serial elements of  $v_v$  and an equivalent inductor  $(Ls + l/2)$ . This circuit representation (Fig 74) is helpful in the next sections to define the current-voltage phase-shift.



Fig 74. (a) Average model of the subsystem  $i_{diff}$ , (b) Average model of the subsystem  $i_s$

### III.3.2 Steady state analysis of variables

This part analyzes the DC and AC component of each variable in the steady state. These two components are described in the relation (III.3.5)

$$\begin{aligned}
 v_{diff} &= V_{diff,dc} + v_{diff,ac} \\
 v_v &= V_{v,dc} + v_{v,ac} \\
 i_{diff} &= I_{diff,dc} + i_{diff,ac} \\
 i_s &= I_{s,dc} + i_{s,ac}
 \end{aligned}
 \tag{III.3.5}$$

where:

DC components are described with subscript DC as  $V_{diff,dc}$ ,  $V_{v,dc}$ ,  $I_{diff,dc}$  and  $I_{s,dc}$ .

AC components with average value zero are described with subscript AC as  $v_{diff,ac}$ ,  $v_{v,ac}$ ,  $i_{diff,ac}$  and  $i_{s,ac}$ .

#### III.3.2.1 DC components of decoupled variables

Each leg of the M2DC converter is controlled to share equally currents of DC grids.

$$\begin{aligned}
 I_{u,dc} &= \frac{P1}{V1 \cdot M} \\
 I_{s,dc} &= \frac{P2}{\alpha \cdot V1 \cdot M}
 \end{aligned}
 \tag{III.3.6}$$

The lower arm sees the difference of current through the upper arm and the middle branch.

$$I_{l,dc} = \frac{1}{V1} \cdot \left( \frac{P1}{M} - \frac{P2}{\alpha \cdot M} \right)
 \tag{III.3.7}$$

Therefore, for the decoupled variables, DC components are defined in (III.3.8) in the steady state.

$$\begin{aligned}
 I_{diff,dc} &= \frac{1}{V1} \cdot \left( \frac{P1}{M} - \frac{P2}{2 \cdot \alpha \cdot M} \right) \\
 I_{s,dc} &= \frac{P2}{\alpha \cdot V1 \cdot M}
 \end{aligned}
 \tag{III.3.8}$$

At a certain voltage ratio  $\alpha$ ,  $I_{s,dc}$  defines power  $P2$ , which is the output power (on DC voltage  $V2$ ).  $I_{diff,dc}$  regulates the difference of grid power (or current) between  $P1$  and  $P2/2$ . If  $P2$  is ensured by  $I_{s,dc}$ , controlling  $I_{diff,dc}$  means regulating  $P1$ . Current  $I_{s,dc}$  indicates also the converter power direction according to its sign.

In another way, DC currents ( $I1/M$  and  $I2/M$ ) are obtained as (III.3.9).

$$\begin{aligned}\frac{I1}{M} &= I_{diff,dc} - \frac{I2}{M} \\ \frac{I2}{M} &= I_{s,dc}\end{aligned}\tag{III.3.9}$$

Notably, the current  $I1/M$  depends on  $I2/M$ , which is different from the MMC.

Such as DC currents, DC component voltages of decoupled variables are shown in (III.3.10), where  $V_{diff,dc}$  is half of voltage  $V1$  and independent of  $\alpha$ .

$$\begin{aligned}V_{diff,dc} &= \frac{V1}{2} \\ V_{v,dc} &= V1 \cdot \left(\frac{1}{2} - \alpha\right)\end{aligned}\tag{III.3.10}$$

In another way, the voltages ( $V1$  and  $V2$ ) can be explained as (III.3.11).

$$\begin{aligned}V1 &= 2 \cdot V_{diff,dc} \\ V2 &= \frac{V1}{2} - V_{v,dc}\end{aligned}\tag{III.3.11}$$

### III.3.2.2 AC components of decoupled variables

The previous chapter has shown the AC component of coupled variables in the phasor diagram. This part explains the AC components in the decoupled forms in the phasor domain by (III.3.12) in Fig 75 to show their relation.

$$\begin{aligned}\underline{V}_{diff,ac} &= \frac{\underline{V}_{mu,ac} + \underline{V}_{ml,ac}}{2} \\ \underline{V}_{v,ac} &= \frac{\underline{V}_{mu,ac} - \underline{V}_{ml,ac}}{2} \\ \underline{I}_{diff,ac} &= \frac{\underline{I}_{u,ac} + \underline{I}_{l,ac}}{2} \\ \underline{I}_{s,ac} &= \underline{I}_{u,ac} - \underline{I}_{l,ac}\end{aligned}\tag{III.3.12}$$

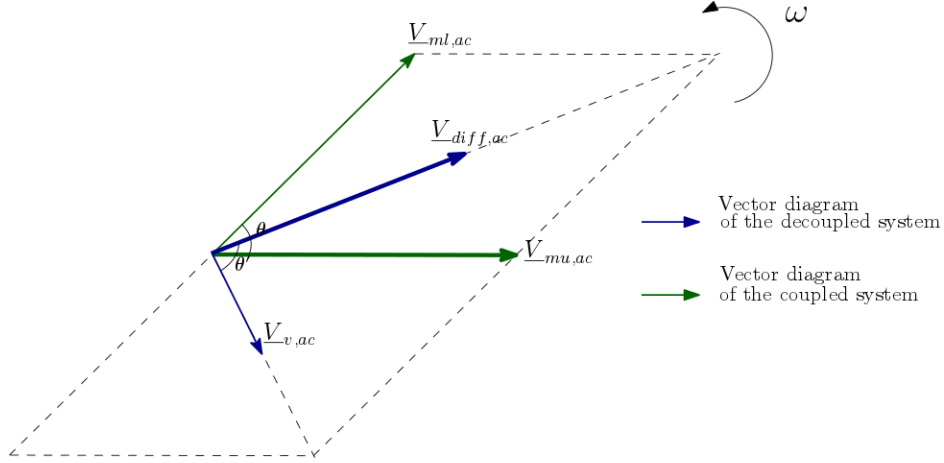


Fig 75. AC voltages in the phasor diagram

The coupled and decoupled variables create two frames of reference phase shifted. The frame of reference created by coupled variables (green) considers  $\underline{V}_{\mu,ac}$  as origin, whereas frame of reference (blue) created by decoupled variables,  $\underline{V}_{diff,ac}$  is considered as the reference (III.3.13).

$$\underline{V}_{diff,ac} = \hat{V}_{diff,ac} \cdot e^{j \cdot 0} \quad (III.3.13)$$

Depending on Fig 75,  $\underline{V}_{ml,ac}$  leads  $\underline{V}_{\mu,ac}$  with an angle  $\theta$  in the coupled frame of reference.  $\underline{V}_{v,ac}$  lags  $\underline{V}_{diff,ac}$  with an angle  $\theta'$  in the decoupled frame of reference (III.3.14).  $\theta'$  is the phase shift between  $\underline{V}_{diff,ac}$  and  $\underline{V}_{v,ac}$ .

$$\underline{V}_{v,ac} = \hat{V}_{v,ac} \cdot e^{-j \cdot \theta'} \quad (III.3.14)$$

Decoupled currents are therefore described by voltage and impedance in (III.3.15). Depending on the sign convention defined in Fig 74, AC currents lead AC voltages with angle  $\varphi_1, \varphi_2$ .

$$\begin{aligned} \underline{I}_{diff,ac} &= -\frac{\hat{V}_{diff,ac}}{l \cdot \omega} \cdot e^{-j \cdot \varphi_1} \\ \underline{I}_{s,ac} &= -\frac{2 \cdot \hat{V}_{v,ac}}{(l + 2 \cdot Ls) \cdot \omega} \cdot e^{-j \cdot (\theta' + \varphi_2)} \end{aligned} \quad (III.3.15)$$

$\varphi_1$  is the phase between  $i_{diff,ac}$  and  $v_{diff,ac}$ . It has the value of  $\arctg\left(\frac{l \cdot \omega}{r}\right)$ .

$\varphi_2$  is the phase between  $i_{s,ac}$  and  $v_{v,ac}$  with the value of  $\arctg\left(\frac{(l+2 \cdot Ls) \cdot \omega}{r+2 \cdot Rs}\right)$ .

Generally,  $l \cdot \omega$  is greater than the internal resistance  $r$  which can be ignored. Both angles  $\varphi_1$  and  $\varphi_2$  can be approximated to  $90^\circ$ . Expressions of current (III.3.15) are therefore described in (III.3.16).

$$\begin{aligned}
I_{diff,ac} &= -\frac{\hat{V}_{diff,ac}}{l \cdot \omega} \cdot e^{-j \cdot \frac{\pi}{2}} \\
I_{s,ac} &= -\frac{\hat{V}_{v,ac}}{\left(\frac{l}{2} + Ls\right) \cdot \omega} \cdot e^{-j \cdot \left(\theta' + \frac{\pi}{2}\right)}
\end{aligned} \tag{III.3.16}$$

### III.4 Current loop design

The current loop aims to control arms currents of the converter and confirm the static analysis of the previous chapter. Advantages and disadvantages of the proposed control are also analyzed.

Each current consists of DC and AC components and each current loop uses only one controller (PI proportional integral) to regulate both components because AC components are difficult to be extracted by a simple filter. A short cutoff frequency of the filter can disrupt the stability of the system.

#### III.4.1 Continuous time transfer functions

As switching frequency of the converter is high enough, transfer functions are established in continuous time by using average current model (III.3.3) and (III.3.4),

(III.4.1) is the decoupled current models of DC component.

$$\begin{aligned}
\frac{dI_{diff,dc}}{dt} &= -\frac{1}{l} \cdot V_{diff,dc} + \frac{1}{2 \cdot l} \cdot V1 \\
\frac{dI_{s,dc}}{dt} &= -\frac{2}{2 \cdot Ls + l} \cdot V_{v,dc} + \frac{1}{2 \cdot Ls + l} \cdot V1 - \frac{2}{2 \cdot Ls + l} \cdot V2
\end{aligned} \tag{III.4.1}$$

(III.4.2) is the decoupled current models of AC component.

$$\begin{aligned}
\frac{di_{diff,ac}}{dt} &= -\frac{1}{l} \cdot v_{diff,ac} \\
\frac{di_{s,ac}}{dt} &= -\frac{2}{2 \cdot Ls + l} \cdot v_{v,ac}
\end{aligned} \tag{III.4.2}$$

This current system is shown in Fig 76 where Fig 76. (a) and (b) concern about DC and AC component current, respectively. DC currents are independent of AC component currents. However, (III.4.1) and (III.4.2) show a similarity of two components model (with a difference of disturbance in the DC current model).

$\left(\frac{1}{2 \cdot l} V1\right)$  is the disturbance in the DC subsystem  $i_{diff}$ .

$\left(\frac{1}{2 \cdot Ls + l} V1 - \frac{2}{2 \cdot Ls + l} \cdot V2\right)$  is the disturbance in the DC subsystem  $i_s$ .

Therefore, the same controller is used considering compensation for each disturbance.



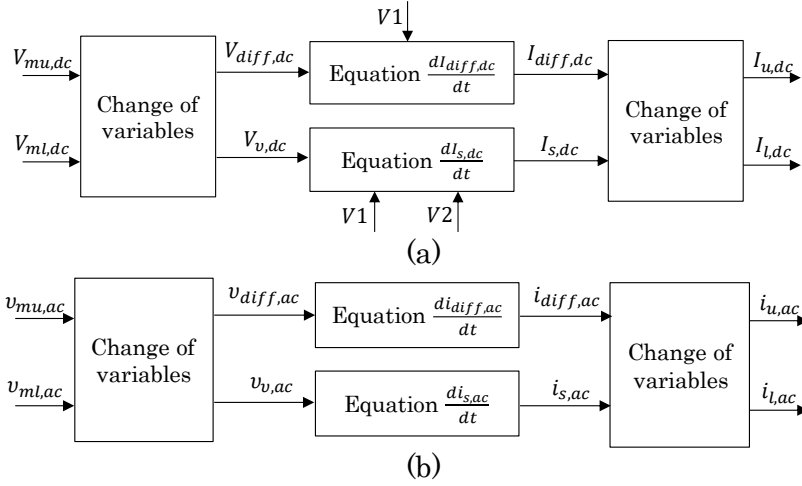


Fig 76. (a) Decoupled average model of DC component of currents, (b) decoupled average model of AC component of currents

Two transfer functions are obtained in (III.4.3) instead of four for each component current. They are used for the current loop controllers design by reversing these transfer functions.

$$\begin{aligned}
 H_{diff}(s) &= \frac{I_{diff}}{V_{diff}} = \frac{1}{l \cdot s} \\
 H_s(s) &= \frac{I_s}{V_v} = \frac{1}{\left(Ls + \frac{l}{2}\right) \cdot s}
 \end{aligned}
 \tag{III.4.3}$$

where  $H_{diff}(s)$  is the transfer function of the subsystem  $i_{diff}$  and  $H_s(s)$  is the transfer function of the subsystem  $i_s$ .

### III.4.2 PI controller and closed current loop

Several types of the controller have been used in the literature to control the MMC converter, such as P, PI, PID (proportional-integral-derivative) and PR (proportional-resonant) [57]. P controller is firstly avoided in this work to reduce errors in steady state. PID and PR controller are not used in our approach, due to their complexity. Finally, a PI controller (Fig 77) is adopted for its simplicity, as current subsystems are first-order systems (III.4.3).

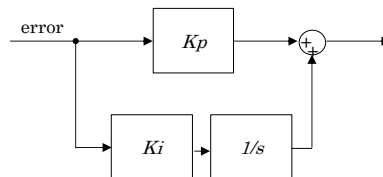


Fig 77. PI controller form

Depending on the basic feedback control system Fig 78, open loop transfer functions (FTBOs) are the product of controller function and currents system transfer functions (III.4.4).

$$FTBO(s) = \left( Kp + \frac{Ki}{s} \right) \cdot H(s) \quad (III.4.4)$$

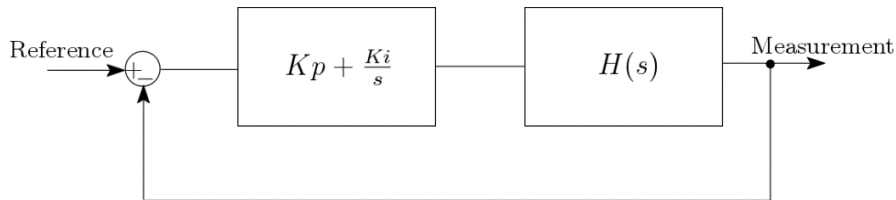


Fig 78. The basic feedback control system

Replacing the transfer functions (III.4.3) in (III.4.4), the open loop transfer functions of the two current subsystems are obtained in (III.4.5).

$$\begin{aligned} FTBO_{diff}(s) &= \left( Kp + \frac{Ki}{s} \right) \cdot \frac{1}{l \cdot s} \\ FTBO_s(s) &= \left( Kp + \frac{Ki}{s} \right) \cdot \frac{1}{\left( Ls + \frac{l}{2} \right) \cdot s} \end{aligned} \quad (III.4.5)$$

where  $FTBO_{diff}$  is the open loop transfer function for subsystem  $i_{diff}$ ,  $FTBO_v$  is the open loop transfer function for subsystem  $i_s$ .

The closed loop transfer functions (FTBFs) are calculated in (III.4.6).

$$\begin{aligned} FTBF_{diff}(s) &= \frac{FTBO_{diff}(s)}{1 + FTBO_{diff}(s)} = \frac{Kp \cdot s + Ki}{l \cdot s^2 + Kp \cdot s + Ki} \\ FTBF_s(s) &= \frac{FTBO_s(s)}{1 + FTBO_s(s)} = \frac{Kp \cdot s + Ki}{\left( Ls + \frac{l}{2} \right) \cdot s^2 + Kp \cdot s + Ki} \end{aligned} \quad (III.4.6)$$

where  $FTBF_{diff}$  is the closed loop transfer function of  $i_{diff}$ .  $FTBF_s$  is the closed loop transfer function of  $i_s$ .

A null steady state error is impossible to obtain to track a sine signal with a PI controller.

As currents  $i_{diff}$  and  $i_s$  are not constant variables, their AC components ( $\omega \neq 0$ ) bring steady state errors to the closed current system. These errors generally create a delay in sinusoidal signals.

To reduce/eliminate this delay, several solutions are possible:

- Decoupling DC and AC components with AC components controlled using DQ transformation by PI controller. The difficulty of this solution is to filter the current measurement without disturbing the stability of the system.
- Changing the PI to the PR controller, which is not the objective of the thesis.
- Reducing the response time of the PI controller. This solution cannot eliminate the delay as the two other solutions but only reduce the delay. Thanks to nowadays technology, DSP or FPGA are able to provide high-speed calculation to satisfy the requirement of the controller. Thus, response time is minimized and produces a reduced delay.

The control block using the PI controller with minimized response time is detailed in Fig 79. It is obtained by reversing the decoupled currents model (Fig 73) and adding the compensations for each disturbance.

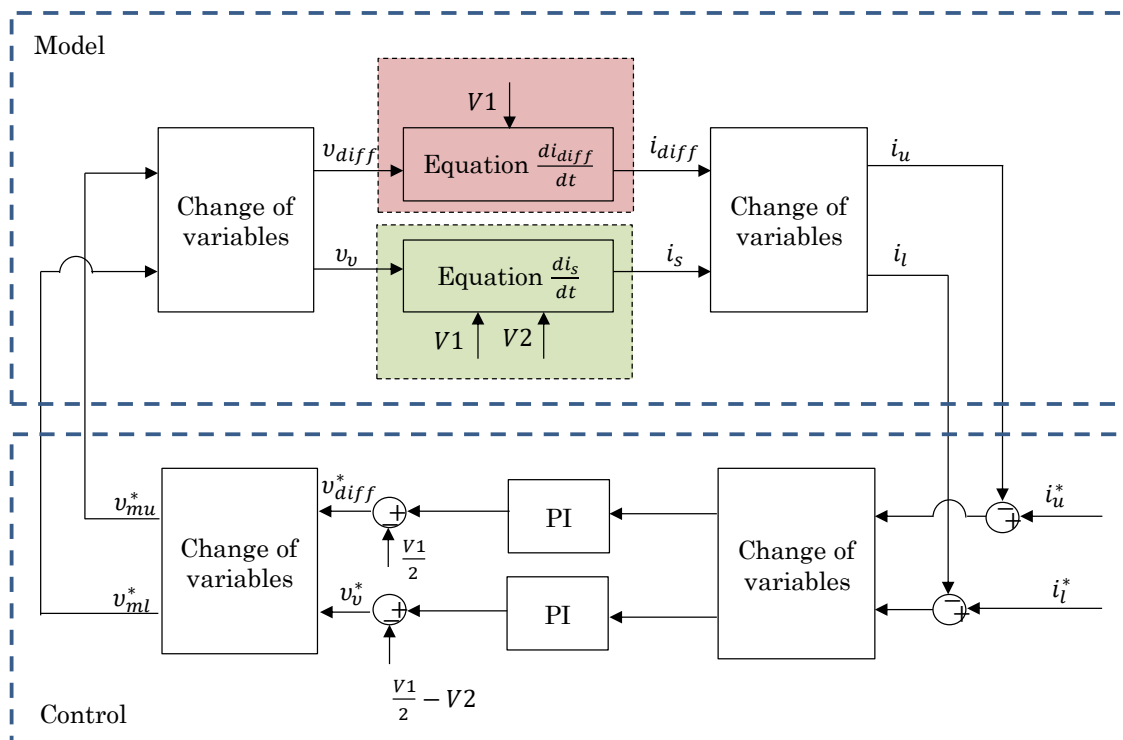


Fig 79. Closed current loop of the M2DC leg

### III.4.3 Static and dynamic analysis of the closed current loop

#### III.4.3.1 Parameters selection of controllers

PI controllers are designed by pole placement method (or full state feedback). Then, placing closed-loop poles allows obtaining the desired response of the system.

Closed current systems (III.4.6) are expected to follow the canonical form  $G(s)$  of second order system (III.4.7):

$$G(s) = \frac{K \cdot \omega_n^2}{s^2 + 2 \cdot \xi \cdot \omega_n \cdot s + \omega_n^2} \quad (\text{III.4.7})$$

where  $\xi$  is the damping ratio.  $\omega_n$  is the natural angular frequency, defined as the oscillate angular frequency that the system is not damped.

To have the minimum response time,  $\xi$  is selected at 0.7 with acceptable overshoot. (III.4.8) describes response time in terms of natural frequency.

$$Tr = \frac{3}{\omega_n} \quad (\text{III.4.8})$$

### III.4.3.2 Static performances of the current loop – CIGRE test case

Static performances of the current loop are shown by simulating the closed current loop in Matlab Simulink. Simulation conditions are referred to the CIGRE group test scenario with *a rated power of 600MW and a rated DC grid voltage (V1/V2) 320kV/250kV*.

- Converter parameter design

To test the current loop, four parameters must be defined in the current model: arm inductance, secondary inductance, operating frequency, and leg number.

Since the converter transmits a high rated power, simulations use three legs instead of two legs in order to share the power and reduce the leg current stress. Thus, the rated power of each leg is around 200MW.

Depending on the analysis of the second chapter, arm inductance is designed to reduce the gradient of fault current. At the condition of DC voltage 320kV, fault current rise rate should be under  $6.4 \cdot 10^6$  A/s. The minimum arm inductance is the value of (II.9.4).

$$l \geq \frac{V1}{2 \cdot \frac{\Delta i_l}{\Delta t}} = \frac{320 \cdot 10^3}{2 \cdot 6.4 \cdot 10^6} = 25mH \quad (\text{III.4.9})$$

The simulation uses this minimum value to avoid large inductor volume.

With the determined arm inductance, the secondary inductance  $L_s$ , which should be greater than arm inductance is set to 250mH to be ten times greater than  $l$ . This inductance value can be changed in the future, according to an optimal design or technological constraints.

Depending on the rated DC voltages (320kV/250kV), the maximum amplitude of AC voltage using half-bridge submodule is shown in Fig 80 according to control choices of the previous chapter. This 70kV maximal AC voltage value considers that both arms have the same AC voltages and phase shifted  $90^\circ$ .

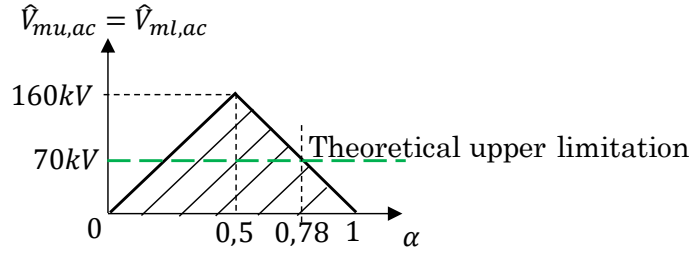


Fig 80. CIGRE test case maximum AC voltage

With the determined rated power, the maximum frequency of the converter, limited by AC voltage, is shown in Fig 81. At  $\alpha = 0.78$ , upper limitation of frequency is 174Hz (green dashed line). Comparing to the maximum experimental frequency 350Hz in high voltage high power applications (red dashed line), the theoretical limitation of 174Hz is a realizable frequency.

Thus, the test (blue dot) is simulated at 100Hz with a security margin in AC voltage.

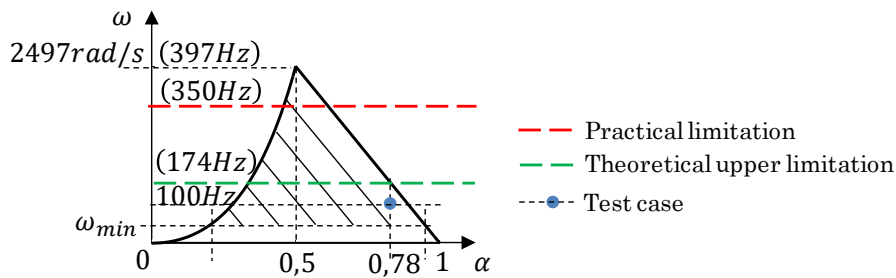


Fig 81. CIGRE test case frequency limitations

In the average model of current, the capacitance of submodule is considered great enough that arm voltages  $v_{mu}$  and  $v_{ml}$  can be considered as voltage sources. Therefore, ripples of capacitor voltages are not taken into account in the current loop.

Table 6 concludes tested parameters of the simulation.

Table 9 M2DCParameters for CIGRE test case

Number of legs	3
Operating frequency	100Hz
Arm inductance $l$	25mH
Secondary inductance $L_s$	250mH

Knowing these parameters, minimum AC currents can be estimated (Fig 82). At  $\alpha = 0.78$ , the theoretical lower limitation of AC currents is  $2 \cdot \sqrt{2}$  times of DC current of a leg. It considers that AC voltages reach the upper limitation. In the test case, AC voltage does not reach its limitation, then AC current will be greater than the minimal value (green dashed line in Fig 82).

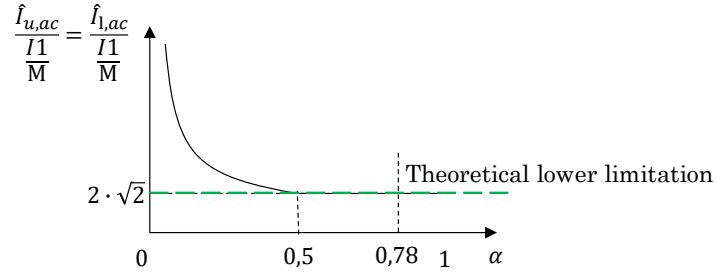


Fig 82. Prediction of AC current minimal values

- PI controller parameters

PI controllers (Table 10) are calculated to have a damping ratio of 0.7. Response time is set to 1ms. This response time is selected to be 10 times faster than the operation period of the converter (10ms) to have minimum steady-state errors.

Table 10 Current controller parameters

	$i_{diff}$ loop	$i_s$ loop
$Kp$	104.9	2152
$Ki$	$0.2 \cdot 10^6$	$4.6 \cdot 10^6$

- Validation of controller parameters and steady-state response

Simulations are realized with a sample time of  $60\mu s$ . The two closed loops of  $i_{diff}$  and  $i_s$  are tested to track their reference.

Since it is difficult to show the response time, then to validate controller parameters with DC and AC references, Fig 83 concerns only DC components with two events. The simulation (red line) tracks the references (blue line) for these two events:

At  $t = 5s$ , the reference of  $i_{diff,dc}$  is increased by 30%.

At  $t = 5s$ , the reference of  $i_{s,dc}$  is increased by 10%.

Overshoots are due to the damping ratio of 0.7. The response time is confirmed around  $Tr = 1ms$ . The system takes a duration of maximum 2ms to reach its steady state. Therefore controller parameters are validated for the DC component.

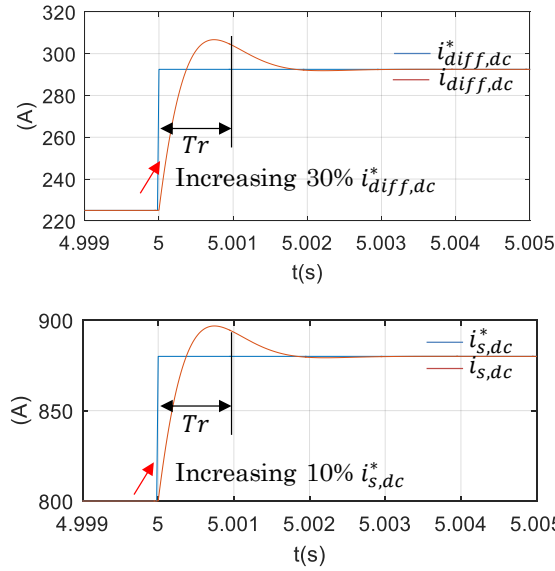


Fig 83. Step response of  $i_{diff,dc}$  and  $i_s$  ( $Tr = 1ms, \xi = 0.7$ )

The same controllers are used for DC and AC components. Simulation results are shown in Fig 84.

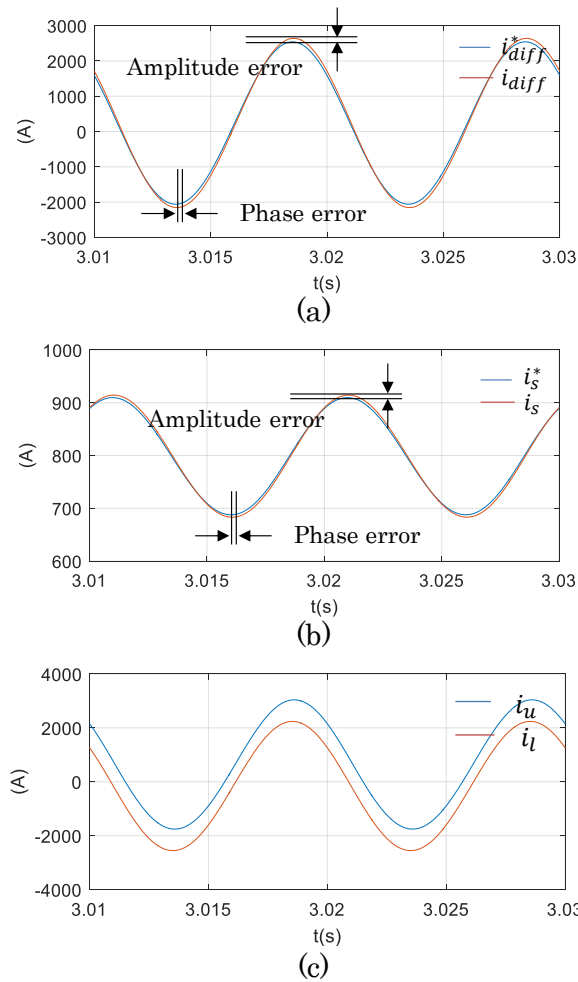


Fig 84. (a)  $i_{diff}$  (b)  $i_s$  (c)  $i_u$  and  $i_l$  of a leg

References and measurements of two currents Fig 84. (a) and (b) are almost overlapping. It can be concluded that parameters of the controllers are set well enough, as steady-state errors are minimized. Fig 84. (c) shows the real coupled currents.

These minimized errors are invisible in the real currents (two arms currents are in phase). If  $Tr$  is shortened, the stability of the system can be disturbed. Therefore, tracking a sine wave with a PI controller needs a compromise between steady state errors and the system stability.

### III.4.3.3 Dynamic performance of the current loop

The dynamic performance of PI controllers is shown in Fig 85 with two current components introducing step events at each current and each component. Each event is imposed independently with sufficient time to get the steady state. Then the interaction between systems is not considered.

At  $t = 5s$ , the reference of the DC component of  $i_{diff}$  is increased by 30%.

At  $t = 5.05s$ , the reference of the DC component of  $i_s$  is increased by 5%.

At  $t = 5.1s$ , the reference of AC component of  $i_{diff}$  is increased by 5%.

At  $t = 5.15s$ , the reference of AC component of the current  $i_s$  is increased by 5%.

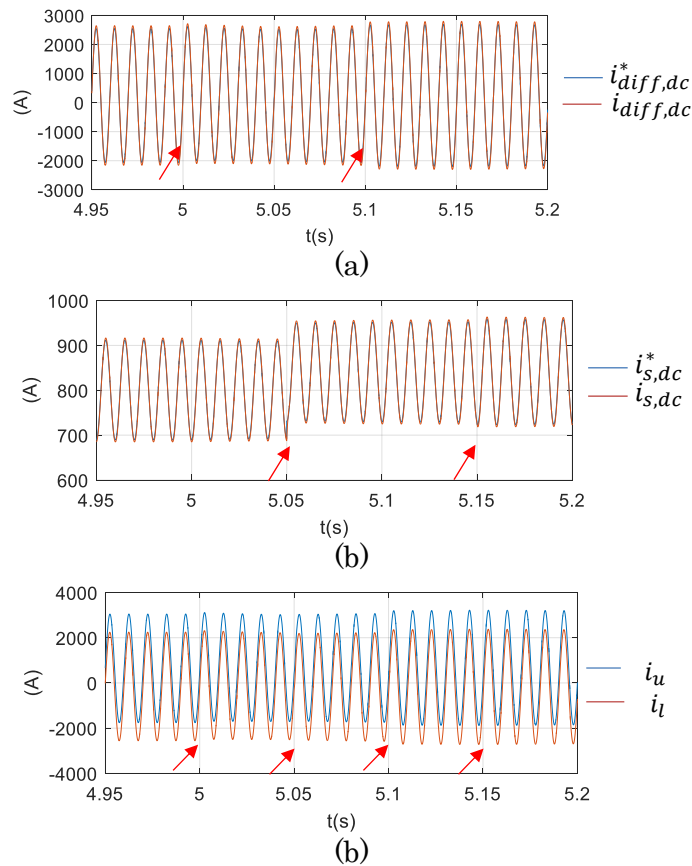


Fig 85. (a) Dynamic performance of  $i_{diff}$  (b) dynamic performance of  $i_s$   
(c) current  $i_u$  and  $i_l$



The two currents  $i_{diff}$  and  $i_s$  are decoupled with independent components. A change in one of the four elements does not disturb the others (Fig 85.(a) and (b)). The real currents  $i_u$  and  $i_l$  (Fig 85.(c)) show equally influences of disturbance in the decoupled currents  $i_{diff}$  and  $i_s$ . Due to the great value of AC components, influences of disturbance in DC (at  $t = 5s$  and at  $t = 5.05s$ ) are less visible than AC one (at  $t = 5.1s$  and at  $t = 5.15s$ ). The delay due to the PI controller is more evident for the decoupled currents ( $t = 5.05s$ ), if the reference changes greatly. This change is almost not visible in real currents, but it influences their stability. In another way, if a rough step occurs in one of the references, the amplified transient error could interrupt the stability of the system.

To conclude, according to the results Fig 85, the tuned parameters of the controllers respect the compromise that the system has a correct static performance and good dynamic without disturbing system stability. It can be noticed that a rough disturbance influences the system stability.

### III.5 Energy model

The energy stored in an arm is the energy stored in an equivalent capacitor depending on the arm average model. To control the internal energy of the converter, it is mandatory to build the energy model. Then the control loop is obtained by reversing the model. The aim of this section is to establish the energy model using decoupled variables and the average model.

#### III.5.1 Energy definition

For the M2DC, each leg can be considered as a container of capacitors in which the internal energy is conserved. Energy charging or discharging is such as put in or take out energy from this reservation. Therefore, the stored energy is used to balance the input and output power and to balance the energy and capacitors voltages of the upper arms and lower arm.

In Fig 86, the energy of a leg is divided into two parts which are the energy of the upper arm  $W_{CU}$  on the left side and the energy of the lower arm  $W_{CL}$  on the right side. These two energy are expressed in (III.5.1) and (III.5.2), respectively.

$W_{CU}$  is the total energy of all capacitors of an upper arm

$$W_{CU} = \sum_{x=1}^{N_u} W_x = \frac{1}{2} \cdot C_{totu} \cdot v_{ctotu}^2 \quad (III.5.1)$$

where  $W_x$  is the energy stored in each capacitor of the upper arm.

$W_{CL}$  is the total energy of all capacitors of a lower arm.

$$W_{CL} = \sum_{y=1}^{N_l} W_y = \frac{1}{2} \cdot C_{totl} \cdot v_{ctotl}^2 \quad (\text{III.5.2})$$

where  $W_y$  is the energy stored in each capacitor of the lower arm.

The “sum of energy”, which is the total stored energy in both arms, noted as  $W_c^\Sigma$ . It indicates the energy of a leg. The “difference of energy”, which is the subtraction of stored energy in both arms, noted as  $W_c^\Delta$  (III.5.3). It indicates the energy fluctuation between upper and lower arm.

$$\begin{aligned} W_c^\Sigma &= W_{CU} + W_{CL} \\ W_c^\Delta &= W_{CU} - W_{CL} \end{aligned} \quad (\text{III.5.3})$$

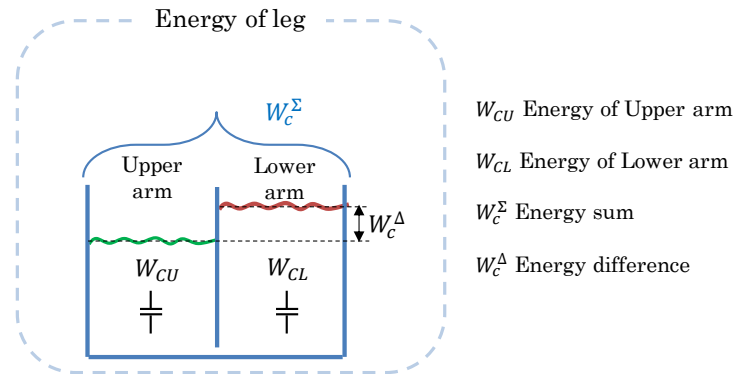


Fig 86. Energy definition in a leg

### III.5.2 Energy model

The upper and lower arm energy evolutions are described by their power expressions (III.5.4). The previous chapter has proposed to add AC components in arm voltages to balance the energy. Power expressions (III.5.4) contain, therefore, a part provided by the DC component and another part provided by the AC component. Its average value indicates the energy stability. The charging and discharging situations of capacitors appear on their ripples.

$$\begin{aligned} \frac{dW_{CU}}{dt} &= i_u \cdot v_{mu} = (v_{diff} + v_v) \cdot \left( i_{diff} + \frac{i_s}{2} \right) \\ \frac{dW_{CL}}{dt} &= i_l \cdot v_{ml} = (v_{diff} - v_v) \cdot \left( i_{diff} - \frac{i_s}{2} \right) \end{aligned} \quad (\text{III.5.4})$$

To simplify the calculation of (III.5.4), the energy model (Fig 87) uses the sum and difference power forms (III.5.5).

$$\begin{aligned}\frac{dW_c^\Sigma}{dt} &= \frac{dW_{cu}}{dt} + \frac{dW_{cl}}{dt} = 2 \cdot v_{diff} \cdot i_{diff} + v_v \cdot i_s \\ \frac{dW_c^\Delta}{dt} &= \frac{dW_{cu}}{dt} - \frac{dW_{cl}}{dt} = v_{diff} \cdot i_s + 2 \cdot v_v \cdot i_{diff}\end{aligned}\quad (III.5.5)$$

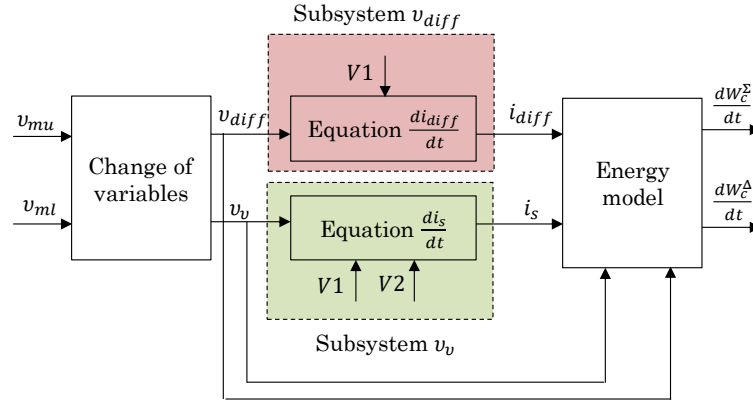


Fig 87. Energy model linked to the current model

Considering DC and AC components and relations (III.4.2), the expressions (III.5.5) are developed in (III.5.6) and (III.5.7).

$$\begin{aligned}\frac{dW_c^\Sigma}{dt} &= P1 - P2 \\ &+ \hat{I}_{diff,ac} \cdot \left( \left( \frac{P1}{V1} - \frac{P2}{2 \cdot V2} \right) \cdot 2 \cdot l \cdot \omega \cdot \sin \omega \cdot t + V1 \cdot \cos \omega \cdot t \right) \\ + \hat{I}_{s,ac} \cdot &\left( \frac{P2}{2 \cdot V2} \cdot (l + 2 \cdot Ls) \cdot \omega \cdot \sin(\omega \cdot t - \theta') + \left( \frac{V1}{2} - V2 \right) \cdot \cos(\omega \cdot t - \theta') \right) \\ + \hat{I}_{diff,ac}^2 \cdot &l \cdot \omega \cdot \sin(2 \cdot \omega \cdot t) + \frac{\hat{I}_{s,ac}^2}{4} \cdot (l + 2 \cdot Ls) \cdot \omega \cdot \sin(2 \cdot \omega \cdot t - 2 \cdot \theta')\end{aligned}\quad (III.5.6)$$

$$\begin{aligned}\frac{dW_c^\Delta}{dt} &= P1 + P2 - \frac{2V2}{V1} P1 - \hat{I}_{diff,ac} \cdot \hat{I}_{s,ac} \cdot Ls \cdot \omega \cdot \sin \theta' \\ &+ \hat{I}_{diff,ac} \cdot \left( \frac{P2}{V2} \cdot l \cdot \omega \cdot \sin \omega t + (V1 - 2 \cdot V2) \cdot \cos \omega t \right) \\ + \hat{I}_{s,ac} \cdot &\left( \left( \frac{P1}{V1} - \frac{P2}{V2} \right) \cdot (l + 2 \cdot Ls) \cdot \omega \cdot \sin(\omega t - \theta') + \frac{V1}{2} \cdot \cos(\omega t - \theta') \right) \\ &+ \hat{I}_{diff,ac} \cdot \hat{I}_{s,ac} \cdot (l + Ls) \cdot \omega \cdot \sin(2 \cdot \omega \cdot t - \theta')\end{aligned}\quad (III.5.7)$$

The derivative of two energies  $W_c^\Sigma$  and  $W_c^\Delta$  can both be decomposed in three frequency components. A DC component due to DC grids, an AC component at  $\omega$  and the other one at  $2 \cdot \omega$ . The energy schema-block of a leg is presented in Fig 88.

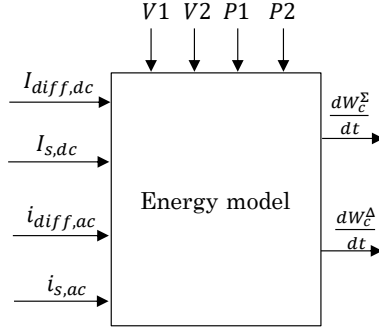


Fig 88. Energy model of M2DC leg

### III.5.3 Steady state analysis of energy stability

Averaging expressions (III.5.6) and (III.5.7), the variations of stored energy are presented in (III.5.8) and (III.5.9) and illustrated in Fig 89.

$$\left\langle \frac{dW_c^\Sigma}{dt} \right\rangle = P1 - P2 \quad (\text{III.5.8})$$

$$\left\langle \frac{dW_c^\Delta}{dt} \right\rangle = P1 + P2 - \frac{2V2}{V1} P1 - \hat{I}_{diff,ac} \cdot \hat{I}_{s,ac} \cdot Ls \cdot \omega \cdot \sin \theta' \quad (\text{III.5.9})$$

(III.5.8) explains that DC components  $I_{diff,dc}$  and  $I_{s,dc}$  control DC powers  $P1$  and  $P2$ . Assuming converter power transmitted from high voltage side  $P1$  to low voltage side  $P2$ , the derivative of stored energy  $W_c^\Sigma$  indicates the power balancing between input and output, and charging/discharging leg capacitors.

- If  $P1 < P2 < 0$ ,  $W_c^\Sigma$  increases. Capacitors of the leg charge globally.
- If  $0 > P1 > P2$ ,  $W_c^\Sigma$  reduces. Capacitors of the leg discharge globally.

In a period of operation, the variation of the stored energy  $W_c^\Sigma$  is independent of AC components. Therefore, DC components balance the input and output powers.

AC components  $\hat{I}_{diff,ac}$  and  $\hat{I}_{s,ac}$  control the variation of energy  $W_c^\Delta$ , since (III.5.9) depends on the DC voltage ratio, powers  $P1$ ,  $P2$  and AC currents  $\hat{I}_{diff,ac}$ ,  $\hat{I}_{s,ac}$ . If  $(P1, P2)$  are controlled by DC components, (III.5.9) depends only on AC currents  $\hat{I}_{diff,ac} \cdot \hat{I}_{s,ac}$ .

In the condition of balanced energy  $W_c^\Sigma$  ( $P1$  equals to  $P2$  without losses), the control of energy  $W_c^\Delta$  has two possibilities:

- For  $2 \cdot P1 \cdot \left(1 - \frac{2 \cdot V2}{V1}\right)$  superior to  $\hat{I}_{diff,ac} \cdot \hat{I}_{s,ac} \cdot Ls \cdot \omega \cdot \sin \theta'$ ,  $W_c^\Delta$  increases that the upper arm is charged and the lower arm is discharged.
- For  $2 \cdot P1 \cdot \left(1 - \frac{2 \cdot V2}{V1}\right)$  inferior to  $\hat{I}_{diff,ac} \cdot \hat{I}_{s,ac} \cdot Ls \cdot \omega \cdot \sin \theta'$ ,  $W_c^\Delta$  decreased that the upper arm is discharged and the lower arm is charged.

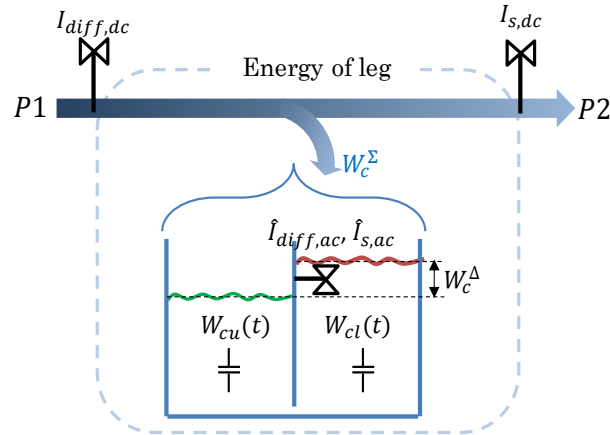


Fig 89. Stored energy of a leg in the steady state

Therefore, the aim of energy control is to balance the energy between the upper and lower arms and to regulate the total arm energy.

### III.6 Energy loop design

The energy loop is the outer loop of high-level control. It is realized with PI controllers. The response time is chosen ten times slower than the inner loop to isolate control loops from each other. Moreover, steady-state errors of the current loop are neglected in this part.

#### III.6.1 Equivalent Low pass filter

A low pass filter removing oscillations from capacitor voltages is used to evaluate equivalent capacitor voltages. This low pass filter is a simple “moving average”, reducing the instability of a large bandwidth conventional  $l-r$  low pass filter. The principle of a simple moving average is shown in equation (III.6.1) and Fig 90. Average value  $\bar{a}(t)$  of a signal  $a(t)$  is obtained by taking the average of the  $n$  number of signals to delay the signal  $a(t)$  by time  $\tau$  each of them [88].

$$\bar{a}(t) = \frac{a(t) + a(t + \tau) + a(t + 2 \cdot \tau) + \dots + a(t + n \cdot \tau)}{n} \quad (\text{III.6.1})$$

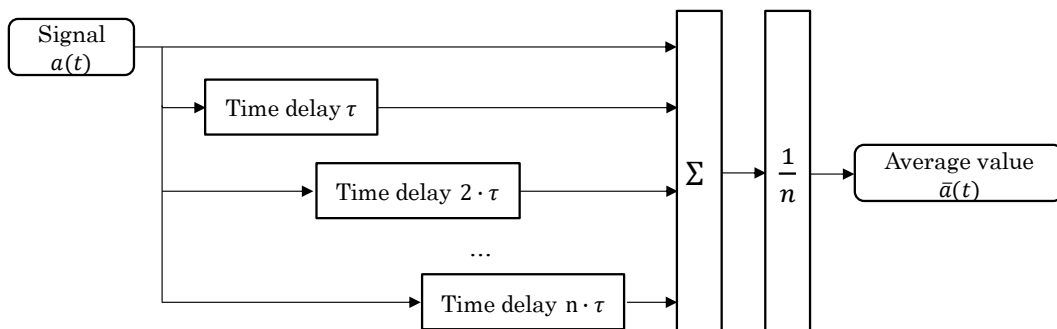


Fig 90. Principle of the simple “moving average”

For a periodic  $a(t)$  with a frequency  $f$ , it is better to select  $n$  and  $\tau$  in the way of (III.6.2) to improve the quality of the moving average value. Otherwise, there will always be unexpected oscillations in the average value  $\bar{a}(t)$ .

$$n \cdot \tau = \frac{1}{f} \quad (\text{III.6.2})$$

### III.6.2 Continuous time transfer function and closed energy loop

According to (III.5.5), the transfer function  $H^\Sigma(s)$  of the energy  $W_c^\Sigma$  and the transfer function  $H^\Delta(s)$  of energy  $W_c^\Delta$  are explained by formula (III.6.3).

$$\begin{aligned} H^\Sigma(s) &= \frac{W_{cu} + W_{cl}}{\frac{dW_c^\Sigma}{dt}} = \frac{1}{s} \\ H^\Delta(s) &= \frac{W_{cu} - W_{cl}}{\frac{dW_c^\Delta}{dt}} = \frac{1}{s} \end{aligned} \quad (\text{III.6.3})$$

Since energy systems are first order systems with constant control targets, the PI controller is adequate for the energy loop. The controller has the same form as Fig 77. The closed-loop transfer functions are described in (III.6.4).

$$\begin{aligned} FTBF^\Sigma(s) &= \frac{Kp \cdot s + Ki}{s^2 + Kp \cdot s + Ki} \\ FTBF^\Delta(s) &= \frac{Kp \cdot s + Ki}{s^2 + Kp \cdot s + Ki} \end{aligned} \quad (\text{III.6.4})$$

The closed energy loop is obtained in Fig 91 where the blue path indicates the control loop of energy sum  $W_c^\Sigma$  and the black path indicates the control loop of the energy difference  $W_c^\Delta$ .

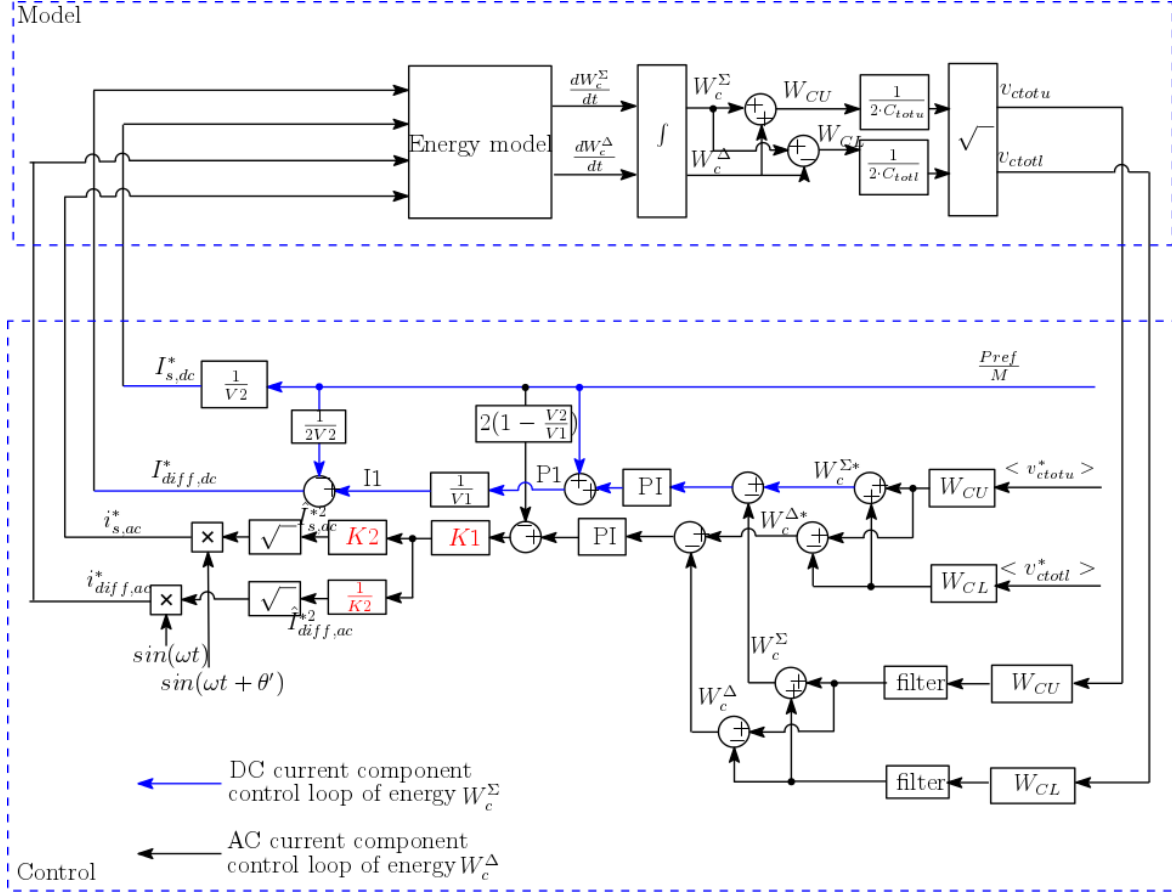


Fig 91. Closed energy loop of an M2DC leg

Considering the power reference  $P_{ref}$  in the Fig 91, a real converter has losses. Input power is certainly different from output due to the losses, which is neglected in the analysis. The expression (III.5.8) will not be zero, but with a small constant value (related to the rated power). Therefore, the power reference  $P_{ref}$  can only be imposed in either the input side  $P1$  or the output side  $P2$ . In our control, the output power  $P2$  is directly controlled, then input power  $P1$  is indirectly controlled by the  $W_c^\Sigma$  energy control loop.

However,  $W_c^\Delta$  control loop keeps neglect the losses in order to isolate two energy loops and to avoid in the fluence of  $W_c^\Sigma$  loop on  $W_c^\Delta$  loop. As can be seen in the Fig 91, DC and AC currents are completely independent. DC component currents are obtained by  $W_c^\Sigma$  loop. Then AC component currents are obtained by  $W_c^\Delta$  loop.

To obtain AC component currents, the expression (III.5.9) indicates numerous possibilities of a selection of two AC amplitudes. The simulation chooses the solution satisfying the choices of the previous chapter  $\hat{v}_{mu,ac} = \hat{v}_{ml,ac}$  and  $\theta = 90^\circ$ .

In the condition  $\hat{v}_{mu,ac} = \hat{v}_{ml,ac}$  and  $\theta = 90^\circ$ , AC voltages  $v_{diff,ac}$  and  $v_{v,ac}$  follow the expression (III.6.5) according to the phasor diagram presented in Fig 92.

$$\begin{aligned} \hat{v}_{diff,ac} &= \hat{v}_{v,ac} \\ \theta' &= -\frac{\pi}{2} \end{aligned} \quad (III.6.5)$$

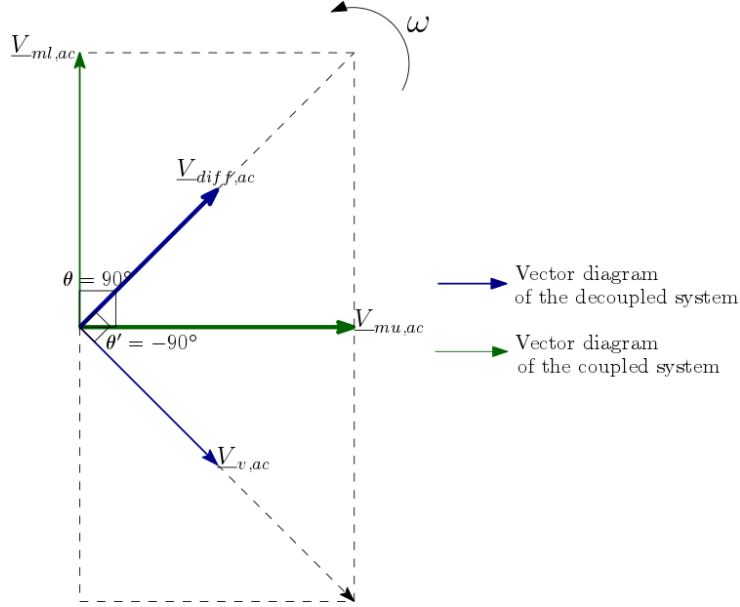


Fig 92. Phasor diagram under the condition  $\hat{V}_{mu,ac} = \hat{V}_{ml,ac}$  and  $\theta = 90^\circ$

The decoupled AC currents are described in (III.6.6) depending on (III.3.16).

$$\frac{\hat{I}_{s,ac}}{\hat{I}_{diff,ac}} = \frac{l}{\frac{l}{2} + Ls} \quad (III.6.6)$$

Therefore, the coefficients K1 and K2 introduced in Fig 91 have the values of (III.6.7).

$$K1 = \frac{1}{Ls \cdot \omega \cdot \sin(\theta')} = \frac{1}{Ls \cdot \omega} \quad (III.6.7)$$

$$K2 = \frac{\hat{I}_{s,ac}}{\hat{I}_{diff,ac}}$$

where,  $\theta' = -90^\circ$ .

Finally, angular frequency  $\omega$  is imposed independently to have the sine wave for AC component currents.

### III.6.3 Static and dynamic analysis of the energy loop

#### III.6.3.1 Static performance of the energy loop

- Converter parameters design

The test of the energy loop uses the parameters of the current loop (Table 6) and submodule capacitors values. Capacitances of submodules have values calculated by the formulas presented in the previous chapter to have +/-5% estimated ripples in  $v_{totu}$  and



$v_{totl}$ . The simulation uses the conventional number of submodules  $N_u = N_l = 200$  applied for two arms, as in an MMC.

Table 11 Parameters of submodule using CIGRE group test scenario

Number of submodules of upper arms	200
Number of submodules of lower arms	200
Equivalent capacitance of upper arms $C_{totu}$	46.8uF
Equivalent capacitance of lower arms $C_{totl}$	130uF
Capacitance of submodule of upper arms $C_u$	9.36mF
Capacitance of submodule of lower arms $C_l$	26mF

- Control parameters

Parameters of PI controllers (Table 12) are calculated using pole placement. The damping ratio of the energy loop is set to 1. Then, the response time is set to 0.3s to be ten times slower than the current loop.

Table 12 Energy controller parameters

	$W_c^\Sigma$ loop	$W_c^\Delta$ loop
$Kp$	16.6	15.6
$Ki$	277.7	245.4

- Steady state response

The energy loop is simulated with the average model in Matlab Simulink. The simulation uses the CIGRE group test scenario ( 600MW, 320kV/250kV, and 60us sample time). Capacitors have been previously charged at the initial condition to have  $v_{totu0} = 320kV$  and  $v_{totl0} = 320kV$ .

Energy steady-state results are shown in Fig 93. (a) and (b).

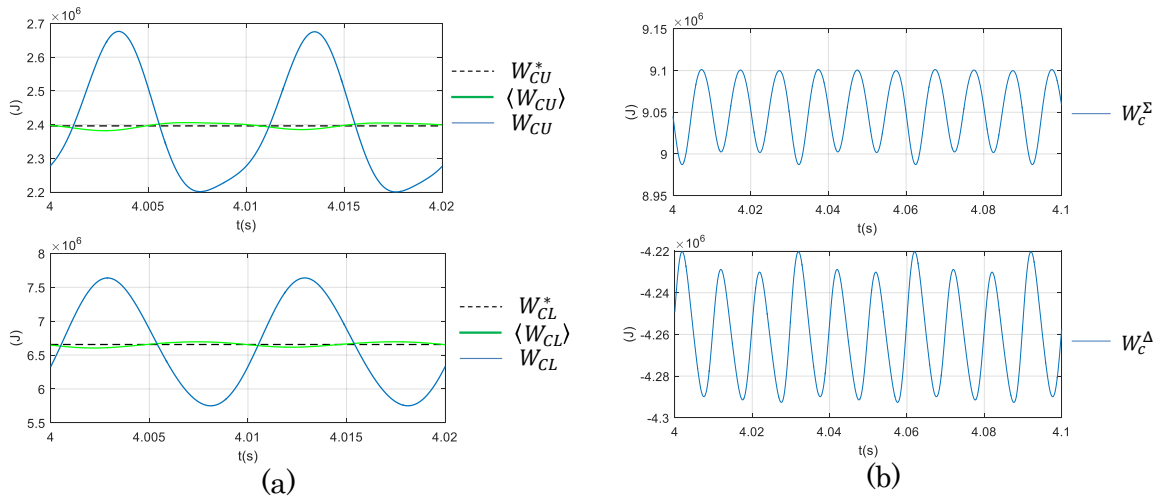


Fig 93. (a)  $W_{CU}$  and  $W_{CL}$  (b)  $W_c^\Sigma$  and  $W_c^\Delta$  of an M2DC leg

Simulated values track correctly their reference. Moreover, there are no steady-state errors, except for small oscillations in the simulation. The cause of the small oscillations is that with 100Hz operating frequency, it is impossible to set the time delay (III.6.8) to be integral multiple of sample time 60us in Matlab Simulink.

$$\tau = \frac{1}{f \cdot n} \quad \text{(III.6.8)}$$

As can be seen in Fig 93, upper and lower arms stock different energy values. It is synthesized in Fig 94. The stored energy of the upper arm is smaller than in the lower arm. The energy  $W_c^\Sigma$  and  $W_c^\Delta$  are kept balanced. With the designed capacitors, M2DC converter leg should stock 9MJ energy  $W_c^\Sigma$  and balance 4.2MJ energy  $W_c^\Delta$  between the upper and lower arm to transmit 200MW/leg.

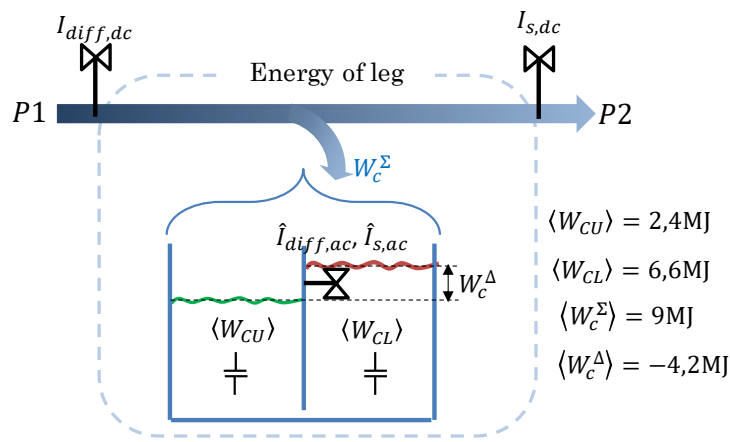


Fig 94. CIGRE test case of energy storage in one leg M2DC

These capacitors create +/-5% ripples in voltages  $v_{ctotu}$  and  $v_{ctotl}$ . The Fig 95 validates the design of the energy loop.

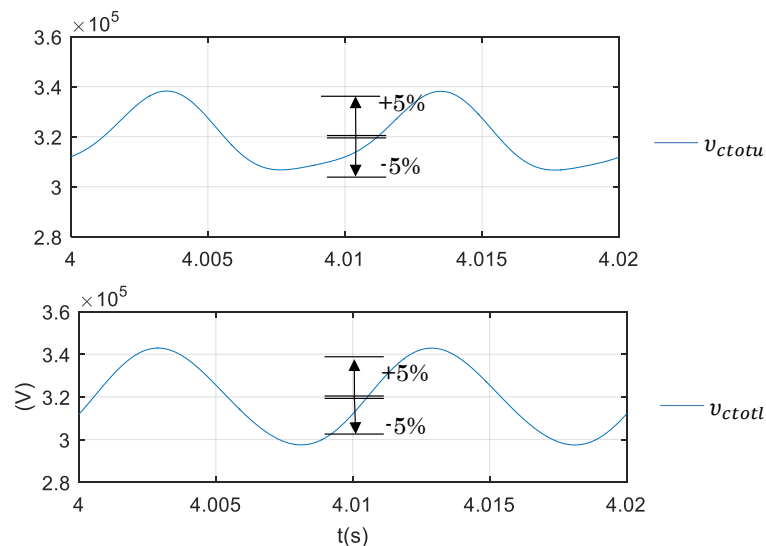


Fig 95. CIGRE test case  $v_{ctotu}$  and  $v_{ctotl}$  of M2DC leg

Slight differences from the theory show the effect of neglected terms in the capacitance design formula. Different shape of two capacitor voltages validate the different energy expressions of two arms explained in the previous chapter. In practice, capacitance value depends also on real components available in the market.

### III.6.3.2 Dynamic performance of energy loop

To analyze the dynamic performance of the energy loop, two step events are imposed on references of  $v_{ctotu}$  and  $v_{ctotl}$ .

At  $t = 7.5s$ , the reference of  $v_{ctotu}$  is increased of 10%.

At  $t = 9s$ , the reference of  $v_{ctotl}$  is increased of 10%.

The events acting on voltage  $v_{totu}$  and  $v_{totl}$  can be translated by a 1% increase of  $W_{CU}$  and  $W_{CL}$ . Then, actions on energy  $W_C^\Sigma$  and  $W_C^\Delta$  follow the description below:

At  $t = 7.5s$ , a 10% increase of  $v_{totu}$  increases  $W_C^\Sigma$  and decreases  $W_C^\Delta$ .

At  $t = 7.5s$ , a 10% increase of  $v_{totl}$  decreases  $W_C^\Delta$  and increases  $W_C^\Sigma$ .

Fig 97 and Fig 97 show, respectively responses of  $v_{totu}$  and  $v_{totl}$  and responses of  $W_{CU}$  and  $W_{CL}$ . Since control targets are constant ( $\langle W_{CU} \rangle$  and  $\langle W_{CL} \rangle$ ), there is no tracking errors between references ( $W_{CU}^*$  and  $W_{CL}^*$ ) and simulations ( $W_{CU}$  and  $W_{CL}$ ). Ripples in ( $W_{CU}$  and  $W_{CL}$ ) or ( $v_{totu}$  and  $v_{totl}$ ) indicate capacitors charging and discharging. Moreover, references of  $v_{totu}$  and  $v_{totl}$  are in the coupled frame. A change in one reference influences the other one.

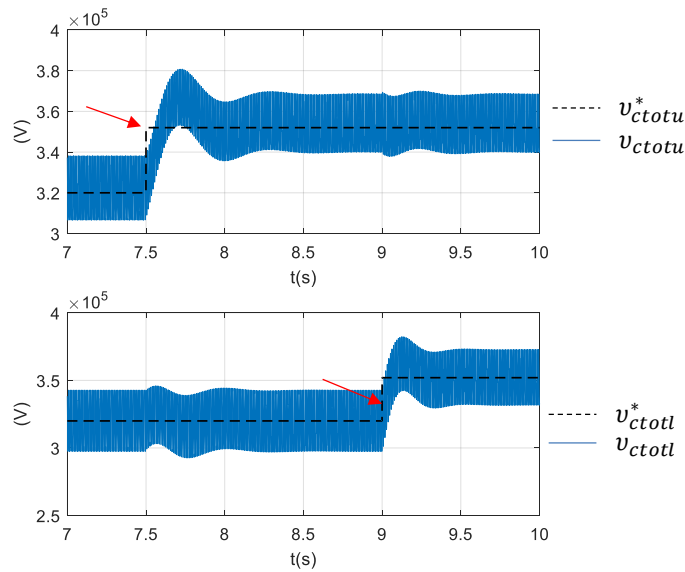


Fig 96. Dynamic response of  $v_{totu}$  and  $v_{totl}$  ( $Tr = 0.3$ ,  $\xi = 1$ )

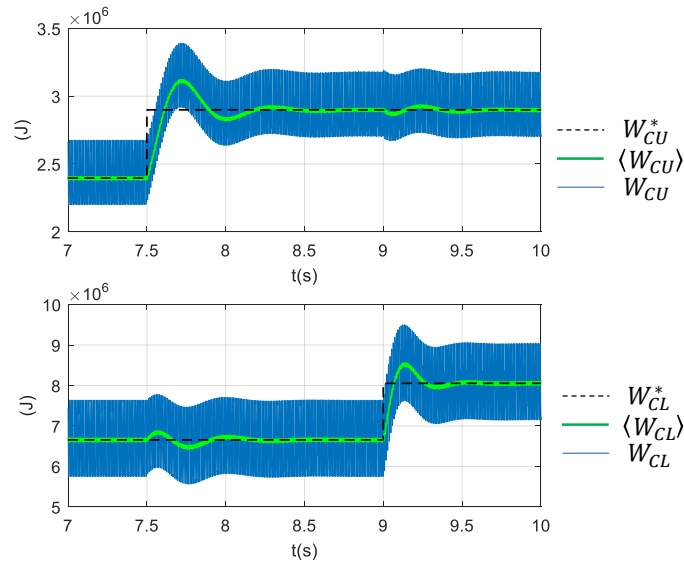


Fig 97. Dynamic response of  $W_{CU}$  and  $W_{CL}$  ( $Tr = 0.3, \xi = 1$ )

Fig 98 shows the input and output power evolutions with these voltage reference variations.

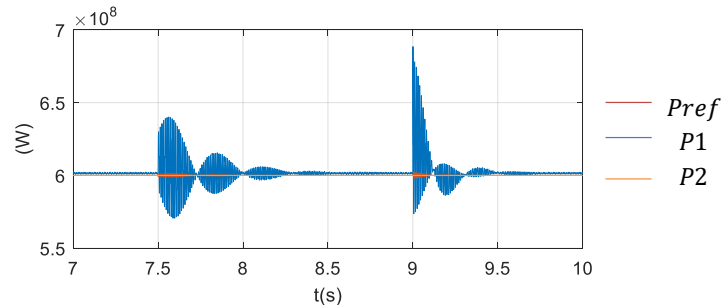


Fig 98. Input and output power ( $P1$  and  $P2$ )

Each event causes a disturbance in the stored internal energy. The disturbance finally appears on the input and output power. As the control reference is set at output  $P2$ , input power  $P1$  is more sensible to every events. Thanks to the energy and current loops, the steady state is obtained in a short time.

### III.7 Validation of AC components using average model

The value of submodule capacitances has been validated by simulations. This section concerns to validate the AC voltage and AC current components, using the CIGRE test case.

The validation of AC components consists of two parts. One part aims to validate the time axis by frames of reference. The other part discusses the limitations of AC components by their amplitudes.

### III.7.1 Validation of frames of reference

Due to the change of variables, coupled variables and decoupled variables create individually each a frame (Fig 75).

The validation is based on the choices  $\hat{V}_{mu} = \hat{V}_{ml}$  and  $\theta = 90^\circ$ . To achieve the choices, the decoupled variables have the relation  $\hat{V}_{diff,ac} = \hat{V}_{v,ac}$  and  $\theta' = -90^\circ$ , which are imposed in the energy loop (Fig 91).

Regarding the simulation result (Fig 99), the relation  $\hat{V}_{diff,ac} = \hat{V}_{v,ac}$  and  $\theta' = -90^\circ$  are set well. Then, the voltage-current relation (III.3.16) and the decoupled model (Fig 74) are validated. The slight ripple in the current  $i_s$  is due to the great value of secondary inductance  $L_s$ .

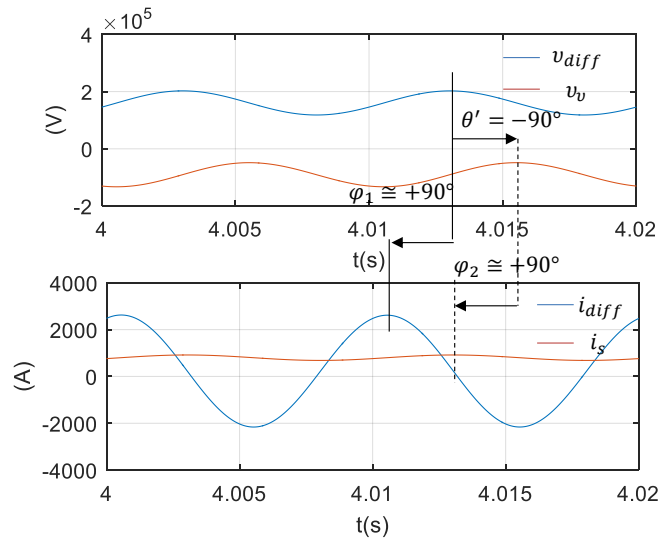


Fig 99. Decoupled variables

Fig 100 shows the desired coupled variables  $\hat{V}_{mu,ac} = \hat{V}_{ml,ac}$  and  $\theta = +90^\circ$ . It confirms the current-current angle  $\lambda$  is around zero due to the great value of  $L_s$ . Then, the phase  $\varphi$  between  $v_{mu}$  and  $i_u$  is around  $135^\circ$ .

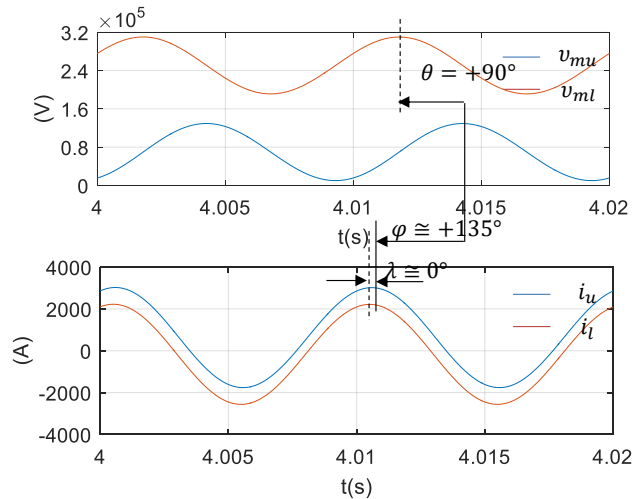


Fig 100. Coupled variables

The vector diagram Fig 101 summarizes temporal waveforms shown in Fig 99 and Fig 100.

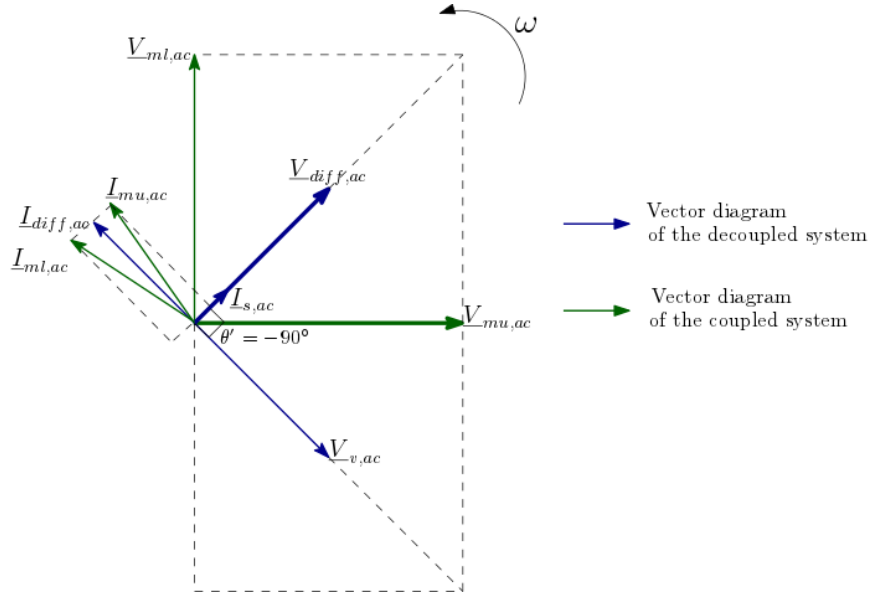


Fig 101. Vector diagram of AC component currents and voltages in M2DC leg

### III.7.2 Validation of limitations of AC components

During the frequency selection Fig 81, the security margin reduces the AC voltage component and increases AC currents. Comparisons between simulations and theory in Fig 102 and Fig 103 validated the previous analysis.

In Fig 102.(a), the measurement of peak to peak of upper arm indicates 119kV, with a 59kV AC amplitude component. Comparing the theoretical upper limitation Fig 102.(b), the simulation value confirms to be inferior to the predicted limitation.

Then, the AC voltage of the lower arm has the same value than the upper arm. The theoretical analysis in the previous chapter is validated.

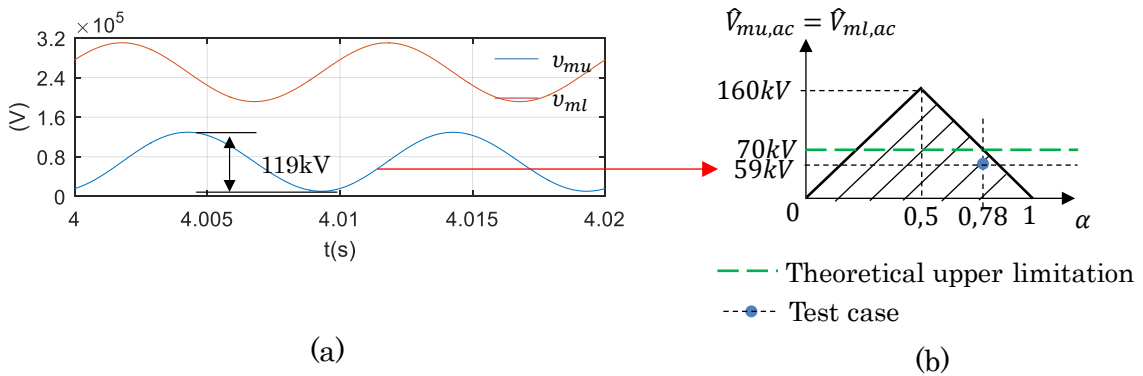


Fig 102. (a) Voltage simulations and (b) theoretical limitation of AC voltage

Since AC voltages are reduced, the increase of AC currents in the simulation is predictable in comparison with minimal values obtained in the best condition.

The DC current  $I1$  is equal to 1875A for the three legs (with 600MW rated power), then 625A per leg. With the ratio of 0.78, the theoretical lower limitation of AC current is  $2 \cdot \sqrt{2}$  times DC current of a leg. The simulation shows finally that AC currents (Fig 103. (a)) are 3.58 times the DC current of a leg, which is 26% superior to the minimal predicted value (Fig 103. (b)).

Fig 103. (a) indicates also that the difference between both arm currents values comes from the DC current  $I2$ , equal to 2400A for three legs, then 800A per leg.

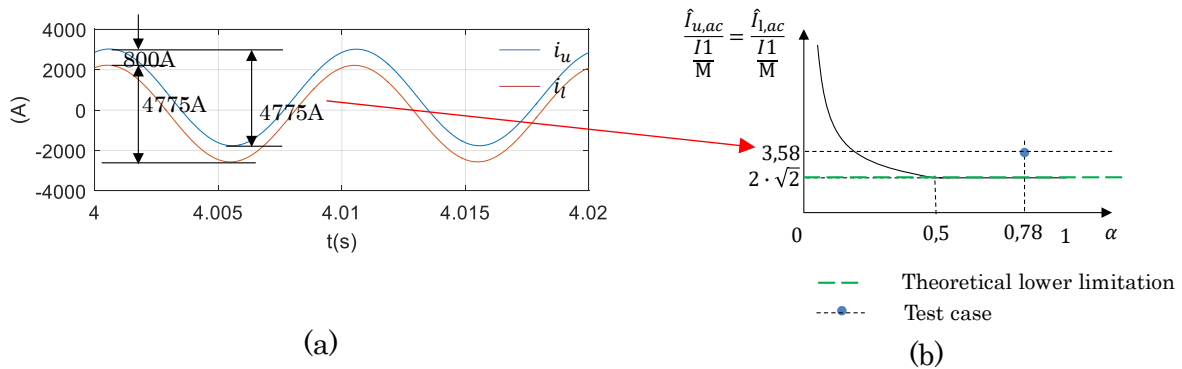


Fig 103. (a) Current simulations and (b) AC/DC currents theoretical limitation

### III.7.3 M2DC global simulation results of CIGRE test case

#### III.7.3.1 Steady state results

Depending on CIGRE specification, DC currents are obtained in Fig 104 with expected theoretical value 1875A/2400A. Therefore, it can be concluded that M2DC converter is able to realize a voltage conversion with the desired ratio and power.

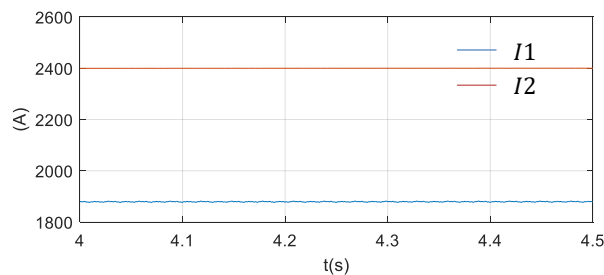


Fig 104. DC currents

Three legs arm voltages and arm currents are shown in Fig 105. (a) and (b). The quality of currents  $I1$  and  $I2$  are ensured by symmetric AC component currents of the three legs (Fig 105. (b)) and by the current loop controller.

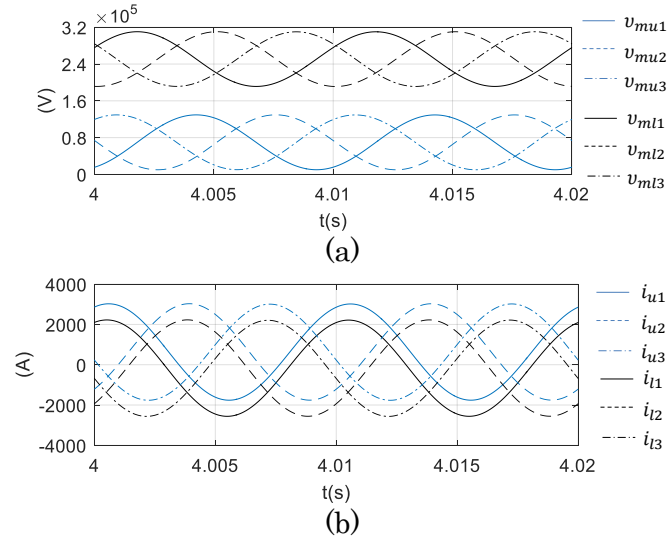


Fig 105. CIGRE test case: (a) Arm voltages (b) arm currents

The well controlled currents are convenient for energy control. The equivalent capacitor voltages (Fig 106) of each leg are balanced.

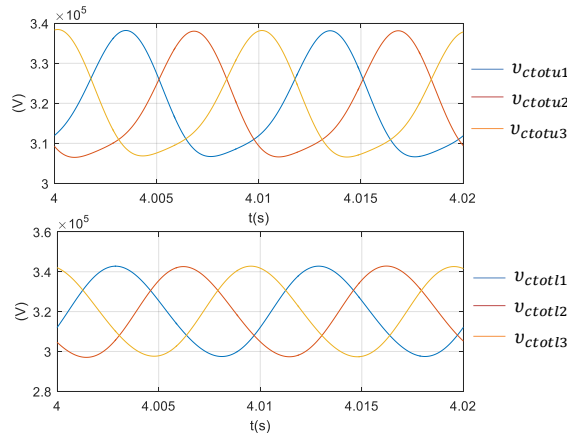


Fig 106. CIGRE test case: Equivalent capacitor arm voltages

Even if the converter has an asymmetric structure, DC currents are pure enough thanks to the current loop to ensure the phase shift angle between each leg.

### III.7.3.2 Dynamic results

The dynamic performance of the converter is shown by changing power reference  $P_{ref}$  of  $P2$  from 600MW to -600MW at  $t=5s$  and then to 300MW at  $t=9s$  (Fig 107).



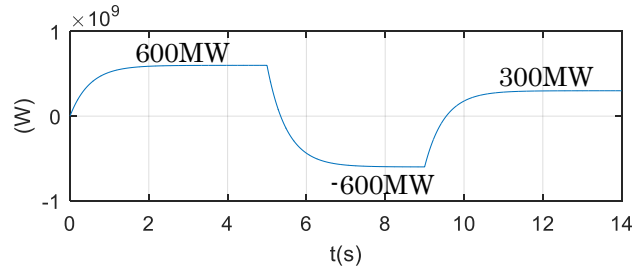


Fig 107. Power reference for P2

The negative currents values validate the power reversibility of the converter (Fig 108. (a)). However, disturbances are appearing in DC currents when power crosses zero Fig 108. (b), (c) and (d).

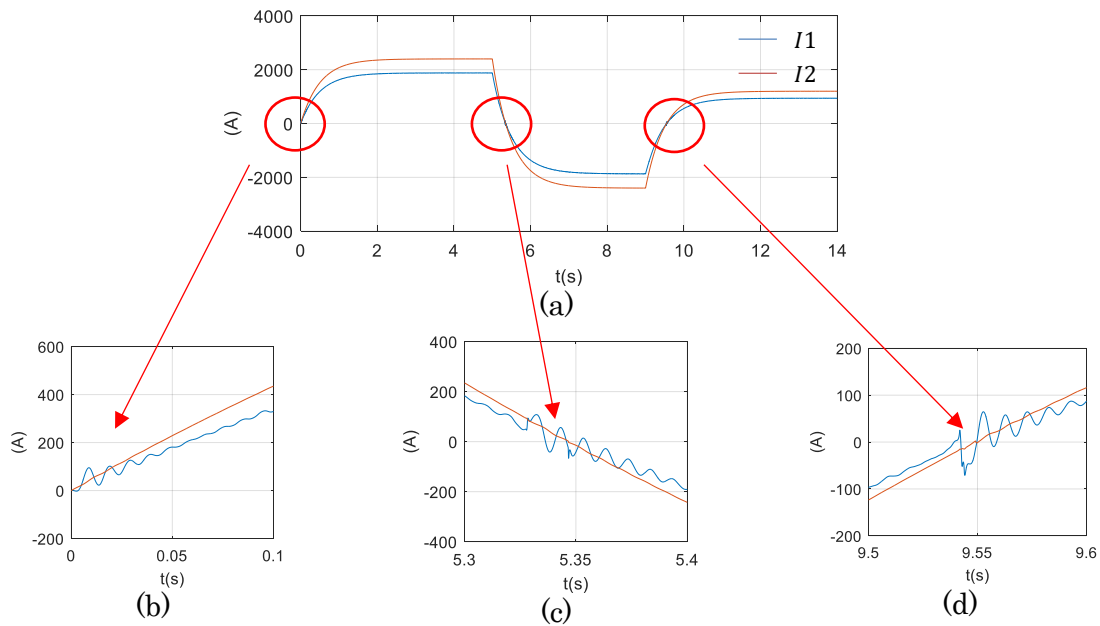


Fig 108. (a) Dynamic of input and output currents (b) zoomed currents at  $t=0s$ , (c) zoomed currents at  $t=5.3s$ , (d) zoomed currents at  $t=9.5s$

When  $P2 = 0$ , AC power is supposed to be zero and each arm has no energy control capability. Therefore, disturbances may appear around zero in Fig 108. (b), (c) and (d). Due to the converter losses (simulated by the internal resistor of inductors),  $P1$  has always a certain value that AC components always exist in the converter. AC power is not as the hypothesis to be zero. The converter is not able to follow its references.

This issue should be analyzed by taking into account losses in the theory analysis to get an improvement of operation and to focus the control stability for very low DC power.

At the same time, energy flow in one leg is shown in Fig 109. The internal energy  $W_{CU}$  and  $W_{CL}$  take around 0.5s to get the steady state.

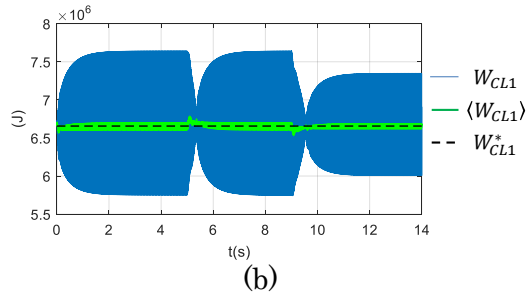
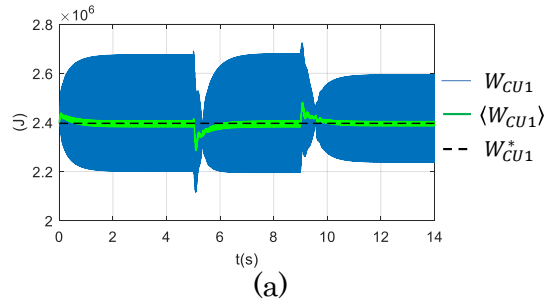


Fig 109. (a) Upper arm energy  $W_{CU}$  (b) lower arm energy  $W_{CL}$

Besides, the amplitude of AC component in voltage (Fig 110) and current (Fig 111) are not impacted by the power direction (at  $t=5s$ ), but by power absolute value (at  $t=9s$ ). Keeping the same frequency and angle  $\theta$ , AC voltage and current amplitudes only change in terms of power reference, which validate the choices of  $\hat{V}_{mu,ac} = \hat{V}_{ml,ac}$  and  $\theta = 90^\circ$ .

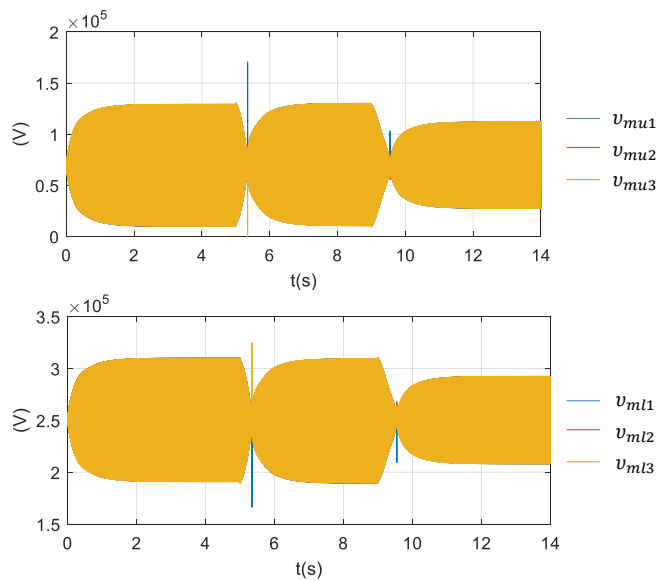


Fig 110. Arm voltages with output power reference variations

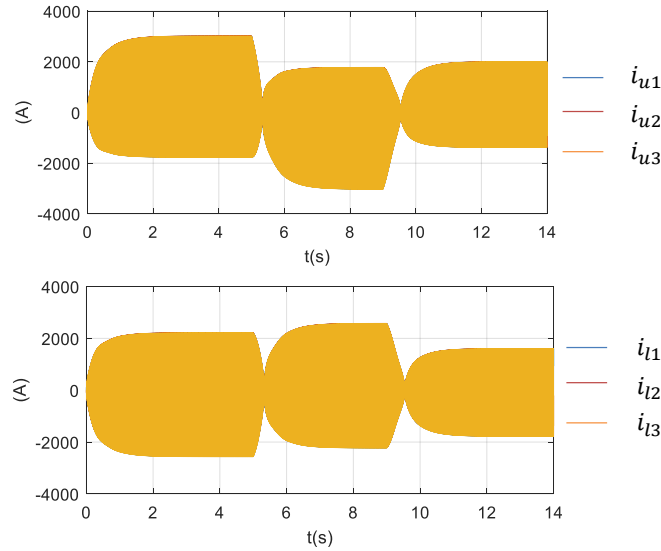


Fig 111. Arm currents with output power reference variations

To conclude, the CIGRE case test gives AC voltages and currents respectively around 59kV and 2387A in steady state. A 600MW power needs finally 50MW from AC components per leg ( $0.5 \cdot \hat{V}_{mu,ac} \cdot \hat{I}_{u,ac} \cdot \cos 135^\circ$ ).

Then, 150MW (three legs) active power from AC components to balance the internal capacitor energy is necessary. This result also satisfy the theory: 44MW per leg ( $(1 - \alpha) \cdot P1/M$ ), then 132MW (three legs) active power required by the converter at  $\alpha = 0.78$ . The difference can be justified by the neglected losses, measure precision and rounding calculations.

### III.8 Conclusion

This chapter has presented the control design of the M2DC converter, which is based as for the MMC, on the internal stored energy control. It consists of current and energy control loops. The current loop has been designed using PI controllers which has the advantage of simplicity, but the disadvantage of unavoidable steady-state errors. To reduce errors, it is required to reduce the response time during the controller design without disturbing the stability of systems.

The energy loop has average values of equivalent capacitor voltages as control targets. Therefore, PI controllers are suitable. During the control design, the choices proposed in the second chapter have been adopted and tested:  $\hat{V}_{mu,ac} = \hat{V}_{ml,ac}$  and  $\theta = +90^\circ$ .

Simulation results have been made considering the CIGRE test case. They confirm the static analysis and the converter design.

It has been noted that very low power issue needs more investigations. Futur works will have to be developed on this specific operating setpoint to control the stability and precise the control strategies for very low power references.

Next chapter concerns the validation of the analysis by real-time simulation and Hardware-In-the-Loop (HIL) to prepare the futur experimental M2DC experimentations using the L2EP MMC prototype.

### III.9 References

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# IV Implementation: Laboratory-based Real-Time simulation and Control Hardware-In-the-Loop (HIL) simulation

## IV.1 Introduction

During the European project “TWENTIES” (transmission system operation with a large penetration of wind and other renewable electricity sources in electricity networks using innovative tools and integrated energy solutions) [93], the L2EP laboratory (Laboratoire d’Electrotechnique et d’Electronique de Puissance de Lille) has developed a small scaled MTDC mock-up to test the voltage control algorithm of a DC grid. After this project, the AC/DC interconnections were upgraded by L2EP lab in close cooperation with Cinergia for the design and the realization of a small scaled MMC mock-up (Fig 112) to test the proposed controls and also to be more representative of a real MTDC grid.

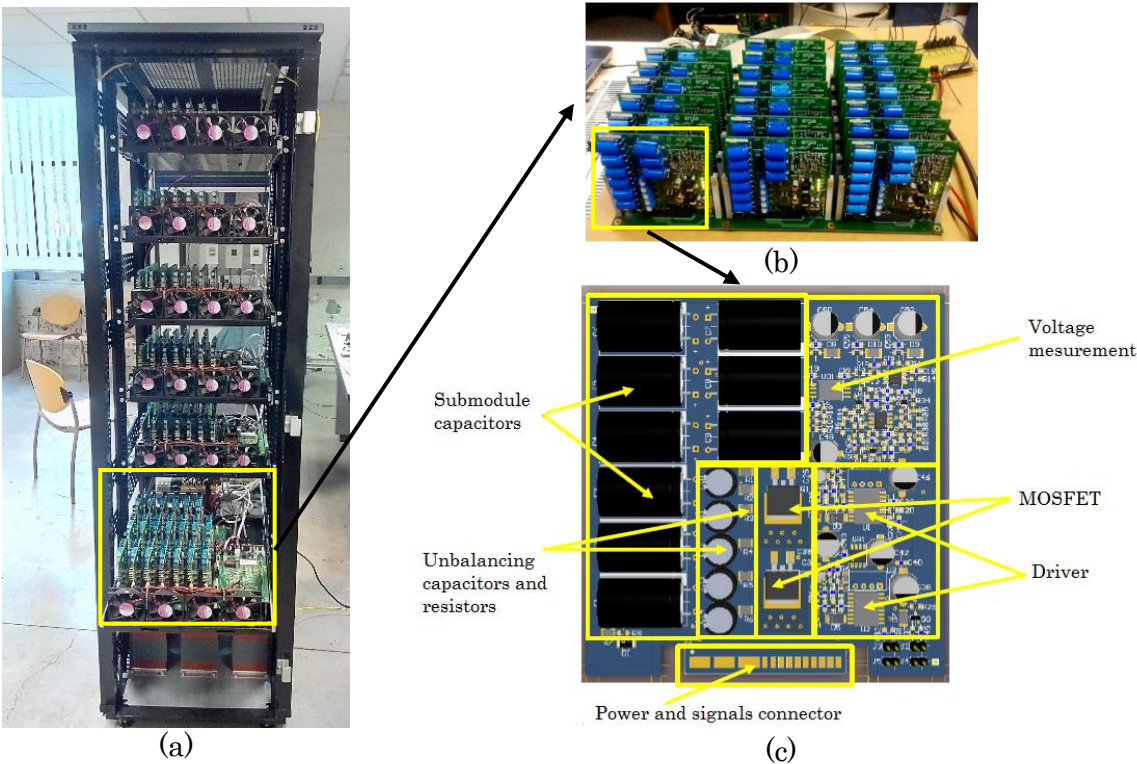


Fig 112. Laboratory MMC mock-up [92], [95] (a) front view (b) an arm (c) a submodule

Since MMC (Fig 113. (a)) and M2DC (Fig 113. (b)) can use the same submodule topology (Fig 112. (b) and (c)), an M2DC mock-up can be obtained by modifying the MMC converter to reduce development time and cost. Our objective is now to convert the existing MMC mock-up to the M2DC, with the design method developed in the second chapter and to test the control developed in the third chapter. In order to reduce the risks and the duration of future M2DC experiments, this chapter details the preparation of this experiment by testing simulations based on Hardware-In-the-Loop. As a fact, MMC mock-up is frequently occupied by other research projects of the laboratory Power System Team.

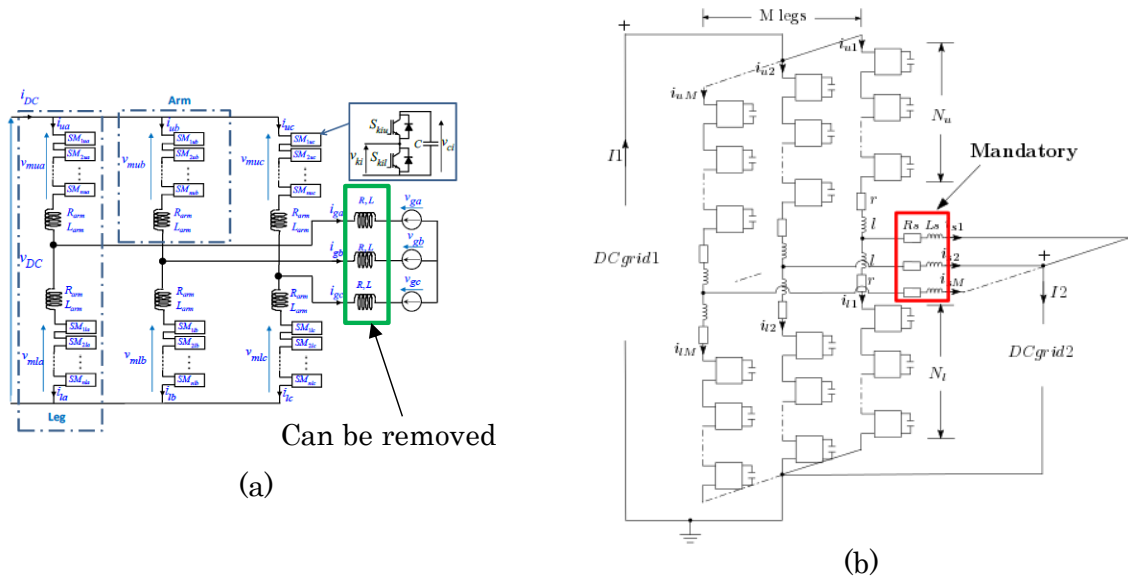


Fig 113. (a) MMC topology [95] (b) M2DC topology

The existing MMC mock-up has the components described in Table 13 [94]. Three legs, or six arms, constitute the global converter. Each arm (Fig 112. (b)) has twenty submodules, where each submodule (Fig 112. (c)) contains capacitors, voltage measurement, semiconductor MOSFET. Amongst these components, MOSFET's rated current  $I_n$ , capacitance value and capacitor rated voltage are setting constraints to the M2DC design.

Table 13 Components and low-level control used in MMC mock-up

Number of legs		3
Submodule	Number	20 per arm
	Capacitor	8mF-63V
	Semiconductor type	MOSFET ( $I_n = 15A$ )
Arm inductor		10mH (50Hz)
Low-level control		NLC (Nearest level control)

Moreover, the mock-up has also 10mH arm inductors with 50mΩ internal resistance at 50Hz. Low-level control of the MMC legs has been designed with the nearest level control method.

## IV.2 Description of test scenarios

### IV.2.1 Selection of secondary inductor and DC voltages

As shown in Fig 113, the main difference between M2DC and MMC is the inductor  $L_s$ . It is mandatory for M2DC to have great value for secondary inductors to minimize AC currents. The simulations use a value of 100mH to be ten times of arm inductor (10mH), which is fixed by the mock-up design. This value ensures the condition  $L_s \gg l$ . Inductor losses are simulated by 100mΩ internal resistance.

DC voltages analysis is necessary to operate the converter in suitable DC grids and converter parameters have to be designed before its utilization. With 20 submodules per arm and capacitor working voltage (20V), total arm voltage  $v_{ctotu}$  and  $v_{ctotl}$  can attain a maximal value of 400V. Therefore, high voltage  $V1$  should be inferior or equal to 400V. Also, depending on the second chapter, the converter has less current stress for high duty ratio ( $0.5 \leq \alpha < 1$ ) where the converter design is then more convenient.

Therefore, considering these two conditions, two voltages  $V1$  and two ratios are tested.

- **$V1$  voltages are 400V and 320V.** The 400V case aims to use maximum submodules of the converter. In the case of 320V, the converter is oversized.
- **The two ratios are 0.5 and 0.78.** Ratio 0.5 aims to test the converter operation principle in a symmetrical structure with the same number of submodules in upper and lower arms. In cases of 0.78, the asymmetrical structure is tested.

According to the combinations of selected voltages and ratios, four test cases are shown in Table 14.

Table 14 Test Cases

	Case 1	Case 2	Case 3	Case 4
$V1$	400V	400V	320V	320V
$V2$	200V	312V	160V	250V
Ratio	0.5	0.78	0.5	0.78
Secondary inductor	100mH(100mΩ)	100mH(100mΩ)	100mH(100mΩ)	100mH(100mΩ)

Case 1 can be useful for the project “TWENTIES” since  $V1$  is equal to 400V. The converter has the same voltages in the upper and lower arm, according to the design of the typical MMC structure using a maximum number of submodules.

Case 2 increases the lower arm voltage in comparison to case 1. Like case 1, the arm voltage of case 2 is sized using DC voltage 400V. Then all submodules of the converter are to be used. Moreover, this case is also expected to be advantageous in terms of current. Since MMC mock-up has the same number of submodules, the upper arms of the converter



in case 2 are less constraint than the lower arms, which use more submodules than the upper arms, according to the respected DC values.

Case 3 is like case 1 symmetrical case, with a reduced DC voltage  $V1$ . The reduction provides an oversize of the converter. Objective of this case is to test the converter behavior changing DC voltages but without changing submodules.

Case 4 is a reduced scale of the CIGRE test case (320kV/250kV). It is asymmetrical as case 2, but with a reduced DC voltage  $V1$ . As  $\alpha = 0.78$ , current stress is expected to be less than in case 3 for the same power. Either the converter structure or the components sizing, MMC mock-up is not specially designed for this type of DC values.

#### IV.2.2 AC voltage limitation

With determined DC voltages, AC component voltage will be limited by the rated value of the mock-up components. Based on the half-bridge submodule topology, amplitudes of AC voltages are (II.7.6) defined as  $\min((V1 - V2), V2)$ , considering the choice  $\hat{V}_{mu,ac} = \hat{V}_{ml,ac}$  and  $\theta = 90^\circ$ .

$$\begin{aligned} \hat{V}_{mu,ac} &= \hat{V}_{ml,ac} \\ \underline{V}_{ml,ac} &= \underline{V}_{mu,ac} \cdot e^{j\frac{\pi}{2}} \end{aligned} \tag{IV.2.1}$$

The arms create theoretically maximum AC amplitudes as Fig 114.

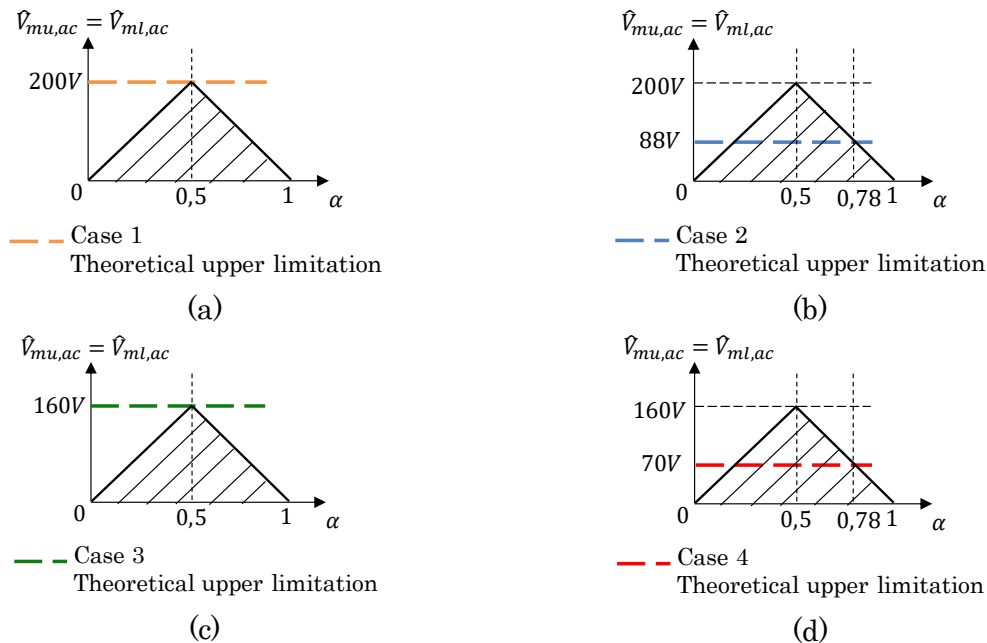


Fig 114. Theoretical maximum AC voltages for different cases

### IV.2.3 DC current leg limitation

Without frequency limitation, DC currents are limited by arm current limitation (Fig 115), then rated current of semiconductors.

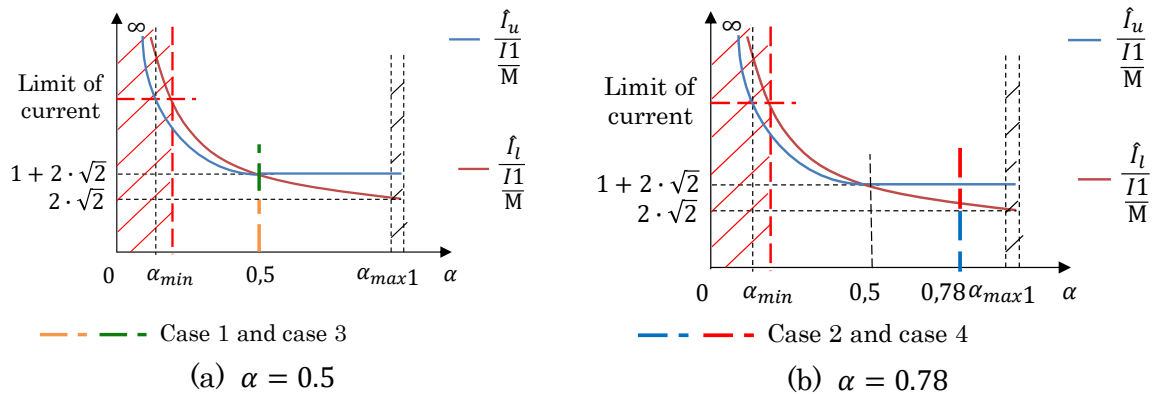


Fig 115. Theoretical arm currents limitations

Therefore, DC current of each arm  $I1/M$  have the expression of (IV.2.2).

$$\frac{I1}{M} < \frac{\hat{I}_u}{1 + 2 \cdot \sqrt{2}} = \frac{\hat{I}_l}{1 + 2 \cdot \sqrt{2}} \quad (IV.2.2)$$

To simplify calculations, it is considered the same current of upper and lower arm regardless of ratio. This simplification preserves also a security margin for asymmetrical cases. Then, with 15A rated current of MOSFET, DC current  $I1/M$  cannot numerically exceed 3.9A per leg. Therefore, in our different cases, 3A is chosen as the maximum DC input leg current ( $I1/M$ ). Then the three legs converter can go through 9A of DC input current  $I1$ .

This DC current limitation induces a maximal DC power of 3600W (400V/9A) for case 1 and 2 and 2800W (320V/9A) for case 3 and 4.

### IV.2.4 AC frequency selection

In the case of maximum power and AC voltage, selections of frequency are shown in Fig 116 where  $\omega_{min}$  is equal to 314 rad/s ( $f = 50Hz$ ), which is the arm inductor design frequency.

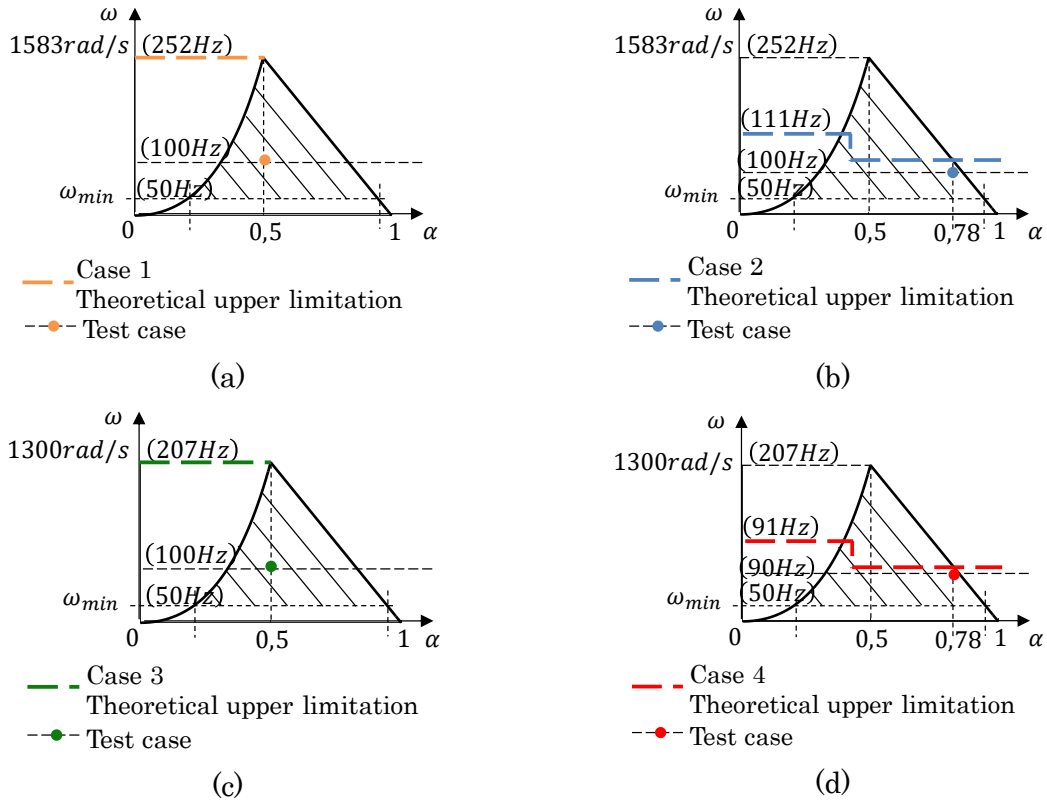


Fig 116. Frequency selections

Different cases have their maximum frequency around 200Hz, but the mock-up has its limited switching frequency around 200Hz. Therefore, the cases will be tested with a reduced frequency 100Hz or less. The reduced frequency will also decrease switching losses of semiconductors, which is convenient for the converter operation.

However, for case 2 and 4, the asymmetrical structure has a risk of under sizing submodule capacitance in the lower arm, since the mock-up has unchangeable capacitors, involving capacitor voltage ripples. To reduce the risk, their frequencies are selected as high as possible. Moreover, the frequency has to be reduced for case 4 according to frequency limitations.

#### IV.2.5 Selection of transmission power

Transmission power is limited by AC voltage and current. Since AC frequency is not at the maximum frequency, AC voltage and AC current change depending on the frequency. To ensure their limits, power design is necessary.

Depending on the equation (IV.2.3), leg power  $P1/M$  is limited by AC voltage.

$$\frac{P1}{M} < \frac{1}{1-\alpha} \cdot \frac{1}{2} \cdot \frac{Ls \cdot (\hat{V}_{mu,ac})^2}{\omega \cdot (2 \cdot l \cdot Ls + l^2)} \quad (IV.2.3)$$

Substituting  $\hat{V}_{mu,ac}$  by equation (II.8.6), (IV.2.5) and (IV.2.6),

$$\hat{I}_u = |I_{u,dc}| + \hat{I}_{u,ac} \quad (IV.2.4)$$

$$|\hat{I}_{u,ac}| \cong \frac{1}{\sqrt{2} \cdot l} \cdot \frac{\hat{V}_{mu,ac}}{\omega} \quad (IV.2.5)$$

$$|I_{u,dc}| = \frac{P1}{M \cdot V1} \quad (IV.2.6)$$

The leg power limitation deduced from arm current one is described in (IV.2.7).

$$\begin{aligned} & \left( \frac{1}{1-\alpha} \cdot \frac{Ls \cdot l \cdot \omega}{(2Ls+l) \cdot V1^2} \right) \cdot \left( \frac{P1}{M} \right)^2 \\ & - \left( \frac{2}{1-\alpha} \cdot \frac{Ls \cdot l \cdot \omega}{(2Ls+l) \cdot V1} \cdot \hat{I}_u + 1 \right) \cdot \frac{P1}{M} \\ & + \frac{1}{1-\alpha} \cdot \frac{Ls \cdot l \cdot \omega}{(2Ls+l)} \cdot (\hat{I}_u)^2 = 0 \end{aligned} \quad (IV.2.7)$$

Resolving the equation (IV.2.7), the leg power limitation is described in (IV.2.8).

$$\frac{P1}{M} < \frac{-b \pm \sqrt{b^2 - 4 \cdot a \cdot c}}{2 \cdot a} \quad (IV.2.8)$$

where

$$\begin{aligned} a &= \frac{1}{1-\alpha} \cdot \frac{Ls \cdot l \cdot \omega}{(2Ls+l) \cdot V1^2} \\ b &= - \left( \frac{2}{1-\alpha} \cdot \frac{Ls \cdot l \cdot \omega}{(2Ls+l) \cdot V1} \cdot \hat{I}_u + 1 \right) \\ c &= \frac{1}{1-\alpha} \cdot \frac{Ls \cdot l \cdot \omega}{(2Ls+l)} \cdot (\hat{I}_u)^2 \end{aligned} \quad (IV.2.9)$$

Limitations of power for our cases are finally described in Table 15.

Table 15 Leg power limitation

	Power limited by AC voltage	Power limited by arm current
Case 1	$\frac{P1}{M} < 3031W$	$\frac{P1}{M} < 952W$
Case 2	$\frac{P1}{M} < 1333W$	$\frac{P1}{M} < 1626W$
Case 3	$\frac{P1}{M} < 1940W$	$\frac{P1}{M} < 892W$
Case 4	$\frac{P1}{M} < 937W$	$\frac{P1}{M} < 1471W$

Notably, the power limitations of Table 15 is obtained with a fixed frequency and variable power, which is different from section IV.2.3 “*DC current limitation*”, power obtained by fixed power without frequency limitation.

As can be seen, at  $\alpha = 0.5$ , (case 1 and case 3), the leg power is limited by the arm current, since reduced frequency increases AC current. However, at  $\alpha = 0.78$ , (case 2 and case 4), the leg power is limited by AC voltage limitation, as the selected frequencies are near their limits. Moreover, the converter transmits more power with DC voltage 400V (case 1 and case 2) than 320V (case 3 and case 4). To facilitate comparison and preserve voltage and current margin, the specifications taken in of four cases are described in the Table 16.

Table 16 Specifications of test cases

	Case 1	Case 2	Case 3	Case 4
$V1$	400V	400V	320V	320V
$V2$	200V	312V	160V	250V
Ratio	0.5	0.78	0.5	0.78
Frequency	100Hz	100Hz	100Hz	90Hz
Power	2400W (800W/leg)	2400W (800W/leg)	1500W (500W/leg)	1500W (500W/leg)

With these specifications, capacitor voltage ripples are predicted with peak-to-peak percentage values in Table 17.

Table 17 Capacitor voltage ripple (in%)

	Case 1	Case 2	Case 3	Case 4
Upper arm	10%	2%	8%	3%
Lower arm	10%	8%	8%	10%

### IV.3 Control development methodology: definitions and simulation development

To minimize damage risks and reduce development time, the work uses firstly a real-time simulation and HIL (Hardware-in-the-loop) simulation to validate converter design and control. Experimental tests will be realized using the real MMC mock-up after these validations.

#### IV.3.1 Real-time simulation definition

Real-time simulation, according to [96], is a reproduction of input and output waveforms, with the desired accuracy. It is the digital twins of the real system. It is representative of the behavior of modeled real power systems. The solution of model equations in a real-time simulator for one-time step is the same time as in real clock [97]. The time required by the simulation to complete the calculation is called execution time

$T_e$ . Its length determines a non-real-time simulation (Fig 117. (a)) and a real-time simulation (Fig 117. (b)).

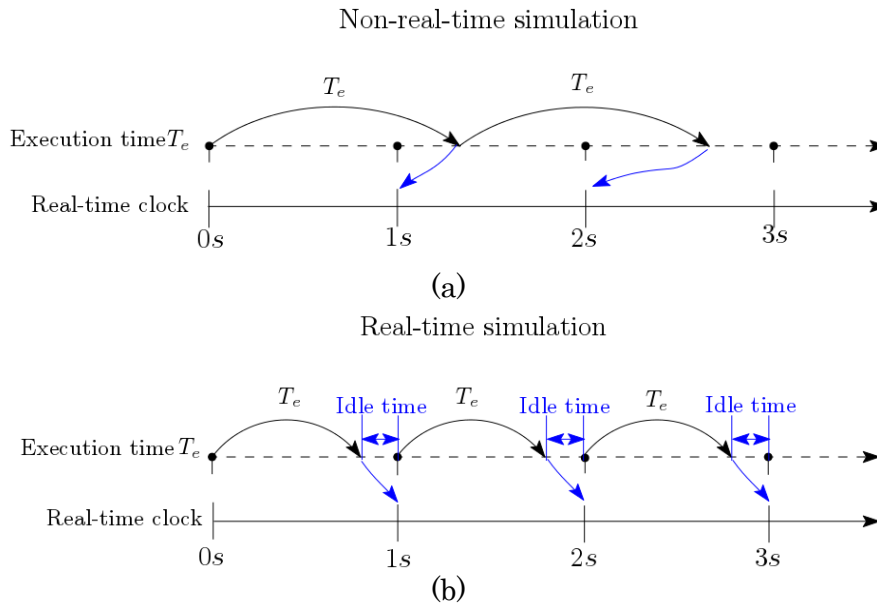


Fig 117. Illustration of real-time simulation and non-real-time simulation [96]

If a simulation execution requires more time than the real clock, the simulation is considered as non-real-time simulation or offline simulation. For example, simulation results in the third chapter obtained in Matlab are non-real-time simulations. To simulate one second of real-time, Matlab uses more than one second to execute the simulation.

For a simulation called real-time, the execution time of the simulation has to be shorter or equal to the selected time step in the real clock. Generally, it is recommended to have a waiting time, also called idle time (shown in Fig 117. (b)). This idle time between two step times ensures a simulation in real-time. Our real-time simulations use OPAL-RT simulators, which are able to execute calculation fast enough to simulate real-time.

### IV.3.2 HIL simulation definition

Hardware-in-the-Loop (HIL) simulation is a real-time simulation associated to control system test. It is a rigorous and dynamic manner with reduced experimental risk and cost [98]. It is considered as a bridge between traditional software non-real-time simulation and real physical system [99]. This technique is used to test control platforms in HVDC systems [100] and considered as a crucial stage for the design and development of controllers [101] for power converters.

HIL simulation combines computer simulation and Hardware under Test (HuT) shown in Fig 118. The HuT is implemented in a physical device while Rest of System (RoS) is simulated in real-time. As the test objective is the validation of the control, the hardware of the HIL simulation is the real control card. This type of HIL simulation has no real power transfer.

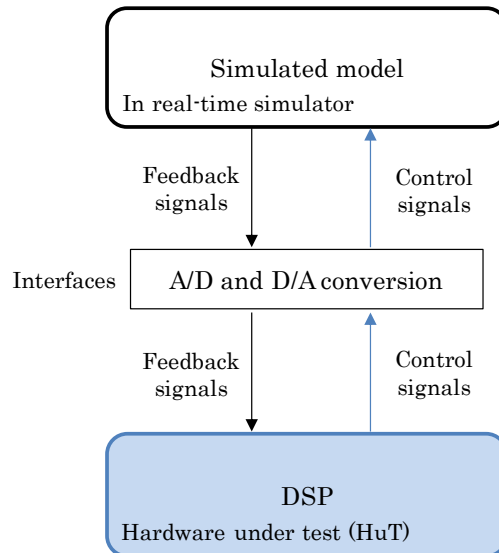


Fig 118. HIL simulation concept [96]

The chapter uses DSP TMS320F28377D of Texas Instrument as HuT to test the proposed control. The converter model is realized in the real-time simulators (OP5600 and 5607). Fig 119 is the HIL simulation structure.

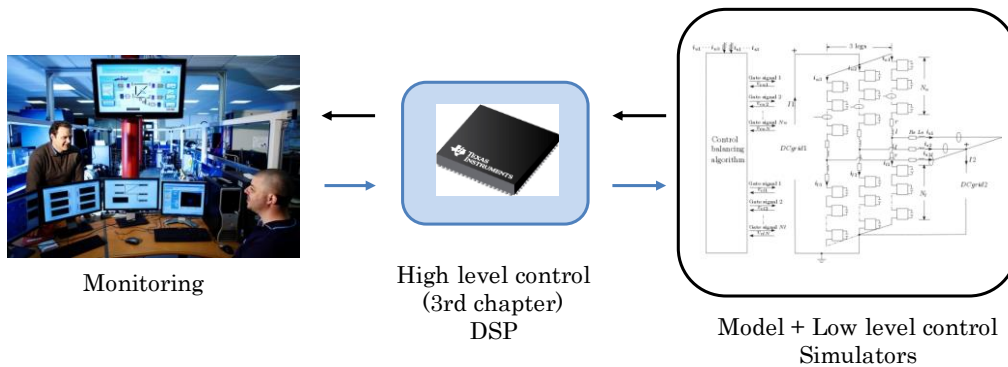
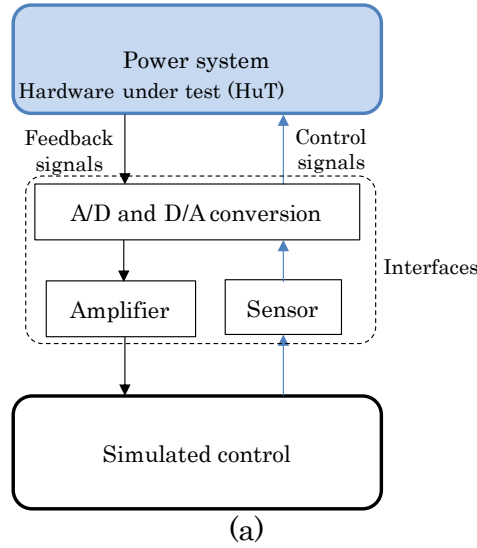
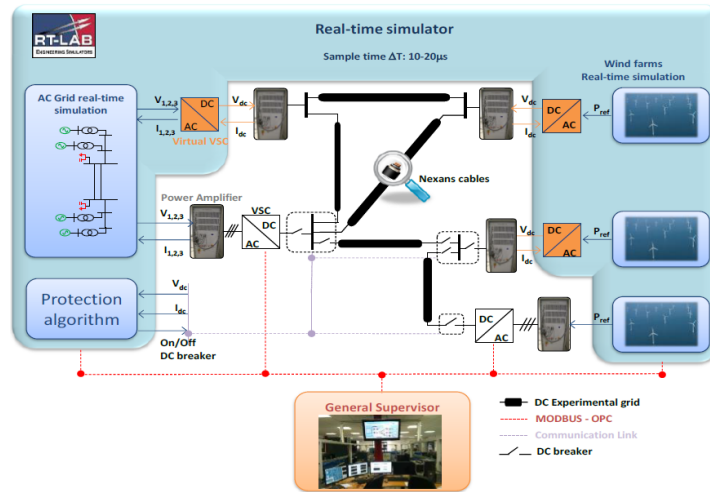


Fig 119. HIL simulation structure

There is also another type of HIL simulation with power transfer “Power HIL simulation (PHIL)”. Its principle concept is that power converter is the test target instead of control. Then, control can be simulated or implemented in a real control card (Fig 120. (a)). Fig 120. (b) is PHIL simulation used in the project TWENTIES [95].



(a)



(b)

Fig 120. (a) PHIL simulation concept [96] (b) PHIL simulation used in TWENTIES [95]

### IV.3.3 Simulations development methodology

From non-real-time simulation based on Matlab to HIL simulation (or experimental test) (Fig 121), several possibilities exist under different models and different simulations environment.

From left to right of Fig 121, our work chooses firstly a change of converter model, from the average model to instantaneous model (Fig 121. 1st stage (a)). Based on the instantaneous model, simulations environment are changed from Matlab to the real-time simulator (Fig 121. 1st stage (b)). The results obtained after these two changes are real-time simulation results.

The objective of the real-time simulation is to take into account capacitor voltages of each submodule and discretization of each arm voltage.

Based on the real-time simulation, control is implemented in an external DSP control card. The objective of HIL simulation is to take into account the neglected information transfer delay and precision used in the real DSP control card.



Experimental tests will be realized based on the validations of HIL simulations. The aim of the future experimental tests is to test the real M2DC converter (power and control), at a small voltage and current scale.

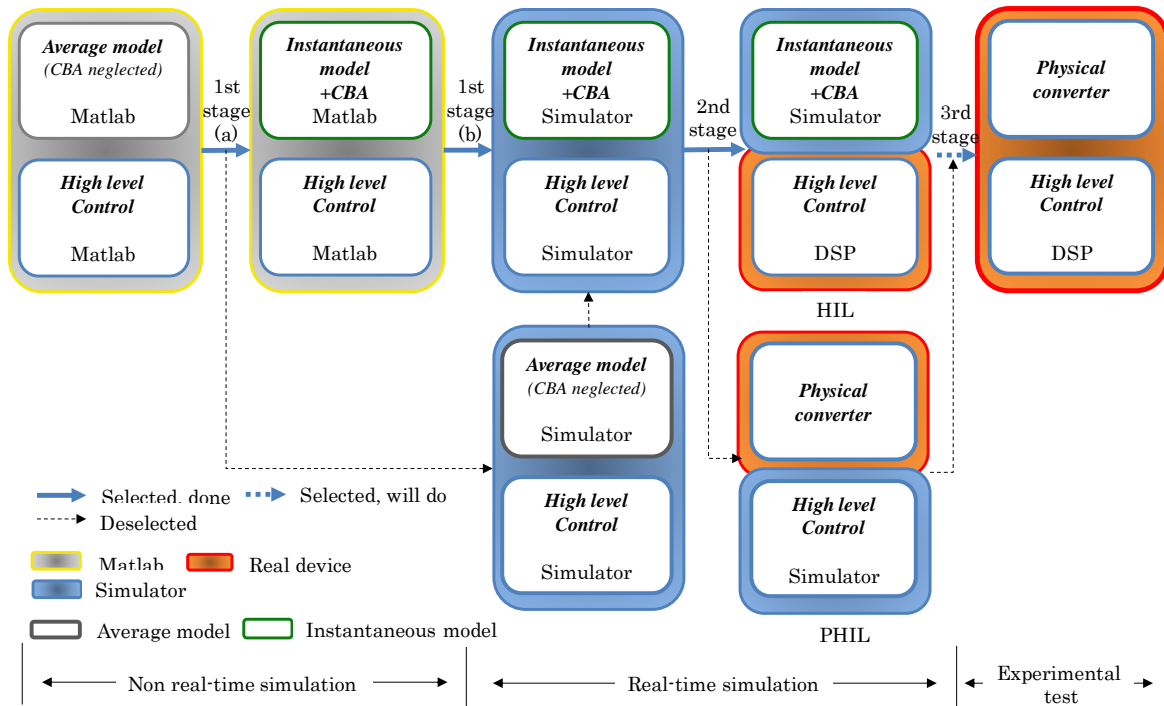


Fig 121. Test process

#### IV.4 Instantaneous model of an arm

The average model limitation is its lack of consideration, for example of the difference between each submodule voltage, voltage discretization, etc. Fig 122. (a) shows arm voltage obtained by the average model. The identical voltage of each capacitor is the average model assumption. To consider the voltage of each submodule, the instantaneous model is used that arm voltage obtained by the instantaneous model is shown in Fig 122. (b).

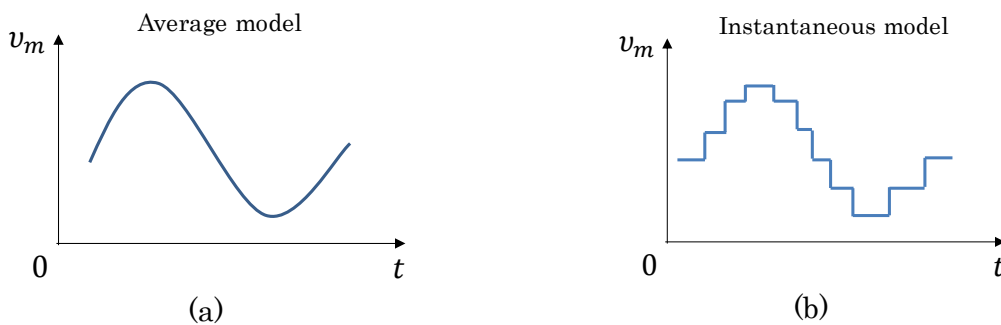


Fig 122. Arm voltage with (a) average model (b) instantaneous model

This model is a Thevenin equivalent circuit model proposed in [103] and [104] and validated by the laboratory in the case of MMC operation. It has advantages of the representation of each submodule and the reduction of heavy calculation.

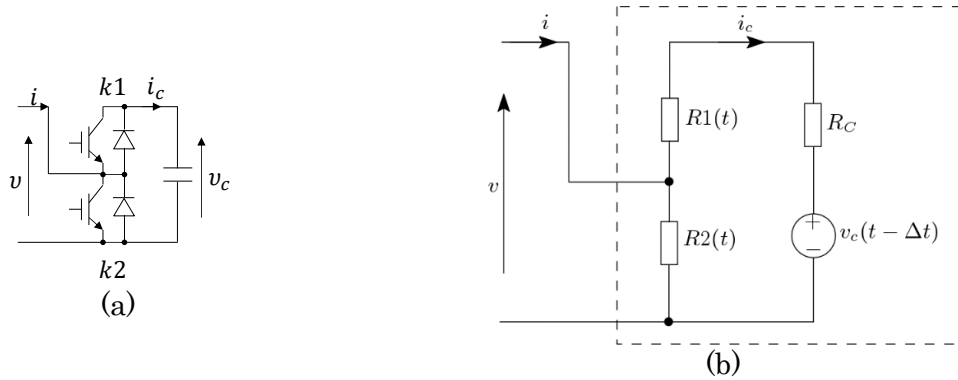


Fig 123. (a) Submodule (b) linearized submodule components

It considers semiconductors ( $k1$  and  $k2$  of Fig 123. (a)) as bidirectional ideal switches. Each semiconductor switch is represented by two linear equivalent resistors ( $R1(t)$  and  $R2(t)$  of Fig 123. (b)) [103] and [104]. The equivalent resistor is time dependent that changes in terms of switching state (Table 1).  $R_{ON}$  represents ON state, which has a small value ( $1m\Omega$  used value).  $R_{OFF}$  represents OFF state with a great value ( $10k\Omega$  used value). Two semiconductors of each submodule are assumed to be identical.

Table 18 Equivalent resistance values

Switching state	Equivalent resistance $R1(t)$	Equivalent resistance $R2(t)$
$k1$ is on, $k2$ is off	$R_{ON}$ ( $1m\Omega$ )	$R_{OFF}$ ( $10k\Omega$ )
$k1$ is off, $k2$ is on	$R_{OFF}$ ( $10k\Omega$ )	$R_{ON}$ ( $1m\Omega$ )

Moreover, the capacitor is modeled in [119] by an equivalent voltage source  $v_c(t - \Delta t)$  in series with a resistor  $R_c$  (Fig 123. (b)), where  $R_c$  is time dependent and capacitance dependent.

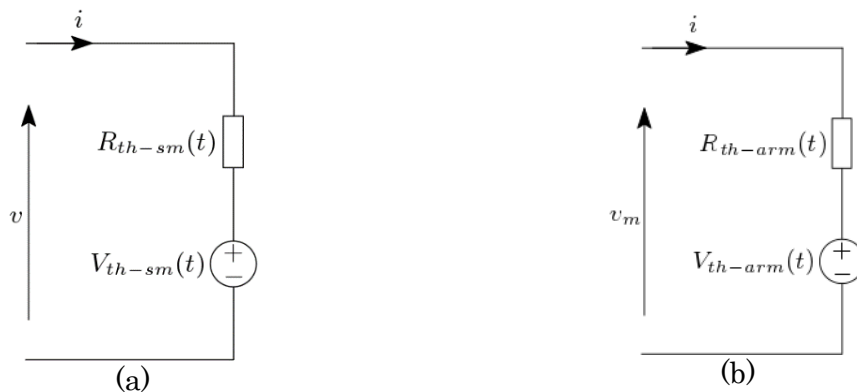


Fig 124. Instantaneous model of (a) submodule (b) arm

Therefore, each submodule (Fig 123. (a)) can be replaced by the equivalent circuit (Fig 124. (a)), which has a relation (IV.4.1).

$$v(t) = R_{th-sm}(t) \cdot i(t) + V_{th-sm}(t - \Delta t) \quad (\text{IV.4.1})$$

where expressions of equivalent resistance  $R_{th-sm}$  and voltage  $V_{th-sm}$  are described in (IV.4.2) [103] and [104].

$$R_{th-sm}(t) = \frac{(R1(t) + R_c(t)) \cdot R2(t)}{R1(t) + R_c(t) + R2(t)} \quad (\text{IV.4.2})$$

$$V_{th-sm}(t - \Delta t) = \frac{R2(t)}{R1(t) + R2(t) + R_c(t)} \cdot v_c(t - \Delta t)$$

For an arm, a series connection of submodules, the instantaneous model used is finally as shown in Fig 124. (a) and expressed in (IV.4.3).

$$R_{th-arm}(t) = \sum_{i=1}^N R_{th-sm_i}(t) \quad (\text{IV.4.3})$$

$$V_{th-arm}(t) = \sum_{i=1}^N V_{th-sm}(t - \Delta t)$$

where  $R_{th-arm}$  and  $V_{th-arm}$  is respectively arm equivalent resistance and arm equivalent voltage.

The advantage of this model is the reduction of calculations [103] and [104] and its application to any number of submodules. Its limitation is the lack of consideration of different semiconductors and non-linear characteristic of the V-I curve of semiconductors.

## IV.5 Low-level control

The objective of this part is to present the nearest level control (NLC) algorithm used in MMC mock-up. The same algorithm is used in M2DC converter since both converters use the same submodule topology.

The instantaneous model needs a low-level control (Capacitor Balancing Algorithm) to select submodule activation and obtain gate signals for each semiconductor. It has also another role of balancing capacitor voltage of each submodule. To realize the three functions, numerous control methods exist in the literature for MMC operation. They are pulse-width modulation (PWM) [105], space-vector modulation (SVM) [106] for high switching frequency applications and selective harmonic elimination (SHE) [107], nearest vector control (NVC) [108], [109], nearest level control (NLC) [110]-[112] for low switching frequency applications.

Since M2DC is particularly proposed for high voltage and high power applications, switching frequency is expected as low as possible to reduce semiconductor switching losses. Therefore, NLC is suitable for its reduction of switching frequency and its simplicity of conception and implementation.

The basic NLC algorithm [110], [111] is described in Fig 125.

- It uses the nearest integer voltage level (round function) to generate gate signals through a classical voltage balancing algorithm.
- The voltage balancing algorithm (CBA) is an algorithm to balance the submodule capacitor voltage. The algorithm selects ON state submodules according to two criteria: capacitor voltage and current direction. If arm current is positive, algorithm activates  $n$  number submodules, which have lowest capacitor voltages, to charge them. If arm current is negative, algorithm activates  $n$  number submodules, which have highest capacitor voltages, to discharge them. The OFF state submodules keep their capacitor voltages constant.
- Gate signals of each submodule are obtained after the voltage balancing algorithm.

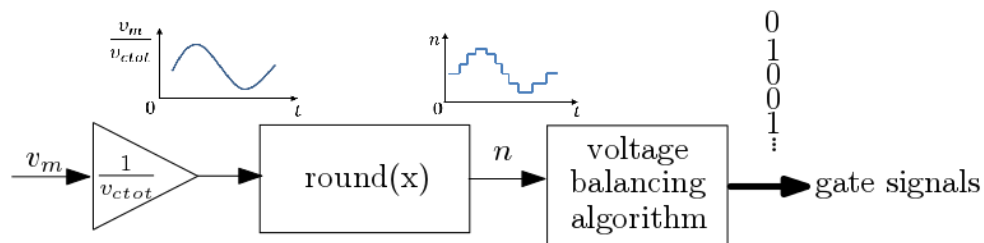


Fig 125. NLC algorithm

Based on the basic NLC algorithm, the algorithm implemented in the mock-up has two improvements to reduce unnecessary switchings. The first improvement consists of executing the voltage balancing algorithm, only if the submodule number changes ([113], [115] and [116]). The second improvement uses a predefined voltage tolerance ([113], [115] and [116]). If the difference between highest and lowest voltage is greater than the voltage tolerance, the voltage balancing algorithm is executed, on the contrary, semiconductor states keep unchanged.

## IV.6 Description of simulation devices

### IV.6.1 Description of real-time simulation devices

The non-real-time simulation uses MATLAB Simulink software to build the average model and control. Model and control are simulated with a step time of 60us.

In the real-time simulation, instantaneous model, low-level control and high-level control are built in the simulators using MATLAB Simulink interface. Calculation of the

model and low-level control is faster than high-level control to ensure the independence of two levels control. Therefore, simulations use a 20us time step for the model and the low-level control and a 60us time step for the high-level control.

Table 19 describes simulation devices for non-real-time simulation and real-time simulation.

Table 19 Simulation devices

	Non-real-time simulation	Real-time simulation
Hardware	-	OPAL-RT simulator (CPU, FPGA) [96]
Application software	MATLAB Simulink	RT-Lab (MATLAB Simulink) [96]
Operating system (OS)	Windows	Host OS: Windows Target OS: Linux (RedHat) [96]
Simulation time	Average model: 60us No low-level control High-level control: 60us	Instantaneous model: 20us Low-level control: 20us High-level control: 60us

#### IV.6.2 Presentation of HIL setup

HIL setup is shown in Fig 126 where the high-level control described in the third chapter is implemented in the DSP with a C code generated by Matlab Simulink.

DSP TMS320F28377D possesses two 32-bit CPUs, which work at 200MHz. HIL uses only one CPU. The other CPU will be useful in the mock-up test to increase the calculation speed but is not presented in this manuscript. Analog-to-Digital Converters (ADCs) of the DSP is selected at 12-bit mode that each analogue measurement is converted to a 12-bit digital signal to be recognized by the DSP.

The converter model and its low-level control are simulated in the simulators (OP5600 and OP5607). The current and voltage measurements are obtained by the simulators from the model via A/D and D/A conversion. DSP takes the measurements to provide modulation signals to low-level control.

HIL uses the same model and test scenarios (Table 16) as real-time simulations. To reduce the number of sensors, only six currents are measured instead of nine currents: currents of three upper arms and three secondary currents. The currents of lower arms are obtained by subtraction of the two measured currents. For the voltage measurement, each submodule has its own capacitor voltage measurement.

Fig 127 is the HIL experimental setup. Two simulators communicate via optical fibre. Their analogue input, output and digital output are connected to two driver circuit to transfer information to the DSP. These two driver circuits require a 3V and 5V power supply.

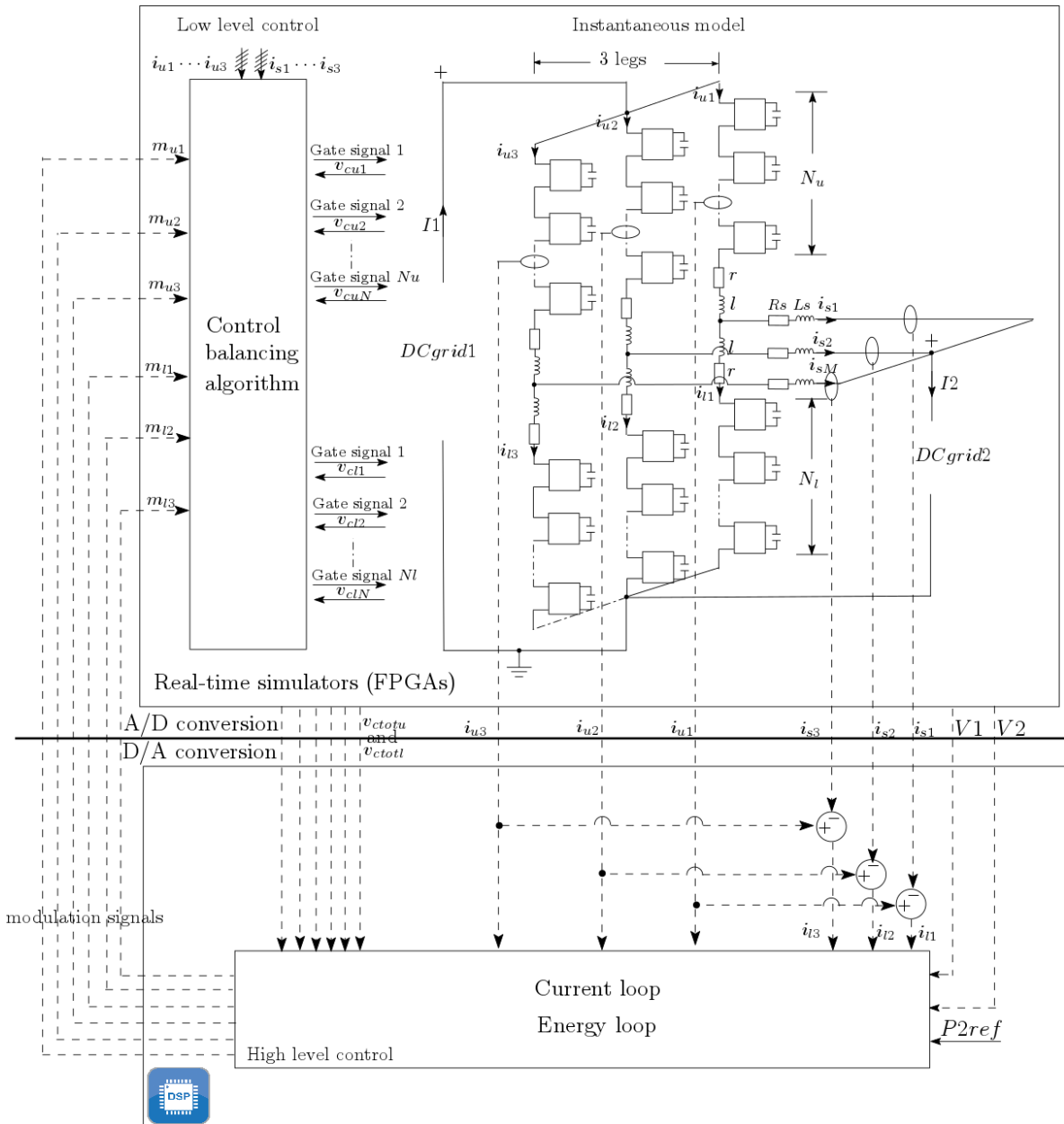


Fig 126. Detailed HIL test structure

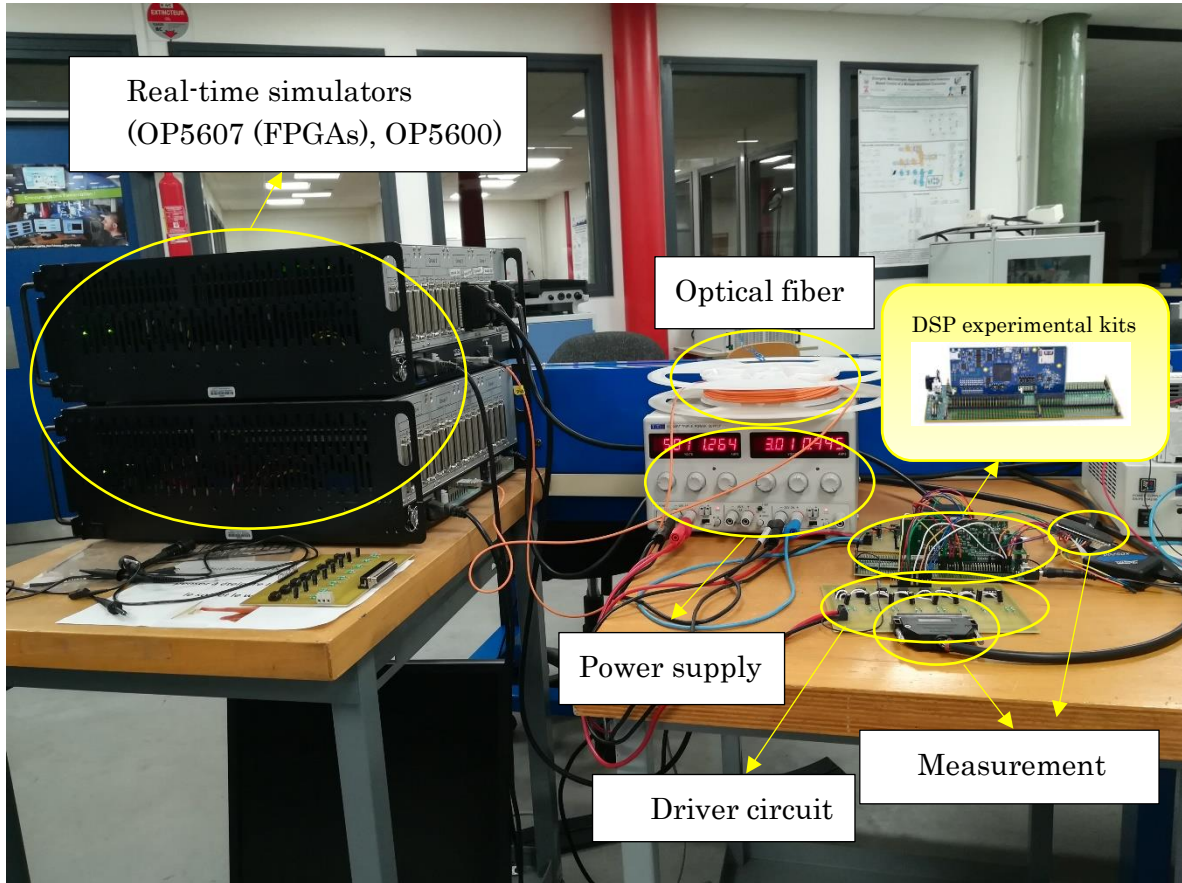


Fig 127. HIL experimental setup

## IV.7 Comparison and validation

Real-time simulations aim to validate the average model of converter using a comparison between the average model and the instantaneous model. The objective of HIL is to test high-level control in real condition via DSP. Simulations use specifications obtained in Table 16.

### IV.7.1 Simulation results in the steady state

#### IV.7.1.1 Test case 1

Case 1 has results shown in Fig 128 for the different steps of the work: (a) Non-real-time simulation, (b) real-time simulation and (c) HIL simulation. Results are presented in four parts: DC current, arm voltages, arm current and equivalent capacitor voltage.

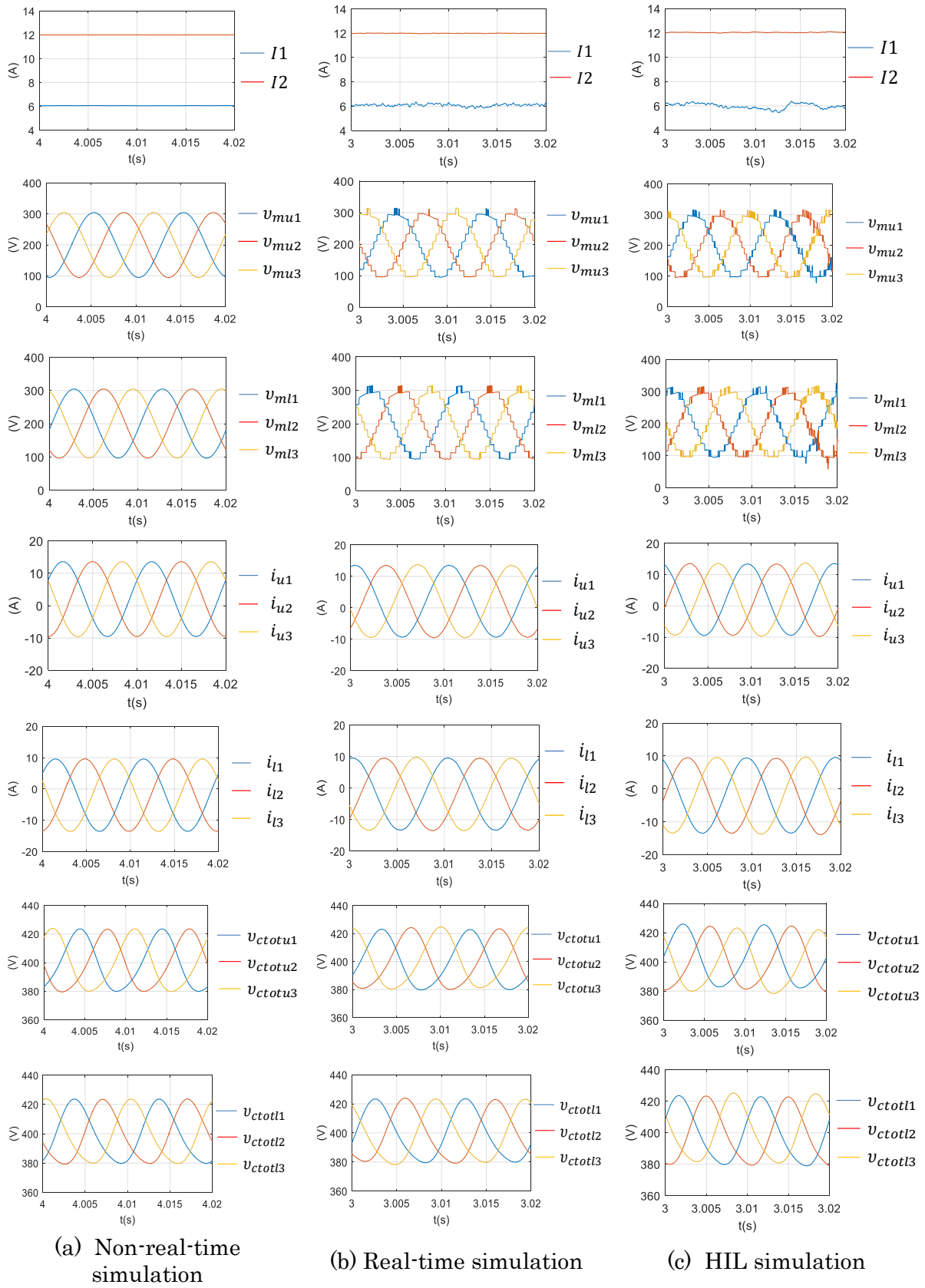


Fig 128. Case 1 in steady state



➤ DC currents results:

DC currents are as continuous as expected in non-real-time simulation. Their quality declines in the real-time simulation due to the consideration of each submodule in the instantaneous model. However, the presence of harmonics is more often in current  $I1$  than current  $I2$ , since current  $I2$  is directly controlled instead of the input current  $I1$ .

In HIL simulation, DC currents contain more harmonics than real-time simulation, particularly in current  $I1$ . The difference combines information transfer delay, DSP calculation precisions and current loop delay.

Finally, DC currents are numerically expected as 6A ( $I1$ ) / 12A ( $I2$ ) in the three simulations, which is conform to the expectation.

➤ Arm voltage results:

As non-real-time simulation uses the average model, arm voltage is considered as a perfect voltage source. This is the reason for the smooth arm voltages in non-real-time simulation. With instantaneous model associated with the low-level control, real-time simulation has a discretization in the arm voltage, which is instantaneously an addition of each capacitor voltage. But the global evolution is the same as non-real-time simulation. Moreover, it is remarkable that semiconductors have more switching at the top of sine waves since  $dv/dt$  is lower at the top than in the middle of a sine wave. At the top, low level control has more choices to charge or discharge capacitors, then more movement and higher switching frequency.

In HIL simulation, arm voltages are almost the same as in real-time simulation, but with more semiconductors switchings. This observation is confirmed by the measurement of the average switching frequency in Fig 131. The switching frequency is greater in HIL simulation than in real-time simulation. The difference is due to DSP calculation precision lower than Matlab. Similar capacitor voltages have more chances to be selected by the low-level control. Therefore, switching frequency in HIL simulation is slightly higher than in real-time simulation.

Finally, with the reduced frequency and power, a 102V amplitude of AC voltage is numerically obtained as in theory (Fig 129), which is confirmed by simulations.

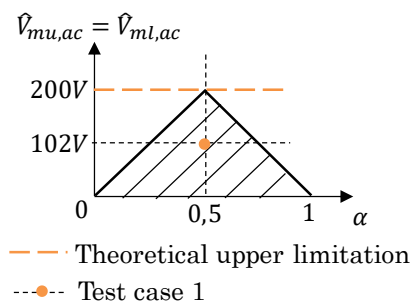


Fig 129. AC voltage component in case 1

➤ Arm current results:

The three types of simulation have almost the same arm currents with a maximum 0.5A difference. The discretization in arm voltage is not present in arm current thanks to inductors of the converter.

Current frequency and phase confirm the converter operation conditions. Since secondary inductor is great, the current of the upper arm and lower arm are almost in phase in the three simulations. Each current has a 100Hz frequency.

Finally, arm currents with measured peak value +/-13.9A are numerically under the rated current of semiconductor and confirm the previous converter current limitation analysis. In currents, an 11.49A AC components are theoretically found. As shown in Fig 130, this AC current can be reduced by an increase of frequency, which increases potentially the switching frequency. Therefore, the 100Hz selection in the simulation is a compromise between current and switching frequency.

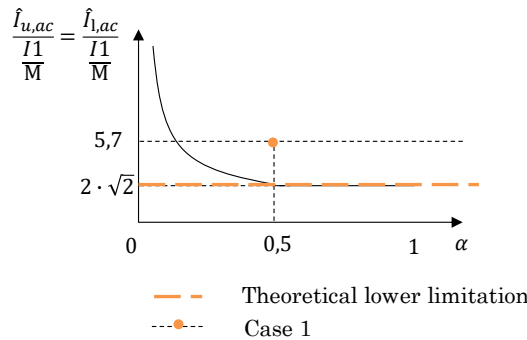


Fig 130. AC current component in case 1

➤ Equivalent capacitor voltage results:

Case 1 uses the symmetrical structure of M2DC converter. The MMC mock-up has been built with similar capacitances of each submodule. Therefore, equivalent capacitor voltages of the upper and lower arm have similar ripples in all simulations.

With consideration of capacitors as voltage sources, the equivalent voltage has identical ripples in three phase-legs. But using the instantaneous model in real-time simulation and HIL simulation, the equivalent voltage of three phase-legs are slightly different to due differences of charge and discharge of each capacitor.

Finally, voltage ripples  $\Delta v_{ctotu}$ ,  $\Delta v_{ctotl}$  are theoretically expected of 18V, then 36V of peak to peak value, which correspond around 10% of the average value  $\langle v_{ctotu} \rangle$ ,  $\langle v_{ctotl} \rangle$ . All the simulations show 44V of the peak to peak value, then around 11% of ripples. The slight difference can come from the approximations made in the capacitance design method.

To conclude, Fig 128 shows the global results of the converter confirming the operation analysis. More details of submodules are shown in Fig 131, which contains 20 submodules capacitor voltages of upper and lower arm in real-time (a) and HIL simulation (b). The average switching frequency is also measured.

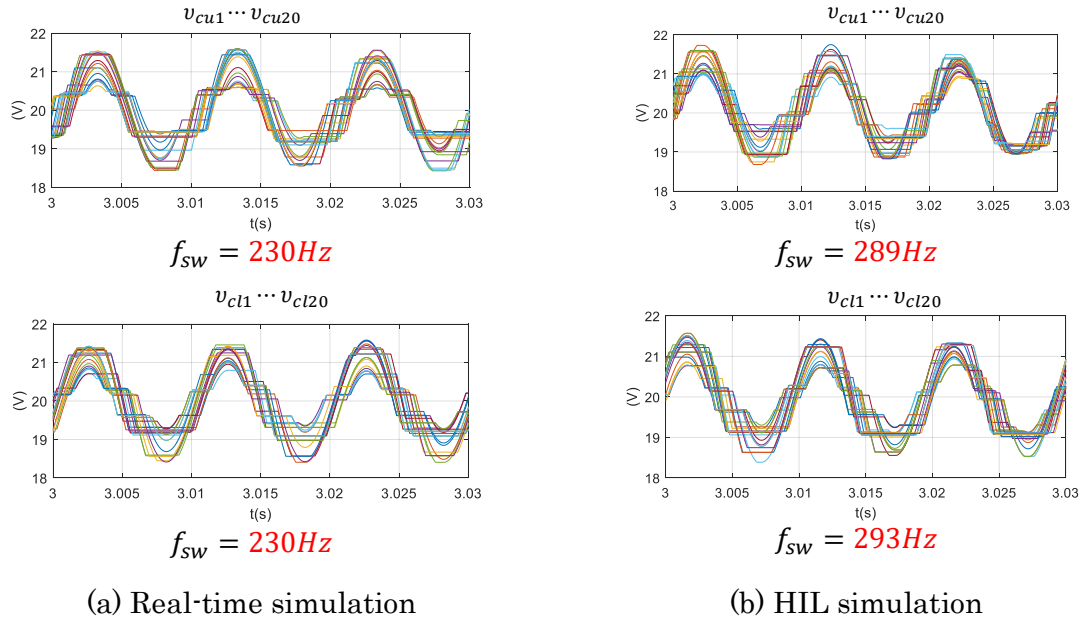


Fig 131. Case 1 capacitor voltages of M2DC leg

As can be seen, all capacitor voltages are around 20V in real-time simulation and in HIL simulation. Both simulations show almost the same switching frequency in upper and lower arms since the upper and the lower arm uses the same number of submodules with same voltage constraints.

To confirm the switching frequency, the work uses average frequency measurement with formula as (IV.7.1).

$$f_{sw} = \frac{\Sigma_{times\_ON}}{t \cdot n_{measured}} \quad (IV.7.1)$$

where  $n_{measured}$  is the number of measured semiconductors of an arm.  $t$  is the total simulation time.  $\Sigma_{times\_ON}$  is the total number of times that  $n_{measured}$  semiconductors switch to ON state in a simulation time  $t$  (Fig 132).

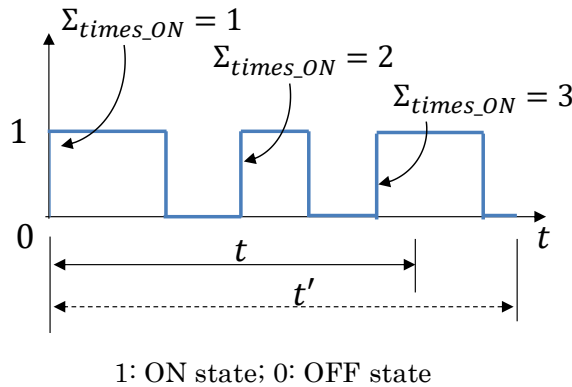


Fig 132. Example of switching frequency calculation

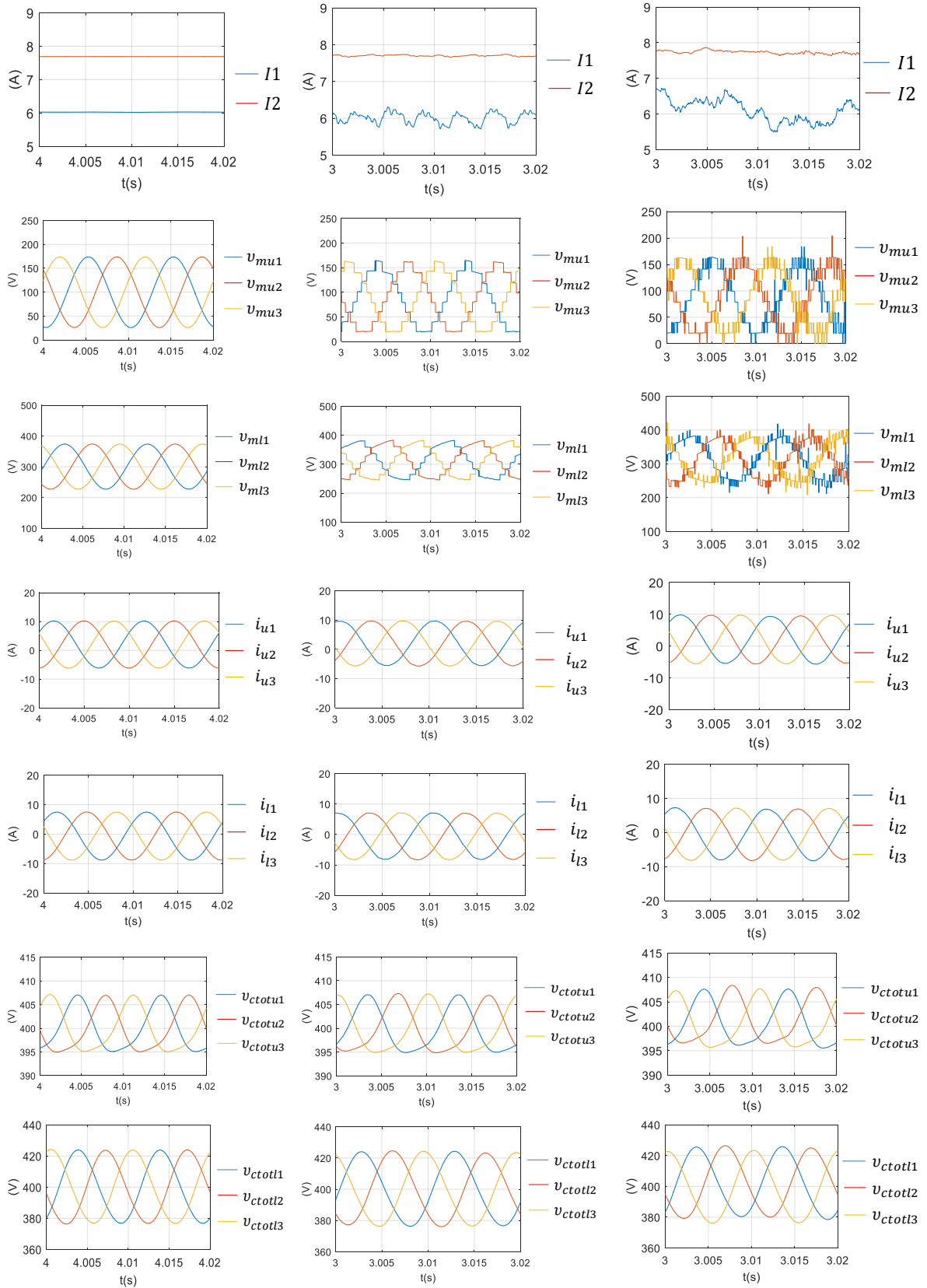
This is an easy method to estimate the average frequency of semiconductor in a period. However, the frequency depends strongly on the simulation time ( $t$ ) measurement. As shown in Fig 132, with the same  $\Sigma_{times\_ON}$  and  $n_{measured}$ , frequency  $f_{sw}$  will be different depending on simulation time  $t$  or  $t'$ . With increasing simulation time, the difference between  $t$  and  $t'$  is negligible. Then frequency measurement is more accurate. But to avoid memory explode, each simulation time varies from a few seconds to a few tens of seconds.

Fig 131 shows around the 200Hz frequency of arm in two simulations, which confirms the low-level control in case 1. The increase of frequency in HIL simulation is due to two reasons: measurement precision and DSP precision.

Firstly, two types of simulation have different simulation time. Simulation time influences directly the frequency results. Therefore, two simulations have a different frequency. Secondly, an increase of switching frequency in HIL simulation is due to the lower precision of DSP. It makes more choices to the low-level control, then higher frequency, as shown in arms voltages of Fig 128. (c).

#### **IV.7.1.2 Test case 2**

Case 2 uses the asymmetrical structure of the converter, where the number of submodules in upper arms is oversized. Three types of simulation are shown in Fig 133. (a) Non-real-time simulation, (b) real-time simulation and (c) HIL simulation. Like case 1, explications of case 2 have four parts: DC currents, arm voltages, arm currents, equivalent capacitor voltages. The final conclusion shows more details of the capacitor voltage of each submodule.



(a) Non-real-time simulation

(b) Real-time simulation

(c) HIL simulation

Fig 133. Case 2 in steady state

➤ DC current results:

As in case 1, DC currents of case 2 are obtained as expected in Non-real-time simulation with the average model, where submodules are not present individually. But this good continuity is no longer true in real-time simulation and HIL simulation, where each submodule is taken into account.

In the real-time simulation, the main harmonic present in current  $I1$  is the third harmonic. It comes directly from errors of currents in the three upper arms and from the fluctuation of internal capacitor voltages. Harmonics can be explained by the internal energy of the converter, since power, then DC current, is controlled by energy  $W_c^2$ . The undersized number of submodules in lower arms relatively to the value of DC voltage  $V2$  should cause more fluctuations in capacitor voltages and energy  $W_c^2$ .

In HIL simulation, due to the lower DSP precision, harmonics of current  $I1$  are amplified.

The current quality issue can be improved by reducing response time in current loops. But the solution can only be realized in real-time simulation, not in HIL simulation. It requires a faster DSP than TMS320F28377D. Therefore, to improve the current quality, three propositions are: decrease number of submodules in upper arms and increase the lower one, design submodule capacitance with the same voltage ripples in upper arms, and lower arms and control separately DC component and AC component of arm currents.

Finally, DC currents are numerically expected at 6A ( $I1$ ) / 7.7A ( $I2$ ), which correspond to the three simulation results.

➤ Arm voltage results:

As shown in case 1, case 2 has arm voltage discretized in real-time simulation and HIL simulation due to the association of the instantaneous model and low-level control.

As talked about previously, case 2 has an oversized number of submodules in upper arms and undersized in the lower one. In the real-time simulation, level numbers are similar between the voltage of upper arms and lower arms. Depending on the operation condition, the work chooses  $\hat{V}_{mu,ac} = \hat{V}_{ml,ac}$ . This choice is the reason of similar voltage level number in the simulation. But due to different capacitor voltages, level number (8 levels) of upper arms is slightly greater than lower arms (6 levels).

In HIL simulation, level numbers are increased in upper arms (10 levels) and lower arms (9 levels) due to the lower precision of DSP than the simulator.

Finally, the amplitude of the AC component voltage is obtained theoretically as 68V, which can be confirmed by the simulations (Fig 134).

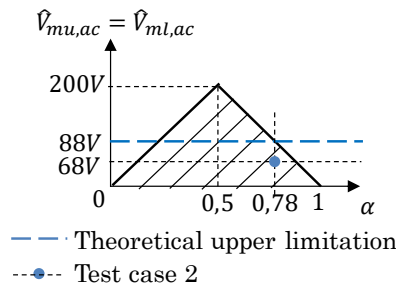


Fig 134. AC voltage component in case 2

➤ Arm current results:

Arm currents of three simulations are almost the same. As explained in case 1, the discretization of arm voltage is not directly observable in the currents due to inductors of the converter. Regarding phases, currents of upper arms and lower arms are almost in phase by the great value of the secondary inductors. Regarding frequency, the 100Hz frequency value is confirmed by three simulations. Finally, the upper arm and lower arm have the same amplitude of AC currents. The theoretical value is 7.6A shown in Fig 135, which is 3.8 times greater than DC current. This AC current is confirmed by simulations.

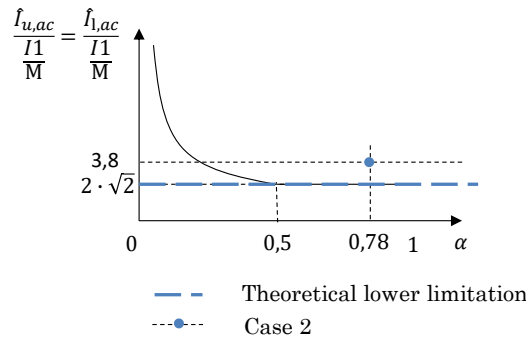


Fig 135. AC current component in case 2

➤ Equivalent capacitor voltage results:

The asymmetrical case 2 has different energy stored in upper and lower arms. With the same capacitance value imposed by the mock-up, different voltage ripples are obtained in equivalent capacitor voltage of each arm. Three simulations show that lower arm ripples are four times greater than upper arm ripples.

As explained in case 1, real-time simulation and HIL simulation consider individually each capacitor of submodules, then slight differences in equivalent capacitor voltage of each arm.

Moreover, Fig 136 shows capacitor voltage of each submodule in one leg in real-time simulation and HIL simulation.

In the real-time simulation, the oversized number of submodules is shown by the large time of OFF-state of semiconductor in the upper arm where voltage is kept constant. Comparing to the upper arm, semiconductors of the lower arm are often in the ON-state that capacitors are charged and discharged in terms of time. Despite the oversized upper arm, all submodules are engaged in the operation, as the lower arm as well. But regarding switching frequency, semiconductors of the upper arm has a lower average frequency than the lower arm due to the oversized submodule.

In HIL simulation, the converter needs more switching movement to make the sine wave of the arms with the same converter model and low-level control as real-time simulation. As mentioned in case 1, frequency measurement is not accurate. But the greater difference between two types of simulation is principally considered due to lower precision of DSP. Since the upper arms are oversized, more capacitors have similar voltage from the view of DSP than real-time simulation. Then low-level control has more choices

to select a semiconductor, then greater frequency. Therefore, reducing the upper arm submodules number is a possible solution to reduce capacitor choices to low-level control.

Finally, comparing both arms, the upper one has a lower frequency than the lower one. All capacitor voltages are maintained around the same operation voltage 20V and equivalent capacitor voltages are maintained at 400V.

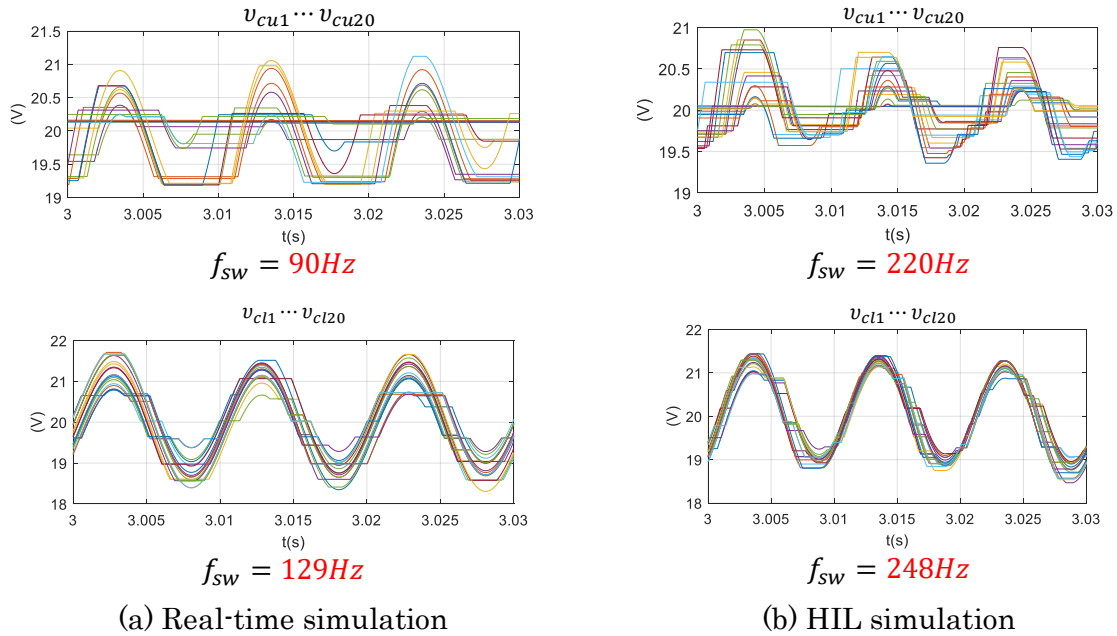


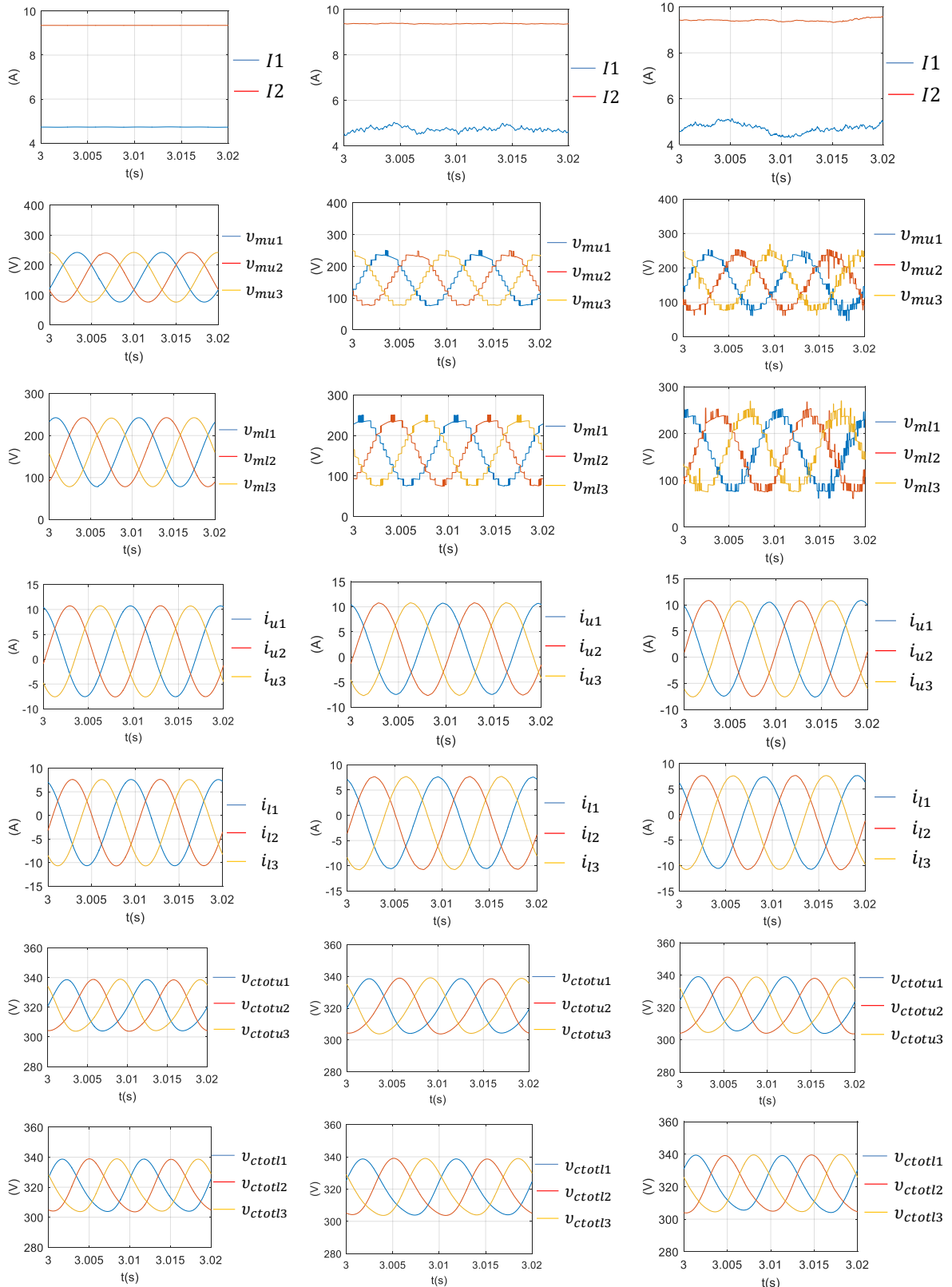
Fig 136. Case 2 capacitor voltages of M2DC leg

To conclude, case 1 and case 2 are able to transmit the same power with a different ratio, which creates different AC power, and AC components in voltage and current. Generally, the M2DC converter is convenient to operate with low AC power to limit losses. But for M2DC realized with an existing MMC converter, it might be a disadvantage to be an asymmetric structure, without specific transformation and adaptations.

#### IV.7.1.3 Test case 3

Case 3 tests the symmetrical structure of M2DC in reduced DC voltage. Three types of simulation results are shown in Fig 137. (a) Non-real-time simulation, (b) real-time simulation and (c) HIL simulation.





(a) Non-real-time simulation

(b) Real-time simulation

(c) HIL simulation

Fig 137. Case 3 in steady state

➤ DC current results:

As case 1 and case 2, DC currents of case 3 have more harmonics in real-time simulation and HIL simulation than non-real-time simulation due to the utilization of instantaneous models. Regarding the symmetrical case 1, case 3 has visually more harmonics. But compared to the asymmetrical case 2, the current quality of case 3 is better than case 2.

In the real-time simulation, the harmonics are supposed to come from low-level control. Since the reduced DC voltage decreases the capacitor voltages (shown in Fig 140), the predefined voltage tolerance in the low-level control might be not suitable with new capacitor voltage. The low-level control can have influences on DC current quality.

In HIL simulation, low precision is still a cause of amplification of harmonics.

Finally, DC currents are numerically confirmed by 4.6A ( $I_1$ ) / 9.3A ( $I_2$ ) as shown in the three simulations.

➤ Arm voltage results:

As non-real-time simulation uses average models, arm voltages are perfect sine waves with DC offset. The consideration of each submodule makes real-time simulation and HIL simulation have discretization in arm voltages.

The reduced DC voltage decreases the DC component of arm voltages. The symmetrical ratio keeps the same DC components in upper and lower arms.

In the real-time simulation, comparing to the symmetrical case 1, case 3 has the same voltage levels (11 levels) in the upper and lower arm than case 1. If a level of case 1 worth to a submodule capacitor voltage (20V), the same number level with smaller AC voltage in case 3 indicates a reduction of capacitor voltage. This is confirmed in Fig 140, where each capacitor voltage is around 16V. Therefore, reduced DC voltage involves a decrease in each capacitor voltage.

In HIL simulation, the number of levels of arm voltage is the same as in real-time simulation. But frequency is higher than in real-time simulation (Fig 140). This increase of frequency is supposed to come from low-level control associated with low precision of DSP card, which neither exists in HIL simulation of case 1, nor in the real-time simulation of case 3.

Finally, the theoretical value of AC component voltage (Fig 138) is confirmed by three simulations.

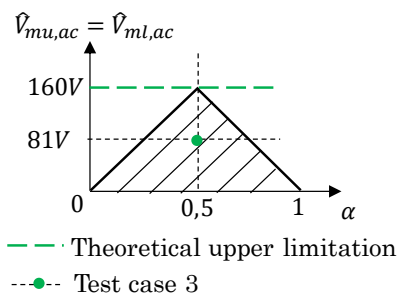


Fig 138. AC component voltage of case 3

➤ Arm current results:

Arm currents in three simulations are almost the same. Its AC component is confirmed by the theoretical value shown in Fig 139 and its frequency of 100Hz. In the three simulations, upper arms and lower arms currents are in phase due to the great secondary inductor.

The reduced operation frequency is the cause of increased AC current, which is six times greater than DC current  $I_1$ . Then, 100Hz frequency is a compromise of switching frequency and AC current, since operation frequency has an impact on the switching frequency of semiconductor. As the result, the switching frequency is around 220Hz in real-time simulation and 315Hz in HIL simulation.

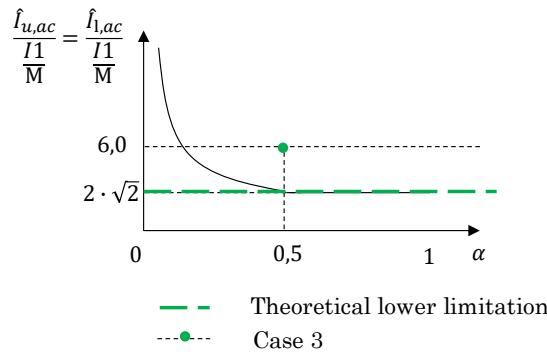


Fig 139. AC component current of case 3

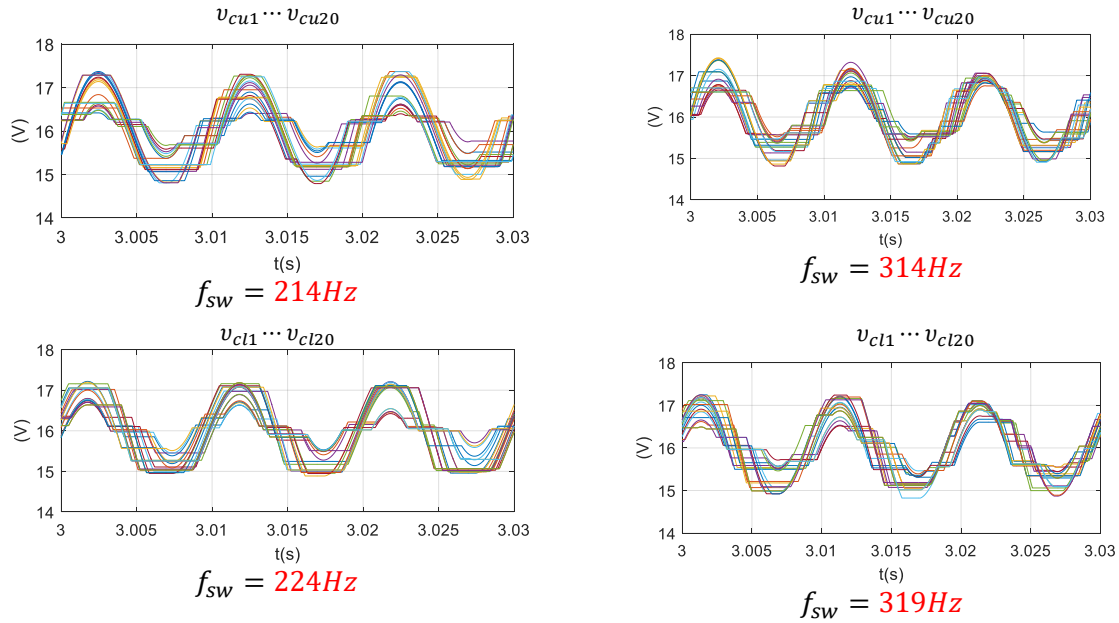
➤ Equivalent capacitor voltage:

In case 3, each capacitor are initially pre-charged to 20V as case 1 and case 2. Due to the reduced DC voltage, each capacitor voltage is finally maintained around 16V shown in Fig 140. Therefore, the equivalent capacitor voltages are maintained around 320V by 20 submodules.

Moreover, since case 3 is the symmetrical case, ripples in the capacitor voltage are the same. As shown in the three simulations, upper arms and lower arms have almost the same voltage ripples. This similarity of equivalent capacitor voltages ensures also the quality of DC currents that case 2 does not have.

As mentioned previously, the difference in switching frequency between real-time simulation and HIL simulation is due to low-level control and DSP precision.

Finally, a theoretical 8% ripples are confirmed by the three simulations.



(a) Real-time simulation

(b) HIL simulation

Fig 140. Case 3 capacitor voltages of M2DC leg

To conclude, case 3 confirms the good behavior of the converter with a reduced DC voltage. In this case, the power should be decreased to avoid overcurrent. The converter uses all submodules by sharing DC voltage to each submodule. The disadvantage is the possibility of changing switching frequency if the converter keeps the same low-level control.

Comparing the three previous cases, case 1 has a maximum AC power due to the highest power and highest DC voltage. Case 2 requires less AC power to transmit the same DC power as case 1. But due to its asymmetrical structure, the original MMC converter design is not suitable for an M2DC converter. Case 3 has less DC power, then less AC power, which is considered similar to case 1, except for their switching frequency.

#### IV.7.1.4 Test case 4

Case 4 tests the asymmetrical structure of the converter with reduced DC voltage. Three types of simulation are shown in Fig 141. (a) Non-real-time simulation, (b) real-time simulation and (c) HIL simulation. Case 4 can be considered as a combination of case 2 and case 3. Therefore, results combine the disadvantages of case 2 and case 3.

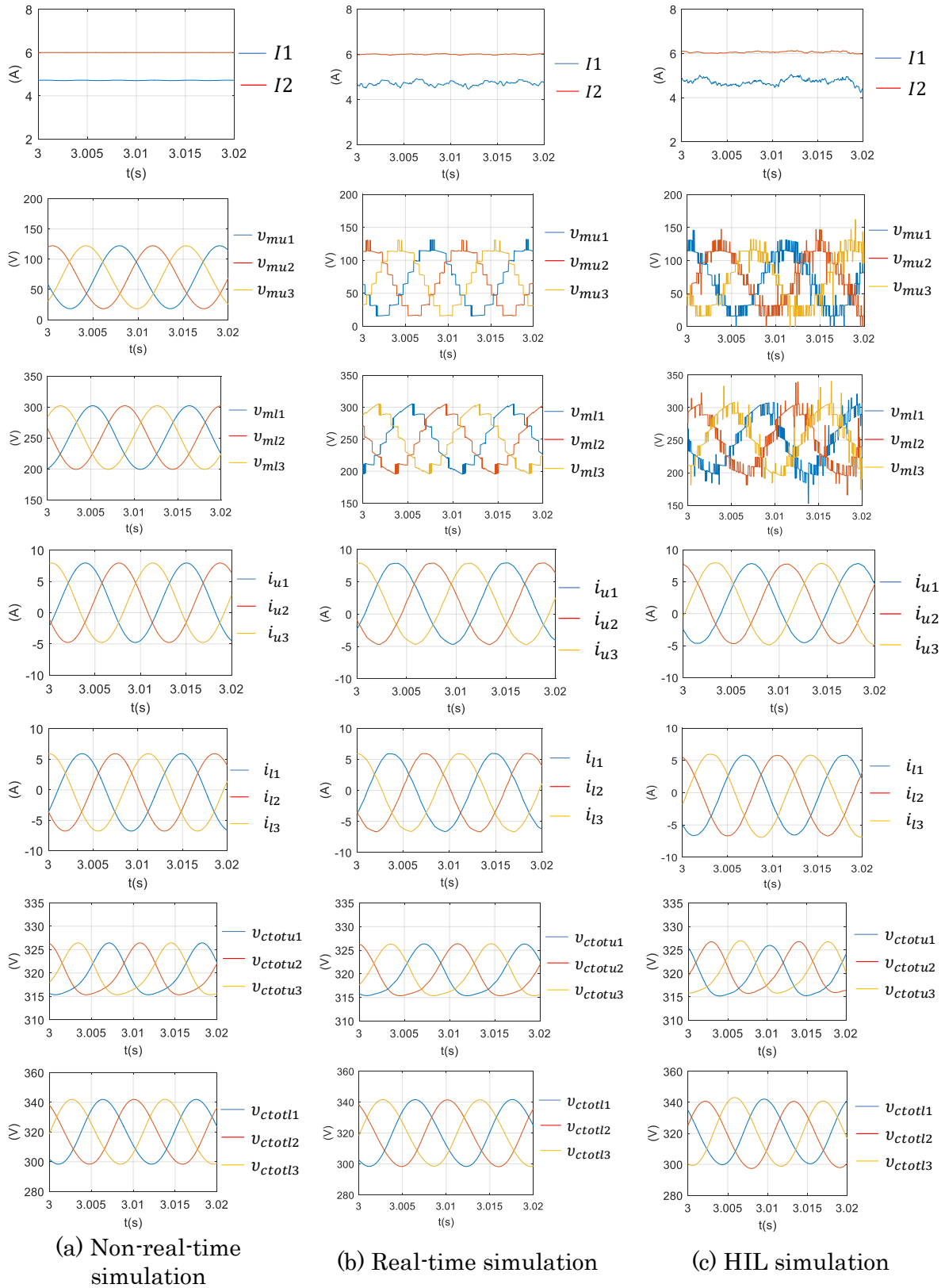


Fig 141. Case 4 in the steady state

➤ DC current results:

The average model makes DC currents continuous as in previous cases. In real-time simulation and HIL simulation, utilization of instantaneous models introduce more harmonics in DC currents. Since HIL simulation still has DSP precision issue, harmonics are amplified.

In the real-time simulation, case 4 has undersized lower arms. As shown in case 2, the undersized number of submodules influences ripples of capacitor voltages, then energy  $W_c^2$ . The third harmonics present, therefore, in DC current  $I_1$  in case 2. Case 4 inherits the third harmonic in DC current by the undersized number of submodules of lower arms. It could be improved by a decreased number of submodules in upper arms, design capacitors using same voltage ripples in the upper and lower arm and control separately DC current and AC current in arms.

Moreover, DC voltage of case 4 is reduced as in case 3 where low-level control could be unsuitable. It could be fixed by improving low-level control.

In HIL simulation, amplified harmonics are due to the DSP precision.

Finally, DC currents are numerically confirmed as 4.6A ( $I_1$ ) / 6A ( $I_2$ ) by three simulations.

➤ Arm voltage results:

Arm voltages are discretized by the instantaneous model in real-time simulation and HIL simulation. Due to the choices on AC voltages  $\hat{V}_{mu,ac} = \hat{V}_{ml,ac}$ , case 4 has similar AC voltages in the three simulations.

In the real-time simulation, case 4 has the same voltage levels as case 2, 8 levels in upper arms and 6 levels in lower arms. The slightly greater levels in upper arms is due to different equivalent capacitor voltages. The different voltages make also different waveform between voltages of upper arms and voltages of lower arms. Regarding case 2, the reduced DC voltage in case 4 decreases DC component voltages of arms. As mentioned previously, case 2 and case 4 have the same levels. Therefore, the decreased AC voltages in case 4 are realized by reducing capacitor voltages, which is confirmed in Fig 144. All submodules of the converter are engaged in the operation with each capacitor voltage reduced to 16V.

In HIL simulation, arm voltage levels are increased to 10 levels in upper arms and 8 levels in lower arms. The difference is explained by the difference in precision between DSP and Matlab.

Finally, the AC voltage of case 4 is theoretically 51V shown in Fig 142, which is confirmed by the three types of simulations.

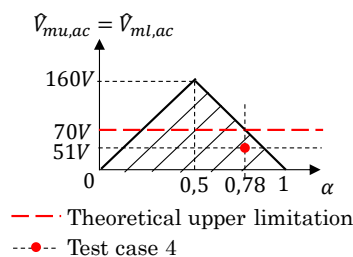


Fig 142. AC component voltage of case 4

➤ Arm current results:

The three simulations have almost the same arm currents with the designed frequency of 90Hz, which is different from the three other cases. Upper arms and lower arms are almost in phase due to the great value of secondary inductors.

Numerically, the amplitude of AC currents is 4 times greater than DC current, then 6.3A. This amplitude is optimized, as the frequency is near the limit value (Fig 143).

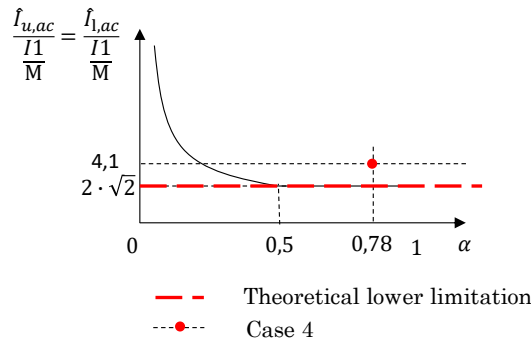
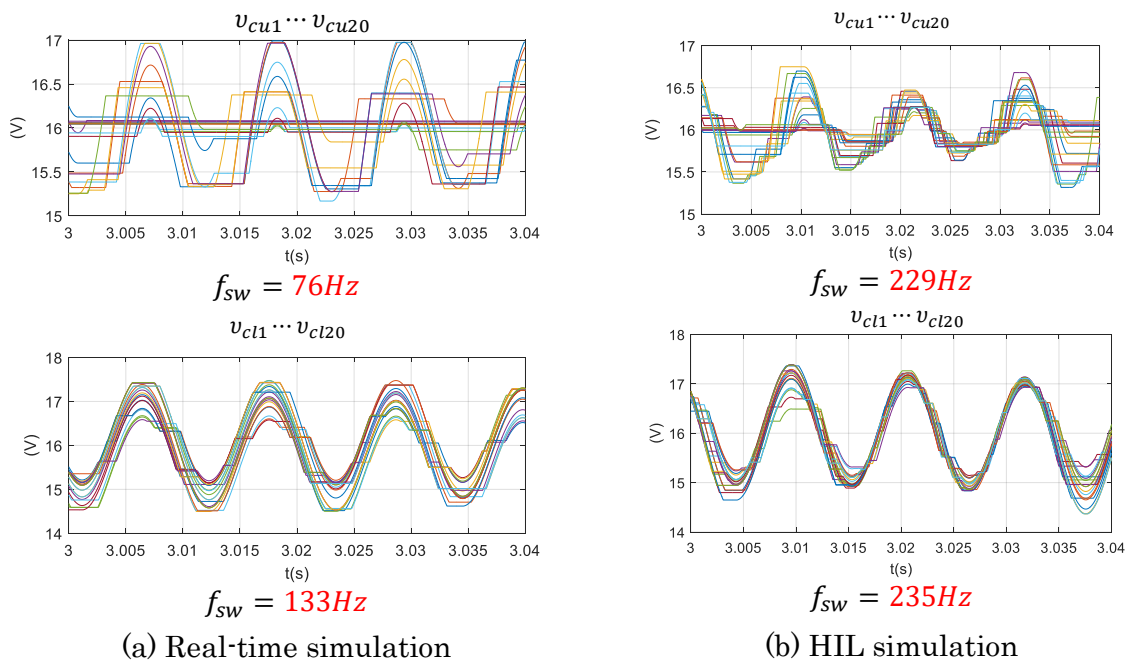


Fig 143. AC component current of case 4

➤ Equivalent capacitor voltage results:

As in case 3, each capacitor is initially pre-charged at 20V. Thanks to the low-level control, each capacitor share equally the reduced DC voltage to 16V. Therefore, 20 submodules of arms provide 320V equivalent capacitor voltage. The ripples are different between the upper and lower arms due to the asymmetrical structure. More details are shown in Fig 144.



(a) Real-time simulation

(b) HIL simulation

Fig 144. Case 4 capacitor voltages of M2DC leg

In the real-time simulation, the oversized number of submodules in the upper arms are shown by the large time of OFF-state of semiconductors. Each submodule of the converter is engaged in the operation. Due to the large semiconductors in OFF-state, upper arms have a lower frequency than the lower arms.

Comparing to the case 2, the reduced operation frequency decreases switching frequency in case 4.

In HIL simulation, switching frequency of upper and lower arms are largely increased due to low-level control and DSP precision. As mentioned in case 3, reduced DC voltage influences low-level control to be no longer suitable. Moreover, with an oversized number of submodules, the disadvantage of DSP precision is more visible.

To conclude, case 4 shows results about the change of DC voltage and ratio without changing converter design. It is confirmed that low-level control will impact results. Moreover, the asymmetrical structure of the converter requires a different design of capacitor in upper and lower arms to maintain similar voltage ripples, which is the base of low-level control.

Comparing four cases, it is generally confirmed that the ratio approached 1 is convenient for power transmission. Since case 2 and case 4 have less AC power, the converter has lower losses to transmit the same power as case 1 and case 3, respectively.

Switching frequency depends on the operation frequency of the converter, according to case 4. Case 4 has the lowest operation frequency, then the lowest switching frequency.

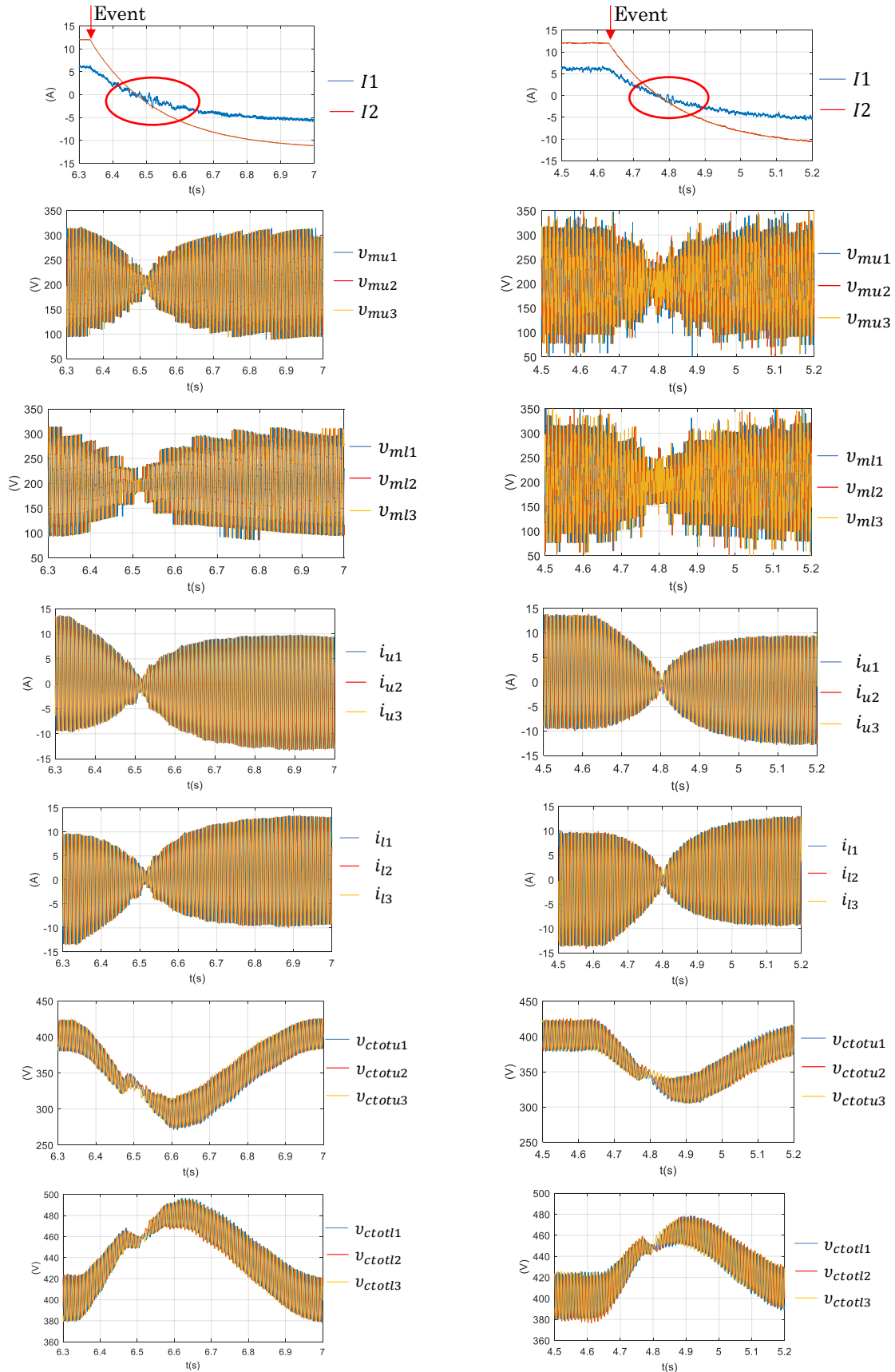
Case 2 and case 4 confirm the disadvantage of having an undersized number of submodules in lower arms.

#### *IV.7.2 Dynamic state: case 1*

Steady-state simulations confirm previously that M2DC is more convenient to be used as a classical MMC in case 1. DC currents of case 1 have fewer harmonics in HIL simulation regarding three other cases. Arm voltages and arm currents are almost overlapping between the three simulations. Case 1 does not have capacitor voltage ripples issue thanks to its symmetrical structure. Therefore, case 1 is selected to show the dynamic behavior of the converter to avoid coupling to different problems.

Case 1 tests the dynamic behavior of the converter control, where power reference is changed from 2400W to -2400W. The power at the positive part aims to test the converter in case of power reducing. The power at negative part aims to test the converter's bidirectional power. The results are shown in Fig 145. (a) Real-time simulation and (b) HIL simulation.





(a) Real-time simulation

(b) HIL simulation

Fig 145. Case 1 in the dynamic state

➤ DC current results:

DC currents are reduced with decreased power in real-time simulation and HIL simulation. The negative currents confirm bidirectional power capability of the converter. Therefore, the converter is able to control power flow in a DC grid.

As mentioned in chapter 3, the converter has zero power issue, which is confirmed by the two types of simulation. The proposition of this issue is the necessity to review the design choice  $\hat{V}_{mu,ac} = \hat{V}_{ml,ac}$  and  $\theta = 90^\circ$ . It makes the amplitude of AC voltage changes in terms of power. In the case of zero power, the amplitude is supposed to be zero, which is inconvenient to the converter operation. To keep AC voltage maximum, it is proposed to control angle  $\theta$  instead of amplitude at low power.

➤ Arm voltage results:

When power is positive, the decreased power reduces AC components of arm voltages. DC components are kept constant by DC grids. When power is negative, the increased negative power increases AC components of arm voltages. Therefore, whatever the power direction, AC voltage is proportional to power.

➤ Arm current results:

DC components of arm currents depend on power direction. If power is positive, upper arms have positive DC components. Lower arms have negative DC components. AC components of arm currents depend on AC voltages. Therefore, the AC voltages reduced by power decrease the AC current. Then, increased negative power increases AC voltages and AC currents.

➤ Equivalent capacitor voltage results:

Equivalent capacitor voltages are maintained around 400V during the power variation. The two simulations show that the energy loop takes around 0.5s to reach steady state. The overshoot of the loop has a value of 100V, which is shared on all submodules of arms (5V by submodule).

To conclude, case 1 has an acceptable dynamic using MMC mock-up. At zero power, the design condition should be deepened to preserve the capacity control of the converter.

## IV.8 Conclusion

The objective of real-time and HIL simulation is to validate the theoretical analysis and the control for the M2DC converter implemented in the MMC mock-up. The methodology used is efficient to find problems hidden by non-real-time simulation.

The converter design proceeded in this chapter is particularly proposed for M2DC transformed from an existing MMC, which is different from the design of the third chapter.

From the simulation results comparisons, average model and theory analysis are validated in the steady state. It is observed that M2DC converter needs less AC power at  $\alpha > 0.5$  to transmit the same power as  $\alpha = 0.5$ . Therefore, the converter is more convenient to be operated for  $\alpha > 0.5$  to reduce AC power and losses. However, the asymmetrical structure of the converter at  $\alpha > 0.5$  needs sizing individually upper and lower arms. For a M2DC converter designed based on MMC converter, upper arm and lower arm have the same components, which is disadvantageous for an M2DC operation. Same capacitance

value increases under size risks in terms of capacitor voltage ripples. Arm voltage could be deformed due to great capacitor voltage ripples, as shown in case 2 and case 4. To reduce the under size risks, operation frequency is mandatory increased to reduce capacitance value. The risks of increase of AC frequency is an increase of the switching frequency, which involves more switching losses. It is a disadvantage for high power applications. Therefore, there is a compromise between capacitance sizing and frequency selection.

Moreover, with increased frequency and reasonable capacitor voltage ripples (case 2 and case 4), DC output currents contain the third harmonic in real-time simulation and HIL simulation due to instantaneous model caused slight different energy in upper and lower arms. This harmonic can be reduced by a decrease of response time in current loops. But this solution is more demanding in DSP calculation speed. With same DSP control card, it is proposed to reduce the number of submodules in arms, to improve the low-level control to isolate unusable submodules, and to size capacitance value with same voltage ripples in upper and lower arms.

Therefore, for an M2DC designed based on MMC, it is more convenient to operate at  $\alpha = 0.5$  to keep MMC symmetrical structure, which is confirmed by case 1 and case 3.

Using the same converter design, low level and high-level control, case 3 confirms also the operationally of M2DC in reduced DC voltages. It should be noted that power should be reduced in this case to avoid overcurrent in the converter.

Four cases in the steady state show a greater switching frequency in HIL simulation. To reduce the switching frequency, low-level control could be improved to avoid unusable movement. Also, low-level control can add a new function to isolate the unusable submodules mentioned previously.

Finally, in the dynamic state, the bidirectional power of the converter is confirmed. Zero power issue shown in the third “control” chapter re-appears in the real-time simulation and HIL simulation. It is proposed to review the design condition of  $\hat{V}_{mu,ac} = \hat{V}_{ml,ac}$  and  $\theta = 90^\circ$  to eliminate the problem due to the extreme low AC voltages and number of submodules at the extreme low power. If the problem comes from neglected losses, it is proposed to review the energy model taking into account losses.

This chapter improves assurance of M2DC experimental test using MMC mock-up of the laboratory in the steady state. Since the components and low-level control of the mock-up must be kept, case 1 is the best configuration to test and verify the instantaneous model to complete the comparisons of “average model”, “instantaneous model” and “physical converter”.

Without oversized submodules, converter design and high-level control can be also experimentally tested. But the future experimental test should avoid zero power before finding a reliable solution for this particular power reference.

## IV.9 References

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## V General conclusion and perspectives

Direct Current (DC) transmission is a reliable and low-cost way to deliver high voltage and great power, regarding traditional Alternative Current (AC) transmission where reactors are mandatory. Actually, most DC links have two converter stations, that power transmit between two stations called Point to Point DC links. To exchange power amid three or more stations, Multi-Terminal DC (MTDC) grid concept has been proposed. The first MTDC grids are “SACO” grid, “Nelson River” grid and “Hydro Quebec – New England” grid and based on thyristor converter technology. More recently, Nanao Multi-terminal VSC HVDC and Zhoushan Multi-terminal DC Interconnection are the first MTDC grids based on VSC technology.

A parallel connection of each DC link has been done as the DC voltage is the same. The objective of these MTDC grids is to have a better control over their power flow. However, more and more DC links have appeared without necessarily the same DC voltage. Its value is not already normalized and depends on the electric manufacturer. Converter technology could also be different (transistor or thyristor technology). These differences between DC links create a conflict to connect them directly. Therefore, future MTDC grid should have an intermediate “HVDC component” to connect different DC links, which is the DC/DC HVDC converter.

Based on the analysis of the test case provided by CIGRE Group B4.76, the DC/DC converter is required to have a voltage capability of more than 100kV and a power capability of more than 100MW. With this specification, a review of all potential DC/DC converters has been realized in Chapter 1. The review is classified by low or high modularity of topologies. In low modularity topologies, Buck has been presented at first. Due to transistor technology, a single Buck (or boost) is not enough to support such high voltage and great power. Therefore, the interleaved technique and series connection of transistors technique are reviewed to increase current range and voltage range of a classical Buck. But the series connection of transistors is difficult to be industrially realized due to its high demanding of control. Therefore, topologies of Double buck / Neutral Point Clamped / Flying Capacitors DC converter are reviewed. They are more advantageous in voltage range than Buck. But their complicated electrical circuit schema makes the topologies low modularity and difficult to be extended to high voltage. Moreover, their capacitors position could be a danger due to concentrated bulk energy stored in the converters. Therefore, it can be concluded that low modularity topologies are not convenient in high voltage and great power applications. Following the low modularity topologies, the chapter reviews topologies with high modularity, which are the series connection of Dual Active Bridge and Modular Multilevel DC converter topologies. The topology “series connection of Dual Active Bridge” is able to increase easily in voltage range thanks to its module Dual Active Bridge converter. But each module has a mandatory transformer to isolate current. The increase of voltage range is an increase in transformer number, which increases also the volume of the converter. Therefore, the end of the chapter thinks about using Modular Multilevel Converter (MMC) topology, which is

a DC/AC converter already used and developed in DC grids. Inspiring its topology, four modular multilevel DC converters have been reviewed by the classification of two stages conversion: Dual Active Bridge version and single stage conversion: Autotransformer, Hybrid Cascaded DC/DC converter and DC-DC Modular Multilevel Converter (M2DC). Amid these topologies, the M2DC has been considered more advantageous in volume and costs, since it requires less active components and passive components. Therefore, M2DC is the topology selected and analyzed in the work.

In Chapter 2, analyses of the M2DC were started with the average model of an arm where voltage, current and energy relations have been shown. With the relations of an arm, analysis is extended to a leg which contains one upper arm and one lower arm. In the analysis, it has been explained the reason for using AC components in the DC/DC converter and the method of eliminating AC signals in DC sides. Since AC signals should be eliminated in DC sides, amplitude, frequency and phases of AC signals become degrees of freedom in the converter operation. These degrees of freedom have been analyzed by their limitations. Based on the limitations, the converter performance has been shown more clearly. The end of the chapter has proposed a design method for arm inductance and submodule capacitance.

These analyses have been validated in Chapter 3 by simulating the converter model and the specific control proposed for the converter in Chapter 2. An energy based control to maintain the capacitor voltage of each submodule is also applied. Simulations in Matlab have also validated the converter high voltage and great power range since voltage level and power of simulations have been based on the CIGRE test case.

With the validation of the theoretical analyses and control in high voltage range, Chapter 4 asked for the confirmation of theoretical analyses and control in Real Time simulation and in Hardware-In-the-Loop (HIL) simulation. Since the objective of the simulations is to validate the converter analyses in practical experimentation, our cheapest way to build the M2DC is using the existing laboratory MMC converter (a down-scaled mock-up). Therefore, firstly an M2DC design method based on existing down scaled MMC has been proposed. To test the whole control, the chapter has developed a methodology of implementation of the control algorithm in HIL simulation. The end of the chapter has validated the converter model, design and control by a similarity of three types of simulations, in which HIL simulation gives more precise results.

During the analysis of the topology, the topic has been focused on the global operation principle. It can be concluded that M2DC has better performance for small tap voltage ( $\alpha > 0.5$ ), thanks to its lower internal AC currents and AC power.

Reminding state of the arts, there are also other potential topologies for high voltage and great power applications, such as Modular Multilevel DC converters (Dual Active Bridge version with or without transformer). These topologies are not studied in this work. Therefore, a deep comparison amid those potential topologies, including M2DC, are expected, at the first, in the future regarding the requirement of the CIGRE test case.

Focusing on the M2DC topology, to complete the validation of the converter model and control in future work, the planned experimental test is necessary to be realized with the downscaled M2DC mock-up and DSP control.

On the other hand, to improve the converter performance, some potential possibilities could be attempted regarding the design and control.

Converter design could be improved by propositions as follow:

- **Study of coupling inductors:** Each coupled inductors in the original proposition is treated as two individual inductors to reduce the complexity due to mutual inductors in this work. But the coupling is convenient to reduce inductor footprint. It is also interesting to investigate the AC components of the converter considering mutual inductors, which might be helpful to reduce AC current.
- **Study of full bridge submodule or hybrid arms:** Since M2DC converter is a direct conversion converter without transformer, it is vulnerable to DC side default. Full bridge or hybrid submodule is generally considered efficient to block DC default. Even though researches on DC breakers have quickly progressed, it is better to have self-protection in case of DC fault for M2DC converter.
- **Study of different numbers of submodules in upper and lower arms:** The M2DC converter can be theoretically operated with different numbers of submodules in upper and lower arms. Moreover, AC components are independent of the submodules number. Therefore, for the asymmetrical structure of M2DC converter applications, the use of a suitable number of submodules is helpful to minimize the design and reduce harmonics in the output DC currents.

Improvement of high-level control of the converter could be:

- **Review of the control condition ( $\hat{V}_{mu,ac} = \hat{V}_{ml,ac}$  and  $\theta = 90^\circ$ ):** This proposition is necessary in case of zero power issue. Its objective is to maintain amplitudes of AC voltages up to a certain minimum value during power decrease.
- **Individual control for each component current:** To improve control precision, it is better to control separately DC component current and AC component current or use more complex controllers (PID, resonant controllers). It is also convenient to the converter analysis since all angles defined in the work will be ensured without delay.

Also, low-level control of the converter could be improved by:

- **Disable unusable submodules:** During HIL simulation, it has been noted that the asymmetrical structure of M2DC converter is less convenient than symmetrical structure if it is designed from MMC converter. To switch easily between MMC and M2DC, it is better to be able to isolate unusable submodules.
- **Full bridge submodule or hybrid arms control:** It is necessary to adapt the low-level control to use full bridge submodules or hybrid arms, which is needed for DC fault protection.



The last part of the perspectives is for grids application:

- **Analysis of the M2DC in MTDC:** It is mandatory to analyze the converter dynamic in an MTDC grid depending on its design and control.
- **Integration of the M2DC in a small scaled MTDC grid:** It is finally mandatory to validate the theoretical analysis in practice. Therefore, the integration of the M2DC in a small scaled MTDC grid is a necessary stage of validations.
- **Adjustable frequency:** It is also possible to use MMC or M2DC with adjustable frequency. Adjustable frequency can be used in MMC (DC/AC converter) for high voltage and great power drive application. For the M2DC, the frequency of AC voltages could be helpful for the converter control and its performances, for example, DC power or voltage. Varying internal AC frequency could allow the M2DC adapting quickly new specification and maximize the efficiency.



## **Etude d'un convertisseur DC-DC pour les réseaux haute tension à courant continu (HVDC) : modélisation et contrôle du convertisseur DC-DC modulaire multiniveaux (M2DC)**

Les travaux présentés dans ce mémoire portent sur les convertisseurs continu-continu (DC/DC) pour les réseaux de transport à Courant Continu (HVDC) dans un contexte de réseau maillé de type Multi Terminaux DC (MTDC). Dans ce genre de réseau, les convertisseurs DC/DC sont nécessaires pour interconnecter ces réseaux. L'objectif de ce travail est donc d'étudier un convertisseur DC/DC pour des applications à haute tension et forte puissance. De nombreux convertisseurs DC/DC classiques existent, mais ne sont pas adaptés à ces niveaux de tension et puissance. Le volume et coût sont les points clés de l'étude pour l'industrialisation des structures dédiées aux réseaux HVDC. Parmi les structures identifiées, le convertisseur Modulaire Multiniveaux DC-DC (M2DC), récent et compact, a été finalement choisi.

Le travail proposé développe l'étude du M2DC en régime établi et une modélisation en modèle moyen de ce convertisseur. Ensuite, des lois de contrôle sont proposées pour valider les analyses précédentes sur la base du principe de l'inversion du modèle. Le travail vise enfin à valider les analyses et le contrôle à l'aide de la maquette du Convertisseur Modulaire Multiniveaux (MMC) du L2EP. Pour cela, un dimensionnement du M2DC basé sur le MMC existant est proposé. Enfin, des simulations HIL (Hardware-In-the-Loop) valident les analyses et montrent la faisabilité du prototypage du M2DC.

### **Mots-clés**

MTDC, DC/DC, M2DC, modélisation, analyse en régime établi, contrôle, Simulation en Temps Réel, Hardware-In-the-Loop (HIL)

## **A DC-DC power converter study for High Voltage Direct Current (HVDC) grid: Model and control of the DC-DC Modular Multilevel Converter (M2DC)**

This work is based on Multi Terminal Direct Current (MTDC) grids. In the MTDC grid, DC/DC converter stations are needed to connect different HVDC grids. A lot of DC/DC converters have been studied and developed, but are not suitable for high voltage and great power constraints. Therefore, the objective of this work is the study of a DC/DC converter for high voltage and great power applications. For the potentially HVDC applications, the volume and costs are major criteria. According to this, a high voltage and great power potential DC/DC converter is selected, which is the Modular Multilevel DC-DC Converter (M2DC).

Focusing on the M2DC, the work proposes analyses in steady state and builds an average model for the converter. Based on the average model, the basic control algorithm for the converter is developed to validate the previous analysis. Since the thesis aims to use the existing L2EP Modular Multilevel Converter (MMC) to test the M2DC model and control, a design of the M2DC based on MMC is proposed. Finally, the M2DC HIL (Hardware In-the-Loop) simulations results are presented confirming previous analyses and allowing to go on to prototyping the M2DC on the base of the existing MMC.

### **Keywords**

MTDC, DC/DC, M2DC, modelling, steady-state analysis, control, Real-Time Simulation, Hardware-In-the-Loop (HIL)