Design of ULP circuits for Harvesting applications

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POUR OBTENIR LE GRADE DE

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SPI

Electronique

Par Verrascina Nicola

Design of ULP circuits for harvesting applications

Sous la direction de : Jean-Baptiste Begueret
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Soutenue le 05/07/2019

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Titre : Conception des circuits à très faible consommation pour des applications Harvesting

Résumé : La très faible consommation dans les appareilles modernes est le facteur-clé pour les capteurs alimentée par une source d’énergie récupérée. La réduction du budget de puissance peut être atteinte grâce à différents techniques lié à trois niveaux d’abstraction : transistor, circuit et système. L’objet de cette thèse est l’analyse et la conception des circuits à très faible consommation pour des réseaux des capteurs sans fils. A’ régulateur de tension et an émetteur RF ont été examiné. Le premier est le circuit principal pour la gestion de puissance ; il agit comme interface entre le transducteur et les autres circuits du capteur. L’metteur est le circuit que exiges le plus de puissance pour fonctionner, donc une réduction de sa puissance il permet une augmentation de la vie opérationnelle du capteur.

Mots clés : WSN, régulateur de tension, émetteur courte portée

Title: Design of Ultra Low-Power Circuits for Harvesting Applications

Abstract: In the modern devices Ultra-low power consumption is the survival key for the energy-harvested sensor node. The reduction of the power budget can be achieved by mixing different low–power techniques at three levels of abstraction: transistor level, circuit level and system level. This thesis deals with the analysis and the design of Ultra-Low Power (ULP) circuits suitable for Energy-Harvesting Wireless Sensor Networks (EHWSN). In particular, voltage regulator and RF transmission circuits are examined. The former is the main block in power management unit; it interfaces the transducer circuit with the rest of the sensor node. The latter is the most energy hungry block and thus decreasing its power consumption can drastically increases the sensor on-time.

Keywords: WSN, LDO, Short-range transmitter, Data-rate

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"To those who fight for the freedom"

Abstract

The increasing diffusion of Wireless Sensor Node (WSNs) and Body-Area sensor Network (BAN) is mainly due to the demand of smart environment in order to increase the quality of life. Several are the application domains:from domotic to industry, from medicine to rural applications. Normally a sensor network counts huge number of sensors that may be placed in hostile environment. Many time the batteries replacement is hard and expensive.Therefore the need to find another type of energy source, replacing the batteries, has created an increasing interest in the scientific academy.

The development of new material and the technological progress have supported the possibility to extract the energy from non-conventional sources for small scale applications. However the amount of energy density is not high as it spans from the highest value of 500 μW/cm^2 for solar source to the lowest one of 1 μ W/ cm^2 for radio-frequency source. The energy constraint poses a several challenge for the designers to extend the lifetime devices. Ultra-low power consumption is the survival key for the energy-harvested sensor node. The reduction of the power budget can be achieved by mixing different low -power techniques at three levels of abstraction: transistor level, circuit level and system level.

This thesis deals with the analysis and the design of Ultra-Low Power (ULP) circuits suitable for Energy-Harvesting Wireless Sensor Networks (EHWSN). In particular, voltage regulator and RF transmission circuits are examined. The former is the main block in power management unit; it interfaces the transducer circuit with the rest of the sensor node. The latter is the most energy hungry block and thus decreasing its power consumption can drastically increases the sensor on-time.

The thesis is structured as follows:

Chapter 1 describes the harvesting sources available in the environment, highlighting for each of them the main advantages and drawbacks when they are applied in small scale devices. The second part of this chapter is dedicated to the low-power techniques. Three levels of abstraction are introduced (CMOS technology, Circuit and System) with their advantages and drawbacks.

Chapter 2 is dedicated to the study of wireless sensor networks. A general framework is given on the sensor architecture with highlights on the fundamental blocks. The expression for the required radiated power is obtained for a given distance. The duty-cycled equation is also obtained to get the best trade-off in terms of required energy, communication channel quality and amount of data transfer.

Chapter 3 focuses on the design of very efficient Low-DropOut voltage (LDO) regulator. Many are the efforts to achieve a good regulation accuracy by addressing ultra low power consumption. Especially for transient response the closed loop frequency response and the slew-rate of the error amplifier requires high quiescent current to achieve good performances. In this work an adaptively bias current and a class-AB error amplifier are implemented in such way the increase in quiescent current is proportional to the very large load current. With these techniques the impact on the global power consumption of LDO is reduced. Moreover high current efficiency for all load conditions is also achieved. The stability of closed loop is ensured by a current buffer and a Miller's capacitor for the whole range of operational load current. The stability is guaranteed also for very low stand-by current.

In chapter 4 the design flow of OOK modulation transmitter is addressed. The low targeted radiated power of -15 dBm poses a severe limitation for the global transmitter efficiency. The first part of the chapter is dedicated to the study of classical cascaded architectures where the oscillator (VCO) is directly connected to the input of the power driver. The trade-off between the supply voltage and the matching network is described highlighting the difficulty to integrate the passive elements of matching network when the supply voltage for the power amplifier is about 1 V and the peak to peak output voltage required over a 50 Ω is in the order of tens millivolts. To circumnavigate this problem a current reuse transmitter is proposed where the power driver and the VCO are stacked and the same bias current is used. With this architecture the supply voltage can be tuned between the two circuits to achieve the best trade-off between the power consumption and the performances of each circuit.

Résumé

La demande toujours croissante d'amélioration de la qualité de vie avec la création des environnements intelligents, a permis la diffusion des reseaux des capteurs sans fil. Les applications envisagées peuvent aller de la domotique à l'industrie, de la medicine à l'agriculture. Le probléme principal pour ces types des capteurs est le remplacement des batteries, étant donné que l'installation pourrait avoir lieu dans des environnement hostiles. Donc la recherche d' autres types des sources d'énergie qui peuvent remplacer les batteries a attiré l'attention de la Communauté scientifique internationale.

Nombreux sont les sources à partir des quelles il est possible obtenir de l'énergie électrique pour des systèmes miniaturisés. Néanmoins la faible énergie mise à disposition par des sources non-conventionnelles, pose un vrai défi pour les concepteurs s'ils veulent augmenter la durée de vie des systèmes. C'est seulement par l'utilisation des circuits à trés faible consommation que les capteures autonomes peuvent représenter un choix valable pour le marché. La réduction du besoin d'énergie peut être atteinte en mélegeant différentes tecniques à trois différent niveaux d'abstraction : transistor, circuit et système.

L'objectif de la thése est la conception et l'analyse des circuits à trés faible consommation appropriés pour des applications d' Energy-Harvesting Wireless Sensor Networks (EHWSN). La première partie détaille le régulateur de tension, qui est le circuit fondamental du bloc dédiée à la gestion de la puissance. La deuxième partie est dédié à l'analyse et à la conception d'un emetteur RF, qui représente le circuit avec la consommation de puissance la plus haute présent dans le capteur. Par conséquent une reduction de la consommation de ce dernier circuit, baisse considérablement la démande d'énergie du systeme dans sa totalité.

La thése est ainsi organisée : Le chapitre 1 décrit les sources de récupération d'énergie disponibles dans l'environnement, soulignant les avantages et les inconvénients quand elle sont appliquées à des circuits miniaturisés. La deuxième partie est dédiée à l'étude des techniques permettant la réduction de la consommation de puissance.

Le chapitre 2 est dédié à l'étude des réseaux de capteurs sans fil. Un cadre genéral de leur architecure est donné. L'équation pour calculer la puissance radiative nécessaire pour couvrir une certaine distance est donnée. En dernier lieu le rapport cyclic optimale est derivée à partir de l'énergie nécessaire, de la qualité du canal de communication et de la quantité des données à transmettre.

Le chapitre 3 décrit la conception d'un régulateur Low-DropOut (LDO) à haute efficacité. L'attention est centrée pour obtenir une trés faible consommation de puissance sans sous-estimer la précision du réglage de tension. Pour obtenir un bonne réglage de tension, l'amplificateur d'erreurs doit avoir un slew-rate élevé, et la réponse en fréquence de la boucle, donc la vitesse de réglage du circuit, doit etre rapide. Les solutions adoptées pour surmonter le probléme sont un amplificateur d'erreur de classe-AB, avec un courant de polarisation qui s'adapte au courant de sortie du régulateur. L'efficacité est élevée pour toutes les conditions du courant de sortie avec moins d'impact sur la consommation de puissance globale du circuit. La stabilité de la boucle est assurée dans toutes les conditions par un buffer de courant et une capacité Miller, meme pour un courant trés faible de stand-by en sortie. Le chapitre 4 décrit la conception d'un émetteur avec une modulation OOK. La faible puissance émise de -15 dBm limite l'efficacité globale du systém.

La premiére partie du chapitre est dédiée à l'étude d une structure classique en cascade, où la sortie du synthétiseur de fréquence (VCO) est directement connectée à l'entrée de l'amplificateur de puissance. Le chapitre continue présentant les compromis de conception pour le réseau d'adaptation quand la tension d'alimentation est élevée alors que la tension aux bor de la charge de 50 Ω est de quelques mV. Une architecture empilée est finalement proposée, où le VCO et le driver de puissance partagent le meme courant de polarisation, afin de répartir la tension d'alimentation entre les deux circuits.

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Chapter 1

Low Power techniques for energy harvesting system

1.1 Energy Harvesting

The concept of making electronic devices electrically independent of expensive, not always available, and exhaustible sources is not new and it has wider applications that are very common. Nowadays it is easy to find large surface solar panels or wind turbines especially in rural environment. In nature many are the sources from which it is possible to obtain electrical energy and several are the environments where harvesting process can find use whether internal or external.

Solar energy, thermal energy, vibrational energy and radio-frequency (RF) energy are the main sources exploited to replace the batteries in micro-scale or nano-scale electronic devices. Excluding solar and thermal energy, kinetic and RF source are not suitable for large-scale applications due to their low energy density.

In the next section these energy sources will be briefly introduced by describing the advantages and the drawbacks.

1.1.1 Solar Energy

The solar harvesting is based on the Photo-Voltaic (PV) effect where photon energy is used to excite an electron from its ground state to an excited state. Most of solar panels are made of by a semiconductor material; when the photon strikes the photo-cell an electron-hole pair is formed, therefore the semiconductor conductivity increases. To avoid the recombination of the two particles a PN junction is needed (N-type and P-type semiconductor overlapping). Basically a solar cell is an unbiased diode that is exposed to the light. If the N and P regions are connected by a load (see Fig. 1.1), power can be extracted from the device. To extract the maximum power from the PV cell the system has to be able to change the PV cell load, because an optimum value is needed for different illumination conditions. A DC-DC converter should be placed between the PV array and the load (see fig. 1.2) for the Maximum Power Point Tracking (MPPT).

One of the main problem with this type of source is the power density variability due to the incident solar luminosity. In outdoor condition high power density is achieved with 100 mW/cm^2 while in indoor environment the irradiated power decreases drastically to 0.5 mW/cm^2 [TTKS14] [WTY11]. Currently, the main efforts in PV harvesting sensor node

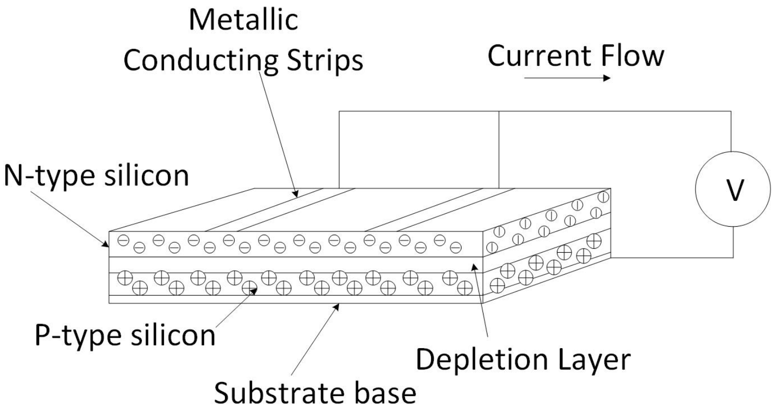


Figure 1.1 – Section of Photovoltaic Cell

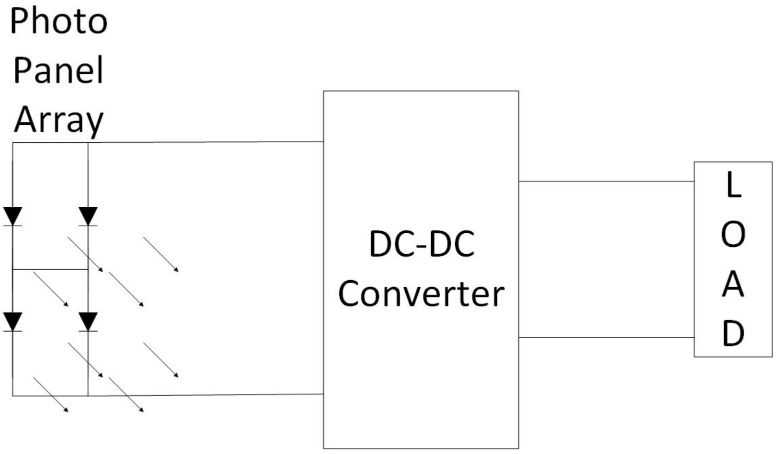


Figure 1.2 – Typical implementation of PV harvesting maximum power point tracking.

are devoted to the system design and the circuit implementation to extract the maximum power from panels which become smaller and smaller [WTY11] [LSS15]and suitable for highly integrated devices.

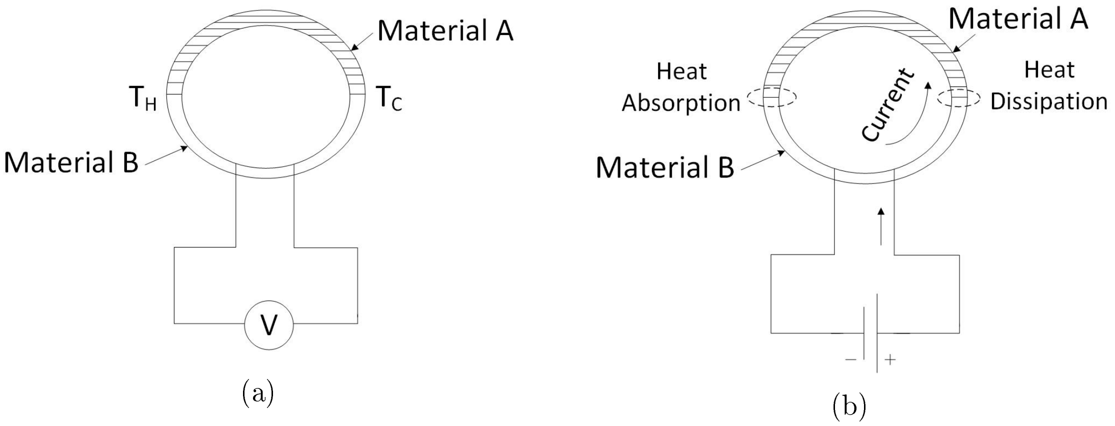


Figure 1.3 – (a) Seedback effect, the generated voltage is proportional to the temperature gradient between the hot point T_H and the cold point T_C (b) Peltier effect the current generated by the applied voltage causes a thermal diffusion from the heat dissipation to the heat absorption.

1.1.2 Thermal Energy

Thermo-electrical basics are used in modern devices to generate electrical or thermal energy depending if Seedback or Peltier effect are exploited as depicted in fig. 1.3.
The Seedback effect describes a phenomena that produces a voltage from a temperature gradient. Applying a temperature difference $\Delta\mathrm{T} = T_C - T_H$ across two metal or semiconductor junctions a voltage V is generated into the circuit

$$V = \alpha_{SB}\Delta T \tag{1.1}$$

where α_{SB} is the Seedback coefficient associated to the material properties.
The Peltier effect produces the opposite phenomenon. The current generated by a voltage applied across two metal junctions causes the electron movement from one side to the other side. Consequently a heat absorption occurs at one junction and a heat dissipation at the other one. The amount of heat removed per time unit from one junction to the another one is given by

$$Q = I\pi_{Pel} \tag{1.2}$$

where I is the circuit current, π_{Pel} is the Peltier coefficient that has to be measured in isothermal condition for the two metals.
It is clear that the material composition, the surface and geometry of contact between the two elements are the main parameters to achieve high conversion efficiency. In [RM17] a thermoelectric energy harvester demonstrates to be able to generate 0.78 mW/ cm^2 with 3.5 K of gradient temperature. With such of power it is possible to accomplish sensing task in 32x32 mm for body area network with comfort wearability. One of main drawbacks of thermal source is its power density variability due to a not constant temperature gradient. Moreover the small output voltage ($\approx$ 40 mV) requires step-up circuit to get a usable voltage.

1.1.3 Kinetic Energy

Kinetic harvesting sensor exploits the energy generated from movement, displacement or mechanical strain to produce electrical energy through electromagnetic, piezoelectric or electrostatic mechanisms.

- **Piezoelectric mechanism**
  Piezoelectric materials exhibit the capacity to generate electrical energy when subjected to a mechanical strain. The dipoles present inside a piezoelectric material becomes polarized when an external force is applied, and the polarization degree is proportional to the strain.
- **Electromagnetic mechanism**
  The conductor movement or the coil rotary in electromagnetic field is used to generate a potential difference which follow the Faraday's law. When an electric conductor is moved through a magnetic field, an electromotive force is induced between the ends of the conductor. This voltage is proportional to the electromagnetic field variations in the time.
- **Electrostatic mechanism**
  A variable capacitor is used to generate an electrical energy when a external vibration is applied. For a charge-constrained device, the plates movement causes an increasing or decreasing voltage across the capacitor, since the charge has to remain the same.

In [MPW$^+$17] the breath movement is used to monitor the patient respiration. The front-end transducer is a piezoelectric material-based sensor. The harvested source is able to sustain a power consumption about 800 μW when the impulse radio ultra-wideband transmitter is active.

1.1.4 Radio-Frequency Energy

Probably nowadays the Radio-Frequency (RF) energy is the most easily available source: the mobile phone, Wi-Fi and Bluetooth connections. The RF harvesting devices are equipped with a antenna, picking-up the RF wave. The corresponding AC voltage is then transformed in a more suitable DC voltage for the electronic blocks by a rectifier circuit.

The conversion efficiency and the voltage available at rectifier output depend mainly on the channel communication qualities, on the antenna performances and on the rectifier losses. As the energy available is small a storage element is mandatory to achieve sensing and transmission operations. The device dimensions are mainly tied to the antenna design, and the conversion efficiency relates on the antenna gain and on power level of the incoming signal. The average energy density of RF source is about 1 μ W/cm^2, but the RF-DC conversion circuit is able to generate voltage in the order of fews volts (1.4 V - 3 V) with an output power of hundreds of micro-watts.

The low energy available from the environment sources (Tab. 1.1) poses an hard challenge for the designers, to guarantee the required performances. Designing nano-watt or micro-watt circuits surely can ensure long lifetime devices but at cost of poor performances.

However there are several approaches to reduce the power consumption in radio and system circuits, which extend at different design level. In the next section the main techniques to design ultra-low power (ULP) system are introduced.

Table 1.1 – Comparative energy sources

	Energy Density	Advantages	Drawbacks
Solar Energy	500 μW/ cm^2	- High energy density -Well developed technology.	-Large occupied area -Indoor degradation
Thermal Energy	60 μW/ cm^2	- Always Available	-Difficult to control - Low output voltage
Kinetic Energy	200 μW/ cm^3	-Several applications -Light weight	-Low conversion efficiency.
RF Energy	1 μW/ cm^3	-Available everywhere -Small surface	-Low energy density -Distance dependent

1.2 Design techniques for ULP circuits

The technology progress in CMOS fabrication has allowed the designers to develop several techniques in order to reduce power consumption in modern devices; not only at the transistor level but there are three different abstraction levels to address, in order to achieve low power consumption for the sensor node:

— CMOS level: Scaling down, thick metal layer, ultra-low leakage MOSFET
— Circuit level: weak inversion, current reuse, multi-threshold CMOS (MTCMOS)
— System approach: wake-up protocol.

1.2.1 CMOS level

It is well-known that the transistor size scaling is described by the Moore's law: the number of transistors into an integrated-circuit chip is doubling approximately every two years without correspondingly increasing the chip costs. The reduced channel length ($L_{channel}$) in metal-oxide-semiconductor FET increases the cut-off frequency as the parasitic capacitances decrease proportionally to the $L_{channel}$

$$C_{gate} = \frac{\epsilon_{ox}\epsilon_o}{t_{ox}} L_{channel} \tag{1.3}$$

where C_{gate} is the MOSFET gate capacitance, ϵ_{ox} is the dielectric constant of silicon oxide, ϵ_o is the permitivity of free space and t_{ox} is the oxide thickness. Considering C_{gate} as the most important parasitic capacitance inside the MOSFET the cut-off frequency f_t can be written as:

$$f_t = \frac{g_m}{2\pi C_{gate}} \tag{1.4}$$

where g_m is the MOSFET transconductance. The f_t is the frequency at which the short circuit small-signal current gain is unitary; fig. 1.4 plots f_t versus the normalized drain

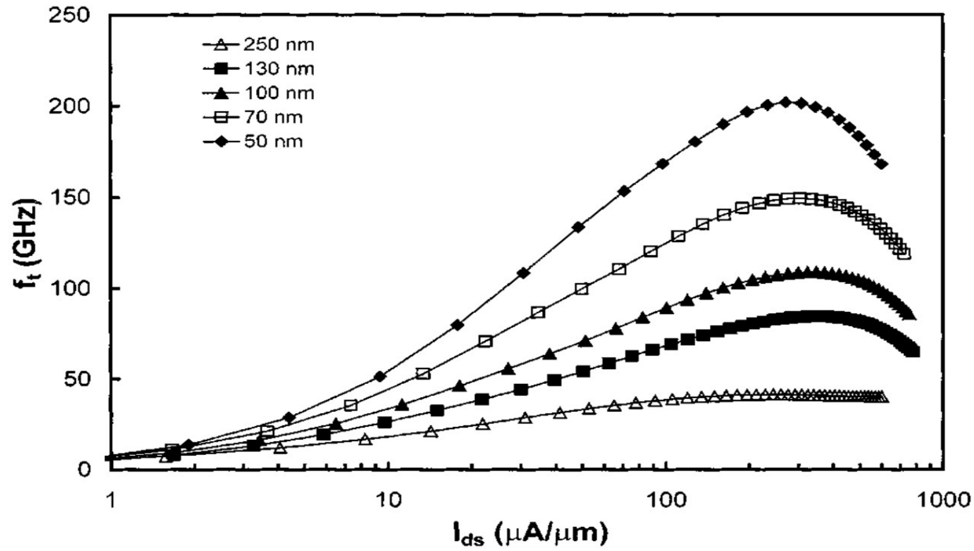


Figure 1.4 – Cut-off Frequency trend in function of current density for different node technology [WKvL+01]

source current density for five technology nodes. RF circuits (Power amplifier, Oscillator, Mixer,etc) take advantages from the MOSFET scaling because the transistor exhibits higher current gain for the same operation frequency. Therefore same performances can be achieved with less current and lower power consumption consequently.

Also the threshold voltage decreases with the size downscaling, because the reduction in oxide thickness allows lower differential potential needed to the MOSFET gate, in order to create the conduction channel. As consequence, it is possible to decreases the supply voltage needed to put the transistors in saturated region. The main benefit when the circuit operates at lower power supply voltage is the reduction in active power dissipation P_{act} for switched topology circuits. P_{act} is proportional to the square of supply voltage V_{DD}, to the capacitors involved in charge and discharge operations and to the switching frequency f_{switch}:

$$P_{act} = C_{switch} V_{DD}^2 f_{switch} \tag{1.5}$$

It seems clear from eq. 1.5, that with the possibility to operate at lower V_{DD} the power consumption decreases. However as the distance between drain-source is reduced and the oxide is thinner, the probability that an electron moves in transistor off-state is higher and thus the leakage current increases degrading the power consumption performance in sleep mode; especially in ultra low duty-cycled system, where the circuit is off most of the time, the leakage current impacts the power budget; ultra-low leakage MOSFET can help with reducing the off-state current.

Moreover the higher chip cost in deeply scaling technology has to be considered especially when low cost system is targeted.

Thick metal layer

Generally speaking the reduction of parasitic resistance allows to reduce the static power dissipation. This is the case for the drain source MOSFET resistance R_{DS} in switching circuit and also for the inductor and capacitor parasitic resistance. In energetic circuit

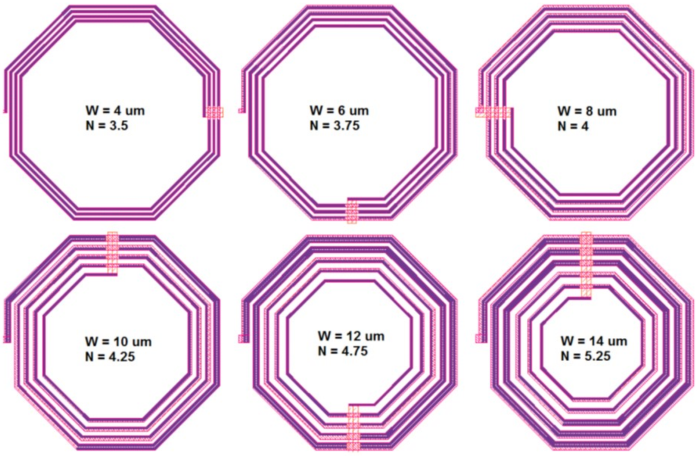


Figure 1.5 – Combinations to achieve 8 nH inductance [Van15] where W is the metal width and N is the numbers of turns.

(LC oscillator, tuned amplifier, buck/bust voltage converter) the impact of lossy elements can be traduced through the quality factor Q [Raz]

$$Q = 2\pi \frac{EnergyStored}{EnergydissipatedperCycle} \tag{1.6}$$

High quality factor is preferable because the energy dissipated in lossy elements is low. A reduction in power consumption can be achieved by using high-Q elements and LC oscillator is a perfect example. In LC oscillator the oscillation is assured if the losses (the parasitic series resistances R_s of Inductor and Capacitor) are counterbalanced by an active element as the MOSFET transconductance g_m.

$$g_m \geq \frac{1}{R_s} \tag{1.7}$$

In first approximation the g_m is proportional to the drain-source current. Therefore for small value of parasitic resistance (high-Q) the g_m needed is lower and the drain-source current decreases proportionally. At low to medium frequency oscillation (from 400 MHz to 15 GHz) a customized inductor can helps in power consumption reduction with higher Q. In [Van15] thick metal and dense tapered spiral inductor shows quality factor improvements for 10 GHz frequency oscillation. Fig. 1.5 depicts different geometries to get 8 nH inductance with the highest Q at the same generated frequency.

1.2.2 Circuit Level

MOSFET operating region

Traditionally, the MOSFET is mostly used in strong inversion (SI) region with a drain-source current in the milli-Ampere range where the gate-source voltage V_{gs} has to be greater than the threshold voltage V_{th}

$$V_{gs} >> V_{th} \tag{1.8}$$

In SI, for N-type Mosfet, I_{DS} is proportional to the square of the effective gate-source voltage

$$I_{DS} = \frac{1}{2}\frac{\mu_n C_{ox}}{n}\frac{W}{L}(V_{gs} - V_{th})^2 \tag{1.9}$$

Where μ is the carrier velocity, C_{ox} is the oxide capacitance, n is a slope factor, W and L are the width and the length of conduction channel. Only from the second half of 90s [EV96], with the diffusion of portable devices the weak inversion (WI) has been taken in consideration to address low power consumption in integrated circuit. In fact when V_{gs} is lower than V_{th}

$$V_{gs} << V_{th} \tag{1.10}$$

the transistor operates in WI with an I_{DS} in the range of micro-Ampere to the nano-Ampere. In this case the current is not more governed by a square law, but it follows an exponential behavior

$$I_{DS} = 2n\mu C_{ox}V_t^2\left(\frac{W}{L}\right)\exp\left(\frac{V_{gs} - V_{th}}{nV_t}\right) \tag{1.11}$$

where V_t is the thermal voltage. However the passage from SI to WI is not abrupt and the two regions are separated by the moderate inversion (MI), where V_{gs} differs above or below V_{TH} to a few tens of mV. Therefore the three regions represent three different degrees of MOS channel inversion. To give a coherent circuit design with the three level of channel inversion the Inversion Coefficient (IC) has been introduced, which allows a continuous design flow from the WI to the SI. The IC [Bin07] can be found by the drain-source current, divided by the product of the shape factor S $= \frac{W}{L}$ and the technology current $I_o = 2n\mu C_{ox}V_t^2$

$$IC = \frac{I_{DS}}{I_o S} \tag{1.12}$$

The IC ranges from 0.01 in WI to 100 in SI and the center value is 1 at the middle of MI. Therefore every value of IC corresponds to a precise level of inversion with a well defined bias point. The transistor width is calculated from the choice of the channel length L, the drain-source current and the inversion coefficient. Depending on the circuit performances, every operating region can accomplish a specific trade-off as shown in fig. 1.6. Many works [EC15] [TSM15] [SH06] demonstrate that designing analog or radio-frequency circuits in MI ensures the best trade-off between power consumption, $\frac{g_m}{I_{ds}}$ efficiency, low voltage design and AC response.

Fig. 1.7 shows a cascoded single stage Operational Transconductance Amplifier OTA where the transistors operate in saturation region. When the MOSFET are biased at the low side of SI (IC = 10) a $V_{ds,sat} = 0.24$ V for each transistor can be assumed, while when the low side of MI (IC = 0.1) is considered the $V_{ds,sat} = 0.12$ V. The only parameter analyzed is the minimum supply voltage needed to bias each transistor in saturation, and the reduction of $V_{DD,min}$ is quite evident. The main drawback when MOSFET operates in WI is the poor frequency response due to a large parasitic capacitance forced by the large MOSFET size. Moreover WI introduces a pronounce dependence en process and temperature variations.

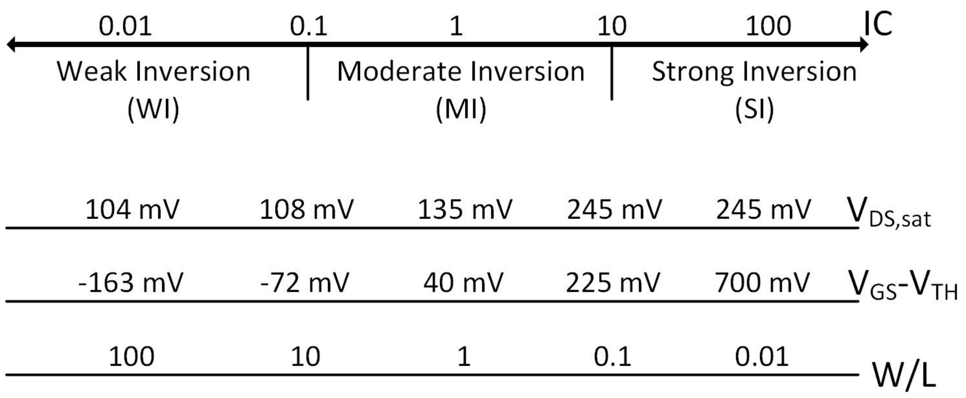


Figure 1.6 – Inversion coefficient line number with voltage and shape factor MOSFET properties [Bin07].

Current Reuse

The static power consumption in electronic circuit is given by the supply voltage V_{DD} and the bias current I_{bias} flowing from the supply voltage to the ground

$$P_{stat} = V_{DD} I_{bias} \tag{1.13}$$

If two cascaded circuits (A and B) are considered (Fig. 1.8) the total power consumption is equal to the sum of the single consumption:

$$P_{stat,tot} = P_{stat,A} + P_{stat,B} = V_{DD,A} I_{bias,A} + V_{DD,B} I_{bias,B} \tag{1.14}$$

The $P_{stat,tot}$ is reduced if the four variables are optimized. The main disadvantage is that the generation of two separate supply voltages increases the system complexity and power budget. In many case the chip size constraint and/or the energy available reduce space freedom degree in the design. Typically a single supply voltage is available for all circuit blocks. Therefore the optimization, from the supply voltage point of view, cannot be achieved completely and a lot of power is wasted. To overcome this problem and if an adequate supply voltage is available, stacked structure can allow power consumption reduction. In this case the bias current is recycled (reused) from the top circuit to the bottom one and the total power consumption is

$$P_{stat,stack} = V_{DD,stack} I_{bias,stack} \tag{1.15}$$

The condition to achieve lower power consumption in stacked topology is $V_{DD,stack} = V_{DD,A} = V_{DD,B}$ and $I_{bias,stack} = I_{bias,A} = I_{bias,B}$. Moreover some precautions have to be taken against cross-talk phenomena, noise and high frequency loop. In [TSM15] a stacked LNA-VCO is presented, where each block achieves comparable performances with the state of the art of stand alone circuit; a LC filter is inserted between the two circuits to present high impedance at the frequency of interest avoiding cross-talk degradation.

The reuse concept can be readapt to circuit level as in [?]. The RC relaxation oscillator used to generate the time reference to the system is reused to implement reading-out circuit for the measurement of the Relative Humidity. Therefore the oscillator accomplishes two tasks saving power consumption and area occupied.

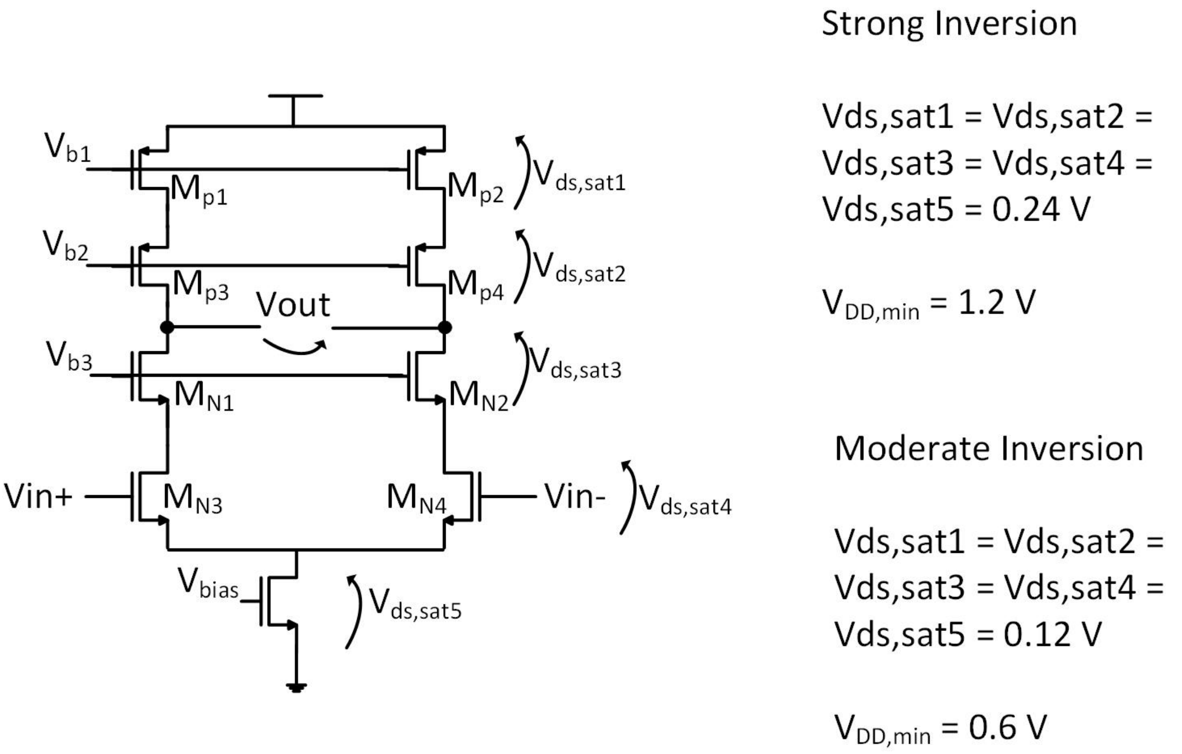


Figure 1.7 – Minimum supply voltage required in classical cascode OTA when the transistors are biased in strong and in moderate inversion.

Multi-threshold CMOS

The leakage power consumption has become a serious problem in below 100 nm technologies. In multi-threshold CMOS (MTCMOS) circuit, high-V_{TH} transistors are used to block the leakage path because of their low leakage current [SGMK15]. Basically it shuts-down a part of the circuit, disconnecting the main blocks from the power supply. Fig. 1.9 illustrates a typical application where high threshold transistors cut-off the NAND logic circuit. However this technique implies an increase in cost process due to an extra mask for the two different threshold voltages. Moreover there is a trade-off between the size of high-V_{TH} transistor and the performances degradation of the main circuit.

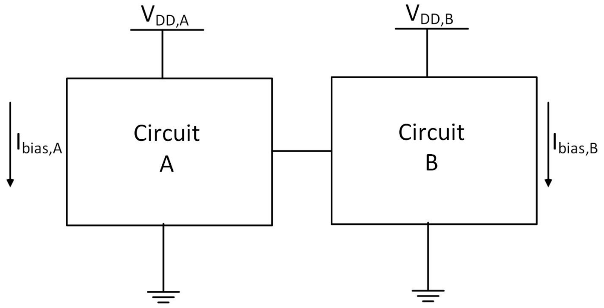


Figure 1.8 – Cascaded circuit block with two separate supply voltage and independent bias currents.

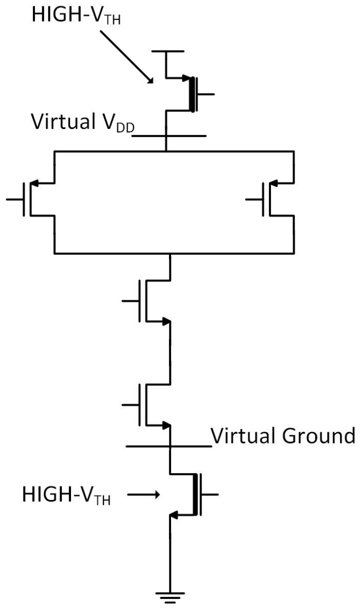


Figure 1.9 – Multi-threshold application in logic circuit.

1.2.3 System level

Wake-up scheme and duty-cycled radio

As it will be described in the next chapters the most hungry part in wireless sensor node is the transceiver circuit. A large number of papers suggest to keep the nodes transmitter part in low-power sleep mode for most of the time, allowing the node to operate at highest power consumption level only for a very short time. Wake-up scheme is a largely adopted technique to reduce the energy consumption extending the sensor node lifetime. Fig. 1.10 depicts the time-slot division for waked-up sensor node. The active time-slot includes:

- start-up time where auxiliary circuits generate the wake-up signal for the transmission/reception part. After the radio-frequency circuits need a settling time to achieve proper operation (especially for the frequency synthesizer).
- transmission/reception time where the communication between the sensor node effectively takes place.

To reduce the required overall energy both start-up and transmission slots have to be as short as possible for a lower power consumption. In [JLBS15] a 5.8 nW wake-up timer

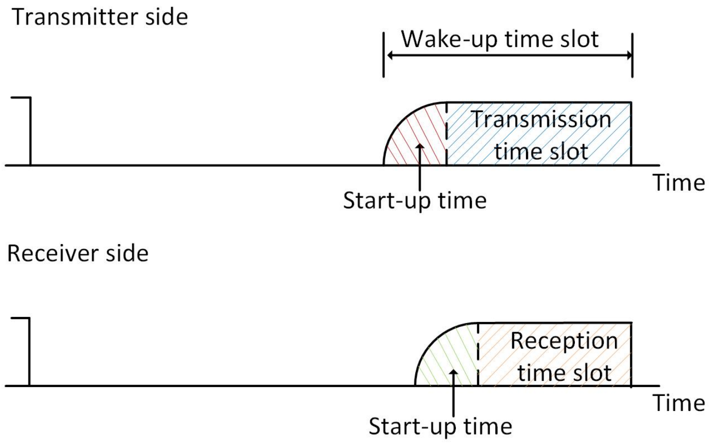


Figure 1.10 – Wake-up scheme timeline.

is presented and it is suitable for EHWSN, whereas in [TRE15a] the long start-up time phase-locked loop (PLL) frequency synthesizer is avoided using a fast film-buck acoustic wave resonator with a time reduction of ≈1000X.
However the system can be further optimized adopting duty-cycled operations during the transmission time. In this case the radio block is turned on/off with a rating that depends on the duty-cycle value:

$$DC = \frac{T_{on}}{T_{on} + T_{off}} \tag{1.16}$$

Aggressive DC in the range of (1-5)% can be adopted in burst communication mode, where a large amount of data is transmitted in short time with high data-rate.

1.2.4 Conclusion

In this chapter a description of the different energy harvesting sources usable for small scale applications has been presented. The low energy density available and the high variability pose a big challenge for the designers. Low-power design techniques are mandatory to extend the devices lifetime. The second part of chapter has described these techniques highlighting the advantages and the drawbacks.

The three level of optimization, transistor, circuit and system, can be combined to achieve the best trade-off between the performances and the power consumption. In the next chapters a system overview and a design flow for very efficient voltage regulator and ultra-low power transmitter are presented.

Chapter 2

System Approach

The technology progress occurred in the last ten years in highly integrated microelectronic circuits, sensors, actuators, and wireless communications technology allowed the dissemination of wireless sensor network (WSN) in several domains:

- **Environmental Monitoring**
  WSN can be used for forest surveillance, weather forecasting. It is a natural candidate, because the variables to be monitored are usually distributed over a large area. In addition WSN can facilitate the measurement of a large variety of environmental data for a huge number of applications such as agriculture, meteorology, geology, zoology, etc.
- **Health monitoring**
  WSN could potentially provide better health-care delivery. They could improve the interaction between the patient and the medical staff. Several physiological parameters can be monitored, as (hearth condition, blood pressure, blood glucose, organ monitor, cancer detector). When the sensors are implanted for healthcare purpose, they are called Body Sensor Network (BSN).
- **Industrial Sensing**
  The industrial sector is one of the most involved player for the development of WSN. With the possibility to acquire information in real-time, unexpected failures can be avoided improving production quality and reducing costs. One of the main use is in the food industry to monitor the food supply chain.
- **Home Security**
  Domestic represents another potential area for WSN. The "smart home" can regulate the room temperature, control air quality, adjusting lighting. Sensor networks can also improve the security of the house by sending an alarm message to the resident when it detects intruders, gas leakage, fire occurrence or other safety risks.

WSN can generally be described as a network of nodes that cooperatively sense and may control the environment enabling interaction between persons or computers and the surrounding environment. In spite of their versatility, the main constraint is the energy needed for the operation, specially when WSN are deployed in hostile environment or over a large area making the battery replacement very difficult, expensive or even impossible. For example, the study carried-out in [KBA16] shows the battery duration for WSNs with ZigBee/IEEE 802.15.4 protocol. This standard has been developed by the Institute of Electronic and Electrical Engineer (IEEE) for low-power, low data-rate wireless personal sensor networks (WPSNs). The most adopted transmission frequency is 2.4 GHz with

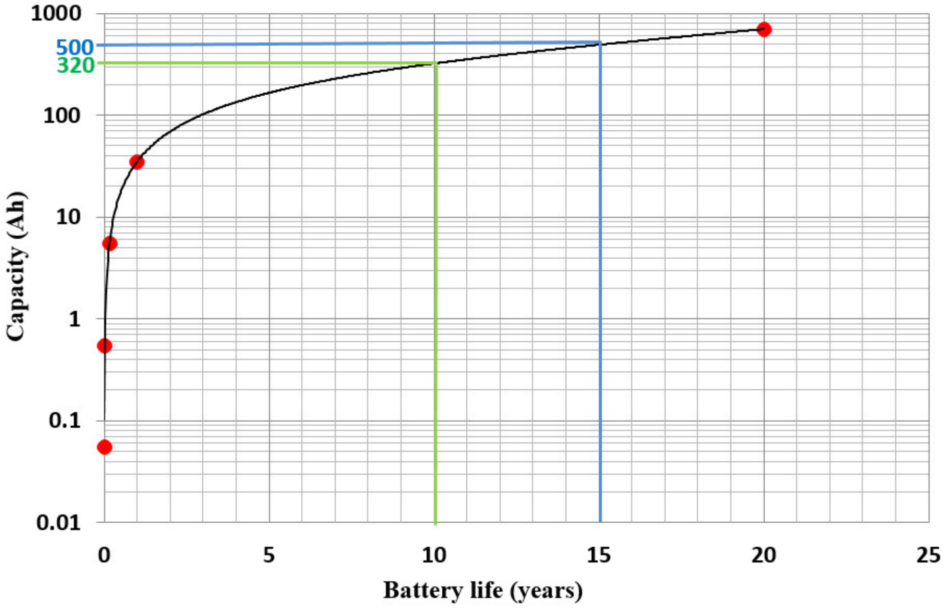


Figure 2.1 – Plot obtained from the measurement results for I = 2.3 mA and k = 1.25.

max data-rate of 250 kits/s and QPSK as transmission modulation. The IEEE 802.15.4 standard is used as a base for developing ad-hoc standard as in the case of ZigBee. ZigBee protocol adds different enhancements as authentication valid nodes, encryption for security and data routing. Moreover ZigBee supports energy harvesting technology for no battery supply.

Therefore one of the main problem of this standard, even if the low power consumption is one of the key point, remains the battery duration. In [KBA16] the study is based on the Peukert's law where the battery life is calculated as

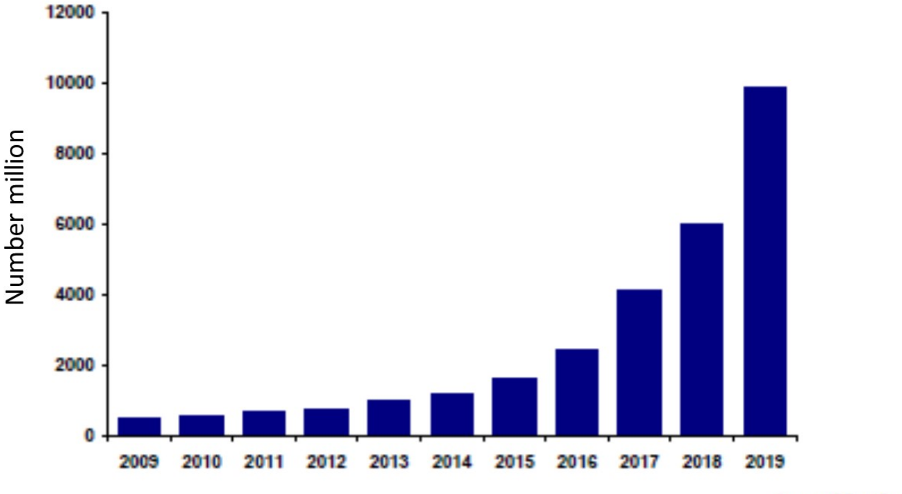
$$L = \frac{C}{IH}^{k} \tag{2.1}$$

where L is the time in hours for a given rate of discharge, H is the discharge time in hours, C the battery capacity in Amp.hours, I current in Amp and k Peukert exponent parameter which is a unique number for each battery. The experiment is conducted for three different batteries with different capacities. The communication distance is about 9 m and the data transmission is continuous. The results are summarized in Fig. 2.1 for I = 2.3 mA and k = 1.25.

Fig. 2.1 shows that, for 10 years of operation a battery with 320 Ah capacity is needed. However such type of battery exhibits large sizes; it is therefore not suitable for high integrated applications.

After a first wave, WSNs have meet a stop in the popularity due to the size limitation. WSN have found a second youth with the technology progress in energy harvesting (EH) domain, where the circuits responsible of energy conversion have assumed sizes more and more tiny easily fitting the request of smaller devices. Therefore, the possibility to have independent small sensor has open the future for new opportunities. The markets for WSNs invoices $ 552.4 millions in 2012 with a forecast of $ 14.6 billions in 2019. The Fig. 2.2 shows the trend of devices powered by EH system used in WSN.

Fig. 2.3 shows the market movement of EHWSN applications from 2012 to 2017. All



Source IDTechEx

Figure 2.2 – Market forecast for EH devices used in WSN applications.

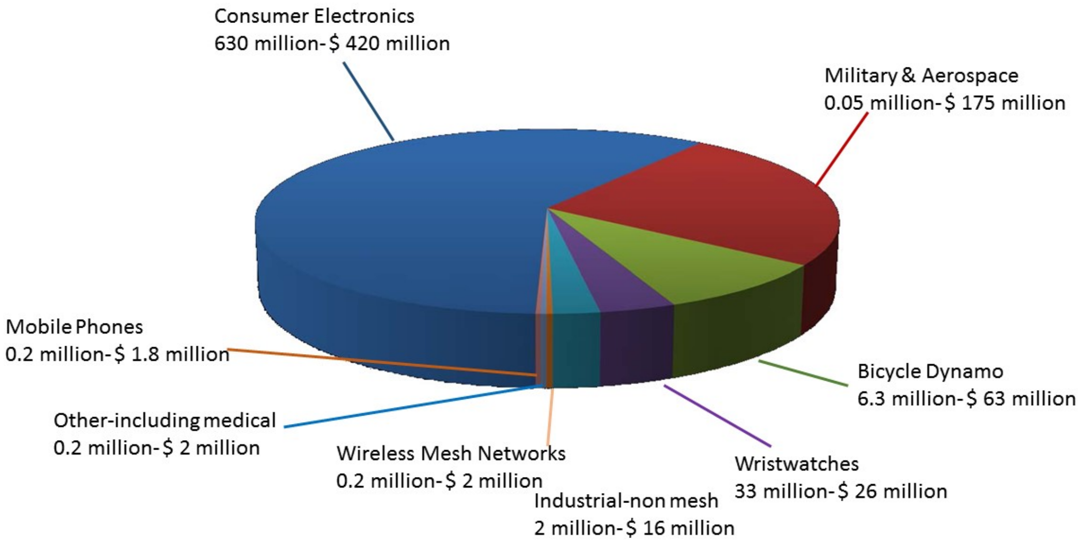
sectors exhibit an growth in the number of employed devices.

To make a sensor networks adaptable for a wide range of applications, the following requirements should be addressed:

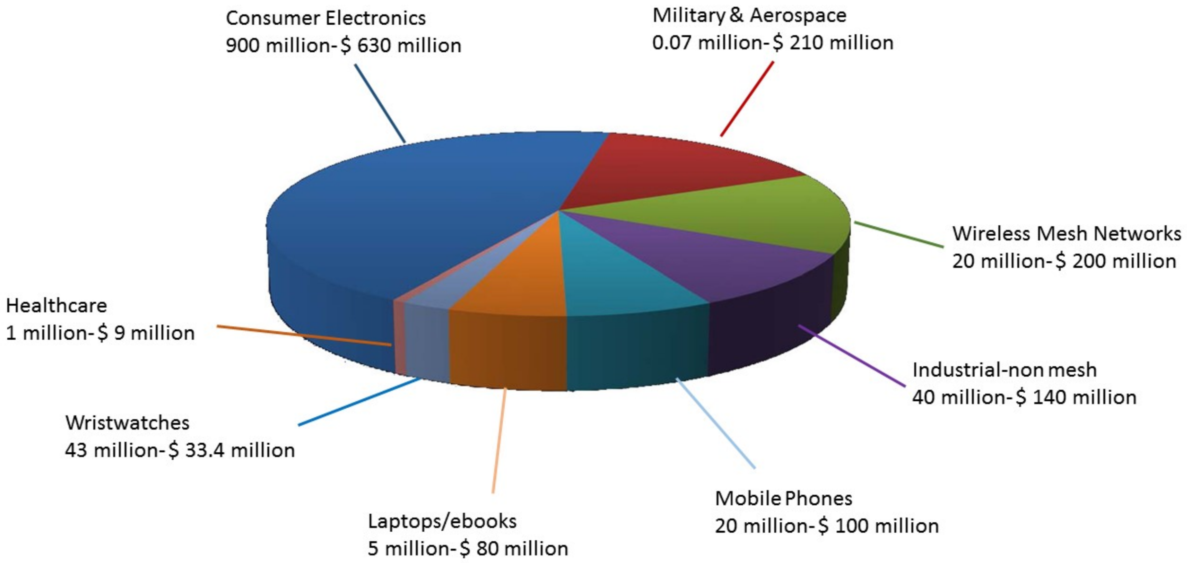
- Low Cost: The utility and scalability of a WSN highly depend on its density, which means large number of sensor nodes in the assignment area. To make the installation cost effective, the cost of individual sensor node should be extremely low.
- Low Power: Nodes must be able to ensure a permanent connectivity and coverage for long periods, up to 10-20 years, without service interruption. Low power consumption represents one of the main challenge in modern devices, and it is of great importance when the sensor is supplied by low density energy source.
- Small Size: WSNs are desired to replace cables that are often impracticable. Therefore, the size of the sensor node must be small enough in order to allow the WSNs to monitor the environment in a discreet and transparent manner.

However nowadays as introduced in the Chapter 1, the energy available from the harvesting transformation is not sufficient to power the sensor node in continuous mode operation. For example the harvested power from vibration in industrial application can easily achieve 100 μW$/cm^2$ [RM10], but modern sensor node in transmission mode requires about 5 to 10 mW depending on the application. Fig. 2.4 shows that if one hand WSN requires less power thanks to development technological, on the other hand high efficient harvesting circuits allow to maximize the low energy available from the environmental sources.

However until now, technologies limitation (for example leakage current, process deviations) and performance constrains (noise, PVT variations) prevent the two curves to reach a intersection point. Actually a continuous autonomous operations can not be therefore assured. The sensing and data communication reliability can be assured only if sensor node operates for a fraction of total time. Therefore the two curves can approach, because micro-watt power availability is able to sustain operations in the range of mW. The building block diagram of an EH sensor node is shown in the Fig. 2.5



(a)



(b)

Figure 2.3 – Energy Harvesting WSN market in 2012 (a) and prevision of market in 2017 (b)

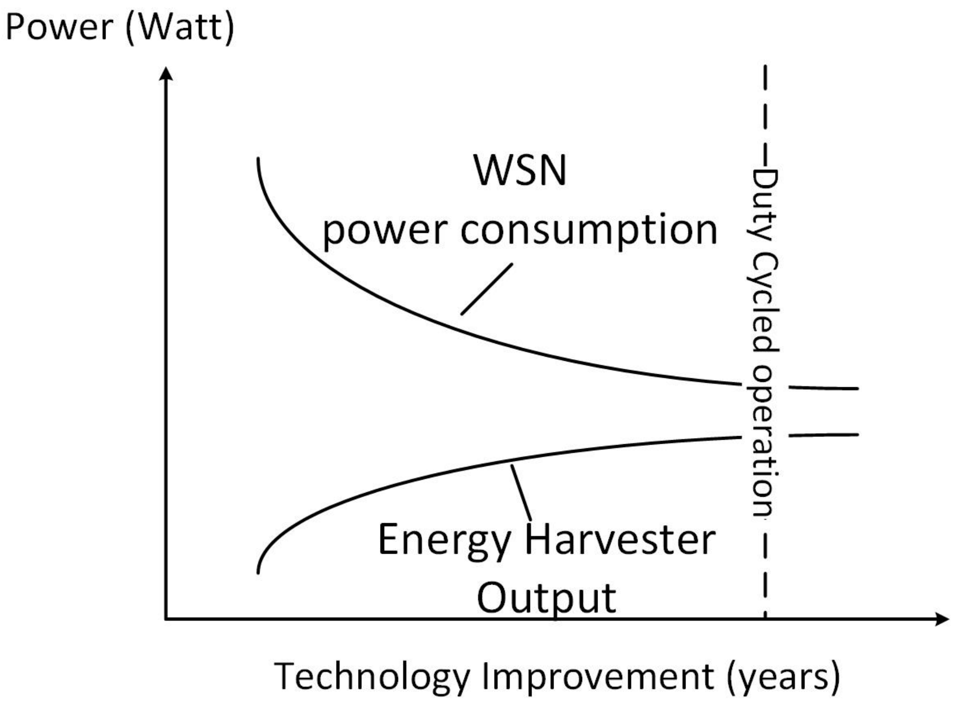


Figure 2.4 – Power comparison between WSN and Energy Harvested circuit.

The electrical energy coming from the harvest transformation can be used to directly supply the sensor node or stored into a supercapacitor or a rechargeable battery. Although in some applications it is possible to bypass the energy storage, in most of the case the storage component acts as an energy buffer for the system, with the main purpose of accumulating and preserving the energy.

In order to manage the energy available from the storage element, the power management unit (PMU) has to be designed to extend the sensor lifetime. It controls the level of stored energy and at the demand of power depending on the adopted protocol, it supplies the sensor and/or the other circuits. The environmental information sensed is then transformed into digital information by the ADC and stored in the memory. In general the sensing and the data transmission are not accomplished at the same time, because the transmitter is the main power hungry block and the energy available is not enough to guarantee the two operations at the same time.

Finally the data transmission can be validated internally by the PMU or externally on demand by the users.

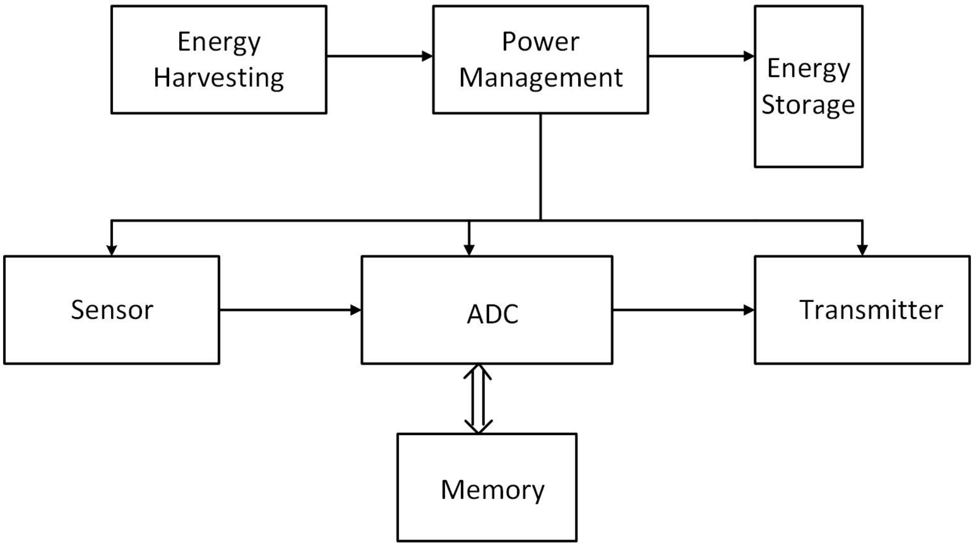


Figure 2.5 – Architecure of energy harvesting sensor node.

2.1 Energy Management

The purpose of this work is to design low-power circuits for RF-energy harvesting WSN. In particular low drop-out voltage regulator and transmitter block have been designed. A framework at the system level can facilitate the circuit design.
As briefly introduced an energy buffer (rechargeable battery or super-capacitor) is mandatory for duty-cycled power manager to stock the energy when the system is in idle mode and then make it available when requested. A simple PMU introduced in [PCFP14] is depicted in Fig.2.6. To supply the regulated voltage to the RF front-end blocks, PMU uses different circuits to manage the stored energy.
Voltage limiter is used to limit the maximum voltage with a safe margin.
The voltage sensor verifies that the voltage across the capacitor is between two defined bends V_{low} and V_{high}.
When the voltage stored into the capacitor reaches V_{low}, the PMU turns-off the voltage regulator and the system is in idle mode. During the idle mode the PMU draws a little bias current due to the monitoring circuits that are continuously on to ensure proper operation. When the voltage capacitor reaches V_{high}, the PMU turns on the voltage regulator, the current flows from the capacitor to the voltage regulator output and the sensing operation and data transmission can take place.
It seems clear that in the case of linear voltage regulator, where the regulated output voltage is obtained "loosing" a part of input voltage over a variable resistor, the stable PMU output voltage V_{reg} has to respect the following condition

$$V_{reg} < V_{low} < V_{high} \tag{2.2}$$

where V_{reg} depends on the application specifications (transmission distance, quality and speed of transmission) and on the circuit architecture (stacked topologies, technology reliability), V_{low} depends on the voltage regulator performances and on the minimum input voltage for which the regulation is ensured, V_{high} can be obtained by the system energy analysis. Fig. 2.7 shows the energy profile (top figure) of harvesting sensor node where the

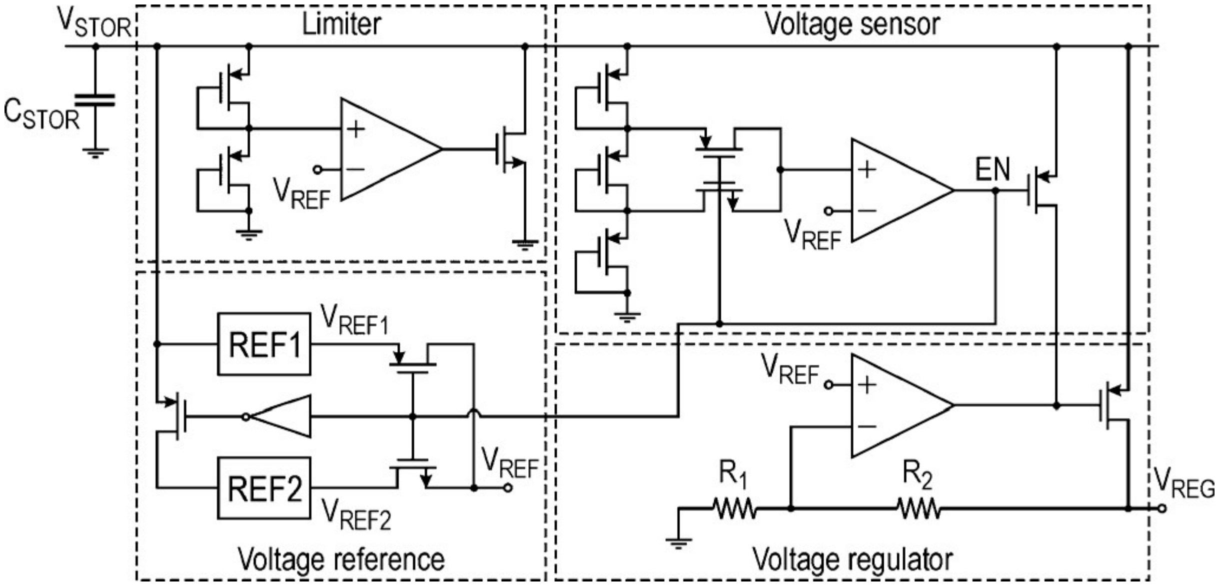


Figure 2.6 – Power management transistor level schematic implemented in [PCFP14]

transmission time t_{on} is less than the idle time t_{off}. In this case high power hungry circuits as frequency synthesizer and power amplifier can be sustained by low power source as RF energy harvesting. The bottom graph in Fig. 2.7 shows the transient of voltage stored in the capacitor and the voltage at the regulator output. During t_{off} the sensor node is in harvesting mode and the capacitor is charging. The charging time depends on source signal quality. During this time interval the energy cost of monitor circuits has to be very low in such way to preserve the capacitor charge.

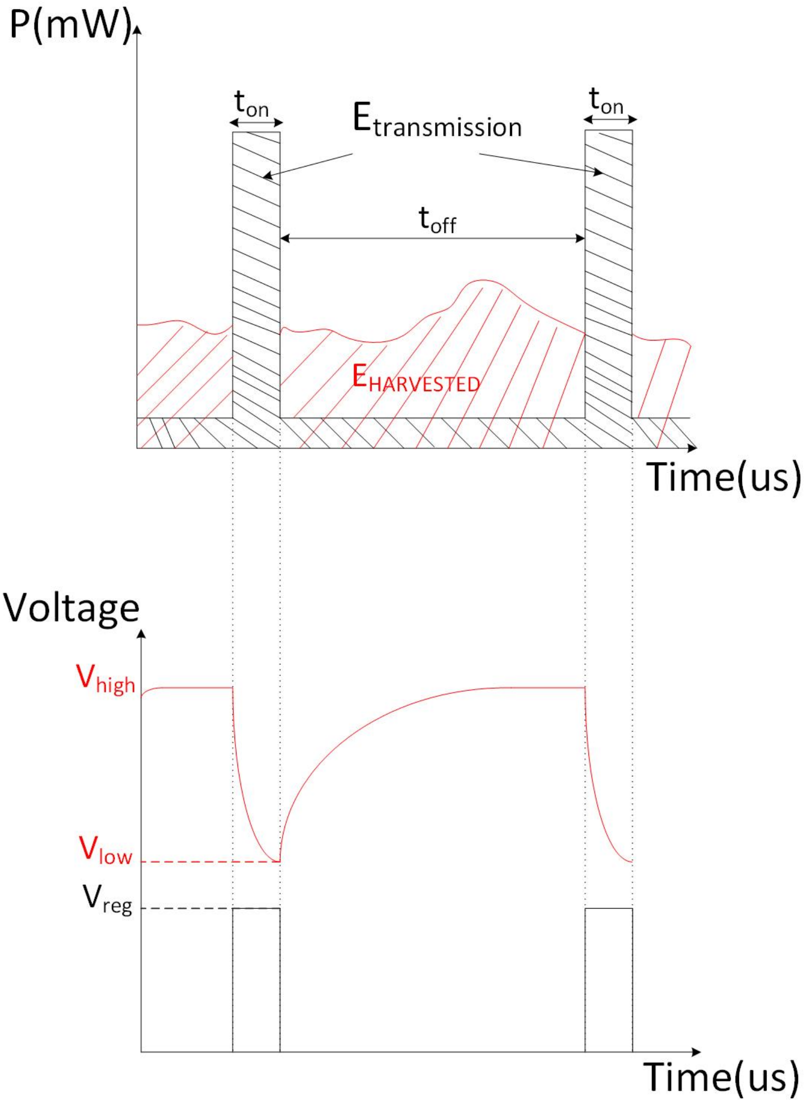


Figure 2.7 – The top graph depicts an example of energy profile in harvesting system. In the bottom graph the trend of voltage stored into the capacitor (red line) and the regulated voltage at the output of the PMU.

The energy stored in the capacitor C is given by

$$E_C = \int_{Q_i}^{Q_f} \frac{Q}{C} \mathrm{d}q = \frac{1}{2C}(Q_f^2 - Q_i^2) \tag{2.3}$$

where Q_f is the charge stored at V_{high} and Q_i is the charge stored at V_{low}. The energy stored in the capacitor can be rearranged as

$$E_C = \frac{C}{2}(V_{high}^2 - V_{low}^2) \tag{2.4}$$

The energy needed for the data communication, assuming OOK modulation scheme for the transmission circuit (PA,VCO), and continuous operation during modulation for the other circuits to reduce start-up time can be written as

$$E_{transmission} = E_{TX} + E_{reg} = (pP_{DC,TX} + P_{DC,system})t_{on} + (I_{load}V_{drop})t_{on} \tag{2.5}$$

The above equation is obtained assuming the following hypothesis :

- The transmitter block is responsible of the DC power consumed $P_{DC,TX}$ modulated by the probability p to transmitting a '0' or '1' data bit.
- $P_{DC,system}$ includes the DC power consumed by the control circuits
- As it will be explained in the next chapter, a linear voltage regulator has been chosen to transform the unregulated input voltage to the regulated output one. The power dissipated by the voltage regulator is mainly due to the voltage dropped across the pass element V_{drop} and to the load current I_{load} that flows from the input to the output. As I_{load} is quite high, due to the bias current drawn by the transmitter, the energy required by the regulator can not be neglected.

Surely the energy required by the transmission block has to be equal to the energy stored in the capacitor

$$E_{transmission} = E_C \tag{2.6}$$

therefore from the upper equation is possible to find the storage voltage V_{high}

$$V_{high} = \sqrt{\frac{2t_{on}}{C}(pP_{DC,TX} + P_{DC,system} + I_{load}V_{drop}) + V_{low}^2} \tag{2.7}$$

Observing the above equation V_{high} relies on different parameters: the size of the storage capacitor C, the power consumed by the transmitter, the type of modulation and also the amount of data to be transmitted. Indeed t_{on} is obtained by the ratio between the data packet length and data-rate. It is interesting to note that V_{high} value impacts the regulator energy efficiency. Without entering into detail,because voltage regulator is the subject of the next chapter, the energy efficiency can be writen as

$$\eta_{energy} = \frac{V_{reg}I_{load}t_{on}}{V_{in}I_{load}t_{on}} = \frac{V_{reg}}{V_{in}} \tag{2.8}$$

V_{in} is not fixed but decreases from V_{high} to V_{low}. The above equation states that the three voltage values V_{reg}, V_{high} and V_{low} have to be as close as possible in order to not deteriorate the regulator efficiency.

2.2 Link budget, data rate and duty cycle.

2.2.1 Required link Budget

Generally the power consumed by the power amplifier (PA) to cover a given distance is the main contribution to the power dissipated by the transmitter block. Outdoor sensors are generally 100 m spaced-out and the communication is almost free of obstacles. On the other hand, in indoor network the transmission antenna has to cover a range about of 5-10 m and the signal quality could be degraded by walls. Different is the situation for BWNs where the distance does not exceed 1 m. The PA DC power is strictly dependent on the RF output power level needed for the applications. The first step in the transmitter design concerns the estimation of the power radiated P_{rad} at the PA output. At first glance, the required P_{rad} can be obtained as follow:

$$P_{rad} = P_{RX} - G_{antenna} - PL = P_{RX} - G_{antenna} - 20\log\left(\frac{\lambda}{4\pi D}\right) \tag{2.9}$$

where P_{RX} is the receiver sensitivity, $G_{antenna}$ is the antenna gain, λ is the wave length for the carrier frequency and D is the communication distance. The gain of a typical surface mount antenna can be estimated at 0 dB for a frequency carrier of 2.4 GHz while the path loss (PL) terms in free space can vary between -22dB to -30dB for a distance D between 1m to 10m. The last term in the right side of the eq. 2.9 P_{RX} is almost difficult to calculate [Ben09] because it relies on several variables:

$$P_{RX,dBm} = N_{in} + NF + 10\log(B) + (Predicted\frac{S}{N}) => P_{RX,linear} = N_{in} \times NF \times B \times \frac{S}{N} \tag{2.10}$$

where N_{in} represents the input noise density originated on the source resistance for example antenna equivalent resistor. N_{in} = -174 dBm/Hz is considered for a perfect receiver at room temperature having a bandwidth of 1 Hz (no internal noise and ability to operate with a signal having the same power as the input noise).

B is the bandwidth of the receiver signal and $\frac{S}{N}$ is the signal to noise ratio and can be specified to attain a given BER (bit error rate), depending on the adopted modulation scheme.

The receiver noise figure NF is the difference between the input $\frac{S}{N}$ and the output $\frac{S}{N}$ and it gives an information about the noise generated by the receiver circuit blocks.

To give an order of magnitude about the receiver sensitivity the Tab 2.1 shows the receiver State of the Art for ultra-low power application.

Table 2.1 – Comparative ULP receiver

	[VHH+11a]	[LBvdH+14]	[OST+16]	[LBW+15]	[PPA+15]
Data-rate	5Mbps	2Mbps	1Mbps	250kbps	250Kbps
Modulation	OOK	HS-OQPSK	GFSK	-	-
Topology	Super Reg.	SIF-PDC	Hybrid Loop	-	-
P_{diss} (mW)	0.534	2.4	6	3.3	11.2
P_{RX} (dBm)	-75	-92	-90	-94	-94.5

Evaluating the data reported in the previous table an average value of -92 dBm can be considered for ULP receiver. Therefore the minimum P_{rad} in the case of 2.4 GHz signal carrier, for an average communication distance D of 5 m has to be equal to -38 dBm. To cover a shorter distance of 1 m the P_{rad} decreases to about -50 dBm. However these are optimistic values, because estimated with the transmission occurring under ideal conditions. To overcome sudden variations, 30 dB of path loss should be added for safe margin. An ULP transmitter with an average transmitter power of -15 dBm is considered. To give an idea about the power consumption of a transmitter, it is possible to assume that the PA is the most power hungry circuit. Therefore the DC power required for a given P_{rad} in the case of class-A topology is:

$$P_{DC} = \frac{2V_{DD}^2}{R_L} \tag{2.11}$$

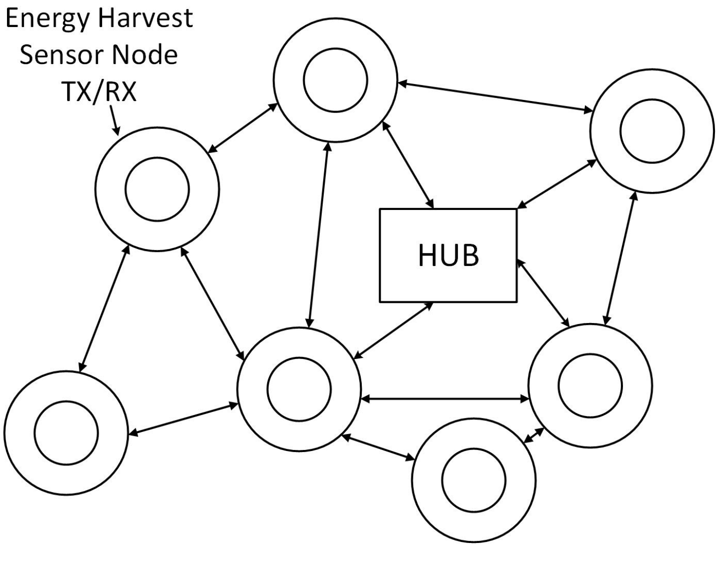


Figure 2.8 – Wireless sensor network mesh architecture

P_{DC} = 40 mW is dissipated to transmit -15 dBm with a supply voltage of V_{DD} = 1 V delivered on a 50 Ω output resistance R_L.

The energy required to transmit n-bit length data depends on the performances of the receiver. High sensitivity demands indeed high receiver power consumption but lower transmitter consumption.

A typical sensor node is equipped with a radio block for transmission and reception operation. For example, in mesh networks (fig. 2.8) the message is propagated along a path by hopping from node to node until it reaches its destination. Optimizing both receiver and transmitter can represent an hard task in energy harvesting environment, because lowering the power radiated surely means lower power consumption for the transmitter circuits but, on the other side, the receiver needs high sensitivity to decrease error bit ratio and this increases its power consumption. The same trade-off occurs when lower sensitivity is accepted, because of the increased radiated power.

To alleviate the sensor node complexity and to separate the trade-off between radiated power and receiver sensitivity, a centralized network (fig. 2.9) can be adopted, where the data message passes from the sensor to the HUB in an unidirectional way. Therefore the sensor nodes are equipped only with the transmission block and they are powered by harvesting source. The HUB can perform both operation, transmission and reception, with high performances because it is equipped with a large capacity battery. The transmitter in sensor node can be optimized under a power consumption point of view, since the receiver can achieve high performances and complexity.

In any case to extend the network lifetime the energy required by the transceiver to process the incoming signal has to be limited. A rendez-vous scheme based on pseudo-asynchronous protocol is possible to adopt where the data transmission is accomplished on demand, using a periodic wakeup scheme. In [LRWW05] is demonstrated that Receiver-Initiated Cycled Receiver (RICeR) outperforms low power consumption when compared to Transmitter-Initiated Cycled Receiver (TICeR). In RICeR the destination node has the task to initiate the packet exchanges. Basically the data transmission is done as follow fig.2.10:

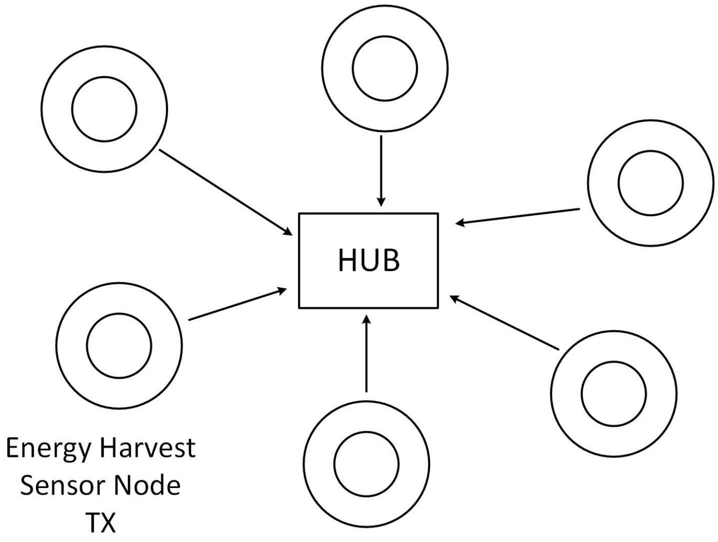


Figure 2.9 – Wireless sensor network star architecture.

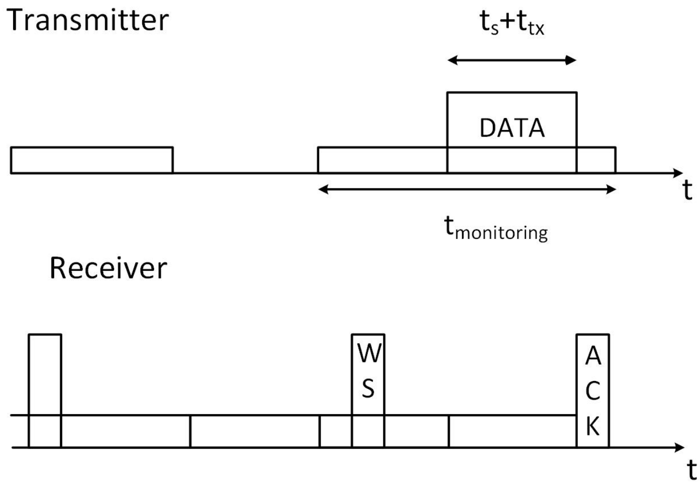


Figure 2.10 – RICER.

The destination node sends a wakeup signal (WS) to the adjacent nodes to communicate the willingness to receive the data packet. If there is no response, the node goes back to sleep. At the same time the source stays awake monitoring the channel. After the (WS), the communication takes place and the destination node ends the session with an acknowledgment sent to the source node.

2.2.2 Data Rate and Duty Cycle Trade-off.

In transmission system, data-rate (DR) is the rate at which the data informations are transmitted. Considering the bandwidth allocation the Shannon's theorem gives the possibility to calculate the channel capacity C (the maximum rate at which the data can be transmitted over given communication path and under given condition)

$$C < B \log_2 \left(1 + \frac{S}{N}\right) \tag{2.12}$$

Where B is the channel bandwidth and $\frac{S}{N}$ is the signal to noise ratio specification.
For short range devices the Electronic Communication Committee (ECC) has established the ERC recommendation [ECC17] for each frequency band and for different applications. For tracking, tracing and data acquisition in sensors and actuators applications, medical body area network system, wireless industrial application in the frequency band 2483.5-2500 MHz for 1 mW max output power radiated the maximum occupied bandwidth has to be less than 3 MHz.
Therefore the channel capacity using the Eq. 2.12 is equal to 10 Mbps for 10 dB of signal noise ratio. As the DR states the TX payload, it is understandable that for a given number of bits N_b higher DR means shorter transmission time. Therefore it is possible to express the energy needed to transmit a string of n bits as

$$E_b = \left[P_{BB} + \frac{P_{rad}}{\eta}\right]\left[\frac{N_b}{DR}\right] = \left[P_{BB} + \frac{P_{RX}}{\eta \times G_{antennna} \times PL}\right]\left[\frac{N_b}{DR}\right] \tag{2.13}$$

where P_{BB} is the power dissipated by the baseband circuits, η is power efficiency which is equal to the ratio of P_{rad} and the DC power dissipated by the TX circuits $P_{DC,TX}$. The E_b stated in the eq. 2.13 is low limited due to some trades-off between the variables involved in the equation.

- The baseband power consumption is limited due to the noise performance and PVT (Process Variation Temperature) as the weak inversion region is exploited for the Mosfet transistors.
- High Power efficiency requires high radiated power, but it is not the case in short distance communication where $P_{rad} \approx 100\ \mu$W. As it will be demonstrated in chapter 4, designing a transmitter block with the same power consumption is a very hard task.
- At first glance it seems that high data rate reduces the required energy [DvdZBK11] [ESY05]. This is true until the power consumption due to the higher frequency operations does not increase excessively. Moreover the noise bandwidth increases accordingly and better sensitivity is required for the same bit error rate.

By introducing the spectral efficiency η_{DR-BW}, as the ratio between DR and B

$$\eta_{DR-BW} = \frac{DR}{B} \tag{2.14}$$

Therefore expressing the P_{RX} in linear value, the eq. 2.13 can be rearranged as

$$E_b = \left[P_{BB} + \frac{N_{in} \times NF \times DR \times \frac{S}{N}}{\eta \times G_{antenna} \times PL \times \eta_{DR-BW}}\right]\left[\frac{N_b}{DR}\right] \tag{2.15}$$

The results obtained is derived for continuously operation. However, intuitively and as largely reported in literature, the sensor node lifetime is extended when a duty-cycle protocol is adopted. Duty Cycle is the ratio between the slot-time when the sensor is on and the total time. This technique allows to preserve energy, because in off mode the node burns very low power in comparison with the on mode.
Following the indication in [TRE15a] the duty cycle DC can be calculated as

$$DC = \frac{DRA}{DR} \tag{2.16}$$

where DRA is the application data rate and DR is the data rate achievable by the system. By obtaining the DR in function of the DC and DRA, substituting it into eq. 2.15 and considering the carrier generation circuits start-up as in fig. 2.10 the energy required to transmit n bit is equal to:

$$E_b = \left[P_{BB} + \frac{N_{in} \times NF \times DRA \times \eta_{DR-BW} \times \frac{S}{N}}{\eta \times G_{antenna} \times PL \times DC} \right] \left[\frac{N_b \times DC}{DRA} + t_s \right] \tag{2.17}$$

The above equations states that an aggressive DC, up to 5%, do not allows a reduction in the required energy per bit because it is present at the numerator and denominator in the right side of the equation. Moreover the choice of low or high value affects the power consumption in both receiver and transmitter part. In wake-up scheme both transmitter and receiver have to be turn-on and turn-off periodically, therefore to achieve low DC the two circuits the start-up time has to be reduced consequently. A quick response is obtained with an increase in the power consumption and observing the eq. 2.17 it is clear its no-monotonic trend with the duty-cycle. Generally speaking aggressive DC requires higher power consumption.
Therefore it is possible from the eq. 2.17 to calculate the optimum DC for which the energy required is minimum.

$$\frac{\delta E_b}{\delta DC} = 0 => DC_{opt} = \sqrt{\frac{N_{in} \times NF \times \eta_{DR-BW} \times t_s \times DRA \times \frac{S}{N}}{\eta \times G_{antenna} \times PL \times P_{BB} \times N_b}} \tag{2.18}$$

The optimum duty-cycle relies on several parameters and there are some constraints which impose the boundaries for the choice of the duty-cycle. For the example $G_{antenna}$ increases with the sphere radius that completely contains the antenna and the small size demanded to the sensor node limits the maximum antenna gain consequently. Processing longer bit string increases the circuit complexity and it affects other system performances as signal-to-noise ratio, the noise figure and the bandwidth efficiency.

2.2.3 Conclusions

An overview has been given of WSN and physical layer node. Moreover the energy constraints have been shown and also the techniques and the circuit performances that have to be considered to extend the node lifetimes have been detailed.
The relation between the maximum and minimum stored voltages into the capacitor and the regulated voltage have been introduced considering the voltage regulator energy efficiency.
As concern the transmit section, the indication about the link budget has been given and the trade-off between the receiver sensitivity and data rate has been explained. Duty-cycle operation shows that to be a powerful technique to reduce the energy cost for transmitted data. Optimum Duty-Cycle value permits to reduce as much as possible the required energy per bit.
The results obtained in this chapter are used to properly design high about the performances for voltage regulator and transmitter.

Chapter 3

Voltage Regulator

In RF energy harvesting system, the DC voltage obtained from the AC-DC conversion of the incoming signal suffers from the variability of the wireless power transfer itself. To smooth these fluctuations a voltage regulator is mandatory to deliver a clean voltage for delicate circuit blocks as: ADC, VCO, etc. As explained in the previous chapter, the low energy available imposes different challenges in terms of performances for every involved circuit. This chapter describes the design methodology of ULP low drop-out (LDO) voltage regulator with good regulation performances while keeping high power efficiency.
The first part of the chapter provides an overview on the main characteristics of the voltage regulator and the comparison between the two topologies of regulation: switching and linear. The reasons of choice are also illustrated. The chapter then ends by describing the design methodology of the LDO regulator with the simulation results.

3.1 Background

In modern devices, the energy management and the power delivery have assumed a crucial role. Optimizing the use of the energy contained in a battery or in other storage device, for example super-capacitor as in the case of harvesting source, allows to extend the autonomy of the device. The power management unit (PMU) Fig. 3.1 is responsible for a balanced distribution of energy according to the circuits consumption and the state of operations.

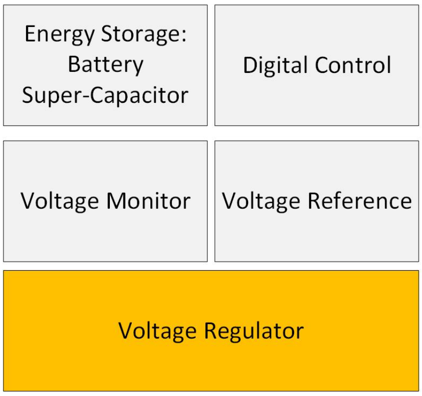


Figure 3.1 – Power Management Unit

The efficiency of harvesting systems strongly depends on the optimization of the power management unit. Due to the energy constraint, only by means of a depth understanding of the application it is possible to make the correct choices in terms of architecture and performances. For example in a body area network application (BAN), the sensor and the transmission block have to turn-on frequently to monitor the vital parameters for a short time period with very short distance (< 10 cm); while in wireless sensor application (WSN) where the distance is more important (> 1 m), the transmission time has to take a longer duration to prevent false data transmission due to channel interference. It is clear that the two applications are different in terms of data-rate, frequency modulation, duty-cycle and power consumption. For example in [MBT$^+$13] the PMU has to manage two different duty-cycled signals, in order to power supply or not the sensor and UWB transmitter, saving the power consumption. Typically the power management unit directly interfaces with the load through the voltage regulator. In most of case, the regulation performances dictate the design specifications of the PMU (output voltage, max. supply current, transient response, etc). The following section describes the two different methodologies of regulation illustrating the advantages and the drawbacks for each of them.

3.2 Voltage Regulator

Voltage regulator is a circuit that converts an unregulated DC input voltage into a stable and clean DC output voltage. A stable and clean voltage at the output terminals is desired, in order to not deteriorate the performances of the load circuits. It is composed of two main parts as depicted in Fig. 3.2

1. the conversion stage transforms the unregulated input voltage to a regulated output one.
2. the control feedback monitors the output voltage and tunes the conversion stage condition in order to keep the output voltage at the nominal value

Evaluating the static and dynamic characteristics, not only permits to compare the different topologies but also to understand the performances to improve which best match with the targeted application.

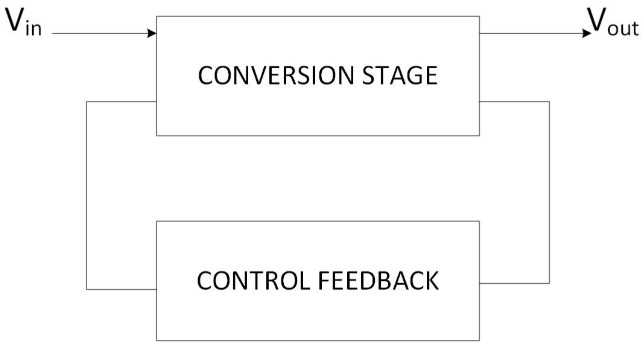


Figure 3.2 – General block diagram of voltage regulator

3.2.1 Static Characteristics

The static characteristics are evaluated under steady-state conditions when all the transient phenomena are clearly completed. They differ for the DC or AC nature.

Efficiency

In energy harvesting system the efficiency is one if not the most important design criterion to evaluate. It gives the power cost of the transformation, in other words the amount of power loss in the circuit. The efficiency is expressed as the ratio between the delivered output P_{out} and the input power P_{in} :

$$\eta = \frac{P_{out}}{P_{in}} \tag{3.1}$$

An efficiency of 100% means no power loss. But with real components the power is dissipated in resistive part or in other way as leakage phenomena.

Power Density

The power density puts in relation the efficiency with the area occupied by the chip. It is expressed as P_{out} normalized to the total area A:

$$PD = \frac{P_{out}}{A} \tag{3.2}$$

Load Regulation

The load regulation describes the variations of the steady-state output voltage when output current I_{LOAD} changes (Fig. 3.3)

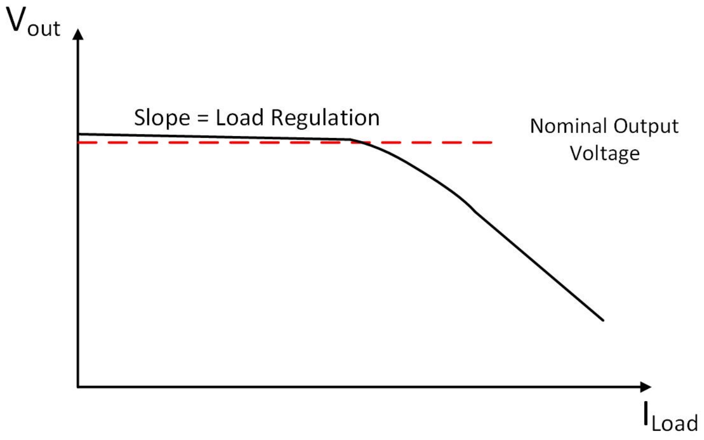


Figure 3.3 – Load Regulation

As the load regulation is not linear for the entire load range, it is measured for the minimum and maximum value

$$LoadRegulation = \frac{V_{out1} - V_{out2}}{I_{out1} - I_{out2}} = \frac{R_{OL}}{1 + A_{ol}\beta_{FB}} \tag{3.3}$$

where R_{OL} is the open loop output resistance, A_{ol} the open-loop gain and β_{FB} the feedback factor of the regulator. V_{out1} and V_{out2} are the boundaries of output voltages considered and I_{out1} and I_{out2} the respective output currents. The load regulation is related to the open loop gain of the converter. So higher open-loop gain is preferred to assure a better regulation.

Line Regulation

The line regulation describes the variations of the steady-state output voltage for a variation of the input voltage V_{in} (Fig.3.4)

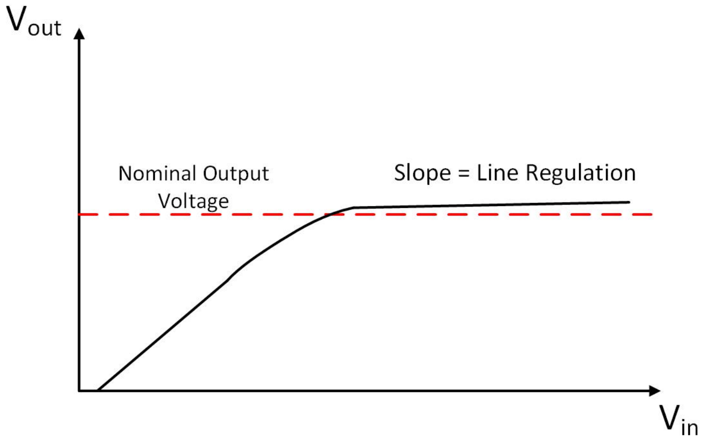


Figure 3.4 – Line Regulation

It is measured for the minimum and maximum value of unregulated input voltage

$$LineRegulation = \frac{V_{out1} - V_{out2}}{V_{in1} - V_{in2}} \approx \frac{1}{1 + \beta_{FB}A_{ol}} \tag{3.4}$$

Where A_{ol} is the open loop gain and β_{FB} is the feedback factor. So line regulation is improved by high open-loop gain.

Noise

The noise is an AC characteristic and it quantifies two aspects of the regulator: 1) the capability to suppress the interferences coming from the input signal; 2) the inherent noise produced by the regulator itself. The noise performances are evaluated with power supply rejection ratio PSR.

3.2.2 Dynamic Characteristics

The dynamic characteristics exhibits the capability of the regulator to restore the output voltage when a transient event appears.

Transient Response: Output overshoot and undershoot
Overshoot and undershoot response are the deviation from the nominal output voltage due to a transient signal in load or control line. The feedback control has large impact on this parameter. A wide bandwidth of the control loop ensures a small voltage variation and a fast settling time at the output voltage when a load/line transient occurs. It should be specified under which circumstances and operating points the overshoot or undershoot occurs.

In the following section the description of two main conversion methodologies are given, switched and linear, illustrating the advantages and the weaknesses of each one and concluding with the analysis that demonstrates as linear regulator is the topology which best suits with the harvesting system.

3.3 Switching versus Linear

The reduction of the dimensions and the chip costs are the biggest challenges in modern electronic devices. Nowadays these problematics are managed with two types of integration: System on Chip (SoC) and System in Package (SiP). In the first approach the electronic circuits are integrated on the same silicon die, while the second includes two or more different technology dies, usually with external passive components. With the aggressive technology scaling achieved in last 10 years and accompanied by the demand of devices ever smaller, SoC is the topology that best fits with these constraints. However, the main problem is the integration of passive components, inductors and capacitors, that suffer from low quality factor. In SiP the possibility to use large passive components with better manufacturing quality, is counteracted by the large occupied area. Moreover, it requires advance packaging technologies (fine pitch flip chip, wire bonding, high density SMT) and complex electromagnetic interference shielding.

The Linear Regulator is well suited to be completely integrated on chip.The Fig. 3.5 depicts a classical representation of a linear regulator. The conversion is performed by changing the resistance of the pass element connected in series between the input and output voltage. The impossibility to be completely integrated occurs only when a large output off-chip capacitor (1 μF) is used to ensure the stability of the negative feedback loop [1]. Recent works have largely demonstrated that when compensation techniques are applied to the internal loop, a small integrable capacitor can be used at the output of the regulator.

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[1] Two methods accomplish the closed loop stability: externally and internally compensated. In the first topology the second order response of the loop is assured with the main pole at the output. In the second one the main pole is located inside the loop.

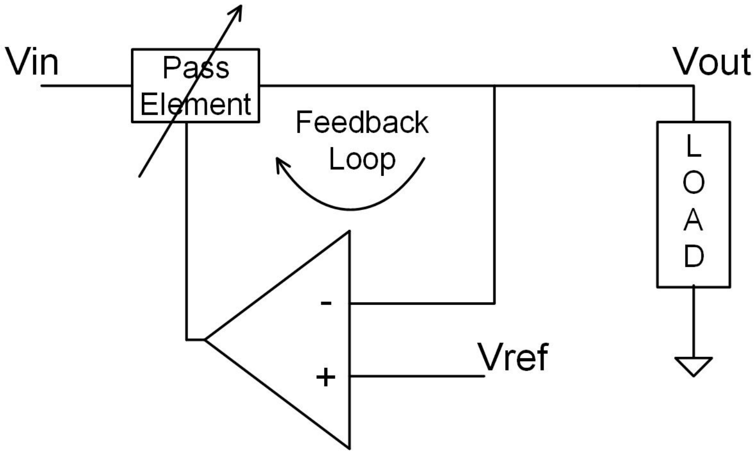

Figure 3.5 – Linear Regulator

For example, only 5 pF compensation capacitor with a cascode current compensation stage to achieve the stability is needed [LGZ⁺15]. Q-reduction circuit proposed in [LML07] permits to minimize on-chip capacitor (7 pF) and quiescent current. One of the main limits is that only down-conversion is possible, given that the output voltage is the difference between the input voltage and the voltage drop over the pass element. Due to the continuous linear control and the fact that the conversion is performed dissipating the power on the pass element, the power efficiency is not one of the strengths of this topology. Analyzing the efficiency equation:

$$\eta = \frac{V_{out} I_{Load}}{(I_{Load} + I_q) V_{in}} \tag{3.5}$$

where I_q is the total drawn current to the ground, it is not preferable to have large conversion ratio $\frac{V_{out}}{V_{in}}$ as anticipated in chapter two. If the quiescent current is negligible respects to the output current, it is clear that transforming 3 V into 1.5 V for example, the maximum efficiency is only 50%. While the unregulated voltage is about 1.8 V the efficiency increases to 83 %. For this reason linear regulator is preferable when the voltage conversion ratio is closely to 1.

As can be easily understood, switching regulator (Fig.3.6) performs the regulation activating one or more switches, in order to energize from the unregulated input voltage or de-energize into the load a storage element as capacitor or inductor.

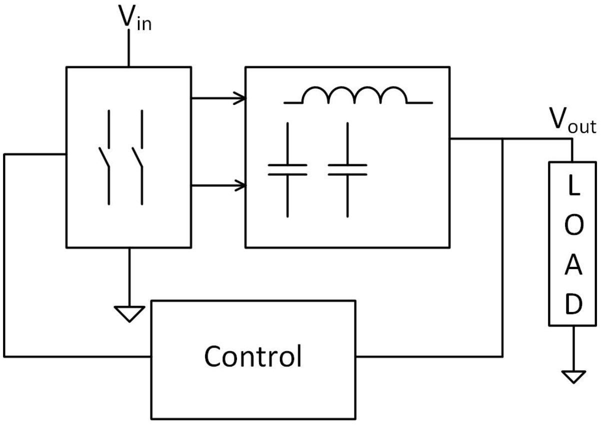

Figure 3.6 – Switching Regulator

Table 3.1 – Comparative switching regulator

	[LARG07]	[HHY+12]	[FF14]	[TSW+15]	[KBW12]
V$_{in}$ (v)	1,6-5,5	1,2-2,5	1,8	1,66	2,4
V$_{out}$ (V)	-	1	0,8-1,2	0,83	0,4-1,4
C$_L$ (μF)	10	4,7	0.0003	-	0.018 Flying Capacitor
L (μH)	47 off-chip	3.3 off-chip	20 10^{-3} Integrated	3D Interposer	10 10^{-3} Integrated
Frequency	37 KHz	-	588 MHz	150 MHz	50-200 MHz
Efficiency	0,84 - 0,88	0,61 - 0,95	0,6	0,82	0,72

The use of energy storage elements and switches permits to transfer the energy from input to output with almost no loss. In theory this makes the switching regulator more efficient than the linear one. In reality the efficiency is strongly dependent on the quality factor of the storage elements. As previously mentioned, integrating the passive elements particularly inductors in CMOS technology is a well-know challenge for the designer. The main reason is the poor quality factor due to the poor conductivity, high series resistance and thin metal layer. That translates in the increment in power loss on the parasitic resistance [LHVY07] (about 70% of power efficiency).

Switching regulators that achieve efficiency above 85% normally requires inductor in the order of 1-100 μH, making the integration not feasible for SoC applications. In [WH08], to attend high efficiency 77,9 % and small passive component 2 nH, a stacked interleaved topology is used. In [RGTSS12] the relationship between the frequency and the inductance is exploited to integrate the inductor (24 nH). But due to the increasing in switching loss with the frequency, the peak efficiency is 60% only. The table 3.1 shows that only for switching frequency in the range of hundreds MHz the inductor can be integrated, while higher power efficiency is achieved with off-chip inductor.

Another aspect that has to be considered is the noise content at the output voltage. The large size of the power switch and the switching behavior are all factors that have a negative impact on this characteristic. The situation is worsen in the case of monolithic switching converter, where high switching frequency is required to integrate the passive elements. Linear regulator for its part presents a low noise contents at the output. It is not rare that linear regulator is positioned after a switching one, since it is able to suppress the ripple and to provide a cleaner voltage supply at its output.

As mentioned previously a good regulator needs a fast response to the load changes. The fast response of the linear topology, in the order of 0.1-1 μs, is due to the simplicity of the feedback loop. This means an advantage in terms of time-to-design and so in terms of cost. Conversely, switching regulator suffers from a slow response. The fine control of the power switches normally requires clock generator, several digital blocks and other waveforms generator blocks depicted in Fig. 3.7. For example a design rule is that the Gain Bandwidth product (GBW) of the feedback loop should be kept limited within 1/5 or 1/10 of the converter switching frequency, to ensure that the switching noise does not increase. But unfortunately limiting the GBW of the control loop means a reduction of the transient response. It is clear that in terms of speed, switching regulator suffers from the complexity of the circuit and from the severals trade-off in terms of ripple/transient/stability/regulation.

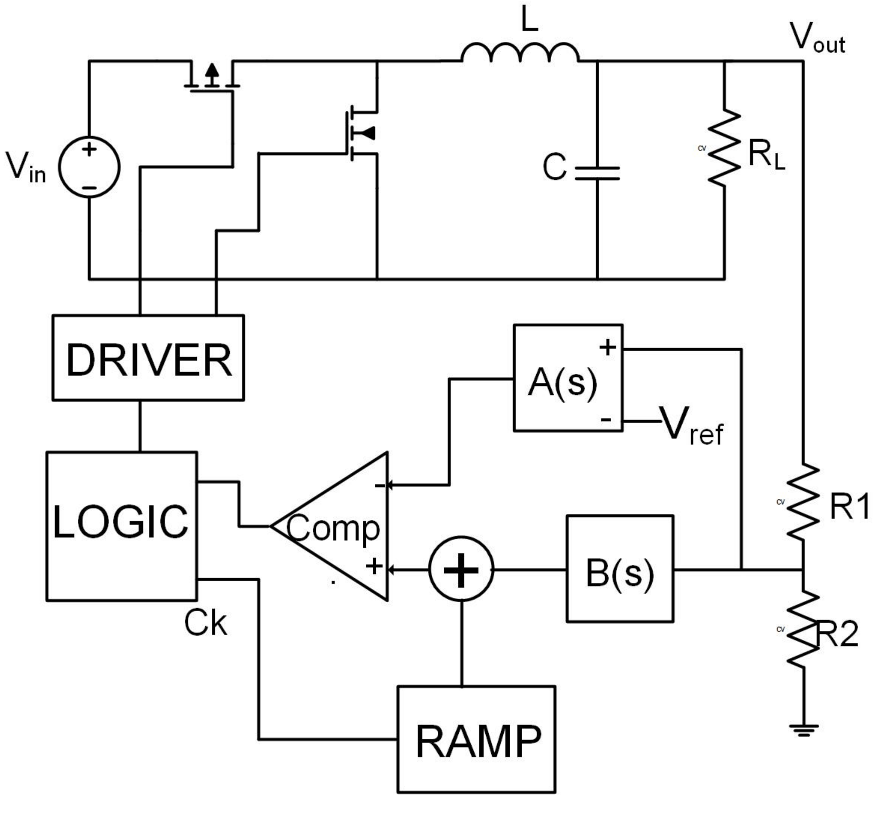

Figure 3.7 – Block Diagram of Buck Converter [WTM10]

There is no doubt that the most appropriate voltage regulator is linked to the application.

Starting from the power efficiency, the on-off behavior of switching regulator permits to extend the lifetime of device with higher capability to transfer the energy from input to output. The power efficiency represents a fundamental design criteria in such low energy system as in the case of RF harvesting source. But the needed of large inductor increases the chip cost.
Since the local oscillator (LO) in transmission block is powered by the voltage regulator the noise content at the output of the regulator has to be as lowest as possible, in order to not degrade the phase noise. Linear regulator exhibits better results than switching one. This latter presents indeed a switching output voltage ripple.

Using on-off modulation and moderated duty-cycle to ensure data transmission with lower energy per bit, the recover time has to be as short as possible to not waste power. Switching on-off the VCO or PA means changing in the load current of the regulator. Since the maximum peak-to-peak voltage of the transmission signal, therefore the output power transmission, depends on the supply voltage it is clear that the fasten response of the linear regulator allows to reduce the time slots where the power transmitted is not at optimal value. Therefore linear regulator with fasten transient response than switching one, optimizes the global efficiency of the whole system.
In conclusion the previously argumentations provide good reasons that the linear regulation is the most appropriated regulator for harvesting applications.

3.4 Low Drop-Out Regulator

Drop-out voltage is the difference between the unregulated input voltage and the regulated output one. As the power dissipated for the regulation is the product of the load current by the dropout voltage, it is mandatory to keep this value very low. As shown in Fig. 3.8 there are three different regions according to the input voltage value. In the linear region V_{out} can be regulated within the allowable dropout voltage with a determinate loop gain. When V_{DO} increases with decreasing V_{in} the output voltage deviates from its nominal value due to the lower loop gain. The pass transistor acts as switch and the regulator enters in dropout region. The V_{DO} is given by:

$$V_{DO} = r_{on} I_D \tag{3.6}$$

where r_{on} is the on-resistance of the pass transistor used as pass element and I_D its drain-source current. As V_{in} decreases further the regulator enters in off region. The headroom in not sufficient for the transistors to properly work and regulation property is lost.

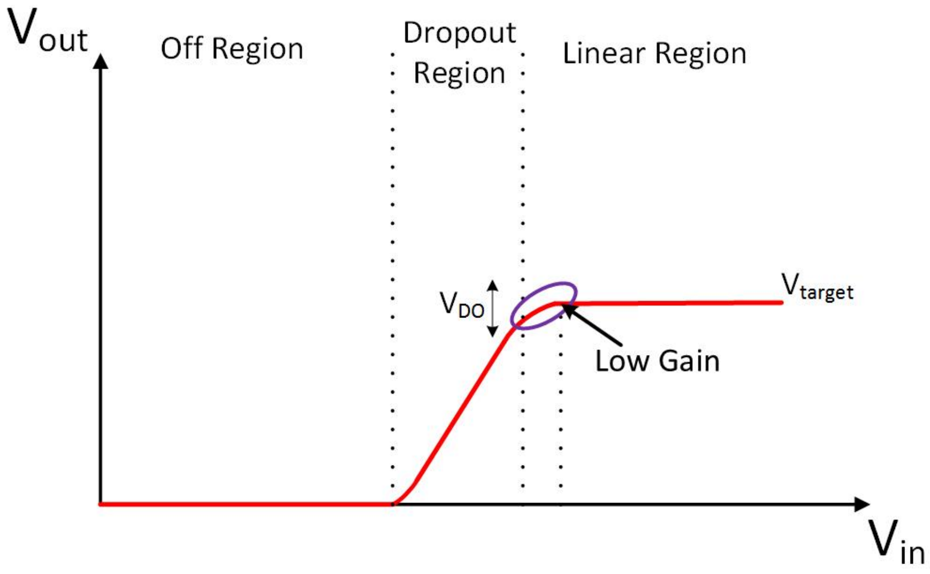

Figure 3.8 – Regulated output voltage versus input voltage.

The smallest amount of voltage drop between the pass element terminals splits linear regulators in two main categories: high drop-out and low drop-out.

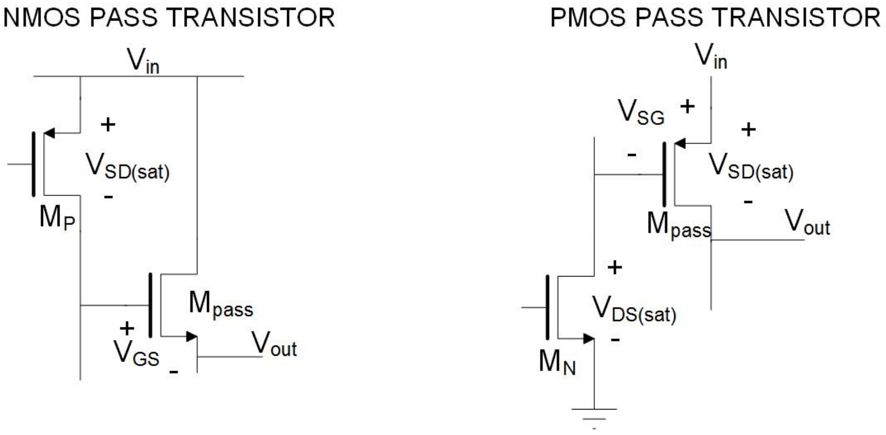

Figure 3.9 – N-type and P-type pass element

The Fig. 3.9 shows that the minimum drop voltage in the NMOS setup is the sum of the gate source voltage of the pass element V_{GS} and the minimum saturation voltage of its driver transistor V_{SD}. Depending on the technology node this value can exceed 0.7 V. In the case of PMOS setup the drop voltage is only the minimum overdrive voltage V_{SD} of the transistor. In modern technologies 0.2 V is a common value. Therefore PMOS transistor is the candidate for the voltage regulator, because as pointed out previously, the power efficiency is affected by the ratio between output and input voltage. However this statement remains valid as long as the output current is hundreds order of magnitude higher than the quiescent current. With very low dropout voltage achievable across the pass transistor, the current efficiency

$$\eta_c = \frac{I_{out}}{I_{out} + I_q} \tag{3.7}$$

is a more interesting specification and one of main design criterion for modern ULP LDO voltage regulator. Since the load current can vary of several orders of magnitude and that standby condition and light[2] load mode occurs most of the time in harvesting systems, current efficiency is an important factor to consider.

Basic LDO Architecture

To restore the output voltage when a variation of the load current appears at the output, the LDO topology requires a PMOS transistor M_p that acts as conversion element. In the case of output voltage variation, due a load requested current, the pass transistor supplies such current to regulate the output voltage V_{out} at the nominal value. Essentially the current that flows from input to output is modulated by a more or less conductive source-drain channel, by means of a lower or higher voltage applied to the gate of the PMOS. Therefore a control signal is needed to drive the gate of this transistor. In Fig 3.10 the classical representation of LDO regulator is depicted. The role of the error amplifier is to generate an error control voltage V_{EA} at its output, according to the difference between the scaled version of the output voltage V_{FB} and the reference voltage V_{REF}. The resistance divider, R_{F1} and R_{F2}, generates the voltage at the positive input of the error amplifier. Finally a capacitor C_L is placed at the output as charge storage element, mainly to tackle the sudden changes in the output load current.

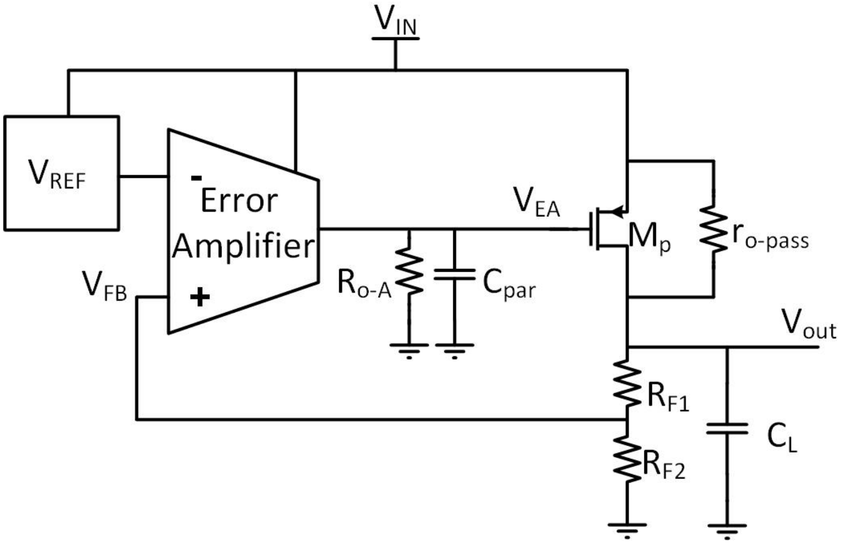

Figure 3.10 – Basic LDO Architecture

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[2] Condition where load current is at the lowest level

Transient response and design trade-off

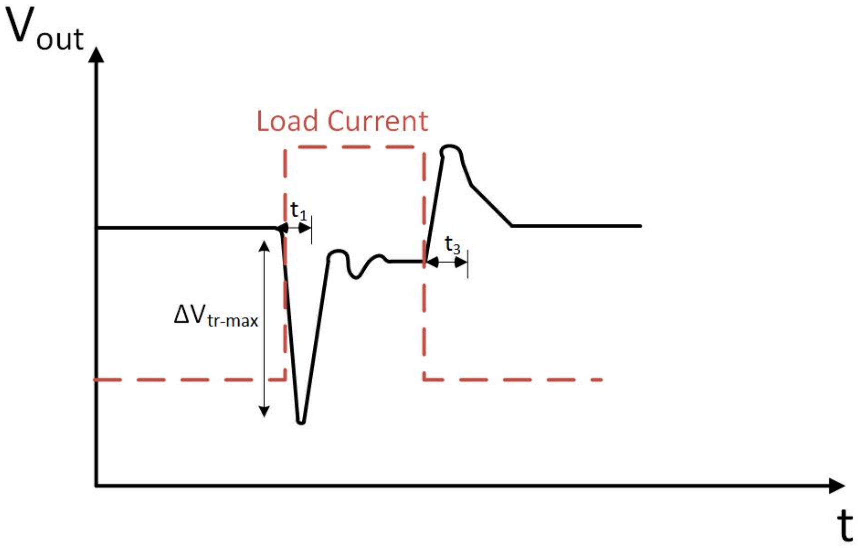


Figure 3.11 – Typical transient Response of LDO regulator

Voltage regulator is a dynamic system since it has to react to load current step, to limit the output voltage peaks and to bring it back to the nominal value in the shortest possible time. The Fig. 3.11 depicts the transient response when a load step appears at the output. When the load current changes from light condition to heavy condition, the pass device cannot immediately supply sufficient load current because the loop inertia, requires time to respond to this large current variation. Therefore, the output voltage experiences a voltage drop. The recover time t_1 depends on the closed-loop bandwidth BW_{cl} and the slew-rate of the error amplifier. The response time can be approximated using eq. 3.8, where t_{sr} is the slew-rate time needed to discharge the parasitic capacitance C$_{par}$ at the gate of PMOS pass transistor.

$$t_1 = \frac{1}{BW_{cl-1}} + t_{sr} \tag{3.8}$$

The closed loop bandwidth BW_{cl} is referred at light load. Similarly, in the case of a current change from heavy to light condition t_3 can be expressed by the eq. 3.9.

$$t_3 = \frac{1}{BW_{cl-3}} + t_{sr} \tag{3.9}$$

Thus, in case of light-to-heavy and heavy-to-light changes t_1 and t_3 are different, because the bandwidths under light and heavy conditions vary and the pass transistor delivers current that is either too low or too high, respectively, to the output load. It seems clearly that the output capacitor C_L acts as current buffer to balance the energy difference between input and output, as long as the pass transistor responds to the load change. That is, C_L delivers energy to the output before the V_{gs} of pass transistor is adjusted to an adequate voltage as show in Fig. 3.12. In the opposite case, the output capacitor can store the extra current from the pass transistor before it turns off to a suitable operation point (Fig 3.13). The maximum output voltage variation $\Delta V_{tr,max}$ can be expressed as

$$\Delta V_{tr,max} = \frac{I_{load1} - I_{load2}}{C_L} t_1 \tag{3.10}$$

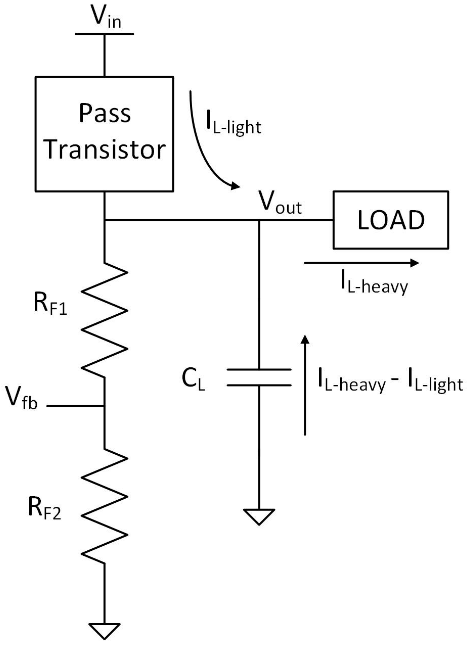


Figure 3.12 – Energy balancing from light to heavy step

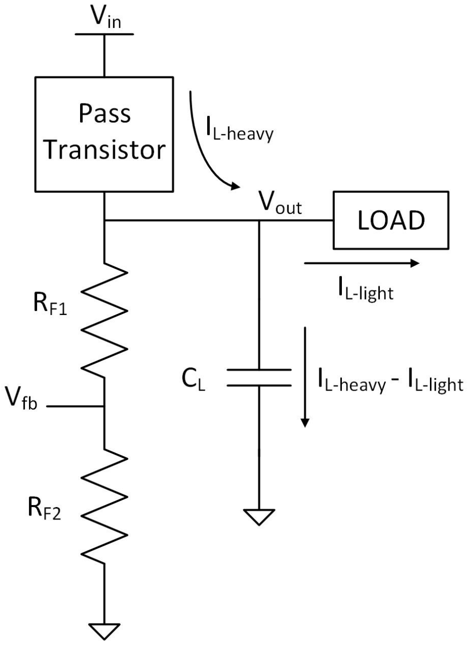


Figure 3.13 – Energy balancing from heavy to light step

Eq. 3.10 shows that a large capacitor limits the output voltage variations. The overshoot can be dissipated by the leakage current at the feedback divider resistor. However, the extra cost needed to provide a large area occupied for the output off-chip capacitor is not suited for the harvesting application. When a C-free[3] topology is applied, the way to compensate the degraded transient response is to reduce the recovering time $t_{1/3}$.
From the eq. 3.8 and eq. 3.9, it is clear that large bandwidth and high slew-rate performance of the error amplifier are mandatory to overcome the absence of large output capacitor. However it implies higher quiescent current, therefore lower current efficiency. In conclusion, a trade-off between speed and power consumption occurs, depending on the size of the output capacitor.

Frequency Response

As explained previously, the regulation is performed through a negative feedback loop. To properly process the signal, the loop has to remain stable for all load conditions. Figure 3.14 shows the linearized model of a LDO.

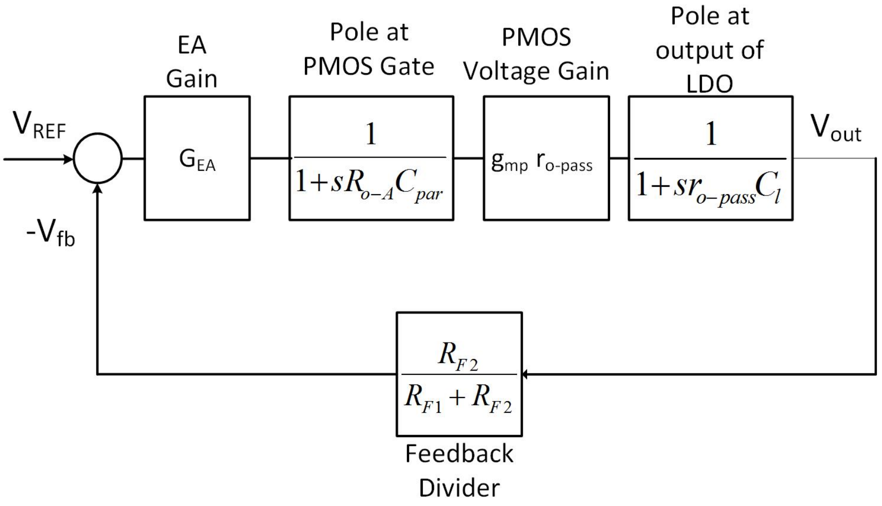


Figure 3.14 – LDO negative feedback diagram

From the Figure 3.14 the open loop gain is:

$$A_{ol}(s) = \frac{G_{EA}g_m r_{o-pass}}{(1+\frac{s}{\omega_0})(1+\frac{s}{\omega_1})} \tag{3.11}$$

---

[3] C-free or Capacitorless indicates a fully integrated topology. Normally for capacitor value in the range of 10-100 pF

where G_{EA} is the voltage gain of the error amplifier, g_{mp} and r_{o-pass} the transconductance and the drain source resistance of the PMOS pass element respectively. The two frequencies ω_0 and ω_1 are expressed as follow:

$$\omega_0 = \frac{1}{R_{0-A}C_{par}} \quad \omega_1 = \frac{1}{r_{o-pass}C_L} \tag{3.12}$$

The capacitance C_{par} is formed by the output parasitic capacitances of the error amplifier and the parasitic capacitance associated to the gate of the transistor M_p. Paying attention to the Miller effect between gate-drain of the PMOS due to its voltage gain, C$_{par}$ is not constant but it varies with the output current. The amount is given by C_{gdM}=$(1$+$g_m r_{o-pass})C_{gd}$.
It is well known from signal theory that a negative feedback loop is stable when:

$$A_{cl} = \frac{A_{ol}}{1+\beta A_{ol}} \quad |\beta A_{ol}| = 1 \quad PM(f_{0dB}) > -180° \tag{3.13}$$

The basic approach to make the feedback loop stable is to ensure a dominant single-pole frequency response. This means that the closed loop gain $A_{ol}\beta$ reaches unity gain frequency with a slope of -20 dB/dec, for example pushing the main pole at very lower frequency. Obviously, the pole frequency position sets the system bandwidth and how quickly the system responds accordingly. Therefore, the frequency response should be designed carefully not only for stability, but also for transient response. In the LDO C-free topology the two main poles are identified from the eq. 3.12 : one at the LDO output and the other at the gate of the pass transistor. Observing the eq. 3.11, the loop compensation is a quite hard task due to the poles movement with the load condition. The pole ω_1 moves with the r_{o-pass} variations therefore with the load current consequently. The pole ω_0 moves with the $g_{mp}r_{0-pass}$ product therefore with the square roots of the load current.

$$\omega_1 \alpha I_L \quad \omega_0 \alpha \sqrt{I_L} \tag{3.14}$$

As the load current can vary from several order of magnitude, the poles moves within of large frequency range. Moreover, the position of the two poles does not change proportionally.

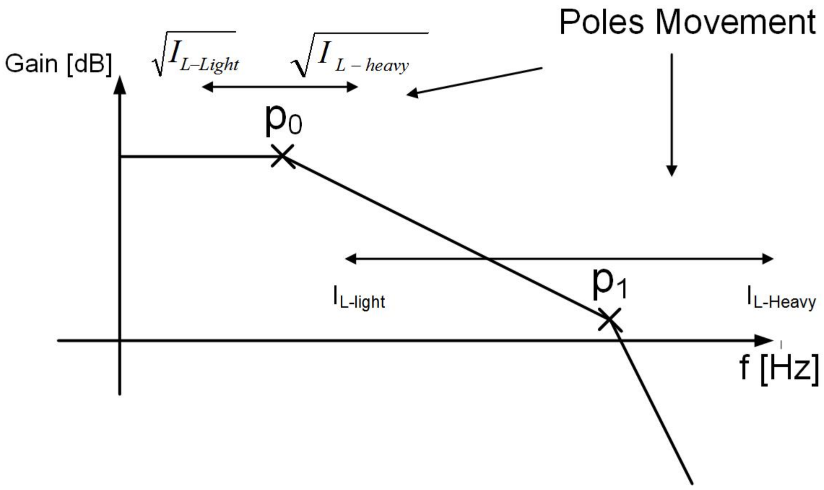


Figure 3.15 – Poles movement with load current

In conclusion the design of LDO voltage regulator demands several efforts to satisfy all specifications. For the purpose of the applications three main aspects were considered for the design:

— Current Efficiency: this is the most important design criteria considered for the regulator. The greater effort was done to keep high current efficiency especially for light load condition. As explained, the system spends most of time in stand-by or low power mode.

— Transient Response: Adaptable is the concept introduced to improve the SR of error amplifier and to extend the BW of the closed loop. Big load step current means higher quiescent current and vice-versa. Therefore, the bias current is adjusted dynamically with the load state.

— Frequency Response: the compensation strategy has to ensure the stability also for ultra-low stand-by current.

3.5 Design Implementation

From the previously done study it is evident that Capacitor-less LDO regulator is the best solution for our application. This section describes the techniques to improve the transient response. Moreover, the compensation strategy is also illustrated. The circuit is designed in a 130nm CMOS technology from STMicroelectronics

3.5.1 Output Target

To start the design of LDO regulator, it is needed to fix the load current boundaries. In fact, its maximum value sets the size of the pass element. The aspect ratio of M_p is fundamental, because the main performances of the regulator revolves around its characteristic. When the M_p supplies the maximum current, the dropout voltage is kept at low value if the transistor has large aspect ratio $S = \frac{W}{L}$ (W and L are the width and the length of the PMOS channel respectively). Once the minimum drop-out V_{DO} is chosen and thanks to the following equation

$$V_{DO} < r_{o-pass} I_{DS,triode} \tag{3.15}$$

where r_{o-pass} and $I_{DS,triode}$ are the drain-source resistance and the drain current when the transistor is on ohmic region respectively, the aspect ratio can be calculated as

$$\frac{W}{L} > \frac{2I_{Dmax}}{\mu_p C_{ox}(V_{inmin} - V_{th})^2 V_{DO}} \tag{3.16}$$

with μ_p the mobility of the carriers, C_{ox} the oxide capacitance , V_{th} the voltage threshold and V_{inmin} is the minimum unregulated input voltage assuming rail-to-rail voltage swing at the output of error amplifier. With the size of M_p it is possible to calculate the drain-source saturation voltage and therefore the input voltage boundary (V_{inB}=V_{out}+V_{sdsat}), when the pass transistor leaves the high gain region and starts to work in dropout region. From the well-known drain current equation of transistor in strong inversion:

$$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{SG} - V_{th})^2 \tag{3.17}$$

the saturation drain-source voltage is:

$$V_{sdsat} = \sqrt{\frac{2I_{Dmax}}{\mu_p C_{ox}\frac{W}{L}}} \tag{3.18}$$

Where I_{Dmax} represents the max load current. From the Eq. 3.18 with fixed drain current, the $V_{SDsat} = (V_{SG} - V_{th})$ decreases if the transistor has larger channel.

The first step to design the regulator is to fix the maximum load current. In the most published works the LDO regulator is characterized with a maximum current load in the range of 50-100 mA [GL10], [POSM14], [ZM11], [HM10]. That is a prohibitive value in harvesting application.

Given the simplicity of the sensor node architecture, it is easy to find that the transmission block is the hungriest part. In first approximation, the maximum load current can be approximated as the sum of the current drawn by the transmitter and an adequate safety margin. This latter is due to the supply current for other regulator load circuits (ADC, sensor, digital circuit). Therefore, a preliminary study about the recent ULP transmitter is mandatory, to better address the design flow of regulator. In [VHH+11b] a 2.4 GHz OOK transmitter with 0 dBm peak power and 10 Mbps data-rate draws 2.5 mA from 1V of V_{DD}. With a more sophisticated and precise frequency generation [TRE15b] to compensate the absence of PLL, the current consumption increases up to 6.8 mA. Ultra Wide Band impulse architecture approach [LCF09] shows that for very short distance, the current consumption decreases drastically under 1 mA.

To help with the design, different OOK transmitters topology have been realized and simulated. The detailed characteristics, and the design flow are presented in the next chapter. For sake of clarity the table Tab. 3.2 shows only their current consumption.

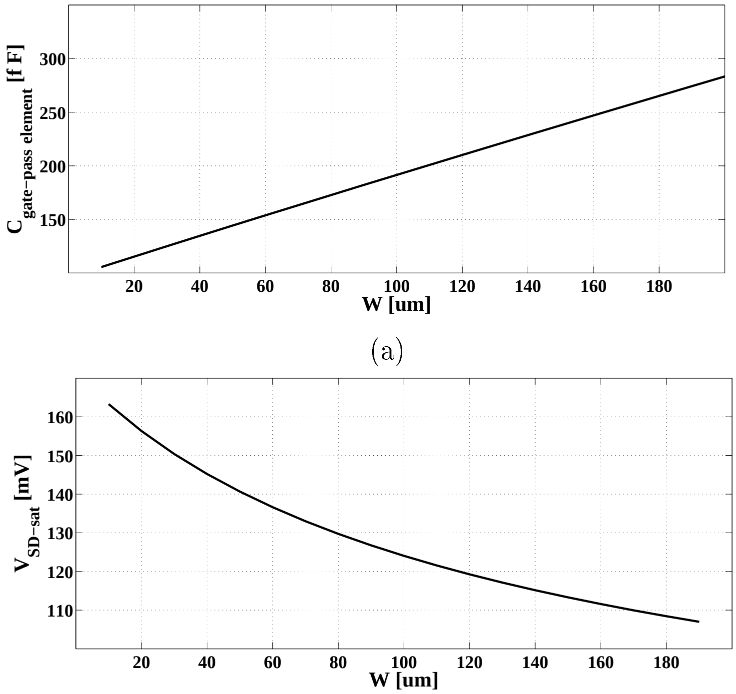
Table 3.2 – Current consumption of designed examples

Current	1^{st} Architecture	2^{nd} Architecture	3^{th} Architecture	4^{th} Architecture	5^{th} Architecture
I_{DC} (mA)	0.670	0.620	0.774	0.737	0.621

To obtain a 2.4 GHz carrier frequency with a peak output power of -15 dBm, the transmitter has to be supplied with an average current of 650 μA. Taking this value as the most important part of the load current and considering the extra current needed to the others circuits, the LDO is designed with a max load current of 1 mA.

However, some trade-off has to be considered before choosing the aspect ratio of Pass Element. In fact the parasitic gate capacitance of the PMOS increases with the size of the transistor. Larger gate capacitance demands better slew-rate performance. If the quiescent current of the error amplifier is not increased to avoid lower current efficiency, the regulator is affected by slower response. Therefore there is a trade-off between power consumption and speed.

With $I_{LOAD} = 1\text{mA}$ and $V_{DO} < 100\text{mV}$, the width of PMOS channel has to be greater than 22 μm (eq. 3.16). This value is obtained with the minimum gate length size L = 0.13 μm. With the aspect ratio of pass element the minimum V_{SDsat} is around 200mV, that gives a V_{inB}=1.2 V, considering $V_{out} = 1\text{V}$. To move the boundary towards values near V_{out}, the size of transistor has to be increased. Figure 3.16 shows the simulated trends of the parasitic gate capacitance and the saturated drain-source voltage of pass transistor for different W, for minimum length gate size.



(a)

(b)

Figure 3.16 – Parasitic gate capacitance C_g (a) and saturation drain-source volatage V_{sd-sat} (b) of the pass transistor for different width W

A width of 200 μm is chosen to improve the robustness of the regulator versus the input voltage variation. In fact as explained previously, this signal suffers from high fluctuations due to the incertitude of RF source. Therefore, decreasing the V_{sdsat} permits to extend the regulator linear region, where the pass element has the maximum gain. In addition also the efficiency is improved as V_{DO} decreases accordingly. But this results in larger parasitic gate capacitance and therefore in slower response.

3.5.2 Overcome current efficiency-transient response trade-off

As pointed out the transient response depends on the slew-rate (SR) performance of the error amplifier and on the bandwidth of the closed loop. In a simple amplifier the slew rate is given by

$$SR = \frac{I_{biasEA}}{C_L} \tag{3.19}$$

where C_L is the load capacitance seen at the output of the amplifier and I_{biasEA} is the bias current of the input differential pair of the error amplifier. Assuming the LDO regulator as a two stage amplifier, and supposing a Miller capacitor C_m to compensate the frequency response of the system, the gain-bandwidth product can be approximated as

$$\omega_{GBW} \approx \frac{G_{mEA}}{C_m} \propto I_{biasEA} \tag{3.20}$$

where G_{mEA} is the transconductance of the input differential pair. Eq. 3.19 and 3.20 show that high bias current is needed to improve the SR and to have large GBW product.

However, with a high and fixed value of bias current the efficiency is affected especially at light load condition. The problem can be circumnavigated if the regulator adapts its closed loop response with the variations of the load current. This translates in higher quiescent current when the LDO is a high load state and lower quiescent current when the output is at light load condition. In this way it is possible to reduce the impact of the regulator on the power budget. The two techniques implemented in this work to achieve this condition are: class AB Error Amplifier and adaptively bias Error Amplifier.

3.5.3 Slew-rate enhancement

Slew rate is the maximum voltage variation per time unit in a circuit node, due to the limited sink or source current. The SR of a circuit is limited by its slowest node: if the node is mostly made of a capacitance C, then the rate of voltage change across the capacitor is described by the well-known equation

$$\frac{dV}{dt} = \frac{I}{C} \tag{3.21}$$

If the current is limited at I_{max}, the maximum voltage change per time unit is

$$SR = max(\frac{dV}{dt}) = \frac{I_{max}}{C} \tag{3.22}$$

The SR can be positive or negative depending if the node sources or sinks the current. For each internal node of the error amplifier EA it is possible to associate capacitors. Clearly the large capacitance seen at the output of the EA limits its SR response and the speed of closed loop consequently. Eq. 3.22 indicates that the power consumption imposes a severe limit for the SR performance when the amplifier is designed to work as a conventional class-A Fig. 3.17

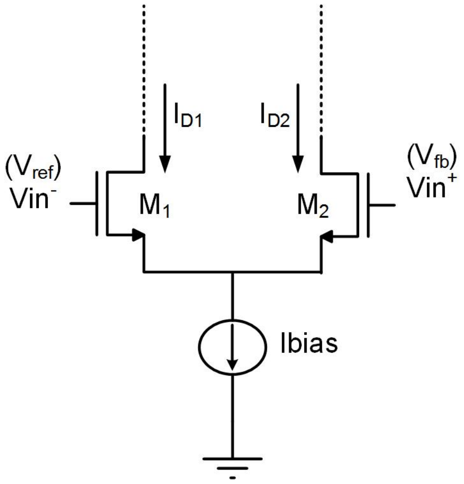


Figure 3.17 – Class-A bias topology

The problem can be circumnavigated if a class-AB EA is used. In [CS90] a self-biasing differential input pair that has a feedback loop allows to increase the quiescent current. Another way to enhance the SR performance is to add some extra circuit to improve the driving capability at the output of the amplifier [GMPP15]. However these approaches exhibit several limits in terms of bandwidth and occupied area. The circuit proposed in this work [LMBRAC05], uses a super class-AB OTA that breaks the trade-off between static power consumption and SR.

Class-AB Error Amplifier

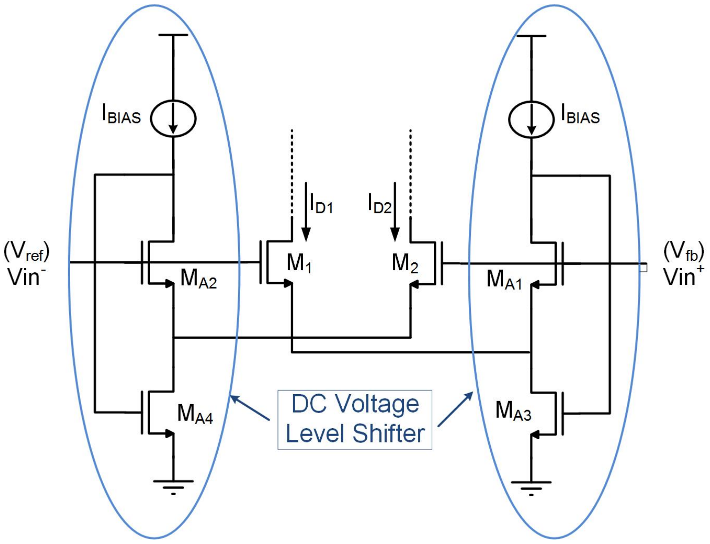


Figure 3.18 – Class-AB bias topology

The Fig. 3.18 depicts the class-AB amplifier core. The input differential pair M_1 and M_2 is cross coupled, at the source, with two flipped voltage follower (FVF) blocks that act as a dc voltage level shifters. At steady state when V_{diff}= V_{in^+}-V_{in^-} $= 0$ the circuit is biased at I_{bias} by the current source. When the system is unbalanced, one of the two transistors M_1 or M_2 experiences higher gate-source voltage, therefore more drain-source current than the other one. For example, if V_{in^+} increases and V_{in^-} is kept constant, the transistor M_2 has larger V_{GS} than the transistor M_1. The consequence is that the current I_{D2} is greater than I_{D1}. The great advantage of this configuration is that at steady-state condition the circuit can be biased with very low quiescent current. Only when the differential input voltage V_{diff}= V_{in^+}-V_{in^-} is not zero, the amplifier is able to supply more current at the output.

The adaptive biasing created by the two FVF cells has a positive impact on the SR performance of the amplifier. The large signal time response is no more limited by the quiescent current but depends on the unbalanced high input signal. Therefore the same benefits of class-AB amplifier can be integrated in LDO voltage regulator, improving current efficiency and transient response. In this case the negative input node of EA has a fixed voltage V_{ref} but the positive input senses the variation of the output voltage of the regulator. It is clear that, only in front of a load current step the EA responds with more current at its output, driving the pass transistor more quickly.

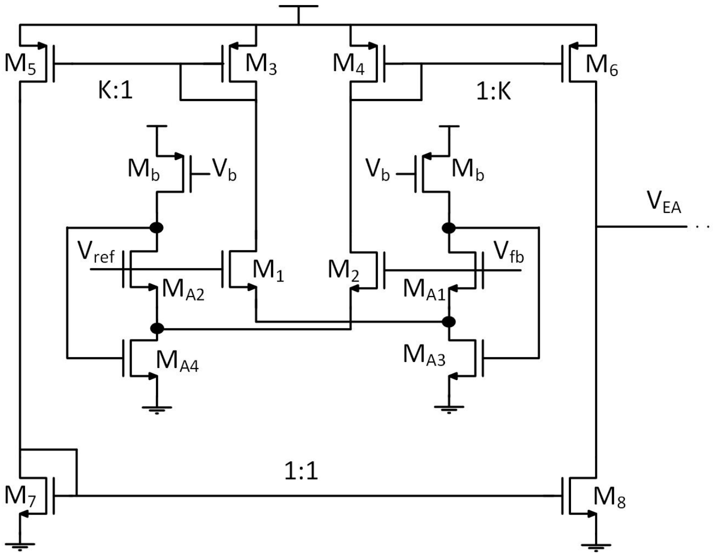


Figure 3.19 – Class AB error amplifier

A Current Mirror OTA depicted in Fig. 3.19 is used to implement the Error Amplifier. The pairs of transistors M_5-M_3, M_4-M_6 and M_7-M_8 act as current mirrors. Depending on the ratio (K) between the aspect ratio (S) of the transistors, this topology can presents high transconductance, large BW and high SR, however at cost of higher output noise and higher power consumption.

To get a first estimation of the total quiescent current of the EA, and its impact on the regulator performances, a minimum current efficiency of 60% was estimated for the output current of 1μA. Considering the quiescent current of 200 nA in the feedback resistors Fig. 3.13, this leads to a global allowed quiescent current for the error amplifier of around 200 nA. The amplifier is designed with the nominal unregulated input voltage of 1.2 V and each transistor M_b is designed to supply I_b=30 nA. In order to bias the transistor M_1 - M_2 and M_{A1} - M_{A2} with the same current, it is needed to set $S_1/S_{A1} = S_2/S_{A2}$ equal to 1. Therefore the total current consumption of the circuit is given by:

$$I_{qtotal} = I_b(4 + 2K) \tag{3.23}$$

To achieve the total current consumption of 180 nA, K is set to 1. In this low bias condition, all transistors operate in sub-threshold region and currents[4] drawing by M_1 and M_2 are given by

$$I_{D1} = I_{DO}\left(\frac{W}{L}\right)_{M1} \exp\left[\log\left(\frac{I_{DA1}}{I_{DO}\left(\frac{W}{L}\right)_{MA1}}\right) - V_{diff}\frac{1}{V_t n}\right] \tag{3.24a}$$

$$I_{D2} = I_{DO}\left(\frac{W}{L}\right)_{M2} \exp\left[\log\left(\frac{I_{DA2}}{I_{DO}\left(\frac{W}{L}\right)_{MA2}}\right) + V_{diff}\frac{1}{V_t n}\right] \tag{3.24b}$$

where I_{DO} is the technology current and it depends on the oxide capacitance, the substrate factor n and the carriers mobility μ_0 and V_T is the thermal voltage about 25 mV at room temperature.

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[4] Drain current equations of transistors M_1 and M_2 is obtained in Appendix

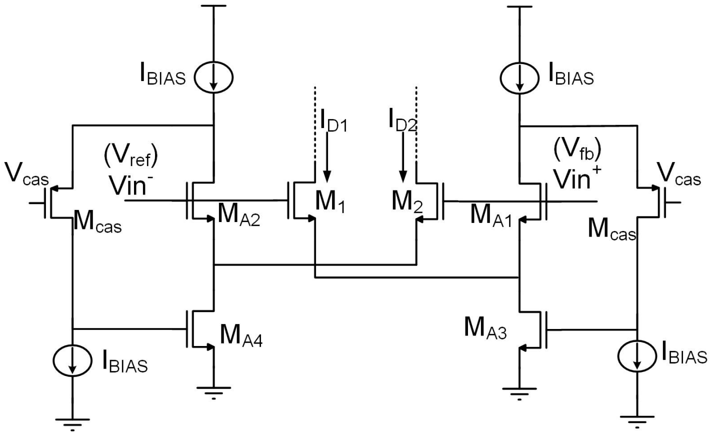
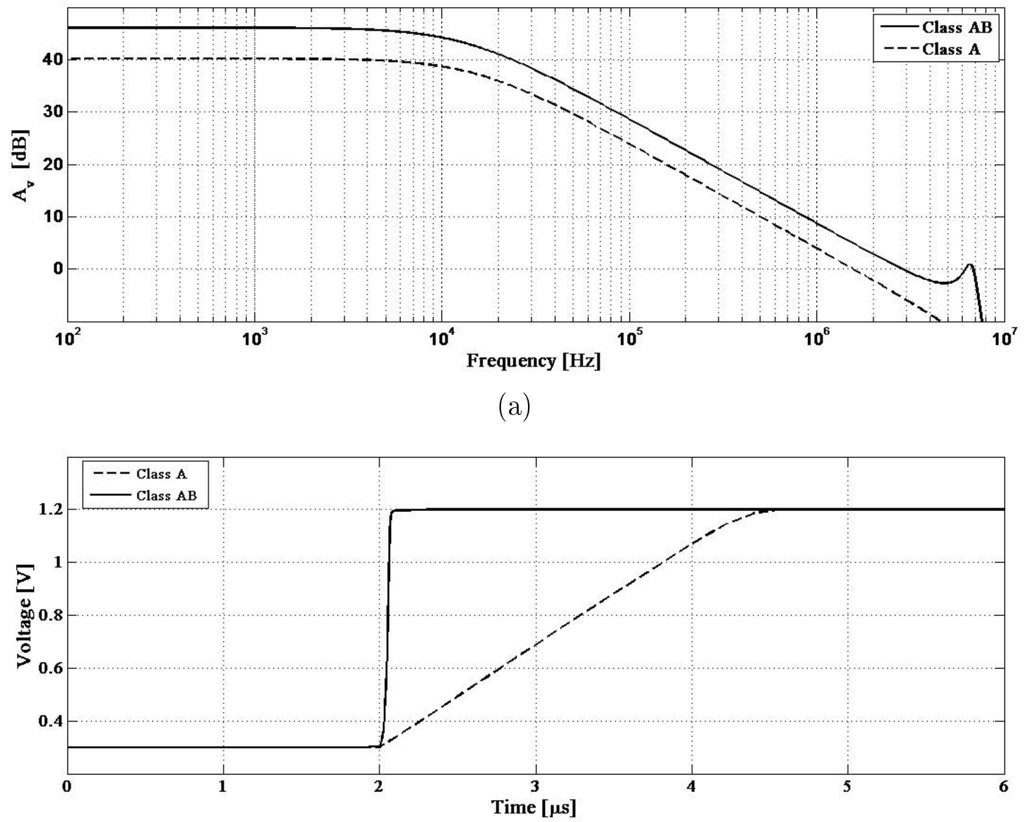


Figure 3.20 – FVF cell with cascode Pmos transistor

The above equations state that the drain current increases exponentially with the large input differential voltage. However to avoid large current process-voltage-temperature (PVT) variations due to the exponential characteristic in weak inversion, the aspect ratio of M_b and the voltage V_b are set in order to keep the transistor in strong inversion. It is worth noting that except M_b, all other transistors have to be oversized, because they experience more drain current than the 30 nA of current bias not only when the system is unbalanced, but also because the circuit provides extra bias current for the error amplifier proportional to the variations of the load current. Consequently transistors M_3-M_4 are much larger than M_b. Therefore the transistors M_{A1}-M_{A2} have lower V_{ds} than M_1-M_2. As a result the drain current is not the same. In order to re-equalize the circuit a PMOS cascoding transistor M_{cas} is inserted in the feedback loop of each FVF cell (Fig. 3.20). They provide a level shift proportional to the bias voltage V_{cas}. Therefore the maximum voltage at the drain of M_{A1}-M_{A2} during idle mode is approximatively $V_{cas}+V_{sgcas}$. With a correct setting of V_{cas} it is possible to re-balance the steady state drain current, however at the cost of extra power consumption.

The fig (3.21a) depicts the voltage gain of the class-AB and class-A for a I_b= 60nA. The simulation highlights that the DC gain and the unity-gain frequency in the case of class-AB are doubled compared to the class-A. The graph shows 46dB versus 40dB and 2.9 MHz versus 1.5 MHz. These results are explained by the fact that the differential ac input signal is applied to both the gate and the source of M_1 and M_2. Therefore the input signal sees a value of the transconductance double respect to the classical class-A topology. In the Fig. 3.21b the great advantage in term of Slew-Rate is more visible, due to the higher current delivered to the output thanks to the adaptively bias.



(a)

(b)

Figure 3.21 – Gain Voltage (a) and SR (b) simulation for I_b= 60 nA for Class-AB error amplifier in solid line and class-A dot line. The simulations are performed with C_L=350 fF.

3.5.4 Extended closed loop Bandwidth

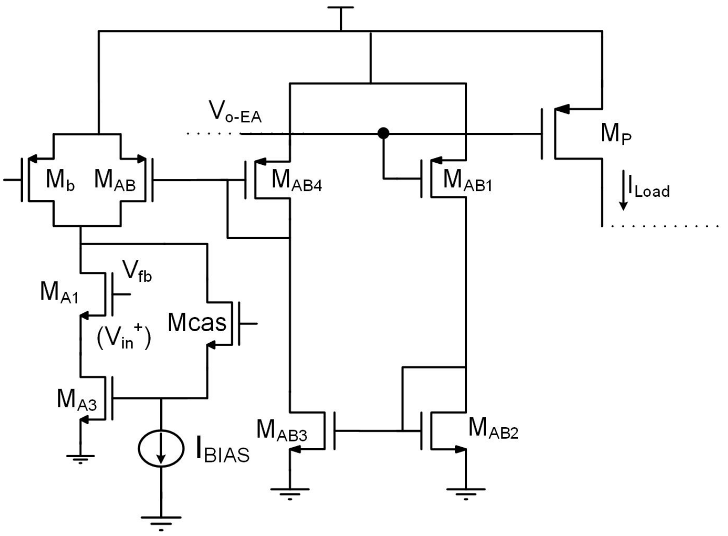


Figure 3.22 – Adaptive biasing system. The rest of the circuit is omitted for simplification purposes

The second design step concerns the implementation of the circuit to adapt the bias current of the error amplifier with the regulator load current. As explained previously, high bandwidth can be achieved with high quiescent current as indicated in Eq. 3.20. It is clear that the system is over-sized in terms of bias current when the output is at light condition. Since high transconductance is needed only for high value of the output current, adapting the g_m of the EA with the load current allows to reduce or to extend the bandwidth of the LDR regulator for the entire load range. Therefore a scaled version of the load current can be used for the I_{bias} of the Error Amplifier, through 3 current mirrors depicted in fig. 3.22. The first reduction is acted by the pair of transistors M_p/M_{AB1}, then the small replica of the load current is mirrored through the pairs M_{AB2}/M_{AB3} and M_{AB4}/M_{AB}. Therefore the bias current supplied by the transistor M$_{AB}$ is given by

$$I_{AB} = \frac{I_L}{mn} \tag{3.25}$$

where m is the scaled factor of the transistor M_{AB1} to the pass transistor M_p and n is the aspect ratio between M_{AB4} and M_{AB}. Considering that the transistors work in weak inversion for all load current range, the GBW product is proportional to

$$\omega_{GBW} \propto I_{bias} + I_{AB} \tag{3.26}$$

However the design of the adaptively biased LDO (AB-LDO) requires a careful study of the loop stability, therefore the two aspects have to be evaluated at the same time.

3.5.5 Compensation Strategy

As introduced in the section 3.4.1, to ensure the correct regulation the frequency response of the closed loop LDO has to respect the stability criteria. In literature are reported different techniques to accomplish this task. Q-reduction technique in [LML07] is used to control the Q of the non dominant pole to compensate the regulator at light load. For a multistage LDO regulator [GRF10] proposes a nested Miller Compensation with a current buffer, to move left-half plane zero towards high frequency. However the main drawbacks of these topologies is that they require big compensation capacitor and the stability is ensured for a well defined minimum load current value.

The Miller compensation strategy with current buffer [GPS12] is used in this work to ensure the stability for the entire load range. Miller capacitor is one of the techniques widely used to assure stable frequency response in a two stages amplifier. However, the well-known disadvantage of the LHP zero limits its strength, especially when a large capacitor is needed to achieve pole splitting effect. The purpose of current buffer is to alleviate the influence of the left-right plane (LHP) zero breaking the forward path created by the Miller capacitor. The frequency response of the voltage regulator can be associated with that of a two stages amplifier. Therefore the same technique can be implemented to compensate the circuit. However the stability is more complicated to achieve due to the load current large span. Respect to other approaches (nulling resistor, Voltage buffer, poe-zero cancellation), the current buffer allows to reduce the compensation capacitor value and not degrade the time response of the circuit [GPP08].

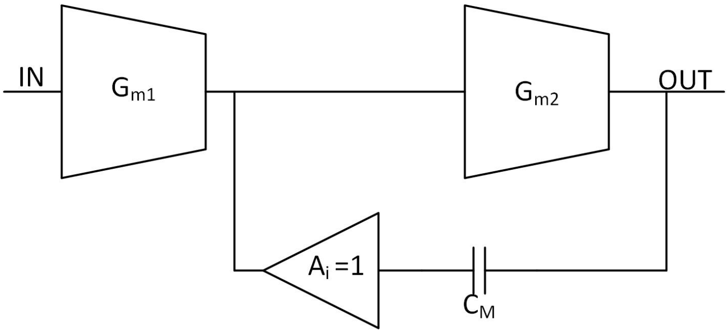


Figure 3.23 – Block Diagram of two stages amplifier with current buffer compensation technique

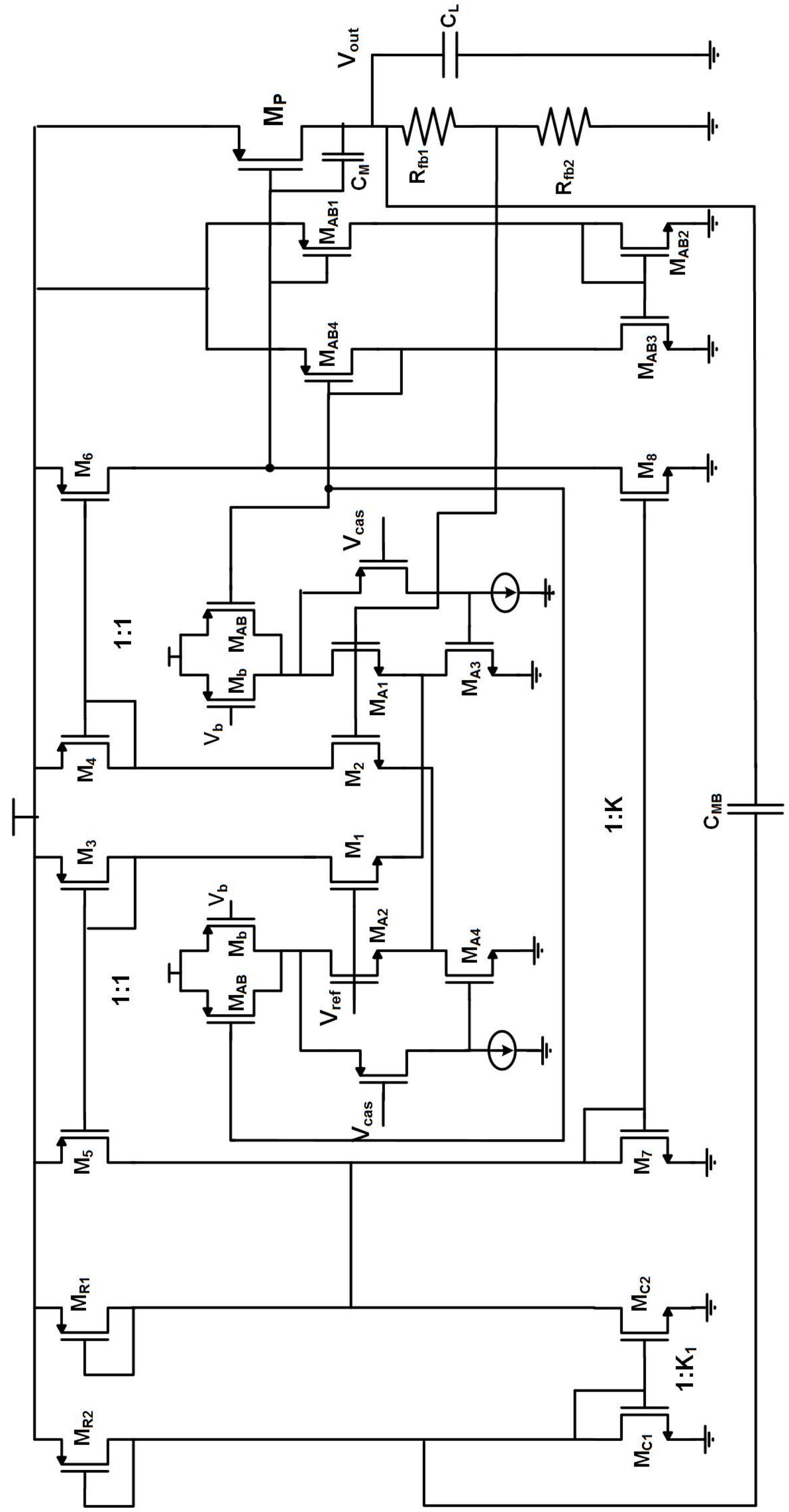


Figure 3.24 – Transistor level design of the LDO voltage regulator proposed in this work

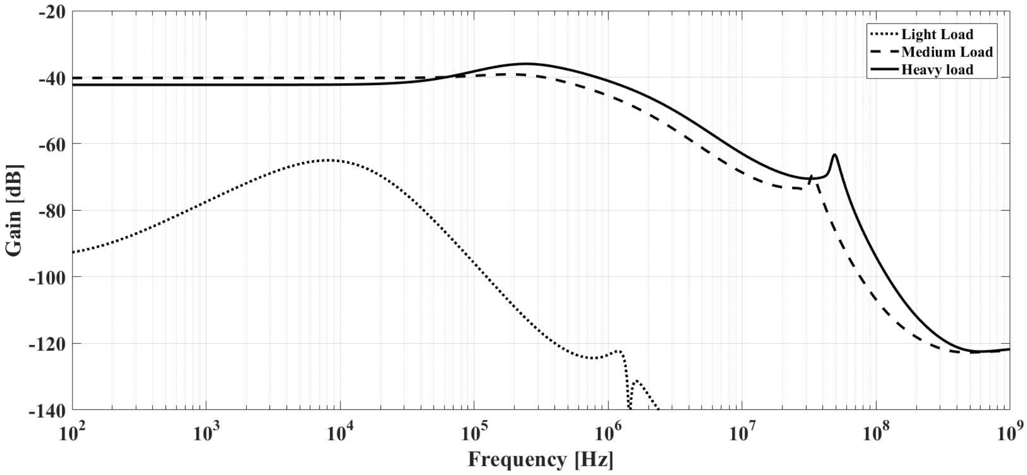


Figure 3.25 – AB loop gain for different load current

The Fig. 3.24 depicts the complete transistor level schematic of the LDO voltage regulator. It is possible to identify the pass transistor M_p, the error amplifier composed by M_1 up to M_8 transistors, the two class AB bias cells composed by M_{A1} up to M_{A4} with the fixed bias transistor M_b and the adaptively bias transistor M_{AB} and the adaptive biasing circuit formed by transistors M_{AB1} up to M_{AB4}. The compensation circuit is formed by the current buffer M_{R1}-M_{R2}/M_{C1}-M_{C2} and the compensation capacitors C_M and C_{MB}. The feedback resistance R_{fb1}-R_{fb2} are realized with a PMOS transistor to reduce the occupied area. The circuit is designed to supply 1 V with a maximum output current of 1mA. The unregulated input voltage range is (1.2-1.4)V. The voltage reference generated by an ultra low power sub-bandgap is 650 mV. The values of feedback resistors are 2.6 MΩ for R_{fb2} and 1.4 MΩ for R_{fb1}, which draw a ground current of 150 nA. One of the design trouble is that the large aspect ratio of the pass transistor imposes a minimum drain current to properly work. For example, if the load current is about 100 nA the transistor is in off-state and the regulation is lost. Therefore to provide the correct operation for the entire current load range the minimum drain current for M_p is provided by the ground current of the resistive network.

If we look closely to the circuit three loops can be identified. The most evident is the main loop needed to perform the regulation. The second is constituted by the AB network to control the bias condition of the EA. The last loop is inside the main loop and is related to the Miller capacitor and the current buffer. Therefore the LDO regulator has a stable response if the three loops respect the Phase Margin and Gain Margin criterion.
The stability of the AB circuit can be assured if the loop gain is always less than 0 dB. Breaking the loop at the gate of the M_{AB} (node at higher impedance), the loop gain is evaluated for the all load range current. The graphs in the Fig. 3.25 shows that the AB network is always stable at every load condition, since that the loop gain is well above 0 dB.

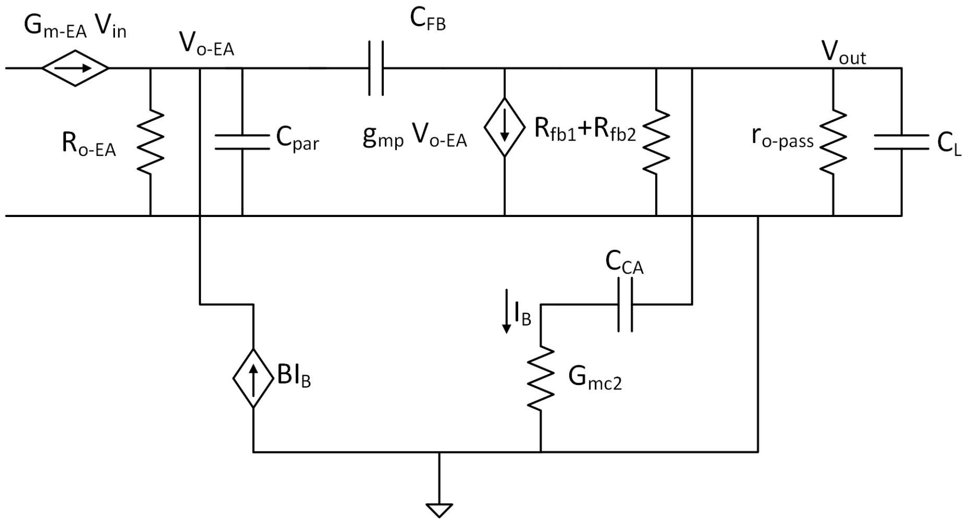


Figure 3.26 – LDO small-signal feedback representation

Once the stability of AB circuit is verified, the study of the frequency response can be related merely to the LDO voltage regulator and the compensation circuit. As introduced in [GPS12] when a buffer Miller compensation strategy is adopted the loop transfer function presents one dominant pole and a pair of complex and conjugate poles. The presence of the complex poles is due to the two nested loops. The open-loop transfer function is given by

$$T(s) = T(0)\frac{\left(1 - \frac{s}{Z_{LHP}}\right)\left(1 - \frac{s}{Z_{RHP}}\right)}{\left(1 - \frac{s}{p_d}\right)\left(1 + \frac{s}{GBW_I} + \frac{s^2}{GBW_I^2 K_{IN}}\right)} \tag{3.27}$$

where GBW_I is the gain-bandwidth product of the internal loop and K_{IN} is the separation factor of the internal loop. The DC gain T(0) is equal to

$$T(0) = G_{mEA} R_{o-EA} g_{mp} R_{out} \tag{3.28a}$$

$$R_{out} = r_{o-pass} || (R_{fb1} + R_{fb2}) \tag{3.28b}$$

the two zeros are

$$Z_{LHP} = \frac{-G_{Mc2}}{C_{MB}} \tag{3.29a}$$

$$Z_{RHP} = \frac{g_{mp}}{C_M + C_{gd-mp}} \tag{3.29b}$$

where G_{Mc2} is the transconductance of the current buffer, while the dominant pole is equal to

$$p_d = -\frac{1}{\left[g_{mp} R_{o-EA}(C_{MB} + C_{FB} + C_L)\right] R_{out}} \tag{3.30}$$

It is worth noting that the stability of the internal loop can be evaluated with the separation factor K

$$K \approx tan(\phi) \approx \frac{|p_2|}{GBW} \tag{3.31}$$

Where ϕ is the phase Margin and p_2 is the first non-dominant pole of the generic transfer function. The separation factor K_{IN} for the proposed voltage regulator is expressed by

$$K_{IN} = \frac{|p_{2IN}|}{GBW_I} = \frac{\left[C_L(C_{FB} + C_{gp})R_{o-EA} + \frac{C_{MB}}{G_{Mc2}}(C_{fb}g_{mp}R_{o-EA} + C_L)\right]^2}{\left[g_{mp}R_{o-EA}(C_{MB} + C_{FB}) + C_L\right] C_L C_{MB}(C_{FB} + C_{gp})\frac{R_{o-EA}}{G_{Mc2}}} \tag{3.32}$$

where p_{2IN} is the first non-dominant pole of the internal loop and $C_{FB} = C_M + C_{gdp}$. With K$_{IN}$=2 the PM = 65° and the system is stable with a small damping factor. The minimum acceptable PM of 50° is for K_{IN}=1.2. The same stability criteria can be adopted for the external loop. The separation factor K_{EX} in this case is related also to the gain-bandwidth product of the external loop

$$K_{EX} = \frac{GBW_{IN}}{GBW_{EX}} \tag{3.33a}$$

$$K_{EX} = \frac{\left[g_{mp}(C_{FB} + C_{MB})R_{o-EA} + C_L)\right]^2}{\left[C_L(C_{fb} + C_{gp})R_{o-EA} + \frac{C_{CM}}{G_{CA}}(C_{FB}g_{mp}R_{o-EA} + C_L)\right] G_{mEA}R_{o-EA}g_{mp}} \tag{3.33b}$$

Where GBW_{EX} is the gain-bandwidth product of the external loop. With a value greater than 1.5 for both separation factors the overall stability is achieved. Following the design methodology given in [GPS12] the design equations for the compensation circuit are

$$C_M = \frac{2C_{gp}}{n-1} - C_{gd} \tag{3.34}$$

$$C_{MB} = \frac{4 - K_{IN}}{BK_{IT}}\frac{2C_{gp}}{n-1} \tag{3.35}$$

$$G_{Mc2} = \frac{\frac{4-K_{IN}}{BK_{IN}}}{\frac{16}{K_{EX}K_I^2}\frac{1}{G_{m-EA}} - \frac{n^2-1}{4}\frac{C_L}{C_{gp}}\frac{1}{g_{mp}^{min}}} \tag{3.36}$$

$$n < \sqrt{\frac{64}{K_{EX}K_{IN}^2}\frac{C_{gp}}{C_L}\frac{g_{mp}^{min}}{G_{m-EA}} + 1} \tag{3.37}$$

Where $B = K_1K$ from Fig 3.24 and n is a scaling factor. Once the system is compensated the dominant pole and the second pole are expressed as

$$p_D = -\frac{1}{g_{mp}r_{o-pass}(BC_{MB} + C_{FB})R_{o-EA}} \tag{3.38a}$$

$$p_2 = -\frac{G_{mp}(BC_{CM} + C_{FB})}{C_L(C_{FB} + C_{gp}) + C_{MB}C_{FB}\frac{g_{mp}}{G_{CA}}} \tag{3.38b}$$

Some considerations have to be carried out about the two separation factors when an adaptively biasing topology is used. At first glance, it is clear that K_{IN} and K_{EX} are not constant for the entire load range. In fact both terms depend on the transconductance of the pass transistor g_{mp} and on the output resistance of the error amplifier R_{o-EA}. Moreover the impact of the transconductance of the EA G_{m-EA} on the stability requires a further study. From (Eq. 3.38a-3.38b) it seems that it does not have any influence on the frequency response of the regulator. However K_{EX} is linked to G_{m-EA} and this is included in the design equations (Eq. 3.36-3.37) for the compensation circuit. Given that G_{m-EA} changes with the load current, it is important to understand which value has to be chosen in order to calculate n and G_{Mc2}. Observing the equation of K_{EX}, the minimum value occurs when the transconductance of the error amplifier is at highest value. Therefore, assuming a Weak Inversion region for the entire load current range, the minimum of K_{EX} is at heavy load condition. In conclusion G_{m-EA}^{max} has to be used to design the compensation circuit.

So the study of K_{IN} and K_{EX} can be related to g_{mp} and R_{o-EA}. Limiting the adaptively bias current of EA, its output resistance does not change substantially. Therefore for the first approach, it is possible to consider that the stability depends largely on the pass transistor transconductance. To confirm this hypothesis, the (Fig. 3.27 3.28) show the trends of K_{IN} and K_{EX} with the g_{mp} and R_{o-EA}.

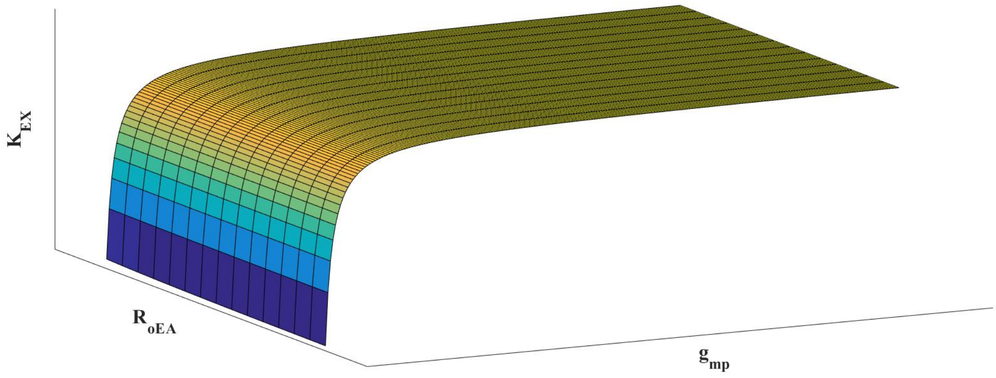


Figure 3.27 – K_{EX} for different values of R_{o-EA} and g_{mp}. The minimum value of separation factor is for light load condition. R_{o-EA} has negligible impact.

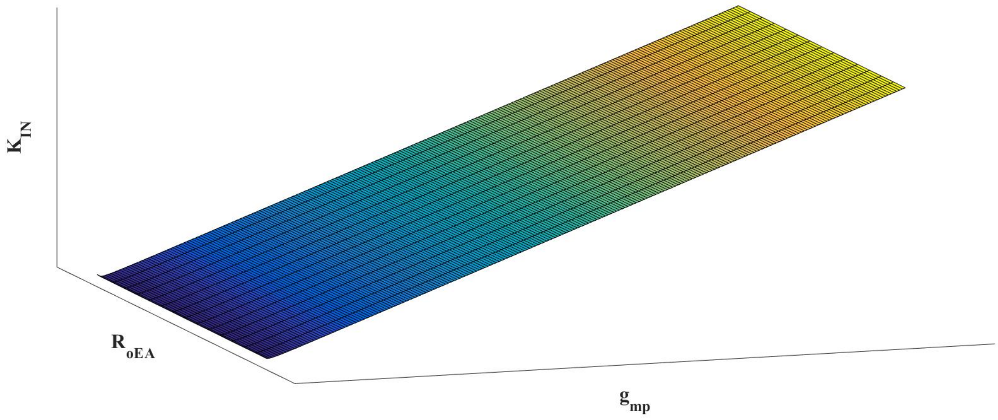


Figure 3.28 – K_{IN} for different values of R_{o-EA} and g_{mp}. The minimum value of separation factor is for light load condition.Also in this case R_{o-EA} has negligible impact.

3.5.6 Transistor Level Design

Once the design equations are established and with the constraints dictated by the application, the design steps of the proposed LDO regulator can be as follow

- achieve high current efficiency ($> 99\%$) from moderate to heavy load. Considering the 300 μA as the moderate load condition the total quiescent current of regulator has to be less than $< 3\mu$A. Being the EA the most power hungry block it is possible to estimate the maximum bias current. With the aim of Eq. 3.23 the I_{AB}^{max} is

$$I_{AB}^{max} = \frac{I_q}{6} - I_b \tag{3.39}$$

  Assuming 60% of the total quiescent current, thus extending the efficiency below the moderate load, $I_{AB}^{max} \approx 200$nA.
- With Eq. 3.25 and with the above value, the scaling factors product mn is about 5000.
- Once all bias condition established, it is possible to calculate the compensation elements Eq. (3.34-3.37). Therefore, setting $I_L^{min} = 300$ nA and $I_{AB}^{max} = 200$nA, the related transconductances are $g_{mp}^{min} = 8{,}78\mu$S and $G_{mEA}^{max} = 6\mu$S. The minimum load current is stated to stand-by mode. K_{IN} and K_{EX} are both set equal to 1.8 to achieve a minimum phase margin of 60°. The output capacitor is 20pF. The parasitic gate capacitance of the pass transistor is about 200 fF. The buffer current gain is B = 1 in order to save the power consumption. The accepted trade-off is a larger occupied areas due to a higher value of the required compensation capacitors. The obtained values are $C_M = 2$pF, $C_{MB} = 3.3$ pF and $G_{Mc2} = 2.5$ μS.

The Fig. 3.29 shows the increasing of I_{AB} with the I_{Load}. The Fig. (3.30-3.31) show the benefits of AB circuit, where the current efficiency is kept above 99% when the load current is higher than 300 μA, while for low load current the system ensures a good value around 70%. At the same time, the GBW of the loop moves from 40 kHz when the output is under light condition, to around 360 kHz under heavy condition, improving the regulator transient response.

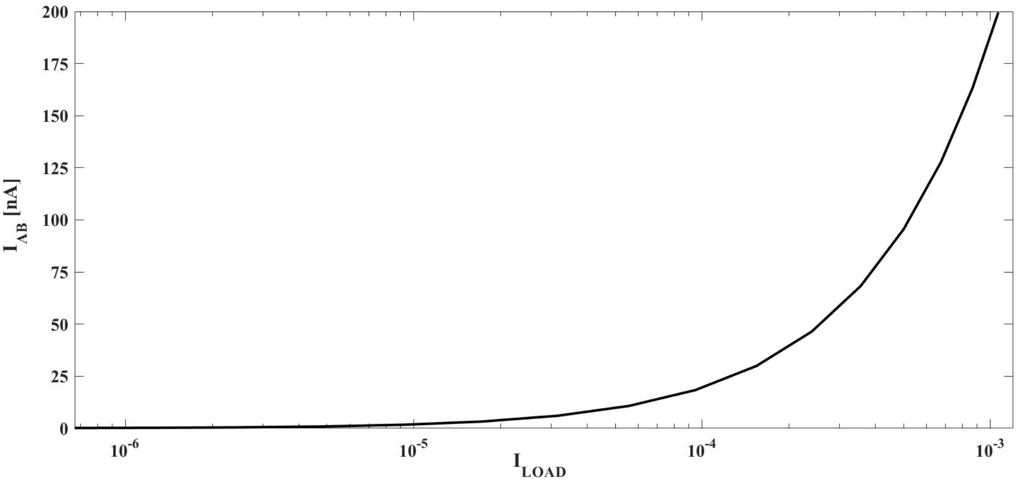


Figure 3.29 – The trend of the bias current adaptability versus the load current.

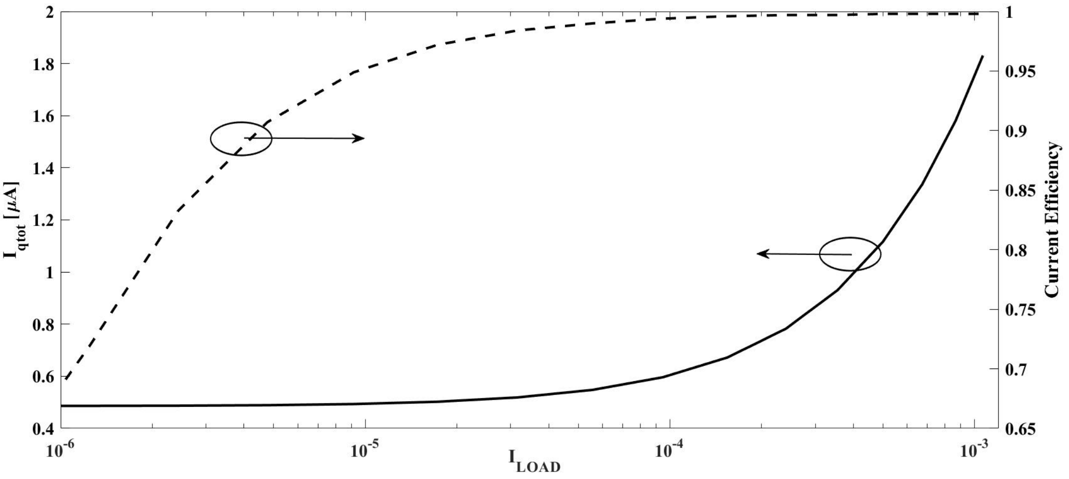
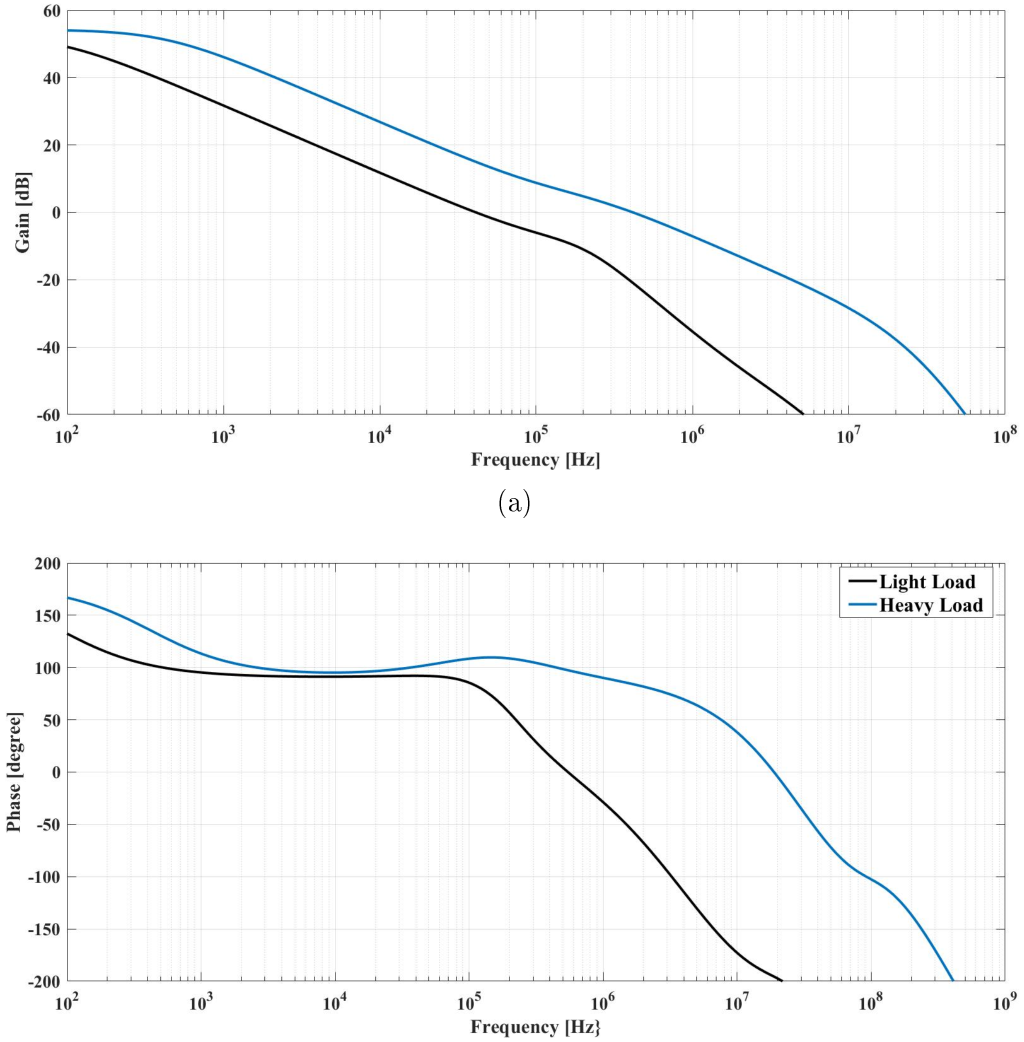


Figure 3.30 – LDO quiescent current and current efficiency versus load current. In this case the trend is shown only for operation mode (I_{Load}= 1 μA-1 mA). For stand-by mode the current efficiency is worsen by the minimum drain current needed to keep ON the pass transistor.



(a)

(b)

Figure 3.31 – (a) Open loop gain for $I_{Load} = 1\ \mu$A (black line) and for $I_{Load} = 1$ mA (blue line). It is evident the GBW product is increased at heavy load condition due to higher G_{mEA}. GBW extends from 40 kHz to 360 kHz (b) Phase for the two load conditions.

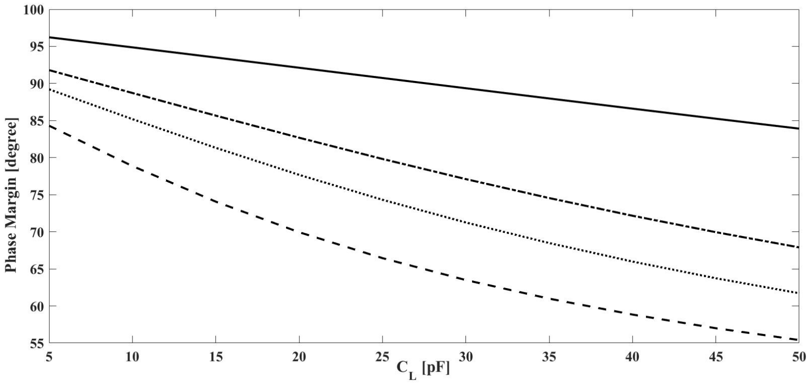


Figure 3.32 – Phase margin versus output capacitor value, for different stand-by output current values. From $I_L^{stand-by} = 205$ nA (dash line) to $I_L^{operation-mode} = 1$ μA (solid line).

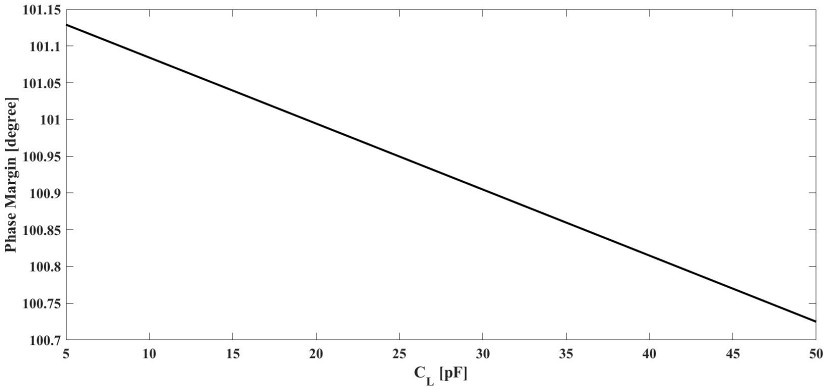


Figure 3.33 – Phase margin versus output capacitor value at heavy load condition

Generally, depending on the fabrication technology, the output capacitor can be integrated for values up to 100 pF. As previously explained, higher value allows to respond more quickly to current demand in the case of low to high step, because it acts as charge supply. However the frequency response and the stability are largely affected by the value of this output capacitor. With the compensation topology adopted in this circuit there is a trade-off between the minimum Phase Margin achievable under stand-by condition and the value of output capacitor. Fig. 3.32 shows that the phase margin is inversely proportional to the value of C_L. For example for the designed circuit the stand-by output current is 250 nA (dashed line) and the output capacitor value is 20 pF, thenthe PM achieved is about 70°. Therefore if C_L is replaced by a larger capacitor of 50 pF to reduce the output voltage spike, the minimum stand-by current has to be increased, to about 800 nA (dash-point line), to achieve the same PM of 70°. Fig. 3.33 shows that heavy load condition the output capacitor has no impact on the phase margin. A minimum phase margin of 90° (Fig. 3.34) is achieved in operating range assuring a stable regulation also with a light load.

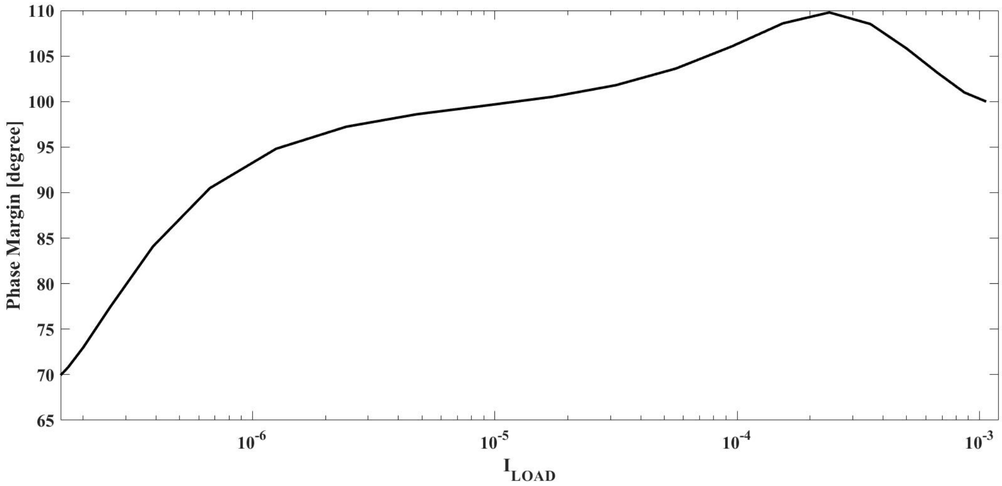


Figure 3.34 – Phase margin versus output current for all operating regions.

Error Amplifier The transistors sizes of the error amplifier are chosen with the aid of the inversion coefficient IC [5]

$$IC = \frac{I_D}{\left(\frac{W}{L}\right) I_0} \tag{3.40}$$

For the MOS technology used in this work, the technology current I_0=0.63 μA for N-channel transistor and I_0=0.187 μA for P-channel transistor. The other two design parameters are the drain current and the channel length. Since the drain current is fixed by the application, the size is related to the choice of the IC and the channel length to calculate the width of transistor. All transistors work at low side of the moderate inversion. This is an accepted trade-off between transconductance-current efficiency and frequency response. Moreover in this region the transistor achieves high power efficiency and low voltage bias. Therefore the range of IC considered for the design is between 0.1 and 0.5. Minimum channel length is avoided for all transistors in order to make the circuit more robust against V_{gs} and V_{th} mismatch. Moreover longer channel transistor operating at low side of Moderate Inversion exacerbates frequency response. Therefore a L = 0.7 μm for all transistors is chosen to limit the parasitic capacitance associated to the internal node of the circuit.

- The bias transistor M_b as previously introduced is the only device that operates in strong inversion. With a drain current of 30 nA this operation mode is possible because the gate voltage is externally driven. The channel width is 0.35 μm.
- The input signal transistors M_1-M_2 and M_{A1}-M_{A2} are sized with an IC = 0.3, to limit drain current mismatch due to threshold voltage variations. Assuming an higher drain current dictated by the class-AB operation ($\approx$ 500nA) the resulting W is equal to 1.8 μm. The final value is decreased to 1.4 μm to accomplish layout techniques as common centroid or interdigitized topologies.
- The two sink transistors M_{A3}-M_{A4} have to support twice the drain current than the input signal transistor. This leads to W = 2.8 μm.
- For the PMOS current mirror transistors M_3 to M_6 the main trade-off is between the drain current mismatch and the DC gain of the Error Amplifier. Therefore, with IC = 0.5 the W equals 3.5 μm.
- The same design criteria is adopted for NMOS sink current mirror M_7-M_8. This leads to W = 1.4 μm.
- The PMOS cascode transistor is designed to have a V_{sg} = 200mV. With a drain current of only 2 nA, the transistor has to operate in deep Weak inversion. Therefore for IC = 0.01 W equals 0.7 μm

Adaptively Bias Circuit The adaptively bias circuit is designed to transfer a scaled version of load current with a scaled factor of 5000. Moreover it is designed to be completely off at light load condition. In order to draw a low quiescent current the factor n $\approx$ 10000. Therefore the total quiescent current for the circuit at heavy load is about 140 nA, where each branch draws 70 nA. The aspect ratio of the transistors are: $S_{M_{AB1}} = (\frac{0.4}{4})$, $S_{M_{AB2}-M_{AB3}} = (\frac{0.7}{7})$ and $S_{M_{AB4}} = (\frac{2.8}{0.7})$. Finally to achieve the desired scaling factor m = 1/2, the aspect ratio of $S_{M_{AB}}$ equals $(\frac{5.6}{0.7})$.

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[5] Introduced in chapter one.

Current Buffer The current buffer is designed to present a transconductance of 2.5 μS to compensate the feedback loop. At weak inversion the equivalent current is about 80 nA. With a L = 0.7 μm and a IC = 0.1, the width of channel is W = 1.4 μm. The current mirror is designed to have B = 1, so the two transistors have the same aspect ratio of $S_{MC1-MC2} = (\frac{1.4}{0.7})$.

3.6 Voltage Reference

Most of the time, nominal operation conditions of electronics devices can change due to extreme variation of environment property or to external interference. Especially temperature is one of the main factor, since that many of transistor parameters are temperature-dependent. The main goal of voltage reference is to generate a stable voltage independent to supply voltage and temperature. An independent supply voltage circuit means that once the equilibrium point is reached the bias condition does not change with the supply voltage. However to eliminate the thermal dependence, it is needed to create two quantities (voltage or current) exhibiting an opposite trend with the temperature.
The three main aspects to be evaluated to quantify the robustness of a voltage reference are: temperature coefficient, power supply rejection ratio PSRR and the minimum supply voltage.

Temperature Coefficient

The temperature coefficient quantifies the output voltage variations respect to the temperature.

$$TC_{eff} = \frac{1}{V_{ref-nom}} \left(\frac{V_{ref-max} - V_{ref-min}}{T_{max} - T_{min}} \right) \tag{3.41}$$

where $V_{ref-nom}$, $V_{ref-max}$ and $V_{ref-min}$ are the output reference voltages at room nominal maximum and minimum temperatures.

PSRR

It is a small-signal characteristic and indicates the capability of voltage reference to suppress the voltage ripple coming from the voltage supply

$$PSRR = 20log \left(\frac{\delta V_{ref}}{\delta V_{DD}} \right) \tag{3.42}$$

where δV_{ref} is the ripple of the output voltage.

Minimum Supply Voltage

The minimum supply voltage is the value from which the output voltage reference is constant. Normally it is measured at room temperature.

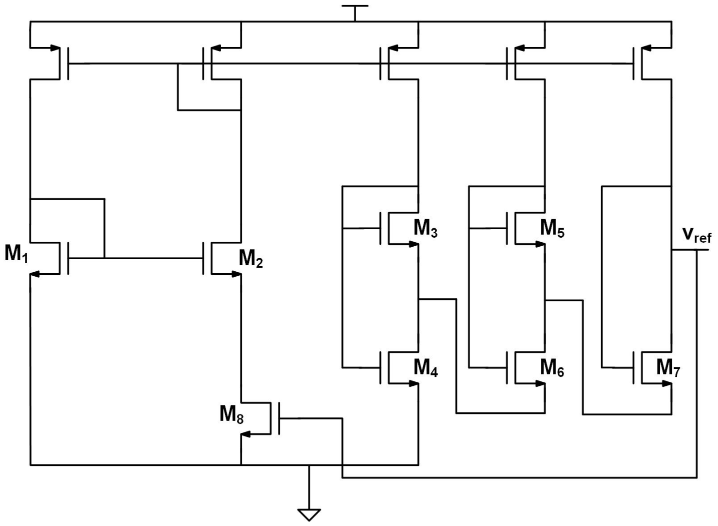


Figure 3.35 – Ueno voltage reference

State of the Art

Ueno Voltage Reference The circuit proposed in [UHAA09] (Fig. 3.35) generates the voltage reference with all transistors in Weak Inversion (WI), excepted the transistor M_8 that acts as resistor being in triode region under Strong Inversion condition. As explained the voltage reference has to be supply independent; in this case the transistors M_1-M_2 and M_8 with the two relative mirror current PMOS transistors generate the current in a self-bias way. This current is then mirrored in the other three branches. The output voltage reference is then equal to

$$V_{ref} = V_{ds7} + V_{ds6} + V_{ds4} = V_{gs7} + V_{gs6} - Vgs5 + V_{gs4} - Vgs3 \tag{3.43}$$

As the transistors work in WI, the Eq. 3.43 can be rearranged as

$$V_{ref} = V_{gs4} + nV_t ln\left(\frac{S_5 S_3}{S_6 S_7}\right) \tag{3.44}$$

Eq. 3.44 shows that a V_{ref} independent from the temperature can be obtained if the two temperature coefficients of the two terms on right side of the equation are opposite. This circuit offers the advantage of eliminating resistors that for nanopower circuits assume high values and therefore large silicon area.

De Vita Voltage Reference To accomplish the main task of voltage reference, in [VI07] the temperature dependence of electrons mobility is eliminated.

The transistors M_1 and M_7 (Fig. 3.36) have gate oxide thicker than the others so higher threshold voltage. In this way the transistors M_1-M_7 and M_2-M$_8$ are biased in WI and SI respectively. The current I_0 generated in the load M_9 is proportional to the square of thermal voltage and the carrier mobility

$$I_0 = \frac{\mu C_{ox} S_8}{2\left(\sqrt{\frac{S_8}{S_2}} - 1\right)^2} \eta^2 {V_t}^2 ln^2\left(\frac{S_7}{S_1}\right) \tag{3.45}$$

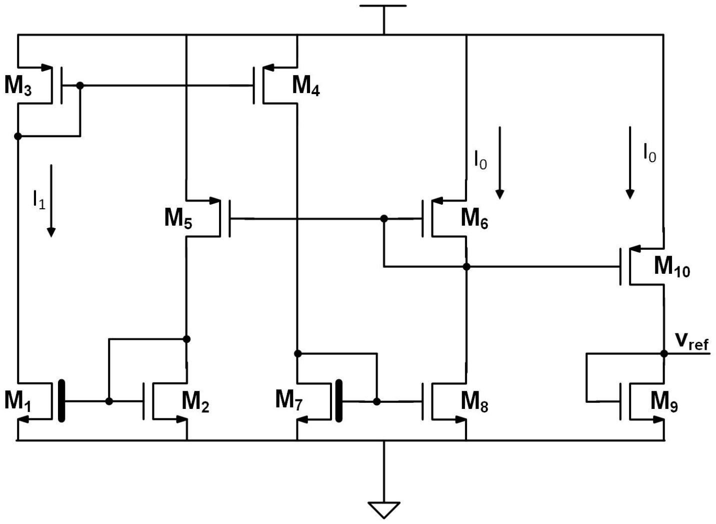


Figure 3.36 – De Vita voltage reference

Since the load transistor is a diode connected in saturation region under SI conditions, the output voltage reference is given by

$$V_{ref} = V_{th10} + \frac{\eta V_t}{\left(\sqrt{\frac{S_8}{S_2}} - 1\right)} \sqrt{\frac{S_8}{S_9}} ln\left(\frac{S_7}{S_1}\right) \tag{3.46}$$

Adjusting the aspect ratio of transistor involved in the Eq. 3.46 the temperature dependence of the output voltage reference can be eliminated.

Bandgap Voltage Reference Normally the use of bipolar transistor as current reference in the circuit makes the output voltage equal to the bandgap voltage of the silicon ($\approx$ 1.12 V).

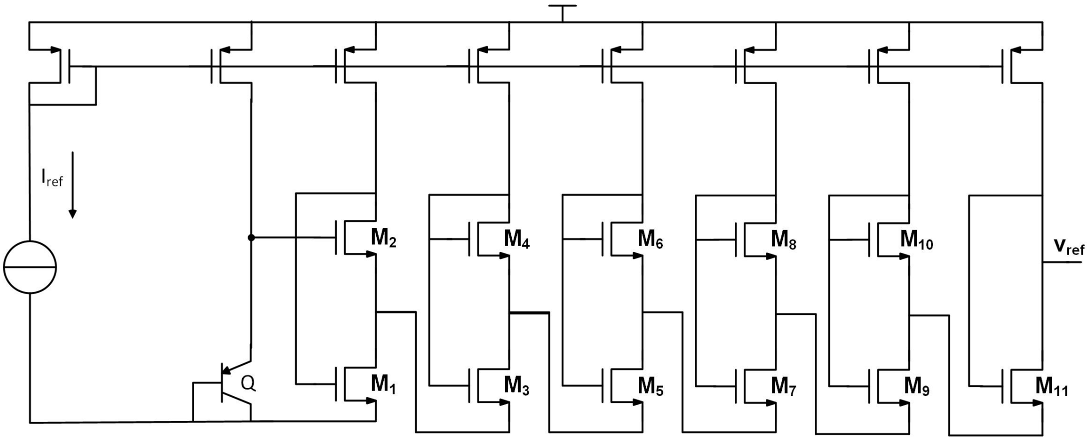


Figure 3.37 – Bandgap Voltage reference proposed in [HUKN10]

The output voltage reference generated by the circuit is given by

$$V_{ref} = V_{BG} + \left(\psi_{V_{be},T} + \sum_{i=0}^{5} V_t ln\left(\frac{S_{2i}}{S_{2i-1}}\right)\right) \tag{3.47}$$

where V_{be} is the silicon bandgap voltage, $\psi_{V_{be},T}$ is the temperature coefficient of base-emitter voltage. Choosing a correct aspect ratio of the involved transistors, the second term in the right side of the equation can be reduced to zero.

In conclusion all the introduced circuits share different aspects:

— To eliminate the temperature dependence 2 quantities are needed: one that has a negative temperature coefficient CTAT (complementary to absolute temperature), that can be generated by a voltage or a current. The other has to increase with the temperature (proportional to absolute temperature PTAT) and the weight of both has to be equal.

— All circuit are working with a quiescent current in the range of nano-ampere. To generate this low current, large resistors are required with a prohibitive occupied area. Therefore only transistor must be used.

— The main problem in the design of a voltage reference is the process variations. The exponential trend of drain current in WI region strongly impacts the performances of the circuit, since the deviation from nominal value is more important than in SI. Moreover the change in the threshold voltage due to the process variation can affect the stability of the output voltage reference. These considerations have to be taken in account into the design flow.

3.7 Circuit Design

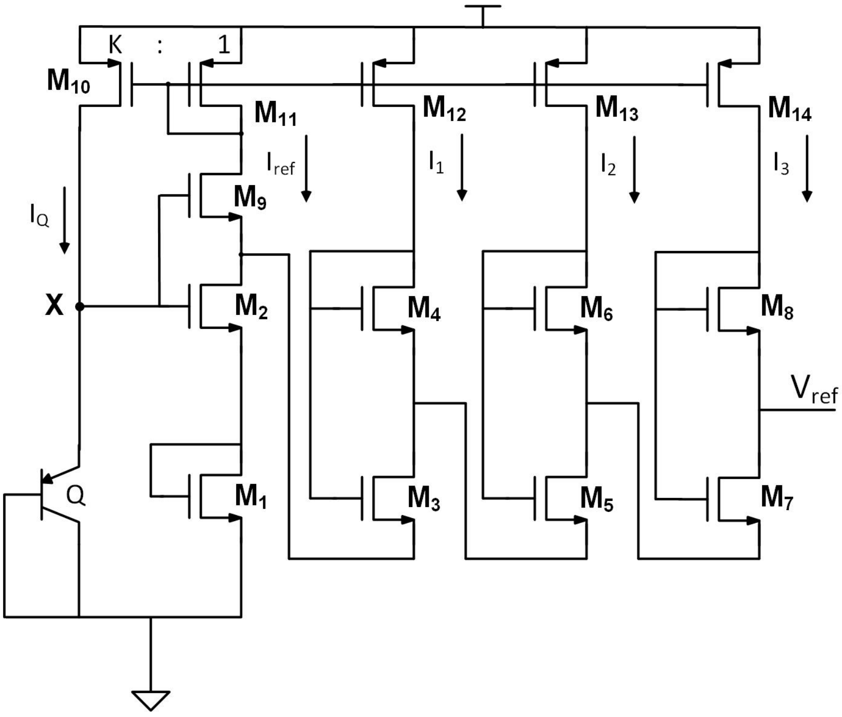


Figure 3.38 – Sub-bandgap voltage reference used in this work

The voltage reference implemented in this work is based on [MKB14]. In the left side of the Fig. 3.38 the CTAT voltage generator is made with the bipolar transistor Q and the MOS transistors M_1-M_2.In fact the voltage at the node X, simply the base-emitter voltage of Q, is equal to V_{gs1}+V_{gs2}. Therefore the gate-source voltage of M_1 can be expressed as

$$V_{gs1} = \frac{V_{eb}}{2} \tag{3.48}$$

This relation is true if the two MOS transistors have the same width and length channel and if the bulk-source voltage is equal to zero. As the CMOS technology process addressed in the present work allows a triple n-well configuration it is possible to tie the bulk node to the source potential. The pair of transistors M_9-M_2 acts as the first PTAT voltage generator. With this configuration V_{ds2} = V_{gs2}-V_{gs9} and it can be expressed as:

$$V_{ds2} = nV_t ln\left(\frac{pS_9}{S_2}\right) \tag{3.49}$$

where p is the number of times that the reference current I_{ref} is replicated to generate the PTAT voltage. To create a self-biased circuit, the voltage at node X is generated by the feedback path through the current mirror M_{11}-M_{10}. In this way choosing the factor K and the aspect ratio of transistors M_1 a non zero equilibrium point can be achieved. With the Eq. 3.48 and knowing that I_Q=$I_{ref} \times K$, V_{eb} can be expressed as

$$V_{eb} = V_t\frac{2mn}{2n-m}\left[ln\left(\frac{I_{D0}K}{I_{sat}4A}\frac{W_1}{L_1}\right) + \frac{V_{th}}{nV_t}\right] \tag{3.50}$$

where n is the slope factor of MOSFET transistor, m and A and I_{sat} are the slope factor, the emitter surface and the saturation current of the bipolar transistor. At this point to counterbalance the CTAT voltage, the only PTAT cell created by transistor M_9-M_2 is not enough. Thus, 3 cascaded source-coupled [VN78] cells are added to eliminate the temperature dependence. To ensure the correct function of every cell, the top transistor has to be in saturation region. Moreover the drain current has to be greater than the leakage current of MOSFET and lower than the value for which the transistor stops to work in WI. Every cell generates a PTAT voltage equal to the drain-source voltage of bottom transistor

$$V_{PTAT} = V_{ds,bottom} = \eta V_t ln\left(\frac{I_{d,bottom}S_{top}}{I_{d,top}S_{bottom}}\right) \tag{3.51}$$

The maximum generated voltage is around 100 - 120 mV. Therefore the total PTAT voltage is given by:

$$V_{PTAT,tot} = \eta V_t ln\left[\frac{I_7I_5I_3I_2}{I_8I_6I_4I_9}\frac{\frac{W_8}{L_8}\frac{W_6}{L_6}\frac{W_4}{L_4}\frac{W_9}{L_9}}{\frac{W_7}{L_7}\frac{W_5}{L_5}\frac{W_3}{L_3}\frac{W_2}{L_2}}\right] \tag{3.52}$$

Finally the output voltage reference is expressed as

$$V_{ref} = V_{gs1} + V_{PTAT,tot} \tag{3.53}$$

Setting the aspect ratio of transistors and the current multiplication factor given by the number of stages in cascade, it is possible to obtain the CTAT coefficient temperature which cancels the thermal dependence of output voltage. Surely one of the main design criteria is the power consumption. But as explained previously the drain current has to be higher than the leakage current. Moreover the aspect ratio of transistors is an important parameter to be taken in account, since it impacts the PTAT coefficient and has to simplify layout techniques as in the case of common centroid. Considering this limitation, it was chosen $S_1 = S_2 = 4$ and $K = 4$. The currents $I_{ref} = I_1 = I_2 = I_3 = 6.5$ nA, thus the collector current of Q is equal to 26 nA. This leads to have $V_x = 0.584$ V. The aspect ratio S_9 is 18. The remaining transistors exhibit a form factor $S_{4,6,8}/S_{3,5,7} = 5$. Therefore the nominal output voltage reference obtained at 27 °C is 650.4 mV. The total quiescent current is 52 nA, for a power consumption of 62.4 nW.

Table 3.3 – Transistors Size

Transistor	Aspect Ratio
M_{11} M_{12} M_{13} M_{14}	(2/1)
M_{10}	(8/1)
M_9	(18/1)
M_2 M_1	(4/1)
M_4 M_6 M_8	(10/1)
M_3 M_5 M_7	(2/1)
Q	1 (emitter area)

Sub-bandgap simulation results

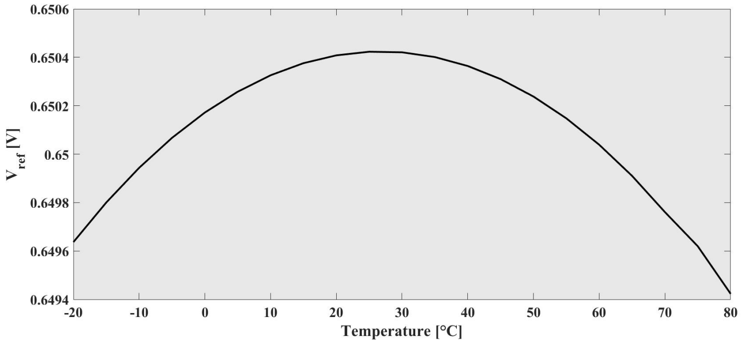
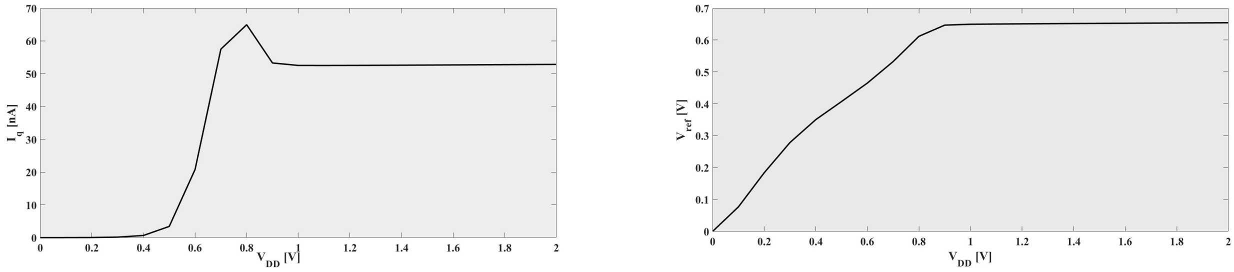


Figure 3.39 – Output voltage reference versus the temperature



(a)

(b)

Figure 3.40 – The quiescent current (a) and the voltage reference (b) versus supply voltage

Fig. 3.39 shows the dependence of V_{ref} on the temperature range. The curve exhibits the typical curvature due to the non-linearity of BJT base-emitter voltage. The temperature coefficient is about 15.9 ppm/°C. The line regulation is 4.75 mV/V from 1V to 2V of supply voltage Fig. 3.40(b). From Fig 3.40(a) it is evident that once the CTAT voltage circuit reaches the equilibrium point, for $V_{DD} = 0.95$ V, the current remains almost constant for the entire supply range. MonteCarlo simulations was performed (Fig. 3.41) to take into account process variations and mismatch. The results shows a mean of 650.4 mV with a standard deviation of $\sigma = 15$ mV. The main disadvantages of WI, is that the process variations have a greater impact on the circuit performances.

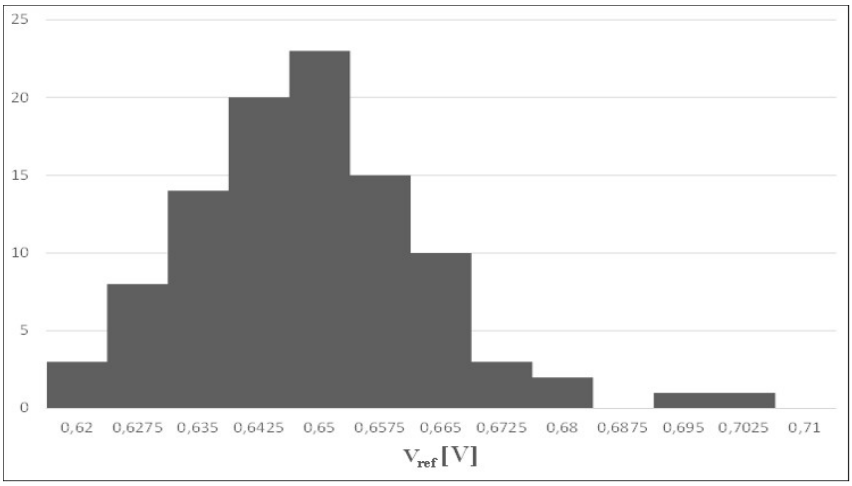


Figure 3.41 – Monte Carlo simulations on the output voltage reference with 100 runs.

3.8 Voltage Regulator Simulation Results

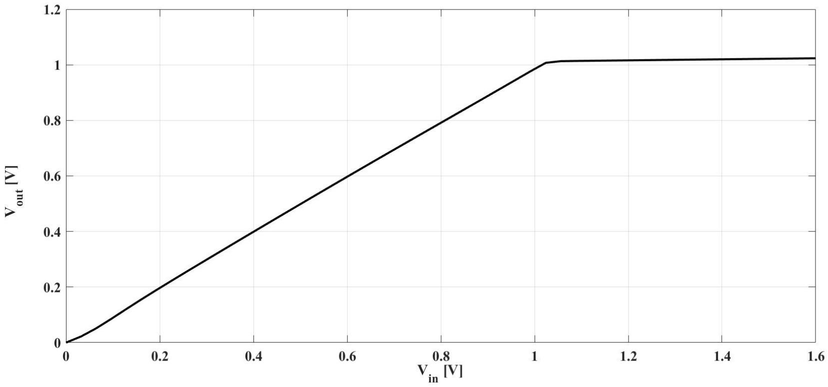


Figure 3.42 – Line regulation (orange line) of LDO when V_{IN} moves from 0 V to 1.6 V. The simulation is performed at heavy load condition.

The final design has been realized in 130 nm Standard CMOS process from ST Microelectronics. Each simulations are performed with sub-bandgap circuit. The Fig 3.42 shows the line regulation of the LDO up to input voltage of 1.6 V. The minimum V_{in} for which the output is at its nominal value of 1 V is about 1.095 V. The LDO shows a line regulation about 17 mV/V. As expressed in the Eq. 3.4 high loop gain is preferable to reduce the variations at the output voltage.
Load regulation is represented in Fig 3.43. The LDO shows a Load regulation about 6 mV/mA. Also in this case high loop gain helps in reduction of output voltage variations. This is evident in the first part of graph where the circuit is at lower bias point. In this range the slope is more accentuated than the second part, because the regulator presents lower open loop gain. Therefore the DC accuracy performances of LDO are dictated by the trade-off accepted in the design stage.
The transient responses of the regulator are depicted in (Fig. 3.44, 3.45 and 3.46) for three different situations. All rise and fall current steps are equal to 100 ns. In Fig. 3.44

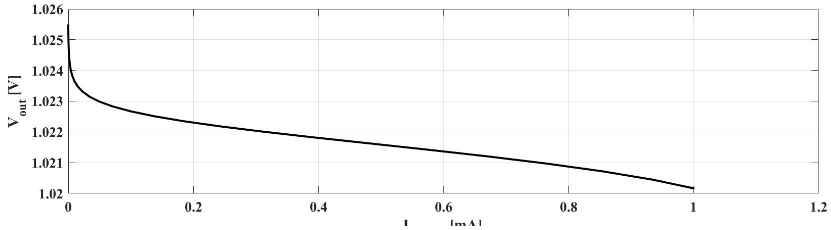


Figure 3.43 – Output Voltage versus output current

the load current changes from 1μA to 1 mA and indicates the operation mode of the regulator. The advantage of the adaptively bias is well evident in terms of speed response. In fact the transient time decreases from 3.2 μs without the adaptively bias to 0.78 ns when the circuit is inserted. It is worth noting that the magnitude of voltage spike is the same for both circuits. This is because at first time the error amplifier counteracts the output voltage variation slewing the gate capacitance of pass transistor. Only when the voltage changes at the EA output, the adaptively bias circuit supplies more current to the amplifier, therefore the bandwidth of closed loop extends accordingly. It is clear that the two circuits with the same EA at the same bias point present an identical voltage spike. The situation appears different when the output current moves from moderate condition to heavy condition as in Fig. 3.46. In this case, at the starting point the closed loop bandwidth of the LDO is larger for the adaptively bias topology and the spike reduction is about 15 mV.

The Fig. 3.47 shows the simulation result in the case of an input voltage step at heavy load condition. Besides the improvement in speed response, the adaptively bias gives better results in term of noise suppression. In fact the PSR at very low frequency is inversely proportional to the closed loop gain. The Fig. 3.48 underlines that when the adaptively bias circuit is removed the power supply rejection is at very low value of -10 dB, while with adaptively bias circuit the improvement is of about 25 dB. Montecarlo simulations were performed for the phase margin (PM) (Fig. 3.49) and output voltage Fig. 3.50. In particular for the PM only worst cases were addressed. The results shows a mean of 92° with a standard deviation of $\sigma = 0.67°$ for $I_{load} = 1\mu A$ and a mean of 65° with a standard deviation of $\sigma = 3.9°$ for stand-by condition. For the output voltage the two extremes of the operating condition were addressed. In this case a mean of 1.029 V is obtained with a standard deviation of σ= 0.025 V for $I_{load} = 1\mu A$. For $I_{load} = 1mA$ the regulator shows a mean of 1.004 V with a standard deviation of σ= 0.024 V.

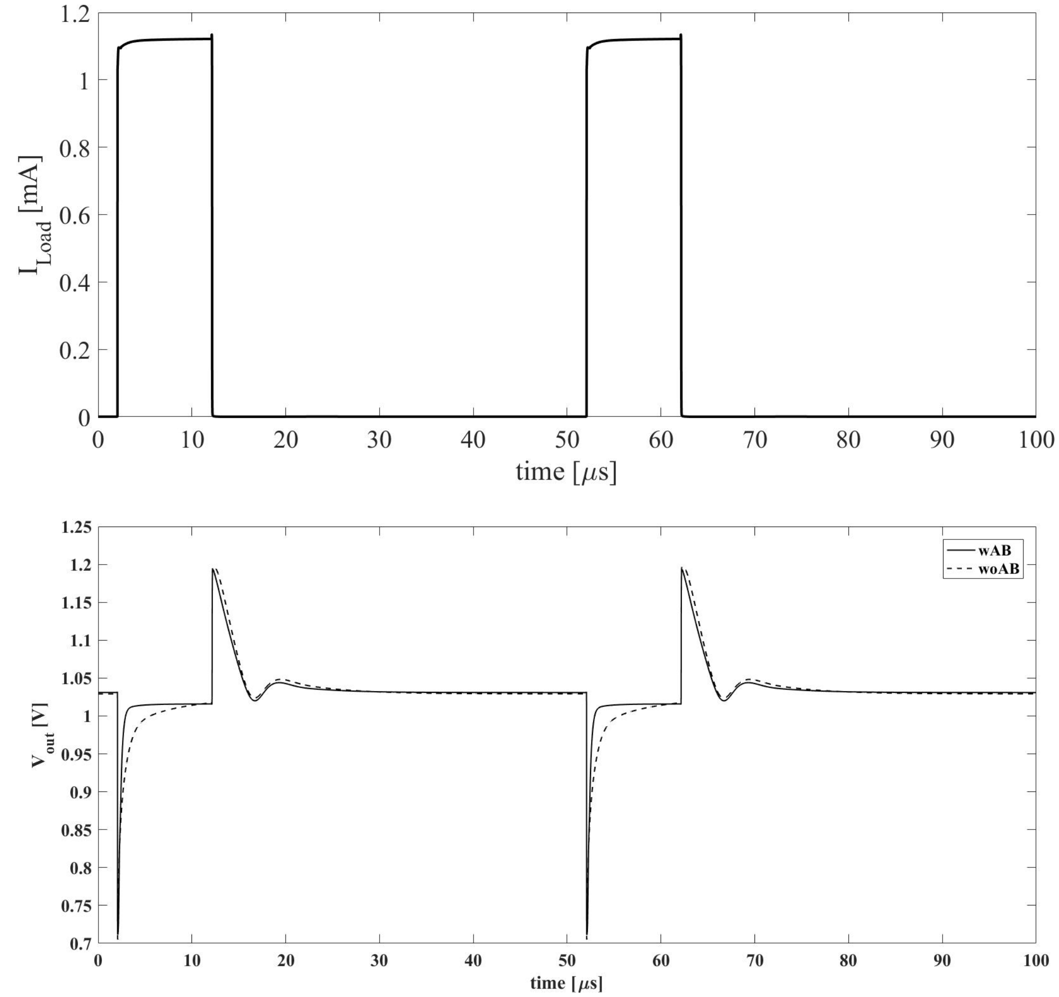


Figure 3.44 – Transient response for a load current step in operation mode. From 1 μA to 1 mA.

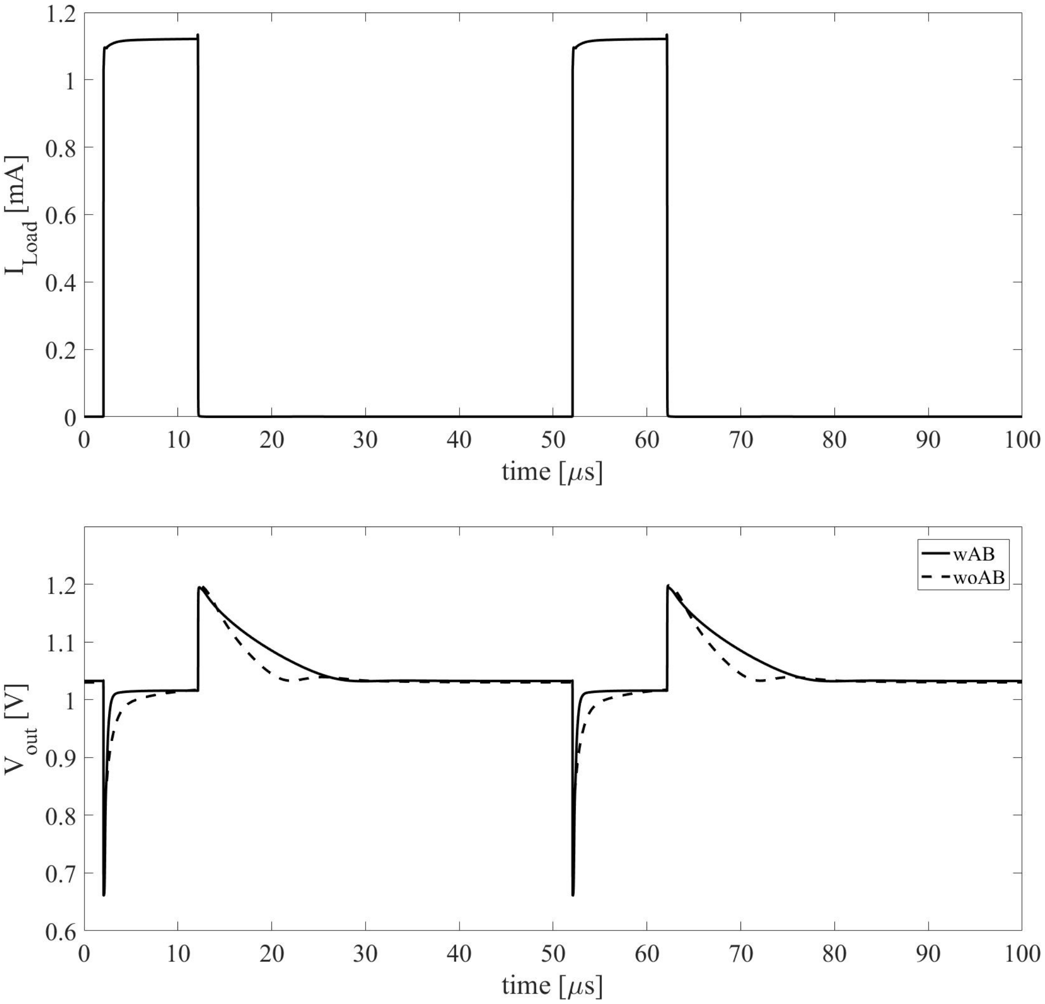


Figure 3.45 – Transient response for a full load current step. From 300 nA to 1 mA.

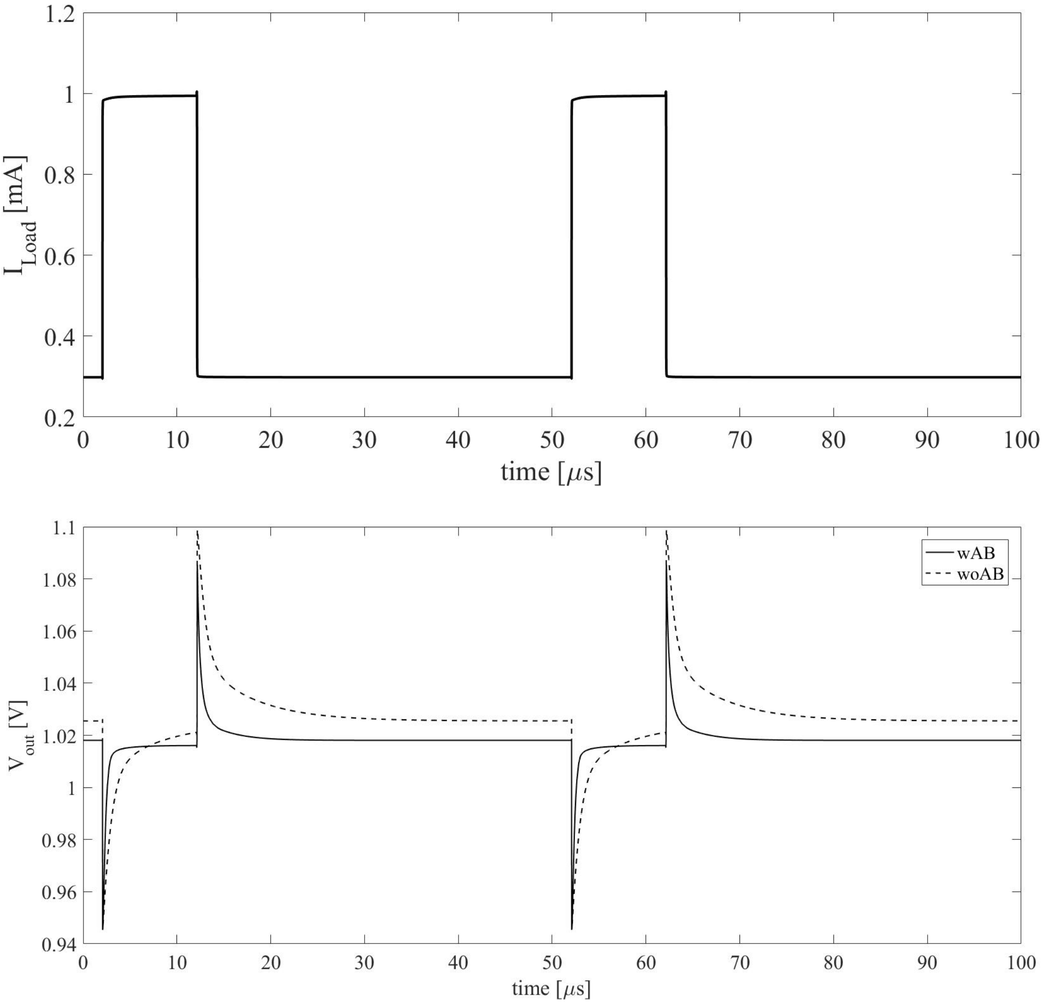


Figure 3.46 – Transient response for a load current step in moderate condition. From 300 μA to 1 mA.

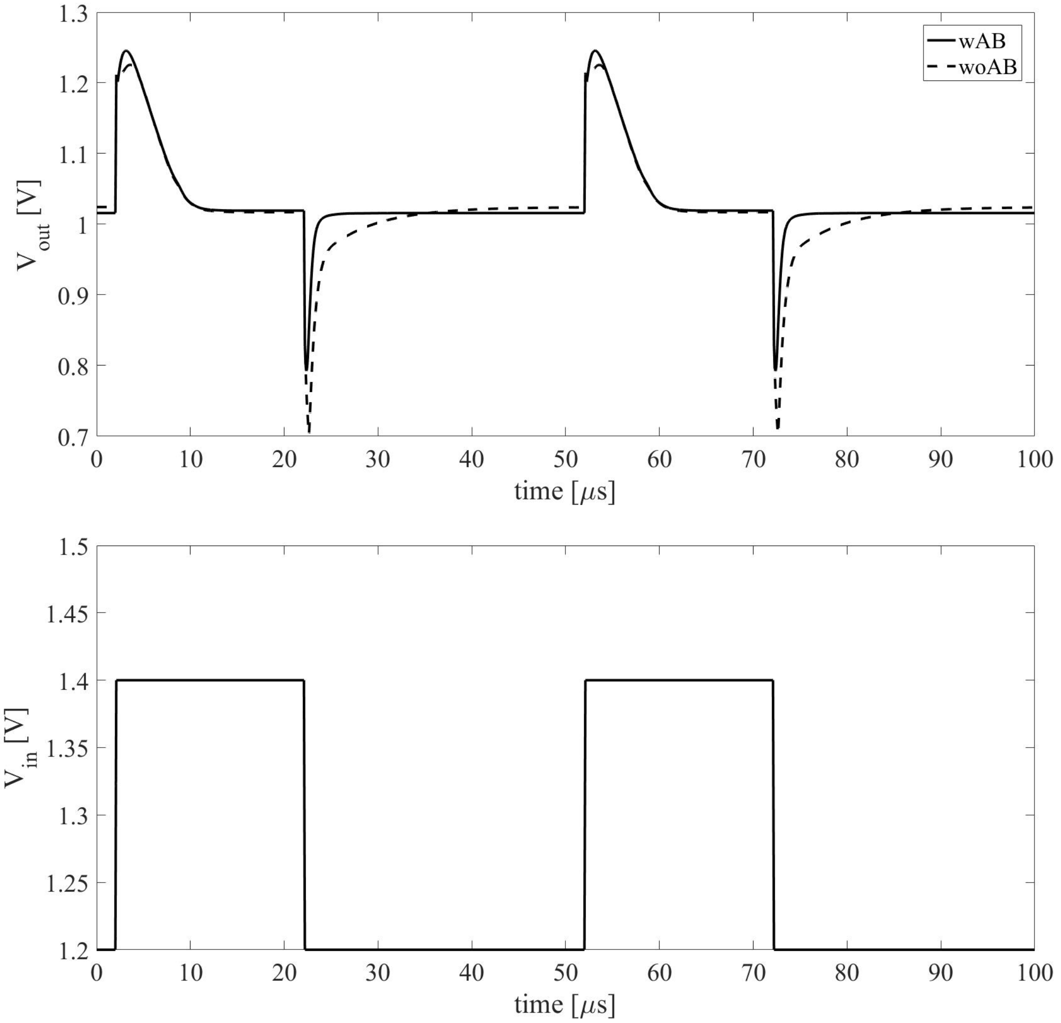


Figure 3.47 – Line transient at heavy load condition

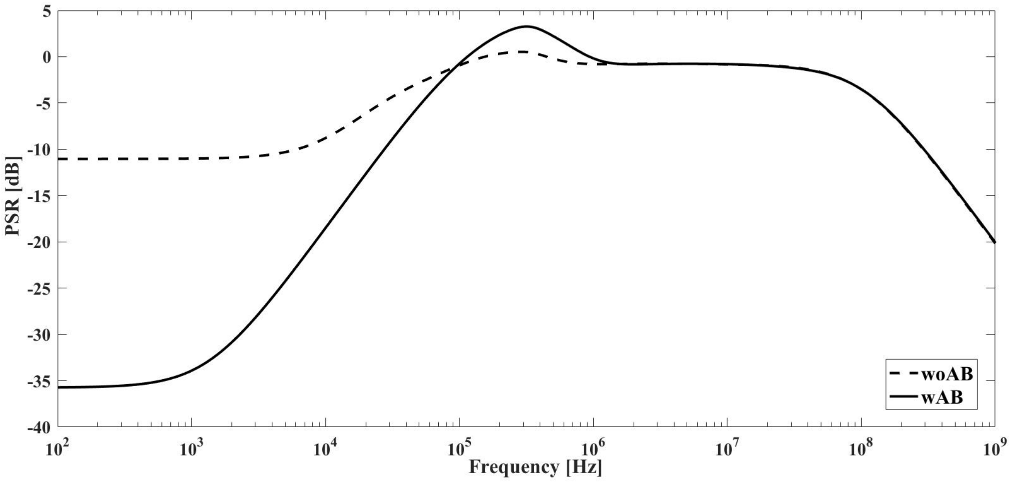


Figure 3.48 – PSR at heavy load condition

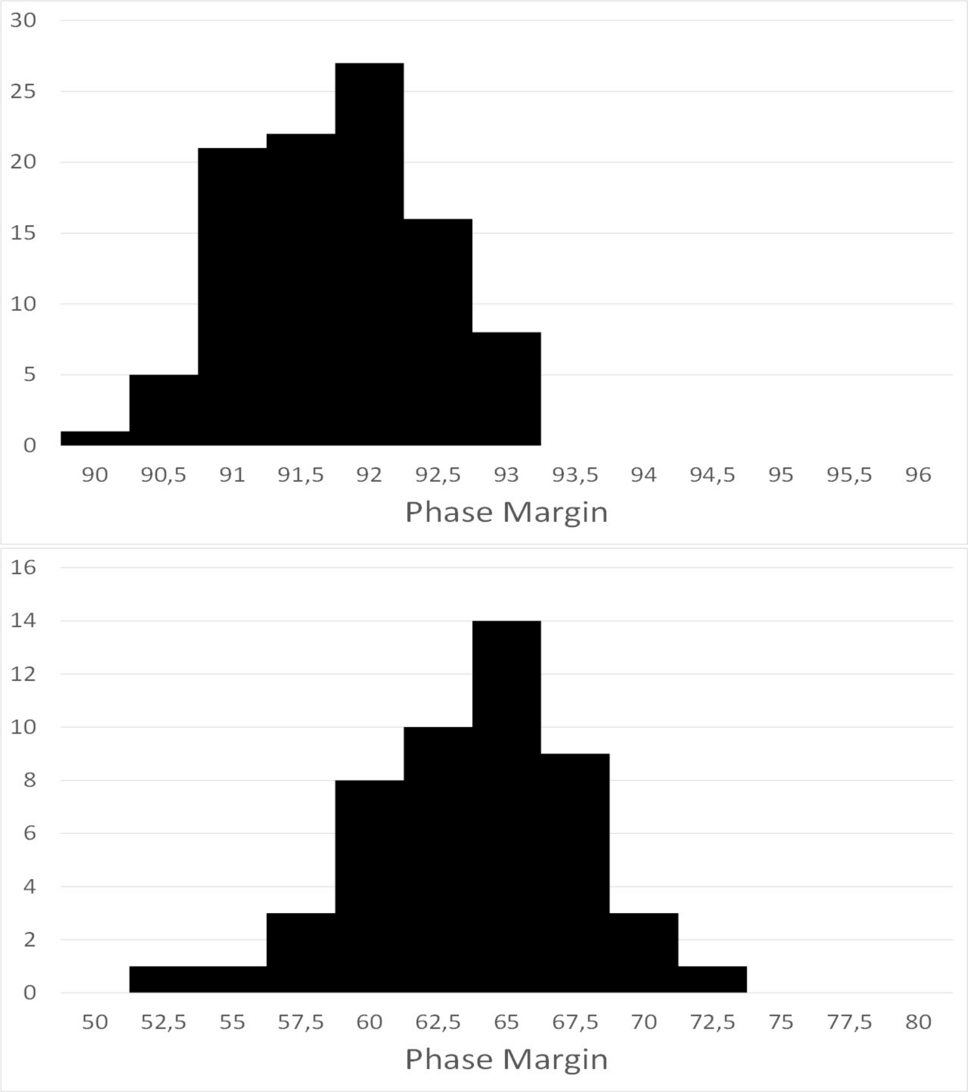


Figure 3.49 – Monte Carlo simulations on the phase margin with 100 runs.a) for stand-by condition b) for minimum operating load condition

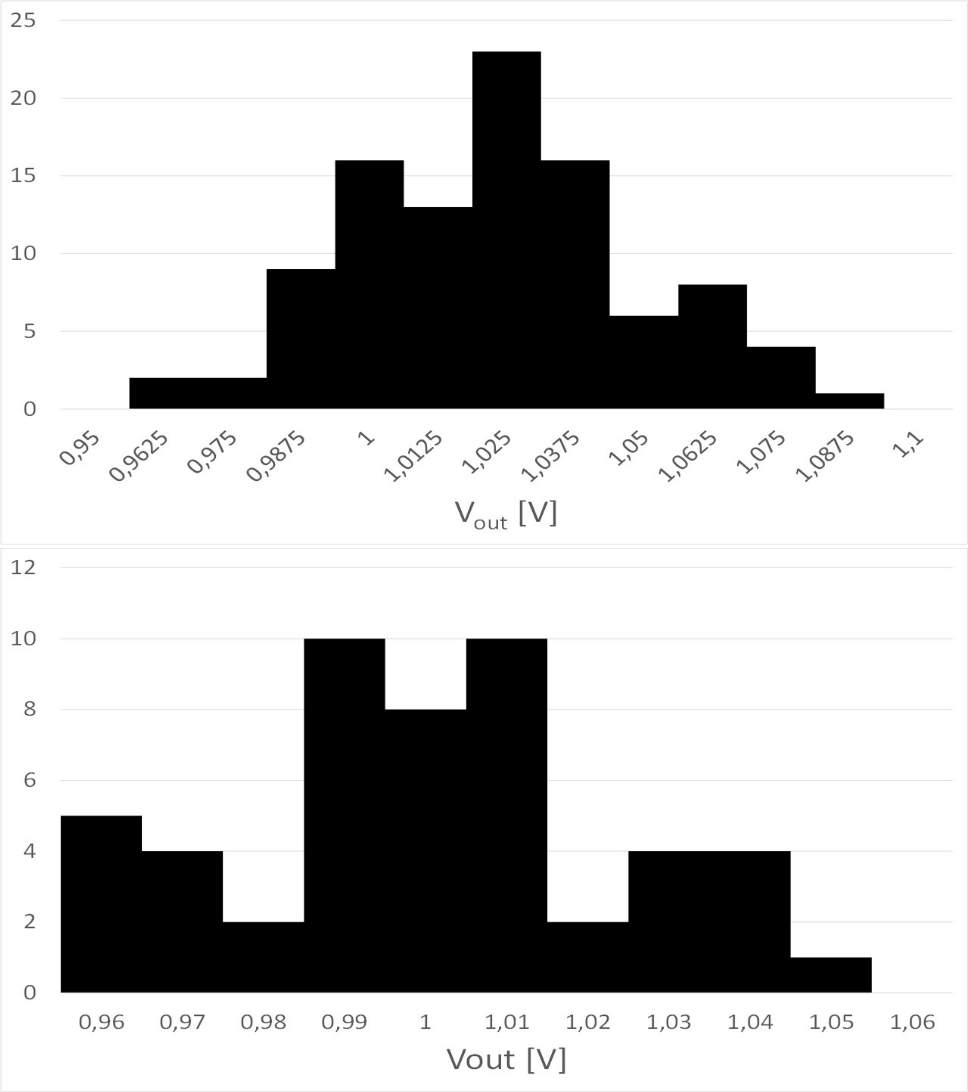


Figure 3.50 – Monte Carlo simulations on the regulator output voltage with 100 runs. a) for minimum operating load condition b) for maximum operating load condition

3.9 Conclusion

An adaptively biased LDO regulator has been designed for harvesting applications. Class AB Error Amplifier and adaptively bias circuit have been adopted to improve the transient response with high current efficiency under all load condition. The stability of the feedback loop has been guaranteed by the Miller compensation capacitor with the aid of the current buffer. The regulator exhibits a minimum PM about 65° for a load current lower than the minimum value in operating range. In this way the stability has been ensured also under stand-by condition.

When the adaptively bias is inserted, the time to recover the nominal output voltage is lesser than 1 μs consuming only 2,25 μW under heavy load condition. Also AC performances take advantage because the error amplifier exploits higher voltage gain due to high quiescent current. The FOM $= t_r \frac{I_q}{I_{load,max}}$ is introduced to compare the different designs, lower value means better performances. Larger FOM respect to [KM14], where the quiescent current is constant for all load range, is balanced by a better current efficiency especially at light load condition. However, considering the strict requirements for the regulator, the designed LDO is well suited for harvesting applications.

Table 3.4 – Comparative switching regulator

	[KM14]	[ZG12]	This Work
V_{out} (V)	1	-	1
V_{DO} (V)	-	0.109	0.12
C_L (pF)	-	2	20
$I_{load,max}$(mA)	5	5	1
I_q(μA)	99.04	12	1.8
Efficiency	98	99	99.9
t_r (μs)	0.161	2	0.9
FOM (ns)	3,18	4,8	1,62

Chapter 4

Ultra-Low power transmitter

Transmitter is one of the most hungry circuit in a communication system. Especially in long range transmission, where high output power level ($>$ 20 dBm) is required, the power amplifier (PA) needs high quiescent current to assure high voltage gain. Moreover the system requires a stable frequency carrier and a clean spectrum to avoid adjacent channel interference. Clearly satisfying all those requirements means complex system and thus higher power consumption. To comply the necessity imposed by the energy constrains in harvesting system, the design approach of transmitter has to be revisited. At first the communication distance is no more longer than 10 m and thus the transmission power level is in the range of tens-hundreds of μW (-20 dBm to 0 dBm). Therefore when the communication distances decrease, as in the case of the WSN, the PA weight in terms of power consumption is comparable with that of the local oscillator LO and matching network MN.

For example adopting high performances receiver, with a frequency correction loop scheme, is possible to use simple and not very accurate local oscillator on the transmitter side. In this way it is possible to avoid high power PLL based frequency generator or high cost crystal reference based system. As reviewed in chapter 2, a non coherent modulation scheme (OOK or FSK) permits to reduce the power consumption and relax the power amplifier linearity, and the low-complexity architecture is a favorable point for ULP transmitter. Unfortunately this configuration suffers from a poor spectral efficiency.

In summary the paradigm "less is better" can represent a way to demolish the problematics of power consumption in ULP transmitter design. Clearly the performances achievable can not be comparable to the classical transmitter and depending on the application some aspects have to be sacrificed.

4.1 Transmitter architecture

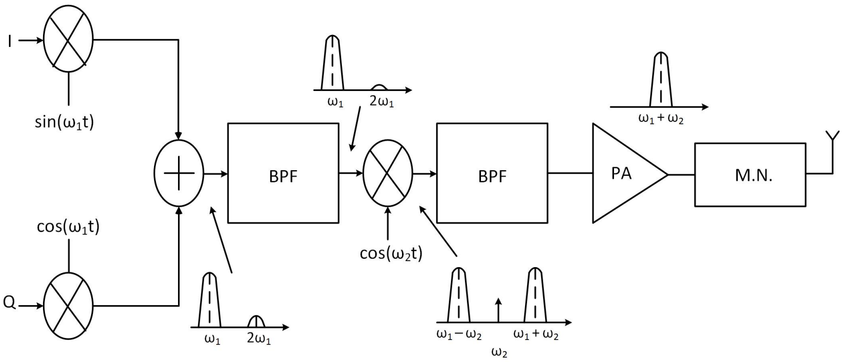


Figure 4.1 – Block diagram of two-step conversion transmitter

A classical two-step transmitter is depicted in Fig. 4.1. This topology is a modified version of direct-conversion architecture in order to avoid injection pulling phenomena [Raz99]. In fact one of the main problems is the high power signal at PA output, which can modify the frequency oscillation of the LO. With the two-step transmitter the PA spectrum is quite far from the frequency generated by the VCO, reducing the risk of frequency shift. However the number of blocks required to achieve high spectrum efficiency and clean frequency are not negligible, unlikely this high power solution can represent a good approach for the target of this work.
Since that in short distance communication the PA output power level is not high, the frequency pulling is less probable and a direct modulation scheme can be a optimum solution to implement very low-power transmitter. In fact only three blocks are needed to generate the RF signal, where the modulation is normally done in the frequency generation circuit Fig. 4.2. Both on-off keying (OOK) and frequency shift keying (FSK) can be implemented where the baseband signal directing modulates the signal transmission. Moreover non-linear high efficient power amplifier can be adopted.

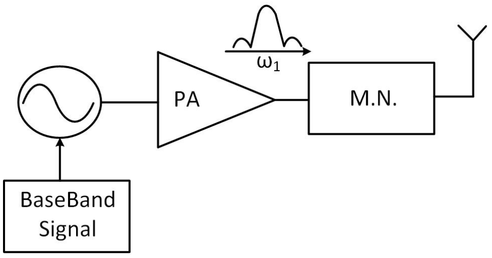


Figure 4.2 – Block diagram of direct modulation transmitter.

It is clear that in direct modulation architecture every block has a more important impact on overall efficiency respect to the high output power transmitter where the main design efforts are addressed to improve the PA efficient. Therefore the global transmitter efficiency can be written as

$$\eta_{TX} = \frac{P_{rad}}{P_{DC,PA} + P_{DC,LO} + P_{DC,mod}} = \frac{\eta_{PA}}{1 + \eta_{PA}\frac{P_{DC,LO}}{P_{rad}} + \eta_{PA}\frac{P_{DC,mod}}{P_{rad}}} \tag{4.1}$$

where P_{rad} is the radiated power level, $P_{DC,LO}$ $P_{DC,PA}$ and $P_{DC,mod}$ are the DC powers dissipated by the local oscillator, the power amplifier and the circuits which generate the modulation signal. It is worth noting that the maximum attainable PA efficiency η_{PA} not only depends on the PA operating class, but in short distance communication the matching network efficiency has a crucial role in terms of power transmission capability. From the analysis in [HP06] the efficiency of a generic L-matching network can be expressed as

$$\eta_{MN} = 1 - \frac{Q}{Q_L} - \frac{Q}{Q_C} \approx 1 - \frac{\sqrt{\frac{R_{opti}}{R_s} - 1}}{Q_L} \tag{4.2}$$

where Q_L and Q_C are the quality factor of inductor and capacitor, Q is the total quality factor of matching network that depends on the transformation ratio between the optimum resistance R_{opti} and the antenna resistance R_s. The approximation is valid only up to 10 GHz, where the poor inductor quality factor dominates the overall efficiency. Some considerations will be done further about the problematics of matching network design when the radiated power is in the range of tens of μW. Even if the transmission efficiency (Eq. 4.1) gives us an instantaneous photography of the transmitter capability to save the available power, this does not highlight the energy cost to transmit a certain amount of data. Moreover, in WSN the transmitter is in stand-by mode for the most part of time. An useful metrics used to evaluate the transmitter is the energy per bit (E_{bit}) needed to transmit a packet of information

$$E_{bit,DC} = E_{bit} + \frac{P_{DC,stand-by}}{DC \times DR} \tag{4.3a}$$

$$E_{bit} = \frac{P_{DC,tot}}{DR} \tag{4.3b}$$

Where DR is the data-rate and $P_{DC,tot}$ and $P_{DC,stand-by}$ are the total powers burned by the transmitter in active and stand-by mode respectively, DC is the duty cycle. However this metric does not facilitate the comparison between different topologies. As first it does not provide information about the radiated power, second to recover the information about the power dissipated in stand-by mode is not always possible. Therefore generally only E_{bit} is used to compare different transmitters. To have a more complete framework, the FOM introduced in [TLHL14] [VHH$^+$11c] can be used to evaluate the performances of different topologies

$$FOM = \frac{E_{bit}}{P_{rad}} \tag{4.4}$$

The above equation relates the transmission efficiency and the data rate highlighting the relation between the transmitter architecture and the application/standard.

State of the Art

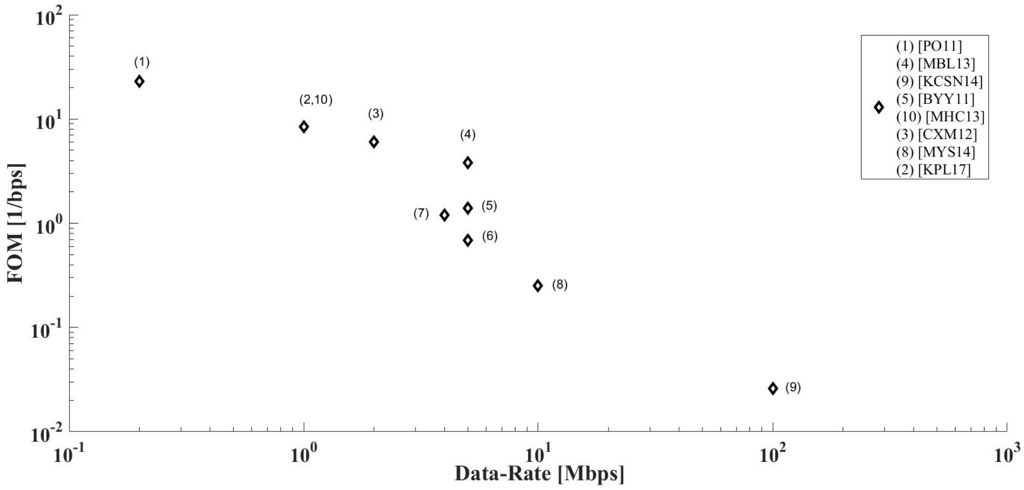


Figure 4.3 – FOM versus data-rate for recent ULP transmitter. [KPL17]

In Fig. 4.3 representative ULP transmitters are classified based on the normalized FOM for respective data-rate. As can be seen most of them adopt a data-rate between 1 and 10 Mbps, proving that in general the information processed in WSN does not require high amount of data. For example the transmitter (dot 9 in the fig.4.3) proposed in [KCSN14] is designed to have high bandwidth to support high data-rate, where the capsule endoscopy system uses high amount of data to generate high resolution image for accurate diagnosis. At the opposite side, for transmitter (dot 1 in the fig.4.3) lower data-rate is chosen for peer-to-peer communication. The architecture is based on multi-phase injection locking [PO11] where the frequency of injected signal is generated at 45 MHz through a stable crystal reference. Then the different phase-shifted signals from the injection locking ring oscillator ILRO are merged in a PA/EDGE-combiner EC Fig 4.4.

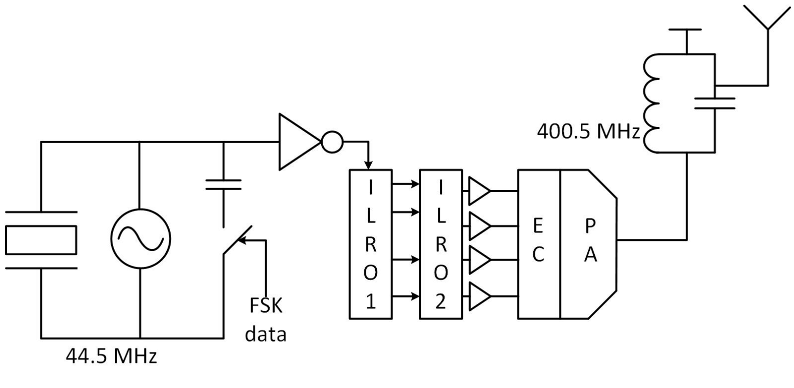


Figure 4.4 – Block diagram of sub-harmonic injection locking transmitter [PO11].

The same sub-harmonic injection-locking architecture is used for transmitters (dots 3 and 10 in the fig.4.3), at the same carrier frequency of 400 MHz. The difference in this case is the amplification stage that is provided by a class-C power amplifier. The main drawbacks of this architecture are the off-chip matching networks where the frequency transmission of 400/500 MHz makes hard the passive integration. An extremely low complexity transmitter (dot 4 in the fig.4.3) is presented in [MBL+13]. The transmitter is composed by a direct-RF power oscillator, where the inductor acts as resonator and radiating element. The carrier frequency in this case is 2.4 GHz. The cross-coupled NMOS oscillator is tail-biased with ultra-low leakage transistor to reduce the stand-by leakage power. The transmitter is designed to support both FSK and OOK modulation.

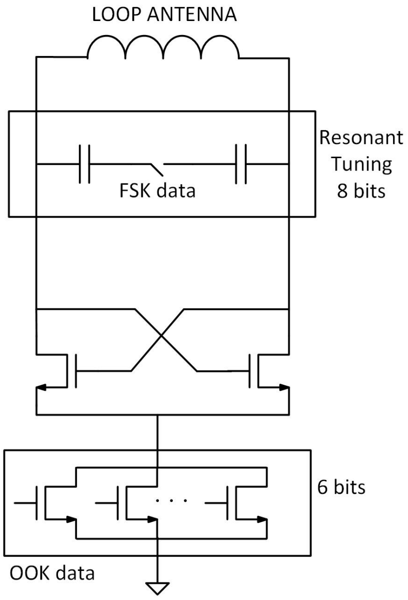


Figure 4.5 – Power VCO transmitter presented in [MBL+13].

From the above analysis, ULP transmitters for short distance range prefer non conventional architecture to reduce the power consumption with low output power and medium/high data-rate. However good performances can be achieved with classical architecture. In the next section several classical direct modulation architectures are reviewed supported by a design guideline to achieve low power consumption.

4.2 ULP Direct Modulation Transmitters.

In classical direct modulation transmitter, optimizing not only PA but also LO and MN is possible to achieve low-power condition, especially with modern devices where the transition frequency easily exceeds 100 GHz for submicron technology. For example, the STMicroelectronics 130 nm CMOS technology offers MOS transistors with a peak f_T of 120 GHz. In addition, the MOSFETs used in low power applications are generally small and therefore, their peak transition is higher than bigger transistors, even if the lower transconductance due the low bias current soothes this improvement. In any case, this high peak f_T allows subthreshold operation, in order to reach higher transconductance efficiency (g_m/I_d). As a consequence, the same RF performances are achieved at lower power consumption. Another design key point is the choice of voltage supply. As the power consumption is directly proportional to V_{dd}^2, decreasing the supply voltage considerably enhances the circuit efficiency. A lower V_{dd} also reduces the electric fields in the device and improves its long term reliability. On the other hand, low V_{dd} reduces the voltage headroom available for cascading transistors, invoking folded solutions.

In the next section the design considerations and the techniques as well as the different circuit blocks of the transmitter are described.

4.2.1 Local Oscillator

The carrier frequency generation can be done through voltage control oscillator VCO. The VCO can be classified in two main architectures: ring oscillator and LC oscillator. Irrespective of the topology the equation for the instantaneous VCO frequency is

$$f_{VCO} = f_o + K_{VCO}V_{ctrl} \tag{4.5}$$

where f_o is the free-running frequency, K_{VCO} is the gain of the VCO that settles how much a change in control voltage will change the VCO frequency. V_{ctrl} is the voltage to set the frequency at the desired value.

A ring oscillator is formed by a odd number of delay stages, where the output of the last stage is brought back to the input of the first one. The oscillation is assured if the ring provides a phase shift of 2π and has a unity voltage gain at the oscillation frequency. A VCO ring oscillator is depicted in Fig. 4.6

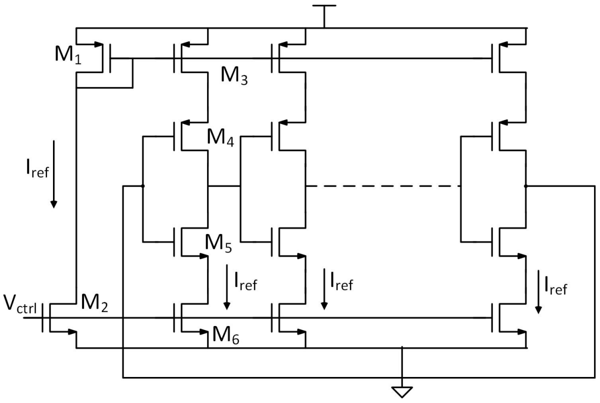


Figure 4.6 – Current starved VCO

The frequency oscillation of a ring oscillator is

$$f = \frac{1}{2Nt_d} \tag{4.6}$$

where N is the number of delay cell and t_d is the delay time of each cells. As the oscillation frequency is inversely proportional to the delay time and which depends on the bias current I_{ref}, V_{ctrl} provides control for the oscillation frequency.
In LC oscillator the frequency is generated through a lossy resonator. In order to sustain the oscillation a small-signal equivalent negative resistor has to be inserted to cancel out the losses, generated by the inductor and capacitor parasitic resistor. Fig. 4.7 shows a general representation of an LC oscillator, pointing out the negative resistor.

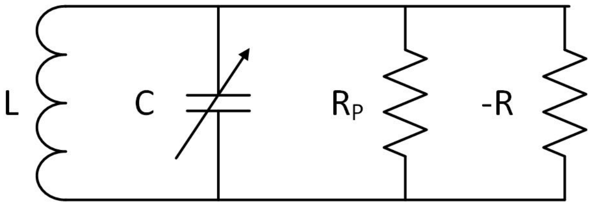


Figure 4.7 – LC resonator with negative resistor to compensate the losses due to parasitic resistor R_P.

The frequency oscillation is given by the resonant frequency of LC tank (Eq. 4.7). To set the desired frequency, the circuit is designed with a tunable voltage capacitor (VariCap).

$$f = \frac{\omega_o}{2\pi} = \frac{1}{2\pi\sqrt{LC}} \tag{4.7}$$

One of the most important property of a VCO is its phase noise. In a noiseless VCO the output voltage is expressed as

$$V_{out}(t) = A\cos(\omega_o t + \phi) \tag{4.8}$$

where A is the output voltage amplitude and ϕ the phase. However in presence of a noisy source the amplitude and the phase are altered. In particular, as depicted in Fig. 4.8 if the noise is injected at the signal peak, the amplitude changes without phase shift, and it recovers its nominal value due to the limiting mechanisms in a real oscillator. While if the noise is injected during the transition Fig. 4.8, the signal phase is shifted and this fluctuation persists infinitely [HLL99]. Therefore the Eq. 4.8 has to be rearranged as follows

$$V_{out}(t) = A(t)\cos(\omega_o t + \phi(t)) \tag{4.9}$$

where A(t) and ϕ(t) are the output voltage amplitude and phase time-dependent. A definition of phase noise [MA08] is as follows

$$L(\Delta\omega) = 10\log\left(\frac{\sum N_{L,i}}{2\Delta\omega^2 C^2 A^2}\right) \tag{4.10}$$

where $N_{L,i}$ is the white noise source and $\Delta\omega$ the offset frequency from the carrier at which the phase noise is measured. One of the unwanted effect of phase noise is the down-conversion of adjacent channels in the band of the desired signal.

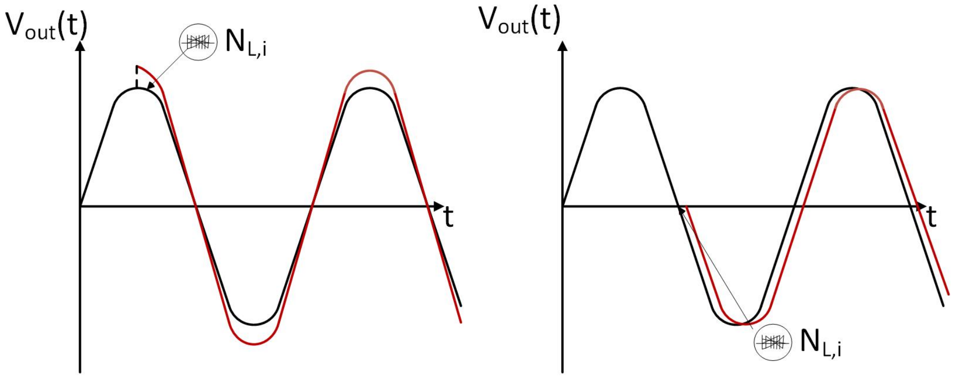


Figure 4.8 – Output voltage variation in presence of noisy source. At the left side the noise is injected at the peak voltage, at the right side the noise is injected at zero transition.

Another important property of a VCO is the range that the oscillation frequency can be varied from its center frequency also named tuning range. For example a VCO with a center frequency of 2.4 GHz and a tuning range of 10% gives the possibility to vary the frequency between 2.16 GHz and 2.64 GHz. A large enough tuning range is important in order to address the frequency shift due to the process and temperature variations.

4.2.2 Ring versus LC Oscillator

In terms of phase noise the LC oscillator has better performances, because of the resonator quality factor Q. A common definition of Q is

$$Q = 2\pi \frac{energy\ stored}{energy\ dissipated\ per\ cycle} \tag{4.11}$$

In a high Q resonator the energy is transfered between the capacitor and inductor with a little dissipation in parasitic series resistances. In this case, the LC oscillator exhibits therefore a low phase noise. In a ring oscillator the energy is stored in the parasitic capacitance of the next stage, that is charged and discharged every cycle. Therefore regarding the Eq. 4.11 LC oscillator has a Q higher than the RO one. Since phase noise is inversely proportional to the quality factor [LH00], clearly at the same power dissipated LC oscillator achieves better performances.

Low frequency noise aspect that makes the RO more noisy is that its noise is high during the transition, which is the worst case scenario in terms of phase shift as previously explained.

A high tuning range is often needed, whether to account for process variations. If a high tuning range is needed, a ring oscillator should be used. This because the parameter that can be varied to change the frequency of the ring oscillator can be varied over wide range. It is possible to reach a tuning range over 50%. In the case of LC oscillator the tuning range is more limited.

In spite of limited tuning range, LC oscillator has been preferred due to better performance in terms of phase noise, and lower power consumption for the same phase noise value.

4.2.3 Designing Low Power LC Oscillator

As discussed previously, LC oscillator is formed by a tank resonator and an active part needed to sustain the oscillation and to assure the start-up condition. Once the oscillation is started, the energy conservation law states that the maximal energy stored in the inductor should match the maximal energy stored in the capacitor:

$$\frac{CA_{peak}^2}{2} = \frac{LI_{peak}^2}{2} \tag{4.12}$$

A_{peak} is the voltage peak across C, and $Ipeak$ is the peak current amplitude through L and its parasitic series resistance R_s. The effective losses in the tank can be calculated as

$$P_{loss} = \frac{R_s I_{peak}^2}{2} = \frac{R_s}{2}\frac{C}{L}A_{peak}^2 \tag{4.13}$$

Reminding that the oscillation frequency is $\omega_o = \frac{1}{\sqrt{LC}}$ this expression can be rearranged as

$$P_{loss} = \frac{R_s}{2}C^2{\omega_o}^2A_{peak}^2 = \frac{R_s}{2L^2{\omega_o}^2}A_{peak}^2 \tag{4.14}$$

one can remark that for a given oscillation the losses, therefore the power consumption, scale with R_s and are inversely proportional to L^2. The previous equations suggest that the tank design should maximize the L/C and/or the L/R_s as well. The first goal might be limited by the required tuning range while the second one by the given technology. Eventually, it is worth noticing that the losses quadratically scale with A_{peak}. However, as Eq. 4.10 states a reduction in output voltage peak makes higher the phase noise.

The inductor L is not only a indispensable player for the frequency generation, but it is an important design parameter to achieve low power consumption with good phase noise. At frequency of interest the parasitic resistance associated to the LC tank R_p is due mainly to the inductor series resistance R_s. Giving the inductor quality factor Q_L it is possible to transform the lossy LC tank into a parallel RLC circuit:

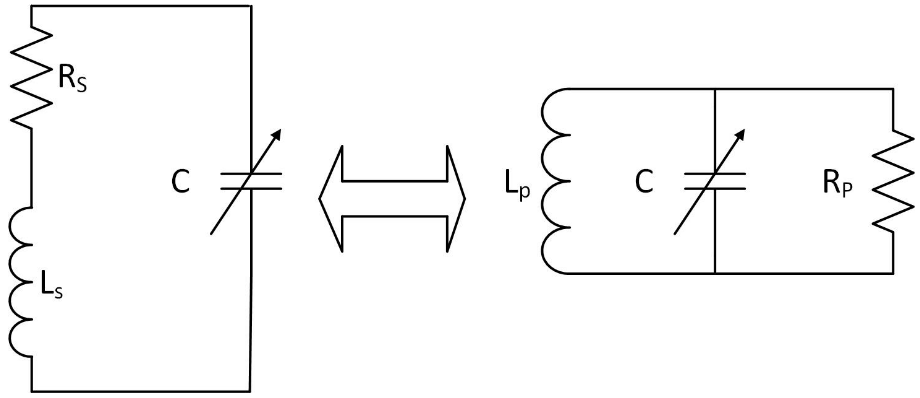


Figure 4.9 – Transformation of series LC tank to parallel one.

$$Q = Q_s = \frac{\omega L_s}{R_s} = Q_p = \frac{R_p}{\omega L_p} \tag{4.15}$$

To understand how the inductor impacts on the power consumption a LC NMOS cross coupled oscillator is introduced in Fig. 4.10. The transistors M_1 and M_2 are the active part

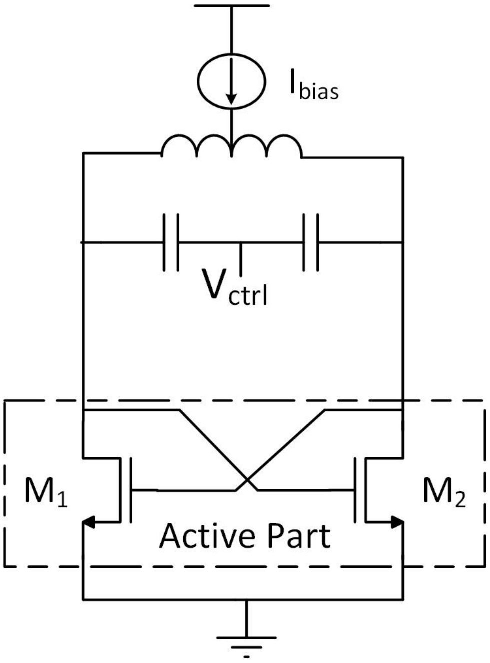


Figure 4.10 – NMOS cross coupled LC oscillator.

of the oscillator needed to satisfy the Barkhausen's criteria. The oscillation is sustained if an adequate loop gain is assumed:

$$\frac{g_{m1,2}}{2} > \frac{1}{R_p} = \frac{R_s}{(\omega L)^2} \tag{4.16}$$

where $g_{m1,2}$ is the transconductance of M_1 and M_2. R_p is forced by the inductor parameters; Eq. 4.16 states that a critical transconductance g_{mcrit} has to be assured. In general the active part is designed to have a g_m three times higher than $g_{m,crit}$. Depending on the transistor operation region, the g_{mcrit} depends only on the drain current in WI and by the transistor size in SI. Eq. 4.16 suggests a high value of L is preferable in addition with high quality factor to achieve lower g_{mcrit}. However the low quality factor of integrated inductor and the larger area occupied by high inductance limit the minimum power consumption achievable.

If a sufficient voltage headroom is available, a way to half the power consumption is to implement a CMOS LC oscillator as depicted in Fig. 4.11.

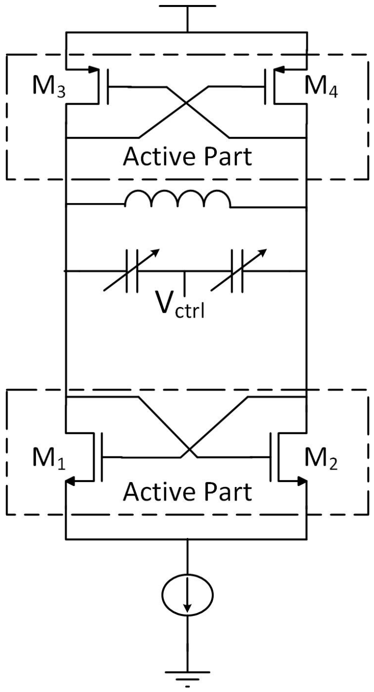


Figure 4.11 – CMOS LC oscillator

Stacking PMOS and NMOS transistors, the transconductance presented to the LC tank is twice than the only NMOS topology. The g_{mcrit} in this case is equal to:

$$g_{mcrit} = \frac{g_{m1,2} + g_{m3,4}}{2} \tag{4.17}$$

where $g_{m3,4}$ is the transconductance of cross coupled PMOS transistor. Observing the Eq 4.17 the same NMOS cross coupled g_{mcrit} can be achieved with the half of current bias. The VCOs depicted in Fig (4.10-4.11) exploit a current source to stabilize the bias point even if this comes with a higher phase noise. If the current source is omitted, larger signal swing, lower power dissipation and lower phase noise can be obtained even if the bias point will be more sensitive to temperature and bias voltage variations and electronics aging, as well.

4.2.4 Power Amplifier

As introduced previously, the PA efficiency is mainly set by its operating class. Classical topologies (A, B, and C class) use the transistor as an amplifier and the operating class is set by the quiescent bias point and the amplitude of the input signal; PAs in Fig 4.12 are indeed not small-signal amplifiers, so the input signal is allowed to modify the transistor bias point.

For these classes the efficiency should be a trade-off with distortion issue. It is also useful here to remind that over-voltages are present in class B and C PA, so that a maximum voltage of twice V_{DD} is applied to the drain of the transistor. This might causes a trouble of long-term reliability. Theoretically, 100% efficiency can be achieved by using switching topologies (D, E, and F class), where the transistors are used as switch and no more as amplifier. The main idea is to avoid that current flows into a transistor

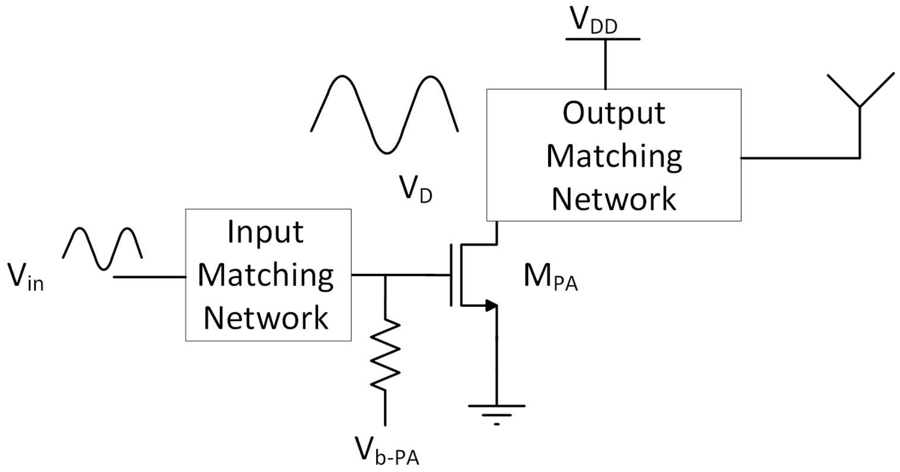


Figure 4.12 – General representation of power amplifier.

when its drain-source voltage is not zero. So, current can flow but the drain-source should be zero (the transistor acts as closed switch) or the drain-source should be not zero but the transistor is off and so current cannot flow (the transistor acts as an open switch). In both cases the transistor is kept cold, because no dissipation takes place. Long term reliability troubles plague also the class E PA, where the maximum voltage applied to the drain can rise up to about 4 times V_{DD}, while this is not the case for the class D and F, where the drain voltage does not exceed V_{DD}.

— Switching/non-switching PA?

Switched PA requires large transistors to achieve smaller on-resistance and these transistors should also be hard driven, as they should operate like switches. As pointed out by Chee [ea06], the resulting high drive requirement largely increases the power consumption. In addition, the matching networks for switched PA are complex and require several inductors, resulting in larger silicon area and higher losses, making this type of PA not suitable for low radiated power applications. On the other hand, non-switched PA requires less drive capability offering higher transmitter efficiency for low radiated powers. For this reason, non-switched PA was adopted in the present work. In particular, class-C operation was used. It is here worth reminding that, as previously described, the OOK scheme does not pose constraint on the PA linearity and therefore a class C PA is well suited in spite of the distortion. As the conduction angle is well lower than π, the transmitter is not always active and low leakage transistors were preferred, in order to minimize the stand-by dissipated power even if their transition frequency f_t is low.

— Single-Ended/differential PA?

Most stand-alone PAs, as the one designed in the present work, are realized in a Single-Ended (SE) topology, since antenna is typically SE, and SE RF circuits are much simpler to test than their differential counterparts. Even if a differential PA would better use the VCO output, as they sense both the VCO output phases, for sake of simplicity, in the present work the PA was designed single-ended. No balun was placed between the VCO/PA interface, in order to avoid extra losses.

— Matching Network

In low power applications, matching network plays an important role, as it should guarantee that no power is wasted at the PA \antenna interface. However the MN efficiency is deteriorated by the high transformation ratio required when the radiate power is in the range of tens of μW. The power delivered to the generic load resistance R_L can be expressed as:

$$P_1 = R_L I_1^2 = R_L \frac{I_{max}^2}{2\pi} \frac{\alpha - \sin(\alpha)}{1 - cos(\frac{\alpha}{2})} \tag{4.18}$$

where P_1 is the power at the fundamental frequency, α the conduction angle, I_1 and I_{max} are the fundamental and the peak current through R_L. However, all PA topologies are most efficient when operating at their peak power, when the drain voltage experiences a full voltage swing of V_{DD}. Therefore, observing the Eq. 4.19 for a very low output power either V_{DD} has to be made very low, or R_{opti} must be made very high:

$$P_{1,max} = \frac{V_{DD}^2}{2R_{opti}} \tag{4.19a}$$

$$R_{opti} = \frac{V_{DD}^2}{2P_{1,max}} \tag{4.19b}$$

For example with $P_{1,max}$=-10 dBm, if the PA operates in class-B ($\alpha = \pi$) and for a V_{DD} = 1.2 V then R_{opti}= 7.2 kΩ.

At this point it is important to evaluate the impact of high R_{opti} on the MN efficiency. For sake of clarity the η_{MN} equation is reported here:

$$\eta_{MN} = 1 - \frac{Q}{Q_L} - \frac{Q}{Q_C} \approx 1 - \frac{\sqrt{\frac{R_{opti}}{R_s} - 1}}{Q_L} \tag{4.20}$$

Once that the MN is inserted, if the network presents no-losses that means Q_L close to infinity, the ratio $\frac{R_{opti}}{R_s}$ does not have any influences on the efficiency. However in real applications, as previously explained, the on-chip inductor exhibits a low quality factor and R_{opti} value strongly affects the MN efficiency. Expressing the power radiated from the antenna P_{rad} as:

$$P_{rad} = \frac{V_{RF}^2}{2R_s} \tag{4.21a}$$

$$R_s = \frac{V_{RF}^2}{2P_{rad}} \tag{4.21b}$$

where V_{RF} is the voltage swing across R_s, and equating the Eq. 4.18 and the Eq 4.21 the relation voltage-resistance is as follow

$$\frac{{V_{DD}}^2}{{V_{RF}}^2} = \frac{R_{opti}}{R_s} \tag{4.22}$$

According to the above equation the matching network efficiency can be expressed as

$$\eta_{MN} = 1 - \frac{Q}{Q_L} - \frac{Q}{Q_C} \approx 1 - \frac{\sqrt{\frac{V_{DD}^2}{V_{RF}^2} - 1}}{Q_L} \tag{4.23}$$

In the case of a standard value of 50 Ω for the antenna impedance, and for a PA operates in class-B, with P_{rad} = -10 dBm the voltage across the antenna resistance V_{RF} is about 0.3 V. Therefore, considering a supply voltage of 1.2 V and $Q_L = 10$ the $\eta_{MN} = 62\%$.
The Eq. 4.23 shows that to improve the global performances and to alleviate the matching network design a low supply voltage close to V_{RF} represents a good solution.

4.2.5 Comparison of different low power direct modulation transmitters

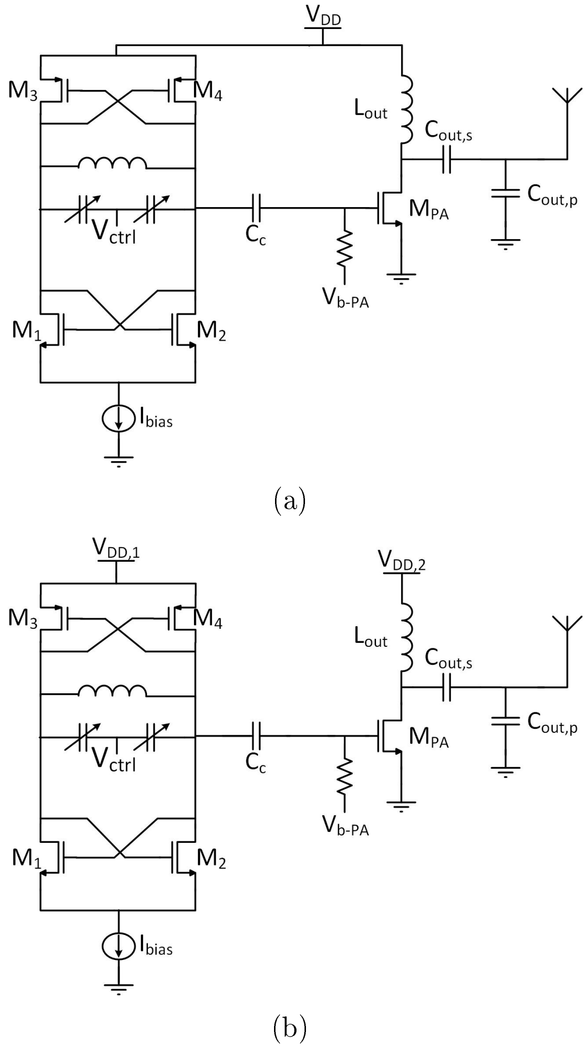
All the considerations carried out in the previous sections on the single building blocks (VCO, PA, MN), have been addressed by designing several topologies of direct modulation transmitters in a bulk 130 nm CMOS technology.
The goal is to transmit -15 dBm (about 32 μW) by keeping as low as possible the DC power consumption.
As previously introduced the VCO pulling phenomena is less problematic when the output power is very low. One of the main interaction between the PA and the VCO frequencies, when are harmonically related, can happen via capacitive signal coupling. In general to avoid frequency drift due to the output load changes, a buffer stage is interposed between the VCO output and the PA input to increase the isolation. As the power consumption increases consequently, and since the PA transistor provides sufficient isolation for the targeted output power the use of buffer stage can be avoided.
Following the previous considerations the two direct modulation transmitters depicted in Fig. 4.13 have been designed with two different supply voltage for the PA stage to demonstrate the better efficiency. Class-C PA and LC VCO are used for both the solutions.

4.2.6 Transmitter Design Steps

The first designed block is the PA and a class-C operating mode has been chosen to achieve high power efficiency. When operating in this mode the transistor is biased in sub-threshold region with a conduction angle (α) less than 180° Fig 4.14. Therefore the period where PA conducts is set by the DC voltage applied at the transistor gate and the overlapping sinusoidal gate voltage swing. It is clear that once all design aspects of the PA are established, the remain transmitter blocks (VCO) have to be designed in order to supply the required voltage amplitude at the PA input to proper set α and ensure the targeted output power.

Power Amplifier

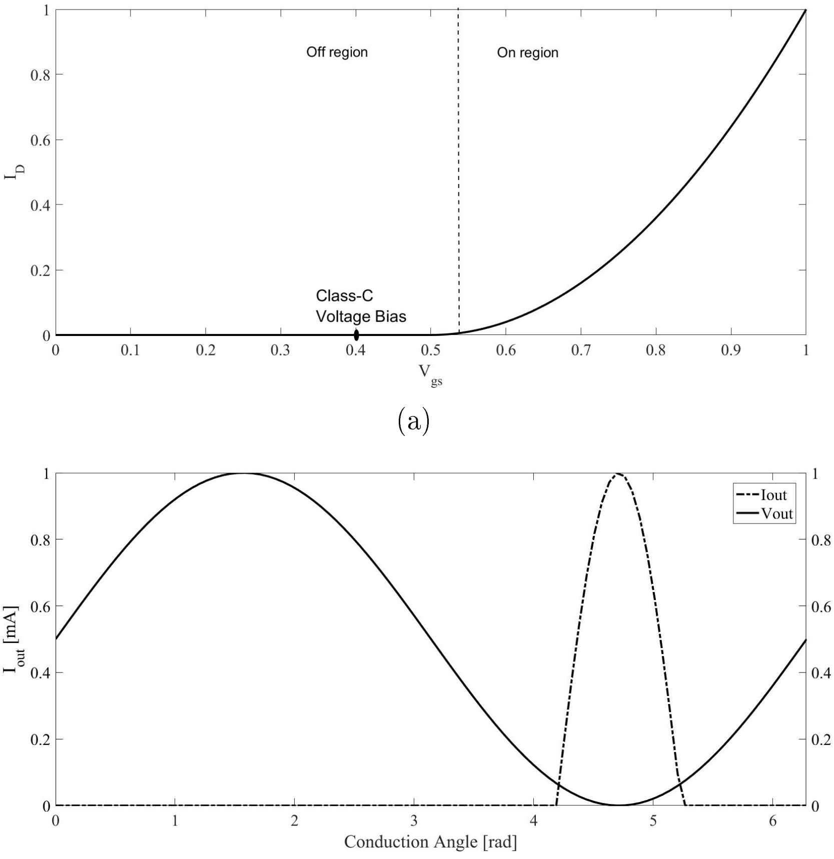
The PA design starts calculating the optimum output load resistor to ensure the maximum voltage swing admissible at the transistor drain $V_{o,max}$. In this way the mini-



(a)

(b)

Figure 4.13 – Transistor level schematic of direct modulation transmitters. Single voltage supply for both VCO and PA (a), double voltage supply to optimize the PA efficiency (b).



(a)

(b)

Figure 4.14 – Bias point to perform class-C operation mode(a) typical voltage and current waveforms at the transistor drain(b) Biasing the transistor at voltage lower than the threshold voltage permits to reduce the voltage and current overlapping period.

mum fundamental RF current (I_1) value is achieved and its DC terms I_{DC} consequently. Therefore the optimum load resistor can be founded from the Eq. 4.19. In this case a more general form is preferable:

$$R_{opti} = \frac{V_{o,max}^2}{2P_{1,max}} \tag{4.24}$$

The difference in the two equations comes from the fact that in Eq. 4.19 a maximum voltage swing of V_{DD} is supposed when the inductor works like a choke. The condition where the inductor carries only DC current and bypasses all the AC currents into the load is $\omega L_{choke} \gg R_L$ with a ratio of about 10. For example:

- For a full drain voltage swing of 0.8 V and considering the targeted output voltage of -15 dBm ($\sim$ 32 μW) the $R_{opti} = 10$ k Ω. Expressing the fundamental RF current as:

$$I_1 = \frac{V_{o,max}}{R_{opti}} \tag{4.25}$$

The peak drain current I_{max} and the DC current are equals to:

$$I_{max} = 2\pi I_1 \frac{1 - cos(\frac{\alpha}{2})}{\alpha - sin(\alpha)} = 2\pi \frac{V_{o,max}}{R_{opti}} \frac{1 - cos(\frac{\alpha}{2})}{\alpha - sin(\alpha)} \tag{4.26a}$$

$$I_{DC} = \frac{I_{max}}{2\pi} \frac{2sin(\frac{\alpha}{2}) - \alpha cos(\frac{\alpha}{2})}{1 - cos(\frac{\alpha}{2})} \tag{4.26b}$$

Taking a conduction angle of 150° $I_{max} = 158$ μA and the DC current is equal to 42.75 μA. However a voltage amplitude equal to V_{DD} would require L_{choke} of 6.5 μH which is impractical at 2.45 GHz even using off-chip components.

However for the designed PA the supply voltage of 0.8 V limits the swing to 0.4 V, because of the 1.2 V voltage forced by the MOS technology. This limitation affects the DC and the RF current:

- If $V_{o,max} = 0.4$ V the $R_{opti} = 2.5$ kΩ and for the same conduction angle of 150° the peak RF current is $I_{max} = 353$ μ A and $I_{DC} = 95.5$ μ A

The above considerations indicate that for the same output power, higher voltage swing at the output means higher load resistance but lower terms of RF current. Therefore the limit imposed by the MOS technology forces the transistor to work with higher drain current thus the PA does not operate at peak efficiency condition.

However the downside of high load resistance is represented by poor MN efficiency when high conversion ratio is needed. In the case of $R_{opti} = 10$ kΩ and considering the standard value of 50 Ω for the antenna impedance the Eq. 4.23 shows a negative value of η_{MN}, because the maximum quality factor Q_L achievable by the inductor is lower than the quantity $\sqrt{\frac{R_{opti}}{R_s} - 1}$. A practicable MN is possible when the $R_{opti} = 2.5$ kΩ, but a poor $\eta_{MN} = 42\%$ demonstrates the drawback of high transformation ratio that significantly impacts the overall performances. All these considerations are based on the fact that the inductor does not work like a choke and a practical value is possible.

The following items are some points to note in this case:

- The higher the ratio of impedance transformation the higher the Q of the transformation is. For a higher Q transformation, the intrinsic quality factor of the inductor in the network must be higher to minimize the losses in the network itself.

- When the transformation ratio is very high, it is sometimes better to do the transformation in multiple steps, but this also degrades efficiency of the network, and leads to more area.
- A trade-off between the power consumption and the matching network design appears when the power radiated is in the range of tens of μW. Fig. 4.16 shows the trends of I_{peak} and I_{DC} for three different values of R_L (2.5 kΩ, 1.25 kΩ, 0.60 kΩ) with the same output peak voltage of 0.4 V when the conduction angle moves from 10° to 180°. As illustrated, the peak currents increase when the load resistance decreases in order to keep constant the output voltage swing, and thus also the DC current increases consequently. Another important point is that the DC current decreases when the conduction angle decreases , while the peak current increases forcing the transistor to work in current capability limit.

The simple L-matching network in Fig. 4.15 demonstrates that a non-integrable on-chip inductor is needed to transform higher impedance to 50 Ω.

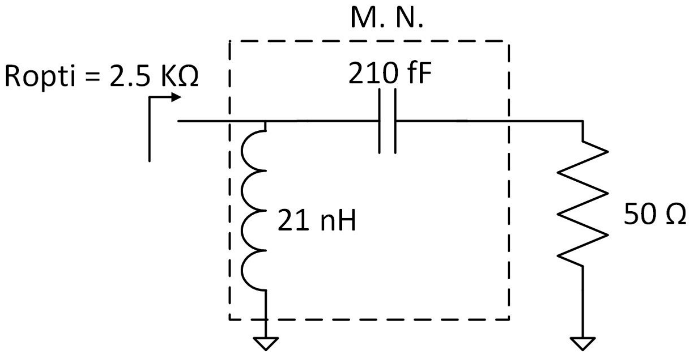
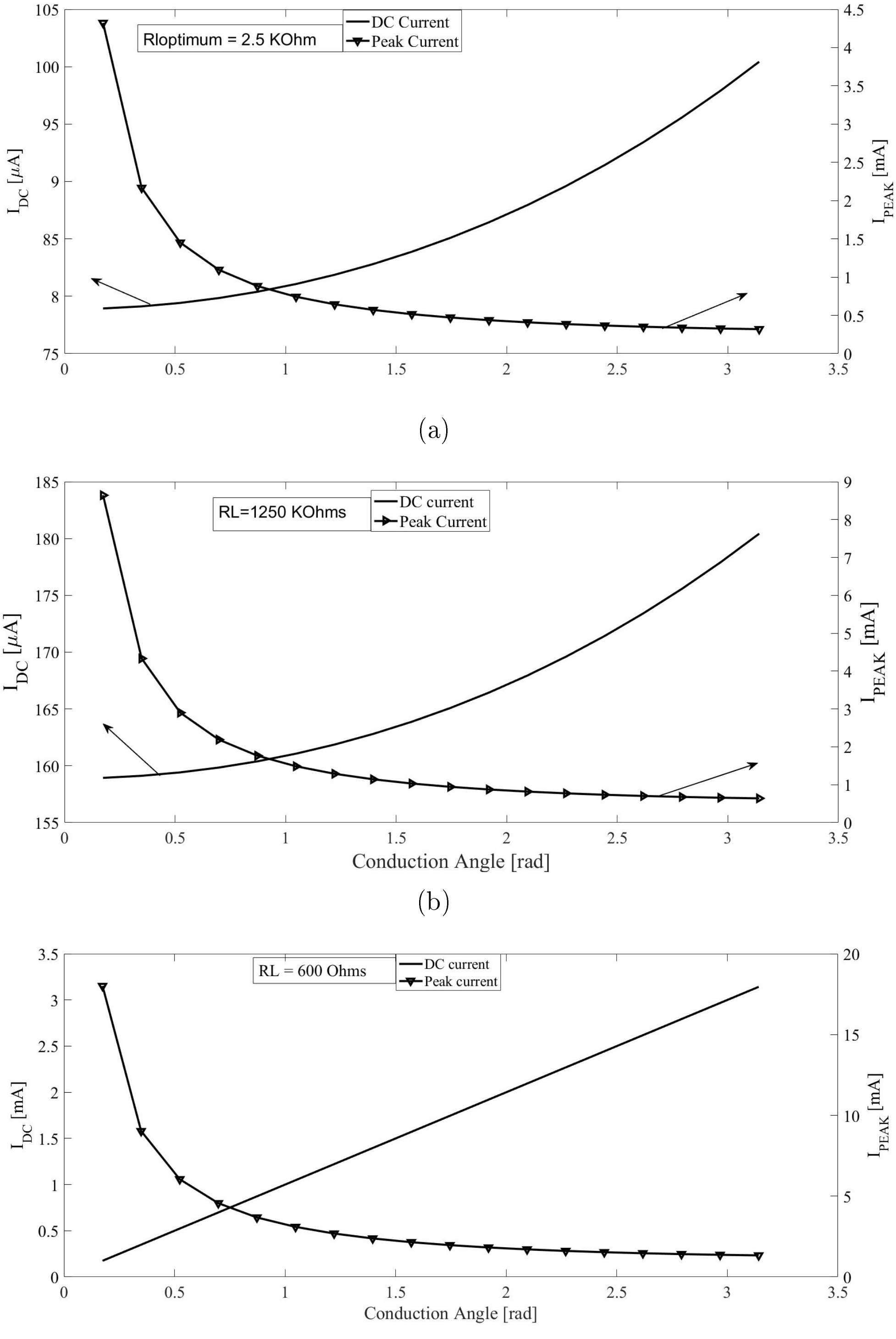


Figure 4.15 – Implementation of L-matching network to transform 50 Ω to the optimum load resistance of 2.5 kΩ. The large value of inductor makes difficult the integration of the passive element.



(a)

(b)

(c)

Figure 4.16 – DC RF current and Peak RF current depending on the conduction angle for three different output resistances and for a $V_{o,max} = 0.4$ V. The period of conduction refers only to class-C operating mode for 10°<α<180°.

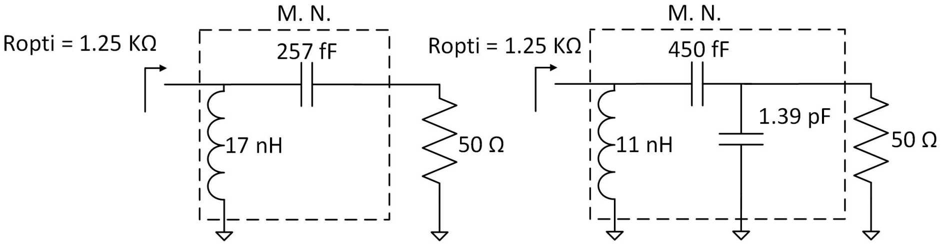


Figure 4.17 – Implementation of L-matching and π-matching networks to transform 50 Ω to the load resistance of 1.25 kΩ. A lower value of inductor is possible when a shunt capacitor is added to the network.

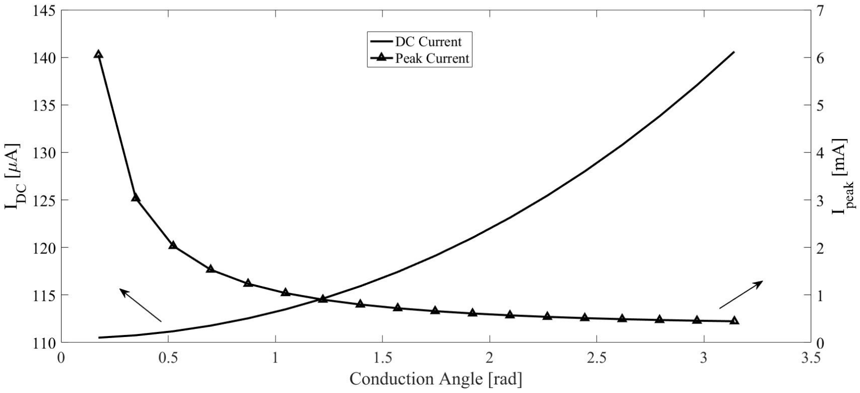


Figure 4.18 – DC RF load current and peak RF load current for $R_L = 1.25k\Omega$ and $V_{o,max} = 0.282V$ depending on conduction angle .

Since the application requires low power consumption the PA should be designed with the highest load resistance and low conduction angle to exploit the low range of DC RF current. However as the main limiting factor is the implementation of matching network, higher power consumption has to be accepted due to a lower load resistance.

To increase the network matching efficiency above 50% and to make feasible its implementation a load resistance of 1.25 kΩ is chosen. To present the correct impedance at the drain of MOS transistor and to filter the unwanted harmonics a π-matching network is used to transform 50 Ω to 1.25 kΩ. This MN performs a better integrability respect to a simple L-matching topology. As seen from the Fig. 4.17 the inductor value scales down from 17 nH to 11 nH and also the capacitor increases from 257 fF to 450 fF, making the MN less susceptible to the capacitive parasites.

Since the targeted power is equal to -15 dBm ($\sim$ 32 μ W) and with the constraint of R_L the peak output voltage is equal to $V_{o,max} = \sqrt{2R_LP_{out}} = 0.282V$. Once the load resistance is set, to perform a class-C power amplifier a conduction angle less than 180° has to be chosen. As explained previously the DC and the peak currents are affected when the conduction angle moves from 10° to 180°. To limit the peak current below 1 mA, it is possible to observe the trend of I_{RF} and I_{DC} from the Fig. 4.18 and $\alpha = 150°$ ($\approx$ 2.7 rad) is chosen that conducts to a I$_{DC}$ $\approx$ 132 μA. The transistor is sized taking in account the MOS efficiency and the required voltage swing at the gate. In fact this latter relates

Table 4.1 – Drain current terms of PA MOSFET for different channel width, for the same conduction angle and output power

Channel Width	$V_{g,DC}$	$V_{g,RF}$	I_{DC}	I_1	P_D
40 μm	310 mV	167 mV	319 μA	424 μA	-12.8
	290 mV	186 mV	298 μA	423 μA	-12.8
	270 mV	205 mV	281 μA	422 μA	-12.8
	250 mV	225 mV	272 μA	424 μA	-12.8
30 μm	310 mV	159 mV	295 μA	424 μA	-12.8
	290 mV	176 mV	280 μA	423 μA	-12.8
	270 mV	194 mV	270 μA	422 μA	-12.8
	250 mV	212 mV	263.7 μA	421 μA	-12.8
20 μm	310 mV	161 mV	274 μA	421 μA	-12.8
	290 mV	178 mV	267 μA	423 μA	-12.8
	270 mV	192.7 mV	260 μA	422 μA	-12.8
	250 mV	208 mV	255.7 μA	421 μA	-12.8

directly to the bias current of the VCO. The MOS efficiency can be expressed as

$$\eta_{MOS} = \frac{I_1 V_1}{2 I_{DC} V_{DD}} \tag{4.27}$$

The Tab. 4.1 is made performing several simulation for different channel widths, at the same output power and at the same conduction angle. The matching network is adapted for each size. The results show that the best MOS current ratio between the DC current and the fundamental current is achieved for the smallest size of 20 μm.
From the previously analysis the transistor channel width is 20 μm and it is biased at 290 mV with an signal amplitude of 178 mV. In this case the PA is in moderate Class-C operation, since that the threshold voltage is about 330 mV with a DC current of 267 μA. The higher I_{DC}, about two times higher than the value obtained from the previously analysis, is due mainly to overcome the loss into the MN.
Once all the PA characteristics are defined the design of the VCO is mainly focused to guarantee the optimum voltage swing at its output with good performances for current consumption and phase noise.

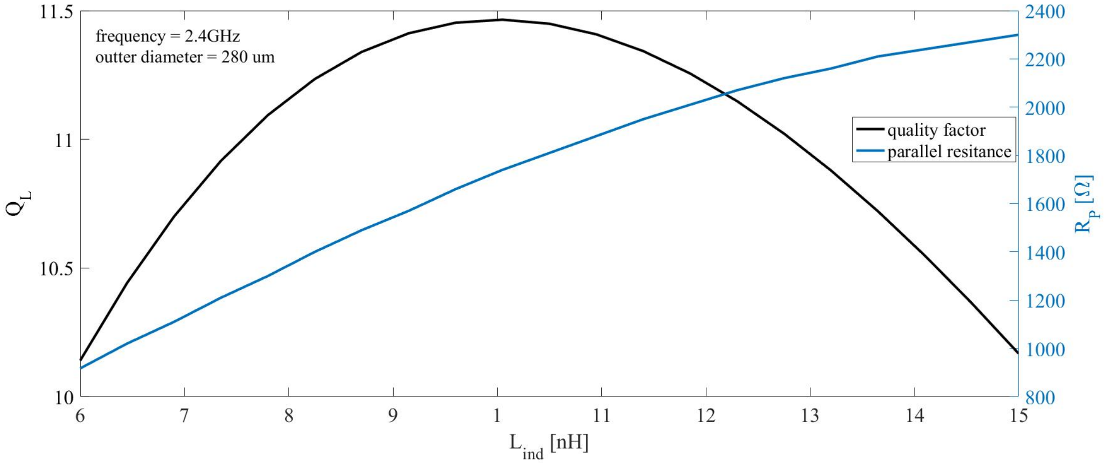


Figure 4.19 – Simulated quality factor Q_L and relative parallel resistance for different inductance values.

VCO implementation

The first design step for the LC VCO in Fig. 4.13 starts with the definition of the inductance parameters. As explained previously the best inductor is the one with the highest parallel resistance, since it will lead to the lowest required transconductance and hence consumption. Moreover high R_p value permits to increase the output voltage swing improving the phase noise performance. Therefore the differential output voltage swing can be expressed as

$$V_{out,diff} = \frac{4I_{bias}R_p}{\pi} \tag{4.28}$$

To find the appropriate inductance value the quality factor and the parallel resistance have been simulated for different values of L. Fig.4.19 shows the results when sweeping the inductance value from 6 nH to 15 nH at the frequency of interest of 2.4 GHz and for a constant outer diameter of 280 μ m. The simulations are related to a coil inductor width of 6.5 μ m and for a number of turns equal to 6. As expected from the Eq. 4.15 R_p increases with L, while Q_L exhibits a parabolic shape. In order to achieve the best ratio $\frac{Q_L}{L}$, the inductance value chosen is 10 nH that entails a R_p of about 1.7 kΩ. Considering a tolerance margin factor of 3 to ensure start-up condition against PVT variations the g_{mcrit} of the active part has to be greater than

$$g_{mcrit} > 1.8mS \tag{4.29}$$

However the main design criterion for the VCO is to ensure the voltage swing at its output which permits to drive properly the PA. The 535 mV of amplitude leads to a bias current of 240 μA. As the transistors exploit WI operation, the related transconductance can be found from the relation

$$g_m = \frac{I_D}{nV_T} \tag{4.30}$$

With the slope factor n = 1.5, the thermal voltage V_T = 26 mV and the drain current I_D = 120 μA the transconductance is g_m = 3.076 μS. This value is largely sufficient to ensure the start-up condition. Each cross-coupled PMOS transistors have a size of 60 μm/0.13

μm, while the NMOS pair has a size of 30 μm /0.13 μm. The tail transistor has a size of 120 μm/ 0.13 μm.
To tune the frequency of oscillation, two n-type accumulation mode MOS varactors are used. The variable capacitors are connected in parallel with the inductors. The tuning voltage V_{ctrl} is applied at the drain/source terminals. Some aspects have to be investigated to reduce the gate resistance and the tank losses consequently. To increase the varactor quality factor, the channel length has to be kept at the minimum value, while an high number of gate fingers allows to decrease the gate resistance. However the width of each fingers is a compromise between the quality factor, the parasitics and the varactor size.

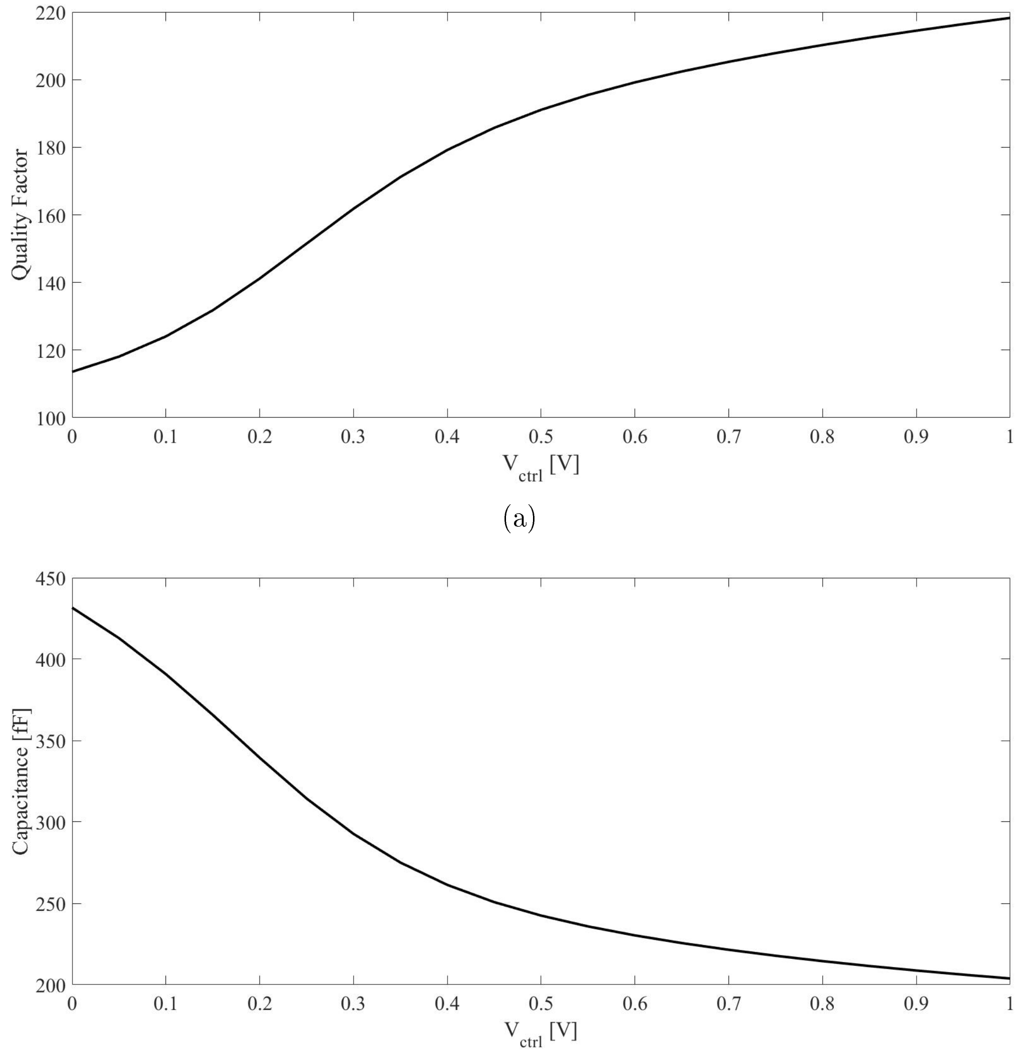


Figure 4.20 – Varactor quality factor (a) and capacitance versus tuning voltage (b)

The Fig. 4.20 shows the varactor quality factor and the capacitance for a tuning voltage from 0 to 1 V. The relative frequency range varies from 2.34 GHz to 2.59 GHz (Fig. 4.21), and the tuning range achieved is about 10%. The Phase noise is shown in Fig. 4.22 and results to be -115.2 dBc/Hz at 1 MHz from the carrier frequency. To evaluate the global performance of the designed VCO the accepted figure of merit FOM $= 20\log(\frac{f_{osc}}{\Delta f}) - L(\Delta f) - 10\log(P_{diss,watt})$ is used, where f_{osc} is the oscillation frequency, Δf the offset

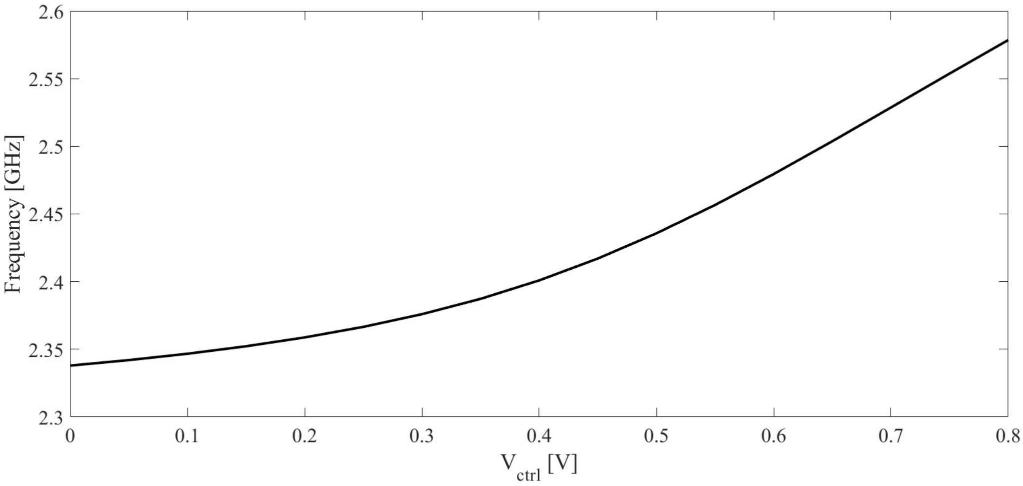


Figure 4.21 – Frequency range versus tunning voltage

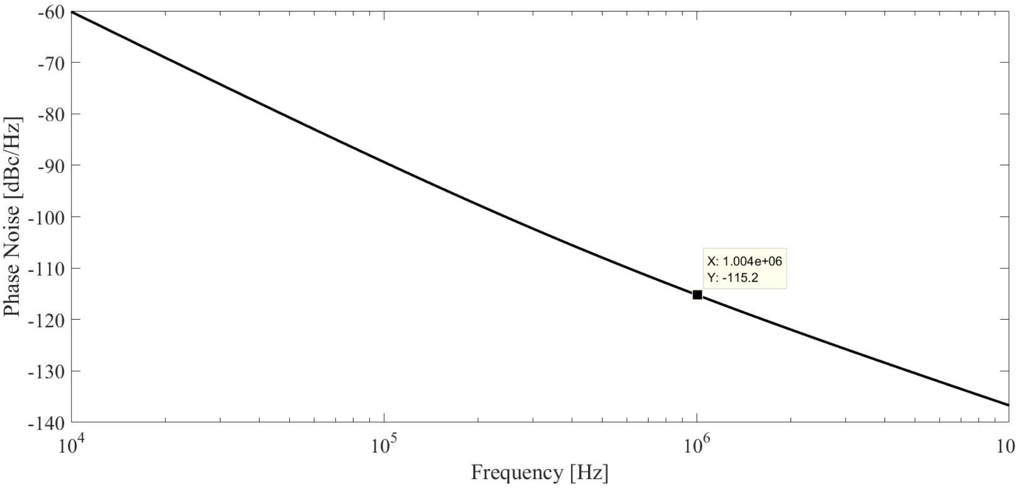


Figure 4.22 – Phase noise performance measured at 1 MHz from the carrier frequency.

frequency and L(Δf) the phase noise at the offset frequency at 1 MHz. The VCO presents the FOM equal to 200 dB.

4.2.7 Transmitter Simulation Results

Two transmitters have been designed to demonstrate the high efficiency when the PA is supplied with a low voltage. Therefore in the first one the VCO and the PA share a single supply voltage equal to 0.8 V, while for the second one the PA is supplied with V_{DD} = 0.4 V.

For both transmitters only DC-blocking capacitor is used to interface the VCO output to the PA input. This is sized to provide minimal capacitance dividing at the fundamental frequency.

- Single Supply Voltage

  In the transmitter supplied with a single V_{DD} the PA dissipates about 212 μW for a 15% of efficiency. Therefore the transmitter has global efficiency of 8%.

— Double Supply Voltage
  Since that the PA is supplied with lower voltage some modifications have been needed to achieve the best efficiency. The MOS transistor has a larger width (60 μm) and the matching network was adapted consequently. The PA transmits the signal with the same conduction angle of 150 ° that corresponds to a dc current of 301 μA. The power dissipated by the PA is now about 120.4 μW for a 26% of efficiency. As consequence the transmitter presents a better global efficiency about 10%.

The Monte Carlo simulations Fig. (4.23-4.24) were performed for the output power. In the case of single supply voltage the transmitter shows a mean of 28μW with a standard deviation of σ=8 μW. While for the double supply voltage the mean value is 31 μW with a standard deviation of $\sigma = 8.5$ μW.

In this section two direct modulation transmitters have been designed for -15 dBm output power, both transmitters are made up by CMOS voltage control oscillator and a class-C power amplifier. However the first one adopts a single $V_{DD} = 0.8$ V for both VCO and PA, while in the second one the PA is supplied with a low voltage $V_{DD} = 0.4$ V to improve the global efficiency. The trade-off between the optimum PA load resistance, the matching network and supply voltage is demonstrated. The simulation results prove that for the low output power a low V_{DD} relaxes the constraints on the matching network and higher efficiency can be achieved.

However the main drawbacks when two voltages are required is the greater complexity in the Power Management Unit due to the necessity of another voltage regulator and the increasing power consumption consequently. In the next section a very efficient transmitter is presented that permits to overcome the inconvenient described above.

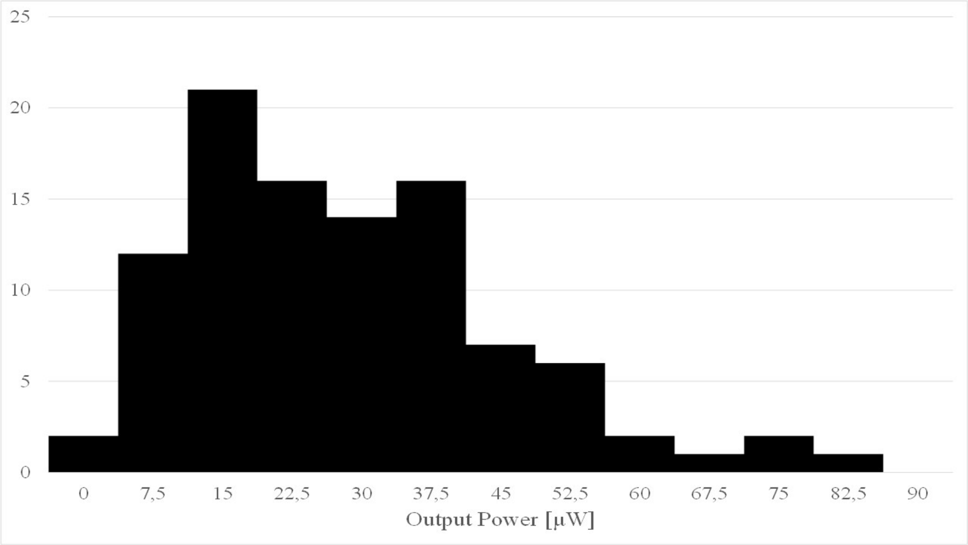


Figure 4.23 – Monte Carlo simulation on the single supply voltage transmitter output power with 100 runs.

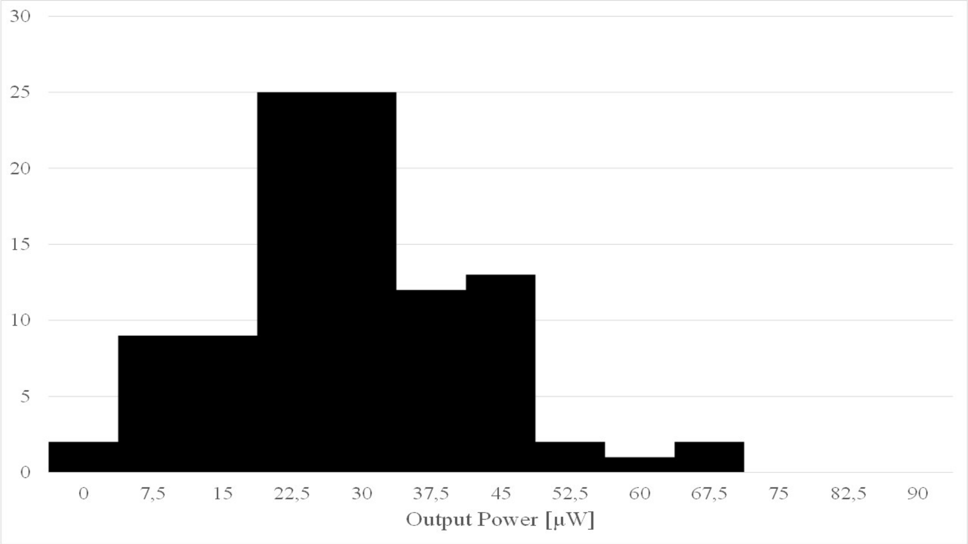


Figure 4.24 – Monte Carlo simulation on the double supply voltage transmitter output power with 100 runs.

4.3 Current Reuse Transmitter

In the previous section the issues about the supply voltage and the matching network at the PA output have been discussed. For very low output power a low V_{DD} was preferred to alleviate the MN and to improve the overall efficiency. However in this work the transmitter is supplied by the regulator described in the previous chapter, which presents an output voltage of 1 V. Surely this voltage does not match very well with the targeted output power of -15 dBm. Therefore to eliminate the necessity of a second regulator to supply an appropriate voltage for the power amplifier a current reuse transmitter has been design.
The idea is depicted in Fig. 4.25, where two possible topologies can be implemented depending if the VCO or the PA is stacked on the top or on the bottom.

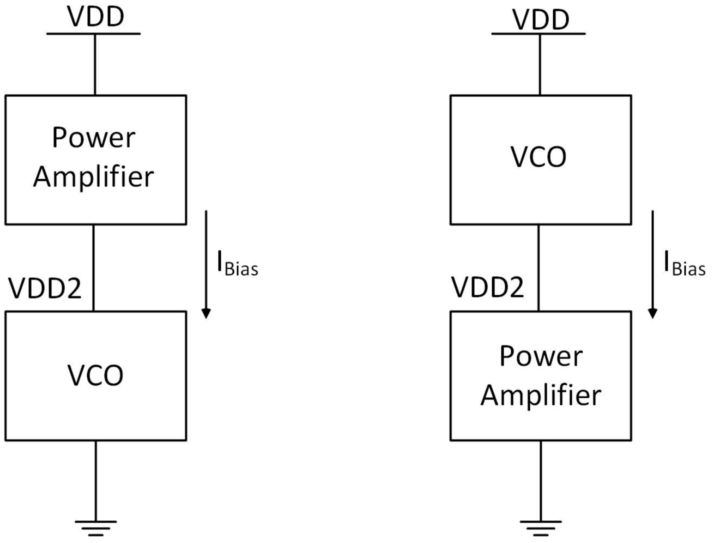


Figure 4.25 – Block diagrams of current reuse transmitter. The two possible solutions are reported depending on the position of the VCO and the PA

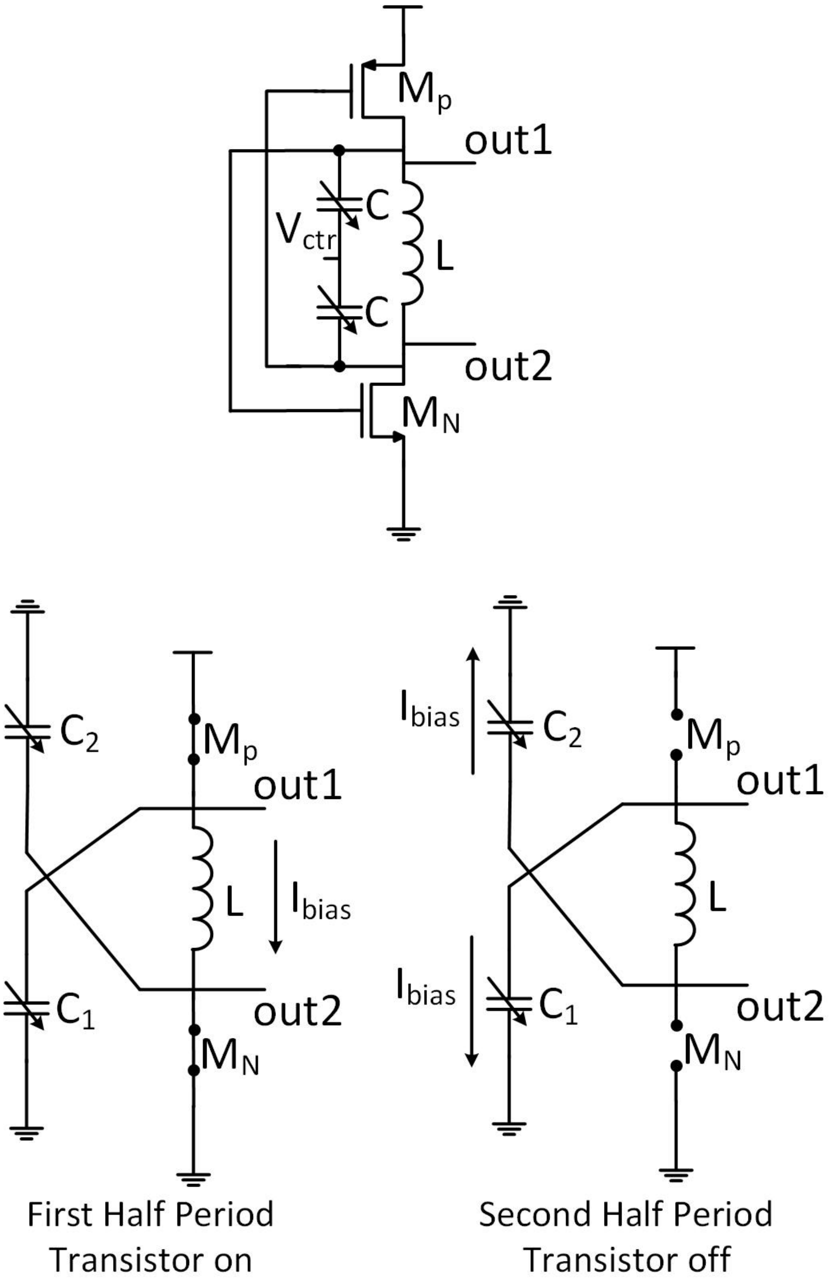
Two main features can be founded in stacked architecture. The first one is related to the total bias current that is recycled from the top block to the bottom one saving power. The second one is related to the supply voltage, since it can be splitted in two optimized voltages for each block. Therefore this architecture can solve the constraints for the targeted output power, where the supply voltage ratio between the VCO and the PA can be adjusted to reduce the required optimum resistance at the PA output.

4.3.1 Current Reuse VCO

The LC VCO implemented to generate the frequency carrier is a current reuse topology [YSCL05]. Fig. 4.26 shows the transistors implementation and the two operating states. The circuit is derived from a classical NMOS cross coupled oscillator, where one of the two NMOS transistors is replaced by a PMOS. Respect to the NMOS topology, the two transistors are on at the same time in the first half of oscillation period when the potential at $Vout_1$ is high. Therefore a direct path is created from the supply voltage and the ground through the transistors and the energy is stocked in the inductor. In the second half period, when V_{out1} is at low level, the (N- and PMOS) transistors are off and current flows through the capacitors. It is interesting to highlight that in the first half period the oscillator is in the voltage limited operation where the amplitude of the oscillation can extend up to V_{DD}. In the second state no limitation is present and the peak oscillation can exceed the supply voltage.Another remarkable point is that the same feature of CMOS cross coupled VCO can be founded in the current reuse topology. Since the transistors switch on at the same time the transconductance presented is twice of that NMOS cross coupled topology for the same bias current. Moreover the absence of the common source node avoids noise addition from the second harmonic term and improve phase noise performance due to a low flicker noise of the PMOS transistor.

However without some modifications, current reuse oscillator is not suitable for fully differential applications since that the output voltage swing is not balanced. The reason comes from the two different operating modes, in the first and in the second half period, and from the large drop in the dynamic current. To re-equalize the output a bias resistor can be added between the NMOS source and the ground, to force the VCO to operate in limited current mode in both periods.

However to work properly and to ensure start-up condition over PVT variations, the stacked topology has to be supplied with a voltage greater than the sum of PMOS and NMOS threshold voltage. For the RF transistors available in the design kit, V_{DD} should be higher than 0.85 V. At this point it seems clear that the 1 V of voltage supply for the transmitter architecture is not suitable to ensure sufficient voltage headroom for the PA and the VCO at the same time. To allow start-up condition also for low supply voltage the NMOS transistor can be biased separately to provide minimum negative resistance to sustain the oscillation [TGF12]. The Fig. 4.27 depicts the modified current reuse VCO, where the NMOS gate transistor is AC-coupled via C_{dec} to the node Y, and the R_{bias} represents the bias resistance. An ac-ground capacitor C_{AC} is needed to ground all high frequencies voltage bias components. However the ac-coupling capacitor and the bias resistor have to be properly sized to provide high enough start-up gain.



First Half Period
Transistor on

Second Half Period
Transistor off

Figure 4.26 – LC current reuse oscillator schematic.The two operating states are also illustrated for the two different oscillation periods.

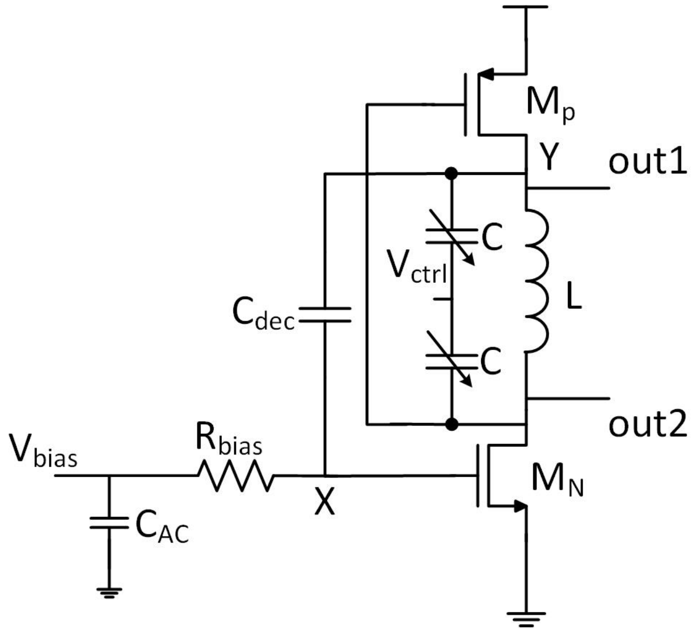


Figure 4.27 – Modified current reuse VCO for low supply voltage.

From the analysis done in [TGF12] the impedance seen at the node Y is expressed as

$$Z_Y = (\frac{1}{R_{bias,Y}} + |A_v|g_{mn} + g_{mp} - |A_V|g_{mn}g_{mp}R_p)^{-1} \tag{4.31}$$

where $R_{bias,Y}$ is the equivalent bias resistance seen at node Y to the ground, $A_v = \frac{V_X}{V_Y}$ is the voltage divider ratio between the node X and Y, R_p is the parasitic resistance of the tank. Since Z_Y has to be negative and high enough to ensure start-up condition, A_v has to be close to one. Considering the gate-source parasitic capacitance of NMOS transistor $C_{gs,nmos}$ the decoupling capacitor C_{dec} should be larger than the parasitic capacitance to ensure high voltage divider ratio.

If $C_{dec} \gg C_{gs,nmos}$ $R_{bias,y} \approx R_{bias}$, therefore to not degrade the tank quality factor R_{bias} has to be higher than R_p. However high value can degrade the phase noise performance due to higher thermal noise. Fig. 4.29 confirms this hypothesis, high value of R_{bias} corresponds to worst PN $R_{bias} = 4.5$ kΩ can represent a good trade-off. Fig. 4.28 plots A_V versus C_{dec}. It is worth noting that the voltage divider ration does not change significantly for $C_{dec} >$ 750 fF thus this value has been chosen.

Also for the current reuse oscillator the frequency tuning is ensured by two NMOS varactors and a 9 nH inductor with a quality factor of 12 at the oscillation frequency. Fig. 4.30 shows the phase noise at 1 MHz from the carrier frequency when the supply voltage moves from 0.6 V to 1 V. Fig. 4.31 shows the FoM and the power dissipation on the same supply voltage range.

In the next section the current reuse transmitter is presented, where the power amplifier stage is stacked on top of the VCO.

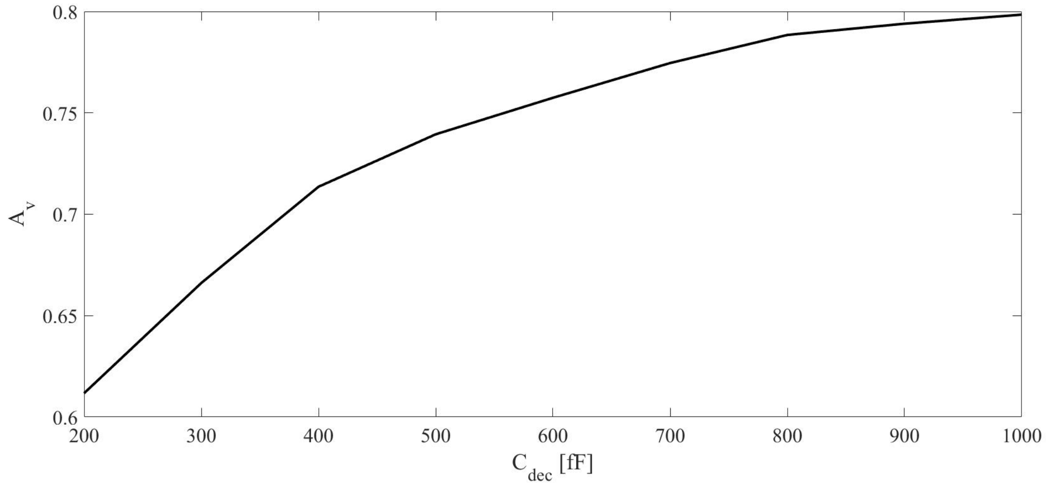


Figure 4.28 – Voltage divider ratio versus the decoupling capacitor C_{dec}

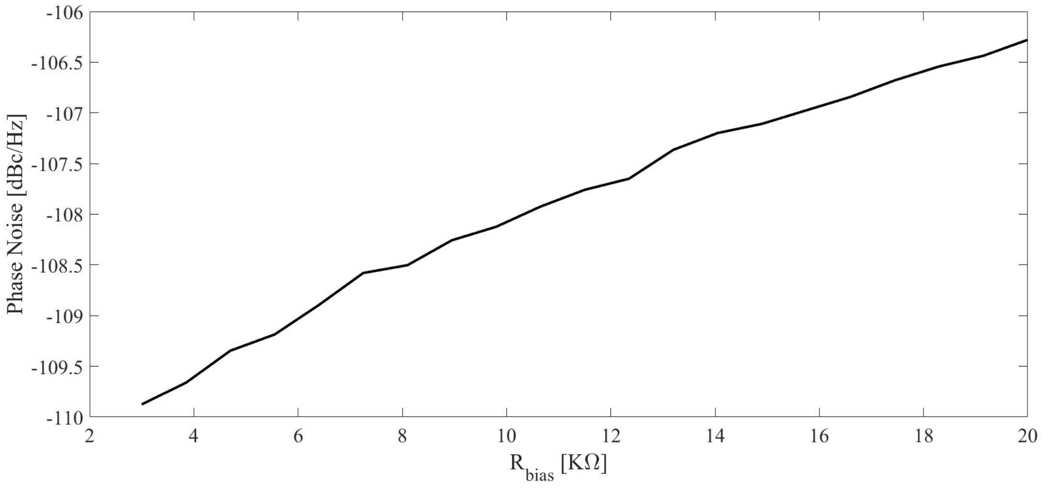


Figure 4.29 – Phase noise performance measured at 1 MHz offset from the carrier frequency versus the bias resistance.

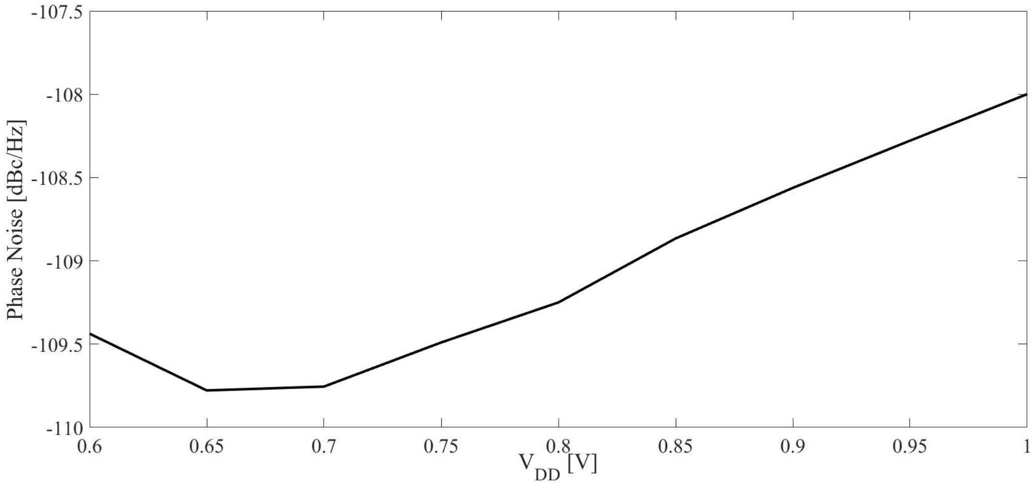


Figure 4.30 – Phase noise simulation at 1 MHz offset from the carrier frequency versus the supply voltage.

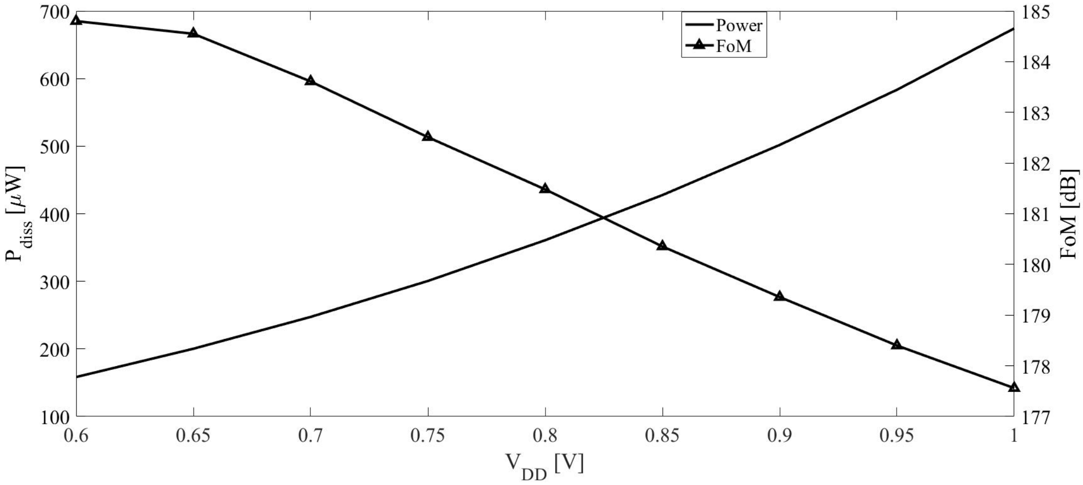


Figure 4.31 – FoM and power consumption for different supply voltage.

4.3.2 Designed current Reuse transmitter

The analysis done previously has demonstrated that 0.6 V external bias voltage V_{DD} ensures the start-up condition for CR-VCO . Therefore 1 V of supply voltage can be adopted for stacked topology since the PA for the targeted output power of -15 dBm achieves better efficiency when its supply voltage is in the range of few hundreds of millivolts.

The partition of the supply voltage depends on the bias voltage applied at the gate of the PA NMOS transistor. Taking as example the Fig 4.32 it is possible to write

$$V_{DD,VCO} = V_{bias} - V_{gs,Mn} \tag{4.32}$$

where $V_{DD,VCO}$ is the oscillator supply voltage, V_{bias} is the voltage applied to the gate of the NMOS transistor and $V_{gs,Mn}$ is its gate-source voltage. Depending on the $V_{DD,VCO}$ and the PA operating classes the V_{bias} has to be chosen accordingly.

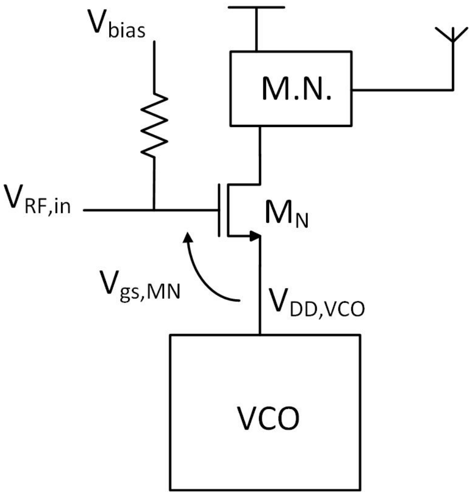


Figure 4.32 – Supply voltage trend.

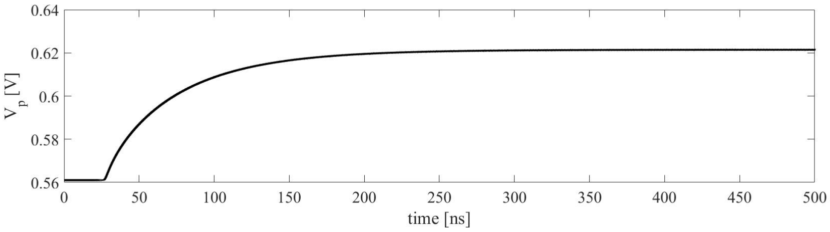


Figure 4.33 – Trend of the voltage at the common node P.

From the study carried out on about the power amplifier in classical transmitter topology and observing the trend of the CR-VCO FoM, the supply voltage about 0.65 V is chosen for the oscillator thus the remaining 0.35 V for the PA is an appropriate value for the M.N. trade-off.

The complete transistor level schematic is depicted in Fig. 4.34 where the PA is stacked on top to have the possibility to explore all PA operating classes and a better control on the output power. To implement current reuse topology and to shunt all AC components avoiding possible high frequency loop and providing a virtual V_{DD} to the VCO, a shunt capacitor of 20 pF is inserted at the PA and VCO common node. In the Fig. 4.33 the trend of the voltage at node P over the time is depicted, since the VCO and the PA are two large signal circuits V_p achieves final value when the oscillation is settled.

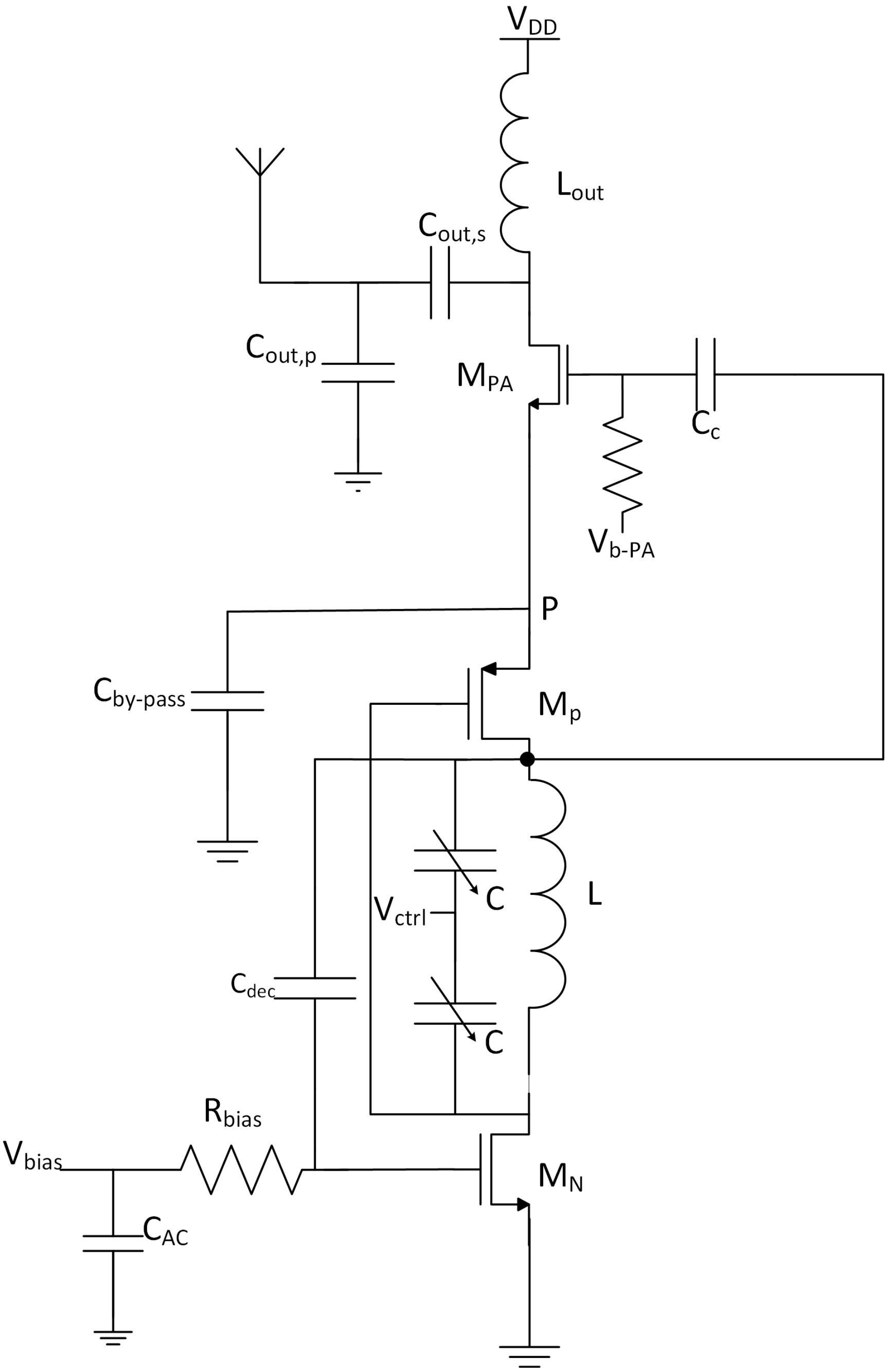


Figure 4.34 – Transistor level schematic of Current Reuse transmitter.

Table 4.2 – Devices size for the designed transmitter.

	Value
L_{out}	7 nH
$C_{out,s}$	450 fF
$C_{out,p}$	1 pF
M_{PA}	$\frac{50}{0{,}13}\frac{\mu m}{\mu m}$
L	10 nH
M_p	$\frac{60}{0{,}13}\frac{\mu m}{\mu m}$
M_N	$\frac{40}{0{,}13}\frac{\mu m}{\mu m}$
C	600 fF
V_{bias}	400 mV
$C_{by-pass}$	20 pF

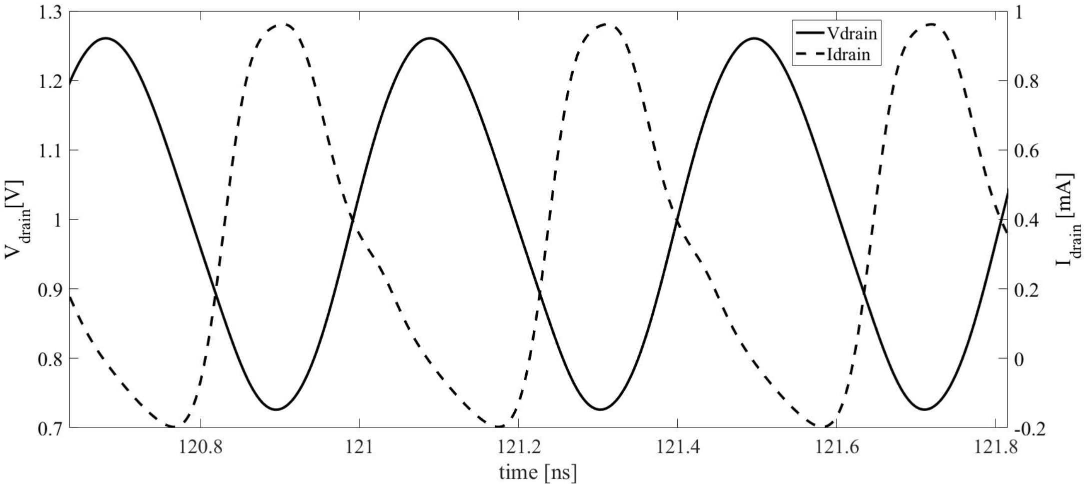


Figure 4.35 – Voltage and Current transient at the M_{PA} drain.

Once the supply voltages for the two blocks are fixed the design methodology is as follow:

- The transmitter bias current is fixed by the targeted output power, by the feasible load resistance (as explained in the previously section) and by the PA operating class with the Eq. 4.25-4.26.
- With the current value the VCO tank inductor is chosen to have sufficient voltage swing at the M_{PA} gate, in order to set the conduction angle properly. The relation can be seen from the Eq. 4.28.
- The relative parasitic inductor resistance fixes the minimum $g_{m,crit}$ necessary to sustain the oscillation. The $g_{m,crit}$ is assured setting the bias voltage of CR-VCO V_{bias} and sizing the transistors M_p and M_N.

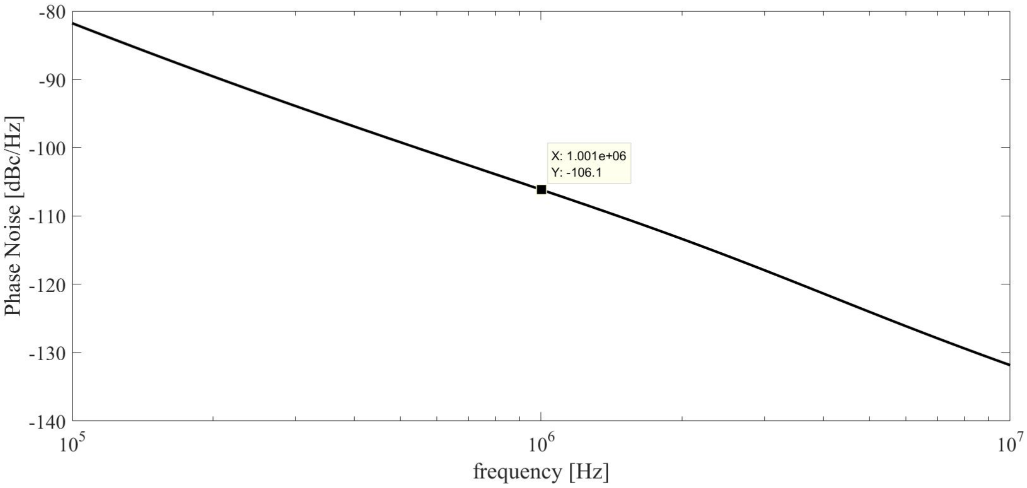


Figure 4.36 – Phase noise simulated at 1 Mhz from the carrier frequency.

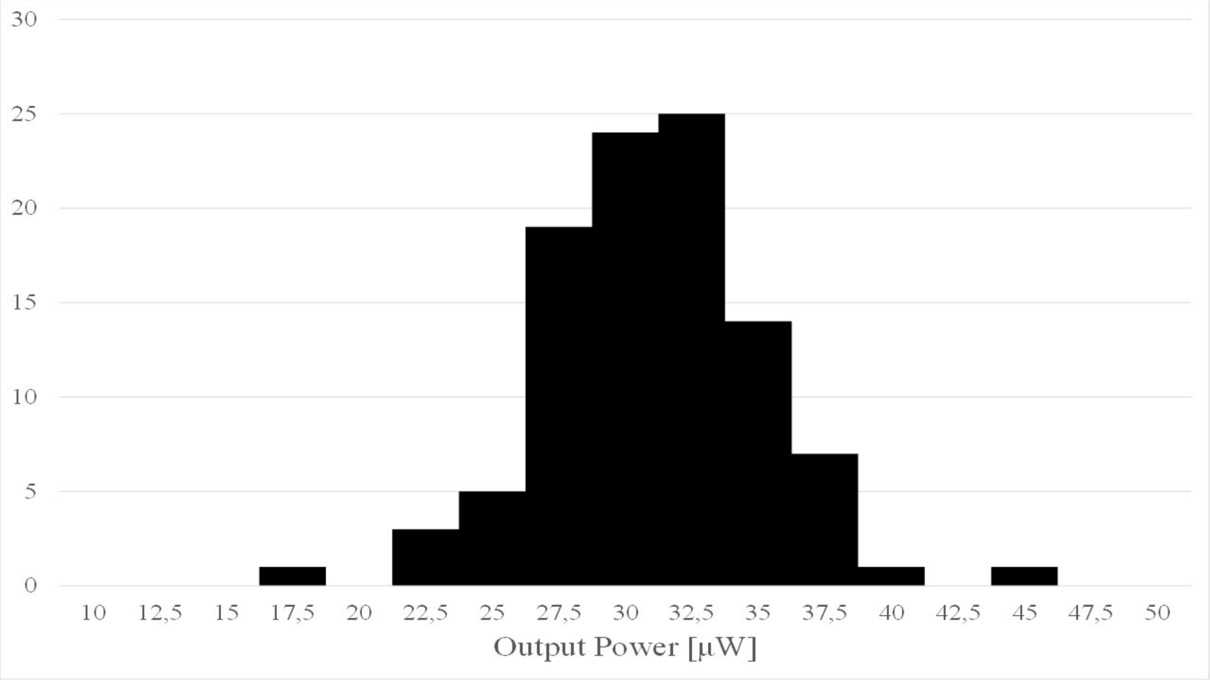


Figure 4.37 – MonteCarlo simulation performed over output power.

The Tab 4.2 summarizes the final values for the transmitter devices. The bias current needed to transmit -15 dBm is about 310 μA for a total power dissipation of 310 μW. The Fig 4.35 shows the transient behavior of current and voltage drain of the power amplifier while the Fig. 4.36 shows the phase noise at 1 MHz from the carrier frequency. The current reuse transmitter exhibits a total power efficiency of 10.5 %.
Fig 4.37 shows the Monte Carlo simulation performed for the output power. The transmitter shows a mean of 32 μW with a standard deviation of $\sigma = 4$ μW.

4.4 Conclusion

In this chapter a design methodology for transmitter in short communication distance has been presented. The output power of -15 dBm entails that the approach should be different from the traditional approach adopted to design long distance transmitter. To achieve low power consumption a direct modulation scheme has been adopted to reduce the number of blocks needed for the transmission.

In the first part of the chapter two classical transmitters have been presented where the voltage control oscillator and the power amplifier are cascaded. The discussion mainly focused on the difficulty to transform the preferably high load resistance, when the power transmitted is about few tens of micro-watt, to the standard 50 Ω input antenna impedance. The trade-off between the supply voltage, the bias current and matching network efficiency have been demonstrated. To show the advantages when the PA is supplied by a lower voltage two transmitters have been designed. In the first one the VCO and the PA share the same supply voltage of 0.8 V, in the second one the VCO maintains the same voltage while the PA is supplied with a voltage of 0.4 V. However a double supply voltage requires another voltage regulator, that means more power dissipated and more complex system.

To circumnavigate this problem, a current-reuse transmitter has been proposed where the VCO and the PA are stacked and the bias current is recycled from the top circuit to the bottom one. The possibility to distribute a single supply voltage in two optimized voltage one for each block offers several degree of freedom for targeted output power, phase noise and power consumption. Moreover for this topology only one voltage regulator is needed reducing the complexity of the system.

Chapter 5

Conclusions

This work investigates the design of ultra-low power circuits for Harvesting applications, in particular LDO voltage regulator and transmission part are involved in the study. To address the design, the first part of dissertation presents the low-power techniques at three different levels: transistors level, circuit level and system level.
In addition the main sources of energy Harvesting are presented outlining the energy available at their output and the level of integration. As the application targeted is the possibility to replace battery with EH source in wireless sensor networks in order to extend the operation lifetime, some system aspects are presented. From the networks architecture to the link budget, data-rate and energy management aspects. These lasts are fundamental aspects to take into account to give the circuit specifications. Moreover the equation to estimate the optimum DC for the lowest energy consumption is given.
Chapter 3 shows that to reduce the regulator power consumption even beyond to use the Mosfet transistors in Moderate Inversion, the better way to reduce the energy budget is to adapt the quiescent current to the load current of the LDO voltage regulator. With the class-AB Error Amplifier and an adaptively bias approach also the transient response is improved. Therefore the LDO exhibits a quiescent current that spans from 560 nA to 1.8 μA when I_{load} moves from 1 μA to 1mA. While the time response is halved. The regulator is designed to transform a variable input voltage of 1.2 V in a stable output voltage of 1 V.
Two architectures for the transmission part are proposed in chapter 4: a classical cascaded topology VCO-PA and a current reuse transmitter. As the radiated power is in the range of some μW, there is a severe trade-off between the matching network efficiency and the power amplifier supply voltage. The achieve a global power efficiency about 10% the oscillator and the amplifier, in cascaded topology, are supplied with two dedicated voltages of 0.8 V and 0.4 V. To avoid two voltage regulators which increases system complexity, the current reuse permits to tune unique voltage supply between the VCO and the PA alleviating the design constraints for the matching network. Therefore a comparable efficiency of 10.5% is obtained. Moreover Montecarlo simulations demonstrate that current reuse topology is more robust against PVT variations.

Perspective

To validate the obtained simulation results, the circuits realization and its measurements are the obvious steps to do consequently. More interesting would be the possibility

to test the circuits in a more complex system, where the signal modulation incoming from the analog-to-digital convert.
As the regulator presents important dependence PVT variations, an additional circuit to adjust the error amplifier bias current could represent a solution to mitigate these effects.
From the transmission side, to improve the spectrum efficiency of the signal radiated a low-power FSK modulation could be easily implemented.

Appendix A

Drain current calculation in class AB Error Amplifier

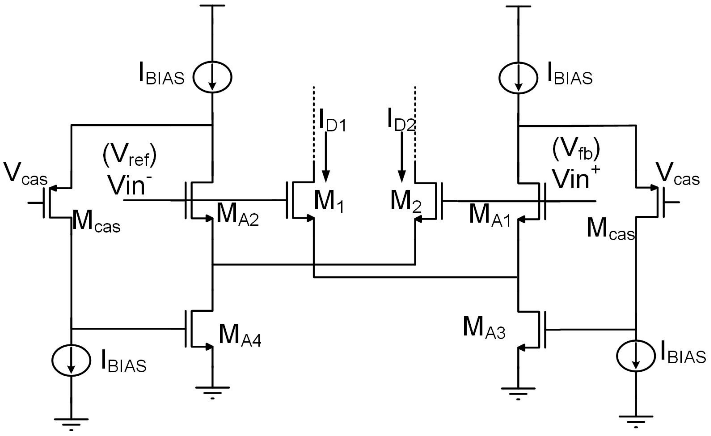


Figure A.1 – FVF cell with cascode Pmos transistor

Since that the transistors M_1, M_2, M_{A1}, M_{A2} operate in sub-threshold the drain currents are expressed as

$$I_{DS,M1} = I_{D0,M1}(\frac{W}{L})_{M1} \exp\left(\frac{V_{gs,M1} - V_{TH}}{nV_t}\right) \tag{A.1a}$$

$$I_{DS,M2} = I_{D0,M2}(\frac{W}{L})_{M2} \exp\left(\frac{V_{gs,M2} - V_{TH}}{nV_t}\right) \tag{A.1b}$$

$$I_{DS,MA1} = I_{D0,MA1}(\frac{W}{L})_{MA1} \exp\left(\frac{V_{gs,MA1} - V_{TH}}{nV_t}\right) \tag{A.1c}$$

$$I_{DS,MA2} = I_{D0,MA2}(\frac{W}{L})_{MA2} \exp\left(\frac{V_{gs,MA2} - V_{TH}}{nV_t}\right) \tag{A.1d}$$

The gate source voltage of M_1 and M_2 is equal to

$$V_{gs,M1} = V_{in}^{-} - V_{s,M1} = V_{in}^{+} - V_{s,MA1} \tag{A.2a}$$

$$V_{gs,M2} = V_{in}^{+} - V_{s,M2} = V_{in}^{+} - V_{s,MA2} \tag{A.2b}$$

From Eq. A1c and A1d the source voltages V_{sA1} and V_{sA2} are equal to

$$V_{s,MA1} = -\log\left(\frac{I_{MA1}}{I_{D0,MA1}(\frac{W}{L})_{MA1}}\right)\eta V_T + V_{in}^{+} - V_{TH} \tag{A.3a}$$

$$V_{s,MA2} = -\log\left(\frac{I_{MA2}}{I_{D0,MA2}(\frac{W}{L})_{MA2}}\right)\eta V_T + V_{in}^{1} - V_{TH} \tag{A.3b}$$

Substituting eq A3a and A3b in A2a and A2b, and then in the A1a and A1b the drain current of transistors M_1 and M_2 is equal

$$I_{D1} = I_{DO}\left(\frac{W}{L}\right)_{M1}\exp\left[\log\left(\frac{I_{DA1}}{I_{DO}\left(\frac{W}{L}\right)_{MA1}}\right) - V_{diff}\frac{1}{V_T n}\right] \tag{A.4a}$$

$$I_{D2} = I_{DO}\left(\frac{W}{L}\right)_{M2}\exp\left[\log\left(\frac{I_{DA2}}{I_{DO}\left(\frac{W}{L}\right)_{MA2}}\right) + V_{diff}\frac{1}{V_T n}\right] \tag{A.4b}$$

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