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POUR OBTENIR LE GRADE DE
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SPÉCIALITÉ: ELECTRONIQUE

Par Ali Mohsen

Harmonic Feedback Multi-Oscillator for 5G Application

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Soutenue le 13 décembre 2018

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Glossary:

1G	First Generation of Wireless Cellular Technology
2G	Second Generation of Wireless Cellular Technology
3G	Third Generation of Wireless Cellular Technology
4G	Fourth Generation of Wireless Cellular Technology
5G	Fifth Generation of Wireless Cellular Technology
BEOL	Back-End of Line
CAD	Computer Aided Design
CMOS	Complementary Metal-Oxide-Semiconductor
CP1	1 dB Compression Point
CPW	Coplanar Wave Guide
CS	Common Source
DIBL	Drain Induced Barrier Lowering
DRC	Design Rules Check
ESR	Equivalent Series Resistance
FBB	Forward Body Bias
FD-SOI	Fully Depleted Silicon on Insulator
FET	Field-Effect Transistor
FFO	Fundamental Feedback Oscillator
f_{\max}	Maximum Oscillation Frequency
f_t	Transit Frequency
g_{ds}	Source-Drain Conductance
g_m	Trans-conductance
HFO	Harmonic Feedback Oscillator
HFMO	Harmonic Feedback Multi-Oscillator
IC	Integrated Circuit
ICP1	Input 1 dB Compression Point
IoT	Internet of Things
ITRS	International Technology Roadmap for Semiconductors
ITU	International Telecommunication Union
LNA	Low Noise Amplifier
LNPA	Low Noise Power Amplifier
LVT	Low Voltage Threshold
M2M	Machine-to-Machine
MAG	Maximum Available Gain
MIMO	Multiple-Input Multiple-Output
mm-wave	Millimeter wave
MOM	Metal Oxide Metal
MSG	Maximum Stable Gain
NF	Noise Figure
OCPI	Output 1 dB Compression Point

PA	Power Amplifier
PAE	Power Added Efficiency
PCB	Printed-Circuit Board
PDC	Consumed DC Power
Pin	Input Power
PLS	Post-Layout Simulation
Pout	Output Power
Psat	Saturated Output Power
RBB	Reverse Body Bias
RF	Radio-frequency
RVT	Regular Voltage Threshold
SoC	System on Chip
SOI	Silicon on Insulator
SS	Sub-threshold Slope
TL	Transmission Line
URLLC	Ultra-Reliable Low Latency
UTBB	Ultra-Thin Body and Buried oxide
VCO	Voltage Control Oscillator
Vth	Threshold Voltage

General Introduction

The 5G rising is on the horizon. As we embark on the road to 5G, the next-generation wireless communications system, there are countless challenges and opportunities emerging for the engineering community. 5G represents both an evolution and a revolution of mobile technologies that reaches the various high level goals. It is widely seen as the generation of wireless that will enable cellular to expand into a completely new set of use and connectivity for a wide range of new applications as smart home, autonomous cars, smart city, and internet of things... These demands motivates the work on mm-wave frequencies, which imposes increasing the specifications and standards of each block. One of the most important blocks in wireless technology is the oscillator. The performance of the oscillator, which is characterized by the phase noise parameter, can dictates the whole communication system performance. This work will present a new architecture of oscillator for the 5G application using the 28 nm UTBB FD-SOI technology from STMicroelectronics. It composed of four chapters.

Chapter 1 will cover the topics of 5G applications, specifications, and bands to be considered. Then it passes to the mm wave transmitter to go deeply inside to the oscillator block then define the phase noise parameter. It discusses the types of LC oscillator used in mm-wave bands. Each type is provided with real examples, and measurement values, in order study the performances of each technique used. A state of arts will be labeled for each type. Then the idea of fundamental feedback oscillators will be presented showing its drawbacks and compare it with the enhanced edition of that which is the harmonic feedback oscillator, showing its improvements on phase noise, frequency-pulling effects, and on behavior with load impedance variation. Then the new architecture will be introduced, which is the harmonic feedback multi-oscillator, showing its improvements over the FFO and the HFO.

Chapter 2 will discuss the technology and the building blocks issues used in the HFMO. First, it covers the bulk CMOS limitation in 28 nm transistor scale and the alternative transistors showing the performances and enhancement of the 28 nm FD-SOI technology in mm-wave applications. The second part is about the power amplifier design parameters, architectures, and classes, which the HFMO is based on. The last part of this chapter is showing the architecture and specifications of the proposed power oscillator HFMO.

Chapter 3 will shows the design steps of each part in the power oscillator system. The overall results of the oscillator is then compared with other oscillators working on the same mm-wave band. Finally, in chapter 4, the work ends with a general conclusion, which provides an overview of the thesis and perspectives for future works.

Chapter 1 : Background from 5G towards Oscillators

1.1 Mobile Technology: an overview

In just 20 years, mobile phone networks have experienced a profound transformation from the second generation 2G (speech communication), the third generation 3G (voice communication and data transfer), to the fourth generation 4G (communication and broadband data transfer). Indeed, a phone designed originally to perform a voice conversation between two users without providing any other service that is to send/receive text message, the modern smartphone has become today a center of data access to a big number of services and applications as games, cameras, economic transactions, internet browser... This generalization of the internet access, via the smartphone and the arrival of video calls grow and keep straight ahead.

The flow of communication started with the invention and development of scientist theories. It started with the theory of "On a Dynamical Theory of the Electromagnetic Field" in 1865 and "A Treatise on Electricity and Magnetism" in 1873 for the Scottish scientist James Clerk Maxwell that named now a day as Maxwell equations. Maxwell equations explain the movement of the electromagnetic waves in a free space, but they were mathematically complex until Oliver Heaviside simplify them by introducing the vector notation and apply them on practical applications as guided waves and transmission lines in 1887. Then, the German physicist Heinrich Hertz prove and validate the theories of electromagnetic waves introduced by Maxwell by a set of experiments in 1891.

Nikola Tesla, a Serbian scientist and inventor, is one of the few individuals that is rarely discussed accredited with major technological advancements. He is the first one who think and apply a wireless transfer of energy without data (power transfer), then he invented the radio wireless communication, which is falsely attributed to an Italian engineer Guglielmo Marconi in 1895 since Nikola Tesla was not submitting his patents to be under his name. Then the microwave enter a freezing stage until the start of World War II that make the wireless communication under field of interest. Most of the nations who participate in the World War II developed the radar system independently which launch the analog communication technique.

The first generation of mobile communication, which was mostly analog wireless system, introduced in 1979. The second-generation 2G mobile networks and the digital switchover with the creation of the GSM standard has introduced new services of transfer of data such as SMS (Short Message Service). Nevertheless, the 2G could not yet respond to the request for access to the internet from mobile phones. This has motivated the development of 3G, which came on the market in 2001 with the first smartphones. Then in 2009, data transfer rates much greater than those of 3G was achieved with the definition of 4G video calls and much larger file transfer.

However, the 4G network cannot meet the growing demand of the number of connected objects. That is why the mobile phone industry chose to develop the network of fifth generation 5G to provide a technical solution to the problem faced by the 4G today.

The 5G will not be an evolution of 4G, rather it will be a full new mobile system; it will be faster, reactive for real time services, connecting people, objects, cars...going toward digitizing the society.

1.2 Fifth generation 5G

1.2.1 5G applications and specifications

Before talking about the specifications of this network, it is necessary to be interested in the evolutions in the world market communications between today and 2020. In their annual report, the Cisco analysts detail their projections for the period 2015-2020. Several predictions are particularly interesting. The first concern is the number of objects connected to an IP network [1] [2]. In 2014 we had 14 billion objects connected to an IP network, in 2019 this number will exceed 24 billion, increase of 10 billion in 5 years as shown in Figure 1-1.

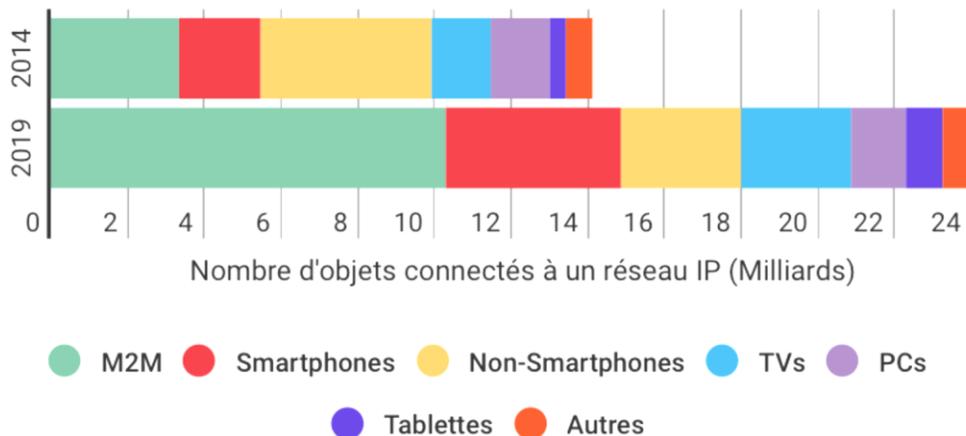


Figure 1-1. Evolution of the number of devices connected to an IP network [1]

The second concern is the number of the wireless connected objects to the mobile network [3]. This number will increase from 7.9 billion in 2015 to 11.6 billion in 2020, an increase of 4 billion in 5 years. In Figure 1-2, it can notice that the share of smartphones objects will exceed 40% by 2020; an increase of 12% compared to 2015.

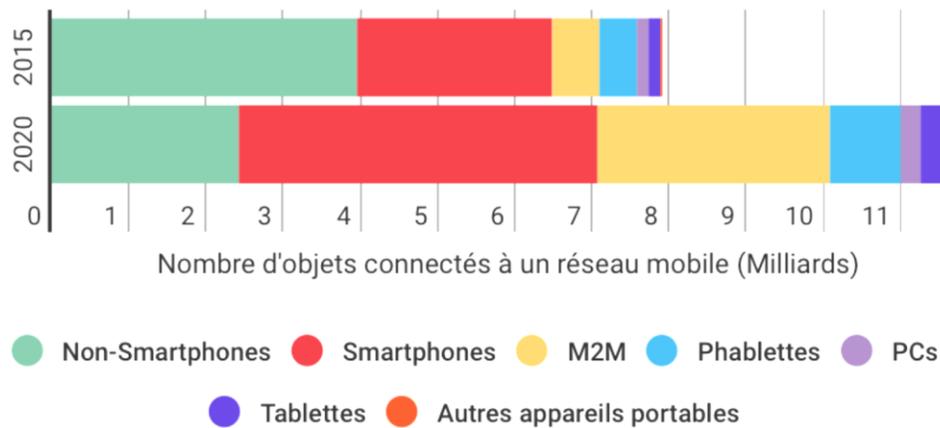


Figure 1-2. Evolution of the number of devices connected to a mobile network

The 5G will provide connectivity for a wide range of new applications as home automation, autonomous car, E-Health, smart City, virtual realities with high definition, industrial process control, entertainment, gaming, and internet of things (IoT). These applications have very different connectivity needs: whereas virtual reality requires a lot of bandwidth to provide a good user experience, autonomous vehicle communications must be reliable and almost instantaneous to be able to mitigate the risks of traffic accidents. IoT (Internet of Things) requires a network capable of communicating simultaneously with a large number of objects, while consuming very little energy to ensure a long battery life.

To meet these heterogeneous needs, International Telecommunication Union ITU [4] has defined three main categories of performance for 5G to be achieved:

- **eMBB:** enhanced Mobile Broadband, meeting very high speed needs
- **URLLC:** Ultra Reliable Low Latency Communications, Addressing Ultra-Fast and Reliable Connection Requirements
- **mMTC:** Massive Machine Type Communications, which concerns communications related to connected objects.

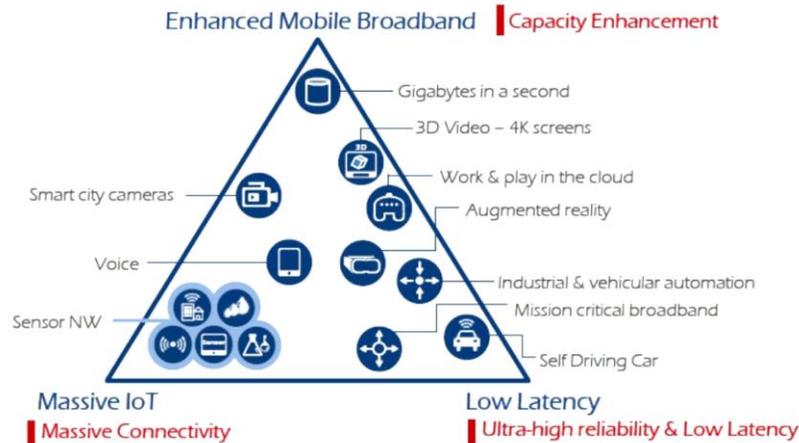


Figure 1-3. The three main categories of 5G [4]

The eMBB is for all applications and services that require connection always faster, for example to allow watching videos in ultra-high definition (8K) or wireless "streamer" virtual reality or augmented reality applications. The Ultra-low latency communications (uRLLC) are all applications requiring extremely high reactivity and a very strong transmission guarantee of the message. These needs are mainly found in transport (reaction time in case of accident risk), in medicine (tele surgery) and, in general, for digitization of the industry. The mMTC mainly encompasses all uses related to the Internet of Things. These services require extensive coverage, low energy consumption and relatively small. The announced contribution of 5G compared to current technologies lies in its ability to connect objects distributed very densely over the territory.

In order to implement these three types of use, eight performances indicators Key performance indicators KPI have established by the International Mobile Telecommunications ITU to specify, quantify and measure features of IMT-2020 (5G) systems:

- Peak data rate (Gbit/s);
- User experienced data rate (Mbit/s);
- Spectrum efficiency (bit/Hz);
- Maximum speed of the terminals or mobility (km/h);
- Latency (ms);
- Connection density or number of objects connected to a zone (devices/km²);
- Network energy efficiency;

- Area traffic capacity (Mbit/s/m²);

According to 5G plan, it should be able to offer a user data rate and a peak data rate respectively 10 and 20 times higher than what is currently available. The maximum density of connections will be multiplied by 10 and the latency divided by at least 10 (the target point-to-point latency is 1 ms, as against 30 to 40 ms to date) as shown in Figure 1-4.

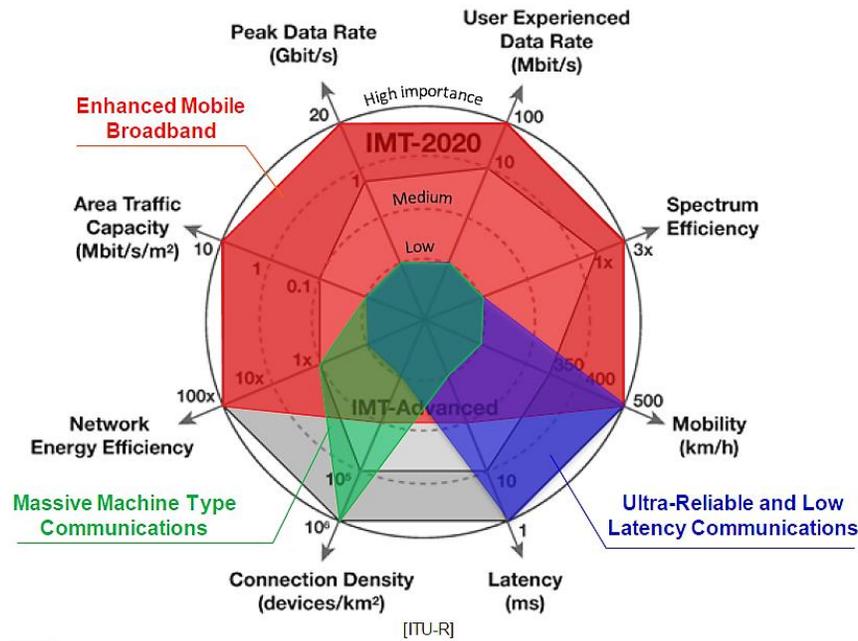


Figure 1-4. Enhancement of key capabilities from IMT-Advanced to IMT-2020 [4]

The goal of 5G, as a successor to 4G, will also be to provide:

- An extremely reliable network, with more homogeneous performances, whatever the position of the user compared to the base station;
- A stable connection even in mobility (with speeds of the order of 500 km/h);
- An increase in energy efficiency (batteries up to 100 times less energy intensive).

The table below summarizes the expected performance of 5G and those currently available with 4G:

Table 1. Comparisons between the performances of 4G and 5G

	4G	5G [4]
Peak data rate (Gbit/s);	1	20
User experienced data rate (Mbit/s)	10	100
Spectrum efficiency (bit/Hz)	x1	x3
mobility (km/h)	350	500
Connection density (devices/km ²)	10 ⁵	10 ⁶
Latency (ms)	10	1
Network energy efficiency	1x	100x
Area traffic capacity (Mbit/s/m ²)	0.1	10

1.2.2 5G Bands

The millimeter band corresponds to frequencies higher than 6 GHz, which mostly not taken into account for the deployment of mobile networks (fronthaul) for reasons of technological maturity and quality of propagation noting that the fronthaul is the connection between the cell tower radio itself and the mobile network control backbone (Baseband Unit). To respond to the incessant increase in data rates and volumes exchanged, it is necessary to use new bands with very large pipelines (more than 100 MHz per user): the millimeter bands could offers such spectrum reserves and their use would in some cases achieves the rates shown in Table 1. In return, their use requires the development of all necessary technologies, miniaturized, low cost and with an energy consumption compatible with portable terminals (oscillators, amplifiers, signal processing, antennas ...). In particular, because of the low propagation quality of the millimeter waves, each cell will have a reduced coverage, which will require the implementation of beamforming techniques, to focus the energy transmitted by the antennas.

5G presents itself as a technology that will use both low frequencies ($f < 1$ GHz), medium frequencies ($1 \text{ GHz} < f < 6 \text{ GHz}$) and, for the first time in consumer networks, high frequencies ($f > 6 \text{ GHz}$) towards mm-wave bands. This spectral diversity is link to the promises of 5G: extended coverage (low frequencies), ultra-high speed (very wide channels in very high bands), low energy consumption. In addition, satellite services will also be able to participate in the development of this new technology, particularly in the most difficultly covered areas or to provide additional backhaul (the link between a base station and the core wired network that is even fiber, coax, or wireless). In this respect, the satellite world is interested in 5G and wishes to be involved in the definition of this generation.

1.2.2.1 Above 6 GHz

At the World Radio communication Conference (WRC-15) in Geneva, under the aegis of the ITU whose objective is to change the distribution of frequencies between users, various discussions on the definition of future mobile bands have enabled the 5G studies to focus on millimeter frequencies over a number of bands between 24 GHz and 86 GHz. The candidates are 24.25 - 27.5 GHz, 31.8 - 33.4 GHz, 37 - 43.5 GHz, 45.5 - 50.2 GHz, 50.4 - 52.6 GHz, 66 - 76 GHz, and 81 - 86 GHz as shown in Figure 1-5. It is important to note that while the above-mentioned bands have identified as 5G bands, there is still no indication at this stage whether they can really inserted for the deployment of this latest generation. Only the results of the technical studies will make it possible to establish the constraints and the rules.

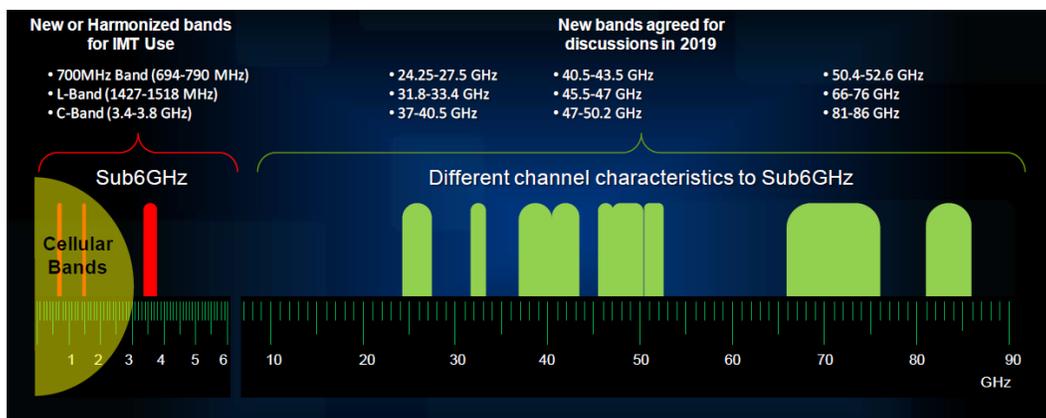


Figure 1-5. The spectra availability and possible usage for 5G deployment

Contrary to the conclusions of the Conference, which reflect the European recommendations, the United States and other Asian countries (Korea, Japan) have decided to launch 5G experiments in the 28 GHz band and equipment manufacturers, such as for example Qualcomm or Samsung, began manufacturing products in the 28 GHz band.

Europe, for its part, decided, following the publication of an opinion of the RSPG (Radio Spectrum Policy Group, a European group of spectral policy in which France is represented by the ANFR) [5], to carry out, as a priority, studies on the 26 GHz band (pioneer band), then on the 32 GHz and 42 GHz bands. In a second step, studies for the introduction of 5G in all other bands identified by WRC-15 will be continue.

The rapid selection of the 26 GHz band as a pioneer band is to allow economies of scale in the production of equipment, since it is very likely that dual-mode equipment, operating in both the 26 GHz band and 28 GHz will be available from the first deployments.

Figure 1-6 shows the sea level atmospheric attenuation for the millimeter band. It shows a small peak at 23 GHz and large peak at 60 GHz of 13dB/km. Indeed, low attenuation level between 10 GHz and 50 GHz of 0.3 dB/km or less occur. A clear atmospheric window can be seen from 70 GHz to 110 GHz with low atmospheric attenuation around 0.5 dB/km. This shows the advantage of the 5G frequency candidates that choose by the ITU.

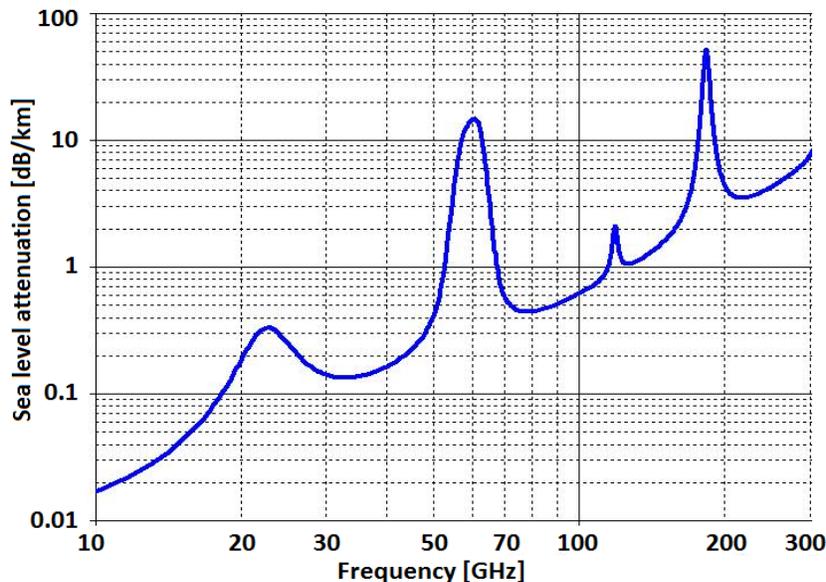


Figure 1-6. Millimeter band Sea level atmospheric attenuation

1.2.2.2 Bands below 6 GHz

- **The band 3.4-3.8 GHz**

The 5G cannot completely conveyed by the millimeter bands: the propagation qualities of these bands make delicate an extended coverage, especially in the less densely populated areas of the territory. In addition, the technological maturity of the use of these tapes for consumer communications is still very low. It is therefore necessary to identify a "core" band, which is less than 6 GHz and proposes network large enough for future 5G operators to be able to provide innovative services and improved quality of service compared to 4G

The 3400 - 3800 MHz band seems to be a good candidate to meet this need. At first, the band 3400 - 3600 MHz then the band 3600 - 3800 MHz have been identified as IMT bands for mobile broadband. In addition, it has a large amount of available spectrum (up to 400 MHz). Finally, technological advances (antenna and signal processing) make it possible to consider the use of these frequencies for the establishment of macro cells, and not just microcells.

This analysis has been confirmed by the European Commission (in its 5G mandate at RSCOM [6]) and the RSPG [7], which consider the 3.4 - 3.8 GHz band as the only credible 5G band for deployment by the end of 2020.

- **Other bands below 6 GHz**

The bands currently used for 2G, 3G and 4G can also be use in the future for 5G deployments. However, the reforming of the 2G, 3G and 4G bands could be tricky, because of the mode of duplexing used by them. Indeed, most mobile communications in Europe use the FDD - Frequency Division Duplexing mode to exchange information. The technical discussions around the 5G however announce the TDD - Time Division Duplexing mode as privileged (if not unique) duplexing mode for this new generation, in particular because it makes it possible to adapt the bandwidth used to the debit and because it is particularly effective when beamforming is used. The use of already harmonized mobile bands for 5G networks will therefore require in-depth technical studies to define the conditions of use and sharing with the services in place. In this respect, the ECC - Electronic Communications Committee has decided to evaluate the potential of some already harmonized bands, in particular the 700 MHz band and the L-band (1427-1492 MHz).

The Bands details can give a vision of networks and services at the horizon 2020 and beyond as shown in Figure 1-7. The 5G service delivery will not be limited to any specific frequency band; rather, it will follow the optimal delivery over the best available spectra. The assumption of the wireless network capabilities:

- 1) 50-Gb/s macro coverage
- 2) 100-Gb/s micro local coverage
- 3) 80-Gb/s E-band back/front-hauling links.

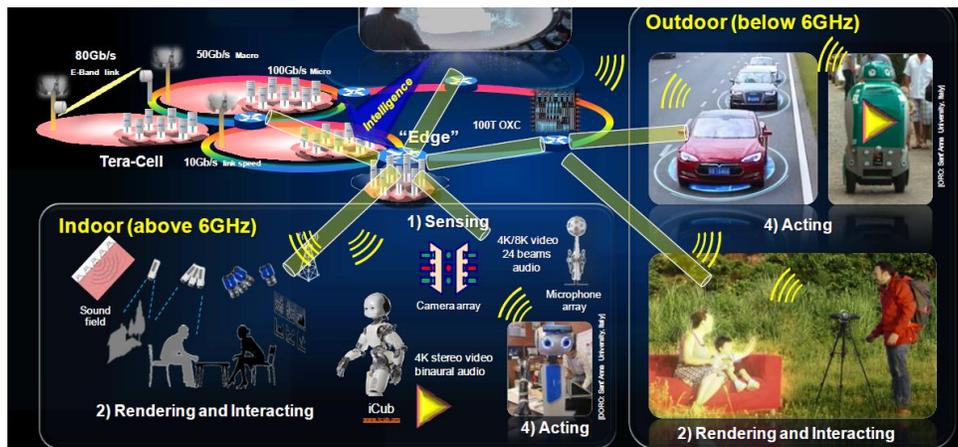


Figure 1-7. The vision of 5G services

1.3 Millimeter Transmitter

The millimeter transmitter and transceiver based on two structures: heterodynes and homodynes. The digital I and Q data, which generated by the Digital Signal Processor (DSP), are converted to continuous signals through digital to analog converters (DACs). These signals are then modulated on a carrier frequency before be amplified by the power amplifier and transmitted by the antenna. The analog part contains local oscillator with phased locked loop (PLL), mixers, and power amplifier.

1.3.1 Heterodyne architecture

The most common structure of issuer architectures is undoubtedly the heterodyne structure. This structure, illustrated in Figure 1-8, is composed as following; the baseband signals Q and I, after being filtered and amplified, are transposed at an intermediate frequency f_{Fi} thanks to two-quadrature mixers phase. The signal is then filtered to remove the f_{Fi} harmonics. Then the signal is transposed again to the frequency $f_{Fi} + f_{HF}$ with a last mixer. This mixture results not only the frequency $f_{Fi} + f_{HF}$ but also the frequency $f_{Fi} - f_{HF}$. The latter is eliminate by a band pass filter. Finally, the signal is then amplified and filtered before being transmitted to the antenna. The useful signal and the image signal have the same power, which mean that the band pass filter of the second conversion stage must be enough to reject the image signal. For a good suppression of harmonics, the integrated band pass filter must have a high order. This architecture also imposes the use of two PLLs with low phase noise. A super heterodyne architecture uses one oscillator with one PLL in which $f_{HF} = n \cdot f_{Fi}$

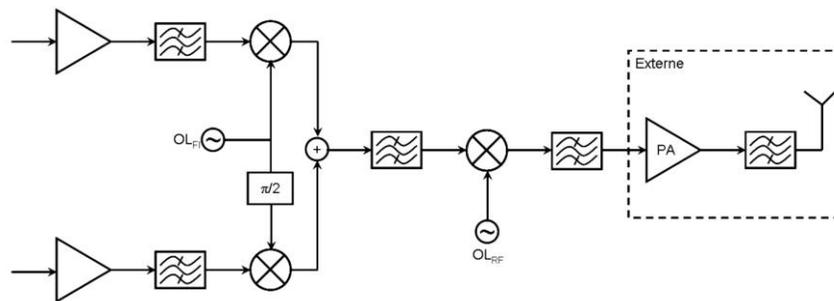


Figure 1-8. Heterodyne Transmitter Schematic

An example of super heterodyne fully integrated 60 GHz transceiver module in a 65nm CMOS technology for wireless high-definition video streaming is illustrated on Figure 1-9. It covers the room 57 to 66 GHz frequency band. It delivers 16 dBm saturated output power with maximum gain of 17.5 dB [8].

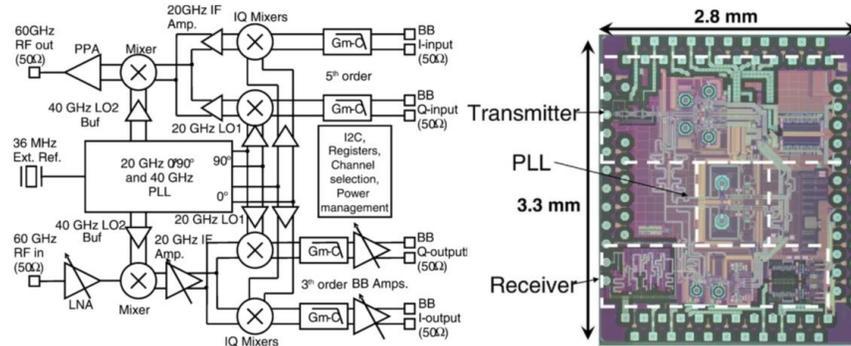


Figure 1-9. Heterodyne Transceiver [8]

1.3.2 Homodyne architecture

To remove the problem of image frequencies, transmitters' studies led to homodyne architecture, also called direct conversion or Zero - Intermediate Frequency (Zero-IF). The signal is directly converted to the frequency at which the signal will be transmitted. This architecture is illustrated in Figure 1-10. This architecture allows a reduction of the cost and the general consumption by grouping I Q modulators and frequency synthesis. This leads to a greater level of integration and better treatment of digital data. Thus, the baseband signal is directly modulated at the RF frequency with two quadrature mixers, a PLL and a local oscillator operating at the RF frequency.

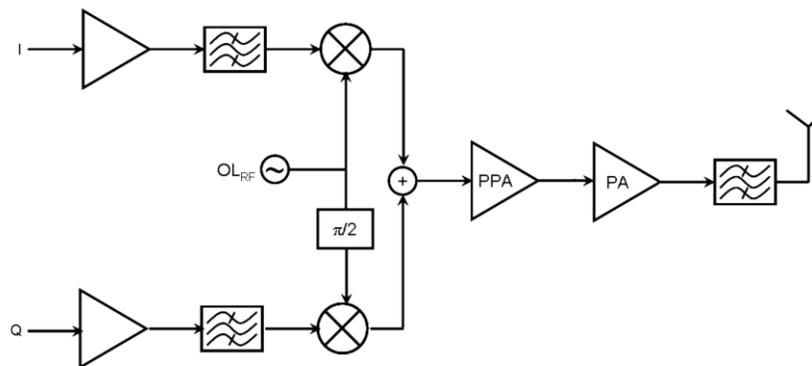


Figure 1-10. Homodyne Transmitter Schematic

This architecture is more compact than heterodyne transmitter because it uses fewer components. Indeed, the image rejection of the channel is performed dynamically by summing the output of the mixers. We thus remove a band pass filter, a second conversion stage in frequency and an external filter of the image frequency. However, it is necessary for the I and Q channels to be well tuned in terms of amplitude and phase. Indeed, it is important to realize a precise phase

quadrature operating at the RF frequency. Inaccurate quadrature leads to bad rejection of the image of the mixture. One of the recurring problems with this architecture is that the elements, much closer to each other, can bring a pulling phenomenon [9]. Indeed, when two oscillating systems are too close, they tend to match by coupling. In a direct conversion transmitter, the local oscillator and the output of the Power Preamplifier (PPA) operate at frequencies, which are close to each other and can be coupled by the substrate. The output signal of the PPA having an output power far superior to that of the local oscillator, the latter can be shifted in frequency. Therefore, it must be ensured that these elements not too close.

An example of homodyne transceiver manufactured in 65nm CMOS technology at 60 GHz is illustrated in Figure 1-11. It is composed of four cells in transmitter and receiver. Each power amplifier can delivers -1,5dBm saturated power with a gain of 24 dB over 8 GHz bandwidth [10].

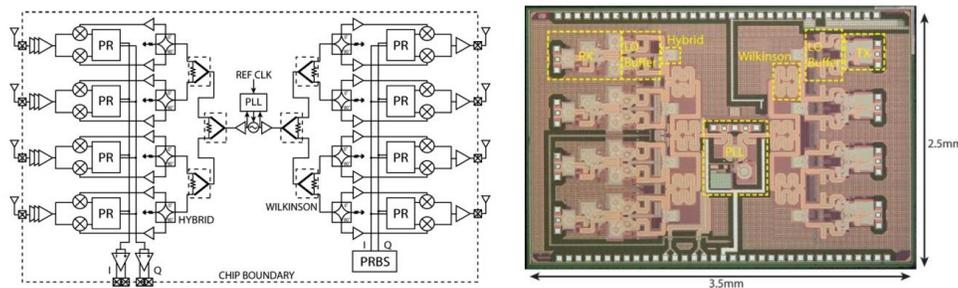


Figure 1-11. Homodyne Transceiver [10]

1.4 Millimeter Wave Oscillators

An oscillator is a circuit generating a periodic signal at a constant or variable frequency. In the latter case, we often talk about voltage-controlled oscillator. Indeed, they are used to generate the signals timing (clocks), to modulate and demodulate signals.

In 5G, there is a clear trend towards the use of high-speed links between mm wave transceivers and digital signal processing in baseband, which requires generation of a frequency clock in the same band with increasing performance in terms of jitter and phase noise. These performances seem to be less compatible with classical architectures of ring oscillators. Moreover, the use of a LC oscillator has many disadvantages for these applications (area, sensitivity, radiation, pulling...).

1.4.1 Oscillator Model

An oscillator is often modeled by the looped system shown in Figure 1-12. It consists of an active part (the gain element) and a passive element (the resonator) buckled by a positive feedback that reinjects part of the signal of the exit at the entrance.

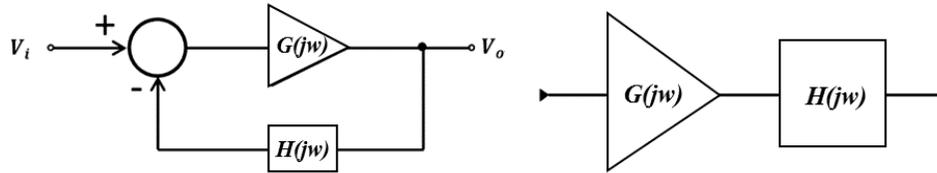


Figure 1-12. a) Oscillator Closed Loop Model

b) Oscillator Open Loop Model

where $A(j\omega)$ is the closed loop gain, $G(j\omega)$ is the gain of the amplifier, and $H(j\omega)$ is the feedback transfer function.

$$A(j\omega) = \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{G(j\omega)}{1 - G(j\omega).H(j\omega)} \quad (1.1)$$

To determine the oscillation conditions. The open loop should be studied. The open loop transfer function is:

$$A_{OL} = \frac{V_o(j\omega)}{V_i(j\omega)} = G(j\omega).H(j\omega) \quad (1.2)$$

For the system to oscillate in steady state, it is necessary that $V_o(j\omega) = V_i(j\omega)$ so that $G(j\omega).H(j\omega) = 1$. This amounts to satisfy the conditions of Barkhausen criteria, which are:

$$|G(j\omega).H(j\omega)| = 1, \quad \text{Arg}\{G(j\omega).H(j\omega)\} = 0[2k\pi]; k \in N$$

Generally, an oscillation starts with the amplification of the noise of the elements of the loop [11]. Indeed, in equilibrium, there is, in principle, no energy transfer between the different elements of the circuit. That's, in fact, the intrinsic noise of the components (the thermal agitation of electrons), which is a random phenomenon that imbalance the device. This imbalance is then amplified by the gain of the loop and the oscillation can then start. To set up the oscillation, the gain of the active part $G(j\omega)$ is greater to the gain of the transfer function of the resonator $H(j\omega)$ Once the oscillation of the device ensured, the main performances of an oscillator are defined as: the oscillation frequency, the power delivered at this frequency, and the phase noise level.

1.5 Phase noise

The noise in the oscillators and, more specifically, the phase noise is the most important parameter to consider in the design of oscillators. In order to understand how important the noise performance can be in oscillator, it is necessary to take an example of some points in RF communication. The space of the frequency bands is divided to several standards of communication. Many standards subdivide their own space into two bands: one for the transmission (Tx), the other for the reception (Rx). Each band is subdivided into channels that are assigned to one or more users. As an example, in the GSM, the Tx transmit band is in the [880 MHz - 915 MHz] range and the Rx receive band is in the [925 MHz - 960 MHz] range and the channels are wide 200 kHz. A high phase noise level in a band can disturb the communications located on an adjacent band. In our example, the phase noise at 11 MHz offset of the carrier of the transmitted signal in the last channel of the band Tx transmission (915 MHz), will end up in the reception band Rx (915 + 11 = 926 MHz). It will therefore scramble the reception signal, which is generally weaker than the broadcast level from the phone.

1.5.1 Principle of noise generation in oscillators

The noise of the oscillators arises from the electronic noise of the constituent components. The phase noise is a phenomenon due to the conversion of different sources of noise into semiconductors around the carrier frequency thereby generating phase modulation. The consequence is the random variation of the frequency of the output signal of the oscillator.

1.5.2 Phase noise in oscillators

Phase noise is manifested by random fluctuations in the period of the output signal of the oscillator. These fluctuations are due to different sources of spreading noise in the spectral power density around the carrier frequency. The phase noise is expressed as a single sideband brought back into a measuring band of 1 Hz. This magnitude noted L is expressed by the ratio between the power in a sideband of the phase noise and the power of the carrier:

$$L(f_m, B) = 10 \log \left\{ \frac{P_n}{P_0} \right\} \quad (1.3)$$

$$P_n = \int_{f_0 + f_m - \frac{B}{2}}^{f_0 + f_m + \frac{B}{2}} SPD(f) df \quad (1.4)$$

The power of the noise is in a frequency band B at the distance f_m of the carrier. P_0 denotes the power of the carrier. Since L (f_m) expresses itself in power by relative to the carrier per frequency band, its unit is in dBc / Hz Figure 1-13. The single sideband phase noise L is defined in dBc / Hz when the power P_n is determined on a bandwidth of 1 Hz [12].

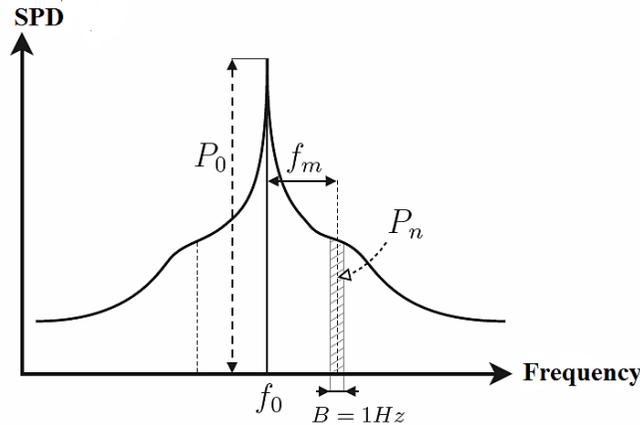


Figure 1-13. Phase Noise Power Spectrum

Many authors have established phase noise estimation techniques that have the advantage of highlighting the influence of certain parameters of the oscillator. The most important one is for Leeson. Leeson's model is a linear model prediction of phase noise defined by the following equation [13]:

$$L(f_{off}) = 10 \log \left(\frac{1}{2} \left[\left(1 + \left(\frac{f_0}{2 \cdot Q \cdot f_{off}} \right)^2 \right) \left(1 + \frac{f_c}{f_{off}} \right) \left(\frac{F \cdot K \cdot T_0}{P_{diss}} \right) \right] \right) \quad (1.5)$$

Where Q is quality factor in charge. F is noise factor. f_0 is the oscillation frequency. K is Boltzmann constant. f_{off} is frequency of the offset. T_0 is temperature (290K). f_c is cutoff frequency. P_{diss} is Power consumed.

According to Leeson, the frequency fluctuations of the oscillator are directly related to the inherent noise of the amplifier of the oscillation loop. The voltage or current fluctuations at the origin of the low frequency noise of the amplifier, and therefore of the transistor in most cases, are converted into frequency fluctuations by the oscillation loop.

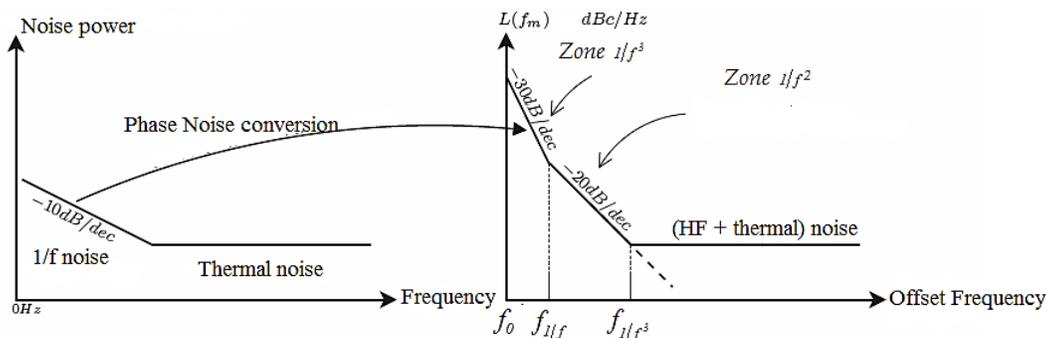


Figure 1-14. a) Transistor Noise

b) Phase Noise of an Oscillator

The phenomenon of converting the amplitude of power noise into phase noise is complex and has different origins as shown in Figure 1-14. The zone $1/f^3$ translates the noise conversion of $1/f$ noise of the transistor. The zone in $1/f^2$ denotes the conversion of white noise by the oscillator. In the noise floor zone (or thermal noise), it is considered that does interfere in the conversion process [14], where:

$$f_{\frac{1}{f^3}} = \frac{f_0}{2Q_{ch}} \quad (1.6)$$

The quality factor has several definitions. The most general definition is 2π times the ratio of stored energy by dissipated energy per cycle [15].

$$Q = 2\pi \frac{\text{Stored Energy}}{\text{Dissipated Energy per cycle}} \quad (1.7)$$

And

$$Q = \frac{\omega_0}{2} \frac{d\varphi}{d\omega} \quad (1.8)$$

From the approximation of the linear system made by B.RAZAVI in [15], the calculation of the quality factor in open loop by the following formula:

$$Q = \frac{\omega_0}{2} \sqrt{\left(\frac{dA}{d\omega}\right)^2 + \left(\frac{d\varphi}{d\omega}\right)^2} \quad (1.9)$$

With

$$H(j\omega) = A(\omega)\exp(j\varphi(\omega)) \quad (1.10)$$

Where A , φ and ω_0 are the amplitude, the phase and the angular velocity of the signal.

1.6 Oscillator Types

1.6.1 LC Oscillators

The LC oscillator can be seen as a set composed of an LC resonator and a negative resistance. The LC circuit is configured to have a resonance frequency close to the desired operating frequency for the oscillator. While the negative resistance realized via the active circuit, allows compensating the resistive portion of the LC block. The advantages of LC oscillators are good phase noise and low jitter noise at high frequency. On the other hand, their surface is very large because they contain an inductance. Moreover, these oscillators consume a lot of energy and have a range of relatively small use. Despite these disadvantages, the LC oscillators remain the oscillators most used in radio communication applications.

1.6.2 LC Oscillator State of Arts

The LC oscillator uses an inductor and a variable capacitor (varactor). The quality factor is usually low at mm wave band that dominates the quality factor of the inductor, which leads to degraded phase noise. Another limitation is that the transistor cannot be increased in size since the parasitic capacitance will let the designer decrease the size of the varactor, which degrades the frequency tuning range (FTR). Many topologies were proposed to improve the quality factor of the LC resonator in the mm wave band. The topologies can be divided into three categories; the conventional one that uses lumped elements (inductor, varactor), hybrid resonator, which uses lumped elements and transmission lines, and finally the distributed resonator which uses only transmission lines.

The work in [16] shows an optimization of the layout level; he made a circular inductor as shown in Figure 1-15 and decreased the parasitic capacitance of the transistor by minimizing the interconnection between the two transistors. The phase noise enhanced to -89 dBc/Hz at 1 MHz offset, 59 GHz center frequency, and 5.8 GHz tuning range.

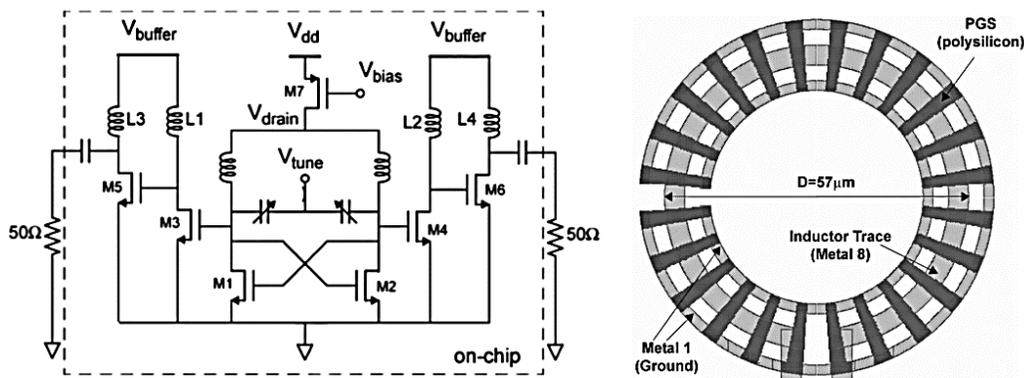


Figure 1-15. a) VCO proposed by [16]

b) Circular Inductor [16]

The authors [17] introduce a new technique; it is based on adding a series inductor with the varactor, then the equivalent shunt conductance of the whole resonator will effectively decrease as higher frequencies, which make the frequency of the oscillator close to the maximum frequency of the transistor. The circuit is shown in Figure 1-16. The varactor losses will be reduced with respect to high frequencies and it will be treated as a variable inductor at a frequency greater than the resonance frequency of L_1 and C_{var} . An attention should be taken in selecting the values of the components. It is designed in 180 nm CMOS technology at 49 GHz with -101 dBc/Hz and 0.8 GHz frequency tuning range (FTR).

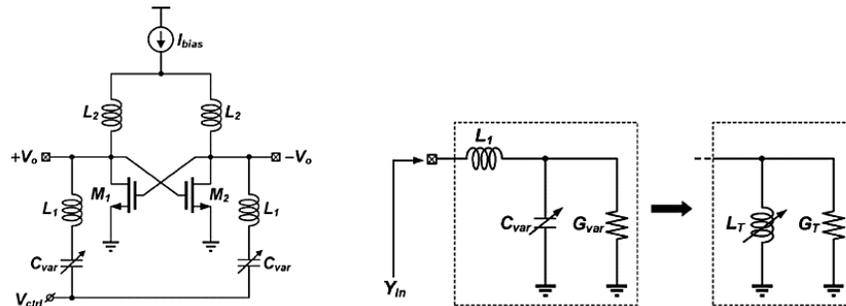


Figure 1-16. a) VCO schematic [17] b) Admittance Transformation [17]

A novel technique was proposed by the authors in [18] to increase the FTR. As shown in Figure 1-17, a switched triple transformer is designed instead of increasing the size of the varactor; it had three states with different values of magnetic coupling. It is designed in 65 nm CMOS technology with 32 GHz FTR and 73.8 GHz center frequency with -112 dBc/Hz at 10 MHz offset. The proposed topology by [15] suffers from complexity in design and from big step size during frequency tuning (1GHz/bit).

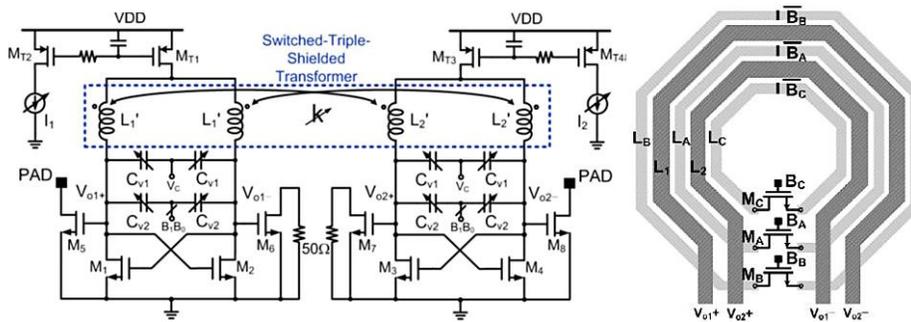


Figure 1-17. a) VCO schematic [18] b) switched Triple Transformer [18]

The authors in [19] also worked in increasing the tuning range, but unlike the work in [18], he utilized a single turn inductor with switched capacitor bank that are digitally controlled, then the effective value of the total capacitance will be varied allowing the oscillation frequency to be varied too. The schematic is shown in Figure 1-18. It is designed in 65 nm CMOS technology with 9.3 GHz FTR and 56 GHz center frequency with -99.4 dBc/Hz at 1 MHz offset.

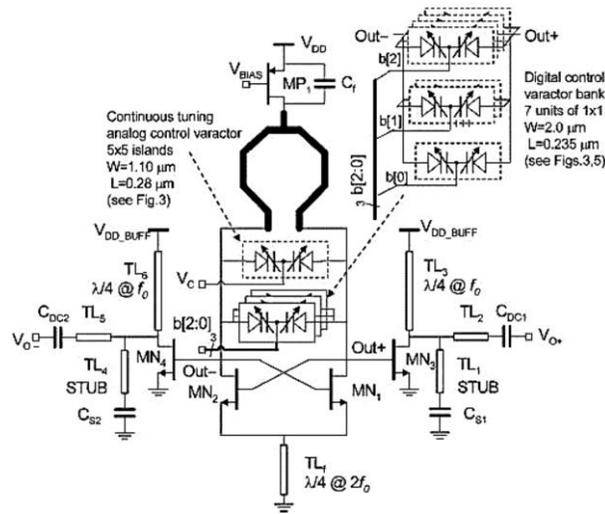


Figure 1-18. VCO proposed by [19]

The works in [20] and [21] are divided into two steps. First, in [20], a high quality factor inductor was designed using multilayer coplanar waveguide with constant length as shown in Figure 1-19. While in [21], the length of the same inductor is varied and tuned after fabrication by the focused ion beam (FIB) technique that trim the shorting pins shown in Figure 1-19 instead of using switches, then as a result, a variable inductor will be utilized by adjusting the length of the transmission line which vary the frequency of oscillation.

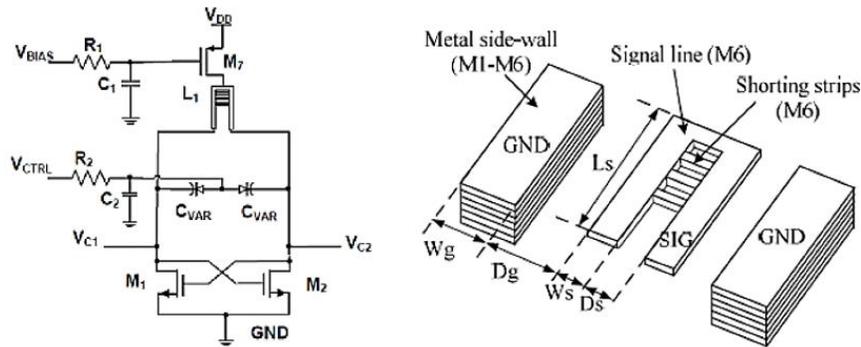


Figure 1-19. a) VCO proposed by [20] [21] b) Multilayer Coplanar Waveguide [20] [21]

A phase noise of -109 dBc/Hz at 10 MHz offset with tuning range of 4.8 GHz in [20] while -108.4 dBc/Hz at 10 MHz offset with tuning range of 10.6 GHz in [21] at 76.5 GHz oscillating frequency in 65 nm CMOS technology.

In the work in [22], the tuning element was an open circuit dielectric artificial drawing (DiCAD), it is digitally controlled. A slow wave differential transmission line is controlled by

varying the effective permittivity, which is controlled by NMOS Pi-switches as shown in Figure 1-20. It achieves -90 dBc/Hz phase noise at 1 MHz offset, 6 GHz tuning range, and 61 GHz oscillating frequency.

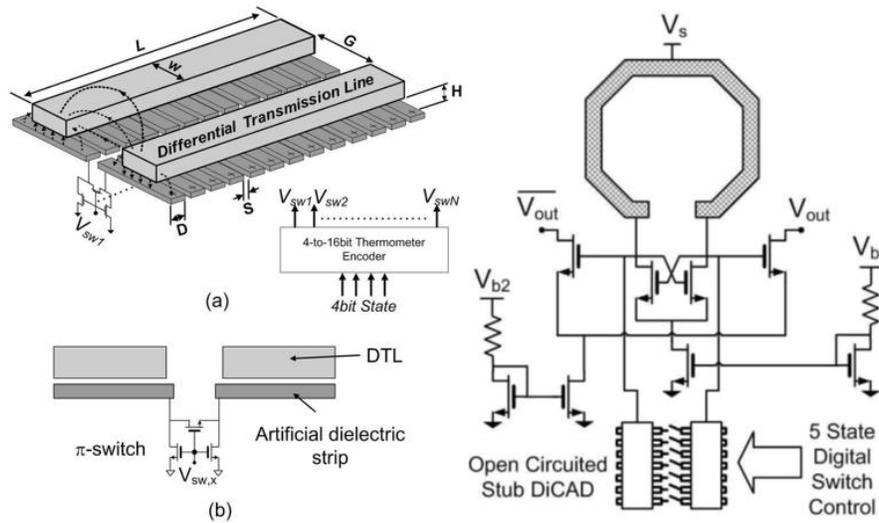


Figure 1-20. a) DiCAD differential transmission line layout b) DiCAD strips schematic c) Digital Control Oscillator [22]

The same tuning method in [22] is applied on an inductor in [23] as shown in Figure 1-21, and on transformer in [24] as shown in Figure 1-22, to form a digital control oscillator. The work in [23] has a resolution or step size of 160 KHz, while [24] has step size of 2.5 MHz, which are better than that of [22] with 1.16 GHz. Both are also designed in 90 nm CMOS technology with 59 GHz oscillating frequency, 6 GHz tuning range, and -93 dBc/Hz phase noise.

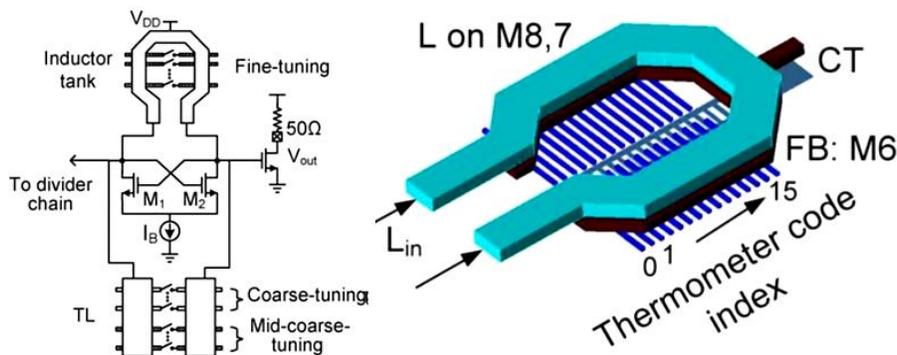


Figure 1-21. a) VCO proposed by [23]

b) Inductor Tank Layout [23]

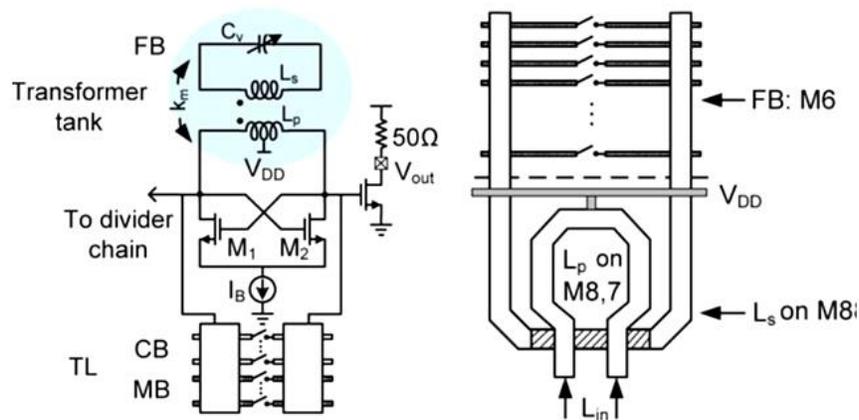


Figure 1-22. a) VCO proposed by [24]

b) Transformer Tuned layout [24]

Table 2. LC Oscillators State of Arts

Reference	CMOS Technology (nm)	F_{osc} (GHz)	Tuning Range (GHz)	Phase Noise (dBc/Hz)	P_{out} (dBm)	P_{DC} (mW)
[16]	130	59	5.8	-89@1MHz	-18	9.8
[17]	180	49	0.8-1.1	-101@1MHz	-11	45
[18]	65	73.8	32	-105@10MHz	-20	10.8
[19]	65	56	9.3	-99.4@1MHz	-9.8	15
[20]	65	76.5	4.8	-109@10MHz	--	14.3
[21]	65	76.5	10.6	-108@10MHz	--	14.3
[22]	90	61	10	-90@1MHz	-5	8.52
[23]	90	59.2	10	-93@1MHz	-3.4	12
[24]	90	58.7	9.75	-94@1MHz	--	14

Each topology is designed with different Back End of Line (BEOL), which make the comparison of the performances more complex. It is clearly that to improve the quality factor of the LC resonator, a switchable or variable inductor is better from utilizing varactor. In addition, the best phase noise achieved is -101 dBc/Hz, and the highest output power is -3.4 dBm that make the presence of the power amplifier obligatory in the transmitter chain.

1.7 Objective and Methodology

Most of the VCOs are implemented in a phased locked loop (PLL); a control system consist of phase detector, low pass filter, and VCO. It is a closed loop to ensure the oscillation at the desired frequency. In [25], he proposed a new topology of microwave and mm wave oscillator. It

is based on an amplifier and a substrate-integrated waveguide (SIW) that has a high quality factor. The fundamental signal, which is amplified, divided into two path: the transmission path, which fed the output with the oscillation signal at the same fundamental frequency, and the coupling path, which fed the input of the amplifier as a feedback system to ensure the oscillation according to Barkhausen law conditions as shown in Figure 1-23 and Figure 1-24.

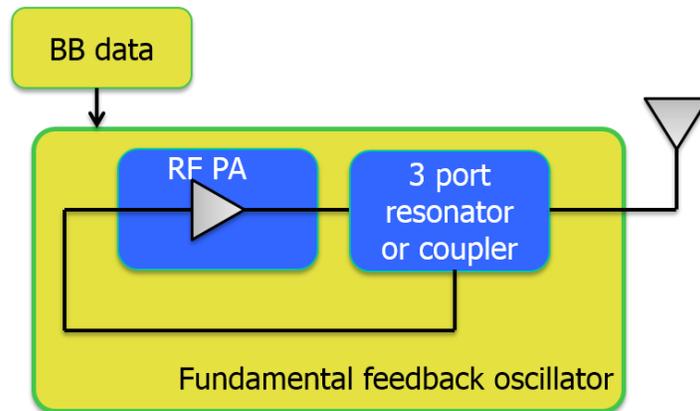


Figure 1-23. Fundamental Feedback Oscillator Topology

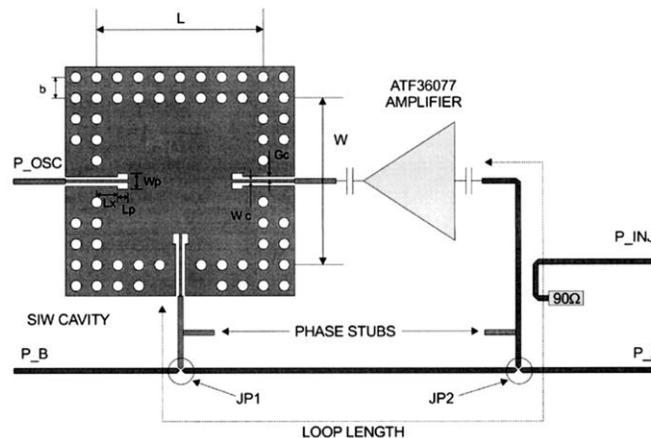


Figure 1-24. Fundamental Feedback Oscillator proposed by [25]

In [25], the output frequency is 12.02 GHz with phase noise -73 dBc/Hz at 100 KHz offset. This topology open a flow that it can be get rid of the power amplifier in the transmitter chain because the power amplifier in the fundamental feedback oscillator that is not found in VCOs (based mainly on PLL), already amplify the signal to fed the antenna directly, which decrease the complexity of the transmitter.

Our team in the IMS Lab worked on the power oscillator as fundamental feedback oscillator. The author in [26] show a TX architecture based on power oscillator using 65nm CMOS

technology from STMicroelectronics. The PA has a class E to achieve high efficiency as shown in Figure 1-25. The output of the PA is connected to a capacitive divider with a filter to form a loop. The power oscillator achieves a high output power of 23.3 dBm at 2.5 V supply voltage, PAE of 60.3%, and oscillating frequency of 1.95 GHz.

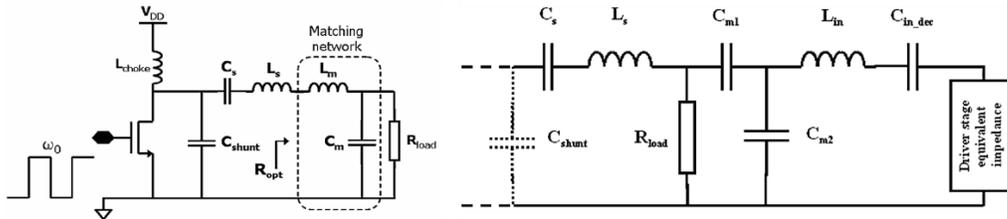


Figure 1-25. a) Class E PA [26] b) Output matching in [26]

Another work is done by the IMS team in [27], it proposed class EF2 power amplifier path using 130 nm CMOS technology at 2.5 GHz operating frequency, and a feedback consist of MOS varactor to form a power oscillator as shown in figure. The use of class EF2 is to reduce the stress voltage across the transistor that has low breakdown voltage, enabling higher output power.

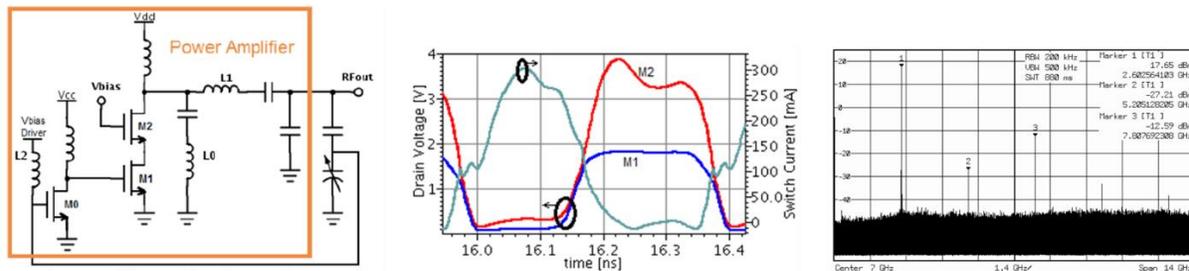


Figure 1-26. a) Oscillator Schematic b) Drain voltage and current c) Output Spectrum [27]

The work in [27] achieves output power of 17.65 dBm at 2.5 V supply voltage, efficiency of 27.1%, and phase noise of -101.6 dBc/Hz at 1 MHz offset

The power oscillator based on fundamental feedback oscillator decreases the pulling effects that occurred between the power amplifier and the local oscillator due to limited on-chip isolation (coupling through substrate) in the conventional transmitter, which degrade the phase noise [9]. While it has a pulling effect between the PA and the antenna

In 17th century, Christiaan Huygens, a Dutch scientist, was confined to bed because of sickness, noticed that the pendulums of two clocks on the wall moved in unison if the clocks were hung close to each other [28]. He assumed that the coupling of the mechanical vibrations through the wall drove the clocks into synchronization. Bahzad Rasavi in [9] ensure that the oscillators are prone to injection locking or pulling. The idea of pulling effect in transmitter chain is that the modulated output signal of the power amplifier has the same frequency of the oscillator. This make

the lattice susceptible to interface the PA output through the substrate causing frequency pulling and phase noise degradation, especially that the output signal of the PA is mainly higher than the output of the oscillator as shown in Figure 1-27.

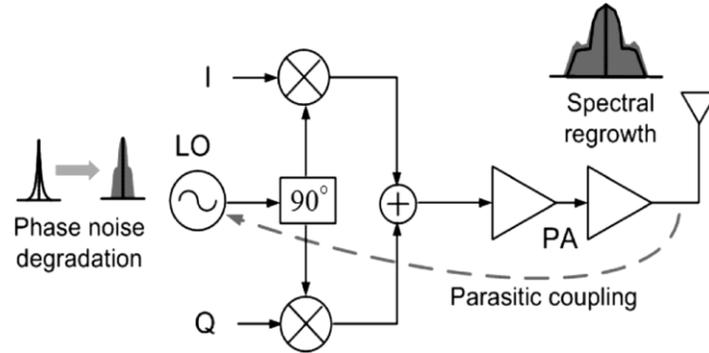


Figure 1-27. Pulling Effect between LO and PA in TX [29]

Various digital processing and shielding techniques are done to increase the isolation between the VCO and PA, but no general solution eliminates the pulling effects [29]. This problem keeps the door open to search for a topology other than PLL in addition to its low efficiency.

In addition, the fundamental feedback oscillator in transmitter chain has two main problems, which are the variation of the load impedance (antenna) and the pulling/locking effect. The antenna has a function to transform the electric energy to electro-magnetic energy where its impedance should be constant at 50Ω. The incident signal is fed from the PA to the antenna through a transmission line of 50Ω too. Adding some parasitic elements as metal obstacles in the environment of the antenna will increase the voltage standing wave ratio. First, the VSWR in the circuit is defined by

$$VSWR = \frac{\max(V(x, t))}{\min(V(x, t))} = \frac{1 + |\Gamma_L|}{1 - |\Gamma_L|} \quad (1.11)$$

Where Γ_L is the ratio of the reflected signal over the incident signal in the transmitter chain, if $\Gamma_L = 0$, it means that there is no reflection and the incident wave is totally radiated from the antenna, and if $\Gamma_L = 1$, it means that all the power of the signal is reflected backward to the PA. The VSWR refers to the minimum and maximum voltage signal that is formed under the effects of reflections. The Figure 1-28 show the phenomena that produce a variation of the antenna impedance. The blue wave in the incident wave, which is radiated by the antenna, the red wave is the reflected signal due to the presence of the obstacle, and the green wave is the sum of both signals. The same phenomena will occurs in the transmission line between the PA and the antenna, which results a variation of the antenna impedance. No such publications for the effects of human body on the antenna in the mm wave band, the only publication is [30], which shows the effects of human body on a horn antenna at the GSM applications band (400 MHz – 900 MHz). It shown a VSWR of 7:1

at 450 MHz and 4:1 at 900 MHz when a human body touches the antenna. A VSWR of 7:1 means that the real impedance change between 7Ω and 30Ω while it should be constant at 50Ω . In mm wave band, the results will be very different but no further studies at this band.

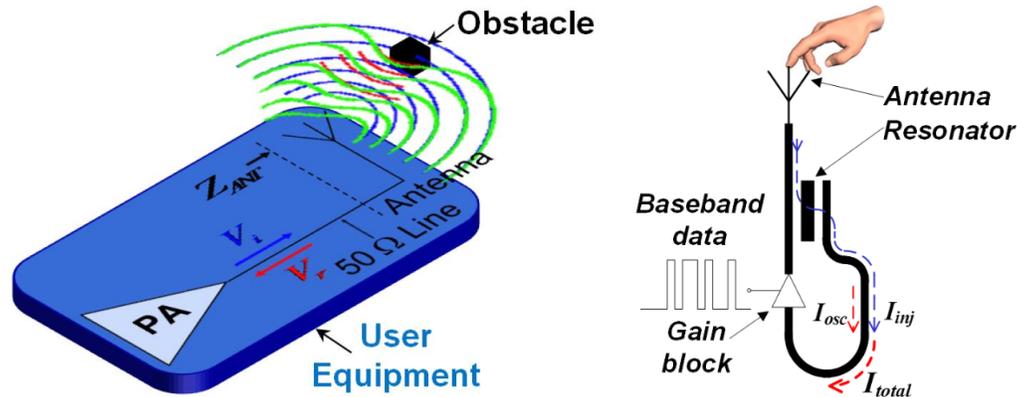


Figure 1-28. a) Obstacles Effect in Antenna Environment b) Pulling Effect in FFO

The second problem is the pulling effect. Because of the reciprocity of the resonator, the reflections of the output signal results in a current injection in the feedback loop as shown in Figure 1-28. Therefore, the conditions of oscillations are modified, and the working frequency with the amplitude of the output signal are altered.

A new novel architecture is proposed in [31]. The idea is to replace the resonator structure by a diplexer port (not duplexer) that will allow the feedback loop to ensure oscillation at the fundamental frequency and being isolated from the output, which supply the signal to be transmitted through the second harmonic. This greatly reduces the impact of the load impedance variation on the nonlinear dynamics of the feedback loop. To show the improvement provided by the choice of using the second harmonic frequency as the transmission signal, two circuits on PCBs were designed in [31] : Fundamental feedback oscillator (FFO) and Harmonic feedback oscillator (HFO). Thus, the proposed new transmitter structure operates at 5.8 GHz with fundamental frequency at 2.9GHz for on-off keying (OOK) transmitters for active RFID tags.

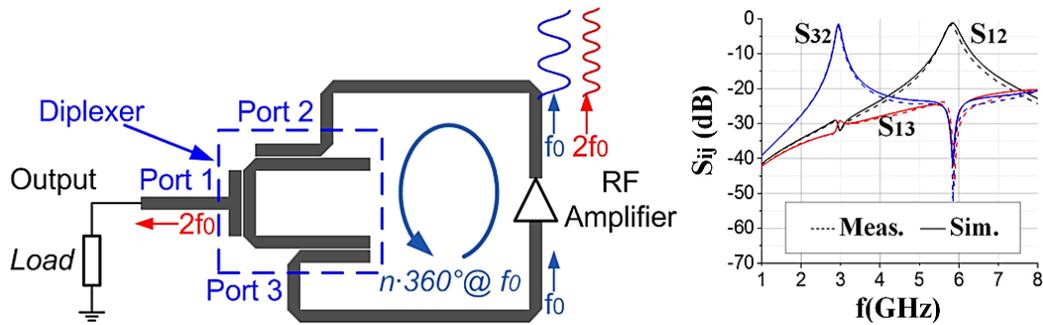


Figure 1-29. a) HFO schematic

b) Diplexer S-parameter

Figure 1-29 shows the harmonic feedback oscillator schematic and the s-parameters of the diplexer. The diplexer has a "U" structure formed from a microstrip line in $\lambda/4$ folded and integrated on a substrate Rogers RT/duroid. The s-parameters of the diplexer show two operating modes with a band-pass effect on the fundamental signal and the other on the second harmonic signal. A loadpull is applied on both circuits to vary the impedance of the load on the oscillator output port in order to have the necessary information on the frequency shift induced by the variation of impedance as well as the phase noise and power on the output port.

The frequency pulling varies from -0.74 to 1.05 % for HFO and from -19 to 15 % for FFO. The phase noise varies from -129 to -135 dBc/Hz for HFO and from -99 to -123 dBc/Hz for FFO. The output power varies from 1.86 to 7.56 dBm for HFO and from -1.5 to 9.5 dBm for FFO. The results show a big enhancement in decreasing the pulling effects and improving the phase noise.

In order to have a comprehensive comparison against the possible mitigations techniques about the effect of "pulling" on the frequency, a third version is added to the comparative study. This version uses the structure based on the fundamental frequency but adds the output port 3dB attenuator. The attenuator is non-reciprocal and can introduce 6 dB attenuation on the injected current. The measurements made on the three structures are grouped in Figure 1-30.

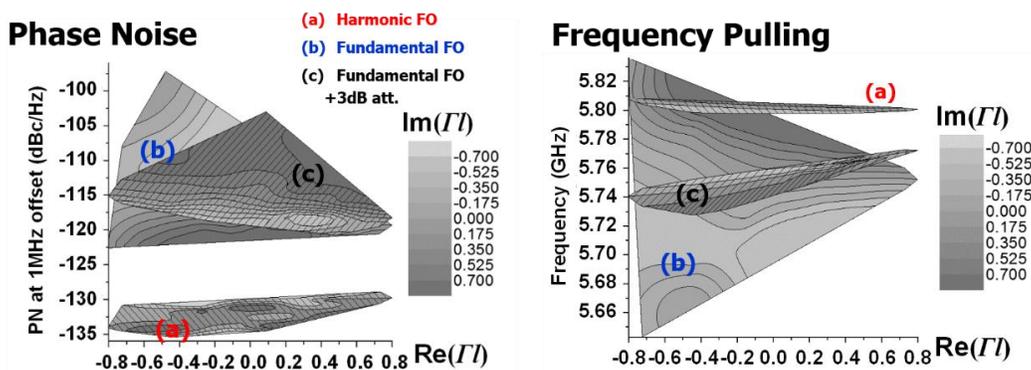


Figure 1-30. HFO vs. FFO vs. FFO+3dB attenuator a) Phase Noise b) Frequency Pulling

The topology based on the second harmonic has the best compromise and the best performance with a pulling effect of frequency 1.8 % against 7.8 % for the structure with the 3 dB attenuator. Totally, the phase noise is improved by 15 dB to be -133 dBc/Hz in HFO while the output power of the oscillating signal (7.34 dBm) is degraded by 1.4 dB compared to that in FFO (8.75 dBm).

The HFO has a disadvantage that the generation of second harmonic power in the amplifier is at the expense of the fundamental one. Choosing the load impedance seen by the amplifier to generate maximum second harmonic conflicts with optimum load impedance to generate the fundamental power, so that a compromise should be taken to have a sufficient power of fundamental power to ensure the oscillation at the feedback including the loss of the diplexer. In addition, the diplexer is a distributed element that occupy a large area with respect to the integrated circuits.

The 5G in mm wave bands are facing challenges in terms of requirements, energy consumption, and high degree of integration. In the domain of oscillators, the HFO shows good performances that well worth the attention to study the design of harmonic oscillator in the mm wave band especially in the 5G frequency candidates found in section 1.2.2. The whole oscillator should be integrated on-chip to increase the efficiency and decrease the whole size. The study will be applied and designed in CMOS technology using 28 nm Ultra-Thin Buried Oxide Fully Depleted Silicon on Insulator UTBB FD-SOI from STMicroelectronics, which will be discussed later about its advantages and specifications. First, the plan begins with choosing the second harmonic and study the performance in addition to the capability of generating output power in the PA in different topologies as common source, cascade, and with different classes as class AB, class B, class C... The idea is then developed after the differential topology is studied; in differential amplifier, the output voltage Volterra series is:

$$V_o = V_{in}^+ - V_{in}^- \quad (1.12)$$

Where

$$V_{in}^+ = V_{noise} + a_0 + a_1V_i^1 + a_2V_i^2 + a_3V_i^3 + a_4V_i^4 + a_5V_i^5 \dots \quad (1.13)$$

$$V_{in}^- = V_{noise} + a_0 - a_1V_i^1 + a_2V_i^2 - a_3V_i^3 + a_4V_i^4 - a_5V_i^5 \dots \quad (1.14)$$

Then

$$V_o = 2a_1V_i^1 + 2a_3V_i^3 + 2a_5V_i^5 \dots \quad (1.15)$$

Several issues can be noticed from the previous equation. First, the noise voltage will be canceled, which decrease the noise floor of the amplifier, which enhance the phase noise as

detailed in section. Second, the even harmonics are also canceled that mean this topology cannot generate a second harmonic signal in the ideal case. However, the third harmonic voltage is doubled which increase the level of the project to work in generating the oscillation signal at the third harmonic. In addition, the fundamental signal voltage is doubled too, which gives the opportunity to have an excess power rather than that need it in the feedback branch, so that the system will be a multi-oscillator which gives two oscillating frequency: at fundamental and at the third harmonic. Figure 1-31 shows the diagram of the proposed harmonic feedback multi-oscillator system. The LNPA block is a low noise power amplifier. It has the function of both: low noise amplifier and power amplifier. Then it is an amplifier, which generates low noise figure (NF) to decreases the noise floor of the oscillator, and outputs a large signal in order to drive the second stage PA. The function of the PA is to generate both power signal at F_0 and $3F_0$. The diplexer will separate the two frequencies with high isolation between the ports. The coupler and the phase shifter are to take a quantity from the fundamental power signal with the appropriate phase shift to ensure the oscillation conditions of Barkhausen.

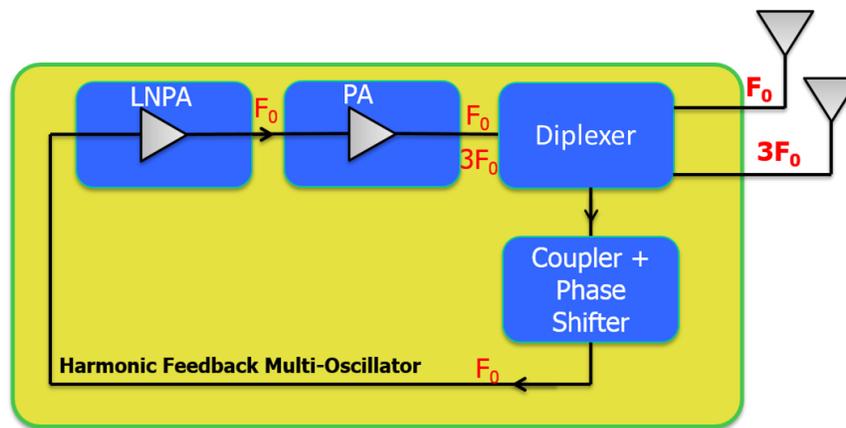


Figure 1-31. Harmonic Feedback Multi-Oscillator Plan

In the third harmonic branch, the diplexer will greatly reduce the impact of the load impedance variation and frequency pulling on the feedback loop. While in the fundamental branch, the coupler will have a power-coupling ratio around -15 dB that means the injected current on the feedback loop will be attenuated by 30 dB. This technique will reduce the impact of the load impedance variation and frequency pulling on the feedback loop, and enhance the performances of the fundamental feedback oscillator topology.

1.8 Chapter Conclusion

In this chapter, an overview of mobile technology is introduced, beginning from the theory ideas of wireless communication until the fourth generation used in our days. Then, a brief explanation of the fifth generation is introduced showing its goals, services, capabilities, and

discuss the frequency candidates at mm wave bands, in order to show a vision how the 5G will be. The flow is deepened to the transmitter architectures used in mm wave band then to the oscillator block. In the oscillator part, it explains the principle of noise generation and noise sources in electronic circuits and in semiconductors, then a model is shown for the phase noise according to Leeson model. The oscillators VCOs were branched to LC types. Each type is provided with real examples, and measurement values, in order to study the performances of each technique used. A state of arts were labeled for each type. Then the idea of fundamental feedback oscillators is explained showing its drawback and compare it with the enhanced edition of that which is the harmonic feedback oscillator. The HFO shows an improvement on phase noise, frequency-pulling effects, and on behavior with load impedance variation. Thus, the harmonic feedback multi oscillator is presented as a new technique to be studied, showing its improvement to have an oscillator that satisfy the demands of 5G oscillator block.

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Chapter 2 Technology and Design Building Issues

Chapter 2 will have three main categories, the first one will provides an overview of the challenges faced by conventional CMOS scaling. It explains fully depleted devices, such as planar UTBB FD-SOI and Tri-Gate FinFET, as the alternative solutions of bulk transistors at 28-nm and beyond, shedding the light on their designs and performance, and comparing their physical properties, electrical properties, and their preferences in different fields and applications. The second category will show the PA parameters, performances, architectures, classes showing my works on class J power amplifier and on PA stability. Then it passes to show the importance of noise figure on the system. Finally, the proposed oscillator system will be introduced.

2.1 CMOS Transistors toward Fully Depleted

Nowadays, transistor technology is going toward the fully depleted architecture; the bulk transistors are becoming more complex in manufacturing as the transistor size is becoming smaller to achieve the high performance especially at the node 28 nm. Before starting the design of the oscillator, a study is done and published in two articles by mine [1] [2], to discuss the basic drawbacks of the bulk transistors, and to explain the two alternative CMOS technology transistors: 28 nm UTBB FD-SOI CMOS and the 22 nm Tri-Gate FinFET. Then it focuses on the comparison between those alternatives and their physical properties, and electrical properties to properly set the preferences when choosing for different mobile media and consumers' applications. As the size of the transistor is downscaled, the decrease of the power consumption, the decrease of the leakage current, and the achievement of high performance should be taken into account. In bulk transistors, the two electrical terminals, source and drain, are built on doped silicon and the flow of electrons between them is controlled by the gate. As the transistor shrinks, the channel is reduced, the control of gate exercised over the channel region is reduced too, thus lowering the transistor performance [3] and allowing some unwanted leakage current flows even if the transistor is off; this leakage is increased, as the channel gets smaller as shown in Figure 2-1 [3].

In an ideal transistor, the channel potential is only controlled by gate voltage (V_g) through gate capacitance. On the other hand, the channel potential, in a real transistor, is also subjected to the influence of drain voltage through drain capacitance, which is between the drain and the channel. When the gate length is large, the drain capacitance is much smaller than the gate capacitance and the drain voltage does not interfere with V_g 's role as the sole controlling voltage. When the channel becomes short, the distance between source and drain gets smaller, and the drain capacitance becomes larger [4]. Then, the transistor will have two terminals that play a role in controlling the channel: drain and gate terminals. In addition, because the drain is connected to a potential voltage V_{DD} , a flow of electrons is occurred and the channel starts to conduct, increasing the leakage current. For a long time, researchers had believed that this problem could be solved by reducing the gate thickness to make a compromise with the largeness of the drain capacitance. But in the 90's, and after several experiments, it was realized that this is not accurate; the leakage current still occurs in the channel interface as shown in Figure 2-1 [5], the gate thickness can make

no difference, whether it is thick or thin. Thus, the solution was to find a technique in which the silicon must not be far from the gate [5].

Two facts drastically reduce device performance: leakage is one of those, and variability is the other [6]. If doping concentration is increased, then leakage is reduced but variability increases [7]. When the transistor is scaled down, the random dopants, which are the difference in implanted impurities concentration, are unacceptable from design point of view. There are other sources of variability such as the metal gate granularity, and line edge roughness as shown in Figure 2-2 [7]. The metal gate granularity is occurred when the metallization annealing results in crystallization of the metal; the metal grains will have different crystallographic orientation that leads to different work functions at the interface between the metal and the high-K material that will cause a variation of the local threshold voltage in the gate area. The line edge roughness is a result from the variations in lithography and etching in fabrication process, which causes a variation in the channel width and gate length.

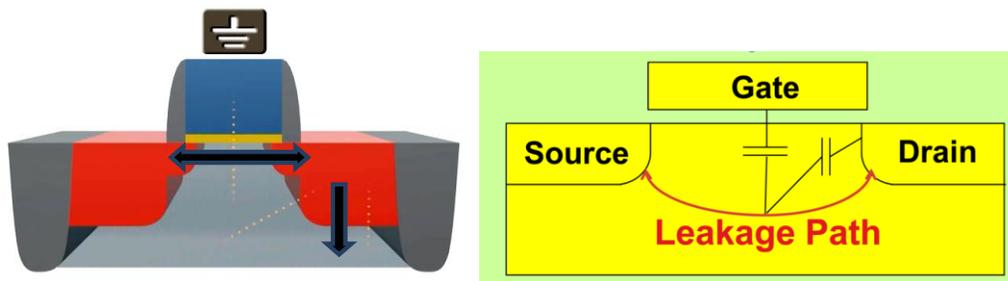


Figure 2-1. a) Bulk CMOS leakage currents at OFF state b) Leakage path [5]

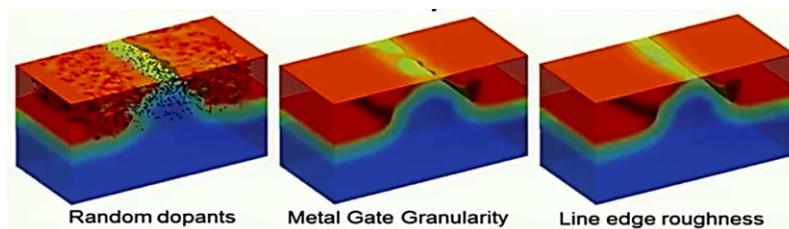


Figure 2-2. Statistical variability in 20 nm CMOS [7]

2.1.1 . Alternative Transistors

Minimizing the leakage current and improving the performance in bulk silicon transistor have been more complex when the node of the transistor arrived to 28 nm. In technology of about 28 nm and below, a new solution was introduced to reduce the complexity and to get the advantage of reducing transistor's geometry: UTBB FD-SOI and Tri-Gate FinFET. Both transistors share CMOS technology with a fully depleted transistor architecture but make the transistor a better switch.

2.1.2 28-nm UTBB FD-SOI

A 28-nm Fully Depleted Silicon On Insulator (FD-SOI) which was built without changing the fundamental geometry of the transistor lies on adding a thin insulator layer of buried oxide positioned under the channel as shown in Figure 2-3. By that, there is no need to add dopants to the channel due to the thin silicon film in the channel, thus making it fully depleted. The net effect is that the gate can now control very tightly the full volume of the transistor body which makes it behave much better than a Bulk CMOS transistor, especially as supply voltage (hence gate voltage) gets lower and transistor's dimensions shrink. The technology of very thin buried oxide is called Ultra-Thin Body and Buried Oxide (UTBB).

On the same technology node, the UTBB FD-SOI has smaller channel effective length 24nm (PB0: poly-bias 0) compared to that of the bulk's one 28 nm. Smaller channel length means shorter path flow for electrons. That reduces the time needed for the electrons' flow from the source to the drain, leading to a fast transistor [8]. UTBB FD-SOI poly-bias enables several channel lengths (PB4=+4nm, PB10=+10nm, and PB16=+16nm) to obtain different V_{th} and to optimize the leakage. This technique is used also in bulk design.

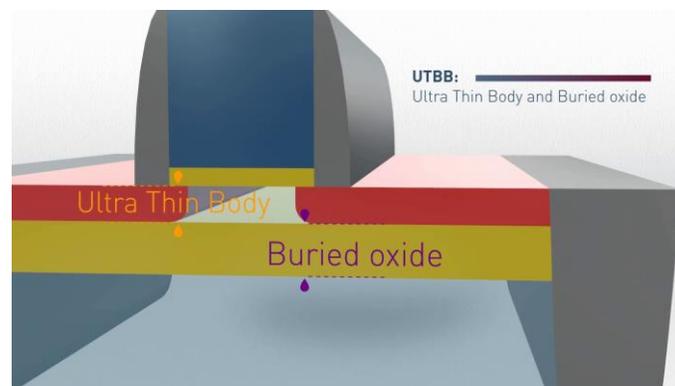


Figure 2-3. UTBB FD-SOI Geometry

The buried oxide insulator layer confines the electron when flowing from the source to the drain as shown in Figure 2-4, so it reduces the leakage current from the channel to the substrate.

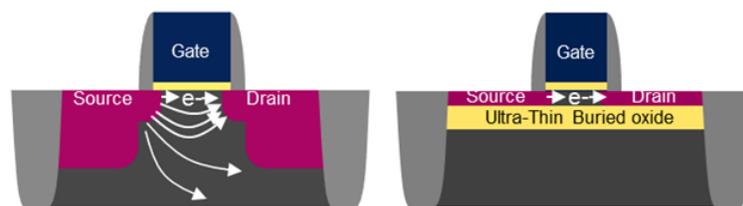


Figure 2-4. Electron Flow

The very thin silicon layer enables the silicon under the transistor gate to be fully depleted of charges; therefore, it eliminates the random dopants fluctuation; as shown in Figure 2-5(b). In

UTBB FD-SOI, field lines from gate cannot terminate in the undoped body (no charges there) because mirror charges are localized beneath BOX and the Lengths of field lines have tight distribution [9]. By that, it decreases the variability [10], and it will have better matching for short channel devices.

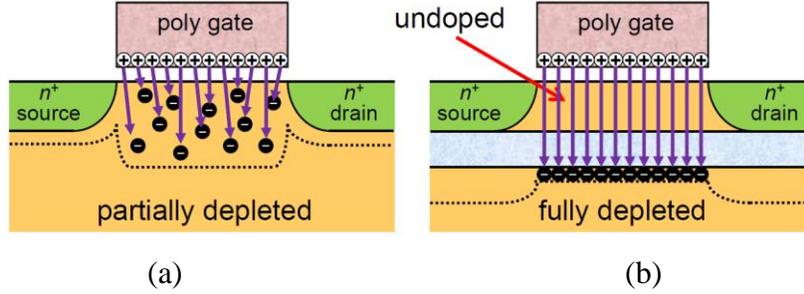


Figure 2-5. Field lines in partially depleted and fully depleted [9]

Also, the absence of channel doping and pocket implants in the fully depleted transistor produces lower noise specifications and higher gains when compared to bulk technologies. The total dielectric isolation of the channel allows for lower drain/source capacitances and leakage currents in addition to the benefit of total latch-up immunity. In addition, the reduction of the gate length decreases the gate capacitance and it has a raised source/drain epitaxy to reduce the access resistance. The saturation drain current, I_D is

$$I_D = \frac{1}{2n} \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (2.16)$$

Where μ : effective mobility, W : device width, L : channel length V_{GS} : gate to source voltage, V_{TH} : threshold voltage.

For the bulk transistor, n is:

$$n = 1 + \frac{\epsilon_{si}}{C_{ox} X_{dmax}} \cong 1.4 \text{ to } 1.6 \quad (2.17)$$

For UTBB FD-SOI, n is:

$$n = 1 + \frac{\frac{\epsilon_{si}}{t_{si}} C_{oxb}}{C_{ox} \left(\frac{\epsilon_{si}}{t_{si}} + C_{oxb} \right)} \cong 1.05 \text{ to } 1.1 \quad (2.18)$$

Where X_{dmax} : maximum depletion width, C_{ox} : gate oxide capacitance, C_{oxb} : buried oxide capacitance, t_{si} : silicon thickness.

Based on the above equations of n , it is clear that the current in UTBB FD-SOI will be higher than that of the bulk transistor by a factor of $\times (1.3-1.4)$.

The Sub-threshold slope (SS) indicates how effectively the flow of drain current of a device can be stopped when V_{gs} is decreased below V_{th} . When I_d-V_g curve of a device is steeper, sub-threshold slope will improve. It is characterized by steep sub-threshold slope that exhibits a faster transition between off (low current) and on states (high current). The sub-threshold slope factor depends on the capacitance of the CMOS technology as in Equation (4), which is degraded due to the insulated layer. The thickness of the insulated layer also plays a role on the capacitance value: as the thickness of insulated layer is increased, consequently capacitance decreases. Therefore, the sub-threshold slope will be decreased [11].

$$S_t = \ln(10) \frac{KT}{q} \cdot \left(1 + \frac{C_d}{C_i}\right) \quad (2.19)$$

Where $\frac{KT}{q}$ is the thermal voltage, C_d is the depletion capacitance, and C_i is the gate oxide capacitance.

In the weak inversion regime, there is a potential barrier between the source region and the channel region. The height of this barrier is a result of the balance between drift and diffusion current between those two regions. The barrier height for channel carriers should be ideally controlled by the gate voltage to maximize trans-conductance. The DIBL (Drain Induced Barrier Lowering) [12] effect occurs when the barrier height for channel carriers at the edge of the source is reduced due to the influence of drain electric field, upon application of a high drain voltage. This increases the number of carriers injected into the channel from the source leading to an increased drain off current as shown in Figure 2-6. Thus, the drain current is controlled not only by the gate voltage, but also by the drain voltage [13].

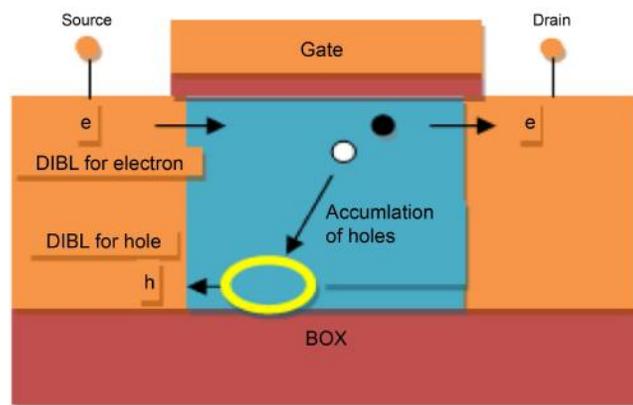


Figure 2-6. DIBL mechanism

The bulk DIBL is as in Equation (2.5):

$$DIBL = 0.8 \frac{\epsilon_{si}}{\epsilon_{ox}} \left(1 + \frac{X_j^2}{L_{el}^2} \right) \cdot \frac{T_{ox}}{L_{el}} \cdot \frac{T_{dep}}{L_{el}} \cdot V_{DS} \quad (2.20)$$

Where ϵ_{si} : silicon permittivity, ϵ_{ox} : gate oxide permittivity, X_j : junction depth, L_{el} : electrical channel length, T_{ox} : gate oxide thickness, T_{dep} : depletion width in bulk transistor, V_{DS} : Drain Source voltage.

The DIBL of UTBB FD-SOI is:

$$DIBL_{FD\text{SOI}} = 0.8 \frac{\epsilon_{si}}{\epsilon_{ox}} \left(1 + \frac{T_{si}^2}{L_{el}^2} \right) \cdot \frac{T_{ox}}{L_{el}} \cdot \frac{T_{si}}{L_{el}} \cdot V_{DS} \quad (2.21)$$

Where T_{si} is the channel thickness.

By comparing Equation (2.5) and Equation (2.6), the UTBB FD-SOI has better DIBL than that of the bulk transistor because UTBB FD-SOI takes into consideration the ultra-thin channel (T_{si}).

2.1.3 Body Bias

To improve the transistor performance, a voltage can be applied to the substrate. This method is called Body Biasing, which facilitates the creation of the channel between the source and the drain resulting a faster switching. Because of the ultra-thin layer in FD-SOI, the biasing creates a buried gate below the channel making the transistor act as a double vertical gate transistor. Scaling down the silicon thickness under the gate of a FD-SOI transistor below 5nm [14] is optimum on SOI substrate in order to limit the leakage current flows as shown in Figure 2-7 [15].

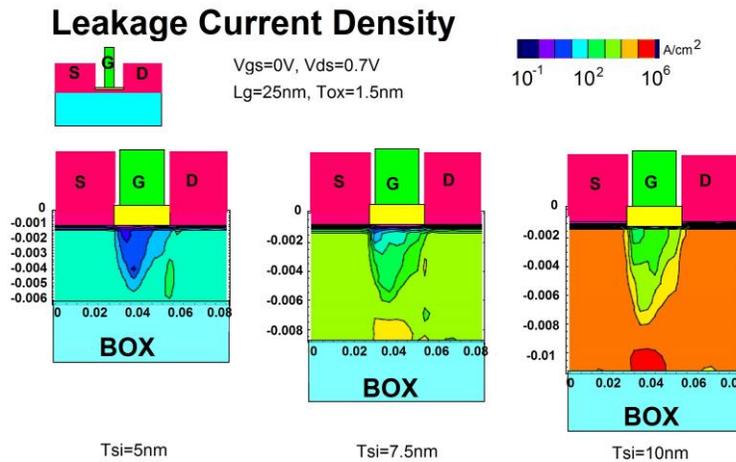


Figure 2-7. Leakage current w.r.t silicon thickness [15]

This Ultra-thin body and BOX (UTBB) FD-SOI transistor architecture (7 nm silicon thickness and 25 nm BOX thickness) has a stronger body effect than bulk transistors and therefore enables effective threshold voltage (V_{th}) management through body biasing. The BOX thickness

(25 nm) is a compromise between an increased parasitic source/drain to substrate capacitance and enhanced body effect. While in bulk technology, the ability of doing body biasing is limited due to the parasitic current leakage, the buried gate in UTBB FD-SOI prevents any leakage in the substrate. Thus, it allows much more voltage on the body leading to a significant boost performance. The range of back-gate biasing in UTBB FD-SOI is quite wider by a factor of 10 (i.e. $-3\text{ V} < V_{BB} < 3\text{ V}$) compared to the bulk technology ($-300\text{ mV} < V_{BB} < 300\text{ mV}$). And the slope of threshold voltage is 85 mV/V vs. 25 mV/V as shown in Figure 2-8 which lead to a significant drive current boost [16]. If V_{BB} is positive, then it is a forward body bias (FBB). But, if it is negative, then it is a reverse body bias (RBB), for NMOS transistor and vice versa for the PMOS transistor.

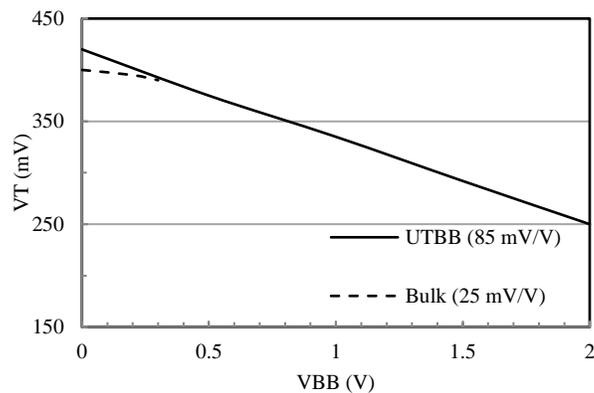


Figure 2-8. Threshold voltage w.r.t. UTBB FD-SOI & Bulk body bias voltage

The characteristics of UTBB FD-SOI vertical double transistor allow the creation of new concept in processor design. Different voltage can be applied independently at the top and at the buried gate [17], and dependently change the characteristics of the transistor. By choosing the optimum voltages at the top gate and the buried one, the transistor characteristics can transform from high performance to low power transistor.

Since the current leakage strongly depends on the threshold voltage V_{th} , different V_{th} transistors can be optimized for speed and low power as shown in Figure 2-9. A higher I_{ON} maximizes the circuit speed because it reduces the charging time of the pad output capacitances of the transistor cell. A lower V_{th} can achieve that higher I_{ON} . However, lowering V_{th} increases exponentially the leakage current. That leads to a compromise between speed and power that the designer should balance.

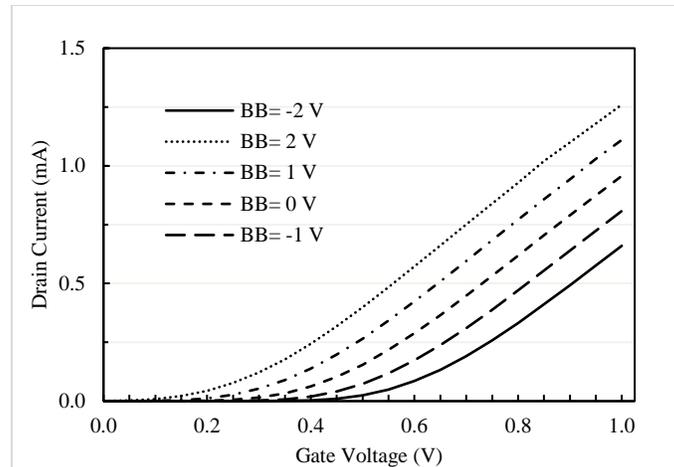


Figure 2-9. Simulation of the shifting effects on the V_T introduced by the back-gate biasing n-channel UTTB FDSOI.

Body bias can be used to vary the maximum frequency: while the FBB can be applied to increase the frequency, the RBB can be applied to decrease it. The dynamic body bias combined with a different voltage frequency scaling (DVFS) can provide the best performance power tradeoffs. Figure 2-10 gives an example for NMOS UTBB FD-SOI transistor. By raising the V_{DD} by 100 mV, the performance is raised on the penalty of larger active power. Similarly, by reducing the V_{DD} by 100mV, the leakage and active power is reduced. It can be applied as a FBB to reduce the threshold voltage by 60mV to introduce frequency gain and more efficient active power, or it can be applied as an RBB to reduce the leakage power as shown in Figure 2-11 [18]. Some points can be optimally selected to make a tradeoff between active and leakage power as in Figure 2-10. Therefore, by overdriving the V_{DD} of the device and applying FBB, a best performance can be reached with $\times 1.6$ of the original maximum frequency. On the other hand, lowering the V_{DD} reduces active power but sacrificing the performance. Moreover, by applying RBB, the leakage power is reduced as well as the maximum frequency, which is reduced to the half. The leakage can achieve 1 pA/um [19].

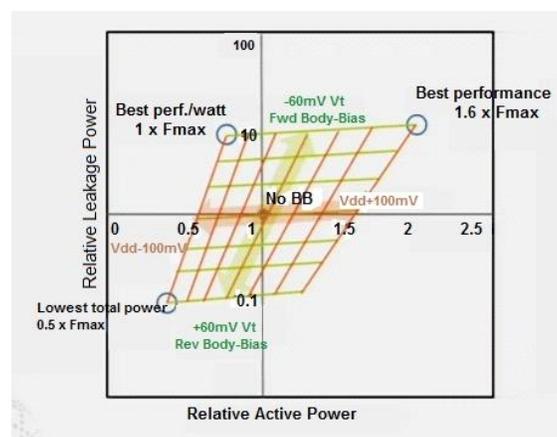


Figure 2-10. Combining DVFS with body Bias [19]

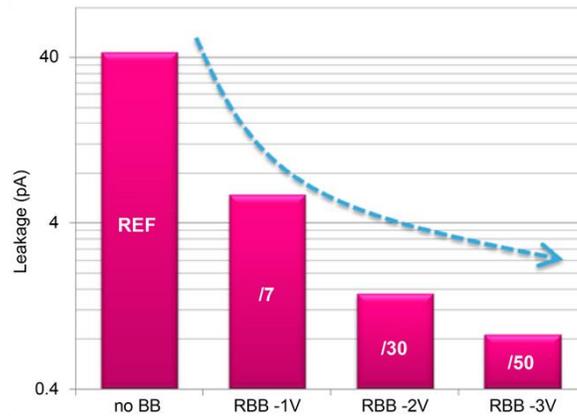


Figure 2-11. RBB Impacts on leakage current [18]

The lower leakage current makes the transistor less sensitive to the temperature; Figure 2-12 is a demo of a processor using the 28-nm UTBB FD-SOI with other bulk transistor, which shows the difference in temperature and power efficiency improvement [20].



Figure 2-12. Temperature of UTBB vs Bulk [20]

The 28-nm UTBB FD-SOI offers two types of transistors to optimize leakage and performance: RVT (conventional well) and LVT (flip well) as seen in Figure 2-13. The forward and reverse bias ranges depend on the doping of the well in which the transistor is residing; keeping in mind that going beyond the bias range creates a parasitic diode between the 'n' and 'p' wells. If optimized for forward body bias using the 'flip well' doping, the effective gate voltage of the transistor can be boosted by as much as 3V, but this restricts the reverse bias shift to -300mV. Conversely, using the conventional well, reverse body bias can be extended to -3V, limiting forward bias to 300 mV [21]. However, if only single transistor is used, NMOS or PMOS transistor (not CMOS), the body bias voltage can be used from -3V to 3V.

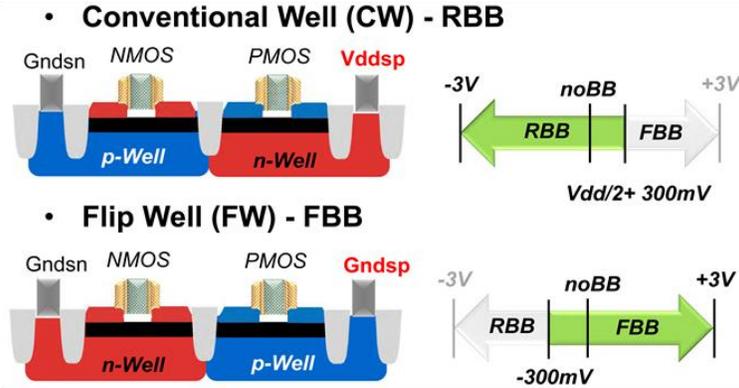


Figure 2-13. Types of UTBB-FD-SOI Transistors

2.1.4 22-nm Intel’s 3D Tri-Gate Transistor

In a conventional planar FET transistor, the current flowing through the channel is closely related to the width (W) of the device, divided by the length (effective L). As the industry scales to smaller nodes, it is ideal to decrease effective L, which improves the drive strength of the transistor. However, shorter transistors have less control over the channel and exponentially higher sub-threshold leakage. To control leakage, the channel is heavily doped, which makes everything more susceptible to variability. A 3D Tri-Gate transistor looks a lot like the planar transistor but with one fundamental change. Instead of having a planar inversion layer (where electrical current actually flows), Intel’s 3D Tri-Gate transistor creates a three-sided silicon fin that the gate wraps around, creating an inversion layer with a much larger surface area as shown in Figure 2-14. The width ($W_{\text{effective}}$) of a Tri-Gate transistor is the sum of all three sides: twice the fin height plus the fin width, which is approximately the 2x of the planar width [22].

The gate exerts more control over the flow of current through the transistor; it surrounds the channel on all three sides and has much better control so that all the charge below the transistor is removed (fully depleted) and there is no depletion capacitance, so it is tightly controlled. This reduces dopants variability because no - or lightly- doping is needed to control the channel. The “fully depleted” characteristics of Tri-Gate transistors provide a steeper sub-threshold slope that reduces leakage current (from 0 V to 0.4 V). The DIBL is given as in Equation (2.7) which is the lowest compared to bulk and UTBB FD-SOI transistors.

$$DIBL_{TRI-Gate} = 0.8 \frac{\epsilon_{si}}{\epsilon_{ox}} \left(1 + \frac{T_{si}^2}{4L_{el}^2} \right) \cdot \frac{T_{ox}}{L_{el}} \cdot \frac{T_{si}}{L_{el}} \cdot V_{DS} \quad (2.22)$$

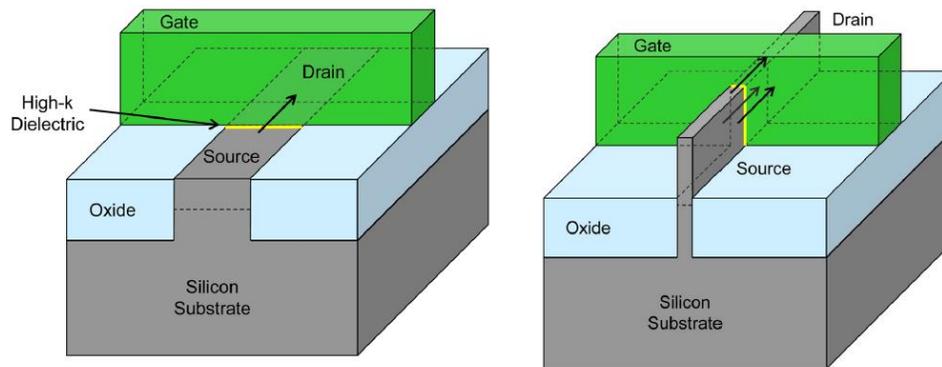


Figure 2-14. Planar (to the left) and Tri-Gate FinFETs [23]

The steeper sub-threshold slope can also be used to target a lower threshold voltage, allowing the transistors to operate at lower voltage to reduce power and/or improve switching speed as shown in Figure 2-15. To build transistors with different performance and leakage, multiple fins are ganged together and share a single gate essentially multiplying the width (higher drive current), and the threshold voltage can be varied by adjusting gate length or by low doping the channel [24].

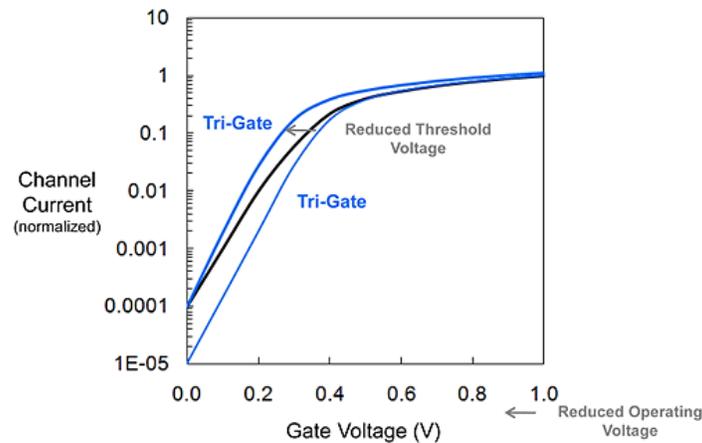


Figure 2-15. Tri-Gate FinFET Drain current w.r.t. gate voltage [23]

The 22-nm Tri-Gate transistors are 18% and 37% faster at 1V and 0.7V respectively than Intel’s 32nm transistors [23]. When transistors are not fully switched on– at low voltage, it shows a very big improvement over conventional planar FET transistor closer to 37% as shown in Figure 2-16. This improves the frequency, but still in practice, the slowest circuits determine the actual frequency in the chip. In addition, the operation at lower voltage comes with good performance, reducing active power by >50% ($P \sim F * V^2$) [23].

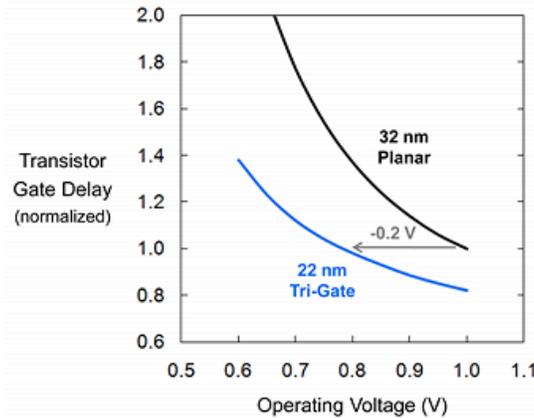


Figure 2-16. Tri-Gate FinFET Performance Improvement [23]

The Tri-Gate FinFET transistors are fully depleted so the carriers flow in threshold and sub-threshold voltage in different places compared to where they flow in high gate bias condition. As seen in Figure 2-17, the charges distribution is at the middle of the channel, and by increasing the gate bias voltage, the charges start to move to the interface and can have fringing effects. Therefore, the charges distribution in the channel is not uniform and complicated. More charges are located at the sharp corner, which will have strong field. Then current passes at the middle at a low bias, and it passes at the surface at a high bias. Intel chooses the trapezoidal shape of the fin while in terms of performance the rectangular fin shape is optimum more than trapezoidal by about 15% [7] as shown in Figure 2-18 and slightly better SS and DIBL [25]. Intel, maybe, wanted to avoid the high concentration of the charges at the two corners of the rectangular shaper, so it goes with the trapezoidal shape, which has one angle where the charges distribution is highly concentrated at high bias. Moreover, the second generation of Intel transistor (14-nm) is going to be more rectangular.

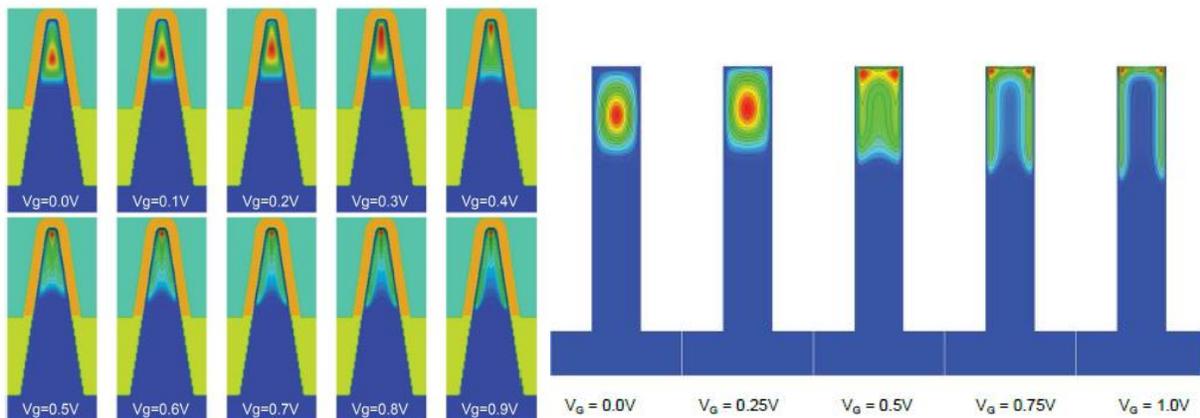


Figure 2-17. Charge distribution in the taper and rectangular Fin respectively [7]

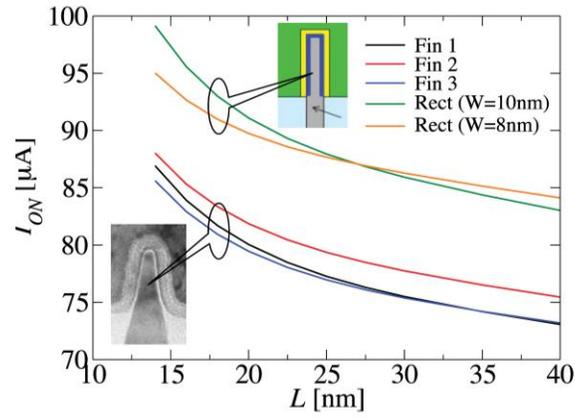


Figure 2-18. Comparison of I_{ON} between rectangular and taper Fins for equivalent width and heights [7]

The 3D nature of Tri-Gate FinFET transistor introduces a new number of parasitic capacitances to be considered. For example, between the gate and the source there will be two sided capacitors other than the top and the bottom capacitors as shown in Figure 2-19 [26]. And the transistor which has multiple fins increases the parasitic resistance (from each fin) and adds interconnect capacitances between fins [26] [27].

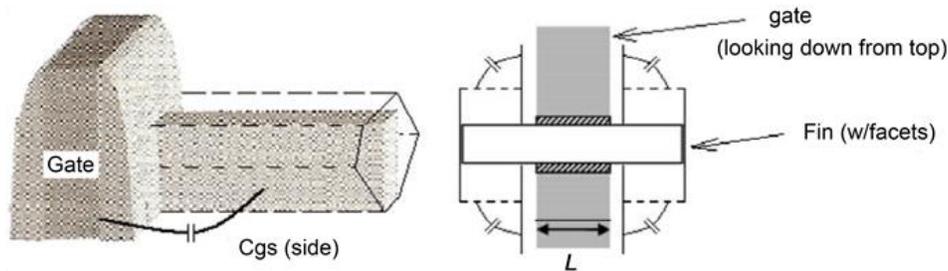


Figure 2-19. Tri-Gate FinFET additional parasitic capacitors [26]

Also, the fabrication process is complicated and more complex than planar technologies especially for the vertical etching, which gives more opportunities to have variations between the shapes and heights of the Fins [28] which causes a variation of the threshold voltage of each transistor [29] as shown in Figure 2-20.

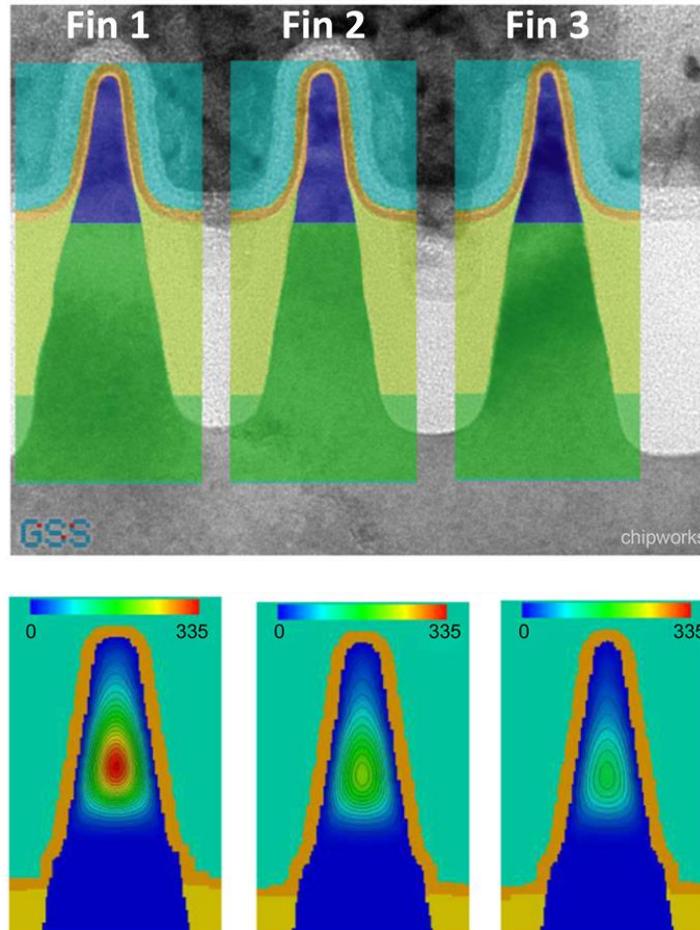


Figure 2-20. Different fins shape due fabrication [7]

2.1.5 28-nm UTBB FD-SOI VS 22-nm Tri-Gate FinFET

Both UTBB FD-SOI and Tri-Gate FinFET share CMOS technology with a fully depleted transistor architecture where any additional voltage to the gate generates charges, which make the transistor a better switch. As a result, lower supply and threshold voltage give much lower dynamic power dissipation. The sections below compared the physical and electrical characteristics of both transistors, and then make an analysis to determine which is more appropriate in analog and digital applications.

2.1.5.1 Individual Transistor Comparison

A. Electrostatic

The Tri-Gate FinFET have better electrostatics (DIBL and SS) and higher drive current per unit area but higher leakage current; A comparison summary is shown in Table 2-1 [30] [31] [32].

Table 2-1. DIBL, SS, ION, and IOFF comparison between Tri-Gate FinFET and 28-nm UTBB

	28 nm UTBB of $T_{soi}=7$ nm [30]		Intel 22 nm Tri-Gate FinFET [31] [32].	
	NMOS	PMOS	NMOS	PMOS
I_{on} ($\mu A/\mu m$)	1070	610	1260 @ 0.8 V_{DD}	1100 @ 0.8 V_{DD}
I_{off} (nA/ μm)	16	30	100	
DIBL (mV/V)	90-95	90-95	46	50
SS (mV/dec)	85-90 @ 1V V_{DD}		69	72

B. Capacitance

The UTBB has lower gate capacitance and less effective capacitance than that of the Tri-Gate, which makes the UTBB FD-SOI capable to work on higher frequency. For example, at the point where UTBB and Tri-Gate have an I_{on} (+30%) more than that of the bulk transistor of $I_{ON} = 900 \mu A/\mu m$, the gate capacitance of the UTBB transistor still constant while the Tri-Gate width transistor is increased by 30% and the gate capacitance by 30% [33]. Then, the very high effective drive current per sq μm of the Tri-Gate FinFET is mitigated somewhat by the higher parasitic capacitances, especially with the multiple fins common gate transistor.

C. Random Dopant Fluctuations

The UTBB is undoped channel device so it is better in lowering the random dopants fluctuations (drops by $\times 3.3$ [33]) and better device matching because the Tri-Gate needs low fin doping (fluctuations drops by $\times 1.8$ [33]) and as the height of the fin increases, the dopants fluctuations are increased too [34]. In addition, there is a mismatch between the neighbor fins [35].

D. Flexibility

The UTBB is more flexible and have more management over speed and power because of the Body Bias technique, which offers a threshold voltage control [36] while Tri-Gate has no body bias [16].

E. Sources of Variability

The sources of variability are the T_{box} (buried oxide thickness) and T_{si} (silicon thickness) in UTBB transistor while in Intel Tri-Gate transistor, the sources are the H_{fin} (fin height), D_{fin} (fin dimension), and Fin taper [24].

F. Fabrication Complexity

For fabrication, the Tri-Gate is process that is more complex. It faced with the challenges of a disruptive approach that requires mastering technological processes compatible with tri-dimensional geometries (in terms of doping, etching, etc.), while the UTBB is much more in continuity with planar Bulk process and may be seen as a better choice of benefits vs. manufacturability trade-off than Tri-Gate FinFET [37] [38].

G. Cost

The cost is a major challenge facing chip manufacturers. Intel estimates that FD-SOI increases the added cost of a finished wafer by 10%, compared to 2% - 3% for Tri-Gate. But, Global Foundries said that 20% lower die cost and a 50% lower mask cost than Tri-Gate FinFET [19]. There is a point that the extra cost of SOI wafers is offset by cost savings made because no longer need to dope the channels, so the extra cost of the start wafer (SOI) is absorbed.

2.1.5.2 Transistor Characteristics in Chips

In a chip embedding billions of transistors, the characteristics of each transistor are not exactly the same. The main reason of this is the different quantity of dopants injected in the channel during manufacturing process. In UTBB FD-SOI, dopants usage is greatly reduced which limits the variability. As a result, the characteristics of each transistor are closer to the average. That allows the transistors to run faster since less margin need to be allowed for process variability. Tri-Gate FinFET has a bigger margin of variability because the complex process of the vertical Fin etching can't give the same Fins shape; that also leads to variant threshold voltage for each transistor.

Such comparisons [39] show that the UTBB FD-SOI is more suited for low power/low leakage applications than the Tri-Gate due to its efficiency at low power. However, the Intel Tri-Gate FinFET is more suited for the high performance (high power) application than the UTBB FD-SOI. Nevertheless, designers should take also into consideration another factor the type of the circuit: analog, RF, digital, memories, etc.

A. For Analog and RF Blocks

Analog designers look for the gain, noise figure, flicker noise, mismatch, power capabilities and f_T/f_{MAX} (f_T : Maximum cut-off frequency, f_{MAX} : Maximum oscillation frequency). Tri-Gate FinFET can achieve significantly higher gain and lower flicker noise than planar-bulk and UTBB FD-SOI MOSFETs due to its superior electrostatic integrity, higher carrier mobility, and lower DIBL. However, gain is lower at higher frequencies due to large source/drain resistance, and the higher parasitic capacitance (effective capacitance with miller component from region between FINs) limits the maximum frequency and raises the noise figure. Differently, the total dielectric isolation of the channel in the UTBB FD-SOI creates lower gate and source/drain capacitance, reduces source/drain leakage currents, and improves latch-up immunity. Additionally, the absence of channel doping and pocket implants in the fully depleted transistor produces lower noise specifications, lower mismatch, and increase the gain. UTBB FD-SOI has higher f_T/f_{MAX} than that of Tri-Gate FinFET due to reduced gate capacitance and raised- S/D (Source/Drain) epitaxy which reduced the access resistance $\{f_T \text{ of N(P): } 300(260) \text{ GHz and } f_{MAX} \text{ of N(P): } 170(120) \text{ GHz [40]}\}$. All these advantages, in addition to the large R_{ON}/R_{OFF} ratio, make UTBB FD-SOI more attractive and favorable to the designers of RF circuits such as power amplifier, mixer, baseband amplifier, and low noise amplifier. The high gain and lower noise with high-speed switch (due to lower parasitic capacitance) attract the analog circuits too. For example, the ADC will be smaller and higher speed, or the LNA will have higher gain and smaller noise figure. So, UTBB FD-SOI has

higher success than Tri-Gate FinFET in analog and RF application [41] [18]. A common problem in both transistor is present for power amplifier designer, which is the limitation of output power due to the low supply voltage V_{DD} and low breakdown voltage.

Global Foundries made a case study of smart watch, which described as co- integrated circuit with low power and RF enabling in [19], where it has a CPU frequency of 1.5 GHz, operating voltage at 0.6 V, and an integration path of Bluetooth, and Wi-Fi with power management integrated circuit. The comparisons are done between 40-nm low power bulk transistor, 28-nm super low power bulk transistor, 28-nm UTBB FD-SOI, and Tri-Gate FinFET. It starts with the 40 nm device; it is interesting to see the battery life improvement over the 40 nm, 28-nm, 28-nm UTBB, and Tri-Gate FinFET as seen in Table 2-2. The battery lifetime is increased due to the power reduction at the ISO frequency, from 4.5 days to approximately 13.85 days with 109.7 mw/day where the Tri-Gate FinFET approaches 11.58 days with 131.2 mw/day. If the forward body bias technique is applied, the power consumed is decreased 76.3 mw/day and the battery life continues increasing to 19.91 days, which is around x5 of the 40-nm device. Other than that, a Bluetooth and Wi-Fi are added to the UTBB with FBB, and it still has lower power consumption (108.3 mw/day) than Tri-Gate FinFET and more battery life (14 days).

Table 2-2. Smart watch performance over transistors [19]

Smart watch	Power @ ISO Freq	Freq.@ ISO power	mW/Day (static+active)	Battery Life (Days)
<i>40LP</i>	1	1	334	4.65
<i>28SLP</i>	0.71	1.56	238.6	6.37
<i>FINFET</i>	0.39	2.8	131.2	11.58
<i>FD- SOI</i>	0.33	2.55	109.7	13.85
<i>FD+FBB</i>	0.23	2.97	76.3	19.91
<i>FD+FBB+BLE</i>	0.23	2.97	85.9	17.7
<i>FD+ FBB+ BLE+WiFi</i>	0.23	2.97	108.3	14

B. For Digital Blocks

In big digital blocks as CPUs and servers, increased power efficiency and decreasing the volume of the digital integrated circuits are the most important requirements. Increasing performance is done by reducing the power:

$$P = \alpha CFV_{dd}^2 + I_{leakage}V_{dd} \quad (2.23)$$

Where V_{DD} has more majority role, Intel 22-nm Tri-Gate FinFET transistor has 37% improved speed performance and 50% power reduction at 0.7 V over the 32-nm planar FinFET as mentioned before. On the other hand, the 28-nm UTBB FD-SOI transistor can achieve the same Tri-Gate FinFET performance at 200 mV_{lower} V_{DD} or (350 mV_{lower} V_{DD} with FBB = 1.5 V) [19]. The other

comparison is that the Tri-Gate FinFET has the best digital scaling area over the UTBB and the Bulk CMOS, which gives priority for the Tri-Gate FinFET. The advantage of the leakage in UTBB transistor will not make a big difference in reducing the power because most of the transistors in CPUs and servers are working and not in standby. Therefore, if it's really a big digital chip with high density and without significant analog integration, where leakage is not a biggest concern and ultimate performance is more favorable, the Tri-Gate FinFET will be absolutely preferable.

C. For Embedded SRAM

Power efficiency and reductions in both static and dynamic power dissipation are needed to improve efficiency. Both transistors have high performance (if UTBB is with FBB). For SRAMs, the point of difference is that the biggest number of transistors can be in standby mode while some others are writing or reading, so lowering leakage can make a big improvement on the power consumption.

The UTBB with RBB (in N-MOS) is the best choice for lowering leakage. Other advantage of the UTBB is the lower gate capacitance, which means that lower row of transistor can be used in addition to the better matching which leads to build smaller SRAMs. Also, the UTBB FD-SOI transistor has the best SER (soft error rate) because of the radiation hardness that is done by its isolation; the gain against the Alpha radiation with respect to bulk CMOS is x1000 for UTBB and x15 for Tri-Gate FinFET, while for Neutron radiation: x100 for UTBB and x10 for Tri-Gate FinFET [42]. In addition, the radiation hardness gives a benefit for sensors and automotive applications. Those reasons make the UTBB preferable for embedded SRAMs circuits.

Currently, STMicroelectronics is working to produce 14-nm UTBB FDSOI transistor, which boost 30% speed and 30% less power consumption [33]. Intel Tri-Gate FinFET, on the other hand, is in the produced the 14nm and in the process to produce 10nm transistors, which decrease the parasitic capacitance and resistance; a challenge to enter the RF applications. Tri-Gate FinFET can be built on SOI substrate as IBM is doing, which has simpler manufacturing, better control over electrostatics in vertically aligned thin channel area [43] [44], higher on state drive performance [45], and back bias capability [46], but higher heat dissipation.

Transistor scaling is a continuous improvement for UTBB FD-SOI with a roadmap: from 28-nm, to 22-nm, to 14-nm, to 10-nm and below which will face physical limitation related to the electrons. Tri-Gate FinFET is more momentum [47]; it is a 3D structure, which starts a new generation of transistors, it has a big chance to grow, and it has more performance per unit volume.

In this work, the 28 nm FD-SOI CMOS technology from STMicroelectronics is the proposed kit to be worked on due to its advantages in the RF design.

2.2 Power amplifier

The power amplifier (PA) is the main block in the transmitter. It is usually intended to provide sufficient power to the signal transmitted through the antenna. By its role, the PA is an

important contributor in the energy consumption of the RF and mm wave transmission. Indeed, it can represent between 30% and 60% of the total dissipated power. Before entering the design phase, it is necessary to review the parameters characteristics of a power amplifier [48]. They will thus make it possible to compare the amplifier designed with the state of the art. It includes the saturated power, linearity, efficiency, gain, stability, bandwidth and the area occupied. Starting from the block diagram of Figure 2-21, these parameters can be found.

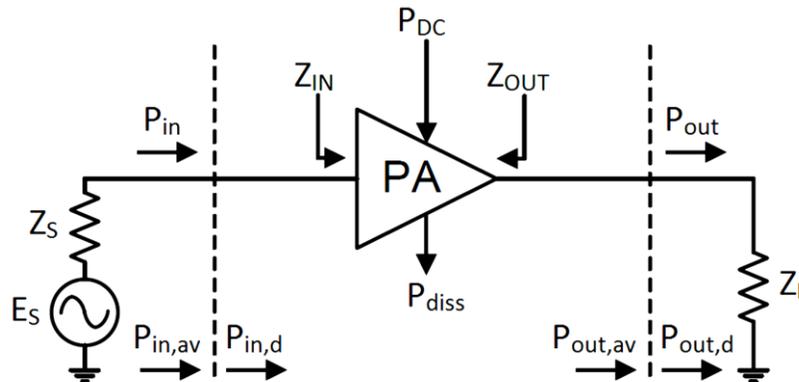


Figure 2-21. PA Parameters

Where

E_s	mm wave source
P_{in}	Input power of the PA
P_{out}	Output power of the PA
$P_{in,av}$	Power available from the source
$P_{in,d}$	Power delivered to the amplifier
$P_{out,av}$	Power available from the amplifier
$P_{out,d}$	Power delivered to the load
P_{DC}	DC power supplied to the amplifier
P_{diss}	Power dissipated by the amplifier
Z_S	Source impedance of the generator
Z_L	Load impedance of the PA
Z_{in}	Input impedance of the PA
Z_{out}	Output impedance of the PA

2.2.1 Gain

The power gain is the amplification factor of an input signal on the output load signal of the PA. The input and output impedance mismatches of the amplifier lead to define several types of gain. If the power transfer between the generator and the power amplifier is optimal, and if all the output power of the amplifier is transmitted to the load, then there is matching of the power gain so $P_{in,av} = P_{in,d}$ and $P_{out,av} = P_{out,d}$. In addition, because of the reflection of the waves at the entrance and the exit of the amplifier, the power available from the generator is greater than

the input power of the amplifier, and the maximum output power of the amplifier is greater than the power transmitted to the load. This leads to different gain definitions:

$$\text{Available gain} = G_A = \frac{P_{\text{out,av}}}{P_{\text{in,av}}} \quad (2.24)$$

$$\text{Operating gain} = G_P = \frac{P_{\text{out,d}}}{P_{\text{in,d}}} \quad (2.25)$$

$$\text{Transducer gain} = G_T = \frac{P_{\text{out,d}}}{P_{\text{in,av}}} \quad (2.26)$$

The transducer gain can take into account the input and output matching losses of the PA, and then it is the most used. Other gains are rather used to calculate the stability and losses of the matching networks at small-signal analysis.

2.2.2 Efficiency:

Defining a power amplifier only by its power gain is limited. Indeed, with more and more devices and mobile applications, the power amplifier must offer the highest possible efficiency, in order to optimize the duration of use in accordance with the intended application. Two efficiency equations are defined: the drain efficiency η_D (for MOS transistors) and the Power Added Efficiency (PAE) [48].

The drain efficiency (η_D) is directly translates the conversion of DC power into RF power achieved by the power amplifier:

$$\eta_D = \frac{P_{\text{out}}}{P_{\text{DC}}} \quad (2.27)$$

However, when the input power is at a significant level compared to the power output, this efficiency definition becomes insufficient. The power added efficiency (PAE) reflects the impact of input power, and it is defined as:

$$PAE = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC}}} \quad (2.28)$$

It can be expressed in terms of drain efficiency and transducer gain as follows:

$$PAE = \eta_D \left(1 - \frac{1}{G_T}\right) \quad (2.29)$$

At mm wave bands, the gain of the power amplifiers is not significant at point to neglect the input power. That's why the figure of merit that mostly used in this case is the power added efficiency. The drain efficiency is frequently used for high gain amplifiers when the input power is negligible compared to the output power.

2.2.3 Linearity:

The PA linearity is the ability to amplify an input signal with minimal distortion. The amplifier should be applied by a sinusoidal continuous signal input while performing a sweep range of input power (P_{in}) as shown in Figure 2-22. where three zones can be defined:

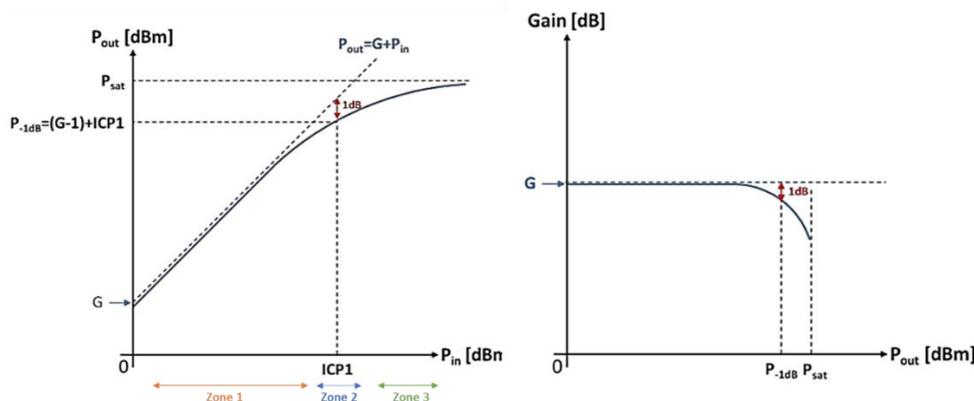


Figure 2-22. PA Linearity Behavior

- Zone 1 or linear zone: the output power evolves linearly with input power. P_{OUT} is then proportional to P_{IN} of a factor equal to the gain G defined before.
- Zone 2 or compression zone: Nonlinearities begin to appear, and gain decreases with increasing P_{IN} . The point where the gain is 1 dB lower than the gain of the linear zone is the point of 1 dB compression, shown in Figure 2-22 at the coordinates ($ICP1$; P_{1dB}).
- Zone 3 or saturation zone: In this area, the output power remains constant regardless of the P_{IN} value. It reaches a maximum P_{SAT} value. The power who cannot refer to the fundamental is then divided on different harmonics. This saturation zone implies performance degradation transistor, until the destruction of the component in case of extended operation in this area

A compromise between linearity and efficiency: the PA is more linear for a low P_{IN} , but in return the transfer of P_{DC} to P_{RF} remains low, which leads to less efficiency. As the input power increases, the efficiency increases, and as the output power compresses and the gain decreases, PAE decrease. There is an optimal value of PAE occurs a few decibel beyond the 1 dB compression point. A typical example is shown in Figure 2-23 by [48].

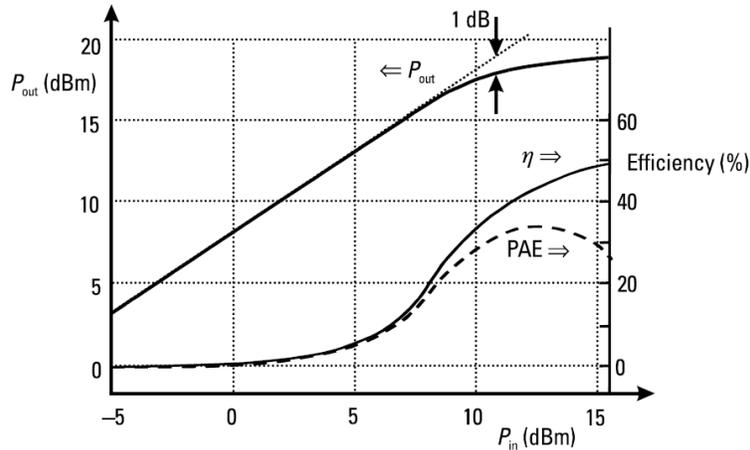


Figure 2-23. Gain and power-added efficiency versus input power

These nonlinearities on the amplitude of the output signal are also referred to as conversion AM/AM. In addition, by plotting the phase of the output signal depending on the power of the input signal, a second type of nonlinearity AM/PM is highlighted (Amplitude/Phase conversion) as shown in Figure 2-24. These two types of non-linearity therefore cause a distortion of the output amplitude and phase signal.

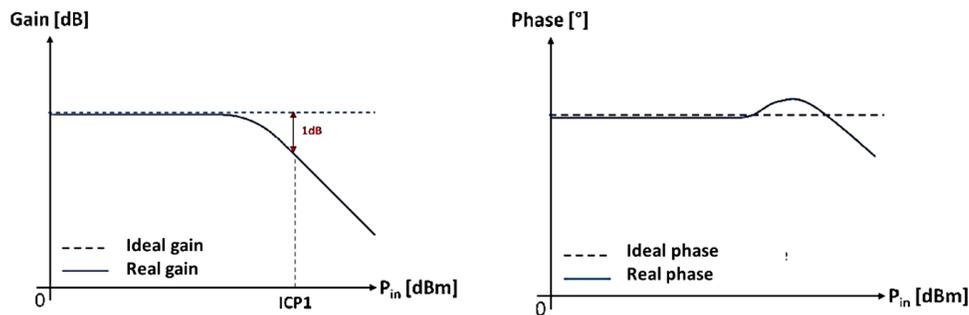


Figure 2-24. Amplitude and Phase non-linearity

2.2.4 PAs Architectures

Several architectures PAs were used in the mm wave band. They can be classified into three categories: common mode, differential or pseudo-differential, and balanced mode.

2.2.4.1 Common Mode Single Ended

The common mode single ended is the simplest and fastest to design. However, this structure is very sensitive to the ground plane that can make stability problem and bring the PA to oscillate. Its power output is based on the number of stacked transistors and their ability to deliver the power, under a given voltage. It uses DC block capacitors on high frequency path and choke inductance with the DC supply voltage. In addition, it needs an electrostatic protection circuit to prevent any degradation during manufacturing process.

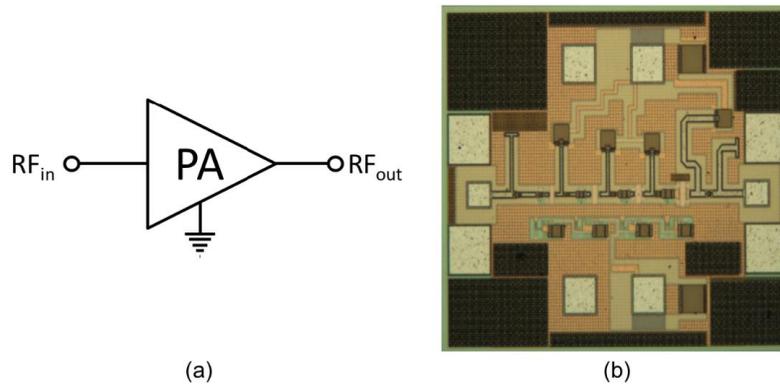


Figure 2-25. a) Single-ended topology schematic b) Implementation example [49]

The single ended architecture consist of two topology, which are mostly used: common source and cascade as shown in figure. The common source (CS) and cascode topologies are used at millimeter frequencies. A transistor in common source has low power gain, problems with stability, and low output impedance. The gate to drain capacitance C_{gd} is like a feedback loop that degrades the insulation and gain. The drain to source capacitance C_{ds} increases with the size increase of the transistor, and it consistently reduces the output impedance. This structure; nevertheless, achieves good voltage excursion which extends from the knee voltage to $2 V_{DD}$ in class A; thus, ensuring good linearity. The cascode structure that consists of two transistors has a priori better gain, better stability, and a wider bandwidth than the common source structure. Indeed, it reduces the input-output capacity and thus improves insulation. This circuit is much more sensitive to parasites, including those related to the connection between the two transistors. The C_{DSB} capacitance (source of the upper transistor, drain of the second transistor, and the body) formed with the substrate absorbs part of the millimeter signal and drops the gain. The output power is less than the common source and the noise figure is slightly bigger than of that in common source.

Table 2-1 summarizes the performance of these two circuits, cascode and common source, according to the main characteristic parameters. We deduce the most suitable topology depending on the point to be optimized. Thus, a common source installation is recommended if you wish to allow the high output power, low noise figure, good linearity, and efficiency. A cascode arrangement is more suitable for the realization of broadband circuits due to its high stability, which facilitates impedance matching.

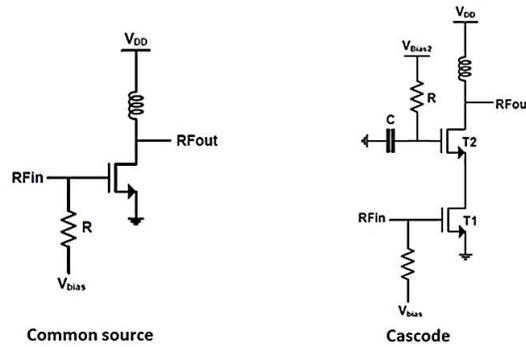


Figure 2-26. Common Source and Cascode Schematic

Table 2-3. Performance of CS vs Cascode

Type	Gain	Linearity	Bandwidth	NF	Output Power
CS	-	+	-	+	-
Cascode	+	-	+	-	+

A modified topology of cascade one is the stacked topology. It is presented in Figure 2-1, and allows a distribution of the polarization so that each transistor sees a portion of V_{DD} [50]. The supply voltage of the amplifier can be increased. Capabilities on transistors mounted in common gate allow to have an RF excursion on the gates, unlike a cascode topology that has an RF ground on the gate of its higher transistor by the great value of C_g . Thus, the RF excursion of the amplified signal is done in a more homogeneous way.

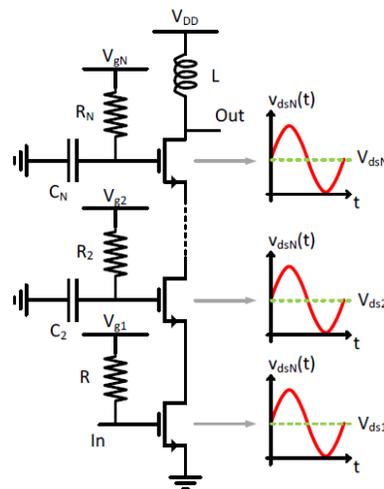


Figure 2-27. Stacked Topology Schematic

2.2.4.2 Differential Topology

The differential structure requires dividing and combining two channels out of phase by 180° with baluns (Balanced to Unbalanced). It allows to create a local virtual ground connection, reducing the parasitic inductive and resistive effect of the ground plane and improving the stability of the PA. In addition, this structure allows to combine the power of two cells of amplification out of phase of 180° at the expense of performance (which can decrease because of the intrinsic losses of the balun) and the surface of the PA. The differential amplifier topology duplicates the output power ideally. It is used with the neutralization technique; it minimizes the gate to source capacitance C_{gd} by presenting a capacitance in parallel shifted by 180° , then it improves the gain of the amplifier and the isolation in the reverse path of the transistor. At millimeter frequencies, the baluns can be implemented by integrated transformers (interleaved or stacked), that have three roles: impedance matching, power combiner/splitter, and 180° phase shift between the differential signals.

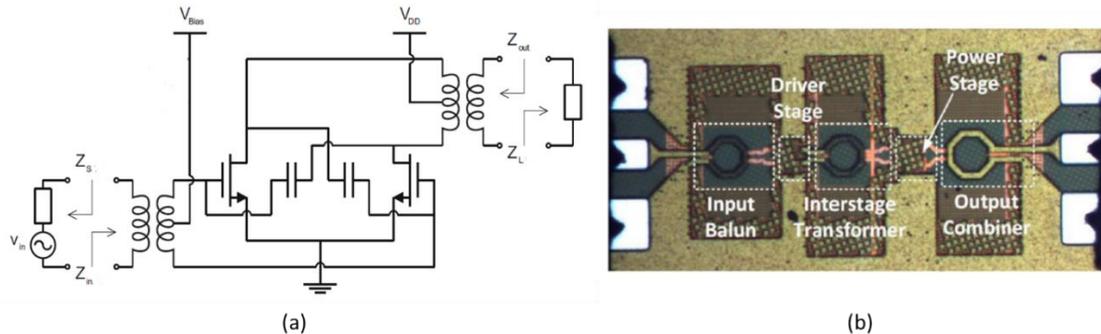


Figure 2-28. a) Differential topology schematic and b) implementation example [51]

2.2.4.3 Balanced Architecture

A circuit having a balanced structure also consists of two quadrature RF channels, but with a phase shift of 90° between the channels (Figure 2-29). This phase shift is achieved by the 3 dB couplers (hybrid couplers or Lange coupler), which requires a large surface area. It improves the stability, and is less sensitive to the impedance mismatch. The power is also doubled at the output after combining the two-standalone amplifiers. The drawbacks are the size of the couples, the sensitivity to the ground plane, and the losses in the coupler that degrades the overall performance. It is used in the design of PAs in mm wave band till the work of [52] that implement 3 dB 90° hybrid coupler in deep submicron CMOS 28 nm FD-SOI technology.

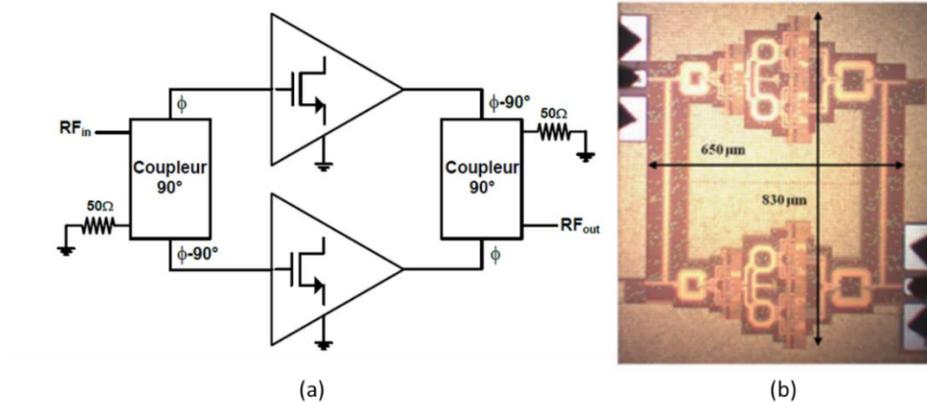


Figure 2-29. a) Balanced Architecture Schematic and b) Implementation example [52]

2.2.5 PA Classes

Several classes have been defined to characterize the operation of an amplifier power. They can be divided into two families: the sinusoidal classes (A, B, C and AB), and switched classes (D, E, and F).

2.2.5.1 Sinusoidal classes

The operating principle of sinusoidal class amplifiers is related to the polarization of the transistor. In CMOS technology, the V_{GS} gate voltage determines the current I_{DS} as shown in Figure 2-30.

- Class A

The bias current of a Class A transistor is located in the middle of the characteristic $I_{DS} = f(V_{GS})$: its amplitude is maximal and its conduction angle is 2π . This class of operation enjoys excellent linearity, but its theoretical efficiency is 50%.

$$\eta_{MAX_ClassA} = \frac{P_{out}}{P_{DC}} = \frac{\frac{1}{4} \cdot (V_{DD} - V_{th}) \cdot I_{max}}{\frac{1}{2} \cdot V_{DD} \cdot I_{max}} \approx 50\% \quad (2.30)$$

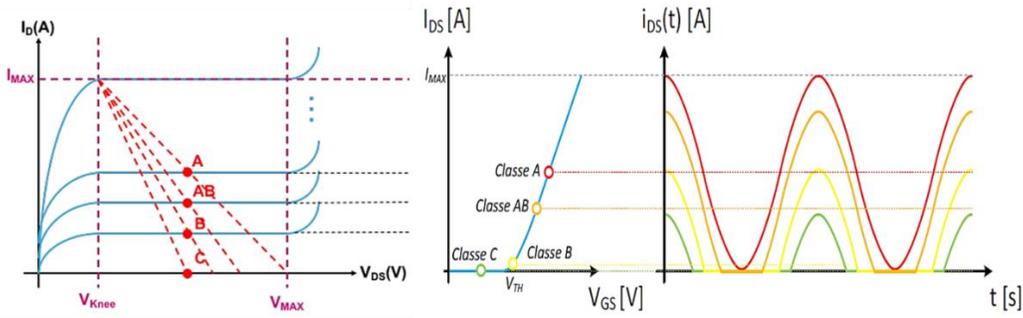


Figure 2-30. Drain Current characteristics w.r.t. Drain and Gate Voltages of Sinusoidal Classes

- Class B

In class B, the bias point is placed at the threshold voltage V_{TH} of the transistor. Thus, the conduction angle is almost halved. This lowering of the polarization point induces a theoretical maximum efficiency for this class of about 78.5%. However, this operation causes the appearance of harmonics, thus reducing the linearity.

$$\eta_{MAX_ClassB} = \frac{P_{out}}{P_{DC}} = \frac{\frac{1}{4} \cdot (V_{DD} - V_{th}) \cdot I_{max}}{\frac{\pi}{V_{DD} \cdot I_{max}}} \approx 78.5\% \quad (2.31)$$

- Class AB

As the name suggests, class AB is an intermediate class. Its angle of conduction is between π and 2π , which implies efficiency between 50% and 78.5%. This class of operation reflects the compromise between linearity and efficiency, which is why it is widely used at millimeter frequencies.

$$\eta_{MAX_ClassAB} = \frac{P_{out}}{P_{DC}} = \frac{1}{2} \cdot \frac{(V_{DD} - V_{th})}{V_{DD}} \cdot \frac{\theta - \sin(\theta)}{2 \sin\left(\frac{\theta}{2}\right) - \theta \cos\left(\frac{\theta}{2}\right)} \quad (2.32)$$

$$\approx 50\% < \eta_{ClassAB} < 78.5\%$$

- Class C

From class C, the conduction angle is less than π . In doing so, it remains the least linear sinusoidal class, with a rather weak output power, but its theoretical efficiency is between 78.5% and 100%.

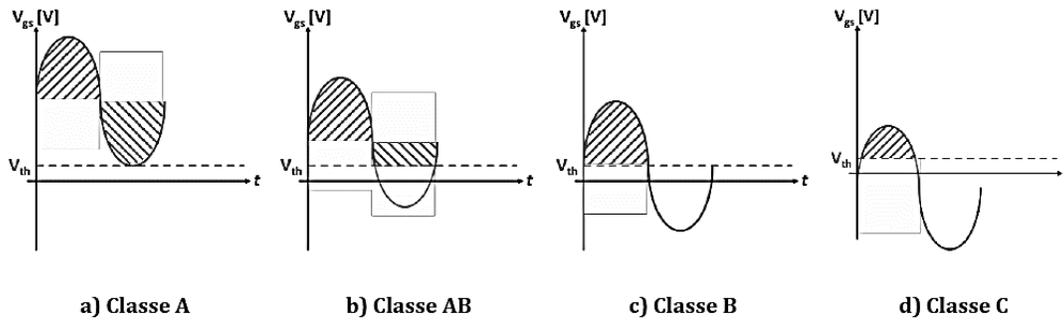


Figure 2-31. Gate Bias Voltages for Sinusoidal Classes

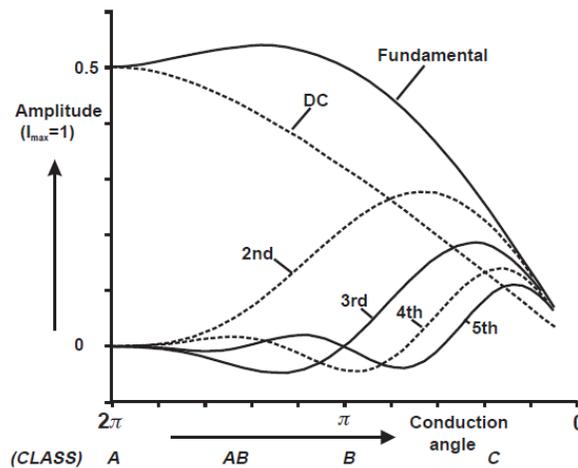


Figure 2-32. Current Harmonics according to the angle of conduction

Figure 2-32 shows the impact of the harmonics on the current I_{DS} according to the angle of conduction used: Class A does not suffer from any harmonic contribution. However, DC component is maximum, reflecting low efficiency. For class B, the level of the fundamental is the same as in class A, but less for a DC contribution. Even harmonics are nonetheless which has a direct impact on linearity. Class C as for it, makes all the components of the signal tend towards 0. We also find the duality of the class AB on this figure. The maximum current at the fundamental is reached for a conduction angle of $\frac{4\pi}{3}$.

2.2.5.2 Switched classes

The operating principle of amplifiers that use high efficiency classes is the reduction of the coexistence time current / voltage. The method applied to achieve is the use of harmonic frequencies (Figure 2-33) in order to model the shape of waveform in current or voltage.

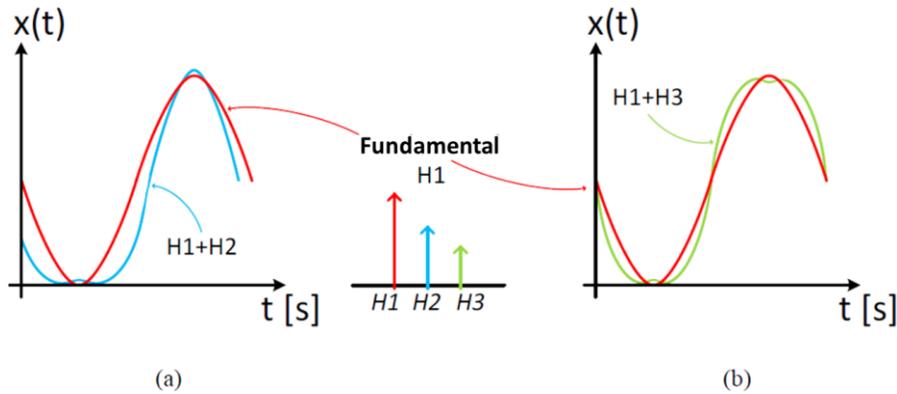


Figure 2-33. Impact of harmonics (a) 2 and (b) 3 on the waveform of a signal $X(t)$

Indeed, the use of harmonic components shapes in fundamental waveform in the time domain, reduce the coexistence time and thus optimize the performance. The addition of harmonic 2, or even harmonic harmonics gives the signal a form toward half-sine, while the addition of harmonic 3, or the odd harmonics give the signal a square shape.

- Class D

An amplifier in class D is formed by two transistors, which allow a conduction alternately. The input signal is square, and a tuned LC filter is used to pass a current in the load at the desired frequency, and eliminate the harmonics of higher orders. Since the voltage and the current do not overlap (Figure 2-34(a)), it is possible to achieve a theoretical efficiency of 100%. However, in reality, the losses of the components degrade the performance. In addition, the drain parasitic capacitance transistors affects the waveform of the voltage which, thus smoothed, reveals a non-zero coexistence time.

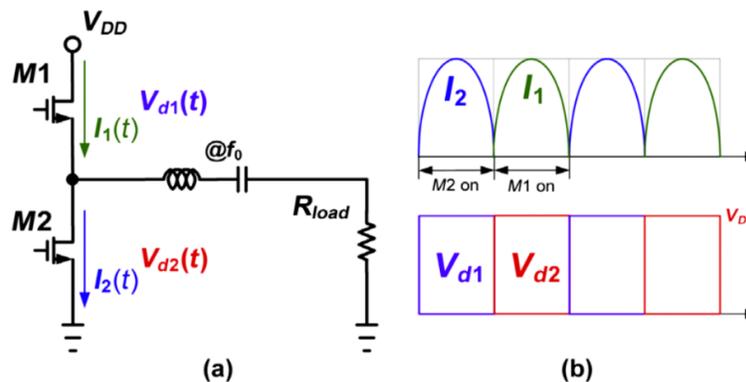


Figure 2-34. a) Circuit diagram of the class D amplifier. b) Voltage and current waveforms

- Class E

The class E amplifier is to use the transistor in switching mode. With a low resistance to the ON state and a very high impedance to the OFF state, the waveforms in current and voltage on the drain of the amplifier are opposition of phase. In the ideal case, the resistance mode is negligible and the power loss is then zero. Similarly, in the ideal case, if OFF mode impedance is very large, no current flows through the transistor, switching is so perfect, the transistor dissipates no power and theoretical performance is to 100%. The overlap of the waveforms between the voltage and drain current is reduced due to the switching time. The difference between the amplifier class D and class E amplifier lies in the fact that the impedance presented at the output of the transistor for the second and third harmonics is an open circuit for class E.

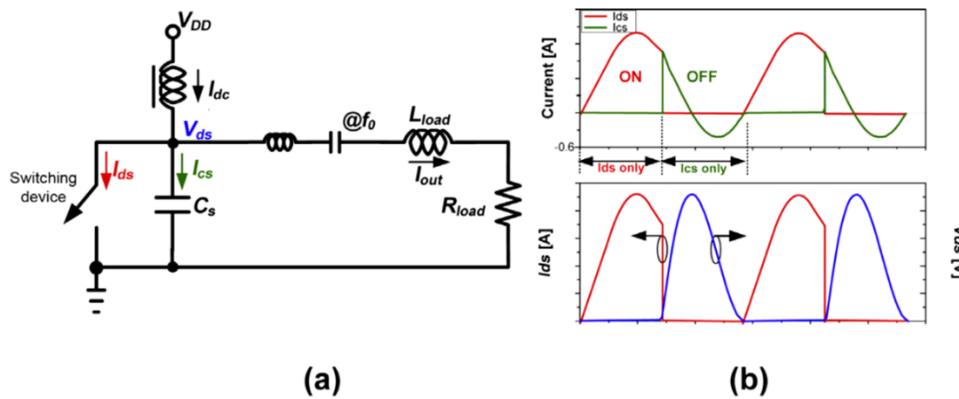


Figure 2-35. a) Circuit diagram of the class E amplifier. b) Voltage and current waveforms

- Class F

The principle of this class is to model the drain voltage of the transistor to make it square, and thus reduce the coexistence time (Figure 2-36). This change is possible, thanks to the output adaptation network, composed of resonant circuits in order to recover the odd harmonics and generate a square output voltage. The time of coexistence decreases with the increase of filtered harmonics, and the efficiency increases up to reach 100% in theory. However, the necessary filters introduce significant losses of insertion, which in practice prevents perfect efficiency.

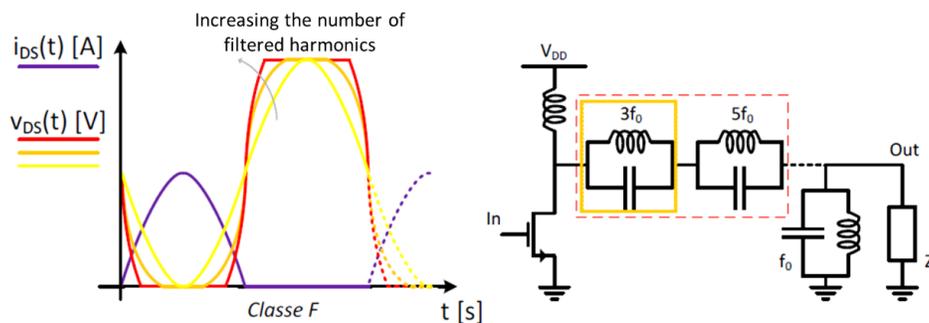


Figure 2-36. a) Voltage and current waveforms. b) Circuit diagram of the class F amplifier

2.2.6 Transistor Size

A width W of the transistor is composed of a number N_f of elementary transistors each having a gate finger width of W_f , as $W_{total} = W_f \cdot N_f$. This transistor may also be cut into N_c cells each containing a plurality of elementary transistors. Figure III-10 shows two examples of possible topologies.

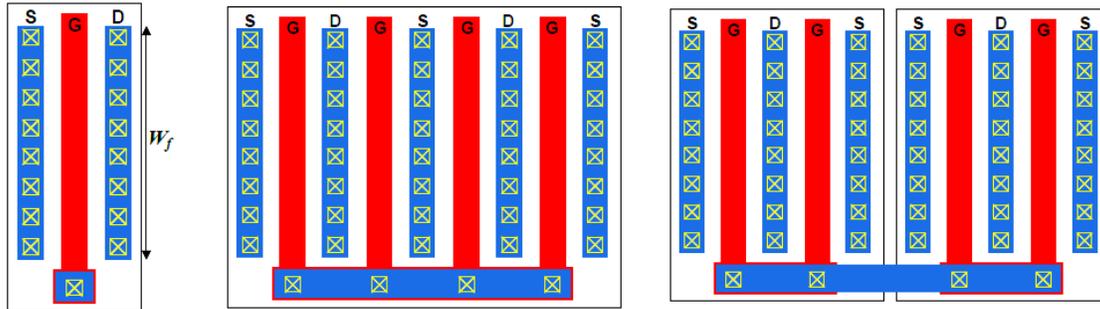


Figure 2-37. a) Elementary Transistor. b) Transistor of $N_f=4$ Fingers. c) Transistor of $N_f=2, N_c=2$

2.2.6.1 Width and number of gate finger

Width W_f finger is critical for millimeter applications. It is directly connected to the gate resistance responsible for the degradation F_{max} . Figure 2-38 shows a result, which have been published in [53] to select the appropriate gate width W_f for each technology node.

The parasitic capacitances and the complexity of modeling are increasing as the number of fingers N_f of the transistor increases. In contrast, a high number of fingers minimizes gate resistance. The impact of parasitic capacitances, including the drain-source capacity C_{ds} , leads to a maximum size of a transistor to avoid too reduce the output impedance. Empirically, it can be written [54] as:

$$W_{max}(\mu m) \approx \frac{10^4}{Frequency(GHz)} \quad (2.33)$$

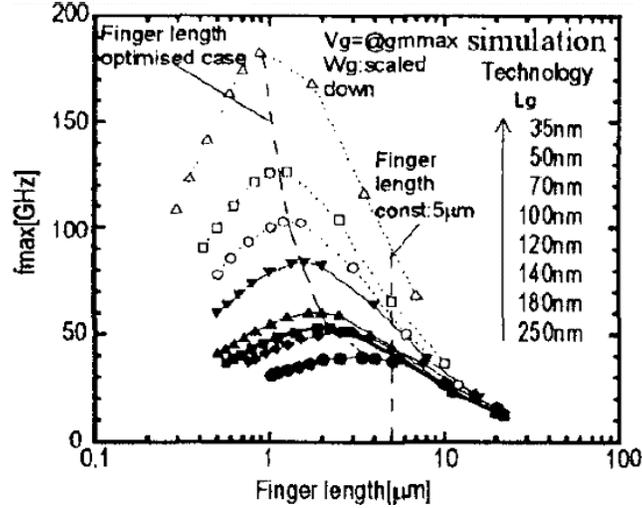


Figure 2-38. f_{max} according to the gate width W_f [53]

2.2.6.2 Transistor Parasitic Interconnects

The equations f_t and f_{max} below, shows that the transistor performance highly dependent on the layout. Indeed, the frequency f_t depend on C_{gd} and C_{gs} capacity while the frequency f_{max} depends on gate R_g resistance, source resistance R_s , C_{gs} , and C_{gd} capacitance.

$$f_t \approx \frac{g_m}{2 \cdot \pi \cdot (C_{gs} + C_{gd})} \quad (2.34)$$

And

$$f_{max} \approx \frac{f_t}{2 \cdot \sqrt{R_g \cdot \left(g_m \cdot \frac{C_{gd}}{C_{gs} + C_{gd}} \right) + (R_g + r_{ch} + R_s) \cdot g_{ds}}} \quad (2.35)$$

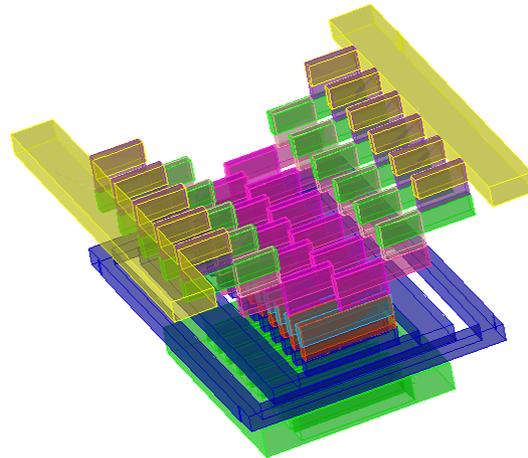


Figure 2-39. Staircase structure of drain and source connections

To reduce the parasitic capacitances, it is possible to have stepped paths to drains and sources, as shown in Figure 2-39. The gate resistance can be reduced by adding more fingers and more access. By taking two access [55] it improves the frequency f_{max} . An example of optimizing the layout of the proposed in Figure 2-40 with a transistor of 19 gate fingers, two access to the gate, and spiral connections to the drain and the source.

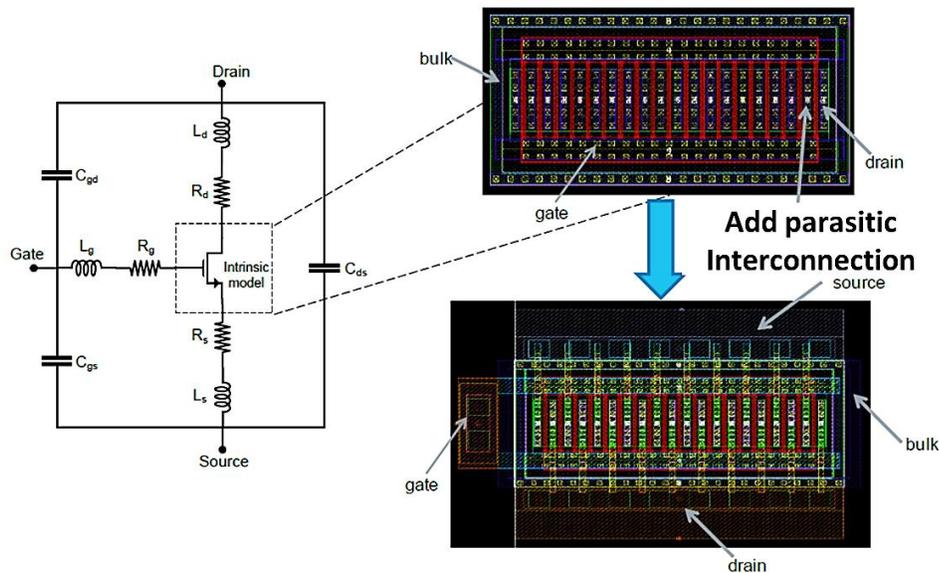


Figure 2-40. Layout Optimization

2.2.7 Class J Power Amplifier

2.2.7.1 Mode of Operation

Class J topology - presented by [56] - is a CS PA with a different output-matching network. The output-matching network is actually the main challenge for this mode of operation.

Transmission line network and pi-section network are two distinct methods capable of achieving Class-J PA. However, based on the fact that transmission lines occupy large area of the integrated circuit, pi-section network is the method chosen in this work as shown in Figure 2-41. The pi-section network presented in Figure 2-41 with suitable values of its components is capable of achieving a phase shift at the second harmonic voltage to be in-phase with the fundamental voltage and shorted the third harmonic voltage to the ground.

The Class J Drain-Source voltage equation is as follows [56]:

$$V_{DS} = V_B * (1 - \cos \theta) \tag{2.36}$$

Where V_B is the equation of class B/AB drain-source voltage waveform and it's given by:

$$V_B = V_{dc} + V_{peak}(-\sin\theta) \tag{2.37}$$

Assuming that $V_{peak} = V_{dc}$, to have Class-AB condition, then

$$V_{DS} = V_{dc}(1 - \sin\theta)(1 - \cos \theta) = V_{dc} (1 - \sin \theta - \cos\theta + 0.5 \sin(2\theta)) \tag{2.38}$$

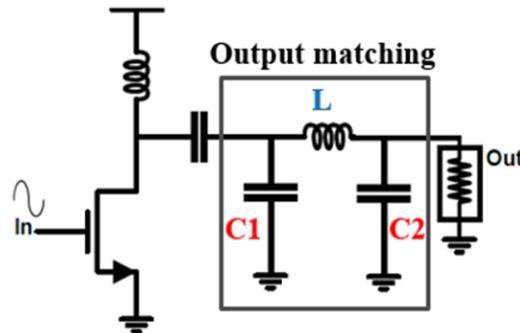


Figure 2-41. Pi- Section Network Operation

Equation (2.23) clearly explains how the transition from the voltage waveform of Class-B to that of Class-J occurred through a phase shift and harmonic boost as shown in Figure 2-42 [57] that increase the output power. Figure 2-43 [58] clarifies the waveforms of both drain-source voltage and currents corresponding to Class-J mode of operation. To achieve these waveforms, the load impedances at both fundamental and second harmonic frequencies are defined by [56] as the following:

$$Z(f_0) = R_{opt}. (1 + j) \tag{2.39}$$

And

$$Z(2f_0) = 0 - j \frac{3\pi}{8} R_{opt} \quad (2.40)$$

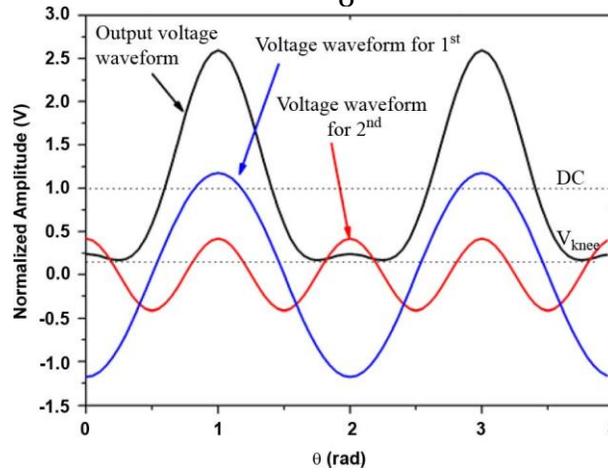


Figure 2-42. Class-J Mode [57]

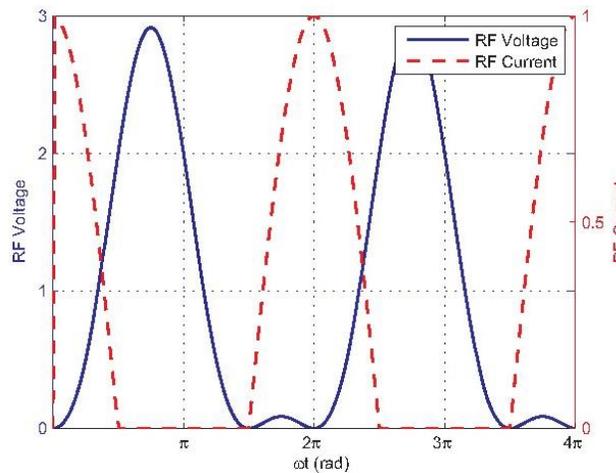


Figure 2-43. Class-J Drain-Source Voltage/Current Waveforms [58]

2.2.7.2 Class AB versus Class J

A study is done and published in [59] presents the design of 5G mm-wave PA using both Common Source Class-AB and Class-J topologies utilizing 28-nm UTBB FD-SOI technology at 28 GHz. Upon taking into consideration the parasitic extraction of the transistor, RF pads, and interconnection to ground, a comparison is made and the theoretical effectiveness of Class-J topology for single stage large signal amplification is simulated. Moreover, two distinct transistors - widths of 250 μm and 350 μm - are simulated where each has its own topology in order to study the impact of increasing the width on the performance of the PA.

Figure 2-44 illustrates the drain-source I-V curves of the Class-J PA at 28 GHz. It is clear that this work had achieved the expected Class-J waveforms as in Figure 2-42 and Figure 2-43; the second harmonic is phase shifted to make a boost for the fundamental frequency signal.

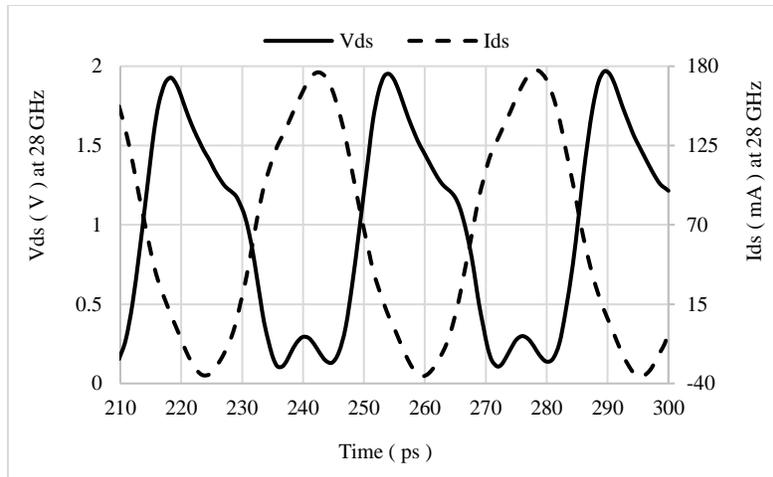


Figure 2-44. Drain-Source IV Curves of Class-J at 28 GHz

Figure 2-45 and Figure 2-46 describe the variation of PAE, P_{out} , and Power Gain as a function of the input power for both 250 μm and 350 μm transistor widths respectively. The Class-J mode of operation allows the increase of both power gain (approximately 1 dB at each width) and higher PAE of the PA (by 6% and 10% at $W=250\ \mu\text{m}$ and $W=350\ \mu\text{m}$ respectively) when compared to the classical Class-AB topology. The enhancement of the output power is due to the shaping of the class-J output waveform, and as the output power increase, the PAE will increase too. Furthermore, it is examined that increasing the width of the transistor has its negative drawbacks on the corresponding power gain because the parasitic increases as the width of the transistor increases.

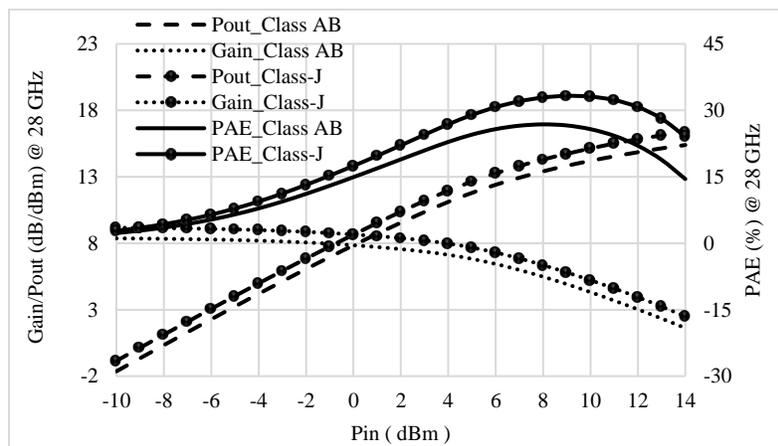


Figure 2-45. PAE, P_{out} , and Gain Comparison for $W=250\ \mu\text{m}$

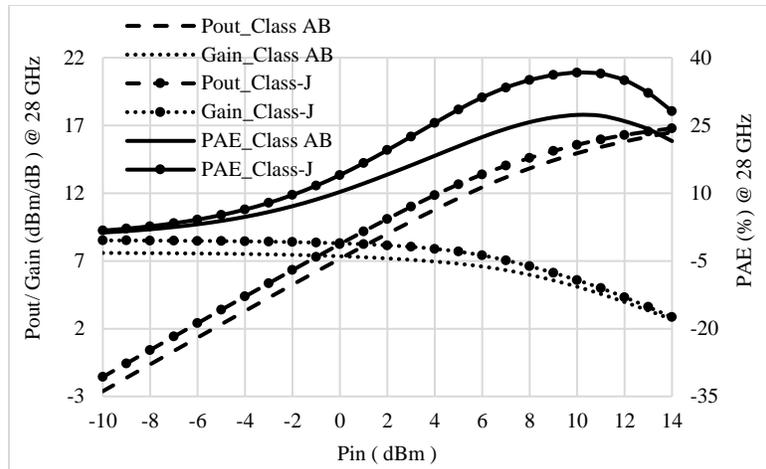


Figure 2-46. PAE, P_{out} , and Gain Comparison for $W= 350 \mu\text{m}$

The bandwidth of the designed mm-wave PA is referred to the -3dB values of the amplifier gain. Class J has theoretically wider bandwidth than that of Class AB. However, the quality factor QF of the inductor in the Class J output matching section plays a dominant role in the bandwidth variation. As the QF decreases the bandwidth increases, but it also degrades the output power, so that a compromise between both parameters is needed.

Table 2-4 represents the bandwidth of different circuits presented in this work. It is noted that increasing the width from $250 \mu\text{m}$ to $350 \mu\text{m}$ affects the bandwidth negatively. This was validated for both Class AB and Class J mode of operations. Moreover, it is noted that the bandwidth of Class AB is narrower than that of Class J when using a $250 \mu\text{m}$ transistor. However, when using $350 \mu\text{m}$ transistor, the Class J mode of operation suffers from a decreased bandwidth performance when compared to Class AB due to the increase of the parasitic effects of the transistor. In practice, the bandwidth of Class J can be increased by decreasing the quality factor of the inductor used in the output-matching network alongside with some regulations in the values of passive components used in the matching networks

Table 2-4. Bandwidth Comparison

Class	AB $250\mu\text{m}$	AB $350\mu\text{m}$	J 250μ	J 350μ
Bandwidth (GHz)	8	7.25	9	6

As a result, Class-J PA design and its analysis show an improvement in output power, power gain, PAE, and bandwidth over than that of Class-AB. This result matches the one mentioned in the theoretical approach.

2.2.8 Stability

When designing a circuit, the analysis of its stability will help preventing it from possible oscillations. In the worst case, these can lead to the destruction of the circuit. At first, the study is

done in a small signal, thanks to S parameters from which different factors are extracted. It is then possible to perform a high signal time analysis or nonlinear analysis, which consists in injecting pulses of high amplitude in some nodes of the circuit to check if it does not start in oscillation mode.

2.2.8.1 Small signal Stability Analysis

Two factors can be used to determine the stability of a two-port device. These factors are related to the values of the S-Parameters, which signify the dependency of stability on the input/output matching networks used in the design process. Since stability is frequency dependent, the stability of the mm-wave PA should be verified by simulating the stability factors listed below over a wide frequency range that varies from low band (DC) to at least $2f_0$; where f_0 is the fundamental frequency. Thus, unconditional stability of the system should be verified.

The Stability Factor, K_f , is derived from the s-parameters. “ $K_f > 1$ ” is a necessary (but not sufficient) condition for stability at a given frequency for a two-port device. It is defined by [60] as follow:

$$K_f = \frac{1 + |S_{11} \cdot S_{22} - S_{21} \cdot S_{12}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{11}| \cdot |S_{22}|} \quad (2.41)$$

Where

$$|S_{11} \cdot S_{22} - S_{21} \cdot S_{12}|^2 = \Delta \quad (2.42)$$

When $K_f > 1$, the circuit will not have an input or output reflection coefficient magnitude, which is greater than unity, no matter what passive matching, may be placed at its input or output [56] As K_f becomes less than 1, the two-port device is no longer unconditionally stable.

The table below summarizes the following stability states the values that can take K_f and Δ

Table 2-5. Conditions of Stability Factors

$ K_f = 1$	$K_f = \pm 1$		Unstable
$ K_f > 1$	$K_f > 1$	$ \Delta < 1$	Unconditionally stable
		$ \Delta > 1$	Conditionally stable
	$K_f < -1$		unstable
$ K_f < 1$			Conditionally stable

In addition to $K_f > 1$ and $|\Delta| < 1$, the other stability factor, B_1 , must be greater than zero to insure unconditional stability for the two-port network. B_1 is defined by [56] as follows:

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |S_{11} \cdot S_{22} - S_{21} \cdot S_{12}|^2 \quad (2.43)$$

If the stability is conditionally one, then circle of source and load impedance can be drawn in the smith chart to specify the impedance region of stable and unstable impedance for source and load separately.

For source stability circle:

$$R_S = \left| \frac{S_{21} \cdot S_{12}}{|S_{11}|^2 - |\Delta|^2} \right| \quad (2.44)$$

And

$$C_S = \frac{(S_{11} - S_{22}^* \cdot \Delta)^*}{|S_{11}|^2 - |\Delta|^2} \quad (2.45)$$

For Load stability circle:

$$R_L = \left| \frac{S_{21} \cdot S_{12}}{|S_{22}|^2 - |\Delta|^2} \right| \quad (2.46)$$

And

$$C_S = \frac{(S_{22} - S_{11}^* \cdot \Delta)^*}{|S_{22}|^2 - |\Delta|^2} \quad (2.47)$$

Where R_S and R_L are the circle radius, while C_S and C_L are the center of source, load circle with respect to Γ_S and Γ_L plans respectively as shown in Figure 2-47.

The stability circles represent the boundary of stable/unstable regions. The result is also depend on S_{11} and S_{22} . If $S_{11} > 1$ or $S_{22} > 1$, the stability region is inside the circle, while if $S_{11} < 1$ or $S_{22} < 1$, the stability region is outside the circle.

Another parameter is introduced by Edwards and Sinski [61], which is μ and μ' . They perform a geometric measurement of the distance between the center of the Smith chart and the nearest point of load or source of stability circle. Thus, if this distance is greater than 1, then the component is unconditionally stable, where

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \cdot \Delta| + |S_{21} \cdot S_{12}|} \quad (2.48)$$

And

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^* \cdot \Delta| + |S_{21} \cdot S_{12}|} \quad (2.49)$$

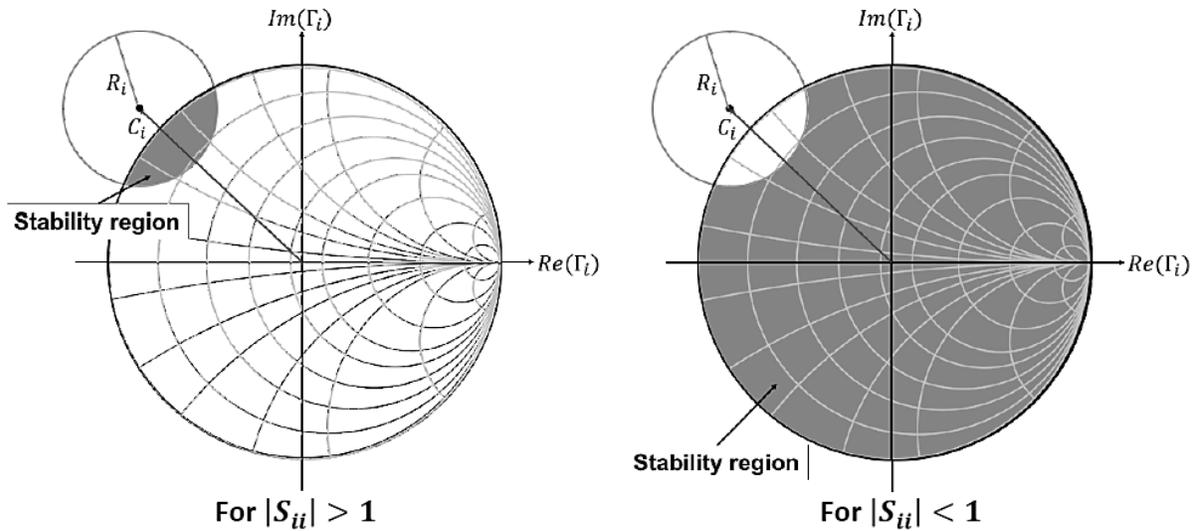


Figure 2-47. Stability Circle

2.2.8.2 Large Signal Stability Analysis

Beside stability factors simulations, an additional technique is used to test the stability of the designed circuits. The technique, simply, consists of injecting positive/negative pulses at different node of the circuit (input, output, V_{DD} , GND...) and then analyzing the transient time response of the output voltage to identify any un-intended oscillations. The output voltage should tend to zero at the steady state to have a stable circuit. Otherwise, oscillations will be observed.

2.2.8.3 Stabilization technique

The main cause of instability is the miller capacitance C_{gd} that makes a negative feedback loop from the drain to the gate by 180° phase shift, and degrades the isolation and gain especially in the common source topology. For the common source amplifier, the parameter y_{12} is the reverse transfer admittance of the port. It represents the isolation between the input and the output and strongly depends on the value of C_{gd} , which makes a limitation for the common source amplifier.

$$y_{12} = -j\omega \cdot C_{gd} \quad (2.50)$$

In addition, the stability factor K_f and the maximum stable gain MSG can be expressed in terms of Y-parameters to study the effect of C_{gd} on the stability. Where

$$K = \frac{2 \cdot R\{y_{11}\} \cdot R\{y_{22}\} - R\{y_{12} \cdot y_{21}\}}{|y_{12} \cdot y_{21}|} = \frac{2 \cdot g_g \cdot g_{ds} + \omega^2 C_{gd}^2}{\omega \cdot C_{gd} \cdot \sqrt{\omega^2 C_{gd}^2 + g_m^2}} \quad (2.51)$$

And

$$MSG = \frac{|y_{21}|}{|y_{12}|} = \frac{|g_m - j\omega \cdot C_{gd}|}{|j\omega \cdot C_{gd}|} \quad (2.52)$$

C_{gd} is also a main parameter in f_t and f_{max} as stated before in equation 2.19 and 2.20. In mm-wave band, the sensitivity of the miller capacitance is increased creating a negative resistance and leading to oscillation problem.

If the internal resistance or losses introduced by the matching networks and by the interconnection of the transistor layout are not sufficient to stabilize a circuit, several techniques are possible. Conventional stabilization techniques are shown below as inductive source degeneration, RC shunt feedback, and neutralization.

- **Inductive source degeneration:**

The inductive degeneration (Figure 2-48) improves stability in the useful frequency band at the expense of the amplifier gain. It creates a resistive term in the input impedance of MOS transistor. It is more used in the LNA circuit. The cascode topology has less stability problems since the inductive degeneration is used for input matching. In addition, the Miller effects is reduced on both transistors in common gate and a common source; the latter is being loaded by an impedance close to $\frac{1}{g_m}$ with a voltage gain of about -1.

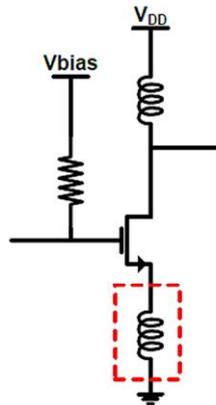


Figure 2-48. Inductive source degeneration CS

- **RC Shunt Feedback**

It consists of a capacitor with series resistance as shown in Figure 2-49. The role of the capacitor is to isolate the DC bias of the drain from that of the gate, while it should be large in order to make very low impedance or ideally short circuit for the RF signal at the frequency of the interest. The value of the resistor should be taken carefully; that increase the stability and save the amplifier isolation. It reduces the gain at low frequencies, while keeping a good gain with a minimum of insertion loss at the desired frequencies.

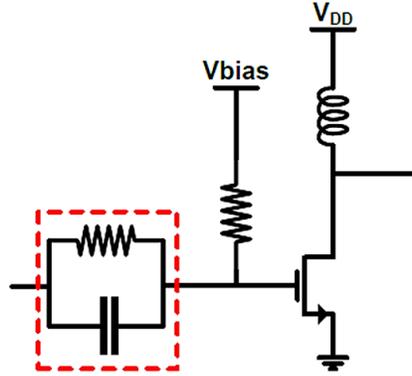


Figure 2-49. RC Shunt Feedback CS

- **Neutralization Capacitance**

The goal here is to minimize the C_{gd} . The neutralization capacitors introduce an equivalent capacitance $-C_n$ (presenting a capacity in parallel shifted by 180°) that compensates for the effect of C_{gd} of the transistor, thereby, the gain is improved [62] [63], and the isolation is improved by making the imaginary part of y_{12} equal to zero (when $C_n = C_{gd}$). Then

$$y_{12} = -j\omega(C_{gd} - C_n) \quad (2.53)$$

With

$$K = \frac{2 \cdot R\{y_{11}\} \cdot R\{y_{22}\} - R\{y_{12} \cdot y_{21}\}}{|y_{12} \cdot y_{21}|} = \frac{2 \cdot g_g \cdot g_{ds} + \omega^2(C_{gd} - C_n)^2}{\omega \cdot (C_{gd} - C_n) \cdot \sqrt{\omega^2(C_{gd} - C_n)^2 + g_m^2}} \quad (2.54)$$

And

$$MSG = \frac{|y_{21}|}{|y_{12}|} = \frac{|g_m - j\omega \cdot (C_{gd} - C_n)|}{|j\omega \cdot (C_{gd} - C_n)|} \quad (2.55)$$

The disadvantage of this technique is the narrow bandwidth. The technique of neutralization with abilities is only possible with a differential circuit.

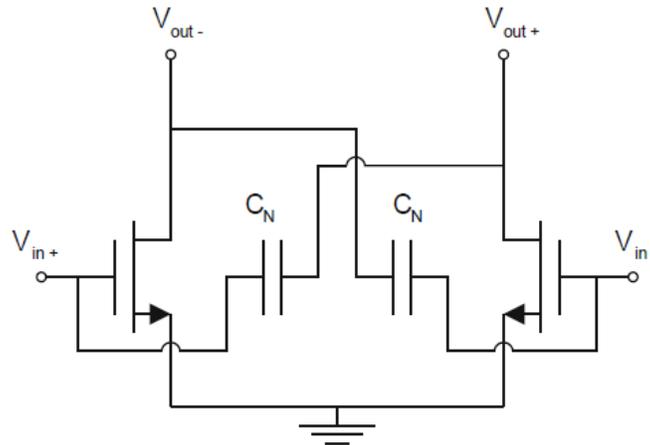


Figure 2-50. Neutralization capacitors in Differential topology

By plotting the K_f and the maximum gain in Figure 2-51, it can deduced about the value of the adequate capacitor.

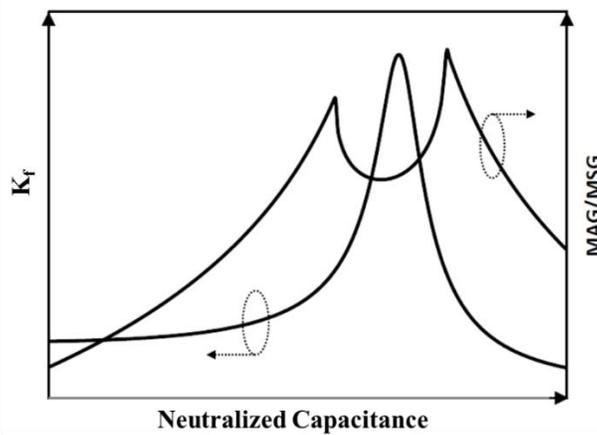


Figure 2-51. K_f and MAG/MSG w.r.t. C_n

- **Modified technique**

A study is done and prepared to introduce as a patent about a new technique, which is added to the common source amplifiers to enhance its behavior and fix some of its flaws: the input/output achieve higher isolation, higher stability, and higher gain than the conventional common source. A theoretical part is explained, and the implementation part consist a simulation of a common source power amplifier circuit using the 28nm UTBB FD-SOI technology at the 5G candidate frequency of 28 GHz compared with a conventional and RC shunt feedback common source power amplifier circuit provided under the same conditions.

The modified CS (used with the new technique) shows improvements on several parameters. According to the reverse isolation, the S_{12} increased from -17dB in conventional and shunt feedback CS to -40 dB in Modified CS as shown in Figure 2-52.

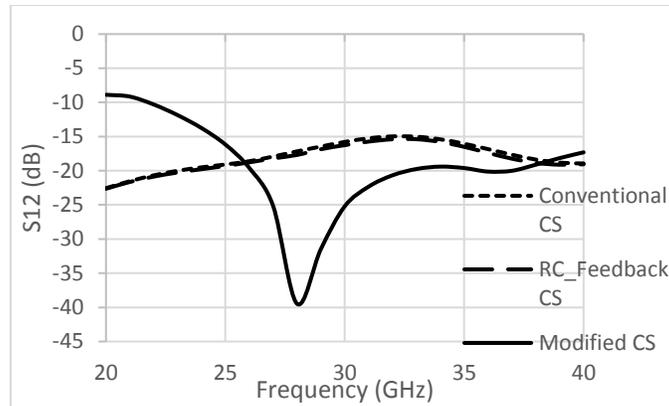


Figure 2-52. Reverse Isolation S_{12} Comparison

According to the stability, the K-factor at the desired frequency (28GHz) is changed from 2.4 in conventional CS to 3.2 in shunt feedback CS to 32 in modified CS as shown in Figure 2-53. The conventional circuit has a stability factor of 2 under the action of source degeneration which comes from the parasitic inductance of the interconnection between the source node and the ground plane.

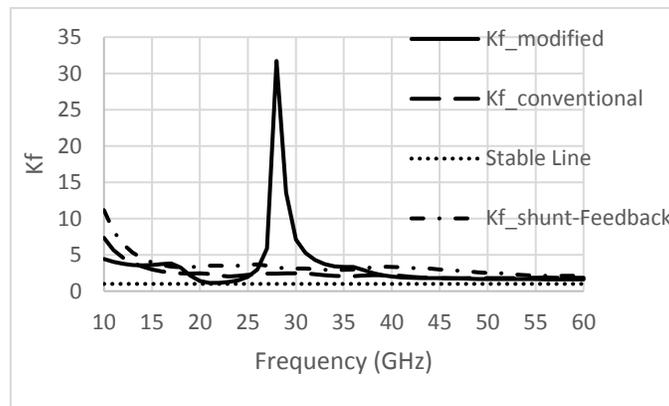


Figure 2-53. K_f of Conventional vs Shunt Feedback vs Modified CS

At 28 GHz, the output power and the power added efficiency PAE are shown in Figure 2-54 and Figure 2-55 respectively. The linear gain in the modified CS is enhanced with 1.7dB higher than that of the conventional CS and around 2.5dB higher than shunt feedback CS. The PAE in the linear region is also enhanced by 2.8% from conventional CS and around 4.2% than shunt feedback CS. The numerical values are stated in Table 2-6.

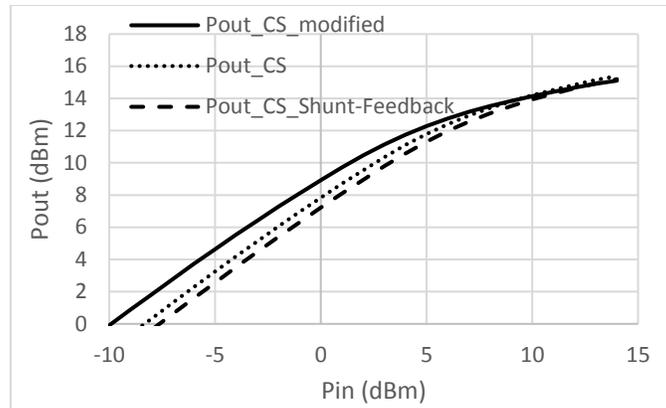


Figure 2-54. Pout of Different CS Techniques

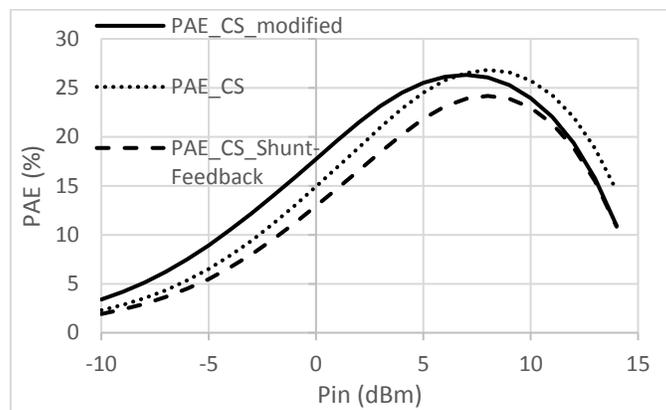


Figure 2-55. PAE of Different CS Techniques

Table 2-6. Power Performance and PAE Comparison

	Linear gain dB	ICP1 dBm	OCP1 dBm	PAE _{sat} %
Conventional CS	8.3	3.5	10.6	26.8
Modified CS	10	1.3	10.2	26.32
Shunt Feedback CS	7.5	4	10.58	24.1

2.2.9 Optimum Load Impedance

The power delivered at the output of an PA depends on the impedance presented to it. If we think in the first place to adapt to the conjugate of the output impedance to maximize the gain, another impedance $Z_{opt} = R_{opt} + jX_{opt}$ may be more relevant to allow PA to provide the maximum power to the load. This is due to non-linearity behavior of the PA in large signal in addition to the limitation of the supply voltage [56]. To understand the idea of avoiding conjugate

matching of the transistor in PA according to the supply limitation, it's better to take an example. A transistor that is a current generator, can supply maximum current of 1A, and has an output impedance of 100Ω (purely resistive to simplify the calculation), then the conjugate matching will be a load of 100Ω . There is a trap that the voltage across the terminal would be 50V, which is higher than the capability of the transistor due to the physical limitation. So that, the transistor will not be in its highest efficiency with the conjugate matching as shown in Figure 2-56.

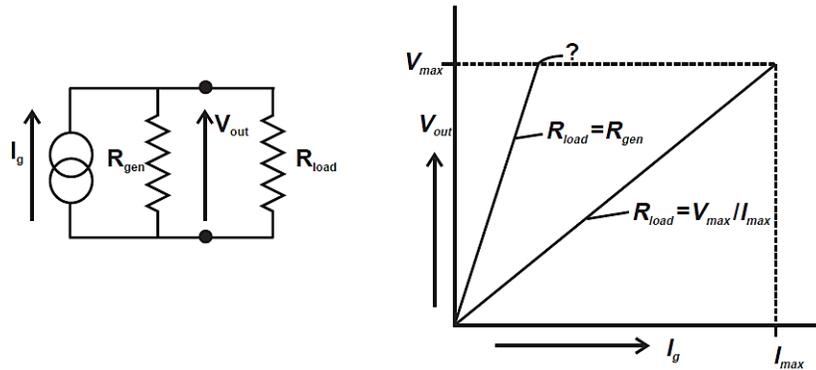


Figure 2-56. Conjugate match and load line match [56]

In order to have the highest power of the transistor (current generator), an R_{opt} is refer to the load line that have maximum current and voltage swing where

$$R_{opt} = \frac{V_{max}}{I_{max}} \quad (2.56)$$

Taking into consideration the generator resistance, then the equation below should be solved.

$$\frac{R_{gen} \cdot R_{opt}}{R_{gen} + R_{opt}} = \frac{V_{max}}{I_{max}} \quad (2.57)$$

2.2.9.1 Graphical method

Figure 2-57 represents the load line of the power amplifier according to whether the load is purely resistive (a), or if it is both resistive and inductive (b). For resistive load, the line is straight, and the equation of R_{opt} is

$$R_{opt} = \frac{2(V_{DD} - V_{knee})}{I_{max}} = \frac{(V_{DD} - V_{knee})^2}{2P_{out}} \quad (2.58)$$

Where

$$P_{DC} = V_{DD} \frac{I_{max}}{2} \quad (2.59)$$

And

$$P_{out} = \frac{I_{max}(V_{DD} - V_{knee})}{4} \quad (2.60)$$

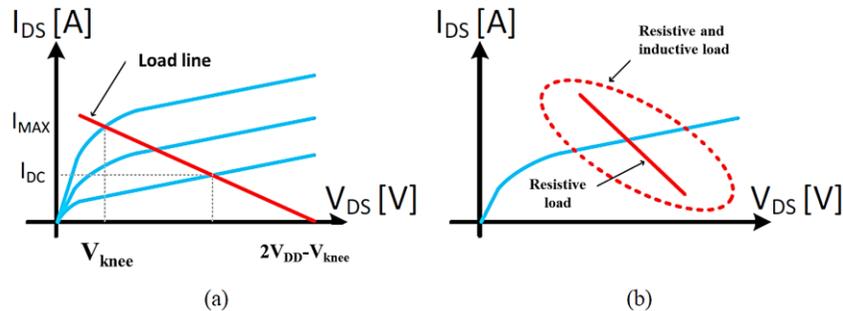


Figure 2-57. (a) Resistive load line and (b) Both resistive and inductive

It can be seen that resistive and inductive load line takes the form of an ellipse, because a significant phase shift between the voltages and drain currents. This has the effect of increasing the excursion of the voltage V_{DS} and the current I_{DS} . The output power is improved greatly. However, determining the inductive part X_{opt} of the optimal impedance Z_{opt} requires a Load-Pull analysis.

2.2.9.2 Load-Pull Analysis

The determination of the optimal complex load impedance Z_{opt} is determined by a Load-Pull analysis, in simulation or experimentally. This analysis is not exclusive to optimizing the output power, but can also be used to optimize the efficiency (PAE) of an amplifier, or its noise, and optimum source impedance. Optimal impedance, as well as constant P_{out} contours of different values, are usually plotted on a Smith chart (Figure 2-58). Note that it is possible on the same principle, to optimize impedances of different harmonics in order to design a nonlinear amplifier. However, the Load-Pull provides no information on the behavior of the phase and the voltage and current dynamics of the transistor, or the losses generated by the matching networks

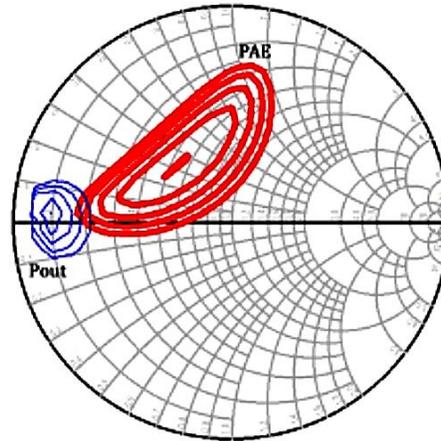


Figure 2-58. Pout and PAE Contours of Load-Pull Analysis

2.2.10 State of Arts

No such PA has a purpose to generate harmonic signal such that it will be the final output, the only works are the harmonic feedback oscillators. Otherwise, such works in [64] and [65] are using the amplifier as harmonic injection power amplifier. The structure is to have to parallel power amplifiers, where the main amplifier generates fundamental power F_0 , while the second amplifier (auxiliary), who's injected with second harmonic using a frequency doubler at its input, has an output connected to the main amplifier. The main goal is to form a shape of the voltage and current waveforms, which is appropriate and necessary to achieve high output power and high efficiency at the fundamental power. The schematic views are shown in Figure 2-59. The frequency of operation is below 2 GHz.

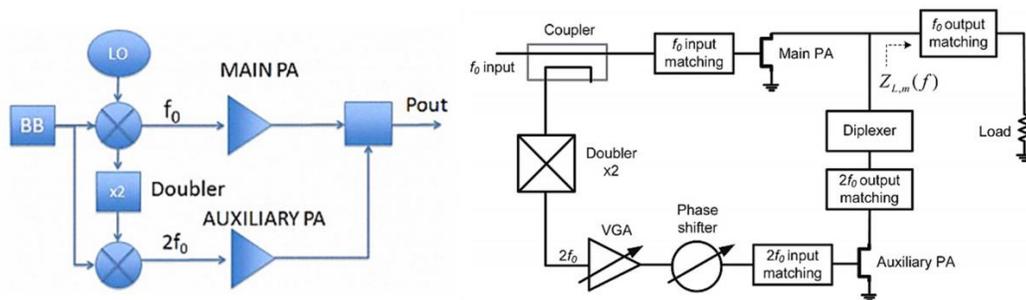


Figure 2-59. Harmonic Injection PA Structure in [64] and [65]

- The PA [66] described in Figure 2-60 uses two differential structure in single stage class AB: common source and cascode. Both worked in shorting the second harmonic to ground in order to maximize the linearity. It is implemented in 28nm CMOS technology Samsung System LSI. However, to get more gain and output power of the PA, a cascode is preferred more than the common source in the differential architecture. In addition, the cascode allows to distribute the power supply on the two transistors, which allows to increase the supply voltage to 2.2V instead of 1.1V, thus increasing the output power.

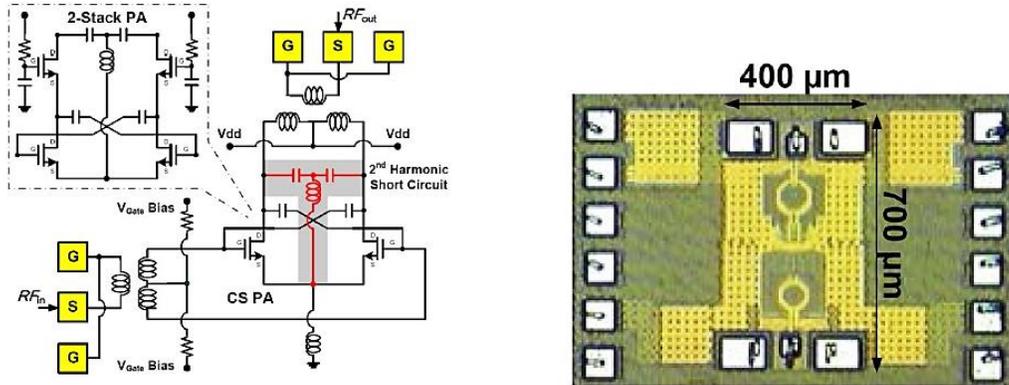


Figure 2-60. The schematic view and the photograph of PA [66]

The PA based on differential cascodes, delivers at 28 GHz a saturation power of 19.8dBm, compression point of 18.6dBm, maximum PAE of 43.3%, and a power gain of 13.6dB as shown in Figure 2-61. While the PA based on differential common source, delivers at 28 GHz a saturation power of 14.8dBm, maximum PAE of 36.5%, and a power gain of 10dB as shown in Figure 2-61. The single stage achieves good linearity and PAE results. It also avoids the losses of multistage passive components, but it cannot achieves high gain.

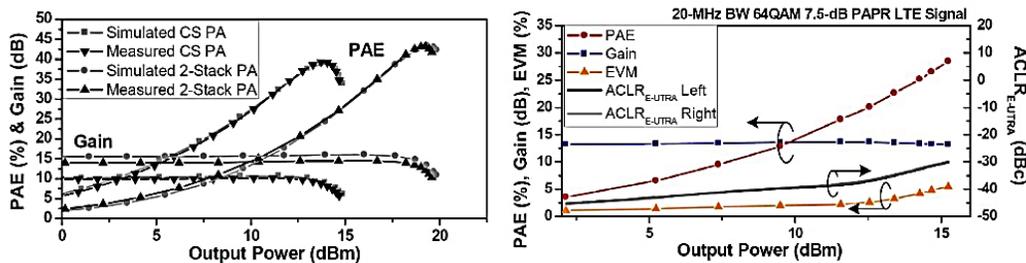


Figure 2-61. PA Performances [66]

- The PA [67] presented in Figure 2-62 consists of double stage differential amplifier mounted in a class AB common source. It is implemented in TSMC 28nm bulk CMOS technology. The input and the output of the PA consist of two baluns that realize the conversion of common mode to differential mode (and vice versa) as well as the impedance matching. The PA based on differential amplifiers, delivers at 30 GHz a saturation power of 14dBm, 1dB compression point of 13.2dBm, maximum PAE of 35.5%, and a power gain of 15.7dB as shown in Figure 2-63. The high PAE achieved even it uses more than one stage is due to the choice of one amplification path, which is better than power combining cells. The single amplification path leads to easier output match with limited losses. However, the power combining cells leads to higher output power.

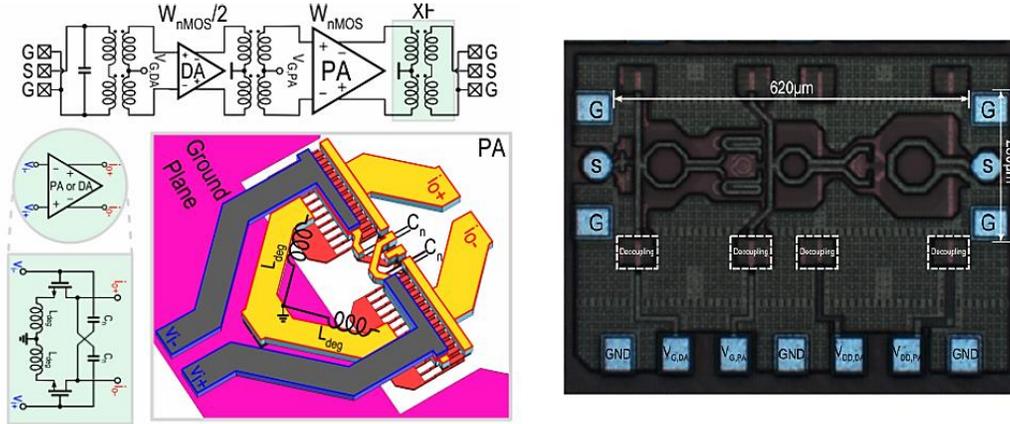


Figure 2-62. The schematic view and the photograph of PA [67]

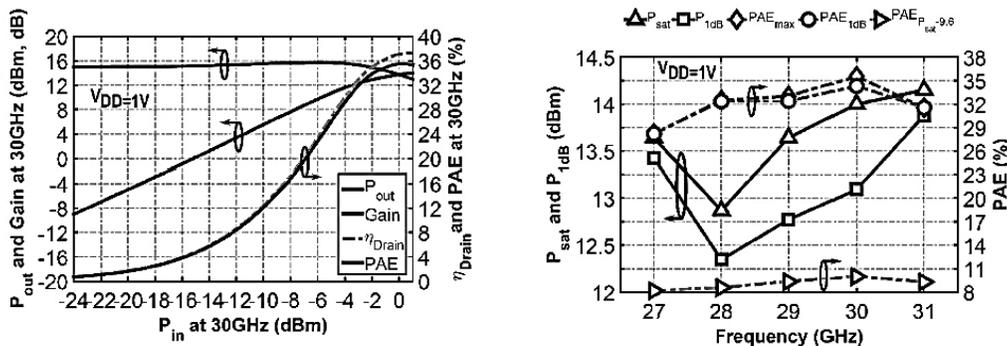


Figure 2-63. PA Performance [67]

- The PA [54] detailed in Figure 2-64 is composed of three stages of amplification. The power of the input signal is first divided into two tracks using a TFR4 transformer, which allows both the conversion of common mode to differential mode, and the input matching. Then in each of the two channels, the differential signal is amplified once, then a second time before it is divided again into two tracks through the transformer TRF2. The four obtained differential signals are then amplified before being recombined at the output of the PAs through the output power combiner TRF1 who, as the entry TRF4 balun, allows conversion of the differential mode to common mode as well as output impedance matching.

The PA had been implemented in 28nm CMOS FDSOI of STMicroelectronics technology. The PA is reconfigurable and can operate in two modes: high gain mode or high linearity mode, depending on the Body Bias feature of the FD-SOI transistor.

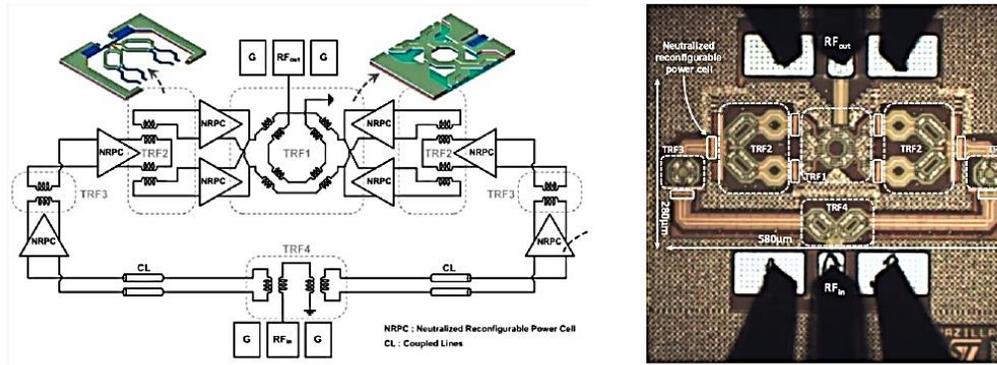


Figure 2-64. The schematic view and the photograph of PA [54]

The PA in the high gain mode delivers at 60GHz a saturation power of 18.9dBm, compression point of 15dBm, maximum PAE of 17.7%, and a power gain of 35dB as shown in Figure 2-65. It consumes 331mW. The PA in the high linear mode delivers at 60 GHz a saturation power of 18.9dBm, compression point of 18.2dBm, maximum PAE of 21%, and a power gain of 15.4dB. In this mode, the linearity is maximized at the expense of the small signal gain. It consumes 74mW.

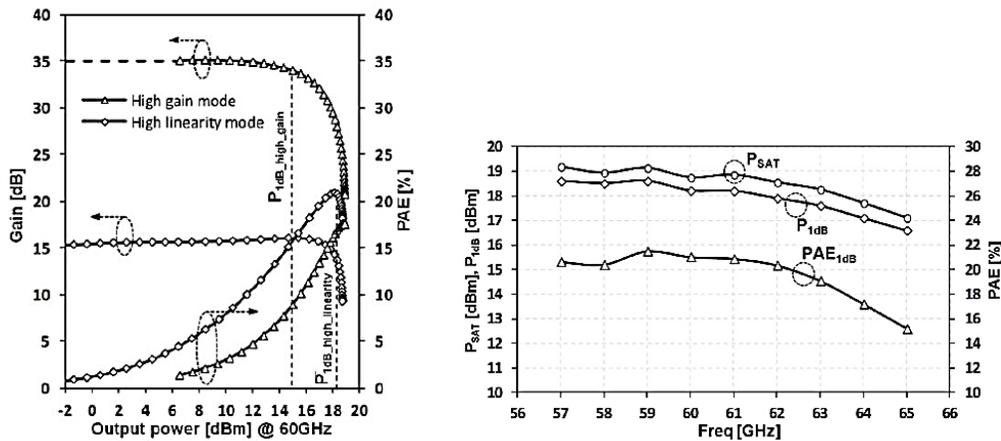


Figure 2-65. PA Performance [54]

It can also operate in a mode "reliability" by lowering the supply voltage, which allows limiting the stress on the power transistors and thus extend the life of the PA. Of course, by decreasing supply voltages, the RF performance degrades slightly, but they still allow the PA to have acceptable operation with a power of saturation and compression of 16.9dBm and 16.2dBm respectively. The maximum PAE reached 21% in this mode. The power consumption is lowered to 58mW.

The use of the body biasing technique offers a very good linearity. In addition, the use of an output transformer to combine four differential cells allows to obtain a higher output power. Note that

special attention must be given to the output transformer, because it realizes the differential mode conversion to a common mode, the impedance matching, and the power combination.

- The PA [52] presented in Figure 2-66 consist of both balanced and differential architectures at 28GHz for beamforming phased-array applications implemented in 28nm FD-SOI technology. The quadrature hybrid coupler has a novel design, which can be integrated in in CMOS technology with small size with respect to other couplers as Lange coupler, quadrature coupler...

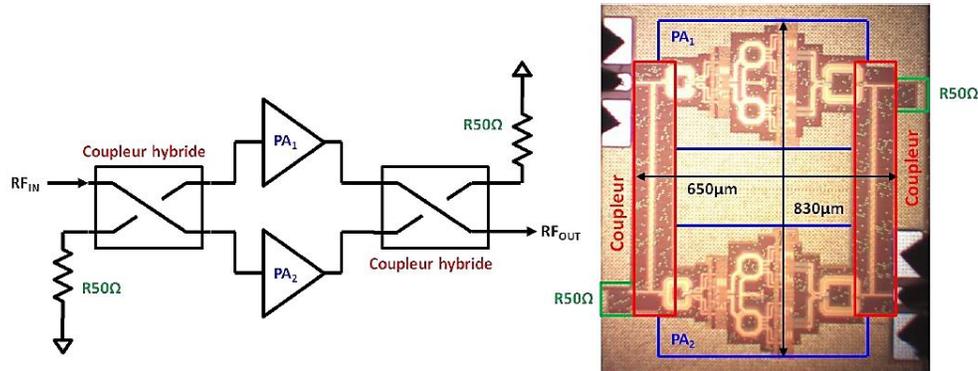


Figure 2-66. The schematic view and the photograph of PA [52]

It has two amplification path, each one is a differential path of three stages: a driver with no re-configurability, and a re-configurability power stage with push pull configuration aims to improve the AM-AM and AM-PM non-linearity's effects as shown in Figure 2-67. The push pull gives the opportunity to use 2V voltage supply instead of 1V, because the voltage is divided at both transistor.

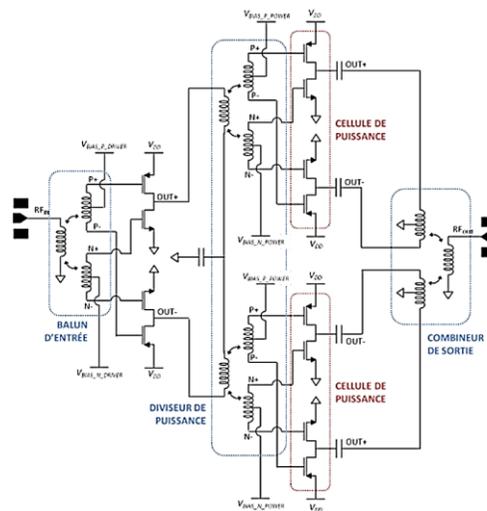


Figure 2-67. Schematic view of individual PA [52]

It works in two modes: high linear mode and high gain mode by controlling the body bias voltage. In high linear mode, the PA delivers a saturation power of 18.7dBm, 1dB compression point of 15.3dBm, maximum PAE of 12.4%, and a power gain of 17.2dB as shown

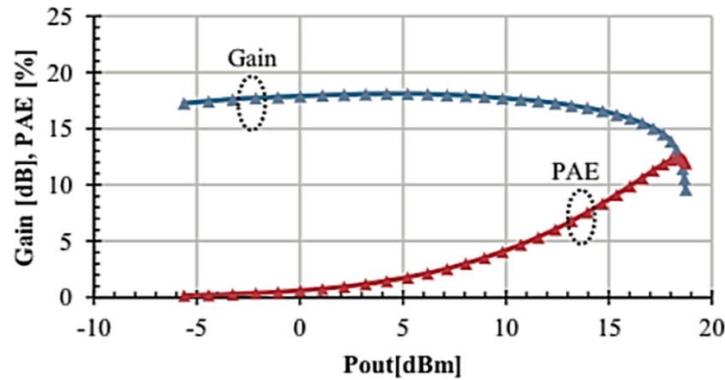


Figure 2-68. PA Performance [52]

The 90° hybrid coupler has the benefit of matching enhancement against the antenna impedance variation due to its characteristics. The large number of passive blocks as power combiner, matching transformers, couplers, and the multi path of amplification decrease the PAE to 12.4%.

- The PA [68] presented in Figure 2-69 consist of both balanced and differential architectures at 31GHz for 5G applications implemented in 28nm FD-SOI technology. It uses the same hybrid coupler as [52]. The driver consist of class A common source differential amplifier, and the power stage is reconfigurable cascade differential amplifier of variable gain controlled by the body bias, it has a range of 10dB.

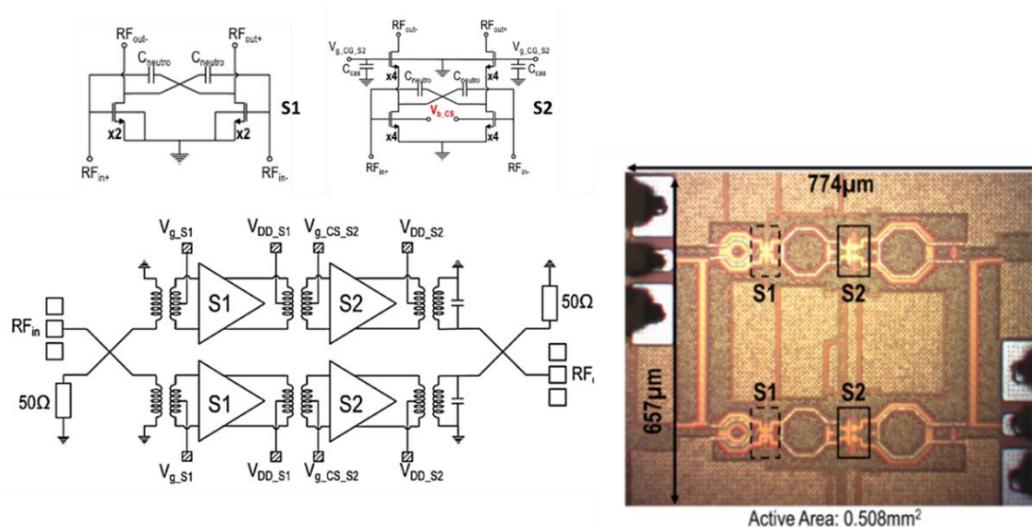


Figure 2-69. Schematic view of individual PA [68]

It has two modes, high linear mode and high gain mode as shown in Figure 2-70. In high linear mode, the PA delivers a saturation power of 17.3dBm, 1dB compression point of 15.3dBm, maximum PAE of 24.7%, and a power gain of 21.9dB. In high gain mode, the PA delivers a saturation power of 17.9dBm, 1dB compression point of 11.6dBm, maximum PAE of 25.5%, and a power gain of 32.6dB.

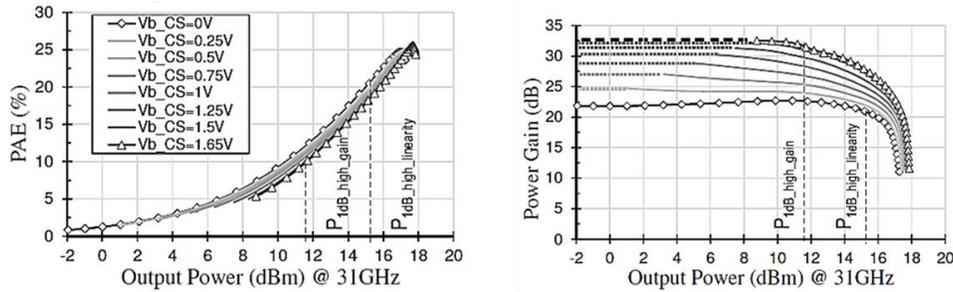


Figure 2-70. PA Performance [68]

It is better to mention a case outside the bulk an FD-SOI CMOS field, especially in 3D FinFET technology to ensure the results obtained in the RF and mm-wave application according to section 2.1. A PA is designed in 14-nm 3D FinFET from Intel at the E-band phased array application [69] as shown in Figure 2-71. It composed of three differential common source stages. A class AB is chosen to achieve high efficiency. In addition, an enhancement is done for the layout to decrease the layout parasitic.

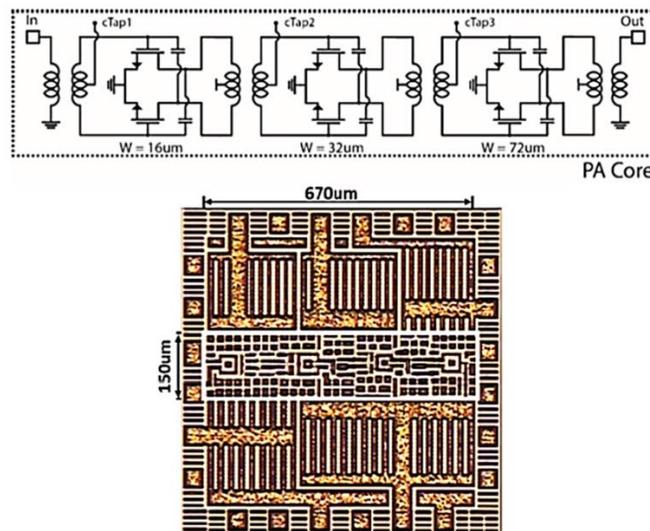


Figure 2-71. The schematic view and the photograph of PA [69]

The PA based on three stages of differential amplifiers, delivers at 71GHz a saturation power of 7.4dBm, 1dB compression point of 1.6dBm, maximum PAE around 8%, and a power gain of 11.9dB as shown in Figure 2-72. These results cannot be acceptable to pass under the 5G

requirements. The main cause is the degradation of transistor performance at high frequency, which reflects the advantage of the FD-SOI technology in mm-wave band.

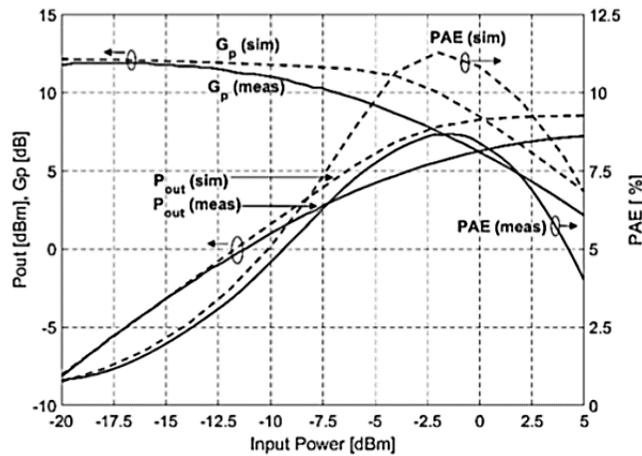


Figure 2-72. PA Performance [69]

2.3 Noises

The noise is a source of imperfection that limits the overall performance of communication systems degrade the quality of the useful signal and therefore disturbs its recovery during its baseband processing.

2.3.1 Noise Figure

The noise factor or Noise Figure (NF) is a criterion that allows to appreciate the quality of a system according to the noise it generates. In other words, it measures the degradation of the link quality by the system. It is therefore defined by the signal ratio of input noise (SNR_{in}) on the output signal-to-noise (SNR_{out}).

$$NF = 10 \log F \quad (2.61)$$

Where

$$F = \frac{SNR_{in}}{SNR_{out}} \quad (2.62)$$

The expression of the noise factor F can be developed from noise modeling of a two-port system [70] in Figure 2-73.

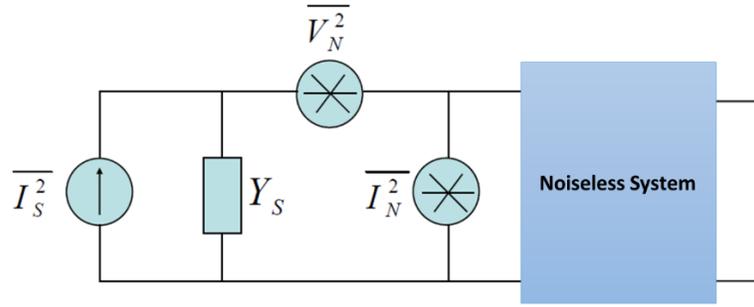


Figure 2-73. Noise modeling of a two-port system

$\overline{I_S^2}$ is the equivalent noise current generator associated with the Y_S admittance.

$\overline{I_N^2}$ and $\overline{V_N^2}$ correspond respectively to the generators noise equivalents current and voltage associated with the studied floor.

The noise factor is defined as follows:

$$F = 1 + \frac{|I_N + Y_S V_N|^2}{\overline{I_S^2}} \quad (2.63)$$

In the case where V_N and I_N are correlated, I_N can be divided into two parts: a correlated with V_N and uncorrelated, where:

$$I_N = I_C + I_U \quad (2.64)$$

With

$$I_C = Y_C V_N \quad (2.65)$$

And

$$Y_C = G_C + jB_C \quad (2.66)$$

The noise factor can thus be defined by

$$F = 1 + \frac{\overline{I_U^2} + |Y_C + Y_S|^2 \overline{V_N^2}}{\overline{I_S^2}} \quad (2.67)$$

This general noise-factor calculation method is used in many research works [71] [72], to propose an optimum dimensioning of the block for a minimum noise factor.

2.3.2 Noise of a System

According to the formula of FRIIS [73], the overall noise factor of a system composed of n cascading stages, as shown in Figure 2-74, is given according to gain G_i and noise factors F_i by the following formula:

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots + \frac{F_n - 1}{G_1 G_2 \dots G_n} \quad (2.68)$$

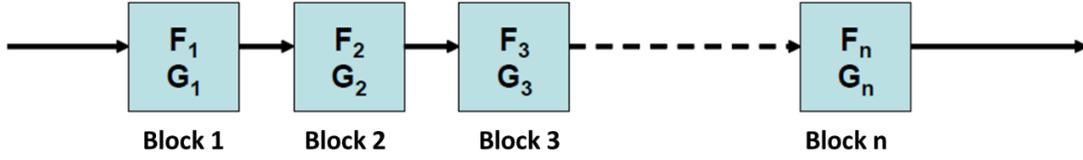


Figure 2-74. Noise factor of n-stage cascade system

The preceding equation highlights the importance of the gain and the noise factor of the first floor. Indeed, it conditions the total noise factor of the system. Therefore, reducing to maximum figure of global noise is to focus more precisely on the first floor. A design methodology must then be adopted to study its noise that depends strongly on the size of the input transistor of the first block.

2.4 Proposed System

The design of the harmonic feedback multi-oscillator HFMO using the 28nm FD-SOI technology consists of LNPA, PA, Diplexer, and Phase Shifter blocks as shown in Figure 2-75. The differential architecture is chosen. In differential amplifier, the Volterra output equations are

$$V_o = V_{in}^+ - V_{in}^- \quad (2.69)$$

Where

$$V_{in}^+ = V_{noise} + a_0 + a_1 V_i^1 + a_2 V_i^2 + a_3 V_i^3 + a_4 V_i^4 + a_5 V_i^5 \dots \quad (2.70)$$

$$V_{in}^- = V_{noise} + a_0 - a_1 V_i^1 + a_2 V_i^2 - a_3 V_i^3 + a_4 V_i^4 - a_5 V_i^5 \dots \quad (2.71)$$

Then

$$V_o = 2a_1 V_i^1 + 2a_3 V_i^3 + 2a_5 V_i^5 \dots \quad (2.72)$$

It has the benefits of boosting the output power of the fundamental signal and the third harmonic signal together. Moreover, it cancels the noise signals with the even harmonic signals, so the NF of the amplifier is from the internal noise of the transistor and due to the internal resistance of the matching circuits. The desired fundamental frequency is 25GHz, and then the third harmonic frequency is the 75GHz. The choosing of these frequencies is to occupy two candidates of 5G frequencies, which make the oscillator wide and more applicable.

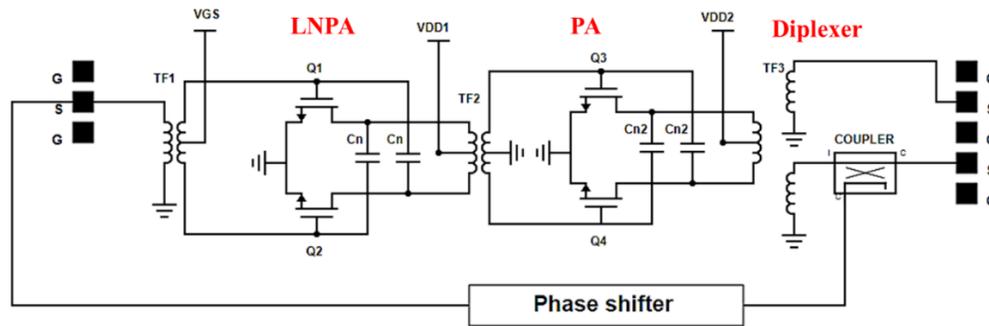


Figure 2-75. HFMO Schematic Diagram

The power oscillator targeted specifications to be achieved are summarized in the table below.

Table 2-7. Power Oscillator Targeted Specification

Fundamental signal frequency (F_0)	25 GHz
Third harmonic frequency ($3F_0$)	75 GHz
Noise Figure (NF)	< 4 dB
Input matching (S_{11})	<10 dB
F_0 output matching (S_{22})	<10 dB
$3F_0$ output matching (S_{33})	<10 dB
Gain	>15 dB
F_0 output power	>10 dBm
$3F_0$ output power	>0 dBm
Phase noise ($F_0, 3F_0$)	< -100 dBc/Hz @ 1 MHz offset
PAE	>9%

Each block has a role and targeted performances, and it can be different from conventional consideration of the amplifiers. The first block is the low noise power amplifier LNPA, its goal is to generate large output power with minimum noise figure. The priority in this block is to have low noise figure (<4dB). The importance of the noise figure in the first block is that it dominates the whole system noise figure as shown in section 2.3.2. A decreased noise figure enhances the phase noise of the system. Moreover, the LNPA will acts as a driver for the PA; it ensures the necessary input power for the PA. The class of operation is class A, which can achieves lower noise figure than other classes due to the absence of the harmonics and reduced noise sensitivity parameter. Moreover, it achieves high gain. TF₁ is an input-matching transformer; it transforms the common mode single end to differential inputs for transistors Q₁ and Q₂, where an attention should be taken to minimize the noise introduced by the integrated transformer. Two C_n are used as neutralized capacitors to stabilize the transistors.

The PA is to amplify the output signal of the LNPA. Other PAs focus in generating the maximum fundamental power with the best or compromised power added efficiency. The harmonics are trapped to ground except in class J, the second harmonic is phase shifted to enhance the fundamental output power. While in this system, the PA is to generate mainly the third harmonic in addition to conventional considerations. The choosing of optimal load impedance for the third harmonic signal will conflicts with the optimal load impedance for the fundamental power signal degrading the efficiency of the PA. The priority in this block is to generate the maximum third harmonic power. TF_2 is an inter-matching transformer. It is used to introduce the optimal load noise impedance to the LNPA, and transform that impedance to the input impedance of the PA transistors with minimum power loss. It is differential-to-differential transformer. The capacitors C_{n2} are neutralized capacitors to stabilize the transistors Q_3 and Q_4 . The PA class of operation is lightly AB, in order to have the advantage of compromise between the output power and the efficiency. The body bias voltage is set to the maximum allowed voltage (3 V) to minimize the threshold voltage and boost the output power.

TF_3 represents the output matching circuit, it consist of diplexer. The diplexer is to differentiate and separate the two frequency signals: 25 GHz and 75 GHz. The isolation between the two ports is very important, because it is the main key to decrease the effects of impedance variation and pulling effects from the $3F_0$ chain on the feedback loop. The diplexer has a band pass behavior, and it will represents the optimum impedance for the transistor to generate maximum third harmonic power. A new topology of diplexer will be introduced as an integrated diplexer transformer, which is compact and integrated on chip. The matching and filtering actions will introduces losses. The target is to have around 25 dB isolation and < 4 dB internal losses. The diplexer will have two output chains; each chain is fed to 50Ω RF PAD.

To construct the feedback loop, part of the output signal F_0 should be fed back to the LNPA input in such a way that the feedback signal is regenerated, re-amplified and fed back again to maintain a constant output signal. The part taken from F_0 can be done by inserting a coupler at the fundamental chain. The coupler is a three-port network, which has input signal, output signal, and coupled signal that fed the input of the LNPA. The first law of Barkhausen is $|G(j\omega).H(j\omega)| = 1$, in other words, the gain within the loop (provided by the overall amplifier) should exactly match the losses caused by the feedback circuit (coupled signal) within the loop. This criteria specify the coupling ratio which should be designed regarding the coupler. In this way, there will be no increase or decrease in the amplitude of the output signal at the steady state. The coupling ratio will be around 16 dB.

The phase shifter is to ensure that the feedback signal is in phase with the input of the LNPA. According to Barkhausen second law, $Arg\{G(j\omega).H(j\omega)\} = 0[2k\pi]$ then a phase shifter is needed to match the phase shift of the coupled signal to that of the LNPA input. Other than that, the oscillation will not be stable or will be destructive. The phase shifter should be around 320° , and can have a loss of 5 dB.

The stabilization of the oscillator system will depend on the compression point of the power amplifier. At initial time, the feedback circuit will have 1 dB power gain more than the amplifier, which make the output signal increased until the PA enter the 1-dB compression point, then the coupled signal will decreased by 1-dB causing the unity gain of the closed loop system at the steady state. This means that the amplifier gain is equal to the feedback losses. The LNPA will be in the linear region and will not enter the compression zone in order to avoid the AM to PM modulation, which can degrade the phase noise of the oscillator. The plan is shown in Figure 2-76 showing the power at each block.

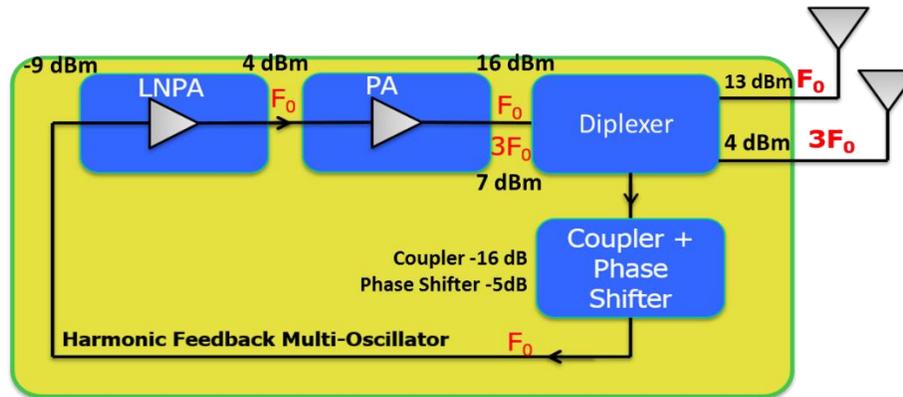


Figure 2-76. HFMO Power Performance

2.5 Conclusion

This chapter is divided into three titles: bulk CMOS limitation and alternative transistors, power amplifier, and HFMO system.

In part one, it provides an overview of the challenges faced by conventional CMOS scaling. It explains fully depleted devices, such as planar UTBB FD-SOI and Tri-Gate FinFET, as the alternative solutions of bulk transistors at 28-nm and beyond, shedding the light on their designs and performance. Then, a comparison is made between the two alternative transistors comparing their physical properties, electrical properties, and their preferences in different fields and applications.

In part two, the characteristic of the power amplifier are explained as gain, efficiency, and linearity. Then it discusses briefly the architectures and the topologies of PA, which are single ended (common source with cascade), differential, and balanced. Then it passes to the classes of the PA, it differentiate them as sinusoidal classes and switching classes. Each class is explained showing the difference of biasing signal, and output current. It discusses the size of transistor and effects of interconnection layout parasitic. Then the class J is introduced and compared with class AB. A comparison is made and the theoretical effectiveness of Class-J topology for single stage large signal amplification is simulated. Moreover, two distinct transistors - widths of 250 μm and 350 μm - are simulated where each has its own topology in order to study the impact of increasing

the width on the performance of the PA. As a result, Class-J PA design and its analysis show an improvement in output power, power gain, PAE, and bandwidth over than that of Class-AB. The result matches the one mentioned in the theoretical approach.

Then it discusses briefly the stability conditions and analysis in small signal and large signal, showing the stabilization techniques used in amplifiers design. A new study is done about a new stabilization technique for the common source amplifier, showing its result on improving the stability, reverse isolation, and gain over the conventional common source and over the conventional stabilization techniques as RC shunt feedback.

The optimum load impedance is also discussed to show the difference between the conjugate matching, graphical method, and load-pull analysis. Then a PA state of arts are listed and discussed briefly showing the results and performances achieved at the most advance nodes of CMOS technology. It passes to the low noise amplifier; the noise figure is defined and explained, showing its effects on the overall system noise.

The third part introduces the design of the oscillator architecture system defining each block with its function and specifications.

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Chapter 3 Design of Power Oscillator

Chapter 3 will show the design of each block starting from back end of line of the kits, RF PAD, and integrated transformers design. Then it passes to the design of the variable gain LNPA showing its performances, results, and comparing it with a state of arts table. It continues to show the design of the PA including the design of inter-matching circuit, the output matching (Diplexer), the coupler, and the phase shifter. Then the oscillator system is simulated showing its results and comparing it with other oscillators, which are working on the same band of frequency.

3.1 FD-SOI BEOL

At the beginning of the study, the Back End of Line (BEOL) 28nm FD - SOI CMOS technology from STMicroelectronics is illustrated on Figure 3-1. It consists of 10 metal layers with vias plus the Alucap top layer. It is divided into three groups:

- Thin metal layers from M1 to M6
- Medium metal layers B1 and B2
- Thick metal layers IA and IB

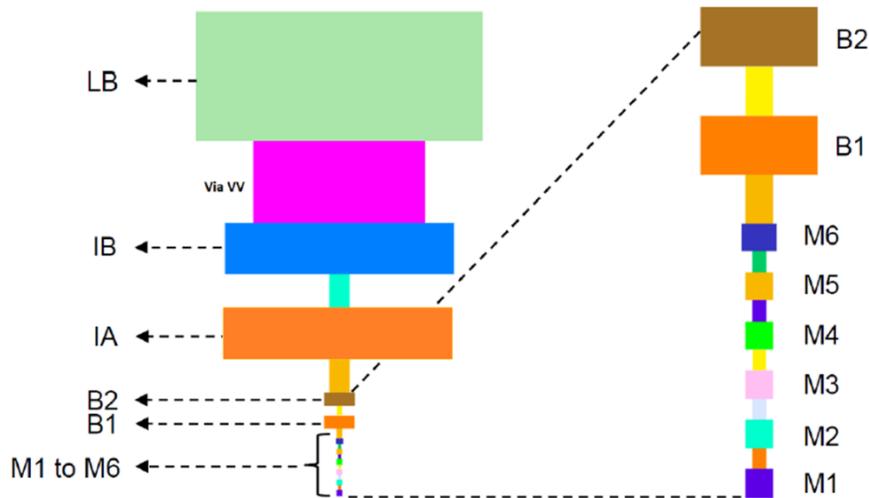


Figure 3-1. 28nm FD-SOI BEOL

The thin layers and medium layers are resistive; they are used to connect transistors to the passive elements, while the passive elements with the interconnections are built in widest and highest layers as IA, IB, and Alucap to reduce the loss of the internal resistance and the parasitic capacitance with the substrate.

After 2017, a new kit from STMicroelectronics was considered, which remove the B1 and B2 metal layers. This step of transformation degrade the performance of circuits at the mm-wave band; the capacitance with the substrate is increased as the distance between the passive elements and the substrate decreased leading to degrade the quality factor for different elements as RF-PADs, inductors, integrated transformers...

The number of design rules to be respected during the layout drawing is increased as the length of the channel decreased as shown in Figure 3-2. For the 28nm FD-SOI, the DRC recorded 5000 rules leading to more time spent in circuit design.

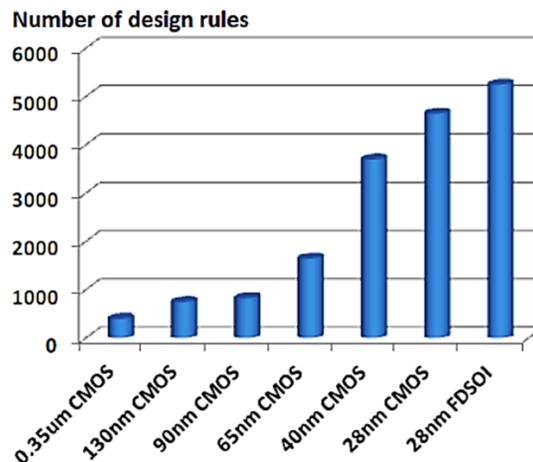


Figure 3-2. CMOS Technology DRC numbers

3.1.1 RF PADs

The RF PAD is an important element in the circuit design. It should support the size of the probe contact in addition to the metal density rules to target for the wire bonding for packaging. The dominant parasitic effect is the capacitance to ground in the mm-wave band. Two types of RF pads are used: shielded and unshielded RF pads. Each of these structures has advantages and disadvantages. Unshielded RF pads have a lower equivalent capacitance but more losses in the substrate. While shielded RF pads prove particularly interesting when the conductivity of the substrate is not well known or immunity with the substrate is desired. In this work, a shield RF pad is used to prevent the leakage into the substrate. As shown in Figure 3-3, lower metals M1 and M2 are stacked to form a shield. The pad area is over Alucap and IB to ensure low resistance and enough area. Dummies are inserted between pad areas and the shield to ensure the mechanical robustness for probe contact.

Electromagnetic simulations are necessary to take into account all the parasitic effects such as inductive and resistive effects associated with metals or capacitive coupling with the ground

plane or substrate. Usually, the equivalent capacitance is calculated by 1-port network analysis where

$$C_{eq} = \frac{1}{Im(Z_{11}) \cdot 2\pi f} \tag{3.73}$$

While this analysis can't calculate the series inductance and resistance of the pad area feeding the circuit, especially that these parameters are important to evaluate in the mm-wave frequency. Then, a two-port network should be done to obtain a PI model of the pad as shown in Figure 3-3 where

$$Z_{diff} = Z_{11} + Z_{22} - Z_{21} - Z_{12} \tag{3.74}$$

And

$$L_s = \frac{Im(Z_{diff})}{2\pi f} \tag{3.75}$$

$$R_s = real(Z_{diff}) \tag{3.76}$$

$$C_1 = \frac{Im(Y_{11} + Y_{21})}{2\pi f} \tag{3.77}$$

$$C_2 = \frac{Im(Y_{22} + Y_{12})}{2\pi f} \tag{3.78}$$

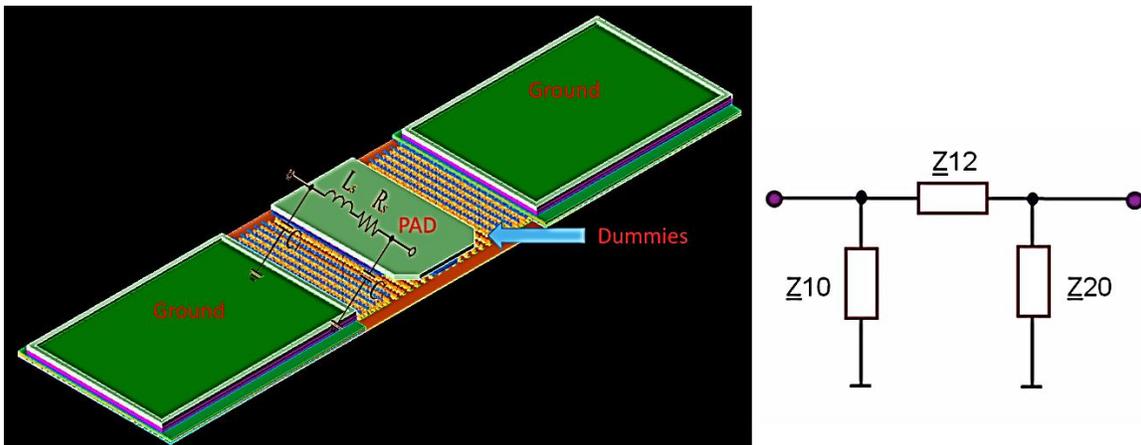


Figure 3-3. a) RF PAD

b) PI model

The table below shows the values of the shielded RF PAD at 25 GHz and 75 GHz

Table 3-1. RLC extraction of RF PAD

Frequency	C ₁	C ₂	L _s	R _s
25 GHz	37.6 fF	12.4 fF	9.8 pH	111 mΩ
75 GHz	46.6 fF	13.7 fF	9.7 pH	220 mΩ

3.1.2 Passive Elements

The capacitors used in the circuits are Metal Oxide Metal (MOM). They are constructed using standard BEOL metals and do not require additional manufacturing steps unlike MIM capacitors (Metal-Insulator-Metal), which were removed in the new kit. The MOM capacitors are built from M1 to M6, it has internal resistance, and attention should be taken for the quality factor of the capacitor at the desired frequency; as the value of the capacitance increases, the size increases and the resonance frequency decreases.

The integrated transformers are used widely in mm-wave band. It had better performance over the lumped elements. It is based on impedance transformation. It can be single end to single end, single end to differential, differential to single end, and differential to differential. In addition, it is used for power combining or power splitter. It consists of two inductor, primary and secondary, which are magnetically coupled.

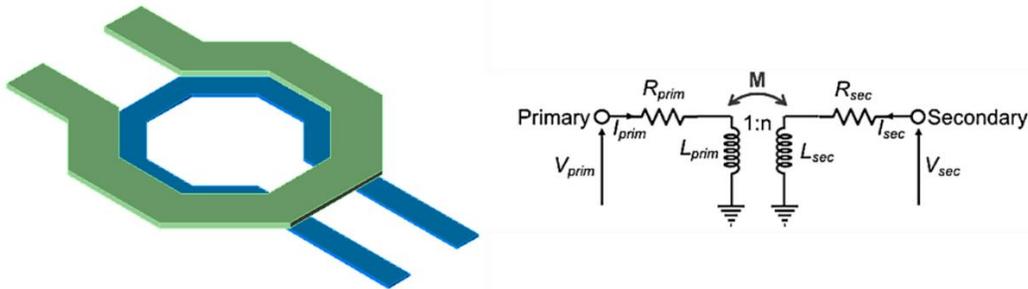


Figure 3-4. Transformer a) 3D view b) model

Currents voltages in primary and secondary are related by the equation

$$\begin{pmatrix} V_p \\ V_s \end{pmatrix} = \begin{pmatrix} j\omega L_p + R_p & j\omega M \\ j\omega M & j\omega L_s + R_s \end{pmatrix} \quad (3.79)$$

Where R_p and R_s represent the primary and secondary series resistors. The mutual inductance M between the two windings is dependent on the coupling coefficient k.

$$M = k\sqrt{L_p L_s} = \frac{Im(Z_{21})}{2\pi f} \quad (3.80)$$

Moreover, the coupling coefficient k can be extracted using the Z parameters

$$k = \sqrt{\frac{\text{Im}(Z_{21}) \cdot \text{Im}(Z_{12})}{\text{Im}(Z_{11}) \cdot \text{Im}(Z_{22})}} \quad (3.81)$$

The transformation ratio n between the input and the output is given by

$$n = \sqrt{\frac{L_p}{L_s}} = \frac{I_p}{I_s} = \frac{V_p}{V_s} \quad (3.82)$$

The input and output impedances are adjusted by varying the diameter of the windings, the metal widths and the coupling coefficient. The quality of each winding factor is defined by

$$Q_p = \frac{\text{Im}(Z_{11})}{\text{Real}(Z_{11})} = \frac{\omega L_p}{R_p} \quad Q_s = \frac{\text{Im}(Z_{22})}{\text{Real}(Z_{22})} = \frac{\omega L_s}{R_s} \quad (3.83)$$

In mm-wave frequencies, the inductance of the windings should not be too high in order to avoid resonance of the transformer. In addition, the shield under the transformer degrades the quality factor at these frequencies. The highest layer Alucap is the best layer that has highest resonance frequency due to the lowest parasitic capacitance with the substrate. The shapes of transformers as square or octagonal does not affects significantly. There are two types of integrated transformer; planar and stacked. The stacked one can achieve higher coupling factor and lower insertion loss. Attention should be made in designing the primary and secondary winding; the single ended coil is designed according to momentum and 1-port network analysis, while the differential coil is designed according to momentum and two-port network. The coil in differential connection achieves higher quality factor and lower series resistance than that in single end connection (approximately ratio of 2).

3.2 LNPA

The first block after the RFPAD input is the low noise power amplifier. The design purpose in this amplifier is to generate low noise figure (NF), since the NF of the first block dominates the NF of the whole system. In addition, the phase noise of the oscillator depends on the noise floor. The amplifier has the function of LNA in addition to power amplifier PA. It generates large output power taking into account the low noise figure of the amplifier stage. It is important to have a variable gain to control the gain of the oscillator loop, thanks to the body bias technique. A variable

and controlled power gain of 10 dB is designed in the STM 28-nm FD-SOI technology at the candidate of the 5G frequency 25 GHz. The LNPA is designed alone as a complete amplifier then it is merged with the second block of the system.

3.2.1 LNPA circuit

Figure 3-5 is the schematic view of the LNPA. It is built with 28-nm LVT FD-SOI transistors, the body bias can be tuned from -3 V to 3 V; but it is more efficient from -2 V to 3 V. A post layout simulation is done for the whole circuit including transistors, transformers, ground plane, DC and RF PADS. The layout is about 522x220 μm^2 without the DC/RF PADS. The transistor is biased in class A, and lightly AB when the body bias voltage is in the negative values. The class A biased voltage is optimum for the noise figure; In the design process of the LNPA, there is a trade-off between the noise matching and the power matching. This problem can be resolved by adjusting the biasing of the transistor input to reduce the noise sensitivity parameter R_n , so that it reduces the dependence of noise figure, NF, on the noise match [1] as shown below

$$F = F_{min} + R_n \cdot R_s |Y_{opt} - Y_s|^2 \tag{3.84}$$

Where F is the noise figure, Y_{opt} is the optimal source admittance for noise matching, and Y_s is the source admittance.

The frequency of operation is 25 GHz to occupy the fundamental signal of the system, and the supply voltage is about 1 V.

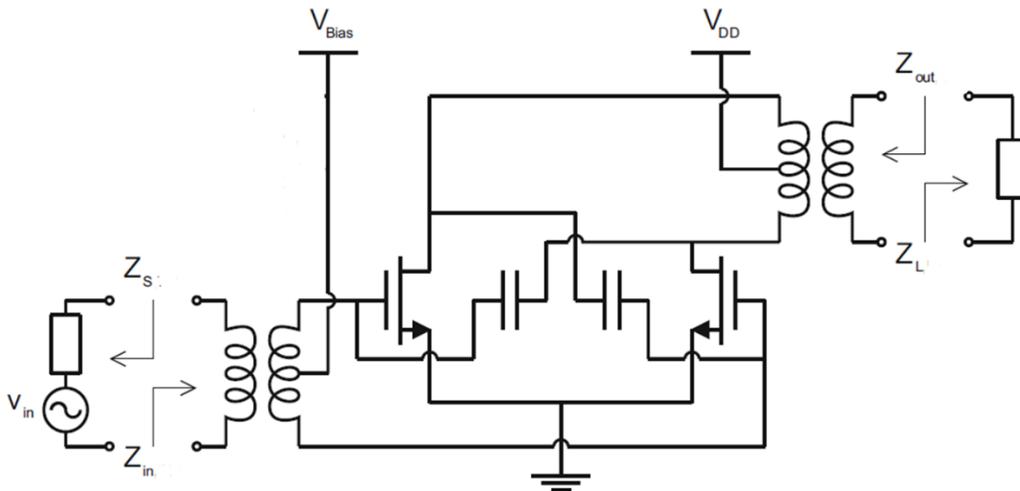


Figure 3-5. LNPA Schematic

The unit cell of the transistor layout has a 1- μm finger width and 50 fingers, which leads to have a total width of 50 μm for the unit cell as shown in Figure 3-6. Each side of the differential side contains two unit cells, and then each side has a width of 100 μm .

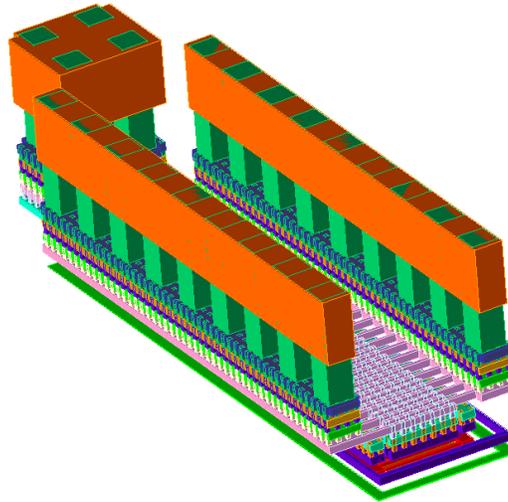


Figure 3-6. Transistor unit cell of $W=50 \mu\text{m}$

The input matching circuit consist of an integrated transformer, which has four purposes: power splitting, impedance power matching, impedance noise matching, and 180° phase between the two signals. The priority should be more for the noise matching. The single ended to differential center taped transformer; horizontal interleaved coils are built in the last metal (Alucap) to increase the quality factor and decreases the internal losses as shown in Figure 3-7. The shape is mastered well to have the desired coupling factor. The differential signals are perfectly balanced with 176° phase shift; 20 mV amplitude imbalance and 4° phase imbalance. The output matching circuit is consisting of differential center taped to single ended transformer; stacked coils are built in the last two metals IB and Alucap; it has 25 mV amplitude imbalance and 10° phase imbalance. The appropriate decoupling capacitors is chosen for the V_{DD} and V_{GS} center tap side taking in consideration the quality factor of each capacitor. A 10 k Ω of polysilicon is added to the coupling capacitors to block the RF signal from its path to DC source.

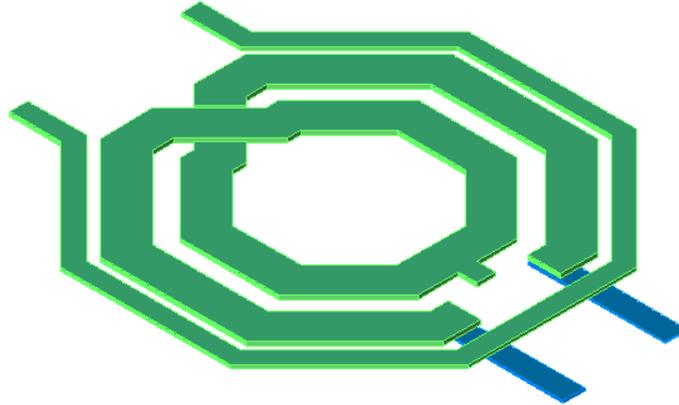


Figure 3-7. Input Matching Transformer

The neutralized capacitor is accurately adapted. The linear and nonlinear stability tests are done and it shows a stability in the steady state. The ground plane stacked from IA to Alucap to decrease its parasitic resistance.

3.2.2 LNPA Results

The results are based on momentum simulation for the RF PADs, transformer, and transistor thick metals, while the thin metals M1 to M6 are extracted using Quantus RLC extractor. The input/output reflection coefficients should be matched at the whole range of the body bias voltage. As shown in Figure 3-8, the input reflection coefficient S_{11} is between -17 dB at $V_{BB} = -2$ V and -28 dB at $V_{BB} = 3$ V, and the output reflection coefficient S_{22} varies between -14 dB and -30 dB at different V_{BB} . The 3-dB bandwidth is between 5 GHz and 6 GHz as the V_{BB} increases from -2 V to 3 V. In addition, the noise figure NF is around 2.75 dB then it degrades to 3.8 dB when the V_{BB} reached -2 V; this is because when the body bias voltage decreases to the negative range, the threshold voltage increased thus the amplifier class of operation start entering lightly the class AB. The small signal S-parameter are taken at the power level of P_{1-dB} .

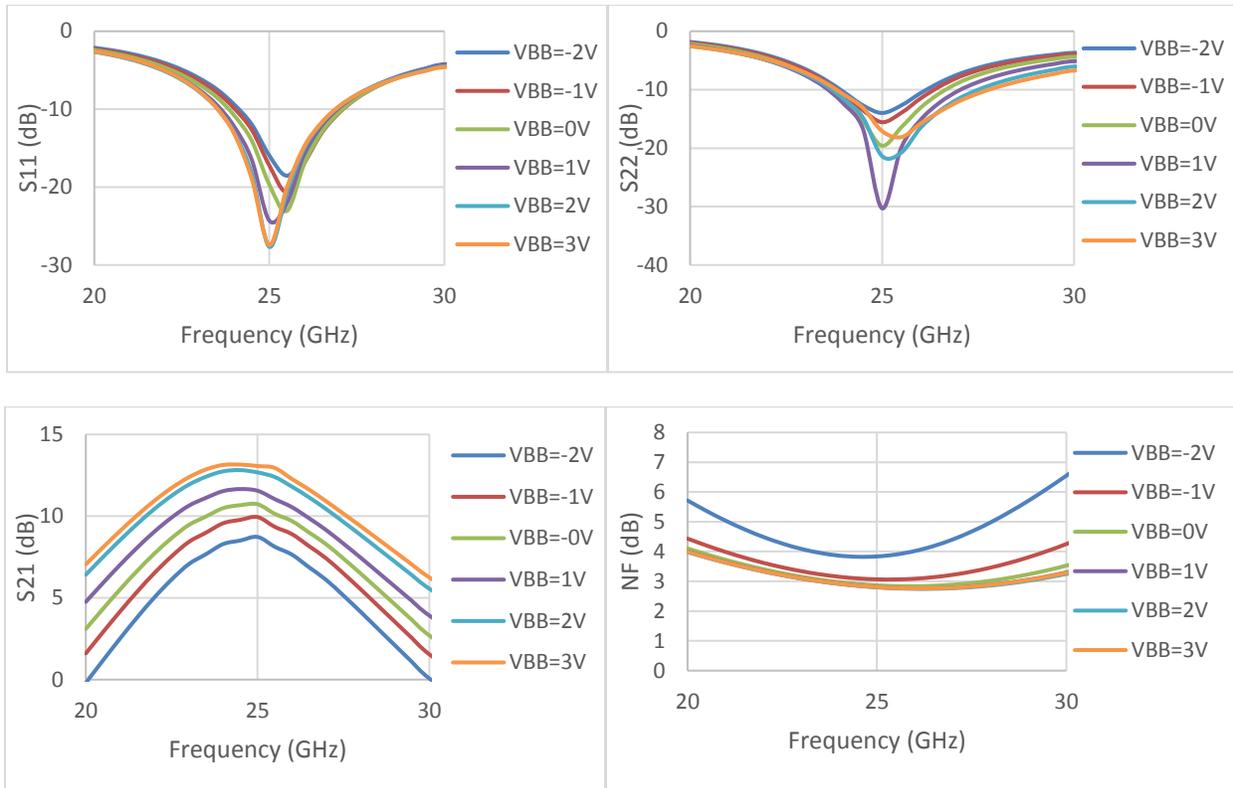


Figure 3-8. LNPA SP and NF at different VBB

The large signal parameters using harmonic balance analysis are shown in Figure 3-9 and Figure 3-10. The saturated output power P_{sat} is between 11 dBm and 13.7 dBm, and the power gain at the $P_{1\text{-dB}}$ point is between 8.8 dB at $V_{\text{BB}} = -2$ V and 15.9 dB at $V_{\text{BB}} = 3$ V. The variation of the power gain at different body bias voltage gives a gain tunable range of 10 dB; thanks to the FD-SOI body bias technique. The PAE_{sat} is 34.8 % and degraded to 23.7 % as the body bias voltage decreased from 3 V to -2 V.

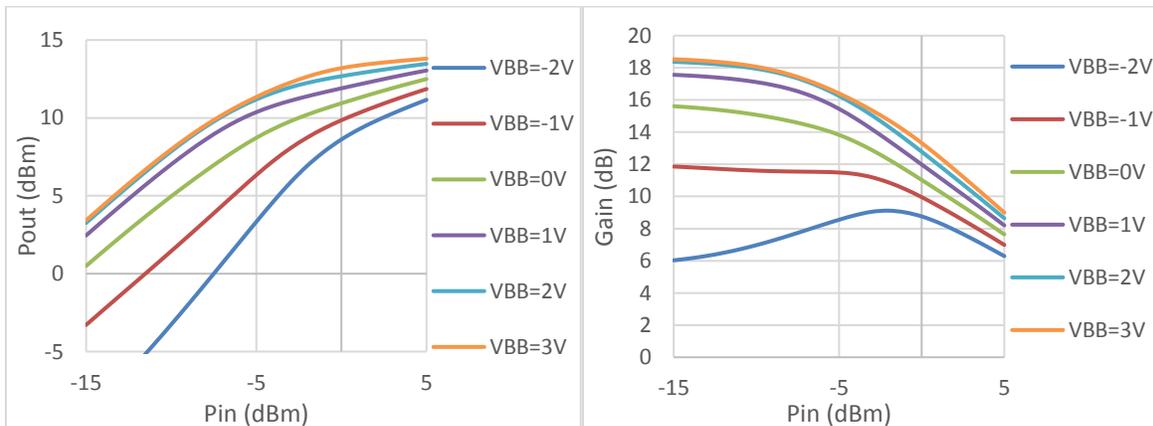


Figure 3-9. Output Power and Gain at different VBB

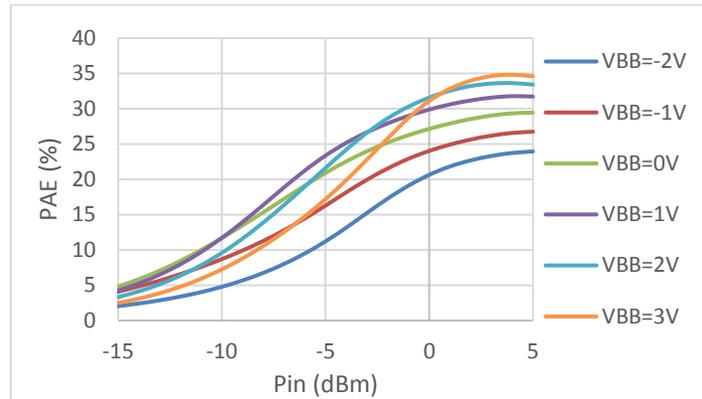


Figure 3-10. PAE at different VBB

Table 3-2 shows state of arts for different low noise amplifier and power amplifiers compared to the LNPA in this work. The LNAs to compare NF and gain parameters, while the PAs to compare the output power and PAE parameters.

For LNAs: In [2], it has the same number of stage as the LNPA but with lower NF and gain, which shows the improvement of the 28-nm over the 90-nm. In [3], it has better gain but higher noise figure than the LNPA; the high gain is due the higher number of stages (3_stages for both). In [4], it has lower gain and higher NF with two stages compared to one stage LNPA, while in [5] a variable gain LNA work in two modes; it have higher gain in but clearly higher NF in both modes with four stages. Note that the number of stages increases the overall gain and the bandwidth of the amplifiers that can reach 30 GHz as [12] (four stages), while the bandwidth designed in LNPA is to occupy the first candidate of the 5G frequencies. In addition, the LNPA has the highest input compression point ICP_{-1db} since LNAs are for small power signals.

For PAs, the work in [6] is two-stage differential amplifier, which has slightly lower gain and higher P_{sat} and PAE_{max} than LNPA; the FoM are very near to each other. In [7], it is done with the same stage number and node scale but in bulk technology. It shows a lower gain with 8.56 dB but higher something simple of P_{sat} and PAE_{max} ; this is due to usage of deep class AB instead of class A, where class A is the most convenient for LNAs, and an overdrive V_{DD} of 1.1 V. Note that the LNPA is not designed for maximum output power, maximum PAE, or lowest NF, but it is a compromise between these parameters.

So that, the LNPA shows the lowest NF and the highest gain when they are compared with taking in consideration the number of amplification stages.

Table 3-2. Amplifiers State of Arts

Reference/ Stage	CMOS Tech	Gain (dB)	NF (dB)	Center Freq.	P _{sat} (dBm)	PAE max %	V _{DD} Volts	PA- FoM	Circuit
[2]: LNA 1_stage	90 nm	13.8	3.8	37 G	--	--	1.2	--	Measured
[3]: LNA 3_stages	28 nm	23	4.5-5.8	50 G	--	--	1	--	Measured
[4]: LNA 2_stages	40 nm	12.5	3.8	60 G			1.2	--	Measured
[5]: LNA 4_stages	28 nm	18	7.8-9.8	81 G	--	--	0.9	--	Measured
		29.6	6.4-8.2	82 G	--	--		--	Measured
[6]:PA 2_stages	28 nm	15.7	--	30 G	14	35.5	1	74.7	Measured
[7]: PA 1-stage	28 nm	10	--	28 G	14.8	36.5	1.1	69.4	Measured
This work: 1_stage	28nm FDSOI	18.56	2.75	25 G	13.7	34.8	1	75.6	Simulated PLS

Where PA_FoM=P_{sat} [dBm] + Gain [dB] + 20log (Frequency [GHz]) + 10log (PAE_{MAX} [%])

3.3 PA

The second block in the system is the power amplifier. The PA design flow is different from that of LNPA. The LNPA follow the same flow of LNA design from left to right (input matching, output matching), while the PA is from right to left (output matching, inter-matching, driver stage, input matching). The PA design flow is shown in Figure 3-11.

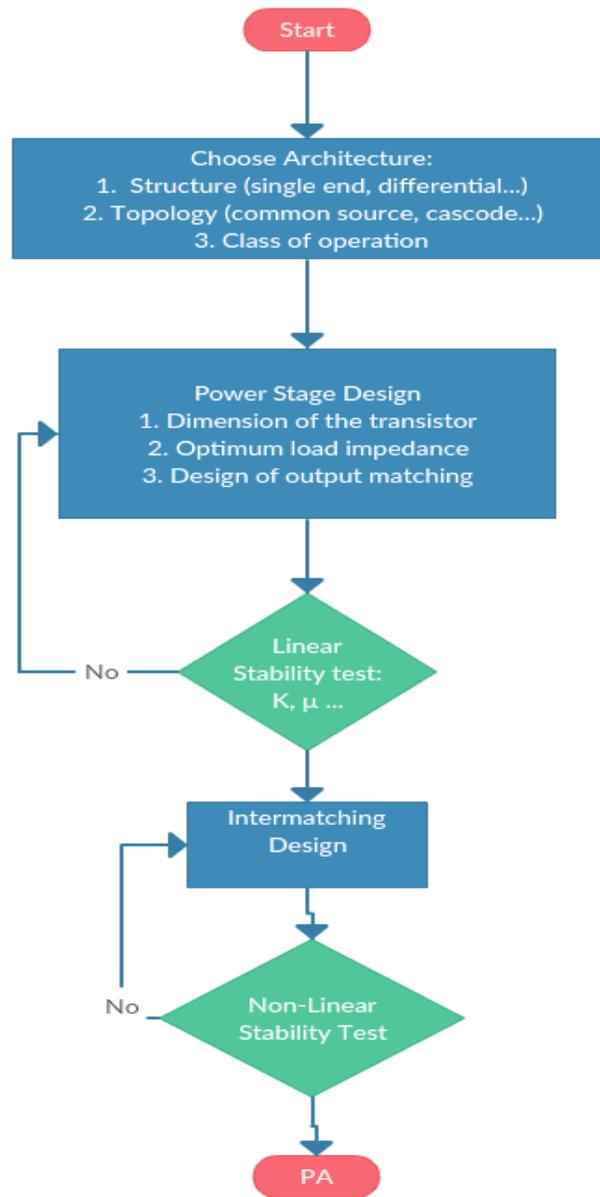


Figure 3-11. PA Design Flowchart

The main question is how the amplifier can generate harmonic signals. First, the class of the amplifier determine the current conduction angle, and as the current conduction angle decreases from 360° towards zero, the generation of the harmonics increases. The best case is class C where the amplitude of the second harmonic current can reach 25% of the maximum current and the amplitude of the third harmonic current can reach 15% of the maximum current amplitude. However, the overall result regarding the output power is low due to the small conduction angle of the drain current.

Second, the impedance of the output matching circuit can help in generating harmonic signals; when the load-pull is done for the PA output port, every point on the smith chart represent an impedance for the PA that will change the output performances of the amplifier. There is an optimum point for the fundamental power, and there is an optimum point for each of the harmonics (second, third...). These points or impedances are usually avoided because the traditional concept of the PA is to amplify the fundamental signal and trap the harmonics by the output circuit.

Third, the behavior of the PA in the saturation region is a non-linear behavior in which as the output power increases reaching the compression point, the fundamental power is compressed, while the harmonics power increases due to the non-linearity relation at the region of compression and saturation.

Finally, the parasitic RLC resulted from the transistor layout and the interconnections, increases the non-linear behavior of the amplifier. In addition, as the width of the transistor increases, the parasitic effects increases too.

In our work, we exploit the second, third, and the fourth point to generate the desired harmonic signal. The target is to increase mainly the width of the transistor, work on the saturation region, and choose the optimum output impedance for the desired harmonic signal. In addition, to double the output power of the fundamental and harmonic signal, the differential architecture is chosen due to that $V_o = 2a_1V_i^1 + 2a_3V_i^3 + 2a_5V_i^5 \dots$ then the third harmonic frequency is chosen to work on. The differential technique has additional advantages. It cancels the even harmonics, which make it easier in the filtering action at the output port. Moreover, the optimum load impedance of the third harmonic signal during the load-pull analysis is not very far from that of the fundamental signal that gives the opportunity to compromise between both points to generate both frequencies with better output power, thus targeting to multi-oscillator.

A study was done before on the single ended power amplifier. It shows an advantage on the output power of the second harmonic signal over the third harmonic. However, it has several disadvantages. The first one is the use of common source topology, which has limited output power and very sensitive to the ground plane losses due to the source degeneration effect. In addition, the optimum load impedance of the fundamental signal is far from that of the second harmonic signal, that means if the amplifier is desired to generate second harmonic signal, the fundamental power will be very low and can only ensure the feedback oscillation loop. These causes lead to search for other solution, which was the differential architecture.

3.3.1 Proposed Transistor

Several simulation were done to choose the optimum width of the transistor that has the ability to generate higher output power of third harmonic. A transistor of width 350 μm and 1 μm

finger width was designed. The layout consist of seven-unit cells. Each cell is $50\ \mu\text{m}$ as shown in Figure 3-12.

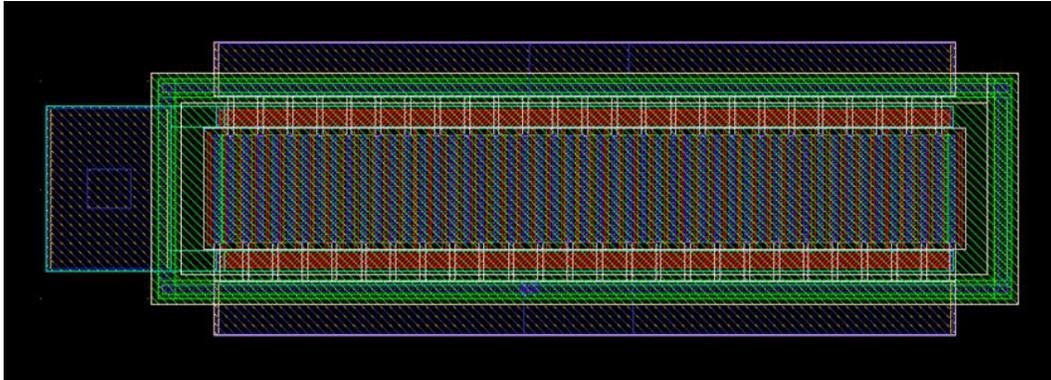


Figure 3-12. PA Transistor Unit Cell

The unit cell consist of the layers from N-well till the M6. The thick metals IA and IA connects the five cells. Figure 3-13 shows the view of both transistors used as differential amplifier with the interconnections of the neutralized capacitors.

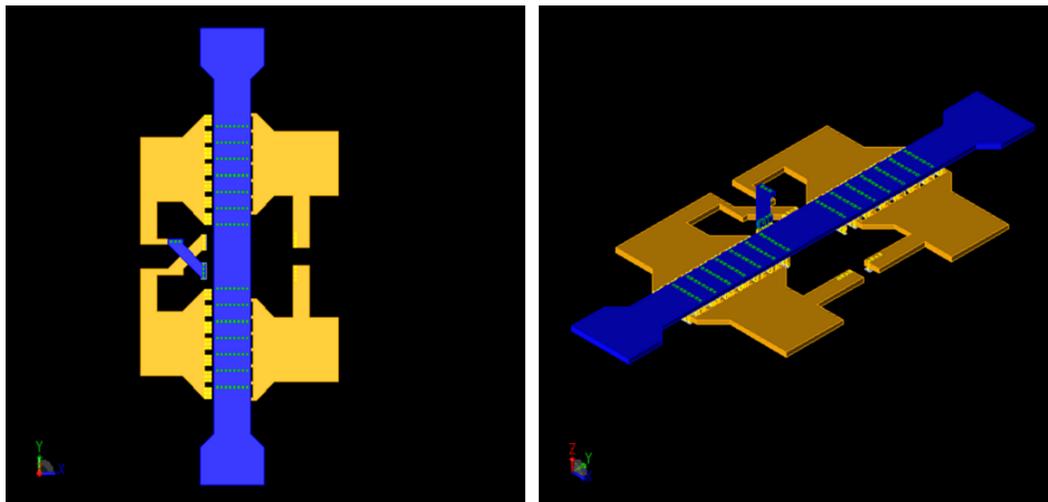


Figure 3-13. Differential Transistors View

An RLC extraction is done for the unit cells (thin metals) and EM momentum simulation is done for the thick metals. The RLC extraction is more efficient where very thin metals and huge number of vias are used, while momentum is more efficient where thick metals are used. The stabilization of the amplifier is done by MOM capacitors (20x50 fingers) using neutralization technique.

3.3.2 Output Matching-Diplexer

The output matching circuit is used to match the 50Ω to the optimum impedance that the amplifier have to see it. In single ended amplifiers, the passive component (LC) are widely used as a form of L section, Pi section, or T section. In addition, integrated transformers shows good performances at mm wave frequencies regarding the size and the internal losses. The matching by transmission lines has the negative side due to its big size ($> \frac{\lambda}{4}$). In differential amplifiers, the matching circuit depends on the integrated transformers due to its abilities in transforming between single ended mode and differential mode, power combining/splitting, and impedance transformation. A load pull analysis is done to adopt the impedance that the amplifier should see at the output of the transistor. The result of the load-pull analysis is shown on the smith chart as shown in Figure 3-14.

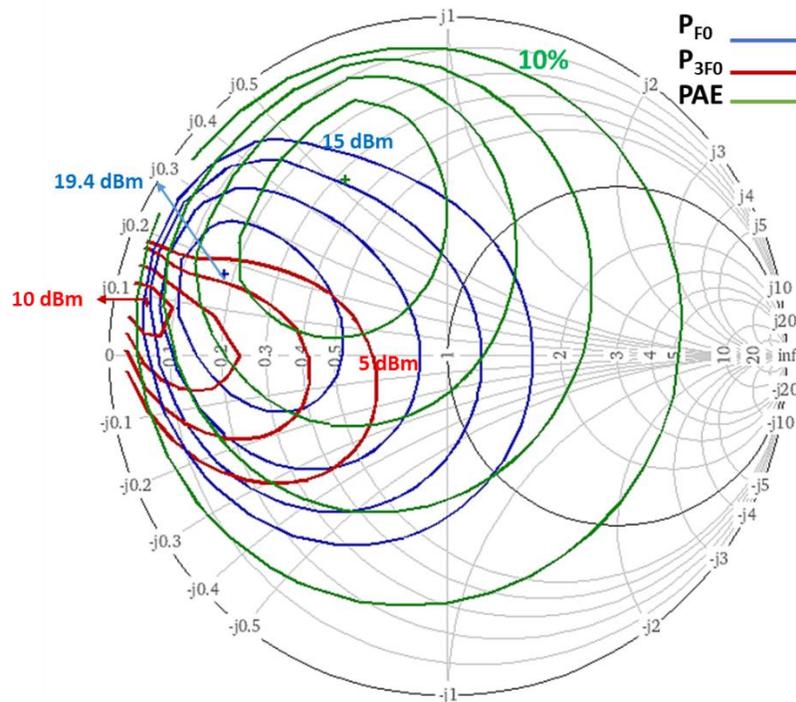


Figure 3-14. PA Load-pull Analysis

The optimum impedance of the third harmonic signal is near to the optimum impedance of the fundamental signal. It gives the opportunity to generate both signals. The PAE of the fundamental signal is decreased as going toward the third harmonic optimum impedance, this ensure the non-linearity of the selectable transistor that the consumed DC power is transformed in a form of generating odd harmonics (third one mainly). The optimum point of the third harmonic

is chosen and is mentioned as a desired value. It joins the circle of 15 dBm fundamental output power and the circle of 10 % PAE.

The output of the PA will have two signals of different frequencies 25 GHz and 75 GHz. then there is a need of diplexer to differentiate between both signals. The diplexer is different from duplexer. It is a three-port network. It splits the incoming signal that include the two signals. It has the action of band pass filter at each of the two frequencies with high isolation. Usually, the mm-wave diplexers are designed outside the chips using transmission lines in order to achieve very high selectivity. This selectivity cannot be achieved using the passive components on chips due to the degraded quality factors at the mm-wave band. Table 3-3 shows different technologies used in diplexer design.

Table 3-3. Comparison between the different technologies used to design mm-wave diplexers [8]

Diplexer Types	Waveguide	Dielectric Resonator	Planar	Quasi-Planar	SIW	HTS (High temperature superconductor)
Frequency	5-100 GHz	0.5-100 GHz	0.5-100 GHz	0.5-100 GHz	0.5-100 GHz	0.5-100 GHz
Quality Factor	Very High	Very High	Low	High	High	Low
Size	Large	Large	Small	Large	Moderate	Small
Power Handling	High	High	Low	High	Low	Low

In our case, an integrated diplexer technology is needed. A way can be used is to transform the differential end to single end and then feed the signals to two band pass filters. Each filter allows a desired frequency to pass and make a resonance for the other one using the lumped elements. This technique has several problems that degrades the performances and can deteriorate the results of the amplifier. The internal loss will be high due to the usage of several stages, and the differential to single end transformation block should be matched at two bands to allows the two frequencies signal to pass to the band pass filter, which increases the complexity.

A new topology is introduced in this work, it is a diplexer based on three layers integrated transformer. It has several functions, which are output-matching circuit, filtering action with good isolation of the 25 GHz and 75GHz, and differential to single ended transformation. They are designed in one block to save area and to decrease the losses. The differential outputs are feeding to the inductor L_0 on IB metal, the IB is vertically between IA and LB (Alucap). The LB layer is designed for the 75 GHz path, it has better quality factor than the layer IA because the distance between the metal layer LB and the substrate is higher than that of IA. An iterative process is

needed to achieve the inductances values L_0 , L_1 , and L_2 with the desired coupling factors. C_1 and C_2 to make the diplexer input port matched at the two frequencies. The challenge is that there is a coupling between the metal layers IA and LB, which means the isolation between 25 GHz and 75 GHz is mainly degraded especially that as the frequency increases, the coupling factor increases too. The solution was to make the L_2 more vertical in shape and L_1 more horizontal in shape to decrease the vertical common area between both inductors. C_3 and L_3 forms a high pass filter to increase the isolation between the 75 GHz path and the 25 GHz path.

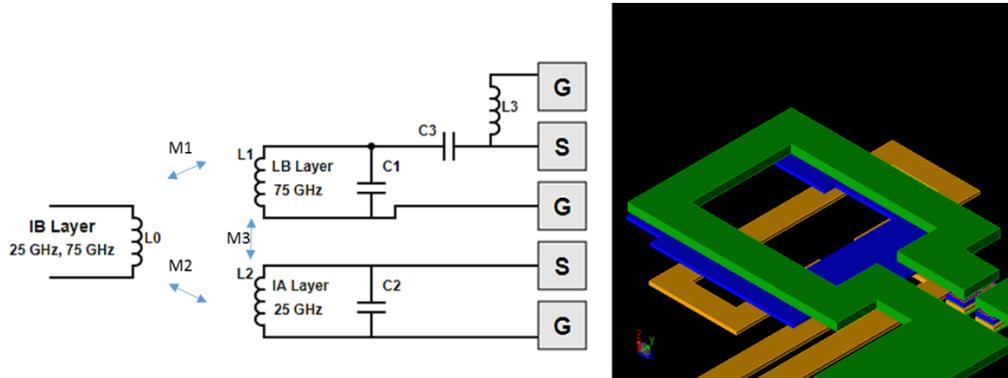


Figure 3-15. Diplexer Schematic and Layout View

The results of the diplexer three-port SP analysis are shown in Figure 3-16. The input matching S_{11} is matched at 25 GHz and 75 GHz. the output matching S_{22} and S_{33} are perfectly matched (< -15 dB). The isolation is between 25 dB and 30 dB. The transmission losses is 3.4 dB at 75 GHz and 3.55 dB at 25 GHz.

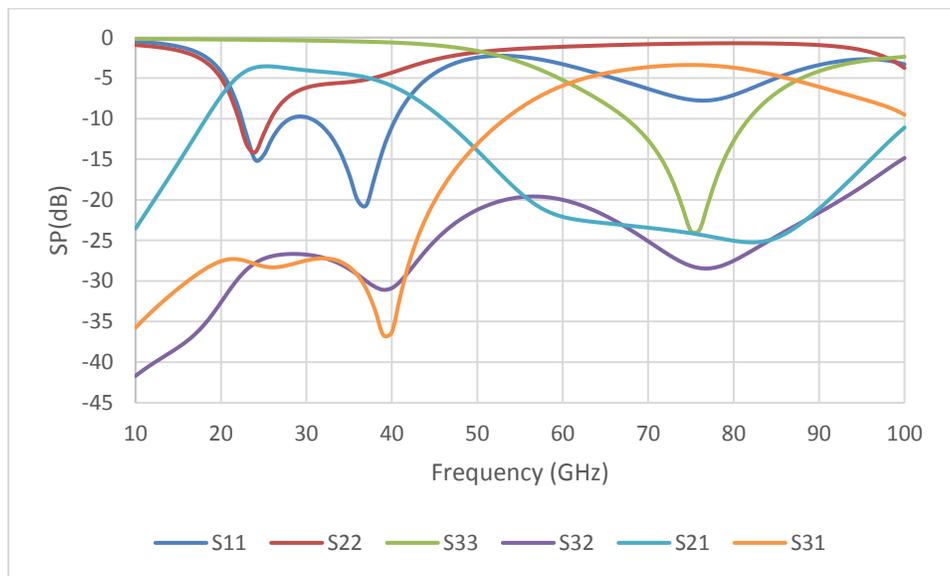


Figure 3-16. Diplexer SP analysis

Regarding the internal losses in the output matching, the disadvantages of using high width transistor is that the desired optimum load impedance is going toward the edge of the smith chart; as the width of the transistor increases, the maximum current increases, and the optimum load resistance is decreased. The transformation ratio to match the $50\ \Omega$ port become bigger, which will introduces more losses in the impedance transformation. The Figure 3-17 shows an example of the transistor width relation with respect to optimum load resistance and PAE at 28 GHz.

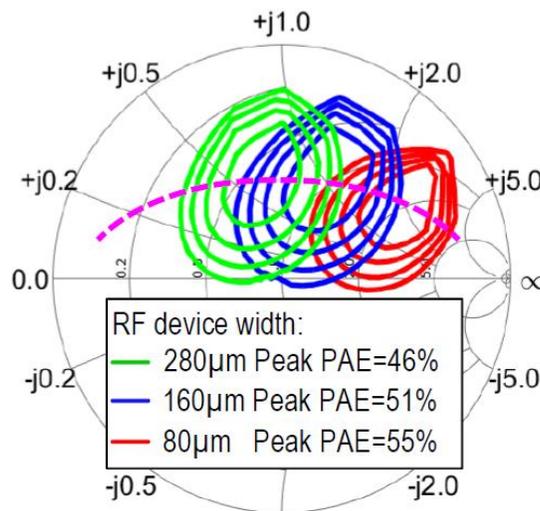


Figure 3-17. Typical Optimum Load Impedance and Peak PAE vs. Device Sizes @28GHz

3.3.3 Inter-matching

The inter-matching circuit is an impedance transformation from the output impedance seen by the driver (LNPA in our case) to the input impedance of the PA. The supply voltage is fed from the midpoint of the primary inductor to supply the LNPA. The integrated transformer transforms the impedance from $85-j20$ to $3-j41$. The layout view is shown in Figure 3-18.

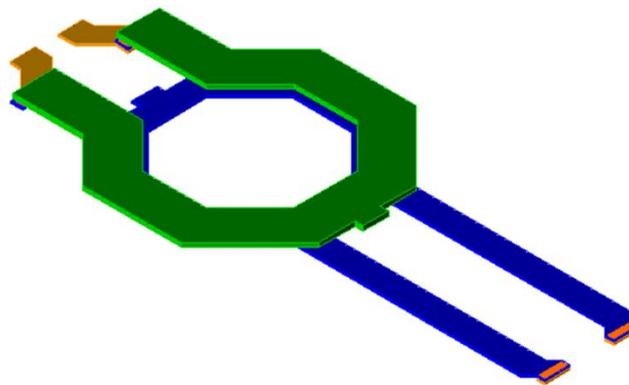


Figure 3-18. Inter-matching Transformer

Figure 3-19 shows the schematic of the PA block, which have the differential architecture. The drain voltage is around 1 V. Coupling capacitors are connected to the dc supply to protect it from RF signals. The neutralized capacitors ensure the stability of the transistors. Each transistor has a width of 350 μm that consist of seven unit cells as shown in Figure 3-13.

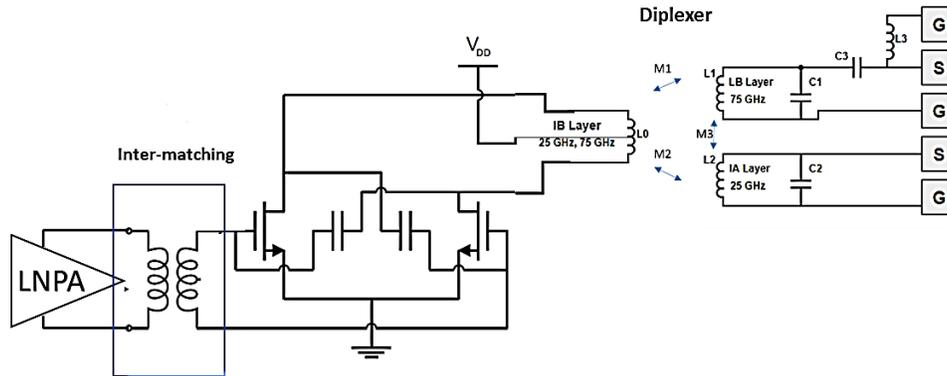


Figure 3-19. PA Schematic

3.3.4 PA Results

After designing the inter-stage transformer, a two-stage amplifier is obtained. Large signal SP, harmonic balance, and stability analysis were done for the amplifier. The large signal S-parameters results are shown in Figure 3-20.

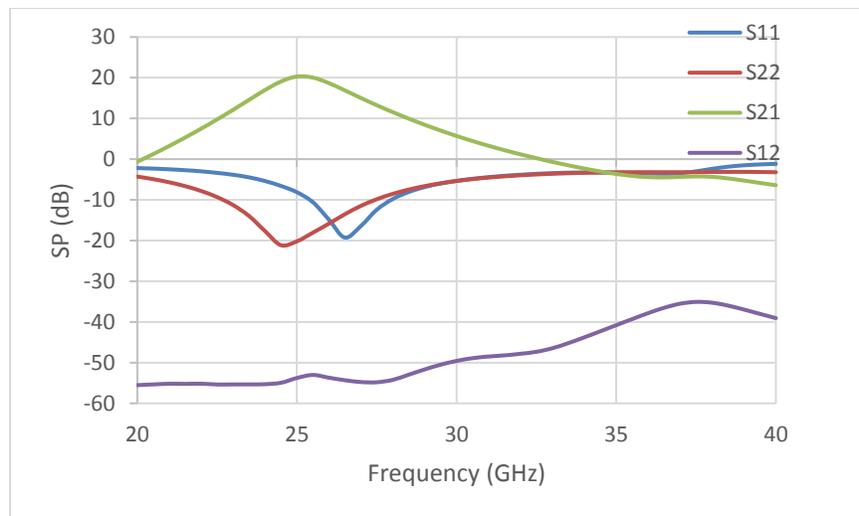


Figure 3-20. PA S-Parameters

The stability factor is shown in Figure 3-21. The linear stability analysis is not sufficient. The non-linear stability analysis (pulse test) shows the stability of the amplifier after optimizing the values of the neutralized capacitors. Each stage has its own ground plane to avoid stability problems. The stability was very sensitive for the ground plane of the second stage (350 μm transistors). As the parasitic inductance of the second stage ground plane increases, the third harmonic power degrades, while it can be enhanced after optimizing the neutralized capacitors, thus it enters the instability conditions. When the ground plane is optimized in shape to decrease the parasitic inductance by making the stack metals wider, the parasitic capacitance increases and lead to instability. The designed ground plane is more inductive and less capacitance to ensure the stability, but it degrades the third harmonic power while not affecting the fundamental power.

The large signal analysis are shown in Figure 3-22. The PAE_{max} is 9.2% for the fundamental, and 10% when the output power is the sum of both frequency signals. The maximum fundamental and third harmonic output power are 14.3 dBm and 4.5 dBm respectively. The maximum gain is 22 dB (at $P_{\text{in}}=-8$ dBm) but it is not constant because the second stage transistors are saturated before the LNPA transistors. The plan is to saturates the second stage transistors while the first stage keeps in the linear region; as the first stage saturates, an AM to PM conversion that can degrades the phase noise later when the amplifier is used in the oscillator system. The obtained results meets the targeted specifications.

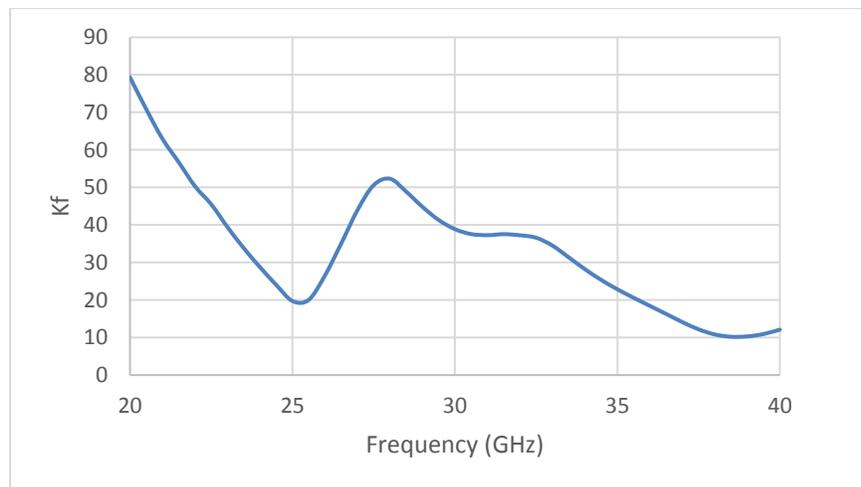


Figure 3-21. Stability Factor K_f

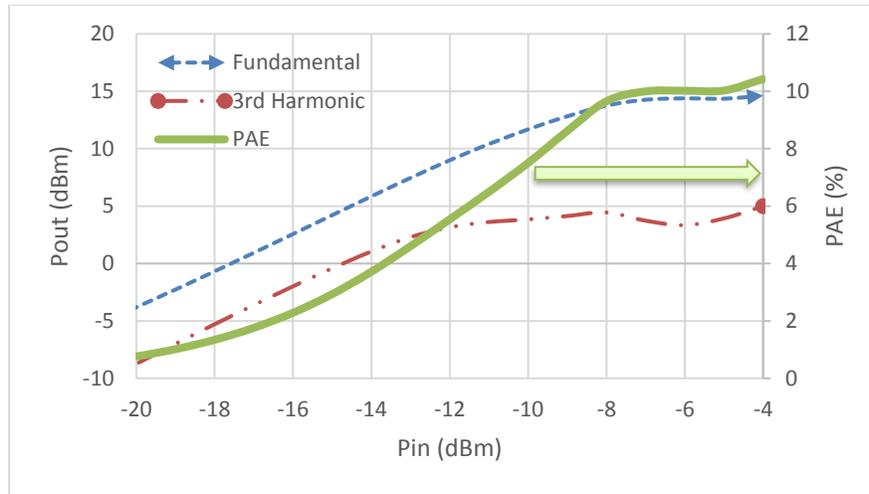


Figure 3-22. PA Large Signal Analysis

Table 3-4 shows PA State of arts at the node of 28 nm. It has clearly shown the advantage of the FD-SOI technology over the Bulk one. In addition, the designed PA in this work have different goals than others. It is not designed to achieve the highest output power or best PAE, it is designed to achieve generation of fundamental and third harmonic output power, and the priority was given for the third harmonic power at the expense of the fundamental power. Even that, it has an acceptable and medium FoM compared to the whole PAs in the table below. Noted that our work is a post layout simulation and not fabricated yet.

Table 3-4. PA State of Arts

Reference/ Stage	CMOS Tech	Max Gain (dB)	Center Freq.	P_{sat} (dBm)	PAE max %	V_{DD} Volts	PA- FoM	Circuit
[6]:PA 2_stages	28 nm	15.7	30 G	14	35.5	1	74.7	measured
[7]: PA 1-stage	28 nm	10	28 G	14.8	36.5	1.1	69.4	measured
[9]: PA 2-stages	28 nm FD-SOI	17.5	28 G	18.7	12.4	2	76	measured
[10]: PA 2-stages	28 nm FD-SOI	21.9	31 G	17.9	24.7	2	82.95	measured
This work: 2_stage	28nm FDSOI	22	25 G	14.3	9.26 (F₀)	1	74.458	Simulated PLS
			75 G	4.5	10 (F₀ & 3F₀)			

3.4 Coupler

To ensure the oscillation loop, a part of the fundamental power should feed the input as Barkhausen law such that $|G(j\omega) \cdot H(j\omega)| = 1$. The traditional couplers as directional coupler, Lange coupler, or Wilkinson divider depends on transmission lines. Every transmission line has a big length (around $\lambda/4$) which will occupy large area on the chip. Moreover, the cost of fabrication for the FD-SOI technology is high. Another solution is found in the work in [11] and convenient for integrated circuit; A third winding is added to the center of the output transformer to take a very small part of the power crossing it. This winding is designed to pair only 1% (-20 dB) of the power. It is made using the same thick layers of the primary and secondary windings of the BEOL in H9SOI technology as shown in Figure 3-23.

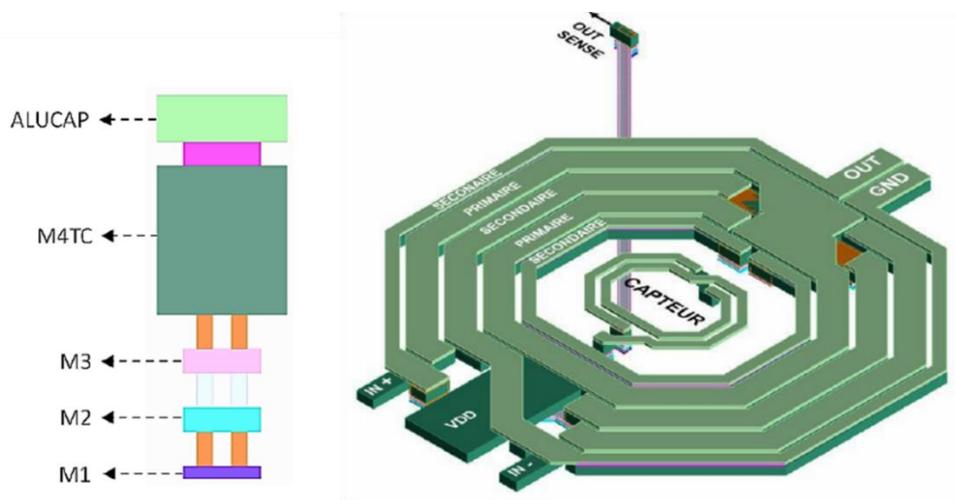


Figure 3-23. Integrated Coupler in H9SOI [11]

In our work, it is very complex to enter a small winding in the diplexer. Moreover, the diplexer is made of three layers, and every winding has low inductance value that reveals a small area. Then it is hard to implement inside the windings. In addition, it will interfere with the matching parameters, and will have a coupling power of both frequencies not only the fundamental.

Another solution, more compact is in [12]. Indeed, the power coupler is performed using a capacitive coupling of the voltage on a transmission line at the output of the PA as shown on the Figure 3-24. The voltage is then converted into a picture of power through the transmission line.

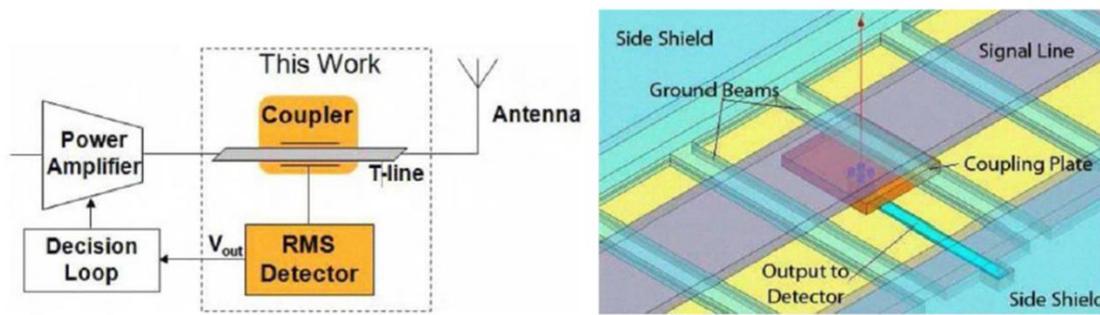


Figure 3-24. Proposed Coupler in [12].

A capacitive coupler with very low influence on the RF path is used. To do this, a small rectangular metal is inserted under the transmission line forming two abilities: one with the transmission line and the other with the substrate, which is grounded. The result is a capacitive divider. This rectangular metal is integrated under a coplanar transmission line at the output of the PA. This solution has the advantage of having a negligible effect on the impedance of the antenna presents to the PA.

The same topology is applied in the BEOL of the FD-SOI. The rectangular metal is sized, and calibrated which have the needed coupling power. The capacitive divider is form between the IB and LB layer. The power-coupling ratio is 16 dB.

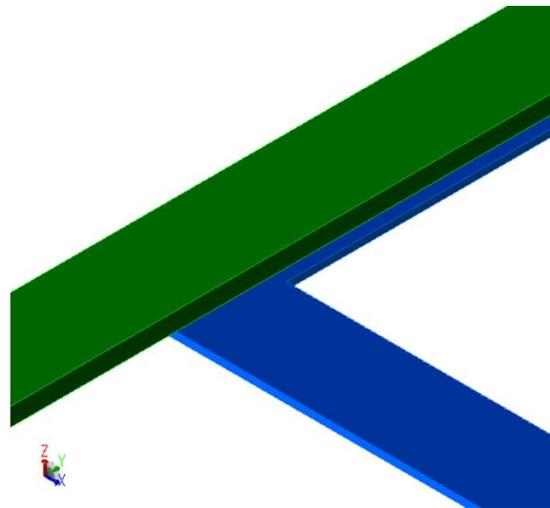


Figure 3-25. Capacitive Coupler Layout

3.5 Phase shifter

The second condition of Barkhausen criteria is to have a phase shift of 360° where $Arg\{G(jw).H(jw)\} = 0[2k\pi]; k \in N$. The output of the coupler is 340° phase shifted from the

input of the LNPA (RF PAD). In addition, the transmission line that will connect the coupler, whose location at the extreme right in the layout, to the input RF PAD, whose location at the extreme left in the layout, can be exploited to be a delay line. The delay line has an electrical length that has a phase shift.

Transmission lines allow the transport of electromagnetic energy in one direction with a wave propagating generally quasi-TEM mode (Transverse Electro-Magnetic). Each line has the characteristic parameters such as characteristic impedance Z_C and the propagation constant γ . Other more specific parameters such as losses per unit length α or effective permittivity ϵ_{eff} , can be deduced from Z_C and γ . Several topologies lines exist: microstrip (MS), coplanar (CPW), slotline, stripline ... The two most used in RF and millimeter integrated circuit structures are the microstrip line and the coplanar line shown in Figure 3-26.

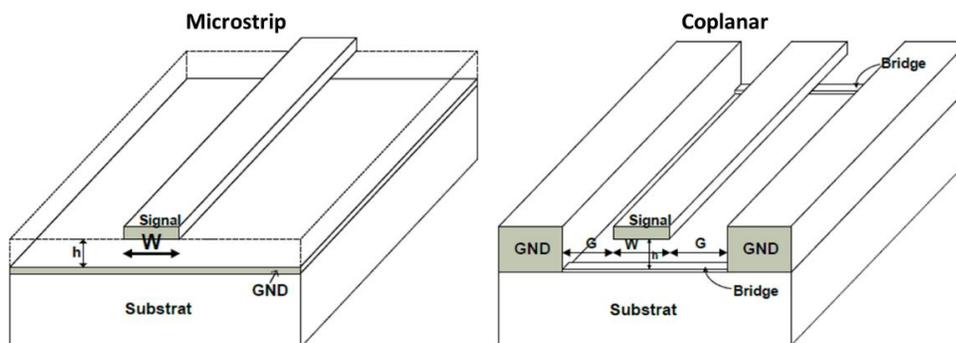


Figure 3-26. Microstrip vs Coplanar TL

The microstrip line MS is formed of a strip conductor and a ground plane separated by a dielectric material. This structure is compact but has few degrees of freedom to adjust the characteristic impedance Z_C , namely the width of the central conductor W and the thickness h of the dielectric. In standard integrated technology, the impedance characteristics achievable range is narrower than that of coplanar lines. However, most of the electric field is concentrated in the dielectric between the conductor and the ground plane, making it an attractive solution for low-resistivity substrates.

The coplanar line CPW consists of a center conductor width W and a ground plane located on each side and spaced by a distance G . It is separated from the silicon substrate by a dielectric of thickness h . The electric field is largely concentrated in the RF line and the ground plane but a part penetrates into the substrate. Bridges arranged at regular intervals help ensure that the ground plane is homogeneous. This type of line is extremely sensitive to the resistivity of the substrate. However, a wide range of characteristic impedances can be achieved.

The choice of transmission line depends on the constraints of the targeted application. In our work, the two types are efficient. The loss in the TL is not a big matter; it can be easily calibrated with the coupler ratio. Due to simplicity, a microstrip line is chosen. The signal is on the LB layer, and the ground plane is built on the Metal-1 connected to the RF PADS ground. The needed length to occupy the phase shift is very high (5mm), but to save area, the TL is drawn in a shape of rectangular zigzag as shown in Figure 3-27.

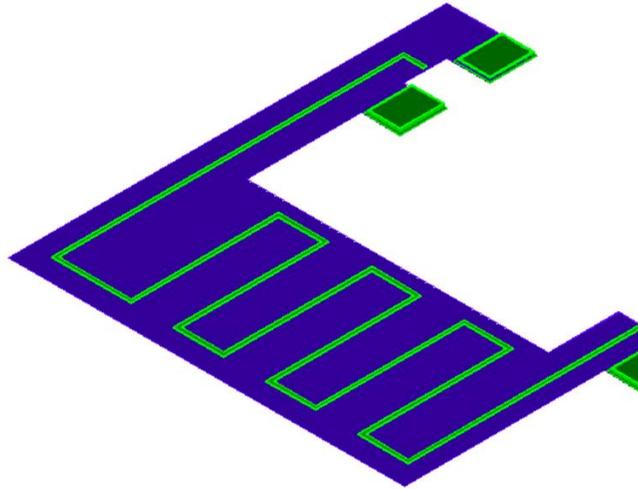


Figure 3-27. Phase Shifter TL

3.6 Overall Architecture Simulated Results

Finally, the oscillator system can be created. The layout of the overall architecture is shown in Figure 3-28. The area with the RF and DC PADS is around 1mm².

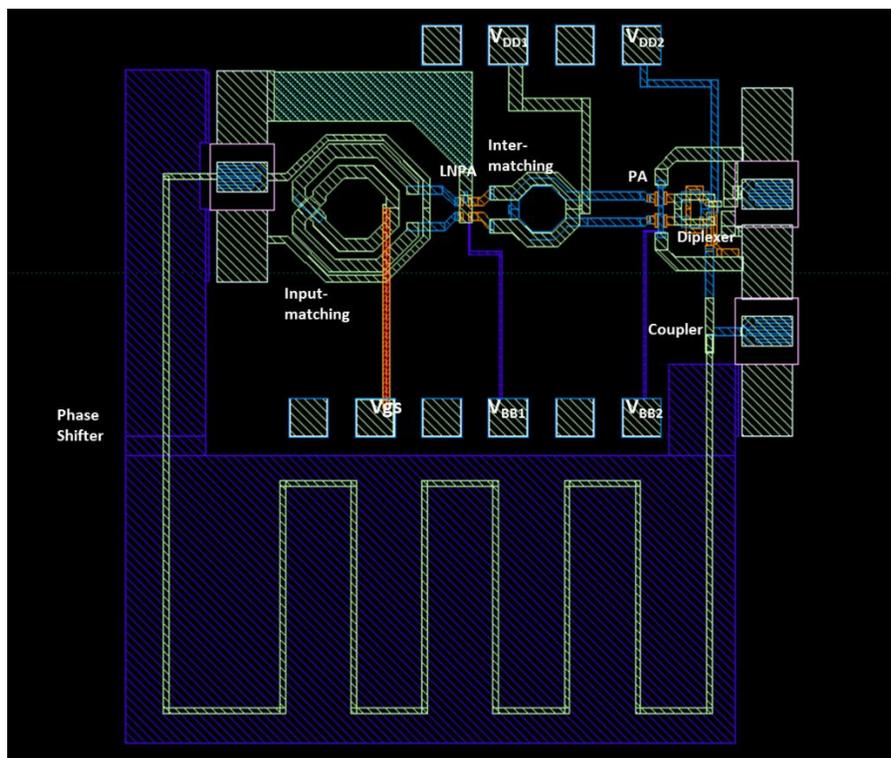


Figure 3-28. HFMO Layout

The phase noise and the output power parameters are to be studied. There are two analysis that can simulate the oscillator and detect the values of the phase noise; the periodic steady state (PSS) using the shooting method, and the harmonic balance (HB). The PSS is preferred for the strongly nonlinear and switching circuit as ring oscillator, while the harmonic balance is preferred for the nonlinear circuits as amplifiers, which our oscillator system is based on. The initial condition is set at the feedback of the circuit. A long transient time is given for the oscillator (60 ns) to enter deeply in the steady state as shown in Figure 3-29. The isolation between the two output ports is around 30 dB, but since the fundamental power is 13.3 dBm then the effective isolation will decrease showing little fundamental voltage in the third harmonic waveform shape.

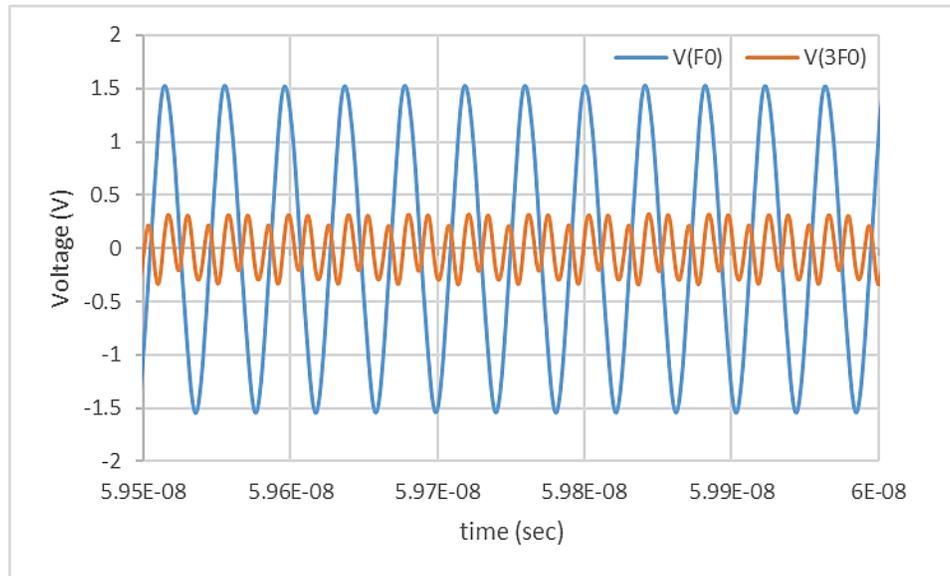


Figure 3-29. HFMO Voltages Waveform

The detectable fundamental and third harmonic oscillating frequency are 24.937 GHz and 74.811 GHz. The phase noise of both signals shows a big enhancement in the mm-wave band as shown in Figure 3-30. The phase noise and the output power of the fundamental signal are -127.7 dBc/Hz at 1 MHz offset and 13.3 dBm; thanks to the 16 dB coupler that decrease the pulling effects. The phase noise and the output power of the third harmonic signal are -130.5 dBc/Hz at 1 MHz offset and 4 dBm; thanks to the integrated diplexer that decreases the pulling effects and isolates the oscillating frequency from the feedback path. To show the strength of the proposed methodology, the load impedance will be varied at the different output ports to simulate the effect of VSWR on Antenna. Usually, when the VSWR is 1:2, it means that the impedance is between 25 Ω and 100 Ω , which is said as poorly matched. No studies are found which calculate the Antenna VSWR affected from obstacles or magnetic components in mm-wave band, however we will take an extreme case, which is VSWR 1:7, which means that the load resistance is between 7 Ω and 350 Ω instead of 50 Ω .

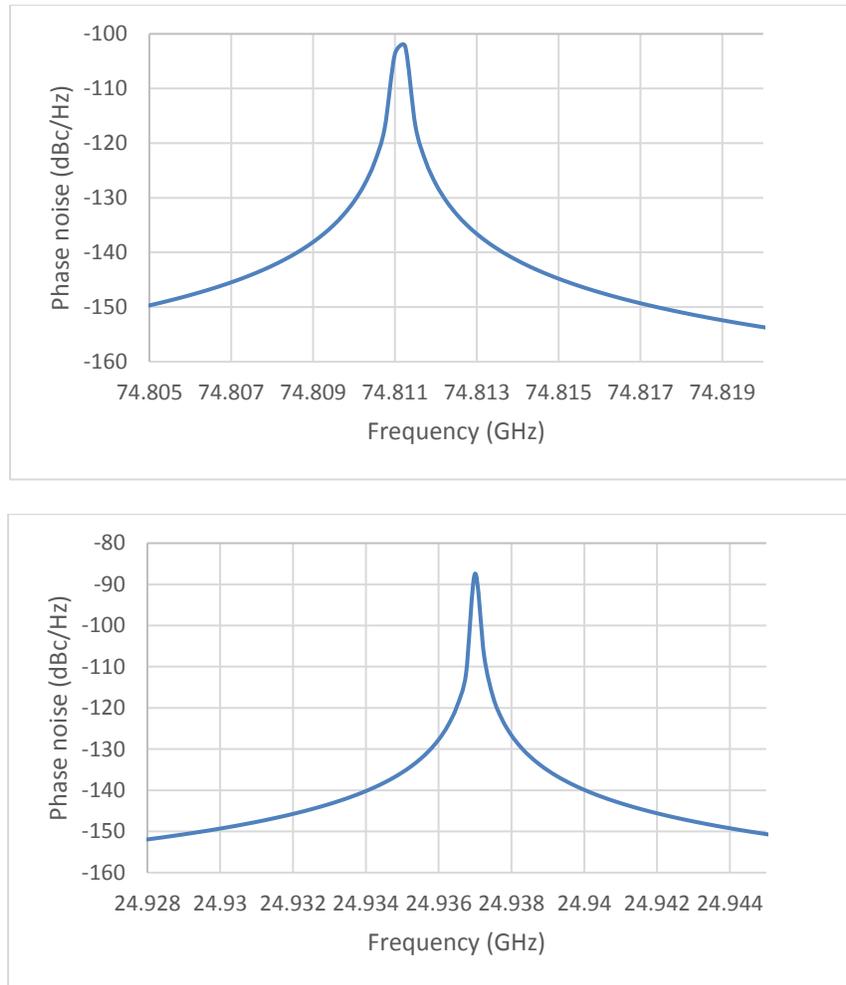


Figure 3-30. HFMO Phase Noise

The results are shown in Table 3-5. It shows a strong immunity of the third harmonic oscillator using the diplexer against the pulling effects and load impedance variation. The Δf is only 0.02% and 0.145% with at 7Ω and 350Ω respectively. It shows an improvement over the harmonic feedback oscillator introduced in chapter 1 (second harmonic oscillator); at same load impedance, the HFMO is 0.02% instead of 0.33% and 0.148% instead of 1% knowing that the oscillating frequency in this work is very high (75 GHz) instead of 5.8 GHz. The two works shows a strength of harmonic oscillators to face the pulling effects and the load impedance variation. The second improvement is for the fundamental chain in the HFMO due to the usage of the 16 dB coupler that attenuates the injection current. It shows only 2% frequency drift at 25 GHz, where the same load impedance in Fundamental feedback oscillator was 5%. Attention should be take care at the fundamental load port, if the impedance is too high, the gate voltage of the transistor in the PA block can hit the breakdown voltage (1.3 V), and if the impedance is too low, the output

power will decrease so that the oscillation can attenuates. The solution to face this problem is to use a reconfigurable coupler.

Table 3-5. Load Impedance Variation Test

R_L (Ω)	Osc Frequency (GHz)	Phase noise (dBc/Hz) @ 1MHz	Output Power (dBm)	Δf (%)
50 at both	74.811	-130.5	4	--
	24.937	-127.7	13.3	--
7 @ Port _{3F0}	74.794	-118	-1.61	0.02
	24.931	-126	13.3	0.02
350 @ Port _{3F0}	74.923	-120	2.35	0.145
	24.974	-103	12.18	0.148
350 @ Port _{F0}	73.254	-105	6.7	2.08
	24.418	-126	11.55	2.08

A state of arts is done for other types of oscillator as PLL using VCO, which are widely used in mm-wave band, with the HFMO. The Table 3-6 is about two desired frequencies. In the 75 GHz region, this work show a clearly difference in the phase noise; all of other works did not achieve lower than -90 dBc/Hz at 1 MHz offset, then they mentioned the 10 MHz offset. Even that, our work has the best phase noise and the highest power (4 dBm). The same idea is for the 25 GHz region; our work has the best phase noise and the highest output power with 13.3 dBm. The weakness of our work when it is compared with others is that there is no control to tune the frequency range; it is fixed over the F_0 and $3F_0$. The idea can be developed in the future to design tunable matching circuits to have a tuning range as other oscillators. Noted that the results of the oscillator obtained are post layout simulation, where the circuit are not fabricated yet.

Table 3-6. Oscillators State of Arts

Reference	CMOS Technology (nm)	F_{osc} (GHz)	Tuning Range (GHz)	Phase Noise (dBc/Hz)		P_{out} (dBm)
[13] measured	130	59	5.8	-89@1MHz	--	-18
[14] measured	65	73.8	32	--	-105@10MHz	-20
[15] measured	65	76.5	4.8	--	-109@10MHz	--
[16] measured	65	76.5	10.6	--	-108@10MHz	--
[17] measured	28	71.4	9.8	-93@1MHz	-114@10MHz	--
		76.1			-117@10MHz	--

This work: PLS simulation	28 FD-SOI	74.811	--	-130@1MHz	-155@10MHz	4
[18] measured	65	25	7.6	--	-123@10MHz -115@10MHz	-16
[19] measured	40 (LP)	23	3.7	-102@1MHz	--	--
[20] measured	28	25	11.1	-103@1MHz	-125@10MHz	-6.55
This work PLS simulation	28 FD-SOI	24.937	--	-128@1MHz	-153@10MHz	13.3

3.7 References

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Chapter 4 Conclusion

The CSH team in the IMS Lab worked on designing power oscillator using the fundamental feedback oscillator, then they developed the idea to design harmonic feedback oscillator. It shows an improvement on the phase noise, against pulling effect, and against load variation effects. It was designed on PCB at little GHz frequency. The idea of the work is to continue this work showing its performance as it is built on chip. The target application was the 5G network.

In Chapter one, an overview of mobile technology is introduced, beginning from the theory ideas of wireless communication until the fourth generation used in our days. Then, a brief explanation of the fifth generation is introduced showing its goals, services, capabilities, and discuss the frequency candidates at mm wave bands, in order to show a vision how the 5G will be. The flow is deepen to the transmitter architectures used in mm wave band then to the oscillator block. In the oscillator part, it explains the principle of noise generation and noise sources in electronic circuits and in semiconductors, then a model is shown for the phase noise according to Leeson model. The oscillators VCOs were branched to LC types. Each type is provided with real examples, and measurement values, in order study the performances of each technique used. A state of arts were labeled for each type. Then the idea of fundamental feedback oscillators is explained showing its drawbacks and compare it with the enhanced edition of that which is the harmonic feedback oscillator. The HFO shows an improvement on phase noise, frequency-pulling effects, and on behavior with load impedance variation. Then a new topology is introduced to study it in the work, which is the harmonic feedback multi-oscillator, showing its improvements over the FFO and the HFO. It shifts the design to higher level as working on third harmonic signals and benefits from the fundamental power signal to have multiple output; thanks to the differential amplifiers architecture. The desired frequencies were the 25 GHz and the 75 GHz as both are candidates to 5G application. In addition, the technology kit chosen is the 28 nm FD-SOI CMOS from STMicroelectronics.

In Chapter 2, it is divided into three titles: bulk CMOS limitation and alternative transistors, power amplifier, and low noise amplifier.

In part one, it provides an overview of the challenges faced by conventional CMOS scaling. It explains fully depleted devices, such as planar UTBB FD-SOI and Tri-Gate FinFET, as the alternative solutions of bulk transistors at 28-nm and beyond, shedding the light on their designs and performances. Then, a comparison is made between the two alternative transistors comparing their physical properties, electrical properties, and their preferences in different fields and applications.

In part two, the characteristic of the power amplifier are explained as gain, efficiency, and linearity. Then it discusses briefly the architectures and the topologies of PA, which are single

ended (common source with cascade), differential, and balanced. Then it passes to the classes of the PA, it differentiates them as sinusoidal classes and switching classes. Each class is explained showing the difference of biasing signal, and output current. It discusses the size of transistor and effects of interconnection layout parasitic. Then the class J is introduced and compared with class AB. A comparison is made and the theoretical effectiveness of Class-J topology for single stage large signal amplification is simulated. Moreover, two distinct transistors - widths of 250 μm and 350 μm - are simulated where each has its own topology in order to study the impact of increasing the width on the performance of the PA. As a result, Class-J PA design and its analysis show an improvement in output power, power gain, PAE, and bandwidth over than that of Class-AB. The result matches the one mentioned in the theoretical approach. Then it discusses briefly the stability conditions and analysis in small signal and large signal, showing the stabilization techniques used in amplifiers design. A new study is done about a new stabilization technique for the common source amplifier, showing its result on improving the stability, reverse isolation, and gain over the conventional common source and over the conventional stabilization techniques as RC shunt feedback.

The optimum load impedance is also discussed to show the difference between the conjugate matching, graphical method, and load-pull analysis. Then a PA state of arts are listed and discussed briefly showing the results and performances achieved at the most advance nodes of CMOS technology. Then the noise figure is defined and explained, showing its effects on the overall system noise.

The last part introduced the design of the harmonic feedback multi-oscillator HFMO using the 28nm FD-SOI technology. The proposed oscillator system consists of LNPA, PA, Diplexer, and Phase Shifter blocks, where each block has its own architecture and specification.

In chapter 3, each block in the oscillator system is introduced alone. The first part presents the BEOL of the kit technology showing its layers, and then it passes to the design of the RF Pads showing its characteristics and its parasitic RLC calculations. The integrated transformers parameters are shown, which the matching circuits in the differential architecture are based on.

The second part shows the design of the variable gain LNPA circuits and layout. The results of small and large signals are shown at different body bias voltages. Moreover, a state of arts is done showing its advantage as lowest noise figure in LNAs and high FoM as PA.

The third part shows the power amplifier; the core block in the oscillator idea, which is responsible of generating the fundamental, and the third harmonic power signals. The proposed transistor layout is designed, and a new topology of diplexer is introduced as an output matching circuit. It is based on integrated transformers. It filters the two output signals with high isolation.

The coupler and the phase shifter are designed according to capacitor divider coupler and the transmission lines delay line respectively.

Finally, the oscillator complete block is simulated showing its performance of output power and phase noise. It is tested under load impedance variation. An oscillator state of arts at 25 GHz and 75 GHz was made. Our work shows the best phase noise over the two frequencies. The third harmonic shows a big strength against the pulling effects and load impedance variation, which is better than that of the previous HFO (based on second harmonic). The same was for the fundamental chain over the previous FFO. Thus, the HFMO topology proposed in this work succeed in getting benefits from the fundamental and third harmonic signals, enhancing them, and achieving high performances.

The strength of the HFMO architecture is integrated with the advantages of the 28 nm UTBB FD-SOI specification that leads to the results achieved in this work, where the results are encouraging for fabrication.

The phase noise achieved in HFMO architecture is clearly enhanced over the phase noise measured in VCO, and as the frequency of application is higher, the differences in phase noise values will be wider, due to the degraded quality factor of the inductor. However, the use of VCO, PLL, mixer, and then PA in a transceiver chain can achieve higher output power, because the PA block will focus on fundamental signal only. In addition, the use of 28 nm UTBB FD-SOI limits the output power because of the low supply voltage and the low breakdown voltage, where the breakdown is only 1.3 V (0.2 V higher than saturated voltage). The usage of higher scale transistor will increases the output power on both frequencies fundamental and third harmonic. Moreover, the transistor will be capable to hold higher gate voltage, and the region between saturation voltage and breakdown voltage will be wider. Then working in this region will generate higher third harmonic output power.

Another advantage of oscillators using VCO is the tuning range; every oscillator has a tuning range for the frequency of oscillation. The HFMO can be developed to have a tuning range by working on the matching networks; every transformer can be connected in parallel to a varactor, the capacitance of the varactor can tune the frequency of matching. The varactor is controlled by voltage and it may needs more than one varactor. So that, the fundamental oscillating frequency will change as that of third harmonic frequency.

The working on second harmonic or third harmonic to achieve higher performances depends on the power amplifier architecture. First, the second harmonic can be generated on common mode single end PA. However, the loss of interconnections in the layout degrades the output power of fundamental and second harmonic signals. On the other side, the differential architecture boosts the output power of the fundamental and third harmonic signals, and enhance

the noise figure. Second, the third harmonic has better immunity than the second harmonic towards the frequency pulling effects. These causes implies the preference of using third harmonic architecture.

List of Publications:

Journals:

1. **Mohsen, A.**, Harb, A., Deltimple, N. and Serhane, A. (2017) 28-nm UTBB FD-SOI vs. 22-nm Tri-Gate FinFET Review: A Designer Guide—Part I. *Circuits and Systems* , 8, 93-110. <https://doi.org/10.4236/cs.2017.84006>.
2. **Mohsen, A.**, Harb, A., Deltimple, N. and Serhane, A. (2017) 28-nm UTBB FD-SOI vs. 22-nm Tri-Gate FinFET Review: A Designer Guide—Part II. *Circuits and Systems* , 8, 111-121.
3. **Ali Mohsen**, Mohammad Jaafar Ayoub, Mostafa Alloush, **Adnan Harb**, Nathalie Deltimple, Abraham Serhane, "Common source power amplifier design for 5G application in 28-nm UTBB FD-SOI technology", *International Journal of Electronics and Communications*, Volume 96, November 2018, Pages 273-278, <https://doi.org/10.1016/j.aeue.2018.09.029>
4. Mouhammad Abou Chahine, Hussein Bazzi, **Ali Mohsen**, Adnan Harb, Abdallah Kassem, "A low-noise voltage-controlled ring oscillator in 28-nm FDSOI technology for UWB applications", *International Journal of Electronics and Communications*, Volume 97, December 2018, Pages 94-101, <https://doi.org/10.1016/j.aeue.2018.10.003>
5. **Mohsen, A.**, Harb, A., Deltimple, N. and Serhane, A., "Low Noise Power Amplifier In 28-Nm Utbb Fdsoi Technology With Forward Body Bias", *International Journal of Digital Information and Wireless Communications (IJDIWC)*, Vol. 8, No. 2, 2018
6. **Mohsen, A.**, Harb, A., Deltimple, N. (to be submit) Variable Gain Differential Low Noise Power Amplifier in 28-nm FD-SOI

Conference Paper

1. Hussein Bazzi, Mouhamad S Abou Chahine , Mostafa Assaf, **Ali Mohsen**, and Adnan Harb, "A Low-Noise Voltage-Controlled Ring Oscillator in 28-nm FDSOI Technology", *IEEE ICM 2017*, 10 – 13 December 2017, Beirut, Lebanon
2. Mohamad Ayoub, Mustapha Alloush, **Ali Mohsen**, Adnan Harb, Nathalie Deltimple, and Ibrahim Serhan, "Class AB vs. Class J 5G Power Amplifier in 28-nm UTBB FD-SOI Technology for High Efficiency Operation", *IEEE ICM 2017*, 10 – 13 December 2017, Beirut, Lebanon