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Thanh-Toan Pham

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et de l'école doctorale : **Electronique, Electrotechnique, Automatique & Traitement du Signal (EEATS)**

Mastering the O-diamond/Al2O3 interface for unipolar boron doped diamond field effect transistor

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Introduction

Nowadays, global warming effect is becoming one of the most challenging issue for the human beings. In order to deal with this issue, many propositions were suggested. Most of them are dealing with the energy crisis, especially electricity. In fact, the amount of electricity needs to supply the demand of more than 6 billion people on earth is tremendous. The main electricity suppliers are coming from "traditional energy" sources like thermal power, nuclear power, hydroelectricity power, etc.. Most of the mentioned power sources are dangerous and/or potentially dangerous for nature and human beings. Therefore, a "greener energy" is highly desired. "Greener energy" has two fold meanings: on one hand, it uses renewable energy sources like solar power, wind power or geothermal energy instead of traditional energy sources, and on the other hand, using the electricity more efficiently. A recent report has pointed out that the energy loss in US is about 10 %, more than the sum of all renewable energy generated in US. Therefore, an effective use of electricity and a limitation of the waste are critical.

Unfortunately, losses are endemic in semiconductor components, the central devices of all power conversion systems. Indeed, most of semiconductor components are fabricated on Silicon (Si), a semiconductor that has reached its physical limits. Even if the new architectures can push Si devices beyond their physical limits, this approach will not provide a long term solution. Therefore, the emergence of new semiconductors with superior physical properties is highly desired for next generation of power electronics. Wide band-gap semiconductors such as silicon carbide (SiC), III-Nitride, gallium oxide (Ga_2O_3) and diamond are promising materials to fabricate devices, exhibiting low loss in the on-state regime and high breakdown voltages in reverse regime. Among them, diamond is the ultimate semiconductor for power devices due to its superior physical properties. Recent progresses on diamond substrates that includes homoepitaxial growth, controlled doping and fabrication processing permits to consider diamond power devices, e.g. Metal Oxide Semiconductor Field Effect Transistors (MOSFET). However,up to now, most of diamond MOSFETs were realized by controlling the two dimensional hole gas (2DHG) on the hydrogen terminated diamond surface. Even though these devices are interesting, their working principle is based on uncertain quantities (trap states in the oxide) and bearing itself the demerits (see further discussion in the thesis).

In order to realize a diamond MOSFET by controlling diamond semiconductor, numerous issues must be overcome. Diamond is a wide bandgap semiconductor which does not have a native oxide layer, find an appropriate candidate for the gate oxide on diamond MOSFET is challenging. The two most important criteria for the gate oxide choice are: i) barrier heights for electrons and/or holes at the diamond/oxide interface in order to ensure a low leakage current from the transistor channel to the gate metal, ii) low density of trapped charges at the diamond/oxide interface and/or in the oxide in order to obtain an efficient Fermi level control from the gate electrode bias. In this context, Chicot et al. [22] have introduced the O-diamond/Al_2O_3 MOSCAP test devices. Marechal et al. [24] measured the type I band alignment at the O-diamond/Al_2O_3 interface, which is favorable to realize both inversion and depletion MOSFETs. This PhD project is a continuation of the two previously mentioned thesis. It includes two main objectives: 1.

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fundamental investigations dedicated to the electrical characteristics of an O-diamond MOS capacitor test device; 2. From understanding MOSCAP test devices to realize an unipolar diamond MOSFET by controlling the diamond semiconductor epilayer. The thesis will include three chapters:

- In Chapter 1, we will discuss the losses of a semiconductor switch in power converter systems and the importance of wide bandgap semiconductors to reduce losses. The comparison between wide bandgap semiconductors by means of Figure-of-Merit (FOM) is followed to demonstrate the superiority of diamond. We will then present in details the important physical properties of diamond for power devices. State-of-the-art of diamond devices will be reviewed. As an introduction for the MOSFET device, we will introduce the working principle of an ideal MOSCAP test device. State-of-the-art of O-diamond MOSCAP test devices will be described. Finally, the chapter will conclude on the purpose of the thesis.

- Chapter 2 will be dedicated to the fundamental of understanding the O-diamond MOS capacitor test device. This chapter will include three parts:

  Part 1: We will firstly address the methodology issues related to diamond growth, fabrication processing, electrical characterization and the reliable issue related to a correct C-V measurements. From correct C-V measurements, we will evaluate different crucial information of a O-Diamond MOS capacitor such as charges components, semiconductor surface potential and space charge region variation with gate potential. High frequency-capacitance method is applied to quantify the interface states density. Electrostatics model based on different charge components will be built. Electrostatics band diagram will be then introduced and the limit of this model will be addressed.

  Part 2: We discuss the origin of leakage currents and capacitance-frequency dependent when O-diamond MOS capacitor is biased in negative potential. We will quantify the interface states density at the O-diamond/Al_2O_3 interface using conductance method. With new interface states density, a complete electrostatics model for O-diamond/Al_2O_3 MOSCAP will be proposed.

  Part 3: We correlate the substrate imperfection versus the electrical characteristics of the O-diamond MOS capacitor. We will discuss the origin of leakage current and the capacitance-frequency dependence when the O-diamond MOS capacitor is biased in positive potential.

- Chapter 3 will introduce our first approach to realize a depletion mode diamond MOSFET. We will firstly address different technical issues related to design, fabrication, measurements and simulation. Then, the combined electrical measurements, analysis and simulation on the diamond MOSFETs and test devices (TLM, MOS capacitor) fabricated on the same sample will be presented. Important parameters of the transistor such as contact resistance and carriers mobility will be quantified. The results on OFF state measurement, simulation and analysis will also be presented. The benchmarking of the device and the projection toward device improvement will be described. Finally, the thesis will be concluded.

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Chapter 1

Boron doped diamond semiconductor for unipolar power devices

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Nowadays, electricity is ubiquitous in our daily life. As shown in Fig. 1.1, human beings are now dealing with a wide range of energy, ranging from kW in some power suppliers to few GW in the grid energy transmission and distribution.

Basically, electricity exists in two forms: Direct Current (DC) and Alternating Current (AC). From the generation at power station to the transmission and delivery to home and electrical devices, electricity is necessary stepping up and stepping down as well as switching between two forms. Therefore, electrical conversion and amplification/attenuation are very important. Figure 1.2 represents the basics electrical circuit of a non isolated DC-DC boost converter (Fig. 1.2a) and a non isolated DC-DC buck converter (Fig. 1.2b). As shown in Fig. 1.2, power devices are the heart of the power converter systems (transistor and diode). Solid state switches like transistors, since being invented in 1947 [25], have replaced vacuum tube in every applications. These devices are critical in any power converter and power system.

In power electronics and power converters, power devices are used in switch mode, switching between two states and targeting the operating regimes with negligible losses: ON-state and OFF-state. Ideally, in the ON-state, the device is working like a conductor and the resistance of the device is 0 (Ω). In the OFF-state, the device is completely isolated and the resistance of the device is infinite.

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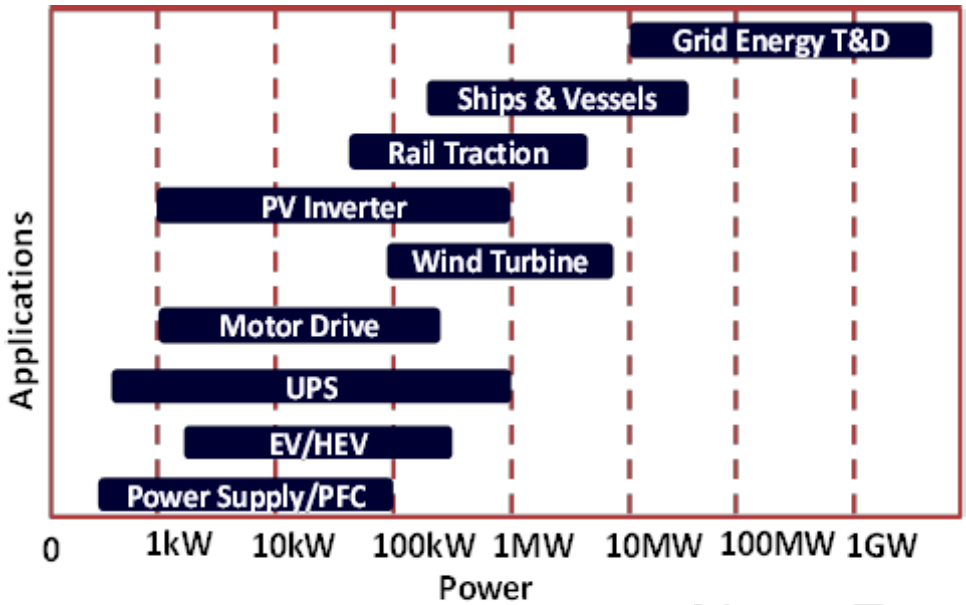

Figure 1.1: Power range requirements of various applications (chart is based on Yole Development report).

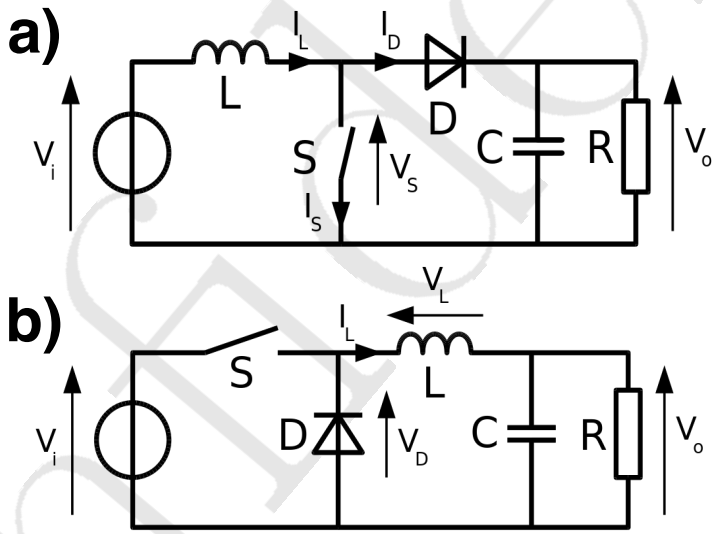

Figure 1.2: Electrical circuit of the power converter a) DC-DC boost converter; b) DC-DC buck converter.

However, as shown in Fig. 1.3, losses in the ON-state (resistance) are endemic for all power devices. There are two typical losses (resistances): loss of the drift region ($R_{on} = \frac{dV}{dI}$) and loss of the device (R - that may include threshold voltage in this case), as shown in Fig. 1.3. A consequence of loss is the heat dissipation and global efficiency reduction. Considering the huge numbers of electrical and electronic devices on the earth, it is indeed significantly contributing to the global warming effect. Conductivity of a material is the most important factor which determines the ON-state current.

In the OFF-state, breakdown voltage is unavoidable and is a design parameter. Breakdown voltage of a device is defined as a voltage in the OFF-state where the sudden onset

current is observed, with application-dependent quantitative leakage current values (leakage current density or leakage current per gate width, breakdown voltage derating and safe operating area). The reverse voltage blocking capability of a device is either dependent on the nature of materials as well as the designs of power devices.

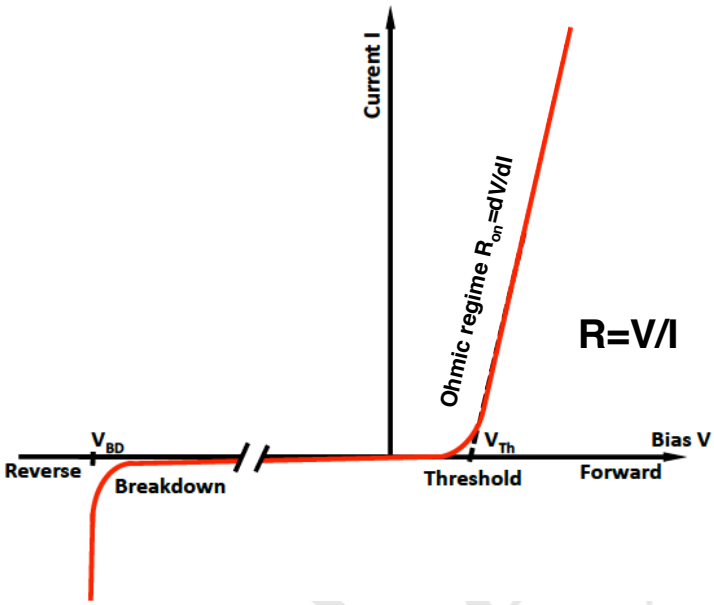

Figure 1.3: Typical electrical characteristic of simple power device (diode) where the loss in the ON-state and breakdown in the OFF-state are unavoidable.

For a long time, Silicon (Si) transistors are the workhorse of the electronics and electrical industry. However, the loss of state-of-the-art Si power devices has been demonstrated much higher compared to wide bandgap power devices [1]. Si is a low critical electric field material (0.3 MV/cm for 100V-400V devices) due to its narrow bandgap nature (1.1 eV) compared to other wide bandgap semiconductors. Even if novel designs push devices performance beyond its physical limits, Si will not provide a long term solution.

The emergence of new semiconductors is urgent. Wide bandgap semiconductor such as III-Nitride, Silicon Carbide (commercialized) and diamond are now considered as the solution for next generation power devices.

In order to evaluate the potential of semiconductors, Figure of Merits (FOMs) [26, 27, 1] are usually used as the mean. There are generally two kinds of FOMs: material FOMs to evaluate a material and device FOMs to evaluate the designs of the devices.

1.1 Unipolar device's Figure-of-Merit(FOM)

Considering the ideal switching waveforms of a power MOSFET (Fig. 1.4), losses of an unipolar switch without taking into account the circuit operation, can be expressed by using the following equation [1]:

$$P_{loss} \approx I_{rms}^2 R_{on} + V_D I_D \left(t_r + t_f\right) f \tag{1.1}$$

[1] http://www.mitsubishielectric.com/news/2013/pdf/0326-a.pdf

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The first term represents the DC conduction loss. The second term represents the switching loss, which is depending on the switching frequency.

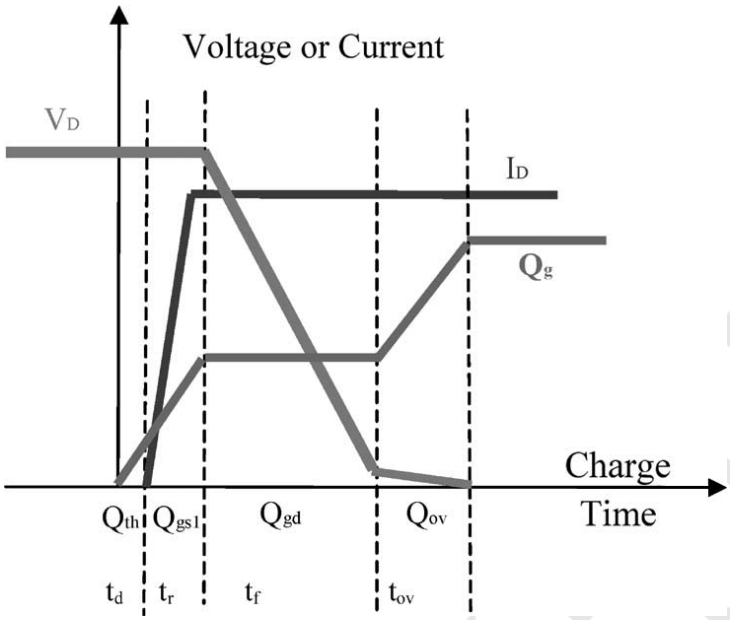

Figure 1.4: Switching waveforms of a generic unipolar power device. Courtesy of Huang et al. [1].

In conduction loss, the most important part is the ON-resistance R_{on} (in case built-in potential is neglected). For an ideal uniformly doped drift region and abrupt junction in Non-Punch-Though (NPT) design (Figure 1.5), the ON-state resistance can be defined using the fundamental semiconductor equation:

$$R_{on} \times S = \left(\frac{W}{q\mu N_A}\right) \tag{1.2}$$

where S is the active surface of the device, W is the width of the drift region, $q \simeq 1.6 \times 10^{-19}$ C is the elementary charge, μ the carrier mobility and W and N_A are the thickness and doping concentration of the drift region, respectively. As a function of the breakdown voltage, the total ON-resistance can be splitted among different contributors other than drift region resistance (e.g. contact resistance, series resistance, heavily doped substrate, channel resistance, ...).

For a compromise between ON-state loss and OFF-state breakdown, the thickness and doping of the drift region must be optimized. Considering the OFF-state under reverse bias, a maximum voltage that can be supported by the drift region is estimated by the critical electric field E_c [27]. Once the maximum electric field in the structure reached the critical electric field of the material, devices will experience a breakdown due to avalanche effect.

Under breakdown conditions, depletion width is given by:

$$W = \frac{2BV}{E_c} \tag{1.3}$$

where BV is the breakdown voltage and E_c is the critical electric field.

The doping concentration in drift region required for a given breakdown voltage is:

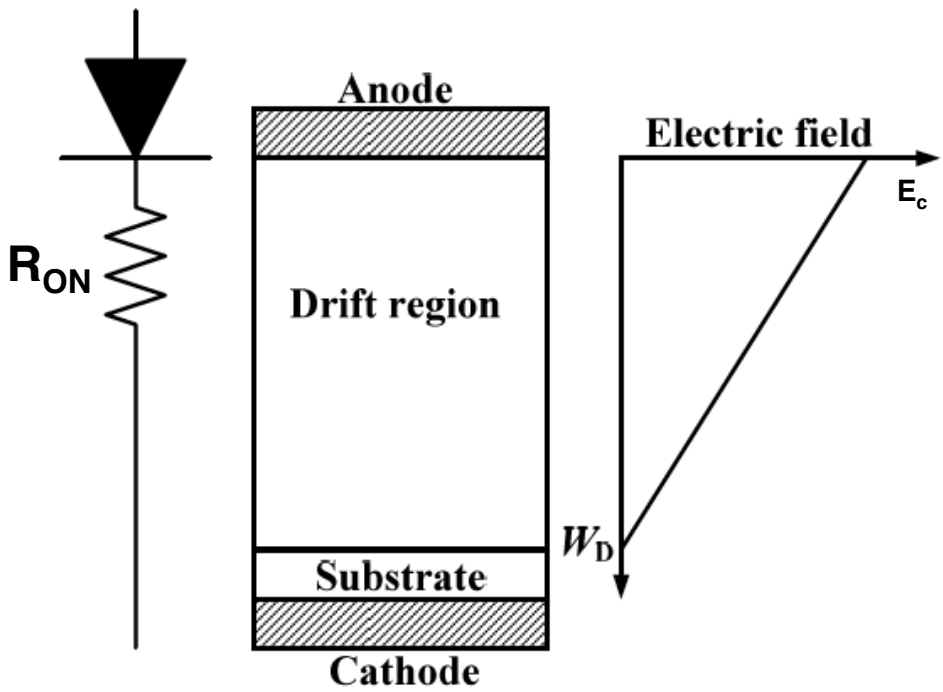

Figure 1.5: Ideal drift region in Non-Punch-Through (NPT) design that considering the compromise between ON-state loss and OFF-state breakdown, considering breakdown is due to avalanche effect when maximum electric field in the structure reached material critical electric field.

$$N_A = \frac{\varepsilon_{sc} E_c^2}{2qBV} \tag{1.4}$$

where ε_{sc} is the semiconductor dielectric constant. By combining the equations 1.2, 1.3 and 1.4, the ideal ON-resistance of the drift region is then expressed as:

$$R_{on} = \frac{4BV^2}{\varepsilon_{sc} \mu E_c^3} \tag{1.5}$$

The denominator is usually preferred as "Baliga material FOM (BMFOM)" [27], which has been derived by Baliga in 1983 as:

$$BMFOM = \varepsilon_{sc} \mu E_c^3 \tag{1.6}$$

In principle, semiconductors with higher BMFOM are expected to have a lower conduction losses. Also, materials with higher critical electric field are expected to have higher breakdown voltages than material with lower critical electric field in a same device design (doping concentration, device structure, etc.). However, there are some issues with BMFOM. Firstly, BMFOM is not taking into account the incomplete ionization of wide bandgap semiconductors, e.g. diamond. Therefore, BMFOM underestimates the ON-resistance of diamond devices at room temperature (RT). Second, the concept of using critical electric field for the comparison is not necessary correct. As shown by Raynaud et al. [28] and Chicot et al. [23], critical electric field is varying with doping concentration by integrating the impact ionization coefficients into the avalanche calculation [29].

The application of the avalanche breakdown condition must be discussed, as some power devices will be limited by other phenomena and never reach the avalanche breakdown (leakage current limit, dielectric breakdown, ...). Finally, BMFOM is correct only for the devices operating at low frequency where conduction loss is dominant. When the operating frequency is high, switching losses becomes important and BMFOM is no longer appropriate.

In order to take into account the switching losses, current rising time (t_r) and voltage falling time (t_f) in Fig. 1.4 were considered by Huang et al. [1]. The author also assumed that during the switching period of high power devices, the charging and discharging of gate-to-drain charge Q_{gd} dominate the switching loss, i.e. $t_f >> t_r$ [1]. The general power losses of equation 1.1 is then approximated by:

$$P_{loss} \approx I_{rms}^2 R_{on} + V_D I_D t_f f \tag{1.7}$$

with $t_f = \frac{Q_{gd}}{i_{g,avg}}$ where $I_{g,avg}$ is the gate current at the Miller Plateau and it can be controlled by the gate driver and gate resistors. Both ON-resistance and Q_{gd} are related to the area of the device by their specific value. Equation 1.7 can be rewritten by considering the area factor of the device as:

$$P_{loss} = \frac{I_{rms}^2 R_{on,sp}}{A} + \frac{V_D I_D f Q_{gd,sp} A}{i_{g,avg}} \tag{1.8}$$

Where $R_{on,sp}$ and $Q_{gd,sp}$ are the specific ON-resistance and specific gate-to-drain charge, respectively. By increasing device area, the first term decreases and the second term increases. Total power loss exhibits a minimum value at an area that:

$$\frac{dP}{dA} = 0 \tag{1.9}$$

Therefore

$$P_{loss,\min} = \left(2 I_{rms} \sqrt{\frac{V_D I_D f}{i_{g,av}}}\right) \left(\sqrt{R_{on,sp} Q_{gd,sp}}\right) \tag{1.10}$$

when the chip area is

$$A_{opt} = \frac{I_{rms}}{\sqrt{\frac{V_D I_D f}{i_{g,avg}}}} \sqrt{\frac{R_{on,sp}}{Q_{gd,sp}}} \tag{1.11}$$

A. Huang claimed that the first term of equation 1.10 is relating to circuit operating and the second term is relating to the device [1]. The second term is considered as the new "device FOM" named as "Huang's device FOM (HDFOM)" [1]:

$$HDFOM = \sqrt{R_{on} Q_{gd}} \tag{1.12}$$

where R_{on} is identical to the expression in equation 1.5. Q_{gd} is the gate-to-drain charge and usually known as Miller charge [1], and can be expressed as:

$$Q_{gd} = k \varepsilon E_D = k \sqrt{\frac{V_D}{V_B}} \varepsilon E_c \tag{1.13}$$

where V_D is the converter bus voltage, and I_D is the switch turn-on and turn-off current, E_D is the peak electric field when $V=V_D$, k represents the area ratio of the gate-to-drain overlap area over the whole chip area [1]. The HDFOM is related to material

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properties by the multiplication R_{on} in equation 1.5 and Q_{gd} in equation 1.13. The minimum loss in equation 1.11 is then expressed as:

$$P_{loss,\min} = \frac{\left\{4I_{rms}\left(V_B V_D\right)^{3/4}\sqrt{\frac{kI_D f}{i_{g,av}}}\right\}}{\left(E_c\sqrt{\mu}\right)} \tag{1.14}$$

The denominator is usually referred as "Huang's material FOM (HMFOM)" [1].

$$HMFOM = \left(E_c\sqrt{\mu}\right) \tag{1.15}$$

A material with higher HMFOM is expected to have a lower loss during operation compared to a material with lower HMFOM. Again, the concept of using critical electric field E_c for comparison is not necessary correct (E_c depends on the doping concentration of the drift layer).

Until now, as far as author's knowledge, these two FOMs are the most common FOMs to evaluate the strength of semiconductors for unipolar high power conversion device applications. Table 1.1 represents the physical parameters of main semiconductors for power devices (Si, SiC, GaN and diamond) and the corresponding material FOM values calculated by its corresponding authors [27, 1].

Property	Unit	Si	4-SiC	GaN	diamond
Bandgap	E_G [eV]	1.1	3.23	3.45	5.45
Dielectric constant	ε_{sc}	11.8	9.8	9	5.5
Breakdown field	E_c(MV/cm)	0.3	2	3-4	10
Thermal conductivity	λ [W/cm.K]	1.5	5	1.5	22
Sat. Drift velocity e-	$v_s[10^7$ cm/s]	1.0	2.0	2.2	2.7
Sat. Drift velocity h+	$v_s[10^7$ cm/s]	1.0			1.1
Electron mobility	μ_e[cm^2/V.s]	1500	1000	1250	1000
Hole mobility	μ_h[cm^2/V.s]	480	100	200	2000
BMFOM	[Si=1]	1	554	188	23017
HMFOM	[Si=1]	1	7.5	8	23.8

Table 1.1: Physical properties and FOMs value of main semiconductors for power device applications.

From these two FOMs, diamond is standing-out as the best semiconductor for unipolar power device applications.

The compromise between ON-resistance versus BV of different materials have also being calculated by Umezawa et al. [2], as shown in Fig. 1.6. This calculation shows that, for a given breakdown voltage at its best operating condition (250 °C), diamond can provide the lowest specific ON-resistance (lowest loss). It's based on the fact that all critical physical properties of diamond are outstanding compared to other semiconductors.

In the following sections, we will discuss in details the critical physical properties of diamond for power devices application. It is ranging from critical physical properties for ON-state current: doping, carriers density and carriers mobility and critical physical properties for OFF-state breakdown voltage: maximum electric field.

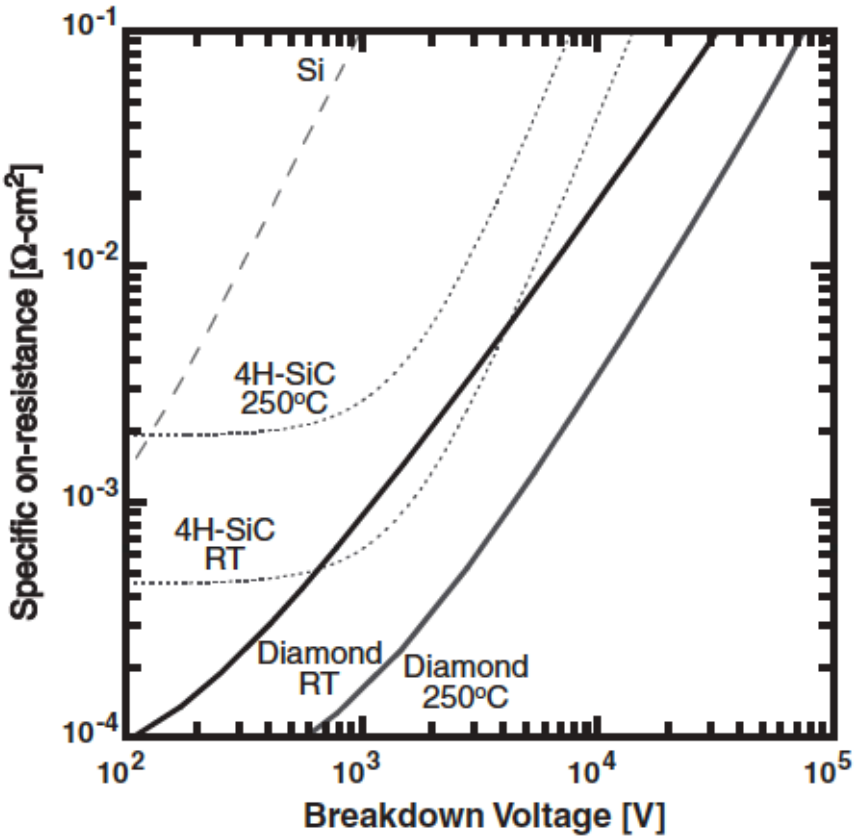

Figure 1.6: ON-resistance and breakdown voltage of different semiconductor at RT and at 250 °C, courtesy of Umezawa et al.[2].

1.2 Diamond semiconductor for power devices

As shown in the previous section, the ON-resistance is the most important parameter which determines the loss of device. ON-resistance is basically including two parts: material resistance and contact resistance. Material resistance is specified by its resistivity, which is defined as:

$$\rho = \frac{1}{qp\mu} \tag{1.16}$$

where p is the free carrier concentration and μ is the carrier mobility. In order to idealize material resistance, both p and μ must be optimized. Free carriers concentration is controlled by the doping, while mobility is depending on the nature of material and different scattering mechanism including doping effect.

1.2.1 Doping

Due to the wide bandgap nature (5.5 eV), diamond was considered as an insulator and had been used as a gate insulator for Field Effect Transistors (FET) [30]. To be considered as semiconductor, diamond must be doped. The concept of diamond doping can be categorized into two main directions: surface doping and bulk doping.

1.2.1.1 Surface doping

Surface transfer doping is considered as a novel doping concept in some semiconductors [31]. This concept is widely used to interpret the surface conductivity of hydrogen terminated diamond (H-diamond) [3, 32]. Figure 1.7 represents the basic idea of surface transfer doping concept in H-diamond. This concept can be understood as: When a di-

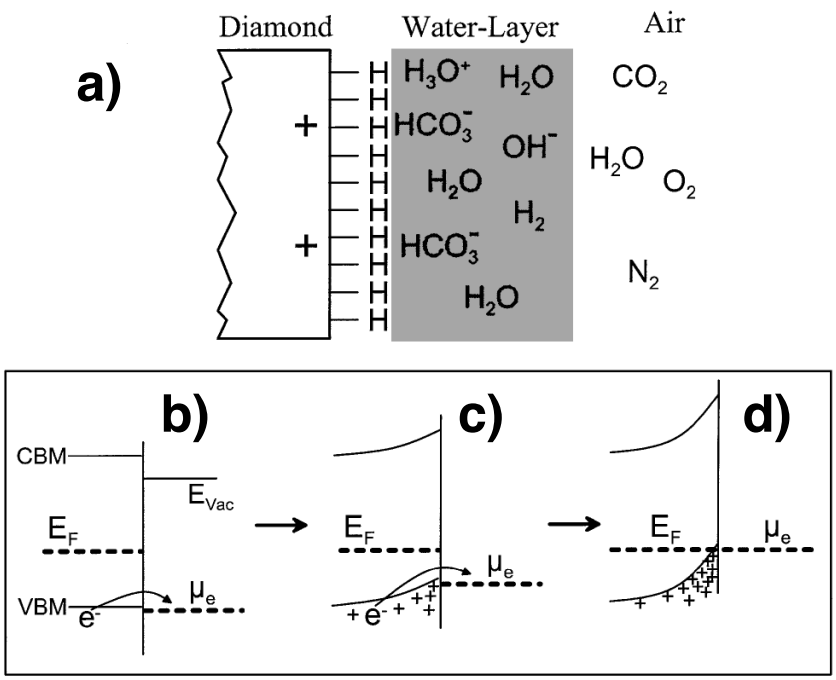

Figure 1.7: Schematic description of surface doping model in H-diamond. Courtesy of Maier et al. [3].

amond layer is terminated by hydrogen, the conduction band is above the vacuum level. Chemical potential is also rigidly moved up. Consequently, H-diamond is a negative electron affinity semiconductor with a relatively high chemical potential (Fig. 1.7b) [33]. In principle, any substance that has a lower chemical potential than diamond and located at diamond surface will attract the electrons from diamond [3, 34]. Naturally, H-diamond surface exposed to the air will condensate a thin water layer (Fig. 1.7a). This thin layer of water has a lower chemical potential than H-diamond. Therefore, electron inside diamond layer will transfer to the diamond surface and the water layer to equilibrate the chemical potential difference (Fig. 1.7c). The electron transfer leaves free hole with typical density of 10^{13} cm^{-2} in the valence band to be accumulated at the diamond surface (Fig. 1.7d). Therefore, once diamond surface is hydrogen terminated and being exposed to the air, diamond surface becomes conductive [3, 34]. This conductive surface will disappear when either the lower chemical potential substance disappear or the H-diamond surface disappear. As shown by Maier et al. [33] by changing diamond surface from H-diamond to oxygen terminated diamond (O-diamond), there are about 3 eV difference in terms of diamond electron affinity and the conductive diamond surface is disappeared.

The surface transfer doping is natural and somehow lack of controllability. Therefore, a more controllable doping method is required.

1.2.1.2 Bulk doping

As other materials in group IV (periodic table) like Si, diamond can be doped by group III elements or group V elements to control free carrier concentrations and the electrical properties. This doping method is challenge because it is required one manage both crystal grow epitaxially as well as dopant incorporation. The pioneer works on incorporating dopants into homoepitaxy diamond were mainly done in Japan [35, 36]. Since then, there are many efforts to investigate boron doped p-type diamond [36, 37, 38, 39, 40, 41, 42, 43, 44] and phosphorous (P) doped n-type diamond [35, 45, 46, 47, 48, 49]. One of the most challenging issue regarding diamond doping is the ionization energy of the dopant which is considerably deep. Figure 1.8a represents the ionization energies of different dopants in diamond. For n-type doped diamond, shallowest dopant is P (0.57 eV). For nitrogen doped diamond, dopant ionization energy is 1.7 eV. For p-type diamond, moderate boron doped diamond introduced a dopant ionization energy of 0.38 eV.

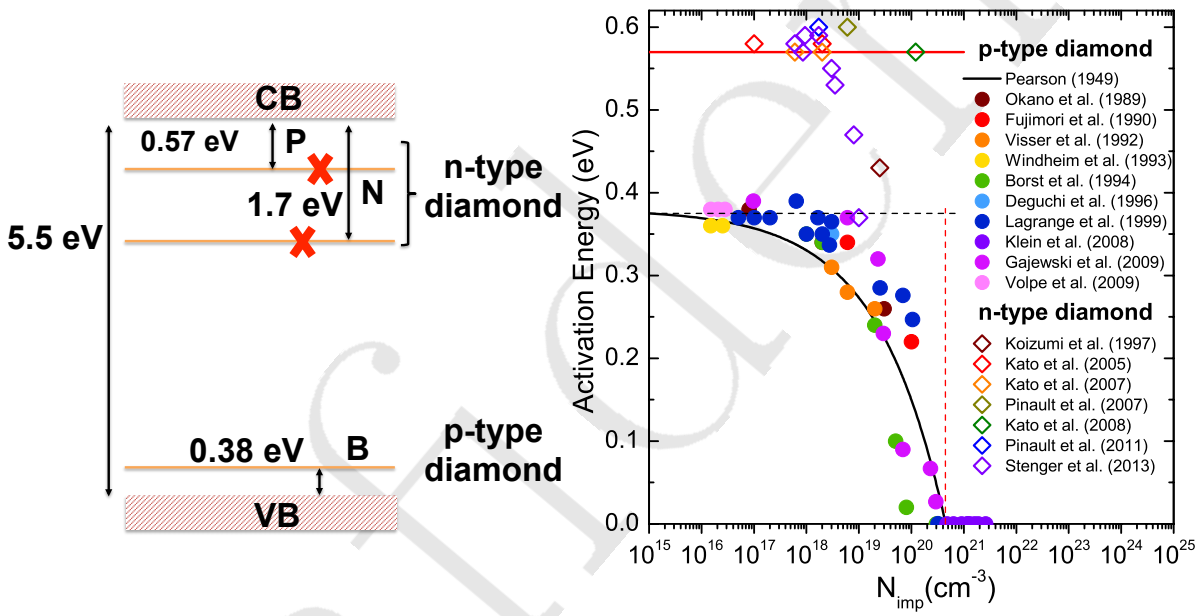

Figure 1.8: Ionization energy of dopants as a function of the impurity concentration in diamond. The experimental boron ionization energies are taken from the literature [Okano 1989, Fujimori 1990, Visser 1992, Windheim 1993, Borst 1995, Deguchi 1996, Lagrange 1999, Klein 2007, Gajewski 2009, Volpe 2009] and the solid curve is drawn after Pearson and Bardeen law [Pearson 1949]. Phosphorus ionization energies are taken from the literature [Koizumi 1997, Kato 2005, Kato 2007, Pinault 2007, Kato 2008, Pinault-Thaury 2011, Stenger 2013]. Its value is assumed to be constant over the entire doping range. Courtesy of Fiori's PhD thesis [4]

Since the dopant ionization of boron doped diamond is much lower compared to n-type diamond, the carriers ionization of p-type is also more effective than n-type diamond. In fact, the carrier activation also depends on doping concentration (N_A) as well as compensation concentration (N_D). As shown by Traore et al. [10], depending on compensation concentration, the ionization ratio of [B] dopant at RT can be ranging from 0.1% to 1% . Therefore, there are a small portion of [B] dopant which can contribute to the free

hole density in the valence band at RT. The activation ratio is significantly increased by raising the temperature to $T = 500$ K, as shown in Fig.1.9b. Therefore, a proper diamond device is expected to have a negative temperature effect (ON-state performance is improved with the increasing of temperature) in a certain range of temperature.

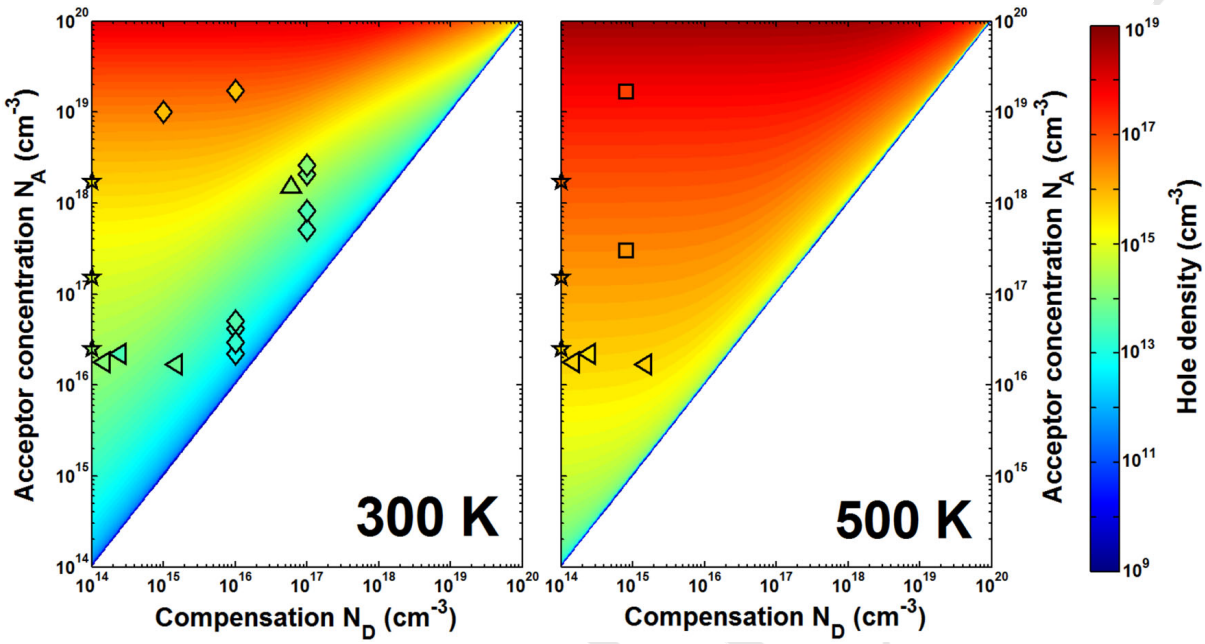

Figure 1.9: Theoretical hole density as function of acceptor concentration and compensation at 300 and 500 K. The symbols are experimental data reported by: Barjon et al. [5], Volpe et al. [6], Gabrysch et al. [7], Werner et al. [8], and Tsukioka et al. [9]. Courtesy of Traore et al. [10]

Another interesting feature of boron doped diamond is the dependence of ionization energy on doping concentration. As shown in Fig. 1.8b, boron ionization energy is varying from 0.38 eV for a doping concentration up to 10^{17} (cm^{-3}) to 0 eV for a doping concentration above $5{\times}10^{20}$ (cm^{-3}) [43]. This behavior is excellently fitted by the Pearson model [50] using the empirical law:

$$E_a\,(eV) = 0.38 - 4.7877 \times 10^{-8} \times N_A^{\frac{1}{3}} \tag{1.17}$$

Where E_a is the thermal ionization energy of boron acceptor and N_A is the boron doping concentration (cm^{-3}). The metallic regime ($N_A = 5 \times 10^{20} cm^{-3}$) is useful to reduce the series resistance in the test device or improve the device performance in punch-through (PT) design. Therefore, mastering a wide concentration range of boron doped diamond is very important for device optimization toward low ON-state loss, high OFF-state breakdown diamond power devices.

Regarding the low ON-state loss, along with carrier density, carrier mobility is equivalently important to determine the resistivity, as shown in equation 1.16.

1.2.2 Carrier mobility and density

Diamond is considered as an ultimate semiconductor partly due to its superior carriers mobility compared to other wide bandgap semiconductors. Pernot et al. [11] have shown

that due to the low optical phonon population, carriers mobility in diamond is elevated at RT. In ideal case, carrier mobility is controlled by lattice scattering and dopant scattering. As shown in Fig. 1.10, for a boron concentration around a few 10^{17} cm^{-3}, the hole mobility is controlled by lattice scattering and an optimal hole mobility as around 2000 cm$^2/V.s$ can be obtained [11]. This hole mobility is higher than the electron mobility of other semiconductor like Si ($\simeq$1500 cm$^2/V.s$), GaN ($\simeq$1250 cm$^2/V.s$) and 4-SiC ($\simeq$1000 cm$^2/V.s$). For a boron concentration larger than a few 10^{17} cm^{-3}, scattering from neutral impurities becomes more important. At boron concentration above 3×10^{18} (cm^{-3}), the scattering from neutral impurity becomes dominant. Once the scattering from neutral impurity is involved, hole mobility is strongly degraded [11]. Similarly, a maximum electron mobility of 1000 cm^2/V.s is determined for the low doped n-type diamond.[51].

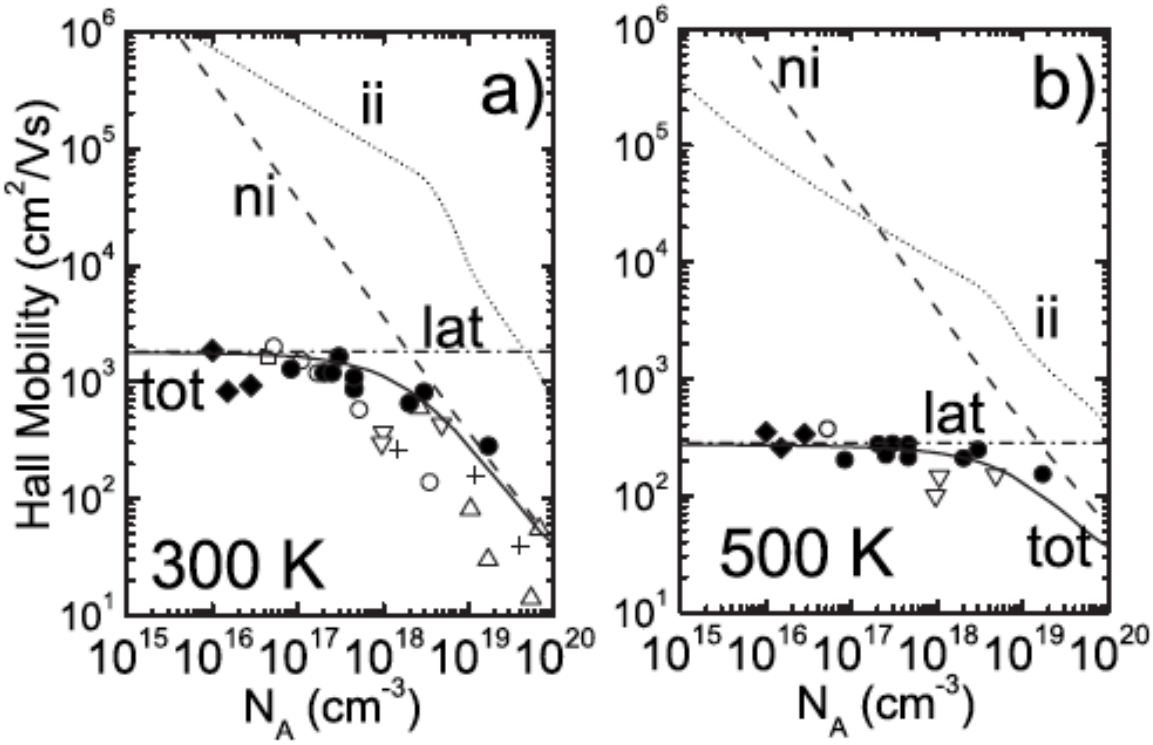

Figure 1.10: The dependence of hole mobility to boron concentration at a) 300 K; b) 500 K. Courtesy of Pernot et al. [11].

Free carriers density and carriers mobility at different doping concentration and temperatures can be calculated by using the model introduced in Volpe et al. [6] and Pernot et al. [11]. The free hole concentration is calculated by using the equation:

$$p = \frac{1}{2}\left(\phi_A + N_D\right)\left\{\left[1 + \frac{4\phi_A\left(N_A - N_D\right)}{\left(\phi_A + N_D\right)^2}\right]^{1/2} - 1\right\} \tag{1.18}$$

where $N_v = 2\left(2\pi m^* k\right)^{3/2}/h^3$ and $\phi_A = \left(g_1/g_0\right) N_v T^{3/2} \times \exp\left(\frac{-E_A}{kT}\right)$, k is the Boltzman constant. The degeneracy factor of boron is assumed to be $g_1/g_0 = 1/4$ and the average hole effective mass is $0.908m_0$. N_A is the doping concentration and N_D is the compensation concentration. More detailed parameters and approximations can be found in the corresponding references [6][11].

Hole mobility at different doping concentrations and temperatures, considering that only phonon scattering and dopant scattering can be calculated by [6][11]:

$$\mu\left(T, N_{imp}\right) = \mu\left(300, N_{imp}\right)\left(\frac{T}{300}\right)^{-\beta(N_{imp})} \tag{1.19}$$

with $N_{imp} = N_A + N_D$. $\beta\left(N_{imp}\right)$ and $\mu\left(300, N_{imp}\right)$ is evaluated individually by fitting the experimental data. The function $\beta\left(N_{imp}\right)$ is calculated as:

$$\beta\left(N_{imp}\right) = \beta^{\min} + \frac{\beta^{\max} - \beta^{\min}}{1 + \left(\frac{N_{imp}}{N_\beta}\right)^{\gamma_\beta}} \tag{1.20}$$

where $\beta^{\min} = 0$ for highly doped material, $\beta^{\max} = 3.11$ for pure material, $N_\beta = 4.1 \times 10^{18}$ cm^{-3} and $\gamma_\beta = 0.617$ for boron doped diamond [6].

The $\mu\left(300, N_{imp}\right)$ function is calculated as:

$$\mu\left(300, N_{imp}\right) = \mu_{\min} + \frac{\mu^{\max} - \mu^{\min}}{1 + \left(\frac{N_{imp}}{N_\mu}\right)^{\gamma_\mu}} \tag{1.21}$$

where $\mu_{\min} = 0$ $(cm^2/V.s)$ for the highly doped diamond in which hopping appears, $\mu_{\max} = 2016$ $(cm^2/V.s)$ is the highest hole hall mobility, $N_\mu = 3.25 \times 10^{17}$ cm^{-3} and $\gamma_\mu = 0.73$ [6].

Thanks to the above analysis, following conclusions can be drawn:

1. Boron doped p-type diamond is more favorable for diamond unipolar devices. This conclusion is based on the fact that boron doped diamond has a lower dopant ionization energy and a higher free carriers concentration compared to n-type diamond. Furthermore, the hole mobility of p-type diamond is much higher compared to electron mobility in n-type diamond.

2. Regarding the compromise of boron concentration and hole mobility, a boron concentration of 10^{17} (cm^{-3}) is highly desired. Therefore, throughout this PhD thesis, a boron doped diamond epilayer of 10^{17} (cm^{-3}) is intentionally mastered.

3. The ideal ON-state device characteristic corresponding to a desired OFF-state breakdown voltage at a certain temperature can be projected by using the relationship between carrier density and carriers mobility with doping concentration and compensation concentration.

1.2.3 Dielectric breakdown field

As mentioned above, OFF-state breakdown voltage of a power device is limited by the maximum electric field of the material. Material with extreme critical electric field is highly desired for power device to control significant OFF-state voltage and consequently high power. As one can see from the different figure of merits, the higher the E_c critical field, the better the figure of merits. Therefore, wide bandgap devices reaching high critical electric field can have a strong impact on power converters

For diamond, Langstrass et al. [52] has reported a paramount critical electric field of 20 MV/cm. However, this value is relatively lacking reality. In the mentioned work, the

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test devices were fabricated on a thick epilayer (30 μm) and highly doped (10^{18} cm^{-3}). Commonly, diamond theoretical critical electric field is considered as around 10 MV/cm.

From experimental reports, diamond breakdown electric field is also very remarkable. P. N. Volpe et al. [12] reported a lateral oxygen terminated boron doped diamond Schottky diode on homoepitaxial boron doped (10^{16} cm^{-3}) diamond with a breakdown voltage of 10 kV and a peak electric field of 7.7 MV/cm at breakdown. The mentioned device structure and performance is shown in Fig. 1.11. Traore et al. also reported a similar breakdown electric field by using pseudo-vertical punch-through design [13]. The experimental breakdown electric fields of diamond are already much higher compared to the theoretical critical electric field of Si (0.3 MV/cm - doping and temperature dependent), 4H-SiC (3 MV/cm - doping and temperature dependent) and GaN (2 MV/cm - doping and temperature dependent, also devices structure dependent - GaN has a wider bandgap than SiC, but GaN devices are lateral where the peak electric field is not achieved due to 3D effects).

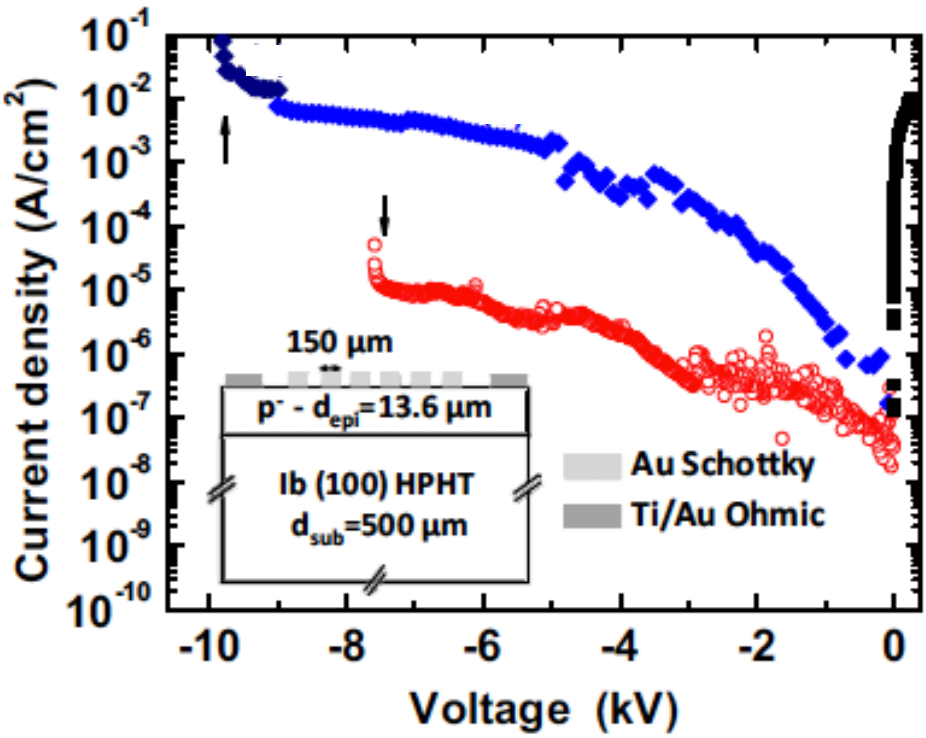

Figure 1.11: O-diamond Schottky diode on homoepitaxial boron doped diamond with a breakdown voltage of 10 kV and a breakdown electric field of 7.7 MV/cm. Courtesy of Volpe et al. [12].

So far, we have shown that boron doped diamond is possibly the ultimate material for unipolar high power devices. It is thanks to an elevated hole mobility and a superior breakdown electric field. The incomplete ionization problem can be solved by increasing the operation temperature. Therefore, diamond appeared to be an ideal candidate for unipolar high power and high temperature applications. In the next part, we will briefly review the architectures and performances of state-of-the-art diamond unipolar devices.

1.3 States-of-the-art of diamond unipolar power devices

Thanks to the superior physical properties, diamond was seriously considered for power devices. After decades of investigation, epitaxial growth and doping control are well mastered [35][36, 40]. Different approaches to realize the diamond devices have been done. It can be categorized into two main directions: 1) two terminals devices such as p-n junction [53], p-i-n junction [54], Schottky diode [55, 56, 12, 13]; 2) three terminal devices such as bipolar transistor like BJT [57][58], JFET [59, 60, 61, 62] and unipolar transistor like MOSFET, MESFET and delta doped FET. The works on bipolar junction transistor (BJT) [57][58] and junction field effect transistor (JFET) [59, 60, 61, 62] introduced numerous remarkable results on both the reliability at high voltage, high temperature and normally-off transistor. Also, delta doped field effect transistors [63][64] are very interesting to the physics point of view, although they did not show any mobility enhancement.

As we have mentioned, in frame of this PhD thesis, we will only focus on unipolar devices. As shown in Fig. 1.2, Schottky diode and transistor switches are the critical elements of a power converter system. Hereinafter, the recent achievements on unipolar diamond Schottky diodes and transistors will be summarized.

1.3.1 Diamond Schottky diode

Diamond Schottky diode with remarkable results were reported on both high ON-states current and high OFF-state voltage. P. N. Volpe et al. [12] reported a breakdown electric field as high as 7.7 MV/cm and a breakdown voltage around 10 kV. Other reports on diamond Schottky diode also shown the remarkable breakdown voltage like Butler et al. (6 kV)[55] and Umezawa et al. (840V- vertical structure)[56].

Traore et al. [13] reported a Punch-Through (PT) pseudo-vertical O-diamond Schottky diode with Zr electrode and achieved an ON-state current as high as 10^3A/cm^2 and an OFF-state voltage of 1 kV, as shown in Fig. 1.12. Thanks to the high ON-state current and high OFF-state voltage, a BFOM larger than 244 MW/cm^2 were obtained [13].

1.3.2 Diamond unipolar transistor

Basically, unipolar transistor can be categorized into either inversion mode transistor (Fig. 1.13a) or depletion mode transistor (Fig. 1.13b). Both inversion mode and depletion mode transistor diamond were realized.

In principle, as any insulator can be used as the gate insulator, the devices should be named as Metal Insulator Semiconductor Field Effect Transistor (MISFET). In this work, we only employed Al_2O_3 oxide for gate insulator. Therefore, the devices will be named as Metal Oxide Semiconductor Field Effect Transistor (MOSFET) hereinafter.

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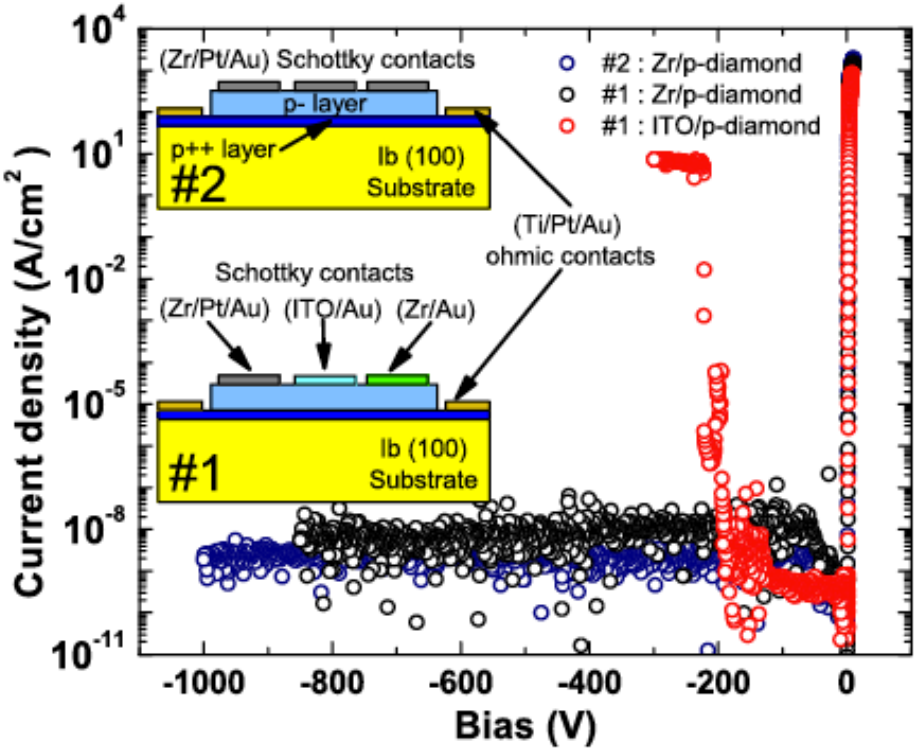

Figure 1.12: Pseudo-vertical diamond Schottky diode and its electrical characteristics, Courtesy of Traore et al. [13].

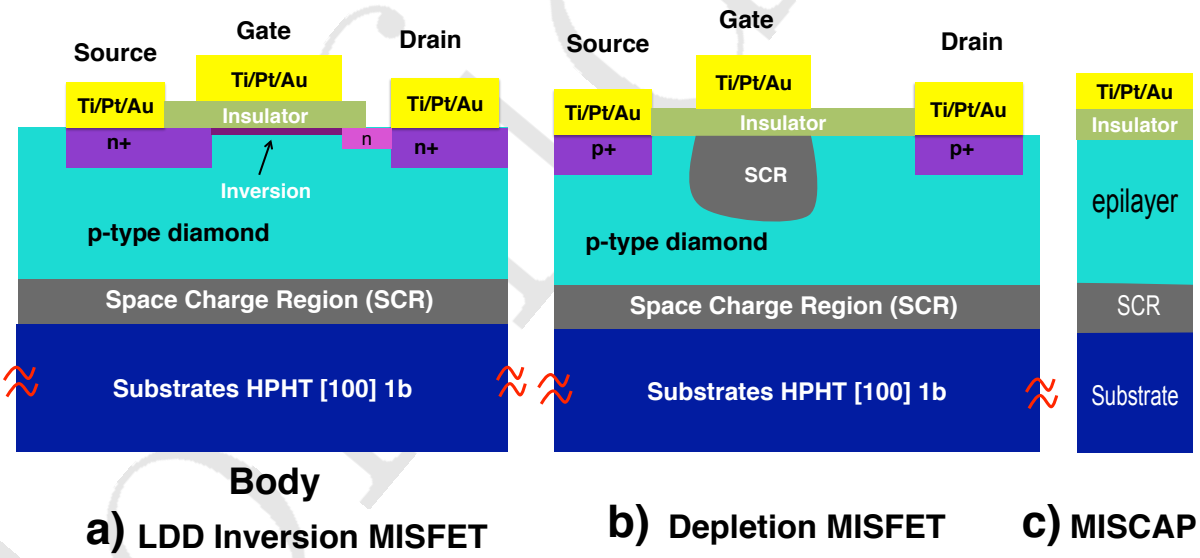

Figure 1.13: Cross-section structure of a) Lightly doped drain inversion MISFET; b) depletion MISFET; c) building block MISCAP.

1.3.2.1 Inversion mode diamond transistor

A conceptual cross-section structure of an LDD nMOS inversion mode transistor is shown in Fig. 1.13a. Here, bulk of the transistor is a p-type semiconductor, source and drain are formed on the n-type semiconductor. An pMOS inversion mode transistor can be formed

by using the n-type semiconductor as the body and p-type semiconductor on source and drain. Due to the p-n junctions between source/drain and bulk semiconductor, inversion transistor is normally-OFF. Transistor is ON when the minority carriers of bulk epilayer are inverted.

Recently, a pMOS phosphorous doped oxygen terminated inversion mode diamond MOSFET was realized by Matsumoto et al. [14]. Cross-section and top view structure of the device are shown in Fig. 1.14a-b, respectively. Device electrical characteristic is shown in Fig. 1.14c. An ON-OFF ratio of 10 order of magnitude was obtained. However, the maximum carrier mobility (8 $cm^2/V.s$) is much lower compared to the potential of diamond. Breakdown voltage was not measured [14], but this transistor structure is not a power transistor (no specific lateral drift region). This device was however a great experimental proof of concept, showing for the first time the inversion regime in diamond.

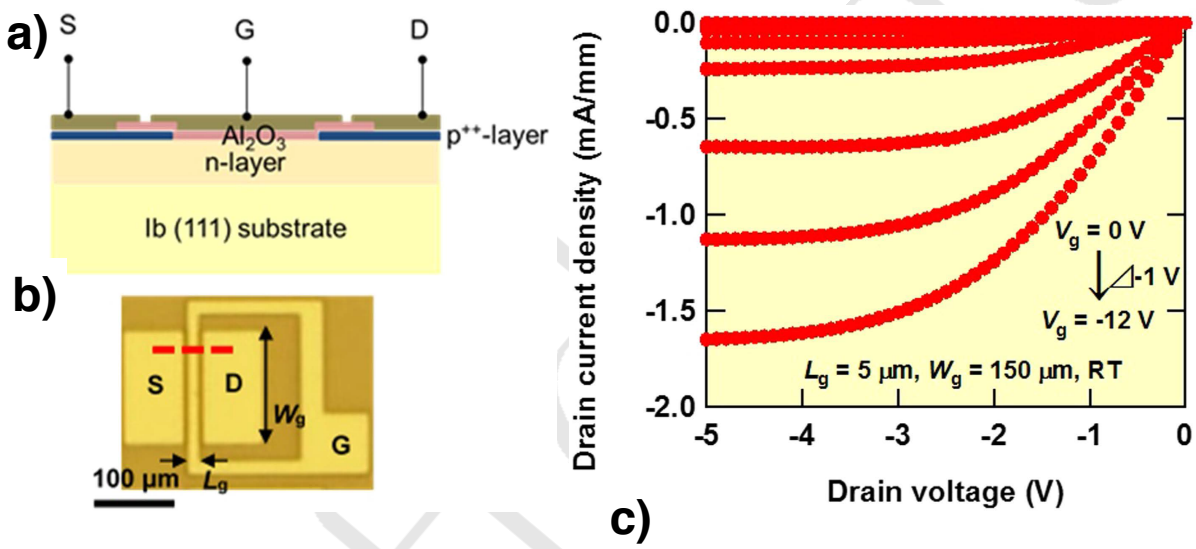

Figure 1.14: Inversion mode of pMOS phosphorous doped oxygen terminated diamond MOSFET: a) cross-section structure; b) top view structure; c) electrical characteristics. Courtesy of Matsumoto et al. [14].

1.3.2.2 Depletion mode transistor

Figure 1.13b represents the cross-section structure of a depletion mode MISFET. By adding/removing the insulator layer, MISFET and MESFET can be achieved, respectively. Since there are no p-n junction at source/drain and epilayer, the device is normally ON. Gate potential is employed to modulate and close the channel (OFF-state). Due to the specific doping concepts as discussed above, depletion mode diamond transistors can be categorized into two main types: surface channel FET and bulk channel FET.

Surface channel FET Thanks to the natural conductive diamond surface as well as the difficulties concerning epitaxial growth and bulk doping controlled, diamond surface channel transistor was widely considered. Kawarada et al. [65] reported a proper H-diamond MESFET in 1994. Since then, further H-diamond MESFETs were fabricated toward the high frequency applications [66, 67, 68].

However, a problem with H-diamond MESFET is the deleterious of 2DHG at elevated temperature. To solve this problem, one employed a protective oxide layer to cover on top of H-diamond surface. In this context, the researchers at NIMS [2] have reported the band alignments and the electrical behaviors of H-diamond with many oxide layers [69, 70, 71, 72, 73]. Band alignment measurements shown that there are a sufficient valence band off-set between H-diamond and oxides. This configuration is, in principle, preferable to block the hole from semiconductor transferring through the oxide layer to metal gate and vice versa. However, due to the negative electron affinity of H-diamond, only type II band alinement between H-diamond/oxide is obtained. There are no barrier for electron from diamond side. Therefore, by using H-diamond, only depletion-mode transistor is expected.

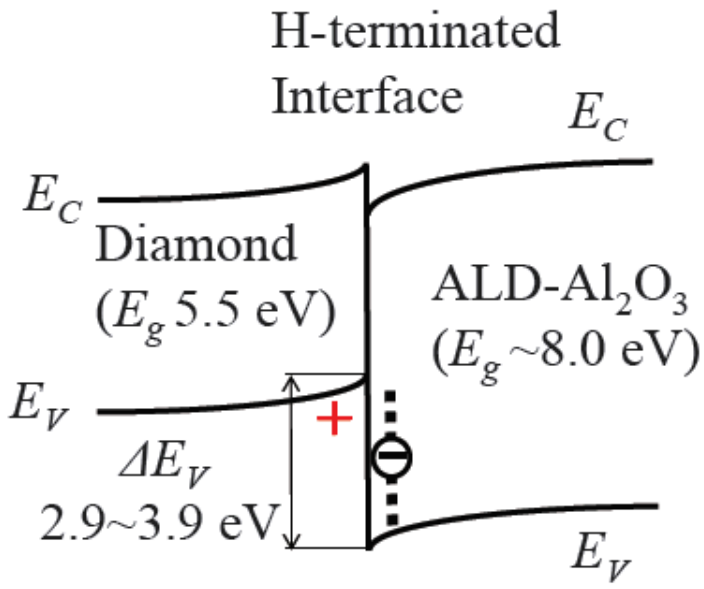

Figure 1.15: The proposed model for the 2DHG at H-diamond/oxide interface. Courtesy of Kawarada et al. [15].

The stability of 2DHG were addressed by the Kawarada's group at Waseda university [3]. Recent approaches demonstrated that Al_2O_3 deposited at high temperature (450°C) could greatly preserve the 2DHG [74, 75]. The origin of 2DHG at H-diamond/oxide interface is proposed to be due to the electron transfer between diamond and the trap states in the oxide, as similar to the concept of 2DHG at H-diamond/air interface (Fig. 1.7). Figure 1.15 represents the proposed model for the 2DHG at H-diamond/Al_2O_3 interface in Kawarada et al. [15].

Thanks to the preservation of 2DHG, many H-diamond MOSFETs were realized [76, 21]. A recent report demonstrated the H-diamond MOSFET with an ON-state current exceeding 100 mA/mm at V_{DS}=-50 V and an OFF-state breakdown voltage of 1700 V for L_{GD} =17μm, as shown in Fig. 1.16 [15]. Until the moment, this is among the best performance of a diamond transistor. This performance is also comparable with the lateral devices of other mature power devices like III-Nitride or SiC.

[2] http://www.nims.go.jp
[3] http://www.kawarada-lab.com/english/index.html

Recently, the Kawarada's group also demonstrated the preservation of 2DHG for not only on the planar structure but also on the trench gate structure [15]. Thank to this particular interest, a vertical trench gate H-diamond MOSFET was recently realized [77].

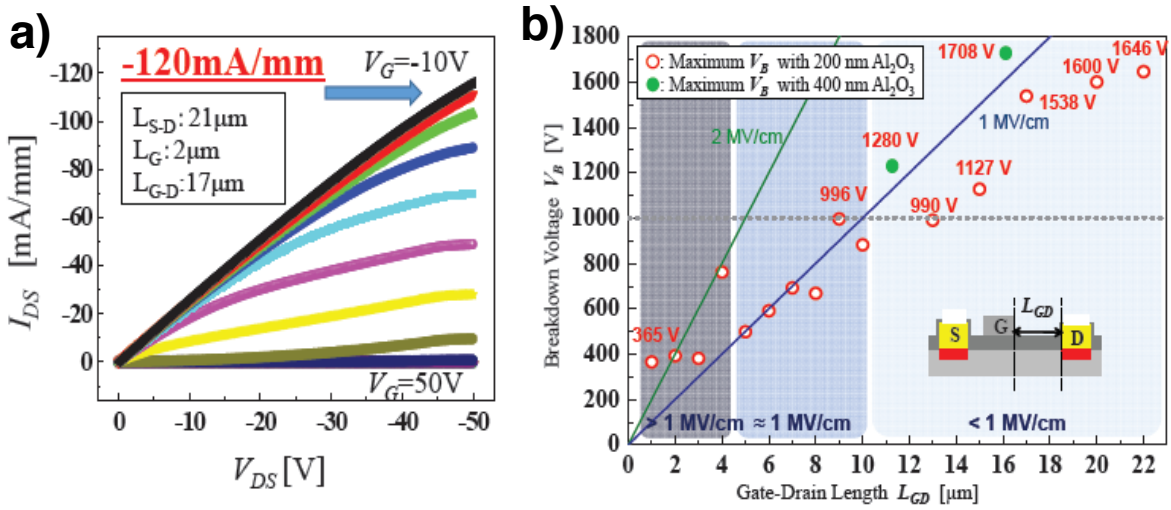

Figure 1.16: Electrical characteristics and breakdown voltage at different gate to drain distances of H-diamond MOSFET. Courtesy of Kawarada et al. [15].

Even if the performance of H-diamond MOSFET is very interesting, its working principle is actually based on an uncontrollability extrinsic factor i.e. trap states in the oxide (as shown in Fig. 1.15). For power electronic applications where the reliability of the device is crucial, this drawback is very undesired and necessary to be eliminated. Also, this device has a positive temperature effect (ON-state resistance is increased by increasing the temperature) [15]. Usually, the surface conduction transistors are based on pseudo-intrinsic substrates, therefore there is no optimization of the doping concentration relatively to voltage breakdown mechanisms.

Bulk channel FET As shown in Fig. 1.13b, a depletion mode transistor can also be realized by controlling the SCR in bulk of epilayer. To realize an effective bulk controlled FET, one needs to firstly master the issues related to epitaxial growth, dopant incorporation and also high ionization energy of the dopant levels. However, since all of the superior physical properties of diamond that we discussed above are related to bulk diamond, a bulk controlled diamond FET is highly desired.

Umezawa et al. [16] realized a bulk controlled diamond MESFET by using oxygen terminated boron doped diamond. Top view structure and cross-section structure of this boron doped diamond MESFET are shown in Fig. 1.17.

Device electrical characteristic is shown in Fig. 1.18a. ON-state current of 0.06 mA/mm is obtained. The ON-state current is limited by the highly resistive contact resistance. For OFF-state breakdown voltage, the device achieved a 1500 V breakdown voltage. Since this device is using bulk as the channel, a negative temperature coefficient is obtained.

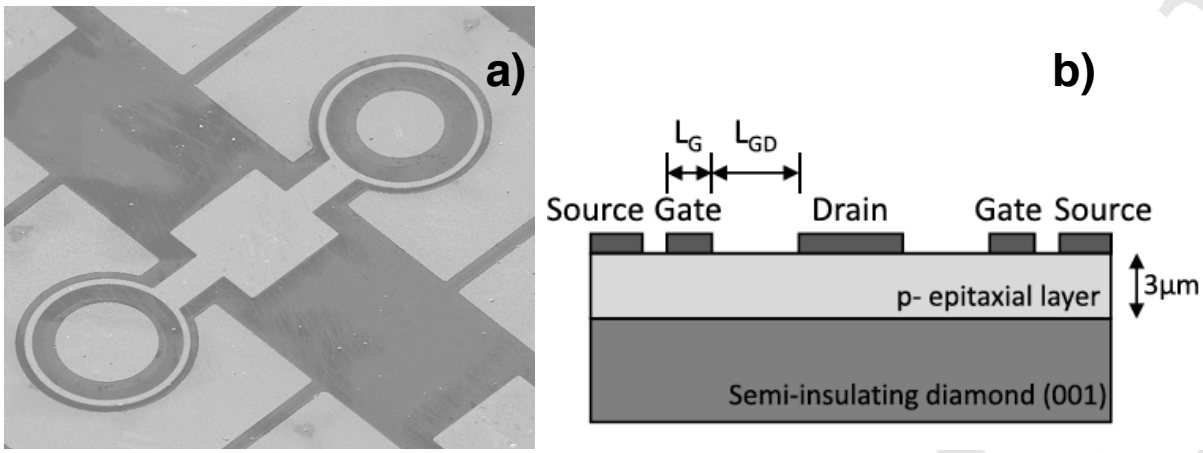

Figure 1.17: Top view structure and cross-section structure of the oxygen terminated boron doped diamond MESFET. Courtesy of Umezawa et al. [16].

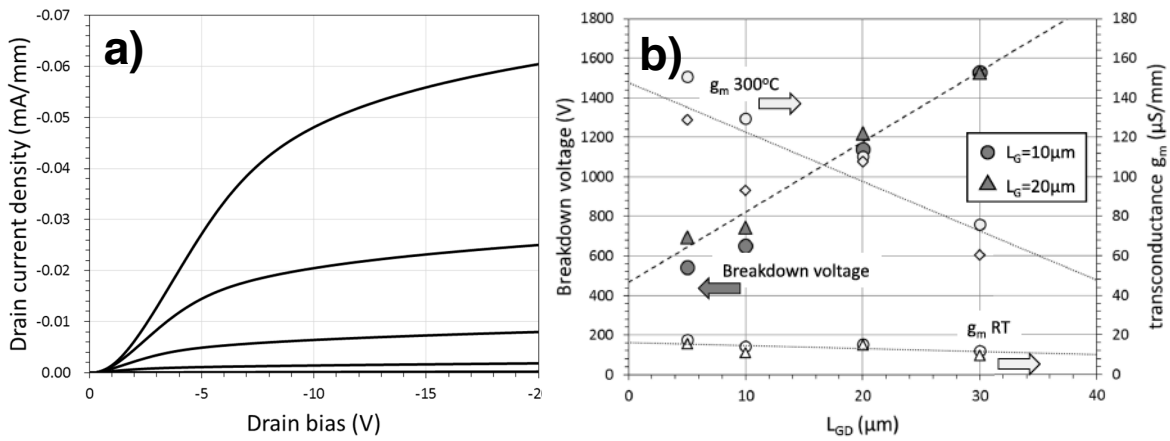

Figure 1.18: MESFET electrical characteristics and breakdown voltage at different gate to length distance. Courtesy of Umezawa et al. [16].

However, there are two problems with the boron doped bulk controlled diamond MESFET. The first problem is related to the versatility of gate bias. Since the gate is formed by a Schottky diode, there are generally a small threshold voltage in the forward regime. Therefore, gate of the transistor is only able to be biased from around 0 V to positive bias (to prevent gate leakage current in the transistor to allow electrostatics controlled diamond epilayer). Therefore, the accumulation regime in semiconductor is not obtainable. This problem can be important in the moderate voltage application (around 1 kV) where channel length is approximate gate to drain distance. Another problem with MESFET is related to reverse current at the Schottky contact between metal gate and diamond. As discussed in Traore PhD thesis [78], reverse current in diamond Schottky diode is controlled by thermionic-field emission. By increasing diamond doping concentration, electric field in reverse bias is being steeper. The typical thermionic emission current in an ideal Schottky diode will be enhanced by the tunneling current occurs at the thinner extension part of the potential barrier. Therefore, in order to prevent reverse leakage current, a low doped drift region of 10^{16} cm^{-3} is required [78]. As we discussed above, this doping concentration is not an optimized value for the trade-off between the

activated carriers and the carriers mobility. Moreover, the doping of the drift region is usually optimized to one particular value, as a function of the targeted breakdown voltage [23].Therefore, in order to be able to bias the gate in negative direction as well as increase the doping concentration of the epilayer to the optimum value (10^{17} cm^{-3}), a gate oxide must be introduced.

1.4 Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

1.4.1 MOS capacitor working principle

As shown in Fig. 1.13, a general feature between the inversion MOSFET and the depletion MOSFET is the MOS capacitor building block (Fig. 1.13c). In principle, once a V_{DS} is applied, the ON/OFF current between source and drain is actually controlled by the voltage at gate metal. The physics behind this phenomenon is gate controlled semiconductor surface potential Ψ_s and semiconductor charges Q_{sc}. This relationship for a p-type semiconductor can be schematically represented in Fig. 1.19. Semiconductor charge Q_{sc} is calculated as a function of semiconductor surface potential Ψ_s as following [17]:

$$Q_{SC}^{A}(\Psi_s) = \pm\left[2\varepsilon_{sc}qN_A\left\{\frac{kT}{q}\left(e^{-q\Psi_s/kT}-1\right)+\Psi_s+\frac{kT}{q}e^{q(\Psi_s-2\Psi_b)/kT}\right\}\right]^{1/2} \tag{1.22}$$

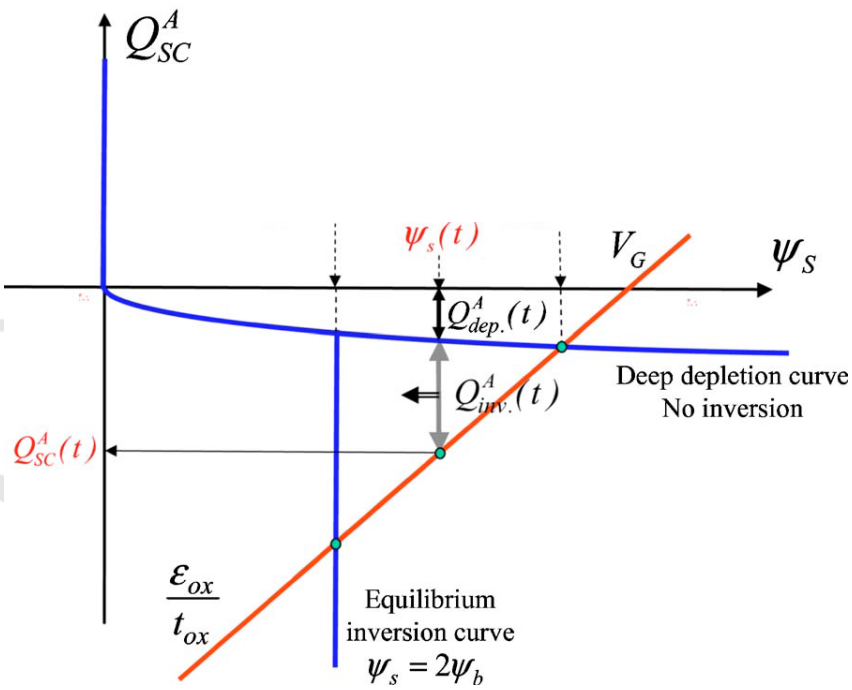

Figure 1.19: Relationship between semiconductor charge Q_{SC} and semiconductor surface potential Ψ_S. Courtesy of Vincent et al. [17].

where Ψ_s is the semiconductor surface potential, Ψ_b is bulk potential which is defined as potential different between intrinsic Fermi Level and Fermi Level in the neutral part. Semiconductor surface potential Ψ_s is defined as the potential difference between surface and neutral part of semiconductor. The (+) and (-) sign correspond to the positive charge of the hole in accumulation regime ($\Psi_s < 0$) and negative charge of electron in inversion regime ($\Psi_s > 2\Psi_b$), respectively.

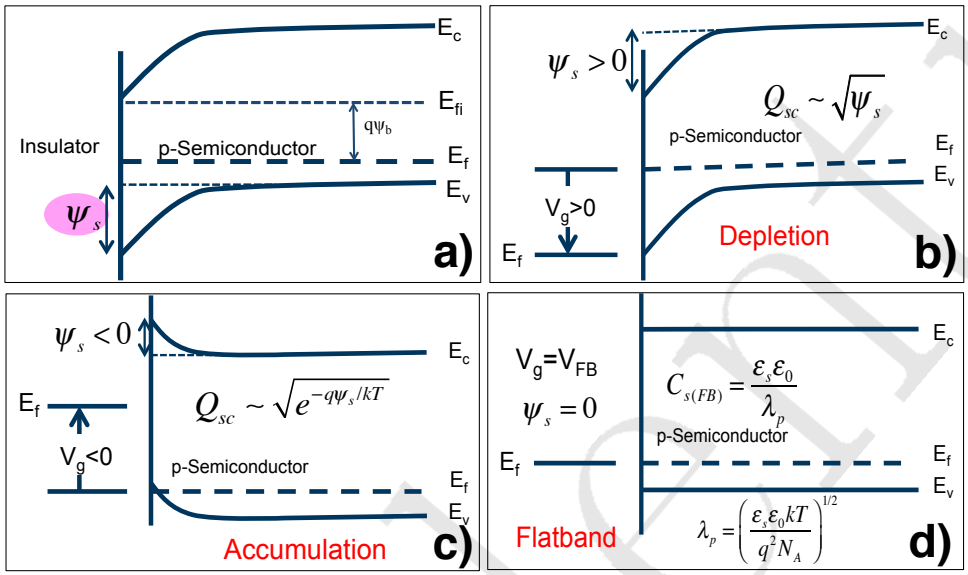

Figure 1.20: Schematics description of different regimes of a MOS capacitor: a) definition of semiconductor surface potential Ψ_S; b) accumulation regime under negative bias; c) depletion and deep depletion regime under positive bias; d) Flatband regime where there are no energy different between surface and neutral part of semiconductor.

In an ideal p-type semiconductor system, by biasing gate metal from negative bias to positive bias, semiconductor surface potential and semiconductor charge are being driven into different regimes:

1. Accumulation: When a negative gate bias is being applied, semiconductor surface band energy is bent upward. Majority carriers are being accumulated at semiconductor-oxide interface, as shown in Fig. 1.20c. Semiconductor charge Q_{sc} (equation 1.22) can be approximated as:

$$Q_{sc} \sim \sqrt{e^{-q\Psi_s/kT} - 1} \tag{1.23}$$

2. Depletion and deep depletion: When a positive bias is being applied, the p-type semiconductor band energy is bent downward, as shown in Fig. 1.20b. Semiconductor is being converted to depletion and deep depletion regime. The semiconductor charge Q_{SC} is proportional to square root of surface potential. Equation 1.22 is approximated by:

$$Q_{sc} \sim \sqrt{\Psi_s} \tag{1.24}$$

3. Inversion: Semiconductor reach the inversion regime when $\Psi_s > 2\Psi_b$ (Fig. 1.19). With Ψ_b is semiconductor bulk potential, as defined in Fig. 1.20a. Semiconductor charge at the surface is being inverted by minority carriers. Semiconductor charge is being exponentially proportioned to $\Psi_s - 2\Psi_b$. Equation 1.22 can be approximated as:

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$$Q_{sc} \sim \sqrt{e^{q(\Psi_s - 2\Psi_b)/kT}} \tag{1.25}$$

4. Flatband: Flatband regime is the position where there are no energy difference between the surface and the neutral part of semiconductor. In another words, semiconductor surface potential is equal to 0 eV, as schematically shown in Fig. 1.20d. Therefore, flatband voltage and flatband capacitance are a demarcation between accumulation and depletion. At flatband voltage, semiconductor charge and consequently semiconductor capacitance is a function of semiconductor intrinsic Debye length as:

$$C_{s(FB)} = \frac{\varepsilon_{sc}\varepsilon_0}{\lambda_p} \tag{1.26}$$

With λ_p is the semiconductor intrinsic Debye length and be calculated as:

$$\lambda_p = \left(\frac{\varepsilon_s \varepsilon_0 kT}{q^2 N_A}\right)^{1/2} \tag{1.27}$$

A "completely electrostatics gate controlled MOS capacitor" is obtained when metal gate can effectively tune semiconductor surface potential and semiconductor charges to all regimes: accumulation, flatband, depletion, deep depletion and inversion. Subsequently, depending on the FET structure and architecture, the current flowing/blocking between source and drain can be controlled by the metal gate.

In this context, in order to examine the possibility of using boron doped diamond for diamond MOSFETs, we need to perform the study on the boron doped diamond MOS capacitor. As illustrated by Maier et al. [33], there are 3 eV difference between H-diamond and O-diamond. With the negative electron affinity of H-diamond(-1.3 eV), there are no oxide candidate to be able to create a type-I band alignment (oxide can create the barriers for both hole in valence band and electron in conduction band of semiconductor) between H-diamond and oxide. Therefore, it is not possible to obtain an inversion MOSFET by using H-diamond. A viable approach is terminated diamond surface by oxygen. Oxygen terminated diamond can be obtained by either oxygen plasma treatment, chemical treatment or deep UV ozone (Xenon lamp centered at 172 nm serve as UV light sourve) treatment [18, 79]. With an electron affinity of approximately +1.7eV [33], O-diamond is expected to have a type-I band alignment with Al_2O_3. Therefore, by using O-diamond, it is possible to realize either depletion-mode transistor and inversion-mode transistor.

1.4.2 O-diamond MOS capacitor

The research on O-diamond MOS capacitor at Wide Bandgap Semiconductor Group (SC2G) [4]- Institute NEEL begun from 2012. Chicot et al. [18] reported the first O-diamond MOS capacitor by using the DUV ozone treatment and a low temperature (100°C) Atomic Layer Deposition (ALD) to deposit Al_2O_3 gate oxide. The initial MOS capacitor test device structures are shown in Fig. 1.21. The author claimed they are able to modulate diamond semiconductor in different regime: accumulation, depletion and deep depletion. However, this initial approach also shown the problematic of gate

[4] http://neel.cnrs.fr/spip.php?rubrique48

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leakage current and capacitance-frequency dependent, as shown in Fig. 1.22. Gate leakage current and strong capacitance-frequency dependent were systematically observed when MOS capacitor devices being biased negatively. Under positive bias, leakage current and capacitance-frequency dependent were also observed, but randomly.

In 2015, Kovi and co-authors [20] at Uppsala University [5] also reported the results on oxygen terminated boron doped diamond MOS capacitor. They employed the identical structure and varied the epilayer doping concentration (from 10^{17} cm^{-3} to 4×10^{19} cm^{-3}). They obtained similar electrical characteristics than Chicot et al. [18]. Test devices exhibit a strong leakage current and strong capacitance-frequency dependent. The authors claimed they observed the minority carriers inversion on the fact that gate leakage currents were significant [20] .

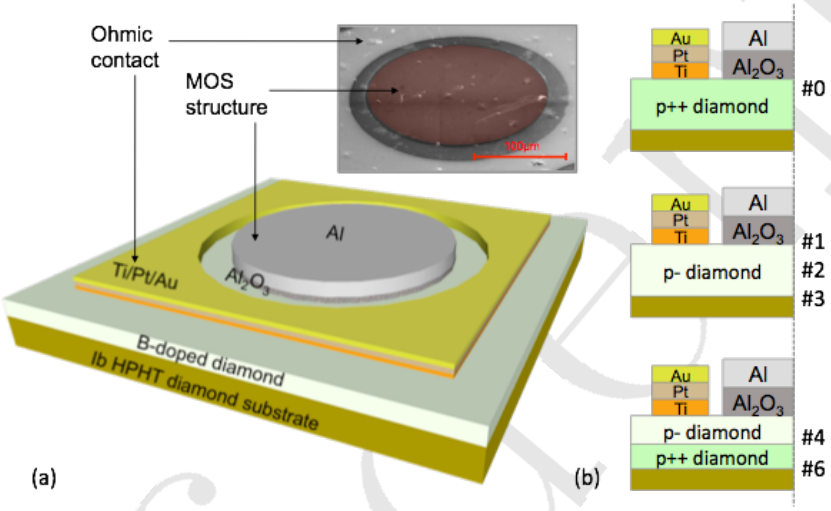

Figure 1.21: First propositional structure of a O-diamond MOS capacitor. Courtesy of Chicot et al. [18]

In 2015, Marechal et al. [19] at SC2G[6] and G2Elab [7]reported the O-diamond MOS capacitor by using pseudo-vertical structure, as shown in Fig. 1.23a. In this new architecture, a metallic p+ diamond is inserted at the bottom electrode to reduce the series resistance. Ohmic contacts were deposited directly on the metallic diamond p+ layer. This architecture allows Al_2O_3 to be deposited at higher temperature (as high as desirable and within the limit of the apparatus). Gate leakage current and capacitance-frequency dependent were greatly reduced, but still existing.

By performing the X-ray Photoemission Spectroscopy (XPS) measurement, type-I band alignment between O-Diamond/Al_2O_3 was determined [19] and shown in Fig. 1.23c. This band alignment configuration allowed to realize both depletion MOSFET and inversion MOSFET as well as confirmed the advantage of using O-diamond for boron doped diamond MOSFETs.

Even if the test device performance has improved, the problematic issues is still existing. There are still systematic leakage currents and capacitance-frequency dependence when test devices are under negative bias. Under positive bias, leakage currents are

[5]http://www.uu.se/en
[6]http://neel.cnrs.fr/spip.php?rubrique48
[7]http://www.g2elab.grenoble-inp.fr

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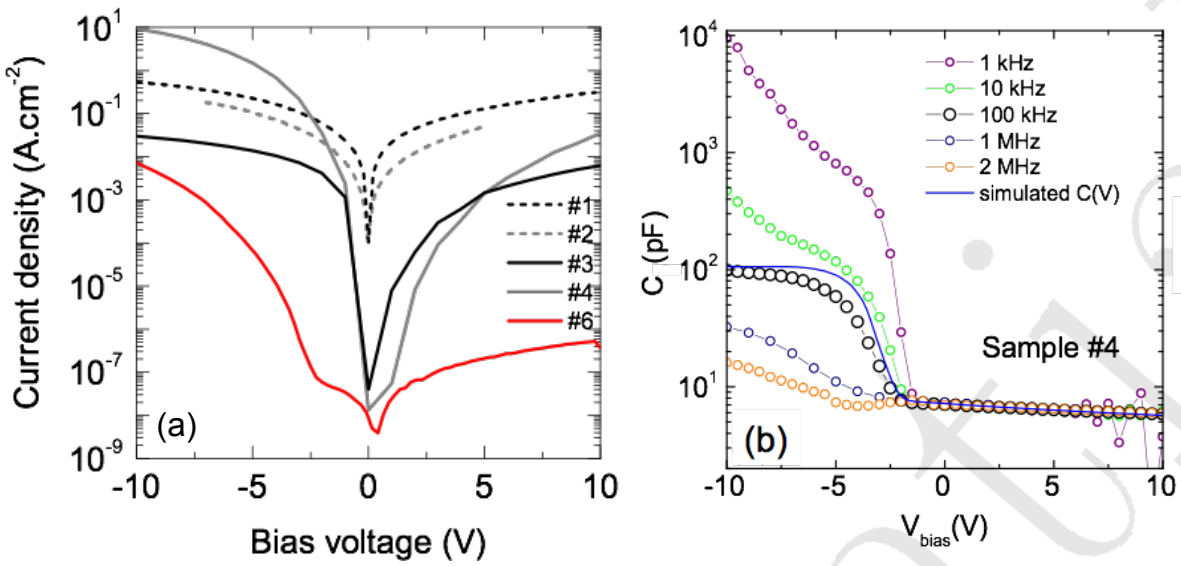

Figure 1.22: Typical J-V and C-V characteristics of some first O-diamond MOS capacitor. Leakage current in both forward bias and reverse bias is observed. Capacitance are strongly frequency dependent. Courtesy of Chicot et al. [18]

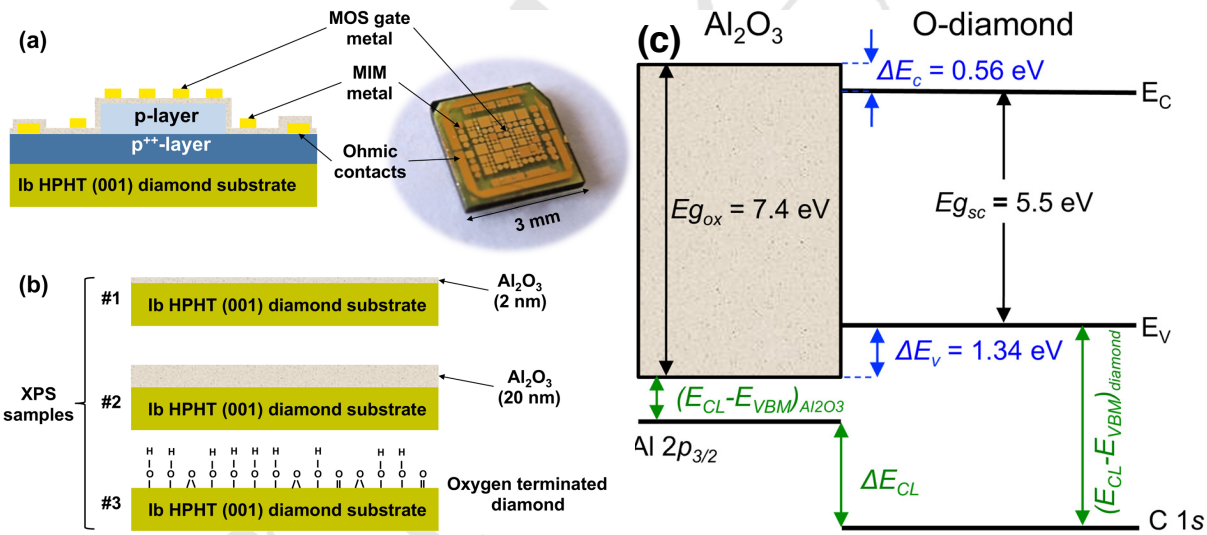

Figure 1.23: a) Pseudo-vertical structure O-diamond MOS capacitor; b) Band alignment between O-diamond and Al_2O_3 deposited at 250 °C. Courtesy of Marechal et al. [19]

still randomly observed. From the understanding point of view, the physical insight of O-diamond MOS capacitor is still unclear. There are not existing an appropriate model on the leakage current under both negative bias and positive bias. The origin of capacitance-frequency dependent is still unclear. Information on the Al_2O_3 gate oxide, the interface and most importantly, the controllability of diamond by using gate bias were not clearly and quantitatively clarified. In the end, a complete electrostatics model for the O-diamond MOS capacitor is still missing at the beginning of my PhD.

From the transistor point of view, a proper unipolar boron doped diamond MOSFET by controlling bulk diamond is still not accomplished at the beginning of this PhD study.

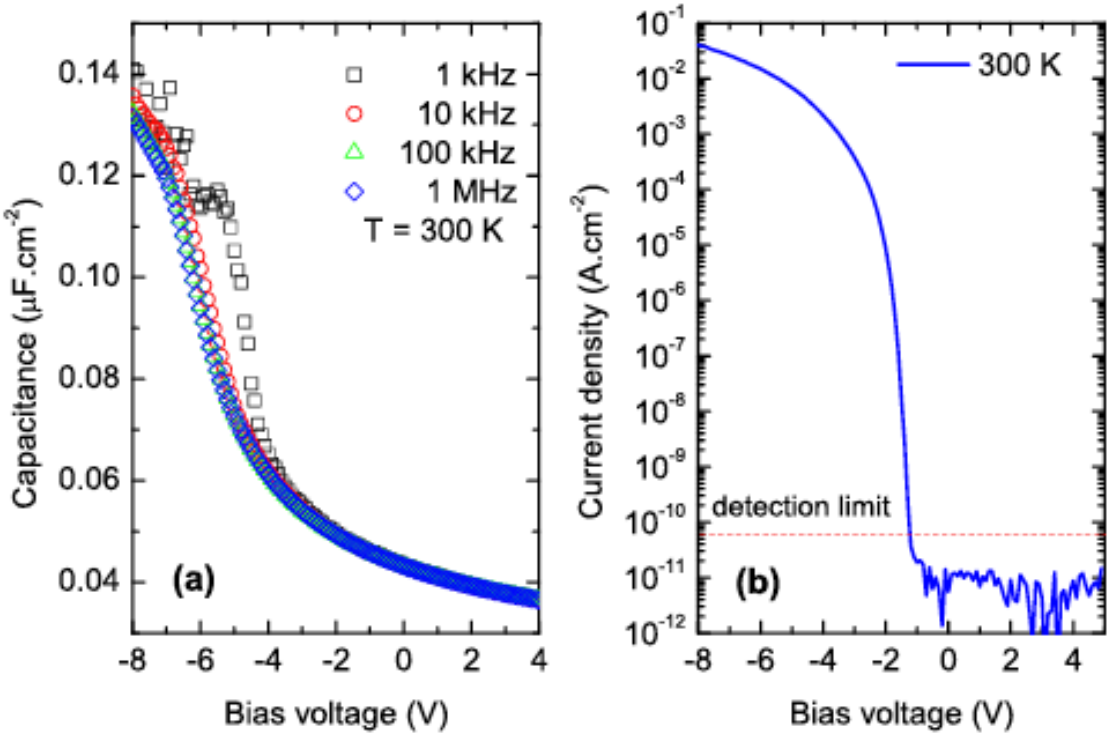

Figure 1.24: Electrical characteristics of the pseudo-vertical O-diamond MOS capacitor, a) C-V characteristic; b) J-V characteristic. Courtesy of Marechal et al. [19]

1.5 Conclusion

Diamond is a fascinating semiconductor with multiple superior physical properties for power electronics devices. However, a 2DHG surface channel diamond MOSFET is seemly not sufficient to fulfill all the potential. Controlling the bulk of diamond to realize a transistor is therefore crucial.

The objective of this thesis is the realization of a bulk controlled boron doped diamond MOSFET for power device applications. The scope of this thesis is ranging from the fundamental investigations the test device MOS capacitors structure and then realization a diamond MOSFET. This thesis is devoted to address the following issues:

i) The reliability of C-V measurements and eliminate the artifacts.

ii) How to access critical information on diamond semiconductor like surface potential, semiconductor charges, space charge width and its variation with gate bias?

iii) What is the origin of leakage current in both forward bias and reverse bias direction? What is the origin of capacitance-frequency dependent in both forward bias and reverse bias? Is it minority carriers inversion observed by Kovi et al [20]?

iv) From the understanding of the MOS capacitor test devices, is it possible to realize a diamond MOSFET by controlling the bulk of diamond? How about the performance and the potential of this transistor?

This manuscript will answer to the mentioned questions by two main chapters:

Chapter 2: This chapter is devoted to the fundamental understanding of MOS capacitor test devices. It is included three parts:

Part 1: This part addresses the methodology issues related to diamond growth

and doping controlled, fabrication processes and electrical characterizations. The reliability issues related to a proper C-V measurements. From proper C-V measurements, we evaluate the information of a O-diamond MOS capacitor such as charges components, semiconductor surface potential and SCR width variation with gate potential. High frequency-capacitance method is being applied to quantify interface states density. Electrostatics model based on different charge components is constructed. Electrostatics band diagram will be introduced and the limit of this model will be discussed.

Part 2: This part is devoted to elucidate the origin of leakage current of MOS capacitors under negative bias. The origin of capacitance-frequency dependent will be discussed. Interface states density will be re-evaluated by using the conductance method with DC current contribution being subtracted. With the interface states density from conductance method, a complete electrostatics simulation will be introduced and compared with experimental results by mean of semiconductor surface potential.

Part 3: This part is devoted to investigate the origin of gate leakage current when MOS capacitors are under positive bias. Device characteristics-substrates profile correlation will be mentioned. Relationship between leakage current and capacitance-frequency dependent when MOS capacitors are under positive bias will be elucidated. Origin of the so-called "inversion" will be discussed.

Chapter 3: This chapter is devoted to introduce the proof of concept of a bulk controlled boron doped diamond MOSFET. We will introduce our approaches to realize a bulk controlled boron doped diamond MOSFET working in depletion mode. The performance of this device will be presented and demonstrated a complete electrostatic gate controlled boron doped diamond MOSFET. Along with the MOSFETs, different test devices such as MOS capacitors, TLMs were also fabricated and will be presented. The combination of MOSFETs with test devices and 2D finite element simulations allows us quantify the critical parameters of the MOSFET like contact resistance and carriers mobility. This device will be benchmark for the purpose of comparison with other diamond transistor and will be projected toward device optimization.

Finally, conclusions and perspectives of this work will be given.

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Chapter 2

Oxygen terminated boron doped diamond metal oxide semiconductor capacitor

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As introduced in the first chapter, the MOS capacitor stack is the building block of a MOSFET. In order to realize a diamond MOSFET, it is necessary to comprehensively control the diamond/oxide interface. Therefore, a complete understanding of the MOS capacitor is required. In this chapter, we will focus on different fundamental aspects of the boron doped O-diamond MOS capacitor test device toward a bulk controlled diamond MOSFET. This chapter will include three parts:

Part 1: We address several technical issues related to a MOS capacitor test device such as: the needs of new structures to reduce series resistance, the diamond growth and device fabrication processes, the electrical measurements and the finite element electrostatics simulation. Then, we examine the artifact effects on the capacitance measurement and we introduce a method to perform a proper capacitance measurement. From the proper capacitance measurement, the methodologies to quantify the crucial information of the MOS capacitor such as semiconductor charge, oxide charge and the variation of semiconductor surface potential versus gate bias will be presented. Interface states density is also extracted from the high frequency-capacitance method. Finite element electrostatics simulation will be employed to simulate the electric field, potential distribution and electrostatics band diagram of the system. The discrepancy between simulation results and experiment results by mean of semiconductor surface potential will be discussed.

Part 2: From the electrostatics band diagram, the origin of leakage currents when O-diamond MOS capacitors are under negative bias (forward current) will be elucidated in this part. A special attention will be paid to the relationship between forward current and interface states. We will also discuss different aspects related to the leakage current such as the limiting processes and the thermal activation processes. Equivalent circuit will be introduced and different approximations will be employed to simplify the model. Conductance method by using the equivalent circuit and subtracting the DC current is employed to extract interface states density. The relationship between DC leakage current and a.c signal measurements will be clarified. A complete electrostatics model will be presented.

Part 3: We discuss the leakage current when the MOS capacitor is under positive bias (reverse current). The relationship of reverse current with substrate imperfection will be clarified by mean of combination electron beam microscope measurements. The effect of DC reverse current on the a.c measurements will be elucidated by mean of equivalent circuit with all determined parameters. The conclusion on minority carriers inversion in O-diamond MOS capacitor by Kovi et al. [20] will be reassessed.

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Part I

Electrostatics

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2.1 Methodology

2.1.1 MOS Capacitor test device structure

As mentioned in chapter 1, one of the problems with diamond devices at RT is the incomplete ionization of the dopant. Even if boron is the shallowest dopant, its ionization energy is still very high ($E_A \simeq 0.38$ eV). Therefore, there are limited number of free carriers on the energy band edges. A consequence of this issue is the series resistance of diamond devices will be high. As shown in Fig. 2.1a, by using the lateral structure without a metallic p+ layer [18], a considerable series resistance in the MOS capacitor is expected since all the current is flowing in the incomplete ionized semiconductor p- layer [22]. Another problem with lateral structure [18] is the limitation of ALD temperature. Due to the photoresist layer on top of diamond substrate, temperature of ALD chamber have to be limited at around 100°C (to prevent damaging the photoresist layer).

In order to solve the mentioned problems, we employed the pseudo-vertical structure [13] with a metallic diamond layer on the back side of the epilayer. With this metallic p+ layer, most of the additional ON-state resistance is localizing in metallic p+ layer, as shown in Fig. 2.1b. Comparing to the lateral structure in Fig. 2.1a, where most of the additional ON-state resistance is localizing in the p- layer, the pseudo-vertical structure is expected to have a much lower series resistance. The pseudo-vertical MOS capacitor is firstly presented in Marechal et al. [19] and his PhD thesis [24]. This structure will be used for all MOS capacitor test devices in this chapter.

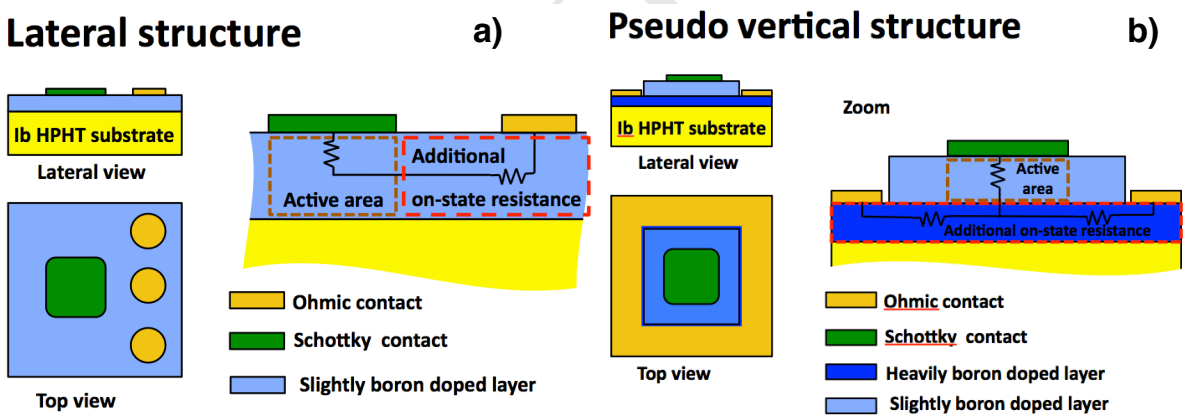

Figure 2.1: Illustration of the conduction path in MOS structures; a) without a buried p++ layer; b) with a buried p++ layer.

Figure 2.2a represents the conceptual cross-section structure of the O-diamond MOS capacitor test devices used in this work. In this structure, a 300 nm metallic diamond p+layer (5×10^{20} cm^{-3}) is inserted at the bottom of p- diamond epilayer (10^{17}cm^{-3}). Both layer were homoepitaxially grown on top of a diamond substrate. The p- layer was then selectively etched to create a mesa structure. Ohmic contact and Metal-Insulator-Metal (MIM) capacitor test devices are allowed to be deposited directly on top of p+ layer. Metal-Oxide-Semiconductor (MOS) capacitor test devices are formed on top of the semiconducting p- layer. Test devices (MIM capacitors and MOS capacitors) were intentionally fabricated with different shapes and sizes. The corresponding plan view structure is shown in Fig. 2.2b.

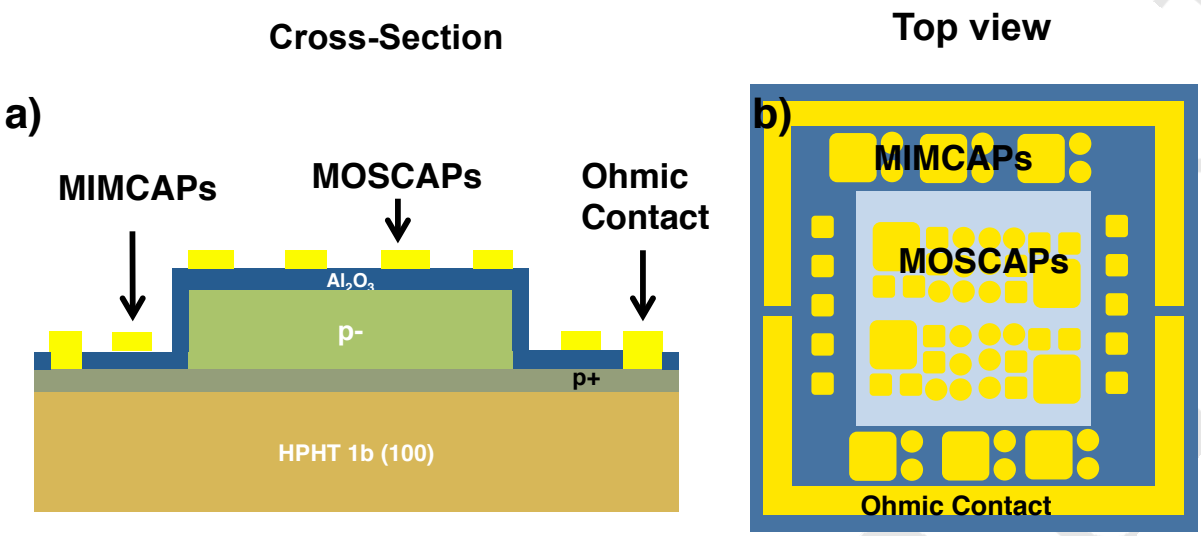

Figure 2.2: a) Conceptual cross-section structure of test devices included Ohmic contact, MIM Capacitors and MOS Capacitors; b) Corresponding plan view of test device structure where MIM capacitors and MOS capacitors are fabricated with different shapes and sizes.

2.1.2 Substrates and cleaning substrates

The 3×3 (mm×mm) High Temperature High Pressure (HTHP) Sumitomo (100) diamond substrate is used to grow the diamond epilayer. Figure 2.3a represents the typical substrates dimension and Figure 2.3b represents an optical profile-meter photograph of the substrate. The substrate was polished by Syntek company to provide the atomically flat diamond surface. Corner-cut was specifically designated to distinguish the top-side and bottom-side of the substrate.

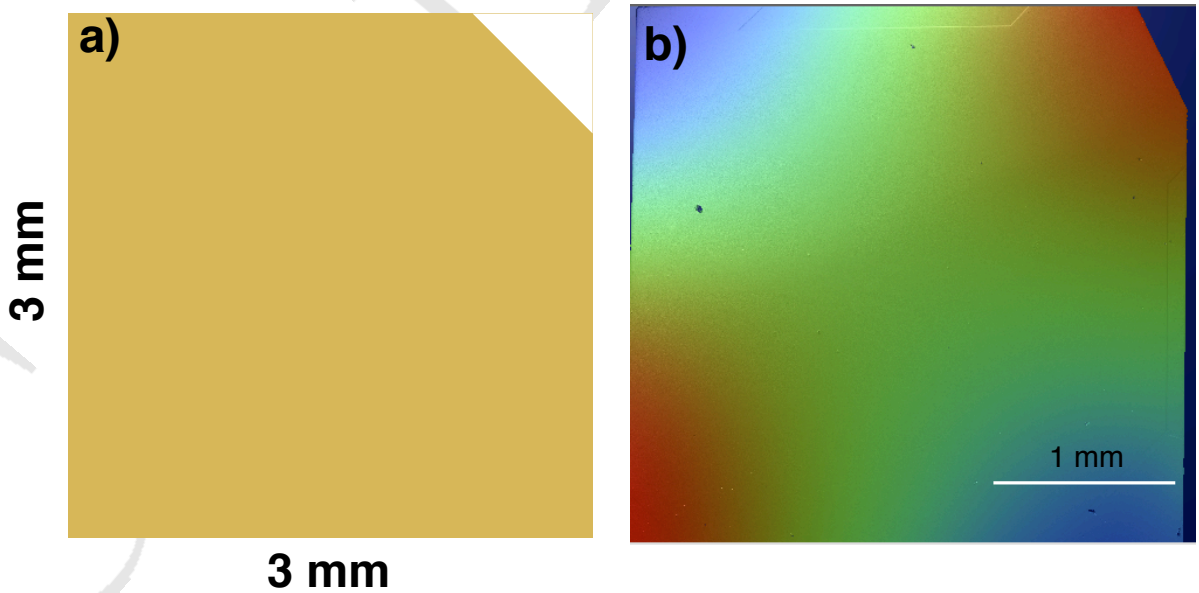

Figure 2.3: a) Typical feature of a 1b HTHP diamond substrate; b) Optical profile-meter photograph of the substrate.

Prior to the growth, the substrate is cleaned by a standard cleaning process. In a first step, the substrate is cleaned with solvent (acetone, ethanol, DI water) in ultrasonic to remove dust and surface contaminations. In a second step, the substrate is immersed into a mixture acid solution of $HClO_4$:HNO_3:H_2SO_4 (1:4:3) at 250°C during 30 minutes to remove carbon-phase and graphite on the diamond surface.

2.1.3 Diamond growth

Diamond epilayers were grown by Microwave Plasma-enhanced Chemical Vapor Deposition (MPCVD) NIRIM reactor [4]. This is a modified version of the Japanese reactor created at NIRIM (National Institute of Research in Inorganic Materials) by Kamo et al. [80]. Figure 2.4b represents the photograph of the MPCVD reactor at Institut NEEL [1] when the plasma ball is activated.

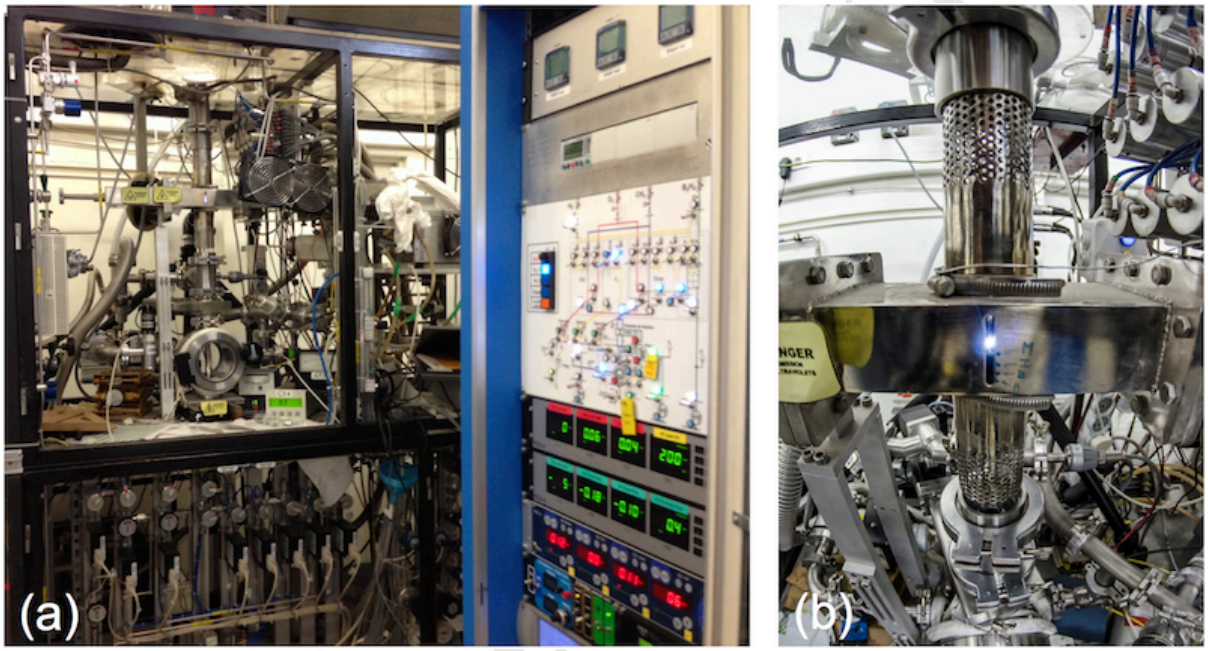

Figure 2.4: MPCVD reactor at Institut NEEL.

Figure 2.5 represents the working principle of the reactor. The reactor working principle is based on a plasma discharge ball at the intersection between silica tube and microwave guide. A microwave guide (generator operating at 2.45 GHz) can be tuned by adjusting the impedance in order to minimize the reflected power and maximize the energy at the plasma discharge ball. Gas sources like methane, oxygen, hydrogen and diborane are used for diamond growth and boron doping control.

Recipe parameters for the growth of p+ layer and p- layer are illustrated in Table 2.1. During growth, the thin film's parameters such as thickness and doping concentration are followed by the in-situ ellipsometry spectroscopy [81]. More details on diamond epilayer growth and doping controlled can be found in the Fiori's PhD thesis [4].

After growth, diamond surface topography is characterized by different methods. Figure 2.6a represents the surface topography measured by optical profile-meter. Figure 2.6b

[1] http://neel.cnrs.fr

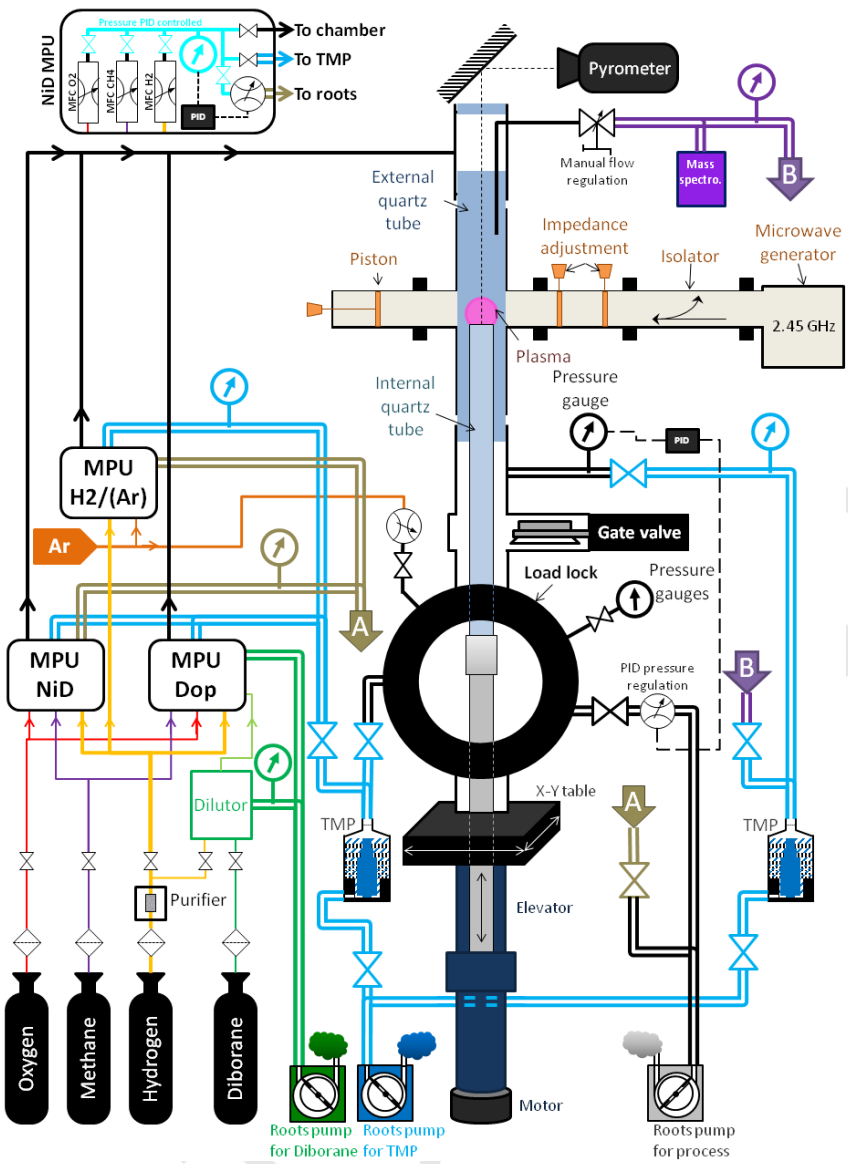

Figure 2.5: Schematics representing the structure and the working principle of the reactor. Courtesy to Fiori's PhD thesis [4]

layer	Pres (Torr)	Temp (°C)	Power (W)	B/C (ppm)	CH_4 (sccm)	H_2 (sccm)	O_2 (sccm)	[B] (cm^{-3})
p^+	33	830	240	1200	7.6	200	0	$5x10^{20}$
p^-	33	870	270	600	1	100	0.25	$2x10^{17}$

Table 2.1: Conditions for growth of metallic diamond (p+) and moderate boron doped diamond (p-).

represents the surface topography measured by Atomic Force Microscope (AFM). From both measurements, the surface Root Mean Square (RMS) are generally found less than 1 nm. On the top of diamond surface, there are remarkable defect structures. More details

on the features of defective structures and their correlation with electrical characteristics of test devices will be addressed in the part 3 of this chapter.

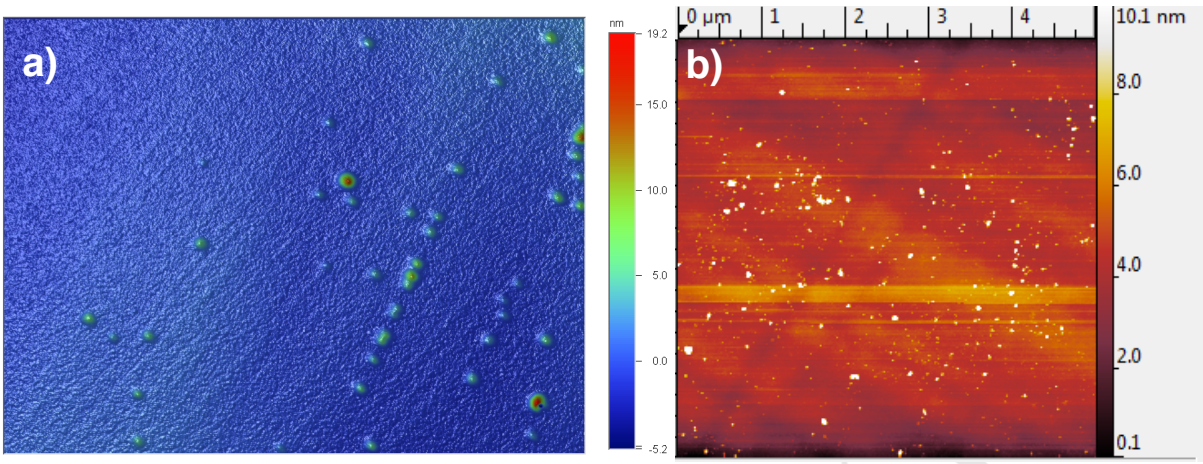

Figure 2.6: Diamond surface topography after growth measured by a) Optical profilemeter; b) AFM.

2.1.4 Test devices fabrication

Figure 2.7 represents the fabrication processes for etching p- layer and ohmic contact deposition.

The corresponding top view structure for each step is also given. Photoresist (S1805) is firstly coated on top of the substrate by using spin coating. A Heldelberg DWL66FS laser lithography instrument is employed to define contact area, as shown in Fig. 2.7a. MF26 developer is used to develop the photoresist. A plasma etching of 30 s is subsequently employed to eliminate the residual photoresist. Plassys ebeam evaporator is employed to deposit a 150 nm Nickel (Ni) mask layer on the defined region, as shown in Fig. 2.7b. The Plassys Reactive Ion Etching (RIE) with a manual process (average etching rate of 40 nm/min) is used for etching p- layer, as shown in Fig.2.7c. After etching, the Ni mask is removed by immerse into aqua-regia solution at 250°C during 30 min. The etched thickness is confirmed by optical profile-meter and mechanical scanning Dektak, as shown in Fig.2.8.

Figure 2.9 represents the test devices (MOS capacitors and MIM capacitors) fabrication processes. In order to replace the hydrogen terminated layer by the oxygen terminated layer, we employed the Deep Ultra Violet (DUV) ozone technique [79]. The DUV ozone treatment is illustrated in Fig. 2.9a. Al_2O_3 gate oxide was then deposited on top of the O-diamond by Atomic Layer Deposition (ALD) method by using a Savannah 100 ALD system from Cambridge Nanotech, as shown in Fig. 2.9b. This deposition method consists in sequential exposure of diamond surface to precursor Trimethylaluminium (TMA) and oxidant water. The pulse and exposure duration were 15 ms and 30 s, respectively. Chamber pressure is typically set as 1.3×10^{-1} (torr). Since there is no photoresist involved during the ALD deposition, the chamber temperature can be increased as high as desirable, in the limit of the equipment. During this thesis, two deposition temperatures were used: 250°C and 380°C (limit of our ALD equipment). After the

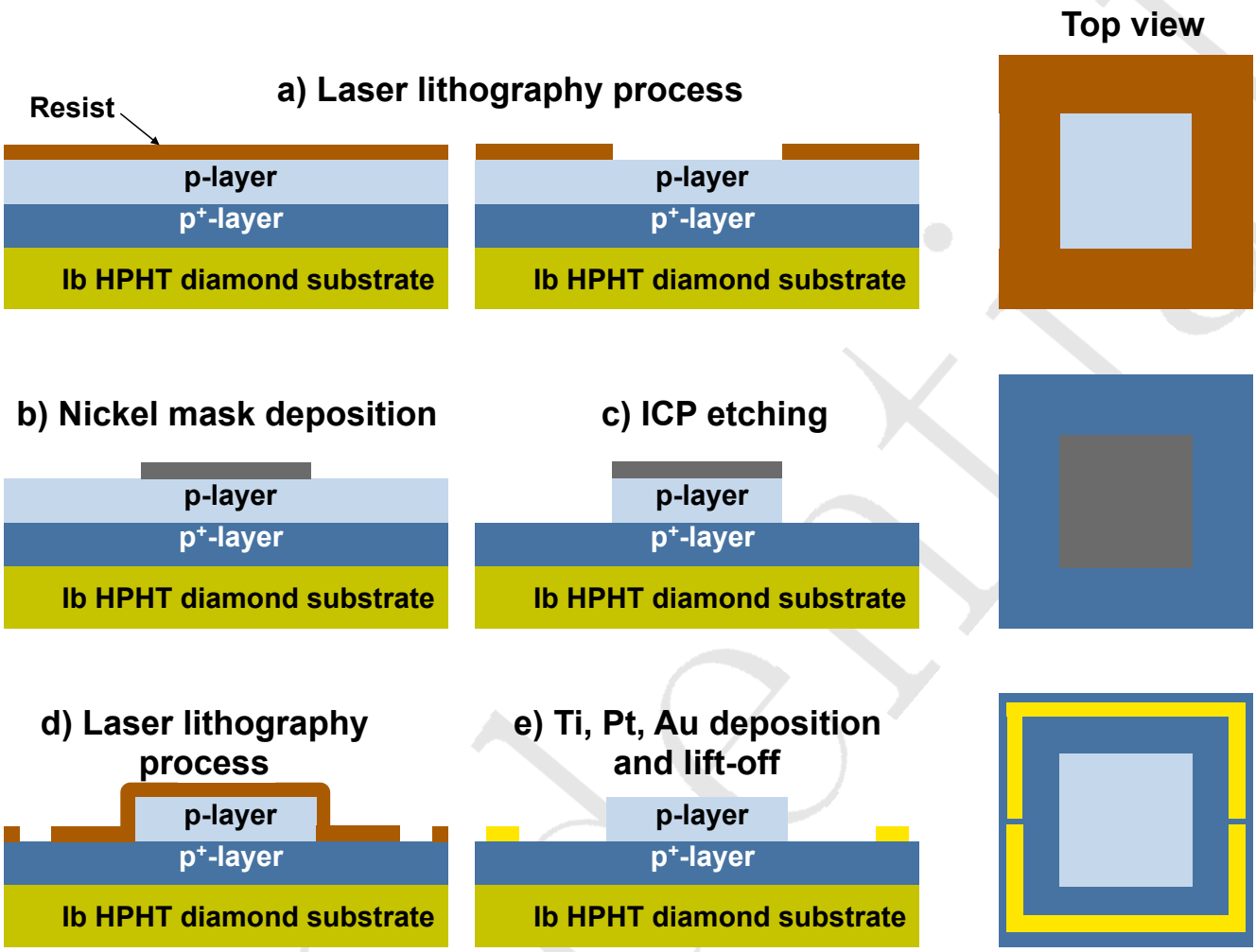

Figure 2.7: Schematics describing the process for diamond etching and ohmic contact fabrication.

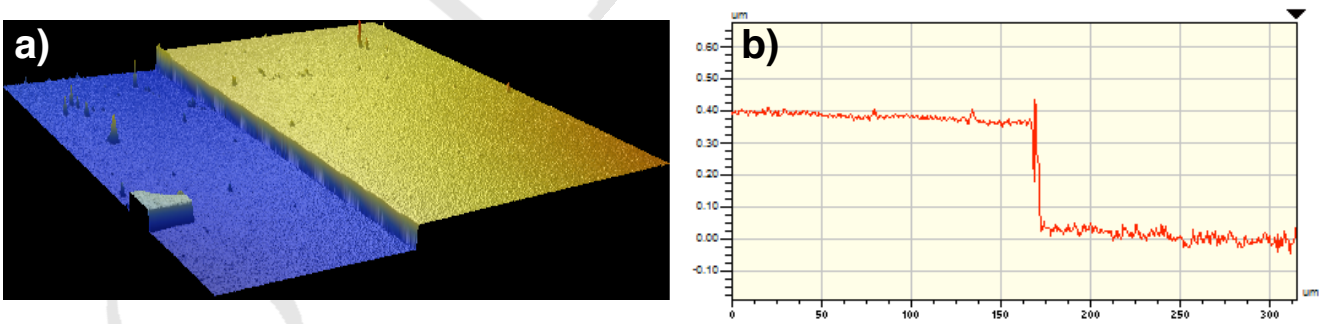

Figure 2.8: a) Optical profile-meter of the etched mesa structure.

gate oxide deposition, the sample is going through a new laser lithography process. This new lithography process allows to define the contact area of MOS capacitors and MIM capacitors, as shown in Fig. 2.9c. Metal gate is then deposited by using Plassys ebeam evaporator. Finally, a lift-off process in acetone is performed to remove the photoresist, as shown in Fig. 2.9d.

During my PhD, I have fabricated 7 test devices dedicated to investigate the O-

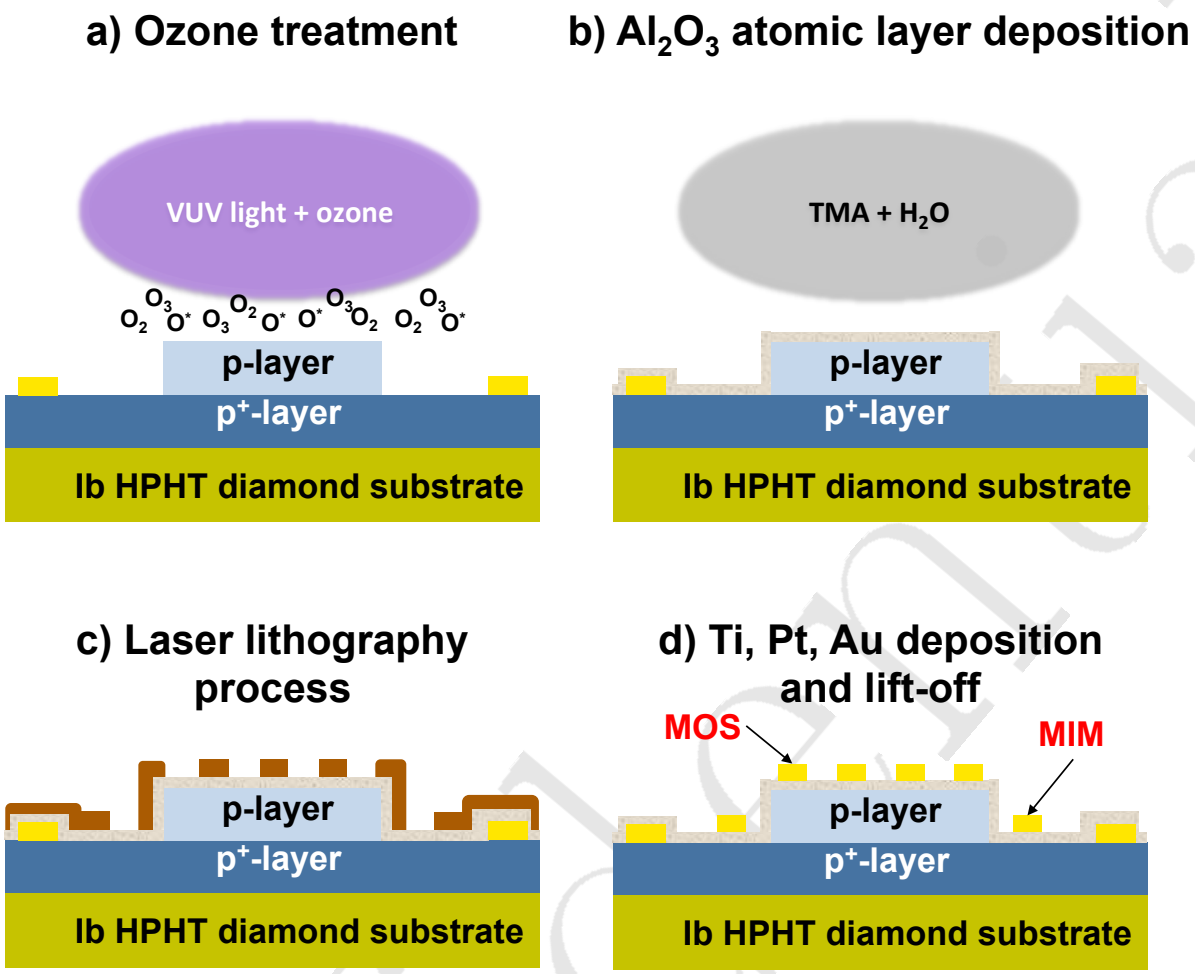

Figure 2.9: Schematic describing MOS capacitors and MIM capacitors fabrication steps.

diamond MOS capacitor. Table 2.2 summarizes the processing details of the fabricated samples studied in this work.

Sample	p- thickness (nm)	Oxide thickness t_{ox} (nm)	Surface treatment	ALD temperature (°C)	Metal electrode	Annealing
#1	600	20	DUV	250	Ti/Pt/Au	NA
#2	300	10	DUV	250	Ni	NA
#3	300	20	DUV	380	Ti/Pt/Au	500°C-VC
#4	400	40	Chemical treatment	380	Ti/Pt/Au	NA
#5	400	40	DUV	250	Ti/Pt/Au	NA
#6	400	20	F- termination	250	Ti/Pt/Au	NA
#7	400	20	DUV	380	Pt/Au	FGA 450°C

Table 2.2: Processing conditions for fabricating test devices during this thesis. DUV indicates deep UV ozone treatment. F-termination indicates the fluorine termination. FGA indicates Forming Gas Annealing.

Figure 2.10 represents the optical photograph of sample #1. MOS capacitors, MIM

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capacitors and ohmic contact are delineated for an eye guiding. The MOS capacitors are then numbering for the systematic measurement and comparison. Figure 2.10b represents the MOS capacitor mask after numbering.

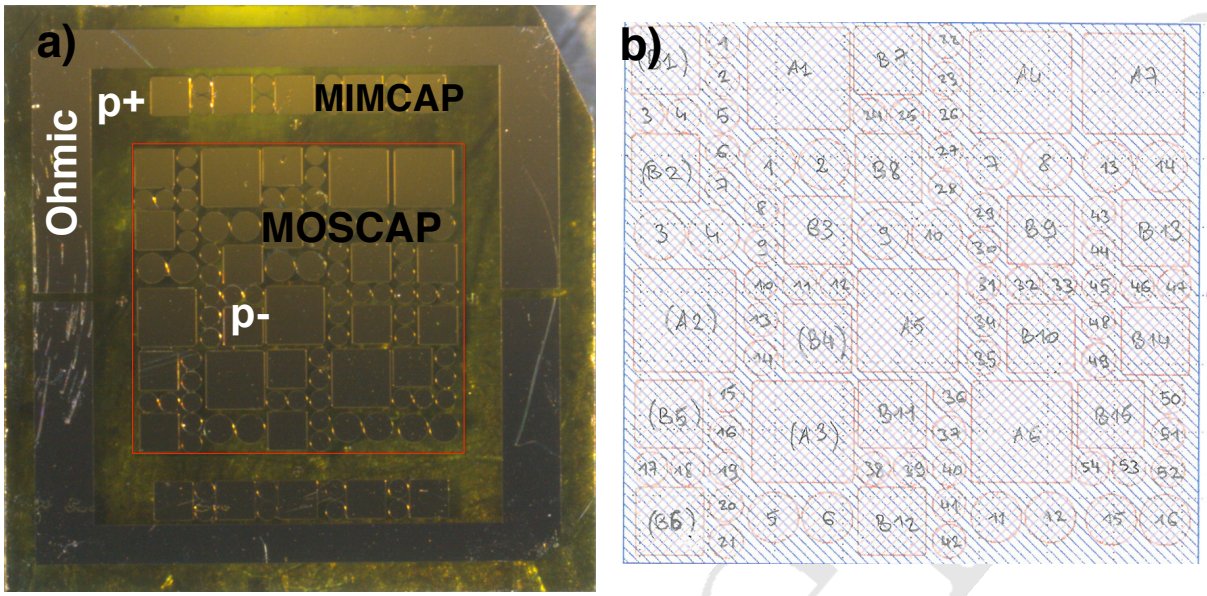

Figure 2.10: a) Optical photograph of the fabricated test devices included Ohmic contact, MIM capacitors and MOS capacitor. b) the mask of MOS capacitor after numbering.

2.1.5 Electrical measurement

2.1.5.1 Experimental set-up

For electrical characterization, tungsten tips were used to probe the contact pads. Ohmic contacts were grounded and potential were applied on top of the test devices, as shown in Fig. 2.11a. Current-Voltage (I-V) characteristics were measured thanks to Keithley 2611, Keithley 6517B electrometer and Solartron Modulab.

For the a.c measurements (impedance/admittance/capacitance), a small a.c signal with an amplitude voltage of V_{ac}=20 mV is superimposed the DC signal (Fig. 2.12a).

Electrical measurements were performed thanks to the electrical characterization platform in our group, as shown in Fig. 2.11b.

2.1.5.2 Capacitance-frequency measurements

Small signal a.c measurements were performed by ModuLab XM MTS [2]. One of the most remarkable feature of this equipment is the concept of multisine/Fast Fourier Transform (FFT) impedance measurement in a wide frequency range (from μHz to MHz). Figure 2.12b represents the Solartron modulab and the accessories in our lab.

As shown in Fig. 2.12a, in order to measure the impedance of a system, a small sine wave a.c voltage is superimposed to the input in order to measure the a.c current at the output. To examine the response of a system against frequency, one usually performs different single measurements at different fixed a.c frequencies (i.e. C-V at different

[2]http://www.ameteksi.com/products/materials-testing-systems/modulab-xm-mts

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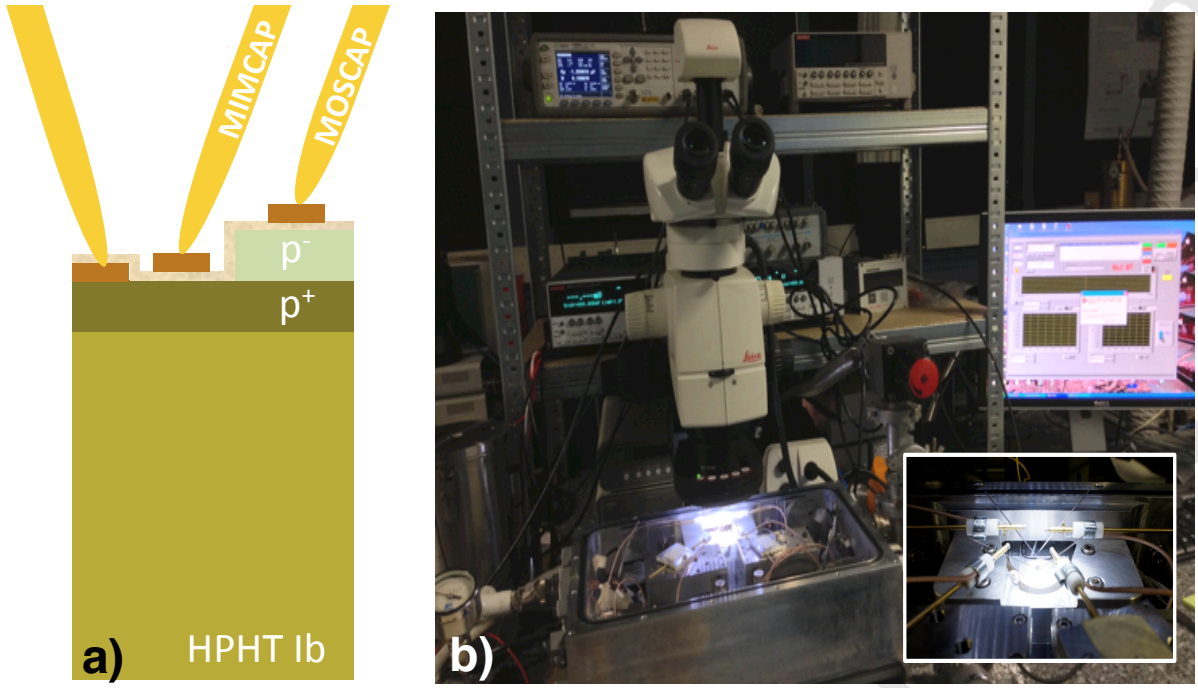

Figure 2.11: a) General electrical measurement configuration; b) Electrical measurement platform at Wide bandgap Semiconductor Group (SC2G)- Institut NEEL

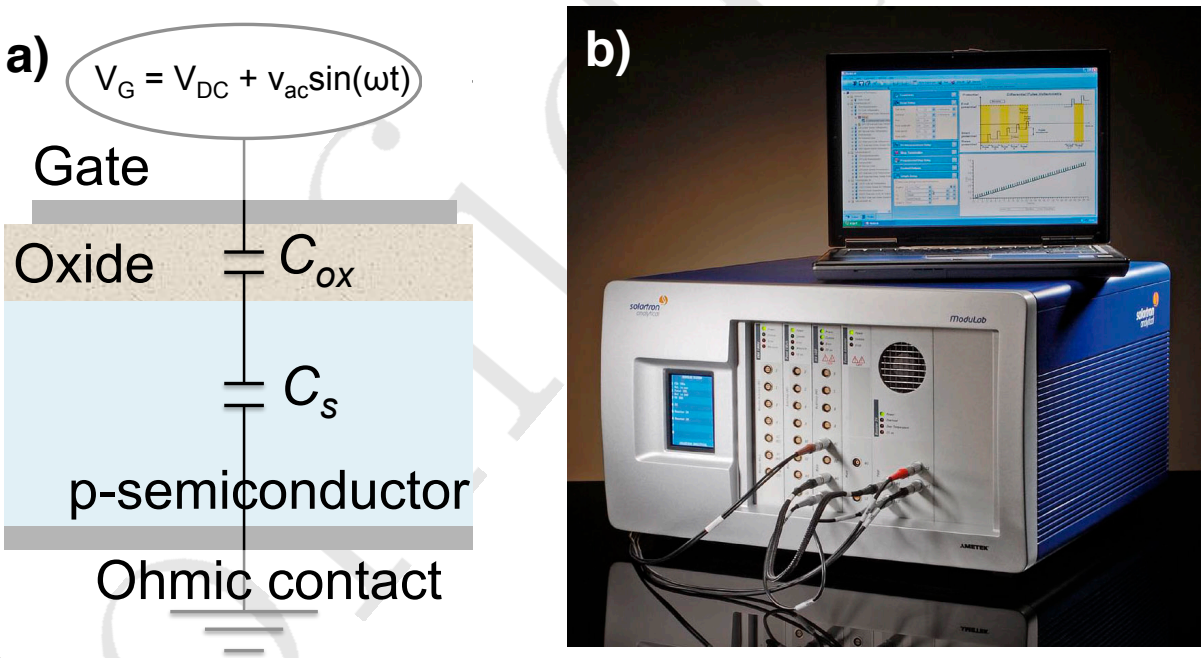

Figure 2.12: a) Impedance measurement configuration; b) Solartron modulab and the accessories

frequencies) by using LCR impedance analyzer. This measurement can introduce some sources of errors, especially the degradation of the sample with different biasing cycles. For instance, DC current can be changed after several C-V measurements. Another problem with LCR impedance analyzer system is the low cut-off frequency (around 1 kHz). Therefore, it's usually difficult to perform the impedance measurement at the

frequency lower than 1 kHz.

The multisine/FFT concept is based on generating and composing different sine waveforms into one measurement, as shown in Fig. 2.13. After that, by using the fast Fourier transform technique, the data on time domain (voltage and current samples collected over a period of time) are converted into the frequency domain (analyzing the frequency content of the signal and presenting impedance v.s frequency data). By using this concept, we are able to measure the response of a system against a wide frequency range, at different fixed gate bias. This is the C-f measurements that we will present in the following parts.

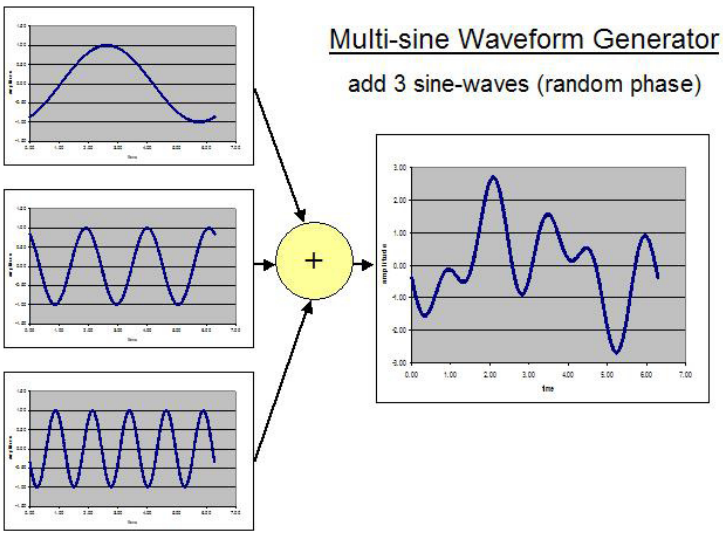

Figure 2.13: Multisine waveforms concept of Solartron Modulab

Since the a.c measurement is performed at fixed gate bias, there is no DC degradation due to the biasing cycles. It is worth mentioning that this measurement in fact took a few seconds to be completed. Therefore, C-f measurement is appropriate to examine the response of a system against frequency. In our a.c measurements, we employed the frequency range from 1 Hz to 1 MHz. By further decreasing the frequency, the impedance of the system is increased rapidly while we did not observe further interesting phenomena.

2.1.5.3 Impedance measurement circuits

In principle, an impedance meter is measuring:

$$Z = Z' + jZ'' \tag{2.1}$$

where $Z' = Re(Z)$ the real part of impedance and $Z'' = Im(Z)$ the imaginary part of impedance, j is the purely imaginary complex number ($j^2 = -1$).Then, depending on the configuration used in the software, the system is able to plot different parameters like C, L or R. However, the assumptions are needed to convert $Z = Z' + jZ''$ to C, L and R. The most used circuit is the parallel circuit $C_p - R_p$, as shown in Fig. 2.14b. Admittance of this $C_p - R_p$ circuit is:

$$Y = Y' + jY'' = \frac{1}{R_p} + j\omega C_p = G_p + j\omega C_p \tag{2.2}$$

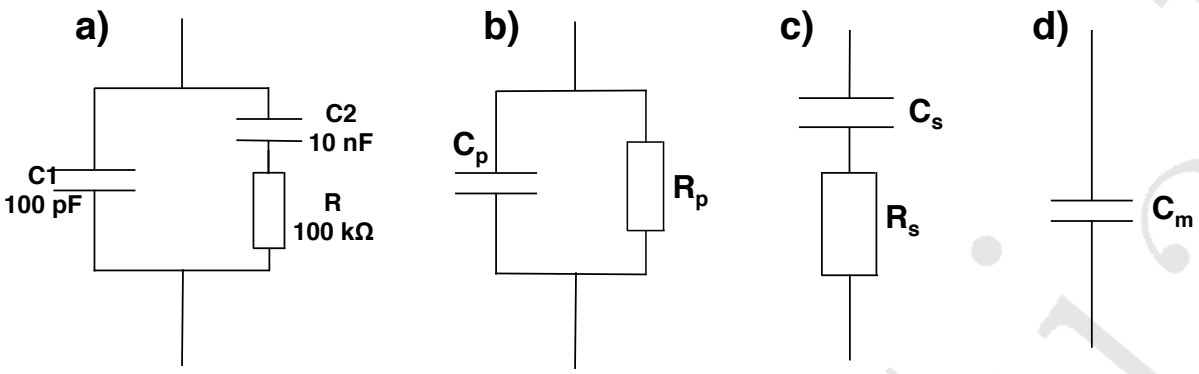

Figure 2.14: a) The calibrated test circuit provided by Ametek Scientific Instruments; b) $C_p - R_p$ circuit; c) $C_s - R_s$ circuit; d) C_m circuit.

Which is equivalent to the inverse of measured impedance. This relationship can be expressed as:

$$\frac{1}{Z} = \frac{1}{Z' + jZ''} = Y \tag{2.3}$$

By conjugate multiplication, equation 2.3 is then equivalent to:

$$Y = \frac{Z' - jZ''}{Z'^2 + Z''^2} \tag{2.4}$$

The parallel capacitance C_p and the parallel conductance G_p is then calculated as:

$$C_p = \frac{Z''}{Z'^2 + Z''^2}\frac{1}{\omega} \tag{2.5}$$

$$G_p = \frac{Z'}{Z'^2 + Z''^2} \tag{2.6}$$

By using the series $C_s - R_s$ configuration (Fig. 2.14c), the series capacitance C_s and series resistance R_s can be directly evaluated as:

$$C_s = \frac{1}{\omega Z''} \tag{2.7}$$

$$R_s = Z' \tag{2.8}$$

For C_m configuration (Fig. 2.14d), the measured impedance is considered to be purely capacitive and C_m can be calculated as:

$$C_m = \frac{1}{|Z|}\frac{1}{\omega} \tag{2.9}$$

We employed the calibrated test circuit (Fig. 2.14a) provided by Ametek Scientific Instruments to determine the measurement circuit used by Solartron Modulab.

The measured capacitance of the calibrated test circuit is compared with different measurement configuration, as shown in Fig. 2.15. This measurement illustrates that Solartron Modulab is using the C_m configuration (Fig. 2.13d) to measure the capacitance. The data can be converted to parallel circuit $C_p - R_p$ or series circuit $C_s - R_s$ by the above procedure (Fig. 2.15).

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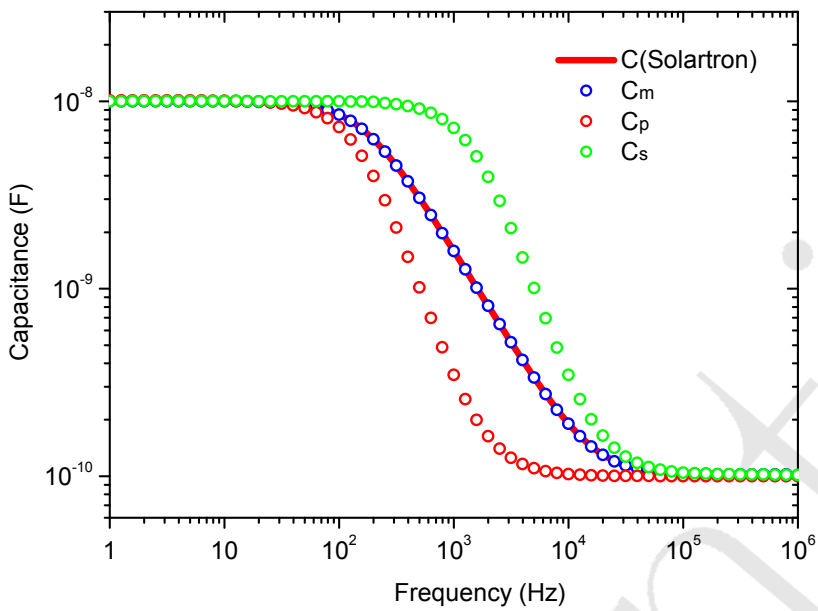

Figure 2.15: Capacitance-frequency characteristic of the calibrated test circuit by using different measurement configurations

2.1.6 Electrostatics simulation

To visualize the electrostatics properties (electric field distribution, potential distribution, band bending) of a MOS capacitor response to gate bias, the electrical measurements are not sufficient. In this context, an electrostatics simulation is highly desired. We employed the Nextnano software [3] to perform the finite element electrostatics simulation.

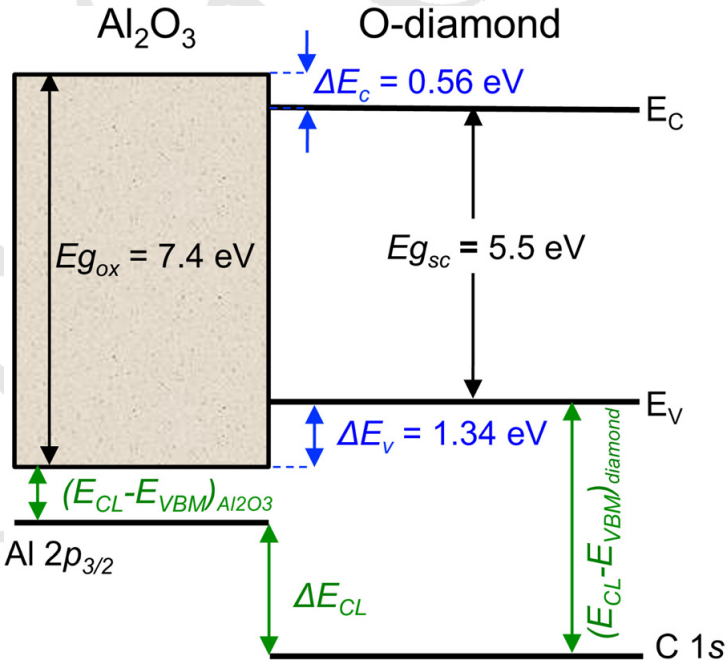

Figure 2.16: Band alignment input configuration for nextnano electrostatics simulation [19].

[3] http://www.nextnano.com/index.php

In order to have the simulations as accurate as possible, the empirical input parameters are highly desired. One important parameter for electrostatics simulation is the O-diamond/oxide band alignment. As mentioned in the first chapter, this parameter has been determined by Marechal et al. [19]. Figure 2.16 represents the type I band alignment between O-diamond and Al_2O_3 that we have implemented into our simulations.

In the following sections, by different experimental approaches, we will gradually determine the parameters for an empirical electrostatics simulation. The simulation results will be compared to experiment results by mean of semiconductor surface potential Ψ_s.

2.1.7 C-V characteristic of an ideal MOS capacitor

We firstly present the C-V characteristics of an ideal p-type Si/SiO_2 MOS capacitor. In ideal case, a MOS capacitor includes two capacitors in series: oxide capacitor C_{ox} and semiconductor capacitor C_{sc}. This ideal configuration is important to examine the response of semiconductor versus gate bias. Under negative bias, semiconductor surface

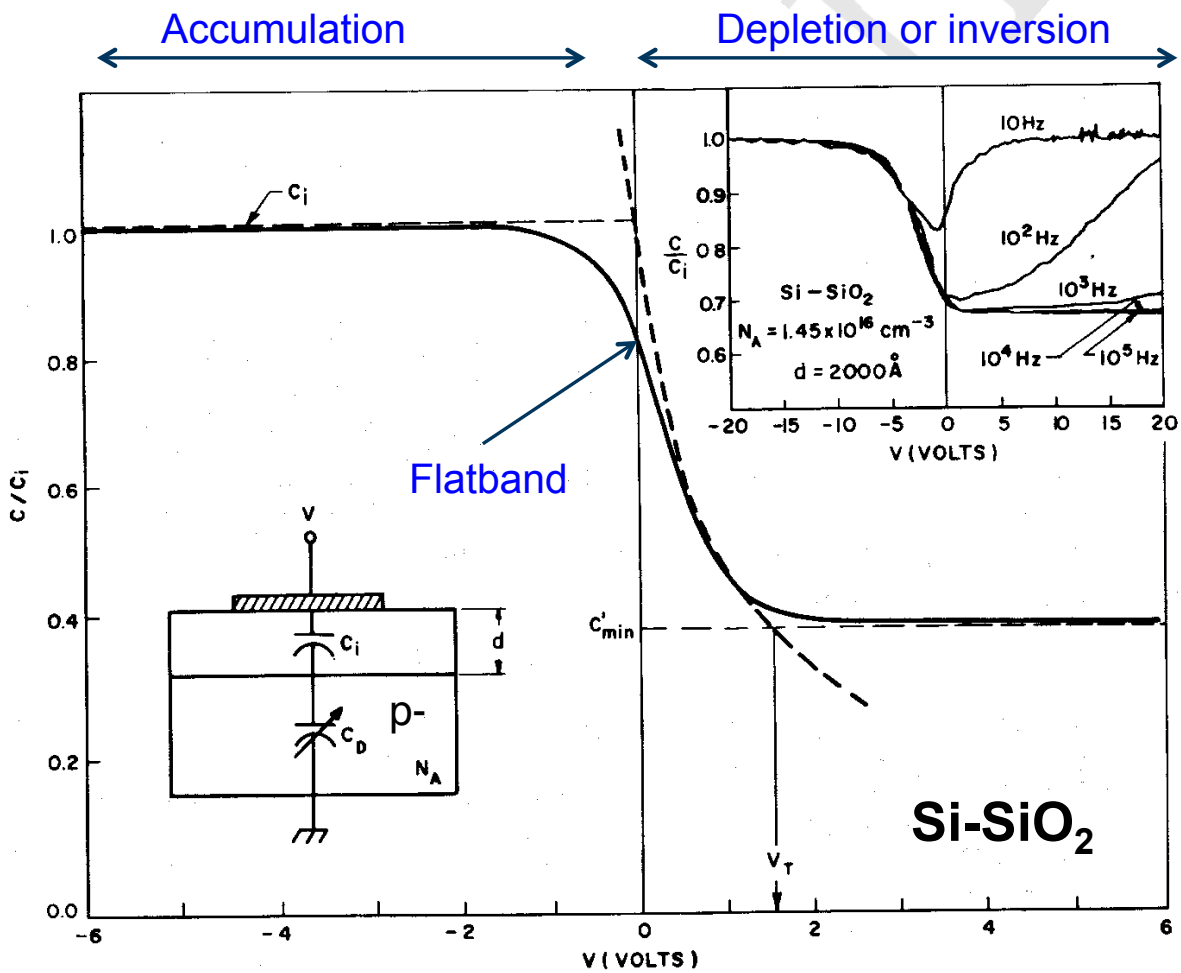

Figure 2.17: Typical Capacitance-Voltage characteristics of an ideal MOS capacitor

potential Ψ_S is bent upward, semiconductor charge is exponentially dependent to semiconductor surface potential Ψ_S [17]. The surface of semiconductor is like a metal. MOS capacitor is in accumulation regime (Fig. 2.17) with a capacitance value equivalent to the oxide capacitance C_{MOS}=C_{ox}.

By sweeping the gate potential from negative bias of accumulation regime toward positive bias, semiconductor is driving toward depletion regime (Fig. 2.17). In depletion regime, semiconductor Space Charge Region (SCR) width and corresponding semiconductor capacitor C_{sc} will be created. Capacitance of the MOS capacitor is equivalent to series oxide capacitor and semiconductor capacitor $C_{MOS} = \frac{C_{ox}C_{sc}}{C_{ox}+C_{sc}}$.

By further biasing in positive direction, semiconductor reaches inversion regime once $\Psi_s > 2\Psi_b$ where Ψ_b is the bulk potential. Capacitance of the MOS capacitor is now depending on applied frequency. At high frequency, $C_{\min}$ value is obtained since the SCR extension is now negligible. Once the applied frequency is equivalent or lower than the minority carriers generation time constant (see the discussion below), inverted minority carriers will be able to participate to the differential capacitance. Measured capacitance will increase with the decrease of frequency, as shown in the top inset of Fig. 2.17. Once the applied frequency is sufficiently low, all minority carriers accumulate at the oxide/semiconductor interface. The surface of semiconductor is again like a metal with the inverted carriers. Capacitance of the MOS capacitor will be equivalent to the oxide capacitance $C_{MOS} = C_{ox}$.

In Si/SiO_2 MOS capacitor, the ideal C-V characteristics are obtained experimentally thanks to the low interface states density at Si/SiO_2 interface, i.e. the order of 10^{10} ($1/eV.cm^2$). In any other MOS capacitor test devices, once the interface states density at oxide/semiconductor interface is high, numerous problems can be generated. Probably, the most serious problem is the lack of control of semiconductor population by gate bias. Subsequently, MOSFET will not work or it will work in an uncontrolled manner. Interface states also affect the C-V measurements of MOS capacitor test devices at different frequencies (see the discussion below). Therefore, interpreting the measurements will be challenging and bearing some possible of misinterpretations.

Along with interface states, there are also different potential artifacts that can affects the MOS capacitor test devices measurements, i.e. oxide fixed charges, oxide mobile charges, series resistance, gate leakage current, and even the combinations among them. Therefore, distinguishing the artifacts and their origin, and accurately quantifying them are crucial for a comprehensively understanding as well as any further improvement. This is the ultimate methodology of this chapter, which is dedicated to the understanding of the O-diamond MOS capacitor test devices. We will firstly examine the general electrical behaviors, distinguish the contributions from artifacts and refine our examination windows. Then, we will gradually quantify the artifacts which could potentially affect our device. Finally, the empirical simulation will be performed to compare with experimental results.

2.2 Electrostatics of O-diamond MOS capacitor

2.2.1 I-V and C-V characteristics

Hereinafter, we will mostly present the results measured from MOS 12, sample #1 (Fig. 2.10). Thanks to the systematic measurements that will be presented later, we show that these measurement results are general, scalable and reproducible.

Figure 2.18a represents the DC I-V characteristics when the gate is biasing from +8V to -8V. We define the biasing in negative direction (0V to -8V) is the forward bias and

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the biasing in positive direction (0V to +8V) is the reverse bias (p-type semiconductor). Forward current and reverse current are the DC current measured for forward bias and reverse bias, respectively. A similar specification is also applied to C-V measurement.

As shown in Fig. 2.18a, the forward current is clearly observed. This behavior is similar to the previous reports [18, 20, 19]. One noticeable improvement in this work compared to previous works [18, 20] is the current density. The leakage current is about two orders of magnitude lower than previous reports [18, 20]. We assign this improvement to the improved Al_2O_3 being deposited at high temperature (250°C). For this MOS capacitor, reverse current is under detection limit. However, this behavior is not general. We will address the reverse current issues in the part 3 of this chapter.

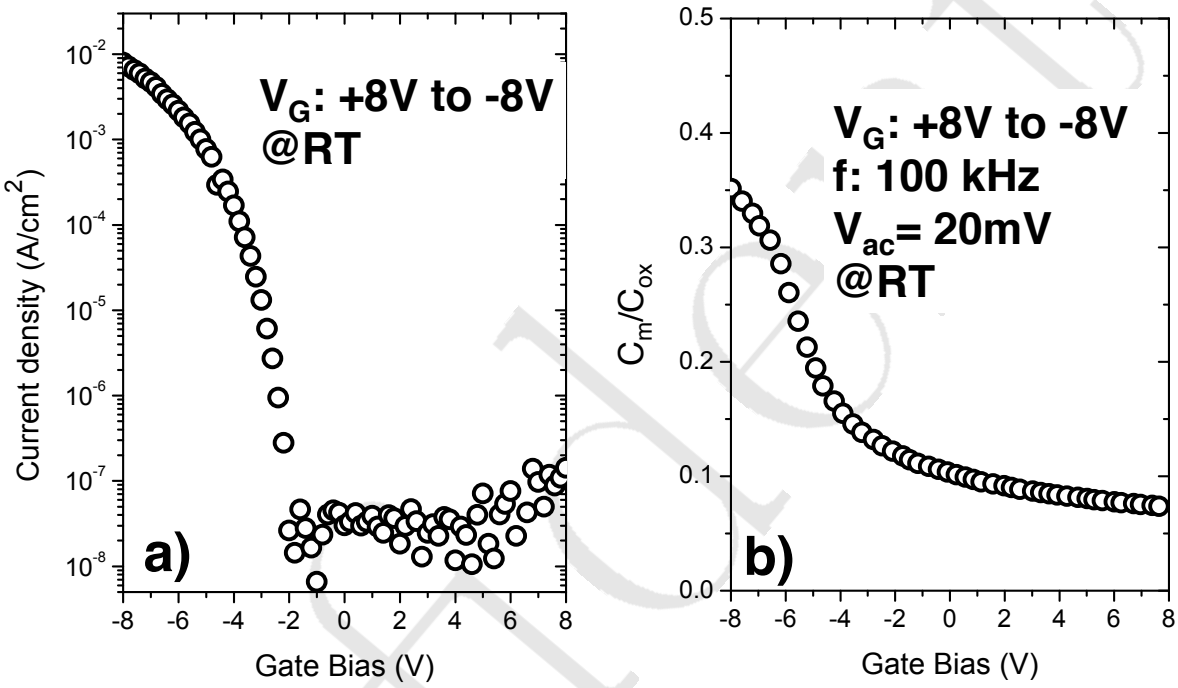

Figure 2.18: a) Typical I-V characteristics of O-diamond MOS capacitors for -8V$\leq V_G \leq$ +8V; b) C-V characteristics of O-diamond MOS capacitor measured by biasing V_G : +8V to -8V at f=100 kHz and V_{ac}=20 mV (MOS12 - Sample #1)

Figure 2.18b represents the C-V characteristic by applying the bias at same range as in I-V measurement. The superimposed a.c frequency is f = 100 kHz and the amplitude V_{ac}=20 mV. We remind that the V_{ac} = 20 mV is constantly used for all a.c measurements in this thesis. A maximum measured capacitance of $C_m = 0.135\mu F.cm^{-2}$ at $V_G = -8$ V has been obtained. Measured capacitance has been normalized to the oxide capacitance C_{ox} in Fig. 2.18b. C_{ox} was measured from MIM capacitor test devices on the same substrate.

Figure 2.19 represents the measured capacitance of MIM capacitor at a fixed gate bias ($V_G = -3$ V) versus frequency (1 Hz to 1 MHz) (Fig. 2.19a) and at a fixed frequency (f=100 kHz) versus gate bias (+4 V to -4 V) (Fig. 2.19b). For an oxide thickness of t_{ox} = 20 nm, measured oxide capacitance is about 0.4 $\mu F/cm^2$. Oxide dielectric constant of $\varepsilon_{ox} \simeq 9$ was evaluated. This dielectric constant is approximately the value reported in literature for the ALD Al_2O_3 [82].

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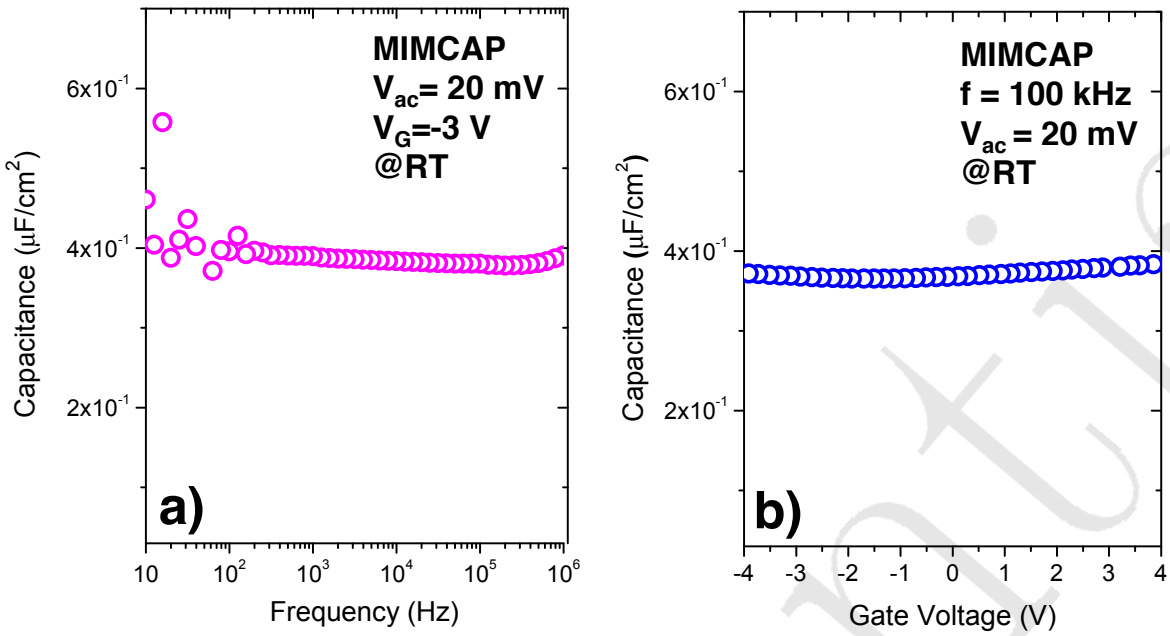

Figure 2.19: Measured capacitance of MIM capacitor by a) Capacitance-Frequency at $V_G = -3V$; b) Capacitance-Voltage at f=100 kHz.

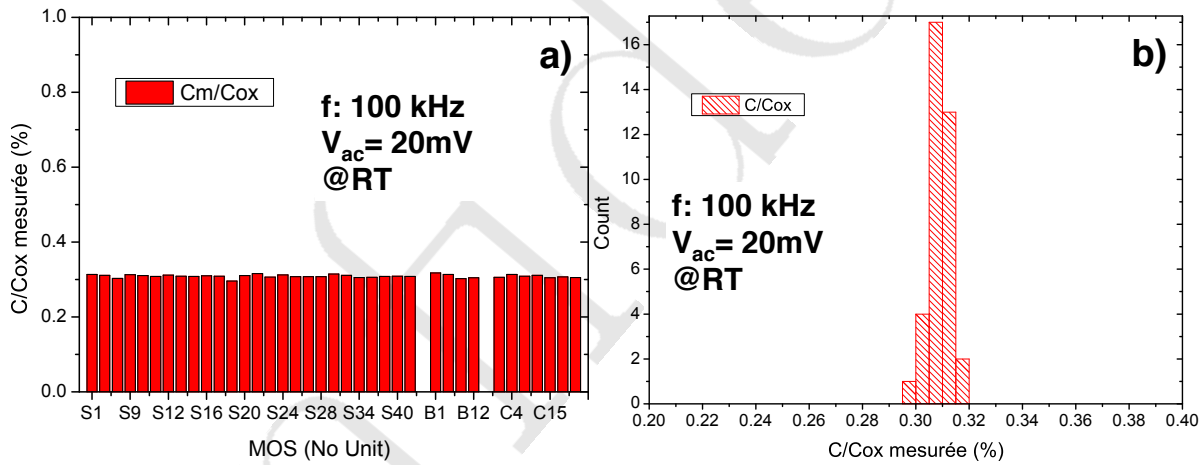

Figure 2.20: Systematic measurements demonstrate the general and reproducible of the C-V characteristics (Sample #3)

From the measured capacitance of MOS capacitors and MIM capacitors, we highlight some notable differences between the C-V characteristic of O-diamond MOS capacitor compared to the C-V characteristic of the ideal Si/SiO_2 MOS capacitor:

1. Under forward bias where we expect the accumulation ($C_{MOS} = C_{ox}$), the measured capacitance is much lower than oxide capacitance $C_m << C_{ox}$. The systematic measurements [4] have demonstrated that this behavior is general for all measurable 38 MOS capacitors on one substrate, as shown in Fig. 2.20. The measured capacitance values are also in good scaling with device areas, as shown in Fig. 2.21.

[4]done by D. Valenducq, a master 1 internship from University Grenoble Alpes at SC2G, Institut NEEL

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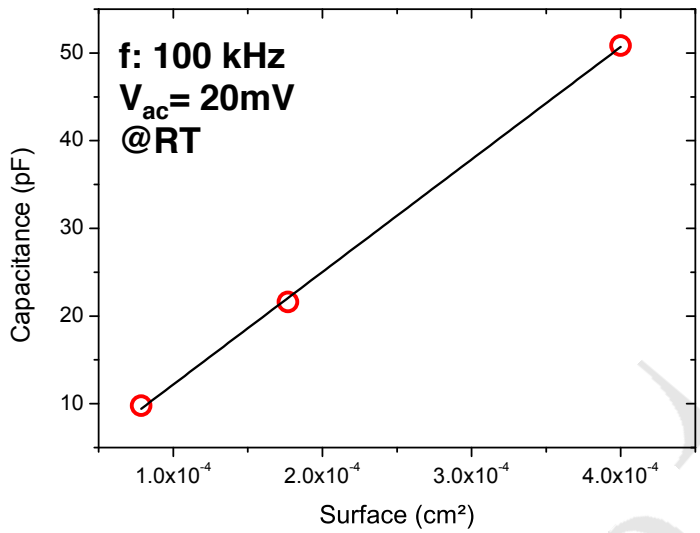

Figure 2.21: Scaling of maximum measured capacitance versus the MOS capacitor surface area (Sample #3).

2. The measured capacitance in reverse regime does not show the saturation of minimum capacitance C_{min}. As long as a more positive bias is applied (up to +14 V, sample 1), the measured capacitance is further decreased.

3. By switching the bias direction, from (+8V to -8V) to (-8V to +8V), the C-V characteristics are almost identical, as shown Fig. 2.22. We conclude the contributions from mobile oxide charges in this MOS capacitor are negligible.

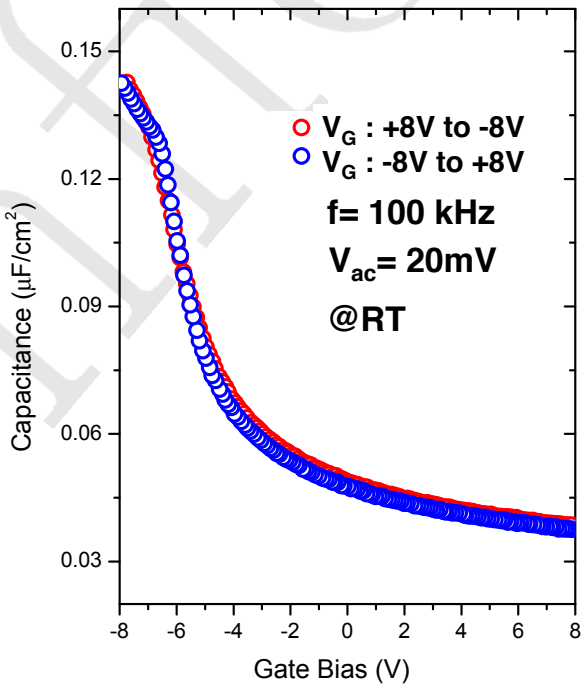

Figure 2.22: The hysteresis C-V characteristics of sample 1 measured by switching the bias direction, from (+8V to -8V) to (-8V to +8V) to estimate the mobile oxide charge (MOS45-Sample #1).

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4. By varying the frequency, measured capacitance of this MOS capacitor has shown different features. In the next section, we will discuss the capacitance-frequency characteristics of O-diamond MOS capacitor under negative bias.

2.2.2 Capacitance-frequency characteristics

As defined in previous section, $C - f$ measurement is performed by fixing the gate bias and sweeping the frequency. By that method, we are able to examine the response of the system versus frequency. Figure 2.23 represents the measured $C_m - f$ characteristics at $V_G = -8V, -4V, -2V$, respectively. Figure 2.23b represents the corresponding conductance-frequency $G_p - f$ characteristics from the same measurement, with $G_p = \frac{1}{R_p}$ from Fig. 2.14 b.

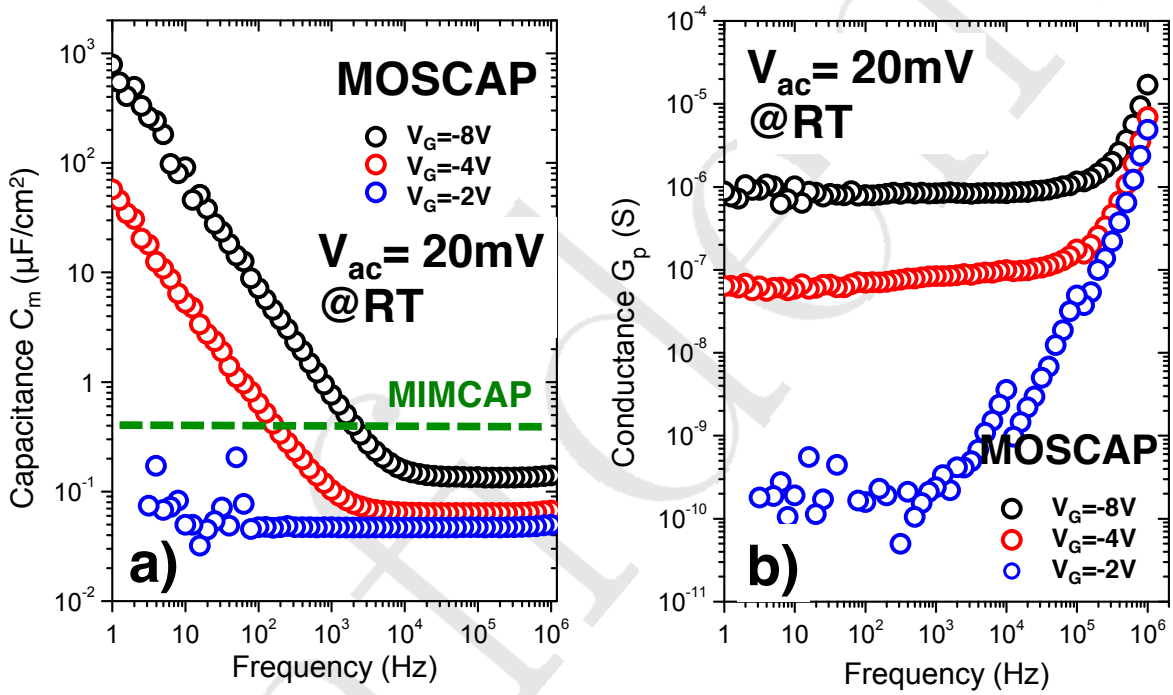

Figure 2.23: a) Capacitance-frequency characteristics at V_G=-8V, -4V, -2V; b) Conductance-frequency ($G_p - f$) characteristics obtained from the same measurement (MOS12-sample #1).

Figure 2.23 demonstrates that both measured capacitance C_m and measured conductance G_p are frequency dependent.

We will now consider the capacitance-frequency characteristics. A special interest is paid to capacitance-frequency dependent behavior. As it is well-known, series resistance and interface states are usually responsible for this effect [83].

2.2.2.1 Series Resistance

As discussed in Chapter 1, a remarkable problem with diamond is the depth of dopant levels and the consequently incomplete ionization. Diamond with a moderate doping

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concentration at RT will have low free carrier density. Subsequently, the epilayer is highly resistive.

Once series resistance is considerable, equivalent circuit of the MOS capacitor is shown Fig. 2.24a. This equivalent circuit is equivalent to the series circuit $C_s - R_s$ in Fig. 2.14c if we convert series capacitors C_{ox} and C_{sc} to C_S. At high frequency, impedance of the capacitors is decreasing ($Z_C = \frac{1}{j\omega C}$). As a result, measured impedance $\left(Z_{(\omega\to\infty)} = R_s + \frac{1}{j\omega C_s} \simeq R_s\right)$ and consequently, measured capacitance C_m $\left(C_{m(\omega\to\infty)} = \frac{1}{\omega Z} = \frac{1}{\omega R_s}\right)$ is actually originated from series resistance.

From the C-f curves in Fig. 2.23a, we conclude that the series resistance effect at high frequency (1 MHz) is not important. Only a small capacitance variation is observed in this frequency range.

Series resistance can be quantified by using the impedance spectroscopy. As mentioned above, at high frequency, the capacitors are "shorted" and the real part of impedance Re(Z) is equivalent to series resistance $Re(Z) = R_s$. From Nyquist plot $Re(Z)$ vs. $Im(Z)$ (Fig. 2.25a) and $Re(Z)$ vs. f plot (Fig. 2.25b), a series resistance of $R_s = 702\ \Omega$ was extracted.

Another potential problem from series resistance in our MOS capacitor is the voltage drop in p- epilayer. For a highly resistive epilayer, the potential drop on epilayer could be elevated when the device is under high injection regime/high leakage. This potential drop could limit the gate bias possibility to modulate the semiconductor in high injection regime. Therefore, series resistance could be the origin of the $C_m << C_{ox}$ effect we observed in the C-V curve (Fig.2.18b).

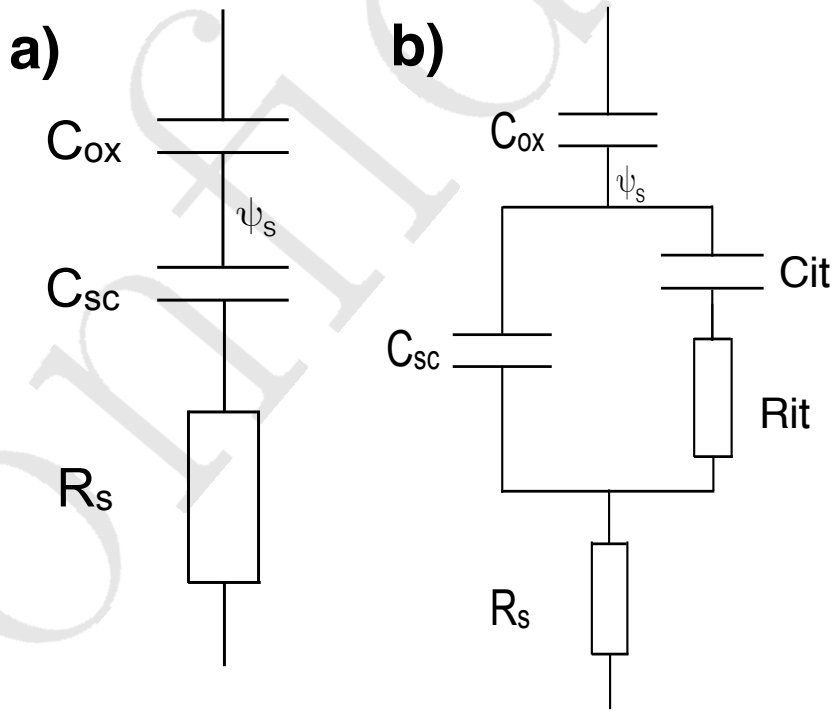

Figure 2.24: Equivalent circuit of a MOS capacitor system in case of a) high frequency regime; b) taking into account the contribution from interface states

By using the series resistance quantified from Nyquist plot and the DC I-V characteristic in Fig.2.18a, a potential drop on series resistance ($V_s \simeq R_s \times I_{DC} \simeq 1$ mV at

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$V_G = -8V$) is evaluated.

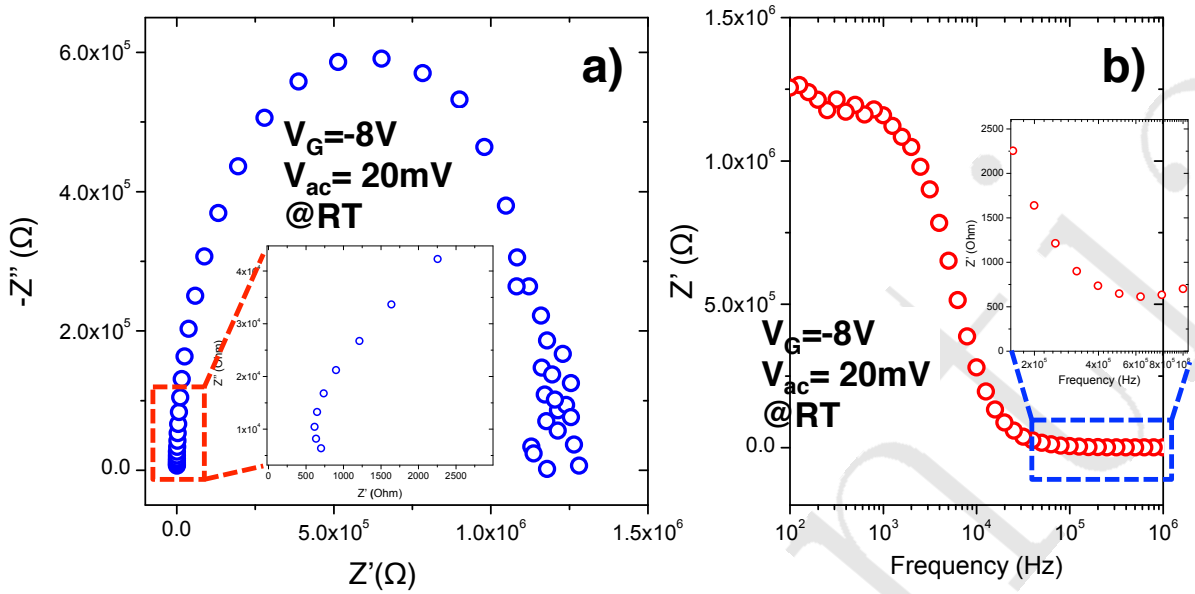

Figure 2.25: a) Nyquist plot (Re(Z) versus Im(Z))of impedance measurements; b) Real part impedance Re(Z) versus frequency (MOS12-sample #1).

We conclude that the series resistance has no considerable effects on our pseudo-vertical O-diamond MOS capacitor test device. This is achieved thanks to the metallic diamond p++ layer, as demonstrated in Fig. 2.1b.

2.2.2.2 Interface State

Interface imperfections generally leads to localized states in the bandgap of semiconductor located at the interface between oxide/semiconductor interface. Interface states communicate with semiconductor conduction band (E_C) and/or valence band (E_V) by capture and/or emission of free carriers [84]. In a MOS capacitor, interface states can have both a.c effects and DC effects.

For the sake of simplification, we firstly consider a single level interface state with density N_{it} located at $E_{it} - E_V$ in a p-type semiconductor. Electron occupancy function of the trap states is described by Fermi-Dirac function:

$$f = 1/\left[1 + \exp\left(\frac{E - E_F}{kT}\right)\right] \tag{2.10}$$

Where k is the Boltzmann constant, T the temperature and E_F the Fermi level. Communication between trap states and band edges is represented by a characteristics time constant τ. Here, we will focus on communication process of majority carriers for sake of clarification. The charge transfer process between interface states and Valence band is either the interface states capture a hole from the Valence band (capture) or interface states emit a hole to the Valence band (emission).

The emission time constant is calculated as [84].

$$\tau = \frac{1}{\sigma_p \upsilon_t N_v X_n} \exp\left(\frac{E_t - E_v}{kT}\right) \tag{2.11}$$

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Where σ_p is the capture cross section of the trap states and υ_t is the mean thermal velocity of majority carriers, X_n is the entropy factor and N_V is the density of states of valence band.

The capture time constant is described as [84].

$$\tau = [\sigma_p \upsilon_t p_s]^{-1} \tag{2.12}$$

where p_s is the hole density at the semiconductor surface.

For the a.c effect, in an ideal MOS capacitor system, interface state is modeled by a series $R_{it}C_{it}$ with a specific time constant defined as $\tau = \frac{1}{R_{it}C_{it}}$. An impedance equivalent circuit with the contribution from interface states is shown in Fig. 2.24b [85][86]. Once interface state time constant is close to the small a.c signal frequency $f \simeq \frac{1}{2\pi\tau}$, [87], interface states start to contribute to the total measured impedance. The measured impedance and subsequently measured capacitance will be deviated by this contribution. Depending on interface states density, by further decreasing the frequency, more interface states will be able to contribute to the total impedance. Hence, capacitance of the system will increase until all the interface states are able to respond to the a.c signal. This is the idea of high-low frequency method [88] to quantify the interface states density. Therefore, interface states can be the origin of the capacitance-frequency dependence at low frequency.

Along with interface state, there are also different artifacts which could affect the capacitance measurement at low frequency range. For example, in III-V/high-k MOSCAP system, the capacitance frequency dependence is assigned to either border traps [89][90] or disorder induced gap states [91][92]. DC gate leakage current can also induce the capacitance-frequency dependence at low frequency [93]. Subsequently, the C-V measurement using a "low frequency" may include many artifacts and will be strongly deviated from the ideal MOS capacitor configuration, i.e. C_{ox}, C_{sc} in series.

Along with a.c effects, interface states can also have DC effects. When Fermi level is crossing the interface state, the capture and emission are equivalent to the charge and discharge of interface states. Once interface states density is high, Fermi level needs to fully charge interface states before moving to the next energy level [94][95]. This process caused the Fermi Level Pinning Effect (FLPE) and it could be at the origin of insufficient gate control semiconductor in accumulation region ($C_m << C_{ox}$ in Fig. 2.18) .

2.2.2.3 Proper C-V measurement

From the discussions on capacitance-frequency dependence on a MOS capacitor, the following conclusions can be drawn:

1. Series resistance can affect the capacitance measurements at high frequency. However, in our pseudo-vertical MOS capacitor test devices, its contribution is minor.

2. Capacitance measurement at low frequency may include many artifacts and can be strongly deviated from an ideal MOS capacitance configuration.

In fact, all of the above analysis can be seen from the $C - f$ measurements in Fig. 2.23. At different gate bias ($V_G = -8V, -4V, -2V$), three regimes in the C-f curves can be observed:

i) High frequency (about MHz): There is a minor effect from series resistance.

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ii) Low frequency (about 10 kHz to 1 Hz for $V_G = -8V$; about 3 kHz to 1 Hz for $V_G = -4V$ and almost negligible for $V_G = -2V$): Measured capacitance is strongly frequency dependent. Capacitance is increased one decade for one decade frequency. In the previous reports on O-diamond MOS capacitor [18][20], capacitance frequency dependence of the "low frequency range" is huge. In Kovi et al. [20], the "low frequency range" is even observed up to few MHz.

iii) Proper frequency (the regime between "high frequency" and "low frequency"): the measured capacitance is constant with frequency. This frequency window is too low to be affected by series resistance and too high to be affected by interface states. In this frequency window, MOS capacitor is close to the proper MOS capacitor configuration, i.e. only includes oxide capacitor C_{ox} and semiconductor capacitor C_{sc} in series and the measured capacitor of the MOS capacitor is: $C_{MOS} = \frac{C_{ox}C_{sc}}{C_{ox}+C_{sc}}$.

Therefore, in order to examine the response of semiconductor versus gate bias, capacitance measurements are necessary to be performed in this frequency window. In this work, we systematically perform the C-f measurements to predefine frequency window for the proper C-V measurements, e.g. Fig. 2.18b. In the next section, we will examine the response of the boron doped diamond epilayer vs. gate bias as well as evaluate different charges components of the O-diamond MOS capacitor thanks to this proper capacitance measurement.

2.2.3 Charges in the MOS capacitor system

2.2.3.1 Semiconductor charges

Figure 2.26 represents the Schottky-Mott plot (reciprocal square capacitance versus gate bias plot $\frac{1}{C^2}$ vs. V_G). The term $\frac{1}{C_m^2} - \frac{1}{C_{ox}^2}$ is used to eliminate the effect from oxide capacitance [96]. The $\frac{1}{C^2} - V_G$ curve exhibits an almost perfect straight line for the gate voltage ranging from V_G=-6V to V_G=8V. From the slope of the curve, the doping concentration of semiconductor layer can be extracted by using the equation:

$$N_A = \frac{-2}{\varepsilon\varepsilon_0 A^2}\frac{1}{dC^2/dV} \tag{2.13}$$

with $\varepsilon = 5.7$ is the diamond dielectric constant, ε_o is the vacuum permittivity and A is the area of the diode. A doping concentration of $N_A = 3 \times 10^{17}\ cm^{-3}$ is extracted from the $\frac{1}{C^2} - V_G$ curve. This value is almost identical with the target value expected from the diamond growth parameters.

Systematic measurements [5] demonstrated the homogeneous dopant incorporation in diamond epilayer. As shown in Fig. 2.27, by using the Schottky-Mott plot, the doping concentration N_A on sample #3 has a very small variation (from 1.6×10^{17} cm^{-3} to 1.9×10^{17} cm^{-3}) and very close to the target doping concentration (2×10^{17} cm^{-3}).

2.2.3.2 Oxide charges

Another feature can be seen from the C-V curve and $\frac{1}{C^2} - V_G$ curve is the shift of the curves toward negative bias corresponding to the ideal case. In fact, this shift is possibly induced

[5] done by D. Valenducq, a master 1 internship from University Grenoble Alpes at SC2G, Institut NEEL

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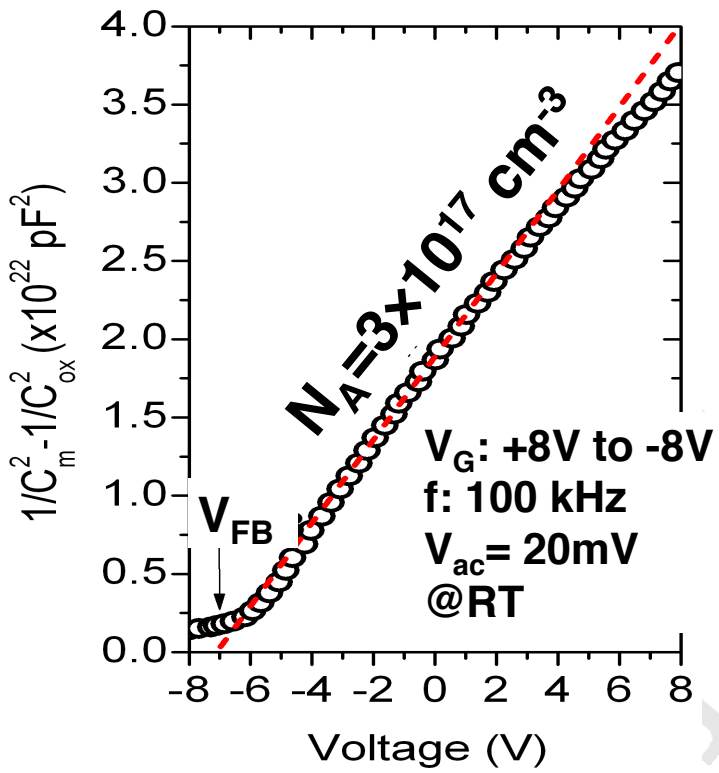

Figure 2.26: Inverse square capacitance-voltage characteristics of O-diamond MOSCAP for extracting doping concentration (MOS12 - sample #1)

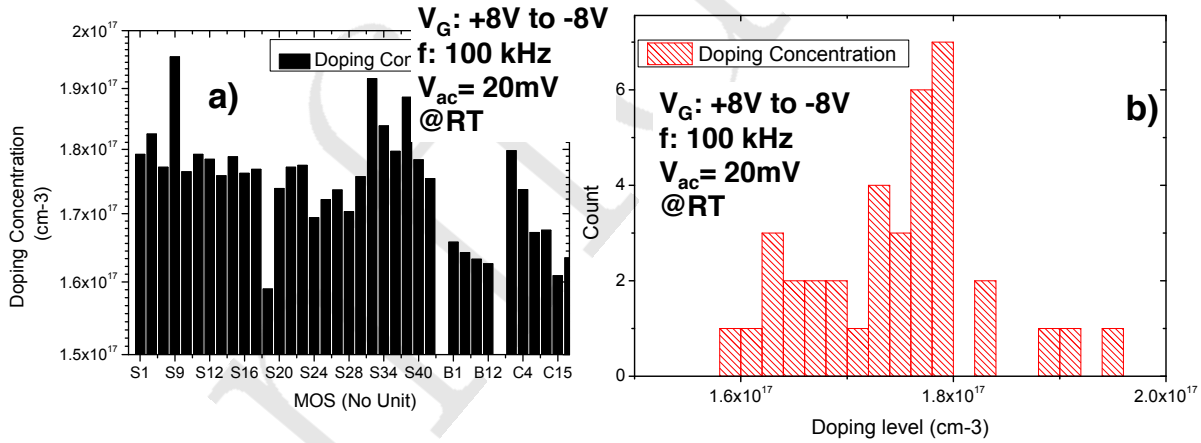

Figure 2.27: Systematic measurement of the doping concentration by using the Schottky-Mott plot (sample #3).

by the interface charges, the oxide charges and the work function difference between metal and semiconductor. However, since our C-V measurements were performed at 100 kHz, we excluded the a.c contribution from the interface state charge. Also, the slope of $\frac{1}{C^2} - V_G$ in the range of examination has reliably reflected diamond doping concentration. The DC contribution of interface states is also negligible. Therefore, we conclude that the shift of flatband voltage V_{FB} is the work function difference between metal and semiconductor Φ_{MS} and the net oxide charges Q_{ox}.

Technically, V_{FB} is evaluated from the linear fitting of the $1/C^2$ slope and its inter-

ception with gate bias axis. As shown in Fig. 2.26, a flat band voltage of V_{FB}=-7.3V is deduced. This value is larger than the theoretical one. Theoretically, $V_{FB} = \phi_{MS} = \phi_M - \phi_{SC} = -2.6\ V$ where $\phi_M = 4.3$ eV is the work function of Ti metal and semiconductor work function is $\phi_{SC} \simeq E_G + \chi_{sc} - E_A$. With $\chi_{sc} = 1.7$ eV is the electron affinity of O-diamond [33]. The discrepancy indicates the presence of net positive oxide charges. By applying the equation:

$$Q_{ox} = \frac{C_{ox}\left(\phi_{MS} - V_{FB}\right)}{qAt_{ox}} \tag{2.14}$$

A net positive oxide charge density of $Q_{ox} = 6 \times 10^{18}\,(cm^{-3})$ is obtained.

2.2.4 Gate controlled diamond semiconductor

As mentioned in chapter 1, the goal of this work is realizing an unipolar bulk controlled boron doped diamond MOSFET. Therefore, the central role of the MOS capacitor test devices is to examine in terms of efficiency of gate controlled boron doped diamond. As shown in chapter 1, semiconductor surface potential Ψ_s is the central quantity for this evaluation.

2.2.4.1 Semiconductor surface potential versus gate bias $\Psi_S - V_G$

As mentioned in chapter 1, the flatband regime is the demarcation between accumulation regime and depletion regime. At flatband, semiconductor charge $Q_{sc}\left(V_G = V_{FB}\right)$ and consequently semiconductor capacitance $C_{sc}\left(V_G = V_{FB}\right)$ is a function of semiconductor intrinsic Debye length as:

$$C_{sc}\left(V_G = V_{FB}\right) = \frac{\varepsilon_{sc}\varepsilon_0}{\lambda_p} \tag{2.15}$$

Where λ_p is the intrinsic Debye length of semiconductor and it depends on doping concentration N_A as $\lambda_p = \left(\frac{\varepsilon_{sc}\varepsilon_0 kT}{q^2 N_A}\right)^{1/2}$.

Since N_A was extracted from the previous section, semiconductor flatband capacitance $C_{sc}\left(V_G = V_{FB}\right)$ can be calculated. Subsequently, flatband capacitance of MOS capacitor $C_{MOS}\left(V_G = V_{FB}\right)$ can be evaluated as:

$$\frac{1}{C_{MOS}(V_G = V_{FB})} = \frac{1}{C_{ox}} + \frac{1}{C_{sc}(V_G = V_{FB})} \tag{2.16}$$

From these relationships, a MOS capacitor flatband capacitance of C_{MOS} $(V_G = V_{FB}) = 0.279\ \mu F.cm^{-2}$ had been evaluated for the MOS12-sample #1. In fact, the maximum measured capacitance of MOS capacitor at $V_G = -8V$ is lower than flatband capacitance $(C_m\left(V_G = -8V\right) = 0.135\ \mu F.cm^{-2})$. This is indicating that diamond is always in depletion regime even for high negative bias $(V_G = -8V)$. This is an important conclusion which is opposite to the previous conclusions from Chicot's PhD thesis [22] and Kovi et al. [20].

Since diamond is always in depletion regime in the measured range, semiconductor SCR is proportional to the square root of surface potential Ψ_s [17] in the whole voltage

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range (+8V to -8V). Therefore, the semiconductor capacitance is also proportional to the square root of semiconductor surface potential as [97]:

$$C_s = \sqrt{\frac{qN_A\varepsilon_o\varepsilon_s}{2\Psi_s}} \tag{2.17}$$

As measured capacitance C_m and oxide capacitance C_{ox} are known, semiconductor capacitance C_{sc} and semiconductor surface potential Ψ_s can be calculated. By performing a simple mathematical derivation of equations 2.16 and 2.17, surface potential corresponding to a gate bias can be deduced by:

$$\Psi_s\left(V_G\right) = \frac{q^2N_A\varepsilon_o\varepsilon_s\left(\frac{C_{ox}}{C_m}-1\right)^2}{2C_{ox}^2} \tag{2.18}$$

In principle, by performing this calculation at different gate bias, we can establish the relationship between semiconductor surface potential against gate bias ($\Psi_s - V_G$), and so evaluate the efficiency of gate control semiconductor.

Figure 2.28b represents the $\Psi_s - V_G$ relationship by using the above mentioned technique.

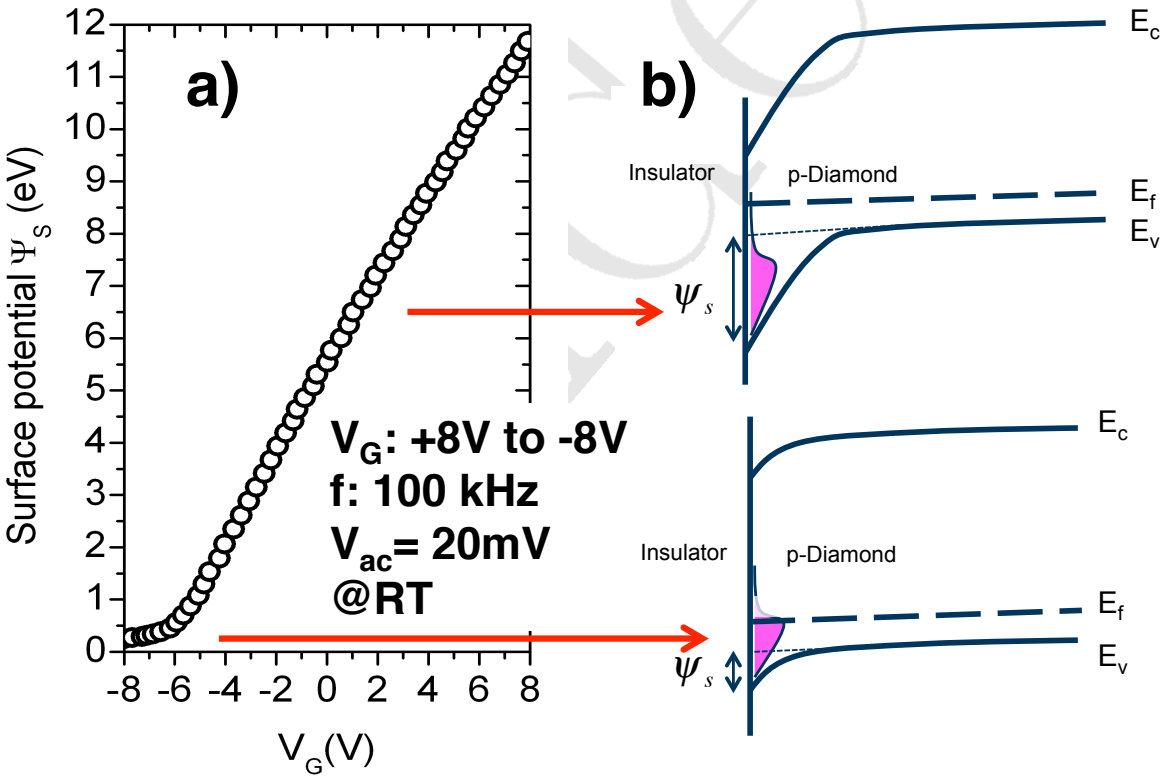

Figure 2.28: a) Diamond surface potential variation with gate bias (MOS12 - sample #1); b) description corresponding to diamond Fermi level moving against gate bias in Figure 2.7a. Fermi level pinning effect is suggested due to interface states (Magenta part in Fig. 2.7 b is the descriptive interface states density)

For high negative bias (V_G : -6V to -8V), the FLPE [94][98] is observed. Semiconductor is approaching but never reach the flatband voltage. For the remained gate bias range

($V_G : -6V$ to $+8V$), gate bias can effectively modulate semiconductor surface potential, even when semiconductor surface potential reaches the condition for inversion ($\Psi_s > 2\Psi_b$ with $\Psi_b \simeq 2.4$ eV). In fact, this is the reason why we were not able to observe the $C_{\min}$ as in the ideal Si/SiO_2 MOS capacitor. Also, as we will shown in the part 3 of this chapter, by decreasing the frequency to lower than 10 Hz, no sign of minority inversion were observed. This is reasonable considering the fact that generation time constant of minority carriers between valence band to conduction band is very large in wide bandgap semiconductors. For diamond with the bandgap of E_g =5.5 eV, the quickest characteristics generation time constant of minority carriers via a midgap state ($E_c - E_t = \frac{E_g}{2}$) can be approximated as:

$$\tau = 2 \times \frac{1}{v_{th}\sigma_e N_v} e^{\frac{E_c - E_v}{2k_b T}} \approx 10^{37} \text{ (sec)} \approx 10^{30} \text{ (years)} \tag{2.19}$$

With v_{th} the mean thermal velocity of carriers, N_v the equivalent density of states of valence band, σ_e is the capture cross-section of a defects in midgap with typical magnitude of 10^{-16} (cm^{-2}).

Practically speaking, with this minority carrier generation time constant, minority carriers inversion is not reachable at thermal equilibrium. Therefore, a source of minority carriers [14] is needed to observe the inversion regime in a diamond MOS capacitor. This is an important difference with respect to narrow bandgap semiconductors. Regarding silicon and other narrow bandgap semiconductors, generation time constant of minority carriers is of the order of seconds. As a consequence, the deep depletion regime in narrow band gap semiconductor will be very difficult to obtain. On the another hand, deep depletion is obtained in diamond semiconductor. The difference between diamond and other narrower band gap semiconductor is that this deep depletion regime is permanent, and does not change with time. This concept will opens a new path to realize a bulk controlled diamond MOS transistor.

2.2.4.2 Depletion width vs. gate bias

From $\Psi_s - V_G$ relationship, the SCR (W) width variation with V_G can be calculated by:

$$W = \sqrt{\frac{2\varepsilon_{sc}\varepsilon_0\Psi_s}{qN_A}} \tag{2.20}$$

Figure 2.29 represents the SCR width of boron doped O-diamond versus V_G. An effectively gate controlled diamond SCR width is obtained. This property will be very useful to realize a depletion mode diamond MOSFET (Chapter 3).

2.2.4.3 Interface states density extracted by Terman method

In this section, we will focus on the high negative gate bias part of the $\Psi_s - V_G$ curve where the FLPE is remarkable. As we have discussed in previous part, FLPE is probably related to the interface states at semiconductor-oxide interface. Therefore, the relative movement of semiconductor Fermi level with gate bias could potentially represents the density of interface states in the gap [99][97]. This is the main idea of high frequency-capacitance method (Terman method) to extract the interface states density [99]. With

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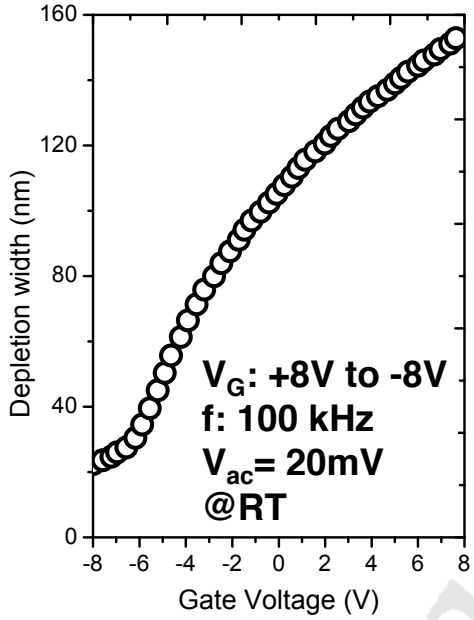

Figure 2.29: Depletion region variation with gate bias (MOS12 - sample #1).

the established $\Psi_s - V_G$ curve, the interface states density can be quantified by high frequency capacitance method [97][99].

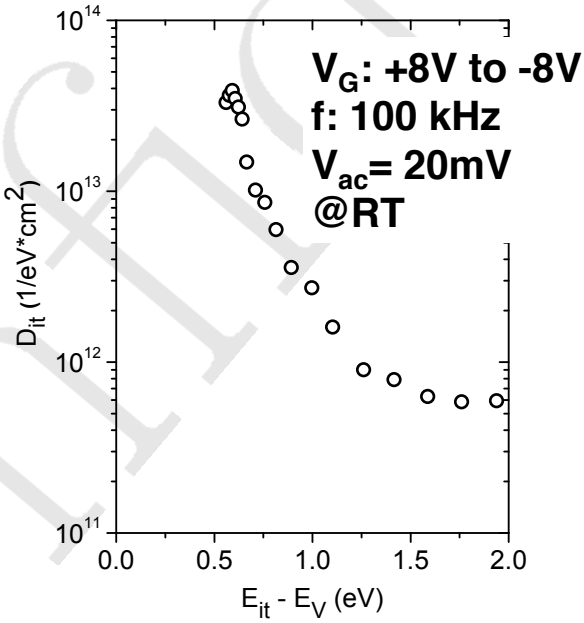

Figure 2.30: Interface density extracted from high frequency method (MOS 12- sample #1)

By evaluating $\frac{d\Psi_s}{dV_G}$, interface states capacitance can be calculated by:

$$C_{it}(\Psi_s) = C_{ox}\left[\left(\frac{d\Psi_s}{dV_G}\right)^{-1} - 1\right] - C_s(\Psi_s) \tag{2.21}$$

Subsequently, the interface states density can be evaluated by [97]:

$$D_{it}\left(\Psi_s\right) = \frac{C_{it}\left(\Psi_s\right)}{q} \tag{2.22}$$

Figure 2.30 represents the interface states density at diamond/oxide interface evaluated by Terman method [99]. From Terman method [99], an interface states density of less than 10^{12} $1/eV.cm^2$ is found in the midgap region and an abrupt increase up to 4×10^{13} (1/eV.cm^2) for the interface states near the valence band ($E_t - E_v \approx 0.6$ eV). We will discuss in more details these results, but a first quick evaluation of emission time constant (equ. 2.11) shows that interface states with $E_{it} - E_v > 1$ eV should not be observed for our DC voltage sweeping rate (100 mV/s)

2.2.5 Electrostatics simulation

As semiconductor charge qN_A, oxide charge Q_{ox} and interface states density D_{it} have been experimentally determined, an empirical electrostatics simulation can be performed. We performed the electrostatics simulation by implementing the semiconductor charge qN_A extracted from $\frac{1}{C^2} - V_G$ curve, oxide charge Q_{ox} extracted from shift of V_{FB} and interface states charge $\sigma_{it}(V_G)$ extracted from Terman method. Interface states charge is evaluated by integrating interface states density over the energy band gap.

Simulation results are shown in Fig. 2.31. Electrostatics band diagrams of MOS capacitor at different gate bias are shown in Fig. 2.31 a-c). Without gate bias ($V_G = 0$ V), due to high density positive charge in the oxide, holes from the $p-$type diamond are attracted to the oxide. A strong built-in potential around 5 eV was created. Also, an approximately 80 nm width close to the oxide/diamond interface is depleted, as shown in Fig. 2.31 b). For a positive bias (Fig. 2.31 c), the SCR is further modulated by gate bias. Deep depletion regime is obtained with a depletion thickness of 130 nm at $V_G = 2$V. Finally, Figure 2.31 a) represents the band diagram for a relatively small negative bias $V_G = -4$V. One remarkable issue from electrostatics simulation, which is not seen trivially from C-V measurement is the potential distribution within the oxide. This electrostatic band diagram is essential to identify the origin of forward current and capacitance-frequency dependence measurement. The electric field distribution of O-Diamond MOS capacitor at different bias regime is shown in Fig. 2.31 d.

The electrostatics simulation is relatively in agreement with experiment results for the gate bias range ($-6V \leq V_G \leq +2V$). However, when gate bias are out of that range, there is a discrepancy between experiment results and simulation results.

For the high positive bias, we understand that the simulation software performed in the ordinary manner where the inversion regime is assumed. As we have shown previously, this is irrelevant without a source of minority carriers.

For high negative bias, the discrepancy is most probably due to the inappropriate density of the input parameters. Figure 2.32 represents the semiconductor surface potential varying with gate bias obtained from experiments and nextnano simulation in negative bias region. As shown in Fig. 2.32, the semiconductor surface potential from simulation result is re-increased for decreasing V_G ($V_G = -6$ V to V_G=-8 V). This region corresponds to the crossing of the Fermi level with the elevated interface states density region. Therefore, the discrepancy is highly suspected due to the overestimate interface states density. In fact, in Terman method, the DC leakage current and the non equi-

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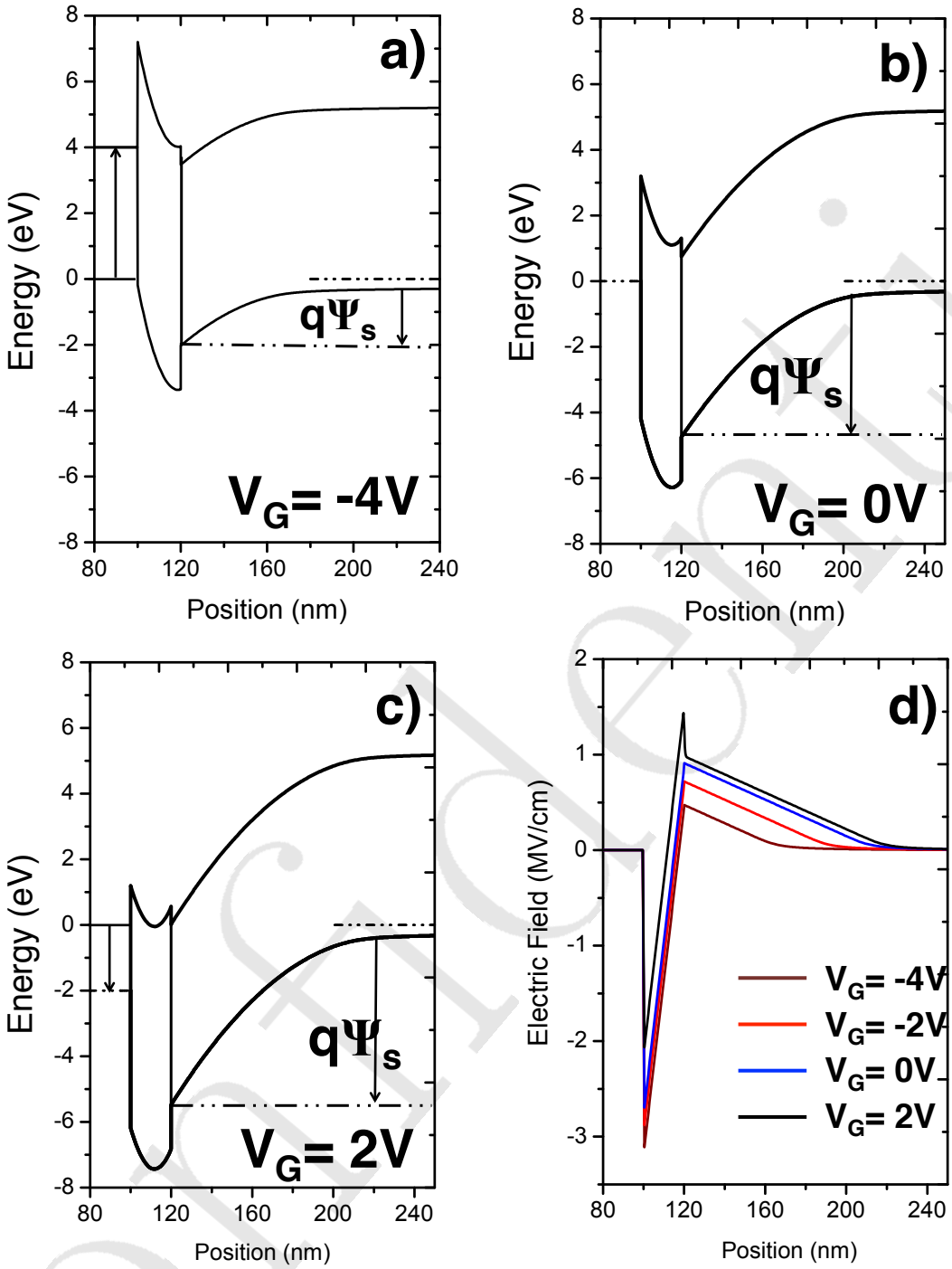

Figure 2.31: Electrostatics band diagram of O-diamond MOS capacitor calculated by Nextnano[3] at different metal gate potentials a) When device is biased positively toward deep depletion; b) When device is under zero bias condition; c) When device is negatively biased toward accumulation; d) Electric field distribution at different bias condition.

librium of the system have not been considered. Another more complementary method that considers DC current and the equilibrium of the system is needed to evaluate the interface states density.

In the Part 2 of this chapter, we will focus on the high negative bias regime ($V_G = -6$

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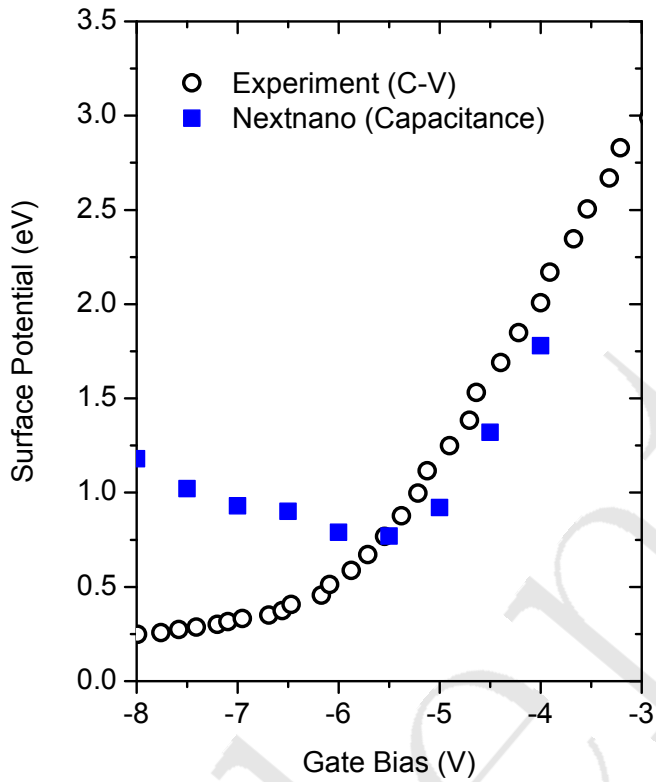

Figure 2.32: Nextnano simulation result compared with experiment by mean of surface potential (MOS12-sample #1).

V to V_G=-8 V - sample #1) toward a more complete electrostatic model. We will explore the origin of DC current and capacitance-frequency dependent in this bias regime. The effects from interface states will also to be discussed. A more appropriate method will be applied to evaluate the interface states density.

2.2.6 Conclusion

This part introduces a new technical approach to reduce series resistance and improve gate oxide in fabricating O-diamond MOS capacitor test devices. We introduce the complementary measurement techniques to obtain a proper C-V measurements. Systematic measurements were performed to ensure the reliability and reproducibility of the system. Crucial information on the MOS capacitor system were obtained. An effective gate controlled diamond SCR width was demonstrated. It is promising to fabricate a depletion mode diamond MOSFET. The issues on leakage currents and capacitance-frequency dependent are still unclear. New approaches are needed to completely understand the O-diamond MOS capacitor test device.

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Part II

O-Diamond MOS capacitor under negative bias: current mechanism and capacitance-frequency dependent

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2.3 Introduction

In the Part 1 of this chapter, we introduced the typical electrical characteristics of a boron doped O-diamond MOS capacitor. We addressed different aspects ranging from diamond growth, fabrication processing and electrical characterization. From electrical measurements, a special attention was paid to obtain the crucial information of the MOS capacitor system. Leakage current and capacitance frequency dependent measurements were systematically observed when devices are biased toward negative direction (forward bias). We addressed the effects from serial resistance and interface states. We proposed a method to eliminate these parasitics thanks to the capacitance-frequency (C-f) measurements. From the "proper capacitance measurement", we evaluated the critical information of O-diamond MOS capacitor such as semiconductor doping concentration N_A, semiconductor surface potential versus gate bias ($\Psi_s - V_G$), semiconductor depletion width versus gate bias ($W - V_G$) and oxide charge density Q_{ox}.

Thanks to the $V_G - \Psi_S$ relationship, we applied Terman's method [99] to extract the interface states density D_{it}. Interface states density exhibit a low density in the midgap region and an elevated density $\left(\text{up to } 4 \times 10^{13}\ 1/\text{eV.cm}^2\right)$ at $E_{it} - E_v = 0.6$ eV.

We implemented the semiconductor charges Q_{sc}, oxide charges Q_{ox} and interface states charges $\sigma_{it}(V_G)$ into the 1-dimensional finite element electrostatics Nextnano simulation. A special attention was paid for the forward bias regime (negative bias). The simulation results are compared with experimental results by mean of semiconductor surface potential Ψ_S. A quantitative agreement was obtained in the V_G range where the gate leakage current is relatively low. Unfortunately, for the V_G range where the gate current is high, the deviation between simulation and experiment is considerable.

Many issues are therefore raising. The first issue is related to the accuracy of input charge densities, especially interface states density D_{it} extracted from Terman method. Since Terman's method was applied without considering leakage current, deduced interface states density could be erroneous. The second issue concerns the origin of forward current and its relationship with electrostatics model. In another words, a method to quantify interface states density while subtracting any contribution from the leakage current is needed. Last but not least, the issue on capacitance-frequency dependence is also considerable. Elucidating the origin of capacitance-frequency dependence and its relationship with leakage current and interface states is necessary. Since interface states, leakage current and capacitance-frequency dependence are critical for the development of any MOS capacitor system toward a MOS transistor, a comprehensive understanding on their behaviors is prerequisite.

This part is devoted to address and solve the above mentioned problems. In the first section, we will re-introduce the general electrical characteristic of the O-diamond MOS capacitors to declare the problems. Then, we propose the forward current mechanism thanks to the electrostatics band diagram. From leakage current mechanism, we construct the physical equivalent circuit linearizing the small signal measurements. Approximated equivalent circuit based on different limiting processes will be discussed. Current limiting process is identified thank to different approaches. From approximated equivalent circuit, DC current is subtracted and conductance method is applied to quantify interface states density D_{it}. As all parameters of the equivalent circuit have been extracted experimentally, measured capacitance-frequency dependence can be simulated by using

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the equivalent circuit. Finite element electrostatics simulation is re-performed to reassess the accuracy of interface state density extracted from high frequency capacitance method and conductance method. In the end, this part will be concluded.

2.4 Results and Discussion

2.4.1 Typical electrical characteristics

Considering the ensemble of O-diamond MOS capacitors that have been previously fabricated by our group [18][19], the results published in literature [20] and the devices fabricated in the frame of this thesis, general electrical characteristics can be summarized in Fig. 2.33.

Figure 2.33a represents the typical DC current-voltage (I-V) characteristics of different MOS capacitors for V_G : $+8V$ to -6V. Here we present MOS C7, MOS C17 and MOS B12 of sample #3. This sample has been annealed and oxide charge were reduced. Under forward bias, forward currents are systematically observed with different magnitudes. Under positive bias, reverse currents are relatively random. The magnitude of forward current does not show a strong relationship with the reverse current. We will devote Part 3 of this chapter to investigate the origin of reverse current and its possible consequence.

Figure 2.33b represents the typical measured Conductance-Voltage ($G_p - V_G$) at different frequencies of MOS C7 - sample #3 for V_G : $0V$ to -6V . Measured conductance are frequency dependent at high frequency range. At a given low frequency range (≤ 1 kHz), the measured conductance is frequency independent and it is almost identical to the statics conductance (DC I-V).

Figure 2.33c represents the typical measured Capacitance - Voltage ($C_m - V_G$) at different frequencies of MOS C7 - sample #3 for V_G : $+8V$ to -6V. Figure 2.33d represents the Capacitance-Frequency ($C_m - f$) at $V_G = -5V$. In fact, this $C_m - f$ curve is equivalent to the cut line at $V_G = -5V$ in Fig. 2.33c. Both "measured capacitance" and "measured conductance" are frequency dependent as identical with the $C_m - f$ and $G_p - f$ in the part 1. Measured conductance behaves in a complementary manner with measured capacitance. (The terms "measured capacitance" and "measured conductance" are used here to discriminate with "corrected capacitance", "corrected conductance" and "equivalent conductance" further defined in the following sections).

The capacitance-frequency dependent phenomena was briefly discussed in the Part 1 of this chapter. It can be summarized into three regimes: 1) High frequency: capacitance measurement is affected by series resistance; 2) Proper frequency: no capacitance-frequency dependence; 3) Low frequency: capacitance increased a decade with frequency decreasing a decade. The "low frequency" range is very different considering different O-diamond MOS capacitor system, ranging from few kHz in Marechal et al. [19] to few MHz in Kovi et al. [20]. In this part, we will elucidate the origin of the capacitance-frequency dependence in this low frequency regime.

2.4.2 Forward current mechanism

In an ideal MOS capacitor, carriers transport between gate metal and semiconductor are necessary being blocked by a gate oxide. Electrostatics gate control of carrier population

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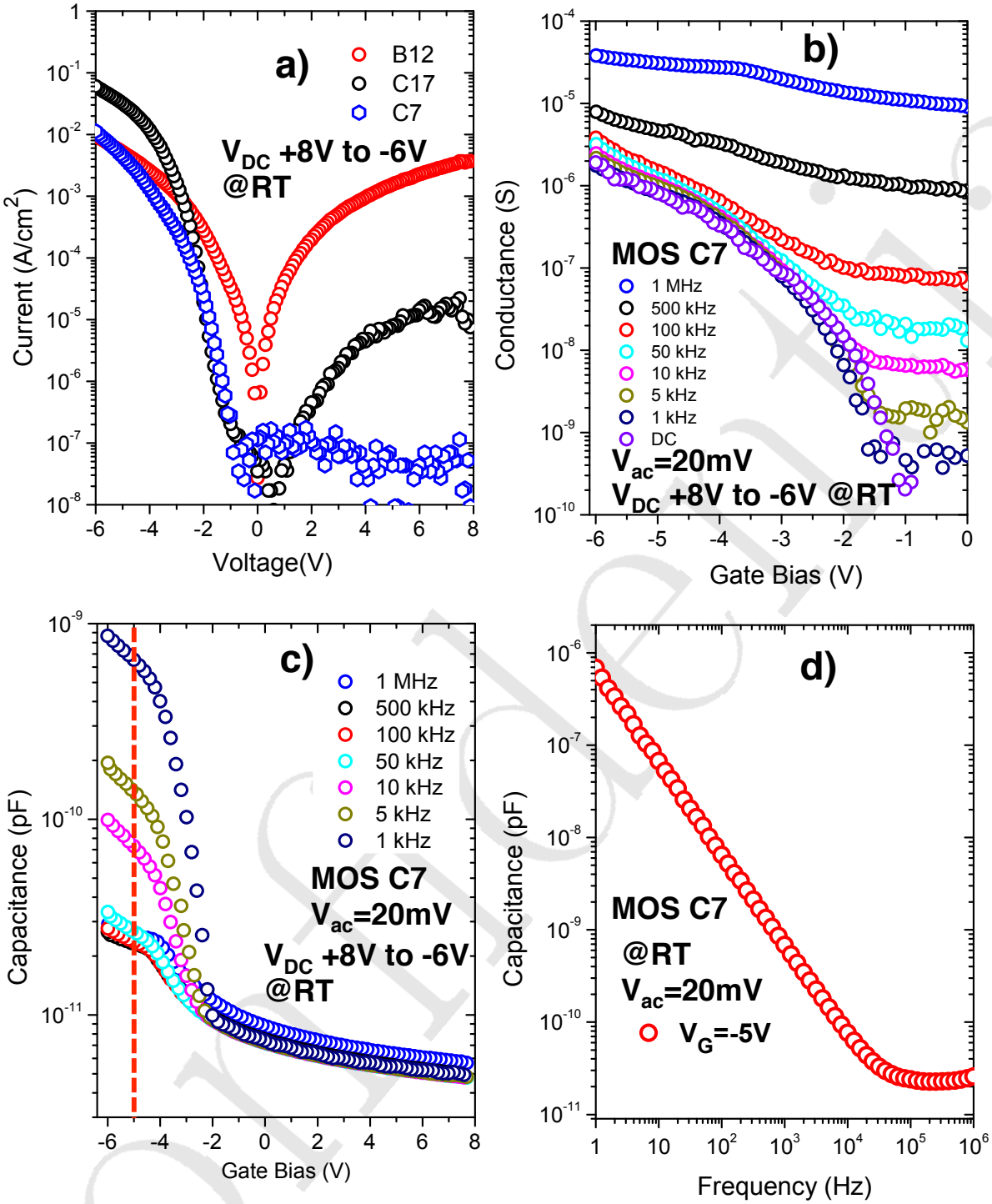

Figure 2.33: a) Current-Voltage characteristics of three MOSCAP: B12, C7 and C17 of sample #3; b) Conductance-Voltage characteristics of MOS C7 measured at different frequencies; b) Capacitance-Voltage characteristics of MOS C7 measured at different frequencies; d) Capacitance-frequency of MOS C7 measured at $V_G = -5V$.

at the oxide/semiconductor interface is crucial for the semiconductor devices. However, in real situations, leakage current is usually observed and perturbs the carrier control.

In order to understand the origin of leakage current, it is important to firstly determine

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the source of transporting carriers. In forward regime, current are initiated from either the accumulated semiconductor majority carriers or gate metal carriers reservoir [100]. For O-diamond MOS capacitor, as evidenced from C-V-f analysis and electrostatics band diagram, we concluded that forward current is initiated from carriers reservoir of metal gate and not from accumulated hole of diamond semiconductor. This conclusion is based on the fact that Fermi Level Pinning Effect (FLPE) preserved diamond in depletion regime, even at high negative bias (e.g $V_G = -8$ V, MOS 12- sample #1). No majority carriers (hole) are able to accumulate at diamond-oxide interface. The transport due to accumulated majority carriers is therefore prohibited.

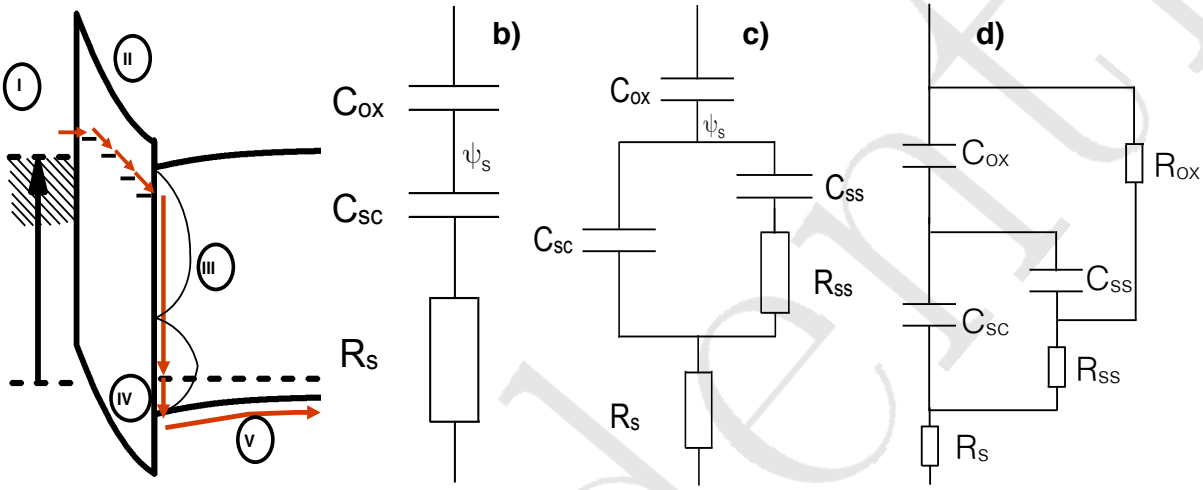

Figure 2.34: (a) Proposed current path mechanism including five steps: I. Electron tunneling from metal gate electrode to oxide gate, II. Hopping from traps to traps in the oxide, III. Recombination to surface traps state, IV. Electron from surface states emit to valence band or hole from valence band captured to interface states, V. Carriers drift in diamond epilayer to the back gate contact. (b) Equivalent circuit of a MOS capacitor without interface states and leakage current; (c) Equivalent circuit including interface states and an ideal gate oxide without leakage current (d) Equivalent circuit where the injected carriers from metal to interface states and the charges transfer between interface states and valence band are taken into account.

The next question to be addressed is, how do these carriers circulate in the MOS capacitor system? Thanks to Nextnano electrostatics band diagram (Fig. 2.31 b), we proposed a 5-steps current mechanism, as shown in Fig. 2.34a. In the step 1, carriers from gate metal are tunnelling into the oxide trap states. Hopping between traps to traps through the oxide is taking place in the step 2. In the step 3, hopping carriers being captured at interface states. The charges transferring between interface states and valence band are taking place in the step 4. Finally, these carriers will be drifted through the diamond epilayer to the back gate contact (p+) and complete the transfer process.

Potentially, the flow at each step may includes different processes in parallel. In principle, the process with highest rate (slowest time constant) will dominate the flow at that step. On another hand, in order to complete a circulation, different steps in series may be involved. The step with the slowest rate (longest time constant) will limit the flow.

In the proposed current mechanism (Fig. 2.34a), interface states play a central role

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with a special interest. They are able to communicate with both the metal electrode and the semiconductor valence band. In principle, each charge transfer process is represented by its characteristic time constant τ. For the sake of simplicity and without losing the generality, we will firstly consider interface states as a single level state at $E_{it} - E_v$ and density of N_{it}. In the following section, we will further discuss the charge transfer of interface states with metal and semiconductor band edge.

2.4.2.1 Charge transfer between interface states and metal

The charge transfer between interface states and gate metal in a MOS capacitor system was addressed by Dahlke and Sze [100]. The complementary theory was then developed by Freeman and Dahlke [101]. In their theory, interface states are modeled as a potential well and communicate with the gate metal by direct tunneling. The charge transfer is considered as an overlapping process of two wave functions. Kar and Dahlke had experimentally studied the metal injection into interface states with a non-degenerate Si substrate and a moderate oxide thickness ($20 - 40$ Å) MOS capacitor system [102]. A notable possible consequence of metal's carriers injection to interface states is that these carriers are possibly accommodating at interface states and therefore modulating Schottky barriers height at Metal-Semiconductor contact [103][104][105].

In our case, the oxide is too thick to observe direct tunneling. Therefore, carriers injection from metal to interface states is suggested to be a process of two consecutive steps: the carriers tunneling from gate metal to oxide trap states (represented by tunneling time constant τ_{tun}) and then carrier hopping between trap sites happens in the oxide (represented by hopping time constant τ_{hop}). We considered that the global characteristic time constant for the charge transfer between metal to interface states τ_T is approximately the time constant of the slower process in two mentioned processes.

Tunneling from metal to many oxide trap states As shown in Fig. 2.34 a), electron from metal gate is suggested to initiate the flow by tunneling into Al_2O_3 oxide layer. Even if there are many possible processes for a carrier from metal gate to be injected into the oxide [106], most of them are practically not possible in our case. It's either direct tunneling, thermionic emission (Schottky injection) or tunneling into many trap states in the oxide. Considering the oxide thicknesses of $10 - 40$ nm that were systematically used for O-diamond MOS capacitors, direct tunneling by overlapping wave functions (theoretically less than 1 nm) [100] is not possible. Thermionic emission is a thermal activation process where carriers from metal have to reach a sufficient energy to jump over the metal-oxide barrier height and being injected into oxide layer. Regarding an approximate 3 eV barrier height between Ti and Al_2O_3, this process is not realistic. Therefore, the tunneling from gate metal into oxide trap states [107] is the most realistic process.

The tunneling current from metal to many oxide trap states can be approximately described by [108]:

$$I = N_t q v \tag{2.23}$$

where N_t is the number of nearest traps that contribute to the conduction and v is the tunneling transmission rate. Tunneling transmission rate is calculated as $v = v_o.f.T$

with $v_0 \sim 10^{13}$ Hz is the attempt frequency which is representing the rate of escape of a particle from a confining structure by quantum tunneling through its outer barrier [109]. f is the Fermi-Dirac function representing the occupancy probability of a trap state in the oxide. It can be expressed by:

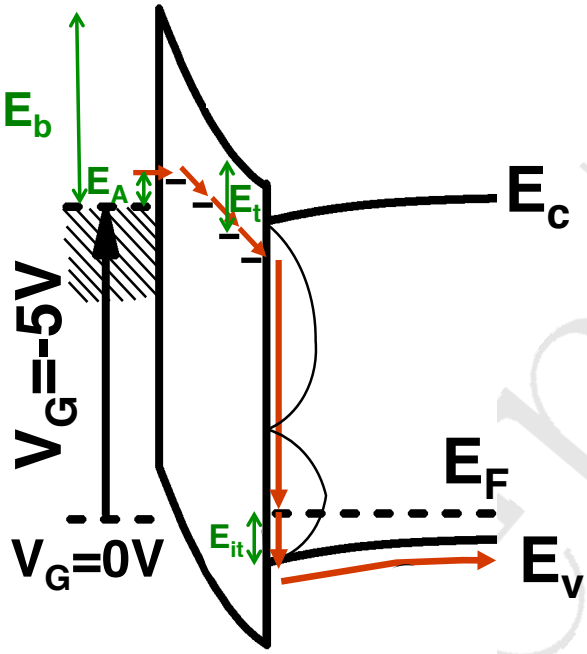

Figure 2.35: Proposed current mechanism of different processes and its corresponding energy level.

$$f = 1/\left(1 + \exp\left(\frac{E_b - E_t + F.t_{ox}}{kT}\right)\right) \tag{2.24}$$

where E_b is the electron barrier between metal electrode and oxide conduction band, E_t is the depth of the traps in the oxide, F is electric field in the oxide and t_{ox} is the oxide thickness (Fig. 2.35). T is the Wentzel-Kramers-Brillouin (WKB) transmission coefficient and can be written as:

$$T = \exp\left(-\frac{4}{3\hbar qF}\sqrt{2m^*}\left(E_t^{3/2} - (E_t - F.t_{ox})^{3/2}\right)\right) \tag{2.25}$$

with $\hbar$ is the reduced Planck constant and m^* effective mass of carrier in the oxide [108].

Hopping in the oxide Carriers transport in the oxide could be the sum of multiple parallel mechanisms [106][108]. One of two main mechanisms is the thermal activation from deep energy traps to oxide conduction band, which is generally called as Poole-Frenkel emission. The second one is tunneling from traps to traps and generally known as Mott hopping. In order to determine the dominant process, transfer rates of each process are necessary to be evaluated.

The Poole-Frenkel emission rate scaled versus T as:

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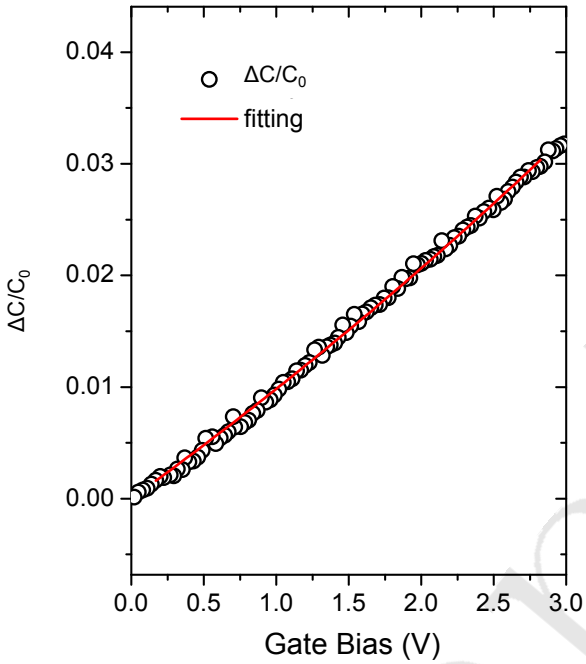

Figure 2.36: DC Capacitance-Voltage non-linearity of MIM capacitors and the fitting to extract hopping distance.

$$v = v_0 \exp\left(-\frac{E_c - E_t}{kT}\right) \tag{2.26}$$

where E_t is the energy of the traps in the band gap of oxide [108] (Fig. 2.35). In case of Al_2O_3 oxide deposited by Atomic Layer Deposition (ALD), trap states are usually ascribed to non-stoichiometry of the oxide. Electron trap level which is nearest to conduction band is $E_c - E_t = 1$ eV [110]. First principle simulation assigned this trap to oxygen vacancies [110].

The trap to trap tunneling rate is calculated as [108]

$$v = v_0 \exp\left(-\frac{2R}{\xi}\right) \tag{2.27}$$

with ξ is the electron wave function localization length $\xi \simeq 0.3$ nm, R is distance between trap sites [108].

Distance between trap sites could be obtained by fitting the DC non-linearity capacitance-voltage of MIM capacitor [111]. The DC non-linearity $\frac{C_{V_G} - C_0}{C_0} = \frac{\Delta C}{C_0}$ (variation of MIM capacitance with gate bias) of MIM capacitor are fitted by the equation:

$$\frac{\Delta C}{C_0} = a\left[\exp\left(bV_G\right) - 1\right] \tag{2.28}$$

With C_{V_G} is the capacitance measurement corresponding to gate bias variation and C_0 is the capacitance corresponding to $V_G = 0$ V. a and b are coefficients and their expression will be detailed in next equation [111]. A complete expression of equation (6)

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is:

$$\frac{\Delta C}{C_0} = \frac{2}{(\varepsilon_0 \varepsilon)^{2n}} \left(\frac{t_{ox}}{L_D}\right)^{1-2n} \frac{1}{(2+\rho)^{2(1-n)}} \frac{1}{\omega^{2n}} \sigma_0^{2n} \times [\exp(nqE_{eff}R/k_BT) - 1] \tag{2.29}$$

with n is an empirical parameters, t_{ox} is the oxide thickness, L_D is the Debye length, E_{eff} is the effective electric field, ρ is the "blocking parameters" which measure charge exchange at the electrode[6]. Experimental DC non-linearity $\frac{\Delta C}{C_0}$ versus V_G is shown in Fig. 2.38 with the fitting curve using equation (6). From fitting curve, b value is evaluated as 0.094. The distance between trap sites in our ALD Al_2O_3 is then estimated of approximately 5 nm.

A rough calculation shows that the tunneling rate from trap to trap is almost 150 times faster than Poole-Frenkel thermal activation rate from traps level to conduction band at room temperature. In case an oxide trap level is closer to oxide conduction band, the injection rate in the step 1 will be mostly dismissed. It is therefore possible to conclude that tunneling from trap to trap is the main carriers transport mechanism in the oxide.

The time for carriers readjustment when they are trapped by interface states (Step III), as usual [84] will be neglected because its thermalization process is very fast compare to other processes.

2.4.2.2 Charge transfer between interface states and semiconductor band edges

In the step IV, the trapped electrons at interface states will be emitted to the semiconductor valence band. Considering the single level interface states model with a density N_{it} and a energy $E_{it} - E_v$ from valence band, the occupation probability of a trap state by an electron is described by Fermi-Dirac function [84]:

$$f = \frac{1}{\left[1 + \exp\left(\frac{E-E_F}{kT}\right)\right]} \tag{2.30}$$

Equivalently, the occupation probability of a trap state by a hole is described as:

$$f_p = 1 - f = f \exp\left(\frac{E - E_F}{kT}\right) \tag{2.31}$$

The hole capture rate is described as:

$$R_p = N_{it}\sigma_p v_{th} f p_s \tag{2.32}$$

and hole emission rate is described by:

$$G = N_{it}\sigma_p v_{th} f_p p_1 \tag{2.33}$$

with σ_p is the hole capture cross-section of the trap states, v_{th} is the carriers mean thermal velocity, p_s is the surface carriers density at thermal equilibrium and is described by:

[6] see Khaldi et al. [111] for more details

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$$p_s = p_b \exp\left(\frac{-e\Psi_s}{kT}\right) \tag{2.34}$$

where p_b is the bulk carriers density and can be calculated as:

$$p_b = N_v \exp\left(\frac{E_v - E_F}{kT}\right) \tag{2.35}$$

where E_F is the quasi-Fermi level and N_v is the effective density of states in the valence band. p_1 represents the carrier density that established at the trap states when quasi-Fermi level equals the trap states level [101] and can be calculated as:

$$p_1 = N_v \exp\left(\frac{E_v - E_{it}}{kT}\right) \tag{2.36}$$

The charge transfer rate of carriers trapped at interface states with semiconductor bands are described by net flow of carriers captured and emitted in Schockley-Read theory [84].

$$U_{cp} = N_{it}\langle\sigma_p \upsilon_{th}\rangle\left(f p_s - f_p p_1\right) \tag{2.37}$$

Recombination time constant of majority carriers with interface states is then calculated as:

$$\tau_R = \frac{1}{\sigma_p \upsilon_{th} p_b}\exp(\Psi_s) \tag{2.38}$$

Injected carriers from gate electrode to interface states and charge transfer of interface states with semiconductor band are described by the differential equation for occupancy of interface states as [101]

$$N_{it}\frac{df_t}{dt} = -U_{cp} + \frac{j}{q}. \tag{2.39}$$

Where j is the current injected from metal gate to interface state. The current in and out interface states discussed above is described by the interface states occupancy f_{ss} [101][102] which is approximated by:

$$f_{ss} = \left(\tau_R f_m + \tau_T f_s\right) / \left(\tau_R + \tau_T\right) \tag{2.40}$$

where f_s and f_m are the bulk semiconductor and metal occupancies, respectively [101].

2.4.2.3 Drift in the diamond layer

The process of electron to be emitted to valence band is equivalent to the process of hole from valence band to be captured to interface states. To replace the evacuated hole, a hole from the back side (p+ layer) will move to diamond surface and be ready for a new capture event [112]. In reverse direction, electrons are transferring to back gate contact (p+) and complete the circulation.

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2.4.3 Equivalent circuit and conductance method

2.4.3.1 Equivalent circuit

In order to model the measured impedance and admittance of a MOS capacitor, linearized equivalent circuit is a well-known concept. Lehovec and Sloboskoy developed a comprehensive theory and derived a general equivalent circuit for the MOS capacitors [113]. Nicollian and Golzberger had paid their special attention to the conductance of interface states in "thick oxide MOS capacitor" [85]. The meaning of "thick oxide" is that the interface states are in equilibrium and close communication with semiconductor band edges. They also developed a model to evaluate the equivalent conductance G_P/ω from C_p and G_p that consists only interface states density and its time constant [85].

For the special case where interface states communicate with both gate metal and semiconductor band edges, Freeman and Dahlke developed a theory as well as derived its corresponding equivalent circuits [101]. Different possible limiting processes were also discussed. The approximations corresponding to each limited case were also done. Since then, there were different discussions about the possibilities and opportunities to employ gate tunneling into interface states to measure a wide range of interface states density [114][102][115]. Kar and Dahlke performed the experiments on Si/SiO_2 MOS capacitor with a moderate oxide thickness and a non-degenerate Si semiconductor to investigate interface states thanks to gate carriers injected to interface states [102].

In the Part 1 of this chapter, we discussed the equivalent circuit of MOS capacitor in an ideal case where only the unavoidable series resistance were involved (Figure 2.34b) and in case of single level interface states in thick oxide MOS capacitor were taking into account (Figure 2.34c).

Corresponding to the current mechanism in Fig. 2.34a, we introduced the equivalent circuit for our O-diamond MOS capacitor (Fig. 2.34d). Non-perfect gate oxide with gate leakage current is modeled by an oxide conductance G_{ox} and an oxide capacitance C_{ox} in parallel. The flow of carriers from metal to semiconductor is injected to the mid point of the interface states recombination circuit, as proposed by Freeman et al. [101].

2.4.3.2 Equivalent circuit approximation

In this section, the O-diamond MOS capacitor general equivalent circuit will be approximated corresponding to different limiting processes. We remind that the equivalent circuit in Fig. 2.34d is actually re-introduced in Fig. 2.37a. In the theoretical model of Freeman and Dahlke [101] and in the experiments and analysis of Kar and Dahlke [102], different limiting processes and their corresponding approximations were discussed. We will briefly reintroduce these approximations here for the purpose of clarification .

As the drift in semiconductor (step 5) is expected much faster compared to two other processes, we will only consider the interface states recombination limited and the oxide tunneling limited.

Interface-states-recombination-limited The interface states recombination is limited when interface states recombination time constant is much longer than the oxide tunneling time constant ($\tau_R >> \tau_T$). In other words, the oxide tunneling rate is much higher than the interface recombination rate. The interface states will therefore be in equi-

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librium with metal. In this case, the interface states-recombination-limited was found to modify the Schottky barrier height due to the charge being accommodated at the interface states [103][104][105]. Therefore, a self-consistent calculation is necessary to be performed in order to not violate the Gauss's law equations, as discussed by Werner et al. [104]. The rigorous self-consistence calculation was done by Muret et al. [105] and also Wegner et al. [104] for Schottky diode with a thin oxide layer.

In case of a MOS capacitor system, the approximated equivalent circuit for the interface recombination limited was introduced by Freeman et al. [101] and Kar et al. [102]. The approximated equivalent circuit is shown in Fig. 2.37b where interface states recombination is in equilibrium with metal and interface states are in the same potential with oxide potential. One important notice is that, in case interface states recombination limited, the measured conductance is frequency independent [101][102].

Oxide-tunneling-limited When the oxide tunneling time constant is much longer with respect to interface states recombination time constant $\tau_T >> \tau_R$, the limiting process is the oxide tunneling. This is approximatively equivalent to interface states are in equilibrium with semiconductor [101][102]. Since interface states are in equilibrium with semiconductor, the injection from metal to interface states is approximated as injection from metal to semiconductor. Interface states therefore will play a similar role with interface states in "thick oxide" model where it is in equilibrium and closed communication with semiconductor band edges. The approximated equivalent circuit for oxide tunneling limited is shown in Fig. 2.37c.

A major difference between interface states recombination limited (Fig. 2.37 b) and oxide tunneling limited (Fig. 2.37c) is the measured conductance-frequency characteristics. For the purpose of comparison, measured conductance circuit is the parallel circuit $C_p - R_p$ in Fig. 2.37g. In case oxide tunneling limited, measured conductance is frequency dependent, as shown in Fig. 2.37c. For interface states recombination limited (Fig. 2.37 b), measured conductance is frequency independent.

Considering our O-diamond MOS capacitor, as presented in previous sections (Fig. 2.33c and Fig. 2.23), measured conductance is frequency dependent. Therefore, we conclude that the oxide tunneling process is the limiting process. The interface states recombination limited is possible in case of high injection MOS capacitors (e.g. current density ≥ 1 A/cm^2). In that case, the carriers injection from metal gate is sufficient to preserve interface states in equilibrium with metal gate. The MOS #4 sample in Chicot et al. [18] and the 4×10^{19} cm^{-3} doped sample in Kovi et al. [20] are most probably interface states recombination limited case.

2.4.3.3 Limiting process

As a consequence from the previous analyses, the oxide tunneling process was identified as the limiting process. However, since oxide tunneling is indeed a two step process, further approximation is needed. Bearing in mind that the limiting process for the transport in the oxide is basically either bulk oxide limited process (hopping between traps to traps) or interface limited process (tunneling from gate metal into oxide trap states). The difference is due to the nature of contact between metal and oxide, i.e. an ohmic contact or an unsaturated contact [116]. Transport in the oxide is usually bounded between the

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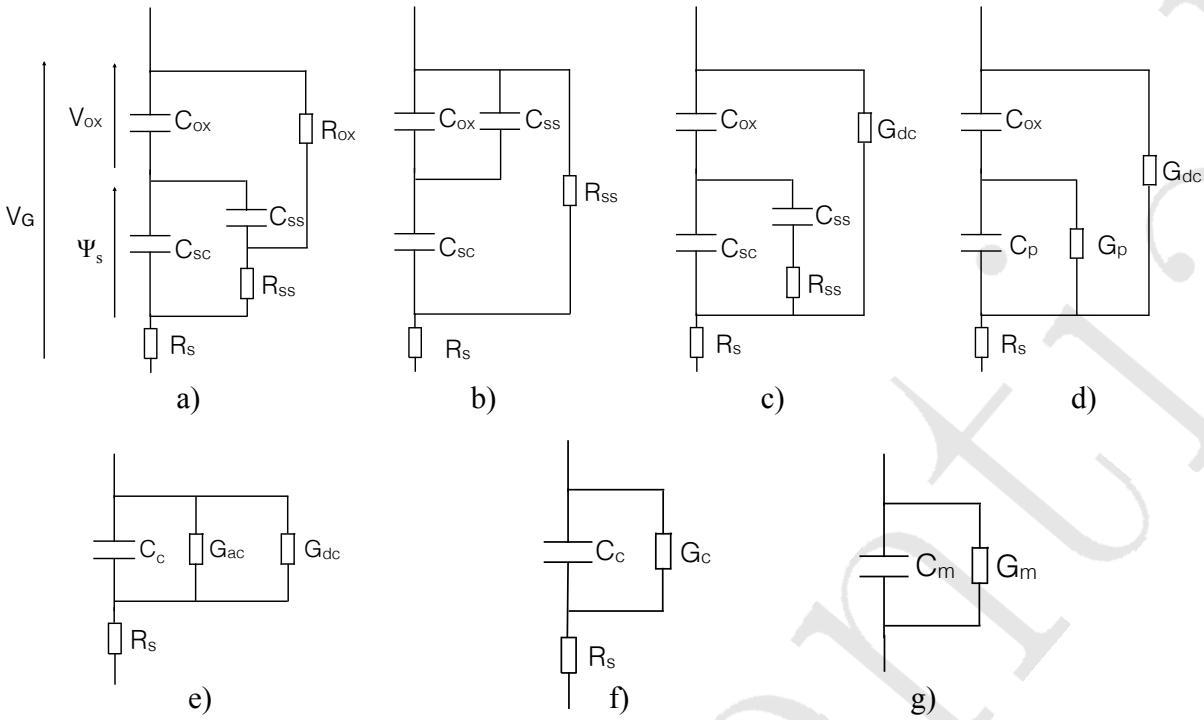

Figure 2.37: Equivalent circuit for O-diamond MOS capacitor: a) general circuit with gate carriers injected to single level interface states; b) approximated equivalent circuit for interface states recombination limited; c) approximated equivalent circuit for oxide tunneling limited; d)-g) step by step circuit transform to achieve measurement circuit; d) Circuit transformed from circuit c); e) circuit transformed from circuit d); f) Circuit transformed from circuit e); g) the parallel circuit for measured capacitance and measured conductance.

ohmic law and Child law space charge limited current. The current is governed by a power law with voltage as $I = AV^{\alpha}$. In order to examine the power law dependence of I-V curve, the semilog IV characteristics of different MOS capacitors (Figure 2.38a) were plotted in logarithm-logarithm scale. Figure 2.38b represents the logJ - logV of different MOS capacitors. No clear ohmic law is observed from log-log plot. $I \sim V^2$ of Child law Space Charge Limited Current (SCLC) [117] is verified in high injection MOS capacitor. For the low injection MOS capacitor, $I \sim V^5$ where interface-limited traps assisted tunneling [118] mechanism is probably governing these low injection MOS capacitor. In order to study the thermal activation process, I-V characteristics were measured at different temperatures (from 150K to 360K).

For high injection MOS capacitor, the I-V characteristics at different temperatures are shown in Figure 2.39a. Figure 2.39b represents the current density measured at $V_G = -8$ V versus temperature (J-T). The J-T curve is well fitted by a $e^{(\frac{T_0}{T})^{1/4}}$ law, which is characteristic of variable range hopping (VRH) [119].

For low injection MOS capacitor, the I-V characteristics at different temperatures are shown in Fig. 2.40a. Figure 2.40b represents the Arrhenius plot of current density measured at $V_G = -8$ V versus temperature. From the slope, a thermal activation energy of $E_A = 215$ meV was evaluated. As suggested from generalized thermionic trap assisted tunneling model [118], this thermal activation energy is assigned to the barriers between

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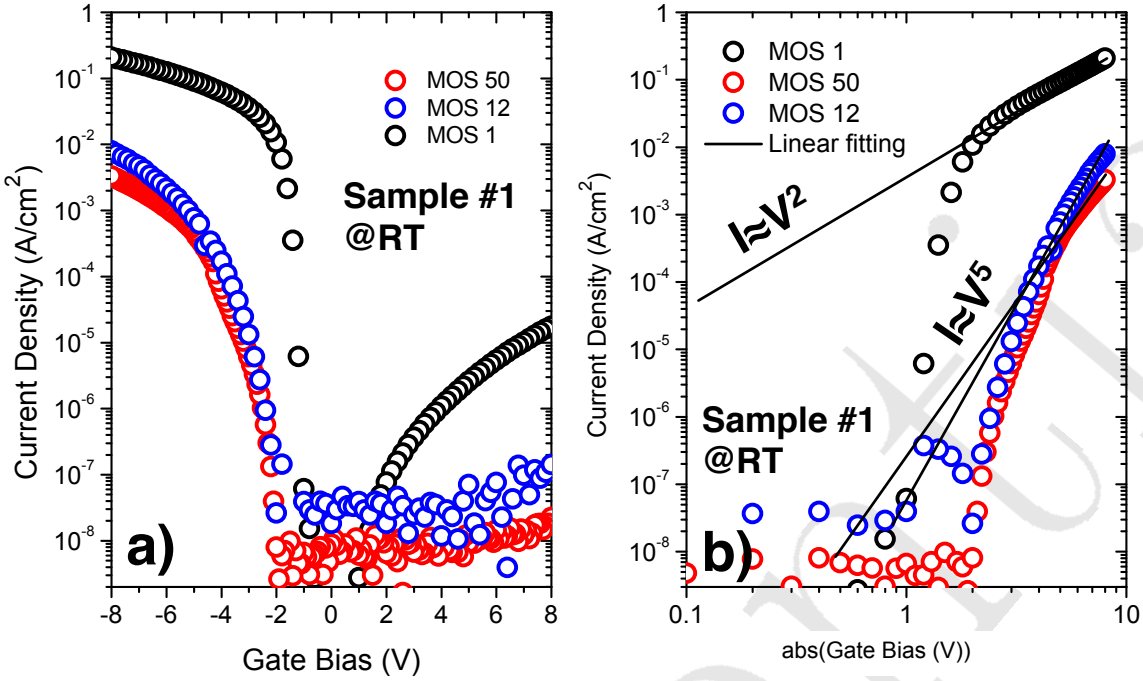

Figure 2.38: a) Semi-log plot Current-Voltage characteristics of high injection MOS capacitor and low injection MOS capacitor; b) the log-log plot to identify the current-voltage power law from linear fitting (MOS 1 and MOS 50 - Sample #1) @RT.

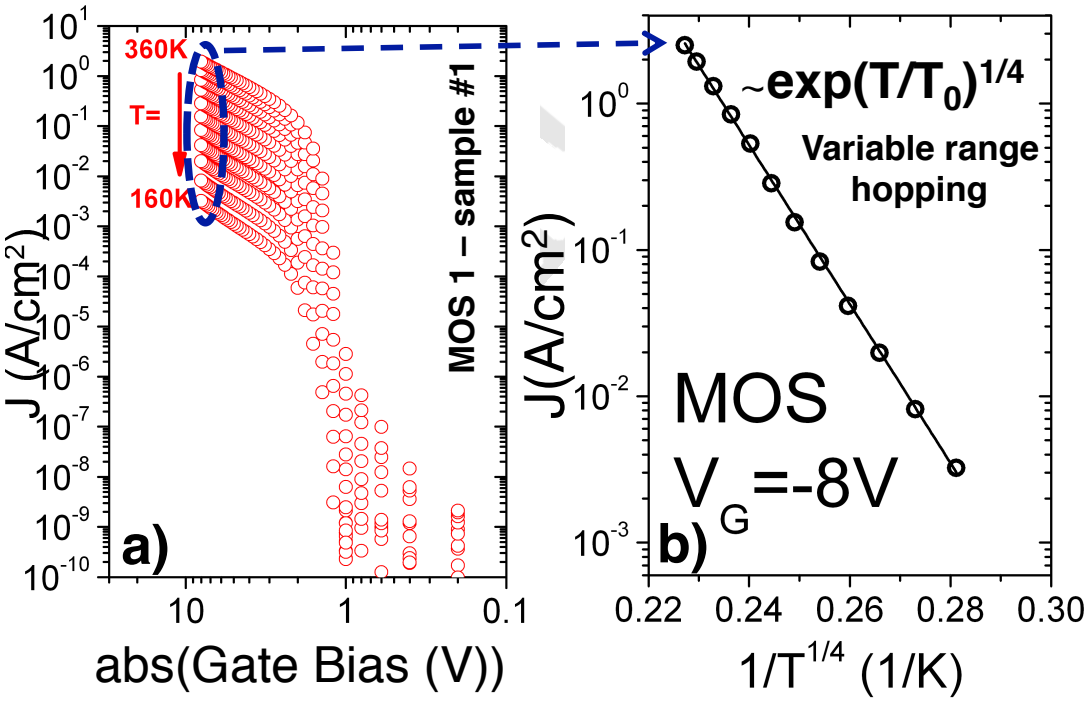

Figure 2.39: a) Current-Voltage characteristics of high injection diode measured at different temperatures ; b) Temperature dependence of gate leakage current versus $\frac{1}{T^4}$ measured at $V_G = -8V$ in MOS 1 -sample #1. The logJ versus $\frac{1}{T^4}$ dependence well fitted by the straight line indicates a variable range hopping in the oxide.

metal and Fermi-Dirac occupancy function of the oxide trap states (Fig. 2.35).

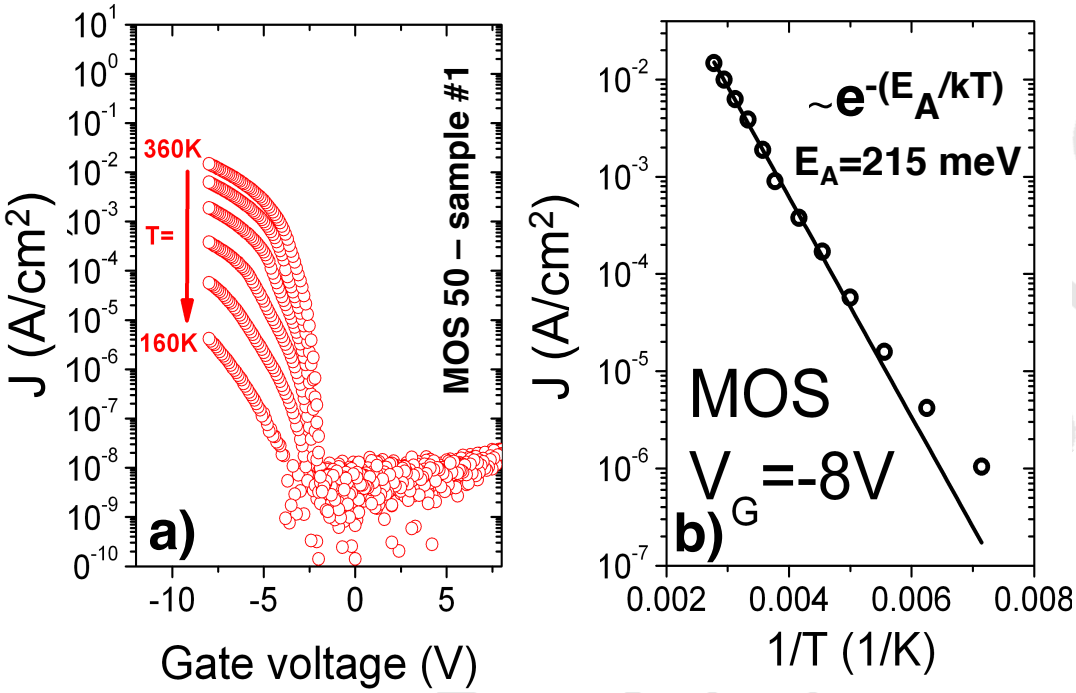

Figure 2.40: a) I-V characteristics of low injection diode measured at different temperatures; b) Arrhenius plot of current density at different temperatures when V_G=-8V indicates a thermal activation energy of 215 meV (MOS 50 - sample #1).

2.4.3.4 Equivalent conductance G_p/ω

Conductance of interface states ($\frac{1}{R_{it}}$ where R_{it} is the one of Fig.2.37) represents the energy loss due to carriers transfer between semiconductor band edge and interface states after a disturbance of a small a.c signal. In more details, it can be understood as the supplied small ac signal in both halves caused the disturbance and drive the equilibrium system between semiconductor band edge and interface states become non-equilibrium. Therefore, there are carriers transferred between interface states and band edge. However, the carriers transfer is not immediate after the signal was supplied but lag behind and caused the loss. The loss is minimized or conductance is maximized when the applied signal is equivalent to the resonant frequency of the interface states. With the applied frequency lower than the resonant frequency, carriers are stored at the capacitance of the interface states but not transferred. Subsequently, conductance of the interface states is decreased. Therefore, conductance of interface states which is bearing the information of interface states should have a bell shape. For conductance method, the goal is to obtain the equivalent interface states conductance in Fig. 2.37d from measured conductance and measured capacitance in Fig. 2.37g.

In order to obtain the equivalent interface states conductance, measured parallel conductance and parallel capacitance are necessary to be corrected to eliminate the series resistance, the DC current and gate oxide capacitance. The circuit transformation is following the procedure introduced by Kar and Dahlke et al. [102] and in Vogel et al. [120].

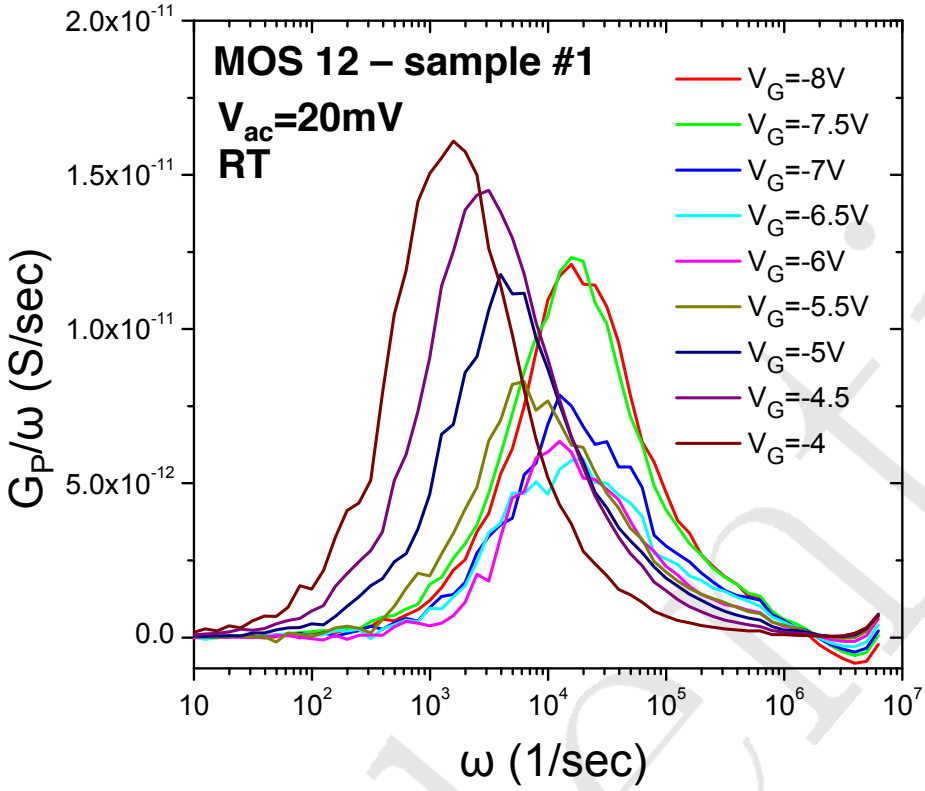

Figure 2.41: Equivalent conductance G_p/ω at different gate bias measured at RT (MOS 12 - Sample #1).

From the measured conductance and capacitance, the corrected conductance and corrected capacitance with series resistance in Fig. 2.37f is given by:

$$C_c = \frac{C_p}{(1 - G_p R_s)^2 + \omega^2 C_p^2 R_s^2} \tag{2.41}$$

$$G_c = \frac{\omega^2 C_p C_c R_s - G_p}{G_p R_s - 1} \tag{2.42}$$

Then, the G_{ac} in Fig. 2.37e is obtained by subtracting the G_c by oxide tunneling conductance G_{dc} as:

$$G_{ac} = G_c - G_{dc} \tag{2.43}$$

where the conductance G_{dc} is determined from derivation of DC current on DC voltage around the gate bias voltage $\left(\frac{dI_{DC}}{dV_{DC}}\right)_{V_G}$.

Then, the ac conductance G_{ac} must be corrected with gate oxide capacitance C_{ox} to obtain the equivalent conductance G_P/ω by using the equation:

$$\frac{G_P}{\omega} = \frac{\omega C_{ox}^2 G_{ac}}{G_c^2 + \omega^2 (C_{ox} - C_c)^2} \tag{2.44}$$

For the purpose of comparison the interface states density with Terman's method, we will present here the data measured on the MOS 12 on sample #1). The equivalent

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conductance at different gate bias are shown in Fig. 2.41. The equivalent conductance represents the clear bell shape feature with a clear maximum $\left(\frac{G_P}{\omega}\right)_{\max}$ peak. As mentioned, the frequency corresponding to the $\left(\frac{G_P}{\omega}\right)_{\max}$ is equivalent to the resonant frequency of interface states. By varying the gate bias from -8 V to -4 V (MOS 12 - sample #1), the $\left(\frac{G_P}{\omega}\right)_{\max}$ are gradually moving toward the lower frequency since Fermi level moving away from valence band.

2.4.3.5 Interface states density

From equivalent conductance G_P/ω, interface states density can be calculated as [85]:

$$N_{it} = 2\left(\frac{G_P}{\omega}\right)_{\max} /q \tag{2.45}$$

with $\left(\frac{G_P}{\omega}\right)_{\max}$ is the maximum of the $\left(\frac{G_P}{\omega}\right)$ curve. Figure 2.42 represents the interface states density extracted by conductance method versus the corresponding energy of the trap states in diamond band gap.

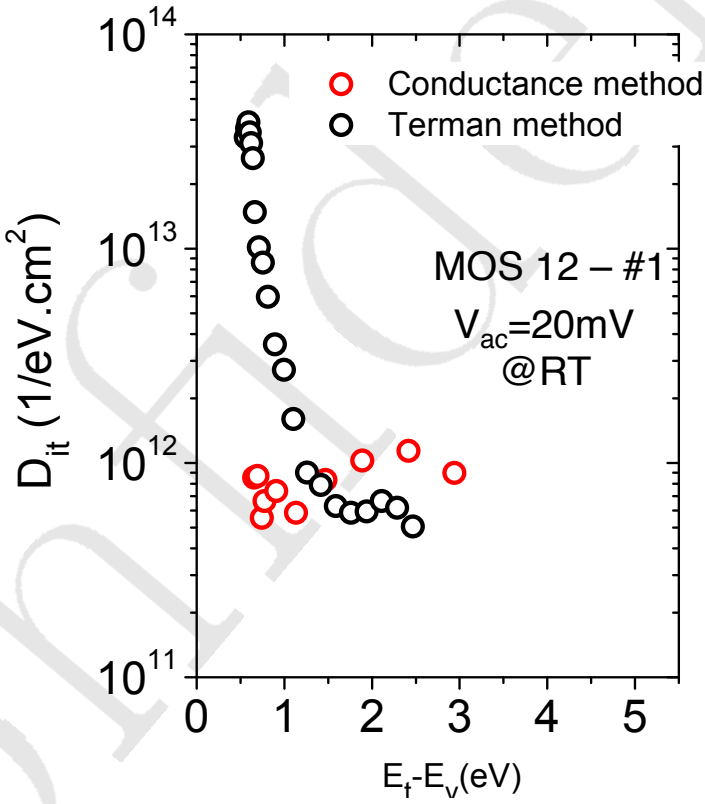

Figure 2.42: Comparison of the interface states density extracted from conductance method and Terman method. MOS12 - sample #1

The energy level of the trap states is calculated using the equation:

$$E_{it}\left(V_G\right) - E_v = \Psi_s\left(V_G\right) + \phi_p \tag{2.46}$$

where $\Psi_s\left(V_G\right)$ is extracted in the previous chapter and $\phi_p \simeq \left(\frac{kT}{q}\right)\ln\left(\frac{N_v}{N_A}\right)$ which is around 0.37 eV in the case of moderate boron doped diamond.

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A notable difference of the interface states density extracted from conductance method compared to the one of Terman's method is the interface states density near the valence band. While the Terman's method shows an elevated interface states density up to $4 \times 10^{13}\,(cm^{-2})$ at $E_{it} - E_v = 0.6$ eV, the results from conductance method are approximately one order of magnitude lower in the same energy range.

This discrepancy is actually due to the gate leakage current. In Terman's method [99], the variation of semiconductor surface potential Ψ_S with gate bias V_G is completely attributed to the interface states at semiconductor-oxide interface. It is true when leakage current through the oxide is negligible. However, when the DC current is sufficient, the potential drop on gate oxide is non-negligible. Therefore, in high injection regime, Terman's method highly overestimates the interface states density.

On conductance method, the contribution of DC current is actually excluded by equation 2.43. Final interface states density will therefore exclude the contribution from DC current. We conclude that the interface states density extracted from conductance method is more reliable than the Terman's method.

2.4.3.6 Interface states feature

By assuming interface states are single level states [85], i.e. Dirac energy distribution for the density of the trap, the equivalent conductance G_P/ω is simulated by using the equation:

$$\frac{G_P}{\omega} = \frac{C_{it}\omega\tau}{1+\omega^2\tau^2} \tag{2.47}$$

where τ is the characteristics time constant of interface states and being determined at $\left(\frac{G_P}{\omega}\right)_{\max}$, where $\omega\tau = 1$. Interface states capacitance C_{it} is determined from the peak of the equivalent conductance G_P/ω as following: $C_{it} = 2\left(\frac{G_P}{\omega}\right)_{\max}$.

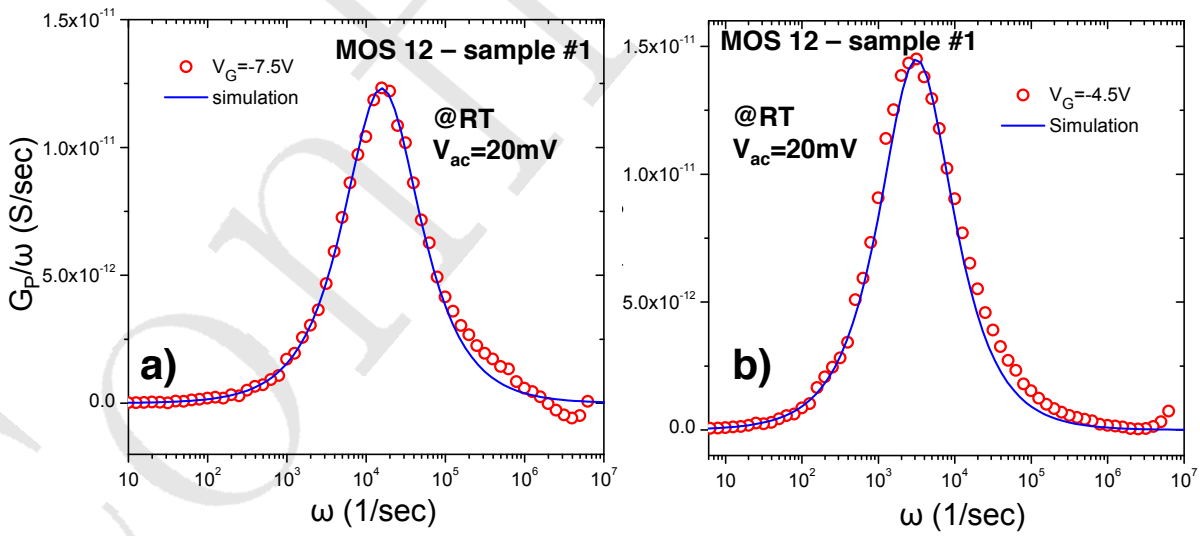

Figure 2.43: Representative equivalent conductance G_P/ω and the simulation by using single level interface state model at $V_G = -7.5V$ and $V_G = -4.5V$. (MOS 12 - Sample #1).

Figure 2.43 represents the experimental equivalent conductance $\frac{G_P}{\omega}$ at representative gate biases ($V_G = -7.5$ V and $V_G = -4.5$ V) and the simulation curves by using single

level interface state model (equation 2.47).

The simulation curves reproduced with a good agreement the experimental curves. Similar results are obtained for different V_G. Therefore, we conclude that single level interface state model is sufficient to describe the interface states between O-diamond/Al_2O_3 interface.

2.4.4 Capacitance-frequency dependence

With the latest interface states parameters evaluated, we have actually determined all parameters of the equivalent circuit (Figure 2.37c). Therefore, the capacitance-frequency characteristic of the system can be simulated to confirm the accurateness of the model. This simulation is performed by LTspice software [7].

Measurement method	MIMCAP	High frequency MOSCAP	Conductance G_P/ω	Characteristic frequency G_P/ω	Static I-V
Parameters / V_G(V)	C_{ox} (pF)	C_{sc} (pF)	C_{it} (pF)	R_{it} (MΩ)	G_{DC} (μS)
-8	70.8	35.8	24.2	2.6	0.64
-7	70.8	31.2	15.7	5.07	0.50
-6	70.8	26	20.9	4.8	0.33
-5	70.8	18.2	23.5	10.7	0.153
-4	70.8	13.36	32.2	19.68	0.05

Table 2.3: Input parameters for the LTSPICE simulation and the corresponding extraction method (MOS 12 - sample #1).

For the purpose of recall, we will summarize the parameters we have extracted and the corresponding extraction method.

Oxide capacitance C_{ox} was measured by using the MIM capacitor. Semiconductor capacitance C_{sc} was evaluated from MOS capacitor measured capacitance C_m at "proper frequency regime"($f = 100$ kHz), by using the relationship:

$$C_{sc} = \frac{C_{ox}.C_m}{C_{ox} - C_m} \tag{2.48}$$

Series resistance R_s is determined from "real part" of impedance measurements at "high frequency regime" $f = 1$ MHz. DC conductance is obtained from the statics I-V characteristics of the test device by using the derivation $G_{DC} = \frac{dI_{DC}}{dV_{DC}}$. Finally, interface states capacitance C_{it} and interface states resistance R_{it} were evaluated from the equivalent interface states conductance $\left(\frac{G_P}{\omega}\right)$. With interface states capacitance $C_{it} = 2\left(\frac{G_P}{\omega}\right)_{\max}$. Interface states resistance is evaluated by using the resonance frequency $\tau_R = \frac{1}{C_{it}R_{it}}$ of the trap states where $\left(\frac{G_P}{\omega}\right)$ show maxima.

The detailed parameters at different gate biases and the corresponding extraction method are represented in table 2.3.

[7] http://www.linear.com/solutions/ltspice

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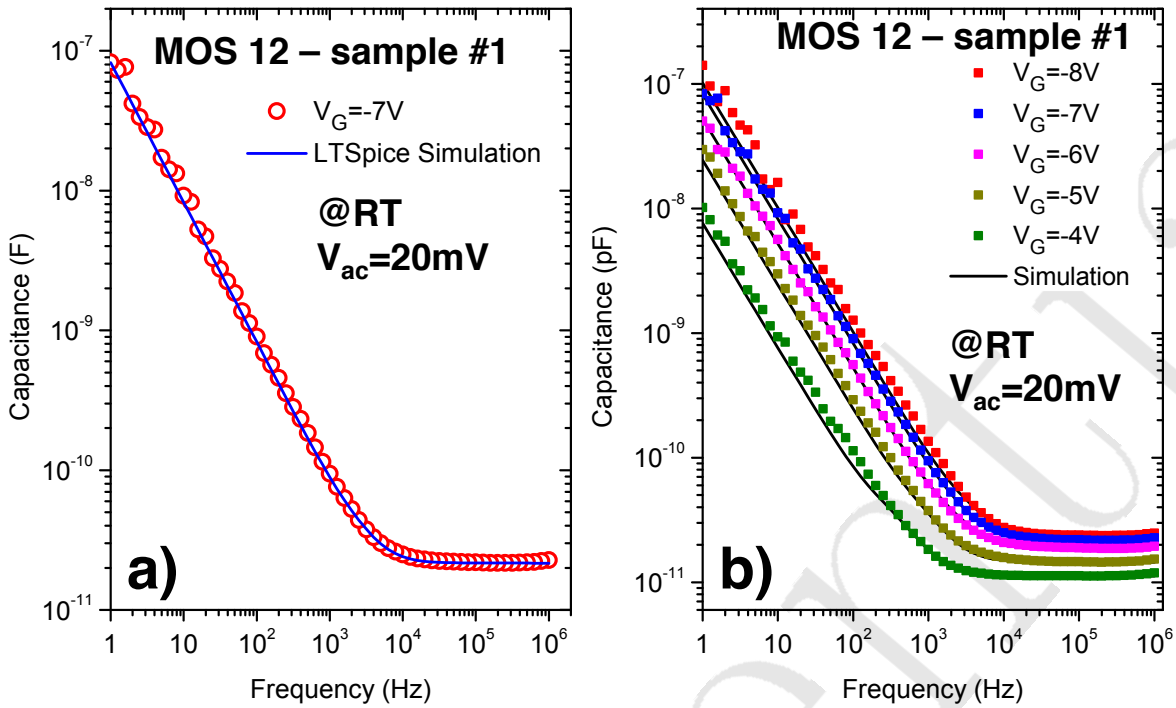

Figure 2.44: Capacitance-frequency dependence of the MOS capacitor test device by comparing the measurements and LTspice simulation a) $V_G = -7V$; b) At different V_G (MOS 12 - sample #1).

The LTSPICE capacitance-frequency $C_m - f$ simulation results are plotted in Fig. 2.44 along with the $C_m - f$ measurement results from MOS 12 - sample #1. The equivalent circuit perfectly reproduced the measured capacitance-frequency dependence. Therefore, we are able to conclude that the measured capacitance-frequency dependence effect observed in O-diamond MOS capacitor is originated from the gate metal carriers injected to interface states and then recombined with diamond valence band.

2.4.5 Electrostatics simulation

Taking into account the new interface state density extracted by conductance method, the electrostatics simulation can be re-performed. We apply here the same 1D simulation model as introduced in the Part 1 of this chapter and replace the interface charges from Terman method by the one extracted from conductance method.

The simulation results are compared with the experiment results by mean of semiconductor surface potential Ψ_s. As shown in Fig. 2.45, by using the interface states density extracted from capacitance method $\sigma_{it}(Capacitance)$, surface potential is firstly well matching with experimental results but then re-increased in the bias range where the test device is highly leaky. On another hand, by using the interface states density extracted by conductance method σ_{it} $(Conductance)$ where the potential drop on the oxide is excluded, electrostatics simulation is well-matching with the experiments. Fermi level pinning effect is reproduced and surface potential variation with gate bias is in good agreement. Therefore, we are able to conclude that this electrostatics model is adequate

for the O-diamond/Al_2O_3 MOS capacitor.

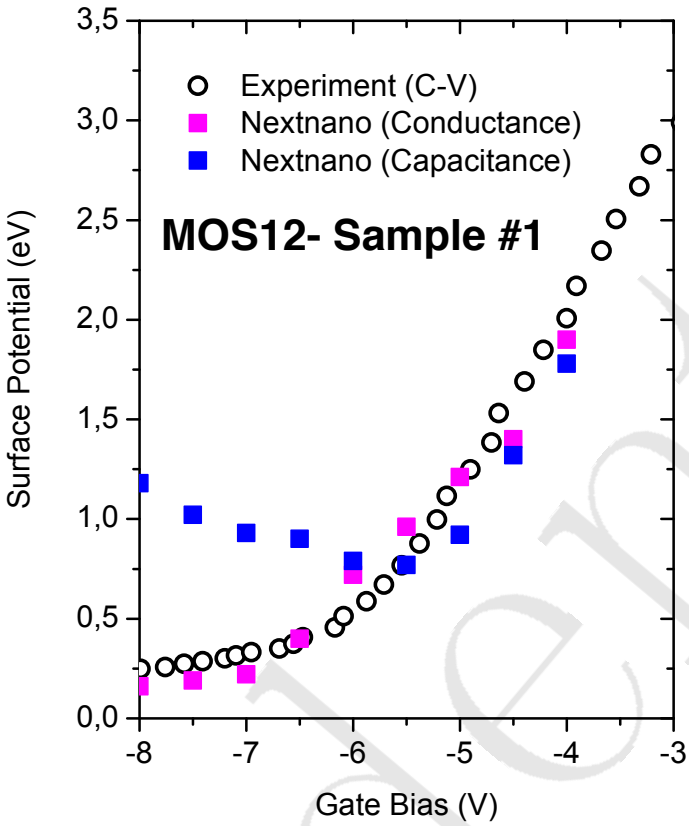

Figure 2.45: Semiconductor surface potential variation with gate bias determined from experiment and from nextnano simulation by using interface states density extracted from Terman method (blue curve) and conductance method (magenta curve).

Also, by identified the origin of FLPE (interface states and the carriers from gate metal injected into oxide and interface states), a new experimental recipe can be applied to eliminate the FLPE for a complete electrostatics gate controlled semiconductor. We will show in the perspective section our new recipe that allows us to eliminate FLPE in O-diamond MOS capacitor for a complete gate controlled boron doped diamond semiconductor.

2.5 Conclusion

In summary, this part was dedicated to elucidate the typical electrical characteristics of O-diamond MOS capacitor. Forward current (negative bias) mechanism is proposed where the oxide tunneling and semiconductor interface state recombination plays an important role. Oxide tunneling limiting process were identified and the corresponding approximation were made. By subtracting DC current, equivalent conductance $\frac{G_P}{\omega}$ and interface states density D_{it} were extracted. Single state model was found sufficient to correlate with experiment results. Impedance and capacitance measurements are well reproduced by simulating the equivalent circuit with all evaluated input parameters. Simulation results demonstrated that gate leakage current via interface states caused the

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capacitance-frequency dependence in O-diamond MOS capacitor. Complete electrostatic model for O-diamond MOS capacitor is also established.

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Part III

O-Diamond MOS capacitor under positive bias: current mechanism and capacitance-frequency dependent

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2.6 Motivation

As shown in Chapter 1, in order to realize a MOSFET, controlling semiconductor into deep depletion regime and/or inversion regime by biasing metal gate is necessary. As shown in the Part 1 of this chapter, one of the special interest with diamond is the capability to reach the deep depletion regime due to very long minority carrier generation time constant. Inversion regime has also been reported recently by Kovi et al. [20]. In the mentioned publication, the authors claimed that they obtained the inversion regime in a diamond MOSCAP by increasing the doping concentration of epilayer and temperature. This conclusion has been deduced from the capacitance-voltage (C-V) measurements of MOSCAP at different frequencies (as shown in Fig. 2.46).

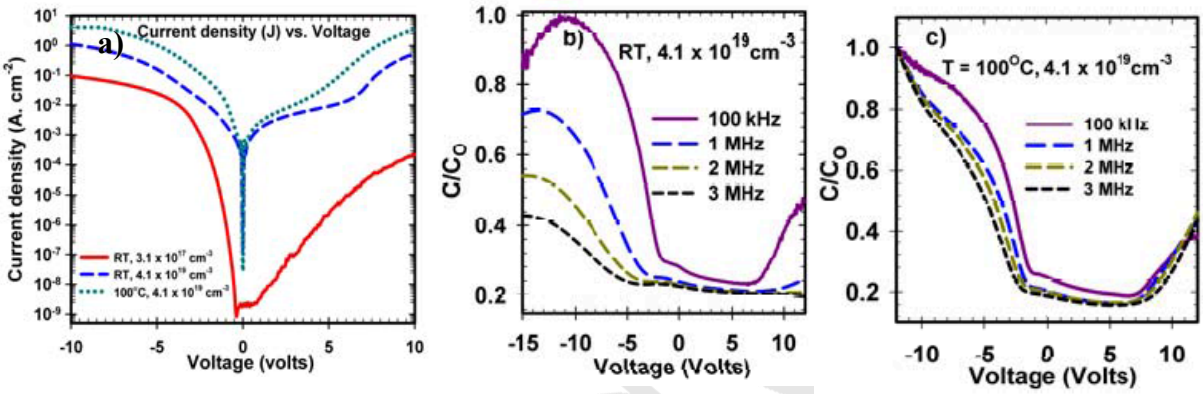

Figure 2.46: Current-Voltage and Capacitance-Voltage characteristic at different frequencies of O-diamond MOS capacitor presented by Kovi et al. [20].

However, this conclusion is indeed very problematic. First of all, reverse current in the capacitance measurement is very high, (almost 1 A/cm^2 at RT and 10 A/cm^2 at 100°C for the 4.1×10^{19} (cm^{-3}) sample, in Fig. 2.46a). Second, the applied frequency under "inversion" regime is very high. As shown in Fig. 2.46b)-c), they observed the so-called "inversion" by applying a frequency of $f \geq 100$ kHz. Considering the minority carriers generation time constant of silicon ($E_g = 1.11eV$) introduced in the Part 1 of this chapter, this mean that diamond ($E_g = 5.5eV$) minority carrier generation time constant is approximately hundred thousand time faster than silicon! This conclusion is in fact not understandable.

In fact, Chicot et al. [18] and us have also observed the similar effects in O-diamond MOS capacitors with epilayer doping concentration of 10^{17} (cm^{-3}), when leakage reverse current (positive bias) occurs. For instance, Figure 2.47 represents the I-V characteristic (Fig. 2.47a) and C-V characteristic at different frequencies (Fig. 2.47b) of MOS B12 - sample #3 (Figure 2.49). The electrical behavior of this MOS capacitor is very similar with the results reported by Kovi et al. [20]. Reverse current is observed and capacitance in reverse regime (positive bias) is highly increased with the decreasing of applied frequency.

However, on a MOS capacitors without reverse current, the so-called "inversion" is not present. For instance, it is clearly the case for the MOS C7 - sample #3 in Fig. 2.49. The electrical characteristics of this MOS capacitor are shown in Fig. 2.48. Figure 2.48a represents the I-V characteristic and Figure 2.48b represents the C-V curves at

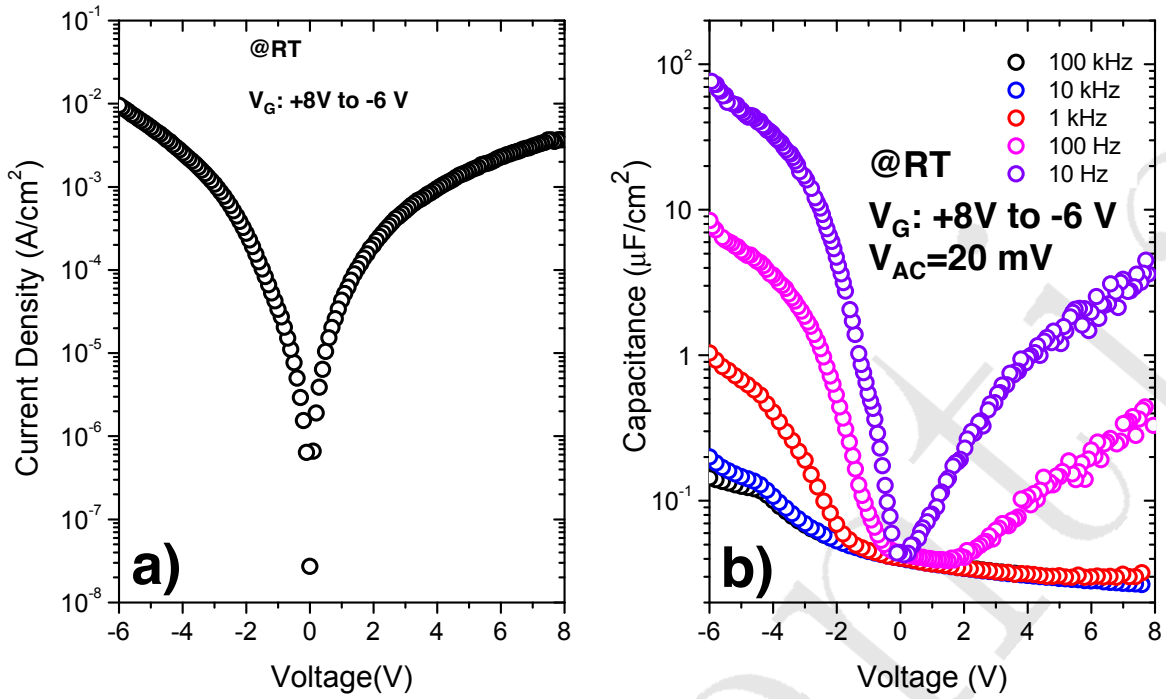

Figure 2.47: a) Current-Voltage and b) Capacitance-Voltage characteristics at different frequencies of the MOS B12 (sample #3).

different frequencies. When a reverse current is not observed, the so-called "inversion" is not present, even at a very low frequency (10 Hz).

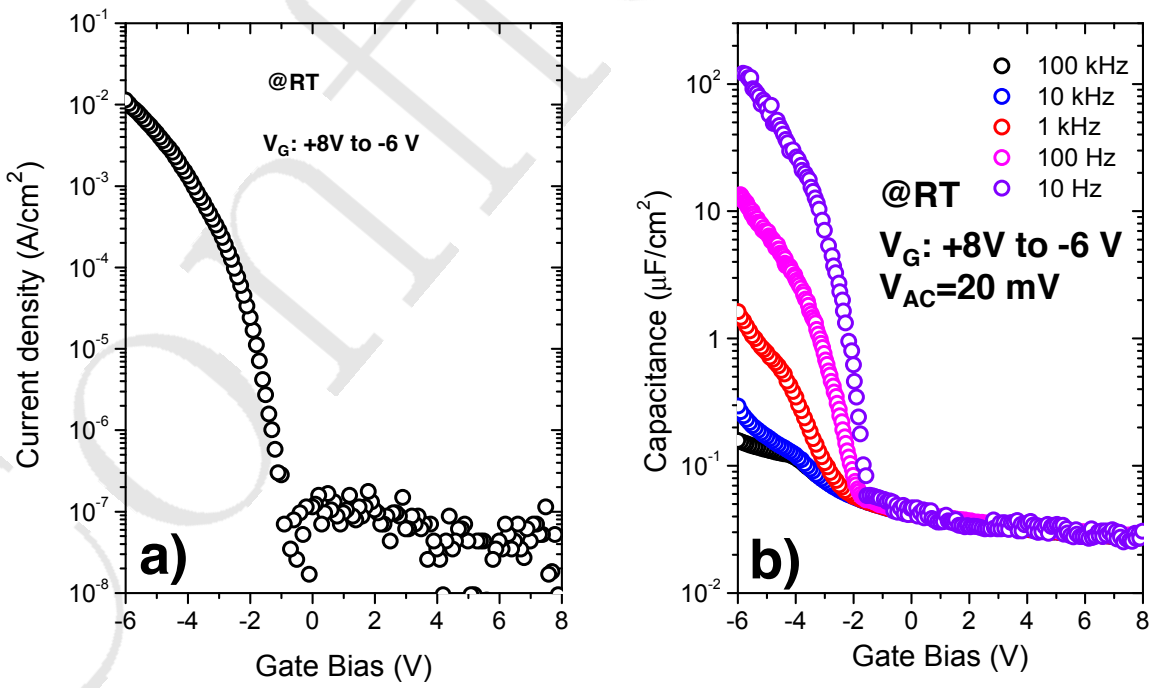

Figure 2.48: a) Current-Voltage and b) Capacitance-Voltage characteristics at different frequency of the MOS C7 (sample #3).

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By systematically measuring different MOS capacitors on a same substrate [8], a similar relationship is observed. Figure 2.49 represents the mapping reverse current and capacitance-frequency dependence of different MOS capacitors on sample #3. Green color indicates the MOS capacitors without reverse current (below 10^{-7} A/cm^{-2} at positive bias) and consequently without capacitance-frequency dependence in reverse regime. Red color indicates the MOS capacitors with reverse current and subsequently capacitance-frequency dependence in reverse regime. Orange color only indicates the MOS capacitors which have metal problem due to lift-off.

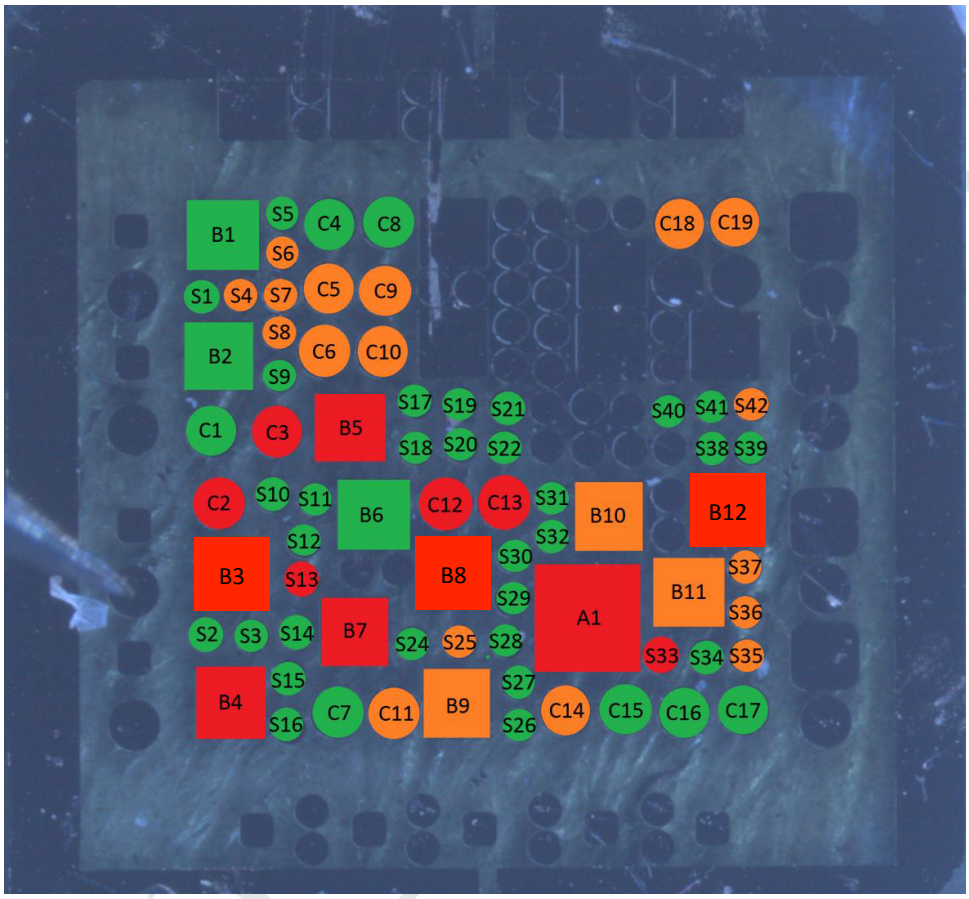

Figure 2.49: Reverse current distribution of different MOS capacitors of sample #3. Green color indicates the MOS capacitors without reverse current (below 10^{-7} A/cm^{-2} at positive bias). Red color indicates the MOS capacitors with reverse current.

From the above observation, we conclude that the so-called "inversion" in O-diamond MOS capacitor is actually a capacitance-frequency dependence effect which is directly a consequence of reverse current in positive bias. Therefore, questions are raising on origin of reverse current and the relationship between DC reverse current and a.c measurements.

We are going to solve the mentioned questions in this work. After the motivation, we will introduce our approach to elucidate the origin of reverse current. A special attention is paid to correlate substrates profile with MOS capacitor's electrical characteristics. The combination of different electron beam microscopy techniques is used to elucidate the

[8] done by D. Valenducq, a master 1 internship from University Grenoble Alpes at SC2G, Institut NEEL

role of substrate on the electrical characteristics of the test device. The reverse current effects on small a.c signal measurements is modeled by an electrical equivalent circuit. The measured capacitance-frequency curve is compared with the simulated results from the equivalent circuit. Finally, we will conclude our works.

2.7 Results and Discussion

As shown in Fig. 2.49, reverse current (under positive bias) is randomly observed even on the same substrate. Since reverse current is not universal, substrate imperfection is highly suspected as the origin. In fact, defects and dislocation on the substrates were found playing an important role in other diamond devices such as Schottky diode [121][122] or Metal-Semiconductor-Metal photodetector [123].

2.7.1 Device characteristics-substrate profile correlation

We will firstly recall the plan view structure of our MOS capacitor test devices. Figure 2.50a represents the optical photograph of sample #1.

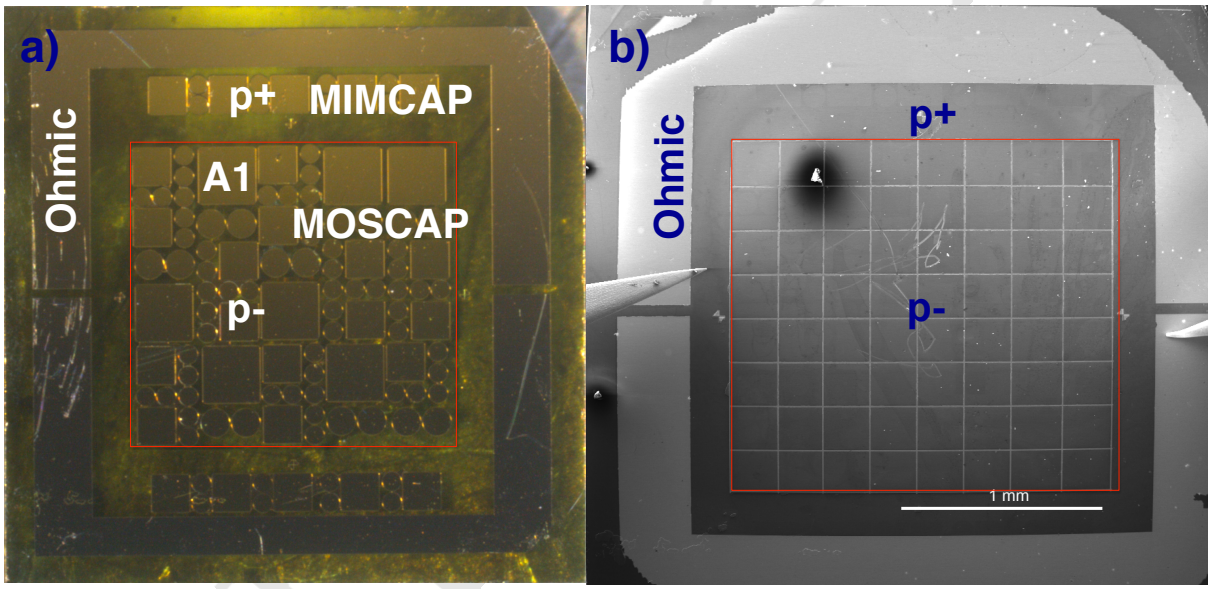

Figure 2.50: a) Optical photograph of the completed test devices (sample #1) including ohmic contact, MIM capacitor and MOS capacitor; b) the FESEM image of substrate in Figure 2.49a after removing gate metal, gate oxide and redeposited ohmic contact on p+ region and grids on p- region for device electrical characteristics-substrate profile correlation.

The test device structure consists of the ohmic contact and MIM capacitor on the p+ region and the MOS capacitor on the p- region. In order to correlate substrate profile with MOS capacitor electrical characteristic, we eliminate gate electrode and gate oxide of the sample after all electrical measurements have been done. The chemical etching by "the aqua-regia" solution is employed. Then, the substrate is immersed in KOH solution. After that, we employed a new lithography process to define a 8×8 grids into the p- region of the substrate (the region previously with MOS capacitors). Ohmic contacts were

also re-deposited onto p+ layer. Figure 2.50b represents the Field Emission Scanning Electron Microscopy (FESEM) photograph of the substrate after the test devices were removed, grid region and ohmic contact were re-deposited. By comparing the plan view structure of test devices with grid region, we were able to determine the substrate region corresponding to each specific MOS capacitors.

Figure 2.51a represents the semilog I-V characteristics of the MOS A1 - sample #1 where reverse current was observed. Figure 2.51b represents the reverse I-V characteristics in log-log scale. Linear fitting indicates the current-voltage power law of I∼V^4 in reverse regime.

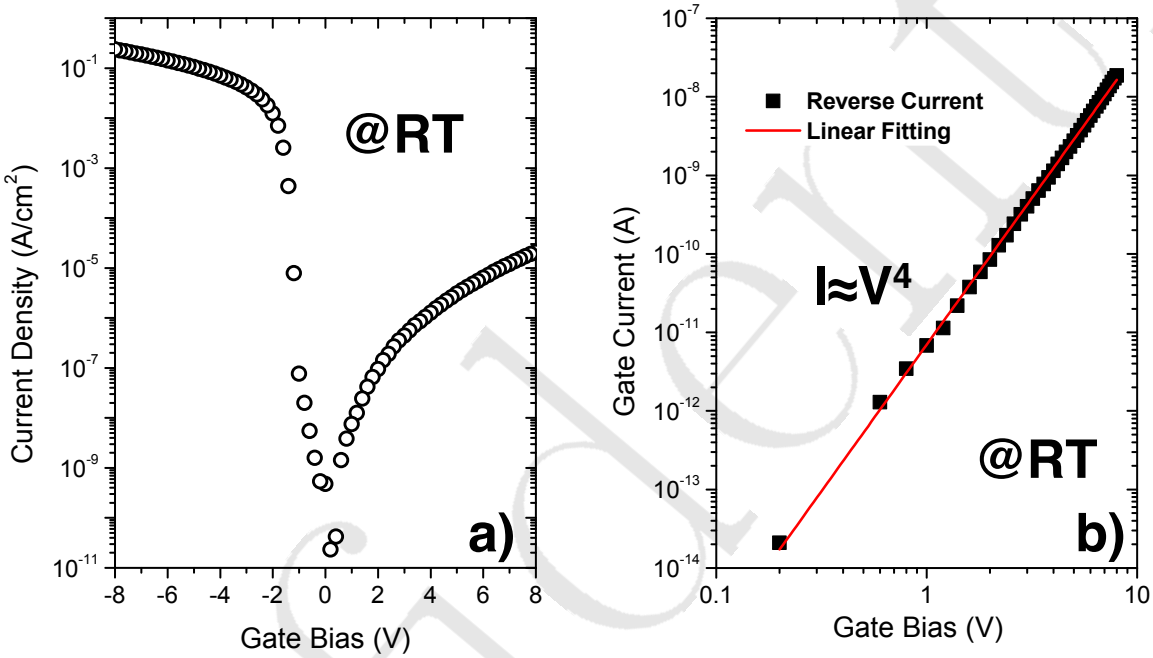

Figure 2.51: a) Current-voltage characteristics of the MOS A1 - sample #1 (Figure 2.50) in semilog plot; b) Reverse current-voltage characteristic (gate under positive bias) in log-log plot (Sample #1).

2.7.1.1 Combined FESEM and electrical measurement

Substrate region corresponding to the MOS A1 - sample #1 is then examined by Field Emission Scanning Electron Microscope (FESEM). Figure 2.52 represents the FESEM image of this grid region at different resolutions. A special notice has been paid to two defective spots: the hexagonal LS1 (Fig. 2.52b) and the rectangular LS2 (Fig. 2.52c).

By employing the FESEM system operated with the micromanipulator system [124], we directly probed the defective spots and measured their electrical characteristic. Ohmic contact was grounded by one tip and the second tip with a radius curvature of 1 μm was mounted on the top of the defective spots. The I-V characteristics of the defective spot were then measured by using Keithley 2611 Electrometer.

Figure 2.53a represents the semilog I-V characteristics of the defective sites under positive bias. The corresponding log-log plot is shown in Fig. 2.53b. A current-voltage ohmic

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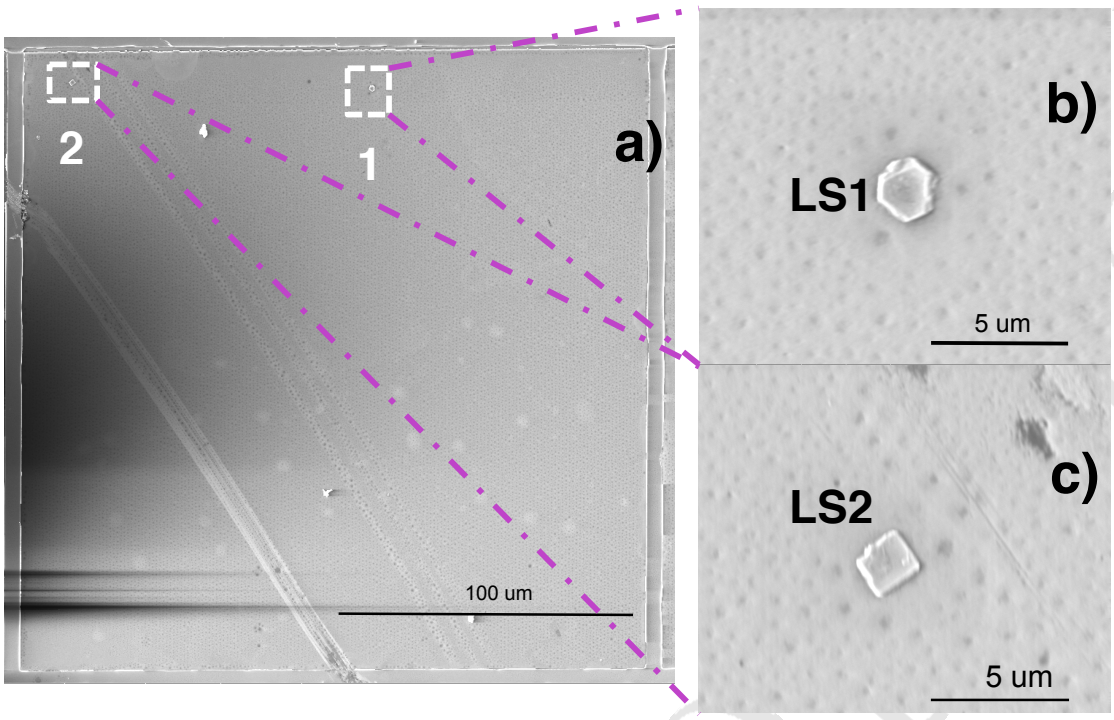

Figure 2.52: a) FESEM image of the grid region corresponding to the A1 MOS capacitor. b) the hexagonal defective leakage spot and c) the rectangle defective leakage spot in the grid region (Sample #1).

law I∼V is obtained from linear fitting the log-log plot. This characteristics indicates that the defective spots have the electrical characteristics similar to a resistance.

By applying the identical measurement configuration and probing the second tips outside the defective spots, current under detection limit is observed (Figure 2.53a, the open black circular). We concluded these defective spots are the killer defect directly related to the reverse current of the MOS capacitor.

2.7.1.2 Cathodoluminescence

We also performed cathodoluminescence (CL) measurements to correlate the localized A-band luminescence to the killer defects. In fact, there are number of discussions on correlating localized band-A-luminescence to killer defects on homoepitaxial diamond devices [121][122]. For the current study, we performed CL spectrum and CL mapping on different grid regions and correlate to electrical characteristics of MOS capacitors. As shown in Fig. 2.54, localized A-band at approximately 420 nm were found at different positions. However, there were no clear correlation between MOS capacitor reverse current and A-band CL. We also employed the micromanipulator system using the identical measurement configuration to measure the electrical characteristic of A-band defective spots. A systematic correlation between A-band defective sites and electrical leakage current was not obtained, as already noticed by Ohmagari et al. [121].

This could be related to the origin of A-band luminescence. The impurities aggregation and segregation at defect positions [123][125] is claimed to be at the origin of A-band luminescence. However, since not all the defect sites are killer defects, A-band are not necessary revealed to killer defects. Therefore, it could be confusing to use CL to identify

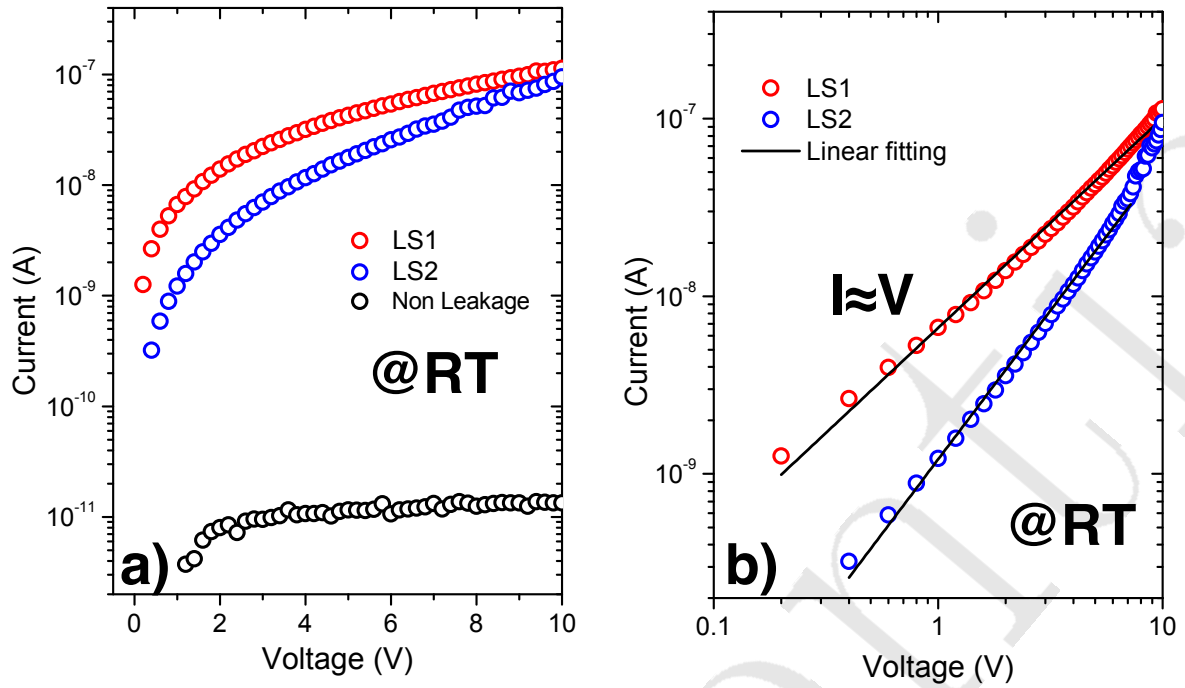

Figure 2.53: a) Current-Voltage characteristics of defective spots under positive bias in semilog plot; b) Current-Voltage characteristics of defective spots under positive bias in log-log plot (Sample #1).

killer defects.

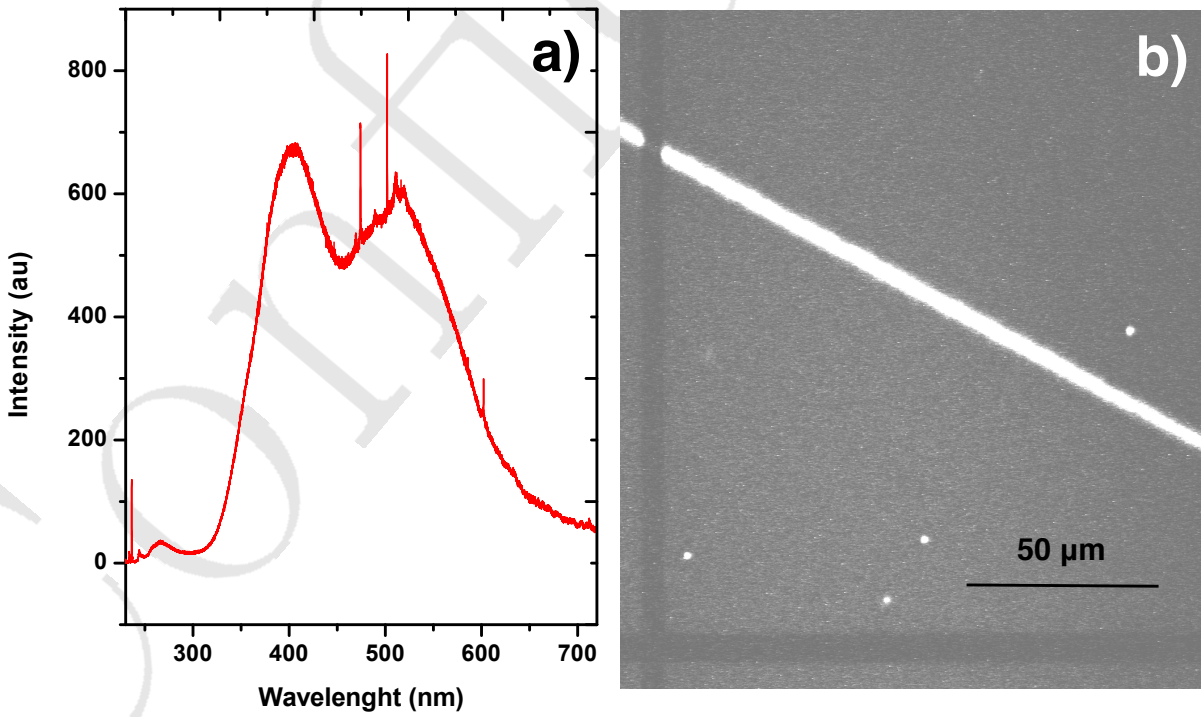

Figure 2.54: a) CL spectrum of diamond substrate; b) CL mapping of diamond substrate recorded at A-band luminescence (sample #1).

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2.7.1.3 Transmission Electron Microscope (TEM)

In order to investigate the features of the defective leakage spots, Transmission Electron Microscopy (TEM) is employed. TEM preparation and measurement had been done by the group of Prof. Daniel Araujo at Cadiz University- Spain. TEM lamella has been prepared by Focus Ion Beam (FIB) technique. Firstly, a Platinum (Pt) film is deposited on top of the defective site LS2 to protect the structure, as shown in Fig. 2.55. After FIB cutting, the lamella was polished several times to obtained the desired thickness (approximately 100 nm) for the TEM measurement.

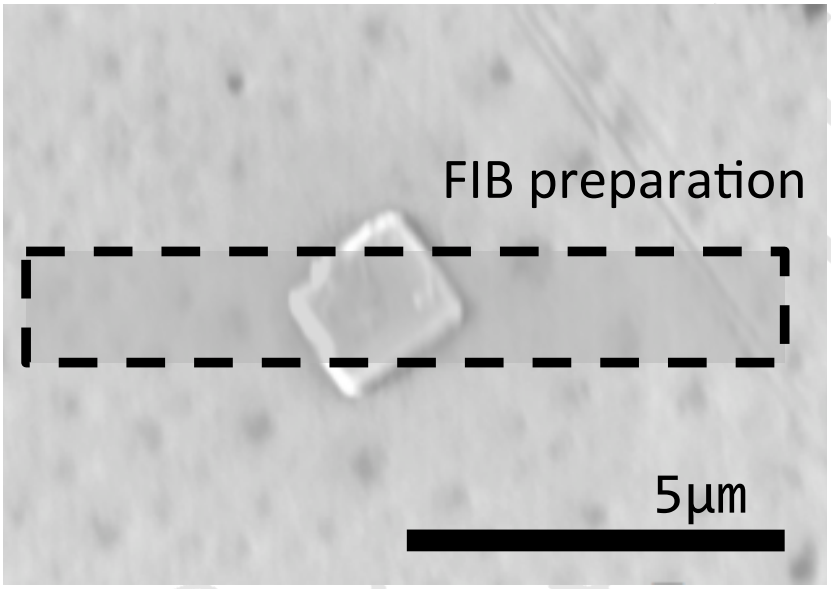

Figure 2.55: FIB preparation for TEM measurement (Sample #1).

TEM image of the defective site LS2 is shown in Figure 2.56a.

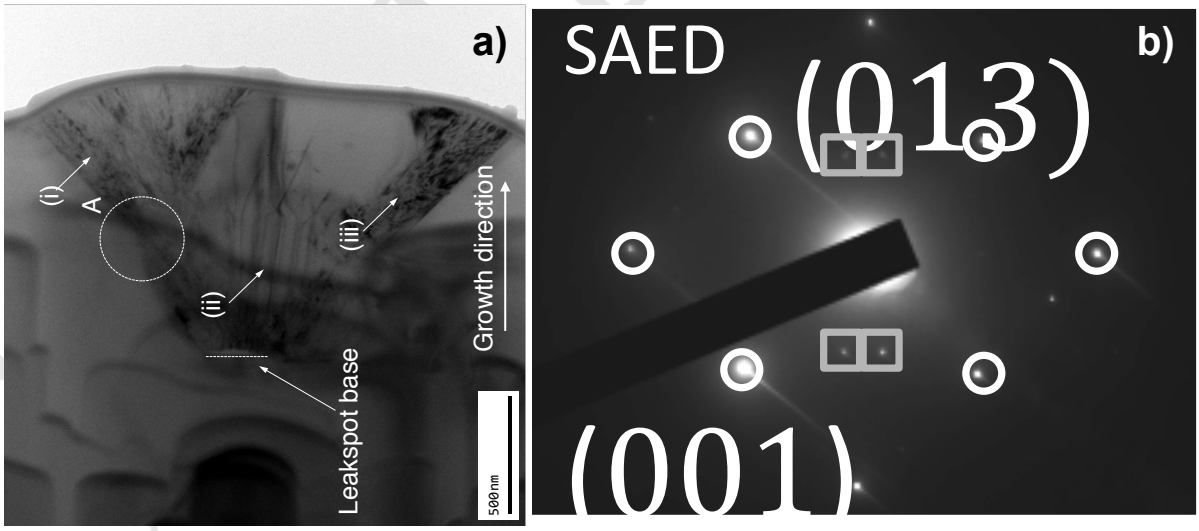

Figure 2.56: a) TEM image of the defective leakage spot; b) Selected Area Electron Diffraction SEAD pattern obtained at position A of Figure 2.56a (sample #1).

The depth of leakage spot is around 900 nm from diamond surface and 1100 nm from leakage spot surface. The leakage spots are initiated from the substrate and have a faster

growth rate than homoepitaxial diamond. Bunch of dislocations were found inside the leakage spot, which was revealed as the indication (i)-(iii) in Fig. 2.56a). Figure 2.56b represents the Selected Area Electron Diffraction (SAED) pattern acquired at position A in Fig. 2.56a.

The SEAD pattern at the substrate and at center of defective spots were also measured separately, as represented in Fig. 2.57. Zone axis of the diffraction pattern measured at the substrate verified the conditions of the 001 pole, where A/B = 1.414 (Fig. 2.57a). Zone axis of the diffraction pattern measured at the center of the defective leakage spot verified the conditions of the 013 pole, where L/M = 1.658 (Fig. 2.57b). Substrate and leakage spot zone axis were superimposed at the boundary (position A of Fig. 2.56a), so that the substrate zone axis 001 and leakage spot zone axis 013 are revealed (Fig. 2.56b).

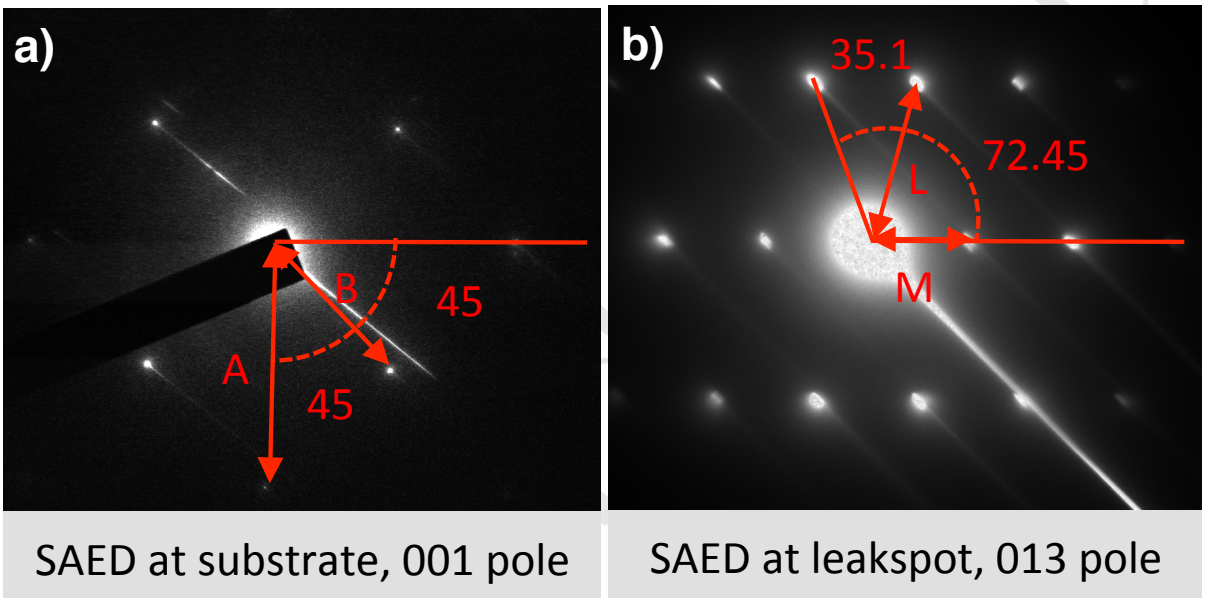

Figure 2.57: Selected Area Electron Diffraction pattern obtained at a) Substrate; b) center of defective leakage spot (sample #1).

By using the relationship:

$$\cos\alpha = \frac{d_{100}}{d_{013}} \tag{2.49}$$

With $d_{hkl} = \frac{a}{\sqrt{h^2+k^2+l^2}}$ where a=0.365 nm is the diamond lattice constant. A $cos\alpha = 0,9487$ which is equivalent with an angle between two crystallographic orientations of α =57.0743^o is determined. We conclude that the diamond-like non-homoepitaxially crystallite with bunch of dislocation inside is the feature of diamond killer defects.

2.7.2 Reverse current mechanism

2.7.2.1 Current mechanism

As we have shown, reverse currents are related to defective leakage spots in the substrate. Figure 2.58 represents our proposed reverse current mechanism. Two sections are included: The section surrounded by blue dash represents the area without defective leakage spots. Since positive voltage is applied, SCR width of diamond epilayer is expanding.

Carriers are not allowed to flow through this region. The corresponding electrostatic band diagram is represented in the left hand side of Fig.2.58.

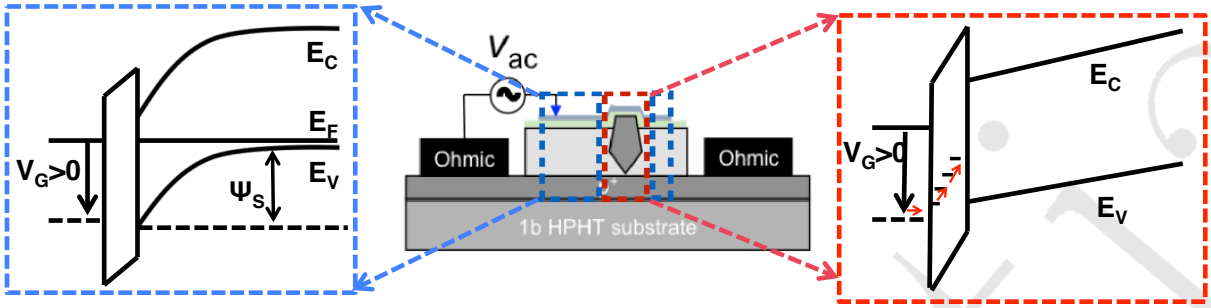

Figure 2.58: Proposed current mechanism and its corresponding electrostatic band diagrams.

When the defective leakage spots are present, the corresponding configuration is shown in the section surrounded by red dash. Since defective leakage spots are equivalent with a resistance, no SCR is able to form. This region is conducting. The proposed electrostatic band diagram corresponding to this region is represented in the right hand side of Fig.2.58.

For the current mechanism, we propose the current mechanism as in Fig. 2.58. Hole from gate metal are suggested to initiate the current flow. Hole firstly being tunnelled into oxide and then hopping through the oxide [106][107][108][118]. Once holes approach the diamond surface, only the region with defective leakage spots are allowed the carriers flowing through. The MOS capacitor without leakage spots will be insulated and no reverse current will be observed.

2.7.2.2 Limiting process

To identify the limiting process, we reconsider the current-voltage power-law from the log-log plot in Fig. 2.51 and Fig. 2.53.

The $I \propto V^4$ of MOS capacitor in Fig. 2.51b indicates that bulk oxide is not the limiting process [106][116][117]. Carriers transport in defective leakage spots are followed ohmic law $I \propto V$, as shown in Fig. 2.53b. Furthermore, the equivalent resistance of defective leakage spots is much lower than the resistance of MOS capacitors. We conclude that the transport through defective sites is not the limiting process. Therefore, for the gate bias range V_G=-8V to V_G=+8 V in current work, limiting process of reverse current is identified as the tunneling from metal to the oxide traps states [118].

Current-voltage were also measured at different temperatures to examine the thermal activation process, as shows in Fig. 2.59a. Current value for V_G=7V at different temperature is plotted in Fig.2.59b. By applying the Arrhenius plot, a thermal activation energy of $E_A \simeq 142\ meV$ was evaluated. This thermal activation energy is assigned to the process at the barrier between metal and the Fermi-Dirac occupation function of the trap states in the oxide [118].

2.7.3 Capacitance-frequency dependence

As shown in Fig. 2.47 and Fig. 2.48, reverse current (positive bias) is the origin of the so-called "inversion" in O-diamond MOSCAP. In order to elucidate the role of reverse

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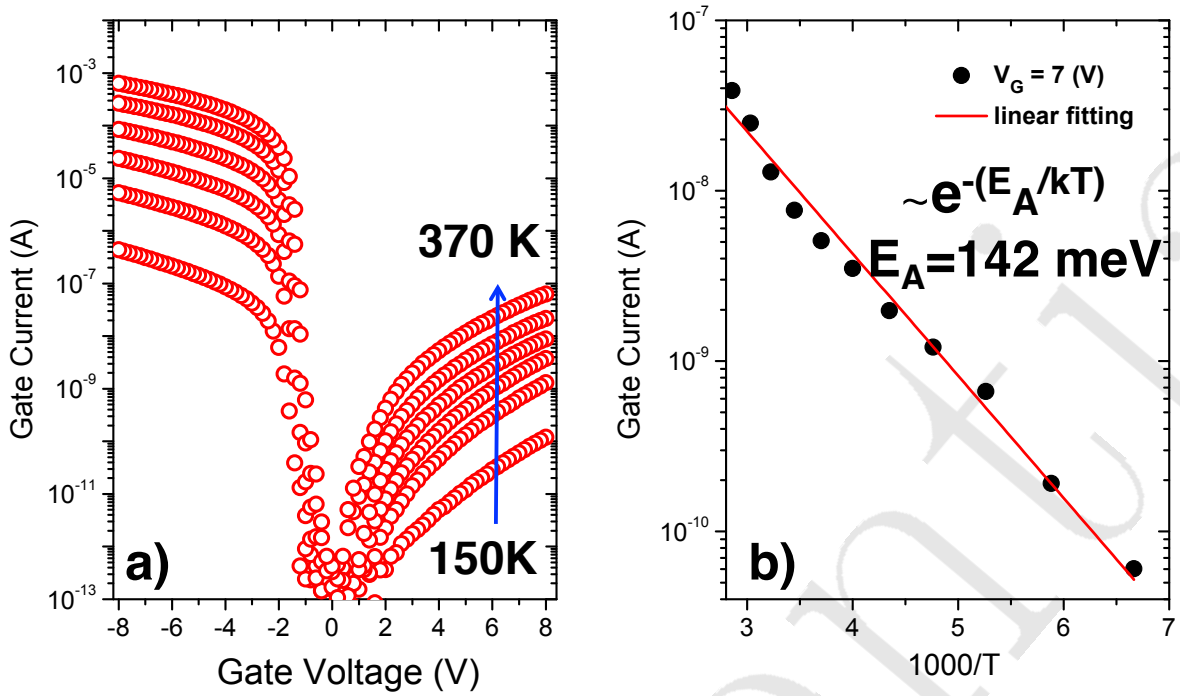

Figure 2.59: a) Current-Voltage of MOS capacitor measured at different temperatures, ranging from 150K to 370K; b) Arrhenius plot of current measured at different temperatures when gate are biased at V_G=7V (MOS A1 - sample #1).

current on capacitance measurement, the capacitance-frequency measurement ($C_m - f$) were performed. For the sake of remembering, this C-f curve is equivalent with the cutline of C-V curves at different frequencies when V_G is fixed. The open circular curve in Fig. 2.61 represents the measured $C_m - f$ curve at V_G=7V. The C-f dependence is clearly observed at low frequency range ($f < 1$ kHz).

2.7.3.1 Equivalent circuit

In order to model the effect of reverse current on $C_m - f$ measurements, we linearized the characteristics around a DC bias by an equivalent circuit. Figure 2.58b represents the proposed equivalent circuit which is based on the current mechanism (Figure 2.58). The area surrounded by a blue dash is corresponding to an ideal MOS capacitor in deep depletion regime. The semiconductor SCR is in series with oxide capacitance C_{ox1} and oxide conductance G_{ox1}. The area surrounded by a red dash represents the equivalent circuit corresponding to the defective leakage spots area. Resistance of defective leakage spots $R_{crystallite}$ are in series with oxide capacitance C_{ox2} and oxide conductance G_{ox2}. Oxide capacitance (C_{ox1} and C_{ox2}) are corresponding to the effective area of the non-defective area and the defective area, respectively.

2.7.3.2 Impedance Simulation

Parameters Extraction The area of the defective leakage spots $S_{crystallite}$ are determined from FESEM measurement. The corresponding capacitance C_{ox2} can be evaluated

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from the equation:

$$C_{ox2} = \frac{\varepsilon_0 \varepsilon_{ox} S_{crystallite}}{t_{ox}} \tag{2.50}$$

Because C_{ox1} and C_{ox2} are two capacitances in parallel, the oxide capacitance C_{ox} is equivalent with: $C_{ox} = C_{ox1} + C_{ox2}$. The C_{ox1} is therefore evaluated by using:

$$C_{ox1} = C_{ox} - C_{ox2} \tag{2.51}$$

where C_{ox} is the oxide capacitance measured from MIM capacitor.

Semiconductor capacitance C_{sc} is evaluated from "proper frequency" capacitance measurements as discussed in the previous part. By using the equation:

$$C_{sc} = \frac{C_{ox} C_m}{C_{ox} - C_m} \tag{2.52}$$

where C_m is the MOS capacitor measured capacitance at high frequency range.

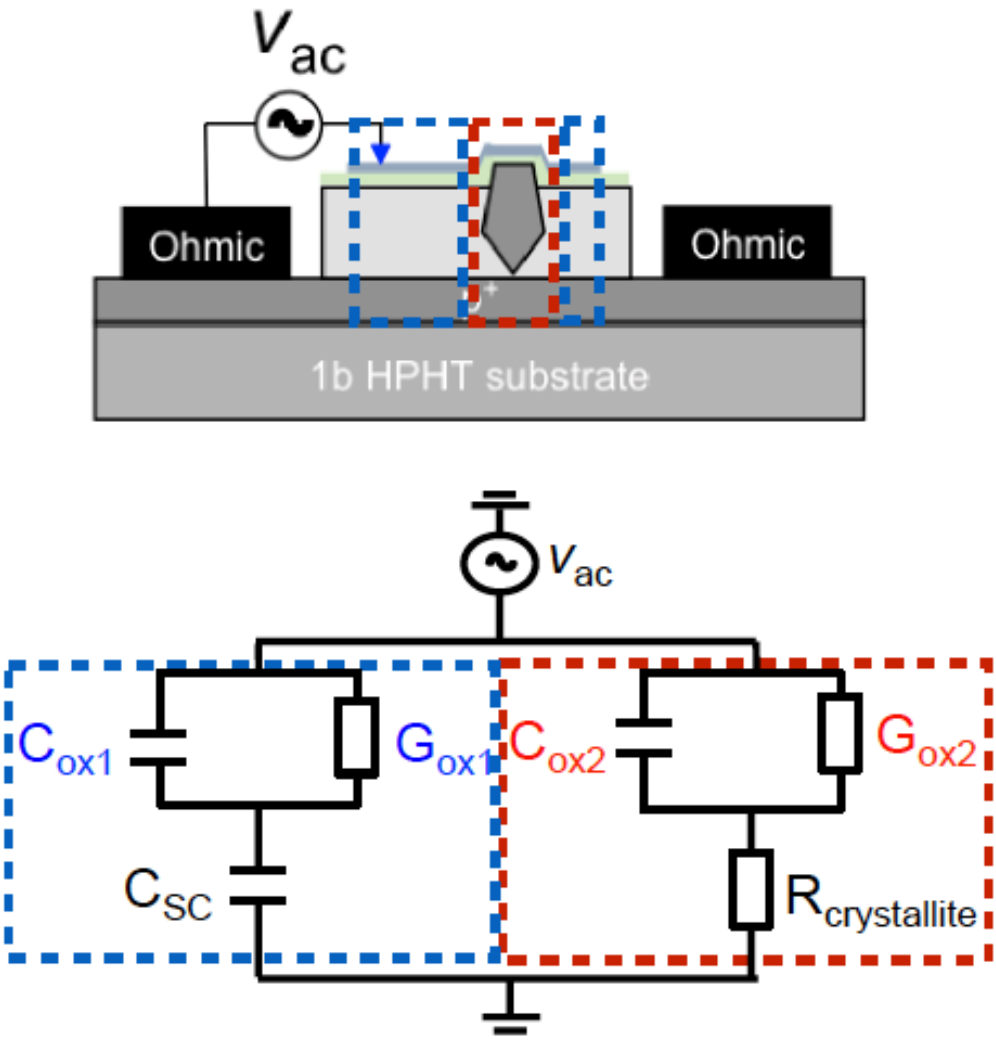

Figure 2.60: Proposed equivalent circuit which is corresponding to the current mechanism for simulating the a.c measurement.

$R_{crystallite}$ is the equivalent resistance of the defective leakage spots. The MOS A1 - sample #1 consists of two defective spots in parallel. Therefore, the equivalent $R_{crystallite}$ can be calculated as:

$$R_{crystallite} = \frac{R_1 \times R_2}{R_1 + R_2} \tag{2.53}$$

where R_1 and R_2 are corresponding to the resistance of the LS1 and LS2 defective leakage spots, which were determined from I-V measurement. The conductance of the crystallite is then evaluated by the inverse of $R_{crystallite}$.

From DC I-V measurement of the MOS capacitor, the DC conductance G_{DC} is evaluated by the derivation:

$$G_{DC} = \frac{dI_{DC}(MOS)}{dV_{DC}(MOS)} \tag{2.54}$$

We considered that DC transport is a process of two serial processes: conduction in the oxide G_{ox} and conduction in the crystallite $G_{crystallite}$. By assuming G_{ox1} is not contributing to the DC transport, the G_{ox2} is evaluated as:

$$G_{ox2} = \frac{G_{DC} \times G_{crystallite}}{G_{crystallite} - G_{DC}} \tag{2.55}$$

In summary, all the parameters in the proposed equivalent circuit can be experimentally determined for an empirical simulation. Table 2.4 represents the parameters we introduced for the impedance simulation. The corresponding extraction method are also indicated.

Measurement method	MIMCAP	FESEM	C_{ox}-C_{ox2}	High frequency MOSCAP	I-V defect	I-V defect	$\frac{R_{LS1} \times R_{LS2}}{R_{LS1} + R_{LS2}}$	$1/R_{crystallite}$	IV MOSCAP	$\frac{G_{DC} \times G_{crystallite}}{G_{crystallite} - G_{DC}}$
parameters / V_G(V)	C_{ox} (pF)	C_{ox2}(pF)	C_{ox1}(pF)	C_{sc} (pF)	R_{LS1}(Ω)	R_{LS2}(Ω)	$R_{cristallite}$(Ω)	$G_{crystallite}$(S)	G_{DC}(S)	G_{ox2}(S)
7	360	1	359	27.8	7.1×10^{7}	1.2×10^{8}	4.46×10^{7}	2.7×10^{-8}	6.54×10^{-9}	9.14×10^{-9}

Table 2.4: Input parameters for the a.c impedance/capacitance simulation and its corresponding extraction method.

Impedance Simulation With all the parameters of the equivalent circuit experimentally determined, the $C_m - f$ curve can be simulated.

The red line in Figure 2.61 represents the simulated capacitance-frequency curve by using the equivalent circuit in Figure 2.60 and the parameters in table 2.4. The simulation curve unambiguously reproduces the measured $C_m - f$ curve. We conclude that the reverse current via defective leakage spots in the epilayer is responsible for the $C_m - f$ dependent. Without reverse current, no $C_m - f$ dependent is observed. We conclude that the conclusion on minority carrier inversion given by Kovi et al. [20] is most probably an effect from their enormous reverse current.

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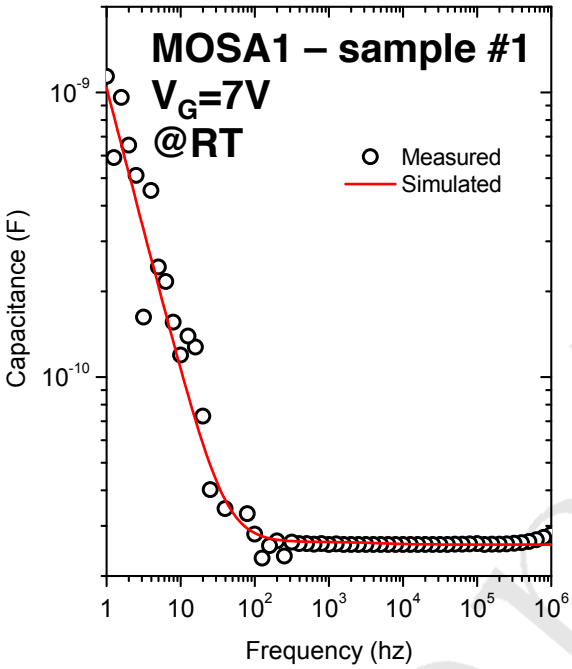

Figure 2.61: Capacitance-frequency dependent in the reverse regime from a.c measurement (closed black circular) and simulation (red line).

2.8 Conclusion

In this work, we investigated the origin of reverse current in O-diamond MOS capacitors. The correlation between substrate profile with MOS capacitors electrical characteristics were done. Diamond-like defective leakage spots with bunch of dislocations inside were found to be responsible for the reverse current at positive bias. Localized A-band peak in CL measurement are not necessary representing the killer defects. Hole injection from metal gate is suggested as the origin of reverse current in O-diamond MOS capacitor. Reverse current caused the capacitance-frequency dependence on C-V measurements. The impedance simulation by using the equivalent circuit with all quantified parameters has unambiguously demonstrated the relationship between reverse current and capacitance measurement. Minority carriers inversion claimed by Kovi and co-authors [20] is most probably an effect from parasitic reverse current.

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2.9 Conclusion of Chapter 2

In summary, this chapter has been dedicated for the understanding of oxygen terminated boron doped diamond MOS capacitor.

Part 1 introduced a new technical approach to reduce series resistance and improve gate oxide in fabricating O-diamond MOS capacitor test devices. We introduce the complementary measurement techniques to obtain a proper C-V measurements. Systematic measurement were performed to ensure the reliability and reproducibility of the system. Crucial information on the MOS capacitor system were obtained. An effective gate controlled diamond SCR width was demonstrated. It is promising to fabricate a depletion mode diamond MOSFET.

Part 2 elucidated the typical electrical characteristics of O-diamond MOS capacitor. Forward current mechanism is proposed where the oxide tunneling and semiconductor interface states recombination played an important role. Oxide tunneling limiting process were identified and the corresponding approximation were made. By subtracting DC current, equivalent conductance $\frac{G_P}{\omega}$ and interface states density D_{it} were extracted. Single state model was found sufficient to correlate with experiment result. Impedance and capacitance measurements are well reproducing by simulating the equivalent circuit with all evaluated input parameters. Simulation results demonstrated that gate leakage current via interface states caused the capacitance-frequency dependence in O-diamond MOS capacitor. Complete electrostatic model for O-diamond MOS capacitor is also established.

Part 3 investigated the origin of reverse current in O-diamond MOS capacitors. The correlation between substrate profile with MOS capacitors electrical characteristics were done. Diamond-like defective leakage spots with bunch of dislocations inside were found to be responsible for the reverse current. Localized A-band peak in CL measurement are not necessary representing the killer defects. Hole injection from metal gate are suggested as the origin of reverse current in O-diamond MOS capacitor. Reverse current caused the capacitance-frequency dependence on C-V measurements. The impedance simulation by using the equivalent circuit with all quantified parameters has unambiguously demonstrated the relationship between reverse current and capacitance measurement. Minority carriers inversion claimed by Kovi and co-authors [20] is most probably an effect from parasitic reverse current.

Thanks to the effective gate controlled diamond SCR width, we will introduce our approaches to fabricate and investigate the depletion mode boron doped diamond MOSFET in Chapter 3.

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Deep depletion concept for diamond MOSFET

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Deep depletion regime is demonstrated in metal oxide semiconductor capacitors using p-type oxygen terminated (100) diamond as semiconductor and Al_2O_3 deposited by Atomic Layer Deposition (ALD) at 380°C. Current voltage I(V) and capacitance voltage C(V) measurements were performed to study the effectiveness gate control diamond semiconductor. An effective modulation of the Space Charge Region (SCR) in deep depletion regime is obtained for positive gate bias. The deep depletion metal oxide semiconductor field effect transistor (MOSFET) using boron doped diamond are demonstrated.

Due to silicon physical limitations, wide band gap semiconductors are attracting a lot of interest for next generation power electronics device application. Among them, diamond is widely recognized as the best material[1] due to its superior physical properties like extreme breakdown field, high thermal conductivity and elevated carrier mobilities. After decades of investigation, diamond epitaxial growth and doping control are well mastered. It opens the path to realize diamond MOSFET which is one of two critical elements of a power converter system, along with Schottky diode.

Most of the diamond based MOSFET have been developed thanks to the surface transfer doping concept on H-terminated diamond[2]. Such MOSFETs, including an oxide layer between the metal and the carrier channel[3-5] are promising devices able to combine low loss in on-state and high breakdown voltage in off-state with a stable behavior. Recently, diamond MOSFET based on O-terminated phosphorous doped diamond[6] working in inversion regime were also demonstrated. The on-state current of these two kind of MOSFETs is strongly dependent to the channel mobility at the interface between oxide and diamond. Indeed, the hole channel carrier mobility of these MOSFET is limited by interface phenomena (surface roughness scattering or interface states scattering) resulting in typical mobility of around 100 $cm^2.V^{-1}.s^{-1}$ for the best case. Thus, the full properties of diamond cannot be explored in such MOSFET. Achieving a hole channel mobility having values comparable to bulk mobility[7] remains a challenge. On the other hand, bulk channel boron doped diamond can be used in MESFET as recently demonstrated[8]. In that case, bulk hole mobility can be achieved but the on-state current of this device is limited by the low doping level required ($N_A \lesssim 10^{16}$ cm^{-3}) to preserve the Schottky contact at the gate without excessive leakage current. In this context and thanks to the oxide barrier, boron doped deep depletion mode MOSFETs are good alternative which will permit to use higher doping level combined with bulk mobility.

The boron doped deep depletion mode MOSFET principle relies on the large band gap of diamond. Generally, wide band gap materials are used because of their ability to sustain high breakdown field which permits to achieve devices having higher blocking voltage than Si. In the deep depletion FET concept, we propose to use the large band gap of diamond in another manner. The large band gap of diamond induces an infinitely long time for the generation of minority carrier. Also, when the deep depletion regime is achieved in diamond and at the opposite to Si, if no source of minority carrier is provided (drain or source in inversion MOSFET for example), the deep depletion regime is stable over time. Here, we demonstrate the interest of this property to fabricate a transistor in which the on-state is ensured thanks to a bulk channel conduction, boron doped diamond epilayer, and the off-state is ensured thanks to the thick depletion induced by the deep depletion regime. This report is dedicated to the description of the deep depletion concept and demonstration.

In a first part, the deep depletion concept will be detailed. Then, the sample fabrication and experimental details will be given. The electrical properties of diamond Metal Oxide Semiconductor Capacitors (MOSCAPs) will be analyzed in terms of deep depletion. The effectiveness of the space charge region modulation will be demonstrated. Finally, the transistor characteristics of two deep depletion diamond MOSFETs will be shown in order to illustrate the device concept.

Figure 1 describes the deep depletion concept. Figure 1a) shows a cross section of a deep depletion transistor. D and S are the drain and source electrodes having a circular and annular shape, respectively. G is the annular gate electrode composed of a stack of oxide and metal deposited on diamond surface. For sack of simplicity, we first consider that D and S are grounded and only the gate

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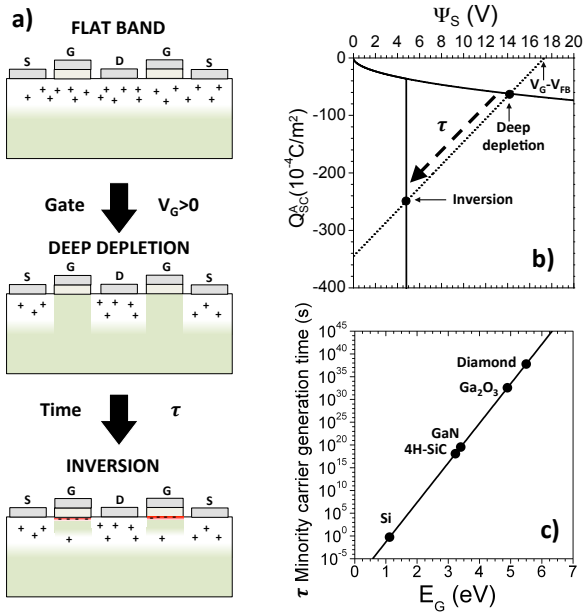

FIG. 1. a) Schematics represent the concept of deep depletion MOSFET for wide bandgap semiconductor. The three different regimes are drawn: flatband regime, deep depletion regime and inversion regime. b) Graphical solution of semiconductor charge per unit area as a function of gate voltage V_G for an ideal MOS structure with $N_A = 1.75 \times 10^{17} cm^{-3}$ acceptor doping level. The thickness and relative dielectric constant of Al_2O_3 are 40 nm and 9, respectively. The transition from the initial deep depletion regime to the inversion regime is characterized by the characteristic time constant τ. c) Minority carrier generation tine constant as function of material bandgap at room temperature using Si parameters for v_{th} and $N_{C,V}$. τ can be considered as infinite for diamond.

electrode can be biased with a voltage V_G. For V_G equals to the flat band voltage of the MOSCAP, no depletion of holes is expected below the gate electrode. The channel between the D and S is fully opened. A drain source voltage can create a channel current across the transistor. This is the on state of the deep depletion transistor. When a gate bias larger than the threshold voltage of the transistor is applied, the transistor is switching from the flat band regime to the depletion regime and then the deep depletion regime. The space charge region extends below the gate contact and would even reach the insulating substrate. The green areas of Fig. 1a) indicate the inversion area of the channel. This is the off state of the transistor. The electric charge below the gate can be quantified and even plot as function of the semiconductor surface potential Ψ_s (Fig. 1b)). The different regimes can be observed. The vertical line at around Ψ_s=4.8 eV represents the abrupt increase of the negative charges at the interface between the semiconductor and the oxide when the inversion regime is reached. Then, thanks to the method introduced by Vincent[9], we can graphically identify the transistor regime by plotting simultaneously the straight line arising from the Gauss theorem in the oxide and in the semiconductor respectively. One example is shown in Fig. 1b) for a high positive gate voltage. The two intercepts of this example correspond to two different regimes: deep depletion and strong inversion. A diamond MOSCAP will switch from the deep depletion regime to the strong inversion regime with a typical time constant τ:

$$\tau = 2 \times \frac{1}{v_{th}\sigma_e N_v} e^{\frac{E_c - E_v}{2k_b T}} \approx 10^{37} \text{ (sec)} \approx 10^{30} \text{ (years)} \quad (1)$$

with v_{th} the mean thermal velocity of carriers, N_v the equivalent density of states of valence band, σ_e is the capture cross-section of a defects in midgap with typical magnitude of 10^{-16} (cm^{-2}). E_c and E_v are the conduction and valence band energy respectively.

This time constant characterizes the time needed for electron (here minority carrier) to be generated from the valence band to the conduction band and so, establish the inversion regime. An evaluation using Si parameters for v_{th} and N_v, is shown in Fig. 1c) as a straight line. As observed, in the case of Si this time constant is of the order of one second meaning that the deep depletion regime is not a stable state in silicon material. Silicon can not be used to fabricate deep depletion transistor. At the opposite, the time constant of larger bandgap like diamond is so large, 10^{37} s at room temperature, that it can be considered as a stable state. In other words, Si MOSCAP switches from deep depletion to inversion in about one second and so, partially open the channel of the transistor degrading the off state of the transistor. At the opposite, diamond MOSCAP stays fully deeply depleted and so ensure the off state of the transistor. This particular property of wide bandgap material opens the route for the fabrication of high voltage high temperature devices. The possibility to use the deep depletion regime in MOSFET can be strongly beneficial in the design of the transistor since thick layer can be depleted with this concept. In order to demonstrate the validity of our concept, we fabricate and analyse diamond MOSCAP and transistors.

For the purpose of investigate the gate control diamond, the O-diamond MOSCAPs were fabricated using the lateral structure[10], as shown in Fig. 2a). Monocristalline diamond layer with 500 nm thick and 5×10^{16} cm^{-3} boron doped is homoepitaxially grown using a microwave plasma assisted chemical vapor deposition (MPCVD) NIRIM type reactor[11] on a 4 × 4 mm^2 Ib high pressure high temperature (HPHT) (001) diamond substrate. Oxygen termination of the semiconducting diamond top layer was done thank to a deep UV ozone treatment[12]. The ohmic contacts and gate contacts were defined by laser lithography (Heidelberg DWL66FS) and electron beam (e-beam) evaporation of Ti/Pt/Au (30/50/40 nm) followed by standard lift-off technique. 40 nm of Al_2O_3 were deposited by Atomic Layer Deposition (ALD) on the whole sample surface at 380°C using a Savannah 100 deposition system from Cambridge Nan-

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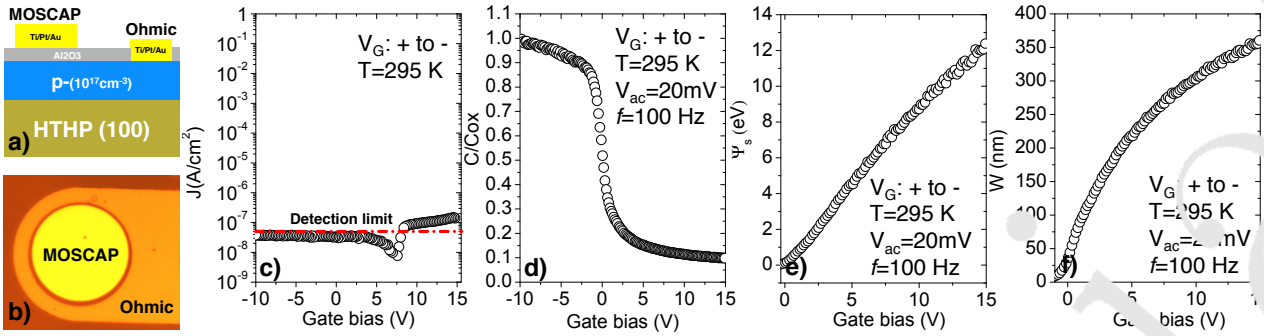

FIG. 2. a) Cross-section structure of the lateral O-diamond MOSCAP. b) Optical top view structure of the fabricated O-diamond MOSCAP. c) I(V) characteristics of the O-diamond MOSCAP for $+15V \leq V_G \leq -10V$ indicates the negligible leakage current. d) C(V) characteristic of the O-diamond MOSCAP indicates the complete electrostatic gate control diamond into accumulation, flatband, depletion and deep deletion regime. e) Semiconductor surface potential variation with gate bias for the gate bias from flatband voltage to deep depletion regime. f) the variation of semiconductor space charge region versus gate bias.

oTech. The precursor was Trimethylaluminium (TMA), and water as oxidant. The pulse and exposure duration were 15 ms and 30 s, respectively, with typical base pressure of 1.3×10^{-1}Torr. After the gate contact deposition, sample is annealed at 500°C in vacuum condition during 30 mins. Optical top view structure of MOSCAP is shown in Fig. 2b).

For MOSCAPs measurements, I(V) was measured by Keithley 2611 source-ammeter. Solartron Modulab with *ac* voltage $V_{ac} = 20mV$ was employed to measure C(V) and capacitance-frequency C(f).

For the purpose of proof-of-concept two deep depletion diamond transistors name GD1 and GD2 have been fabricated. The MOSFETs structure is identical to the structure presented in Fig. 1a). On sample GD1, a 20nm Al_2O_3 was deposited at 380°C onto the top of diamond epilayer (2×10^{17} cm^{-3} boron doped and 230 nm thick). On sample GD2, we deposited 40 nm Al_2O_3 at 380°C onto the top of diamond epilayer (5×10^{16} cm^{-3} boron doped and 500 nm thick). Typical thermal annealing is employed for ohmic contacts[13] of MOSCAPs and MOSFETs. For MOSFETs measurement, a two channel Keithley 2636 Source Meter Unit was used.

Figure 2c) represents the I(V) characteristic of the O-diamond MOSCAP. In this sample, leakage current are almost under detection limit for the bias range from -10V to +15V. The C(V) characteristic of O-diamond MOSCAP that were normalized to oxide capacitance C_{ox} is shown in Fig.2d). A complete p-type semiconductor MOSCAP operation (accumulation, flatband, depletion, deep depletion) is obtained. In this case, C_{ox} is estimated using $C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox}}$ where ε_0 vacuum permittivity, $\varepsilon_{ox} = 9$ is the oxide dielectric constant and t_{ox} is the oxide thickness. Prior to perform C(V) measurements, the a.c frequency is pre-determined by using C(f) measurements to eliminate the artifacts interfere C(V) measurements[14].

The ideal I(V) and C(V) characteristic of this sample is obtained thanks to the improvements of oxide and oxide/diamond interface. The details of new process improved oxide and oxide/diamond interface can be found in[15].

As mentioned above, the goal of this work is to demonstrate the deep depletion concept for boron doped diamond MOSFET. Therefore, the central role of the MOSCAP test devices is to examine the efficiency of gate control diamond semiconductor specialized on deep depletion regime.

As it is well-known, for depletion and deep depletion regime, semiconductor SCR is proportional to the square root of surface potential Ψ_s[9]. Consequently, the semiconductor capacitance C_{sc} and semiconductor surface potential can be evaluated from C(V) measurements[14,15]:

$$\Psi_s\left(V_G\right) = \frac{q^2 N_A \varepsilon_o \varepsilon_s \left(\frac{C_{ox}}{C_m} - 1\right)^2}{2C_{ox}^2} \tag{2}$$

The $\Psi_s - V_G$ relationship in Fig. 2e demonstrates the efficiency of gate control diamond semiconductor in deep depletion regime. Minimum capacitance $C_{\min}$ that generally observed in Si/SiO_2 MOSCAPs when Ψ_s reaches the inversion condition ($\Psi_s > 2\Psi_b$)[16] is not observed in diamond MOSCAPs. As illustrated in Fig. 1, this is the special characteristic of wide bandgap semiconductor due to the infinite minority carrier generation time constant.

From $\Psi_s - V_G$ relationship, the SCR width (W) versus V_G can be calculated by:

$$W = \sqrt{\frac{2\varepsilon_{sc}\varepsilon_0 \Psi_s}{qN_A}} \tag{3}$$

Figure 2f) represents the SCR width of boron doped O-diamond versus V_G. In the current configuration, 360 nm thick of diamond can be modulated. This analysis is critical to realize the deep depletion diamond MOSFET.

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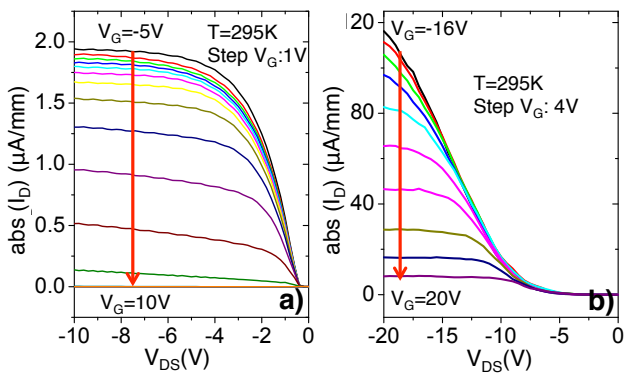

FIG. 3. Transistor characteristics measured by sweeping V_{DS} at different fixed V_{GS}.a) transistor characteristics of sample GD1; b) transistor characteristics of sample GD2.

The proof of deep depletion diamond MOSFETs concept is demonstrated in Fig 3. We introduce here the transistor characteristic of two transistors. The transistor characteristic is measured by sweeping the source to drain voltage (V_{DS}) at different gate bias, ranging from negative to positive. As shown in Fig 3, current between source and drain is clearly controlled by the potential at gate electrode. The devices clearly exhibit transistor characteristics with ON-state and OFF-state. For both cases, gate leakage currents are under the apparatus detection limit (data not shown) demonstrated that the transistors are controlled electrostatically by the potential at metal gate.

As demonstrated, the deep depletion concept is working well for different epilayer thicknesses, doping concentrations, different oxide thicknesses and also enlarge for different structures. This demonstration opens the concept of the vertical deep depletion MOSFET working like a Junction FET (JFET)[17] without the need of the n-type layer.

In summary, we demonstrated in this work the deep depletion concept which is unique of wide bandgap semiconductor. We fabricated O-terminated diamond MOSCAPs to investigate the effectiveness of gate control diamond semiconductor, specialized on deep depletion regime. We demonstrated the first ever a boron doped diamond MOSFET working by the deep depletion concept. This work opens the new perspectives to fully exploit the potential of diamond for MOSFET applications.

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Comprehensive electrical analysis of metal/Al_2O_3/O-terminated diamond capacitance

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Metal oxide semiconductor capacitors were fabricated using $p-$type oxygen-terminated (001) diamond and Al_2O_3 deposited by atomic layer deposition at two different temperatures 250°C and 380°C. Current voltage I(V), capacitance voltage C(V) and capacitance frequency C(f) measurements were performed and analyzed for frequencies ranging from 1 Hz to 1 MHz and temperatures from 160 K to 360 K. A complete model for the MOSCAPs electrostatics, leakage current mechanisms through the oxide to the semiconductor and small *a.c.* signal equivalent circuit of the device is proposed and discussed. Interface states densities are then evaluated in the range of $10^{12} eV^{-1}.cm^{-2}$. The strong Fermi level pinning is demonstrated to be induced by the combined effects of the leakage current through the oxide and the presence of diamond/oxide interface states.

I. INTRODUCTION

Diamond has been widely recognized as an ideal semiconductor for power devices[1,2] due to its superior physical properties. Recent progresses on diamond substrate, homoepitaxial growth, doping control and fabrication processing permit to consider the diamond power devices, e.g. Metal Oxide Semiconductor Field Effect Transistors (MOSFET). Most of the diamond MOSFETs[3-5] reported in the literature were realized thanks to the two dimensional hole gas (2DHG) at the hydrogen terminated diamond (H-diamond) surface due to surface doping concept[6]. Performances of H-diamond MOSFETs are promising[4] and optimizations of the structures are still under investigations[5,7,8]. Recently, the first MOSFET transistor working in inversion regime has been reported[9]. In order to obtain such carrier inversion, $n-$type oxygen-terminated (O-terminated) (111) diamond epilayer has been used as substrate material in order to create a $p-$type channel MOSFET. These two MOSFETs architectures are opening the route for the fabrication of the next generation of diamond based MOSFETs for power electronics. However, a deep understanding of the oxide and interface properties of the gate transistor is still missing. In this work, we report an exhaustive analysis of metal oxide semiconductor capacitor (MOSCAP) fabricated on O-terminated diamond.

In order to examine the gate control boron doped diamond, Chicot et al.[9] introduced the O-diamond/Al_2O_3 MOSCAPs test device. Strong leakage currents[10] and capacitance frequency dependence[11] were observed through the O-diamond MOSCAPs with Al_2O_3 deposited by ALD at 100°C. Kovi et al.[12] employed an identical structure using Al_2O_3 deposited by ALD at 250°C and reported similar electrical characteristics. Marechal et al.[13] employed the XPS measurements and determined the type of band alignment at O-diamond/Al_2O_3 interface with Al_2O_3 deposited by ALD at 250°C. However, in all mentioned reports, a complete understanding on the electrical characteristics of boron doped O-diamond/Al_2O_3 MOSCAPs is still lacking.

This work is devoted to investigate the diamond/Al_2O_3 interface and the origin of gate leakage current and capacitance-frequency dependence for O-diamond MOSCAP. In the first section, we briefly introduce the fabrication processes and the general electrical characteristic of the O-diamond MOSCAPs to illustrate the main issues. In the second section, we address the electrostatic properties of the O-diamond MOSCAPs, we introduce an approach to reliably perform the C(V) measurements and a method to quantify the semiconductor surface potential versus gate bias ($\Psi_S(V_G)$). Electric charges properties such as semiconductor doping concentration, oxide charges and interface states charges are then quantified from C(V) measurements. The electrostatic band diagrams are built by taking into account the charge components of the MOSCAP test device. Electrostatics simulations are compared with experimental results $\Psi_S(V_G)$. In the third section, we propose a model for the leakage current mechanism under negative bias thanks to the electrostatics band diagram. From leakage current mechanism, we build the physical equivalent circuit linearizing the small signal measurements. Approximated equivalent circuit based on different limiting processes is discussed. Current limiting process is identified thanks to different approaches. From the approximated equivalent

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circuit, the conductance method is adapted to our specific MOSCAPs and applied to quantify interface states density D_{it}. The impedance/admittance frequency dependence of the MOSCAP test device is empirically simulated by using the proposed equivalent circuit with all parameters extracted from experimental analysis. Finally, the paper is summarized.

II. MOSCAP FABRICATION AND TYPICAL ELECTRICAL CHARACTERISTICS

This section is dedicated to the description of the MOSCAPs fabrication process. Then, the typical I(V), C(V) and C(f) measurements done on these MOSCAPs will be illustrated and discussed.

A. Experimental details

The test devices composed of a stack of a heavily (p+ layer) and a lightly (p− layer) boron-doped homoepitaxial mono-crystalline diamond layer grown by using a microwave plasma assisted chemical vapor deposition (MPCVD) NIRIM type reactor on a 3 × 3 mm^2 Ib high pressure high temperature (HPHT) (001) diamond substrate. The cross-section structure is shown in Fig. 1 a). The optical plan view structure of one fabricated test device is shown in Fig 1b. The moderately boron-doped diamond layer ($N_A \simeq 3 \times 10^{17}$ cm^{-3}) is in contact with the gate oxide. The heavily boron doped ($N_A \simeq 5 \times 10^{20}$ cm^{-3}) metallic diamond p+ layer acts as a low resistive ohmic contact electrode in order to reduce the series resistance. Vacuum ultraviolet (VUV) ozone treatment resulted in the Oxygen termination of the diamond surface[14]. The Al_2O_3 gate oxide was deposited by atomic layer deposition (ALD) on the whole sample surface using a Savannah 100 deposition system from Cambridge NanoTech. The precursor was Trimethylaluminium (TMA), and water was used as the oxidant. The pulse and exposure duration were 15 ms and 30 s, respectively, with typical base pressure of 1.3× 10^{-1}Torr. The ohmic contacts and gate contacts were defined by laser lithography (Heidelberg DWL66FS) and electron beam (ebeam) evaporation of Ti/Pt/Au (30/50/40 nm) followed by standard lift-off technique. The ohmic contact was deposited directly on p$^+$ layer prior to Al_2O_3 deposition. This structure offers the advantage of having both MIMCAPs and MOSCAPs on the same sample, as shown in Fig. 1a). The details of two representative samples are presented in table I. These two samples are chosen as their electrical characteristics are mostly similar in term of leakage current density, capacitance-voltage and capacitance-frequency behaviors. The only difference is the shift of flatband voltage due to charge in the gate oxide, as it will be discussed in the following sections.

The DC Current-Voltage I(V) characteristic was measured by Keithley 2611 source-ammeter. Small-signal measurements (C(V), C(f), impedance, admittance) were performed with a constant a.c voltage of V_{ac} = 20 mV by Solartron Modulab impedance analyzer. Capacitance characteristics that will be introduced in the following section represent the measured capacitance of the equipment which is $C_m = \frac{1}{\pi f Z}$. Where Z is the modulus of the measured impedance. To perform conductance method, the parallel capacitance-conductance circuit ($C_p - R_p$) can be evaluated by using the real part and imaginary part of the measured impedance. Electrostatics simulation was performed using Nextnano^3 software. The band alignment for electrostatics simulation is employed from the XPS measurement introduced by Marechal et al.[13]

Sample	t_{p-} (nm)	t_{p+} (nm)	t_{ox} (nm)	O-termination	T_{dep} of ALD (°C)	$T_{annealing}$ (°C)
#1	600	300	20	VUV	250	NA
#2	300	300	20	VUV	380	500

TABLE I. Sample structures details: thickness of moderately doped layer t_{p-}, heavily doped layer t_{p+}, oxide layer deposited by ALD t_{ox}, treatment for oxygen termination (VUV ozone treatment is defined as VUV), ALD deposition temperature T_{dep} and annealing temperature $T_{annealing}$.

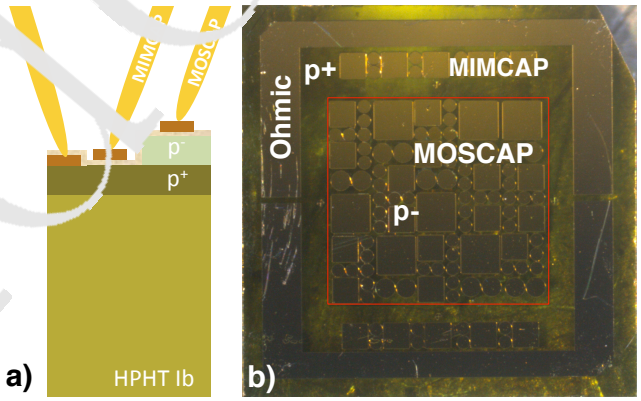

FIG. 1. Structure of the test device that include Ohmic contact, MIMCAPs and MOSCAP a) Cross-section; b) Top view.

B. Typical electrical characteristics

Typical electrical characteristics of O-diamond MOSCAPs can be summarized in Fig. 2. These results are measured from MOSC7 test device on sample #2 and in agreement with O-diamond MOSCAPs that have been previously fabricated and reported by our group[11,13] and the results published in literature[12].

Figure 2a) represents the I(V) characteristics. Under negative gate bias, leakage currents are systematically observed. Under positive bias, leakage currents are

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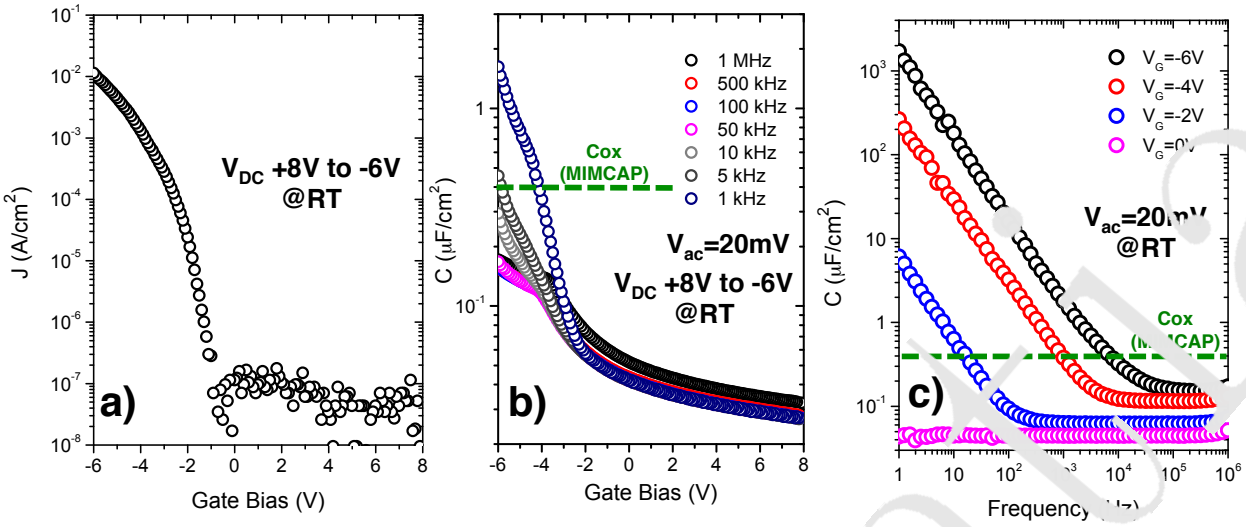

FIG. 2. Typical electrical characteristics of O-diamond MOSCAPs. Data shown here is measured from MOSC7, sample #2 (surface area A=1.77×10^{-4} cm^2): a) I(V) characteristics; b) C(V) characteristics measured at different frequency, ranging from 1 kHz to 1 MHz; d) C(f) characteristics measured by fixing gate bias at V$_G$=0V, -2V, -4V and -6V and sweeping frequency from 1 Hz to 1 MHz.

randomly observed among several test devices (for the current MOSCAP, leakage current under positive bias are under the apparatus detection limit). In the following sections, we will elaborate the origin of leakage currents and capacitance-frequency dependence for the O-diamond MOSCAPs under negative bias. The origin of leakage currents and capacitance frequency dependence for O-diamond MOSCAPs under positive bias will be discussed in another work.

Figure 2b) represents the C(V) characteristic at different frequencies, ranging from 1 kHz to 1 MHz on the same MOSCAP test device and the same bias range with I(V) measurement. A strong capacitance frequency dependence is observed when the strong negative gate bias ($-4\ V \leq V_G \leq -6\ V$) is applied. For the high positive bias range, the capacitance-frequency dependence is not observed in this MOSCAP test device.

The capacitance-frequency dependence under negative bias can be further seen by C(f) measurements, as shown in Fig. 2c). From the $C(f)$ curves, three different regimes can be distinguished. *i) High frequency regime* (between 500 kHz and 1 MHz): There is a minor effect from series resistance which induces a slightly capacitance increase versus f. However, in our pseudo-vertical MOSCAPs, series resistance contribution is almost negligible. *ii) Low frequency regime* (from 1 Hz to about 40 kHz for $V_G = -6\ V$; from 1 Hz to 4 kHz at $V_G = -4\ V$; from 1 Hz to 200 Hz at $V_G = -2\ V$; and almost negligible in the whole frequency range for $V_G = 0\ V$): the measured capacitance is strongly frequency dependent. Capacitance decreases with a slope of 20 dB/dec. Previous reports on O-diamond MOSCAPs[11,12] showed that the capacitance frequency dependence of the "low frequency range" is huge. In Kovi et al.[12], the "low frequency range" is even observed for the frequencies up to few MHz. *iii) Middle frequency regime* (the regime between "high frequency" and "low frequency"): the measured capacitance is constant versus frequency. This frequency window is too low to be assigned to a series resistance effect and too high to be related to an interface states contribution. The C(V) measurement in this frequency window is considered as the proper C(V) characteristic of the MOSCAP. In another word, MOSCAP test device is in the ideal MOSCAP configuration i.e. oxide capacitor C$_{ox}$ and semiconductor capacitor C$_{sc}$ are in series. In this configuration, the measured capacitor of the MOSCAP writes: $C_{MOS} = \frac{C_{ox}C_{sc}}{C_{ox}+C_{sc}}$.

In the following section, we will employ this proper C(V) measurement to evaluate the key informations of our O-diamond MOSCAP test devices.

III. ELECTROSTATICS: ELECTRIC CHARGES, ELECTRIC FIELD AND POTENTIAL DISTRIBUTION

This section is dedicated to quantify different electric charge components and to establish the electrostatic band diagram of the O-diamond MOSCAP.

A. Proper C(V) measurement

As shown in the typical C(f) characteristics (Fig. 2c), capacitance measurement is affected by series resistance at high frequency regime and by other artifacts at low frequency regime. In our experiment, prior to perform

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C(V) measurements, the C(f) measurements have been systematically employed to determine the "middle frequency" window which corresponds to each MOSCAP.

The open red circle curve in Fig. 3 represents the C(V) characteristics of MOS 12−sample #1 at $f = 100$ kHz, which is in the proper frequency window of this MOSCAP device. From the proper C(V) curve, notable behaviors can be noticed as:

i) Under negative bias, for bias lower than the flatband voltage of the MOSCAP, the accumulation regime is expected corresponding to ($C_{MOS} = C_{ox}$). In our case, the measured capacitance is much lower than the oxide capacitance $C_m << C_{ox}$ even for $V_G = -8\ V$. Measured capacitance can be normalized to the oxide capacitance $C_{ox} = 0.4\mu F.cm^{-2}$, measured from MIMCAP test devices on the same sample. A maximum measured capacitance of $C_m = 0.135\mu F.cm^{-2}$ at $V_G = -8\ V$ is observed, corresponding to $C_m \simeq 0.35C_{ox}$. The systematic measurements demonstrated that this behavior is general for all measurable MOSCAPs on the same substrate[15].

ii) The measured capacitance for positive bias does not show the saturation of minimum capacitance C_{min}. Up to $V_G = +8\ V$, the measured capacitance monotonously decreases versus V_G corresponding to the deep depletion regime.

iii) By sweeping the bias voltage from $+8\ V$ to $-8\ V$ and then from $-8\ V$ to $+8\ V$, C(V) characteristics are almost identical. No sign of mobile oxide charges in this MOSCAPs test devices can be observed[15].

In summary, from the proper C(V) measurement, three different charge components in the O-diamond MOSCAP can be envisaged: semiconductor charges, oxide charges and interface charges.

B. Semiconductor charges

From proper C(V) measurement, the semiconductor doping concentration is extracted using the Schottky-Mott plot. The open black circle curve in Fig. 3 represents the Schottky-Mott plot (reciprocal square capacitance versus gate bias plot $\frac{1}{C^2}$ vs. V_G). The term $\frac{1}{C_m^2} - \frac{1}{C_{ox}^2}$ is used to eliminate the effect from oxide capacitance[16]. The $\frac{1}{C^2}(V_G)$ curve exhibits an almost perfect straight line for the gate voltage ranging from V_G=−6 V to V_G=+8 V. From the slope of the curve, the doping concentration of the B-doped semiconducting diamond layer can be extracted by using the equation:

$$N_A = \frac{-2}{\varepsilon\varepsilon_0 A^2}\frac{1}{dC^2/dV} \quad (1)$$

with $\varepsilon = 5.7$ the diamond dielectric constant, ε_o the vacuum permittivity and A the area of the diode. A doping concentration of $N_A = 3 \times 10^{17}\ cm^{-3}$ is extracted from the $\frac{1}{C_m^2} - \frac{1}{C_{ox}^2}$ versus V_G curve. This value is almost identical with the targeted value expected from the diamond growth parameters. Systematic

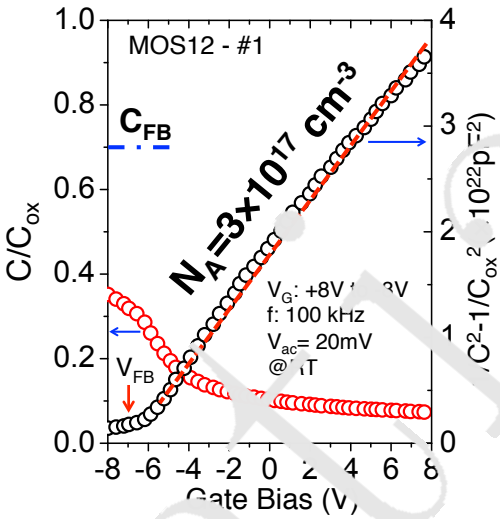

FIG. 3. Proper C(V) measurement indicates that diamond are in depletion regime even for $V_G = -8V$. Doping concentration of diamond epilayer is extracted from $\frac{1}{C^2}(V_G)$ curve (MOS12 - sample #1).

measurements demonstrated the homogeneous and well-controlled dopant incorporation in B-doped diamond epilayer

C. Oxide charges

One notable feature that can be seen from the C(V) curve and $\frac{1}{C_m^2} - \frac{1}{C_{ox}^2}$ versus V_G curve is the shift of the curves toward negative bias, compared to the ideal case. In fact, this shift is possibly induced by the interface charges, the oxide charges and the work function difference between metal and semiconductor. However, since our C(V) measurements were performed at 100 kHz, we can exclude the a.c contribution from the interface charges. As, the slope of $\frac{1}{C_m^2} - \frac{1}{C_{ox}^2}$ versus V_G in the range of examination has reliably reflected diamond doping concentration, the DC contribution of interface states is deduced to be negligible also for this gate voltage range. The experimental flatband voltage V_{FB}, corresponding to the voltage at which the extrapolated $\frac{1}{C_m^2} - \frac{1}{C_{ox}^2}$ straight line intercepts the horizontal axis, is equals to $-7.3\ V$. This value is larger than the theoretical one, i.e. $V_{FB} = \phi_M - \phi_{SC} = -2.6\ V$ where $\phi_M = 4.3\ eV$ is the work function of Ti metal and the semiconductor work function is $\phi_{SC} \simeq E_G + \chi_{sc} - E_F = -6.9\ eV$ with $\chi_{sc} = 1.7\ eV$ the electron affinity of O-diamond[17], E_G the diamond band gap and E_F the Fermi level in the neutral region of the B-doped diamond referenced from the valence band ($E_V = 0$). This experiment demonstrates that the measured flat band voltage includes a contribution of charges in the oxide Q_{ox}. By applying the equation[18]:

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$$Q_{ox} = \frac{C_{ox}\left(\phi_{MS} - V_{FB}\right)}{qAt_{ox}} \tag{2}$$

A net positive oxide charge density of $Q_{ox} = 6 \times 10^{18}\left(cm^{-3}\right)$ is deduced for sample #1. The shift of flatband voltage in sample #2 is about $-5.4\ V$ where the oxide charge is calculated as $Q_{ox} = 3.5 \times 10^{18}\left(cm^{-3}\right)$.

D. Fermi level pinning effect due to a strong interfaces states density

MOSCAP is the suitable device to examine the efficiency of gate controlled semiconductor structure. As discussed by Vincent et al.[19], semiconductor surface potential Ψ_s is the critical quantity for this evaluation. Ψ_s corresponds to the electrical potential variation between the neutral part of the semiconductor, where the Fermi level is flat, and the semiconductor surface, i.e. at the oxide interface. When $\Psi_s = 0$ eV, the semiconductor is in the flatband regime. Therefore, flatband regime is the demarcation between accumulation regime and depletion regime. In the flatband regime, the semiconductor charge $Q_{sc}\left(V_G = V_{FB}\right)$ and consequently the semiconductor capacitance $C_{sc}\left(V_G = V_{FB}\right)$ is a function of the intrinsic semiconductor Debye length as:

$$C_{sc}\left(V_G = V_{FB}\right) = \frac{\varepsilon_{sc}\varepsilon_0}{\lambda_p} \tag{3}$$

where λ_p is the semiconductor intrinsic Debye length, which writes $\lambda_p = \left(\frac{\varepsilon_{sc}\varepsilon_0 kT}{q^2 N_A}\right)^{1/2}$.

With N_A extracted from the previous section, the semiconductor flatband capacitance $C_{sc}\left(V_G = V_{FB}\right)$ can be evaluated. Subsequently, the flatband capacitance of the MOSCAP $C_{MOS}\left(V_G = V_{FB}\right)$ is evaluated as:

$$\frac{1}{C_{MOS}(V_G = V_{FB})} = \frac{1}{C_{ox}} + \frac{1}{C_{sc}(V_G = V_{FB})} \tag{4}$$

From these relationships, a MOSCAP flatband capacitance of $C_{MOS}\left(V_G = V_{FB}\right) = 0.27\ \mu F.cm^{-2}$ is evaluated for MOS12 - sample #1. With the semiconductor doping concentration being homogeneous[15], this value is typical of the MOSCAP measured on the whole sample. As shown in Fig. 3, the maximum measured capacitance of O-diamond MOSCAP at $V_G = -8\ V$ ($C_m = 0.135\ \mu F.cm^{-2}$) is lower than the flatband capacitance C_{FB}. Therefore, it can be concluded that the diamond MOSCAP is always in depletion regime even for high negative bias ($V_G = -8\ V$). In previous reports, Chicot et al.[10,11] and Kovi et al.[12] measured similar C(V) characteristics and deduced that their MOSCAP reached the accumulation regime. However, the present study shows that this assignment is erroneous and the misunderstanding is induced by the parasitic frequency dependence.

Since diamond is always in depletion regime, semiconductor Space Charge Region (SCR) is proportional to the square root of the surface potential Ψ_s[19] in the whole voltage range ($+8\ V$ to $-8\ V$). Therefore, the semiconductor capacitance is also proportional to the square root of the semiconductor surface potential as[20]:

$$C_s = \sqrt{\frac{qN_A\varepsilon_o\varepsilon_s}{2\Psi_s}} \tag{5}$$

As the measured capacitance C_m and the oxide capacitance C_{ox} are determined, the semiconductor capacitance C_{sc} and the semiconductor surface potential Ψ_s can be calculated. By performing a simple mathematical derivation of equations 4 and 5, the surface potential corresponding to a specific gate bias voltage can be written:

$$\Psi_s\left(V_G\right) = \frac{q\ N_A\varepsilon_o\varepsilon_s\left(\frac{C_{ox}}{C_m} - 1\right)^2}{2C_{ox}^2} \tag{6}$$

In principle, by performing this calculation at different gate bias, we can establish the relationship between semiconductor surface potential versus gate bias voltage ($\Psi_s - V_G$), and so evaluate the efficiency of gate control semiconductor. For negative gate bias (V_G : down to -8V), Ψ_s stays positive showing that the Fermi Level Pinning Effect (FLPE)[21] is observed. The semiconductor regime at the interface approaches but never reaches the flatband voltage. This FLPE can be illustrated by the $\frac{1}{C_m^2} - \frac{1}{C_{ox}^2}$ values, which are saturating and tending to a positive value for gate bias lower than -6V.

The strong FLPE observed here is assumed to be due to the presence of interface states in the semiconductor forbidden gap[20,22]. An evaluation of their density can be done thanks to the quantitative analysis of the capacitance stretching due to FLPE. This is the main idea of the high frequency-capacitance method developed by Terman[22]. With $\Psi_s - V_G$ evaluated from eq.6, the interface states capacitance C_{it} versus Ψ_s is calculated by the high frequency capacitance method[20,22]:

$$C_{it}\left(\Psi_s\right) = C_{ox}\left[\left(\frac{d\Psi_s}{dV_G}\right)^{-1} - 1\right] - C_s\left(\Psi_s\right) \tag{7}$$

Subsequently, the interface states density D_{it} can be evaluated by[20]:

$$D_{it}\left(\Psi_s\right) = \frac{C_{it}\left(\Psi_s\right)}{q} \tag{8}$$

An interface states density of less than 10^{12} ($\mathrm{eV}^{-1}.\mathrm{cm}^{-2}$) is found in the midgap region and an abrupt increase up to 4×10^{13} ($\mathrm{eV}^{-1}.\mathrm{cm}^{-2}$) for the interface states near the valence band edge ($\mathrm{E}_t - E_v \approx 0.6$ eV). We will see later that this method is not adapted to our case and overestimates the D_{it} values. Indeed, the leakage current through the oxide is too high to consider the interface under equilibrium.

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E. Electrostatics simulation

We performed the electrostatics simulation by implementing the semiconductor charges qN_A extracted from the $\frac{1}{C^2} - V_G$ curve, oxide charges Q_{ox} extracted from the shift of V_{FB} and interface charges $\sigma_{it}(V_G)$ extracted from Terman method. Interface states charge is evaluated by integrating the interface states density over the energy band gap.

The electrostatics band diagrams of O-diamond MOSCAP for a gate bias of -5V is shown in Fig. 4 a). One remarkable issue from electrostatics simulation, which is not obvious from C-V measurement is the potential distribution within the oxide. This electrostatic band diagram is essential to identify the origin of leakage currents and capacitance-frequency dependence under negative bias.

IV. GATE OXIDE LEAKAGE CURRENT MECHANISM AND EQUIVALENT SMALL SIGNAL CIRCUIT

This section is dedicated to the analysis of the leakage current from metal to semiconductor and the corresponding equivalent small signal circuit.

A. Leakage current mechanism

In an ideal MOSCAP, the gate oxide prevents carrier transport between the gate metal and the semiconductor. Electrostatics gate control of carrier population at the oxide/semiconductor interface is crucial for semiconductor devices. However, in real situations, leakage currents are usually observed and perturb the carrier control.

In order to understand the origin of leakage currents, the source of transporting carriers must be determined. For a p-type MOSCAP under negative bias regime, currents are initiated from either the accumulated semiconductor majority carriers or gate metal carriers reservoir[23]. For O-diamond MOSCAPs, as evidenced from $C-V-f$ analysis and electrostatic band diagram, we concluded that leakage current under negative bias is initiated from carriers reservoir of metal gate and not from accumulated hole of diamond semiconductor. This conclusion is based on the fact that MPE preserved diamond in depletion regime, even at high negative bias (e.g $V_G = -8$ V, MOS 12 - sample #1). No majority carrier (hole) are able to accumulate at the diamond-oxide interface. The transport due to accumulated majority carriers is therefore prohibited.

The next question to be addressed is, how do these carriers circulate in the MOSCAP system? Thanks to Nextnano electrostatics band diagram, we proposed a 5-steps current mechanism, as shown in Fig. 4a). In step 1, carriers from gate metal are tunneling into the oxide trap states. Hopping between traps to traps through the oxide is taking place during step 2. In step 3, hopping carriers are captured by interface states. The charge transferring between interface states and valence band are taking place in step 4. Finally, these carriers drift through the diamond epilayer to the back gate contact (p^+) and complete the transfer process.

Potentially, the flow at each step may includes different processes in parallel. In principle, the process with highest rate (slowest time constant) dominates the flow at that step. On another hand, in order to complete a circulation, different steps in series could be involved. The step with the slowest rate (longest time constant) is the limiting process.

In the proposed current mechanism (Fig. 4a), interface states play a central role with a special interest. They are able to communicate with both the metal electrode and the semiconductor valence band. In principle, each charge transfer process is represented by its characteristic time constant τ. For the sake of simplicity and without losing the generality, we will firstly consider interface states as a single level state at energy $E_{it} - E_v$ and density N_{it}. In the following sections, we will discuss further the charge transfer between interface states with metal and semiconductor band edge.

1. Charge transfer between metal and interface states

The charge transfer between gate metal and interface states in a MOSCAP system was addressed by Dahlke and Lee[23]. The complementary theory was then developed by Freeman and Dahlke[24]. In their theory, interface states are modeled as a potential well and communicate with the gate metal by direct tunneling. The charge transfer is considered as an overlapping process of two wave functions. Kar and Dahlke experimentally studied the metal injection into interface states with a non-degenerate Si substrate and a moderate oxide thickness (20 − 40 Å) MOS capacitor system[25]. A notable possible consequence of carriers injection from gate metal to interface states is that these carriers are possibly accommodating at interface states and therefore modulating Schottky barriers height at Metal-Semiconductor contact[26–28].

In our case, the oxide is too thick to observe direct tunneling. Therefore, carriers injection from metal to interface states is suggested to be a process of two consecutive steps: the carriers tunneling from gate metal to oxide trap states (represented by tunneling time constant τ_{tun}) and then carrier hopping between trap sites happens in the oxide (represented by hopping time constant τ_{hop}). The two consecutive processes must happen in series and so the tunneling time constant τ_T (from metal/oxide to oxide/semiconductor interface) writes:

$$\tau_T = \tau_{tun} + \tau_{hop} \tag{9}$$

a. Tunneling from metal to oxide trap states As shown in Fig. 4 a), electrons from gate metal are suggested to initiate the flow by tunneling into Al_2O_3 gate

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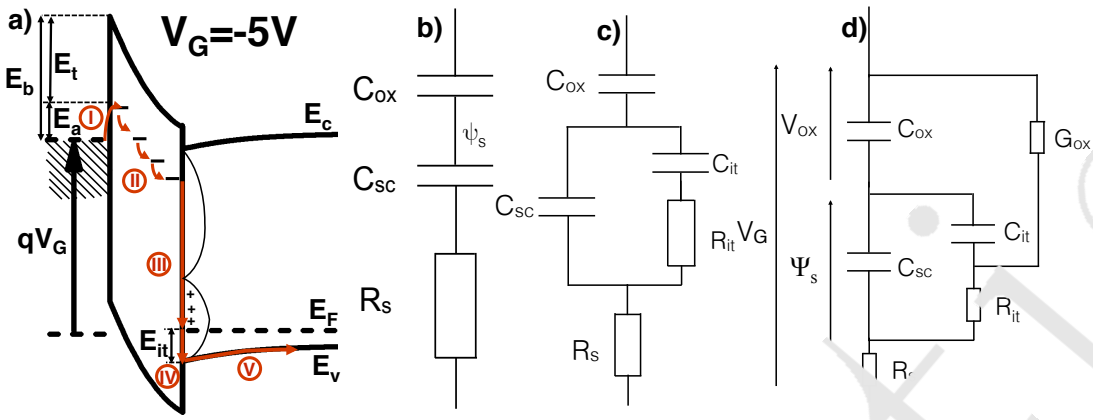

FIG. 4. (a) Finite element calculation of MOSCAP band diagram under negative gate bias $V_G = -5V$. The arrows illustrate the proposed current path mechanism including five steps: I. Electron tunneling from metal gate electrode to oxide gate, II. Hopping from traps to traps in the oxide, III. Recombination to surface trap states, IV. Electron from surface states emit to valence band or hole from valence band captured to interface states, V. Carriers drift in diamond epilayer to the back gate contact. (b) Equivalent circuit of a MOSCAP without interface states and leakage current; (c) Equivalent circuit including interface states and a gate oxide without leakage current (d) Equivalent circuit where the injected carriers from metal to interface states and the charges transfer between interface states and valence band are taken into account.

oxide layer. Even if there are many possible processes for a carrier from gate metal to be injected into the gate oxide[29], most of them are practically not possible in our case. It is either direct tunneling, thermionic emission (Schottky injection) or tunneling into many trap states in the oxide. Considering the oxide thicknesses of $10-40$ nm that were systematically used for O-diamond MOS capacitors, direct tunneling by overlapping wave functions (theoretically less than 1 nm)[23] is not possible. Thermionic emission is a thermal activation process where carriers from the gate metal have to reach a sufficient energy to jump over the metal oxide barrier height and being injected into the oxide layer. Regarding an approximate 3 eV barrier height between Ti and Al_2O_3, this process is not realistic. Also, the tunneling from the gate metal into oxide trap states[30] of the gate oxide is the most realistic process.

Tunneling current from the gate metal to oxide trap states can be approximately described by[31]:

$$I = N_t q \nu_{tun} \tag{10}$$

where N_t is the density of nearest traps contributing to the conduction and ν_{tun} is the tunneling transmission rate. The tunneling transmission rate is:

$$\nu_{tun} = \frac{1}{\tau_{tun}} = v_o f_T T_{WKB} \tag{11}$$

with $v_0 \sim 10^{13}$ Hz the attempt frequency which represents the rate of escape of a particle from a confining structure by quantum tunneling through its outer barrier. f_T is the Fermi-Dirac function representing the occupancy probability of a trap state in the oxide. It can be expressed by:

$$f_T = 1/\left(1 + \exp\left(\frac{E_a + Fx}{kT}\right)\right) \tag{12}$$

where $E_a = E_b - E_t$ is the electron barrier between metal electrode and trap states, E_b is the electron barrier between metal electrode and oxide conduction band, E_t is the energy of the traps in the oxide, F is electric field in the oxide and x is the distance from the metal/oxide to the trap where the electron is tunneling (Fig. 4a)). T_{WKB} is the Wentzel-Kramers-Brillouin (WKB) transmission coefficient and can be written as[32]:

$$T_{WKB} = \exp\left(-\frac{4}{3\hbar qF}\sqrt{2m^*}\left((E_t + qFx)^{3/2} - E_t^{3/2}\right)\right) \tag{13}$$

with $\hbar$ is the reduced Planck constant and m^* the effective mass of electron in the oxide[31].

b. Hopping in the oxide Carriers transport in the oxide could be the sum of multiple parallel mechanisms[29,31]. One of two main mechanisms is the thermal activation from deep energy traps to oxide conduction band, which is generally called Poole-Frenkel emission. The second one is tunneling from traps to traps, also called hopping. In order to determine the dominant process, transfer rates of each process are necessary to be evaluated. The Poole-Frenkel emission rate is scaled versus T as $v_0 \exp\left(-\frac{E_c - E_t}{kT}\right)$ where E_t is the energy of the traps in the oxide band gap[31]. In the case of Al_2O_3 oxide deposited by ALD, trap states are usually ascribed to the non-stoichiometry of the oxide. From first principle simulation, the oxygen vacancy is found to be the electron trap level which is the nearest from the conduction band as $E_c - E_t = 1$ eV[33].

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The trap to trap tunneling rate is calculated as[31]

$$\nu_{hop} = \frac{1}{\tau_{hop}} = v_0 \exp\left(-\frac{2R}{\xi}\right) \tag{14}$$

with ξ the electron wave function localization length $\xi \simeq 0.3$ nm, R distance between trap sites[31]. Distance between trap sites could be obtained by fitting the DC non-linearity capacitance-voltage of MIMCAPs[34]. The distance between trap sites in our ALD Al_2O_3 is then estimated to be approximately 5 nm[15].

A rough evaluation shows that the tunneling rate from trap to trap is almost 150 times faster than Poole-Frenkel thermal activation rate from traps level to conduction band at room temperature[15]. In case that an oxide trap level is deeper from oxide conduction band, which will be found below, the injection rate in step I will be even slower. It is therefore possible to conclude that tunneling from trap to trap is the main transport mechanism in the oxide.

2. Carrier readjustment

In step III, carrier readjustment is taking place. The readjustment process is a transfer from the energy levels of the oxide traps to the quasi-Fermi level of semiconductor at semiconductor/oxide interface. As depicted in Fig. 4 a), interface traps include two main parts. Acceptor-like levels close to the conduction band and donor-like levels close to the valence band, defining a Charge Neutrality Level (CNL). If the quasi-Fermi level is below the CNL (as shown in Fig. 4 a) donor-like levels will be positively charged between the quasi-Fermi level and the CNL. The other interface states will be neutral. In this case, the time for carriers readjustment, trapped by interface states (step III), will be neglected because its thermalization process is very fast compared to other processes[35].

3. Charge transfer between interface states and semiconductor band edges

In step IV, the trapped electrons at interface states emit to the semiconductor valence band. We will firstly consider the single level interface states model with density N_{it} and energy $E_{it} - E_v$ from the valence band.

The serial charge transfers from gate electrode to interface states and from interface states to semiconductor valence band can be described by the differential equation[24]:

$$N_{it}\frac{df_t}{dt} = -U_{cp} + \frac{j}{q}. \tag{15}$$

where j is the current injected from metal gate to interface states. U_{cp} is the charge transfer rate of trapped carriers at interface states to semiconductor valence band and can be described by[?] :

$$U_{cp} = N_{it}\sigma_p\langle v_{th}\rangle\left(f p_s - f_p p_1\right) \tag{16}$$

with σ_p is the hole capture cross-section of the trap states, v_{th} is the carriers mean thermal velocity, f and f_p are the occupation probabilities of a trap state by an electron and hole, respectively[?] . $p_s = p_b \exp\left(\frac{e\Psi_s}{kT}\right)$ is the surface carriers density at thermal equilibrium with p_b the bulk carriers density. $p_1 = N_v \exp\left(\frac{E_v - E_{it}}{kT}\right)$ represents the carrier density that established at the trap states when the quasi-Fermi level equals the trap states level[24]. E_F is the quasi-Fermi level and N_v is the effective density of states of the valence band.

The current in and out interface states discussed above is then described by the interface states occupancy f_{ss}[24,25] which is:

$$f_{ss} = \left(\tau_R f_m + \tau_T f_s\right)/\left(\tau_R + \tau_T\right) \tag{17}$$

where f_s and f_m are the bulk semiconductor and metal occupancies respectively[24]. τ_R is the recombination time constant of majority carriers with interface states and to be calculated:

$$\tau_R = \frac{1}{\sigma_p v_{th} p_b}\exp(\Psi_s) \tag{18}$$

4. Drift in the diamond layer

The process of electron being emitted to the valence band is equivalent to the process of holes from the valence band to be captured by interface states. To replace the evacuated hole, a hole from the back side (p+ layer) will move to the diamond surface and be ready for a new capture event[36]. In the reverse direction, electrons are transferring to the back gate contact (p^+) and complete the circulation.

B. Equivalent circuit and approximation

1. Equivalent circuit

In order to model the measured impedance and admittance of a MOS capacitor, linearized equivalent circuit is a well-known concept. Lehovec and Sloboskoy[37] developed a comprehensive theory and derived a general equivalent circuit for the MOS capacitors. Nicollian and Golzberger[38] paid special attention to the conductance of interface states in "thick oxide MOS capacitor": The meaning of "thick oxide" is that the interface states are in equilibrium and close communication with the semiconductor band edges. They also developed a model to evaluate the equivalent conductance G_P/ω that consists

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only interface states density and its time constant from the parallel capacitance-conductance ($C_p - R_p$) circuit[38].

For the special case where interface states communicate with both gate metal and semiconductor band edges, Freeman and Dahlke[24] developed the theory as well as the corresponding equivalent circuits. Different possible limiting processes were also discussed. The approximated equivalent circuits corresponding to each limiting case were also proposed. Since then, there were different discussions about the possibilities and opportunities to employ gate tunneling into interface states to measure a wide range of interface states density[25,39,40]. Kar and Dahlke[25] performed the experiments on Si/SiO_2 MOSCAPs with moderate oxide thickness and a non-degenerate Si semiconductor to investigate interface states thanks to gate carriers injected to interface states.

In an ideal case, where only the unavoidable series resistance of the drift layer is involved, the equivalent circuit of MOSCAP can be represented by Fig. 4b). In case of single level interface states involved in thick oxide MOSCAP (without leakage current), the equivalent circuit is represented as in Fig. 4c).

In our O-diamond MOSCAPs, corresponding to the current mechanism suggested in Fig. 4a), we introduce an equivalent circuit as in Fig. 4d). Non-perfect gate oxide with gate leakage currents is modeled by an oxide conductance G_{ox} and an oxide capacitance C_{ox} in parallel. The flow of carriers from metal to semiconductor is injected to the mid point of the interface states recombination circuit, as proposed by Freeman et al.[24].
This general equivalent circuit can be further simplified by the approximations corresponding to the leakage current limiting process.

2. Approximation

The O-diamond MOSCAP equivalent circuit will be simplified to the approximated equivalent circuits depending on the limiting transport processes of the leakage current. We remind that the equivalent circuit in the general case is shown in Fig. 4c. In the theoretical model of Freeman and Dahlke[24] and in the experiments and analysis of Kar and Dahlke[25], different limiting processes and their corresponding approximations were discussed. We will briefly reintroduce these approximations here for the purpose of clarification.

As the carriers readjustment to interface states (step II) and drift in semiconductor (step V) are expected to be much faster compared to two other processes, we will only consider the interface states recombination limited and the oxide tunneling limited.

a. Interface states recombination limited The interface states recombination is limited when the interface states recombination time constant is much longer than the oxide tunneling time constant ($\tau_R >> \tau_T$). In other words, the oxide tunneling rate is much higher than the interface recombination rate. The interface states will thus be in equilibrium with the gate metal. In this case the interface states recombination limited was found to modify the Schottky barrier height due to the charge accumulated at the interface states[26–28]. Therefore, a self-consistent calculation is necessary to be performed in order to not violate the Gauss's law equations, as discussed by Werner et al.[27]. The rigorous self-consistence calculation was done by Muret[28] and also Wegner et al.[27] for Schottky diodes with a thin oxide layer.

In case of a MOSCAP system, the approximated equivalent circuit for the interface recombination limited was introduced by Freeman and Dahlke[24] and Kar and Dahlke[25]. The approximated equivalent circuit is shown in Fig. 5a) where interface states recombination is in equilibrium with the gate metal and interface states are in the same potential as the oxide potential. In this circuit, G_{it} is equal to $\frac{1}{R_p}$. One important notice is that, in case interface states recombination limited, the measured conductance is frequency independent[24,25].

b. Oxide tunneling limited When the oxide tunneling time constant is much longer compared to the interface states recombination time constant $\tau_T >> \tau_R$, the limiting process is the oxide tunneling. This means that interface states are considered to be in equilibrium with the semiconductor[24,25] and so, the injection from metal to interface states is approximated by an injection from the gate metal to the semiconductor. Interface states therefore will play a similar role as in the "non-leaky thick oxide" model where the interface states are in equilibrium and close communication with semiconductor band edges. In this circuit, G_{dc} is approximated to G_{ox} in Fig. 4b. The approximated equivalent circuit for oxide tunneling limited is shown in Fig. 5b).

A major difference between *interface states recombination limited* (Fig. 5 a) and *oxide tunneling limited* (Fig. 5b) is the measured conductance-frequency characteristics. For the purpose of comparison, the measured conductance circuit is the parallel conductance-capacitance $C_p - R_p$ circuit in Fig. 5f). In case of oxide tunneling limited, the measured conductance is frequency dependent, as shown in Fig. 5b). For the case of interface states recombination limited (Fig. 5a), the measured conductance is frequency independent[25].

Considering our O-diamond MOSCAP in this work, the measured conductance frequency dependent[15] indicates that the oxide tunneling process is the limiting process. The interface states recombination limited is possibly responsible in case of high injection MOSCAPs (e.g. current density ≥ 1 A/cm^2 at -8 V). In that case, the carriers injection from gate metal is sufficient to preserve interface states in equilibrium with the gate metal. The sample MOS #4 in Chicot et al.[10] and the sample 4×10^{19} cm^{-3} boron doped diamond in Kovi et al.[12] are most probably interface states recombination limited.

As a consequence from the previous analyses, the oxide tunneling process was identified as the limiting process in our MOSCAP test devices. However, since oxide tunneling is indeed a two step process, a further approximation

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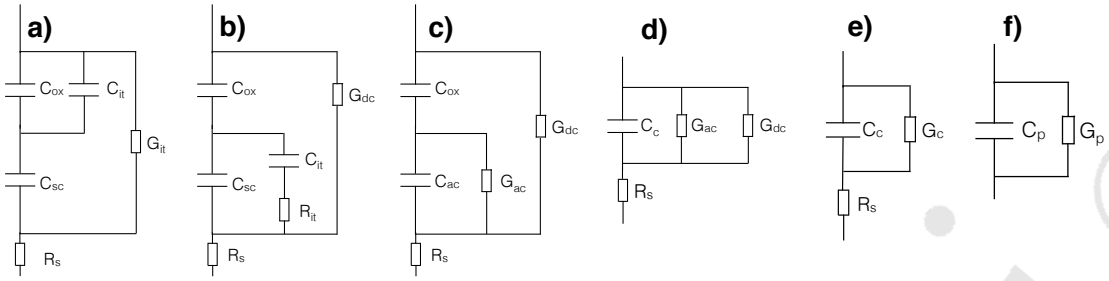

FIG. 5. Equivalent circuit for the O-diamond MOSCAP corresponding to the approximation: (a) approximate equivalent circuit for the interface states recombination limited case ($\tau_R >> \tau_T$) where $G_{it} = \frac{1}{R_{it}}$; (b) approximated equivalent circuit for the oxide tunneling limited case ($\tau_T >> \tau_R$) where $G_{dc} \approx G_{ox}$.; (c) Circuit (b) transformed to include a continuum of interface states.; (d) Circuit (c) transformed to show capacitance corrected for series resistance (C_c) and the c. conductance (G_{ac}); (e) Circuit (d) transformed to show C_c and conductance corrected for series resistance (G_c): (f) Circuit (e) transformed to show measured capacitance (C_p) and measured conductance (G_p):

is needed. Bearing in mind that the limiting process for oxide tunneling is either bulk oxide limited (hopping between traps to traps) or interface limited (tunneling from gate metal to oxide trap states). The difference is due to the nature of the contact between metal and oxide, i.e. an ohmic contact or an unsaturated contact[41]. Ohmic contact indicates the strong injection of carrier from metal electrode to oxide layer. Unsaturated contact indicates the low injection of carrier from metal electrode to oxide layer. Depending on the nature of metal/oxide contact, I(V) characteristics will exhibit a specific power law of $I = AV^{\alpha}$. Therefore, in order to examine the power law of MOSCAPs and the contact nature at metal/oxide interface, we introduce the I(V) curves in the log-log plot. Figure 6 a) and Figure 6 c) represent the power law of two typical MOSCAPs: low injection MOSCAP (MOS50 - sample #1) and high injection MOSCAP (MOSA1 - sample #1), respectively.

For the low injection MOSCAP at RT (Fig. 6 a)), the $I \sim V^5$ law indicates that the metal-oxide contact in this device is the unsaturated contact. The interface-limited traps assisted tunneling[42] mechanism is probably governing this low injection MOSCAP at RT.

To study the thermal activation process, we measured the I(V) characteristic of the low injection MOSCAP at different temperatures, ranging from 160 K to 360 K. Figure 6b) represents the Arrhenius plot current density versus temperature of the low injection MOSCAP, measured at three different gate bias: $V_G = -8\ V$, $-6\ V$ and $-4\ V$. From the slope the thermal activation energy at different gate bias can be evaluated. The thermal activation energies are varying from $E_A = 260\ meV$ at $V_G = -4V$ to $E_A = 208 meV$ at $V_G = -4V$. As suggested from the generalized thermionic trap assisted tunneling model[42], this thermal activation energy is assigned to the barriers between metal and Fermi-Dirac occupancy function of the oxide trap states (Fig. 4a). This thermal activation energy variation with gate bias is in agreement with eq. 12.

For high injection MOSCAP (MOSA1 - sample #1), the I(V) characteristics at different temperatures from 160 K to 360 K are shown in Fig. 6 c). At RT, the $I \sim V^2$ of Child law Space Charge Limited Current (SCLC)[43] is identified (Fig. 6c). This power law indicates that the metal-oxide contact of this MOSCAP is an Ohmic contact at RT and the limiting process is the trap-to-trap hopping process in the bulk of the gate oxide.

Figure 6d) represents the current density measured at $V_G = -8$ V versus temperature of the high injection MOSCAP. The J-T curve is well fitted by a $e^{(\frac{T_0}{T})^{1/4}}$ law, which is characteristic of variable range hopping (VRH)[44]. This further confirms the trap-to-trap hopping space charge limited current in the high injection MOSCAPs.

In summary, this analysis demonstrates that one of the most important origin responsible for the leakage current of O-diamond MOSCAPs is the trap states in the gate oxide. To improve the gate control diamond semiconductor, the gate oxide leakage current must be minimized by introducing a new process that could limit both the metal/oxide interface injection and traps to traps hopping in the bulk of the oxide layer.

V. INTERFACE STATES OF AL_2O_3/O-TERMINATED DIAMOND

This section is dedicated to the investigation of interface states properties at Al_2O_3/O-terminated diamond interface. Thanks to the small signal equivalent circuit discussed above, we will be able to use a corrected conductance method in order to determine the interface traps density and their energy location within the diamond bandgap.

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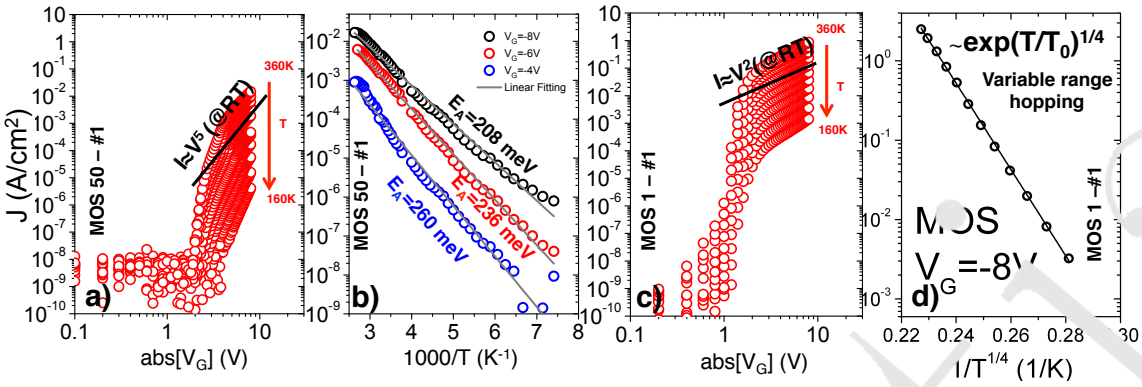

FIG. 6. (a) Experimental log-log plot I(V) characteristics of the low injection MOSCAP (MOS 50 - sample #1). (b) Arrhenius plot current density versus Temperature at different gate bias: V_G=-8V, -6V and -4V, indicates the thermal activation energy of the low injection MOSCAP. (c) Log-log plot I(V) characteristics of high injection MOSCAP (MOS1-sample #1); (d) Current density at $V_G = -8V$ versus versus $\frac{1}{T^4}$ indicates the variable range hopping in the high injection MOSCAP.

A. Equivalent conductance G_p/ω

The conductance of interface states ($G_{it} = \frac{1}{R_{it}}$ where R_{it} is the one of Fig. 4c represents the energy loss due to carrier transfer between semiconductor band edge and interface states after a disturbance of a small *ac* signal. In more details, it can be understood as the supplied small *ac* signal in both halves caused the disturbance and drive the system between semiconductor band edge and interface states become to be out of equilibrium. Therefore, there are carriers transferred between interface states and band edge. However, the carrier transfer is not instantaneous after the signal was supplied but lag behind and caused the loss. The losses are minimized or the conductance is maximized when the applied signal is equivalent to the resonant frequency of the interface states. With the applied frequency lower than the resonant frequency, carriers are stored at the capacitance of the interface states but not transferred. Subsequently, the conductance of the interface states is decreased. Therefore, the conductance of interface states which is bearing the information of interface states should have a bell shape. In the conductance method, the goal is to obtain the equivalent interface states conductance from measured conductance and capacitance ($C_p - R_p$).

In order to obtain the equivalent interface states conductance, measured parallel conductance and parallel capacitance are necessary to be corrected in order to eliminate the series resistance, the DC current and gate oxide capacitance. In this work, the circuit transformation follows the procedures introduced by Kar and Dahlke et al.[25] and by Vogel et al.[45]

From the measured conductance and capacitance, the corrected conductance with series resistance of Fig. 5f) is given by:

$$C = \frac{C_p}{(1 - G_p R_s)^2 + \omega^2 C_p^2 R_s^2} \tag{19}$$

and the corrected capacitance by:

$$G_c = \frac{\omega^2 C_p C_c R_s - G_p}{G_p R_s - 1} \tag{20}$$

Then, G_{ac} in Fig. 5e) is obtained by:

$$G_{ac} = G_c - G_{dc} \tag{21}$$

where the conductance G_{dc} is determined from the slope of the DC current versus DC voltage curve at a given gate bias voltage $\left(\frac{dI_{dc}}{dV_{dc}}\right)_{V_G}$. Then, the ac conductance G_{ac} must be corrected with the gate oxide capacitance C_{ox} to obtain the equivalent conductance G_P/ω by using the equation:

$$\frac{G_P}{\omega} = \frac{\omega C_{ox}^2 G_{ac}}{G_c^2 + \omega^2 (C_{ox} - C_c)^2} \tag{22}$$

For the purpose of comparison the interface states density with Terman's method, we will present here the data measured on the MOS 12 on sample #1). The equivalent conductance at different gate bias are shown in Fig. 7a). The equivalent conductance shows the clear bell shape feature with a clear maximum $\left(\frac{G_P}{\omega}\right)_{\max}$ peak. As mentioned above, the frequency corresponding to the $\left(\frac{G_P}{\omega}\right)_{\max}$ is equivalent to the resonant frequency of interface states. By varying the gate bias from $-8\ V$ to $-4\ V$ (MOS 12 - sample #1), the $\left(\frac{G_P}{\omega}\right)_{\max}$ are gradually moving toward the lower frequency since the Fermi level is moving away from the valence band.

B. Interface states properties

From the equivalent conductance G_P/ω, the interface states density can be calculated as[38]:

$$N_{it} = 2\left(\frac{G_P}{\omega}\right)_{\max} / q \tag{23}$$

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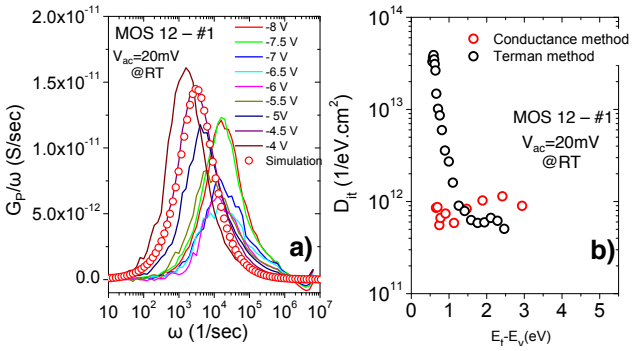

FIG. 7. (a) Equivalent conductance G_p/ω at different gate bias ranging from -4V$\leq V_G \leq -8V$ of the MOS 12 - Sample #1, measured at RT. The single level interface state model is employed to simulate the equivalent conductance and demonstrate a good agreement. ; (b) Interface states density at O-diamond/Al_2O_3 interface measured by conductance method (open red circle curve) and by Terman method (open black circle curve).

with $\left(\frac{G_P}{\omega}\right)_{\max}$ the maximum of the $\left(\frac{G_P}{\omega}\right)$ curve. The open red circle curve in Fig. 7b) represents the interface states density extracted by conductance method versus the corresponding energy of the trap states in diamond band gap. The energy level of the trap states is then calculated by using the equation:

$$E_{it}\left(V_G\right) - E_v = \Psi_s\left(V_G\right) + \phi_p \tag{24}$$

where $\Psi_s\left(V_G\right)$ is extracted in the previous electrostatics section and $\phi_p \simeq \left(\frac{kT}{q}\right)\ln\left(\frac{N_v}{N_A}\right)$, which is assumed to be 0.37 eV in the case of moderate boron doped diamond.

A notable difference of the interface states density extracted from the conductance method compared to the interface density extracted from Terman's method (the open black circle curve in Fig. 7b)) appears near the valence band. While Terman's method gives an elevated interface states density up to 4×10^{13} $\left(cm^{-2}\right)$ at $E_{it} - E_v = 0.6$ eV, the results from the conductance method are approximately one order of magnitude lower in the same energy range.

This discrepancy is attributed to the gate leakage current and subsequently, the potential drop in the gate oxide. In Terman's method[22], the variation of semiconductor surface potential Ψ_S with gate bias V_G is completely attributed to the interface states at the semiconductor/oxide interface. It is true when leakage current through the oxide is negligible. However, when the DC current is sufficient, the potential drop in the gate oxide is non-negligible. Therefore, in high injection regime, Terman's method highly overestimates the interface states density and cannot be used to evaluate the interface trap density.

In the conductance method, the contribution of DC current is actually excluded by equation 21. The final interface states density will therefore exclude the contribution from DC current. Electrostatic simulations $\Psi_S - V_G$ using the interface states density extracted from Terman's method and from the conductance method have further demonstrated the accuracy of the conductance method[15]. We conclude that the interface states density extracted from the conductance method is more reliable than Terman's method.

	MIM	HF MOS	G_p/ω	τ_{it}	DC I-V
V_G(V)	C_{ox}(pF)	C_{sc}(pF)	C_{it}(pF)	R_{it}(MΩ)	$G_{dc}(\mu S)$
-8	70.8	35.8	24.2	2.6	0.64
-7	70.8	31.2	15.7	4.07	0.50
-6	70.8	26	20.9	4.8	0.33
-5	70.8	18.2	23.5	10.7	0.153
-4	70.8	13.36	3[illegible]2	19.68	0.05

TABLE II. Input parameters for the LTSPICE simulation and the corresponding extraction method.

By assuming that the interface states are single level states[38], i.e. Dirac energy distribution for the density of the trap, the equivalent conductance G_P/ω can be simulated by using the equation:

$$\frac{G_P}{\omega} = \frac{C_{it}\omega\tau}{1+\omega^2\tau^2} \tag{25}$$

where τ is the characteristic time constant of interface states and is determined at $\left(\frac{G_P}{\omega}\right)_{\max}$, where $\omega\tau = 1$. The interface states capacitance C_{it} can be determined from the peak of the equivalent conductance G_P/ω as $C_{it} = 2\left(\frac{G_P}{\omega}\right)_{\max}$. Knowing all parameters, the measured equivalent conductance can be simulated using equation 25 for the single level interface states model. The simulation curves by using single level interface state model and the parameters extracted from the conductance method are in agreement with the experimental curves for the bias range -4V $\leq V_G \leq -8V$[15], as depicted in Fig. 7a). We conclude that the single level interface state model is sufficient to describe the interface states at the O-diamond/Al_2O_3 interface. The similar results are also obtained for sample #2.

VI. CAPACITANCE-FREQUENCY DEPENDENCE

This section is dedicated to reproduce the capacitance-frequency characteristic of the O-diamond MOSCAPs by using the small-signal equivalent circuit introduced in the previous section (Figure 5b). The impedance simulation is performed with LTSPICE software.

One can note that all the parameters of the equivalent circuit have been experimentally extracted. The oxide capacitance C_{ox} was measured by using the MIMCAP. The semiconductor capacitance $C_{sc}\left(V_G\right)$ was evaluated from MOSCAP capacitance measurements at "middle frequency regime"(f = 100 kHz), as described in section III. Series resistance R_s can be determined from the "real part" of impedance measurements in the "high

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frequency regime" $f = 1$ MHz[15]. The DC conductance is obtained from the statics I-V characteristics of the test device by using $G_{dc} = \frac{dI_{dc}}{dV_{dc}}$. It must be noticed that $G_{dc}(\omega) = G_{ox}(\omega) + \frac{1}{R_{it}}$ is frequency dependent due to the hopping process which is represented by $G_{ox}(\omega)$. However, from MIMCAP measurements, a negligible frequency dependence was measured in this frequency range. The G_{ox} variation from MIMCAP is lower than 10 nS for frequencies ranging from $1Hz$ to $1kHz$[15]. Finally, interface states capacitance C_{it} and interface states resistance R_{it} were evaluated by conductance method $\left(\frac{G_P}{\omega}\right)$ with $C_{it} = 2\left(\frac{G_P}{\omega}\right)_{\max}$ and $R_{it} = \frac{\tau_R}{C_{it}}$ where τ_R is extracted at $\left(\frac{G_P}{\omega}\right)_{\max}$.

Table II summarizes the parameters extracted by various methods at different gate bias for the impedance simulation. The LTSPICE simulation results are plotted

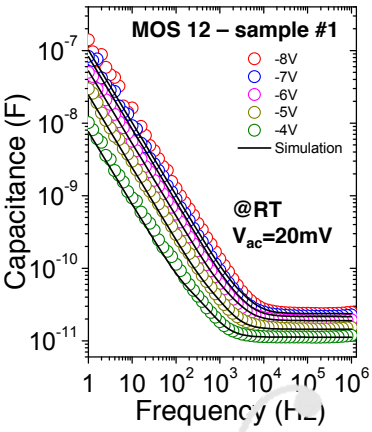

FIG. 8. Measured Capacitance-frequency dependence of the MOSCAP test device is reproduced by LTspice simulation with all the parameters extracted experimentally.

in Fig. 8 along with the capacitance-frequency dependent curves measured from MOS 12 - sample #1. The simulations using the proposed equivalent circuit and all extracted parameters reproduce the measured capacitance-frequency dependence of the O-diamond MOSCAP. We conclude that the capacitance-frequency dependence of the O-diamond MOSCAPs is originated from the complex charge transfer process from metal to oxide and recombine with diamond valence band at the interface states.

In summary, the comprehensive electrical characterization, analysis and simulations have demonstrated that the complex charge transfer process from gate metal to gate oxide, traps to traps hopping in bulk oxide and the interface/valence band recombination is the origin of the parasitic leakage currents, FLPE and capacitance-frequency dependence observed in the O-diamond MOSCAPs. Therefore, in order to eliminate these artifacts, it is very important to improve the oxide crystallinity, to increase the oxide thickness to decrease the hopping rate and to improve the interface of the O-diamond/Al_2O_3 interface.

VII. CONCLUSION

In summary, the comprehensive electrical characterization, analysis and simulations have demonstrated that the complex charge transfer process from gate metal to gate oxide, traps to traps hopping in bulk oxide and the interface/valence band recombination is the origin of the parasitic leakage currents, FLPE and capacitance-frequency dependence observed in the O-diamond MOSCAPs. Thanks to this comprehensive understanding, we established a new method that allows the complete electrostatics gate controlled O-diamond MOSCAP. This will open a new route toward gate controlled diamond MOS devices for power electronic applications.

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Chapter 3

Depletion-mode Metal Oxide Semiconductor Field Effect Transistor (MOSFET) on Oxygen Terminated boron doped Diamond

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3.1 Introduction

3.1.1 Transistor electrical characteristics

In Chapter 2, the comprehensive studies on boron doped O-diamond MOS capacitor test device were detailed. Based on electrostatics model, current transport mechanism and

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a.c small signal analyses, the prominent electrical characteristics can be summarized as follows:

1. When the O-diamond MOS capacitor is under negative bias, the FLPE was observed due to interface states and carriers injection from the gate metal. The accumulation of majority carriers (holes) was not obtained.

2. When the O-diamond MOS capacitor is under positive bias, an efficient control of the Space Charge Region (SCR) width in diamond was obtained. This special feature opens an opportunity to realize a depletion mode diamond MOSFET (D-transistor).

First, we will briefly introduce about the general concept of a transistor. The first transistor is realized in 1947 at Bell lab by Bardeen and Brattain [25]. Transistors are categorized into two types: current controlled transistors (BJT, Thyristor, GTO) and voltage controlled transistors (FET transistors as JFET, MOSFET, MESFET). The MOSFET family consists in two main types: enhancement mode and depletion mode. Figure 3.1a represents the typical structure of an enhancement transistor, with electron as majority carriers. Basically, a MOSFET includes a Source (S), a Drain (D) and a Gate (G), with a Bulk/Substrate contact (B). In a proper transistor, when V_{DS} is applied, the current flowing between S and D (I_{DS}) is controlled by the voltage between G and S (V_{GS}). An enhancement mode MOSFET is usually a normally OFF transistor where the channel and/or Drain-Source regions have a high impedance for $V_{GS} = 0$ V. A depletion mode MOSFET is usually a normally ON transistor where the channel has a reduced impedance when $V_{GS} = 0$ V. Even if there are certain differences between an enhancement MOSFET and a depletion MOSFET, their typical electrical characteristics are relatively similar. Typical electrical characteristic of a MOSFET is shown in Fig. 3.1b. For a small V_{DS}, I_{DS} increases linearly with V_{DS}. This is the linear region where the transistor is working like a resistor. For a high V_{DS}, I_{DS} saturates with the increase of V_{DS}. This is the saturation region where the transistor is working like a current source. The magnitude of the saturation current is actually controlled by V_{GS}. For V_{GS} below the threshold voltage (V_{th}), only leakage current flow between electrodes - OFF state. In this state, the transistor is working like an open circuit. By increasing V_{DS}, breakdown of the device will be observed. Subthreshold leakage current is readily increased due to breakdown event.

In fact, depletion mode transistors are the oldest members of the MOSFET family. A depletion mode transistor is required in those applications that need a normally-ON switch. Inverter, voltage follower or switch are the obvious applications with a depletion mode transistor. However, most of the efforts in the past were pushed to the enhancement mode transistors. It is because that most of the transistors were realized on narrow band gap semiconductors like Si where the inversion is obtainable and deep depletion is unobtainable. Moreover and to the application point of view, normally OFF devices are preferred in power electronics to reduce the risk of power short circuit. The concept of depletion mode transistors is widely considering recently on different III-V or III-O materials, as example in N-type β-Ga_2O_3 [126, 127, 128].

3.1.2 Diamond FET devices

As discussed in Chapter 1, diamond is the ultimate material for power device applications. Even if some others diamond MOSFETs were already realized, most of them are usually

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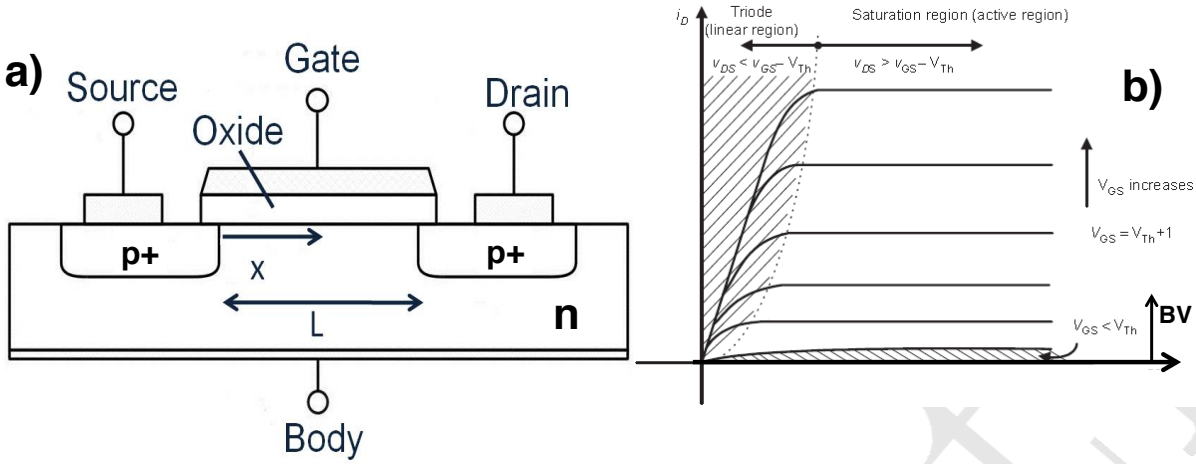

Figure 3.1: a) Typical structure of an enhancement transistor; b) Typical electrical characteristics of a Transistor

based on the concept of two dimensional hole gas (2DHG) at the H-terminated diamond surface.

3.1.2.1 H-diamond MOSFET

A general device cross-section and plan view structure of the H-diamond MOSFET are shown in Fig. 3.2.

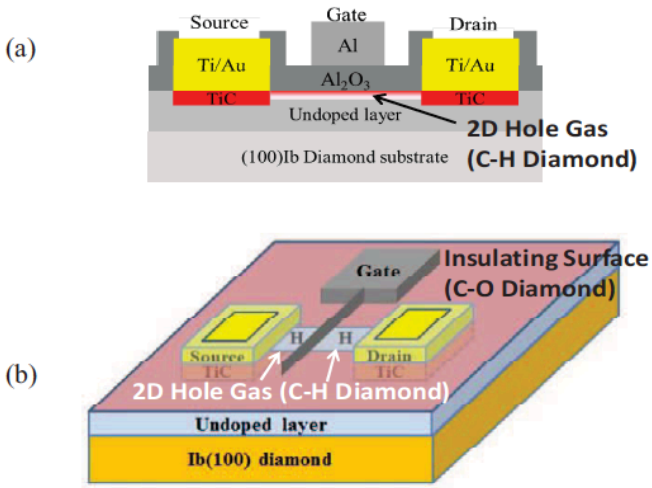

Figure 3.2: Structure of a transistor on H-diamond. a) Cross-section structure; b) Plan view structure. Courtesy of Kawarada et al. [21]

A particular feature of a H-diamond MOSFET is that most of the time the substrate is intrinsic or highly resistive. Therefore, the Breakdown Voltage (BV) is relatively fixed by the distance between Drain and Gate (L_{GD}). The ON-state resistance is fixed by the sheet carrier density, the carrier mobility in the 2DHG, the distance between Drain and Source (L_{DS}), the distance between Drain and Gate (L_{GD}) and the Gate Length (L_G). Even if there are remarkable results like ON-state current around 100 mA/mm at $V_{DS} = -50$ V and OFF-State breakdown voltage up to 1700 V [76][21], there are certain

demerits in this kind of devices. As we pointed out in Chapter 1, its working mechanism is based on an uncontrolled parameters (negative charges in the oxide). Moreover, temperature effects typically increase the ON state resistance, similar to GaN HEMTs and other transistors at typical temperatures. Since 2DHG and BV are not related, there is another approach which can take benefits of bulk diamond properties: by optimizing the drift region doping level (Drain-Gate, its doping and thickness), we can find a better compromise in channel sheet carrier density versus BV. Indeed, using higher doping levels can increase the peak electric field [23]. Moreover, boron doped channel resistance will exhibit a negative then positive temperature coefficients, where as 2DHG based devices will have a positive coefficient.

3.1.2.2 Bulk controlled diamond transistor

In bulk controlled MOSFET, the substrate doping concentration is optimized (BV vs. R_{on} compromise). The BV is fixed by the Non-punch though (NPT) design. The ON-state resistance is a consequence of the drift region design L_{GD}, channel region L_G and conduction region L_{GS}. R_{on} typically exhibits a negative then positive temperature coefficient [23].

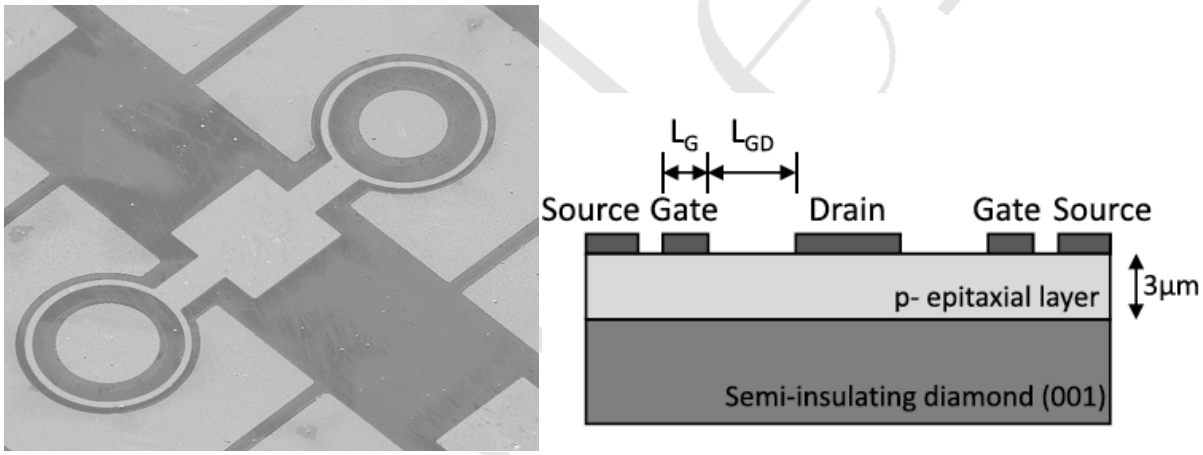

Figure 3.3: Structure of the p-type diamond MESFET a) top view; b) cross-section. Courtesy of Umezawa et al. [16].

Diamond MESFETs that were introduced by Umezawa [16] are the first properly bulk controlled boron doped diamond transistors. Figure 3.3 represents the cross-section structure and top view structure of the diamond MESFETs. High breakdown voltages (≥1500 V) were obtained [16]. ON-state currents were highly limited by contact resistance. The ON-state is sufficiently improved by increasing the temperature, with an improvement by a factor of 3 between RT and 300°C. The demerit of this structure is the constraint in doping concentration ($\leq 10^{16}\,(cm^{-3})$) of the epilayer to limit the gate leakage current of the Schottky contact [78]. As a consequence, the drift region can not be ideally optimized as in Chicot et al. [23], targeting higher doping levels where BV of the order of kV are desired. Also, in p-type MESFET device, only positive bias can be applied by gate metal because the Schottky contact between gate metal and diamond epilayer. Therefore, accumulation regime in p-type semiconductor can not be obtained. In some moderate breakdown voltage device (about 1 kV), this limitation is undesired to improve

ON-state current. The utilization of a gate insulator can circumvent these constraints, allowing one to increase the doping level of the epilayer as well as biasing the gate metal in negative bias voltage toward accumulation.

The aim of this chapter is to introduce the first design and proof of concept to realize a depletion mode diamond MOSFET. After the introduction, we will present the design, the fabrication process, the electrical measurements and the 2D finite element simulations. The electrical measurements on the test devices such as Transmission Line Model (TLM) and MOS capacitors will be presented in the next part. The electrical characteristics, their analysis and the 2D simulation of the diamond transistor in both the ON-state and OFF-state are followed. Finally, the chapter will be concluded.

3.2 Methodology

3.2.1 Transistor design

We will firstly present in details the design of our transistors in the following sections.

3.2.1.1 Cross-section

The conceptual cross-section structure of the device is shown in Fig. 3.4.

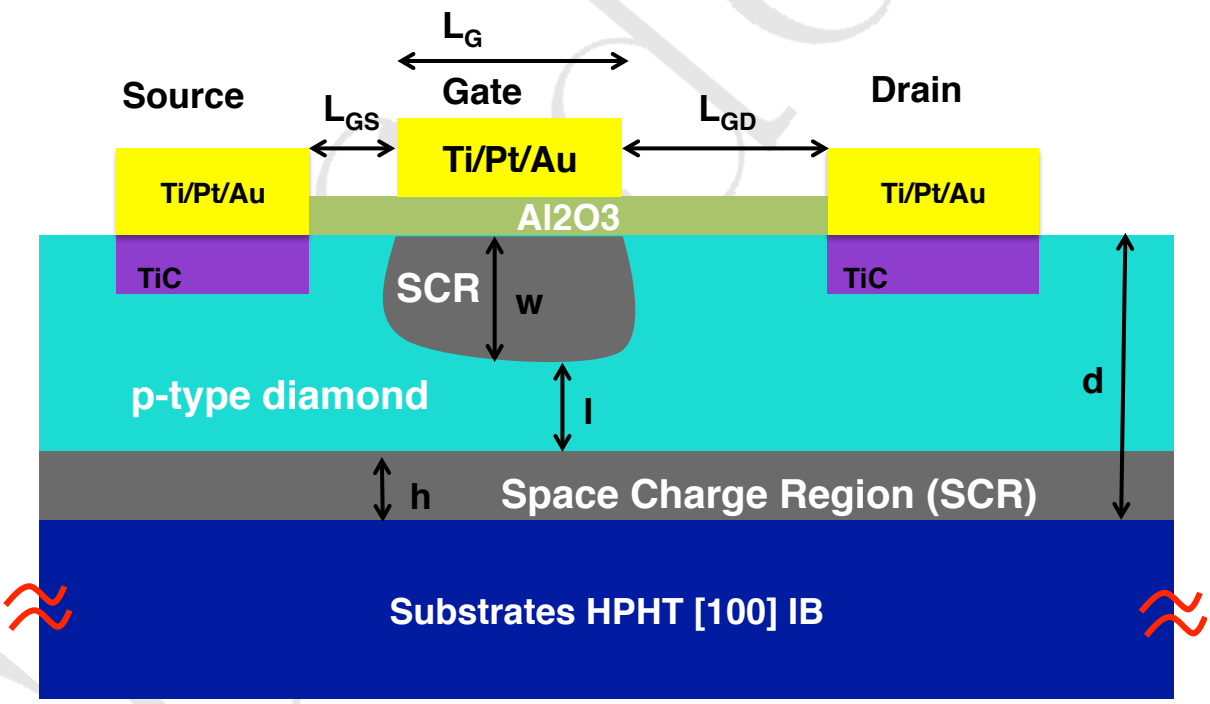

Figure 3.4: Cross-section structural concept of depletion mode oxygen-terminated boron doped diamond MOSFET.

There are two Space Charge Regions (SCR) in the p-type diamond epilayer: SCR at oxide-diamond interface and the SCR of the p-n junction at substrate-epilayer interface. Carriers are flowing in the neutral and conducting region between source and drain. The ON-OFF regime of the device is controlled by modifying the SCR width under the gate relying on the deep depletion through the MOS capacitor.

The p-n junction is formed because 1b diamond substrates are highly Nitrogen (N) doped with the assumed N concentration of 3×10^{19} cm^{-3} [22]. The expected depletion width in the epilayer at substrate-epilayer interface is calculated by the relationship:

$$W_{epi} = 2\sqrt{\frac{\varepsilon_{sc} kT}{2q^2 N_D} \frac{1}{\left(1 + N_{A/} N_D\right)} \ln \frac{N_A N_D}{n_i^2}} \tag{3.1}$$

where N_D is the [N] donor concentration of the substrate, N_A is the [B] acceptor concentration in the epilayer, n_i is the intrinsic carriers concentration. Figure 3.5 represents the expected depletion width in p-type epilayer with different doping concentration [22].

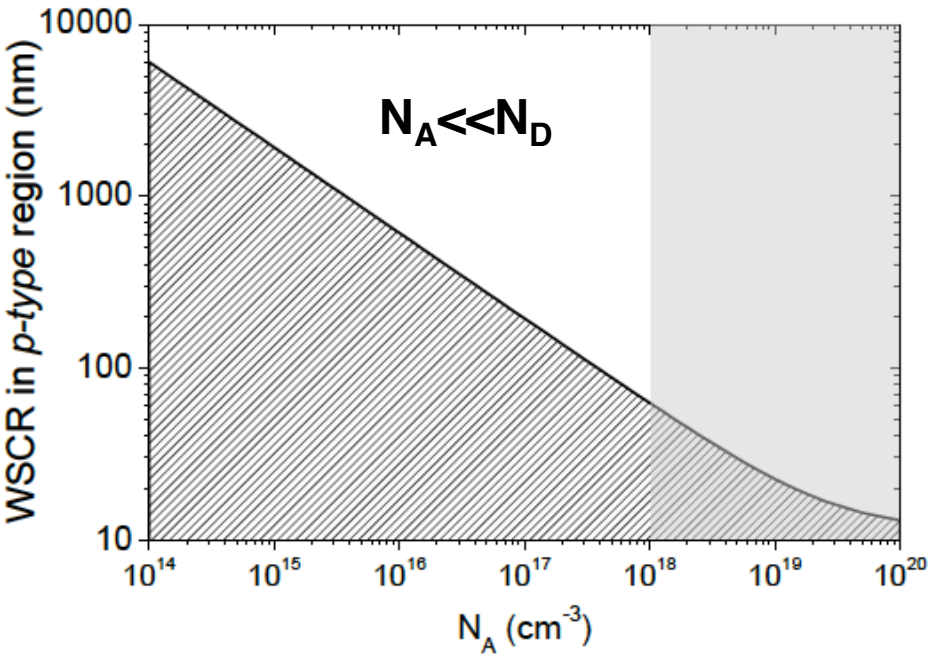

Figure 3.5: Expected depletion region width between substrate and epilayer with different doping concentration. Considering the 1b substrate is highly nitrogen doped ($N_D = 3 \times 10^{19}$ cm^{-3}). Courtesy of Chicot's PhD thesis [22].

In the first approach, we fabricated two samples with multiple diamond transistors and test devices on a same substrate. In sample #1, a p-type diamond epilayer with the target boron doping concentration of $2{\times}10^{17}$ cm^{-3} and a Al_2O_3 gate oxide with a 20 nm thickness were employed. Sample #2 is fabricated to target higher breakdown voltages device. Therefore, the epilayer doping concentration is decreased (target $5{\times}10^{16}$ cm^{-3}) and the oxide thickness is increased (40 nm). Consequently, sacrificed SCRs width of 100 nm and 230 nm are expected for sample #1 and sample #2, respectively (Fig. 3.5).

The details of the two sample parameters and processing conditions are presented in table 3.1

.

In principle, the channel is OFF when the two SCRs are collapsed and the whole thickness of epilayer under the gate is depleted. The channel is ON when the neutral region under the gate is existing. As we have mentioned, in some moderate breakdown voltage applications (around 1 kV), the channel conductance can be improved by the

Name	[B] (cm^{-3})	d_{epi} (nm)	T° ALD (°C)	t_{ox} (nm)	Ohmic annealing (°C)	Oxide annealing (°C)
#1	2×10^{17}	230	380	20	600	NA
#2	5×10^{16}	500	380	40	700	500°C-VC

Table 3.1: Details of substrate parameters and processing conditions of two sample.

free hole gas under the gate when the MOS structure are under accumulation regime. Furthermore, if the accumulation regime can be obtained, one can design a normally-OFF D-mode diamond transistor. However, as we have identified the FLPE of O-diamond MOS capacitor toward accumulation in the Chapter 2, we designed here a Normally-ON transistor, taking sufficient margins to guarantee that both a ON state and a OFF state will be possible.

Regarding the dimensions of the device, the distance from Source to Gate (L_{GS}) is kept constant as $L_{GS} = 4$ μm during this experiment. Two values of the gate width (L_G) are chosen as $L_G = 3$ μm and $L_G = 4$ μm. These values have been a consequence of sufficient margin to the fabrication point of view, but both L_{GS} and L_G can be reduced: L_{GS} must be designed to prevent gate to source breakdown (both in air and in diamond), where L_G must be reduced as much as possible (lithography and gate technique limits). We are then varying the distance from Gate to Drain as $L_{GD} = 2$ μm, 3 μm, 5 μm, 10μm. The $L_{GD} = 10$ μm is expected to obtain the highest V_{BD} for the low doped sample (sample #2, with a dependence of BV on L_{GD}). For the highly doped sample, short L_{GD} is expected to obtain a low R_{ON}, where larger L_{GD} must not modify the BV.

3.2.1.2 Top view

We intentionally introduced different device structures to target high voltage, high total current and bidirectional devices (double gated transistors), while investigating the effect of total active area and key parameters sweeping. The devices designed are the stripe structure (one short finger), the circular structure (optimized 3D electric field distribution), the multiple-finger structure and double gate structure (bidirectional voltage-current transistors).

For this first proof of concept, two lithography levels are considered: "ohmic" contact (drain and source metallization - in red color in Fig. 3.6 to Fig. 3.7) and gate metal (in yellow color in Fig. 3.6 to Fig. 3.7).

To target a high ON-current device, wide transistors are required. We employed then the stripe structure and finger structure, as shown in Fig. 3.6. For the stripe structure, three different channel widths ($W = 30$ μm, 100 μm, 150 μm) were designed. As explained herein below, finger based transistors are designed for the purpose of ON state measurement.

A problem with the stripe and finger structures is the edge effects that could lead to premature voltage breakdown. In order to minimize the edge effects, we designed

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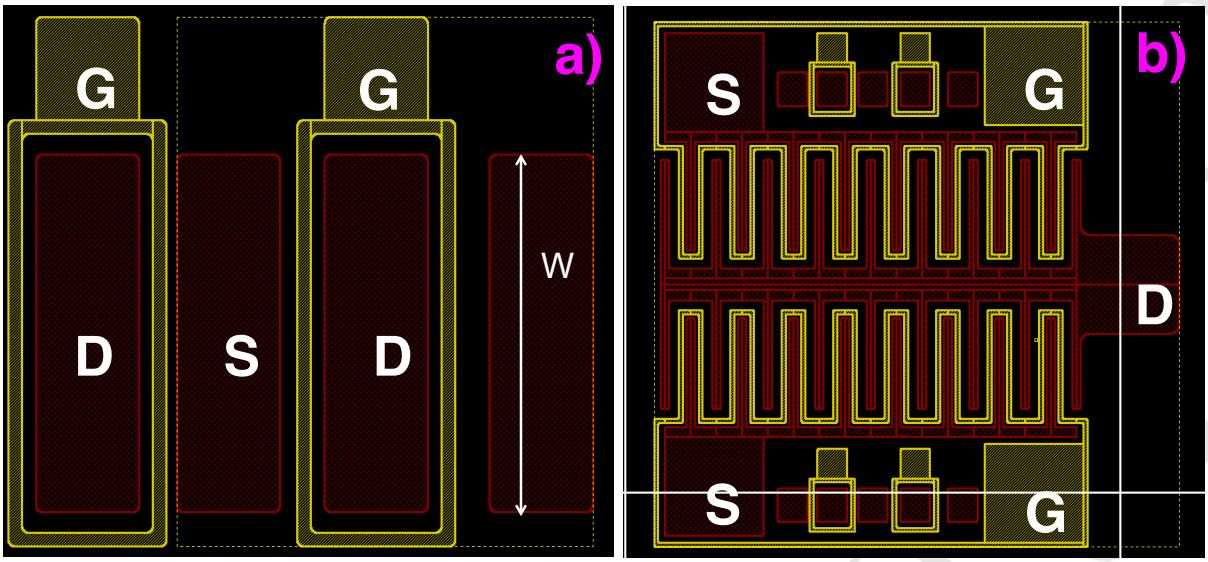

Figure 3.6: Transistor structure target high ON-states current a) Stripe structure; b) Fingers structure.

the circular structures to target the high voltage device and prevent premature 3D edge voltage breakdown. The device structure is shown in Fig. 3.7.

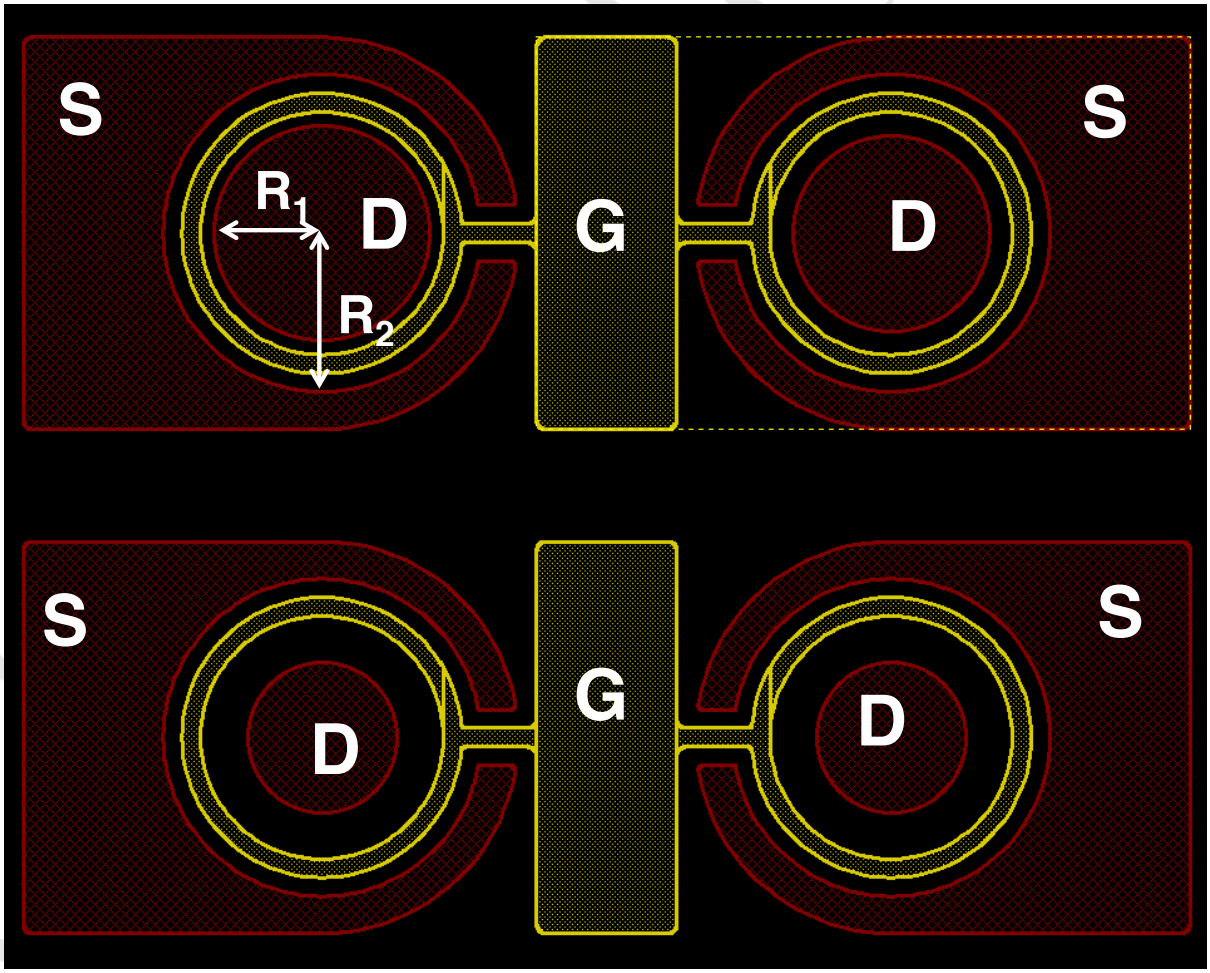

Figure 3.7: Circular structure transistor target high OFF-state breakdown voltage.

Along with the different transistor structures, we also introduced test devices like MOS capacitors and TLM, with the limit of our two lithography fabrication processes. TLM is inserted at the border to measure the contact resistance and sheet resistance. Different device structures and test devices are included in a reticule. A complete structure of a reticule is shown in Fig. 3.8a. The complete mask includes 3×3 reticules and the TLM. The full mask structure is shown in Fig. 3.8b.

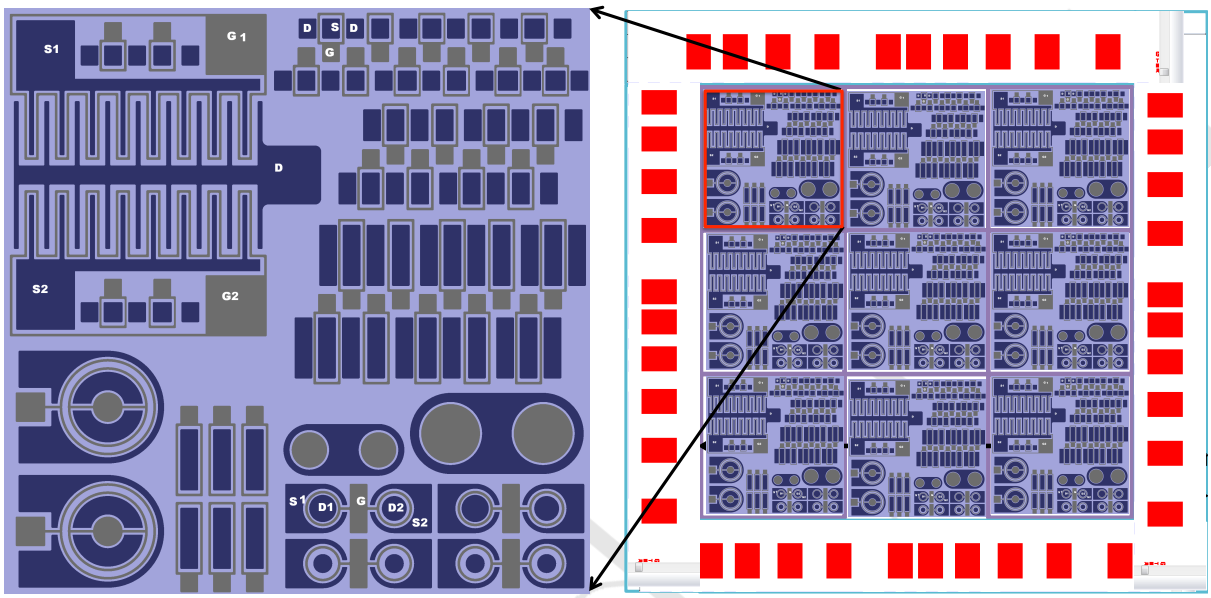

Figure 3.8: a) A complete structure of a reticule included different device structures and test device; b) The full mask structure includes 3×3 reticules and the TLM.

3.2.2 Fabrication

Boron doped diamond epilayers were grown on a $4 \times 4mm^2$ Ib High Pressure High Temperature (HPHT) Nitrogen-doped substrate. Detailed conditions on diamond growth and doping controlled were addressed in chapter 2 and also previous PhD of the group [4, 22, 78, 24].

For the device fabrication, different processes in series are needed. The detail flowchart of devices fabrication processes are shown in Fig. 3.9.

After the growth of epilayers, dusts were removed by using conventional solvent in ultrasonic condition. Then, graphite and non-diamond phase were removed by using conventional cleaning recipe of a three acid mixture (H_2SO_4, HNO_3 and $HClO_4$) at $300°C$, as shown in step 1, Fig. 3.9.

For the fabrication process, positive photoresist S1805 was coated on top of epilayer by using conventional spin coating which produces a thickness approximately 5 μm, as shown in the step 2 - Fig. 3.9. Laser lithography (Heidelberg DWL66FS) was employed to define the contact area. In order to obtain the expected device structure, two steps of lithography were performed (step 3 and step 7 - Fig. 3.9). After lithography process, the substrate is going through the develop and plasma etching to remove residual photoresist on the patterned region before metal deposition. Plassys ebeam evaporator was used in

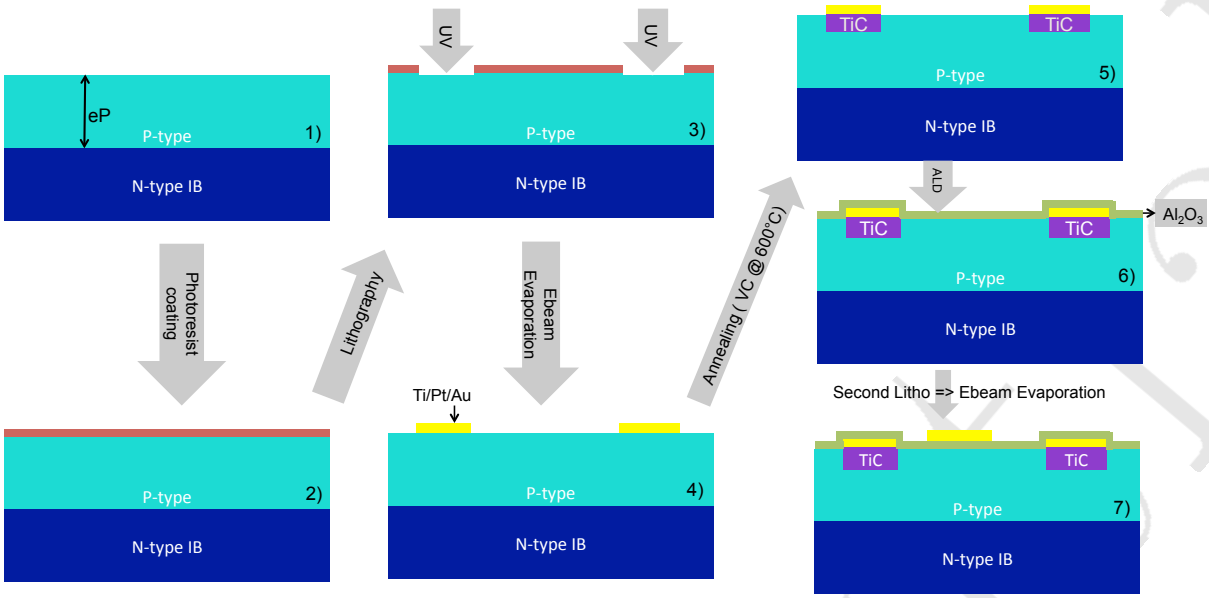

Figure 3.9: The flow chart fabrication process of depletion mode O-diamond MOSFET.

the step 4 to deposit the stack of Ti/Pt/Au stack with thickness of 40 nm/10nm/40 nm respectively (Fig. 3.9). Lift-off was done by rinsing the substrate in acetone solution.

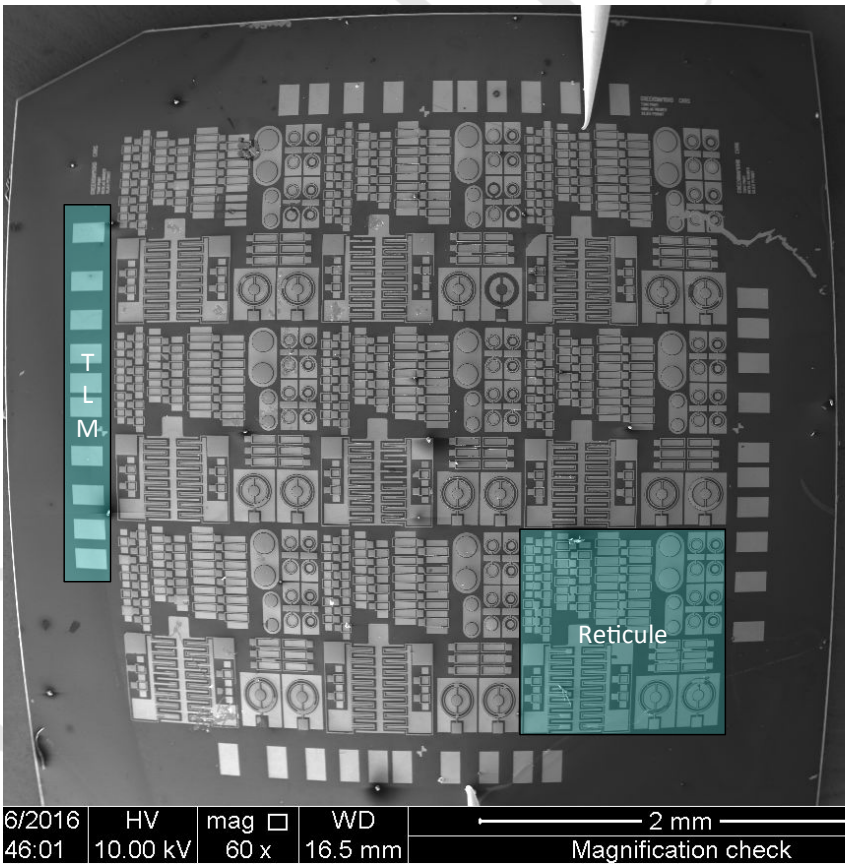

Figure 3.10: Top view FESEM photograph of the completed boron doped diamond MOSFET and test devices (sample #1).

Since as-deposited Ti/Pt/Au on top of diamond does not show ohmic contact behav-

ior, an annealing at high temperature was required [129]. In order to form ohmic contact, the samples were annealed at high temperature (600° C for sample #1 and 700 °C for sample #2) in vacuum environment with typical pressure of $10^{-8}(mbar)$ in the step 5 - Fig. 3.9. The diamond surface were then oxygenated by using deep UV-ozone treatment [79]. Al_2O_3 gate oxide were deposited at $380°C$ by using Savannah 100 deposition system from Cambridge NanoTech in the step 6 - Fig. 3.9. The precursor was Trimethylaluminium (TMA) and oxidant was water. The pulse and exposure duration were 15 ms and 30 s, respectively. Typical chamber pressure was 1.3×10^{-1} (Torr).

Figure 3.10 represents FESEM image of the completed devices after the fabrication.

3.2.3 Measurements

Devices were probed by employing a homebuild micromanipulator system in the Field Emission Scanning Electron Microscope (FESEM) chamber [124]. For the MOSFET measurement, a two channel Keithley 2636 Source Meter Unit was used. For the test devices (i.e. MOS capacitors) a Solartron Modulab was used, with an AC voltage $V_{ac} = 20$ mV and the frequency ranging from 1 Hz to 1 MHz.

3.2.4 Simulation

For device simulation, Silvaco 2D Atlas [130] was employed. Simulation is performed in this work for a two fold purpose: Firstly, thanks to existing models that were developed previously in our group [23, 131, 24], a finite element analysis will be conducted on diamond MOSFET. The simulation results will be compared with experimental results. Thanks to the simulations in 2D structure, visualization is easier and further support for the understanding. However, since the simulation models are not really completed (oxide charges, interface states and leakage current were not included), a further improvement will be required. In the second fold purpose, parameters that were extracted from the experimental results will be provided for an empirical model. This is an important step since diamond is a relatively new material. Many parameters are still unknown. Considering the fact that experiments for diamond power devices are costly and time consuming, an as completed as possible simulation model is highly desired.

Since the efforts to build a simulation model for diamond power devices were started previously and there are number reports in literature [131, 23, 24], only brief details on the models will be provided in the frame of this thesis. Interested readers could find more physical insights of the simulation models in the corresponding references [131, 23, 24].

The 2D simulation configuration is shown in Fig. 3.11. We introduced the parameters that are identical with experiment for the purpose of reproducing the experimental structure. A diamond epilayer with the doping concentration of 2×10^{17} cm^{-3}, compensation concentration of 10% and the thickness of 100 nm were introduced (i.e. sample #1). This epilayer thickness is introduced by subtracting the p-n junction depletion width. Structure dimension with $L_{GS} = 4$ μm, $L_G = 4$ μm and $L_{GD} = 3$ μm were used for the simulation, but a larger numerical design of experiments has been simulated (different L_{GS}, L_G, L_{GD}, oxide thickness, doping and thickness of drift region, temperature, metal work function, ...). Gate metal work function was kept as Ni work function $W = 4.3$ eV. The substrate was considered as an oxide layer for the sake of minimizing the simulation

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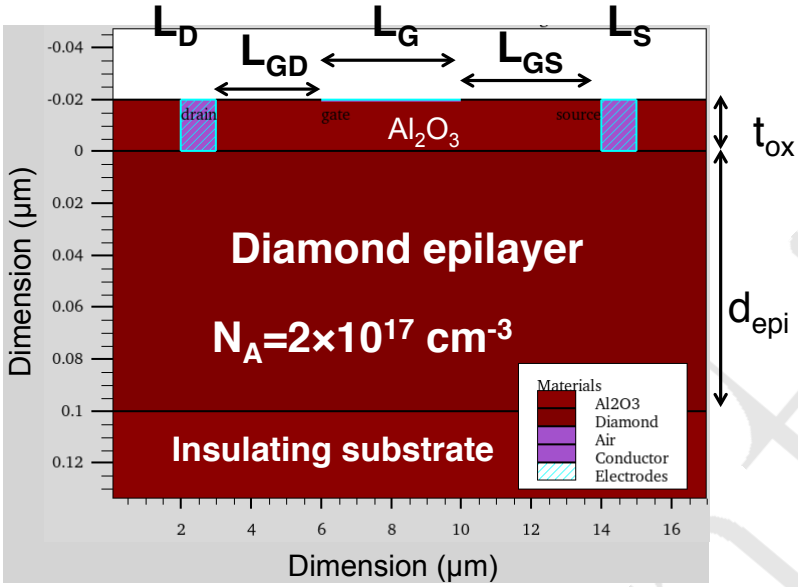

Figure 3.11: Silvaco simulation configuration with diamond epilayer thickness of 100 nm and doping concentration of $2\times10^{17}cm^{-3}$, oxide thickness of 20 nm, $L_{GS} = 4\mu m$, $L_G = 4\mu m$, $L_{GD} = 3\mu m$, $L_D = 1\mu m, L_S = 1\mu m$. Substrate were considered as an insulator to minimize the simulation time constant.

time. The dimensions of the source and drain contact were minimized as $L_D = 1$ μm, $L_S = 1$ μm. In principle, this approximation will not affect the simulation results since the current path is almost localized at the edge of the contact toward the channel. The thickness of the oxide layer is $t_{ox} = 20$ nm. Neither oxide charge nor interface states was implemented in this first simulation. Temperature for the simulation was kept at Room Temperature (RT) as $T = 300$ K but has been increased up to 550 K. The gate width in this simulation is 50 μm.

In fact, in the simulation, the temperature can be swept to reproduce the experimental condition. Also, the impact ionization coefficient [29][132] can be introduced [24] to predict or reproduce the breakdown voltage dependent on avalanche mechanism.

3.3 Results and Discussion

Hereinafter, we will present the results of test devices and the diamond transistors obtained, with a special focus on sample #1.

3.3.1 Test devices

3.3.1.1 MOS capacitors

In order to obtain the insight of the diamond transistors, test device MOS capacitors are fabricated on the same substrate. Figure 3.12 represents the optical photograph of an area in sample #1 where the MOS capacitors and MOSFET are exposed. Test device MOS capacitors were fabricated by employing the structure that was introduced by Chicot et al. [18]. Round shape MOS capacitors with the diameters of 100 μm and 60 μm are

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surrounded by the ohmic contact (lateral distance between ohmic and MOS capacitor is fixed to 4 μm). The following results were obtained from the MOS capacitor with a 100 μm diameter. A remarkable difference compared to our previous test device MOS capacitor is the absence of metallic p+ layer. Consequently, as discussed in chapter 2, the series resistance is expected to be much higher compared to the pseudo-vertical MOS capacitors (chapter 2).

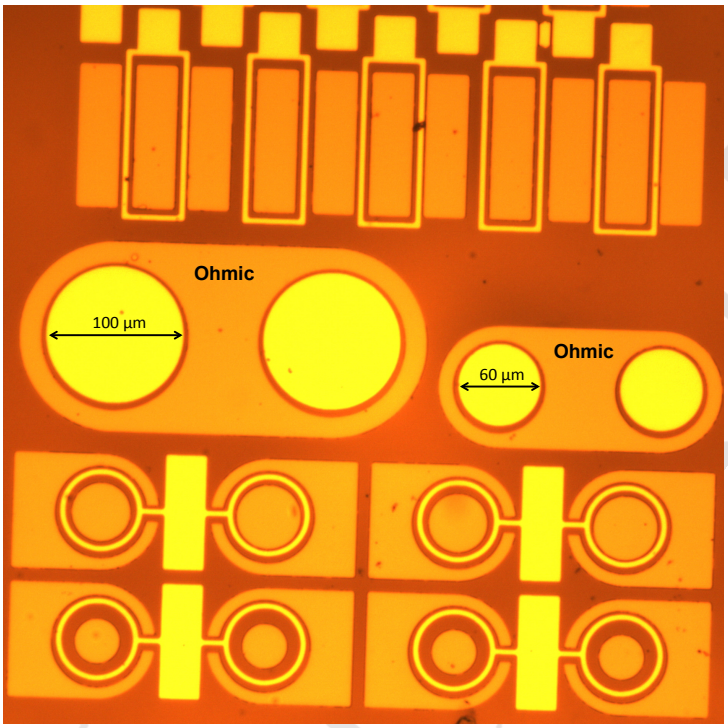

Figure 3.12: Top view of MOS capacitor structures captured by optical microscope.

Due to the high resistance issue, the C-V measurement is not trivial. In order to perform a proper C-V measurement and eliminate series resistance effect, an appropriate frequency is necessary. We performed Capacitance-frequency (C-f) measurement with a fixed gate bias ($V_G = -3\ V$) to determine the appropriate frequency range. Figure 3.13b represents the C-f curve of a MOS capacitor test device. From the C-f curve, we can see that the artifacts like leakage current (Fig. 3.13a), interface states and series resistance strongly affect the capacitance measurement, as discussed in chapter 2. The C-f curve also indicate that C-V measurements are necessary to be measured at the frequency range of few hundreds hertz.

Figure 3.13c represents the C-V curve measured at three different frequencies ($f = 300$ Hz, 400 Hz, 500 Hz). The C-V behavior is almost identical with the C-V curve obtained from the MOS capacitor with the p+ layer. Fermi Level Pinning (FPE) effect is observed in negative bias regime at high leakage current. Capacitance-frequency dependent effect is also observed. In positive bias, the SCR extension is clearly obtained. It is remarkable that the capacitance value is significantly decreasing for $V_G \geq +4.3$ V. Then, the capacitance is completely saturated at a very low value for $V_G \geq +7$ V. This is an indication of the collapse of two SCRs where the effective area of the capacitor is greatly reduced. The transition is perhaps due to the non-homogenous charge distribution in the oxide region. As we will show in the next part, this C-V curve is consistent with the pinch-off current

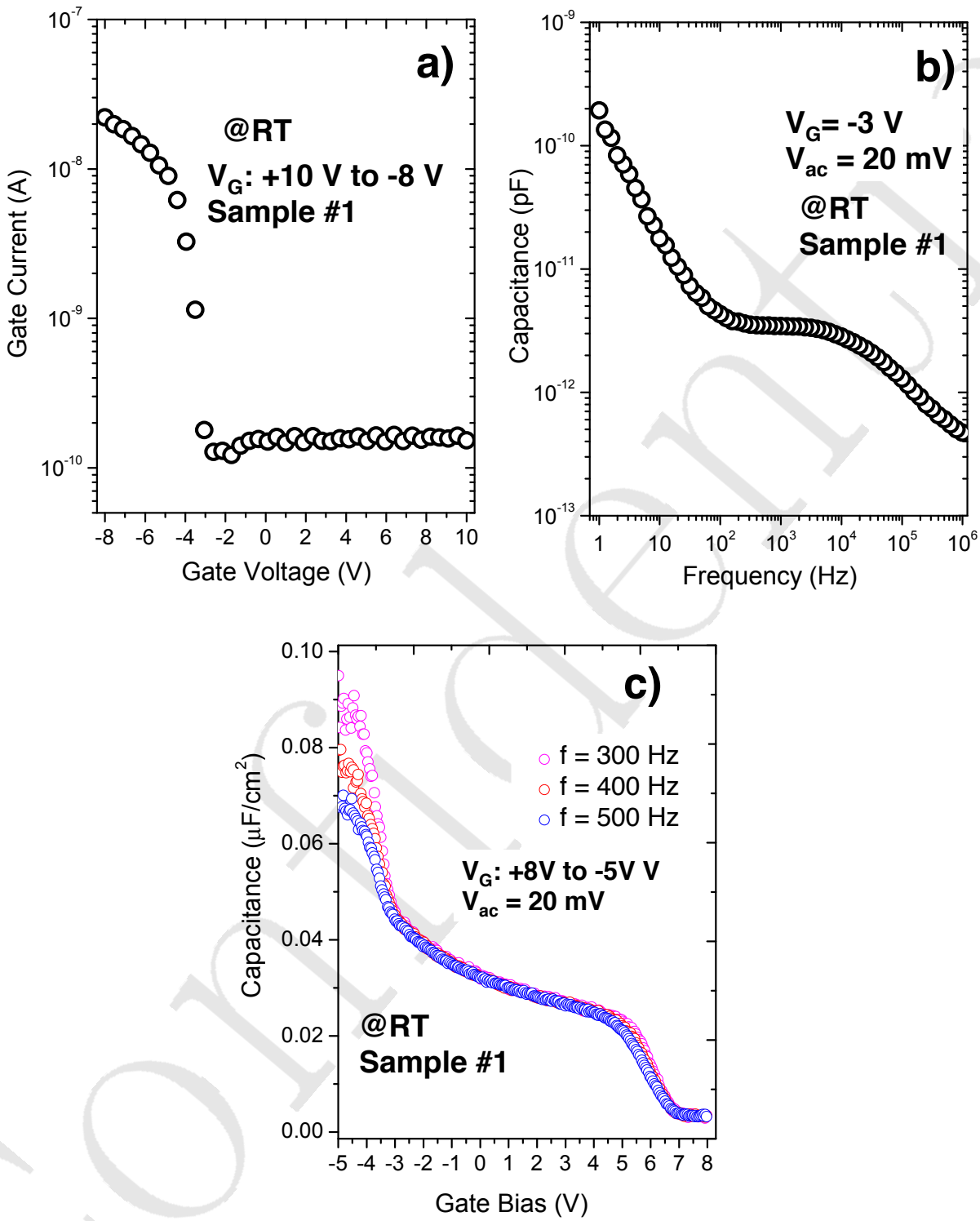

Figure 3.13: Electrical characteristics of MOS capacitor test devices on the diamond transistor sample: a) Current-Voltage characteristic; b) Capacitance-frequency characteristic at $V_G = -3\ V$; Capacitance-Voltage characteristics measured at different frequency. (Sample #1 - @RT).

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in DC electrical characteristic of the diamond depletion MOSFET.

Inverse square capacitance ($1/C^2$) is plotted against V_G in Fig. 3.14 to extract the doping concentration from the relationship:

$$N_A - N_D = \frac{-2}{\varepsilon\varepsilon_0 A^2}\frac{1}{dC^2/dV} \tag{3.2}$$

where $\frac{1}{dC^2/dV}$ is the slope from linear fitting of $\frac{1}{C^2} - V_G$ curve in Fig. 3.14.

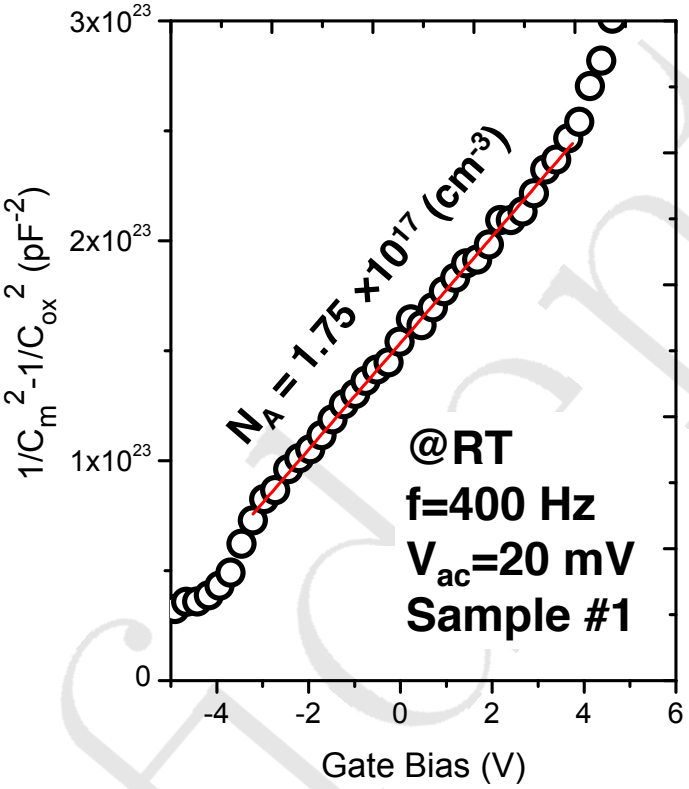

Figure 3.14: Reciprocal square capacitance plotted with gate bias to extract effective doping concentration (sample #1 at RT).

The linear fitting curve in Fig. 3.14 shows that there is an almost linear curve for the gate bias ranging from $-3\ V < V_G < +4.3\ V$. A doping concentration of approximately $1.75 \times 10^{17}\ cm^{-3}$ is extracted by using the slope in this range. This extracted doping concentration is close to the boron-doping concentration targeted during the diamond growth.

By employing the technique we have introduced in the Chapter 2, the expansion of the SCR with gate bias is also evaluated. First of all, we evaluate the variation of semiconductor surface potential Ψ_S with gate bias V_G, as shown in Fig. 3.15a. The corresponding SCR variation with gate bias is shown in Fig. 3.15b. Oxide capacitance is assumed to be $C_{ox} \simeq \frac{\varepsilon_{ox}\varepsilon_0}{t_{ox}}$ with $\varepsilon_{ox} \simeq 9$ oxide dielectric constant and $t_{ox} = 20$ nm oxide thickness.

From Fig. 3.15b, a SCR width of approximately 190 nm at $V_G \simeq +4.5\ V$ is deduced. From this SCR width, we can deduced that a sacrificed epilayer thickness of $h \simeq 40nm$ is initially depleted at the p-n junction of epilayer-substrate interface. The substrate is probably less N-doped than the assumed value ($N_D \simeq 3 \times 10^{19}$ cm^{-3}).

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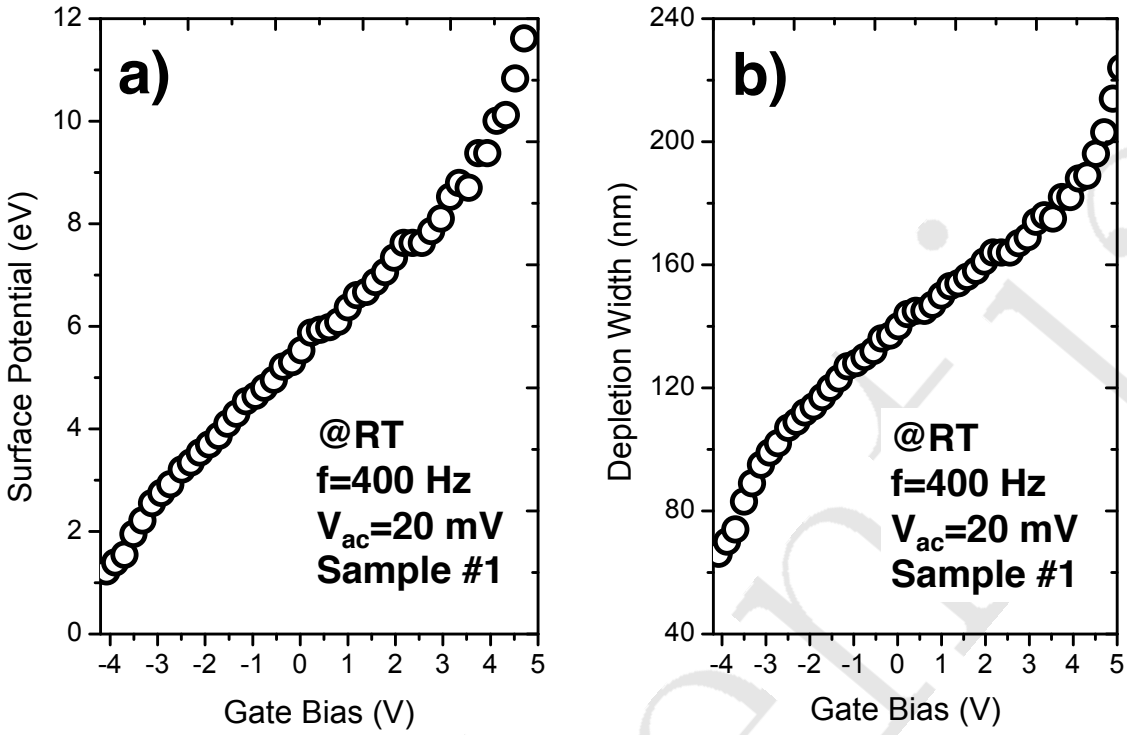

Figure 3.15: a) Surface potential variation with metal gate bias; b) Corresponding depletion width variation with gate bias.

For an efficient transistor, along with the effectiveness SCR width modulation, ohmic contact is also very important. In order to evaluate the contact resistance, we introduced the Transmission Line Model (TLM) test device.

As in any semiconductor electronic devices, ohmic contact is very important to maximize ON-state current. TLM is fabricated to examine the ohmic behavior of the contacts and also the sheet resistance of epilayer.

3.3.1.2 Transmission Line Model (TLM)

First, we will briefly discuss the working principle of TLM. TLM is an array of electrode pads that have an identical size with different spacing between the pads, while controlling the current spread between the contacts. The measured resistance between two electrode pads is the summation of two contact resistances and sheet resistance. R_T can be calculated as:

$$R_T = 2R_C + R_S \frac{L}{W} \tag{3.3}$$

where L is the distance between two electrodes, W is the width of the electrodes, R_C is the contact resistance and R_S is the semiconductor sheet resistance. Assuming the contact resistance and sheet resistance are homogeneous over the sample size, the measured resistance is then a function of L. Therefore, in order to obtain the contact resistance and sheet resistance, the measured resistances are plotted against L. A proper measurement should give a linear curve where the slope is corresponding to $\frac{R_S}{W}$ and the intercept to y-axis yield to the corresponding $2R_C$.

Figure 3.16 represents a typical conceptual structure of the TLM. In the current work, TLM are the multiple electrode pads of Ti/Pt/Au with width of W=150 μm and spacing between pads L of 10 μm, 25 μm, 50 μm, 75 μm, 100 μm and 150 μm.

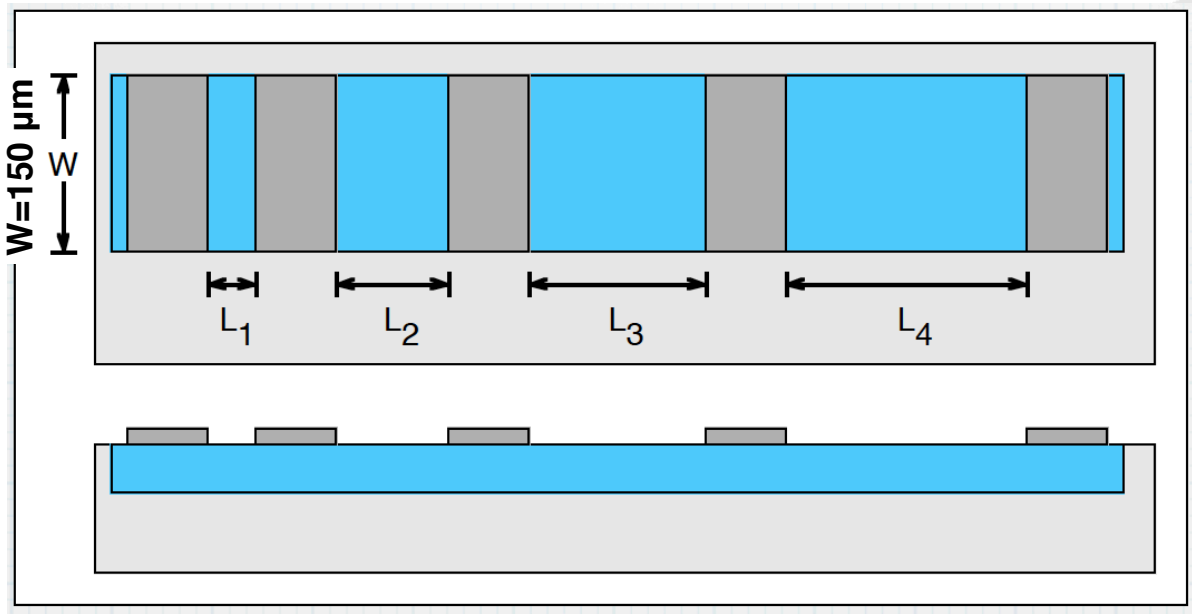

Figure 3.16: Conceptual description of the TLM test device.

For an accurate contact resistance measurement, mesa etching is required [129]. However, in the first approach, we tuned the fabrication processes to quickly demonstrate a first proof of concept for depletion mode diamond MOSFET. Therefore, for the sake of simplicity in the fabrication, mesa etching was not performed in the current study, as this step was not necessary for the first designs of diamond transistors. The lack of mesa etching step played a relatively important role on TLM electrical characteristics. For instance and for the pads with a short spacing ($L < 75\ \mu m$), the measured resistance is strongly deviated and the obtained value are usually unreasonable. This can be explained as current spreading is not evenly distributed ($W >> L$), and a significant part of the current flow is not perpendicular to the LTM contacts. Fortunately, the pads with a long spacing ($L \geq 75\ \mu m$), the TLM is worth of interest. The measured resistance is consistent with the pads spacing.

Figure 3.17a represents the I-V characteristics at RT of three TLM at different spacings: $L = 75\ \mu$m, 100 μm and 150 μm, respectively. The ohmic contact behavior of the contacts was not obtained. Regarding the origin of non-ideal ohmic behavior, it is important to refer to the comprehensive discussion by Tachibana et al. [133]. The ohmic contact is actually formed thanks to a defective region at the interface between diamond and metal electrode, which is mediating the carriers tunneling between metal and diamond. Therefore, the non-ideal ohmic contact is likely indicating a good quality of diamond at the interface. Also, there is a barrier of approximately 0.5 eV between TiC/diamond [133], which is possibly responsible for the non-ideal ohmic contact. The non-ideal ohmic contact will definitely affect the device performance, as we will show in the following parts. Therefore, it is very important to improve the ohmic contact in the upcoming approaches.

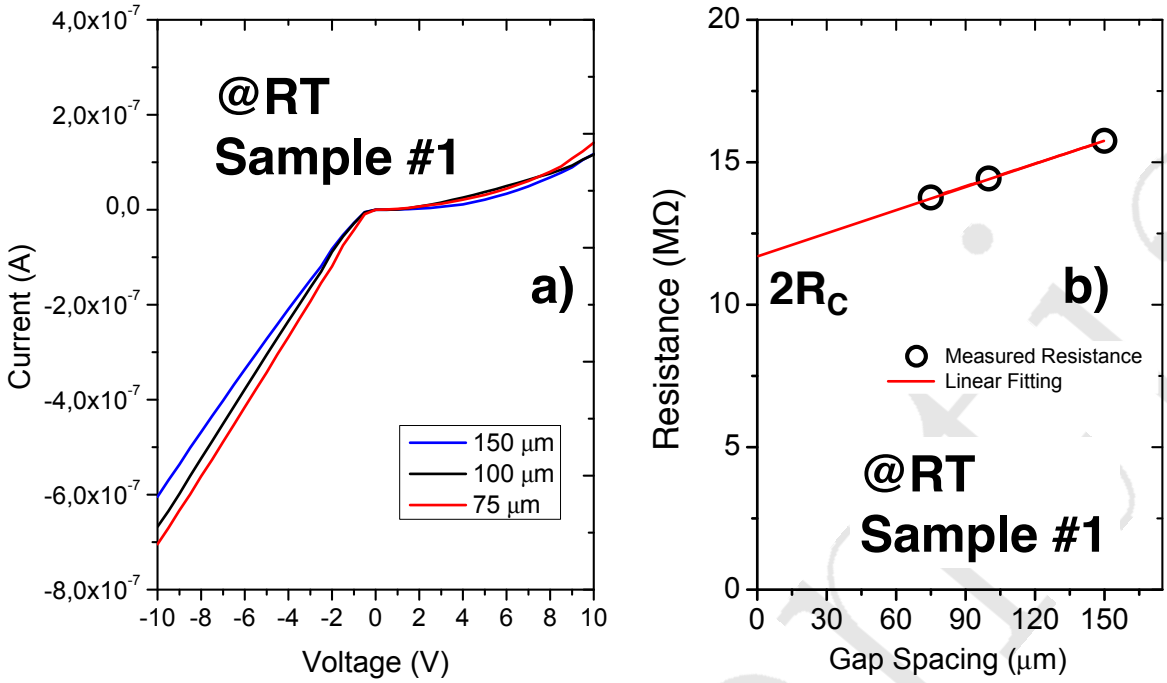

Figure 3.17: a) Typical IV characteristics of the Ohmic contact after annealing at 600°C; b) Measured resistance as function of electrode spacing with linear fitting to extract sheet resistance and contact resistance

From I-V characteristics in Fig. 3.17a), the measured resistance is evaluated by the derivation $\frac{dV}{dI}$ and followed by an averaging of the derivative over negative bias direction. Figure 3.17b) represents the measured total resistance with three pads spacing of L=75 μm, 100 μm and 150 μm, respectively. The linear fitting of the total resistance as a function of the gaps gave a straight line with the slope of 26.4 kΩ/μm and an intercept with y-axis at 11.7 MΩ.

A corresponding sheet resistance of approximately $R_{Sheet} \simeq 4$ M$\Omega/\square$ has been evaluated. From sheet resistance, the resistivity of our sample is consequently being evaluated by using the effective epilayer thickness of $t \simeq 190$ nm that was evaluated from MOS capacitance measurement on the same sample (Fig.3.15). From the relationship $\rho = R_{Sheet} \times t$, a resistivity of $\rho \simeq 75$ $\Omega.cm$ was obtained.

A recent theoretical calculation from Traore et al. [10] based on the neutrality equation taking into account the main scattering mechanisms in boron doped diamond [11] has pointed out the relationship between boron doping concentration N_A, compensation concentration N_D and resistivity ρ at different boron doping concentration. The region corresponding to the doping concentration ($N_A = 1.75 \times 10^{17}$ cm^{-3} extracted from MOS capacitor measurement - Fig. 3.14) and the resistivity ($\rho \simeq 75\Omega.cm$ evaluated from TLM measurement- Fig. 3.17) is the transition from yellow to green region (Fig. 3.18). This region is corresponding to a compensation concentration of around $5\times10^{15} cm^{-3} \leq N_D \leq 2 \times 10^{16}$ cm^{-3} (Fig. 3.18). This $\lesssim$10% compensation is consistent with the previous reports by fitting the Hall measurements by Volpe et al. [6]

From the relationship between doping concentration, resistivity and compensation concentration, we can project the hole concentration thanks to the exhaustive analysis

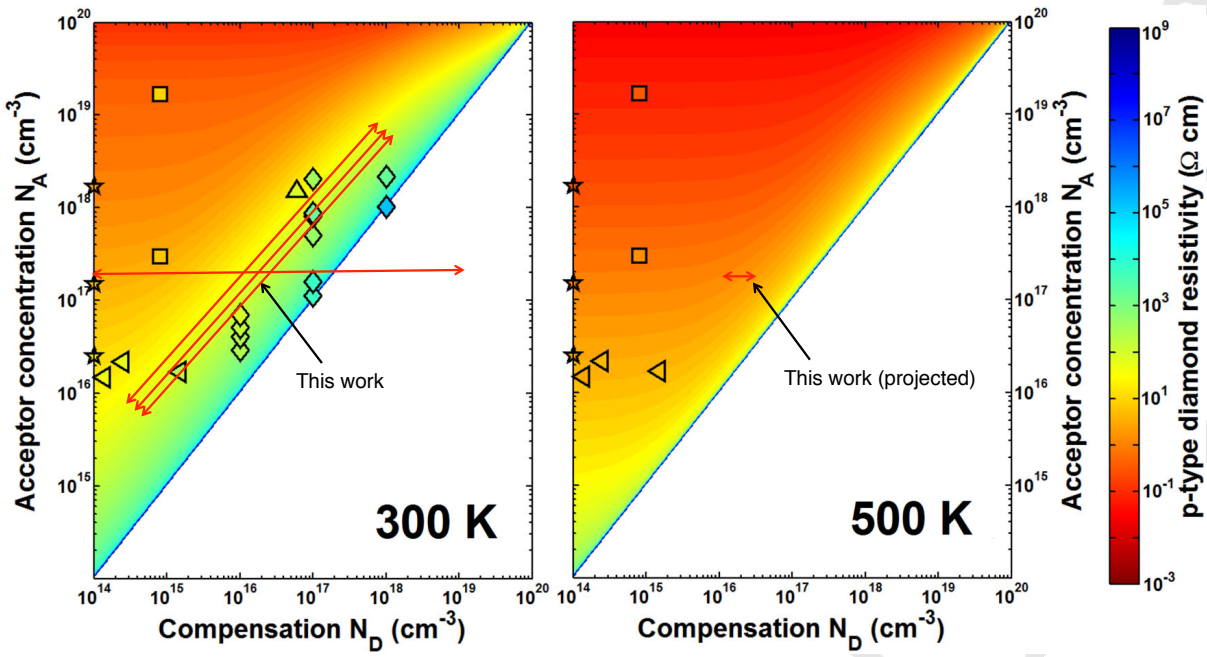

Figure 3.18: The relationship between compensation concentration N_D and resistivity of boron doped diamond at different dopant concentration N_A. Courtesy to Traore et al. [10]

given by Traore et al. [10]. As shown in Fig. 3.19, for the range of resistivity measured by TLM test devices, the hole concentration can be ranging from 3×10^{13} (cm^{-3}) for the highly compensated sample to 2×10^{14} (cm^{-3}) for the slightly compensated sample.

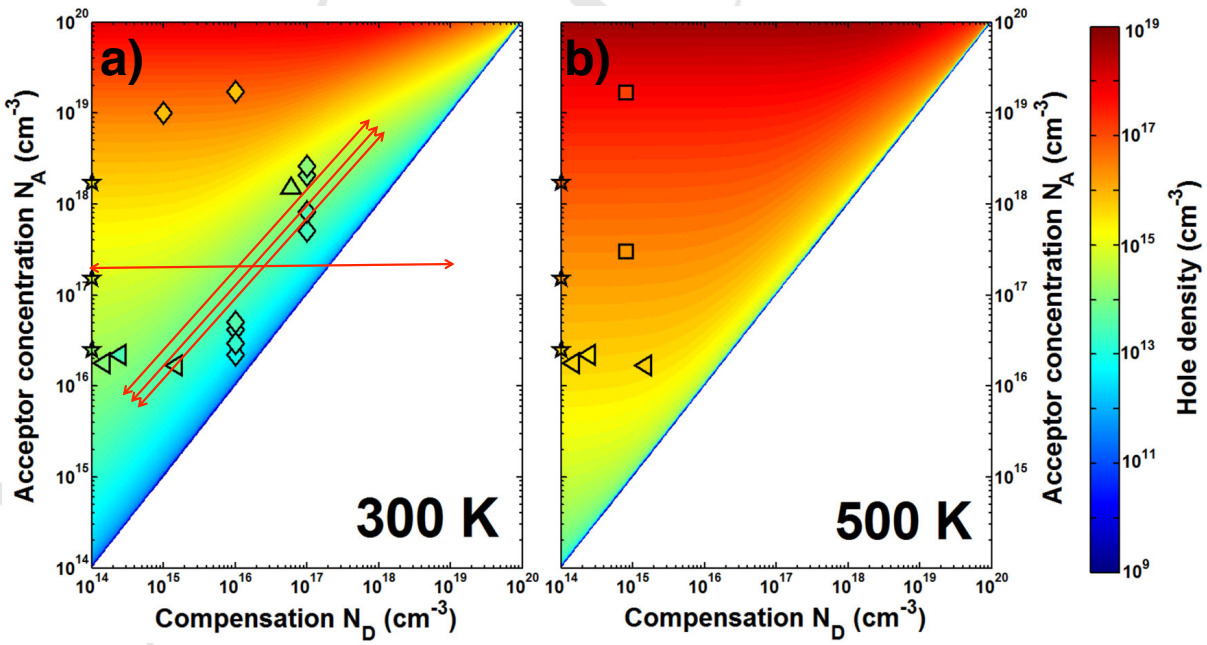

Figure 3.19: The relationship between compensation concentration N_D and hole concentration of boron doped diamond at different dopant concentration N_A. Courtesy to Traore et al. [10]

By increase the temperature to 500 K for the same condition of doping concentration

and compensation concentration, resistivity is projected to be decreased more than 10 times, as shown in Fig. 3.18.

From the interception of fitting curve with y-axis, contacts resistance $2R_c \simeq 11\,(M\Omega)$ has been determined for the TLM with the width W=150 μm. A normalized contact resistance $2R_c.W = 175$ k$\Omega.cm$ is obtained. This normalization has been employed since the 2D simulation has shown that all the carriers are being collected at the boundary of the contact pads toward the another one (will be shown in Fig. 3.23b).

3.3.2 Transistor Performance

Figure 3.20 represents the FESEM image of the fabricated transistors under measurement configuration. Figure 3.20a represents the stripe structure transistor. The ON-state current that will be presented below is measured from this device. The specific dimensions of this transistor are: W=34μm, L_{DS}=10μm, L_G=3μm, L_{GS}=4μm and L_{GD}=3μm.

Figure 3.20b represents the FESEM image of the circular transistor, from which the OFF-state performance will be presented. The specific dimensions of this transistor are: L_G=4μm, L_{GS}=4μm and L_{GD}=10μm. From both transistors, the dimensions are the designed values (mask), and do not take into account possible misalignments and process variations.

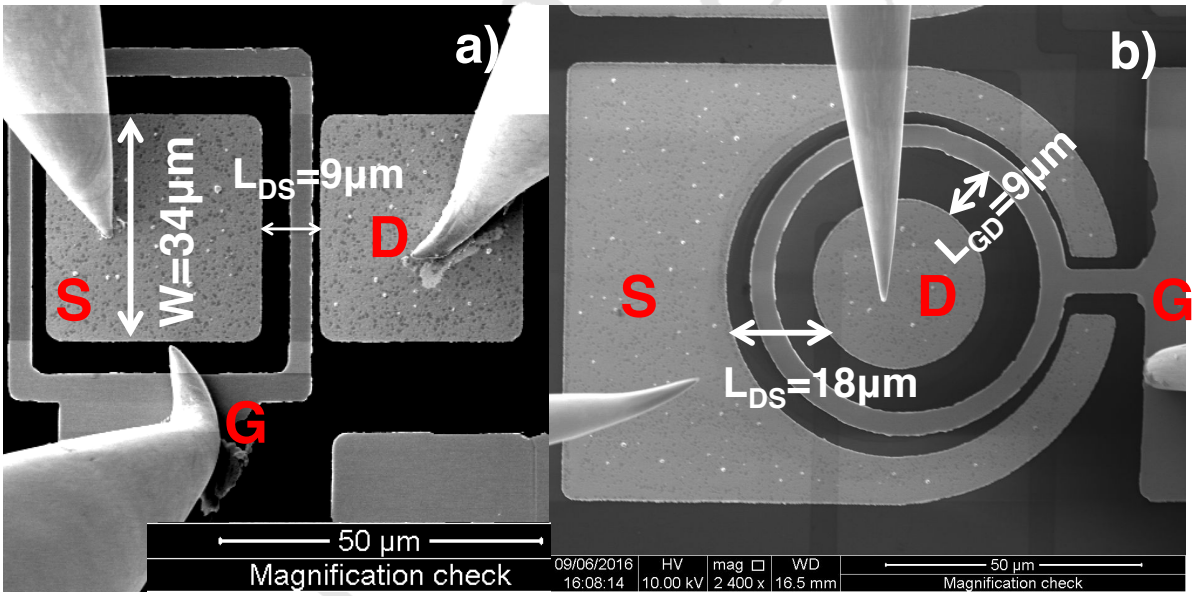

Figure 3.20: FESEM image of the boron doped diamond MOSFET. a) Stripe structure MOSFET target high ON-state current; b) Circular structure target high OFF-state breakdown voltage. Device dimension parameters were taken from mask design. Measurements have been performed at RT in the vacuum chamber of FESEM system.

3.3.2.1 ON-State

Transistor transfer characteristics I_{DS} were measured by sweeping V_{DS} from 0 V to -10 V at different fixed V_{GS}, ranging from -5 V to $+10$ V.

Figure 3.21 represents the transfer characteristic of the stripe structure transistor. The transfer characteristic clearly shows three typical regimes of a proper transistor: linear

regime, saturation regime and pinch-off regime. The diamond transistor is normally-ON since $I_{DS} \neq 0$ at $V_{GS} = 0$ V and $V_{SD} > 0$ V. A maximum ON-state saturation current of around $1,9$ μA/mm is measured at RT. This ON-state saturation current at RT is comparable with the diamond MESFET reported by Umezawa [16]. However, this ON-state current is much lower than the reports from H-diamond MOSFET [76][21] and inversion diamond MOSFET [14]. One of the problems with this transistor is the non-ideal ohmic contact which is highly limiting the ON-state current. Also, since the FLPE prevents diamond from reaching the accumulation regime, the ON-state current is partially limited. Last but not least is the contribution from incomplete ionization of boron doped acceptor at RT due to the deep ionization boron doped level. A projected ON-state current of few 10 times higher is expected for device working at the high temperature (500 K), assuming contact resistance is not changing by increasing the temperature.

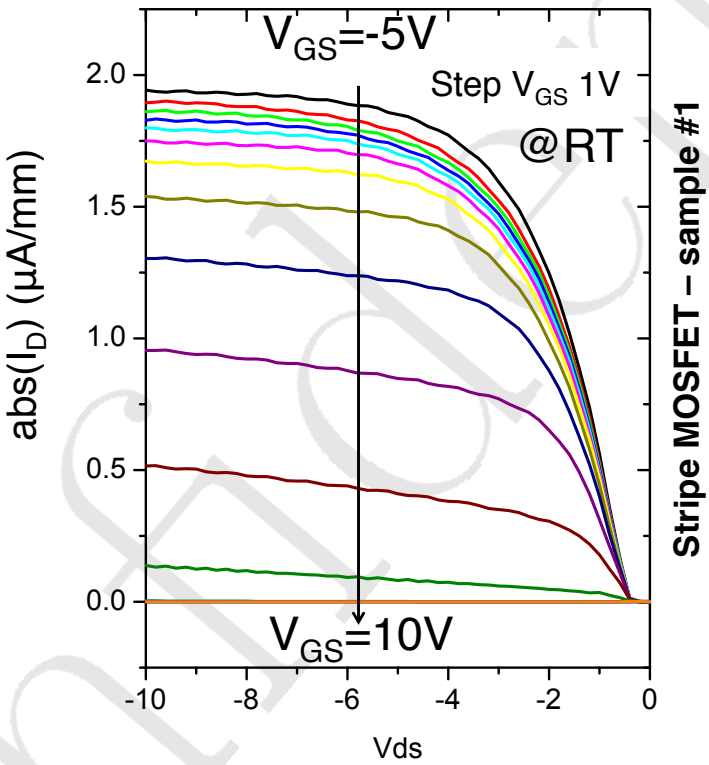

Figure 3.21: Transfer characteristics of the stripe transistor -sample #1 measured by sweeping V_{DS} from 0V to -10V at different fixed gate biasV_{GS} (V_{DS}: -5V to 10 V, step V_{GS} : 1V). The measurements have been performed at RT in the vacuum chamber of FESEM system.

The Gate to Source leakage current (I_{GS}) is under the detection limited for the whole V_{GS} range of measurements in this device, as shown in Fig. 3.22b. This negligible gate leakage current demonstrates that this MOSFET is a complete electrostatics gate controlled transistor with an insulated gate.

In the OFF-state, the Drain leakage current is below the apparatus detection limit for a $V_{GS} \geq 7$ V. The channel is completely pinched off. This behavior is in agreement with the C-V characteristics of the test device MOS capacitor that we have shown in Fig.

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3.13. It is a clear evidence that the two SCRs were collapsed.

In order to obtain the transconductance of the device, we measured the transfer characteristics of the transistor by varying V_{GS} at a fixed V_{DS}, at RT. At a fixed V_{DS}=-10 V, the measured I_{DS} as a function of V_{GS} and the corresponding transconductance are shown in Fig. 3.22. An ON/OFF ratio of approximately 10^5 was obtained, as shown in Fig. 3.22a, acknowledging an OFF state leakage current below detection limit (reduced W of the transistor).

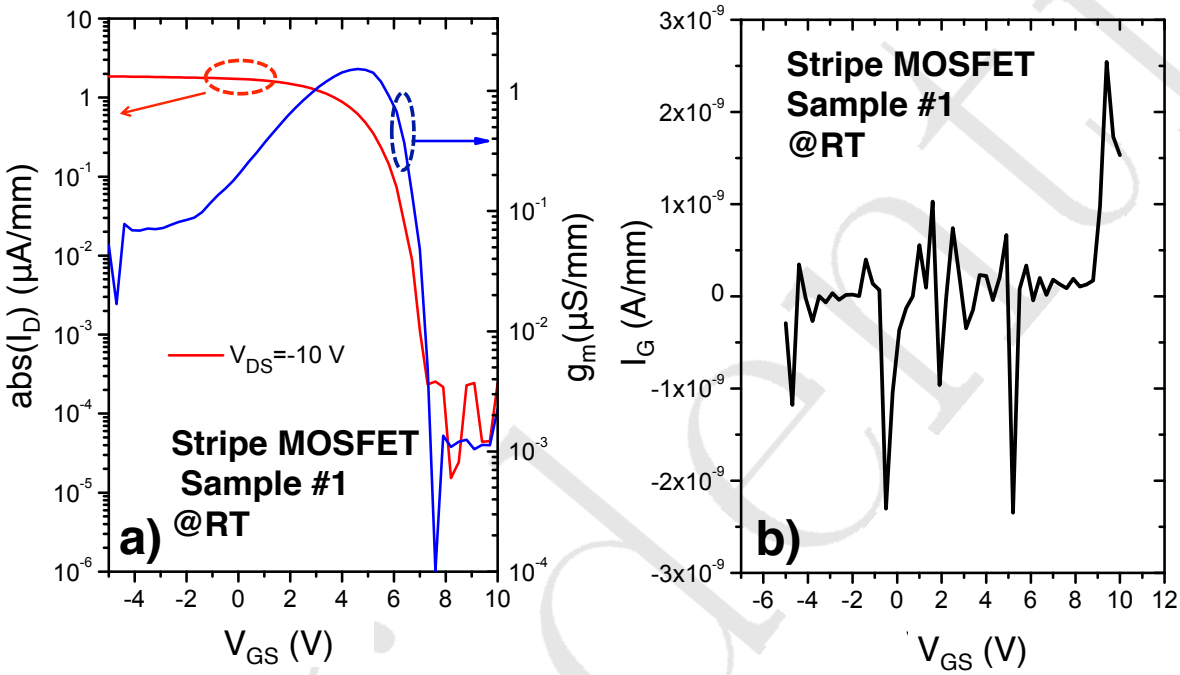

Figure 3.22: a) Transfer characteristics of the stripe transistor -sample #1 measured by sweeping V_{GS} from +10V to -5V at a fixed V_{DS} (V_{DS}=-10V) ; b) Gate leakage current I_{GS} measured instantaneously with transfer I_D. The measurement have been performed at RT in the vacuum chamber of FESEM system.

Electrical measurements demonstrated that the device is a complete electrostatics gate controlled transistor. In order to understand the physics involved in our devices, it is important to visualize electrostatic parameters like potential distribution, electric field distribution and hole concentration distribution. The 2D Silvaco Atlas finite element based simulation tool is an ideal solution to access the electrostatics profile inside the device.

Hereinafter, we will present the electrostatics profile of the device with the simulation parameters introduced in Fig. 3.11. For the ON-state simulation, V_{SD} is kept as low as possible ($V_{SD} = 1$ V in this case) to minimize the potential perturbation under the gate region.

The potential distributions at three different gate bias ($V_{GS} = -5V$, $0V$, $6V$) are shown in Fig. 3.23a-c), respectively.

The corresponding electric field distribution at three different corresponding gate bias ($V_{GS} = -5V$, $0V$, $6V$) are shown in Fig. 3.23 d-f), respectively.

The corresponding hole distribution at three different gate bias ($V_{GS} = -5V$, $0V$, $6V$) are shown in Fig. 3.24 a-c), respectively.

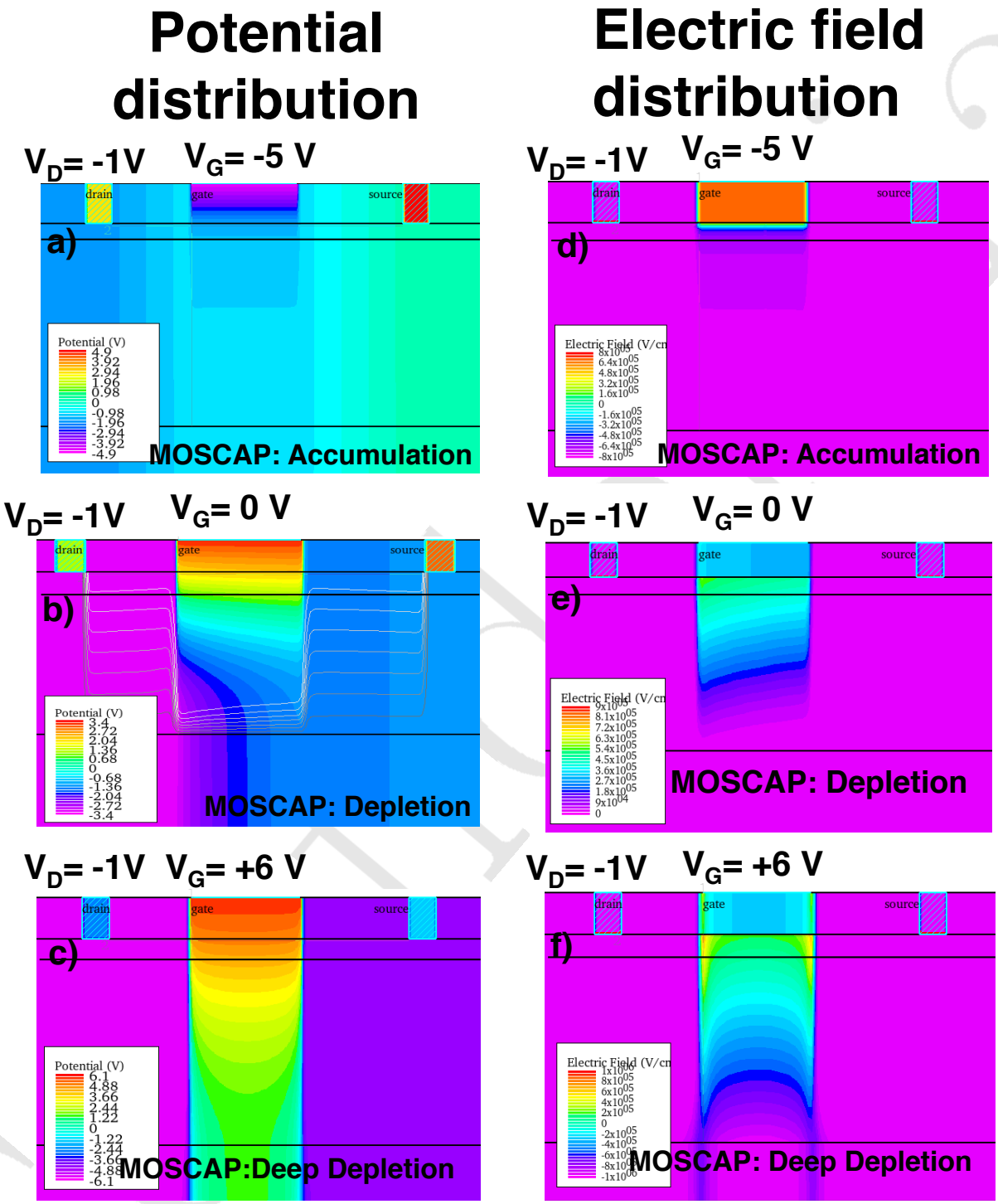

Figure 3.23: Silvaco Atlas simulation the potential distribution at different gate bias a) V_{GS}=-5 V ; b) V_{GS}=0 V; c) V_{GS}=6 V; and electric field distribution at three different gate bias: a) V_{GS}=-5 V ; b) V_{GS}=0 V; c) V_{GS}=6 V. Simulation configuration were presented in Fig. 3.11 and temperature is assumed at RT.

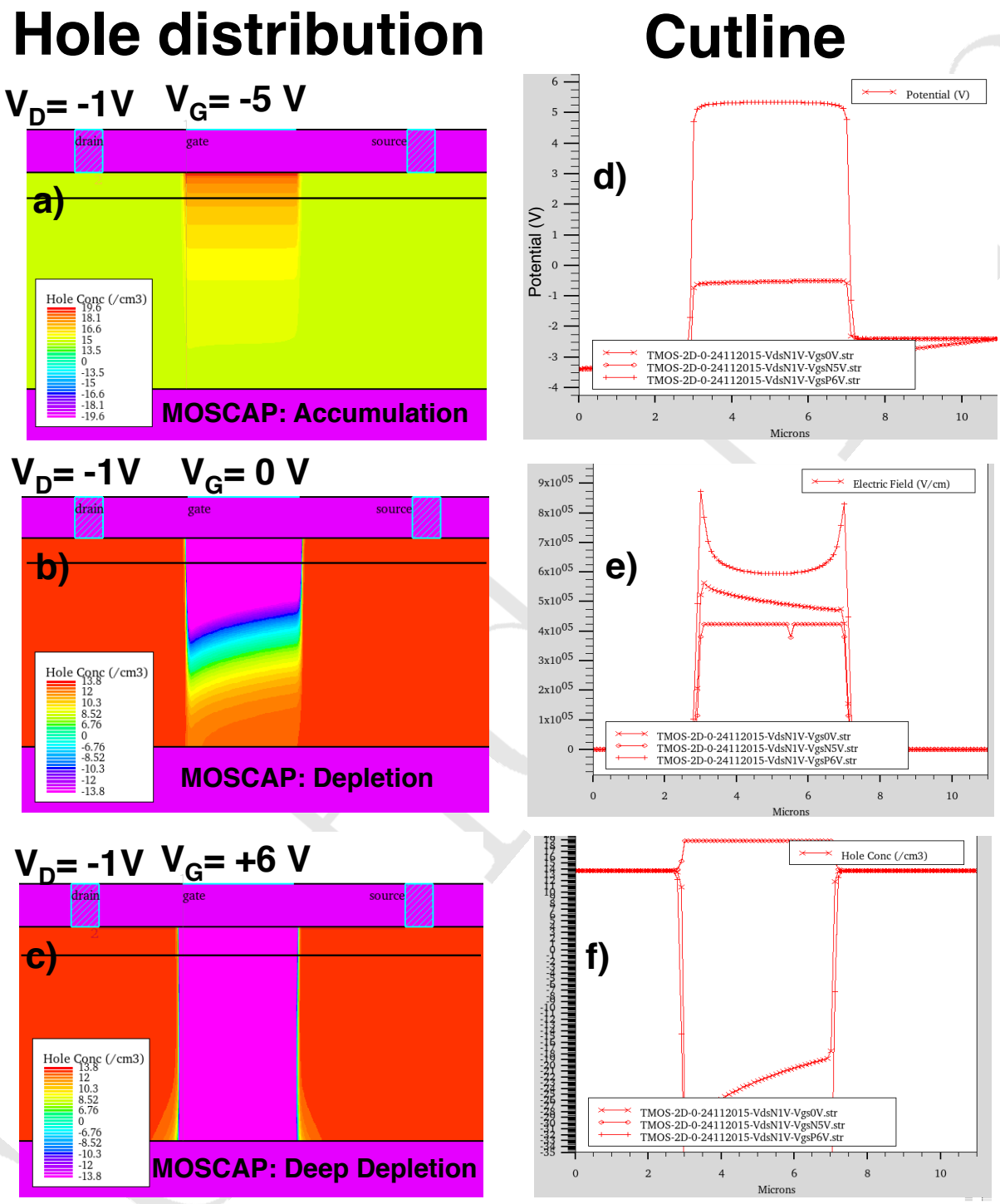

Figure 3.24: Silvaco Atlas simulation of the hole distribution at different gate bias a) V_{GS}=-5 V ; b) V_{GS}=0 V; c) V_{GS}=6 V; Cutline of the d) potential distribution; e) electric field distribution; f) hole distribution. Simulation configuration were presented in Fig. 3.11 and temperature is assumed at RT.

Figure 3.24d represents the cutline potential distribution, which is corresponding to the potential distribution in Fig. 3.23a-c). Figure 3.24e represents the cutline electric field distribution, which is corresponding to the electric field distribution in Fig. 3.23d-f). Figure 3.24e represents the cutline hole distribution, which is corresponding to the hole distribution in Fig. 3.24a-c).

The simulation results are relatively coherent with the experimental results. At V_{GS}=0 V, a part of the epilayer is depleted due to metal-semiconductor work function difference. However, since the oxide charge was not included, the quantitative agreement was not reached. At high negative gate bias V_{GS}=-5 V, the hole accumulation underneath the gate is observed. As shown from the analysis in Part 1, Chapter 2 as well as the C-V measurement on the MOS capacitor test device on this sample, this accumulation is not obtained in experiment due to FLPE. In this simulation, interface states and gate oxide leakage current were not implemented. Therefore, in order to have a better agreement between simulation results and experiment results, it is important to either eliminate interface states and/or leakage current in the experiments or include interface states and gate oxide leakage into the simulation models.

Regarding the current path, from the simulation we can observe that most of the ON state current is collected at the boundary of the source and drain contacts toward the gate, as shown in Fig. 3.23 b. The simulated transfer characteristics (I_{DS} at a fixed V_{SD} with V_{GS} varying) is represented in linear scale and logarithm scale in Fig: 3.25. The ON-state current in the simulation results is considerably higher than the experiment results, since perfect ohmic contact have been set in the simulation ($R_{contact} = 0\ \Omega$).

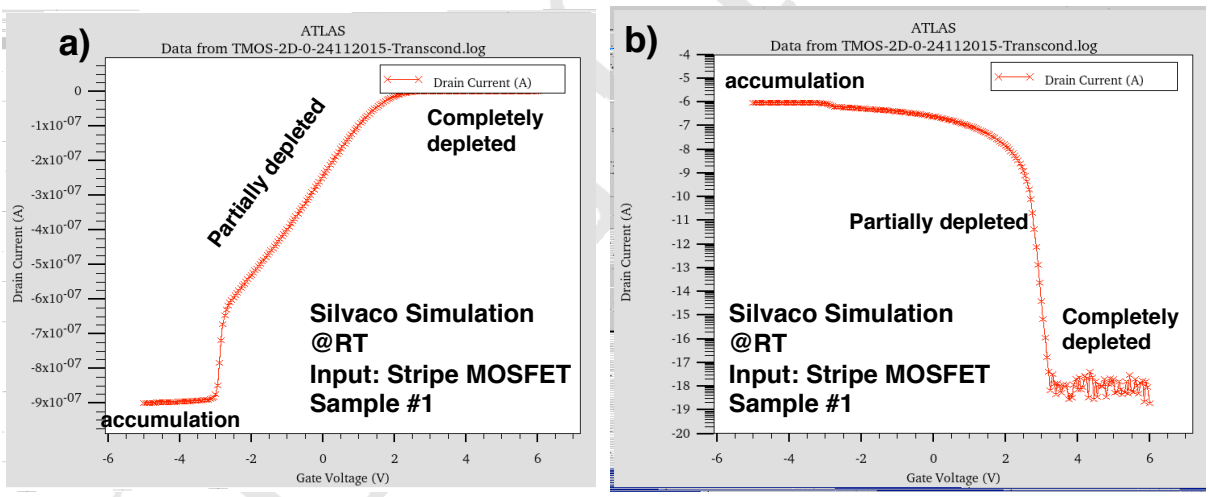

Figure 3.25: Silvaco simulation of drain current (I_D) for $V_{DS} = -1V$ at different gate bias (V_{GS} : $-5V$ to $+6$V) in a) linear scale; b) semilog scale. Simulation configuration is identical with the Fig. 3.11 and temperature is kept at RT.

One of the most interesting part in these simulations is the electrostatics distribution. As we can see from Fig. 3.23, and Fig. 3.24, fully depletion is observed for a gate bias of $V_{GS} = +6\ V$. Also, the extension of SCR width is almost localized under the gate region. We believe this effect is originated from the low V_{SD} value that were applied, together with a large L_G value (larger than the lateral Drain-Gate SCR). In the following section, we assume this effect is still valid for a small V_{SD} in the linear regime.

3.3.2.2 Transistor parameters

As we discussed in the first part of this chapter, a transistor is working like a resistor in the linear regime. It is therefore important to distinguish the linear-regime and the saturation regime to extract the parameters of the transistor. In the linear regime, the channel charge density is presumably substantial distributed along the channel [134]. Therefore, the charge transport is dominated by the drift phenomenon. There is no diffusion transport even at low V_{DS} since there is no p-n junction at the contact like in an inversion mode MOSFET [134]. Figure 3.26 represents the I_{DS} measurements with V_{GS} at different fixed V_{SD} values. From Fig. 3.21 and Fig. 3.26, the linear regime is determined for a low V_{DS} range of approximately V_{DS}=-0.4 V to V_{DS}=-2 V.

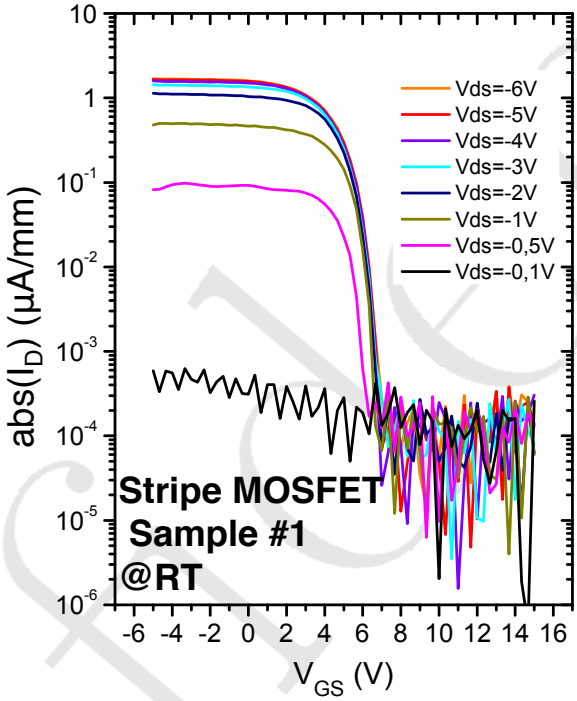

Figure 3.26: a) Transfer characteristics of the stripe transistor -sample #1 measured by sweeping V_{GS} from +14V to -5V at different fixed V_{DS} (V_{DS}: -0.1V to -6V). The measurement have been performed at RT in the vacuum chamber of FESEM system.

The channel conductance in the linear region is defined as the slope of $I_{DS} - V_{DS}$ in the Fig. 3.21 and can be evaluated by the derivation:

$$g_D = \frac{dI_{DS}}{dV_{DS}} \tag{3.4}$$

Inverse channel conductance is equivalent with the sum resistance between source and drain.

3.3.2.3 Contact resistance of the diamond MOSFET

Figure 3.27 represents the descriptive device structure and the equivalent resistance between source and drain. We employed the hypothesis that the current flowing between

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source and drain is parallel and constant. As we have refined our analysis in the linear region of the transistor where charge densisty is presumably substantial distributed along source to drain [134], this hypothesis is reasonable.

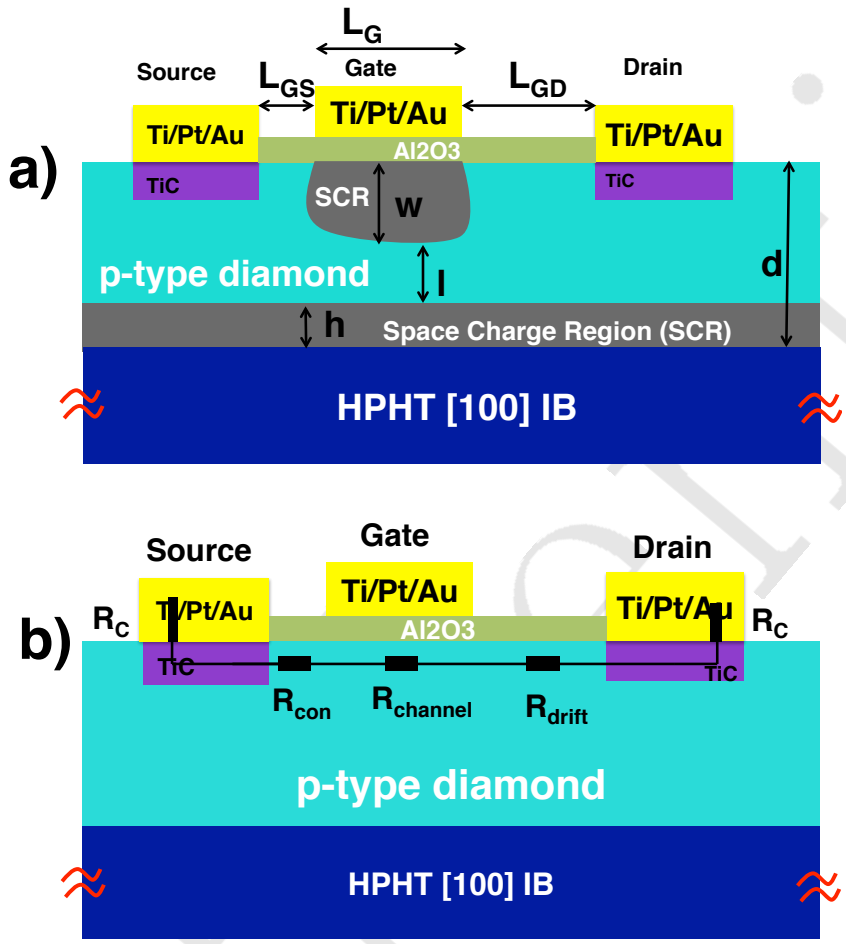

Figure 3.27: a) Descriptive cross-section of the depletion mode diamond MOSFET; b) Equivalent Source to Drain resistance of the MOSFET corresponding to the cross-section and non-negligible contact resistance.

From the equivalent resistance in Fig. 3.27b, the "source to drain resistance" can be expressed as:

$$1/g_D = R_{SD} = 2R_C + R_{con} + R_{channel} + R_{drift} \tag{3.5}$$

This expression is introduced since the gate to source leakage current (I_{GS} - Fig. 3.22b) is negligible. The $2R_C$ being the contact resistance of source and drain, which includes any contribution from the metal resistance and the metal-semiconductor interfaces. R_{con} is the resistance in the conduction region between source and gate. Considering the cross-section structure of the device in Fig. 3.26 and the top view structure in Fig. 3.6, R_{con} can be calculated by:

$$R_{con} = \rho \frac{L_{GS}}{W(d-h)} \tag{3.6}$$

With L_{GS} is the gate to source distance. R_{drift} is the resistance in the drift region between gate and drain. The current spreading is assumed to fill completely the epilayer

in the Gate to Source region (as suggested by the simulation from Fig. 23b), since L_{GS} >> epilayer thickness). For a low V_{SD} voltage in the linear regime, the R_{drift} is calculated by:

$$R_{drift} = \rho \frac{L_{GD}}{W\,(d-h)} \tag{3.7}$$

Where L_{GD} is the distance from gate to drain. The channel region is defined as the region under gate. The corresponding channel resistance is calculated as (hole distribution is neglected and carrier distribution is supposed constant within w):

$$R_{channel} = \rho \frac{L_G}{W\,(d-w-h)} \tag{3.8}$$

By using the resistivity that was extracted from TLM test device at RT, the R_{con} and R_{drift} can be calculated. Equation 3.5 can be then rearranged as:

$$R_{SD} - R_{con} - R_{drift} = 2R_C + R_{channel} \tag{3.9}$$

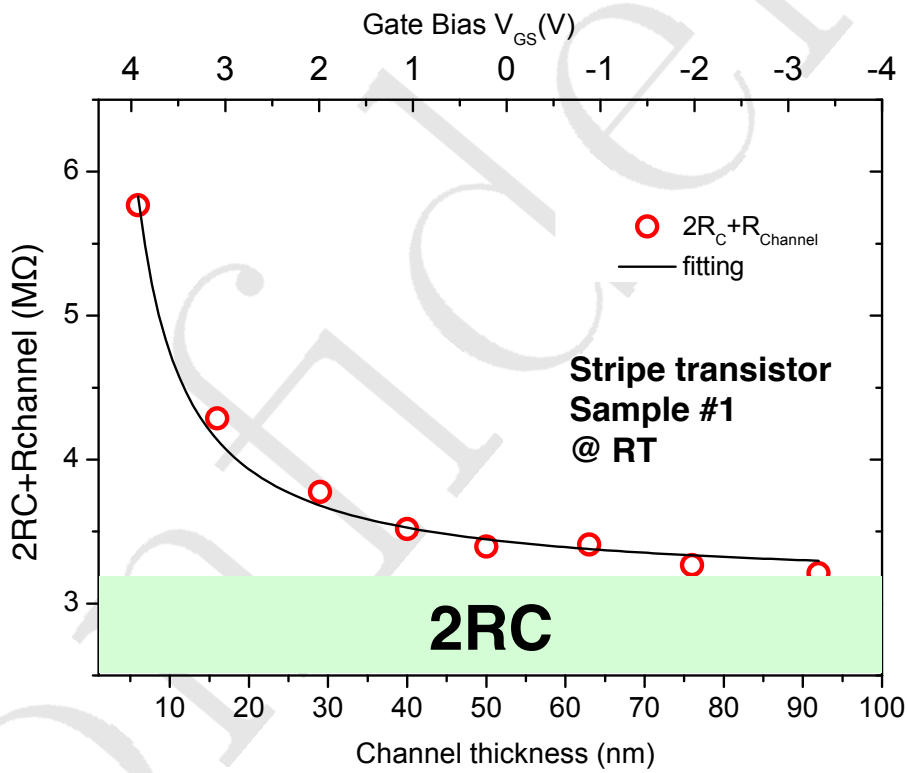

Figure 3.28: 2RC+Rchannel versus channel thickness (the width of neutral region under gate) at different V_{GS} (top x-axis).

As the parameters in the left side of the equation (R_{SD}, R_{con}, R_{drift}) were determined, the unknown parameters in the right side of the equation (R_C and $R_{channel}$) can be determined. By replacing $R_{channel}$ in equation 3.8 into equation 3.9, equation 3.9 can be rewritten as:

$$R_{SD} - R_{con} - R_{drift} = 2R_C + \rho \frac{L_G}{W} \frac{1}{(d-w-h)} = 2R_C + \rho \frac{L_G}{W} \frac{1}{x} \tag{3.10}$$

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where d, w, h are the thickness of epilayer, the SCR width at diamond/oxide interface and the SCR width at epilayer/substrate p-n junction, respectively. $x = (d - w - h)$ is the neutral region width between the 2 SCRs (see Fig. 3.26).

As one can see in equation 3.10, the right side of the equation is a function of $\frac{1}{x}$ and is limited by the $2R_C$. Therefore, in principle, the value of $2R_C$ can be found by plotting $R_{SD} - R_{GS} - R_{GD}$ against $\frac{1}{x}$. With x is the value measured by MOS capacitor test device, assuming the extension of SCR in the MOSFET is similar to the MOS capacitors. In fact, the correlation between transistor electrical characteristics and MOS capacitor behavior as well as 2D Silvaco Simulation have demonstrated this assumption is reasonable for the linear regime. Therefore, the variation of drain conductance in linear regime versus gate bias (I_{DS} vs. V_G - linear region, Fig. 3.21) is similar to a TLM test device. In this case, x (equation 3.10) is equivalent to L (equation 3.3).

Figure 3.28 represents the $R_{SD} - R_{GS} - R_{GD}$ plotted versus channel thickness (the width of neutral region under gate). By using equation 3.10 for fitting Fig. 3.28, contact resistance of $2R_C \simeq 31$ MΩ is determined. A normalized $2R_C W \simeq 110\ k\Omega.cm$ is obtained. This value is in agreement with the contact resistance evaluated by the TLM technique. This contact resistance is very high and highly hinders the carriers collection between source and drain. It is therefore very important to improve the contact resistance in the next fabrication run.

3.3.3 Mobility

The carriers mobility between source and drain can be evaluated after eliminating the contribution from contacts resistance 2RC. The intrinsic semiconductor resistance is obtained after eliminating the contribution of the contact resistance as:

$$R_{Semi} = R_{SD} - 2R_C \tag{3.11}$$

With R_{semi} is as defined as in Fig. 3.27, it can be calculated as:

$$R_{Semi} = \rho \left[\left(\frac{L_{GS} + L_{GD}}{t} \right) + \frac{L_G}{t - x} \right] \tag{3.12}$$

The carrier mobility under low field in semiconductor region can be evaluated as:

$$\mu = \frac{1}{qpR_{Semi}W} \left[\left(\frac{L_{GS} + L_{GD}}{t} \right) + \frac{L_G}{t - x} \right] \tag{3.13}$$

Considering the hole concentrations that we have projected from TLM measurement, the hole mobility of our device could ranging from $\mu_h \simeq 300$ cm^2/V.s for the lowly compensated sample to $\simeq 1700$ cm^2/V.s for the highly compensated sample. These value of hole mobility is typical for the bulk conduction of boron doped diamond at doping concentration of 2×10^{17} cm^{-3} [11]. This mobility is around the highest reported mobility in a diamond MOSFET, compared to inversion diamond MOSFET ($\mu_h = 8$ cm$^2/V.s$) [14] and H-diamond MOSFET (30-100 cm$^2/V.s$, this mobility has been measured by Hall effect measurement) [76]. Even this mobility could bearing some source of errors (since contact resistance were too high and compensation concentration has not been systematically quantified), this value highlights the clear benefits of a depletion mode diamond FET with an insulated gate. An improved contact resistance as well as the fabrication of the Hall bar test devices on the same substrate for the systematic investigation the compensation of the sample are critical in the next fabrication run.

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3.3.4 OFF-State

One of the most unique feature of wide bandgap semiconductors is the endurability against a high electric field in the OFF-state regime. In our device, breakdown voltage is measured by applying a positive gate bias ($V_{GS} = +12\ V$) to ensure the pinch-off of the channel. Then, V_{DS} is swept in the negative direction from 0 V to -200 V (limit of the apparatus). The current compliance is set as low as 25% ON-states current to limit the destructive high power passing through the device. The measurements have been done in the FESEM chamber under vacuum.

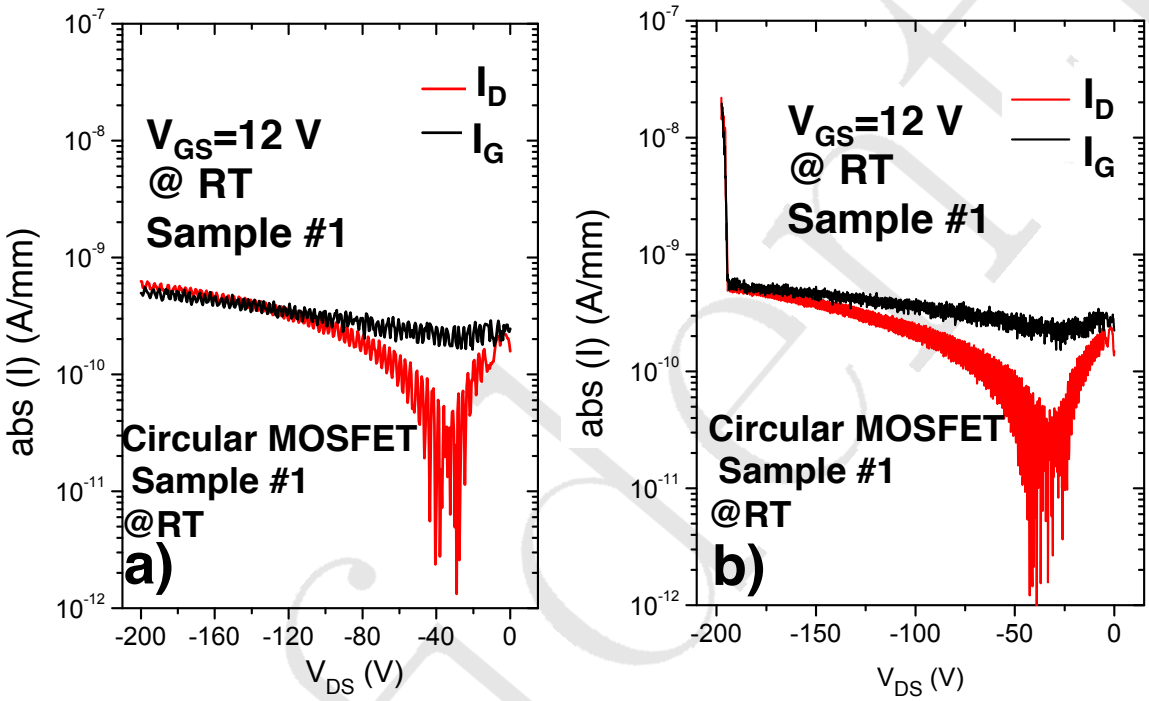

Figure 3.29: Breakdown voltage measured with V_{GS}=-12 V and drain voltage sweeping in negative bias voltage to $V_{DS} = -200$ V (limit of the apparatus): a) first cycle breakdown measurement; b) 5th cycle breakdown measurement.

Figure 3.29 represents the measured breakdown voltage of the circular device in Fig. 3.20b (I_D vs. V_{DS} and I_G vs. V_{DS}). Subthreshold leakage current is less than 10^{-10} (A). Subthreshold drain leakage current is found firstly decrease when V_{DS} is biasing from 0V to -40V and then increase for V_{DS} from -40V to -200V. This drain leakage current could be related to the potential gradient between Source and Gate as well as Drain and Gate. Since subthreshold leakage current is an important factor could initiate the premature breakdown of the MOSFET devices, a systematic investigation of the subthreshold leakage current mechanism is highly suggested. The device is able to withstand an OFF state voltage up to -200 V without any catastrophic voltage breakdown (sudden increase of subthreshold leakage current). By using the linear electric field approximation between gate and drain, a lower bound electric field is evaluated at less than 1 MV/cm for a bias of -200 V. However, since the drift layer is moderately doped (1.75×10^{17} cm^{-3}), this approximation is highly underestimating the peak electric field of the drift region.

In order to evaluate the breakdown electric field of the device, we performed a Silvaco

Atlas simulation by fixing $V_{GS} = +6$ V and sweeping V_{DS} to -200 V without implementing the impact ionization and avalanche breakdown mechanism. The temperature of this simulation is kept at RT. The simulation results are shown in Fig. 3.30 and Fig. 3.31.

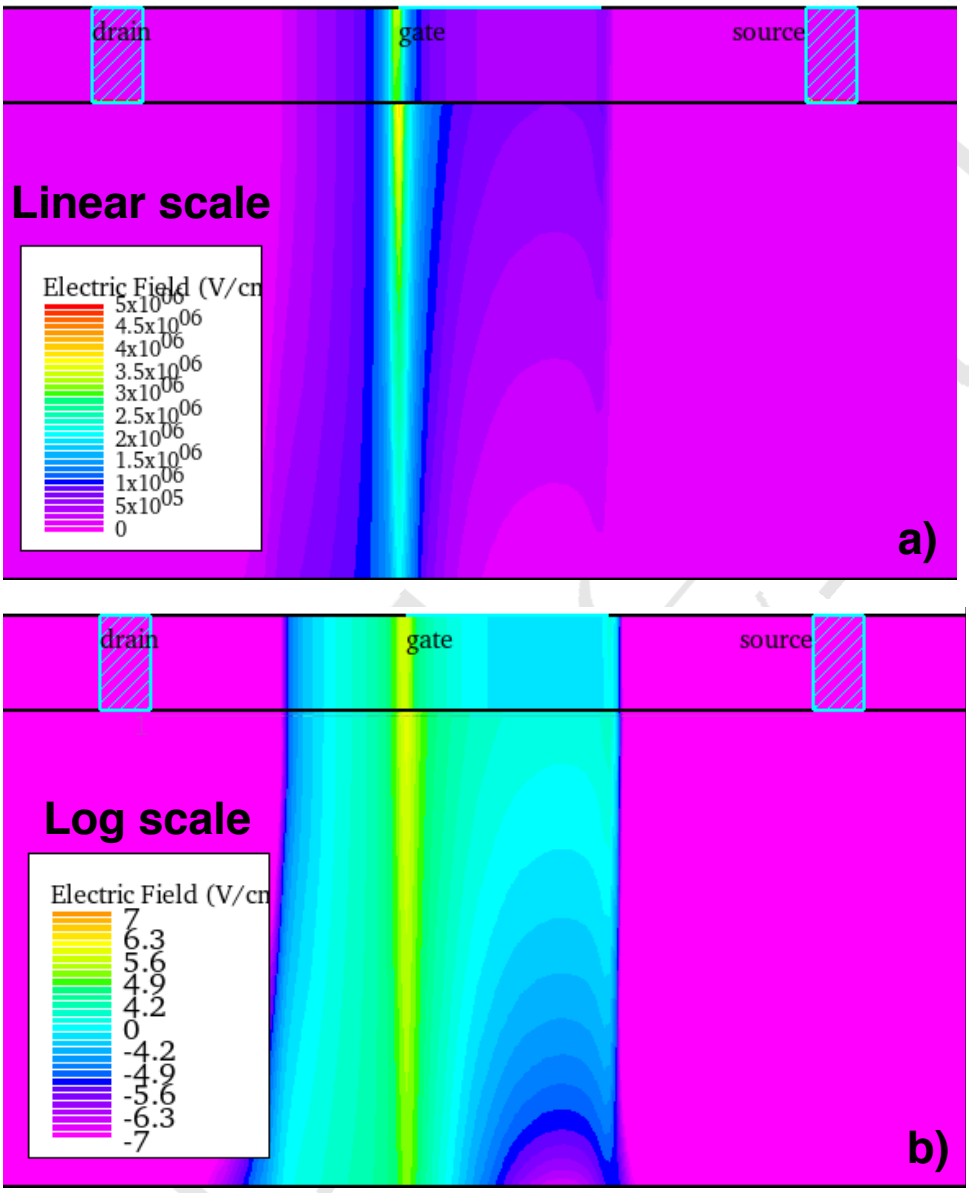

Figure 3.30: Silvaco Atlas simulation critical electric field for V_{DS}=-200 V without impact ionization a) in linear scale; b) logarithm scale

Figure 3.30 represents the electric field distribution in the structure plotted in the linear scale (Fig. 3.30a) and in the logarithm scale (Fig. 3.30b). The 2D field profiles show a spike electric field as high as 4 MV/cm beneath the gate, in diamond layer and toward the drain. This significant spike electric field could potentially initiate the premature breakdown effect. Figure 3.31 represents the cut-line of electric field in the diamond region and in the oxide region. As we can see in the Fig. 3.31b, there is an electric field as high as 3.4 MV/cm in the oxide region. Even if this electric field is lower than the critical electric field of Al_2O_3, it could potentially lead to the premature breakdown of the device. Therefore, the implementation of a field plate is necessary

to dissipate the spike electric field at the drain side of gate contact. Nonetheless, the estimated peak electric field in our fabricated transistor is close to 4 MV/cm at -200 V, which is already a high value in a lateral design without any field plate.

Also, as shown in Fig. 3.30, there is wide SCR under the gate region. This wide lateral SCR under the gate could potentially be an origin of the premature breakdown and the increase of the leakage current. These effects seem maximized since L_G is very close to L_{GS} and L_{GD}. Therefore, by reducing the gate length, it could be possible to improve the breakdown of the device.

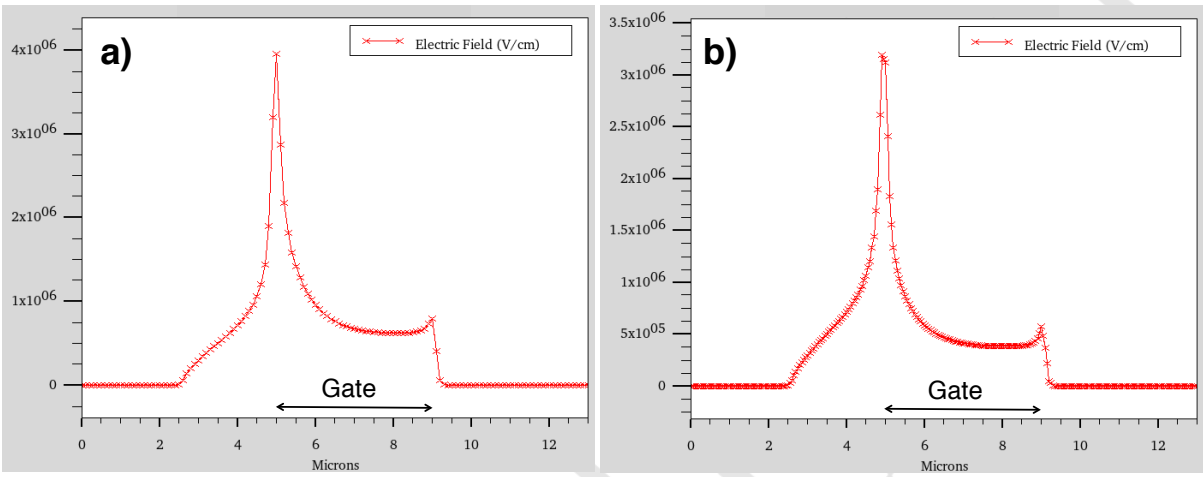

Figure 3.31: Cut line of Silvaco Atlas simulation critical electric field for V_{DS}=-200V without impact ionization a) In diamond epilayer; b) In oxide layer

When the device experiences several OFF state measuring cycles (5 cycles), the first onset current is observed at around 197 V, as shown in Fig. 3.29b. More investigation are required for the OFF state analyses: applying different V_{GS} values and measuring the different BVs, trapped charges discharging sequences, modifying the temperature, observing the destructive breakdown.

3.4 Benchmarks

In order to compare to other diamond transistors [16] [21], the Figure of Merit (RonS vs. BV) of this work is benchmarked Fig. 3.32 and projected toward device optimizations. The open circles are corresponding to devices performance at RT. The crosses are corresponding to the device performances at high temperatures.

The magenta spots represent the performance at RT (measured) and 573 K (measured) of the best diamond MESFET developed by Umezawa et al. [16] (the dimensions are estimated from the publication). These MESFET are based on a bulk conduction, therefore limited by the incomplete ionization of boron at RT, similar to the MOSFET developed in this PhD. Contrary to our MOSFET devices, the MESFETs are limited by the Schottky gate, preventing them to achieve good performances on highly doped boron layer.

The cyan spots represent the performances of the H-Diamond MOSFET (measured) developed by Kawarada et al. [21], where the conduction is based on 2DHG and not bulk conduction (dimension taken from the publication). Based on different current conduction

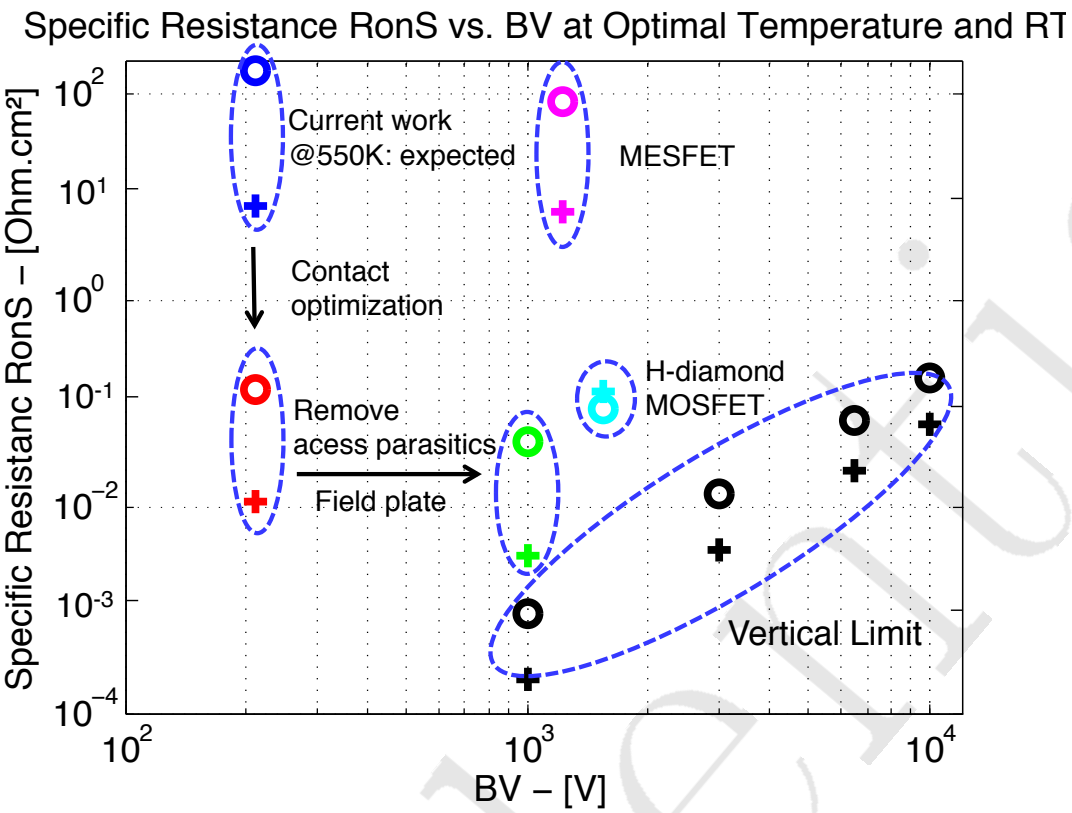

Figure 3.32: Specific ON-resistance versus breakdown voltage of different diamond transistors.

mechanisms, the ON state resistance of the MESFET exhibits a Negative Temperature Coefficient (NTC), whereas the 2DHG based devices have a Positive Temperature Coefficient. This difference is due to the increase of free carriers with higher temperatures in MESFET, whereas a higher temperature reduces the carrier mobility in 2DHG without positive effects compensating this mobility reduction.

The D-mode MOSFET in this work is represented by the blue circle (measured at RT) and the blue cross (this spot is expected). As we have discussed in the previous section, the ON-state current of this device is highly limited by the contact resistance. In fact, the contact resistance represents more than 90% of the total resistance of the device. An improvement of the contact resistance will strongly improve the ON-state current of this device. As shown by Chen et al. [129], using a proper post treatment or regrowth a highly doped p+ layer for ohmic contact, the specific contact resistance can potentially be reduced to less than 10^{-5} $\Omega.cm^2$. Taking into account the improved contact resistance, the FOM of our MOSFET at RT is expected to move to the open red circle in Fig. 3.32. The ON-state current is therefore potentially comparable with the ON-state current of the H-diamond MOSFET [21], albeit with a smaller BV.

Regarding the OFF-state breakdown voltage, as we have shown in the previous part, a spike electric field at the drain side of gate contact could potentially caused the premature breakdown. In order to reduce the peak electric field, a field plate technology is critical in such lateral high voltage devices. It has been demonstrated that by using the field plate, breakdown voltage is highly improved in the lateral design [135]. Therefore, the implementation of field plate(s) is required in the transistor design to allow the

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diamond reaching its theoretical avalanche breakdown voltage. Assuming that the breakdown is only due to the avalanche effects (impact ionization), a maximum breakdown voltage using the same epilayer doping concentration (1.75×10^{17} cm^{-3}) is expected at approximately 1000 V in the Non Punch Through condition [23].

In the optimized structure for typical high voltage power devices, the ON-resistance is generally mainly due to the resistance of the drift region, which is the smallest total resistance possible for a BV value. Any other source of series resistance must be further eliminated. If one can achieve both the reduction on series resistance along with field plate structure to maximize the breakdown field, the FOM of our MOSFET can be improved as the green spots in the Fig. 3.32. Further reductions on the RonS for the same BV can be achieved, but it would require a thicker drift region, where the channel would consequently be more difficult to fully deplete.

The critical challenges with our device architecture is to achieve a high electric field, and to combine a thick drift region, with a channel exhibiting distinctive ON and OFF states. Nonetheless, new lateral architectures can be further optimized, and the theoretical minimum RonS FOM at RT is plotted in Fig. 3.32 (this is the limit of the vertical devices). The theoretical breakdown voltage vs. specific ON-resistance has been determined by considering the ideal mobility where the scattering mechanisms are purely phonon and doping dependent [11][6].

As far as breakdown voltage is concerned, Chicot et al. [23] introduced an optimization calculation breakdown voltage based on avalanche effect with the up to date ionization coefficients [132][29]. As shown in Fig. 3.33, for different breakdown voltage 1 kV, 3 kV, 6.5 kV, 10 kV, the optimized doping concentration and drift region is 1.8×10^{17} (cm^{-3}), 1.9×10^{16} (cm^{-3}), 5.5×10^{15} (cm^{-3}), 2.5×10^{15} (cm^{-3}) and 1.9 μm, 10 μm, 27 μm, 48 μm, respectively, in a NPT configuration. The question of avalanche breakdown in diamond devices remains however open, since most observed breakdown mechanism are destructive and non-reproducible, or based on excessive leakage current.

Since our MOSFET architecture is based on free carriers from boron doped diamond, the ON resistance can be reduced at higher temperatures. However, the increase of free carrier is compensated by the decrease of carrier mobility, as presented in chapter 1. For each targeted voltage breakdown (i.e. doping level and length of the drift region), it exists therefore an optimal temperature where the Ron is minimized. Such points are presented in Fig. 35 (the black crosses). The key challenges will be now to push the FOM towards those theoretical values, with outstanding performances relatively to other semiconductors devices.

3.5 Conclusion

In summary, by using the oxygen terminated boron doped diamond and an optimized MOS capacitor technology, we have demonstrated a lateral diamond MOSFET. This transistor is normally ON and is working in depletion mode. A clear transistor action with both ON and OFF states was achieved. By fabricating and analyzing the test devices like TLM, MOS capacitors and the combination of 2D simulation and electrical models, the physical parameters of the transistors are evaluated. The high contact resistance is currently limiting the ON-state current, which was expected. The simplified process

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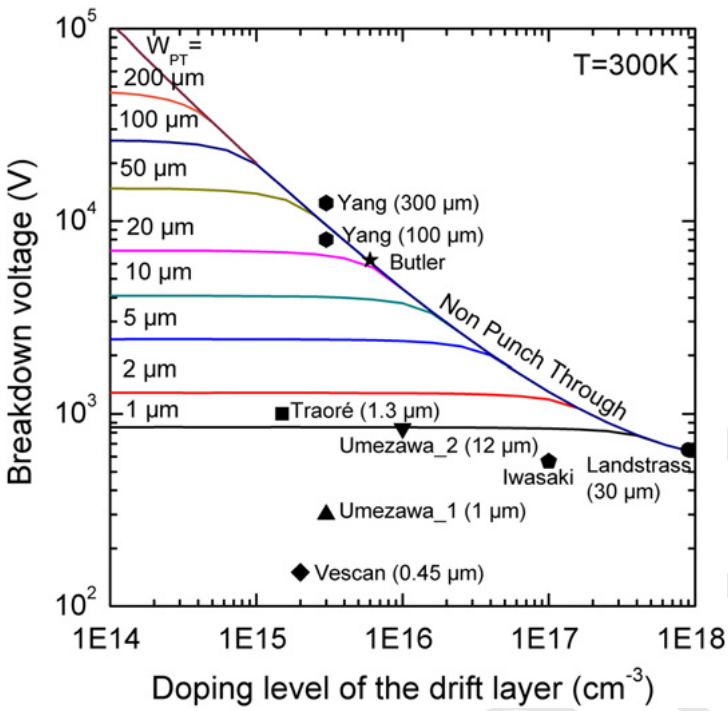

Figure 3.33: Specific ON-resistance vs. different breakdown voltage of NPT boron doped diamond devices. Courtesy to Chicot et al. [23]

was selected for the sake of reducing the fabrication time, albeit with large contact resistances. After excluding the contribution from the contact resistance, the hole mobility is quantified. A high hole mobility (from 300 cm^2/V.s to 1700 $cm^2/V.s$ has been evaluated. It is among the highest carriers mobility in a diamond transistor. A breakdown voltage higher than 200 V is measured. The 2D simulation illustrates a corresponding critical electric field of 4 MV/cm at the gate edge. The device performance is benchmarked with other diamond transistors, highlight further optimizations. There is still an open road to improve the performances of lateral and vertical transistors based on CVD diamond.

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3.6 General Conclusion and Perspective

3.6.1 General Conclusion

This thesis has been dedicated to investigate the boron doped oxygen terminated diamond/Al_2O_3 MOS capacitors for unipolar diamond transistor devices.

In chapter 1, we have shown that boron doped diamond is a fascinating semiconductor with multiple superior physical properties for power electronics devices. The 2DHG surface channel diamond MOSFET is seemly not sufficient to fulfill all the potential. Controlling the bulk of impurities doped diamond to realize the transistors is therefore crucial.

Chapter 2 has been dedicated for the understanding of oxygen terminated boron doped diamond MOS capacitor. This chapter is including three main parts:

Part 1 introduced a new technical approach to reduce series resistance and improve gate oxide in fabricating O-diamond MOS capacitor test devices. We introduce the complementary measurement techniques to obtain a proper C-V measurements. Systematic measurement were performed to ensure the reliability and reproducibility of the system. Crucial information on the MOS capacitor system were obtained. An effective gate controlled diamond SCR width was demonstrated. It is promising to fabricate a depletion mode diamond MOSFET.

Part 2 elucidated the typical electrical characteristics of O-diamond MOS capacitor. Forward current mechanism is proposed where the oxide tunneling and semiconductor interface states recombination played an important role. Oxide tunneling limiting process were identified and the corresponding approximation were made. By subtracting DC current, equivalent conductance $\frac{G_P}{\omega}$ and interface states density D_{it} were extracted. Single state model was found sufficient to correlate with experiment results. Impedance and capacitance measurements are well reproduced by simulating the equivalent circuit with all evaluated input parameters. Simulation results demonstrated that gate leakage current via interface states caused the capacitance-frequency dependence in O-diamond MOS capacitor. Complete electrostatic model for O-diamond MOS capacitor has been also established.

Part 3 investigated the origin of reverse current in O-diamond MOS capacitors. The correlation between substrate profile with MOS capacitors electrical characteristics were done. Diamond-like defective leakage spots with bunch of dislocations inside were found to be responsible for the reverse current. Localized A-band peak in CL measurement are not necessary representing the killer defects. Hole injection from metal gate are suggested as the origin of reverse current in O-diamond MOS capacitor. Reverse current caused the capacitance-frequency dependence on C-V measurements. The impedance simulation by using the equivalent circuit with all quantified parameters has unambiguously demonstrated the relationship between reverse current and capacitance measurement. Minority carriers inversion claimed by Kovi and co-authors [20] is most probably an effect from parasitic reverse current.

In Chapter 3, by using the oxygen terminated boron doped diamond and an optimized MOS capacitor technology, we have demonstrated a lateral diamond MOSFET.

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This transistor is normally ON and is working in depletion mode. A clear transistor action with both ON and OFF states was achieved. By fabricating and analyzing the test devices like TLM, MOS capacitors and the combination of 2D simulation and electrical models, the physical parameters of the transistors are evaluated. The high contact resistance is currently limiting the ON-state current, which was expected. The simplified process was selected for the sake of reducing the fabrication time, albeit with large contact resistances. After excluding the contribution from the contact resistance, the hole mobility is quantified. A high hole mobility (from 300 cm^2/V.s to 1700 $cm^2/V.s$) has been evaluated. It is among the highest carriers mobility in a diamond transistor. A breakdown voltage higher than 200 V is measured. The 2D simulation illustrates a corresponding critical electric field of 4 MV/cm at the gate edge. The device performance is benchmarked with other diamond transistors, highlight further optimizations. There is still an open road to improve the performances of lateral and vertical transistors based on CVD diamond.

3.6.2 Perspective

To realize the higher OFF-state breakdown voltage (few kVs), drift region doping concentration are necessary to be reduced and oxide thickness are necessary to be increased (like transistor sample #2). As shown in Fig. 3.34, the transistor of our sample #2 exhibits the clear electrostatics gate modulates source-drain current effects. However, since the epilayer has not been optimized, the OFF-state regime of this device can not be obtained (since reverse leakage current start to appear at high positive gate bias). Therefore, the thickness of epilayer have to be further optimized to ensure that both the ON-state and OFF-state regime of the transistor can be obtained.

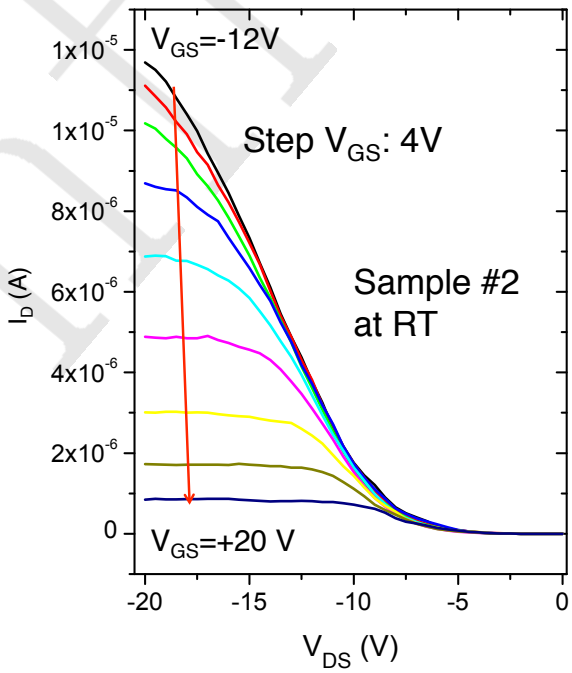

Figure 3.34: Electrostatics gate controlled the current between Source and Drain at different gate bias. Transistor sample #2.

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Nevertheless, sample #2 is very interesting since accumulation regime in O-diamond MOS capacitor were observed for the first time. As shown in chapter 2, due to interface states and leakage current, FLPE prevents the O-diamond MOS capacitor reach accumulation. In our transistor sample #2, by using thick oxide (40 nm) and the annealing at 500 $°C$, we have removed the forward leakage current, as shown in Fig. 3.35a and reduce interface states. The O-diamond MOS capacitor exhibits a proper C-V curve with the clear accumulation, flatband, depletion and deep depletion regimes, as shown in Fig.3.35b.

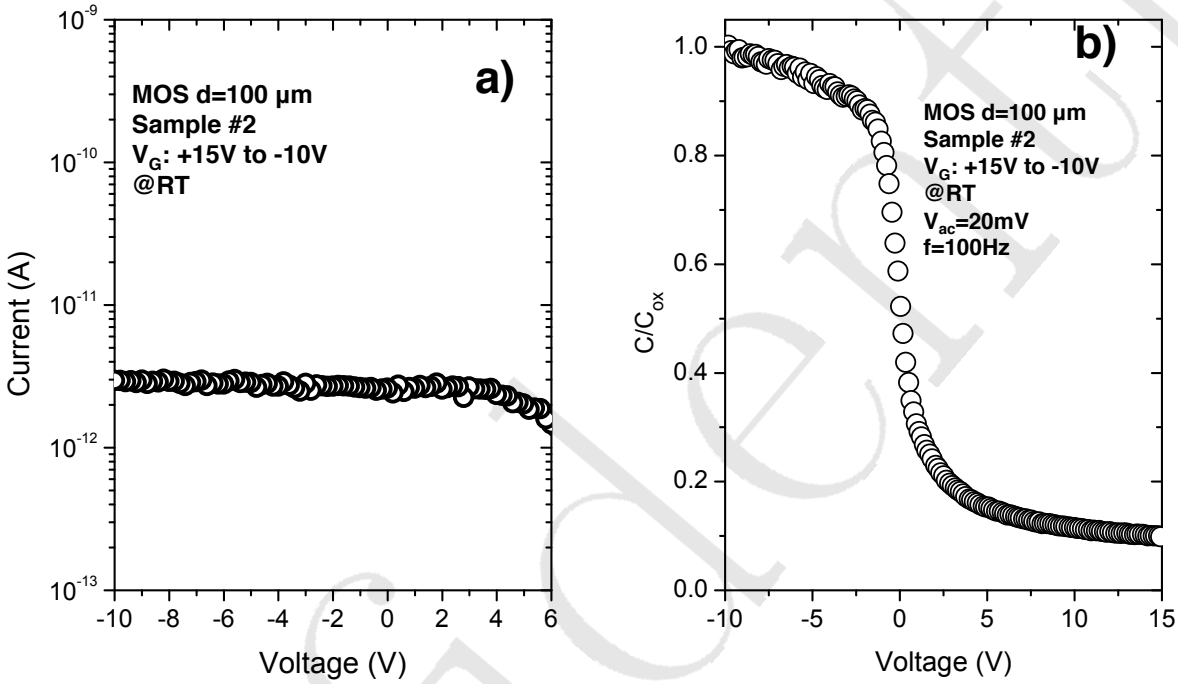

Figure 3.35: a) DC leakage current and b) Capacitance-voltage characteristic measured at 100 Hz of MOS 100um, sample #2.

Investigate the accumulated hole gas will be important to improve the depleted mode boron doped diamond MOSFET, especially in the ON-state. Therefore, fabricate the Hall bar test devices on the same sample to investigate the accumulated hole gas is needed in near future. This Hall bar test device is also required to investigate the compensation of the boron doped diamond epilayer. It will allow us to be more quantitative on transistor analysis.

Regarding ON-state current, as we have demonstrated, the ON-state current of this device is highly limited by the contact resistance. An improvement of the contact resistance is critical. Therefore, optimizing the ohmic contact annealing temperature or performing the selective etching and then regrowth the p+ diamond for ohmic contact is highly desired. Also, optimized transistor structure to eliminate parasitics resistance toward a smallest total resistance possible for a given BV value is highly desired to improve the device performance.

Regarding the OFF-state breakdown voltage, as we have shown in the previous part, a spike electric field at the drain side of gate contact could potentially caused the premature breakdown. A field plate technology is critical in such lateral high voltage devices.

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Therefore, the implementation of field plate(s) is required in the transistor design to allow the diamond reaching its theoretical avalanche breakdown voltage. Identifying the subthreshold leakage current is also equivalently important. Since subthreshold leakage current can be the origin of premature breakdown voltage. Therefore, additional electrical measurements to identify the subthreshold leakage current is critical to understand the premature breakdown voltage and further improve the OFF-state performance.

In the end, thanks to the mastering diamond/oxide interface, the first proper bulk controlled boron doped diamond power MOSFET has been realized. This will open the new path to realize the other bulk controlled diamond MOSFETs for power devices.

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Deep-depletion mode boron doped monocrystalline diamond metal oxide semiconductor field effect transistor

Thanh-Toan Pham, Julien Pernot, David Eon, Etienne Gheeraert and Nicolas Rouger

***Abstract*—A p-type deep-depletion mode monocrystalline diamond MOSFET is demonstrated for the first time, with a $190nm$-thick controllable channel. Such a device offers new opportunities for a better optimization of the bulk doping versus designed breakdown voltage and the resulting figure of merit. Diamond MOSFETs with Boron doping of $1.75 \times 10^{17} cm^{-3}$ and using $20nm$ ALD deposited Al_2O_3 as the gate oxide show promising IV characteristics, with a clear ON and OFF state operation. The MOSFETs have a normally-ON operation with typical threshold voltages of $V_{TH} = +7V$ and a ON-state drain current of $I_{SD} = 1.9\mu A/mm$ at $V_{SD} = 10V$ and $V_{GS} = -5V$, at room temperature. A high hole mobility from $300cm^2/V.s$ to $1700cm^2/V.s$ has been extracted both for channel and bulk regions. Just before the experimental voltage breakdown at $200V$, the gate leakage is still below $0.6nA/mm$ at room temperature and the peak electric field in diamond at the gate edge is simulated at $4MV/cm$. Beyond this first experimental proof of concept, these combined values show the high potential of deep-depletion mode Boron doped diamond MOSFETs.**

***Index Terms*—Diamond transistor, Boron doped monocrystalline diamond, depletion mode diamond MOSFET.**

I. Introduction

Diamond has unique properties such as a wide bandgap of 5.5eV, a high thermal conductivity of 20W/cm.K, high free carrier mobility and hopping conduction mechanisms. The classical doping techniques of diamond rely on incorporation during growth of impurities with high activation energies (p-type Boron 0.38eV and n-type Phosphorous 0.6eV), with consequently p-type doping as the main approach. These properties can have a high impact in electronics and power electronics applications, where diamond (power) devices can have better performances at high temperatures (400K-700K), with outstanding figures of merit (lower specific ON state resistance $R_{ON}S$, higher breakdown voltages BV). Several diamond transistor architectures have been proposed in the litterature, with a special focus on two dimensional hole gas (2DHG) based Field Effect Transistors (FET) [1], [2], Junction FETs [3], [4] and MEtal Semiconductor FETs [5], [6]. Diamond 2DHG FETs require a Hydrogen (H) terminated diamond surface and a specific control of H-terminated surface and adsorbed ions during the fabrication. The ON state resistance in such transistors depends on surface conduction (sheet free carrier concentration and hole mobility in 2DHG, typical resistivity with a positive temperature coefficient) whereas the OFF state voltage breakdown is governed by typically unintentional doped diamond. In other p-type diamond transistors as MESFETs, the drift region is designed accordingly to the $R_{ON}S$ versus BV optimization (typical resistivity with a negative temperature coefficient), but with limitations due to excessive gate leakage for higher doping levels. Typical hole mobilities in previous diamond transistors were $8cm^2/V.s$ [7] and $30 - 100cm^2/V.s$ [8] (hall effect measurement), showing room for improvements. On the other hand, several efforts on the MOS gate stack on Oxygen (O) terminated monocrystalline diamond have been done in [9], [10], offering new opportunities for diamond MOSFETs on O-terminated surfaces and better FET channel control. Novel MOSFET architectures have been also demonstrated in other wide bandgap materials, as with n-type $\beta-Ga_2O_3$ depletion mode MOSFETs [11]–[14]. In this work, we design and develop a deep depletion mode diamond p-type MOSFET with a MOS gate on O-terminated diamond - figure 1. This normally-ON MOSFET will be grown on a nitrogen doped (n-type) monocrystalline diamond substrate. This depletion mode MOSFET offers new opportunities for a reliable fabrication and better $R_{ON}S$ versus BV compromises over a wide range of breakdown voltage and temperatures (in comparison with 2DHG FETs), and with a strongly reduced gate leakage (in comparison with MESFETs).

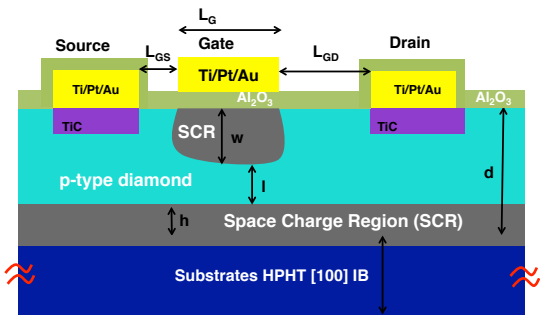

Fig. 1. Conceptual cross-section structure of the depletion mode oxygen-terminated boron doped diamond MOSFET.

II. Fabrication

As a first proof of concept, two mask levels are processed, namely for ohmic contacts (drain and source contacts) and for

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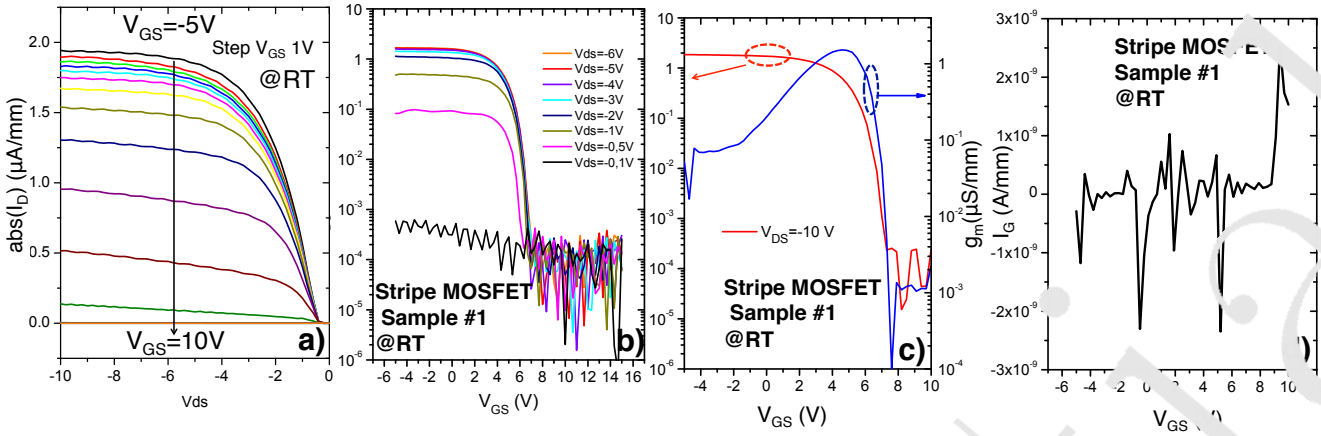

Fig. 3. Transfer characteristics of the stripe transistor measured by a),b) and c) Drain current I_D for different sweep conditions; d) Gate leakage current I_G measured during c). The measurements have been performed at RT in the vacuum chamber of FESEM system.

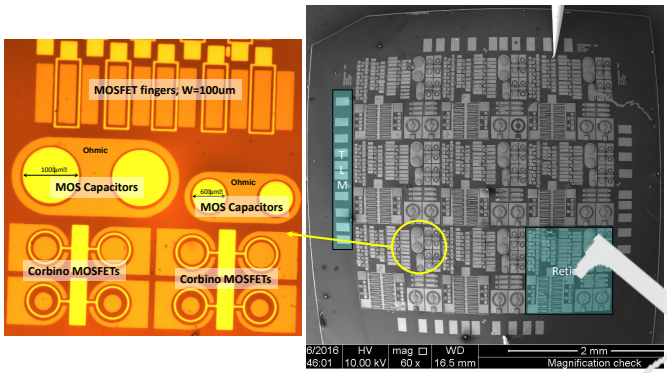

Fig. 2. Top view of the fabricated boron doped diamond MOSFET and test devices: left, zoom under optical microscope and right, SEM image of the whole diamond sample.

Type, Device #	Lgs	Lg	[illegible]	W
	μm	μm	μm	μm
Finger, #1	4	3	3	34
Corbino #2	4	[illegible]	10	176

TABLE I
PARAMETERS OF SELECTED TRANSISTORS - MASK DIMENSIONS.

gate regions (gate metal on top of high k gate oxide) - Figure 2. First, a CVD Boron doped diamond layer was grown on a $4 \times 4mm^2$ Ib High Pressure High Temperature (HPHT) Nitrogen-doped diamond substrate. Detailed conditions on MPCVD diamond growth and doping control were addressed in our previous publications [9], [10], [15]. A 230nm thick boron doped layer was grown using a gas mixture of methane ($[CH_4]/[H_2] = 1\%$), diborane ($[B]/[C] = 600ppm$) at a pressure of 33 Torr and a temperature of 870°C, targeting $[B] = 2 \times 10^{17} cm^{-3}$. Oxygen was used in the gas phase ($[O_2]/[H_2] = 0.25\%$) in order to increase the crystalline quality of the layer. After the growth of epilayers, dusts were removed by using conventional solvent in ultrasonic condition. Then graphite and non-diamond phase were removed by using a conventional cleaning recipe of a three acid mixture (H_2SO_4, HNO_3 and $HClO_4$) at 300°C. Laser lithography (Heidelberg DWL66FS) was employed. Plassys electron beam evaporator was used to deposit the stack of Ti/Pt/Au (thicknesses of 40 nm/10nm/40 nm respectively), followed by lift-off in acetone solution. Since as-deposited Ti/Pt/Au on top of diamond does not show ohmic contact behavior, an annealing at high temperature is required [16]. The sample was then annealed at 600°C in vacuum environment with typical pressure of 10^{-5} (mbar). The diamond surface was then oxygenated by using deep UV-ozone treatment [17]. A 20nm thick Al_2O_3 gate oxide was deposited at 380°C by using Savannah 100 deposition system from Cambridge NanoTech. The precursor was Trimethylaluminium (TMA) and oxidant was water. The pulse and exposure duration were 15 ms and 30 s, respectively. Typical chamber pressure was 1.3×10^{-1} (Torr). As shown in figure 2 and table I, both MOSFET fingers and cylindrical corbino structures have been fabricated, respectively for better ON state characterization and electric field management in OFF state. The dimensions have been targeted as a first proof of concept, with a limited stress on lithography and fabrication steps.

III. Results and Discussion

Key parameters have been extracted with test structures on the same sample (MOS capacitors): the boron doping is $1.75 \times 10^{17} cm^{-3}$ and the SCR extension in the CVD p-type diamond towards the n-type substrate is 40nm (C-V). The consequent sheet resistance and resistivity of the p-type neutral region is estimated at $R_{sheet} = 4M\Omega/\square$, $\rho_{epi} = 75\Omega.cm$ (room temperature, doping compensation).

A. ON-State and OFF-State

Figure 3 shows the clear ON-state and OFF-state operations of the depletion mode diamond transistor (#1), with a normally-ON behavior: the maximum drain saturation current is $I_{DS} = -1.91\mu A/mm$ at $V_{DS} = -10V$ and $V_{GS} = -5V$, a threshold voltage $V_{TH} = +7V$ and a gate leakage below detection limit over the swept biasing conditions. In the linear regime, the measured specific ON resistance is 162

$\Omega \cdot cm^2$ (active region, without contact areas). Due to the FESEM setup, it was not possible to measure the temperature effects on the transistors. A $R_{ON}S$ of 8 $\Omega \cdot cm^2$ is expected at higher temperatures. As evidenced by Conductance-Bias-frequency analyses, Fermi Level Pinning Effect (FLPE) due to interface states prevents however to achieve the accumulation regime in ON state (**[1REF]**). The breakdown and OFF-state characterization of the Corbino #2 transistor is presented in figure 4: the maximum breakdown voltage is close to $200V$, with a low leakage current close to the breakdown ($10^{-10}A$ or $0.6nA/mm$). Figure 4c) shows the simulated electric at $200V$, with the gate biased in deep depletion regime. The simulated peak electric field in diamond is 4MV/cm, with a SCR width towards drain of 2.5μm. These values show great opportunities for further improvements, with already attractive performances.

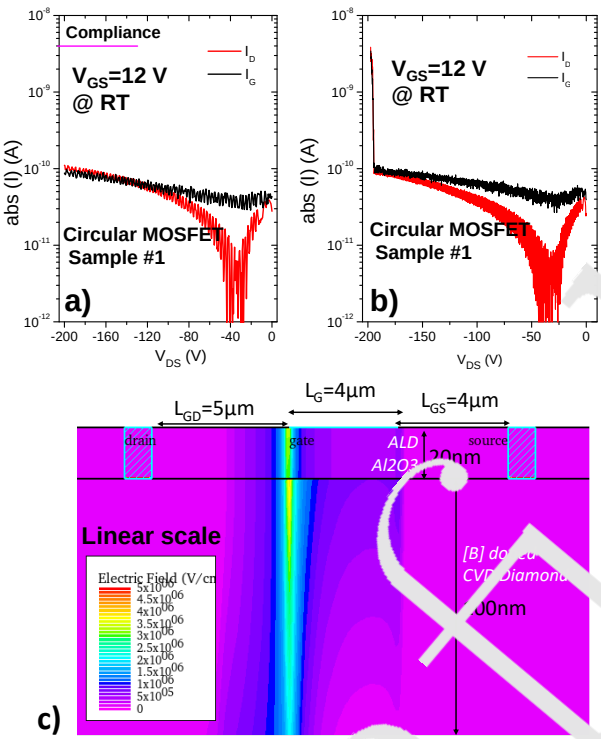

Fig. 4. Breakdown voltage measured with V_{GS}=-12 V and drain voltage sweeping in negative bias voltage to $V_{DS} = -200$ V (limit of the apparatus): a) first cycle breakdown measurement; b) 4th cycle breakdown measurement. c) 2D simulation at $V_{DS} = -200$ V and $V_{GS} > V_{TH}$

B. Carrier mobility

Assumptions: constant doping profile + no carrier gradient + no 2D/3D current spreading. The carriers mobility between source and drain can be evaluated after eliminating the contribution from contacts resistance 2RC $R_{Semi} = R_{SD} - 2R_C$, whereas R_{semi} is as defined as in Fig. 1, it can be calculated as: The carrier mobility under low field in semiconductor region can be evaluated as:

$$\mu_h = \frac{1}{qpR_{Semi}W}\left[\left(\frac{L_{GS}+L_{GD}}{d-h}\right)+\frac{L_G}{d-h-l}\right] \quad (1)$$

Considering the hole concentrations that we have extracted from TLM measurement, the hole mobility of the device extracted at different gate biases is ranging from $\mu_h \simeq 300$ cm^2/V.s for the lowly compensated sample to $\simeq 1700$ cm^2/V.s for the highly compensated sample. These values of hole mobility are typical for the bulk conduction of boron doped diamond at doping concentration of 2×10^{17} cm^{-3} [18]. This mobility is around the highest reported mobility in a diamond MOSFET. Even if this mobility could bearing some source of errors (since contact resistance were too high and compensation concentration has not been systematically quantified), this value highlights the clear benefits of a depletion mode diamond FET with an insulated gate. An improved contact resistance as well as the fabrication of the Hall bar test devices on the same substrate for the systematic investigation the compensation of the sample are critical in the next fabrication run.

C. Benchmark

In order to compare to other diamond transistors [6] [19], the Figure of Merit (RonS vs. BV) of this work is benchmarked in figure 5, highlighting measured performances and foreseen improvements (circles and crosses are respectively performances at RT and high temperatures). Combining these attractive figures of merit with extremely low leakage current and high temperature operation capability, depletion mode diamond transistors are demonstrated for the first time as realistic solutions.

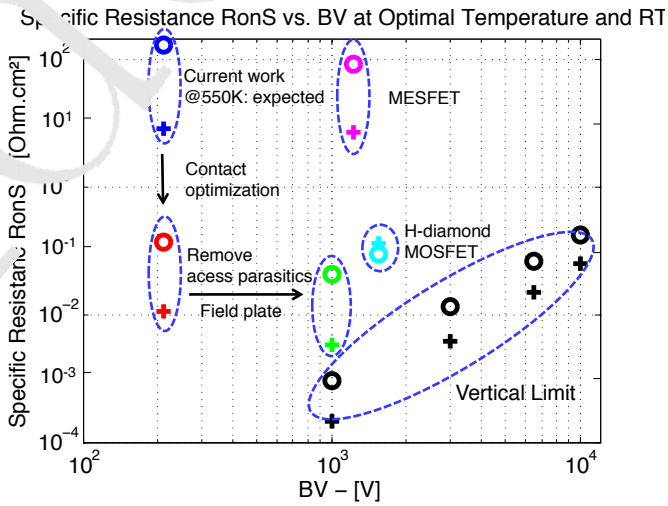

Fig. 5. Specific ON-resistance vs breakdown voltage.

IV. Conclusion

In summary, by using the oxygen terminated boron doped diamond and an optimized MOS capacitor technology, we have demonstrated a lateral diamond MOSFET. This transistor is normally ON and is working in the deep depletion mode. A clear transistor action with both ON and OFF states was achieved. A simplified fabrication process was selected for the sake of reducing the fabrication time, albeit with large contact resistances. After excluding the contribution from the

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contact resistance, the hole mobility is quantified. A high hole mobility (from 300 cm^2/V.s to 1700 $cm^2/V.s$ has been evaluated. It is among the highest carriers mobility in a diamond transistor. A breakdown voltage higher than $200V$ is measured. The 2D simulation illustrates a corresponding critical electric field of 4 MV/cm at the gate edge. The device performance is benchmarked with other diamond transistors, highlighting further optimizations. There is still an open road to improve the performances of lateral and vertical transistors based on CVD diamond. Such improvements will focus on the reduction of series resistance and interface state density, annealing at high temperature to improve the gate oxide crystallinity, reaching the accumulation regime, adding an efficient field plate and optimizing transistor dimensions.

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