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préparée au sein du **Laboratoire des Systèmes Photovoltaïques (LSPV/CEA-INES) / Laboratoire de Génie Electrique de Grenoble (G2Elab)**
dans **l'École Doctorale Electronique, Electrotechnique, Automatique et Traitement du Signal**

Design and Characterization of a Three-phase Current Source Inverter using 1.7kV SiC Power Devices for Photovoltaic Applications

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Abstract

Classically, the energy conversion architecture found in photovoltaic (PV) power plants includes solar arrays delivering a maximum voltage of 1kV followed by a step-up chopper connected to a three-phase Voltage Source Inverter. This multistage conversion system (DC/DC + DC/AC) is then connected to the medium-voltage grid through a low-voltage/medium-voltage transformer. In order to simplify the PV systems, this research work focuses on the study and implementation of a DC/AC topology employing a single power processing stage: the three-phase Current Source Inverter (CSI). To deal with the inconvenient of high conduction losses when implementing this topology, wide-bandgap Silicon Carbide (SiC) semiconductors are used, allowing to efficiently convert energy while keeping a relatively high switching frequency. Nonetheless, since the available power semiconductor modules on the market are not compatible with the CSI, a novel 1.7kV SiC-based voltage bidirectional module is developed in the context of this thesis. Hence, the dynamic characterization of the new SiC device is carried out and serves as the basis for the design of a 60kW CSI prototype. Finally, the inverter efficiency is evaluated at nominal operating conditions, employing both a calorimetric and electrical methods. The obtained results confirm the CSI ability to operate efficiently at high switching frequencies (η>98.5% @60kHz). The originality of this work lies mainly in the design, characterization and implementation of the new 1.7kV full-SiC power module adapted to the CSI topology.

Keywords: Power electronics, DC/AC converters, Current Source Inverter (CSI), Silicon Carbide (SiC), Photovoltaics, Power module.

Résumé

Classiquement, la chaîne de conversion d'énergie électrique des centrales photovoltaïques comporte un champ photovoltaïque (PV) délivrant une tension maximale de 1kV suivi d'un hacheur élévateur connecté à un onduleur de tension triphasé. Cette chaîne de conversion à deux étages (DC/DC + DC/AC) est ensuite raccordée sur le réseau moyenne tension à l'aide d'un transformateur élévateur. Dans l'objectif de simplifier les systèmes de conversion PV, ce travail de recherche s'intéresse à l'étude et la mise en œuvre d'une topologie DC/AC n'employant qu'un seul étage de conversion : l'onduleur de courant triphasé. Bien que relativement simple, l'onduleur de courant présente comme inconvénient majeur ses pertes par conduction. Pour pallier à ce problème, des interrupteurs grand-gap au Carbure de Silicium (SiC) sont employés, ce qui permet de convertir l'énergie à haut rendement ($\eta > 98.5\%$) tout en gardant une fréquence de découpage élevée (plusieurs dizaines de kHz). Les modules à semi-conducteurs de puissance disponibles sur le marché n'étant pas compatibles avec ce type de convertisseur, des modules dédiés intégrant du SiC ont été développés dans le cadre de cette thèse. La caractérisation dynamique de ces nouveaux modules a été réalisée dans le but de servir de point d'appui à la conception d'un démonstrateur d'onduleur de courant d'une puissance nominale de 60kW. Enfin, le rendement de la partie semi-conducteur de puissance est évalué à l'aide d'une méthode calorimétrique confirmant la capacité de cette topologie à fonctionner à des fréquences de découpage plus élevées. L'originalité de ces travaux réside principalement dans la conception, la caractérisation ainsi que la mise en œuvre d'un nouveau module de puissance dédié à cette topologie. Cette dernière étant connue mais peu étudiée à l'heure actuelle avec des interrupteurs au SiC.

Mots-clés: Electronique de puissance, Conversion DC/AC, Onduleur de courant, Carbure de Silicium (SiC), Photovoltaïque, Modules de puissance.

Acronyms and Abbreviations

4qCSI	CSI with four-quadrant switches
AC	Alternating current
AMB	Active metal brazing
BOS	Balance of system
BW	Bandwidth
CAPEX	Capital expense
CCM	Continuous conduction mode
CM	Common mode
CSC	Current source converter
CSI	Current source inverter
CSI7$_{\text{op.1,2}}$	CSI with 7 switches employing modulation strategy 1 and 2
CT	Current transformer
CTE	Coefficient of thermal expansion
D^{2}PAK	Semiconductor package also kwon as TO-263
DC	Direct current
DCM	Discontinuous conduction mode
DMOSFET	Double-diffused MOSFET
DPF	Displacement power factor
DPT	Double-pulse test
DSCT	Double-stage current transformer
DUT	Device under test
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EPBT	Energy payback time
ESL	Equivalent series inductance
ESR	Equivalent series resistance
FEA	Finite element analysis
FOM	Figure of merit
FR4	Flame resistant 4
HS	High-side

HVDC	High-voltage direct current
HVRT	High voltage ride-through
*i*Boost	Interleaved boost converter
IGBT	Insulated gate bipolar transistor
LCOE	Levelized cost of energy
LS	Low-side
LV/MV	Low-voltage/medium-voltage
LVRT	Low voltage ride-through
MOSFET	Metal-oxide-semiconductor field-effect transistor
MOV	Metal oxide varistor
MPPT	Maximum power point
MPP	Maximum power point tracking
MPS	Merged pin-Schottky
NPC	Neutral point clamped
OPEX	Operating expense
PBT	Polybutylene terephthalate
PCB	Printed circuit board
PTC	Positive temperature coefficient
PV	Photovoltaic
PWM	Pulse width modulation
RMS	Root-mean-square
SBD	Schottky barrier diode
SMD	Surface-mount device
SOA	Safe operating area
SVM	Space vector modulation
TCC	3-level camping cell
THD	Total harmonic distortion
TIM	Thermal interface material
VSC	Voltage source converter
VSI	Voltage source inverter
WBG	Wide-bandgap
ZCS	Zero-current switching
ZVS	Zero-voltage switching

Ag	Silver
Al	Aluminum
Al_2O_3	Aluminium oxide or alumina
AlN	Aluminium nitride
AlSiC	Aluminum/Silicon carbide
Cu	Copper
GaN	Gallium nitride
MnZn	Manganese/Zinc
NiZn	Nickel/Zinc
Pb	Lead
Si	Silicon
Si_3N_4	Silicon nitride
SiC	Silicon carbide
SiO_2	Silicon dioxide
Sn	Tin

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Luís Gabriel ALVES RODRIGUES

Corre um boato aqui donde eu moro
Que as mágoas que eu choro são mal ponteadas
Que no capim mascado do meu boi
A baba sempre foi santa e purificada

Diz que eu rumino desde menininho
Fraco e mirradinho a ração da estrada
Vou mastigando o mundo e ruminando
E assim vou tocando essa vida marvada

É que a viola fala alto no meu peito humano
E toda moda é um remédio pros meus desenganos
É que a viola fala alto no meu peito, humano
E toda mágoa é um mistério fora deste plano

Pra todo aquele que só fala que eu não sei viver
Chega lá em casa pruma visitinha
Que no verso ou no reverso da vida inteirinha
Há de encontrar-me num cateretê

Vide vida marvada
Rolando Boldrin, o Sr. Brasil

A toda minha família,
especialmente a minha mãe, Nilza, e
aos meus avós, vó Maria, vó Ana e vô Luiz.

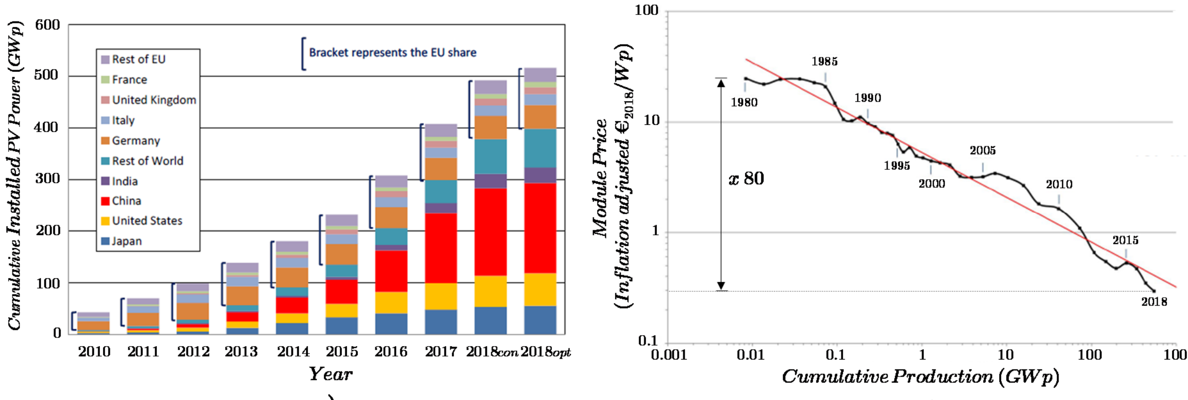
Table of Contents

Chapter 1

Introduction

1.1 Photovoltaic Scenario Overview

The most important challenges faced by society in recent years are related to sustainable development and climate change. Due to the limited resources of fossil fuels together with efforts to reduce global warming, governments have been leading the change to low-carbon energy systems. In this energy transition context, in both academia and industry, great research effort is focused today to increase efficiency and limit costs of renewable energy sources as hydropower, wind, solar, and biomass. Among all alternative energy sources, solar photovoltaic (PV) technologies have been drawn particular attention, attracting in 2017, 58% of all new renewable energy investments worldwide, i.e., €140 billion [1]. As pointed out in [2], [3], the levelized cost of energy[1] (LCOE) in utility-scale PV power plants has reached, in some cases, that of fossil fuel-fired electricity. Also, the benchmark PV system LCOE has decreased by over 75% during the period 2009 – 2018 [1]. The main contributor to that is the decrease of PV solar panel prices (85% for the same period). In Figure 1.1 are depicted the cumulative installed PV power worldwide and the learning curve of PV module prices, where all commercially available technologies are included.



a) b)

Figure 1. 1 – a) Cumulative installed PV power worldwide from 2010 to 2018. Source: modified from [1] and b) PV module price learning curve – all commercially available technologies included. Source: modified from [4].

Thanks to the attained maturity level of PV technology, the energy payback time[2] (EPBT) of PV systems in high solar irradiance regions in Europe might be

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[1] The LCOE is an average cost indicator that takes into account the amount of energy produced by a power plant during its entire lifetime with regard to its total cost of manufacturing, installation and operation.

[2] The EPBT of a power generating system is defined as the time required to generate as much energy as is consumed during production and lifetime operation of the system. The energy required to recycle the PV system when it reaches the end-of-life is not taken into account here.

as low as one year [4]. Hence, considering a typical PV power plant lifespan of 20 years, such a PV system is capable of producing twenty times the amount of energy that was needed for its manufacturing, installation and lifetime operation.

For the reasons mentioned above, the PV technology has known an exponential growth in terms of installed power in the last decade, reaching more than $0.5\mathrm{TW_p}$ worldwide in 2018 (see Figure 1.1 (a)). Nevertheless, to keep making this technology more competitive, several challenges must be addressed with the aim of capping costs and increasing energy yield. With this in mind, all elements in the balance of system[3] (BOS) (e.g., inverter, junction boxes, installation equipment and etc.) are equally concerned.

1.2 Power Electronics for Photovoltaics

Although being the most known element in photovoltaics, the PV generator (or PV cell) is not the only fundamental component of a PV system. In reality, the voltage and current produced by a PV generator are DC quantities. Thus, to be able to inject power into the grid or feed an AC load, a DC-AC converter (or inverter) is often employed. Furthermore, due to its non-linear i–v characteristic[4], the PV cell presents a single maximum power point (MPP), which must be constantly tracked by the inverter to maximize energy yield during operation. In the literature, numerous maximum power point tracking (MPPT) techniques can be found [5], [6]. Since the PV voltage varies during the day according to the weather and cell's temperature conditions, the inverter is also responsible to dynamically ensure a constant RMS AC output voltage. PV inverters can be designed in single- and three-phase configurations. Due to the presence of a low-frequency (100Hz) fluctuating power component in single-phase systems, this inverter category is usually limited to a few kW and plays a minor role in the overall PV inverter market share [4] (mainly due to cost reasons). On the other hand, three-phase inverters account for more than 95% of the market share [4] and are the preferred solution in commercial and utility sectors [3].

When operating in grid-tied mode, the inverter must be able to: *i)* insure the DC-AC conversion with minimum power quality requirements [7]; *ii)* offer grid support injecting or absorbing reactive power, complying with grid codes and regulations [8]; *iii)* disconnect itself from the grid, when necessary (anti-islanding)

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[3] All PV power plant components and costs other than PV modules.

[4] The i–v characteristic of a PV cell depends mainly on the cell's temperature and weather conditions [5]. In its simplest electrical model, a DC current source in anti-parallel with a diode is often employed [5], [6].

[9] and *iv)* have the capability to ride-through low and high voltage grid fault events, complying with LVRT and HVRT requirements, respectively [10].

Figure 1.2 shows the basic architectures found in utility-scale PV power plants employing three-phase central and string inverter concepts.

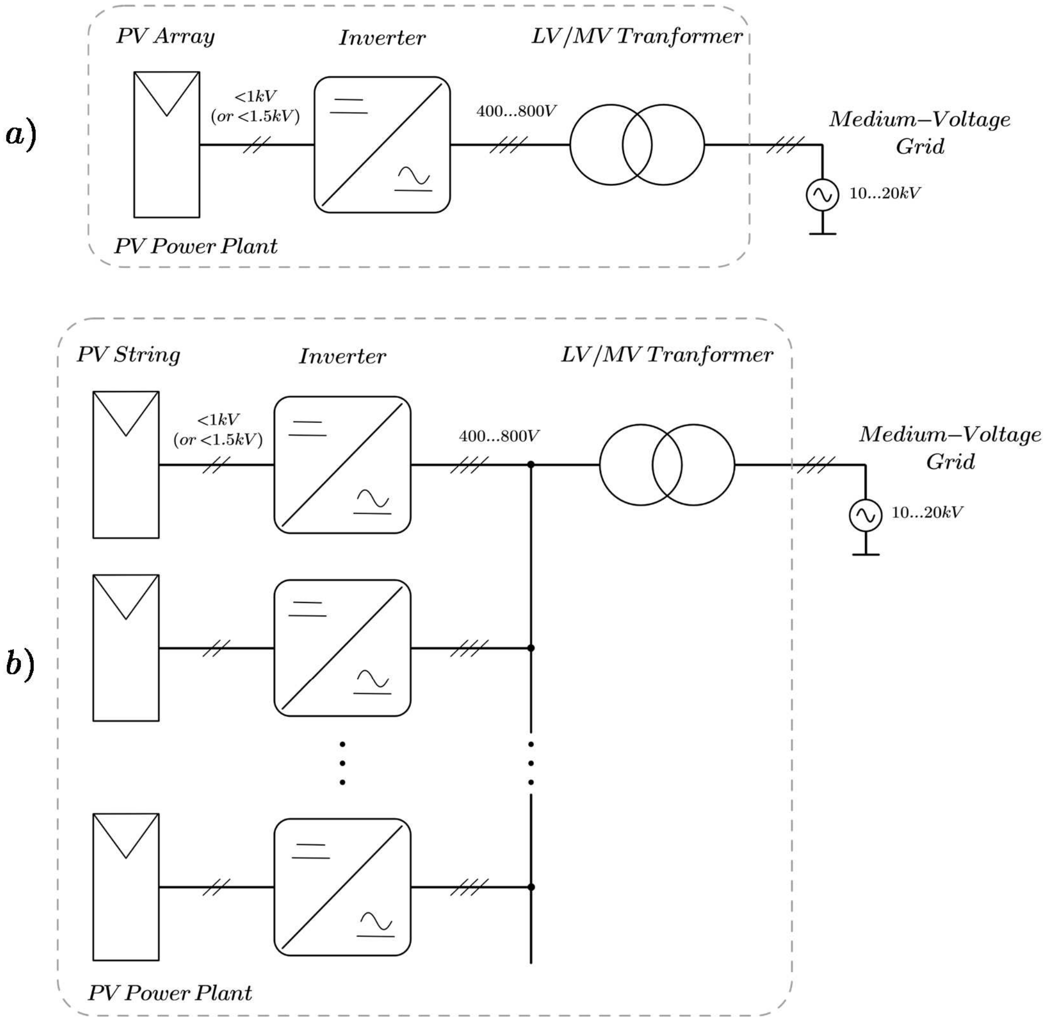

Figure 1. 2 – Basic PV power plant architectures employing three-phase a) central and b) string inverter concepts.

Considering the case of multi-MW central inverter, the PV strings are paralleled to obtain a single electricity-producing unit called PV array[5]. Diversely, with the string inverter concept, smaller generating units are employed and, not rarely, string inverters of up to 150kW presenting multi-MPPT inputs are used.

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[5] In the literature, some confusion exists between the terms array and string. As pointed out in [11] and employed in this work, string consists of a number of PV modules interconnected electrically in series to produce a given maximum operating voltage (V_{oc}) and array is an interconnected system of PV modules that function as a single electricity-producing unit. The modules are assembled as a discrete structure, with common support or mounting.

In both architectures, a low-voltage/medium-voltage (LV/MV) step-up transformer allows the PV power plant to be connected to the local MV grid.

Concerning the lifetime aspect of PV systems, there is a considerable gap between the typical lifespan of inverters (5 to 15 years [3], [12]) and that of PV panels (around 25 years [13]). From an operation and maintenance point of view, inverters are considered to be the weakest components in PV systems. In [14], it is reported that inverters were responsible for 37% of unscheduled maintenance events in a 50MW$_{\mathrm{p}}$ PV plant, accounting for 59% of the associated overall repair costs. In [15], similar results are presented about the high cost of inverter failures, which comprises not only the service cost itself, but also the energy losses due to the PV power plant downtime. When identifying the root causes of inverter reliability issues, power semiconductors and DC-link capacitors (often electrolytic type) represent the most common failure sources [16]. Taking all this into consideration, the improvement of PV inverter reliability remains a topic to be addressed in order to reduce operation and maintenance costs, as well as energy losses due to inverter downtime.

1.3 Research Motivations and Objectives

In Figure 1.3 is depicted a chart with three possible actions to be taken at the inverter design level to increase the energy yield and reduce costs of utility-scale PV power plants.

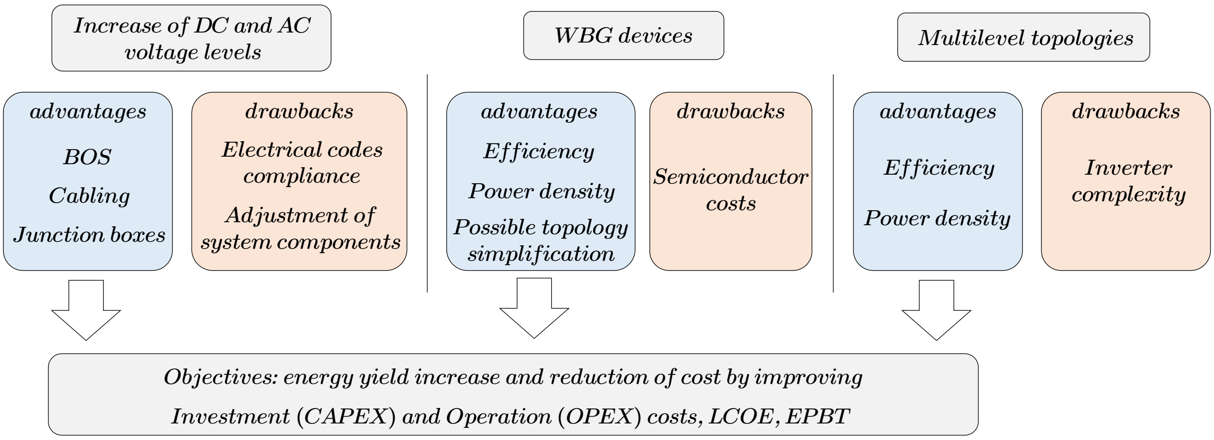

Figure 1. 3 – Possible actions to be taken at the inverter design level to increase the energy yield and reduce costs in large-scale PV systems.

A historical trend in PV systems is the progressive rise of the string voltage levels. In recent years, the first 1.5kV PV power plants have started operating [17]. When shifting from 1kV to 1.5kV strings, savings related to the initial PV plant investment costs (CAPEX) are possible (up to 4.5%) [17]. This cost reduction is mainly related to the BOS, thanks to the reduction of cabling cross-section and number of system components. On the other hand, the main drawbacks of higher string voltages (consequently grid voltages as well) relate to electrical codes compliance (not yet well stablished in some countries) and adjustment of existent materials and system components to higher DC voltages [17].

Another possible action to facilitate capping costs in PV domain is the implementation of wide-bandgap (WBG) semiconductors, especially Silicon Carbide (SiC) and Gallium Nitride (GaN) devices. Due to their superior physical and electrical properties, the efficiency of energy conversion systems can be sensibly improved, lowering PV LCOE. Thanks to their aptitude to operate at superior switching frequencies, the inverter power density can be increased, helping to reduce the PV plant mounting and shipment costs, for example. Furthermore, WBG devices present outstanding on-state characteristics, allowing the power electronic engineer to redesign and simplify standard converter topologies. For example, by reducing the number of active switches and the associated complexity, while improving reliability and possibly lifetime. However, the major drawbacks of such semiconductors are related to their early stage of technological maturity, leading to: *i)* relatively high cost, which might be overcome to some extent by massive-scale production and *ii)* reliability issues. Concerning SiC devices, the reliability-critical aspects have been reported to involve gate-oxide long-term reliability and stability [18], [19], operation under short-circuit and avalanche conditions [20] and power cycling capability [21], [22]. Countermeasures to some of these problems can already be found in the literature and involve improved semiconductor manufacturing processes and advanced packaging technologies.

A final possibility considered here to improve PV yield is the use of multilevel inverters. The associated advantages are similar to that of WBG devices, with exception to the possibility of simplifying the inverter system. In reality, the implementation of multilevel inverters often comes with the price of increasing semiconductor switch part count and complexity.

Having the chart of Figure 1.3 in mind, this Ph.D. project aims to redesign, based on WBG semiconductors, the standard DC-AC converter architecture in PV applications. With the purpose of suppressing the DC-link capacitors and simplifying the inverter topology, the single-stage three-phase Current Source Inverter (CSI) is proposed. Thanks to their compatible voltage rating levels together with exceptional on-state characteristics, Silicon Carbide (SiC) devices are employed in this work. Thereby, implementing the CSI topology with SiC devices brings the possibility to increase the grid voltage level, suppress the DC-link capacitors, reduce the switches part count and simplify the power stage topology. Each of these advantages and potentials limitations will be discussed in detail in the following chapters.

1.4 Dissertation Outline

Chapter 2 aims to present and analyze the most recent research advances in both academia and industry areas concerning the following aspects: *i)* state-of-the-art commercially available PV inverter topologies, *ii)* WBG devices in power electronic systems for performance improvement and *iii)* implementation of the CSI topology in PV applications. Thereby, the main research opportunities are identified.

In **Chapter 3**, the CSI principle of operation is discussed. This serves as the basis for the inverter semiconductor losses analyses. Particular attention is given to semiconductor conduction losses, since they represent one of the major CSI drawbacks. Besides the standard CSI switch configuration, other three variants found in the literature claiming to reduce conduction losses are compared, taking into account their advantages and limitations to operate with a PV generator. From this comparative study, a final CSI switching configuration is chosen, in order to be implemented in a new full-SiC power module in Chapter 4.

Chapter 4 covers the semiconductor power integration for CSIs. Initially, based on the topology specificities and the target PV application, attention is given to the design of a novel 1.7kV full-SiC power module. Then, all steps to an industrial realization of this new device are discussed – from the packaging material selection, passing by the substrate and housing layout designs to the choice of semiconductor bare dies. The second part of Chapter 4 is dedicated to the dynamic characterization of the developed SiC module. In this context, switching losses are obtained, providing the basis for the CSI design in the subsequent chapter.

In **Chapter 5**, the CSI validation is carried out through experiments at nominal power. For this purpose, a 60kW prototype employing the developed 1.7kV SiC modules is fully presented, together with the main design guidelines for passive elements and cooling system. Focus is given to the module's thermal aspects and efficiency at switching operation conditions. Thus, the developed

60kW CSI prototype is characterized using both electrical and calorimetric methods.

Finally, **Chapter 6** summarizes the main research achievements and conclusions presented in this dissertation. Also, future research areas are identified and discussed accordingly.

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Chapter 2

State of the Art Review

With the purpose of placing the Ph.D. project objectives with regard to the cutting edge research advances in power electronics, a literature review is carried out in this chapter. Starting from common PV inverter topologies and their associated drawbacks, the implementation of wide-bandgap (WBG) devices in combination with the single-stage three-phase Current Source Inverter (CSI) is proposed. With such a solution, PV inverter's complexity could be reduced while increasing performances. Due to their higher blocking voltage rates, focus is given to SiC devices in this work. Then, a review of CSI for PV applications is presented and a more detailed analysis on the potentials of the proposed SiC-based CSI for performance improvement is carried out. Finally, the chapter summarizes the main research challenges and opportunities.

2.1 Review of Three-phase Photovoltaic Inverter Topologies

PV inverters are normally voltage source-based converters [1], [2] and can be classified with regard to their number of power processing stages. Thereby, two main categories arise, namely single-stage and multistage inverters [2]. In Figure 2.1 (a) and (b) are depicted, respectively, the block diagram of a three-phase single- and two-stage inverter topologies.

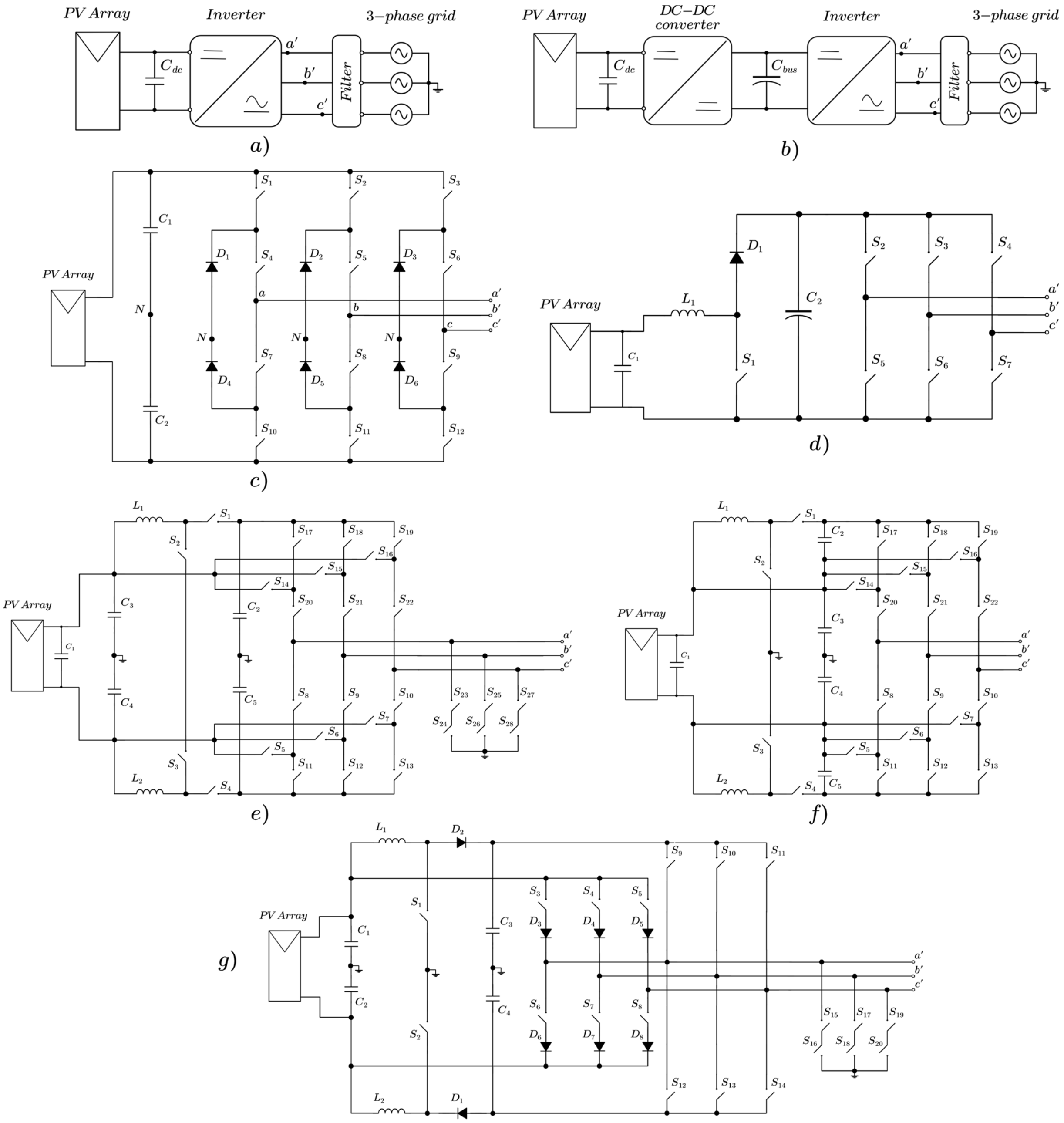


Figure 2. 1 – Three-phase inverter block diagram for a) single-stage and b) two-stage architectures. c) Single-stage three-phase NPC inverter. Two-stage three-phase architectures: d) boost + VSI, e) symmetric boost + 5-level VSI, f) symmetric boost + 4-level VSI and g) symmetric boost + 5-level TCC VSI.

As can be seen, in the two-stage inverter topology, a DC-link capacitor bus (C_{bus}) is implemented in order to respect the interconnection rule of sources and limit the DC voltage ripple [3]. For these purposes, electrolytic capacitors are often employed, thanks to their good compromise between energy density and costs [4]. Nevertheless, as mentioned in § 1.2, these components are often associated to high failure rates in field operation [5], [6]. On the other hand, the DC filter capacitor (C_{dc}) – present in both inverter categories – serves to stabilize the PV voltage, helping to perform the MPPT. C_{dc} represents minor reliability issues, since it is often of small value and then realized through metallized polypropylene film capacitors (known to have superior reliability performances [4]). The choice for a supplementary power processing stage is justified, in many cases, by the wider input DC voltage range (i.e., MPP voltage range) [2], which facilitates the PV power plant design [7] and increases energy yield.

With the rapid growth of photovoltaics in recent years, several companies have joined the market, making available a vast range of PV inverter systems, featuring different topologies and characteristics [8]. In Figure 2.1 are depicted some of these commercial three-phase PV inverters. In greater detail, Figure 2.1 (c) shows an example of a single-stage topology, the Neutral Point Clamped (NPC) inverter [1]. Figures 2.1 (d), (e), (f) and (g) present multistage converters, respectively, boost + 2-level Voltage Source Inverter (VSI) [8], e) symmetric boost + 5-level VSI [9], f) symmetric boost + 4-level VSI [10] and g) symmetric boost + 5-level VSI with 3-level camping cell (TCC) [11]. These topologies are found in a large power range (from a few tens of kW to more than 1MW), featuring single or multi MPPT inputs. Although not extensive, from Figure 2.1, the common aspects usually shared by PV inverters become clear: they all implement multilevel and/or multistage topologies. Thereby, an increase of the device's part count (i.e., number of semiconductor switches, gate driver units, voltage/current sensors and etc.) as well as the converter complexity is inevitable.

In the light of this, next section discusses the implementation of WBG devices (especially SiC devices) in power electronic systems for performance improvement, i.e., reduction of the converter's complexity and increase of power density and efficiency.

2.2 SiC vs. Si – Potentials of Wide-bandgap Devices for Performance Improvement in Energy Conversion Systems

2.2.1 Brief Overview of WBG Materials and Properties

Since the development of solid-state electronics in the 1950s, Silicon (Si) has been the most commonly used semiconductor material in energy conversion systems. Today, thanks to its advanced maturity level, innovative breakthroughs are rarely achieved with this technology [12]. Thus, in order to keep improving the performance of power electronic converters, alternative semiconductor materials are of interest, especially those presenting wider bandgaps. Among the most developed WBG materials are Silicon Carbide (SiC) and Gallium Nitride (GaN). Table 2.1 presents the main physical properties of these WBG semiconductors. For comparison, Si properties are presented as well. Due to their blocking voltage rating limitation (typically <650V), GaN devices are not the focus of this work.

Table 2. 1 – Main physical properties of semiconductor materials [13], [14].

Property	Symbol (unit)	Si	4H-SiC [1]	GaN [2]
Bandgap	$E_G\ (eV)$	1.1	3.26	3.45
Relative dielectric const.	$\varepsilon_r\ (-)$	11.8	9.6	9.0
Breakdown electric field	$E_{crit}\ (MV/cm)$	0.3	3.0	5.0
Thermal conductivity	$\lambda\ (W/K.cm)$	1.5	4.9	1.3
Melting temperature	$T_m\ (°C)$	1420	2830	-
Electron mobility	$\mu_n\ (cm^2/V.s)$	1500	1140	1250
Hole mobility	$\mu_p\ (cm^2/V.s)$	480	50	850
Baliga's FOM [3]	FOM_B (relative to Si)	1.0	554	188

1) Only 4H-SiC polytype is considered here, since it is the most common choice for power devices due to its relatively good manufacturability and superior physical properties [15]. 2) Properties of GaN material and not that of HEMT GaN [14]. 3) FOM_B defines the material efficiency to minimize conduction losses for unipolar devices.

When designing high-voltage power semiconductors, one of the major material properties to consider is the critical electric field strength (E_{crit}). The E_{crit} for SiC is ten times higher than that for Si. The higher breakdown level is the main parameter which allows SiC-based devices to drastically reduce specific on-state resistance ($R_{on,sp}$). Taking the case of unipolar devices, by simply shifting from Si to SiC, a drift-layer resistance reduction of two to three orders of magnitude is possible at any blocking voltage level [12]. Otherwise, for a given current rating, SiC devices tend to present much smaller active chip area than their Si counterparts. This analysis is supported by the Baliga's figure of merit (FOM_B in Table 2.1), which defines the material efficiency to minimize conduction losses for unipolar devices.

Concerning the comparison of switching behaviors for Si- and SiC-based devices, this should be done carefully. When compared to Si-based bipolar switches (e.g., insulated gate bipolar transistor – IGBT), the faster switching behavior of SiC unipolar devices (e.g., metal-oxide-semiconductor field-effect transistor – MOSFET) must not be only attributed to the SiC material itself. In reality, due to the absence of minority carrier storage of unipolar structures, their switching transition is only dependent of the device's parasitic capacitances. This is typically not the case for IGBTs, no matter the employed material (Si or SiC). Nevertheless, if comparing, for example, a given bipolar device based on Si and SiC, the later will present faster switching transient [12]. Thanks to the high SiC E_{crit}, a thinner blocking-voltage layer can be implemented, leading to less overall stored charges during operation.

Another key factor for performance improvement often related to SiC utilization is the material aptitude for operating at elevated temperatures (>500°C). Indeed, the SiC material properties are well suitable for this purpose, since its thermal conductivity, melting point and chemical stability are sensibly better than those of Si [12]. However, when taking into account realistic power application conditions, thermal runaway is likely to occur if junction temperatures exceed a certain threshold – due to carrier mobility degradation with temperature [16]. From the integration perspective, packaging reliability represents another bottleneck for high-temperature operation [17].

For deeper discussion on SiC technology and properties, the reader is invited to consult the following references: [15], [18], [19].

2.2.2 SiC-based Semiconductor Devices

Since 2001, when the first SiC device (the Schottky barrier diode – SBD) was introduced in the market by Infineon, much progress has been done in terms of device's structure and process optimization. Nowadays, most of SiC diodes present a merged pin-Schottky (MPS) structure and SiC trench MOSFET structures are not rarely employed. Figure 2.2 presents the basic structures found in state-of-the-art SiC diodes and MOSFETs.

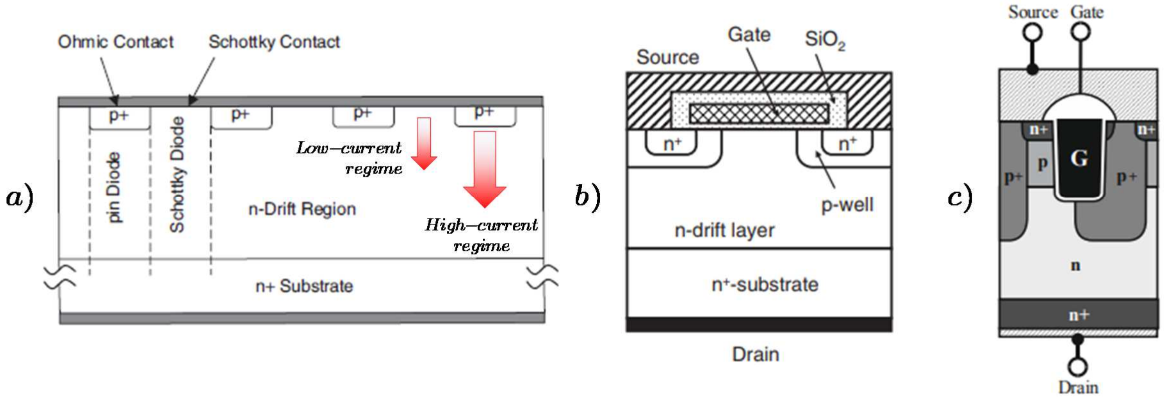


Figure 2. 2 – a) Structure of MPS diode (source: modified from [15]), b) DMOSFET (source: modified from [12]) and c) trench MOSFET with asymmetrical channel (source: modified from [20]).

The MPS diode, presented in Figure 2.2 (a), is a structure that combines the advantages of both pin and Schottky diodes, featuring no reverse recovery characteristic under nominal operation, improved surge current capability and low reverse-bias leakage-current [15], [18]. Thanks to the interdigitated Schottky and highly-doped p-type regions, the device presents two distinct operating behaviors. At nominal forward current condition, the p$^+$ regions are not triggered and the device acts as a standard unipolar SBD. On the other hand, at high-current events (e.g., surge current), the p$^+$ regions start to inject carriers acting then as a bipolar device, reducing the on-state losses and giving a supplementary surge capability margin. Figure 2.2 (b) and (c) presents the common MOSFETs structures employed by manufacturers Wolfspeed and Infineon, respectively. Due to the smaller cell pitch featured by SiC MOSFETs (thanks to the higher E_{crit}), their gate-oxide (SiO$_2$) structure is more prone to suffer from high electric field gradients, possibly degrading long-term reliability. Furthermore, the low electron mobility at the SiC/SiO$_2$ interface (due to interface defects) represents a challenge to threshold voltage ($V_{gs,th}$) stability [20]. Having in mind the object of improving the channel mobility (to reduce $R_{on,sp}$, increasing then wafer yield) while not degrading long-term reliability aspects, manufacturers have been improving their processes and developing their own specific device structures.

Figure 2.3 presents the major SiC device manufacturers and their commercially available components at the time of the present work. Manufactures which do not commercialize their SiC devices, such as GE, are not considered in this chart. As can be seen, all manufacturers, except for United Silicon Carbide, concentrate their efforts on the development of SiC MOSFETs and SBDs, especially for low-voltage applications (600-700V) and 1.2kV. The progressive migration to higher blocking voltages, i.e., 1.7kV, can also be seen.

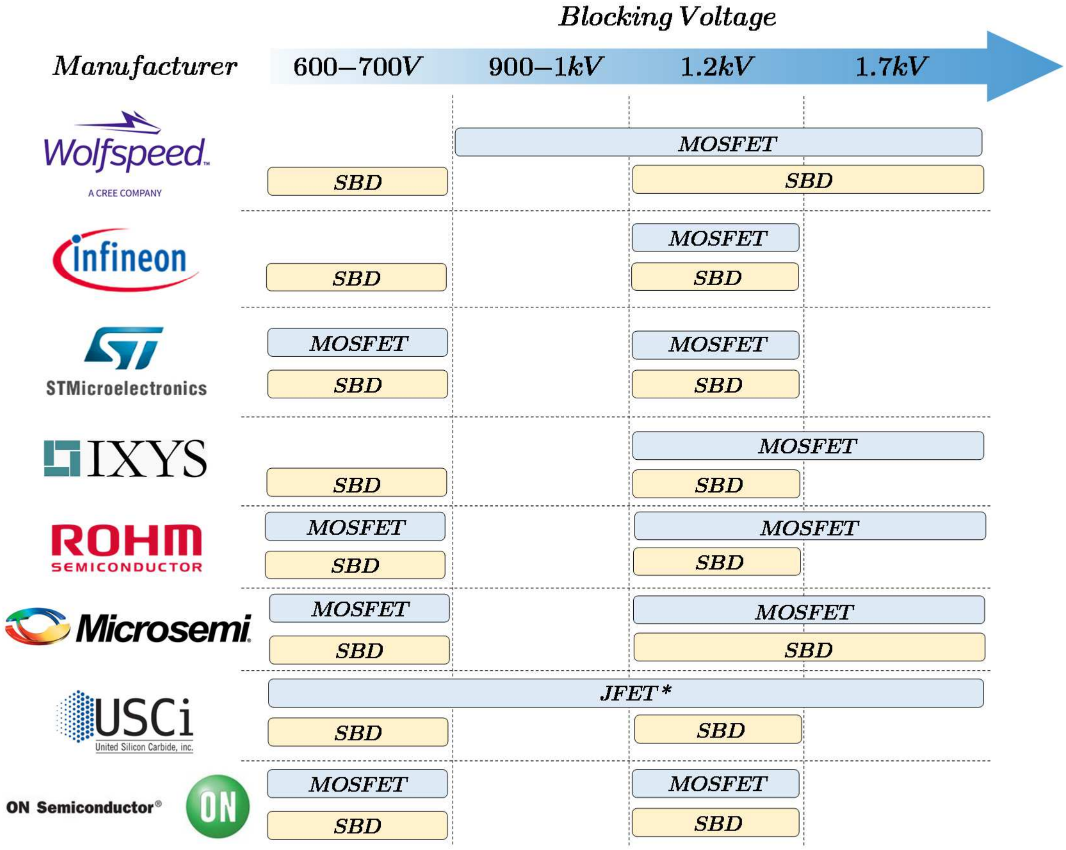
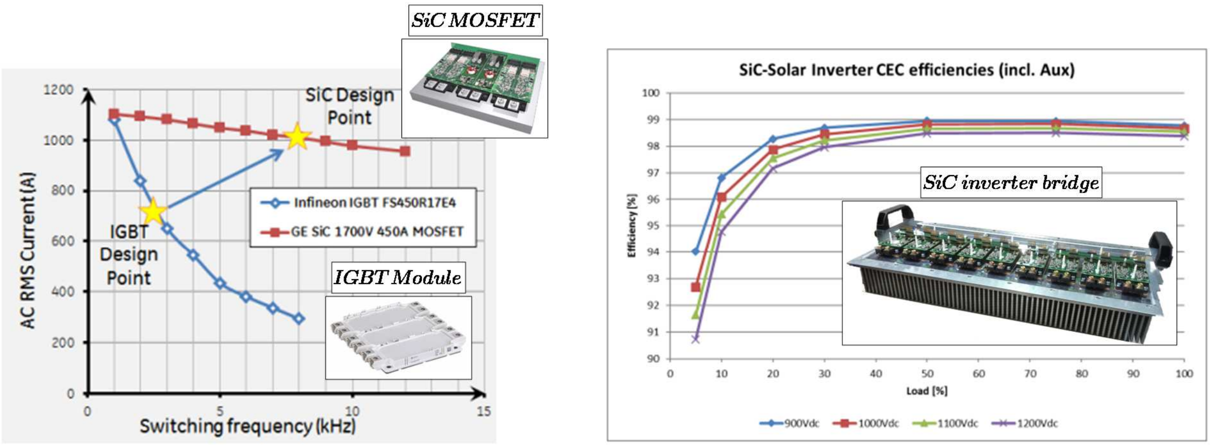


Figure 2. 3 – Major SiC device manufacturers and their commercially available components. *normally-on and -off devices are included. Source: modified and updated from [17].

2.2.3 SiC Devices for Inverter Performance Improvement

Given the superior SiC properties discussed in the previous sections, a typical example is presented here concerning the performance improvement of inverters through SiC implementation. Figure 2.4 depicts the performance of a 2.5MW SiC-based PV central inverter [21]. Originally, such PV application employed 1.7kV Si-based IGBTs operating at 2.6kHz in a VSI configuration (number of levels not specified in [21]). Due to the relatively high semiconductor losses, water-cooling system was implemented.



a) *b)*

Figure 2. 4 – a) Output current derating as a function of the switching frequency when employing Si IGBTs and SiC MOSFETs modules and b) inverter efficiency at different input voltages and three-phase bridge mounted on air-cooled heatsink. Source: modified from [21].

From Figure 2.4 (a), one concludes that, in its SiC version, the PV inverter is capable of operating at much higher switching frequencies without strongly penalizing the output power (due to devices' junction temperature limit), which is notably not the case when employing Si IGBTs. Also, a 25°C additional junction temperature margin is obtained with the SiC modules. Concerning the new selected switching frequency ($F_{sw,SiC}$), it is set to be 8kHz, i.e., $F_{sw,SiC} = 3 \cdot F_{sw,Si}$. However, at the highest possible switching frequency operating point $F_{sw,SiC} = 10 \cdot F_{sw,Si}$. Thanks to semiconductor losses reduction (up to 50%), the SiC-based inverter is now air-cooled, allowing to reduce thermal cooling system complexity and increase power density. With regard to the new achieved efficiency, the SiC inverter has shown to be capable of operating with 99% efficiency at lower input voltage levels (900V). To summarize, when replacing the Si-based semiconductors by their SiC counterparts, increased switching frequency, efficiency and power density were achieved together with important cooling system simplification.

2.3 Three-phase Current Source Inverter for Photovoltaic Applications: a Single-stage Topology as an Alternative Solution to Voltage Source-based Converters

Historically, Current Source Converters (CSCs) have been employed in energy conversion systems since the early 1960s and 1970s, for HVDC and motor drive applications, respectively [22]. Nonetheless, in recent years, a growing number of scientific papers have proposed the use of CSCs in a large variety of systems, ranging from power factor correction rectifiers [23], [24] to renewable energy source integration to the grid [25]–[29]. Due to the high level of conduction losses in the CSC [23], this topology is not rarely out of consideration, as long as semiconductors presenting good on-state characteristics are employed (e.g., in higher voltage applications, by using bipolar devices as IGBTs). However, as discussed in § 2.2.1, their intrinsic charge storage characteristic make their switching behavior slower and the presence of tail current and turn-off recovery (e.g., for pin diodes) is inevitable. Consequently, to cap switching losses within reasonable boundaries, the designer has no choice but to limit the switching frequency, resulting in a bulky and expensive DC-link inductor. In view of these facts, Voltage Source Converters (VSCs) have historically been preferred over CSCs in most cases. Nevertheless, the recent advances in power electronic semiconductors (especially concerning WGB devices) have made possible to improve the performances of CSCs by reducing conduction losses and increasing switching frequency at the same time. Thereby, making the CSC a compelling solution to standard VSCs. That represents one of the main reasons behind the emerging research interest on CSC-related topics.

Having in mind the research motivations and objectives discussed in § 1.3, this Ph.D. project aims to evaluate the potentials of the single-stage three-phase SiC-based Current Source Inverter in photovoltaic applications. The adopted CSI power range is that of a typical string inverter (around 60kW). Figure 2.5 illustrates the three-phase PV CSI operating with the grid.

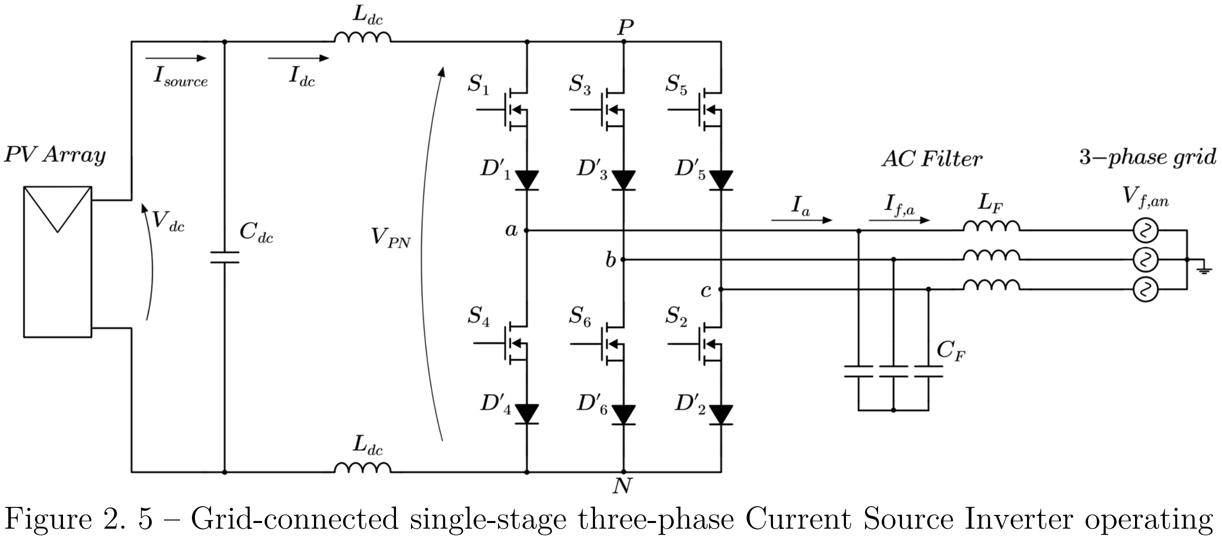


Figure 2. 5 – Grid-connected single-stage three-phase Current Source Inverter operating with a PV array.

In the literature, the CSI utilization as grid interface for photovoltaics has been investigated in a few research works, especially for low power PV applications, i.e., limited to a few kW. In the following, the most relevant works are summarized and discussed.

In [29], [30], a 250W three-phase CSI is proposed to operate as grid interface for PV modules. By directly integrating the microinverter on the PV module's backside, an "AC module" results, being capable of directly injecting power into the 400V grid. Figure 2.6 (a) depicts the final CSI inverter and the AC module. Due to absence of galvanic insulation, a special modulation strategy has been developed, in order to minimize common mode earth leakage currents at the PV module level. Note that this issue is not found in utility-scale PV plants, thanks to the LV/MV transformer (see Figure 1.2). In terms of efficiency, three different semiconductor configurations are analyzed under 25kHz switching operation, leading to a maximum European Efficiency[6] (η_{euro}) of 95.8% when employing 900V MOSFETs and SiC series diodes. As claimed by the authors, the CSI implementation approach might increase the PV reliability, thanks to its single-stage approach and elimination of electrolytic capacitors.

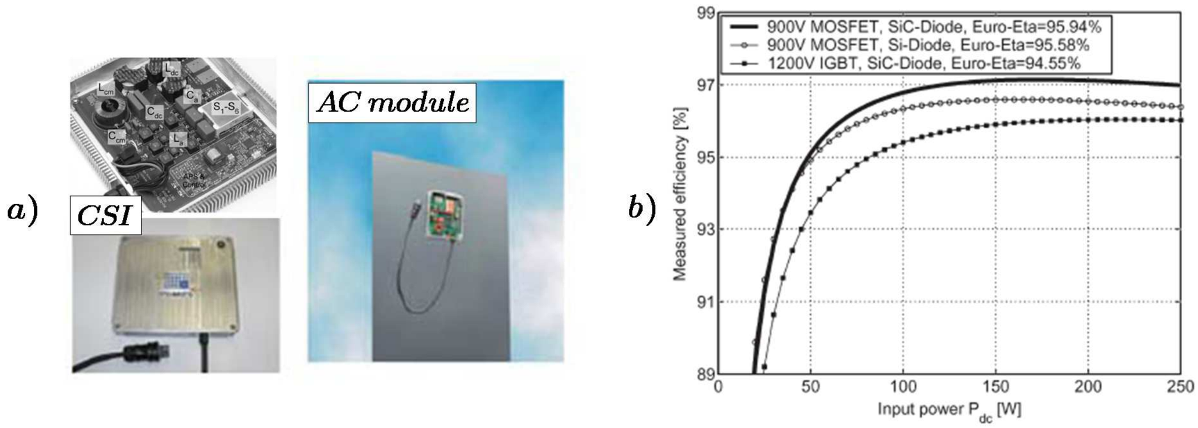


Figure 2. 6 – a) CSI prototype and "AC PV module" with integrated inverter on the backside and b) efficiency results. Source: modified from [30] and [29].

Another interesting CSI implementation is presented in [25], where the switch configuration is chosen to be based on SiC MOSFETs in synchronous rectification mode. Thus, a 5kW three-phase PV CSI is developed to operate with the 400V grid. Figure 2.7 presents the CSI prototype and its efficiency. In the referred work, the switching frequency is 145kHz, in order to fulfill conducted emissions requirements with reasonable filtering efforts. Then, the intrinsic low level of the full-SiC CSI switching losses is put in evidence in the paper. As demonstrated through losses calculations, the operation at 300kHz with relatively high η_{euro} (>97.5%) is also possible, especially with devices integrated in D^{2}PAK

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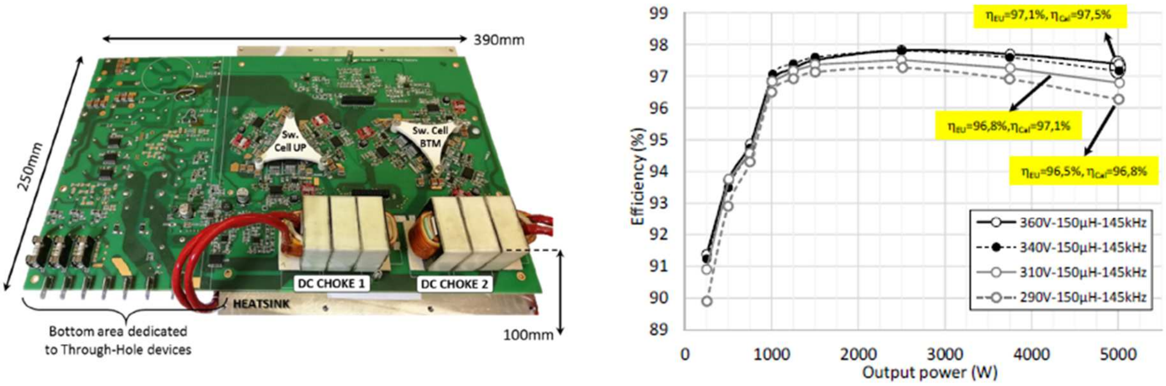
[6] The European Efficiency is calculated from the efficiency average over a given power distribution (power range) corresponding to the operating climatic conditions of a central European location, where: $\eta_{euro} = 0.03 \cdot \eta_{5\%} + 0.06 \cdot \eta_{10\%} + 0.13 \cdot \eta_{20\%} + 0.1 \cdot \eta_{30\%} + + 0.48 \cdot \eta_{50\%} + 0.2 \cdot \eta_{100\%}$.

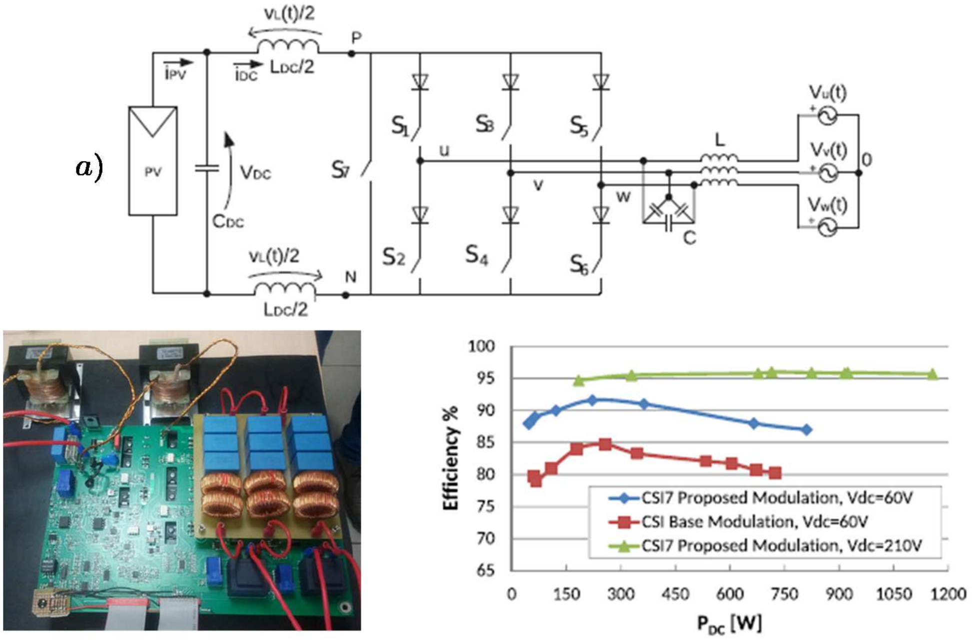
packaging (thanks to the reduced parasitics). As pointed out by the authors, the CSI equipped with latest generation SiC devices represents a compelling alternative to standard VSIs. Furthermore, thanks to its low switching losses, the CSI topology represents a good candidate for high-power density applications.



a) *b)*

Figure 2. 7 – a) CSI prototype and b) efficiency results. Images courtesy of [25].

In [26], a modified CSI topology, named CSI7, is proposed for PV applications (cf. Figure 2.8 (a)). With the aim of reducing conduction losses, an additional switch (S_7) is added to the traditional CSI bridge. Thus, during the freewheeling phases (or zero vector application times), the DC current flows uniquely through S_7. In general terms, the CSI7 is particularly interesting when a high voltage step-up ratio (G_V) between the PV array and the grid is required, since greater G_V ratios lead to longer freewheeling phases.



b) *c)*

Figure 2. 8 – a) CSI7 topology, b) developed prototype and c) efficiency results. Source: modified from [26].

Figure 2.8 presents the CSI prototype employing 1.2kV Si IGBTs and the obtained efficiency curves. Another important CSI7 advantage is related to common mode earth leakage currents, which can be reduced when implementing specific modulation techniques.

Taking into consideration all the elements presented in this chapter, if compared to multistage and/or multilevel voltage source-based structures, the SiC-based Current Source Inverter for PV applications might bring the following benefits:

- Reduced device's part count (number of switches, associated gate driver units, current/voltage sensors);
- Reduced complexity, thanks to the single power processing stage;
- Potentially improved reliability, thanks to the elimination of DC-link capacitors and reduced complexity; and
- Potentially higher efficiency, thanks to the single power processing stage;
- Potentially higher power density, thanks to the fast switching behavior of unipolar SiC devices in combination with the inherent CSI low level of switching losses.

2.4 Research Challenges and Opportunities

The main research challenges and opportunities are listed as follows:

- Very few research on power integration/packaging for WBG-based CSC applications has been reported in the literature. As far as the author is aware, only one work deals with the realization of a SiC-based power module laboratory prototype intended for CSC applications [31];
- Since VSCs are the predominant topology in most applications today, there is a lack of CSC adapted components, as gate drivers and related protections;
- Implementation of SiC devices with minimum parasitics, in order to take full advantage of their properties;
- Characterization of SiC devices presenting fast switching transients;
- Investigation and minimization of CSI losses, mainly conduction losses, for efficiency improvement considering PV operating conditions; and
- Challenges related to the practical implementation and characterization of a medium-power (60kW) SiC-based CSI.

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Chapter 3

Three-phase Current Source Inverter Topology

In this chapter, the Current Source Inverter (CSI) topology is introduced. Firstly, its principle of operation is presented implementing space vector transformation. From that, the CSI switching cells arrangement is analyzed together with their main switching losses mechanisms. Since conduction losses represent one of the major CSI drawbacks, particular attention is given to this topic. Therefore, the mechanisms of on-state losses for SiC MOSFETs and diodes are studied in detail. Besides the standard CSI switch configuration, other three variations found in the literature claiming to reduce conduction losses are compared, taking into account their advantages and limitations to operate with a photovoltaic string. Finally, the topological duality between Voltage Source and Current Source Converters is explored in order to implement an analytical method for the AC line current spectrum determination.

3.1 Introduction

The three-phase Current Source Inverter (CSI) topology is depicted in Figure 3.1. The inverter bridge is composed of six current-unidirectional switches with reverse voltage blocking capability ($S_{1..6}$, $D_{1..6}$). On the DC side, a DC-link choke (L_{dc}) ensures the converter's current-source based characteristic and a filtering capacitor (C_{dc}) is normally added in order to attenuate the current ripple in the DC source (I_{source}) and to stabilize its voltage (V_{dc}). On the other hand, the CSI bridge is connected to the mains through a three-phase C-L filter (C_F, L_F). The presence of C_F guarantees the mains instantaneous voltage source behavior - allowing the interconnection of DC and AC sources - and is responsible for filtering the AC line current (I_a), together with the line inductor (L_F). With an appropriate control, the CSI is capable of injecting sinusoidal current waveforms ($I_{f,a}$) into the grid.

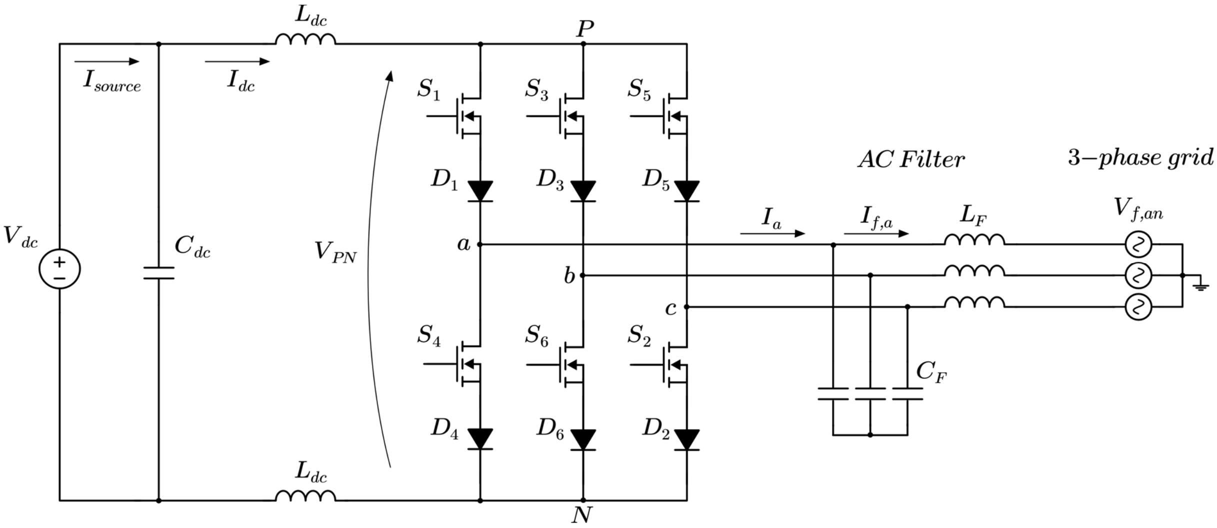
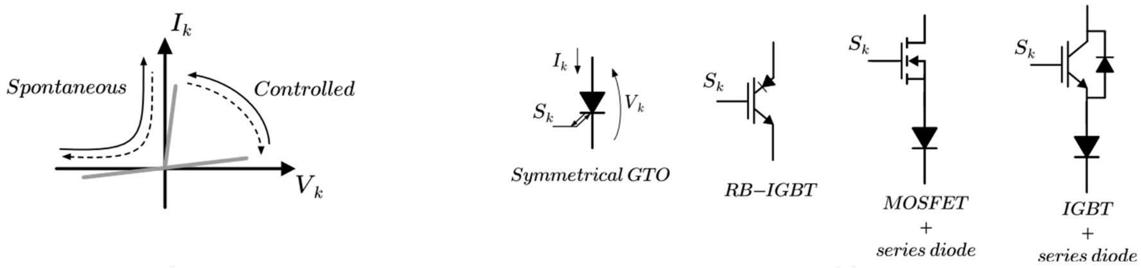


Figure 3. 1 – Three-phase Current Source Inverter topology.

In this work, Pulse Width Modulation (PWM) technique is employed. For that reason, the use of fully controlled turn-on and turn-off switches is required [1]. Figure 3.2 shows the idealized $i-v$ characteristic for the CSI power devices, as well as four possible switch realizations. Considering the case where the voltage bidirectional device is made out of a serial connection of an IGBT and a diode, the need for an IGBT anti-parallel diode should be pointed out. Although it does not conduct any current, this additional diode is necessary since IGBTs are not designed to withstand reverse voltages [2]. Diversely, if MOSFETs are employed, any anti-parallel device is needed, thanks to the intrinsic body-diode presence within the MOSFET structure.



a) b)

Figure 3. 2 – a) Idealized $i - v$ characteristic for CSI power devices and b) possible switch realizations.

3.2 Principle of Operation

For the CSI analysis, a simplified circuit representation is shown in Figure 3.3, where:

- V'_{S_i} and I'_{S_i} , $i \in [1,2,\dots,6]$ are the instantaneous S'_i switch blocking voltage and current, respectively;
- V_{PN} and $I_{a,b,c}$ are the modulated instantaneous DC voltage and line currents, respectively; and
- $V_{f,a,b,c,n}$ are instantaneous line-to-neutral voltages defined by

$$\begin{aligned} V_{f,an} &= \hat{V}_{f,l-n} \,.\cos(\omega t + \varphi) \\ V_{f,bn} &= \hat{V}_{f,l-n} \,.\cos(\omega t - 120° + \varphi) \\ V_{f,cn} &= \hat{V}_{f,l-n} \,.\cos(\omega t + 120° + \varphi) \end{aligned} \tag{3.1}$$

where $\hat{V}_{f,l-n}$ is the peak value of the fundamental line-to-neutral voltage and φ the grid phase displacement power factor (DPF) angle.

In order to properly control the CSI switches, two conditions must always be met, independently of the adopted PWM technique: *i)* the DC current (I_{dc}) flow should not be interrupted, i.e., at least one high-side (HS) switch (S'_1,S'_3,S'_5) and one low-side (LS) switch (S'_4,S'_6,S'_2) must be on at any time and *ii)* the line currents ($I_{a,b,c}$) should be defined by the modulation pattern and not by the load conditions, i.e., at most one HS switch and one LS switch must be on at any time [3]. Considering that, one single operation constraint can be stated as follows: at any instant of time, only one high-side switch (S'_1,S'_3,S'_5) and one low-side switch (S'_4,S'_6,S'_2) must be on – excluding commutation (overlapping) intervals [1], [3], [4].

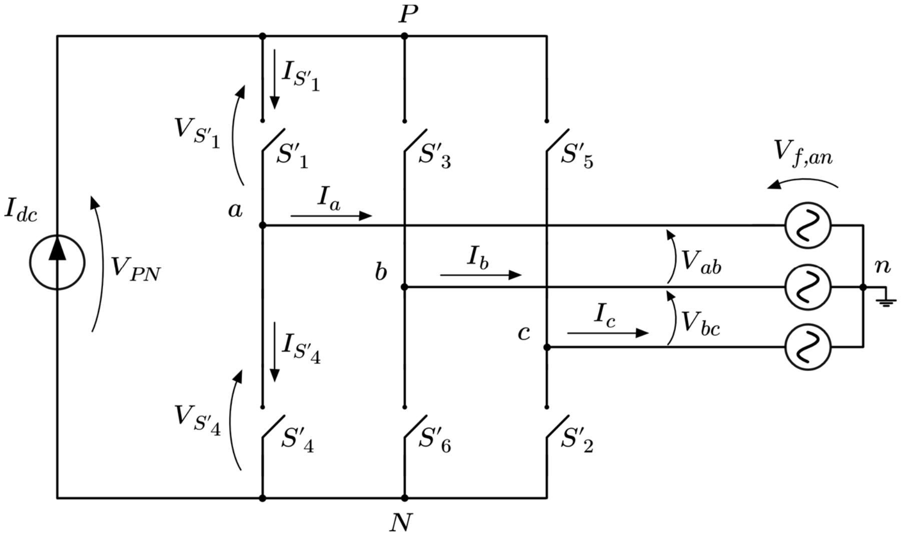


Figure 3. 3 – Simplified representation of the three-phase CSI. Herein, the switches are considered to be ideal and they are divided into two groups: high-side switches (S'_1, S'_3, S'_5) and low-side switches (S'_4, S'_6, S'_2).

Due to the discontinuous behavior of voltages and currents in PWM converters, the notion of binary switching function can be employed [1], [5]. Herein, the switches are assumed to be ideal, since no device's voltage drop neither leakage current exist during the on- and off-state, respectively. Furthermore, the transition from one state to another is made instantaneously.

Hence, an independent switching function can be defined for each switch, as follows:

$$f_i = \begin{cases} 1, & if\ S'_i\ is\ on \\ 0, & if\ S'_i\ is\ off \end{cases} \quad \text{where} \quad i \in [1,2,\ldots,6] \tag{3.2}$$

Then, from the unified operation constraint previously stated and considering the high-side group of switches, one can write:

$$f_1 + f_3 + f_5 = 1 \tag{3.3}$$

The same is valid for the low-side group, so that

$$f_4 + f_6 + f_2 = 1 \tag{3.4}$$

The switching currents are associated with the DC current source by

$$I_{S'_i} = f_i\, I_{dc} \tag{3.5}$$

Summing the currents in nodes *a*, *b* and *c*, the line currents can be written as follows:

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} f_1 & f_4 \\ f_3 & f_6 \\ f_5 & f_2 \end{bmatrix} \begin{bmatrix} I_{dc} \\ -I_{dc} \end{bmatrix} \qquad (3.6)$$

Using Eq. 3.2 and analyzing the high-side voltage loops, one can define the voltage across the switch S'_1 as

$$V_{S'_1} = (f_1 - 1)V_{f,an} + f_3\, V_{f,bn} + f_5\, V_{f,cn} \qquad (3.7)$$

In a similar way, Eq. 3.3 is used to define the switch S'_4 blocking voltage:

$$V_{S'_4} = (1 - f_4)V_{f,an} - f_6\, V_{f,bn} - f_2\, V_{f,cn} \qquad (3.8)$$

Knowing that $V_{PN} = V_{S'_1} + V_{S'_4}$, the DC voltage becomes

$$V_{PN} = (f_1 - f_4)V_{f,an} + (f_3 - f_6)V_{f,bn} + (f_5 - f_2)V_{f,cn} \qquad (3.9)$$

With the equations defined above, the following observations can be made:

- for a given I_{dc} operating point, the switching current $I_{S'_i}$ in a CSI is always a constant value and equal to I_{dc} (cf. Eq. 3.5);
- the switching voltage $V_{S'_i}$ is a function of the grid voltage and is then sinus modulated (cf. Eq. 3.7); and
- the line currents can only assume three discrete values $I_{a,b,c} \epsilon [-I_{dc}, 0, +I_{dc}]$ (cf. Eq. 3.6).

The operation constraint of having one HS switch and one LS switch conducting at any time instant leads to nine CSI valid switching combinations (or states), which are summarized in Table 3.1.

Table 3. 1 – Switching states and Space Vectors.

State	On-state switches	I_a	I_b	I_c	Space Vector (normalized to I_{dc})
1	$[S'_1, S'_2]$	I_{dc}	0	$-I_{dc}$	$\overrightarrow{I_1} = 1 + j0.577$
2	$[S'_2, S'_3]$	0	I_{dc}	$-I_{dc}$	$\overrightarrow{I_2} = j1.155$
3	$[S'_3, S'_4]$	$-I_{dc}$	I_{dc}	0	$\overrightarrow{I_3} = -1 + j0.577$
4	$[S'_4, S'_5]$	$-I_{dc}$	0	I_{dc}	$\overrightarrow{I_4} = -1 - j0.577$
5	$[S'_5, S'_6]$	0	$-I_{dc}$	I_{dc}	$\overrightarrow{I_5} = -j1.155$
6	$[S'_6, S'_1]$	I_{dc}	$-I_{dc}$	0	$\overrightarrow{I_6} = 1 - j0.577$
7	$[S'_1, S'_4]$	0	0	0	$\overrightarrow{I_7} = 0$
8	$[S'_3, S'_6]$	0	0	0	$\overrightarrow{I_8} = 0$
9	$[S'_5, S'_2]$	0	0	0	$\overrightarrow{I_9} = 0$

Among all valid switching states, 1,2,…,6 are defined as active states since power is transferred to the mains, i.e., $I_{a,b,c} \neq 0$. On the other hand, 7, 8 and 9 are defined as zero states, given that I_{dc} is bypassed and no current is transferred to the mains.

3.2.1 Space Vector Transformation

Assuming that the CSI generates a three-phase balanced set of line currents, where $I_a(t) + I_b(t) + I_c(t) = 0$, each switching state can be expressed as a stationary complex vector ($\vec{I}_{1..9}$) in the $\alpha - \beta$ plane [3]–[5]. In the same way, the desired set of line currents can be represented as a rotating complex reference vector ($\vec{\imath}_{ref}$) in the aforementioned plane. This space vector transformation – firstly proposed for the analysis of electric machines in the 1920s – has been widely used in modern Power Electronics systems to numerically implement PWM techniques [6].

To derive the CSI space vectors, one can apply Eq. 3.10 to each valid switching state, as follows:

$$\vec{I}_{1..9} = i_\alpha + j i_\beta = \frac{2}{3}\left(I_a e^{j0} + I_b e^{j2\pi/3} + I_c e^{j4\pi/3}\right) \tag{3.10}$$

As a result, six active vectors and three zero vectors are obtained (cf. Table 3.1). In the $\alpha - \beta$ plane, the region between two adjacent active vectors is referred as a sector. In Figure 3.4, all valid vectors and sectors are presented.

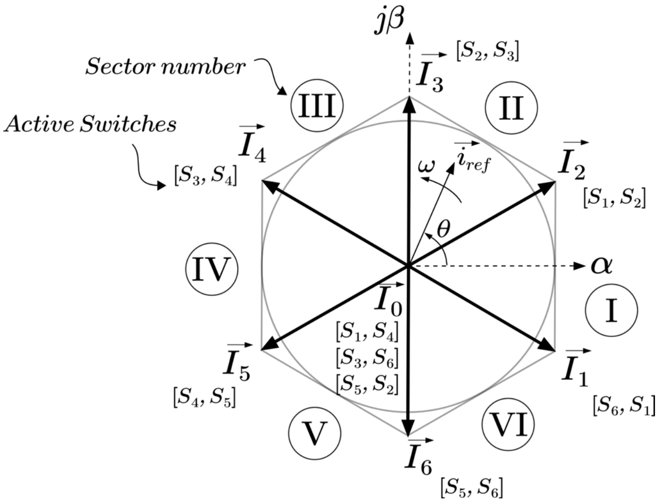


Figure 3. 4 – Space vector diagram and $\alpha - \beta$ plane.

It is important to note that $\vec{\imath}_{ref} = |\vec{\imath}_{ref}|e^{j\theta}$ rotates with an angular velocity of $\omega = 2\pi f$, where f is the fundamental grid frequency (e.g., 50Hz). Furthermore, it is related to the modulation index by

$$M = \frac{\left|\vec{\imath}_{ref}\right|}{I_{dc}} = \frac{\hat{I}_f}{I_{dc}} \qquad \text{for} \quad 0 < M < 1 \tag{3.11}$$

where $\hat{I}_f$ is the peak value of the fundamental frequency component in $I_{a,b,c}$.

Thus, for a given absolute value and angle, $\vec{\imath}_{ref}$ can be synthesized by two nearby active vectors ($\vec{I}_i$ and $\vec{I}_{i+1}$) and one zero vector ($\vec{I}_z$) [3]–[5]. Based on ampere-second balance principle, the application time for each space vector should hold:

$$\begin{gathered} \vec{\imath}_{ref}\, T_s = \vec{I}_i\, T_i + \vec{I}_{i+1}\, T_{i+1} + \vec{I}_z\, T_z \\ T_s = T_i + T_{i+1} + T_z \end{gathered} \tag{3.12}$$

where T_s, T_i, T_{i+1} and T_z are, respectively, the PWM sampling period and the application time for the vectors $\vec{I}_i$, $\vec{I}_{i+1}$ and $\vec{I}_z$.

For a given Sector $i \,\epsilon\, [I, \dots, VI]$, Eq. 3.10 can be applied to Eq. 3.12. Then, solving it to the application times, the following is obtained:

$$\begin{aligned} T_i &= M\,.\,sin(\pi/3 - \theta) \\ T_{i+1} &= M\,.\,sin(\theta) \qquad \text{for} \quad 0 < \theta < \pi/3 \\ T_z &= T_s - T_i - T_{i+1} \end{aligned} \tag{3.13}$$

Although the space vector transformation determines the active vectors to be applied and their application times, no criteria is defined for the zero vector selection as well as for the sequence in which each vector is used [4]. The influence of these parameters on the AC line current spectrum will be investigated in § 3.5.

3.2.2 CSI Operation in Combination with a PV String – Steady-state Analysis

Assuming an ideal inverter input-output power equilibrium, the DC input voltage is related to the AC grid voltage as follows:

$$V_{dc} = \frac{\sqrt{3}}{2} \cdot \hat{V}_{f,l-l} \cdot M \cdot cos\varphi \qquad \text{for} \quad 0 < M < 1 \tag{3.14}$$

where $\hat{V}_{f,l-l}$ is the peak value of the fundamental line-to-line grid voltage. From this equation, the CSI voltage step-up characteristic becomes clear.

When operating with a PV string, the CSI must be capable of dynamically tracking the Maximum Power Point (MPP) in the entire inverter power range. This requirement is possible through appropriate control of AC voltages and currents in the dq frame [7], as long as the relationship between DC and AC quantities of Eq. 3.14 is guaranteed. Consequently, the PV string sizing becomes crucial in order to properly operate the CSI. Figure 3.5 depicts a typical PV generator characteristic with the CSI operating range and the iso-power curves.

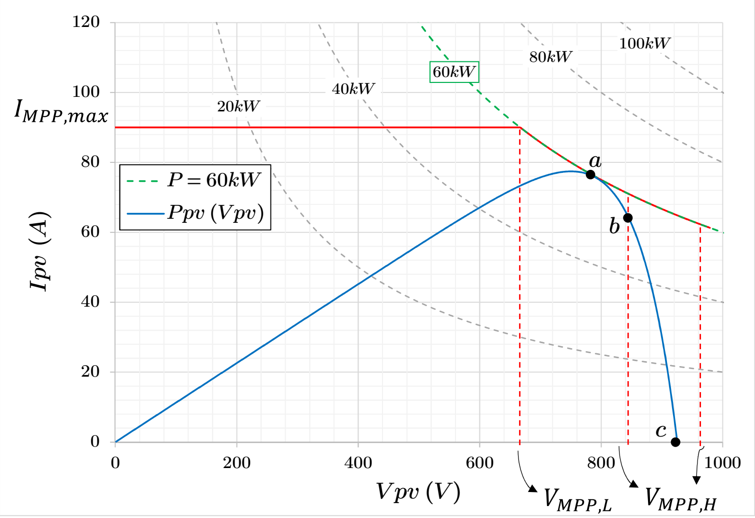


Figure 3. 5 – Typical PV generator $i - v$ characteristic for $P_{PV} = 60kW$ (blue), inverter operating range (solid red line) and the iso-power curves (dashed grey lines).

Due to its current-based source characteristic, the CSI must be capable of extinguishing the DC current (I_{dc}) at any operating point before shutting down and opening all switches. This can be accomplished by imposing a null I_{dc}^{*} reference in the loop control or actively clamping the DC choke by means of an external circuit [8]. A typical shut-down action might be necessary in the case of inverter maintenance during the day, for example.

The maximum current within the MPP range ($I_{MPP,max}$ in Figure 3.5) is defined by the PV string short-circuit current (I_{sc}), which is likely to occur, e.g., in a hot day in combination with a strong solar irradiation. $I_{MPP,max}$ is fixed in order not to exceed the semiconductor thermal limit while ensuring a high enough inverter efficiency. The lower limit of MPP voltage range ($V_{MPP,L}$ in Figure 3.5) is defined by the intersection of $I_{MPP,max}$ with the inverter nominal iso-power curve. The upper limit of MPP voltage range ($V_{MPP,H}$) is directly imposed by the grid voltage level, according to Eq. 3.14. In general, a wide MPP voltage range is preferred, in order to increase the PV system flexibility.

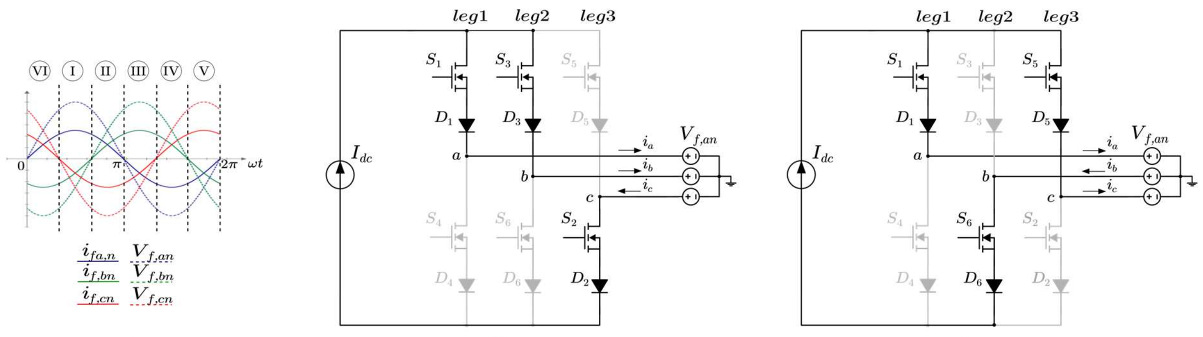
As an example, assuming the case of a three-phase 690V grid voltage, $I_{MPP,max} = 90A$ and a nominal CSI power of 60kW, the MPP voltage range is given by $V_{MPP} = V_{MPP,H} - V_{MPP,L} = 845 - 665 = 180V$. As depicted in Figure 3.5, in the case of a forced shut-down, the control loop is only capable of bringing the operating point from *a* to *b* – in this case, an auxiliary circuit (e.g., an IGBT with a series diode in parallel to L_{dc}) would be necessary to extinguish the I_{dc} current and bring the inverter to point *c*. Increasing the grid voltage level to 800V could enlarge the MPP voltage range ($V_{MPP} = 314V$) while giving more flexibility to the array dimensioning, possibly avoiding an auxiliary shut-down circuit utilization.

3.2.3 Analysis of the Switching Cell Disposition

For the converter switching cell analysis, it is assumed that the CSI generates a balanced system of three-phase sinusoidal currents, defined by

$$\begin{aligned} I_{f,an} &= \hat{I}_{fn} \,.\cos(\omega t) \\ I_{f,bn} &= \hat{I}_{fn} \,.\cos(\omega t - 120°) \\ I_{f,cn} &= \hat{I}_{fn} \,.\cos(\omega t + 120°) \end{aligned} \tag{3.15}$$

where $\hat{I}_{fn} = MI_{dc}/\sqrt{3}$. The grid voltage is the same as in Eq. 3.1. For the sake of simplicity, a unitary DPF is considered, i.e., $\varphi = 0$. Figure 3.6 (a) shows the set of voltage and current waveforms.



a) b) c)

Figure 3. 6 – a) CSI output voltage and current waveforms ($\varphi = 0$); b) CSI equivalent circuit concerning the state transition $\vec{I}_3$ to $\vec{I}_2$, when the reference vector $\vec{\imath}_{ref}$ is located in Sector II and c) CSI equivalent circuit concerning the state transition $\vec{I}_1$ to $\vec{I}_6$, when the reference vector $\vec{\imath}_{ref}$ is in Sector VI. The phase-to-neutral voltages ($V_{f,a,b,c,n}$) are represented as continuous voltage sources, since they are considered to be constant over the entire switching period.

To illustrate the switching process in a CSI, consider, e.g., that the reference vector $\vec{\imath}_{ref}$ is located in Sector II (see Figure 3.4). Thus, the two active nearby vectors $\vec{I}_3$ and $\vec{I}_2$ (corresponding to the active switches $[S_1, S_2]$ and $[S_2, S_3]$, respectively) and a zero vector ($\vec{I}_z$) should be applied. Assuming the angular interval $2\pi/3 < \omega t < 5\pi/6$, where $V_{an} > V_{bn} > V_{cn}$ (see Figure 3.6 (a)), the diode D_3 is conducting (see Figure 3.6 (b)). Then, the transition from the space vector $\vec{I}_3$

to $\vec{I}_2$ will lead to the MOSFET S_3 turn-off and the diode D_1 turn-on. In other words, at this point, the switching process occurs in the high-side group of switches from leg2 to leg1. Now, considering the reference vector $\vec{\imath}_{ref}$ located in Sector VI. Then, the two active nearby vectors $\vec{I}_6$ and $\vec{I}_1$ (corresponding to the active switches $[S_5, S_6]$ and $[S_6, S_1]$, respectively) and a zero vector ($\vec{I}_z$) should be applied. Assuming the angular interval $0 < \omega t < \pi/6$, where $V_{cn} > V_{an} > V_{bn}$, the diode D_1 is conducting (see Figure 3.6 (c)). Then, the transition from the space vector $\vec{I}_1$ to $\vec{I}_6$ will lead to the MOSFET S_1 turn-off and the diode D_5 turn-on. At this point, the switching process occurs in the HS switch group from leg1 to leg3.

If this previous analysis is carried out for the entire fundamental grid period, $0 < \omega t < 2\pi$, the following conclusions can be drawn [9]:

- the switching cells are always horizontally disposed, i.e., the commutation process occurs exclusively between two HS or LS switches;
- for both the HS and LS switch groups, the switching cell moves between legs 1 – 2 – 3 accordingly to the grid sector; and
- due to the symmetry between all sectors, the number of switching transitions will be identical between legs 1 – 2, 1 – 3 and 2 – 3.

3.2.4 Current and Voltage Stresses of Power Semiconductors

Regarding the semiconductors current stress, the average value of the CSI switching current $I_{S'_{1..6}}$ is given by

$$I_{avg,S_{1..6}} = I_{avg,D_{1..6}} = \frac{1}{2\pi}\int_0^{2\pi} I_{S'_{1..6}}\, d\omega t = \frac{I_{dc}}{3} \tag{3.16}$$

The RMS value of $I_{S'_{1..6}}$ is obtained with

$$I_{rms,S_{1..6}} = I_{rms,D_{1..6}} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} {I_{S'_{1..6}}}^2\, d\omega t} = \frac{I_{dc}}{\sqrt{3}} \tag{3.17}$$

It is worth noting that due to the CSI operation constraint, the semiconductor current stress is independent of the employed PWM technique.

Neglecting the voltage drop on the AC line inductors (L_F in Figure 3.1), the maximum switching blocking voltage is defined as follows:

$$V_{max,S_{1..6}} = V_{max,D_{1..6}} = \sqrt{3}\,\hat{V}_{f,l-n} = \hat{V}_{f,l-l} \tag{3.18}$$

For the selection of devices' voltage rating, two other factors should be taken into account: *i)* grid voltage fluctuations. Although the voltage between points *a*, *b* and *c* (cf. Figure 3.1) cannot change instantly – in theory they are connected to an ideal voltage source (C_F) –, the RMS grid voltage value can be increased up to 115% according to some grid codes [10], [11] and *ii)* a reasonable safety margin should be taken into account, due to switching overvoltage transients, Single Event Burnout robustness and other reliability aspects [12], [13]. In doing so, the devices' minimum voltage blocking capability is expressed by

$$V_{rating} \geq \left(1 + \delta v_{grid} + \delta_{SM}\right) \cdot \hat{V}_{f,l-l} \tag{3.19}$$

where δv_{grid} and δ_{SM} represent the allowed grid voltage fluctuations and the adopted voltage safety margin, respectively.

3.2.5 Typical waveforms

The circuit of Figure 3.1 is simulated using PSIM. In this case, the CSI operates injecting power into the three-phase 690V grid, for $\varphi = 0$. All simulation parameters are presented in Table 3.2. The steady-state waveforms are shown in Figure 3.7.

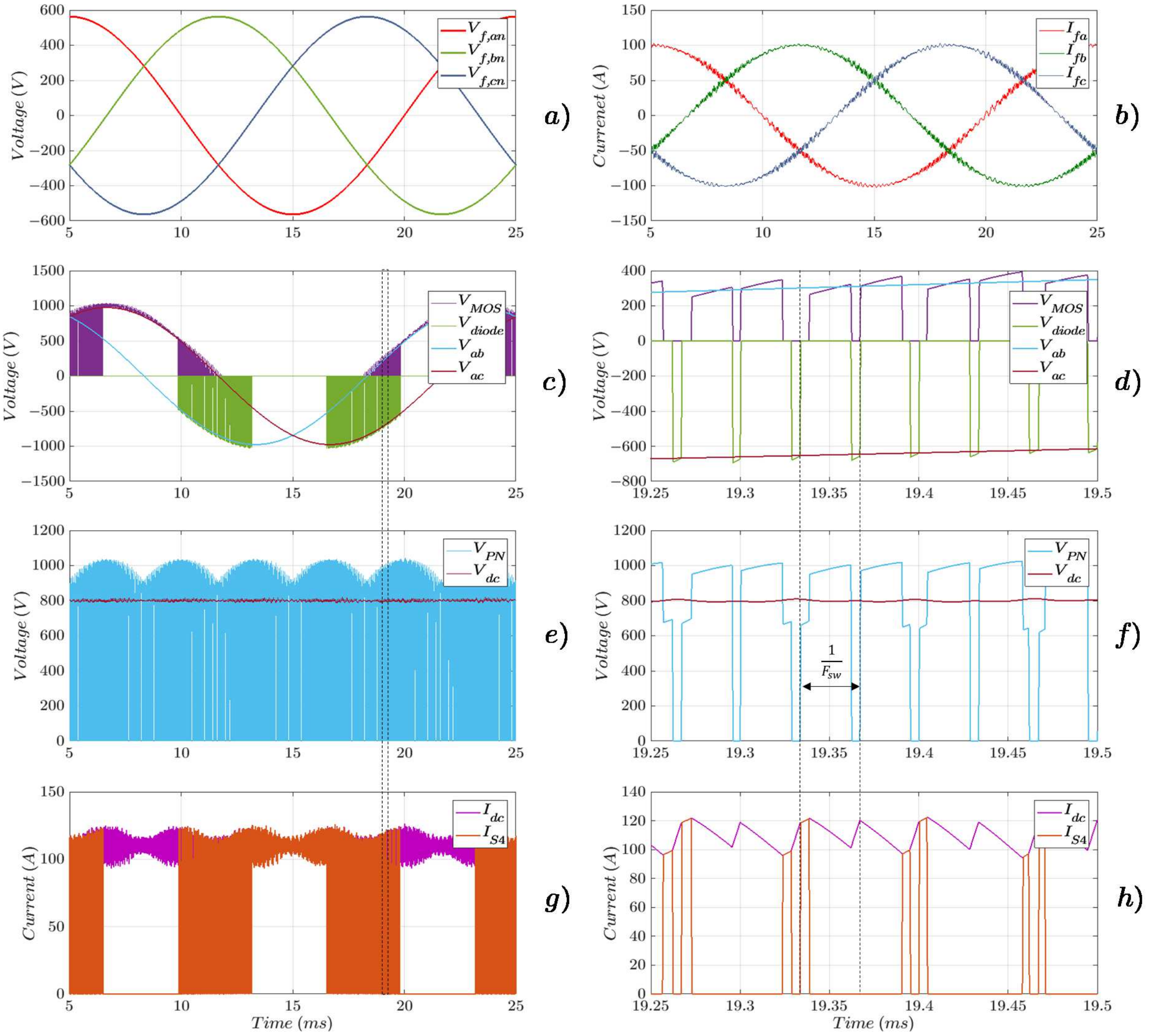


Figure 3. 7 – Simulated waveforms: a) line-to-neutral grid voltages, b) line currents, c) and d) V_{S4} (or $V_{MOS} + V_{diode}$) switching voltage, e) and f) DC link voltages, g) and h) DC link current and I_{S4} switching current.

Table 3. 2 – Simulation parameters for the CSI operation.

Parameter	Symbol	Value
Output active power	P_{out}	85kW
RMS grid voltage	$V_{f,l-l}$	690V
DC voltage	V_{dc}	800V
Switching frequency	F_{sw}	30kHz
DC link choke	L_{dc}	105µH
DC filtering capacitor	C_{dc}	10.8µF
Output AC capacitor	C_F	24µF
Output AC inductor	L_F	75µH

3.3 Semiconductor Conduction Losses

Taking as example the circuit of Figure 3.1 and considering the CSI operation constraint, it is observed that, at any given time, two MOSFETs and two diodes conduct the full DC current. Due to this permanent on-state condition of multiple devices, Current Source-based Converters exhibit relatively high conduction losses, potentially limiting the overall efficiency [14], [15]. Nonetheless, as mentioned in Chapter 2, this issue can be overcome by the implementation of wide-bandgap devices, which intrinsically have a reduced specific on-state resistance ($R_{on,sp}$) [16].

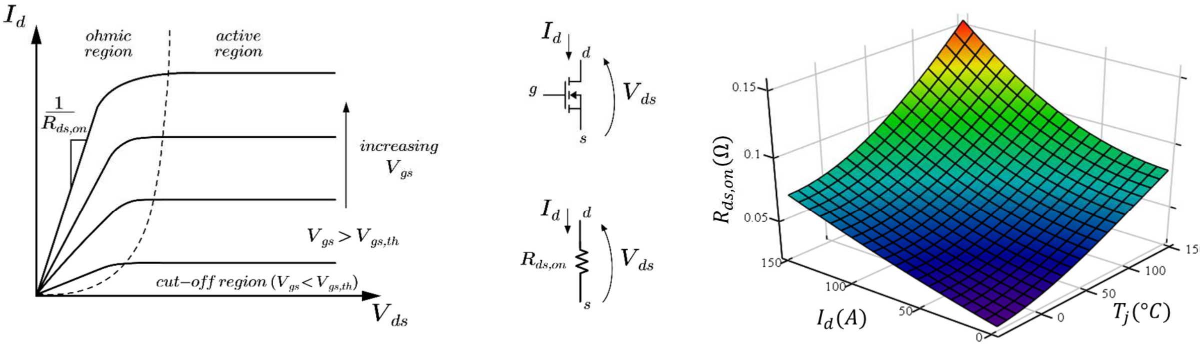
In this section, conduction losses mechanisms of SiC MOSFETs and diodes are described and their impacts on inverter efficiency are investigated for four different CSI switch configurations.

3.3.1 Static modeling of semiconductor devices

a) Power MOSFET

Figure 3.8 (a) shows the static current-voltage characteristic for the MOSFET 1st quadrant operation, where three distinct regions can be described:

- cut-off or blocking region: the applied gate-to-source voltage is smaller than the threshold voltage ($V_{gs} < V_{gs,th}$) - the device is then in the blocking state. At this condition, low-voltage MOSFETs ($V_{rating} \leq 1.7kV$) generate negligible losses, due to low level of leakage current [17];
- active or pinch-off region: the device is in a transition phase between on- and off-state, since the voltage V_{gs} exceeds $V_{gs,th}$. Then, its drain current I_d is related with V_{gs} through the device's transconductance ($g_{fs} = f(I_d, V_{gs})$). At this point, the switching losses mechanism takes place; and
- ohmic region: the MOSFET's current carrying channel being considered to be fully developed, i.e., $V_{gs} - V_{gs,th} > V_{ds} > 0$, the device can be simply modeled as a resistance controlled by the gate-to-source voltage (cf. Figure 3.8 (a) and (b)). The impact of V_{gs} on $R_{ds,on}$ can be explained by the channel resistance modulation, since an increase in V_{gs} leads to a decrease in the channel resistivity, decreasing then the overall specific resistance. Nevertheless, the choice of V_{gs} must be a trade-off between on-state resistance and long-term gate oxide reliability and stability [18].



a) ***b)*** ***c)***

Figure 3. 8 – a) 1st quadrant current-voltage characteristic of an n-channel MOSFET, b) static model for the ohmic region operation and c) $R_{ds,on}$ as a function of drain current and junction temperature (@ $V_{gs} = 20V$) for the SiC bare die CPM2-1700-0045B.

Besides the dependence of $R_{ds,on}$ on V_{gs}, two other factors influence the MOSFET specific resistance: its junction temperature (T_j) and drain current (I_d). First, knowing that the SiC carrier mobility ($\mu_{n,SiC}$) decreases with temperature, an increase in T_j leads to increases in overall on-state resistance [18]. Second, when the device's channel is crossed by a current, the uniformly distributed inversion layer underneath the gate oxide is narrowed, leading to an increase of the channel resistance [19]. Figure 3.8 (c) depicts the characteristic of $R_{ds,on} = f(I_d, T_j)$ for the SiC MOSFET bare die CPM2-1700-0045B at $V_{gs} = 20V$. As shown, the referred SiC device has a positive temperature coefficient (PTC), i.e., $dR_{ds,on}/dT_j > 0$, which makes paralleling easier [20]. Furthermore, to precisely estimate conduction losses, the influence of junction temperature cannot be neglected, since $R_{ds,on@40A}(125°C) = 1.8 \cdot R_{ds,on@40A}(25°C)$. The same is valid for I_d, as $R_{ds,on@25°C}(50A) = 1.23 \cdot R_{ds,on@25°C}(5A)$.

Based on the MOSFET datasheet, its on-state resistance characteristic can be empirically described as follows:

$$R_{ds,on}(T,I) = a_1 + a_2 I + a_3 T + a_4 I^2 + a_5 IT + a_6 T^2 + a_7 I^2 T + a_8 I T^2 + a_9 T^3 \qquad (3.20)$$

where $a_{1,2..9}$ are fitting constants. To simplify the nomenclature, the junction temperature and drain current are denoted by T and I, respectively. In this equation, the 2nd and 3rd order cross terms are employed to improve the model accuracy even though they do not have any physical meaning.

Thus, the MOSFET average power dissipation in on state is given by

$$P_{cond,MOS}(T_j, I_d) = R_{ds,on}(T_j, I_d). I_{rms,d}^2 \qquad (3.21)$$

b) Schottky Barrier Diode (SBD)

The SBD forward current-voltage characteristic and its static model are presented in Figure 3.9.

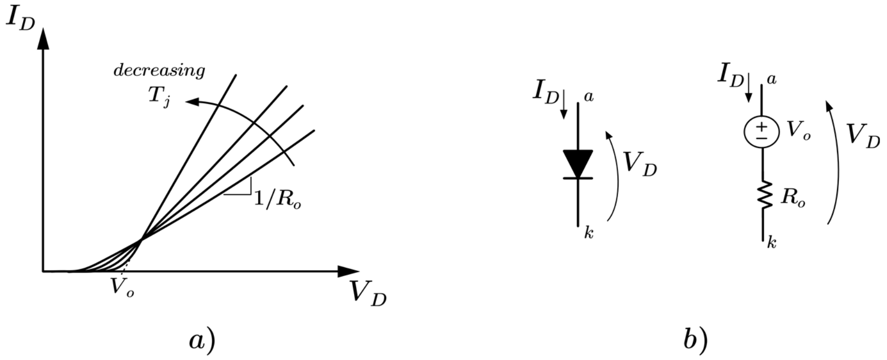


Figure 3. 9 – a) Current-voltage forward behavior of a generic SiC SBD and b) the adopted static model.

When forward biased, two components form the voltage drop across the SBD. First, a threshold voltage (V_o) is developed on the metal-semiconductor interface which decreases somewhat with junction temperature [21]. Second, an ohmic voltage drop ($I_D \cdot R_o$) arises across the drift layer, which increases with temperature due to the decreasing of electron mobility. In order to take into account this temperature dependence of SBD on-state behavior, Eq. 3.22 can be employed, where $b_{1,2..5}$ are fitting constants.

$$\begin{gathered} R_o(T_j) = b_1 + b_2T_j + b_3T_j^2 \\ V_o(T_j) = b_4 + b_5T_j \end{gathered} \tag{3.22}$$

Thus, the SBD average conduction power losses becomes

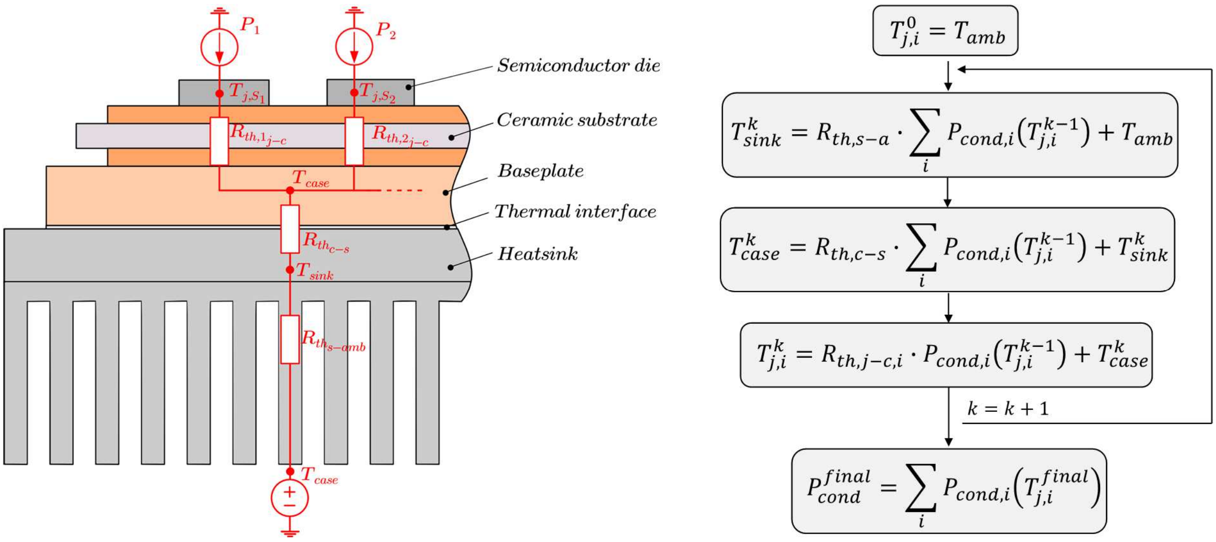
$$P_{cond,D} = V_o(T_j).I_{avg,D} + R_o(T_j).I_{rms,D}^2 \tag{3.23}$$

3.3.2 Conduction losses estimation

As discussed in the previous section, conduction losses are tightly related to semiconductor junction temperature. Thus, in order to precisely estimate losses, a thermal model for the cooling system must be developed [13]. Figure 3.10 (a) shows the basic structure of a power semiconductor module together with its steady-state unidirectional thermal model. Here, the heat spread is considered to be ideal (i.e., isothermal elements) and only stationary operation condition is taken into account (i.e., thermal capacitances are neglected). Then, for a given semiconductor S_1, its conduction losses can be written as

$$P_{cond,S1}(I_{S1}, T_{j,S1}) = \frac{T_{j,S1}(P_{cond,S1}) - T_{amb}}{R_{th-eq,S1}} \tag{3.24}$$

where $R_{th-eq,S1}$ indicates the equivalent thermal resistance between junction to ambient for S_1. Thus, the electro-thermal coupling of conduction losses becomes evident and an iterative process can be applied to find the solution of Eq. 3.24. Figure 3.10 (b) shows the flowchart for the estimation of temperature-dependent conduction losses.



a) *b)*

Figure 3. 10 – a) Basic structure of a power module with the considered thermal model and b) flowchart for temperature-dependent conduction losses estimation.

3.3.3 Comparison of different CSI switch configurations in terms of conduction losses

In order to identify the most adapted CSI switch configuration for PV applications, three CSI variations found in the literature that claim to reduce conduction losses are studied, namely, a) CSI with seven switches (CSI7) [22], b) CSI with four-quadrant switches (4qCSI) [23] and c) Delta-type CSI [24]. In the comparison, a quantitative analysis is carried out having the standard six-switch Current Source Inverter (CSI) as the reference. For the conduction losses model, the DC-link current (I_{dc}) is considered to be constant and it is equally shared between identical devices (i.e., no mismatch between semiconductors). Figure 3.11 presents all four considered CSI variations and their respective thermal models.

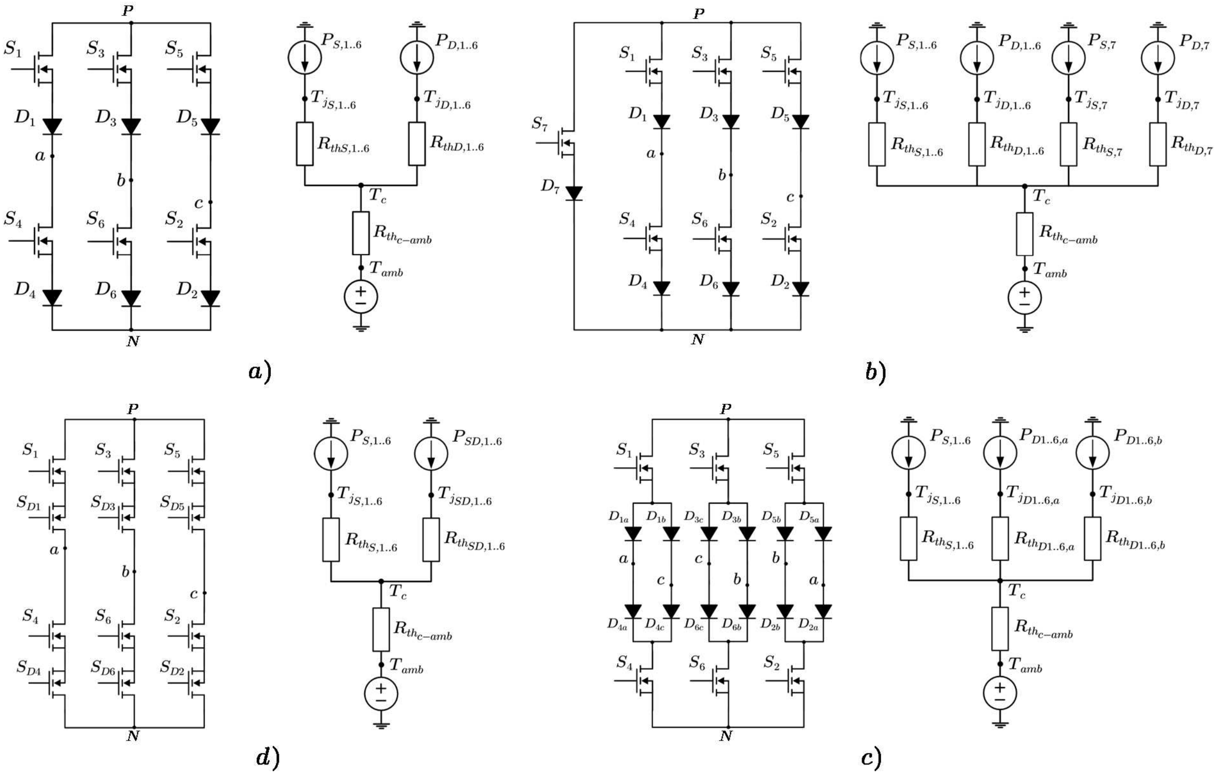


Figure 3. 11 – Four possible CSI switch configurations and their respective thermal models: a) standard six-switch Current Source Inverter (CSI), b) CSI with seven switches (CSI7), c) Delta-type CSI and d) CSI with four-quadrant switches (4qCSI).

In all cases, the DC and AC voltage levels are, respectively, $V_{MPP} = 745V$ and $V_{f,l-l} = 690V$, unless otherwise specified. The employed reference semiconductors are 1.7kV SiC MOSFET CPM2-1700-0045B (dimensions 4.08x7.35mm^2) and diode CPW5-1700-Z050B (dimensions 6x6mm^2), from Wolfspeed, and the number of dies in parallel per device is denoted n. In Appendix I, the on-state characteristic of the mentioned devices are presented together with their fitting constants, as introduced in § 3.3.1.

To help quantitatively compare the CSI solutions, the inverter efficiency and European Efficiency are defined as follows:

$$\eta^* = \frac{P_{in} - P_{cond}(T_j, I_{dc})}{P_{in}} = \frac{I_{dc} \cdot V_{MPP} - P_{cond}(T_j, I_{dc})}{I_{dc} \cdot V_{MPP}} \tag{3.25}$$

$$\begin{aligned} \eta^*_{euro} = 0.03 \cdot \eta^*_{5\%} + 0.06 \cdot \eta^*_{10\%} + 0.13 \cdot \eta^*_{20\%} + 0.1 \cdot \eta^*_{30\%} + \cdots \\ + 0.48 \cdot \eta^*_{50\%} + 0.2 \cdot \eta^*_{100\%} \end{aligned} \tag{3.26}$$

Thus, two figures of merit (FOM) relating the used chip area with the maximum allowed input power and the European Efficiency can be defined, respectively:

$$C_{DU} = \frac{P_{in,max}}{\sum_i A_{chip,i}} = \frac{I_{dc,max} \cdot V_{MPP}}{A_{T,chip}} \tag{3.27}$$

$$FOM = \frac{1}{A_{T,chip} \cdot (1 - \eta^*_{euro})} \tag{3.28}$$

where $I_{dc,max}$ is the current for which $T_{j,max} = 125°C$ is reached and $A_{T,chip}$ is the total used semiconductor area. As they are presented, C_{DU} and FOM are related to the converter's cost-effectiveness and are then quantities to be maximized.

The adopted parameters in the thermal models are shown in Table 3.3 and the devices' current stress for all CSI variations are summarized in Table 3.4.

Table 3. 3 – Adopted thermal parameters.

$R_{th,j-c,S} = 0.4K/W$	$R_{th,c-amb} = 0.1K/W$
$R_{th,j-c,D} = 0.33K/W$	$T_{amb} = 40°C$
$R^*_{th,j-c,D} = 0.66K/W$ [1]	$T_{j,max} = 125°C$

1) diode thermal resistance in the case of Delta-type CSI.

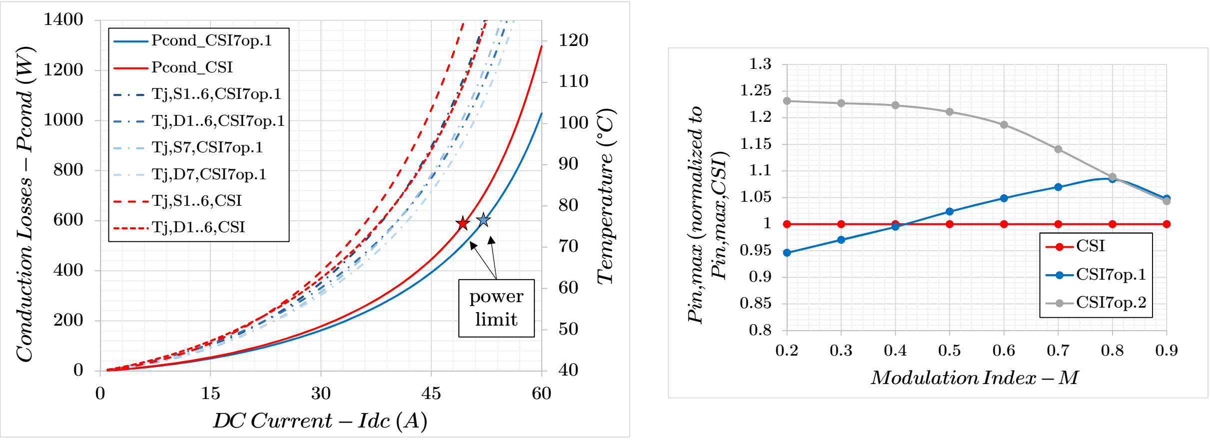
Table 3. 4 – Device's current stress for the studied CSI switch configurations.

CSI	$I_{avg,S,D_{1..6}} = \frac{I_{dc}}{3}$	$I_{rms,S,D_{1..6}} = \frac{I_{dc}}{\sqrt{3}}$
CSI7$_{op.1}$	$I_{avg,S,D_{1..6}} = \frac{M}{\pi} I_{dc}$ $I_{avg,S,D_7} = \left(1 - 3\frac{M}{\pi}\right) I_{dc}$	$I_{rms,S,D_{1..6}} = I_{dc}\sqrt{\frac{M}{\pi}}$ $I_{rms,S,D_7} = I_{dc}\sqrt{1 - 3\frac{M}{\pi}}$
CSI7$_{op.2}$ [1]	$I_{avg,S,D_{1..6}} = \left(\frac{1}{3} \cdot \frac{R_7}{r} + \frac{M}{\pi} \cdot \frac{R_1}{r}\right) I_{dc}$ $I_{avg,S,D_7} = \left(\frac{R_1}{r}\right)\left(1 - 3\frac{M}{\pi}\right) I_{dc}$	$I_{rms,S,D_{1..6}} = \frac{I_{dc}}{r}\sqrt{{R_7}^2 \frac{1}{3} + {R_1}^2 \frac{2M}{\pi}}$ $I_{rms,S,D_{1..6}} = I_{dc}\left(\frac{R_1}{r}\right)\sqrt{1 - 3\frac{M}{\pi}}$
Delta-type CSI	$I_{avg,S_{1..6}} = \frac{I_{dc}}{3}$ $I_{avg,D_{1..6}a} = \left(\frac{1}{6} - \frac{M sin(\varphi)}{4\pi}\right) I_{dc}$ $I_{avg,D_{1..6}b} = \left(\frac{1}{6} + \frac{M sin(\varphi)}{4\pi}\right) I_{dc}$	$I_{rms,S_{1..6}} = I_{dc}\sqrt{\frac{1}{3} - \frac{\sqrt{3} M cos(\varphi)}{4\pi}}$ $I_{rms,D_{1..6}a} = I_{dc}\sqrt{\frac{4\pi - 6M sin(\varphi) - 3\sqrt{3} M cos(\varphi)}{24\pi}}$ $I_{rms,D_{1..6}b} = I_{dc}\sqrt{\frac{4\pi + 6M sin(\varphi) - 3\sqrt{3} M cos(\varphi)}{24\pi}}$
4qCSI	Idem CSI	

1) $r = R_1 + R_7$, where R_7 is the resistance of $(S_7 + D_7)$ and R_1 the resistance of $2 \cdot (S_{1..6} + D_{1..6})$.

a) CSI with 7 switches (CSI7)

In [22], the possibility of adding a 7th switch in the classic CSI is discussed. The idea here is to minimize conduction losses by applying the freewheeling/zero states ($\vec{I}_z$) through S_7 (see Figure 3.11 (b)), which has a reduced on-state resistance. To be able to operate in a wide range of $\cos(\varphi)$, a series diode (D_7) is required. The ratio between different branch resistances is assumed to be $R_1 = 2 \cdot R_7$ (cf. Table 3.4). With the added 7th switch, the inverter may now operate with two distinct modulation strategies, namely, op.1 and op.2. While operating in op.1 mode, the zero states are exclusively applied with S_7 (as in [22]). On the other hand, in op.2 mode, the zero states are applied with (S_1, S_4, S_7), (S_3, S_6, S_7) and (S_5, S_2, S_7), which allows a decrease of the RMS current per device, helping to further reduce conduction losses. Figure 3.12 presents the CSI and $\text{CSI7}_{\text{op.1}}$ conduction losses and the maximum allowed input power as a function of the modulation index, for $n = 1$. Table 3.5 summarizes all obtained results for $n = 1$.



a) *b)*

Figure 3. 12 – a) Conduction losses for the CSI and $\text{CSI7}_{\text{op.1}}$ and their respective devices' junction temperatures for $M = 0.88$; $n = 1$ and b) maximum allowed input power as a function of the modulation index.

From Figure 3.12 (b), one concludes that the modulation strategy op.2 brings the most benefit for the CSI7 in terms of $P_{in,max}$, especially for $M \leq 0.6$. This is due to the fact that thermal stress is more equally shared between the devices. When employing the modulation strategy op.1, $P_{in,max}$ decreases with M, for $M < 0.8$. At this point, the most thermally constrained device becomes S_7. Concerning the FOMs in Table 3.5, it is possible to conclude that the 17% of chip area increase for the CSI7 is more cost-effective for lower modulation indexes. Nevertheless, when considering 1kV PV strings and 690V or 800V grid, the CSI operation within $M < 0.7$ is very unlikely to happen, making the CSI7 a less compelling solution for these applications. However, in the case of residential PV systems – where lower

DC voltages are available – the CSI7 could be an interesting solution, especially if considered with a hybrid switch configuration, e.g., making $S_{1..6}$ Si-based and S_7 SiC-based devices.

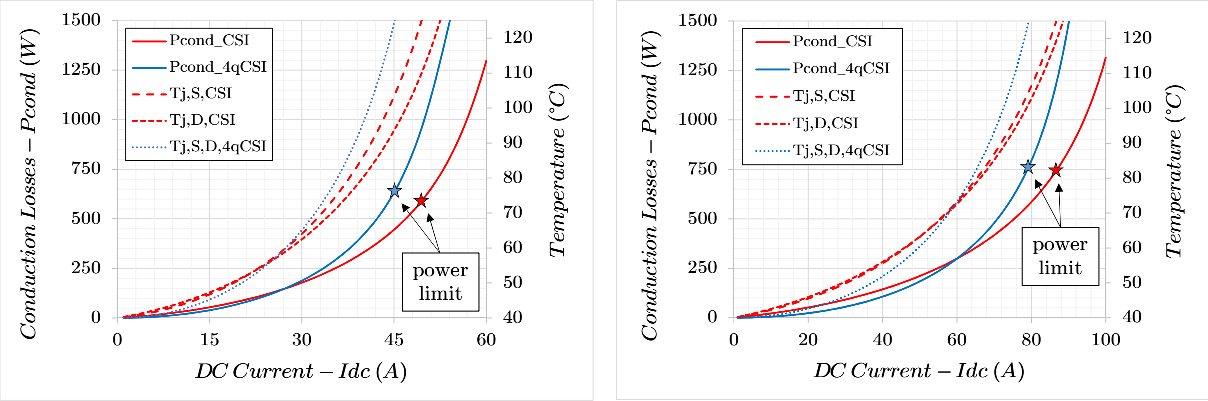
Table 3. 5 – Results for CSI7 when $n = 1$.

Switch config.	V_{MPP} (V)	M	$\frac{A_{T,chip}}{A_{T,chip,CSI}}$	$\Delta P_{in,max}(\%)$ (compared with CSI)	$\frac{C_{DU}}{C_{DU,CSI}}$	$\eta(\%)$ @ $P_{in,max,CSI}$	$\frac{FOM}{FOM_{CSI}}$
CSI	745	0.88	1	0	1	98.41	1
CSI7$_{\text{op.1}}$			1.17	5.71	0.91	98.62	0.95
CSI	686	0.7 [1]	1	0	1	98.27	1
CSI7$_{\text{op.1}}$			1.17	7.03	0.92	98.7	1.08
CSI7$_{\text{op.2}}$			1.17	13.76	0.97	98.78	1.11

1) considering $V_{f,l-l} = 800V$.

b) CSI with four-quadrant switches (4qCSI)

In several CSI applications, the major part of conduction losses arises from the series diodes ($D_{1..6}$) [23]. This is especially true for light-load conditions, where efficiency is usually limited by the diode's junction voltage drop (V_o). To overcome this drawback, the diodes can be replaced by MOSFETs (with low specific resistance) operating in the 3rd quadrant, i.e., in synchronous rectification mode (cf. Figure 3.11 (b)) [25]. Thereby, one can take full advantage of MOSFET's paralleling, since its equivalent on-state resistance is inversely proportional to the number of dies in parallel, which is typically not the case when using diodes (because of V_o). Figure 3.13 depicts the 4qCSI conduction losses for two different die configurations and Table 3.6 summarizes the results.



a) b)

Figure 3. 13 – Conduction losses and junction temperatures for the CSI and 4qCSI considering a) one single chip per device ($n = 1$) and b) three chips per device ($n = 3$).

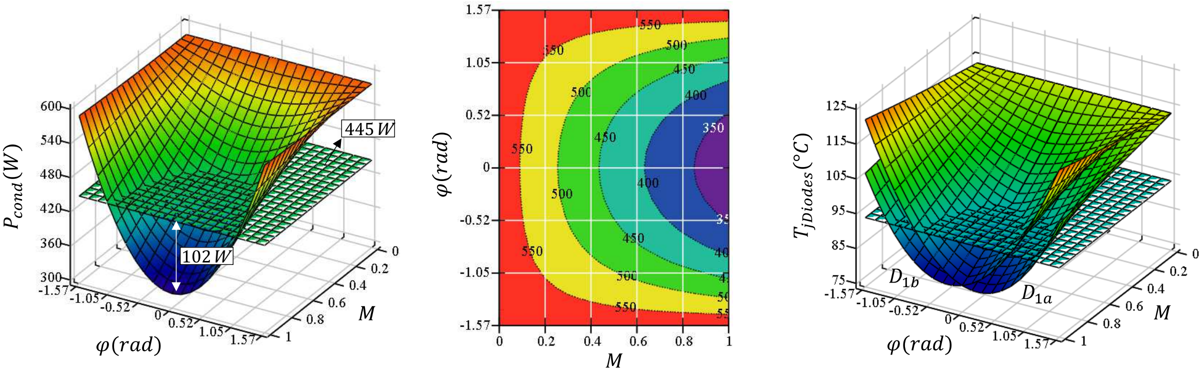
From this graph, it can be seen that while increasing the number of paralleled dies, the difference in terms of conduction losses between the CSI and 4qCSI also increases, as expected. This leads to a considerably higher FOM_{4qCSI} when $n = 3$, thanks to its improved European Efficiency. Additionally, it is worth noting that in both cases, the 4qCSI maximum allowed input power is derated in comparison with the CSI. Since only MOSFETs compose the 4qCSI, the electro-thermal coupling accelerates the increase of losses with I_{dc}. Despite that fact, $C_{DU,4qCSI} \cong C_{DU,CSI}$, resulting from the smaller footprint of MOSFET chips when compared to that of diodes. Concerning the 4qCSI drawbacks, they are mainly related to the number of MOSFETs in the topology. When doubling the number of controllable switches, the driver units might be doubled as well, increasing costs and complexity. Besides that, the four-quadrant switch timing controls must be adjusted to minimize the conduction time through the MOSFET's body diode [25]. From the presented results, the 4qCSI equipped with the considered 1.7kV SiC devices seems to be an interesting solution for medium- or high-power PV applications.

Table 3. 6 – Results for the 4qCSI.

Switch config.	n	V_{MPP} (V)	$\frac{A_{T,chip}}{A_{T,chip,CSI}}$	$\Delta P_{in,max}(\%)$ (compared with CSI)	$\frac{C_{DU}}{C_{DU,CSI}}$	$\eta(\%)$ @ $P_{in,max,4qCSI}$	$\frac{FOM}{FOM_{CSI}}$
CSI	1	745	1	0	1	98.67	1
4qCSI			0.91	-9.17	0.99	98.13	1.07
CSI	3	745	1	0	1	99.03	1
4qCSI			0.91	-8.16	1.01	98.7	1.24

c) Delta-type CSI

As discussed for the CSI7, a possible solution to cap conduction losses is to simultaneously share the DC current between multiple CSI legs. With this in mind, the authors in [24] have proposed the Delta-type CSI (see Figure 3.11 (d)). The idea here consists in splitting each series diode (e.g., D_1 rated for x amps) into two smaller ones ($D_{1,a,b}$ rated for $x/2$ amps) and connecting them to the grid in a delta-configuration. Thus, with an appropriate modulation strategy, the I_{dc} current can be shared between legs, allowing to alleviate conduction losses in the MOSFETs. It should be noted that this is achieved without adding any supplementary chip area. Also, another advantage of the Delta-type CSI concerns the series diode's blocking voltage rating, which is 15% less than in the traditional CSI configuration [24]. Figure 3.14 shows the Delta-type conduction losses for $n = 1$ and $I_{dc} = 45A$. All the results are summarized in Table 3.7.



a) b) c)

Figure 3. 14 – a) 3D plot and b) contour plot with the iso-power curves of conduction losses in the Delta-type CSI for $n = 1$; $I_{dc} = 45A$ and c) the respective diode junction temperatures. The planes in a) and c) represent $P_{cond,CSI}$ and $T_{jD1..6,CSI}$.

From Figure 3.14 (a), it is remarkable the reduction of conduction losses in the Delta-type CSI. When operating with $M = 0.88$ and $\varphi = 0$, this switch configuration allows a reduction of 23% in conduction losses, if compared with the CSI. This leads to an increase of more than 13% in the maximum input power. At the same time, the improved sharing of I_{dc} between MOSFETs helps to increase η_{euro}, as shown by the superior FOMs. On the other hand, for lower values of $cos(\varphi)$, a thermal stress imbalance arises between the series diodes, as depicted in Figure 3.14 (c). In this study, it was seen that for $\cos(\varphi) < 0.5$, the Delta-type CSI becomes a less compelling solution than the CSI. Hence, when considering a Delta-type inverter capable of operating within $0 < \cos(\varphi) < 1$, which is often the case in PV, the worst case scenario should be taken into account (i.e., $cos(\varphi) = 0$), penalizing the cost-effectiveness of such a solution.

Table 3. 7 – Results for the Delta-type CSI when $n = 1, M = 0.88$ and $V_{MPP} = 745V$.

Switch config.	$\cos(\varphi)$	$\frac{A_{T,chip}}{A_{T,chip,CSI}}$	$\Delta P_{in,max}(\%)$ (compared with CSI)	$\frac{C_{DU}}{C_{DU,CSI}}$	$\eta(\%)$ @ $P_{in,max,CSI}$	$\frac{FOM}{FOM_{CSI}}$
CSI	-	1	0	1	98.41	1
Delta-type	1	1	13.59	1.14	98.82	1.21
Delta-type	0.5	1	0.9	1.01	98.37	0.97

With all the results presented in this section, the classic six-switch CSI seems to better fulfill the specifications for the target PV application. Thanks to its cost-effectiveness regarding the PV voltage levels, capability of operating within a wide range of $cos(\varphi)$, reduced number of gate driver units and simplicity, the CSI has been selected to be the focus of the present work.

3.4 Switching Event in the CSI Topology

In a CSI, the switching event always takes place under constant current and depends on the grid voltage to occur. After an entire switching cycle, four commutations are perceived within the switching cell: two of these under hard-switching condition and two under soft-switching condition [26], [27]. In this section, the CSI switching mechanisms are described together with switching losses and their differences from Voltage Source Inverter's are highlighted.

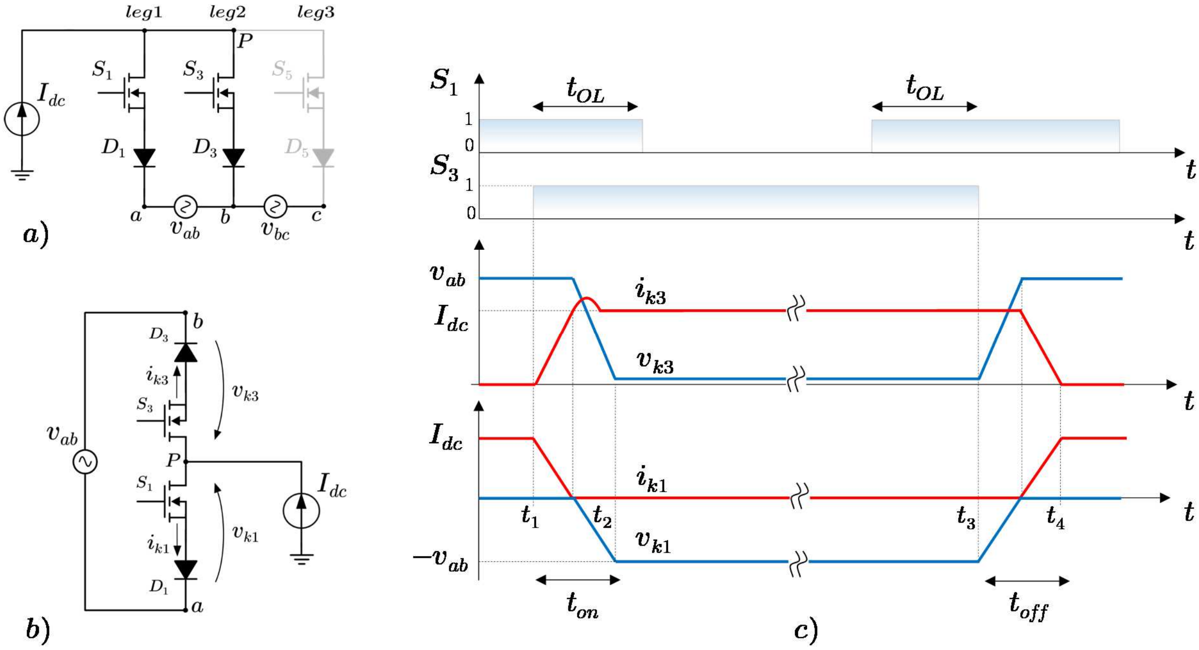


Figure 3. 15 – a) CSI high-side switches when switching between legs 1 and 2, b) its reorganized switching cell and c) simplified switching waveforms.

To exemplify the switching event in the CSI, let's consider the circuit of Figure 3.15 (a). Here, only the high-side switches are depicted, since they are independent of the low-side devices. The commutation is assumed to take place between leg 1 and 2. For that reason, SW_5 is considered to be in the off-state and is not, a priori, involved in the commutation. In this analysis, SW_x refers to the macro-switch x, i.e., the serial connection of the SiC MOSFET S_x and the SBD D_x. Excluding leg3, the aforementioned circuit can be redrawn for clarity, as presented in Figure 3.15 (b).

Initially, it is considered that $v_{ab} > 0$ and SW_1 is conducting (see Figure 3.15 (c)). At this point, D_3 is forward biased and it does not conduct any current, since S_3 is off. When the overlapping time (t_{OL}) begins (@t_1, S_3 is turned-on), current starts to flow through SW_3, since $v_b < v_a$. Knowing that $I_{dc} = cte$, the growing i_{k3} forces i_{k1} to decay to zero, blocking D_1. At this point, SW_1 experiences soft turn-off at zero current and D_1 starts to block a negative voltage reaching $v_{k1} = -v_{ab}$. On the other hand, at $t = t_2$, S_3 has finished turning-on under hard-switching condition and the overlapping time can finally be ended. After some lapse of time, SW_1 must be turned-on again. Thus, S_1 is gated on, starting the t_{OL}. Since D_1 is now reverse biased, nothing happens until $t = t_3$, where S_3 is switched off. Again, S_3 encounters a hard turn-off, since its voltage rises while $i_{k3} = I_{dc}$. As soon as $v_{k3} = v_{ab}$, diode D_1 becomes forward biased and current starts flowing under zero-voltage switching condition. If the same analysis is carried out considering $v_{ab} < 0$, it can be seen that hard-switching arises from SW_1 whilst soft-switching is observed for SW_3. In order to insure proper operation, it is noticeable from Figure 3.15 (c) that the SW_3 hard turn-on transition (t_{on}) must be ended before the overlapping time extinguishes, i.e., $t_{OL} > t_{on}$. This same observation could be directly obtained if duality principle between CSI and VSI is applied, since the latter requires a minimum dead-time dictated by hard turn-off commutation [28].

From the previous analysis, it can be stated that, within a CSI switching cell, the MOSFET in the forward biased macro-switch will encounter hard-switching losses for both turn-on and turn-off transitions, whereas the remaining switches do not generate any additional switching losses - as far as SBD are employed (cf. § 4.5.4, where experimental validation is presented). In summary, even though being composed of four devices, the CSI switching cell always involves two of them in the commutation, one diode and one transistor. For that reason, the switching losses mechanism in the CSI can be compared to any other MOSFET/diode switching cell. In the following sections, a brief description of switching losses mechanisms for a SiC MOSFET/SBD switching cell is presented.

a) Turn-on transition

Figure 3.16 shows the detailed time intervals for the turn-on switching transient together with their equivalent circuits. Initially, it is considered that SW_3 is conducting I_{dc}, i.e., S_3 is gated on and the diode D_3 is forward biased.

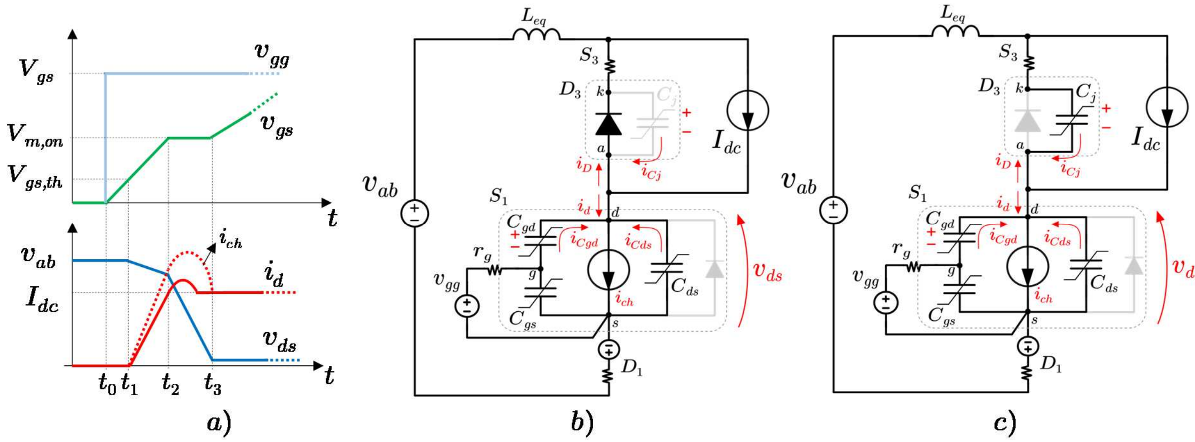


Figure 3. 16 – a) Switching waveforms at turn-on transition and switching cell equivalent circuits for b) $t_1 \leq t < t_2$ and c) $t_2 \leq t < t_3$. Here, only the equivalent circuits related to intervals that generate switching losses are shown.

Then, the switching transient can be divided into four intervals, as follows:

- **Interval I ($t_0 \leq t < t_1$)**: at $t = t_0$, the driving circuit applies a high enough positive voltage V_{gs} in order to turn-on the MOSFET. The input capacitance $C_{iss} = C_{gs} + C_{gd}$ starts to be charged, but since $v_{gs} < v_{gs,th}$ the device is still in the off-state and no switching losses are perceived, since $P_{sw} = \int_{tsw} i_{ch} \cdot v_{ds}\, dt$;
- **Interval II ($t_1 \leq t < t_2$)**: At instant t_1, the voltage $v_{gs} = v_{gs,th}$ and the MOSFET channel is formed. At this point, the device behaves as a current source controlled by V_{gs} through its transconductance g_{fs}. Then, the drain current i_d rises (also i_{ch}), while the diode forward current i_D decreases. This imposes a *di/dt* in the power loop which in turn induces a voltage drop (due to parasitic inductance L_{eq}) on the MOSFET drain-to-source terminal. The v_{ds} variation leads the output capacitance $C_{oss} = C_{gd} + C_{ds}$ to start discharging itself through the channel. During this stage, switching losses are generated and its main contributor is the crossover between the rising i_{ch} and v_{ds};
- **Interval III ($t_2 \leq t < t_3$)**: At $t = t_2$, i_d reaches I_{dc} and leads D_3 to block, since $i_D = 0$. At this point, the diode's junction capacitance C_j is no longer short-circuited and starts to charge with i_{Cj} due to the positive *dv/dt* at its terminals. It is worth noting that i_{Cj} has no other way to charge but through the MOSFET channel. Simultaneously, the voltage v_{ds} falls at a high *dv/dt*, leading C_{oss} to completely discharge via the channel. During this stage, switching losses are generated and its main portion comes from the devices' parasitic capacitances, since $i_{ch} = i_{Coss} + i_{Cj} + I_{dc}$;

- **Interval IV ($t \geq t_3$)**: once v_{ds} reaches $i_d \cdot R_{ds,on}$, v_{gs} continues to increase. Interval IV is a lossless period, since the commutation in the power loop has been finished.

b) Turn-off transition

Figure 3.17 shows the time intervals for the turn-off switching transient and their equivalent circuits.

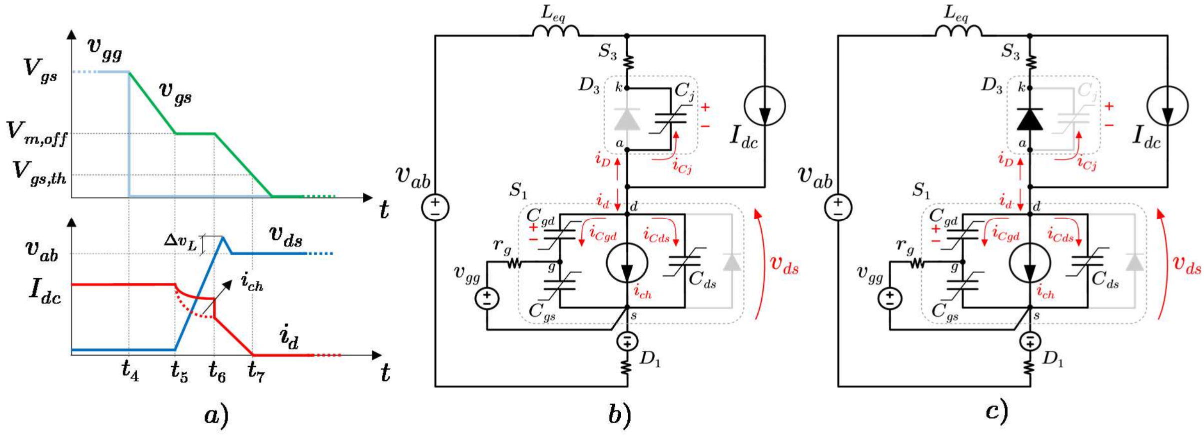


Figure 3. 17 – a) Switching waveforms at turn-off transition and switching cell equivalent circuits for b) $t_5 \leq t < t_6$ and c) $t_6 \leq t < t_7$.

Again, the switching transient can be divided into four intervals, as follows:

- **Interval V ($t_4 \leq t < t_5$)**: at $t = t_4$, the gate driver applies a negative voltage to turn-off the MOSFET and the discharge process of C_{iss} starts. In this phase, there is no turn-off losses, since the voltage and current in the power loop are unchanged;
- **Interval VI ($t_5 \leq t < t_6$)**: At instant t_5, v_{gs} reaches the Miller voltage $V_{m,off}$ and the MOSFET starts turning off provoking an increase in v_{ds}. The positive dv_{ds}/dt leads to the charge of C_{oss} as well as the discharge of C_j. Knowing that $i_d = I_{dc} - i_{Cj}$, the channel current decreases, becoming $i_{ch} = I_{dc} - i_{Cj} - i_{Coss}$. From this, it is clear that if $i_{Cj} + i_{Coss}$ is sufficiently large and the circuit driver is fast enough to cut off the channel, i_{ch} can be extinguished before t_6, producing a nearly lossless turn-off transition (i.e., quasi-ZVS condition [23], [29]). This phase ends when D_3 is forward biased, i.e., $v_{ds} = v_{ab}$;
- **Interval VII ($t_6 \leq t < t_7$)**: at $t = t_6$, C_{gd} is completely discharged and the Miller plateau is ended. Then, i_d starts decreasing towards zero. An overvoltage is then created over the MOSFET due to L_{eq} together with L_{eq}–C_{oss} resonance. If the quasi-ZVS condition is not fulfilled, there is an

additional portion of turn-off losses due to the crossover of v_{ds} and $i_{ch} = i_d$ [30];

- **Interval VIII** $(\boldsymbol{t \geq t_7})$: at this point, the switching event in the power loop is ended and there is no turn-off losses.

Based on the previous analysis, the countermeasures to reduce switching losses are summarized in Table 3.8.

Table 3. 8 – Countermeasures to reduce switching losses.

	Turn-on	Turn-off
Capacitive Losses	Decreasing C_j, C_{oss}, ${v_{sw}}^1$	Decreasing R_g, C_{oss}, i_{sw}, ${v_{sw}}^1$
i_{sw} x v_{sw} crossover	Decreasing R_g, L_{eq}, C_{oss}, i_{sw}, v_{sw} Increasing $V_{gs,on}$	Does not exist, if quasi-ZVS conditions are fulfilled

1) considering $C_{oss} = cte$, which is reasonable at higher voltages.

3.4.1 Simulation-based comparison of switching event in the CSI and VSI topologies

To investigate the differences in terms of switching losses between the CSI and VSI switching cells, the circuits of Figure 3.18 (a) and (b) are implemented in LTspice. The Spice die models C2M0040170D and CPW51700Z050B, from Wolfspeed, are used for the SiC MOSFETs and diodes, respectively. Then, two cases are analyzed: switching under high (50A) and low (10A) current condition. The results are depicted in Figure 3.18 (c) and (d).

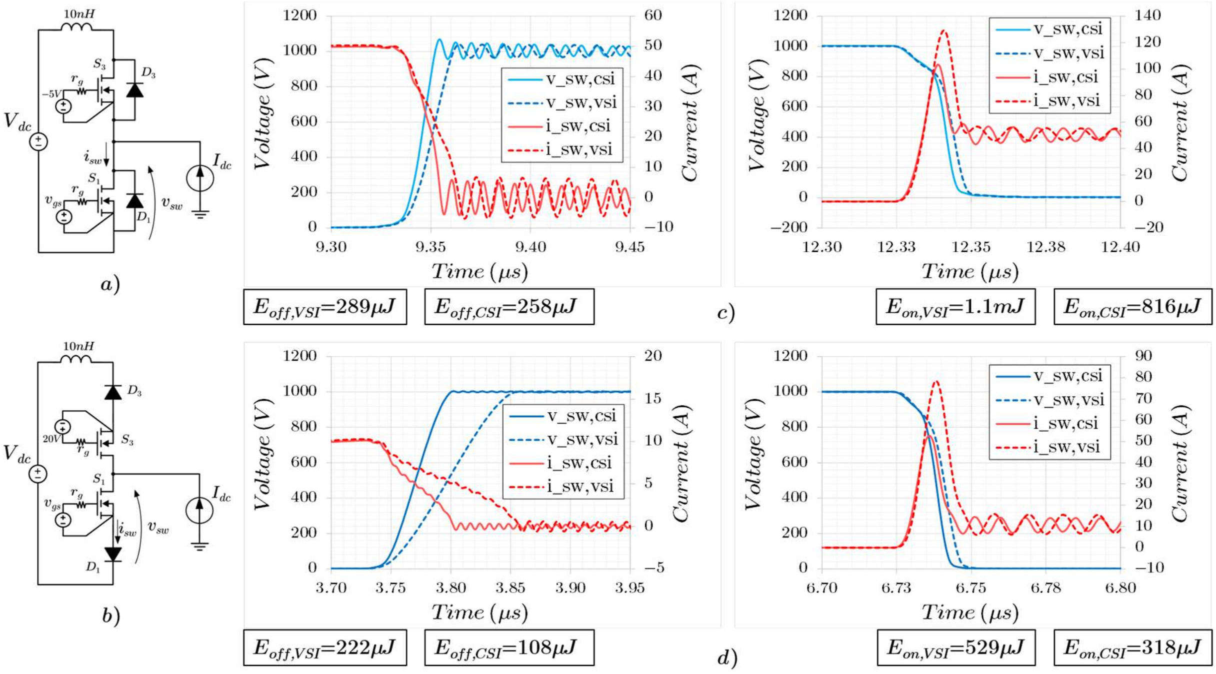


Figure 3. 18 – Implemented circuits for a) VSI topology and b) CSI topology. The switching waveforms are presented in c) for $I_{dc} = 50A$ and d) for $I_{dc} = 10A$. In the simulations $V_{dc} = 1kV$, $r_g = 8\Omega$, $V_{gs,on} = 20V$ and $V_{gs,off} = -5V$.

In all cases, it can be observed that the highest *dv/dt* happens in the CSI switching cell, as expected. Since the $C_{oss,VSI}$ has an additional term (C_j), the VSI *dv/dt* is slowed down [31]. For that same reason, the VSI *di/dt* at turn-off is reduced, producing a lower v_{sw} overvoltage at high switching currents. On the other hand, at turn-on, the *di/dt* is unchanged, since it is meanly dictated by r_g and g_{fs}, which are common for both circuits [32]. Concerning the switching losses, the CSI presents the lowest values in all cases. However, when looking at the turn-off under high switching current, the ratio $E_{off,VSI}/E_{off,CSI}$ is almost unitary. This might arise from the fact that, at $I_{dc} = 50A$, the conditions for quasi-ZVS are not satisfied and the crossover loss term becomes preponderant over the capacitive one. Considering the turn-on transition, it is clear the influence of a larger capacitive loss term for the VSI, since $i_{sw,peak}$ reaches 80A for $I_{dc} = 10A$. In summary, the absence of an antiparallel diode (and then C_j) in the CSI switching cell allows decreasing switching losses by capping their main contributors: i_{sw} x v_{sw} crossover (by increasing *dv/dt* and *di/dt*) and capacitive terms.

It should be noted that during simulation, only the external drain current i_{sw} is measurable (and not i_{ch}). Then, switching losses are computed through $i_{sw} \cdot v_{sw}$. Due to the charge/discharge process of C_{oss}, the obtained losses are underestimated at turn-on and overestimated at turn-off. This issue will be further discussed in § 4.4.

3.5 Space Vector Modulation Strategies

When employing PWM converters, the nature of pulsed currents and voltages generated by the switching circuits must, in most cases, be filtered - that to fulfill power quality requirements and obligatory standards. However, a tradeoff exists between filtering efforts (and then costs) and power quality. For that reason, a precise description of converter's voltage and current spectrum must be carried out. The impact of different CSI Space Vector Modulation (SVM) strategies on AC current waveforms has been reported in the literature [5], [33]–[35]. However, the vast majority of these works deal with this topic comparing modulation strategy performances under relatively low switching frequencies, i.e., around 1kHz. In [36], the authors propose a methodology to evaluate the AC current spectrum of three-phase Current Source Converters (CSC) through their duality principles regarding Voltage Source Converters (VSC). Then, three modulations strategies are compared and experimental data is provided. Nevertheless, any indicator is given concerning the power quality of these modulations, as for example the Total Harmonic Distortion (THD). In this section, a similar methodology to the one proposed in [36] is employed, in order to investigate the impact of different SVM techniques operating at higher pulse rates (9kHz) on the AC current spectrum of CSIs.

3.5.1 Methodology for Current Spectrum Determination

To calculate the CSI phase current spectrum, the double Fourier integral method is applied. In the literature, this method is also referred as geometric-wall-model [36] and it has been widely used in power electronics since the 1970s to analytically determine the harmonic content of PWM waveforms [37]. As the name suggests, it is a frequency-domain method and is very useful to determine the harmonic components of a switched phase leg in VSCs, since it can be applied for any modulation method regardless the filter topology [5], [36]. Diversely, the geometric-wall-model cannot be directly applied to CSCs, since a binary notion does not exist within the phase legs, i.e., due to the special operation constraints, the upper and lower switches are not complementary. For that reason, some simplifications and the use of duality rules are necessary to correctly predict the CSC phase current spectrum using the double Fourier integral technique.

a) Duality between Voltage Source and Current Source Converters

First, let’s assume the generic three-phase VSC of Figure 3.19 (a) and its corresponding graph representation.

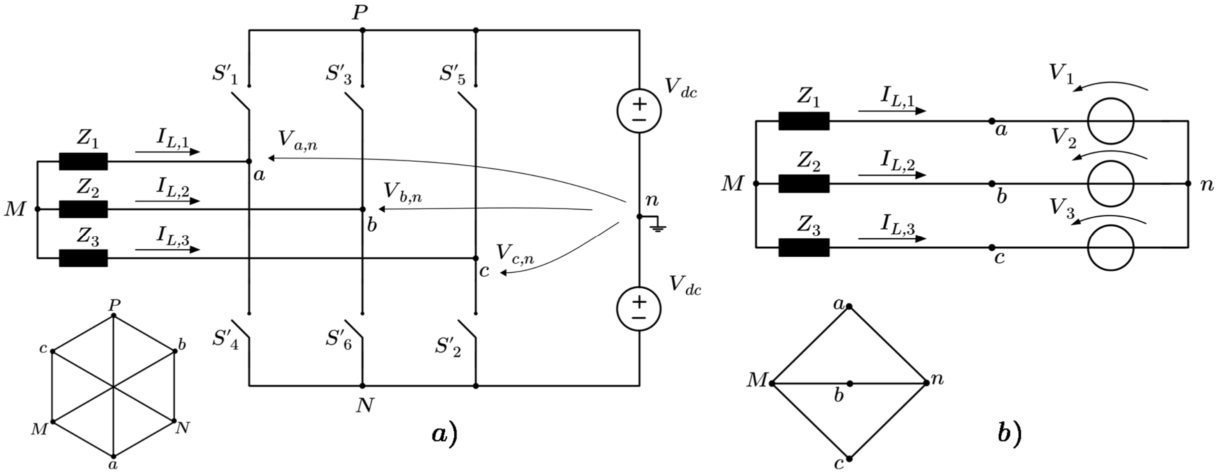


Figure 3. 19 – a) three-phase VSC and b) its simplified circuit. At the bottom their corresponding graphs are shown.

From graph theory, it is known that for a given circuit and its corresponding graph representation, a dual must exist, if and only if, the original graph is planar, i.e., if it can be drawn on a plane without any intersection of branches [38]. Knowing that, it becomes clear that the presented VSC does not have a direct dual. Therefore, a simplification should be applied. From the AC line impedance $Z_{1,2,3}$ point of view, the VSC bridge can be replaced by controlled voltage sources, as follows:

$$V_{1,2,3} = V_{a,b,c,n} = f_{1,2,3}(t) \cdot V_{dc} \tag{3.29}$$

where $f_{1,2,3}(t) \in [-1, 1]$ are binary switching functions. In Figure 3.19 (b), the resulting simplified VSC and its graph are shown. Now, without any intersection of branches, a dual can be derived.

The steps for the determination of the VSC dual graph are given in Figure 3.20. They can be summarized as follows:

i) Applying graph rules [38] to the simplified VSC, its dual network (since current and voltage orientations are defined) is obtained (in red);

ii) The dual circuit is redrawn for clarity. At this point, the duality principle between *i)* and *ii)* can be easily checked, since Y connections in the VSC circuit become Δ connections in its dual, voltage sources become current sources, impedances become admittances and so on. Moreover, when solving the VSC circuit and its dual and comparing the solutions, one concludes that the VSC loop currents become dual's node voltages, showing again the duality validity;

iii) The $\Delta - \mathrm{Y}$ transformation is applied to both sides of the dual circuit; and

iv) The inverse transformation of Eq. 3.29 is applied to obtain the three-phase CSC.

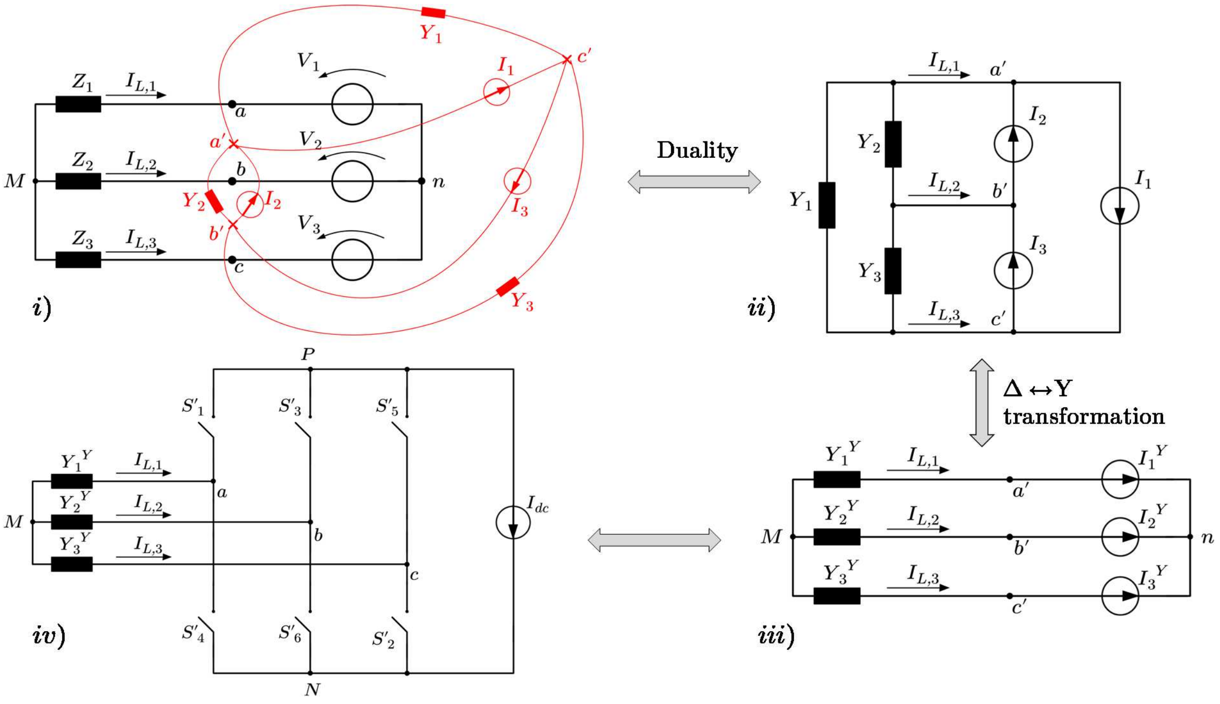


Figure 3. 20 – Step-by-step procedure to obtain the dual CSC circuit: *i)* simplified VSC and its dual circuit (in red); *ii)* dual circuit in Δ configuration; *iii)* dual circuit in Y configuration, after applying the $\Delta - \mathrm{Y}$ transformation and *iv)* three-phase CSC.

Finally, the CSC phase currents can be expressed as

$$i_{L,1}(t) = i_1^Y(t) = i_1(t) - i_2(t) = V_{a,n}(t) - V_{b,n}(t) \qquad (3.30)$$

From this equation, one concludes that for a given modulation strategy, the phase currents of a CSC correspond to the combination of two VSC phase-to-neutral voltages. Thus, applying the geometric-wall-model for these VSC phase voltages, the AC phase current spectrum of the related CSC can be obtained.

b) Double Fourier Integral Analysis

The phase-to-neutral PWM voltage waveform V_1 of a VSC phase leg can be considered as a function of two periodic and independent variables, namely $x(t) = \omega_c t + \theta_c$ and $y(t) = \omega_o + \theta_o$, where ω_c is the carrier angular frequency, ω_o is the fundamental angular frequency and θ_c and θ_o are arbitrary phase offset angles. Thus, from Fourier transform theory [5], $V_1(x,y)$ can be expressed as a summation of harmonic components, as follows:

$$\begin{aligned} V_1(x,y) = \frac{A_{0,0}}{2} &+ \sum_{n=1}^{\infty}[A_{0,n}\cos ny + B_{0,n}\sin ny] \\ &+ \sum_{m=1}^{\infty}[A_{m,0}\cos mx + B_{m,0}\sin mx] \\ &+ \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty}[A_{m,n} cos(mx+ny) + B_{m,n}\sin(mx+ny)] \end{aligned} \tag{3.31}$$

with the corresponding coefficients in complex form:

$$A_{m,n} + jB_{m,n} = \frac{1}{2\pi^2}\int_0^{2\pi}\int_0^{2\pi} f(x,y)\cdot e^{j(mx+ny)}dx\,dy \tag{3.32}$$

Eq. 3.32 presents a general form of the Fourier integral that must be solved to determine the harmonic components of V_1. However, to take into account the specificities of different SVM strategies, its integration limits must be adapted. This adaption should then consider the used carrier and reference waveforms. When employing a trailing edge sawtooth carrier, Eq. 3.32 becomes

$$V_1^{m,n} = \frac{V_{dc}}{2\pi^2}\int_0^{2\pi}\int_0^{\pi(1+M(y))} e^{j(mx+ny)}dx\,dy \tag{3.33}$$

And considering a classic triangle carrier waveform:

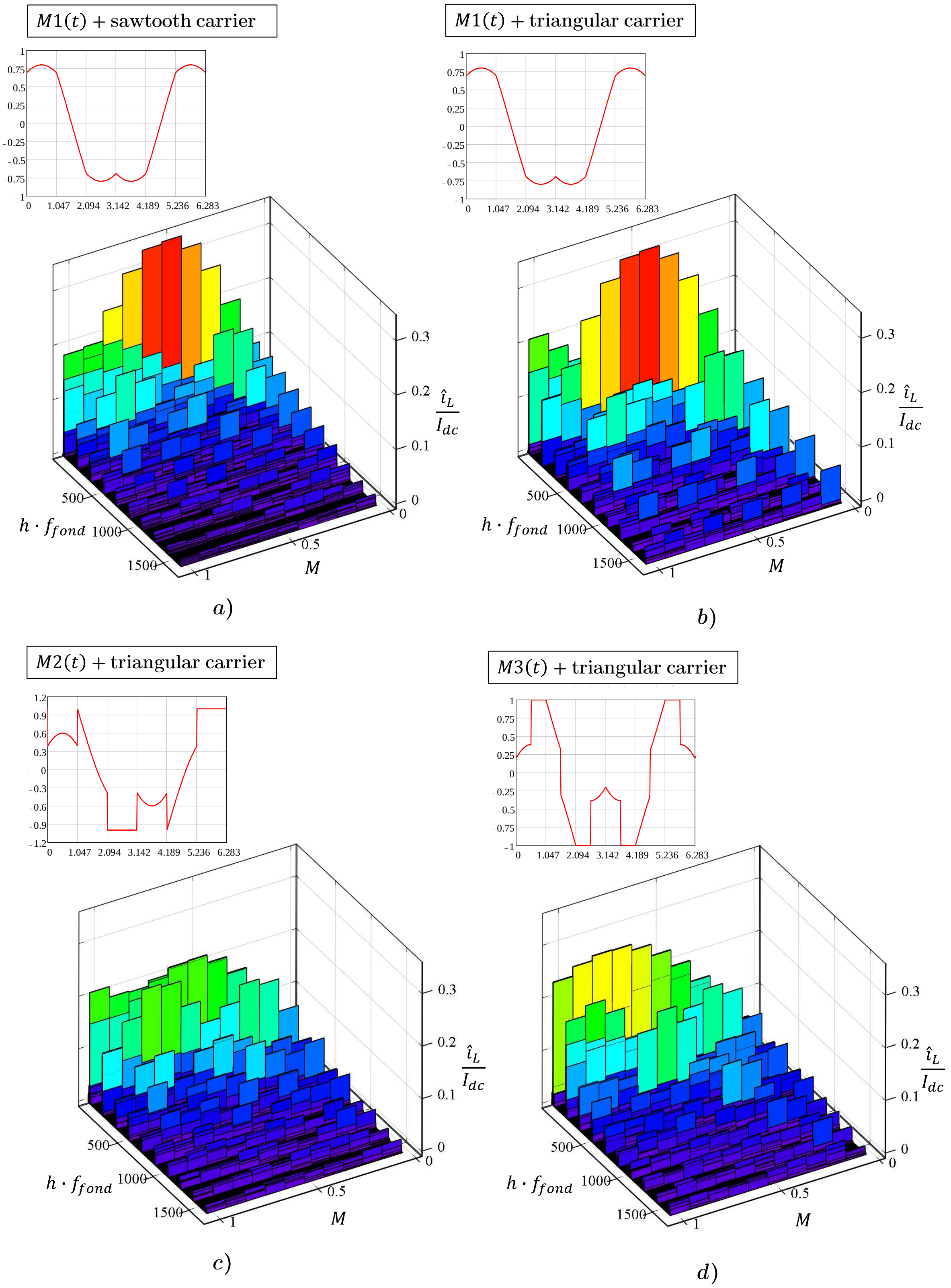
$$V_1^{m,n} = \frac{V_{dc}}{2\pi^2}\int_0^{2\pi}\int_{\frac{\pi}{2}(1-M(y))}^{\frac{\pi}{2}(3+M(y))} e^{j(mx+ny)}dx\,dy \tag{3.34}$$

The function $M(y)$ in the previous equations represents the adopted modulation or reference signal. For example, in the simplest case where sinus modulation is used, $M(y) = M\,cosy$, with M being the modulation depth. If third harmonic injection is intended, the reference function becomes $M(y) = M[cosy + 1/6\cos(3y)]$ and so on.

Here, it should be pointed out that the modulation function is an input to the double Fourier integral method. Thus, when analyzing a given space vector strategy, the first step to be taken consists on finding the corresponding “analog” modulation function to the specific space vector sequence. In [39], the relationship between SVM and carrier-based PWM is given.

3.5.2 Calculation Results

According to Eq. 3.32, calculations were carried out in order to determine the harmonic components of the CSI phase currents when employing four different SVM techniques. The complete current spectra are shown in Figure 3.21. For the calculations, a MathCad routine has been created to numerically solve the Fourier integrals. Then, the following parameters were assumed: $\omega_c/\omega_o = 9000/50$, the number of sideband harmonics is set to 40 and carrier harmonics are calculated until $1600 \cdot 50 = 80kHz$.



$a)$ $b)$

$c)$ $d)$

Figure 3. 21 – Current spectra normalized to the DC current as a function of the modulation index M and harmonic order h for the four studied SVM techniques. The fundamental components (@50Hz) are not shown. $f_c = F_{sw} = 9kHz$.

In order to quantitatively evaluate the obtained current spectra, the THD_i and the Distortion Factor ($DF_i^{\%}$) are defined as follows:

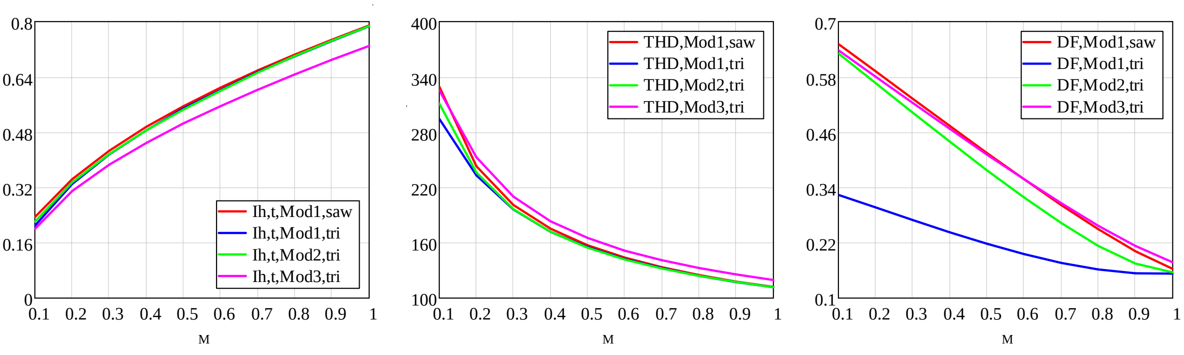
$$THD_i^{\%} = \frac{100}{I_{fond}} \sqrt{\sum\nolimits_{h=2}^{\infty} I_h^2} \tag{3.35}$$

$$DF_i^{\%} = \frac{100}{I_{fond}} \sqrt{\sum\nolimits_{h=2}^{\infty} \left(\frac{I_h}{h}\right)^2} \tag{3.36}$$

$$I_{h,T} = \sqrt{\sum\nolimits_{h=2}^{\infty} I_h^2} = \sqrt{i_L^2 - i_{fond}^2} \tag{3.37}$$

where I_{fond} and I_h are, respectively, the RMS value of the fundamental and the h^{th} phase current harmonic. In Eq. 3.37, $I_{h,T}$ represents the RMS value of all harmonic components of I_L.

For each modulation technique, the aforementioned indicators are calculated and presented in Figure 3.22.



a) *b)* *c)*

Figure 3. 22 – a) RMS value of all harmonic components summed, b) $THD_i^{\%}$ and c) $DF_i^{\%}$. All three parameters are calculated until the 1600th harmonic component, i.e., 80kHz.

Analyzing the results from Figure 3.21, it can be concluded that the obtained current spectra are consistent with the theoretical and experimental data provided in [36]. Concerning the THD_i, all four modulations can be considered to be quite equivalent. Nevertheless, it should be pointed out that this indicator does not take into account the order of the harmonic components and thus, should not be used when no filtering element is present. On the other hand, the DF_i demonstrates that the Modulation technique 1 in combination with a triangular carrier shows considerably improved harmonic behavior. However, the price to be paid for passing from a sawtooth carrier to a triangular carrier is that the switching operations are doubled (and then the switching losses) [36]. Regarding the total RMS harmonic current, Mod3 presents a reduction, which could be an advantage during filter design phase in high-current CSI applications.

3.6 Summary and Conclusion

In this chapter, the CSI principle of operation has been presented. Furthermore, the conduction losses mechanisms have been discussed in detail together with their associated electro-thermal coupling effects. This will serve as the basis for the following chapters.

Among the four CSI variations investigated in the present chapter, the standard CSI seems to find its place thanks to its simplicity and capability to operate within the entire $cos\varphi$ range. As a result, this switching configuration has been adopted and will be implemented in a novel full-SiC power module in the subsequent chapter. However, the Delta-type CSI is still a very good candidate for medium- and low-power PV applications. In fact, the cost-effectiveness of such a solution could be considerably improved if the diode's voltage rating is reduced – since its blocking voltage is 15% lower than that of the MOSFETs. For example, with an appropriate layout (to limit turn-off overvoltage) and operating on a 690V grid, 1200V SiC diodes and 1700V SiC MOSFETs might be a possible solution.

Although not investigated in this work, the impact of different CSI modulation strategies on Common Mode (CM) current generation is crucial for PV applications, especially in the low-power range, where no transformer is present between the PV inverters and the grid. In [7], a specific zero vector selection criteria is proposed to reduce the CM current to the ground. Nonetheless, as far as the author is aware, at the present time no extensive investigation has been conducted to evaluate the tradeoffs between CM current generation, AC line current spectra and switching losses in CSI modulation strategies.

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Chapter 4

Design and Characterization of a Novel 1.7kV Full-SiC Power Module

The scope of this chapter covers the semiconductor power integration for the Current Source Inverter. Initially, based on the topology specificities and the target PV application, attention is given to the design of a novel 1.7kV full-SiC power module. With this objective in mind, all steps to an industrial realization of this new device are discussed – from the packaging material selection, passing by the substrate and housing layout designs to the choice of semiconductor bare dies. The second part of Chapter 4 is dedicated to the dynamic characterization of the developed SiC module. To implement the double-pulse test technique, a wide-bandwidth current sensor is developed and its performance is compared to other state-of-the-art current sensor techniques'. Then, switching losses are obtained, which will serve as the basis for the CSI design later in this work. Furthermore, the tradeoffs between EMI generation potential and switching speed is discussed based on the switching speed characterization.

4.1 Introduction

In a converter system, the power semiconductors can be used as discrete devices or integrated in power modules. Typically, discrete devices are employed in low-power applications, whereas power modules are often utilized in medium- and high-power converters (several tens of kW and beyond) [1]. Comparing both technologies, the latter is associated with improved thermal performance and reliability [2]. Furthermore, when paralleling of devices is necessary to increase current capability, integrating all semiconductors in the same packaging helps to reduce parasitics, which in turn improves the overall converter performance [3].

Taking into account the power requirement in the present work (60kW, as it will discussed later in this chapter) and the aforementioned reasons, a good approach to the CSI realization seems to be the multi-chip power module. Figure 4.1 presents some of the most widespread Si-based power module configurations available on the market [4].

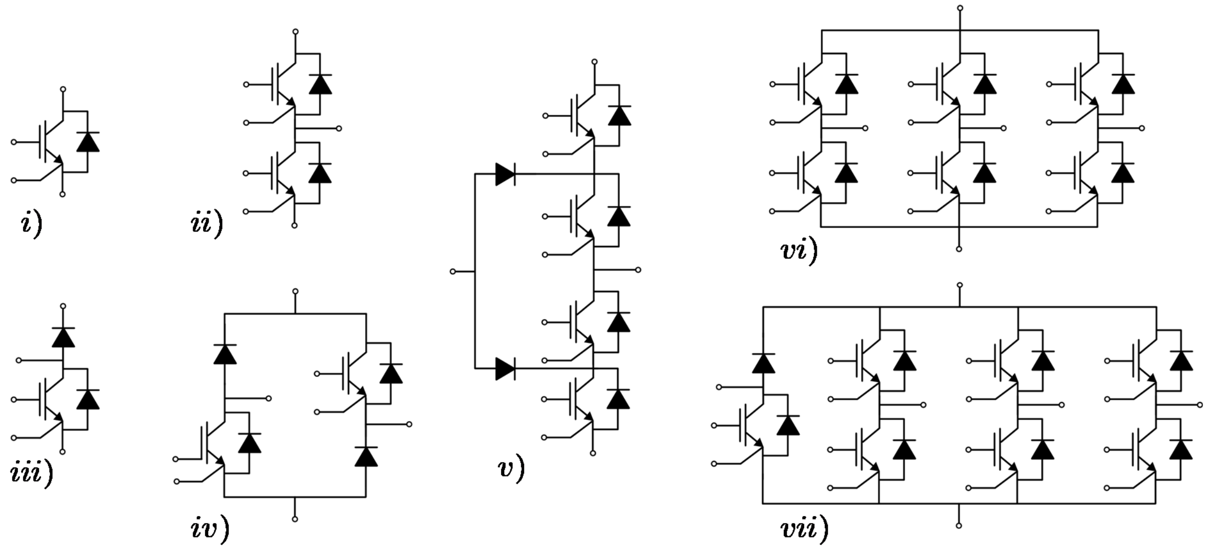


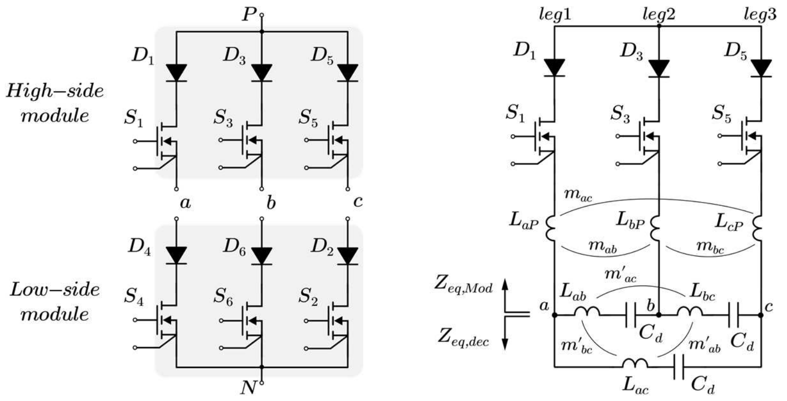
Figure 4. 1 – Most common commercially available Si-based power modules.

As can be seen, the most commonly used module switch configurations do not present reverse voltage blocking capability. When looking at the available SiC power module market, the range of choices is even reduced. For that reason, the development of a new SiC device adapted for CSI applications is required.

In this chapter, a preliminary study of the module's substrate layout is carried out through electromagnetic and electrical simulations, in order to investigate the influence of unbalanced stray inductances on the switching cell's performance. Based on theoretical and experimental results, specific switch arrangements are proposed to equilibrate all CSI switching cells. The experience and knowledge obtained from this study serve as the basis for the development of a novel multi-chip 1.7kV full-SiC power module. Moreover, the dynamic characterization of the new developed device is carried out through the double-pulse test technique employing a high-frequency double-stage current transformer.

4.2 Power Integration for Current Source-based Topologies

In order to reduce the parasitic elements in the commutation loop, all semiconductor dies forming the switching cell should be integrated in the same module packaging [4]. Considering VSCs, the phase-leg configuration is commonly used. However, in CSC applications, this arrangement is no longer adequate, since the switching cells alternate between legs. Hence, a reasonable solution is to integrate all high-side (HS) (or low-side (LS)) switches, then the three switching cells, in the same power module packaging, as shown in Figure 4.2 (a).



a) b)

Figure 4. 2 – a) CSI power module configuration and b) lumped-circuit model for the high-side module.

Figure 4.2 (b) shows a lumped-circuit model for the CSI high-side module including the decoupling capacitors (C_d). In order to obtain identical switching characteristics (*dv/dt*, *di/dt*, voltage overshoot, etc.) for all three switching cells, the equivalent impedance seen between the points $a - b$, $b - c$ and $a - c$ must be as similar as possible. The most straightforward solution to fulfill this condition is to impose an electrical symmetry in both module ($Z_{eq,Mod}$) and decoupling capacitors ($Z_{eq,dec}$) sides, to yield $Z_{eq,Mod,a-b} = Z_{eq,Mod,b-c} = Z_{eq,Mod,a-c}$ and $Z_{eq,dec,a-b} = Z_{eq,dec,b-c} = Z_{eq,dec,a-c}$. Thereby, one ensures that all semiconductors in the CSI power module will withstand the same overvoltage and overcurrent during switching transients.

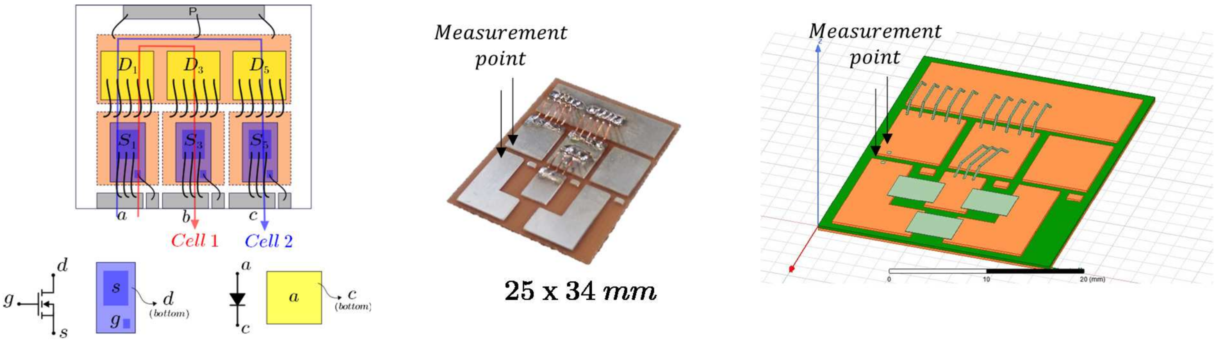
From a manufacturing point of view, it is preferable that the high- and low-side modules share a common substrate layout which helps to increase standardization, then reducing costs. Furthermore, any additional industrial process targeting to modify the devices' electrodes metallization is not recommended. This could significantly complicate the module's fabrication and impede the cost effectiveness of such a solution [3].

4.2.1 Module Substrate Design

a) Conventional layout

A conventional HS module is presented in Figure 4.3 (a). In this configuration, the bare dies are disposed side by side on the substrate. This juxtaposing arrangement leads to an asymmetry in the switching loops. Obviously, the switching cells between points $a - b$ or $b - c$ (Cell1) are shorter than the switching cell $a - c$ (Cell2). As a consequence, Cell2 stray inductance (L_{Cell2}) tends to be greater than that in the other commutation loops (L_{Cell2}). Furthermore, this module layout makes it more difficult to achieve a balanced decoupling system, since there will always be one switching cell which is decoupled through a longer path (i.e., switching cell $a - c$).

These inconveniences are even more accentuated for WBG devices, since they exhibit extreme di/dt and dv/dt dynamics [5]. The side effects of this switching loops asymmetry were shown in [6], but no solution has been proposed.



a) b) c)

Figure 4. 3 – a) Conventional CSI high-side module, b) substrate layout prototype and c) Q3D model.

On the other hand, placing the dies side by side allows a better substrate utilization (i.e., fill factor), leading to cost reduction and increased power density. In addition to this, the square format of the substrate and the presence of only right angles lead to optimized manufacturing processes.

b) Alternative layouts: "Y" and "Δ" balanced switching cells

With the aim of balancing all CSI switching cells, two alternative layouts are proposed, as shown in Figure 4.4 (a) and Figure 4.5 (a). Herein, the approach consists of imposing a rotational symmetry of order three (i.e., 120°) between all module legs. The center of rotation being composed of the common node N or P, for LS and HS modules, respectively.

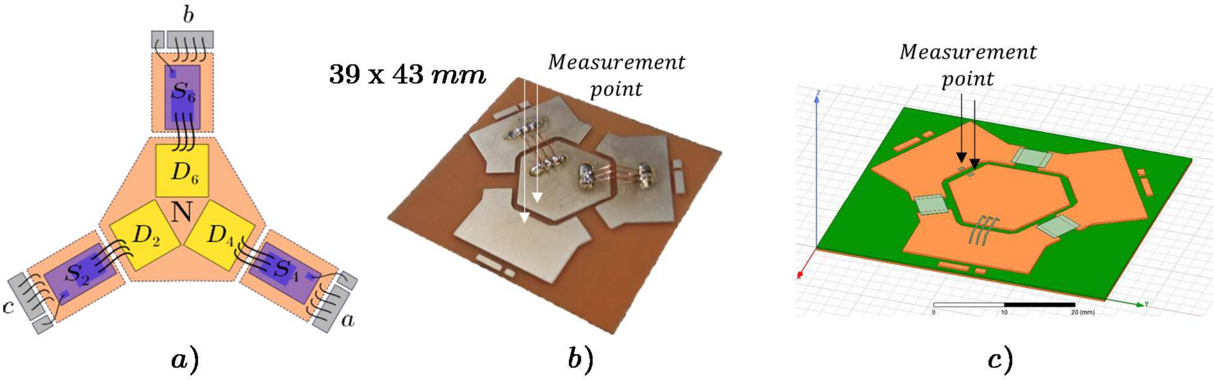


Figure 4. 4 – a) "Y" balanced CSI low-side module, b) substrate layout prototype and c) Q3D model.

Due to its symmetric geometry, the proposed "Y" and "Δ" layouts allow a balanced system in terms of switching cell stray inductances as well as for the decoupling capacitors. Nevertheless, these balanced layouts lead to a poorer substrate utilization (lower fill factor) as well as a more complex geometry, which might degrade its manufacturability.

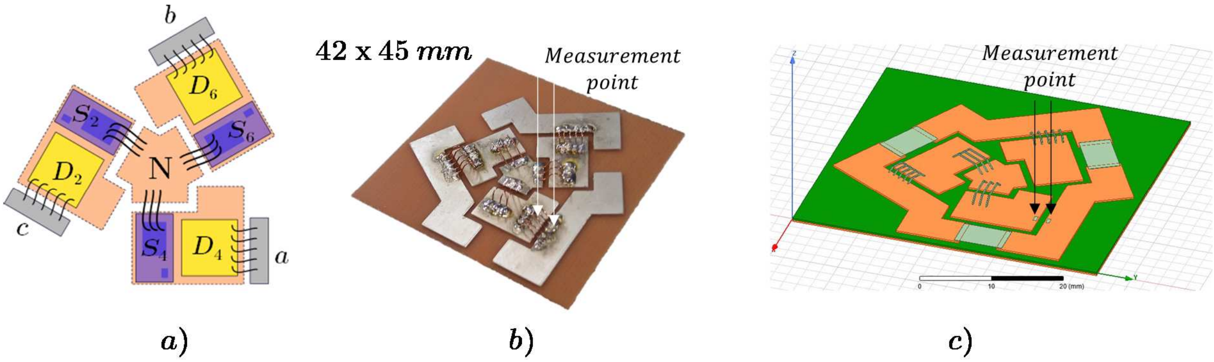


Figure 4. 5 – a) "*Δ*" balanced CSI low-side module, b) substrate layout prototype and c) Q3D model.

4.2.2 Electrical Performance Evaluation

a) Preliminary case study: substrate without backside metallization

With the purpose of evaluating the layouts described above, three different prototypes were built. The devices are shown in Figures 4.3 (b), 4.4 (b) and 4.5 (b). In all substrates, FR4 is chosen as the insulating material (300µm thick) on which a front side copper metallization of 230µm thick is deposed. The bare die interconnections are realized through wire-bondings of 250µm in diameter (3 and 5 wire-bondings for the connection of MOSFETs and diodes, respectively). Additionally, it is considered that the switching cells are decoupled with ceramic capacitors (C_d in Figure 4.2 (b)) directly soldered on the module metal substrate (for measurement simplicity, the capacitors are basically replaced by a short circuit, due to their relatively low impedance at high frequencies). It is important to emphasize that, as a first step, the substrates were fabricated without any backside metallization.

Thus, the electrical evaluation of the prototypes is carried out according to the following protocol:

- for the conventional layout, considering Cell1 parasitic extraction, the module's leg3 and leg1 are disconnected (by removing the wire-bondings in these respective legs) and then, the stray inductance is assessed from the measurement points shown in Figure 4.3 (b). Regarding Cell2 parasitic extraction, the module's leg2 and leg1 are disconnected, allowing then to obtain the equivalent stray inductance from Cell2 measurement points; and
- for the balanced layouts, the equivalent stray inductances are obtained from the measurement points shown in Figures 4.4 (b) and 4.5 (b) while disconnecting one of the two remaining legs.

In order to assess the layout's stray inductances, the wide bandwidth precision impedance analyzer Keysight model E4990A (120MHz) in combination with the impedance probe kit 42941A are used. The expected inductance measurement accuracy for all setups in this work is estimated to be between 1 and 10% [7]. Figure 4.6 shows the impedance measurement setup.

a) *b)*

Figure 4. 6 – a) Impedance Analyzer E4990A and b) impedance probe adapter 42941A.

Finally, based on the equivalent upper limit frequency approximation [8], a measurement testing frequency of 20MHz is chosen (considering a current rise/fall time of $t_{r,f} \cong 20ns$). The results are presented in Table 4.1.

Table 4. 1 – Comparison of measurement and simulation results.

Layout	Conventional		"Y" balanced	"Δ" balanced
	Cell1	Cell2		
Q3D Simulation (nH)	12.50	20.56	7.89	15.06
Measurement (nH)	11.95	19.04	7.24	13.57

To verify the validity of the obtained measurement results, electromagnetic simulations are performed using the Finite Element Analysis (FEA) software Ansys Q3D Extractor. The Q3D substrate models, which have the same characteristics than the respective prototypes, are depicted in Figures 4.3 (c), 4.4 (c) and 4.5 (c). To comply with the experimental protocol, a 20MHz testing signal is selected for layout evaluation. The simulated stray inductance values are presented in Table 4.1, showing a good agreement with the experimental results.

According to Table 4.1, the superiority of the proposed balanced layouts compared to the conventional one is clearly demonstrated. The "Y" layout shows a reduction of 36.9% in terms of parasitic inductance, with respect to the best conventional module switching cell (Cell1).

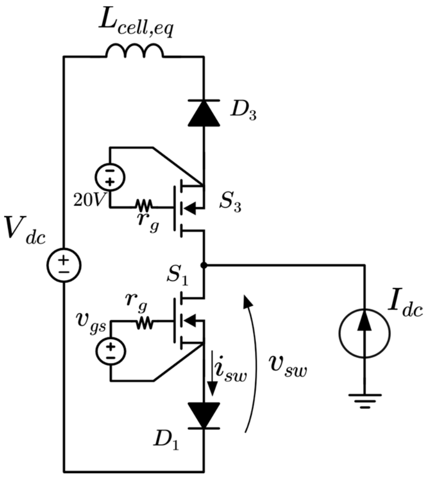
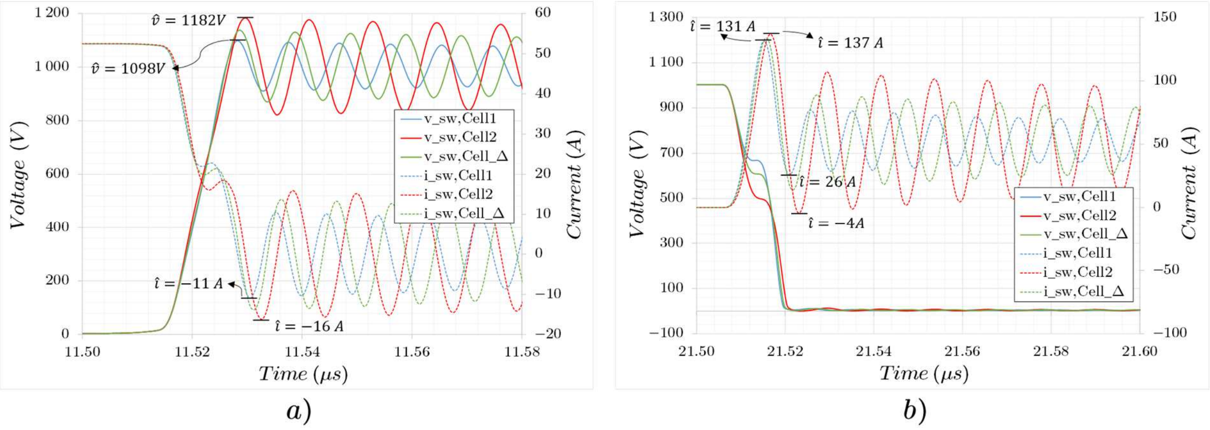


Figure 4. 7 – LTspice double-pulse test circuit. $V_{dc} = 1kV$, $V_{gs} = 20/-5V$ and $r_g = 2.5\Omega$

To verify the effects of stray inductance in the CSI switching waveforms, a double-pulse test (DPT) circuit is implemented in LTspice (cf. Figure 4.7). The Spice die models C2M0040170D and CPW51700Z050B, from Wolfspeed [9], are used for the MOSFETs and diodes, respectively. The simulated stray inductance value for both modules (conventional and "Δ" balanced) are used in the DPT circuit ($L_{cell,eq}$ in Figure 4.7). The switching waveforms are shown in Figure 4.8.

Considering the conventional module, it can be seen from LTspice simulations that there is a significant behavioral difference in switching transients between Cell1 and Cell2. During turn-off transitions, the switches involved in commutation loop Cell2 block 118% of the bus voltage (i.e., 1182V) while switches in Cell1 block 110% (i.e., 1098V). On the other hand, the proposed "Δ" layout clearly eliminates this unbalance drawback, yielding identical commutations (then balanced constraints over the semiconductors) with lower switching overvoltages (when compared to conventional layout Cell2). Furthermore, EMI aspects might be improved, since current oscillations are also significantly reduced [10].



a) *b)*

Figure 4. 8 – 1000V / 50A ($r_g = 2{,}5\Omega$) switching waveforms at turn-off a) and turn-on b) transients. The indices Cell1 and Cell2 represent both switching cells in the conventional module, whereas $Cell\_\Delta$ refers to the "Δ" balanced module layout.

b) Second case study: substrate with backside metallization

In order to investigate the influence of the backside metallization on the layout parasitic elements, a second series of prototypes was built. The new substrates are similarly designed than those previously presented, except for the added 230µm copper backside metallization. For these new layout setups, the stray inductances are measured and simulated according to the same protocol described in the previous section. The results are presented in Table 4.2.

Table 4. 2 – Comparison of measurement and simulation results.

Layout	Conventional		"Y" balanced	"Δ" balanced
	Cell1	Cell2		
Ansys Q3D Simulation (nH)	6.00	6.61	3.75	6.64
Measurement (nH)	5.66	5.89	3.08	5.82

Here, the simulated and experimental results are in good agreement as well. Furthermore, all parasitic inductance values have been strongly reduced. Irrespective of the layout structure, the stray inductance decreased by a factor greater than two. Nevertheless, regarding the conventional module, the relative difference between $L_{stray_{Cell1}}$ and $L_{stray_{Cell2}}$ has not followed this tendency: now, both switching cells are almost balanced. Figure 4.9 shows the surface current density magnitude ($|\overrightarrow{J_{ac}}|$) for an excitation of 1A/20MHz, in the case of the conventional module Cell2.

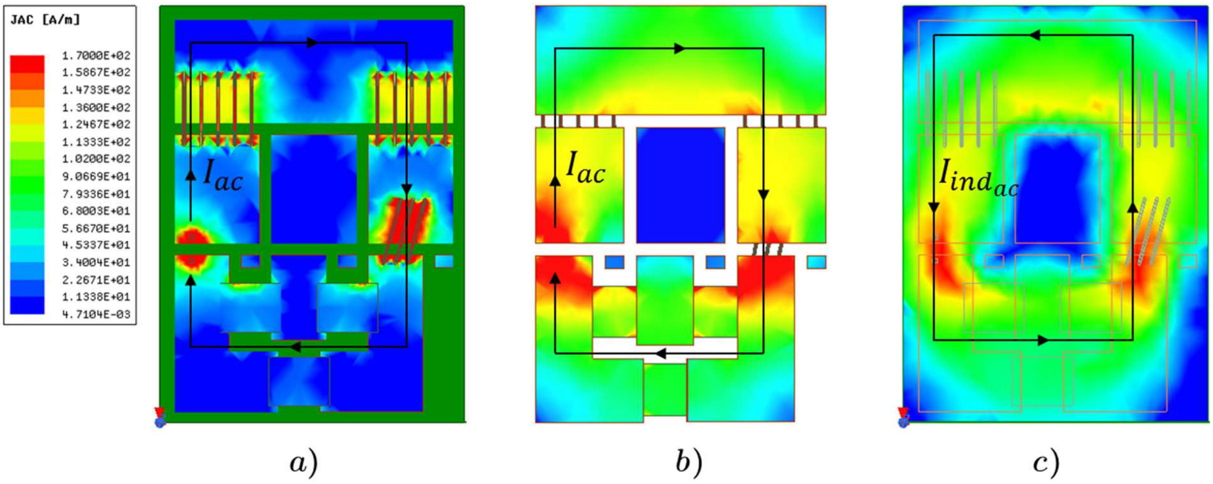


Figure 4. 9 – Alternating current vector module ($|\overrightarrow{J_{ac}}|$) at 20MHz for: a) front side metallization (top), b) front side metallization (bottom) and c) backside metallization (top).

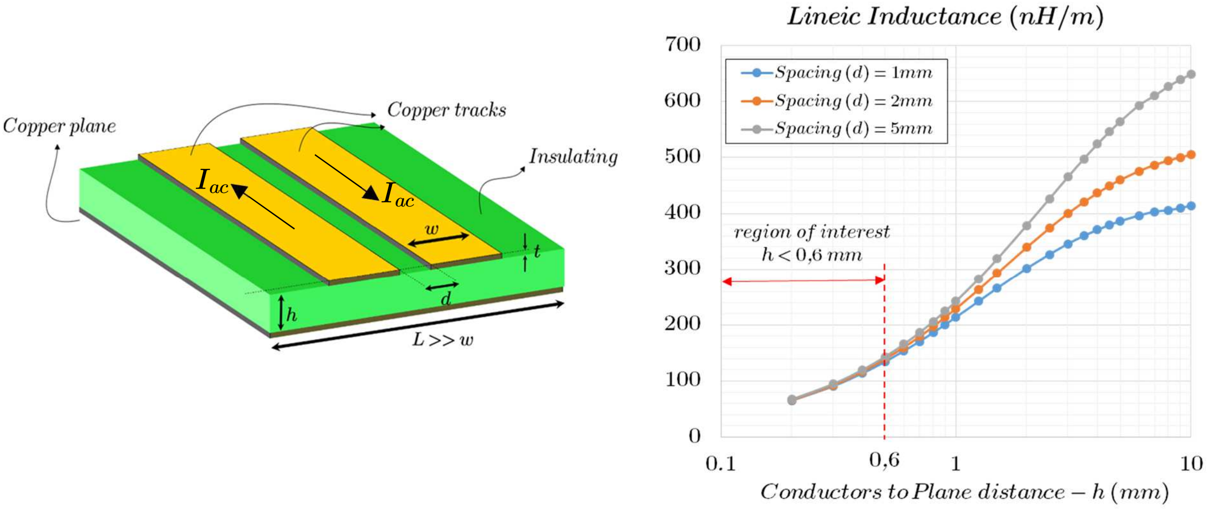
The parasitic inductance reduction in all layouts can be explained by the induced eddy currents in the backside copper layer ($I_{ind,ac}$ in Figure 4.9 (c)) [11]–[13]. Due to proximity effect, the current excitation (I_{ac}) flowing in the substrate front side metallization (see Figure 4.9 (a) and (b)) induces a surface current

($I_{ind,ac}$) in the backside metallization. This net induced current $I_{ind,ac}$ equals zero (since the backside metallization is open-circuited) and has the same magnitude but opposite direction of its source (according to Lenz's law) [11]. As a result, the net magnetic field around the front side conductors decreases, reducing then the corresponding partial inductance [12].

Nonetheless, the balance between the conventional layout switching cells cannot be explained by this analysis. For that reason, the next section is dedicated to this topic, but in a more generic case.

4.2.3 Qualitative Modeling of a Coupled Microstrip – a Generic Case

The case of the conventional layout switching cells can be generalized via a coupled microstrip circuit. This problematic, well known in telecommunications domain [14], is presented in Figure 4.10 (a). To set an example, the following values are considered in the analysis: width $w = 7mm$ and thickness $t = 230\mu m$.

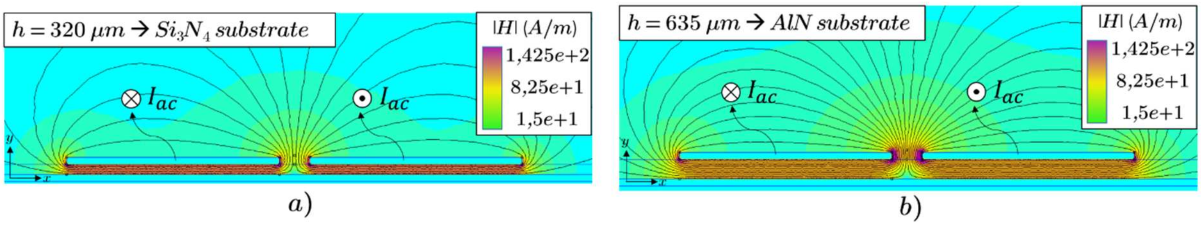


a) b)

Figure 4. 10 – a) Coupled microstrip schematic and b) lineic inductance as a function of the substrate thickness h.

The front side tracks represent two adjacent legs in the conventional module. Thus, each track is crossed by an alternating current (I_{ac}) of opposite directions. To verify the dependency of the track's partial inductance with respect to substrate thickness (h), FEA electromagnetic simulations are performed using FEMM software. Thus, three different track spacing values (d) are employed and an excitation signal of 20MHz is applied. The results are presented in Figure 4.10 (b).

As can be seen, the track's inductance per unit length strongly depends on the substrate thickness, as discussed in the previous section. Furthermore, when the insulating substrate is thin enough (i.e., $h < 0.6mm$), the lineic inductance becomes independent of the track spacing (d). In such a case, the majority of the magnetic field (and then the magnetic coupling) is confined between the front and backside metallization and not between the tracks. This fact explains the reduced difference between $L_{stray,Cell1}$ and $L_{stray,Cell2}$ with the presence of a substrate backside metallization. Figure 4.11 illustrates the magnetic field magnitude distribution for two typical values of substrate thickness (h), when $d = 1mm$.



a)

b)

Figure 4. 11 – Magnitude of the magnetic field distribution considering a) $h = 320\mu m$ and b) $h = 635\mu m$. The thickness of 320µm and 635µm are often employed in Si_3N_4 and AlN substrates, respectively.

In the case of a relatively high substrate thickness ($h = 635\mu m$ – typically the case for AlN substrates), the surface currents are no longer concentrated along the x-axis but also in the y-direction, due to an increased coupling between the tracks. Thus, the net magnetic field around the front side tracks and in between them is increased, leading to a higher inductance value [12].

As previously discussed, the substrate backside metallization has a strong influence on the switching cells' stray inductances, tending to naturally balance them. Nevertheless, in the case of a module with external decoupling capacitors, the "Δ" and "Y" layout solutions remain attractive.

4.3 Industrial Realization of the Full-SiC CSI Module

4.3.1 Material Selection

In most applications, the power module must ensure the electrical contact and insulation between parts, conduct and spread the generated heat flux from the chips to the cooling system, mechanically support the electrical parts and protect them from the external environment (against humidity and dust, for example) [1], [15]. In order to successfully meet these requirements, several elements must be assembled. Figure 4.12 depicts a standard power module structure with its stack-up materials.

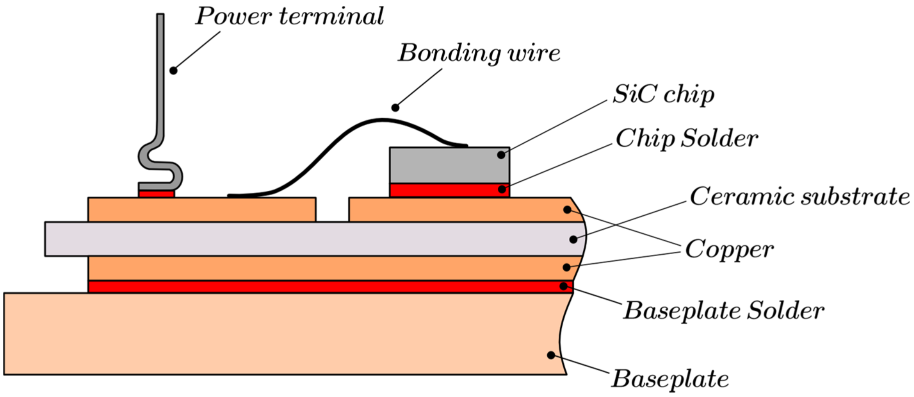


Figure 4. 12 – Basic structure of a power semiconductor module with baseplate. The housing and encapsulating material are not shown.

In order to improve the converter's power density, the junction-to-case thermal resistance should be minimized. This can be accomplished by increasing the module's chip area or improving the overall stack-up materials thermal conductivity. Furthermore, reliability aspects must be considered when designing the module. Since PV inverters does not operate at constant load, temperature gradients exist within the package. This leads to a mechanical stress or fatigue between adjacent layers, since the materials forming the module exhibit different coefficients of thermal expansion (CTE). For that reason, the materials should be selected in such a way that their CTEs are as close as possible.

a) Ceramic substrate

As presented in Figure 4.12, the semiconductors must be electrically isolated from the baseplate. A good compromise between thermal conductivity and electrical insulation is found in metallized ceramic substrates [1]. In the following, the pros and cons of the three most widespread ceramic substrates are given [1], [15], [16]:

- Alumina (Al_2O_3): low-cost material and mature technology / poor thermal conductivity and CTE mismatch with SiC;
- Aluminium Nitride (AlN): good thermal conductivity, high dielectric strength and improved CTE matching with SiC (compared to Al_2O_3) / poor cycling capability; and
- Silicon Nitride (Si_3N_4): good CTE matching with SiC and good mechanical properties, leading to high temperature cycling capability (especially for

substrates fabricated through Active Metal Brazing (AMB) process) / emerging technology and reduced thermal conductivity (compared to AlN).

In Table 4.3 are summarized the main properties of the aforementioned ceramics. A more detailed description of their mechanical characteristics can be found in [16].

Table 4. 3 – Characteristics of the considered ceramics [1], [3].

Material	Thermal Conductivity (W/m.K)	CTE (ppm/K)	Dielectric strength (kV/mm)	Relative permittivity (ε_r)	Bending strength (MPa)
Al_2O_3	24	6.8	15	9.8	350
AlN	180	4.7	20	9.0	360
Si_3N_4	70	3.4	14	9.2	700
SiC	260 @100°C	3	-	-	-

Taking into account its good mechanical properties, the Si_3N_4 substrate fabricated through AMB process is selected in this work. It should be pointed out that the drawback of poor thermal conductivity can be overcome by implementing thinner substrates. While the standard thickness of AlN substrates is 635µm, manufacturers are able to produce Si_3N_4 with 320µm in thickness (thanks to its mechanical characteristics) [17]. In doing so, excellent thermal cycling capability with an AlN-like thermal resistance can be achieved. Nonetheless, the price to be paid for this reliability improvement is that the parasitic capacitance per unit area with respect to ground is increased by nearly a factor of two (see ε_r in Table 4.3), directly impacting EMI behavior.

b) Baseplate

Most power modules utilize a baseplate to conduct the heat flux from the substrate to the heatsink. The baseplate serves as a mechanical support and heat storage to the module. Also, it helps to spread the heat and homogenize temperatures within the package. In the following, the pros and cons of the two considered baseplate materials are presented [15], [16]:

- Copper (Cu): low-cost material and excellent thermal conductivity / substantial CTE mismatch with SiC and high-mass density material; and
- Aluminum/Silicon Carbide (AlSiC): good CTE matching with ceramic substrates and low-mass density material / additional manufacturing costs and poor thermal conductivity (both compared to Cu).

Their characteristics are compared in Table 4.4.

Table 4. 4 – Characteristics of the analyzed baseplate materials [3], [15].

Material	Thermal Conductivity (W/m.K)	CTE (ppm/K)	Young modulus (GPa)	Mass density (g/cm^3)
Cu	398	17.8	130	8.96
AlSiC	175	8	240	3

Due to its good thermal conductivity and the high cost-sensitivity of PV inverters, Cu is the selected material for the baseplate. This implies however a proper solder alloy selection between the substrate and the baseplate: a good stress-absorbing solder is required, i.e., having low elastic modulus, high mechanical strength and fatigue resistance [16].

c) Soldering

In order to bond together the different components of a power module, soldering is commonly employed [15]. Different solder alloys are then applied between layers to meet manufacturing and mechanical requirements. In all cases, the solder layer should guarantee: high electrical and thermal conductivity, matching CTE with regard to the layers to be soldered and good mechanical properties. During the manufacturing process, the semiconductor chip is firstly soldered on the substrate with a high-temperature solder alloy, i.e., $T_{melting} > 250°C$. This is normally achieved with high Pb content alloys. Secondly, the substrate is soldered on a baseplate through a low-temperature soldering process, $T_{melting} < 250°C$. Thanks to their good mechanical properties, maturity and relatively low cost [16], the high-temperature alloy Pb92.5/Sn5/Ag2.5 is selected for the chip-substrate solder. The substrate-baseplate solder is chosen to be Sn96.5/Ag3.5, since it is compatible with the selected Cu baseplate [16]. The chosen alloy's characteristics are summarized in Table 4.4. The Sn/Ag alloy is also employed to solder the module's terminals.

Table 4. 5 – Characteristics of the employed solder alloys [15], [18].

Soldered Components	Alloy	Liquidus Temp. (°C)	Thermal Conductivity (W/m.K)	CTE (ppm/K)
Chip-substrate	Pb92.5/Sn5/Ag2.5	296	44 @110°C	29
Substrate-baseplate Terminals-substrate	Sn96.5/Ag3.5	221	33 @85°C	22

d) Interconnections

The internal module's interconnections are realized through Al wire-bondings. To alleviate and share the thermal constraints imposed by the high-current density levels of SiC modules, as many wire-bondings as possible are placed on the die's top-side metallization. Moreover, this helps to reduce the associated parasitic inductance, since the net magnetic field around the wires tends to decrease, approximating that of a solid ribbon [12]. The external terminals are Cu-based and they are selected to be solderable, allowing to have a low-profile module, which is critical factor to reduce parasitic inductances (this will be further discussed in § 4.3.4).

In Table 4.6, the final CSI module characteristics are summarized.

Table 4. 6 – CSI module characteristics.

Component	Material	Characteristics
Bonding wire	Al	5 x ø 300μm (diode) 3 x ø 300μm (MOSFET) 1 x ø 125μm (MOSFET gate)
Substrate	Cu/Si_3N_4/Cu	Thickness: 300/320/200μm Size: 50.8 x 50.8 mm
Chip solder	Pb92.5/Sn5/Ag2.5	Thickness: 90μm Liquidus temp.:296°C
Baseplate solder	Sn96.5/Ag3.5	Thickness: 200μm Liquidus temp.:221°C
Baseplate	Cu	Thickness: 4mm Size: 60 x 80mm
Encapsulation material	Silicone gel (TSE 3062)	Thermal conductivity: 0.17W/m.K Dielectric strength: 18kV/mm
Housing	Plastic (PBT)	Max. operating temp.: 125°C

4.3.2 Definition of Module Voltage and Current Ratings

The semiconductor voltage rating is linked to the AC grid voltage, as discussed in § 3.2.4. In this work, the developed CSI module is meant to operate on a three-phase 690V grid. From Eq. 3.18, $V_{rating} > 1120V$, considering 15% of grid fluctuations and no safety margin. Given that, it becomes apparent that 1.2kV devices are not suitable for the application. Therefore, for all diodes and MOSFETs, $V_{rating} = 1.7kV$.

On the other hand, the module current rating cannot be readily determined, since it is linked to thermal limits of the module's components and a tradeoff between efficiency and chip area (i.e., costs). For a given converter power rating (P_n) and switching frequency (F_{sw}), the maximum allowed junction-to-case thermal resistance ($R_{th,j-c,max}$) should be firstly defined to insure safe operation under the worst case scenario. Then, the minimum number of chips in parallel is determined for a given stack-up of materials forming the module. Finally, efficiency calculations can be carried out and the final number of chips in parallel (n) obtained. In the following, these steps are presented using the same Wolfspeed devices introduced in § 3.3.3.

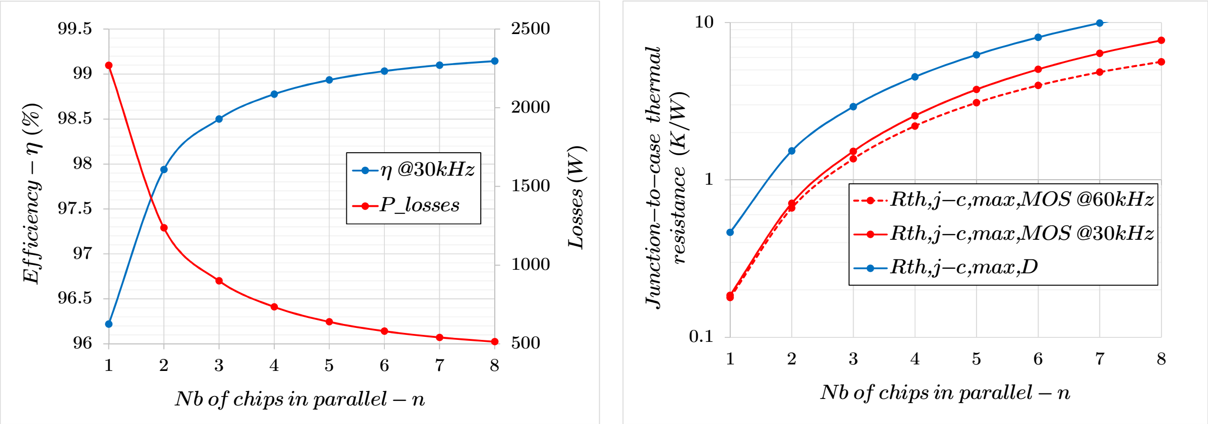
The CSI losses are maximized when the inverter operates at the lowest MPP voltage and nominal power. In that condition, junction temperatures should not exceed $T_{j,max}$. Then, $R_{th,j-c,max}$ per die is defined:

$$R_{th,j-c,max} = \frac{T_{j,max} - T_{case}}{P_{cond}(T_{j,max}) + P_{sw}} \tag{4.1}$$

where P_{cond} and P_{sw} refer to conduction and switching losses per chip, respectively (for the diodes $P_{sw} = 0$). Considering the modulation technique Mod1 in combination with a sawtooth carrier, switching losses are defined as

$$P_{sw}(F_{sw}, I_{dc}) = \frac{F_{sw}}{2\pi} \int_{0}^{\pi/2} E_{sw,MOS}(\theta, I_{dc}) d\theta \tag{4.2}$$

Thus, assuming $P_n = 60kW$ and $V_{MPP,min} = 665V$ (leading to $I_{dc} = 90A$), a set of LTspice simulations is carried out to obtain $E_{sw@90A}(V_{ds}, n)$. Conduction losses are modeled as in § 3.3.1. Finally, considering the thermal limits $T_{j,max} = 150°C$ and $T_{case} = 100°C$, the maximum allowed junction-to-case thermal resistance per die is calculated (cf. Figure 4.13).



a) b)

Figure 4. 13 – a) Total semiconductor losses and efficiency as a function of n and b) maximum allowed $R_{th,j-c}$ per die. Conditions: $I_{dc} = 90A$, $T_j = 125°C$, $V_{grid} = 690V$; $r_{g,on} = 2 \cdot r_{g,off} = 2.5\Omega$.

Due to the low level of switching losses, the total CSI semiconductor losses does not increase in the range $1 < n < 8$. As a consequence, $R_{th,j-c,max}$ presents a non-linear behavior meanly due to conduction losses, being slightly different from 30kHz to 60kHz.

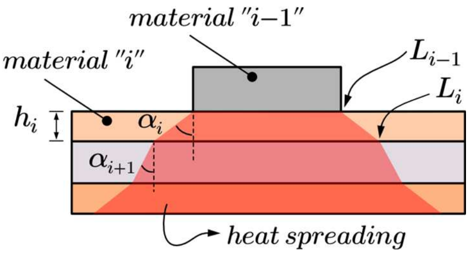


Figure 4. 14 – Heat flux path.

Once known the thermal requirement per chip, the thermal resistance of the actual module is investigated. In that regard, the heat flux path is calculated based on the heat spreading angle (α) approach [19]. Here, it is assumed that the heat dissipates homogenously with an angle α_i inside the layer "i", as far as its thermal conductivity k_i is constant. At material interfaces, α changes according to Eq. 4.3. Thus, for a given packaging geometry and material properties, the equivalent junction-to-case thermal resistance is considered as the summation of the layers' thermal resistances. Eq. 4.4 and 4.5 give the R_{th} of a layer conducting heat that is generated from a square and rectangular heat source geometries, respectively [20], [21].

$$\alpha_i = \tan^{-1}\left(\frac{k_i}{k_{i-1}}\right) \tag{4.3}$$

$$R_{th,i} = \frac{h_i}{k_i \cdot L_i \cdot L_{i-1}} \tag{4.4}$$

$$R_{th,i} = \frac{1}{2k_i(x_{i-1} - y_{i-1})\tan\alpha_i} \cdot \ln\frac{x_{i-1}(y_{i-1} + 2h_i\tan\alpha_i)}{y_{i-1}(x_{i-1} + 2h_i\tan\alpha_i)} \tag{4.5}$$

where h_i and L_i represent the thickness and the increased heat spreading source dimension in layer "i", respectively. x_i and y_i are the heat source length and width for rectangular heat sources. The increase of the heat source dimensions (L, x or y) is calculated by $\beta_i = \beta_{i-1} + 2h_i \tan\alpha_i$, with $\beta \in [L, x, y]$. It should be noted that this method does not take into account any coupling thermal resistance between the dies, i.e., the heat flux paths do not cross each other until the bottom of the baseplate.

With the aforementioned expressions and the stack-up characteristics given in Table 4.6, the equivalent junction-to-case thermal resistances can be calculated. Assuming that the heat is generated at the top of the dies (with thickness of 380µm for both diode and MOSFET) and their active areas correspond to 80% of the total chip area (estimated value – not provided in datasheet), one has $R_{th,j-c,MOS} = 0.219K/W$ and $R_{th,j-c,D} = 0.25K/W$. Comparing these results with the graph of Figure 4.13 (b), it can be concluded that a minimum number of two chips in parallel per device is required.

Now, in order to estimate the attainable gain in terms of European Efficiency when $n \geq 2$, a new set of simulations should be carried out to obtain $E_{sw}(V_{ds}, I_{dc}, n)$. In Figure 4.15 the efficiency curves are plotted as a function of the input power for $n = 2$ and $n = 3$.

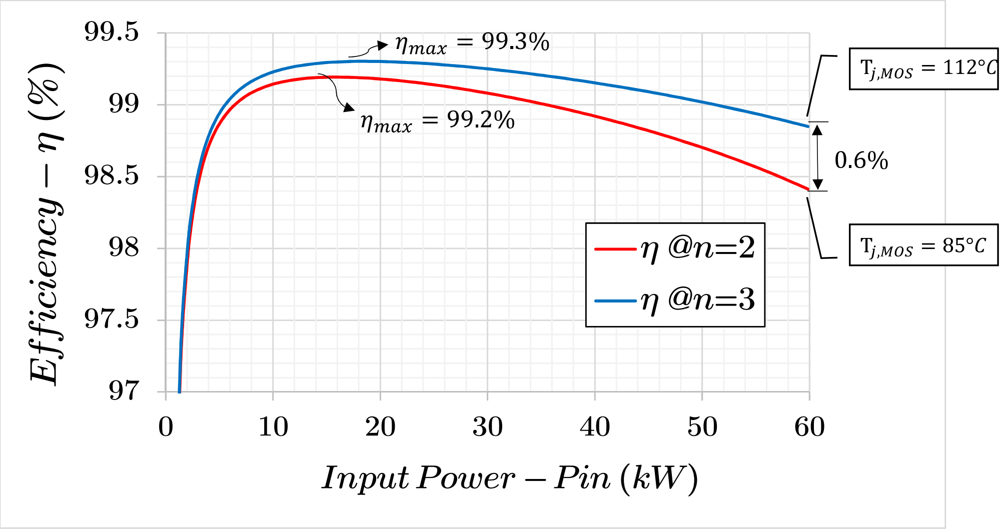


Figure 4. 15 – Efficiency curves for $n = 2$ and $n = 3$. Assumed conditions: $T_{amb} = 40°C$, $F_{sw} = 30kHz$, $R_{th,c-amb} = 0.05K/W$, $V_{grid} = 690V$ and $r_{g,on} = 2 \cdot r_{g,off} = 2.5\Omega$.

From these curves, a non-negligible difference (0.6%) in terms of efficiency at nominal power is observed. This translates into a much lower device thermal stress when $n = 3$. The peak efficiency however is slightly changed (roughly 0.1%). On the other hand, the European Efficiency calculation yields $\eta_{euro,n=2} = 98.88\%$

and $\eta_{euro,n=3} = 99.1\%$. Finally, the number of chips in parallel is set to be $n = 2$, since the estimated CSI semiconductor efficiency is considered to be good enough for the target PV application.

4.3.3 Analysis of the Packaging Thermal Resistance Sharing

With the previous heat spreading calculation method, it is possible to distinguish the contributions of different layers to the overall packaging thermal resistance. In Figure 4.16, this is shown for the diode $R_{th,j-c}$ considering two baseplate materials: Cu and AlSiC.

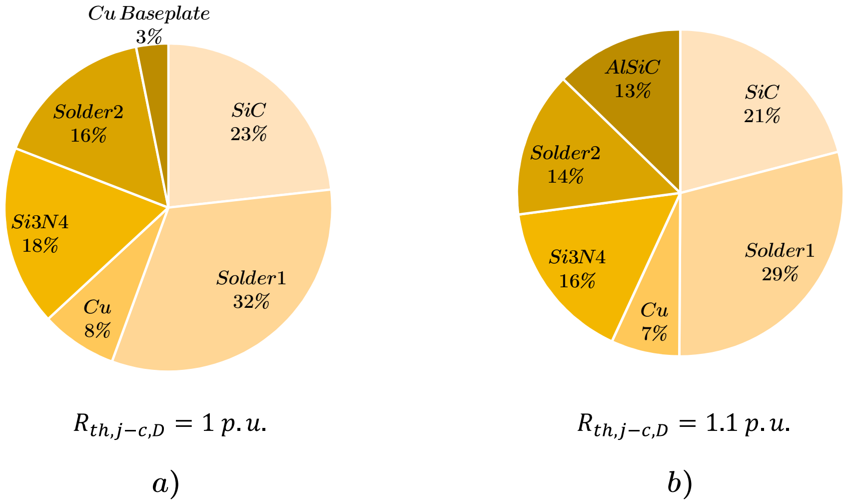
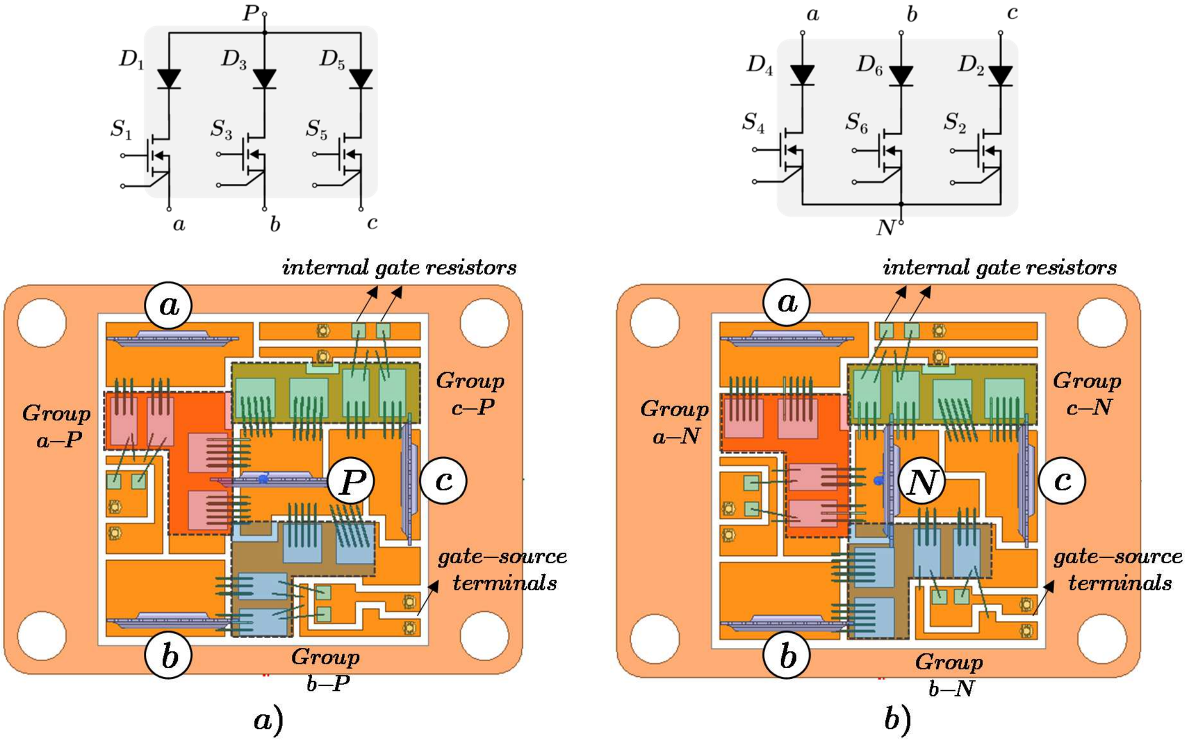


Figure 4. 16 – SiC diode junction-to-case thermal resistance sharing for two baseplate materials: a) Cu and b) AlSiC.

As can be seen, an increase of 10% in the $R_{th,j-c}$ might be observed when changing the baseplate material from Cu to AlSiC. The relatively high contribution of SiC material to the overall $R_{th,j-c}$ comes from the small active area of the devices (in this case estimated to be $80\% \cdot 6 \cdot 6\text{mm}^2$). Also, in these calculations, the SiC thermal conductivity at 100°C is taken into account and not 370W/mK (@25°C), as usually found in the literature ($k_{SiC@25°C}/k_{SiC@100°C} = 1.42$) [3].

4.3.4 Module Design

Having acquired experience with the preliminary study on substrate layout configurations, the module industrial realization is carried out. Here, the possibility of directly integrating decoupling capacitors on the module's substrate is not considered, due to reliability and robustness issues [22], [23]. To improve the substrate surface utilization while insuring balanced switching cells, the optimal layout design is found to be a hybrid solution between the conventional and "Δ" balanced configurations. Thus, after several design iterations, a final packaging layout is obtained. Figure 4.17 shows the actual high- and low-side CSI modules.



a)

b)

Figure 4. 17 – a) High-side and b) low-side modules together with their corresponding electrical configurations.

The rotational symmetry between the CSI chip groups (or legs) around the P and N points can be clearly seen. The power terminals a, b and c are symmetrically arranged as well. It is important to emphasize that both HS and LS modules share an identical substrate and housing layouts. The only difference being the placement of the bare dies, P/N terminals and wire-bonding connections. From an outside view, the LS and HS modules only differ in terms of the P/N connectors, which are shifted by 90° with respect to each other (this to avoid mounting mistakes during inverter assembly). Internal gate resistors (5Ω per MOSFET) are integrated within the module to help damp gate oscillations and equilibrate the current sharing between paralleled devices during switching transients. The module presents a footprint of 62 x 82mm and a low-profile (12mm high) with a minimum isolation voltage of 4kV. The complete module's datasheet is presented in Appendix II.

It should be noted here that in the HS module, the series connection diode–MOSFET is implemented, i.e., the diodes have a common-anode connection. For the LS module, it becomes MOSFET–diode, leading to a common-source connection of MOSFETs. If the same configuration MOSFET–diode (or diode–MOSFET) is implemented for both HS and LS modules, two distinct substrate layouts must be designed (solution to be avoided).

To evaluate the final design, the CSI switching cell stray inductances are obtained by simulation using Ansys Q3D Extractor, for an excitation frequency of 20MHz. The results are presented in Table 4.7.

Table 4. 7 – Q3D simulation results.

Switching Cell	$Cell_{a-b}$ (nH)	$Cell_{b-c}$ (nH)	$Cell_{a-c}$ (nH)
High-side Module	16.31	15.25	15.15
Low-side Module	15.72	15.19	15.26

As can be seen, all switching cells for both HS and LS modules are properly balanced, demonstrating the effectiveness of the proposed design approach.

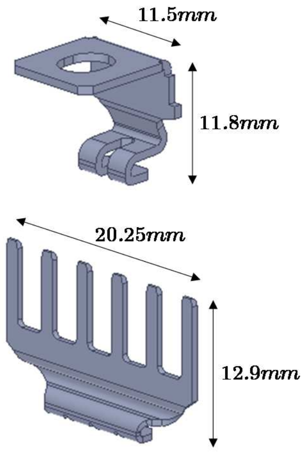


Figure 4. 18 – Screw and solderable terminals.

Due to the wide distance (>3cm) between the module's power terminals (a, b and c), their mutual inductances are nearly zero. Considering that the magnetic field around the terminals are in quadrature with that generated in the substrate, the overall switching cell stray inductance can be written as $L_{cell} = 2 \cdot L_{term} + L_{sub}$, where L_{term} and L_{sub} are the self partial inductances of power terminals and substrate, respectively. Then, when using solderable terminals (see Figure 4.18), L_{term} is evaluated to be 1.57nH, i.e., $2 \cdot L_{term} \cong 20\% \cdot L_{cell}$. On the other hand, if screw-terminals are employed, L_{cell} is increased by a factor of 28% and $2 \cdot L_{term} \cong 40\% \cdot L_{cell}$. For that reason, solderable terminals are implemented in the module. Concerning L_{sub}, its biggest contribution comes from the wire-bondings. As soon as a current "i_{ac}" propagates through the cylindrical paralleled wires – then in the z direction as well – the magnetic coupling with the substrate backside metallization is reduced, increasing the net magnetic field around the "i_{ac}" current path. Consequently, when increasing the ceramic thickness from 320µm to 635µm (typical AlN thickness), only a minor L_{sub} improvement of 1nH is perceived.

In order to investigate the DC current distribution within the module, a DC analysis is carried out. The HS module is considered here. Then, a current

$I_{dc} = 52A$ is injected from terminals a, b and c to terminal P. Figure 4.19 shows the current density analysis results.

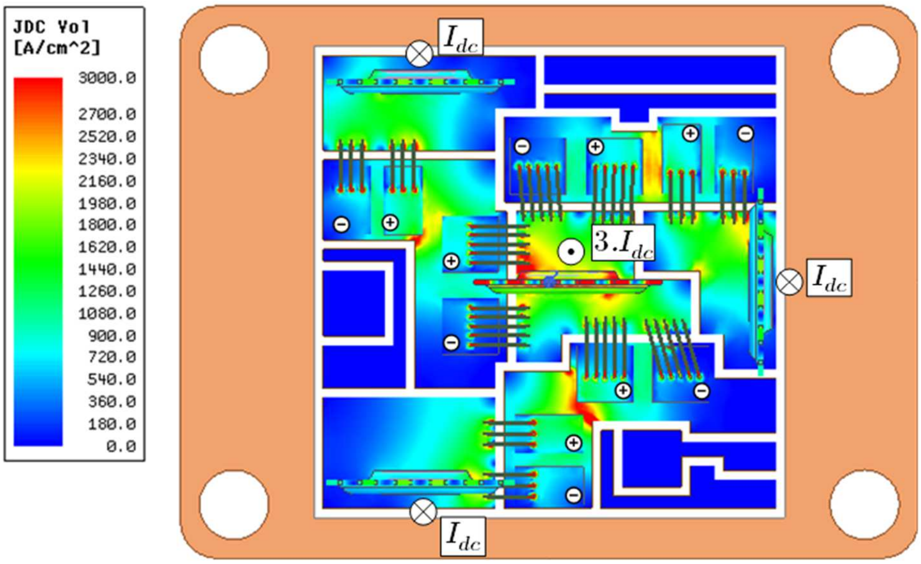
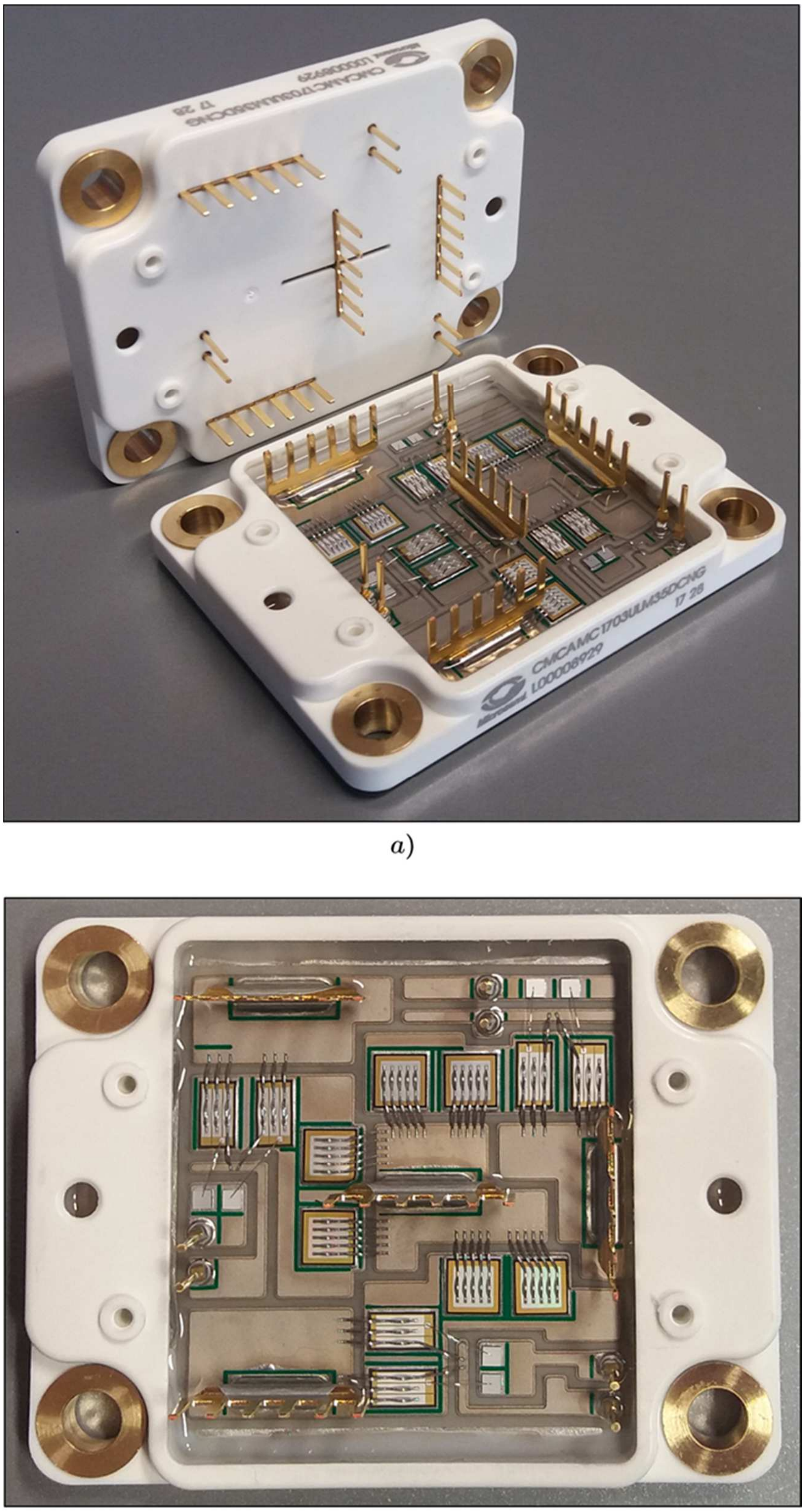


Figure 4. 19 – DC current distribution inside the HS module for $I_{dc} = 52A$. The most constrained chips are marked with a ⊕ sign.

Although the symmetric arrangement of chip groups appears to be very effective to balance switching cell stray inductances, it can be seen that the dies of a same group do not carry the same DC current. The continuous current tending to take the less resistive path (then the shortest), the chips which are closer to the P terminal see a higher current density. Nonetheless, since the SiC devices present a positive temperature coefficient, this effect tends to be counterbalanced. This subject will be further discussed through experiments in § 5.3.3.

When compared to low-inductance state-of-the-art two-level VSI modules [24], the developed CSI device seems to be a step behind. However, it is important to point out that the CSI topology features particularly low switching losses, giving a degree of freedom for the designer to reduce switching speed without significantly degrading converter efficiency. In addition, the author believes that, for this power range and considering a balanced switching cell design, the presented industrial solution has reached the limits of this packaging technology. Further improvement would be possible by 3D-packagings or directly integrating the decoupling capacitors on the module substrate.

Figure 4.20 shows the final industrial version of the CSI modules. The employed industrial design rules as well as manufacturing processes are carried out by Microsemi.



a)

b)

Figure 4. 20 – Industrial version of the CSI module – a) low-side module with and without lid and b) high-side module without lid.

4.4 Implementation of the Double-Pulse Test Characterization Method for SiC Devices Benchmarking

All semiconductor loss calculations carried out so far in this chapter consider 1.7kV SiC devices from Wolfspeed. Nonetheless, at the time of the present work, another manufacturer has made its SiC devices available. In this section, in order to evaluate and select the most suitable dies for the final CSI module, a methodology for switching characterization is implemented. For that purpose, three current measurement techniques are investigated and experimentally compared.

4.4.1 Switching Losses Measurement Methods

The switching losses characterization techniques can be basically divided into two categories: electric- and calorimetric-based methods [25]. The latter has the advantage of being more accurate, since thermal time constants are large enough to avoid fast transient measurement imprecisions. However, calorimetric methods are typically time-consuming and demand more complex measurement setups [25], [26]. Furthermore, it is unknown if the device operates within the safe operating area (SOA) boundaries. On the other hand, electrical measurement techniques represent the most commonly employed method, which are based upon voltage and current measurements (both DC and AC values) and its post-treatment data. In the literature, several types of electrical semiconductor characterization can be found [27]–[29]. In [28], an opposition method setup is proposed in order to estimate the switching losses without introducing any current sensor in the switching cell. Nevertheless, semiconductor's switching trajectory within the SOA remains unknown and the separation of conduction and switching losses becomes more challenging, since junction temperatures are not controlled. Also, the load inductor losses must be estimated and subtracted from the measured overall losses. In [29], a methodology is proposed to assess the total switching losses of devices in phase-leg configuration including the contribution of the non-active HS switch – due to transient cross-talk between HS and LS switches. For that purpose, a special measurement setup is implemented using a double-pulse test (DPT) circuit with two supplementary probes. In the CSI topology, the presence of the series diodes does not allow any short-circuit condition. For that reason, the cross-talk between MOSFETs may not lead to supplementary switching losses. Thus, when employing SBDs, switching losses are generated only within the LS switch, excluding the need for measurements in the upper switch. The authors in [27] propose a modification of the standard DPT circuit in order to be able to characterize voltage-bidirectional devices as a function of the blocking voltage.

In this work, the adopted electrical characterization method is the double-pulse test. The DPT method features the following advantages [30], [31]:

- fast measurement time, keeping the die's junction temperature under controlled conditions;
- simple test setup. Only two probes (current and voltage) are used and any steady-state measurement is required, i.e., no control loop is implemented (this is not the case for the opposition method); and
- positioning of device's switching trajectory within the SOA is known.

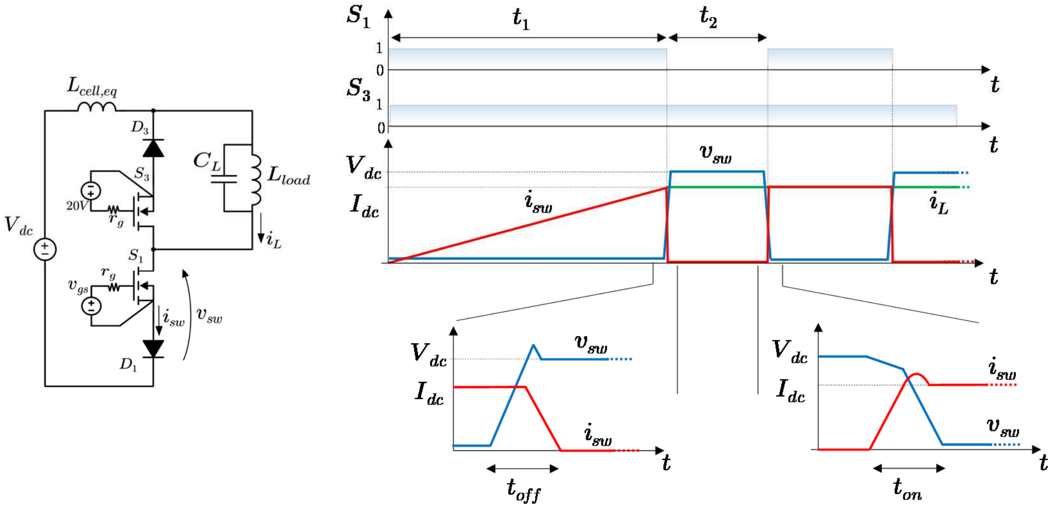
Nevertheless, when employing the DPT technique, the major obstacles to deal with are related to:

- need for wide-bandwidth (BW) current and voltage sensors;
- insertion of a current measurement sensor in the switching cell;
- misalignment between voltage and current probes; and
- underestimation of turn-on losses and overestimation of turn-off losses.

In the following, the DPT operation principle is described together with the measures to be taken to address the aforementioned drawbacks.

4.4.2 Double-Pulse Test Method

Figure 4.21 depicts the DPT circuit with voltage-bidirectional switches and the associated typical waveforms.



a) ***b)***

Figure 4. 21 – a) Double-pulse test circuit and b) typical waveforms.

For a given switching voltage, the DPT technique allows to obtain the semiconductor switching energies by transitorily applying the nominal load current to the switching cell. For that reason, devices can be fully characterized at nominal operation conditions, but with minimal power requirement. From Figure 4.21, the duration of the first pulse (t_1) is adjusted to rise the inductor current (i_L) to the desired value (I_{dc}). At the end of t_1, the LS switch is turned-off at (V_{dc}, I_{dc}) and the associated losses are computed as $E_{off} = \int_{t_{off}} i_{sw} \cdot v_{sw}\, dt$. Then, i_L freewheels through the HS switch during t_2, which must be set large enough to allow all turn-off ringing to be completely dumped. At the end of t_2, the LS switch is turned-on again, but at (V_{dc}, I_{dc}), and turn-on losses E_{on} are computed as for E_{off}. Thanks to the rapidity of measurements, the junction temperatures undergo a negligible increase and can be controlled by an external hot-plate, for example.

When prototyping, the investigated DPT test rig should be as similar as possible to the final converter design (in terms of parasitics). This becomes especially true when WBG devices are employed [3], [29]. Additionally, the load inductor parasitic capacitance (C_L), which adds to that of the HS switch, should be minimized. In this work, all tests are carried out using a single-layer air-core load inductor, with $C_L < 10pF$.

The issue of probes misalignment comes from the fact that all circuit components have their own transfer function. In this way, the response for a given input signal might be different from one component to another. Also, reflection phenomena are seen in high-frequency signals, causing unwanted distortions and delays. In order to eliminate the relative delay (also known as skew) between voltage and current probes, some methods are proposed in the literature [29]. In this work, the probes' relative delay is compensated (or deskewed) using a non-inductive SMD resistor (r). This is achieved with the help of an external circuit, which is composed of a low-voltage MOSFET that switches under resistive load (the SMD device) conditions. The resistor value should be high enough to yield $r \gg \omega l_r$. The switching losses sensitiveness to probes' skew will be further discussed through experiments in § 4.5.3.

As discussed in § 3.4, the fact of measuring the external MOSFET drain current leads to a misevaluation of turn-on and turn-off losses. Nevertheless, when operating in hard-switching condition, as it is the case in CSIs, loss calculations are carried out with $E_{total} = E_{on} + E_{off}$. Hence, after an entire switching period, the underestimation of E_{on} is compensated by the overestimation of E_{off}. Consequently, the overall estimation of losses holds true.

Concerning the wide-bandwidth voltage probe requirement, it may be accomplished by measuring the voltage across the device under test (DUT) with a passive voltage probe. The utilization of active probes should be avoided, due to their reduced BW. Additionally, ground loop paths at the probe's terminals should be minimized (e.g., by using BNC connectors) [32]. With regard to current sensor requirements, these are much more complex, since wide-bandwidth current sensor techniques tend to be intrusive, adding a large amount of stray inductance in the switching cell. For that reason, the next section is dedicated to this topic.

It is important to emphasize that in a measurement system, the oscilloscope's BW is also a critical parameter, which should be compatible with the signal to be measured [32]. When employing oscilloscopes with high-impedance inputs (e.g., 1MΩ), 50Ω feed-through BNC terminators should be used to avoid reflection phenomena within the measurement coaxial cables.

4.4.3 Current Measurement Techniques

When using the DPT method for switching losses characterization, the DUT switching current must be measured as accurately as possible. Considering the high-speed switching behavior of WBG devices, the high-frequency aspects of sensors should be carefully investigated. As discussed in [8], for wideband systems, the rise and fall times ($t_{r,f}$) of a signal are closely related with its BW by the following relation $BW = \delta / t_{r,f}$, $\delta \epsilon [0.35, 0.45]$, where δ denotes a factor depending on the time-domain response overshoot ($\delta = 0.45$ for a signal with an overshoot of 10%). Thus, for a switching current rise time of 20ns (assuming $\delta = 0.45$) the equivalent signal bandwidth is 22.5MHz. In order to properly measure this impulsive current without any significant high-frequency attenuation, the current sensor BW of $22.5 \cdot 10 = 225MHz\ @3dB$, at least, would be required.

During characterization, the current sensor should not influence the DUT switching behavior. For this reason non-intrusive sensors are preferable, as Hall-effect probe and Rogowski coil. However, these sensors do not fulfill the minimum BW specifications [29], [33]. Hence, intrusive wideband methods must be employed and a rigorous analysis of parasitics insertion should be done. In this work, three wideband state-of-the-art current measurement techniques are investigated, namely coaxial shunt, double-stage current transformer (DSCT) and active shunt. Figure 4.22 depicts the considered current sensors.

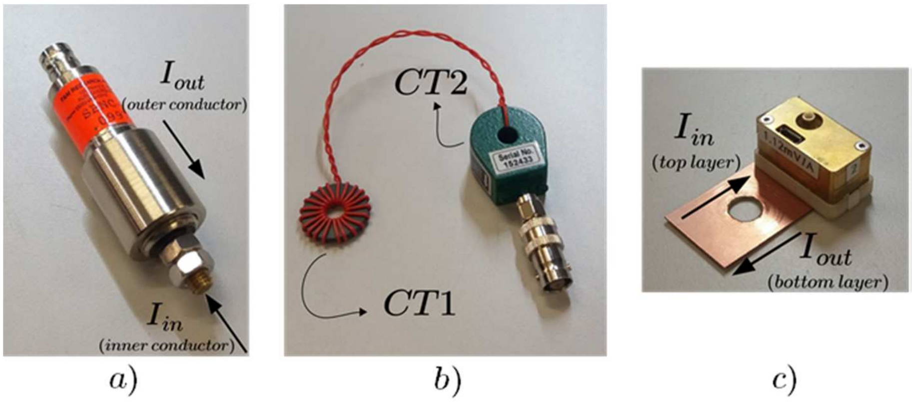


Figure 4. 22 – a) Coaxial shunt, b) Double-stage current transformer and c) Active shunt.

a) Coaxial shunt

The coaxial shunt (see Figure 4.22 (a)) is a low-inductive measuring resistor. The voltage drop across it (V_{mes}) represents then an image of the current to be measured (I_{mes}). Its low-inductive characteristic arises from the coaxial construction of the device, which ideally allows the cancelation of the magnetic field in its interior [8]. Thus, a purely resistive element can be obtained. However, the magnetic coupling between the inner and outer conductors not being perfect (k_l and $k_L < 1$, see Figure 4.23 (a)), some parasitic inductance arises. Figure 4.23 (a) shows the coaxial shunt equivalent electrical model.

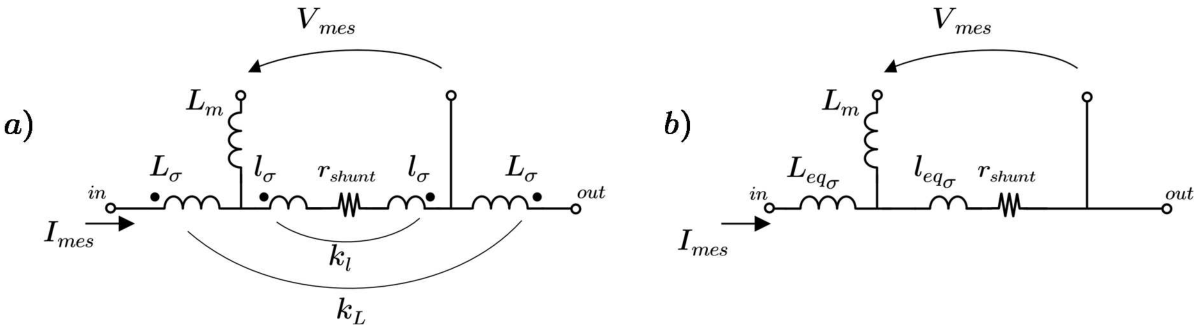


Figure 4. 23 – a) Coaxial shunt equivalent model and b) simplified model.

In the previous model, L_σ, l_σ, L_m and r_{shunt} represent, respectively, the inner/outer conductor's self-inductance, the associated sense resistor inductance, the BNC connector self-inductance and the sense resistor element itself. As can be seen, the identification of all parasitic elements represents a difficult task, mainly concerning the value of l_σ and the magnetic coupling between the coaxial conductors (dictated by the device's internal geometry). For this reason, a simplified model (seen from the in–out points) is proposed (see Figure 4.23 (b)). In this case, the total insertion inductance (L_{ins}) is given by $L_{ins} = L_{eq,\sigma} + l_{eq,\sigma}$. In this work, a coaxial shunt with the following characteristics is used: $r_{shunt} =$

$99.7m\Omega$ and $BW = 1.2GHz$. Using a high-precision impedance analyzer (the same as described earlier in this chapter), the coaxial shunt insertion inductance is assessed to be $L_{ins} = 4.2nH$ (with 1 to 10% accuracy). Nevertheless, the contributions of L_{eq_σ} and l_{eq_σ} remains unknown.

Another drawback concerning the utilization of coaxial shunt is related to its non-isolated characteristic. In fact, when measuring the DUT's v_{sw} and i_{sw} (through V_{mes}), ground bounce phenomenon is likely to happen [34], since the v_{sw} and V_{mes} probe ground points cannot be the same.

b) Double-stage current transformer (DSCT)

The second current measurement technique evaluated is the Current Transformer (CT). Several models of these current sensors are available on the market [35]. The main CTs drawbacks are related to their bulky size and low current saturation levels (especially for high-frequency models). In order to overcome these disadvantages, a second CT stage (CT1 in Figure 4.22 (b)) is added in the measurement setup, as shown in Figure 4.25. This additional CT is made with a 4F1 high-frequency ferrite core (NiZn material) and it is only 2mm thick. In doing so, the flat CT introduces a minimum amount of stray inductance in the switching cell (stray inductance which is also introduced by the spacers between the module and the PCB, as discussed in [36]). The flat 4F1 ferrite core is machined from a bigger "E" core, allowing it to assume the exact form of the module's terminals, for example. The secondary of CT1 is composed of 21 turns in a single layer winding. CT2 is a Pearson Current Monitor model 2877 ($300Hz < BW < 200MHz\ @3dB$ and $t_{rise} = 2ns$) with a single turn winding in its primary side.

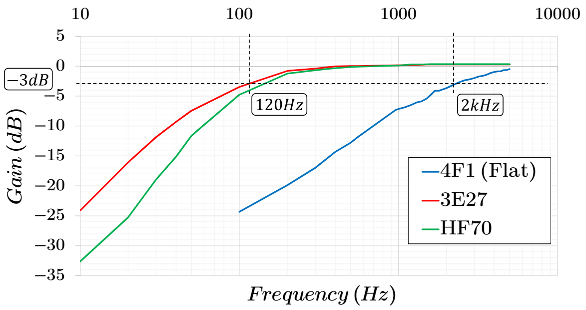


Figure 4. 24 – DSCT low-frequency response.

The frequency response of CTs were studied in [37] and [38], for the case of a single-stage current sensor. Then, parasitic elements were investigated but the presented approach remains time-consuming due to the sensor model complexity (see Figure 4.25). In this work, the current sensor BW is experimentally assessed. For this purpose, a current amplifier is built to produce a variable frequency sinusoidal signal ($I_{mes}(\omega)$). Thus, the DSCT gain is obtained by a simple output/input relationship. In Figure 4.24, the DSCT low-frequency gain is presented for three different ferrite cores: 4F1 flat core (NiZn), HF70-T18x6x10

(NiZn) and 3E27-TX22/14/6.4 (MnZn). From these results, one concludes that the DSCT with the flat core has the highest lower cutoff frequency ($f_L \cong 2kHz\ @3dB$), which might come from the magnetic core volume reduction, since the magnetizing inductance is also decreased [37], [38]. Nevertheless, it does not represent an inconvenient for the DPT implementation, since the higher cutoff frequency is critical. The DSCT high-frequency gain is discussed later on in the section.

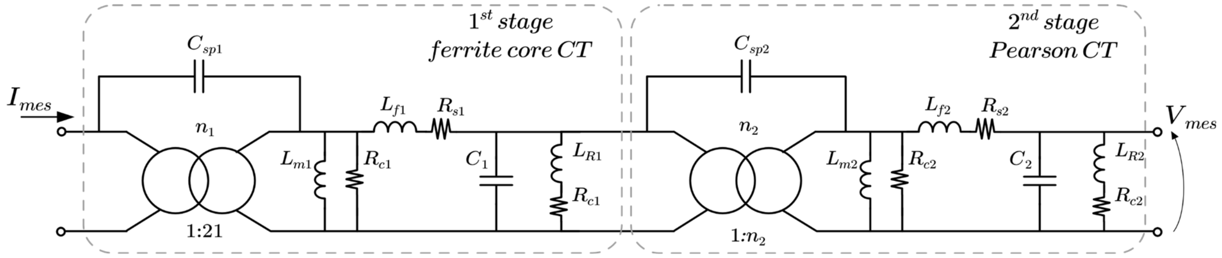


Figure 4. 25 – Double-stage current transformer model with its parasitic elements, where C_{sp}, L_m, R_c, L_f, R_s, C, L_R and R_c denote, respectively, the interwinding capacitance, magnetizing inductance, core parallel equivalent resistance, leakage inductance, secondary winding resistance, secondary winding capacitance, sense resistor inductance and sense resistance.

Concerning the DSCT insertion inductance (L_{ins}), it is assessed for the three different cores. The results are as follows: $L_{ins,4F1-flat} = 0.45nH$, $L_{ins,HF70} = 0.40nH$ and $L_{ins,3E27} = 1.48nH$. It is worth noting that the total insertion inductance ($L_{ins,total}$) can be obtained by summing up the above mentioned L_{ins} and the stray inductance added by the spacers between the module and the PCB, i.e., $L_{ins,total} = L_{ins} + L_{spacer}$. Since L_{ins} represents a very low value, efforts should be concentrated to minimize L_{spacer}, which justifies the need for a flat current transformer.

c) Active shunt

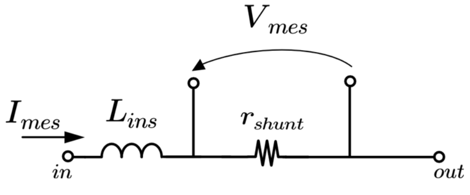


Figure 4. 26 – Active shunt equivalent model.

The third current measurement technique analyzed herein is the active shunt, depicted in Figure 4.22 (c). This current sensor is based on the Rogowski coil principle [8] and it has the following characteristics: $70kHz < BW < 400MHz$ and sensitivity of 1.12mV/A. Its simplified equivalent electric model is presented in Figure 4.26. Its insertion inductance is measured to be $L_{ins} = 1.4nH$.

Due to the complexity involved in making a high-frequency oscillator (several hundreds of MHz) with a high enough output current capability, the high-frequency behavior of the presented current sensors are analyzed under real switching conditions. For this purpose, a DPT circuit prototype adapted to 1.7kV/225A SiC MOSFET modules (CAS300M17BM2, from Wolfspeed) is built (cf. Figure 4.27).

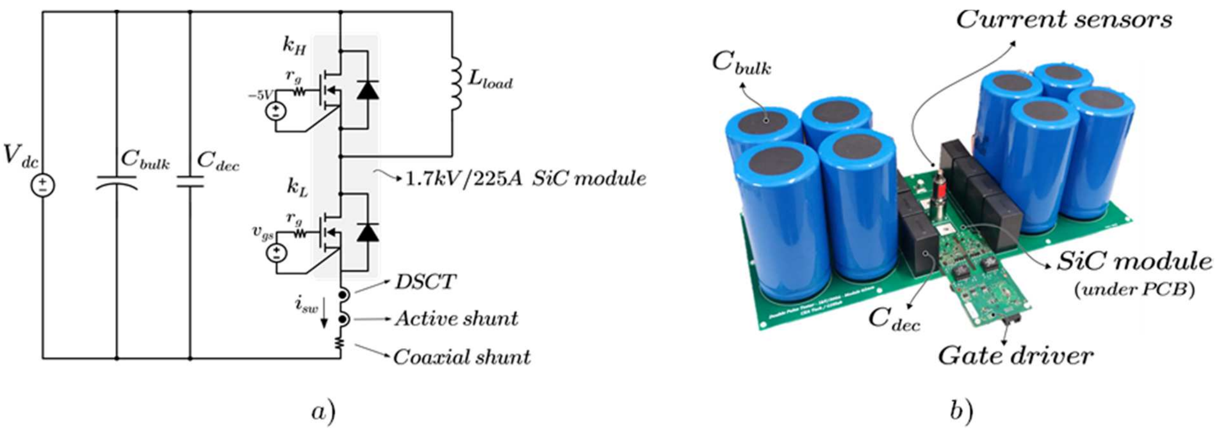


Figure 4. 27 – a) DPT circuit and b) 1.7kV/225A SiC-based DPT prototype, where all current sensors are simultaneously tested.

During the tests, all current sensors are simultaneously introduced in the switching cell for straightforward comparison. Figure 4.28 presents the current waveforms at 800V/250A turn-on transient.

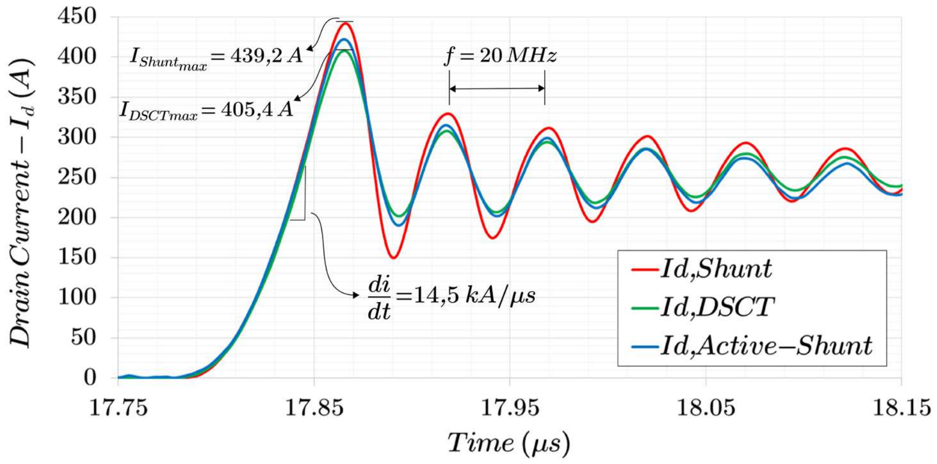


Figure 4. 28 – Turn-on current transient waveforms for the three assessed current sensors.

From these waveforms, it can be seen that both DSCT and Active shunt show a similar behavior – no signal distortion nor high attenuation levels are detected. Nevertheless, concerning the coaxial shunt response, its current overshoot and associated ringing are amplified with regard to that of the other two sensors. This might be explained by the existence of a non-negligible stray inductance in series with the sense resistor element (see $l_{eq,\sigma}$ in Figure 4.23 (b)), which could cause an overvoltage that does not represent the actual current to be measured [8]. Furthermore, a slightly deformation of the expected sinusoidal ringing is perceived in the coaxial shunt signal. A possible explanation for that could be a phase changing in the sensor transfer function around the ringing frequency (i.e., 20MHz).

Thanks to its low insertion inductance, good adaptability to the DUT's terminals and BW characteristics, the current measurement technique chosen for semiconductor characterization in this work is the DSCT.

4.4.4 Selection of SiC Devices

With the aim of choosing the most suitable semiconductors for the developed CSI module, two combinations of MOSFET and series diode – from two different manufacturers – are evaluated. The device's characteristics are given in Table 4.8 and 4.9. For that purpose, two standard SP3 modules (from Microsemi) sharing the same layout are fabricated with the devices of manufacturer 1 (Wolfspeed) and manufacturer 2. Then, a new DPT prototype is developed in order to compare their performances. In Figure 4.29 are depicted the SP3 module and the developed DPT employing the DSCT current sensor. Herein, the voltage measurements are carried out using a passive voltage probe (Lecroy PPE4kV 1:100, $BW = 400MHz$) in combination with a BNC connector and the data is acquired with a high definition oscilloscope (Lecroy Wavesurfer 3054, 4GS/s, $BW = 500MHz$).

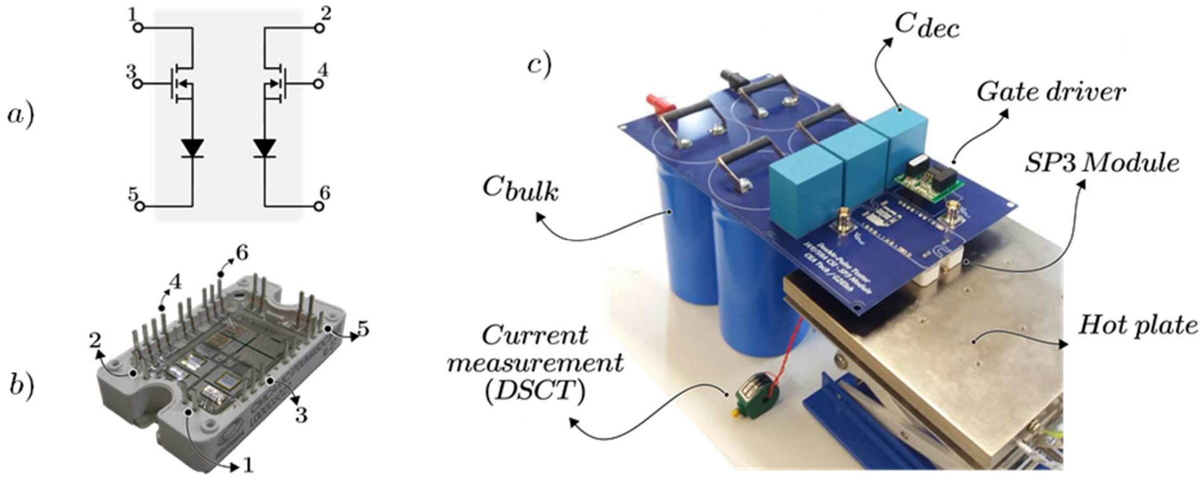


Figure 4. 29 – a) Voltage-bidirectional SP3 module pinout, b) 1.7kV SiC SP3 module and c) DPT prototype.

Table 4. 8 – Diode parameters for semiconductor manufacturers 1 and 2.

Parameter	$V_{rating}(V)$	$V_f(V)$	$C_D(pF)$
Manufacturer 1	1700	2.7 $^{1)}$	160 $^{2)}$
Manufacturer 2	1700	2.5 $^{1)}$	234 $^{3)}$

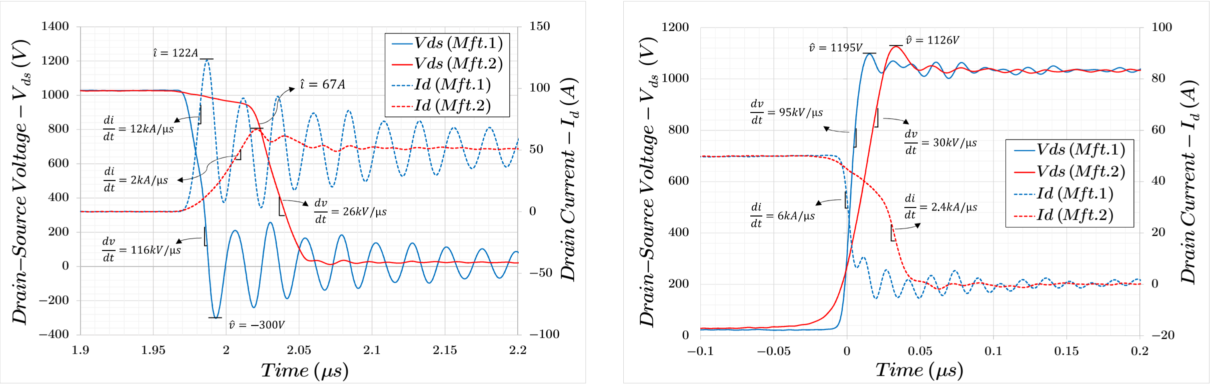
Test conditions: 1) If=50A, Tj=175°C 2) Vr=1200V, f=1MHz 3) Vr =1100V, Tj=25 ° C, f=1MHz.

Table 4. 9 – MOSFET parameters for semiconductor manufacturers 1 and 2.

Parameter	$V_{rating}(V)$	$I_d(A)$	$R_{ds,on}(m\Omega)$	$R_{g,int}(\Omega)$	$C_{iss}(pF)$	$C_{oss}(pF)$	$C_{rss}(pF)$
Manufacturer 1	1700	48 $^{1)}$	90 $^{3)}$	1.3 $^{5)}$	3672 $^{7)}$	171 $^{7)}$	6.7 $^{7)}$
Manufacturer 2	1700	58 $^{2)}$	85 $^{4)}$	14.9 $^{6)}$	3606 $^{8)}$	127 $^{8)}$	34 $^{8)}$

Test conditions: 1) Vgs=20V, Tc=100°C 2) not specified 3) Vgs=20V, Id=50A, Tj=150°C 4) Id=23A, Vgs=18V, Tj=125°C 5) f=1MHz, Vac=25mV 6) Id=23A, Vgs=18V, Tj=125°C 7) Vgs=0V, Vds=1000V, f=1MHz, Vac=25mV 8) Vgs=0V, Vds=800V, f=1MHz 9) Vds=1200V, Vgs = -5/20V, Id=50A 10) Vdd=400V, Id=23A, Vgs=18V, Rl=17.4Ω.

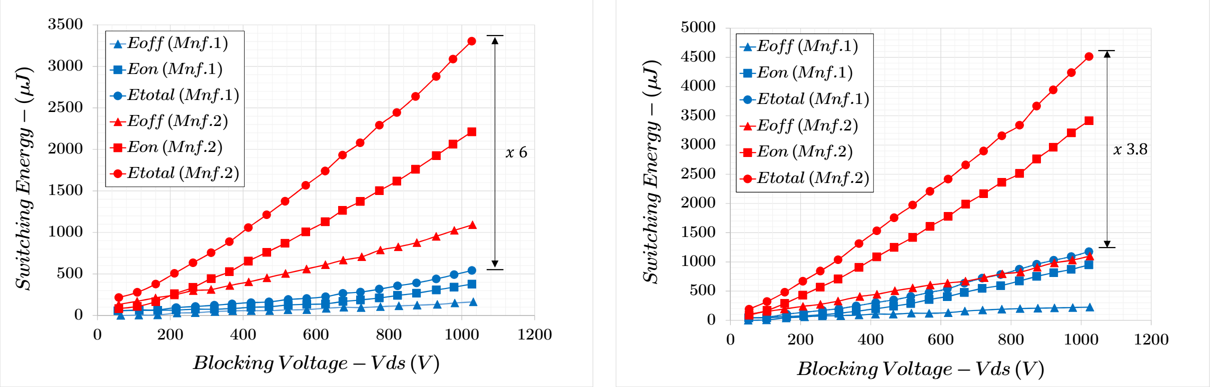
The switching waveforms at 1000V/50A for both SP3 modules are presented in Figure 4.30. From that, the faster switching behavior of dies from manufacturer 1 is clearly seen. Nevertheless, it might go along with a poorer EMI behavior due to the high current and voltage ringing amplitudes. Due to the standard design of the used SP3 modules, the DPT HS and LS switches are connected through a track on the PCB, leading to a high switching cell parasitic inductance, which in turn, increases ringing.



a) *b)*

Figure 4. 30 – Switching waveforms at a) turn-on and b) turn-off transients. Test conditions: $r_{g,on} = 2.5\Omega$, $r_{g,off} = 1.4\Omega$, $V_{driver} = +20/-5V$ and $T_j = 150°C$.

From two distinct operation conditions, the switching losses $E_{sw} = f(V_{ds})$ are calculated and presented in Figure 4.31. As expected, the semiconductor losses from manufacturer 1 are significantly lower. At $V_{ds} = 1000V$ and $r_{g,on} = 2.5\Omega$, a factor 6 exists between the total switching losses of manufacturer 1 and 2. Such a difference can be explained by two factors: firstly, the MOSFETs from manufacturer 2 present a much larger internal gate resistance ($r_{g,int}$) (cf. Table 4.8), capping the switching dynamic. Secondly, the reverse transfer capacitance (C_{rss}) of these devices are notably higher than that of manufacturer 1 – this capacitance being crucial during the Miller phase, switching losses are significantly increased as well [30].



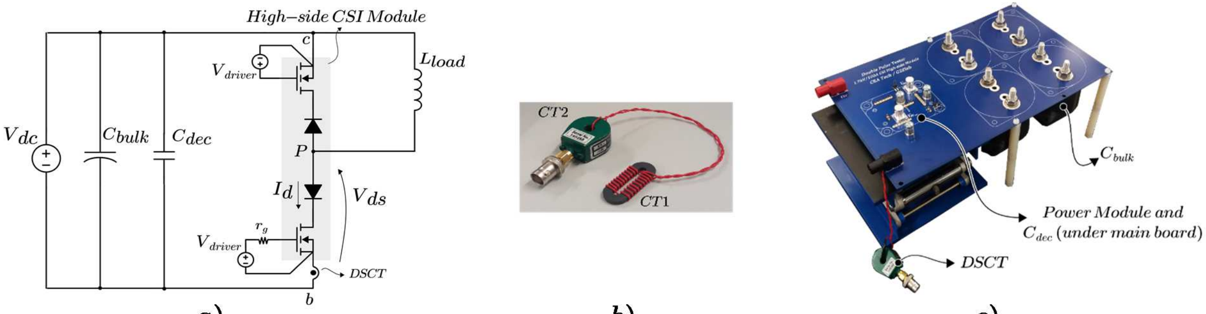
a) b)

Figure 4. 31 – Switching energies for $I_d = 50A$ and for two different conditions: a) $r_{g,on} = 2.5\Omega$ and $r_{g,off} = 1.4\Omega$, $T_j = 150^{\circ}C$ and b) $r_{g,on} = 8.5\Omega$ and $r_{g,off} = 4.4\Omega$ and T_{amb}.

Based on the previous results, the devices from Wolfspeed are selected to be integrated in the CSI module. In doing so, a supplementary design degree of freedom is obtained and the tradeoff between switching losses and EMI aspects can be carried out.

4.5 Dynamic Characterization of the Developed CSI Module

In order to characterize the developed CSI module, a DPT circuit adapted to the switching cell b–c of the high-side module is built. Figure 4.32 shows the DPT circuit and its prototype.



a) b) c)

Figure 4. 32 – a) DPT circuit, b) DSCT with modified flat core and c) DPT prototype.

To adapt the DSCT to the module's terminal, a new flat 4F1 ferrite core is fabricated in an oblong form, having 20 turns in its secondary winding (see Figure 4.32 (b)). The total DSCT insertion inductance is measured to be $L_{ins} = 1.49nH$. All switching voltage measurements are carried out using the same setup described in § 4.4.4. In order to limit switching overvoltages and reduce ringing, a dedicated decoupling board is developed (see Figure 4.33). On this separate board, six C0G ceramic capacitors 6x10nF/2000V (C3040C103JGGAC) per switching cell are placed as close as possible to the power modules. From FEA using Q3D Extractor, the overall switching cell stray inductance is assessed to be $L_{stray,total} = 17.4nH$ (@20MHz). From this, one concludes that the decoupling board is responsible for adding approximately 2nH in the original switching loop.

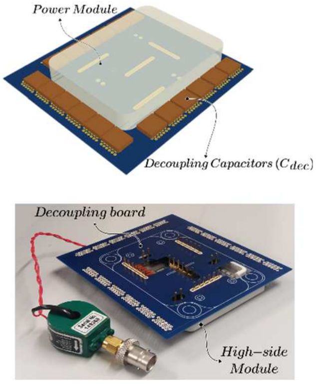


Figure 4. 33 – C_{dec} decoupling board

Fig. 4.34 shows the module switching waveforms for the most constrained case, where the switched voltage and current are $V_{ds} = 1000V$ and $I_d = 100A$, respectively.

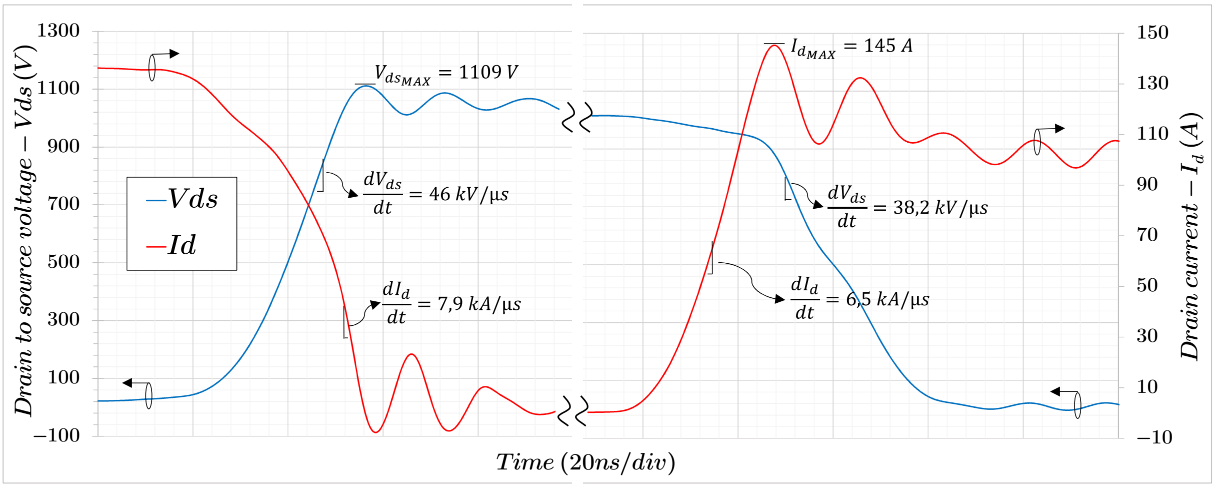


Figure 4. 34 – 1kV/100A switching waveforms at turn-off and turn-on transients. Test conditions: $r_{g,on} = 6.8\Omega$, $r_{g,off} = 4.3\Omega$, $V_{driver} = +20/-5V$ and T_{amb}.

From these waveforms, it can be seen that during turn-off transient, the semiconductors withstand 110% of the bus voltage, staying far away from their SOA limits. Furthermore, at turn-on, practically any voltage oscillation is seen. This might confirm the effectiveness of the decoupling capacitors and support the fact that the switching speed could be further increased (decreasing r_g), in order to reduce switching losses. Nonetheless, as pointed out in [39], a tradeoff must be found between increased switching speeds and EMI generation.

4.5.1 Switching Speed Characterization

To optimize the CSI operation in terms of switching losses and EMI generation, the switching speed characterization is carried out. Figure 4.35 illustrates the variation of the switching energy versus the maximum absolute dV_{ds}/dt for several external gate resistor values (r_g).

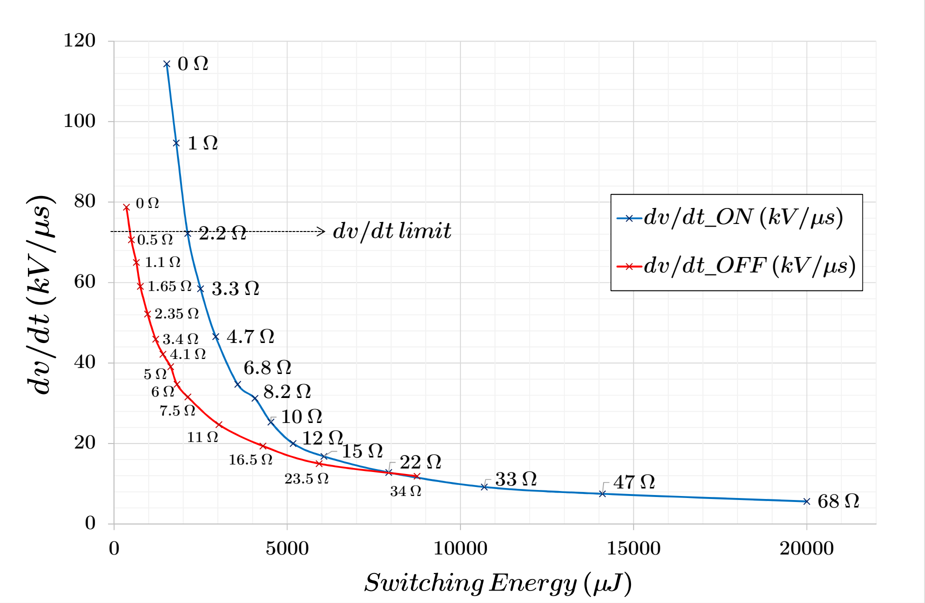


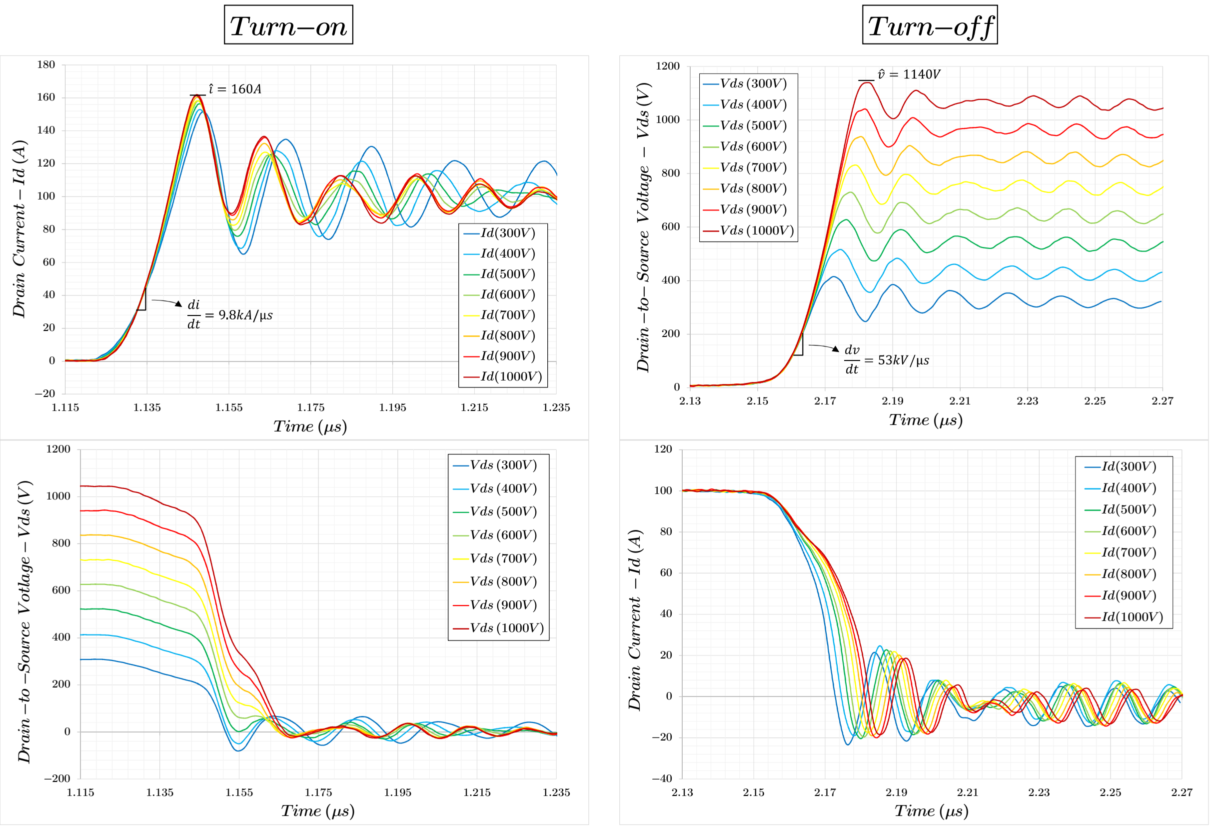
Figure 4. 35 – Switching speed characterization for 1kV/100A. In the y-axis, dv/dt represents the maximum absolute value of the blocking voltage during switching.

As shown, for values of $r_{g,on} < 2.2\Omega$, minimal changes in terms of switching losses are observed. On the other hand, dv/dt levels are strongly increased from this point. Considering a direct approximation of trapezoidal switching waveforms [40], elevated switching speeds (or dv/dt and di/dt levels) might increase the high-frequency spectral amplitude, leading to a higher EMI generation potential. Consequently, additional filtering and/or shielding efforts would be required to comply with EMC standards [39]. Another factor to be taken into account is the isolated DC-DC converters employed in gate drivers, which are commonly limited in terms of dv/dt immunity [41]. Furthermore, in order to improve the tradeoff between total switching losses ($E_{on} + E_{off}$) and high-frequency spectrum generation, the switching transition at turn-on and turn-off events should be matched [40]. From Figure 4.35, one concludes that it occurs when $r_{g,on} \cong k \cdot r_{g,off}$, with $1 < k < 4$. Taking all this into account, the optimum external gate resistor values are chosen to be $r_{g,on} = 2.2\Omega$ and $r_{g,off} = 1.1\Omega$, insuring a maximum dv/dt rate of approximately 70kV/µs.

It should be noted here that the presented switching speed characterization alone is not capable of predicting the inverter's EMI conducted emission levels [42]. Nevertheless, it still represents a reasonable approach to be implemented in an early design phase to identify and avoid less advantageous operating conditions.

4.5.2 Switching Losses Characterization

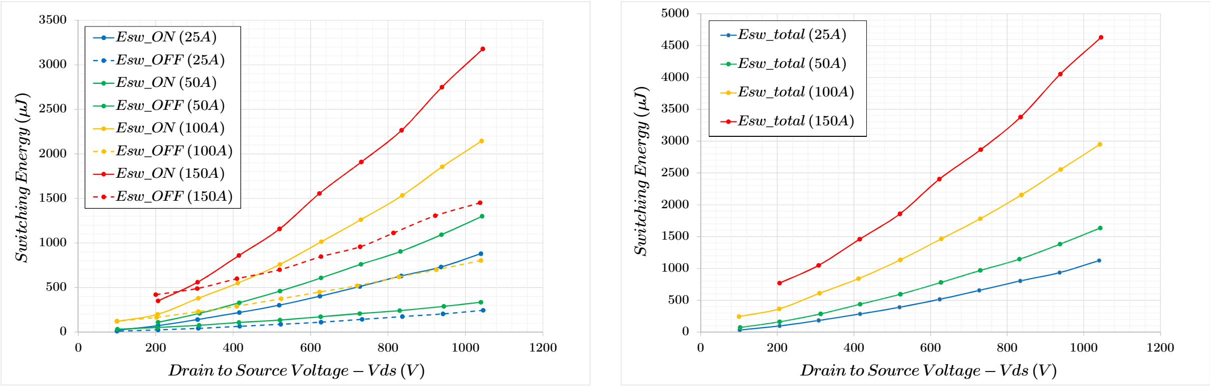
Once defined the external gate resistor values, the complete switching characterization is carried out. Figure 4.36 shows the switching currents and voltages waveforms for a constant switched current. The test conditions are as follows: $I_d = 100A$, $V_{ds} = (300{,}400, \ldots, 1k)V$, $r_{g,on} = 2.2\Omega$, $r_{g,off} = 1.1\Omega$ and T_{amb}. Figure 4.37 depicts the corresponding switching energies as a function of the blocking voltage.



a) *b)*

Figure 4. 36 – Superimposed drain-to-source voltage V_{ds} at a) turn-off and c) turn-on. Superimposed drain current I_d at b) turn-off and d) turn-on. Test conditions: $I_d = 100A$, $r_{g,on} = 2.2\Omega$, $r_{g,off} = 1.1\Omega$, $V_{driver} = +20/-5V$ and T_{amb}.

To be able to predict the converter efficiency for the entire power range, the switching characterization is carried out for other three drain current values: $I_d = (25, 50{,}150)A$. The corresponding results are presented in Figure 4.37.

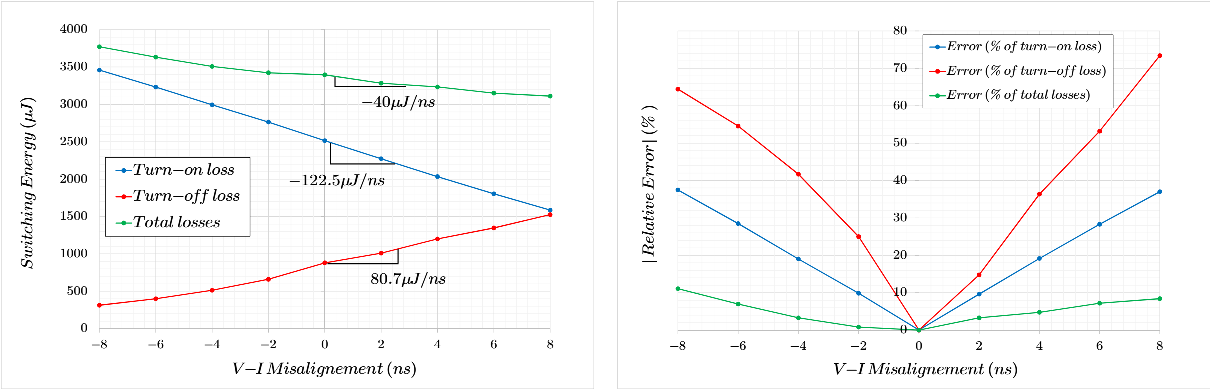


a) *b)*

Figure 4. 37 – a) Turn-on and turn-off and b) total switching energies for different switched current values. Test conditions: same as in Figure 4.36.

4.5.3 Influence of Probes' Relative Delay on Switching Losses

To evaluate the influence of voltage and current probes' relative delay on switching losses, a controlled V-I misalignment is introduced during the post-treatment of characterization data. For this purpose, the voltage and current switching waveforms at 1000V/100A, $r_{g,on} = 3\Omega$ and $r_{g,off} = 1.65\Omega$ are used as reference. Figure 4.38 presents the obtained results.



a) *b)*

Figure 4. 38 – a) Sensitivity of the switching energies to the V-I misalignment and b) the corresponding absolute values of the switching energies relative error.

From Figure 4.38 (a), it can be seen that a positive V-I misalignment implies the turn-on losses to be underestimated. Since the same delay is applied for the entire switching period, the turn-off losses are then overestimated, as expected. Knowing that turn-on losses are dominant over turn-off losses (see Figure 4.37), the overall calculated switching energy decreases as well. In Figure 4.38 (b), the absolute values of the switching energies relative error are shown. As can be seen, the calculated switching energies are very sensitive to the probes' misalignment.

A relative delay of 4ns induces an error of 36% and 20% on the turn-off and turn-on energies, respectively. Nonetheless, when considering the total switching energy $(E_{on} + E_{off})$, the equivalent error reduces to reasonable values, i.e., 4.8% at 4ns. This natural error compensation becomes less effective as soon as the difference between E_{on} and E_{off} is increased, e.g., when operating at quasi-ZVS condition.

4.5.4 SBD Switching Analysis

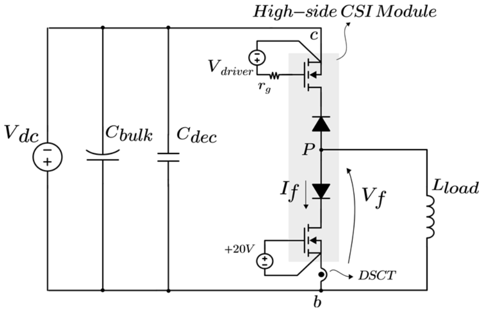
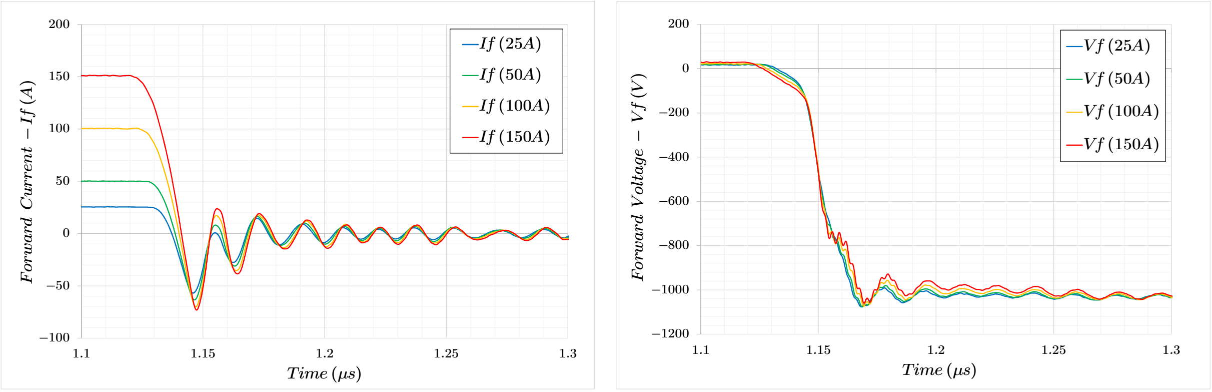


Figure 4. 39 – Modified DPT connection allowing to assess the diode switching behavior.

With the purpose of investigating the 1.7kV SiC SBD switching behavior, the DPT connection is modified as proposed in Figure 4.39. Here, the utilization of an isolated DC voltage source allows the measurement setup to be the same as before. However, the upper switch must be controlled now. The lower switch is constantly kept in on-state. Figure 4.40 presents the SBD switching waveforms at turn-off transient for different switched currents. Based on that, the SBD capacitive charge is calculated in each case. The results and summarized in Table 4.10.



a) *b)*

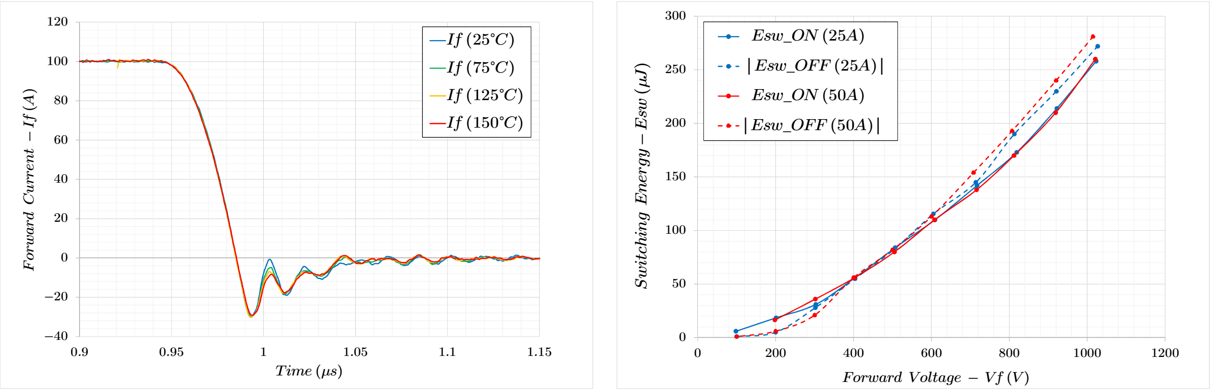
Figure 4. 40 – SBD turn-off switching waveforms for different switched currents. Test conditions: $V_f = 1000V$, $r_{g,on} = 2.2\Omega = 2 \cdot r_{g,off}$ and T_{amb}.

Table 4. 10 – Calculated SBD capacitive charge from measurement.

$I_f\ (A)$	25	50	100	150
$di/dt\ (kA/\mu s)$	7.9	9.5	12.6	14.3
$Q_c\ (nC)$	698.51	701.32	719.24	738.65

In each case, the diode's stored capacitive charge is calculated integrating I_f from the zero-crossing to 1.3μs. As can be seen, the diode's current ringing amplitude increases with the switched current and so the di/dt (see Table 4.10), which is dictated by the transconductance of the controllable switch (upper MOSFET). On the other hand, Q_c stays nearly constant, indicating no bipolar reverse-recovery behavior. This is as expected, since the switched currents are far away from the limit of activation of highly p-doped regions in the MPS structure [1]. It should be noted that in the device's datasheet $2 \cdot Q_c = 693nC\ @25^{\circ}C$, showing a good agreement with measurements. Also, this supports the employed current sensor's accuracy, mainly related to the current overshoot amplitude measurement.

Figure 4.41 (a) shows the SBD switched current waveforms for different junction temperatures. Table 4.11 summarizes the calculated Q_c in each case.



a) *b)*

Figure 4. 41 – a) 1000V/100A SBD's turn-off current waveforms for different junction temperatures at $r_{gon} = r_{goff} = 10\Omega$ and b) SBD switching energies as a function of the blocking voltage for two different switched currents at $r_{gon} = 2 \cdot r_{goff} = 2.2\Omega$ and T_{amb}.

Table 4. 11 – Calculated SBD capacitive charge from measurements in Figure 4.41 (a).

$T_j\ (^{\circ}C)$	25	75	125	150
$Q_c\ (nC)$	758.07	761.98	763.99	740.55

Again, the MPS diode operates as a purely unipolar device and no bipolar effect is seen – Q_c being constant over the entire temperature range.

In Figure 4.41 (b), the diode's turn-on and turn-off switching energies are depicted. From that, it can be concluded that the diode operates practically as an ideal capacitive element, since its overall switching energy $E_{on} + E_{off}$ adds up to zero (in the worst case, $E_{on} + E_{off} = 30\mu J$). These results also verify the validity of the probe's relative delay compensation method. Otherwise, considerable E_{on} and E_{off} estimation errors would arise, as discussed in the previous section.

4.5.5 Decoupling Capacitor Current Measurement and Sizing

As presented in § 4.5, ceramic capacitors are placed as close as possible to the power module's terminals to reduce switching cell stray inductances. In the literature, not rarely these capacitors are directly integrated within the packaging [3], [43]. On the one hand, this well-known practice is very effective in reducing ringing and voltage overshoots. On the other hand, the dimensioning of these decoupling capacitors (C_{dec}) can represent a difficult task, since the current flowing through them depends on the excitation frequency (imposed *di/dt* during MOSFET turn-on, for example) and on the values of all passive elements (parasitics or not) in the circuit (C_{dec}, C_{oss}, C_{bulk}, L_{stray} and so on). In this work, the presented DPT circuit can be used to measure the decoupling capacitor instantaneous current during switching through a two-step procedure. This can be achieved thanks to the dedicated board on which the decoupling capacitors are soldered and the adaptability of the employed DSCT current measurement technique. Firstly, for a given switched current and voltage values (I_d, V_{ds}), the current through the switching cell I_{mes1} is assessed (see Figure 4.42 (a)). Then, the DPT is disassembled and the DSCT is placed between C_{bulk} and C_{dec}, as depicted in Figure 4.42 (b). After soldering the module's terminals on the mainboard again, the current measurement I_{mes2} is taken for (I_d, V_{ds}). Hence, the decoupling capacitor current is obtained with $I_{C_{dec}} = I_{mes2} - I_{mes1}$. In Figure 4.43 (a) are depicted the relevant turn-off waveforms at $I_d = 50A$ and $V_{ds} = 600V$.

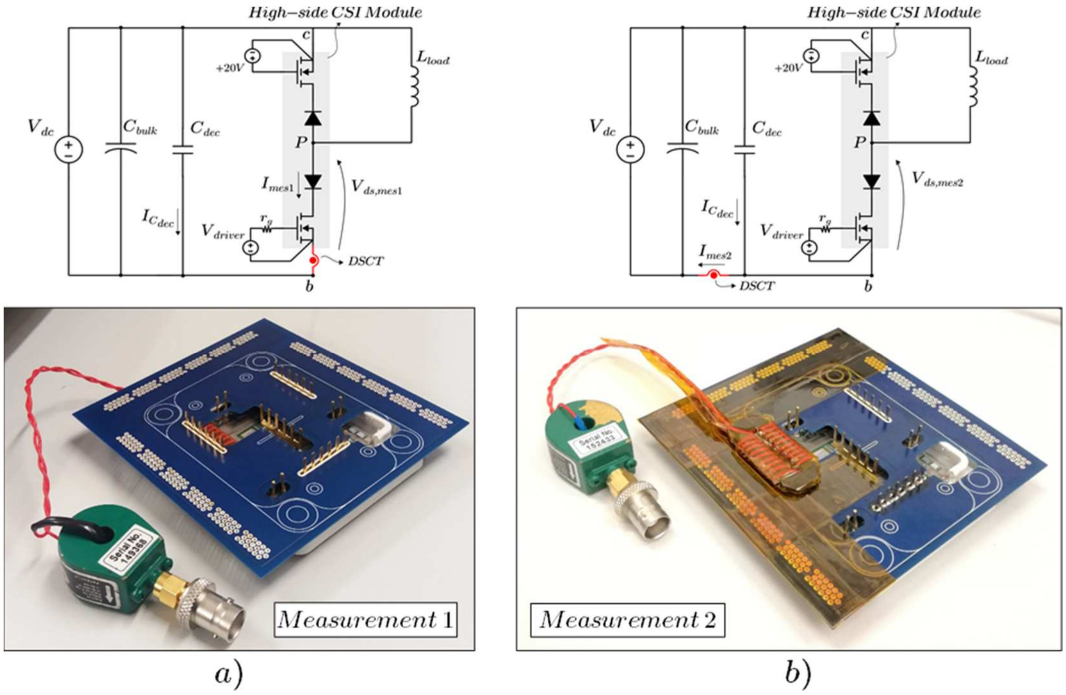


Figure 4. 42 – Measurement setups for the decoupling capacitor current evaluation.

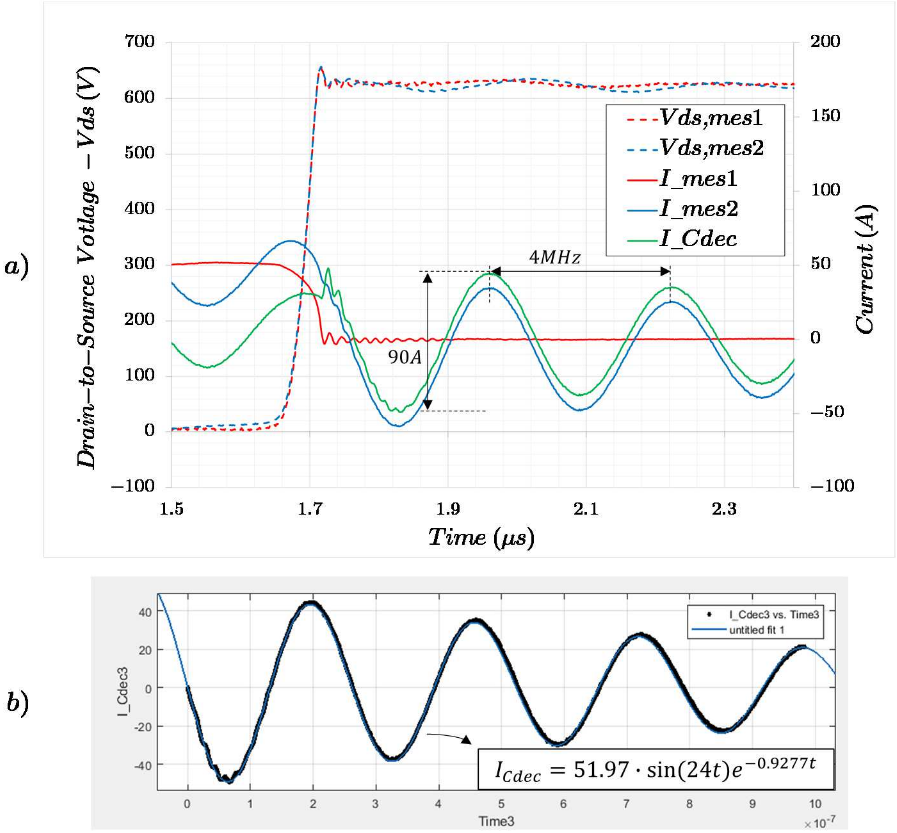


Figure 4. 43 – a) Switching waveforms at $I_d = 50A$, $V_{ds} = 600V$ and $r_{g,on} = r_{g,off} = 10\Omega$ and b) C_{dec} current fitting equation.

As one can see, the switching characteristics in V_{ds} waveforms are not changed from measurement 1 to measurement 2. This proves that switching cell (and so its parasitics) has not been changed between the PCB disassembling –

assembling soldering process. Concerning the current measurements, the effects of resonance in C_{dec} current can be clearly seen. During commutation, C_{dec} must provide not only the high impulsive current (usually associated with C_{oss} charge/discharge process) but also all the resonance oscillations with the mainboard reactive elements (C_{bulk} and parasitic inductances). Consequently, a high-amplitude (90A peak-to-peak) current at 4MHz appears as the main component of $I_{C_{dec}}$. With the aim of calculating the RMS value of $I_{C_{dec}}$, a curve fitting is employed to find $I_{C_{dec}}(t)$ (see Figure 4.43 (b)). Thus, $I_{rms,C_{dec}}$ can be calculated as follows:

$$I_{rms,C_{dec}} = \sqrt{2F_{sw} \int_0^{\frac{1}{2F_{sw}}} I_{C_{dec}}^2(t)dt} \tag{4.6}$$

Figure 4.44 shows the evolution of $I_{rms,C_{dec}}$ as a function of the switching frequency. In this calculation, the following assumptions are made: *i)* the same function $I_{C_{dec}}(t)$ is taken into account for both turn-on and turn-off transitions and *ii)* $I_{C_{dec}}(t)$ is assumed to be completely dumped at the end of $1/F_{sw} \cdot 2$.

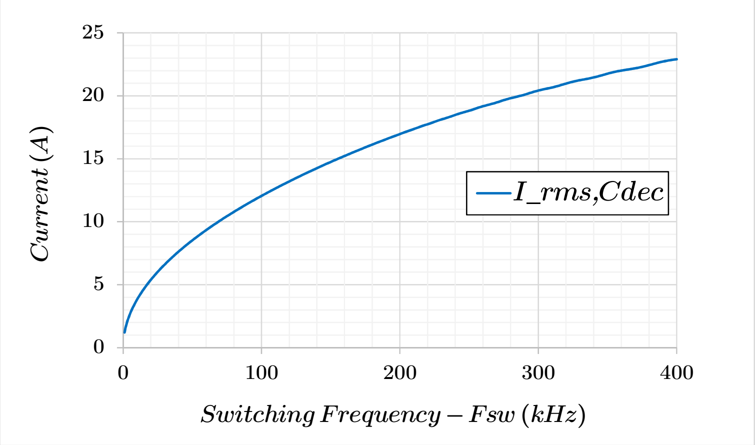


Figure 4. 44 – Decoupling capacitor RMS current as a function of the switching frequency.

From the previous graph and taking as reference the ceramic capacitor C3040C103JGGAC of § 4.5, whose ESR is measured to be 16.3mΩ @4MHz, the average losses at 200kHz equals to 4.7W. In this work, six ceramic capacitors are paralleled, leading to 0.8W of dissipation per device. Hence, one concludes that even with high current amplitudes (90A peak-to-peak) seen in $I_{C_{dec}}$, its fast dumping behavior helps to keep its RMS value (and then losses) within a reasonable range.

As shown in this section, the main contribution for the RMS current of decoupling capacitors does not come from the charge/discharge C_{oss} process, as often considered [3]. Furthermore, it should be noted that other low frequency components (at F_{sw} and its multiples, for example) could be seen in $I_{C_{dec}}$ during nominal inverter operation at F_{sw}, which cannot be verified with the DPT circuit.

4.6 Summary and Conclusion

This chapter discussed the design and characterization of a novel SiC power module dedicated to CSI applications. From a preliminary study using FR4-based insulated substrates, several semiconductor die arrangements have been investigated. As a result, balanced switching cells – in terms of parasitics – were obtained. This introductory study served as a basis for the CSI module realization in its industrial version. Then, a step by step procedure was given, covering the packaging material selection, thermal resistance calculations, substrate and housing layout design, choice of module's terminals and semiconductor dies. Although this work studied in detail the module's parasitic inductances, the packaging Common Mode (CM) parasitics have not been investigated. Especially the CM capacitors between points P and N to the ground. As seen in § 4.5.1, the developed module is capable of achieving high *dv/dt* rates (>100kV/µs). Hence, further research is required to quantify and evaluate the advantages and drawbacks of going up to such high switching speeds.

In the literature, SiC-based power modules employing standard soldering alloys and materials are associated to have reduced cycling capability [44], [45]. Due to the high SiC stiffness, some studies indicate, for a given packaging technology, that the SiC-based module lifetime is reduced to 1/3 of its equivalent Si-based module [45]. For a future industrial utilization of the developed CSI module, this aspect should be investigated in combination with the specific CSI thermal constraints found in the target application.

As discussed in § 4.3.4, for the power range of this work and considering a balanced switching cell design, the presented industrial solution seems to have reached the limits of the employed packaging technology. Hence, a possible research field to improve the existent module would be related to 3D-packaging. Having the possibility to make interconnections in the z-direction, a balanced design might be more easily achieved, bonding wires could be avoided and thermal resistances improved.

Concerning the current sensor bandwidth characterization, several attempts have been made during this work, but without success. A test bench allowing to excite the current sensors with several amps at hundreds of MHz would make possible to easily determine the sensors' transfer functions. Hence, the DSCT design could be fine-tuned and the influence of each design parameter (e.g., number of turns, core material and etc) on the sensor gain/phase could be experimentally obtained.

4.7 References

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Chapter 5

Design and Experimental Evaluation of the 60kW CSI Prototype

With the aim of experimentally validating the Current Source Inverter (CSI) operation at nominal power, a prototype employing the developed 1.7kV SiC modules is presented in this chapter. For that purpose, the main design guidelines for passive elements and cooling system are discussed. Especial attention is given to the module's thermal aspects, which are studied through DC current tests. From that, an electro-thermal model is developed, allowing to precisely estimate the generated power losses per semiconductor chip. The mechanisms of semiconductor thermal runaway are also investigated. Based on the power module dynamic characterization results, efficiency calculations are carried out in this chapter. Moreover, the CSI is compared with a standard two-stage voltage-source based solution. Concerning the inverter experimental evaluation, the complete hardware description is given, including the setup for direct measurement of junction temperatures. Finally, the developed 60kW CSI is characterized using both electrical and calorimetric methods. Thanks to the employed characterization methodology, switching and conduction losses are dissociated.

5.1 Introduction

In Chapter 4, the CSI power module design and its dynamic characterization have been fully described. Now, the present chapter aims to study the operation of the developed SiC module under nominal switching conditions. For this reason, a 60kW CSI prototype is presented together with its main design guidelines. To investigate the module's thermal behavior, preliminary DC current tests are carried out, revealing a certain thermal asymmetry between the semiconductor chips of a same power module. As will be seen, the existence of non-negligible mutual thermal resistances and current unbalance between the dies are the root cause of this issue. From these experiments, the cooling system is validated and a thermal model is developed, allowing to precisely predict the power losses generated per chip.

Regarding the CSI operation at nominal power, the prototype is evaluated using a three-phase resistive load under open-loop condition. The test setup is built in such a way that the inverter efficiency can be assessed for different switching frequencies, but at constant DC current ripple. In doing so, the low impact of switching losses on inverter efficiency is experimentally validated. Once defined a fixed switching frequency (60kHz), the CSI efficiency is investigated for two distinct DC voltages (665V and 755V) along the entire inverter power range.

As pointed out in [1], the accurate measurement of losses in a power converter system becomes very challenging as soon as its efficiency approaches unity. Hence, to keep the measurement uncertainty within reasonable boundaries, the power losses should be assessed directly. In Chapter 5, this is accomplished through a calorimetric method, where the semiconductor losses are measured separately from the overall inverter losses. Additionally, the CSI power modules are equipped with temperature sensors, which allow to directly measure the dies' junction temperatures under nominal switching operation. Thanks to that, switching and conduction losses are independently evaluated.

5.2 Sizing of Passive Components

5.2.1 DC Inductor

The DC-link inductance (L_{dc}) is usually defined to insure Continuous Conduction Mode (CCM) while limiting the DC current ripple to a certain value ($\Delta I_{dc,max}$) [2]. With regard to its implementation, the use of two DC-chokes (split between points P and N, see Figure 3.1) is preferred, since it creates symmetric common-mode (CM) paths to the ground. For a given modulation strategy, the value of L_{dc} is obtained by its volt-second principle in steady-state condition. Considering, for example, one switching period located in Sector I, one obtains

$$\Delta I_{dc} = \frac{1}{2T_{sw}L_{dc}} \int_{0}^{T_{sw}} ([V_{dc} - (V_{an} - V_{bn})] \cdot T_i + [V_{dc} - (V_{an} - V_{cn})] \cdot T_{i+1} + V_{dc} \cdot T_z)\, dt \qquad (5.1)$$

Note that the previous expression holds true for any tri-state modulation strategy, i.e., $T_i - T_{i+1} - T_z$, independently of the space vectors application order. During the zero vector application time, L_{dc} can be expressed as follows:

$$L_{dc} = \frac{V_{dc} \cdot T_z \cdot T_{sw}}{2 \cdot \Delta I_{dc}} \qquad (5.2)$$

Applying Eq. 5.1 at the sector boundaries, where T_z is maximized (and so the current ripple), yields $T_z/T_{sw} = \left(\hat{V}_{f,l-l} - V_{dc}\right)/\hat{V}_{f,l-l}$. Assuming now a minimum PV power ($P_{PV,min}$), where the inverter shall start operating, the maximum DC current ripple is obtained with $\mathit{\Delta} I_{dc,max} = 2 \cdot P_{PV,min}/V_{dc}$. Finally, a minimum inductance value $L_{dc,min}$ to insure CCM operation is given by

$$L_{dc,min} = \frac{V_{dc}^2 \cdot \left(\hat{V}_{f,l-l} - V_{dc}\right)}{2 \cdot F_{sw} \cdot P_{PV,min} \cdot \hat{V}_{f,l-l}} = \frac{V_{dc} \cdot \left(1 - \frac{M\sqrt{3}}{2}\right)}{2 \cdot F_{sw} \cdot \mathit{\Delta} I_{dc,max}} \qquad (5.3)$$

Since the DC voltage can assume any value within the range $0 < V_{dc} < V_{oc}$, Eq. 5.3 should be maximized with regard to V_{dc}. Eq. 5.4 presents $L'_{dc,min}$ which insures CCM operation for any value of V_{dc}.

$$L'_{dc,min} = \frac{4 \cdot \left(V_{f,l-l}\right)^2}{27 \cdot F_{sw} \cdot P_{PV,min}} \qquad (5.4)$$

Figure 5.1 depicts $L'_{dc,min}$ as a function of the switching frequency considering $V_{f,l-l} = 690V$, and $P_{PV,min} = 5\% \cdot 60kW$.

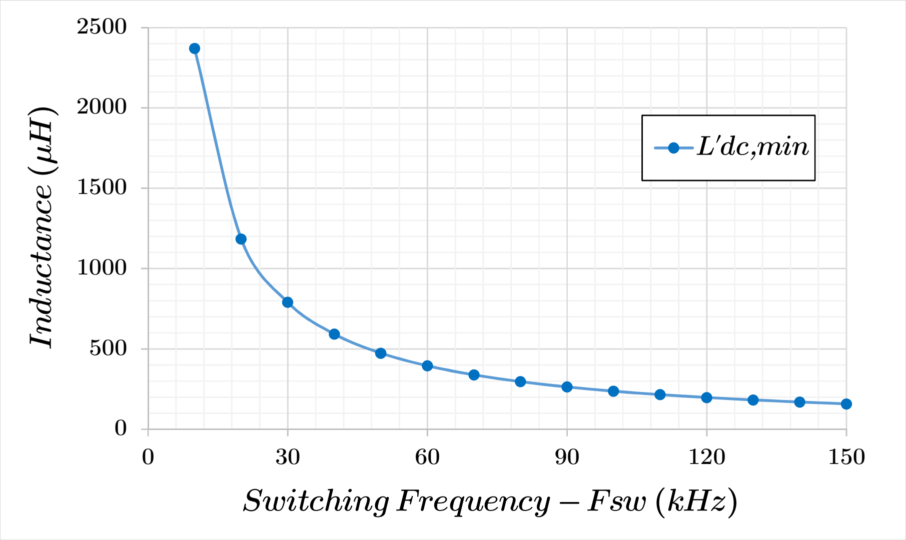


Figure 5. 1 – Minimum value of $L'_{dc,min}$ as a function of the switching frequency.

From Eq. 5.4, it becomes clear the degrees of freedom the designer has to minimize the value of the DC inductance. At first sight, efforts should be concentrated to reduce the value of the squared term $V_{f,l-l}$. However, as will be further discussed in § 5.4.1, reducing the grid voltage level directly penalizes the CSI cost-effectiveness from a semiconductor point of view. Another possible solution is to increase the minimum PV power for inverter startup. This, again, represents a drawback, since the inverter might not be able to operate at low solar irradiance levels. The third possibility and the most straightforward one is to simply increase the switching frequency (as shown in Figure 5.1). Nevertheless, it becomes less effective for $F_{sw} > 75kHz$ and a tradeoff between efficiency and power density (then costs) must be found.

An alternative way to reduce the value of L_{dc} is to operate the inverter in Discontinuous Conduction Mode (DCM) [3]. Considering a PV application, the CSI could operate in CCM at nominal power and switch to DCM, with an appropriate control strategy, in the case of low solar irradiance levels.

5.2.2 DC Capacitor

Ideally, all the I_{dc} current ripple should flow through the DC filter capacitor C_{dc}. This, in order to insure a fixed PV string voltage (V_{dc}) and allow the MPP to be tracked without oscillating around the (V_{MPP}, I_{MPP}) point. In practice, an admissible DC voltage ripple is assumed, e.g., 1% of V_{dc}. The minimum value of C_{dc} is given by Eq. 5.5 [4]. To avoid resonances with CSI generated high-frequency harmonics, the DC filter (L_{dc} and C_{dc}) resonance frequency should be well below F_{sw}, i.e., $F_{sw} \geq 10/(2\pi\sqrt{L_{dc} \cdot C_{dc}})$.

$$C_{dc,min} = \frac{\Delta I_{dc,max}}{8 \cdot \Delta V_{dc} \cdot F_{sw}} \tag{5.5}$$

5.2.3 AC Filter

The most common AC filter topology employed in Current Source Converters is the second order LC filter, thanks to its simplicity and low part count [5]–[7]. The boundaries for the choice of L_F and C_F (cf. Figure 5.2 (a)) values are determined by the maximum low-frequency voltage drop across L_F, the reactive power absorbed by C_F and the filter's cutoff frequency (f_{cutoff}).

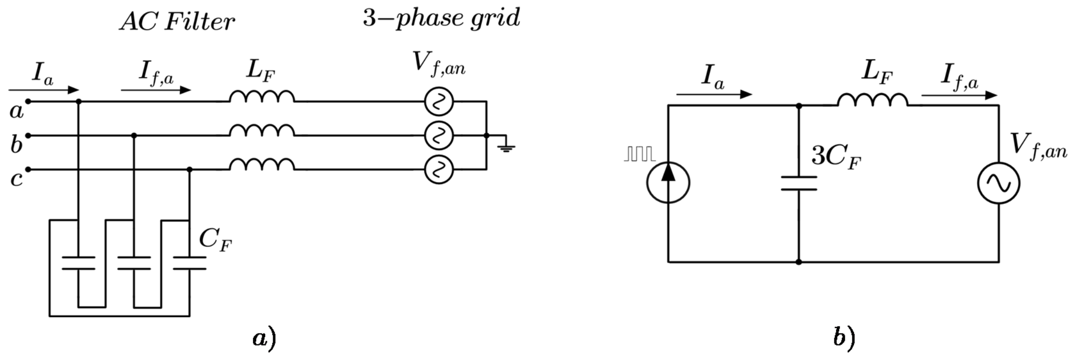


Figure 5. 2 – a) Three-phase LC filter with Δ-connected capacitors and b) its single-phase equivalent model.

Considering a single-phase equivalent circuit with Δ-connected capacitors (cf. Figure 5.2 (b)), the AC filter transfer function is given by

$$G_i(j\omega) = \frac{I_{f,a}(j\omega)}{I_a(j\omega)} = \frac{\frac{1}{3.j.\omega.C_F}}{j.\omega.L_F + \frac{1}{3.j.\omega.C_F}} \tag{5.6}$$

The upper limit of C_F value should be chosen in order to insure a relatively high power factor even in light-load conditions. Then, considering Δ-connected C_F capacitors, the following applies:

$$C_{F,\Delta,max} \leq \frac{(5 \ldots 10\%) \cdot P_n}{3 \cdot 2\pi f_{grid} \cdot V_{f,l-l}^2} \tag{5.7}$$

On the other hand, the voltage drop V_{L_F} across L_F should not exceed 2% of the grid voltage peak value. Note that V_{L_F} is added to the semiconductor blocking voltage and, for that reason, should be minimized. In addition, V_{L_F} counteracts to reduce the CSI MPP voltage range.

$$L_{F,max} \leq \frac{2\% \cdot \hat{V}_{f,l-l}}{2\pi f_{grid} \cdot I_{f,a}} \tag{5.8}$$

To avoid unwanted resonances with non-characteristic low-order harmonics in the grid and with harmonics generated by the PWM, the following should be taken into account:

$$10 \cdot f_{grid} \leq f_{cutoff} \leq 0.1 \cdot F_{sw} \tag{5.9}$$

An attenuation factor α is then defined for the most critical harmonics, i.e., around F_{sw}. Given the criteria above together with α, an initial couple of values (C_F, L_F) can be chosen using:

$$C_F \cdot L_F = \frac{1}{3 \cdot 2\pi \cdot F_{sw}^2}\left(1 - \frac{1}{\alpha}\right) \tag{5.10}$$

From this point, an iterative process can be implemented [6] where the decision criteria is set to be the THD_i. Figure 5.3 depicts the flowchart for the filter elements calculation.

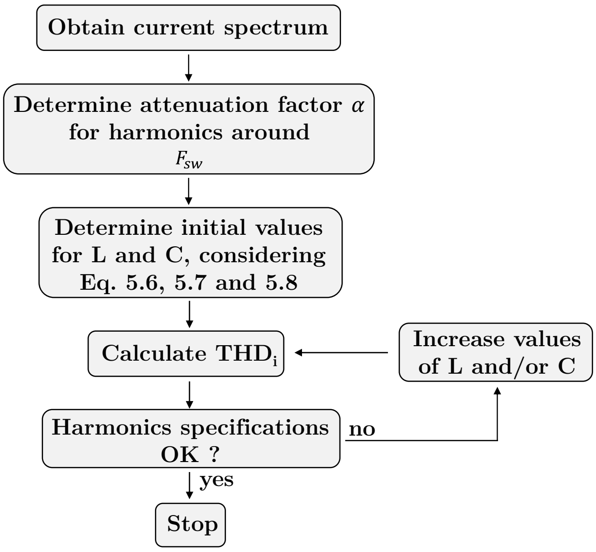


Figure 5. 3 – Flowchart for calculation of the AC filter elements.

Concerning the three-phase filter capacitors C_F, the designer has the choice to connect them in Y or Δ configuration (obviously, after employing the corresponding Y-Δ transformation). In terms of stored energy, both options are equivalent. Nevertheless, seen from the switching cell terminals, a Y connection leads the equivalent series inductance (ESL) to be doubled. As discussed in § 4.5.5, this parasitic inductance should be minimized to avoid resonances with the switching cell decoupling capacitors. Another advantage of Δ-connected capacitors is that their values and RMS currents are reduced by a factor of $1/\sqrt{3}$ (if compared to Y-connected elements). On the other hand, Δ-connected capacitors are more stressed in terms of RMS voltage (by a factor of $\sqrt{3}$). This might became an issue especially for higher grid voltage levels (e.g., 800V), where the choice of commercially available AC capacitors suitable for high-frequency operation (several tens of kHz) is strongly restricted.

In high-current applications, another important factor to consider when designing filter capacitors is the RMS current per component, which should not exceed the manufacturer's recommendations. Also, that is a variable to be taken into account while calculating the capacitor lifetime. Then, the total current per capacitor, considering Δ connected elements, is presented in Eq. 5.11. Here, the reactive current at grid frequency and all harmonic components are considered.

$$I_{C_{F,\Delta}} = \frac{\sqrt{\sum_{h=2}^{\infty} I_{a,h}^{2} + \left(V_{f,an} \cdot 2\pi f_{grid} \cdot 3 \cdot C_{F}\right)^{2}}}{\sqrt{3}} \tag{5.11}$$

5.3 Thermal Management

In many power electronic applications, semiconductor devices are the major contributors to overall power losses [8]. For that reason, the cooling system must be carefully designed to insure safe thermal operation in the worst case condition. Besides that, with the aim of reducing costs, a minimum heat sink thermal resistance per volume is desired. Taking into account the CSI power level in the present work and to be independent of installation/mounting constraints, only forced convection is considered.

5.3.1 Heat Sink Sizing

To insure safe thermal operation, i.e., $T_j < 150°C$, a minimum case-to-ambient thermal resistance ($R_{th,c-amb,min}$) should be calculated. This is carried out taking into account the minimum DC voltage ($V_{MPP,L}$) at nominal power when the maximum ambient temperature occurs. Here, the same CSI thermal model of § 3.3.3 is implemented to calculate the devices' junction temperatures through the flowchart of Figure 3.10. The obtained switching energies of § 4.5.2 are considered in the calculations. Then, assuming the worst thermal case $T_{amb} = 50°C$, $T_{c,max} = 125°C$, $F_{sw} = 60kHz$, $P_n = 60kW$, $V_{dc} = 665V$ and $T_{j,max} = 150°C$, the minimum case-to-ambient thermal resistance is $R_{th,c-amb,min} = 0.5K/W$.

The adopted thermal interface material (TIM) is a compressible graphite sheet (PGS) EYGS0611ZLWH, from Panasonic, whose thermal conductivity is 28W/mK. Choosing a solid material as TIM allows an easier prediction of the case-to-sink thermal resistance ($R_{th,c-s}$), since its thickness might be adjusted by the module's mounting torque/pressure. Furthermore, problems associated with repeatability of the module's mounting procedure are avoided. This is typically not the case when employing thermal grease, due the difficulty to control the applied grease layer. The chosen heat sink is the LAV1830024 with integrated fans, from Fischer Elektronik. Its thermal resistance is 0.023K/W. In Table 5.1, the characteristics of the adopted TIM and heat sink are summarized.

Table 5. 1 – Characteristics of the adopted cooling system.

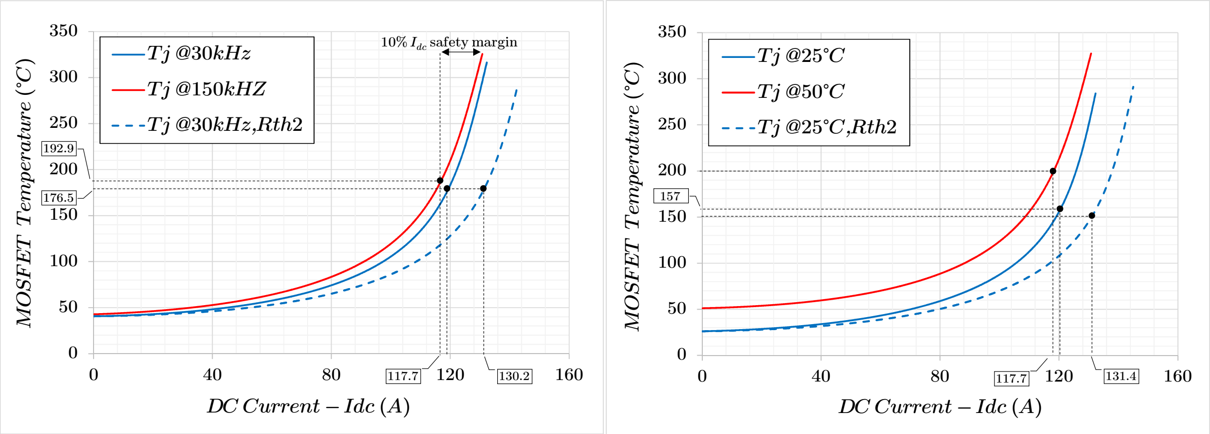
TIM (EYGS0611ZLWH)	Thickness/compressibility : 200µm/40% (@600kPa) Thermal conductivity: 28W/mK (z-direction) Thermal resistance: 0.2cm^{2}K/W (@600kPa) Dimensions: 82x62mm
Heat sink (LAV1830024)	Dimensions: 243x300x120mm Material: Al Thermal resistance: 0.023K/W Fans voltage supply: 24V

Implementing the aforementioned thermal resistances $R_{th,c-s}$ and $R_{th,s-amb}$ in the CSI thermal model, in the worst case scenario, the SiC MOSFET and diode junction temperatures are $T_{j,MOS} = 130°C$ and $T_{j,D} = 108°C$, respectively.

5.3.2 SiC Module Thermal Runaway

The capability of SiC devices to operate at very high temperatures (up to 600°C) is not rarely found in the literature [9], [10]. In most cases, only the intrinsic material capability is regarded, without taking into account realistic application conditions. In that direction, some studies [11], [12] have indicated that the practical temperature limit of SiC power devices is much lower than the material potential itself. For a given cooling system, this thermal limitation can be explained by the semiconductor intrinsic self-heating effect [11], which is caused by the electron mobility degradation with the temperature, as discussed in § 3.3.1. As an example, let's consider the case of a power MOSFET generating a given amount of conduction losses, which are dissipated through a heat sink. The system thermal stability is guaranteed as far as the amount of generated heat is lower than the heat sink capability to evacuated losses. If the MOSFET current is increased to a certain level, this condition might not be satisfied anymore and the system enters into thermal runaway.

To evaluate the thermal limits of the developed SiC module, the overall semiconductor losses ($P_{cond} + P_{sw}$) are calculated for a given switching frequency, cooling system ($R_{th,c-s} = 0.004K/W$ and $R_{th,s-amb} = 0.023K/W$) and DC current (I_{dc}) stress. Thus, the criteria of thermal runaway is defined when the derivative of I_{dc} with respect to the MOSFET junction temperature tends to zero. Additionally, a 10% current safety margin is applied. In this analysis, only the MOSFETs junction temperatures are of interest, since they represent the most thermally stressed devices at nominal power. Figure 5.4 depicts the obtained results for two case studies: a) fixed ambient temperature at different switching frequencies and b) fixed switching frequency at different ambient temperatures.



a) *b)*

Figure 5. 4 – Thermal runaway characteristic of the CSI module for a) $T_{amb} = 40°C$ and $F_{sw} = (30; 150)kHz$ and b) $F_{sw} = 60kHz$ and $T_{amb} = (25; 50)°C$. The dashed blue lines indicate the thermal characteristics when $R_{th,s-amb}$ is reduced by a factor of two.

From Figure 5.4 (a), it can be seen that the thermal runaway condition for $F_{sw} = 150kHz$ occurs at 130.8A/325°C. However, when applying the 10% safety margin on the DC current, this limit drops sharply to 117.7A/193°C, which is far away from the theoretical SiC material thermal limit. Thanks to the intrinsic low level of switching losses in the CSI topology, minor change is perceived in its thermal runaway behavior when varying the switching frequency from 30kHz to 150kHz. This observation supports the fact that the CSI is capable of operating at higher switching frequencies.

On the other hand, ambient temperature changings have a non-negligible impact on the module thermal runaway characteristic. As can be seen in Figure 5.4 (b), the maximum junction temperature ($T_{j,max}$) shifts from 157°C to 200°C, when varying the ambient temperature from 25°C to 50°C. The module current capability remains almost unchanged (120A to 117.7A). In the conduction heat transfer mechanism, the difference of temperature between the semiconductor junction and the ambient imposes the heat flux rate from the die to the ambient accordingly to the respective thermal resistance. This explain the fact that, when shifting the ambient temperature from 25°C to 50°C, the MOSFET $T_{j,max}$ is also shifted in the same direction. In that way, an increase in the ambient temperature pushes the thermal instability limit to higher temperatures as well and the converter does not have its power limit capped much. When employing a higher performance cooling system – $R_{th,s-amb}$ improved by a factor of two – (dashed blue lines in Figure 5.4), the module current capability is also increased, as expected.

As discussed in [11], SiC-based power conversion systems in which conduction losses are dominant over switching losses (as for the CSI) are more prone to thermal instability problems. Solutions to this issue could involve: *i)* operating at higher ambient temperatures, to push $T_{j,max}$ to higher levels – which is not recommended for other converter components (e.g., capacitors), *ii)* increasing the contribution of switching losses, which are temperature-independent, in the overall semiconductor losses and *iii)* simply improving the cooling system performance.

5.3.3 Experimental Evaluation of the Module Thermal Behavior

With the aim of experimentally evaluating the CSI module thermal behavior and the cooling system performance, the test setup presented in Figure 5.5 is built. Here, the power modules are mounted on the aforementioned heat sink and the semiconductors are thermally stressed with a DC current (I_{dc}) imposed by an external power supply. In these tests, the module's dielectric gel is removed and the devices are painted matt black (assumed emissivity of 0.95), in order to have sharp thermal images of the dies without reflection. Then, all semiconductor junction temperatures are directly measured with an infrared camera FLIR A300 placed 40cm away from the modules. The I_{dc} measurement is carried out using a Lecroy CP150 current probe.

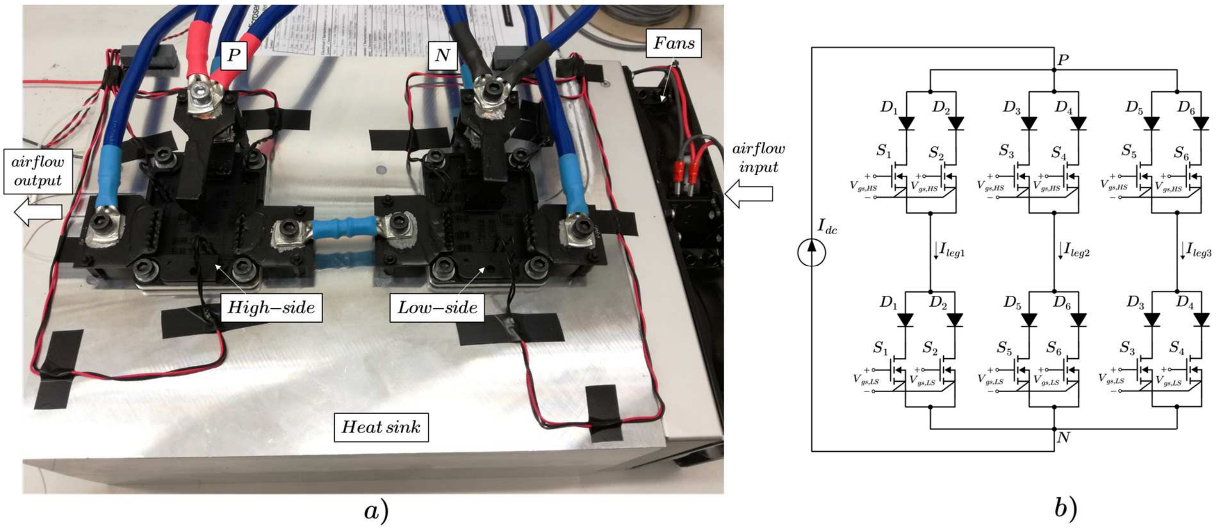


Figure 5. 5 – a) Experiment setup for DC current thermal tests and b) its corresponding electric circuit. Test conditions: $V_{gs} = 20V$ and $V_{fan} = 24V$.

Figure 5.6 depicts the employed nomenclature for each semiconductor die in both high- and low-side modules.

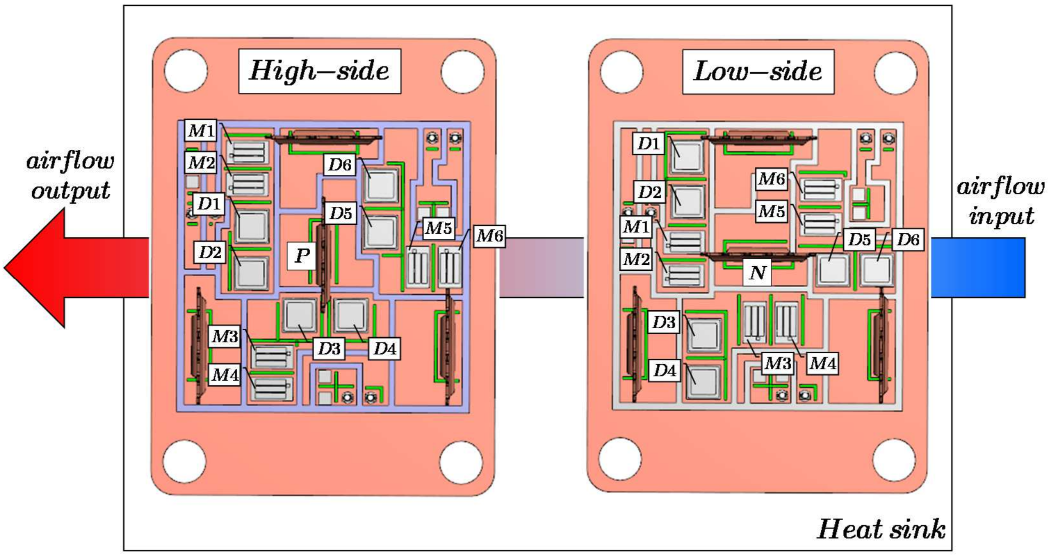


Figure 5. 6 – Employed nomenclature of dies for the thermal tests.

To analyze the temperature distribution inside the modules, a DC current is applied to thermally stress the dies while keeping a safety margin of $T_{j,max} = 125°C$. Starting at 20A, I_{dc} is imposed until the thermal stability is reached, which takes approximately 25min for each point. Figure 5.7 presents the results for two DC current values. Here, the junction temperatures are measured in the center of the dies using markers of 3x3 pixels (black crossed squares in Figure 5.7). T_j is then obtained doing the mean-value of these 9 (3x3) measured values.

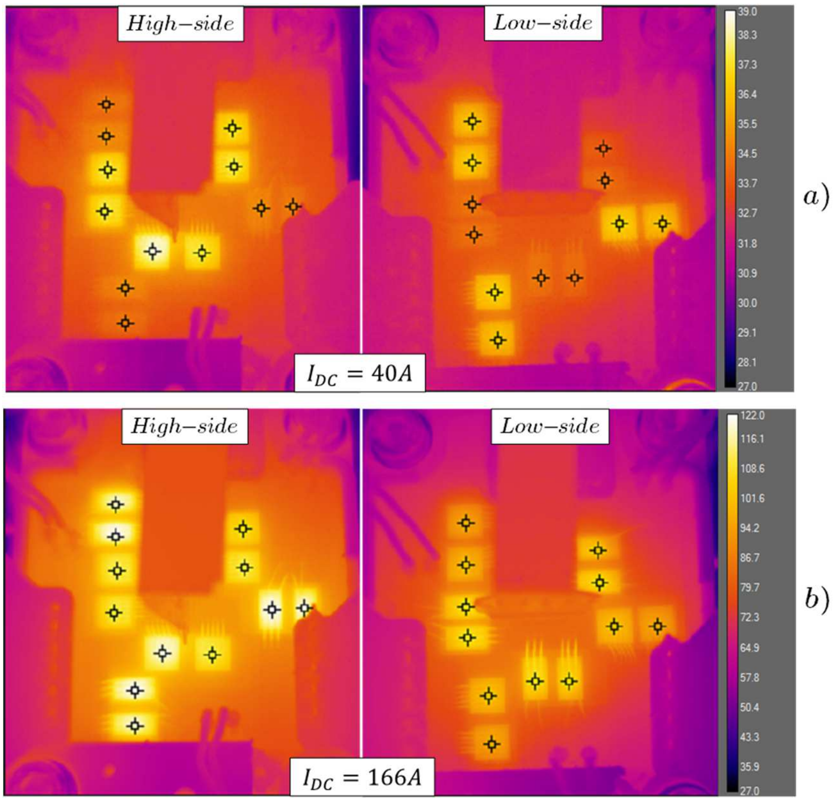
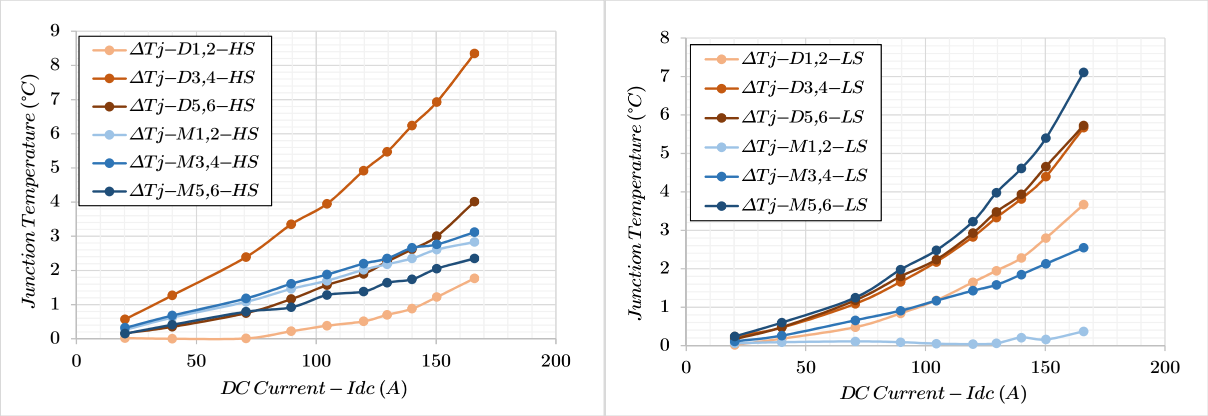


Figure 5. 7 – Junction temperatures when a) $I_{dc} = 40A$ and b) $I_{dc} = 166A$.

As expected, at light-load conditions (cf. Figure 5.7 (a)), the most thermally stressed devices are the SiC diodes – due to the presence of the threshold voltage (V_o), as highlighted in § 3.3.3. When increasing I_{dc}, the junction temperatures of MOSFETs set the module thermal limit. Considering the case where $I_{dc} = 166A$, it becomes clear that the devices do not share a common junction temperature. In reality, the chips which are closer to the common node P/N tend to be more thermally stressed. As foreseen in § 4.3.4 through FEM Q3D simulations, the dies offering a less resistive path for the DC current see higher current densities. Furthermore, these devices in the center of the module have their equivalent junction-to-case thermal resistance increased, due to the mutual self heating effect between dies [13]. Diversely, the dies located in the module periphery (e.g., $M_{1,4,6-HS}$) are less thermally coupled with other dies (in this case less important mutual thermal resistances exist) and might then better evacuate losses. As a matter of fact, there is an exact correspondence between the most thermally stressed devices in Figure 5.7 (b) and the devices which carry the highest current levels in Figure 4.19. This observation supports the fact that, although presenting a positive temperature coefficient, the employed SiC devices are not capable of fully compensating their mutual current unbalance. In Figure 5.8 are presented the deviation of junction temperatures per chip pair, i.e., $\Delta T_{j-D1,2-HS} = |T_{j,D1-HS} - T_{j,D2-HS}|$, and so forth.



a) *b)*

Figure 5. 8 – Junction temperature deviations per die pair for the most constrained case, i.e., $I_{dc} = 166A$, in the a) high-side and b) low-side module.

In view of the HS module, one concludes that reasonable temperature deviations (<4°C) occur for all die pairs, with exception of devices D_3 and D_4. Since group of semiconductors 3-4 is disposed in an L-shaped form in close proximity to group 1-2, the chip D_3 placed at the corner is simultaneously heated up by the devices of its group and by the neighboring group. However, it should be noted that, even presenting the highest module junction temperature, D_3 does not generate switching losses during nominal operation, as shown in § 4.5.4. Thereby, it should not be the limiting device in the module. Concerning the LS power module, the MOSFET pair of dies 5-6 are the most thermally unbalanced devices. Contrarily to the previous case, the temperature deviation $\Delta T_{j-M5,6-LS}$ comes from the fact that M_6 represents the less hot device in the packaging, since it is located in the module periphery, far away from the other chip groups. Besides that, diodes in the L-shaped groups 3-4 and 5-6 are considerably unbalanced. At this point, it can be concluded that the paralleling of SiC diodes is more prone to thermal unbalance than SiC MOSFETs. This might be explained by the fact that SiC diodes present a loss component (V_o), which has a negative temperature coefficient. Hence, even though being compensated by the positive temperature coefficient of R_o, V_o does not contribute to counterbalance current mismatches in paralleled chips.

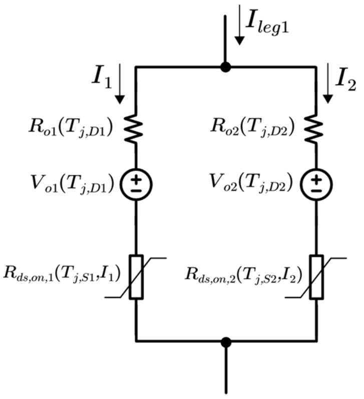


Figure 5. 9 – Employed PSIM model for current sharing estimation.

Knowing that a non-negligible difference exists in terms of the junction temperatures within the CSI module, of interest now is how these thermal disparities affect the losses generated per chip. Having this in mind, a PSIM model is developed to estimate the I_{dc} current sharing between all chips in both HS and LS modules. Figure 5.9 exemplifies the employed model for the HS group of dies 1-2. Based on its on-state characteristic (cf. Appendix I), a non-linear resistive element is used to model the MOSFET on-state resistance taking into account its junction temperature and drain current dependency. The SiC diodes are modeled using voltage source and resistive elements, whose values only depend on their junction temperatures. Hence, together with I_{dc}, all 12 measured junction temperatures are the simulation input. Thereby, the chips current sharing as well as the power losses per chip can be easily computed. In Table 5.2 and 5.3 are summarized the results for the most constrained thermal case, i.e., $I_{dc} = 166A$.

Table 5. 2 – DC current sharing between branches in legs 1, 2 and 3 for $I_{dc} = 166A$.

$\Delta I_{1,2-HS}$ (A)	$\Delta I_{3,4-HS}$ (A)	$\Delta I_{5,6-HS}$ (A)	$\Delta I_{1,2-LS}$ (A)	$\Delta I_{3,4-LS}$ (A)	$\Delta I_{5,6-LS}$ (A)
0.252	0.597	0.373	0.149	0.457	0.997

$I_{leg1} = 55.2A$, $I_{leg2} = 55.63A$ and $I_{leg3} = 55.17A$.

Table 5. 3 – Simulated power losses deviation between device pairs for $I_{dc} = 166A$.

Device	$\Delta P_{1,2-HS}$ (W)	$\Delta P_{3,4-HS}$ (W)	$\Delta P_{5,6-HS}$ (W)	$\Delta P_{1,2-LS}$ (W)	$\Delta P_{3,4-LS}$ (W)	$\Delta P_{5,6-LS}$ (W)
MOSFET	0.18	1.52	0.83	0.46	0.99	1.64
Diode	0.69	0.57	0.46	0.03	0.51	1.61

From these data, one concludes that the current sharing between branches are quit balanced. At its worst, ($\Delta I_{5,6-LS} = 0.997A$) the branch current mismatch represents only 1.8% of $I_{dc}/3$. Nevertheless, the pair of devices that undergo the biggest current sharing disparities also encounter the greatest differences in terms of generated power losses (e.g., the LS group 5-6 and HS group 3-4). On the other hand, the chips that have the lowest power losses deviations (the same is valid for T_j, see Figure 5.8) are those of HS and LS group 1-2. The in-line arrangement of dies in these groups facilitates the homogeneity of junction temperatures. In a future work, the possibility of avoiding L-shaped chip arrangements should be considered, in order to improve the module thermal management. Furthermore, a supplementary design modification to reduce the thermal coupling between MOSFETs (most thermally stressed devices in switching operation) of a same group of dies is to dispose the semiconductors as follows: MOS-diode-MOS-diode (and not MOS-MOS-diode-diode, as is the case in the developed module). This could lead to more homogenous junction temperatures within the packaging.

In Table 5.4, the absolute deviation of power losses with regard to the average losses per chip are given.

Table 5. 4 – Absolute deviation of power losses with regard to the average for $I_{dc} = 166A$.

Device	Module	dP_1 (W)	dP_2 (W)	dP_3 (W)	dP_4 (W)	dP_5 (W)	dP_6 (W)
MOSFET	HS	0.48	0.66	0.25	1.27	0.36	0.47
	LS	0.70	0.24	0.56	0.44	1.23	0.41
Diode	HS	0.17	0.53	0.31	0.89	0.65	0.19
	LS	1.35	1.38	1.61	1.1	1.72	0.11

$\bar{P}_{M-HS} = 54.88W$, $\bar{P}_{D-HS} = 41.29W$, $\bar{P}_{M-LS} = 50.75W$ and $\bar{P}_{D-LS} = 40.08W$.
Absolute deviation definition : $dP_{M,D,i} = |P_{M,D,i} - \bar{P}_{M,D}|$.

Here, in the worst possible thermal scenario, i.e., $I_{dc} = 166A$, a relatively equal sharing of losses between the devices within a same packaging is observed. Considering, for example, diode D_3 in the LS module, its losses are only 1.61W (or 4%) above the average (40.08W). Consequently, one concludes that, even under different junction temperatures, the devices integrated in the same packaging can be assumed to generate equivalent conduction losses, due to the relatively good share of I_{dc}. This is an important observation on which the CSI calorimetric characterization method will be based later on in this chapter.

Moreover, it should be pointed out that the HS and LS modules do not experience the same effective sink-to-ambient thermal resistance. Due to practical reasons, one module is placed closer to the fans than the other. Thus, the CSI thermal limit is dictated by the furthest module with respect to the fans (HS module in this case). Then, at 166A, $T_{j,max,M-HS} - T_{j,max,M-LS} = 14°C$.

5.4 Efficiency Estimation

In this section, semiconductor efficiency calculations are carried out considering the CSI operation with two distinct grid voltages. Based on the previous thermal tests, the cooling system model is calibrated to take into account its non-idealities. Thereby, $R_{th,c-s} = 0.005K/W$ and $R_{th,s-amb} = 0.025K/W$ are now considered. Assuming the CSI operation on a 690V grid, $P_{in} = 60kW$, $F_{sw} = 60kHz$, $R_{g,off} = 1.1\Omega = 2 \cdot R_{g,on}$ and the same modulation strategy Mod1 employed in § 4.3.2, the semiconductor efficiency is calculated for three DC voltages (equal to the mid- and limit-values of the MPP voltage range, as discussed in § 3.2.2). Figure 5.10 shows the efficiency curves together with the module junction temperatures for the most constrained thermal scenario ($V_{dc} = 665V$). As a case study, F_{sw} is defined in order to cap the total L_F and L_{dc} inductor losses at 500W, at nominal power. The losses are modeled based on toroidal powder core inductors in combination with Litz wire for both DC and AC inductors; iGSE method based on Steinmetz coefficients and Dowell approximation are also used for core and copper losses estimation, respectively.

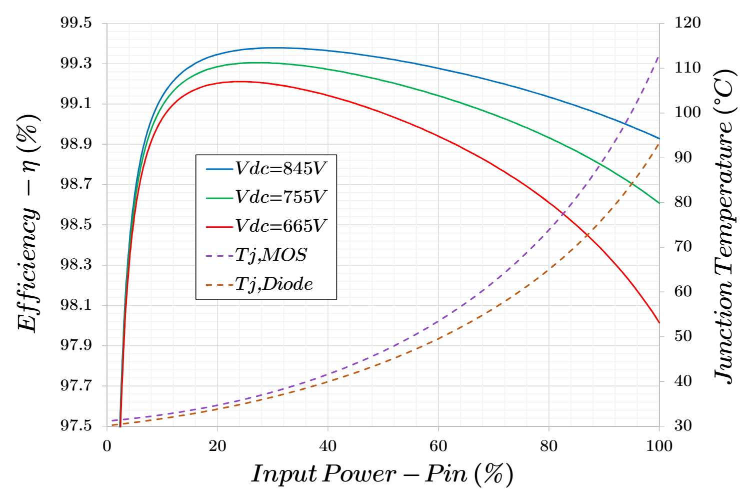


Figure 5. 10 – Semiconductor efficiency as a function of the input power and junction temperatures for $V_{dc} = 665V$, $r_{g,off} = 1.1\Omega = 2 \cdot r_{g,on}$, $T_{amb} = 30°C$ and $P_{in} = 60kW$.

The highest efficiency (99.38%) is given for a DC voltage of 845V at 30% of P_{in}. On one hand, due to fast increasing of MOSFET conduction losses with the input power (because of the $r.i^2$ term), the CSI efficiency is degraded to 98% in the worst case ($V_{dc} = 665V$ @60kW). On the other hand, thanks to the fact that the CSI switches block a sinus-modulated voltage, the C_{oss}–related switching losses are relieved, making possible to achieve a relatively high efficiency at light load conditions: for all DC input voltage levels, $\eta > 99\%$ when $P_{in} > 10\%$. This characteristic is particularly interesting for solar applications, since PV inverters operate most of the time in partial load conditions. In terms of the European Efficiency, the CSI presents $\eta_{euro} = 99.22\%$, 99.08% and 98.86% for $V_{dc} = 845V$, $755V$ and $665V$, respectively.

Figure 5.11 depicts the CSI iso-efficiency curves and the module thermal limit (dictated by $T_{j,MOS}$) for $V_{dc} = 665V$. These results show the low CSI efficiency sensibility with regard to F_{sw}. In fact, when increasing F_{sw} from 1kHz to 300kHz, the maximum admissible input power is degraded from 67.1kW to 61.3kW, which represents only a 9% derating. This supports the fact of placing the CSI as a well-suited topology for high-frequency applications.

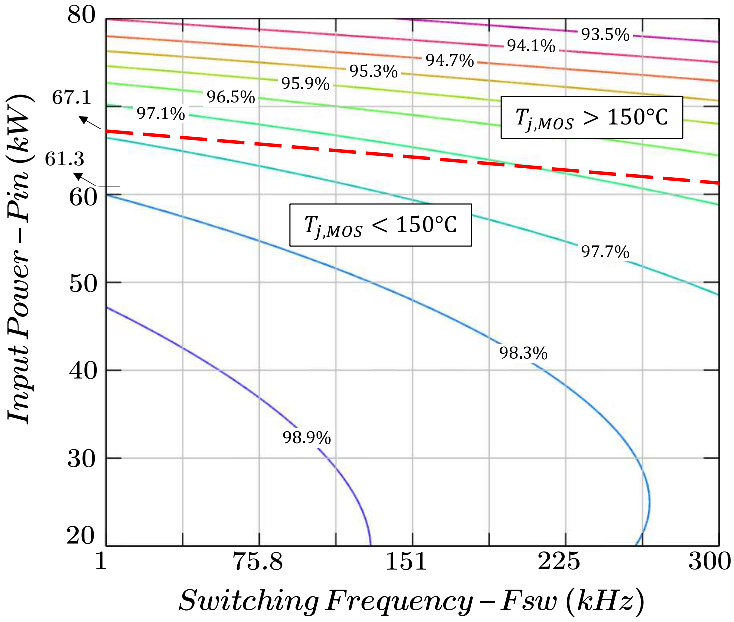


Figure 5. 11 – CSI iso-efficiency curves and module's thermal limit (red line) as a function of F_{sw} for $V_{dc} = 665V$ and $T_{amb} = 30°C$.

5.4.1 CSI Operation on a Three-phase 800V Grid

Now, considering the CSI operation on a three-phase 800V grid, the efficiency calculations carried out so far are redone. Table 5.5 summarizes the obtained results.

Table 5. 5 – Results for the CSI operation on a three-phase 800V grid.

Grid voltage	Max. device blocking voltage (V)	V_{MPP} range (V)	AC grid current [1] (A)	η_{max} [2] (%)	η_{euro} [2] (%)	$T_{j,MOS,max}$ [3] (°C)	$P_{in,max}$ [4] (kW)
800V	1131	314	43.3	99.41	99.28	115	65.6
690V	976	180	50.2	99.38	99.22	113	65.9

Considering: 1) constant Pin=60kW 2) constant Pin=60kW, Fsw=60kHz and Vmpp,H 3) same as in 2) excepted for Vmpp,L and 4) limited by $T_{j,MOS,max}$, when Fsw=60kHz and Vmpp,L occurs.

From that, the following conclusions can be drawn: *i)* the V_{MPP} range is remarkably increased for the 800V grid; *ii)* any significant thermal stress is added while changing grid voltage levels (due to the low level of switching losses); *iii)* costs might be capped when designing AC components (AC filter, power terminals, line relays and etc) for the 800V grid, since the respective line currents are reduced and *iv)* the peak and European efficiencies are not noticeably modified from one grid voltage to another. Nevertheless, in a design where the junction temperatures approach their thermal limits (150°C) at nominal power, it has been seen that a non-negligible difference in terms of η_{euro} appears. In such cases, the semiconductor electro-thermal coupling can be alleviated by increasing the grid voltage for a given power level. The only drawback of augmenting the AC grid voltage is related to the semiconductor's voltage safety margin and lifetime issues. However, making use of 1.7kV devices in combination with a proper layout design (C_{dec} included), the switching overvoltages might be restricted within reasonable values, allowing the CSI to safely operate on an 800V grid.

5.5 Comparison with a Standard Solution: DC-DC Boost Converter in combination with a Three-phase Two-level Voltage Source Inverter

To compare the CSI performance with a standard two-stage voltage-source based structure, the DC-AC conversion system composed of a DC-DC boost converter in combination with a three-phase two-level Voltage Source Inverter (VSI) is evaluated in this section (see Figure 5.12). Therefore, considering identical specifications for a 60kW PV application, focus is given to compare both solutions in terms of semiconductor efficiency and DC passive elements sizing. The comparison regarding the AC filtering efforts is not performed here. As seen in § 3.5.1 and more extensively analyzed in [14], due to their duality rules, CSCs and VSCs generate similar current and voltage spectra, respectively, when equivalent modulation strategies are employed. Thus, for a given switching frequency, identical AC filtering efforts are required for both inverters. Furthermore, the most common employed AC filter topology in VSCs is the 3rd order LCL filter (and not the 2nd order LC filter, as is usually the case in CSCs). Thereby, a straightforward comparison of different filter topologies in different converters could lead to the conversion systems misevaluation.

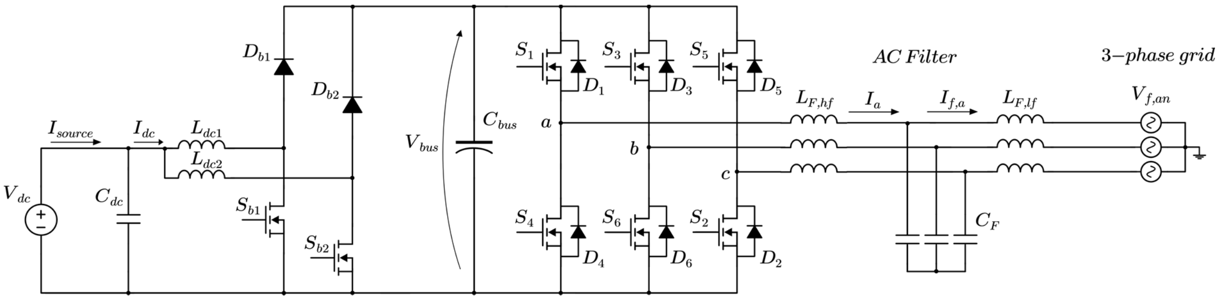
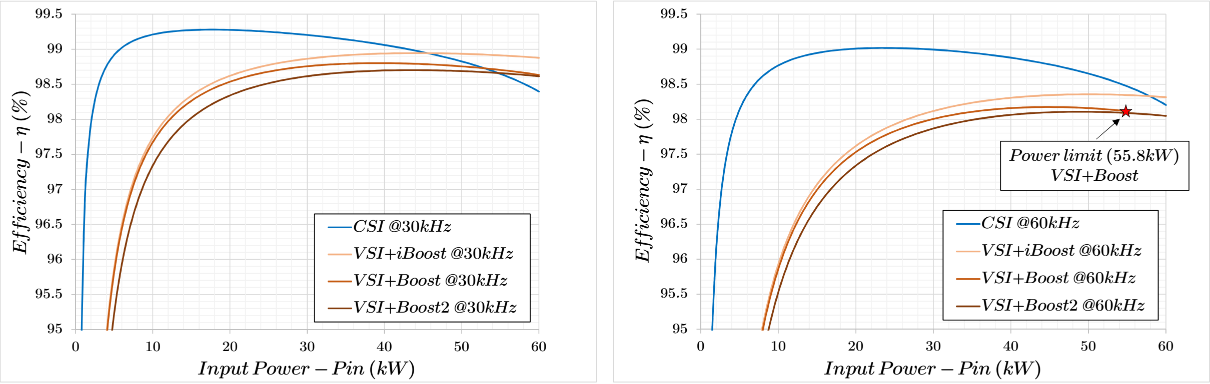


Figure 5. 12 – Two-stage topology: interleaved boost converter in combination with a three-phase two-level VSI.

Concerning the DC-DC voltage step-up converter, three unidirectional boost configurations are studied here, namely, Boost, Boost2 and *i*Boost. The Boost and Boost2 are simply boost converters (with a single L_{dc} inductor element) and they differ from each other by the number of semiconductor chips in parallel per device, which is doubled for Boost2 ($n_{Boost2} = 2 \cdot n_{Boost}$). *i*Boost stands for the interleaved boost converter with two legs, where n_{Boost} chips in parallel per device and per leg are employed. The *i*Boost legs 1 and 2 have their corresponding DC inductors ($L_{dc1,2}$ in Figure 5.12) operating at $F_{sw}/2$ each. The SiC devices used in the comparison are CPM2-1700-0045B (for all MOSFETs) and CPW5-1700-Z050B (for the series and anti-parallel diodes), from Wolfspeed. In this study, two chips per device are considered to cope with the power requirement (60kW), i.e., $n_{VSI} = n_{Boost} = n_{iBoost} = 2$. The PV conversion system and the thermal specifications are as follows: $V_{f,l-l} = 690V$, $V_{dc} = 740V$, $I_{dc} = 81A$, DC current ripple $\Delta I_{dc,max} = 20\% \cdot I_{dc}$, $V_{bus} = 1.2kV$ (for the VSI), $R_{th,c-amb} = 0.08K/W$, $R_{th,j-c,D} = 0.33K/W$, $R_{th,j-c,MOS} = 0.4K/W$ and $T_{amb} = 25°C$. For all cases, switching energies are obtained from LTspice simulations, leading to $E_{sw,VSI}(I_{dc})$, $E_{sw,Boost2}(I_{dc})$, $E_{sw,Boost}(I_{dc}) = E_{sw,iBoost}$ and $E_{sw,CSI}(V_{f,l-l})$. Concerning the VSI operation, the SiC anti-parallel diodes are assumed to conduct all the current when MOSFETs are gated off (synchronous rectification mode not considered). More detail about the employed thermal models and analytical expressions of losses are presented in Appendix III. In Figure 5.13 are depicted the semiconductor efficiency curves for all studied cases taking into account two distinct switching frequencies (30kHz and 60kHz).



a) *b)*

Figure 5. 13 – Semiconductor efficiency curves for a) $F_{sw} = 30kHz$ and b) $F_{sw} = 60kHz$.

As previously discussed in this chapter, thanks to the low level of switching losses, the CSI presents relatively high efficiency in light-load conditions. Diversely, the efficiency of all voltage-source based topologies is penalized due to the C_{oss} switching losses term. In the case of VSI+Boost, the boost MOSFET junction temperatures exceed 150°C, limiting the maximum power to 55.8kW @60kHz. Despite the fact of employing the same semiconductor chip area, when comparing the solutions VSI+Boost2 and VSI+*i*Boost, the later has a significant advantage in terms of switching losses. Since each *i*Boost leg is independently decoupled, its associated devices' C_{oss} per leg are not paralleled. This is typically not the case for Boost2, where all output capacitors are in parallel. Table 5.6 summarizes the calculated European Efficiency as well as the figure of merit FOM (introduced in § 3.3.3) for all studied converter systems.

Table 5. 6 – Calculated η_{euro} and FOM for all four studied PV converter systems.

	F_{sw} (kHz)	VSI+Boost	VSI+*i*Boost	VSI+Boost2	CSI
$\eta_{euro}(\%)$	30	98.3	98.42	98.11	99.02
	60	-	97.29	96.98	98.73
$\frac{FOM}{FOM_{CSI}}$	30	0.57	0.54	0.45	1
	60	-	0.41	0.37	1

$FOM = 1/(A_{T,chip} \cdot (1 - \eta_{euro}))$.

As expected, the CSI presents the highest η_{euro} for both switching frequency values. Moreover, thanks to the presence of a single conversion stage, the topology appears to be the most cost-effective (highest FOM), from a semiconductor point of view. The VSI+Boost converter operating at 30kHz appears to be the second most cost-effective solution. Here, it should be pointed out that the η_{euro} of VSI+*i*Boost solution could be improved by shutting down one *i*Boost leg in light-load conditions (while insuring CCM operation). This could improve its FOM, especially for $F_{sw} = 60kHz$. Table 5.7 shows the DC passive elements and their characteristics for the three studied topologies capable of operating at 60kHz.

Table 5. 7 – DC passive elements sizing and their characteristics for the studied PV converter systems operating at 60kW.

Topology	F_{sw} (kHz)	L_{dc} (µH)	$P_{L_{dc,total}}$ (W)	$Weight_{L_{dc,total}}$ (kg)	C_{bus} (µF)	$E_{L_{dc,total}} + E_{C_{bus}}$ (J)
VSI+*i*Boost	30	220.6	145.2	1.6	15	11.16
VSI+Boost2		585	192	4	15	12.72
CSI		790.1	498	9.9	-	5.18
VSI+*i*Boost	60	110.3	308.6	0.9	7.5	5.58
VSI+Boost2		292	160	2.4	7.5	6.36
CSI		395.1	412	6	-	2.60

The DC capacitor (C_{dc}) is not considered in the comparison since its value is common for all cases - the same current ripple is assumed in all converter configurations.

As can be seen, the CSI DC passive elements present the lowest stored energies amongst all solutions. Nevertheless, for both switching frequency cases, the CSI shows the highest DC-link inductance values (and also the related losses and weight). Hence, when dimensioning a CSI, the designer has a larger F_{sw} range to find a compromise to minimize L_{dc} (then costs) while keeping switching losses within reasonable limits. With this in mind, the optimum CSI switching frequency tends to be higher than that of Voltage Source Inverters, which are more prone to suffer from limited efficiency due to switching losses.

5.6 Hardware Description

Based on the design guidelines discussed in § 5.2, the present section describes the developed 60kW CSI prototype together with its main components. With respect to the AC filter design, a relatively low switching frequency (i.e., 15kHz) has been considered. Since the experimental test rig is intended to be evaluated in a vast switching frequency range (15-60kHz), $F_{sw} = 15kHz$ is taken as the dimensioning frequency. Then, the AC filter values are calculated to be $C_F = 20\mu F$ (Δ–connected) and $L_F = 280\mu H$. In Table 5.8, details about the filter components are provided. Concerning the DC side, L_{dc} is chosen to be a coupled inductor, as depicted in Figure 5.14 (a). In doing so, with a single component, three distinct inductance values are obtained, depending on the employed terminal configuration. In this work, three identical coupled inductors are fabricated (cf. Figure 5.14 (b)), which can be connected in series or in parallel. This allows to have a multitude of L_{dc} values, which is particularly interesting for tests with a variable switching frequency at constant DC current ripple. The DC inductor values are measured at 30kHz to be $L_{1-2} = 182\mu H$, $L_{1-3} = 484\mu H$ (with terminals 2-4 short-circuited) and $L_{1-4} = 242\mu H$ (with terminals 2-3 short-circuited). The DC filter capacitor value is $C_{dc} = 10.8\mu F$. Table 5.8 summarizes the details of the selected DC components.

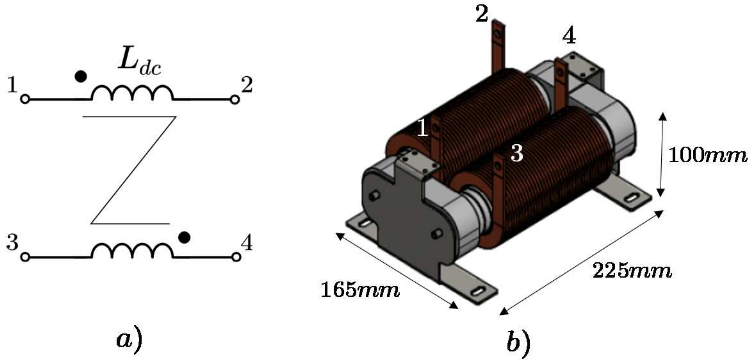


Figure 5. 14 – a) Coupled DC-link inductor and b) its realization.

Table 5. 8 – Details of the employed filter components.

Component	Value	Description
AC inductor (L_F)	280µH	SiFe core – solid round wire Dimensions (WxLxH): 108x120x95mm
AC capacitor (C_F)	20µF	2x 10µF/750Vac/20A@>1kHz Leclanché (Metallized Polypropylene) PAM 75-10.0 cvs5 K
DC capacitor (C_{dc})	10.8µF	4x 2.7µF/1.3kV/5A@10kHz Epcos (MKP) B32776T1275K000
DC inductor (L_{dc})	variable	Powder core with distributed airgaps – single flat helical winding (39 turns per leg)

5.6.1 Protection Circuit

In general, the CSI faults can be associated with three abnormal operating conditions [15]: short-circuit, overcurrent and current interruption. Due to the presence of the series diodes ($D'_{1..6}$ in Figure 5.15 (a)), a CSI short-circuit condition is only possible if the voltage bidirectional switch loses its blocking capability (i.e., series diode malfunction). In such case, short-circuit between the grid phases may occur. For that reason, protection devices as fuses and relays should be implemented on the AC grid side. When operating with a PV generator, overcurrent faults are unlikely to happen, since the maximum DC current is known and equal to the PV string short-circuit current (I_{sc}). On the other hand, due to its current-source based characteristic, an interruption of the DC-link inductor current will lead to serious overvoltages across the opened path terminals. This fault condition represents the typical failure mode in PV CSIs and its root cause is often related to: erroneous modulation, gate driver and/or semiconductor failures and mains blackout (if the inverter control is exclusively fed from the AC grid side, for example).

In the literature, some overvoltage protection circuits can be found. In [16], a crowbar circuit is proposed to short-circuit the DC-link during overvoltage fault. The main drawback of this solution is the crowbar action response delay. In reality, when employing SiC devices, the current source interruption is made almost instantly. Then, the overvoltage rise rate is only limited by the CSI parasitic capacitances (C_{oss}, C_{Ldc}, C_{CM} and etc) [15]. Given that, the time to charge the input capacitor and then turn-on the crowbar controllable switch (IGBT or MOSFET) is typically not short enough to avoid system damage. In [17] and [18], diode bridge circuits are proposed to detect and extinguish overvoltages. The advantage of these methods relies on the spontaneous turn-on behavior of diodes, which can act instantly in case of fault. Both solutions are studied and compared in this section. Figure 5.15 (b) and (c) depicts their schematics, namely protection circuit I and II, respectively.

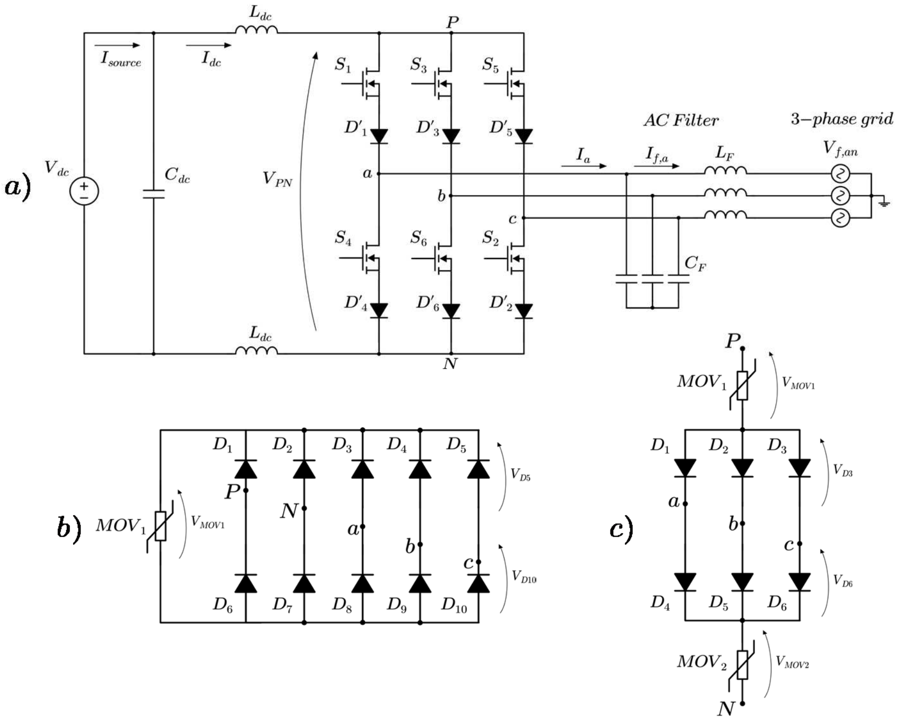
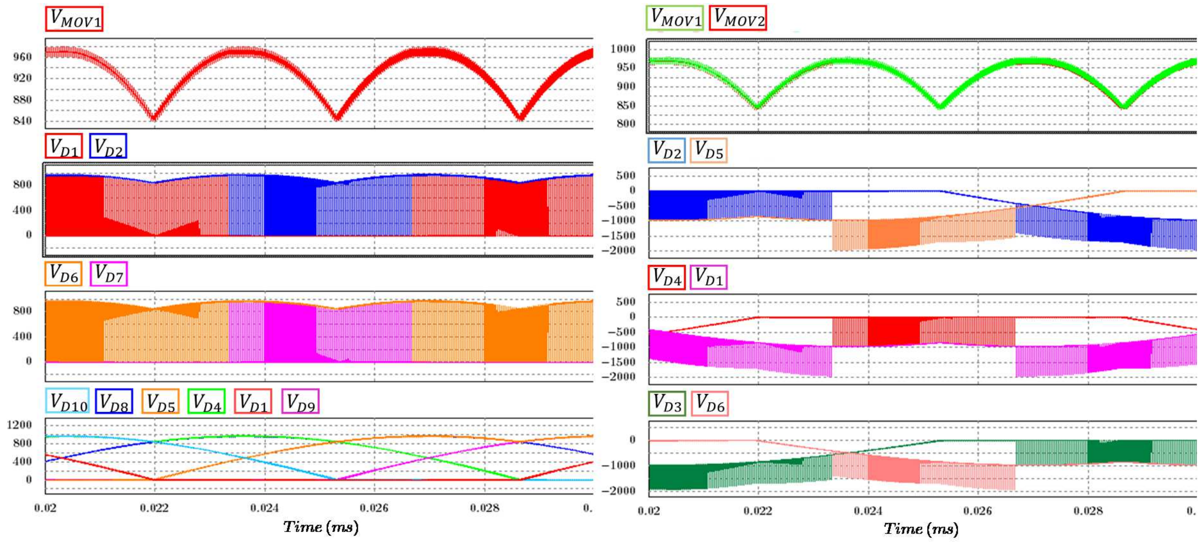


Figure 5. 15 – a) Three-phase CSI, b) protection circuit I [17] and c) protection circuit II [18].

To analyze their principle of operation, both protection circuits are simulated using PSIM for the case of a CSI operating at 30kHz on a 690V three-phase grid. The voltage limiting devices ($MOV_{1,2}$ in Figure 5.15) are modeled as a parallel RC circuit ($R = 1M\Omega$ and $C = 1nF$). The obtained voltage waveforms (defined as in Figure 5.15) are shown in Figure 5.16.



a) b)

Figure 5. 16 – Voltage waveforms for a) protection circuit I and b) protection circuit II.

Concerning the protection circuit I, at normal operation, six out of ten diodes operate at the grid frequency, i.e., 50Hz. The remaining diodes are forward biased with a frequency F_{sw} during one half of the grid period. Then, an equivalent number of 2 diodes are charged/discharged at any time during normal inverter operation. Besides the energy needed to charge and discharge the protection devices, the diodes' junction capacitances are added to the power semiconductors C_{oss}, slowing down dv/dt rates and increasing switching losses. In this protection scheme, the maximum diode blocking voltage is 976V ($\hat{V}_{f,l-l}$). With regard to protection circuit II, all diodes operate at F_{sw} during one half of the grid period. Then, an equivalent number of 3 diodes are charge/discharged at F_{sw}. Here, it is worth noting that all diodes float between zero and $-2 \cdot \hat{V}_{f,l-l}$. In Table 5.9 are summarized the main characteristics of both protection schemes.

Table 5. 9 – Comparison of protection circuits I and II.

Protection Circuit	Nb of diodes	Diode max. blocking voltage (V)	Equivalent Nb of diodes under dv/dt @ F_{sw}	Nb of diodes operating at 50Hz	Nb of voltage limiting devices
I	10	$\hat{V}_{f,l-l}$	2	6	1
II	6	$2 \cdot \hat{V}_{f,l-l}$	3	–	2

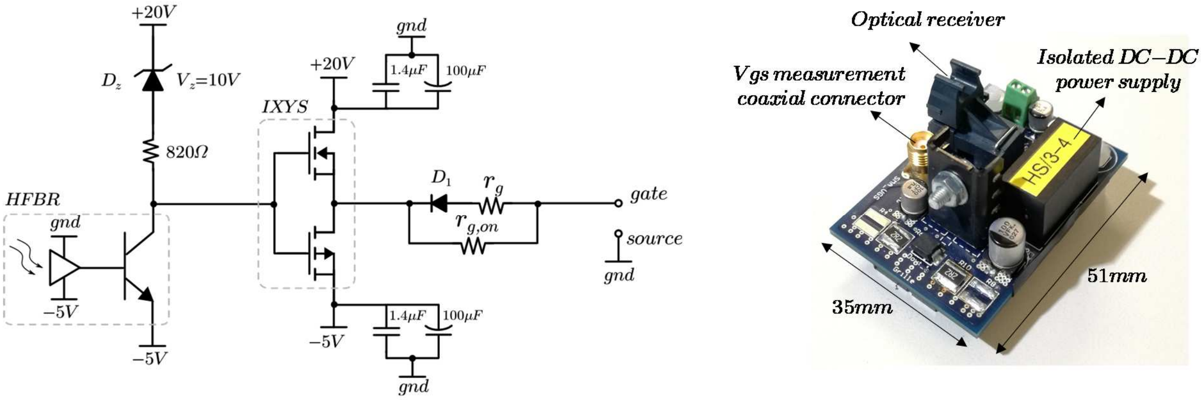
In this work, the CSI protection circuit II is implemented. The fact of having two separate voltage limiting devices allows the designer to split the protection circuit in two, making its implementation easier. Hence, $D_{1..6}$ are realized using SMD 1.2kV/10A SiC Schottky diodes (STPSC10H12-Y, from STMicroelectronics) – two devices in series per diode – and the voltage limiting devices are chosen to be Metal Oxide Varistors (MOV) (B72240L0751K102, from TDK), which typically present low parasitic capacitance (<1nF @1kHz). The circuit protection realization is shown in Figure 5.20.

Although being capable of absorbing great amounts of energy (1.2kJ during 2ms), MOVs are not suitable to continuously dissipate power. For that reason, during abnormal operation, the fault should be detected as soon as possible and the DC-link inductor short-circuited. With this in mind, a possible protection circuit might be a hybrid solution of a crowbar in combination with a diode bridge and MOV. Thereby, the MOV could be designed to limit the initial overvoltage while a crowbar IGBT is turned-on.

5.6.2 Gate Driver

When designing a gate driver adapted to WBG devices, the following specifications are usually considered [19]: *i)* electrical isolation between the logic control and power circuits with a sufficient *dv/dt* immunity, *ii)* capability of quickly charging and discharging the power device input capacitances, *iii)* gate-to-source voltage oscillations and overshoots, *iv)* power capability to gate the power device with the specified voltages when operating at F_{SW} and P_n and *v)* low jitter and delay mismatch levels.

Most of commercially available gate drivers are suitable for voltage-source based topologies. Therefore, they are designed to prevent failure by shutting down the controlled power device in the case of short-circuit condition. However, as discussed in the previous section, the typical CSI failure mode is the DC current source interruption. For that reason, an appropriate gate driver without any protection or presenting protection against drain-to-source overvoltages should be implemented. In this work, a new optically isolated gate driver is built. Figure 5.17 presents the driving circuit and its corresponding realization.

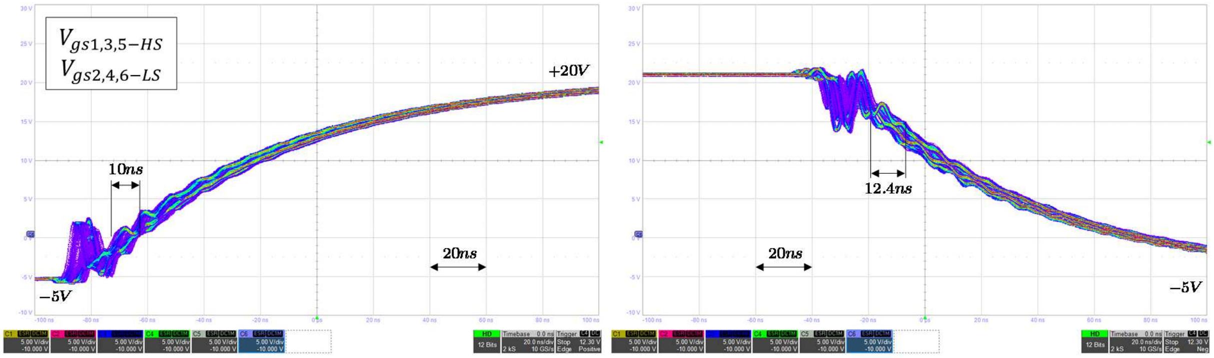


a) *b)*

Figure 5. 17 – a) Optically isolated gate driver circuit and b) its realization.

For the presented gate driver, electrical isolation is insured by a fiber optic link between the logic control and power circuits. Optic receivers Avago HFBR 2531z are employed for this purpose. The *dv/dt* immunity is guaranteed by choosing a DC-DC converter Murata MGJ2D052005SC (+20/-5V, 2W) with reinforced insulation (up to 80kV/µs @1.5kV). The driver output stage is a 14A MOS-based push-pull configuration IXDN614YI from IXYS. Moreover, two distinct resistors are employed to independently adjust turn-on and turn-off transition times. The gate driver does not present any protection circuitry.

Figure 5.18 presents the jitter analysis for all six CSI gate drivers when loading an RC circuit with $r_{g,on} = r_{g,off} = 10\Omega$ and $C_{load} = 6.8nF$. For reminding, the CSI module $C_{iss} = 7.3nF$.

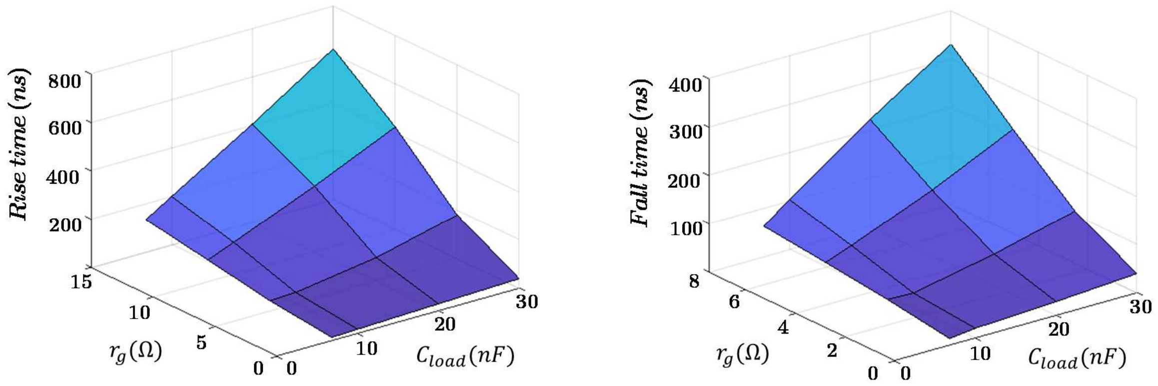


a) *b)*

Figure 5. 18 – Gate driver jitter measurement for all six control signals ($V_{gs1,3,5-HS}$ and $V_{gs2,4,6-LS}$) for $r_{g,on} = r_{g,off} = 10\Omega$ and $C_{load} = 6.8nF$. A digital Lecroy HDO8000A oscilloscope in infinite persistence mode is employed in these measurements.

From these results, on concludes that the jitter and delay mismatches are restricted to relatively small values – reaching its maximum (12.4ns) at turn-off transition. Also, it should be noted that the obtained values include the control signal delay variations from the optic emitter as well.

To assess the gate driver's capability of quickly turning on and off a given semiconductor, the voltage rise and fall times when charging and discharging an RC circuit are measured. Figure 5.19 shows the results for several combinations of RC values.



a) *b)*

Figure 5. 19 – Gate driver voltage rise and fall times as a function of the resistance and capacitance load values. A 20-80% criteria is used for the time interval definitions.

Figure 5.19 indicates that the driver voltage response depends on the load RC variations and it increases linearly with τ. This supports the fact that the driver push-pull output stage might not limit the drain current rise/fall times in the power loop.

Concerning the gate driver parasitic inductance, it is measured to be 13.3nH from the gate-to-source points (see Figure 5.17). With regard to its power limit, the developed driver has been evaluated with an RC load ($r_{g,on} = r_{g,off} = 2.35\Omega$ and $C_{load} = 6.8nF$) up to 125kHz. At this point, the driving voltages +20/-5V are limited to +19.2/-4.3V and a maximum DC-DC power supply temperature of 46°C is observed. If higher switching frequencies are intended (or a higher number of chips in parallel is required), a 5W DC-DC converter might be needed.

5.6.3 Busbar

The interconnections of the CSI modules and other passive components are realized by means of a four-layer PCB planar busbar. The chosen dielectric material is FR4 (630µm in thickness) and all four conductive layers are Cu-based (210µm). On the top layer, the SMD protection components, gate drivers, power terminals and DC capacitors are mounted. Besides, this layer may be used as shielding, when it is connected to the ground. The subsequent layers 2, 3 and 4 are connected to the grid potentials *c*, *b* and *a*, respectively. On the bottom layer, ceramic decoupling capacitors are soldered as close as possible to the power modules. Then, C_{dec} arrangement is made identical to the one presented in § 4.5. To insure the connection between layers, when necessary, through-hole and blind vias are employed.

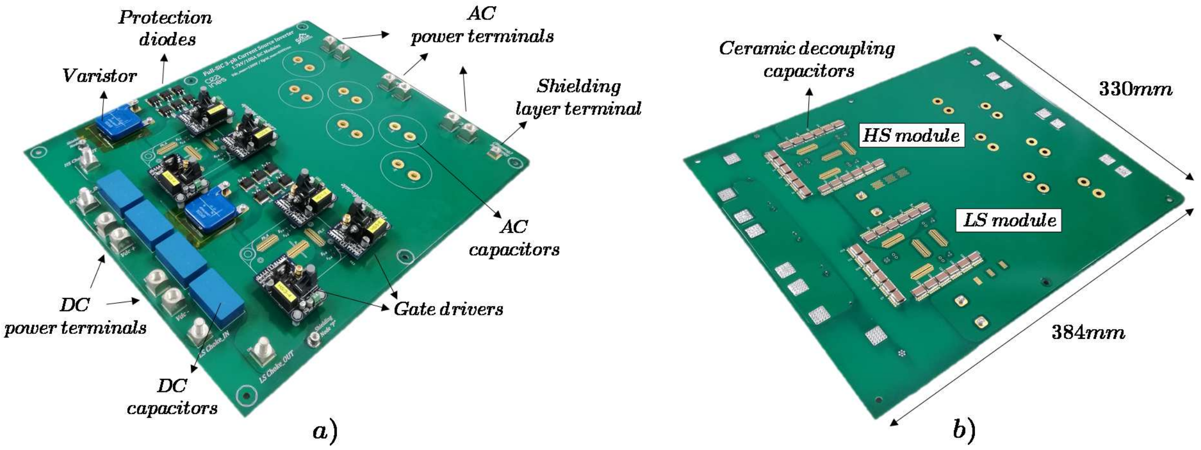


Figure 5. 20 – a) Top and b) bottom view of the developed four-layer PCB busbar.

5.6.4 Setup for Direct Measurement of Junction Temperatures

Knowing the semiconductors' junction temperatures is of great importance while characterizing power electronic systems. In the literature, several methods for T_j measurement are found [20], [21], as thermal radiation detectors (infrared cameras), pn-junction diffusion voltage measurement method (Vce(T)-method) and direct assessment using temperature sensors (e.g., thermocouples). Since the CSI modules are located under the busbar, the use of infrared cameras is not considered. Although widely employed in reliability tests [21], [22], the Vce(T)-method needs the converter to be shut down during a short period of time. This in turn makes its implementation more difficult from a practical point of view. In this work, the module's junction temperatures are directly assessed by placing temperature sensors in contact with the chips. Moreover, by using optic temperature sensors (OTG-F, range -40/250°C, from OpSens), isolation problems often related to the utilization of thermocouples are avoided. Having the information of T_j during switching operation brings the following advantages: *i)* safety of operation, since the evolution of T_j is monitored, *ii)* precise estimation of conduction losses can be done and *iii)* dissociation of switching and conduction losses can be carried out (if the overall semiconductor losses are known).

To place the temperature sensors on the chips, the module dielectric gel is removed. Then, the sensor tip is positioned in contact with the die (see Figure 5.21 (a)) and a thermal adhesive is used to attach the sensor on the semiconductor surface (Figure 5.21 (b)). Afterwards, the module is refilled again with the dielectric gel for operation at nominal voltage. Figure 5.21 (c) shows the heat sink overview with all eight temperature sensors. Thereby, two MOSFET and diodes from each module are monitored, namely $D_{1,2-HS}$, $M_{1,2-HS}$, $D_{5,6-LS}$ and $M_{5,6-LS}$.

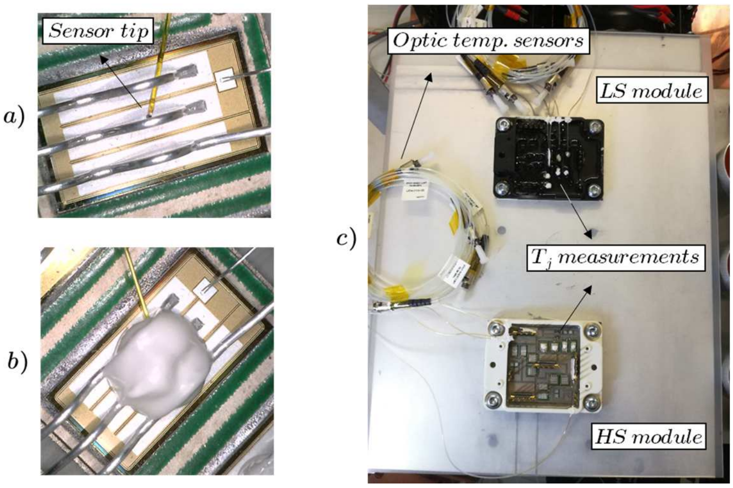


Figure 5. 21 – a) Positioning of the temperature sensor before attaching, b) attached temperature sensor and c) heat sink overview with all eight junction temperature sensors.

5.7 CSI Characterization

Figure 5.22 presents the block diagram of the experimental CSI test rig. Its main components are listed as follows: DC power supply (Electro-automatik 10x 15kW/1000V), three-phase 60kW full-SiC CSI prototype, three-phase resistive charge (Cudoint 250kW/690V), DSpace control platform with optic interface and measurement/monitoring equipment (oscilloscope Lecroy HDO8108A and power analyzer LMG670).

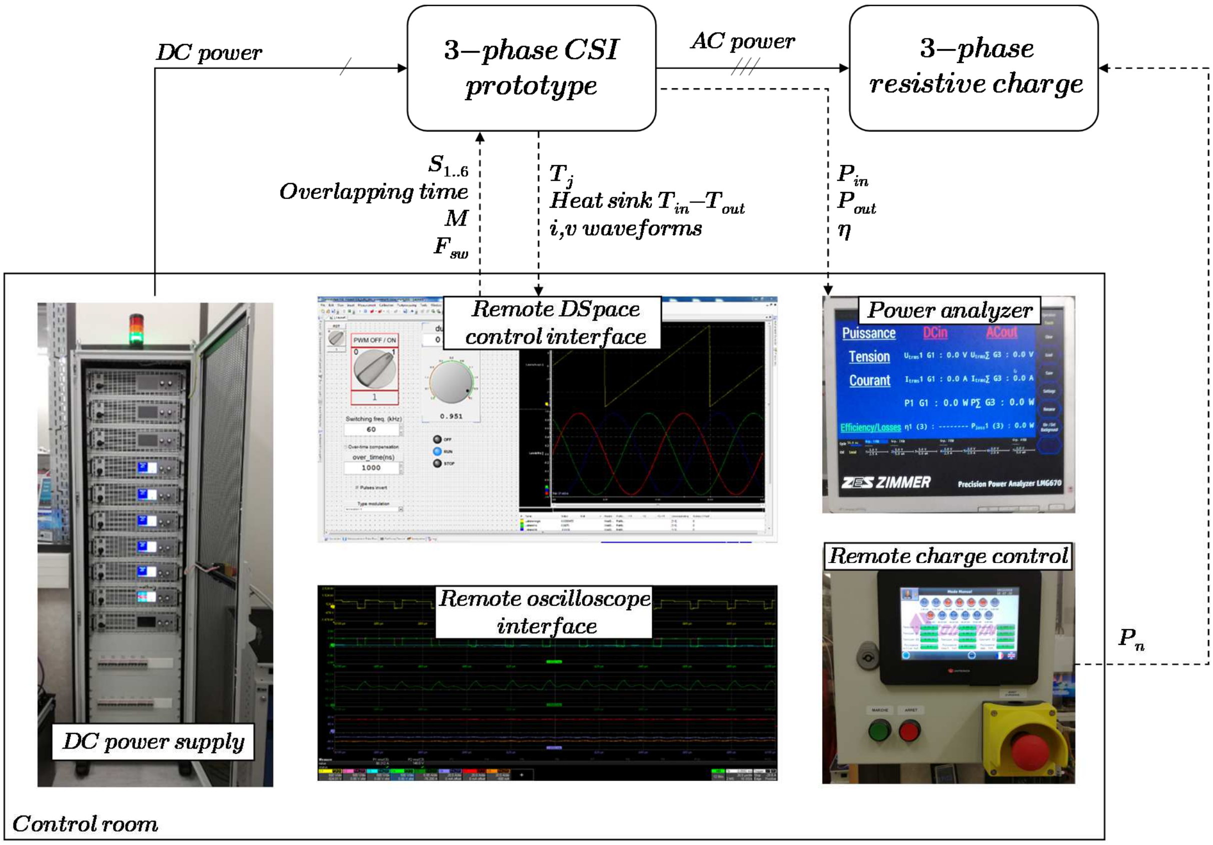


Figure 5. 22 – Experimental test rig block diagram description.

The 3D CAD model of the developed CSI prototype is presented in Figure 5.23 (a). After assembled on a metallic support, the power stack dimensions are 33x56x16cm. In order to measure an average value of the heat sink airflow output temperature, a mixer chamber is implemented (see Figure 5.23 (b)). The positioning of temperature sensors (T_{in} and T_{out}) is also represented in Figure 5.23. Hence, the in/out heat sink temperature difference is computed as $\Delta T_{sink} = T_{out} - T_{in}$.

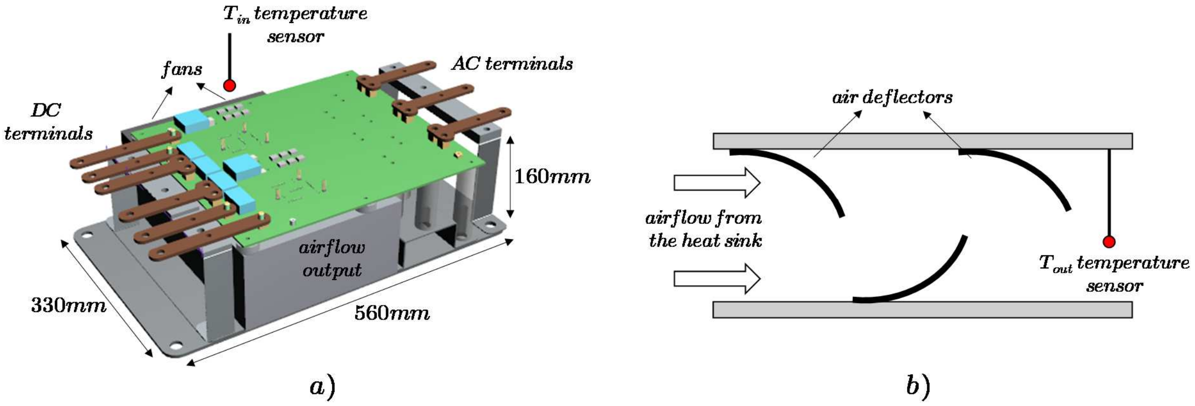


Figure 5. 23 – a) 3D CAD model of the CSI prototype and b) airflow mixer chamber with temperature sensors positioning.

In Figure 5.24 is depicted the CSI prototype with the apparatus for calorimetric characterization. The details of the employed measurement equipment are given in Table 5.10.

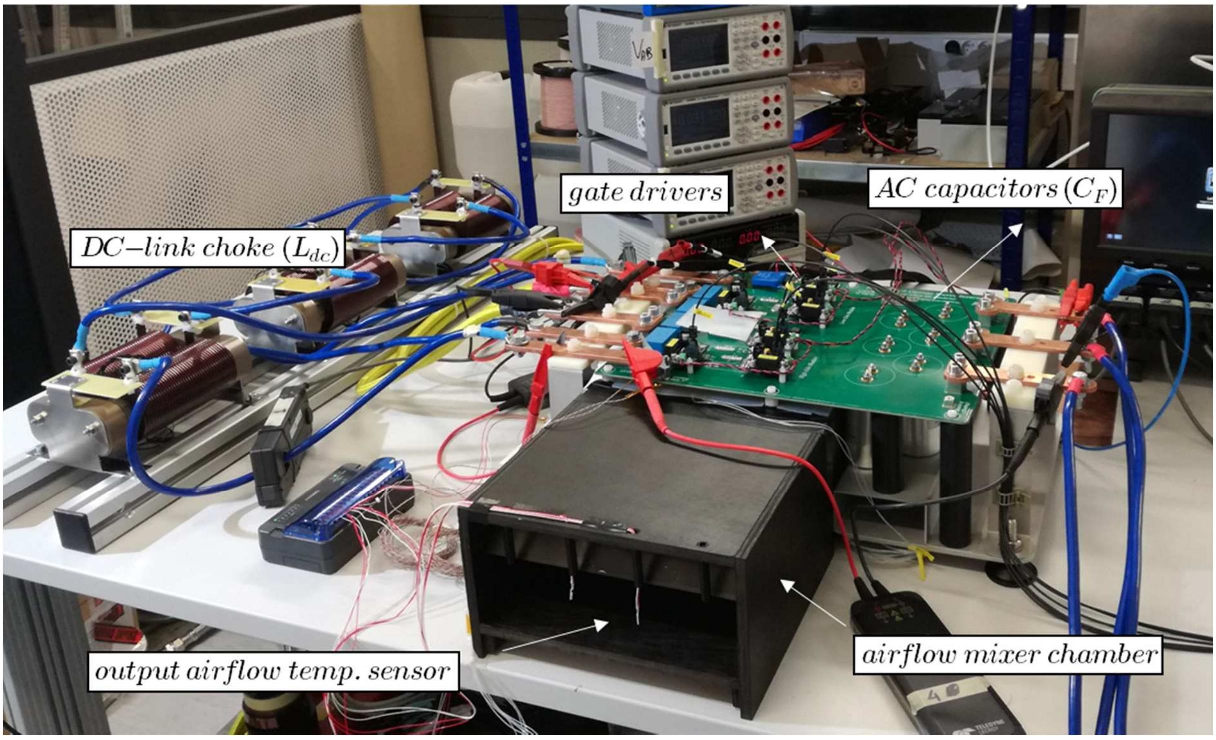


Figure 5. 24 – Assembled CSI prototype. To keep a constant DC current ripple while varying F_{sw}, three coupled DC-link chokes are available, allowing several L_{dc} values to be obtained. The AC filter inductor (L_{ac}) is not present in the image.

Table 5. 10 – Characteristic of the employed measurement equipment.

Measurement	Characteristics
Voltage	High-voltage differential probe Lecroy HVD 3106 (1500V/120MHz)
Current	AC/DC Current probe Lecroy CP150 (150A/10MHz)
Efficiency (electrical method)	Precision power analyzer - Zimmer LMG670 DC voltage (L60-CH-A1), AC voltages (3x L60-CH-C1) and DC/AC currents (PTC200)
Junction temperature	Optic sensors OpSens (OTG-F, temp. range -40/250°C)
Heat sink in/out temperature	PT100 – classe A/4 wires * Labfacility (XF-935-FAR)
Decoupling ceramic capacitor temperature	Thermocouple type T *

* Data acquired with Hioki data logger unit LR8511.

5.7.1 Heat Sink Characterization for Calorimetric Semiconductor Losses Determination

Before proceeding to tests under switching operation, the heat sink thermal characteristic (*dissipated losses vs.* ΔT_{sink}) must be obtained. Thereby, a preliminary DC current test similar to the one presented in § 5.3.3 is carried out. The semiconductor junction temperatures are obtained from the optic sensor measurements, where all the HS MOSFETs and diodes are assumed to have an average temperature of $\bar{T}_{j,M-HS} = (T_{j,M1-HS} + T_{j,M2-HS})/2$ and $\bar{T}_{j,D-HS} = (T_{j,D1-HS} + T_{j,D2-HS})/2$, respectively. Analogously, for the LS module, one has $\bar{T}_{j,M-LS} = (T_{j,M5-LS} + T_{j,M6-LS})/2$ and $\bar{T}_{j,D-LS} = (T_{j,D5-LS} + T_{j,D6-LS})/2$. As discussed in § 5.3.3 (cf. Table 5.4), from a losses distribution point of view, these are reasonable assumptions to be made. Then, the dissipated power is estimated based on the PSIM conduction losses model depicted in Figure 5.9. The heat sink characteristic curve is presented in Figure 5.25. The points where $\Delta T_{sink} < 6°C$ are not taken into account due to incertitude reasons.

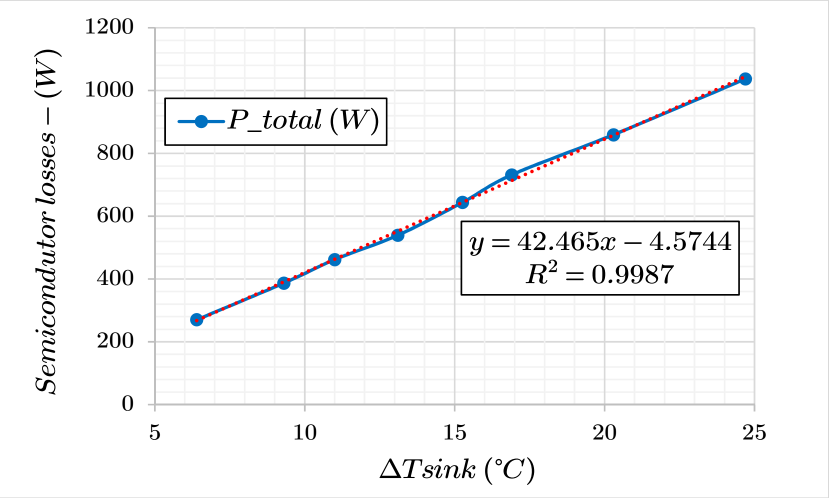


Figure 5. 25 – Heat sink characteristic curve.

Hence, a first order equation $P_{losses} = 42.465 \cdot \Delta T_{sink} - 4.5744$ is fitted to the experimental data. This being defined, the overall semiconductor losses ($P_{sw} + P_{cond}$) can be precisely obtained, as far as a significant input/output heat sink temperature difference exists (e.g., $\Delta T_{sink} > 6°C$).

5.7.2 Waveforms at Nominal Switching Operation

Figure 5.26 and 5.27 presents the CSI waveforms under identical operation conditions for two distinct modulation strategies: Mod1 (discussed in § 4.3.2) and Mod2, respectively. Mod2 is a tri-state modulation strategy that has been proposed in [2]. Its main advantage is the reduced CM voltage, which is achieved by accordingly choosing the zero-state vectors to be used per sector.

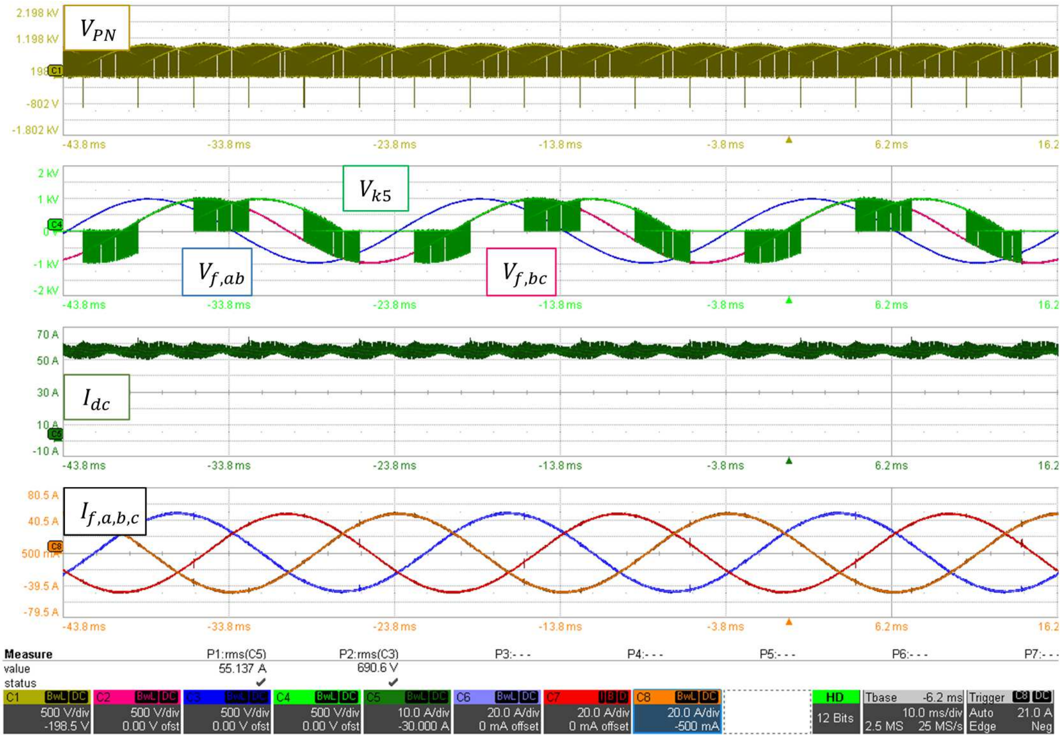


Figure 5. 26 – CSI waveforms while feeding a three-phase resistive charge in open-loop configuration. V_{k5} is the switching voltage. Test conditions: Modulation technique Mod1, $V_{dc} = 735V$, $V_{f,l-l} = 690V$, $P_{in} = 40kW$, $F_{sw} = 15kHz$, overlapping time $t_o = 1\mu s$ and $r_{g,on} = r_{g,off} = 10\Omega$.

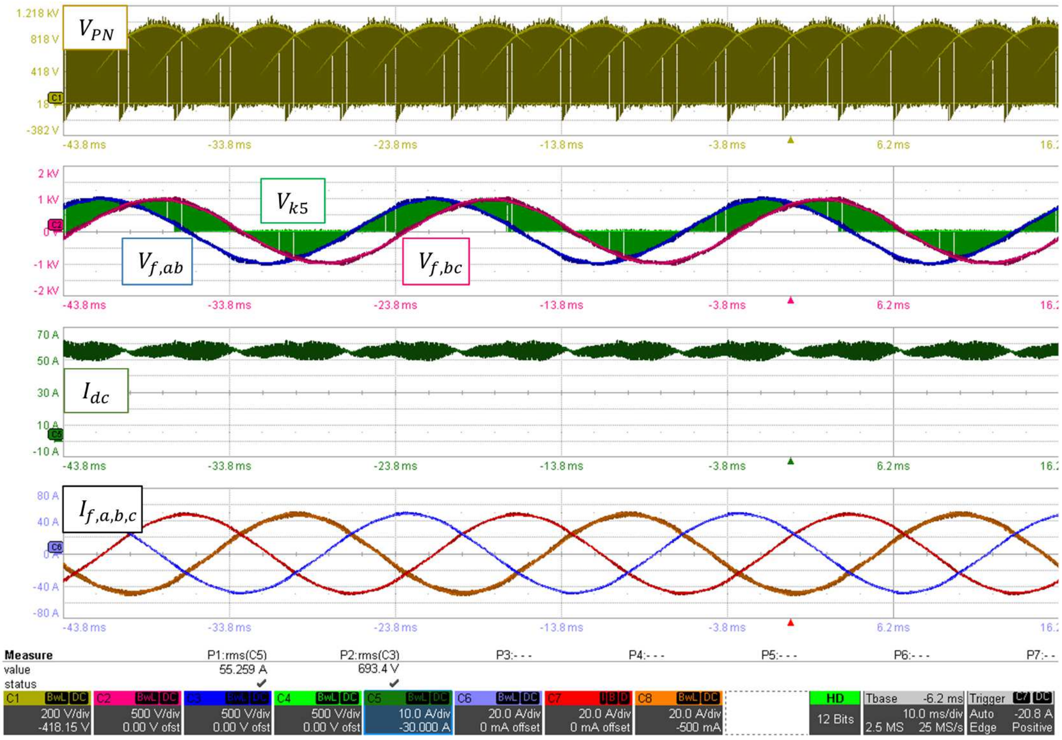


Figure 5. 27 – CSI waveforms while feeding a three-phase resistive charge in open-loop configuration. V_{k5} is the switching voltage. Test conditions: Modulation technique Mod2, $V_{dc} = 735V$, $V_{f,l-l} = 690V$, $P_{in} = 40kW$, $F_{sw} = 15kHz$, overlapping time $t_o = 1\mu s$ and $r_{g,on} = r_{g,off} = 10\Omega$.

For both modulation techniques, sinusoidal AC voltages and currents are produced. The main difference between the presented waveforms concerns the switch blocking voltage (V_{k5}). Nevertheless, while carrying out experiments employing Mod1 at nominal power, the generated CSI CM currents were responsible for shutting down the DC power supply. For that reason, only Mod2 has been employed in the following experiments.

Another issue encountered during tests is related to the inverter operation feeding a resistive load. As an example, Figure 5.28 presents the CSI voltage waveforms at 9kW.

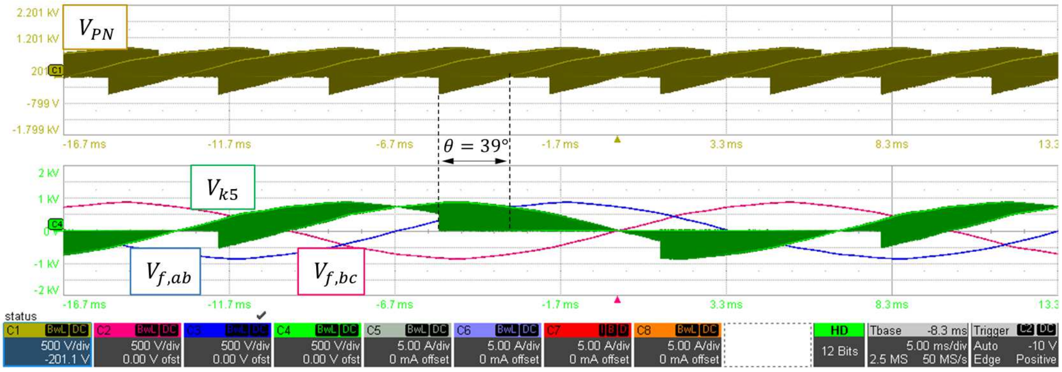


Figure 5. 28 – Voltage waveforms for open-loop operation at light-load condition. Test conditions: Mod2, $V_{dc} = 530V$, $V_{f,l-l} = 630V$, $P_{in} = 9kW$, overlapping time $t_o = 1\mu s$ and $F_{sw} = 40kHz$.

When operating in combination with a resistive load, the AC displacement power factor (DPF) angle θ seen by the three-phase bridge (i.e., at points *a*, *b* and *c*) depends on the load level condition. At full-load, θ tends to zero and the semiconductors operate at unity $cos\theta$ (as is the case in Figure 5.27). As far as the CSI load level decreases, θ tends to a value that is only imposed by the AC filter. In Figure 5.28, at 9kW, $\theta = 39°$. Hence, the semiconductor losses evaluation cannot be carried out at unity $cos\theta$ for the entire CSI power range. Note that this issue cannot be solved implementing a control loop while keeping a passive load – grid-connected operation would be required.

5.7.3 Influence of Switching Frequency on Semiconductor Losses

To verify the impact of switching frequency on the CSI switching losses, the inverter is operated from 15kHz to 60kHz for a given DC current RMS value ($I_{dc} = 55A$) and AC grid voltage ($V_{f,l-l} = 690V$). To minimize the impact of the DC current ripple on semiconductor losses, the DC-link choke configuration is modified from one F_{sw} value to another. Furthermore, in order to reach the thermal steady-state condition, a time interval of 25 minutes for each point is considered. Then, the total semiconductor losses ($P_{total}(F_{sw})$) are measured employing the methodology of § 5.7.1. Finally, switching losses are estimated with $P_{sw}(F_{sw}) = P_{total}(F_{sw}) - P_{cond}(I_{dc}, T_j)$. The results are presented in Figure 5.29.

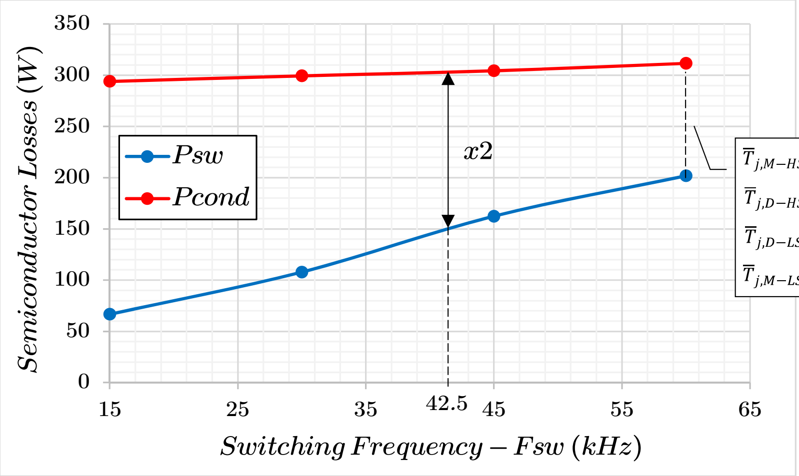


Figure 5. 29 – Switching and conduction losses vs. switching frequency. Test conditions: Mod2, $M = 0.9$, $V_{f,l-l} = 690V$, $I_{dc} = 55A$, overlapping time $t_o = 1\mu s$ and $r_{g,on} = r_{g,off} = 10\Omega$.

From this results, the low impact of switching frequency on switching losses is remarkable, since $P_{sw} = 50\% \cdot P_{cond}$ @42.5kHz and $P_{sw} = P_{cond}$ @91kHz (when neglecting the influence of increasing T_j on P_{cond}). Furthermore, the HS MOSFET junction temperature variation is within 17°C ($\overline{T}_{j,M-HS}$ @60kHz – $\overline{T}_{j,M-HS}$ @15kHz). Note here that $r_{g,on} = r_{g,off} = 10\Omega$, which is a relatively large value. As discussed in § 4.5.1, passing from $r_{g,on} = 10\Omega$ to 2.2Ω allows the switching energy to be capped by a factor of two at 1kV/100A.

5.7.4 Efficiency Measurements

The CSI overall and semiconductor efficiencies, namely η and η_{semi} are presented in Figure 5.30 for $F_{sw} = 60kHz$ and two different input voltages. η is measured using the precision power analyzer described in Table 5.10 and η_{semi} is obtained through the calorimetric method. The DC-link choke value is $L_{dc} = 181\mu H$. The respective junction temperatures are shown in Figure 5.31 for $V_{dc} = 665V$.

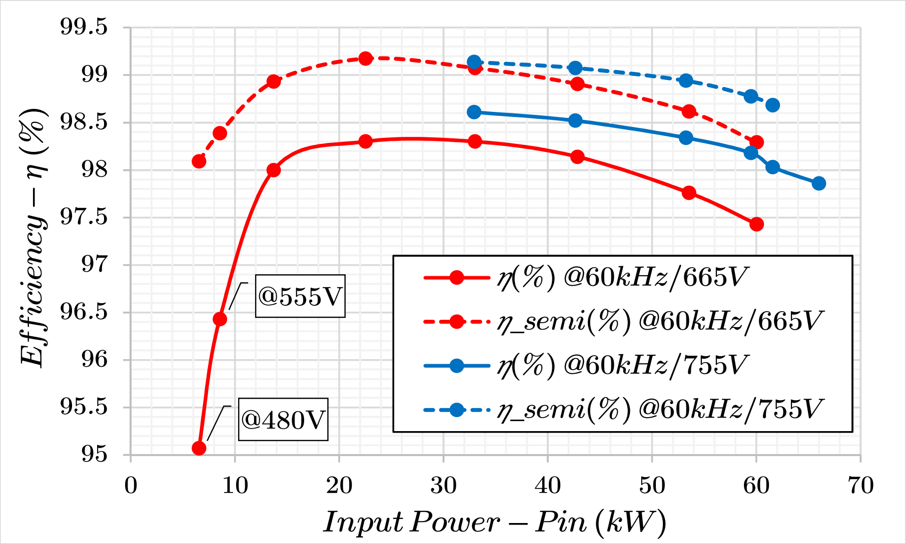


Figure 5. 30 – Overall CSI efficiency (from electrical measurement) and semiconductor efficiency (from calorimetric measurement). Test conditions: Mod2, $V_{f,l-l} = 690V$, $F_{sw} = 60kHz$, overlapping time $t_o = 1\mu s$ and $r_{g,on} = 2 \cdot r_{g,off} = 2.2\Omega$.

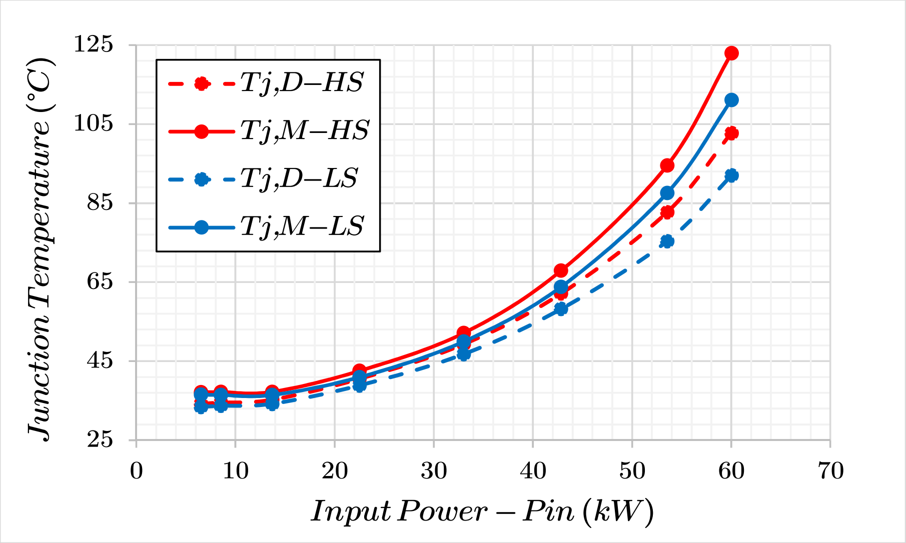


Figure 5. 31 – Measured junction temperatures for the case $V_{dc} = 665V$. Test conditions: same as in Figure 5.30.

Concerning the inverter efficiency curve for $V_{dc} = 665V$, the two points where $P_{in} < 20kW$ are taken with $V_{dc} = 480V$ and $555V$. For that reason, the CSI European Efficiency cannot be calculated. To be able to operate with a constant input voltage for the entire power range, the AC voltages must be imposed, i.e., grid-connected operation with the associated control loop would be required. As discussed in § 5.3.2, the junction temperatures follow an exponential behavior and the inverter maximum power is limited by the HS MOSFETs. Nevertheless, at 60kW, all devices' junction temperatures do not exceed 125°C. With regard to the semiconductor efficiency, it reaches its maximum value (99.2%) around $P_n/3$. On the other hand, the maximum measured value of the inverter efficiency is 98.6% when $V_{dc} = 755V$.

The distribution of losses is presented in Figure 5.32 for both DC input voltages at 60kW and 60kHz.

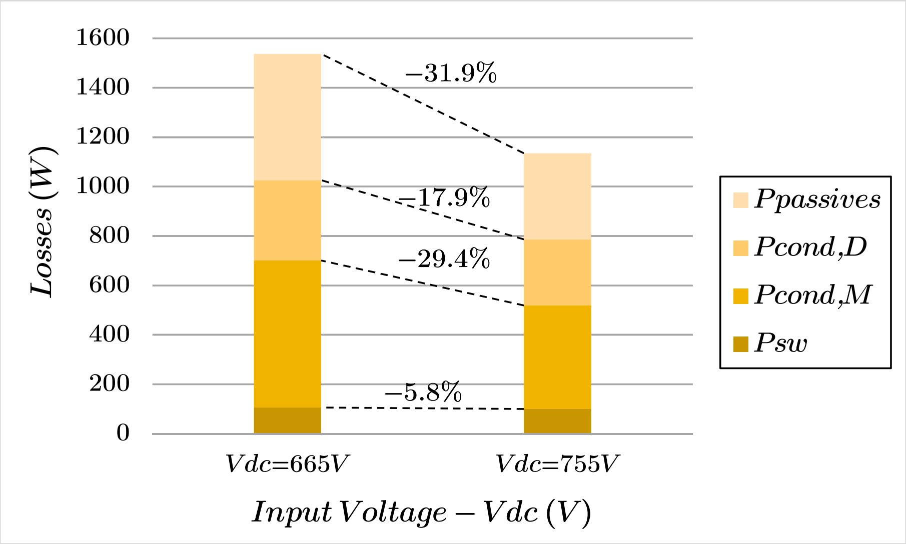


Figure 5. 32 – Overall losses distribution for two different input voltages at 60kW and 60kHz. Test conditions: same as in Figure 5.30.

Here, the advantage of a higher DC voltage level can be seen. When passing from $V_{dc} = 665V$ to $755V$, the overall losses are reduced by 30%, leading to an efficiency gain of 0.8%. The major contributors to this are the losses of passive components (mainly from the DC-link choke) and MOSFET conduction losses. The diodes' conduction losses are less impacted by the current reduction due to their threshold voltage (V_0). With regard to the switching losses, they represent only 7% of the overall losses at $V_{dc} = 665V$, having then minor influence on the CSI efficiency in both DC input voltage cases.

5.8 Summary and Conclusion

In this chapter, focus has been given to the CSI experimental validation at nominal power. From the main design guidelines, a 60kW inverter prototype was built, allowing to evaluate the CSI in a large range of switching frequency (up to 60kHz). Thanks to the employed characterization methodology, the dissociation of conduction and switching losses was performed.

From a thermal management point of view, the employed arrangement of modules on the heat sink has led to considerable junction temperatures unbalance between the HS and LS modules (reaching 14°C in the worst case). As a consequence, the CSI power limit was dictated by the HS devices, while the LS semiconductors were considerably less thermally stressed. In a future realization, an alternative converter layout should be implemented, to better homogenize both HS and LS junction temperatures and improve the CSI power limit. Considering the adopted arrangement of dies within the packaging, the L-shaped groups of dies have shown the worst junction temperature unbalances. To improve this issue, in future works, the possibility of implementing only in-line group of dies should be considered. Moreover, a supplementary design modification would involve a different arrangement of dies, i.e., MOS-diode-MOS-diode instead of MOS-MOS-diode-diode.

As seen throughout this chapter, semiconductor conduction losses (P_{cond}) represent the main contributor to the CSI overall losses even at relatively high switching frequencies, i.e., 60kHz. In order to cap P_{cond} for a given power, the CSI should be designed to operate with the highest admissible grid and PV voltage levels. An alternative solution is to simply increase the semiconductor chip area, with the drawback of increasing the C_{oss}–related switching losses term as well. To cope with this problem, the paralleling of n elementary CSI blocks could be implemented [23]. Figure 5.33 depicts the three-phase CSI with two blocks in parallel.

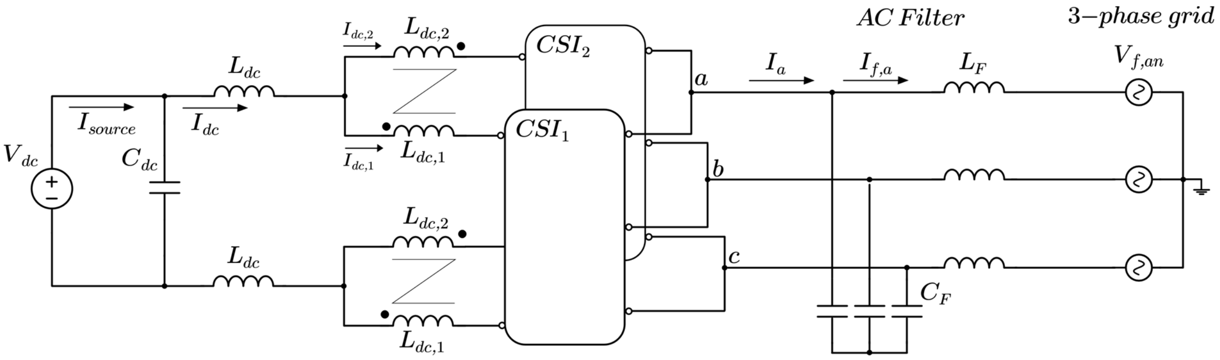


Figure 5. 33 – Three-phase five-level CSI with the coupled interphase inductors.

Making use of interleaved converter properties, the AC current spectrum can be improved (shifting the carrier frequency by a factor of n), limiting then grid filtering efforts. Additionally, as pointed out in [23], it gives the possibility to the designer to inversely couple the interphase DC-link inductors ($L_{dc,1,2}$) of the n CSIs, which in turn allows the average DC flux to be cancelled in the resulting magnetic element. The remaining DC chokes (L_{dc}) operate at $n \cdot F_{sw}$ and they insure a limited DC current ripple. This might sensibly reduce the overall DC inductor volume, weight (bulkiest element in the standard CSI) and costs, since

L_{dc} and $L_{dc,1,2}$ can be separately optimized taking into account their distinct operating conditions.

Concerning the CSI efficiency measurements, the developed module has shown the capability of operating efficiently at 60kHz, since $\eta_{semi} > 99\%$ for both input voltage levels (665V and 755V). The maximum inverter overall efficiency was measured to be $\eta > 98.5\%$ for $V_{dc} = 755V$. Finally, the CSI aptitude of operating at higher switching frequencies has been experimentally validated, indicating that a fair compromise between power density and efficiency, i.e., definition of $F_{sw,CSI}$, might be considerably higher than that for voltage-source based inverters. This conclusion is in agreement with the results obtained from the theoretical efficiency comparison carried out in § 5.5, where the VSI+boost semiconductor efficiency approaches that of the CSI when $F_{sw,VSI+boost} = F_{sw,CSI}/2$.

5.9 References

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Chapter 6

Conclusions and Future Work

In this dissertation, the key aspects concerning the implementation of a SiC-based three-phase Current Source Inverter in photovoltaic systems have been investigated. In this final chapter, the main research achievements and conclusions are summarized within three research topics. Also, possible future research areas are identified and discussed accordingly.

6.1 Power Integration for CSI Applications

The main related achievements are summarized as follows:

- Design and realization of the 1.7kV full-SiC voltage bidirectional power module. This is the first work reported in the literature, which investigates the advantages and challenges associated with the design of a SiC module in an industrial version for CSI applications;
- Detailed experimental investigation correlating aspects of the module layout design and the obtained thermal performance; and
- Theoretical evaluation of the maximum admissible CSI operating conditions, i.e., input current, ambient temperature and switching frequency, in order to avoid semiconductor thermal runaway.

In Chapter 4, the design and realization of a novel SiC power module dedicated to CSI applications have been carried out. Due to their specific operating constraints, the power integration for current-source based topologies appeared to be considerably more complex than that of voltage-source based converters. Since the CSI commutation process involves the devices of three different legs, attention must be payed to the minimization of all switching cell stray inductances while keeping them well balanced. To achieve these objectives, the proposed solution of this work consisted in designing two separate modules, namely high- and low-side modules, and disposing the semiconductor dies per groups, which were in turn symmetrically placed on the module's substrate. In doing so, an equivalent stray inductance of approximately 15nH was obtained for all switching cells. Although systematically studied in Chapter 4, specifications concerning the packaging Common Mode (CM) parasitics were not taken into account during the module's design phase. For this reason, in an eventually module redesign, the CM capacitors between points P and N to the ground should be taken as variables to be minimized.

In Chapter 5, the developed module's thermal performance has been experimentally investigated, showing a non-negligible asymmetry in terms of junction temperatures between the chips. Considering the actual design, the

L-shaped groups of dies have shown the worst junction temperature unbalances. To improve this issue, in future works, the possibility of implementing only in-line group of dies should be considered. Moreover, a supplementary design modification to homogenize and alleviate the electro-thermal coupling between adjacent MOSFETs would involve an alternate arrangement of chips, i.e., MOS-diode-MOS-diode instead of MOS-MOS-diode-diode.

For a future implementation of the CSI module in a commercial PV inverter, reliability studies should be carried out concerning the following aspects: *i)* the CSI junction temperature profile during the day with regard to load (solar irradiance) variations. As experimentally verified in Chapter 5 (cf. Figure 5.32), conduction losses represent up to 85% of MOSFET power losses. Thereby, the CSI junction temperature profile might be sensibly different from that of standard VSIs [1], whose switching losses contribution to overall losses is much more relevant. The impact of such different losses distribution constraints on inverter lifetime should then be investigated; *ii)* in the literature, SiC-based power modules employing standard soldering alloys and materials are associated to have reduced cycling capability [2], [3]. Due to the high SiC stiffness, some studies indicate, for a given packaging technology, that the SiC-based module lifetime is reduced to 1/3 of its equivalent Si-based module [3] .

Finally, as discussed in § 4.3.4, for the power range of this work and considering a balanced switching cell design in terms of parasitics, the presented industrial solution seems to have reached the limits of the employed wire-bonding packaging technology. Thus, a possible research field to improve the existent module performance would involve 3D-packaging solutions. Having the possibility to make interconnections in the z-direction, a balanced design might be more easily achieved, bonding wires could be avoided and thermal resistances improved.

6.2 Dynamic Characterization of 1.7kV SiC Devices

The main related achievements are summarized as follows:

- Development and evaluation of a low-intrusive wide-bandwidth current measurement sensor, the Double-stage Current Transformer (DSCT); and
- Complete dynamic characterization of the developed CSI module, through the double-pulse test (DPT) technique.

The complete dynamic characterization of the CSI module has been presented in Chapter 4, employing the DPT technique. In order to measure the switching transient current waveforms with minimum switching loop insertion inductance, a new current sensor, namely DSCT, has been developed. The DSCT is composed of a high-frequency (4F1 material) flat ferrite core having the form of the module's electrodes. These features insure the DSCT implementation with minimum stray inductance while having a high enough bandwidth. To assess the DSCT performance, a comparative study with two other state-of-the-art current sensors, namely coaxial shunt and active shunt, has been conducted. Contrarily to the coaxial shunt, which suffers from an amplified ringing and overshoot as well as inaccurate/distorted response, the DSCT had shown good dynamic response (together with the active shunt).

Concerning the adopted switching speed characterization procedure, it had shown to be an effective predesign step, allowing the designer to identify, in an early project phase, the tradeoffs and no-go zones in terms of *dv/dt* and switching losses and adequately choose the gate resistance values.

6.3 Inverter Level

The main related achievements are summarized as follows:

- Design, realization and characterization of the 60kW three-phase SiC-based CSI prototype;
- Implementation of a calorimetric method for semiconductor losses measurement;
- Implementation of a measurement setup to directly assess the semiconductors' junction temperatures, allowing the dissociation of conduction and switching losses; and
- Theoretical evaluation and comparison concerning the following aspects: *i)* CSI topological variations to reduce conduction losses, *ii)* efficiency estimation of standard two-stage voltage-source based structures and the CSI and *iii)* CSI operation with different grid voltage levels.

In order to reduce conduction losses, four CSI topological variations, namely, standard CSI, CSI7, Delta-type CSI and 4qCSI, have been studied and compared in Chapter 3, taking into account PV application requirements. The main conclusions can be summarized as follows: *i)* the CSI7 switch configuration had not shown to be a compelling solution as far as low modulation indexes (e.g., $M<0.7$) are employed, i.e., for high voltage boost ratios; *ii)* the 4qCSI variation becomes more interesting, from a η_{euro} point of view, when a higher number of paralleled chips are implemented. Nevertheless, the maximum allowed input power is reduced, due to the increased electro-thermal coupling behavior of MOSFETs and *iii)* the Delta-type CSI had shown to be a very interesting solution in terms of cost-effectiveness, if the required inverter operation is restricted to $\cos(\varphi) > 0.5$. Hence, thanks to its cost-effectiveness with respect to the considered PV voltage levels, capability of operating within a wide range of $cos(\varphi)$, reduced number of gate driver units and simplicity, the standard CSI with six controllable switches has been selected to be the focus of the present work.

In Chapter 5, focus has been given to the CSI experimental validation at nominal power. For this purpose, a 60kW inverter prototype was built. From the experimental results, the inverter capability to operate efficiently at relatively high switching frequencies ($\eta_{CSI,max} > 98.5\%$ $@F_{sw} = 60kHz$) has been confirmed. Nonetheless, conduction losses still represent the main contributor to the CSI overall losses – from Figure 5.32, at 60kW, P_{cond} accounts for 58% of the overall inverter losses. For that reason, to cap P_{cond} for a given power, the CSI should be designed to operate with the highest admissible grid and PV voltage levels.

Concerning the theoretical comparison carried out in § 5.5, between two-stage voltage-source based topologies and the CSI, it was possible to see that, for equivalent semiconductor European Efficiency levels, the CSI can be operated at considerably higher switching frequencies. Besides that, the two-stage voltage converter efficiency approaches that of the CSI when system complexity and/or additional chip area are implemented. On the other hand, even with relatively high switching frequency operation, the bulkiest CSI element is the DC-link choke. As discussed in § 5.8, the paralleling of CSI blocks in interleaved operation could cope with this problem, reducing the volume of the overall DC-inductors without increasing switching losses.

Finally, further research effort would be required to cope with the DC current (I_{dc}) interruption issue, which can occur in two distinct situations: *i)* scheduled inverter shut-down (discussed in § 3.2.2). In this case, if the PV string is properly designed with regard to its open-circuit voltage (V_{oc}), the CSI control loop is capable of bringing the operating point to $(V_{dc}, I_{dc}) \cong (V_{oc}, 0)$ and safely open all switches. However, for any reason, $V_{dc} \cong V_{oc}$ cannot be reached (cf. Figure 3.5), an external circuit (e.g., crowbar type) should clamp the DC-link choke before opening the CSI switches; otherwise, an abrupt current interruption should be considered together with the implementation of voltage limiting devices (e.g., Metal Oxide Varistors (MOV)) sized to absorb – only one time – the energy $E_{MOV} = 0.5(2L_{dc})I_{dc}^2$. *ii)* DC current interruption due to operating fault condition (discussed in § 5.6.1). In such event, the control loop time constant is not short enough to limit overvoltages, whose *dv/dt* rate is uniquely limited by the CSI parasitic capacitances (C_{oss}, C_{Ldc}, C_{CM} and etc). As a consequence, a practically instant reaction is necessary. This might be achieved by implementing a hybrid protection solution consisting of a crowbar in combination with a diode bridge and MOV, as presented in § 5.6.1. Given that, the MOV could be designed to limit the initial overvoltage while a crowbar circuit is turned-on.

During experimental tests with the 60kW CSI prototype, problems with DC-current interruption were encountered. Since any overvoltage detection circuit with feedback action was employed, the DC-link choke was kept being charged through the CSI switches during fault condition (probably due to a gate driver malfunction). This in turn had led to the protection circuit destruction, due to its continuous power dissipation. From these experiences, the need for a detection circuit with fast feedback action to the crowbar and/or CSI switches becomes evident and should be implemented in future realizations.

6.4 References

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Appendices

Appendix I – On-state Characteristic Fitting Constants for the employed SiC devices

The following fitting constants are used in Eq. 3.20 to describe the on-state resistance characteristic for the 1.7kV SiC MOSFET CPM2-1700-0045B:

$$\begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \\ a_5 \\ a_6 \\ a_7 \\ a_8 \\ a_9 \end{bmatrix} = \begin{bmatrix} 29.72 \\ 0.1574 \\ 0.2114 \\ 0.001012 \\ -0.001821 \\ 0.001462 \\ 1.318 \cdot 10^{-5} \\ 7.206 \cdot 10^{-6} \\ -4.044 \cdot 10^{-6} \end{bmatrix} \tag{I.38}$$

Figure I.1 presents a comparison of the MOSFET $R_{ds,on}$ fitted equation with experimental data from manufacturer's datasheet.

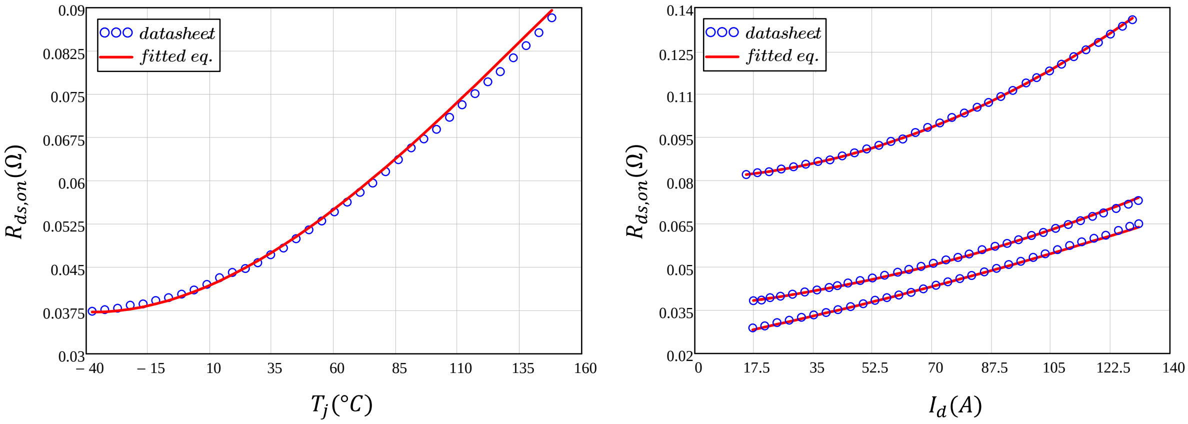


Figure I. 1 – Curve fitting of on-state resistance characteristic for the 1.7kV SiC MOSFET CPM2-1700-0045B: $R_{ds,on} = f(T_j)$ $@I_d = 50A; V_{gs} = 20V$ (left) and $R_{ds,on} = f(I_d)$ $@T_j = (150, 25, -40)°C$; $V_{gs} = 20V$ (right).

The following fitting constants are used in Eq. 3.22 to described the forward characteristic of the 1.7kV SiC diode CPW5-1700-Z050B :

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \\ b_5 \end{bmatrix} = \begin{bmatrix} 4 \cdot 10^{-7} \\ 7 \cdot 10^{-5} \\ 0.0116 \\ -0.0013 \\ 0.9653 \end{bmatrix} \tag{I.39}$$

Figure I.2 presents a comparison of the fitted equation for the diode forward behavior with experimental data from manufacturer's datasheet.

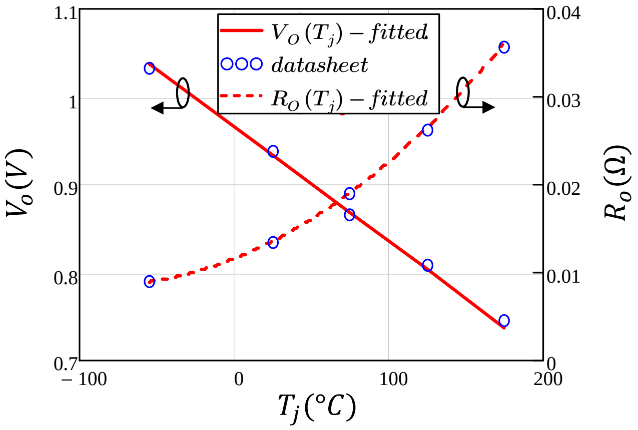
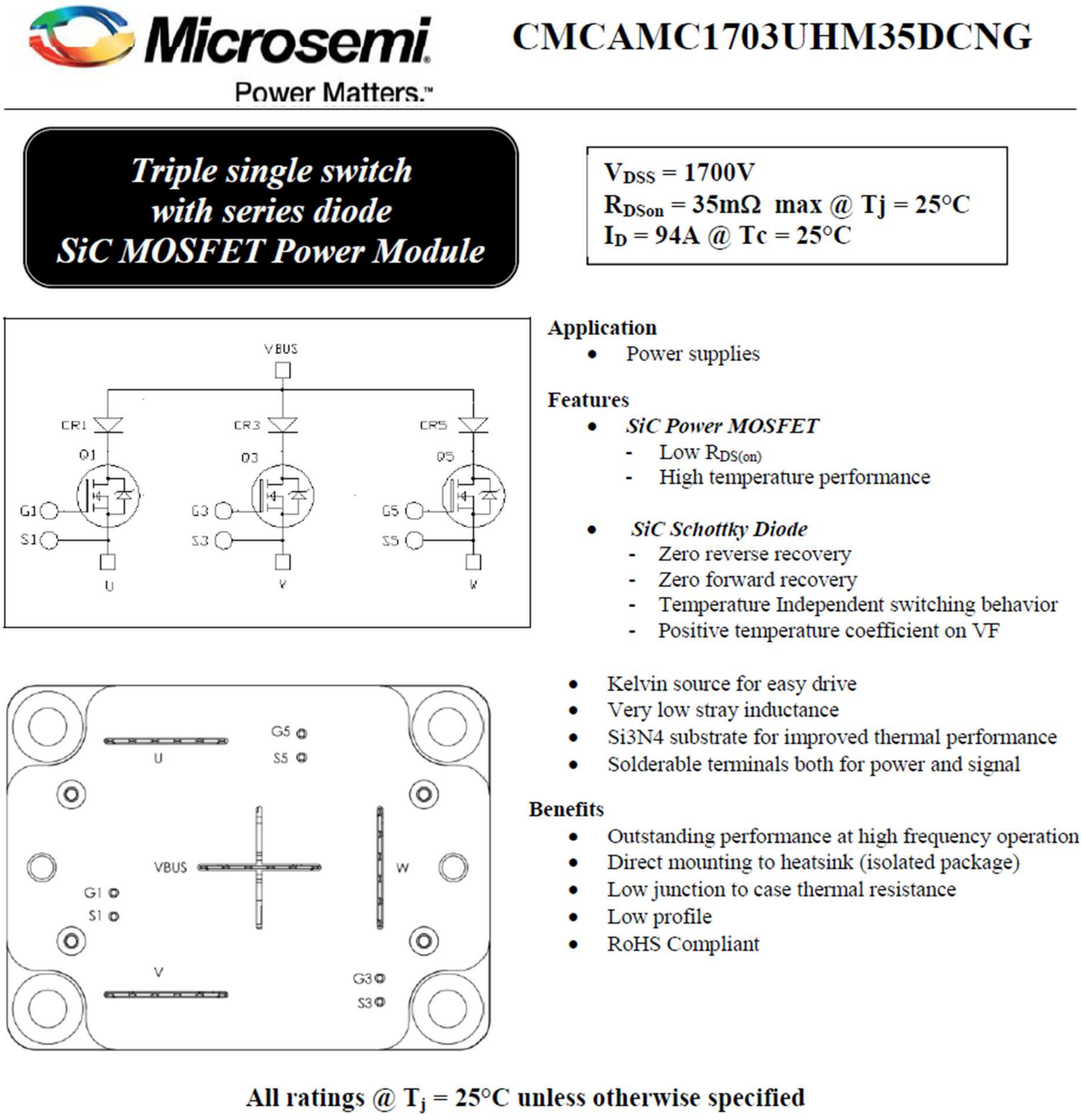


Figure I. 2 – Curve fitting of forward characteristic for the 1.7kV SiC Merged pin Schottky Diode CPW5-1700-Z050B.

Appendix II – Datasheet of the 1.7kV Full-SiC CSI Modules

In this appendix are presented the complete datasheet of the developed full-SiC 1.7kV CSI modules.

a) HIGH-SIDE module



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CMCAMC1703UHM35DCNG

Triple single switch
with series diode
SiC MOSFET Power Module

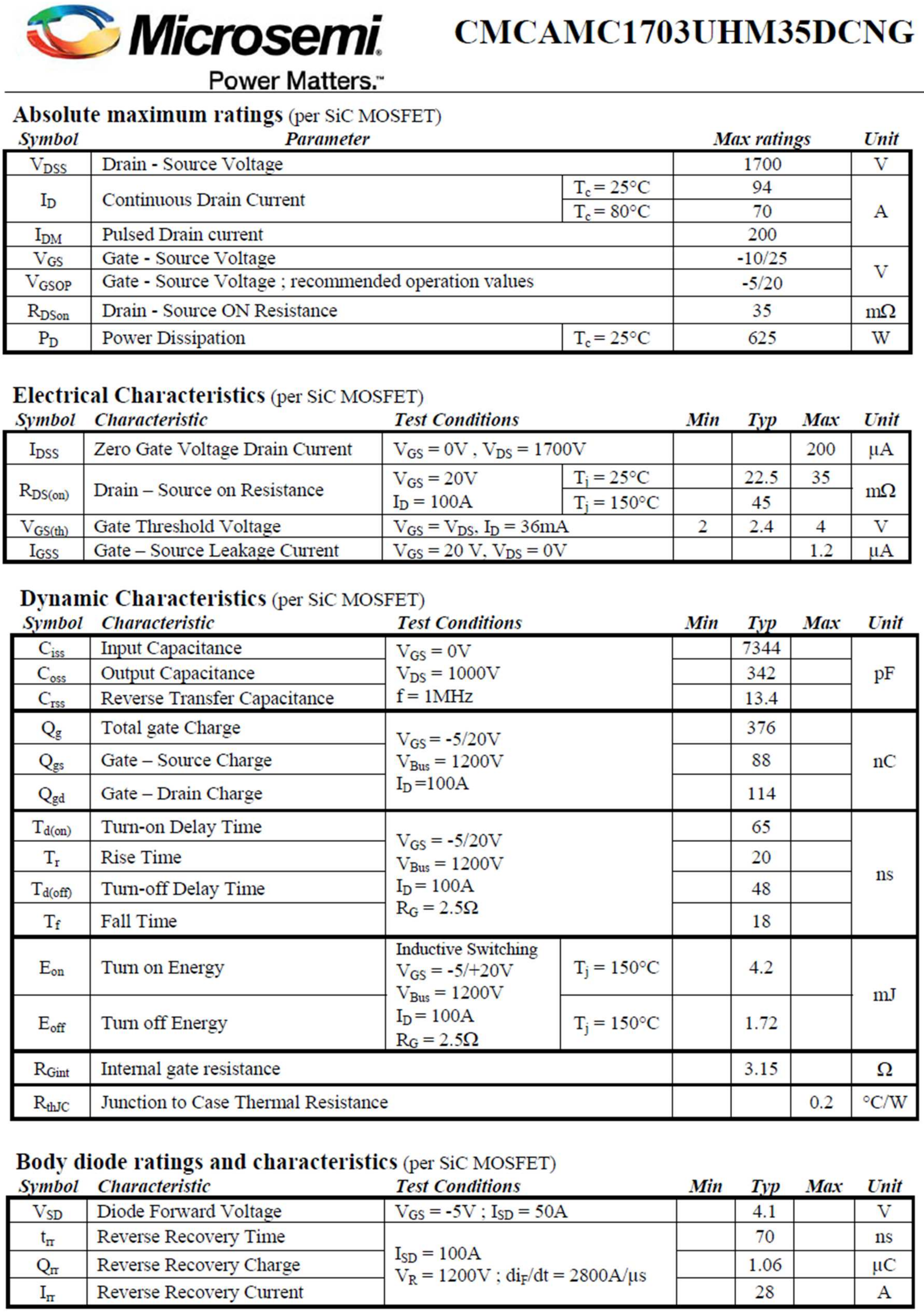
V_{DSS} = 1700V
R_{DSon} = 35mΩ max @ Tj = 25°C
I_D = 94A @ Tc = 25°C

Application
- Power supplies

Features
- ***SiC Power MOSFET***
  - Low $R_{DS(on)}$
  - High temperature performance
- ***SiC Schottky Diode***
  - Zero reverse recovery
  - Zero forward recovery
  - Temperature Independent switching behavior
  - Positive temperature coefficient on VF
- Kelvin source for easy drive
- Very low stray inductance
- Si3N4 substrate for improved thermal performance
- Solderable terminals both for power and signal

Benefits
- Outstanding performance at high frequency operation
- Direct mounting to heatsink (isolated package)
- Low junction to case thermal resistance
- Low profile
- RoHS Compliant

All ratings @ T_j = 25°C unless otherwise specified



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Absolute maximum ratings (per SiC MOSFET)

Symbol	*Parameter*		*Max ratings*	*Unit*
V_{DSS}	Drain - Source Voltage		1700	V
I_D	Continuous Drain Current	$T_c = 25°C$	94	A
		$T_c = 80°C$	70	
I_{DM}	Pulsed Drain current		200	
V_{GS}	Gate - Source Voltage		-10/25	V
V_{GSOP}	Gate - Source Voltage ; recommended operation values		-5/20	
R_{DSon}	Drain - Source ON Resistance		35	mΩ
P_D	Power Dissipation	$T_c = 25°C$	625	W

Electrical Characteristics (per SiC MOSFET)

Symbol	*Characteristic*	*Test Conditions*		*Min*	*Typ*	*Max*	*Unit*
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0V$, $V_{DS} = 1700V$				200	µA
$R_{DS(on)}$	Drain – Source on Resistance	$V_{GS} = 20V$ $I_D = 100A$	$T_j = 25°C$		22.5	35	mΩ
			$T_j = 150°C$		45		
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 36mA$		2	2.4	4	V
I_{GSS}	Gate – Source Leakage Current	$V_{GS} = 20$ V, $V_{DS} = 0V$				1.2	µA

Dynamic Characteristics (per SiC MOSFET)

Symbol	*Characteristic*	*Test Conditions*		*Min*	*Typ*	*Max*	*Unit*
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 1000V$ f = 1MHz			7344		pF
C_{oss}	Output Capacitance				342		
C_{rss}	Reverse Transfer Capacitance				13.4		
Q_g	Total gate Charge	$V_{GS} = -5/20V$ $V_{Bus} = 1200V$ $I_D = 100A$			376		nC
Q_{gs}	Gate – Source Charge				88		
Q_{gd}	Gate – Drain Charge				114		
$T_{d(on)}$	Turn-on Delay Time	$V_{GS} = -5/20V$ $V_{Bus} = 1200V$ $I_D = 100A$ $R_G = 2.5\Omega$			65		ns
T_r	Rise Time				20		
$T_{d(off)}$	Turn-off Delay Time				48		
T_f	Fall Time				18		
E_{on}	Turn on Energy	Inductive Switching $V_{GS} = -5/+20V$ $V_{Bus} = 1200V$ $I_D = 100A$ $R_G = 2.5\Omega$	$T_j = 150°C$		4.2		mJ
E_{off}	Turn off Energy		$T_j = 150°C$		1.72		
R_{Gint}	Internal gate resistance				3.15		Ω
R_{thJC}	Junction to Case Thermal Resistance					0.2	°C/W

Body diode ratings and characteristics (per SiC MOSFET)

Symbol	*Characteristic*	*Test Conditions*	*Min*	*Typ*	*Max*	*Unit*
V_{SD}	Diode Forward Voltage	$V_{GS} = -5V$; $I_{SD} = 50A$		4.1		V
t_{rr}	Reverse Recovery Time	$I_{SD} = 100A$ $V_R = 1200V$; $di_F/dt = 2800A/\mu s$		70		ns
Q_{rr}	Reverse Recovery Charge			1.06		µC
I_{rr}	Reverse Recovery Current			28		A

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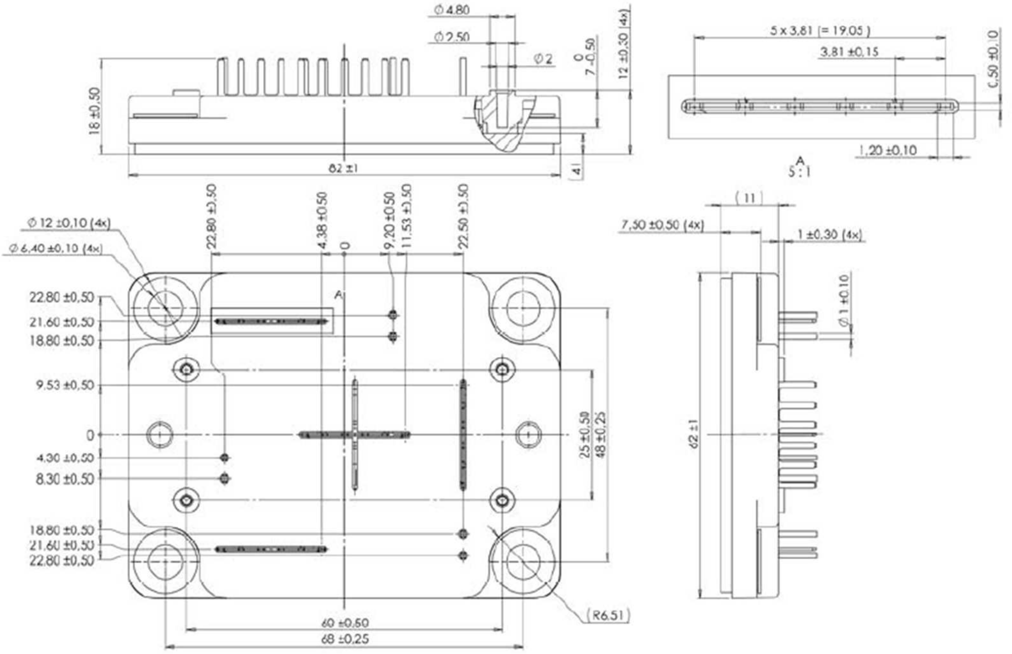
SiC schottky diode ratings and characteristics (per SiC diode)

Symbol	*Characteristic*	*Test Conditions*		*Min*	*Typ*	*Max*	*Unit*
V_{RRM}	Peak Repetitive Reverse Voltage					1700	V
I_{RRM}	Reverse Leakage Current	V_R=1700V	T_j = 25°C		240	1500	µA
			T_j = 175°C		500	3200	
I_F	DC Forward Current		Tc = 125°C		100		A
V_F	Diode Forward Voltage	I_F = 100A	T_j = 25°C		1.6	1.9	V
			T_j = 175°C		2.5	2.8	
Q_C	Total Capacitive Charge	V_R = 1100V			740		nC
C	Total Capacitance	f = 1MHz, V_R = 550V			480		pF
		f = 1MHz, V_R = 1100V			468		
R_{thJC}	Junction to Case Thermal Resistance					0.165	°C/W

Thermal and package characteristics

Symbol	*Characteristic*			*Min*	*Max*	*Unit*
V_{ISOL}	RMS Isolation Voltage, any terminal to case t =1 min, 50/60Hz			4000		V
T_J	Operating junction temperature range	SiC MOSFET		-40	150	°C
		SiC diode		-40	175	
T_{JOP}	Recommended junction temperature under switching conditions			-40	$T_J$max - 25	
T_{STG}	Storage Temperature Range			-40	125	
T_C	Operating Case Temperature			-40	125	
Torque	Mounting torque	To heatsink	M6	3	5	N.m
Wt	Package Weight				250	g

Package outline (dimensions in mm)



b) LOW-SIDE module

Non-specified characteristics are identical to that of the high-side module.

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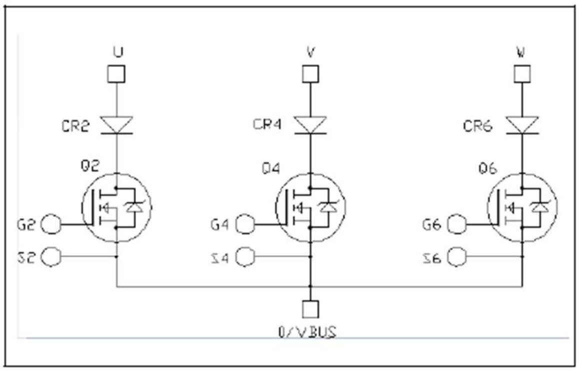
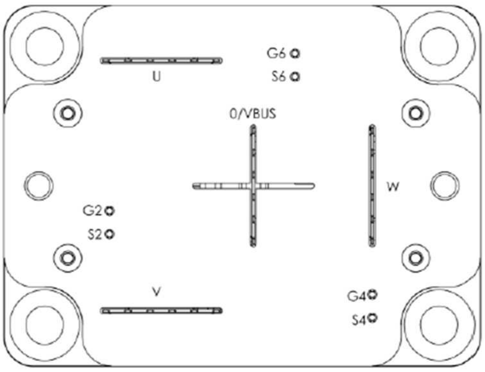
CMCAMC1703ULM35DCNG

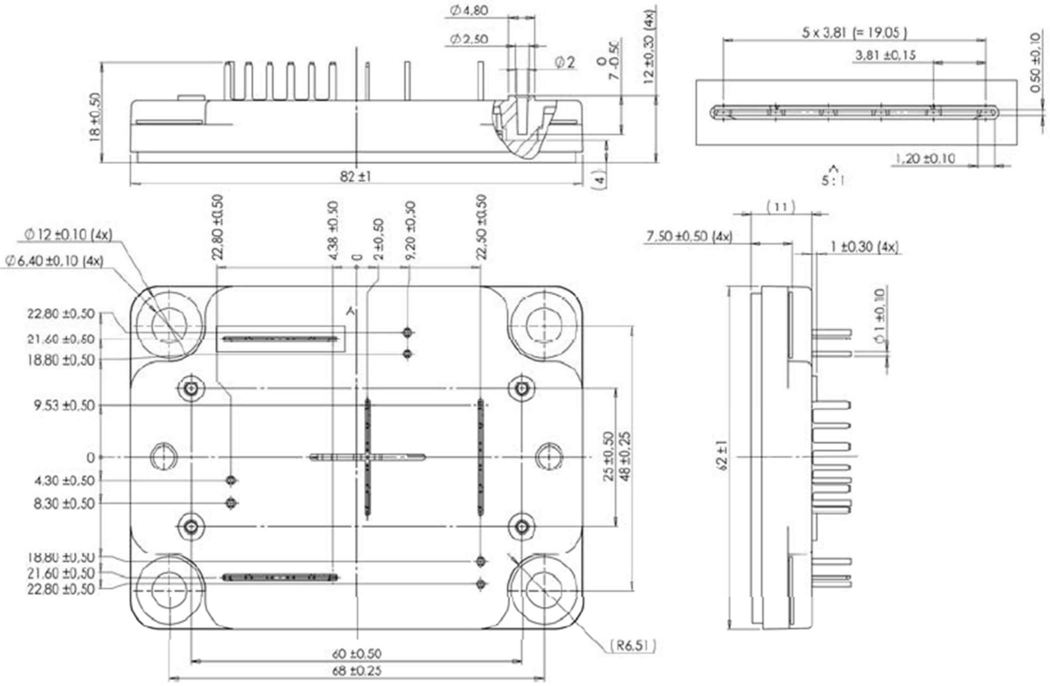
Triple single switch
with series diode
SiC MOSFET Power Module

V_{DSS} = 1700V
R_{DSon} = 35mΩ max @ Tj = 25°C
I_D = 94A @ Tc = 25°C





Package outline (dimensions in mm)



Appendix III – Design Considerations for the DC-DC Boost Converter in combination with a Three-phase Two-level Voltage Source Inverter

In this appendix are presented the design considerations and employed analytical expressions in losses calculations for the two-stage voltage-source based topology (see Figure III.1). The PV conversion system and the thermal specifications are as follows: $V_{f,l-l} = 690V$, $V_{dc} = 740V$, $I_{dc} = 81A$, DC current ripple $\Delta I_{dc,max} = 20\% \cdot I_{dc}$, $V_{bus} = 1.2kV$ (for the VSI), $R_{th,c-amb} = 0.08K/W$, $R_{th,j-c,D} = 0.33K/W$, $R_{th,j-c,MOS} = 0.4K/W$ and $T_{amb} = 25°C$.

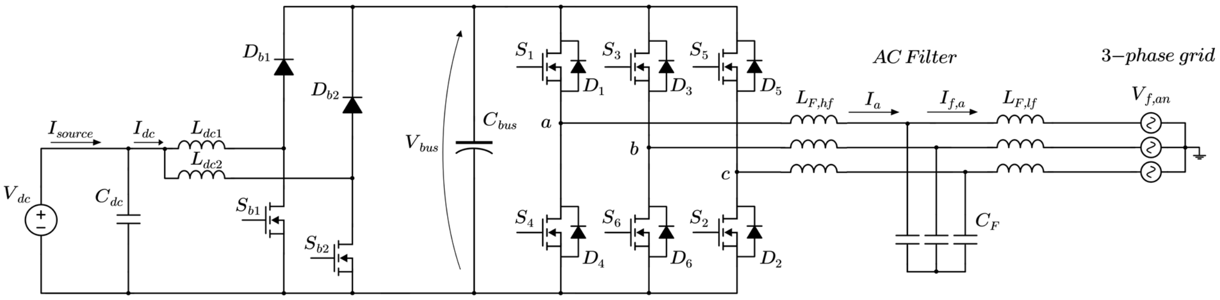
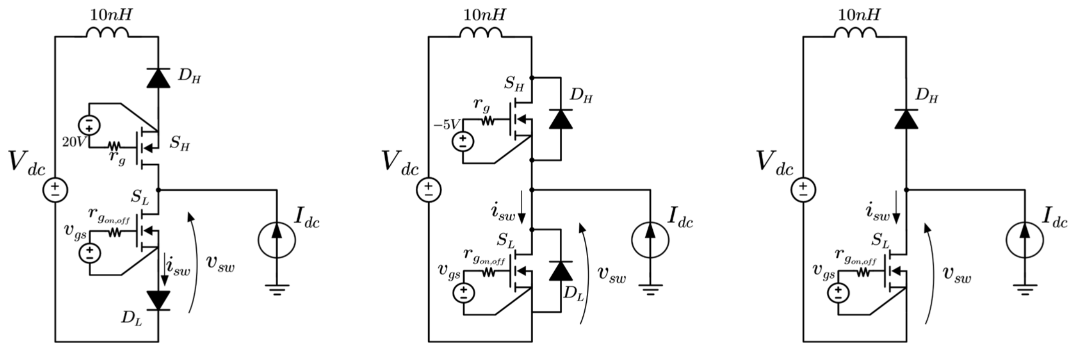


Figure III. 1 – Two-stage topology: interleaved boost converter in combination with a three-phase two-level VSI.

c) Determination of the Switching Energy Functions

To determine the switching energy functions ($E_{sw} = E_{sw,on} + E_{sw,off}$), LTspice simulations are carried out taking into account each device and topology configurations. Figure III.2 presents the implemented switching cell for all studied converters, namely, three-phase Current Source Inverter (CSI), three-phase two-level Voltage Source Inverter (VSI), interleaved boost (*i*Boost) and boost (Boost and Boost2) converters. In all cases, two chips per device ($n = 2$) are considered, with exception of Boost2, where $n = 4$. For the *i*Boost configuration, two interleaved legs are assumed, i.e., $q = 2$.



a) *b)* *c)*

Figure III. 2 – Implemented switching cell models in LTspice environment to obtain the switching energy functions for the following topologies a) CSI, b) VSI and c) all three boost configurations – *i*Boost, Boost and Boost2. Employed device models from Wolfspeed: CPM2-1700-0045B (MOSFETs) and CPW5-1700-Z050B (diodes). Simulation conditions: $r_{g,on} = 10.5\Omega$, $r_{g,off} = 8\Omega$, $v_{gs,on,off} = +20/-5V$ and $V_{dc} = 1200V$ (fixed for the VSI and boost converters only).

For all boost converters, Eq. III.1 is used to describe $E_{sw} = f(I_{dc})$. The corresponding coefficients are summarized in Table III.1.

$$E_{sw}(I_{leg}) = 10^{-6} \cdot \left(k_1 I_{leg}^2 + k_2 I_{leg} + k_3\right) \tag{III.40}$$

where $I_{leg} = I_{dc}/q$. For the Boost and Boost2, $q = 1$. Concerning the VSI, Eq. III.2 applies. Table III.1 summarizes the corresponding coefficients.

$$E_{sw}(I_{f,a}) = 10^{-6} \cdot \left(\frac{k_1}{4}\hat{I}_{f,a}^2 + \frac{k_2}{\pi}\hat{I}_{f,a} + \frac{k_3}{2}\right) \tag{III.41}$$

where $\hat{I}_{f,a}$ is the peak value of the line current fundamental component.

Table III. 11 – Coefficients for definition of $E_{sw} = f(I_{dc})$.

Topology	k₁	k₂	k₃
VSI	0.1028	22.185	1835.3
Boost2	0.1414	47.323	1664.9
*i*Boost and Boost	0.0999	25.275	819.6

For the CSI, the dependency of E_{sw} with regard to the grid angle θ (then the grid voltage ($V_{f,l-l}$) as well) and PV current (I_{dc}) must be known. For that reason, several sets of simulations must be carried out to have $E_{sw} = f(\theta, I_{dc})$. Then, the following second order polynomial equation can be employed to fit the obtained switching energy data:

$$E_{sw}(\theta, I_{dc}) = k'_1 + k'_2\theta + k'_3 I_{dc} + k'_4\theta^2 + k'_5\theta I_{dc} + k'_6 I_{dc}^2 + k'_7\theta^3 + k'_8\theta^2 I_{dc} + k'_9\theta I_{dc}^2 \quad \text{(III.42)}$$

The employed coefficients in Eq. III.3 are given by:

$$\begin{bmatrix} k'_1 \\ k'_2 \\ k'_3 \\ k'_4 \\ k'_5 \\ k'_6 \\ k'_7 \\ k'_8 \\ k'_9 \end{bmatrix} = \begin{bmatrix} -23.77 \\ 473.8 \\ -2.82 \\ 1213 \\ 29.71 \\ 0.04799 \\ -616 \\ -1.973 \\ -0.2402 \end{bmatrix} \cdot 10^{-6} \quad \text{(III.43)}$$

d) Semiconductor Losses Calculations

- DC-DC Boost Converters

The boost transistors $S_{b1,2}$ current stress is given by

$$\begin{aligned} I_{avg,Sb1,2} &= \alpha \cdot I_{leg}(q) \\ I_{rms,Sb1,2} &= \sqrt{\alpha} \cdot I_{leg}(q) \end{aligned} \quad \text{(III.44)}$$

The boost diodes $D_{b1,2}$ current stress is defined as

$$\begin{aligned} I_{avg,Db1,2} &= (1-\alpha) \cdot I_{leg}(q) \\ I_{rms,Db1,2} &= \sqrt{1-\alpha} \cdot I_{leg}(q) \end{aligned} \quad \text{(III.45)}$$

Concerning the conduction and switching losses generated by the boost transistor, the following applies:

$$\begin{aligned} P_{cond,Sb1,2}(T_j, I_{leg}) &= \frac{R_{ds,on}(T_j, I_{leg})}{\beta} \cdot I_{rms,Sb1,2}^2 \\ P_{sw,Sb1,2}(I_{leg}) &= F_{sw,leg} \cdot E_{sw}(I_{leg}) \end{aligned} \quad \text{(III.46)}$$

where $F_{sw,leg} = F_{sw}/q$. $\beta = 1$ to all boost topologies, except for Boost2, where $\beta = 2$. Also, in the previous equation, $R_{ds,on}$ represents the equivalent on-state resistance of two MOSFETs in parallel. Its temperature and current dependencies are model as in Appendix I.

Only conduction losses are considered to be generated by the SiC diodes:

$$P_{cond,Db1,2}(T_j) = V_o(T_j) \cdot I_{avg,Db1,2} + \frac{R_o(T_j)}{\beta} \cdot I_{rms,Db1,2}^2 \quad \text{(III.47)}$$

Finally, the overall semiconductor boost losses are defined as follows:

$$P_{boost} = q \cdot \left(P_{cond,Sb1,2}(T_j, I_{leg}) + P_{sw,Sb1,2} + P_{cond,Db1,2}(T_j)\right) \tag{III.48}$$

- **Three-phase Two-level VSI**

The VSI transistors $S_{1..6}$ current stress is given by

$$\begin{gathered} I_{avg,S1..6} = \frac{\hat{I}_{f,a}}{2\pi} \cdot \left(1 + M_{VSI} \cdot \frac{\pi}{4} \cdot \cos(\phi)\right) \\ I_{rms,S1..6} = \hat{I}_{f,a} \cdot \sqrt{\left(\frac{1}{8} + \frac{M_{VSI}}{3\pi} \cdot \cos(\phi)\right)} \end{gathered} \tag{III.49}$$

where $M_{VSI} = 2 \cdot \frac{\hat{V}_{f,l-n}}{V_{bus}}$ is the VSI modulation depth.

The VSI anti-parallel diodes $D_{1..6}$ current stress is defined as

$$\begin{gathered} I_{avg,D1..6} = \frac{\hat{I}_{f,a}}{2\pi} \cdot \left(1 - M_{VSI} \cdot \frac{\pi}{4} \cdot \cos(\phi)\right) \\ I_{rms,D1..6} = \hat{I}_{f,a} \cdot \sqrt{\left(\frac{1}{8} - \frac{M_{VSI}}{3\pi} \cdot \cos(\phi)\right)} \end{gathered} \tag{III.50}$$

Concerning the conduction and switching losses generated by the VSI transistors, the following applies:

$$\begin{gathered} P_{cond,S1..6}(T_j, \hat{I}_{f,a}) = R_{ds,on}(T_j, \hat{I}_{f,a}) \cdot I^2_{rms,S1..6} \\ P_{sw,S1..6}(\hat{I}_{f,a}) = F_{sw} \cdot E_{sw}(\hat{I}_{f,a}) \end{gathered} \tag{III.51}$$

Only conduction losses are considered to be generated by the VSI SiC diodes:

$$P_{cond,D1..6}(T_j) = V_o(T_j) \cdot I_{avg,D1..6} + \frac{R_o(T_j)}{\beta} \cdot I^2_{rms,D1..6} \tag{III.52}$$

Then, the overall VSI semiconductor losses are defined as follows:

$$P_{VSI} = 6 \cdot \left(P_{cond,S1..6}(T_j, \hat{I}_{f,a}) + P_{sw,S1..6}(\hat{I}_{f,a}) + P_{cond,D1..6}(T_j)\right) \tag{III.53}$$

Finally, the semiconductor efficiency for the two-stage VSI+boost converter is calculated with:

$$\eta_{semi} = \frac{P_{in}}{P_{in} + P_{boost} + P_{VSI}} \tag{III.54}$$

- Three-phase CSI

Identical current stress and losses expressions presented in Chapter 3 are used for CSI again. The same is valid for the associated equivalent thermal model.

e) Thermal Model for the VSI+boost Converter

Figure III.3 depicts the assumed thermal model for the two-stage VSI+boost converter. The iterative process presented in § 3.3.2 is used again to obtain the final junction temperatures for a given converter input power level.

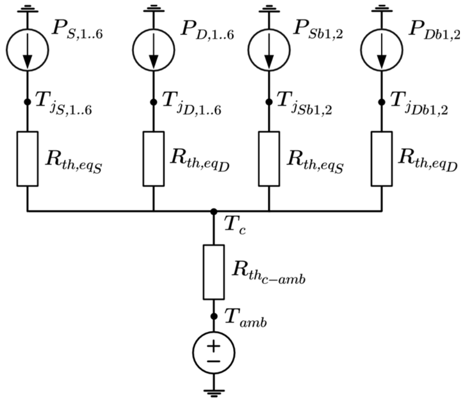


Figure III. 3 – Considered thermal model for the VSI+boost converter.

f) Dimensioning of Components for the VSI+boost Converter

- DC-link Capacitor (C_{bus})

The analytical DC-link capacitor sizing in a two-stage conversion system can represent a challenging task, since its resultant voltage ripple is a function of three independent variables: the boost switching frequency, VSI switching frequency and grid fundamental frequency. For that reason, in this work, the value of C_{bus} is obtained by simulation using PSIM, where its minimum value is chosen to insure a maximum DC voltage ripple of $5\% \cdot V_{dc}$.

- DC Boost Inductor (L_{dc})

The main DC boost inductor (L_{dc}) dimensioning criteria is the DC current ripple.

$$L_{dc}(q) = \frac{V_{bus}\left[\gamma(q\alpha) \cdot \frac{1-\gamma(q\alpha)}{q}\right]}{\Delta I_{dc,max} \cdot I_{dc} \cdot F_{sw}} \tag{III.55}$$

where $\gamma(q\alpha)$ represents the relative duty cycle value, assuming a value between zero and one.