New FDSOI-based integrated circuit architectures sensitive to light for imaging applications

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THÈSE

Pour obtenir le grade de

DOCTEUR DE LA COMMUNAUTE UNIVERSITE GRENOBLE ALPES

Spécialité : **Nano Electronique et Nano Technologies**

Arrêté ministériel : 25 mai 2016

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préparée au sein du **Laboratoire d'électronique et des technologies de l'information (CEA-LETI)**
dans **l'École Doctorale électronique, électrotechnique, automatique et traitement du signal (EEATS)**

Études de nouvelles architectures de composants intégrés sensibles à la lumière en filière FDSOI pour les applications de type imageur

Thèse soutenue publiquement le **07/06/2019**,
devant le jury composé de :

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To all the seekers of knowledge lost in the Mediterranean Sea

AKNOWLEDGEMENTS

I conducted my three years thesis research at LETI, in the advanced CMOS integration laboratory (LICL) in CEA-Grenoble. One of the best assets of LETI is the availability of experts that are always willing and benevolent to help and share their knowledge on the campus. Thanks to them I was able to learn and develop many new competences, so I'd like to start by thanking all the people at LETI that helped me achieve this work.

I'd like to thank the members of my jury, Pr. Pierre Magnan, Dr. Yang Ni, Pr. Francis Calmon, Pr. Albert Theuwissen, and Dr. Frederic Lalanne, for reading my manuscript, attending the defense and for all the positive and important feedback that helped me increase the quality of this manuscript. It was an honor having you all in my jury.

My warmest gratitude to my supervisors: Olivier Rozeau, SPICE modeling master, thank you for your guidance despite me "Papillonner" way too much, and for answering my questions during the countless times I entered your office saying "Olivier, j'ai une question" (I never had only one question though). Thank you for challenging me and demanding rigor in my work, helping me become a much better researcher. Laurent Grenouillet, process integration master, thank you for the good vibes ;), your constant enthusiasm which always motivated me to do better, and for your encouragement and support. I learned the benefit of having a positive critical thinking from you. Thank you also for the "end of contract-defense" period where you were always responding and available to discuss the manuscript/poster/paper (or to listen to me complaining) at the rdc of the bcc building. My thesis director Alexei Tchelnokov for all your encouragement and advices, and for being available to participate to our periodic meetings and enriching the discussion every time. Finally, thank you all three for the guidance and the rehearsals and review of paper/manuscript/presentations, I learned so much during these three years thanks to you. I hope I'll have the pleasure of working with you all again in the future!

I'd like to thank my manager, Maud Vinet, for welcoming me in the LICL, and for your encouragement throughout the thesis. Thank you, the early morning technician team, Claude, Jean-Mi, Marie-Pierre, and Paul, for all the good memories around a nice Nespresso. Special thanks to Claude with whom I shared the office for three years. Thank you for all the conversations on variable topics, all the French grammar/movies/books/singers 70s pop culture knowledge that you shared with me (whether I wanted or not ;)). Thank you Louis (waaw), for genuine funny, interesting conversations. Thanks to all the people in the lab that I interacted with, whether it was in meetings, lunch, coffee or just discussions in the office: Bernard, Christophe, Valerie, Zdeneck, Hervé, Yves, Cyrile, Claire, Perrine, François, Laurent, Nils, Alexandre L, Sylvain, Laurent and Jean-Pierre. The electrical tests team: Jean and Alex V (you guys will always be my first mentors), Denis for your help with the IPE and all the fruitful discussions, Niccolo for negotiating on the equipment's and wafers, Jacque, Xavier, Alain, Charles, the phd community Ilias, Artemisia, and Kostas (aka Istanbul) for making me a café frappé whenever I wanted one, and for the support through a good laugh whenever I had problems with my tests. Thank you Pascal Scheiblin from the simulation lab for your help with Silvaco and the VWF, and Christophe Licitra for the last minute simulations.

Thank you the Padawan team of the LICL that gave meso many wonderful memories of these three years spent in the lab. The old generation: Julien, Alex, Mathilde, Jose, thank you guys for the pause café, the magic music quiz, and for making me feel part of the team right away. Rémy-sempai, who I would ask questions instead of opening a book on semiconductor physics and thanks to whom I learned so much from new French vocabulary to animals walk…whatever. Luca (thanks for the Loacker!), Vincent (secret kawai at heart), Sotiris (Café frapé), Benoit, Corentin, Loic, and Fabien. My generation: Jessy (rose et papillon), Thomas, and Carlos, we made it! Thank you guys for the support, discussions, breaks, and advice. The new generation: Giulia (girls power!) thank you for being an example of confidence, and inspiring me to become stronger, Camila with whom it was a pleasure sharing the same office, thank you for your support during the difficult time that are deadlines, and for the encouragement and discussions, just chill you're going to do great ;), Daphnée, zen and give you a sense of zénitude, thanks for your cheerfulness and the good laughs, Mariia, Elizabeth, Louise, for sharing the office for short yet memorable periods of time. I wish to all of you the best of the best in life.

Thank you Marie, Faiza, and Amna for always maintaining my nostalgia for the other side of the Mediterranean Sea, and to Yumi-chan for maintaining my nostalgia for an even further away side. My best friends in Libya: Tasnim, Rawad, Elham, Nouran, and Arwa, who didn't loosen their support and encouragement even though I missed all their important events. Thank you for everything guys, I've missed you a lot and I'll see you soon!

I'd like to thank my family for their support throughout my education. Thank you, aunts, uncles, and cousins in France and Libya. Special thanks to tata Salha for listening to me complaining and worrying during these 3 years, and for attending my defense. Thanks mom and dad, for your unconditional support and constant encouragement, my brothers Marwan, Hicham, Sofian, Yazid, and Walid, my Sis-in-law Hamida and my niece Boubou. You guys always find a way to make me laugh away all my problems.

Finally, thank you everyone that helped me succeed and get where I am today.

Sincerely

Lina Kadura

TABLE OF CONTENT

GLOSSARY

List of Abbreviations

Acronym	***Definition***
AC	Alternative current
ADC	Analog-to-Digital Converter
ADAS	Advanced Driving Assistance System
AI	Artificial Intelligence
APS	Active Pixel Sensors
AR	Augmented Reality
ARC	Anti-Reflection Coating
BB	Back Bias
BEOL	Back End Of Line
BF	Body Factor
BOX	Buried OXide
BSI	Back Side Illumination
CCD	Charge Coupled Device
CDS	Correlated Double Sampling
CIS	CMOS Image Sensors
CMOS	Complementary Metal Oxide Semiconductor
CTRIM	Crystal-TRIM
DC	Direct Current
DCL	Duty Cycle
DPS	Digital Pixel Sensor
DR	Dynamic Range
DRAM	Dynamic Random Access Memory
DRC	Design Rule Checker
DRM	Design Rule Manual
DTI	Deep Trench Isolations
DUT	Device Under Test
FBB	Forward Back Bias

FDSOI	Fully Depleted Silicon On Insulator
FEOL	Front End Of Line
FF	Fill Factor
FoM	Figure of Merit
FPGA	Field-Programmable Gate Array
FPN	Fixed Pattern Noise
FSI	Front Side Illumination
FWC	Full Well Capacity
GND	Ground (reference zero)
GO1	Thin Gate Oxide
GO2	Thick Gate Oxide
GP	Ground Plane
HDR	High Dynamic Range
IR	Infrared
LIDAR	Light Detection and ranging
LIVS	Light Induced VT Shift
LVT	Low VT
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MtM	More than Moore
MUX	Multiplexer
NA	Numerical Aperture
NIR	Near Infra-Red
OBB	Optical Back Biasing
PD	Pull Down
PFM	Pulse Frequency Modulation
PM	Pulse Modulation
PPS	Passive Pixel Sensor
PU	Pull Up
PWM	Pulse Width Modulation
QE	Quantum Efficiency
RBB	Reverse Back Bias
RVT	Regular VT
SCE	Short Channel Effect
SNM	Static Noise Margin

SNR	Signal to Noise Ratio
SOI	Silicon On Insulator
SPAD	Single Photon Avalanche Diode
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	Static Random Access Memory
SS	Subthreshold Swing
STI	Shallow Trench Isolations
TEM	Transmission Electron Microscopy
ToF	Time of Flight
TSV	Through Silicon Via
UTBB	Ultra-Thin Body and BOX
VDD	Supply Voltage
VLC	Visible Light Communication
VR	Virtual Reality
VTC	Voltage Transfer Curve

INTRODUCTION

Today's technology is moving towards enabling a smarter environment. Sensors are everywhere, and their number is expected to drastically increase in the future years. New applications englobed in the Moore's law spin off, More-Than-Moore (MtM), have been demonstrated. Light sensors are major contributors to this evolution. Used primarily as image sensors, they now have evolved towards ambient intelligence application when used as motion, proximity, ambient light sensors and so on. The image sensor industry growth has not declined since the first camera was embedded in mobile phone that later became smartphones. The pixel size kept shrinking over the years and new technologies were developed to continue improving their performance. Today's challenges regarding image sensors include high speed, high performance, small size and always less energy consumption. To achieve the aforementioned criteria, 3D stack technology of multiple layers, including the processing and memory layer on top of the sensor have been developed. To avoid complex process integration, planar embedded sensors, where the structure is by default 3D-like, will increase the ease of integration at a lower cost. Also allowing the use of more advanced technological nodes will not only reduce the pixel size, but also the power demands of the circuit. Finally, decoupling the sensing from the readout is an interesting solution to allow the optimization of both parts and expend the range of detection using the same readout circuit. It is in this context that falls the thesis topic.

A Light sensor based on the co-integration of a Fully Depleted Silicon-On-Insulator (FDSOI) transistor with a photodiode underneath the Buried Oxide (BOX) is thoroughly studied, simulated, and characterized. This sensor, called ***FDPix*** and shown in Figure I-1, features very small size, simplified process, and low power consumption. when illuminated, the photogeneration in the photodiode will modulate the transistor electrical characteristics by means of a capacitive coupling between the front and back interfaces. Therefore, no electrical connection is present nor needed between the sensing transistor and the photosensitive element for the device to operate. This maintains the size of the sensor minimum since it is composed of only one transistor.

The thesis was conducted at LETI, a French research institute located in Grenoble, France, that tremendously contributed to the development of the FDSOI technology, along with its regional partners, STMicroelectronics and SOITEC, in the 2005s. All the devices studied and characterized in this work were fabricated at STMicroelectronics using 28nm node FDSOI technology. In the view of MtM applications, and the proven performance of FDSOI in analog/RF sensors, this thesis topic follows this unstoppable trend of integrating more intelligence as close as possible to the sensor.

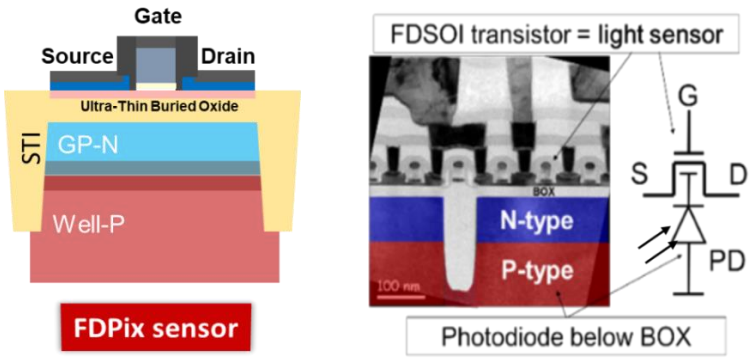

Figure I-1: FDPix sensor sideview, TEM image and schematic

Thesis organization:

Chapter 1 is dedicated to the state of the art of the field of image sensors. Starting with an economical and market view on the topic, it follows a presentation of the standard image sensor and the main figure of merits (FoM). Specific sensor architectures that optimize certain of these FoMs are also discussed, such as small pixel dimensions and logarithmic pixels. Finally, the main trending applications are briefly introduced and discussed based on the sensor architecture used.

Chapter 2 kicks off the investigation on the FDPix sensor. The main physical phenomenon characterizing the sensor operation in the DC domain are studied. The FDSOI transistor and the photodiode that forms the structure are modeled. Finally, the FDPix sensor is evaluated by considering the combination of the two. The DC characteristics are discussed using TCAD simulation and opto-electrical characterization of the fabricated devices. A fabrication flow is also presented highlighting the main step to be modified in the 28nm process flow to obtain our sensor. The chapter is concluded by introducing an important property of the FDPix based on Complementary Metal Oxide Semiconductor (CMOS) integration.

Chapter 3 continues the study of the response of the FDPix in the time domain. The equivalent capacitance network of the device is analyzed, and the response times of the sensor are characterized. A reset method is developed, and the transient response curve of the sensor discussed. We will show that a good agreement is obtained between the developed model implemented in SPICE environment and the electrical characterization. Finally, a test case with variable light stimuli is presented.

Chapter 4 presents the optimization of the FDPix technological and operational parameters in DC and transient domain. Both the transistor and photodiode are optimized, and the main tradeoffs are discussed. In this chapter, we also present different integration schemes investigated to optimize the device parameters, such as Back Side Illumination (BSI) and junction engineering. A conclusion on scaling effect on the device is drawn and summarized, as well as a perspective regarding the possible versatility of integration of the sensor.

Chapter 5 is design oriented. Different pixel architectures were designed, layouted, fabricated and tested. We divided them in two categories: analog pixels based on amplifier circuits, and digital-like pixels based on Pulse width

Modulation (PWM) and light sensitive inverters. The designed pixel circuits were proven to be functional. We conclude the chapter by presenting simulated and tested logic devices such as Static Random Access Memory (SRAM) and pass gates sensitivity to light illumination, which opens perspectives in smart sensor applications.

Chapter 6 ends the thesis manuscript with a general conclusion, and the major perspectives regarding the FDPix sensor.

Details regarding the simulation tools and models, as well as the characterization setup specifications and data processing codes are given in **Appendix A** and **B**. **Appendix C** presents extra pixel circuit configurations developed during this work.

CHAPTER ONE

Chapter 1 : Image Sensors and Light Detectors

The increase of user interactive applications is driving the semiconductor industry towards more heterogeneous technologies, in which both the analog sensing and digital processing are of equal importance. The scaling of the transistor dimensions following Moore's law *[MOORE 1998]* and Dennard scaling *[DENNARD 1974]* allowed the digital electronics applications to improve over the years. Digital circuits today demonstrate impressive performance with lower power consumption, and always smaller size. Due to the emergence of new fields of applications, and the evolution of the societal needs, the industry redefined the Moore's law to englobe these new applications. Two subsets were defined (Figure 1-1). The "More Moore" section continues the scaling, or rather the effective scaling of the transistor using advanced material technology and processes. The size of the transistor is relatively constant, but its performance is still following the prediction using technology enabler elements (beyond CMOS). The second divergence from the Moore's law is the More-than-Moore (MtM). The MtM deals with diversification based on an application-oriented technology development route, where the consumer is of major interest. MtM englobes applications enabling ambient intelligence that concerns health, mobility, communication, security, etc *[ARDEN]*. These applications are mainly in need of devices that interacts with the outside world. Therefore, it concerns analog and RF circuits, powering circuits, sensors and actuators, biochips and so on. The digital is no longer the driving force in MtM. However, for most of the applications, a heterogenous integration is necessary. In this category falls one of the major driving applications in the MtM, the CMOS Image Sensor (CIS).

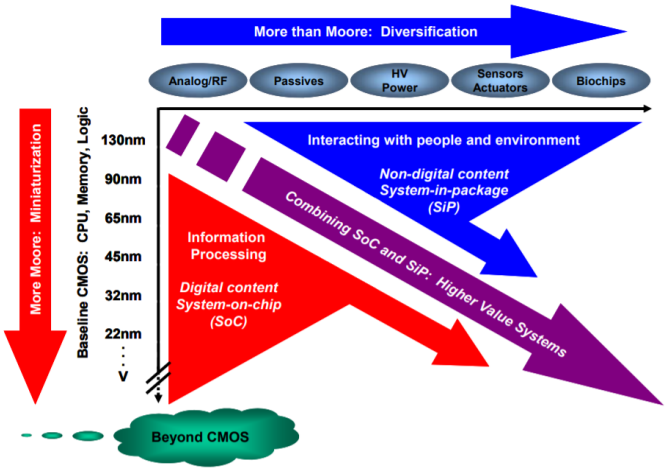

Figure 1-1: The ITRS trends, towards miniaturization (More Moore) towards diversification (More-Than-Moore) [ARDEN]

The CIS is a heterogenous technology. The photon-to-electron conversion is performed by the pixel array, the readout is using analog amplifiers, and finally the image processing is performed on digital data. Since its development in the 90s, and due to the integration of the camera in the mobile phone in 2000, the CIS market has encountered a steady growth. As reported by *[YOLE DEVELOPPEMENT 2018A]*, the CIS market is expected to grow from $16B in 2017 to $24B in 2023, or as expressed in Figure 1-2 in terms of production volume *[IBS 2018]*. Today, the mobile market is still the main driver and is not expected to back down with the introduction of dual and triple camera systems. The report presented by Yole shows a 17% growth in the mobile part of the CIS market. Since 2010, CIS devices upgraded

to feature Back-Side Illumination (BSI) combined with 3D stack process. Now the hybrid stack and multi-level stack have become the new trends. These technologies enabled new features such as slow motion and 3D imaging embedded in smartphones. These advances in CIS were enabled by the three key players that dominates the market, namely Sony (42%), Samsung (20%), and Omnivision (11%). They have been dominating the CIS market by developing BSI, 3D stack process and hybrid integration.

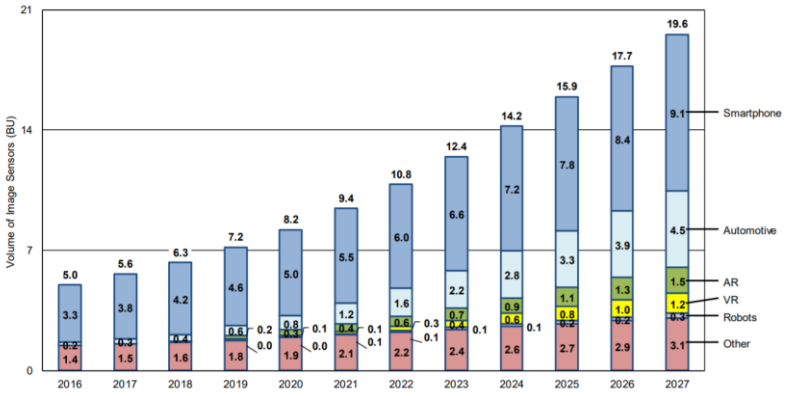

Figure 1-2: production volume of CMOS image sensors for different application segment [IBS 2018]

Other domains of application have experienced an important growth during the past years. The automotive which is a major trend in the industry at the moment, experienced a 23% growth between 2016 and 2017. Security also have become a major contributor to the CIS market with a 26% growth. Finally, Artificial Intelligence (AI), Augmented Reality (AR) and Virtual Reality (VR) are applications that attract a lot of attention and are major contributors to the demands on CIS. The CIS ecosystem has indeed shifted from "vision for imaging to vision for sensing" (*Yole)* as depicted in Figure 1-3. All ambient intelligence application englobed in the MtM, are contributing to the constant demand of improved key metric performance of image sensors.

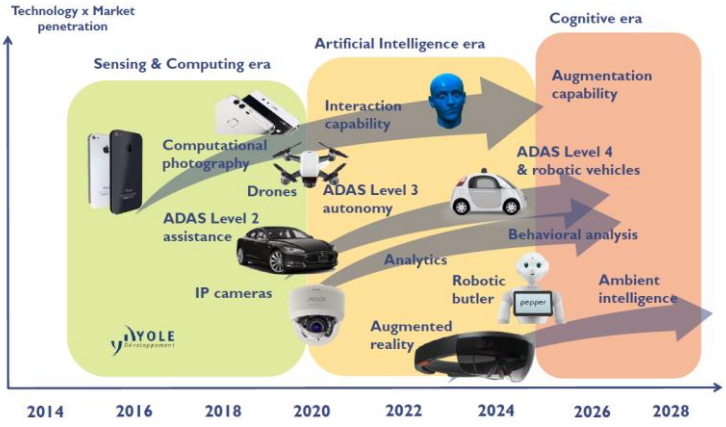

Figure 1-3: Roadmap for CIS application [YOLE DEVELOPPEMENT 2018A]

1.1. Standard camera system

A standard camera system is shown in Figure 1-4. The procedure of image capture can be described as follows:

- The light (sun light or artificial) is reflected on the scene, and the incoming reflected waves interact with the camera system by first being focused by the main camera lenses on the sensor.
- The light is then focused on each photosite by means of microlenses present per pixel.
- Since the photosite detect only the brightness of the scene, each pixel has a color filter to discriminate the color. This is obtained by using a mosaic Bayer color filter *[BAYER 1976]*, composed 50% of green pixels and 25% red 25% blue. A demosaicing process[1] is performed to process the raw data and obtain the final image.
- The monochromatic light penetrates the photosite where the conversion of photon-to-electron takes place due to the photoelectric effect. The photogenerated charges are then converted to a voltage analog output by analog amplifiers either located at the array level, or locally in the pixel.
- The analog voltage readout is further amplified and converted to digital data using an Analog-to-Digital Converter (ADC).
- The digital signal is further processed for error and noise correction and saved in a memory.

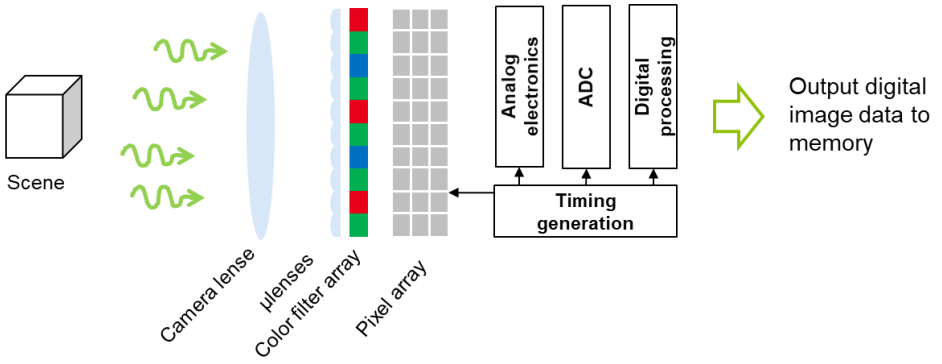

Figure 1-4: Standard color imaging camera system

The system shown and described is for visible light imaging. For other application targeting detection rather than color imaging, some component will differ, such as the presence or not of a color filter array. Also, the processing blocks will depend on the pixel architecture used. The pixel array is what ultimately determines the quality and efficiency of the system. We will present in the next sections a comparison between the two standard pixel technologies that dominated the market of digital imaging, namely the charge coupled devices (CCD) and the Complementary metal oxide semiconductor (CMOS) pixels.

[1] Demosaicing is a digital image processing algorithm used to reconstruct the image from the color samples. It is performed using simple interpolation techniques such as nearest neighbor interpolation.

1.1.1. CMOS vs CCD

Up until the 90s, the image sensor industry was dominated solely by Charge-Coupled Devices (CCD) developed in the 70s. A CCD sensor consist in an array of MOS capacitors *[HOWELL 2003]* (Figure 1-5.a). When illuminated, the photo-generated charges are collected in the potential well. Then the charges are readout within the array by sequentially biasing the gates of one column and are then converted to a voltage by an amplifier located outside the array. The advantages of the CCD are high quality/resolution imaging, high sensitivity, ~100% fill factor[2] and low noise. However, the readout is slow due to serial readout, it has a dedicated process not compatible with standard CMOS process, which resulted in a relatively higher price.

The first CMOS image sensors (CIS) were developed in the 70s, where the pixel was composed of only a photodiode and one select transistor and was called Passive Pixel Sensor (PPS). Although offering a high FF, its noise performance much lower than CCD, prevented it to be considered for imaging. It is in the early 90s, when the CMOS Active Pixel Sensor (APS) was developed *[FOSSUM 1993]* that the CIS became a true competitor to CCD. In APS, the amplifier is integrated per pixel resulting in a local charge-to-voltage conversion and a voltage readout (Figure 1-5.b). This inevitably increased the number of transistors per pixel which reduced the FF. However, its compatibility with standard CMOS process allowed the miniaturization and reduced the manufacturing cost. In CCD, since the charges photogenerated need to be transferred, it requires more power. Also, the readout is performed in series, which highly limits the sensor speed. It is also very sensitive to temperature variation and in some applications needs to be cooled. CIS allowed random access in the same way as Dynamic Random Access Memory (DRAM), where the voltage analog output is readout in parallel, which highly increases speed and decreased power consumption.

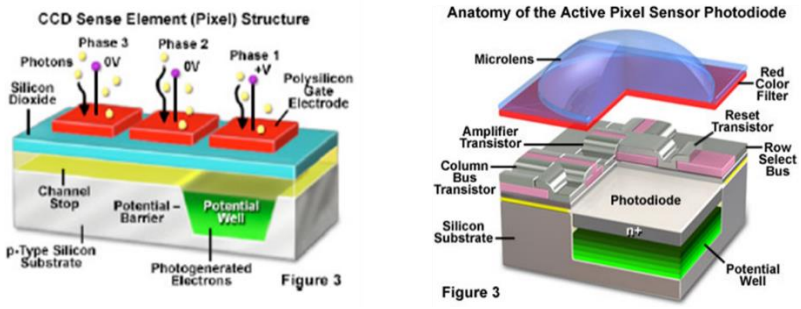

Figure 1-5:CCD vs CMOS image sensor pixel structure [HOWELL 2003][TURCHETTA]

Due to their superior performance and small size over CMOS, CCD dominated the market until early 2000s. In 2000, the first mobile phone featuring an embedded camera was developed by Sharp in Japan *[DIGITALTRENDS 2013]*. This camera used a CMOS image sensor with 0.11-megapixel resolution. The main driver for developing CIS became the mobile device market. Starting from there, the potential of market growth for embedded camera was evident. In 2017 about 1.2 trillion digital pictures were taken and 85% of them using smartphones *[STATISTICA 2017]*. The sensor requirement for mobile application are: small size, low cost, speed and low power. For all these properties the CIS surpassed the CCD. At the beginning of CIS era, the image quality was not comparable with CCD due to lower FF

[2] The Fill Factor represent the ratio of the photosensitive area to the total area of the pixel. It will be defined in later sections

and higher noise, but now with the advance in CMOS technology and image sensor technology improvement, CIS quality is as good as CCD if not better, for lower power consumption and high-speed imaging. Now the CMOS market surpasses the CCD as shown in Figure 1-6. However, CCD are still used in niche applications such as ultra-high-resolution applications, and ultra-low-light applications such as astrophotography. Since the market is moving towards smart sensing, there is no doubt that CIS will stay the main sensor used for future applications.

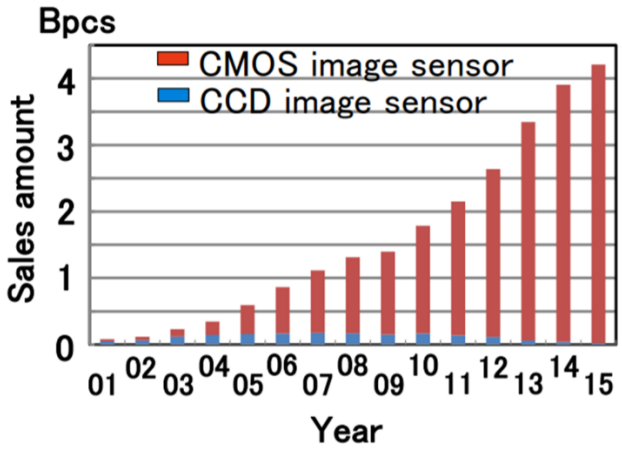

Figure 1-6: sales amount in the past years for CCD and CMOS [TERANISHI 2018]

In the following section of this chapter, the main CMOS sensor properties are discussed. We will present the most common architectures, as well as architectures that optimizes specific parameters such as size and Dynamic Range (DR).

1.1.2. CMOS image sensors standard architectures

1.1.2.1. Passive Pixel Sensor (PPS)

When the CIS was first developed in the 70s, it was as the passive pixel sensor (PPS) shown in Figure 1-7.a. This architecture is simple, it only contains a diode for detection and a transistor for row selection. Although being simple, this technology suffered from poor image quality, slow readout, and large noise resulting from the capacitive mismatch between the pixel and the column bus which resulted in high KTC noise. Therefore, the CCD dominated since it offered much better performance.

1.1.2.2. Active Pixel Sensor (APS)

The Active Pixel Sensor (APS) was first proposed by Noble in 1968 *[NOBLE 1968]*, and more greatly studied under this term, APS, in the 90s by Eric Fossum *[FOSSUM 1993]*. This architecture consisted in adding the column amplifier per pixel to perform charge-to-voltage conversion locally. In this manner, a voltage output is readout instead of charge transfer. This resulted in reducing power consumption, random access, and high-speed readout. Although adding transistor per pixel reduced the FF, the improvement due to the advantages mentioned resulted in making this architecture the most widely used today. The first version of the APS consisted in three transistors per pixel (3T APS) and is shown in Figure 1-7.b, where a reset (RST), source follower (SF), and row select (SEL) transistors are implemented per pixel. Due to the reset transistor being connected directly to the photosensitive node, this pixel has

a high reset noise. In early 80s, N.Teranishi developed the pinned photodiode *[TERANISHI 1982]* where a P+ layer is implanted at the interface to passivate the Si/SiO2 interface states. This approach considerably reduced noise. Initially integrated for CCD devices, it was later used in CIS *[FOSSUM 2014][GUIDASH 1997]* which allowed considerable reduction of dark current, increase of saturation level and improved sensitivity. It also resulted in using electronic shutter by using a transfer gate (TX) and a floating diffusion (FD) node. This architecture is shown in Figure 1-7.c. and is called the four transistor (4T) APS. The 4T APS architecture is the most used pixel sensor today. By decoupling the reset node from the sensing node, the reset noise was reduced. True Correlated Double Sampling (CDS) technique (section 1.2.1.4.d) can be implemented, and when complete charge transfer is achieved, the image lag[3] is suppressed using this architecture.

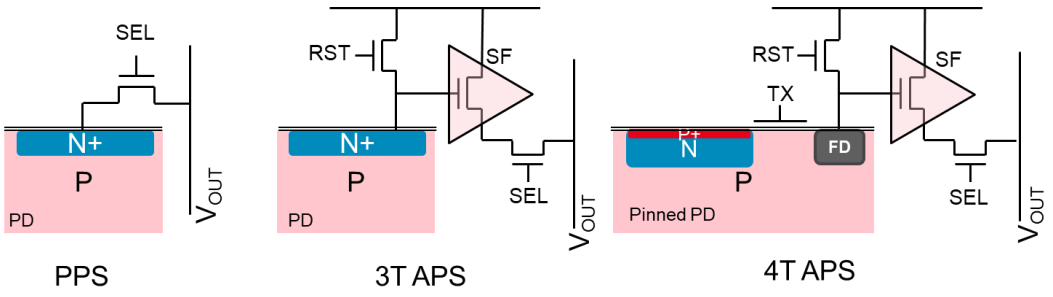

Figure 1-7: Standard pixel architectures: a) PPS b)3T APS c)4T APS

1.1.2.3. Digital Pixel Sensor (DPS)

In the previously mentioned architectures, the output of the pixel is an analog voltage signal. After the readout this voltage is converted to digital data using an Analog-to-Digital Converter (ADC), which is usually located at the end of each column. The first developed Digital Pixel Sensor (DPS) was reported by *[FOWLER 1994]*, where an ADC and a memory node are implemented per pixel as shown in Figure 1-8. Integrating the ADC per pixel increases the Signal-to-Noise Ratio (SNR) by reducing readout noise, it increases the Dynamic Range[4] (DR) since the signal swing is not limited by the supply, and allows high speed imaging (>10 kfps *[KLEINFELDER 2001]*). However, adding the ADC and memory per pixel inevitably increased drastically the pixel size and lower its FF due to higher transistor count per pixel. For this reason, DPS are not used in consumer electronics market. Nevertheless, with the CMOS technology scaling, the FF of DPS improved. Also, obtaining a digital output allows increasing image processing functionality which made these pixels adequate for smart pixel applications, as discussed in section 1.3.2.1.

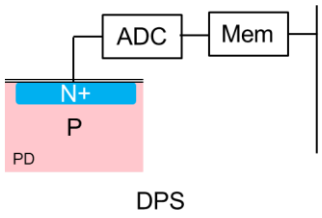

Figure 1-8: Standard DPS architectures

[3] Image lag is due to incomplete reset and thus results in presence of information from the previous frame
[4] Range of light intensities the sensor can detect and discriminate. It will be defined in detail in later sections.

1.1.2.4. Standard pixel operation

Figure 1-9 below shows the basic 3T APS voltage output, where the operation sequence is indicated and consists in three phases:

1. Reset phase (reset transistor ON) where the photodiode voltage is set to a reference voltage Vref.
2. Exposure phase (reset transistor OFF), where the photons are integrated in the photodiode capacitance during a fixed integration time (t_{int}).
3. And readout (SEL and SF ON), where the voltage level is sampled and further processed at the column, chip, or off chip level.

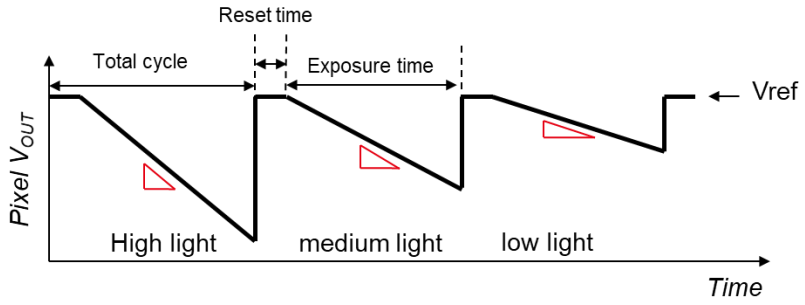

Figure 1-9: standard CIS operation

Depending on the type of pixel and its response, more phases might be implemented. For example, a double reset scheme is used to perform noise canceling (CDS) in most sensor designs. Also, depending on the t_{int}, more or less charges are collected which will affect the sensitivity and DR. An illustration of the ideal response vs optical power of a linear APS is illustrated in Figure 1-10 below. An ideal DR would be the whole intensity range before saturation, however, the minimum detectable level will depend on noise, as will be explained in further sections.

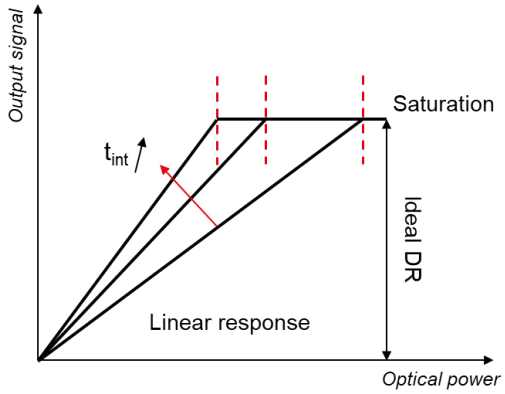

Figure 1-10: simplified illustration of linear image sensor response for different t_{int}

1.2. Pixel design: key parameters and architectures

In this section, the main pixel sensor properties are presented. The discussion will include the geometrical, electrical and optical properties. The point is to be able to compare the different architectures proposed in the next section based on the presented properties.

1.2.1. Pixel parameters

1.2.1.1. Size & Fill Factor (FF)

As previously mentioned, one of the main advantages of using CMOS compatible technology is the reduction in size following the scaling law *[DENNARD 1974]*. As shown in Figure 1-11, due to the shrink of transistor gate length and development of advanced process node, the pixel size was reduced, and the power consumption lowered. Today, commercialized consumer electronics pixels are in the micron range. However, the CMOS process evolution could not be directly used in CIS. The high leakage at small dimension, and the dielectrics used in Back End Of Line (BEOL), are some of the reasons that led to the development of a process specific to CIS. As can be observed on Figure 1-11, there is a gap between the CIS process and the main stream CMOS process of about three generations *[THEUWISSEN 2007]* however the scaling rate is almost identical.

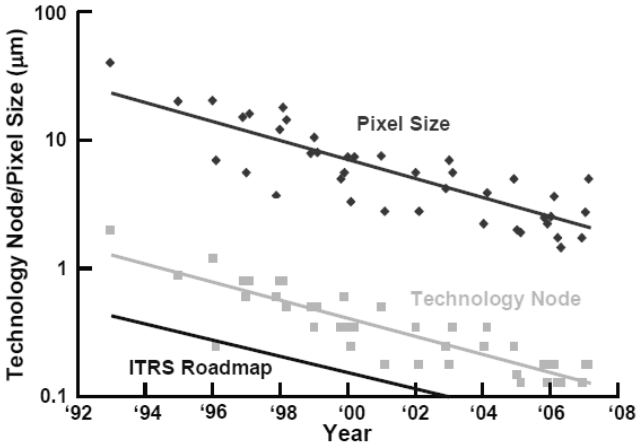

Figure 1-11: scaling of APS [THEUWISSEN 2007]

Also, using Front Side Illumination (FSI) configuration where the pixel is illuminated from the top through the metal layers, with the increase of pixel density the metallization design has become more difficult to deal with. The distance between metal lines is shortened and the light path focused by the micro-lenses might get reflected on the metal lines which causes crosstalk. Therefore, other solutions have been proposed such as integrating waveguides between the microlens and the photodiode to obtain better focus of the light *[AGRANOV 2009][LEE 2019]*. However, the best solution came as a natural evolution, consisting in Back Side Illuminated (BSI) sensor, where the light is incident on the back surface of the sensor after thinning it down. The BSI process is discussed in more details in section 1.2.2.1 and in Chapter 4.

The reduction in pixel size results in better spatial resolution at the expense of lower sensitivity. Also, the Signal to Noise ratio (SNR) will be lower due to smaller pixel area and thus less photon absorbed. Reducing the pixel size will also affect the Full Well Capacity (FWC) and thus the DR. All these parameters will be presented in the following sections.

Another important parameter related to the pixel size and scaling is the Fill Factor (FF). FF is defined as the ratio or percentage of photosensitive area to the total pixel area (Figure 1-12.a). It represents how much of the total pixel area

is used to collect photons, or inversely the area that is shadowed by either transistors or metal lines. A high FF results in a higher sensitivity since more charges are collected by the pixel, therefore it should be maximized. Since the pixel transistors followed the scaling law, their dimensions were reduced which allowed the improvement of the FF. To overcome the reduced FF, micro-lenses are added to the pixel to focus the light on the photodiode area and reduce optical cross talk between pixels as illustrated in Figure 1-12.b.

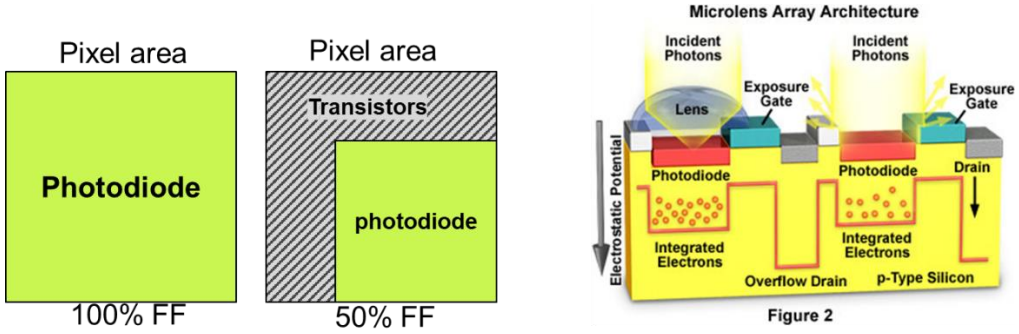

Figure 1-12: a) Schematics showing the reduction of FF by adding transistors/pixel b) The use of micro lenses to increase the FF [HAMAMATSU]

1.2.1.2. Sensitivity & Quantum efficiency

The sensitivity of a linear response sensor such as the 3T-4T APS, is defined as the slope of the transfer function in V/lux.s or e^-/lux.s. It represents the potential change for a given light intensity and integration time. Therefore, it is highly dependent on the Quantum efficiency (QE) of the sensor.

The QE is what quantifies how efficiently the incident photons are collected and converted to electrons. It is wavelength dependent since it depends on the absorption of the photosensitive material, but also accounts for all the optical loses that might occur due to reflection, refraction, and absorption of the incident light before it reaches the photosensitive area. To maximize it, anti-reflecting coating are used, and the stack between the surface of the sensor and the photodiode is optimized to avoid reflections at the interfaces. Also, the reflections on the metal lines must be minimized when using FSI. For example, using microlens greatly improves the QE and thus the sensitivity of the sensor. Using BSI improves the QE by avoiding these reflections.

1.2.1.3. Dynamic Range, Conversion Gain, and Full Well Capacity

a) Dynamic range

The dynamic range (DR) is what quantifies the range of light intensity detectable and measurable by the sensor. It is calculated as the ratio between the highest detectable signal (S_{max}) and the lowest detectable signal (S_{min}) limited by the noise floor. It can be expressed as:

$$DR = 20 * \log\left(\frac{S_{max}}{S_{min}}\right) \quad (1\text{-}1)$$

A high DR is desirable to ensure image quality at the low and high end of the scene intensities. It is limited at the low end by noise, and at the high end by Full Well Capacity (FWC) and pixel saturation. Common linear pixel sensor

exhibits a DR of about 60dB. The human eye DR is >150dB due to an intrinsic logarithmic response *[SUDHAKARAN 2012]*. In section 1.2.4, different sensor architecture that were proposed to enhance the DR are presented.

b) Conversion gain

The conversion gain (CG) is what characterize the charge-to-voltage conversion. It is measured in V/e^-, and thus is dependent on the capacitance of the photodiode. A high CG is desirable to increase the sensitivity especially at low light. It can be expressed as:

$$CG = \frac{\Delta V_{out}}{N_e} \tag{1-2}$$

Where ΔVout is the pixel output (V_{out_light}-V_{out_ref}) as a response to N_e electrons. N_e will depend on the QE and the photon flux. We can also express this equation as:

$$CG = \frac{\Delta Q}{N_e * C_J} \tag{1-3}$$

From (1-3) we can see the dependence of the CG on the junction capacitance C_J which will constitute a compromise with DR as will be explained in the next section. These equations are quite simplistic. In practice, the CG is measured by considering the photon shot noise and dividing it by the mean of the pixel output signal.

c) Full well capacity

The Full Well Capacity (FWC) represents how many charges can be detected before the sensor saturates and is measured in number of charges. It will determine the DR of the sensor. When the noise is not considered, and to get a rough idea of the number of charges that the well can contain, the following equation can be used:

$$FWC = \frac{C_J * V_J}{q} \tag{1-4}$$

Where C_J is the diode capacitance, V_J the applied voltage across the junction and q the elementary charge. From (1-4) we can see that increasing the capacitance increases the amount of charges that can be collected. However, increasing the capacitance will also decrease the CG. The higher is the FWC the higher is the DR, however, the loss in sensitivity due to the reduction in CG will decrease the range at the low intensity end. This results in the well-known DR/sensitivity tradeoff. Also, with the reduction of pixel size, the capacitance of the photodiode is also reduced, which negatively affected the FWC.

1.2.1.4. Noise parameters

Signal-to-Noise Ratio (SNR) represents the ratio of the useful signal to the unwanted parasitic signals. It is what defines the image quality. Therefore, it should be as high as possible, by increasing sensitivity and CG, but more importantly, by decreasing the noise. To understand the importance of the SNR, the main noise sources in a pixel are introduced.

The noise sources in an image sensor can be divided into the following categories:

- Temporal noise: this includes photon shot noise, dark current shot noise (Q_{shot}), amplifier flicker 1/f noise, and reset kTC noise (Q_{reset}).
- Spatial noise: mainly Fixed Pattern Noise (FPN) (Q_{FPN}) that includes Dark FPN, the pixel source follower FPN and column FPN.
- System noise: more related to readout ($Q_{readout}$), such as line noise and crosstalk, as well as ADC quantization noise.

The total pixel noise is the sum of the mentioned components and can be expressed as:

$$Q_n = Q_{shot} + Q_{reset} + Q_{readout} \tag{1-5}$$

The FPN contribution (Q_{FPN}) is not included in 1-5 since it can easily be corrected using CDS techniques, as presented in section 1.2.1.4.d. As illustrated in Figure 1-13, dark current noise is dominant at low illumination, while the shot noise, particularly the photon shot noise that increases with the signal, is dominant at higher light intensities. We will define in more details the major contributor to pixel noise in our case: dark current, reset kTC noise, and FPN.

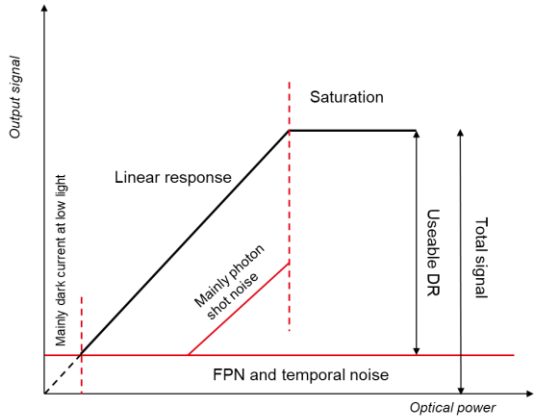

Figure 1-13: simplified illustration of CMOS APS output voltage curve with the main noise components

1.2.1.4.a. Dark current

Dark current results in the unwanted output signal when no light is applied and therefore is not due to photogeneration but to thermal generation. The major causes of dark current are the defects generated in the lattice during fabrication, that generate traps at the interfaces (Si/SiO_2), the recombination due to drift in depletion region, and diffusion in the quasi-neutral regions of the diode. Dark current has always been a source of noise that is very tricky to deal with since it is not fully understood. It is highly dependent on temperature variations due to its thermal SRH (Shockley-Read-Hall recombination) component. To account for the dark current, dark pixels, or pixels that are shielded from the incident light, are implemented to measure the dark current variation and apply a correction algorithm to the image. Another way to reduce the dark noise is to subtract a dark frame from the following frames. This takes into account the dark signal dependence on integration time and gain; however, it doesn't consider the temperature increase. The improvement in process technology and the development of different techniques to reduce it allowed the improvement of the dark signal. Initially dominated by the surface and interface states, it was drastically improved by introducing

the pinned photodiode where the pinning layer passivated the interface states *[TERANISHI 1982]*. Using advanced nodes, it is now in the range of tens of pA/cm² for pixels smaller than 4µm as shown in Figure 1-14 *[MCGRATH 2017]*.

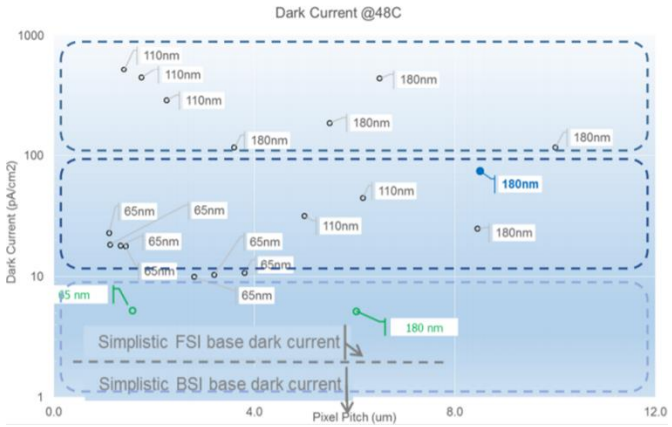

Figure 1-14: dark current values for major CIS manufacturer vs pixel pitch [MCGRATH 2017]

1.2.1.4.b. Reset kTC noise

The thermal noise resulting from the reset operation is commonly called reset noise or kTC noise. It results from the resistive nature of the reset transistor that switched the capacitive node. Considering the 4T APS, this node is the floating diffusion node. As all thermal noise voltage, it can be defined as:

$$V_n = \sqrt{kT/C} \tag{1-6}$$

It is measured in V_{rms}, where *k* is the Boltzmann constant, *T* the temperature in Kelvin, and *C* the integration node capacitance. It can also be measured as an amount of charge in Coulomb as:

$$Q_n = \sqrt{kTC} \tag{1-7}$$

Therefore, the kTC noise decreases with temperature. To reduce the charge kTC, the capacitance must be reduced (opposite for voltage kTC). Reducing the capacitance also increases the CG, however there is a tradeoff. The lower capacitance value increases the necessary supply voltage. In 4T APS, with the introduction of the pinned photodiode, and the use of true CDS, the reset noise can be almost completely canceled. Also, the use of fully depleted node reduces considerably the kTC noise by reducing the capacitance.

1.2.1.4.c. FPN

The fixed pattern noise is a spatial noise resulting from the mismatch between pixel parameters due to process variations. It either results in a variation in gain or an offset. For standard APS circuit, it can be divided as: 1) pixel FPN which includes FPN due to photodetector variation (ex: area, C_J etc), and the amplifier variation (V_T, W/L ratio etc), 2) the column FPN due to column current bias variations.

The offset FPN can be extracted by measuring the variance of the output voltage under uniform illumination condition (including dark) without including the temporal noise and is not signal dependent. The gain FPN however, increases

with the signal since it is defined by the variance of the pixel gain times its photo response. The FPN is given in % of output voltage swing or % of well capacity. The gain FPN which includes DSNU (dark signal non-uniformity) and PRNU (pixel response non-uniformity) is more complex to address than the offset FPN. The offset FPN can easily be removed using CDS techniques (next section), while the gain FPN has to be minimized by using process integration techniques to reduce its major sources such as dark current.

1.2.1.4.d. Correlated Double Sampling (CDS)

Correlated double sample (CDS) is a technique widely used to remove constant noise component in analog signal by sampling it twice and calculate the difference *[KIM 2015]*. It was first introduced in the 70s for CCD and later implemented in CIS to remove FPN offset noise, reset noise and in some cases, flicker noise. A basic CDS circuit is illustrated in Figure 1-15. The 4T APS architecture allowed the use of CDS to remove reset noise by sampling the FD first just after reset, and second after transferring the charges at the end of the integration time. However, it does not reduce the dark current noise.

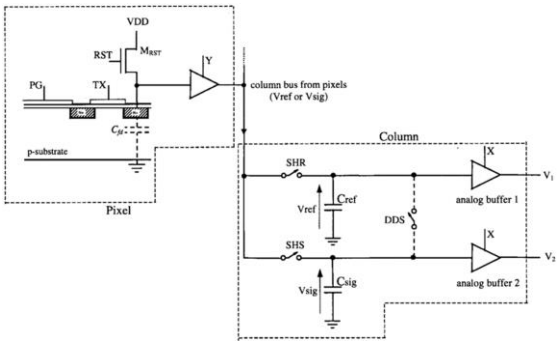

Figure 1-15: typical CDS circuit for 4T APS [DEGERLI 2000]

1.2.2. Process integration optimization

1.2.2.1. Back Side Illumination

The BSI integration consists in flipping the sensor so that the light will be incident directly on the photodiode without going through the BEOL of the pixel (Figure 1-16). The process was first developed in the 70s but was reserved to specific application that required higher QE such as astronomy imaging. It became mainstream for high end consumer application when the pixel size decreased below 2µm, motivated by the mobile phone market, where higher resolution at the same sensor size is required *[IWABUCHI 2006][PAIN 2005][WUU 2009]*. When FSI is used, the optical path will include the total thickness of the BEOL. The reflection on the metal lines induced losses and crosstalk between pixels. The optimization of the FSI BEOL techniques *[COHEN 2006]* were no longer enough to adjust to the scaling of the CMOS technology and reduction in pixel pitch, making the distance between metal lines shorter and shorter. Therefore, BSI came as a natural solution to increase the QE, but also to allow the use of more advanced standard BEOL technologies. A comparison between FSI and BSI sensors is shown in Figure 1-16. The industries developed foundry compatible processes, and thanks initially to the contribution of Sony and Omnivision, this technology is now mainstream. The first to implement BSI in mobile phone cameras were OmniVision in 2007 *[RHODES 2009]*. Today, more than 50% of the mobile phone market implement BSI *[YOLE DEVELOPPEMENT 2017]*.

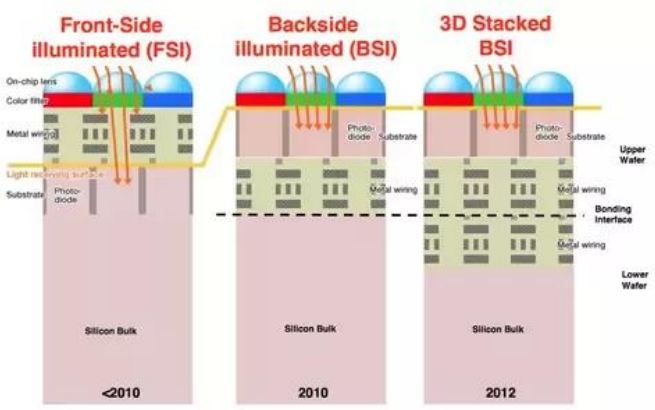

Figure 1-16: FSI vs BSI CMOS APS structures [YOLE DEVELOPPEMENT 2017]

In chapter 4, we will discuss in more details the available process flow for BSI and evaluate the implementation of this technique for our sensor.

1.2.2.2. 3D stack

Today's industry shifted to the 3D stack process integration which allows the integration of the CMOS processing part on top of the pixel (Figure 1-16). The advantage being the possibility of using more advanced technology nodes for the processing circuit. Since 2010, the trend is the combination of BSI and 3D stack to reach ultimate pixel size/performance tradeoff. Also, combined with BSI, it allows the addition of more functionalities without deteriorating the FF. Recently, Sony announced their 3-level 3D stack image sensor *[HARUTA 2017]* composed of the back illuminated pixel array, a DRAM level, and the digital processing level (Figure 1-17). The proximity of the DRAM allows fast processing and fast frame rate.

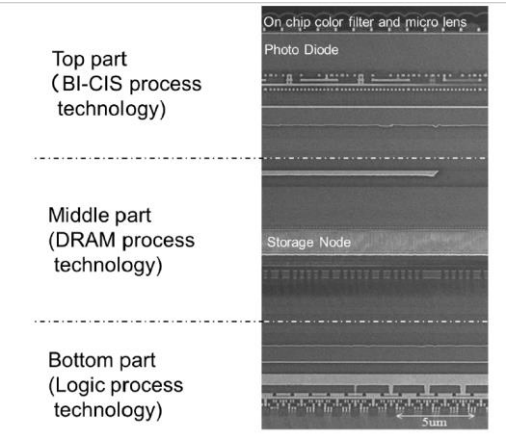

Figure 1-17: 3-level stack image sensor [HARUTA 2017]

1.2.3. Small pixel architectures

As mentioned before, the scaling of CMOS technology is what allowed CIS to be dominant on the mobile imaging market. For this reason, pixel architecture that requires a smaller number of transistor while keeping high performance were developed. Here we present the industry standard and the pixels featuring one transistor per pixel (1T APS), a category we will later benchmark our sensor to.

1.2.3.1. Shared transistors architecture

As one of the main advantages of CIS over CCD is the scalability, research was driven to reduce the pixel size to the submicron scale, by reducing the number of transistors per pixel. An architecture that was developed in early 2000s and became today an industry standard is the shared pixel architecture *[McGrath 2005]*. In this design, the FD node of 2 to 4 pixels are connected and they share the same reset transistor (RST), source follower (SF), and row select (SEL). A two transistor (2T) per pixel architecture was developed *[Chow 2001]* where the FD, reset, and SF are shared between 2 pixels and the row selection is performed by the TX. Also, a 1.75T pixel was developed *[Cohen 2006][Mori 2004][Wakabayashi 2010]* in which the FD, reset, SF, and SEL transistors are shared between 4 pixels as shown in Figure 1-18. This architecture is the standard architecture used in industry. And finally a 1.5T is also available *[Cohen 2006][Takahashi 2004]* that is similar to the previous one only the SEL transistor is removed.

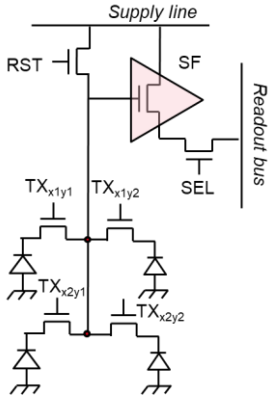

Figure 1-18: 1.75T shared architecture pixel sensor

Using a sharing architecture comes with some drawbacks. The first and most evident is the loss of symmetry which will increase the mismatch in performance between the different pixels. Another problem is the FD capacitance that increases since it is shared. Increasing the FD capacitance negatively impact the conversion gain (CG) of the sensor. However, these problems are corrected using noise canceling techniques and boosting architectures as proposed by *[Wakabayashi 2010]*.

1.2.3.2. 1T pixel sensors

The ultimate pixel size shrinking would be to use only one transistor (1T) per pixel. Several technologies were proposed along the years. In the 1T pixel architecture, only one transistor is used for all the phases of integration, readout, and reset. Depending on the bias applied on the transistor, the pixel operation can be controlled. Here we are presenting some of the most promising technologies developed, and later in the manuscript, we will benchmark the FDPix, which falls in that category.

One of the most promising 1T pixel is based on using Charge Modulation Device (CMD) proposed by *[Hynecek 1991][Matsumoto 1991]* initially to replace the CCD for high density imagers. It was later studied also by STMicroelectronics *[Tournier 2007a][Tournier 2006][Tournier 2008]*. The concept is based on charge accumulation and transistor characteristics modulation in an N-type MOSFET bulk. A floating P- (or N depending on transistor type) zone is implanted under the channel of the MOSFET, it is surrounded by N-Well implants that are

connected to the drain of the transistor (Figure 1-19.a). When the device is under illumination, photogenerated electrons are driven towards the drain area, and the holes accumulate in the potential valley created by the floating P-Well. This accumulation of charge will induce a potential change that modulates the V_T of the transistor. The source voltage is thus modulated and can be readout and sampled. The reset phase is performed by applying a bias on the gate to remove the potential well and evacuate the charges toward the substrate. This allow the reduction of the reset noise and suppresses the image lag. It is a CMOS compatible process and thus reduces the cost effectively.

Recently, Fudan university conducts research on using SOI structure as 1T pixels. *[LIU 2015]* proposes the use of a floating gate-floating diode concept where the photogenerated charges are accumulating in the floating gate and modulate the drain current. Although high responsivity is achieved, the structure is rather complex to realize. More recently, the FDSOI transistor back biasing was investigated as a 1T pixel sensor. In *[DENG 2017][WAN 2018]*, a high back bias is used to create an inversion layer on the back channel of the FDSOI as shown in Figure 1-19.b. When illuminated, the photogenerated charges in the channel will accumulate at the gate/channel interface. This accumulation of charge will induce a potential that changes the back-channel characteristics and thus modulates the transistor current. And finally in *[CAO 2018]*, a high back bias voltage is applied to deplete the low doped substrate. The depletion region will act as a potential well where the photogenerated charges in the bulk will accumulate and modulate the transistor V_T. The same group also proposed a configuration where a pseudo-MOS is used *[ARSALAN 2018]*. High responsivity is achieved, however the high applied back bias needed for these architectures render the device difficult to implement in CMOS circuit.

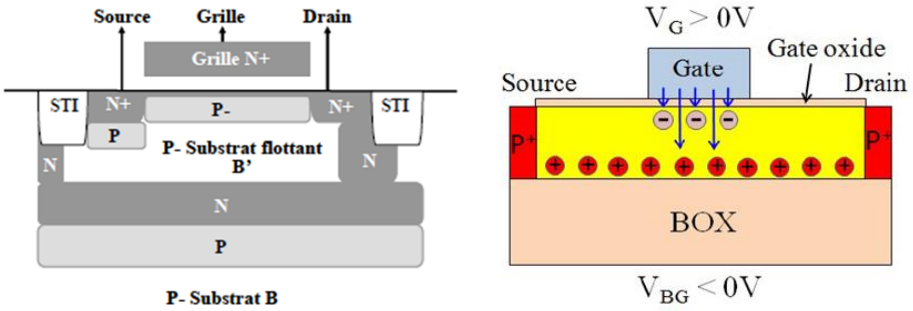

Figure 1-19: a) CMD based 1T pixel as proposed by [TOURNIER 2007B] *b) FDSOI based channel coupling as proposed by* [DENG 2017]

Another solution using a Tunnel FET (TFET) was investigated by *[NIRSCHL 2005]* and more recently by *[DAGTEKIN 2015]*. A TFET transistor junction is used to detect light illumination and modulate the transistor current in a phototransistor fashion. However, the voltage bias used are higher compared with other 1T solutions.

Other proposed 1T structure are based on using other materials than Silicon. For example, in *[OKYAY 2007]*, they use photogeneration in a depleted Germanium gate to modulate the transistor drain current. Since the photo-absorption is the Germanium, they obtain a photosensitivity in the infrared range, compatible with optical telecommunication. They also suggest its implementation as an inverter to optically control latches which is a concept we explored and is presented in chapter 5. *[GUO 2016]* proposes a 1T device also based on SOI FET back side coupling effect, however, in the proposed integration, the channel is in graphene. The photogeneration and accumulation of charges at the

BOX/substrate interface will result in back biasing the graphene channel. Since graphene mobility is much higher than Si, the corresponding measured current is much higher than the initial photocurrent.

All the previously discussed devices properties are summarized in Table 1-1. At the end of the manuscript, we will compare out 1T device performance with the previously discussed architecture.

Table 1-1: reduced of transistor /pixel architecture summary

	Units	1T pixel sensor					Shared architectures			
		[Tournier 2007A]	*[Tournier 2008]*	*[Arsalan 2018]*	*[Liu 2015]*	*[Cao 2018]*	*[Mori 2004]*	*[Cohen 2006]*	*[Wakabayashi 2010]*	*[Chow 2001]*
tech node	*µm*	0.18	0.13	-	0.18	-	0.25	0.13	0.14	0.35
pixel pitch	*µm*	2.2	1.4	-	-	-	2.25	1.75	1.65	8
T/pix	*#*	1	1	1	1	1	1.75	1.75	1.75	2
FF	*%*	46	50	-	-	-	-	-	-	49
VDD	*V*	3.3	1.2/3.3	V_{BG}=18V	1-2V	V_{BG} high	2.5	-	-	3.3
CG	*µV/e- or /h+*	47	58	-	19.2	-	-	70	75	-
FWC	*e- or h+*	3500	2000	-	-	-	5000	8000	9130	-
Idark	*e-/s or h+/s*	-	39.7	-	-	-	-	25	3	10 (pA)
sensitivity	*e- or h+/lux.s*	-	590	-	-	-	3800	5000	9890	-
DR	*dB*	40	52	-	-	-	-	-	71	-

1.2.4. Pixel architectures for DR extension

As discussed in section 1.2.1.3, the DR is of major importance for the sensor to operate under a wide range of illuminations. In this section, we will focus on the logarithmic, and linear-logarithmic pixel sensors since the present device under study is in this category, and therefore will be benchmarked to the available technologies. We also briefly mention more general techniques used with linear sensor for Hight Dynamic Range (HDR) applications.

1.2.4.1. Logarithmic pixel sensor

The human eye covers a wide DR of more than 150dB, mainly thanks to its logarithmic response. To mimic this response and avoid the need of signal processing, sensors exhibiting an intrinsic logarithmic response were developed. One of the first demonstrations of such a pixel was presented by *[Chamberlain 1984]*. As most developed logarithmic APS, it is based on the relation between the MOSFET drain current and gate voltage in subthreshold. Such a structure is shown in Figure 1-20. The log response is due to the logarithmic dependence of the MOSFET subthreshold current as shown in (1-8) below:

$$I_{PH} = I_{dark} e^{\left(\frac{V_{GS}-V_T}{nV_{th}}\right)} \qquad (1\text{-}8)$$

Where I_{PH} is the photocurrent, I_{dark} is the dark current, V_{GS} the MOSFET gate to source voltage, n is the body effect, and V_{th} the thermal voltage. This type of pixels resulted in DR reaching 140dB *[Kavadias 2000][Loose 2001]*. However, due to the operation of the transistor in subthreshold, the response is highly dependent on V_T variation resulting from process variability. This will induce a large FPN *[Joseph 2007]* which is the major drawback of this technology. Also, since the sensor operates in a continuous readout fashion (no integration), flicker noise is high, and standard CDS techniques cannot be implemented, which eventually results in poor low-light sensitivity. And finally,

the small output voltage swing due to logarithmic compression reduces the image contrast sensitivity. However, they do find applications in the field of bio-inspired vision sensors such as artificial retinas.

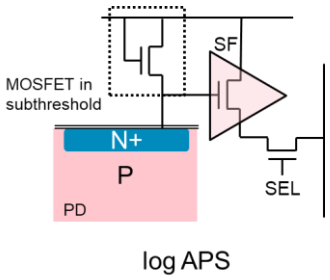

Figure 1-20: Standard logarithmic pixel architecture

Other techniques to generate a logarithmic response based on using the diode in photovoltaic mode were developed *[MATOU 2001][NI 2011]*. They are based on measuring the open circuit voltage of the diode that naturally has a logarithmic dependence on the photocurrent. This technique has been the basic component of Yang Ni's work that resulted in being commercialized by NIT. Due to the wide range of application where a high DR is required, several techniques to improve the logarithmic pixel performance, mainly regarding FPN were developed *[LAI 2004]*. Also, since they exhibit poor low light sensitivity, new sensors combining both linear and logarithmic response were developed as presented next.

1.2.4.2. Linear-Logarithmic pixel sensors

To account for the poor sensitivity at the low light end of logarithmic pixels, while keeping the high DR, linear-log pixels were developed *[BAE 2016][CHOU 2014][TU 1998]*. These pixels exhibit a linear response at low light intensities which improves the sensitivity, and logarithmic response at high light intensity to maintain the high DR. An example of such pixels is proposed by *[VATTERONI 2008]* where a MOS cascode is added to the 3T pixel to obtain a logarithmic response, resulting in a DR of 112dB. Later the same technique was adopted by *[BAE 2016]* where two linear responses are obtained with a logarithmic response at the high intensity end. A linear-logarithmic sensor was commercialized by NIT *[NI 2018]*. This pixel is based on exploiting the photovoltaic region of operation of the photodiode to obtain the logarithmic response *[NI 2017][NI 2011]*.

The main problem of these pixels resides in FPN noise and pixel size, since adding functionalities requires more transistors. However, due to the real need of such sensors, many recent researches have been focused on techniques to suppress the FPN noise. The table shown below summarizes a few of the published work on logarithmic and linear-logarithmic sensors.

Table 1-2: logarithmic and linear-logarithmic publications

Author	*Units*	*[Miyatake 2007]*	*[Bae 2016]*	*[Rhee 2005]*	*[Lee 2013]*	*[Bae 2016]*	*[Chou 2014]*	*[Ni 2001]*	*[Storm 2006]*	*[Guo 2009]*	*[Vatteroni 2008]*	*[Lee 2013]*	*[Ni 2011]*
tech node	***µm***	0.18 (CIS)	0.35	0.5	0.5 (CIS)	0.35	0.18	0.8	0.18	0.5	0.35	0.13 (CIS)	0.35
pixel pitch	***µm***	12	10	20.7	2.25	13	6	30	5.6	23.4x 27.15	9.4	2.25	10
#T/pix		7 +1 capa	5	6	2.5	4	5	4	7	7	5	4T std	-
FF	***%***	38	28.4	34	-	15.3	-	-	33	24.56	30	-	30
VDD	***V***		3.3	5	3.3	3.3	3.3	-	-	-	3.3	3.3	-
FPN	***% or mVrms***	2.6	0.95	-	-	-	1.96	12.26	4	23.88	1.39	0.58	<1.5 mV
sensitivity	***mV/dec***	60	70	48	90lsb	-	55	53	77	79.98	-	90lsb	90
	/lux.s	9.7V	257/5 1 mV	-	-	-	651m V	-	-	-	-	1804 lsb	3V
DR	***dB***	190	>106	94.8	105	97	143	>120	143	121.26	112	105	>120

1.2.4.3. Others HDR techniques

The DR of the standard 4T APS can be extended by optimizing the reset and readout steps and keeping the same intrinsic DR. The most known techniques are the Well capacity adjustment *[Yang 2000]*, multiple capture where picture taken using different integration time are combined *[Gao 2015][Meylan 2006]*, and time-to-saturation using DPS architectures *[Stoppa 2002]*. The purpose is to extend the DR at the high end since standard APS have very good low light performance. The well capacity and self-reset consist in avoiding reaching full well capacity, i.e. saturation, by resetting to remove a proportional amount of charges. Multiple capture and time to saturation require the dependence of the integration time on photocurrent. The multiple capture for example, which is the most widely used technique today, consists in taking dual or multiple pictures per frame using different integration times, and combine them to obtain the HDR picture (technique called Tone mapping).

All these techniques have the drawback of requiring some sort of on-chip processing of the signal to obtain the final HDR picture while in the previously discussed structure, the output voltage has a direct logarithmic dependence on the photocurrent, and thus the logarithmic compression is obtained without the need of extra circuitry.

In the next section, some of the most trending image sensor applications are briefly presented. The idea is to identify the need of the future technologies regarding pixel architecture and performance.

1.3. Technologies and applications

Considering the main market i.e. smartphones, more and more sensors will be embedded in these devices in the near future. Three main types are i) High resolution since the smartphone camera are expected to have almost the SLR (Single-Lens Reflex camera) quality with a smaller sensor size, ii) the 3D imaging already implemented for facial recognition, and iii) motion detectors to increase user interactivity. Also, automotive is a major sector for CIS. The main sensors today implemented in cars for example are visible light sensors, 3D sensors, night vision and LiDAR (Light Detection And Ranging). On top of that with the development of ambient intelligence, more sensors such as motion, proximity or ambient light sensors will be implemented *[PAUWELS 2007]*. This will also lead to the development of smarter image sensors that consume very low power.

For visible imaging, the 4T pixel is the one used today by most industrials. Combined with BSI and 3D stack, its sensitivity can go down to the photon counting. Depending on the application, the restriction on the sensor size and power consumption will vary. For example, for mobile phone, the main demands are small size and low power consumption, compared with automotive applications where the DR and reliability is of higher importance. In this section, we will briefly introduce these technologies and the type of sensors used.

1.3.1. Time of Flight (ToF)

Time of Flight (ToF) imaging is a range finding technique *[HORAUD 2016]*. It consists in sending modulated laser pulses or continuous wave (usually in the NIR or IR range) and measuring the time it takes the signal to travel back and forth to hit the receiver. By measuring this time, the distance of the objects can be calculated using the simple equation:

$$distance = \frac{1}{2} * c * t \qquad (1\text{-}9)$$

Where c is the speed of light and t the calculated time at the receiver as illustrated in Figure 1-21.

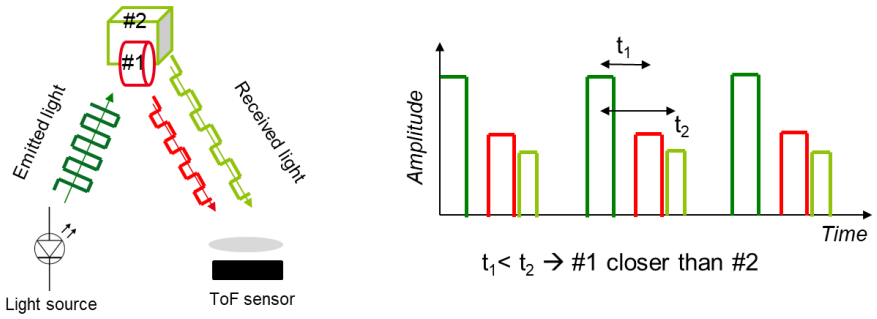

Figure 1-21: ToF principle schematic

Other technique do exist for range finding such as structured light used for facial recognition for example, or laser triangulation *[ABOALI 2017]*, however, ToF being more compact, low cost, and allow high speed detection, it is becoming the technology of choice to implement range finding applications *[LI 2014]*. These applications include 3D imaging, facial recognition, proximity sensor, LIDAR, and others where the information needed is the distance of the

object from the receiver. One of the advantages of ToF technique over its competitor is the use of a standard CMOS array as the receiver. The commonly used technology is the Single Photon Avalanche Photodiode (SPAD) that offers an ultra-high-speed, high precision, and almost no noise detection necessary for pulsed based ToF. A SPAD consists in a photodiode operating in the Geiger mode near the avalanche breakdown. In this region, a single photon absorbed can cause avalanche breakdown and a flow of electrons *[PERENZONI 2016]*. Since the light reflected back to the sensor is usually very low (~photons), a SPAD is necessary. Other receiver using 4T APS were also investigated *[ILLADE-QUINTEIRO 2015]*. The main demanded characteristics is an almost null dark current to obtain a high SNR.

1.3.1.1. Machine vision and 3D imaging

An example of machine vision application is facial recognition implemented today in smartphones. It can be performed by classical 2D imaging, where algorithms are used for edge detection and feature extraction. However, depth ranging has been preferred such as structured light technique as previously mentioned *[CHANG 2008]*. ToF is also a good candidate due to its immunity to the possible shadowing, since it detects a change in delay not in intensity, and to its higher frame rate. The ease of isolating the subject from the background and fast frame rate allowed ToF to be used in applications such as proximity sensors *[STMICROELECTRONICS]* or gesture recognition. A 2D depth map can be extracted from the 3D point data collected at every pixel in the receiver array, also, a 3D image can be reconstructed from these "point-cloud" data. An example of a 2D map and 3D image is shown below.

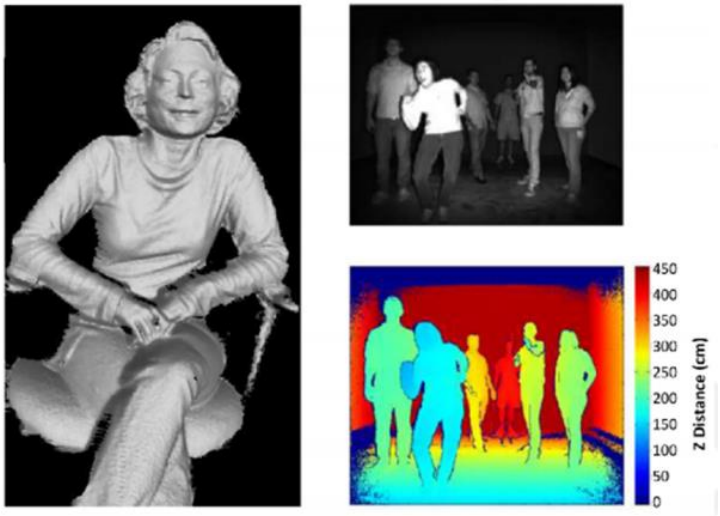

Figure 1-22: example of obtained ToF 2D and 3D images [QUINTEIRO]

1.3.1.2. LiDAR

LiDAR is a technology that has been widely used in domain such as geographical and atmospheric mapping, civil engineering, surveyance, and defense. Nowadays LiDARs represent one of the best solutions for robots and self-driving cars vision. It is also a main part of most Advanced Driver Assistance Systems (ADAS) *[YOLE DEVELOPPEMENT 2017B]*. It consists in illuminating a scene with non-visible non-harmful light source and reconstruct the 3D imaging based on ToF calculation. The most common type is the laser scanning LiDAR, where multiple laser pulses are incident on the scene and the reflections are detected. This technique requires mechanical rotation of a

mirror to properly direct the laser beam. Another type of LiDAR is called solid-state LiDAR, where in this case, the whole system (emitter and receiver) is manufactured on one silicon chip, and no scanning rotation is required. Since there is no rotation, the field of view of this technique is not as high as the laser scanning. However, due to their cheaper cost and smaller size, solid state LiDAR are expected to dominate the market in 2025 for more ADAS oriented applications *[WALFORD 2019]*. The laser source wavelength depends on the object and environment to be detected. The most common use Near Infrared Range (NIR ~900nm), since silicon can be used, it's relatively cheap to manufacture using common CMOS technology *[JARVIS 2018]*. Also, the detector used depends on distance of detection. For short distances for example, a standard photodiode can be used. For longer distances, a SPAD is required. An example of the image obtained from a flash LiDAR is shown below.

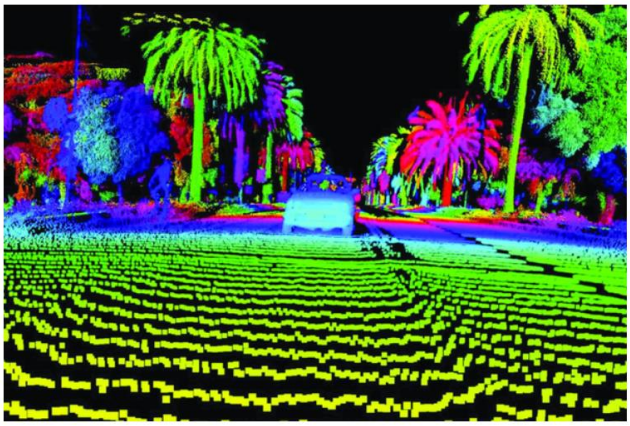

Figure 1-23: Example of a LiDAR reconstructed ToF image [LUMINAR 2017]

1.3.2. Computational imaging and smart sensors

Computational imaging englobes sensors where the signal detected is not used as such but processed with complex algorithms to obtain the final result. For example, since a distance is extracted, ToF requires image processing to obtain the final output, therefore it falls in the category of computational imaging. As the trend of adding more intelligence in the sensor continues, and with the rise of new applications with increased user interface and interaction such as Virtual Reality (VR) *[LIU]* Augmented Reality (AR) and also the development of Artificial Intelligence (AI), the computational imaging has become a priority. Depending on the technique, different sensors and applications are englobed in that category. We will here discuss an important option that is the event-based smart sensors for high speed and low power consumption imaging. They are retina-based sensors where the data are pre-processed locally, mimicking the biology retina operation *[TURCHETTA 2018]*.

1.3.2.1. Event based smart image sensors

The classical imaging can be classified as frame-based. When the image is taken, the whole pixel array captures the light. This will inevitably generate a lot of redundancy in data flow when the same scene without any variation is captured. This kind of redundancy cannot be tolerated in application where real time image processing is required such as autonomous cars. For this purpose, image sensors inspired by the retina operation were developed and are called event-based sensors *[LEÑERO-BARDALLO 2018][NI 2014]*. These sensors are designed using the DPS sensor discussed in section 1.1.2.3. The idea is to pre-process the signal at the focal plane of the array by adding functionalities

to the pixel, such as ADC and memory. In this case, the pixel size is not the issue since it is oriented towards high end application, however, with the use of 3D stack and BSI, this might change in the future years.

The basic functioning of an event-based sensor consists in generating the photocurrent during exposure, sensing a voltage that has a logarithmic dependence on photocurrent, comparing the voltage variation to a threshold, and releasing a pulse, i.e. an event, when that threshold is reached. Therefore, the information is transmitted in time domain. The advantages of such an architecture is the low data rate over a wide DR, and its low power due to transistor operation in subthreshold. In Figure 1-24, an example of such a circuit is given *[LICHTSTEINER 2008][POSCH 2014]*. We can see that it is composed of the photodiode circuit that mimics the photoreceptor, a deferential circuit and a comparator. The pixel signals are also shown. We can see that the analog logarithmic variation of the pixel response is represented as a series of spikes at the output. The change in analog voltage modulates the frequency of the spikes and the polarity of the spikes changes as a response to change in photocurrent (increase or decrease). Finally, an image of a moving person obtained with this event-based circuit is shown where the brighter pixel corresponding to positive increment of logarithmic voltage, and the darker pixels corresponds to negative variation. More details on the sensor can be found in the previously mentioned references. A comparison of different event-based architectures can be found in *[TURCHETTA 2018]*.

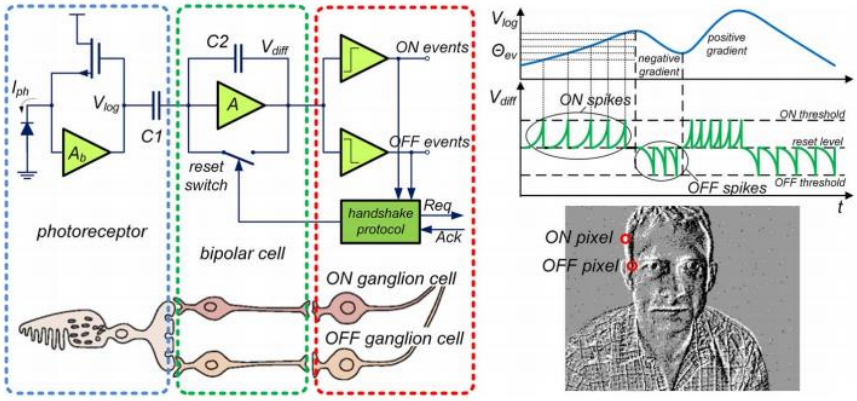

Figure 1-24: an example of event-driven circuit as presented in [POSCH 2014]

1.4. Chapter one summary

This chapter presented an overview of the current image sensor technologies and state of the art. The current market trends were first discussed. Then the standard pixel sensor architectures, namely the passive, active, and digital pixel sensor were introduced. The different sensor parameters were defined. We presented some comparison of sensors designed to optimize specific parameters that will be relevant to our work, such as size and DR. Finally, a discussion on trending applications such as depth ranging using ToF, LiDAR and smart sensors were briefly introduced.

The sensor technology demands depend on application. Considering the mobile, automotive and ambient intelligence market, ToF sensors will be widely used since they present the most compact, low price, and high accuracy compromise on the market. For implementing efficient ToF, the sensor must be ultra-fast response with high SNR. For application in automotive such as LiDAR, the DR must be maximized as well. Finally, the addition of processing in the pixel level allowed the development of smart sensors based on mimicking the silicon retina. These sensors present HDR, low power, and low data rate since the redundancy is eliminated by using an event-based architecture. They will benefit greatly from the pixel size reduction which will allow the decrease of total pixel area.

Throughout the manuscript, our sensor will be investigated based on the properties presented in this chapter and compared with conventional technologies. The DR, size, and process simplicity will be emphasized as the main properties of our design, which allow it to be considered for the mentioned applications. As presented in the introduction, the studied sensor is based on FDSOI technology. Thus, in the next chapter, the FDSOI technology will be first introduced in more details.

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CHAPTER TWO

Chapter 2 : New FDSOI based pixel sensor (FDPix)

Today, standard pixels contain 3 to 4 transistors per pixel, with a total area <1.5 µm². Decreasing the size negatively affected the sensitivity. As discussed in Chapter 1, Back Side Illumination (BSI) scheme and 3D stack processes contributed to overcome this drawback. Also, combining these two techniques allowed the addition of new functionalities by adding more transistors per pixel without decreasing the Fill Factor (FF). However, the process integration increased in complexity and cost. Nevertheless, today, the use of both techniques in image sensor industry is a standard approach. The inherited linear response of the conventional image sensors allowed the increase of the sensitivity at low illumination to the single photon counting but limited the Dynamic Range (DR) of the sensor to around four decades of intensity. To address the market of High DR (HDR) applications e.g. automotive, the logarithmic sensors were developed. However, their poor performance at low light and FPN noise as mentioned in Chapter 1, prevented them to break into the consumer market *[GAMAL 2005]*.

In this work, we conduct a study on the FDPix device; a single Fully Depleted Silicon-On-Insulator (FDSOI) transistor used as a light sensor. The one transistor (1T) pixel is obtained by monolithically integrating a photodiode in the substrate of an FDSOI transistor, using a standard fabrication process similarly to a 28nm FDSOI CMOS technology. The pixel structure is intrinsically 3D-like with the sensing element being on top of the photosensitive element, without using 3D stack process. Therefore, the structure is relevant for backside illumination operation, which allows the full advantage of advanced node process and obtains very small pixel size.

The device sensitivity to light is a result of a capacitive coupling that takes place between the photosensitive element and the sensing/reading transistor. The sensing node and the reading transistors are electrically isolated. The structure is such that, any semiconductor material allowing a p-n junction can be used as the photosensitive element, making this device adequate for any wavelength detection. Its intrinsic HDR, small size, and implementation using advanced nodes FDSOI technology, makes it an attractive choice for automotive and low power applications.

This chapter presents the main device structure and principle of operation. We will go more into details on the physical phenomenon at steady state and describe the modeling of the FDPix device in DC regime. The developed model is confronted to TCAD simulations and electrical characterization. After that, a detailed process flow is depicted. Finally, the last section discusses the complementary property (CMOS) of the FDPix.

2.1. FDPix: a new pixel sensor

2.1.1. Pixel structure description

Before getting into the particularities of the FDPix structure, the next section presents an overview of the FDSOI transistor, building block of the FDPix device.

2.1.1.1. Fully Depleted Silicon-On-Insulator (FDSOI) transistor

FDSOI is a planar technology that came as a solution to improve the bulk transistor performance and continue the scaling while maintaining a simple planar fabrication process *[FENOUILLET-BÉRANGER 2008]*. It was developed by LETI *[CEA 2017]* and commercialized by several industrial such as STMicroelectronics *[ARNAUD 2018]* , Samsung *[LOW 2016]* and Global Foundries *[CARTER 2016]*. The main addition that distinguishes it from the classical planar MOSFET using bulk substrate is the addition of a thin oxide layer called the Buried OXide (BOX) whose main function is to isolate the transistor channel from the bulk substrate. Isolating the channel prevents leakage currents and parasitic capacitances between the source/drain and the bulk. However, it is the Ultra-Thin Body and BOX (UTBB) architecture *[LIU 2010]* that unlocked the ultimate property of this technology: the adjustment of the threshold voltage (V_T) by applying a back bias to achieve the best tradeoff between performance and power consumption *[ARNAUD 2012][GRENOUILLET 2012][LIU 2011]*. The ultra-thin body allows the channel to be fully depleted and thus results in a coupling between the front and back surfaces of the channel. The BOX adds a capacitance that allows the control of the back-channel interface by applying a bias at the BOX/substrate interface. The FDSOI is in fact, a dual gate transistor, where the second gate is available due to a doped region below the BOX called the Ground Plane (GP) and Well as illustrated in Figure 2-1. As a result, the short channel effects (SCE) are reduced, the performance and power consumption are improved, and the minimum gate length is decreased, with respect to the bulk.

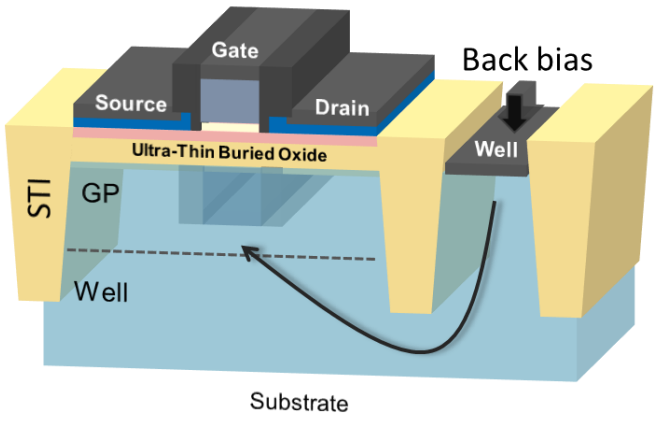


Figure 2-1:FDSOI transistor showing the back gate, GP, Well and the back-bias connection

The second gate (called back gate in this work) is defined by the GP and modifies its potential (V_B) through the Well. This is called back biasing (BB). Through capacitive coupling, the threshold voltage (V_T) of the transistor increases or decreases by applying a positive or negative potential on the back gate. Two options are available:

a) Forward Back Bias (FBB) by applying a positive V_B (negative for PMOS) and thus decrease the $|V_T|$ of both MOSFETs.
b) Reverse Back Bias (RBB) by applying a negative V_B (positive for NMOS) to increase the $|V_T|$ of both MOSFETs.

If we take the NMOS case, the FBB allows performance boosting of the MOSFET by increasing the "on" state current, while the RBB reduces its power consumption by decreasing the "off" state current (same thing for the PMOS). In addition, the UTBB architecture allows the calibration of the nominal V_T by controlling the GP doping concentration, with either p or n-type doping. Altering the doping type and/or the concentration results in different flavors of V_T, Low and Regular (LVT and RVT) are available for both N and PMOS transistor. When the transistor type is the same as the GP type, the device is LVT, opposite corresponds to RVT. For example, high performance applications like processor's core, only uses LVT devices, and for low power devices, RVT is preferred.

In this work, the 28nm UTBB FDSOI technology is used for implementing our device. Some specifications must be mentioned regarding the transistor:

- The body (channel) is 7nm thick, allowing full depletion and short channel effect reduction whatever the supply voltages.
- The channel is also undoped which reduces V_T variability and mismatch.
- The BOX is 25nm thick, and as mentioned before, enables efficient back biasing.
- Two V_T flavors are available, LVT and RVT.
- Two gate oxide (GO) thicknesses are available: GO1 with an EOT=1.6nm, and GO2 with an EOT=3.7nm.

Moreover, the device can be implemented using more advanced or relaxed nodes as long as the architecture (UTBB) is the same.

Apart from its excellent electrostatic control that allowed the scaling down to the 14nm node *[LIU 2014][WEBER 2014]*, FDSOI technology presents remarkable performance in RF and analog applications *[CARTER 2016]*. It has become the technology of choice for low power analog circuits as a result of the back biasing that offers an additional degree of freedom for circuit design using very low supply voltages *[CATHELIN 2017][FENOUILLET-BERANGER 2010][NOEL 2011]*.

For all the reasons aforementioned, the FDSOI appeared (and had proven) to be the right choice for the sensor design. In this work, we investigate the option of adding functionalities to the bulk of the FDSOI transistor. By integrating a photosensitive element, the V_T of the transistor varies with external light illumination. As a result, the FDSOI transistor can be used as an analog sensor device, in our case, a light sensor.

2.1.1.2. FDSOI/photodiode integration

The structure side view and TEM image are shown in Figure 2-2. It consists in an FDSOI transistor, where a p-n junction is monolithically integrated under the BOX, by modifying the ion implantation step of the GP, and the Well (the lower part of the substrate as shown in Figure 2-2). Different junction profiles are defined by choosing the right

dose and energy during this step to obtain a junction below the BOX and avoid residual dopants in the channel of the transistor. The complete process flow is presented in section 2.1.3.Transistors with no diode below the BOX (unipolar doping) are also fabricated for reference purposes.

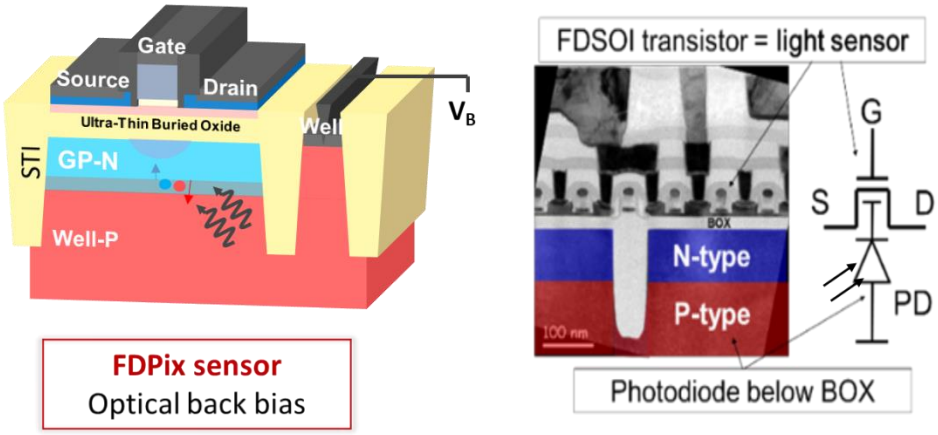


Figure 2-2: FDPix structure and TEM image

2.1.1.2.a. STI for pixel isolation

Standard FDSOI technology uses Shallow Trench Isolation (STI) to isolate the transistors from each other, which prevents latch up and minimizes leakage current. In FDPix, their main function of isolation is unchanged. We consider each transistor as a pixel where the STI defines the total area and prevents crosstalk between pixels. Therefore, the junction depth should not exceed the STI depth, which is about 300nm. The Si/SiO_2 interface defects generated during the process can increase the recombination and reduce the sensor's sensitivity. Therefore, as will be explained further in the process section, a thermal annealing is performed after the implantation to reduce the defects. Also, the Sa/Sb of the transistor, which are the distance between the poly gate and active edge, i.e. STI, at drain and source sides respectively, should be large enough for the STI interface to be far front the gate area where the coupling occurs.

2.1.1.2.b. Floating node and well connection for back bias

The GP is the sensing node of the FDPix. As indicated in Figure 2-2, the BOX on one side, and the junction depletion region on the other side isolate it, therefore it is electrically floating, allowing its potential to vary as a response to light illumination. This is a particularity of the FDPix device where no electrical connections to the sensing node are required for the device to work. Although the GP is floating, the Well connection inherited from the standard FDSOI is still available. In other words, the second electrical gate can also be used to bias the Well and modifies the GP potential. This Well connection allows the biasing of the photodiode in either reverse or forward to control the current passing through it. We took advantage of this second gate to reset the pixel as demonstrated in Chapter 3.

2.1.2. Operation Principle

2.1.2.1. FDPix and the Light Induced V_T Shift (LIVS)

The operation of the FDPix device relies on the capacitive coupling between the FDSOI transistor and its back gate (i.e. GP). As previously mentioned, the FDSOI V_T is modulated by applying a potential on the back gate. The source

of this potential variation in our case is the photogeneration of charges in the photodiode implemented under the BOX. When photons with energy higher than the band gap of Silicon (1.14eV) are absorbed in the PN (or NP) junction, the photogenerated electron-hole pairs are separated by the junction electric field. Since the GP is floating and the Well is at a fixed potential (e.g. V_B), the charges will accumulate at the BOX/GP interface. This is shown in Figure 2-3 where the band diagram of the FDPix device with NP junction is obtained using TCAD simulation. We can see that in this case, holes are evacuated through the well, and the electrons accumulate which results in shifting the bands upward. The change in carrier concentration at the BOX/GP interface induces a potential change analogous to the back bias, only here it is an optical back bias.

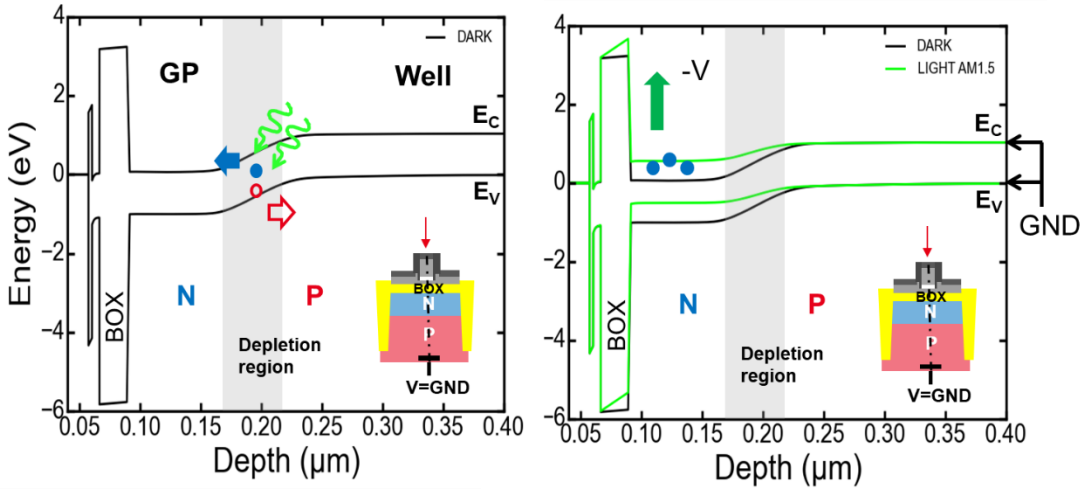


Figure 2-3: FDPix Band diagram across the gate showing the effect of photon absorption in the substrate (TCAD)

The optical back biasing will shift the transistor's V_T. This is called Light Induced V_T Shift (LIVS) and is the key parameter to be optimized in the FDPix device. Figure 2-4 shows the I_DV_G curve obtained experimentally for standard FDSOI N- and PMOS transistors (left) and FDPix device (right) with and without light illumination. The LIVS can be observed only on the FDPix device, and it is positive for both NMOS/NP and PMOS/PN configurations, as it is defined by the following equation:

$$LIVS = |V_{T\_light}| - |V_{T\_dark}| \tag{2-1}$$

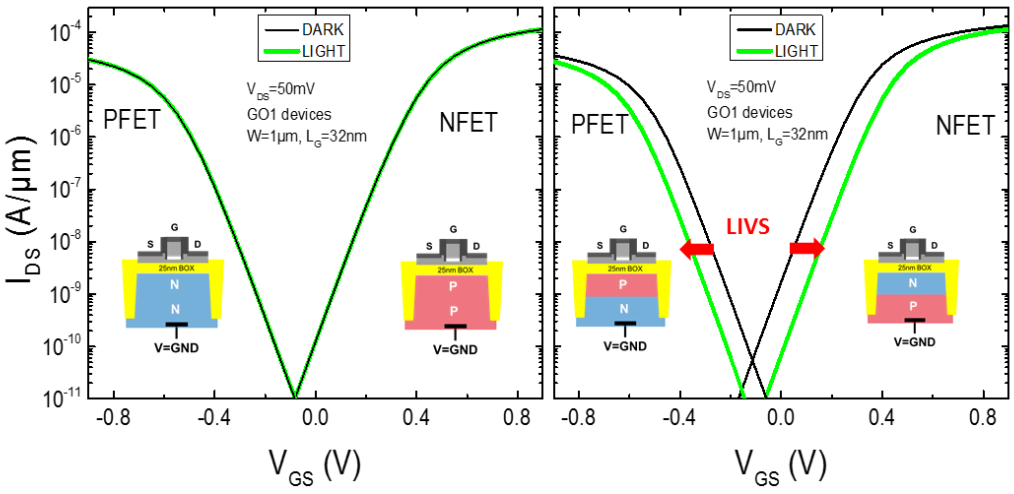


Figure 2-4: I_DV_G curves for reference FDSOI and FDPix N- and PMOS transistors in dark and under illumination

To further understand the phenomenon in more details, an analytical model is derived and calibrated with TCAD simulations and electrical characterization as presented in the next sections.

2.1.1.1. Modeling of the DC response

2.1.1.1.a. FDSOI capacitive coupling

In FDSOI, due to the ultra-thin channel thickness (7nm in our case using 28nm node), the front gate depletion layer and the back-gate depletion layer will overlap whatever the applied voltages resulting in a fully depleted channel.

The V_T of the front channel depends on the surface potential of both front (φ_{S1}) and back (φ_{S2}) channel interfaces as illustrated in Figure 2-5. To model the interface coupling, we first calculate the expression for the potential in the channel of the FDSOI by applying Poisson's equation in the structure shown in Figure 2-5, using the depletion approximation, where mobile carriers are negligible:

$$\frac{d^2\varphi}{dx^2} = \frac{qN_{ch}}{\varepsilon_{Si}} \tag{2-2}$$

Where q is the elementary charge, N_{ch} is the doping concentration of the channel, and ε_{Si} is the silicon permittivity. By integrating (2-2) twice between the front interface (x=0) and the back interface (x=T_{Si}, the channel thickness), the potential in the channel can be expressed as:

$$\varphi(x) = \frac{qN_{ch}}{2\varepsilon_{Si}}x^2 + \left(\frac{\varphi_{S2} - \varphi_{S1}}{T_{Si}} - \frac{qN_{ch}T_{Si}}{2\varepsilon_{Si}}\right)x + \varphi_{S1} \tag{2-3}$$

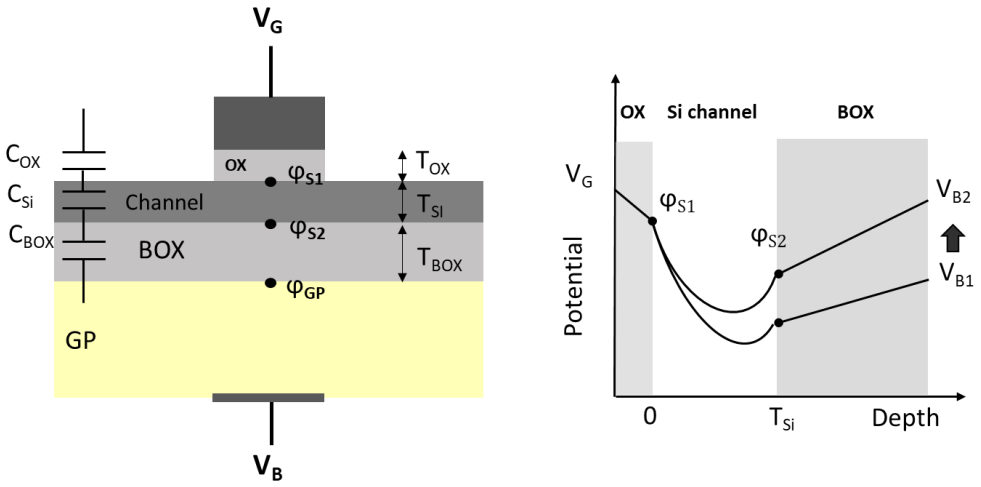


Figure 2-5: FDSOI potential across the structure assuming no depletion in the back plane (adapted from [COLINGE 2004] *)*

The threshold voltage is calculated from the front gate voltage (V_G) at threshold conditions. Gauss law is applied across the gate oxide to derive the expression for V_G as a function of the electric field, the following equations are obtained:

$$E_{S1}\varepsilon_{Si} = C_{OX}(V_G - V_{FB} - \varphi_{S1}) \tag{2-4}$$

$$V_G = \frac{E_{S1}\varepsilon_{Si}}{C_{OX}} + V_{FB} + \varphi_{S1} \tag{2-5}$$

Where C_{OX} is the gate oxide capacitance, E_{S1} is the electric field at the front interface, and V_{FB} is the flat band voltage of the front gate that depends on gate material (i.e. work function). The electric field can be calculated by deriving (2-3) as follow:

$$E(x) = \frac{d\varphi(x)}{dx}$$

$$E(x) = -\frac{qN_{ch}}{\varepsilon_{Si}}x - \left(\frac{\varphi_{S2} - \varphi_{S1}}{T_{Si}} - \frac{qN_{ch}T_{Si}}{2\varepsilon_{Si}}\right) \tag{2-6}$$

Thus, E_{S1} is obtained by substituting x=0 in (2-6):

$$E_{S1}(x = 0) = \left(\frac{\varphi_{S1} - \varphi_{S2}}{T_{Si}} + \frac{qN_{ch}T_{Si}}{2\varepsilon_{Si}}\right) \tag{2-7}$$

Similarly, the E_{S2} can be calculated from (2-6) by substituting $x=T_{Si}$, the following equation is obtained:

$$E_{S2}(x = T_{Si}) = \left(\frac{\varphi_{S1} - \varphi_{S2}}{T_{Si}} - \frac{qN_{ch}T_{Si}}{2\varepsilon_{Si}}\right) \tag{2-8}$$

$$E_{S2} = E_{S1} - \frac{qN_{ch}T_{Si}}{\varepsilon_{Si}} \tag{2-9}$$

Thus, by substituting (2-7) in (2-5) the V_G expression becomes:

$$V_G = V_{FB} + \left(1 + \frac{C_{Si}}{C_{OX}}\right)\varphi_{S1} - \frac{C_{Si}}{C_{OX}}\varphi_{S2} + \frac{\frac{1}{2}qN_{ch}T_{Si}}{C_{OX}} \quad (2\text{-}10)$$

Where C_{Si} is the channel capacitance. The two surface potentials must be evaluated. The front surface potential φ_{S1} is replaced with its threshold value φ_{S1}^{TH} as derived in *[LACORD 2012]* and can be expressed as:

$$\varphi_{S1}^{TH} = \frac{kT}{q}\ln\left(\frac{\frac{C_{OX}kT}{q}}{qn_iT_{Si}}\right) \quad (2\text{-}11)$$

Where k is the Boltzmann constant, T is the temperature in Kelvin, and n_i is the intrinsic doping concentration. This equation is derived from the inversion charge condition for FDSOI where the inversion charge at threshold is given by $Q_{inv}^{TH} = C_{OX}\frac{kT}{q}$.

The channel back-surface potential φ_{S2} is obtained by applying Gauss law in the BOX and substituting E_{S2} with (2-9) as:

$$\varphi_{S2} = V_B + \frac{\varepsilon_{Si}}{C_{BOX}}E_{S2} \quad (2\text{-}12)$$

$$\varphi_{S2} = \frac{C_{BOX}}{C_{BOX}+C_{Si}}V_B + \left(\frac{C_{Si}}{C_{BOX}}\frac{C_{BOX}}{(C_{BOX}+C_{Si})}\right)\varphi_{S1} - \frac{C_{BOX}}{C_{BOX}+C_{Si}}\left(\frac{qN_{ch}\varepsilon_{Si}}{2C_{BOX}C_{Si}}\right) \quad (2\text{-}13)$$

Where, C_{BOX} is the BOX capacitance. By substituting (2-13) in (2-10), and replacing φ_{S1} with its threshold value φ_S^{TH}, the V_T expression is obtained as:

$$V_T = V_{FB} + (1+A)\varphi_{S1}^{TH} + \frac{qN_{ch}T_{Si}}{2C_{OX}}\left(\frac{AC_{OX}}{C_{BOX}} + 1\right) - AV_B \quad (2\text{-}14)$$

Where $A = \frac{C_{Si}C_{BOX}}{C_{OX}(C_{Si}+C_{BOX})}$.

The previous calculations were carried out assuming a metallic GP, so that the surface potential at the BOX/GP interface (φ_{GP}) is equal to the back bias ($\varphi_{GP} = V_B$) as shown in Figure 2-5, and the flat band condition is assumed. However, the GP is a semiconductor doped at a concentration around $10^{18}/cm^3$, therefore, the depletion has to be taken into account since it will increase the effective thickness of the BOX, and V_B will be replaced by $V_B' = V_B - V_{FB2}$ where V_{FB2} is the flatband voltage of the back gate, as illustrated in Figure 2-6. By taking back depletion into consideration, the V_T expression can be re-written as:

$$V_T = V_{FB} + (1+A)\varphi_{S1}^{TH} + \frac{qN_{ch}T_{Si}}{2C_{OX}}\left(\frac{AC_{OX}}{C_{BOXeff}} + 1\right) - AV_B' \quad (2\text{-}15)$$

Where C_{BOXeff} represent the BOX effective capacitance when its thickness is $T_{BOXeff} = \frac{\varepsilon_{OX}}{\varepsilon_{Si}}t_{depGP} + T_{BOX}$. The depletion thickness T_{depGP} can be calculated as shown below:

$$T_{depGP} = \sqrt{\frac{2\varepsilon_{Si}}{qN_{GP}}(\varphi_{GP} - V'_B)} \tag{2-16}$$

Where N_{GP} is the GP doping concentration. φ_{GP} is evaluated by considering the continuity of the electric field across the BOX. Meaning that $E_{S2}\varepsilon_{Si} = E_{BOX}\varepsilon_{OX} = E_{GP}\varepsilon_{Si}$. Based on this equality and the previous derived equations for the surface potentials in the channel at threshold, the following expression is obtained for φ_{GP}:

$$\varphi_{GP} = V'_B + \frac{1}{4}\left[(2qN_{GP}\varepsilon_{Si})^{1/2}\left(\frac{1}{C_{Si}} + \frac{1}{T_{BOX}C_{BOX}}\right) \pm \sqrt{2\varepsilon_{Si}qN_{GP}\left(\frac{1}{C_{Si}} + \frac{1}{T_{BOX}C_{BOX}}\right)^2 - \frac{2qN_{ch}T_{Si}^2}{\varepsilon_{Si}} - 4\left(V'_B + \varphi_{S1}^{TH}\right)}\right]^2 \tag{2-17}$$

The GP depletion can be neglected in the following cases:

- If the BOX thickness is large compared with the depletion thickness ($T_{depGP} << T_{BOX}$).
- If the GP is highly doped. As we can see from (2-16), the depletion thickness depends on the doping concentration, the higher the concentration, the less the depletion.
- For N-type GP, when a negative back bias is applied, and for P-type GP, when a positive back bias is applied. In both cases, an accumulation layer will exist, therefore depletion doesn't exist.

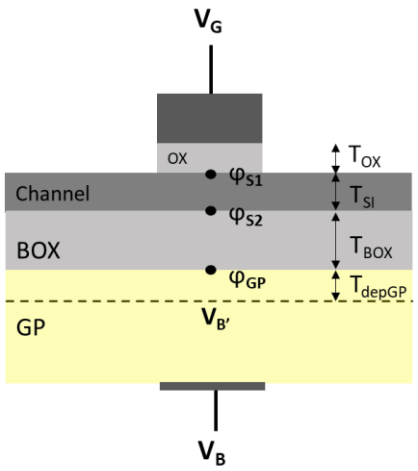


Figure 2-6: FDSOI potential across the structure considering the GP depletion

Equation (2-15) evaluates the V_T of long channel FDSOI transistor, meaning that no short channel effects are taking into account at this stage. The front channel V_T varies with the back bias only when fully depleted. If a strong back bias is applied, it can cause inversion of the channel back-surface which results in a transistor being always ON whatever the front gate V_T and potential, since the source and drain are connected via that back channel. In our study, we assume that the channel back-surface is depleted in the range of considered back bias variations.

Hence, the V_T can be modulated using the applied back bias voltage, i.e. GP potential V_B. *[NOEL 2011]* Figure 2-7 shows the variation of V_T plotted vs applied back bias (V_B) for different concentration of N- and P-Type GP.

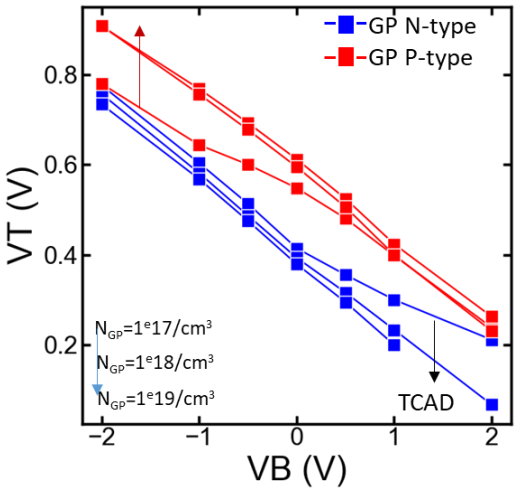


Figure 2-7: V_T vs V_B for N and P-type ground plane (GP)

The slope of these curves quantifies the coupling coefficient. It is called the Body Factor denoted as BF, and can be defined as the variation of V_T for a one Volt variation in V_B in mV/V. Since the slope is approximately constant for concentrations in the range of 1e18 /cm^3 as can be seen in Figure 2-7, we will assume that the GP depletion is negligible and derive the BF from (2-14) as:

$$BF = \frac{dV_T}{dV_B} = -A = -\frac{C_{Si} * C_{BOX}}{[(C_{Si} + C_{BOX}) * C_{OX}]} \tag{2-18}$$

$$BF \propto \frac{T_{OX}}{(T_{Si}\, T_{BOX})}$$

Although equation 2-18 is an approximation, we can see that the BF represents the ratio of the capacitances involved in the coupling that it quantifies. It can also be derived by applying a capacitive divider across the FDSOI equivalent capacitance circuit shown in Figure 2-5.

Therefore, the BF primarily depends on the thicknesses of gate oxide, BOX, and channel. It also depends on the GP concentration as can be noticed in Figure 2-7, where the slope changes from FBB to RBB. This is due to BOX/GP interface depletion (T_{depGP}) that is higher for lower GP concentration as previously mentioned, which alters the BOX capacitance. Table 2-1 summarizes the analytical BF values for different BOX and gate oxide thicknesses.

Table 2-1: Analytical Body Factor values for different BOX and gate oxide thicknesses

Body Factor (BF) values for different T_{BOX} and T_{OX} combinations (in mV/V)		**T_{OX} (nm)**	
		1.6 (GO1)	***3.7 (GO2)***
T_{BOX} (nm)	***15***	92	213
	20	72	166
	25	60	135

Now considering the FDPix device, the LIVS is related to the GP potential changing with illumination through the BF as shown in (2-19) below:

$$\Delta V_T = LIVS = V_{T_{light}} - V_{T_{dark}} = BF * \Delta V_B \quad (2\text{-}19)$$

Therefore, the conversion gain of the FDPix is represented by the BF, and thus depends on the technological parameters. As can be seen from Table 2-1, the BF, i.e. conversion gain, can be more than doubled by using for example a thicker gate oxide.

Since in the FDPix the back bias is now optical, where the V_B variations are due to photogenerated charges in the bulk, the V_T is modulated through the photodiode current and voltage. Thus, to study the effect of adding the photodiode, the basic junction equations are first derived. After that, the photogeneration is added to calculate the photocurrent, and the photodiode IV characteristics are derived. This is presented in the next sections.

2.1.1.1.b. Photodiode

In practice, the junction doping profile generated by ion implantation has a Gaussian distribution, but to facilitate the modeling, a uniform doping concentration is assumed in both sides, N_a in p side, N_d in n side.

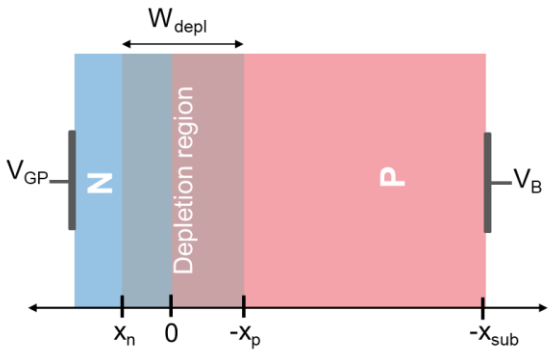


Figure 2-8: modeled NP diode with corresponding layers depth

First, the junction is described at equilibrium. The joining of semiconductor material with different doping levels, thus different quasi-Fermi level, generates a potential difference that is called the diode built-in potential denoted as ϕ_{bi}. It is derived by calculating the difference between the quasi-Fermi levels of both sides of the junction and the following expression is obtained:

$$\phi_{bi} = \frac{kT}{q} \ln\left(\frac{N_a N_d}{n_i^2}\right) \quad (2\text{-}20)$$

Therefore, the diode built-in potential depends on the doping concentration of both junction sides. Now, the Poisson equation is solved in the depletion region to calculate the field and potential, from which the depletion region width is also derived. The E-field is calculated as:

$$\frac{dE}{dx} = -\frac{\rho}{\varepsilon_{Si}} = \frac{qN_{a\backslash d}}{\varepsilon_{Si}} \tag{2-21}$$

By integrating (2-21) and applying boundary condition at the depletion region edge where the field is zero, the E-fields on both sides are obtained as follows:

$$E_N(x) = \frac{qN_d}{\varepsilon_{Si}}(x - x_N) \qquad for\ 0 \le x \le x_N \tag{2-22}$$

$$E_P(x) = \frac{qN_a}{\varepsilon_{Si}}(x_P - x) \qquad for\ 0 \ge x \ge x_P \tag{2-23}$$

Where x_n and x_p are the limit of the depletion region in N and P side of the junction respectively as indicated in Figure 2-8. The potential at both sides can be calculated by integrating the two previous equations. Considering the P side to be at zero potential, the boundary conditions are:

- V(x) = 0 at x=x_p
- V(x) = ϕ_{bi} at x=x_n

The potentials can thus be written as:

$$V_N(x) = \frac{qN_d}{2\varepsilon_{Si}}(x - x_N)^2 + \phi_{bi} \qquad for\ 0 \le x \le x_N \tag{2-24}$$

$$V_P(x) = \frac{qN_a}{2\varepsilon_{Si}}(x_P - x)^2 \qquad for\ 0 \ge x \ge x_P \tag{2-25}$$

After obtaining the expression of field and potential at steady state, the depletion width can be calculated. Since the E-field is continuous across the depletion region, equations (2-22) and (2-23) are equal at x=0. Thus, the depletion region width can be obtained as:

$$x_N - x_P = W_{dep} = \sqrt{\frac{2\varepsilon_{Si}\phi_{bi}}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)} \tag{2-26}$$

The lightly doped region is going to deplete more. When a one-sided junction is assumed, the depletion region in the highly doped side can be ignored. For example, when a PiN diode is used, where an intrinsic (low doped) layer is sandwiched between the n-type and p-type highly doped Silicon, W_{dep} is approximately equal to the intrinsic region width, in all bias conditions since it's always depleted. PiN diodes are used as photodetectors to improve the sensitivity since the photon collection volume is increased. The option of using a PiN diode in the FDPix has been investigated and is presented in Chapter 4.

When a bias is applied across the junction, the potential difference between the two sides is no longer equal to the built-in potential ($V_J = V_{GP} - V_B \neq \phi_{bi}$). To account for this change, the depletion region width expression can be rewritten as follows:

$$W_{dep} = \sqrt{\frac{2\varepsilon_{Si}}{q}\left(\frac{1}{N_a}+\frac{1}{N_d}\right)(\phi_{bi} - V_J)} \quad (2\text{-}27)$$

Therefore, when the junction is reverse biased, the depletion region width increases. As will be discussed in Chapter 3, the depletion capacitance, which is derived from the depletion region width, will also vary with applied bias and so will the transient response of the diode.

The diode I(V) characteristics are now derived starting with the ideal current equation or the Shockley equation *[HU 2010]* which is expressed as:

$$I_J = I_S(e^{\left(\frac{qV_J}{kT}\right)} - 1) \quad (2\text{-}28)$$

Where I_S is the reverse saturation (leakage) current of the junction, mainly due to diffusion of minority carriers through the junction depletion region. This current is also referred to as *dark current* and is a main source of noise in image sensors applications as mentioned in Chapter 1. The reverse saturation current can be calculated by solving the current continuity equation in both quasi-neutral regions, and can be expressed as:

$$I_S = Aqn_i^2\left(\frac{D_n}{N_A L_n}+\frac{D_p}{N_D L_p}\right) \quad (2\text{-}29)$$

Where A is the area of the diode, D_n and D_p are the diffusion coefficient of holes in N region and electrons in P regions respectively, L_n and L_p are the diffusion length of holes in N region and electrons in P region respectively, and is equal to $L = \sqrt{D_{n/p}\tau_{n/p}}$, where $\tau_{n/p}$ is the carrier life time.

The recombination/generation in the depletion region will dominate at low forward bias. It is called the Shockley-Read-Hall (SRH) current and will add a drift component to the diode ideal current equation. The SRH current is calculated by integrating the recombination/generation rate across the junction. Assuming mid-gap recombination centers, the SRH current is expressed in forward bias as follow:

$$I_{G\backslash R} = A\frac{qn_i W_{dep}}{\tau_{dep}}\left(e^{\frac{qV}{2kT}} - 1\right) \quad (2\text{-}30)$$

In forward bias, the SRH current is due to recombination. While in reverse bias, it increases the leakage current due to generation. It can be expressed in reverse as:

$$I_s + I_{G\backslash R_{reverse}} = I_s + A\frac{qn_i W_{dep}}{\tau_{dep}} \quad (2\text{-}31)$$

τ_{dep} is the carrier's life time in the depletion region and thus depends on defect density. A high τ_{dep} is desired to reduce the leakage current as can be seen from equation (2-31). Therefore, the process must be precisely controlled to reduce the generation of defects. The SRH current is usually modeled by adding an ideality factor (n) to the ideal current equation, which is multiplied to the thermal voltage. Its value varies between 1 and 2. When n=1, only diffusion is considered (ideal diode), and when n=2, only the recombination is taken into account.

In fact, additional currents, the Trap-Assisted-Tunneling (TAT) current, the Band-to-Band-tunneling (BTBT) current and the avalanche break down current also participate to the non-ideality of the diode IV curve. Since the avalanche break down happens only at high reverse bias, they will be neglected in our study. The total diode current can thus be expressed as:

$$I_{J\_tot} = I_J + I_{SRH} + I_{BTBT} \tag{2-32}$$

Now that the I(V) characteristics of a standard p-n junction has been derived, the current due to photogeneration of carriers under light illumination, i.e. photocurrent, is derived.

The photogenerated electron-hole pairs will contribute to the photocurrent when absorbed in the depletion region separated by its E-field, or if they can diffuse to the depletion region and reach that same E-field when generated in the quasi-neutral region. Thus, it has two main components as presented below:

- A drift component due to absorption in depletion region, which can be calculated by integrating the photogeneration rate in the depletion region given by:

$$G(x) = \alpha(\lambda)\phi_0 e^{-\alpha(\lambda)x} \tag{2-33}$$

  Where $\alpha(\lambda)$ is the absorption coefficient as a function of wavelength, Φ_0 is the photon flux in $m^{-2}sec^{-1}$. Φ_0 can be expressed using the optical power density (P_{opt}) in W/cm^2, through the equality $\Phi_0 = P_{opt} * \lambda/hc$. Where h is the Plank constant and c is the speed of light. The drift component of the photocurrent is expressed as:

$$I_{PH_{drift}} = \int_0^{Wdep} G(x)dx = q\phi_0\left(e^{(-\alpha W_{dep})} - 1\right) \tag{2-34}$$

  We will consider the calculation at a constant wavelength.

- The diffusion currents, which results from the electron-hole pairs photogenerated in the quasi-neutral region. They are calculated on both sides of the junction by solving the current continuity equation *[SZE 2007]*. We obtain:

$$J_p^{PH} = \frac{q\Phi_0\alpha L_p}{\alpha^2 L_p^2 - 1}\left[\frac{\left(\frac{S_p L_p}{D_p} + \alpha L_p\right) - e^{-\alpha x_n}\left(\frac{S_p L_p}{D_p}\cosh\frac{x_n}{L_p} + \sinh\frac{x_n}{L_p}\right)}{\left(\frac{S_p L_p}{D_p}\sinh\frac{x_n}{L_p} + \cosh\frac{x_n}{L_p}\right)} - \alpha L_p e^{-\alpha x_n}\right] \tag{2-35}$$

$$J_n^{PH} = \frac{q\Phi_0\alpha L_n}{\alpha^2 L_n^2 - 1}e^{-\alpha x_p}\left[\alpha L_n - \frac{\frac{S_n L_n}{D_n}\left(\cosh\frac{x_{sub}}{L_n} - e^{-\alpha x_{sub}}\right) - \frac{S_n L_n}{D_n}\cosh\frac{x_n}{n} + \sinh\frac{x_{sub}}{L_n} + \alpha L_n e^{-\alpha x_{sub}}}{\left(\frac{S_n L_n}{D_n}\sinh\frac{x_{sub}}{L_n} + \cosh\frac{x_{sub}}{L_n}\right)}\right] \tag{2-36}$$

Where J_p and J_n are the diffusion currents densities of holes in n region and electrons in p region respectively, and $S_{n/p}$ are the recombination velocities. To simplify these equations, we are making some assumptions:

a) The junction is assumed narrow on the N-side, such that $x_n << L_p$, and the recombination is null (Sp=0).

b) The p-type substrate is much thicker than the diffusion length of electrons such that $x_p >> L_n$.

These assumptions allow us to obtain the following simplified equations:

$$J_p^{PH} = \frac{q\Phi_0\alpha^2 L_p^2}{\alpha^2 L_p^2 - 1}[1 - e^{-\alpha x_n}] \tag{2-37}$$

$$J_n^{PH} = \frac{q\Phi_0\alpha^2 L_n^2}{\alpha^2 L_n^2 - 1} e^{-\alpha x_p} \tag{2-38}$$

Therefore, the total photocurrent can be written as:

$$I_{PH} = A\left(J_n^{PH} + J_{ZCE}^{PH} + J_p^{PH}\right) \tag{2-39}$$

The total photodiode current is given by:

$$I_{TOT} = I_{J\_tot} - I_{PH} = (I_J + I_{SRH} + I_{BTBT}) - (I_n^{PH} + I_{ZCE}^{PH} + I_p^{PH}) \tag{2-40}$$

Now that all the current associated with the photodiode responses and bias conditions were derived, the photodiode voltage can be calculated. At steady state, the net current flowing I_D is zero, therefore, under illumination the photodiode is in solar cell mode with open circuit characteristics as shown in Figure 2-9. The potential across the diode corresponds to the difference between the built-in potential and the open circuit voltage (V_{OC}). V_{OC} can be calculated by setting the total diode current to zero (I_{J_tot}=0) and solve for V_J in equations (2-28) and (2-40), the following expression is obtained:

$$Voc = \frac{kT}{q}\ln\left(\frac{I_{PH}}{I_s} + 1\right) \tag{2-41}$$

The V_{OC} is a forward bias voltage that results from the photocurrent bias. Since it depends, as seen in (2-41), on the saturation reverse current, which depends on the quality of the junction and the density of defect, a high quality silicon junction will achieve higher V_{OC} for the same intensity. In crystalline silicon solar cell for example, a V_{OC} of 750mV can be achieved at AM1.5[5].

[5] AM1.5 is the air mass coefficient which defines the optical length at zenith (normal to the earth surface) through the atmosphere. 1.5 is used as a standard in solar cell. The spectrum is shown in Appendix B.

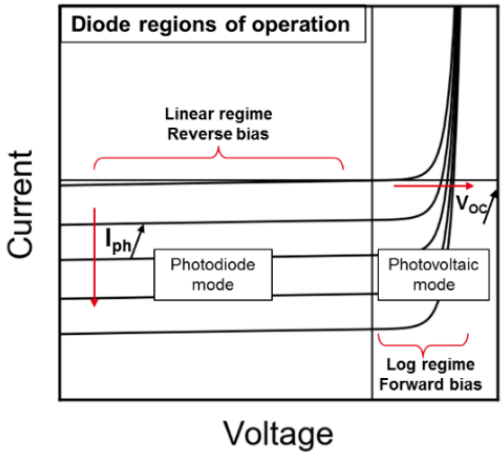


Figure 2-9: classical I(V) curve for a photodiode showing the different regions of operation and the increase in reverse current due to photocurrent

Finally, the two components previously demonstrated are coupled to model the steady state response of the FDPix sensor. This is done by considering the voltage variation across the photodiode as a back bias in FDSOI as illustrated in Figure 2-10.

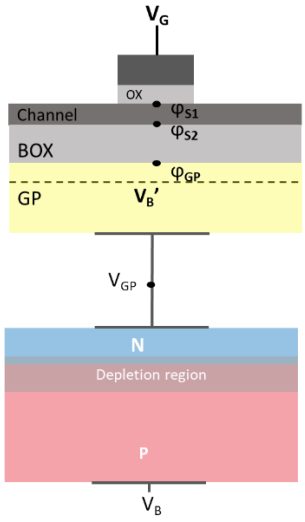


Figure 2-10: FDPix modeled by taking the photodiode as the source of the Back bias in an FDSOI transistor

If V_B is at GND, and the structure is in dark, the transistor characteristics are equivalent to a standard FDSOI transistor with no diode, for the same GP doping concentration. When a constant light flux is incident on the FDPix, with V_B clamped at ground, the open circuit voltage is impacting the n-type GP potential since it's floating. Thus, the voltage across the photodiode V_J is equal to:

$$V_N - V_P = (\phi_{bi} - V_{OC}) - 0 \tag{2-42}$$

To support our model, TCAD simulations were performed as shown in Figure 2-11. We can see that the potential in the N-type GP changes when light illumination is applied. This is equivalent to applying a negative back bias which results in a higher V_T according to equation (2-15).

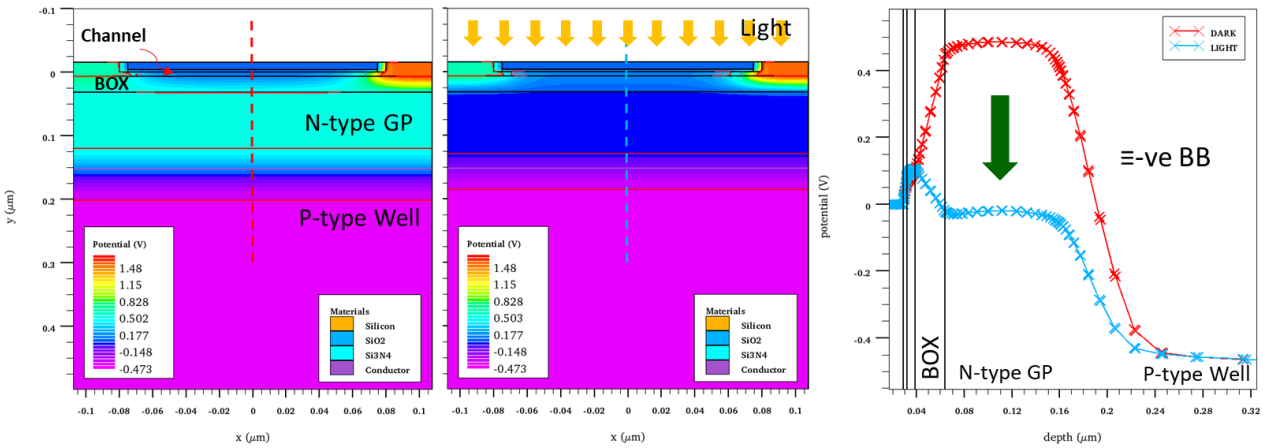


Figure 2-11: a) FDPix structure potential in dark and under light illumination b) cutline 2D potential showing the decrease in GP potential as equivalent to a negative back bias

Model validation:

In this part, N-type MOSFET is considered for FDPix device. Although both transistors N and P-types were tested and calibrated.

LETI has developed a model to describe the UTBB FDSOI called LETI-UTSOI2 *[Poiroux 2013][Poiroux 2015]*. It is a surface potential-based model where the low-doped channel transistor is modeled, including the back-surface inversion under strong forward back bias condition. LETI-UTSOI2 has been successfully used for various applications *[Ghouli 2016]*. Therefore, the model card is used to describe the FDSOI transistor to simulate the FDPix device. The model is described in more details in appendix A. Also, the JUNCAP2 junction model *[Scholten 2006][Scholten 2010]* is implemented to describe the PN junction currents and capacitances. This model describes the junction in all regimes without using any non-physical fitting parameter. It contains the ideal current, the Shockley-Read-Hall (SHR) generation/recombination current, the BTBT current, the TAT current and avalanche breakdown. The developed photocurrent model was added to the aforementioned models to fully describe the FDPix sensor. Finally, these models are implemented and imported in device libraries used in SPICE simulations.

First, the FDSOI transistor was calibrated with experimental results as shown in Figure 2-12. The device is a long channel (L=2µm, W=2µm) GO2 NMOS transistor with PN oriented diode (P-type GP, RVT) integrated under the BOX. The transistor I_DV_G and V_TV_B, which both represent very important figure of merits to accurately describe our sensor, are well reproduced by the model. The measured BF is around 122mV/V, not so far from the analytical value of 135mV/V for these technological parameters, the difference might be due to the BOX/GP interface depletion that takes place for negative back bias in case of P-type GP, and where the BF is measured. For the positive values of V_B however, a small divergence is observed. This is attributed to transient phenomena in case of the characterization that

were not taken into account in the simulation at this stage, since the device is studied at equilibrium. More details and explanations will be presented on transient phenomena in the next chapter.

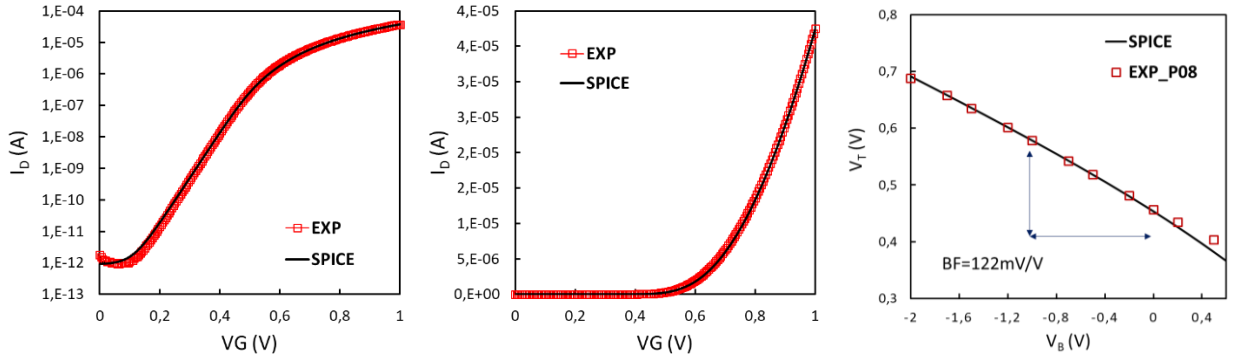


Figure 2-12: model calibration with TCAD simulation. $I_D V_G$ linear and log and the $V_T(V_B)$

The model is calibrated with TCAD simulation results for different junction profiles. In TCAD, the doping is modeled by using the implantation profile obtained using CTRIM simulation tool *[POSSELT 1994]*, which allows the extraction of the Gaussian profiles depending on energy, dose, tilt, rotation and species, through a defined stack of multilayer materials. The simulated meshed structure is shown in Figure 2-13 with the corresponding doping profile.

The I(V) of the diode obtained with SPICE simulations versus TCAD is shown in Figure 2-14. The accurate description of the diode characteristics is of outmost importance since it is what differentiate an FDPix from a standard FDSOI. The addition of the diode will have a more important impact when tested in transient domain, since it adds a parasitic capacitance, as will be discussed in the next chapter.

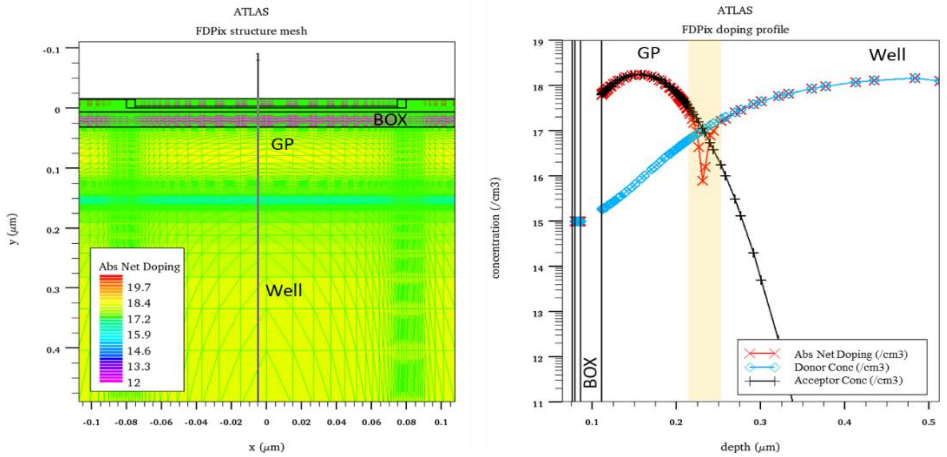


Figure 2-13: FDPix structure mesh in TCAD with a cut that shows the doping profile of the diode obtained with CTRIM simulations

The photodiode response is calibrated by adjusting the diode parameters that include: Area, I_S, I_{JMAX} and other parameters proper to the JUNCAP2 model such as *MJ* that defines the junction transition, and must be used to calibrate the abrupt step junction of the model with the Gaussian profile junction of the TCAD. The area is probably the trickiest part because the coupling occurs only under the channel, so the total area of the diode is considered equal to *(W*L)+fringing field*. The fringing field will slightly increase the coupling area. For long channel devices, this can be

neglected, but for short channel devices, it has to be taken into consideration, since it changes the capacitance of the junction and thus its transient behavior.

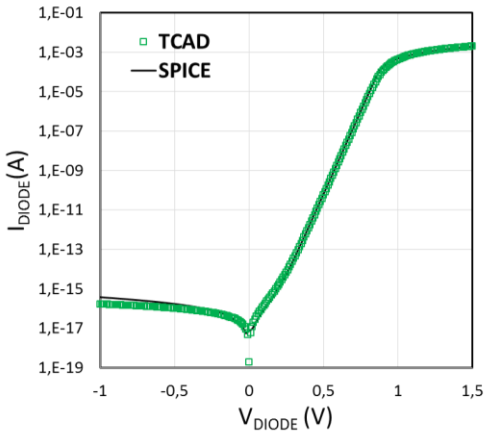


Figure 2-14: p-n junction I(V) calibration model vs TCAD

2.1.1.2. FDPix response to light: LIVS vs optical power

The modeled LIVS versus P_{opt} curve obtained in steady state i.e. DC conditions, is compared with electrical characterization results. The tests are performed by applying a constant light illumination using a Xenon wide band source on the device in Front Side illumination (FSI) configuration (Appendix B), and the measurement are performed after a wait time to ensure that the device reaches equilibrium. Since the I_{ph} is linear with P_{opt} as shown in equations (2-34), (2-37) and (2-38) through Φ_0, V_{OC} has a logarithmic dependence with light intensity. Therefore, the LIVS response to P_{opt} when the device is in steady state ($LIVS_{SS}$) is logarithmic as shown in Figure 2-15 and demonstrated in (2-43) below:

$$LIVS_{SS} = BF * \Delta V_{GP} = BF * \frac{kT}{q} * ln\left(\frac{I_{PH}}{I_S} + 1\right) \quad (2\text{-}43)$$

The explored optical power is limited by the instrumentation used in opto-electrical characterization. The device tested is an N-type GO2, W=L=2µm, using FSI. In the considered range, the model fitted well the characterization results as can be seen in Figure 2-15. However, some parameter had to be adjusted. This included the capacitance of the junction, since the model was calibrated to TCAD simulation and not to the device junction, the capacitance was underestimated. Also, the optical power intensity. No notion of fill factor (FF) was added to the model, which resulted in the curve being generated at lower intensities assuming that the whole area was illuminated, therefore overestimating the photocurrent and thus the V_{OC} for lower intensities. In future optimization of the model, the FF should be known and multiplied by the area.

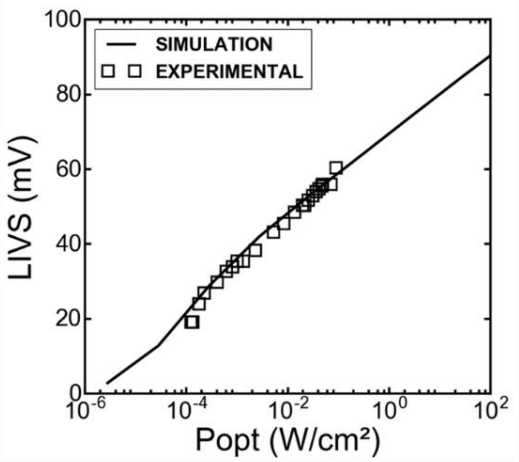


Figure 2-15: LIVS vs POPT for an NMOS/PN model and electrical results

In the previous results, the sensor response doesn't reach saturation. Using TCAD simulations, the sensor's logarithmic response vs optical power density results in a wide Dynamic Range (DR) of about 120-130dB. The upper limit of the DR depends on the saturation of the sensor, which can be modeled by considering the maximum potential variation of the junction denoted as ΔV_{GP_max} and the BF of the transistor. In DC, the ΔV_{GP_max} corresponds to the maximum V_{OC}. The maximum theoretical V_{OC} should correspond to the built-in potential of the diode, above which the diode is strongly forward biased, and no charge can accumulate, therefore the sensor saturates. In reality, it will saturate before reaching the ϕ_{bi} since the barrier will be low enough for the charges to diffuse. Again, this will depend also on the defect density. For the sake of simplicity, ϕ_{bi} is considered as the maximum potential. This is illustrated in Figure 2-16, where the band diagram of the structure is shown.

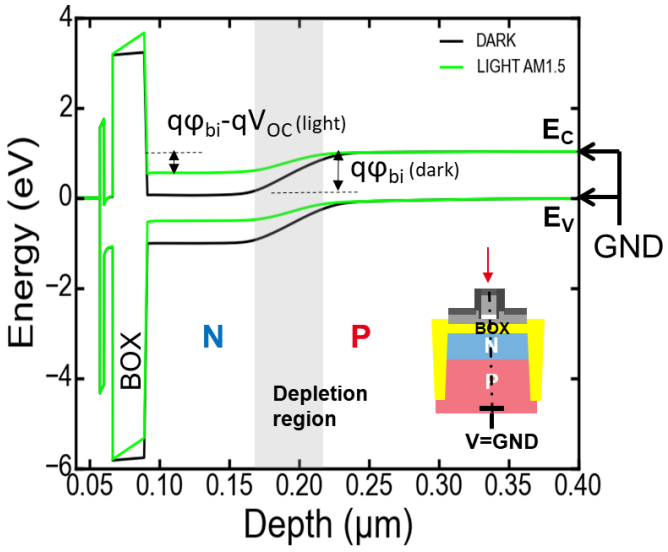


Figure 2-16: band diagram of FDPix device for different diode orientation obtained from TCAD simulations

The saturation LIVS in steady state (LIVSss_sat) can be calculated as shown below:

$$LIVS_{ss\_sat} = BF * \Delta V_{GP\_max} = BF * \phi_{bi} \quad (2\text{-}44)$$

Therefore, for a GO2 device in 28nm technology, where the BF~135mV/V and a photodiode with ϕ_{bi}=0.95V, the maximum LIVS in DC is equal to 135mV/V*0.95V ≅130mV.

Hence, the saturation of the sensor will depend on:

- Junction quality or defect density that defines the carriers life time on which depend the leakage current.
- Doping concentration which determines the built-in potential and thus the potential barrier and the leakage.
- The LIVSsat will depend on the BF which determines the slope of the LIVS vs Popt shown in Figure 2-15, however, the DR does not depend on the BF since the saturation illumination power doesn't depend on it.
- The junction barrier in transient. Here we consider the electrical back gate (the Well) to be at GND, therefore the barrier is equal to the built-in potential, but if an AC bias is applied, this barrier can be either lowered or increased depending on the voltage applied.

All the previous mentioned points will be studied in more details and optimized in Chapter 4.

2.1.1.3. Impact of light on transistor characteristics

2.1.1.3.a. MOSFET I_DV_G and I_DV_D

The standard figure of merits of a MOSFET can be extracted from its I_DV_G curve, where the drain current (I_D) is plotted vs the voltage applied on the gate (V_G). To extract the V_T, different methods are available *[ORTIZ-CONDE 2013]*. In this work, the V_T is extracted using the constant current method *[LEE 1982]* which consist on measuring V_G at a current (I_T) given by:

$$I_T = I_0 \frac{W}{L} \quad (2\text{-}45)$$

Where W and L are the transistor width and length respectively. The I_0 term is user-defined and usually taken to be equal to 100nA. This method is widely used in industry due to its simplicity. Since for the FDPix we measure a ΔV_T, thus it can be obtained at any I_0 as long as it is in subthreshold regime.

Shifting the V_T results in modulating I_D at a constant V_G. As can be seen in Figure 2-17, the $I_D(V_D)$ curves for an N-type FDPix GO1 with L=30nm and W=1µm, shift to lower current in the case of NP oriented junction, which results from an increase in V_T, and shifts upward to higher current for the PN oriented junction due to a decrease of V_T. As depicted in Figure 2-18.a. the current is modulated up to 350% with light when biased in subthreshold regime.

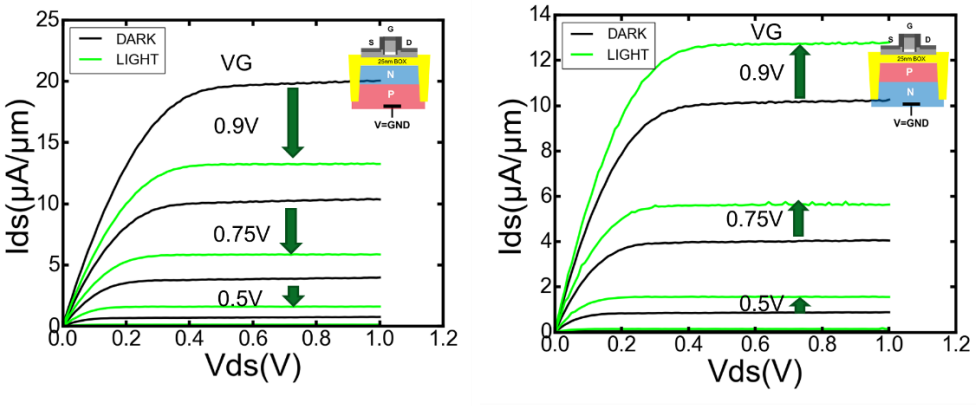


Figure 2-17: I_DV_D curves at different V_G polarization and for a) NP, b) PN oriented photodiodes

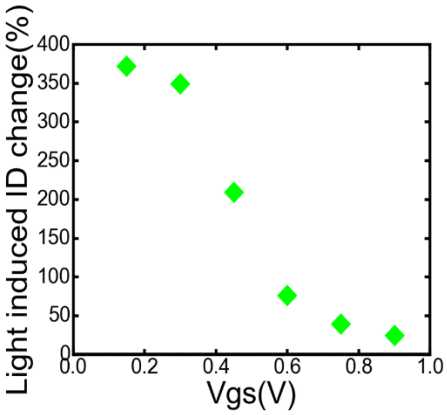


Figure 2-18: modulation of the drain current with light for different V_{GS} at V_{DS}=0.9V (saturation)

When monitoring the current varying with light, the equivalent V_T variation is calculated based on two criteria:

a) The device must be biased in subthreshold ($V_G \leq V_T$)

b) The subthreshold swing does not depend on light illumination.

If these two conditions are respected, the V_T shift i.e. LIVS, can be calculated from the current variation. Since the first criteria is easily obtain by setting the appropriate V_G, we will discuss next the subthreshold swing of the transistor to check its dependence on the different parameters.

2.1.1.3.b. Subthreshold swing (SS)

Since the MOSFET is not an ideal switch, it has a finite on/off transition represented by the sub-threshold swing (i.e. inverse subthreshold slope). It is a key property for digital applications where the MOSFET is used as a switch. This transition must be as sharp as possible to insure high-speed switching and low power consumption. It can be expressed as the inverse of the slope of the I_DV_G curve (I_D is plotted in log) in subthreshold region as:

$$SS = \frac{dV_G}{dlog(I_D)} \tag{2-46}$$

A more explicit expression is derived in *[COLINGE 2004]* based on the diffusion current mechanism in subthreshold as:

$$SS = \frac{kT}{q} * \frac{\ln(10)\, dV_G}{d\Phi_{S1}} = \frac{kT}{q} * \ln(10)\left(1 + \left(\frac{1}{C_{OX}}\right) * \left(\frac{C_{Si}C_{BOX}}{C_{Si} + C_{BOX}}\right)\right) \quad (2\text{-}47)$$

This expression can also be derived by applying a capacitive divider across the equivalent capacitive circuit shown in Figure 2-5 similarly to the BF calculation as previously discussed. Assuming $C_{BOX} << C_{Si}$ and $C_{BOX} << C_{OX,}$ which is usually the case as long as the BOX is much thicker than the gate oxide and channel, the SS can be expressed as follow:

$$SS = \frac{kT}{q} * \ln(10) \quad (2\text{-}48)$$

This expression gives the theoretical maximum achievable SS at room temperature of 60mV/decade. For the present FDSOI technologies, the SS is close to 65mV/dec due to the use of thin buried oxide.

2.1.1.3.c. LIVS calculation from I_D ratio and SS

The current in subthreshold can be expressed as:

$$I_{Dsubth} = I_T * e^{\left(\frac{V_G - V_T}{SS/\ln(10)}\right)} \quad (2\text{-}49)$$

Where I_T is defined by equation (2-45). Therefore, a linear variation in V_T results in an exponential variation in current. By taking the ratio of the current variation (I_{D1}/I_{D2}), assuming constant V_G and SS, the ΔV_T can be calculated as:

$$\Delta V_T = V_{T2} - V_{T1} = SS * \log\left(\frac{I_{D1}}{I_{D2}}\right) \quad (2\text{-}50)$$

From the previous discussion, we can see how a constant SS that does not change with light illumination would simplify the calculation, which is the case as can be verified in Figure 2-19 for 23 tested GO2 N-type FDPix devices with L=2µm, at room temperature. If it did change with illumination, its variation must be taken into account adding a complexity to output processing.

The previous equation can be re-written for the FDPix as follows:

$$LIVS = V_{Tlight} - V_{Tdark} = SS * \log\left(\frac{I_{Ddark}}{I_{Dlight}}\right) \quad (2\text{-}51)$$

The I_{Ddark} is the reference current. In DC, when the sensor is initially at equilibrium, it is equal to I_T. However, as will be further explained in Chapter 3, this reference current is affected by transient phenomenon.

Figure 2-19 also show the V_T dispersion in dark and under illumination for the 23 tested GO2 L=2µm N-type FDPix devices with NP oriented photodiode. The measured mean LIVS (μ_{LIVS}) is 44mV, with a variance (σ_{LIVS}) of around 4.8 mV. It is lower than the V_Ts variance of 10mV, since the LIVS that represent a delta, will not be impacted by the same process variability. However, this variance is due to global variability on a 300mm wafer, and therefore should

not be considered for FPN estimation. To estimate the FPN, the local variability of the technology should be considered.

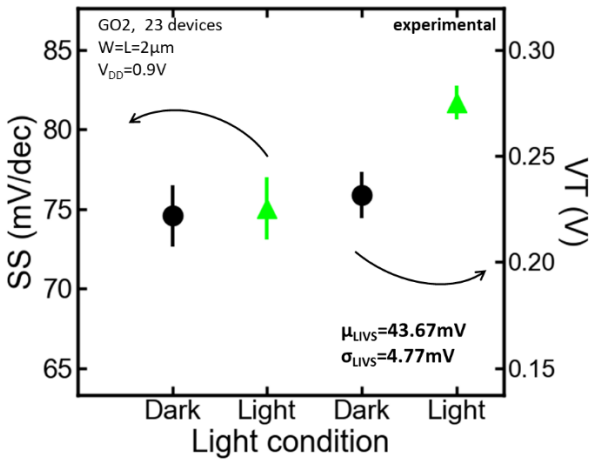


Figure 2-19: Subthreshold swing and threshold voltages for dark and under illumination conditions, for 23 devices tested

As a conclusion, the FDPix DC response is well described and modeled, since it matches the experimental results. In Chapter 3, the transient behavior is studied and modeled by considering all the capacitances involved in the sensor operation.

As was discussed previously, the sensor technological parameters and defect density have a direct impact on its response and performance. Therefore, the next section presents the detailed process flow of the FDPix sensor, highlighting the main challenges to obtain a high-quality sensor.

2.1.3. Process flow

Regarding integration, standard FDSOI process integration is used, therefore, the FDPix comes with no extra cost, since no additional masks are required. The structure is 3D-like with the transistor being on top of the photosensitive element, which allows the addition of complex electronic functions on top of the photodiode. In addition, Back Side Illumination (BSI) should be used to maximize the FF.

The UTBB architecture of the FDSOI transistor was atained mainly due to the availability of very high quality SOI wafers. The ultra thin channel and BOX are obtained thanks to a process called SmartCut™ developed by LETI and comercialized by SOITEC *[BRUEL 1995]*. It is depicted in Figure 2-20 and explained next.

2.1.3.1. SOI SmartCut process

The process start with the oxidation of a silicon wafer (~750µm thick for 300mm wafers) denoted in Figure 2-20 as wafer "A". After that, hydrogen ions are implanted through the oxide layer to create a "weaken" layer. The implantation energy is what determines the hydrogen layer implantation depth and thus, the Si film thickness (7nm for 28nm technology). The wafer is then bonded to a handle silicon wafer that represents the substrate of the SOI. The handle wafer is also oxidized. Both wafers undergoe cleaning processes to prepare the bonding surfaces. After the oxide-oxide bonding, the ultra thin crystalline channel is obtained using a low temperature thermal anneal to break

the hydrogen bonds. A high temperature thermal annealing and Chemical Mechanical polishing (CMP) are then performed (with Angstrom precision) to obtain the final high quality SOI. The splitted wafer (wafer A) is recycled. By controling the oxidation step of both wafers, various BOX thicknesses can be obtained. In our case, 25nm BOX is used. As previously mentioned in section 2.1.1.1, the thicknesses of the body and BOX are key parameters that determines the performance of the FDPix device, since they determine the BF.

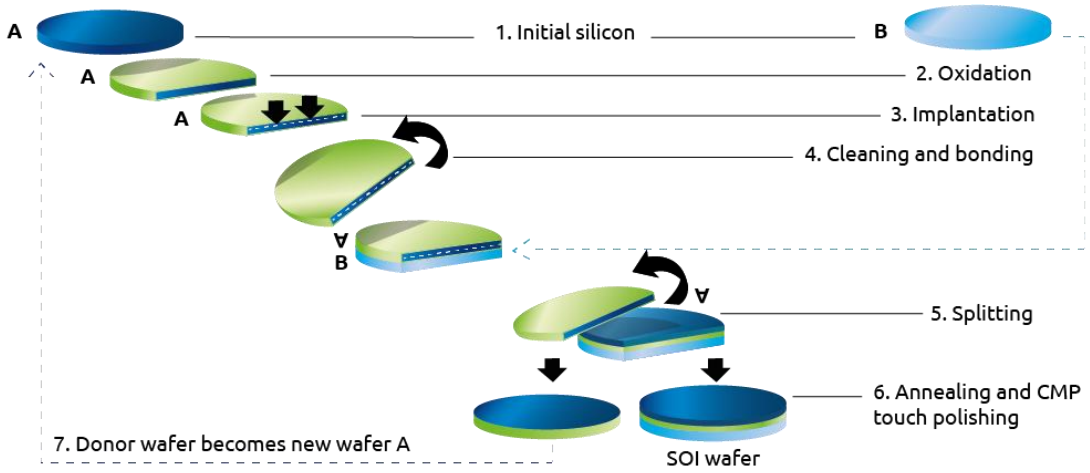


Figure 2-20: SOITEC SmartCut™ process to obtain high quality SOI wafers with ultra-thin Si film [SOITEC]

2.1.3.2. FDPix process flow

1. SOI wafer and STI patterning

Starting with an SOI wafer processed as explained in the previous section, the first step is the active region and STI patterning. First, a nitride layer is deposited, and the trench are patterned. Following that, the trench are filled with SiO_2, and finally a CMP is performed. The obtained STI are 280nm deep.

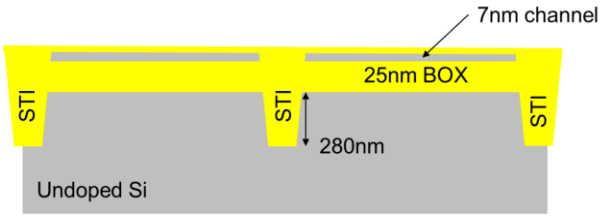


Figure 2-21: process starting point: the SOI wafer

2. GP and Well implantation (photodiode definition)

This step is the one that we modify to obtain the FDPix device characteristics. It is what differentiate an FDPix process from the standard FDSOI. In standard FDSOI technology, three implantations of the same type are performed, one for GP and two for the Well to insure good electrical conduction when using back bias. As shown in the schematic, we choose the GP and Well doping of opposite type to obtain the photodiode. Various junctions are obtained using

different implantation energy and doses. A typical doping profile is showed in Figure 2-23, where the zero on the x-axis represent the BOX/GP interface. This profile was obtained using CTRIM simulation. We can see that the junction is at 160nm below the BOX, which does not exceed the 280nm STI depth, thus keeping a good pixel isolation.

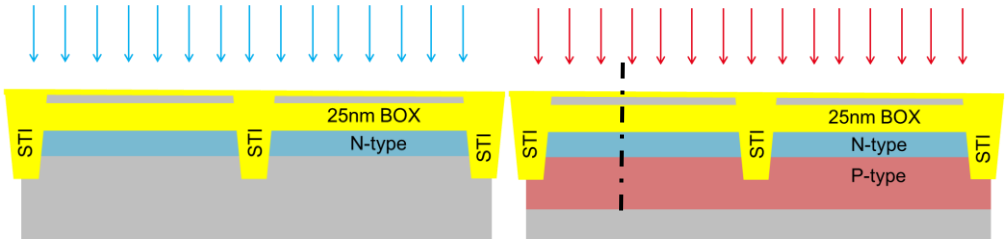


Figure 2-22: GP and Well implantation through the BOX

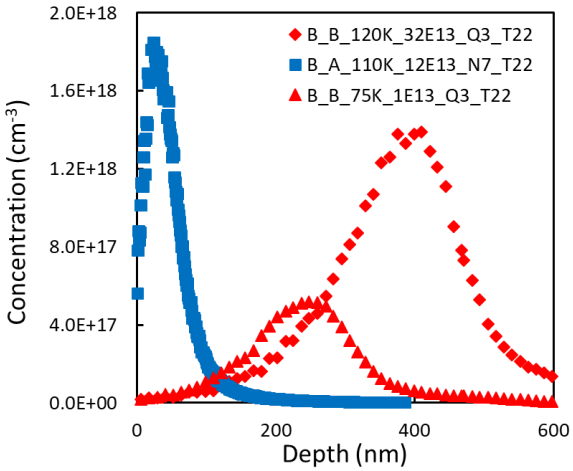


Figure 2-23: CTRIM based photodiode doping profile obtained after implantation

Since the GP and Well are implanted prior to the gate stack deposition, following the implantation, a thermal anneal called spike anneal (1050C° for 5 sec) is performed to reduce the defects generated during the previous step, without deteriorating the transistor. We believe that it is thanks to this annealing step that we obtained high quality photodiode.

3. Gate stack deposition

Next is the gate stack. Depending on the layers materials, different deposition techniques are used. In addition, depending on the gate oxide thickness, the process is slightly different but we will not go into details here and just take the process of a thin oxide (GO1, EOT=1.6nm), keeping in mind that thick oxide devices (GO2, EOT=3.7nm) are also available. The stack is composed of InterLayer (IL), high-K dielectric (HfO_2), the metal gate TiN and a doped poly Si layer. Using high-k material came as a solution to reduce the oxide thickness while maintaining a good capacitance and minimizing gate leakage current *[COLINGE 2002]*. The metal gate was introduced to avoid poly-Si gate depletion when the channel is inverted which degraded the Equivalent Oxide Thickness (EOT), and to avoid the HfO_2 reacting to poly-Si which caused Fermi level pinning and increased the V_T *[HOBBS 2004][LU 2018]*. The metal choice is made depending on the work function, which determines the V_T. The TiN with a mid-gap work function can

be used on both N and PMOS transistor. After that, the Hard Mask (HM) is deposited and the gate patterning (Lithography and etching) is performed.

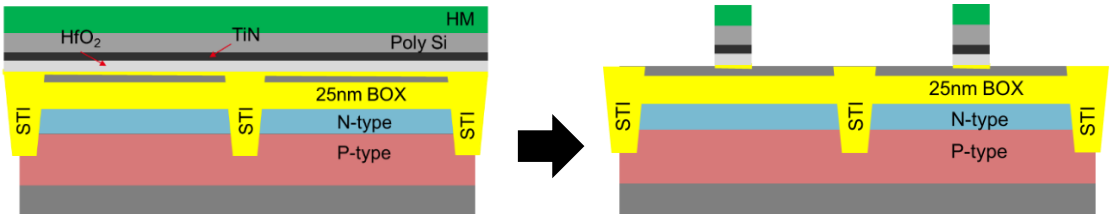


Figure 2-24: Gate patterning

4. Spacer deposition and S/D epitaxy

Following the gate patterning, the spacers are deposited and using epitaxial growth, the raised source and drain are implemented. Using raised S/D, which was introduced by intel in the 90 nm node *[MISTRY 2004]*, allows the reduction of the access resistance, and it also had a beneficial advantage of avoiding the silicidation to reach the channel and the BOX *[LU 2018]*.After that, the S/D implantations are performed, and a thermal annealing is used to activate the dopant and to define the junction, which insures a good access resistance.

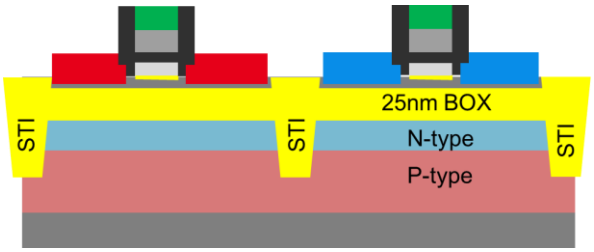


Figure 2-25: spacer deposition, S/D epitaxy and dopant implantation and activation through a spike anneal

5. Salicide, contacts, and BEOL

In this step, the S/D and the gate are silicided, which consists in creating a silicon-metal compound (e.g. NiPtSi) to minimize the access resistance. After that the contacts are etched and filled with a metal (typically Tungsten W) and connected to metal one (M1). Finally, the Back End Of Line (BEOL) process is performed, and ends with the connection of the last metal line with the aluminum pads used in electrical characterization to polarize the device. The number of metal layers will differ depending on the structures implemented on the wafer.

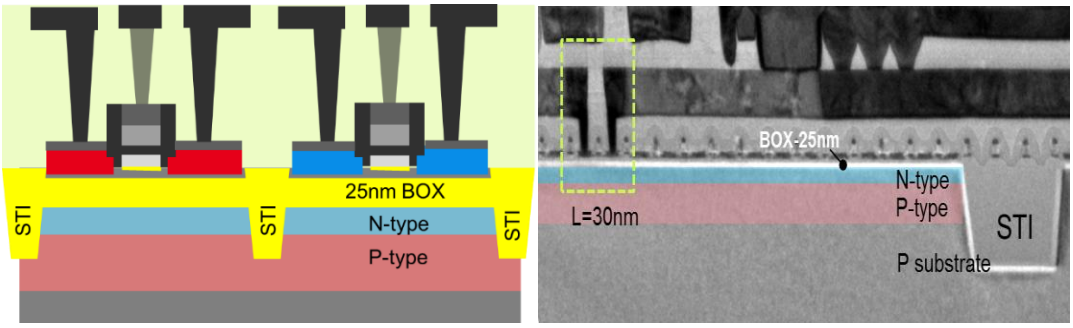


Figure 2-26: finished process with silicidation, contact and BEOL schematic and TEM image

The first fabrication run was as close as possible to the standard process. It established a baseline for performances of the light-sensitive FDSOI transistor, before further optimization. Therefore, no specification regarding metal lines were taken into account on the first batch. Since we are using Front Side Illumination (FSI), the light has to go through all the metal layers, which reduces the FF due to absorption and reflection. This was corrected on a future batch where the layout is optimized for FDPix by avoiding shadowing due to metal lines.

Conclusion:

The complete simplified flow is shown in Figure 2-27. Here a simplified version was depicted with only the main steps. The key points to remember are:

- The FDPix uses the same standard FDSOI process flow, only the type of dopants in the implantation step of GP and Well are modified.
- No extra cost is associated with the process.
- The thermal annealing after the implantation helps obtaining a high quality, i.e. low leakage, photodiode.
- Different photodiode orientation can be implemented for both N and PMOS transistor, and they can be different for each as shown in Figure 2-27.
- Metal lines should be optimized when FSI is used.
- Optimized process integration scheme are discussed in Chapter 4 for device performance optimization

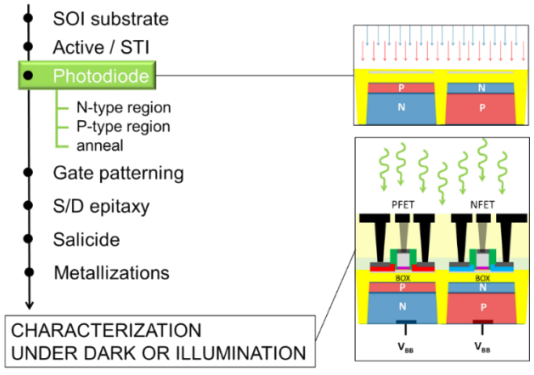


Figure 2-27: process flow of FDPix device where the only altered step, the implentation is highlighted

2.2. Complementary FDPix sensors

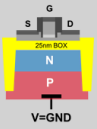
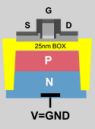
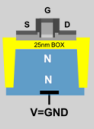
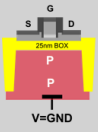
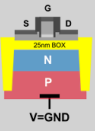
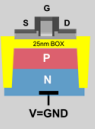
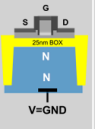
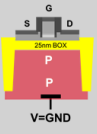
2.2.1. NMOS and PMOS pixels

One of the main advantages of the FDPix device is its complementarity. Both type of transistors, N- and P-type, results in an opposite LIVS when the same diode orientation is implemented (positive for NMOS, negative for PMOS). Since the channel type are different, the same potential will have an opposite effect on N and PMOS that is also observed when using BB. This will allow the design of CMOS analog and digital circuit specific to our structure, as will be discussed in chapter 5.

2.2.2. Photodiode orientation

The transistor type is not the only complementary element here. The diode orientation regarding the BOX also results in different responses. Analogous to a positive or negative back bias, the diode orientation will determine the type of charge accumulating at the BOX-GP interface that causes the LIVS. For example, an NMOS with an NP oriented junction results in a +ve LIVS, while if a PN junction is used a negative LIVS is measured, and vice versa for the PMOS. Keeping in mind that changing the GP type results in changing the nominal V_T of the transistor. Table 2-2 shows a summary of the different combinations of transistor type and diode orientations.

Table 2-2: FDPix available configurations for N- and P-type transistors and different diode orientations with the corresponding LIVS

FET type	PFET				NFET			
Configuration below the BOX								
Light effect	negative back bias	positive back bias	none	none	negative back bias	positive back bias	none	none
FET Light-Induced V_T-Shift (LIVS)	forward BB	reverse BB	none	none	reverse BB	forward BB	none	none
LIVS amplitude	Increases w/ P_{OPT} and BF	Increases w/ P_{OPT} and BF	none	none	Increases w/ P_{OPT} and BF	Increases w/ P_{OPT} and BF	none	none

2.3. Chapter two summary

In this chapter, the main subject of this thesis was introduced: the FDPix light sensor. Here is a short summary of the key points that were discussed:

- This thesis is about the study of the FDPix device. It consists in a monolithically integrated photodiode under the BOX of an FDSOI transistor, which results in a light sensor.
- The response is characterized by a Light Induced V_T shift (LIVS), which modifies the electrical characteristics of the MOSFET.
- There is no electrical connection between the sensing and the photosensitive elements of the FDPix, isolated from each other by the BOX.
- The LIVS is due to a capacitive coupling between the front and the back-channel interface, which is proper to a fully depleted structure. The back channel being dependent, also through a capacitive coupling, on the BOX/GP potential, the V_T of the transistor depends on the photogenerated charges in the GP which generates a potential variation. This is analogous to the back bias, although in this case, the back bias is optical, making the second gate of the FDSOI transistor, an optical gate.
- Structure-wise, the individual pixels are isolated from each other by the STI.
- The BF of the FDSOI transistor determines the conversion gain of the pixel.
- The pixel DC response to light illumination is logarithmic due the diode being biased in photovoltaic mode, resulting in an intrinsically high DR of about 120dB.
- Regarding the fabrication process, no extra cost is related to obtaining this technology; the standard UTBB FDSOI process flow is used, and the FDPix is obtained by modifying the substrate implantation type.
- One of the most promising properties of the sensor is its complementarity depending on whether an NMOS or PMOS is used, and on the diode orientation.

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CHAPTER THREE

Chapter 3 : Transient analysis: dynamic response and reset

Image sensors are dynamic devices that, depending on application, need to operate at high frame rate *[XU 2014]*. Some research groups developed CIS exceeding the 20Mfps (frame per second) for Ultra High Speed (UHS) imaging used in monitoring ultra-fast phenomena such as material breakdown, fluidics, high speed impact and so on *[KURODA 2017][KURODA 2016]*. Others *[GEURTS 2017]* combined HDR and high frame rates. The standard minimum frame rate for video capture is 50 to 60 fps. To evaluate where the FDPix stands regarding the maximum operational frame rate, the transient behavior of the device must be studied, modeled and optimized. It will determine the integration time/sensitivity tradeoff optimizations based on response times and will allow us to develop an efficient reset technique.

In the previous chapter, the FDPix steady state response was presented. We showed that the analytical model matched the TCAD simulations results and the opto-electrical characterizations. In this chapter, the capacitances involved in the transient responses are identified. The transient effects of the transistor and the photodiode are evaluated, and the developed model is confronted to the TCAD simulations and the electrical characterization. The response of the device to a light pulse is investigated in more details by varying the technological parameters. Then a Reset method based on the use of the electrical back gate of the FDSOI transistor is developed and evaluated to provide a stable dark level reference output.

3.1. FDPix transient components

The FDPix sensor is based on a capacitive coupling between front gate and back gate of the FDSOI transistor as was discussed in Chapter 2. When capacitors are involved in a circuit, they are always considered as parasitic that slows down the circuit dynamic response. It is usually quantified by the RC product, denoted as τ, which adds charging/discharging times consuming power when the currents or voltages are transitioning between levels. This is also true for the FDPix.

The considered transient responses are: the time it takes the system to respond to light when turned on (due to generation and accumulation of free carriers), and the time it takes to go back to its initial condition when light is turned off (evacuation/recombination of free carriers). Both are presented and the analysis are based on TCAD simulations and opto-electrical characterization, and the developed model is confronted to them.

Figure 3-1 below shows the experimentally monitored drain current of an N-type FDPix sensor with an NP oriented photodiode, when a light pulse is applied. We can notice the dissymmetry of the transient responses. The response of the sensor to the light tuning ON is relatively fast and the current decreases due to a positive LIVS. When turning the light off, the sensor takes more than 10 seconds to reach equilibrium. This transient time depends on the photodiode leakage currents. Thus, the very long transient time indicates the very low leakage current due to a low level of defect density in the photodiode. This low level of defect density is mainly obtained thanks to the thermal annealing that cures the ion implantation generated defects, as discussed in the previous chapter.

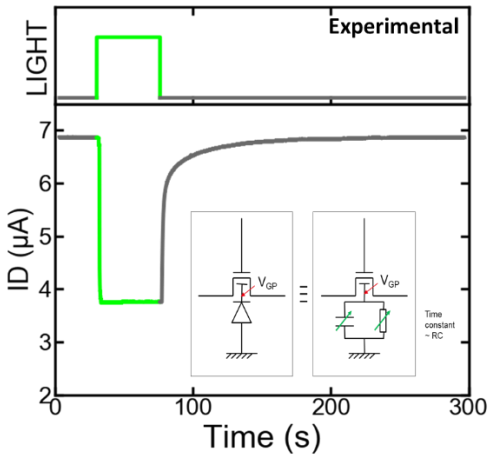

Figure 3-1: drain current monitoring for an N-FDPix with NP oriented diode when light is pulsed

The V_{GP} (GP potential) response times to the light depend on how fast the junction capacitance is charged (or discharged) represented by the RC product, τ (inset of Figure 3-1). Therefore, to fully understand the transient responses of the floating node, we will first identify the capacitances and time constants associated with both the FDSOI transistor and the photodiode. After that, the main capacitances influencing the behavior of the FDPix in transient are identified and the technological parameters influence on them are studied.

As was the case for the DC analysis presented in the previous chapter, the two components of the FDPix, the FDSOI transistor and the photodiode, are treated separately and calibrated. After that the final FDPix equivalent circuit is simplified depending on the supply biases and the transient responses are confronted to TCAD simulations.

3.1.1. FDSOI transistor capacitance network

The capacitance network of the FDSOI transistor is shown in Figure 3-2. It is common to divide them into two categories:

- Intrinsic capacitances, which are the capacitance responsible of the transistor effect. They are the ones adjacent to the gate including C_{OX}, C_{Si}, and C_{BOX}, denoted as C_{TOT} and expressed as:

$$C_{TOT}^{-1} = C_{OX}^{-1} + C_{Si}^{-1} + C_{BOX}^{-1} \tag{3-1}$$

- Extrinsic capacitances, which are the parasitic capacitances that slow down the device performances. They result from fringing fields and overlap between the gate and the S/D, and the junction capacitances between S/D and the substrate.

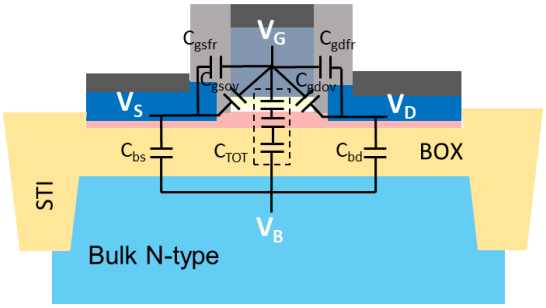

Figure 3-2: FDSOI equivalent capacitive network

The values of these capacitances must be calibrated to reproduce accurately the dynamic currents. C_{gg} is the total front gate capacitance, and C_{bb} is the total back gate capacitance, they can be written as:

$$C_{gg} = C_{ggi} + \left(C_{gsov} + C_{gsfr} + C_{gdov} + C_{gdfr} + C_{gbov}\right) \tag{3-2}$$

$$C_{bb} = C_{bbi} + (C_{bd} + C_{bs}) \tag{3-3}$$

Where C_{ggi} is the intrinsic gate capacitance denoted previously as C_{TOT}, and C_{bbi} is the intrinsic back gate capacitance. The other capacitances are extrinsic. It includes:

- The overlap capacitances between the gate and drain (C_{gdov}), the gate and source (C_{gsov}), and gate and bulk (C_{gbov}): C_{gdov} and C_{gsov} can be evaluated as a standard parallel plate capacitor taking L_D, the overlap length, and W to calculate the total area as $C_{gd/sov}=WL_DC_{OX}$. Since the S/D are highly doped, this capacitance can be considered as independent to the biases. The C_{gbov} capacitance results from the overlap between gate and

substrate outside of active region. It is considered negligible since it's much smaller than the other extrinsic and intrinsic capacitances.

- The fringing fields capacitances between gate and source (C_{gsfr}) and gate and drain (C_{gdfr}): These can be divided as outer fringe (through spacer) and inner fringe (through channel) capacitances. The inner fringe component is considered only when channel is fully depleted. In case of the formation of an inversion or accumulation layers, the gate to channel capacitance would be much higher than the inner fringe one (C_{gc}>>C_{ifr}) and thus will cancel it. The outer fringe capacitances can also be neglected with respect to the other extrinsic capacitances *[COLINGE 2002]*.
- The junction capacitances between S/D and bulk: These capacitances can be significant in the bulk architecture. However, in our case using thin silicon film and a buried oxide, the junctions are extremely thin and isolated by the BOX. They can be expressed as *[COLINGE 2002]*:

$$C_{bs\backslash d} = \frac{C_{BOX}}{\sqrt{1 + \frac{2C_{BOX}^2 V_{DB}}{qN_{GP}\varepsilon_{Si}}}} \tag{3-4}$$

Where V_{DB} is the drain-bulk voltage, and N_{GP} is the GP doping concentration. Therefore $C_{bs/d}$ is smaller than the BOX capacitance and is much smaller than the bulk junction capacitance which allowed performance improvement compared with bulk architecture.

As shown in Figure 3-3, the model reproduces accurately the total gate capacitance for a long channel FDSOI transistor. For short channel devices (not shown here), the drain to source capacitance must be included. On the C_{bb} results, an offset is observed between the model and TCAD simulations, but as we can see, the bulk capacitance is lower than the front gate capacitance, so this difference is tolerated in the simulation since it will not have a major effect on the transient properties.

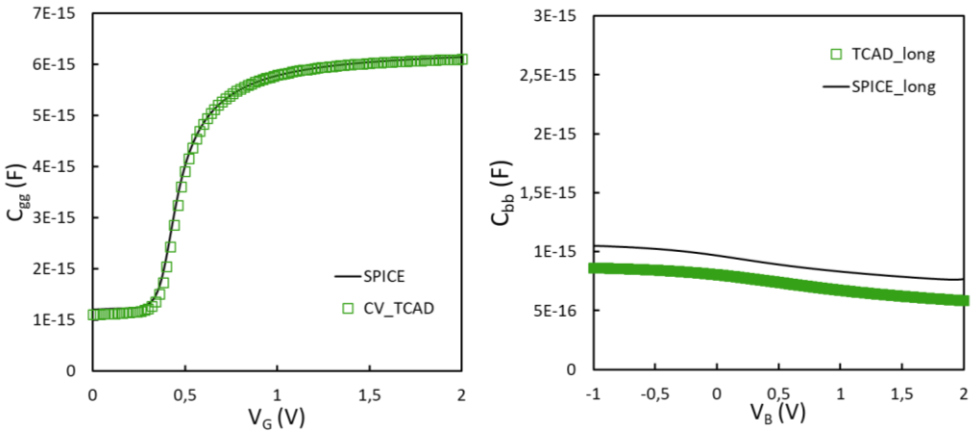

Figure 3-3: a) C_{gg} vs V_G b) C_{bb} vs V_G for NMOSFET GO2 showing good accordance between TCAD and simulation results

3.1.2. Photodiode equivalent RC circuit

The photodiode equivalent circuit for the forward and reverse biases are shown in Figure 3-4. The shunt resistance depends on the junction resistance, which is ignored in reverse bias since it is considered infinite (calculated value in

the order of 10^{15} Ohm). The leakage current, i.e. photocurrent, will reduce the shunt resistance in reverse. Hence, for high intensity illumination, the shunt resistance might need to be considered even in reverse bias. The series resistance represents the semiconductor and contact resistances. In our case, highly doped Si Well is biased, therefore this resistance is very small and ignored in the equivalent circuit.

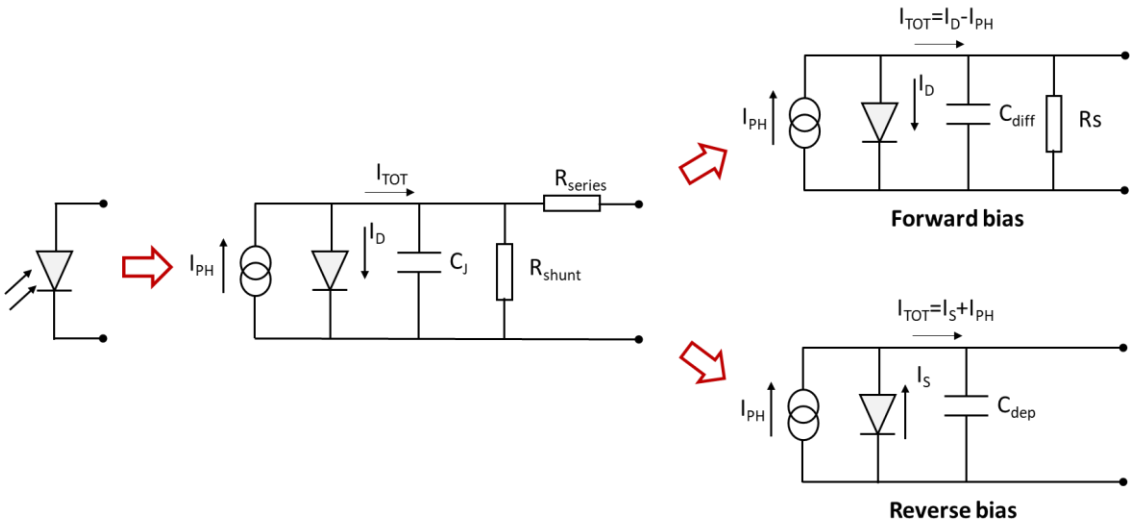

Figure 3-4: photodiode equivalent circuit approximation in forward and reverse bias

The capacitance depends on the dynamic current. Under different bias conditions, the carriers involved in generating the dynamic current are not the same, thus resulting in two different capacitances depending on whether the photodiode is biased in forward or reverse conditions. These two capacitances are:

a) The depletion capacitance: This capacitance is due to the drift of minority carriers through the depletion region that generate the reverse current. Since it is due to carrier's drift in depletion region where the electric field is high, the time constant can be neglected and the capacitance is thus considered independent of frequency *[SZE 2007]*. It can be derived by calculating the derivative of the charge in the junction, or can be considered as a parallel plate capacitor, and calculated using the depletion width given in equation (2-28) as:

$$C_{dep}(V_J) = \frac{\varepsilon_{Si}A}{W_{dep}} = \sqrt{\frac{q\varepsilon_{Si}A^2}{2}\left(\frac{N_aN_d}{N_a+N_d}\right)} * \frac{1}{\sqrt{\phi_{bi}-V_J}} \tag{3-5}$$

Where V_J is the diode bias. The zero bias capacitance is simply obtained by putting V_J=0V in the previous equation as:

$$C_{J0} = \frac{\varepsilon_{Si}A}{W_{dep0}} = \sqrt{\frac{q\varepsilon_{Si}A^2}{2}\left(\frac{N_aN_d}{N_a+N_d}\right)} * \frac{1}{\sqrt{\phi_{bi}}} \tag{3-6}$$

Where $W_{dep0}=W_{dep}|_{VJ=0V}$. Thus (3-5) can be re-written as:

$$C_{dep}(V_J) = \frac{C_{J0}}{\sqrt{1 - \frac{V_J}{\phi_{bi}}}} \tag{3-7}$$

C_{J0} is one of the main model parameters that will determine the transient behavior of the FDPix. A typical value of C_{J0} in our case is in the ~1.5 fF/µm² range. The variation of the depletion capacitance with applied bias depends on the doping of both sides of the junction. The higher the doping the less depletion, and thus less capacitance variation. For high speed diodes, this capacitance is often reduced by using a PiN diode as mentioned previously in Chapter 2. In the case of a PiN, the depletion width is considered equal to the intrinsic region width since it is depleted in all regions of operation. This will be further demonstrated in following sections.

b) The diffusion capacitance: This capacitance is due to minority carrier diffusion in quasi neutral regions under forward bias. Thus, by integrating the excess minority carriers in each region (p_{n0} for holes in N region and n_{p0} for electron in P region), the charge can be calculated as *[HU 2010]*:

$$Q_p = qL_p p_{n0}\left(e^{\frac{qV_J}{kT}} - 1\right) \tag{3-8}$$

$$Q_n = qL_n n_{p0}\left(e^{\frac{qV_J}{kT}} - 1\right) \tag{3-9}$$

Where L_p and L_n are the diffusion lengths of holes and electrons minority carriers respectively. Thus, by deriving the charge with respect to applied bias, the following expressions for the diffusion capacitances can be obtained for both regions as:

$$C_{diffp} = \frac{dQ_p}{dV_D} = \frac{q^2}{kT} L_p p_{n0}(e^{\frac{qV_J}{kT}}) \quad \text{and} \quad C_{diffn} = \frac{dQ_n}{dV_D} = \frac{q^2}{kT} L_n n_{p0}(e^{\frac{qV_J}{kT}}) \tag{3-10}$$

This results in the following expressions for the total diffusion capacitance:

$$C_{diff} = C_{diffN} + C_{diffP} = \frac{q^2}{kT}\left(L_p p_{n0} + L_n n_{p0}\right)e^{\frac{qV_J}{kT}} \tag{3-11}$$

This capacitance has an influence under high forward bias. The FDPix operation range as previously mentioned do not exceed the maximum V_{OC} of approximately ϕ_{bi}. When the diode is strongly forward biased, no carriers accumulate in the GP and therefore the sensor saturates. Thus, the diffusion capacitance is not expected to influence light detection transient, because the diode bias ranges where it becomes dominant are not explored.

Since it depends on the carrier diffusion lengths, and thus life time in the quasi neutral regions, the time constant associated to this capacitance but also the resistance can be reduced by introducing impurity in the diode that increases the SRH recombination and thus reduce carrier life time. High speed diodes can be obtained with this method. However, since our main application is detection, adding impurities will decrease the sensor sensitivity to light illumination as will be discussed in Chapter 4.

Therefore, the total junction capacitance is given by:

$$C_J(V_J) = C_{dep}(V_J) + C_{diff}(V_J) \tag{3-12}$$

The modeled photodiode capacitance is calibrated and compared with TCAD simulation as shown in Figure 3-5. The junction profile is the one presented in the previous chapter in Figure 2-22 with both sides of the junction doped to around 1e18 cm^{-3}. The main parameters to be tuned are the area and the doping profile or junction depletion profile, since these parameters determine most of the junction characteristics. C_{J0} parameter is extracted directly from TCAD simulation. As can be seen, the reverse bias is very accurately reproduced. In the forward regime, the model is clamped at a predefined value since our range of operation in forward regime for the intensity simulated will not exceed 0.6-0.7V.

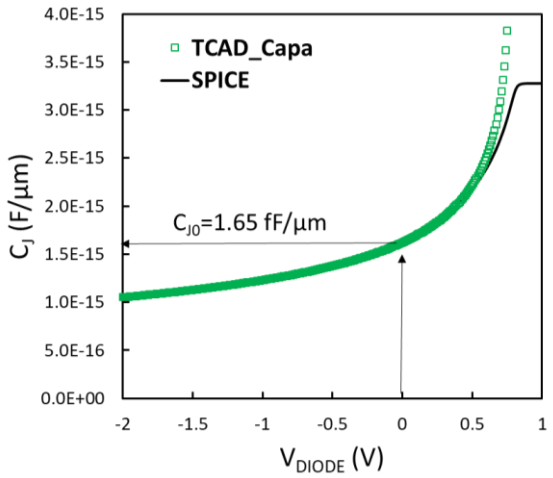

Figure 3-5: PN junction capacitance vs applied voltage, simulation vs TCAD

The value of C_{J0} according to equation (3-6) depends on W_{dep}. Figure 3-6 shows how the C(V) of a PiN junction with uniform doping regions (1e18cm^{-3} for the P-Well and 1.5e17cm^{-3} for the N-GP), varies for different intrinsic layer thicknesses (Ti), i.e. depletion region widths. We can see that C_{J0} as expected from equation (3-6) is reduced when using thicker Ti region in PiN junction. However, it should be noted that increasing the depletion region will also increase the reverse current (dark current of the sensor) due to higher SHR current, and thus reduce the $LIVS_{SS}$ value in DC due to lower V_{OC}. Thus, a compromise must be made, as will be further discussed in Chapter 4.

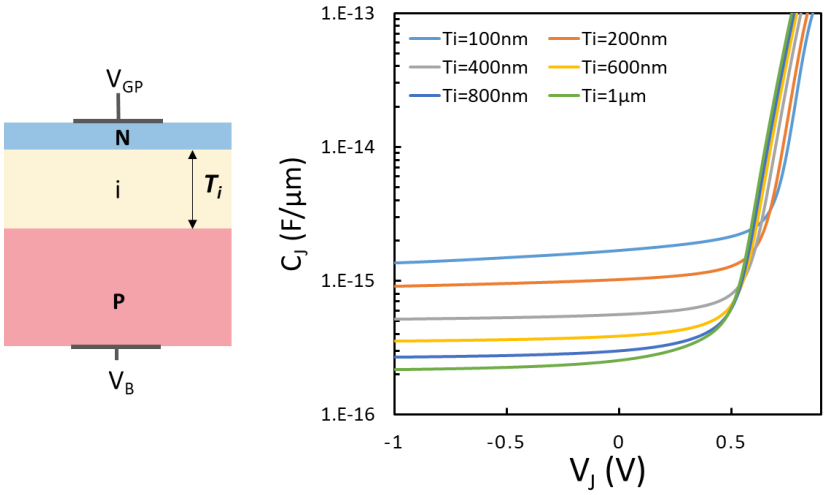

Figure 3-6: PiN diode C(V) for different intrinsic layer thickness ($V_J=V_B-V_{GP}$)

3.1.3. FDPix capacitance network

After considering all the capacitances, the equivalent circuit of the FDPix is shown in Figure 3-7. The back gate of the FDSOI transistor, which is now the GP, is floating, and is biased using the V_B applied on the Well, through the photodiode RC circuit.

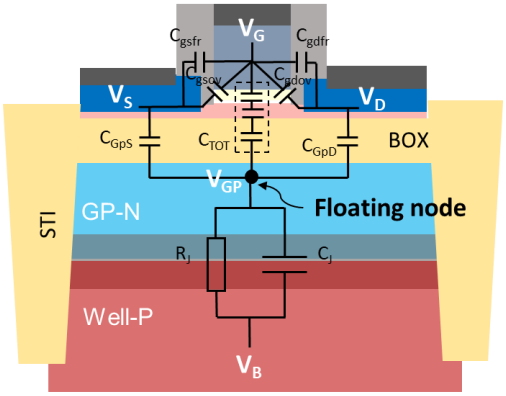

Figure 3-7: FDPix equivalent capacitance network

Figure 3-8 shows the transient SPICE simulation results vs TCAD when the potential of the GP of an N-type FDPix with NP junction is monitored while applying a light pulse. The SPICE model reproduces accurately the time constants associated with the device operation vs the TCAD results and thus can be used for further transient SPICE simulations.

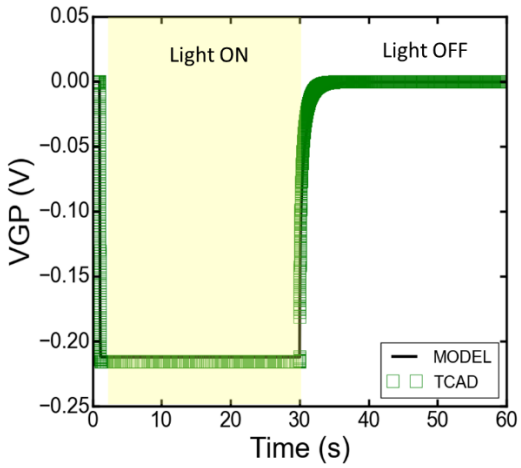

Figure 3-8: SPICE simulations vs TCAD monitoring of GP potential for FDPix NMOS with NP diode when a light pulse is applied

3.2. FDPix transient characteristics

The considered transient responses are:

- The time it takes the system to response to light when turned on (generation and accumulation of carriers)
- The time it takes to go back to initial condition when the light is turned off (evacuation/recombination of carriers).

Both are presented below using TCAD simulations. The simulated device is an N-type FDPix with NiP oriented diode (positive LIVS) with uniform doping regions, the transistor is biased in the subthreshold regime by applying a constant V_G of 0.44V and V_{DS} of 0.9 V. The time constant τ is measured at 63% of final signal level.

The response time of the FDPix will depend on the photodiode response times which can be expressed as:

$$\tau_j = \sqrt{\tau_{drift}^2 + \tau_{RC}^2 + \tau_{diff}^2} \tag{3-13}$$

Where τ_{drift} is the transient due to drift of photogenerated carriers in depletion region, it is dependent on the E-field and W_{dep} and is usually in the range of 100s of pico seconds to nano seconds *[GOUSHCHA 2017]*. τ_{RC} is the transient due to the junction capacitance and load resistance, this part is dominant in our case and is going to be analyzed in detail in the next section. τ_{diff} is the transient due to the charges generated in the quasi neutral region that diffuse to reach the depletion region. It is much higher than the drift component but since the N and P region are in the order of magnitude of the diffusion lengths, it is also going to be negligible in our case. Hence, the transient is approximated as the RC component and is demonstrated next.

3.2.1. Rise time (Light ON) transient

To evaluate the transient properties, the floating node (sensing node) equivalent capacitance (C_{eq}) must be first estimated for the different biases and light conditions. We start by assuming the sensor is at equilibrium when light is applied (no charge in GP). The four terminals of the FDPix are biased at constant voltages (V_{GS}=0.44V, V_{DS}=0.9V,

V_B=0V) and the only transient node is V_{GP}, this allows us to simplify the capacitive network shown in Figure 3-7 as shown in Figure 3-9 below.

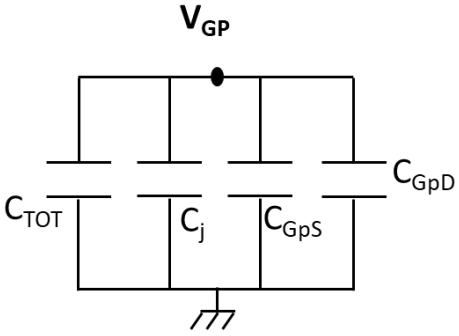

Figure 3-9: FDPix capacitance network when four constant bias are applied

Therefore, the floating node equivalent charging capacitance can be expressed as follows:

$$C_{eq} = C_{TOT} + C_J + C_{GpS} + C_{GpD} \tag{3-14}$$

Where C_{GpS} and C_{GpD} are equal (Sa=Sb) and approximately equivalent to C_{BOX}. C_{eq} is considered constant in the explored bias range. In fact, it does have a slight dependence on bias mainly due to C_J, however, it doesn't exceed the 9%, therefore we take the zero-bias value in our analysis. The rise time constant can be expressed as:

$$\tau_{rise} = RC_{eq} = \frac{V_{OC}}{I_{PH} + I_{dark}} * C_{eq} \tag{3-15}$$

This is demonstrated using TCAD simulations. The drain current is monitored as explained previously for different pulse light intensities as shown in Figure 3-10.a. τ_{rise} is extracted and plotted vs P_{opt} in Figure 3-10.b. As predicted from (3-15), the rising time is shorter for higher light intensities. The response time is linear for most of the intensities; however, we can observe a divergence between the model and TCAD possibly due to the I_{dark} that is not the same in both and becomes predominant for low light intensities.

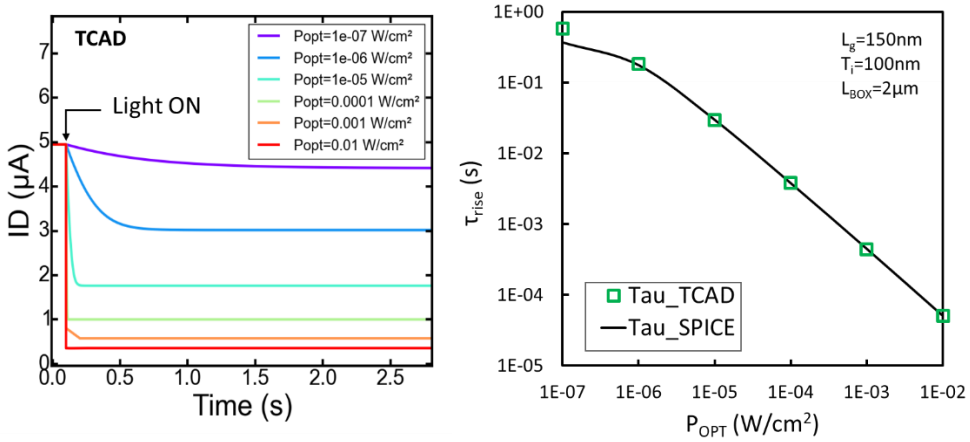

Figure 3-10: a) drain current monitoring for N-type FDPix with NP oriented diode representing the rise time of the sensor for different light intensities b) extracted τ_{rise} vs Popt confronting SPICE to TCAD

The rise time has a direct effect on the sensitivity of the sensor. It is the factor determining the tradeoff between speed (frame rate) and sensitivity as presented in the next section.

3.2.1.1. Integration time

The integration time represents the time of charge collection in the sensor, or the sampling rate since the signal is readout at the end of the integration time. It is related to the frame rate (FR) as shown below:

$$T_{int} = \frac{1}{FR} \tag{3-16}$$

Figure 3-11.b shows the calculated LIVS from the I_D variation ratio using equation (2-51) vs. P_{opt} at different frame rates. As we can see, when increasing the integration time i.e. reduce FR, the curve takes back the DC response shape with a log dependence on P_{opt}. For intensities $\geq 10^{-4}$ W/cm², changing the FR has no effect since the sensor reaches steady state. For intensities lower than 10^{-4} W/cm², the amount of collected charges depends on the integration time, therefore, the LIVS will depend on t_{int}. This discussion gives an insight to two possible regimes of operation for this sensor, namely when sampled before and after steady state is reached. This will be further investigated in section 3.3.2.

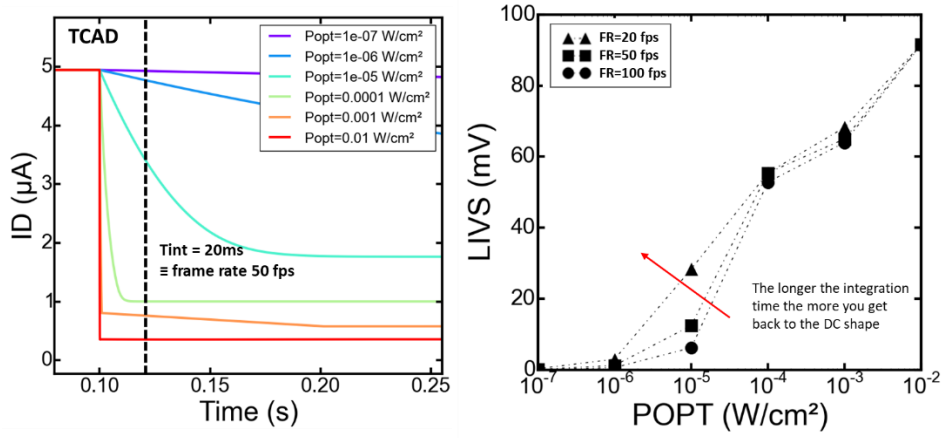

Figure 3-11:a) ID transient for N-type FDPix with NiP oriented junction at different Popt b) LIVS extracted at different frame rates (the 1e-3 W/cm² is to be extracted using better interpolation)

Since the integration time represents the time given for the junction capacitance to charge/discharge, the longer it is, the more charges are collected and the more sensitive is the sensor. Therefore, to achieve high sensitivity at fast frame rate, the rise time response of the sensor must be optimized. To do so, the RC_{eq} product must be decreased. In the next sections, we investigated the effect of technological parameters of the transistor and the diode on the FDPix response time.

3.2.1.2. Dependence on transistor parameters (L_G, T_{BOX})

The FDPix response time is studied by varying the transistor parameters to change C_{gg} and C_{bb}, keeping the same photodiode total area. The gate length (L_G) and the BOX thicknesses (T_{BOX}) are varied. As can be seen in Figure 3-12.a. and Figure 3-12.b, increasing the gate length slightly increases the time constant, but the effect is negligible,

and changing the BOX capacitance has no impact on the rise time either. This is expected from (3-14), since the junction capacitance is approximately one decade higher than the other capacitances in the circuit and thus is dominant. Therefore, the transistor parameters have no effect on the rise time of the sensor. This means that the sensor dimensions can be scaled down without altering the response time. Also, the BOX thickness can be reduced to obtain a higher conversion gain (i.e.BF) as discussed in Chapter 2, without degrading the response time. Therefore, the response time should not be affected negatively by using more advanced technological nodes.

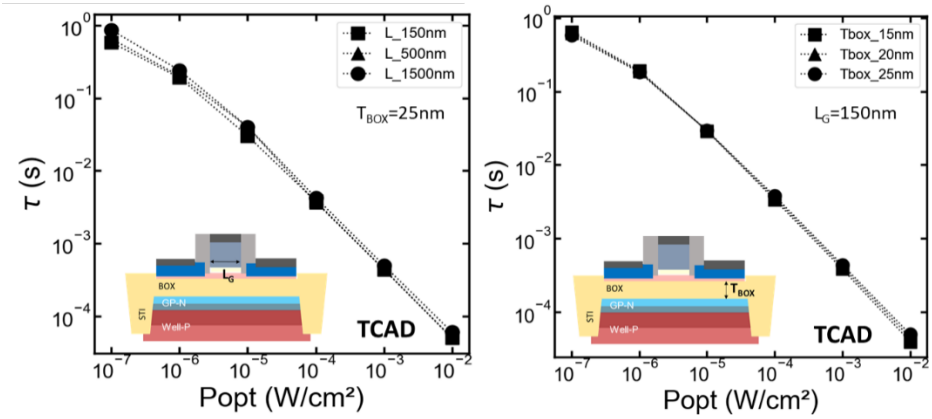

Figure 3-12:Rise time constant vs optical power density for a) varying L_G, b) varying T_{BOX}

3.2.1.3. Dependence on diode parameters (Ti, L_{BOX})

As discussed previously, the junction capacitance has a larger impact on the response time since it is larger than the other capacitances in the circuit keeping the dimensions of the transistor constant (L_G=150nm, T_{BOX}=25nm). First, τ_{rise} is measured for different depletion region widths (Ti), which as shown in Figure 3-6, changes the junction capacitance. Since C_{J0} has a direct dependence on W_{dep} as described in (3-6), C_J decreases by a factor of two when W_{dep} is doubled, which in turn decreases C_{eq} and thus τ_{rise} as shown in Figure 3-13.a. Increasing T_i not only decreases the junction capacitance but also, since the photon collection and carriers separation volume is larger, the photocurrent for a given intensity is higher, which decreases R and thus τ_{rise}.

The second significant parameter is the diode area denoted as L_{BOX} in the inset of Figure 3-13a. Since TCAD simulations are 2D, the width is by default always equal to 1µm. We can see from Figure 3-13.b. that decreasing the area increases the rise time, this can be explained as follows. Although decreasing the area will decreases C_{j0}, it also decreases the collection area and thus the photocurrent, which in turn increases the resistance in the RC_{eq} product. This I_{PH} reduction will counterbalance the decrease in C_{j0} and result in a higher τ_{rise}.

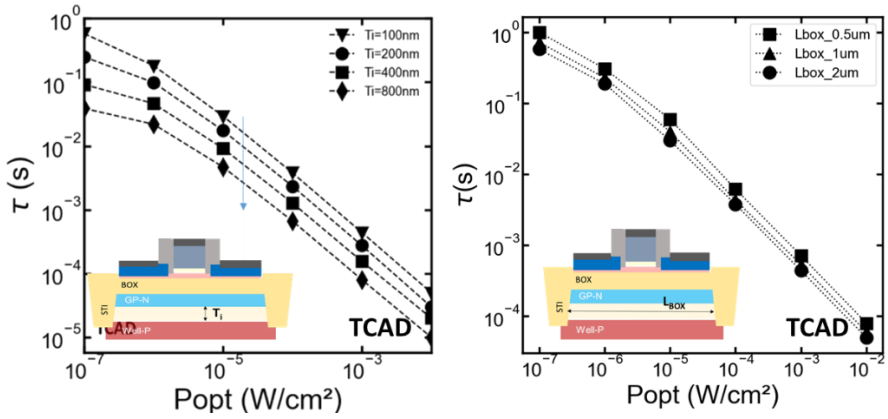

Figure 3-13: rise time constant vs optical power density for a) varying T_i, b) varying L_{BOX}

Therefore, to optimize the sensitivity/integration time tradeoff, a low junction capacitance should be privileged, however, decreasing the junction capacitance will also influence the DC parameters like the steady state level and Full Well Capacity (FWC), as will be further discussed in Chapter 4.

3.2.2. Fall time (Light OFF) transient

Assuming the FDPix is in steady state for a given constant light intensity. When the light is turned off, the photogenerated charges previously accumulated in the GP will evacuate or recombine until the GP reaches equilibrium. As previously shown in Figure 3-1, and shown below in Figure 3-14.a and 14.b. for different light intensities, this return to equilibrium decay (τ_{fall}) is long. When the light is off, the photogeneration stops (I_{PH}=0), thus the charge evacuation depends solely on the reverse current (dark current I_{dark}), and a long decay indicates a low dark current as previously mentioned. At low light intensity, the rise and fall transient time are almost identical since in both cases, the dark current is the dominant at low light, then in the rise time case, increasing intensity will increase the photocurrent, thus accelerate the decay.

Comparing with rising time, the C_{eq} in the RC_{eq} product is the same since the FDPix is biased the same manner. However, the resistance that previously depended on I_{PH} in this case depends on I_{dark} of the junction. From the experimental data shown in Figure 3-1, knowing the SS, C_{j0} (extracted from TCAD), and the BF, the dark current is estimated to be equal to ~5e-18A/µm² (0.5nA/cm^2) which corresponds to ~130 e/s for a diode area of 4µm².

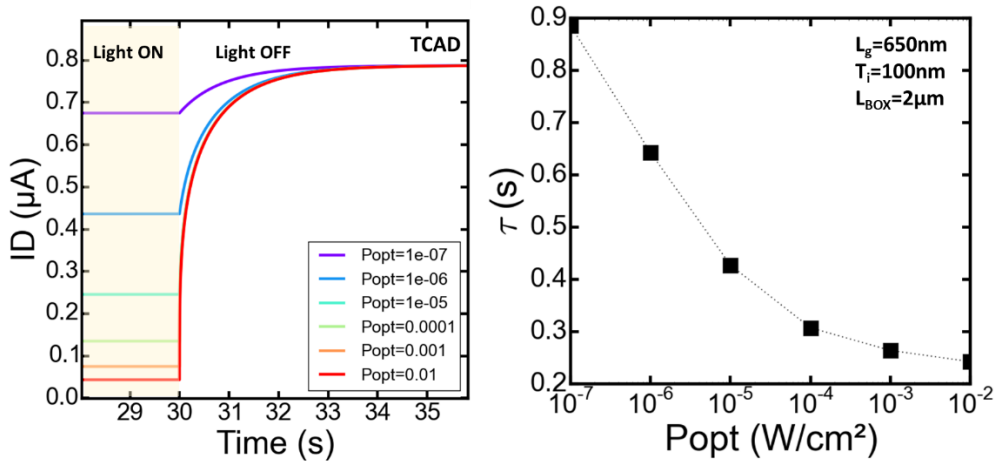

Figure 3-14:a) I_D monitoring for N-type FDPix with NP oriented diode for different light intensities b) extracted fall time vs P_{opt}

3.2.2.1. Dependence on diode parameters (Ti)

We previously identified the junction capacitance to be dominant on the rise time. It is expected to be the same for the fall time response. As was the case for the rise time, τ_{fall} is lower when using thicker T_i as shown in Figure 3-15. Using thicker intrinsic region junction reduces the photodiode capacitance and also, increases the dark current as described in (2-31) in Chapter 2, on which depends τ_{fall}. However, we can also see from Figure 3-15 that the steady state value is lower when increasing Ti as previously mentioned, due to higher leakage.

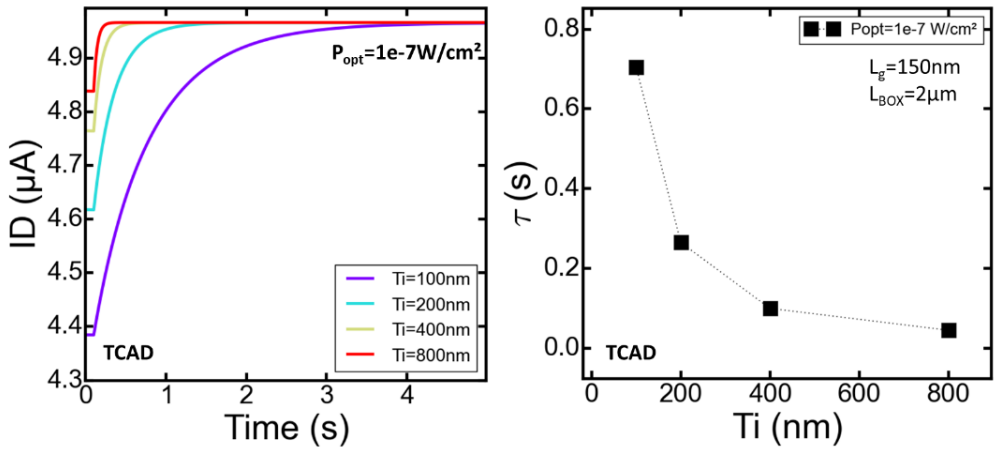

Figure 3-15: a) ID transient response for different Ti thickness at Popt=1e-7W/cm² b) extracted time constant vs Ti thickness

For the FDPix to operate at a conventional FR (20-50 frame/sec minimum for video capture), the long fall time measured is not practical for continuous readout. Therefore, in the following section, a reset scheme to initialize the GP potential and provide a dark initial level is investigated using the electrical back gate of the FDSOI transistor.

3.3. Reset operation and FDPix dynamic response

We investigated and developed a reset scheme based on the use of the electrical back gate of the FDSOI transistor to set the initial potential of the GP. This technique would prevent the need of a dedicated reset transistor per pixel, thus

maintaining the pixel size minimum, as illustrated in Figure 3-16. Keeping in mind that adding a transistor/pixel for reset has also been investigated and appeared to be functional. The results are presented in appendix C.

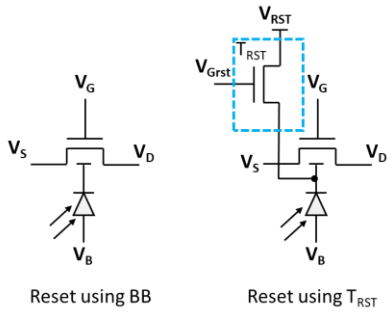

Figure 3-16: FDPix reset scheme: a) using the back bias, b) using reset transistor

The conditions to validate the efficiency of the reset are:

- Whatever the initial light intensity, when the reset is applied, the potential level must go back to the same value. In other words, the reset should be independent on light intensity.
- The initial value should be the one in dark conditions.
- An efficient reset is achieved when all the photogenerated charges are evacuated, avoiding any image lag in no lag.

Periodically resetting and sampling the sensor will result in an output response driven by the transient response of the floating node. The dynamic response is presented in section 3.3.2.

3.3.1. FDPix reset using back bias

The main idea is to apply a back bias to forward bias the junction as illustrated in Figure 3-17. After photogeneration (Figure 3-17.a) and accumulation of carriers in the floating GP (Figure 3-17.b), opposite type of carriers are injected to recombine with the photogenerated ones and bring the potential back to its initial level. This is done by forward biasing the junction as illustrated in Figure 3-17.c. where the junction forward current accelerates the decay time and resets the floating node. Thus, for an FDPix with NP oriented junction, a positive pulse is applied, while for a PN oriented junction, a negative pulse is applied. The initial potential of the GP after reset depends on the reset pulse parameters and the FDPix technological parameters.

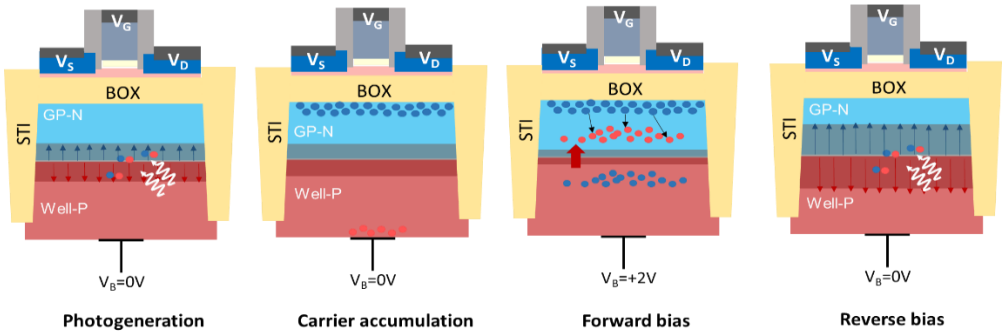

Figure 3-17: structure view of reset procedure: a) photogenerated carrier separation by junction electric field b) charge accumulation in GP c) forward bias the junction to reset d) initial condition reverse bias after reset

To verify the operation of this reset technique, the standard back bias of the FDPix must be first studied under dark conditions. Because of the presence of the junction in the bulk that adds a capacitance, the back-bias influence on the floating GP potential is subject to a capacitive divider. Furthermore, the transient response is also impacted, as can be seen in Figure 3-18 that shows the monitored GP potential of an N-type FDPix with NP junction, when a 1V pulse is applied on the back gate, with a pulse duration (t_{pulse}) of 10 secs. The SPICE and TCAD simulations are in excellent agreement. Four regions of operation are discriminated and analyzed. The important potential to be fully analyzed is the V_{RST} (analogous to the Vref mentioned in Chapter 1), which is the initial GP potential after reset that determines further pixel characteristics like the DR and FWC. Its dependence on the initial GP potential at t_{rise} (called V_{GPinit}) and pulse timing parameters is further analyzed and presented next.

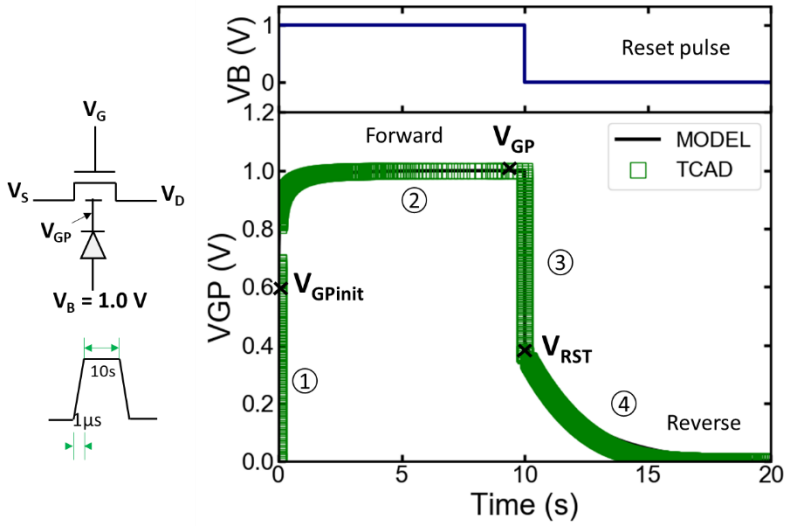

Figure 3-18: GP potential monitoring when applying a positive pulse to forward bias the NP junction

3.3.1.1. FDPix response to reset pulse in dark: Capacitive divider

When V_B is pulsed, the response of the GP can be divided into four regions as shown in Figure 3-18 where a 1V V_B pulse is applied on the back gate of an FDPix, and $|V_{GP}|$ is monitored:

- Region 1: V_B rising edge

During t_{rise}, dV_B/dt will generate an $i_j(t)$ that charges the capacitance C_{eq} with a $Q_{rise}(t)$ according to the following equation:

$$\#Q_{rise}(t) = \frac{1}{q}\int_0^{t_{rise}} i_j(t)\,dt \tag{3-17}$$

The dynamic current charges the capacitance during rising edge resulting in a voltage drop on C_J and making V_{GP} initially lower than V_B. This is shown in Figure 3-19.a. where a cut of the potential across the FDPix device was performed in TCAD at the rising edge of V_B, and where we can see that the change in V_B (here of 2V) was not entirely reproduced on the V_{GP}.

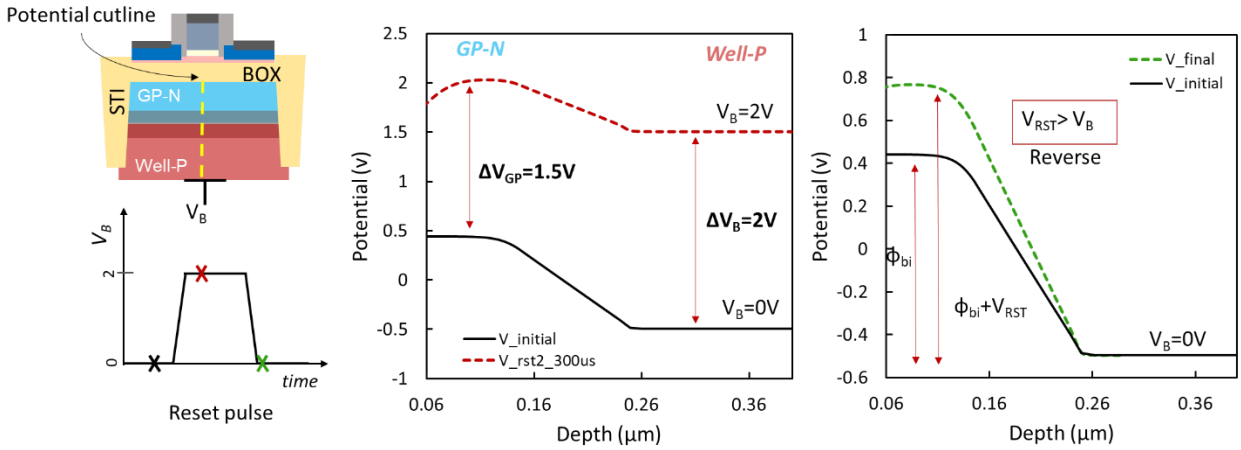

Figure 3-19:Potential across N-type FDPix NiP photodiode during VB pulse (red dotted line) and after the pulse (green dotted line) showing the initial reverse bias state of the junction (initial potential in black full line) (TCAD)

The initial potential of the GP denoted as V_{GPinit} in Figure 3-18, is determined by applying a capacitive divider across the equivalent circuit shown in Figure 3-20 below.

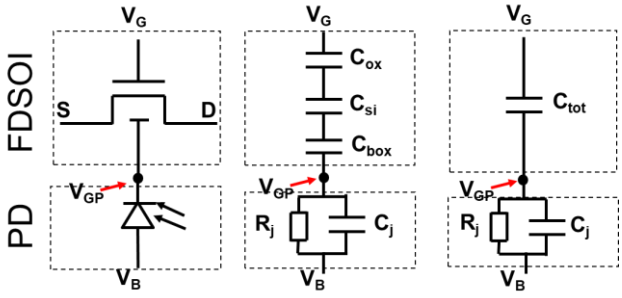

Figure 3-20: Reset mechanism for FDPix with NP photodiode

Considering the initial potential equal to zero, V_{GPinit} can be expressed as follows:

$$V_{GPinit} - V_B = (V_G - V_B) * \frac{C_{TOT}}{C_{TOT} + C_j}$$

$$V_{GPinit} = V_G\left(\frac{C_{TOT}}{C_{TOT} + C_j}\right) + V_B\left(1 - \frac{C_{TOT}}{C_{TOT} + C_j}\right) \tag{3-18}$$

V_{GPinit} thus depends on both V_G and V_B values. In the previous simulations V_G is constant, biasing the transistor in subthreshold. Since during rising edge the junction is forward biased, the current $i_j(t)$ is high, and no delay is observed on the V_{GP} that reaches V_{GPinit}. The total number of stored charges during rising edge can be expressed as:

$$\#\Delta Q_{init} = \frac{(V_B - V_{GPinit}) * C_{eq}}{q} \tag{3-19}$$

- Region 2: V_B pulse constant

Starting from V_{GPinit}, V_{GP} drifts till it reaches its steady state value which is the applied V_B. this corresponds to the discharge of the equivalent capacitance. If steady state is not reached, the GP potential $V_{GP}(t)$ can be calculated by integrating the current as follow:

$$V_{GP}(t) = \frac{1}{C_{eq}} * \int_{t_{rise}}^{t} \big(i_{dark}(t) + i_{PH}(t)\big)dt + V_{GPinit} \tag{3-20}$$

Thus, the value of the $V_{GP}(t)$ will depend on the light intensity. The transient time from V_{GP}=V_{GPinit} to V_{GP}=V_B depends on the leakage current of the diode which will allow the injected charges during rising edge to recombine (discharge of C_{eq}) for the GP to reach equilibrium.

- Region 3: V_B falling edge.

When the back-bias pulse is removed, the injected carriers in the quasi neutral region will charge the diode capacitance. In this case, there are minority carriers as opposed to the majority carriers generated by light illumination. When V_B returns to zero, the same capacitive divider described previously takes place, and the capacitance is charged. If steady state was reached, the potential drop is symmetrical and the initial V_{GP} just after V_B falling edge denoted as V_{RST} will represent the drop on the capacitance and is equal to:

$$V_{RST} = V_B - V_{GPinit} \tag{3-21}$$

However, if steady state was not reached during the pulse, meaning that the capacitance is not fully discharged when the pulse goes back to zero, the V_{RST} will be lower than its value shown in (3-21). The injected charges during falling edge will recombine with the residual charges from rising edge, and then charge the capacitance. Due to the voltage drop on C_J, at V_{RST} the junction is reverse biased (V_{RST}-V_B<0) and thus the initial state of the junction just after reset is reverse bias. This is shown in Figure 3-19.b where we can see that the final potential just after reset is higher than the initial one. Also, according to (3-20), the $V_{GP}(t)$ value depends on I_{PH}, this means that the initial potential (V_{RST}) is light intensity dependent. However, the higher the photocurrent, the faster the capacitance is discharged. Thus, for high intensity incident light, V_{RST} becomes independent of P_{opt}. This is further discussed in section 3.3.3.

- Region 4: V_B back to ground.

After that, the system goes back to equilibrium at a rate that depends on reverse leakage current since the diode at V_{RST} is reverse biased. Thus, we can expect a dependence on photocurrent as well, as will be shown in later sections. Important points are:

- The back-bias pulse will charge the junction capacitance by injecting minority carriers in quasi-neutral regions.
- These excess carriers in the GP will generate a potential which after the reset pulse, results in reverse biasing of the junction.
- The junction after reset is in reverse, analogous to the standard image sensor reset. Meaning that the charges are integrated before they reach steady state in forward regime, for a certain range of light intensities depending on $t_{int.}$

3.3.1.2. FDPix response to reset pulse under light illumination

Now the reset using the back gate is evaluated in the presence of light and photogenerated charges in the GP. First, we will see how the decay time is reduced by resetting just after the light is turned off highlighting the dependence on the initial state of GP. After that, resetting while a constant light illumination is applied, thus in the presence of a constant photocurrent. The simulations and opto-electrical characterization presented hereafter were performed for different light intensities (more details in appendix B). All the terminals of the transistors are biased with constant voltages, only the bulk (V_B) is biased in a transient signal.

3.3.1.2.a. Reset after light turned off

Considering the case where initially the GP is in steady state at a potential value corresponding to the V_{OC} of the light intensity applied. The light is turned off and at the same time a reset pulse is applied on the back gate. When the pulse is applied, the photocurrent is zero since the light source is off which stops the photogeneration. The transient decay previously observed that depended solely on dark current, is now much faster since the diode is forward biased and an $i_j(t)$ current will increase the recombination of photogenerated carriers.

The reset pulse parameters should be optimized to ensure all the photogenerated charges are evacuated. To evaluate the impact of these parameters, we extracted from SPICE simulations the potential offset $\Delta V_{RST,}$ which is defined as the delta between the initial GP potential V_{RST} in dark (reference level), and the V_{RST} in case a light intensity was applied. ΔV_{RST} ideally should be equal to zero. If it is not equal to zero, the reset is not efficient enough and all the charges of the previous frame were not evacuated which results in image lag.

- V_B pulse amplitude:

The idea is to check if this offset between dark level and light is reduced when increasing V_B to insure the same level is achieved. Since the amplitude of the reset pulse will determine V_{GPinit}, the higher the amplitude the higher is the initial ground plane potential, thus the higher is the number of excess minority carriers introduced in the GP. Figure 3-21.a. shows ΔV_{RST} vs Popt for V_B values ranging from 0.8V to 1.8V. The offset is smaller for higher V_B since more charges are injected in the floating node.

A high reset amplitude is preferred to ensure all the photogenerated charges are evacuated and that the potential level is stable after the pulse for all light intensities. However, increasing the pulse amplitude will also increase the V_{RST} level. If V_{RST} is too high, the transistor might not be operating in subthreshold region which is necessary for the FDPix.

- V_B pulse width:

According to (3-20), when varying the pulse width (t_{pulse}), the amount of injected charges during rising edge that recombine will change. Therefore, it will affect the amount of charges in the GP. When plotting ΔV_{RST} vs P_{opt} for different pulse widths, as shown in Figure 3-21.b, the same trend as for varying the pulse amplitude can be observed. The longer the pulse, the longer the capacitance has time to discharge resulting in a smaller offset. We used a pulse width of 300µs in future simulations with a pulse amplitude of |2V|, which results in an efficient reset performance keeping the operation of the MOSFET in subthreshold.

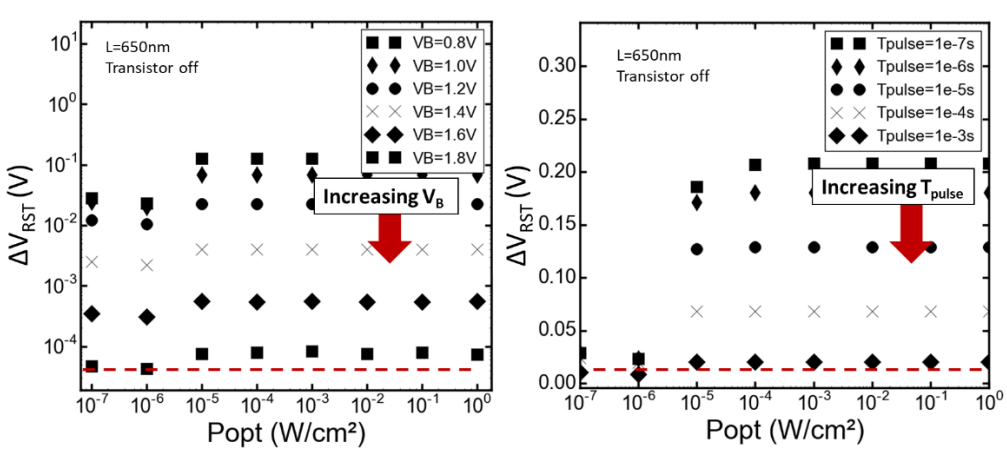

Figure 3-21: GP potential offset vs optical power density for a) different V_B b) different t_{pulse}

Figure 3-22 shows the SPICE simulation results where different light power densities are applied. The drain current of an N-type FDPix sensor with PN oriented junction (V_T decreases with light, negative LIVS) is monitored while applying a reset pulse immediately after the light is turned off. The pulse parameters optimized are 300µs width and -2V amplitude (negative to forward bias the FDPix PN oriented junction).

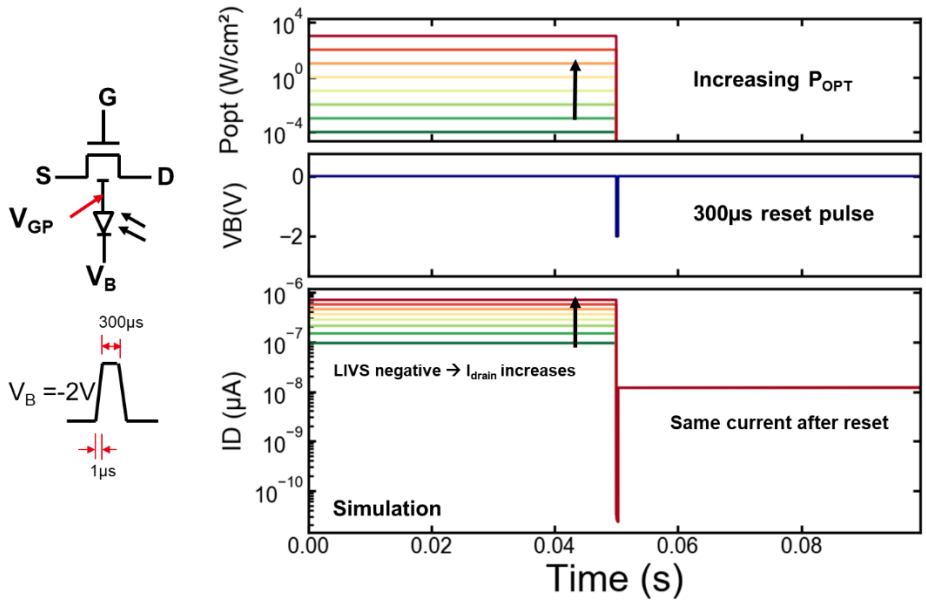

Figure 3-22: Drain current of N-type FDPix with PN diode when reset pulse of -2V amplitude and 300µs width is applied after turning the light off

We can see that after the reset pulse is applied, the current returns to the same level, independently of the initial light intensity. V_{GPinit} doesn't depend on light according to (3-18), the capacitance is fully charged during the rising edge and the drop on it is thus the same. The GP potential at pulse level ($V_{GP}(t)$) however does depend on light since the transient due the capacitor discharge is a function of leakage current according to (3-20), but since in this case the light is turned off, the transient doesn't depend on I_{PH}, and the same $V_{GP}(t)$ is achieved which results in the same V_{RST}.

This means that all the photogenerated charges recombined and the new potential level depends on the charges injected during the reset pulse. Thus, the transient when light turns off is reduced and a new acquisition can start.

3.3.1.2.b. Reset under constant light illumination

Since in real application, the incoming light on the sensor is constant or varies with time, the reset is also validated for these two cases, with the second one being addressed in section 3.4. Opto-electrical characterization are used to evaluate the reset for an N-type FDPix with PN photodiode. The light illumination is applied using an optical fiber in Front Side Illumination (FSI) manner. We vary the optical power density by using different obturator positions and numerical aperture (NA). More details on the characterization setup can be found in appendix B.

The applied voltages at the transistor terminals are shown in Figure 3-23 with the reset pulse sequence. We used a 50 frames/second frame rate, i.e. 20ms integration time. Since the diode has PN orientation, a negative bias of -2V is applied to forward bias it. The monitored transient I_D for the different applied intensities is shown in Figure 3-24. We can see that the current changes as a function of light intensity and that after the reset pulse, it goes back and start at the same level for the range of the intensities measured. By this test, we validated the efficiency of using the back gate of the FDSOI transistor as a reset gate.

From Figure 3-24, we can notice two types of evolution of the drain current during the integration time, namely before steady state, and after steady state is reached. This indicate that the response of the sensor is not just logarithmic since it doesn't reach steady state for all the intensities when sampled at 20ms, as previously discussed in section 3.2.1. We can also notice from this figure a sharp transition in the drain current evolution in time. This is assigned, as will be explained in more details in the following section, to the photodiode operating in two regimes. The transition between the two results in a sharp transition on the current. By working in transient and applying a reset at a certain frame rate, the sensor response will depend on the number of charges either integrated or accumulated in the GP, as investigated in more details in next section.

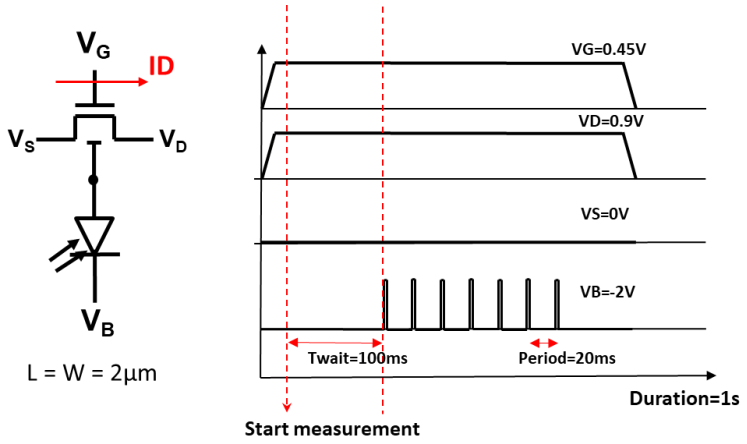

Figure 3-23: transistor terminals bias during reset operation

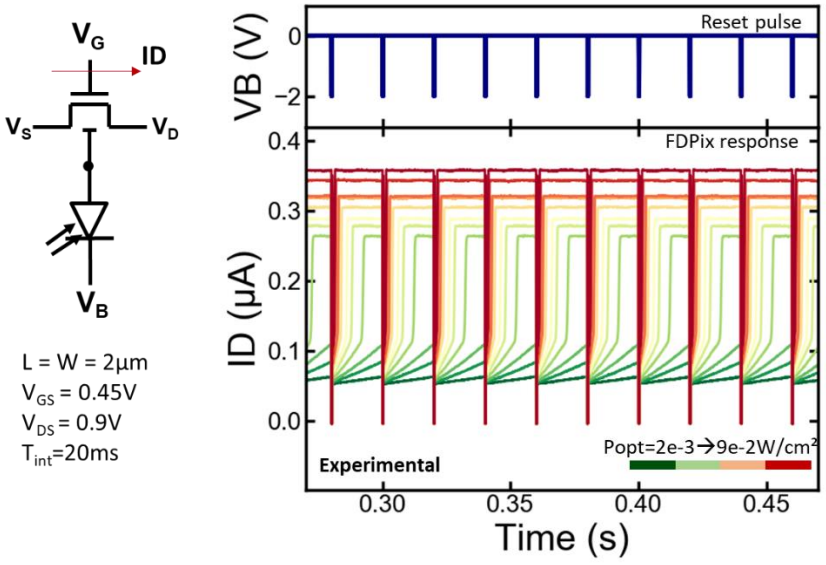

Figure 3-24: FDPix drain current monitoring while applying constant light at different intensities at 50 fps

3.3.2. Regions of operation

3.3.2.1. Steady state mode (logarithmic response)

When the FDPix reaches steady state, the drain current level corresponds to a V_{OC} as previously explained in Chapter 2. Hence, when the integration time is long enough for the sensor to reach steady state, the response is logarithmic as shown in Figure 3-25. This mode can be implemented in a continuous readout manner or by using adaptive integration time methods. Since the saturation is reached faster for higher light intensities, the integration time t_{int} must be light intensity dependent.

As mentioned before and modeled in Chapter 2, the logarithm response results in a high DR. This mode of operation has some advantages. Since the junction is operating in photovoltaic mode, the dark current is very low, and thus the sensor is highly sensitive in long acquisition. However, the sensitivity at low light is limited.

3.3.2.2. Integration mode (linear-log response)

When the sensor is sampled before it reaches saturation, the sensor output corresponds to charge integration. After the reset pulse, the diode is reverse biased, and the junction capacitance is charged. Starting from this reset potential (V_{RST}), the photogenerated charges will increase the reverse current of the diode, resulting in a capacitor discharging time that depends on light intensity. This corresponds to the decay observed in region four of Figure 3-18. Therefore, using equation (3-20), V_{GP} level at t_{int} can be described as:

$$V_{GP}(t) = \frac{1}{C_j}\int_0^{t_{int}} i(t)dt \tag{3-22}$$

Considering a constant illumination, $i_j(t)$ is constant and equal to $I_{PH}+I_{dark}$, $V_{GP}(t)$ can be calculated as:

$$V_{GP}(t) = \frac{1}{C_j} * (I_{PH} + I_{dark}) * t_{int} \tag{3-23}$$

This expression is valid until the diode reaches forward bias region. Starting from there, the capacitor initially charged with excess minority carriers during reset, is discharged and the photogenerated charges starts to accumulate in the GP. The junction reaches open circuit condition (photovoltaic mode) and the logarithmic response previously measured is obtained as shown in Figure 3-24. The sharp transition previously observed is thus assigned to the photodiode operation reaching open circuit condition.

Therefore, when the sensor is sampled while in transient (not steady state), V_{GP} has a linear dependence on P_{opt} and the response of the sensor, i.e. LIVS, is thus linear, as shown in Figure 3-25.b. The slope of the linear response, later refer to as sensitivity, can be modeled as:

$$\frac{dV_{GP}}{dP_{opt}} = \frac{t_{int}}{C_j} \tag{3-24}$$

The equivalent LIVS linear region slope can be calculated by multiplying (3-24) by the BF as:

$$\frac{dV_{GP}}{dP_{OPT}} * \frac{dV_T}{dV_{GP}} = \frac{dV_T}{dP_{opt}} = \frac{t_{int}}{C_j} * BF \tag{3-25}$$

Therefore, the sensitivity of the linear response depends primarily on the integration time, junction capacitance, and BF, while the log sensitivity only depends on BF.

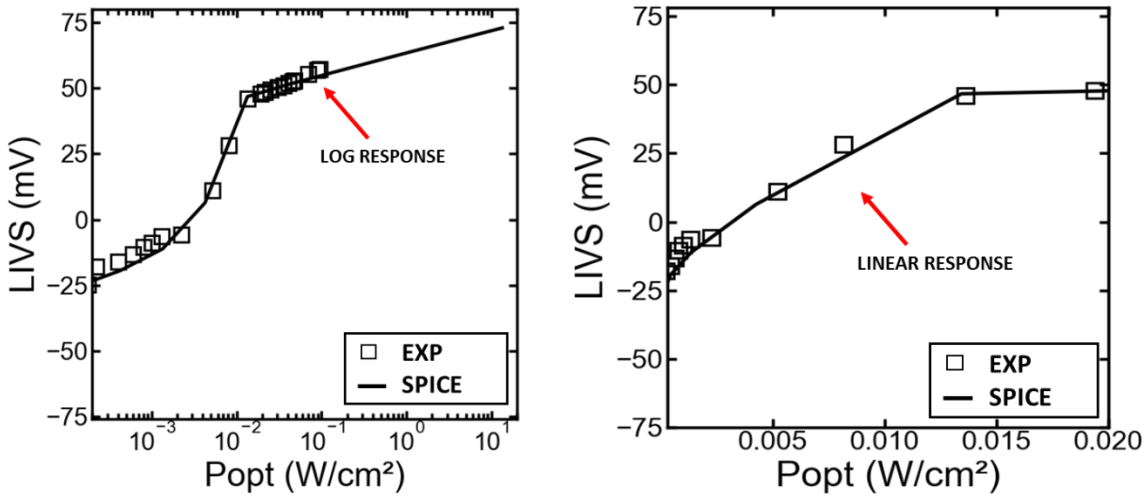

Figure 3-25: LIVS vs optical power density highlighting the two regions of operation of the FDPix a) log response in accumulation mode, b) linear response in integration mode

The FDPix has thus two responses: logarithmic when steady state is reached which extend the dynamic range for high intensities, and linear when sampled during integration which increases the sensitivity of the sensor for lower light intensities. Either of these two modes can be used or combined during operation since they depend on integration time. Both region's DR and sensitivity will be studied and optimized in Chapter 4.

3.3.3. History effect (lag, residual charges)

When resetting the floating node, all the photogenerated charges must be evacuated so that when a new acquisition starts, the initial potential in the GP is the same whatever the light intensity variation. If this is not the case, a lag can be observed on the obtained image due to residual charges from previous frame.

In section 3.3.1.1, we mentioned that when steady state is reached during the pulse and after, V_{GP} response to a V_B pulse is symmetric. It corresponds initially to V_B minus the drop on the junction capacitance, then the transient during the discharge of that same capacitance. However, when steady state is not reached, which is the case for lower light intensities and dark condition, the capacitance is not fully discharged because the reset pulse and/or the integration time are not long enough. This results in the drift of the GP potential under applied reset pulse train until it reaches steady state. This drift is due to the incomplete discharge of the capacitance after the pulse. Therefore, when the following pulse is applied, the drop on C_J is different since there are remaining charges from the previous pulse. Therefore, the potential level V_{GPinit} that depends on that drop will stabilize after a few pulses, enough to charge the capacitance completely.

This effect is illustrated using SPICE simulations in Figure 3-26.a. For low light intensities, the GP potential drifts until the capacitance is fully charged. Therefore, frames that are sampled at different times will result in different output for the same intensity. This can be observed in Figure 3-26.b. where the V_{GP} level vs P_{opt} shift depending on sampling time for lower intensities.

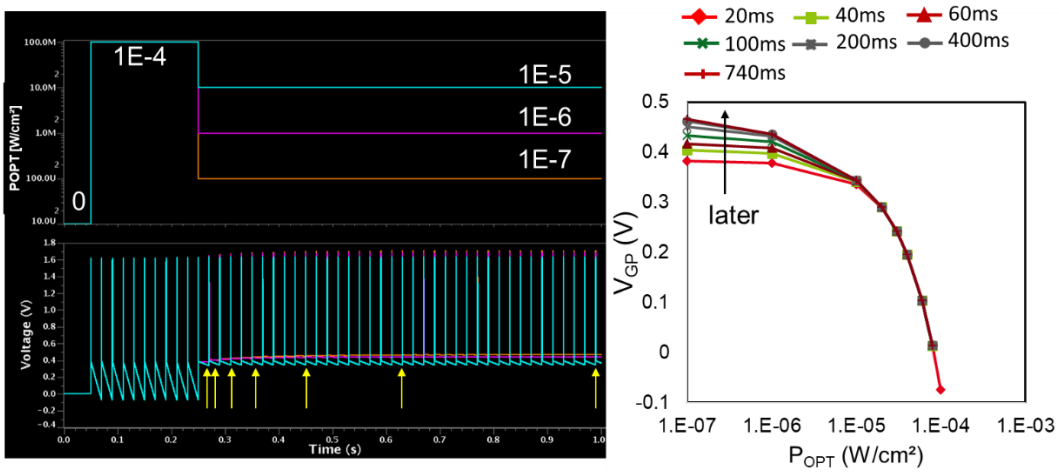

Figure 3-26: SPICE simulation of V_{GP} for different intensity variations at different sampling time

This drift was also observed experimentally for a range of low intensities, when pulsing an N-type FDPix with PN junction and is shown in Figure 3-27. Here the device is similar to the one tested in Figure 3-24 with V_G=0.44V and V_{DD}=0.9V. What can be noticed is that the drift time constant depends on light intensity. The higher the light intensity, the higher is the reverse current, and thus the discharge of the capacitance, which reduces the time constant.

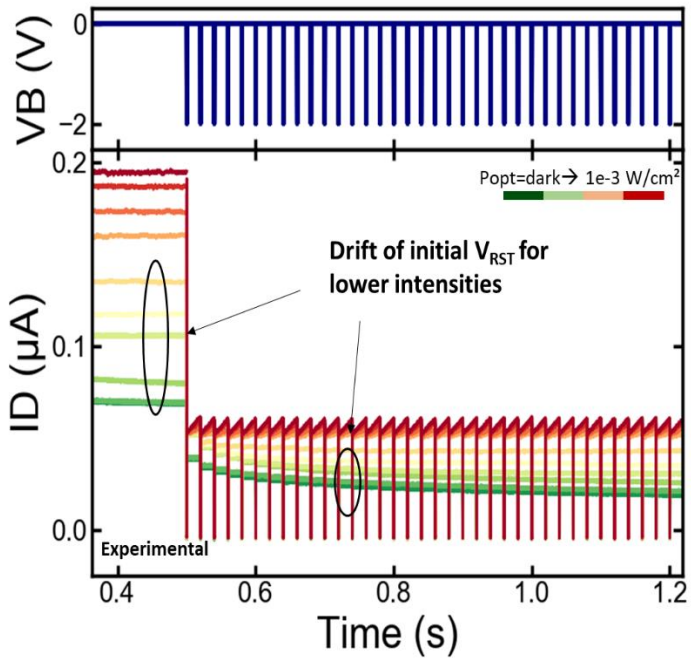

Figure 3-27: drain current monitoring while applying reset pulse train on an N-type FDPix with PN oriented diode

This drift in potential as mentioned before, will be the source of error when sensing low intensities. To reduce this transient, a higher reset pulse amplitude can be used, or a longer pulse width. Both these parameters increase the charging speed of the capacitance which will reduce the transient. However, during our study, we kept using the same reset parameters and extracted the data from the stationary region of operation.

3.4. FDPix response to variable light illumination

For the FDPix to be used as a 1T pixel, drain current variations are measured at the output. SPICE simulation is used to evaluate the response of the device to a variable light source. A pulse sequence of different light intensities is applied on an N-type FDPix with NP oriented junction and the drain current is monitored, while using a 20ms integration time and resetting by applying a +2V pulse train on the transistors back gate. The transistor is biased to work in subthreshold region, thus using a V_G close to its V_T of 0.38V. The results are shown in Figure 3-28. By sampling the current level at the end of integration, the light intensity variation can be measured, and the image can be reproduced. Since the diode is NP oriented, the V_T of the transistor increases with light intensity, hence the drain current at fixed V_G is decreasing with light.

We can see the impact of the history effect when switching back to dark or lower intensity. Due to the transient, the current level is hardly accurately detected. Also, these low-level illuminations will probably fall in the noise floor. Further studies to set the noise floor should be considered to determine the minimum measurable current variation in the circuit. However, measuring a current requires a higher power consumption. In Chapter 5, different circuit configurations are proposed to convert the current variation into voltage variation at the output.

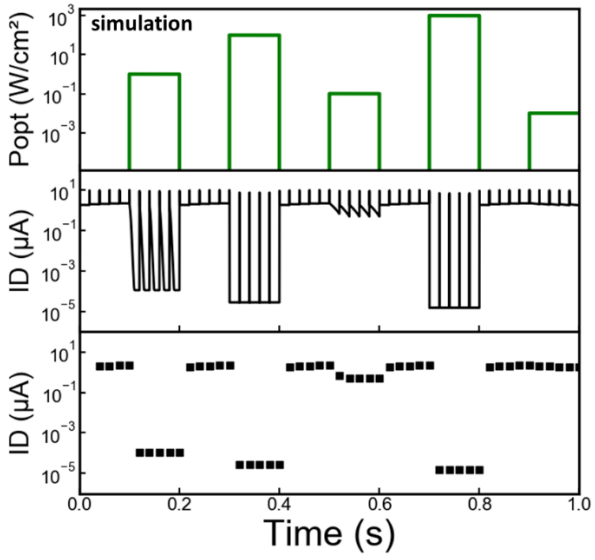

Figure 3-28: SPICE simulation for N-type FDPix with NP junction drain current response to variable light intensities, using a 20ms integration time.

The study of light variation detection was also performed experimentally by applying a constant light and using an optical chopper at different frequencies (see appendix B for the characterization setup), while applying a reset pulse train on the back gate of an N-type FDPix PN oriented junction. The monitored drain current is shown in Figure 3-29.

Two different light intensities are applied, the chopper frequency was 4Hz, and a 20ms integration time is used. As was the case for SPICE simulation, a drift is observed on the dark level due to history effect. Otherwise, for higher intensities, the sensor level corresponds to the applied light illumination and the reset is efficient.

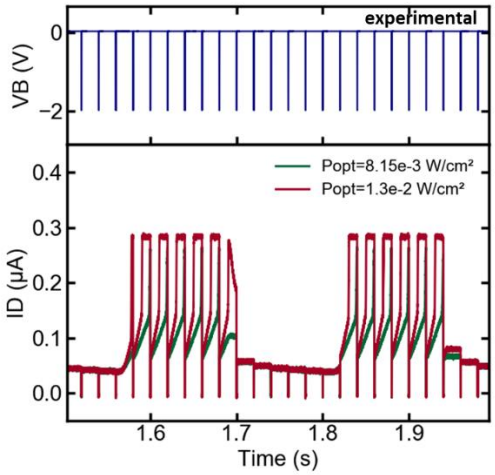

Figure 3-29: drain current transient for an N-type FDPix with PN oriented diode for two different light intensity and using an optical chopper at 4Hz frequency

Hence, the FDPix sensor is operational and effectively reset using a back bias. The history effect can be reduced by optimizing the reset pulse as previously mentioned. The basic response and operation of the sensor in DC and transient have been presented. The next chapter presents the optimization of the technological parameters to improve the response, and the main characteristics of the sensor are presented.

3.5. Chapter three summary

In this chapter, the transient response of the FDPix sensor was studied and modeled, and an efficient reset scheme was demonstrated. The key points are summarized below:

- Due mainly to the junction capacitance, the response of the sensor is slow when light pulse is applied, especially for low intensities.
- The transient is well modeled and described in the developed compact model for SPICE simulations.
- Resetting the GP node using the back gate is an efficient and innovative way to reset while maintaining small pixel size.
- The sensor has a linear response at low intensity since biased in reverse after the reset pulse, and logarithmic for higher intensities where the saturation is reached, and the V_{OC} is measured.
- The lin-log response allows high DR (~120dB expected based on TCAD simulations) while maintaining good sensitivity at low light intensities.
- A history effect needs to be managed for low light conditions by optimizing the reset pulse.
- Finally, the sensor was tested when a variable light was applied, and the signal was reproduced successfully in both simulation and experimental.

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CHAPTER FOUR

Chapter 4 : FDPix optimization and tradeoffs

So far, the structure of the FDPix was presented and its operation in DC and transient was discussed. The device performance dependence on the technological parameters was briefly introduced. This chapter presents guidelines to sensor optimization by varying the technological parameters, and operation conditions. The main sensor properties are introduced and quantified, and solutions to improve them are presented. The light detection efficiency is also addressed. Several integration solutions are proposed. The standard front side illumination (FSI) FDPix is optimized by using back side illumination (BSI), the junction shape is improved to collect the charges more efficiently, and the FDPix is presented as a universal readout circuit considering different materials as photosensitive elements. Other aspects of the FDPix such as the temperature stability and scaling are also discussed in this chapter. The main goal being to present the possibilities of future implementation of the FDPix and how to improve its performance, as a function of targeted applications.

The main properties addressed in this chapter are:

- Conversion gain: In the case of the FDPix, it is the LIVS generated for one electron in the back plane. Therefore, it is highly dependent on the body factor and is expressed in $\mu V/e^-$.
- Sensitivity: We define the sensitivity as the slope of the LIVS vs optical power (Popt) curve. For the FDPix, two sensitivities are defined: the linear region sensitivity in mV/lux.s, and the log region sensitivity in mV/dec.
- Dynamic Range (DR): The minimum and maximum detectable light intensities will determine the overall DR of the sensor. A high DR is necessary to capture a wide range of intensities in a scene. Since the sensor has two responses, the DR of each is discussed.
- Full Well Capacity (FWC): how many charges can the photodetector detect before saturation for each region of operation.
- Response time: how fast the sensor responses to light. As discussed in Chapter 3, there is a tradeoff between speed and sensitivity.
- Integration time: the DR of linear vs DR of log response depend on t_{int}.
- Spectral response (responsivity): the response of the sensor vs incident light wavelength.

4.1. Influence of technological and operation conditions

4.1.1. Transistor body factor

The transistor Body Factor (BF) is what determines the conversion gain of the sensor. Conversion gain is a figure of merit that quantifies the output variation for one collected charge as explained in Chapter 1. In our case, the output is the LIVS, therefore the change in V_{GP} is multiplied by the BF, and the conversion gain can be expressed as follows:

$$Conversion\ gain = BF * \frac{q}{C_{eq}} \tag{4-1}$$

This equation highlights the dependence of the conversion gain on the well charge capacity. The larger the capacitance, the more charges are stored, but at the expense of lower conversion gain. If we consider the BF value for a standard thick gate oxide (GO2) in 28nm FDSOI technology (BF~135mV/V), and C_{eq} for a PiN junction of 2µm² area and 100nm of intrinsic region thickness (T_i), the conversion gain for the FDPix is in the orders of ~5.5 µV/e^- (equivalent to 40 µV/e in a standard sensor where the BF is not taking into account). This value can be increased by either increasing the BF or decreasing the junction capacitance. For example, using a buried oxide thickness (T_{BOX}) of 15nm (BF=213mV/V) and a T_i of 400nm, the conversion gain is increased to ~20µV/e^-. Decreasing the area of the junction considered here will directly impact the CG as well. As previously mentioned in Chapter 1, the CG depends on noise, specially photon shot noise, therefore this calculation is just to highlight the dependences on the different process parameters.

Therefore, the BF is what determines the conversion gain which then determines the slope of the LIVS vs Popt curve. Also, we mentioned before that the slope is what quantifies the sensitivity of the FDPix. Figure 4-1.a. shows TCAD simulation results for a logarithmic response FDPix when varying the gate oxide thickness (T_{OX}) and T_{BOX}. It is clear from this figure that the higher the BF, the higher is the conversion gain and thus, the sensitivity (steeper slope). For example, the LIVS at Popt=0.1W/cm² for GO2 with 15nm of T_{BOX} is increased by a factor of 2.5 compared to the thin gate oxide (GO1) with 25nm T_{BOX}.

In transient regime, where the sensor has a linear-log response as explained in the previous chapter, the variation of the BF will also increase the conversion gain in both regimes. This is shown in Figure 4-1.b. where SPICE simulation results for an FDPix with different T_{BOX} and using an integration time (t_{int}) of 20ms are shown. As we can notice, the transition intensity from linear to logarithmic changes slightly with the BF, this is due to the dependence of V_{RST} on the capacitance of the BOX as expressed in equation (3-16) and (3-17).

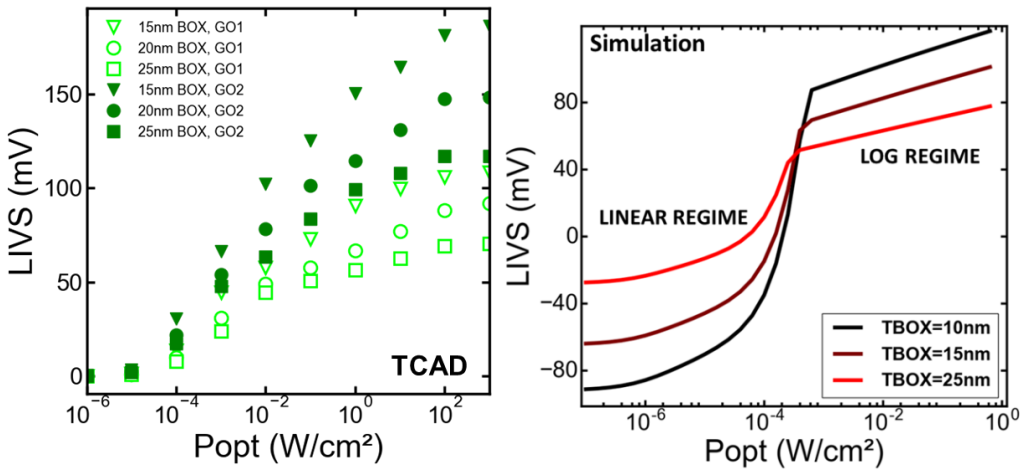


Figure 4-1:a) LIVS vs Popt for N-type FDPix with different T_{BOX} and EOT b) transient response using 20ms integration time, varying T_{BOX}

Thus, a higher BF is better; however, there are some drawbacks to increasing the BF, which are:

- The minimum dimensions of the transistor increase. For example, the minimum gate length L_G of a GO1 device is 30nm while for a GO2 is 150nm (28nm node).
- The reduction of T_{BOX} is limited. Thicknesses <10nm results in quantum effects such as tunneling and the main function of isolation of the BOX is bypassed. Also, the parasitic capacitances mentioned in Chapter 3 become important and the performance of the transistor deteriorate. Finally, process-wise, using a thin BOX complexify the processing of the STI and silicidation of S/D.
- The subthreshold swing (SS) depends on the capacitances as presented in equation (2-48) in Chapter 2. Hence, increasing the BF will result in a degraded SS. This has a direct impact on the operation range of the FDPix.

As previously investigated in Chapter 3, increasing the transistor dimensions (L_G and T_{BOX}) have negligible effect on the sensor response time (τ_{rise}). Therefore, increasing the BF does not affect the light detection performance, speed wise. The overall DR, which is defined as the sum of the linear region DR_{lin} and the logarithmic region DR_{log}, is not impacted by the BF variation. Table 4-1 below summarizes the SPICE simulation results of conversion gain, sensitivity and DR for different T_{BOX} thickness, i.e. different BFs. Since the saturation of the sensor is not reached in characterization and SPICE, the DR values presented in Table 4-1 are underestimated. The TCAD simulation shown in Figure 4-1.a. resulted in 7 decades of light variation before saturation, which corresponds to a DR of 140dB. However, the minimum detectable LIVS which determines the lower limit of the DR, will ultimately depend on the noise floor which is not considered here.

Table 4-1: sensitivity and DR for different T_{BOX} with a T_{OX} of 3.7nm, T_{Si} of 7nm, Ti of 100nm, and t_{int} of 20ms

		Conversion gain (µV/e⁻)	Sensitivity		DR		
			Lin (mV/lux.s)	Log (mV/dec)	Lin (dB)	Log (dB)	Total (dB)
T_{BOX} (nm)	25	5.48	1.7	8.12	48	67	115
	15	7.93	2.05	10.5	52	65	117
	10	10.18	2.33	11.62	55.5	61	116

4.1.1 Junction parameters

The junction depletion region is of main interest here, which is approximately the intrinsic region thickness (Ti) for PiN photodiodes. It is what determines the junction capacitance and its RC product. Therefore, most of the FDPix properties depend on the junction parameters. The response time depends on the RC, the conversion gain and the saturation level depend on the capacitance. Finally, the leakage of the junction will affect the steady state level in DC, and the overall sensitivity of the device.

As introduced in Chapter 1, the Full Well Capacity (FWC) can be calculated by integrating the junction capacitance from initial potential, to the saturation potential (V_{OCsat}) which corresponds to approximately the built-in potential (ϕ_{bi}) defined in equation (2-21) in Chapter 2. Depending on the region of operation, the FWC will differ as shown in Figure 4-2, where the band diagram of a NP junction is illustrated considering different modes of operation.

The initial GP potential V_{GP} will be either:

- Zero in photovoltaic mode where the junction is at equilibrium, as illustrated in Figure 4-2.a.
- V_{RST} in integration mode, as shown in Figure 4-2.b. and c.

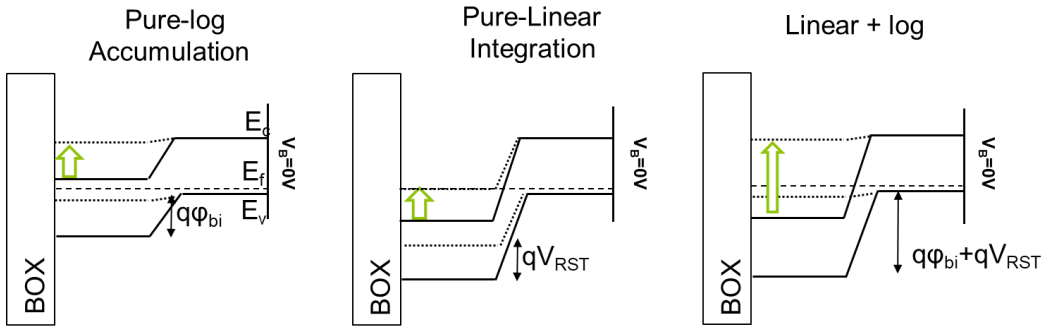


Figure 4-2: schematic of band diagram evolution of the FDPix NP junction in different regime, a) accumulation, b) integration, c) both

Thus, the FWC can be expressed for logarithmic mode pixels as:

$$FWC_{log} = \frac{1}{q} * \int_0^{Vocsat} C_j(V)dV \tag{4-2}$$

And for integration mode as:

$$FWC_{lin} = \frac{1}{q} * \int_{V_{RST}}^{0} C_j(V)dV \quad (4\text{-}3)$$

Since the type of charges in both regimes are different (integration vs photovoltaic) the FWC is considered separately for each region. The total FWC for lin-log operation is the sum of the two contributions as:

$$FWC_{lin-\log} = FWC_{log} + FWC_{lin} \quad (4\text{-}4)$$

A large FWC is desirable to increase DR_{lin}, as more charges can be integrated and accumulated, however, it is at the expense of lower sensitivity at low light intensities due to a lower conversion gain, as explained in the previous section.

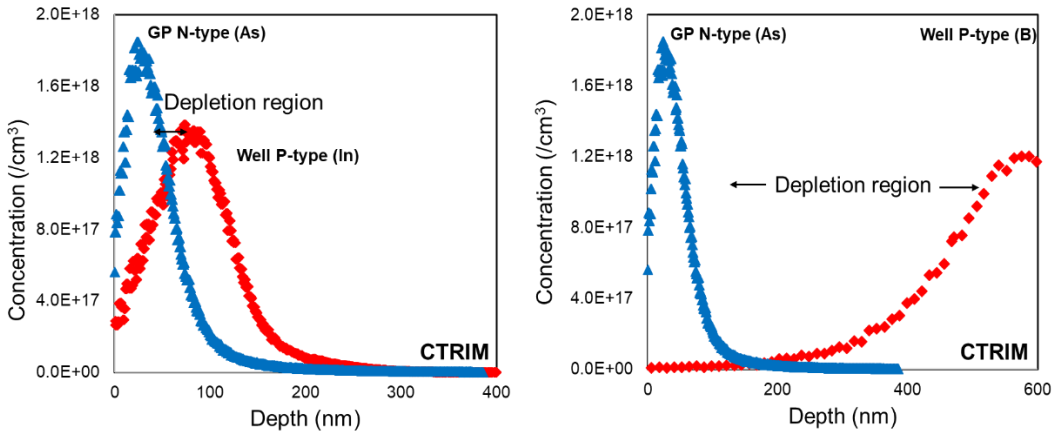
To calculate at which power density the sensor saturates ($Popt_{sat}$), we calculate the number of photons corresponding to FWC_{log} using the Quantum Efficiency (QE), and multiply it by its energy. Therefore, it can be estimated as shown below:

$$Popt_{sat} = \frac{FWC_{log}}{QE} * \frac{h\upsilon}{area} \quad (4\text{-}5)$$

At this power density, V_{OC} will reach ϕ_{bi} and the $LIVS_{SS\_sat}$ is obtained, as described in equation (2-44) in Chapter 2. The dynamic range upper limit is defined by $Popt_{sat}$, and the lower limit depends on the noise level which determines the minimum detectable light intensity. The study of noise was not performed during this work.

4.1.1.1 Doping profile

The junction implantation profile is a major parameter to be well defined in the process. It determines the junction capacitance and resistance but also the photon collection volume. Multiple splits were implemented. Using CTRIM simulations, we can generate doping profiles for different implantation species, doses, energy, angle etc. The obtained profiles are then modeled in TCAD by Gaussian distributions and are used to define split tables for fabrication. We used Boron and Indium as acceptors (p-type), and Arsenic and Phosphorus as donors (n-type). The doses and energy used resulted in either narrow (Figure 4-3.a), regular (chapter 2, Figure 2-22), or wide (Figure 4-3.b) junction. Figure 4-3 shows example of the obtained NP junction with the corresponding doses and energies, where the x=0 corresponds to the BOX/GP interface.



Designed Junction	Materials		Dose (cm^{-2})		Energy (keV)	
	N-type	P-type	N-type	P-type	N-type	P-type
Narrow	As	B	1.2e13	1.5e13	110	30
Regular	As	B	1.2e13	3.2e13	110	120
Wide	As	B	1.2e13	3.2e13	110	180

Figure 4-3: doping concentration distribution for different implanted junctions starting at the BOX/GP interface (x=0)

The quasi-neutral regions will deplete depending on their respective concentration. The GP doping concentration should be high enough to minimize BOX/GP depletion which would negatively affect the BF, and also to avoid full depletion, which may lead to the overlap between the junction depletion region and the BOX/GP depletion.

In TCAD simulation, a PiN junction with uniform doping concentration is used to study the effect of increasing the depletion region on both DC and transient. The N-type GP region thickness is 150nm, the total substrate thickness is 3µm, and the intrinsic region width Ti is varied. BSI illumination is used in the simulations, and both N and P regions are doped with a concentration of $1e18cm^{-3}$. Larger depletion region results in higher carrier collection efficiency and thus increases the drift component of the photocurrent for a given light intensity (equation 2.35). However, increasing the intrinsic region increases the reverse saturation current of the diode on which V_{OC} is inversely proportional, thus lowering the LIVS in logarithmic mode. This is shown in Figure 4-4.a, where the LIVS in DC is plotted vs P_{opt}. We can see that increasing the intrinsic region width reduces the LIVS for a given intensity. However, in transient where the charges are integrated, using a thicker T_i results in a faster response since the RC product is reduced as was demonstrated in Chapter 3. This is shown in Figure 4-4.b. where the LIVS extracted from transient response using 10ms integration time is plotted vs Popt. We can see that the linear region response increases for higher T_i values, while the log response is degraded.

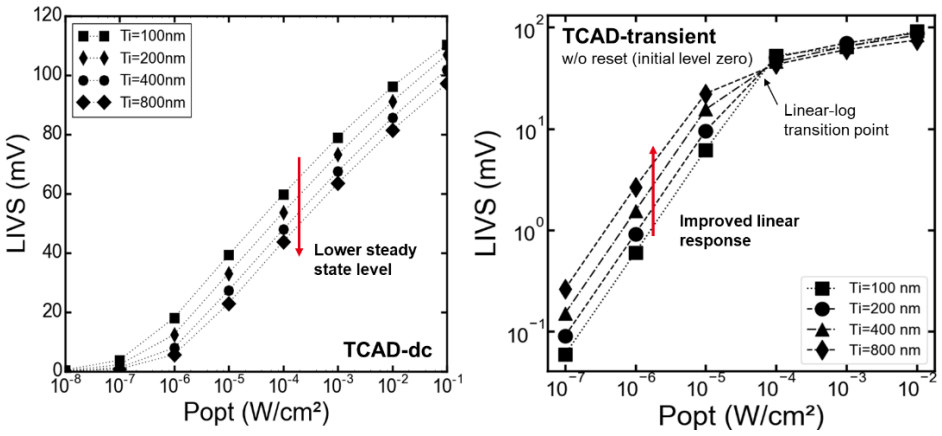


Figure 4-4: the effect of varying the intrinsic region thickness on a) LIVS in linear scale vs P_{opt} in DC b) LIVS in log scale vs P_{opt} in transient using a 10ms integration time

In conclusion, using a thicker intrinsic region increases the linear region sensitivity but reduces the logarithmic region steady state level. For high-speed application, the PiN junction with thick *i* region is preferable.

The conversion gain and FWC are calculated using equations (4-1)-(4.4). By considering the C_j for different T_i showed in Figure 3.6 in Chapter 3, a V_{RST} of 1V and V_{OCsat} of 0.6V, the results are presented in the Table 4-2.

Table 4-2:Conversion gain and FWC for different operation mode pixels while varying the junction capacitance. The device is standard GO2 with T_{BOX}, T_{OX}, and T_{Si} being equal to 25, 3.7, and 7nm respectively

Ti (nm)	**Conversion Gain (µV/e-)**	**FWC_{lin} (#e⁻)**	**FWC_{log} (#e⁻)**	**$FWC_{lin-log}$ (#e⁻)**
100	5.28	9168	7234	16402
200	7.89	6173	4381	10554
400	12.3	5444	2593	8037

Regarding process integration, some specifications must be mentioned. All the junctions fabricated were using ion implantation as previously mentioned, which limits the intrinsic region width range. For example, the deepest implantation available in the standard process is the Deep NWell (DNW), which is used to isolate the transistors from each other. The peak of its doping concentration is located at around 800nm below the BOX which would allow us to obtain an intrinsic region width of ~700nm. Also, the STI must be considered here. The depth of the STI in standard 28nm process is 280nm, meaning that if the intrinsic region is thicker, we need deeper trench to isolate the pixels. Thus, to obtain these junction different solutions are possible:

- Using ion implantation as previously mentioned, although limited in depth. The deeper the implant the more energy and dose you need which should be carefully controlled to avoid residual dopant in the channel of the transistor.

- Using epitaxy. This will be further discussed in section 4.2.2.2.a. The idea is that we can process the photodiode on a separate wafer and bond the wafer to the FDSOI BOX interface, which would allow the definition of the diode using epitaxy or other methods.

4.1.1.2 Junction leakage

The sensitivity, steady state level and speed of the sensor are highly related to the leakage current of the junction, also called dark current in image sensors. Leakage current is due to carrier recombination; thus, it depends on the carrier lifetime in the material, which is inversely proportional to the recombination rate. The recombination process considered in our case, where silicon doped to ~$10^{18}cm^{-3}$ is used, is the SHR recombination. This process is due to the presence of traps, i.e. recombination sites in the band gap of the material whose density increases with the doping concentration or by implanting defects.

In the following two sections, we discuss the leakage current and its impact on the device performance, based on defect concentration and operation temperature.

4.1.1.1.a. Defect concentration

We studied the effect of adding defects to the junction and its impact on the LIVS. On one of the splits with the regular implantation profile, we implanted carbon atoms with the profile shown in Figure 4-5. The carbon atoms across the junction will act as recombination sites that increase the leakage current of the junction. In other words, the path created with the carbon atoms lowers the junction shunt resistance.

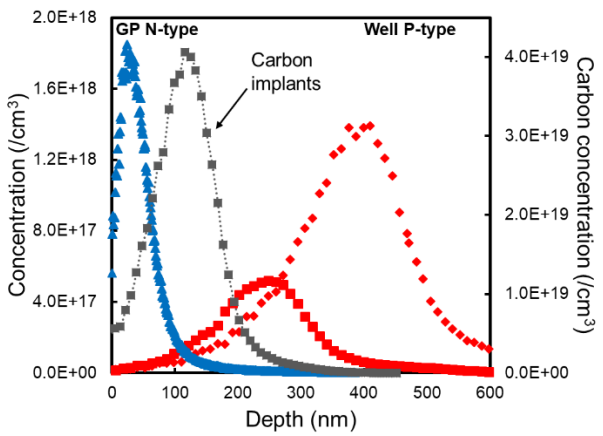


Figure 4-5: implantation profile starting from BOX/substrate interface (x=0) showing the GP, Well, and defects (carbon) implants

The FDPix with carbon atoms are characterized and compared to the regular junction. The DC test results are shown in Figure 4-6.a. where the LIVS value for GO1 and GO2 devices are plotted. As expected, the leaky junction results in almost canceling the LIVS for the GO1 device and reduces it by half for a GO2 one. Regarding transient response, the leaky junction will have much faster response and return to equilibrium time since the carriers' lifetime and RC product are reduced. This is shown in Figure 4-6.b. where the drain current is monitored when the light is turned off, for the standard junction and the carbon implanted one.

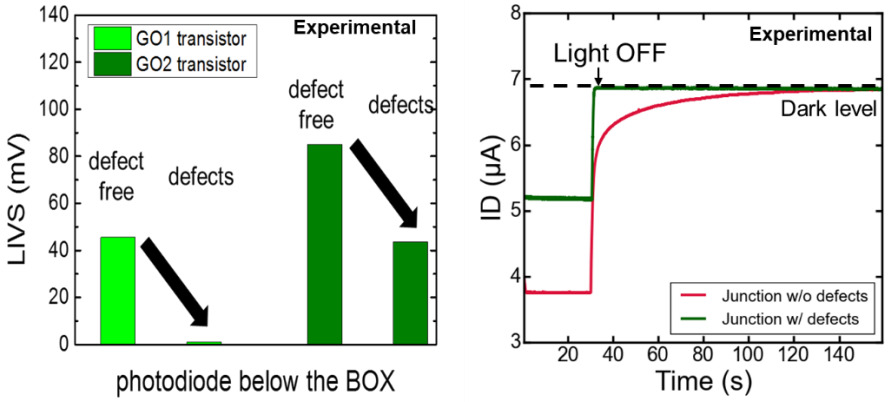


Figure 4-6: a) Drain current transient for an N-type FDPix where defects have been implanted in the junction, b) the impact of these defects on the LIVS dc

Implementing defects to increase the junction speed is a technique used for high speed receiver diodes , or for micro resonators to enhance the detection at certain wavelengths *[ACKERT 2011]*, however, for image sensors or light detectors where every photon counts, the junction quality must be as high as possible by perfectly controlling the process.

4.1.1.1.b. Temperature stability

As discussed in Chapter 1, the impact of temperature on image sensors is thoroughly studied and optimized but is still one of the major problems encountered in today's image sensors *[CHOUBEY 2008]*. The main problem is caused by the leakage current, i.e. dark current (I_{dark}), that doubles every 7-8°C increase in temperature. This is due to the bandgap reduction with temperature which in turn increases the n_i term in equation (2-29) and (2-30). The LIVS of the FDPix dependence on temperature follows the same trend as standard image sensor since we are also using a p-n silicon junction as photosensitive element. In Chapter 3, from the experimental data shown in Figure 3-1, we estimated the dark current of the regular junction profile at room temperature (fixed SS, BF and C_{J0}) to be equal to ~5e-18A/µm² (0.5nA/cm^2) which would corresponds to ~130 e/s for a diode area of 4µm². We performed steady state measurements on the regular junction FDPix device at different temperatures. Two effects are important for the FDPix sensor, the impact of temperature on the SS of the transistor that determines the conversion of the I_D variations to LIVS, and on the LIVS, both being presented in Figure 4-7. The SS has a direct dependence on T as was described by equation (2-47). The measured SS shown in Figure 4-7.a, are in accordance with (2-47), where an increase of 25°C increases SS by a factor of 1.08. The dependence of LIVS on temperature comes from the dependence of V_{OC} on the dark current, it can be described by the following equation:

$$\frac{dLIVS}{dT} = BF * \frac{dV_{OC}}{dT} \tag{4-6}$$

The dV_{OC}/dT is about -2.2mV/°C for silicon photodiode *[LÖPER 2012]*, which results in a dLIVS/dT for a GO2 device of ~0.286mV/°C. It is in accordance with the measured data of an N-type FDPix with NP oriented junction, shown in Figure 4-7.b, the results represent the mean of extracted LIVS at steady state ($LIVS_{SS}$) on 25 samples. We can see that for a 25°C increase in temperature, the $LIVS_{SS}$ decrease is ~7.5mV, which is close to the modeled 7.2mV (0.286*25).

This is also true for the 348K to 375K increase. However, from 323K to 348K, we can notice a more abrupt change in LIVS of about 27mV, this is still unexplained since the V_{OC} variation are approximately linear with the temperature *[LÖPER 2012]*. Possible parasitic element on the wafer could probably be the cause for this discrepancy.

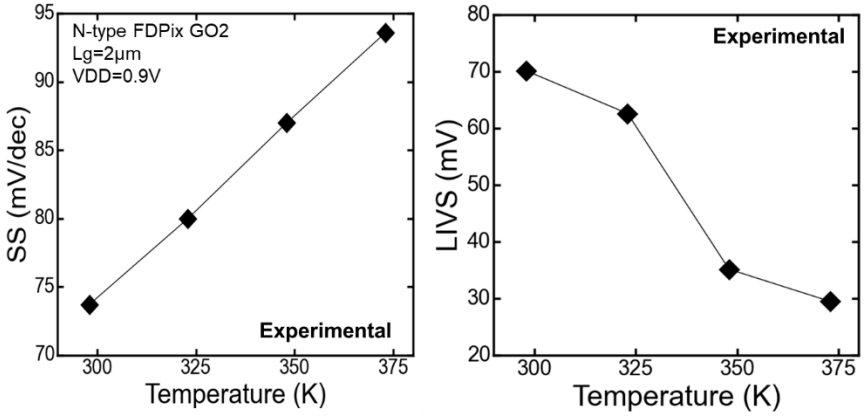


Figure 4-7: effect of temperature on a) subthreshold swing b) LIVS

In conclusion, the increase in temperature will affect both regions of operation of the sensor. As demonstrated, it will decrease the saturation level in logarithmic region. Also, increasing the temperature will result in a loss of contrast between pixels since they will saturate at lower intensities. This is one of the main drawbacks of logarithmic pixels. It can be corrected by adding an antiblooming drain, as proposed in *[NI 2018]* which will generated a positive offset in the linear regime easily corrected in postprocessing. Finally, the increase in temperature reduces the overall SNR of the sensor, since it increases the dark current noise, which is dominant at low light intensity and determines the DR lower limit. We discussed in Chapter 1 some process optimization technique to minimize it, such as using a pinned photodiode. Some post processing techniques can also be implemented. For example, to account for the dark current increase, a temperature sensor or a dark pixel is often integrated with the array to measure the variation and perform post processing correction on the measured signal. Another way is to subtract a dark frame from the following frames, which takes into account the dark signal dependence on integration time and gain; however, it doesn't consider the temperature increase.

4.1.2 Impact of operation conditions on FDPix performance

The two main parameters to dynamically tune the DR of the two regimes are discussed and their effect is demonstrated.

4.1.1.2. Reset pulse amplitude

The reset pulse amplitude (V_B) is what will determine V_{RST} according to the equation (3-23) developed in Chapter 3, where we studied it effect on history effect and lag. The initial potential has an impact on the FWC_{lin} and thus on DR_{lin}. Increasing V_{RST} will extend the range of operation in linear, i.e. will lead to higher DR_{lin}, and the transition point from linear to log shifts to higher Popt values for a given t_{int}. Therefore, if the linear range is to be privileged, a high reset pulse should be used. The FWC of the linear and log regions are estimated using SPICE for different V_{RST} values

considering an FDPix with PiN junction where T_i is 100nm. The results are summarized in Table 4-3 below for a standard GO2 with T_{BOX}, T_{OX}, and T_{Si} equal to 25, 3.7, and 7nm respectively.

Table 4-3:FWC of standard GO2 FDPix for different operation mode pixels while varying the V_{RST}

V_{RST}(V)	FWC_{lin}(#e⁻)	FWC_{log}(#e⁻)	$FWC_{lin-log}$ (#e⁻)
0.5	4645	7234	11879
1	9168	7234	16402
2	16948	7234	24182

As expected, the higher the V_{RST} the higher the FWC_{lin} which increases the DR_{lin}. The FWC_{log} is constant for all V_{RST} since it depends on junction profile and doping (i.e. V_{OCsat}), and since the C_J doesn't vary much with reverse bias, the conversion gain is also approximately constant.

4.1.1.3. Integration time

The integration time will determine at what optical power does the sensor change operation from linear to logarithmic. The longer the t_{int} the more time is available for the sensor to reach steady state. Also, more charges are integrated for the same light intensity resulting in higher sensitivity when measured in mV/lux. This is demonstrated in Figure 4-8 where the LIVS is plotted vs P_{opt} for different t_{int}, as obtained using SPICE simulations. As expected, the slope of the linear regime increases with t_{int}, and the transition point shifts to lower light intensities since the sensor will reach FWC_{lin}. Which means that longer integration time reduces the DR_{lin}. As seen in equation (3-27) in Chapter 3, the sensitivity in linear regime is proportional to the integration time, meaning that there is a factor of two between the slope of t_{int}=20ms and t_{int}=10ms as shown in Table 4-4. Thus, the integration time is a variable that allows the tuning of the sensor response. Usually, t_{int} is adapted to the scene intensity. For low light intensity scenes, it is longer to increase the number of integrated charges and thus output variation.

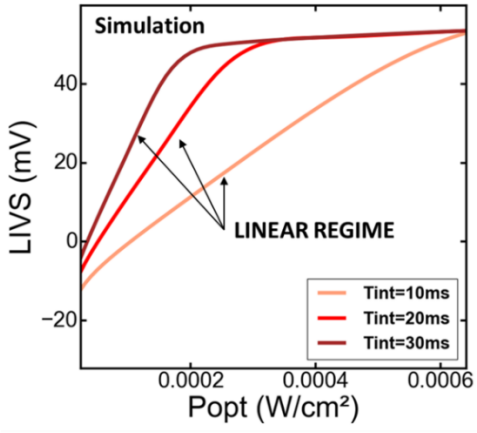


Figure 4-8: regions of operation tuning by changing the integration time

The linear response results in higher sensitivity at low light, as was discussed in Chapter 1 in the linear-log sensors section. The transition and respective DR of these two operating regions can be tuned using t_{int} and V_{RST}. Ultimately, the selection of these two parameters is application dependent. The following table summarizes the simulation results with the sensitivity in linear (in µV/lux) and logarithmic for different t_{int} values for standard GO2 FDPix.

Table 4-4: sensitivity and DR value for different t_{int} for the standard GO2 FDPix

		Sensitivity		**DR**		
		Lin (mV/lux)	**Log (mV/dec)**	**Lin (dB)**	**Log (dB)**	**Total (dB)**
t_{int} (ms)	10	16.6	8.12	55	65	120
	20	33.2	8.12	48	72	120
	30	49.8	8.12	44	76	120

4.2. Light detection optimization

In this section, we will study the photonics aspects of the FDPix sensor. Its responsivity and the Quantum Efficiency (QE) are evaluated, and we present integration schemes to improve the FF and the photon collection efficiency. Finally, we propose a perspective of using different materials as photosensitive elements, which will result in using the FDPix for different spectrum sensing.

4.2.1. FDPix spectral response

The photosensitive element, i.e. the photodiode, implemented in the FDPix is a standard silicon junction. The silicon bandgap is around 1.12eV, which means that it absorbs photon in the visible range and Near Infra-Red (NIR). The range of absorbed wavelengths is approximately 400-1100nm. Figure 4-9 shows the FDPix spectral response obtained experimentally using a monochromator (more details on the setup can be found in appendix B). the DUT is an N-type FDPix with NP oriented junction. We can see that the sensor LIVS reproduces the Xenon source power spectrum accurately (that was measured using a silicon photodiode) in the range of wavelengths previously mentioned. This indicates that the system is linear, and that the devices response accurately to the optical power.

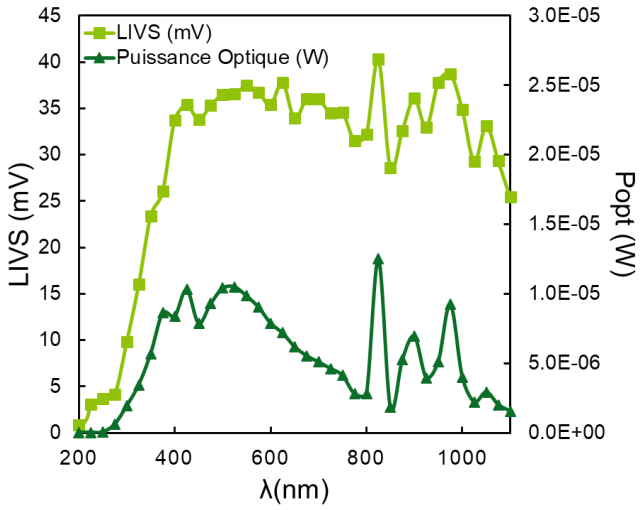


Figure 4-9: FDPix spectral response and the applied optical power

The responsivity is defined as the ratio between output signal and input optical power. It is wavelength dependent and is measured in A/W. In our case, the responsivity can be defined as:

$$R(\lambda) = \frac{\Delta I_D(\lambda)}{P_{opt}(\lambda)} \tag{4.8}$$

Where ΔI_D is the change in drain current with light. From R(λ), the quantum efficiency (QE) can be calculated as follows:

$$QE(\lambda) = R(\lambda) * \left(\frac{hc}{q\lambda}\right) \tag{4.9}$$

Where *h* is the Plank constant, *c* is the speed of light, *q* the elementary charge and λ the wavelength. The R and QE depend on how efficiently the photon reach the photodiode, are absorbed, and converted to electrons. Thus, in all image sensors, an antireflection coating (ARC) is used to minimize the surface reflection, and the surface is passivated to minimize surface recombination. Also, the junction should be carefully designed by considering the doping concentration on each side, the material used and their respective band gap, and the location of the depletion region from the surface of the sensor, since the absorption coefficient and absorption depth are wavelength dependent. As can be seen in Figure 4-10, the absorption coefficient is very high at low wavelength, but the absorption depth is very low, meaning that the photons are absorbed in the first few nanometers. For example, a silicon junction located near the surface will optimize the QE in the blue region of the spectrum (short wavelength) while decreasing the QE in the red part of it (long wavelength). That's why surface passivation is very important to reduce surface recombination.

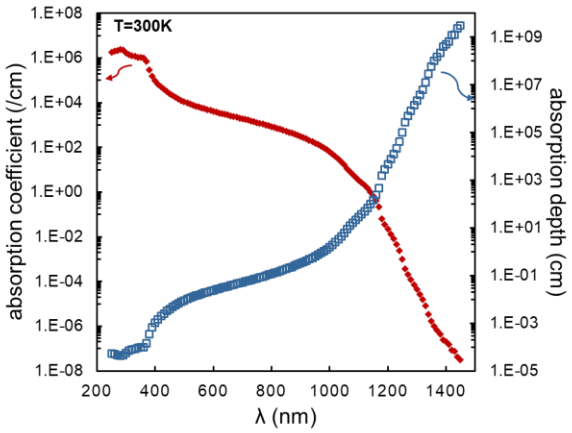


Figure 4-10: Silicon absorption coefficient and absorption depth [GREEN 1995]

Another metric that is highly design or layout dependent is the Fill Factor (FF) of the device. Using FSI, the sensor is shadowed by the BEOL non-optimized for image sensing applications, S/D silicidation, and transistor gate. If a specific process would be used, the S/D will be partially unsilicided, the BEOL optimized to avoid covering the device, and ARC and microlenses would be implemented, as it is the case for standard image sensors. However, the gate stack shadowing cannot be avoided, and the photosensitive part is inevitably underneath it.

The transmittance of the gate stack is characterized. The gate stack of standard 28nm FDSOI CMOS node is shown in Figure 4-11. The thickness of the oxide varies depending on the type of gate oxide thickness. Since we mainly characterized GO2, it is set in the simulation at 3.7nm.

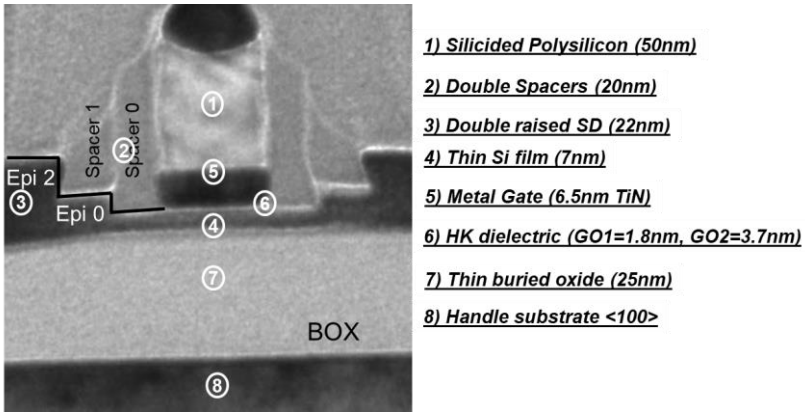


Figure 4-11: Gate stack layers of 28nm FDSOI transistor

Using the DeltaPsi2 Software *[HORIBA]*, the transmittance, or percentage of the incident light reaching the substrate, is calculated considering reflectance and absorption of the different layers but without taking into account the silicidation. The results are shown in Figure 4-12. As we can see, the gate effectively blocks the incident optical power since less than 20% transmittance is obtained. The peak observed at around 500nm could be due to the high contrast in refractive index between the different layers forming the stack. Due to this different, multiple reflections occurs at the interfaces which might be responsible for the appearance of modes in the transmission *[ATEF 2014]*. We can

conclude that most of the visible spectrum is blocked by the gate, which reduces the FF and thus the sensitivity of the device.

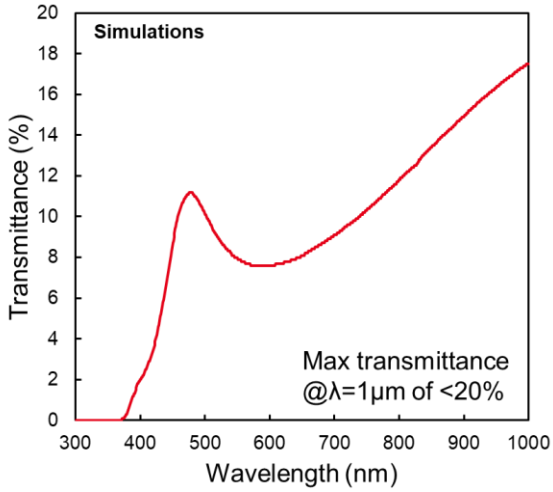


Figure 4-12: transmittance curve for the gate stack of the FDPix sensor without considering the Silicidation

Since the gate is what primarily shadows the structure, the best way to go around it is using Back Side Illumination (BSI). This is discussed in the following section.

4.2.2. Back side illumination (BSI)

As introduced in Chapter 1, the BSI integration consist in flipping the sensor so that the light will be incident directly on the photodiode without going through the BEOL of the pixel. When FSI is used, the optical path will include the total thickness of the BEOL. The reflection on the metal lines induced losses and crosstalk between pixels. A comparison between FSI and BSI sensors is shown in Figure 4-13 below.

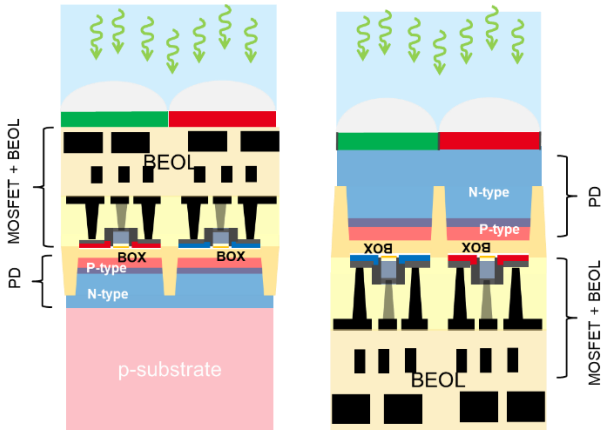


Figure 4-13: comparison between FSI and BSI FDPix structure

In the case of the FDPix, the advantage of the sensing transistor being on top of the photosensitive element renders this structure optimized for BSI. In the two following sections, TCAD simulations comparing FSI to BSI responses are presented, and different integration are proposed and discussed.

4.2.2.1. TCAD simulation

Two identical N-type FDPix NP oriented GO2 structures are compared, one illuminated from the top with a 100µm substrate, the other one is the BSI structure, where the light is coming from the bottom and the substrate is thinned down to 3µm distance from the BOX as shown in Figure 4-14. 3-5µm of Si are necessary to maximize the absorption of the spectrum. The results are shown in Figure 4-14 where the LIVS vs Popt are plotted for FSI and BSI. We can see that using BSI, the steady state response is improved for a given intensity, which is seen as a one decade shift towards lower light intensity.

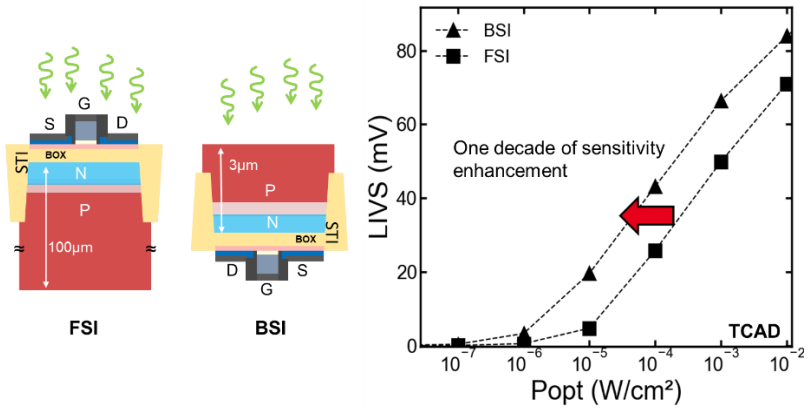


Figure 4-14: LIVS vs Popt comparing FSI and BSI

4.2.2.2. Process flow

The main challenge in BSI integration is the thinning down of the ~775µm wafer to about 3-5µm while insuring a surface roughness as low as possible (<50A). Surface roughness generates recombination sites which decreases the blue range sensitivity and increases the dark current *[VEREECKE 2015]*. Therefore, a back thinning using an etch stop layer is necessary to achieve the demanded quality. Two main solutions were proposed *[LAHAV 2014]*, namely using an SOI or a P/P+ wafer. Both these techniques can be implemented for the FDPix BSI. We will first present a process flow using a double SOI, with the second BOX used as a stopping layer. Then, we investigate the use of P/P+ layer solution for backside thinning.

4.2.2.2.a. BSI integration using double BOX structure

This first approach is close to the standard BSI SOI process *[CAVACO 2015][EDELSTEIN 2011][PAIN 2005][PAIN 2009]*, where the pixel is processed on an SOI, then transferred to a handle wafer and back thinning in performed. The BOX is used as an etch-stop layer due to the high Si-SiO2 selectivity and protects the Si active layer surface during backside thinning, which is the main advantage of this technique. The integration of the second BOX process is depicted in Figure 4-15. Two solutions are possible:

- Using two SOI wafers, where wafer A is bonded to a handle wafer and thinned down to the BOX, then wafer B, where the silicon film represents the total photodiode thickness (3-5µm), is bonded to the BOX of wafer A. After that the handle wafer is removed, the STI are processed, and the process flow continues.

- Using a sequential approach which starts with one SOI wafer similar to the wafer B in the previous solution. The photodiode is either implanted or deposited, and a thermal silicon dioxide is created to form the BOX of the FDPix. After the oxide, poly silicon is deposited which will form the channel of the transistor. Finally, the STI are processed and the process flow continues. The advantages of this approach are the reduction in cost since no additional SOI wafer is necessary. The drawback is the poly-silicon channel that will degrade the transistor performance and increase variability and mismatch as oppose to the crystalline channel.

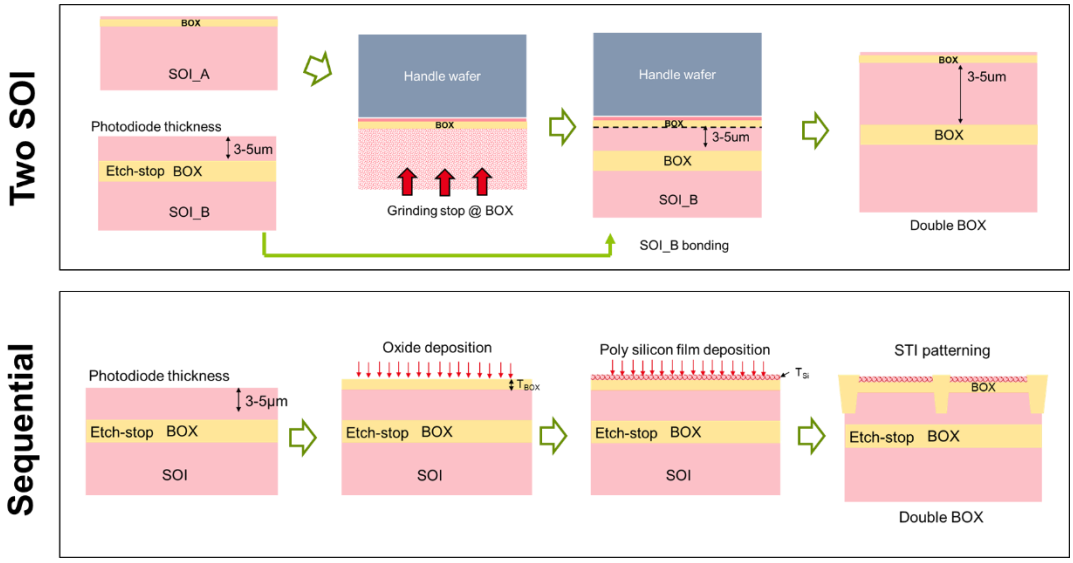


Figure 4-15: Double BOX integration for BSI FDPix

The advantage of this technique resides in processing the photodiode separately. Meaning that the photodiode can be grown using epitaxy or deposition technique in addition to the standard ion implantation used previously. Therefore, we can also consider other materials than silicon.

The rest of the integration is equivalent to the standard BSI integration using SOI wafer. Starting with the double BOX wafer, the BSI FDPix process is depicted in Figure 4-16. The Front End of Line (FEOL) including Photodiode implantation and FDSOI transistor process is performed, followed by the BEOL. After that, the front surface is bonded to a handle wafer to perform back side thinning, that will stop at the first BOX. After that the BOX is removed using the Si as etch-stop. The next steps are standard to image sensors: surface passivation, ARC deposition, color filter arrays and µlenses. To perform these last steps, some alignment marks must be readable from the backside. The wafer is then transferred on a rigid transparent glass wafer and the handle on the front side is removed. Finally, the electrical pads are contacted on the back side using Through Silicon Vias (TSVs).

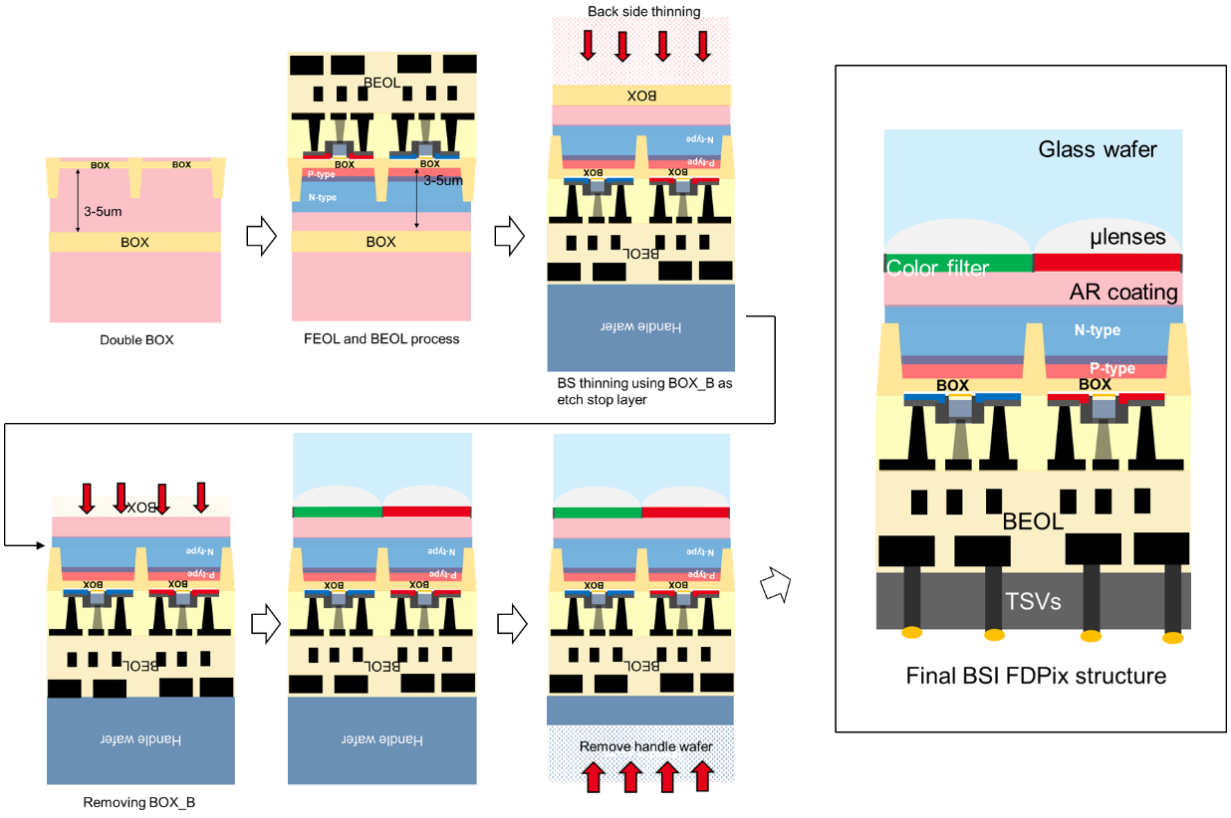


Figure 4-16: FDPix BSI integration

Another advantage of using the double BOX integration is that it simplifies Deep Trench Isolation (DTI) patterning since the second BOX provides an etch stop layer. And to go a step further, a possible integration which would allow the access to the GP of the device via an electrical connection, is using a dual-STI approach *[GRENOUILLET 2012]*. It consists in using DTI to isolate the transistors from each other, and STI to allow the biasing of the GP as shown in Figure 4-17. We previously mentioned that we investigated the option of contacting the GP to add a reset transistor, which resulted in a 2T FDPix, and the results are presented in Appendix C. The dual-STI scheme is a solution that can be used to obtain the 2T pixel.

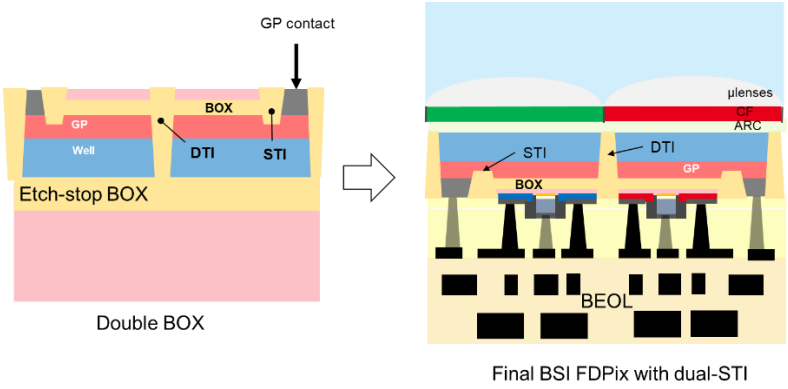


Figure 4-17: example of FDPix integration using dual-STI approach for GP contacting

The BSI SOI is the simplest and most efficient technique, with which high surface quality and low surface roughness are obtained. The main drawback of this technique is the cost of using SOI wafers, that led the industries to develop alternatives.

4.2.2.2.b. BSI integration using P/P+ wafer structure

In this case, instead of bonding an SOI as wafer B, a P/P+ wafer is bonded. The back thinning in this case is much more complexed since there is no etch-stop layer. It is based on the dependence of etch rate on the dopant concentration *[HUSTER 1993]*, and since P/P+ have almost three decades of difference in concentration, it reasonably allows a control of the back thinning. After that the FEOL and BEOL process are performed, and the wafer is bonded to a handle wafer for back thinning. The first step is to thin down to approximately 20µm from the BOX interface, then the special CMP step to stop at the P/P+ interface and obtain the required roughness, is performed *[G WUU 2019][RHODES 2009][WUU 2009]*. After the thinning the flow is identical to the one previously presented.

The main advantage of using this technique is to avoid using another SOI wafer and the cost that comes with it. However, the processing of the FEOL requires a high temperature budget with annealing and dopant activation steps. This will result in dopant diffusion at the P/P+ junction, and thus the loss of a sharp stopping interface *[LAHAV 2014]*. Also, the surface roughness obtained is not enough and a dedicated CMP step has to be performed after the thinning.

4.2.2.2.c. BSI process of FDPix without etch stop layer

All the process steps described hereafter were performed in LETI's clean room. Since the wafers studied are fully processed 300mm wafers in 28nm FDSOI technology, there is no etch-stop layer integrated for back side thinning. Therefore, the first solution we explored is to thin down without having a specific etch-stop layer. The process is summarized in Figure 4-18. We used a temporary bonding technique for backside thinning using grinding followed by a dry polishing.

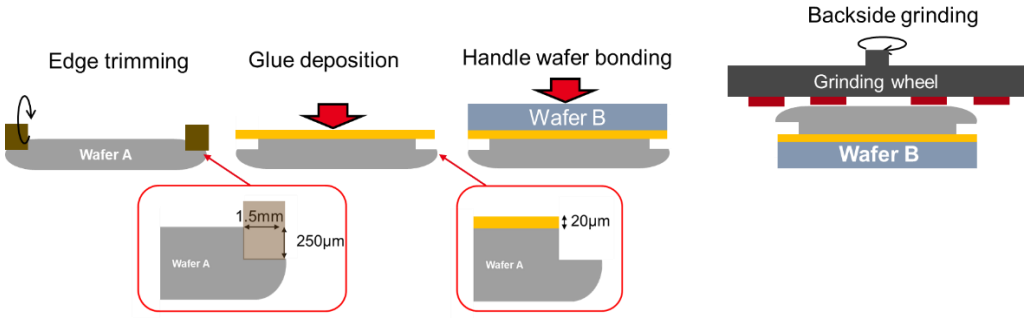


Figure 4-18: Temporary wafer bonding for backside grinding

The first step is to perform edge trimming on the wafer A to avoid edge damage during grinding. The trimming reduces the total radius of the upper part of the wafer by 3mm. After that the temporary adhesive material is deposited. The adhesive layer is 20µm thick. The thinner the glue thickness, the thinner the final obtained thickness with grinding. After that a polymer bonding to wafer B is performed. Post bonding Scanning Acoustic Microscopy (SAM) images are shown in Figure 4-19.a and Figure 4-20.a, where we can see a void free, uniform bonding.

The backside grinding is performed in two steps. First by removing the substrate using a rough grinding, wafer A is thinned down from 775µm to 166µm. After that a fine grinding step targeting 20µm thickness is performed. The first trial resulted in major delamination as can be seen in Figure 4-19.b. This might be due to a high rough grinding speed that generated too much stress in the structure, we should remind here that we are using the 28nm technology, thus the BOX is only 25nm thick, and the temporary glue is not rigid.

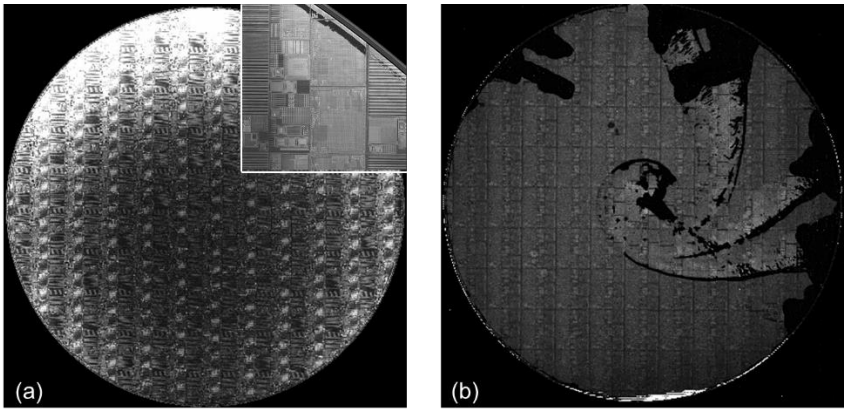


Figure 4-19: back thinning using grinding on FDSOI wafers a) after bonding of handle wafer b) after back thinning (target 150µm)

To avoid this problem, a thermal anneal is performed after the rough grinding to cure the possible generated defects, and the fine grinding speed is reduced. The resulted SAM measurements are shown in Figure 4-20.b for post rough grinding with 166µm thickness, and Figure 4-20.c. for post fine grinding with 20µm thickness. We can see some delamination appearing at the top edge of the wafer.

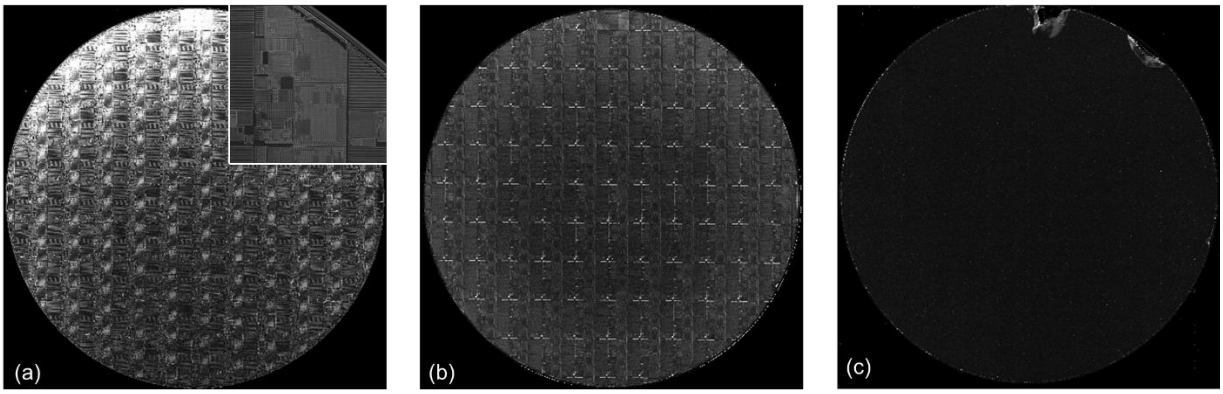


Figure 4-20: acoustic image of thinned down wafer a) after handle wafer bonding b) after rough grinding (target reached 166µm) c) after fine grinding (target reached 20µm)

Lastly the thinned wafer is transferred to a transparent substrate for BSI. Since the wafers went through all technological steps, we couldn't use bonding on glass wafer that requires high temperature. Therefore, we successfully transferred the thinned 300mm diameter and 20µm thickness wafer, to an adhesive transparent dicing tape and frame. The handle wafer B is debonded mechanically, and the glue is removed using a solvent. The final wafer is shown in Figure 4-21, where when illuminated from the back side, we can see the red light from front side which means that

the thickness is low enough to not absorb the red wavelength. For future test, a characterization bench needs to be adapted for BSI illumination and front electrical biasing.

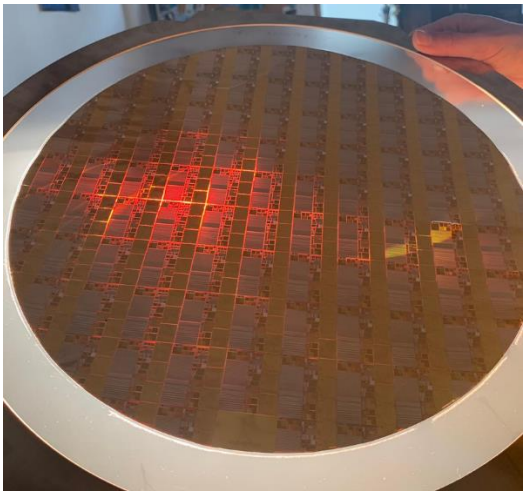


Figure 4-21: thinned 300mm wafer on transparent dicing tape and frame illuminated from the back side

The previous discussion highlighted the complexity in obtaining a BSI integration. The proposed integration using a double BOX structure is the most efficient, however, it does require another SOI wafer which will increase the cost process-wise. The use of a P/P+ integration avoid the use of an SOI; however, this technique is far more complex and requires very high accuracy and controlled process. Therefore, the SOI is still today the technology of choice for many image sensors industries *[LAHAV 2014]*.

4.2.3. U-Shape photodiode implantation profile

Since the FDPix depends on a capacitive coupling that occurs adjacent to the gate, a way to improve the sensitivity at low light would be to drive the collected charges to that area. The idea is to shape the junction so that the E-field that separates the photogenerated charges drives them underneath the gate area. The proposed structure is shown in Figure 4-22. The photodiode is shaped in a U form with an intrinsic region inserted between the N and P region. This *i* region is introduced to enlarge the collection volume as was the case for planar photodiodes. Also, the isolation of the sensing node from the surfaces of the STI might also results in lower leakage.

For the GP (N-type in Figure 4-22) to cover the whole surface of the gate, a tradeoff is made between its concentration and area. If it is the same length as the gate, the depletion will decrease the overlap area at the BOX/GP interface. Therefore, to avoid this loss in area, either the length of the GP is increased to account for the depletion, or its concentration is increased to limit it. Also, this integration is preferable with BSI, otherwise, the photodiode junction is completely covered by the gate which will reduce the efficiency using FSI.

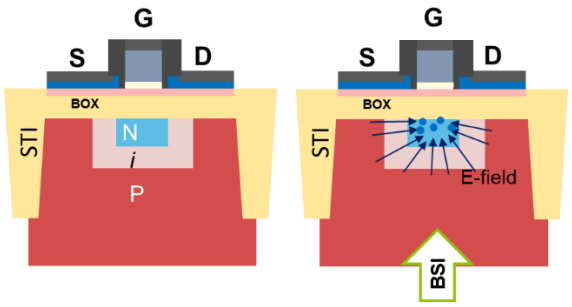


Figure 4-22: FDPix sensor with U-shaped junction

4.2.3.1. TCAD simulation

The structure shown in Figure 4-22 is simulated in TCAD using uniformly doped regions (N_D=1e18cm^{-3}, N_A=1e18cm^{-3}) and is compared to the identical planar case as shown in Figure 4-23. The GP is 150nm thick, the intrinsic region is 100nm, and the substrate is 3µm. In both cases BSI is used. The results are shown below where we can see that for low intensities the LIVS is improved by a factor of ~1.6 at 1 µW/cm² using the U-shaped junction, due to the better photocarriers collection under the gate. Also, a higher LIVS is obtained when using a higher GP concentration due to the optimized overlap with the gate by reducing the depletion, where a factor of 2.6 increase is measured. The same improvement is obtained (not shown here) by keeping the same concentration but extending the GP area beyond the gate length of 150nm for GO2 device by 30nm on each side to account for depletion.

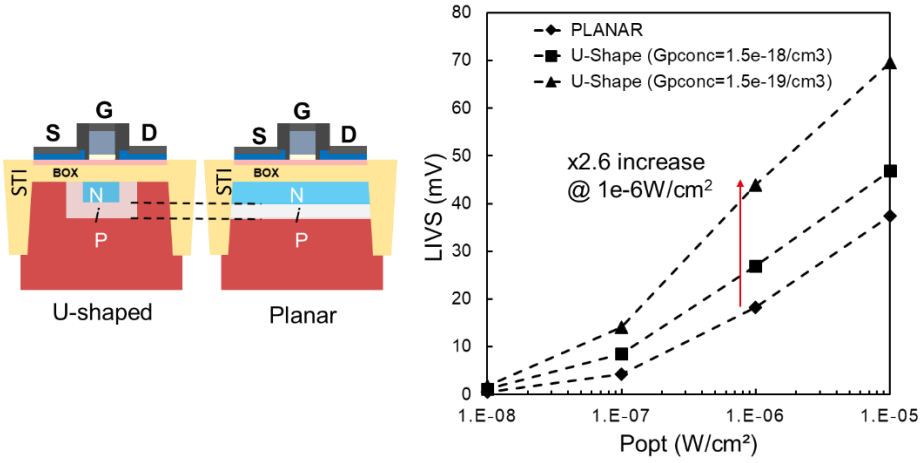


Figure 4-23: TCAD results LIVS vs Popt for standard planar junction FDPix and the U-shaped junction

4.2.3.2. Process flow

To obtain the U-shaped junction below the gate, two self-aligned process integrations are proposed *[KADURA 2019]*:

1. Using a ***gate last process*** *[CHATTERJEE 1997][GUILLAUMOT 2002]*:

   The process steps are shown in Figure 4-24. Starting with a doped GP and Well (P-type in our schematic), after removing the sacrificial gate, and before removing the cap oxide, an ion implantation step is used to counter dope the GP and obtain the N region just underneath the gate. This implies using high enough implantation doses, or preferably, multiple implantations at lower doses to avoid residual dopants in the

channel. After that the cap oxide, that prevented the channel to be impacted by the previous step, is removed and the gate is processed. The gradient that results in the intrinsic region will depend on the energy of implantation and the species used.

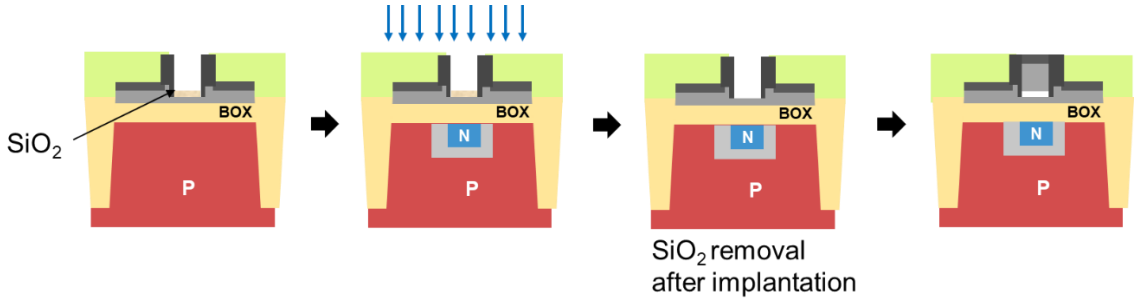


Figure 4-24: gate last process for processing the U-shaped junction FDPix

2. Using self-alignment with gate first process:

   In the standard flow, after processing the gate stack, the ion implantation step to counter dope the GP is performed. Controlling the tilt and energy will determine the depth and area of the N region. for example, a first implantation with low energy is used to ensure the doping of the BOX/GP area, then a higher energy implantation with a lower tilt can be used to dope the GP deeper. This is shown in Figure 4-25. Also, following the N region implantation, another implantation step can be added, with no tilt (perpendicular to the gate) to redefine the P-region at both sides of the N-region.

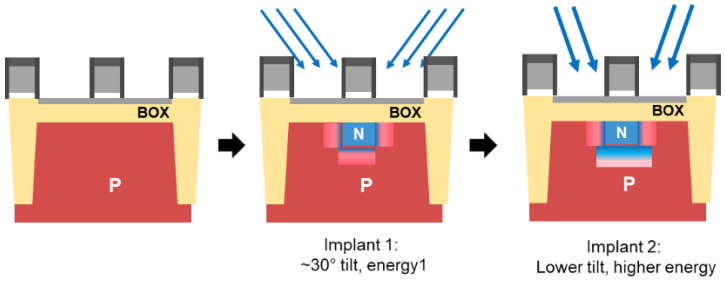


Figure 4-25: gate first self-aligned process for U-shaped junction

Comparing these two proposed techniques, the gate last approach is more convenient in the sense that it doesn't need multiple implantation steps to form the photodiode, and it is not limited by the gate length, while the gate first will be limited to short length transistors.

4.2.4. The FDPix for multiple spectrum detection

An important advantage of the FDPix sensor is the electrical isolation of the sensing transistor from the photosensitive element. Since all photodetectors are based on the photoelectric effect, i.e. light generating electrons, it implies that any material can be used as a photosensitive element. The conditions are that the structure is UTBB, the GP is floating, and the Well is biased at fixed potential. The photogenerated charges will accumulate at the BOX/GP interface and produce an LIVS. Therefore, to explore other parts of the electromagnetic spectrum, the FDPix can be implemented using other materials sensitive in the targeted wavelength range. For example, if the FDPix is to be used as a UV

detector, a wide-bandgap semiconductor should be used as the photosensitive element (ex: ZnO, GaN, GaAlN, SiC etc). Or if the IR range is to be enhanced, III-V materials or heterostructures (GaAs/InGaAs) can be used. Figure 4-26 shows the different materials with their respective wavelength detection range.

MATERIAL	WAVELENGTH SENSITIVITY (nm)
Ge	800 - 1700
InGaAs	800 - 2600
PbS	~1000 - 3500
Si	190 - 1100
GaN/AlGaN	300 - 400

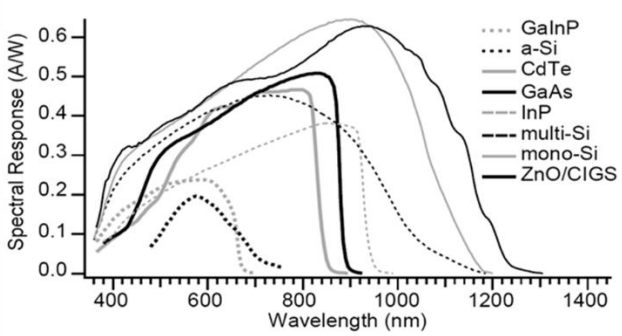


Figure 4-26: spectral response of different compound and semiconductor materials [LIU 2012]

Evidently, many materials are not CMOS process compatible, which makes it impossible to process the transistors on top. Therefore, they should be processed on a different wafer (usually 200mm or 100mm) and bonded to the BOX after thinning down the substrate in a similar manner as for the BSI process shown in Figure 4-15, where the bonded wafer would comprise the junction. The best solution would be to use oxide-oxide bonding between the BOX and the wafer on which the photosensitive junction is processed. Major advances on III-V/Si and II-VI/Si process and bonding widely used in photonics *[BOLKHOVITYANOV 2009][COMYN 2015][KLEM 1989][SADANA 2015]*, resulted in the availability of well controlled integration solution regarding these materials.

Since the transistor is processed (FEOL and BEOL), the bonding process temperature budget will be limited. Therefore, the selected process should not exceed the 500°C to insure the stability of the top transistor and BEOL *[BEN-AKKEZ 2013][BRUNET 2016][COUDRAIN 2009]*. Adding to the temperature budget limit is the pixel isolation. Since the substrate is thinned to the BOX, it means that the STI are also removed. Thus, trench isolations must be processed on the photosensitive wafer prior to bonding, or post bonding by using alignment marks visible from the back side.

Therefore, given that the material can be bonded to the backside of the FDSOI transistor, any readout circuit implemented with the sensing transistor can be used to detect a large range of wavelengths, which opens perspectives towards a universal readout circuit technology. This would replace the classical bonding used in sensors such as the Indium bumps that requires a more complex process and alignment.

4.3. FDPix scaling

The previous discussions in this chapter highlighted the effect of varying the dimensions of the transistor and junction on FDPix DC and transient performances, as well as its optical properties. In this section, we summarize the main technological and operational parameters and their influence on the figure of merits considered in Table 4-5 below.

Table 4-5: FDPix technological parameters impact on figure of merits

	Conversion gain (BF/C_{eq})	Sensitivity		Speed	DR		Spectral response (responsivity)	Steady state LIVS	FF	
		Linear	log		Linear	log			FSI	BSI
Lg	x	x	x	x	x	x	x	x	---	x
W	-	++	++	++	-	+	x	x	---	x
T_{OX}	+++	++	++	x	x	x	x	++	x	x
T_{Si}	---	--	--	x	x	x	x	--	x	x
T_{BOX}	--	--	--	+	x	x	x	--	x	x
Ti	++	+++	--	+++	--	++	++	---	x	x
Area	--	--	x	++	-	+	x	x	++	x
t_{int}	x	+++	x	x	--	++	x	x	x	x

Scaling down the device will have an impact on sensitivity that can be counter balanced by increasing the body factor, which increases the conversion gain, and using BSI. If the minimum dimensions of a GO1 and GO2 devices would be used, the pixel area defined as $W*(L+S_A+S_B)$ would be approximately 0.0182µm² for the GO1, and 0.0624µm² for the GO2. However, it is recommended in image sensor design (analog sensors in general) to not use minimum length transistor to avoid short channel effect and the degradation of the transistor performance, but also and most importantly, larger dimensions reduce process variability and thus mismatch induced noise in analog circuits.

The optimization of the FDPix is application dependent. For example, if the FDPix is to be used as a visible light detector, speed and sensitivity at low light, as well as noise performances are dominant parameters to be optimized by using a high BF, and a PiN junction. Other applications would require high DR but allows long acquisition time, thus an NP junction should be used with a higher capacitance. The use of the FDPix presents also major process simplifications since bonding can be used without the need of electrical connections. It can also be used to detect any range of wavelengths just by changing the photosensitive material. In conclusion, the FDPix provides a versality of implementation that open perspectives towards highly integrated light sensors.

4.4. Chapter four summary

In this chapter, the main parameters of the FDPix were investigated, and their influence on both DC and transient responses were compared. This included the photodiode parameters and leakages, and the dependence on the temperature. The impact of operation conditions such as the reset pulse amplitude V_B and the integration time t_{int}, was also demonstrated. After that the optical properties of the FDPix were discussed and alternative integration solutions were proposed to increase the sensitivity.

Important points:

- Conversion gain depends primarily on the body factor which quantifies the coupling between front and back interface, and on junction capacitance.
- The junction profile determines its capacitance, on which depends the conversion gain and the FWC as was presented. The dynamic range of each region of operation is directly proportional to the FWC.
- The leakage of the photodiode reduces its shunt resistance thus its RC time constant. However, it also reduces its sensitivity and saturation LIVS.
- The FDPix dependence on temperature follows the same trends as image sensor, considering the dependence of the dark current on temperature, which in turn lowers the open circuit voltage.
- The gate is what primarily shadows the sensor when front side illumination is used, considering non-silicided S/D.
- Since the photosensitive element is under the sensing transistor, BSI should be privileged.
- BSI process requires an etch stop layer or etch-stop technique that insures the correct thinning thickness and good surface quality necessary to obtain high quantum efficiency.
- Using BSI, the junction profile can be optimized to drive the photogenerated charges underneath the channel where the coupling occurs, using a U-shaped photodiode.
- The FDPix device can be used to detect any range of wavelength by using other materials than silicon as photosensitive element as long as the structure (ultra-thin body and BOX) is maintained. These materials should response to requirements regarding bonding with the BOX interface and thermal budget used.
- The FDPix is scalable to more advanced technology nodes, keeping a high body factor.

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CHAPTER FIVE

Chapter 5 : FDPix-based pixel circuit design and validation

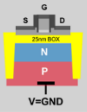
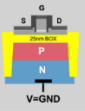
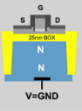
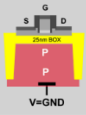
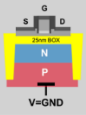
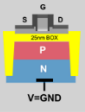
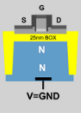
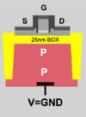
The FDPix as presented so far, results in a current variation at the output in response to the LIVS. In this chapter, we present different circuit design based on the FDPix sensor. The main purpose being to convert the current variation into analog voltage variation and time domain variation. Multiple circuits implementations are proposed in the analog and digital domains. The circuits are based on the complementarity property of the FDPix introduced in chapter 2. We will demonstrate a 2T FDPix sensor that employs an N-type and P-type FDPix, where a gain is obtained on the LIVS. Also, the basic logic gate, i.e. CMOS inverter, is made sensitive to light and exploited to design a Pulse Width Modulated (PWM)-based pixel. A time domain signal variation with light intensity is obtained using this design. The designed circuits were all fabricated using 28nm FDSOI technology, and the following analysis and discussions are based on SPICE simulations and opto-electrical characterization results. The implementations proposed will be compared based on the characteristics of the pixel (#of T/pix, FF, size, DR) and an estimation of the static power consumption are presented.

The last part of this chapter discusses different perspectives for using the FDPix for smart pixel sensors design. As will be presented, logic devices and memories can be made sensitive to light and functions can be implemented for light detection.

5.1. FDPix complementarity property

As introduced in Chapter 2, the complementarity property of the FDPix allows us to consider different CMOS implementations. Analogous to the back bias in FDSOI transistor, the N-type and P-type FDPix exhibit different responses for the same GP potential change, which results in complimentary responses. When the N- and P-type FDPix are integrated with the similar photodiode orientation, they will exhibit opposite polarity LIVS, while if they are integrated with opposite photodiode orientation, the LIVS polarity is the same for both. The different configurations are summarized in Table 2.1 which is replicated below. As can be seen in Table 5-1, this provides design options regarding whether to use the same photodiode orientation which would simplify the process, or opposite orientation which would synchronize the N-type and P-type responses.

Table 5-1: FDPix available configurations for N- and P-type transistors and different diode orientations with the corresponding LIVS

FET type	PFET				NFET			
Configuration below the BOX								
Light effect	negative back bias	positive back bias	none	none	negative back bias	positive back bias	none	none
FET Light-Induced V_T-Shift (LIVS)	forward BB	reverse BB	none	none	reverse BB	forward BB	none	none
LIVS amplitude	Increases w/ P_{OPT} and BF	Increases w/ P_{OPT} and BF	none	none	Increases w/ P_{OPT} and BF	Increases w/ P_{OPT} and BF	none	none

Some design consideration must be pointed out:

- The nominal V_T depends on the type of GP and its doping concentration.
- Design wise, the Design Rule Manual (DRM) proper to the 28nm technology provides rules regarding opposite well implantation minimum distance, which means that to optimize the size of the layout, it is better for the two MOSFETs to have a common Well.

We took into account these considerations when designing the structures presented in this chapter, privileging an opposite type of MOSFET instead of an opposite type of Well. However, these considerations are especially important when the standard 28nm technology is used. If a specific device optimization is possible, then the nominal V_T can be set whatever the type of the GP by adjusting the gate work function.

In the next section, analog pixels are first demonstrated starting with the 1T current mode FDPix. Following that, based on this feature of complementarity, we investigated analog circuit design where the V_T variation is converted to output voltage variations.

5.2. Analog FDPix

5.1.1 Current mode pixels

When the FDPix is characterized as a single device, the output that we investigated so far is the variation of transistor drain current. From the variation of current and knowing the SS, the LIVS can be calculated. If this device would be used as a 1T pixel, the current needs to be readout of the pixel array (current mode pixel).

Current mode pixels drew some attention due to their lower power consumption, low noise, and ease of analog processing which allows in-plane processing. However, the major drawback of such pixel which limited their implementation is the FPN, since CDS is not easily performed on a current output. However, different architectures were developed. One of the earliest works was presented by *[MCILRATH 1997]* where the current mode readout techniques are evaluated to compare the noise level of such architectures. Current mirror buffers are used to draw the signal off chip, and a differential readout scheme is used to reduce the noise. In *[GRUEV 2010][PHILIPP 2007][PHILIPP 2005]*, they replaced the source follower and row select of standard 3T APS by PMOS transistors, where the source follower now acts as a transconductance amplifier converting the voltage drop on the diode to current. A fixed voltage is applied on the column, which can be varied to modulate the conversion gain of the pixel. Hong et al. *[HONG 2001]* proposed an inverted logarithmic current mode pixel, that reduces the FPN of conventional logarithmic sensors, and increase the voltage swing while maintaining high DR. In the proposed design, the pixel output is the modulated source follower current that is readout and converted to voltage using a transresistance amplifier located off-chip.

Although current mode pixel presents some advantages, the difficulty of implementing a CDS scheme to remove FPN, has preventing these pixels to be used in mainstream technologies. Taking into consideration these drawbacks, we privileged the readout of a voltage rather than a current. Therefore, we designed circuits that converts threshold voltage variation into output voltage variations. However, possibility of using the FDPix as a current mode pixel is not completely discarded. Our purpose here is to show that both options are available.

The main idea to convert LIVS to output voltage variation is to take advantage of the CMOS technology. As discussed in the previous section, the N-type and P-type FDPix have opposite LIVS for the same photodiode orientation. This property led us to investigate CMOS analog circuit amplifiers as potential pixel circuits. In regular amplifiers, the output gain can be tuned with the transistor dimensions and is sensitive to the transistors $V_{T.}$ The two inverting amplifiers studied are the saturated load amplifier, (i.e. source follower, cascode connected), and the push pull amplifier (i.e. CMOS inverter). Both are presented next and compared in section 5.4 regarding size, linearity, gain, range of operation, and power consumption.

5.1.2 Saturated load inverter amplifier

The circuit schematic of the standard saturated load inverter is shown in Figure 5-1.a. The circuit is composed of two transistors: a diode connected PMOS transistor, where the gate and drain are short circuited, and an NMOS used as a driver transistor. The diode connected PMOS is always in saturation, and thus represent the saturated load of the amplifier. The Voltage Transfer Curve (VTC) of the amplifier is obtained using SPICE simulation and is shown in

Figure 5-1.b. where the output voltage (V_{OUT}) is plotted vs input voltage bias (V_{BIAS}). GO1 devices were used with L=W=1µm. We can see that the input level is inverted at the output, which makes this amplifier, an inverting amplifier.

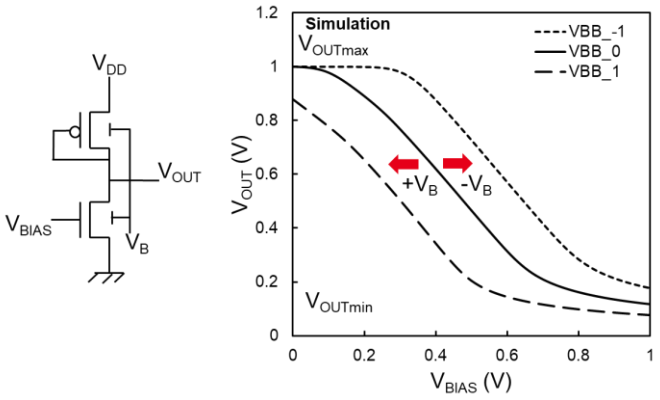


Figure 5-1: saturated load inverter a) schematic b) VTC at different VB

In Figure 5-1.b we can identify from the VTC different regions of operation of the inverter depending on the applied V_{BIAS}. The maximum V_{OUT} is when V_{BIAS} is zero, which bias the NMOS in cutoff. Thus, it can be expressed as:

$$V_{OUTmax} = V_{DD} - |V_{Tp}| \tag{5-1}$$

The minimum V_{OUT} is achieved when V_{DD} is applied on the NMOS gate, in this case the NMOS is in the linear regime, and the PMOS in saturation. By equating the drain current equations of both transistors and solving for V_{OUT} assuming the N and PMOS have identical V_T (V_{TN}=V_{TP}=V_T), the following equation is obtained:

$$V_{OUTmin} = V_{DD} - V_T - \frac{V_{DD} - V_T}{\sqrt{1 + \left(\frac{\beta_p}{\beta_n}\right)}} \tag{5-2}$$

Where β_n=C_{ox}*µ$_n$*W_n/L_n, and β_p=C_{ox}*µ$_p$*W_p/L_p, are the gain factors of the N- and PMOS respectively. The region of interest in our case, is the transition region where the maximum V_{OUT} variation can be achieved at a constant V_{BIAS}. Since the PMOS is diode-connected, it is always in saturation (V_{DS}<V_{GS}-V_{Tp}). Therefore, the current flowing in the circuit can be calculated as:

$$I_{Dsat} = \frac{\beta_p}{2}\left(V_{SG} + V_{Tp}\right)^2 \tag{5-3a}$$

Considering the voltage applied on the terminals the previous equation can be rewritten as:

$$I_{Dsat} = \frac{\beta_p}{2}\left(V_{DD} - V_{OUT} + V_{Tp}\right)^2 \tag{5-3b}$$

Since in the transition region, the NMOS is also in saturation, its drain current equation can be written as:

$$I_{Dsat} = \frac{\beta_n}{2}(V_{BIAS} - V_{Tn})^2 \tag{5-4}$$

Equating (5-3a) and (5-4) and solving for V_{OUT}, the following expression is obtained:

$$V_{OUT} = V_{DD} + V_{Tp} - \sqrt{\frac{\beta_n}{\beta_p}}(V_{BIAS} - V_{Tn}) \quad (5\text{-}5)$$

We can see from (5-5) that the VTC is directly proportional to the threshold voltages of the transistors. This is demonstrated in Figure 5-1.b. where a common back bias is applied to the N and PMOS back gates. The curve shifts depending on the polarity of the bias. From (5-5), we can see that the output voltage increases, i.e. the VTC shift towards V_{DD}, when V_{Tn} increases and $|V_{Tp}|$ decreases (negative V_B), and vice versa (positive V_B). This is very convenient for our application since using the same diode orientation, the opposite V_T shift polarity is obtained on the PMOS and NMOS. Therefore, the two transistors can be processed on a common Well, which optimizes the pixel size. Also, we can see from (5-5) that V_{OUT} will also depend on the beta ratio (β_n / β_p) which implies that it can be tuned by changing the dimensions of the transistors as will be further discussed in the next section. The modulation of the V_{OUT} with incident light intensity is presented next when both transistors are replaced by FDPix.

5.1.2.1 FDPix saturated load inverter: DC and transient characterization

By replacing the driver and the saturated load transistors by an N-type and P-type FDPix respectively, we designed a 2T pixel sensor. The output exhibits a Light Induced V_{out} Shift ($LIV_{out}S$), analogous to the LIVS of the single FDPix which can be defined as:

$$LIV_{out}S = V_{OUT\,light} - V_{OUT\,dark} \qquad @V_{BIAS} = Const \quad (5\text{-}6)$$

The schematic of the FDPix saturated load inverter is shown in Figure 5-2.a. The structures were layouted using 28nm DRM, varying the dimensions to obtain different beta ratio. The devices used are GO2 to optimize the conversion gain. Since the characterizations are performed using FSI, the S_a/S_b of the transistors are larger than minimum dimensions to maximize the light absorption, as can be seen in the layout (Figure 5-2.c). This is only to ensure that a response is measurable, and the functionality of the circuit validated. For practical implementation, the minimum dimensions can be used, taking into consideration the scaling effect discussed in Chapter 4. Also, in this architecture, the FF is maintained high since both transistors are sensitive to light. At the end of this section, we present examples of more compact pixel layout using minimum dimensions available for this technology.

The fabricated lot does not contain any specific implants; therefore, the junction is located between the unipolar N-type GP and Well as in standard process, and the p-type substrate as shown in Figure 5-2.b, which is the standard configuration for FDSOI process. The N-Well is left floating and the substrate is kept at ground for the device to work as an FDPix. From the sideview in Figure 5-2.b, we can see that the junction is located deeper, pass the STI depth (280nm). For studying the single device this is not a major problem, however for array implementation, it will result in an increased crosstalk. Moreover, this non-optimized implementation is for the purpose of design demonstration and validation.

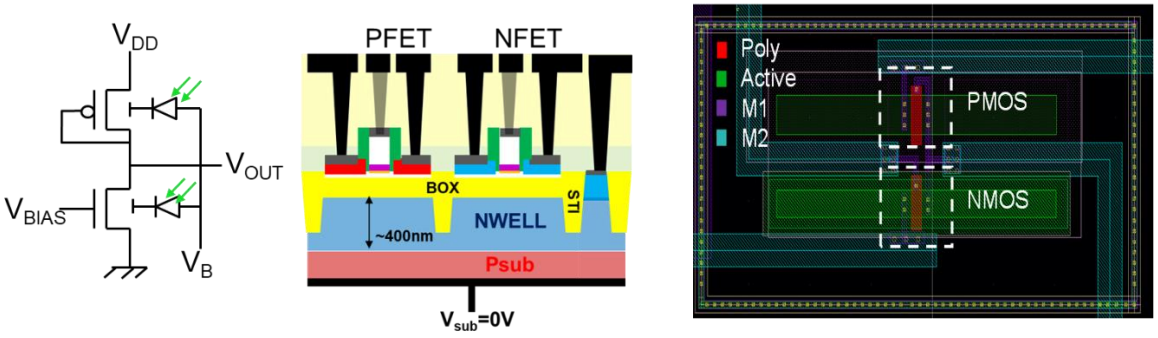


Figure 5-2: source follower amplifier implemented using FDPix sensors a) schematic b) sideview, c) layout view for the 1.51/1.0µm W ratio, and L=330nm

Since the diode is NP oriented, a positive LIVS is expected for the N-type FDPix and a negative one for the p-type FDPix, which results in a VTC shift to higher V_{BIAS}, equivalent to the case where a negative V_B is applied. This is demonstrated in Figure 5-3.a, where the static experimental VTC of the FDPix inverter is measured for different light intensities, while applying a V_{DD} of 1V. The light source used is a wide band Xenon lamp (more details in appendix B), and the transistors dimensions are L=1µm, and width ratio W_n/W_p is 1.1/1.56µm. We extracted the steady state $LIV_{out}S$ at a V_{BIAS} of 0.45V and plot it vs Popt in Figure 5-3.b. Single FDPix N-type and P-type were also fabricated with the same specifications as the ones implemented in the inverter and their LIVS is also plotted in Figure 5-3.b. As can be noticed, a gain of almost x4 on the single FDPix LIVS is obtained. Also, since the variation of V_{OUT} with V_T is linear, we obtain the same intrinsic logarithmic response as the single device, and the DR is maintained at 120-130dB.

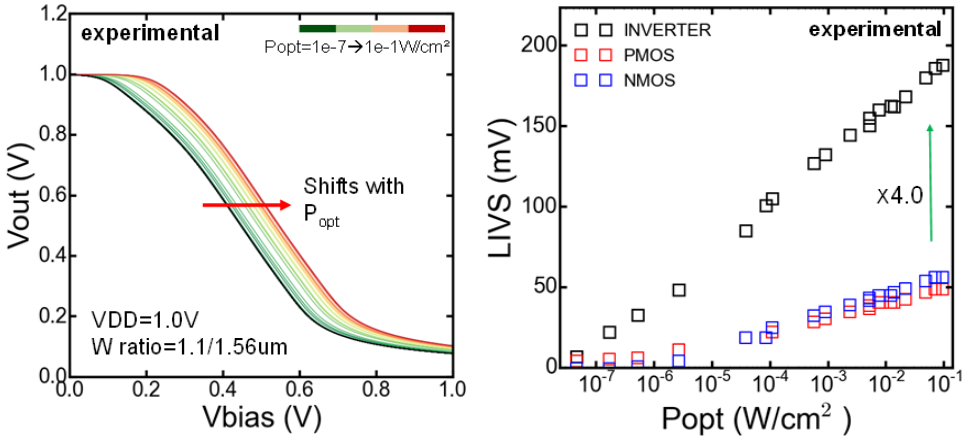


Figure 5-3: a) VTC of source follower amplifier at different light intensity b) LIVS vs Popt for N-type and P-type FDPix and $LIV_{out}S$ vs Popt for light sensitive source follower amplifier

The gain is calculated by deriving (5-5) supposing LIVSn=LIVSp, the following expression is obtained:

$$\frac{dV_{OUT}}{dV_T} = \frac{\mathrm{LIV_{out}S}}{\mathrm{LIVS}} = \sqrt{\frac{\beta_n}{\beta_p}} + 1 \qquad (5\text{-}7)$$

From (5-7), it is clear that by increasing the beta ratio, smaller PMOS and/or wider NMOS, the gain can be modulated as shown in Figure 5-4.a, where it increases from 4 to almost 5.5 at V_{BIAS}=0.45V using a width ratio W_n/W_p of 2.2/0.77µm. The higher gain, however, is obtained at the expense of a narrower operation range for V_{BIAS} and increase in size. This tradeoff is shown in Figure 5-4.b. If in the previous example, the V_{BIAS} was selected to be too close to V_{OUTmax} or V_{OUTmin}, the sensor would have saturated, and the DR reduced. Therefore, V_{BIAS} should be carefully selected to maximize the range of intensities detected, and the gain.

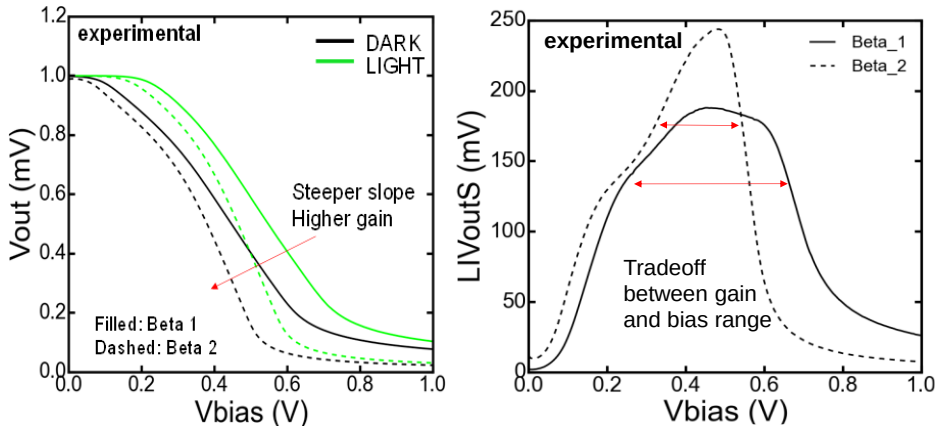


Figure 5-4: a) VTC of source follower for different Beta ratio b) LIVoutS vs V_{BIAS} for different Beta ratio

Now the transient response is studied. Using SPICE simulations, the transient response of the FDPix saturated load inverter to a light pulse is simulated, with and without applying a reset pulse on the common back-gate. The results are shown in Figure 5-5 where, the light pulse of 0.1W/cm², the reset pulse of 1.5V with 1ms pulse width, and finally the V_{OUT} for the two cases, are shown. The simulated devices are GO1 with Lg=W=1µm for both N and PMOS transistors. The sensor transient is identical to the single FDPix discussed in Chapter 3. The response to the light pulse is faster than the long decay that follows it to return to equilibrium. As was the case for the single FDPix, the back gate is used to accelerate this transient, resetting the FDPix saturated load inverter. Since both transistors are on the same Well, the reset pulse is applied commonly to both N and PMOS back gate at the falling edge of the light pulse. As we can see from Figure 5-5, the V_{OUT} goes back to an initial output level, which eliminates the transient.

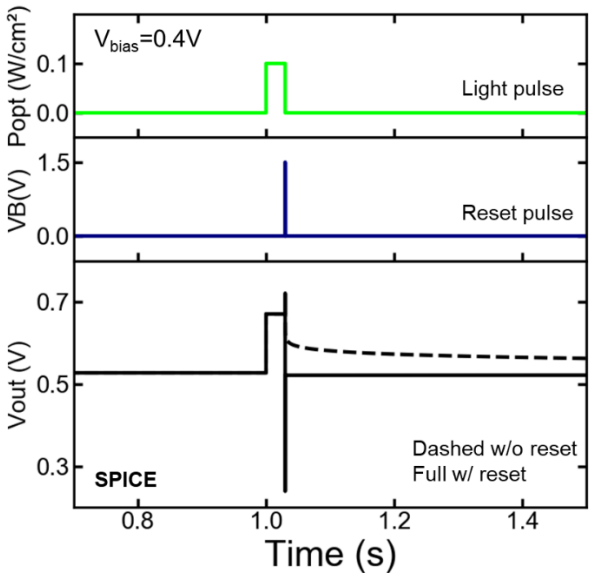


Figure 5-5: Transient response of the FDPix saturation load inverter to light pulse for two cases: without reset (dashed line) and with reset (full line)

Thus, we can expect the same behavior as the 1T FDPix that exhibits a linear-log response when sampled in transient and at steady state. The CMOS implementation and the resulting gain will result in a better sensitivity in both regimes of operation, while keeping the high DR.

5.1.2.2 Static power consumption

The power consumption in standard image sensor depends on the source follower, the readout circuit, the bias circuit, and the ADC *[CHOI 2017]*. In this section, the power consumption is evaluated considering only the 2T FDPix single device static dissipation. The purpose is to compare with the other architectures proposed in this chapter. The average total power consumed is equal to the sum of the static and dynamic power as follows:

$$P_{tot} = P_{static} + P_{dynamic} \tag{5-8}$$

The static power depends on the leakage current of the transistors when the sensor is on standby (V_{BIAS}=0), and on the supply voltage. It is calculated using the following equation:

$$P_{static} = V_{DD} * I_{leak} * N_{pix} \tag{5-9}$$

Where N_{pix} is the total number of pixels in the array (row*column) and is equal to one for a single pixel. I_{leak} is the average current level in standby (V_{BIAS}=0, V_{DD}). Figure 5-6 shows the SPICE simulation results for the saturated load inverter in GO1 device with W=L=1µm for both transistors. When the sensor is at V_{BIAS}=0, the driver NMOS transistor is in cutoff. This results in an almost zero static power consumption, which mainly depends on the leakage current of the NMOS. In the simulation results, this current is equal 10pA. However, since the PMOS is always in saturation as previously mentioned due to its diode connection, the current at V_{BIAS}=V_{DD} is very high (>10µA) since both transistors are on. For this reason, this type of inverter is never used in digital circuit. P_{static} is calculated for one pixel (N=1), and

for a QVGA format array (row=320, column=240) using (5-9) for different supply voltages, and the results are summarized in Table 5-2 below.

Table 5-2: Static power consumption values for the FDPix saturated load inverter at different V_{DD}

V_{DD} (V)	I (pA) @V_{BIAS}=0	I (µA) @V_{BIAS}=V_{DD}	avg(I) (µA)	P_{static}(µW)	QVGA (mW)
0.4	9.43	0.716	0.358	0.143	11
0.6	9.65	4.74	2.37	1.42	109
0.8	9.86	13.2	6.60	5.28	405
1.0	10.1	26	13	13	998

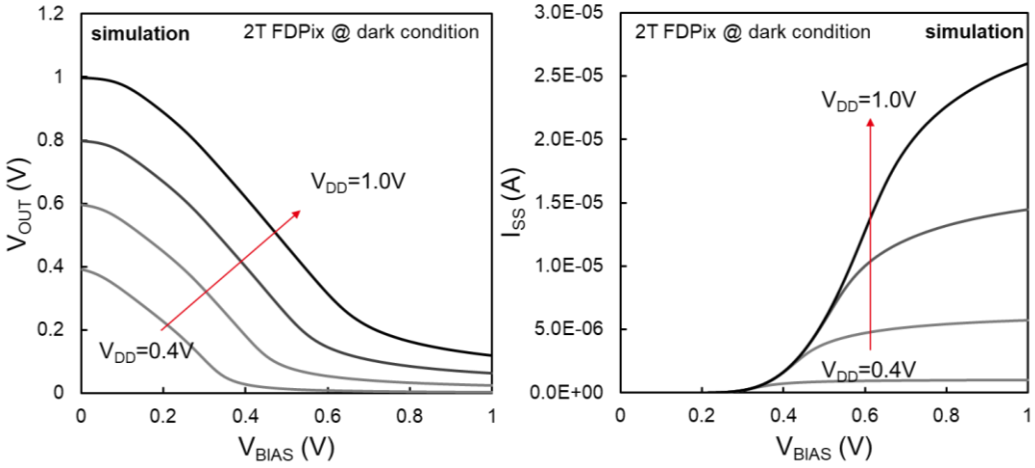


Figure 5-6: SPICE simulation for saturated load inverter at different V_{DD} a) VTC b) supply current I_{SS}

This static power consumption is not acceptable, especially since the dynamic power has an even higher contribution to the overall power consumption. To reduce it, the most obvious solution would be to lower the supply voltage. For example, in the previous results, since GO1 devices are used, the V_{DD} was lowered to 0.4V which considerably reduced the leakage, and also, will allow the use of a lower V_{BIAS}. This can also be seen in Figure 5-7.a where the experimentally measured VTC of the GO2 FDPix saturated load inverter is measured at different V_{DD}. However, changing V_{DD} will also affect the output voltage range of operation. As can be seen in Figure 5-7.b, where the $LIV_{out}S$ vs V_{BIAS} is plotted, the higher the V_{DD} the larger is the range of bias operation.

Another solution would be to avoid short circuiting the gate and drain and polarize the PMOS gate independently similarly to a linear load inverter *[JAEGER 2011]*. This would greatly improve the static power consumption since the PMOS can be biased in cutoff to reduce leakage. However, it would require another independent supply voltage to bias the PMOS, which complexifies the BEOL. Nevertheless, it is a more feasible implementation compared with the diode connected load case.

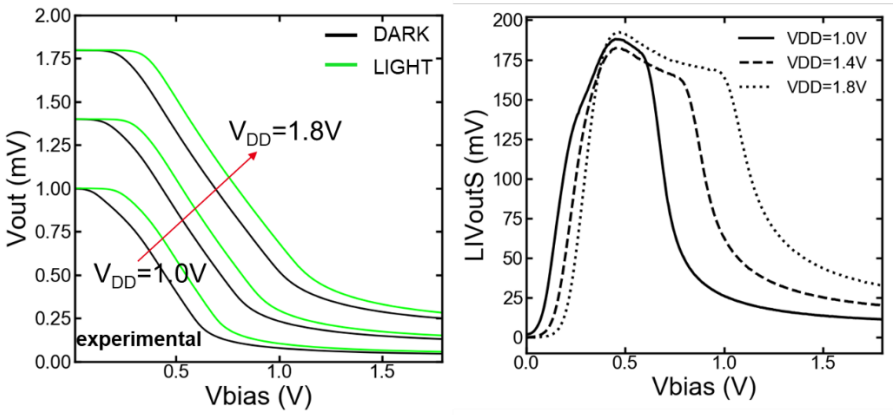


Figure 5-7: a) VTC of source follower at different V_{DD} b) $LIV_{OUT}S$ vs bias for different V_{DD}

5.1.2.3 Minimum size implementation

The previously fabricated and tested devices were fabricated using large dimensions since the priority was to validate the concept by ensuring a high signal using GO2 devices. Although it is not recommendable to design using minimum dimensions which cause higher mismatch, in this section, an example of pixel layout using minimum dimensions for GO1 and GO2 devices is shown. GO1 (BF~65mV/V) minimum dimension 1T FDPix were already tested and it resulted in an LIVS ~30mV, which means that when used in this structure where the FSI can be optimized by using non-silicided S/D and optimizing the BEOL, it could be amplified to 120mV. To improve even more the FF, BSI should be used as was discussed in Chapter 4.

An example of a what could be a layout of the 2T FDPix saturated load inverter in an array-like environment is shown in Figure 5-8 (not to scale). Based on the 28nm FDSOI design rule manual (DRM), the total pixel area if designed using GO1 devices is in the order of 0.22µm², and if designed using GO2 devices, is in the order of 0.5µm². these dimensions are smaller than most available pixels that used less advanced technological nodes.

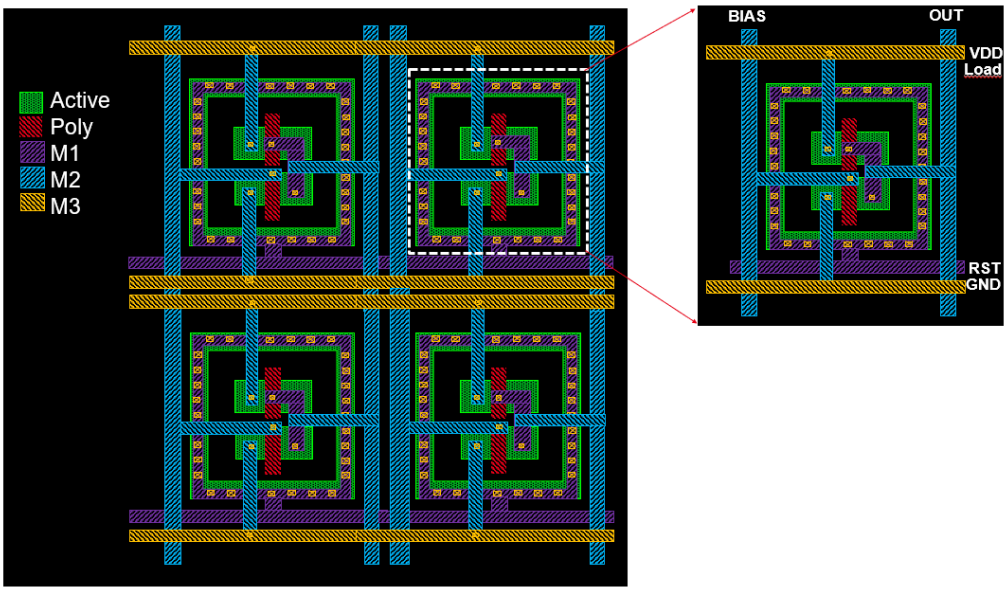


*Figure 5-8: Example of layout (not to scale) of 2*2 pixels of 2T FDPix*

To conclude, the light sensitive saturated load inverter can be used as an efficient high DR, and high sensitivity 2T pixel sensor. However, leakage current reduction techniques must be implemented. In the next section, a building block for digital application, namely the CMOS inverter, is investigated.

5.1.3 Push pull amplifier: CMOS inverter

In the same manner as for the saturated load inverter, the push-pull inverter, also known as CMOS inverter, is investigated. The goal being to characterize the light response of this inverter to further implement it in digital-oriented design. The main motivation for using this configuration is the power consumption. The CMOS inverter has the particularity of consuming very low power since current flows only when it switches from high-to-low or low-to-high state. Its VTC also depends on the V_T of the PMOS Pull Up (PU) and NMOS Pull Down (PD) transistors and is shown in Figure 5-9 below.

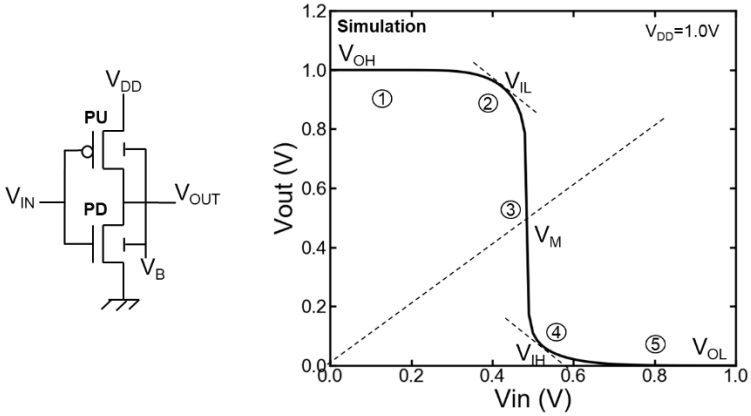


Figure 5-9: CMOS inverter schematic and VTC

As indicated in Figure 5-9, the inverter VTC can be divided into five regions. In each of these regions, the associated V_{IN} and V_{OUT} will have a dependence on the V_T of the PU and PD transistors. The following derivations were adapted from *[RABAEY 1995]* and *[WESTE 2011]*.

∗ *Region (1):*

In this region, the input voltage is in the range of $0 < V_{IN} < V_{Tn}$, resulting in the NMOS biased in cutoff, and the PMOS in linear. The output voltage level in this region (V_{OH}) is pulled up to V_{DD} by the PMOS. Since the NMOS is in cutoff, only its leakage current is flowing (~pA range), therefore the inverter consumes almost no power when biased in this region, i.e. standby.

∗ *Region (2):*

The V_{IN} range is $V_{Tn}<V_{IN}<V_{DD}/2$, which corresponds to the NMOS biased in saturation ($V_{OUT}>V_{IN}-V_{Tn}$), and the PMOS in linear. The parameter to be extracted is the V_{IL}, which is the maximum input voltage before the inverter switches. The V_{OUT} in this region is calculated by equating the linear drain current of the PU transistor with the saturation drain current of the PD transistor. The obtained V_{OUT} expression in region 2 is:

$$V_{OUT} = V_{in} - V_{TP} + \sqrt{(V_{in} - V_{DD} - V_{TP})^2 - \frac{\beta_n}{\beta_p}(V_{in} - V_{TN})^2} \quad (5\text{-}10)$$

Now by deriving the gain and equating to -1, the V_{IL} is obtain and is expressed as:

$$\frac{dV_{OUT}}{dV_{IN}} = -1 \quad (5\text{-}11a)$$

$$V_{IL} = \left(1 + \frac{\beta_n}{\beta_p}\right)^{-1} * \left(2V_{OUT} + \frac{\beta_n}{\beta_p}V_{TN} - V_{DD} - |V_{TP}|\right) \quad (5\text{-}12b)$$

∗ *Region (3):*

This is called the transition region. In this region, both NMOS and PMOS are in saturation, therefore, a high transition current will be flowing, and is thus the region that results in the most dynamic power. The switching voltage (V_M), which is where V_{OUT}=V_{IN}, is modeled by equating the drain saturation current of the PU and PD transistors. The following expression is obtained:

$$V_M = \frac{V_{DD} + V_{Tp} + \sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \quad (5\text{-}12)$$

when β_n=β_p, and V_{Tn}=V_{Tp}, the VTC is symmetrical/balanced, and the V_M is equal to $V_{DD}/2$. This region will be further explored when implementing the FDPix sensor.

∗ *Region (4):*

The V_{IN} range is $V_{DD}/2 < V_{IN} < V_{DD}-V_{Tp}$, where the NMOS is in linear regime, and PMOS in saturation. The parameter to be extracted is the V_{IH}, which is the minimum input voltage before the inverter switches from high to low. It is modeled by equating the saturation current of the PU transistor with the linear current of the PD transistor results in the V_{OUT} expression as:

$$V_{OUT} = V_{in} - V_{TN} + \sqrt{(V_{in} - V_{TN})^2 - \frac{\beta_p}{\beta_n}(V_{in} - V_{DD} - V_{TP})^2} \quad (5\text{-}13)$$

Deriving (5-13) to obtain the gain and equating to -1 results in:

$$V_{IH} = \left(1 + \frac{\beta_p}{\beta_n}\right)^{-1} * \left(2V_{OUT} + V_{TN} + \frac{\beta_p}{\beta_n}(V_{DD} - |V_{TP}|)\right) \quad (5\text{-}14)$$

∗ *Region (5):*

This is the logic Zero state, where the $V_{IN} > V_{DD}-V_{Tp}$, resulting in the NMOS being biased in linear and the PMOS in cutoff. The output is thus pulled down by the NMOS to GND (V_{OL}=0). Also, as for region 1, since one of the transistors is in cutoff, almost no power is consumed in this state.

To evaluate the dynamic response of the inverter, the commutation delay (t_p) is of major importance. It is defined as the mean delay between the input and output signal at 50% for both rise and fall time, as depicted in Figure 5-10. The

high-to-low transition delay (t_{pHL}) will depend on the PD transistor V_{Tn}, while the low-to-high (t_{pLH}) will depend on the PU transistor V_{Tp}. Therefore, to obtain a symmetrical response the two threshold voltages must be identical. In CMOS inverter design, the width ratio between the two transistors usually accounts for the difference in mobility (which arises from the difference in effective mass between electrons and holes), and will result in a balanced V_T.

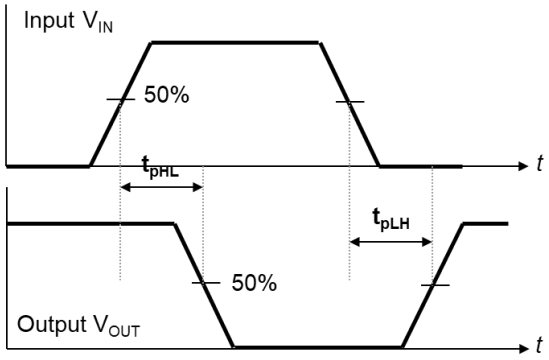


Figure 5-10: CMOS inverter propagation delay definition

The propagation delays can be expressed as:

$$t_{pHL} = \frac{C_L V_{DD}}{2}\left(\frac{1}{\beta_n (V_{DD} - V_{TN})^2}\right) \quad (5\text{-}15a)$$

$$t_{pLH} = \frac{C_L V_{DD}}{2}\left(\frac{1}{\beta_p (V_{DD} - V_{TP})^2}\right) \quad (5\text{-}16b)$$

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} \quad (5\text{-}16c)$$

Where C_L is the load capacitance. In the case of a chain of inverters such as in a ring oscillator, C_L is the sum of: the output capacitance of the first inverter, the line capacitance, and the input capacitance of the following inverter which is mainly the gate capacitances. The dependence of the propagation delay on the threshold voltages of the transistor is the key property that will be exploited for Pulse Width Modulation (PWM) based design discussed in section 5.3.

Based on the previous discussion it is clear that the VTC and propagation delay of the inverter can be modulated by changing: the β_n/β_p ratio (i.e. transistor dimensions), the V_{Tn} and V_{Tp}, and the V_{DD}. Since we're using the FDSOI technology, a back bias applied on the PU and PD transistors can also be used to dynamically tune the VTC and thus the t_p. When the same V_B is applied on both PU and PD, the VTC curve will shift either to higher (PU: FBB, PD: RBB) or lower (PU: RBB, PD: FBB) V_M values. This is shown in Figure 5-11.a. where SPICE simulations are performed on a GO1 type CMOS inverter with L=W=1µm. Moreover, if a different V_B polarity is applied on each transistor, or if V_B is applied on only one of the two transistors, the slope of the VTC is changed as shown in Figure 5-11.b.

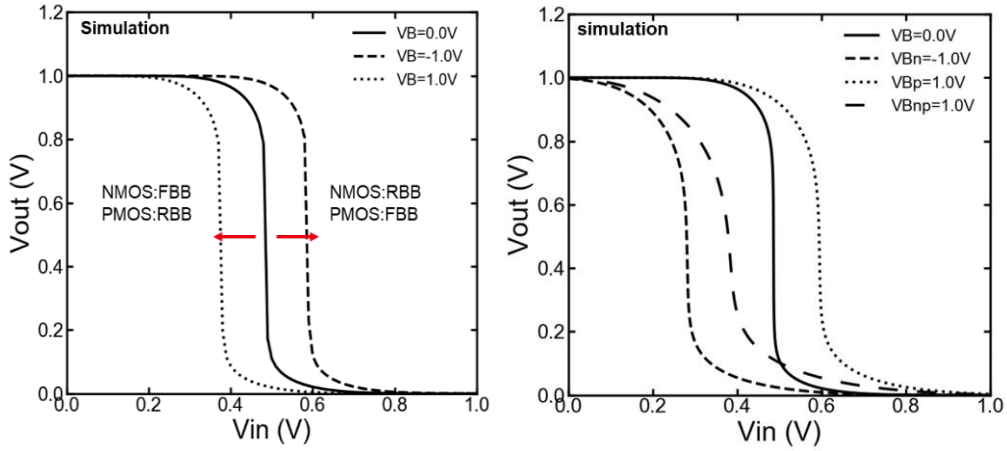


Figure 5-11: VTC of CMOS FDPix inverter with bias applied on either the NMOS, PMOS, or both

In the next section, the CMOS inverter VTC is modulated with the LIVS of its PU and PD transistors when replaced by FDPix devices.

5.1.3.1 FDPix light sensitive CMOS inverter: DC and transient characterization

Based on the previous discussion, we designed a light sensitive CMOS inverter with the PU transistor replaced by a P-type FDPix and the PD transistor by an N-type FDPix as shown in the inset of Figure 5-12.a. The junction is the same as the one previously shown in Figure 5-2, where the standard implants were not modified. Therefore, it has an NP junction between the N-Well and the P-substrate and is common to both N and PMOS. The transistors are GO2 with L=330nm and Wp/Wn=1.56/1.1 µm. The LIVS exhibited by each transistor (positive for NMOS and negative for PMOS) results in shifting the VTC of the inverter as a function of light intensity as shown in Figure 5-12. Increasing optical power results in a higher shift of the inverter's V_M proportional to the LIVS of both transistors as expected from equation (5-12), that shows the linear relationship between V_M and the LIVS. The gain in this case is equal to unity ($dV_M/dLIVS = 1$) which means that changing the beta ratio will not affect the amplitude of the shift. The V_M light induced shift is plotted vs optical power density in Figure 5-12.b. where the same logarithmic response is obtained as expected.

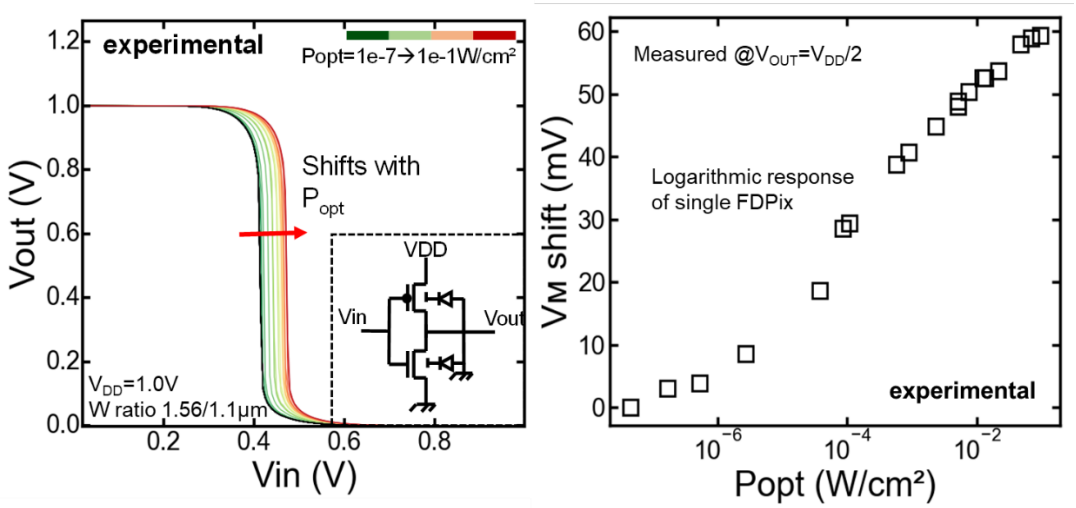
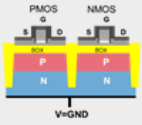
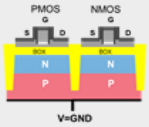
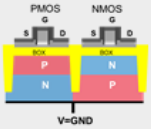
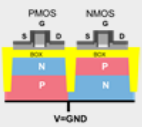


Figure 5-12: VTC of FDPix CMOS inverter a) for different light intensities b) LIV$_M$S vs Popt for CMOS inverter FDPix

If the CMOS inverter is used as an analog amplifier, a bias voltage would be applied on the input, and the output shift as a function of Popt would be readout. Although the inverter has a high gain compared with the saturated load inverter, the transition region slope is very abrupt which results in a too narrow region of bias operation. Also, the variation of output voltage with respect to Popt is highly non-linear which distorts the log response of the sensor. This is where the application demands different approaches; for digital, it is required to make this slope as steep as possible to reduce dynamic power, while in analog, the operation region should be as large as possible to allow a high range of operation. The slope of the VTC depends on the beta ratio between the PU and PD transistors. Also, as previously mentioned, it can be modulated by applying an opposite back bias on the transistors. However, if both transistors are to be back biased using different V_B polarity, it requires to isolate their respective wells. This is turn will negatively affect the dimensions of the pixel.

We previously showed in Figure 5-12 the response of the inverter to light by a V_M shift proportional to the applied optical power density. Since the photodiode implanted was NP oriented, the V_M shifted to higher values towards V_{DD}. As it is the case for FDPix single device, by using the opposite diode orientation the opposite effect is obtained. Thus, by using a PN oriented junction, the V_M will shift to lower values (towards GND). The use of a common well is advantageous process wise, since it keeps the size of the pixel minimum, and the same reset pulse is applied to both transistors. However, using different Wells is still an option to modulate the inverter slope and thus its propagation delay in transient. All the possible configurations and the resulted VTC modulation are summarized in Table 5-3 below, which are also valid for the saturated load inverter.

Table 5-3: different diode configurations for light sensitive inverters (OBB: Optical Back Biasing)

DIODE CONFIGURATIONS				
NMOS	Forward OBB	Reverse OBB	Reverse OBB	Forward OBB
PMOS	Reverse OBB	Forward OBB	Forward OBB	Reverse OBB
Inverter VTC Light response	Shifts lower V_M	Shifts higher V_M	Sharper commutation	Slower commutation

After investigating the static response of the CMOS inverter, its transient response is now considered. The inverter output transient response is shown in Figure 5-13.a, where a light pulse of 0.1W/cm² is applied to the FDPix inverter with L=W=1µm for both transistors. The inverter output is initially at zero state (V_{IN}=0.48V > V_M), although the zero is not reached since the V_{IN} applied is lower than V_{DD}. The light pulse will shift the VTC towards higher V_M values, which in turn results in a V_{IN}<V_M, therefore, the output state changes from zero to one. In fact, the light pulse acts as a bias that changes the state of the inverter. This property is further exploited for logic design in section 5.4.

After the light is turned off, the V_{OUT} level exhibits a transient that depends on the response of the individual FDPix presented in Chapter 3. However, we can see from Figure 5-13 that the transient shape is different since both N and P-type FDPix are implemented. This is due to the very narrow operation region which results in "seeing" both transistors region of operation, linear and saturation, in the same manner as the inverter VTC shape. It is not observed in the saturated load inverter since the region of operation is larger. The reset of the light sensitive inverter is particularly efficient since the output can have only two states. Therefore, even if one of the transistors is not completely resetted, as soon as the output is lower than V_M, the inverter level switches. This is shown in Figure 5-13.b. where the inverter V_{OUT} after applying a reset pulse of 1.5V returns to state zero almost instantaneously.

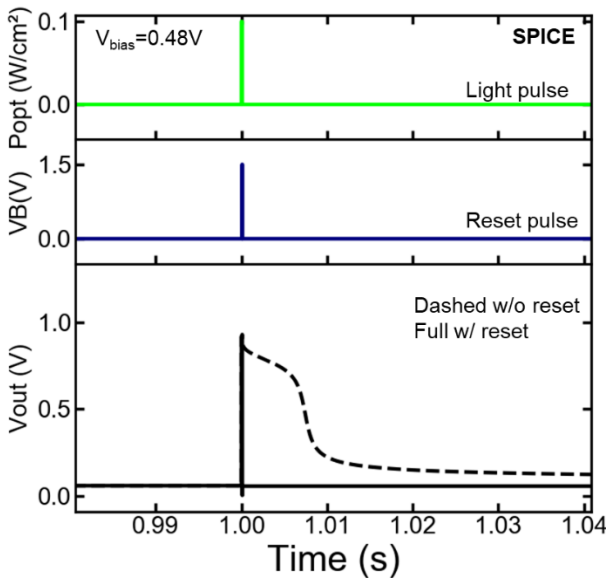


Figure 5-13: V_{OUT} transient response to a light pulse with and without a reset applied at light pulse falling edge

5.1.3.2 Static power consumption

As mentioned previously, the main advantage of the CMOS inverter is the very low static power consumption compared to the previous structure. In this case, one of the transistors is always OFF in standby, thus the current is the leakage current of either the PD when V_{IN} is zero, or PU when V_{IN} is one. This can be seen in Figure 5-14.a where the VTC at different V_{DD} is plotted for a GO1 type inverter simulated using SPICE. Increasing the supply voltage increases the peak current (the current at V_{IN} = V_M) as shown in Figure 5-13.b. which will increase the dynamic power consumption. Also, since we're using GO1, the supply voltage can be lowered to 0.4V here and the circuit will still be working which implies the feasibility of using the light sensitive CMOS inverter for ultra-low power applications, such as event-driven and smart sensors *[COTTINI 2011]*.

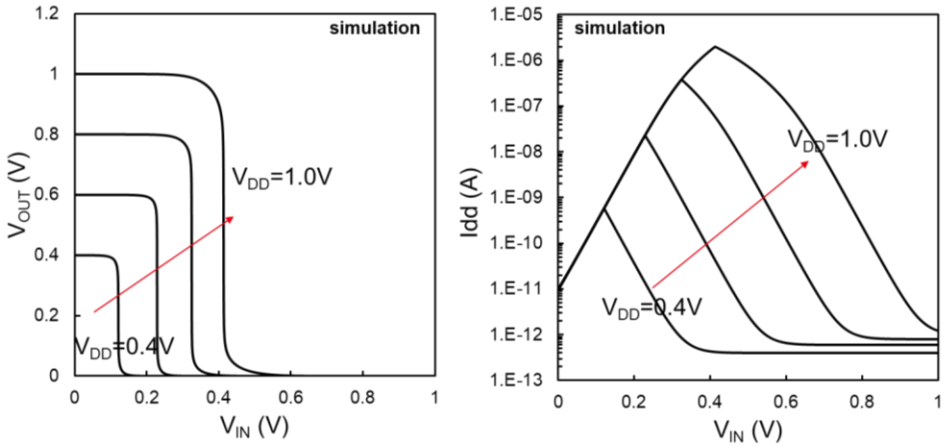


Figure 5-14: a) VTC of CMOS inverter at different V_{DD} b) supply current (y axis in log) at different V_{DD}

The static power consumption can be evaluated the same way as for the saturated load inverter using equation (5-9). Table 5-4 shows the simulated values for single stage light sensitive inverter. We can see that for the same transistor dimensions, the P_{static} of the CMOS inverter is in *pW* which is 6 decades less than the saturated load inverter.

Table 5-4: Static power consumption of CMOS inverter for different supply voltages

V_{DD} (V)	P_{static}(pW)	QVGA (nW)
0.4	2.2	168
0.6	3.3	253.44
0.8	4.4	337.92
1.0	5.5	422.4

Regarding total pixel size, we can expect the same footprint as the previous saturated load amplifier if not smaller, since the two gates are connected. Also as was the case for the analog, the fill factor (FF) is not reduced by adding a transistor since it is also sensitive to light. This sensor can be used for monochromatic detection application such as optical receiver for visible light communication *[ALMER 2015][CAILEAN 2015]*. In these applications, the light intensity is not measured, the change of state of the pixel indicates the presence or not of light. The efficient low power operation is a major advantage for this kind of technology and is one of the best assets of the CMOS FDPix inverter. Moreover, the inverter is the basic component of all digital circuits. In section 5.3, we present pixels design using the FDPix inverter for light detection in the time domain.

In the next section, we discuss the array implementation comparison for the proposed analog sensors.

5.1.4 Pixel array configuration

In image sensor architecture, the conversion of photo-electric conversion is performed by the pixel array. The size of the array in pixels determines the resolution of the sensor. For example, a QVGA format has a resolution of 320x240 pixels. One of the latest commercialized Canon DSLR features a full frame resolution of 50.6 MPix *[CANON]*. Recently, *[BIGPIXEL 2019]* reported the largest image resolution with 198 GPix. Evidently, a tradeoff must be made between the sensor total size and the resolution. However, the shrinking of the pixel size following CMOS technology scaling allowed the increase of the sensor resolution for the same total size, which is a critical demand for mobile phone market.

In Figure 5-15, a standard sensor architecture with the pixel array and the different readout blocks is presented. Depending on the pixel architecture, the sensor might require additional blocks specific to the pixel. The main components of an image sensor chip are:

- The pixel array that converts light into an electrical analog signal.
- The row and column decoders that allows random access of the pixels, which is one of the advantages of CMOS over CCD.
- The analog to digital converter (ADC) in this case located outside the pixel array. It can be implemented per column or global.
- Here simplified into the clock and control signal block, this bock also accounts for the signal generation blocks, the memory, the oscillator etc.
- Also, not shown here, in most standard image sensor a CDS block is implemented in the column readout to remove the FPN as mentioned in Chapter 1.

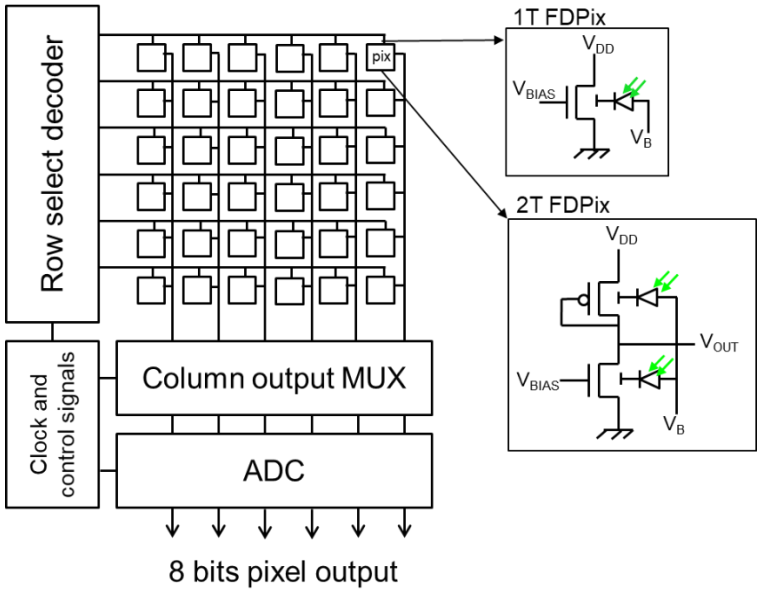


Figure 5-15: CIS architecture with the 1T FDPix or the 2T FDPix sensor presented as implemented pixels

To implement the FDPix, the standard architecture can be used. In the case of the 1T FDPix, since the readout signal is a current, a transimpedance amplifier is used in the column readout to convert it to voltage. For the 2T FDPix, where an analog voltage is readout as in standard APS, the standard CIS architecture can be used. Also, since the reset in our case can be implemented simultaneously to all pixels without going through the MUX, a global shutter operation by adding a memory node per pixel can be envisaged *[MEYNANTS 2014]*. Otherwise, rolling shutter readout is implemented which requires the isolation of each row, and applying a reset on an entire row at a time.

The linear-log response of the FDPix doesn't change the main blocks of the sensor. However, it will influence the ADC scheme, where an adaptive ADC or logarithmic ADC, with higher resolution in the linear regime and lower resolution in the logarithmic regime, might be necessary *[BERMAK 2006]*. This is a preferable approach to use the 8bit-10bit encoding accuracy while maintaining high image quality. If the whole linear-log response was to be sampled, the ADC resolution will need to be higher than 10bit which then will demand more memory. Considering the GO2 2T saturated load inverter shown in Figure 5-3.b operating in logarithmic mode, the total voltage swing was 200mV (although saturation is not reached so it will be higher). Thus, using an 8-bit resolution ADC, the Least Significant Bit (LSB) which represents the minimum voltage change needed for the counter to increment the digital code, is equal to 0.781mV. This calculation doesn't account for noise, but it gives an idea of the accuracy required.

5.1.5 Conclusion on analog pixels

We discussed in this section the different possible implementations of the FDPix in the analog domain. It can be used as a current mode 1T pixel, a voltage mode 2T pixel, or a logic gate. The most important feature of these designs comes from the versality of integration and bias possibilities that were summarized in Table 5-3. What also can be used to tune the response is the back gate of the transistors. This back gate can be common to both or isolated to allow independent bias on the N and PMOS. However, this does come with an area penalty as previously mentioned. The simplicity of the proposed circuits allows their implementation using standard readout circuits and commonly used

sensor blocks in standard image sensors. Size and power consumption are the main advantages. Using advanced node technology allows the use of lower supply voltage, and small transistor dimensions coupled with low transistor count per pixel, results in extremely small pixel area, while maintaining a good FF.

The next section will discuss another type of FDPix-based architecture, for time domain imaging.

5.3. Time domain pixels

In standard CIS, the analog output voltage is readout using column amplifiers, and the signal is then converted to a digital signal using ADCs. We discussed in Chapter 1 the advantages of integrating the ADC per pixel, which results in the so-called Digital Pixel Sensor (DPS). Due to higher noise immunity which characterizes digital signals, the DPS sensors have a higher SNR. Also, they exhibit a higher DR, since they are no longer limited by the supply voltage, and provide high image quality *[SKORKA 2014]*. However, most DPS designs increases the number of transistor per pixel to more than 30T/pix *[CHEN 2011]*. Therefore, this technology has not been used in consumer electronics market where the total chip size must be maintained as small as possible while ensuring high image quality. However, it did find applications in the low-volume market such medical, industrial, and surveillance imaging.

Most DPS designs are based on Pulse Modulation (PM) schemes, whether it is Pulse Width Modulation (PWM), or Pulse Frequency Modulation (PFM). Both techniques were widely implemented as the first step of the ADC conversion. In this section, we present an FDPix design where the signal is pre-processed or pre-digitized locally in the pixel. It is based on the use of the light sensitive CMOS inverter presented in section 5.1.2. By comparing the signal locally with a reference one, the output of the pixel is converted to time domain variations due to the inverter propagation delay dependence on light intensity. This pixel performs pulse width modulation (PWM) using light intensity variations.

5.3.1. Pulse Width Modulation (PWM) principle

PWM is a technique used primarily in power supply control, since the average of the signal depends on the Duty Cycle (DCL) of the pulse signal. The DCL is the percentage of the signal period where the level is high. Changing the DCL varies the average output signal measured (Figure 5-16). It is also a modulation technique used in telecommunication *[SUH 1987]*. The advantage of this technique is the power consumption since it consumes power only at the transition from high to low or low to high. Also, there are only two voltage levels, thus the signal is immune to supply fluctuation or losses and distortion of the signal amplitude.

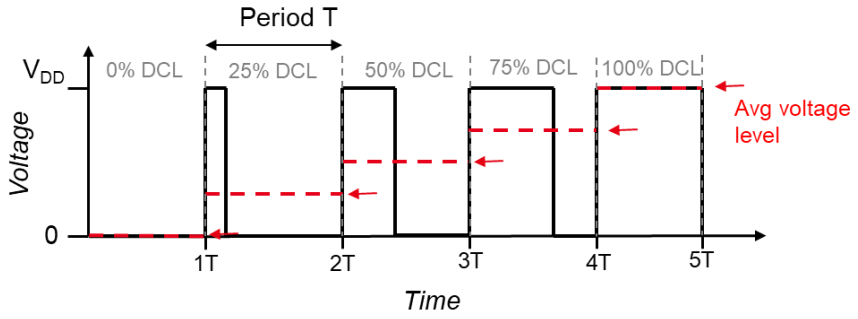


Figure 5-16: Pulse width modulation principle

Previous work used PWM for DPS design *[CHEN 2015][CHUNG 2013][KAGAWA 2007][KITCHEN 2004]*. The analog signal is compared to a reference, since the reference signal is reached slower or faster depending on the photocurrent generated, the output pulse width varies as a function of light intensity. The counter that finally samples the PWM signal is either located in the pixel, or outside, in which case it is either implemented per column or globally to the whole array which reduces power consumption *[KAGAWA 2007]*.

5.3.2. The PWM-based FDPix sensor

The proposed Light sensitive PWM circuit is presented in Figure 5-17. It is composed of two inverters and a comparator. One of the inverters is an FDPix light sensitive inverter (INV_L), the other is a standard FDSOI inverter (INV_D). The input signal is common, and the outputs are connected to the input of the comparator. Depending on the type of comparator and input waveform, the output signal will differ. The idea is to obtain a square wave with a DCL that varies with light intensity. This modulation is due to the difference in V_M thus in propagation delay of the two input inverters.

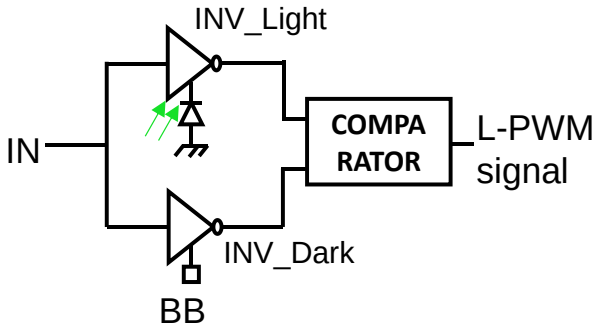
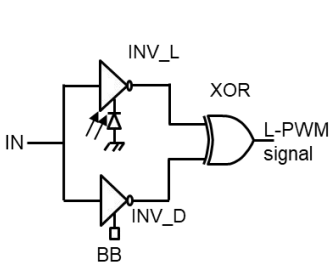


Figure 5-17: FDPix based DPS

Our first design uses an exclusive-OR (XOR) gate as a comparator. The circuit schematic and the layout view of this configuration are shown in Figure 5-18. Since the XOR is not sensitive to light, the minimum dimensions are used, and it is implemented using GO2 devices for the supply voltage to be common to all the circuit. The advantage of using a XOR as a comparator is that it guaranties an output whether the V_M of the inverters are matched/balanced or not, since it outputs a ONE whenever the input signals are different. Thus, if the V_M are exactly matched, the output should be zero, if not, an initial pulse is measured at the output, this can be seen in the truth table shown in Figure 5-18. Moreover, the number of transistors of this design is 12T/pixel, which is lower than conventional DPS *[CHEN 2011]*.

This number can be reduced by sharing the comparator between multiple pixels, as will be discussed at the end of this section. Since the standard inverter is processed on a different Well, and both inverters have the same dimensions, the nominal V_{Ts} of its PU and PD will not match the ones of the FDPix inverter, which implies that the V_M will be mismatched if the default process is used. Some specifications regarding the design must be mentioned:

- The distance between the outputs of the FDPix inverter and the standard inverter to the input of the XOR must be identical to ensure that any variation in the output pulse is due to light variation and not different RC losses.
- As for the analog pixel, we wanted to ensure to obtain a high output signal to validate the design concept. Therefore, the Sa/Sb are larger, and silicide block layers are used, which increases the transmission of light through the S/D. Nevertheless, these dimensions can be drawn using minimum dimension.
- The design is not optimized layout-wise.



XOR Truth table

INV_L	*INV_D*	*OUT*
0	0	0
0	1	1
1	0	1
1	1	0

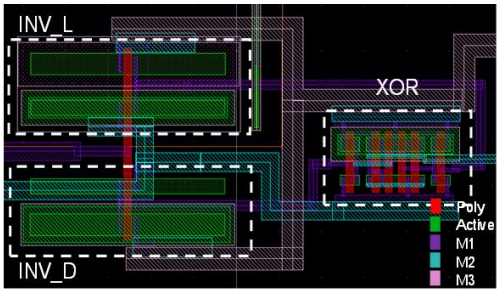


Figure 5-18: PWM-based FDPix sensor a) schematic b) layout

Figure 5-19 demonstrates the static opto-electrical characteristics from hardware measurements showing the output of both inverters and the XOR vs input voltage sweep. The inverters have the same aspect ratio, with L=330nm and Wp/Wn of 1.56/1.1µm. The junction of the light sensitive inverter is similar to the one showed in Figure 5-2, thus it's an NP junction between N-Well and P-substrate. The sweep in input signal is applied commonly to both inverters, and both inverters and XOR bulk are at GND. The supply voltage used is 1.4V, and the optical power density of a Xenon wideband source used is 1e-2 W/cm². The pulse output width is reduced by ~53mV under light illumination, which is the same as the V_M light induced shift of the light sensitive inverter.

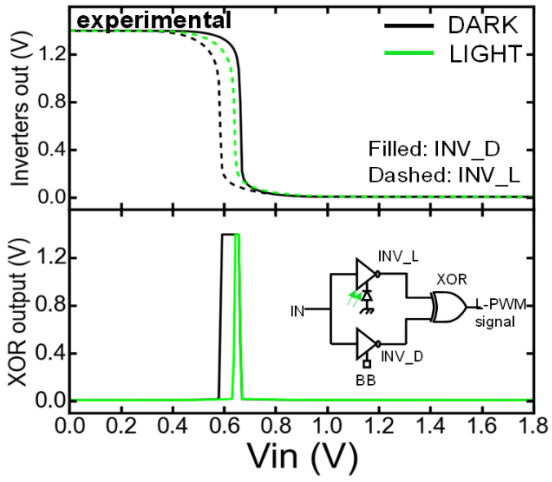


Figure 5-19: PWM-based FDPix output of each inverter and XOR for NP oriented junction

We also performed the test using a different photodiode orientation for the light sensitive inverter. In this case the junction is PN oriented located between the P-Well and the Deep-NWell, leaving the PWell floating and biasing the DNW at GND (Figure 5-20.a). It results in the complementary effect where the shift under illumination is measured in the opposite direction as illustrated in Figure 5-20.b. This is due to the VTC of the FDPix inverter shift to lower V_M as opposed to higher V_M for NP junction as previously shown. This means that if both inverters are sensitive to light, and their junctions are opposite polarity, the V_M shift observed on the output pulse can be doubled. More configurations of the PWM FDPix are presented in appendix C.

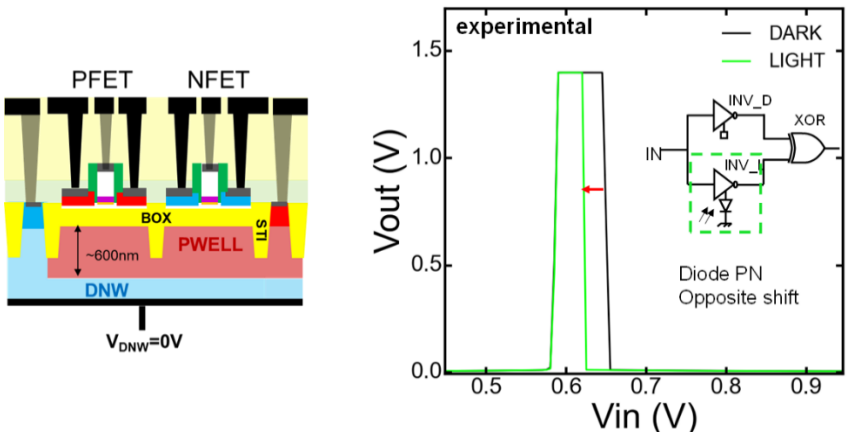


Figure 5-20: LPWM FDPix with PN oriented junction a) side view b) output of the XOR

As discussed, and also shown in Figure 5-11, the VTC of a single inverter is modulated by applying a back bias. Since the wells of the two inverters in the PWM FDPix are isolated, a back bias can be applied on the non-sensitive inverter to calibrate or tune the initial output signal. As presented in Figure 5-21.a., a positive or negative back bias changes the width of the initial pulse output in dark condition by shifting the non-sensitive inverter VTC. Thus, the back bias allows choosing whether to measure an increase or decrease of the pulse width, i.e. DCL, with light illumination. This is shown in Figure 5-21.b. where the pulse width in mV is plotted vs applied back bias V_B. We can also see that the amplitude of shift due to light illumination is not affected by the bias which indicates good isolation between the Well of the two inverters.

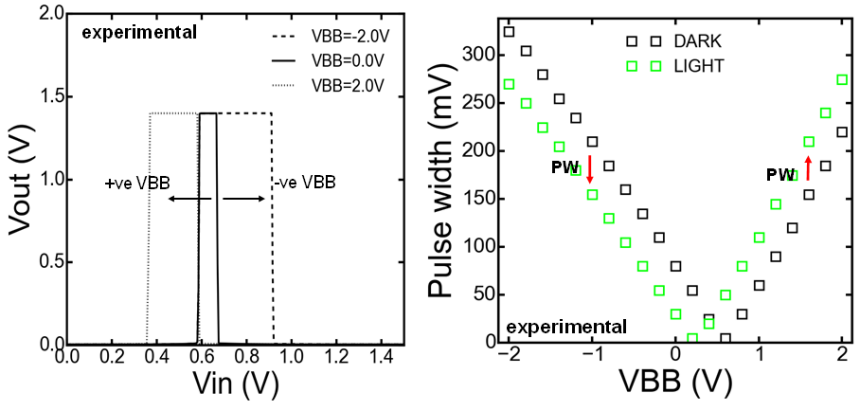


Figure 5-21: a) effect of back bias on XOR output signal width b) output width vs applied VB

This property of back biasing can also be used to extend the response of the sensor. In Figure 5-19 if the light sensitive inverter V_M shift increases beyond the non-sensitive inverter V_M, the pulse width modulation, i.e. DCL modulation, changes polarity which is not desirable since it renders the readout more complex. To avoid it, the initial V_M can be selected to allow maximum range, but more importantly, the back bias can be used to dynamically tune the V_M. This is even more important if other gates are used as comparators.

Figure 5-22.a and b show the schematic and layout for the case of a NAND gate used as a comparator, reducing the number of transistors per pixel to 8T/pixel vs 12T/pixel using an XOR gate. The inverter dimensions are the same as previously shown (L=330nm and Wp/Wn of 1.56/1.1µm), however the Sa/Sb in this case are dissymmetrical for layout purposes. All the polarizations are the same as the one used for the XOR case. Figure 5-22.c. shows the output results of both inverters and the NAND, where we can see a shift of the rising edge. When using a NAND gate as a comparator, if the inverters are unbalanced (V_M not matched), we may not obtain any variation at the output pulse width. For example, in the results shown in Figure 5-22.c., if the V_M of the FDPix inverter is higher than the V_M of the standard inverter, no light shift can be measured at the output. This will also result in limited DR since higher intensities may shift the V_M to higher values beyond the standard inverter V_M. However, this is easily corrected, as was the case for the XOR, by applying a back bias to tune the inverters V_M allowing a higher margin. Also, the same complimentary effect as measured for the XOR circuit when using a different diode orientation is expected.

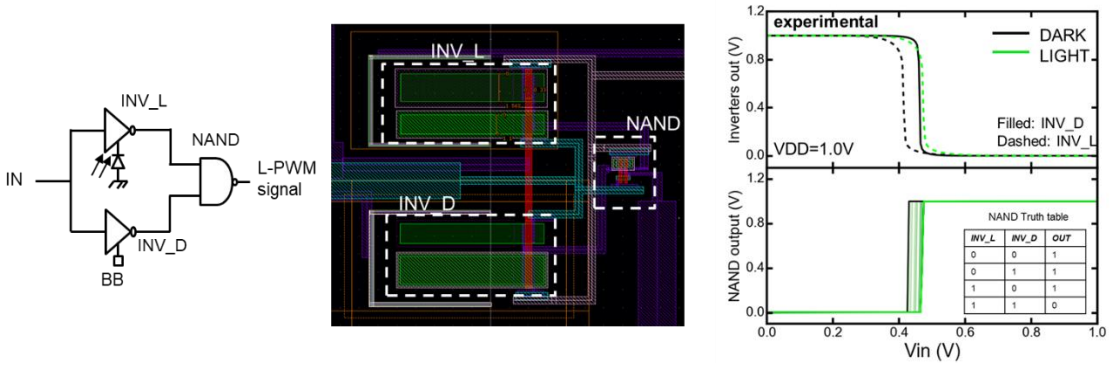


Figure 5-22: LPWM FDPix using NAND gate a) schematic b) layout c) output of each inverter and NAND gate for NP oriented junction

Figure 5-23 shows the FDPix inverter light induced V_M shift vs Popt, the XOR delta pulse width, and the NAND rising edge shift, when a V_{DD} of 1V is applied. We can see the agreement between the three until Popt reaches ~1e-2 W/cm², at this point both inverters are matched (identical V_M). Passed that point the XOR response changes polarity as previously discussed, and the NAND saturates. By applying a back bias, both the XOR and NAND output shift would have followed the inverter curve.

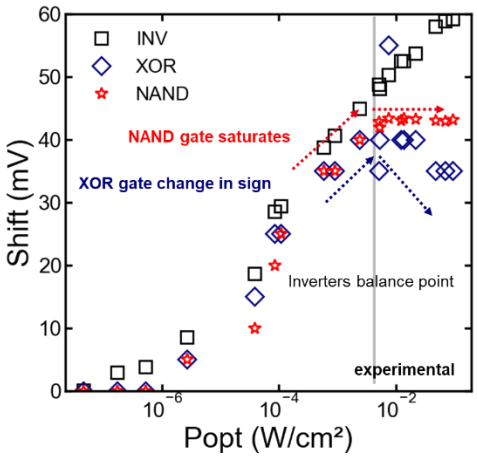


Figure 5-23: Light induced Shift for the single inverter, the XOR output, and the NAND output

Now the transient response is evaluated. The difference in V_M between the inverters is going to generate a change in the transition delay, t_{pHL} and t_{pLH}. This difference can be modeled using equations (5-16). We tested experimentally the response by applying a periodic triangular wave (V_{PP}=1.4V, $t_{rise/fall}$=2ms) at the input port and monitored the output signal under different light intensities. This is performed for the two circuits discussed with the XOR and NAND as comparators, and the results for the NAND case are shown in Figure 5-24.

As was discussed in the static measurements, when comparing the two inverters output in dark condition, the two V_M are unbalanced. Therefore, the two inverters have an initial difference in propagation delay. When the circuit is under illumination, the light will increase the V_M of the light sensitive inverter. This means that the V_{TN} is increased and the V_{TP} is decreased. As demonstrated in equation (5-16), the commutation delay depends on the V_T. Therefore, t_{pLH} that depends on V_{TN} will be longer, while t_{pHL} that depends on V_{TP} will be shorter. The change in Pulse Width (PW) of the signal can be expressed as:

$$\Delta PW = \Delta t_{pHL} + \Delta t_{pLH} \tag{5-17}$$

This can be seen in the output signal shown in Figure 5-24.a where the NAND output pulse rising edge commutes later and the falling edge earlier when increasing the light intensity. This results in the modulation of the signal DCL with light. From (5-17) and Figure 5-24.a, we can see that to measure a change in pulse width, i.e. DCL, the change in t_{pHL} and t_{pLH} must be opposite, otherwise they cancel each other out. This imposes the V_T shift to be opposite for the N-type and P-type FDPix, which in turns means they must be processed on a common well. The other case where the change in V_T is similar for both transistors, will result in changing t_P (change of the VTC slope). This property was investigated for implementing Pulse Frequency Modulation (PFM) sensors using light sensitive ring oscillators but is not discussed here.

Figure 5-24.b shows the NAND output change in pulse width plotted vs Popt for different V_{DD}. We can see that increasing the V_{DD} increases the DR since the saturation occur for higher intensities. This saturation as previously mentioned is due to the V_M of the light sensitive inverter becoming higher than the reference inverter V_M, so the sensor

is in fact not saturated, but the range of operation is lower when using a low V_{DD}. Again, this is easily avoided by choosing appropriate V_M for the standard inverter that will allow maximum swing, or dynamically tune it by applying a back bias.

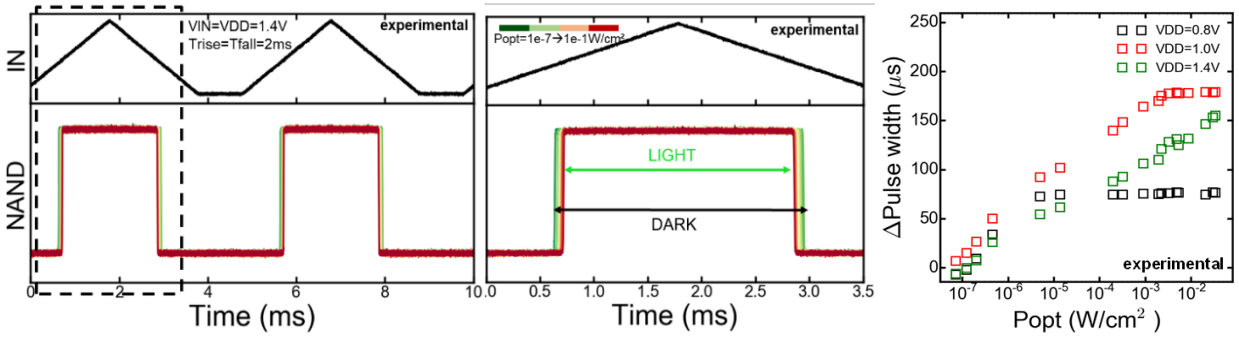


Figure 5-24: a) transient characterization of the DPS FDPix using a NAND gate as comparator b) change in PW vs Popt at different V_{DD} for the NAND gate case

The input signal used was a triangular wave were the rising and falling edge duration was 2ms. The resolution of the light induced PWM will directly depend on this edge duration. Meaning that for the same LIVS, a higher ΔPW can be obtained using a longer rise/fall time. Therefore, using a high rise/fall time for the input signal reduces the constraint on the sampling rate to encode the signal accurately. However, this comes at the cost of power consumption. The input signal can be optimized by windowing the voltage swing. Since the region of interest is the transition region, the input signal swing can be limited to a lower and higher voltage values that ensure a high enough range for transition.

The static power consumption can be estimated based on the measured I_{leak} for the single inverter. For the NAND case, the static power consumption is evaluated by considering the inverters connected to the supply and estimating the total I_{leak} (I_{leak_tot}) as:

$$I_{leak_{tot}} = \left(I_{leak_{inv}} * 2\right) + I_{leak_{NAND}} \tag{5-18}$$

For the XOR gate, $2*I_{leakinv}$ must be added to the previous equation. The estimated P_{static}, considering leakage current of 1.1pA, are shown in Table 5-5 for both type of comparators, and for single pixel and a QVGA array format (320*240).

Table 5-5: static and dynamic power consumption of PWM FDPix sensor for different supply voltages

V_{DD} (V)	P_{static} NAND (pW)	P_{static} XOR (pW)	QVGA (nW) NAND	QVGA (nW) XOR
1.0	4.4	6.6	337.92	506.88
1.4	6.16	9.24	473.008	709.632
1.8	7.92	11.88	608.256	912.384

Since the XOR contains two extra inverters vs the NAND, the total P_{static} is slightly higher. By using GO1 devices, the supply voltage can be decreased which reduces the static power consumption.

Regarding pixel size, the fill factor is reduced in this configuration since only 2 transistors of the 8 are sensitive to light. The area of this inverter can be bigger than the others by changing the Sa/Sb. Also, both inverters can be light sensitive to obtain a gain in the output as previously discussed. Different options to optimize the pixel size are available:

1) *Using minimum dimensions:*

   Since advanced node technology is implemented, the transistor minimum gate length can be as low as 30nm (GO1). The only layout constraint is the difference of well between the light sensitive inverter and the non-sensitive one. Depending on the diode orientation and configuration of the well for both inverters, an isolation might be needed to allow back biasing of the non-sensitive inverter without affecting the sensitive one. This can be achieved by using a Deep NWell which consumes layout area. Also, for the V_{DD} to be common to the inverters and comparators, it's better to design using one gate oxide type, however it is not an obligation, the comparators for example can be implemented with thinner oxides.

2) *3D stack:*

   As presented in Chapter 1, today's industry shifted to the 3D stack process integration which allows the integration of the CMOS processing part on top of the pixel. The advantage being the possibility of using more advanced technology nodes for the processing circuit, and adding more functionalities without deteriorating the FF. Today, well controlled processes are available since most high-end sensors use 3D stack *[YOLE DEVELOPPEMENT 2018B]*.

   Therefore, the possibility of stacking the comparator level on top of the inverters presents itself as the best solution.

3) *Sharing component between pixels:*

   The possibility of sharing the comparator between multiple pixels should also be considered. Early work on reducing pixel size demonstrate pixels where the readout transistors are shared between four adjacent pixels, reducing the effective pixel size, as was presented in Chapter 1. The non-sensitive inverter can also be shared, which reduces considerably the effective number of transistors per pixel.

Therefore, multiple solutions are available to optimize the size of the pixel without deteriorating the performance. Ultimately, the size will be depending on the comparator used and thus on the application.

The main advantages of the PWM is the local comparison of the signals, which leads to reduced process variability related errors. In addition, by representing the LIVS in time domain, the signal is immune to voltage level variations achieving high Signal to Noise Ratio (SNR), high DR, and low power pixel sensor. More importantly it opens perspective on using the FDPix inverter to design low power, smart pixel sensors.

5.3.3. Pixel array configuration

To implement the PWM-based FDPix in a sensor array, the main decision is to where should the Time to Digital Converter (TDC) be located, which can be a simple counter. The two options are: per pixel, which is generally the case in standard DPS for the output of the pixel to be purely digital, or per column which will avoid the addition of extra transistors per pixel and lower the power consumption as pointed out in *[KAGAWA 2007]*. Therefore, the main difference with the analog sensor architecture is the absence of the ADC block that might be replaced by the TDC.

Depending on the comparator used, the output signal will change and thus, the readout technique must be adapted. For example, the XOR output will require edge-to-edge detection readout while the NAND gate output can be sampled

with a counter. The sampling rate which determines the bandwidth, should be high enough to ensure high temporal resolution by discriminating the optical power density measurements. The oscillation frequency of a 101-stage ring oscillator in FDSOI 28nm technology is ~500MHz, which means that a sampling rate as high as 2ns can be implemented. After that comes the resolution of the conversion. Considering the whole ΔPW_{max} range to be 150µs, if an 8-bit scheme is used, the LSB will be equal to 585ns, and for 10-bit resolution, the LSB is 146ns. Also, since the response is logarithmic as previously discussed for the analog pixels, an adaptive conversion scheme must be used, such as logarithmic ADC *[GUILHERME 2003][PAGIN 2017]*. In general way of speaking, the PWM-based FDPix signal must be optimized to ensure the correct output signal encoding while limiting the power consumption.

5.4. Analog and PWM-based pixel summary

A summary of the analog and PWM-based pixel is presented in Table 5-6 below. Since both these pixels architecture would address different applications, a direct comparison is not justified. Regarding size, the 2T pixel presents the best tradeoff, keeping a maximum FF. They also generate a gain on the LIVS that can be tuned by changing the device critical dimensions. However, the power consumption is still a negative point although as previously mentioned it can be optimized by slightly modifying the design.

Concerning the PWM-based pixels, their local comparison, and time domain readout are expected to lower the noise due to supply voltage fluctuation. The tunability of these designs using the back gate presents one of its major assets. Also, the multiple implementation option available can address different range of applications in the time domain imaging field, such as event-driven and smart pixel sensors as mentioned in Chapter 1.

Both implementations kept the inherited high DR of 6-7 decades. The transient response with reset was unfortunately not tested, but we can expect the same linear-log response as the 1T FDPix, since the presented architecture had linear dependence on LIVS.

Table 5-6: Summary of FDPix implementations

	Circuit comp.	**#of T/pixel**	**Readout signal**	**Gain**	**Tunability using VBB**	**Power consumption**
FDPix	N-or PMOS transistor	1	Current	x	+	x
Analog	Sat. load inverter	2	Voltage	++	+	--
PWM	2 INV+XOR	12	Rising edge-to-Rising edge	x	++	++
	2 INV+NAND	8	Pulse width	x	++	+++

5.5. Perspectives towards light sensitive logic

We previously presented the sensitivity to light of the basic building block of many logic circuits and all logic gates, the CMOS inverter. As was shown in Figure 5-12, the VTC of the inverter shifts with light intensity when implemented using FDPix. This property has been further used to design PWM based FDPix sensor as was presented in the previous section. Since most logic gates are based on PMOS PU and NMOS PD logic, virtually any logic/digital/analog circuit can be made sensitive to light, which opens multiple doors in the field of reprogrammable logic and light detectors. In the following sections we will present example of digital circuits building blocks when implemented using FDPix.

5.5.1. Light sensitive SRAM

A good example of logic sensitive to light starts with the 6transistor Static Random Access Memory (6T SRAM). A 6T SRAM cell consist in two cross-coupled inverters and two access transistors as shown in Figure 5-25.a. The gate of the access transistors is connected to the WordLine (WL) which allows the selection of the cell in the array. Their drain is connected to the BitLine (BL), either the true (BLT) or false (BLF). Depending on the bias applied on the BLF, BLT and WL, a specific operation is performed, namely Read, Write, or Erase of the cell. The cross-coupled connection of the inverters provides a positive feedback loop that results in the bi-stable characteristic of the SRAM. The VTC of the SRAM (butterfly curve) as shown in Figure 5-25.b, is composed of the two inverters' individual VTCs. The two stable points of the SRAM operation are A and B, which corresponds to a one or a zero stored in the cell. One of the most important figures of merit of the SRAM is the Static Noise Margin (SNM). As shown in Figure 5-25.b, it is defined as the square side nested in the VTC and is given in Volts. If a DC noise is larger than the SNM, the SRAM becomes unstable and the data is lost.

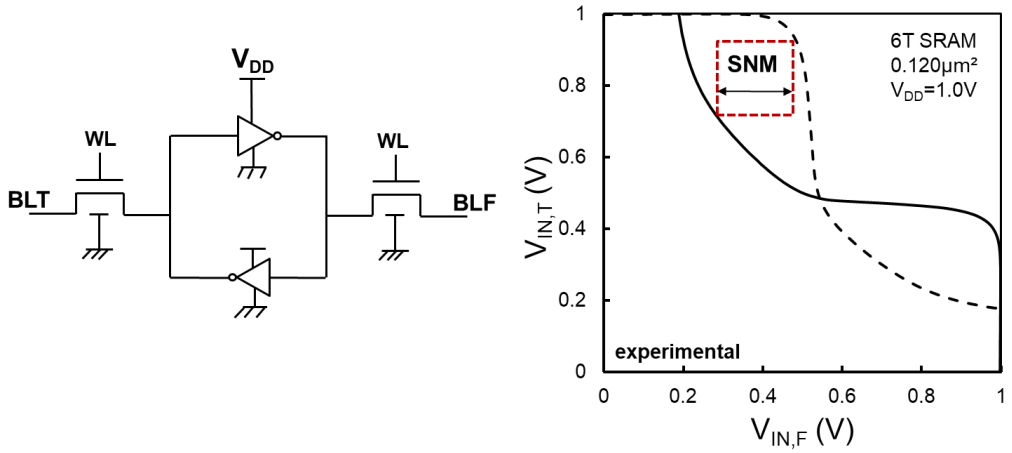


Figure 5-25: 6T SRAM a) schematic b) butterfly curve

When implementing the SRAM using FDPix inverters, it becomes sensitive to light. A preliminary experimental demonstration is presented in Figure 5-26, where photodiodes were co-integrated under FDSOI SRAM cells smaller than 0.2µm² and characterized under dark and illumination. A clear change in the SNM is observed when the SRAM is front side illuminated (Figure 5-26) due to the shift of the inverters VTC with light. As expected, the SNM is kept unchanged when a reference SRAM with no diode is illuminated. This result suggests that memory effects controlled by photons are possible on very small footprints. The observed photo-induced effect can be strongly increased; we performed our experiments on GO1 devices (small expected LIVS) and FSI is used. An optimized integration can be readily envisaged, using BSI and GO2 devices.

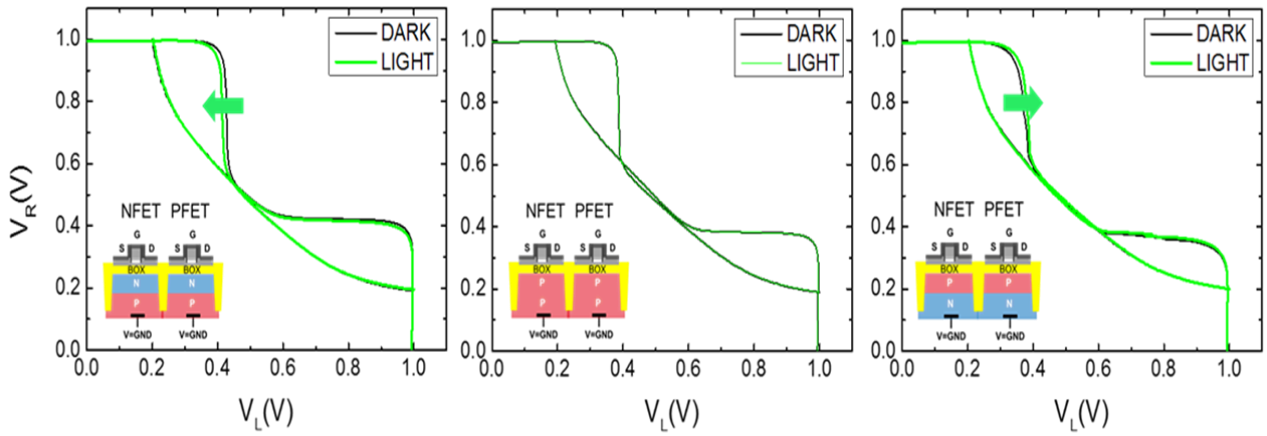


Figure 5-26: SRAM sensitive to light implemented using FDPix invertors

5.5.2. Light sensitive gates

So far, the CMOS inverter logic was discussed. In this section we investigate pass-transistor logic and D-latch (i.e. flipflop). These two devices are building blocks in combinational and sequential logic, as they are used in Multiplexers (MUXs) and registers. These circuit depend on a clock or control signal. The idea is to make that signal light dependent so that the functionality is triggered only under illumination using a light sensitive inverter.

Passgate logic is based on using the transistors as switches rather than to connect the supply or GND as CMOS inverters. The applied signal controls both the V_{GS} and V_{DS} of the transistors. It was developed to reduce the number of transistors in logic gates. Now it is mainly used in MUX and latches. A simple CMOS passgate is shown in Figure 5-27.a, in which a light sensitive inverter biased close to its V_M is buffering the control signal. When a light is applied, the inverter VTC shifts to higher V_M which switches the output level. The SPICE simulations results are shown in Figure 5-27.b. where we can see that the signal is transferred ("passed") only when the light is ON. Therefore, just by adding an inverter, the passgate function can be controlled with light.

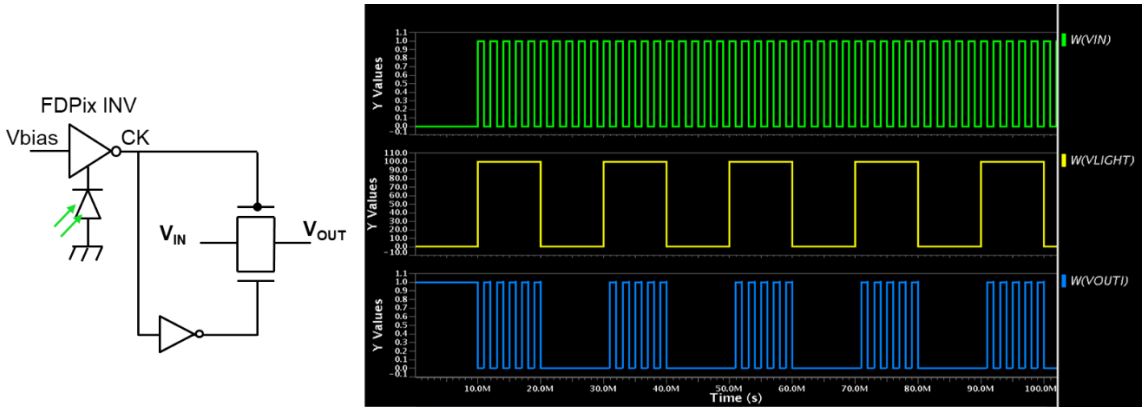
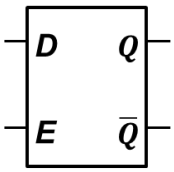


Figure 5-27: light controllable passgate with schematic and SPICE simulation results

Therefore, since most logic circuit depends on a clock signal, by using a light sensitive inverter, a light pulse can be used to switch the circuit. Another example is given below with the D-latch or flip-flop.

A D-latch is a sequential logic circuit component that reproduces the input signal as a function of the enable signal state and maintain the previous value as shown in Figure 5-28. Thus, it is used as a memory point in sequential logic. Latches are level sensitive, while flip-flops are edge triggered. An example of a D-latch circuit is shown in Figure 5-29.a. where two passgates and two CMOS inverters are used. D-latches are used as buffers and flip-flop are the main component of registers and are used in FPGA.



E	*D*	*Q*	$\bar{Q}$	*comment*
0	X	Q_{old}	$\bar{Q}_{old}$	No change
1	0	0	1	Reset
1	1	1	0	Set

Figure 5-28: D-latch symbol and truth table

We propose a design where the enable signal is controlled with a light pulse in a similar manner as presented previously for the passgate. By using a light sensitive inverter biased around its V_M, a light pulse that shifts the VTC and thus the output level of the inverter can be used to either latch the value or store it by controlling the enable signal. SPICE simulation was used to evaluate the functionality of the circuit. The dimensions used are L=W=1µm, for GO2 devices with NP oriented junction. The results are shown in Figure 5-29.b, where we can see that the output level changes only when 0.1W/cm² light intensity is applied, and the Q holds its last value when the light is off.

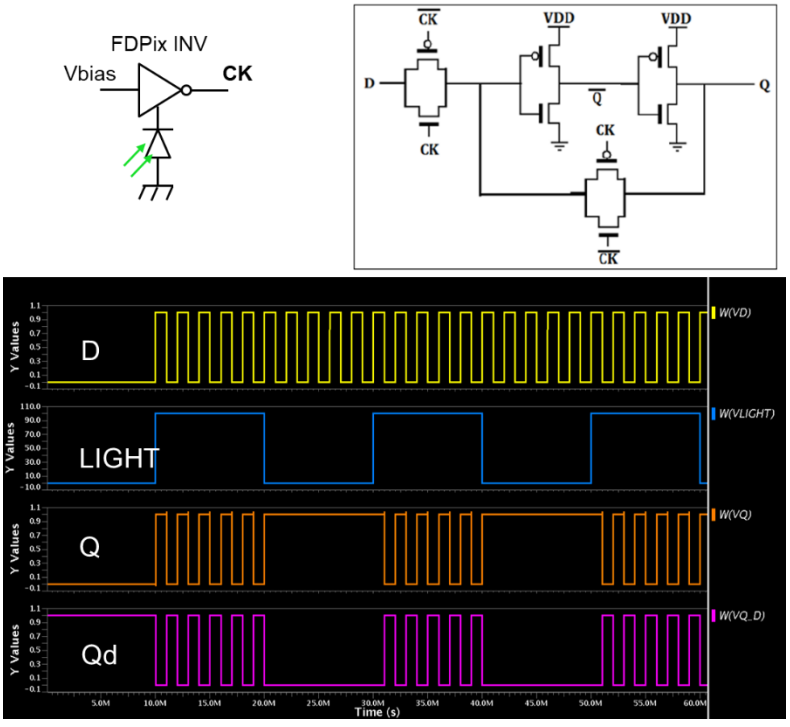


Figure 5-29: Light controllable D-latch with schematic and SPICE simulation results

The previous circuits can be implemented on very small footprint. As they are building blocks for digital design, the possibility of altering the circuit functionality with light can find applications is various domains. This property can be

used at the interface of photonic and electronic circuits with optical interconnects, and optical communication receivers where the light intensity is not measured. Other applications presented in Chapter 1 such as LIDAR, and event-based smart sensors can be envisaged using the circuits presented in this chapter where the detection in time domain and intrinsic logarithmic response are key properties. Depending on the application, some specific figure of merits must be optimized. We demonstrated in this last section the versatility of using the FDPix for both analog and digital applications, and perspectives of using this advanced node technology for future smart sensor applications.

5.6. Chapter five summary

In this chapter we presented different circuit design architectures that utilizes the FDPix as main component to achieve light detection. All the presented designs were based on the complementarity property of the FDPix and present different options of output signal, in analog and time domain. The main points are summarized below:

- An analog design was presented where the variation of V_T due to light are converted to output voltage variations.
- The pixel contains two transistors (2T) and is based on the saturated load inverter amplifier design.
- A gain is obtained on the output LIVS when the same diode orientation is implemented under the P and NMOS transistors.
- The CMOS inverter is made sensitive to light by using FDPix as PU and PD transistors.
- The VTC of the inverter shifts proportionally to the LIVS of the PU and PD transistors, which in turn modulates the V_M and propagation delay of the inverter.
- Depending on the diode orientation and Well sharing, the VTC and propagation delay can be modulated in four different ways, allowing multiple integration options depending on application.
- PWM-based FDPix was designed using the light sensitive CMOS inverter, where the output variation is in time domain, to pre-digitize the signal prior to readout.
- Due to local comparison and time domain operation, the output signal is immune to supply voltage fluctuations and process variability.
- All the circuits designed were validated using SPICE simulation and electro-optical characterization.
- Based on the light sensitive inverter, SRAM cells, passgate, and sequential logic components are made sensitive to light which opens perspectives towards photon driven memory and reprogrammable logic.

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CHAPTER SIX

Chapter 6 : Conclusion and perspectives

6.1. FDPix characteristics summary

The thesis work was on the study of a new light sensor, the FDPix. During this thesis, the single device which consist of an FDSOI transistor co-integrated with a photodiode underneath the Buried Oxide (BOX) was investigated. The key figure of merit of the FDPix was defined as the Light induced V_T shift (LIVS). This LIVS results from the ground plane (GP) potential variation due to photogenerated carrier in the substrate. No electrical connection exists between the sensing transistor and the photodiode since they are isolated by the BOX. The photosensitivity of the transistor is a result of a capacitive coupling between the front and back channel interfaces that modifies the V_T. This property is called the back bias (BB) and is a major advantage of the FDSOI technology. Therefore, in the FDPix, the BB is an optical BB (OBB).

First, the device was investigated in the DC domain by means of TCAD simulation and opto-electrical characterization. The BF which quantifies the capacitive coupling, is identified as the determining parameter that affect the conversion gain and sensitivity of the pixel. Also, the DC response of the FDPix (LIVS vs Popt) is logarithmic due to the operation of the diode in photovoltaic mode. The logarithmic response results in a high intrinsic DR of 120-130dB.

We further explored the transient response of the sensor. Due to the floating nature of the sensing node, a reset scheme to evacuate the accumulated charges and start a new acquisition was developed. We developed a compact model to describe the DC and transient behavior of the sensor and further investigate it using SPICE simulation. An efficient reset scheme was developed and validated using electrical characterization. it is based on the use of the back gate to avoid the need of an extra transistor/pixel, and thus keep the size minimum. When the device is readout during transient, the response is linear due to the photodiode initially operating in photoconductive mode. Therefore, the FDPix has two responses, linear at low light intensities when the transient is long, and logarithmic at higher intensities when the device reaches steady state at a given V_{OC}. The transition and DR of both regions is controlled via the integration time. This double response allows the increase of sensitivity at low light illumination while maintaining the high DR, without the need of DR extension techniques that adds transistors per pixel. Finally, we demonstrated using SPICE and opto-electrical characterization that the 1T FDPix can effectively be used as a light sensor by reproducing a pattern of light intensity variations.

After studying the device behavior, we investigated the different factors that need to be optimized to improve its response in both domains. Both the impact of the photodiode and transistor on FDPix performance were investigated. The leakage current of the diode appeared to be an important factor in DC and transient and demonstrated that the temperature had the same effect as conventional sensor where the dark current increases with temperature, and thus lowers the $LIVS_{SS}$. We also demonstrated that using a PiN diode will increase the sensitivity of the device in linear due to a lower capacitance, however at the expense of lower $LIVS_{SS}$. Changing the junction profile modulates its capacitance and thus its full well capacity (FWC), which in turn affect directly the DR of each region of operation.

The impact of bias and timing parameters, on which depends both regions sensitivity and DR, was also demonstrated. After that the optical properties of the FDPix were discussed and alternative integration solution were proposed to increase the sensitivity. Considering the use of front side illumination (FSI), the metal layers should be optimized and the S/D unsilicided. Since the photodiode is naturally underneath the transistor without using 3D integration processes, and that the gate is what primarily shadows the structure when FSI is used, BSI should be privileged to increase the sensitivity and quantum efficiency. BSI was proven to improve the detection using TCAD simulation. We also propose a BSI integration flow, highlighting the key factors to be carefully controlled during the process of back thinning and bonding, such as the availability of an etch stop layer. We also demonstrated how by shaping the profile of the junction around the gate area the low light sensitivity can be improved by driving the photogenerated charges towards the coupling area.

In the final chapter we discussed a more circuit approach of the study. one of the most important properties of the FDPix as mentioned several times in the manuscript, is the complementarity between the N- and P-type FDPix, and NP vs PN oriented diode. This give rise to multiple CMOS based circuits demonstrated in Chapter 5. An analog 2T FDPix using a saturated load inverter configuration was design, fabricated and tested, and results in a gain on the measured DC response. Furthermore, when integrated using FDPix devices, the voltage transfer curve (VTC) of a CMOS inverter shifts proportionally to the LIVS of the pull-up and pull-down transistors, which in turn modulates the transition voltage (V_M) and propagation delay of the inverter. This later property is exploited to design PWM-based pixel sensors, where the light intensity variations are represented by a variation in the output signal pulse width in time domain, which results in a pre-digitize signal prior to readout and a signal that is immune to voltage supply variations. Using an 8T/pixel design, a variation up to 180µs was experimentally measured. The power consumption of these circuits is expected to be very low since the circuit consumes almost no power in standby, and 28nm node with very low V_{DD} can be used. Also, the circuit response can be modulated using back biasing, and different response can be obtained based on the diode orientation, which adds degrees of freedom to the designers. Finally, we demonstrated that any logic circuit can be made sensitive to light based on the light sensitive inverter. A 6T SRAM with a total area <0.120µm² implemented using FDPix is made sensitive to light, and sequential logic blocks, such as latches, are also controllable via a light-generated clock signal.

FDPix main advantages:

- Size and the use of advanced node technology
- Tuneability inherited from the FDSOI back biasing technique.
- 3D-like structure where the photosensitive element is underneath the sensing transistor.
- Versality of integration since no electrical connection is needed between the top and bottom which prevents the need of stacking connection such as Indium bumps or TSVs. Also, any material can be used as photosensitive element to detect different parts of the spectrum, given their compatibility for the back side bonding.
- No need of extra masks to obtain the FDPix, the standard UTBB FDSOI process is used. The structure is obtained by modifying the ion implantation step of the GP and/or Well.

- The FDPix is scalable to more advanced technology nodes, keeping a UTBB structure with high body factor.
- High DR range of more than 120dB was demonstrated.
- Ultra-Low power can be achieved since the V_{DD} is lower than 1V.

Table 6-1 compares the FDPix regarding the logarithmic and lin-log pixels mentioned in Chapter 1, based on technological node, number of transistors per pixel, supply voltage, and dynamic range. The references can be found in Chapter 1. We can see that the FDPix offer the most compact solution since it contains only one transistor when used in current mode and uses a supply voltage of 0.9V which reduces the power consumption. However, a more accurate comparison would include the FPN which is the major drawback of such sensors, which should be studied in future work.

Table 6-1: Comparison of the FDPix with log and lin-log architectures

Ref	***tech node (µm)***	***#of T***	***VDD (V)***	***DR (dB)***
[Miyatake 2007]	0.18 (CIS)	7 +1 capa	-	190
[Bae 2016]	0.35	5	3.3	>106
[Rhee 2005]	0.5	6	5	94.8
[Lee 2013]	0.5 (CIS)	2.5	3.3	105
[Bae 2016]	0.35	4	3.3	97
[Chou 2014]	0.18	5	3.3	143
[Ni 2001]	0.8	4	-	>120
[Storm 2006]	0.18	7	-	143
[Guo 2009]	0.5	7	-	121.26
[Vatteroni 2008]	0.35	5	3.3	112
[Lee 2013]	0.13 (CIS)	4	3.3	105
[Ni 2011]	0.35	-	-	>120
This work	**28nm**	**1**	**0.9**	**120-130**

6.2. Future work

Here is quick guideline to what could be investigated next.

- The different noise sources proper to the pixel should be investigated, such as the dark current, and the kTC reset noise.
- Readout circuit design and array implementation, which would allow the noise parameter extraction such as FPN, readout noise, and the estimation of the total power consumption.
- The spectral properties as a function of junction position, which can possibly be used to avoid the need of filters.
- More in-depth study of memory sensitive to light for highly integrated sensors.
- The possibility of using DTI and back thinning
- The use of the FDPix for smart pixel design and detection, for example by using the inverter.

- Also, considering the implementation of the FDPix not as an independent pixel but rather to improve the performance of standard pixel by controlling the V_T variation of the source follower with light.

6.3. Perspectives

Based on the characteristics of the device investigated during this work, the potential of integrating highly dense image sensor using FDPix is feasible. Since the trend is moving toward more embedded function close to the sensor, a device such as the FDPix would allow integrating more function and more intelligence in the sensor, while maintaining small size and low power consumption. Its versatility and tuneability are what distinguish such architecture. It can be integrated with different materials for detection spectrum tuning, which represents a great asset since it allows the use of the same detector architecture in a wider range of applications. Its intrinsic wide dynamic range presents an important property for ambient intelligence applications and automotive. It can also find application in IoT sensor network where the power consumption and small size is key. Also, smart sensors based on reconfigurable logic with light can be implemented by a simple CMOS inverter. The trend toward vision for sensing is definitely enabled by technologies that allow the integration of more intelligence very close to sensor and memory.

For a more general perspective regarding FDSOI technology which has proven to be, yet again through this work, a versatile technology. It was already acquired that it was the technology of choice for low power RF and analog sensor. The possibility of detecting light my co-integrating a diode in the bulk highlight the versatility of this technology to be used for different kind of sensors based on the same frontside-backside capacitive coupling. More functionalities can be embedded close to the transistor for different types of sensors used in IoT networks.

APPENDIX

Appendix A : Simulation tools and software

A.1. TCAD Simulations

TCAD simulation is a Finite Element Method (FEM) based simulation that consist in calculating the different semiconductor parameters by solving the Poisson's equation, the Continuity equation, and transport equation at every mesh node and bias point.

The software used in this work is SILVACO, that provides different applications based on the desired device simulation. We used ATLAS, a 2D/3D device simulation software for electrical and optical characterization of our device in DC, and transient. ATLAS comes with multiple modules, the one used are:

- S-PISCES for the electrical part. It is used for silicon-based devices and solve the previously mentioned device equations.
- LUMINOUS, a ray trace and light absorption module. It calculates the photogeneration rate by first calculating a light intensity profile within the structure.

The device should be carefully meshed for proper simulation conversion as shown in Figure A-1. The regions with fine meshing should be the ones where the electric field is the highest. In our case, the MOSFET, including gate oxide, channel, and the BOX back interface where the charges accumulate, and the junction depletion region. The mesh in the bulk and BOX can be relaxed.

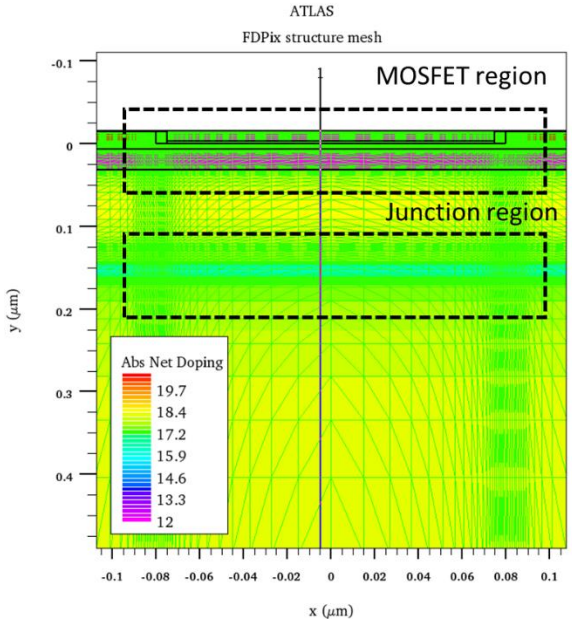


Figure A-1: FDPix mesh in TCAD simulation

The basic models used in all the simulations are:

- CVT: Lombardi mobility model. It considers all the mobility dependences including concentration and electric field dependences.

- FERMI: used for carrier transport statistics
- SRH: Recombination model, used with fixed carrier life time.

In DC simulations, we added the following:

- CONSRH: with concentration dependent life time
- BGN: to account for bandgap narrowing when high doping concentration are used.
- NI.FERMI: intrinsic concentration calculated using Fermi statistics and fetched back in the SRH model
- DGROOT, DG.N, DG.P: Quantum potential and density gradient models

In transient when resetting the device using back gate, the simulation time is much higher. To reduce it, and since we look at a difference in value rather than the absolute value, we used only the basic models (CVT, SRH, FERMI) adding to them BTBT, band-to-band-tunneling that can occur in high electric field in the diode junction.

For the optical simulation, at each bias point or time step for transient, the complex refractive index of the materials is used. The amplitude of the intensity at each grid point is calculated using the real part, and the absorption and photogeneration is calculated using the imaginary part, to extract carrier concentration at each grid point. The transfer matrix method is used as it is the most efficient for layered devices.

Both monochromatic simulation and wideband were performed. The reference spectrum used in the simulation is the AM1.5 sola spectrum shown in Figure A-2, with total integrated power of 100mW/cm². In general, we specify the wavelength range in the simulation to be from 0.3 to 1.4µm. The beam is always incident normal to the surface (90° angle).

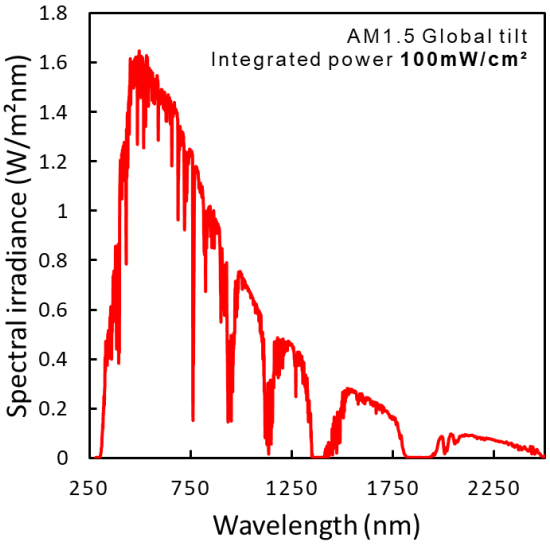


Figure A-2: AM1.5 solar spectrum used in TCAD simulation

A.2. SPICE simulation

SPICE simulation is used for circuit design. It allows the check of the operation of the circuit and predict its behavior under AC, DC and transient bias. SPICE simulator works by solving the compact model equations that describe the different component in a circuit. Therefore, to perform circuit simulation of the FDPix using SPICE, a dedicated model was developed. The full procedure is summarized in Figure A-3.

The analytical model as mentioned in Chapter 2, is based on Leti-UTSOI2.1 *[POIROUX 2013][POIROUX 2015]* for the FDSOI transistor description, and JUNCAP2 *[SCHOLTEN 2010]* for the diode definition. Adding to the diode description, is the photogeneration equations (Chapter 2). Here some specification regarding Leti-UTSOI2.1 are given.

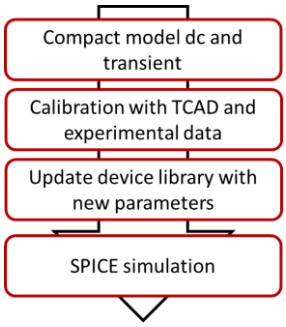


Figure A-3: circuit design simulation flow

Leti-UTSOI2.1 is a surface potential-based model developed at Leti for UTBB FDSOI MOSFET description. It specifically works for lightly doped silicon film (channel). It accurately describes the coupling that occurs between the back and front interface, as well as back interface inversion. Therefore, using UTSOI2.1, the behavior of the transistor can be predicted for a large range of back bias voltages.

The model, offers two sets of parameters, Global and local, that are provided in the model card. By modifying these parameters, the model is calibrated with experimental data and TCAD simulation to accurately describe the hardware. The same procedure is performed for the photodiode model.

The device library (*.lib*) contains subcircuits (*.subckt*) that represent the different types of MOSFETs as well as their V_T flavor (RVT and LVT). It also contains subcircuit for the junction, defined as either PN or NP oriented. For each of these subcircuits, a set of global and local parameters are defined and alterable. Some of these parameters can be defined globally in the device description which will allow its modification within the netlist. Finally, a subcircuits for the FDPix-NP and FDPix-PN are also defined. An example of FDPix-NP subcircuit is given below:

```
* --------------------N-channel LVT MOSFET with diode NP --------------------*

.subckt lvtnfet_pwell D G S B P Bp swphoto=0 popt=1.0e3 w=210.0n l=30.00n nf=1 as=0.000
ad=0.000 ps=0.000 pd=0.000  vfbo=-160m tox=1.000n

x1 D G S Bp lvtnfet w='w' l='l' nf='nf' vfbo='vfbo' tox='tox'
x2 B Bp P diodeNP area=2.0p swphoto='swphoto' popt='popt'

.ends lvtnfet_pwell
```

The subcircuit name is “lvtnfet_pwell”, what follows the name is the nodes of the device, in our case, Drain, Gate, Source, Back gate, P_{opt} (defined as a potential), and ground plane. The parameters that come after that are all adjustable within the netlist. Then we can see the two component x_1: lvtnfet and x_2: diode NP that were defined in the library prior to this subcircuit. For the PWM-based circuits, the library also contained subcircuits for the inverters, NAND and XOR.

The Netlist is where the circuit is described with devices and nodes, and where the test is defined and set. All the different bias are applied to the nodes, the sweeps are also defined and the type of test to be performed selected. An example of a netlist for light sensitive inverter test is shown in Figure A-4 below.

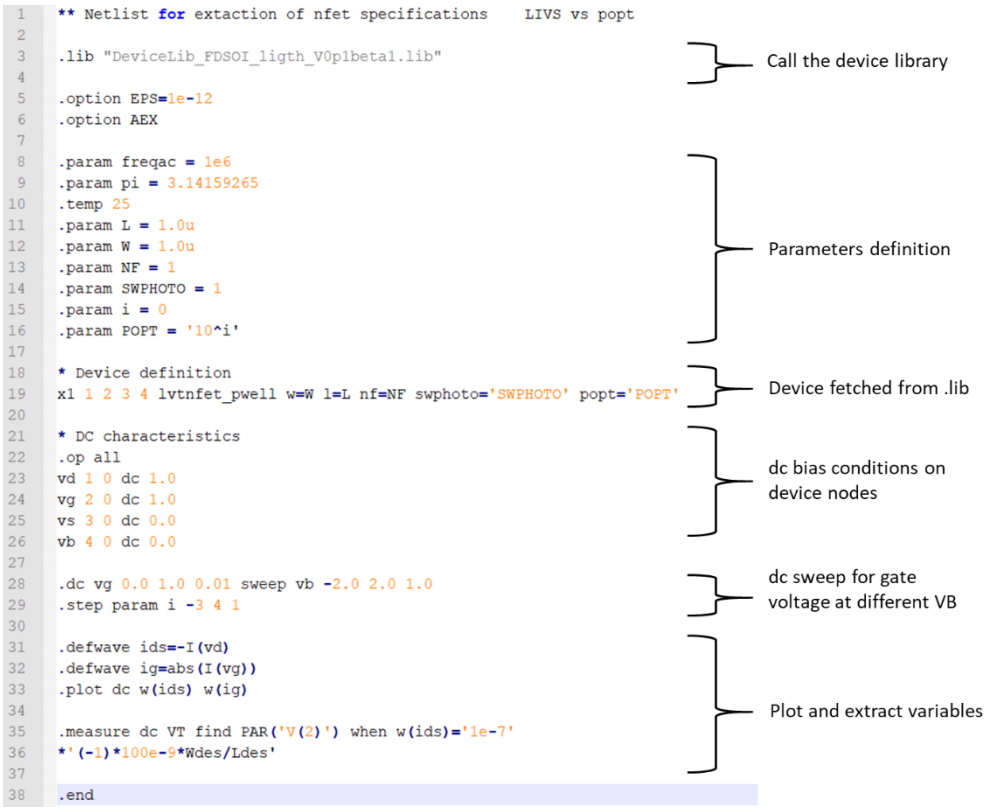


Figure A-4: SPICE netlist example for IDVG on FDPix

Thanks to the developed compact model for the FDPix, several circuits were designed and fabricated where the expected behavior was validated. In the current version however, the noise module is not taken into account in the MOSFET and photodiode components, therefore, future work to improve the model should include the noise parameters.

Appendix B : Opto-electrical characterization setup

This appendix provides some specifications regarding the deferent components of the opto-elecrical characterization setup that was used during this thesis, to test the devices in DC and transient. The complete setup is schematically represented in Figure B-1 and shown in Figure B-2. It consists in two part: the electrical test part, and the optical source part. All tested wafers were 300mm wafers in 28nm FDSOI technology manufactured at STMicroelectronics, and only front side illumination (FSI) was used.

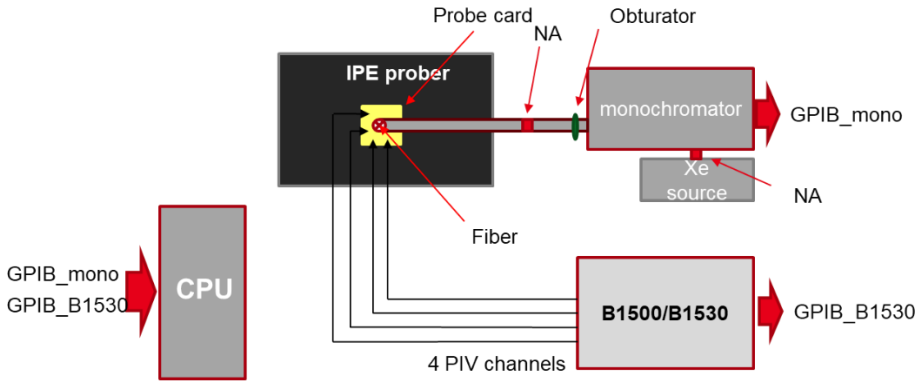


Figure B-1: FDPix opto-electrical characterization setup

Figure B-2: pictures of the developed setup

The setup consists in a wafer prober for wafer manipulation, electrical analysis tools, and an optical source. The light source output is always perpendicular to the device front surface. Depending on the test, the sequence might differ, but a standard test is:

1. Move to die
2. Move to contact (tips on pads)
3. First test in dark
4. Turn light on
5. Run test
6. Data acquisition and save

The different parts of the setup are presented next.

B.1. Wafer prober

A wafer prober is necessary to manipulate the wafer at the µm scale. Two different types were used during this work:

- Cascade semi-automatic wafer prober: this tool can be remotely controlled with a computer, using commands within GPIB protocol, which allows the launch of automatic parametric tests on multiple dies. It comes with several probe tips (connected to micromanipulators) for connecting and bias Device Under Test (DUT) pads. This prober was mainly used for preliminary DC tests where the light source is the microscope wide band light is used in on-off position only. It was measured to be equal to ~300mW/cm².
- The second wafer used is a Signatone full manual (Figure B-2). the advantage of this prober is that a monochromator optical source is mounted on it which allowed us to vary the light intensity in a controlled way, and the availability of a probe card compatible with the prober. It also has a top hat and a dark environment cover to avoid parasitic light. All the transient tests were performed on this prober. The main disadvantage is that no programed cartography can be performed since the prober cannot be controlled via software.

B.2. Semiconductor analyzer

The electrical test (bias and measurement) are performed using the following two equipment:

- A Keysight B1500 device analyzer, allowing quasi static tests (DC), for example I(V) characteristics. It also integrates the Keysight B1530 plug-in module.
- Keysight B1530 is a waveform generator fast measurement unit (WGFMU) plugged-in module. Its main function is to output voltage pulses, together with aggressive current measurement capabilities. Using the B1530 *[KEYSIGHT TECHNOLOGIES]*:
    - Voltages with arbitrary pulse shapes, and 10ns programming resolution can be applied.
    - It has a fast current/voltage measurement mode (fastiv) that allows to apply and measure simultaneously the voltage and current with a resolution of 2nA, and a sampling rate of 5ns.

During this work, a B1500 with 2 B1530 racks has been used, thus providing 4 synchronized channels.

B.3. Monochromator and light source specifications

The optical part of the setup is composed of:

- A 450W Xenon source Ozone free with the spectrum measured using a silicon sensor (190nm to 1100nm range) and shown in Figure B-3.a. that provides a range of wavelength form UV to NIR (200 to 2400nm).
- A monochromator TRIAX 180, which is used to output a monochromatic light. It is composed of two Numerical Apertures (NA) at the input and output of light wave. The NA opening is from 0.8 to 7mm (0.25*1/8” to 2.24*1/8”). A set of two mirrors, one that reflect the source light towards the output, and the other the reflected a diffracted light from grid to output. The wavelength is selected by controlling the orientation of the diffraction grid, which is done using a software.

- An UV optical fiber (1550µm diameter) at the output of a catadioptric adaptation system, that transmit the monochromatic signal to the DUT.

We used the monochromator in two ways, one for spectral characterization (LIVS vs wavelength) presented in Chapter 4, the second and the most used way, using wideband spectrum of the source (visible light) to obtain a maximum of response. To vary the optical power density, the NA is varied. Figure B-3.b show the power density modulation for different NA and using an obturator with two different positions. The minimum NA recommended is 0.25", bellow that value, the output is not reliable. To explore a maximum range of intensities, the obturator position is first used in the "1.0" position for lower intensity, and then on the "1.5" position to obtain higher intensities.

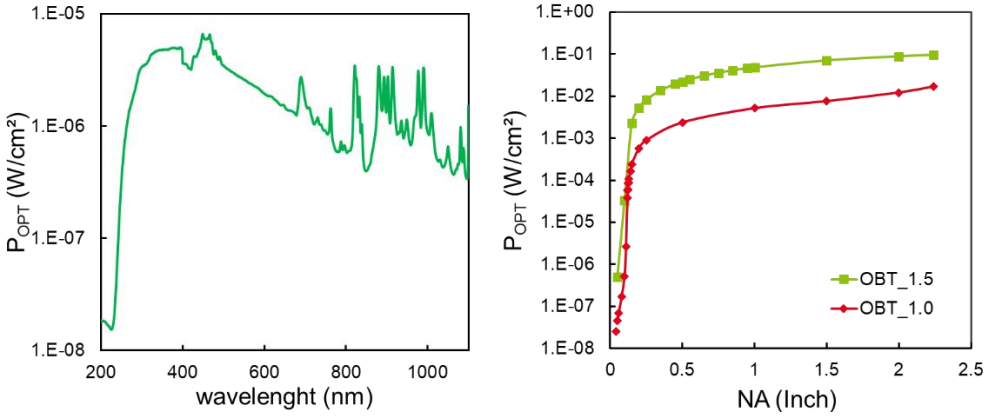


Figure B-3: a) Xenon source Spectral response b) modulation of output power using NA and OBT

The sensor used to measure the optical power density is approximately at the same distance from the optical fiber output as the DUT when illuminated using the fiber. Therefore, the measured power density corresponds to the one incident on the surface of the device.

B.4. Instrumentation using Python and LabView

All the tools are controlled using computer programs. The monochromator is controlled using a user interface programmed in LabView where the commands are communicated using GPIB protocol. The semiconductor analyzer is fully controlled using a script codded in Python. The program takes into account prober type (manual vs semi-auto), the number of channels available, and the test to be run (DC, transient). The main functions of the program are:

- Control DUT position and contact of probes (for semi-auto prober only)
- Define and run the test sequences, patterns, and timing through commands translated to GPIB through a command library.
- Create systematic files for saving the acquired measurement data.
- Pre-processing of data for fast visualization of test results.

An example of such a program is presented below.

```
1   # -*-coding:Latin-1 -*
7   import B1530driver as B1530
8   import matplotlib.pyplot as plt
9   import numpy as np
10  import os as os
11  import time
12  import visa
13  from matplotlib import rc
14  import matplotlib as mpl
15
16  #VARIABLES FOR RESULTS FILE
17  Lot = 'Q531123'
18  waferNo = 'P08'
19  scribeName = 'PCO03'
20  deviceNo = '1'
21  testName = 'Reset'
22  comment='1_Pulse__reset_var_[0, 0.05,0.1,0.122,0.128,0.14, 0.2, 0.25, 0.5] @ 1.0'
23
24  cascadeActiv = False
25
26  #EQUIPMENTS GPIB ADDRESSES
27  b1530_gpib = r'GPIB0::17::INSTR'
28  cascade_gpig = r'GPIB0::28::INSTR'
29
30  ##DEFINITION OF FUNCTION FOR OUTPUT FILE
31  def plot para(title, x label, y label):
40  def result file(lot, waferName, test, scribe):
67  def parameter file(loc,VDD,VGG,VBB,Tpulse,noPoints, tduration, tavg, vRange,twait,tperiod,irange,trise):
87  def dieNo(die, x=0, y=0, na=0):
91  def results write(location, device, die, rslT, rslV, rslI, rslIG):
107
108 #TEST OPTIONS
109 def OneReset():
259 def Reset():
406
407 ##CASCADE PROBER INITIALIZATION
408 if cascadeActiv:
414 if cascadeActiv:
416 else:
418 if cascadeActiv:
427
428 ########################################
429 #### RUN TEST, PLOT, AND SAVE DATA ####
430 ########################################
431
432 for i in range(nbDice):   ###loop over the number of die
487
488 print 'GAME OVER'
489
```

All the data processing is also performed using Python scripts. An example is given below of the function used in a script to calculate the SNM of measured SRAM cells.

```
def SNM_extract(x1, y1, x2, y2, sidex):
    """
    function to extract the SNM from the butterfly curve.
    Only for one side
    x1--> Vin, y1 --> Vout || x2 --> reversed Vin, y2-->reversed Vout
    it returns the side of the square (ie SNM), and the Points at of the corners
    """
    #initial side length to be compared with
    side = 0

    #initial list where points will be saved
    points_interest = []

    # points_a is of the form [[x1,y1], [x2,y2],...[xn,yn]] of the first curve
    points_a = np.vstack((x1,y1)).T
    # points_b same as points_a but for the second curve
    points_b = np.vstack((x2, y2)).T

    for i in range(len(points_a)):
        for j in range(len(points_b)):
            if sidex=='left':
                dx = points_a[i][0]-points_b[j][0]
                dy = points_a[i][1]-points_b[j][1]
            elif sidex=='right':
                dx = points_b[j][0] - points_a[i][0]
                dy = points_b[j][1] - points_a[i][1]
            if debug==True:
                print dx, '\n', dy
            if (abs(dx-dy) <= 0.01) and (dx>side):
                side = dx
                if debug==True:
                    print 'dx= ',dx,'\ndy = ',dy, '\n dx - dy = ',abs(dx)-abs(dy)
                points_interest = [points_a[i],points_b[j]]
            else:
                pass
    return side, points_interest
```

The extracted square sides are then compared to find the largest possible that defines the SNM.

```
side1_snm, point_winner1 = SNM_extract(Vblf_sweep[0:len(Vblf_sweep)/2], Vblt_dark[0:len(Vblt_dark)/2],
                                       list(reversed(Vblf_dark))[0:len(Vblf_dark)/2],list(reversed(Vblt_sweep))[0:len(Vblt_sweep)/2], 'left')

side2_snm, point_winner2 = SNM_extract(Vblf_sweep[(len(Vblf_sweep)/2):-1], Vblt_dark[(len(Vblt_dark)/2):-1],
                                       list(reversed(Vblf_dark))[(len(Vblf_dark)/2):-1],list(reversed(Vblt_sweep))[(len(Vblt_sweep)/2):-1], 'right')

if light:
    side3_snm, point_winner3 = SNM_extract(Vblf_sweep[0:len(Vblf_sweep)/2], Vblt_light[0:len(Vblt_light)/2],
                                           list(reversed(Vblf_light))[0:len(Vblf_light)/2],list(reversed(Vblt_sweep))[0:len(Vblt_sweep)/2], 'left')

    side4_snm, point_winner4 = SNM_extract(Vblf_sweep[(len(Vblf_sweep)/2):-1], Vblt_light[(len(Vblt_light)/2):-1],
                                           list(reversed(Vblf_light))[(len(Vblf_light)/2):-1],list(reversed(Vblt_sweep))[(len(Vblt_sweep)/2):-1], 'right')


if debug:

if side1_snm>side2_snm:
elif side1_snm<side2_snm:

if light:
```

Appendix C : Extra experiments and results

C.1. FDPix sensor with reset transistor

In standard image sensors, a transistor is dedicated to reset the diode and set the initial voltage at V_{RST} (V_{RST}=V_{DD}-V_{Trst}). We also considered this option to reset the sensor. Although in our case, the sensing node, i.e. GP, is floating and no electrical connection are available in standard 28nm process technology. However, multiple integration scheme were propose to provide a GP connection in FDSOI, since it would improve the back bias performance and avoid parasitic diodes between different wells in a chip *[GRENOUILLET 2012]*.

Therefore, we performed opto-electrical characterization on a fabricated 2T FDPix using an NMOS reset transistor (Trst) as shown in Figure C-1, where a schematic and layout of the fabricated structures are shown. The reset is performed by pulsing the gate of the Trst for it to be ON and the potential of the GP to be set at V_{DD}-V_{Trst}. This is called a "hard reset" as opposed to "soft reset" where the junction is reseted just enough to avoid saturation, which expands the DR.

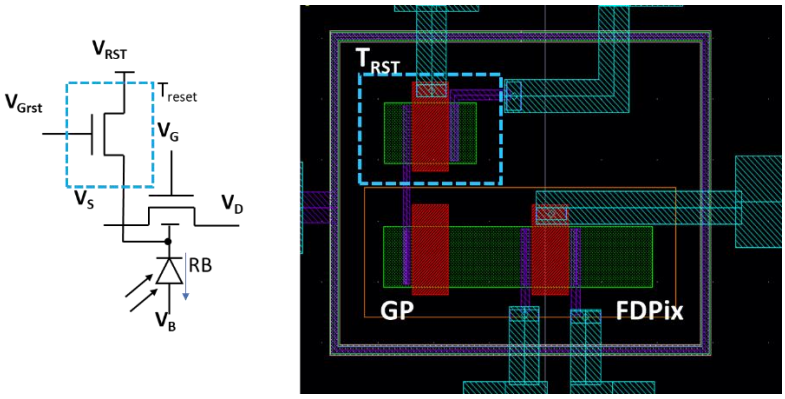


Figure C-1: schematic and layout of 2T FDPix w/ reset transistor

The tests are first performed in DC. Figure C-2 shows the obtained I_DV_G curves for the FDPix in dark and under illumination. The V_{RST} applied to Trst is set to 0V, thus when turning Trst ON, the GP potential should be fixed at 0V. Under dark condition, the curve doesn't change whether Trst is ON or OFF. When the Trst is OFF, we can observe the LIVS under illumination. When turning Trst ON by applying V_{DD} at the gate, a current will flow preventing the accumulation of charges, therefore the curve doesn't shift and stays at the dark condition position, which indicates that the GP potential can effectively be controlled through Trst.

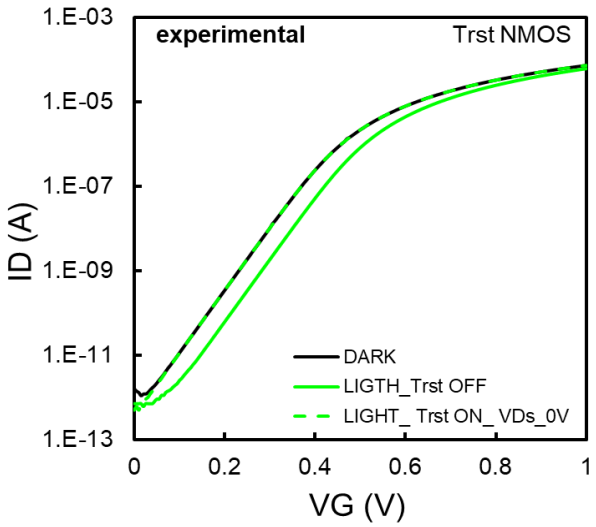


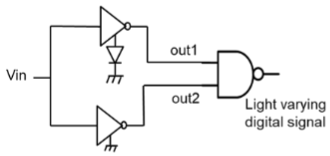
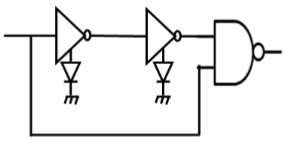
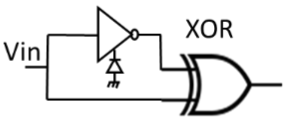
Figure C-2: IDVG for the 2T FDPix with NMOS reset transistor

C.2. PWM-based FDPix: other implementation options

The PWM-based circuit presented in Chapter 5 is based on the comparison of the output of two inverters connected at the input of a comparator (parallel inverters). Based on the same principle, other circuit implementations were evaluated using SPICE simulations and presented below.

The discussed circuits are summarized in Table C-1, where the pros and cons of each are presented.

Table C-1: PWM-based FDPix circuit design options

Circuit 1: **Parallel inverters**	Circuit 2: **Series inverters**	Circuit 3: **Single inverter**
		
+ 8T/pix (advanced nodes 28FDSOI) + High DR + Ultra low power operation + Tunability using back bias + Optimized FF without 3D process (monolithic integration) + High SNR - Counter not included	+ 8T/pix + Higher FF + Accuracy of signal depend on # of inverters - Counter not included	+ 10T/pix + No variability issues - Counter not included

C.2.1. Series inverters

In this case, both inverters are sensitive to light to obtain a gain on the duty cycle change. The diode orientations are similar for the two inverters to obtain an identical variation with light. Again, different comparators can be used, the NAND is used for simulation examples. This architecture results in higher FF since both inverters are sensitive to light. The light effect is also averaged using this kind of configuration, which means the accuracy of the measurement depend on the number of inverters in series.

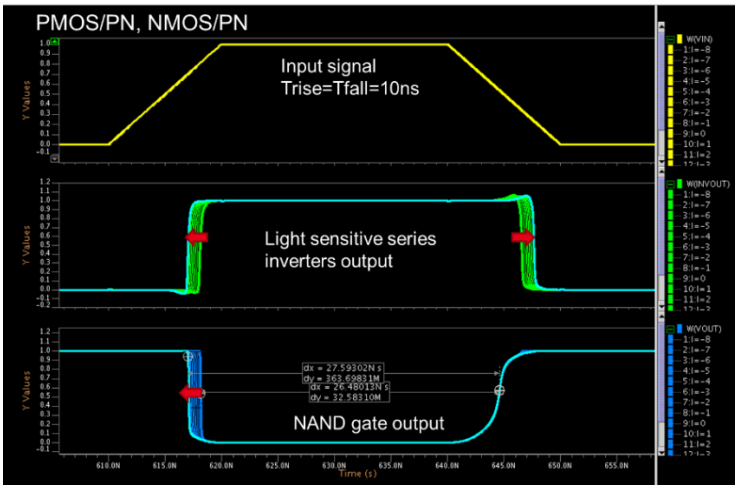


Figure C-3: series inverter PWM-based FDPix SPICE simulation results using PN oriented diode

C.2.2. Single inverter and comparator

In this case, the NAND gate cannot be used, instead the XOR gate is used. The diode polarity is different for each transistor in the inverter. If the inverter is well balanced, the shifts from both sides will compensate and so there will be no change in the duty cycle. But if they're not (as in the simulation) a change can be detected whatever the diode orientation.

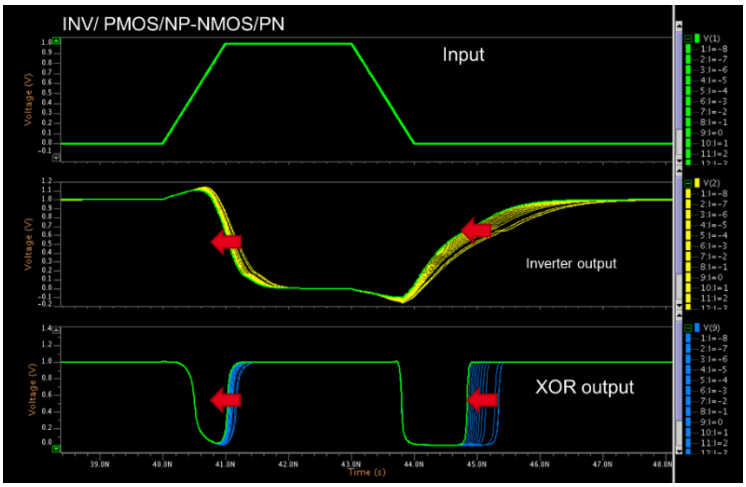


Figure C-4:single inverter PWM-based FDPix SPICE simulation results

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Study of new FDSOI-based integrated circuit architectures sensitive to light for imaging applications

Abstract

A new type of light sensor called FDPix, composed of one transistor (1T) per pixel is investigated. It consists in co-integrating an FDSOI (Fully-Depleted Silicon-On-Insulator) transistor with a photodiode to enable light sensing through optical back biasing. The absorption of photons and resulting photogenerated charges in the diode will result in a Light Induced V_T Shift (LIVS). The LIVS is due to a capacitive coupling between the front and back gate of the FDSOI transistor and represents the key performance metric to be extracted and optimized. In this work, the device behavior in dc and transient domains was thoroughly investigated and modeled. Although not limited to this node, all the devices tested were fabricated using 28nm node FDSOI technology. By means of TCAD simulations and opto-electrical characterization, the device parameters such as Body Factor (BF) and junction profile were optimized to improve its performance. It was found that the FDPix is in fact a dual response sensor. It exhibits a linear response at low light intensity which results in high sensitivity, and a logarithmic response at higher intensities that ensures a high dynamic range (DR) of more than 120dB. The dedicated developed model is implemented in SPICE environment for circuit design. New pixel circuit in analog and digital domain, based on the FDPix were designed, fabricated, and tested. The results obtained and presented in this work, shows the potential of using the FDPix sensor for smart, highly embedded, low power image sensors for More-than-Moore applications.

Keywords FDPix, UTBB FDSOI technology, Capacitive coupling, LIVS, CIS, embedded light sensor

Etude de nouvelles architectures sensibles à la lumière en filière FDSOI pour des applications de type imageurs

Résumé

Un nouveau type de capteur de lumière appelé FDPix, composé d'un transistor (1T) par pixel, est étudié. Il consiste à co-intégrer un transistor FDSOI (silicium sur isolant entièrement déserté) avec une photodiode pour permettre la détection de la lumière par polarisation arrière optique. Les charges photogénérées dans la diode induisent un décalage de tension de seuil (V_T) sous illumination, appelé LIVS. Le LIVS est dû au couplage capacitif entre les grilles avant et arrière du transistor FDSOI et représente la métrique de performance clé à extraire et à optimiser. Dans ce travail, le comportement du dispositif en régimes continu et transitoire a été étudié et modélisé de manière approfondie. Bien qu'ils ne se limitent pas à ce nœud, tous les dispositifs testés ont été fabriqués en technologie FDSOI 28nm. Au moyen de simulations TCAD et de caractérisations électro-optiques, les paramètres du dispositif, tels que le facteur de couplage (BF) et le profil de la jonction, ont été optimisés pour améliorer ses performances. Il a été constaté que le FDPix est en fait un capteur à double réponse. Il présente une réponse linéaire aux intensités lumineuses faible qui se traduit par une sensibilité élevée, ainsi qu'une réponse logarithmique aux intensités élevées assurant une grande plage dynamique (DR) supérieure à 120 dB. Un modèle dédié a été développé et implémenté en environnement SPICE pour la conception de circuits. Ainsi, des nouveaux pixels, analogiques et numériques, ont été conçus, fabriqués et testés. Les résultats obtenus et présentés dans ce travail montrent le réel potentiel d'implémentation du FDPix dans des capteurs de lumière intelligents, ultra compacts, et de faible consommation, destinés aux applications More-than-Moore.

Mots clefs FDPix, technologie UTBB FDSOI, couplage capacitif, LIVS, capteur d'image CMOS, capteur intégré