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Development and study of advanced dielectrics for low-voltage printed transistors

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THÈSE

Pour obtenir le grade de

DOCTEUR DE LA COMMUNAUTÉ UNIVERSITÉ GRENOBLE ALPES

Spécialité : NANO ELECTRONIQUE ET NANO TECHNOLOGIES

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préparée au sein du **Laboratoire CEA/LITEN**

dans l'**École Doctorale Electronique, Electrotechnique,
Automatique, Traitement du Signal (EEATS)**

Etude et développement de diélectriques avancés pour des transistors imprimés low- voltage

Development and study of advanced dielectrics for low-voltage printed transistors

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General introduction

Electronics as we know it today takes an important part of our modern lives. It is present in phones, cars, houses and most of the other aspects of our society. However, classic electronics may sometime be limiting in terms of costs and applications. Most electronic devices are based on processors/chips fabricated from silicon, which is mostly obtained through costly and energetically demanding processes like refining and doping using high temperature ovens. As a result, these components are extremely efficient but can also sometime be expensive, fragile and non-compliant.

Complementary to the classic microelectronics, organic electronics can be fabricated from solution processable materials and with temperature rarely exceeding 200 °C. Moreover, these organic materials present some interesting properties not found in classic electronic like transparency, conformability or in some case full flexibility. These new properties can expand the scope of possible applications for electronic device. However, as the field organic electronics is still relatively young compared to the classic microelectronics, the performances of most organic devices are relatively low if compared to their inorganic counterparts.

With the expansion and development of the internet of things, a concept aimed towards the interconnectivity of daily objects and applications, there is an increasing need for high efficiency and adaptable electronic devices. A possible approach to

meet this criteria is to take advantage of the performance of microelectronics and the adaptability of organic electronics by combining them into new devices like seen curved OLED screens. However, not all organic device are already compatible with classic electronic, for example most printed organic transistors operate at voltage from 20 to 30 volts whereas classic electronics chips operate around five volts or below (3.3 V, 1.8 V and 1.2 V). Moreover, the reduction of operating voltage for organic transistors would also reduce their energy consumption which might be a critical factor for hand-held or wearable applications since this type of devices will likely rely on battery to operate.

Considering this problematic, the focus of this thesis was to study the impact transistor's operating voltage reduction while remaining compatible with solution/printing process and consequently study the characteristic of the materials used for the fabrication of these type of devices.

This work is articulated in four different chapters:

Chapter 1 The first section of this chapter describes the basic theory regarding organic semiconductors, the working principle of transistors and the different methods used for their characterisation. It will then present the different approaches reported in the literature for the reduction of operating voltage in organic transistors and detail the methodology followed in this work.

Chapter 2 This second chapter focusses on the study of the dielectric properties of a polymeric high- κ material (Polyvinylidene fluoride derivatives). We will discuss here the impact of chemical composition, bias, frequency and temperature on the measured dielectric properties. Furthermore we will discuss the impact of a specific bilayer dielectric structure on the previously mentioned properties.

Chapter 3 The third chapter of this thesis will focus on the transistor device. We will study the impact of the selected high- κ dielectric on the transistor characteristic and compare its performance to a standard device.

Chapter 4 This final chapter will investigate the electrical stability of both the reference device and low-voltage transistor and aim to understand the origin of possible difference between these two devices.

Context of the topic

This chapter aims to explain the context of low-voltage organic transistors and the different theoretical building blocks of this topic. In the first part, we will discuss Organic Thin Film Transistors (OTFTs), how they are fabricated, from what materials and the theoretical equations describing their ideal behaviour. Then we will discuss the different approaches to reduce the operating voltage of standards OTFTs. Finally we will describe the objectives of this thesis, our selected approach for low-voltage transistors and the general layout for our study.

1.1. ORGANIC THIN FILM TRANSISTORS

1.1.1 Basic materials in electronic

In classic electronics, there are commonly three main classes of materials considered (superconducting, spintronics and metamaterials are not in the scope of this work) :

Conductors Materials capable of conducting electricity ($\rho \leq 10^{-6} \Omega.m$), which valence and conduction bands superimpose one another (usually metals or highly doped materials).

Insulators Materials not capable of conducting electricity ($\rho \geq 10^{15} \Omega.m$), the difference of energy level between their valence and conduction bands is generally above 5 eV.

Semi-conductors All other materials comprised between conductors and insulators, their conduction behaviour may be changed via external physical input. They display a Band Gap (E_g) smaller than insulators ($0.3 \text{ eV} < E_g < 5 \text{ eV}$).

Historically, inorganic materials were the first semiconductors used and developed, with their properties reported as early as 1821 (Seebeck effect). In the early part of the 20th century an unified theory of solid-state physics theorized that the origin of semiconducting properties were the highly ordered crystalline lattices that generate bands of energy levels allowing transport of charge carriers.

In Figure 1.1 is depicted a simplified representation of these energy levels in the different classes of materials used in classic electronics. The dashed line represents the Fermi level (E_F) which is a theoretical energy level that has a 50 % chance of being filled by an electron. In the case of semiconductor materials, the position of the bands relative to the E_F dictates its conduction properties. In intrinsic semiconductors, the Fermi level sits in the middle of the band gap but if this semiconductor is doped with electron donor/acceptor species the E_F shifts. If the dopant is an electron donor, the Fermi level is shifted towards the conduction band and the semiconductor becomes a N-type. If the dopant is an electron acceptor the level shift toward the valence band and the semiconductor is thus a P-type.

1.1.2 Organic semiconductors

Organic semiconductors (OSCs) were discovered much later than their inorganic counterparts, so much so that the first transistor (December 1947[1]) was built before the first reported organic semiconductor crystal[2, 3]. In 1977 Shirakawa et

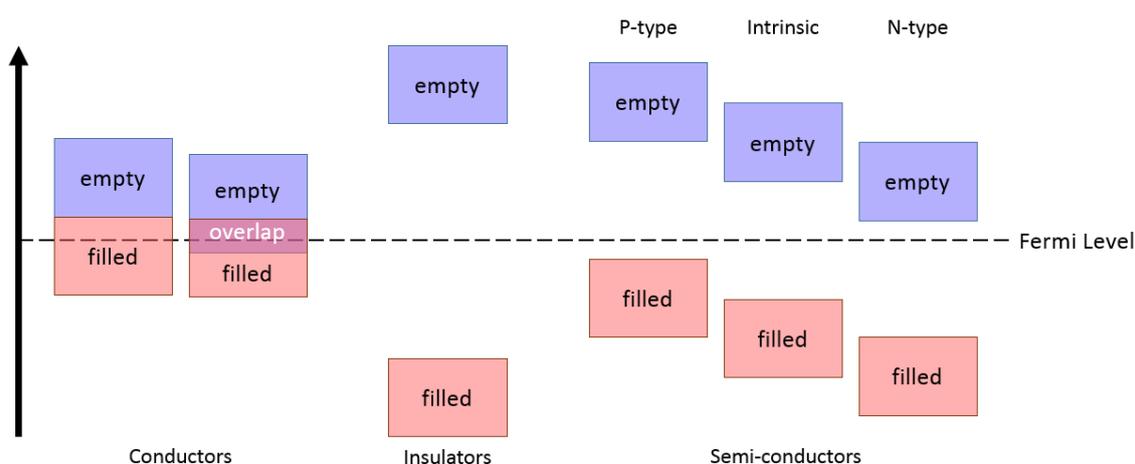


Figure 1.1: Schematic representation of energy levels in different types of materials.

al[4] reported the first polymeric (iodine doped poly-acetylene) material exhibiting semiconducting properties.

As explained previously, the origin of semiconducting properties in inorganic materials find its source in the intermediate band gap between its conduction and valence bands. These bands are a product of the highly organized covalent bonding present in inorganic crystalline structures. However, no such three dimensional bonding is generally observed in organic materials as organic crystals are commonly built from stacked molecules held together by Debye interactions.

Pursuing their study on organic semiconductors H. Shirakawa, A.G MacDiarmid and A.J Heeger received the Nobel price of physics in 2000 for their work on the organic semiconductor theory[5]. They theorized that the semiconducting properties in polymers are enabled by the π -bonding between two atoms in a molecules. When multiple π -bonds are in proximity (stacked in a crystal or along a polymer chain) the resulting energy levels of each molecules or monomers will produce degenerate energy levels. With a sufficient amount of molecules/monomers the multitudes of degenerated energy levels will effectively act as valence and conduction bands as described in Figure 1.2.

Two main families of organic semiconductors, with both their strengths and weaknesses, exists:

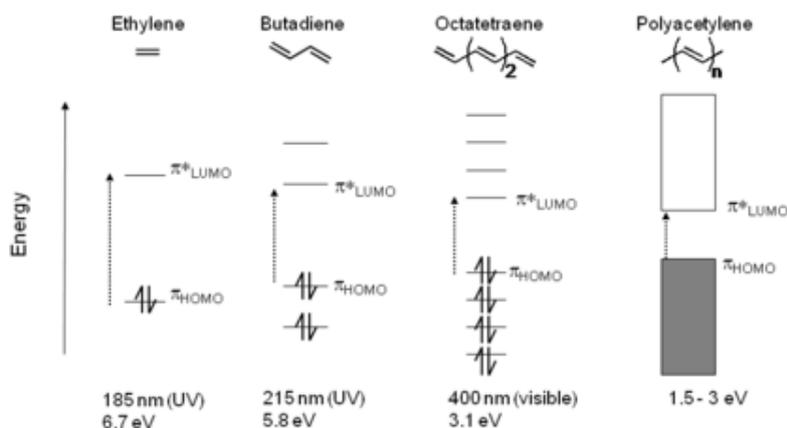


Figure 1.2: Evolution of energy for bonding and antibonding levels in π -bounded polymers with the number of monomer units, the band gap is represented by the energy difference between the Highest Occupied Molecular Orbital (HOMO) and the Lowest Unoccupied Molecular Orbital (LUMO) (reproduced from[6]).

Small molecules They often rely on a highly ordered stacking (crystals) for charge carriers transport[7]. As a result the primary mean of deposition for small molecules is vacuum evaporation as solution process is prone to form lesser quality crystals (ie : higher grain boundary density). They usually show higher mobilities than their polymeric counterpart as can be seen in Figure 4.12.

Polymers Their are constituted of long arrangement of monomers containing π -bounds. Generally they offer the advantage of high reproducibility over large surface as they may be semi-crystalline or amorphous, to the price of a overall lower mobility. They are mainly solution processable and can either be deposited via coating or printing techniques.

1.1.3 Organic transistor theory - basic principle

The various transistor structures available in classic electronic rely on two main operation principles (or a combination of both). One based on the junction between n-type and p-type semiconductors and the other based on the capability of semiconductors to modulate their conductivity when exposed to an external electric field

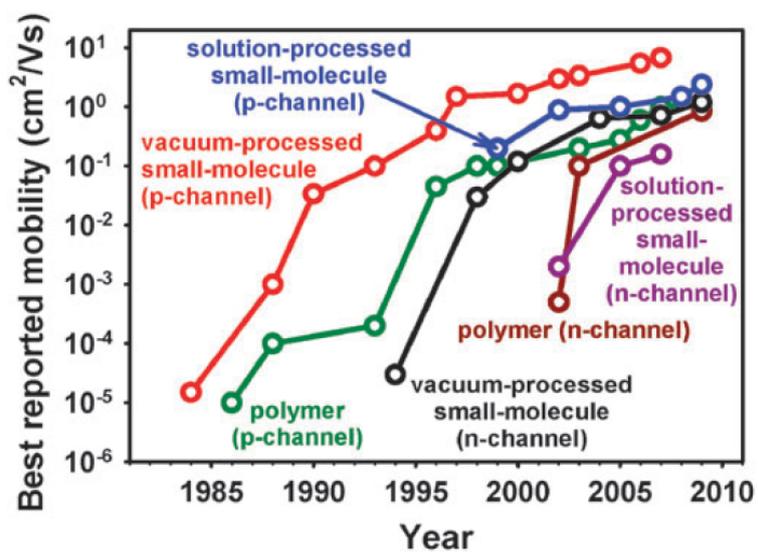


Figure 1.3: Evolution of mobility in organic semiconductors through the years (reproduced from [8]).

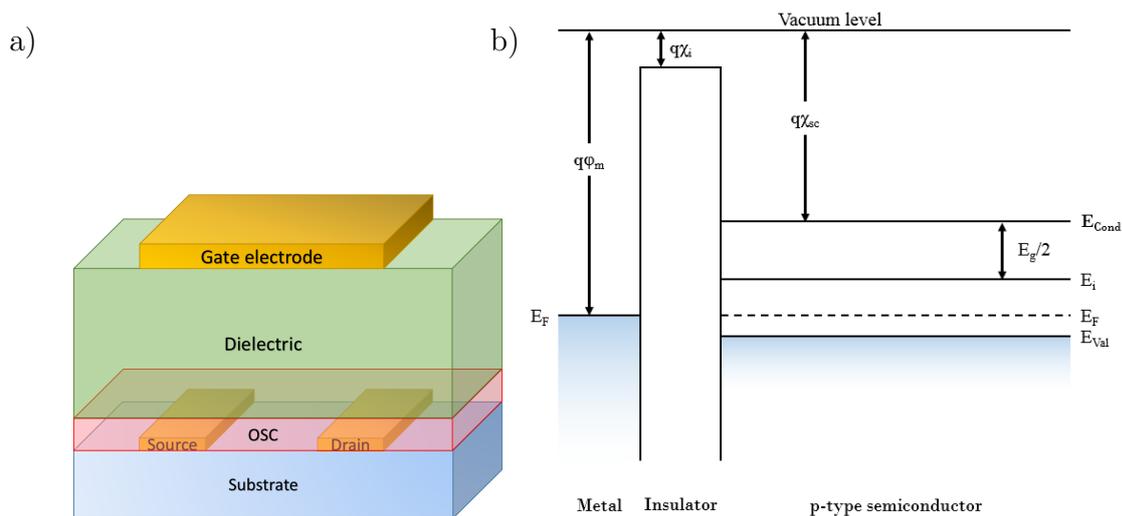


Figure 1.4: a) Schematic structure of an organic field effect transistor and b) the representation of energy levels for a p-type semiconductor MIS capacitor.

(field effect). However, organic transistors are mainly Thin Film Transistors (TFTs) which place them in the Field Effect Transistors (FETs) category. Organic Field Effect Transistors (OFETs) are built from the stacking of an organic semiconductor, an insulator and three conductive electrodes (Source, Drain and Gate) as is described in Figure 1.4 a).

To better understand the operation principle of FETs we can look at a simplified structure: the Metal-Insulator-Semiconductor (MIS); and then extrapolate its behaviour to the transistor structure. In Figure 1.4 b) is represented an ideal p-type semiconductor MIS structure (from the band theory point of view) at energy equilibrium (ie: with no applied voltage). On this diagram are represented: the metal work function (ϕ_m), electronic affinities for the insulator (χ_i) and the semiconductor (χ_{sc}) and E_{cond} , E_i , E_{val} , E_F the energy of respectively the conduction band level, the intrinsic Fermi level, the valence band level and the effective Fermi level of the p-type semiconductor. At equilibrium and in an ideal structure, the Fermi level of the semi-conductor and the metal's work function are aligned. This state is known as the Flat Band state since both the conduction and valence bands are straight. However, the Fermi level shifts when an electrical potential is applied, introducing a bending in the semiconductor's bands.

Depending on amplitude of the applied voltage and the semiconductor's type there are three main modes that may be achieved in the MIS structure and by extension in FETs (Figure 1.5). These modes are known as the accumulation, weak inversion and strong inversion mode. Typical MOSFET transistors operate in strong inversion mode, meaning that the charge carriers responsible for current transport in MOSFET are in fact the minority charge carriers. With a high enough applied voltage the majority charge carriers are fully depleted from the interface. However, in organic transistors, the primary mode of operation is not imposed by the semiconductor but rather by the ϕ_m of the source and drain electrodes. If their work function is close to the HOMO of the organic material injection of holes into the semiconductor will be enabled (lower injection barrier) however if it is closer to the LUMO then electrons will be the majority charge carriers[9].

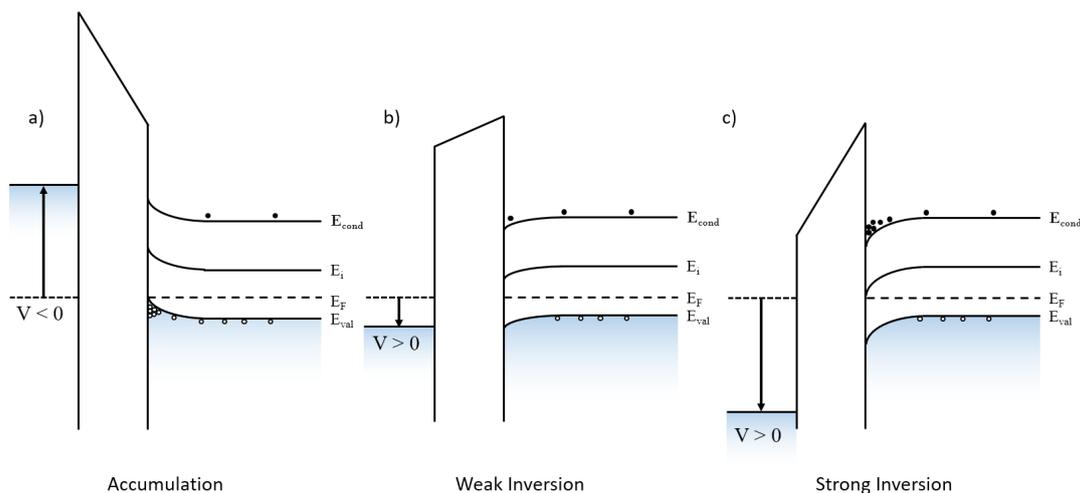


Figure 1.5: Schematic representation of the three modes observable in a p-type MIS capacitor a) accumulation, b) weak inversion and c) strong inversion.

In real MIS/FETs, there are multiple deviations from the ideal behaviour described previously. Firstly, the metal's work function and the Fermi level of the semiconductor may not be of equivalent energy meaning that the semiconductor's bands could already be bent when no voltage is applied to the semiconductor. Subsequently this means that there is a given gate voltage where the bands are made to be flat, namely the Flat Band Voltage[10] (V_{FB}).

In addition, interface might not be of the highest quality and the energy potential created by trap states at the insulator/semiconductor interface or in the bulk of the semiconductor will also have to be compensated by the applied V_{GS} in order to achieve operation conditions. The sum of these voltage deviations is defined as the threshold voltage (V_{th}), which indicates the voltage where significant conduction at the interface is achieved (discussed later in this chapter).

1.1.4 Organic transistor theory - regimes of operation

Figure 1.6 illustrates the previous principle applied to a p-type OFET. When no voltage is applied to the gate ($V_{GS} = 0 V$) and to the drain ($V_{DS} = 0 V$), the charge carriers (holes in the case of a p-type) are spread all across the bulk of

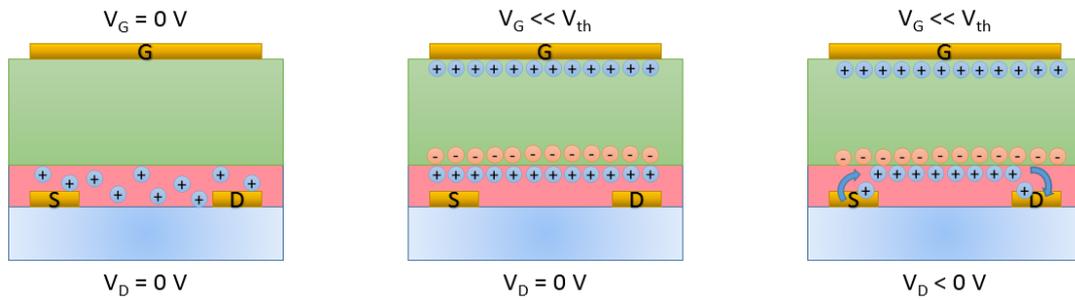


Figure 1.6: Simplified representation of a p-type organic transistor behaviour with the application of specific voltages at the different electrodes.

the semiconductor. When the gate voltage is beyond the threshold voltage the accumulation of holes at the interface forms a conductive channel where the current can flow if a voltage is applied across the source and drain electrodes.

The density of accumulated charge carriers in the channel is directly controlled by the vertical electric field applied to the semiconductor ($V_{GS} - V_{th}$). However, while the transistor is in operation a voltage is also applied to the drain electrode. Meaning that the field is not constant from the source to the drain and thus that the accumulation of charge carrier in the channel is reduced the closer it is to the drain. This subtlety is extremely important as it is the origin of two different operating regime in field effect transistors : linear and saturation regime.

When the drain voltage is negligible compared to the vertical field ($V_{DS} \ll V_{GS} - V_{th}$) the deformation of the channel is also considered negligible and the density of carrier is considered unchanged along the length of the channel (the length L is referring to the distance between source and drain; first panel of Figure 1.7).

The density of carriers close to the drain will steadily decrease with an increase of V_{DS} thus resulting in a localized decrease of the channel thickness until a specific voltage $V_{DS sat}$ is reached. At this exact voltage the channel reaches a so called “pinch-off” condition where the layer of carrier is at the limit of the drain electrode region. When V_{DS} is increased above $V_{DS sat}$ the pinch-off region moves further down the length of the transistor. However, the voltage at the pinch-off point remains equal to $V_{DS sat}$ which produces a constant saturation current ($I_{Dsat}(V_{GS})$) as long

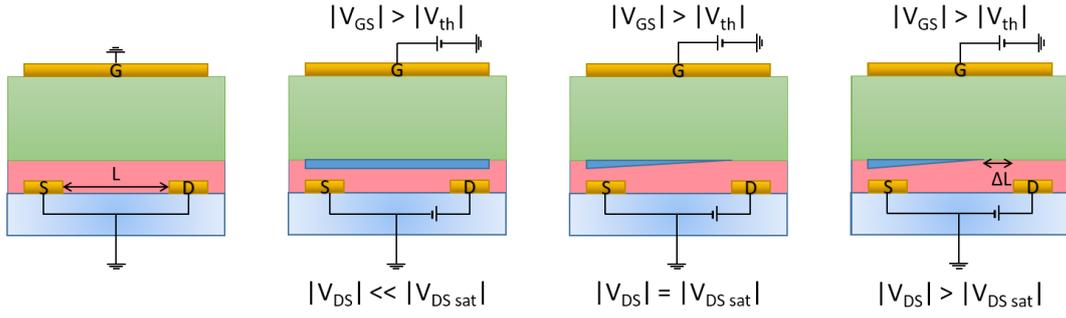


Figure 1.7: Evolution of channel thickness with the increase of drain voltage.

as ΔL (length of the channel free region) is much lower than L [11]. A more visual representation of this explanation may be found in Figure 1.7.

The theoretical current passing through an ideal field effect transistors is described by Equation (1.1):

$$I_{DS}(V_{GS}) = \frac{W}{L} \mu_{eff} V_{DS} Q_{inv}(V_{GS}) \quad (1.1)$$

With W and L respectively the width and length of the transistor in metre (m); μ_{eff} the effective mobility of the charge carriers in the channel (in $cm^2.V^{-1}.s^{-1}$) and $Q_{inv}(V_{GS})$ the variation of charge at the interface with the applied gate voltage (C/cm^2). This equation was originally developed in the case of MOSFET transistors but may be applicable to organic structures if the inversion charge is replaced with an accumulation charge (Q_{acc}). Practically it is simplified to Equation (1.2) and Equation (1.3) that describe the current flowing in the transistor for both linear and saturation regime.

$$I_{DS \text{ lin}} = \frac{W}{L} \mu_{eff} C_i V_{DS} \left(V_{GS} - V_{th \text{ lin}} - \frac{V_{DS}}{2} \right) \quad (1.2)$$

$$I_{DS \text{ sat}} = \frac{W}{2L} \mu_{eff} C_i V_{DS} (V_{GS} - V_{th \text{ sat}})^2 \quad (1.3)$$

Where C_i is the surface capacitance of the dielectric layer in Farad per square centimetres ($F.cm^{-2}$). However, these equations only stay true if the transistor is in strong accumulation (ie : above V_{th}) and if there is no strong deviation from ideality. For an extended demonstration of these two equations in MOSFET structure we refer the reader to *Physics of semiconductor devices*[10] which discusses the fundamental principle of semiconductor materials applied to electronic devices.

1.1.5 Basic Theory - extractions of the key parameters

The basic characterisation of a transistor typically relies on two different measurements:

Transfer measurement This measurement consists in applying a fixed drain voltage, either below or above $V_{DS\ sat}$ and a V_{GS} sweep. The gate voltage sweep may be unidirectional or measured in both direction of gate voltage to yield information about any potential hysteresis. In logarithmic scale these curve are separated in three region (Figure 1.8 a)): OFF region where the channel is not present (1), subthreshold region where the channel is created (2) and the ON region where the channel is established (3) (Figure 1.8 a)).

Output measurement At a fixed gate bias, the drain voltage is increased from zero to a maximal bias. This measurement illustrate the transition from linear to saturation regime. Generally multiple curves with different V_{GS} are plotted on the same graph to evaluate the evolution of the drain current in saturated region (Figure 1.8 b)).

As stated previously these two sets of measurements are at the core of the transistor's characterisation since most of the key parameters defining the device can be extracted from them. Threshold voltage (V_{th}), mobility (μ_{eff} or μ_{FE} in the case of non idealities), ON-OFF current ratio (I_{ON}/I_{OFF}), subthreshold swing (SS) and contact resistance (R_C) are some of the most commonly used parameters to benchmark the performance of a transistor.

The first four parameters are generally obtained with the help of transfer curves and various types of extraction methods. The most simple parameter to extract from these curves is I_{ON}/I_{OFF} : the ratio between the current in the OFF region of

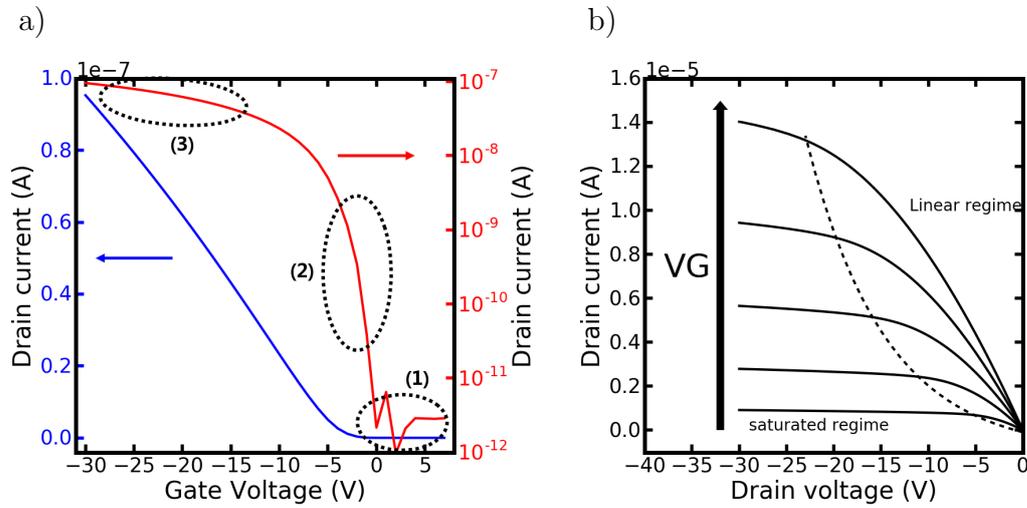


Figure 1.8: a) Transfer curve measurement of a standard transistor in linear regime plotted in linear and semi-logarithmic scale b) output curve measurement of the same transistor at increasing V_{GS} (the dashed line represent an approximate separation between the linear and saturated region respectively on the right and left hand-side).

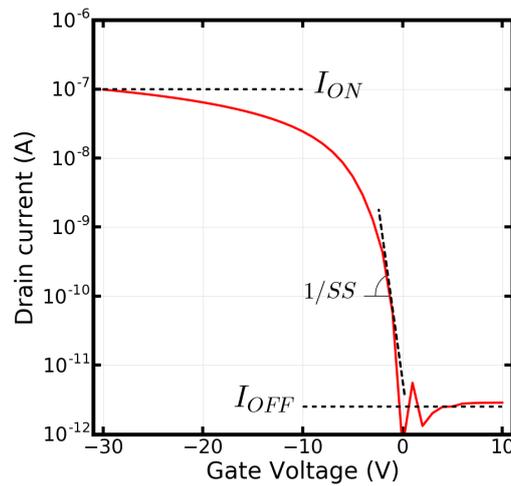


Figure 1.9: Extraction of I_{ON} , I_{OFF} and SS from a transfer curve in semi-logarithmic scale.

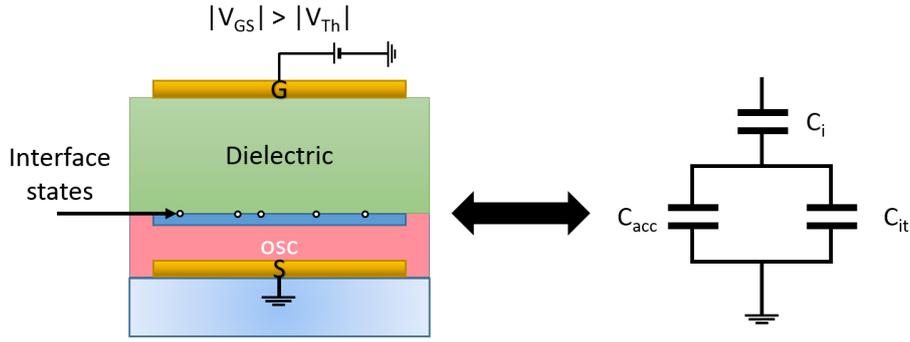


Figure 1.10: Electrical equivalence of an accumulated organic transistor with C_i the insulator’s capacitance, C_{acc} the accumulated channel capacitance and C_{it} the localized trap states.

the transistors and in the ON region, it is expressed in decades. As transistors are generally used as switches in circuits, a large ON/OFF ratio allows for a sharper distinction between the two states of the device.

The subthreshold swing (SS) describes the “speed” at which the transistor switches from OFF to ON. It is extracted from the inverse of the slope in the sub-threshold region (Figure 1.9) and is directly impacted by the quality of the transistor’s interface. In MOSFET devices, the equation of the subthreshold swing (Equation (1.4)) is impacted by the gate capacitance, the depletion layer (C_D), the capacitance of the interface traps (C_{it}), q the elementary charge, k_b the Boltzmann constant ($J.K^{-1}$) and the temperature (T).

$$SS = \ln(10) \left(\frac{k_b T}{q} \right) \frac{C_i + C_{it} + C_D}{C_i} \quad (1.4)$$

As such, the theoretical limit for a fully depleted ($C_D = 0$) and defect free transistor ($C_{it} = 0$) at ambient temperature is approximately 60 mV.dec^{-1} . Contrary to MOSFETs, organic transistors cannot operate in depletion mode and thus the depletion layer capacitance (C_D) can be removed from this equation.

The most common extraction method for threshold voltage and mobility is the Extension of Linear Regime (ELR) method or transconductance method. Transconductance (g_m) is defined as the differential between the drain current and applied gate voltage at a given drain voltage (Equation (1.5)) and yields a specific mobility

dubbed Field Effect mobility (μ_{FE}). In ideal cases $\mu_{FE} \approx \mu_{eff}$ when the device is in strong accumulation (ie : $V_{GS} > V_{th}$). However, because g_m is calculated from the measured drain current, deviation from ideality can be expected and the nuance between the two mobilities is important. To simplify the comprehension, we can say that μ_{eff} is a material parameter and is constant with V_{GS} and μ_{FE} is a device parameter which is V_{GS} dependent. In linear regime the transconductance is written as following :

$$g_m = \left(\frac{\partial I_{Dlin}}{\partial V_{GS}} \right)_{V_{DS}} = \frac{W}{L} \mu_{FE} C_i V_{DS} \quad (1.5)$$

In ideal transistors, once the channel is created the g_m should remain constant. In practice, the drain current is not always linear due to various factors (contact resistance, mobility dependence with V_{GS} ect...)[12]. In order to extract V_{th} and μ_{FE} a linear regression is made on the drain current around the small window of peak g_m as illustrated in Figure 1.11 a). Equations (1.6) to (1.8) describe the extraction of $\mu_{FE lin}$ and V_{th} ; with A and B being respectively the slope and intercept of the regression.

$$I_{DS reg} = g_m \left(V_{GS} - V_{th} - \frac{V_{DS}}{2} \right) \equiv A V_{GS} + B \quad (1.6)$$

$$\mu_{FE lin} = \frac{L A}{W C_i V_{DS}} \quad (1.7)$$

$$V_{th} = -\frac{B}{A} - \frac{V_{DS}}{2} \quad (1.8)$$

ELR method may also be used when the transistor operates in saturation. Since the current is proportional to $(V_{GS} - V_{th sat})^2$, plotting the square root of the drain current versus the gate voltage allows for a simple reading of the V_{th} when this linear regression intercept with the abscissa (Figure 1.11 b)). Mobility may then be calculated using Equation (1.9) with A the slope of the linear regression.

$$\mu_{FE sat} = \frac{A^2}{\frac{W}{L} V_{DS} C_i} \quad (1.9)$$

Because of the potential flaws of this technique, other extraction methods have been proposed in the literature. In this work, we routinely performed extractions via the ‘‘Current to square root of the transconductance ratio’’ method (Usually shortened to Y method or YFM) alongside the ELR method to verify the validity of our results. The Y method was proposed to compensate the effects of potentially large R_C on

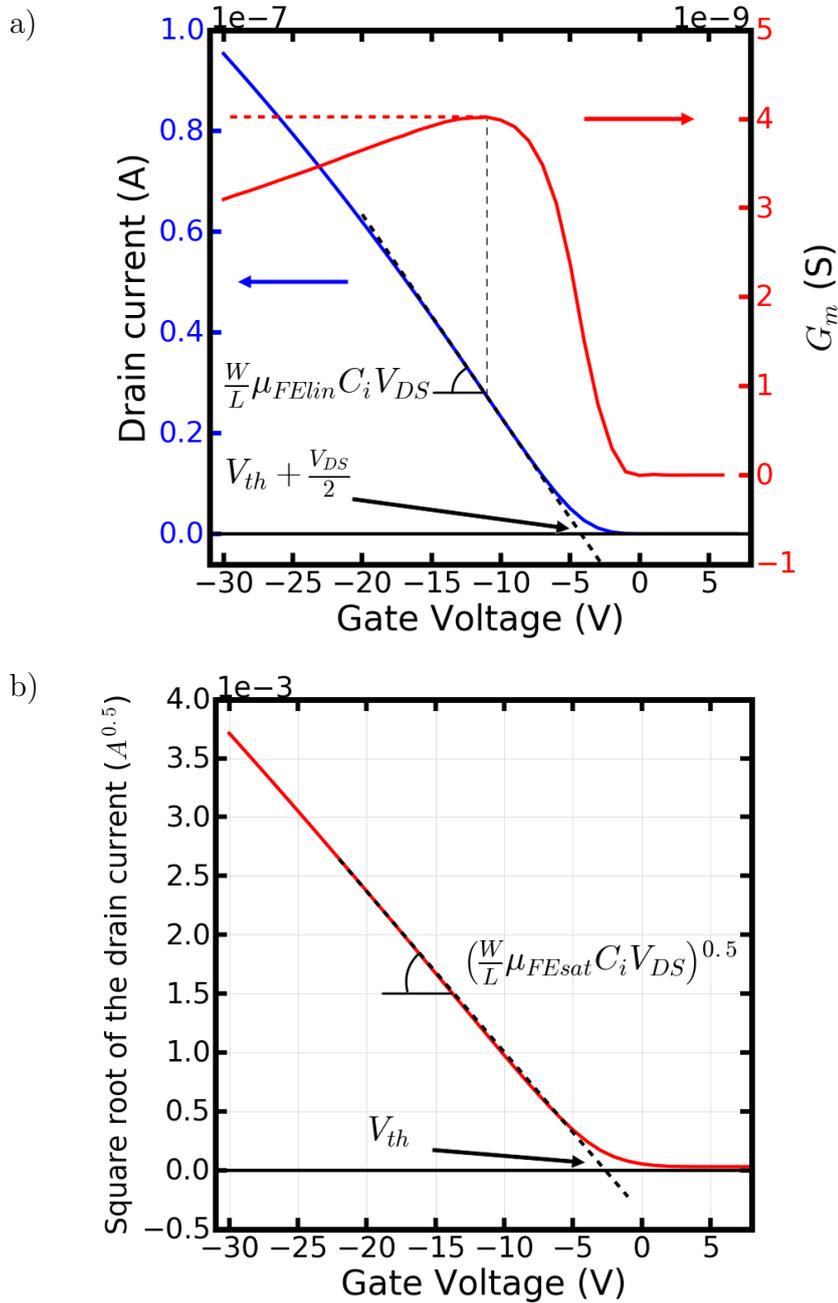


Figure 1.11: Extraction of V_{th} and μ_{FE} with a) the ELR method in linear regime at the maximum of g_m (with the dashed red line representing an ideal transconductance) and b) the ELR method in saturation regime.

extracted threshold and mobility. The full methodology for the YFM have been proposed by G. Ghibaudo[13] and relies on Equation (1.10):

$$Y = \frac{I_{DS}}{\sqrt{g_m}} = \sqrt{\frac{W}{L} \mu_0 V_{DS} C_i \cdot (V_{GS} - V_{th})} \quad (1.10)$$

With μ_0 the low field mobility, representing the intrinsic mobility of the charge carriers in the material. Similarly to the ELR in saturated regime the value of threshold voltage is obtained when the linear regression of the Y plot crosses the abscissa.

We discussed here two main extraction methods used throughout our study but it should be noted that there is a plethora of techniques proposed in the literature. However, we do not aim to explain each and every methodologies available and we refer the interested reader to the work of Ortiz et al[14] which regroups most of the threshold voltage extractions identified in the literature.

Finally, the last key parameter to consider when benchmarking a FET is the value of series resistance when accessing the channel. The schematic electrical representation of a field effect transistor in Figure 1.12 a) describes the transistor as a variable resistance ($R_{channel}$) coupled to two static resistance representing the contact between source/drain and the semiconductor (R_C). Ideally the charge injection from the source and drain into the channel should behave as a ohmic contact. Practically, the metal's work function and the HOMO level of the semiconductor may not exactly be matching and thus may induce a Schottky barrier preventing the acces to the channel at low V_{DS} .

In organic field effect transistor Self-Assembly Monolayers (SAMs) are usually applied to the contacts prior to the semiconductor deposition in order to finely tune the connection between the two materials. A qualitative technique to evaluate the presence of a significant R_C is to observe the output curves of the transistor. If a Schottky barrier is present, the current at low V_{DS} will display a non linearity generally dubbed as a "S-shape" similar the one present in the red curve of Figure 1.12 b).

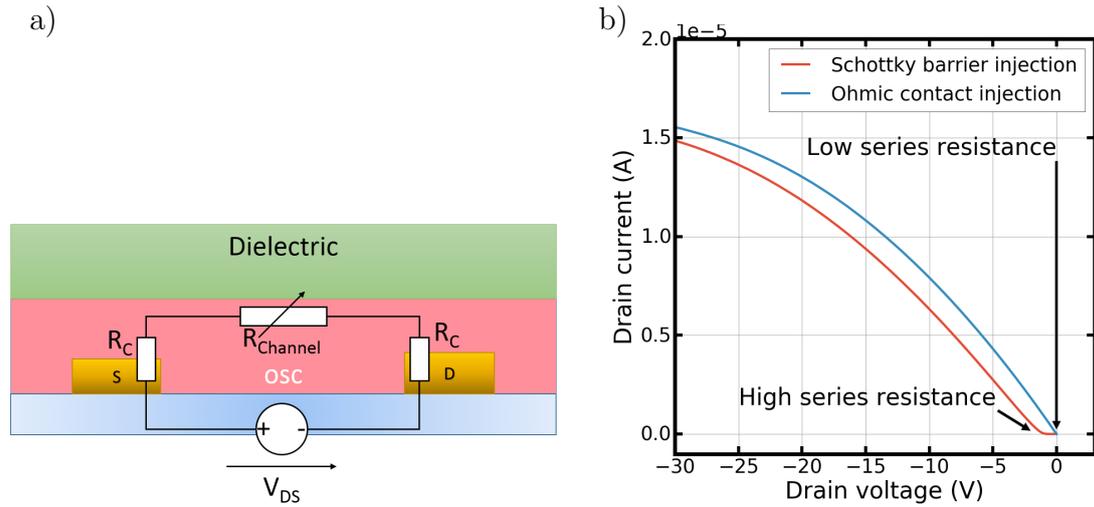


Figure 1.12: a) Electrical representation of the total channel resistances b) ideal injection and Schottky barrier impact on output curves.

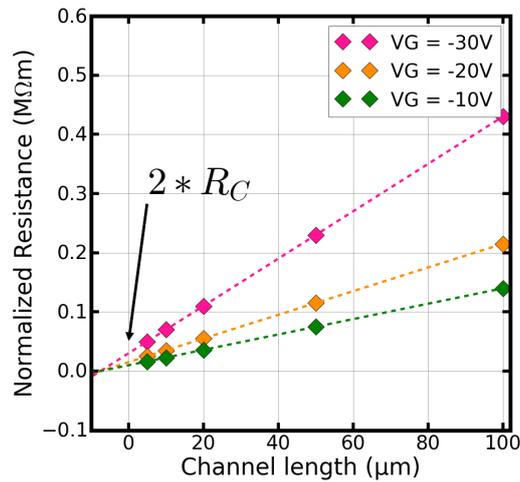


Figure 1.13: Example of transfer line method for the extraction of contact resistance.

To achieve a quantitative characterisation of the access resistance, one may resort to the Transmission Line Measurement (TLM) which postulates that global resistance of the channel consists of two components: the channel resistance and the contact resistance [15]. By measuring the output current of transistors with identical width and increasing length we can plot the total resistance of the transistor at a given V_{GS} . With a simple linear regression of these resistance versus the length of the transistor, we can find at the ordinate an hypothetical transistor without channel, but with two contact resistance in series and thus extract an average contact resistance for the desired transistor structure (Figure 1.13).

Conclusion 1.1 (Organic Transistors) *Organic semiconductor based transistors are fairly young when compared to their inorganic counterparts but thanks to simpler chemical synthesis and processing capabilities there is a plethora of materials and structures possible for OTFTs. In order to adequately characterise them, organic electronics borrows from the tremendous work that have been produced in the past century in order to establish microelectronic as we know it today.*

1.2. LOW VOLTAGE FOR ORGANIC THIN FILM TRANSISTORS

1.2.1 Physical dependence of operating voltage

From early on the main focus in organic electronics was to improve the semiconductor, to increase its mobility, stability and reproducibility. As a result, the trend of publication in the literature reported a steady increase in current and operating speed, getting closer to the performances of state of the art amorphous silicon FETs[8]. However, operating voltage of such transistors remained well above the microelectronic standards with the first reports concerning the reduction operating voltage in organic transistor published around the year 2000[16, 17]. Nevertheless, with the rise of wearable devices they were many incentive to further reduce the operating voltage in order to be compatible with the classic microelectronics.

To reduce the operating voltage one must first defines it, the general consensus is that the transistor may be considered in operation when V_{GS} is approximately three times superior to V_{th} . Despite being observed experimentally, the classic definition of threshold voltage does not exactly apply to the organic transistor[18] and as such its physical origin is still up to debate in OFETs. To gain insight on the expected behaviour of V_{th} in our structure, we can study two different approaches inspired by the classic microelectronics.

First, a classic silicon MOSFET approach where the threshold voltage is described

as the sum of V_{FB} representing the mismatch between the gate metal's work function and the semiconductor's HOMO level[19]; Ψ_s the semiconductor's surface potential; and the summed ratio of Q_{inv} the inversion charge of carriers at the interface; Q_D the charge of the depletion layer and N_{it} the density of interface states (Equation (1.11)) over C_i .

$$V_{th} = V_{FB} + \Psi_s + \frac{Q_{inv} th + Q_D + q N_{it} \Psi_s}{C_i} \quad (1.11)$$

In the case of OFETs, the transistor operates in accumulation, meaning that Q_{inv} should be modified to an accumulation charge (Q_{acc}) and that there is no depletion layer rendering Q_D null. The threshold voltage in organic transistor could thus be described with Equation (1.12):

$$V_{th} = V_{FB} + \Psi_s + \frac{Q_{acc} th + q N_{it} \Psi_s}{C_i} \quad (1.12)$$

The second approach is based on the Fully Depleted Silicon On Insulator (FDSOI) MOSFET structure. As its name suggest it operates in full depletion of the semiconductor meaning that these devices only operates in inversion. To an extent they behave similarly to OFETs (non-doped and of opposite semiconductor type) as they can only operate in accumulation. Generally, it can be stated that in this type of structure, the drain current is proportional to the gate to channel capacitance (C_{gc})[20]. This capacitance is defined as the variation of the inversion charge (or accumulation in the case of OFET) with the applied gate voltage (Equation (1.13)).

$$C_{gc} = \frac{dQ_{inv}}{dV_{GS}} \quad (1.13)$$

And in the presence of interface traps can be formulated as Equation (1.14)[20]:

$$C_{gc}(V_{GS}) = \frac{C_i \beta' Q_{inv}(V_{GS})}{\beta' Q_{inv}(V_{GS}) + C_i} \quad (1.14)$$

$$\beta' = \frac{q}{\left(1 + \frac{C_{it}}{C_i}\right) k T} \quad (1.15)$$

In FDSOI structures, V_{th} is reached when C_{gc} achieves half of the insulator's capacitance value. From Equations (1.14) and (1.15) we understand that this values of voltage is directly impacted by C_i and C_{it} .

With the help of these two descriptions of the threshold voltage, we can understand that the main factors that could effectively lower the operating voltage in organic

transistors would be the improvement of the interface quality (density of localized state) and/or an increase of the insulator layer's capacitance. Both these approach have already been implemented in inorganic transistors with the use of improved processing, reduction of oxide thickness and implementation of new materials. Over the last years similar solutions have been proposed for their organic counterparts with success regarding the reduction of operating voltage.

1.2.2 Interface

Having an adequate interface quality has always been a critical factor in transistors. As seen from Equations (1.4) and (1.11), the density of interface states influences the operating voltage of the transistor as it impacts both threshold voltage and subthreshold swing. Practically it is the ratio of C_{it} over C_i that dictates V_{th} and SS . As such, the capacitance induced by the trap states should always be considered with respect to the insulator's capacitance.

The interface quality can be impacted by multiple external factors during processing, alongside with some intrinsic material properties[21]. To limit the detrimental effects and variability introduced by environmental conditions, the fabrication of OFETs is generally conducted in a clean room with controlled temperature and humidity levels. However, this only limits interface states introduced by external contaminants and in order to further improve interface quality one must also be concerned by the purity and homogeneity of the materials used and, in some structures, the compatibility between the semiconductor and dielectric.

To this day, small molecules (mainly pentacene derivative) are some of the most performing organic semiconductors[22]. However, they are highly dependent on molecular orientation and homogeneous crystalline structure for their remarkable performance and are mainly deposited via evaporation process in order to achieve this essential ordering.

Despite the good quality of such vapour-deposited semiconductor layers, the

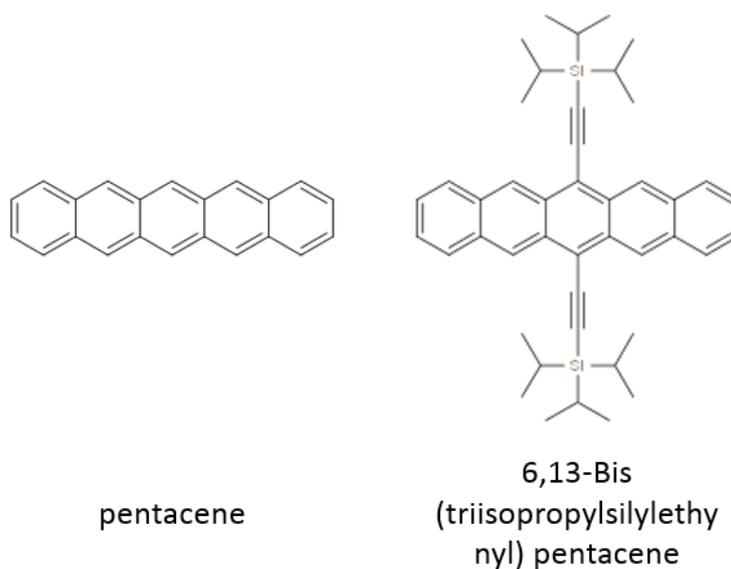


Figure 1.14: Topological depiction of the pentacene and TIPS-pentacene molecules.

research interest slowly shifted to solution processed materials in order to take advantage of the various large area printing technologies compatible with organic electronics. Because pentacene molecules display poor solubility in most organic solvents (ie: mainly soluble in hot chlorinated benzenes) it could not be directly compatible with printing technologies. However, pentacene derivatives with higher solubility have been proposed in the literature[23]. As a result the 6,13-Bis (triisopropylsilyl)ethynyl pentacene (Figure 1.14; generally shortened to TIPS-pentacene) is now one of the most commonly used material for solution processed small molecules. The introduction of the triisopropylsilyl ethynyl side chains allow for a higher solubility[24]. However, this increased processability comes at a cost. As the side chains force an non-optimal orientation onto the pentacene backbone, the performances of this material are slightly lower than the peak performance of its parent molecule.

In 2009 an US patent[25] proposed the use of additives to counteract this phenomenon, by introducing polystyrene in small proportion to the semiconductor the global performance of the TIPS-pentacene was greatly improved. This blend exhibited high hole mobility thanks to the segregation of the two materials and the

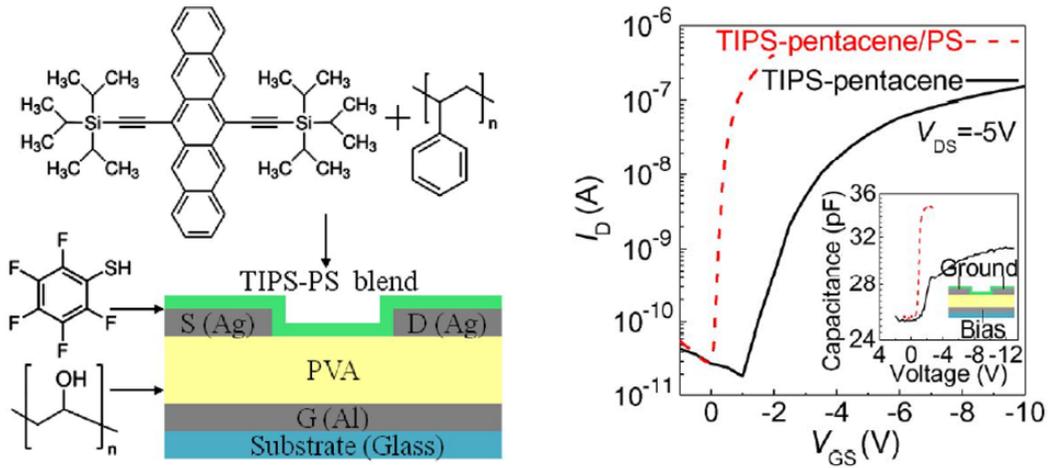


Figure 1.15: Low voltage transistor and comparative transfer curve with and without polystyrene additive reproduced from the work of L. Feng et al[27]

difference of crystallization rates, as the pentacene rapidly crystallized it assembled at the interface before the polymer[26]. As result multiple proofs of concept for low-voltage OFETs where proposed in the literature using the previously cited blend of polymer and small molecule semiconductor[27–29] (Figure 1.15).

1.2.3 Ultra-thin dielectrics

As prior mentioned, another possibility to reduce the operating voltage of FETs is to increase the capacitance of the gate dielectric. This increase would translate in a reduced threshold voltage, a steeper subthreshold swing and improved drain current (Equations (1.2) and (1.3)). If we consider the surface capacitance of an insulating layer (Equation (1.16)), we notice that since the vacuum permittivity (ϵ_0) is a physical constant, the thickness (d_i) and the dielectric constant material (κ ; also referred to as relative permittivity ϵ_r) are the only two tunable parameters that can improve the capacitive coupling of the dielectric.

$$C_i = \frac{\epsilon_0 \kappa}{d_i} \quad (1.16)$$

When the reduction of the dielectric thickness was pushed to the extreme, it led to the discovery of SAMs dielectrics and their first application in 1993[30]. This

Low-V thin film transistors:

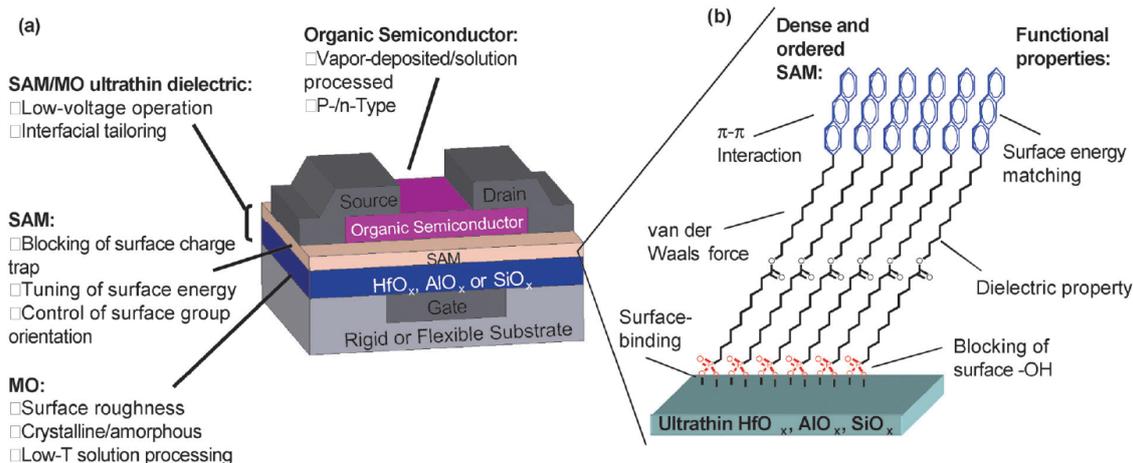


Figure 1.16: (a) Schematic of SAM/metal oxide hybrids as ultrathin dielectrics and interface for low-voltage OFETs. (b) Typical p-s-PA SAM on metal oxides with optimized dielectric and interfacial properties (reproduced from [32])

technology consist in grafting a layer of auto organized molecules on a gate electrode presenting a native oxide or an ultra thin deposited oxide. This effectively yields an insulating layer with a thickness in the nanometre range thus providing extremely high C_i . Although the actual measured capacitance for these layer are often considerably lower than the one expected with Equation (1.16) since other phenomena may occur at such low thickness (series resistance, Fermi-level pinning, tunnelling).

As there are many types of SAMs dielectrics that have been investigated and that there are various chemical functions which may be added or removed from the molecules to suit any need, it is hazardous to give an exhaustive description of their structures [31]. However, there are some common traits that can be found in most of the reported materials: a grafting site bounding to the oxide layer, an alkyl chain granting insulating properties and in some case a functional group for improved interaction with the semiconductor (Figure 1.16).

From early on, this approach enabled the fabrication of OFETs with operating voltage in the range of the couple of volts [33–35]. Despite impressive reported performance, there are some general concerns regarding this technology, for example: high leakage, lack of flexibility and lack of compatibility with large area processing.

Although some articles addressed these issues to some extent[32, 36, 37] most of the SAMs OFET discussed in the literature are produced on solid substrate thus limiting the investigation of prior mentioned concerns. A recent advance in this field can be attributed to the work of Zschieschang et al [38] as they reported the fabrication of below-one-volt transistors with both types of semiconductors thus enabling the production of low voltage organic circuits.

1.2.4 High permittivity dielectrics

Finally, another possibility to maximize the gate capacitance is to increase the permittivity/dielectric constant of the gate insulator. As previously, this approach have already been studied and implemented in microelectronics. As the thickness of the SiO_2 became thinner and closely reaching 2 nm tunnelling effects drastically increased the gate leakage. To circumvent this problematic the introduction of high- κ materials (relative to SiO_2) had been advised as it would allow for equivalent or improved gate capacitance with thicker oxide thickness. A similar problematic have been observed in common solution processed dielectrics as an extended reduction of thickness led to apparition of pinholes in the insulator layer thus drastically increasing leakage and lowering yield.

Historically the term high- κ originates from the microelectronics were it referred to any insulator materials with a higher dielectric constant that of the silicon dioxide($\kappa_{\text{SiO}_2} = 3.9$). In new high performance inorganic transistors, the replacement of choice for SiO_2 is the hafnium dioxide (HfO_2) with a permittivity of approximately 25[39].

There are multiple materials, organic or inorganic, that have high enough permittivity to be considered as high- κ dielectrics. However, some concerns regarding their implementation in transistors have been raised in the literature as multiple articles reported drastic mobility loss when the high- κ materials was directly in contact with the semiconductor. Most of these reports where reporting bottom gate transistors

with highly structurally dependent semiconductors (ie: crystalline small molecules) which sparked some controversy about the dielectric of choice in OFETs[40] (low- κ versus high- κ). However, the same behaviour have been demonstrated on single mono-crystal transistors which should not suffer from the structural impact of a bottom dielectric[41].

This detrimental effect have been theorized and attributed to a broadening of the density of states by the localized dipoles of high permittivity materials by Richard et al[42]. However, this interaction should be short ranged (ie: nanometres) and could be prevented by an ultra-thin low- κ layer between the semiconductor and the high- κ .

To circumvent this detrimental effect, two general structure have been proposed :

Nano-composites Generally composed of extremely high- κ inorganic particles suspended in a low- κ polymer matrix[43].

Bilayers Referring to the deposition of a thin low- κ buffer layer between the semiconductor and the high- κ material.

Both these dielectric structures may yield high capacitance from solution processed layers in the acceptable range of thickness for printed organic transistors. Consequently, the application of such materials to the transistor structure have been reported to enable lowered operating voltage[28, 44–47].

Both these methodologies are not without drawbacks as high- κ material generally exhibit higher conduction and lower stability than their low- κ counterparts.

In the case of nano-composite dielectrics, the main concern is generally related to the particle load in the polymeric matrix. When the quantity of particles in a medium is increased there is a chance to cross the percolation threshold. When above this critical load there is a high probability to create large particle clusters spanning across the whole dielectric thus drastically increasing leakage and other detrimental effects[48].

In the bilayer structure the problematic mainly concerns to the homogeneity of the thin low- κ layer. Since pinholes may form when it reaches critical thickness, the risk of leakage is increased with ultra-thin buffer layers. Additionally, the monolithic high- κ layer may cause some flexibility issues as some oxide can be prone to cracks. To retain most of the advantages granted by organic electronics (ie: solution processing and flexibility) the choice of high- κ material in bilayers for OFETs generally leans toward polymeric material approach as was demonstrated by li et al[49]

Conclusion 1.2 (Low voltage organic transistors) *The reduction of operating voltage in organic transistors may be enabled either by the reduction of parasitic capacitance (ie: traps) and/or the increase of the gate capacitance. The former requiring chemically optimized materials and the later requiring either the implementation of ultra thin dielectrics or high- κ materials.*

1.3. THIS THESIS

1.3.1 State of the art in low-voltage OTFTs

All technological approaches discussed in the prior section of this chapter were successfully reported in the literature. In Table 1.1 we listed some of “the state of the art” transistors implementing one or multiple techniques for operating voltage reduction. We can see that most of the solution proposed in this table display V_{th} in the range of the volt or below which is enough to fall into the “low-voltage” category. If we consider the data gathered in this table, it is noticeable that a low threshold voltage value was enabled either by a high C_i or a low N_{it} .

In Table 1.2 we propose a summary of the general strengths and weaknesses concerning the average transistor when implementing one of the prior discussed technologies. This table, based on a selection of reviews concerning the topic[31, 52–54], aims to reflect the global state of each types of low-voltage transistor technologies. However, it remains a gross generalization and does not depict the reality of all study

Table 1.1: Example of state of the art low-voltage transistors integrating one or more operating voltage reduction technique described in this chapter (The * following some values indicates that they were calculated from data and not directly provided in the article).

Technology	Dielectric structure	Total thickness (nm)	C_i ($nF.cm^{-2}$)	κ	V_{th} (V)	μ_{eff} ($cm^2.V^{-1}.s^{-1}$)	SS ($mV.dec^{-1}$)	N_{it} (cm^{-2})	I_{ON}/I_{OFF}	I_G (A)	Ref
SAM dielectric	AlOx/SAM	5.7	700	4.5*	-0.5	0.4	90	2.28.10 ¹² *	10 ⁵	10 ⁻¹³	Zscheschang et al[38]
High- κ oxide bilayer	Cytop (35 nm)/HfO ₂ - Al ₂ O ₃ (33 nm)	68	40.8	3.1*	-1.2	1.4	320	1.10.10 ¹²	10 ⁵		Jia et al[50]
Bilayer and nano-composite	PVP(25 nm)/BST- P(VDF-HFP)	178	64.4	12.9*	-0.5	0.06	169	7.47.10 ¹¹ *	10 ³	10 ⁻⁰⁹	Faraji et al[44]
Bilayer	PS (2.8 nm)/P(VDF- TrFE-CFE) (160 nm)	162.8	26	4.8*	-2.5	0.62	330	7.44.10 ¹¹ *	10 ⁴		li et al[49]
Bilayer and improved interface	PVC (114 nm)/P(VDF- TrFE-CFE) (250 nm)	364	46.3	19.0*	-0.8	0.12	64	1.92.10 ¹⁰	10 ⁶		Zhao et al[51]
Improved interface	PVA	407	12.2	5.6	-0.5	1	100	5.26.10 ¹⁰ *	10 ⁵	10 ⁻⁰⁹	Feng et al[27]

Table 1.2: General strengths and challenges of the low-voltage technologies for organic transistors.

	Optimized interface	SAMs dielectric	Nano-composite	Bilayer
Interface quality	+++	+	++	++
Gate capacitance	-	+++	++	++
Robustness	++	-	+	+
Flexibility	++	-	+	++
Printable	+	-	++	++
Stability	++	++	-	-
Challenges	<ul style="list-style-type: none"> • Processing conditions • Potential structural constraint 	<ul style="list-style-type: none"> • Leakage • Printability • Low flexibility 	<ul style="list-style-type: none"> • Leakage through percolation • Homogeneity • Frequency stability 	<ul style="list-style-type: none"> • Hysteresis • Frequency stability

in each category. As such it should rather be considered as reporting potentially improvable features rather than to be an exact depiction of the technology's capability.

From these observations, we considered that the integration of a high- κ in a bilayer structure was the most attractive candidate for potentially large area and flexible applications since this type of material is easily solution processable in the adequate range of thickness and should exhibit good flexibility. To retain most of the mechanical properties in the final transistor structure we chose to implement a polymeric material as the high- κ component of our bilayer. We will further elaborate on the device frame and selected materials in the following section.

1.3.2 Materials and structure selected for OTFT fabrication

In order to adequately evaluate and compare the properties of a chosen dielectric, the intrinsic performance of the semiconductor layer should remain as constant as possible and the overall properties of the transistor be highly reproducible. Considering that requirement, we made several choices regarding materials and structures for the transistor fabrication.

The transistor's processing was carried out on flexible substrate with lithographed gold contacts to minimize the disparity potentially introduced by printed electrodes. Gold was selected for its stability and work function (5.1-5.47 eV depending on measurement method) which can be finely tuned by the addition of a SAM (not a dielectric in this particular case). In bottom gate transistors, the semiconductor is deposited directly onto the dielectric, thus conforming to the specificity of its surface. To avoid the potential variability introduced into the OSC, we preferred a top-gate transistor structure (Figure 1.4 a)) which would allow for a consistent deposition surface.

In order to avoid mobility inconsistencies arising from highly crystalline dependent small molecules, a semi-crystalline polymer semiconductor has been preferred in order to ensure stable and reproducible performance. We chose a commercially available package of material as the main body of our transistor structure. The **lisicon®** package, purchased from Merck (Germany), offers a selection of contact SAMs, polymeric semiconductors and low- κ dielectrics with various formulations or dilutions for the desired requirements. We used the following materials in our transistor structure:

M001 Self assembled monolayer solution used for tuning gold contacts work function and facilitate the access from the metal electrode into the semiconductor thus allowing acceptable contact resistance (R_c).

SP400 Polymeric semiconductor (red color) with an average mobility of approxi-

ately $0.7 \text{ cm.V}^{-1}.\text{s}^{-1}$.

D320 Non fluorinated low- κ dielectric ($\kappa_{D320} \approx 2.2$), optimized compatibility with SP400 semiconductor.

Each of these material is pre-packaged in solution with adequate dilution for the desired processing technique (Spin-coating, screen printing, gravure printing ect...). The fact that the full composition of these materials is not disclosed by the manufacturer would arguably hinder the physical comprehension of some transistor's aspect. Nevertheless, theses phenomena are not in the core of our study and choosing these material allow for highly reproductive process and performance which will help to evaluate the impact of the high- κ dielectric in similar conditions when added into the transistor's stack.

The SAM deposition was carried out in a solution bath and spin-coating was used for the semiconductor and dielectrics. The full fabrication of the transistor is further discussed in Chapter 3

In this transistor configuration, the gate electrode was the last layer to be deposited. It could be either printed or vapour deposited from various inks or materials. However, some parasitic effects like diffusion in the dielectric, mechanical abrasion, uneven coverage or oxidation might be introduced by the use of inadequate inks or metals. To limit these issues we chose to use thermally evaporated gold as the gate electrode. The evaporation was carried out though a shadow mask in a vacuum evaporator using Joule's heating principle as potential degradation to the dielectric can be introduced by the electron beam method (further explained in the next chapter).

The final resulting structure should provide reproducible data for the accurate characterisation of high- κ materials in a bilayer transistor.

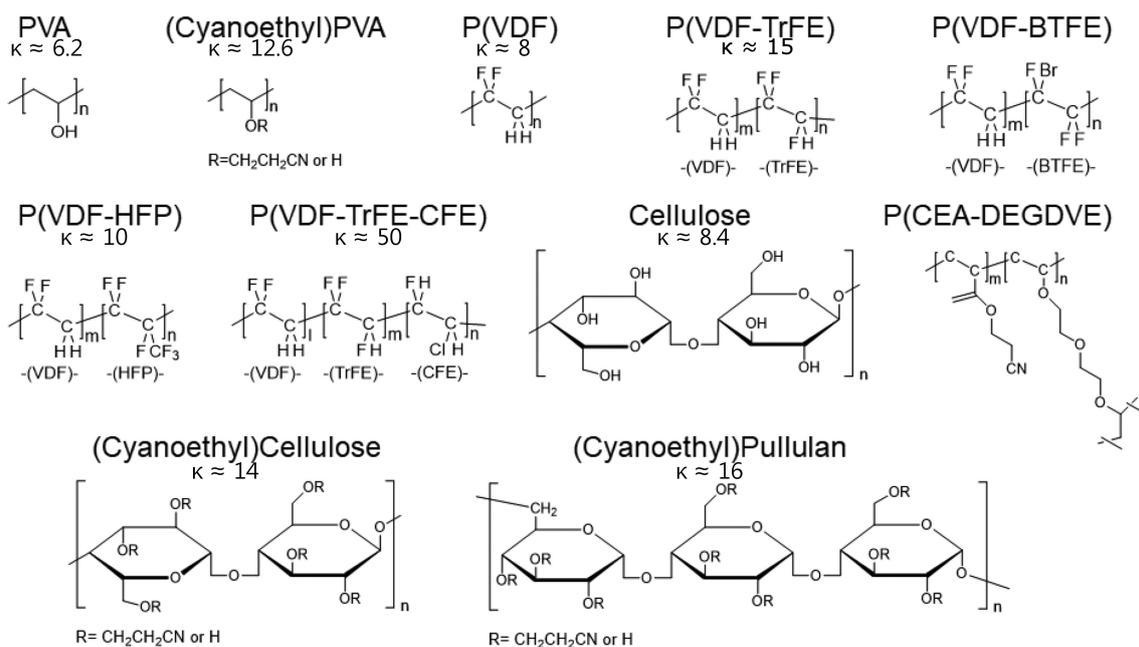


Figure 1.17: Example of polymers (with chemical structure) displaying dielectric constant higher than SiO_2 (adapted from [53]).

1.3.3 High- κ polymer and methodology

As stated previously and by silicon standard, for a material to be a high- κ , its dielectric constant should be higher than 3.9. However, because of their general structure organic polymers generally display low permittivity and only a small portion achieve high enough performance to fall in the high- κ category. We can see in Figure 1.17 that the general strategy for high permittivity polymers is to have either large amount of dipolar moment or atoms with large electronic cloud like fluorine.

Polyvinylidene difluoride (PVDF) and its derivative are a family of dielectric polymer with one of highest highest permittivity recorded in organic polymer ($> 10.\kappa_{D320}$) alongside with some other interesting dielectric properties like ferroelectricity, thermoelectricity and piezoelectricity. We chose to make them the main focus of our study and to evaluate their impact when introduced in a transistor structure. Multiple examples of low-voltage transistors implementing this type of material in a bilayer structure have already been reported with relative success in the literature[47, 55, 56].

However, instabilities are often reported in the final transistor and few in depth study of the dielectric materials are provided. We selected the terpolymers (polymer with three different monomer units) derived from PVDF as their properties can be finely tuned with composition and a such could be tailored to the transistor's needs.

The main goal of our study was to understand and link the dielectric properties of the high- κ polymers to the final transistor structure. To do so, we first studied the terpolymer material by itself in a simple Metal-Insulator-Metal (MIM) capacitor to probe its dielectric behaviour. We investigated the impact of various intrinsic and extrinsic parameters on the material's properties to have a deeper understanding of the terpolymer's dielectric behaviour. The high- κ material was then studied in a bilayer dielectric structure to evaluate the impact of a low- κ layer in series with the terpolymer. The geometry of the bilayer was modified to gain insight on the relation between its two constitutive dielectrics.

Once a good understanding of the dielectric was achieved, we began the integration of the high- κ into the transistor structure. In order to be able to understand the changes introduced by the bilayer dielectric we first established a reference devices based solely on the low- κ dielectric to act as a baseline for comparison purpose. After which we proposed and studied a first proof of concept for a low-voltage transistor based on a relaxor-ferroelectric bilayer. The introduced variation in operating voltage and hysteresis was studied with the help of variation of geometry identical to the one conducted one the capacitor structure. As a consequence we produced an optimized transistor structure capable of operating at low voltage while maintaining most of the baseline properties encountered in the reference structure.

Finally, we investigated the stability of the bilayer transistor regarding electrical stress as these device are generally used as part of larger circuits with constant electrical solicitations. Thus granting insight on the reliability of the fabricated low-voltage transistor. In a similar fashion to the rest of this work, the response of the bilayer was compared to a reference transistor, thus allowing to keep track of the modifications introduced by the high- κ polymer.

Conclusion 1.3 (This thesis) *To meet printing and solution processing requirements we chose to evaluate the implementation of a high- κ dielectric in the gate stack to produce low-voltage OTFTs. From the few high permittivity organic polymers available, we chose to study terpolymers based on the polyvinylidene difluoride (PVDF) as they are the most promising in terms of dielectric constant and tunability. However, these materials display various dielectric properties that may impact the transistor behaviour. We thus proposed to first study the terpolymer in a stand-alone structure (MIM capacitor) to evaluate and understand its properties. Then integrate it into the transistor stack and compare the resulting low-voltage TFT to a reference device. Finally we will study the reliability of the produced low-voltage transistor regarding electrical stress.*

Polyvinylidene fluoride based materials and their characterization in metal-insulator-metal capacitor structure

Introduction of a high- κ dielectric as gate insulator will drastically impact the OFETs characteristics. It is thus important to evaluate and understand the intrinsic properties of such materials before drawing questionable conclusions on observation of the rather elaborate transistor structure. This chapter thus aims to study high- κ polymers derived from PVDF in simple MIM parallel plate capacitors.

The first section of this chapter will begin with a brief introduction of the dielectric theory and the measurement of dielectric properties, to then be followed by a structural introduction of the Polyvinylidene fluoride based materials and origin of their specific behaviours. In a second section we will discuss relative the impact of chemical composition, bias, frequency and temperature on the characterisation the dielectric properties of the terpolymer. Finally the last section of this chapter will be devoted to the study of a possible linear window of operation in the terpolymer along with the impact of a low- κ layer addition to the high- κ .

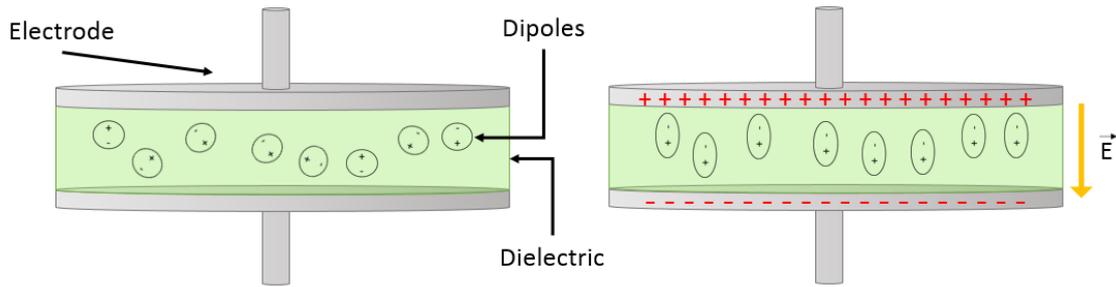


Figure 2.1: Schematic representation of the polarization phenomenon in a parallel plate capacitor (MIM structure).

2.1. POLARIZATION

2.1.1 Polarization, electrical displacement and permittivity

By definition, dielectrics/insulators are materials exhibiting poor electrical conductivity. Unlike metals, when placed in an electric field the current cannot flow through these materials as they do not possess free electrons capable of drifting across the bulk of volume. The bound charged elements present in any materials (atoms and electronic clouds) will however be displaced by the applied electric field[57]. Positive charged elements will be displaced in the direction of the field, and negative charged elements will be displaced in the opposite direction of the field. As a result electrically neutral molecules could present a local electric dipolar moment (Figure 2.1). At a larger scale this translate to a net bound charge (Q_b) at the surface of the material.

Polarization (\vec{P}) is the vector field that expresses the summed response of such dipole moments. It is defined as the “dipole moment per unit volume” ($C.m^{-2}$) introduced by these displacements and is described by Equation (2.1) with v a volume element in the material (m^3) and $\Sigma\vec{p}$ the sum of local dipolar moment in this volume ($C.m$).

$$\vec{P} = \frac{\Sigma\vec{p}}{v} \quad (2.1)$$

However, the polarization field only accounts for one part of the intrinsic field responding to the external applied electric field. Gauss’s law dictates that the free space charges response should also be considered. The electric displacement field

(\vec{D}) represents the summed effect of the free charges and the bound charges in an electric field as described by Equation (2.2).

$$\vec{D} = \varepsilon_0 \vec{E} + \vec{P} \quad (2.2)$$

Where \vec{E} is the electric field ($V.m^{-1}$) and ε_0 the vacuum permittivity or permittivity of free space ($F.m^{-1}$).

In the case of a linear, homogeneous and isotropic dielectric material, the polarization is proportional to and aligned with the electric field \vec{E} [58].

$$\vec{P} = \chi \varepsilon_0 \vec{E} \quad (2.3)$$

With χ the dimensionless material parameter called electric susceptibility. As a result the electrical displacement in an ideal dielectric is also proportional to the applied field (Equation (2.4)).

$$\vec{D} = \varepsilon_0 (1 + \chi) \vec{E} = \varepsilon_0 \kappa \vec{E} = \varepsilon \vec{E} \quad (2.4)$$

From this demonstration are defined two parameters : the absolute permittivity ($\varepsilon = \varepsilon_0(1 + \chi)$) and the relative permittivity (κ or ε_r also referred to as dielectric constant). Both these parameter are often simply called permittivity which may lead to some confusion. When “permittivity” will mentioned in this work it will further refer to κ as it is the most relevant parameter in our case and when ε is needed the denomination “absolute permittivity” will be specified.

By definition, permittivity should only be mentioned in the case of a linear, homogeneous and isotropic dielectrics[57]. However, for commodity, it is often used in the literature for non ideal materials despite its lack of physical veracity. Dielectric constants provided in the literature are generally extracted from discrete capacitance measurements (Equation (1.16)) in a linear window of operation. However, depending on the material and measurement conditions, the relationship between polarization field and electric field might not always be linear.

There are five types of microscopical polarization that can occurs in dielectrics[59]:

*CHAPTER 2. PVDF BASED MATERIALS AND THEIR
CHARACTERIZATION IN MIM CAPACITOR STRUCTURE*

- Electronic polarization** Deformation of an atom's electronic cloud, shifting the barycentre of negative charge from the positively charged nucleus (induced dipole, present in all dielectrics).
- Atomic polarization** Change in dipole moment introduced by the vibrational stretching of the chemical bond between two different atoms (permanent dipole, present in all dielectrics).
- Dipolar polarization** Rotation of permanent dipoles present in polar dielectrics.
- Ionic polarization** Occurs when ions are present in the dielectric as these species drift with the applied electric field (presence of impurities or in electrolytic dielectric).
- Interfacial polarization** Introduced by the presence of interfaces in a multicomponent system. (Maxwell-Wagner effect)

The global polarisation, and thus the permittivity, is the result of the superposition of each of these phenomena (if present in the material). As each of these mechanisms display different amplitudes, response times or saturation windows, the permittivity is critically dependent on various external parameters. A qualitative evolution of permittivity with the frequency is reported in Figure 2.2, where each phenomenon display a specific cut-off frequency above which the polarization mechanism cannot follow the speed of the electric field. As a consequence, the solicitation frequency used in a measurement should always be provided when κ is discussed.

As the permittivity of a material is the macroscopic sum of all polarization types present microscopically, the maximization of each of these phenomena will generate an increased dielectric constant. For example, most of the high- κ polymers, generally display large dipole moment monomer units[53]. However, an increase in permittivity from a large dipolar density generally comes at the cost of linear behaviour. If the dipoles do not interact with one another, their rotation towards the applied field is not hindered and largely increase the amount of charge available at the electrodes (larger κ). Once all dipoles are aligned with the field only the

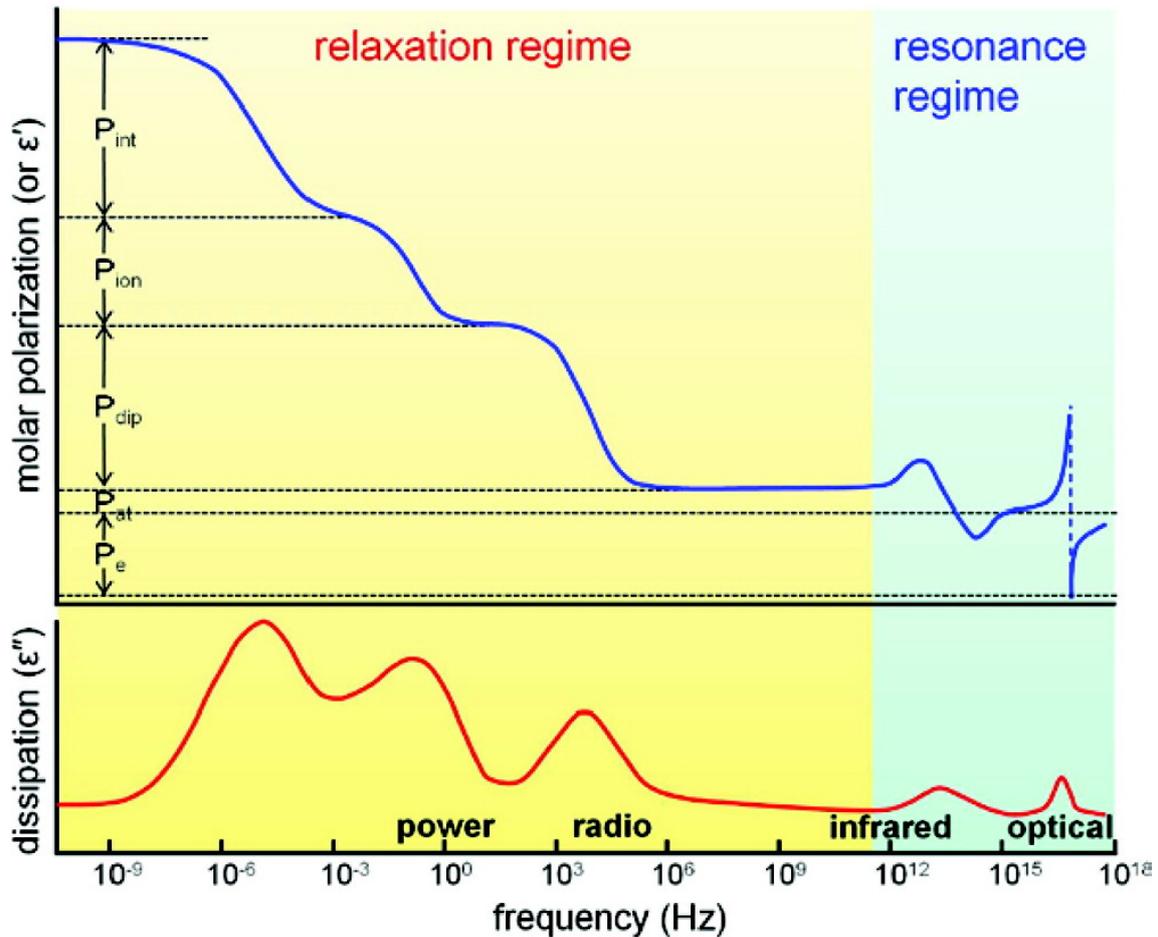


Figure 2.2: Different types of polarization as a function of frequency in polymers. P_e : electronic polarization; P_{at} : atomic polarization; P_{dip} : (dipolar) orientational polarization; P_{ion} : ionic polarization; P_{int} : interfacial polarization. The top panel shows the molar polarization (or the real part of permittivity), and the bottom panel shows the dissipation factor (the imaginary part of permittivity)(reproduced from [60]).

atomic and electronic polarization are left to contribute to the polarization, hence the saturation of permittivity. This is generally the case in paraelectric materials where each molecule presents a permanent dipole but no global polarization on average.

In some materials, often semi-crystalline, identically oriented dipoles will form small ordered domains[61, 62]. In these so called nano-domains, the local electric field is screened by the electrostatic interactions between the dipoles. As a result, the global electric field required to rotate a single dipole is increased, thus introducing a small hysteresis to the $P(E)$ plot (Figure 2.3). Once above a critical applied field named Coercive Field (E_C), a dipole has the possibility to switch its orientation with the field. As a result the interaction with neighbouring dipole is broken and the local screening

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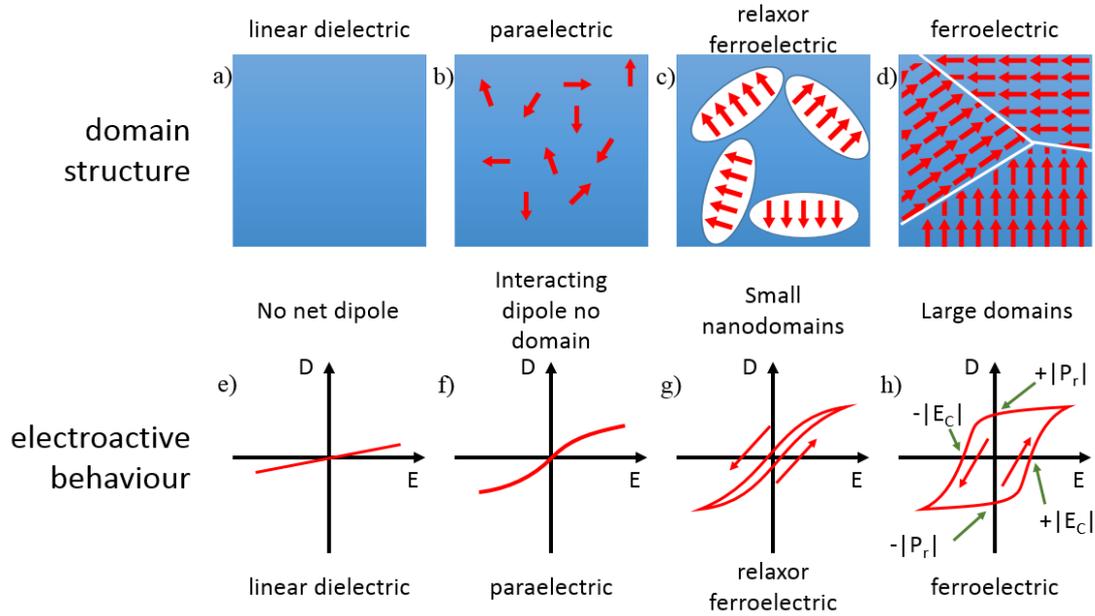


Figure 2.3: Illustration of microscopic structure [a)b)c)d)] and hysteresis loop [e)f)g)h)] for respectively a linear, paraelectric, relaxor-ferroelectric and ferroelectric dielectric (adapted from[65]).

of electric field is lowered, inducing a cascading effect quickly rotating all dipoles in the domain[63]. Since each nano-domains behaves independently and present different E_C values (ie: different number/density of dipoles) the transition observed in polarization is gradual. This behaviour is referred to as relaxor-ferroelectric (RFE) since it was historically discovered throughout the degradation of ferroelectric (FE) structures[64].

As FE materials present large ordered domains, the screening of the applied electric field by the dipolar interaction is extremely potent. This effect generates larger hysteresis and more abrupt transitions from one “polarized” state to the other. The strength of these interactions is such that the dipoles will remain oriented without any external electric field applied, this phenomenon being known as the Remnant Polarization (P_r). Because of the stability provided by the large dipolar interactions the charge generated by the remnant polarization might still be measured after months[66, 67].

Conclusion 2.1 (Polarization) *The displacement field of a material is resulting from the summed response of all the local charges in the material (polarization) and the free space charge to an applied electric field. Permittivity is the factor describing the proportionality between this displacement field and electric field in an ideal dielectric. Although this constant is only defined for an ideal insulator, its extraction via capacitance measurements for non-linear (ferroelectric, relaxor-ferroelectric) systems is often encountered and generally accepted in the literature. There are multiple origins possible for non-linearities and hysteresis in dielectrics. However, in the materials studied here the main cause of ferroelectric behaviour is the long range dipolar interaction.*

2.1.2 Fabrication of capacitors and electrical measurements

Dielectrics are generally measured in a parallel plate capacitor (with a structure similar or as a close variation to the one seen in Figure 2.1). The capacitance of such structures is one of the most useful and accessible parameter available to discuss the properties of any studied dielectric. To access this value, a sinusoidal voltage (Figure 2.4 a)) with a set level (U), frequency (ω) and also possibly a bias offset (U_{DC}), is applied across the capacitor as input signal. The complex impedance (Z) of standard RC circuits (Figure 2.4 b)) can then be fitted to the current flowing through the sample thus returning the capacitance and resistance values for these equivalent structures.

As mentioned earlier, the measured capacitance of a dielectric is susceptible to be impacted by various experimental conditions. Hence, capacitance values are often presented as a function of frequency ($C(f)$) or bias ($C(V)$) which provides a better insight on the available windows of operation and phenomena contributing to the polarisation (Figure 2.5). In this work, we used an *Agilent Precision LCR meter (E4980A)* to measure the capacitance values of our samples.

Whilst such data is generally useful, information about the dynamic behaviour is

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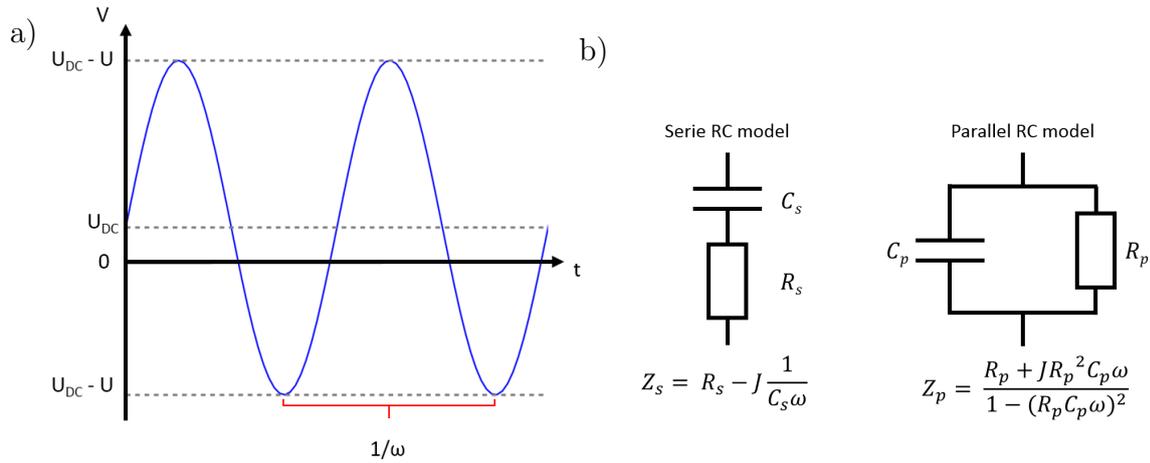


Figure 2.4: a) a simple sinusoidal voltage input; b) electrical schematic and complex impedance of the fitted RC model.

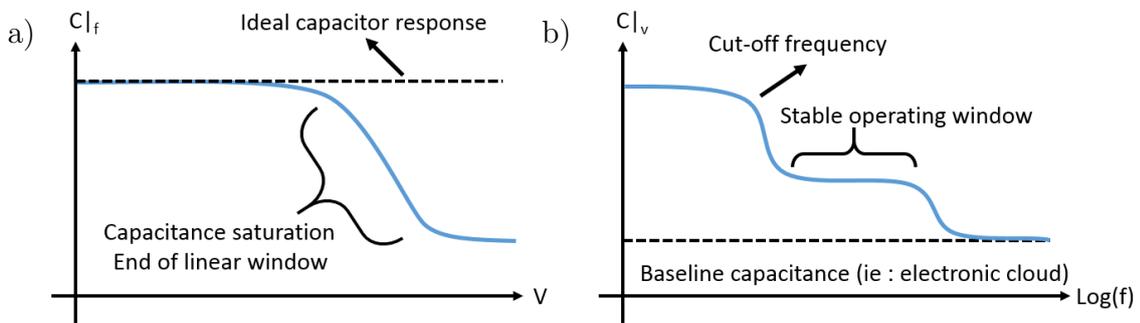


Figure 2.5: General representation of a) capacitance versus applied voltage and b) capacitance versus frequency.

often required for the full understanding of the dielectric properties. Considering that the capacitance measurement only provides information about a determined operating point (oscillation around a specific bias), it might still be considered as a static acquisition. In order to understand the dielectric’s behaviour in a dynamic environment, one may rely on “polarization cycle” measurements. However, and despite its name, this acquisition does not directly probes the polarization but rather the resulting net surface charge accumulated on the electrode ($C.m^{-2}$) at a given time. When plotted versus the applied electric field it allows for the observation of any non-linearity or hysteresis present in the sample similar to the one seen in Figure 2.3 e)f)g)h).

There are commonly two typical experimental set-ups that can provide this type of information : the Sawyer-Tower circuit and an integrating circuit. In both cases,

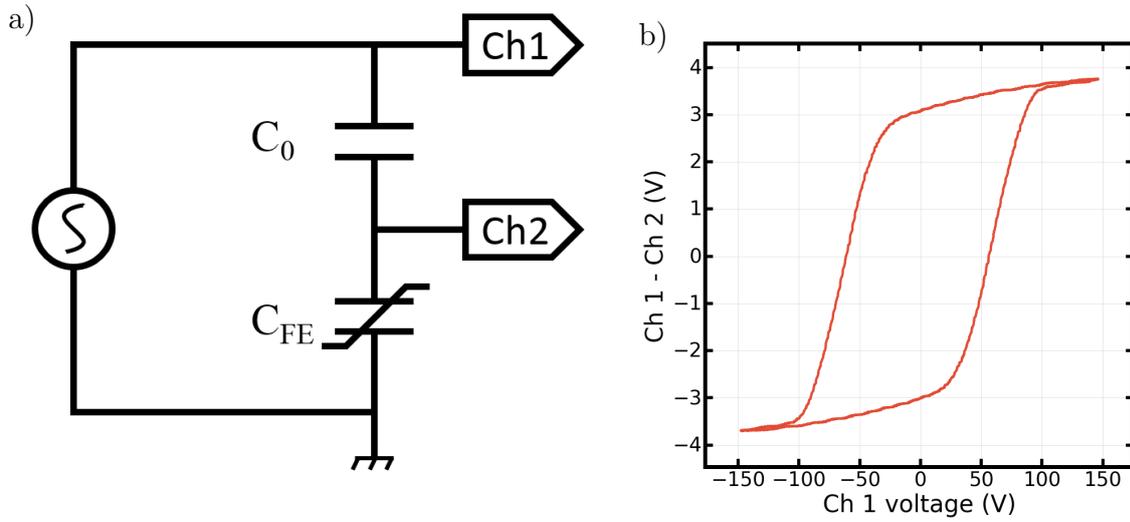


Figure 2.6: a) Electrical schematic of a simple Sawyer-Tower setup with C_0 the measured sample and b) an example of xy oscilloscope reading for a ferroelectric material (P(VDF-TrFE) capacitor).

a signal is applied to the dielectric sample but their acquisition method rely on two different physical principles.

The Sawyer-Tower set-up describes a family of electronic circuits used to measure hysteresis in ferroelectrics, it acquired its name from the two scientists that first proposed its use in 1930[68]. The most simple form of its kind only requires an alternating generator, a linear capacitor with a know capacitance higher than the studied sample ($C_0 \gg C_{FE}$) and an oscilloscope to probe different the voltages (Figure 2.6 a)). A simple XY plot rendered directly on the oscilloscope allow for a quick reading of the hysteretic behaviour in a material (Figure 2.6 b)), but in order to actually extract the net surface charge for the ferroelectric sample (Q_{FE}) a simple mathematical transformation is needed. As the reference capacitor is linear and with a known capacitance, the charge at its terminal follows Equation (1.16). When adapted to the set-up and by taking into account the surface of the sample's electrodes (S_{FE}) the equation of capacitance becomes Equation (2.5).

$$Q_{FE} = \frac{C_0 (V_{ch1} - V_{ch2})}{S_{FE}} \quad (2.5)$$

One of the main drawback of this set-up is the that the sample is continuously cycled during the acquisition which may introduce a fatigue phenomenon in the

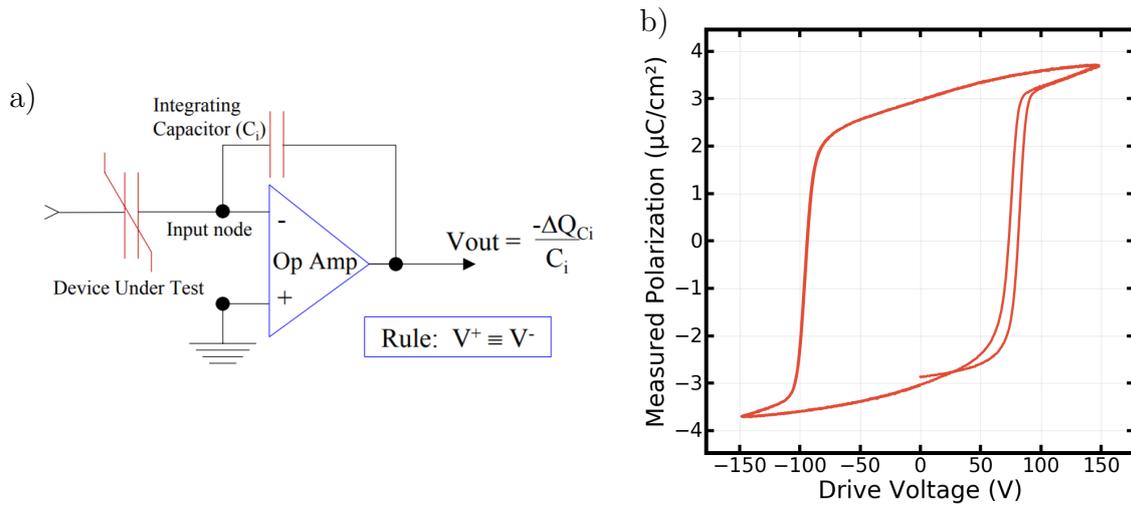


Figure 2.7: a) Electrical schematic of an integrator circuit (reproduced from radiant technologies. inc documentation) b) an example of polarization measurement acquired with integrator based set-up where the initial polarization behaviour can be seen (P(VDF-TrFE capacitor).

material[69, 70] alongside with an impossibility to evaluate the initial response of the material to the electrical stimulus.

Integrator circuits operate by directly integrating the current passing through the sample when a voltage is applied. This is generally the more modern approach, it allows for a direct reading from any signal and as a result requires less solicitation of the sample. Current integration is performed electrically with the help of an operational amplifier, an example for such circuit can be found in Figure 2.7 a). Contrary to the Sawyer-Tower, acquisition by integrator circuits begins at the same moment that the driving voltage is applied. As a result transitive behaviour from “rest” to “solicited” can be observed (Figure 2.7 b)) and the actual persistence of the remnant polarization can be evaluated. All the P(E) acquisition from this work have been conducted on a *Radiant Technologies. inc Precision Multiferroic*.

Regardless of the set-up a “Polarization” measurement does not exactly returns the polarisation of the measured sample. Both of the methods described previously aim to quantify the amount of charges accumulated at sample’s electrodes when a voltage is applied. This accumulation is the result of the integration of the current

flowing through said electrodes at a given time (Equation (2.6)).

$$Q(t) = \int_0^t I(t) dt. \quad (2.6)$$

With the electrical current defined by the current density (\vec{J}) flowing through an enclosed surface (S) :

$$I = \iint_S \vec{J} \cdot d\vec{S} \quad (2.7)$$

In the case of an ideal dielectric, the only current density present is introduced by the dielectric displacement (\vec{J}_D). However, no insulator is perfect and conduction can still be occur to certain an extent. This yields a current density \vec{J}_C where σ is material's conductivity.

$$\vec{J}_D = \varepsilon_0 \frac{\partial \vec{E}}{\partial t} + \frac{\partial \vec{P}}{\partial t} \quad (2.8)$$

$$\vec{J}_C = \sigma \frac{\partial \vec{E}}{\partial t} \quad (2.9)$$

As a result, the global current flowing at the dielectrics terminals is described with Equation (2.12)

$$I = \iint_S (\vec{J}_C + \vec{J}_D) \cdot d\vec{S} \quad (2.10)$$

$$= \iint_S \left(\sigma \frac{\partial \vec{E}}{\partial t} + \varepsilon_0 \frac{\partial \vec{E}}{\partial t} + \frac{\partial \vec{P}}{\partial t} \right) \cdot d\vec{S} \quad (2.11)$$

$$= \frac{\partial}{\partial t} \iint_S \left((\sigma + \varepsilon_0) \vec{E} + \vec{P} \right) \cdot d\vec{S} \quad (2.12)$$

From this we can easily understand how a large amount of leakage (ie: high conductivity) would hinder the probing of any polarization behaviour. Furthermore, if the material's dielectric constant is not high enough the free space charge impact on the measurement could be significant. Unfortunately, leakage is generally poorly commented and there are some papers in the literature wrongly reporting ferroelectric material based on misinterpreted polarization measurements. In 2008 J.F. Scott highlighted this problematic with a satirical article describing a ferroelectric behaviour found in banana fruits[71]. In this report, he compared the $P(E)$ cycles of a banana peel to a known ferroelectric material ($\text{Ba}_2\text{NaNb}_5\text{O}_{15}$). In both case hysteresis could be observed however one was caused by electrical conduction through the fruit's skin and the other by an actual ferroelectric behaviour. Here, we propose

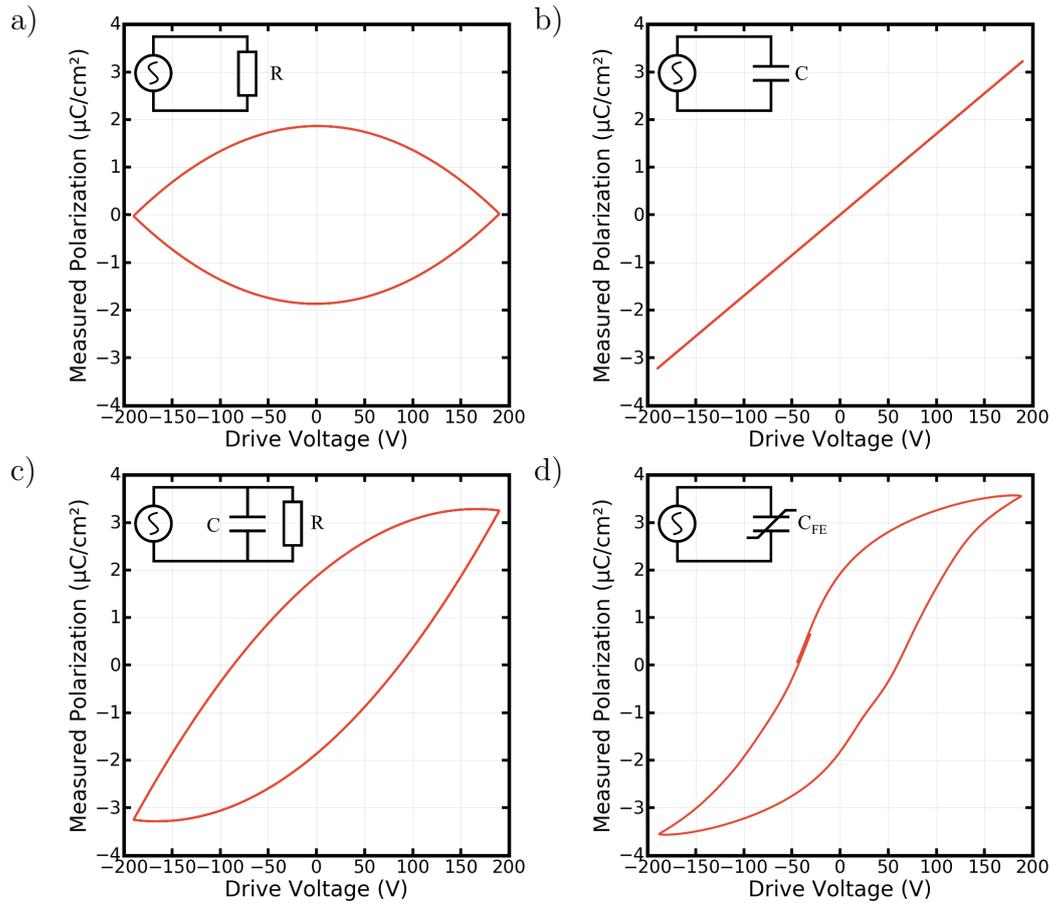


Figure 2.8: Example of a polarization response of a) a theoretical resistor, b) a theoretical capacitor, c) a theoretical parallel RC circuit and d) a real ferroelectric material to a triangular input signal.

to illustrate the relative likeness in hysteresis cycle between a lossy capacitor (parallel RC circuit) and a material that actually presents some ferroelectric behaviour (a P(VDF-TrFE) capacitor) in Figure 2.8. The sum of the integrated current from a resistor and a capacitor in parallel yields a large hysteresis cycle with pointed extremities (with a triangular input signal; Figure 2.8 c)) that may be mistaken for the saturation in the ferroelectric. To avoid misinterpretation, one should look for an actual saturation of the polarization along with the presence of a concave shape at the extremities of the polarisation. Furthermore, these two behaviours exhibit different frequency, signal and temperature dependency which may allow for a better distinction.

Conclusion 2.2 (Measurements) *Polarisation measurements generally rely on the measure of the current flowing through electrode of a sample. Because of the intrinsic flaws of this process one should always be careful for the parasitic phenomena that may distort the acquired data. By reproducing the measurements over a large array of samples and by varying the measurement parameters we are confident that most parasitic behaviours were identified prior to the drawing of conclusion in our study.*

2.1.3 Polyvinylidene fluoride and derivative materials

Because of its highly non-chemically reactive profile polyvinylidene fluoride is widely used in a large variety of industrial fields mainly as a coating or directly as piping material. However, since the discovery of its piezoelectric properties in 1969[72] it was also extensively studied in electronics. The origin of the large permittivity exhibited by this family of material can partially be attributed to the large dipolar moment of the VDF unit (for example: $|\vec{p}_{P_{VDF}}| = 2.1 D$ [73] versus the dipolar moment of a classic dielectric $|\vec{p}_{P_{MMA}}| = 1.46 D$ [74]). Like most materials, its microscopical structure is the main drive of its macroscopic properties.

Polyvinylidene fluoride is a semi-crystalline material[75, 76]. Meaning that it generally forms structure with ordered crystallites dispersed in an amorphous matrix. It is the configuration and quantity of said crystallites that are at the core of the peculiar ferroelectric properties exhibited by this polymer family. Based on x-ray diffraction data reported in the literature, Tashiro et al proposed three chain conformations encountered in the ordered part of the polymer[77]:



Figure 2.9: Chemical formula of the PVDF and a 3D representation of the VDF unit (grey: carbon, green: fluorine and white: hydrogen).

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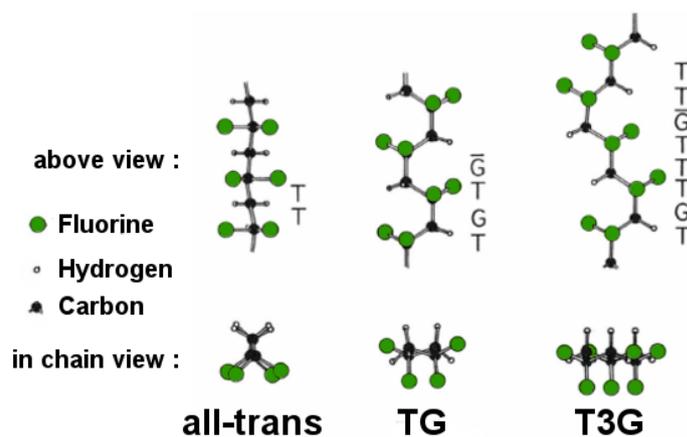


Figure 2.10: The three general chain conformations for ordered PVDF homopolymers (adapted from [77]).

In this diagram the letter T (trans) and G (gauche) refer to the arrangement of monomer unit. A trans arrangement indicates that the two consecutive monomers are in the same orientation where as the gauche arrangement indicates a rotation in the consecutive monomer units orientation. The three global conformations obtainable in VDF crystals are the all-trans, the trans-gauche and the trans³-gauche. Of the three, it is the all-trans that displays the highest global dipolar moment as all molecular moment in the chain are oriented in the same direction.

From these three different chain configurations, four crystalline structures can emerge. They are generally referred to as : α , β , γ and δ . Theses structure have been described in terms of crystalline parameters (a, b, c) and rotation symmetry in K. Tashiro[78, 79] and A.J Lovinger[80, 81] respective works.

β phase (all-trans) Composed by all-trans chains oriented in the same direction, this crystalline lattice presents the highest dipolar moment. The principal source of the ferroelectric behaviour observed in PVDF is generally attributed to this polar phase[82].

γ phase (T³G) Sometimes mistaken for the β phase[83], this is another polar crystallite of the PVDF. Because of its T³G chain conformation,

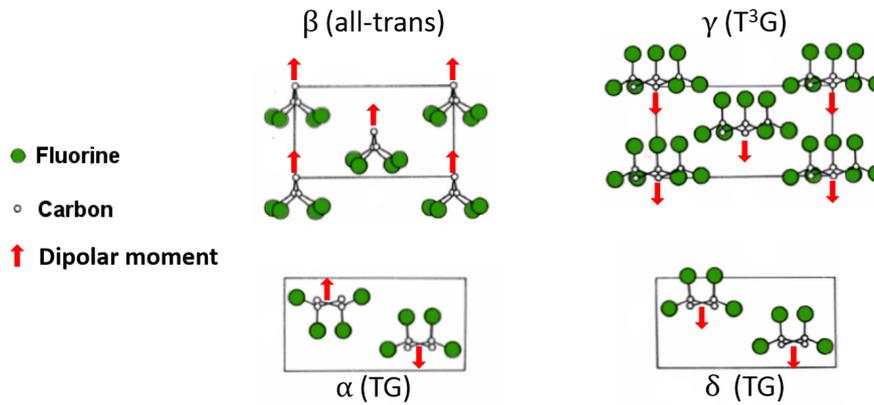


Figure 2.11: The four main crystalline lattices achievable in pristine PVDF[77].

the global polar moment of this structure is lower than the one found in the β structure.

- α phase (TG) The paraelectric phase of the PVDF. The global moment of this crystalline structure is null as the polar moment of the TG chains compensates one another.
- δ phase (TG) Achieved by the electrical polling of the α phase[84]. The alignment of a polymer chain with the electric field grants a global polar moment to the crystalline lattice. However, the stability of this phase is precarious and will generally return to the α phase when no longer electrically stimulated.

It was shown in the literature that the α phase is the most commonly occurring phase in pristine PVDF films but with the help of various processing methods (solvent, mechanical treatment, annealing, electrical polling) any of the other phases could be obtained[77, 85, 86]. The ferroelectric (and thus piezo/pyroelectric) properties of the β phase were generally sought for various applications but the processing methods needed to achieve these properties would not always be compatible with fabrication of devices (mechanical stretching, high pressure quenching[77, 86]). To circumvent this issue, a chemical solution has been proposed through the addition of a co-monomer in the polymer chain.

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Figure 2.12: Chemical formula of the P(VDF-TrFE) copolymer and a 3D representation of the TrFE unit (grey: carbon, green: fluorine and white: hydrogen).

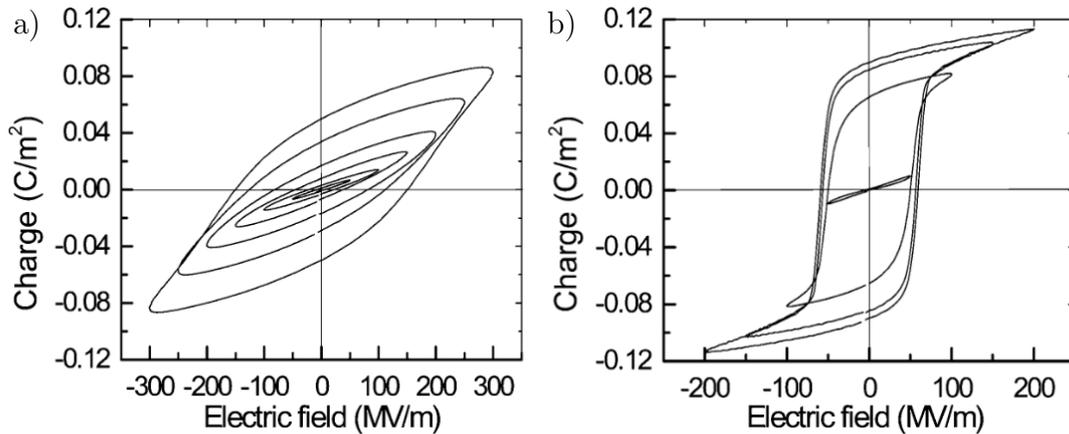


Figure 2.13: Comparison between the evolution of polarization cycle with maximal bias of a) the pristine PVDF and b) a P(VDF-TrFE) copolymer (adapted from [89]).

Introduction of trifluoroethylene (TrFE) units (Figure 2.12) within the PVDF polymer chain is equivalent to a head-to-head tacticity chain defect which increases the lateral parameter of the crystalline lattice and results in a weakened chain constrain which was reported to stabilize the β phase and promote its germination[87, 88]. Physically this translates to a decrease of the Curie transition temperature (T_C) below the melting temperature[88] and an improved long distance interaction the dipoles. Because of this stabilization and increased crystallinity, the P(VDF- TrFE) exhibits cleaner ferroelectric polarization loop when compared to the PVDF as can be seen in Figure 2.13[89].

With the demonstration of an improved β phase stability the interest in the dielectric properties of the P(VDF-TrFE) copolymer grew[90]. This general interest lead to the production of various studies concerning the physical properties of the P(VDF-TrFE)[91] and the impact of monomers ratio onto said properties[88, 92, 93]. Since the relationship between crystallinity and physical properties of PVDF-based copolymer was well established, studies on the impact of structural defects in the

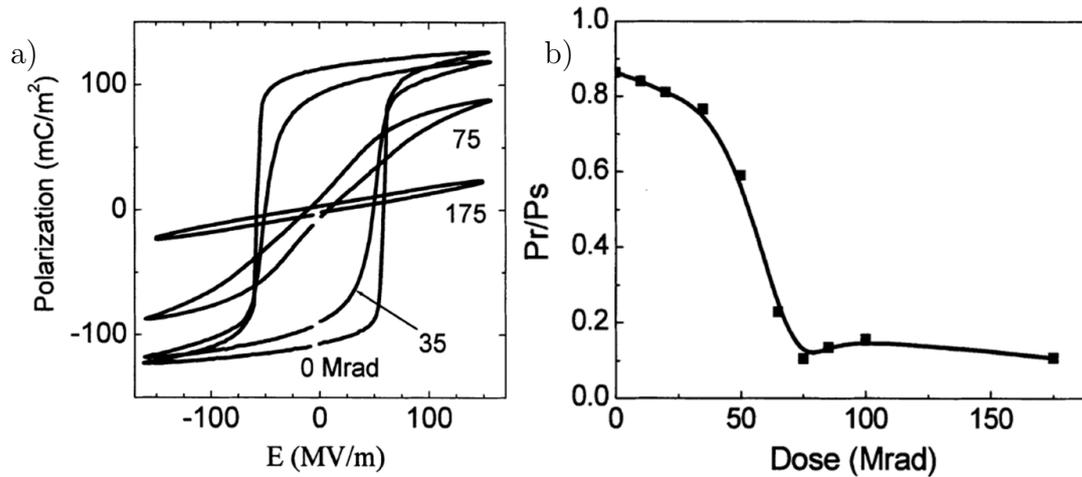


Figure 2.14: a) Polarization hysteresis loop from irradiated P(VDF-TrFE) (0 to 175 Mrad) and b) Ratio of remnant polarization over saturation polarization (at 150V/m) versus irradiation (reproduced from [94]).

copolymer crystals had been proposed. In order to achieve a higher defect content, the scientific community investigated various physical and chemical methods that would prove to drastically impact the polarization and other physical properties (electrostriction, pyroelectricity ect).

Reports in the literature described that an electron irradiation of the P(VDF-TrFE) copolymer, depending on power and length of exposure, fragmented the large crystalline domains. This resulted in smaller crystallite size and thus in a global change of polarization profile[94, 95]. To explain this phenomenon, Hiczler et al proposed that the irradiation created radical species on the chain, which would initiate chemical reactions leading to the formation of peroxides in the chain when exposed to air[96]. These newly introduced chemical species would thus act as structural impurities in the crystalline lattice destroying long distance organization in the material. In Figure 2.14 we may observe a gradual decrease of remnant polarization, saturation polarization (maximum measured polarization; P_S) and coercive field with each increasing dose of radiation. One may also notice a transition from a ferroelectric loop (0 and 35 Mrad) to a relaxor-ferroelectric after a 75 Mrad irradiation (Figure 2.14). And finally after a 175 Mrad dose, the copolymer lost any ferroelectric-like behaviour and resemble something similar to a lossy dielectric.

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Figure 2.15: 3D representation of a) the CFE and b) CTFE units (grey: carbon, green: fluorine, blue: chlorine and white: hydrogen).

The irradiation also introduced a noticeable increase in permittivity of the copolymer. As the long range interaction between the molecular dipolar moment was broken down, their ability to quickly respond to the applied electric field increased and thus allowed for a higher permittivity. As prior, this new properties revealed to be extremely interesting for some applications but the use of high power radiation in the fabrication process would present a challenge. Again, a chemical solution similar to the one seen for the copolymer was proposed: introducing third “bulkier” monomer in the polymer chain[97].

The two most commonly encountered ter-monomers in the literature are the 1-chloro-1-fluoroethylene (CFE) and the chlorotrifluoroethylene (CTFE)(Figures 2.15 and 2.16). These two molecules include a large chlorine atom in their composition (Van der Waals radius for chlorine is 175 *pm* versus 135 *pm* for fluorine) which was demonstrated to produce an effect on polarization similar to the crystallites irradiation[87]. The microscopic origin of the relaxor-ferroelectric behaviour in these novel terpolymers has been extensively discussed and the general consensus to this date propose that the large ter-monomer randomly positioned in the chain may acts as a physical pinning point similar to the chemical pinning introduced by irradiation[65] (Figure 2.16). Recently this theory was further elaborated to account for the presence of Dual Hysteresis Loop (DHL) and Single Hysteresis Loop (SHL) observed the terpolymers[98, 99], SHL describing an hysteresis with a consistent width in the polarization (ferroelectric-like) whereas DHL refers to an hysteresis with a thinner width at the center (anti ferroelectric-like)(Figure 2.17).

A proposed origin for these two behaviours finds its sources in the difference of pinning strength for each monomer. Yang et al theorized that the CFE being

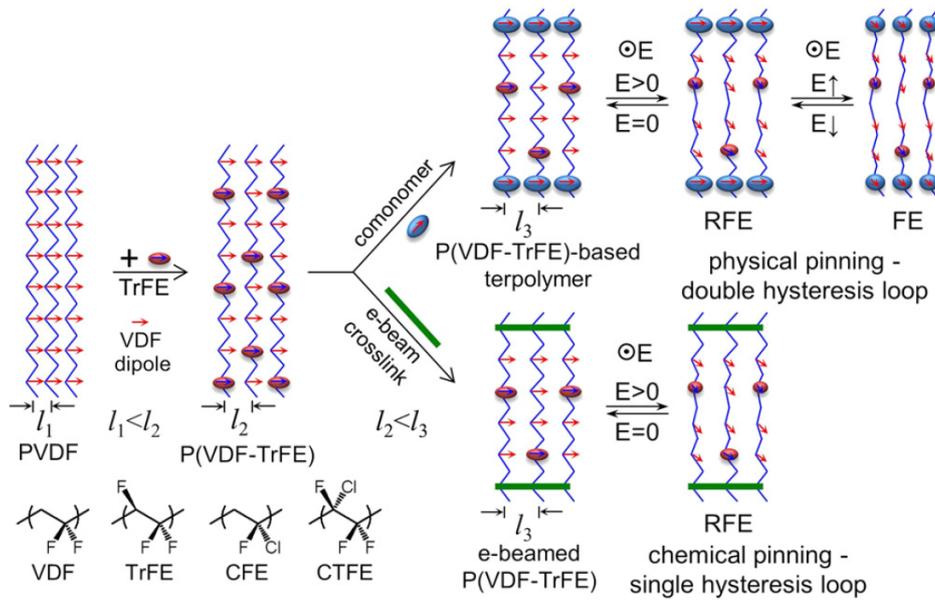


Figure 2.16: Schematic representations of physical (temporary) and chemical (permanent) pinning in laterally expanded P(VDF-TrFE) crystals, namely, P(VDF-TrFE)-based terpolymers and e-beam cross-linked P(VDF-TrFE) copolymers. l_1 , l_2 , and l_3 are average inter-chain distances in PVDF, P(VDF-TrFE), and P(VDF-TrFE)-based terpolymers or e-beamed P(VDF-TrFE), respectively. The orange-red and blue ovals with arrows in them represent dipolar TrFE and the third co-monomer with larger sizes. The green bars represent the chemical cross-links inside the crystal (reproduced from [65]).

smaller with a larger dipole moment ($|\vec{p}_{CFE}| = 1.8 D$) is less spatially constrained and could switch orientation thus losing its pinning ability at high field causing dual loop hysteresis. Whereas the CTFE being a larger monomer with a smaller moment ($|\vec{p}_{CTFE}| = 0.64 D$) would keep its orientation and pinning property thus only allowing for a single loop [100] (Figures 2.17 a) and 2.17 b)). However, because Yang's study was conducted on stretched films and examples of both DHL/SHL polarization can be found in the literature (and this present work) for either P(VDF-TrFE-CTFE) or P(VDF-TrFE-CFE) (Figures 2.17 c) and 2.17 d)) questions are still unanswered concerning these behaviours.

Globally speaking, the P(VDF-TrFE-CFE) presents a thinner hysteresis and a larger dielectric constant (generally reported above 50) [48, 100, 101] which makes it the terpolymer of choice for low-voltage organic transistors [49, 102]. However, because of the lack of access to this material for the most of the duration of this

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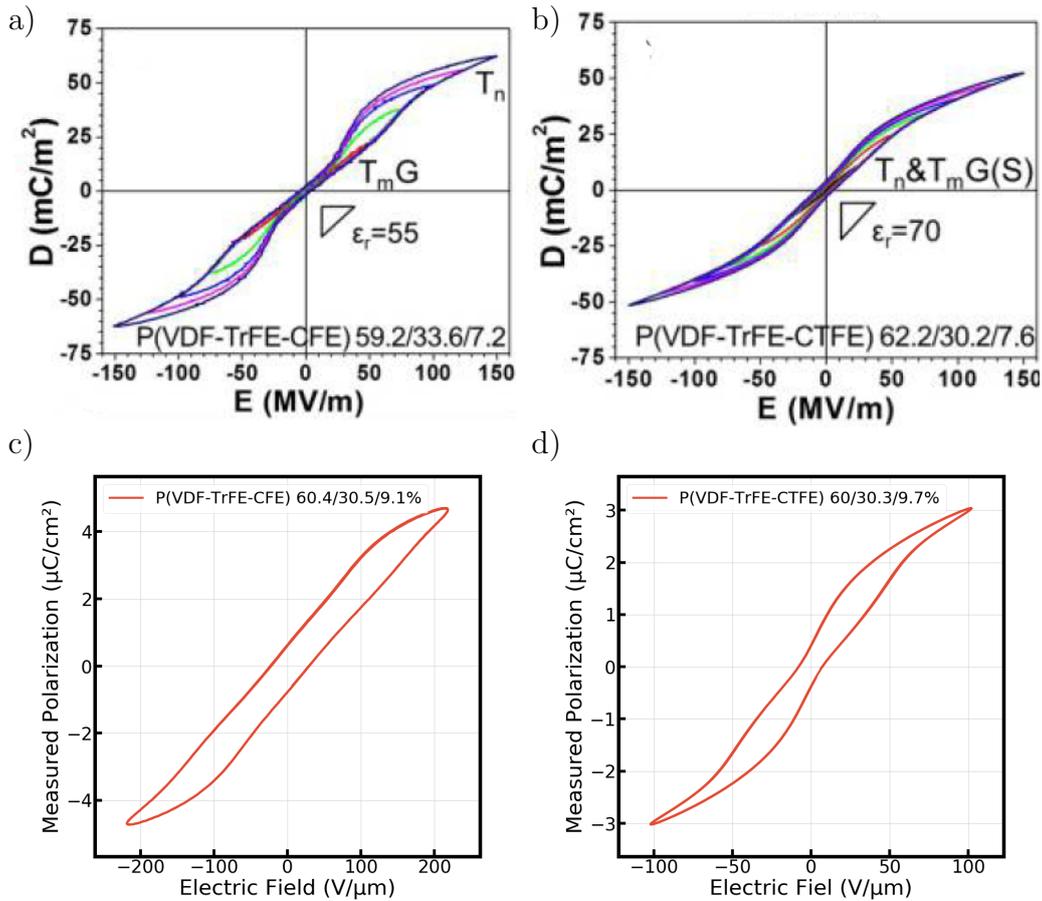


Figure 2.17: Polarisation cycle reproduced from [100] for a) P(VDF-TrFE-CFE) (59.2/33.6/7.2) and b) P(VDF-TrFE-CTFE) (62.2/30.2/7.6); Polarisation cycle conducted on capacitors fabricated in this thesis: a) P(VDF-TrFE-CFE) (60.4/30.5/9.1) and b) P(VDF-TrFE-CTFE) (60/30.3/9.7).

thesis, the large part of this work will discuss the properties of P(VDF-TrFE-CTFE) polymers. Nevertheless, the CTFE might be better suited for the study of the relaxor-ferroelectric behaviour as its polarization hysteresis is more pronounced. As such, the variation in this hysteresis might be easier to monitor. We are confident that some of the observation gathered in this work could be equivalent to the CFE polymer, however we advice the reader to be cautious with overly general conclusion as the behaviour of these materials is heavily composition dependent.

Conclusion 2.3 (PVDF-based materials) *The large range of dielectric properties displayed by the polymers from the PVDF family are rarely encountered in other organic materials. As such they are extremely attractive for a large array of applications. However, the RFE behaviour present in the terpolymer may also introduce undesired phenomena in the transistor's characteristic. A deeper characterization of its dielectric properties is thus required in order to understand its possible impact on OTFTs.*

2.2. P(VDF-TRFE-CTFE) AS A DIELECTRIC MATERIAL

2.2.1 Sample fabrication

The samples discussed in this chapter were fabricated on 125 μm thick flexible PEN (Polyethylene naphthalate) sheets with pre-patterned gold electrodes (30 nm). The deposition of high- κ was carried out via spincoating from a solution consisting of a polymer powder (purchased from Piezotech-Arkema) dissolved in cyclopentanone for at least 24 h . The low- κ layers have been obtained by spincoating from a commercial solution in decane. Where spinning speed (rpm) and solution viscosity were the main parameter influencing the final film thickness. After a 5 min annealing at 115 $^{\circ}\text{C}$ of the polymer film a 150 nm gold top electrode was deposited via thermal evaporation through a shadow mask. In the case of bilayer dielectric capacitors (discussed later in this chapter), the deposition and annealing of the low- κ is followed by a partial stripping of this layer on a portion of the electrodes with the help of toluene. Which was then followed by the deposition/annealing of a high- κ relaxor ferroelectric layer. The partial cleaning of half of the capacitors provided the access to bilayer capacitors and simple RFE capacitors with identical terpolymer thickness on the same substrate.

2.2.2 Impact of chemical composition on electrical properties

Regarding the context of a transistor's gate insulator, an optimum dielectric should be linear, loss-less and exhibiting the highest possible permittivity. The combination of all this properties could enable low operation voltage in transistor while preserving and ideal behaviour. Consequently, the main objective of this section is to evaluate and understand the general properties of the P(VDF-TrFE-CTFE) terpolymer to propose an adequate dielectric structure for the transistor.

As discussed previously, the dielectric properties of the P(VDF-TrFE-CTFE) are directly impacted by its chemical composition. Since terpolymers are made of three different monomer units that are randomly distributed along the chain, their composition ratio is the common way to distinguish them in the literature. It is usually done like so : P(VDF-TrFE-CTFE)(X/Y/Z). In this notation X,Y and Z respectively refer to the percentage of VDF, TrFE CTFE (or CFE in the case of P(VDF-TrFE-CFE); Figure 2.19).

To obtain the best possible performances in the final transistor, the optimum terpolymer would present the highest possible permittivity and the narrowest hysteresis possible. A simple process to determine the most suitable material was to study

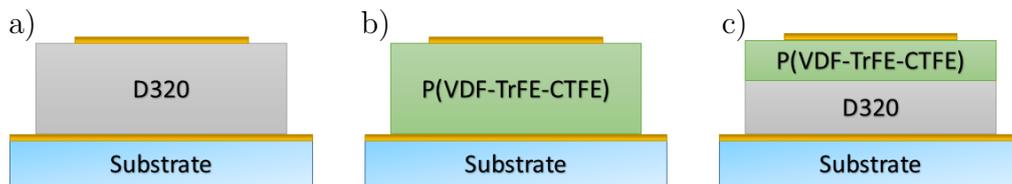


Figure 2.18: Schematic of the parallel plate capacitor studied a) low- κ , b) high- κ and c) bilayer.

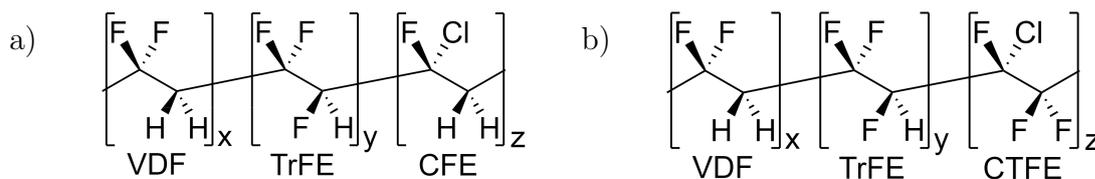


Figure 2.19: General chemical formula of the a) P(VDF-TrFE-CFE) and b) the P(VDF-TrFE-CTFE)

2. $P(\text{VDF-TRFE-CTFE})$ AS A DIELECTRIC MATERIAL

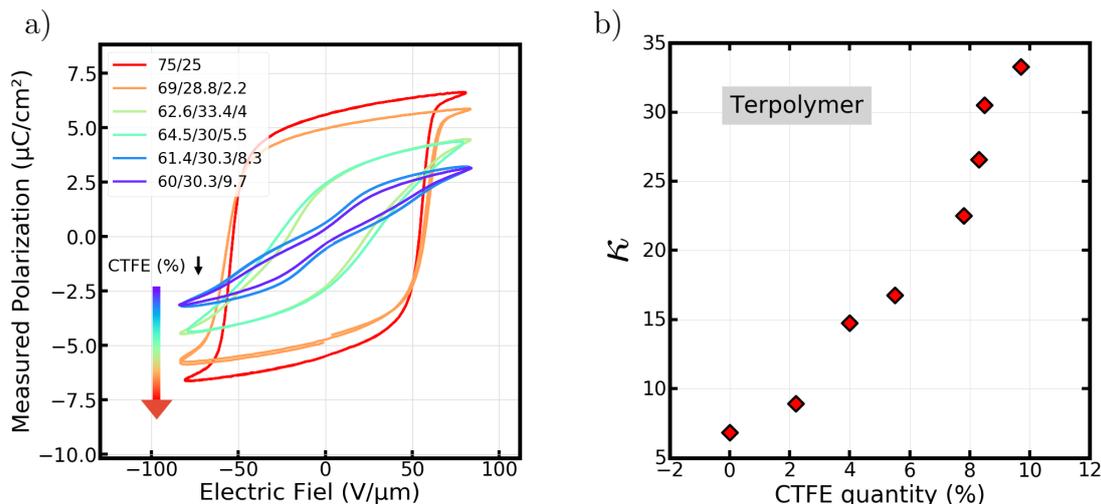


Figure 2.20: Evolution of a) polarization behaviour (input: 100 Hz sinusoid) and b) the dielectric constant with the composition of P(VDF-TrFE-CTFE) (bias: 0 V, level: 0.1 V, frequency: 100 Hz)

a selection of terpolymer with an increasing CTFE content (%).

Figure 2.20 a) describes the evolution of the terpolymer polarization cycle when the CTFE content is increased. In red is represented an example of P(VDF-TrFE) copolymer ferroelectric hysteretic cycle to act as a base line for polarization comparison. We can notice three different behaviours depending on the global composition. When the amount of CTFE in the chain is small ($\approx 2\%$) the terpolymer polarization profile is closely matching the ferroelectric copolymer. When the quantity of CTFE is further increased ($\approx 4 - 5\%$) the polarization cycle appears to be slanted, we can also notice that the coercive field is drastically reduced to a loop that can be described as ferroelectric-like. With the help of deflection measurement (on the same set of samples studied here) Lheritier et al argued that the terpolymer retained some electromechanical properties related to ferroelectricity up until 8% CTFE content [103].

Finally, when at high CTFE content (above 8%) a typical relaxor-ferroelectric DHL behaviour appears in the polarization cycle, at this stage the coercive field is extremely reduced compared to the original copolymer. Moreover, we would like to emphasize that since the polymer's performance are also impacted by the VDF/TrFE ratio, the result discussed here should be taken as guideline for RFE behaviour rather

than absolute conclusion on the impact of CTFE.

One of the consequences of increasing the CTFE in the chain is that the remaining ordered states in the material are now even more fractionated and thus the long distance interactions are further broken down. As a result, the local polar moment of the monomer units can respond more freely to any applied electric field. The evolution of permittivity with CTFE in Figure 2.20 b) illustrates the improved response capability of the material. These results are coherent with some reports from the literature describing improved permittivity for P(VDF-TrFE-CTFE) with high CTFE content[97, 104].

From this data we can infer that a terpolymer with a large amount of CTFE would exhibit the best performances in the context of a transistor's gate dielectric. In light of this conclusion, we selected the 60/30.3/9.7 composition as the main material studied during this thesis. It should be noted that terpolymer compositions with higher CTFE content have been reported in the literature (14%)[105, 104] but are achieved through specific synthesis process and where not available from our supplier. As their general fabrication and structure might be different from the materials discussed here we will limit our conclusion on the subject. To further evaluate our selected composition's compatibility with the transistor structure we will continue this section with a frequency and temperature study.

2.2.3 Frequency

As mentioned in the earliest part of this chapter, the physical phenomena responsible for the polarisation in a dielectric have different frequency and bias responses. The impact of such parameters on both the low- κ and selected terpolymer can be found in Figure 2.21:

We can notice a general stability from the low- κ dielectric (excepted some noise at low frequency). Neither frequency nor bias appears to have a significant impact the capacitance within the observed range. With this observation we can confidently

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assume that our low- κ dielectric is linear (in our operation window) and exhibits a dielectric constant of 2.2 which is coherent with the documentation provided by the supplier.

However, the same cannot be said for the high- κ dielectric (Figure 2.21 b)), which presents a high frequency and bias dependency as can be expected from such material. From this measurement, we can notice a saturation of capacitance with bias along with an asymmetry of the profile regarding positive and negative bias. This difference may be explained by a different interface energy between the top and bottom electrode. Despite the fact that they are made from the same metal, their respective work function may be influenced by the deposition technique.

The frequency dependency observed in Figure 2.21 b) can be problematic in the transistor since an accurate capacitance value for the insulator is required to extract the semiconductor's mobility. In order to meet these requirements, we performed a quasi-static capacitance measurement (QSCV). This methodology allowed for the extraction of the capacitance in similar conditions to the transistor's operation setup, yielding a dielectric constant of 35.3.

The drop in capacitance caused by an increased measurement frequency can also

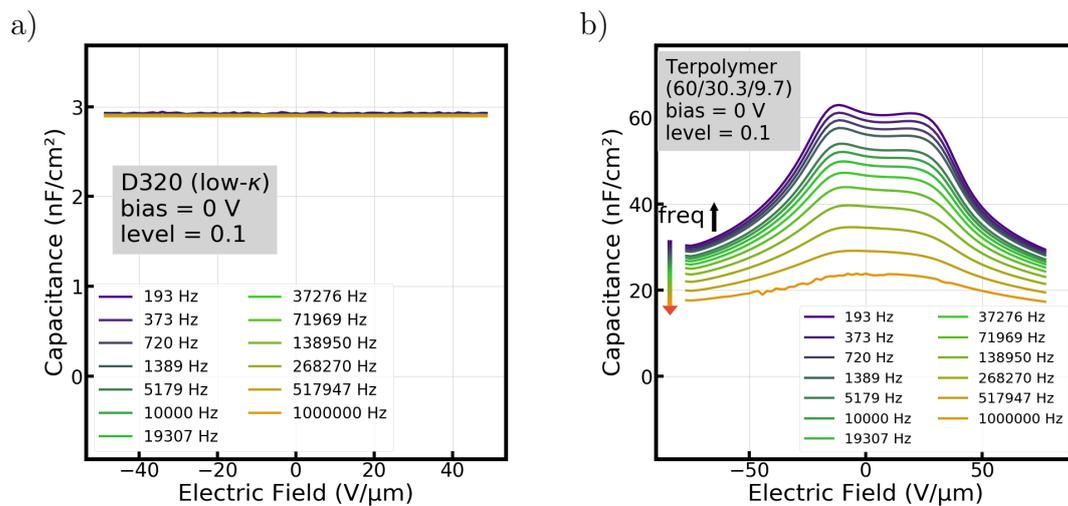


Figure 2.21: Capacitance measurement versus bias at different sollicitation frequencies for a) the D320 (reference low- κ) (film thickness: ≈ 640 nm) and b) the $P(\text{VDF-TrFE-CTFE})$ (60/30.3/9.7) (level = 0.1 V; film thickness: ≈ 520 nm).

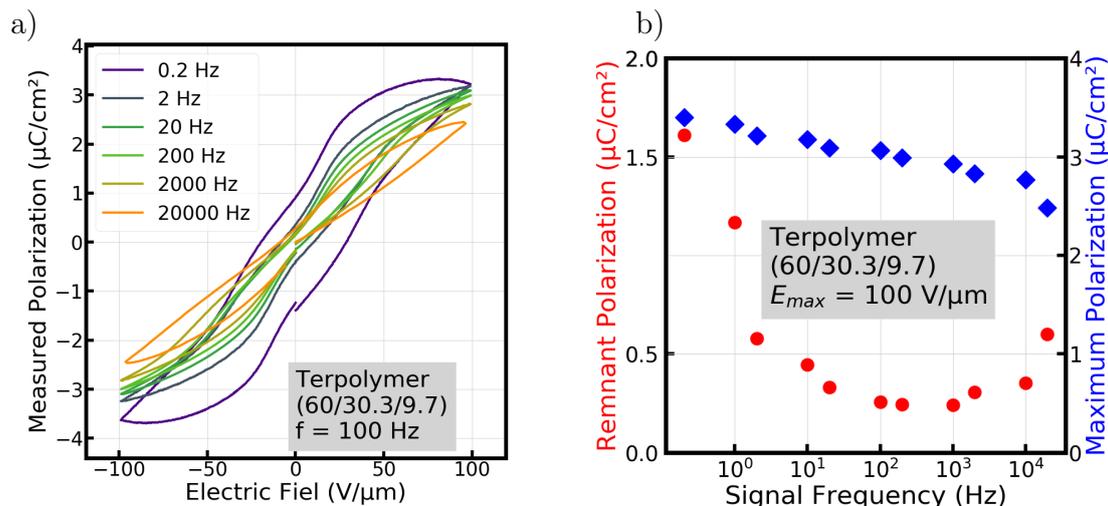


Figure 2.22: a) Evolution of polarization cycle (input signal: triangular) with frequency of P(VDF-TrFE-CTFE) (60/30.3/9.7) and b) extraction related of maximal polarisation (here $P_{max} = P(100 V.\mu m^{-1})$) and remnant polarization ($P_r = |P(0 V.\mu m^{-1})|$).

be noticed in polarisation cycles (Figure 2.22 a)) as the average slope of the hysteretic cycle and the maximal polarisation (P_{max} ; Figure 2.22 b)) follows a decreasing trend with frequency. Monitoring the $P_r(f)$ yields information about the evolution of hysteresis, as can be expected the cycle appears to be swollen with slow measurement speed. Because of the longer integration time the amount of charges generated by leakage is considerable compared to the actual polarisation of the material. As a result the hysteresis; and thus the measured remnant polarization; is artificially enlarged. However, this artefact of measurement should disappear with higher integration speed. In the case of the transistor structure, leakage, in moderate proportion, should not impact the output current, meaning that this phenomenon have little to no impact on the final device.

An increase in P_r is also noticeable at high frequency (above 1 kHz). Contrary to the previous discussed phenomenon, leakage current could not be the origin of this hysteresis enlargement. A similar behaviour was reported in ferroelectric copolymers when measured at high speed, the origin of this phenomenon was attributed to the a latency in the ferroelectric domains switching time[106]. As the electric field speed is increased, the inertia of dipole alignment in the material begin to have a significant impact. As a result the applied field is higher than the real E_C when the

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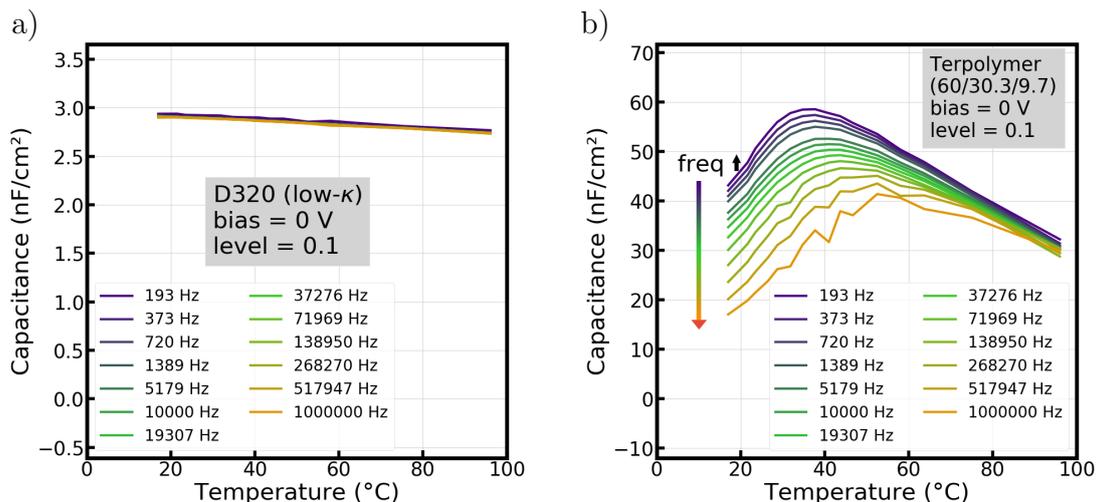


Figure 2.23: Evolution of capacitance (bias = 0 V, level = 0.1 V) versus temperature at different frequency for a) the D320 (reference low- κ) (film thickness: ≈ 640 nm) and b) the $P(\text{VDF-TrFE-CTFE})$ (60/30.3/9.7) (film thickness: ≈ 520 nm)

dipole rotation finally occurs thus artificially enlarging the hysteresis. This denotes a significant impact of high frequency on the polarisation hysteresis, impact that could also have repercussion on the transistor's behaviour.

2.2.4 Temperature

Temperature is a critical factor when studying dielectrics. As most of the polarization phenomena are based on interaction with the local electric field, the surplus of energy brought by an increase in temperature might change their responses to an external electric field. Because of their various origins, polarization mechanisms at play in a material may respond differently to the increased thermal energy induced by higher temperature: $k_b T$. In the case of a classic low- κ dielectric an increase in temperature induces a degradation of the capacitance (Figure 2.23 a)) as the increased thermal motion in the molecules lowers the orientation response to the applied field.

In the case of ferroelectric materials, there is a well know phenomenon occurring at a critical temperature: the Curie temperature (T_C). When the T_C is reached the interaction between molecular dipoles is screened by thermal energy, which induces a transition to a paraelectric behaviour. In ferroelectrics, this transition is identified

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when the capacitance reaches a peak in temperature[107]. In classic inorganic ferroelectric materials, this transition peak is generally well defined. However, because relaxor-ferroelectrics consist of a degraded ferroelectric behaviour the peak may appear broader. In Figure 2.23 b) we can see that the terpolymer's T_C peak is approximately $35\text{ }^\circ\text{C}$ at $\approx 200\text{ Hz}$ and increase with frequency to approximately $55\text{ }^\circ\text{C}$ at 1 MHz .

Polarisation wise, this transition impacts the cycle in two different ways. An increase in temperature up to the T_C will translate to a gain in maximal polarization (P_{max}). However, if the temperature is further increased, P_{max} will begin to decrease (Figure 2.24 b)). Despite a similar decreasing trend in both capacitance and polarization (Figure 2.23 b)), one can notice that the peak temperature for P_{max} is not equal to the one seen for capacitance. One possible cause of this discrepancy can be attributed to the fact that the capacitance (measured at 0 V) and the maximal polarisation are respectively the response for small and large signals. Furthermore, the different values of electric field necessary to extract each of these parameters could also be a origin of this difference.

The second impact of this temperature related transition affects the hysteretic behaviour of the polarization cycles. As the T_C is a temperature above which the ferroelectric interaction is screened, no hysteresis should be observable if the temperature is further increased. However, we can notice in Figure 2.24 a) that a large hysteresis is present at high temperature (above $50\text{ }^\circ\text{C}$) which is in contradiction with the theory. However, extraction of the remnant polarization with temperature (Figure 2.24 b)) indicates an initial drop in P_r . This decrease in hysteresis size is consistent with the one expected in the case of the Curie transition and should in theory be null when the material reaches a paraelectric state.

When the temperature is further increased the P_r rises to values even larger than the one observed at ambient temperature. However, it is also noticeable that the polarization cycle at high temperature ($T = 63.5\text{ }^\circ\text{C}$) does not exhibit any of classic relaxor-ferroelectric aspects (saturation, DHL ect...). Since this type of cycles are

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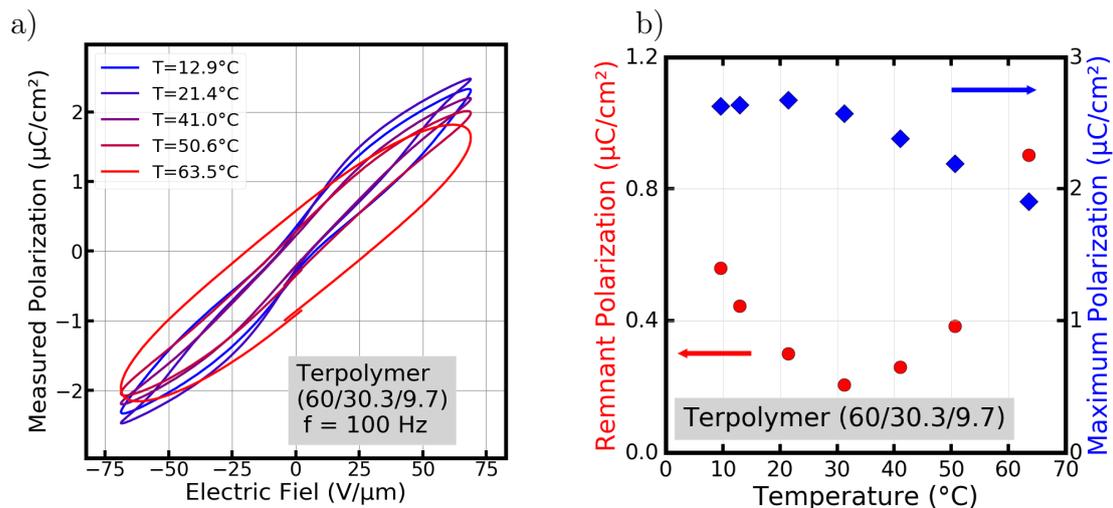


Figure 2.24: a) Evolution of polarization cycle (input signal: 100 Hz sinusoid) with temperature of P(VDF-TrFE-CTFE) (60/30.3/9.7) and b) extraction related of maximal polarisation (here $P_{max} = P(60 V.\mu m^{-1})$) and remnant polarization ($P_r = |P(0 V.\mu m^{-1})|$).

generally attributed to lossy dielectric, we can infer that the increase in “remnant” polarization could be attributed to an activation of conduction with temperature rather than to an actual ferroelectric related hysteresis. Similarly to the low speed measurement, this surge in leakage should not have an impact on the transistor hysteretic behaviour as the conduction charge are not bound in the dielectric. As a result, no hysteresis related to the RFE behaviour should be observed in the transistor transfer curve above the T_C .

Conclusion 2.4 (Composition and temperature) *The RFE behaviour of the terpolymer is primarily governed by its chemical composition, we thus selected a high CTFE content polymer for its thinner hysteresis and high permittivity. Furthermore, bias, frequency and temperature also heavily impact the polarization response of the high- κ dielectric. Because of the impact of leakage on polarization measurement, it is not always easy to differentiate it from actual polarization. However, since the transistor is not sensitive to leakage, this issue should not have a significant impact on its characteristic.*

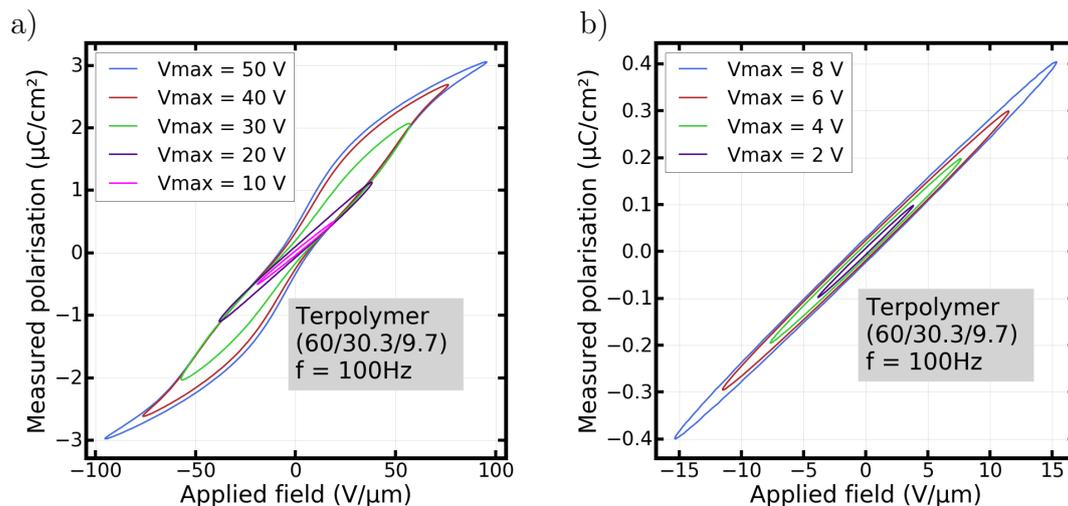


Figure 2.25: Evolution of polarization cycle with input signal with increasing bias amplitude (100 Hz sinusoid) a) full amplitude and b) zoom at low field (Sample thickness: 520 nm; Max bias: 56 V).

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2.3.1 Non-linearities with bias

The theoretical equations of drain current in transistors (Equations (1.2) and (1.3)) assume that the insulator layer behaves like an ideal dielectric, it is thus obvious that instabilities in the dielectric will affect the extracted mobility, threshold voltage and subthreshold swing. When considering the evolution of the terpolymer's capacitance with bias in Figure 2.21 b) we can observe a fair amount of variability even in the unsaturated region which might generate problematic extractions in the final transistor structure. However, capacitance measurements only inform on the small signal response of the material (level = 0.1 V) and as such polarization measurements might be better suited to probe the dielectric behaviour in similar electrical conditions to the one encountered for the transistor characterization.

The evolution of polarization behaviour with increasing V_{max} (Figure 2.25 a)) indicates that the saturation in polarization only occurs at high field value. However, when at low field (Figure 2.25 b)), the polarization cycle is equivalent to the response produced by a lossy linear dielectric. Electrically, this type of response can be

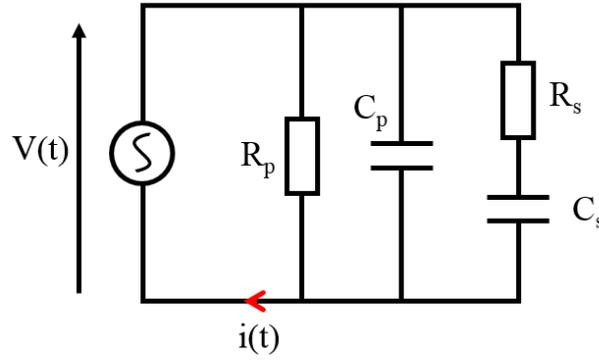


Figure 2.26: Electrical schematic of a parallel and series RC circuit returning a polarisation profile comparable to a lossy dielectric.

modelled with series and parallel RC circuits (Figure 2.26 a)).

We would like to stress the fact that this model does not hold any real physical meaning concerning the relaxor-ferroelectric material as the origin of hysteresis is more likely to be caused by the RFE behaviour rather than by an actual dielectric loss. However, a fitting model could indicate the presence of a linear-like behaviour within this voltage window.

Each branch of this circuit generates a specific polarization response to a sinusoidal input voltage (Equation (2.13)).

$$V(t) = U \sin(\omega t) \quad (2.13)$$

When the current passing through each branch is summed and integrated, it produces a polarisation profile similar to the one observed in the terpolymer at low field (Figure 2.27). The major contribution to the capacitive response of the material is provided by the parallel capacitor (Equation (2.15)), the parallel resistor contribution fitting the hysteresis width (Equation (2.14)). In this circuit, each branch displays a specific charge response to a sinusoidal input

$$q_{R_p}(t) = \frac{U}{R_p} \left(1 - \frac{\cos(\omega t)}{\omega}\right) \quad (2.14)$$

$$q_{C_p}(t) = C U \sin(\omega t) \quad (2.15)$$

$$q_{R_s C_s}(t) = \frac{1}{\sqrt{\omega^2 + \frac{1}{\tau^2}}} \frac{U}{R_s} \left(\sin(\omega t + \phi) - \sin(\phi) e^{-\frac{t}{\tau}} \right) \quad (2.16)$$

$$\text{With } \tau = R_s C_s \quad \text{and} \quad \phi = \arctan(\omega \tau) \quad (2.17)$$

The fitting of a stable hysteresis cycle could be achieved with a simple parallel RC circuit as mentioned prior. However, this simple circuit would not be able to fit the transitional regime in the beginning of the measurement and as such it would require to manually off-center the raw data to achieve adequate fit. However, with its fading exponential (Equation (2.16)), the RC series branch can adequately replicate this behaviour. Once the elapsed time is larger than the time constant of the series RC branch (τ) the steady state is achieved and produce a stable hysteretic cycle (Figure 2.27 c)).

When conducted on the terpolymer's polarization cycle, the fit closely matched the polarization response at low field (Figure 2.28 a)). However, we can see in Figure 2.28 b) that when at high voltage, the parallel/series RC model cannot fit the cycle any more because the saturation and DHL introduced by the RFE behaviour are unable to replicate with simple linear components. The coefficient of determination of a model is a good indicator of the quality of the fit between the data and model and we can observe the evolution of this coefficient with the maximal applied voltage in Figure 2.29. The model/data agreement begins to decrease when the maximal applied electric field reaches $40 \text{ V} \cdot \mu\text{m}^{-1}$, indicating the end of the linear-like behaviour window.

2.3.2 Low- κ dielectric as a buffer layer for the high- κ relaxor-ferroelectric

If we consider the thicknesses and voltages commonly used in organic transistor devices (ie: sub-micron and generally above 20 V), we can conclude that the window of linear-like behaviour in the terpolymer is relatively narrow for the TFT application. However, we mentioned in Chapter 1 that because of their incompatibilities with

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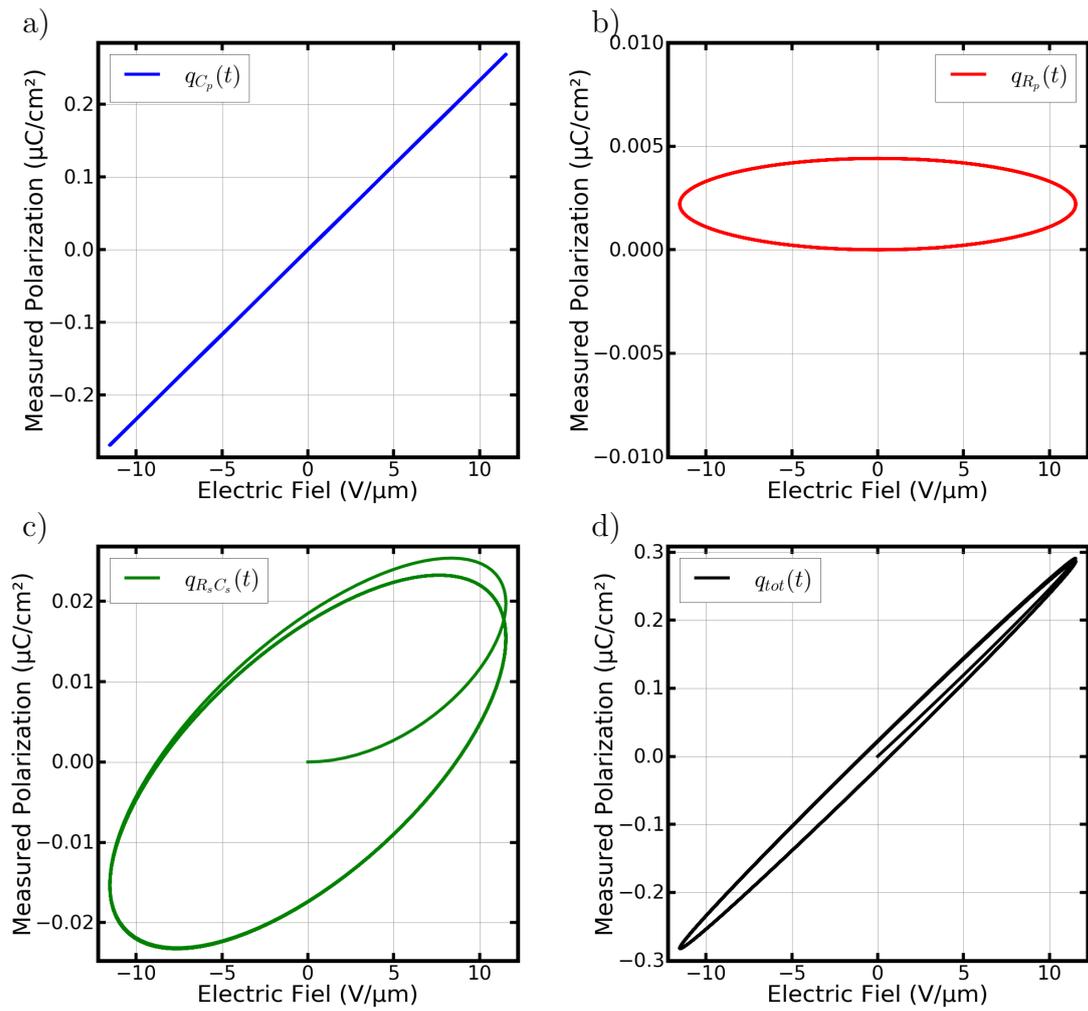


Figure 2.27: Equivalent polarization response for a) the parallel capacitor (C_p), b) the parallel resistor (R_p), c) the RC series branch ($R_p C_p$) and d) for the full equivalent circuit.

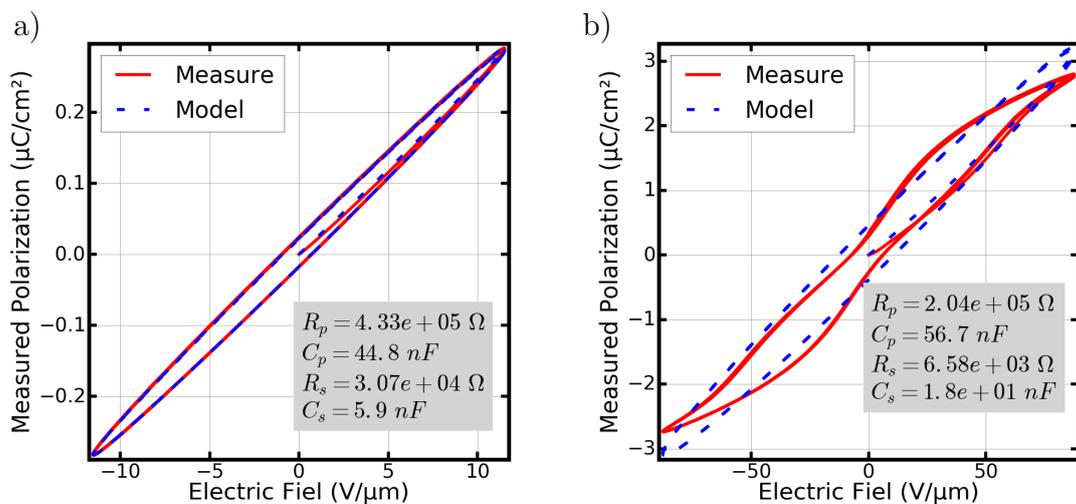


Figure 2.28: Comparison of fitted model versus raw polarization at a) low field and b) high field.

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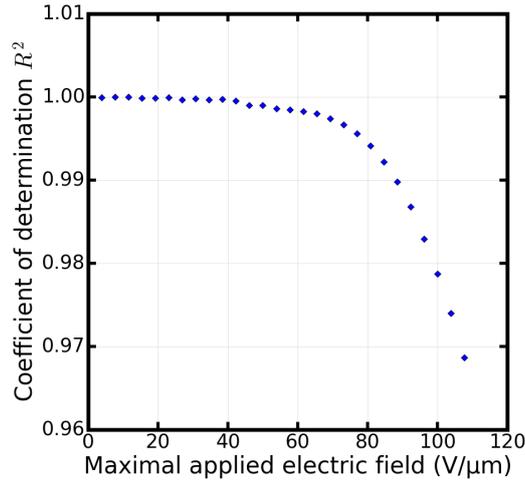


Figure 2.29: Evolution of the parallel/series RC model coefficient of determination with the maximal applied field on the terpolymer.

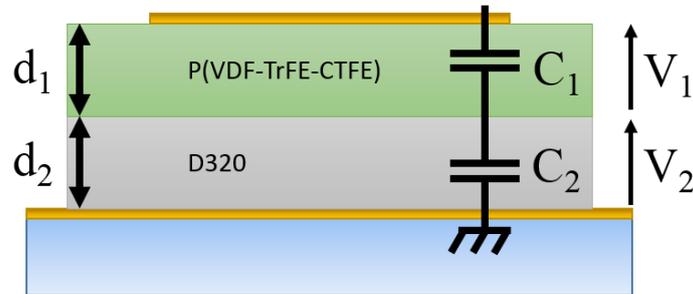


Figure 2.30: The general bilayer structure used in this work and its electrical equivalent approximated with capacitors.

organic semiconductors, high- κ materials are not often used as stand-alone gate dielectric. The common structure proposed in the literature consists of a thin low- κ material and a thicker layer of high- κ : this type of structure is referred to as bilayer dielectric [28, 44–47].

From an electrical standpoint, the bilayer structure is equivalent to two capacitors in series. As such it verifies the principle of charge conservation stating that the net charges present at the two capacitors' terminals are identical:

$$Q_{tot} = Q_{D320} = Q_{PVDF} \quad (2.18)$$

With Q_{tot} the global charge at the electrodes, Q_{D320} the charge at the low- κ 's interface and Q_{PVDF} the one at the terpolymer's interface.

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If the electric field applied to the terpolymer layer is well below $40 \text{ V} \cdot \mu\text{m}^{-1}$ its behaviour might be approximated to a linear dielectric. Assuming this working hypothesis, Equation (2.18) becomes:

$$C_{eq}V_{tot} = C_2V_2 = C_1V_1 \quad (2.19)$$

With C_1 , C_2 and C_{eq} the respective capacitance of the P(VDF-TrFE-CTFE), low- κ and the equivalent capacitance of the stack (Figure 2.30). V_1 , V_2 and V_{tot} the voltage across the terpolymer layer, the D320 layer and the whole stack respectively. We can also define X as the fraction of the terpolymer layer in the total bilayer dielectric :

$$d_{tot} = d_1 + d_2 \quad (2.20)$$

$$d_1 = Xd_{tot} \quad (2.21)$$

$$d_2 = (1 - X)d_{tot} \quad (2.22)$$

With the help of Equation (1.16) and the assumption of linear behaviour we can evaluate the equivalent dielectric constant of the stack (ε_{eq}) as well as the portion of voltage applied to the terpolymer material:

$$\varepsilon_{eq} = (d_1 + d_2) \frac{\varepsilon_1 \varepsilon_2}{\varepsilon_1 d_2 + \varepsilon_2 d_1} \quad (2.23)$$

$$= \frac{\varepsilon_1 \varepsilon_2}{\varepsilon_1 (1 - X) + \varepsilon_2 X} \quad (2.24)$$

$$V_1 = \frac{V_{tot}}{1 + \frac{\varepsilon_1 d_2}{\varepsilon_2 d_1}} \quad (2.25)$$

$$= \frac{V_{tot}}{1 + \frac{\varepsilon_1 (1 - X)}{\varepsilon_2 X}} \quad (2.26)$$

As can be inferred from Equations (2.24) and (2.26), the final properties of the low- κ /high- κ bilayer dielectric are critically dependent on the ratio of their two permittivities and on the fraction of terpolymer in the bilayer.

To corroborate our linear behaviour hypothesis, we have fabricated bilayer capacitors with an increasing low- κ thickness. The fabrication of these samples followed the process described in the early part of this chapter and the respective solutions

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Table 2.1: Fabrication details for an array of bilayer capacitors with increasing D320 thickness.

		A	B	C	D
Low- κ D320	weight content (%)	4	4	7.5	7.5
	spin speed (<i>rpm</i>)	4000	1000	4000	1000
	measured thickness (<i>nm</i>)	62.4 ± 1.7	119.4 ± 1.7	333.2 ± 5.6	626.6 ± 48.9
P(VDF-TrFE-CTFE) (60/30.3/9.7)	weight content (%)	6	6	6	6
	spin speed (<i>rpm</i>)	1200	1200	1200	1200
	measured thickness (<i>nm</i>)	612.7 ± 10	618.5 ± 18.2	604 ± 8	611 ± 23
Fraction of terpolymer	<i>X</i> (%)	90.8	83.7	64.5	49.4

and spin speed used in their fabrication is listed in Table 2.1. The evolution of the equivalent permittivity with the low- κ layer thickness closely follows the predicted theoretical trend which indicates that bilayers effectively behaves in a linear fashion at low field (Figure 2.31).

The bilayer's polarization profile presents an improved maximal polarization when compared to the low- κ dielectric and a reduced hysteresis when compared to the RFE (Figure 2.31 b)). This trade-off between the properties of two materials can be tailored with the tuning of the thickness ratio. The modularity of the bilayer dielectric makes this structure a good candidate for organic transistors in general.

We used the same RC circuit fit described prior to evaluate the evolution of linearity in the bilayer structure (Figure 2.32 a)). Like for the terpolymer, a good fit is returned at low maximal field and the critical field value for this bilayer is more than three time larger than the one observed in the raw terpolymer. Moreover, we can see in Figure 2.32 b), that the measured capacitance of the bilayer is quite stable

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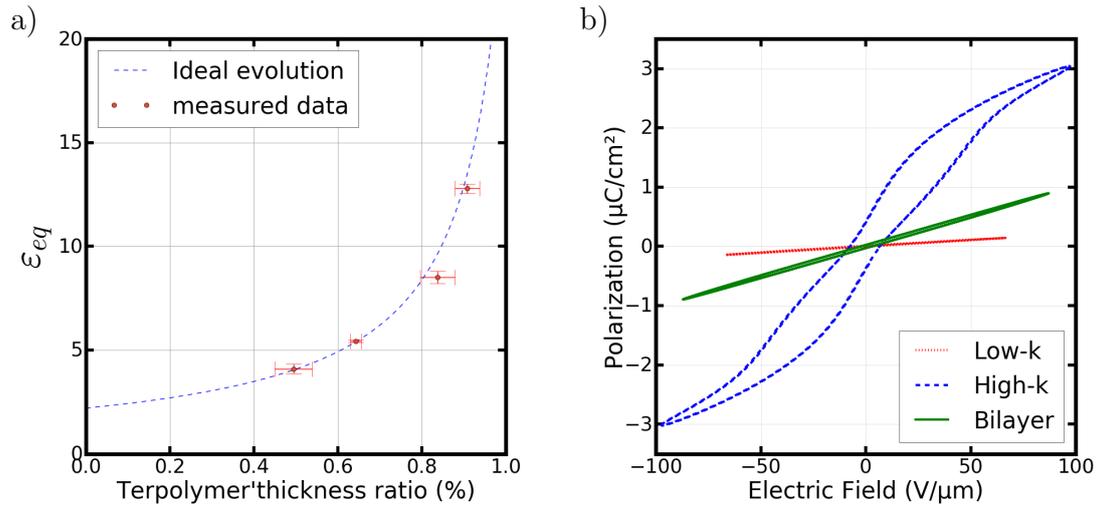


Figure 2.31: a) Evolution of the bilayer's equivalent dielectric constant with the terpolymer's thickness ratio (acquired from capacitance measurement $1kHz$) and b) comparison of polarization for the terpolymer, a bilayer ($X \approx 90\%$; $d_{tot} = 540\text{ nm}$) and the low- κ (100 Hz sinusoidal input signal).

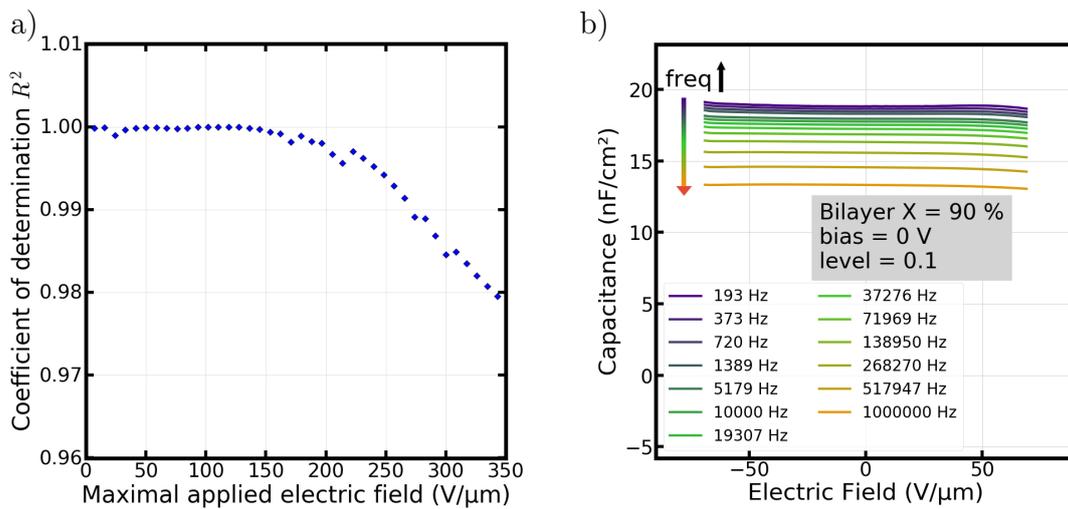


Figure 2.32: a) Evolution of the coefficient of determination for a parallel/series RC model fitted to the bilayer's polarization and b) capacitance measurement versus bias at different solicitation frequencies for a bilayer dielectric ($X \approx 90\%$)

with bias in a similar fashion to the low- κ . However, we can also notice a decrease of the bilayer's capacitance with frequency, a behaviour that may be inherited from its terpolymer subcomponent.

Conclusion 2.5 (Bias stability and bilayer dielectrics) *In addition to the hysteresis, the terpolymer's dielectric response is not extremely stable with bias. With the help of a RC model we estimated that it retained a linear-like polarization behaviour up to a maximal voltage of $40 \text{ V}\cdot\mu\text{m}^{-1}$. However, high- κ are rarely implemented alone in transistors and are often used in conjunction with a thin low- κ buffer layer. Effectively, this layer acts as a capacitor in series and thus lowers the effective permittivity of the bilayer but extends its window of linearity. As a result, the bilayer is more bias-stable and displays reduced hysteresis when compared to the raw terpolymer.*

2.4. CHAPTER CONCLUSION

In this chapter we explained that the capacitance, permittivity and polarization are the resulting sum of multiple microscopic responses to an external electric field. In theory, each physical component of the dielectric material could be tailored to maximize the global polarization response. However, each of these microscopic phenomena may have specific response to the applied bias or frequency and thus measurement protocols should always be carefully established and reported when discussing dielectric parameters.

In dielectrics, a higher molecular moment will increase the permittivity since the rotation of such dipole with the field will bring a larger quantity of charge to the interface. However, it may also come at the cost of linearity as once these dipole are aligned with the field they no longer contribute to the local variation of charge and thus induce a saturation in the polarization. Furthermore, the interaction between ordered dipoles may potentially screen an external electric field thus produced a ferroelectric or relaxor-ferroelectric behaviour.

The polyvinylidene fluoride regroups both of these traits with a high permittivity (for a polymer) and an hysteresis in polarization. In order to improve this FE behaviour, the material was chemically modified by integrating another monomer in

the chain thus producing a copolymer : the P(VDF-TrFE). The random placement of the TrFE units in the chain promoted the formation of a specific crystalline structure with high ferroelectric properties (β phase).

After the observation of improved permittivity in the irradiated copolymer was attributed to the creation of microscopical defects in the crystallites, introduction of another more bulkier monomer in the chain was proposed. Both the P(VDF-TrFE-CTFE) and the P(VDF-TrFE-CFE) terpolymers present some of the highest permittivity observed in polymers. We demonstrated that the ratios of monomers in the chain plays an important role in the relaxor-ferroelectric behaviour and that a high CTFE content in the chain enables an increased dielectric constant while reducing the hysteresis width. As a result we chose to study the P(VDF-TrFE-CTFE) (60/30.3/9.7) since it was the composition with the highest CTFE content available to us.

With capacitance and polarization measurements, we demonstrated that the dielectric properties of the terpolymer are highly impacted by the bias and frequency of the acquisition. This behaviour could be attributed to the high dipolar density in the chain. With the help of capacitance/temperature measurements we identified a transition similar to a Curie temperature above which no RFE behaviour should be observed. However, because of the principle of polarization measurement; which also integrates leakage current; hysteresis-less polarization cycle could not be observed.

We then used a RC circuit mathematical model to probe the evolution of a potential linear-like polarization windows in the high- κ . The terpolymer's polarisation cycles were adequately fitted with the model up until a maximal voltage of $40 \text{ V} \cdot \mu\text{m}^{-1}$ above which the saturation started to take place.

Finally we evaluated the impact of a low- κ buffer layer deposited prior to the high- κ layer as it is the common structure used for transistors with this type of materials. We demonstrated that despite the non-linearities present in the terpolymer, the bilayer's equivalent dielectric constant behaved like two linear capacitors in series when at low field. The polarization response of the bilayer structure appeared to be

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a trade-off between the low- κ and the RFE as it displayed reduced hysteresis and lowered maximal polarization when compared to the raw terpolymer. Capacitance measurements and the fit of RC model indicated an improved bias stability in the bilayer structure while the instability in frequency introduced by the terpolymer were still present.

With its improved permittivity (compared to the classic low- κ) the bilayer structure in general is a promising dielectric candidate for low-voltage transistors. As such impact on the transistor's performance will be studied in the following chapter.

Integration of P(VDF-TrFE-CTFE) for low voltage solution processed organic thin film transistors

In order to accurately understand the impact of the high- κ dielectric on organic transistors, we will first evaluate the behaviour of a classic low- κ dielectric based transistor that will serve as reference for the rest of this study. In the first part of this chapter we will discuss the fabrication and an in depth characterization of a low- κ OTFT as a reference. Then we will assess the requirements for the implementation of the high- κ dielectric and its impact on the transistor behaviour. Subsequently we will evaluate a first proof of concept for a transistor implementing a bilayer as gate insulator (low- κ /high- κ) and evaluate the impact of the low- κ buffer layer thickness on the overall transistor performance. Finally, we will discuss the fabrication of an optimized bilayer structure for low-voltage transistors able to operate below -3.3 V.

3.1. LOW- κ REFERENCE TRANSISTOR : FABRICATION AND CHARACTERIZATION

3.1.1 Material and process

The fabrication process was carried out in a class 1000 clean room environment in order to limit any air-born contamination like dust particles. A $125\ \mu\text{m}$ thick sheet of Polyethylene naphthalate (PEN) with pre-lithographed gold contacts was used as a flexible substrate. The main source/drain layout used throughout this work is referred to as “Backplane”, it is separated in four quadrants (Figure 3.1), which each serve different purpose. Transistors studied in this work mostly came from the upper right quadrant ($Q2$) and lower right quadrant ($Q4$). The $Q2$ is composed of 196 identical multi-fingered transistors with a width of $500\ \mu\text{m}$ ($4 \times 125\ \mu\text{m}$) and a length of $20\ \mu\text{m}$ (Figure 3.1 b)). The lower right quadrant ($Q4$) had two purpose : evaluating the contact resistance as it consists of a large array of transistors in a TLM configuration (varying length and width) and measuring the dielectric’s properties with an array of capacitors.

Each substrate came with a plastic liner to limit any external contamination, once

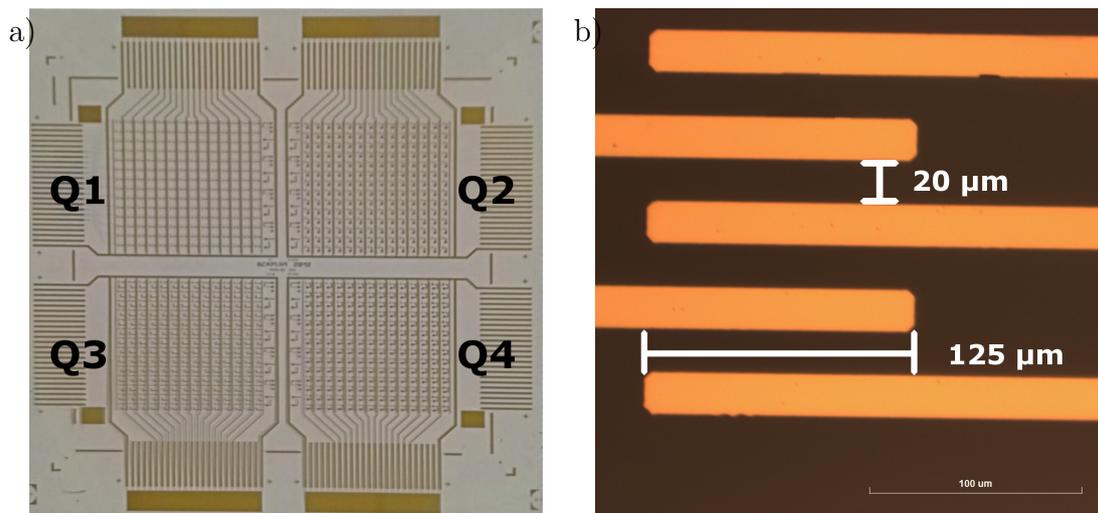


Figure 3.1: a) Layout of the “Backplane” substrate with gold electrodes and b) source/drain microscopy of the 500/20 transistors.

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this liner was removed, the flexible substrate underwent a temperature treatment at 100 °C to remove any residual strain in the polymer sheet. The substrate was then cleaned via an O_2 plasma before the actual fabrication process. The self assembly monolayer (SAM) was deposited in bath of M001 solution for a minute, washed twice with isopropyl alcohol (IPA), dried with compressed air and then annealed at 115 °C. The SP400 Semiconductor layer was deposited via a spin-coating method. To reach a thickness of 30 nm, the solution was spun at 1400 rpm for 30 s and then annealed at 100 °C. Prior to the deposition of the dielectric layer, the semiconductor was stripped from the capacitor zone in Q4 with the help of cotton swab and toluene solvent. The low- κ dielectric layer was then spun from a decane solution at a desired concentration for 30 s and annealed at 115 °C.

In the case of the classic reference structure, this layer was directly followed by the gate deposition. For a bilayer structure, a section of the Q4 capacitor was again cleaned with toluene to produce a low- κ free zone in order to produce a pristine terpolymer layer of identical thickness to the one in the bilayer. The desired terpolymer would be spun from a cyclopentanone solution for 30 s and annealed at 115 °C. A 150 nm gold gate was then finally deposited via thermal evaporation under vacuum to finish the transistor stack. Spin speed and the polymer weight concentration in the solution were the two main parameters influencing the final thickness of the both types of dielectric layers.

The first step of our study was to produce a standard transistor structure (Figure 3.2 b)) to serve as a reference against which we could compare the performance of bilayer transistors and identify newly introduced behaviours. To fabricate this structure we used a 12.5 % solution (D320-DEC-125) spun at 1000 rpm for the insulating layer deposition. The thickness of the produced layer was measured at 637 ± 17 nm with an average capacitance of 3.06 ± 0.12 nF.cm⁻¹. However, a measurement protocol had to be established prior to the electrical characterization of this structure.

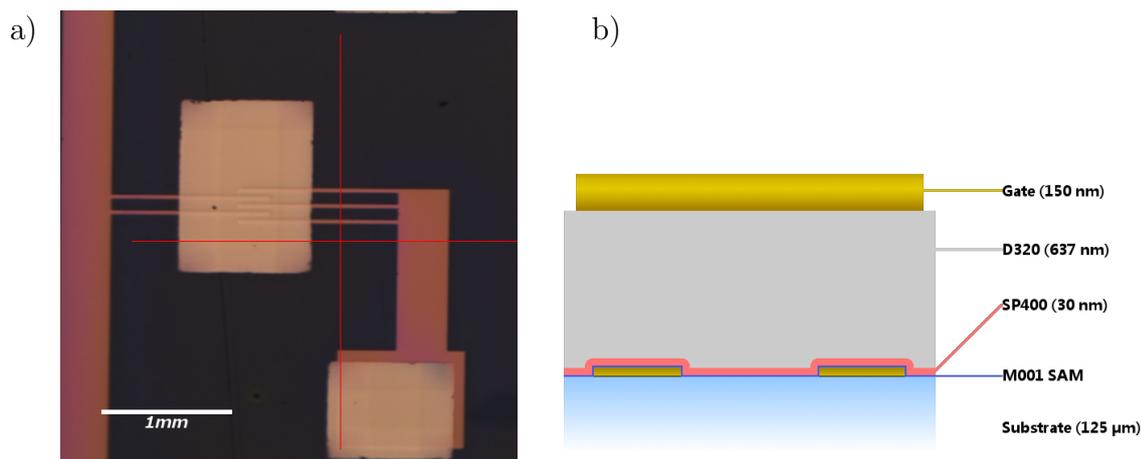


Figure 3.2: a) Microscopy of the fully finished device b) cross-cut schematic of the reference transistor stack.

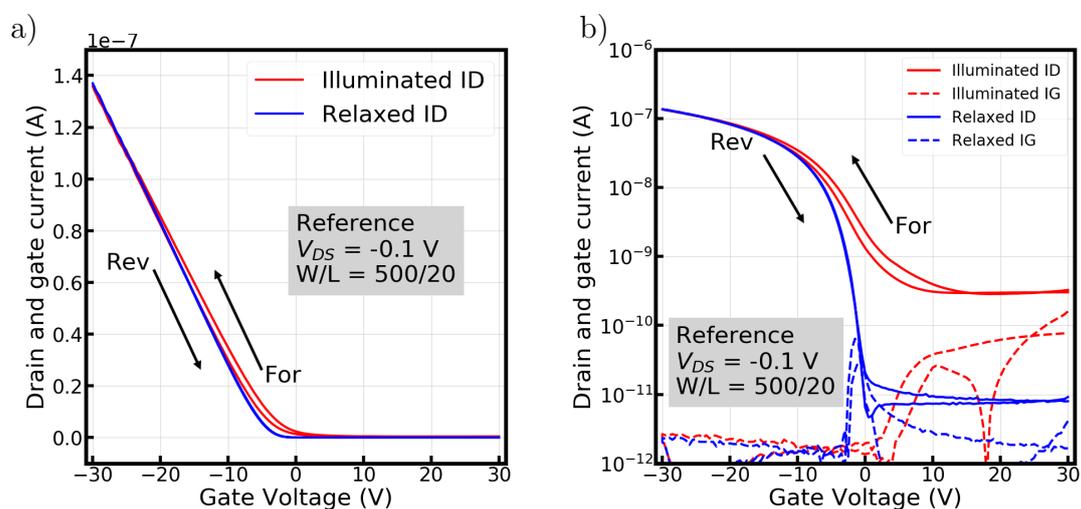


Figure 3.3: Transfer curve of an organic transistor under illumination (red) and after several hours in the dark (blue) in a) linear scale and b) logarithmic scale.

3.1.2 Light sensitivity

Like most semiconductors based devices, organic transistors are often photosensitive. Meaning that their properties may change when illuminated[108]. However, contrary to photodiodes or photovoltaic cells, this effect is generally unwanted in transistors as it introduces variability in the performance.

Generally, the contact between the transistors terminals (Gate, Source and Drain) and the semiconductor analyser is achieved through the help of SMU probes that are placed via the help of a microscope. By doing so, the transistors is exposed to the

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powerful light used in microscopes (in our case : eVue III pro microscope equipped with white LED lights), thus changing properties of the OSC.

To illustrate the photo-sensitivity of our devices, we measured one of our reference transistor under illumination and after ten hours in the dark (Figure 3.3). Under illumination, the OFF current was higher by more than one decade which would drastically impact the subthreshold swing of the device. Our transistors were first measured in the forward direction ($\|V_{GS\ max}\|$ to $-\|V_{GS\ max}\|$) and then in the reverse direction ($-\|V_{GS\ max}\|$ to $\|V_{GS\ max}\|$), an anticlockwise hysteresis was visible in the illuminated transistor's characteristic whereas none was discernible when the photo-activation was relaxed (Figure 3.3 b)).

In order to extract the adequate transistor parameters and generate reproducible measurement conditions, we evaluated the minimum "relaxation" time needed to reach a stable operating regime. We monitored the decrease of current between the source and drain electrode ($V_{DS} = -0.1\ V$; $V_{GS} = 0\ V$) after turning the microscope's light off ($t_{OFF} = 10\ s$) (Figure 3.4 a)). To avoid any potential degradation caused by a long electrical sollicitation, only the first hundred seconds were measured under constant bias. After this initial period, the evolution was monitored through small logarithmically spaced sollicitations (5 s each).

The increased conductivity induced by the photoactivation displayed an extremely small time constant as the measured current approximately gained two orders of magnitude in less than a minute of light exposure and reached a stable regime in approximately ten minutes (Figure 3.4 a)). However, the relaxation of this phenomenon was extremely low by comparison as it took at least three hours to decrease the drain current by two orders of magnitude and the stable regime was not reached after several hours(Figure 3.4 a)). As a compromise between performance stability and practicality, a systematic three hours darkness delay was conducted prior the characterisation of transistors.

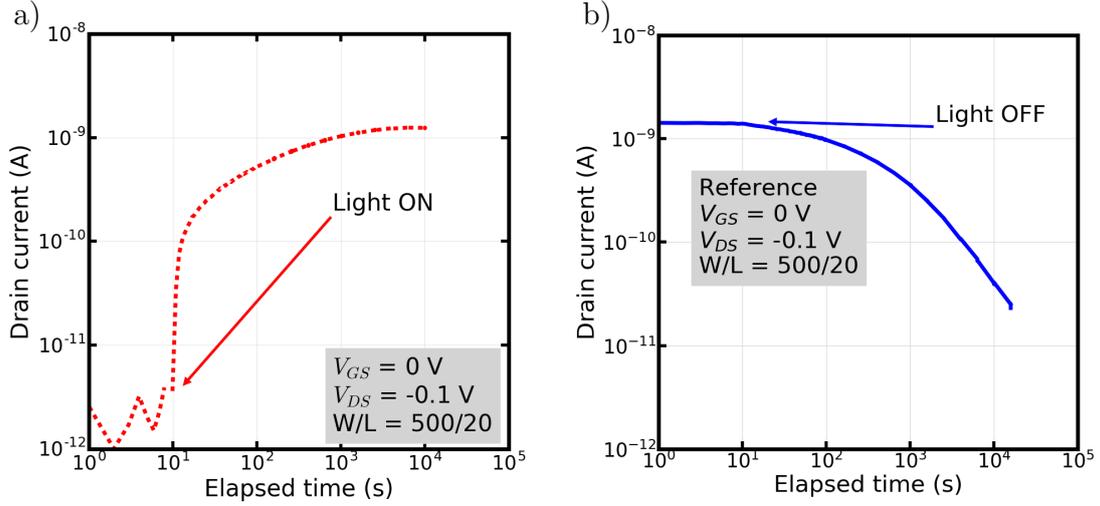


Figure 3.4: Evolution of current with the photoactivated conduction versus time a) excitation b) relaxation.

3.1.3 Electrical characterization of the reference

Whether in saturation or linear regime, no noticeable deviation from ideality (ie: large hysteresis, dual slope or curvature in the linear regime) was observable in the transfer curves of this reference structure (Figure 3.5). Moreover, the device displayed standard performance for this type of OTFT : $V_{th\ lin} = -5.3\ V$, $\mu_{eff\ lin} = 0.67\ cm^2.V^{-1}.s^{-1}$ and $I_{ON}/I_{OFF} \approx 10^4$. It should be noted that despite what could be observed on Figure 3.5 a) a small anticlockwise hysteresis of approximately $100\ mV$ (ie: $\Delta V = V_{forward}(1\ nA) - V_{reverse}(1\ nA)$) was still present in both regimes. The positive sign of this hysteresis could be compatible with carrier trapping at high gate voltage, yet it remained insignificant relative to the maximal applied voltage. A variability study of the performance for the full foil should be conducted to fully establish this structure as our reference.

The transfer measurement in linear regime for the 196 TFT in Q2 for the reference structure can be found in Figure 3.6 (saturation regime available in Annex). In this foil, the main cause of defectiveness was found to be either from an excess of leakage or defects in the stack (ie: particles), thus any transistors with abnormal leakage current ($I_G(-30\ V) > 10^{-9}\ A$) was considered to be non functional. As a result the yield of working devices in this quadrant was approximately 87 %.

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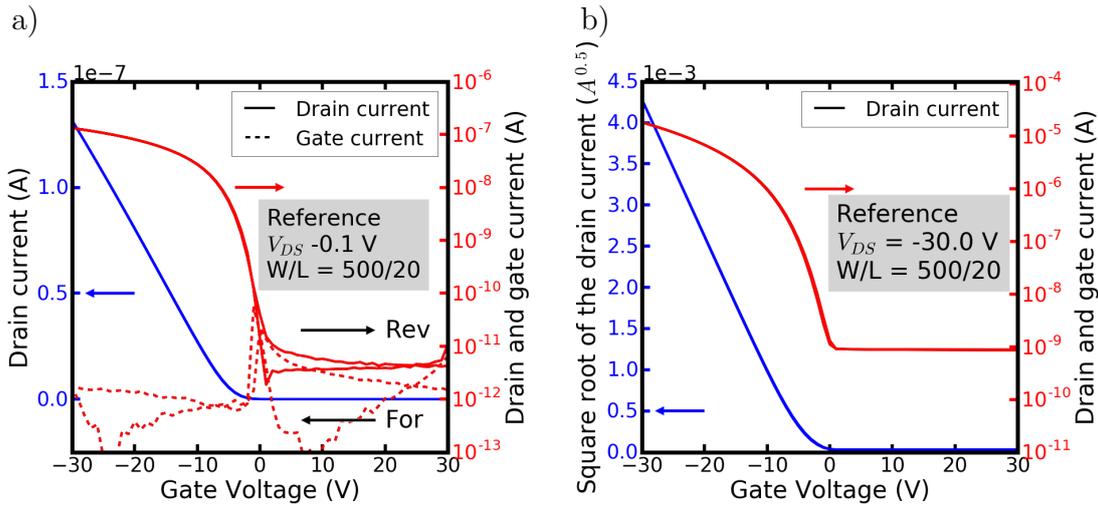


Figure 3.5: Low- κ transfer curves of the reference structure in : a) linear regime and b) saturation regime.

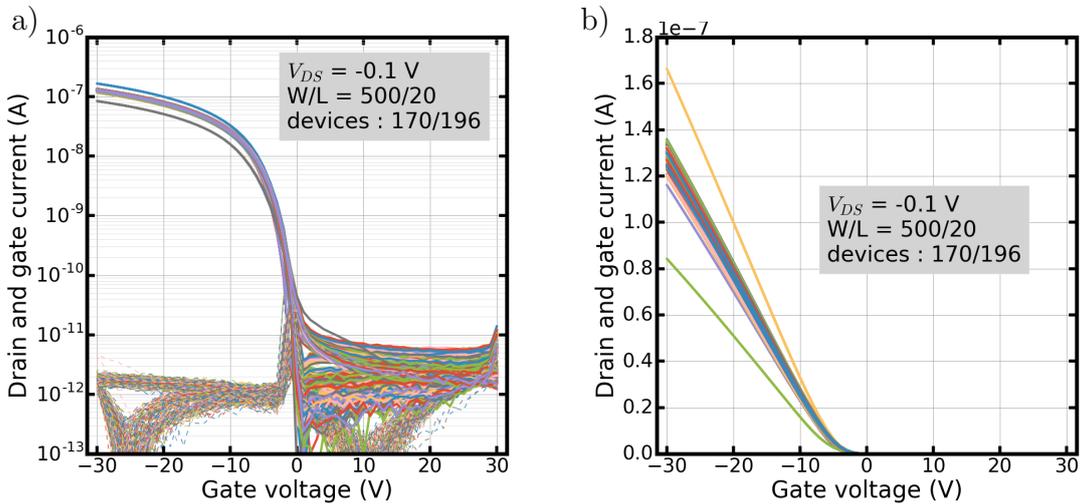


Figure 3.6: Linear regime transfer curves for the full Q_2 of the reference foil in a) logarithmic and b) linear scale.

The spread of transfer curves for this foils of transistor appeared to be relatively narrow, except for two outliers, whether in logarithmic or linear scale (Figure 3.6). This indicated a good device-to-device reproducibility over the whole quadrant. However, to discuss the variability in a more quantitative approach, we regrouped in Table 3.1 the median and standard deviation of the key parameters generally used in transistors characterization. The low standard deviation of each parameters (usually below 10 % of the median value) indicated that the performance disparity remained quite low across the quadrant. Moreover, to the exception of the subthreshold swing (and thus the N_{it}), the parameters extracted from the forward direction (positive

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Table 3.1: Extracted parameters for the second quadrant of the reference structure (median \pm standard deviation) .

Sample	Mode	Direction	μ_{eff} ($cm^2.V^{-1}.s^{-1}$)	V_{th} (V)	SS ($V.dec^{-1}$)	N_{it} (cm^{-2})	ΔV at 1 nA (V)	I_{ON} (A) ($V_{GS} = -30 V$)
Low- κ Reference $C_i = 3.06 nF.cm^{-2}$	Linear $V_{DS} = -0.1 V$	Forward	0.69 ± 0.03	-4.79 ± 0.17	0.87 ± 0.14	$2.62e^{11} \pm 0.43e^{11}$	0.087 ± 0.028	$1.31e^{-7} \pm 0.06e^{-7}$
		Reverse	0.69 ± 0.03	-4.91 ± 0.17	1.79 ± 0.08	$5.58e^{11} \pm 0.25e^{11}$		
	Saturation $V_{DS} = -30 V$	Forward	0.70 ± 0.03	-3.98 ± 0.26	1.90 ± 0.2	$5.90e^{11} \pm 0.65e^{11}$	0.210 ± 0.050	$1.81e^{-7} \pm 0.09e^{-7}$
		Reverse	0.71 ± 0.03	-4.15 ± 0.29	1.90 ± 0.2	$6.36e^{11} \pm 1.96e^{11}$		

to negative gate bias) were similar to the one extracted from the reverse direction (negative to positive). The difference in the extracted SS for the linear regime could be explained by the mismatch in OFF current between the forward and reverse direction due to the dynamic transition in turn-off (illustrated by the black arrows in Figure 3.5 a)). These observation concerning the performance, disparity and overall yield of the foil consolidates our choice of structure for the reference transistor.

Typically, for this type of transistors, the drain voltage chosen for linear transfer curves is in the range of the volt, allowing to retain linear behaviour ($|V_{DS lin}| \ll |V_{GS} - V_{th}|$) whilst limiting the negative impact of contact resistance. However, because our structure was aimed to be compared to low-voltage transistors, an even lower drain voltage was required ($V_{DS lin} = -0.1 V$). We probed the access resistance to the channel at low voltage via the help of the TLM test structure integrated in $Q4$ (Figure 3.7 a)). The reference structure presented a contact resistance of approximately $4.0 \cdot 10^3 \Omega.cm$ for $V_{GS} = -30 V$ and $V_{DS} = -0.1 V$ which accounted for approximately 10 % of the total channel resistances for devices equivalent to the $Q2$ test structure. This R_C value was in the same order of magnitude to one encountered in the literature in similar structures[109]. Unfortunately, the proportion

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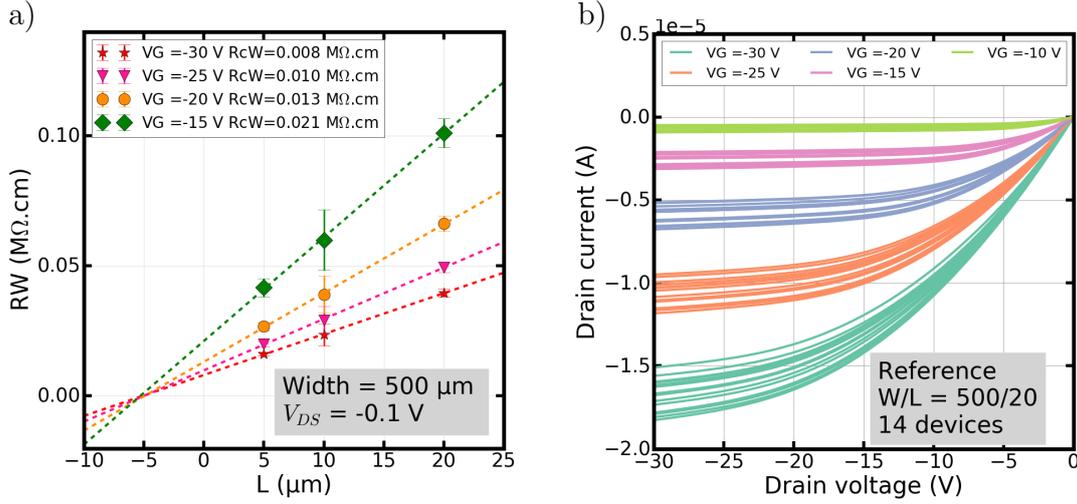


Figure 3.7: a) TLM for the reference structure performed on the $Q4$ and b) example of output curves for fourteen transistors with source drain layout equivalent to the devices in $Q2$.

of contact resistance to the whole channel resistance is not often commented and we could not find a suitable comparison in the literature.

Despite the measured R_C , no “S-shape” was observable at low-bias in the reference’s output curves (Figure 3.7 b)). Meaning that the contact between the electrodes and the channel remained ohmic despite the relatively high the access resistance. While a particular care to the impact of resistance on performance should be kept, these observation validates the low drain voltage measurement protocol.

Conclusion 3.1 (Reference and protocol) *To establish a strong baseline for our study we have fabricated an array of transistors based on the low- κ dielectric. Prior to the full characterisation of these samples we monitored the impact of light on the transfer curve of the standard device and established a “relaxation” protocol ensuring a consistent measurement of each transistor. The reference structure yielded a relatively narrow performance dispersion thus establishing a strong baseline for comparison purpose.*

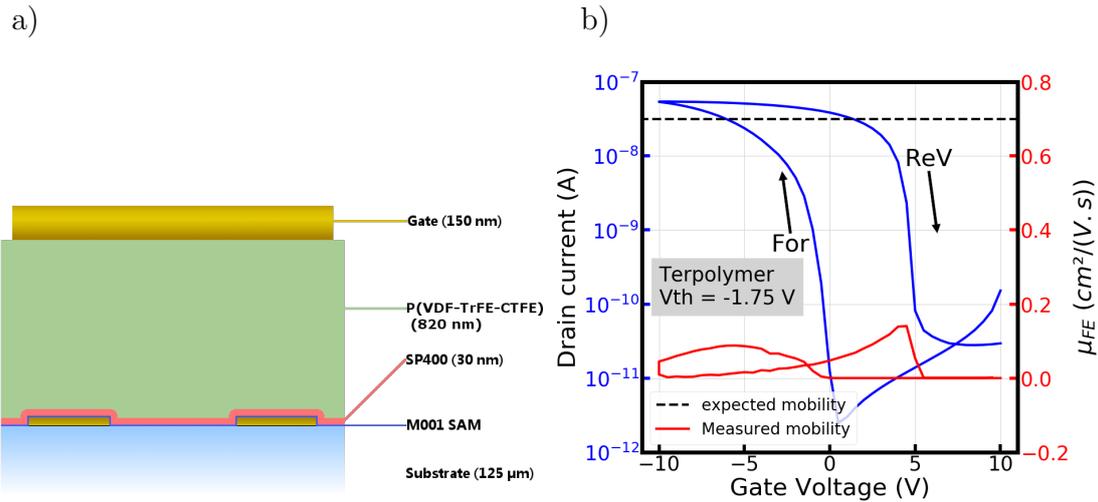


Figure 3.8: a) cross-cut schematic of the “full-terpolymer” transistor stack. and b) the transfer curve associated with such transistor.

3.2. TERPOLYMER INTEGRATION IN THE TRANSISTOR STRUCTURE

3.2.1 Direct integration

Integration of a high- κ dielectric directly onto the semiconductor has been documented in the literature and is generally reported to induce a degradation of the semiconductor performance[40–42]. However, and as explained in the Chapter 1, the relation between the crystalline structure of the semiconductor and the dielectric upon which it was deposited (bottom gate OTFT) is generally overlooked. In order to evaluate the detrimental effect of the high- κ on our semiconductor, we fabricated transistors using the only terpolymer as gate insulator Figure 3.8 a). A 6 w% terpolymer solution (solvent: cyclopentanone) was spun directly onto the semiconductor at 1500 rpm to produce an dielectric layer of approximately 820 nm with a capacitance of 37.8 nF.cm⁻².

From the characteristic found in Figure 3.8 b), it could be seen that the threshold voltage of the “full terpolymer” transistor ($V_{th} = -1.75$ V) was effectively lowered when compared to the reference. However, a noticeable drop in the semiconductors mobility ($\mu_{eff\ lin} \approx 0.09$ cm.V⁻¹.s⁻¹) alongside with a large hysteresis ($\Delta V(1$ nA) $\approx 0.5 * V_{GS\ max}$) was also present, thus supporting the reports of incompatibilities

2. TERPOLYMER INTEGRATION IN THE TRANSISTOR STRUCTURE

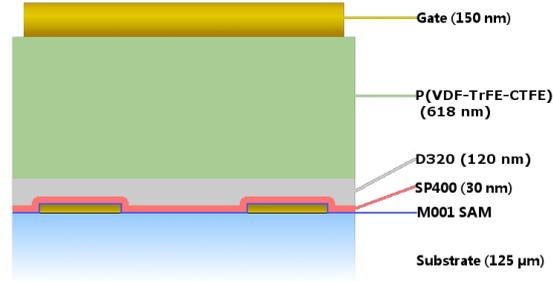


Figure 3.9: a) cross-cut schematic of the PoC_A transistor structure.

between semiconductors and high- κ materials. Moreover, most of the fabricated “full terpolymer” transistors presented a relatively high amount of leakage which further reduced the viability of this approach.

3.2.2 Introduction of the bilayer approach

In order to avoid channel degradation and retain a good interface quality, a low- κ layer is often used as a buffer layer between the semiconductor and the terpolymer[47, 110], This technique will be the main focus of this section. Following the previous observations concerning the degradation of semiconductor performance, we chose to begin the study of the bilayer transistor with the integration of a relatively thick layer of low- κ dielectric ($\approx 120 \text{ nm}$) when compared to some of the proof of concept reported in the literature[51, 56]. The main goal of this approach was to gain a first understanding the bilayer’s impact on the transistor prior to the optimization of its performance.

To fabricate these devices, we used a 4 $w\%$ low- κ (D320) solution in decane and a 5 $w\%$ terpolymer (P(VDF-TrFE-CTFE) 60/30.3/9.7) solution in cyclopentanone; both solutions were spun at 1000 rpm reaching a thickness of $120 \pm 5 \text{ nm}$ for the D320 and $618 \pm 20 \text{ nm}$ for the terpolymer (Figure 3.9). The resulting bilayer dielectric displayed a surface capacitance of $12.25 \pm 0.21 \text{ nF.cm}^{-2}$. In the rest of this chapter, this foil of transistors will be referred to as “PoC_A”.

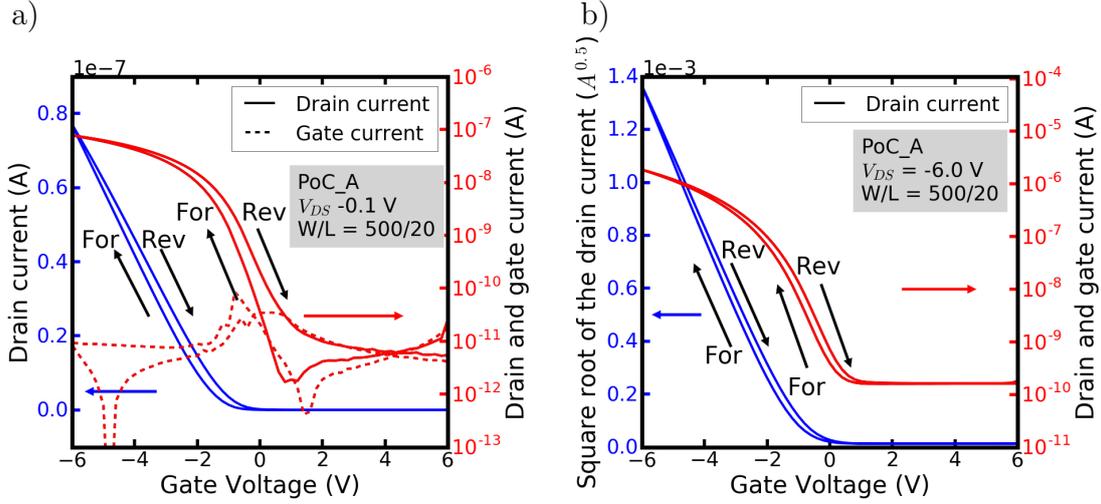


Figure 3.10: Transfer curves in a) linear and b) saturation regime for a median device from the PoC_A foil.

Two main differences from the reference foil can be seen in the PoC_A median transistor's transfers curves (Figure 3.10). First, this foil achieved a similar On current (here $\approx 7e-8$ A) at a fourth of gate voltage need for the reference foil. This evolution appeared to be coherent with the increase in gate capacitance introduced by the bilayer structure.

The second noticeable phenomenon was the apparition of a clockwise hysteresis, where the reverse drain current was higher than the forward drain current. Although this type of hysteresis could have been caused by various physical phenomena within the dielectric[111], we could confidently attribute it to the RFE behaviour still present in the bilayer dielectric's polarization profile. In this precise case, the width hysteresis between the forward and reverse curves was approximately 6.5 % of the maximal bias applied to the transistor. However, since the polarization hysteresis in the terpolymer dielectric could be impacted by frequency, so could be the current hysteresis in the transistor.

In order to be able to compare the two structure, both transistors should be in a similar operating state. As such, we set the maximal bias ($V_{GS_{max}}$) applied to each transistor to the point when their drain current would reach approximately 0.1 nA. Furthermore, to achieve equivalent duration for each measurement and regardless of the maximal applied voltage, a constant current acquisition time was

2. TERPOLYMER INTEGRATION IN THE TRANSISTOR STRUCTURE

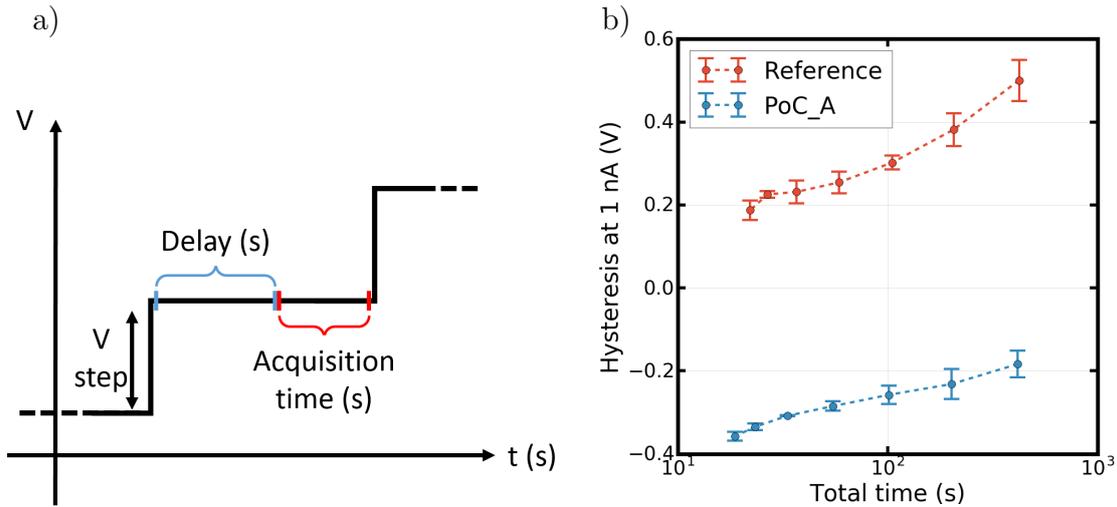


Figure 3.11: a) Illustration of the different time introduced by the acquisition of each data point in the transfer curve and b) the evolution of hysteresis versus the total duration of the transfer curve (Each curve represents the median of four devices).

set up along with a constant amount of voltage steps (ie: 200 data points for each curves) for the transfer curve measurement. Finally, a variable delay could be applied prior each acquisition (Figure 3.11 a)) in order to modulate the global length of the measurement.

With this speed variation protocol we were able to adequately compare the evolution of hysteresis in the reference and the PoC_A transistors (Figure 3.11 b)). Both curves appeared to follow a similar trend. However, since the two hysteresis were originally of opposite sign, it actually translated to an opening of the hysteresis for the reference and a closing of the hysteresis for the bilayer. The evolution of current hysteresis observed for PoC_A did not agree with the evolution of polarization hysteresis from Chapter 2 (Figure 2.22 b) as the terpolymer's measured polarization hysteresis should theoretically remain stable at long measurement duration (ie: in the absence of leakage). This led us to believe that both structure actually presented an equivalent trend but with a different starting point and that the origin of this positive hysteresis shift could find its source at the low- κ /semiconductor interface. However, more investigation might be need for a better understanding of the phenomenon at play.

The ON current dispersion displayed in Figure 3.12 was arguably larger than

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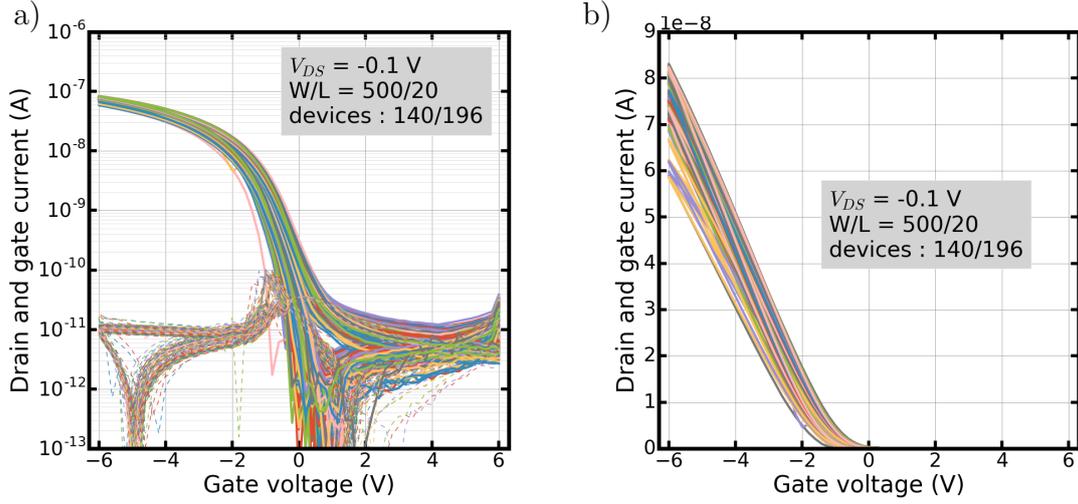


Figure 3.12: Transfer curves in a) linear and b) saturation regime for a median device from the PoC_A batch.

Table 3.2: Extracted parameters for the second quadrant of the PoC_A foil (median \pm standard deviation).

Sample	Mode	Direction	μ_{eff} ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	V_{th} (V)	SS ($mV \cdot dec^{-1}$)	N_{it} (cm^{-2})	ΔV at 1 nA (mV)	I_{ON} (A) ($V_{GS} = -6 V$)
Bilayer PoC_A $C_i =$ $12.25 nF \cdot cm^{-2}$	Linear $V_{DS} =$ $-0.1 V$	Forward	0.58 ± 0.03	-1.57 ± 0.08	311 ± 137	$3.24e11 \pm 1.76e11$	-404 ± 25	$7.66e-8 \pm 0.48e-8$
		Reverse	0.53 ± 0.03	-1.07 ± 0.11	691 ± 70	$8.11e11 \pm 0.91e11$		
	Saturation $V_{DS} =$ $-6 V$	Forward	0.54 ± 0.03	-1.28 ± 0.07	720 ± 86	$8.46e11 \pm 1.1e11$	-276 ± 29	$1.21e-7 \pm 0.19e-7$
		Reverse	0.48 ± 0.03	-0.92 ± 0.07	737 ± 78	$9.71e11 \pm 1.01e11$		

the one observed in the reference. Moreover, the overall yield off the foil was lower ($\approx 71\%$) which did not bode well for performance of the PoC_A foil. However, as the global quality of a batch of organic transistors could be heavily impacted by environmental conditions during the fabrication, the integration of the bilayer was not to be incriminated before further study.

As for the reference structure, Table 3.2 regroups the extracted typical transistor

2. TERPOLYMER INTEGRATION IN THE TRANSISTOR STRUCTURE

parameters for the viable devices (140/196) in the second quadrant of the PoC_A foil. The median extracted mobility for this bilayer structure ($\mu_{eff\ lin} \approx 0.55\ cm.V^{-1}.s^{-1}$) was noticeably lower than the one extracted from the reference which could be explained by a lesser interface quality. Not unlike the reference, a mismatch of subthreshold swing could be seen between the forward and reverse transfer curves. As there was no noticeable difference in the slope of the characteristic (Figure 3.10), this mismatch could again be attributed to the difference OFF current levels. consequently the highest value of SS (and thus N_{it}) should be the most relevant indicator for these structures. As such, it indicated that the PoC_A foil presented a lesser interface quality when compared to the reference, which might justify the degraded mobility. In theory, this degraded interface quality should not have been induced by the terpolymer material because of the low- κ buffer layer. As such, further study would be required to conclude on the matter.

Another noticeable phenomenon in the extracted parameters was the difference between forward and reverse extracted mobility. Since the gap between the two values was larger than their respective standard deviation, the difference appeared to be statistically significant. As it was not likely that the intrinsic mobility of the semiconductor would change with forward or reverse bias, the most probable explanation for this mismatch could be attributed to the extraction itself.

A possible origin for this phenomenon could be the RFE behaviour of the terpolymer. For the purpose of average capacitance extraction, we approximated the lens shaped polarization (“pointed” ellipse; Figure 3.13 a)) to a linear-like behaviour (Chapter 2). However, the actual variation of charge at the interface of the dielectric might not be completely linear. When considering the capacity to be equivalent to the small signal response of the charge on the dielectric interface at a given voltage (Equations (2.6), (2.7) and (2.12)), the differential capacitance could be calculated with[112, 113]:

$$C_i = \frac{d\sigma_s}{dV} \quad (3.1)$$

Were σ_s is the surface charge and V is the surface potential.

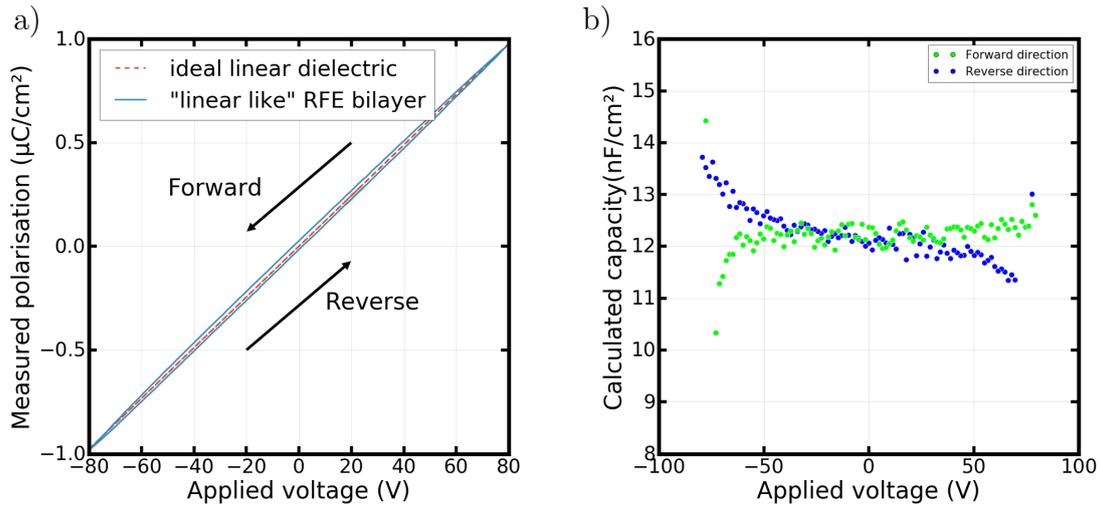


Figure 3.13: a) Polarization profile of the PoC_A bilayer and representation of an equivalent linear dielectric; b) differential capacitance calculated from the polarization data.

As we can see from Figure 3.13 b), the value of forward and reverse differential capacitance will change depending on the applied bias direction. In the case of p-type transistors, negative gate bias are required to reach the ON state, and as such the forward capacitance would be lower than the reverse one. Consequently, the forward mobility could be over estimated (and the reverse mobility could be underestimated) with the assumption of a constant C_i , which was coherent with our observations. However, since the precision of polarization measurement may not be accurate enough and since the calculation of differential capacitance implied some approximations (absence of leakage), we did not have the ability to strongly support this theory with quantitative data.

The final characterisation stage of PoC_A foil was the evaluation of the access to the channel. The transfer line measurement (Figure 3.14 a)) yielded a contact resistance of $R_C = 4.0 \cdot 10^3 \Omega \cdot \text{cm}$ at $V_{GS} = -3.3 \text{ V}$ and $V_{DS} = -0.1 \text{ V}$. This value accounted for approximately 10 % of the total channel resistance which was identical to the one seen in the reference structure. In a similar way, no ‘‘S-shape’’ could be observed in the output curve of the samples. Two devices were removed from Figure 3.14 b) as they presented high gate leakage.

3. OPTIMIZATION OF THE BILAYER DIELECTRIC

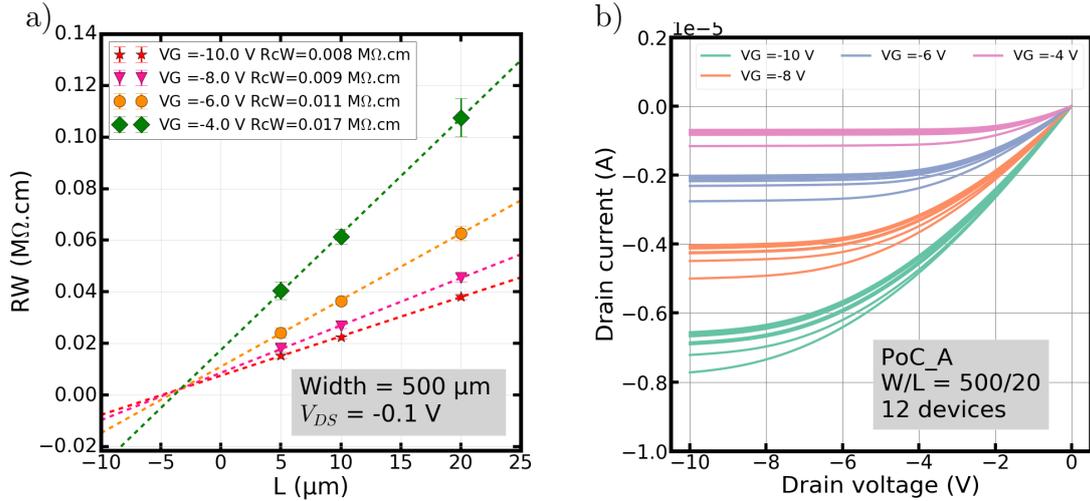


Figure 3.14: a) TLM for the PoC_A on the Q4 and b) example of output curves for twelve transistors with source drain layout equivalent to the devices in Q2.

Conclusion 3.2 (Integration of the P(VDF-TrFE-CTFE)) *We confirmed the that the direct integration of the terpolymer onto the semiconductor decreased the performance of our devices. We thus fabricated a transistor structure with a protective low- κ layer in between semiconductor and the high- κ material to prevent any degradation while increasing the gate capacitance. From this proof of concept, we were able to better understand the reduction of operating voltage, the evolution of hysteresis and the impact of the RFE bilayer on the extracted mobility. To further deepen our comprehension of this structure, we will modify the bilayer geometry while monitoring previously mentioned parameters.*

3.3. OPTIMIZATION OF THE BILAYER DIELECTRIC

3.3.1 Impact of low- κ layer thickness

The integration of the bilayer dielectric structure in our transistor had successfully reduced its operating voltage. However, some phenomena introduced by the bilayer dielectric in the transistor characteristic were yet to be fully understood. To further investigate the impact of the bilayer dielectric on the transistor, we have fabricated

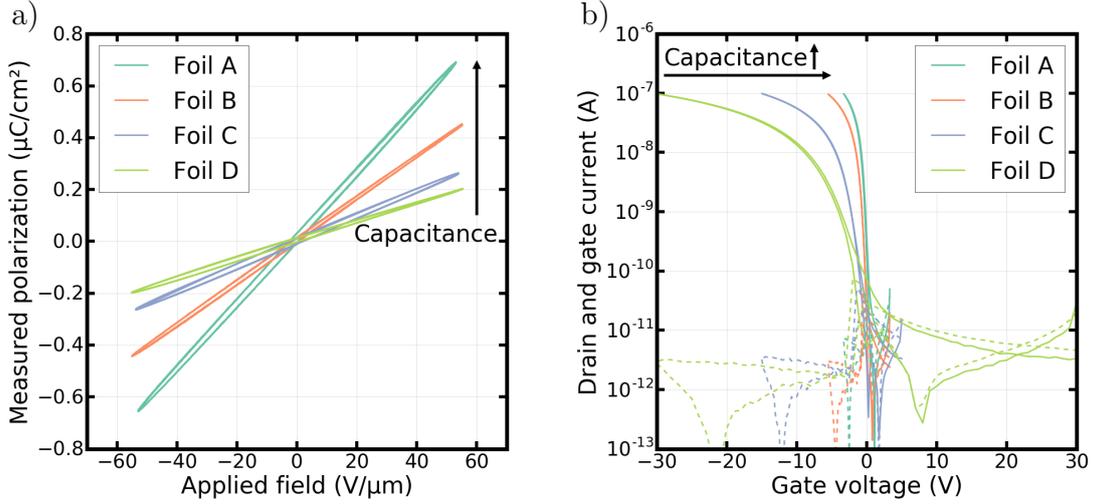


Figure 3.15: a) Polarization profile for each foils equivalent bilayer dielectric and b) transfer curves of the median transistor of each foils.

four foils of bilayer transistor with each an increasing low- κ thickness. The fabrication process and sub-layers geometry of each of these foils are identical to the bilayer dielectrics described in Table 2.1 (Chapter 2).

It should be noted that because of a high amount of leakage, no functioning device could be produced with a low- κ thickness below 60 nm, thus limiting our study in terms of ultra-low thicknesses.

We have reported the transistor's extractions essential to the discussion concerning the impact of geometry in Table 3.3. This condensed table mainly includes the extracted parameters of the linear transfer curve in forward direction for each foils. However, the full table of extraction and the associated transfer curves are available in Annex.

As expected, the median threshold voltage of each foil decreased with the increase of gate capacitance, which was itself linked to the reduction of the low- κ layer thickness. Considering the equation of threshold voltage discussed in Chapter 1 (Equation (1.12)), there were multiple factors that could influence the V_{th} value. However, since the gate metal, semiconductor and interface in the discussed samples were identical V_{FB} , Ψ_S , N_{it} and $Q_{acc\ th}$ should have remained relatively constant. This hypothesis was supported by the linear relationship between the threshold

3. OPTIMIZATION OF THE BILAYER DIELECTRIC

Table 3.3: Main extracted parameters for the foils A,B,C and D (median \pm standard deviation)

Sample	A	B	C	D
low- κ /high- κ (nm)	62 nm/613 nm	120 nm/619 nm	333 nm/604 nm	627 nm/611 nm
C_i (nF/cm ⁻²)	18.80 \pm 0.61	11.15 \pm 0.47	5.27 \pm 0.03	2.95 \pm 0.08
V_{th} (V)	-0.99 \pm 0.10	-1.56 \pm 0.07	-4.28 \pm 0.46	-8.06 \pm 0.59
μ_{eff} (cm.V ⁻¹ .s ⁻¹)	0.71 \pm 0.06	0.69 \pm 0.03	0.76 \pm 0.05	0.65 \pm 0.03
ΔV at $I_{DS} = 1$ nA (mV)	-420 \pm 45	-239 \pm 66	-331 \pm 76	-196 \pm 100
Q2 Yield (%)	94.4	90.8	92.5	86.6

voltage and the inverse of capacitance seen in Figure 3.16 a). From this observation we gathered that the terpolymer had no significant impact on the semiconductor's properties, regardless of the low- κ thickness.

Furthermore, we could observe that mobilities extracted from the different foils did not appear to be directly impacted by the bilayer structure. As their value remained the same range than the reference structure, we could conclude that the degraded mobility in PoC_A was probably caused by environmental factors during processing rather than by the introduction of the bilayer as the dielectric. The global yield of functional devices was not affected by the D320 layer thickness (if above 60 nm) and thus might only be impacted by external environmental factors during their fabrication.

Each foil presented a clockwise hysteresis (negative value) of approximately the same order of magnitude. There were no discernable patterns in the extracted values. In Figure 3.16 b) were represented the evolution of hysteresis with measurement time (five devices per foil). Contrary to the PoC_A (Figure 3.11 b)), the general trends observed in the bilayer foils did not exactly match the one displayed by the reference. Except for the B samples, the hysteresis values begun to shift towards the negative values (ie: increase of the clockwise hysteresis) to then shift to positives one (ie: reduction of clockwise hysteresis) which might have indicated the superposition of

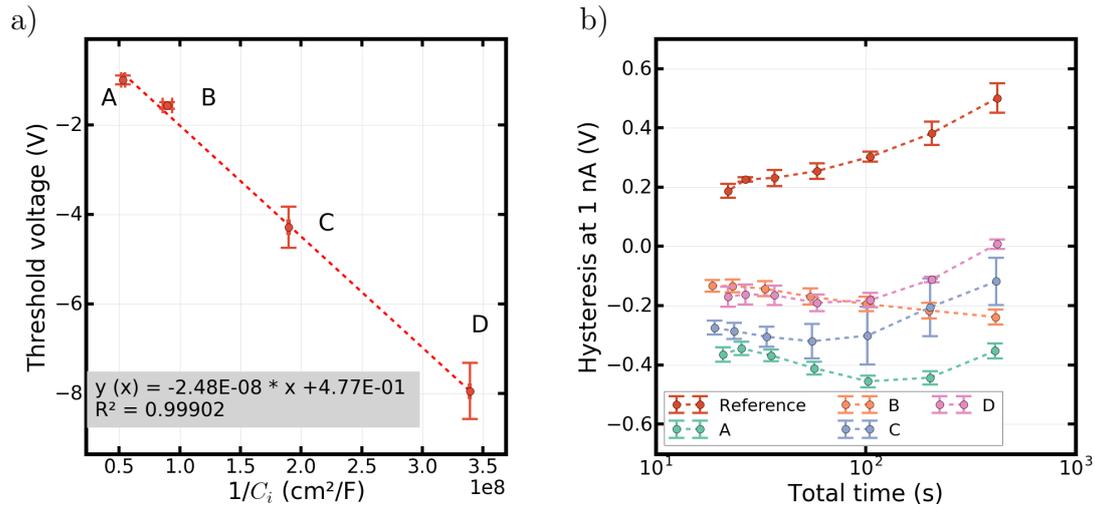


Figure 3.16: Polarization measurement and equivalent capacitance

two different behaviours. However, we could see that this behaviour was not shared by foil B, which hindered our understanding of this phenomenon.

Overall, the variation of geometry mainly impacted the capacitance of the bilayer dielectric thus modifying the threshold voltage of the transistor without any noticeable detrimental effects on the mobility and interface quality and variation of hysteresis. As such, the main path of optimization for this bilayer structure would be to minimize the low- κ and the global thickness of the bilayer to achieve the highest possible equivalent permittivity while maintaining the homogeneity to limit the leakage to a minimum.

3.3.2 Optimized bilayer

With a better understanding of the performance and limitations of the bilayer transistor, we were in measure to produce an improved bilayer dielectric structure to better fit our goals in terms of operating voltage. From the previous section we gathered that the key factors to take into account when producing a relaxor-ferroelectric based bilayer transistor were the thicknesses and permittivities of the two respective materials. With the low- κ layer thickness being limited by our processing capabilities (ie: increase of defects density at ultra-low thickness) and with the ratio

3. OPTIMIZATION OF THE BILAYER DIELECTRIC

the two materials impacting the polarization and equivalent permittivity of the bilayer structure, the degrees of freedom for the optimized bilayer dielectric were few.

In this section we will discuss two foils of transistors fabricated with the same process to gain insight on the sheet-to-sheet reproducibility of this optimized bilayer structure. These two batches of transistors will be further referred to as “OPT_A” and “OPT_B” for the sake off differentiation.

In order to maximize the capacitance of the dielectric layer while maintaining acceptable gate current levels, we chose to aim for a global dielectric thickness of approximately half a micron. The thin low- κ layer was spun at 4000 *rpm* from a 4 *w%* decane solution, reaching a thickness of approximately 58 *nm*. The subsequent terpolymer layer was spun at 1500 *rpm* from a 5 *w%* cyclopentanone solution producing a layer of approximately 435 *nm*.

In Figure 3.17 are represented the transfer curves (linear and saturation) of a randomly selected transistors from both OPT_A and OPT_B (linear scale available in Annex). Both devices achieved; at $V_{GS} = -3.3$ V; a I_{ON} similar to the one produced at $V_{GS} = -30$ V by the reference transistor (Figure 3.6). From this observation, we could conclude that the operating voltage for these optimized bilayers was lowered

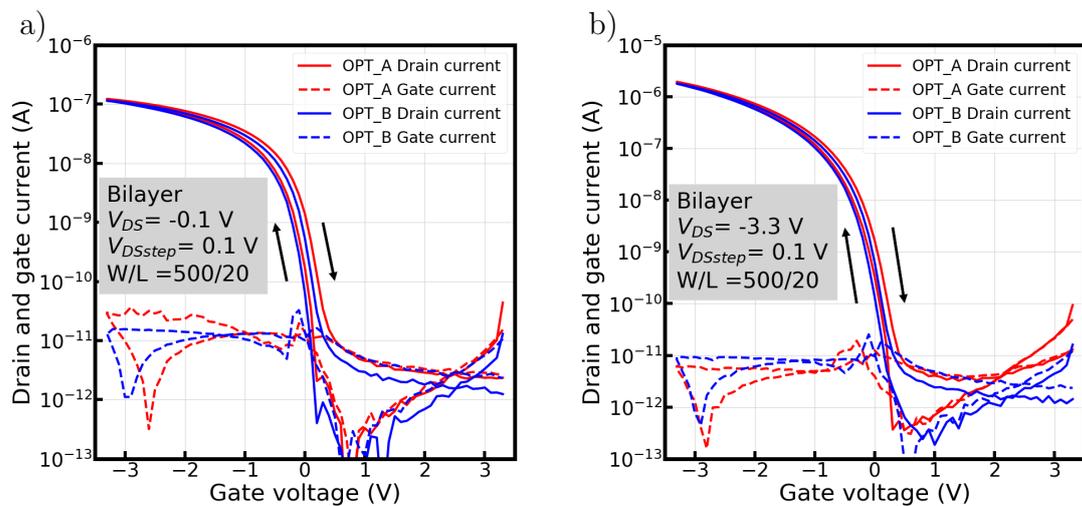


Figure 3.17: Comparison of transfer curves for OPT_A (red) and OPT_B (blue) in a) linear and b) saturation regime.

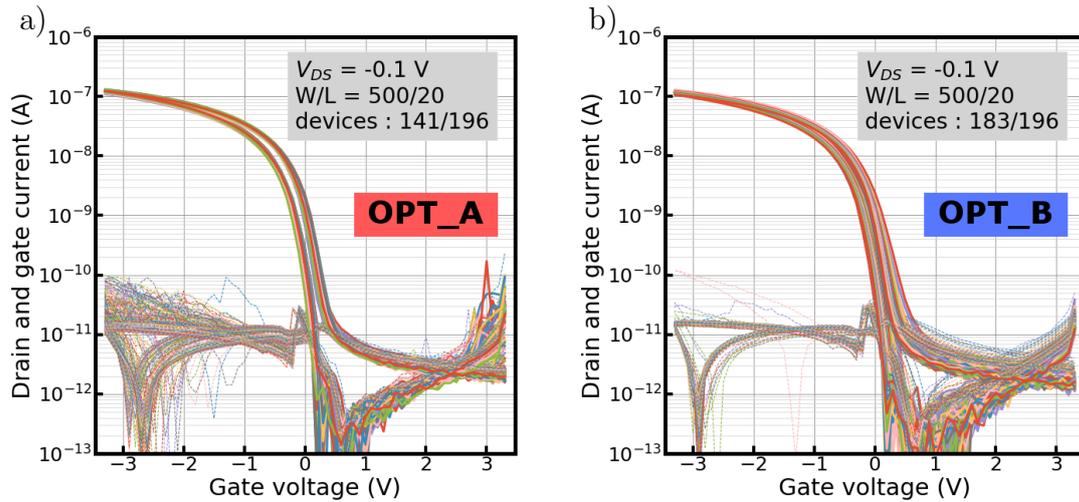


Figure 3.18: Linear regime transfer curves for all the functioning transistor of the second quadrant for a) OPT_A and b) OPT_B.

to approximately a ninth of reference's, while maintaining a relatively low gate leakage. Furthermore, both sample presented an hysteresis of similar amplitude to one another.

Transfer curves for the full amount of functional transistors (ie: with acceptable leakage current) from $Q2$ of both foils can be found in Figure 3.18. Both foils presented a relatively narrow current dispersion despite the presence of a higher than average leakage in the OPT_A foil. The yield of functioning transistors in OPT_A and OPT_B was respectively 72 % and 95 %, with leakage being the primary cause of malfunction like in the reference structure. We are confident that better processing capabilities should able to improve the overall yield of these structures.

Extractions of key parameters of both foils can be found in Table 3.4. The difference of approximately 0.3 nF.cm^{-2} ($> 2\%$) in the measured gate capacitance for the two device could be caused by a thickness difference in one of its two constitutive dielectric layers. This capacitance gap could be translated to a variation of less than 2 nm in the low- κ dielectric thickness or a less likely 20 nm variation in the terpolymer thickness.

From the median values of mobility, interface density, and ON current, we could infer that the intrinsic properties of the semiconductor were relatively similar to the

Table 3.4: Extracted parameters for the second quadrant of OPT_A and OPT_B foils (median \pm standard deviation).

Sample	Mode	Direction	$\mu_{eff} (cm^2 \cdot V^{-1} \cdot s^{-1})$	$V_{th} (mV)$	$SS (mV \cdot dec^{-1})$	$N_{it} (cm^{-2})$	ΔV at 1 nA (mV)	$I_{ON} (A)$
Bilayer OPT_A $C_i = 22.88 \text{ nF} \cdot cm^{-2}$	Linear $V_{DS} = -0.1 \text{ V}$	Forward	0.74 ± 0.04	-394 ± 36	108 ± 17	$1.16e^{11} \pm 0.40e^{11}$	-201 ± 19	$1.21e^{-7} \pm 0.09e^{-7}$
		Reverse	0.67 ± 0.04	9 ± 34	180 ± 8	$2.89e^{11} \pm 0.19e^{11}$		
	Saturation $V_{DS} = -3.3 \text{ V}$	Forward	0.73 ± 0.03	-264 ± 24	148 ± 52	$2.11e^{11} \pm 1.24e^{11}$	-143 ± 11	$1.9e^{-6} \pm 0.1e^{-6}$
		Reverse	0.63 ± 0.04	2 ± 30	186 ± 18	$3.04e^{11} \pm 0.43e^{11}$		
Bilayer OPT_B $C_i = 22.56 \text{ nF} \cdot cm^{-2}$	Linear $V_{DS} = -0.1 \text{ V}$	Forward	0.74 ± 0.04	-459 ± 72	108 ± 21	$1.14e^{11} \pm 0.50e^{11}$	-169 ± 19	$1.16e^{-7} \pm 0.03e^{-7}$
		Reverse	0.67 ± 0.04	-9 ± 39	172 ± 14	$2.65e^{11} \pm 0.35e^{11}$		
	Saturation $V_{DS} = -3.3 \text{ V}$	Forward	0.72 ± 0.02	-292 ± 22	148 ± 63	$2.10e^{11} \pm 1.51e^{11}$	-127 ± 9	$1.83e^{-6} \pm 0.06e^{-6}$
		Reverse	0.64 ± 0.02	-6 ± 27	182 ± 21	$2.91e^{11} \pm 0.50e^{11}$		

CHAPTER 3. INTEGRATION OF P(VDF-TRFE-CTFE) FOR LOW VOLTAGE SOLUTION PROCESSED ORGANIC THIN FILM TRANSISTORS

one observed in the reference (Table 3.1). However, the slight disparity between the forward and reverse mobility discussed previously in this chapter was also present in both samples. The global hysteresis for both foils of optimized transistors was in the range of 200 mV which translated to approximately 6 % of the maximal applied field, which half of the initial bilayer device (Table 3.2).

The generally accepted consensus in electronics is that the operating voltage of a transistor is achieved at approximately three times its threshold voltage. Considering this rule of thumb, our median devices could be considered in operating mode when $\|V_{GS}\| = 1.5 V$, even if the maximal standard deviation of the population was considered the potential operating voltage for this type of transistors was well below 3.3 V making them suitable for TTL (Transistor-Transistor logic) chips or even compatible with standard microelectronic chips.

Conclusion 3.3 (optimization) *By fabricating bilayer transistors with an increasing low- κ thickness, we were able to understand the link between transistor properties and the dielectric structure. Except for the threshold voltage and subthreshold swing, no other extracted parameters were significantly impacted by the variation in dielectric structure. With the improved understanding of this dielectric structure, we were able to fabricate two foils of optimized low-voltage transistors with relatively identical properties. These transistors were able to perform similarly to the reference device but at a fraction of its operating voltage.*

3.4. CHAPTER CONCLUSION

In this chapter we have reported the result of our study concerning the integration of a low- κ /high- κ bilayer dielectric into a transistor structure. In order to evaluate the impact of the bilayer on the performance of the transistor we have fabricated and characterized a reference device solely using the D320 (low- κ material) as insulating layer. This reference foil of transistors displayed high operating voltage ($\approx -30V$) and a mobility in the range of the expected values ($\mu_{eff} \approx 0.7 cm.V^{-1}.s^{-1}$). The

good device-to-device reproducibility of extracted parameters allowed for a strong comparison baseline for the rest of the study.

As the direct integration of the terpolymer in the transistor had proven to degrade the overall performance of the semiconductor, we produced a first proof of concept for a bilayer OTFT. The integration of a relatively thin layer of low- κ dielectric between the semiconductor and the high- κ relaxor-ferroelectric material prevented the drastic degradation of mobility while significantly reducing the threshold voltage of the device. However, we noticed that the extraction of mobility was compromised to some extent as the effective capacitance of a bilayer dielectric could present some bias dependent non-linearities of the second order.

By modifying the bilayer dielectric geometry, we concluded that the semiconductor's performance remained mostly unchanged regardless of the low- κ layer thickness. Meaning that the mobility and interface quality would be mostly affected by processing conditions. Moreover, the increased gate capacitance caused by the change in geometry induced a decrease in threshold voltage and thus operating voltage. This relationship between V_{th} and C_i closely matched the one expected in CMOS devices. However, no link could be drawn between the current hysteresis and the structure of the bilayer dielectric.

Finally, with an improved understanding of properties and limitations provided by the structural study of the bilayer dielectric, we were able to fabricate optimized low-voltage devices. These transistors could operate below 3.3 V with a tenth of the threshold voltage displayed by the reference low- κ structure, with an acceptable sheet-to-sheet reproducibility.



Electrical stability

The finality of our low-voltage transistor is to be part of an organic circuit or sensor and as such, it will be constantly exposed to electrical stimuli. This could gradually affect the performances of a given transistor[114]. Because of the plethora of materials and structures available for OTFTs, there are few in-depth studies that investigate the microscopic origins of these instabilities. In the first part of this chapter we will first evaluate the stress response of the low- κ reference to establish a base-line behaviour. Then we will compare the evolution of the optimized bilayer to said reference and evaluate the impact of the terpolymer on the electrical stability of the device. Finally, we will study the evolution of stress behaviour with temperature.

4.1. INTRODUCTION TO THE GATE BIAS STRESS

4.1.1 Electrical Protocol

The go-to method to simulate the impact of circuit operation on transistors is the Bias-Temperature Stress (BTS), where a constant bias is applied to the transistor's electrodes for a given period of time at a fixed temperature[115]. Electrical stress commonly focusses on two biases either the Gate Bias Stress (GBS) or the Drain Bias

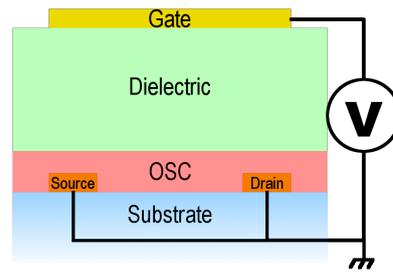


Figure 4.1: Electrical representation of the GBS on a transistor.

Stress (DBS)[116] (In specific cases both biases are applied at the same time[117]). These two stresses respectively give informations on phenomenon occurring in the dielectric and/or at the interface for the GBS; in the bulk of the semiconductor and at the injection between source/drain and the OSC for the DBS. As this present work mainly focusses on the impact of dielectrics on transistor properties we focussed on a GBS protocol.

There are two main method to monitor the evolution of the transistor with the GBS. A fast acquisition of a single point in the I_{ON} region that would not disrupt the stress for more than a few milliseconds, from this current value will be extrapolated the evolution of V_{th} . However, this methodology assumes that only the threshold voltage would be impacted and thus would not allow for the monitoring the subthreshold region. Or a slower acquisition of the full transfer curve that will provide all needed information but will stop the stress for a longer period of time rendering the short time stresses less reliable. Because the hysteretic impact of the relaxor-ferroelectric material would better observed in the sub-threshold region of the curve we opted for the full transfer curve method.

The GBS protocol used in the rest of this chapter will consist in the application of a selected bias to the gate ($V_{GS\ str}$) for 10^4 s while the source and drain electrodes are electrically grounded (Figure 4.1). Full transfer curves in linear regime are periodically obtained with a fast integration time (full curves acquisition was approximately 6 s) in order to limit the disruption of the stress to a minimum.

4.1.2 Impact of the stress on the transfer curves

In order to be able to adequately discuss the GBS impact on the transistor, we needed to be sure that the observed phenomena were solely induced by the GBS and not by the large quantity of transfer curves performed during the stress. In order to do so, we conducted a GBS where the $V_{GS\ str}$ was set to 0 V for both the reference and the OPT_A foils.

The full amount of transfer curves measured during these dummy tests (ie: 22 curves over 3 h) are reported in Figure 4.2 where it can be seen that no noticeable change occurred over time. From this observation we could confidently assume that the acquisition had no significant impact by itself on either transistor structures.

In the rest of this chapter, we focussed on Negative Gate Bias Stress (NGBS) as it was the most coherent measure with p-type transistors since their operating regime would only be achieved with negative voltage. Positive Gate Bias Stress was however not investigated.

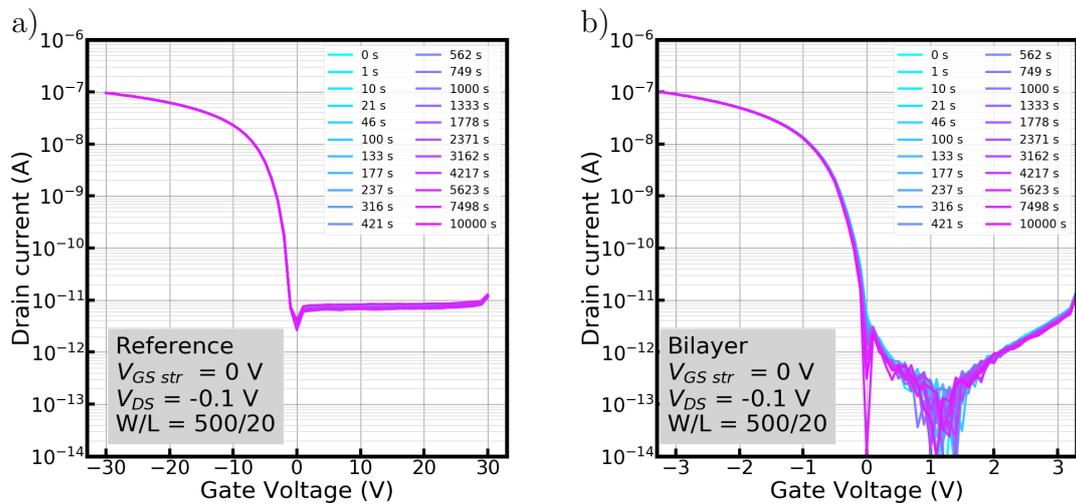


Figure 4.2: Gate bias stress measurement at $V_{GS\ str} = 0\text{ V}$; log-scale transfer curves for a) the low- κ structure and b) the optimized bilayer structure.

Conclusion 4.1 (Gate Bias Stress protocol) *BTS is a tool commonly used to evaluate the electrical reliability of organics transistors. We chose to perform Gate Bias Stress to investigate the impact of different dielectrics on the electrical stability of the transistor. The selected measurement protocol consist of apply a set gate bias ($V_{GS\ str}$) for 10^4 s and regularly monitor the evolution of the transistor with the help of full transfer curve acquisition. The acquisition of these transfer curves during the stress had no significant impact on the transistor characteristic.*

4.2. REFERENCE TRANSISTOR UNDER NEGATIVE GATE BIAS STRESS

4.2.1 Impact of stress on Transfer curves

To first evaluate the reference transistor, we applied a Negative Gate Bias Stress (NGBS) equivalent to its operating voltage ($V_{GS\ str} = -30V$). The NGBS response of the transistor was a global shift of the transfer curve towards the negative gate voltage values (Figure 4.3 a)). This shift could be translated to a decrease of the current measured at $V_{GS\ max}$. At the three hour mark, the I_{ON} displayed an average 6.7 % loss (average of 3 different devices). When plotted in logarithmic scale no large impact on the sub-threshold slope could be seen (Figure 4.3 b)). A following extraction of the various transistor's key parameters throughout the stress would allow for a better evaluation of its impact on the reference structure.

4.2.2 TFT Parameter Extractions

In an effort to be as rigorous as possible in our conclusion and limit the human factor, each GBS was conducted on at least three devices and extractions where performed using an automated software.

The extracted mobility remained constant throughout the NGBS (Figure 4.4 a))

2. REFERENCE TRANSISTOR UNDER NEGATIVE GATE BIAS STRESS

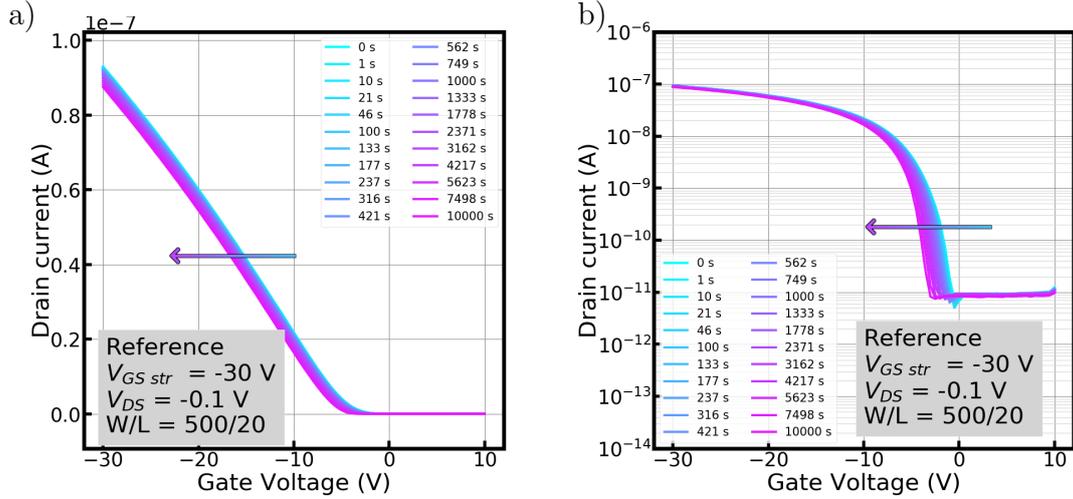


Figure 4.3: Reference Structure - Negative Gate Bias Stress measurement at ($V_{GS\ str} = -30\text{V}$) in a) linear and b) logarithmic scales.

thus indicating that the conduction in the channel was not degraded by the creation of a significant quantity of interface traps in the semiconductor. The evolution of the subthreshold swing with the stress would allow for a higher precision in regarding the quantity of interface states, however as can be seen in Figure 4.4 b) the extraction of this parameter was proven difficult. In order to limit the disruption caused to the stress by the acquisition of transfer curves, the measurement duration and the definition of the gate sweep were minimized. As a result, this global noise in the extracted was induced by the lack of measurement points ($V_{GS\ step} = 0.5\text{ V}$) in the subthreshold region of the transfer curve. Never the less, no global trend was observable either in Figure 4.4 b) or Figure 4.3 b) thus supporting the hypothesis concerning the absence of any significant interface trap formation during the stress. The shift in the transfer curves would thus mainly be caused by a variation of threshold voltage (ΔV_{th}) in the same direction as the applied bias.

$$\Delta V_{th}(t) = V_{th}(t) - V_{th}(0) \quad (4.1)$$

The variation of ΔV_{th} across the three measured device was relatively low when compared to the total shift induced by the NGBS (Figure 4.4 c)). This type of degradation would generally be attributed to the creation of new electronic states at the interface[118] or to the trapping of charge carrier into the dielectric itself[114, 117, 119]. In the literature, this type of shift would often be compared to

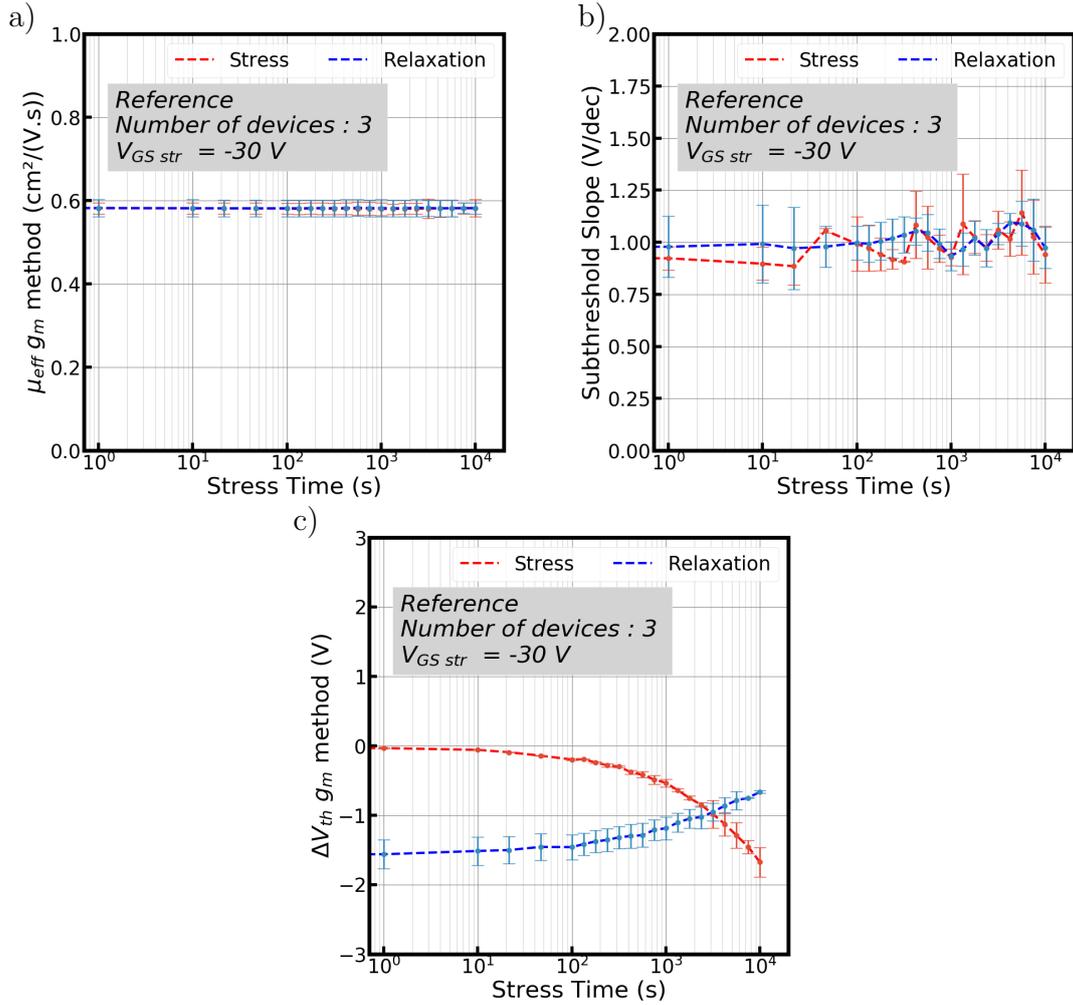


Figure 4.4: Evolution of the average a) mobility b) subthreshold swing and c) the threshold voltage shift.

a model based on a multi-trap release behaviour borrowed from amorphous silicon TFT [120, 121]. Furthermore, an equivalent relaxation duration (3 h) relaxation was not sufficient to return to the initial threshold voltage value, indicating that “de-trapping” did not present the same time constant as the stress.

4.2.3 Impact of bias amplitude on the reference

Other stress measurement were then carried out a various NGBS amplitude in order to fully characterise the response of the reference structure. When $V_{GS\ str} > V_{th}$, no dependence could be seen in the resulting ΔV_{th} (Figure 4.5 a)). Furthermore, the

2. REFERENCE TRANSISTOR UNDER NEGATIVE GATE BIAS STRESS

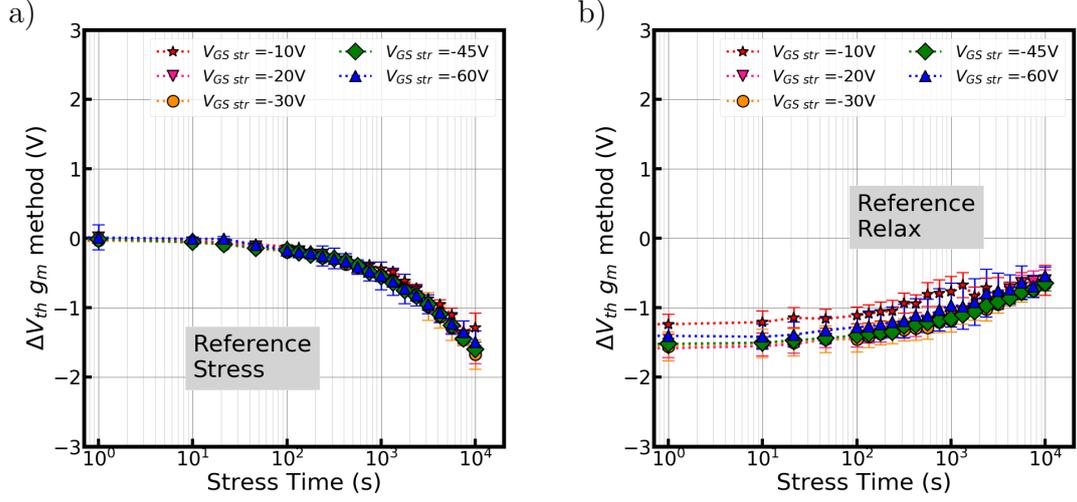


Figure 4.5: Threshold voltage shift through stress and relaxation at different .

relaxation ΔV_{th} followed the same trend for each $V_{GS\ str}$ and reached an identical value after three hours of relaxation (Figure 4.5 b)).

The multi-trap release model prior discussed is mathematically described as stretched exponential (Equation (4.2)):

$$\Delta V_{th}(t) = V_0 \left\{ 1 - \exp \left[- \left(\frac{t}{\tau} \right)^\beta \right] \right\} \quad (4.2)$$

$$\tau = \tau_0 \exp \left(\frac{E_a}{kT} \right) \quad (4.3)$$

$$V_0 = V_{GS\ str} - V_{th}(t = 0) \quad (4.4)$$

Where V_0 is the effective voltage drop across the insulator (Equation (4.4)), τ is the characteristic trapping time (Equation (4.3)) and β is the stretched-exponential exponent. However, in our case, the ΔV_{th} was not impacted by a variation in the amplitude of applied bias which would contradict the premises of the model. As a result the V_0 prefactor in the fit parameters presented in Figure 4.6 a) did not hold true physical meaning and is only given for benchmarking purpose. We also conducted a power law fit (Equation (4.5)) as it is a common methodology in classic microelectronic.

$$\Delta V_{th}(t) = \alpha t^\beta \quad (4.5)$$

The β parameter obtained with the power law fit was close to 0.5, meaning that these threshold voltage shift displayed a square root dependency regarding time

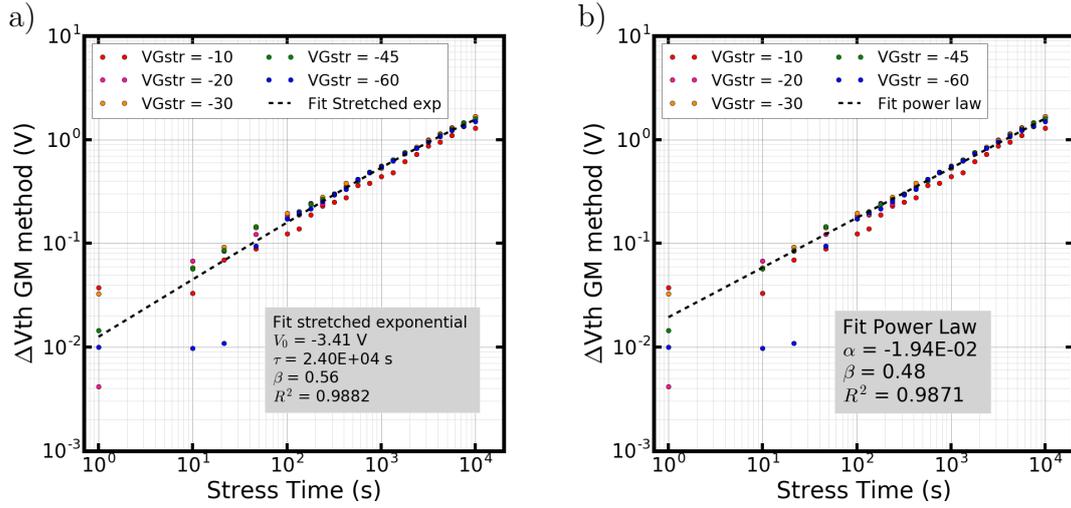


Figure 4.6: Average ΔV_{th} shift for each $V_{GS\ str}$ along with a) a stretched exponential fit and b) a power-law fit.

(Figure 4.6 b)). Interestingly, the solution for Fick's second law of diffusion, solved for the case in the hypothesis of a constant concentration of holes (ie: accumulated channel interface); also displays a square root of time dependency[122]. However, in the case of diffusion, the shift should be proportional to the quantity of charge carrier at the interface and by extension to the applied gate voltage.

As it was not the main focus of our work to describe phenomenon in the reference structure but rather to understand the impact of the relaxor-ferroelectric material we did not investigate further on the matter.

Conclusion 4.2 (Reference structure under NGBS) *When submitted to a NGBS protocol of any amplitude above its threshold voltage, the reference structure transistors undergoes a V_{th} shift to the negative values. As the mobility and subthreshold swing of the transistors are not significantly impacted by the stress, this shift appeared to be induced by carrier trapping from the semiconductor into the dielectric. To the best of our knowledge, this bias non-dependency have not been discussed in the literature.*

4.3. BILAYER TRANSISTOR UNDER NEGATIVE GATE BIAS STRESS

4.3.1 Bilayer: impact of stress on transfer curve and extractions

At first, the application of a NGBS on the optimized bilayer ($V_{GS\ str} = -3.3\ V$) appeared to produce an effect similar to the reference as the transfer curves shifted towards the negative values. However, the average current current loss observed after three hours was only 3.2% of the initial output current at $V_{GS} = -3.3\ V$ which was approximately half of the drop experienced by the reference transistor.

This disparity could be explained by the difference in the extracted ΔV_{th} evolution during the stress (Figure 4.7 b)). At short stress times ($t < 4.10^3\ s$), the curve first shifted towards the positive value of V_{th} to then gradually shift towards the negative values at longer times. This behaviour appeared to be the superposition of two opposite trends with different time dependency. To ease comprehension, this trend will be further referred to as “turn-around” in the rest of this chapter as the shift starts towards the positive gate voltage to then turn to the negative values.

Similarly to the reference structure, no significant trend was observable in the extracted mobility throughout the GBS (Figure 4.7 c)). This indicated that this turn-around did not find its origin either in the channel or in the bulk of the semiconductor.

4.3.2 Bilayer: impact of bias amplitude

In a similar fashion to the reference, we conducted NGBS with increasing bias on the bilayer transistor. Contrary to the low- κ transistor, the ΔV_{th} was significantly impacted by the $V_{GS\ str}$ variation (Figure 4.8 a)). At low gate bias, ΔV_{th} followed a trend similar to the one observed in the reference, with no significant turn-around. However, when the bias was gradually increased, the early shift to the positive voltage values was more and more present until the negative shift became barely noticeable

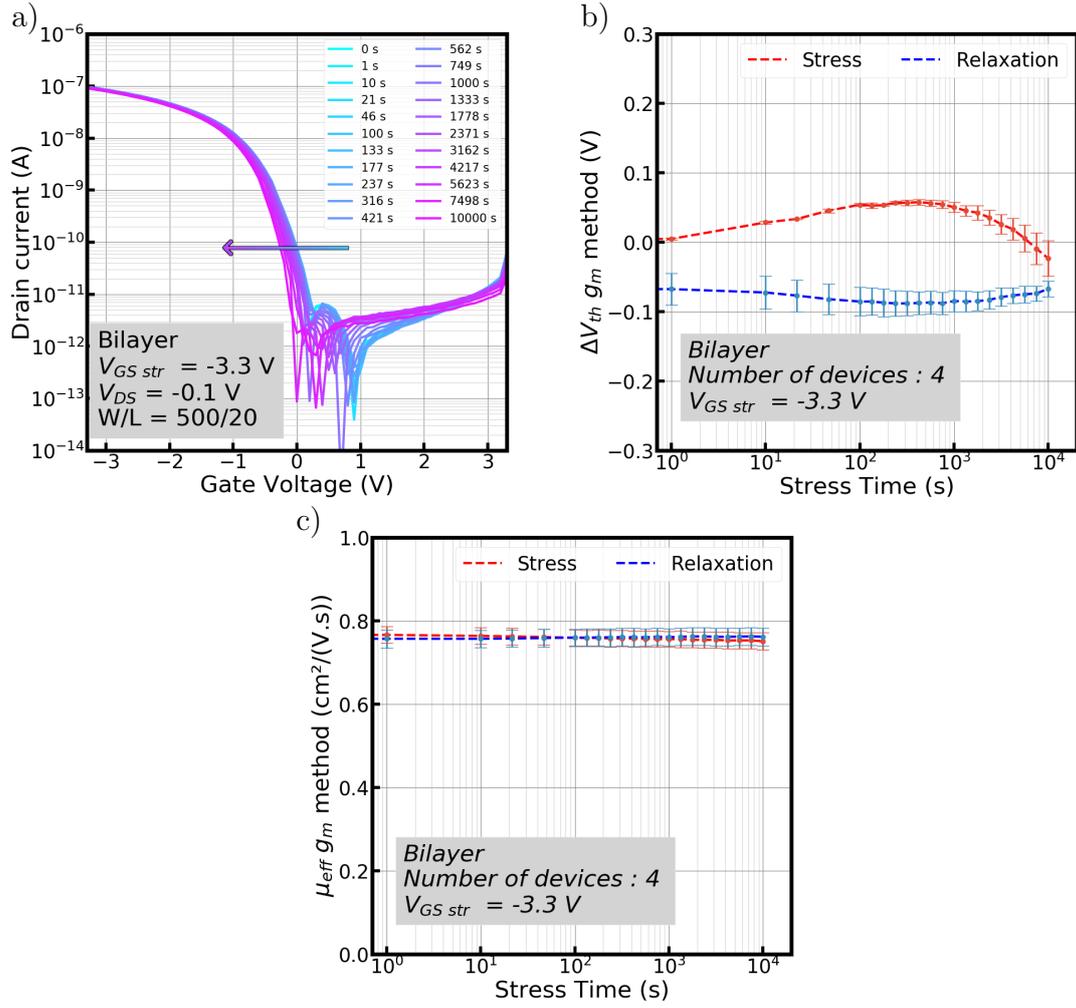


Figure 4.7: a) Example of bilayer's transfer curve evolution through stress ($V_{GS\ str} = -3.3$ V); average evolution of b) threshold voltage and c) mobility throughout the NGBS.

at $V_{GS\ str} = -6$ V.

When in relaxation, the positive component of the turn-around decreased relatively quickly to then reach an identical negative ΔV_{th} for each amplitude, thus indicating that the negative component of the turn-around could be bias independent. Both of these observations support the hypothesis that the turn-around could originate from the superposition of two physical phenomena with different times constants. A fast positive shift potentially introduced by the terpolymer and a slow negative shift introduced by the low- κ /semiconductor interface.

3. BILAYER TRANSISTOR UNDER NEGATIVE GATE BIAS STRESS

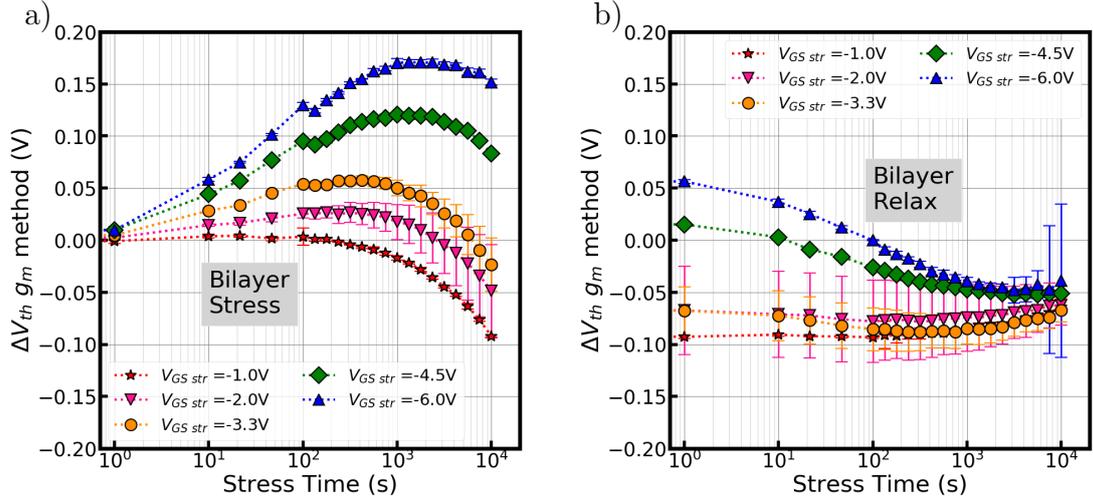


Figure 4.8: Bilayer structure threshold voltage shift at various gate bias through a) stress and b) relaxation (at least three device per curve).

4.3.3 Comparison of the two structures

Comparing the two transistor structures side by side was not a straight forward process. Since the average value for the V_{th} and the amplitude of the shift was not in the same order of magnitude, plotting them on the same scale could hide most of the information regarding the bilayer[56] (Figure 4.9 a)). As the main difference between these two structures arise from the C_i , a simple normalization of the the ΔV_{th} with Equation (4.6) would translate this relative voltage shift into a relative density of charge variation at the interface (ΔN_{ot}), with q representing the elementary charge.

$$\Delta N_{ot} = \frac{C_i}{q} \Delta V_{th} \quad (4.6)$$

Despite the presence of a similar trend, the relative charge carrier variation observed in the bilayer at low gate bias ($V_{GS\ str} = -1V$) did not exactly match the one encountered in the reference (Figure 4.9 b)). This difference hinted that the turn-around remained present even with extremely weak electrical solicitations.

This turn-around behaviour have been previously reported in the literature [56, 123–126] and have been attributed to various causes depending on the studied OTFT structure or dielectric. In our structure, three potential sources could be considered :

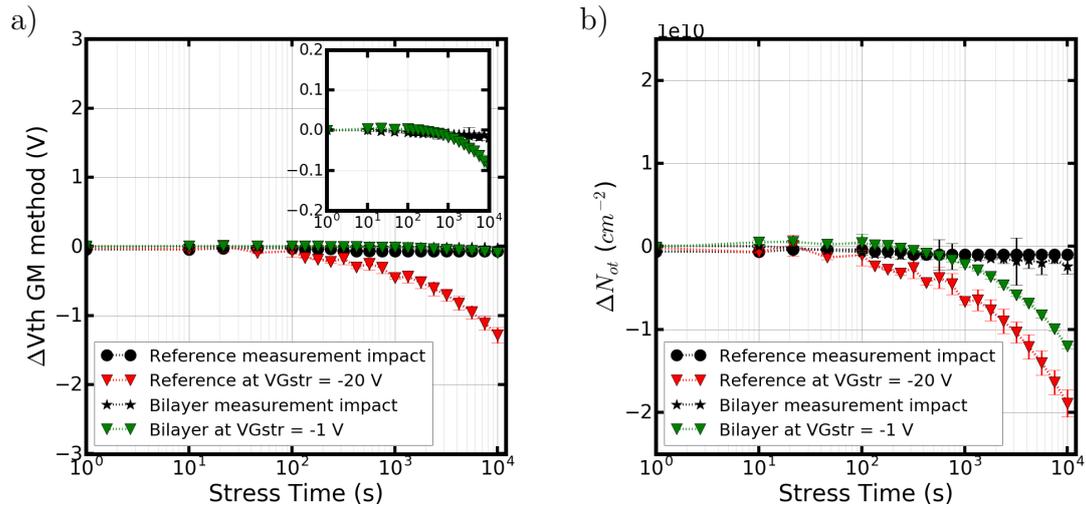


Figure 4.9: a) Average threshold voltage shift for the two structure (inset : zoom on the y axis) and b) the relative density of charge variation ΔN_{ot}

- Trapping of negative charge from the gate electrode into the dielectric.
- Latency in the dipole alignment.
- Drifting of ions present in the dielectric (generally attributed to water molecules in the dielectric).

Each effect could be compatible with a positive shift in the threshold voltage due to the increase of negative potential with respect to the channel. However, further investigation remains necessary to precisely pinpoint the origin of the turn-around encountered in our bilayer device. A possibility to identify the phenomenon causing the bias-dependent positive shift, would be to monitor the evolution of this turn-around with temperature. As each of these phenomena should present a different relation to a variation of temperature (i.e.: acceleration for ions and T_C for dipoles), the change in the NGBS could allow for a clearer distinction.

Conclusion 4.3 (Bilayer NGBS) *When submitted to a negative gate bias stress, the bilayer structure presented a bias dependent V_{th} shift to the positive voltage values that superimposed on the negative shift observed in the reference structure. A study of the impact of temperature on the NGBS response would allow for a better understanding of this behaviour.*

4.4. IMPACT OF TEMPERATURE

4.4.1 Bilayer dielectric evolution with temperature

As the low- κ and high- κ characterization in temperature have both been performed in Chapter 2, only the optimized bilayer structure remain to be studied. We will first study the impact of temperature on the stand-alone bilayer dielectric (MIM capacitor structure), to then focus on the transistor's transfer curves and finally evaluate its impact on the NGBS response.

The evolution of capacitance with temperature was a critical factor to monitor as most our key parameters extraction rely on C_i for an accurate extraction (ie: μ_{eff} , N_{it} , ΔN_{ot}). As a quick overview of Chapter 2, we reported that the low- κ capacitance value presented a linear decrease with temperature and that the terpolymer displayed a behaviour consistent with a Curie temperature (T_C) similar to the one observed in ferroelectric materials.

In the case if the optimized bilayer dielectric ($X \approx 90\%$), the capacitance evolution with temperature presented a peak similar to the one observed in the terpolymer (Figure 2.23). Depending on the measurement frequency, the peak temperature ranged from approximately 35 °C to 55 °C. However, because of the low- κ the T_C related peaks are less defined and the transition appeared to be broader than in the pristine terpolymer.

As discussed for the terpolymer, the polarization response of the bilayer was

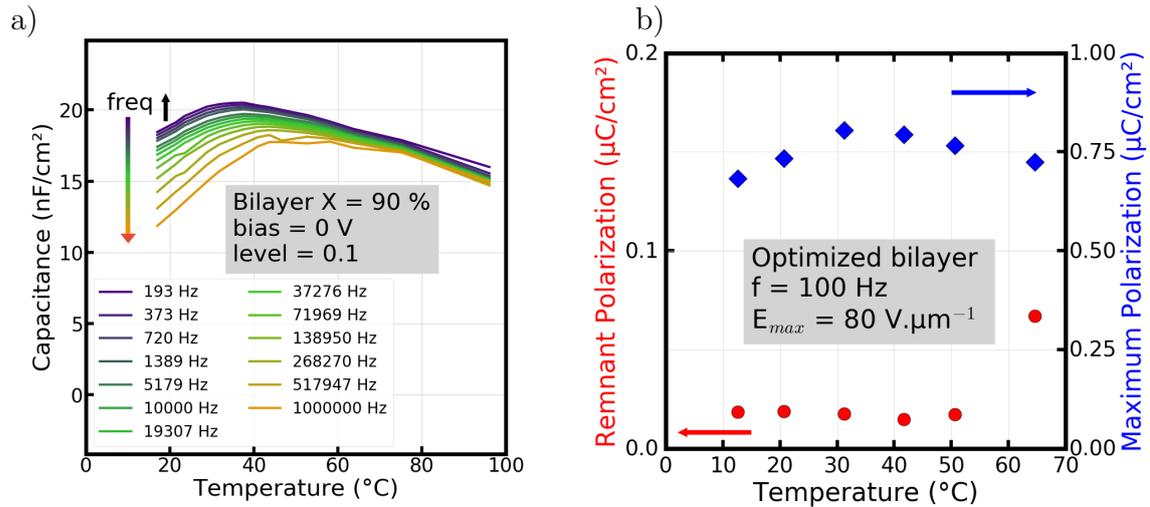


Figure 4.10: a) Evolution of the optimized bilayer's capacitance at different frequency and (bias = 0 V) b) extraction of maximum polarization and remnant polarization with temperature for the optimized bilayer ($f = 100 \text{ Hz}$ and $E_{max} \approx 80 \text{ V} \cdot \mu\text{m}^{-1}$).

directly linked to its measured capacitance. Consequently, a peak of maximal polarization was noticeable at approximately $33 \text{ }^\circ\text{C}$ which would be coherent with the supposed Curie transition. However, the expected drop in remnant polarization (ie: hysteresis) could not be observed due to the activation of conduction with temperature.

As highlighted previously, polarization measurements could differentiate the conduction current from an actual polarization current. As such, monitoring evolution of RFE hysteresis at high temperature was proven to be relatively difficult. However, as the conduction in the transistor channel is only affected by the bound charge in the dielectric (Equation (1.1)), a small variation in leakage should not impact on the current hysteresis. As a result, the transistor structure should be a good tool to monitor the evolution of the RFE behaviour.

4.4.2 Evolution of the transistor characteristic with temperature

Both transistor structures were measured from ambient temperature to just above $60 \text{ }^\circ\text{C}$. However, the increase in temperature also induced dilatation in the measurement setup and thus required a constant SMU probe repositioning. As such the

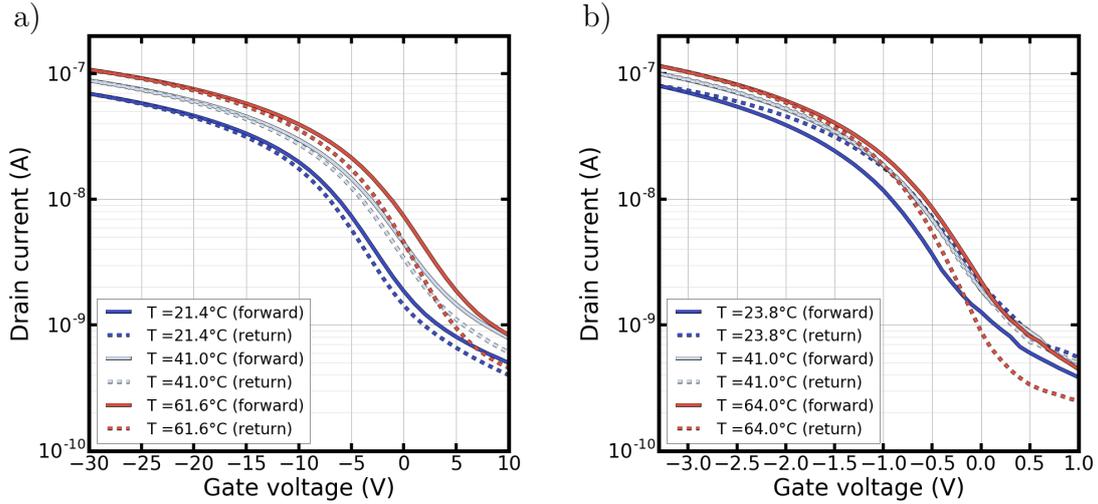


Figure 4.11: Transfer characteristic measured at different temperatures ($V_D = -1\text{ V}$) for a) the reference transistor and b) the bilayer structure.

acquisition of transfer curves with temperature had to be performed under illumination which increased the OFF current and the reference's anticlockwise hysteresis as explained in Chapter 3. For the sake of clarity, Figure 4.11 only displays the transfer curves for three key temperatures, (more temperatures can be found in Annex).

In the case of the low- κ dielectric (Figure 4.11 a)), the rise in temperature induced an increase in I_{ON} which did not correspond to the evolution of the low- κ capacitance measured in Chapter 2 (Figure 2.23 a)). As the C_i should decrease with temperature, the only possible explanation for this improved current would be an activation of mobility. Furthermore, we could see that the anticlockwise hysteresis present at low temperature was enlarged at high temperature which was coherent with an acceleration of trapping dynamic.

In the bilayer structure (Figure 4.11 b)), the ON current also increased with temperature. However, contrary to the reference, the bilayer displayed a clockwise hysteresis consistent with the RFE behaviour at ambient temperature. When the temperature was increased to approximately 40°C , the hysteresis almost disappeared. Finally, when temperature was then further increased close 60°C the hysteretic behaviour became anti-clockwise and similar to the one observed in the reference.

This change in the bilayer's hysteresis direction and the similarity between the

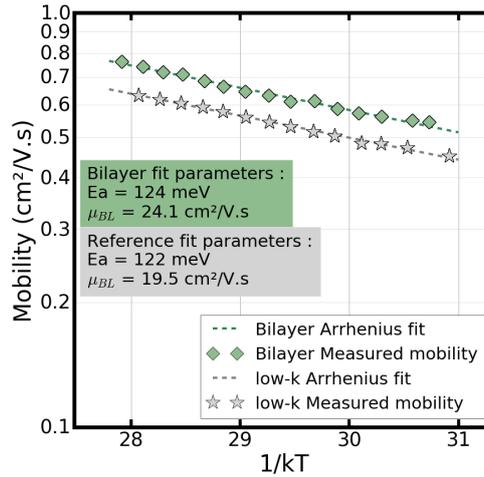


Figure 4.12: Evolution of mobility for reference and the bilayer in an Arrhenius plot.

final current hysteresis in both samples indicated that RFE behaviour introduced by the terpolymer disappeared at high temperature. One might argue that the increase of trapping at operating voltage with higher temperature could overcome the hysteresis introduced by the bilayer, however the similarities in term of width of the hysteresis (relative to their respective maximal voltage) for both structure at 60 °C tend to disprove this hypothesis.

Using the linear regime equations for the transistor in Chapter 1 and the temperature/capacitance measurements, we were able to extract μ_{eff} at various temperature for both structures (Figure 4.12 a)). A simple Arrhenius law was used to fit the evolution of mobility with temperature in order to evaluate its activation energy for both devices:

$$\mu_{eff} = \mu_{BL} \exp\left(-\frac{E_a}{k_b T}\right) \quad (4.7)$$

This temperature/mobility relationship was consistent with a multi-trap and release conduction mechanism in the semiconductor[127]. Such behaviour have been observed in an existing study based on OTFT using the same polymeric semiconductor[128]. The fitted parameters μ_{BL} (band-like mobility) and E_a (traps activation energy) were in the same order of magnitude than the one reported in the literature, which places the effective width of localized trap states close to 120 meV and the band-like mobility around 18 $cm^2/V.s$ which was similar to monocrystalline pentacene[129].

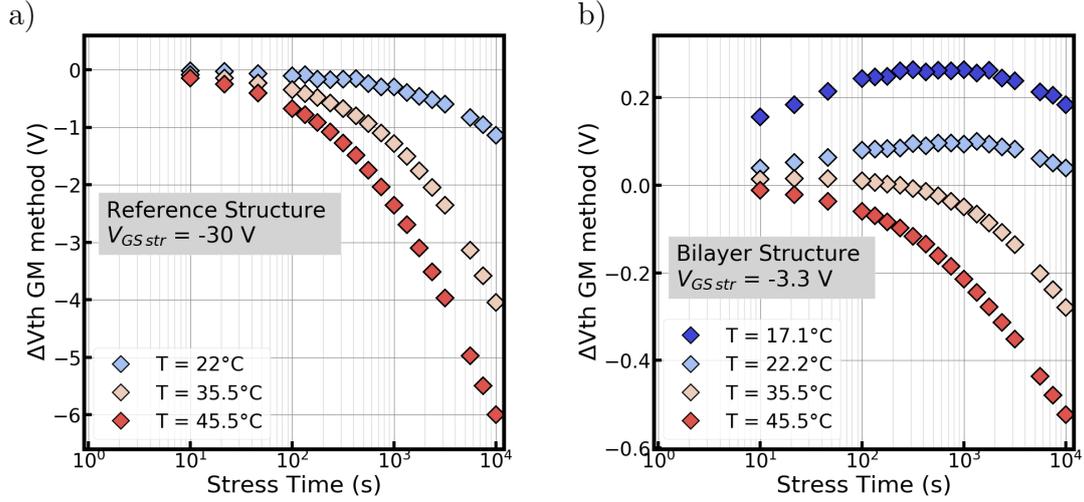


Figure 4.13: Threshold voltage shift through GBS measurement at different temperatures for a) the reference structure ($V_{GS_{str}} = -30$ V) and b) the bilayer structure ($V_{GS_{str}} = -3.3$ V).

4.4.3 Impact on turn-around phenomenon

The acquisition of the OTFTs characteristics in temperature allowed for a better understanding of the relaxor-ferroelectric response in the bilayer structure. To strengthen this study, we conducted NGBS measurement at key temperature points: ambient ($T < T_C$), mid-transition ($T \approx T_C$) and above transition ($T > T_C$).

In the reference structure, the increase in temperature appeared to accelerate the negative threshold shift. So much so, that when the stress was conducted at 45°C the final ΔV_{th} was five times larger than at ambient temperature. However, the general shape of the curve was not significantly impacted (Figure 4.13 a)).

In the case of the bilayer transistor, the positive shift responsible for the turn around appeared to be maximized at low temperature (17°C) and progressively disappeared when the temperature was increased. No turn-around could be observed above the terpolymer's T_C (45°C) thus producing a monotonic negative shift similar to the reference transistor.

In order to adequately compare the two structures, Equation (4.6) was used to convert the each threshold voltage shift into a relative charge carrier density at the

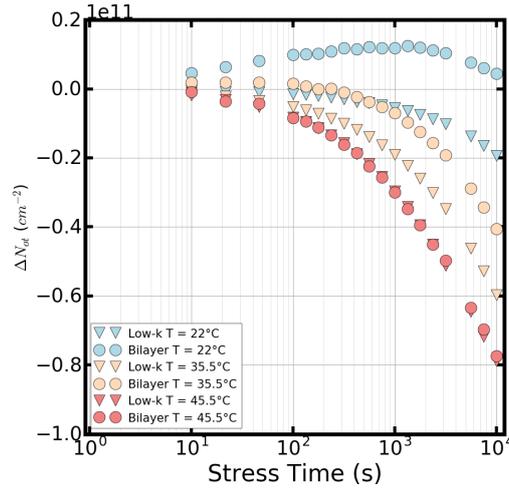


Figure 4.14: Relative charger carrier shift variation at different temperature for the low- κ and the bilayer.

interface (Figure 4.14). Here, triangular markers represent the ΔV_{th} in the low- κ structure ($V_{GS\ str} = -30\ V$) and the circle markers represent the shift in the bilayer ($V_{GS\ str} = -3.3\ V$). At ambient temperature, these structures displayed two distinct behaviours: a monotonic shift for the reference and a turn-around for the bilayer. When temperature was increased to $35\ ^\circ C$, the ΔN_{ot} curves for both devices were accelerated towards the negatives values but the final gap between the two curve remained relatively constant ($\approx 2e^{10}\ cm^{-2}$). Finally, when the temperature was further increased up to the terpolymer T_C ($45\ ^\circ C$), both curves superimposed one another and reached an identical final ΔN_{ot} .

Earlier in this chapter, we demonstrated that the negative shift observed in the reference structure was bias independent. With the evolution of ΔN_{ot} in temperature we observed an identical trend in both device when stressed at $45\ ^\circ C$. As such, if we assume that the phenomenon observed in the reference was also responsible for the negative component of the turn-around in the bilayer, it should also be independent from the applied bias. All this observation combined lead to believe that :

H1 : The turn-around phenomenon is the superposition of two behaviours, a negative shift introduced at the low- κ /OSC similar to the one observed in the reference and a positive shift introduced by the high- κ terpolymer component of the

bilayer dielectric.

H2 : The RFE behaviour; or more generally the dipolar interaction in the terpolymer; is responsible of the positive shift component of the turn-around observed in the bilayer as it is no longer existing above the material's T_C .

Conclusion 4.4 (NGBS in temperature) *The temperature plays a critical role in the performances of the transistors, especially with the bilayer dielectric which displays a T_C at approximately 35 °C. When measured above this critical temperature, the bilayer transistor displayed a behaviour identical to the reference structure while maintaining low-voltage operation. Despite the difference in dielectric materials both structures displayed a similar mobility/temperature relationship. This peculiar evolution in temperature was also observed in the NGBS response of the bilayer transistor where the turn-around effect observed at ambient temperature disappeared when above the T_C .*

4.5. CHAPTER CONCLUSION

In this chapter, we investigated the impact of electrical stress on our two main transistor structures by submitting these devices to a negative gate bias stress. This measure consisted in a set gate bias ($V_{GS\ str}$) applied for approximately three hours ($10^4\ s$) while monitoring the evolution of the transistor's parameters via logarithmically time spaced transfer curves.

The NGBS was found to have no significant impact on either the mobility or the subthreshold swing. However, in the reference transistor, a shift of the transfer curve towards the negative gate voltage values was observed. This shift was effectively introduced by an alteration of the threshold voltage during the NGBS. This negative ΔV_{th} was found to be extremely consistent from one transistor to another and to be bias dependent. To the best of our knowledge this sort of behaviour has not been reported in the literature.

The bilayer's stress response was similar to the reference in terms of mobility and subthreshold swing stability. However, a significant difference of threshold voltage shift was present. At short stress times, we could observe a gate bias dependent shift to the positive gate voltage values which then returned to a negative shift similar to the one observed in the reference. The superposition of these two shifts was thus referred to as turn-around. Reports from the literature demonstrated that this type of positive shift could be generated by an array of different phenomenon.

In order to identify the specific origins of this turn-around behaviour, we monitored its evolution with temperature. By conducting NGBS measurement at various key temperature points, we could notice the reduction of the positive shift in the bilayer structure stress response. When above the terpolymer's Curie temperature, the positive shift could no longer be observed and the variation of relative charge density were identical for both structure. These observations support the hypothesis that the turn-around observed in this low-voltage bilayer structure could be attributed to the long range interaction between dipoles in the dielectric material, or to simply put it, to the residual ferroelectric behaviour in the P(VDF-TrFE-CTFE).

Conclusion and perspective

5.1. CONCLUSION

This work was articulated around the advancement of low-voltage organic transistors while maintaining their compatibility with large area processing or printing methods. As such, we chose to study the implementation of high- κ polymer as gate insulator since they appeared to be the most suitable for this specific problematic. Consequently, the goal of this study was to highlight and understand the relationship between the high- κ material's dielectric properties and the performance of the resulting low-voltage transistors.

In the earliest part of this thesis, we selected derivatives of the polyvinylidene fluoride (PVDF) as the main focus of our study. Since these terpolymers displayed the highest recorded permittivity amongst the typical of polymeric insulators available, they were considered to be the best high- κ candidate from this class of materials.

We first established a link between the variation in composition of the P(VDF-TrFE-CTFE) and the evolution in its dielectric properties. As the proportion of the third monomer (CTFE) increased in the terpolymer chain, its polarization behaviour evolved from a true ferroelectric to a relaxor-ferroelectric effectively reducing the

width of the hysteresis and increasing the dielectric constant of the polymer. Since; at first order; a desirable dielectric for low-voltage transistors should present the highest permittivity with the smallest hysteresis possible, we chose to study the terpolymer with the highest CTFE content available. This specific composition presented a permittivity of approximately 35 which is fifteen times superior to the classic low- κ dielectric used as a reference.

We then thoroughly studied the impact of bias, frequency and temperature on the measured properties of this material. The selected terpolymer showed strong dependency with all three aforementioned measurement parameters: saturation of capacitance and polarisation could be observed with an increased bias, a drop in capacitance with the increase of solicitation frequency, but also a capacitive response closely resembling one seen in pristine ferroelectrics when reaching a Curie temperature (reaching a peak around 45 °C). Because of the activation of conduction (leakage), we were not able to confirm the vanishing of polarization hysteresis above the supposed T_C . Nevertheless, as the transistor structure was less sensitive to leakage, the evolution of polarization with temperature could be evaluated further in the study.

In order to evaluate and define a potential linear window of operation for this high- κ dielectric, we used a simple electrical model based on various linear components to fit the low field polarization profile of the terpolymer. The fit produced an exact match to the measured polarization up until approximately 40 V/ μm thus delimiting a voltage below which the terpolymer could be considered equivalent to a linear lossy dielectric.

As high- κ material are often used in conjunction with a layer of low- κ , we studied the impact of such structure on the capacitance and polarization measurements by producing four bilayer dielectrics with an increasing D320 thickness. The equivalent permittivity of these devices closely followed the one predicted by the theoretical equations of linear capacitors in series which further supported the hypothesis of linear behaviour. The polarization profile of these bilayer structures appeared to

be a trade-off between the polarization response of its sub-layer as it produced a cycle with a higher polarization than the low- κ and a drastically reduced hysteresis when compared to the terpolymer. We then fitted the previously mentioned linear electrical model to the polarization measurement conducted on the bilayer with the thinnest layer of D320 available ($X \approx 0.9\%$; $d_{tot} = 540\text{ nm}$). The frequency stability was equivalent to the one observed in the pristine terpolymer. However, the critical linear field measured for this structure was approximately $150\text{ V}\cdot\mu\text{m}^{-1}$ indicating a great improvement in its bias stability which was then supported by capacitance measurements.

Once the in-depth characterization of the terpolymer and bilayer dielectrics were performed, the next step of this study was to investigate their implementation as gate insulator for transistors. First, we have fabricated a standard transistor structure using the low- κ as gate dielectric to establish a reference baseline of performance to evaluate the impact of the terpolymer on the transistor. This reference structure displayed a median mobility of approximately $0.7\text{ cm}\cdot\text{V}^{-1}\cdot\text{s}^{-1}$ and a threshold voltage of approximately -4.85 V in linear regime. The average contact resistance of this structure was measured to be $4.0\cdot 10^3\ \Omega\cdot\text{cm}$ at $V_{GS} = -30\text{ V}$ and $V_{DS} = -0.1\text{ V}$, which did not introduce any noticeable “S-shape” in the output curves. With a relatively good device-to-device reproducibility and a yield of approximately 87% this reference structure offered a strong point of comparison for the rest of this study.

The direct implementation of the terpolymer onto the semiconductor resulted in a transistor with large hysteresis and a degraded mobility. Moreover, very few transistors on the foil were functional due to high amount of leakage. To circumvent this degradation we implemented a 120 nm low- κ buffer layer onto the semiconductor prior to the deposition of the terpolymer. This simple bilayer structure was used as a proof of concept and a first approach to understand the impact of the bilayer dielectric into the transistor structure.

The fabricated PoC_A foil presented a reduced threshold voltage compared to the reference ($V_{th} \approx -1.6\text{ V}$), this reduction was comparable to the increase in gate

capacitance provided by the bilayer dielectric. However, this structure was not as performing as the reference in terms of mobility ($\mu_{FE} \approx 0.55 \text{ cm.V}^{-1}.\text{s}^{-1}$) and yield of functioning devices (71 %). This degradation of performance could be caused a lesser interface quality between the semiconductor and the low- κ . Moreover, the introduction of the terpolymer in the transistor stack generated a clockwise hysteresis compatible with its relaxor-ferroelectric behaviour exhibited in polarization. It also introduced a difference between the forward and reverse extracted mobility, this deviation could have been introduced by the approximation of the bilayer capacitance to a linear dielectric, thus overlooking the hysteretic component introduced by the RFE behaviour in its real capacitive response.

To better understand the impact of the bilayer structure onto the transistor's characteristic we fabricated four bilayer transistors with each an increased low- κ thickness, ranging from 60 *nm* to 600 *nm*. All of these new fabricated foils presented mobilities equivalent to the reference along with a yield of approximately 90% even at the lowest D320 thickness, which indicated that the loss of performance displayed by the PoC_A foil was probably introduced by environmental parameter rather than by the integration of the bilayer dielectric.

In these four structures, the threshold voltage versus gate insulators capacitance evolution closely followed the trend predicted by the equation of threshold voltage in MOSFETs. This observation further supported the hypothesis that the bilayer dielectric could be approximated, on the first order, to a linear dielectric in the range of thickness and voltage studied here. No visible trend could be noticed in the evolution of hysteresis versus thickness as all four devices displayed a negative hysteresis (clockwise) in the same order of magnitude ($\Delta V_{th} \approx -300 \text{ mV}$). Furthermore, no clear trend appeared in the evolution of hysteresis width when the measurement speed was modified.

With a better understanding of the general properties of bilayer transistors, we have been able to produce an optimized dielectric structure presenting an average permittivity of 12.70 for a total thickness of 494 *nm*. In order to probe the

reproducibility of this optimized dielectric, two identical foils of transistors were fabricated : OPT_A and OPT_B. Both foils presented a median threshold voltage of approximately -400 mV , a median mobility of approximately $0.7\text{ cm.V}^{-1}.s^{-1}$ and a clockwise hysteresis of approximately -200 mV . The standard deviation of these extracted parameters was mostly below 10% of median value. Moreover, distribution of both foils was overlapping thus indicating a relatively good foil-to-foil reproducibility. Considering that a transistor's operating voltage is considered achieved at three times its threshold voltage this optimized bilayer transistor structure could be considered to be in operation at -3.3 V . We are confident that this operating voltage and the dispersion of threshold voltage could be further improved with better processing capability (ie: thinner and more homogeneous layers).

Finally, the reference and optimized structure were exposed to electrical stress in order to evaluate the evolution of their properties when in constant electrical solicitation. In the reference, a shift of the transfer curves to the negative values was observed when a negative gate bias stress was applied to the reference structure. This shift appeared to be solely induced by a variation of threshold voltage, probably caused by charge carrier trapping from the channel into the dielectric. This behaviour appeared to be strictly monotonic but moreover was not impacted by the amplitude of gate bias, which could be in contradiction with hypothesis of the diffusion of carrier.

In the case of the bilayer structure, the observed NGBS response appeared to be superposition of a positive threshold voltage shift at early stress time which would then turns into a negative shift comparable to the one seen in the reference. Unlike the reference, this turn-around behaviour was heavily impacted by the amplitude of the gate bias. In order to precisely attribute the cause of this phenomenon we monitored its response to increasing temperature.

Prior to the NGBS measurements in temperature, we monitored its impact on the transfer curves. In both transistor structures, an increase in temperature is accompanied by an augmentation of drain current in the ON region which is caused

by an activation of mobility with temperature. With the fit of a simple Arrhenius law we were able to determine that both devices displayed a similar activation energy thus further supporting the hypothesis that the integration of a bilayer dielectric did not significantly impact the semiconductor's properties and interfaces.

Another impact of the increasing temperature on the transistor's characteristic concerned the evolution of hysteresis. In the case of the reference structure, the trap related hysteresis (anticlockwise) also appeared to be activated with temperature as it widened significantly at 61.6 °C. However, the anticlockwise hysteresis observed at ambient temperatures in the bilayer transistor's characteristic steadily decreased up until no hysteresis was discernible at 41 °C. When the temperature was further increased (64 °C.), its characteristic presented an anticlockwise hysteresis of similar amplitude to the one observed in the reference transistor.

Concerning the NGBS, the monotonic threshold voltage shift observed in the reference was accelerated towards the negative voltage values with higher temperatures. So much so that the final amplitude of the shift was five times larger at 45 °C than at ambient temperature. This acceleration of the negative shift was also observed for the bilayer transistor, where the amplitude of the turn-around phenomenon steadily decreased with temperature. When at 45 °C, no positive shift could be observed in the bilayer's NGBS response. When converted into a relative density of charge at the interface, these high temperature negative shift observed in both structure would match perfectly. This observation supported the statement that the turn-around could be the sum of two different phenomena, the fast positive shift being introduced by the RFE behaviour of the terpolymer and the negative shift occurring at the interface between the low- κ and semiconductor.

In conclusion, the fabrication of a low-voltage organic field effect able to operate below 3.3 V was enabled by the integration of a solution processed high- κ polymer. An in-depth study dielectric in a Metal-insulator-Metal structure provided a good understanding of the capacitance and polarization properties displayed by the terpolymer in a pristine or bilayer structure. These specific properties could

then be used to explain some of stress and temperature behaviours presented by the low-voltage bilayer transistor.

5.2. PERSPECTIVE

While many interesting results were discussed in this works, there are some part of this study that could be further investigated.

For example, further investigation on the high- κ polymer chemistry could be pursued either with the study of higher CTFE content, a larger array of compositions or conducting a similar study onto the P(VDF-TrFE-CFE). As mentioned in Chapter 1, our access to this material was limited for the most part of study. Nevertheless, by the end of this work we managed to fabricate a bilayer transistor integrating the CFE terpolymer as the high- κ component of the bilayer transistor. The fabricated device presents little current hysteresis when compared to the optimized CTFE bilayer ($\Delta V@1 \text{ nA} = -56 \text{ mV}$; total measurement speed $\approx 6 \text{ s}$) with an equivalent operating voltage (Figure 5.1 a)). However, the fact that a negative hysteresis is still present and that the NGBS response of this CFE bilayer displayed a turn-around indicates that there is a RFE behaviour in the P(VDF-TrFE-CTFE) (Figure 5.1 b)). Behaviour that could be investigated with a similar approach than the one proposed in this work.

In Chapter 3 we investigated the stability of the bilayer and reference transistor in frequency. While we were able to probes the evolution of current hysteresis in bilayer transistors with the help of the delay protocol, this measurement was only able to monitor relatively low solicitation frequencies ($f \approx 0.05 \text{ Hz}$ to $f \approx 0.002 \text{ Hz}$). For circuit applications, the validity of dynamic behaviour should be evaluated with higher frequencies. The small signal response of the current (above threshold voltage) at a high frequency input on the gate electrode could yield information on the stability of the low-threshold voltage related to the high capacitance of the RFE dielectrics. A direct approach would be to integrate this bilayer transistor into a

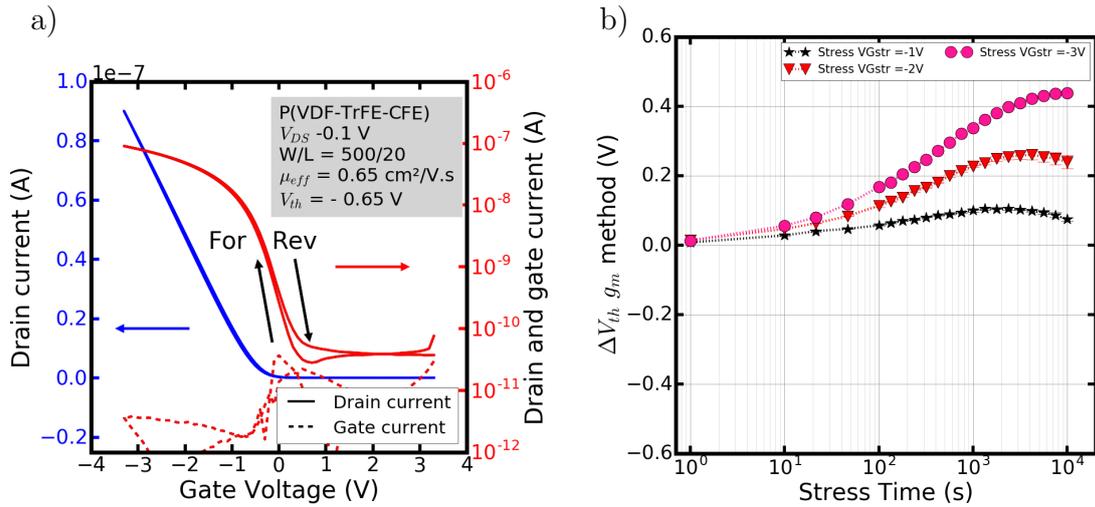


Figure 5.1: a) linear regime transfer curve of a bilayer transistor implementing a CFE terpolymer and b) the NGBS response associated to the CFE bilayer transistor.

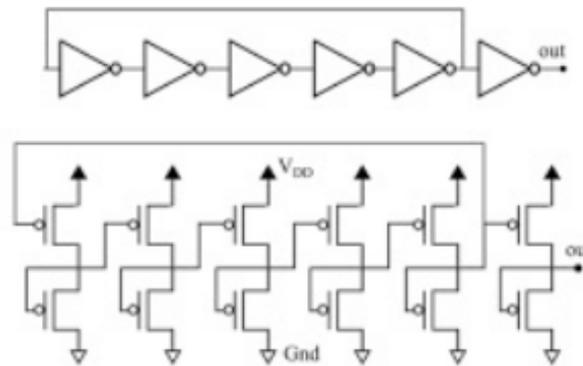


Figure 5.2: Electrical schematic of a five stage ring oscillator (reproduced from [130]).

ring oscillator structure (Figure 5.2), the impact of relatively high frequency on the transistor characteristic could theoretically be extracted[130].

A Final perspective of this work would be the transfer of the bilayer technology to printing process. The spin-coating method used in this work is an effective tool for the study of various array of solutions but is relatively limited when a specific deposition pattern is required (ie: circuits).

The formulation of the dielectric inks would need a specific adaptations, yet thanks to their polymeric nature and because of the range of targeted thickness we are confident that the transfer of the bilayer technology to printing process like

gravure printing could provide similar homogeneity and overall performance of the low-voltage bilayer transistor. The scale up of such technologies in printed OTFT circuits could enable direct compatibility with batteries and classic silicon chips.

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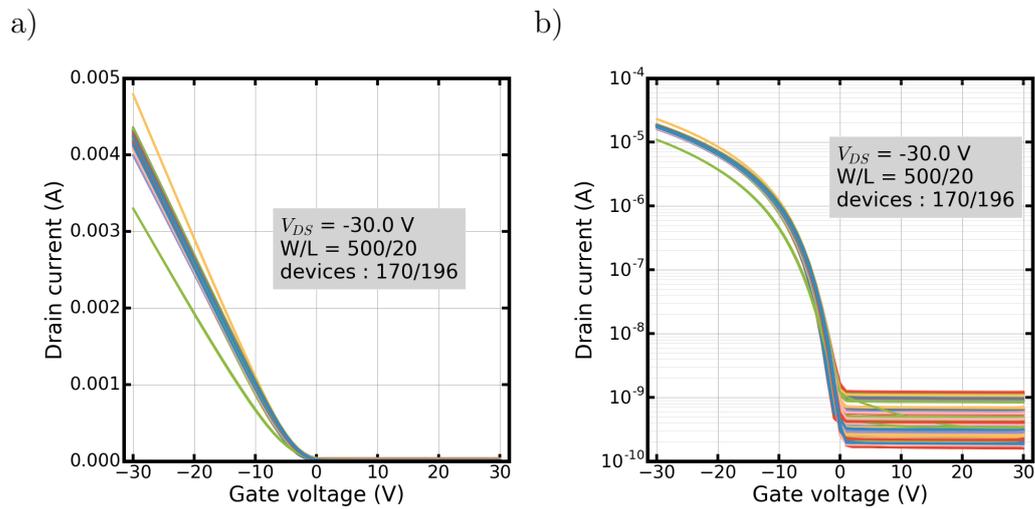
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Annex

ANNEX A



ANNEX B

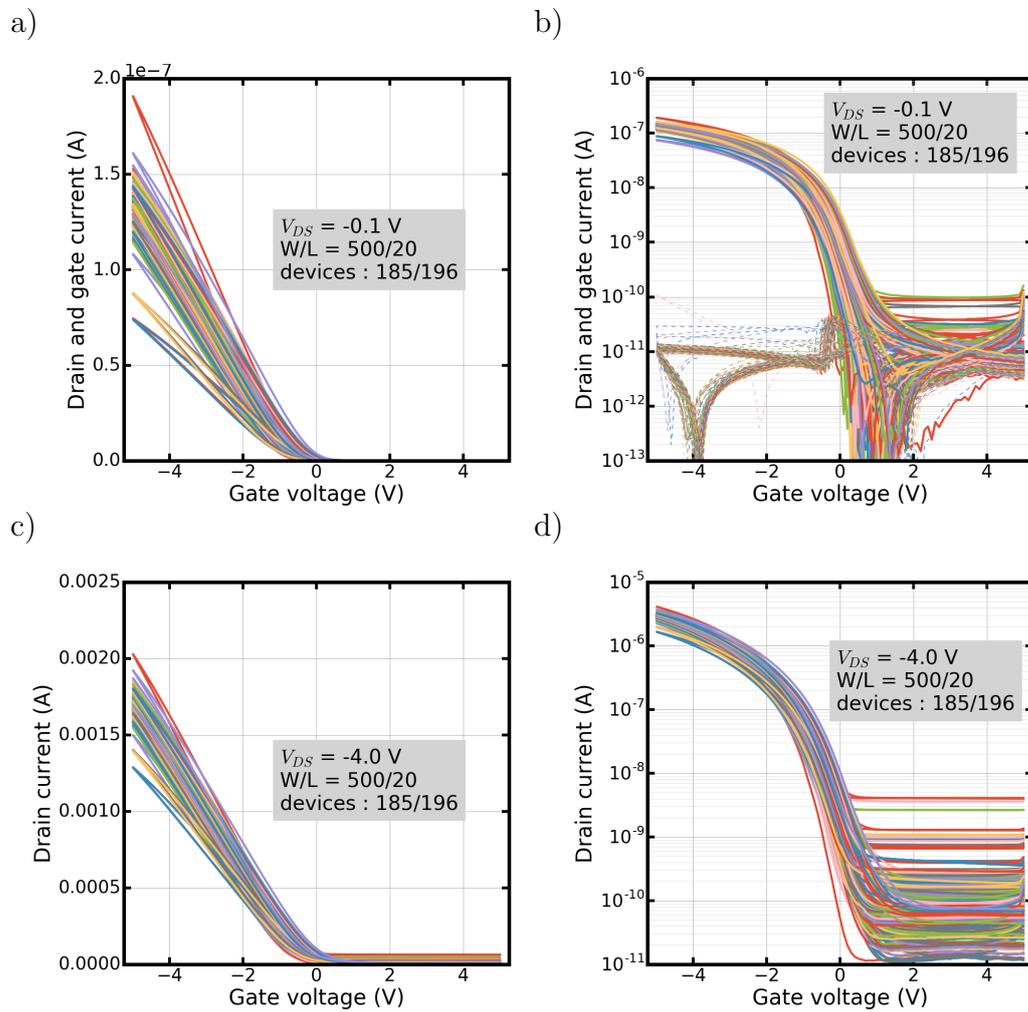


Figure .4: Foil A transfer curves a)b)linear regime and c)d) saturation regime.

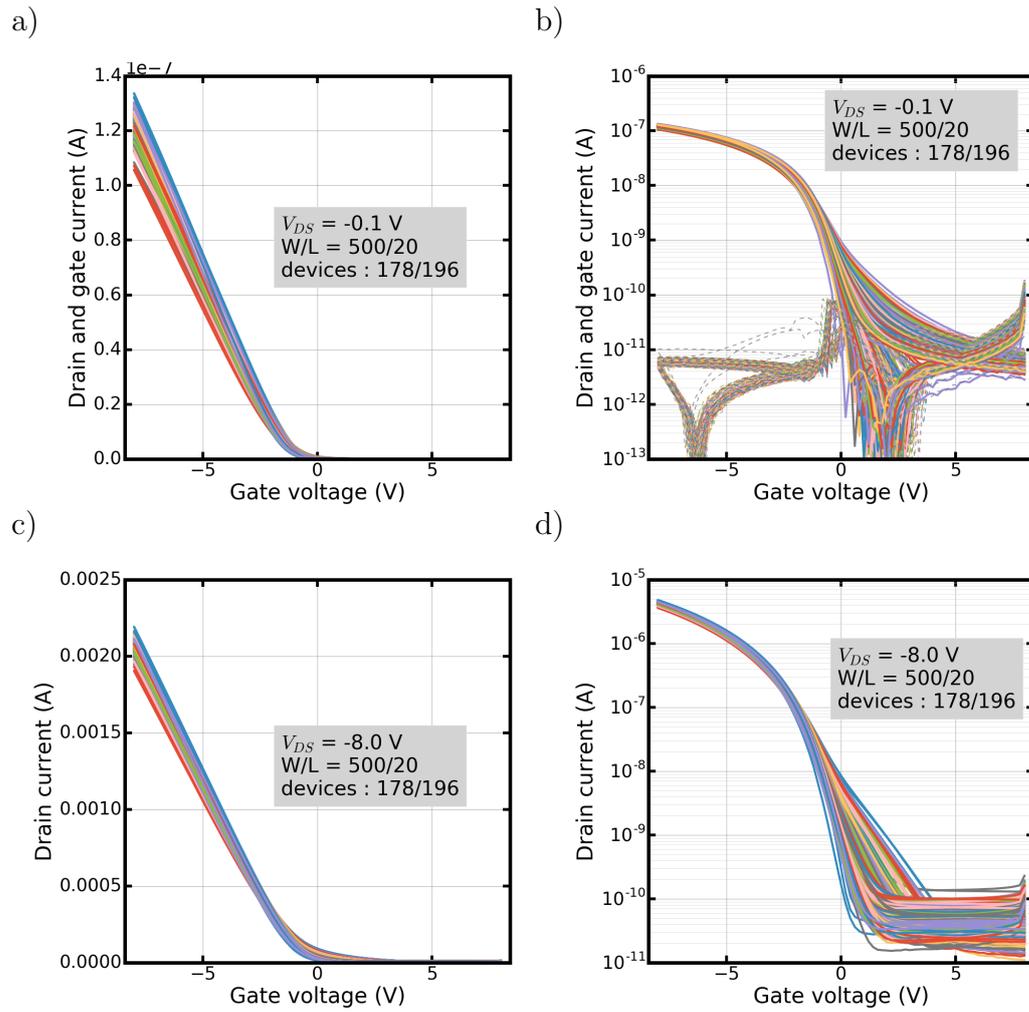


Figure .5: Foil B transfer curves a)b)linear regime and c)d) saturation regime.

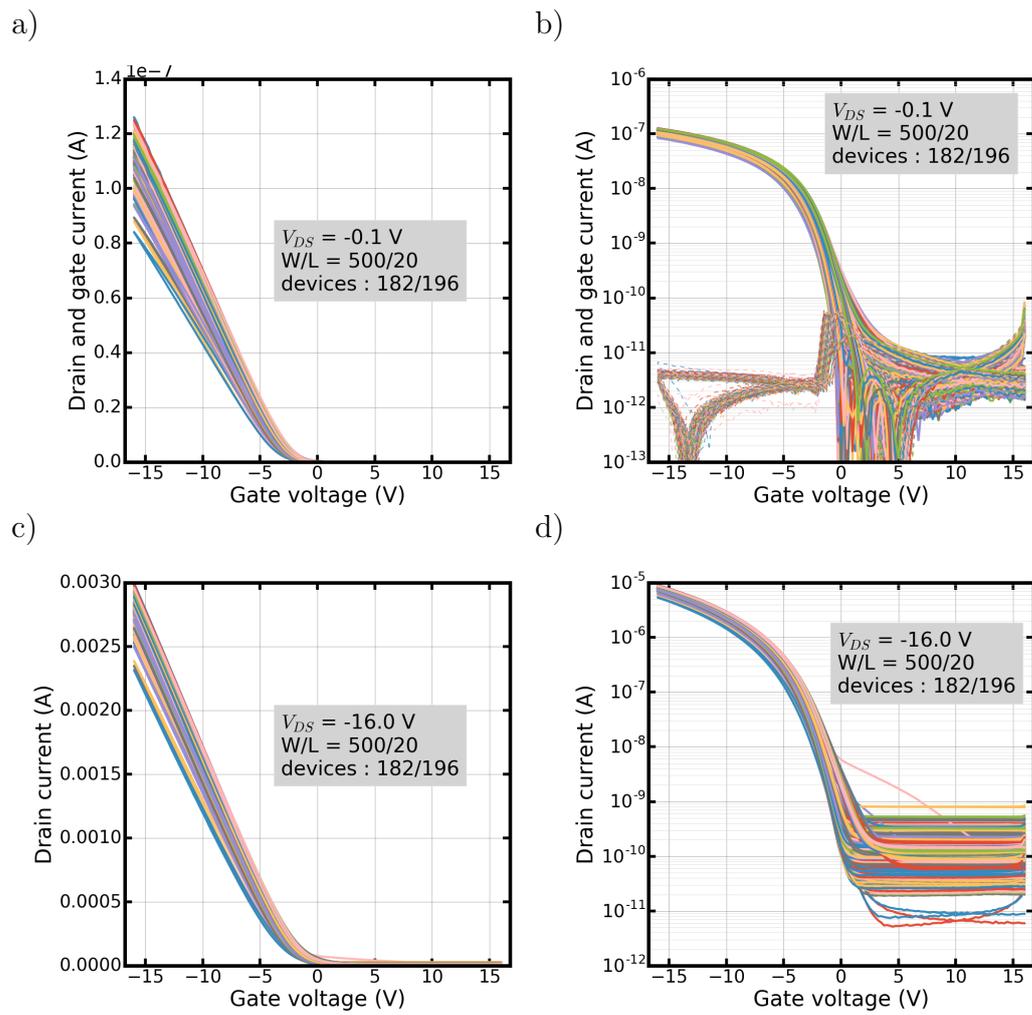


Figure .6: Foil C transfer curves a)b)linear regime and c)d) saturation regime.

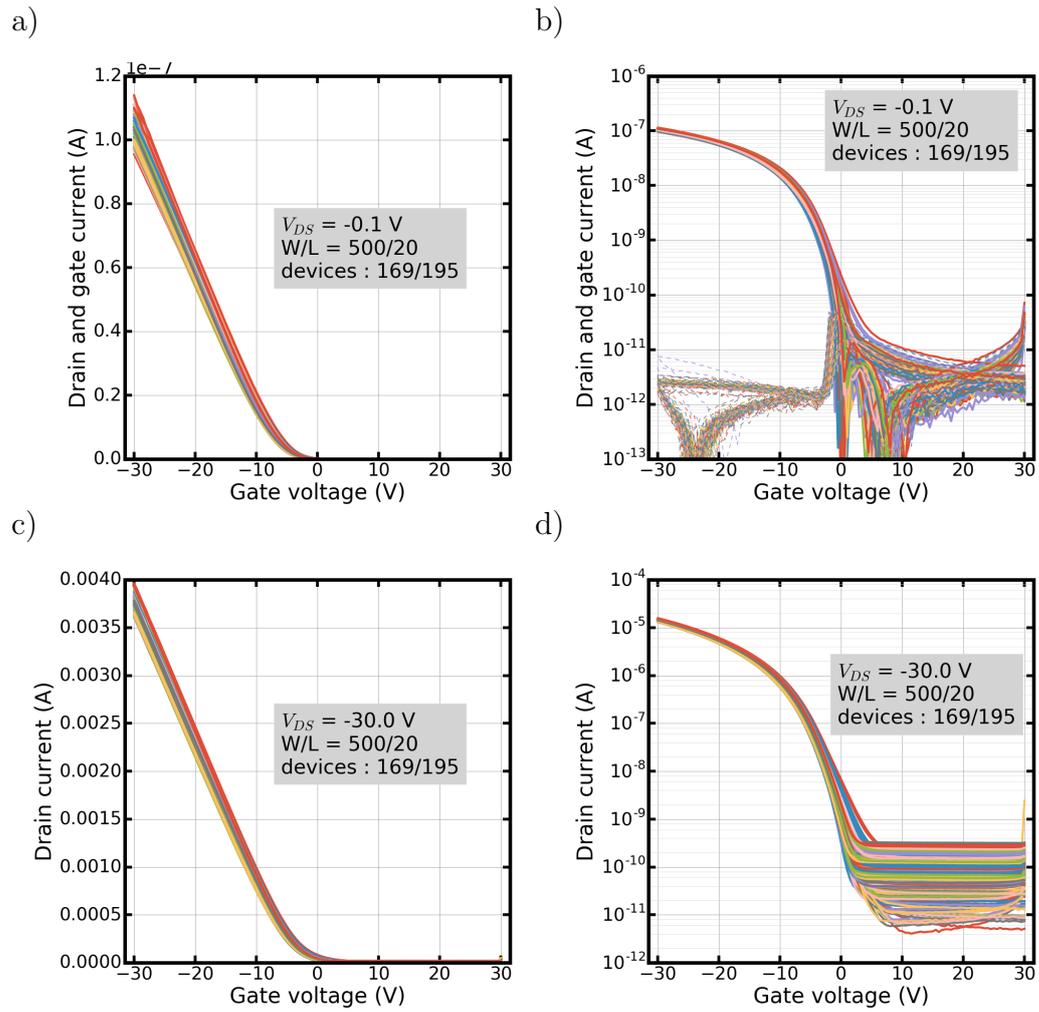


Figure .7: Foil C transfer curves a)b)linear regime and c)d) saturation regime.

Table .1: Extracted parameters for the second quadrant of the bilayer foil A, B,C and D (median \pm standard deviation).

Sample	Mode	Direction	μ_{eff} ($cm^2.V^{-1}.s^{-1}$)	V_h (V)	SS ($mV.dec^{-1}$)	N_n (cm^{-2})	ΔV at 1 nA (V)	I_{ON} (A)
Bilayer A $C_i = 18.88 nF.cm^{-2}$	Linear $V_{Ds} = -0.1 V$	Forward	0.71 ± 0.06	-0.99 ± 0.10	184 ± 110	$2.46e^{11} \pm 2.17e^{11}$	-0.42 ± 0.05	$1.32e^{-7} \pm 0.12e^{-7}$
		Reverse	0.63 ± 0.05	-0.34 ± 0.10	484 ± 33	$8.37e^{11} \pm 0.65e^{11}$		
	Saturation $V_{Ds} = -4 V$	Forward	0.65 ± 0.05	-0.67 ± 0.11	514 ± 183	$8.98e^{11} \pm 3.63e^{11}$	-0.30 ± 0.04	$2.83e^{-6} \pm 0.28e^{-6}$
		Reverse	0.54 ± 0.05	-0.19 ± 0.09	500 ± 56	$8.69e^{11} \pm 1.1e^{11}$		
Bilayer B $C_i = 11.15 nF.cm^{-2}$	Linear $V_{Ds} = -0.1 V$	Forward	0.69 ± 0.03	-1.56 ± 0.07	773 ± 229	$8.35e^{11} \pm 2.68e^{11}$	-0.24 ± 0.07	$1.22e^{-7} \pm 0.05e^{-7}$
		Reverse	0.66 ± 0.03	-1.26 ± 0.06	935 ± 128	$1.02e^{12} \pm 1.5e^{11}$		
	Saturation $V_{Ds} = -8 V$	Forward	0.66 ± 0.03	-1.12 ± 0.05	927 ± 659	$1.02e^{12} \pm 7.71e^{11}$	-0.12 ± 0.05	$4.29e^{-6} \pm 0.20e^{-6}$
		Reverse	0.62 ± 0.03	-0.95 ± 0.03	970 ± 179	$1.06e^{12} \pm 2.09e^{11}$		
Bilayer C $C_i = 5.27 nF.cm^{-2}$	Linear $V_{Ds} = -0.1 V$	Forward	0.76 ± 0.05	-4.28 ± 0.46	395 ± 193	$1.86e^{11} \pm 1.07e^{11}$	-0.31 ± 0.24	$1.12e^{-7} \pm 0.07e^{-7}$
		Reverse	0.71 ± 0.06	-3.6 ± 0.56	1344 ± 134	$7.11e^{11} \pm 0.74e^{11}$		
	Saturation $V_{Ds} = -16 V$	Forward	0.67 ± 0.03	-2.84 ± 0.27	1282 ± 193	$6.76e^{11} \pm 1.61e^{11}$	-0.26 ± 0.08	$7.64e^{-6} \pm 0.61e^{-6}$
		Reverse	0.64 ± 0.03	-2.43 ± 0.23	1272 ± 195	$6.71e^{11} \pm 1.08e^{11}$		
Bilayer D $C_i = 2.95 nF.cm^{-2}$	Linear $V_{Ds} = -0.1 V$	Forward	0.65 ± 0.03	-8.06 ± 0.59	674 ± 199	$1.90e^{11} \pm 0.62e^{11}$	-0.196 ± 0.10	$1.05e^{-7} \pm 0.03e^{-7}$
		Reverse	0.64 ± 0.03	-7.51 ± 0.70	2502 ± 194	$7.56e^{11} \pm 0.55e^{11}$		
	Saturation $V_{Ds} = -30 V$	Forward	0.62 ± 0.02	-5.06 ± 0.26	2293 ± 793	$6.92e^{11} \pm 2.46e^{11}$	-0.08 ± 0.06	$1.42e^{-5} \pm 0.05e^{-5}$
		Reverse	0.61 ± 0.02	-4.78 ± 0.03	2262 ± 221	$6.84e^{11} \pm 0.69e^{10}$		

ANNEX C

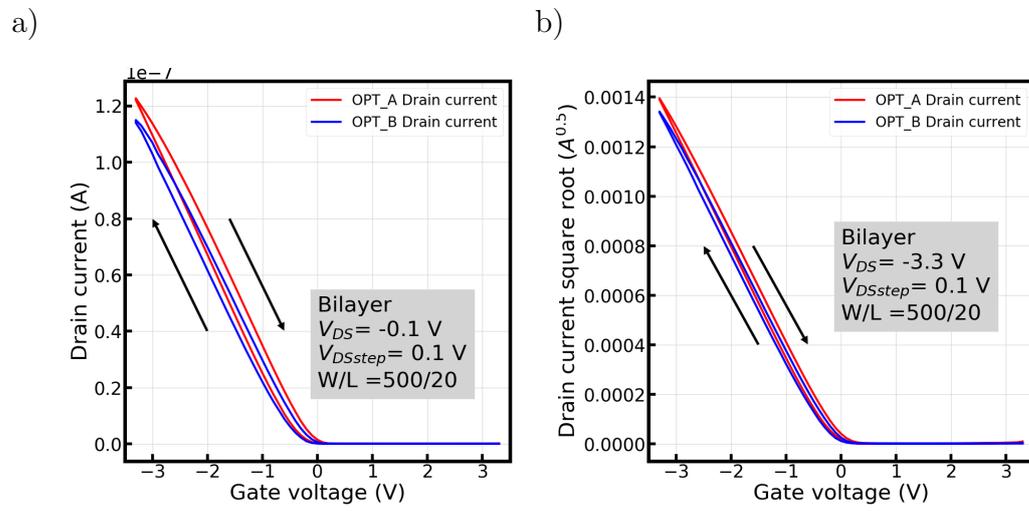


Figure .8: Comparison of transfer curves for OPT_A (red) and OPT_B (blue) in a) linear and b) saturation regime (linear scale).

ANNEX D

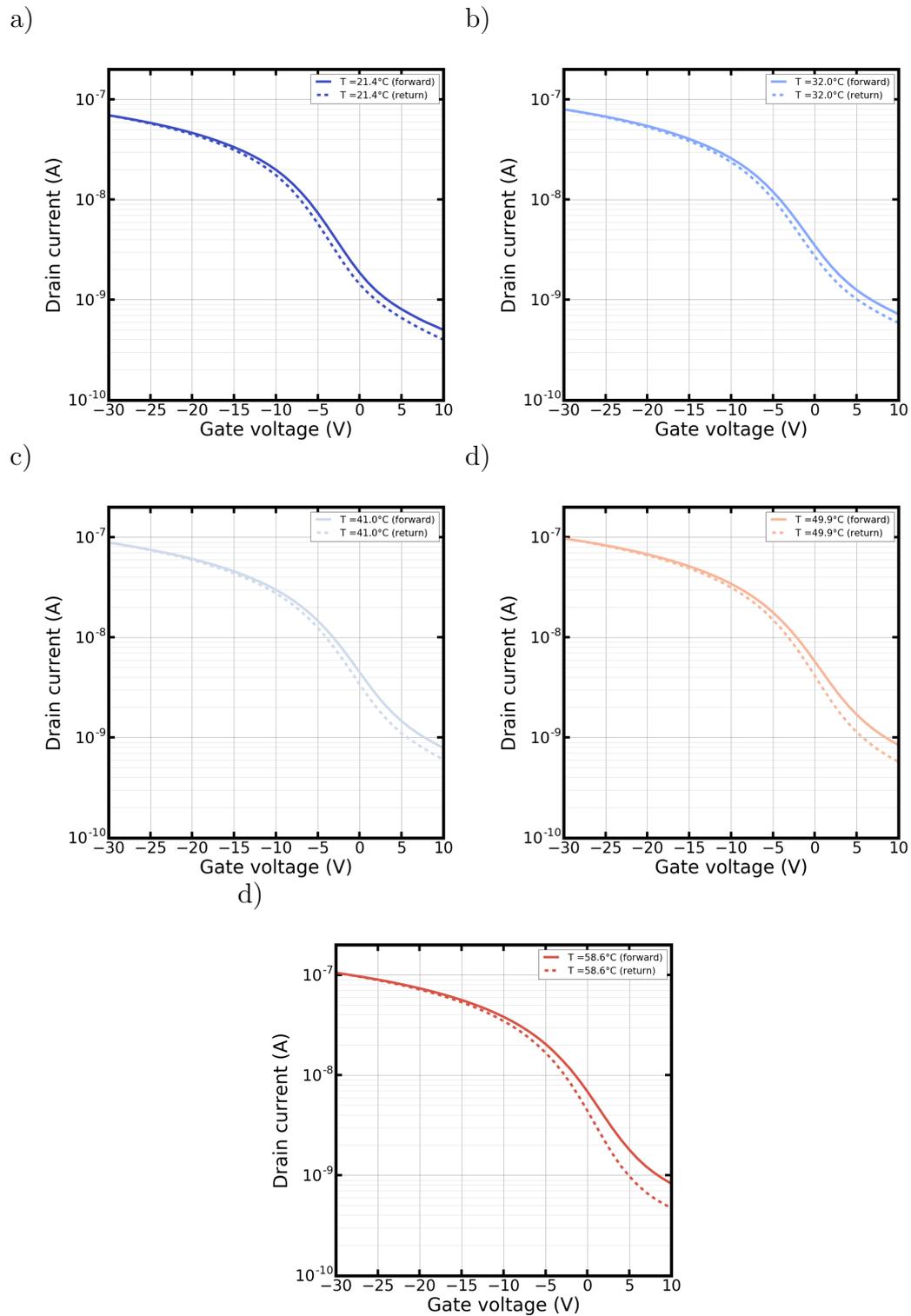


Figure .9: Illuminated transfer curves for the Reference at various temperatures a) 21.4°C , b) 32.3°C , c) 41°C , d) 49.9°C and e) 58.6°C .

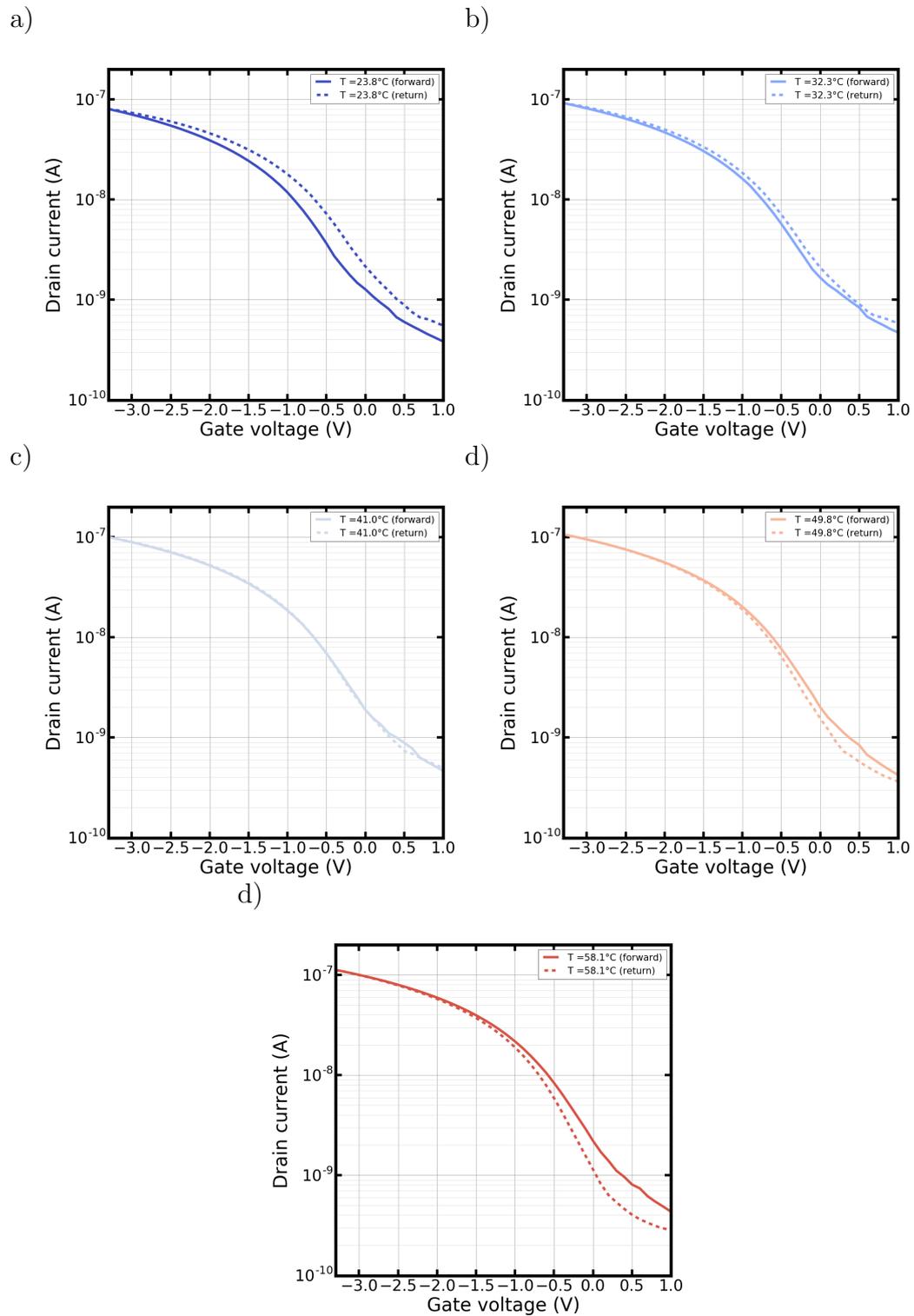


Figure .10: Illuminated transfer curves for the bilayer at various temperatures a) 23.8°C , b) 32.3°C , c) 41°C , d) 49.8°C and e) 58.1°C .

List of acronyms

BTS Bias Temperature Stress

DHL Dual Hysteresis Loop

ELR Extension of Linear Regime

FDSOI Fully Depleted Silicon On Insulator

FE Ferroelectric

FET Field Effect Transistor

GBS Gate Bias Stress

HOMO Highest Occupied Molecular Orbital

LUMO Lowest Unoccupied Molecular Orbital

MIM Metal-Insulator-Metal

MIS Metal-Insulator-Semiconductor

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

NGBS Negative Gate Bias Stress

OFET Organic Field Effect Transistor

OTFT Organic Thin Film Transistor

PEN Polyethylene naphthalate

PVDF polyvinylidene fluoride

P(VDF-TrFE) poly(vinylidene fluoride-co-trifluoroethylene)

P(VDF-TrFE-CFE) poly(vinylidene fluoride-ter-trifluoroethylene-ter-1-chloro-1-fluoroethylene)

P(VDF-TrFE-CTFE) poly(vinylidene fluoride-ter-trifluoroethylene-ter-chlorotrifluoroethylene)

Q2 Second quadrant

Q4 Fourth quadrant

QSCV Quasi-Static capacitance versus voltage

SAM Self-Assembled Monolayer

SHL Single Hysteresis Loop

T³G Trans Trans Trans Gauche orientation

TFT Thin Film Transistor

TG Trans Gauche orientation

TLM Transfer Line Measurement

List of symbols

Symbol	Description
C_0	Reference frequency
C_D	Depletion layer capacitance
C_{eq}	Equivalent capacitance for the bilayer
C_{FE}	Capacitance of the ferroelectric sample
C_{gc}	Gate to channel capacitance
C_i	Insulator surface capacitance
C_{it}	Interface states capacitance
C_p	Parallel capacitor
C_s	Series Capacitor
\vec{D}	Displacement field
d_i	Insulator's thickness
\vec{E}	Electrical field
E_a	Trap activation energy
E_{cond}	Conduction band level
E_F	Effective Fermi level
E_g	Band gap
E_i	Intrinsic Fermi level
E_{val}	Valence band level

Symbol	Description
f	Frequency
gm	Transconductance
I	Current
$I_{D\ lin}$	Linear drain current
$I_{D\ sat}$	Saturation drain current
I_G	Gate current
I_{ON}	ON current
I_{OFF}	OFF current
\vec{J}	Density of current
k_b	Boltzmann constant
L	Channel length
N_{it}	Density of interface states
\vec{p}	Dipolar moment
\vec{P}	Polarization field
P_{max}	Maximal polarization
P_r	Remnant polarization
P_s	Saturation polarization
q	Elementary charge
Q_{acc}	Accumulation charge
$Q_{acc\ th}$	Threshold accumulation charge
Q_b	Bounded charge
q_{Cp}	Quantity of charge generated by the parallel capacitor
Q_{D320}	Net charge at the low- κ layer's interfaces
Q_{FE}	Net surface charge at the ferroelectric sample electrodes
Q_{inv}	Inversion charge
$Q_{inv\ th}$	Threshold inversion charge
Q_{PDVF}	Net charge at the high- κ layer's interfaces

Symbol	Description
q_{Rp}	Quantity of charge generated by the parallel resistance
q_{RsCs}	Quantity of charge generated by the series resistor and capacitor
Q_{tot}	Net charge at the bilayer capacitor's electrodes
R^2	Coefficient of determination
R_c	Contact resistance
$R_{channel}$	Resistance of the semiconducting channel
R_p	Parallel resistor
R_s	Series resistor
S	Surface
SS	Subthreshold swing
T	Temperature
t	time
T_C	Curie temperature
U	Level
U_{DC}	Bias
v	Volume element
V	Potential
V_0	Effective voltage drop across the insulator
V_{DS}	Voltage applied to the drain respective to the source
$V_{DS\ sat}$	Pinch-off voltage
V_{FB}	Flat-band voltage
V_{GS}	Voltage applied to the gate respective to the source
$V_{GS\ max}$	Maximal gate voltage
$V_{GS\ str}$	Gate bias during the stress
$V_{GS\ step}$	Voltage step during gate voltage sweep

Symbol	Description
V_{th}	Threshold voltage
$V_{th\ lin}$	Linear threshold voltage
$V_{th\ sat}$	Saturation threshold voltage
V_{tot}	Total voltage applied on bilayer capacitor
W	Channel width
Z	Complex impedance
ΔN_{ot}	Relative density of charge variation at the interface
ΔV_{th}	Variation of threshold voltage
ε	Absolute permittivity
ε_0	Vacuum permittivity
ε_r	Relative permittivity or dielectric constant
κ	Relative permittivity or dielectric constant
μ_0	Low-field mobility
μ_{BL}	Band like mobility
μ_{eff}	Effective mobility
μ_{FE}	Field effect mobility
$\mu_{FE\ lin}$	Linear regime field effect mobility
$\mu_{FE\ sat}$	Saturation regime field effect mobility
ρ	Electrical resistivity
σ	conductivity
σ_s	surface charge
τ	Time constant
ϕ	Phase
ϕ_m	Work function
χ	Electric susceptibility
χ_i	Insulator electronic affinity
χ_{sc}	Semiconductor electronic affinity
Ψ_s	Surface potential at the semiconductor interface

Symbol	Description
ω	Pulsation

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“Investigation on Hysteresis and Bias Stress Behavior for low-Voltage Organic Transistor Based on Relaxor-Ferroelectric Polymers”

A. Gaitis, M. Charbonneau, R. Coppard, C.Serbutoviez, G. Ghibaudo

- InnoLAE 2018, Cambridge, United Kingdom

“Stability and In Depth Characterization of Low-Voltage Organic Thin Film Transistor Based on Low-k/High-k Bilayer Dielectric”

A. Gaitis, M. Charbonneau, R. Coppard, C.Serbutoviez, G. Ghibaudo

ARTICLES

T.Sekine, **A. Gaitis**, J. Sato, K. Miyazawa, K. Muraki, R. Shiwaku, Y. Takeda, H. Matsui, D. Kumaki, F. Domingues Dos Santos, A. Miyabo, M. Charbonneau, S. Tokito.

“Low Operating Voltage and Highly Pressure-Sensitive Printed Sensor for Healthcare Monitoring with Analogic Amplifier Circuit”

ACS Appl. Electron. Mater., 2019, 1 (2), pp 246252

A. Gaitis, M. Charbonneau, R. Coppard, C.Serbutoviez, G. Ghibaudo

“Impact of Gate Bias Stress Impact on Low-k/High-k Dielectric Structure for Low-Voltage Organic Transistors”

To be submitted

Resumé français

Cette thèse s'articule autour de l'étude des diélectriques à haute permittivité et de leurs implémentation dans la structure des transistors organiques afin de proposer une solution pour réduire leurs tensions de fonctionnement tout en restant compatible avec des processus de fabrication par impression. La première partie cette thèse se concentre sur la théorie des semi-conducteurs et transistors organiques ainsi que les différentes approches de réduction de tensions proposées dans la littérature. Elle se focalisera ensuite sur l'étude des propriétés diélectriques de matériaux polymère à haute permittivité issu du PVDF (Polyfluorure de vinylidène) ainsi que de l'impact de la composition du matériau, la fréquence, la tension de mesure ainsi que de la température sur le caractère relaxeur-ferroélectrique qu'exhibe ces matériaux polymères. L'étude portera ensuite sur l'intégration du terpolymère en tant qu'isolant de grille dans une structure de transistor organique et de son impact sur la caractéristique du dit transistor. L'évolution du comportement électrique de cette nouvelle structure de transistor sera comparée à une référence utilisant un diélectrique standard ainsi qu'aux observations sur le comportement diélectrique tirées du chapitre 2. Finalement, on étudiera la fiabilité électrique de ces deux structures de transistor en les soumettant à un stress électrique de plusieurs heures, puis en comparant l'évolution de leurs propriétés.

English summary

This thesis discusses the study of high permittivity dielectrics and their implementation in the organics transistors structure in order to reduce their operating voltage while maintaining their compatibility with solution/printing processes. The first part of this work focusses on the theory of organic semiconductors and transistors. It will also discuss the various approaches proposed in the literature to reduce operating voltage in such devices. It will then discuss the study of the dielectric properties of materials derived from the PVDF (polyvinylidene fluoride). The evolution of the relaxor-ferroelectric behaviour exhibited by these polymers will be monitored versus the chemical composition, frequency, bias and temperature. After an in-depth characterization of the high-k dielectric in a capacitor structure, we will evaluate its impact on the transistors characteristic and compare the performance of this new devices to a reference transistor. These observation will be compared to the study of the dielectric in Chapter 2 in order to gain insight on the physical origin of these new behaviour. Finally, we will study and compare the reliability of the low-voltage and reference transistor with the help of electrical stress.

Mots clefs :
