Innovative devices in FD-SOI technology

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Dispositifs innovants de la technologie FDSOI

Innovative devices in FD-SOI technology

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To my lovely wife Jihye *and two sons Seungmin, Seunghyun*

For my father-in-law Eunhyun and mother-in-law Boktae

For my parents, Younghong and Juemyung

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Best regards to all my friends!

Abstract/Résumé

Investigation of Innovative FDSOI Devices and Applications

The main purpose of this PhD work is to investigate the fundamentals of floating body effects (FBEs) in recent generations of ultrathin FDSOI devices. Several FBEs, (i) kink effect, (ii) gate-induced FBE, (iii) parasitic bipolar transistor, (iv) sharp switching, (v) current hysteresis, and (vi) transient and history effect (MSD), are scrutinized in terms of interaction between holes and electrons in ultrathin transistor body. The key point is that in an n-channel SOI MOSFET the FBEs are originated from the interplay of the excess holes which are either being stored or eliminated. For better understanding of FBEs, the body potential V_b has measured directly in H-gate body contact n-MOSFETs. The dynamic V_b variation has also been monitored successfully thanks to lateral P^+ body contacts extended into the undoped-silicon film underneath the front-gate.

Through the measurements of V_b, there are three major findings highlighted for the first time: (i) correlation between the onset of the FBEs and the V_b variation, (ii) new experimental evidence of super-coupling effect observed while the surface potential is changed from depletion to volume inversion, (iii) establishment of a new technique for extracting threshold voltage V_T compared with the typical methods based on the current-voltage characteristics.

Finally, innovative FDSOI devices such as back-gated InGaAs lateral N^+NN^+ MOSFET, and Z^2-FET sensors, are characterized. We demonstrate the basic performance of the InGaAs-on-Insulator substrate by using Ψ-MOSFET technique. Sensing features of the Z^2-FET are investigated under magnetic field or illumination.

Etude de dispositifs et applications FDSOI innovants

L'objectif principal de ce travail de doctorat est d'étudier les principes fondamentaux des effets de corps flottants (FBE) dans les dispositifs FDSOI ultraminces de dernières générations. Plusieurs FBE, (i) kink, (ii) FBE induit par la grille, (iii) transistor bipolaire parasite, (iv) commutation brusque, (v) hystérésis de courant, et (vi) effet transitoire (MSD), sont examinés en termes d'interaction entre des trous et des électrons dans le corps ultramince. La clé de voûte est que les FBE proviennent de l'interaction des trous en excès qui sont stockés ou éliminés. Pour une meilleure compréhension des FBE, la variation du potentiel interne V_b a été mesurée directement sur les n-MOSFET a contact en H. La variation dynamique de V_b a également été étudiée grâce aux contacts latéraux P^+ prolongés dans le silicium non dopé situé sous la grille avant.

Grâce à la mesure de V_b, trois résultats principaux ont été mis en évidence pour la première fois: (i) la corrélation entre l'apparition des FBE et la variation de V_b, (ii) de nouvelles preuves expérimentales de l'effet de super-couplage observé alors que le potentiel de surface voire entre déplétion et inversion, (iii) une nouvelle méthode d'extraction de la tension de seuil, comparée à la méthode typique basée sur la caractéristique courant-tension.

Enfin, des dispositifs FDSOI innovants, comme le MOSFET latéral N^+NN^+ sur InGaAs à grille arrière, et le Z^2-FET en tant que magnétodiode et capteur optique, sont caractérisés. Nous démontrons les performances de base du substrat InGaAs sur isolant en utilisant la technique du pseudo-MOSFET. Les caractéristiques de détection du Z^2-FET sont vérifiées sous champ magnétique et sous éclairage.

Table of Acronyms

Acronym Nomination	Nomination
BCN	Body contact n-MOSFET
BJT	Bipolar junction transistor
BTBT	Band-to-band tunneling
BOX	Buried oxide
CMOS	Complementary metal oxide semiconductor
CMP	Chemical mechanical polishing
DRAM	Dynamic random access memory
DIBL	Drain induced barrier lowering
DSPT	Double spacer patterning technique
EUV	Extreme ultraviolet
FDSOI	Fully depleted silicon-on-insulator
FBEs	Floating body effects
FET	Field effect transistor
GIFBE	Gate induced floating body effect
GIDL	Gate induced drain leakage
hQFP	Hole quasi Fermi potential
ITRS	International technology roadmap for semiconductors
IC	Integration circuit
MOSFET	Metal oxide silicon field effect transistor
MSD	Meta stable dip
PDSOI	Partially depleted silicon-on-insulator
PBT	Parasitic bipolar transistor
PW	Pulse width
RSD	Raised source and drain
SOI	Silicon-on-insulator
SCEs	Short channel effects
SS	Subthreshold swing
SRH	Shockley-Read-Hall
SOS	Silicon-on-sapphire
SPT	Spacer pattern technique
SEU	Single event upset
SIMOX	Separation by implanted oxygen
TFET	Tunneling field effect transistor
UTBB	Ultrathin body and BOX
Z^2-FET	Zero impact ionization and zero subthreshold swing FET

Table of Symbols

Symbol	Unit	Description
C	F	Capacitance
C_{ox}	F/cm^2	Oxide capacitance per unit area
C_{Si}	F/cm^2	Silicon capacitance per unit area
C_{it}	F/cm^2	Interface trap capacitance per unit area
C_G	F	Total gate capacitance
C_{BOX}	F	Buried oxide capacitance
ΔV_{FB}	V	Shift in flat band voltage
ΔV_T	V	Threshold voltage roll-off due to short channel effect
E_C	J	Conduction band edge
E_V	J	Valance band edge
E_f	J	Fermi energy level
E_g	J	Energy gap of silicon (= 1.12 eV)
E_i	J	Intrinsic Fermi level
$E_{fn,\ fp}$	J	Fermi energy level on the n-side, p-side of a PN diode
ε_0	F/cm	Vacuum permittivity (= 8.854 x 10^{-14})
ε_{Si}	F/cm	Silicon permittivity (= 1.04 x 10^{-12})
ε_{ox}	F/cm	Oxide permittivity (= 3.45 x 10^{-14})
φ_{ms}	V	Work-function difference between metal and silicon
φ_n	V	Electron quasi-Fermi potential
φ_p	V	Hole quasi-Fermi potential
Ψ_S	V	Surface potential
Ψ_B	V	Bulk potential
Ψ_{bi}	V	Built-in potential
Ψ_F	V	Fermi potential
$I_{D,}\ I_S$	A	Drain and source current
$I_{Gf,}\ I_{Gb}$	A	Front-gate and back-gate current
I_b	A	Body current
K_B	J/K	Boltzmann constant (= 1.38 x 10^{-23})
L, W	cm	Source and drain diffusion lengths
L_G, L_{eff}	cm	Gate length in layout, effective gate channel length
N_A, N_D	cm^{-3}	Acceptor, donor impurity density
n_i	cm^{-3}	Intrinsic carrier density
T	K	Absolute temperature (e.g. room temperature = 300 K)
$V_{D,}V_S$	V	Drain and source voltage
V_{Gf}, V_{Gb}	V	Front-gate and back-gate voltage
V_b	V	Body voltage (at body contact terminal)
V_{Tf}, V_{Tb}	V	Front-gate and back-gate threshold voltage
$W_{d,}\ W_{d\ max}$	cm	Depletion-layer width, maximum depletion-layer width
X_j	cm	Junction depth

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Chapter 1

Introduction

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1.1 General Introduction

This first chapter represents a general introduction of silicon-on-insulator (*SOI*) technology. We briefly touch upon scaling limit issues which are well documented in the complementary metal–oxide–semiconductor (*CMOS*) industry. Recently, the scaling trend has begun to saturate and short-channel effects have forced semiconductor manufacturer to abandon the traditional planar bulk MOSFET for novel types of devices such as the Fin-FET or fully depleted SOI devices. In the following section, the state-of-the-art SOI technology is introduced as a realistic option in terms of overcoming the fabrication complexity for the CMOS industry and expanding the scaling limits. In particular, the innovative wafer fabrication process called Smart-Cut^{TM} has been invented and commercialized for high-end and reliable CMOS products. This technology leads to a new business model for those who want to make creative and high performance products. The fundamental features of SOI devices are presented in the following section as well.

1.2 Silicon-On-Insulator (SOI) Technology

SOI technology has emerged about 40 years ago for eliminating the parasitic elements in the bulk CMOS technology. One of the motivations was to decrease the parasitic capacitance of source and drain due to the presence of a buried oxide (*BOX*) underneath the devices [1], [2]. Another motivation for developing SOI technology was the anticipated better robustness of SOI transistors to ionizing radiations, making it attractive for military and aerospace applications [3]–[5]. SOI technology, due to the presence of a BOX layer between the device and the substrate, enables one to achieve a smart solution against the previously issued problems and to enhance device performance. The BOX can prevent the interference for a device active layer from electron-hole pairs generated by a radiation event. Lastly and most importantly, the SOI technology would definitely be a promising alternative to bulk silicon MOSFETs in nanoscale device technology. Since the beginning of the 21st century, SOI technology has steadily increased its market share for specific applications such as a radio frequency (RF) device, advanced satellite components, photonics based on SOI, and solar-cell application. The high manufacturing cost of SOI wafers, however, is an obstacle to its adoption for mainstream CMOS products. Today's CMOS devices have reached the 10 nm node, and bulk MOSFET technology has run out of steam because of insurmountable short-channel effects. In this

respect, the advanced SOI technology enables one to surmount almost all of the technical issues experienced in the bulk CMOS process.

Some of the remarkable features of advanced SOI technology are:

(i) The use of an SOI substrate can inherently eliminate the detrimental parasitic effects such as the source/drain junction capacitance, latch-up, single event upset (*SEU*), and reduce body effect.

(ii) Shallow junctions are easily formed to diminish the SCE by adjusting the thickness of the top silicon.

(iii) Back-channel contribution can be controllable via the competition between the two gates (inter-gate coupling or double gate action).

Furthermore, using the back-gate action, the threshold voltage can be tune, even dynamically, in FDSOI MOSFETs [6].

1.2.1 Scaling Limit of Bulk Silicon MOSFETs

The miniaturization of MOSFETs has been driven by reducing the geometrical parameters of transistor as illustrated to Figure 1.1. It has been enabled the increase of the density of transistors and enhanced the performances of integrated circuits. Hence, semiconductor manufacturers could gain high revenue and got low-cost competitiveness thanks to device scaling.

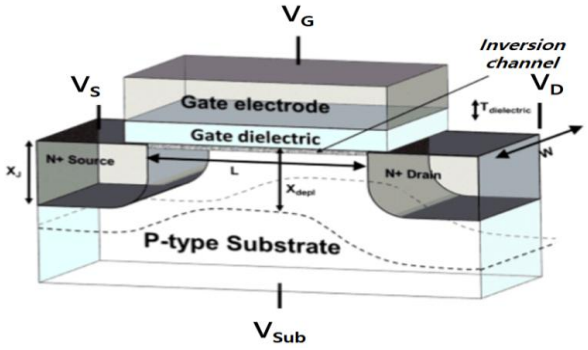

Figure 1.1: A simple schematic view of the bulk MOSFET [7].

However, classical scaling has now reached some fundamental limits and device shrinking is near saturation. For conventional DRAMs, for example, the scaling trend has been tracked well on the market prediction until approximately 29 nm technology node in 2013. In the same generation, by the way, two more nodes (*i.e.* around 25 and 21 nm) were added in order to overcome the patterning complexity and extend the life span of the lithography technique. Since then, the prediction trend of

ITRS began slowing down and even lagging behind the market requirements. The scaling trend was updated in the ITRS 2015, showing three or more than three nodes (i.e. 2x, 2y, 2z and 1x, 1y, 1z, 1a) in the same generation (Fig. 1.2). Major DRAM companies constantly search a breakthrough to meet the market requirements such as lowering operating voltage, reducing power consumption, and increasing high density or bandwidth. Figure 1.3 shows the revolutionary history of scaling the DRAM cell transistor for 25 years. Nowadays, all chip makers have been developing for DRAM products based on a 6F2 layout and a Fin-FET with buried word-line scheme. Furthermore, the development period near the 10 nm technology node becomes almost 2 years long whereas 20 nm nodes had been developed for more or less 1.5 years each.

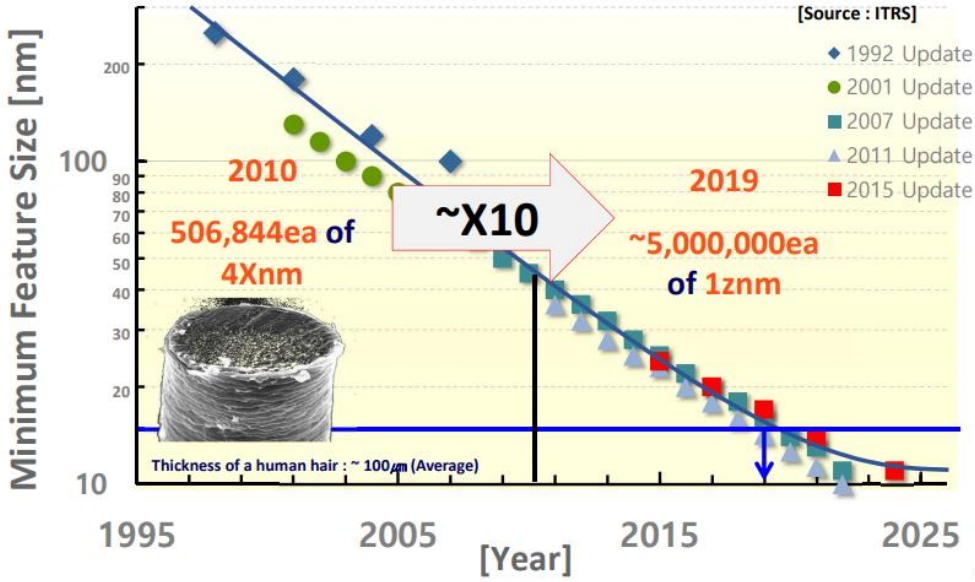

Figure 1.2: Evolution of the DRAM scaling trend with minimum feature size.

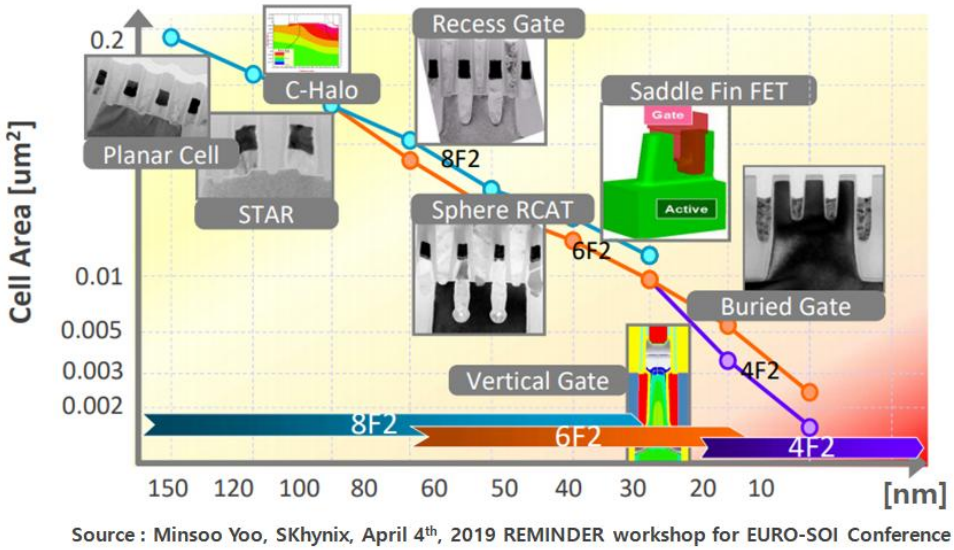

Figure 1.3: History of evolution for DRAM cell transistor and scaling roadmap.

The semiconductor industry is trying its hardest to push scaling to the limits. This requires investments in new equipments, such as extreme-ultraviolet (*EUV*) photolithography. Changing a device structure or material is the other way for pushing scaling to the limit. Among the two transistor architectures adopted by industry, namely the Fin-FET and the FDSOI transistor, we have chosen to study the latter. The family of Silicon-on-Insulator MOSFETs brings versatile benefits in terms of structural point of views such as reduction of junction capacitance, thin silicon body for shallow source/drain junctions, device isolation by buried oxide (*BOX*), and back-gate biasing for threshold voltage tunability.

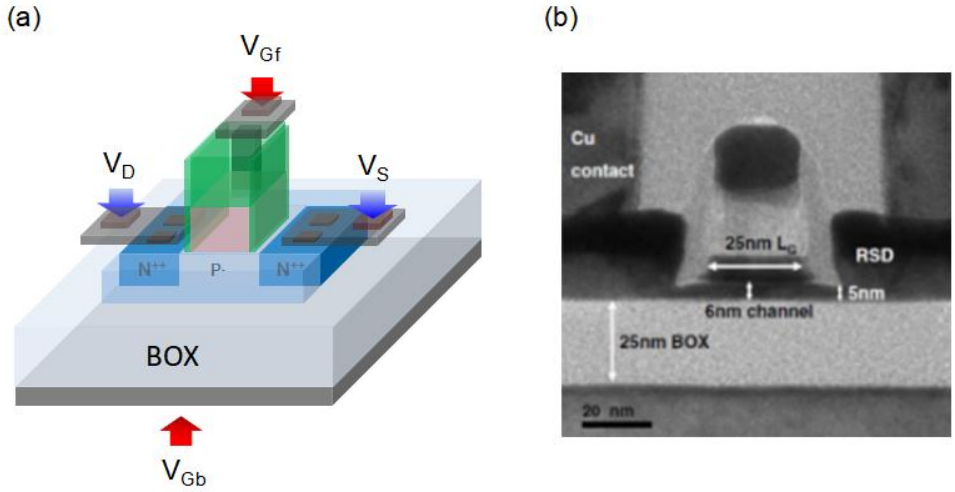

Figure 1.4: (a) 3D-view of a classical Silicon-on-Insulator (SOI) n-MOSFET, (b) a cross-section TEM view of SOI MOSFET fabricated by STMicroelectronics [8].

1.2.2 State-of-the-art of SOI Technology

The SOI technology has unique fundamentals which enhance CMOS device characteristics. It has the following inherent basic features: (i) Dielectric isolation (BOX), (ii) Shallow junction via a thin body (or ultrathin body; UTB), (iii) use of high-quality, ultrathin advanced Smart-Cut^{TM} material. A classical planar fully-depleted (FD) SOI MOSFET can be integrated with a second gate underneath the BOX (back gate) which can be used to modulate the threshold voltage (Fig. 1.4). Double-gate or triple-gate devices, using a multi-gate architecture, care expected to replace single-gate devices at some point in the future. (Fig. 1.5a, b) [7], [9]. Better short channel effect (*SCE*) reduction is the reason why the multi-gate architecture is attractive for making very short transistors. The SCE in the bulk silicon device is inevitably uncontrolled when the gate channel length becomes shorter than about 15 -20 nm. In sub-section 1.2.2, we introduce the multi-gate FDSOI MOSFETs and the way to mitigate the SCE due to improvements in electrostatic control of the channel by the gate.

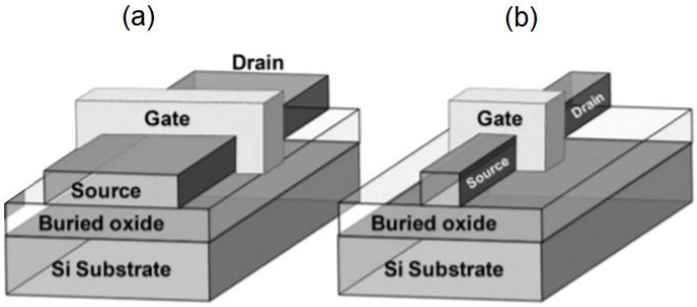

Figure 1.5: (a) Single-gate SOI MOSFET, (b) Double-gate (or trigate) SOI MOSFET [2].

The BOX layer in SOI MOSFETs can basically eliminate the parasitic elements which were experienced in the bulk-silicon MOSFETs. For example, in a bulk CMOS design aiming at low power consumption,the leakage current and S/D capacitance elements can degrade the device performance. But, in SOI technology, the active layer is naturally separated from the bulk substrate by the BOX. Consequently, the junction leakage and capacitance are minimized thanks to the basic SOI structure.

A shallow junction is naturally obtained in the SOI structure by adjusting the thickness of the top silicon film. This is also helpful in reducing SCEs. The absence of vertical S/D junctions yields a substantial reduction of the parasitic elements between the substrate and the source and drain. This can lower RC-delay time and power consumption. Thus, these fundamental benefits can contribute that SOI devices operate much faster and with lower leakage current than bulk CMOS devices.

In the past, several methods for manufacturing SOI wafers were investigated, such as epitaxial lateral overgrowth [10]–[12], zone-melting recrystallization [13]–[15], ion implantation [16]–[18], and wafer bonding [19]–[21]. Among those, we will only mention two types of SOI structure fabrication: Separation by Implanted Oxygen (*SIMOX*) [16], [22]–[25], and the wafer bonding technique [26], [27].

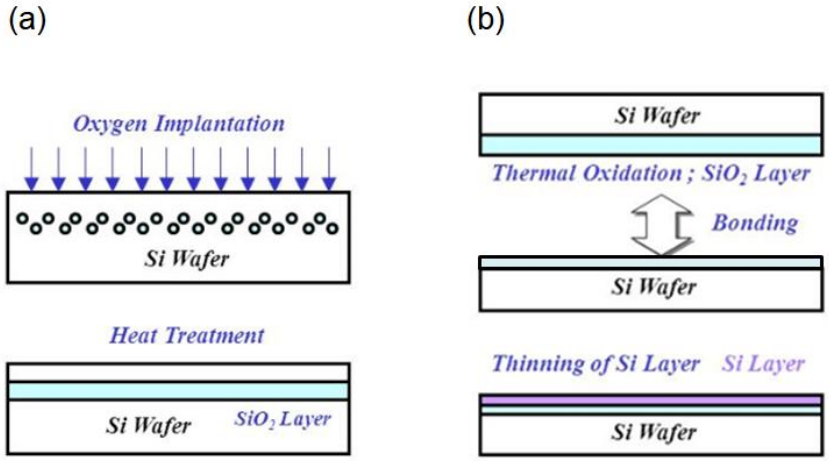

Figure 1.6: Two different techniques to produce SOI wafer: (a) separation by ion implantation of oxygen (SIMOX), (b) direct wafer bonding and etch-back technique.

The essential principle of SIMOX is to use ion implantation technique in order to create a buried SiO_2 layer in the silicon wafer (Figure 1.6a). The deeply implanted oxygen atoms in the silicon wafer oxidize and form the BOX during high temperature annealing process. The wafer bonding and etch-back technique is simpler than other SOI fabrication methods. Two oxidized wafers are naturally bonded, then etched (or polished) down to a target thickness for SOI application. The bonding mechanism is related to hydrophilic surfaces of two oxidized wafers even in room temperature. Since the wafers are bonded at room temperature, thermal annealing is followed in order to strengthen the bonding energy in between the wafers. In the following section, another technique for SOI wafer fabrication method is introduced. This technique turns out to be the most successful at the present time.

1.2.3 SOI Wafer Fabrication: Smart-Cut™ Process

UNIBOND SOI wafers are produced using the Smart-Cut™ process [28]. The key to this process is the combination of ion implantation process and wafer bonding techniques in order to transfer a thin sheet of the semiconductor material onto a dielectric, which becomes the BOX layer. This widely-used technology was invented at the *CEA-LETI* and is now used to produce SOI wafers at the industrial scale. The Smart-Cut™ process has been gradually expanded gradually and is used to produce various types of SOI wafers. The process has been transferred to *SOITEC*, the market leader for SOI wafers.

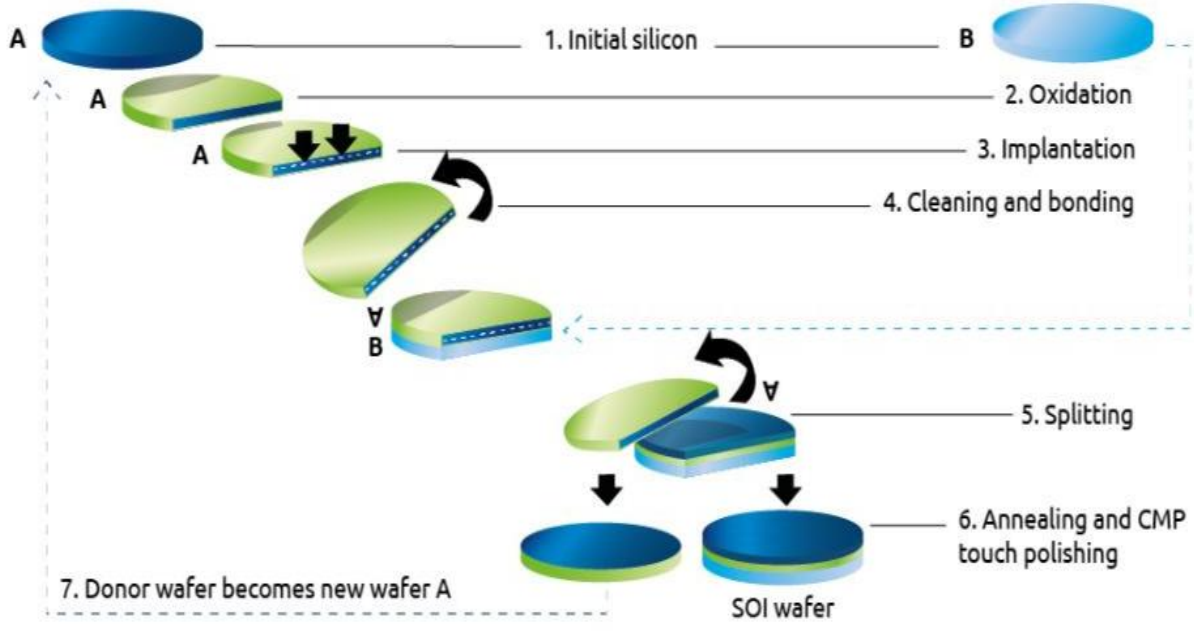

Figure 1.7: Smart-Cut™, an advanced SOI wafer fabrication technique by SOITEC Inc.

The Smart-Cut™ process is illustrated in Figure 1.7 and can be explained as follows:

(i) Two wafers are needed for the Smart-Cut. One wafer 'A' (in Figure 1.6), 'donor' wafer, has been oxidized prior to the hydrogen implantation process. This oxide layer at the top surface will become the BOX. Hydrogen atoms are implanted into the donor wafer at a specific depth for splitting the two wafers later.

(ii) Wafer 'B', called 'handling' wafer, can be either in bare condition or oxidized. The handle wafer plays the important role as a mechanical support for the SOI structure.

(iii) The wafer 'A' is placed onto wafer 'B' in a face-down direction for direct wafer bonding. Two-phase heat treatment is performed. During the first phase, at a temperature of about 500 °C, the donor wafer 'A' splits along a plane defined by the hydrogen implantation range, and the thickest part of wafer 'A' is separated from the bonded wafer structure.. As a result, there are two parts left behind this process: a thin layer of mono-crystalline silicon on oxide on top of the handle wafer 'B' and a remainder of the donor wafer 'A' which can be recycled and be used again as a donor wafer. The second phase of the heat treatment is conducted at a higher temperature for strengthening the bond between the Si/BOX layers and the handling wafer 'B'.

(iv) Finally, a touch-CMP process is carried out to achieve good uniformity of the silicon films. The process can be engineered differently to yield SOI wafers required for specific applications such as RF switches or photonics (Fig. 1.8).

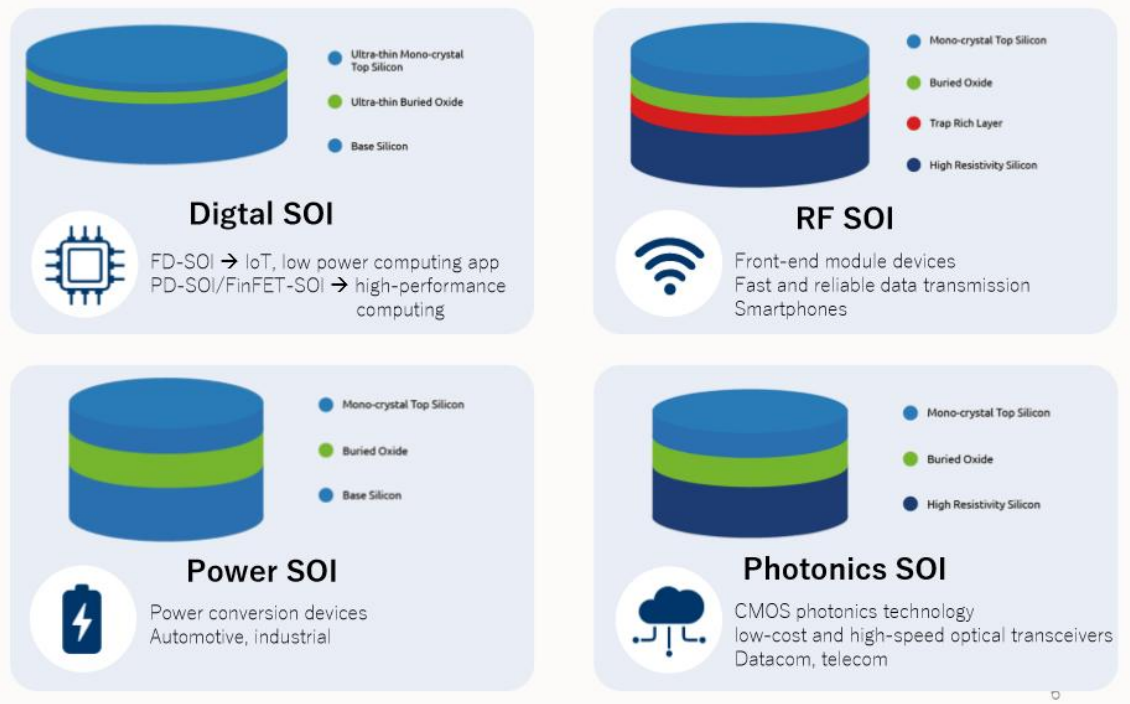

Figure 1.8: Different types of engineered SOI wafer for specified commercialized products: generic CMOS devices, RF circuit and components, power chips, and photonics applications.

1.2.4 Summary

The SOI technology shows substantial potential to overcome the CMOS scaling limit via its unique features. In particular, parasitic elements can be minimized or eliminated. Many parasitic effects found in the bulk silicon devices originate from the interaction between the device and the substrate. In this respect, it is easy to understand that SOI devices are free from the interactions with the supporting substrate thanks to the BOX layer. The SOI substrate allows being robust against the latch-up phenomenon, which is caused in bulk devices by the feedback of the two inherent bipolar transistors.

The *Smart-Cut*^{TM} technique has been established as the mainstream procedure to produce standard and creative SOI wafers. This technology expands progressively into the CMOS industry. It enables to design and fabricate novel multi-gate architectures in order to improve device performance and electrical properties.

1.3 Ultimate Scalability and Flexibility of SOI Devices

Regarding the limitation of photolithography technology, a common issue in the CMOS industry was to obtain a fine pattern from a single exposure step. However, the single exposure was faced the critical problem to shrink device dimension under the 20 nm generation node because of a lack of photolithography process margin: pattern collapse and distortion. In order to solve this issue, multiple-patterning techniques have been proposed and set up. These spacer pattern technique (*SPT*) or double spacer pattern technique (*DSPT or DPT*) make the production cost and process complexities inevitably rise (in Fig. 1.9a), albeit IC chip makers can extend their technology road-map. That rising cost is a tremendous obstacle for the growth rates of IC industries. Meanwhile, the cost competitiveness of a FDSOI technology is expected be lower than the bulk silicon process as we approach the 10 nm generations (Fig. 1.9b). Despite the higher cost of SOI wafers, the FDSOI CMOS technology already begins to compete with the bulk silicon and FinFETs in the total fabrication cost.

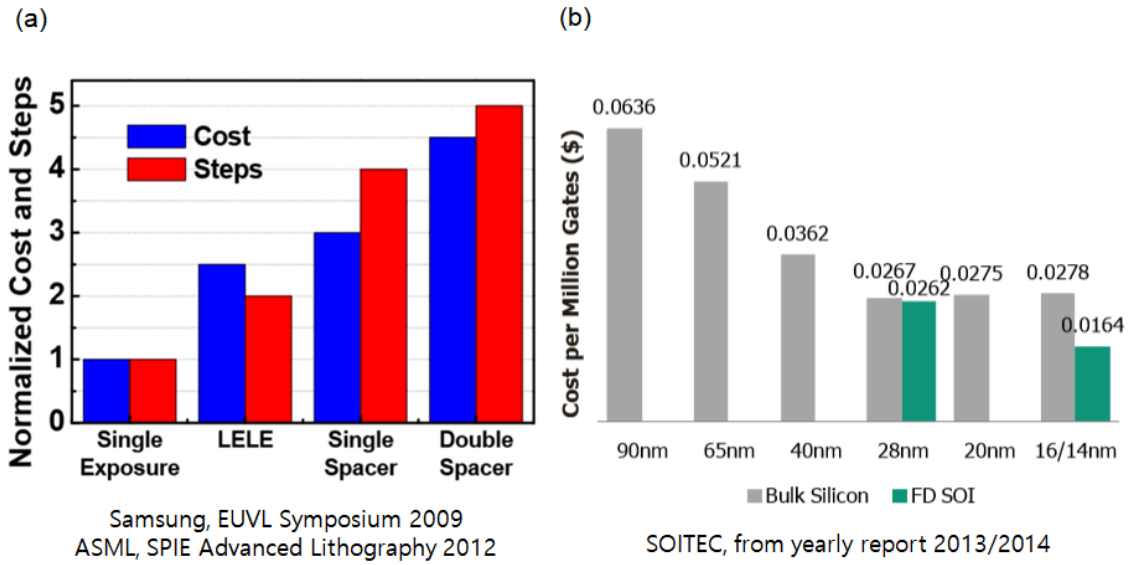

Figure 1.9: (a) Comparison of production cost, depending on different lithography methods. (b) Possible competitiveness of production cost optimization using FDSOI technology.

One should note here that the process flow in FDSOI is much simpler than the bulk silicon process. For designing a simple inverter using the bulk silicon process, twin-well must be defined and kept within the minimum design rules between each well, i.e. N-well and P-well (Fig.1.10a). In contrast, for the FDSOI CMOS inverter, there is no need to form the well to place each type of transistors (Fig. 1.10b).

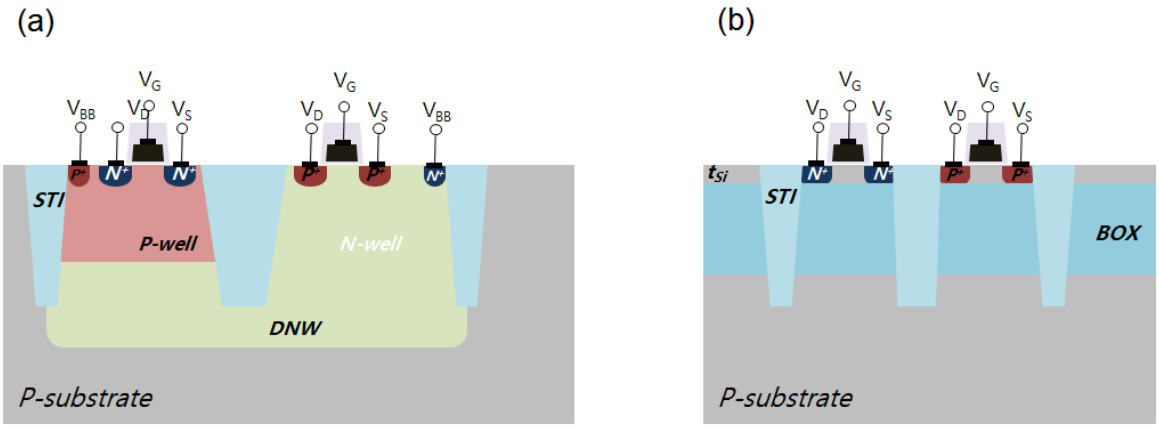

Figure 1.10: Cross-section views of CMOS inverter (a) in the bulk process, and (b) in the FDSOI technology.

In FDSOI devices, the ultrathin active layer for transistors is explicitly determined by oxidation and etching. The source and drain terminals can be made thicker using the selective epitaxial growth, i.e. raised source-drain (*RSD*) technique. To put it differently, SOI devices density is increased over bulk because there are no restricting design rules associated with well formation.. The absence of wells offers area flexibility. This means that FDSOI devices are more efficient than bulk silicon

transistors in terms of integration density.

In the following sub-sections, we describe two different types of SOI devices: the typical planar PD or FDSOI MOSFET with one gate and advanced FDSOI with multi-gate shapes. Afterward, the electrical mechanisms in ultrathin SOI MOSFETs will be discussed: inter-gate coupling, super-coupling effect, and short channel effects.

1.3.1 Planar Partially-Depleted and Fully-Depleted SOI Devices

Thus far, CMOS devices have been designed and fabricated by the bulk silicon technology. The devices are just placed at the top surface of the wafer, reaching a depth of less than approximately 200 nm (0.01% of the wafer thickness). This means that almost all (99.99%) of the remainder silicon serves as a mechanical support and can cause parasitic effects to occur.

In contrast, SOI technology can precisely adjust the necessary thickness of the active areas by Smart-Cut™ process. Basically, the SOI devices can be categorized by the top thickness (t_{Si}) of the silicon film: partially depleted (*PD*) SOI and fully depleted (*FD*) SOI. The difference is that whether or not the space-charge region (or depletion-region) induced by the gate covers the whole silicon body. The formation of the depletion region and its depth are crucial factors to eliminate the floating body effects (*FBEs*) and improve the electrical properties in SOI MOSFETs. For simplicity, there are two types of SOI devices described by the energy band diagram shown in Figure 1.11.

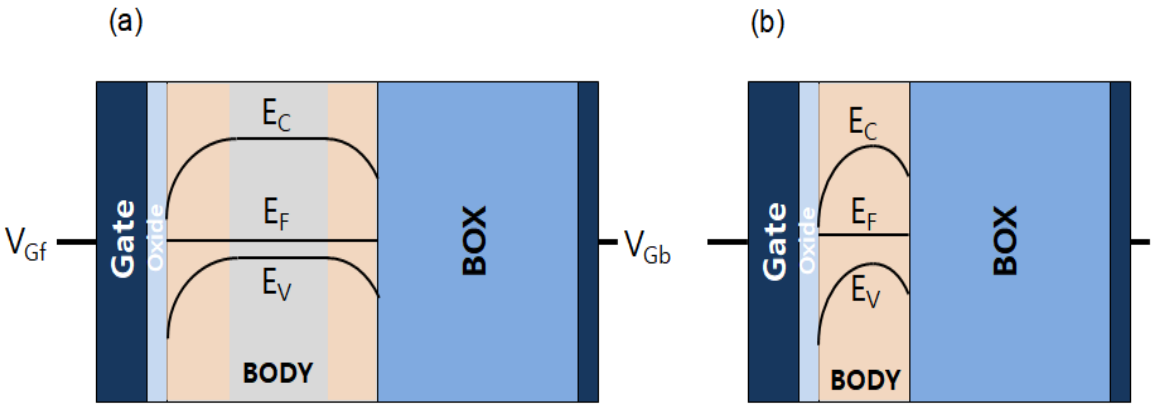

Figure 1.11: Energy band diagrams for (a) partially- (b) fully-depleted n-MOSFET devices, operated in strong inversion condition beyond the threshold voltage. The highlighted regions in the body show the depleted regions induced by the front- and back-gate biases, which inhibit the presence of majority carriers. In this diagram, the back interfaces is about to reach the condition of weak inversion.

The band bending commands the majority carrier (holes) to stay away from the interface between the silicon film and the gate oxide or BOX. The depletion region is proportional to the

positive gate bias, thereby reflecting the surface potential (φ_s) variation. The depth of the depletion region is given by a simple formula derived from the Poisson's equation:

$$W_{depletion} = \sqrt{\frac{2\varepsilon_{Si}\varphi_S}{qN_{A,D}}} \tag{1.1}$$

where φ_s indicates the surface potential at the front interface and the doping levels for n- or p-MOSFET is N_A or N_D, respectively. The maximum depletion width, $W_{d\,max}$, is reached at threshold voltage; where $\varphi_S = 2\,\varphi_F$:

$$W_{d\,max} = \sqrt{\frac{4\varepsilon_{Si}\varphi_F}{qN_{A,\,D}}} \tag{1.2}$$

where the bulk Fermi potential is $\varphi_F = \frac{kT}{q}\ln\left(\frac{N_{A,D}}{n_i}\right)$.

If the silicon body is much thicker than the maximum depletion width ($W_{d\,max}$), a neutral region subsists underneath the front depletion region. The name of partially depleted (*PD*) MOSFET is originated from this neutral region (Fig.1.10a). The neutral region can be connected to an external terminal via a P^+ body contact (assuming an n-channel transistor). Through this connection, the body potential variation can be monitored and correlated with the onset of the floating body effects. This measurement is utilized in chapter 2 and elaborated in detail in chapter 3.

For a thin-film SOI device (Fig. 1.10b), however, the silicon film is thinner than the maximum depletion width ($W_{d\,max}$). This means that the depletion width covers the entire volume of the silicon body, thereby expelling out all majority carrier (holes). These devices, called FDSOI MOSFETs, are considered to be free of floating body effects because there is no longer a neutral region where the holes can accumulate in. In order to verify this postulate, we experimentally scrutinize the floating body effects such as kink effect, PBT, Gate-induced FBE, sharp-switching characteristics, transient effect, Meta-Stable-Dip (*MSD*) effect, and super-coupling effect in chapter 2 and chapter 4.

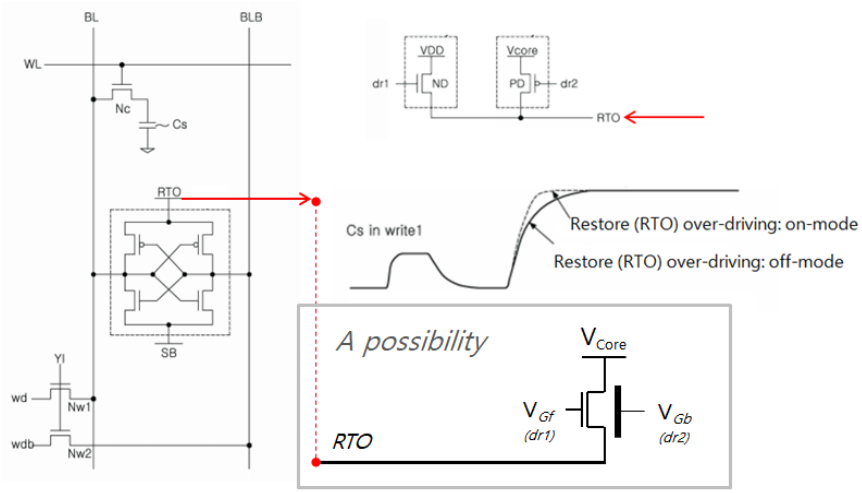

Figure 1.12: A possibility: an FDSOI over-drive for current boosting during writing mode in DRAM.

From a pragmatic point of view, the FDSOI MOSFETs with depleted back interface have attractive features such as superior short-channel behavior, boosted current characteristics, and low subthreshold slope. These unique electrical properties can be taken into account for the analog circuit design. In current over-driving mode, for example, one FDSOI driver can be used instead of two transistors as depicted in the grey box (Fig. 1.12). In this case, a RTO driver needs to boost the current gain quickly while a selected cell capacitor is written for high state '1'. Generally, a conventional DRAM consists of two pull-up drivers to control the over-driving mod. They operate one by one via synchronized signals. For the FDSOI driver, the current can be controlled by the interaction of two gates independently.

1.3.2 Multi Gate FDSOI Devices

Typical SOI MOSFETs consist of two gate electrodes: one is the top gate with the thin gate oxide and the other is the bottom gate underneath the BOX layer. The top gate is used to manage the current conduction and the bottom gate to control the threshold voltage. The back channel conduction is unsuitable for normal operation. It is necessary to maintain a certain condition of depletion or accumulation at the back interface in order to benefit from the coupling effect. This inter-gate coupling allows enhancing the device characteristics. The body factor '*n*' is derived from the subthreshold swing as expressed below:

$$SS = \mathrm{n} \cdot \frac{K_B \cdot \mathrm{T}}{|\mathrm{q}|} \ln(10) = \boldsymbol{n} \cdot 59.6 \cdot \frac{\mathrm{T}}{300\ \mathrm{K}}\ \mathrm{mV/dec}, \tag{1.3}$$

where K_B is Boltzmann's constant, T is the temperature, and q is the charge of an electron. The body factor indicates how efficiently the gate controls the channel region in terms of electrostatics and is associated with the electrostatic coupling effect between the gate and the channel. The body factor is generally n = 1.2 ~1.5 in bulk silicon devices and n = 1.05 ~ 1.11 in FDSOI devices [29]. The theoretical lowest value $n=1$ corresponds to ideal characteristics of devices. This low value is not always attained in FDSOI because of the capacitance mismatch between the front gate oxide and the BOX. The concept of the symmetric double-gate SOI MOSFET was proposed to solve this issue: the two gate electrodes have the same thickness of gate oxide as depicted in Figure 1.13a. The left- (or front) and right-gate (or back) are tied together physically, and therefore induce the same electric field, but in opposite directions, into the silicon body via the gate oxide. The total electric field is lower which enables higher mobility and volume inversion (or bulk inversion) effect [30].

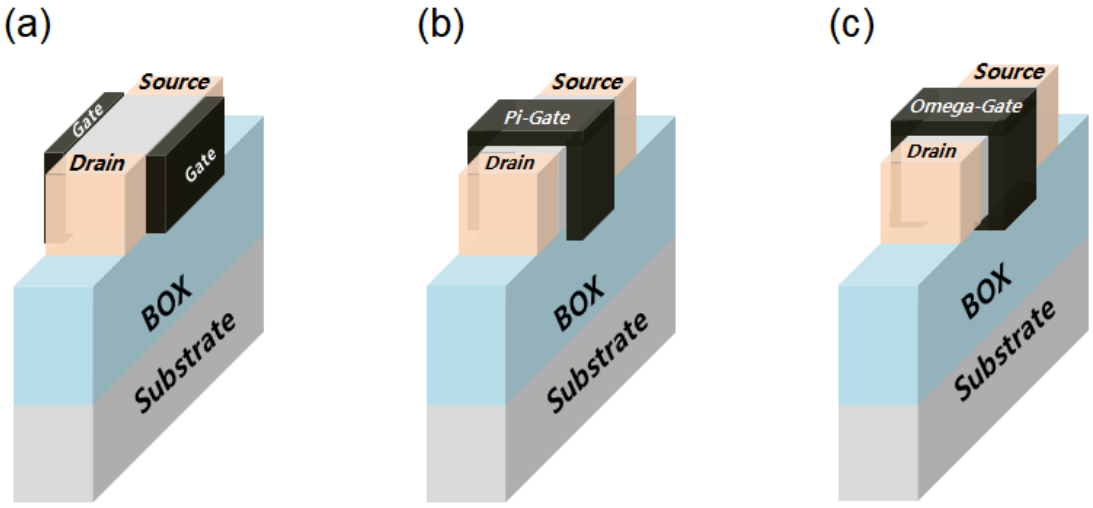

Figure 1.13: Different types of the multi-gate SOI MOSFET distinguished by the gate configuration: (a) double gate, (b) Pi(Π) gate (likewise the tri-gate Fin-FET), and (c) Omega(Ω)-gate.

Among many cases, there are two best-suited multi-gate architectures: the channel region is partially covered with the gate material (Fig. 1.13b; *tri-gate or Π-gate*) or almost surrounded by the gate electrode (Fig. 1.13c; Omega-gate). The capacitive coupling between the gate electrode and the channel region governs the electrostatic behavior. To put it differently, a better electrostatic controllability of the channel region can be achieved by increasing the influence from the gate. The simplest way is to enlarge the area of the gate region (wrapped sides). It can also be accomplished by reducing the cross section of the channel region, i.e. film height and width. Accordingly, an improved multi-gate SOI MOSFET would look like a nanowire device.

That is why chip makers have considered switching from the bulk silicon technology to more advanced CMOS architecture: FinFET or FDSOI. The FDSOI and the family of multi-gate MOSFETs are unavoidable for low power and RF applications in the CMOS industry.

1.3.3 Ultrathin Body and BOX (UTBB) MOSFETs

The presence of an ultrathin body and BOX (*UTBB*) is used to control the SCE more effectively in nanoscale FDSOI MOSFETs. For a thinner BOX layer formed under the silicon body, a more precise channel controllability can be achieved as illustrated in Figure 1.14. The channel control depends on the electrostatic influence from the front- and back-gate in FDSOI MOSFETs. A thinner BOX enhances the action of the back gate. The two gates compete and interfere with each other in order to govern the channel region: the inter-gate coupling effect. The fundamental inter-gate coupling effect in a floating body FDSOI MOSFET was first modeled by *Lim and Fossum* [6].

In the following sections, the typical implications of the coupling effect are summarized. In addition, the extreme case of the inter-gate coupling named super-coupling effect is explained in ultrathin FDSOI MOSFETs.

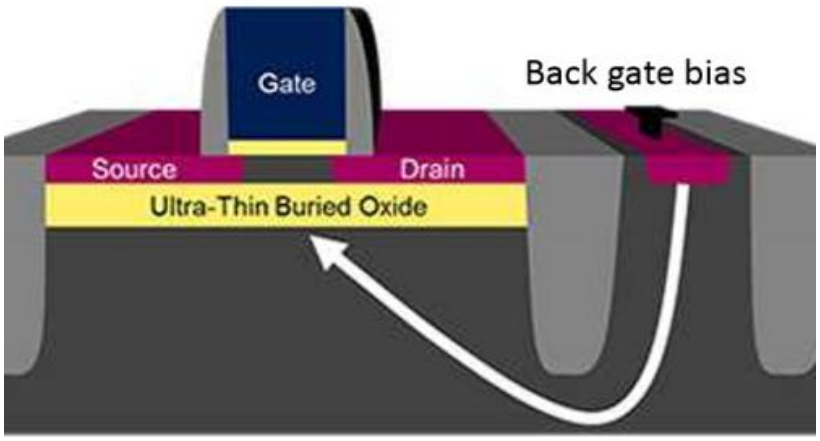

Figure 1.14: UTBB FDSOI MOSFET with back-bias applied via a P+ contact.

1.3.3.1 Inter-Gate Coupling Effect: Typical Coupling Mechanism

One of the innate features in SOI MOSFETs is that electrical properties of the channel region are influenced by the completion between the front gate and the back gate bias. In a relatively thick silicon body, *i.e.*, PDSOI MOSFETs, the front- and back-interface can be triggered independently and contribute simultaneously to the channel conduction. This means that each channel is mutually exclusive and does not affect the opposite channel. Conversely, for FDSOI MOSFETs, the inter-gate coupling mixes the contributions of each interface. Note that since the front interface is prevailing due to a relatively thin gate oxide, the back interface acts as a virtually linked component. This can be possibly analyzed via the body potential variation. This practical approach is dealt with in the following chapter 3. The general main consequences of the inter-gate coupling are described below:

- Tuning threshold voltage via the opposite interface contribution.
- Boosting current conduction with trimming the interaction of the two gate biases.
- Adjusting transconductance and field-effect mobility (in chapter 2).
- Designing innovative devices featuring steep switching characteristics (in chapter 4).
- Mitigating SCE in UTBB MOSFETs.

To begin with, we remind how one interface can change the threshold voltage of the other side base on the model established by Lim and Fossum [6]. The model explains the variation of the front-channel threshold voltage versus back-gate bias, represented in Figure 1.15. There are three obvious domains. For depletion of the back interface, there is a linear change of the threshold voltage. This case is extremely important for the design of low-power circuits. Although this model assumes several conditions (long channel, low drain bias, constant doping profile, no quantum effect), it has been proven by exhaustive measurement to be valid and useful.

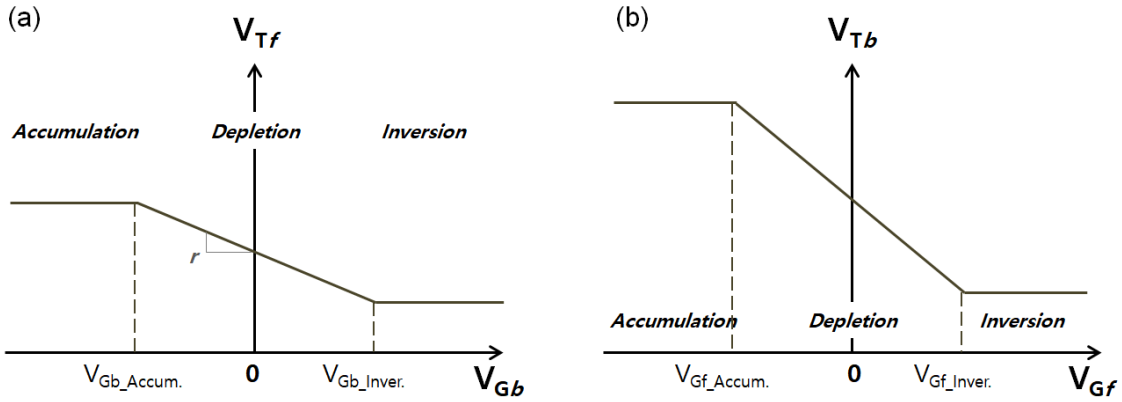

Figure 1.15: The classical inter-gate coupling model proposed by Lim and Fossum for (a) front- and (b) back-interface threshold voltage. Three distinct domains can be indicated, depending on the opposite interface conditions: accumulation, depletion, and inversion, respectively.

The standard definition of front-channel threshold voltage, V_{Tf}, implies that $\phi_{sf} = 2\,\phi_F$ (Lim and Fossum used the Fermi level as the potential reference [6], [9]). The relationship between gate voltage and surface potentials are given by Equation (1.4):

$$V_{Tf,b} = \phi_{Sf,b} + \phi_{oxf,b} + \phi_{msf,b} \tag{1.4}$$

where $\phi_{msf,b}$ are metal-semiconductor work functions. The front-gate voltage is given by Equation 1.5:

$$V_{Gf,b} = \phi_{FBf,b} + \phi_{Sf,b}\left(1 + \frac{C_{Si\_} + C_{itf,b}}{C_{oxf,b}}\right) - \phi_{Sb,f}\frac{C_{Si}}{C_{oxf,b}} - \frac{2Q_{cf,b} + Q_{Si}}{2\,C_{oxf,b}} \,. \tag{1.5}$$

Equation 1.5 is obtained for the front-gate voltage.

Case 1: Back-interface accumulated ($\phi_{sb} = 0$)

Since the back surface potential is pinned to zero, i.e. $\phi_{sb} = 0$, the front-gate threshold voltage V_{Tf} becomes independent as depicted in Figure 1.15. The value is given by Equation 1.6.

$$V_{Tf\_acc} = \phi_{FBf} + (1 + \frac{C_{Si} + C_{it\_f}}{C_{oxf}}) \cdot 2\phi_F - \frac{Q_{Si}}{2\,C_{oxf}}$$

(1.6) [31].

Case 2: Back-interface depleted (and $0 < \phi_{sb} < 2\phi_F$)

As soon as the back interface is depleted, the V_{Tf} begins to decrease more for positive V_{Gb} as described by Equation 1.7:

$$V_{Tf\_dep} = V_{Tf\_acc} - \frac{C_{Si} \cdot C_{BOX}}{C_{oxf} \cdot (C_{BOX} + C_{Si} + C_{it\_BOX})} (V_{Gb} - V_{Gb\_acc})$$

(1.7) [31].

V_{Gb_acc} represents the limiting voltage below which the back interface is accumulated whatever V_{Gf} values are. V_{Gb_acc} is given by Equation 1.8:

$$V_{Gb\_acc} = \phi_{FBb} - \frac{C_{Si}}{C_{BOX}} \cdot 2\phi_F - \frac{Q_{Si}}{2\,C_{BOX}}$$

(1.8) [31].

Case 3: Back-interface inverted ($\phi_{sb} = 2\phi_F$)

In the end, the back interface is completely inverted and then the V_{Tf} again reach a saturation region independent on the back gate bias. The V_{Tf} is given by Equation 1.9:

$$V_{Tf\_inv} = \phi_{FBf} + (1 + \frac{C_{it\_f}}{C_{oxf}}) \cdot 2\phi_F - \frac{Q_{Si}}{2\,C_{oxf}}$$

(1.9) [31].

1.3.3.2 Super-Coupling Effect

The critical case of inter-gate coupling is called “super-coupling” effect [32]. The super-

coupling effect dictates that only one type of mobile carriers can be accommodated in an ultrathin silicon body. The limit for the silicon thickness where the supercoupling is revealed or not is known as critical thickness, t_{Si}* [6], [30], [33]. If the silicon film thickness (t_{Si}) is thinner than the critical thickness, *i.e.* $t_{Si} < t_{Si}$*, the potential drop across the body is insufficient to sustain both carriers simultaneously. Namely, the body acts like a quasi-rigid potential well where one of the gates prevails. Figure 1.16 shows thick-body and ultrathin body SOI transistors. For the thick-body device (Fig. 1.16a), electrons and holes can co-exist in the body. However, for ultrathin device, the supercoupling inhibits the presence of both carriers.

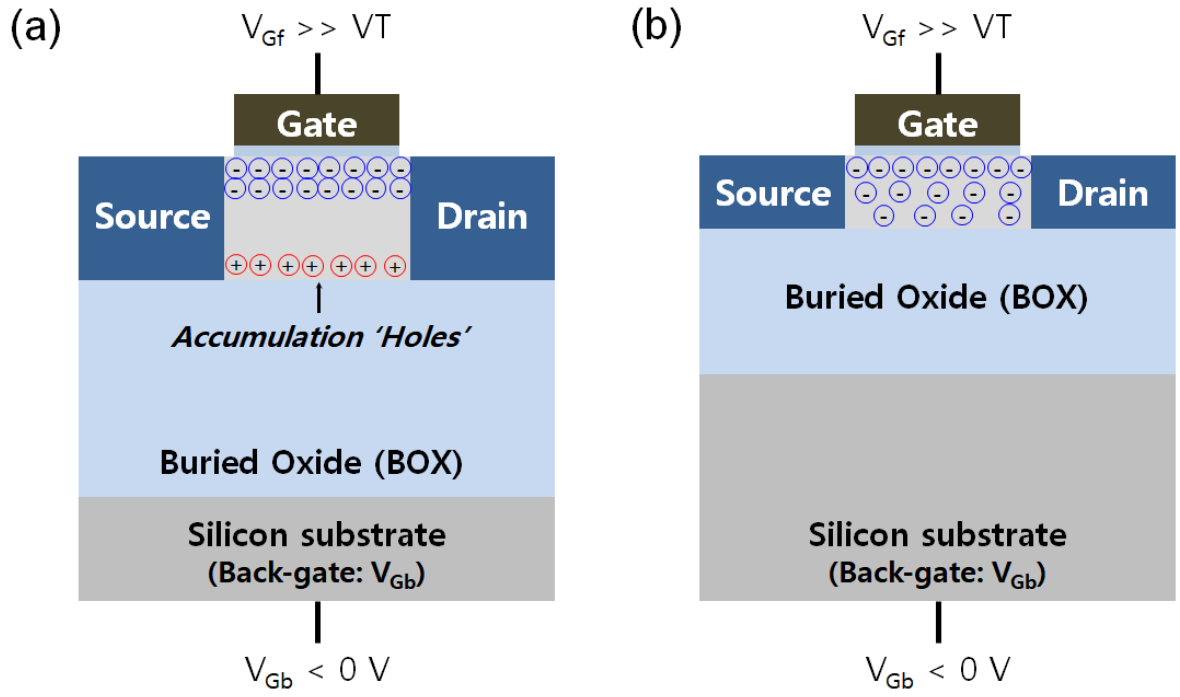

Figure 1.16: Cross-section views showing (a) thick and (b) ultrathin FDSOI MOSFETs with negative V_{Gb}

This implies that the dominant gate governs the whole silicon body (volume inversion as accumulation): Not only the front channel but also the back channel tend to follow the regime of operation imposed by the front gate, instead of being independent (Fig. 1.16b). The hole accumulation layer disappears in ultrathin body due to super-coupling effect.

The supercoupling is an intrinsic size effect, occurring typically for body thickness in the sub-10nm range. Technology parameters (gate stack, BOX thickness) and biases can only modify the critical thickness t_{Si}* without questioning the fundamental nature of supercoupling [33]. Figure 1.17a shows three curves, showing experimental evidence of 1D supercoupling as a function of silicon film thickness. For thicker devices (t_{Si} > 25 nm), there are plateau regions where the front-gate threshold voltage is independent at the negative back-gate voltage. This saturated region can be attributed to the

holes populations at the back-channel. The accumulated holes layer screens the impact of the back-gate bias into the front-channel.

However, for the ultrathin body (t_{Si} = 7.8 nm), the plateau is no longer visible (t_{Si}* = 9.6 nm > t_{Si} at V_{Gb} = -7 V) [33].

Figure 1.17b presents the role of gate length. For long channel device (1 μm), the flat region in accumulation is observed around V_{Gb} = -5 V. This region disappears in shorter channels where the super-coupling effect becomes stronger and 2-dimensional. The practical consequence is that the range of V_{Tf} tuning is extended.

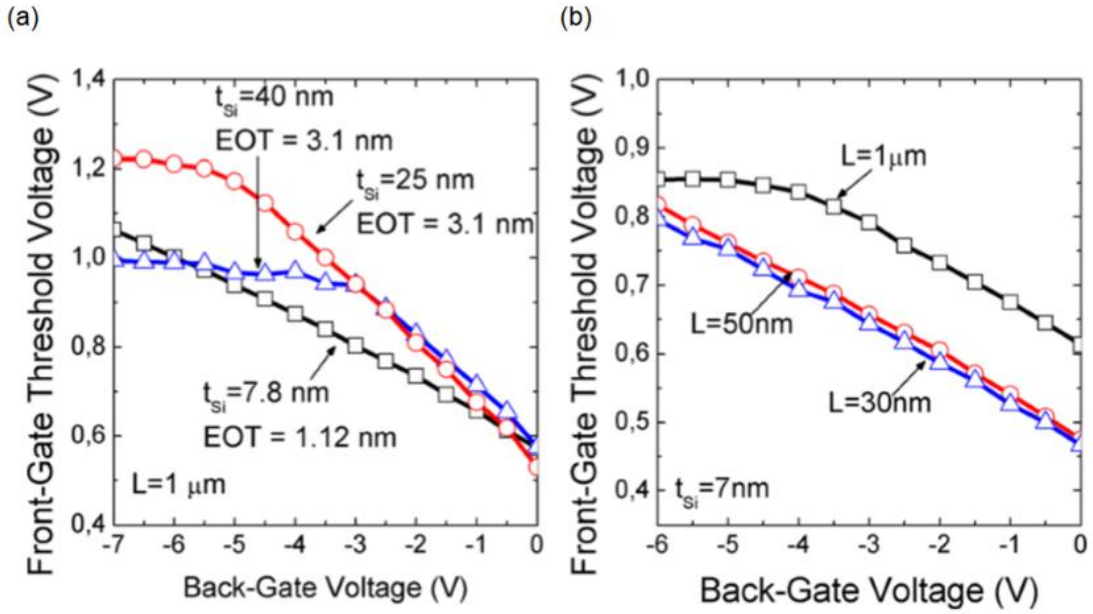

Figure 1.17: Experimental variation of front-gate threshold voltage versus back-gate bias, showing impact of (a) silicon thicknesses and (b) gate lengths. L = 1 μm, t_{BOX} = 25 nm, $N_A = 10^{15}$ cm4 V_D = 0.02 V [33].

A. Critical Si-Film Thickness (t_{Si}*)

The t_{Si}* is the minimum body thickness where both a front-inversion channel and a back-accumulation simultaneously co-exist. Eminente et al. showed the analytical 1-D expression for the critical thickness is given by Equation 1.11 [30]:

$$t_{Si}^{*} = \frac{k_B \cdot T \varepsilon_{Si}}{q \cdot C_{BOX}\left(V_{FB_{Gb}} - V_{Gb}\right)} \ln\left[\frac{N_A \cdot C_{OX} \cdot C_{BOX}\left(V_{FB_{Gb}} - V_{Gb}\right)}{q \cdot \varepsilon_{Si} \cdot n_i^2}\right]. \quad (1.11)$$

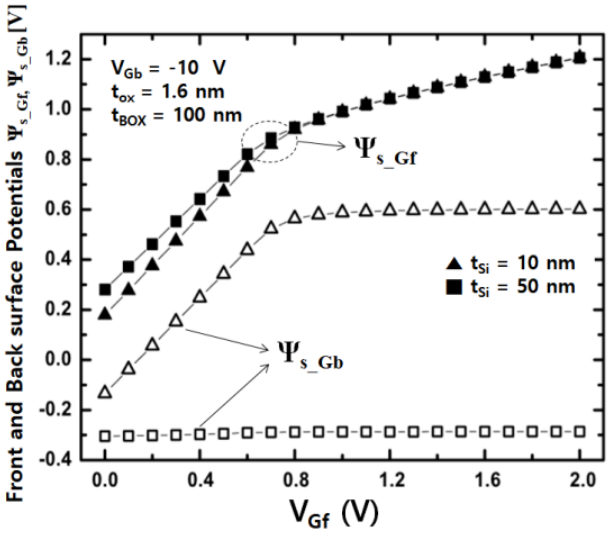

Figure 1.18: Surface potential as a function of the front-gate bias for thick- and thin-silicon body [30]. *For the ultrathin device (triangle shape), the back-surface potential follows the front-surface potential because of the supercoupling effect.* V_{Gb} *= -10 V,* t_{OX} *= 1.6 nm,* t_{BOX} *= 100 nm.*

In FDSOI MOSFETs with sub-critical thickness, the potential variation across the silicon body is not strong enough to induce large concentrations of electrons and holes at opposite interfaces. Figure 1.18 shows surface potential variation at the front- and back-interface versus the front-gate bias. For the thick film (t_{Si} = 50 nm), the front-surface potential (Ψ_{s_Gf}) is varied with the front-gate bias but the back-surface potential (Ψ_{s_Gb}) is unchanged. In contrast, for thin film (t_{Si} = 10 nm), while the front-surface potential is increased, the back-surface potential follows due to the inter-gate coupling. This indicates that the back-channel is strongly associated with the front-gate bias, leading to 'volume' inversion. In this respect, we scrutinize the body potential variation in FDSOI MOSFETs. It was measured directly in quasi-steady-state condition using the *P*+ body contact of n-MOSFETs. The body potential variation, which is the main topic of Chapter 3, provides new experimental evidence of the super-coupling effect in ultrathin FDSOI MOSFETs.

B. Threshold Voltage Coupling

The supercoupling effect is examined by evaluation the threshold voltage variation with the back-gate bias. Figure 1.19 shows the simulated results, depending on several film thicknesses from 10 nm to 5 nm. For t_{Si} = 10 nm film (Fig. 1.19a), the front threshold voltage (V_{Tf}) varies from 2 V to -5 V and then it saturates beyond the V_{Gb} = -5 V. A plateau region is observed because of the presence of an accumulation holes layer at the back-interface; i.e. inter-gate coupling stops.

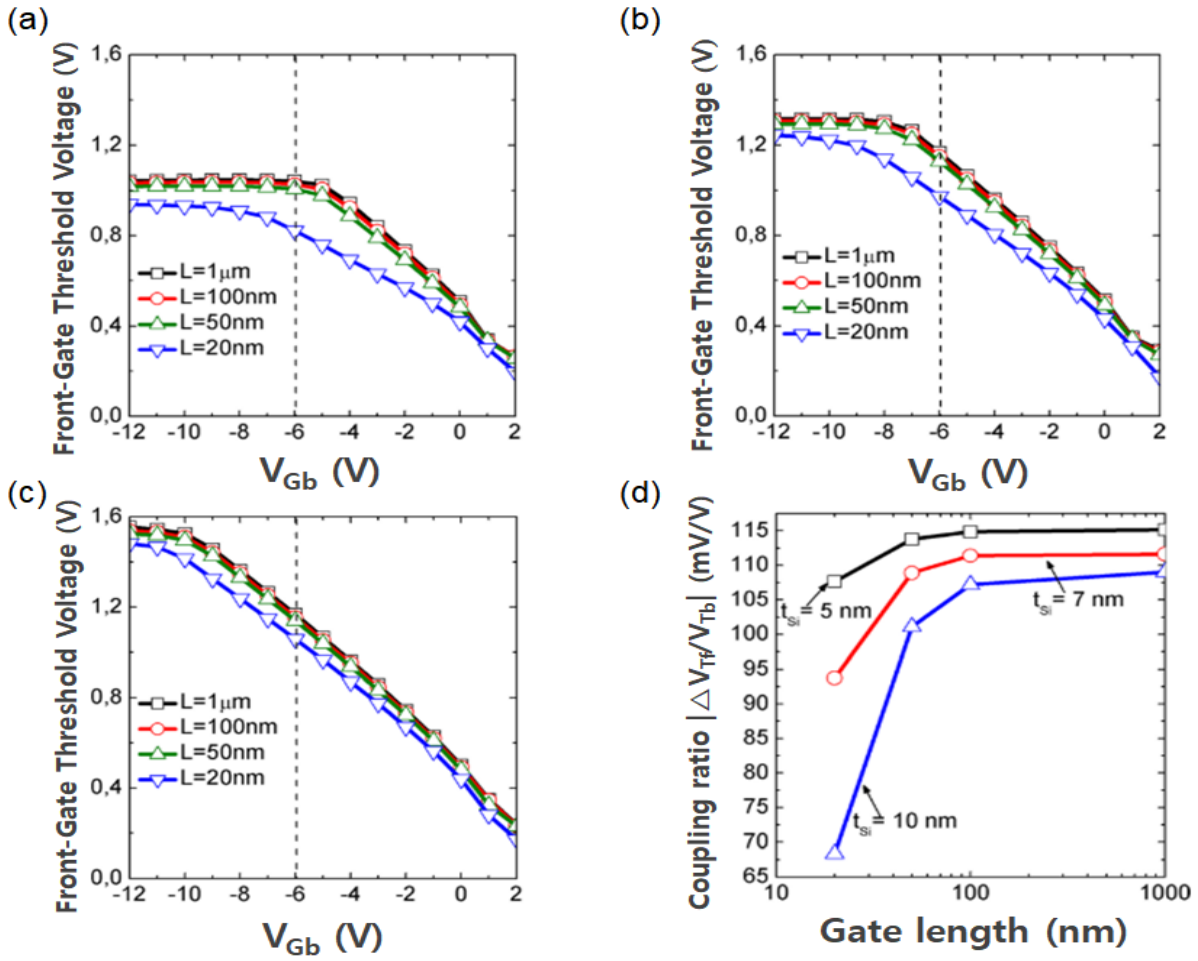

Figure 1.19: Front-gate threshold voltage coupling curves for variable SOI thickness, (a) t_{Si} = 10 nm, (b) t_{Si} = 7 nm, and (c) t_{Si} = 5 nm. (d) The coupling coefficient extracted from the maximum slope in the decreasing threshold voltage region. t_{OX} = 1 nm, t_{BOX} = 10 nm, V_D = 0.02 V, and V_{Gf} = 1 V [33].

The plateau appears for V_{Gb} more negative in thinner silicon films as demonstrated in Figure 1.19b, c. The enhancement of electrostatic control is accomplished by thinning the silicon thickness. For a short channel device (L_G = 20 nm) on t_{Si} = 10 nm (Fig. 1.19a), this curve deviates from the long channel coupling curves, due to the SCE. In an ultrathin body (t_{Si} = 5 nm), however, the lateral encroachment from drain is well controlled. The saturation region tends to disappear, therefore reducing the SCE [7]. In a practical point of view, the back-gate control can be applicable even for voltages lower than -6 V in the ultrathin body (< 10 nm) and BOX (> 10 nm).

Figure 1.19d shows the front body factor (or front-to-back gate coupling ratio) versus the gate length. When the body thickness is much thinner than the gate length (L_G), the gate coupling ratio is very high and shows little variation with L_G. This implies that the front-gate bias is stronger thanks to the thinner body. In thicker films, the SCEs make the coupling coefficient to decrease dramatically.

1.3.3.3 Short channel Effects in FDSOI

In modern electronic industries based on VLSI circuits, the device scaling is the most substantial factor to enhance device performances such as high-speed operation, low-power consumption, and increasing integration density. To achieve all of that, the critical dimensions of MOSFETs have to be shrunk physically. Reducing the channel length is a simple way to meet the requirement but the short-channel effects (*SCE*) must be considered completely. The performances of MOSFET devices are related to the electrostatic control of the channel by the gate.

In general, for the nanoscale VLSI circuit design, the effective channel length influences the device characteristics related to the SCEs such as subthreshold slope degradation and drain-induced barrier lowering (*DIBL*). It is obvious that the SCEs are originated by the encroachment of the electric field from the terminals, i.e. source and drain, into the effective channel region underneath the gate. This encroachment leads to competition for the control of the available depletion area underneath the gate, thereby decreasing the threshold voltage. When the drain voltage is high enough, the surface potential in the channel and inversion electrons are no longer controlled by the gate bias. The lateral depletion width (W_d) of source and drain is given by Equation 1.12 [2] with source bias (V_S), drain bias (V_D), and built-in potential barrier (V_{bi}):

$$W_{d\_S,D} = \sqrt{\frac{2 \cdot \varepsilon_{Si} \cdot N_D (V_{bi} + V_{S,D})}{q \cdot N_A (N_D + N_A)}}. \tag{1.12}$$

No matter what novel technologies are used for device integration, this depletion width has to be minimized. Less influence from the lateral encroachment yields good immunity against the main SCE: threshold voltage roll-off (due to shared depletion charges) and drain induced barrier lowering (*DIBL*).

In FDSOI MOSFETs, especially, the SCE is inherently mitigated by the shallow silicon thickness but it is not perfectly diminished due to the source and drain electric field, *i.e.* 2-D effects [1], [7], [30], [33]. The latter matter thus has to be considered and solved even for ultrathin FDSOI MOSFETs. Regarding the reduction of the SCE, a viable approach is used to the multi-gate architectures discussed in section 1.2.2.

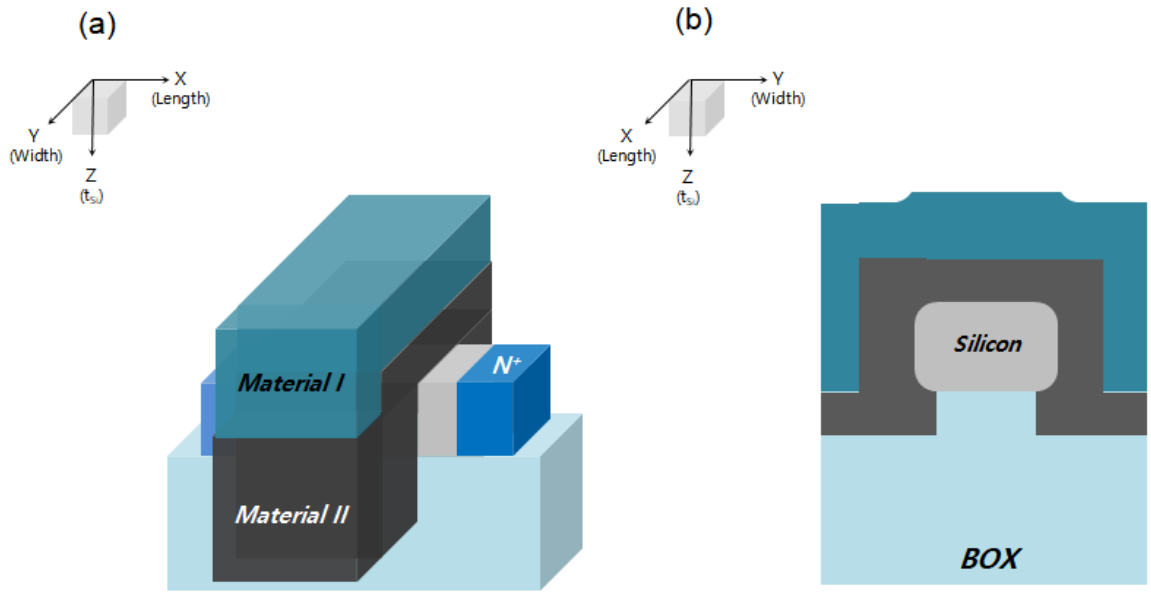

Figure 1.20: (a) Pi (Π) gate or (b) Omega (Ω)-gate shape can reduce the SCEs because the surrounding gate dominates, attenuating the contribution of the electric field from the source and drain into the channel region.

In case of FDSOI MOSFETs, very thin body and BOX are helpful to attenuate the SCE by increasing the electrostatic control. In order to be immune from the SCE, the depletion width (Equation 1.12) and natural length (Equation 1.13) should be at least six-times [7] to one order [34] of magnitude smaller than the gate length. The natural length is defined by the extension of the electric field lines from the source and drain into the channel region. It is given by the general expression:

$$\lambda_n = \sqrt{\frac{\varepsilon_{Si}}{n \cdot \varepsilon_{ox}}\left(1 + \frac{\varepsilon_{ox}}{4\varepsilon_{Si}}\frac{t_{Si}}{t_{ox}}\right) t_{Si} \cdot t_{ox}}. \quad (1.13)$$

The effective number of gates, denoted '*n*', corresponds to 1, 2, 3, or 4 for a single- [35], double- [36], triple- [37], and quadruple-gate devices [29]. In particular, the '*n*' can be extended to Π-gate and *Ω*-gate devices albeit a non-integer value of n ranging between 3 and 4 [38], [39].

In multi-gate MOSFETs (Fig. 1.21), the silicon body is more or less surrounded by the gate material. This means that the electric field on the many-sides of the gate can control the channel conduction until forming the inversion layer, electrons in a case of n-MOSFET, at the surface.

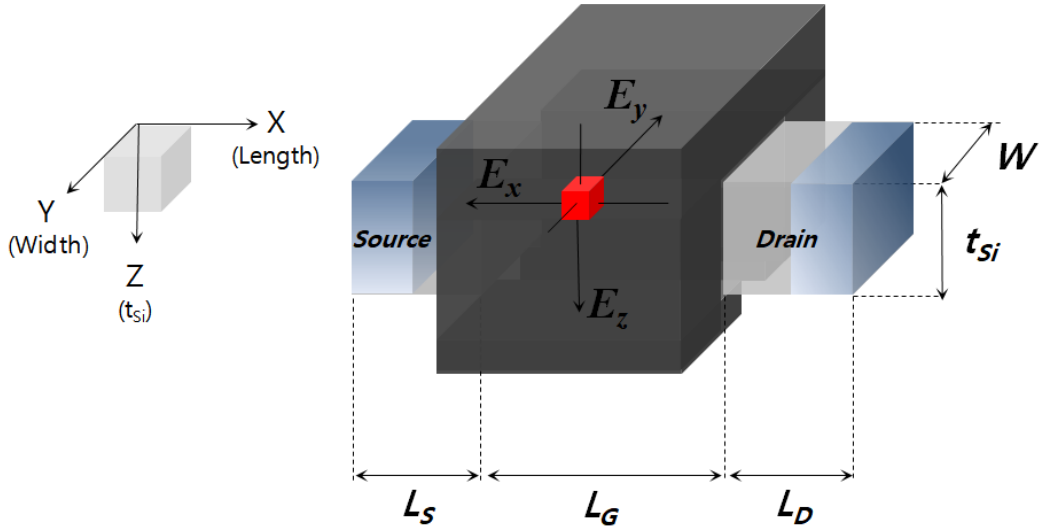

Figure 1.21: Electric field elements depicted in rectangular coordinate system.

Within the spatial potential distribution in the channel region, the x-direction electric field (E_x) term is reduced by the other components (E_y, E_z) in Figure 1.21. The ultimate target is to eliminate the influence of the x-direction that causes short channel effects. Increasing the other components of the electric field countervails the encroachment of the drain bias, therefore enabling shorter transistors to operate correctly.

1.3.4 Compound Semiconductor on Insulator Devices

Semiconductor on Insulator (*SOI*) is a generic term describing the various CMOS applications. Among those, boosting the carrier mobility is a valuable approach to enhance device performance without side effects. This is because current density is proportional to the carrier mobility. There are many possible solutions to get high-mobility channels such as Ge, strained silicon (*SiGe*), and all III-V compounds materials for advanced high-speed devices [40], [41]. Figure 1.22 shows the process flow for III-V-on-Insulator wafers fabricated by *IBM Zurich Research Laboratory*. Direct wafer bonding (*DWB*) is used to prepare large-scale wafers before processing the ultrathin III-V-OI devices.

The III-V compound semiconductors are now taken into account for mainstream research in order to extend the CMOS technology roadmap beyond the 14 nm node. In particular, it is envisioned that $In_{(x)}Ga_{(1-x)}As_{(x \geq 0.53)}$ n-MOSFETs will be coupled to (Si)Ge p-MOSFETs to deliver an optimum electron/hole performance while leveraging the wide industry experience with SiGe. The potential benefits of InGaAs-based nMOSFETs have already been demonstrated [42]–[45].

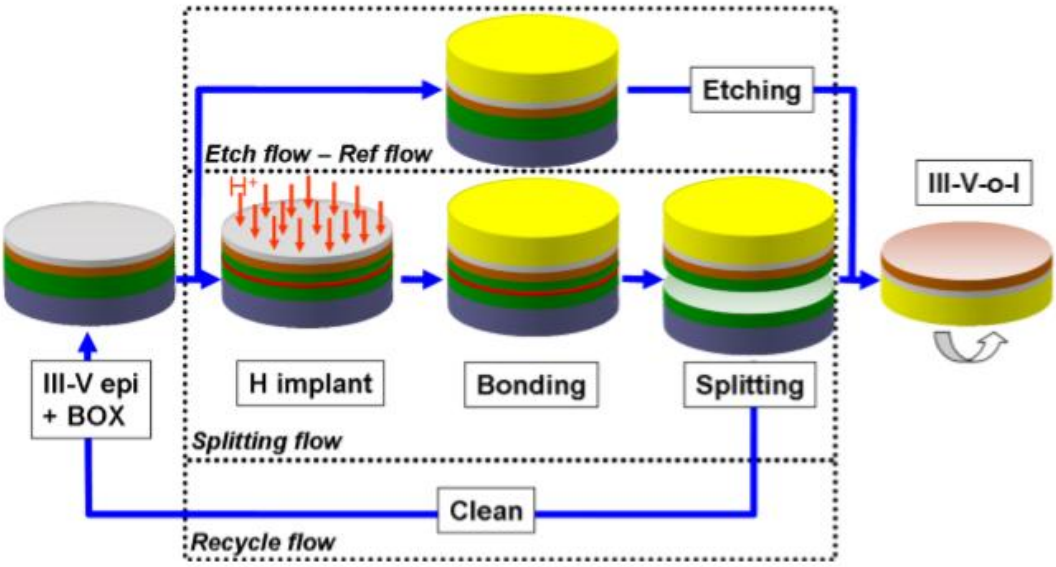

Figure 1.22: Process flow of III-V-on-Insulator wafer fabrication fully compatible with VLSI standards using Direct wafer bonding (DWB), hydrogen implantation, thermal splitting, selective etching, and reusing the InP donor wafer [46].

In chapter 4, InGaAs-On-Insulator MOSFETs are demonstrated in terms of device fabrication, and typical characterizations.

1.3. Conclusion

Thus far, the bulk silicon technology has been flourishing by the down-sizing strategy, i.e. device scaling. However, the "*happy scaling*" period is now terminated because of the poor electrostatic control of the channel by the gate in ultra-short devices and complexity of the device fabrication. Device scaling becomes the most critical concern of the CMOS industry in terms of reducing production cost and achieving high device performance. With its superior short-channel effect control, the FDSOI technology stands as an attractive and realistic option instead of the silicon process for the semiconductor industry. In particular, several types of SOI wafer and SOI devices enable easily implemented commercial products: RF IoT and low-voltage devices, aerospace components, solar application. Thinning the transistor body is crucial for dealing with the short channel effects. In such ultrathin transistors, the coupling and super-coupling mechanisms are emphasized opening new sources for circuit design. Newly suggested architectures, i.e. multi-gate FDSOI devices, are also taken into account to enhance the electrostatic dominance of the gate on the

channel region.

Chapter 2 will demonstrate several floating body effects (FBEs) in FDSOI MOSFETs, showing experimental results via multi-angled approaches. The main implication is whether or not the FBEs are still alive in FDSOI MOSFETs.

Chapter 3 will investigate the dynamic body potential variation in non-equilibrium conditions. This enables to inspect the change of the body state during the onset of the FBEs. The results are useful for explaining the steady-state FBEs and for developing several applications.

Chapter 4 will show advanced SOI devices: A lateral junctionless MOSFET based on a InGaAs-on-Insulator structure. In addition, sensor applications are demonstrated using Z^2-FET device.

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Chapter 2

Floating Body Effects in Ultrathin FDSOI MOSFETs

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2.1 Introduction

In MOSFETs with an isolated body, such as SOI devices, multi-gate devices, SOI-FinFET, and nanowire transistor, the majority carriers can give rise to unexpected effects. The majority carrier population in those devices is sometimes difficult to control without the presence of a body contact. Namely, the absence of body contact precludes the majority carrier population for reaching an equilibrium state after specified biasing conditions: when a negative bias applied to the gate of n-MOSFET a supply of holes is required, the generation of which is a relatively slow process. Conversely, getting rid of excess positive charges takes time once the positive gate bias is removed. The excess or deficit of majority carriers, compared with regular operation condition, leads to peculiar mechanisms that carry the generic name of Floating-Body Effects (*FBEs*).

The FBEs have been notorious in partially-depleted (*PD*) SOI devices. One of the well known FBE is the *kink effect*, which has been understood in Silicon On Sapphire (*SOS*) MOSFETs very early on [1]–[3]. The mechanism is that majority carriers generated by impact ionization accumulate into the neutral region of the device, thereby increasing the body potential and lowering the threshold voltage, which suddenly increases drain current. Since then, during the evolution of SOI technology [4], [5], the family of known FBEs has increased in number. They originate not only from impact ionization but also from band-to-band tunneling (*BTBT*), direct tunneling through the gate dielectric, the application of transient biases, and illumination or ionizing radiations. Although the FBEs can provide extra current and boost circuit speed, they are generally viewed as parasitical mechanisms responsible for non-linearity [6]–[12], hysteresis [13]–[16], latch [17]–[19], transient and history effects [20]–[25].

It is commonly believed that FBEs do no longer exist in fully-depleted (*FD*) SOI MOSFETs. The FBEs can be triggered by excess (or deficit) holes in the body, but in FDSOI there is no neutral region where the excess/deficit hole can find place underneath the channel region. Due to this reason, the FBEs are not taken into account in dedicated compact FD-SOI models.

However, there are abundant experimental reports revealing the possible activation of vestigial FBEs in relatively thick FD-SOI transistors. The basic argument is that the body of the transistor – still isolated by the BOX, gate oxide, and junctions – is not totally free from variations in majority carrier charge. The isolated body can be susceptible to bring the change of majority carrier into out-of-equilibrium conditions: increasing external bias, changing temperature, transient state, and exposure to light.

The main purpose of this chapter is not to review the FBEs since these are widely documented in the literature. Instead, we examine for the first time their viability in state-of-the-art FD-SOI MOSFETs with an ultrathin body, thinner or slightly thicker than 10 nm. The results are of practical

importance for SOI-based circuit design or SOI device engineers. Hence, we demonstrate many-sides experiments where the absence or presence of FBEs can be correlated to film thickness It is found that the body thickness, back bias and scan speed are relevant parameters that impact of FBEs. In particular, the competition between FBEs and super-coupling effect in sub-10 nm thick films is briefly outlined in Chapter 2. The following sections describe the various voltage-dependent or time-dependent FBEs under investigation. Three less usual mechanisms, namely gate-induced floating body effect (*GIFBE*), metal-stable dip (*MSD*) and super-coupling, are discussed.

2.2 Kink Effect in Ultrathin Fully-Depleted SOI MOSFETs

The kink effect is defined by the appearance of non-linear behavior in the output characteristics of a SOI MOSFET as demonstrated in Figure 2.1 [4], [5]

This effect is quite pronounced in partially-depleted (*PD*) SOI MOSFETs. Majority carriers are generated by impact ionization and stored within the neutral region. As a result, the body potential begins to increase and then lowers the threshold voltage progressively [1], [4]–[7]. Since more carriers are available in the channel, the impact ionization process is amplified, which further increases the body potential. This positive feedback mechanism results in a sudden increase in drain current that can be beneficial for current drive and speed in logic circuits as the current over-driver circuitry in the conventional DRAM. It is, however, detrimental for the linearity of analog circuits.

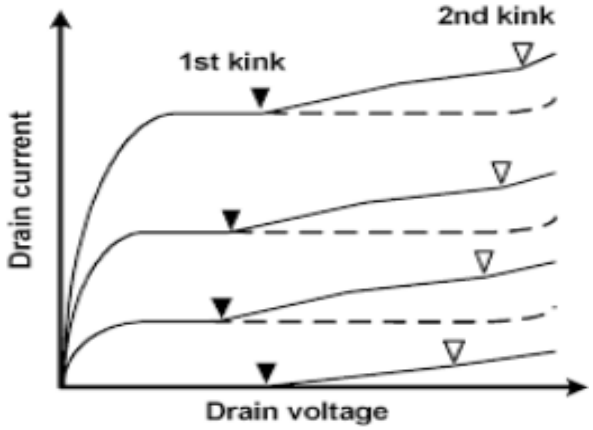


Figure 2.1: Experimental I_D (V_D) characteristics in n-channel SOI MOSFETs showing the onset of the kink effect (solid lines), which disappears by connecting the body to the ground [5].

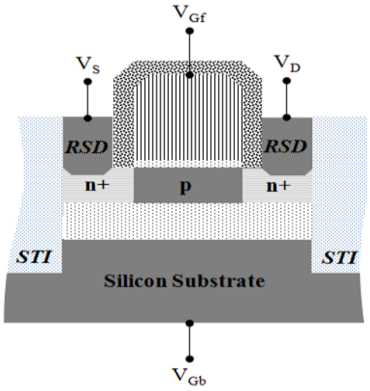
We revisit the presence of the kink effect systematically in ultrathin FDSOI MOSFETs fabricated by CEA-Leti or STMicroelectronics for 28 nm node technology. The back-gate bias enables to control the kink effect via the formation of an accumulation holes layer at the back interface. The kink is more or less pronounced according to the film thickness and channel length. However, in ultrathin (< 10 nm) and/or very short transistors (L < 50 nm), the kink is entirely absent as a consequence of super-coupling effect.

Generally speaking, the kink effect has also been observed in relatively thick fully depleted (*FD*) SOI MOSFETs, where the back gate was used to convert FD operation into PD mode [7]. A negative back-gate voltage enabled the storage of enough holes near the back Si-BOX interface, thereby triggering the kink behavior of output characteristics [7], [26]. In the following sub-section, experimental results and TCAD simulations are demonstrated for verifying the kink effect in FDSOI devices. We show up-to-date recent data about the kink effect:

- The experimental conditions enabling the activation of the kink effect in state-of-the-art n-channel FDSOI MOSFETs with the thickness from 25 nm to 8 nm are investigated (2.2.2.).
- The body potential variation is monitored and then correlated to the drain current characteristics in order to interpret the onset of the kink effect.
- Pulsed measurements are performed in order to confirm the impact of the generation rate of majority carriers on the kink effect during a designated pulse period and width (2.2.3.).
- TCAD device simulation is conducted (2.2.4.) that guides us to interpret the variation of the kink effect.

2.2.1 Experimental Details

Several generations of FDSOI MOSFETs have been examined. The thickness of Si film (t_{Si}) varied from 25 nm down to 8 nm and the buried oxide (BOX) was 25 nm thick. The top silicon body was either initially undoped (background doping of $N_A \sim 10^{15}$ cm^{-3}) or lightly doped ($N_A \sim 10^{17}$ cm^{-3}). The FDSOI fabrication process at STMicroelectronics included a high-k/metal gate scheme with thin or thick dielectric. We investigated n-channel devices with variable gate lengths down to L_G = 40 nm. Back-gate bias (V_{Gb}), ranging from 0 V to -10 V was applied through a highly doped ground plane ($N_A \sim 10^{18}$ cm^{-3}) as depicted in Figure. 2.2.



Device information		
Parameters	**Type-I**	**Type-II**
t_{si} [nm]	**25**	**8.5**
Width [µm]	10	
Length [nm]	40 to 1000	
t_{ox} [nm]	2.9	
BOX [nm]	25	
N_A [cm^{-3}]	10^{17}	
Gate	Poly	
Source/ Drain	Raised Source and Drain	

Figure 2.2: A simple schematic of a FDSOI MOSFET with raised source drain (RSD), generally used for verifying the FBEs.

Five-terminal body-contacted devices were used for monitoring the body potential as illustrated in Figure 2.3. This type of devices enabled us to observe the internal variation of potential via the integrated body contact. Especially, the 'H-gate' FDSOI MOSFET design provides two symmetric body contacts at both ends of the gate. This can help to eliminate the sidewall direct leakage current path underneath the gate layer. Thus, the net current only flows between the source and drain unless the body contact is connected to ground (0 V) or to a positive voltage (> V_T) as in the forward mode of a diode.

It is worth using a body contact of the H-gate MOSFET to examine the presence of the floating body effects even in extremely thin film devices. When the body under the gate is fully depleted and then inverted, the whole inverted area acts as an n-type semiconductor resistor. The output current flows not only at the front surface, but also in the body according to the volume inversion concept [5], [27].

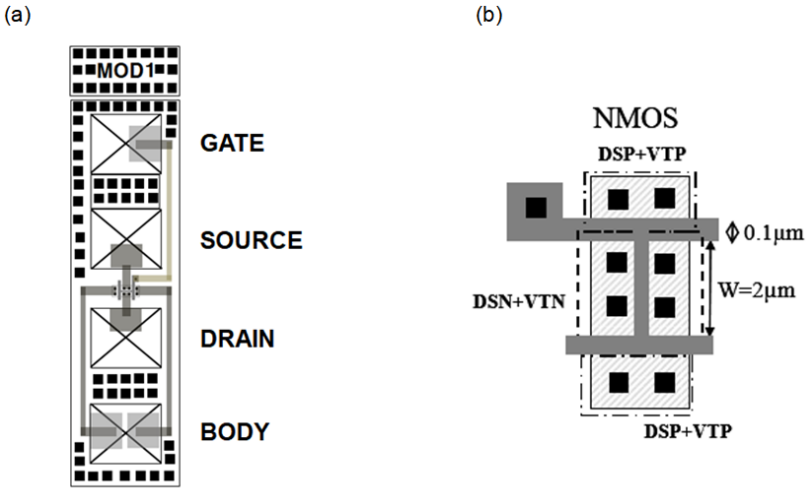


Figure 2.3: (a) Metal pad configuration of test module, (b) layout for an H-gate body-contact n-MOSFET device.

2.2.2 DC Measurement

A prominent kink effect is clearly found in DC conditions when the back gate (V_{Gb}) became negative voltage from 0 V to -10 V, respectively (Fig. 2.4a, b).

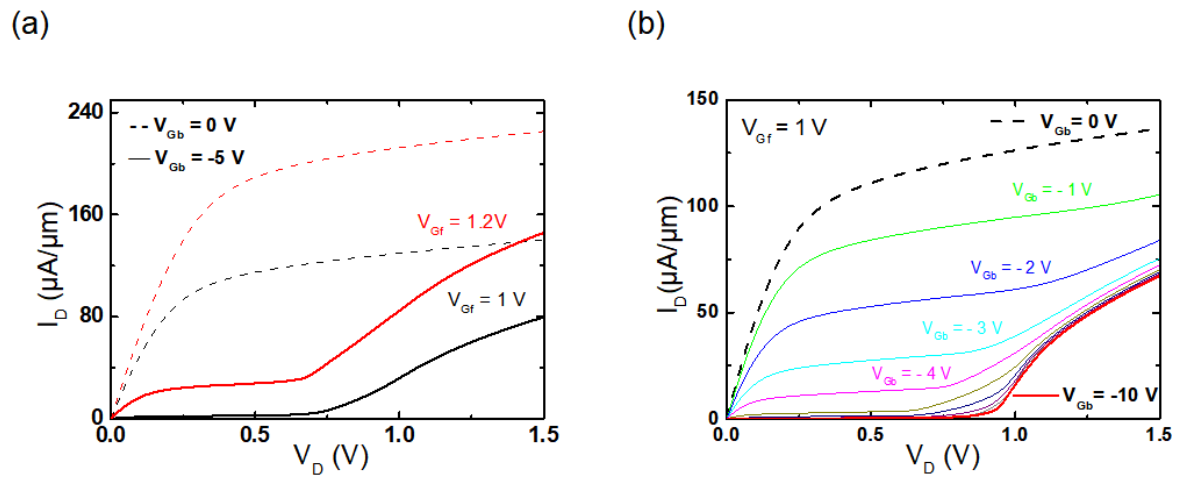


Figure 2.4: Normalized output $I_D(V_D)$ characteristics with back-gate voltage (a) V_{Gf} = 1 V, 1.2 V and V_{Gb} = 0 V or -5 V. (b) V_{Gf} = 1 V and V_{Gb} = 0 to -10 V. W = 10 μm, L = 150 nm, t_{Si} = 25 nm, t_{ox} = 2.9 nm, t_{BOX} = 25 nm.

Case 1: Floating-body transistors

Figure 2.4a shows typical output $I_D(V_D)$ characteristics of 25 nm thick transistor. In normal operation with a back-gate grounded (V_{Gb} = 0 V), there is no kink effect as dashed lines show. However, for negative back-gate bias (V_{Gb} = 0 to -10 V), a marked kink effect develops for V_D ~ 0.7–1 V. The amplitude and onset of the kink depend on the front-gate bias and back-gate bias (Fig. 2.4). Namely, the kink is accentuated by the interface coupling effect: a negative back bias increases the front-channel threshold voltage and decreases the drain current. FDSOI MOSFETs with several gate lengths, from 1 *μm* to 40 nm, are demonstrated. Figures 2.5a-d show that for V_{Gb} < -5 V, the drain current seems to jump from 'zero' (sub-threshold value) to a high value (strong inversion). That is because the excess holes generated by impact ionization increase the body potential and, therefore, trigger the kink.

In short transistors (L_G = 50, 40 nm; Fig. 2.5e, f), the kink is noticeably attenuated and hardly detectable for several reasons:

(i) The potential barrier at the source is lower than in long transistors. This drain-induced barrier lowering (*DIBL*) enables the holes generated by impact ionization to escape through the forward-biased source junction instead of accumulating in the body.

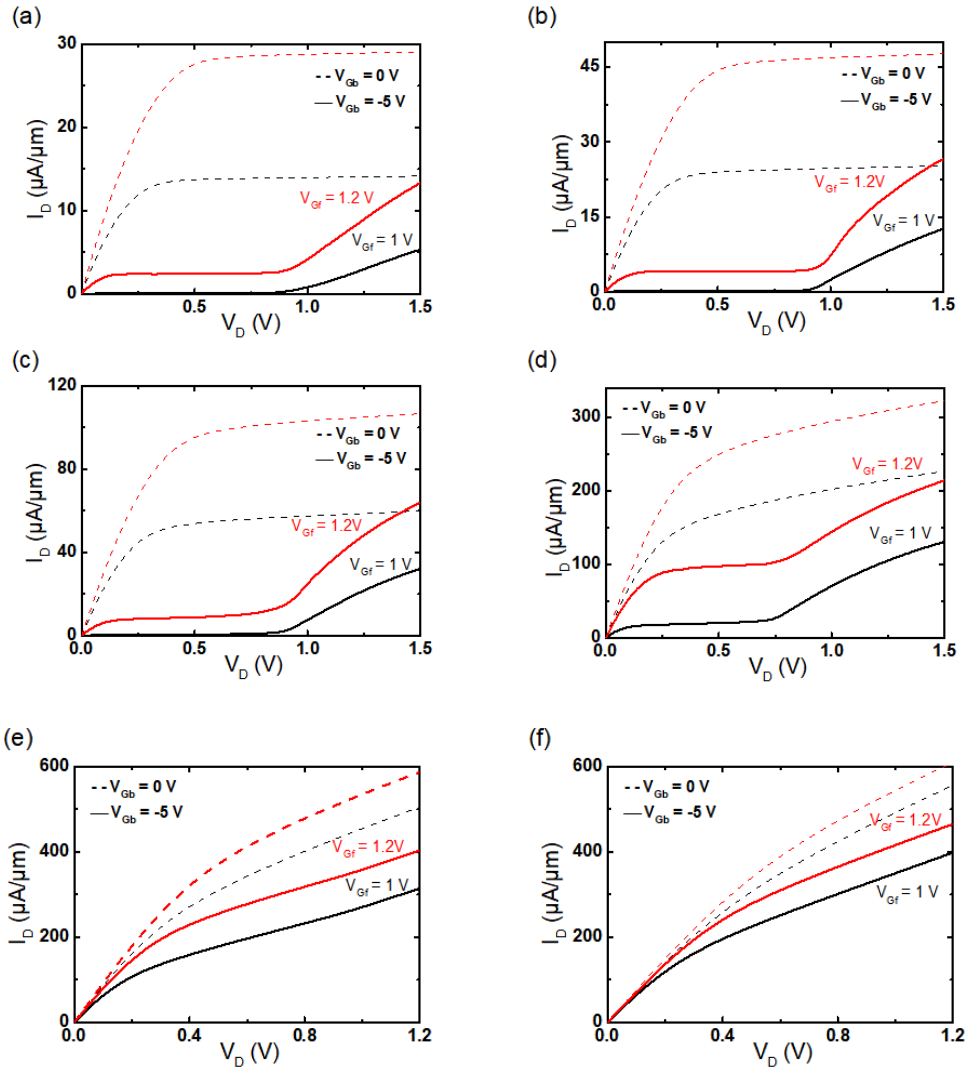


Figure 2.5: Impact of back-gate bias V_{Gb} from 0 V to -10 V (step -1 V) on $I_D(V_D)$ characteristics for various channel lengths: (a) 1 µm, (b) 500 nm, (c) 250 nm, (d) 100 nm, (e) 50 nm, and (f) 40 nm; W = 10 µm, t_{Si} = 25 nm, t_{ox} = 2.9 nm, and t_{BOX} = 25 nm.

(ii) The large output conductance induced by DIBL can mask the kink-related current increase; the competition between kink and DIBL is visible in Figure 2.5e, f.

(iii) The accumulation of holes is weakened by the proximity of the source and drain junctions. The lateral fringing fields, from source/drain through the substrate and BOX, modify the body potential [12], [13] and attenuate the impact of back-gate bias in short-channel devices [14]. It follows that the influence of back-gate on kink is attenuated.

The critical voltage V_C for kink onset is defined as the inflection point in $I_D(V_D)$ curves (see Fig. 2.6a), which corresponds to a conductance peak. At a constant gate voltage, V_C would tend to decreases slightly as long as channel lengths are shorter (Fig. 2.6b). The reason is that the lateral field and impact ionization are stronger in short channel devices, thereby shifting the kink onset to lower drain bias.

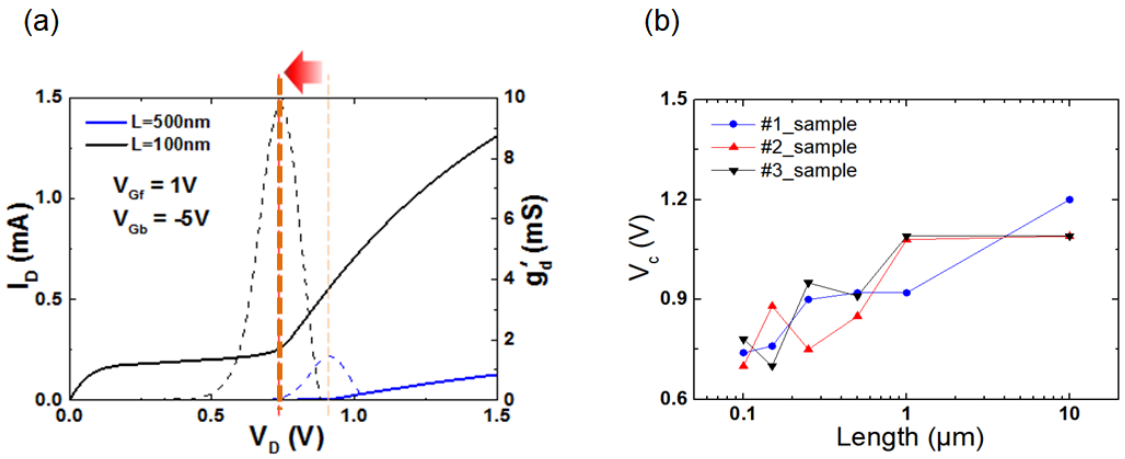


Figure 2.6: (a) Experimental $I_D(V_D)$ characteristic and output conductance $g_d(V_D)$ curves for L = 500 nm and 100 nm. (b) The critical voltage V_c tendency extracted from the peak of output conductance verses channel lengths. For V_{Gf} = 1 V, V_{Gb} = -5 V and W = 10 μm.

Case 2: H-gate body contacted n-MOSFET

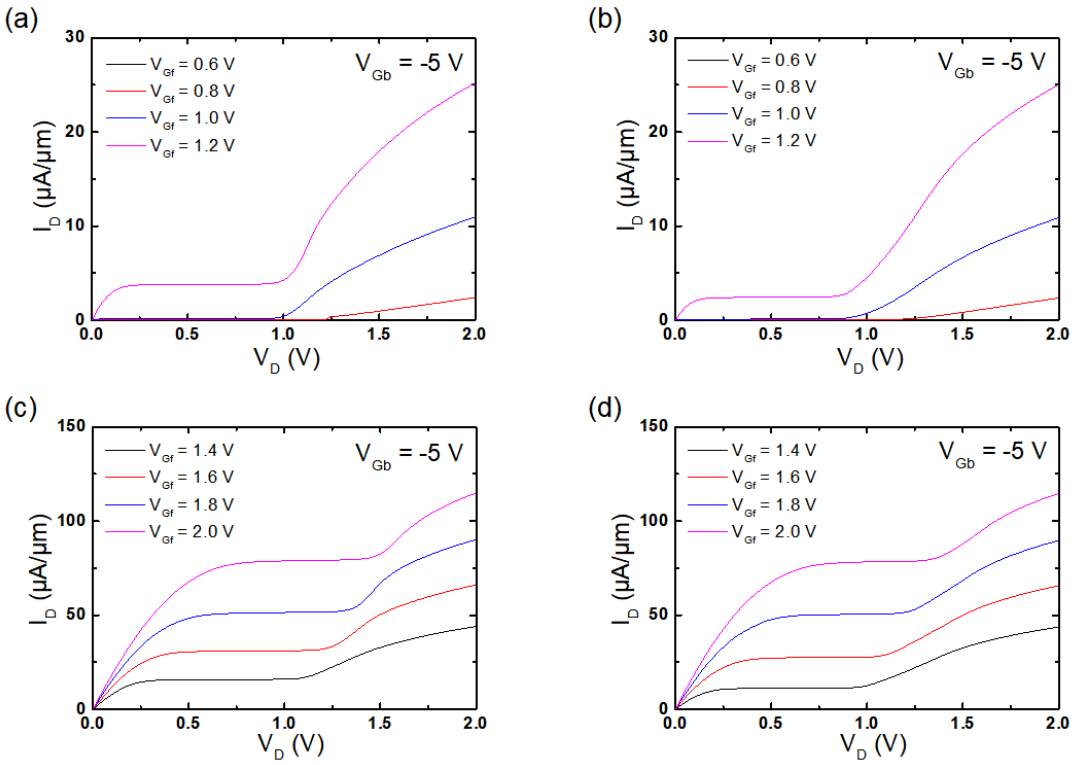


Figure 2.7: Comparison of output characteristics with different front gate voltages (from 0.6 V to 2.0 V) between the normal n-MOSFET (a, c), and H-gate body contact n-MOSFET with floating body (b, d). For t_{Si} = 25 nm, t_{BOX} = 25 nm, L = 1 μm and W = 10 μm.

The typical characteristics of the H-gate body-contacted MOSFETs with t_{Si} = 25 nm and the body floating are reported in Figure 2.7. DC characteristics are almost the same tendency in terms of

current magnitude and critical voltage. The only difference is that the rising slew of the H-gate device is slightly shaper than the normal n-MOSFET.

Whatever the V_{Gb} bias, there is no kink effect as long as the body contact is grounded and able to expel the generated majority carrier charge (Fig. 2.8a). However, when the body is floating (Fig. 2.8b), the kink appears for negative V_{Gb}, in agreement with Fig. 2.4.

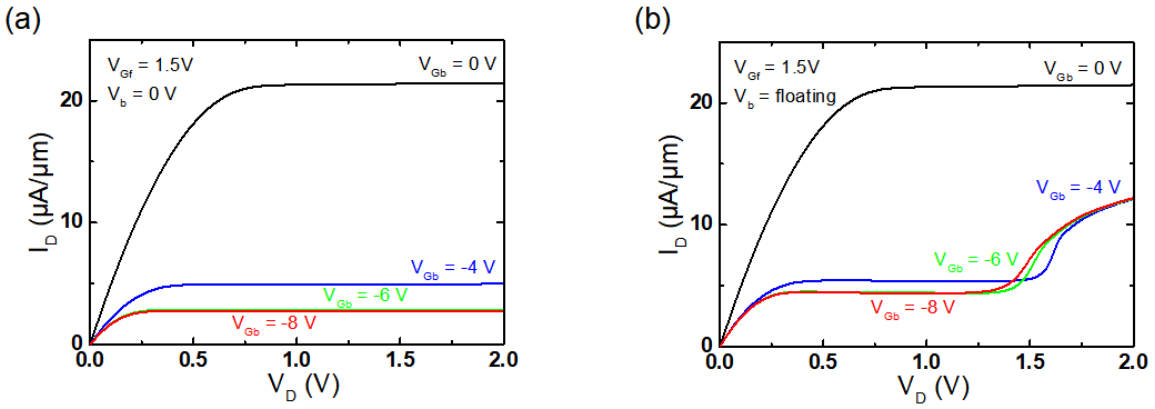


Figure 2.8: Comparison of I_D (V_D) characteristics of 5-terminal FDSOI MOSFETs measured with the body contact (a) V_b = 0 V; the excess holes are expelled through the grounded body as in bulk silicon device or (b) the body floating condition as for SOI device. V_{Gf} = 1.5 V, t_{Si} = 25 nm, t_{BOX} = 25 nm, W = 10 μm, and L_G = 5 μm.

We measured the body potential in the transistors for the first time. Figures 2.9a demonstrates the close correlation between kink effect and body potential variation. In 'thick' device (t_{Si} = 25 nm), a sharp increase in body potential occurs concomitantly with the kink onset. An intriguing aspect is that FD-SOI MOSFETs with sub-10 nm film thickness do not exhibit the kink effect regardless of the negative back-gate bias, channel length or drain bias. In these devices the body potential remains flat as V_D is increased (Fig. 2.9b).

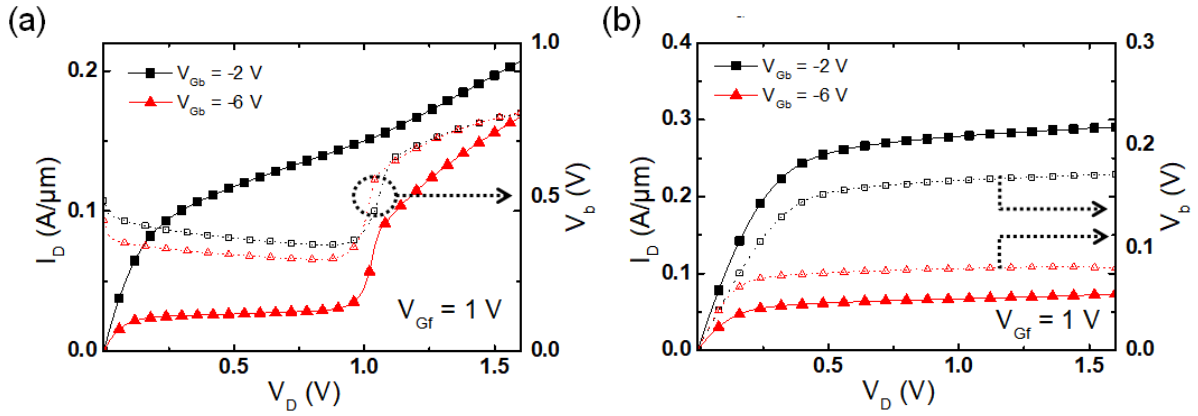


Figure 2.9: Output DC characteristics and corresponding body potential V_b, in FD-SOI MOSFETs with variable Si film thickness. (a) t_{Si} = 25 nm, (b) t_{Si} = 7 nm, L_G = 100 nm and t_{BOX} = 25 nm.

This result is an indirect proof of the super-coupling effect [28], [29].

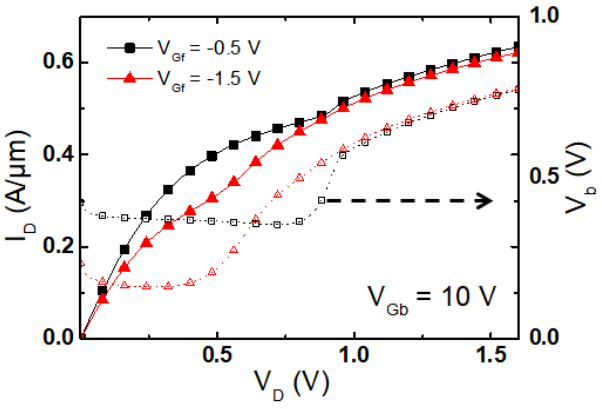


Figure 2.10: Back-gated output characteristics measured with the front gate biased in accumulation and the back gate in inversion. The body potential V_b increases at the kink onset.

The kink effect is also evidenced by operating the back channel and biasing the front-gate bias in accumulation, as demonstrated in Figure 2.10. The jump in body potential clearly indicates the activation of the kink. V_b does not change until enough holes are accumulated in the body, which explains why the kink turn-on voltage V_D is necessarily higher for lower negative gate bias (V_{Gf} = -0.5 V).

Case 3: Ultrathin body contacted n-MOSFET

In the case of ultrathin body n-MOSFETs with t_{Si} = 8 nm, the output characteristic is obviously different and quite interesting. The remarkable point shown in Figure 2.11 is that the kink effect could not be activated even with a negative back-gate voltage, meaning that the majority carriers do not accumulate and contribute the change of the floating body potential. This result may look surprising but is an authentic direct consequence of a super-coupling effect [28], [30], [31]. The super-coupling inhibits the co-existence of a front electron-channel and an accumulated hole-channel at the back interface in transistors which are thinner than ~10 nm. Since the accumulated holes cannot be formed at the back, the output current is unaffected from the kink effect.

It is well-known that the super-coupling effect is enhanced in short channel devices and can disappear in thicker devices. This argument can also be invoked to explain the kink-length dependence noted in Figure 2.5: The kink is clearly attenuated in shorter transistors. The super-coupling mechanism has been interpreted and archived by numerical simulations [31] and recently by dedicated experiments [29] using the 4-gate MOSFET architecture [32].

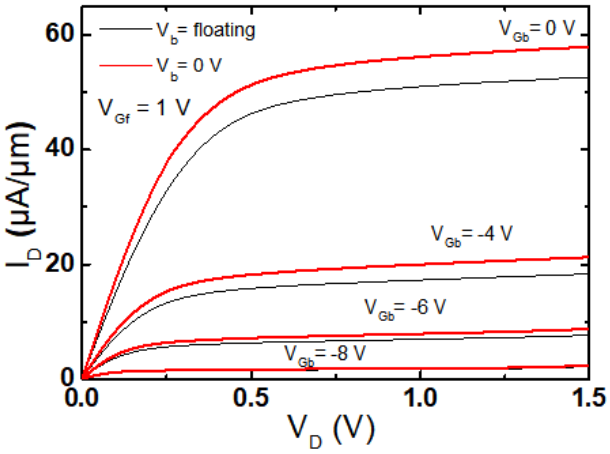


Figure 2.11: Output of $I_D(V_D)$ characteristics of 5-terminal ultrathin FDSOI MOSFETs measured with the body contact grounded or floated. V_{Gf} = 1 V, t_{si} = 8 nm, t_{BOX} = 25 nm, W = 10 μm, and L_G = 5 μm.

2.2.3 Pulsed-Mode Measurement

The total amount of impact ionization is rigorously dependent on the lateral electrostatic field governed by drain bias. The drain voltage waveform we have used is depicted in Figure 2.12a. This arrangement enables to tune the pulse duration and the duty ratio that control the duration of impact ionization, charge accumulation in the body and self-heating. Indeed, the measured drain current is computed within one period of time. For example, drain bias is just applied to 20 mV for 0.5 ms out of 5 ms period as shown in Figure 2.12b.

Figure 2.13 shows $I_D(V_D)$ characteristics in DC (Fig. 2.13a) and pulse modes (Fig. 2.13b, c) with different front gate biases, from 1.2 V to 2 V, respectively.

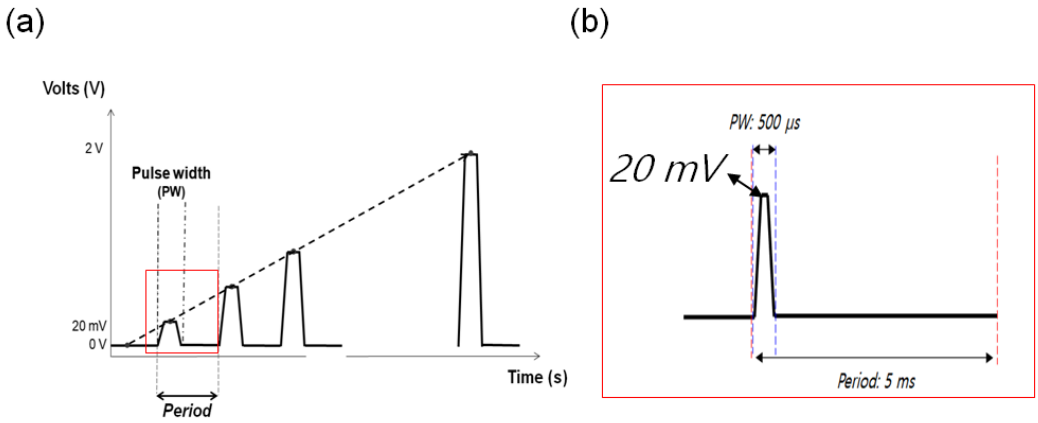


Figure 2.12: Ramped drain voltage configuration as a sawing waveform for pulse mode measurement.

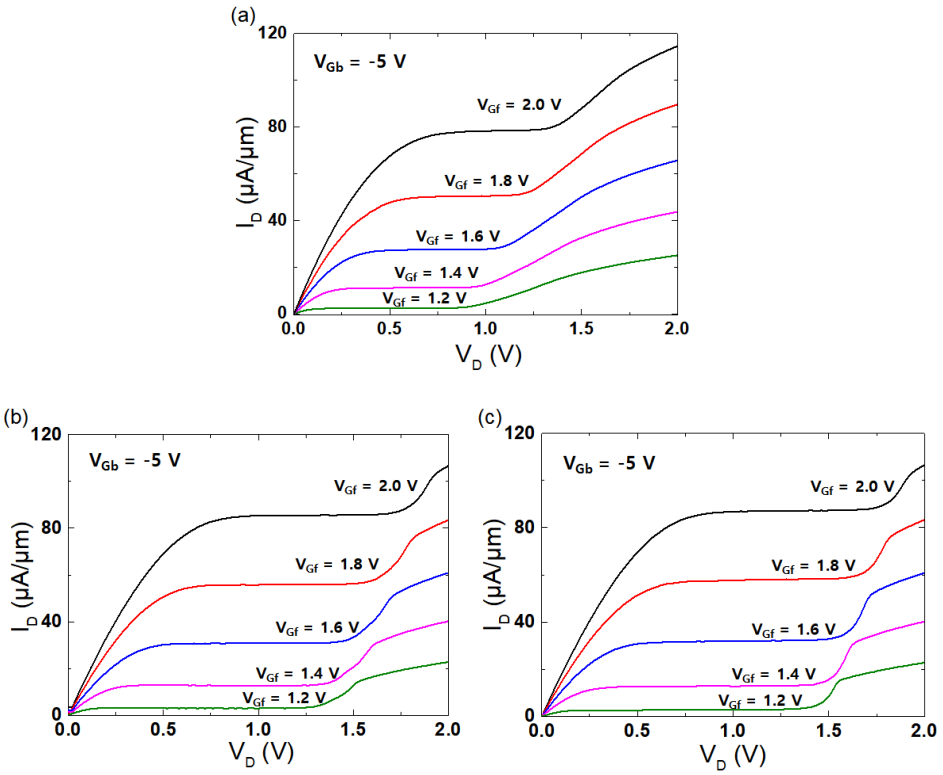


Figure 2.13: Kink effect output characteristics as a function of gate bias V_{Gf} in the normal n-MOSFET. (a) DC bias condition, and pulsed mode measurement: minimum pulse width of 0.5 ms per (b) a short period of 5 ms and (c) a long period of 500 ms.

Two cases are represented:

One is a short period of 5 ms (Fig. 2.13b) and the other is a long period of 500 ms (Fig. 2.13c) with the same pulse width (0.5 ms). In fact, the kink effect is obviously shifted to the right (at higher V_D) compared with DC results. This implies that the excess *holes* generated under the specified pulse mode conditions are insufficient to trigger immediately the kink effect; therefore a much larger impact ionization rate (*i.e.*, higher V_D) is required.

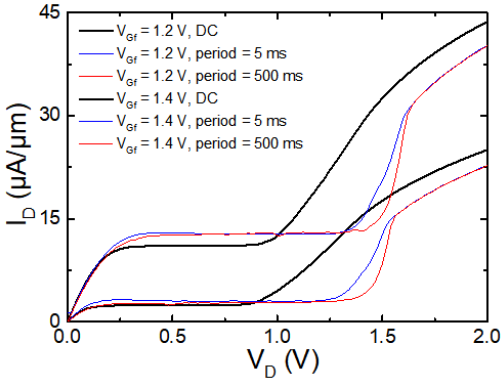


Figure 2.14: Comparison of the kink effect measured in DC and pulsed modes for a normal n-MOSFET device. V_{Gb} = - 5 V, t_{Si} = 25 nm, t_{BOX} = 25 nm, W = 10 μm, L_G = 1 μm, and PW = 0.5 ms.

The DC and pulsed mode characteristics of a normal FDSOI n-MOSFET are superimposed in Figure 2.14. For short pulse widths (0.5 ms) of drain voltage in the saturation region ($V_D \approx 0.8$ V), the drain current is clearly higher than that in DC condition. This reveals the impact of device self-heating in DC mode, which reduces the carrier mobility, thus the drain current is lowered.

Surprisingly, the output characteristic is entirely different beyond the kink region ($V_D \approx 1.5$ V): despite the increased self-heating, the current in DC mode is much higher than in short pulsed modes. This result confirms that the number of holes generated during short pulse duration is insufficient, unable to raise the body potential as much as in DC. A lower potential explains both the reduced drain current and the higher V_D needed to trigger the kink effect in the pulsed mode. Further confirmation is obtained by considering the impact of the pulse period in Figure 2.14. For longer time (500 ms) in-between two pulses, some of the stored holes recombine, which again results in an increase of the voltage needed for kink onset.

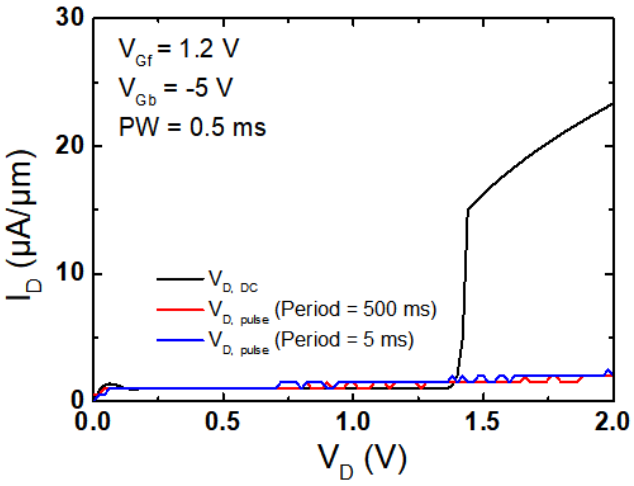


Figure 2.15: Drain current characteristics of 5-terminal MOSFET in DC and pulse mode (V_{Gb} = -5 V) for a long channel device with a short pulse width of drain voltage (0.5 ms)and a long or short period, respectively. t_{Si} = 25 nm, t_{BOX} = 25 nm W = 10 µm, L = 1 µm.

Figure 2.15 shows the case of 5-terminal n-MOSFET device. In spite of the body contact being left floating, there is no trace of the kink effect for short pulses width of drain voltage (0.5 ms), regardless of the pulse period or the negative back-gate bias. In order to clarify this behavior, the body potential variation was monitored as a function of drain bias and pulse parameters. Several interesting aspects are revealed in Figure 2.16a:

- There is a clear correlation between the onset of the kink effect and abrupt rise in body potential.
- The body potential is always smaller in pulsed mode than in DC.
- The shorter the pulse width, the higher the drain voltage needed to trigger the kink.

- For very short pulses (0.5 ms), the body potential is unchanged and independent on V_D.

Additional experiments show that a longer pulse period increases the recombination probability of excess holes. For such a long time in off-state, fewer excess holes would be retained in the body owing to leakage currents and SRH recombination in the volume and at the interfaces. As a result, the body potential measured with a long pulse period (500 ms) is lower than for short periods or DC.

Figure 2.16b shows the variation of the quasi-Fermi potential for holes, as obtained from TCAD device simulation. The correlation with the body potential variation is striking and understandable, which validates our interpretation.

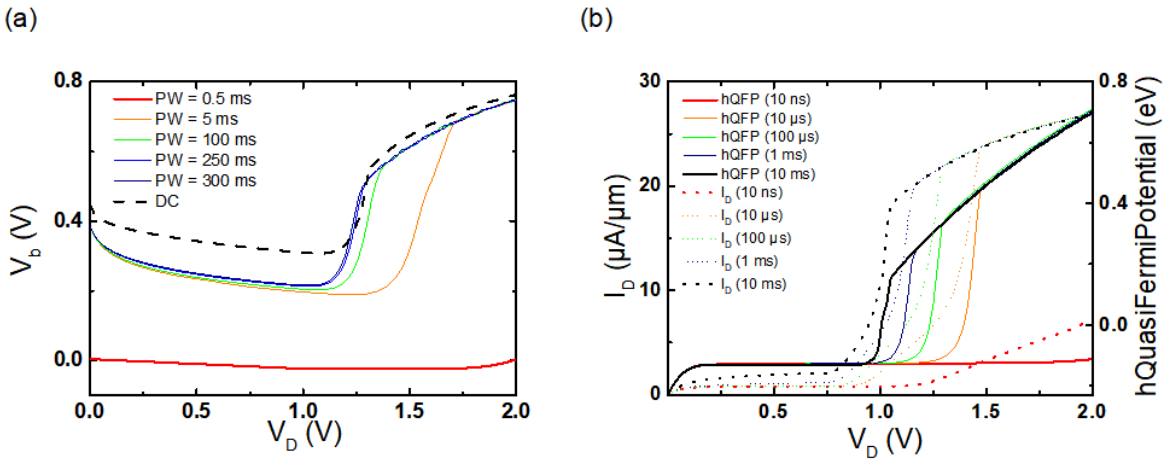


Figure 2.16: (a) Body potentials versus drain bias and pulse width (PW), measured with long-period pulses (500 ms). (b) Simulations showing the quasi-Fermi potential of holes and $I_D(V_D)$ characteristics. V_{Gf} = 1.2 V, V_{Gb} = -5 V, t_{Si} = 25 nm, t_{BOX} = 25 nm. W = 10 µm, L = 1 µm.

From pulsed-mode measurements we can speculate indirectly how many holes are available, i.e. stored into the body, to contribute the change in the body potential variation. That variation is all caused by the amount of the excess holes. The number of holes generated by impact ionization is proportional to the pulse duration. For short pulse widths, this number is clearly lower than in DC condition and the onset of the kink voltage increases.

However, an alternative mechanism, based on the capacitive coupling between the drain and the body, can be invoked. A V_D pulse may increase dynamically the body potential and, as a result, the source-body junction becomes forward biased, enabling the hole-evacuation from the body. The capacitive coupling is obviously accentuated in shorter pulse modes and more holes can be swept through the source. Since fewer holes are still left in the body, the kink voltage increases. Albeit reasonable, this scenario is negated by the experiments and simulations of Figure 2.16: there is no increase of the body potential (V_b) for shorter pulse width, *i.e. PW* = 0.5 ms (Fig.2.16a).

2.2.4 TCAD Device Simulation

Synopsys tools, Sprocess and Sdevice simulator, were used to further investigate the kink effect. The numerical models for the simulation are represented in Table 2.1. Especially, a hydrodynamic transport model was used to study the kink effect because the conventional drift-diffusion model was inadequate to reproduce it. The hydrodynamic model can take into account lattice temperature, thus the carrier diffusion is well computed as well as the hot electrons temperature.

Model	
Statics and global	Fermi
	Hydrodynamic (eTemperature)
	Band-gap narrowing (OldSlotboom)
Recombination	Shockley-Read-Hall (SRH)
	Hole and Electron Avalanche Generation
	Band-to-band Tunneling Model
Mobility	Doping dependency
	Carrier-carrier scattering
	Transversal and high field saturation

Table 2.1: Numerical device simulation models for further study of the kink effect.

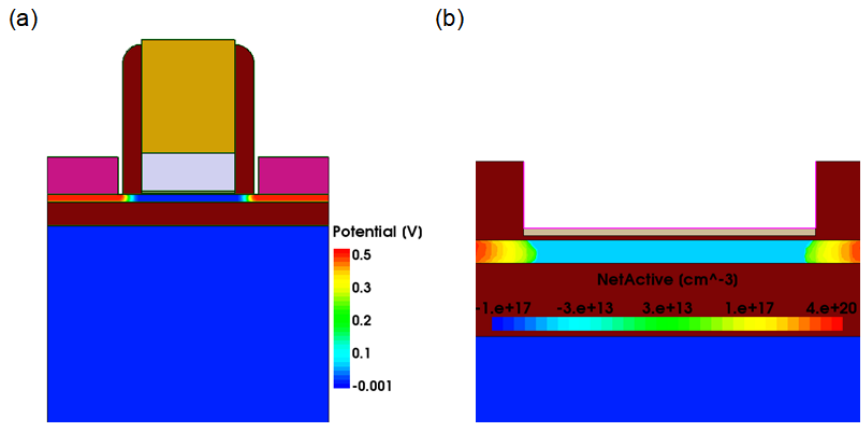


Figure 2.17: (a) Cross-section view of the simulated FDSOI n-MOSFET with a P^+ ground plane under the BOX, (b) channel region underneath the gate.

Thin and thick FDSOI MOSFETs are simulated. The device structure (Fig. 2.17) is designed with Sprocess tool. Transient solver in Sdevice is used for duplicating the kink effect, which is of Sentaurus Workbench version J-2014. 09 [33] The simulation includes physical models such as SRH generation and recombination with a temperature-dependency option, hydrodynamic model with an e-

Temperature option and electron-hole avalanche generation for impact ionization [34]. Figure 2.18 shows the simulated current-voltage characteristics, with different front and back gate voltages, that match the experimental curves of Figure 2.4: the kink is activated by back-gate biasing and depends on front-gate voltage.

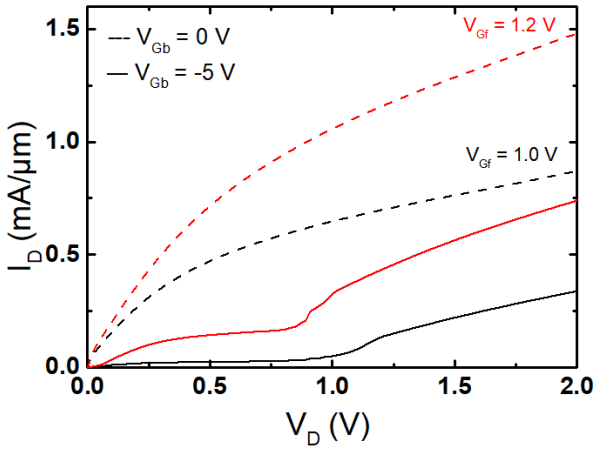


Figure 2.18: Duplicated kink effect in TCAD device simulation. t_{Si} = 25 nm, t_{BOX} = 25 nm, L = 100 nm, V_{Gf} = 1 V, V_{Gb} = 0 and -5 V.

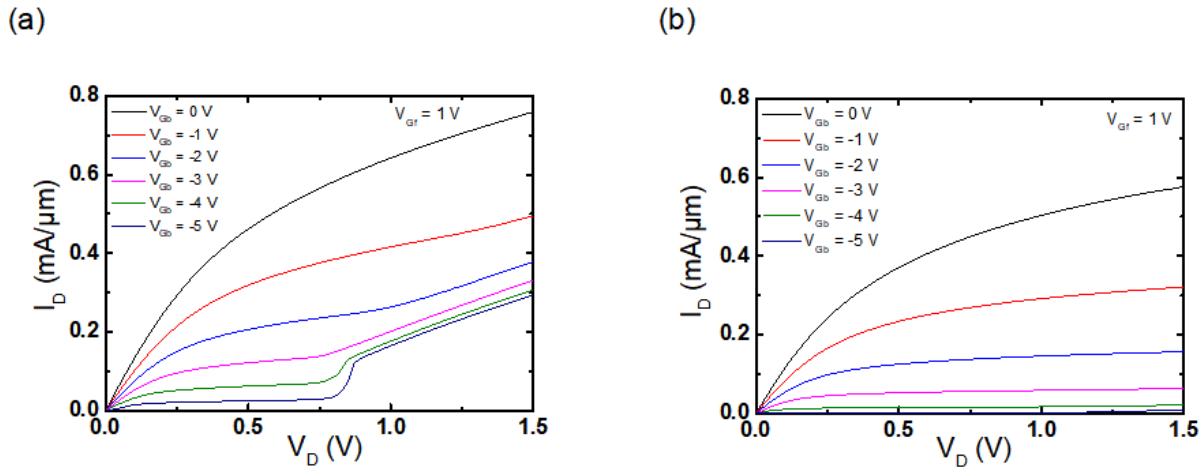


Figure 2.19: Simulated $I_D(V_D)$ characteristics for different back-gate voltages: (a) t_{Si} = 25 nm, (b) t_{Si} = 8 nm. L = 100 nm, , t_{BOX} = 25 nm, V_{Gf} = 1 V, V_{Gb} = 0 to -5 V.

The impact of negative back bias is shown in Figure 2.19 for devices with different film thickness. Only in thicker devices does have the kink effect developing for V_{Gb} < -2V (Fig. 2.19a). It occurs for approximately the same drain voltage as in the experiment ($V_D \approx$ 0.9V, see Fig. 2.4 or 2.5d). Conversely, for ultrathin 8-nm FDSOI MOSFET, the kink effect is invisible even for negative back-gate voltages (Fig. 2.19b).

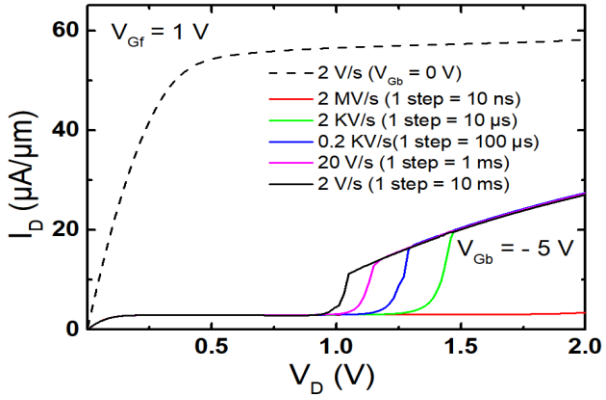


Figure 2.20: Transient simulation of output characteristics for a unit step time increased from 10 ns to 10 ms, respectively. V_{Gf} = 1 V, V_{Gb} = -5 V, t_{si} = 25 nm, t_{BOX} = 25 nm, W = 10 µm, L = 1 µm.

Figure 2.20 demonstrates the impact of V_D sweeping time and intervals in between each step. The sweep time reflects the muliplication of cycles where excess carriers are generated by impact ionization. It thus corresponds to the avalanche generation rate in the floating body. Namely, the net density of excess positive carriers is dominant to control the body potential and hence governs the onset of the kink. The fastest sweeping with 10 ns steps is unable to trigger the kink, in good agreement with the experimental curves of Figure 2.16a. The variation with sweep time of the critical voltage of the kink-onset is equally matching as the experiment results.

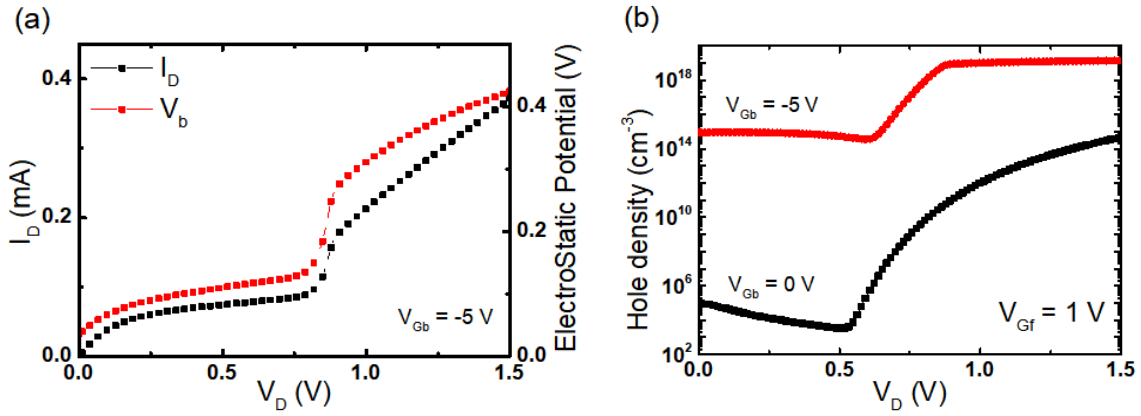


Figure 2.21: (a) Correlated variations of drain current and body potential at the onset of the kink effect duplicated by TCAD simulation. (b) Excess holes density at the back interface as a function of the drain bias. L_G = 100 nm, t_{Si} = t_{BOX} = 25 nm, V_{Gf} = 1 V, V_{Gb} = -5 V.

Figure 2.21a reproduces the behavior of a thick and short channel device (t_{Si} = 25 nm and L = 100 nm). The body potential (red symbols) and drain current (black symbols) variations are well correlated and sharp in the vicinity of the kink, as observed in the experiments of Figure 2.9a. The concentration of holes is represented as a function of drain bias in Figure 2.21b. Once the impact

ionization becomes effective enough, many excess holes (~ 10^{19} cm^{-3}) accumulate at the back interface owing to the negative back bias, V_{Gb} = -5 V. In contrast, for grounded back gate, the concentration of accumulated holes is irrelevant, 4 orders of magnitude lower, unable to trigger the kink. Again, the simulations confirm that in ultra-thin device (t_{Si} = 7 nm): there is no kink effect despite the negative back-gate bias. Even after impact ionization turns on, the hole density remains low and the body potential variation is basically flat.

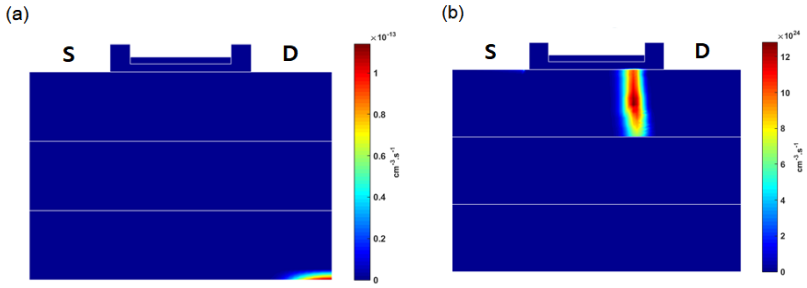


Figure 2.22: Impact ionization multiplication rate extracted from simulation for 'thick' n-MOSFET. L = 100 nm, t_{si} = 25 nm, t_{BOX} = 25 nm, V_{Gf} = 1.2 V and V_{Gb} = 0 V. (a) V_D = 0.1 V and (b) V_D = 1.2 V.

Further simulations were intended to clarify the impact ionization rates near the drain junction (Fig. 2.22) and the concentrations of holes accumulated in the body. The impact ionization rate, negligible for V_D = 0.1 V (Fig. 2.22a), increases substantially for V_D = 1.2 V (Fig. 2.22b).

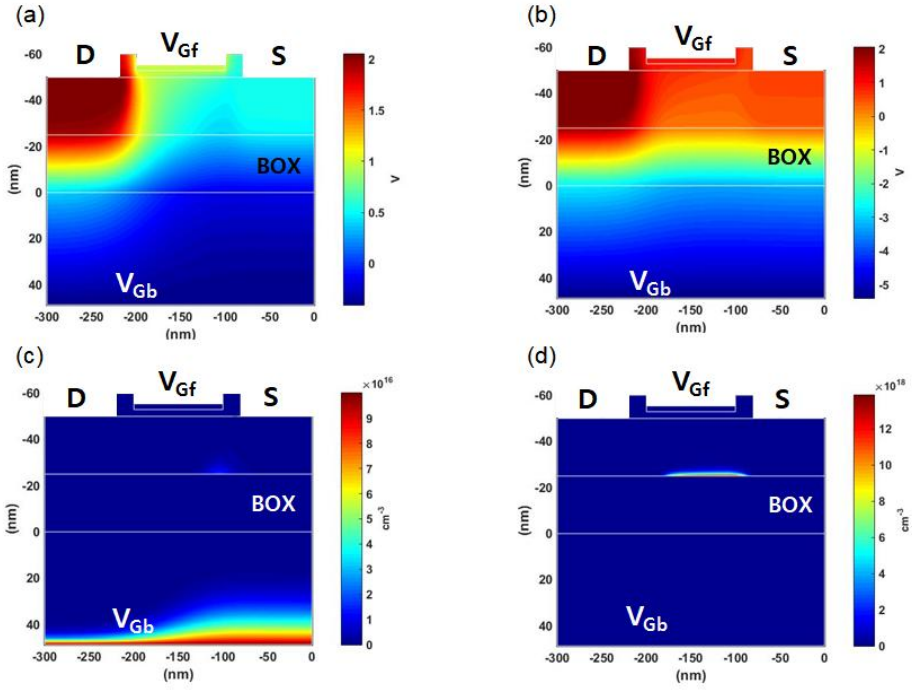


Figure 2.23: Electrostatic potential profiles with (a) V_{Gb} = 0 V, (b) V_{Gb} = -5 V and hole concentration at the back interface of the silicon body with (c) V_{Gb} = 0 V, (d) V_{Gb} = -5 V, respectively. For t_{si} = 25 nm, t_{BOX} = 25 nm, L = 100 nm, and V_{Gf} = 1 V.

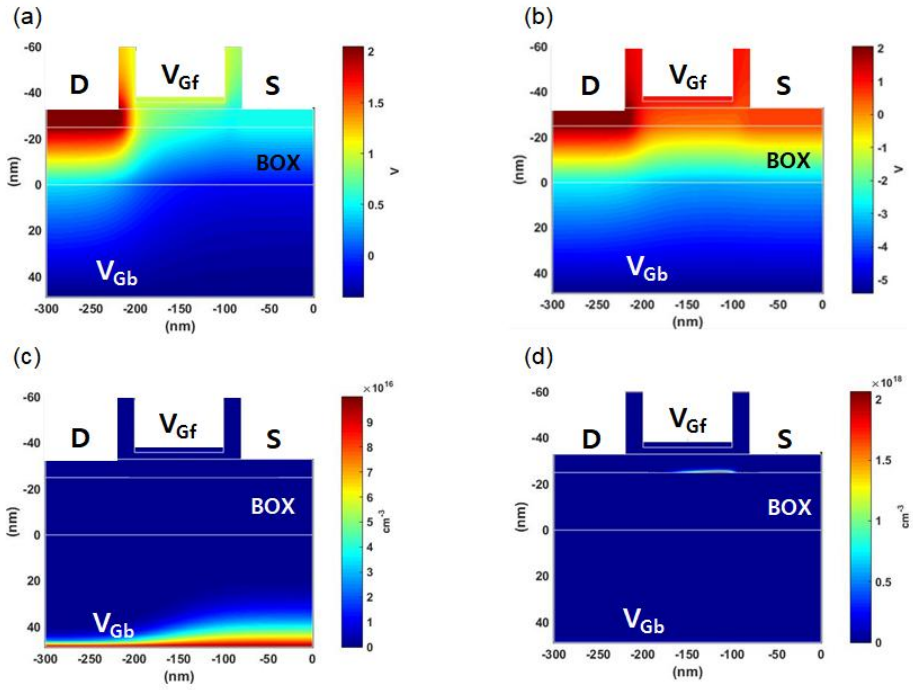


Figure 2.24: Electrostatic potential profiles with (a) V_{Gb} = 0 V, (b) V_{Gb} = -5 V and hole concentrations at the back interface of the silicon body with (c) V_{Gb} = 0 V, (d) V_{Gb} = -5 V, respectively. For t_{si} =8 nm, t_{BOX} = 25 nm, L = 100 nm, and V_{Gf} = 1 V.

Figures 2.23 and 2.24 show electrostatic potential profiles and hole concentration with the back gate voltages of V_{Gb} = 0 V and -5 V. The holes generated by impact ionization at the drain region are stored in the body, essentially near the source terminal, and modify the body potential accordingly. Although the ultrathin device has a certain amount of holes at the back interface, the excess holes cannot trigger the kink effect. The density of the positive charge is indeed much higher in Figure 2.23d than in Figure 2.24d. The difference of the excess holes magnitude is due to super-coupling effects.

2.2.5 Summary

Our study gives experimental evidence for the possibility of kink effect in ultrathin fully-depleted MOSFETs. TCAD device simulations were conducted to validate the measurements and analyze the role of excess-holes on body potential increase and kink onset. The kink effect can be activated even in 25 nm thick FDSOI transistors by applying a negative back bias. This is not harmful for circuit operation because $V_{Gb} < 0$ is generally used to maintain the transistor in OFF-state where the additional current is less relevant. Furthermore, modern FDSOI MOSFETs, with 6-7 nm body

thickness, are certainly kink-free; circuit designers can safely use a wide range of back bias for threshold voltage tuning, which is actually the main asset of this technology.

Pulsed measurements indicate that the critical voltage V_C for kink onset is higher than in DC mode and depends on the pulse duration. V_C increases for shorter pulses, until the kink is totally eliminated for very fast measurements. In transistors with sub-10 nm thick body or channel shorter than 50 nm, the kink is invisible, being impeded by the super-coupling effect. The kink effect, super-coupling, and back-biasing are inter-related effects which are specific to FDSOI devices.

2.3 Gate-Induced FBE (GIFBE) in Ultrathin MOSFETs

2.3.1 Experimental Details

In FDSOI MOSFETs with thin gate dielectric (< 2 nm), the body can be charged by occurring the gate tunneling current. The direct tunneling of electrons from the valence band of silicon film into the gate leaves excess holes in the body [10], [11]. The excess holes increase the body potential, which is reducing the threshold voltage. Consequently, the subsequent lowering of the threshold voltage boosts the drain current and gives rise to a second peak in transconductance as demonstrated in Figure 2.25 [11]. This mechanism is called gate-induced floating body effect, GIFBE. The first report on GIFBE was for partially depleted SOI MOSFETs, about 20 years ago [10].

<table>
<tr><th colspan="3">Device Parameters</th><th colspan="3">Terminal Voltage Ranges</th></tr>
<tr><th>t_{Si} (nm)</th><th>BOX (nm)</th><th>L_G (µm)</th><th>V_D (V)</th><th>V_{Gf} (V)</th><th>V_{Gb} (V)</th></tr>
<tr><td rowspan="2">8</td><td rowspan="7">25</td><td>1</td><td rowspan="7">0.02</td><td rowspan="2">0 – 1.2
(ΔV = 20 mV)</td><td rowspan="7">0, -2, -4, -6,
-8, -10</td></tr>
<tr><td>0.1</td></tr>
<tr><td rowspan="2">12</td><td>1</td></tr>
<tr><td>0.1</td><td rowspan="2">0 – 1.5
(ΔV = 20 mV)</td></tr>
<tr><td rowspan="3">25</td><td>1</td></tr>
<tr><td>0.5</td><td rowspan="3">0 – 2.0
(ΔV = 20 mV)</td></tr>
<tr><td>0.2</td></tr>
<tr><td>0.1</td></tr>
</table>

Table 2.2: For systematic measurements to identify the GIFBE in FDSOI MOSFETs.

The body-contact FDSOI MOSFETs, combining three different silicon films and few gate lengths, are examined systematically (Table. 2.2). This work represents experimental results for the GIFBE in recent FDSOI MOSFETs.

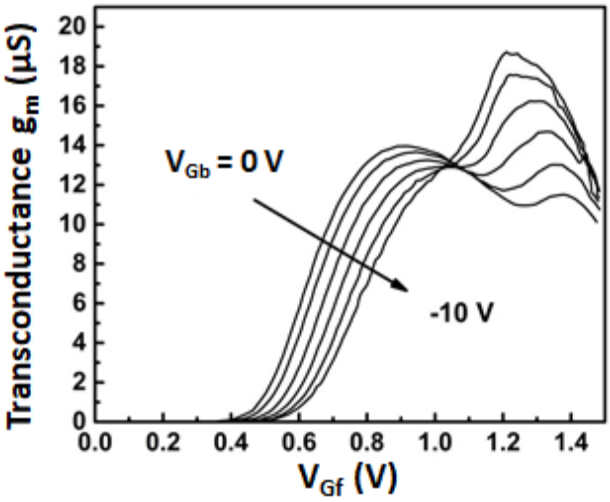


Figure 2.25: Transconductance vs. front-gate voltage in FDSOI n-MOSFET showing the impact of GIFBE. t_{ox} = 1.6 nm, t_{Si} = 17 nm, t_{BOX} = 145 nm, V_D = 0.1 V [11].

2.3.2 Current and Transconductance Characteristics

We show the band diagram for explaining the basic mechanism of GIFBE. The tungsten metal gate, silicon dioxide, p-type silicon body, and buried oxide (*BOX*) layers are illustrated in separated columns in Figure 2.26a. After becoming one system, the Fermi level is completely flat in Figure 2.26b. When a depletion layer (or weak accumulation) is formed at the back interface for negative V_{Gb}, the threshold voltage of devices is increased. For strong inversion condition (V_{Gf} > 1.8 V) at the front interface, the gate tunneling current (I_{Gf}) begins to aggregate excess holes into the floating body as illustrated in Figure 2.26c. The potential of the back interface increases gradually and influences the front-surface potential via the coupling effect. Once the excess holes prevail into the floating body, the device shows additional current conduction. Indeed, the front-channel threshold voltage is lowered which is leading to a sudden increase of the drain current as demonstrated in Figure 2.27.

This positive feedback mechanism in a floating body device is deemed to enhance the device performance (high transconductance and boosting current) or to be detrimental as a parasitic effect (non-linearity).

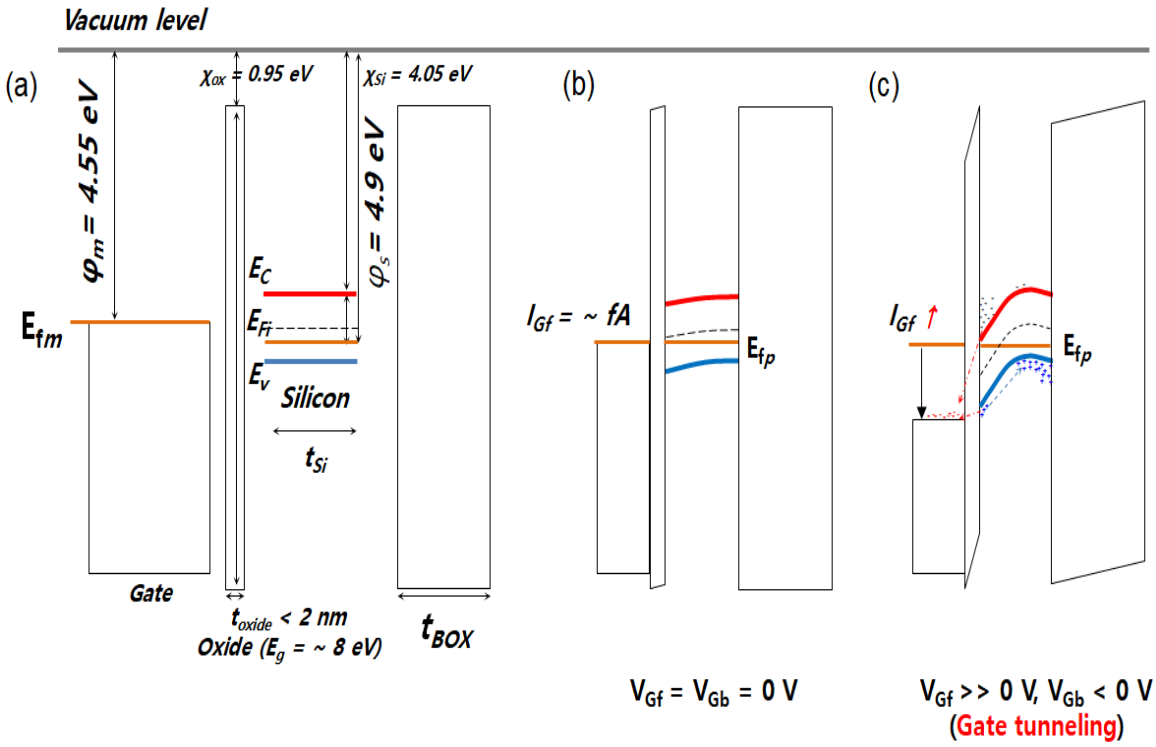


Figure 2.26: Energy-band diagrams of an ultrathin FDSOI MOSFET: (a) in independent systems, (b) thermal equilibrium-state in one system, and (c) gate tunneling via a thin gate oxide at high gate voltage.

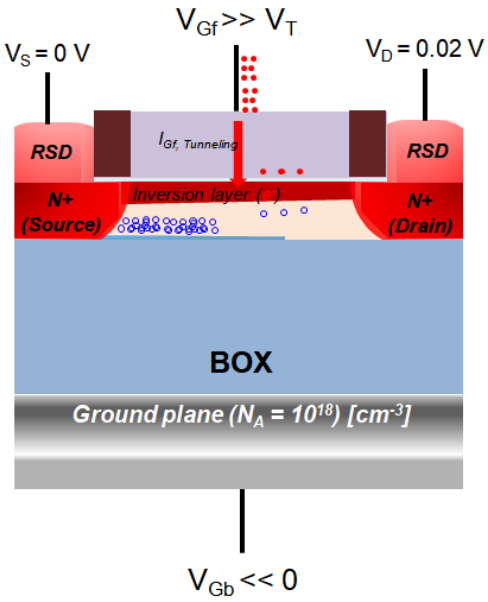


Figure 2.27: Schematic of GIFBE mechanism in FDSOI n-MOSFET, showing excess holes created by the gate tunneling current $I_{Gf,T,}$ which contributes to excess holes left into the floating body. The excess holes lower the front threshold (V_T) and drastically increase drain current instantly.

In general, this mechanism depends on the oxide thickness and occurs at a gate voltage for which the drain current increases suddenly (Fig 2.28a). For 25 nm thick FDSOI MOSFET, the changed slope of drain currents is corresponding to a second peak of transconductance g_m (1.7 V in

Fig. 2.28b). The GIFBE is evaluated at a low drain voltage (V_D = 0.02 V) which excludes any contributions associated with impact ionization. A negative back-gate voltage reinforces the amplitude of the GIFBE peak which eventually can mask the first peak that reflects the field-effect mobility (Fig. 2.28b).

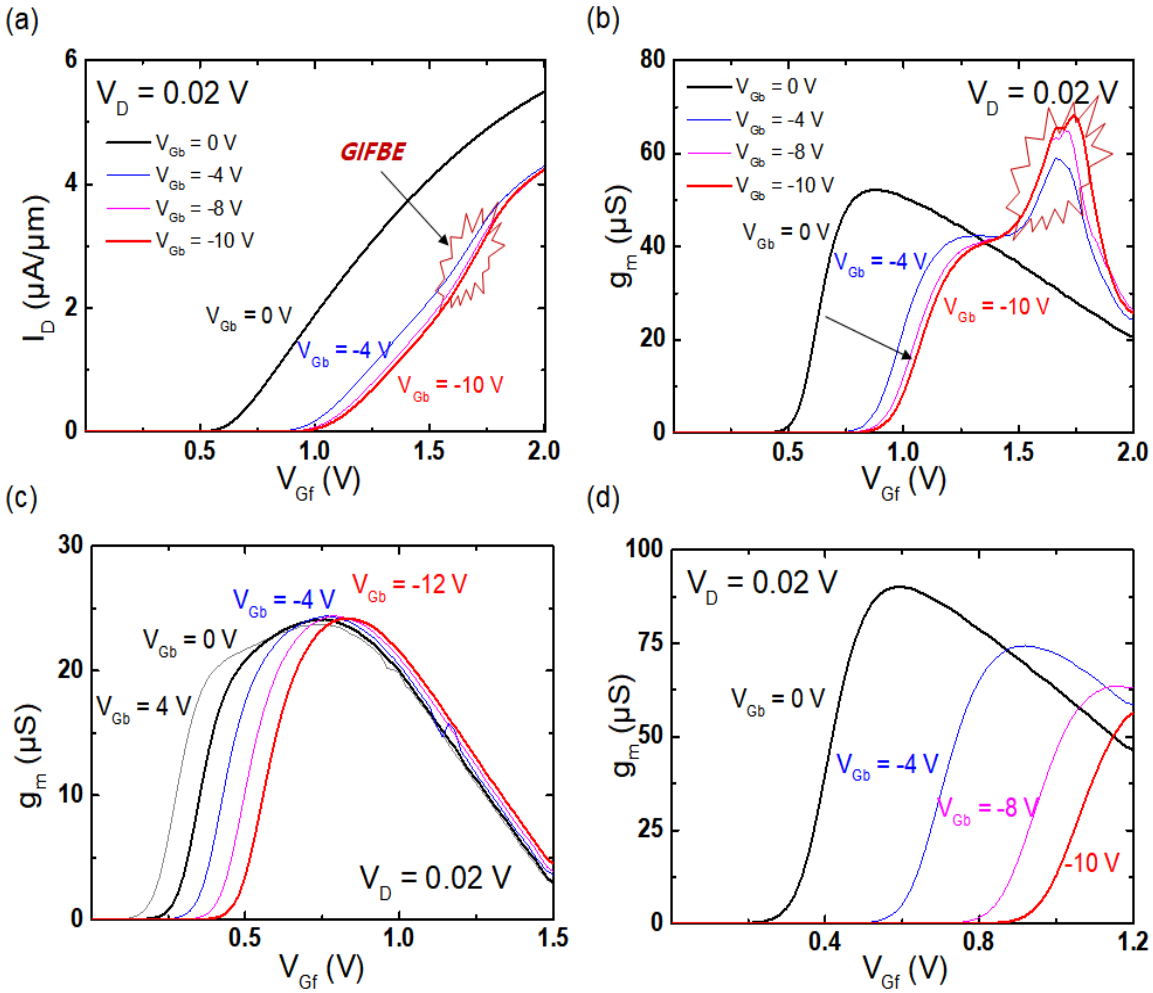


Figure 2.28: Drain current and transconductance g_m versus gate voltage for variable biasing of the substrate. (a) t_{Si} = 25 nm, drain current, and (b) transconductance showing an ample second peak for negative V_{Gb}. (c) t_{Si} = 12 nm: the GIFBE is smaller and tends to merge with the regular g_m peak for V_{Gb} < -10 V. (d) t_{Si} = 8 nm: there is no GIFBE peak. t_{BOX} = 25 nm, t_{ox} = 2.9 nm, V_D = 0.02 V, and L = 1 µm.

The mobility-related peak is shifted to the right by interface coupling effect [35], whereas the GIFBE peak is rather fixed. The two transconductance peaks may eventually merge as illustrated in Figure 2.28c where the GIFBE peak is less pronounced because the body thickness is relatively thinner (t_{Si} = 12 nm). By meaning of the super-coupling, the positive charge of holes needed to trigger the GIFBE peak cannot be sustained for t_{Si} = 8 nm. Hence the transconductance characteristics exhibit normal behavior with GIFBE-free evolution with back-gate bias (Fig. 2.28d).

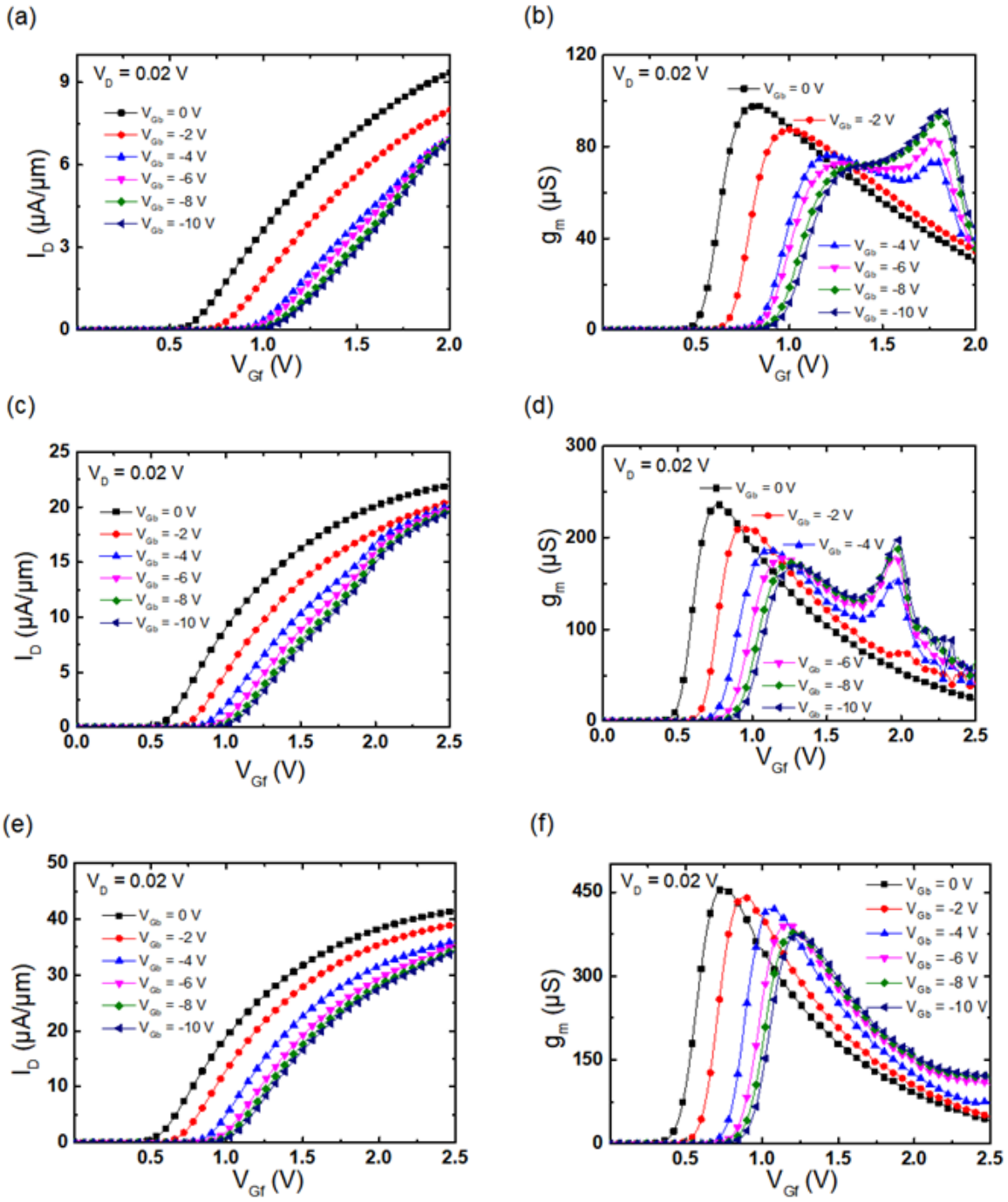


Figure 2.29: Experimental data of drain current I_D and transconductance g_m versus gate voltage for variable biasing of the substrate. Independence on channel length, showing (a) - (b) L = 500 nm, (c) - (d) L = 200 nm, (e) - (f) L = 100 nm. $t_{Si} = t_{BOX}$ = 25 nm, t_{ox} = 2.9 nm, V_D = 0.02 V.

Figures 2.29 and 2.30 reproduce experimental drain current and transconductance curves showing the dependence with channel length (L = 500 nm, 200 nm, and 100 nm and film thickness.

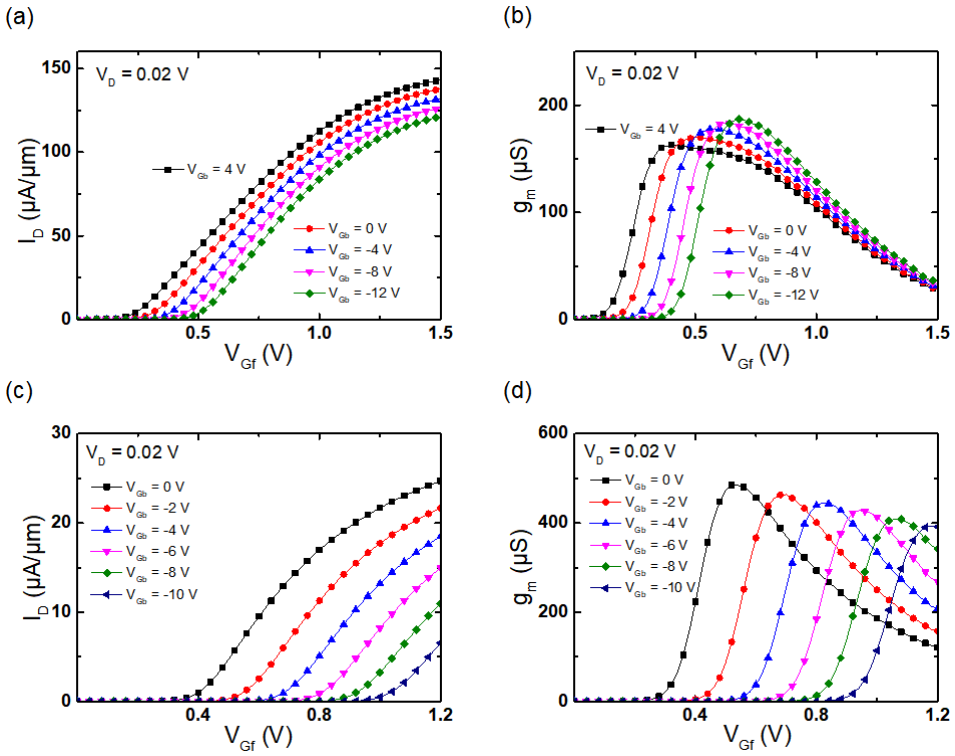


Figure 2.30: Experiment data of drain current and transconductance g_m versus gate voltage in short channel devices, showing (a) - (b) t_{Si} = 12 nm, (c) - (d) t_{Si} = 8 nm. L = 100 nm, t_{BOX} = 25 nm, t_{ox} = 1.5 nm.

Through the experiments, the gate length has a crucial impact on the GIFBE as shown in Figure 2.31a. In shorter devices, the second peak is attenuated and reveals at higher gate voltage. These features are attributed to the partial elimination of holes near the source terminal. Namely, more holes need to be generated (meaning higher V_{Gf}) for lowering the threshold voltage. In transistors shorter than 100 nm, the proximity of the junctions inhibits the conservation of the positive charge in the body and therefore the GIFBE peak vanishes.

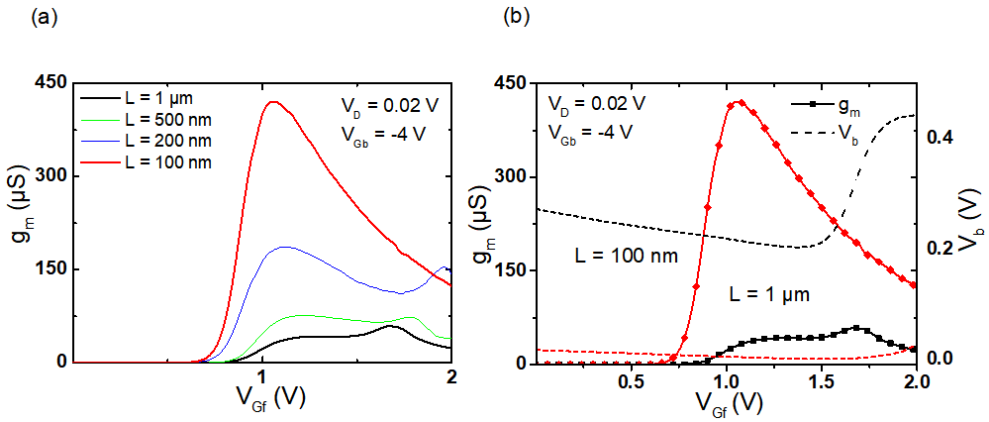


Figure 2.31: (a) Transconductance versus gate voltage measured for different gate lengths. (b) Correlation between transconductance g_m (plain symbols) and body potential V_b (dashed lines) in long and short MOSFETs. t_{BOX} = 25 nm, t_{ox} = 2.9 nm, V_D = 0.02 V, and L = 1 µm, 100 nm.

To acquire further insight, we have measured the variation of the body potential (Fig. 2.31b). In a long transistor (L = 1 µm), the GIFBE appears as soon as the body potential increases steadily following the accumulation of a sufficient number of excess holes. The GIFBE-peak bias corresponds to the inflection point of the potential curve. There is no such potential variation in the short device which clearly explains the absence of GIFBE. Figure 2.32 shows another way to correlate the GIFBE through measured gate current which includes the tunneling current. The transconductance and body potential variation begin to change after significantly increasing the gate current as indicated by blue arrows in Figure 2.32a, b.

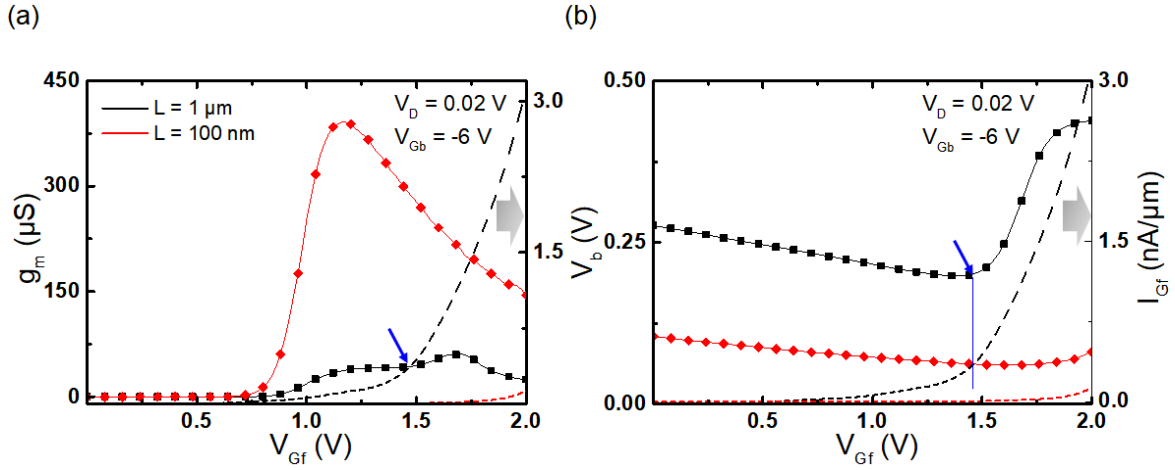


Figure 2.32: Gate current with (a) transconductance and (b) body potential as a function of V_{Gf}

A simple method to confirm that GIFBE originates from gate tunneling is to monitor the back-channel characteristics (Fig. 2.33a, b). The difference is that the buried oxide is very thick, which excludes any chance for the carriers to tunnel through. Even for negative front-gate bias, supposed to maintain holes if any, the transconductance exhibits classical behavior without a GIFBE peak.

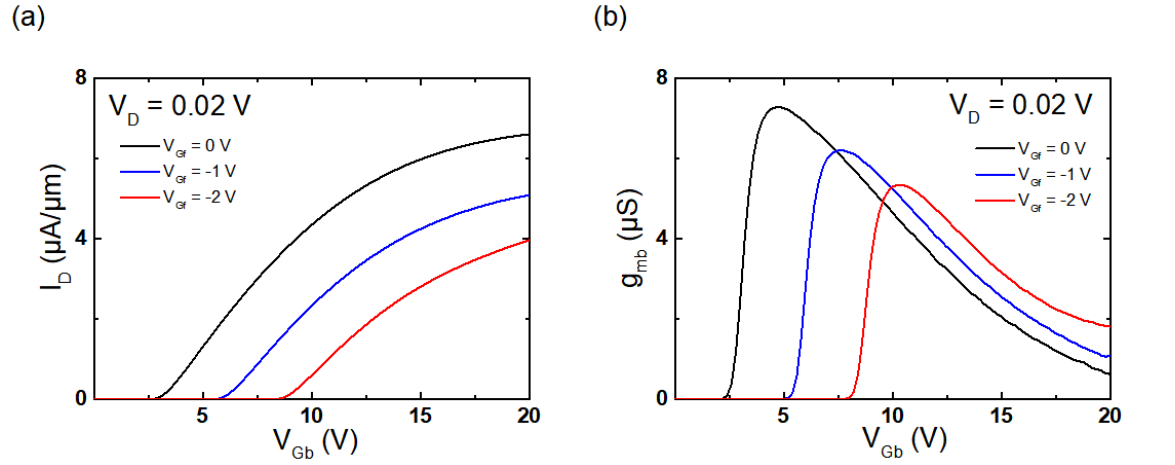


Figure 2.33: GIFBE-free back-channel characteristics. Drain current and transconductance g_m versus back-gate voltage for variable biasing of the front gate. t_{Si} = 25 nm. t_{BOX} = 25 nm, V_D = 0.02 V, and L = 1 µm.

2.3.3 Summary

In FDSOI MOSFET, we demonstrated that GIFBE is still revealed and observed at low drain voltage and strong inversion regime. The main reason is that the gate tunneling current through a thin oxide, *i.e.* < 2 nm, leaves excess holes within the silicon body. By doing this operation, the silicon body can be charged by majority carriers (holes). This is a critical cause of the immediate current boosting, therefore reflecting the second peak of g_m. The higher the negative substrate bias, the stronger the accumulation hole layer at the back interface, where the GIFBE is reinforced. Since the accumulated holes built up in the silicon, the body potential at the back interface is increased. Consequently, the raise of the body potential contributes to lower the threshold voltage of devices, thereby adding drain current. As long as the GIFBE is detectable from the transconductance g_m, this effect may be capable for current over-driving circuitries.

In the case when the second peak of g_m has higher values, the gate leakage current should be verified in terms of dielectric reliability for correct device operation. For the practical CMOS application using GIFBE, device and circuit engineers should take into account a proper thickness of the gate dielectric in order to prevent an anticipated malfunction due to the gate leakage current.

2.4 Parasitic Bipolar Transistor Effect

In general, the MOSFET structure encompasses a lateral NPN bipolar junction transistor (*BJT*) inherently, the activation on which relies on the forward biasing of the source-body (*i.e., emitter-base*) junction. The PBT effect was discussed by Sun et al., regarding the latch-up breakdown in a typical silicon device [36]. In addition, a study by Chen et al [37] proved that band-to-band tunneling (*BTBT*) can be amplified by the PBT in short channel SOI devices. Since then, the parasitic bipolar transistor (*PBT*) has been systematically investigated in partially-depleted SOI MOSFETs and reported by Reichert et al [38]. Particularly, Liu et al. have scrutinized the parasitic bipolar effect in ultrathin FDSOI MOSFETs in terms of holes generated by BTBT [19]. As long as the PBT effect appears in SOI MOSFETs, it has detrimental consequences on the linearity of I-V curve.

In this section, we focus on the parasitic bipolar amplification in ultrathin FDSOI MOSFETs. Based on experiments, the bipolar amplification will be clarified by changing drain voltages and back-gate conditions: accumulation, depletion, and inversion. Likewise, the ultrathin FDSOI MOSFETs

without the body contact have also put to activate the innate bipolar device owing to the accumulation of positive charges generated by impact ionization or BTBT. The parasitic bipolar transistor is noticeably effective in short devices as base narrowing of BJT. In an OFF state (V_{Gf} < 0), the MOS channel underneath the gate is unformed and the bipolar transistor current becomes more dominant.

2.4.1 Experimental Details

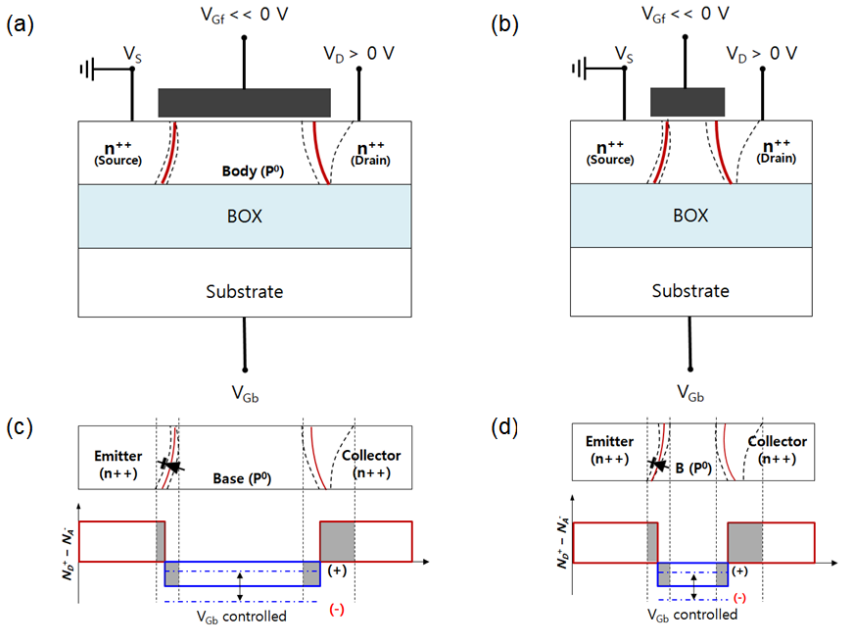


Figure 2.34: Schematic illustrations of a (a) long- and (b) short-channel FDSOI MOSFET, with corresponding BJT terminals: Emitter, Collector, and Base. For a (c) long base width, and (d) narrow base device.

Figure 2.34 shows the schematic illustrations of the FDSOI MOSFET and its intuitive internal junction's profiles near source and drain. It is analogous as a bipolar junction transistor (*BJT*). The source and drain terminals are regarded as emitter and collector in the BJT. The floating body can be acted as a base region of the parasitic BJT in order to control the current conduction in the device. We show current transfer characteristics for long- and short-channel FDSOI n-MOSFETs in an ultrathin film, t_{Si} = 8 nm. With applying different back-gate biases (for V_{Gb} = -5 V, 0 V, +5 V), the drain currents are measured as a function of the front-gate voltage from -1 V to +1.2 V.

When the negative gate bias is strong enough, for the off-state regime (V_{Gf} < 0 V), the *n*+ region under gate can become depleted, and even inverted. As soon as the surface near drain region is inverted, the leakage current increases due to the field crowding in the drain junction. This leakage current is called gate-induced drain leakage, or GIDL [39]. Indeed, the PBT amplification causes the GIDL current in ultrathin FDSOI MOSFETs.

2.4.2 Transfer Characteristics

Figures 2.35a,b show drain current characteristics of a long-channel n-MOSFET (L = 1 µm) in the thick silicon film (t_{Si} = 25 nm). In the negative region of the front-gate bias with V_{Gb} = 0 V, drain leakage currents are clearly increased with the drain bias. The leakage current is originating from the drain region with the negative front-gate voltage, i.e. GIDL. When the drain bias is higher than 0.5 V, the GIDL currents are increasing more rapidly and shifted to the right direction. This confirms the bipolar amplification effect in FDSOI MOSFETs [19]. In particular, bipolar amplification is significantly evidenced for positive back-gate bias (V_{Gb} = 5 V), where the leakage current is unacceptable (Fig. 2.35b).

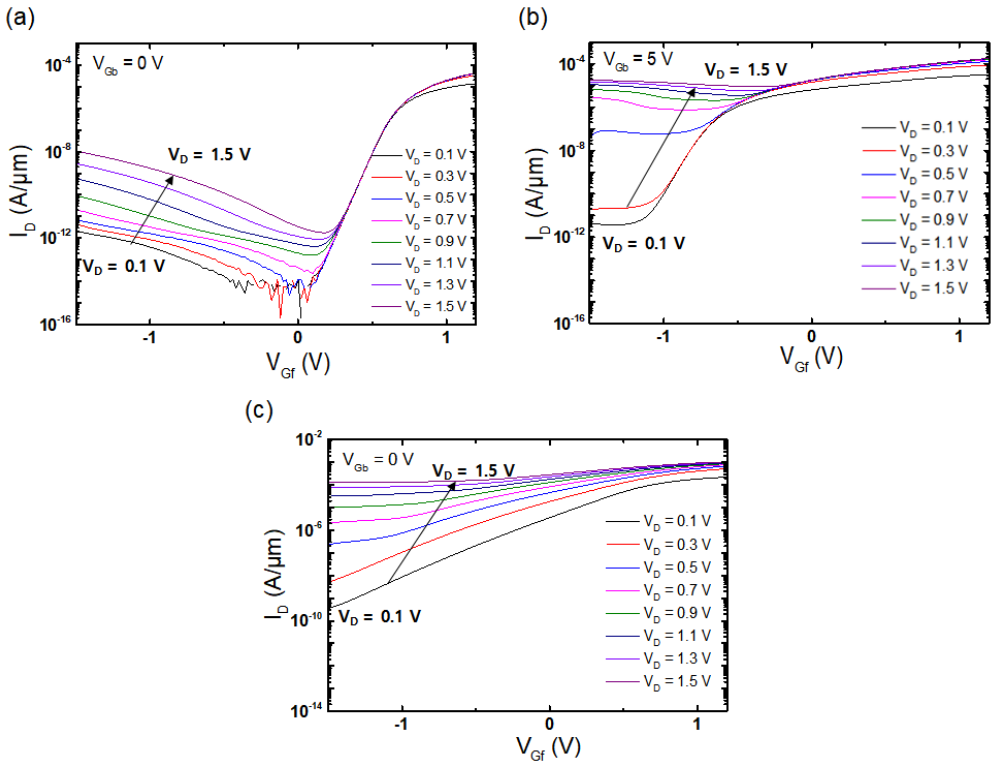


Figure 2.35: Experimental drain current characteristics in thicker FDSOI BCN MOSFETs, from low (0.1 V) to high drain bias (1.5 V), as a function of the front-gate voltage with different back-gate biases. Llong channel device (L = 1 µm) with (a) V_{Gb} = 0 V and (b) V_{Gb} = 5 V. Short channel device (L = 50 nm) with (c) V_{Gb} = 0 V. t_{Si} = t_{BOX} = 25 nm, W = 10 µm, L = 1 µm.

The short channel device (L = 50 nm) also presents an increase in the leakage current after applying V_D higher than 0.5 V as represented in Fig. 2.35c. For a long-channel (L = 1 µm) device in ultrathin typical FDSOI MOSFETs, there is no drain current amplification from the parasitic BJT component although the front-gate bias is negative and the drain bias is changed from 0.1 V to 1.5 V (Fig. 2.36). Namely, for an off-state condition (V_{Gf} < 0 V), the drain leakage current is normally

increased with drain bias as expected from pure GIDL effect.

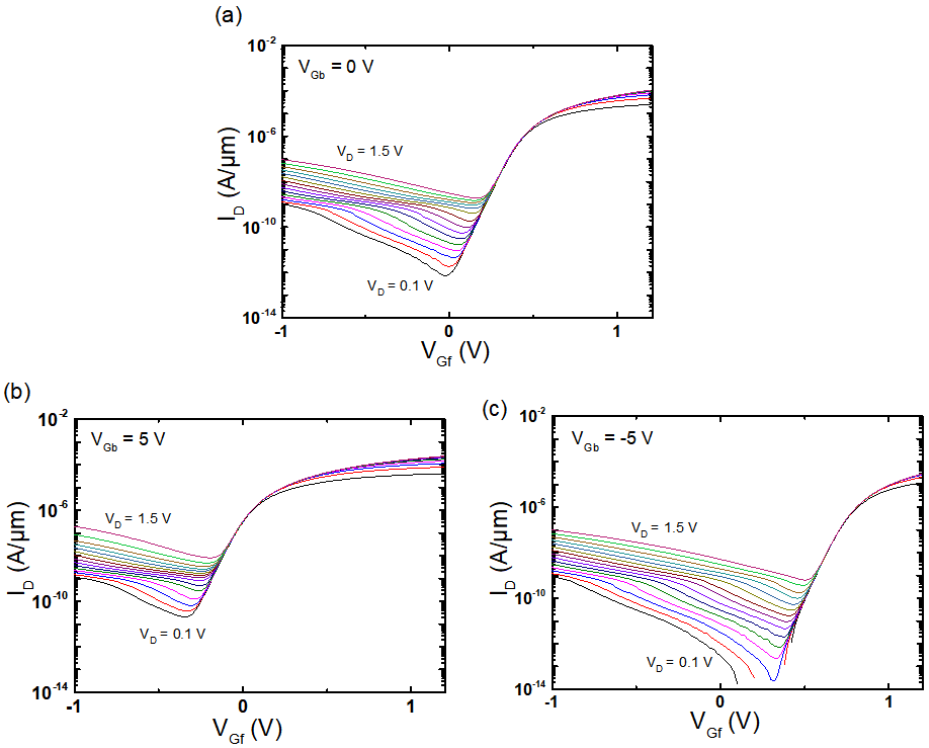


Figure 2.36: Experimental drain current characteristics, from low (0.1 V) to high drain bias (1.5 V), as a function of the front-gate voltage with different back-gate biases. (a) V_{Gb} = 0 V, (b) V_{Gb} = 5 V, and (c) V_{Gb} = -5 V, respectively. t_{Si} = 8 nm, t_{BOX} = 25 nm, W = 10 µm, L = 1 µm.

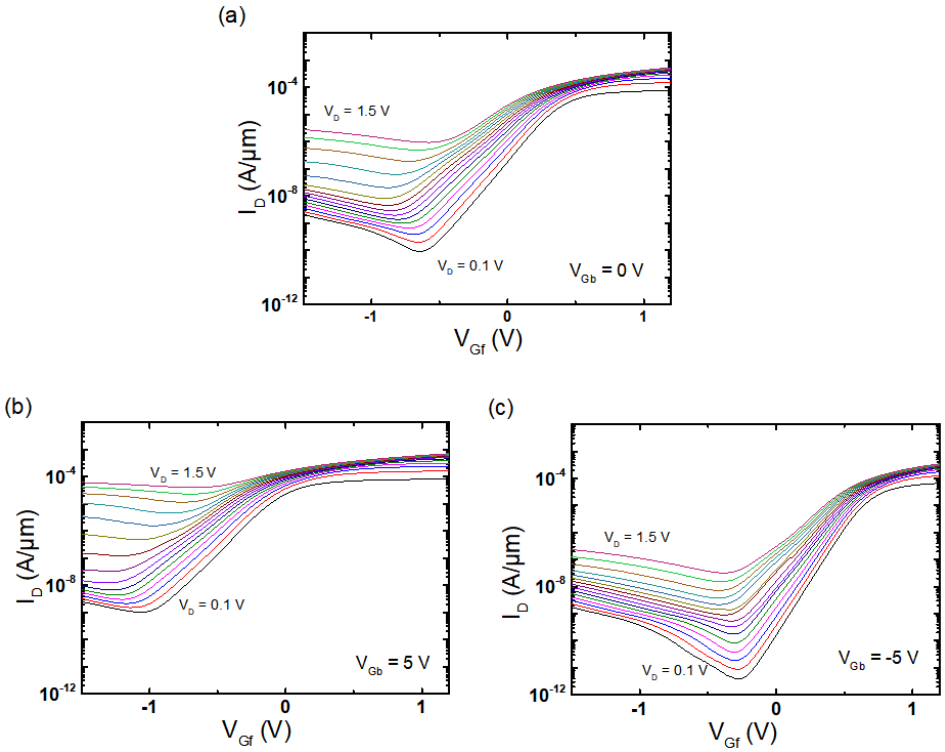


Figure 2.37: Experimental drain current characteristics for a short channel device with different back-gate biases (a) V_{Gb} = 0 V, (b) V_{Gb} = 5 V, and (c) V_{Gb} = -5 V. t_{Si} = 8 nm, t_{BOX} = 25 nm, W = 10 µm, L = 30 nm.

For a short device and V_D higher than 1 V, there is an explicit bipolar amplification of the GIDL current (Fig. 2.37a). This current amplification is attributed to the parasitic bipolar transistor effect. The PBT effect is even more clearly visible with positive V_{Gb}. In the case, the leakage current becomes unacceptable (Fig. 2.37b). The good news is that the drain leakage can be reduced by several orders of magnitude using the negative back-gate voltage (Fig. 2.37c). This result is astonishing given the fact that floating body effects are exacerbated by negative V_{Gb}. The reason is that a strange effect takes place: the increase of the injection barrier. The PBT effect is inhibited by the increase of barrier height at the body to the source junction thanks to the back-gate contribution [4], [5].

Liu et al. described the cause for the GIDL amplification using TCAD simulation with several models. The PBT is observed by activating the BTBT model. The holes densities for low and high V_D were also checked in the simulation. The body potential at the back interface increases with the drain voltage, from V_D = 0.2 V to 1.5 V. [19].

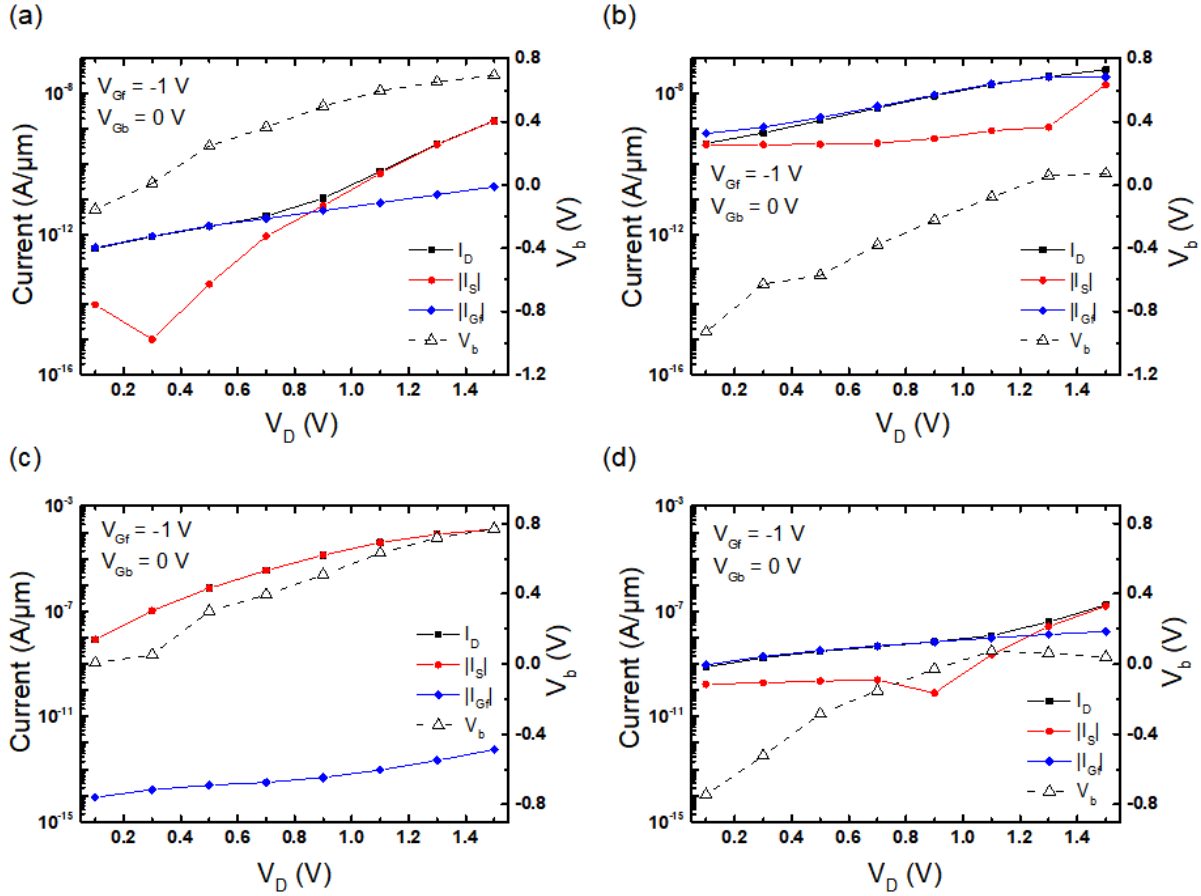


Figure 2.38: Comparison of drain, source, front-gate, and body potential measured from BCN MOSFETs with applying the front-gate (V_{Gf} = -1 V) and back-gate (V_{Gb} = 0 V) voltages. Drain voltages varied from 0.1 V to 1.5 V, respectively. For a long channel device (L_G = 1 µm) with (a) t_{Si} = 25 nm and (b) t_{Si} = 8 nm. For a short channel device (L_G = 50 nm) with (c) t_{Si} = 25 nm and (d) t_{Si} = 8 nm. V_{Gf} = -1 V, V_{Gb} = 0 V, t_{OX} = 2.9 nm, and t_{BOX} = 25 nm.

Figure 2.38 shows currents for drain, source, and front-gate at V_{Gf} = -1 V in a long channel (Fig. 2.38a, b) and short channel (Fig.2.38c, d) devices, experimentally. The back-gate current (I_{Gb}) is generally neglected because of thick buried oxide (BOX). For long and short channel devices, the source current (I_S) is less (or similar) than the drain current (I_D) when V_D is swept from 0.1 V to 1.5 V. For the long devices on thick (25 nm) and ultrathin film (8 nm), the source current (I_S) is lower than I_D due to the gate current contribution. The I_S of the ultrathin device is rather constant until reaching V_D higher than 1.3 V, whereas thicker device exponentially increased. Likewise, for the short channel devices, the I_S shows the same tendency as in long devices, being less different than I_D.

In order to clarify role of the holes generated by BTBT, body potential variation (V_b) is measured via a lateral *P+* contact in H-gate BCN MOSFET. Interestingly, for thicker devices (t_{Si} = 25 nm), the V_b is gradually increases, with the drain voltage from around 0 V to 0.8 V. For thin devices (t_{Si} = 8 nm), the V_b is constantly increased from -0.9 V to 0 V and then saturated. This implies that the holes injected by BTBT even at higher drain voltage are insufficient in the ultrathin film in order to modify the body potential.

2.4.3 Summary

The PBT effect was investigated in long- and short-channel FDSOI n-MOSFET. For the long channel device, there is an absence of the bipolar gain although the band-to-band tunneling current still exists (*GIDL contribution*). For the short channel device (L = 30 nm), we can see a remarkable increase of the leakage current with V_D as soon as the parasitic bipolar transistor is activated on. The PBT effect accentuates the GIDL current. The PBT effect can be deactivated with negative back-gate bias which helps increasing the emitter-base potential barrier. The thinning of the silicon body is required to eliminate or suppress the PBT effect. It finally disappears in a film thinner than 5 nm [19].

2.5 Sharp-Switching and Hysteresis Characteristics

Generally, the ideal value for the subthreshold slope (*or subthreshold swing, SS*) in MOSFETs is known as a 59.6 mV/dec at room temperature (*T = 300 K*). For bulk silicon MOSFETs, it is higher than ‘80 mV/dec’ whereas the FDSOI MOSFETs it is close to the theoretical limit of ‘60

mV/dec'. The SS is a critical indicator for the switching performance of MOSFET devices.

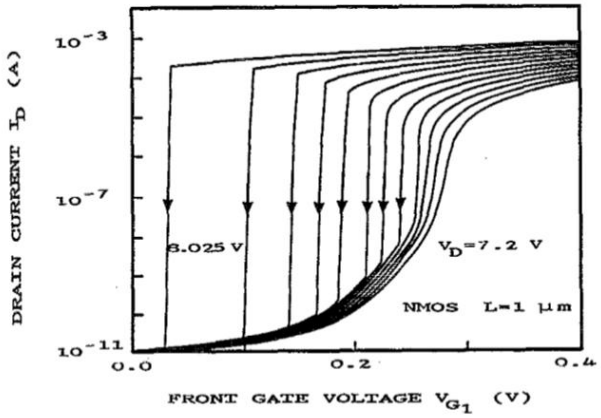


Figure 2.39: Experimental $I_D(V_G)$ characteristics showing the hysteresis-phenomenon in the n-channel SIMOX MOSFET. L = 1 µm, V_D = 7.2-8.025 V (step = 75 mV). The transients correspond to a negative gate voltage sweep [13].

In weak inversion, not only is the lateral field stronger for a given V_D but also the drain current depends exponentially on the body potential. For high drain voltages, the subthreshold characteristics $I_D(V_G)$ become S-shaped. This snapback effect is represented experimentally by a hysteresis with anomalously sharp subthreshold slopes (Fig. 2.39) [5].

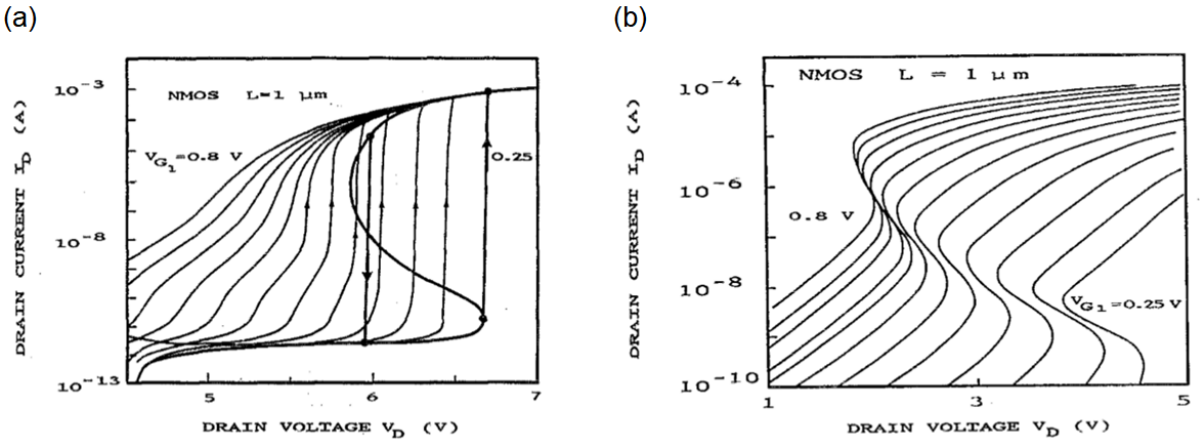


Figure 2.40: Experimental $I_D(V_D)$ characteristics showing the hysteresis-phenomenon measured by either (a) increasing the drain voltage or (b) by imposing the current [13].

Figure 2.40 shows $I_D(V_D)$ characteristics measured by imposing either the voltage or current. Sharp-switching feature and hysteresis are shown for different gate voltages as a function of drain bias. All curves correspond to a positive drain voltage sweep, except the bold solid lines (Fig. 2.40a). These curves reconstructed from current mode measurement indicate three possible current values for a given V_D. In order to avoid the spontaneous current oscillations, a high impedance load resistor is

helpful. Various groups have been proposed several approaches to duplicate the snapback effect [17], [40]. In the following section, a relevant experiment for supporting the sharp-switching (*or S-shape*) feature is conducted on recent FDSOI n-MOSFETs.

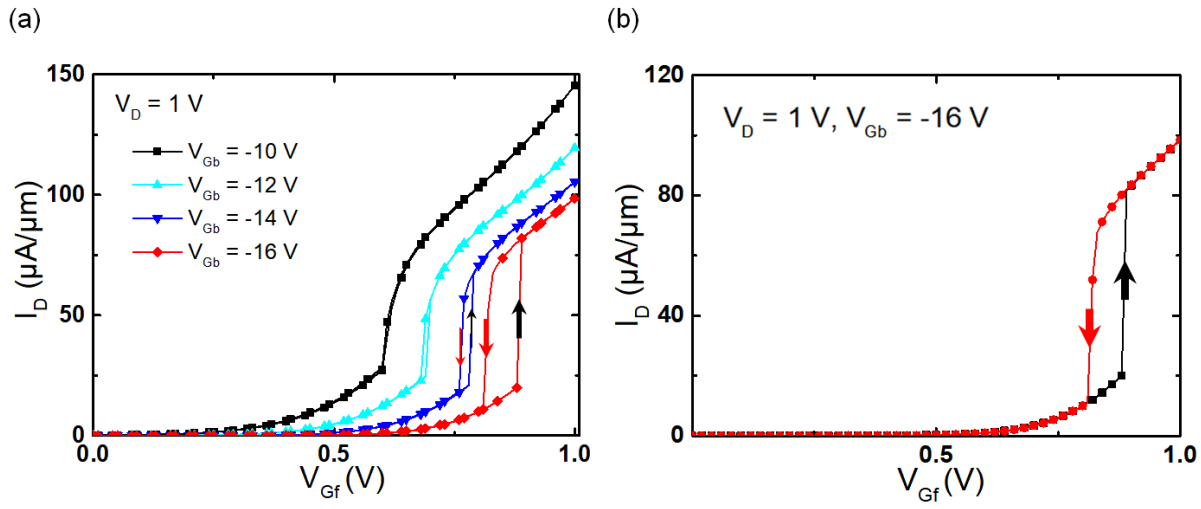


Figure 2.41: (a) Experimental $I_D(V_{Gf})$ characteristic of a normal FDSOI n-MOSFET measured for various negative back-gate biases. (b) Double sweeped curve highlighting the hysteresis and sharp switching behavior that occurred for V_{Gb} = -16 V and V_D = 1 V. t_{Si} = 25 nm, t_{BOX} = 25 nm, G_{ox} = 2.9 nm, W = 10 µm, L = 70 nm.

2.5.1 Steady-State Characteristics

For FDSOI MOSFETs, a sharp switching behavior can be achieved by combining impact ionization and the inter-gate coupling between back- and front-gate contributions. In a weak inversion condition, the current-voltage dependence is exponential and makes more visible small changes in body potential. With V_D in saturation, even at very low drain current, impact ionization takes place and supplies a modest number of holes that slightly increase the body potential. The resulting lowering of threshold voltage increases exponentially the density of channel electrons and the number of ionization events. Consequently, the body potential is raised further and therefore cascading more impact ionization. This positive feedback loop gives a rise as an abnormally sharp transfer characteristic with hysteresis (Fig. 2.41a). Detailed modeling shows that the hysteresis in DC curves is the manifestation of an S-shaped characteristic that can be measured by forcing the current [13].

Thick SOI MOSFETs are subject to transistor latch, meaning that they cannot be turned off. The positive holes charge stored in the floating body is sufficient to keep the electron channel turned ON even after the gate returns to a negative bias. In our FD-SOI MOSFETs, the latch effect could not be activated because the body charging is too weak. On the other hand, the hysteresis is not spontaneous and opens up only at high negative back-gate bias (Fig. 2.35a). In particular, for even large negative

V_{Gb} in Figure 2.41b, the hysteresis window is severely limited for the 25 nm thick device.

However, a key distinguished feature is that all transistors thinner than 10 nm are entirely restrained from latch, sharp switch and hysteresis. There are no positive holes charges maintained in the floating body in agreement with the super-coupling principle.

2.6 Transient and History Effect: Meta-Stable-Dip (MSD) Effect

Floating body, inter-gate coupling, and transient effects are all effective in SOI MOSFETs. In thin film devices based on FDSOI technology, the electrical characteristics are governed by competition in between front- and back-gate biases, and inter-gate coupling effect [4], [5], [13], [28]. Although FDSOI MOSFETs are deemed to be free from the classical FBEs, the silicon body is still left floating. The floating body allows us to obtain beneficial effects and interesting applications.

A new memory effect in FDSOI MOSFETs has been reported for the first time in [41]. It is a promising candidate for 1T-DRAM applications [42]–[45]. This effect is named meta-stable dip (*MSD*). The effect is mainly linked to the long carrier generation lifetime in the floating body. It also occurs at low drain voltage without any influence of the impact ionization. The MSD effect gives rise to a dip in transconductance g_m, when the front-gate voltage is scanned from negative to positive values (Fig. 2.42).

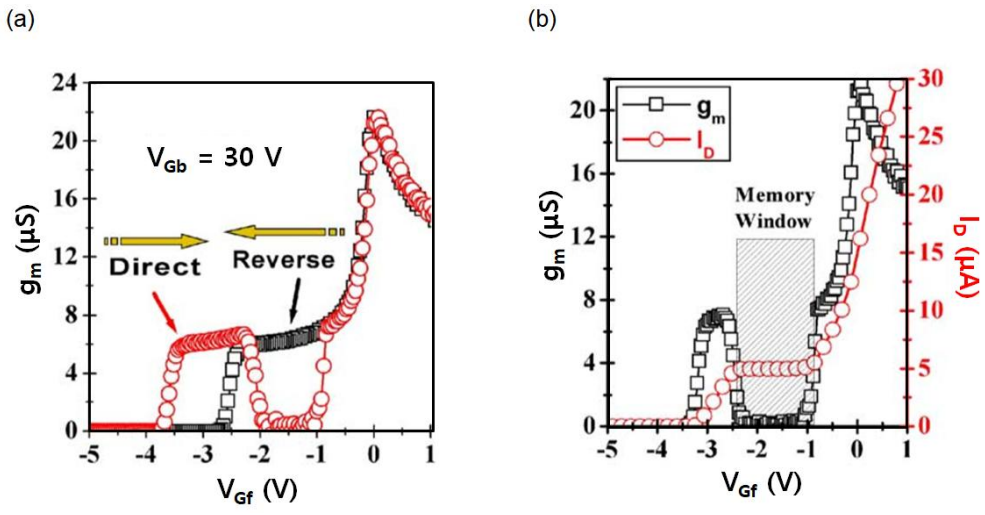


Fig. 2.42: Measured transconductance g_m versus decreasing (reverse scan; black symbol) and incrasing (direct scan; red symbol) of front-gate bias V_{Gf}. (a) $g_m(V_{Gf})$, (b) $g_m(V_{Gf})$ and drain current. V_D = 0.1 V, V_{Gb} = 20 V. t_{Si} = 80 nm, t_{BOX} = 400 nm, and t_{ox} = 10 nm [42].

2.6.1 Generic MSD features and a new memory effect

When the back interface is biased in the inversion mode (V_{Gb} = 20 V), a typical shape of the front-channel transconductance can be observed as demonstrated in Figure 2.42a. The front-gate voltage (V_{Gf}) is swept in two directions: from inversion to accumulation (reverse scan) or vice versa. For a direct scan of V_{Gf} (from accumulation to inversion), the transconductance shows a specific dip. The meta-stable-dip (MSD) was originally defined from this characteristic. As V_{Gf} increases in the direct scan, transconductance g_m begins to grow reflecting the back-channel activation through the interface coupling. The transconductance plateau corresponds to the linear decrease of the back-channel threshold voltage and current with the front-gate bias [35]. In the dip region (Fig. 2.42b), interface coupling stops and the back-channel current growth is blocked. The transconductance is therefore zero. After V_{Gf} increases beyond the voltage from which the front interface is accumulated, the g_m recovers a normal behavior [46]. For a reverse scan (Fig. 2.42a), the transconductance plateau is not affected by the MSD.

For memory applications, there are two distinguishable states: high or low current level. MSD features two different states by applying negative V_{Gf} (in the dip region) and controlling the front-gate sweeping direction. For reading data from the MSD memory cell, the drain current is measured in the dip region where the transconductance is zero or non-zero, respectively.

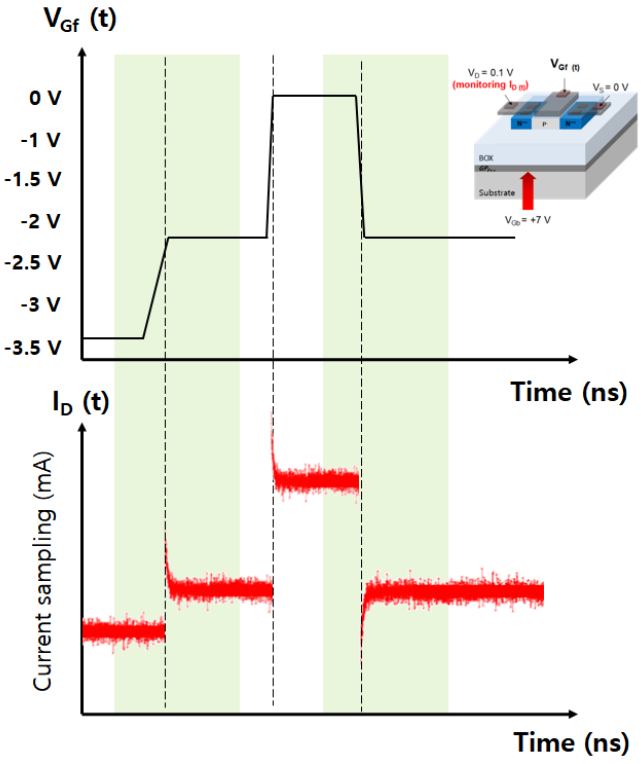


Fig. 2.43: Drain current sampling diagram with pulsed gate biases for measuring the transient current.

For examining the memory operation, transient measurements are performed in FDSOI MOSFETs. For this experiment, a current sampling mode is required to evaluate the transient current as a function of time (s). When the front-gate is biased in pulsed mode, the transient drain current is measured as depicted in Figure 2.43.

2.6.2 Transient Current Evaluation

A short channel FDSOI n-MOSFET, L = 60 nm and t_{Si} =t_{BOX} = 25 nm, was used for examining the transient effect and hysteresis. Figure 2.44 shows two cases for a FD-SOI transistor with the back-gate biased positively such as to induce a back-channel electron current. In Figure 2.44a, the front-gate is switched sharply from depletion or inversion into moderate accumulation (V_{Gf} : 0 to -2.2 V). Since no holes are immediately available, the body potential drops drastically by capacitive coupling, following the gate signal. This effect reminds the deep depletion mechanism well-known in MOS capacitors [33]. As a result, the threshold voltage of the back channel increases suddenly beyond the equilibrium value and the current is totally or partially suppressed, depending on V_{Gb} magnitude. Gradual generation of holes enables the current to increase with time (*undershoot*, in Fig. 2.44c) until it recovers the equilibrium value.

In the reciprocal situation (Fig. 2.44b), the front interface is initially set in strong accumulation state where higher negative gate bias (V_{Gf} = -3 V) activates *BTBT* at the gate corners. The tunneling process is able to supply the necessary amount of holes in the front channel for the transistor to be in equilibrium condition. However, as soon as the device is switched rapidly into the moderate accumulation (V_{Gf}: -3 to -2.2 V), almost all holes are maintained at the front interface although the gate bias is now insufficient to govern the overpopulation of the holes. As a result, the body potential is higher than that in equilibrium and the current decreases with time (*overshoot*) during the recombination of excess holes, as depicted in Fig. 2.44d.

In order to implement memory applications, this transient effect can be emulated as a capacitor for saving the information using the overpopulation of holes. Initially, for V_{Gb} = +7 V, the back interface has to be more or less in inversion state that makes the reference current level (I_{ref}) for the memory operation. For writing high-state (‘1’ data) with V_{Gf} = -3.5 V, plenty of holes created by BTBT are gathered at the front interface owing to the negative front gate bias. Those holes directly influence the back electron channel conduction because of increased body potential. The back-channel threshold voltage (V_{Tb}) is lower than in the non-equilibrium ‘0’ state. The back channel current (I_0) is enhanced progressively, whereas I_1 decreases with time. Both currents become equal (Fig. 2.46) when

equilibrium is reached. The retention time is estimated from the time needed to reach equilibrium (at V_{Gf} = *-2.2 V* in this case).

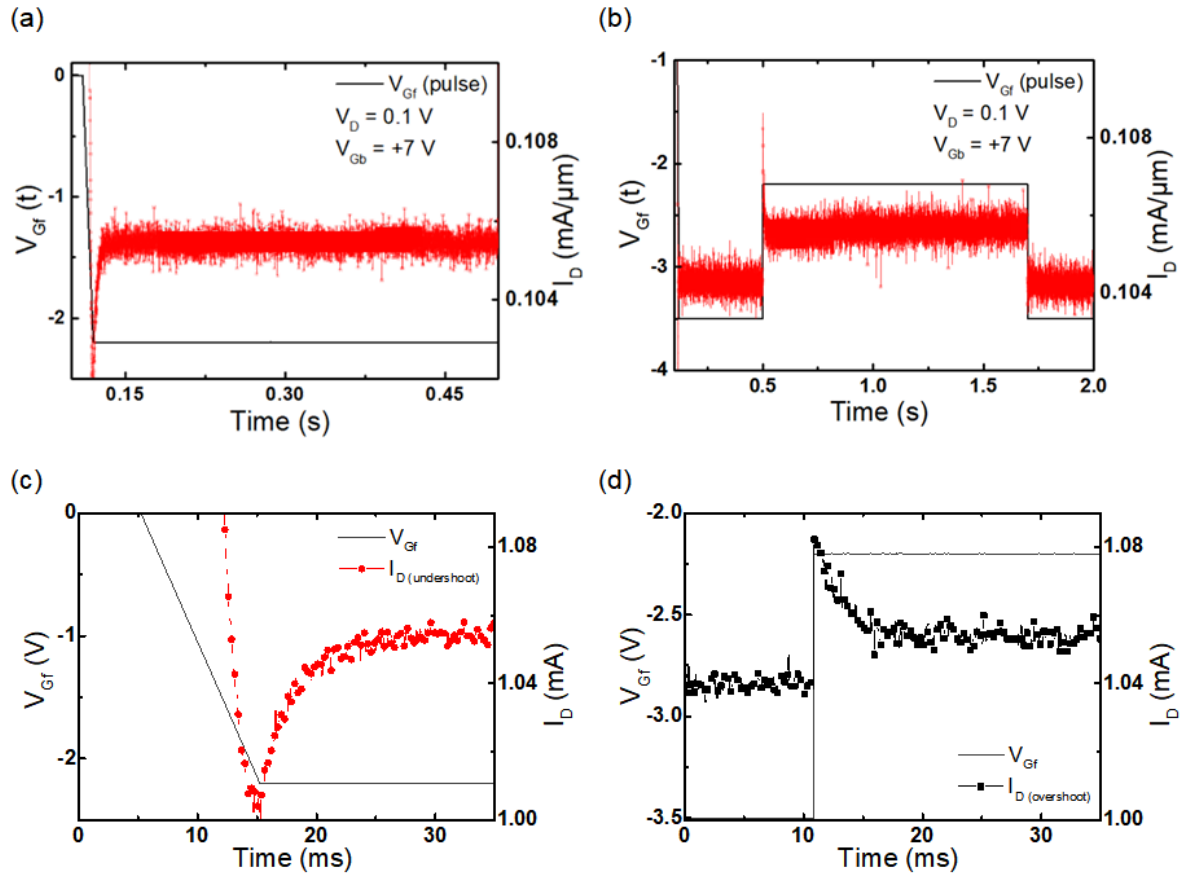


Fig. 2.44: Experimental transient currents measured in (a) undershoot condition with applying the V_{Gf} pulsed from 0 V to -2.2 V, and (b) overshoot condition: V_{Gf} pulsed from -3.5 V to -2.2 V. Zoom on the transient variations of drain current in the conditions of (c) undershoot and (d) overshoot. t_{Si} = 25 nm, t_{BOX} = 25 nm, W = 10 µm, L = 60 nm, V_D = 0.1 V, V_{Gb} = +7 V.

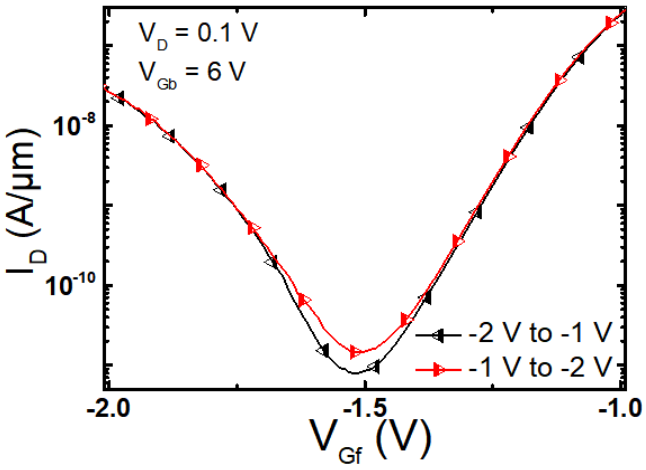


Fig. 2.45: Transfer characteristics in double sweep mode, showing a small hysteresis, which is inadequate for capacitor-less 1T-DRAM application. t_{Si} = 25 nm, t_{BOX} = 25 nm, W = 10 µm, L = 1 µm , V_D = 0.1 V, V_{Gb} = +6 V.

This transient effect, called Meta-Stable Dip (*MSD*) [25], also results in a hysteresis in $I_D(V_{Gf})$ curves (Fig. 2.45). Unfortunately, the MSD hysteresis shrinks with film thickness and is much weaker in ultrathin body than reported earlier for 80 nm film. The effect is totally suppressed in 8 nm thick films. The MSD originates from the coexistence of the electron inversion channel at the bottom interface with the holes accumulation channel at the front interface which, in ultrathin body, is negated by the super-coupling effect.

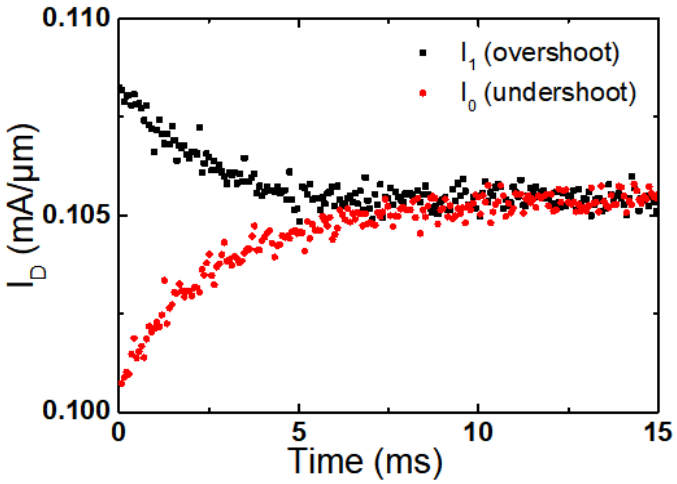


Fig. 2.46: Normalized transient currents, I_1 and I_0, overlaped on the same axis in order to determine the retention time. t_{Si} = 25 nm, t_{BOX} = 25 nm, W = 10 µm, L = 1 µm , V_D = 0.1 V, V_{Gb} = +6 V.

However, the retention time of two states is modest *(~10 ms*) and can be inappropriate for an application as capacitor-less floating-body memory (*MSDRAM*) application [47].

2.7 Conclusions

In this chapter, the floating-body effects (*FBEs*) have experimentally been revisited and scrutinized in advanced ultrathin FDSOI MOSFETs. Through the various experiments, we demonstrated that the FBEs were not spontaneous anymore without particular conditions such as back-gate biasing. We also proved that having silicon thickness less than 10 nm avoids the FBEs.

For the first time, the body potential variation was used to correlate the onset of the FBEs, especially the kink effect. The key point is that all of FBEs are originated from the interplay of the excess holes which are stored or eliminated in the floating body. We have measured directly the body

potential variation related to the excess holes. This measurement allows detailed information for FDSOI MOSFETs and its CMOS applications.

In the following chapter 3, we will demonstrate the dynamic body potential measurement in FDSOI MOSFETs and even in ultrathin devices.

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Chapter 3

Dynamic Body Potential Variation in Ultrathin FDSOI MOSFETs

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3.1 Introduction

Fully depleted SOI and multiple-gates MOSFETs are the best candidates for pushing transistor scaling beyond the 5 nm node. FDSOI MOSFETs are generally considered to be free from floating-body effects (*FBEs*) which affect Partial-depleted (*PD*) transistors [1]. In dynamic mode, body potential can temporarily escape the gate control, leading to several dynamic FBEs such as current overshoot and undershoot [2], gate-induced floating-body effect (*GIFBE*) [3], and Meta-Stable Dip (*MSD*) effect [4]. These dynamic FBEs enable pragmatic applications: development of capacitor-less 1T DRAM [5], EEPROM programming and history effects in integrated circuits.

In ultrathin FDSOI MOSFETs, the dynamic body potential variation gives us practical information on the majority carriers in the thin body. Bawedin *et al.* have mainly investigated the dynamic variation of the body potential via systematical measurements and numerical simulations [6]. The transient FBEs take place during particulars operation mode of SOI MOSFETs. For digital or analog circuit applications, the front-gate bias range roughly extends between the flat-band voltage and close to the threshold voltage. It means that front surface states vary from accumulation/depletion to strong inversion. The dynamic FBEs, however, may occur in lower bias range than the flat-band voltage for n-MOSFETs. For the capacitor-less DRAM, the dynamic FBEs are essentially relevant in terms of capacitive coupling in deep depletion ($V_G << V_{FB}$) and body charging by band-to-band (*B2B*) tunneling current.

Figure 3.1 shows experimental curves of gate current I_{Gf} and its corresponding body potential Φ_B variation. When the front-gate voltage is scanned from +0.5 V to -5 V value, a non-monotonous variation of the body potential (Fig. 3.1b) and the resulting gate current (Fig. 3.1a) are observed. In that particular case, the gate current corresponds to the displacement current induced by the voltage difference between the gate bias and the body potential.

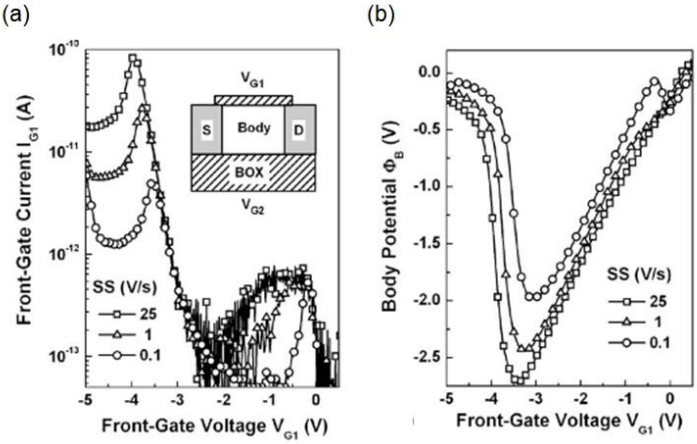

Figure 3.1: Measured dynamic (a) gate current I_{Gf} [6] *and (b) corresponding body potential Φ_B versus a decreasing front-gate voltage V_{Gf} scanned from depletion to accumulation in a PD SOI n-MOSFET. Scan speed (Ss) is varied from 0.1 to 25 V/s. t_{ox} = 4 nm, t_{Si} = 100 nm, t_{BOX} = 400 nm, and L_G = 1 µm. $V_D = V_S = V_{Gb}$ = 0 V.*

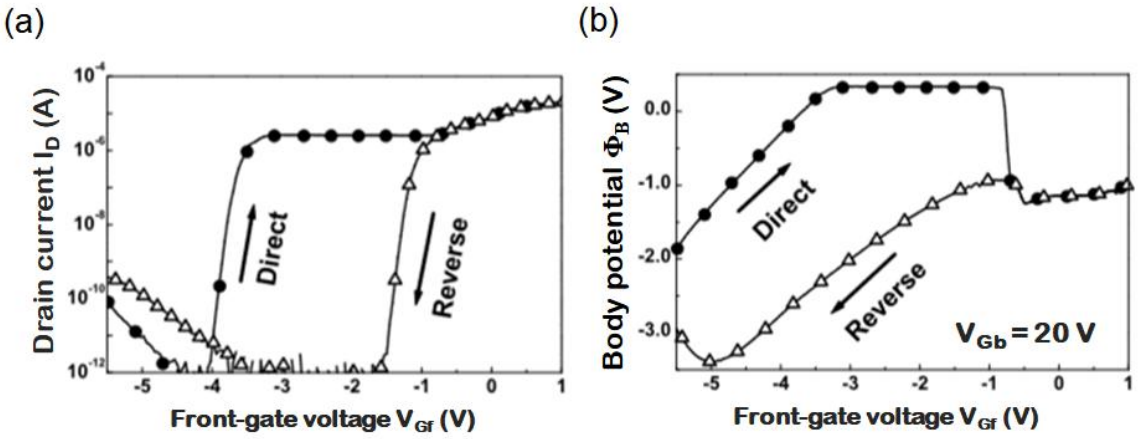

Figure 3.2: (a) The measured transient drain current I_D hysteresis (or meta-stable effect) resulting from (b) the transient body potential Φ_B variations for a SOI n-MOSFET. t_{ox} = 4 nm, t_{Si} = 100 nm, t_{BOX} = 400 nm, and L_G = 1 μm [6].

The specific drain current transfer characteristics (Fig. 3.2a) arise from the body potential variation (Fig.3.2b) and hence depend on the front-gate voltage V_{Gf} scan directions (direct or reverse). The transient gate current I_{Gf} (Fig. 3.1a) and the drain current I_D hysteresis are indeed revealed when the front- or back- interface potential moves between inversion/depletion and accumulation.

Note that the dynamic inter-gate coupling and the temporary lack of majority carriers are responsible for the particular behavior of the body potential Φ_B showed in Figure 3.2b. These body potential variations produce specific current characteristics (Fig. 3.1a, Fig. 3.2a). The principles of the 1T-DRAM memory, i.e., the Meta-Stable DRAM (MSDRAM [5]), originate from the MSD effect.

In the following section, we investigate and measure the body potential V_b variations in ultrathin (8 nm < t_{Si} < 25 nm) FDSOI n-MOSFETs with body contacted (BCN). Furthermore, a new method for determining the front and back channel built-up will be proposed by measuring V_b and its derivative.

3.2 Body Potential Measurement in Non-Equilibrium

In general, measuring the body potential V_b variation in floating-body devices is impossible without physical connection to the body. Thus, specific structures with body contacts were used to monitor the V_b of the floating body potential. The body contacted device is illustrated in Figure 3.3. It consists of a heavily doped P^+ region connected to the undoped silicon body underneath the front-gate.

These devices were initially designed to monitor the body current (majority carrier generation) but also were used as a lateral bipolar transistor: the P^+ region is a base contact; the source and drain correspond to the emitter and collector [7]. If the body contact is grounded, any floating body effects (*FBEs*) are efficiently eliminated because the excess or lack of majority carriers (holes) inside the body are instantaneously balanced (expelled or provided) by/trough the grounded body terminals.

For the first time, thanks to the availability of the P^+ body contact, the body potential V_b variation evidences the impact of majority carrier accumulation in the floating body correlated with the onset of FBEs: kink effect, gate-induced FBEs, and parasitic bipolar transistor effect. Several experimental results are demonstrated in section 3.2.3.

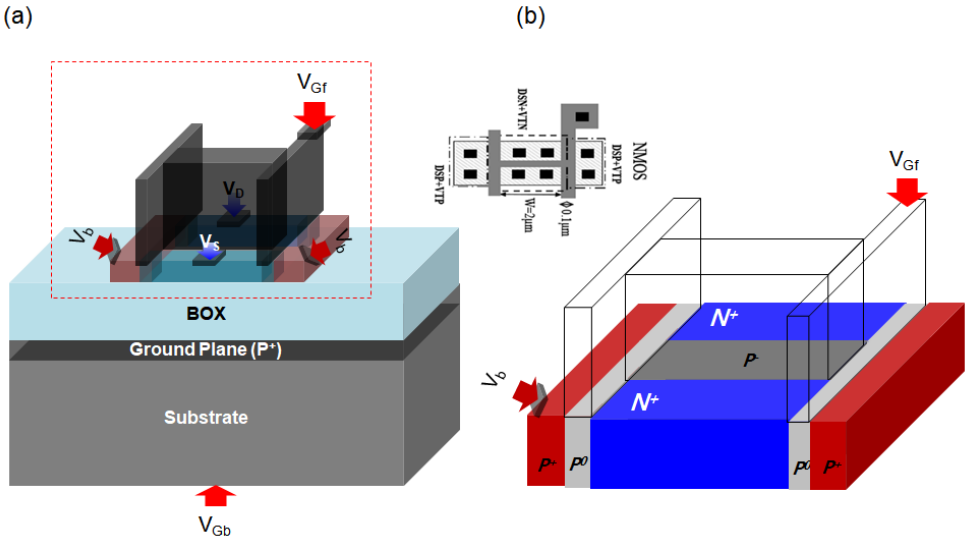

Figure 3.3: (a) Schematic of an H-gate body contacted n-MOSFET (BCN) fabricated in the 28 nm FDSOI. (b) Zoom of the lateral side of the BCN device.

3.2.1 Experimental Details

Device Parameters				Terminal Voltage Ranges		
t_{Si} (nm)	BOX (nm)	t_{ox} (nm)	L_G (µm)	V_D (V)	V_{Gf} (V)	V_{Gb} (V)
8	25	G_{o1} (1.5 nm)	1	0, 0.02, 0.2	0 – 1.2 (ΔV = 20 mV)	+10, +8, +6, +4, +2, 0, -2, -4, -6, -8, -10
			0.1			
			0.05			
12			1		0 – 1.5 (ΔV = 20 mV)	
			0.1			
25		G_{o2} (2.9 nm)	5		-5 to 0 V, 0 – 2.0 (ΔV = 20 mV)	
			1			
			0.1			
			0.05			

Table 3.1: Device parameters of BCN MOSFETs and terminal voltage range for the body potential measurement.

The H-gate body contact n-MOSFET offers five terminals: front- and back-gate, source, drain, and P^+ body contact. The main physical parameters of the BCN devices are presented in Table 3.1. The body potential V_b is measured by setting a source measurement unit (SMU[1]) in a zero current source mode (I_b = 0 A). Note that the V_b measurement setup guarantees extremely low leakage currents during the body potential probing, preventing any perturbation of the device behavior.

3.2.2 DC Characteristics of Body Contact n-MOSFET

Typical $I_D(V_{Gf})$ characteristic of a long channel BCN MOSFET is represented in Figure 3.4. Threshold voltage V_T is controlled by adjusting the back-gate bias thanks to inter-gate coupling [8].

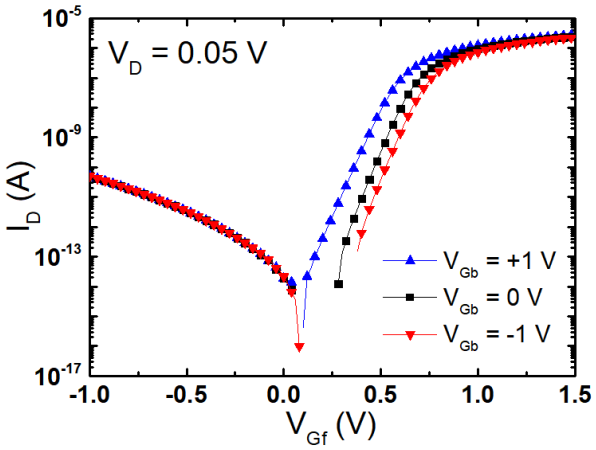

Figure 3.4: Typical $I_D(V_{Gf})$ characteristics with back-gate biases: V_{Gb} = -1 V, 0 V, and +1 V. t_{Si} = t_{BOX} = 25 nm, t_{ox} = 2.9 nm and L_G = 5 µm. V_D =0.05 V, V_{Gb} = +1, 0, -1 V, respectively.

When the front-gate voltage V_{Gf} is such as the front interface is in strong accumulation mode, the body potential will be influenced by the density of holes. The main relevant holes generation mechanism is induced by band-to-band tunneling at the overlap region between gate and drain. Another source of holes could be the drift-diffusion current if the body-drain junction is in reverse mode.

While V_{Gf} decreases from 0 V to negative values (Fig. 3.4), an increase of drain current can be observed. This increase is caused by the gate induced drain leakage (*GIDL*). There is also channel coupling between the front- and back-interface. Generally, steady-state coupling can be preserved as long as V_{Gf} remains higher than the front flat-band voltage V_{FB}. Once V_{Gf} becomes lower ($V_{Gf} < V_{FB}$), the body potential is driven by two main contributions: (i) the dynamic inter-gate coupling and (ii) the

[1] B1500 Keysight Analyzer

majority carrier generation-recombination (lack or excess of carriers regarding equilibrium). Depending of the gate bias sweep speed, when V_{Gf} is scanned from inversion/depletion into accumulation, the body potential keeps decreasing following the front-gate voltage if the majority carrier generation is not efficient enough to build the accumulation layer. Therefore, the whole body may enter into the deep depletion in the non-equilibrium regime. Since the front interface cannot accumulate holes instantly, the potential drop over the body arises from the capacitive coupling among the two gates (front and back) [6].

Figure 3.5 shows typical drain current I_D as a function of the front-gate bias with drain bias, V_D = 0.05 V and 0.1 V, respectively. Figure 3.6 presents the gate current and body potential variation obtained when the gate bias is scanned from inversion to accumulation (all other terminals being grounded). The body potential shows a V-shaped behavior with a minimum value (Fig. 3.6b) corresponding to the inflection region of gate leakage currents around V_{Gf} = -1.5 V, i.e. close to the front flat-band voltage (Fig. 3.6a). The gate current variation visible when the gate bias is swept in the depletion regime (-1.5 V < V_{Gf} < 0 V) may be attributed to the displacement current originating mainly from the body potential variation ($I = C \cdot \frac{d(V_{Gf}-V_b)}{dt}$).

Note that in this bias range, the I_{Gf} variations cannot be attributed to the holes current generated by the BTBT. The point where the body potential starts to increase indicates that the holes needed to build the front accumulation layer are steadily provided. At this stage, we can reasonably assume that the BTBT becomes more dominant than the charge supplied by the drift-diffusion current. Therefore, when V_{Gf} < -1.5 V, an increase of V_b is observed (Fig. 3.6b). As far as the BTBT generation provides holes into the body, the total hole-density required for steady state can be exceeded. Thus V_b begins rising consequently (Fig. 3.6b).

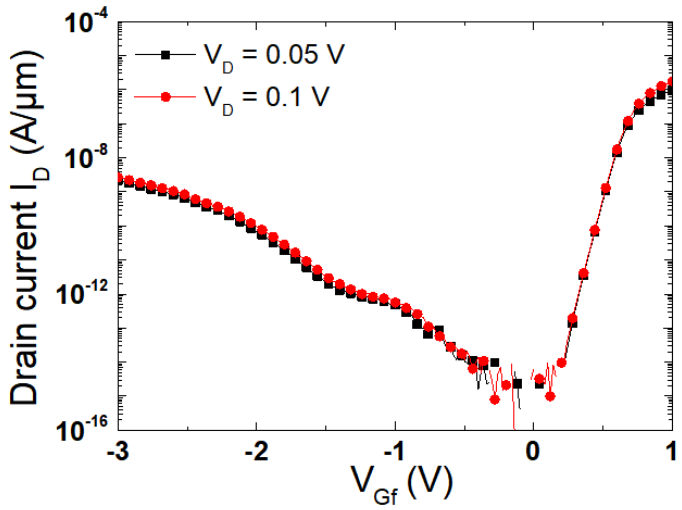

Figure 3.5: Typical drain currents measured with drain bias, V_D = 0.05 V, 0.1 V. t_{Si} = t_{BOX} = 25 nm, t_{ox} = 2.9 nm and L_G = 5 μm.

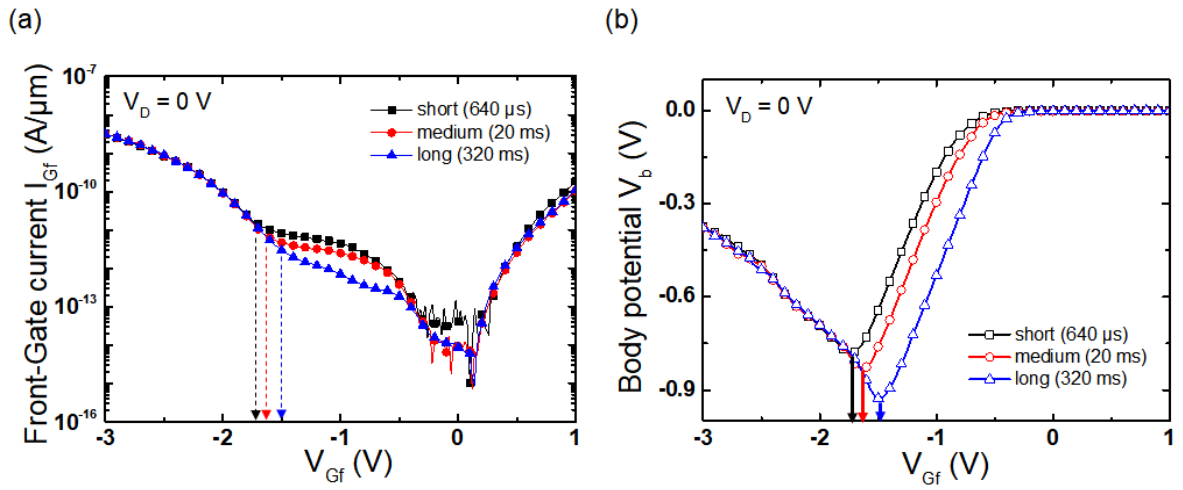

Figure 3.6: Measured (a) front-gate current I_{Gf} and (b) body potential V_b versus the front-gate voltage. The front-gate V_{Gf} sweeps from inversion (or depletion) to accumulation mode, from 1 V to -3 V. t_{Si} = t_{BOX} = 25 nm, t_{ox} = 2.9 nm and L_G = 5 μm. V_D = V_S = V_{Gb} = 0 V.

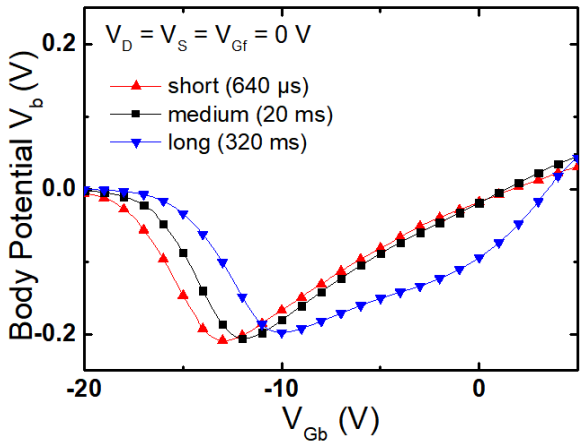

Figure 3.7: Measured V_b during sweeping back-gate V_{Gb} from inversion to accumulation. t_{Si} = t_{BOX} = 25 nm, t_{ox} = 2.9 nm and L_G = 5 μm. V_D = V_S = V_{Gf} = 0 V.

For further information, the V_b variation is demonstrated as a function of back-gate bias in Figure 3.7. A similar behavior is observed when the back-gate bias is scanned from inversion to accumulation. Note that for the long integration sweep time, the body potential variation linearity is jeopardized. Up to now, we can only suppose that this phenomenon is due to unexpected majority carrier generation, but its origin needs to be further clarified.

3.2.3 Correlation with FBEs

For the first time, we investigate the relationship between body potential variation and the onset

of FBEs. Dedicated experiments (revisiting kink effect, gate induced FBE, parasitic bipolar transistor effect) and TCAD simulation were conducted in order to identify the role of majority carriers (hole) for the FBEs.

In this section, the V_b variation measurement provides us with the experimental supplements of FBEs in I_D (V_{Gf} or V_D) characteristics.

A. Kink Effect

The kink-effect is one of the most classical floating-body effects in partially-depleted SOI MOSFETs: majority carriers are generated by impact ionization and stored within the body, lowering the threshold voltage (see chapter 2).

Figure 3.8 shows $I_D(V_D)$ and body potential V_b (empty symbols) variation in the same plot. For a thick n-MOSFET (t_{Si} = 25 nm) with negative back-gate bias (V_{Gb} = -6 V, red curves), V_b changes at a point where the drain current increases due to the kink effect (Fig. 3.8a). At this point, the excess-holes generated by impact ionization in the drain-body junction are accumulated/stored in the body; thereby we note the sudden increase of body potential. However, in a thinner silicon body the potential is not significantly changed in spite of the higher negative back-gate voltage (V_{Gb} = -6). It evidences that the holes cannot be stored in the body. These holes are steadily evacuated through the source-body junction or eventually recombined with the electrons of the front inversion layer. The V_b is unchanged as demonstrated in Figure 3.8b. According to this result, we can confirm the influence of the "super-coupling effect" stating that below a critical silicon film thickness both inversion and accumulation layers at opposite interfaces cannot coexist [9].

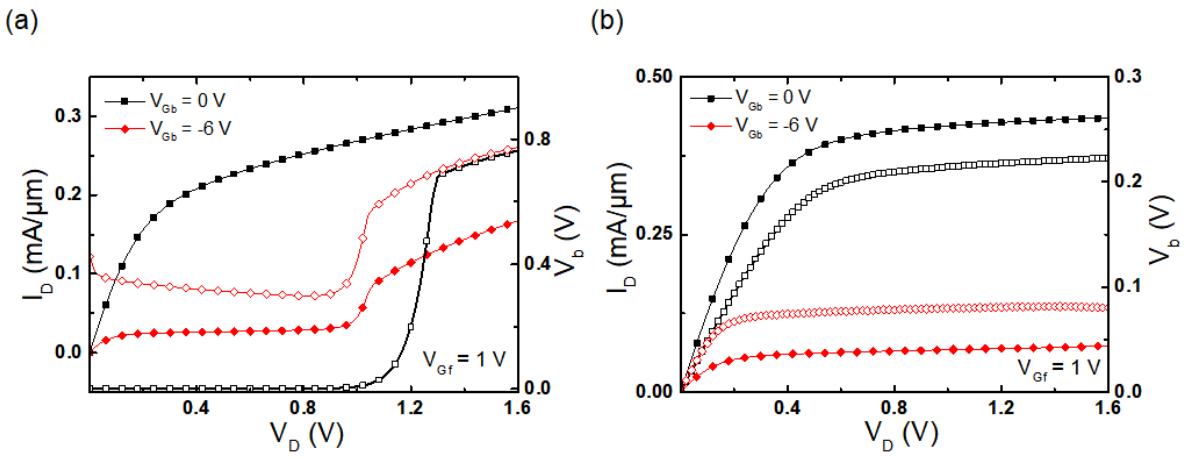

Figure 3.8: I_D (V_D) characteristics with measured body potential variation in (a) a thick (t_{Si} = 25 nm) and (b) an ultrathin (t_{Si} = 8 nm) MOSFET. t_{BOX} = 25 nm, t_{ox} = 2.9 nm and L_G = 100 nm. V_{Gf} = 1 V and V_{Gb} =0, -6 V.

B. Gate-Induced Floating Body Effect (GIFBE)

In FDSOI MOSFETs with thin gate dielectric (< 2 nm), the floating body can be charged by the gate current. Direct tunneling of electrons from the valence band of the body into the gate leaves excess holes in the body [3], [10]. This effect is called gate-induced floating body effect (GIFBE, see chapter 2). The GIFBE is measured at low drain voltage which excludes any contribution from impact ionization. The excess holes created by the direct tunneling can be detected through the change of V_b. Figure 3.9 represents the drain current I_D, transconductance g_m, and body potential variation V_b as a function of V_{Gf}. Through the V_b variation measurements (as it was usually performed using the drain current characteristics), the GIFBE can also obviously be observed as soon as the body potential increases steadily owing to the accumulation of the excess holes. The GIFBE-peak bias corresponds to the inflection point of the body potential curve. This is correlated to the change of the slope of drain current (see the black bold curve inside the dashed circle). In a plot of the transconductance g_m, it corresponds to the second peak (see the blue bold curve). This implies that direct tunneling of valence band electrons from the silicon body into the gate leaves an excess of holes in the floating body. This excess of holes lowers the threshold voltage and increases drain current I_D drastically similarly to the kink effect.

In order to obtain further insight about the V_b variation, gate current I_{Gf} is also measured precisely via high-resolution (HR) probe unit. Figure 3.10 shows the measured gate current I_{Gf} that increases when the slope of V_b variation. It is worth noting that the increase of I_{Gf} simultaneously with the V_b variation corroborates the fact that the gate current origin is direct tunneling current (electrons coming from the valence band in the silicon at the body/gate interface). Indeed, the V_b variation reflects the change of the majority carrier holes population in the floating body.

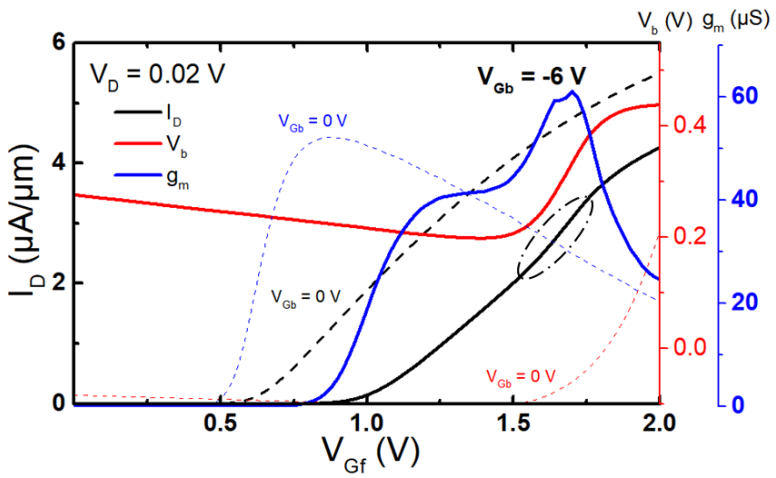

Figure 3.9: Measured I_D, V_b, and g_m with low drain voltage (V_D = 0.02 V). Correlation with between transconductance g_m (blue curve) and body potential V_b variation (red curve) in long channel MOSFET during sweeping back-gate V_{Gb}. $t_{Si} = t_{BOX}$ = 25 nm, t_{ox} = 2.9 nm and L_G = 1 µm. V_D = 0.02 V, V_{Gb} = 0 V and -6 V.

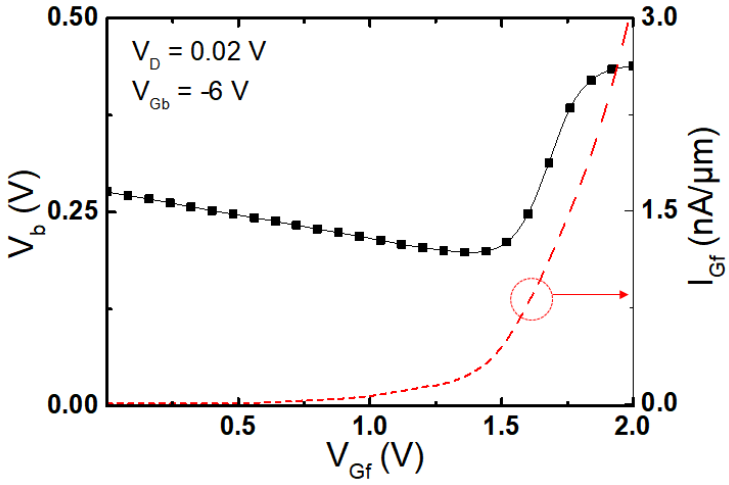

Figure 3.10: Correlation between measured V_b and gate current I_{Gf} versus front-gate bias. t_{Si} = t_{BOX} = 25 nm, t_{ox} = 2.9 nm and L_G = 1 μm. V_D = 0.02 V, V_{Gb} = -6 V.

C. Parasitic Bipolar Transistor (PBT) Effect

In general, a lateral NPN bipolar transistor is inherent in MOSFETs, the activation of which relies on the forward biasing of the source-body (*i.e.*, emitter-base) junction. Although FDSOI MOSFETs have no connection to the silicon body, the emitter-base junction can be mildly forward-biased thanks to the accumulation of positive charges (majority carriers) generated by impact ionization or BTBT [7], [11]. The parasitic bipolar transistor is effective in short (narrow base) MOSFETs, where the bipolar gain is high, and contributes to the total current. In the OFF state (V_{Gf} < 0), the MOS channel is blocked and the bipolar current becomes more pronounced (see chapter 2 for details).

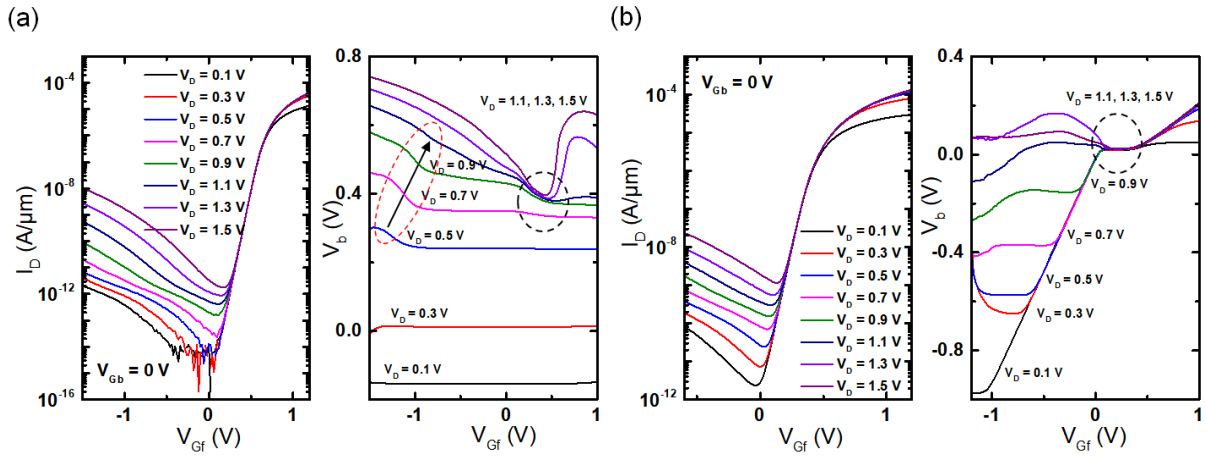

Figure 3.11: I_D (V_{Gf}) characteristics and the V_b variation, with drain voltage V_D changed from 0.1 V to 1.5 V, respectively. For (a) a thick, t_{Si} = 25 nm and (b) an ultrathin BCN MOSFET versus the front-gate V_{Gf} bias, t_{Si} = 8 nm. t_{BOX} = 25 nm, t_{ox} = 2.9 nm and L_G = 1 μm. V_{Gb} = 0 V, V_D = 0.1 to 1.5 V (step = 0.2 V).

The V_b variation is measured to confirm the PBT first in thick BCN MOSFETs with t_{Si} = 25 nm. The drain current I_D (I_{off} related to GIDL effect at V_{Gf} < 0 V) is steadily increased when increasing drain voltage V_D beyond 0.5 V as demonstrated in Figure 3.11a. At the same time, the V_b variation remains more or less flat or slightly increases when V_D is lower than 0.5 V (right panel in Figure 3.11a).

Remarkably, for V_D higher than 0.5 V, there are two obvious different behaviors of the V_b variation. One is where the magnitude of V_b is gradually increased with high drain bias and the rising points are shifted to the right (red dashed circle in Fig. 3.11a). The other is where the first increasing point of V_b is pinned for V_{Gf} values near 0.45 V (V_D > 0.9 V, black dashed circle).

Conversely, for the ultrathin BCN MOSFETs, there is no longer existence of the PBT even at higher drain voltage V_D (Fig. 3.11b). The V_b variation also shows different behavior compared with the thick MOSFETs. For V_D less than 1.1 V, the V_b at V_{Gf} = -1 V shows negative values and almost a tendency to decrease. It means that excess holes generated by the BTBT are ineffective in ultrathin FDSOI MOSFETs because of the lower barrier at the source junction.

3.3 Gate coupling characterization in ultra-thin film revisited by body potential measurements

3.3.1 Introduction

In an ultrathin FDSOI MOSFETs, there is a coupling effect between front- and back-gate called supercoupling effect which restricts the co-existence of electrons and holes in ultrathin semiconductor films [12]. Figure 3.11 depicts the charge distribution in thick (a) and thin (b) film under same bias conditions.

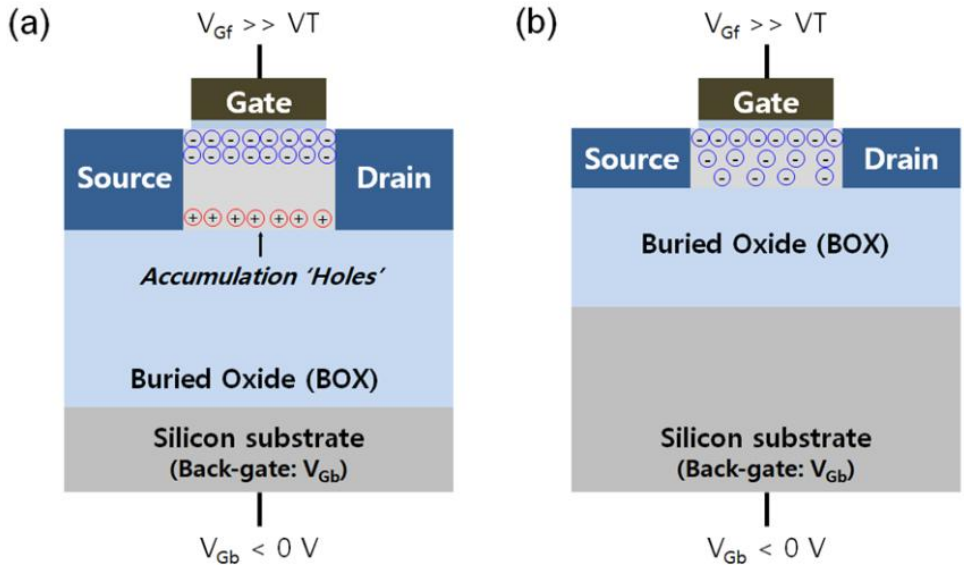

Figure 3.12: (a) Thick-body SOI MOSFET, showing co-existence of two carriers: electrons and holes. (b) Ultrathin body MOSFETs inhibits the presence of two carriers in the body, simultaneously.

When a positive bias is applied to the front-gate, an inversion layer is formed. If a negative bias is applied at the back-gate, depending of the thickness of the silicon film, a back accumulation hole layer can co-exist within the same body (Fig. 3.12a). In relatively thick films (t_{Si} > 20 nm), the two channels are clearly separated by a depletion region. The properties of either channel depend on the bias applied to the opposite gate; the inter-gate coupling effect may be beneficial for several applications where the two gate interact, *e.g.* dynamic threshold control and 1T-DRAM [13]–[15]. However, when a critical thickness is achieved (t_{Si} <～10 nm), the electron and hole layers cannot be formed simultaneously (Fig. 3.12b). The body of the transistor is filled with either electrons (volume inversion) or holes (volume accumulation), depending on the bias and polarity of the dominating gate.

A number of experimental results have pointed *indirectly* toward the supercoupling effect:

(i) Single-transistor capacitorless dynamic memory cells (1T-DRAM), which require the presence of holes and electrons in the body, show degraded properties as the film is thinner and eventually stop working [16].

(ii) The Electron-Hole Bilayer Tunneling Field-Effect Transistor (EHB-TFET) is based on two apparently contradictory requirements: (a) formation of distinct electron and hole layers and (b) very thin body such as to trigger vertical band-to-band tunneling [17], [18]. The concept is very attractive but it could not be demonstrated experimentally so far.

(iii) The linear variation of the electron-channel threshold voltage (V_{TN}) with the bias applied on the opposite gate stops when a hole accumulation channel is formed ($V_{Gb} < V_{TP} < 0$) [8]. The range of V_{TN} variation, used for performance tuning in ON and OFF regimes, expands in thinner films [19], indicating the increasing difficulty to build the hole channel. Experiments and simulations have also suggested that supercoupling is a 2-D size effect amplified in short devices.

(iv) The supercoupling effect was *directly* probed by using a four-gate FD SOI n-MOSFET (G^4-FET in Fig 3.13). This device has two independent lateral P+ contacts and typical N^+ source/drain contacts. It is demonstrated experimentally by measuring hole current (I_P) and electron current (I_N), respectively. In ultrathin body (t_{Si} = 7 nm), only the I_N or I_P can be detected thanks to the supercoupling effect [20].

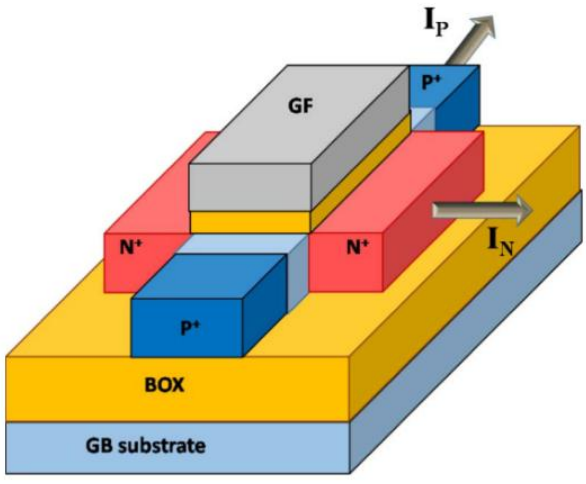

Figure 3.13: Schematic of four gates FDSOI n-MOSFET (G^4-FET).

In the following section, we present a new experimental evidence of the supercoupling effect using the body contact of an n-channel (BCN) MOSFET (Fig. 3.3). The body potential V_b variation in the ultrathin BCN MOSFET is measured to highlight whether or not two types of carriers (electrons and holes) can be accommodated in the thin body. In addition, we propose a new approach to extract the threshold voltage for ultrathin FDSOI MOSFETs (section 3.3.7).

3.3.2 Measurement setup

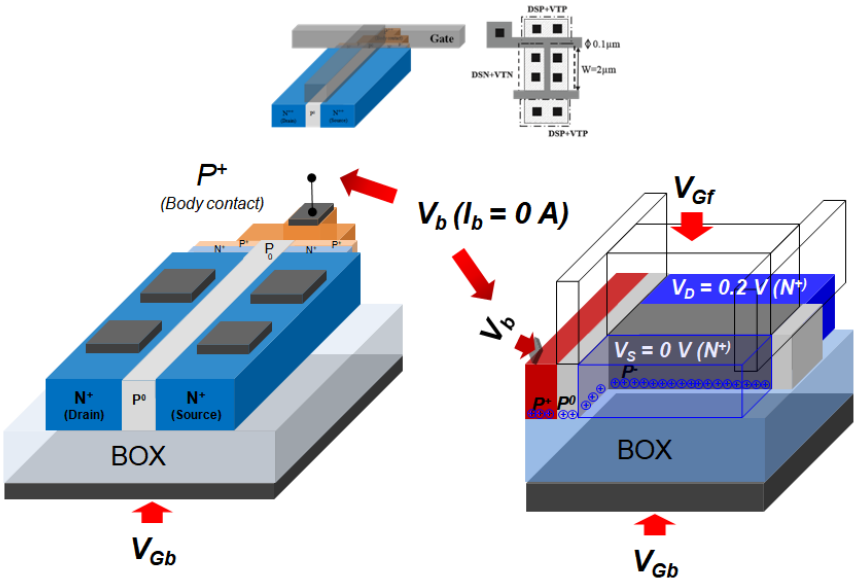

Figure 3.14: Schematic views of the H-gate FDSOI BCN MOSFETs.

Figure 3.14 shows the schematic of H-gate FDSOI BCN MOSFETs with different 3D views. The BCN MOSFETs are used for *in-situ* measurement of the body potential. The test equipment comprises an Agilent B1500 analyzer and a dedicated probe station. In particular, for measuring the internal voltage of the body, the probe is set the current source mode where the body current (I_b) can be controlled. By setting the value of I_b to 0 A, the probe connected to body contact can measure the voltage owing to high impedance value of the system (I_{bc} = 0 A).

Systematic measurements were performed on recent generations of FD-SOI transistors fabricated in CEA-Leti and STMicroelectronics. The silicon film thickness t_{Si} varies from 8 nm to 25 nm and the buried oxide (BOX) is 25 nm thick. The silicon layer was left undoped ($N_A \sim 10^{15}$ cm^{-3}). The FDSOI process includes a high-k/metal gate stack with thin (1.5 nm) or thick (2.9 nm) dielectric. A back-gate voltage V_{Gb}, ranging maximum from +15 V to -15 V to avoid damaging the BOX, was applied to a highly doped ground plane ($N_A \sim 10^{18}$ cm^{-3}), which is acting as a back gate. In addition, the Synopsys packages used for TCAD simulations were Sentaurus Workbench version J-2014. 09 [21] and device user guide I-2014. 09 [22]. The simulator includes physics models such as Shockley-Read-Hall generation/recombination.

3.3.3 Experiments

Figure 3.15a presents the body voltage (or potential) V_b variation in ultrathin devices as a

function of the front voltage at different drain biases with a fixed back-gate bias. It is worth noting that when a negative back-gate bias (V_{Gb} = -10 V) is applied, V_b shows peculiar curves as demonstrated in Figure 3.15b. When the front-gate bias is increased, V_b initially follows a standard behavior. However, after passing a "critical" bias point, V_b drops (Figure 3.15b). This may be related to supercoupling effect in the ultrathin body (t_{Si} < 10 nm). This drop takes place when the vertical depletion width expands down to the bottom interface, *i.e.* when the back accumulation layer vanishes. In contrast, for a thick device (t_{Si} = 25 nm) with V_{Gb} = 0 V, the variation of V_b is very small, less than 1 mV (Fig. 3.15c). In spite of the negative back-gate bias (V_{Gb} = -10 V), we observe a behavior of the V_b that depends on V_D (Fig. 3.14d). For thick films, the slight increase of V_b with V_D may be attributed to the hole charging of the body originating from the increase of the drift-diffusion current at the body-drain junction.

When source and drain contacts are floating, the V_b shows a linear behavior as a function of front-gate bias (Fig. 3.16). Namely, the initial V_b value is determined by the "residual" majority carrier density inside the body and the floating body is entirely governed by the competition between the front- and back-gate voltages.

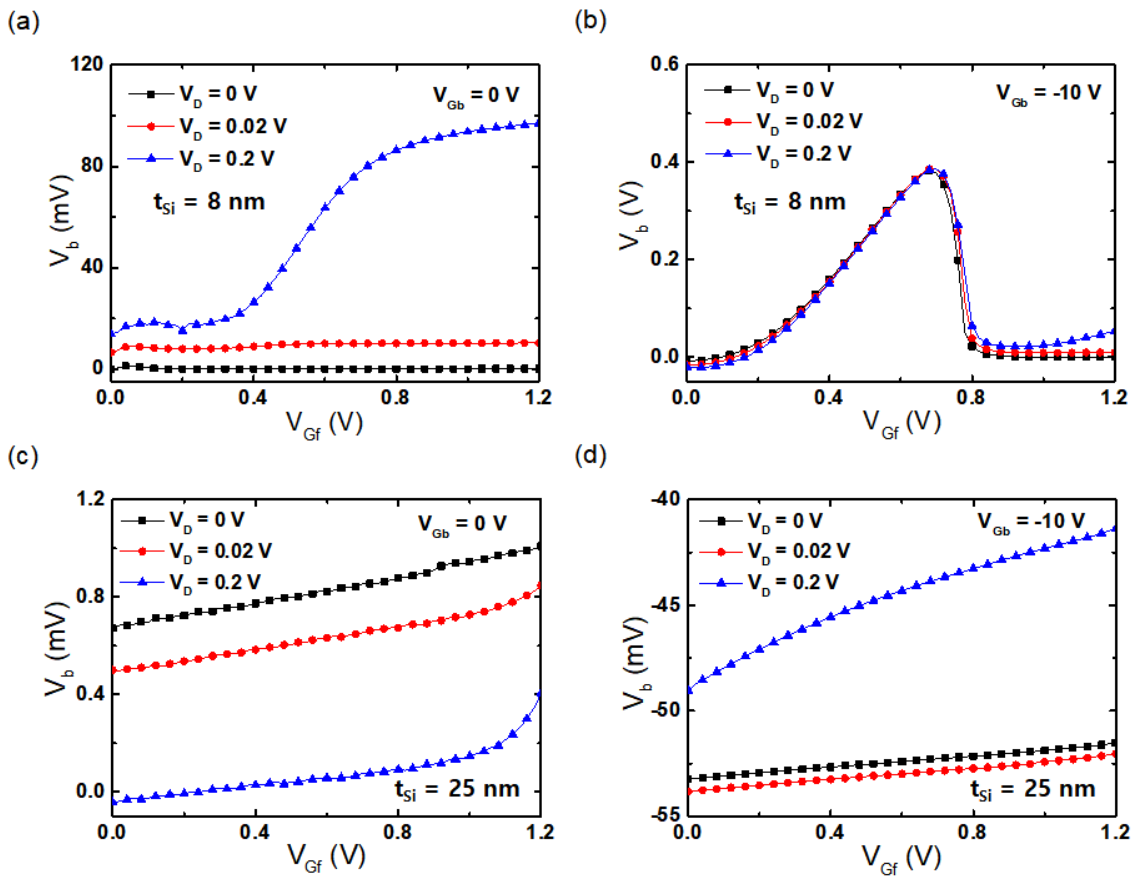

Figure 3.15: Measured body voltage V_b variations with drain biases from 0 V to 0.2 V versus the front-gate bias. For thin devices (t_{Si} = 8 nm) with (a) V_{Gb} = 0 V, (b) V_{Gb} = -10 V, and thick devices (t_{Si} = 25 nm) with (c) V_{Gb} = 0 V, (d) V_{Gb} = -10 V, respectively. W = 10 µm and L_G = 5 µm.

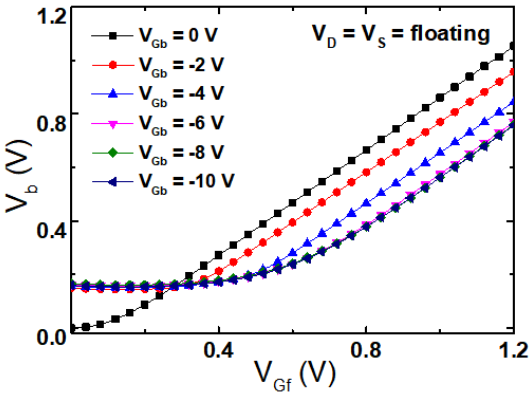

Figure 3.16: V_b variations for negative back-gate voltages V_{Gb}, from 0 V to -10 V, with the source and drain contacts floating. t_{Si} = 8 nm, W = 10 µm and L_G = 5 µm.

In the following sub-sections, we report additional experimental results to clarify the triangular V_b shape for the supercoupling effect in the ultrathin BCN MOSFETs. The experiments investigate the dependency of back-gate voltage, film thickness (t_{Si}), gate length (L_G), and scan speed/direction.

A. Body Potential V_b Variation with Current Transfer Characteristics

Figure 3.17a shows typical $I_D(V_{Gf})$ characteristics at different back-gate V_{Gb} voltages in ultrathin FDSOI BCN devices (t_{Si} = 8 nm). When the back interface is in accumulation mode (V_{Gb} < 0 V), the drain current I_D is a part of source current I_S which is recombined inside the thin body when the weak inversion at the front-interface started. Hence, no I_D is observed in the plot because it has negative value (Fig. 3.17b). In a log scale I_D (V_{Gf}) subthreshold regime, one can see that the current is exponentially dependent of V_{Gf} (the linear part of I_D is observed for V_{Gf} < V_T).

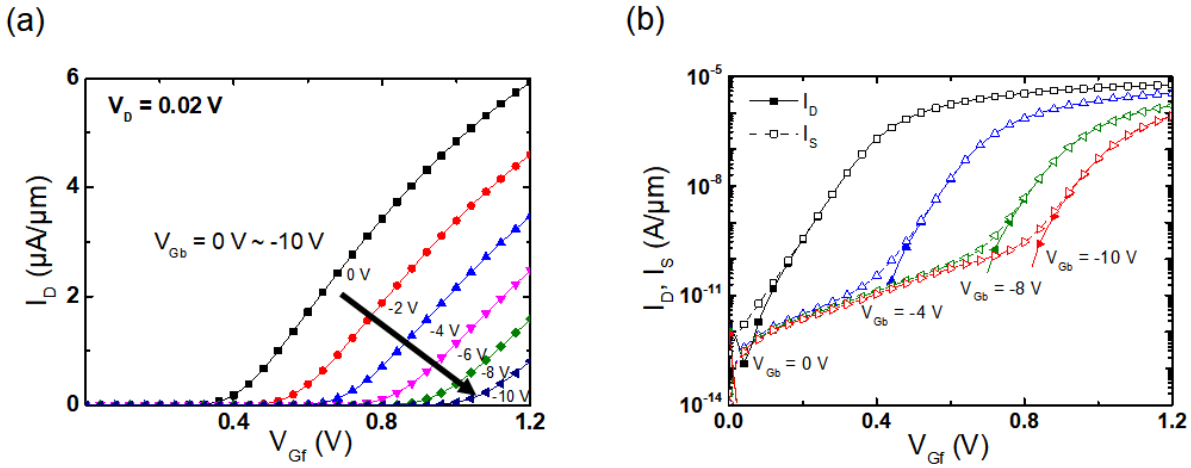

Figure 3.17: Drain current I_D characteristics with negative back-gate voltage V_{Gb} (from 0 V to -10 V) in BCN MOSFETs, (a) linear-scale and (b) log-scale with source current I_S. t_{Si} = 8 nm, t_{BOX} = 25 nm, t_{OX} = 1.5 nm, W = 10 µm and L_G = 1 µm. V_D = 0.02 V.

As demonstrated in Figure 3.17b, the I_D flows backwards until the holes are expelled from the body into the source. Consequently, the source current I_S (empty symbol in Fig. 3.17) increases gradually through the forward-biased body-to-source junction. Figure 3.18 shows the correlation between I_D and V_b, which is significantly informative in terms of the sharp drop occurring within the body potential characteristics. Once I_D flows in "steady-state" conditions through the ultrathin body, the V_b variation stops (Fig. 3.18). We may attribute this behavior to the supercoupling effect *i.e.* to the fact that the body cannot accommodate two types of carriers in ultrathin film simultaneously [19].

Furthermore, the subthreshold swing (SS) values are more or less 61 mV even for negative back-gate biases as indicated in Figure 3.18. Thus ideal current characteristic, *i.e.*, the lowest possible subthreshold swing is achieved. Expelling holes from the back interface activates the influence of the BOX capacitance; hence the two capacitances C_{Si} and C_{BOX} are in series. In that case, the SS is minimum because $C_{BOX} << C_{Si}$ and $C_{BOX} << C_{OX}$ [23].

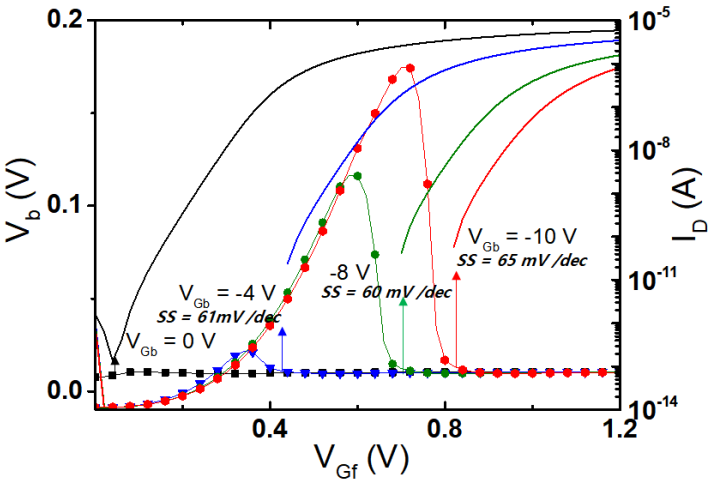

Figure 3.18: Body potential V_b variations and drain currents I_D, depending on the different back-gate biases. Subthreshold swing (SS) is also indicated. t_{Si} = 8 nm, t_{BOX} = 25 nm, L_G = 5 µm, V_D = 0.02 V.

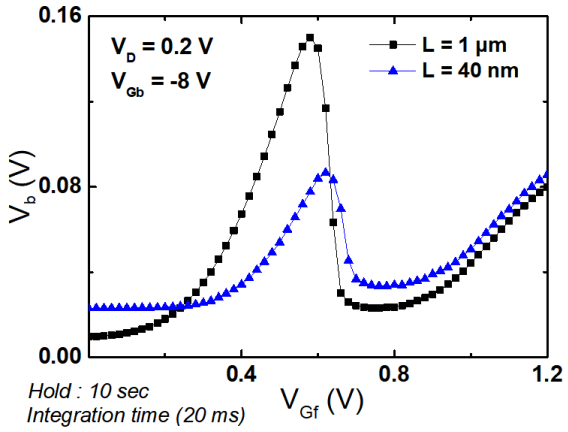

Figure 3.19: Long- and short-channel BCN MOSFETs, showing the V_b variation versus front-gate voltage with negative back-gate, V_{Gb} = -8 V. t_{Si} = 8 nm, t_{BOX} = 25 nm, t_{OX} = 1.5 nm, V_D = 0.2 V.

The triangular shape of the body potential V_b variation can also be observed even in short channel devices as demonstrated in Figure 3.19. For a short channel BCN MOSFETs (L = 50 nm in Fig. 3.20a), the V_b variation presents the same tendency as in long channel devices. Drain current I_D, source current I_S, and gate current I_{Gf} are represented as a function of the front-gate bias (Fig. 3.20b). For a short channel device (L = 50 nm), the subthreshold swing characteristics are also slightly improved about 4.5 % even for V_{Gb} = -10 V (Fig. 3.20c).

This can be a result of the activation of coupling via C_{BOX}. The gate coupling is mitigating the series capacitance between silicon body and BOX as long as the back interface influences the front channel current conduction via the C_{BOX} [24].

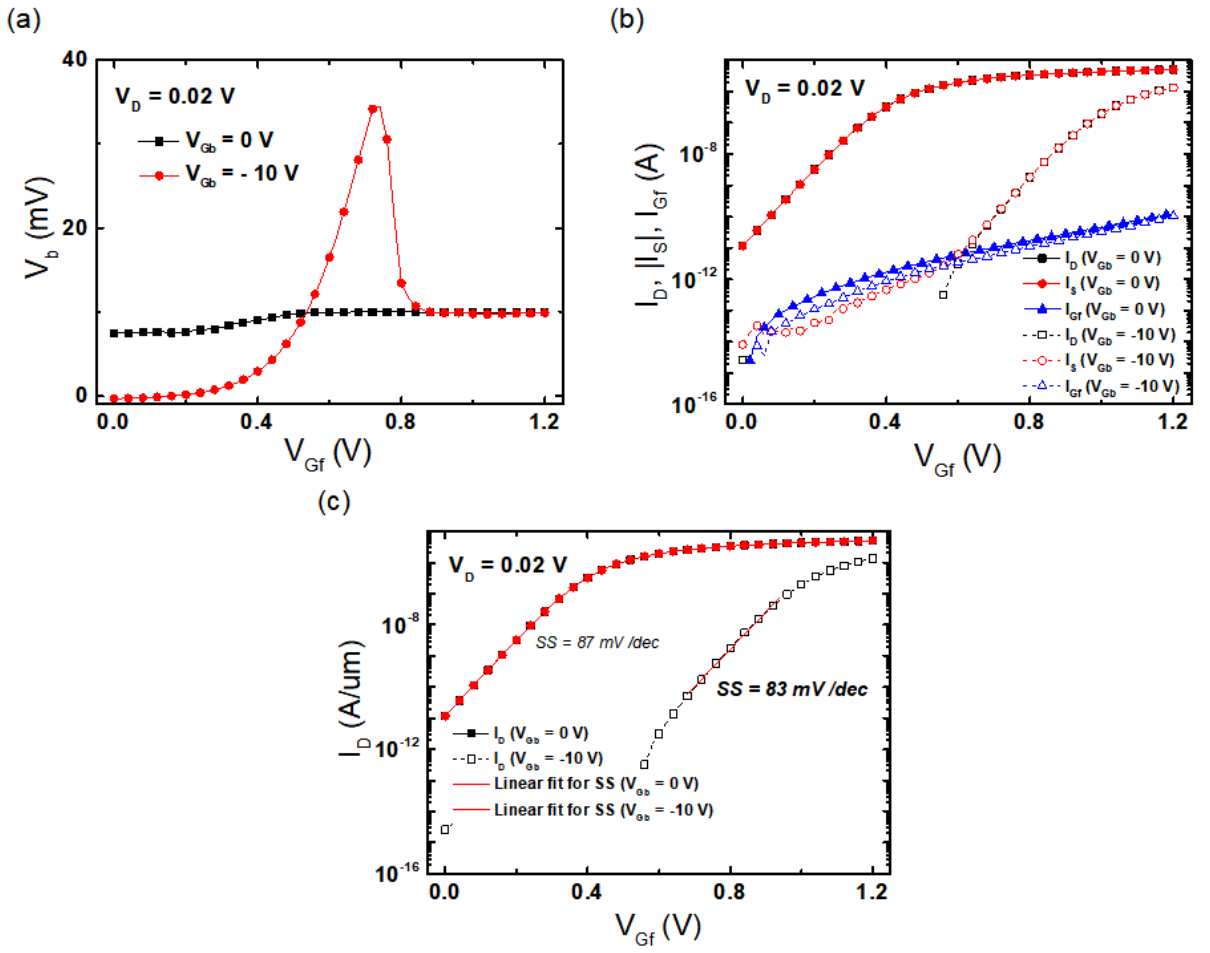

Figure 3.20: A short channel device, showing (a) the V_b variations with front-gate voltage for variable back-gate bias, (b) drain, source, and gate currents, and (c) subthreshold swing. t_{Si} = 8 nm, t_{BOX} = 25 nm, L_G = 50 nm, V_D = 0.02 V.

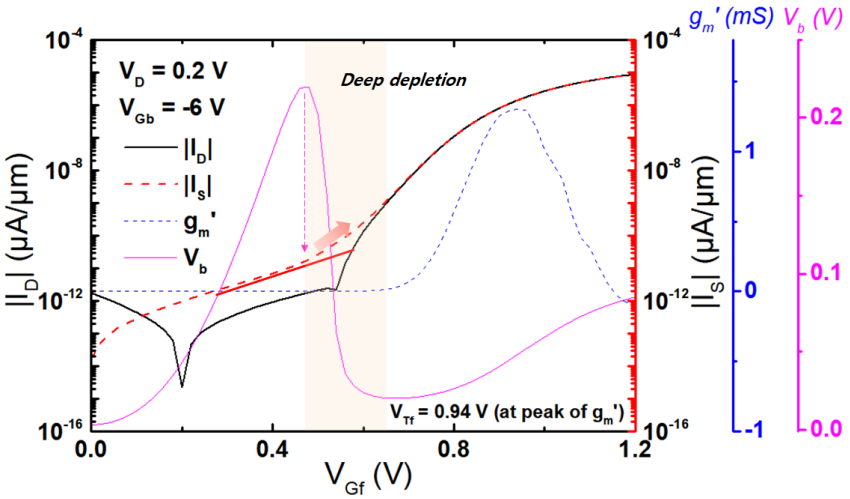

Figure 3.21: Body potential variation reflects the change of source I_S and drain I_D currents. Derivative of transconductance g_m' also shows the threshold voltage V_T. t_{Si} = 8 nm, t_{BOX} = 25 nm, L_G = 5 μm.

According to the V_b variation measurement, the hole layer at the back interface is preserved until the V_b peak onset, *i.e.*, until the vertical depletion width reaches the back interface (Fig. 3.21). Once the depletion width is such as the remaining holes are "totally" expelled toward the source (drain) junction, the body is fully depleted and the body potential drops. As a result, we can also observe that the source current demonstrates an increase as depicted in Figure 3.21 (near the red arrows). This "extra" source current increase may be related to a displacement current linked to the sharp V_b drop. After the electron channel builds up under the front gate, the drain current I_D flows in steady-state condition and the V_b variation recovers steadily to almost half of the drain bias. This V_b recovery region can be used as a new method of extracting the threshold voltage in ultrathin FDSOI MOSFETs. This new approach is presented in section 3.3.5.

B. Impact of Silicon Body Thickness and Back-Gate Contribution

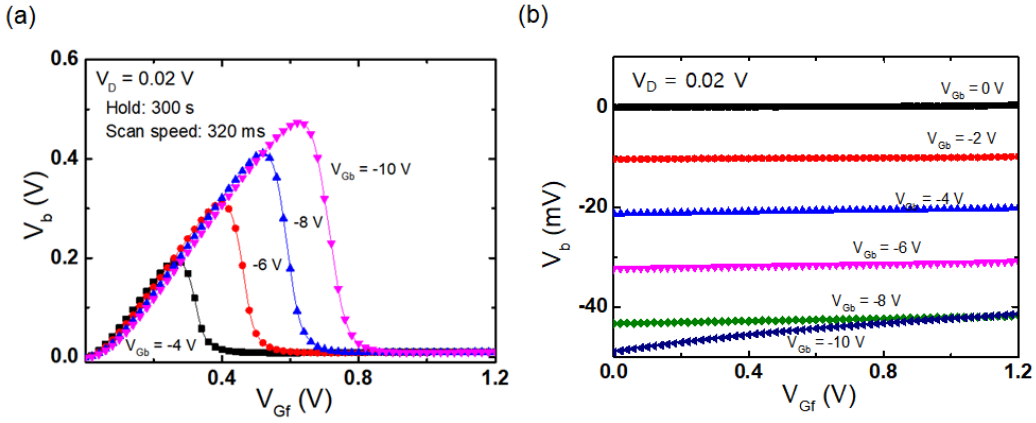

Figure 3.22: Body potential variation in (a) ultrathin body (t_{Si} = 8 nm) and (b) thick body (t_{Si} = 25 nm), with negative back-gate biases. t_{BOX} = 25 nm, L_G = 5 μm, V_D = 0.02 V and V_{Gb} = 0 V to -10 V.

Figure 3.22 presents the impact of silicon body thicknesses, t_{Si} = 25 nm (a) and 8 nm (b) for variable back-gate bias. The V_b variation in thick body devices is relatively flat and much less influenced by the front and back-gate biases as demonstrated in Fig. 3.22b.

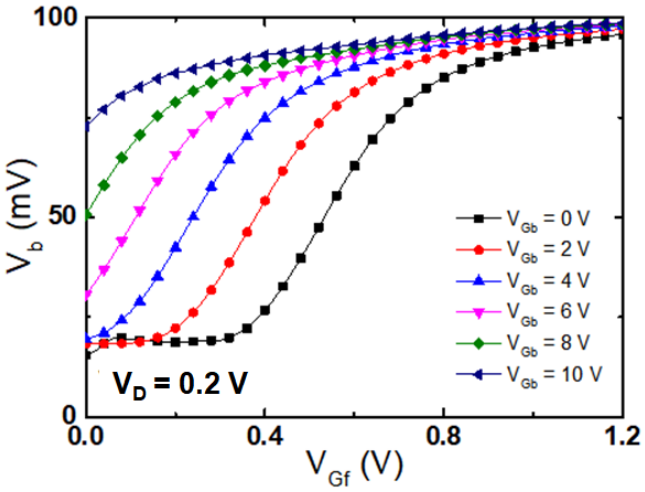

Figure 3.23: Measured the V_b with positive back-gate biases. t_{Si} = 8 nm, t_{BOX} = 25 nm, L_G = 5 µm.

The case of a positive back-gate bias (V_{Gb} = 0 V to +10 V) highlights typical body potential variation in Figure 3.23. As far as the back-channel variation depends on the front-gate V_{Gf} bias, V_b increases up to a point where the front inversion layer is formed. If the back inversion is not present, *e.g.* for V_{Gb} < 5 V (back-channel threshold voltage V_{Tb} ~ 5 V), the body potential remains flat (V_{Gb} = 0 V) or slightly increases (V_{Gb} < 4 V) until the front inversion layer starts to be formed. The linear V_b increase occurs as long as the front interface remains in weak inversion. Once the strong front inversion regime is reached, the V_b shape starts to bend as it could be observed in standard $I_D(V_G)$ curves plot in log scale. This means that here, V_b can be considered as a straight inner view of the body state and an image of the drain current variations. The front threshold voltage can be extracted from the linear transition of V_b.

C. Impact of Scan Speed and Direction

The V_b variation is examined by changing the bias scan speeds. The scan speed modification is achieved by changing the integration time (*IT*). By default the selected IT values of the analyzer are: 640 µs (short, 31.25 V/s), 20 ms (medium, 1 V/s), and 320 ms (long, 62.5 mV/s). Otherwise, it can set to a custom value between 80 µs and 1 s in manual mode. Figure 3.24 presents the dependence of the V_b variation on the scan speed. For the longest integration time, the peak of the V_b variation is higher

than in the other cases. It could mean that sufficient time is required to maintain the accumulated holes in the ultrathin body. Conversely, for short integration time, the holes can be quickly expelled into the source junction due to the fast scan of the front-gate bias. Figure 3.24b shows the source current I_S, which for the short integration time is higher than for other scan speeds (up to V_{Gf} = 0.3 V). During the fast scanning mode (31.25 V/s) of the front gate, the holes in the body move towards the source as long as the front-depletion width expands downward. As a result, V_b decrease because of the lack of holes in the ultrathin body.

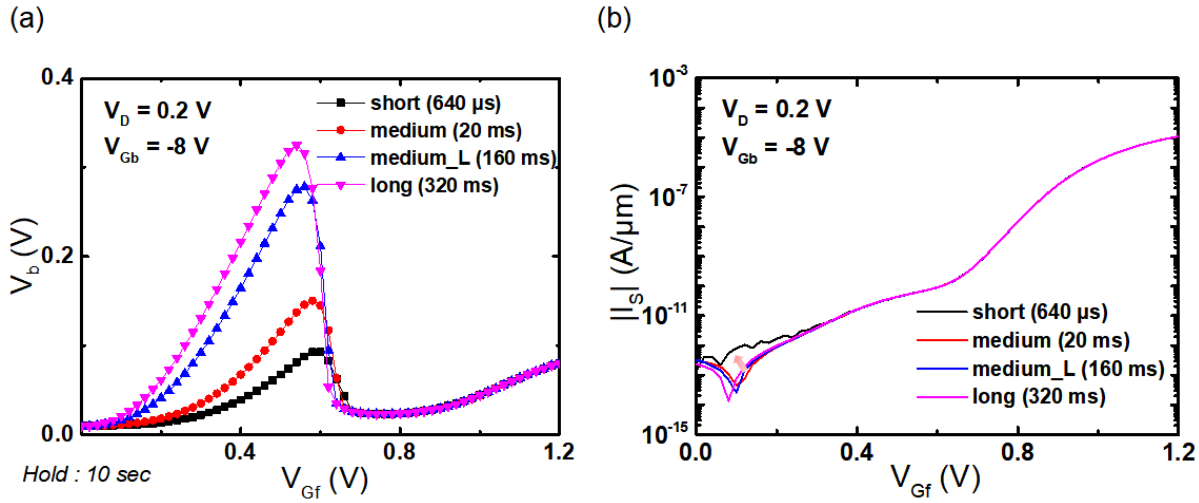

Figure 3.24: (a) V_b variation with bias scan speed (from 640 µs to 320 ms) and (b) source currents I_S are demonstrated in order to indentify the reason why the V_b is low value in the fast scan mode, short integration time (640 µs). t_{Si} = 8 nm, t_{BOX} = 25 nm, L_G = 5 µm.

For further understanding the V_b variation, double sweep mode measurements were also performed. This means that V_{Gf} scanning is performed from depletion to inversion mode and reciprocally (Fig. 3.25). When the front-gate bias is increased from 0 V to 1.2 V (strong inversion), an electron channel layer is formed, as expected. The V_b variation drops to low values (Fig. 3.25) because electrons prevail in strong inversion mode. However, the slight increasing tendency in inversion regime is worth noting in terms of extracting the threshold voltage in ultrathin FDSOI MOSFET (see on 3.3.5).

A noticeable change of the V_b behavior when V_{Gf} is scanned from inversion to accumulation is observed as the front interface enters in the weak inversion regime. From that point, when V_b increases, its slope is lessened (less sharp) while the V_b peak is shifted to (or occurs at) more negative V_{Gf} values (the V_b peak values seem to be preserved for all V_{Gb} values).

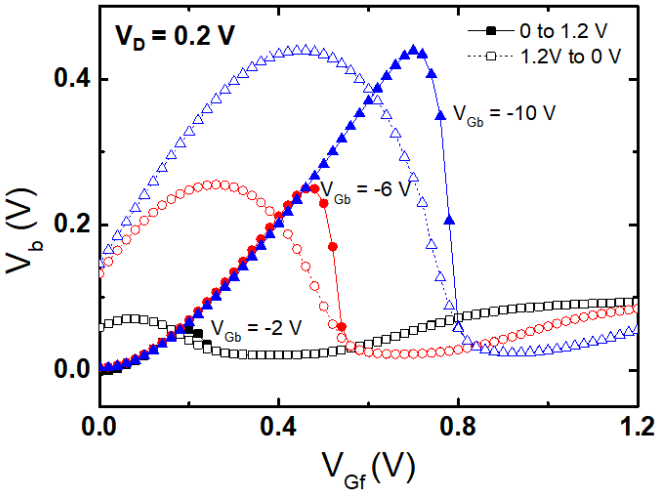

Figure 3.25: The V_b variation measures in double sweep mode,scanning from 0 V to 1.2 V and return to 0 V right after (scan speed = 20 ms). t_{Si} = 8 nm, t_{BOX} = 25 nm, L_G = 5 µm.

3.3.4 TCAD Device Simulation

Quasi-stationary and out of equilibrium body potential study was originally performed in thick FD SOI devices [4], [6]. The physical mechanisms dealing with the body potential variation were extensively investigated through electrical measurements and TCAD simulations. It was highlighted that the body potential measured through a high impedance source measurement unit (SMU of an Analyzer) reflects the hole quasi-Fermi level variations.

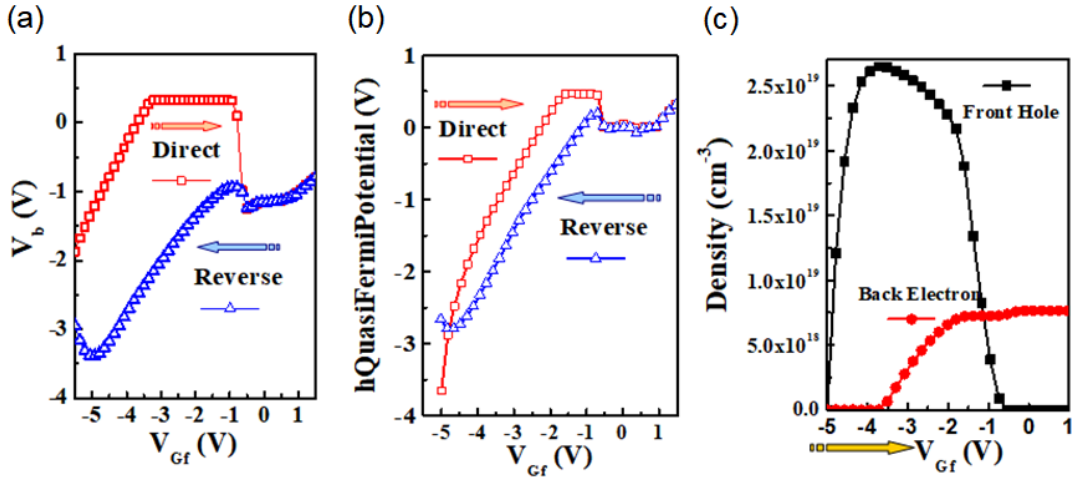

Figure 3.26: (a) Measured body potential and (b) simulated hole quasi-Fermi level QFL versus decreasing (reverse scan) and increasing (direct scan) front-gate bias V_{Gf}. (c) Simulated hole and electron densities versus increasing (direct scan) front-gate bias V_{Gf}. V_{Gb} and V_D are 30 V and 0.1 V respectively. t_{BOX}, t_{ox} and t_{Si} are 400 nm, 10 nm and 80 nm. The channel length and width are 300 µm [6].

Qualitatively, TCAD simulations in thick films demonstrated that the measured out of equilibrium body potential (Fig. 3.26a) follows the hole quasi-Fermi potential variations (Fig. 3.26b).

In the same way as the hole quasi-Fermi level inside the whole body can be imposed/fixed by applying a bias to the P^+ body contact. Conversely, the hole quasi-Fermi level (*i.e.*, the "mirror" of the hole density (Fig. 3.26c)) can be measured at the body contact. It is worth noticing that to achieve such a result experimentally, a "zero current" condition needs to be imposed at the body contact (*e.g.* the measurement setup has a very high input resistance).

Consequently, the measured body potential is able to provide qualitatively the majority carrier (hole) density variations. By "qualitative", we mean that only a relative hole density variation can be determined and this, for the two following main reasons: (i) the initial/residual hole concentration when the measurement starts is unknown and (ii) only the average body potential in the whole film is measured. The latter "drawback", however, is less troublesome since the hole quasi-Fermi level remains constant in the whole film from the front to the back interface. As a matter of fact, if we consider 2D effects coming from short channel effects, the "constant" quasi-Fermi level statement needs to be reconsidered.

In our simulations, we consider the hole quasi-Fermi level to evaluate the gate coupling effect in very thin films (t_{Si} =8 nm). To obtain further insights, TCAD simulation was conducted. A test device structure is made by Sprocess tool, Sentaurus Workbench version J-2014. 09. (Fig. 3.27) [21].

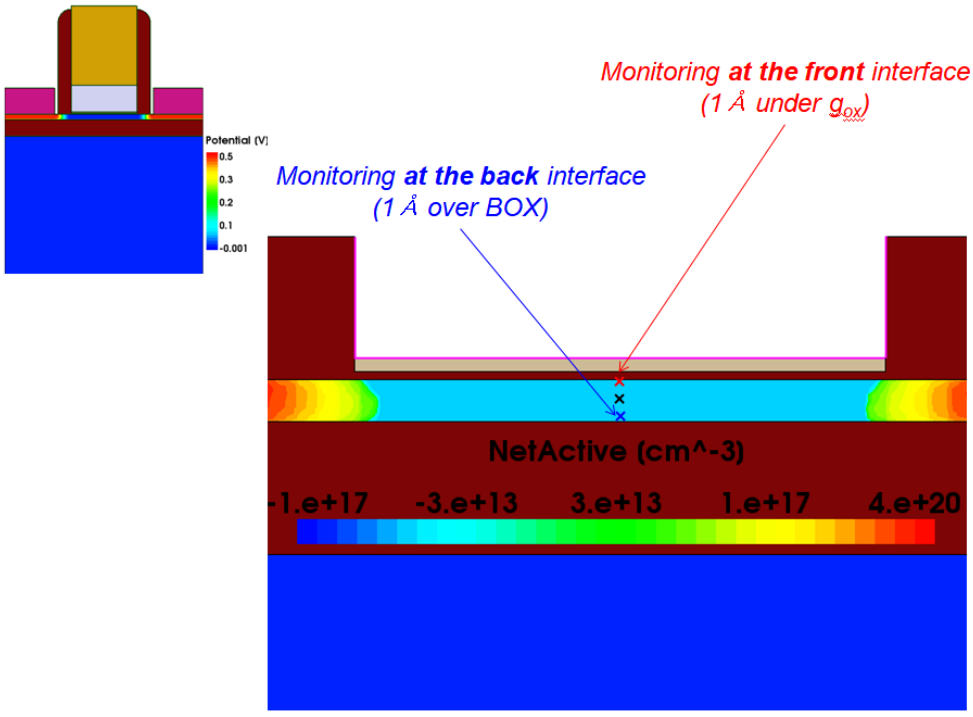

Figure 3.27: Cross-section view of a test structure made by sprocess. t_{Si} = 8 nm, t_{BOX} = 25 nm, L_G = 100 nm.

Table 3.2 shows bias conditions for electrodes: drain (V_D), source (V_S), front-gate (V_{Gf}), and back-gate (V_{Gb}). The Poisson equation is used for initialization of each electrode (Standard solver initialization in quasi-stationary mode with Poisson equation with all contacts set at 0 V).

	Initialization		Hold (1 s)	V_{Gf} transient sweep		Remark
	initial	*final*		*initial*	*final*	
V_D	0 V	0.2 V	←	←	←	-
V_{Gb}	0 V	Variable	←	←	←	Variable values: 0 V, -1 V, -2 V, -4 V, -6 V, -8 V -10 V
V_{Gf}	0 V	0 V	0 V	←	2 V	Sweeping front-gate
V_S	0 V	0 V	0 V	←	←	-
Time	0 s	0.2 s	1.2 s	1.2 s	2.7 s	Adjustable

Table 3.2: Drain, source, front-gate, and back-gate bias conditions in transient simulation.

Before sweeping the front-gate bias, V_D and V_{Gb} are set at constant values to reproduce the experimental conditions. Before the V_{Gf} transient sweep starts, a hold time is also applied (1 s with V_{Gf} kept constant). As shown in Figure 3.28, the transient V_{Gf} simulation is conducted after initialization (1.2 s). Front-gate voltage V_{Gf} is swept from 0 V to 2 V (Table 3.2).

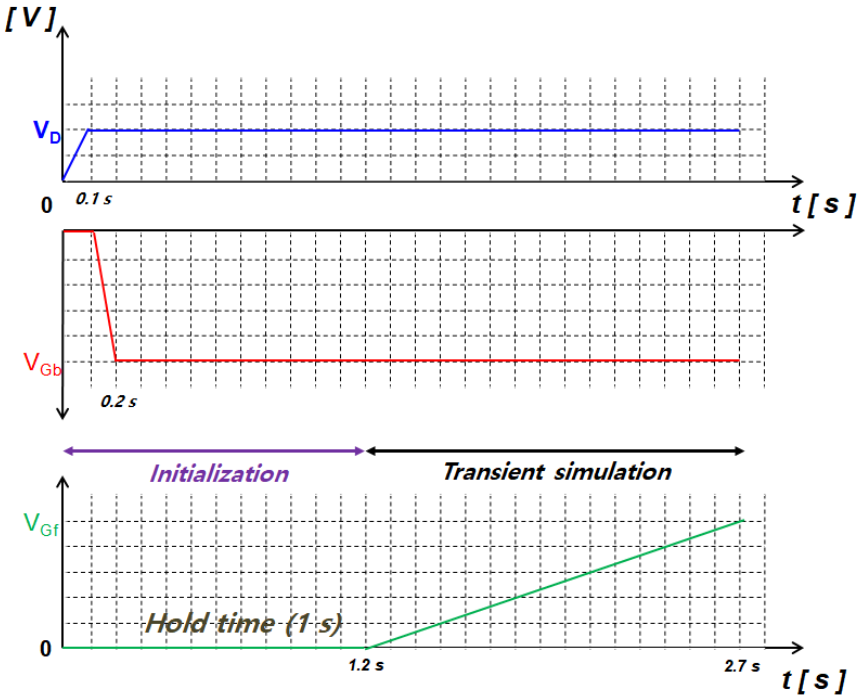

Figure 3.28: Transient simulation timing patterns with initialization and hold time.

Figure 3.29a shows typical drain current $I_D(V_{Gf})$ characteristics with negative back-gate biases (V_{Gb} = 0 V to – 10 V). For the thin body device, the drain current is shifted when the back-gate voltage becomes more negative. The hole quasi-Fermi potential shows a drop similar to the that of the measured body potential V_b (Fig. 3.29b). Experimentally, this means that the hole layer disappears as

soon as the front electron channel is formed in the thin body. However, the TCAD simulation shows a different behavior when V_{Gb} becomes lower than -6V. The hole quasi-Fermi potential shows a plateau which extends when V_{Gb} becomes more negative as demonstrated in Figure 3.29b. From the simulation point of view, this effect should be induced by the fact that holes at the back interface cannot be fully expelled out from the body.

In the measurement case, as much as negative V_{Gb} becomes, the body potential keeps the same behavior and sharply drops to zero. This may suggest that the drop of body potential is related to the measurement setup. The following explanation is proposed: when the back accumulation disappears, the resistance of the body contact is drastically increased. We may reasonably suppose that, in such a condition, the input impedance "seen" by the B1500 Analyzer becomes higher than its own input impedance. Consequently, the voltage level (*i.e.* the measured body potential) will drop accordingly due to a resistance divider effect. If the effective impedance decreases, "leakage" body current may flow through the body contact. Hence, the remaining holes can be expelled allowing to properly depleting the body. Notice that the leakage current at the body contact induces a low resistive path between the body and the drain contacts. This could explain why half of V_D (*i.e.* $V_D/2$) is measured through the body contact when the front inversion layer is in strong inversion regime.

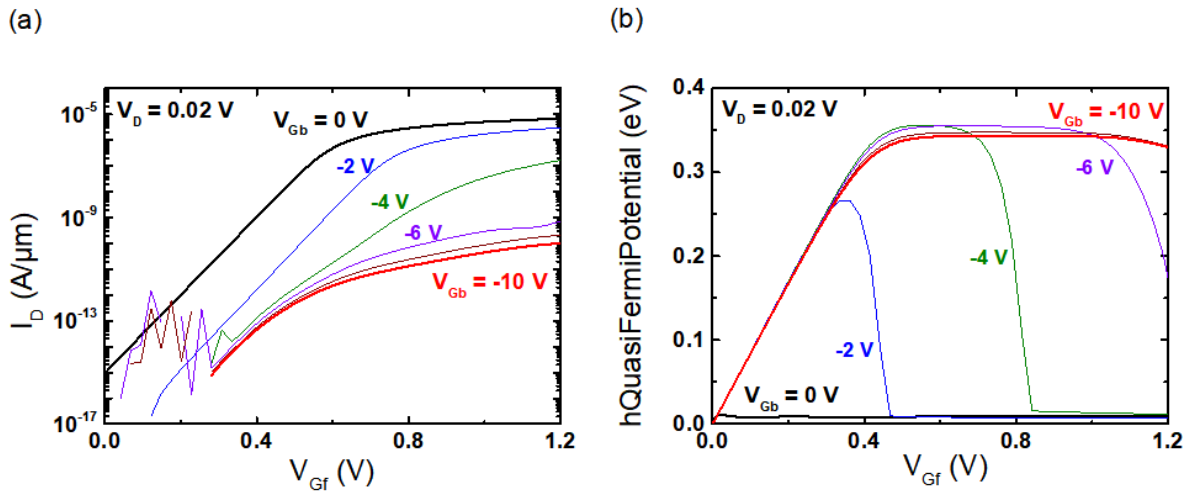

Figure 3.29: TCAD device simulation of (a) I_D (V_{Gf}) versus front-gate bias and (b) Quasi-Fermi potential for holes. t_{Si} = 8 nm, t_{BOX} = 25 nm, L_G = 100 nm, V_D = 0.02 V, and V_{Gb} = 0 V to -10 V (step = -2 V).

Note that in the simulation, for V_{Gb} values lower than -4V, the I_D current behaves as if the front interface can never be in weak inversion regime, even for low V_{Gf} values (no linear I_D curve is observed in the log plot). However, the carrier densities study will reveal that the back-hole layer is well suppressed (Fig. 3.30a).

Figure 3.30 shows carrier density profiles of holes at the back-interface and electrons at the front-interface. For the thin device (t_{Si} = 8 nm), the hole density suddenly drops below 10^{10} cm^{-3} for

V_{Gf} > 0.6 V (Fig. 3.30a). However, the hole density of the thick device (t_{Si} = 25 nm) is kept constant even in strong inversion regime ($V_{Gf} > V_T$) (Fig. 3.30b). Remark that the holes quasi-Fermi potential (hQFP) variation at the back interface can still indicate the density of holes change.

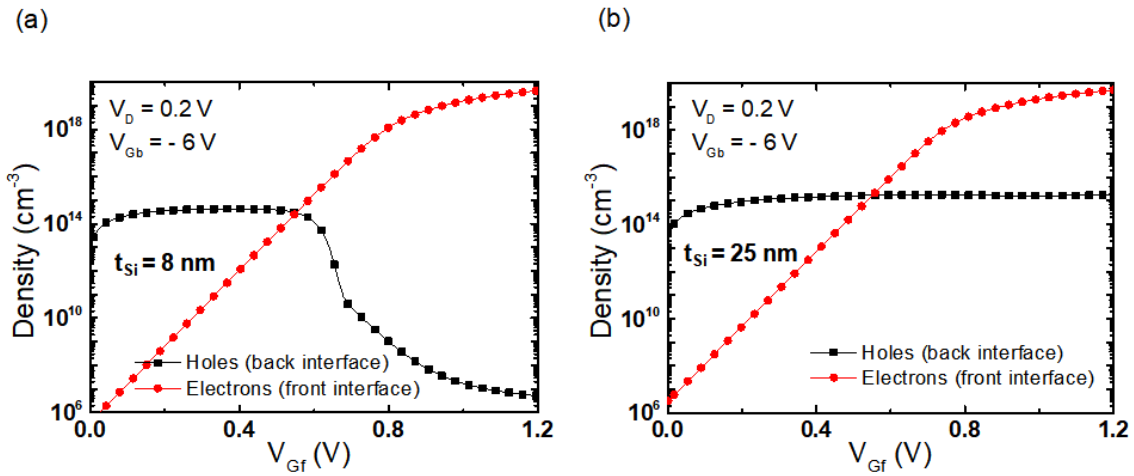

Figure 3.30: Carrier density profile at the back-interface for electron (red symbol) and hole (black symbol), depending on the film thickness with (a) t_{Si} = 8 nm, (b) t_{Si} = 25 nm. L_G = 100 nm, V_D = 0.2 V, and V_{Gb} =-6 V.

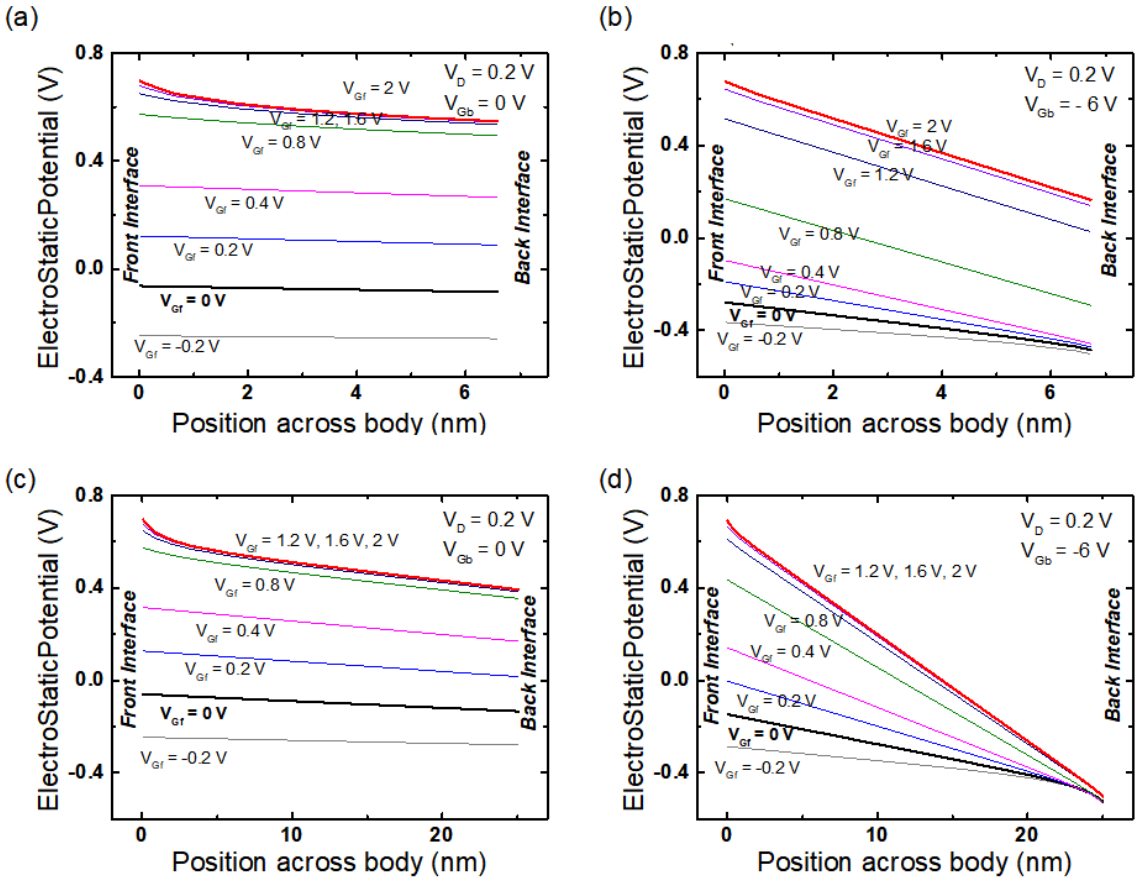

Figure 3.31: Electrostatic potential distributions across the ultrathin body (t_{Si} = 8 nm) present with (a) V_{Gb} = 0 V, (b) V_{Gb} = -6 V. For a relatively thick body (t_{Si} = 25 nm), the electrostatic potential shows with (c) V_{Gb} = 0 V, (d) V_{Gb} = -6 V. V_D = 0.2 V, V_{Gf} =-0.2, 0, 0.2, 0.4, 0.8, 1.2, 1.6, and 2 V, respectively. t_{BOX} = 25 nm, L = 1 μm.

Electrostatic potential (EP) profiles are plotted between the front- and back-interfaces in Figure 31. Figures 3.31a,b show the EP in the ultrathin body. When the front-gate bias V_{Gf} changes from -0.2 V to 2 V with grounded back-gate bias (V_{Gb} = 0 V), the EP at the front-interface increases and the back-interface EP saturates (Fig. 3.31a, c). For the thin device at V_{Gb} = -6 V, the EPs of back-interface are pinned at the same value under V_{Gf} < 0.5 V. As soon as the front-gate voltage increases beyond 0.5 V, the back surface potential increases together thanks to the gate coupling effect (Fig. 3.31b). When the V_{Gf} bias becomes higher than 1.2 V, the EP value at the back-interface becomes positive. It means that the thin body is completely inverted, *i.e.* volume inversion is reached.

For thick devices, the EP at the back-interface is firmly pinned at around -0.5 V due to the negative back-gate bias (V_{Gb} = -6 V in Fig. 3.31d). Whatever the positive front-gate voltage value applied, the back-surface potential is unchanged as shown in Figure 3.30d.

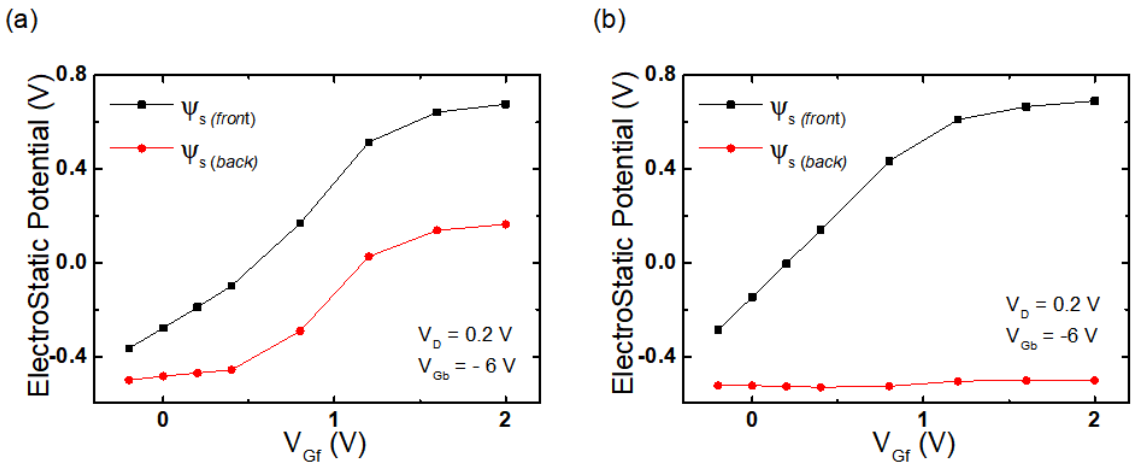

Figure 3.32: Electrostatic potential distribution at the front- and back-interface as a function of V_{Gf}. (a) t_{Si} = 8 nm, (b) t_{Si} = 25 nm. t_{BOX} = 25 nm, L = 1 μm.

Figure 3.32 presents the surface potential at the front- and back-interface as a function of the front gate bias. For the thin device, the back-surface potential follows the front-surface potential (Fig. 3.32a). The back-surface potential of thick device remains constant value (Fig 3.32b). Two carriers (electrons and holes) can co-exist in the relatively thick film as expected.

3.3.5 New Approach for Extracting V_T in Ultrathin FDSOI MOSFET

The threshold voltage V_T of typical MOSFETs can be extracted by either measuring the drain current-voltage or capacitance characteristics [25]. V_T extraction for SOI MOSFETs is also compatible with standard methods. But, when the silicon film thickness becomes thin, the source/drain series resistance becomes critical parameters for extracting V_T. The second derivative method was developed

to eliminate the dependence on the series resistances that induces inaccuracy in the threshold voltage extraction [26].

In this section, we propose a new V_T extraction method for the volume inversion regime in ultrathin FDSOI MOSFET by measuring the body potential V_b variation. The method is supposed to be independent of the high series source/drain resistance because the measured body potential technique is performed without any current flow. Our experimental results are also compared to a typical method of second derivative of g_m [26], [27] in terms of V_T accuracy for ultrathin FDSOI MOSFETs.

A. General methods for extracting V_T

The classical threshold voltage V_T has been determined by the intercept of a tangent through the peak point (linear transconductance g_m) of the low drain $I_D(V_{Gf})$ characteristics as shown in Figure 3.32a. This is a basic experimental method for extracting V_T. The determined V_T is about $3kT/q$ higher than the $2\Psi_B$ threshold voltage due to inversion-layer capacitance effects [25].

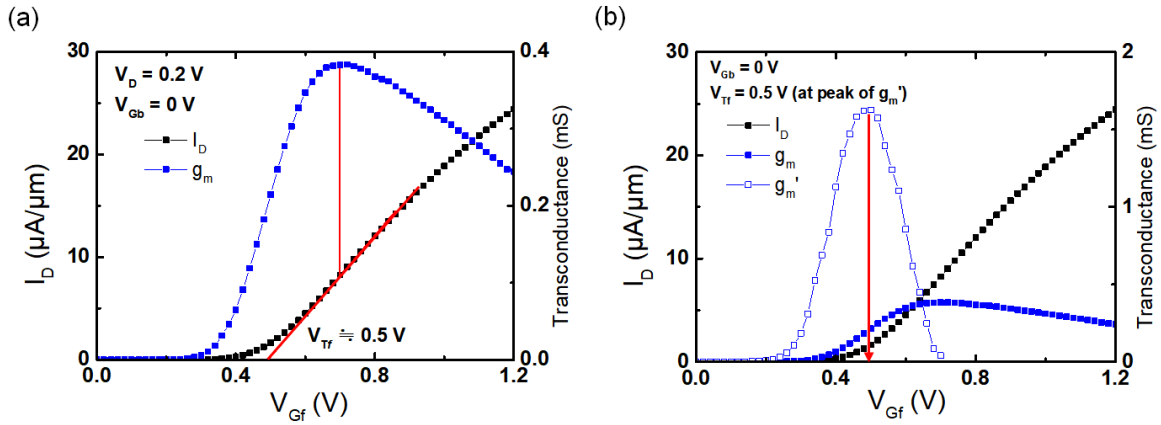

Figure 3.32: Threshold voltage V_T extraction with two methods: (a) the linearly extrapolation method in I_D (V_{Gf}) and (b) second derivative g_m method. t_{Si} = 8 nm, t_{BOX} = 25 nm, L_G = 5 μm, V_D = 0.2 V.

In FDSOI devices, the peak of the second derivative of front-channel $I_D(V_{Gf})$ characteristics yields the front threshold voltage for different conditions at the back interface (Fig. 3.32b).

B. New proposal for ultrathin FDSOI MOSFETs

The measured body potential V_b variation emphasizes in three domains (see in Fig. 3.21): (i) a gradually increasing region (back-accumulation and front-depletion occur simultaneously), (ii) an abrupt decreasing region (expelling out the holes into source then completely depleting the body at the

back interface), and (iii) a V_b recovery region due to the inversion electron layer. The recovery region provides us crucial information about the volume electron inversion and its threshold voltage.

For low drain voltage (V_D = 0.2 V) and V_{Gb} = 0 V, V_b shows two different slopes: (i) one is close to V_{Gf} = 0.1 V (but the increase is difficult to observe) and (ii) another is showing a clear linear behavior (blue line fit) as demonstrated in Figure 3.33a. Interestingly, the linear increasing V_b region corresponds to the change in the second derivative of g_m curve (red symbols).

At this point, we have examined the V_b variation at different back-gate biases from -2 V to -10 V (step = -2 V) in order to find out the linear region of the pure front inversion layer as shown in Figures 3.33b,c. We highlight that the linear regions are observed as soon as the curve of the first derivative of g_m begins to change. Figure 3.33d shows linear correlation between the V_b and V_T.

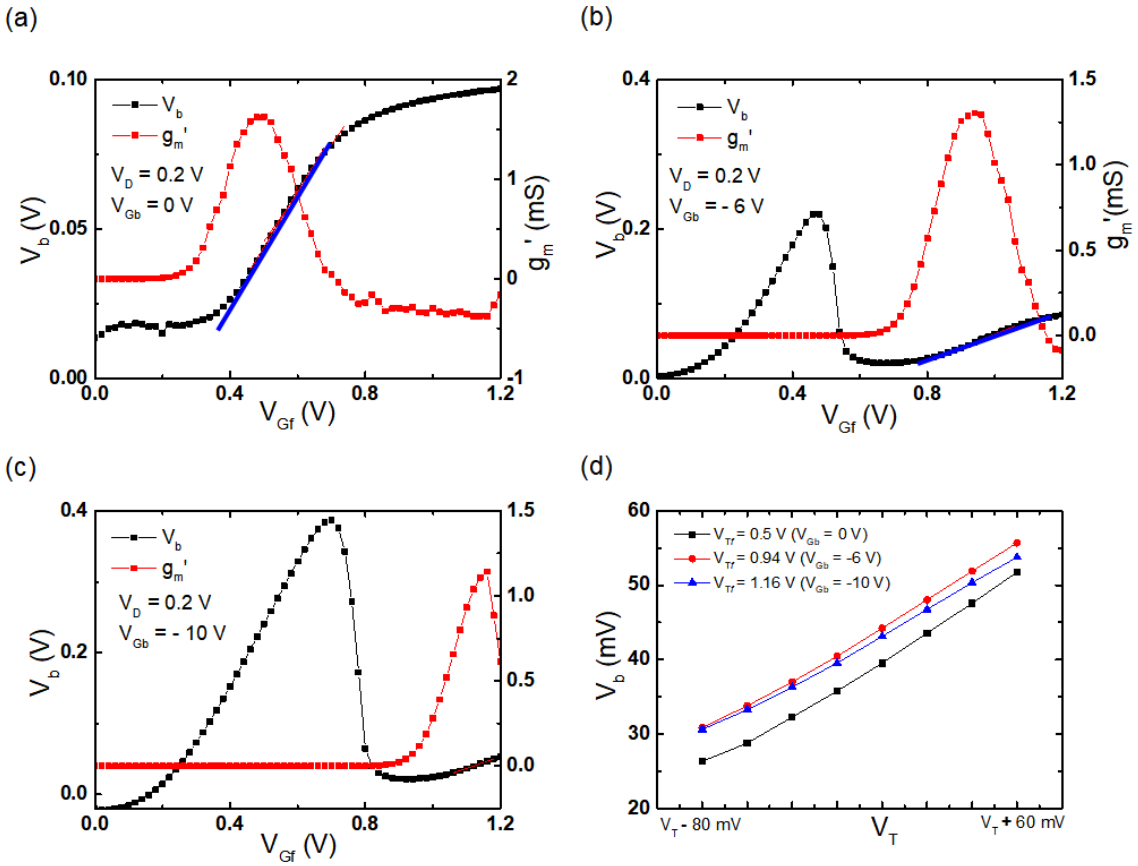

Figure 3.33: Body potential V_b variation and the first derivation g_m with back-gate voltages: (a) V_{Gb} = 0 V, (b) V_{Gb} = -6 V, (c) V_{Gb} = -10 V. (d) Correlation between the V_b and g_m'. t_{Si} = 8 nm, L_G = 5 μm, V_D = 0.2 V.

As previously discussed, the peak of the first derivative of g_m gives us the threshold voltage. The colored arrows in Figure 3.34a show that the peaks of the V_b derivative are corresponding to the linear change regime of drain current in the inversion mode. In order to confirm the relation between the peak values of the V_b derivative and V_T, the first derivative of g_m and the first derivative of V_b were plotted in the same graph (Figure 3.34b). The two different curves (derivatives of g_m and V_b) indicate

the same values corresponding to the front threshold V_{Tf}. It means that the proposed V_b derivative method can be used to determine the threshold voltage V_T in ultrathin FDSOI MOSFETs.

It is worth noting that measuring the V_b variation is useful to identify the different interface state regimes in ultrathin FDSOI MOSFETs. First of all, a moderate increase of V_b (before reaching the V_b peak value) reflects the expansion of the depletion width and the holes gradually vanish. Secondly, the sudden V_b drop evidences that the holes layer at the back-interface has entirely disappeared. After inversion takes place under the front gate, in strong inversion regime, the inversion electron layer shields the thin body from further penetration of the front-gate field [25]. In this condition, the measured V_b clearly indicates that half of the drain bias is probed by the analyzer (Figure 3.33b,c at V_{Gf} = 1.2 V).

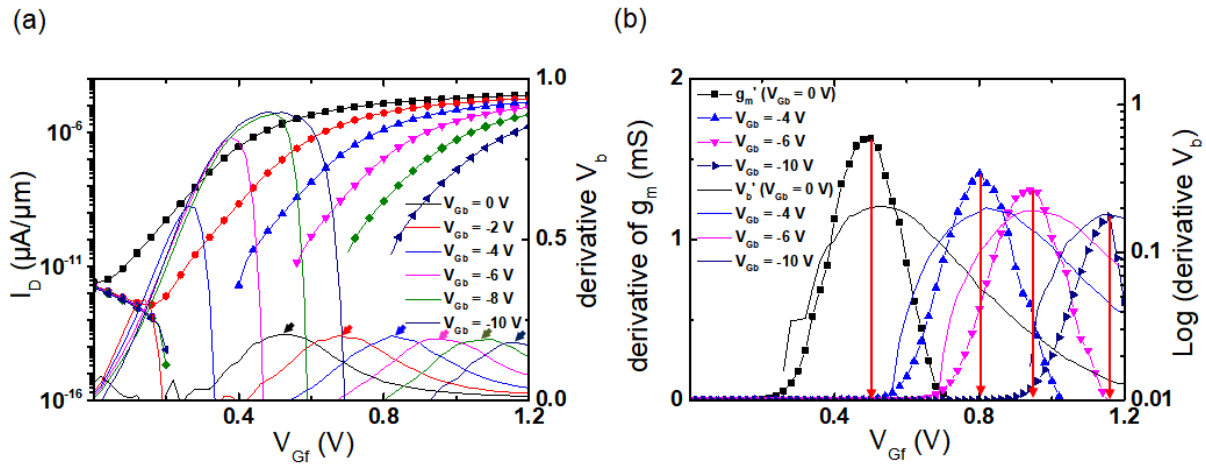

Figure 3.34: Threshold voltage V_T extraction methods: (a) classical method in I_D (V_{Gf}) (b) first derivative of g_m method. t_{Si} = 8 nm, t_{BOX} = 25 nm, L_G = 5 µm, V_D = 0.2 V.

3.4 Conclusion

The dynamic body potential V_b was experimentally measured using a P^+ body contact in ultrathin H-gate FDSOI MOSFETs. The measured V_b shows good correlations with the onset of the FBEs. According to the experimental measurements, three major findings can be highlighted:

(i) For the first time, the body potential variation was used to correlate the FBEs such as kink effect, GIFBE, and PBT. The point is that the FBEs are originated from the interplay of the excess holes which are stored or eliminated in the thin body.

(ii) We can predict the behavior of excess holes through the variation of V_b. As soon as the

volume inversion (electrons of n-MOSFETs) is just formed, V_b suddenly drops and the accumulated holes are expelled from the body. This is caused by the super-coupling effect. The new experimental evidence of super-coupling effect is directly comprehended by monitoring the V_b behavior.

(iii) A new technique for extracting threshold voltage V_T has been developed for the first time in the ultrathin MOSFETs. The V_T was extracted from the peak value of the V_b derivative in the inversion regime. The derivative V_b peak corresponds with accuracy to the V_T derived by the typical method, i.e., the g_m derivative extraction technique.

What stands out most from this finding is the establishment of a reliable V_b measurement for a precise understanding of the change related to the variation of excess holes in the ultrathin body.

3.5 References

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Chapter 4

Investigation of Advanced SOI applications

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4.1 Introduction

Silicon (or Semiconductor)-on-insulator technology inherently provides remarkable features for advanced devices [1]–[4]. SOI devices exhibit unusual characteristics such as sharp-switching behavior [1], inter-gate coupling by competition between the front- and back-gate [5], and compatibility with novel semiconductor materials [6]–[8]. This makes possible the design of innovative SOI devices [9]–[14].

In the following sections, we explore emerging devices such as an InGaAs-on-insulator lateral N^+NN^+ MOSFET, Z^2-FET magnetodiode, and optical detector.

4.2 Back-gated InGaAs-On-Insulator Lateral N^+NN^+ MOSFET

Back-gated InGaAs-on-insulator lateral N^+NN^+ MOSFETs were successfully fabricated by direct wafer bonding and selective epitaxial regrowth. These devices were characterized using a revisited pseudo-MOSFET configuration. Two different transport mechanisms are evidenced: volume conduction in the undepleted region of the film and surface conduction at the interface between InGaAs and buried insulator. We propose extraction techniques for the volume mobility and interface mobility. The impact of film thickness, channel width, and length is evaluated. Additional measurements reveal the variation of the transistor parameters at low temperature and under externally applied uniaxial tensile strain.

4.2.1 Introduction

The extension of Moore's law is based on two pillars: (i) electrostatic integrity of small transistors and (ii) improvement of transport properties for high speed. Only fully depleted devices, such as FinFETs, planar SOI or nanowires, benefit from excellent control of the gate on the channel, leading to attenuated short-channel effects and leakage current. Technology-wise, Semiconductor on Insulator (SOI) is the most straightforward, and pragmatic approach. Mobility boosters consist in adding strain, selecting the crystal orientation or, more drastically, replacing silicon with other semiconductors [7], [8], [13], [15], [16].

According to ITRS predictions [17], high-mobility channel materials such as Ge, SiGe and III-V compounds are promising candidates for the next generations of MOSFETs, able to deliver the necessary power-performance benefits and added functionality for CMOS and System-on-Chip applications [18]–[20]. Furthermore, devices fabricated on semiconductor-on-insulator substrates have better electrostatic control with decreased short channel effects and reduced leakage current [21]–[23]. Merging the merits of III-V compounds and SOI is a recent option explored as starting substrate (III-V on insulator) for device fabrication. In particular, InGaAs-on-insulator structures are attractive [24] to integrate high-performance FinFETs [25], planar MOSFETs on insulator and hybrid InGaAs/SiGe CMOS circuits [26]. This technology is rapidly evolving. Nevertheless, InGaAs-on-insulator films are prone to additional carrier scattering, compared to layers grown on bulk crystalline buffers such as InP [27] or InAlAs [28], owing to the presence of the buried oxide (BOX) and related back interface.

Our work is focused on the technological optimization via detailed investigation of transport properties in simple test devices. $In_{0.53}Ga_{0.47}As$ layers transferred on oxide were characterized using a modified version of the well-known pseudo-MOSFET (Ψ-MOSFET) configuration [29]. Lateral N^+NN^+ structures have been fabricated on InGaAs-on-insulator layers to mimic the channel transport of a MOSFET while minimizing the impact of process-induced damages. Section 2 presents the main processing steps. The measurement set-up and typical transistor characteristics are shown in section 3. A suitable procedure, based on the extension of Y-function technique, is proposed in section 4 for extracting the electron mobility in the film bulk and at the interface. We discuss the carrier mobility as a function of film thickness, temperature from 77K to 300K, and uniaxial tensile strain.

4.2.2 Device Fabrication

The fabrication of back-gated lateral N^+NN^+ transistors utilizes some of the key steps developed for InGaAs FinFETs [25]. The characteristics are expected to be representative of those in fully-processed devices with back-gate operation. The n-layer is a non-intentionally doped InGaAs-on-insulator (InGaAs-OI) grown in a metal organic vapor phase epitaxial reactor. InGaAs-OI layers on Si which have an initial doping concentration of $N_D \sim 2\times10^{17}cm^{-3}$ are prepared by direct wafer bonding of nominally-undoped $In_{0.53}Ga_{0.47}As$ films of varying thickness (25 nm, 50 nm, 100 nm and 200 nm) grown on InP wafers as described in [30]. The carrier concentration measured by Hall effect on a 200-nm-thick InGaAs on InP layer before bonding is of $2\text{-}3\times10^{16}cm^{-3}$. The buried oxide (BOX) consists of 25 nm thermal SiO_2, 10 nm Al_2O_3 and the high-k dielectric stack used in [25], for a resulting C_{BOX} of $0.11\mu F/cm^2$.

The fabrication of lateral N^+NN^+ structures starts with the deposition of a SiO_2 hard-mask to define the length of the n-region (Fig. 4.1(a)). Sn-doped $In_{0.53}Ga_{0.47}As$ N^+ regions ($N_D = 5x10^{19}$ cm^{-3})

are selectively grown (Fig. 4.1(b)) at low temperature as in [31]. The hard-mask is removed (Fig. 4.1(c)) and a mesa isolation is performed by wet etching (Fig. 4.1(d)). The top interface of the n-region is formed with same high-k dielectric as used for the bottom interface. The process is completed by the deposition of a SiO_2 layer (Fig. 4.1(e)), etching via holes and W metal contacts (Fig. 4.1(f)). It should be noted that although the bottom and top InGaAs/high-k interfaces are formed with the same deposition process, they differ in the fact that the bottom interface is exposed to the thermal budget of the N+ selective epitaxial process, contrary to the top interface. This leads to a difference in the interface trap density comparable that the difference between Gate-first and Replacement-metal-gate devices in [25].

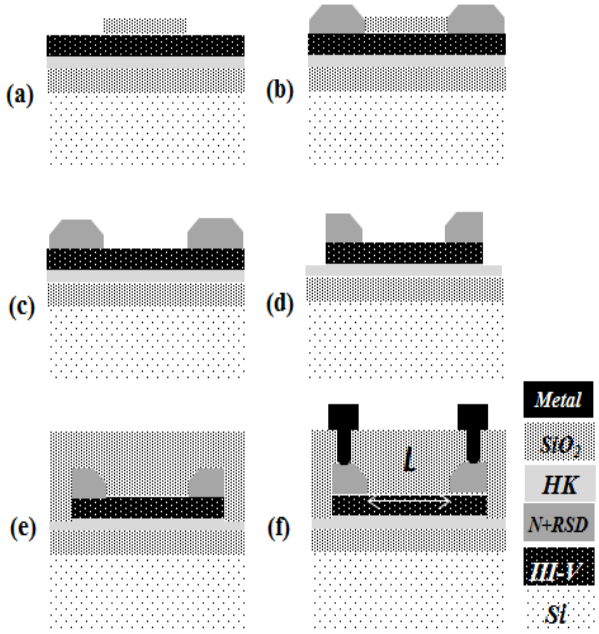

Figure 4.1: Schematic processing sequence of lateral N+NN+ test structure : (a) SiO2 hard-mask on InGaAs-OI layer with bottom passivation, (b) growth of N+ InGaAs contacts, (c) hard-mask removal, (d) mesa wet etching, (e) top passivation and interlayer dielectric deposition, (f) contact and metallization.

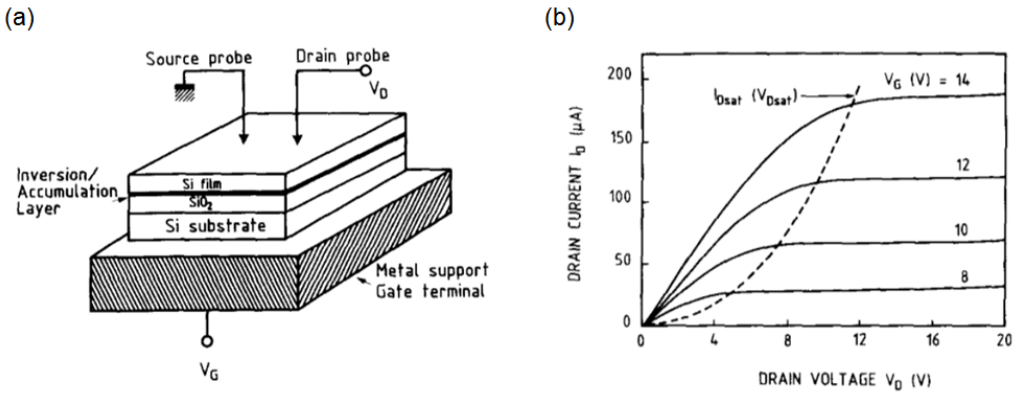

Figure 4.2: (a) Classical schematic of pseudo (Ψ)-MOS transistor in SO1 structures. (b) Typical drain current versus drain voltage curves [29].

4.2.3 Measurement Setup: Pseudo Ψ-MOSFET

The upside-down MOS structure inherent in all SOI materials is used: the bulk silicon substrate as a gate terminal, the buried oxide as the insulator, and the thin silicon overlay as the transistor body. The quality of the crystalline silicon film, buried oxide, and interfaces should be known before starting the costly processing of integrated circuits. There is a simple and reliable electrical technique called pseudo (Ψ)-MOSFET [29]. The Ψ-MOSFET takes advantage of the specific configuration of SOI structures. It allows a rapid correlation between electrical and synthesis parameters of as-grown SOI wafers. To operate in situ (without lithography/metallization) this pseudo-MOS transistor (9'-MOSFET), low-pressure probes are placed on the upper Si film forming source and drain point contacts (Fig. 4.2a) [29]. Figure 4.2b shows typical drain current I_D versus drain voltage V_D characteristics.

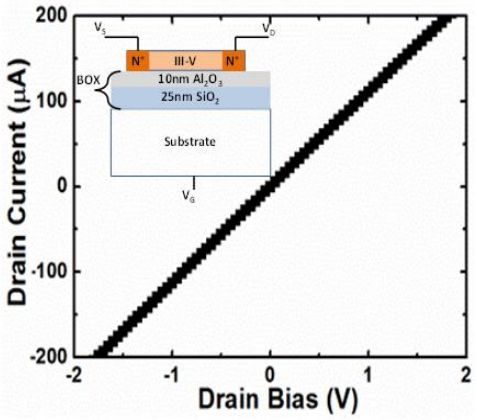

Figure 4.3: Measured drain current I_D versus drain bias V_D for gate bias V_G=0, L =200 μm and W =20 μm.

Figure 4.3 shows the schematic of the tested structures and current variation with drain bias confirms ohmic-behavior in between two contacts. InGaAs layers with different thicknesses t_{InGaAs} (25 nm, 50 nm, 100 nm and 200 nm) were fabricated on a buried oxide which is composed of 10 nm Al_2O_3 over 25 nm SiO_2. The doping concentration of the InGaAs film was of approximately 10^{16} cm^{-3}. The static analysis was performed by sweeping the gate bias V_G and measuring the drain current (I_D) between source and drain. Instead of the standard pressure probes of the Ψ-MOSFET, implemented metal contacts are used as source and drain. This configuration was established to get the material quality and avoid affecting probe-induced defects owing to the metal contacts. It is called *Pseudo*-Ψ-MOSFET. This metal pad configuration is adequate because the impact of series resistance and probe-induced defects for affecting the mobility can be reduced. The channel dimensions are also better defined by the inter-contacts distance, representing the channel length L and width W.

4.2.4 Current and Transconductance Characterization

A. Drain Current

Transfer characteristics are reported in Figure 3 for transistors with variable InGaAs channel thickness. All devices present a modulation of the drain current with gate voltage, the degree of which depends on thickness.

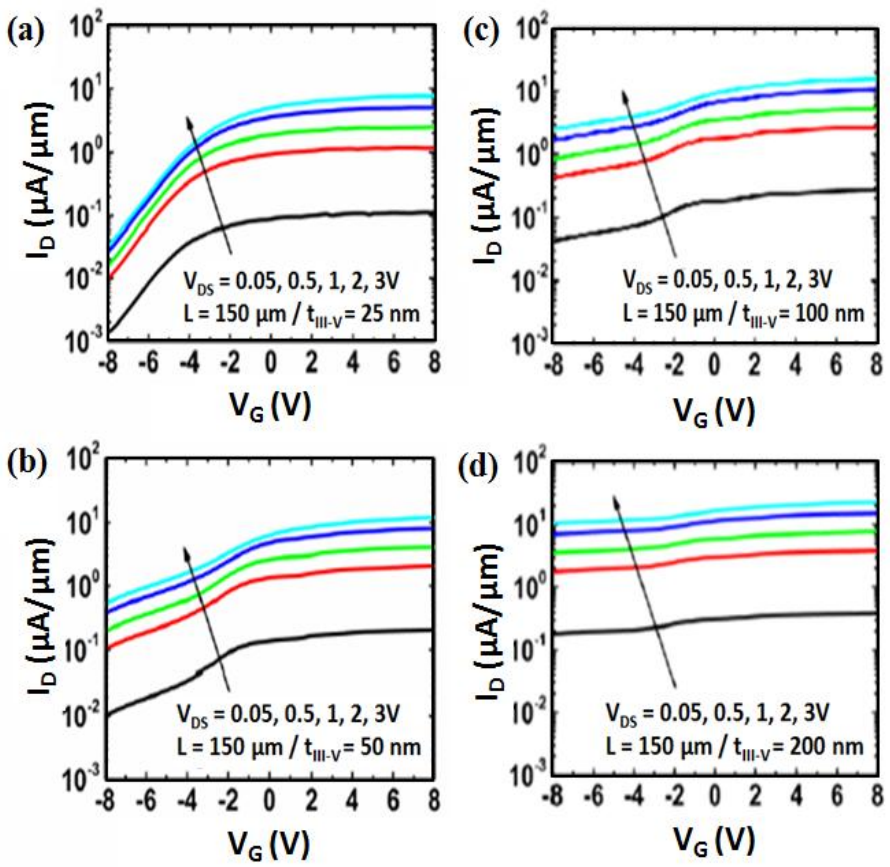

Figure 4.4: Back-gate I_D-V_G characteristics of lateral N+NN+ InGaAs-OI structures for (a) 25nm, (b) 50nm, (c) 100nm and (d) 200nm thick InGaAs film. Note the transition from full depletion (a) to partial depletion (d).

For positive V_G, the field effect induces the formation of an accumulation region at the film-BOX interface, whereas for negative V_G, the film is subject to depletion. The thinner channel (Fig. 4.4a) shows the typical signature of full-depletion operation: very low leakage current, high ON/OFF current ratio, relatively steep subthreshold slope. These parameters tend to degrade in thicker films (Fig. 4.4b, c), albeit the ON current increases. The 200 nm thick InGaAs transistor (Fig. 4.4d) operates at the limit of partial depletion since the drain current saturates and remains high for increasingly negative gate voltage.

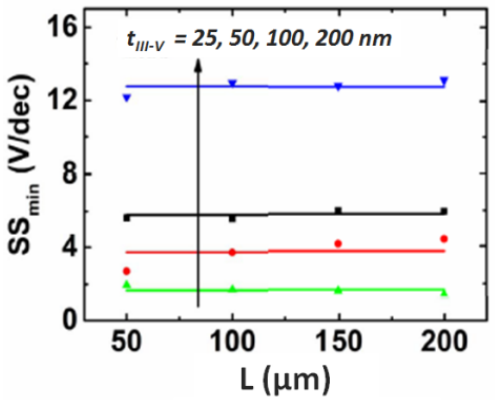

Figure 4.5: Minimum subthreshold swing (SS) versus channel length (L) for devices with InGaAs film thickness of 25nm, 50nm, 100nm, and 200 nm.

The gradual change from full depletion to partial depletion is also reflected by the variation of the subthreshold swing (SS) with thickness: SS increases massively in 200nm film (Fig. 4.5).

Figure 4.6(a) shows the ON-resistance which varies linearly with the channel length. Extrapolation of these curves to $L = 0$ indicates that all samples have a similar contact resistance (about $5\ k\Omega.\mu m$), which is rather low for InGaAs-OI samples thanks to the optimized process of the source/drain terminals. The slope of the lines indicates the sheet resistance of the film (measured at $V_G = +8\ V$), which strongly depends on thickness as illustrated in Figure 4.6(b). This curve can be modeled by considering two parallel conduction channels [32].

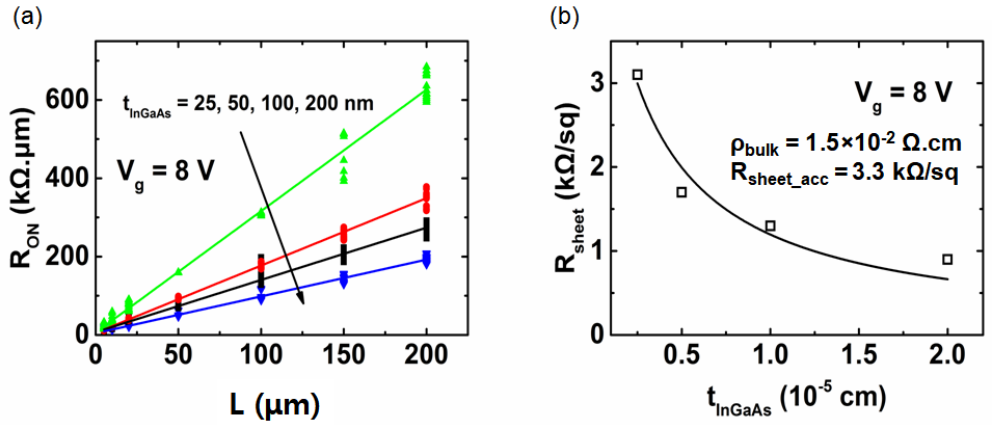

Figure 4.6: (a) On-resistance R_{ON} versus channel length L_g extracted at $V_G = 8\ V$ and $V_D = 0.05\ V$ for four different InGaAs-OI thickness. (b) Sheet resistance R_{sheet} deduced from (a) versus InGaAs film thickness fitted by a two parallel conductance model.

B. Transconductance

Figure 4.7a shows the drain current I_D (plain symbols) and associated transconductance gm (empty symbols) versus gate bias in thick InGaAs film (200nm). A plateau is visible in $I_D(V_G)$ curve for $V_G \approx 0$ and the $g_m(V_G)$ characteristic features two unusual peaks. It is known that in conventional

MOSFETs the derivative of the transconductance with respect to gate bias yields one peak, the position of which indicates the threshold voltage [33]. In our samples, there are two clear peaks (see Fig. 4.7b) which give evidence for a double conduction mechanism in the InGaAS film. Since the films are doped, bulk conduction is possible even in absence of V_G. A negative gate bias induces a depletion region at the film-BOX interface, which modulates the thickness of the conduction volume.

The left peak in Figure 4.7b, obtained for negative gate bias, indicates the threshold voltage V_T. This means that for $V_G > V_T$, the depletion region starts to shrink. The right peak corresponds to the flat-band voltage V_{FB} that defines the onset of the accumulation channel [23]. Beyond flat-band voltage ($V_G > V_{FB} \approx +1.1$ V), an accumulation channel forms at the InGaAs-BOX interface and adds to the bulk conduction. We call these mechanisms *bulk conduction* and *surface conduction*.

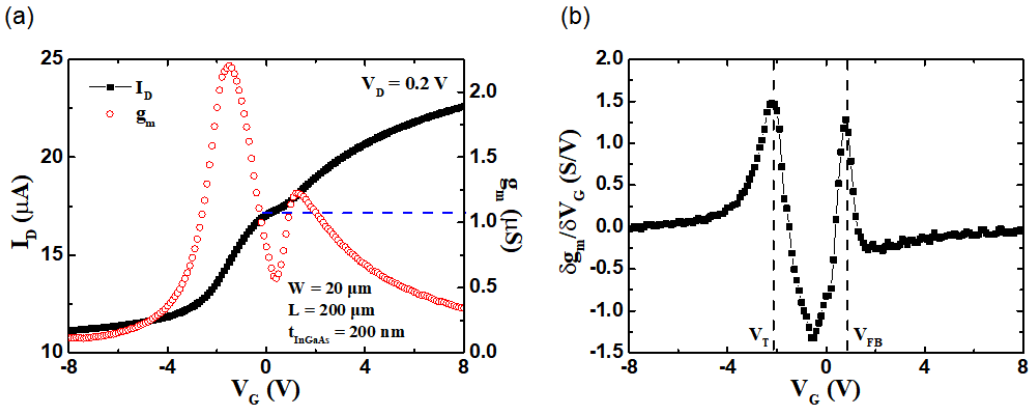

Figure 4.7: (a) Drain current I_D (plain symbols) and transconductance g_m (empty symbols) versus gate bias. The dashed line represents the 'bulk' current I_{Vol}. (b) Corresponding g_m derivative versus V_G, which features a double threshold voltage behavior. t_{InGaAs} = 200 nm, W = 20 µm, and L = 200 µm.

The double-peak shape of the transconductance evolves to a single-peak in very thin films where the contribution of the neutral volume to drain current tends to vanish. For 25nm thick film and long channel device (L = 200 µm), the second peak of transconductance is hardly visible as shown in Figure 4.8.

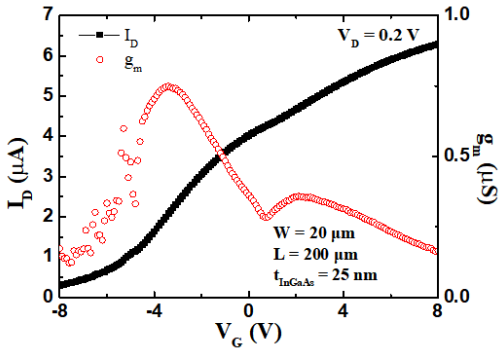

Figure 4.8: Drain current I_D (black solid symbols) and transconductance g_m (red empty symbols) as a function of gate bias. t_{InGaAs} = 25 nm, W = 20 µm, and L = 200 µm.

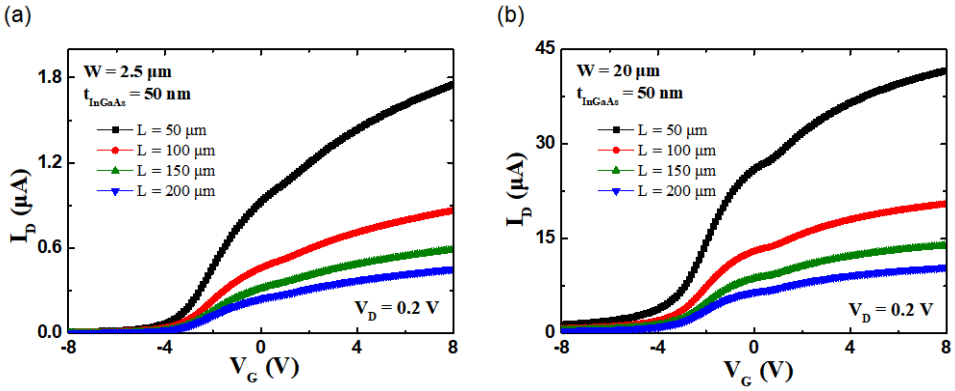

Figure 4.9: Drain current I_D versus gate bias for different channel lengths, from 50 µm to 200 µm, showing the width dependency. (a) W = 2.5 µm, (b) W = 20 µm. t_{InGaAs} = 25 nm and V_D = 0.2 V.

Figure 4.9a shows well behaved drain current (I_D) transfer characteristics of a relatively narrow device (W = 2.5 µm) with different channel lengths. For a wide device (W = 20 µm), the drain current follows same tendency except for the much higher magnitude of current level (Fig. 4.9b). Figure 4.10 presents characteristics measured in devices with different thicknesses, long channel and variable widths: W = 2.5 µm (Fig. 4.10a), W = 5 µm (Fig. 4.10b), W = 10 µm (Fig. 4.10c), and W = 20 µm (Fig. 4.10d). Here is noted that 100 nm and 200 nm thick devices behave as partially depleted, except when the width is minimized (W = 2.5 µm).

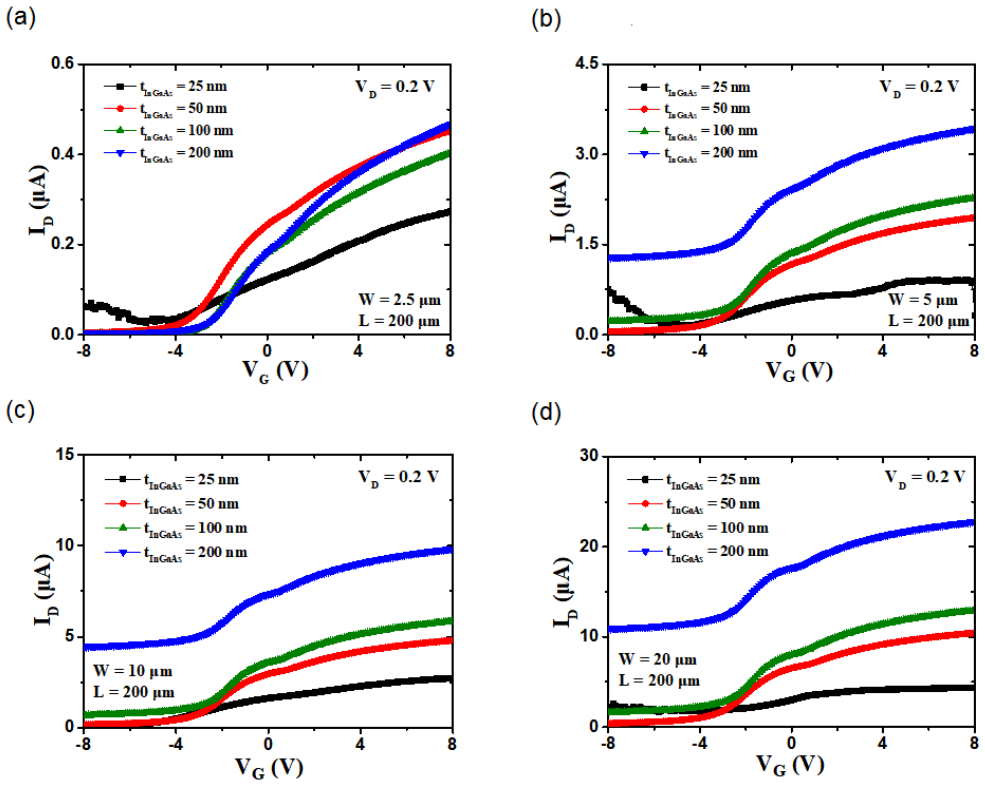

Figure 4.10: Drain current I_D versus gate voltage for long device widths and different thickness of InGaAs film. (a) W = 2.5 µm, (b) W = 5 µm, (c) W = 10 µm, and (d) W = 20 µm with a long length (L = 200 µm). V_D = 0.2 V.

4.2.5 Mobility Evaluation

A. Partial and Full Depletion

Before attempting to extract the mobility, we need to evaluate whether the films are fully depleted or not. Given a doping level N_D, it is possible to compute the maximum width W_{d_max} of the depletion region in the InGaAs film [34]:

$$W_{d\_max} = \sqrt{\frac{4 \cdot \varepsilon_{III\text{-}V} \cdot k \cdot T \cdot \ln\left(\frac{N_D}{n_i}\right)}{q^2 \cdot N_D}} \tag{1}$$

where $\varepsilon_{III\text{-}V}$ and n_i are the InGaAs dielectric constant and the intrinsic doping concentration. According to the film quality, $\varepsilon_{III\text{-}V}$ can vary between $13.1 \cdot \varepsilon_0$ and $14.1 \cdot \varepsilon_0$ [35], where ε_0 is the vacuum permittivity.

Considering $n_i = 6.3 \cdot 10^{11}\ cm^{-3}$ [35], the maximum depletion width is between *197 nm* and *205 nm*, which means that films thinner than *200 nm* are definitely fully depleted. In contrast, the *200 nm* thick layer is at the boundary between partial and full depletion. Figure 4.11 reports the measured $I_D(V_G)$ curves in thick devices with same length ($L = 200\ \mu m$) and different widths. Wide transistors are clearly partially depleted with large I_D current flowing in the un-depleted region of the film. But, interestingly, the narrower device ($W = 2.5\ \mu m$) exhibits full depletion, suggesting a 2D mechanism[36]: the lateral depletion, assisted by defects and charges located on the sidewalls, reinforces the vertical depletion induced by the gate.

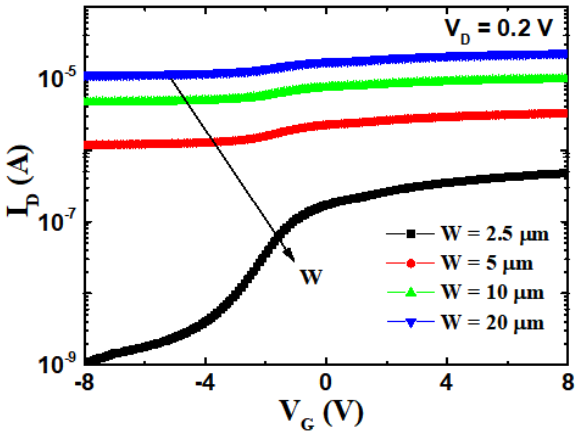

Figure 4.11: Drain current characteristics I_D versus gate bias V_G with different widths. $t_{InGaAs} = 200$ *nm*, $L = 200$ *µm and* $V_D = 0.2$ V.

B. Bulk Mobility

According to the approach developed by Liu *et al.* [37] for heavily doped Si layers, the drain current in bulk conduction regime can be written as:

$$I_D = \frac{W}{L} \cdot C_{BOX} \cdot \mu_{Vol} \cdot V_D \cdot (V_G - V_0) \tag{2}$$

where C_{BOX} is the buried oxide capacitance and V_0 is a characteristic voltage which may enable full depletion of the channel [37] :

$$V_0 = V_{FB} + \frac{q \cdot N_D}{C_{BOX}} \cdot t_{III\text{-}V} \tag{3}$$

N_d is the active doping concentration. Eq. (2) accounts for the thickness variation of the neutral (undepleted) region with gate bias. In highly doped, partially depleted films, V_0 is hypothetical, as it cannot be reached experimentally; it is extrapolated from the measurements. In principle, the bulk mobility μ_{Vol} is independent on gate bias unless the film has to be inhomogeneous with vertical profiles of mobility, defects and dopants. It may also depend on the vertical field induced by surface charges, in particular when the neutral region becomes very thin. The device ON-resistance includes the contribution of the series source/drain resistance R_{SD}:

$$R_{ON} = \frac{V_D}{I_D} = R_{SD} + \frac{L}{W \cdot C_{BOX} \cdot \mu_{Vol} \cdot (V_G - V_0)} \tag{4}$$

Rewriting I_D, we obtain:

$$I_D = \frac{W}{L} \cdot C_{BOX} \cdot \frac{\mu_{Vol}}{1 + \theta_1 (V_G - V_0)} \cdot (V_G - V_0) \cdot V_D \tag{5}$$

where

$$\theta_1 = R_{SD} \cdot \mu_{Vol} \cdot C_{BOX} \cdot \frac{W}{L} \tag{6}$$

The transconductance is:

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{W}{L} \cdot C_{BOX} \cdot \frac{\mu_{Vol}}{[1 + \theta_1 (V_G - V_0)]^2} \cdot V_D \tag{7}$$

This equation explains the transconductance variation with gate voltage in bulk conduction regime. Since the difference (V_G-V_0) can be very significant, especially for thick films, the transconductance decay with V_G is abrupt, as shown in Fig. 6a.It follows that the bulk mobility extracted from either Eq. 2 or transconductance peak is highly underestimated due to the series resistance effect. This problem can be circumvented by constructing the Y-function:

$$Y_{Vol} = \frac{I_{Vol}}{\sqrt{g_m}} = \sqrt{\frac{W}{L} \cdot C_{BOX} \cdot \mu_{Vol} \cdot V_D \cdot (V_G - V_0)} \tag{8}$$

where the impact of R_{SD} is erased.

Drawing Y_{Vol} versus V_G results in a straight line region, more pronounced in long devices (Fig. 4.12). The intercept with the horizontal axis yields V_0, and the slope gives the bulk mobility:

$$\mu_{Vol} = \frac{Slope^2}{\frac{W}{L} \cdot C_{BOX} \cdot V_D} \tag{9}$$

This methodology is similar to the Y-function technique used in inversion-mode MOSFETs [38] except that μ_{Vol} and V_0 have different meaning.

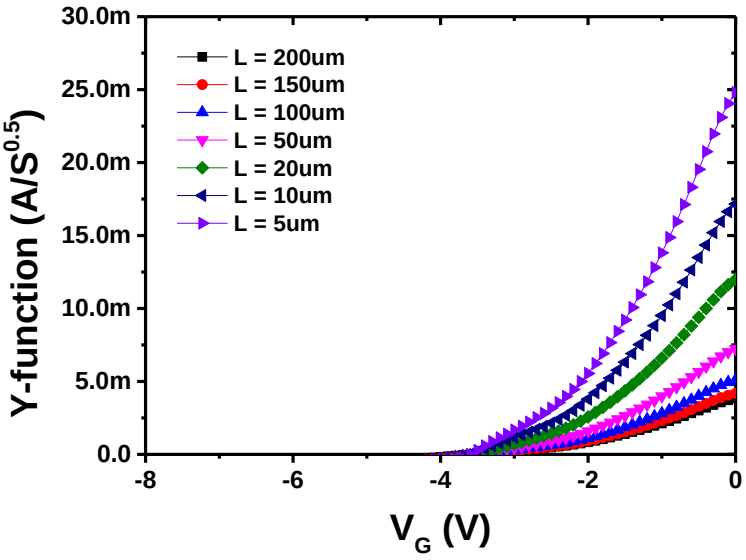

Figure 4.12: Y-function in depletion regime $Y_{vol}(V_G)$ for 200 nm thick InGaAs devices with different gate lengths. For W =10 um and V_D = 0.2 V.

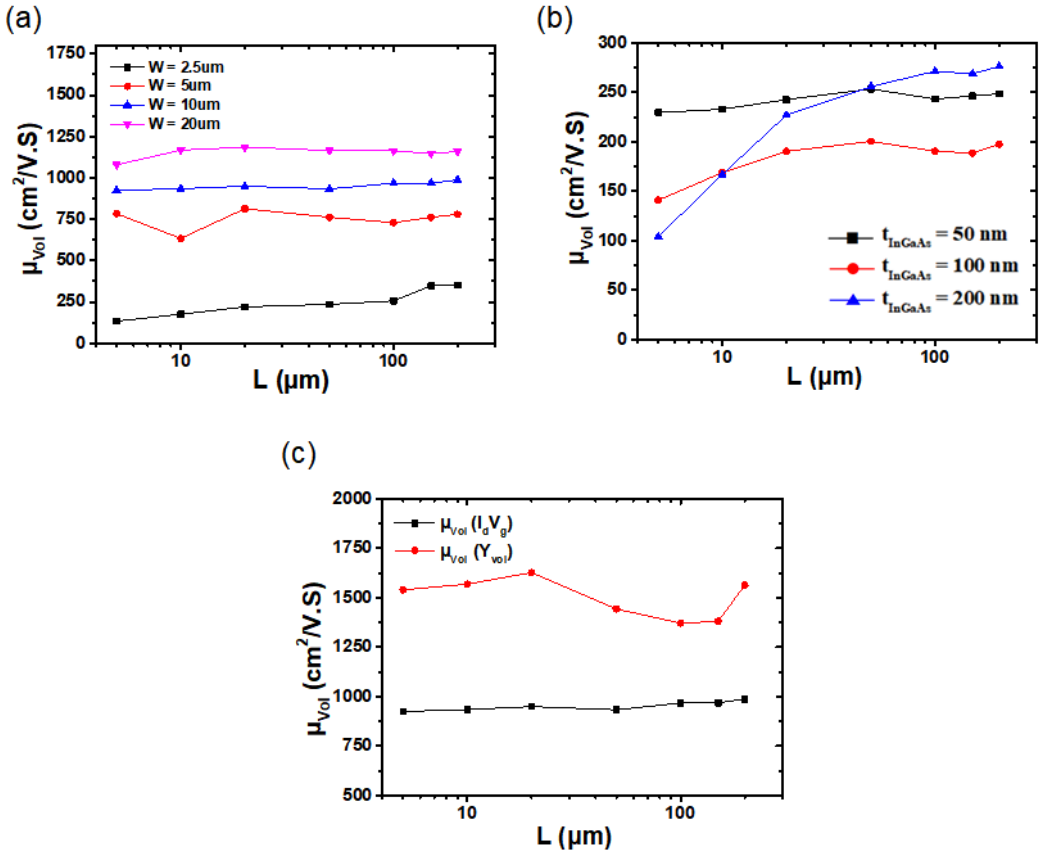

Figure 4.13: Extracted bulk mobility versus channel lengths in (a) 200 nm thick films with variable width and (b) narrow devices of 2.5 um with different thickness. (c) Comparison of bulk mobility values extracted from $I_D(V_G)$ curves with Eq.(2) or by using Y_{vol}-function method (Eq.(8)). For W = 10 μm, t_{InGaAs} = 200 nm, V_D = 0.2 V.

The extracted μ_{Vol} (Fig. 4.13a) is rather constant with the gate length L. The bulk mobility reaches 1200 $cm^2/V.s$ in thick and wide devices (Fig. 4.13a). Net mobility degradation is noticed in 25–50nm thick films and also in narrow devices (Fig. 4.13a, b), where carrier scattering on the sidewalls comes into play. Figure 4.13c compares the bulk mobility extracted from $I_D(V_G)$ curves with Eq. (2) and from Y_{Vol}-function. The latter method is not affected by source and drain series resistance and provides at least 40% higher mobility. The series resistance is included in coefficient (see Eq.(6)) which can be determined from the slope of $1/\sqrt{g_m}$ versus V_G curve:

$$\frac{1}{\sqrt{g_{m(}V_{G)}}} = \frac{1+\theta_1 \cdot (V_G - V_0)}{\sqrt{C_{BOX} \cdot \frac{W}{L} \cdot \mu_{Vol} \cdot V_D}} \qquad (10)$$

Figure 4.14 confirms the linear variation of $1/\sqrt{g_m}(V_G)$ curves in bulk conduction mode. Using this method (Eq. (10)), the extracted coefficient θ_1 is around 0.5 V^{-1} for all devices, which implies that the series resistance increases in longer channels.

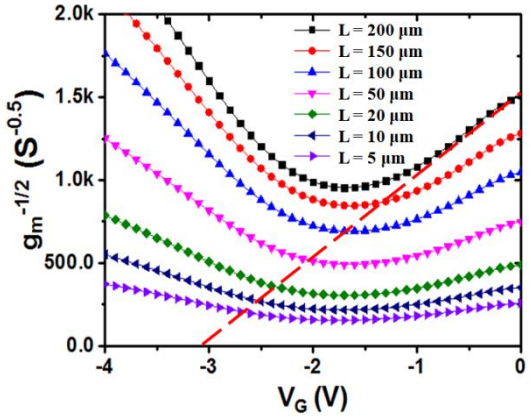

Figure 4.14: Plot of $1/\sqrt{g_m}$ versus V_G in bulk conduction (on right region). The dotted line shows the linear fit with Eq.10 in order to determine coefficient θ_1 and the series resistance. W=10 µm, $t_{III\text{-}V}$ = 200nm, V_D = 0.2 V.

C. Surface Mobility

Surface conduction occurs for $V_G > V_{FB}$, when the accumulation channel starts forming at the film-BOX interface and adding to the bulk current flowing in the whole neutral film. The surface current is given by the difference between the total current I_D and the maximum bulk current $I_{Vol,m}$ measured at $V_G = V_{FB}$ (see dashed line in Fig. 4.6a).The surface mobility μ_S at the film-BOX interface is obtained from another version of the Y-function (Y_S) adapted to the accumulation current [38]:

$$Y_S = \frac{I_D - I_{Vol}}{\sqrt{g_m}} = \sqrt{\frac{W}{L} \cdot C_{BOX} \cdot \mu_s \cdot V_D \cdot (V_G - V_{FB})} \tag{11}$$

The curves $Y_S(V_G)$ are linear as shown in Figure 4.15. The flat-band voltage V_{FB} is determined from the intercept with the gate voltage axis and the surface mobility in the accumulation channel from the slope, as indicated in Eq. (11).

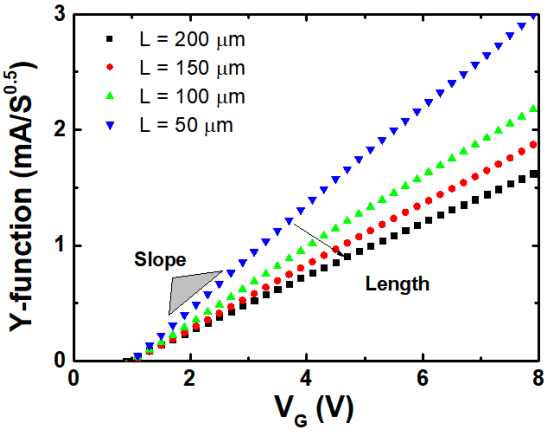

Figure 4.15: Y_S-function in accumulation regime $Y_S(V_G)$ for W= 20 µm, t_{InGaAs} = 200 nm thick InGaAs devices with different gate lengths. V_D = 0.2 V.

Figure 4.16 shows the surface mobility μ_S versus gate length. The μ_S is significantly lower than the bulk mobility μ_{Vol} by a factor of two due to stronger field-effect and additional carrier scattering at the interface film-BOX [18]. The μ_S is superior in thick films (100-200 nm) where the coupling between top surface defects and bottom channel is attenuated. The quality of the InGaAs-BOX interface is assumed constant given the stability of the fabrication process. The lowest mobility is measured for 25 nm thick devices and is attributed to the charged defects exist in the top surface. The difference between the front-surface and back-surface potentials induces a vertical field, $E_{int} = (\Psi_{S1} - \Psi_{S2})/t_{InGaAs}$, that obviously increases in thinner films [39]. Even thought the influence of the gate-induced field is ignored in Y-function, the mobility is still affected by the intrinsic field. In other words, the genuine low-field mobility is not accessible.

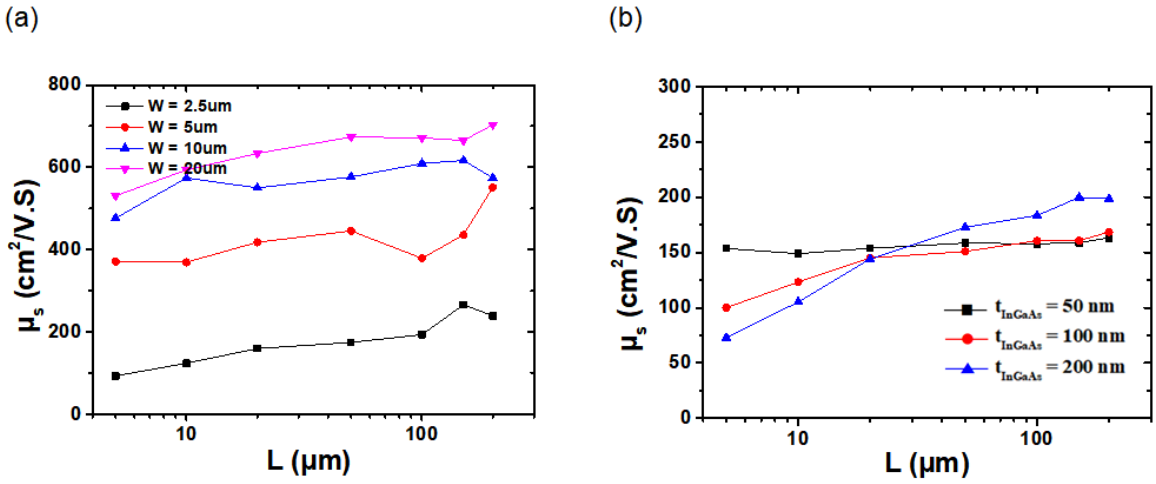

Figure 4.16: Extracted surface mobility versus gate length in (a) 200 nm thick devices with different widths, and (b) narrow devices of 2.5 μm with variable thickness. V_D = 0.2 V

D. Low-temperature Measurements

Figure 4.17a shows the drain current versus gate bias characteristics measured at different temperatures *T*. As reported for junctionless devices [40], the drain current in accumulation regime increases at lower temperature primarily because the mobility is improved (reduced phonon scattering). At the same time, the flat-band voltage (empty symbols in Fig. 4.17b) increases which delays the formation of the accumulation channel. Fig. 4.17b also presents the subthreshold swing *S* (plain symbols) versus *T*. A linear decrease of *S* with temperature is found between 200 K and 300 K, already documented for undoped MOSFETs [7]. The swing tends to saturate below 150 K, presumably due to the increase of the effective density of traps.

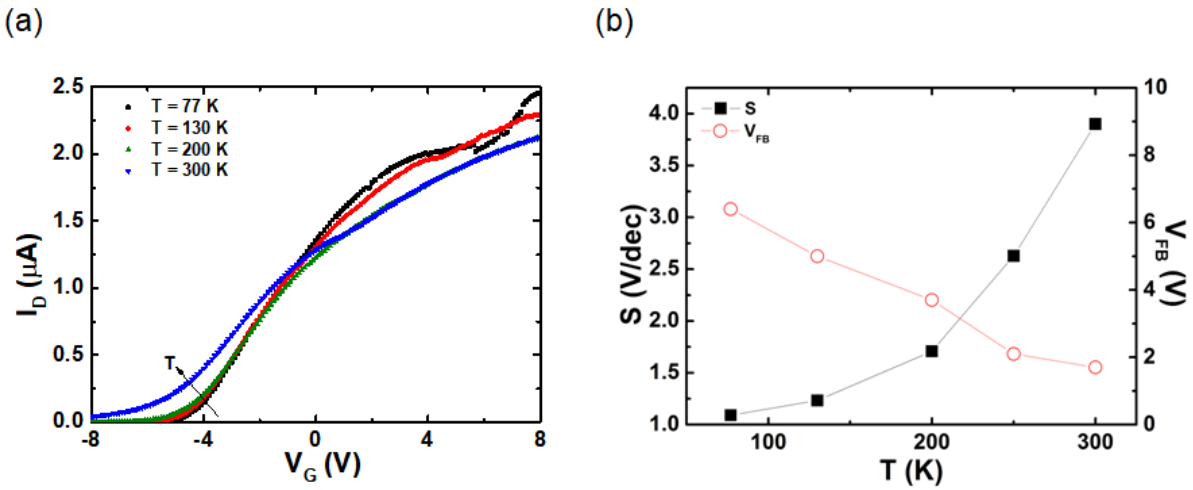

Figure 4.17: (a) Drain current as a function of gate bias measured at variable temperature. (b) Associated variations of sub-threshold swing S and flat-band voltage V_{FB} with low temperature T. For t_{InGaAs} =25 nm, W = 5 μm, L = 100 μm, and V_D = 0.2 V.

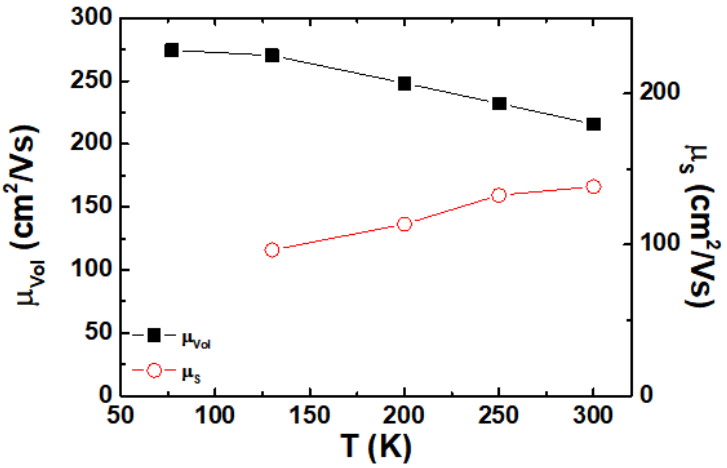

Figure 4.18: Bulk μ_{vol} and surface mobility μ_S as a function of temperature T.

Figure 4.18 shows bulk (μ_{vol}) and surface mobility (μ_s) as a function of temperature. Bulk mobility increases at low temperature. The reason is that phonon scattering is reduced and the doping is insufficient to have dominant coulomb scattering. However, the surface mobility clearly decreases at low temperature. This behavior can be explained by the increase of surface scattering due to higher density of interface traps.

E. Strain Effect

Samples are diced in 2 cm x 3 mm pieces and mounted in a 3-point bending setup (Fig. 4.19) where uniaxial tensile strain can be applied up to 0.2 % without breaking the samples. The ON-current

I_{ON} benefits from tensile strain applied along the <110> transport direction and increases at a rate of 10-15% per percent of strain (Fig. 4.20).

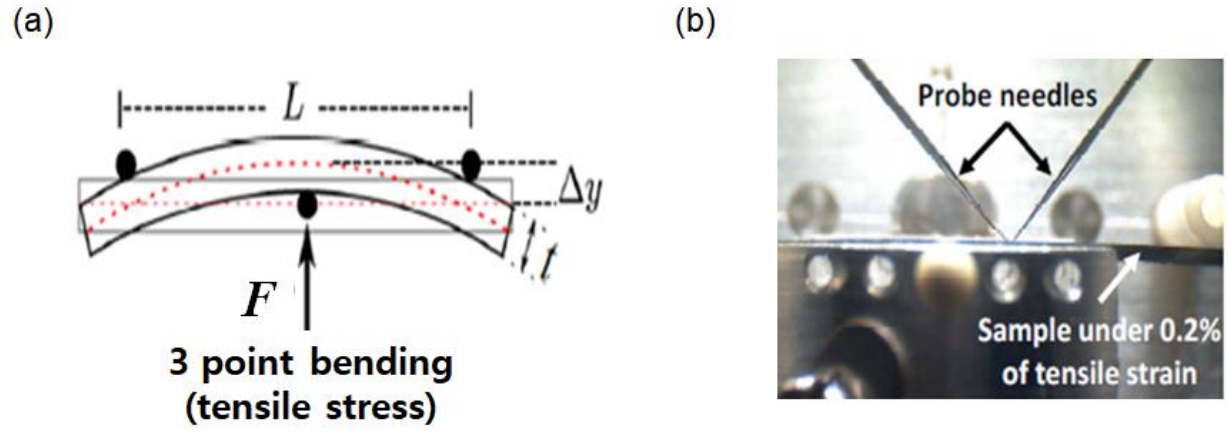

Figure 4.19: (a) Schematic of 3-point bending configuration used to apply uniaxial tensile strain on the sample. (b) Pictured from the side of the 3-point bending setup showing the semiconductor layer under tensile strain and the contact probes.

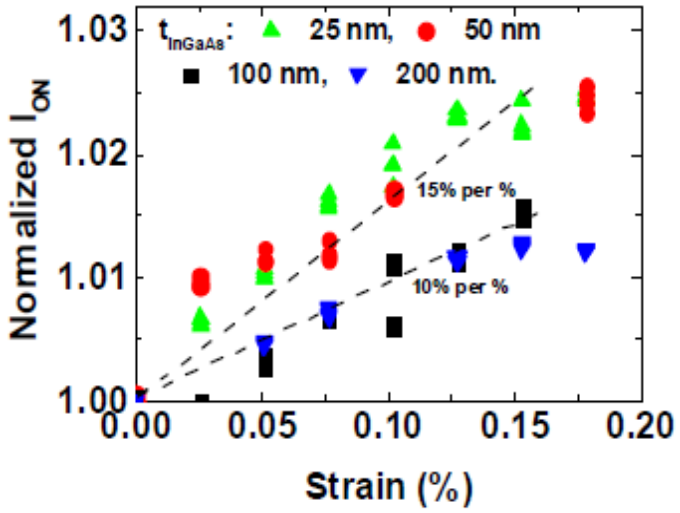

Figure 4.20: Improvement rate of I_{ON} (at Vg = 8 V) versus uniaxial tensile strain for different InGaAs-OI thicknesses.

4.2.6 Summary

We have fabricated and characterized back-gated accumulation layer MOSFETs on InGaAs-on-Insulator wafers. These simple test structures are intended to provide a quick feedback for InGaAs technology optimization. Detailed measurements point out the coexistence of two conduction mechanisms (bulk and interface accumulation). The plateau present in $I_D(V_G)$ curves and the double-peak transconductance reveal the transition from bulk conduction to surface-dominated conduction. A

methodology was proposed for the extraction of carrier mobility in the neutral volume and at the film-BOX interface. The bulk mobility is always higher than the surface mobility and exceeds 1100 cm^2/V.s in 100-200 nm thick InGaAs films. The lowest mobility was measured on very thin (*25 nm*) layers which suffer from strong coupling between top interface defects and conduction channel. The InGaAs material properties were also investigated as a function of aspect ratio and low-temperature operation. Finally, uniaxial tensile strain in the <110> transport direction highlighted the improvement the on-current with a rate of 10-15% per percent of strain.

4.3 Transducers using Z^2-FET

4.3.1 Introduction

The Z^2-FET features zero subthreshold-swing (<1 mV/decade of current) and zero impact ionization. This device is capable of transducer applications. The Z^2-FET is a simple p-i-n structure which has a partially covered gate electrode. Indeed, there are two regions: one is underneath the front-gate (L_G) and the other is an opened surface (L_i) as depicted in Figure 4.21. The two regions, i.e. L_G and L_i, are controlled by the front- and back-gate bias. It means that carrier concentration can be manipulated by the gate voltage. This is the concept of electrostatic doping [12], [41]. We use the device in forward mode (V_A > 0 V) where sharp switching is observed. The electrostatic doping can be obtained by either applying voltage via gates [12], [41]or by depositing impurities on the surface of the un-gated region [14]. The un-gated region plays an important role in changing the electrical conduction as a trigger. For sensing applications, in particular, this region is used to detect external inputs such as mechanical force, chemical species deposition the surface, thermal variation, magnetic field, and illumination.

4.3.2 Z^2-FET Device Operation

Figure 4.21 shows the family of Z^2-FET devices: (4.21a) standard Z^2-FET, (4.21b) Z^2-FET with dual ground-plane and (4.21c) Z^3-FET without front-gate. The standard Z^2-FET is a PIN diode,

similar to a TFET but operated in forward-bias mode. Electrostatic barriers are formed, via gate disposition and biasing, to prevent electron/hole injection into the channel until the gate or drain bias reaches a turn-on value. The front and back gates induce electrostatic doping in the undoped body so the device looks like an N^+PNP^+ thyristor, although the mechanisms of operation differ [42]. The gate action leads to band modulation along the channel that blocks the current flow. A positive feedback mechanism between the electron and hole injection barriers causes the device to abruptly switch (< 1 mV/decade) from OFF state with low leakage current to ON state with high drive current. Other band-modulation devices have recently been proposed for sharp switching, ESD protection, and memory applications [43]–[47]

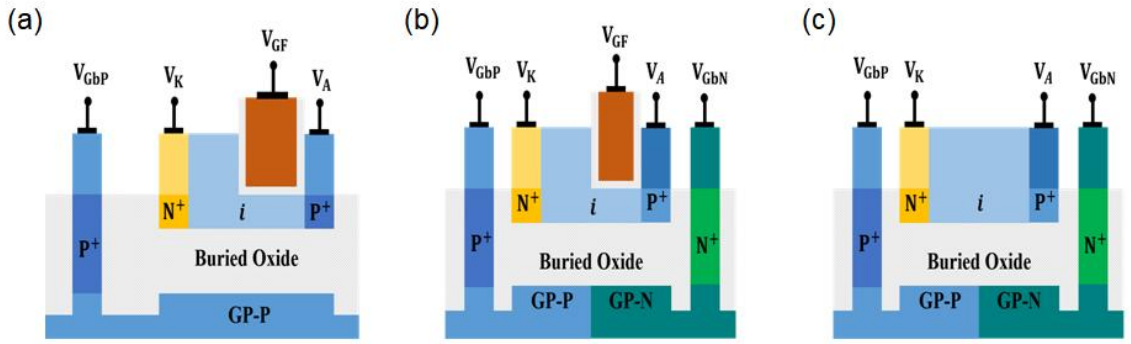

Figure 4.21: Schematic view of different band-modulation Z-FET devices: (a) standard Z^2-FET (b) Z^2-FET with dual ground-plane and (c) Z^3-FET without front-gate.

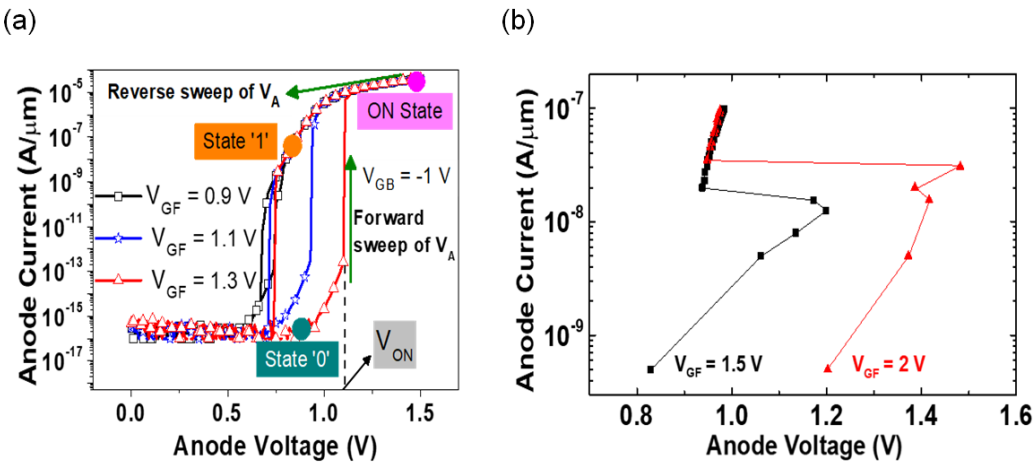

Figure 4.22: Experimental I_A-V_A curves for different gate voltages in quasi steady-state (DC mode). Measurements were performed by setting the gate biases for several seconds, then (a) slowly scanning the anode voltage to reveal the hysteresis or (b) forcing the anode current to reach the S-shaped curve. $L_G = L_{int}$ = 200 nm.

The Z^2-FET is a partially gated P-I-N diode as illustrated in Figure 4.21a. The cathode (N^+ doped source) is grounded and the anode (P^+ doped drain) is positively biased. In 28 nm FDSOI [48] technology, the Z^2-FET features undoped ultrathin silicon film (t_{Si} = 7 nm), thin buried oxide (t_{BOX} = 25 nm) and raised epitaxial layer (t_{epi} = 15 nm) in the drain, source and ungated regions to reduce the series resistance [49]. The front-gate ($V_{GF} > 0$) and back-gate (ground-plane, $V_{GB} < 0$) are biased to

form a virtual NPNP structure, blocking the electron injection from cathode and the hole injection from anode. Fig. 4.22a shows typical hysteresis in I_A-V_A characteristics measured by scanning the anode bias (with a voltage source). The hysteresis originates from an *S*-shaped I-V characteristic that can actually be measured by imposing the anode current with a current source (Fig. 4.42b). For low anode voltage, the barriers created by the gates maintain the device in OFF state ('0'). When the turn-on voltage V_{ON} is reached, the feedback mechanism makes the injection barriers to collapse and the current reaches the normal value of a PIN diode (‘1’ state). The switching mechanism is strongly dependent on the modification of the minority carrier concentrations (electrons in the ungated P-region and holes in the gated N-region). The quasi-Fermi levels evolve significantly during the memory cycle. In the hysteresis window, for the same value of V_A, two different currents are observed which can be used as state ‘1’ and state ‘0’ for a static memory (1T-SRAM). We will see that the 1T-DRAM is more complex being governed by non-equilibrium conditions which shift the memory window, V_{ON} and reading voltage to higher V_A.

The band-modulation effect results in sharp transition from low to high current, with an I_{ON}/I_{OFF} ratio of 8 decades (Fig. 4.22). The turn-on voltage and the hysteresis window are enlarged by increasing the barrier heights via $V_{GF, GB}$. For reverse V_{GF} scan, the device remains in ON state until it reaches a point (~ 0.7 V) at which it turns OFF. The two equilibrium states, ‘0’ and ‘1’, are shown in Figure 4.22a. As the hysteresis is achieved with V_A and V_{GF} of about 1 V, the Z^2-FET is attractive for low-power embedded memory applications.

The schematic description above, using the feedback between energy barriers and carrier injection, does not capture the full complexity of the operation mechanisms in Z^2-FET. A detailed physics-based model has been derived by Taur [42]. The leading idea is the continuity of the total current for each of the three P-N junctions: at anode, at cathode and in the center of the body. The model includes the generation-recombination (GR) and diffusion currents for electrons and holes and accounts for the rapid variation of the quasi-Fermi levels with bias. MOS equations define the concentrations of electrons N^* and holes P^* (‘electrostatic’ doping [41]) in the gated and ungated regions, respectively. 5 equations are sufficient to reproduce the hysteresis and S-shape of DC characteristics. Each step of this continuous model was backed by exhaustive numerical simulations.

In the following sections, we present two types of sensing applications: a magnetodiode and an optical detector. The mechanisms of device operation depend on the external inputs: a magnetic field or light. These input signals are precisely collected (or detected) through the un-gated region. This leads directly a change of carrier concentration and spatial distribution in the intrinsic region during device operation. In other words, the electrostatic doping profile (or less carrier density) is changed in the un-gated region. Consequently, the output current is inevitably varied as expected for sensing characteristics.

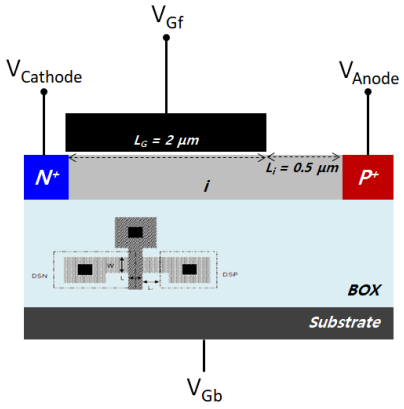

Figure 4.22: A schematic of a partially gated p-i-n diode with opened surface (L_i).

4.3.3 Magnetic Sensor

In general, Van-der-Pauw and MOS-Hall devices [10] are typical magnetic sensors. Most magnetic sensors are based on the Hall Effect, thus we describe the fundamentals in terms of the magnetic sensing operation.

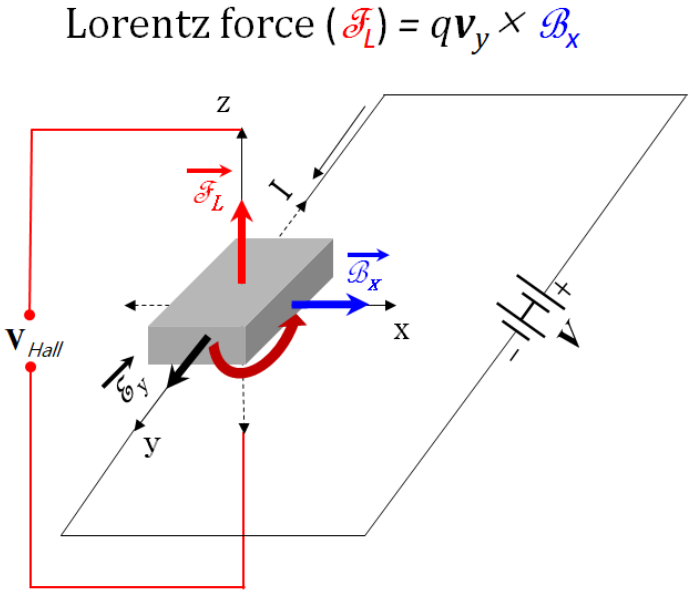

Figure 4.23: Basic setup for measuring the Hall voltage (V_{Hall}).

Figure 4.23 shows a basic setup for identifying the substrate type and carrier concentration by measuring the Hall voltage. An electric field (*E*) and magnetic field (*B*) are applied perpendicularly to each other on y- and x-axis as depicted (Fig. 18). For example, in a p-type substrate, the Lorentz force exerts an average upward force on the majority carrier in the substrate, therefore piling up electrons

and holes at the top side of the substrate. The Hall voltage (V_H) can thus be measured externally [34].

In ambipolar samples, the Lorentz force (F_L) under the magnetic field can force both types of charge carriers to be piled up on the one side in the silicon body. This implies that the deflected holes and electrons can recombine at the same surface. Based on this principle, an SOI magnetodiode can be used for magnetic sensing operation [9], [11], [50]. This device is simply based on the p-i-n structure. While the device is under the forward mode, electrons and holes can easily be injected into the intrinsic layer from the N^+ and P^+ junctions, imposing double injection conditions [9]. In relation to what we have previously said about the Hall effect, when a magnetic field is applied laterally across the current direction of a PIN diode, electrons and holes carriers in the body will be shifted either upward or downward by the Lorentz force. This implies that it would be possible to control the amount of the recombination current by manipulating the magnetic field. If the quality of the top and bottom interfaces is different, then the magnetodiode signal will differentiate the polarity and intensity of the magnetic field.

The PIN diode with partially covered gate material is an adequate device that contains a high density of trap sites at the front surface (Fig. 4.24). When the gate-controlled PIN diode is under the forward mode (V_A > 0 V) without external gate biases (V_{Gf} = V_{Gb} = 0 V and B = 0 T), the intrinsic layer in the L_i is filled with many of injected holes and electrons. Accordingly, the measured current is that of a normal diode (black curve in Fig. 4.24). As soon as the magnetic field (B = 0.5 T) is applied to the diode, however, the current is slightly enhanced. That is because the F_L (Lorentz force) pushes down the carriers to the bottom interface where the interface traps are relatively less numerous than in the uncovered gate region. The recombination rate is reduced at the bottom interface accordingly; therefore the total current can be changed as shown in Figure 4.24 (red curve).

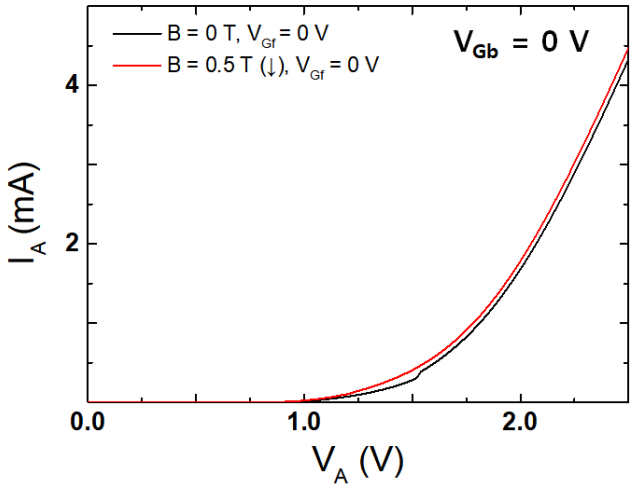

Figure 4.24: Current-voltage characteristics of a p-i-n diode under magnetic field (red line) and without magnetic field (black line). L_G = 2 μm, L_i = 0.5 μm, B= 0 or 0.5 T, and V_{Gf} = V_{Gb} = 0 V.

4.3.3.1 Measurement Setup

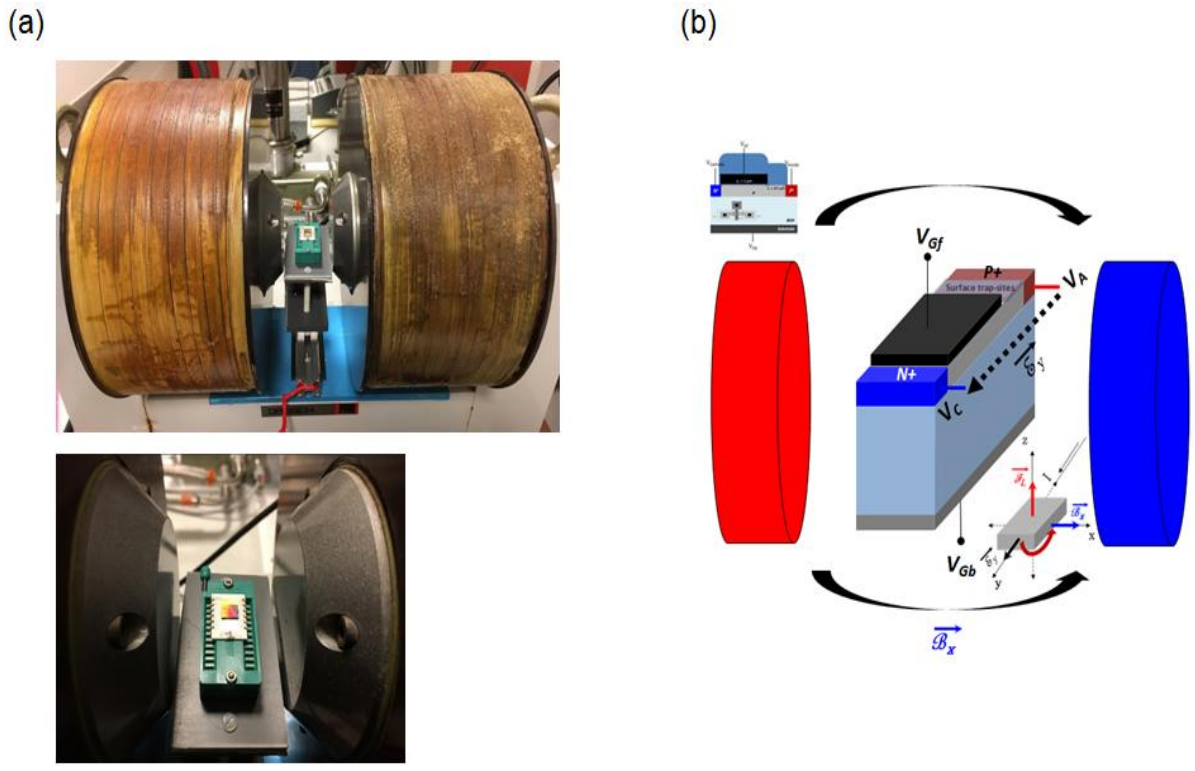

Figure 4.25: (a) A test chip placed in between two magnets, and (b) a schematic for measuring current under the magnetic field.

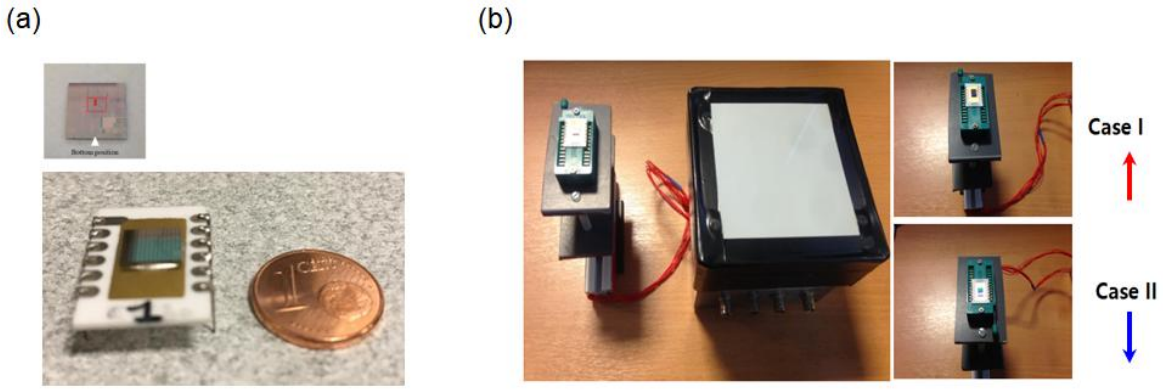

Figure 4.26: (a) Test devices wired on the special package, (b) support fixture for pinning the test device in between two magnets.

Figure 4.25a shows the equipment for generating the magnetic field. The test chip is placed in the middle of the magnet (Fig. 4.25a). The packaged test chip (Fig. 4.26a) is connected to a control panel as pictured in Figure 4.26b and then evaluated through a semiconductor analyzer, *B1500A*. We used B = 0.5 T magnetic field. The experiments were performed at room temperature.

4.3.3.2 DC characteristic under Magnetic Field

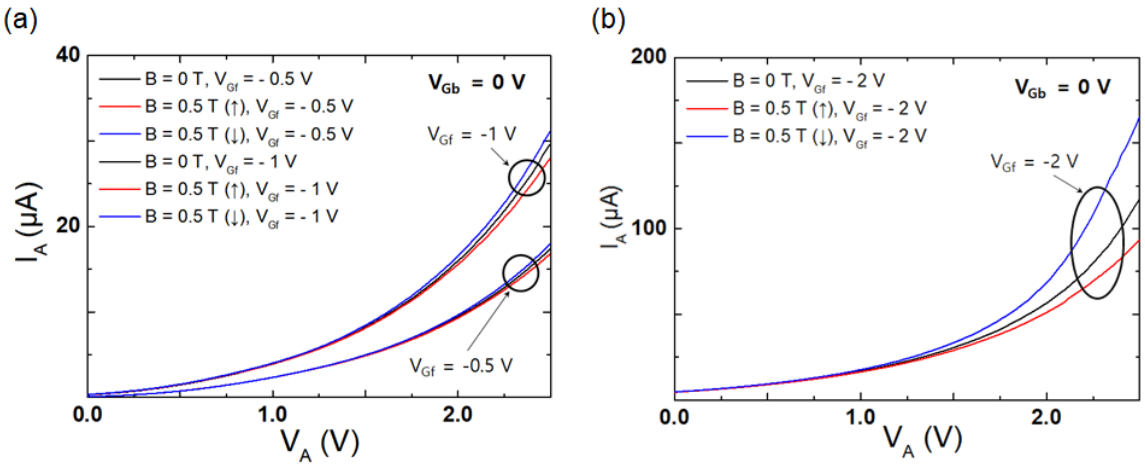

Figure 4.27: I_A (V_A) with magnetic field for (a) V_{Gf} = -0.5, 1 V and (b) V_{Gf} = -2 V. L_G = 2 μm, L_i = 0.5 μm, V_{Gb} = 0 V.

The Z^2-FET structure has been used to verify the magnetic sensing characteristics in DC mode. In order to change the current direction under the magnetic field, the supporting fixture for test devices has been placed between the electromagnet poles and configured in two cases as pictured in Figure 4.26b. Current-voltage characteristics in DC mode experimentally confirm the magnetodiode properties: the current is enhanced when the carriers are detected toward the non-defective interface. Since the recombination rate is reduced, the average carrier density is higher, thereby enabling more current to flow. Figure 4.27 demonstrates the possibility for magnetic sensor application via Z^2-FET structure. For the upward direction of the Lorentz force (red curves), the current is less because carriers can be rapidly recombined at the defective surface. Conversely, for the downward direction (blue curves), the currents are indeed increased thanks to the relatively high-quality Si-BOX interface.

Note that the magnetodiode sensitivity can be modulated by the gate voltage. The best sensitivity we measured reaches 100 μA/T for V_{Gf} = -2 V (Fig. 4.27b).

4.3.3.3 Summary

Magnetodiode characteristics of partially gated p-i-n diodes have been evaluated under a magnetic field (0 to 0.5 T). The sensing ability is confirmed in output currents, which clearly depend on the magnetic field intensity and direction. The sensing mechanism is related to the Lorentz force, generated by crossing the current and magnetic field. Carriers are moved towards one side of the device, depending on the Lorentz force regardless of their polarity. The recombination rate at the

surface defines the value of the current.

According to the experiments, the current in case II (↓; blue curves) is always higher than in the two other cases. It means that the recombination rate is reduced at the bottom interface owing to the relatively good in quality interface. In contrast, the opposite interface is more defective and recombines the carriers in the surface traps. The diode current is lowered accordingly.

4.3.4. Optical Sensors

Optical sensors are normally used for detecting either optical signals or light illumination. In a semiconductor, the conductivity is given by $\sigma = q(\mu_n n + \mu_p p)$ [34]. When incident light (ħν) shines on the surface of semiconductor [51] or in an electro-statically doped area [41], carriers are generated by photons as depicted in Figure 4.28 and contribute to an increase in conductivity. The enhancement of conductivity is caused by an increase of the number of free carriers (electrons and holes).

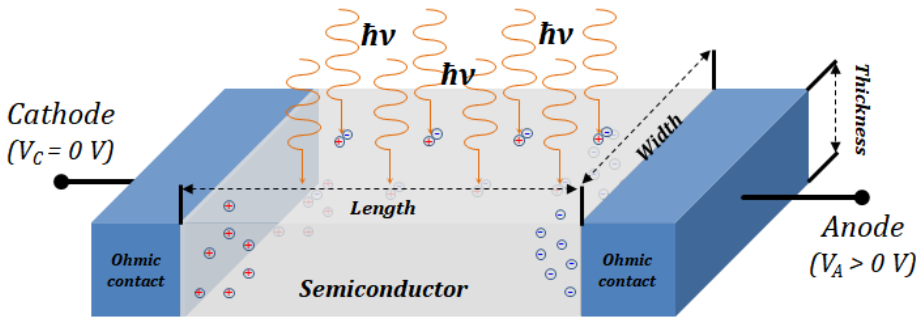

Figure 4.28: Schematic diagram of a photoconductor with applying bias in between anode and cathode [51].

For a band-modulation device such as the Z^2-FET, the number of carriers induced by light can trigger lower the junction barrier near the un-gated region and modifying the triggering voltage. The high sensitivity of this region encourages applications of Z^2-FET as a detector for optical signals.

4.3.4.1 Measurement Setup

The un-gated section of PIN structure, partially covered by gate material, is examined in order to identify the characteristic of optical sensing. Figure 4.29 shows the schematic of the Z^2-FET used

for evaluating the sensitivity under illumination as a photo-detector.

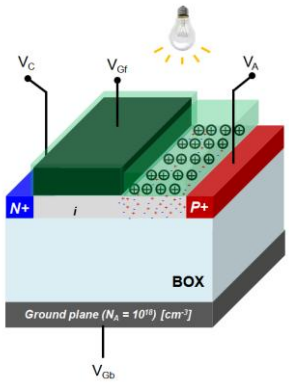

Figure 4.29: Schematic of Z^2-FET for measuring the photosensitivity under light illumination.

A semiconductor analyzer (*B1530A*) and *Elite300* probe station are used for measuring the sensing current (I_A) in DC mode. A halogen lamp built in the probe station served as light source.

4.3.4.2 DC characteristics

Figure 4.30a represents typical current-voltage characteristics extracted from several devices labeled 1st, 2nd, 3rd, 4th, 5th, and 6th in Figure 4.30. The typical sharp switching behavior [1] is shown in Figure 25a. It reflects the existence of blocking regions that prevent the injection of electrons and holes into the body. Thus, the anode current (I_A) in the dark is constrained until around 0.85 V of the anode voltage (V_A). Under the illumination from the lamp, the leakage current shows fluctuations at low V_A. When V_A exceeds 0.5 V, I_A increases exponentially as in a regular PIN diode operated in forward mode (Fig. 4.30b).

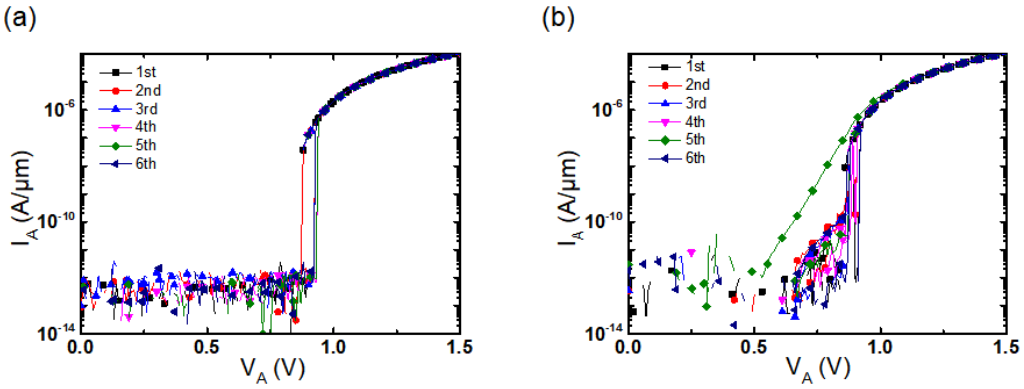

Figure 4.30: (a) I_A (V_A) characteristics without light, and (b) with light. For V_{Gf} = V_{Gb} = 0 V, L_G = 2 μm, L_i = 0.5 μm.

In particular, the green curve (#5th device) corresponds to a typical diode. The ratio between photo-current and dark-current is very high. This implies that the excess carriers induced by photons unblock the device by demolishing the injection barriers. The Z^2-FET turns into a standard PIN diode when the increase of current arises from the recombination of electrons and holes in the body region.

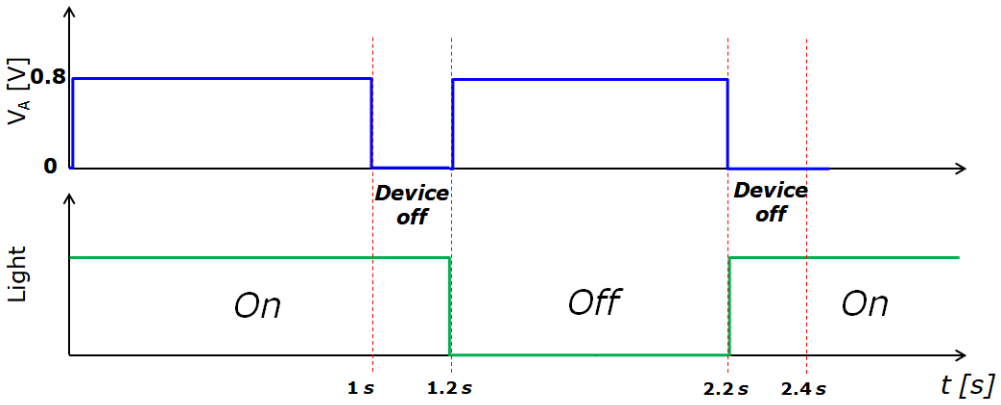

Figure 4.31: Sequences of light process and anode voltage pulses (V_A) from 0 to 0.8 V.

Current sensing is performed by applying pulsed anode voltage (V_A) as depicted in Figure 4.31. Light (a halogen lamp) is turned on or off, being controlled by the outside control panel. A *Labview* program helps to set the pulsed V_A sequence and monitor the current in the sampling mode.

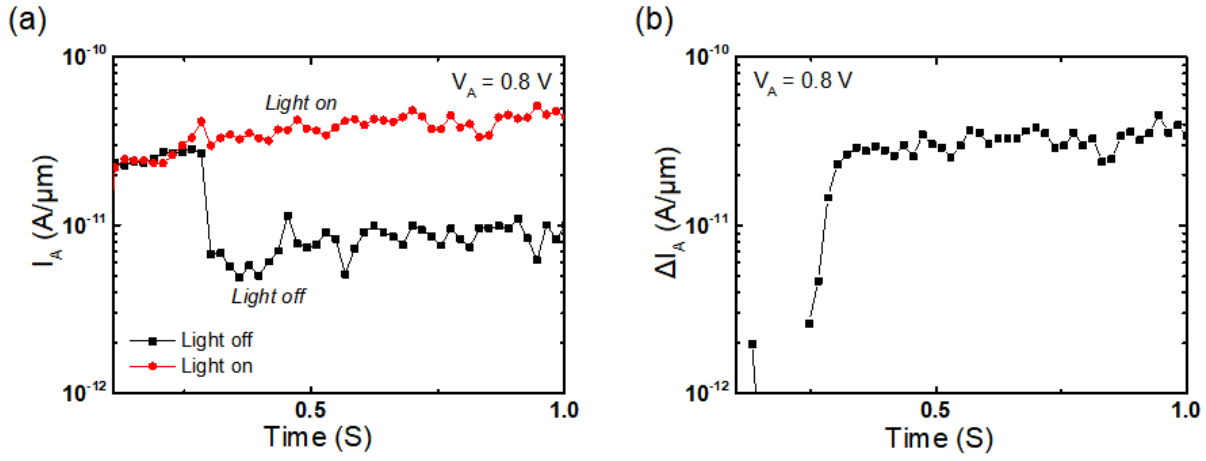

Figure 4.32: A constant voltage of V_A = 0.8 V is used during the measurement (a) Anode current variation with time in the un-gated PIN diode with and without light, (b) current difference between photo-current and dark-current.

Figure 4.32 shows the result of current characteristics measured in the sampling mode with a pulsed voltage (V_A = 0.8 V). The current level clearly depends on the presence of light. With shining light, the photo-current reaches the same amount as in the DC mode (Fig. 4.30b). In contrast, without

light, the dark-current is lower. This comparison indicates that light is able to turn on a Z^2-FET biased near the transition point. Our measurement suggests the possibility to use Z^2-FET as optical detector.

The optical sensing feature is confirmed by the increase in current under illumination. The main reason is that the carriers generated by photons cause the collapse of the reverse-biased virtual p-n junction in the middle of the body. As a result, the output current is enhanced as soon as the junction is set in a forward mode and the Z^2-FET transforms in a typical PIN diode. Our preliminary results have been consolidated recently by Wan et al [14] who demonstrate excellent performance of Z^2-FET photo detector.

4.4 Conclusion

We have characterized innovative devices in FDSOI technology. Regarding the technology of compound semiconductor on insulator, InGaAs on Insulator MOSFETs were fabricated and evaluated, and operated as the Ψ-MOSFET. This device is called a back-gated InGaAs lateral N+NN+ MOSFET. There are two current conduction mechanisms: One is bulk (or bulk) conduction where the back interface is depleted by negative bias, $V_{Gb} < 0$ V. The other is surface conduction where the back interface is accumulated with electrons by positive bias, $V_{Gb} > 0$ V. Our experiments confirm that the bulk mobility is higher than the surface mobility and exceeds 1100 cm^2/V.s in 100-200 nm thick InGaAs films. The lowest mobility is extracted from the thin (*25 nm*) layers which suffer from strong coupling between top interface defects and conduction channel.

Among many transducers based on SOI devices, we have examined the capability of Z^2-FET structure to serve as a magnetic sensor and optical. The partially gated PIN diode was characterized under specific conditions: magnetic field or illumination. In the case of magnetodiode operation where one surface became high defect density, the output currents are noticeably dependent on the magnetic field and its direction. The reason is that all carriers are moved by the magnetic field toward the same surface; therefore the net current is influenced by the rate of surface recombination.

The Z^2-FET structure also shows photosensitivity and can be used as an optical detector. The sensing performance of Z^2-FET deserves to be investigated in more detail in a dedicated project on PhD.

4.5 References

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Conclusion

General Conclusion

5. General Conclusions

The aim of this thesis was to investigate a number of innovative devices fabricated in FDSOI technology. Chapter 1 introduced the state-of-the-art of SOI technology such as SOI wafer fabrication, PD/FD SOI MOSFETs, multi-gate SOI MOSFET, and electrostatic mechanisms: inter-gate coupling, super-coupling effect, and short-channel effects.

In chapter 2, the floating body effects (FBEs) have experimentally been revisited in the context of ultrathin FDSOI MOSFETs. Our multi-angle and systematic experiments demonstrated that the FBEs are no longer spontaneous as in thicker transistors and require particular conditions such as back-gate biasing to occur.. We also proved that a silicon body thickness less than 10 nm inhibits the FBEs because of the super-coupling effect.

In chapter 3, we have accomplished body potential V_b measurements in ultrathin FDSOI MOSFETs. The potential V_b has been measured using the body contact in H-gate FDSOI MOSFETs. The measured V_b showed convincing correlations with DC and AC characteristics in terms of the onset of the FBEs. According to the experimental measurements, three major findings could be highlighted:

(i) For the first time, the body potential variation was used to clarify the FBEs such as kink effect, GIFBE, and PBT. The point is that the FBEs are originated from the interplay of the excess holes which are stored or eliminated in the thin body.

(ii) We could predict the behavior of excess holes through the variation of the V_b. As soon as the volume inversion (electrons of n-MOSFETs) was formed, the potential dropped suddenly and expelled out the accumulated holes from the body. This sharp V_b drop is caused by the super-coupling effect. The new experimental evidence of super-coupling effect, obtained by monitoring the V_b, adds to earlier measurements and simulations.

(iii) New technique for extracting threshold voltage V_T has been developed for the ultrathin MOSFETs. The V_T was extracted from the peak value of the V_b derivative in inversion region. This original definition of V_T was demonstrated to precisely meet the V_T values derived by conventional methods: g_m derivative in and y-function.

In chapter 4, we have characterized InGaAs on Insulator MOSFETs operated inΨ-MOSFET mode. In this device, called back-gated InGaAs lateral N+NN+ MOSFET, there are two current conduction mechanisms. One is volume conduction when the back interface is depleted by negative bias, $V_{Gb} < 0$ V. The other is surface conduction where the back interface is accumulated with

electrons by positive bias. Our experiments confirmed that the volume mobility is higher than the surface mobility and exceeds 1100 $cm^2/V.s$ in 100-200 nm thick InGaAs films. A lower mobility was extracted from the thin (*25 nm*) layers which suffer from strong coupling between top interface defects and conduction channel. Future technology aims at improving the interface quality and carrier mobility.

Among many transducers based on SOI devices, we have examined the capability of Z^2-FET structure to serve as a magnetic and optical sensor. In the case of magnetodiode operation, where one surface has high defect density, the output currents are noticeably dependent on the magnetic field intensity and direction. The reason is that all carriers are moved by the magnetic field toward the same surface; therefore the net current is influenced by the rate of surface recombination. The Z^2-FET structure also shows photosensitivity and can be used as an optical detector. The sensing performance of Z^2-FET is attractive and deserves to be investigated in more detail in dedicated projects.

6. Contributions and Publications

Journal publications

H. J. Park, M. Bawedin, M. S. Parihar, H.-J., Park, and S. Cristoloveanu, “Back-gated InGaAs-On-Insulator Lateral N+NN+ MOSFET: Fabrication and Typical Conduction Mechanisms” *Solid-State Electronics,* Volume 128,pp. 80-86, February (2017)

H. J. Park, M. Bawedin, H. G. Choi, and S. Cristoloveanu, “Kink effect in FDSOI MOSFETs” *Solid-State Electronics,* Volume 143, pp. 33-40, May (2018).

M.S. Parihar, K. H. Lee, **H. J. Park**, J. Lacord, S. Martinie, J.-Ch. Barbe, Y. Xu, H. El Dirani, Y. Taur, S. Cristoloveanu and M. Bawedin, “Insight into carrier lifetime impact on band-modulation devices, *Solid-State Electronics*, Volume 143, pp. 41-48, May (2018).

S. Cristoloveanu, K. H. Lee, **H. Park**, and M. S. Parihar, “The concept of electrostatic doping and related devices,” *Solid-State Electronics 155,* pp. 32–43 (2019).

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Hyungjin Park, Maryline Bawedin, Kyunghwa Lee, Jean-Pierre Colinge, Sorin Cristoloveanu, "Is FD-SOI immune to Floating Body Effects?" 2018 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S) (2018)

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K. H. Lee, M. Bawedin, M. S. Parihar, **H.-J., Park**, and S. Cristoloveanu, "Carrier lifetime evaluation in FD-SOI layers," Solid State Device Research Conference (ESSDERC), (2017).

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L. Pirro, **H. J. Park**, I. Ionica, M. Bawedin, L. Czornomaz, V. Djara, V. Deshpande, S. Cristoloveanu, "Volume and Interface Conduction in InGaAs Junctionless Transistors" *Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (ULIS), (2016).*

7. Résumé de la Thèse

Chapitre 1 - Introduction

Le premier chapitre présente une introduction générale à la technologie SOI (Silicium sur Isolant). Nous abordons brièvement les problèmes de miniaturisation des transistors complémentaires métal–oxyde–semiconducteur (CMOS). Récemment, la stratégie de réduction d'échelle des composants a été mise à l'épreuve car les effets de canal court ont obligé les fabricants de semi-conducteurs à abandonner le MOSFET planaire traditionnel pour de nouveaux types de dispositifs tels que les FinFETs ou SOI totalement déserté (FD-SOI). La technologie SOI de pointe est présentée comme une option réaliste permettant de surmonter la complexité de fabrication du secteur CMOS et d'élargir les limites de dimensionnement. En particulier, le procédé innovant de fabrication de plaquettes appelé Smart-Cut™ a été commercialisé pour les produits CMOS haut de gamme et fiables. Les caractéristiques fondamentales des transistors FD-SOI sont également présentées.

La technologie CMOS sur silicium massif a été florissante grâce à la stratégie de réduction de la taille des dispositifs. Cependant, la période de "réduction d'échelle heureuse" est maintenant terminée en raison du faible contrôle électrostatique du canal par la grille dans les dispositifs ultra-courts et de la complexité de la fabrication du dispositif. Avec son contrôle supérieur des effets à canal court, la technologie FD-SOI représente une option attrayante et réaliste pour remplacer le silicium massif. Plusieurs types de dispositifs et de plaquettes SOI permettent notamment la mise en œuvre de produits commerciaux performants : dispositifs RF IoT et basse tension, composants aérospatiaux, processeurs rapides. L'amincissement du corps du transistor est crucial pour traiter les effets de canaux courts. Dans ces transistors ultra-minces, l'accent est mis sur les mécanismes de couplage et de super-couplage, ouvrant ainsi de nouvelles options pour la conception de circuits.

Chapitre 2 - Effets de substrat flottant dans les transistors MOSFET FDSOI ultra-fins

Les FBE (floating-body effects) ont été notoires dans les dispositifs SOI partiellement déplétés (PD). L'un des effets les plus connus est l'effet kink, qui a été compris très tôt dans les MOSFET en silicium sur saphir (SOS). Les porteurs majoritaires générés par l'ionisation par impact s'accumulent dans la région neutre du dispositif, augmentant ainsi son potentiel et abaissant la tension de seuil, ce qui

augmente soudainement le courant de drain. Depuis lors, au cours de l'évolution de la technologie SOI, le nombre de mécanismes FBE s'est élargi. Ils proviennent non seulement de l'ionisation par impact, mais également de l'effet tunnel bande-à-bande (BTBT), du passage tunnel direct à travers le très mince diélectrique de grille, de l'application de polarisations transitoires et de l'éclairage ou des rayonnements ionisants. Bien que les FBE puissent fournir un courant supplémentaire et augmenter la vitesse du circuit, ils sont généralement considérés comme des mécanismes parasites responsables des effets de non-linéarité, d'hystérésis, de verrouillage, et de courants transitoires.

Il est communément admis que les FBE n'existent plus dans les MOSFET SOI totalement déplétés (FD). Les FBE peuvent être déclenchés par des trous en excès (ou déficients) dans le corps du transistor, mais dans le FD-SOI, il n'y a pas de région neutre où les trous peuvent s'accumuler. Pour cette raison, les FBE ne sont pas pris en compte dans les modèles compacts dédiés au FD-SOI. Cependant, il existe de nombreux rapports expérimentaux révélant l'activation possible des FBE résiduels dans des transistors FD-SOI relativement épais. L'argument de base est que le corps du transistor - toujours isolé par le BOX, l'oxyde de grille et les jonctions - n'est pas totalement exempt de variations de la charge des porteurs majoritaires. Le corps isolé peut être susceptible d'entraîner des conditions hors d'équilibre.

Nous examinons pour la première fois leur viabilité dans des MOSFET FD-SOI très avancés, à corps ultra-mince de l'ordre de 10 nm. Les résultats ont une importance pratique pour les concepteurs de circuits basés sur SOI. Nous démontrons systématiquement plusieurs situations où l'absence ou la présence des FBE peut être corrélée à l'épaisseur du film. Au travers des différentes expériences, nous avons démontré que les FBE n'étaient plus spontanés mais sous conditions particulières telles que la polarisation de la grille arrière. Nous avons constaté que l'épaisseur du film de Si, la polarisation arrière et la vitesse de balayage sont des paramètres essentiels. Nous décrivons également la compétition entre les FBE et l'effet de super-couplage dans des films d'une épaisseur inférieure à 10 nm. Nous avons prouvé qu'une épaisseur de silicium inférieure à 10 nm évitait les FBE.

Pour la première fois, la variation du potentiel dans le corps du transistor a été mesurée et utilisée pour corréler l'apparition des FBE, en particulier les effets kink, GIFBE et MSD métastable. Le point clé est que tous les FBE proviennent de l'interaction des trous en excès qui sont stockés ou éliminés dans le corps flottant. Nous avons mesuré directement la variation du potentiel liée aux trous en excès. Ces résultats permettent d'obtenir des informations détaillées sur les MOSFET FD-SOI et ses applications CMOS.

Chapitre 3 - Variation dynamique du potentiel dans MOSFET FDSOI ultraminces

Les MOSFET FD-SOI et à grilles multiples sont les meilleurs candidats pour pousser la mise à l'échelle du transistor au-delà du nœud 5 nm. Nous avons vu que les MOSFET FD-SOI ne sont pas exempts d'effets à corps flottants. En mode dynamique, le potentiel de corps peut échapper temporairement au contrôle de la grille, ce qui entraîne plusieurs FBE dynamiques conduisant à une augmentation/réduction temporaire du courant. Ces FBE dynamiques permettent des applications pragmatiques: développement de mémoire 1T-DRAM sans condensateur, programmation de mémoires EEPROM et effets d'histoire dans des circuits intégrés.

Dans les MOSFET FD-SOI ultra-minces, la variation dynamique du potentiel nous donne des informations pratiques sur les porteurs majoritaires présents dans le corps. Nous avons poursuivi les travaux de Bawedin *et al* sur la variation dynamique du potentiel au moyen de mesures systématiques et de simulations numériques. Les FBE transitoires ont lieu pendant des modes particuliers du fonctionnement des MOSFET SOI. Pour les applications de circuits numériques ou analogiques, la plage de polarisation de la grille avant s'étend approximativement entre la tension de bande plate et un peu au-dessus de la tension de seuil. Cela signifie que l'état de l'interface film-oxyde varie de l'accumulation, à la déplétion et la forte inversion. Les FBE dynamiques peuvent toutefois apparaître dans une plage de polarisation inférieure à la tension de bandes plates. Pour la mémoire DRAM sans condensateur, les FBE dynamiques sont essentiellement pertinents en termes de couplage capacitif en déplétion profonde ($V_G << V_{FB}$) et de charge engendrée par un courant de tunnel bande-à-bande (*B2B*). Dans ce cas particulier, le courant de grille correspond au courant de déplacement induit par la différence de tension entre la polarisation de la grille et le potentiel du corps.

Des caractéristiques spécifiques de transfert (courant de drain *vs.* tension de grille) résultent de la variation du potentiel du corps et dépendent donc des directions de balayage de la tension de grille avant V_{Gf} (directe ou inverse). Le courant transitoire de grille I_{Gf} et l'hystérésis du courant de drain se manifestent lorsque le potentiel des interfaces avant ou arrière varie entre inversion et accumulation.

Notons que le couplage dynamique inter-grilles et l'absence temporaire de porteurs majoritaires sont responsables du comportement particulier du potentiel qui produit des caractéristiques de courant inhabituelles. Le principe de la mémoire 1T-DRAM (nommée MSDRAM) provient de l'effet MSD.

Nous avons étudié les variations du potentiel du corps V_b dans les FDSOI n-MOSFET ultra-minces (8 nm < t_{Si} < 25 nm) à l'aide d'un contact P^+. Le potentiel mesuré montre de bonnes corrélations avec l'apparition des FBE. Selon les mesures expérimentales, trois résultats principaux peuvent être mis en évidence:

(i) Pour la première fois, la variation du potentiel a été utilisée pour corréler les FBE tels que l'effet kink, le GIFBE et le bipolaire parasite. Le fait est que les FBE proviennent de l'interaction des trous en excès qui sont stockés ou éliminés dans le corps mince.

(ii) Nous pouvons prédire le comportement des trous en excès par la variation de V_b. Dès que

l'inversion de volume (électrons dans n-MOSFET) vient d'être formée, V_b tombe soudainement et les trous accumulés sont expulsés du corps. Ceci est causé par l'effet de super-couplage, dont nous apportons une nouvelle preuve expérimentale.

(iii) Une nouvelle technique d'extraction de la tension de seuil V_T a été mise au point pour les MOSFET ultra-minces. V_T a été extraite de la valeur du maximum de la dérivée de V_b dans le régime d'inversion. Le pic de la dérivée V_b correspond avec précision à la V_T obtenue par le procédé classique, c'est-à-dire la technique d'extraction par la dérivée de la transconductance.

Ce qui ressort le plus de cette étude est l'établissement d'une mesure fiable de V_b pour une compréhension précise des changements liés à la variation des trous en excès dans le corps ultra-mince.

Chapitre 3 – Etude de transistors et applications SOI avancés

La technologie silicium (ou semiconducteur) sur isolant fournit des fonctionnalités remarquables aux dispositifs avancés. Les dispositifs SOI présentent des caractéristiques uniques telles qu'une pente sous le seuil minimale, un couplage entre grilles permettant l'ajustement de la tension de seuil et la compatibilité avec de nouveaux matériaux semiconducteurs. Cela rend possible la conception de dispositifs SOI innovants.

Nous avons exploré des dispositifs émergents tels qu'un MOSFET InGaAs sur isolant, une magnétodiode Z^2-FET et un détecteur optique.

Des MOSFET InGaAs sur isolant ont été fabriqués dans le cadre d'une coopération avec IBM. Les dispositifs de test sont des transistors N^+NN^+ commandés par une grille arrière. Nous avons mis en évidence deux mécanismes de conduction de courant: l'un est la conduction en volume qui subsiste lorsque l'interface arrière est déplétée par une tension de grille négative ; l'autre est la conduction de surface où l'interface arrière accumule des électrons pour une tension positive. Nous avons mis au point une méthode originale qui permet de déterminer les paramètres de chaque régime de conduction. Nos expériences confirment que la mobilité volumique est supérieure à la mobilité de surface et dépasse 1100 cm^2/Vs dans des films InGaAs de 100-200 nm d'épaisseur. Les couches minces (25 nm) souffrent d'un fort couplage entre les défauts de l'interface supérieure et le canal de conduction qui conduit à des mobilités dégradées.

Parmi de nombreux transducteurs basés sur des dispositifs SOI, nous avons examiné la capacité de la structure Z^2-FET à servir comme capteur magnétique et optique. Il s'agit d'une diode PIN partiellement recouverte d'une grille qui montre des caractéristiques de commutation très abruptes. Nous l'avons caractérisée dans des conditions spécifiques: champ magnétique ou éclairage. Sous éclairage, la tension de déclenchement est modifiée produisant à un courant supérieur (par 6-8 ordres

de grandeur) à celui mesuré en obscurité.

Dans le cas du fonctionnement de la magnétodiode, la différence entre les deux interfaces en termes de densité de défauts, conduit à des courants de sortie qui dépendent sensiblement du champ magnétique et de sa direction. La raison en est que les électrons et les trous sont déplacés par le champ magnétique vers la même surface; par conséquent, le courant net est influencé par le taux de recombinaison de surface.