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Non-Foster Circuits Applied to Full-duplex Systems

Saadou Al Mokdad

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Par

Saadou Almokdad

« Non-Foster Circuits Applied to Full-duplex Systems »

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Summary

ACKNOWLEDGMENTS.....	I
SUMMARY.....	II
TABLE OF FIGURES	V
LIST OF TABLES	XII
GENERAL INTRODUCTION	1
CHAPTER 1	3
1. INTRODUCTION	3
1.2 DUPLEXING TECHNIQUE IN MODERN WIRELESS LINKS.....	4
1.2.1 TIME DIVISION DUPLEX (TDD).....	4
1.2.2 FREQUENCY DIVISION DUPLEX (FDD).....	4
1.2.3 OTHER DUPLEXING/MULTIPLEXING TRANSMISSION TECHNIQUES	5
1.3 ADVANTAGES AND DISADVANTAGES OF FULL-DUPLEX TECHNIQUE.....	6
1.4 SOURCES OF SELF-INTERFERENCE.....	7
1.5 FD REQUIREMENTS.....	8
1.5.1 PASSIVE SELF-INTERFERENCE SUPPRESSION	11
1.5.2 ANALOG SELF-INTERFERENCE CANCELLATION	11
1.5.3 DIGITAL SELF-INTERFERENCE CANCELLATION	12
1.6 DISTORTION AND NOISE ISSUES IN FD.....	13
1.7 PROPOSED TOPOLOGIES FOR SI CANCELLATION.....	15
1.8 ANTENNA SPECIFICATIONS FOR A COMPACT FD SYSTEM.....	18
1.9 MOTIVATION, OBJECTIVES AND PROPOSED TOPOLOGY	19
1.10 ORGANIZATION OF THE THESIS	20
1.12 REFERENCE	21
CHAPTER 2	23
2.1 INTRODUCTION TO FOSTER AND NON-FOSTER ELEMENTS	23
2.3 NIC AND NII BASICS.....	24
2.4 TOPOLOGIES OF NIC	26
2.5 OTHER NON-FOSTER TOPOLOGIES.....	27
2.5.1 NIC BASED ON AMPLIFIERS	27
2.5.2 NIC BASED ON A TRANSFORMER.....	28
2.5.3 NON-FOSTER CIRCUITS BASED ON A NEGATIVE GROUP DELAY NGD	28
2.5.4 NON-FOSTERS BASED ON DISTRIBUTED AMPLIFIER.....	29
2.7 NICS CHOSEN CIRCUIT	30
2.7.1 CASE R_0 INFINITE:	31
2.7.2 CASE R_0 IS FINITE	32
2.8 STABILITY WITHIN NICS.....	33

2.9 LINVILL ANALYSIS LIMITATION.....	35
2.10 CONCLUSION.....	36
2.11 REFERENCES.....	37
CHAPTER 3	39
3.1 PHASE SHIFTER.....	39
3.2 TYPES OF PHASE SHIFTERS	40
3.2.1 ACTIVE AND PASSIVE PS	40
3.2.2 MECHANICAL OR ELECTRONIC PHASE SHIFTERS.....	41
3.2.4 FIXED OR ADJUSTABLE PHASE SHIFTERS	41
3.2.3 DIGITAL OR ANALOG TUNABLE PHASE SHIFTERS	42
3.2.5 RECIPROCAL OR NONRECIPROCAL PHASE SHIFTERS.....	43
3.2.6 PURE PHASE SHIFTERS	43
3.3 1ST DESIGN OF PS TUNABLE AROUND 180° USING NF CIRCUIT.....	44
3.3.1 PROPOSED TOPOLOGY.....	45
3.3.2 NF CAPACITANCE DESIGN AND MINIMIZATION OF RESIDUAL RESISTIVE PART .	45
3.3.3 IMPROVED REDUCTION OF RESISTIVE PART OF NF CAPACITANCE AT THE	
S-PARAMETERS LEVEL	48
3.3.4 ACTIVE TUNABLE PURE PHASE SHIFTER SIMULATION RESULTS	50
3.4 STABILITY STUDY.....	51
3.4.1 STABILITY STUDY BASED ON NDF	51
3.4.2 STABILITY STUDY: INFLUENCE OF DC BIAS.....	54
3.4.3 STABILITY STUDY: INFLUENCE OF TRANSMISSION LINE	56
3.5 DESIGN OF NON-FOSTER COMPONENTS USING TRANSISTOR WITH LOW	
TRANSITION FREQUENCY	58
3.5.1 MEASURED RESULTS	60
3.5.1.1 Prototype 1.....	60
3.5.1.2 Prototype 2.....	61
3.5.1.3 Prototype 3.....	64
3.5.2 2ND DESIGN OF TUNABLE PS	68
3.6 CONCLUSION.....	71
3.7 PERSPECTIVES ON PS	72
3.8 REFERENCES.....	73
CHAPTER 4	75
4.1 INTRODUCTION.....	75
4.1.1 DEFINITION OF AN ESA	75
4.1.2 TYPICAL APPLICATIONS OF ESAS	76
4.1.3 CHARACTERISTIC IMPEDANCE OF ESA	76
4.1.4 FUNDAMENTAL PARAMETERS OF ESA.....	78

4.1.4.1 Quality factor Q	78
4.1.4.2 Bandwidth.....	79
4.1.4.3 Gain-Bandwidth Limitation of Lossless Passive Matching Networks	80
4.2 ACTIVE CIRCUITS APPLIED TO IMPEDANCE MATCHING	82
4.3 METHODOLOGY OF COMBINED NON-FOSTER AND PASSIVE BROADBAND MATCHING NETWORKS.....	83
4.3.1 CONVENTIONAL MONOPOLE ANTENNA	83
4.3.2 FIRST MATCHING TOPOLOGY: NF-PASSIVE-ANTENNA.....	85
4.3.3 SECOND MATCHING TOPOLOGY: PASSIVE-NF-ANTENNA.....	89
4.3.4 PROPOSED MATCHING TOPOLOGY: PASSIVE-NF-PASSIVE-ANTENNA	91
4.3.5 TOPOLOGIES COMPARISON AND DISCUSSION.....	93
4.4 DESIGN OF A FULL-DUPLEX FRONT-END DEDICATED TO CLOSE AND ELECTRICALLY SMALL ANTENNAS (ESA) BY USING NF CIRCUITS	96
4.4.1 FULL DUPLEX APPROACH USING PASSIVE ELEMENTS	96
4.4.1.1 Analysis of topologies.....	98
4.4.1.2 Simulations and Measured Results	99
4.4.2 FULL DUPLEX TOPOLOGY USING NON-FOSTER ELEMENTS	102
4.4.2.1 Non-Foster matching of one monopole antenna.....	102
4.4.2.2 Non-Foster Matching and decoupling.....	108
4.4.2.3 Combining Two Levels of Self-Interference Cancellation	111
4.5 CONCLUSION.....	113
4.6 REFERENCES	115
CHAPTER 5	117
APPENDICES	129
APPENDIX A.....	119
APPENDIX B.....	121
APPENDIX C.....	124
APPENDIX D.....	129
COMMUNICATIONS AND PUBLICATIONS	132

Table of Figures

FIGURE 1.1 TRANSMISSION MODES.....	4
FIGURE 1.2 COMPARISON BETWEEN TDD, FDD, AND FD IN TERM OF UPLOADING AND DOWNLOADING DATA IN FREQUENCY AND TIME DOMAIN	5
FIGURE 1.3 VARIOUS LEVELS IN THE TX AND THE RX CHAIN TO GET SI CANCELLATION.....	8
FIGURE 1.4 ILLUSTRATION OF REQUIRED LEVELS AND DISTRIBUTION OF SI CANCELLATION	9
FIGURE 1.5 DIFFERENT SECTIONS OF SIC	10
FIGURE 1.6 BLOCK DIAGRAM OF ANALOG RF SELF-INTERFERENCE CANCELLATION.....	12
FIGURE 1.7 BLOCK DIAGRAM OF DIGITAL BASEBAND SELF-INTERFERENCE CANCELLATION.....	13
FIGURE 1.8 WHAT THE RADIO IS EXPECTED TO TRANSMIT (A), WHAT IS ACTUALLY TRANSMITTED (B).....	15
FIGURE 1.9 ANTENNA SEPARATION	16
FIGURE 1.10 ANTENNA PLACEMENT.....	16
FIGURE 1.11 MIDU TOPOLOGY	17
FIGURE 1.12 ELECTRIC BALANCE TOPOLOGY.....	17
FIGURE 1.13 TOPOLOGY TO REDUCE SI IN A COMPACT FD FRONT-END	20
FIGURE 2.1 REACTANCE OR SUSCEPTANCE OF FOSTER ELEMENT ALONG FREQUENCY AXIS	23
FIGURE 2.2 REFLECTION COEFFICIENT OF FOSTER AND NF ELEMENTS ON SMITH CHART.....	24
FIGURE 2.3 SCHEME OF NIC (A), AND NII (B) TWO-PORT NETWORKS	25
FIGURE 2.4 BASIC NIC TOPOLOGY SHOWING VOLTAGE FLOW (RED ARROWS) AND CURRENT FLOW (BLUE ARROWS).....	25
FIGURE 2.5 AMPLIFIER BASED NIC	28
FIGURE 2.6 TRANSFORMER BASED NIC.....	28
FIGURE 2.7 (A) SERIES AND PARALLEL RLC RESONATORS USED FOR OPTIONING NGD. (B) COMBINATION OF SERIES AND PARALLEL RLC RESONATORS FOR WIDEBAND NGD RESPONSE	29

FIGURE 2.8 SCHEMATIC OF TUNABLE NEGATIVE CAPACITOR USING NGD CIRCUIT BASED ON DISTRIBUTED AMPLIFIER.....	29
FIGURE 2.9 SMALL SIGNAL π -MODEL REPRESENTATION OF BJT TRANSISTOR	30
FIGURE 2.10 NIC OPEN CIRCUIT STABLE (OCS) TOPOLOGY.....	31
FIGURE 2.11 NIC OPEN CIRCUIT STABLE (OCS) TOPOLOGY WHERE R_0 IS FINITE	32
FIGURE 2.12 GENERAL TOPOLOGY OF NIC WITH STABILITY CONDITIONS	34
FIGURE 2.13 IDEAL NIC DIAGRAM PRESENTING REFERENCE PLAN FOR (A) OPEN-CIRCUIT AND (B) SHORT-CIRCUIT STABILITY CONDITION	34
FIGURE 3.1 TWO-PORT NETWORK SCHEMATIC OF A PHASE SHIFTER	40
FIGURE 3.2 EXAMPLE ON MECHANICAL PHASE SHIFTERS [15] (A), AND ELECTRICAL PHASE SHIFTERS [16] (B).....	41
FIGURE 3.3 BUTLER MATRIX (A), PHASE INVERTER (B)	42
FIGURE 3.4 DIGITAL PHASE SHIFTER (A), ANALOG PHASE SHIFTER (B)	42
FIGURE 3.5 STRUCTURE OF PURE PHASE SHIFTER: TRANSMISSION LINE (TL) CASCADED WITH THE NON-FOSTER (NF) ELEMENT (A), IDEAL BEHAVIOR OF THEIR PURE PHASE RESPONSE (B)..	43
FIGURE 3.6 PROPOSED PHASE SHIFTER TOPOLOGY	44
FIGURE 3.7 EVEN-MODE EQUIVALENT CIRCUIT (A), ODD-MODE EQUIVALENT CIRCUIT (B).....	45
FIGURE 3.8 EQUIVALENT XCP CIRCUIT MODEL WITH OUTPUT AT SOURCE (A), AND WITH OUTPUT AT DRAIN (B)	46
FIGURE 3.9 CASCADING SOURCE AND DRAIN TOPOLOGY TO GET -1pF	48
FIGURE 3.10 XCP INPUT IMPEDANCE (IMAGINARY AND REAL PARTS) FOR OUTPUT AT SOURCE AND DRAIN COMPARED TO A NEGATIVE CAPACITANCE OF -2pF	48
FIGURE 3.11 REAL PART OF THE CASCADED NF TOPOLOGY AND THE MODIFIED ONE (A), IMAGE OF MODIFIED CASCADE TOPOLOGY COMPARED TO -1pF (B).....	49
FIGURE 3.12 MODIFIED SOURCE XCP TOPOLOGY	49
FIGURE 3.13 SCHEMATIC OF THE MODIFIED CASCADED NF TOPOLOGY	50

FIGURE 3.14 THE COMPLETE CIRCUIT STRUCTURE OF THE ACTIVE PHASE SHIFTER	50
FIGURE 3.15 PS REFLECTION AND TRANSMISSION COEFFICIENTS (A), PHASE VARIATION USING A VARACTOR (B)	51
FIGURE 3.16 PHASE SHIFTER TOPOLOGY WITH SUSPECTED NODES	52
FIGURE 3.17 NDF OF THE PHASE SHIFTER	52
FIGURE 3.18 NUMBER OF ENCIRCLEMENT OF NDF AROUND THE ORIGIN	53
FIGURE 3.19 DRAIN TOPOLOGY IMPEDANCE AND ITS LOAD IMPEDANCE	53
FIGURE 3.20 DRAIN TOPOLOGY IMPEDANCE COMPARED TO LOAD IMPEDANCE	54
FIGURE 3.21 BIAS NETWORK FOR SOURCE TOPOLOGY	55
FIGURE 3.22 NUMBER OF ZEROS OF NDF ACCORDING TO VALUE OF C_L	55
FIGURE 3.23 SOURCE TOPOLOGY WITH INDUCTORS L TO MIMIC INTERCONNECT LINES	56
FIGURE 3.24 OSCILLATION FREQUENCY AS A FUNCTION OF INDUCTANCE VALUE.....	57
FIGURE 3.25 TRANSISTORS GAIN VS FREQUENCY COMPARISON	59
FIGURE 3.26 DE-EMBEDDING IN ADS	59
FIGURE 3.27 NIC STRUCTURE WITH AVAGO VMMK-1218 FET STRUCTURE (A), BUILT VIEW (B).....	60
FIGURE 3.28 SPECTRUM OF OSCILLATING NIC WITH AVAGO VMMK-1218 PHEMT.....	60
FIGURE 3.29 NIC STRUCTURE: (A) TOP VIEW, (B) PERSPECTIVE VIEW, (C) BUILT VIEW	61
FIGURE 3.30 COMPARISON BETWEEN MEASURED AND SIMULATED RESULT OF LOADED NIC ..	62
FIGURE 3.31 MEASURED RETURN LOSS ON SMITH CHART OF LOADED NIC LAYOUT.....	62
FIGURE 3.32 DE-EMBEDDED MEASURED RETURN LOSS ON SMITH CHART OF NIC.....	63
FIGURE 3.33 DE-EMBEDDED REACTANCE OF THE NIC.....	63
FIGURE 3.34 THE CAPACITANCE AND INDUCTANCE OF THE DE-EMBEDDED NIC	64
FIGURE 3.35 NIC STRUCTURE: (A) TOP VIEW, (B) PERSPECTIVE VIEW, (C) PHOTO.....	65
FIGURE 3.36 COMPARISON BETWEEN MEASURED AND SIMULATED RESULT OF BFR93A NIC .	66
FIGURE 3.37 DE-EMBEDDED MEASURED RETURN LOSS ON SMITH CHART OF BFR93A NIC ...	66

FIGURE 3.38 DE-EMBEDDED REACTANCE OF THE BFR93A NIC.....	67
FIGURE 3.39 THE CAPACITANCE AND INDUCTANCE OF THE DE-EMBEDDED BFR93A NIC	67
FIGURE 3.40 THE CAPACITANCE AND INDUCTANCE OF THE DE-EMBEDDED NIC	68
FIGURE 3.41 2 ND PS REFLECTION AND TRANSMISSION COEFFICIENTS (A), AND PHASE TRANSMISSION (B).....	68
FIGURE 3.42 NDF OF THE 2 ND PHASE SHIFTER	69
FIGURE 3.43 NUMBER OF ENCIRCLEMENT OF NDF AROUND THE ORIGIN FOR THE 2 ND PS	69
FIGURE 3.44 2 ND PS STRUCTURE: (A) TOP VIEW, (B) PERSPECTIVE VIEW, (C) BUILT VIEW.....	70
FIGURE 3.45 COMPARISON BETWEEN MEASURED AND SIMULATED RESULTS FOR 2 ND PS.....	71
FIGURE 3.46 COMPARISON BETWEEN MEASURED AND SIMULATED RESULTS FOR THE TRANSMISSION PHASE OF THE 2 ND PS.....	71
FIGURE 4.1 A DIPOLE ANTENNA CIRCUMSCRIBED BY A SPHERE WITH RADIUS A	76
FIGURE 4.2 SOME EXAMPLE OF ESA USED IN EVERYDAY LIFE SYSTEM SUCH AS (A) GARAGE KEYLESS DOOR OPENER [3], (B) VEHICULAR MULTIFUNCTION ANTENNA [4], (C) A RFID TAG ANTENNA [5]	76
FIGURE 4.3 SMALL ELECTRIC DIPOLE (A), IMPEDANCE Z _A AS FUNCTION OF SIZE FACTOR KA (B) [7]	77
FIGURE 4.4 SINGLE TURN SMALL LOOP ANTENNA (A), RESISTIVE AND REACTIVE RESPONSE OF SMALL LOOP WITH A/D = 100.....	78
FIGURE 4.5 COMPARISON BETWEEN 1 STAGE L-NETWORK AND 2 STAGE L-NETWORK ON Q FACTOR (A), THE EFFECT OF Q FACTOR ON BANDWIDTH (B)	80
FIGURE 4.6 PORT LOSSLESS MATCHING NETWORK FOR A SERIES PASSIVE RC	81
FIGURE 4.7 A POSSIBLE REFLECTION COEFFICIENT RESPONSE WITH A 2-PORT MATCHING NETWORK FOR A SERIES PASSIVE RC [15]	81
FIGURE 4.8 COMPARISON BETWEEN (A) PASSIVE AND (B) ACTIVE MATCHING FOR AN ESA, REPRESENTED AS A SERIES CAPACITOR	82

FIGURE 4.9 ANTENNA SCHEMATIC AND RETURN LOSS.....	84
FIGURE 4.10 ANTENNA IMPEDANCE (REAL AND IMAGINARY) PARTS.....	84
FIGURE 4.11 MAXIMUM ACHIEVABLE ANTENNA RADIATION EFFICIENCY.....	85
FIGURE 4.12 ANTENNA MATCHING ON SMITH CHART.....	86
FIGURE 4.13 RESISTANCE CIRCLES ON SMITH CHART.....	86
FIGURE 4.14 ANTENNA WITH PASSIVE TRANSFORMER (A), ANTENNA WITH NF-PASSIVE MATCHING (B).....	87
FIGURE 4.15 ANTENNA MATCHING STEPS ON SMITH CHART.....	87
FIGURE 4.16 (A) ONE STAGE L PASSIVE MATCHING (B) TWO STAGES L MATCHING (C) THREE STAGES L MATCHING.....	88
FIGURE 4.17 MULTI-STAGE L-NETWORKS VS NF AND PASSIVE MATCHING.....	88
FIGURE 4.18 ANTENNA MODEL AT LOW FREQUENCY (A), NF REACTIVE PART COMPENSATION (B), COMPLETE MATCHING (C).....	89
FIGURE 4.19 STEP BY STEP MATCHING ON SMITH CHART.....	90
FIGURE 4.20 PASSIVE-NF MATCHING.....	90
FIGURE 4.21 ILLUSTRATION OF THE STEP-BY-STEP MATCHING USING THE 3RD TOPOLOGY (A) PASSIVE MATCHING, (B) NON-FOSTER MATCHING, (C) PASSIVE TRANSFORMER.....	91
FIGURE 4.22 STEP-BY-STEP WIDEBAND MATCHING FOR THE 3RD TOPOLOGY.....	92
FIGURE 4.23 COMPARISON BETWEEN THE THREE TOPOLOGIES.....	92
FIGURE 4.24 COMPARISON BETWEEN QUALITY FACTORS OF THE THREE TOPOLOGIES.....	92
FIGURE 4.25 INCIDENT AND REFLECTED WAVES AT THE MATCHING CIRCUIT ACCESSSES.....	94
FIGURE 4.26 COMPARISON OF TTC FOR THE THREE TOPOLOGIES.....	94
FIGURE 4.27 EFFICIENCY OF THE SYSTEM.....	95
FIGURE 4.28 PROPOSED FULL-DUPLEX SYSTEM.....	96
FIGURE 4.29 RETURN AND INSERTION LOSS BETWEEN TWO CLOSELY SEPARATED ANTENNAS...	97

FIGURE 4.30 SCHEMATIC OF TWO CLOSELY SPACED MONOPOLES AS PROPOSED IN [22] (A), MODIFIED TOPOLOGY (B).....	97
FIGURE 4.31 TWO-PORT NETWORK REPRESENTATION OF REFERENCE TOPOLOGY (A), AND MODIFIED ONE (B).....	99
FIGURE 4.32 EVEN ODD MODE REPRESENTATION OF REFERENCE TOPOLOGY (A), AND MODIFIED ONE (B).....	99
FIGURE 4.33 MANUFACTURED STRUCTURE OF REFERENCE TOPOLOGY (A), AND MODIFIED ONE (B).....	100
FIGURE 4.34 MANUFACTURED STRUCTURE OF REFERENCE TOPOLOGY AT 2.3 GHZ (A), AND MODIFIED ONE AT 2.3 GHZ (B), REFERENCE TOPOLOGY AT 1.6 GHZ (C), AND MODIFIED ONE AT 1.6 GHZ (D).....	101
FIGURE 4.35 SIMULATED EFFICIENCY OF THE FIVE CONFIGURATIONS.....	101
FIGURE 4.36 REALIZED GAIN COMPARISON BETWEEN TWO MONOPOLE, REFERENCE TOPOLOGY, AND MODIFIED ONE AT 1.6 GHZ (A), AND 2.3 GHZ (B).....	102
FIGURE 4.37 SCHEMATIC OF NON-FOSTER CIRCUIT WITH ANTENNA SHOWING THE CURRENT PATH (A), THE CORRESPONDING LAYOUT (B), AND THE PHOTO OF THE FABRICATED ONE (C)	103
FIGURE 4.38 SURFACE CURRENT DISTRIBUTION AT 1.6GHZ (A) GEOMETRY OF NON-FOSTER CIRCUIT AND ANTENNA WITH ALL THE ASSOCIATED ELEMENTS (B).....	104
FIGURE 4.39 COMPARISON BETWEEN SIMULATED AND MEASURED RETURN LOSS OF A MONOPOLE ANTENNA MATCHED BY NF CIRCUIT.....	105
FIGURE 4.40 COMPARISON BETWEEN ANTENNA WITH/WITHOUT NF MATCHING FOR IMAGINARY PART (A), AND REAL PART (B)	105
FIGURE 4.41 EFFICIENCY COMPARISON OF ANTENNA WITH/WITHOUT NF MATCHING	105
FIGURE 4.42 COMBINED PASSIVE AND NF MATCHING FIRST TOPOLOGY (A), SECOND TOPOLOGY (B), FABRICATED FIRST TOPOLOGY (C), AND FABRICATED SECOND TOPOLOGY (D)	106

FIGURE 4.43 SCHEMATIC OF COMBINED PASSIVE AND NF MATCHING, TOPOLOGY 1 (A), AND TOPOLOGY 2 (B)	107
FIGURE 4.44 COMPARISON BETWEEN NF MATCHING AND COMBINED PASSIVE AND NF MATCHING.....	108
FIGURE 4.45 SIMULATED VS MEASURED RESULT OF PASSIVE NF MATCHING OF TOPOLOGY ONE (A), AND TOPOLOGY TWO (B).....	108
FIGURE 4.46 TWO MONOPOLE ANTENNAS MATCHING AND DECOUPLING USING NF CIRCUITS (A), AND MATCHING USING NF CIRCUIT AND DECOUPLING USING PASSIVE CIRCUIT (B)	109
FIGURE 4.47 TWO PORT NETWORK REPRESENTATION (A), EVEN-ODD MODE REPRESENTATION (B)	110
FIGURE 4.48 SIMULATED RETURN AND INSERTION LOSS OF NF MATCHING AND DECOUPLING (A), NF MATCHING AND PASSIVE DECOUPLING (B).....	111
FIGURE 4.49 PROPOSED FD TOPOLOGY (A), WITH IDEAL ELEMENTS (B)	112
FIGURE 4.50 SIMULATED RETURN AND INSERTION LOSS OF IDEAL FD SYSTEM	112
FIGURE 4.51 COMPARISON BETWEEN SIMULATED RETURN AND INSERTION LOSS WITH IDEAL ONES.....	112

List of Tables

TABLE 1.1 COMPARISON BETWEEN HD AND FD	7
TABLE 1.2 ROUGH ESTIMATION OF SI CANCELLATION REQUIREMENTS TO ENABLE FD IN 4G AND Wi-Fi	10
TABLE 1.3 SUMMARY OF THE FOUR TOPOLOGIES	18
TABLE 2.1 IMPEDANCE CONVERTER AND INVERTER PARAMETERS	25
TABLE 2.2 COLLECTION OF NIC TOPOLOGIES	26
TABLE 3.1 PARAMETRIC STUDY ON INDUCTOR AND FREQUENCY OF OSCILLATIONS	57
TABLE 3.2 COMPONENTS USED IN THE IMPLEMENTED NIC.....	61
TABLE 3.3 COMPONENTS USED IN THE IMPLEMENTED NIC USING BFR93A	65
TABLE 3.4 COMPONENTS USED IN THE IMPLEMENTED PS USING SKY TRANSISTOR	70
TABLE 4.1 BANDWIDTH COMPARISON BETWEEN DIFFERENT MATCHING TOPOLOGIES	93
TABLE 4.2 COMPONENT VALUES FOR EACH TOPOLOGY	100
TABLE 4.3 COMPONENT VALUES USED IN BOTH TOPOLOGIES OF COMBINED PASSIVE AND NF MATCHING.....	107
TABLE 4.4 COMPONENTS VALUES FROM CALCULATION USED IN BOTH MATCHING AND DECOUPLING TOPOLOGIES	110

General Introduction

This PhD study is made in the context of a co-tutelle work between the Lebanese university and Université de Bretagne Occidentale (UBO, Brest). At UBO, this PhD is hosted at Lab-STICC laboratory (UMR CNRS 6285) in the MOM department (Microwave, Optoelectronics and materials) in the DIM Team (Dispositifs et Interfaces Multiphysiques). The field of investigation of DIM team is wide and the design of devices and systems in RF and Microwave domain is the federative element of the team that brings original solutions in various domains: telecommunications, sea, defense and health.

The main goal of this work consists in achieving a wireless Full-Duplex (FD) system where the user can transmit and receive signal using the same frequency at the same time. Our aim is to build this FD in the context of small electronic devices (e.g. IoT, 5G...). In addition, many standards and frequency bands are emerging currently, which lead us to focus on a wide operating bandwidth.

In wireless Full-Duplex system, the main issue is the self-interference (SI) that occurs between the transmitter chain and the receiver chain. The SI cancellation (SIC) architecture is usually divided into three main parts: decoupling or isolation at the antenna level (often called passive decoupling), analog cancellation (either in RF or in baseband) and digital cancellation. This thesis is dedicated to SIC at the antenna and analog levels in order to achieve a high isolation level (at least 40dB) between the transmitter chain and the receiver chain.

In the context of wireless Full-Duplex for wireless small devices, the most restricting constraint comes from the limited space, which is very tricky upon antenna design. Indeed, ideally the antenna should be single and small. However, none of single antenna full-duplex system is able to emit and receive following the same direction, which is mandatory for our system. Moreover, most Full-Duplex systems that include SIC system at the antenna level rely on wave cancellation at RX antenna and thus require at least three antennas.

Analyzing state-of-the-art on FD wireless system is thus of prime interest to bring out the pros and cons of the most relevant systems for our application. The four main topologies are compared in chapter I and are identified to be narrow band and difficult to transpose to our context. Therefore, we put forward a FD topology that consists of the first two stages of SIC (i.e. antenna decoupling/isolation and analog cancellation). The first stage consists in matching and decoupling the two antennas in order to widen the frequency bandwidth of FD and offers a first level of SIC. The second one requires a tunable phase shifter (slightly tunable around 180°) associated with an attenuator. By combining these two stages together, we expect to achieve a high isolation level between the transmitter chain and the receiver chain over a wide frequency range.

Our redefined goals are therefore to build up the first stage of SIC (i.e. matching and decoupling network) and to design a variable PS that is going to be used in the second stage of SIC.

Since our goal is dedicated for small electronic devices (e.g. IoT ...), miniaturized antenna are thus required. One way to miniaturize an antenna is to shift down its operating frequency band. Such antennas are known as ESA (Electrically Small Antenna). Classical passive matching networks can do this but only over a narrow band due to a gain-bandwidth limitation. Indeed, in order to widen the bandwidth of our antenna we could introduce losses into the system, which in terms would lower the antenna gain. Thus for a wider high gain

band result, we suggest to use non-Foster matching circuit (i.e. that use negative capacitances and inductances). Chapter II will present a state-of-the-art of the different kinds of non-Foster circuits. Among them, XCP circuits (cross-coupled pair of transistors) seem a priori more likely to get wider frequency response than other techniques. In addition, we propose to study the behavior of NF circuit (i.e. how it works) in details through analysis and synthesis equations in order to understand the negative behavior of the system and to identify the most significant associated parasitic effects. Finally, Normalized determinate function (NDF) technique that seems to be the most relevant technique for XCP stability analysis will be described and will be used in order to test the stability of our circuits under study.

In Chapter III, a Phase Shifter (PS) topology based on NF circuit is introduced. The phase shifter offers a 180° phase shift potentially tunable (theoretically pure phase value, i.e. a flat phase in transmission) between its two ports and requires the use of negative capacitance. We will present a thorough study of the PS topology, including equations and expected ideal performance. The PS design performance greatly depends on the quality of the negative capacitance, which is difficult to keep ideal over a wide frequency band. Thus, we will present and test experimentally different configurations and improvements in the design of XCP circuits in order to improve the purity of the non-Foster element. Moreover, the stability method described in chapter II will be used to verify the reliability of this key element of the PS but also of this PhD work. Several parameters are likely to be tricky when working above 1GHz with XCP circuits. At least, three of them should be particularly supervised: i) the residual real part of XCP circuit, ii) interconnect lines and iii) the transition frequency of the selected transistor. The first one should influence the PS performance whereas the two others could bring stability issues.

In chapter IV, our goal focuses at last on the design of the wireless compact FD system. The relevance and performance of the proposed topology will be studied by considering a system based on two closely separated planar monopole antenna. All studies and techniques explored and validated in previous chapters will be implemented here to move towards this goal. Thereby, non-Foster circuits will be used to match the antennas in a wide frequency band much lower than their initial resonance frequency (i.e. antennas are then considered as electrically small antenna (ESA)) and also to decouple the antennas in order to get a first level of SIC. Prior to that, the definition of ESAs and their limitations using only passive element for matching will be recalled. A methodology study will be carried out in order to find the best way to match the antenna in order to have a wideband high gain performance. Almost at all steps (i.e. matching, decoupling), analysis equations will be given and the results obtained by using actual non-Foster components will be compared in simulation and experimentally to those from passive networks. Moreover the efficiency of the whole systems (passive and NF) will be quantified and compared. We will also put forward some improvements in the NF decoupling architecture.

Lastly, we will combine the two stages of SIC together (i.e. at the antenna level and by using PS and attenuator). As a first step, we will identify the maximum achievable SIC level by using ideal elements that will serve as a reference while implementing our actual NF components. A discussion will be given to identify the origin of any differences between the ideal response and the obtained one.

Finally, some conclusions will be drawn and some prospects will be suggested to go beyond the potential limitations of our compact FD system.

General Introduction

This PhD study is made in the context of a co-tutelle work between the Lebanese university and Université de Bretagne Occidentale (UBO, Brest). At UBO, this PhD is hosted at Lab-STICC laboratory (UMR CNRS 6285) in the MOM department (Microwave, Optoelectronics and materials) in the DIM Team (Dispositifs et Interfaces Multiphysiques). The field of investigation of DIM team is wide and the design of devices and systems in RF and Microwave domain is the federative element of the team that brings original solutions in various domains: telecommunications, sea, defense and health.

The main goal of this work consists in achieving a wireless Full-Duplex (FD) system where the user can transmit and receive signal using the same frequency at the same time. Our aim is to build this FD in the context of small electronic devices (e.g. IoT, 5G...). In addition, many standards and frequency bands are emerging currently, which lead us to focus on a wide operating bandwidth.

In wireless Full-Duplex system, the main issue is the self-interference (SI) that occurs between the transmitter chain and the receiver chain. The SI cancellation (SIC) architecture is usually divided into three main parts: decoupling or isolation at the antenna level (often called passive decoupling), analog cancellation (either in RF or in baseband) and digital cancellation. This thesis is dedicated to SIC at the antenna and analog levels in order to achieve a high isolation level (at least 40dB) between the transmitter chain and the receiver chain.

In the context of wireless Full-Duplex for wireless small devices, the most restricting constraint comes from the limited space, which is very tricky upon antenna design. Indeed, ideally the antenna should be single and small. However, none of single antenna full-duplex system is able to emit and receive following the same direction, which is mandatory for our system. Moreover, most Full-Duplex systems that include SIC system at the antenna level rely on wave cancellation at RX antenna and thus require at least three antennas.

Analyzing state-of-the-art on FD wireless system is thus of prime interest to bring out the pros and cons of the most relevant systems for our application. The four main topologies are compared in chapter I and are identified to be narrow band and difficult to transpose to our context. Therefore, we put forward a FD topology that consists of the first two stages of SIC (i.e. antenna decoupling/isolation and analog cancellation). The first stage consists in matching and decoupling the two antennas in order to widen the frequency bandwidth of FD and offers a first level of SIC. The second one requires a tunable phase shifter (slightly tunable around 180°) associated with an attenuator. By combining these two stages together, we expect to achieve a high isolation level between the transmitter chain and the receiver chain over a wide frequency range.

Our redefined goals are therefore to build up the first stage of SIC (i.e. matching and decoupling network) and to design a variable PS that is going to be used in the second stage of SIC.

Since our goal is dedicated for small electronic devices (e.g. IoT ...), miniaturized antenna are thus required. One way to miniaturize an antenna is to shift down its operating frequency band. Such antennas are known as ESA (Electrically Small Antenna). Classical passive matching networks can do this but only over a narrow band due to a gain-bandwidth limitation. Indeed, in order to widen the bandwidth of our antenna we could introduce losses into the system, which in terms would lower the antenna gain. Thus for a wider high gain

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Chapter 1

Full Duplex Overview

1. Introduction

The evolution of the mobile cellular and wireless networks has led to increased global network traffic [1]. The increase of smart devices (e.g., smart phones, and Internet of Things (IoT) devices) and the race for 5G drives toward finding a solution for air interface enhancements to use the radio resources more efficiently. Future 5G objective is to provide capabilities for very high data rates, very low latency, high reliability, and the possibility to handle intense device densities, in both cost and energy efficient manner [2]. Moreover, 5G and IoT are strongly related as 5G, due to its highly flexible architecture, is intended to offer a unified communication platform for the IoT and thus to potentially be a catalyst for IoT growth and vice versa.

In that context, Full-duplex (FD), i.e. transmitting and receiving simultaneously in the same frequency band, has received significant attention in both academia and industry [3], [4]. Several efforts are now underway to use FD technology in future cellular 5G standards [5] and in IoT [6].

FD wireless transmission is considered as an encouraging method for future wireless systems as it handles many key issues spectral efficiency. Nevertheless, this FD approach places strong requirements to the transceiver implementation due to self-interference (SI) phenomena (i.e. the transmitter signal is leaking into its own receiver signal). But if it is successfully handled, it will provide significant improvements to wireless systems [7]. Enabling wireless devices to operate in FD mode will lead to doubling their spectral efficiency in terms of transmitted bits per second per Hz. FD system can improve collision avoidance/detection mechanism, reduce air interface delays in networks, and improve the secrecy performance of the system [8].

FD wireless technique has been already used in the 1960's with FD radars [9] with a approach named "feed-through nulling". A high level of isolation was experienced but the system was very bulky, heavy and expensive which avoid such implementations in spatial and terrestrial wireless communication systems like cellular mobile. In relay configurations, Full Duplex systems have been used in some special cases such as high gain cell enhancer but they required a high physical separation and isolation between the receiver and transmitter more likely to be feasible in a relay context; moreover these systems had to face out some severe restrictions on the transmitter output power [10].

However, interest in using FD for the future evolution of wireless systems has significantly increased in the past few years due to some actual and reliable implementations. Potential use cases proposed for FD include relaying, microwave backhaul links, mesh networks, cognitive radio, access points/base stations and mobile systems [11], [12]. Short-range systems (e.g., Pico-cells in mobile wireless systems and Wi-Fi systems) are especially feasible operation environments for FD because the SI requirements are much more relaxed in these environments compared to large cell systems.

1.2 Duplexing Technique in Modern Wireless Links

Globally, wired and wireless communication can be either simplex or duplex. A simplex communication is a one-way communication. On the other hand, a duplex communication is a two-way communication, where both nodes can communicate with each other in both forward and reverse directions. Duplex systems are presented in two forms: Half-Duplex (HD) and Full-Duplex communication FD. Figure 1.1 shows the three communication techniques: Simplex, Half-Duplex and Full-Duplex. Most current communication terminals operate in HD mode, separating the transmission and reception in either time or frequency domain. Wireless HD is a bidirectional transmission, which is mainly based on two orthogonal channels using time (i.e., Time Division Duplex (TDD)), or frequency (i.e., Frequency Division Duplex (FDD)) dimensions, in order to offer a separation between the transmitted and received signals. These methods are described in the following sections.

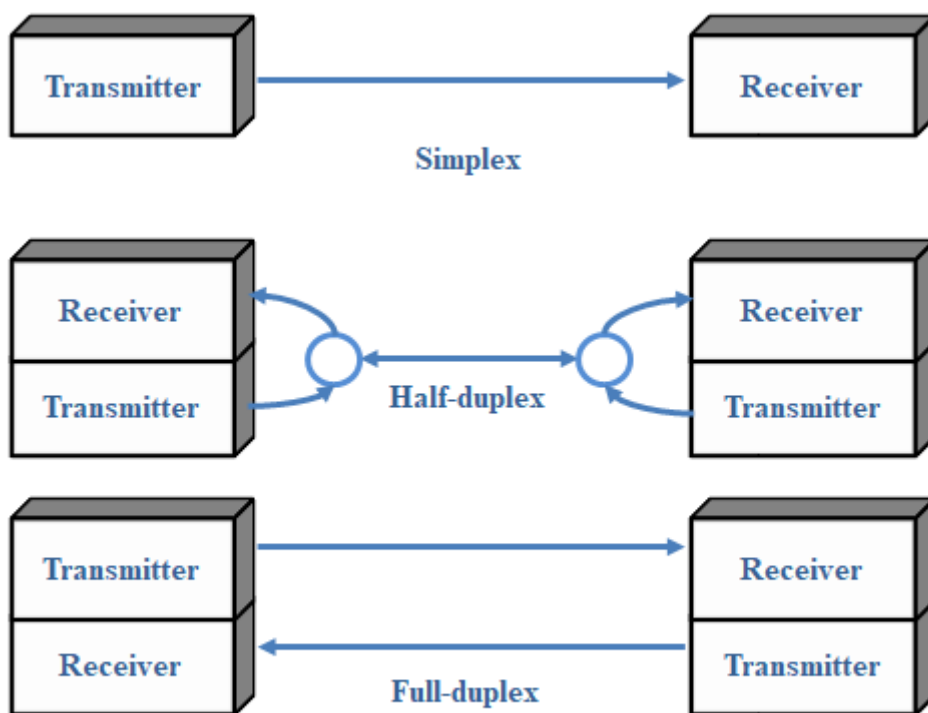


Figure 1.1 Transmission modes

1.2.1 Time Division Duplex (TDD)

TDD uses a single frequency band for transmitting and receiving. This method uses the same frequency band by assigning different time slots to transmit and receive information. For example, uplink is transmitted at time 'T1' instance and downlink is transmitted at time 'T2'. Both uplink and downlink transmissions will take place at same RF carrier frequency [13]. The information to be transmitted can be voice, video, or computer data in serial binary format.

1.2.2 Frequency Division Duplex (FDD)

In FDD, both uplink and downlink transmissions will be assigned two separate frequencies F_{c1} and F_{c2} respectively. Both utilize same time slot 'T' for transmission. FDD uses more frequency spectrum resources, generally at least twice the spectrum needed by

TDD. However, it does not suffer from discontinuous transmission encountered using TDD. Despite that, in both TDD and FDD the available communication resources are not efficiently utilized. Both TDD and FDD are two spectrum usage techniques used for mobile communication networks such as mobile Wimax, LTE, etc.

1.2.3 Other Duplexing/Multiplexing Transmission Techniques

Other duplexing and multiplexing techniques can be combined with TDD and FDD classical techniques, such as orthogonal frequency division multiplexing access OFDMA, which uses a large number of frequency carriers orthogonal to each other (i.e. the peak of each carrier starts at the null of its neighbor carrier). CDMA (Code division multiple access CDMA) is another duplexing technique that allows numerous signals to occupy a single transmission channel, where each signal has its own code. So only a receiver whose frequency response is programmed with the same code can intercept it. Both OFDMA and CDMA use multiple frequencies for communications thus more frequency spectrum resources are required; moreover, both are utilized in FDD or TDD mode.

In order to enhance the efficiency of wireless and mobile communications, it is relevant to transmit and receive simultaneously in the same frequency band and simultaneously, which is leading to Full-Duplex technique. Indeed, FD uses the same frequency and same time slot for both uplink and downlink which overcomes both TDD and FDD in term of efficient usage of link resource [13]. Figure 1.2 shows FD technique compared to both TDD and FDD in terms of upload and download data.

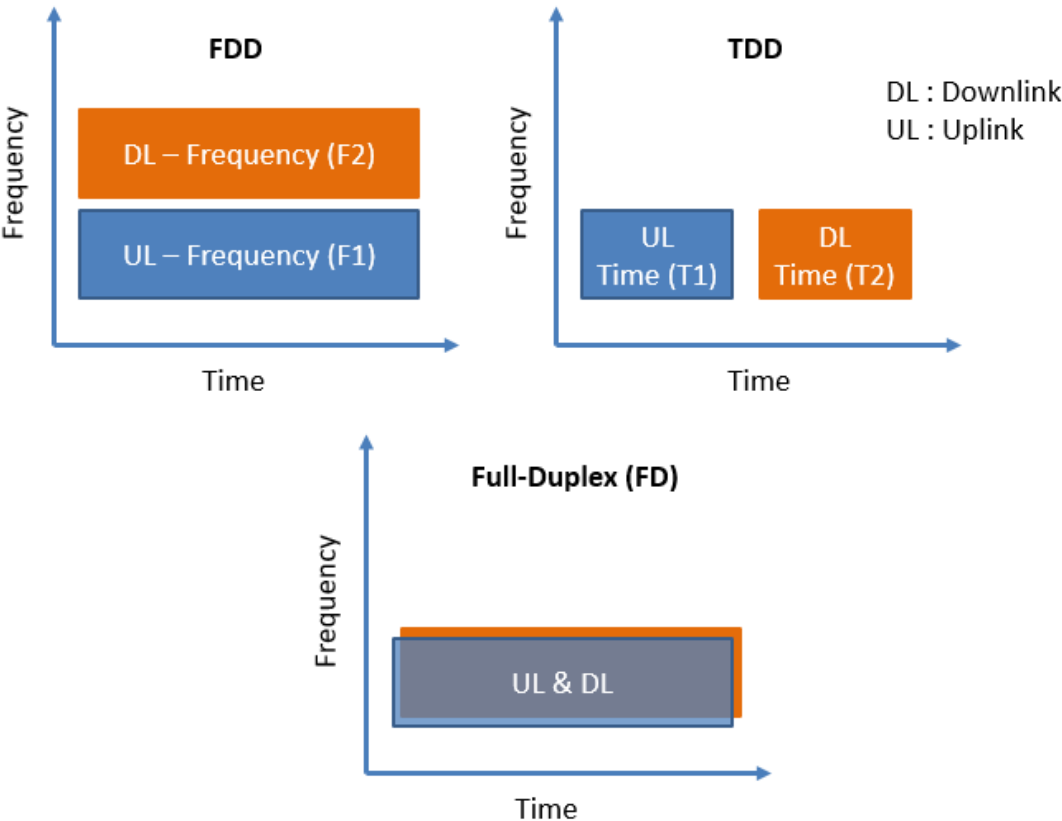


Figure 1.2 Comparison between TDD, FDD, and FD in term of uploading and downloading data in frequency and time domain

1.3 Advantages and Disadvantages of Full-Duplex technique

FD has several advantages, but also exposes weaknesses compared to HD. For example, due to a double throughput gain, an FD node has to process twice as many packets as an HD node due to its simultaneous transmission and reception. The advantages and disadvantages of FD are summarized below.

Advantages of FD:

- **Throughput gain:** As compared to HD, FD has nearly doubles the throughput gain of HD. But none of the existed FD techniques experimentally attained the theoretical doubling throughput gain, because the wireless system always suffer from signal to noise ratio (SNR) loss due to the high self-interference (SI) problems, which is caused by the large power difference between the transmitted signal and the received signal of interest arriving from a remote antenna (TA) [14]. In fact, strong SI may decrease the SNR of FD to fall below that of the HD systems, which in this case destroys the interest of using FD.
- **Solving the hidden terminal problem:** The problem of hidden terminals can be solved using FD. Let us consider a scenario of multiple nodes having data in their buffer for direct transmission and reception from a common access point (AP). If a node starts transmitting its data to the AP and the AP simultaneously starts transmitting data back to this node, the other nodes will hear the transmissions from the AP and delay their transmissions to avoid collisions. By using FD, the node will not delay its transmission because FD uses the same link to transmit and receive data.
- **Reducing congestion:** link congestion occurs when a link is carrying more data than it can handle. This might lead to package lost. However, with the aid of FD, a node is capable of both transmitting and receiving simultaneously; hence, the network throughput approaches the single link capacity, while simultaneously benefitting from the spatial diversity gain.
- **Reducing the end-to-end delay:** as compared to the conventional store-and-forward technique employed in HD, FD is capable of forwarding and receiving package at same time, which reduces the end-to-end delay between the two remote nodes.

Disadvantages of the FD:

- **SI:** Using the FD technique, the power of the transmitted signal is higher than that of the received signal, and back reflected signals also affect the received signal, hence, the interference imposed upon the received signal would consequently degrades the FD throughput gains.
- **A higher buffer size:** a sufficiently large buffer size compare to HD is required for enabling the packets to be forwarded (that would otherwise have been discarded due to queue overflow).

The advantages and disadvantages of FD compared to HD are summarized in Table 1.1. In practical implementations, the decision as to whether adopting the FD or the HD depends on several factors, such as the system throughput gain required, the SI cancellation capability, and the affordable hardware/software complexity, etc. Among the mentioned factors, the SI signal significantly constrains the advantages of the FD techniques and would be the key limiting factor in developing FD systems.

Table 1.1 Comparison between HD and FD

Content	HD	FD
Throughput Gain	Lower	Higher (in theory is 2 x that of HD)
Hidden Terminal Collision	Suffered	None
Congestion	Higher	Lower
End-to-end Delay	Higher	Lower
Self-Interference	None	High
Queuing Size	Smaller	Larger

SI degrades the receiver (RX) performances unless it is cancelled out (ideally to noise floor level). The total SI cancellation depends on the system scenario and should reach more than 100dB in some applications, particularly those with long distance wireless links. To solve this challenge, the SI reduction needs to be implemented in multiple stages across the FD transmitter (TX) chain. The implementation of the FD is limited by the capability of the radio transceivers to be able to provide a high SI cancellation level. To overcome this problem, an implemented method should prevent the transmitted signal from leaking back to its own receiver and to cancel any SI from the receiver path using knowledge of the transmitter signal. These methods should be implemented along the TX chain, including digital chain, analog chain, and at the antenna level. More details about SI are developed in the following sections.

1.4 Sources of Self-Interference

Potential use cases for FD transmission in wireless networks are short-range radio connections, such as in future 5G small indoor or outdoor radio cells (e.g., femto or pico-cells), device-to-device connections, transmission in mesh networks, etc. The main target in all cases is to improve spectral efficiency beyond legacy HD. Depending on the system scenario, the transmitted power level may range from 80dB to 120dB higher than the receiver noise-floor level, implying that the total SI cancellation should be at least on the same order. Figure 1.3, shows a FD link with a local and remote TX chain. Each chain has one antenna to transmit and another one to receive signal. We can notice three main sources of SI that limit the proper reception of the signal coming from the remote node by the local RX. First, leakage occur on-board (type A). Such direct cross talk is predominant in dense integration. Second, line-of-sight leakage between the two antennas may also occur (type B). This SI is reduced by implementing antenna with specific polarizations or radiation patterns or by isolating between the two antennas. Finally, TX signals can be reflected from nearby objects back into the receiver (type C). Such multipath reflection results in frequency-dependent SI and is particularly challenging in numerous multipath channels, mainly Non-line-of-sight (NLOS) path, encountered in indoor environment.

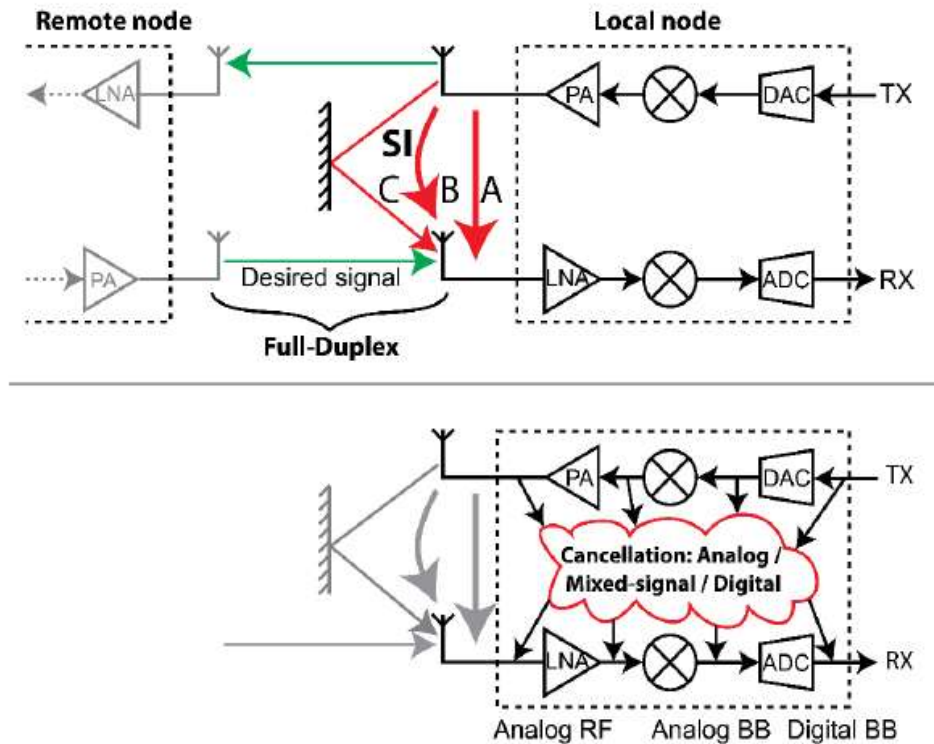


Figure 1.3 Various levels in the TX and the RX chain to get SI cancellation

Most of the SI cancellation techniques rely on copying a reference signal from the TX chain and subtracting it after modification (i.e. attenuation and phase shifting) in the RX chain. Figure 1.3 provides all possible places in the transmitter and receiver chain where we can apply SI cancellation methods. The RF/analog and antenna solutions focus on canceling the SI from direct cross talk and line-of-sight leakage (type A and B), while the digital solutions cancellation is introduced to suppress the residual SI below or close to the receiver noise floor thanks to adaptive algorithms and covering also the SI due to multi-path reflection.

1.5 FD Requirements

To implement FD, SI needs to be cancelled enough so that its power is reduced to the same level as the receiver noise floor. There is no point in canceling beyond that level since we will not see any benefits. Considering a scenario where the main signal is being transmitted at 20dBm (100mW) and having a noise floor level around -90dBm, then SI is then calculated as $20 - (-90) = 110\text{dB}$ above the receiver noise floor. The transmitter noise is around 50dB above the receiver noise floor, and the nonlinear harmonic components are 80dB above the noise floor as shown in Figure 1.4. Note that these numbers are consistent with other RF measurement studies reported in [15] for standard Wi-Fi. Moreover, if SI is not sufficiently cancelled, then any residual SI will act as noise or jammer to the received signal and degrades SNR. For instance, if the received signal SNR without FD is 25dB but after using FD it is reduced to 5dB due to 20dB residual SI. This is worse than using the original HD link with 25dB SNR and it is better in this case to turn off FD.

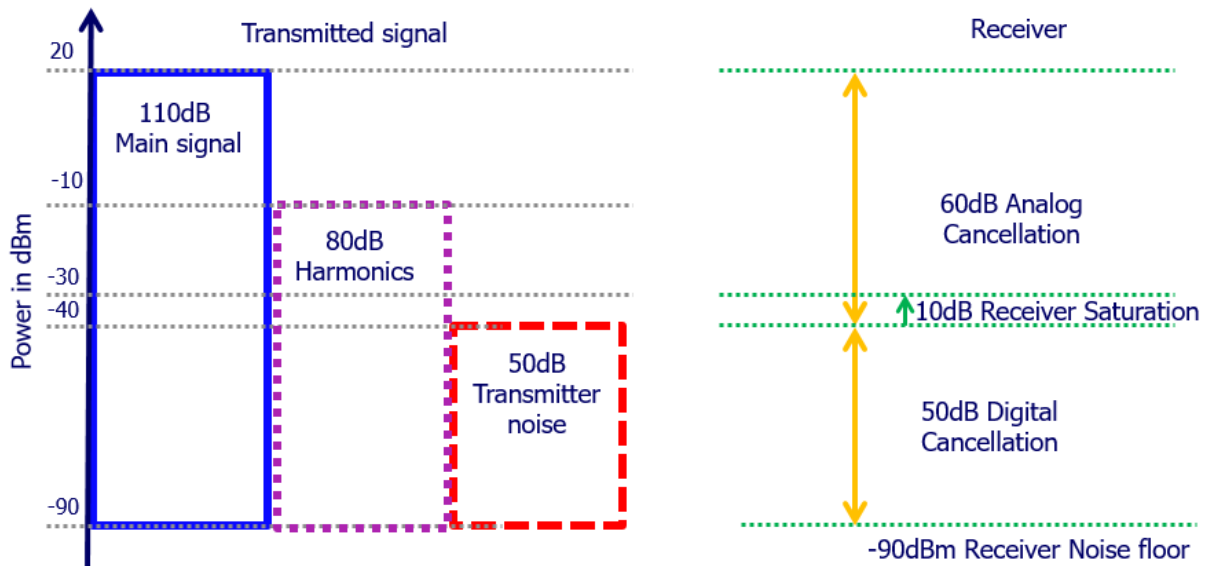


Figure 1.4 Illustration of required levels and distribution of SI cancellation

There are four main ideas from the above analysis:

- 1) Most FD system need to provide around 110dB of SI cancellation to reduce it to the receiver noise floor.
- 2) Transmitter noise is by definition random noise, which cannot be cancelled by any algorithm. The better way to cancel transmitter noise is to copy the TX signal in the analog/RF domain section and cancel it there.
- 3) A final constraint is that if the SI signal is above the analog to digital converter (ADC) full scale range, this leads to the saturation of the RX chains. Assume a 12 bits ADC resolution is used in Wi-Fi systems, in practice it is necessary to leave 2 bits of margin (i.e. a 12 bits ADC should be used as a 10 bits ADC to reduce quantization noise). We have a theoretical 60dB of dynamic range, which implies that the strongest signal level that can be present on the input to the radio relative to the receiver noise floor is $-90\text{dB} + 60\text{dB} = -30\text{dB}$, beyond this level the receiver will go into saturation.

To sum up, most FD design needs to provide at least 110dB of linear cancellation that can only be achieved by combining multiple levels of SIC, e.g. 60dB of analog cancellation and 50dB of digital cancellation as seen in Figure 1.4. Furthermore, Table 1.2 [16], [18] presents the amount of SI cancellation required to enable FD operations in several technologies for both 4G and Wi-Fi. Despite that, if by any chance the analog and digital cancellations suffer from some performance degradations due to hardware imperfections, their combined cancellation may not be enough. To solve this problem a method called passive suppression [19] is also invoked to reduce the SI by increasing the pass loss between the transmitting and receiving antenna of the FD node (Figure 1.5). In the following sections, we will address some methods to perform passive suppression, digital and analog cancelation of SI.

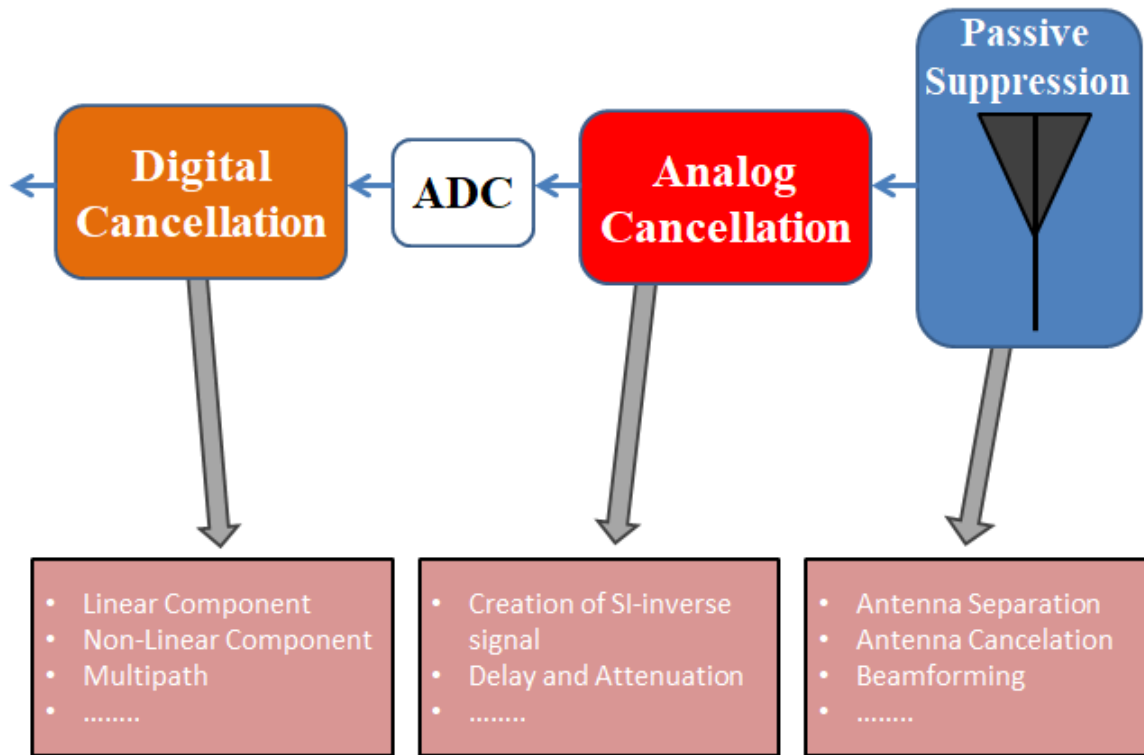


Figure 1.5 Different sections of SIC

Table 1.2 Rough estimation of SI cancellation requirements to enable FD in 4G and Wi-Fi

Generations	Technologies / Access Technology	Channel Bandwidth	Transmit power	Noise power	Required SI cancellation
4G	Long Term Evolution Advanced (LTE-A) (Orthogonal / Single Carrier Frequency Division Multiple Access) (OFDMA / SC-FDMA)	20 MHz	46 dBm	-101 dBm	147 dB
Mobile WiMAX	Worldwide Interoperability for Microwave Access (WiMAX) (Scalable Orthogonal Frequency Division Multiple Access (SOFDMA))	10 MHz	44 dBm	-106 dBm	150 dB
Wi-Fi	802.11ac - Gigabit Wi-Fi (nicknamed 5G Wi-Fi)	20, 40, 80, 160 MHz	20 dBm	-90 dBm	110 dB
	802.11ad - Wireless Gigabit (Microwave Wi-Fi)	2 GHz		-81 dBm	101 dB
	802.11af – White-Fi	5, 10, 20, 40 MHz		-98 dBm	118 dB

1.5.1 Passive Self-Interference Suppression

Passive or “antenna level” SI suppression is defined as the attenuation of the SI signal done by the path loss effect due to the physical separation and/or isolation between the TX and RX of the same node [4].

First, by reducing the electromagnetic coupling between the TX and RX at the antenna level, the power of SI can be reduced as it arrives to the receiving antenna. Numerous methods of passive SI suppression exist [20], [21]. For example, passive suppression can also depend on beamforming techniques by directing the lobes of TX and RX antennas in different directions [20], which also reduce the SI between the two antenna. This means that the system can emit and receive simultaneously in the same frequency band but not in the same direction, i.e. a complete FD wireless link is not allowed between two nodes. In a multi antenna system, the polarization decoupling technique enables the TX and RX antennas to operate with the help of orthogonal (e.g. horizontal and vertical) polarizations to reduce their coupling [21].

1.5.2 Analog Self-Interference Cancellation

The principle of most analog cancellation techniques can be summarized as follows: in order to sufficiently reduce the SI power, a copy of the radio signal is required to create a reference signal corresponding to a perfect replica of the SI signal. Combining the created replica with the SI signals is in theory capable of perfect SI cancellation [22]. Analog cancellation can take place either at the RF or at the analog baseband stage [23] or at both stages.

At RF level, analog cancellation can be realized by executing the following two steps:

- Creation of SI-inverse signal: Basically, SI inversion can be implemented by an FD radio upon simply inverting a signal by inverting its phase. A balanced/unbalanced (Balun) transformer, which is a common component in RF, can be utilized for perfectly (in theory) converting between an input signal and its inverse at all time.
- Delay and attenuation adjustment: Since the signal is transmitted over the ether, then it will surely experiences both attenuation and delay in all practical scenarios, hence an identical attenuation and delay has to be applied to the inverted SI as seen in Figure 1.6.

Nevertheless, subtracting the SI from the received signal by simply depending on the SI-inversion technique remains a challenge in practical systems, because the FD radio only knows the “clean” digital representation of the baseband signal, rather than its processed counterpart transmitted over the air. As discussed briefly in the upcoming section, digital SI cancellation is thus required to complete the Passive, analog and/or RF SIC level.

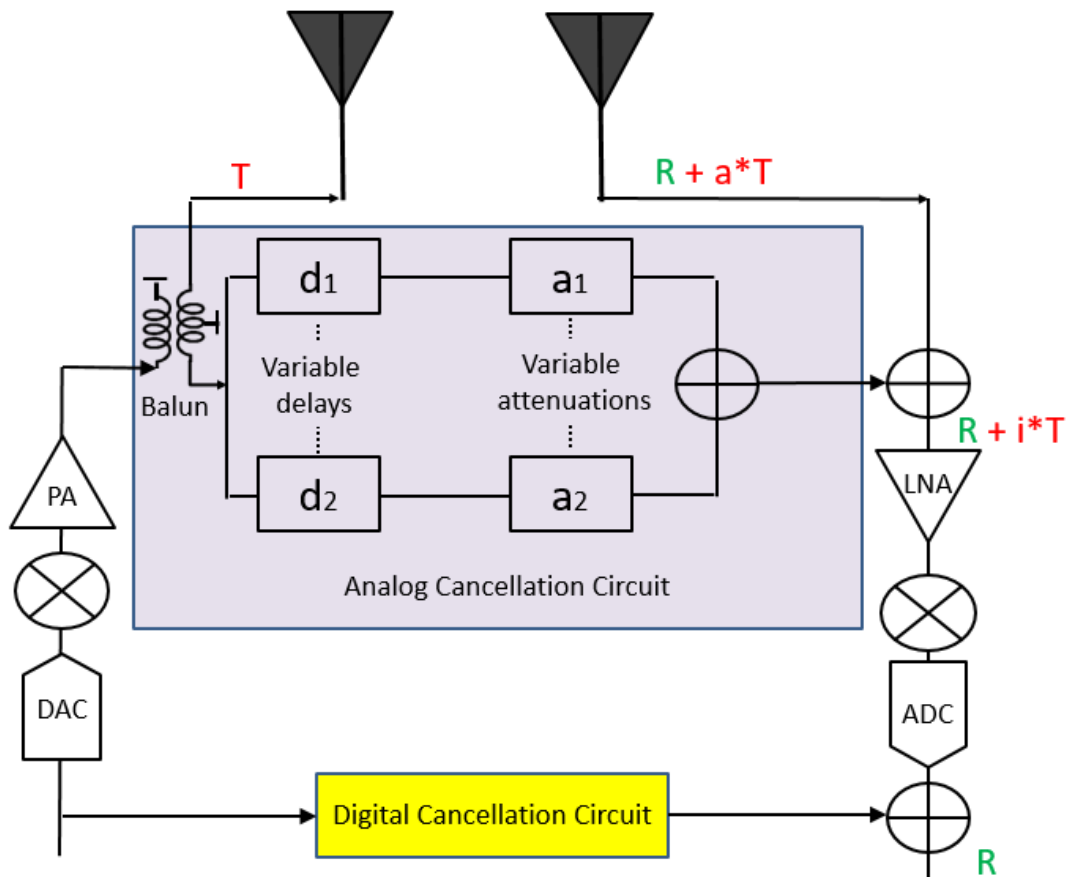


Figure 1.6 Block diagram of Analog RF self-interference cancellation

1.5.3 Digital Self-Interference Cancellation

Digital cancellation by definition operates in the digital domain and exploits the knowledge of the interfering signal in order to cancel it after the received signal has been quantized by the ADC [24]. To achieve this, the transmitter send first a reference signal to the receiver, which is used to estimate the linear and non-linear distortion in phase and magnitude experienced by the SI signal (mostly in the channel and analog/RF components). It allows building a copy of the actual residual SI to digitally subtract it. Coherent SI-detection can also be employed to recover the SI by correlating the received signal with the clean regenerated SI-inversion-based reference signal, which is available at the output of the FD transmitter. This technique then requires the receiver to estimate both the delay and phase shift between the transmitted and the received signals, relying on techniques such as the correlation peak-based algorithm for subtracting the SI signal. Consequently, the linearity and nonlinearity of the system component of the leakage channel must be accurately characterized for the sake of high SI cancellation in the digital domain, Figure 1.7 shows an example of block diagrams in digital baseband self-interference cancellation.

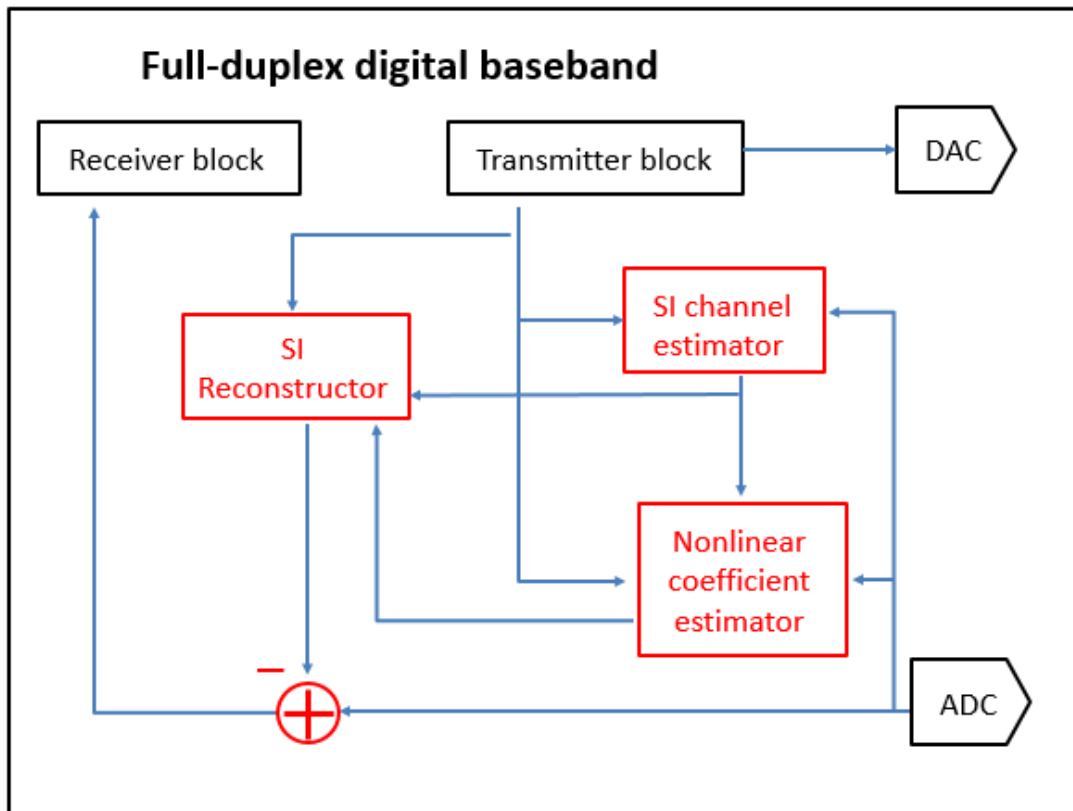


Figure 1.7 Block diagram of digital baseband self-interference cancellation

In conclusion, these three methods (i.e. antenna level, analog and digital SIC) are necessary for a FD system in order to achieve a high SI cancellation between the TX chain and the RX chain [11].

1.6 Distortion and noise issues in FD

Researchers at Stanford [22] and other groups in industry and academia [25] have proposed proof-of-concept designs to build FD system. It can be noticed that designing FD generally focuses first on SI cancellation at the antenna level mainly for two reasons. First, as the power difference between the transmitted and received signal is maximal, SI might cause a high risk of saturation of the receiver. Moreover, using directly the actual TX signal close to the antenna as a reference is preferable since it contains most information regarding any TX imperfections such as TX-generated noise and distortion that the signal has experienced. If, for example, the TX reference would be copied before the power amplifier (PA), then the PA nonlinearities would not be canceled out. Many designs have made significant progress on the SI cancellation problem [26]. However, some designs show 85dB of cancellation in simulation, which leaves about 25dB of residual SI (if 110 of SIC is expected as in Figure 1.4) and therefore reduces the SNR. To see the throughput benefits with these FD designs, the HD SNR of the link has to be extremely high (45dB or higher), i.e. the two nodes should be separated by not more than 5m to see such high SNRs. Outside this range, it would be better to turn off FD and use only the HD mode. However, these designs were intended for low-power and narrow-band wireless links, as ZigBee where 85dB of SI cancellation is sufficient for FD. Wi-Fi is far more demanding in terms of both bandwidth as well as cancellation level.

Indeed, the reader might ask: why achieving wireless FD is still so challenging. After all, the sender knows the signal being transmitted, subtracting it should be easy to implement), but in fact, the RX antenna does not know exactly what has been actually emitted. What it does know is the “clean” digital representation of the signal in baseband. Varying near-field environment (e.g. a person holding the device) constantly changes the magnitude and phase of type A and B SI (Figure 1.3), which requires an adaptive solution. When the signal is converted to analog and up-converted to the right carrier frequency, the TX signal will look different from its baseband form. Analog components in the TX chain alter the signal in both linear and non-linear ways, impairments and added noise (e.g., from PA) will also affect the signal. Moreover, small inaccuracy (e.g., oscillator might be tuned slightly off their oscillation frequency) will also shift the transmitted signal characteristics away from the expected SI. In fact, the transmitted signal is a combination of nonlinear function of the ideal transmitted signal along with unknown noise. Unsurprisingly, naively subtracting a “known” version of the TX signal without considering for all these analog distortions does not work.

RF front-end is not simply a black box that takes the digital signal, converts it to analog, up-converts it to the carrier frequency and sends it. In fact, this abstraction turns out to be incorrect. Radios distort the signal being transmitted. These distortions can be divided into three major categories:

- 1) Linear Components: these distortions on the modulated signal (e.g. 2 tones as in Figure 1.8.a) are due to attenuation and reflections from the environment. These are linear components because they can be written as a linear combination of delayed copies of the main two tones.
- 2) Non-Linear Components: these distortions are created from inside the circuit, because the circuit takes in an input signal x and create an output signal that contains non-linear cubic and higher order terms such as x^3 , x^5 . These higher order signals have significant frequency content close to the transmitted frequencies that correspond to all the harmonics that correspond to signal distortions, as seen in Figure 1.8.b.
- 3) Transmitter Noise: a radio will always have noise, for a typical WiFi radio the noise power level is of about -90dB (1 picowatt) [15]). This extra noise is generated from high power components in the transmitter chain such as Power Amplifier. The authors in [26] referred to as broadband noise. Figure 1.8 shows what the radio is expected to transmit (a), and what is actually transmitted (b).

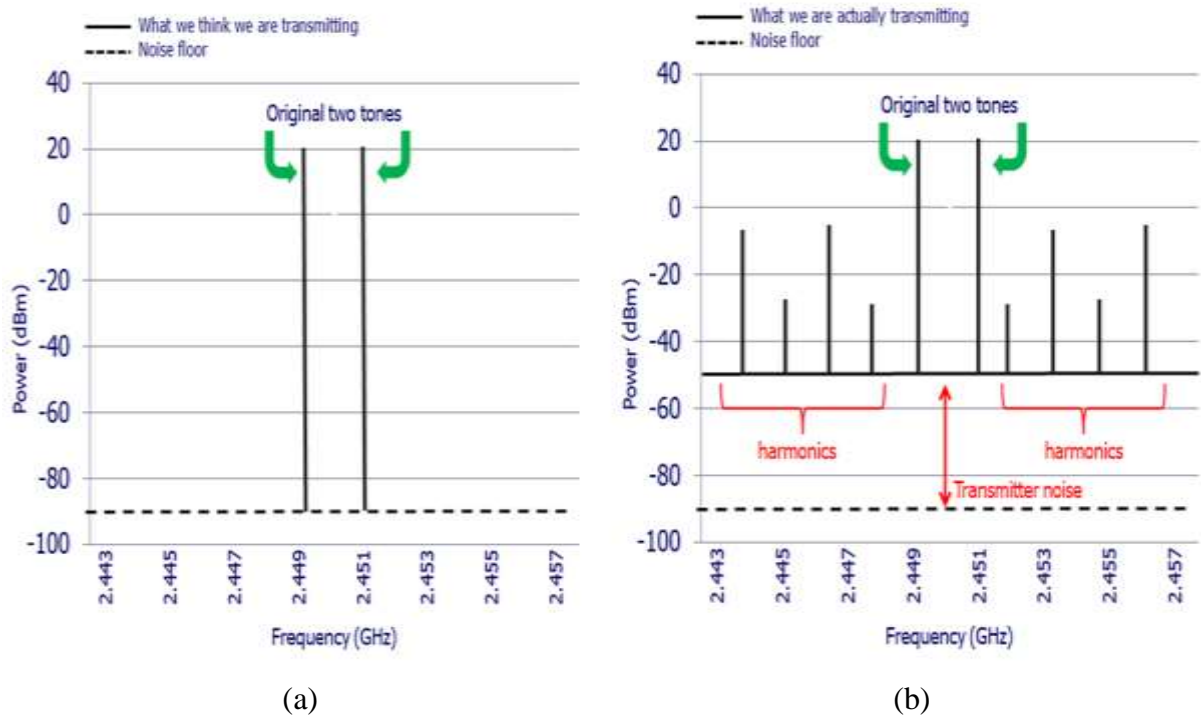


Figure 1.8 what the radio is expected to transmit (a), what is actually transmitted (b)

1.7 Proposed topologies for SI cancellation

Many designs have been proposed recently to implement FD wireless systems. All focus on achieving a high SI cancellation: some designs are based on SI canceling transceiver front-end structure [27]. Other designs are based on dual-polarized micro-strip patch antenna structures, complemented with an active analog cancellation network [28]. Other designs are based on an electrical balance duplexer circuit, which connects with a single port antenna [29]. The most significant ones are detailed below:

- 1) **Antenna separation:** This design is based on a variable phase shifter and a variable attenuator that are added between the two antennas (Figure 1.9). This path intends to provide a 180° phase difference and an identical signal level of the SI transmitted signal coupled at the receiver, in order to cancel it up at the receiver antenna [30]. In [30], a cancellation of about 33dB is achieved over a 100MHz bandwidth. The two antennas are separated from each other by a distance much greater than $\lambda/2$ in order to reduce the coupling level (direct SI) between TX and RX. On the other hand, this distance is not preferable for compact devices especially at lower operating frequency where the wavelength will be large.

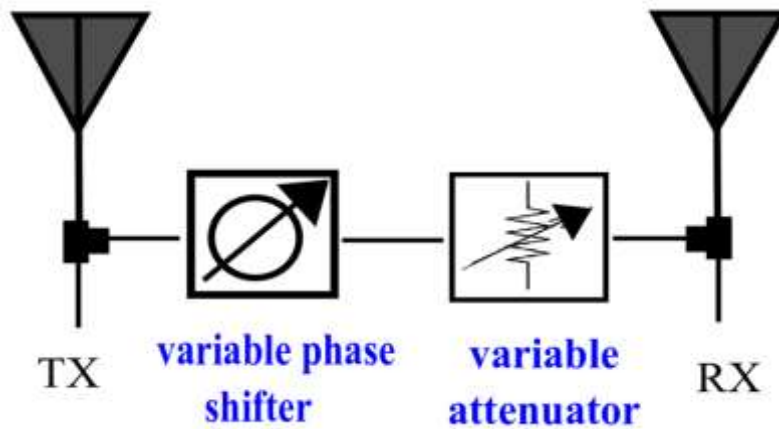


Figure 1.9 Antenna separation

- 2) **Antenna placement:** Two TX and one RX antennas are structured in a way to force the TX signals to cancel each other at the receiver position (Figure 1.10). The first antenna is set at a distance d from the receiver and the second antenna is at distance $d + \lambda/2$ from the receiver (λ is the wavelength of the operational frequency). As a result, there will be a 180° phase difference between them, which results in a destructive interference at the RX level. In theory, a null is created at the position of the RX if the leakage power magnitude level from the pair of TXs are identical which is impossible to obtain in practical implementation. Thus, this method can only reduce the SI from about 30dB and with the help of digital cancellation it can reach 60dB at least but remains intrinsically narrowband [30].

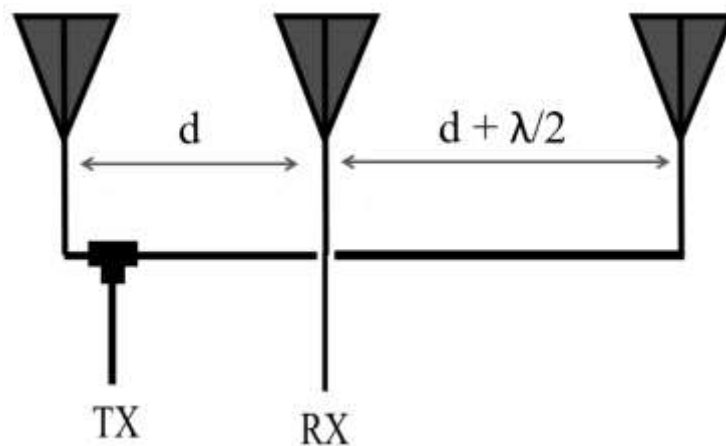


Figure 1.10 Antenna placement

- 3) **MIDU topology:** In MIDU (Enabling MIMO Full-Duplex) project, a symmetric placement of antenna is used to cancel SI in a FD system [31]. Antenna cancellation technique is duplicated at both transmit and receive stages. The two identical transmit antennas are separated by a distance d and transmit at the same time but with opposite phase; thus, for the receiver antenna, the potential null point will be located on the perpendicular bisector of the line connecting the two transmitter antennas Figure 1.11. The same principle is applied at the receiver stage and can potentially eliminate the need of other forms of analog cancellation, thereby avoiding the need for delays and variable attenuator. In [31], the overall isolation is about 45dB over a bandwidth of 625 KHz. It should be pointed out that the radiation patterns of TX antennas shows a null on RX antenna axis and identically for RX antenna pattern on TX axis. This technique is potentially more wideband than the second one.

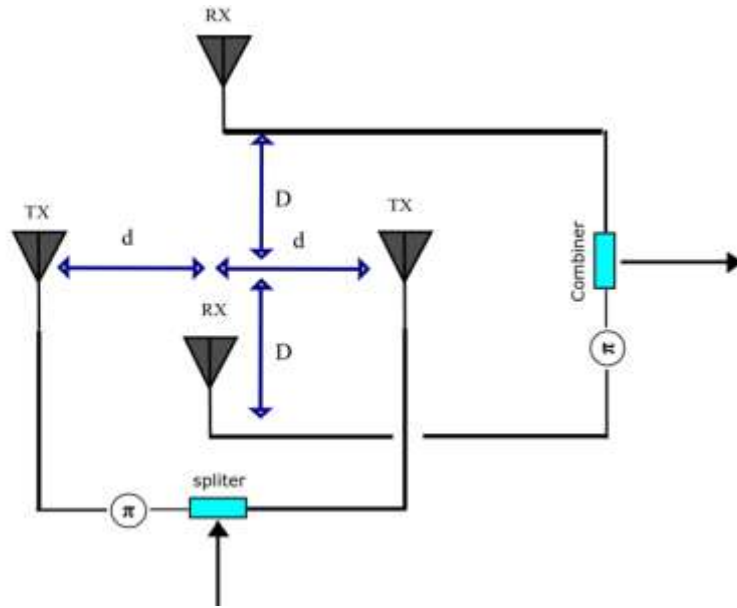


Figure 1.11 MIDU topology

- 4) **Electric Balance topology:** This technique uses only one antenna to transmit and receive simultaneously at the same time, which is an advantage for compact devices. The RF circuit is made up of a transformer and a balance network which is a tunable load impedance (Figure 1.12), virtually isolating the receiver from the transmitter [29]. In [29], this technique offers around 47dB of isolation over a narrow bandwidth about 229MHz.

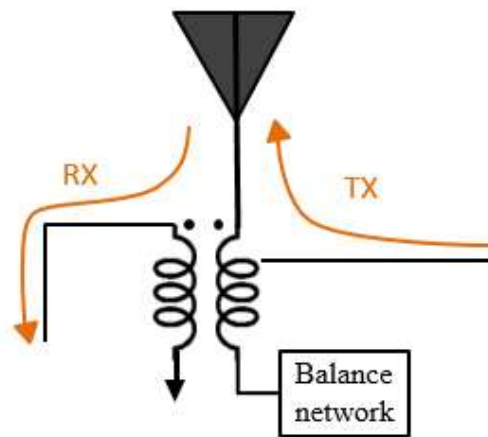


Figure 1.12 Electric Balance topology

Table 1.3 summarizes the four topologies advantages and disadvantages. These topologies are mainly suitable to actively boost the isolation between TX and RX branches. Indeed, in practice they can provide isolation by 30dB - 47dB before reflections (NLOS: Non-Line-Of-Sight paths) become the dominant SI. A complementary digital SI canceller with flexible and adaptive algorithm is then more suited to get rid of these NLOS reflections.

Table 1.3 Summary of the four topologies

Techniques	Isolation	Advantages	Disadvantages
Antenna separation	33dB	<ul style="list-style-type: none"> • TX and RX are widely separated which increase the path loss between them offering a good isolation • Suitable for narrowband scenarios 	<ul style="list-style-type: none"> • Requires manual tuning and therefore do not adapt to the environmental changes
Antenna placement	30dB	<ul style="list-style-type: none"> • Easy to implement 	<ul style="list-style-type: none"> • Requires 3 antennas; extra cost • Suffers from amplitude mismatch • Very narrowband
MIDU	45dB	<ul style="list-style-type: none"> • Suitable for narrowband scenarios • Offer higher cancellation level between TX and RX • Provides extra RF chain 	<ul style="list-style-type: none"> • Requires at least 4 antennas; extra cost • Suffers from amplitude mismatch • Requires manual tuning and therefore do not adapt to the environmental changes
Electric Balance	47dB	<ul style="list-style-type: none"> • Uses one antenna • Suitable for small compact devices • Not constrained by separation distance 	<ul style="list-style-type: none"> • Requires manual tuning • Suffers from non-linear distortions which limits isolation bandwidth

1.8 Antenna specifications for a compact FD system

The future communication generation (5G) and the strong demand for multi-function or multi-standard devices call for the use of wide-band/multi-band antennas. In Internet of Things (IoT), M2M (Machine to Machine) and medical sensors, antennas need to be implemented in small devices to ensure the interaction between the sensors and their environment and to allow a widespread use.

Thus, antennas are required to be small, compact and low-cost. Although the need for wide-band small antennas is spreading, the design and the matching of Small Antennas (SA) or Electrically Small antennas (ESA) is not an easy task especially in wide and low frequency band applications. Indeed, SAs famously suffer from high quality factor Q value since there is a high reactive energy stored in their near field and a small real power is propagated in their far field [32]. In other words, SA and ESA are intensely reactive, which results in a poor efficiency-bandwidth trade-off when using passive impedance matching [33]. This limit can be overcome by adding active elements, such as non-Foster Circuits (NFC) to the antenna's matching circuit, which are characterized by their negative reactance [33].

We suggest exploring in this PhD the study and design of NF circuits, which will serve as key components to achieve a high SI cancellation between two SAs in order to realize a compact full-duplex system. The Non-Foster circuits will be implemented at different levels of the front-end and a dedicated front-end topology is put forward in the following section.

1.9 Motivation, Objectives and Proposed topology

FD is an emerging subject that has attracted many researchers' interest through the past few years as it can play important role in the coming future 5G communications and IoT devices. However, there exist many challenges for deploying FD, the main one is the high SI cancellation between the TX chain and the RX chain. It was found out that for communication systems, we need around 110dB of SI cancellation, and this cancellation can only be achieved by two levels of SIC at least, i.e., analog and digital cancellation. Analog cancellation focuses on the Radio front-end and can proceed at antenna stage and/or in RF/analog-base band circuits, while digital cancellation is basically an algorithm that deals with all the distortions and noise that the signal faces along the RX chain and in NLOS channels.

Many topologies have been recently studied to achieve FD system, where they can offer around 30dB - 47dB of SI cancellation at the analog/RF stage. The amount of SI cancellation needed depends mainly on the system scenario and application; and since our focus is on small devices (e.g. IoT), the need of compact devices is of prime interest. Then, our goal is to design a compact FD front-end based on two small antennas (TX and RX) working at a low frequency range and if possible over a wide frequency range. In that context, the two antennas have to be small and need to be really close to each other, i.e. much more closer than in previous FD front-end studies. It means that none of the aforementioned approaches is suitable for these tough specifications.

Indeed, the close proximity of the antennas requires a specific decoupling topology where non-Foster circuits may bring some advanced solutions by cancelling or compensating the reactive components that model the antenna coupling. The Non-Foster circuits, through is a dedicated matching network, seem also to be a promising way to shift antenna operating band to low frequency which corresponds to compactness improvement.

Moreover, a 2nd stage or complementary SI cancellation circuit is intended to achieve a higher SI cancellation level and we put forward the design of a 180° phase shifter based on non-Foster in that aim.

In this thesis, we propose to design and implement a compact FD front-end system following the topology depicted in Figure 1.13 . A Non-Foster circuit will be studied first. Then, a phase shifter tunable around 180° over a wide frequency range will implemented by using this NF circuit. A frequency band from 1GHz to 4GHz will be targeted. This tunable phase shifter is dedicated to the second level of SI cancellation (i.e. analog SIC in figure 1.13). This Non-Foster topology will also be used to match and decouple two antennas placed close to each other in order to get the first level of SIC. The antennas will have initial resonance frequencies around 2.3-2.4GHz. The matching and decoupling circuits are intended to allow the antennas to operate at a lower and wider frequency range than their initial operating bandwidth (i.e. at around 1.6GHz), which corresponds to a miniaturization of antennas, namely electrically small antenna (ESA), suitable for compact devices such as IoTs.

We are hoping for our topology to provide at least 45dB of SI interference cancellation, which is at the state-of-the-art level and potentially sufficient for short-range wireless FD system.

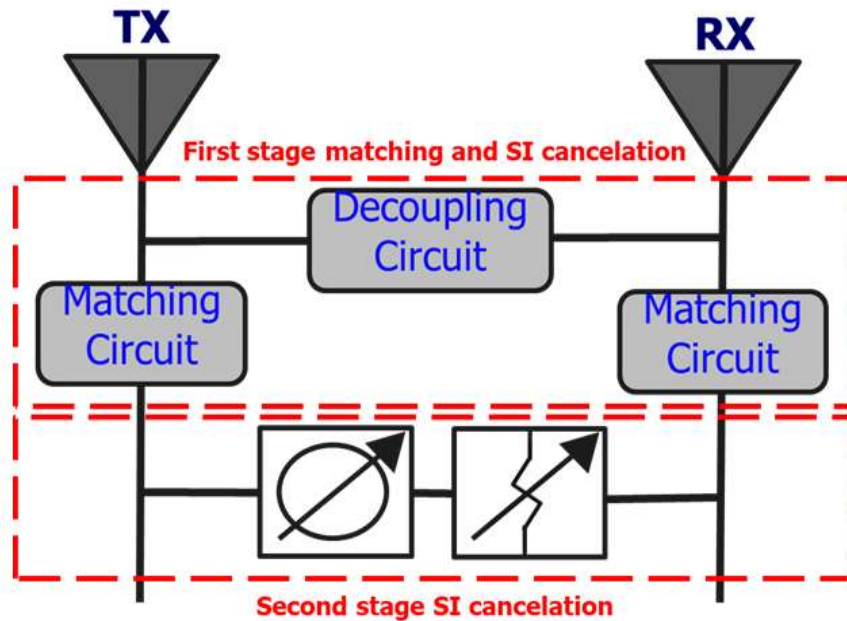


Figure 1.13 topology to reduce SI in a compact FD front-end

1.10 Organization of the Thesis

In this chapter, a brief introduction of FD, covering up the SI issues between TX chain and RX chain have been proposed. SI cancellation are usually organized following three levels and existing Antenna/RF/analog SI cancellation techniques (i.e. the first two analog SIC levels) have been detailed, compared and discussed prior introducing a new topology based on non-Foster circuits.

The fundamental characteristics of Non-foster circuits will be addressed in Chapter 2, where a literature review on non-Foster, the used topologies, and the main stability issues are all covered.

Chapter 3 will deal with the design of a variable phase shifter that is going to be used inside the second stage of FD topology in order to provide a complementary SI cancellation level. NF circuit stability will be thoroughly studied. In addition, we will discuss the difficulties in working with NF circuit due to the parasitic components and will bring and try some ideas to get rid of the main undesired parts.

In Chapter 4, the concept of ESA will be addressed, covering up the quality factor and Gain bandwidth limitation of antenna when using passive element, and how to overcome that limitation when using NF circuit. In addition, a method to decrease the quality factor and increasing the matching bandwidth by using combinations of both passive and Non-Foster elements will be carried out in order to achieve a wide bandwidth matching at low frequency (around 1.6 GHz) and a high efficiency gain. Moreover, a decoupling circuit is also introduced in order to achieve the first level of SI cancellation between the Transceiver and receiver, finishing up with a complete FD system by combining the two SI cancellation stages with two monopole antennas.

Chapter 5 will present the main conclusions of the thesis together with some perspectives and the future work.

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Chapter 2

Non-Foster Reactive Elements

In this chapter, we introduce an overall view about Non-Foster elements, where the basics idea on how to achieve a Non-Foster response is addressed, which include some of the famous topologies that are used to build a Non-Foster circuit. In addition, the overall stability study on Non-Foster is also discussed. This chapter will set the stage for Chapter 3 where Non-Foster circuit is used to designing a tuneable phase shifter.

2.1 Introduction to Foster and Non-Foster elements

In 1924, Ronald M. Foster came up with a theorem, that pointed out that the frequency derivatives of the reactance X and the susceptance B of a component are positive [1], which relates to the total stored energy in that element and is therefore positive [2]. In other words, the slope versus frequency of the reactance or the susceptance will be positive as seen in the following equations:

$$\frac{\partial X}{\partial \omega} > 0 \quad \text{and} \quad \frac{\partial B}{\partial \omega} > 0 \quad (2.1)$$

Figure 2.1 shows the reactance or susceptance curve of a Foster element versus frequency. Since the frequency derivatives of the reactance and the susceptance are positive, the reflection coefficient (Γ) of Foster elements (positive inductor and/or capacitor) rotates in the clockwise (CW) direction on the Smith chart when increasing frequency as seen in Figure 2.2. On the other hand, what makes NF elements so special is that they generate energy rather than consuming it, which makes the frequency derivative of the reactance (or the susceptance) negative where on Smith chart the reflection coefficient of NF elements (negative inductor and/or capacitor) rotates in the counter-clockwise (CCW) direction and satisfy the following equation:

$$\frac{\partial X}{\partial \omega} < 0 \quad \text{and} \quad \frac{\partial B}{\partial \omega} < 0 \quad (2.2)$$

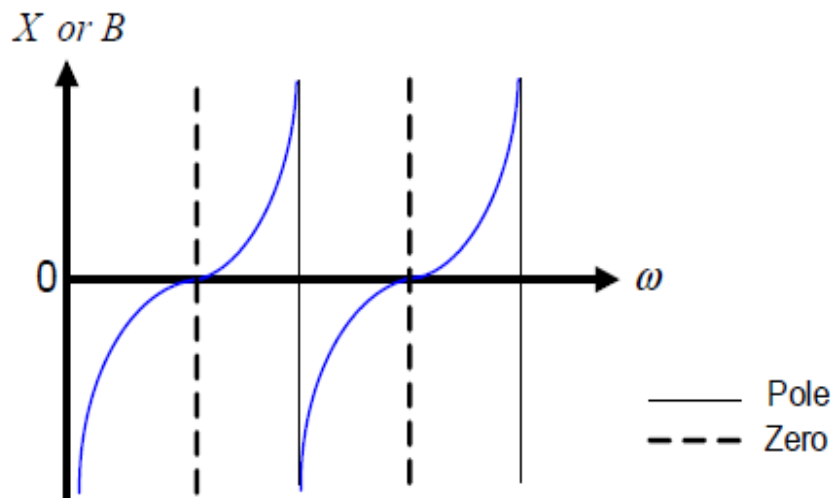


Figure 2.1 Reactance or susceptance of Foster element along frequency axis

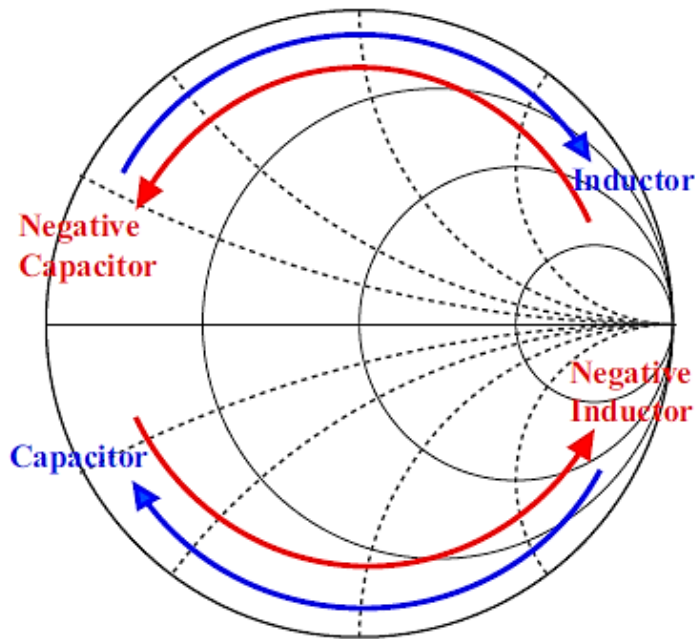


Figure 2.2 Reflection coefficient of Foster and NF elements on Smith chart

Negative inductors and negative capacitors do not exist in nature, and therefore they must be generated using active circuits, such as transistors or, less commonly used, Resonant-Tunnelling Diodes (RTD) [3]. The first type of Non-Foster circuit topology relies on a NIC (Negative Impedance Converter) introduced by Merrill in 1951 [4], which was built using vacuum tubes. The initial aim was to construct negative impedance repeater in the purpose of cancelling the transmission resistor on the telephone line. Then, Linvill built the first NIC using transistors in 1953 [5]. Linvill also designed many other versions of both balanced and unbalanced NIC. He also considered the stability conditions of the NIC. Additional circuits were realized by Yanagisawa [6] and Larky [7]. It is worth mentioning that there have been many proposed NIC topologies [8], [9], but few of them have been implemented in practice, as stable prototypes, which confirms the difficulty in building this kind of circuits.

Due to the negative frequency slope provided by NF reactance, NIC can be used to completely cancel reactance over a wide frequency range. Therefore, NIC can be used for many purposes such as: impedance matching [13], cancelling the phase delay of a circuit that results in reduced phase dispersion [17], it can be used as a capacitance multiplier in the design of integrated low-pass filters [18], it can be applied to increase the temperature sensitivity in a bridge sensor [19]. In addition, NIC can be loaded on a transmission line to realize a non-dispersive fast-wave transmission line [20], which is used to build a squint-free leaky wave antennas [21] and true time delay components in squint-free arrays [22].

2.3 NIC and NII basics

NF elements can be implemented by two groups of circuits called Negative Impedance Converters (NICs) and Negative Impedance Inverters (NIIs). As seen in Figure 2.3, NIC is a two-port network terminated at one port by an impedance, and the other port presents the negative value of that impedance multiplied by a scaling factor. The principle of operation of a NIC, configured in one of the earlier topologies by using two cross-coupled Bipolar Junction Transistors (BJT), is shown in Figure 2.4. The red arrows showing voltage flow and blue arrows showing Current flow generate an impedance $Z_{NIC} = -|K|Z_L$ as seen across source terminals. This phenomenon is possible due to a voltage inversion at the load impedance (Z_L)

terminals. On the other hand, NII is also a two-port network terminated at one port by an impedance, but by looking at the other port we will see the inverse of the impedance with a negative scaling factor. For example, if the load impedance was a capacitor, then at the other port we will have a negative inductor.

NIC and NII can be represented using [ABCD] matrix as shown in Table 2.1, and satisfying the following conditions of ($k_1k_2 < 0$ and $G_1G_2 < 0$). In addition, depending on the sign of k_1 and k_2 , NIC can change either the direction of the load current hence called current inversion NIC (INIC) or change the polarity of the load voltage hence called voltage inversion NIC (VNIC). The same thing is also applied for NII.

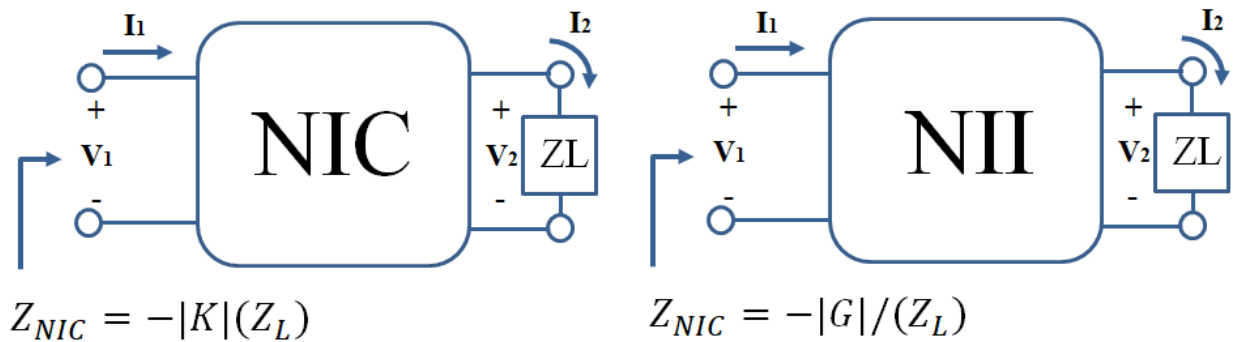


Figure 2.3 Scheme of NIC (a), and NII (b) two-port networks

TABLE 2.1 IMPEDANCE CONVERTER AND INVERTER PARAMETERS

Conversion Type	[ABCD] parameters
Impedance Converter	$\begin{bmatrix} k_1 & 0 \\ 0 & k_2 \end{bmatrix}$
Impedance Inverter	$\begin{bmatrix} 0 & 1/G_1 \\ G_2 & 0 \end{bmatrix}$

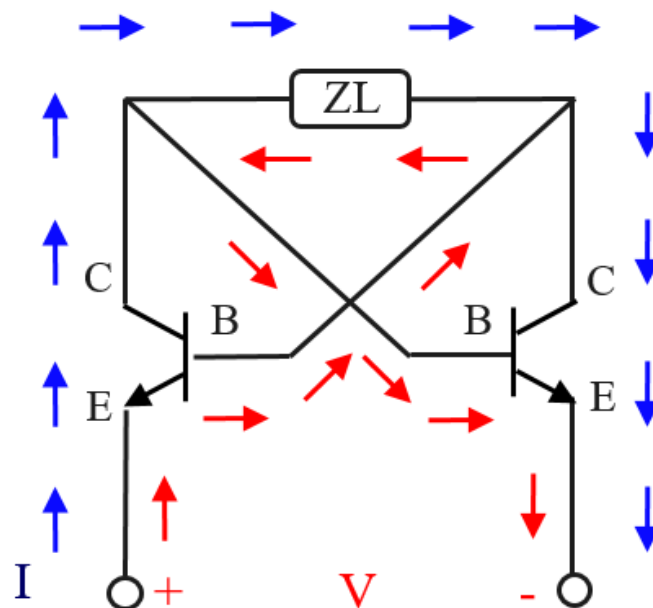


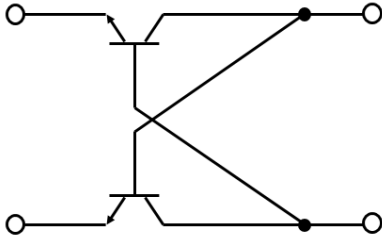
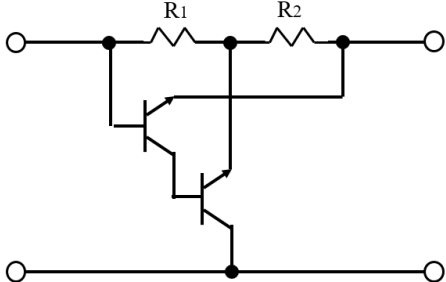
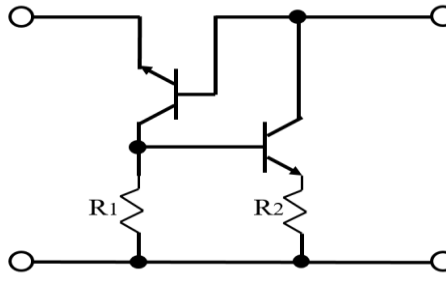
Figure 2.4 Basic NIC topology showing Voltage flow (red arrows) and Current flow (blue arrows)

2.4 Topologies of NIC

NIC can be constructed using different topologies. Table 2.2, shows some of these topologies. A few comments regarding the design and of these circuits are given below:

- These circuits can be designed using either PNP or NPN bipolar transistors.
- All NIC are unbalanced topologies (i.e., the input and output ports have a common terminal), except for the Linvill topology which is a balanced one.
- NIC circuits can be used as either open-circuit stable (OCS) at one port or as short-circuit stable (SCS) at the other port [10].
- All NICs shown in Table 2.2 are build using two transistors and two resistors, except for the Linvill's cross-coupled topology, which uses only transistors.
- All NICs perform differently in terms of noise, stability, non-linear behavior and sensitivity. For example, in [11] a sensitivity comparison was carried out between two classes of NICs.

Table 2.2 Collection of NIC topologies

Done by:	NIC Topology
Linvill (1953) [12]	
Larky(1956)[13]	
Yanagisawa(1957)[14]	

Sandberg(1960) [15]	
Myers(1965)[16]	

2.5 Other Non-Foster topologies

Asides from the use of transistors and the Linvill's schematic to realize NF elements, there are other means of realizing these elements, in the upcoming subsections we present four different topologies for achieving a NF element.

2.5.1 NIC Based on Amplifiers

Harris et al. in 1968 propose the use of multiple amplifiers for realizing an NIC [12]. Based on a concept of voltage inversion NIC with a voltage gain (A_V) of 2, as seen in Figure 2.5, the Feedback lines connect the two terminals of the impedance to invert with the input terminals of the amplifier, When A_V , the amplifier gain is equal to 2, and the input impedance can be $-Z_L$. However, since the gain of the amplifier cannot be steady this will limits the performance of the NIC at high frequencies. The equation of this NIC is given below:

$$V_1 = I_1 Z_L + A_V V_1 \quad (2.3)$$

From equation (2.3), we can calculate the input impedance (Z_{in}) as follows:

$$Z_{in} = \frac{V_1}{I_1} = \frac{Z_L}{1 - A_V} \quad (2.4)$$

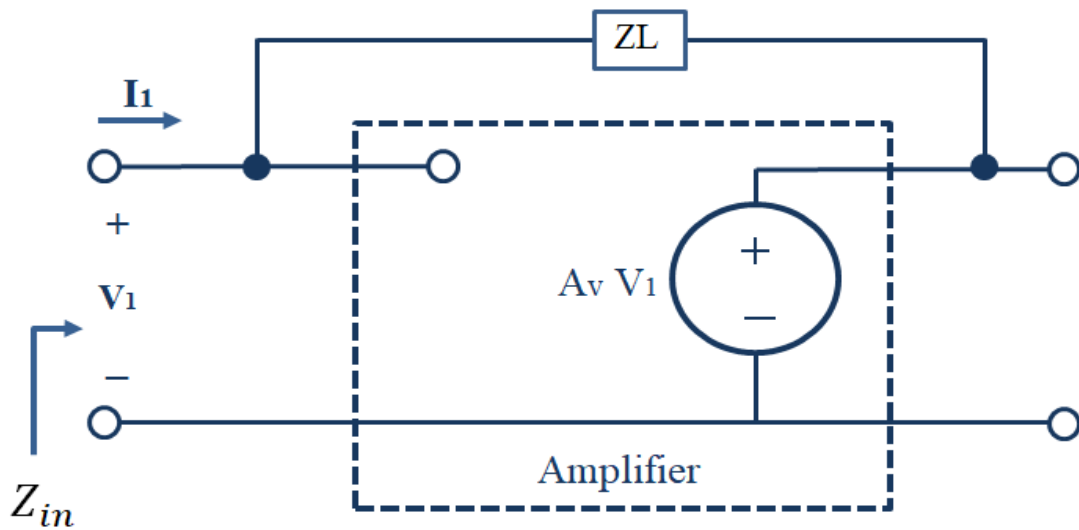


Figure 2.5 Amplifier based NIC

2.5.2 NIC Based on a Transformer

Reference [13] also proposes another schematic for achieving an NIC. A transformer is used to achieve the phase inversion needed that produces the impedance converter. The value of the negative impedance is dependent on the turning ratio of the transformer (Appendix A). Figure 2.6 shows the NIC based on a transformer.

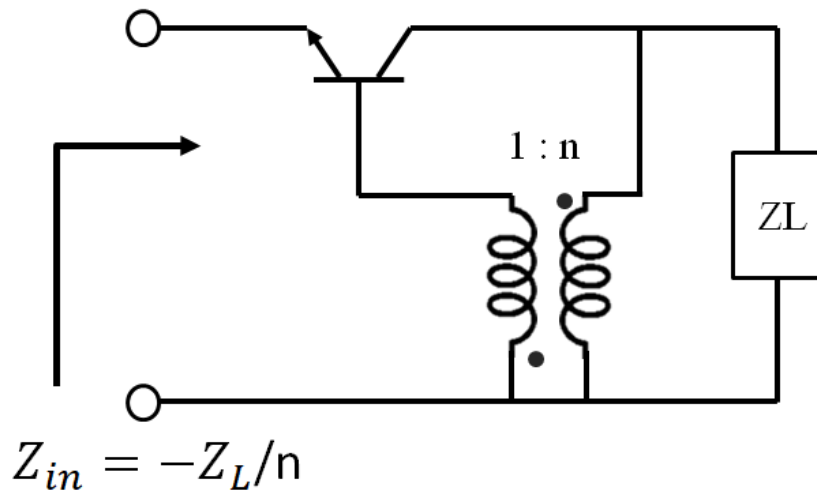


Figure 2.6 Transformer based NIC

2.5.3 Non-Foster circuits Based on a Negative Group Delay NGD

This method introduces a new view in realizing NF elements based on wave propagation theory. In addition, this configuration solves the electrical stability problems of the traditional designs. This method compares between NF elements and NGD networks, and shows that both share the same influence on propagating waves [14]. In general, the group delay in propagation τ_D can be determined by examining the phase response ϕ of a network using the following equation:

$$\tau_D = -\frac{\partial \phi}{\partial \omega} \quad (2.5)$$

According to this equation, the group delay of NGD is equivalent to an increasing phase response with frequency, which is the same behaviour of NF. NGD networks can be designed using series and parallel RLC resonators operating around their resonance frequencies as shown on Figure 2.7. However, NGD suffers from losses due to the use of resistive elements. In fact, losses in NGD can be compensated by the use of transistors [15].

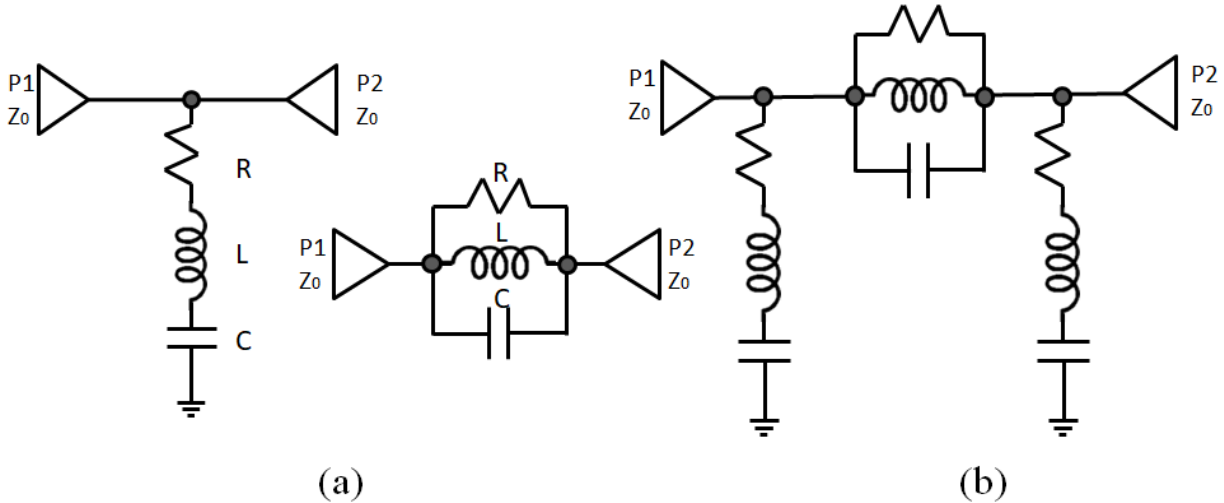


Figure 2.7 (a) Series and parallel RLC resonators used for optioning NGD. (b) Combination of series and parallel RLC resonators for wideband NGD response

2.5.4 Non-Fosters Based on Distributed Amplifier

An unconditionally stable NIC circuit can also be built using two-stage microwave distributed amplifier that is based on negative group delay. The NGD circuit is built by using two stage distributed amplifier based on microwave transversal-filters. The trans-conductance of each stage can be adjusted by tuning its gate voltage, and the input/output phase responses can be tuned by two varactors, thus realizing tuneable NF characteristics between its reverse port (P2) and input port (P1), as shown in Figure 2.8. This topology provides good input and output impedance matching and can offer an unconditional stability[16].

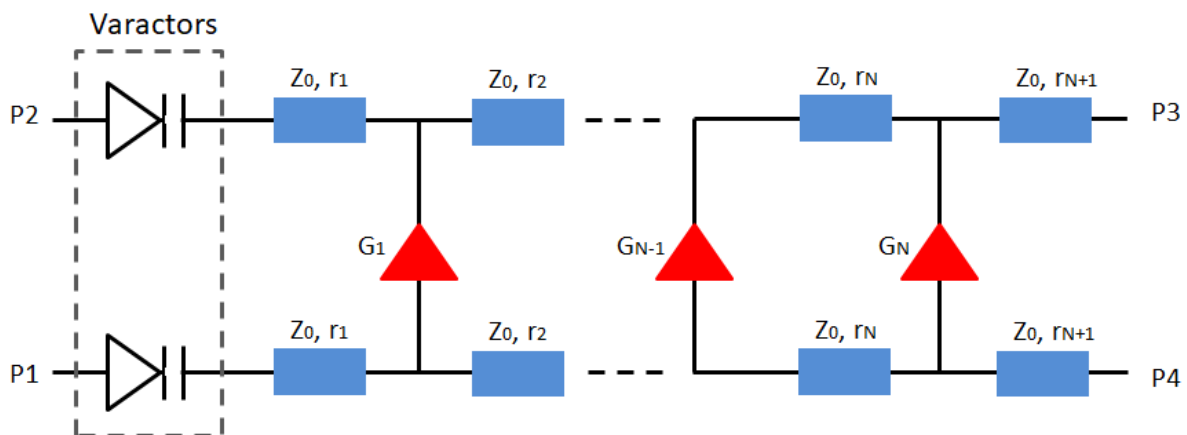


Figure 2.8 Schematic of tuneable negative capacitor using NGD circuit based on distributed amplifier

2.7 NICs chosen circuit

We have chosen Linvill's balanced Open Circuit Stable (OCS) NIC composed of two BJTs as a circuit to achieve NF element Figure 2.9, shows the small signal π -model for a BJT. Without neglecting both addressed r_{π} the internal capacitances (C_{π} in the BJT or C_{gs} in the FET). Figure 2.10, shows the circuit of OCS. Two cases have been taken as a study: r_o is infinite (1), and r_o is finite (2).

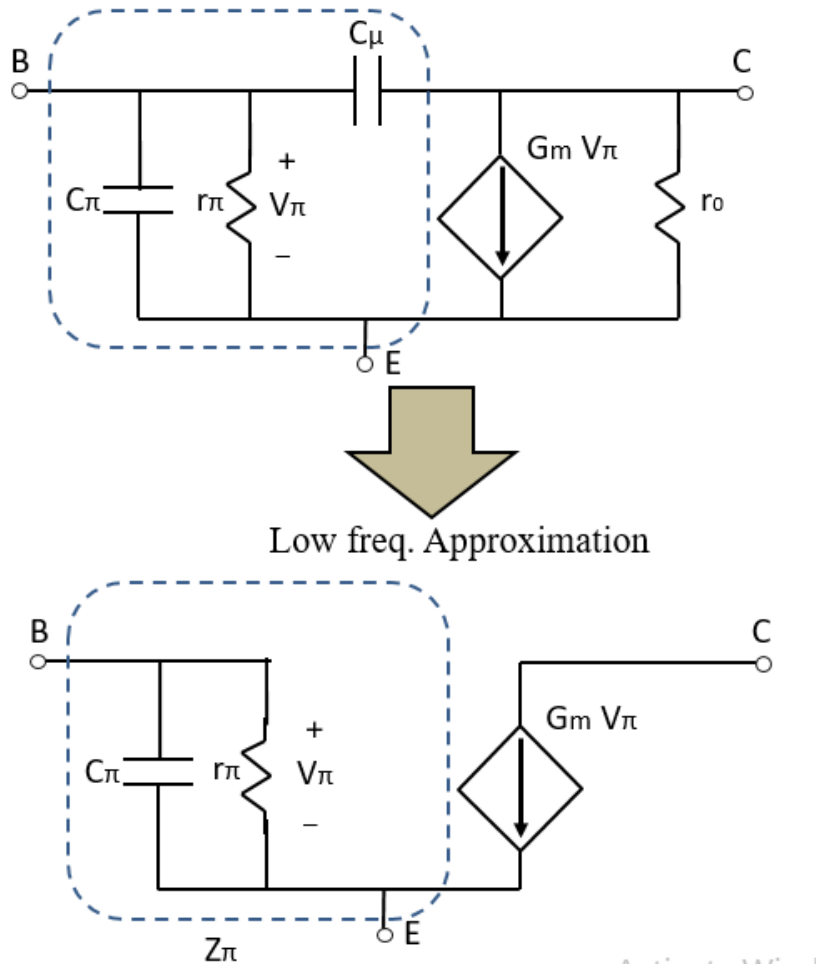


Figure 2.9 Small signal π -model representation of BJT transistor

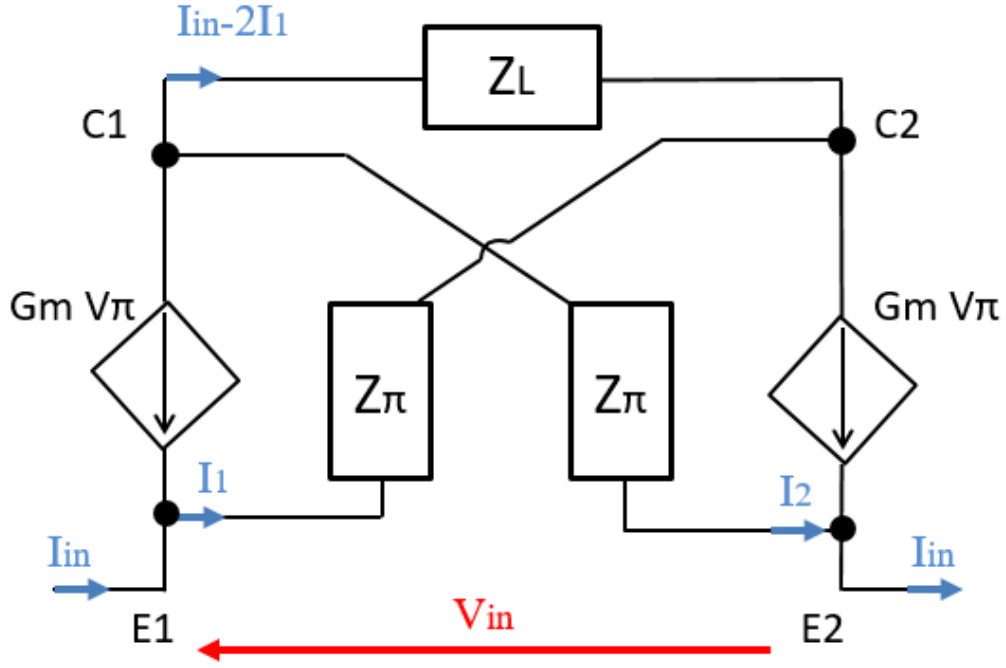


Figure 2.10 NIC Open Circuit Stable (OCS) topology

2.7.1 Case r_0 infinite:

After replacing each BJT with the small signal model, we can then calculate the input impedance of the circuit as given below:

$$V_{in} = V_{E1C2} + V_{C2C1} + V_{C1E2} \quad (2.6)$$

Since the topology is symmetrical, then equation (2.6) can be simplified as:

$$V_{in} = V_{C2C1} + 2 * V_{C1E2} \quad (2.7)$$

Where V_{C2C1} is calculated as:

$$V_{C2C1} = -Z_L * (I_{in} - 2 * I_2) \quad (2.8)$$

Moreover, I_2 is given by:

$$I_2 = I_{in} - g_m V_{\pi} \quad (2.9)$$

In addition, V_{π} is given by:

$$V_{\pi} = Z_{\pi} * I_2 \quad (2.10)$$

Replacing (2.10) in (2.9) we will get:

$$I_2 = \frac{I_{in}}{(1 + g_m Z_{\pi})} \quad (2.11)$$

Replacing (2.11) in (2.8) and adding it to (2.7) we can calculate the input impedance as follows:

$$Z_{in} = Z_L \left(\frac{2}{1 + g_m Z_{\pi}} - 1 \right) + \frac{2 * Z_{\pi}}{1 + g_m Z_{\pi}} \quad (2.12)$$

Moreover, for low frequency approximations ($r\pi \gg 1$ and $gm \gg Z\pi$), (2.12) can be approximated by:

$$Z_{in} \approx -Z_L + \frac{2}{gm} \quad (2.13)$$

It can be noticed from equation (2.13) that using an ideal transistor the impedance converter coefficient is unity. The second part of equation (2.13) is defined as parasitic element due to the non-ideal transistors.

2.7.2 Case r_0 is finite

Figure 2.11 represents OCS circuit after considering r_0 as finite value, according to it, we can calculate the input impedance as follows:

$$V_{C1E1} = -r_0(I_{in} - I_1 + gmV_{B1E1}) \quad (2.14)$$

Where V_{C1E1} is given as:

$$V_{C1E1} = -r_0(I_{in} + V_{B1E1}(Z_\pi + gm)) \quad (2.15)$$

Moreover, V_{C2E2} can be calculated as follows:

$$V_{C2E2} = r_0(I_{in} - V_{B2E2}(Z_\pi + gm)) \quad (2.16)$$

V_{B1E1} is given as:

$$V_{B1E1} = V_{C1E1} - V_{C1C2} \quad (2.17)$$

Moreover, due to symmetry we have:

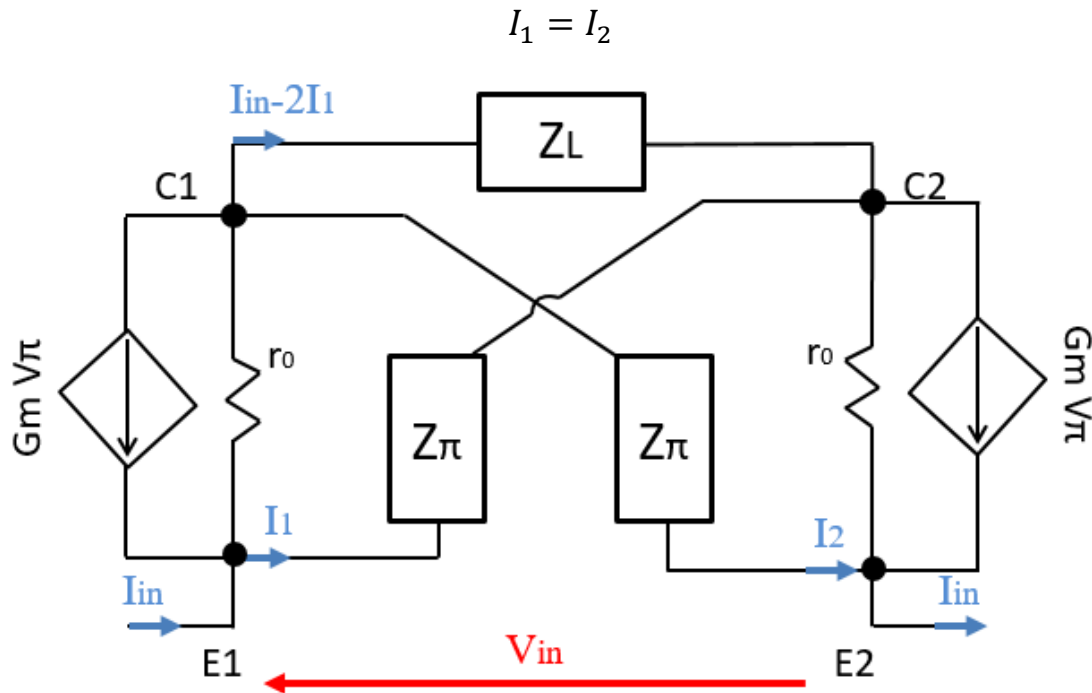


Figure 2.11 NIC Open Circuit Stable (OCS) topology where r_0 is Finite

From that, we express V_{B1E1} and V_{B2E2} as follows:

$$V_{B1E1} = \frac{V_{C1E1} - Z_L * I_{in}}{1 + 2Z_L Z_\pi} \quad (2.18)$$

$$V_{B2E2} = \frac{V_{C2E2} + Z_L * I_{in}}{1 + 2Z_L Z_\pi} \quad (2.19)$$

Replacing (2.18), (2.19) in (2.15) and (2.16) respectively, we get:

$$V_{C1E1} = \frac{-r_0 * I_{in} \left(1 - \frac{Z_L * (gm + Z_\pi)}{1 + 2Z_L Z_\pi}\right)}{1 + \frac{r_0 * (gm + Z_\pi)}{1 + 2Z_L Z_\pi}} \quad (2.20)$$

$$V_{C2E2} = \frac{r_0 * I_{in} \left(1 - \frac{Z_L * (gm + Z_\pi)}{1 + 2Z_L Z_\pi}\right)}{1 + \frac{r_0 * (gm + Z_\pi)}{1 + 2Z_L Z_\pi}} \quad (2.21)$$

The input voltage is given as:

$$V_{in} = V_{C1C2} + V_{C2E2} - V_{C1E1} \quad (2.22)$$

For simplicity of equations, we are going to assign the following variables as follows:

$$A = gm + Z_\pi, B = 1 + 2Z_L Z_\pi, \text{ and } C = 1 + \frac{r_0 * A}{B}$$

Substituting (2.20) and (2.21) in (2.22) we can calculate the input impedance as:

$$Z_{in} = \frac{2 * r_0}{C} + Z_L * \left(1 - \frac{2 * r_0}{C} \left[\frac{Z_\pi}{C} + \frac{A}{B}\right]\right) + \frac{2Z_L^2 Z_\pi}{C} \left[\frac{A * r_0}{B * C} - 1\right] \quad (2.23)$$

For low frequency approximations ($r\pi \gg 1$, $r_0 \gg 1$, and $gm \gg Z_\pi$), thus, the variables can be approximated by:

$$A = gm, B = 1 \text{ and } C = 1 + gm * r_0$$

Which finally gives the same simplified approximation of the input impedance as in the previous case.

$$Z_{in} \approx -Z_L + \frac{2}{gm} \quad (2.24)$$

2.8 Stability within NICs

The cross-coupled transistor topology of the NIC circuit has a positive feedback network in order to generate negative impedances. This leads to stability issues, unless we properly load the NIC with appropriate impedance to ensure the circuit's stability. This last sentence is explained by Linvill stability analysis, which was carried out on the equivalent circuit model of the BJT.

He first separates the analysis of the balanced topology and presents it in two cases [5]. His study can be simplified as follows: first, if the input to the NIC is at the emitter of the transistor, then the NIC will be considered as an open circuit stable (OCS) by making sure that the NIC sees an open circuit at its input. Second, if the input to the NIC is at the base-collector junction, then the NIC will be considered as a short circuit stable (SCS) by making

sure that the NIC sees a short circuit at its input as depicted in Figure 2.12. In addition, stability for the OCS can be achieved (i.e., the input impedance Z_{NIC} poles are all in the Left Half-Plane (LHP)) if the value of the impedance at the left side of the reference plane (Z_s), satisfies the following condition for all frequencies.

$$|Z_s| \geq |Z_{NIC}| \text{ or } |Y_s| \leq |Y_{NIC}| \text{ OCS port} \quad (2.25)$$

Likewise, for the short-circuit stability, a necessary condition for the NIC to be stable (i.e., the input impedance, Z_{NIC} has no poles in the RHP) is that the absolute value of the admittance at the reference plane (Z_s) should satisfy the following condition for all frequencies.

$$|Z_s| \leq |Z_{NIC}| \text{ or } |Y_s| \geq |Y_{NIC}| \text{ SCS port} \quad (2.26)$$

Figure 2.13 demonstrates the stability conditions. Thus, care must be taken to ensure that the impedance conditions are satisfied throughout the bandwidth of operation of the NIC.

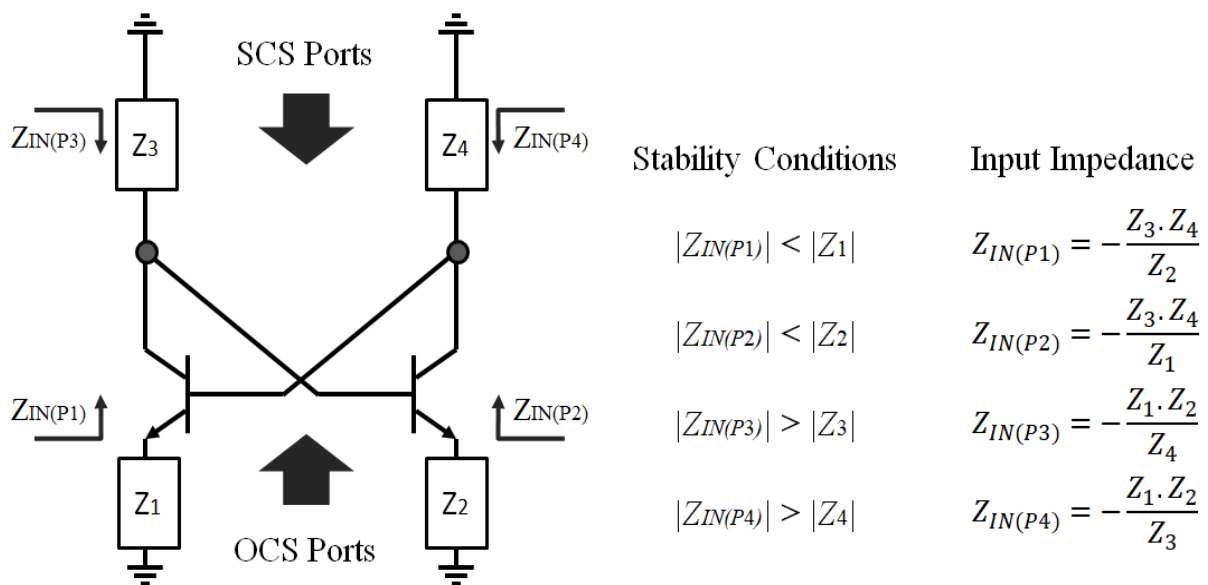


Figure 2.12 General topology of NIC with stability conditions

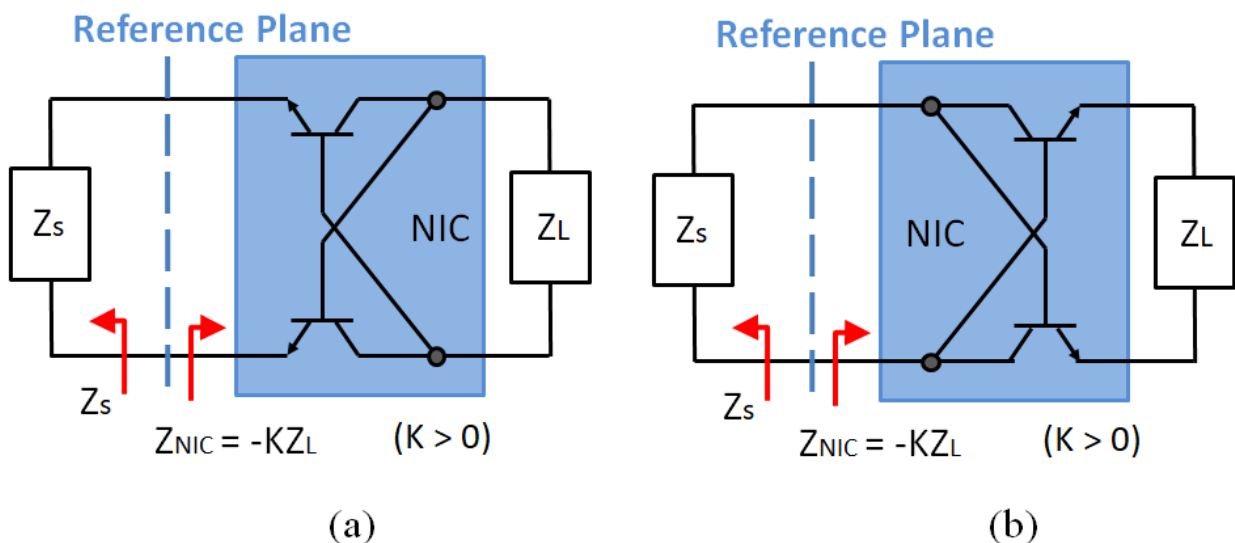


Figure 2.13 Ideal NIC diagram presenting reference plan for (a) open-circuit and (b) short-circuit stability condition

2.9 Linvill Analysis Limitation

Linvill analysis suffers from two drawbacks, first, the analysis on OCS or SCS does not take into consideration important factors, for instance, the reactive nature of the NIC load, or the dispersion of the circuit components with frequency. Because of these reasons, the OCS-SCS validation is a necessary but non-sufficient condition for the system stability, which means that instabilities and oscillations may still be observed in practice. Number of reported works dealing with the circuit stability can be found in reference [10], [23]. These methods are all based on the Nyquist stability criterion [24] to check if the network function does not have any poles in the RHP (Right Half-Plane) of the s-plane. One of the conventional parameters to evaluate the stability of the circuit is Rollet K [25], or μ factor [26]. These parameters are function of two port network related to the S-parameters (but also can be applied with z, g, y or h-parameters) which search for unconditional stability by making sure that the input/output impedances of the system are positive real. The K and μ factors depend on which port the analysis is carried out.

The K factor, proposed in [25], is a dimensionless quantity that must be greater than 1 at all frequencies for the system to be stable, and it can be computed as follows:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta_s|^2}{2|S_{12}||S_{21}|} \quad (2.27)$$

And the second condition is that:

$$\Delta_s = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad (2.28)$$

Recently these two conditions have been grouped into one parameter μ , which must be >1 for the system to be stable, and is defined as follows:

$$\mu = \frac{1 - |S_{11}|}{|S_{22} - \Delta_s S_{11}^*| + |S_{21}S_{12}|} \quad (2.29)$$

The main drawback of these parameters is the fact that they ignore characteristics of more complex elements, as they are based on characterized devices (e.g. transistors) known to be stable under special measurement equipment [27]. These criteria could fail because of the use of a reduced two-port version for predicting stability of an N-node network, ignoring some of the possible poles in the RHP of the system. Those tests (Rollet factor K or μ) are only valid if another condition (a proviso) is already satisfied. That proviso includes the evaluation of all the possibly hidden poles of the whole system, including those from the active devices, by evaluating the stability of the respective well-terminated model (e.g. S-parameters terminated at Z_0 , or Z-parameters terminated in opens) of each component in the system.

In the early years of microwave circuits design, the proviso has often been ignored because it is not an easily calculated parameter, moreover because it was not been a problem for circuits with only a single active device (e.g. single stage amplifiers) [27]. This is acceptable if the S-parameters used in the analysis come from measurements and the basic device (the transistor) is known to be stable. This is not always the case of a NF circuit [27], [28].

As the limitations of the K and μ factors have been stated, in addition to that, testing every node in the circuit for instability is a valid approach. However, therein lays a problem. Large circuits possess complex patterns of poles and zeros which makes it important to select

the correct nodes for testing to avoid numerical errors. Other method is to test the properties of the entire circuit matrix rather than the properties of specific nodes. If there are oscillations, there must be zeroes in the Right Half-Plane (RHP). This method is not efficient because the matrix can be very large. Alternative method to study the stability of the circuit is to use Normalized Determinant Function NDF that was first devised by Platzker and al. in [29]. The NDF is defined as the ratio of Δ_s/Δ_{s_0} , where Δ_{s_0} is the network determinant when all active devices are turned off [30]. Since Δ_{s_0} is the determinant of a passive network, it has no RHP zeros thus, it does not offer any poles to NDF at RHP. NDF can also be given as in the following equation.

$$NDF(s) = \frac{|Y(s)|}{|Y_0(s)|} = \frac{\Delta_s}{\Delta_{s_0}} \quad (2.3)$$

Where $|Y(s)|$ is the determinant of the system, and $|Y_0(s)|$ is the determinant of the same circuit but with all the dependent generators (i.e., active elements in the NIC) switched off. We can determine the number of zeros of the NDF in the RHP as the number of encirclements of the NDF around the origin in the complex plot. The system will be stable if the NDF does not encircle the origin when it is evaluated from $\omega = -\infty$ to $\omega = +\infty$ [29]. For our NIC circuit we will use NDF method to study its stability.

2.10 Conclusion

Non-Foster circuit can be used in many applications due to its unnatural reactance behaviour vs frequency, NF can be achieved using different kinds of topologies, the famous one is called Linvill negative impedance converter, which is designed using two transistors, and can be used either as open circuit stable looking at one port of NIC or as short circuit stable by looking at the other port of NIC. Unfortunately this topology suffers from instability issues which limit its performance unless it is carefully loaded with a well dedicated impedance following the stability conditions which was studied by Linvill. Moreover, it was noted that these conditions are not enough to ensure stability of the circuit, and thus we have to perform another stability study on the circuit to ensure its stability. Indeed, it was noted that Rollet factor K and μ do not fully state that the circuit is stable, therefore an alternative stability method named normalized determinate function is used which is more confidential than K or μ when it comes on testing the stability.

Through this part of the thesis, we are going to use NDF to study if our NIC circuit is stable or not. The next chapter is going to address the design of a variable phase shifter that is build using NIC circuit and the stability issues of this circuit were also been studied.

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Chapter 3

Active Tunable Phase Shifter

As introduced in Chapter 1, a phase shifter is needed in the proposed full-duplex topology. Indeed, this topology requires a 180° phase shifter (or phase inverter) with a slight tunability around that phase value. Moreover, this phase shifter is expected to exhibit a frequency independent phase shift (or flat phase in transmission) from 1 GHz to 4 GHz (where many IoT systems operate in this frequency band) over the tuning range.

To get these characteristics, we will use non-Foster circuits to design a tunable wideband phase shifter. This chapter will focus on both: the design of the non-Foster circuits and the phase shifter.

The chapter is organized as follow: first, PS definition will be recalled, and then we will describe the main types of PS, and identify applications that can benefit from PS. Later, the 1st design of a PS is presented with a discussion of the stability study that has been carried out on our proposed topology, after that a design of a stable Non-foster circuit is carried out, finishing up with final design and implementation of stable PSs. The experimental results of these circuits are analyzed and discussed before concluding and giving some perspectives on PS.

3.1 Phase Shifter

Phase Shifters (PSs) [1], [2] are among the most demanded, studied and commonly used electronic RF circuits in the radio transmitter and receiver chain. They are essentially used in phased array antennas [6] to achieve electronic beam steering by controlling the phase signal delivered to radiating array elements.

One other important application of the phase shifter is in a digital PLL [5], where PS are used to remove phase and/or frequency error from a received signal. They are also utilized extensively in phase modulators, microwave measurement systems and instrumentation, microwave frequency translators [7] and many other applications.

Moreover, the rapid growth of the communication systems toward the fifth-generation (5G technology) requires, among other components, wideband or multiband PSs that cover the required bandwidth while having the possibility to control its phase shift when needed (e.g. beamforming, image rejection mixers, tunable channelized filters, etc..).

Among wideband PS topologies, phase-inverters are particularly highly demanded devices and can be implemented by using 180-degree Balun or by signal-to-ground inversion [3], [4]. They can potentially be designed to feature multiple frequency bands as well as Ultra-Wide-Band (UWB) performance. However, these wideband inverters do not offer the possibility of phase adjustment while keeping wide band behavior.

A Phase Shifter is simply a two-port device that changes the phase of any incoming RF signal with a level of attenuation as low as possible. A two-port phase shifter is shown in Figure 3.1. Assuming the phase shifter is ideal (i.e. lossless), for an input signal V_1 at port 1 and for a shifted phase Φ , then the output signal at port 2 will be given as $V_1 e^{j\Phi}$.

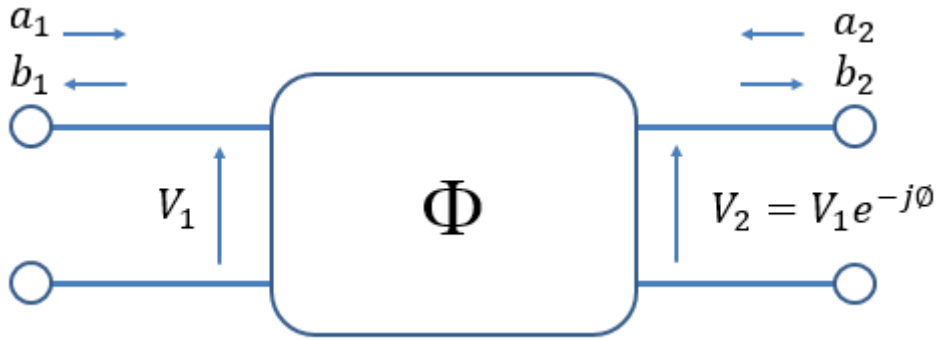


Figure 3.1 Two-port network schematic of a phase shifter

An ideal reciprocal two-port phase shifter's scattering matrix is depicted as follows:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} 0 & e^{-j\Phi} \\ e^{-j\Phi} & 0 \end{pmatrix} \cdot \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \quad (3.1)$$

In practical usage, phase shifters have some amount of insertion loss, which of course greatly depends on the PS type, the components used and the operating frequency. The insertion loss of the signal is obviously given as:

$$IL(dB) = 20 \log_{10} |S_{21}| \quad (3.2)$$

3.2 Types of Phase Shifters

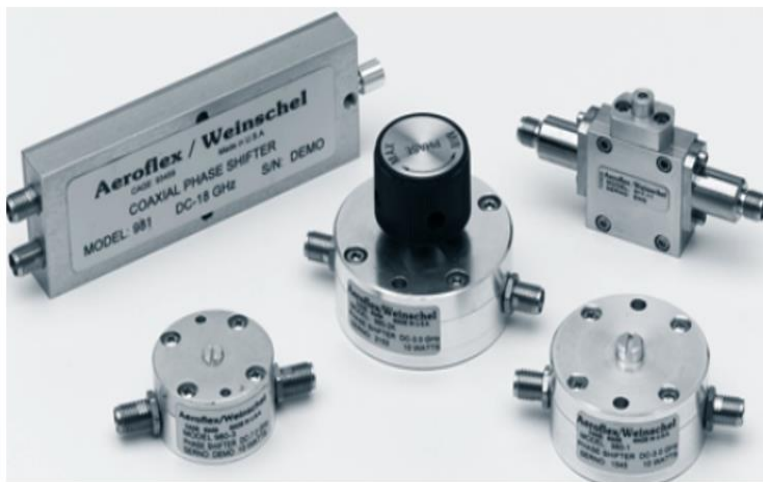
Phase shifters can be classified into several types according to their properties or designs. These classifications can be: active or passive, electronic or mechanical, digital or analog, fixed or adjustable, reciprocal or nonreciprocal etc. [5]. Other classifications can be done depending on fabrication technology or applications. Some of these different PS types are briefly explained below.

3.2.1 Active and Passive PS

Active and passive phase shifters are widely used for many applications. Passive phase shifters can exhibit large signal performance, but exhibit insertion loss [6], [7]. On the other hand, active phase shifters can provide loss compensation, while introducing potentially more non-linearity to the system [8], [9]. Varactor are often used when precise phase shifts are required, but varactors are likely to generate distortion for high level signals [10]. Recently, new designs of active PS have arisen with innovative characteristics. Sometimes called "pure phase shifters", they are able to provide a phase shift in transmission (not a differential phase shift as for common PS) that remains constant versus frequency (frequency independent) [11], [12].

3.2.2 Mechanical or Electronic Phase Shifters

Depending on the way used to introduce tunability in RF/Microwave phase shifters, they can be categorized as mechanical or electronic. “Mechanical phase shifters” are generally constructed using transmission line or waveguide structures. The phase shift is achieved by some kind of mechanical tuning, such as rotating a knob which causes the physical length of the line/guide to deviate [13]. Mechanical phase shifters are usually analog and reciprocal devices that have considerably low insertion losses but generally bulky Figure 3.2-a. They are also simple to fabricate and cheap compared to the electronic type. On the other hand, electronic phase shifters provide phase shift through an electronic command, usually by using voltage controlled networks [14] Figure 3.2-b. This feature makes the electronic phase shifters operate much faster and much precisely than mechanical ones, which give them a great advantage that explain their current more widespread use.



(a)



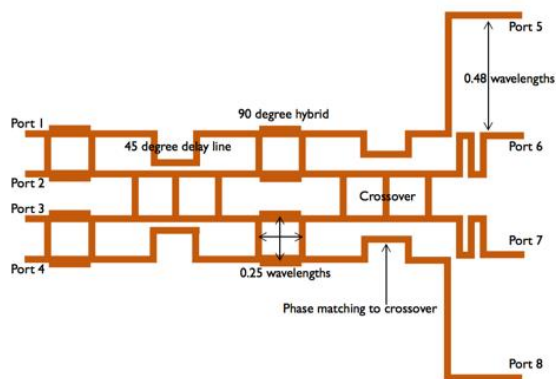
(b)

Figure 3.2 Example on Mechanical Phase Shifters [15] (a), and Electrical Phase Shifters [16]

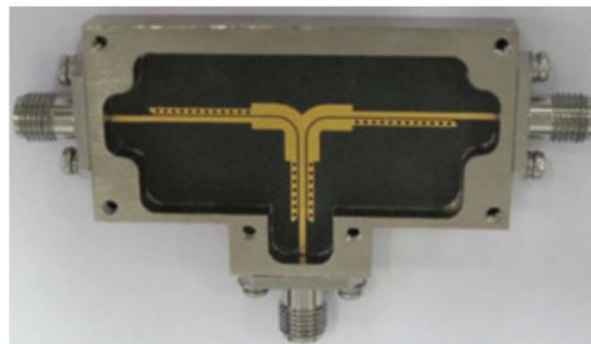
(b)

3.2.4 Fixed or Adjustable Phase Shifters

A phase shifter can be either a fixed or an adjustable one. Although an adjustable phase shifter can always be used as a fixed one, because of cost and design complexity, fixed phase shifters may be preferred in some applications such as Butler matrices [17] as seen in Figure 3.3.a. Phase inverter are a particular case among fixed PS Figure 3.3.b, they are almost systematically fixed and most researches focus on wideband behavior dedicated to systems with parallel branches and multiple ways such as out-of-phase baluns [18]. On the other hand, adjustable phase shifters are mostly used as crucial components in electronic scanning for array radars [19]. Both adjustable and fixed PS are required in applications where a fine pre-processing or during- tuning of phase shift is necessary. One should notice that fixed phase shifters are easier to design for wideband applications than tunable ones for which wideband performances are generally hard to keep over the tuning range. This remark is true for phase inverters where tunable components are particularly tricky to implement.



(a)

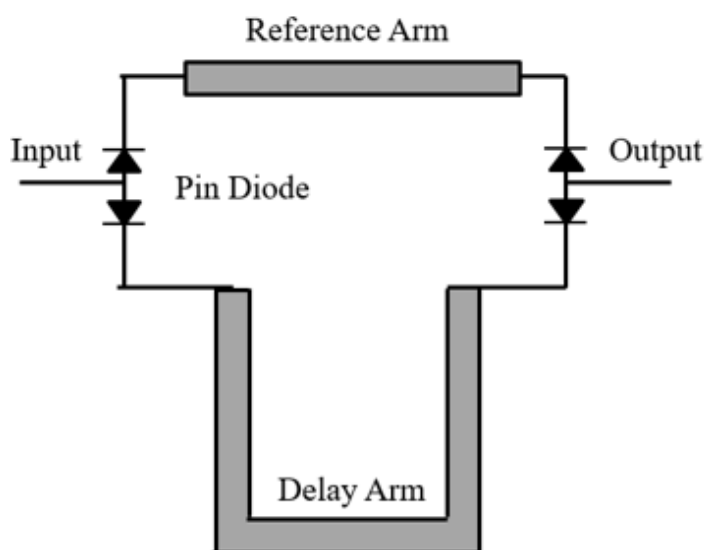


(b)

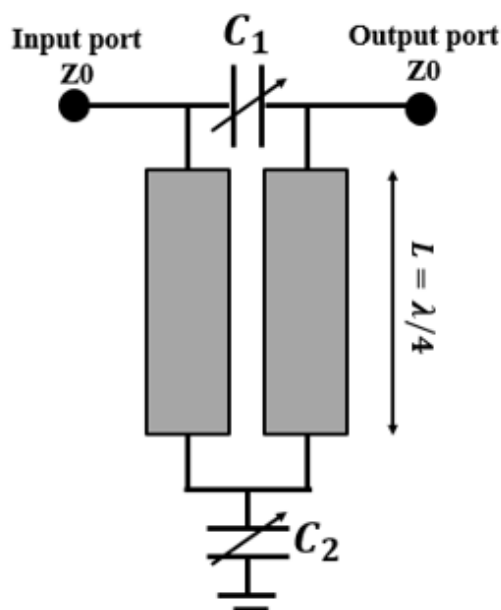
Figure 3.3 Butler matrix (a), Phase inverter (b)

3.2.3 Digital or Analog Tunable Phase Shifters

Analog phase shifters have continuously variable phase control that allows getting each and every phase value in given phase range. Analog phase shifters are usually controlled by voltage to phase transfer curve to get the desired phase shift. On the other hand, digital phase shifters can only target a specific number of phase states and cannot supply an arbitrary phase shift [2]. A truth table exists for digital phase shifters, which refer to their different phase states. An apparent disadvantage of an analog phase shifter is the sensitivity of the phase shift in case of slight variations in the control voltage. Indeed, digital phase shifters are in general less sensitive and dispersive [5]. Analog phase shifters can be realized with Varactor diodes which capacitances vary versus voltage or by using materials with properties that can be controlled electrically or magnetically [20]. Digital phase shifters are mostly realized by PIN diodes or micro-electro-mechanical systems (MEMS) that switch on or off according to the command signal [5]. Figure 3.4 shows an example of an analog phase shifter and a digital phase shifter.



(a)



(b)

Figure 3.4 Digital phase shifter (a), Analog phase shifter (b)

3.2.5 Reciprocal or Nonreciprocal Phase Shifters

Reciprocal phase shifters can be used in both directions different from non-reciprocal phase shifters, which generally offer different phase shifts for the two directions of propagation. Non-reciprocity in phase shifters is generally due to the use of active components, e.g. transistors.

3.2.6 Pure Phase Shifters

“Pure” Phase Shifters corresponds to PSs that exhibit a flat phase in transmission (contrarily to classical PSs where the phase shift difference or the relative phase shift can be flat), they are also sometimes called “frequency independent phase shifter”. “Pure” phase shifter can be implemented by using Non-Foster elements or Negative Group Delay circuits [21]. Circuits close to pure phase shifter can be used to solve Beam-squinting issue usually found in beamforming and particularly for series-fed antenna arrays. Indeed, in that case, transmission lines are required to interconnect the different antennas and Non-Foster or NGD circuits can be used to compensate the delay introduced by these lines [24]. An example of pure PS is depicted in Fig. 3.5.a. Generally, this flat phase value in transmission is obtained by cascading a transmission line by a NGD or a NF circuit that have the same phase slopes in absolute value but of opposite signs.

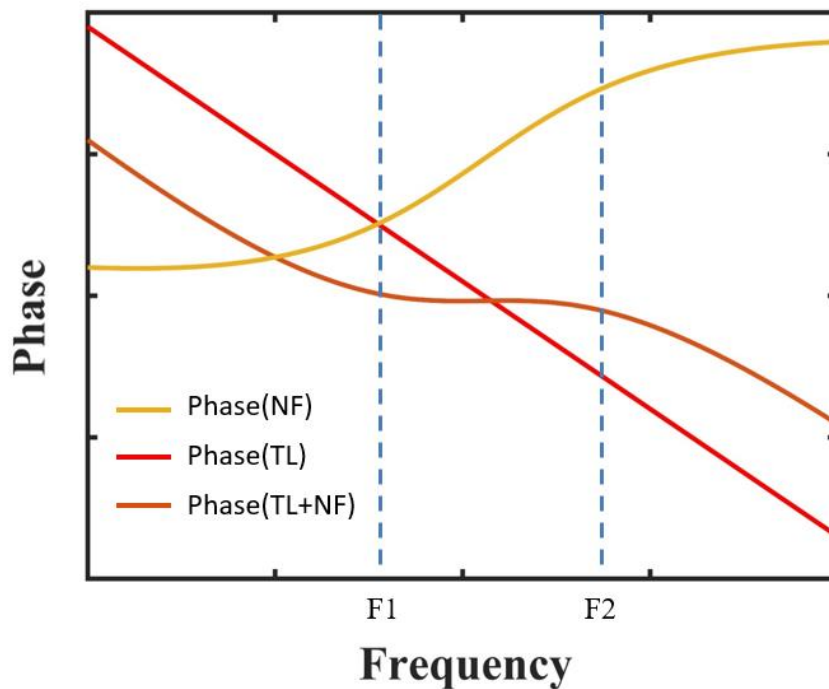
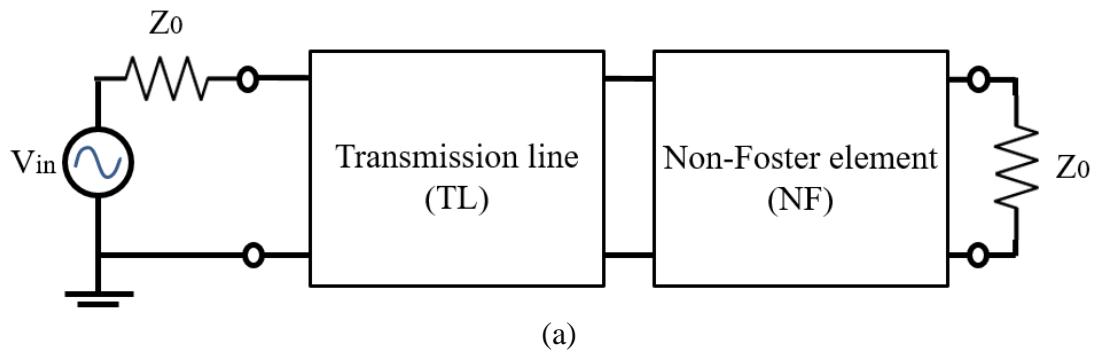


Figure 3.5 Structure of pure phase shifter: transmission line (TL) cascaded with the Non-Foster (NF) element (a), ideal behavior of their pure phase response (b)

The characteristics of pure PS seem particularly attractive for Full-Duplex application. Indeed, pure PS can be implemented between two close antennas to provide a pure inverted signal (without extra-length and with a frequency independent phase value) from the transmitter antenna to the receiver one, thus creating a null signal at the receiver part in order to provide a level of isolation between them.

3.3 1st Design of PS Tunable around 180° using NF Circuit

It's important to recall that our specifications correspond to the design of an active phase shifter tunable around 180° that exhibits a frequency independent phase shift from 1 GHz to 4 GHz. Moreover, as previously introduced, for a Full-Duplex system where TX and RX antenna are really close to each other, a pure phase shifter is preferable.

In [1], the authors present an active pure phase shifter topology that exhibits a 180° frequency independent phase shift. This PS topology is based on Non-Foster (NF) elements namely negative capacitors, which are generated using a Negative Impedance Converter (NIC) circuit [22]. Only simulation results are shown in [1], but this topology seems, a priori, promising for our Full-Duplex application.

Negative capacitors are used to get a frequency independent PS by somehow compensating for the positive capacitor of the structure. As explained in chapter II, Non-Foster components will be designed by using NIC based on FET cross-coupled pairs (XCP).

The PS topology is based on two identical capacitive Π -circuits, each consisting of two shunt capacitances (C_1) and a negative capacitance ($C_2 = -C_1$) connected in series as illustrated in Figure 3.6. Moreover, by replacing the shunt capacitances (C_1) by varactors diodes, phase tunability can be introduced around 180° while keeping the constant phase in transmission. Moreover, the analysis of the circuit stability will also be required. Compared to [1], we propose thereafter: i) to provide synthesis/design equations of the PS, ii) to make an extended parasitic influence analysis by taking into account extra components of the small signal equivalent model together with a deep study of stability, and iii) to investigate different experimental implementations.

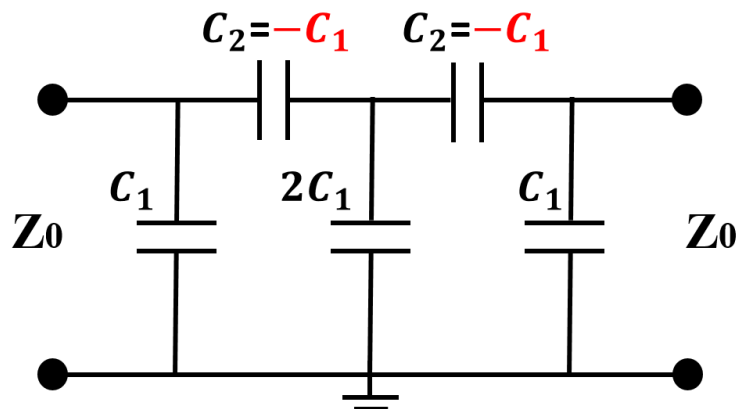


Figure 3.6 Proposed Phase Shifter Topology

3.3.1 Proposed Topology

The 2-port phase shifter circuit [1] is shown in Figure 3.6, which is made up of three shunt capacitances (C_1) and two negative capacitances ($-C_2$) connected in series and having the same absolute value. The insertion loss can be calculated as follow:

$$S_{21} = \frac{Z_{in,e} - Z_{in,o}}{(Z_{in,e} + 1)(Z_{in,o} + 1)} \quad (3.3)$$

$Z_{in,e}$ and $Z_{in,o}$ are the normalized even and odd input impedances respectively displayed in Figure 3.7-a and 3.7-b, and they are expressed as follows:

$$Z_{in,e} = \frac{C_2 - C_1}{j\omega C_1(2C_2 - C_1)Z_0} \quad (3.4)$$

$$Z_{in,o} = \frac{1}{j\omega(C_1 - C_2)Z_0} \quad (3.5)$$

As a result, we can calculate the phase of S_{21} as:

$$\theta = \text{Arctan} \left(\frac{-(C_2 - C_1)(1 + C_1(2C_2 - C_1)\omega^2 Z_0^2)}{Z_0\omega((C_2 - C_1)^2 - C_1(2C_2 - C_1))} \right) \quad (3.6)$$

Where the impedance Z_0 is equal to 50Ω . It is worth noting that this equation gives 180° of phase value in transmission only if the capacitors C_1 and C_2 have the same absolute value. Moreover, since C_1 is a passive element while $-C_2$ is an active one, it is of prime importance that C_2 perfectly fits $-C_1$ over the expected frequency range, particularly C_2 should present a zero real part while keeping a constant imaginary part, which was not done in [1].

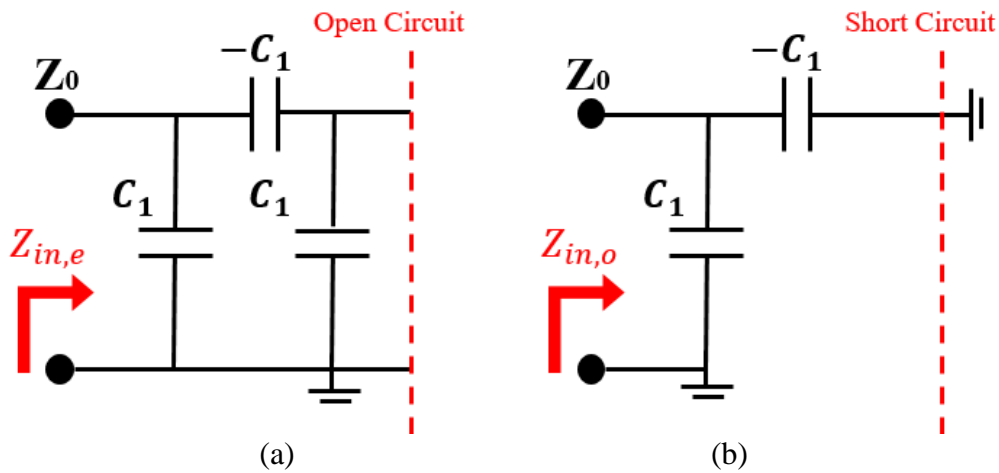


Figure 3.7 Even-mode equivalent circuit (a), Odd-mode equivalent circuit (b)

3.3.2 NF Capacitance Design and Minimization of Residual Resistive Part

As explained in Chapter II, a negative capacitance can be generated using Linvill's Negative-Impedance-Converter (NIC) topology that uses cross-coupled pair (XCP) of transistors [23] to transform the load reactance into a negative one. XCP implementations

with FET have been selected because they are able to operate over wider bandwidth and at higher frequencies than other approaches [24], e.g. than NGD circuits which are mainly based on resonance. Moreover, XCPs are the only topologies that are intrinsically bidirectional (this feature is important for our application). Nevertheless, XCPs are loop-back active circuits known to be sensitive to internal parasitics from the transistors themselves and to external interconnects and component spurious effects; this issue being worsen at high frequencies.

For this reason, we propose here more complete equation than previous analytic studies where we have taken into account more parasitic components of the small-signal FET model in order to identify and quantify their influence on both imaginary and real parasitic parts. Then, the influences of interconnect lines and component spurious effects will also be quantified while studying the final circuit implementation.

Two different types of XCP with output at the FET source (Figure 3.8-a, later called source topology) and output at the drain (Figure 3.8-b, later called drain topology) are respectively studied.

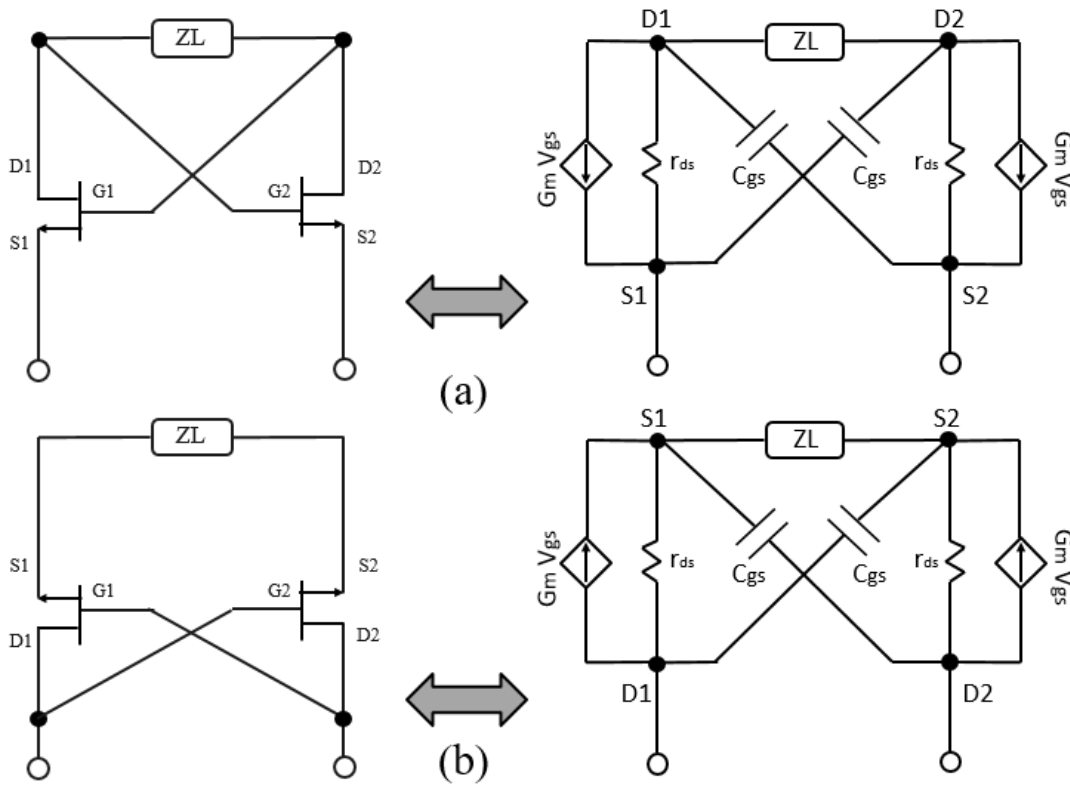


Figure 3.8 Equivalent XCP circuit model with output at source (a), and with output at drain (b)

Based on Figure 3.8 the input impedance of the source and drain topology are respectively expressed as follows:

$$Z_{in, Source} = \frac{2r_{ds}(C_L + C_{gs})(C_L + C_{gs} + C_L g_m r_{ds})}{(C_L + 2C_{gs} + C_L g_m r_{ds})^2 + (C_{gs} C_L r_{ds} \omega)^2} + j \left(\frac{\frac{1}{\omega} (C_L + 2C_{gs} + C_L g_m r_{ds})(g_m r_{ds} - 1) - C_{gs} C_L r_{ds}^2 \omega (C_{gs} + 2C_L)}{(C_L + 2C_{gs} + C_L g_m r_{ds})^2 + (C_{gs} C_L r_{ds} \omega)^2} \right) \quad (3.7)$$

$$Z_{in, Drain} = \frac{2r_{ds}(C_L+C_{gs})(C_L+C_{gs} - C_Lg_m r_{ds})}{(C_L+2C_{gs} - C_Lg_m r_{ds})^2 + (C_{gs}C_L r_{ds}\omega)^2} + j \left(\frac{-1}{\omega} \frac{(C_L+2C_{gs} - C_Lg_m r_{ds})(g_m r_{ds}+1) - C_{gs}C_L r_{ds}^2 \omega (C_{gs}+2C_L)}{(C_L+2C_{gs} - C_Lg_m r_{ds})^2 + (C_{gs}C_L r_{ds}\omega)^2} \right) \quad (3.8)$$

In these expressions, C_L is the capacitance of the load Z_L to be inverted. Usually, these input impedance expressions are not expressed as complete as those presented in (3.7) and (3.8). Indeed, C_{gs} is usually not considered [22], and $g_m.r_{ds}$ is considered much greater than one, which lead to simplification of (3.7) and (3.8) as (3.9) and (3.10) respectively.

$$Z_{in, Source} \approx \frac{2}{g_m} - \frac{1}{jC_L\omega} \quad (3.9)$$

$$Z_{in, Drain} \approx -\frac{2}{g_m} - \frac{1}{jC_L\omega} \quad (3.10)$$

From equations (3.9) and (3.10), it is obvious that i) even after a high level of simplification a significant parasitic real part remains in both topology and ii) that intuitively, cascading the source and drain topologies in series seems promising to minimize the real part of the whole input impedance.

Let's verify these assumptions for a real FET, here VMMK-1218 FET is used (Appendix B). This low noise GaAs pHEMT FET was chosen due to its small package (i.e. with less parasitic), a wide operating frequency range and an ease-of-use, due to only positive DC voltage requirement for bias. Moreover, it shows a high g_m value, suitable to avoid high resistive parts in XCPs. The values for small signal model parameters for $V_{ds}=4V$ and $I_{ds}=15mA$ are $g_m=0.2509 S$, $C_{gs}=1.203pF$ and $r_{ds}=242.2\Omega$. For that FET and if C_L corresponds to a few pF, $(C_{gs}+C_L) \ll (C_L.g_m.r_{ds})$ and $g_m.r_{ds} \gg 1$, thus (3.7) and (3.8) can be approximated by:

$$Z_{in, Source} \approx \frac{2(C_L+C_{gs})}{(C_Lg_m)} - \frac{1}{jC_L\omega} \quad (3.11)$$

$$Z_{in, Drain} \approx -\frac{2(C_L+C_{gs})}{(C_Lg_m)} - \frac{1}{jC_L\omega} \quad (3.12)$$

Equations (3.11) and (3.12) show that for classical g_m values the NF circuits have non-negligible real part values and that C_{gs} contributes to increase significantly these real parts. On the contrary, the influence of C_{gs} on the reactive part is rather low. Moreover, the idea of cascading both topologies to achieve a negative capacitance with a reduced real part is still valid and will be used. For our PS, we chose C_1 to be 1pF as an example, and we used our synthesis equations to achieve a pure negative capacitance $C_2 = -1pF$. Then by using unsimplified equations (3.7) and (3.8), the input impedance of both topologies is calculated in order to fit an ideal -2pF (i.e. -1pF will be obtained by putting in series two capacitance of -2pF, one from the drain topology and the second one from source topology) as given in Figure 3.9. The input impedance for each topology is seen in Figure 3.10.

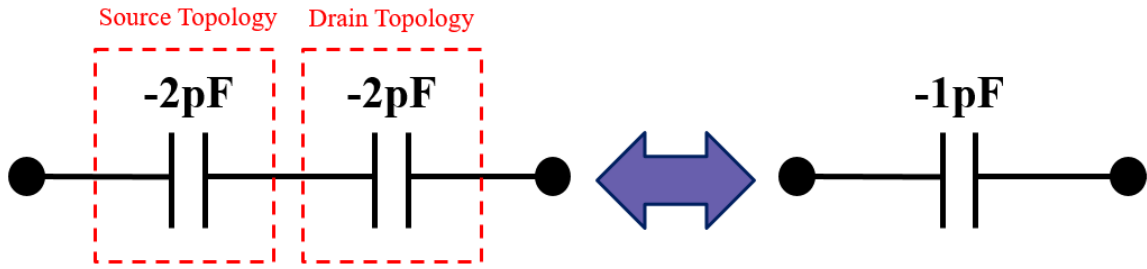


Figure 3.9 cascading source and drain topology to get -1pF

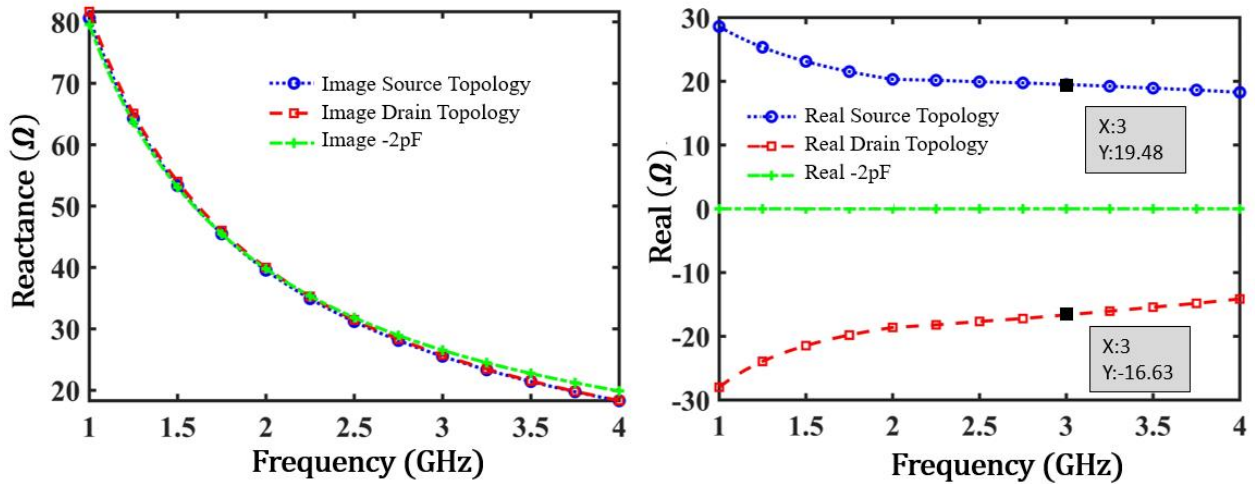


Figure 3.10 XCP input impedance (Imaginary and Real parts) for output at source and drain compared to a negative capacitance of -2pF

Z_L of the source topology must be equal to a capacitance with a value of $C_s = 1.9\text{pF}$ for the source topology and $C_d = 2.1\text{pF}$ for the drain topology to fit a -2pF capacitance. Where C_s and C_d are the loaded capacitors of the source and drain topologies respectively.

From Figure 3.10, it can be noticed that the real part of the source topology is not exactly the opposite of the drain one (markers in Figure 3.10.b), meaning both circuits cascaded (source and drain) will not present a perfect zero real part. We suggest in the following section a second level of reduction of the residual real part in this cascaded topology.

3.3.3 Improved Reduction of Resistive Part of NF Capacitance at the S-Parameters Level

In this section, we first quantify the level of residual real part by cascading both topology (Figure 3.11-a) when S-parameters of the VMMK-1218 (at the bias point $V_{ds}=4\text{V}$ and $I_{ds}=20\text{mA}$ for both XCP) are used in simulations instead of equations. As previously suggested, by cascading both topologies with around -2pF capacitance, it is possible to target a -1pF NF capacitance. Figure 3.11-a (red curve) shows that the real part of the negative capacitance is actually reduced but not much as expected and remains positive, and Fig. 3.11.b shows the -1pF response of the cascaded topologies. To reduce furthermore the real part of the cascaded circuits, we propose to modify the source topology by adding an inductance between Gate and Drain as illustrated in Figure 3.12.

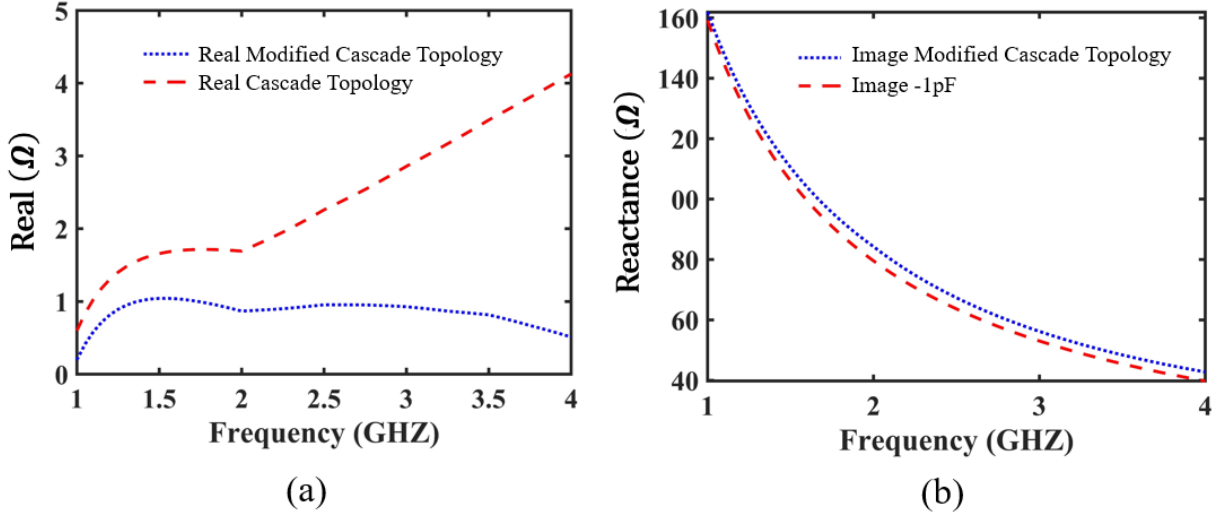


Figure 3.11 Real part of the cascaded NF topology and the modified one (a), image of modified cascade topology compared to -1pF (b)

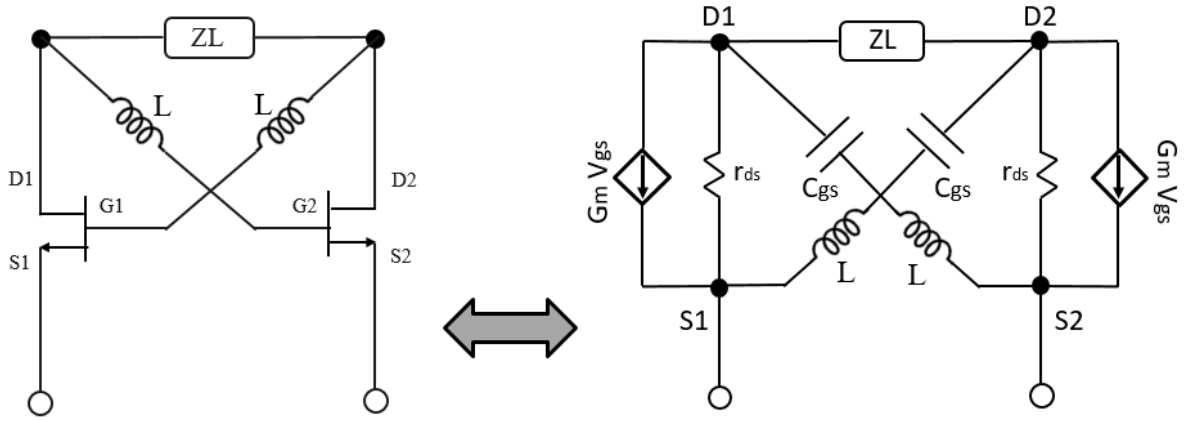


Figure 3.12 Modified source XCP topology

The equation for the modified source topology is calculated as follows:

$$\begin{aligned}
 Z_{in, Source} = & \frac{2r_{ds}(C_L + C_{gs} - C_{gs}C_L L\omega^2)(C_L + C_{gs} + C_L g_m r_{ds} - C_{gs}C_L L\omega^2)}{(C_L + 2C_{gs} + C_L g_m r_{ds} - C_{gs}C_L L\omega^2)^2 + (C_{gs}C_L r_{ds}\omega)^2} \\
 & + j \left(\frac{\frac{1}{\omega}(C_L + 2C_{gs} + C_L g_m r_{ds} - C_{gs}C_L L\omega^2)(g_m r_{ds} - 1 + C_{gs}L\omega^2)}{(C_L + 2C_{gs} + C_L g_m r_{ds} - C_{gs}C_L L\omega^2)^2 + (C_{gs}C_L r_{ds}\omega)^2} \right) \\
 & - j \left(\frac{C_{gs}C_L r_{ds}^2 \omega (C_{gs} + 2C_L - 2C_{gs}C_L L\omega^2)}{(C_L + 2C_{gs} + C_L g_m r_{ds} - C_{gs}C_L L\omega^2)^2 + (C_{gs}C_L r_{ds}\omega)^2} \right) \quad (3.13)
 \end{aligned}$$

By using Equation (3.13), we can tune the value of L in order to have a real part for the source closely equal to that of the drain, while having the imaginary part close to -2pF. Finally, by cascading the drain topology with a modified source XCP, and choosing $C_s=1.3\text{pF}$, $L=1.95\text{nH}$, and $C_d=2.3\text{pF}$ as shown in Figure 3.13, it is possible to keep the resistive part below 1 Ω and to fit the expected reactive part as evidenced by Figure 3.11 (blue dot curves).

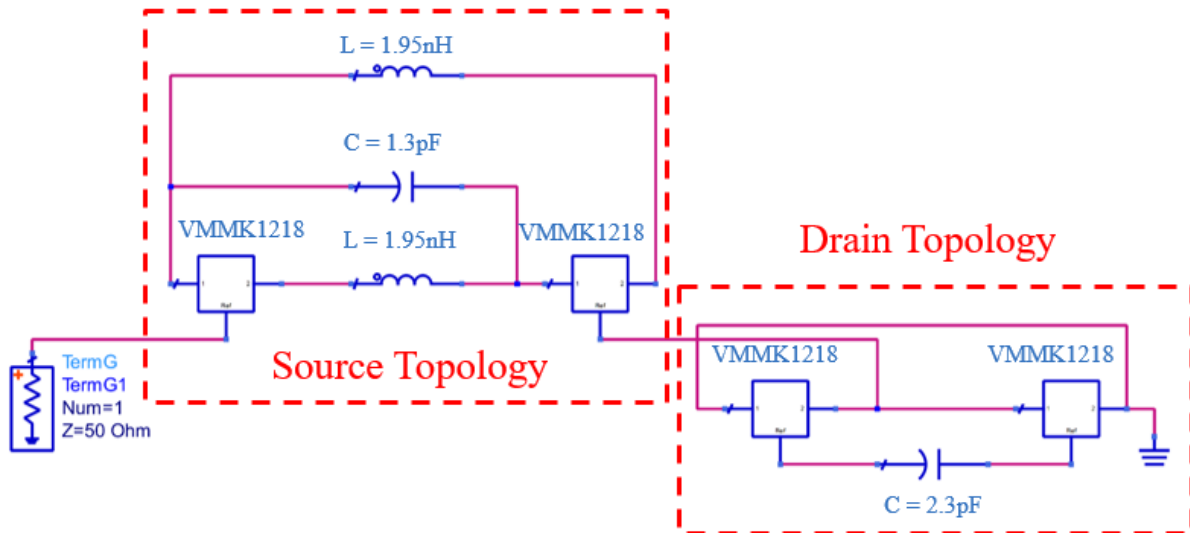


Figure 3.13 Schematic of the modified cascaded NF topology

3.3.4 Active Tunable Pure Phase Shifter Simulation Results

In the PS schematic displayed in Figure 3.6, the ideal non-Foster components (i.e. the negative capacitors) are substituted in simulations by our modified cascaded source-drain topology, in order to get -1pF capacitance with a very low resistance. The resulting schematic of the PS is illustrated in Figure 3.14. The input reflection coefficient (S_{11}) and the forward transmission coefficient (S_{21}), as well as the phase of S_{21} , are depicted in Figure 3.15-a.

As can be noticed from the results, the phase shifter circuit exhibits a good performance within a frequency range of 1 GHz to 4 GHz with a good match and a low insertion loss of -0.789 dB while offering a rather flat “pure” phase response of 180° , which in term corresponds to a null group delay response. In addition, in order to tune the PS, the capacitances C_1 were replaced by varactors. The results of the phase variation are given in Figure 3.15-b for C_1 varying from 1pF to 0.85pF .

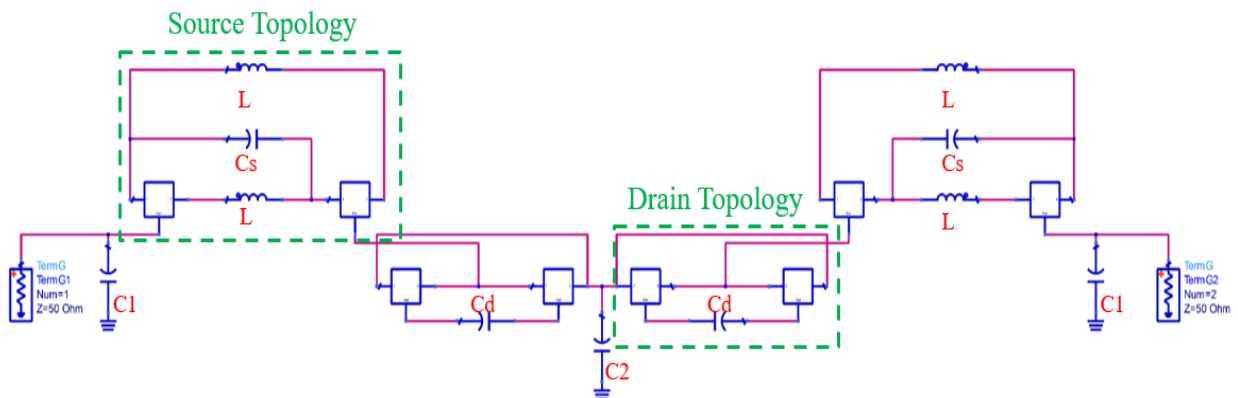


Figure 3.14 The Complete circuit structure of the active phase shifter

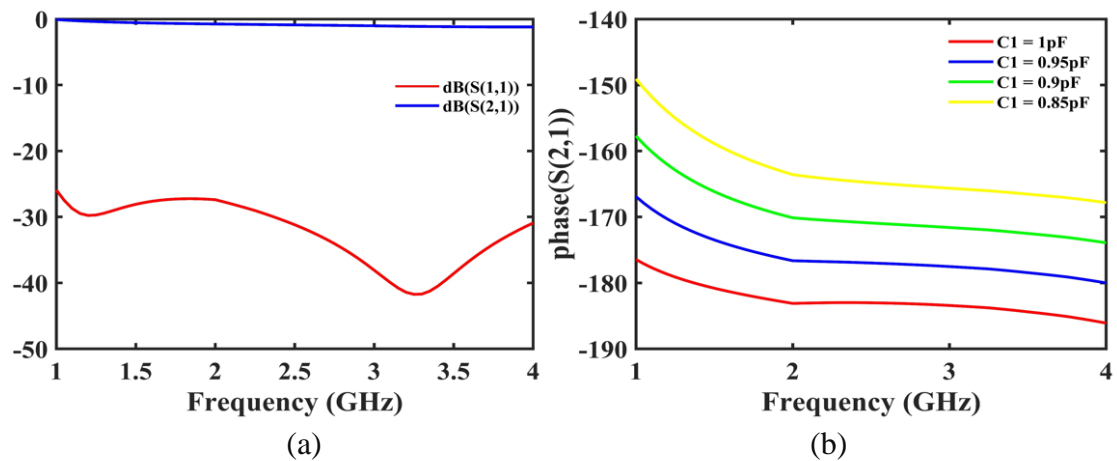


Figure 3.15 PS reflection and transmission coefficients (a),
Phase variation using a Varactor (b)

Thus, at this stage, the proposed modified topology of PS seems relevant to achieve a flat tunable phase around 180° in the frequency range of 1GHz - 4GHz.

3.4 Stability Study

After having analytically studied the NF components and the active phase shifter, validated the theoretical study using ADS Software, and achieved a tunable phase response from 1 GHz to 4 GHz, we must study the stability of the circuit. Indeed NF circuits are known as mainly hard to work with due to their stability issues.

Our stability study is going to be divided into two steps, the first step is to study the Normalized Determinant Function NDF-based method (i.e. the method itself and also its implementation on our circuit) and the next step is to study the influence of biasing parts and distributed sections (typically transmission lines) on stability.

3.4.1 Stability study based on NDF

The stability of the circuit is studied by using NDF method. Indeed, common methods based on K-factor and μ -factor, are usually not valid for non-Foster circuit [25], [26]. On the other hand, NDF is an efficient tool to study the stability of circuits with multiple feedbacks by looking for the existence of Zero in the RHP (Right half of the complex plane) [27].

The main steps to calculate NDF are as follows:

1) Write down the admittance or impedance matrix from Kirchoff's rules at each suspect element or node of the circuit (a suspect node is the node which can cause RHP zeroes to appear, suspect elements consist of transistors, dependent sources (VCVS, VCCS, C CVS, CCCS), and negative valued resistors, inductors, and capacitors (i.e. non-Foster elements)).

2) Calculate the determinant Δ of the admittance matrix.

3) Deactivate all the active devices in the matrix (e.g., let $g_m = 0$ for transistors).

4) Calculate the determinant of the deactivated network matrix as Δ_0 .

5) Then, NDF is calculated as:

$$NDF = \frac{\Delta}{\Delta_0} = \frac{|Y(\omega)|}{|Y_0(\omega)|} = \frac{(s - z_1)(s - z_2) \dots}{(s - p_1)(s - p_2) \dots} \quad (3.14)$$

Where z_1, z_2, \dots and p_1, p_2, \dots are the zeros and poles of NDF, respectively, and $s = \sigma + j\omega$ is the complex frequency in the Laplace transform. Considering these properties, the number of zeros of the NDF in the RHP (poles of the system in the RHP) is equal to the number of clockwise encirclements around the origin that the NDF makes when ω ranges from $-\infty$ to ∞ . Therefore, the system will be stable if, and only if the NDF does not clockwise encircle the origin of the complex plane.

Figure 3.16 shows the phase shifter topology with all the suspected node. It is worth mentioning that we are using the equivalent model of the transistor in order to calculate NDF. Indeed, when calculating the determinant of the deactivated network matrix Δ_0 all the transistors must be deactivated (i.e. $g_m=0$), and that cannot be done using the S-parameters of the transistor.

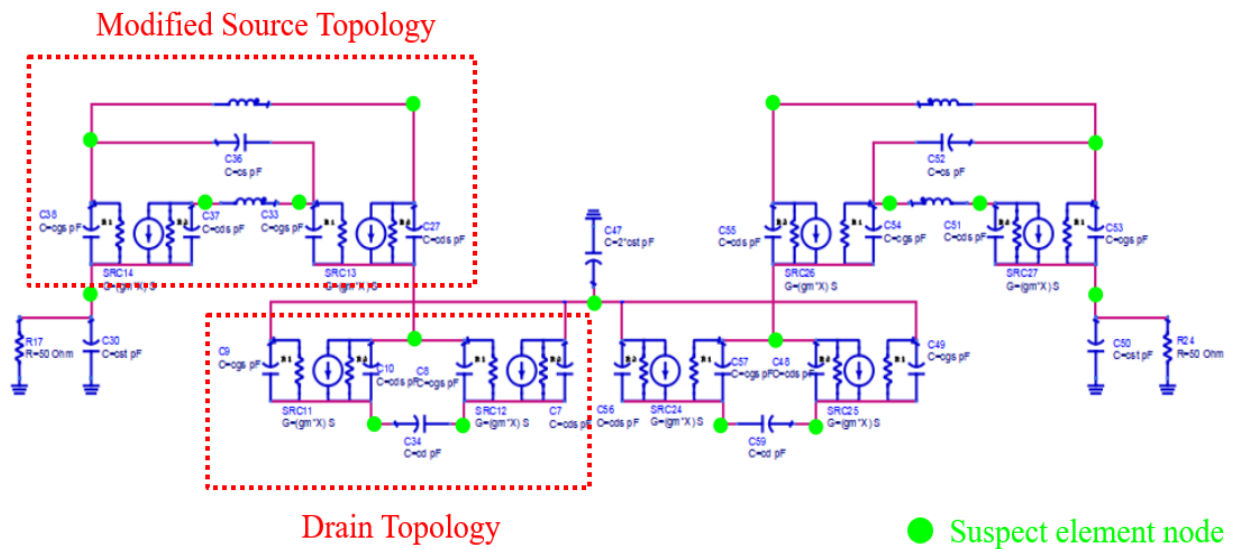


Figure 3.16 Phase Shifter Topology with Suspected Nodes

Figure 3.17 shows the NDF of the circuit, where it can be clearly observed how the NDF encircles the origin in a clockwise sense, so the circuit is found to be unstable. In addition, the predicted oscillation frequency is around 440 MHz (where the NDF first encircles the origin). One can actually know how many times the NDF encircles the origin by dividing the phase of NDF by 360° : the NDF encircles the origin five times, as shown in Figure 3.18.

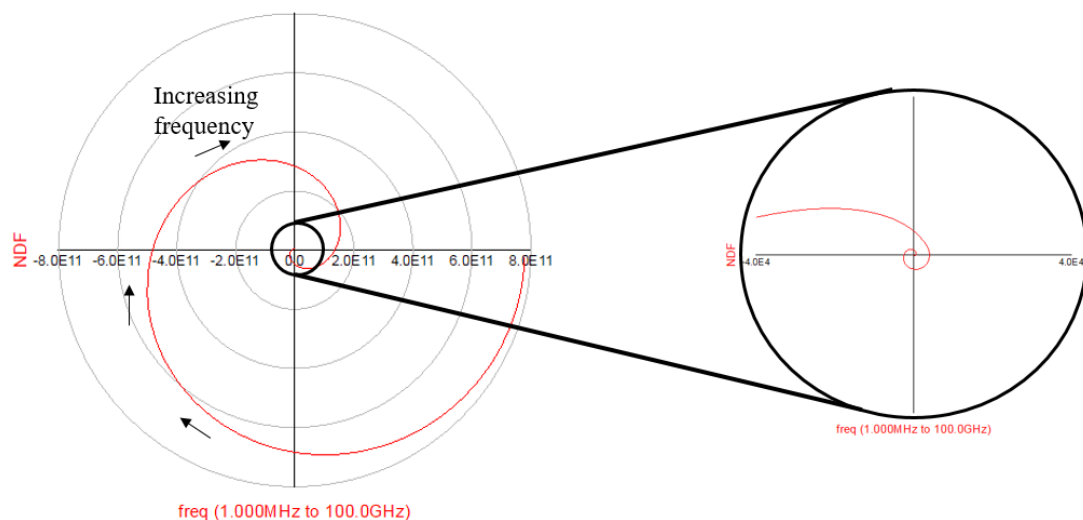


Figure 3.17 NDF of the Phase Shifter

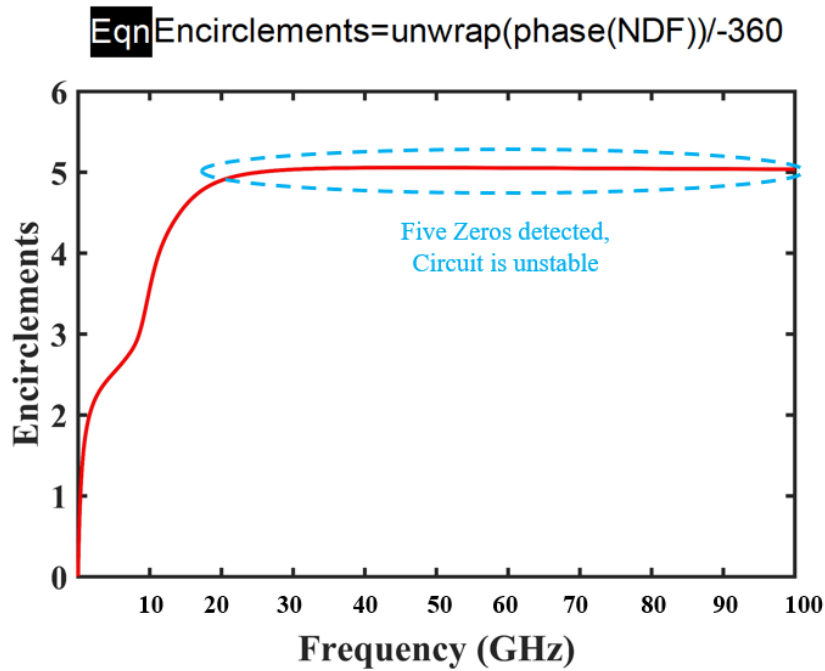


Figure 3.18 Number of Encirclement of NDF around the Origin

It is worth to mention that instability of the phase shifter obtained from NDF mainly comes from the drain topology. Indeed, if we analyze more precisely the stability of the drain topology alone by using Linvill stability, the drain topology would be stable if its inverted impedance is greater than its load impedance (i.e. $|Z_{load}| \leq |Z_{NIC}|$). Figure 3.19 illustrates the PS where only a drain topology is used while showing its impedance and the load ones. Thus, Figure 3.20 clearly shows that the previous stability condition is not satisfied here because the inverted impedance of the drain topology is less than the load impedance.

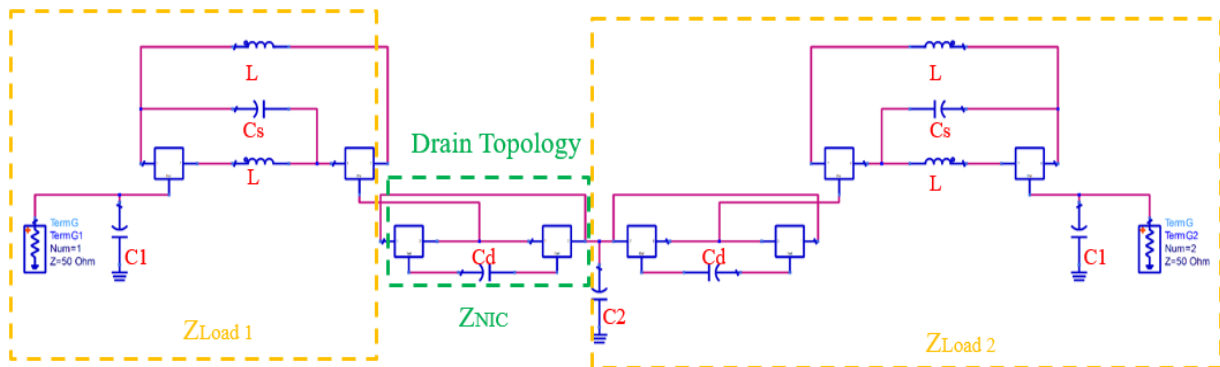


Figure 3.19 Drain Topology Impedance and its Load Impedance

This stability analysis leads us to re-design the PS using only the source topology. It should be noted that designing a PS with only source topology would degrade the flat phase response because of the residual spurious real part of the source topology. In addition to that, having a real part in the PS topology will affect the phase and magnitude responses, but on the other hand, it will help the circuit to be stable.

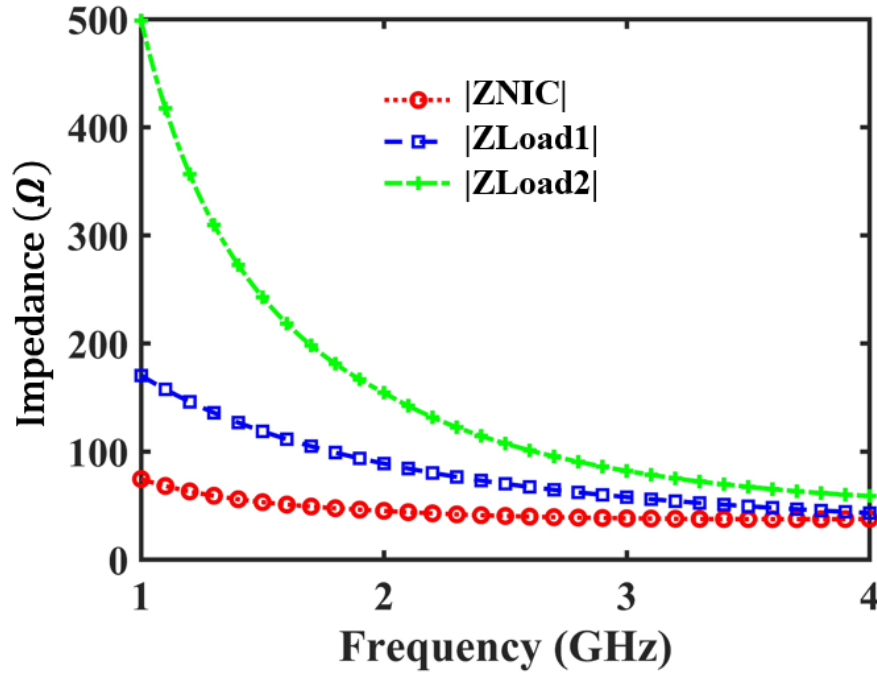


Figure 3.20 Drain Topology Impedance compared to load Impedance

3.4.2 Stability study: influence of DC Bias

Prior an actual implementation, it is also of prime interest to quantify the influence on stability of the elements required around the initial PS circuit. The transistors need to be properly biased for normal operation (here V_{DS} and I_{DS}). An inductor with a large inductance value and a high self-resonant frequency is usually used. However, such inductor may be difficult to find or to implement in practice. Thus, a resistor is usually added in series to alleviate the requirement on inductors at the expense of increased power consumption. To study the effect of DC Biasing on stability, we used a small signal model transistor with the capacitances (DC block) included for source topology.

Figure 3.21 shows the schematic of XCP (NIC) with DC biasing networks at the source of transistors. For the source topology to be stable, it must satisfy the following condition (i.e. $|Z_{load}| \geq |Z_{NIC}|$ or $|C_{load}| \leq |C_{NIC}|$). Then, we have assigned values for all the elements inside the source topology as follows: $C_L = 1$ pF, $C_{NIC} = 2$ pF (the capacitance to be inverted), $R_{b1} = 4$ k Ω , $R_{b2} = 1$ k Ω , $L_b = 200$ nH. We have done the stability study according to the NDF analysis and by setting the value of C_{NIC} to 2 pF, while varying the value of C_L . We can notice from Figure 3.22, that the bias network has a little impact on the stability conditions. Indeed, the circuit happens to be instable for $C_L > 2.3$ pF instead of $C_L > 2$ pF for a biasing network with $R_{b2} = 1$ k Ω . The circuit becomes more stable by further increasing the resistance to 2 k Ω . However, increasing this resistance in the bias network will increase the amount of consumed power.

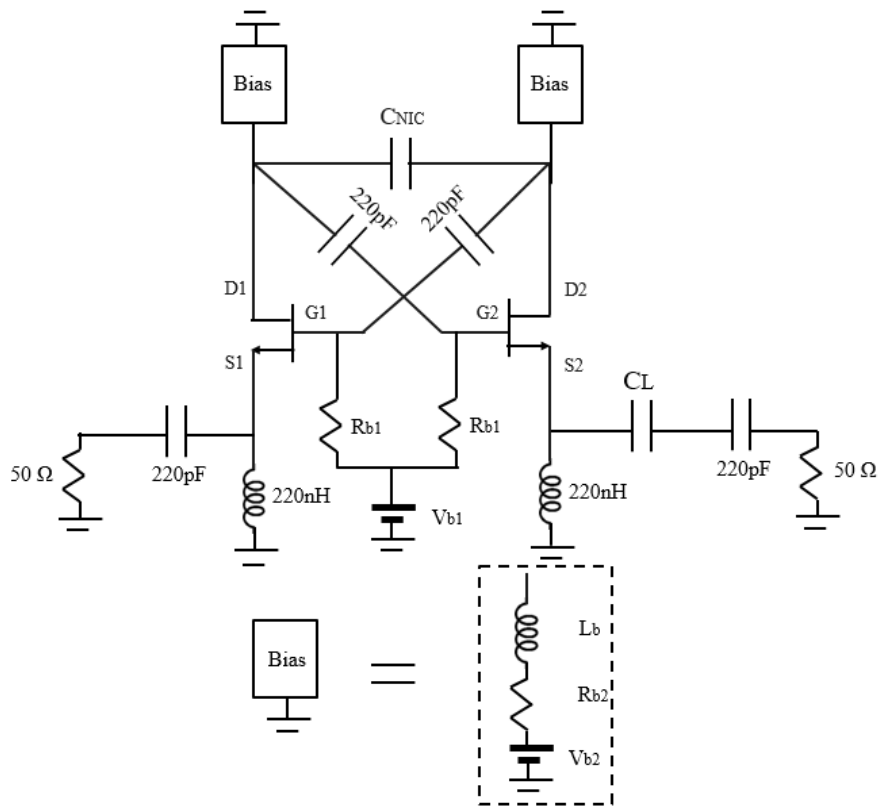


Figure 3.21 Bias Network for Source Topology

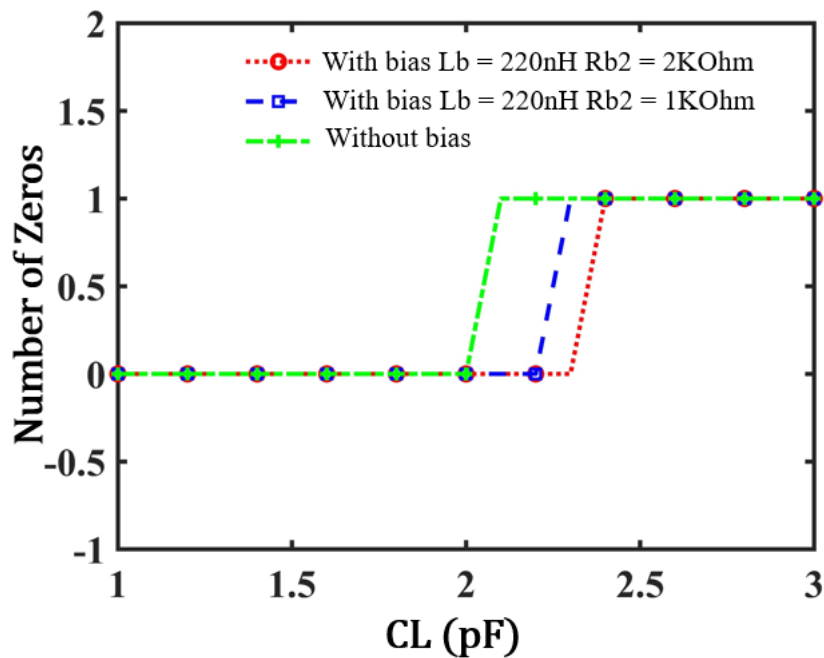


Figure 3.22 Number of Zeros of NDF according to value of C_L

3.4.3 Stability study: influence of transmission line

In our desired frequency band (i.e. 1GHz - 4GHz), the interconnections between distinct elements in the circuit are usually considered as negligible, since the Transmission Lines (TLs) are very short compared to the operational wavelength (i.e. $\ll \lambda$). Nevertheless, it is found that even a short section of TL in the layout of XCP can influence the stability, especially for the TLs in the feedback path (i.e. the path through the two connections between

the gate of the first transistor and the drain of the second one). We will study the effect of the feedback TL on stability by using NDF. Figure 3.23 presents the source topology with inductors L that are used to approximate the short transmission lines that form the feedback path. For FET $g_m \rightarrow 0$, thus we can calculate the determinant of admittance matrix of the circuit in Figure 3.23 as follows:

$$\Delta = \begin{vmatrix} sC_{NIC} + \frac{1}{sL} & -sC_{NIC} + gm & -gm & -\frac{1}{sL} & 0 \\ -sC_{NIC} + gm & sC_{NIC} + \frac{1}{sL} & -\frac{1}{sL} & -gm & 0 \\ 0 & -gm - \frac{1}{sL} & gm + \frac{1}{sL} + Y_S & 0 & 0 \\ -gm - \frac{1}{sL} & 0 & 0 & gm + \frac{1}{sL} + sC_L & -sC_L \\ 0 & 0 & 0 & -sC_L & sC_L + Y_L \end{vmatrix} \quad (3.15)$$

Y_S and Y_L correspond to the admittance of the 50 Ω reference ports. To deactivate the active elements, we set $g_m = 0$ to obtain Δ_0 . The zeros of NDF are calculated as $\Delta/\Delta_0 = 0$ where NDF is given by:

$$NDF = 2s^3L^2g_mC_{NIC}C_LY_L * [g_m + Y_L] + s^2Y_L * [2C_{NIC}C_LL * [2g_m + Y_L] + g_m^2L^2Y_L * [C_{NIC} - C_L]] + 2sC_{NIC}Y_L * [C_L + g_mY_LL] + Y^2 * [C_{NIC} + C_L] \quad (3.16)$$

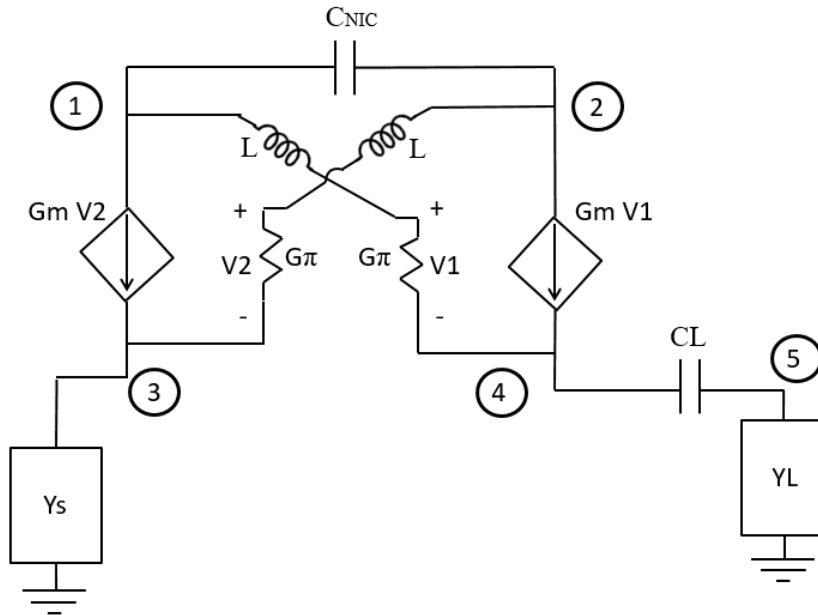


Figure 3.23 Source Topology with Inductors L to mimic interconnect lines

It is found that the circuit has three zeros, and for the circuit to be stable all zeros (named Z_i) must be in the left hand side LHD (i.e. all zeros must be negative).

We set the value of C_{NIC} to 1pF and C_L to 1.2pF and we vary the inductance value L that models the inductance value of the transmission line. We can calculate the oscillation frequency using the following equation:

$$s = \sigma + j\omega \quad (3.17)$$

$$f_{oscillation} = \frac{\omega}{2\pi} \quad (3.18)$$

Table 3.1 presents a parametric study on the effect of the length of the feedback path (represented as inductors L) and the predicted frequency of oscillation. It is noticed for the value chosen for the inductor L, Z_2 and Z_3 are in the RHD, thus an oscillating frequency will occur. Hence, the stability and the maximum frequency achievable of an NIC circuit are greatly dependent on the feedback path length. In addition, it was noted that as the value of inductance L decrease, the oscillation frequency increase as shown in Figure 3.24, until we reach a minimum value of L where all the zeros calculated are positive, which indicate a stable circuit.

Table 3.1 Parametric Study on Inductor and Frequency of Oscillations

Inductor L (nH)	Z_1	Z_2	Z_3	Oscillating Freq (GHz)
1	-3.4e9	-724.1e6 + i*7.44e9	-724.1e6 - i*7.44e9	-----
1.9	-1.7e9	-32.31e6 + i*5.47e9	-32.31e6 -i*5.47e9	-----
2.1	-3.3e9	37.22e6 + i*5.23e9	37.22e6 -i*5.23e9	0.831
3.1	-1.075e9	277.2e6 + i*4.29e9	277.2e6 -i*4.29e9	0.682
4.1	-0.813e9	0.4e9 + i*3.71e9	0.4e9 - i*3.71e9	0.59
5.1	-0.658e9	0.4e9 + i*3.30e9	0.4e9 - i*3.30e9	0.52
6.1	-0.546e9	0.52e9 + i*3.01e9	0.52e9 -i*3.01e9	0.47

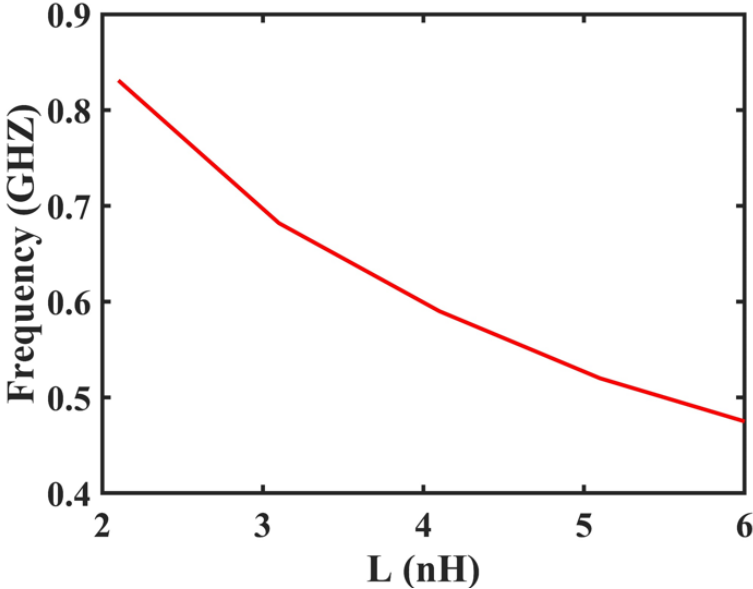


Figure 3.24 Oscillation Frequency as a Function of Inductance Value

We have noticed from calculation (Table 3.1) that if the value of the inductance is above 1.9nH then the circuit will be unstable, we can calculate the actual length of the TL using the following equations [28]:

$$Z_0(\Omega) = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln \left[\frac{5.98H}{(0.8W + T)} \right] \quad (3.19)$$

$$C_0(pF/in) = \frac{0.67(\epsilon_r + 1.41)}{\ln[5.98H/(0.8W + T)]} \quad (3.20)$$

$$L_0(nH/in) = C_0 Z_0^2 \quad (3.21)$$

Using RO4003 substrate (relative permittivity $\epsilon_r = 3.38$, substrate thickness $H = 0.81$ mm, conductor thickness $T = 0.0175$ mm, and conductor width $W = 0.5$ mm), we can get the feedback path length of the TL that is required for the circuit to be stable, which is equal to approximately 0.4mm. This is a very short distance, which is difficult to achieve for a circuit implemented in classical hybrid technology. One way to solve this problem is to build the circuit by using a double layer substrate (with small thickness) where the feedback length will be on one layer while the other components will be on the other layer. Another preferable solution is to use a transistor with a transition frequency lower than the expected frequency of oscillation, which will help preventing the system from going into oscillation. Indeed, in that case, the transistor has a gain much lower than unity after the transition frequency, which should avoid any oscillation to occur.

3.5 Design of non-Foster components using transistor with low transition frequency

Using the information obtained from the stability study in the previous section, a priori stable and oscillation free XCPs are designed by using transistors with low transition frequency (TF) in order to get a non-Foster components (negative capacitance). Three NIC source circuits have been designed using three different transistors Two FET transistors (SKYWORKS SKY65050-372LF and Avago VMMK-1218) and one BJT transistor (NPX BRF93A), datasheets of these transistors are given in appendices B, C, and D.

Figure 3.25 shows the gain vs frequency of the three transistors. From the graph, it can be seen that the TF of the BRF93A transistor is 6GHZ, 12GHZ for SKY65050-372LF transistor, and 23GHZ for VMMK-1218 transistor. This therefore makes the BFR93A and SKY65050-372LF transistors more preferable for designing NIC. It should be mentioned that the topologies were fabricated using Roger RO4003 substrate with thickness of 0.81mm, dielectric constant of 3.38, and loss tangent of 0.0022, and Vias of 0.5mm diameter. The copper plane has a thickness of 0.0175mm.

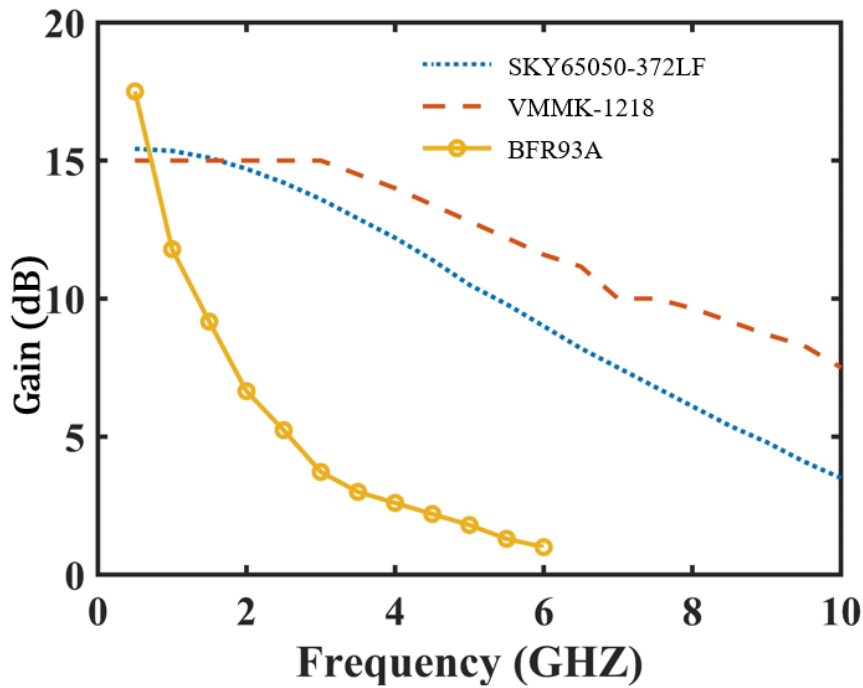


Figure 3.25 Transistors Gain vs Frequency Comparison

As previously mentioned, negative reactance may be unstable, mainly due to the component being inverted having some resistance, which also gets inverted. This inverted resistance is one of the source of the instability within negative impedances. Therefore, to ensure the entire structure to be stable and ultimately measurable, it is necessary to add positive components between the NIC ports and the measurement ports. This makes both the reactance and resistance measured at the measurement ports always positive and the NIC performance and characteristics are then de-embedded from the measured results. The de-embedding includes the transmission line and the load capacitance (C_{Load} , here equal to 4 pF).

The de-embedding is done using the De_Embed2 element in ADS design environment as given in Figure 3.26. The measured S - parameters of the TL only are loaded into the De_Embed2 block, together with a 4pF capacitance (C_{Load}), which negates the effect of positive elements leaving only the inverted one. The De_Embed2 block was then connected in series at both ends with the S - parameter block of the measured NIC circuit.

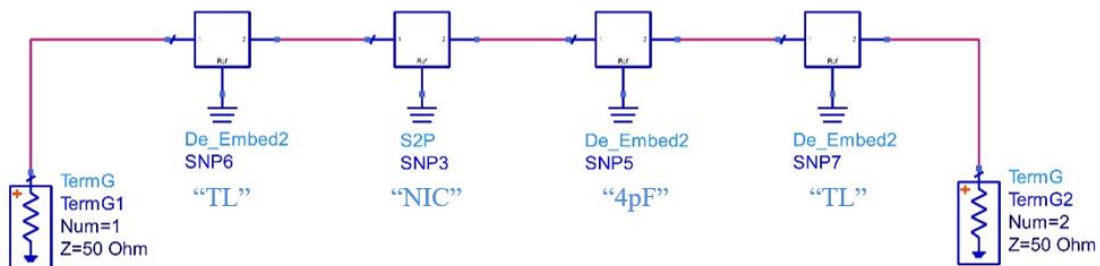


Figure 3.26 De-embedding in ADS

3.5.1 Measured Results

3.5.1.1 Prototype 1

Initial attempts to fabricate the non-Foster circuit involved the use of the Avago VMMK-1218 FET transistor, with a TF of 23 GHz. The NIC layout differs from that of SKYWORKS SKY65050-372LF and is shown in Figure 3.27. The transistors were biased at $V_{ds} = 4V$ and $I_{ds} = 20mA$. This prototype was found unstable and oscillates around 10 GHz. The first indication of instability occurs whenever the NIC is powered up. The powering sequence for the FET transistor is that the drain voltage is turned on first and then the gate voltage. Turning on the gate voltage usually helps controlling the current through the drain but because of the instability the DC control over the gate and drain are lost. Hence, it is never possible to bias the transistors to the required bias conditions. Connecting port two of the NIC structure to a spectrum analyzer with port one terminated with a matched load shows spikes within the frequency band where the transistor is active as shown in Figure 3.28. Many attempts to damp the oscillation have been tried which included extra high pass filters within the NIC, modification of the bias network. Unfortunately, all failed to bring the oscillation under control. Then, a new prototype was implemented using another FET.

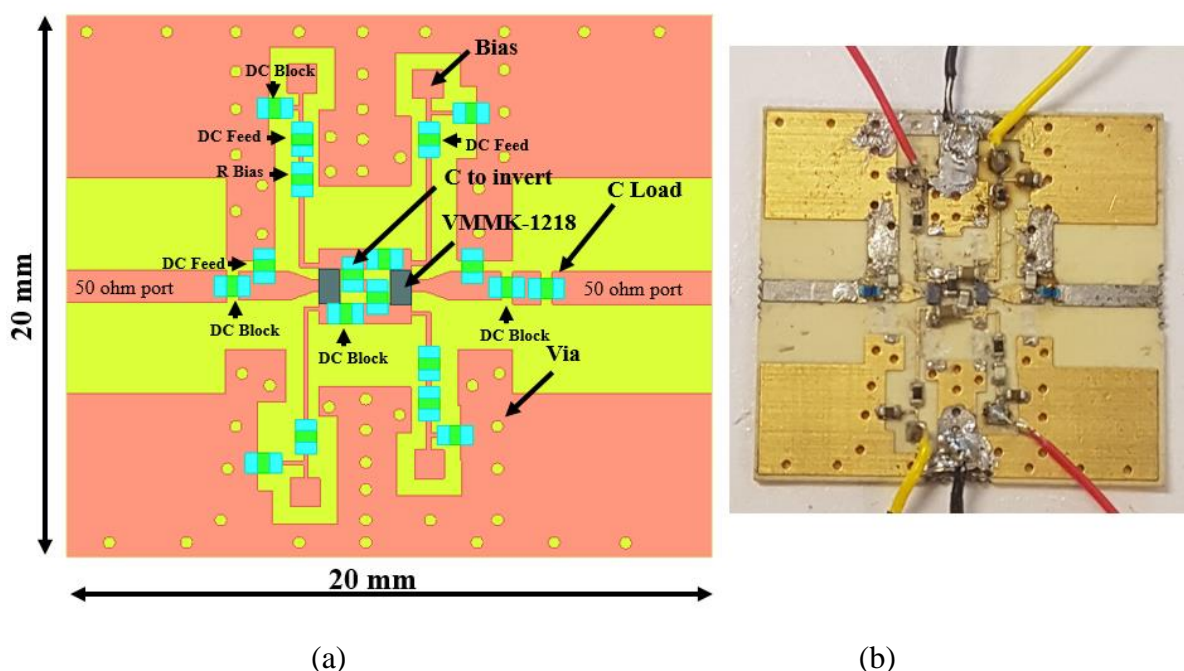


Figure 3.27 NIC Structure with Avago VMMK-1218 FET Structure (a), Built View (b)

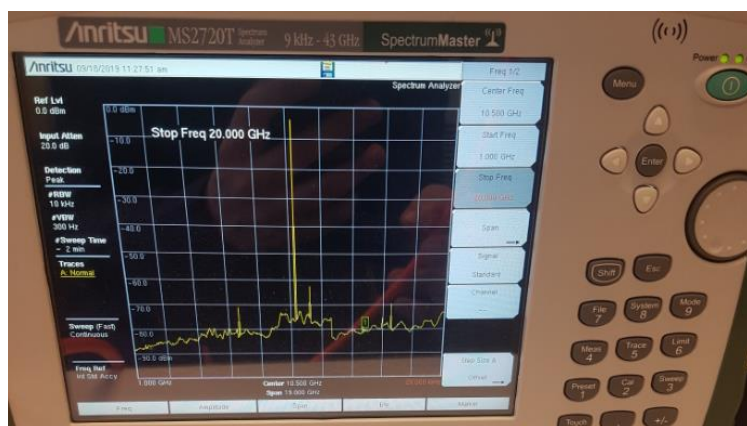
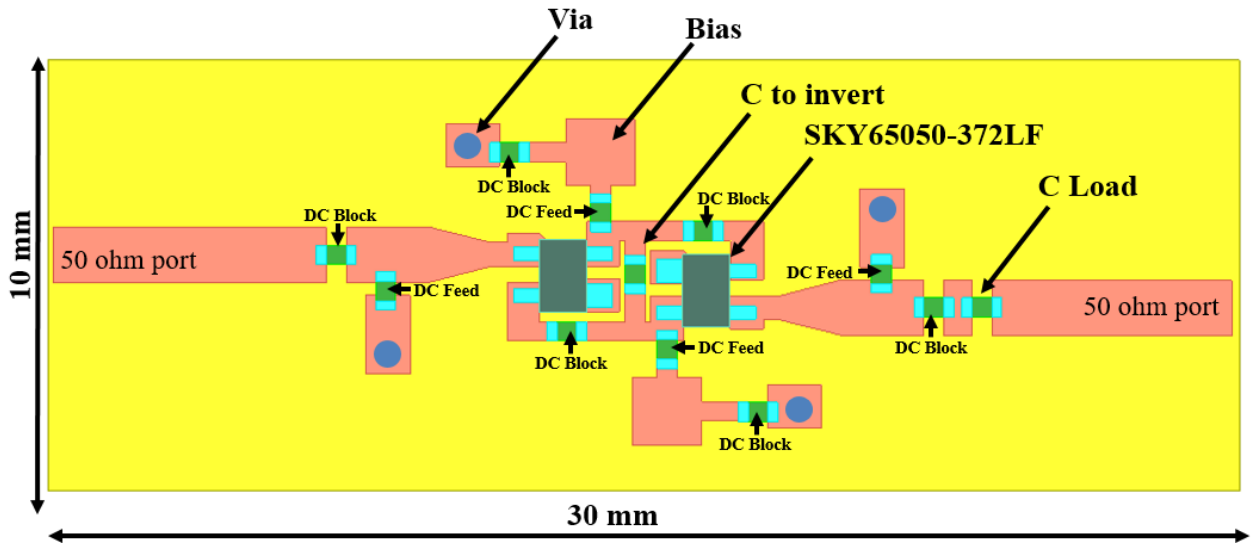


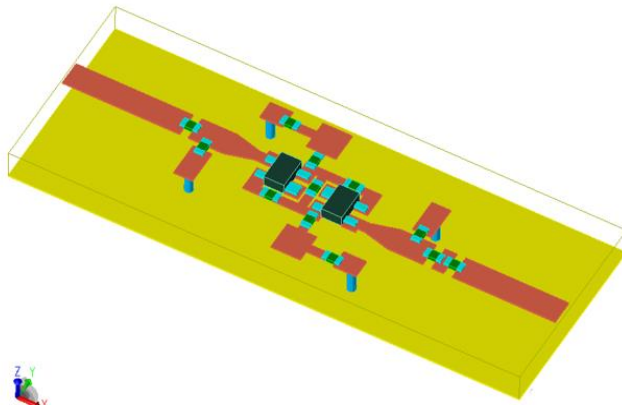
Figure 3.28 Spectrum of Oscillating NIC with Avago VMMK-1218 pHEMT

3.5.1.2 Prototype 2

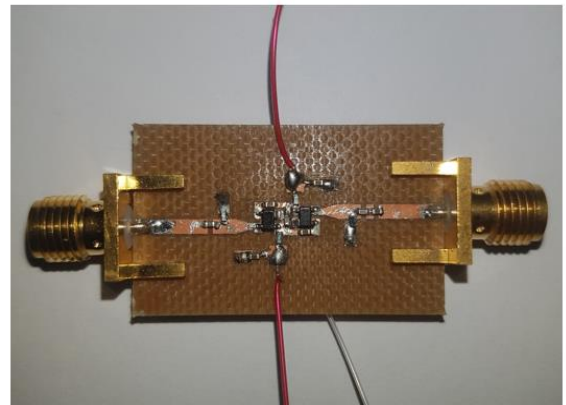
Prototype 2 used the SKYWORKS SKY65050-372LF FET transistor with a lower TF (12 GHz) and the overall structure is shown in Figure 3.29. Its dimensions are 30mm × 10mm. Figure 3.29.a shows the top view of the layout and contains the transistors, the capacitor to invert, the DC bias network and C_{Load} . Table 3.2 shows the list of elements used to realize this NIC.



(a)



(b)



(c)

Figure 3.29 NIC Structure: (a) Top View, (b) Perspective View, (c) Built View

Table 3.2 Components Used in the implemented NIC

Component	Manufacturer	
Transistor	SKYWORKS	SKY65050-372LF
Capacitor (to invert)	Murata 0402	5pF
Capacitor (load)	Murata 0402	4pF
Capacitor (DC Block)	Murata 0402	10nF
Inductor (DC Feed)	Murata 0402	200nH

The measured S_{11} and S_{21} parameters of the structure compared to that of simulated ones are shown in Figure 3.30. It should be noted that this loaded circuit exhibits Foster performance as it rotates clockwise around the Smith Chart as seen in Figure 3.31. The clockwise rotation is due to the connecting transmission lines and the additional loaded capacitor added between the measurement port and the NIC terminals to ensure stability. Figure 3.32 presents the de-embedded NIC performance, which clearly shows a non-Foster behavior by a section of the locus having anti-clockwise rotation around the Smith Chart. The reactance against frequency plot (Figure 3.33) also shows a negative slope, which is a characteristic of Non-Foster elements.

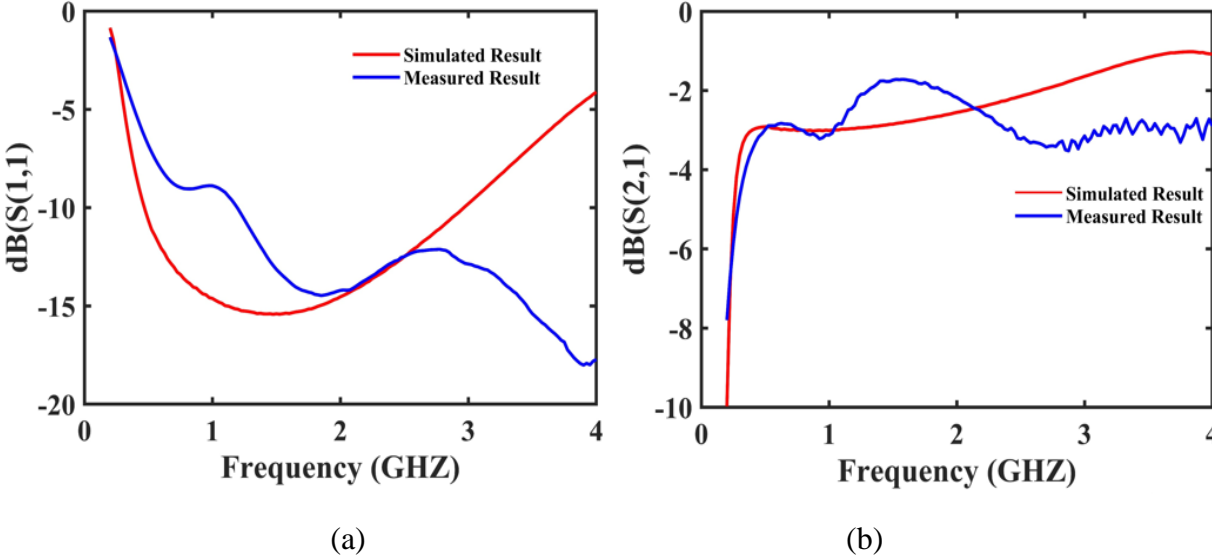


Figure 3.30 Comparison between Measured and Simulated Result of loaded NIC

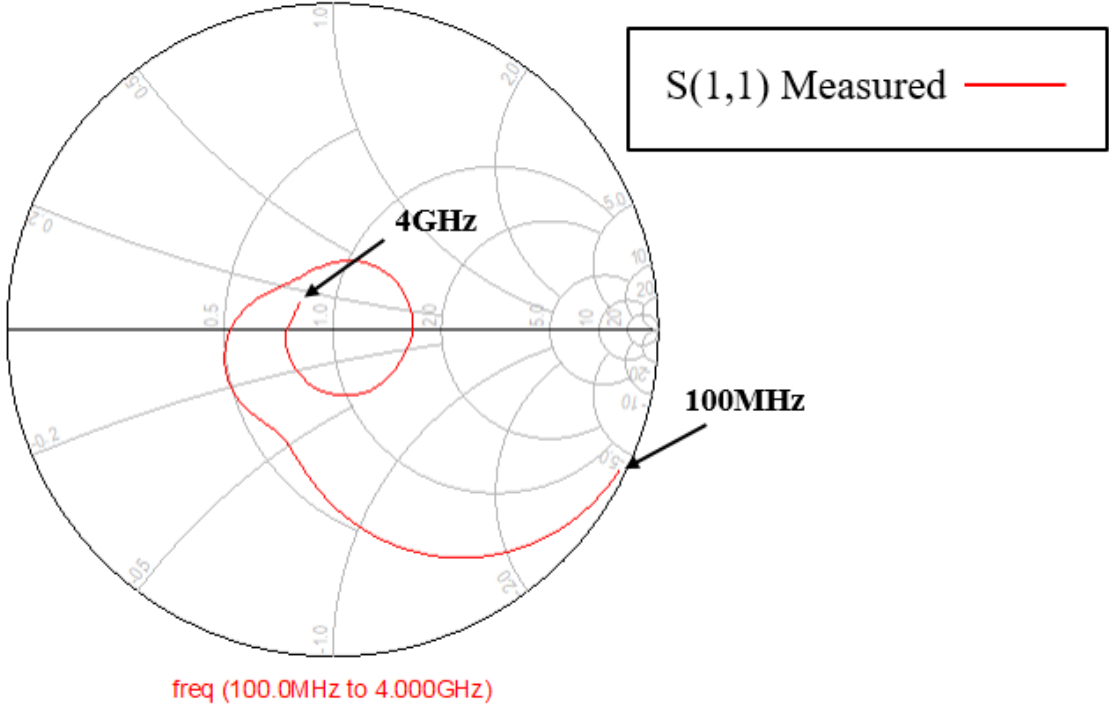


Figure 3.31 Measured Return Loss on Smith Chart of loaded NIC Layout

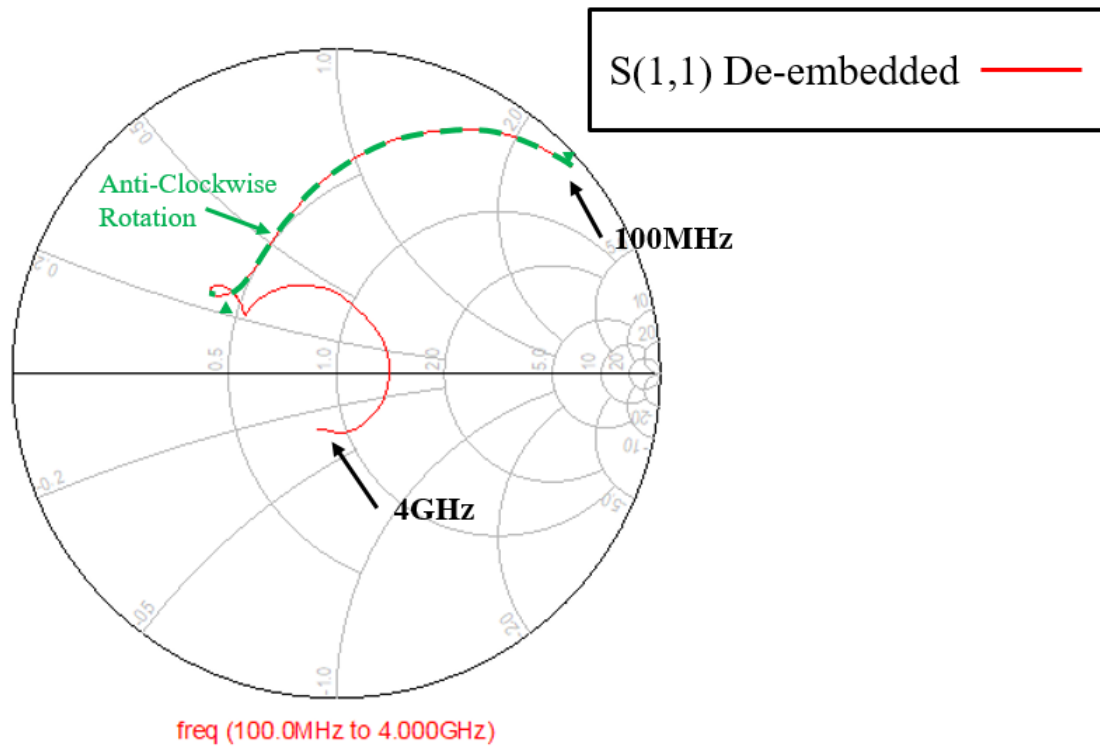


Figure 3.32 De-embedded Measured Return Loss on Smith Chart of NIC

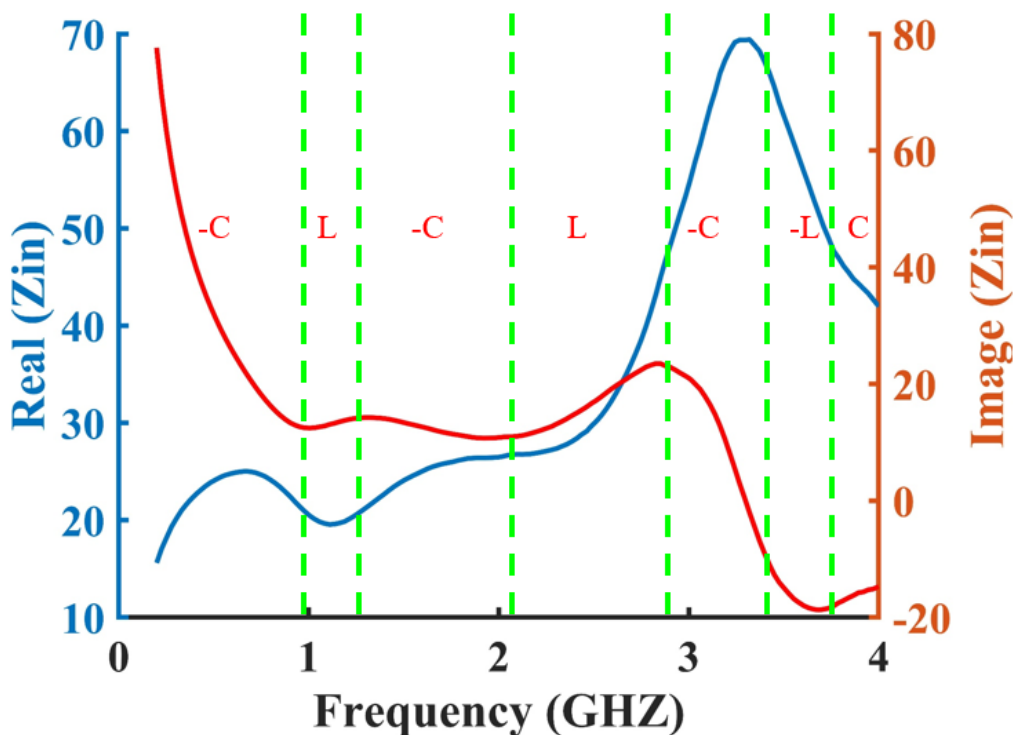


Figure 3.33 De-embedded Reactance of the NIC

The series capacitance/inductance seen between the ports of the NIC is shown in Figure 3.34. It can be seen that at frequencies below 1GHz, the NIC acts as a negative capacitance of value around -10pF. These values are computed from the measured reactance of the de-embedded NIC using equations 3.22 – 3.23. This behavior can also be observed by looking at the impedance plots on a Smith chart (Figure 3.32) where the locus crosses between the negative capacitive into the inductive region and vice versa.

$$C(pF) = \frac{1}{2 * \pi * Freq * X_{NIC De-embedded}} \quad (3.22)$$

$$L(nH) = \frac{X_{NIC De-embedded}}{2 * \pi * Freq} \quad (3.23)$$

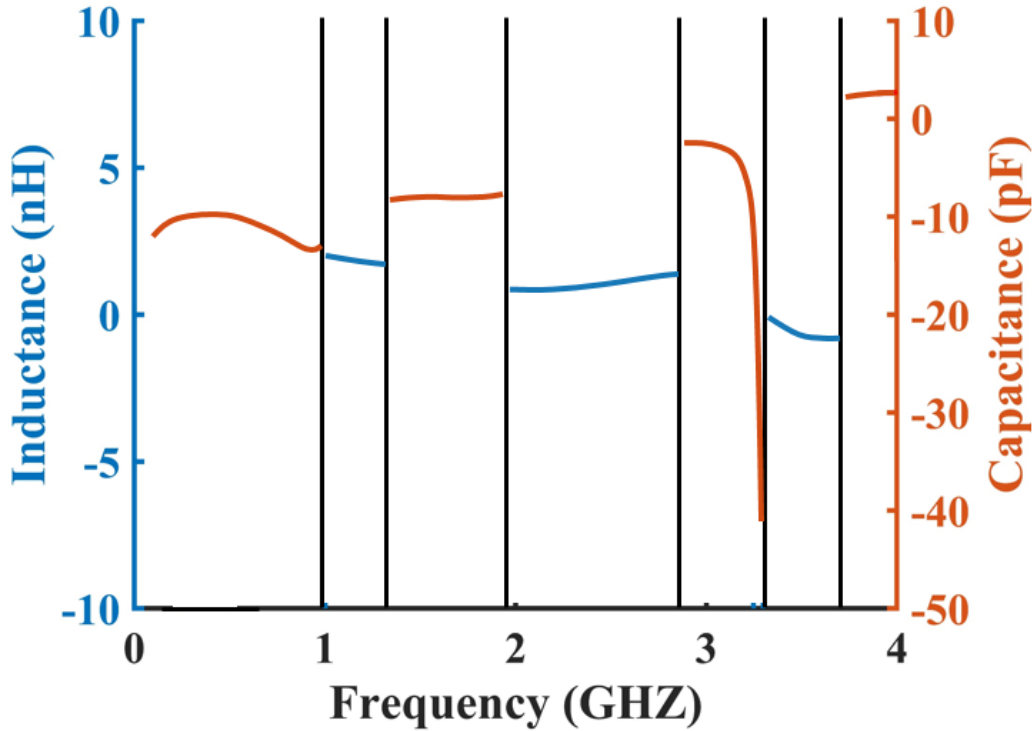
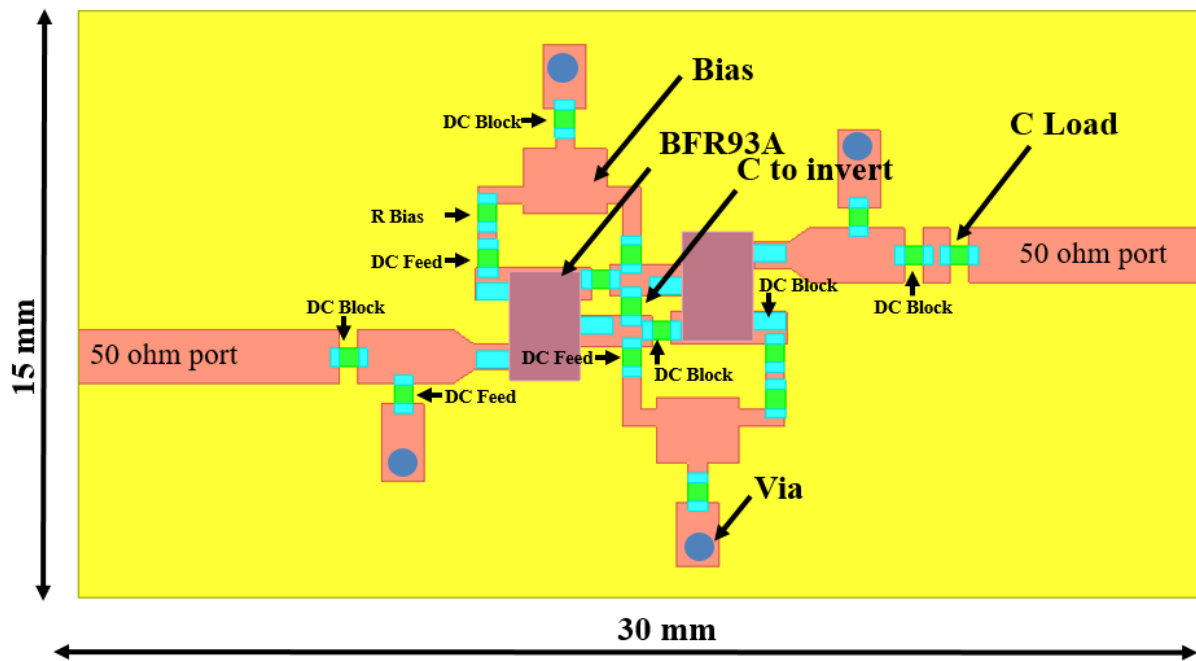


Figure 3.34 The Capacitance and Inductance of the De-Embedded NIC

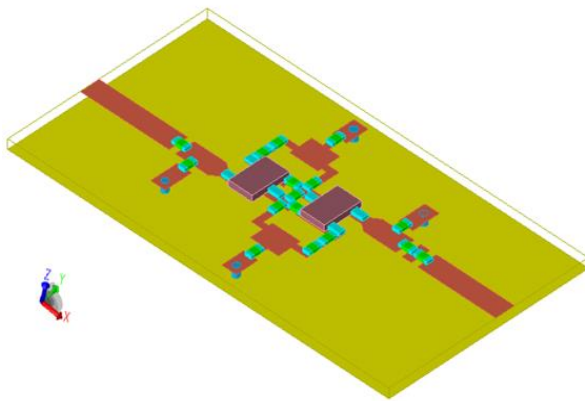
We can notice from the measurement that the circuit does not provide a pure negative capacitance response, may be due to the tolerance and spurious effects of each component. In addition, our NIC circuit also has a real part which is the main reason of the -4dB attenuation seen in Figure 3.30-b. Indeed, the de-embedded real value is given in Figure 3.33, where we can notice that we have around 20Ω for the real part. This response highlights i) the possibility of obtaining Non-Foster behavior below and above 1 GHz using XCP, ii) the difficulty of getting a pure phase response over the desired bandwidth with a low attenuation and iii) as expected at these frequencies, the circuit response is sensible to parasitic effects.

3.5.1.3 Prototype 3

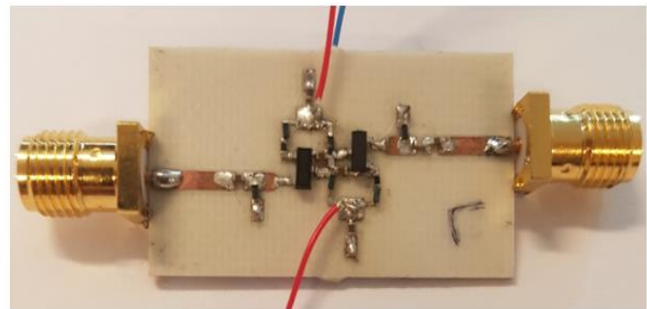
Prototype 3 used the NXP BFR93A BJT transistor with a lower TF (6 GHz) and the overall loaded NIC structure is shown in Figure 3.35. Its dimensions are $30\text{mm} \times 10\text{mm}$. Figure 3.35-a shows a top view of the layout while Table 3.3 shows the list of elements used. It should be mentioned that all the results were done up till 3 GHz because we only had the S - parameter file of BFR93A transistor up to 3 GHz.



(a)



(b)



(c)

Figure 3.35 NIC Structure: (a) Top View, (b) Perspective View, (c) Photo

Table 3.3 Components Used in the implemented NIC using BFR93A

Component	Manufacturer	
	Transistor	NPX
Capacitor (to invert)	Murata 0402	5pF
Capacitor (load)	Murata 0402	4pF
Capacitor (DC Block)	Murata 0402	10nF
Inductor (DC Feed)	Murata 0402	220nH
R_{Bias}	Murata 0402	10k Ω

The measured S_{11} and S_{21} parameters of the structure compared to that of simulated ones are shown in Figure 3.36. Figure 3.37 presents the de-embedded NIC performance, which shows a non-Foster performance by a section of the locus having anti-clockwise rotation around the Smith Chart. The reactance against frequency plot (Figure 3.38) also shows a negative slope, which is a characteristic of non-Foster elements, and the calculated values for the capacitance and inductance are given in Figure 3.39.

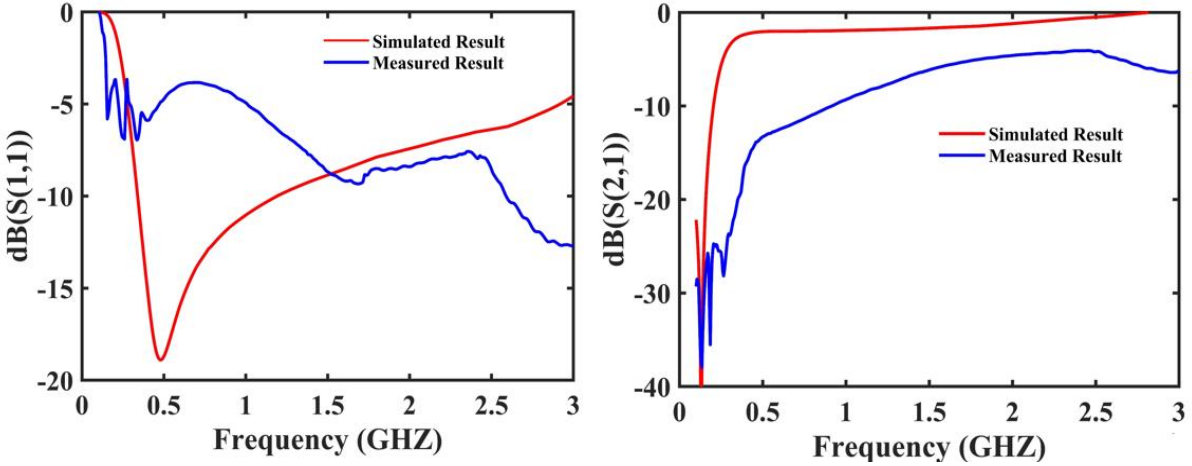


Figure 3.36 Comparison between Measured and Simulated Result of BFR93A NIC

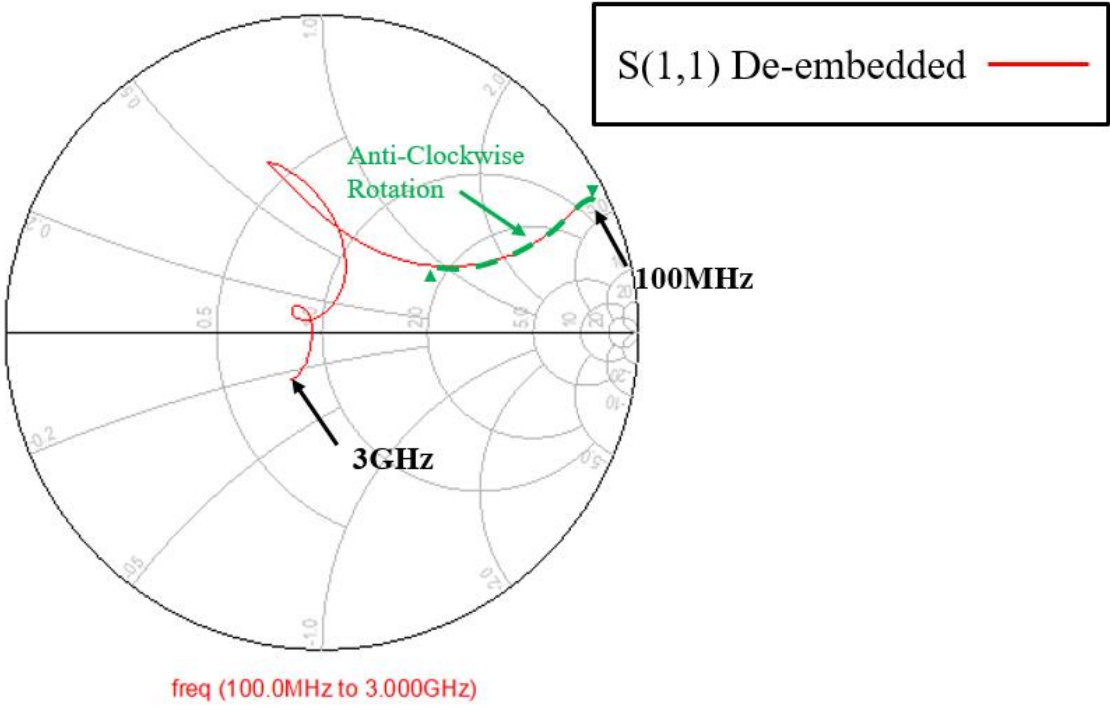


Figure 3.37 De-embedded Measured Return Loss on Smith Chart of BFR93A NIC

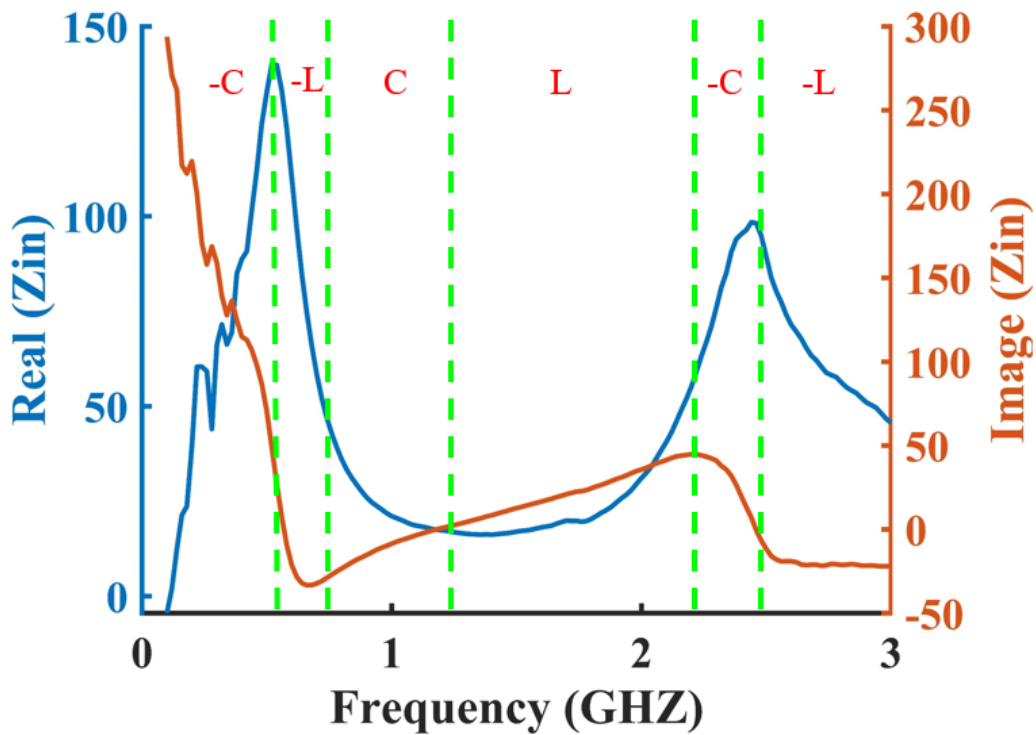


Figure 3.38 De-embedded Reactance of the BFR93A NIC

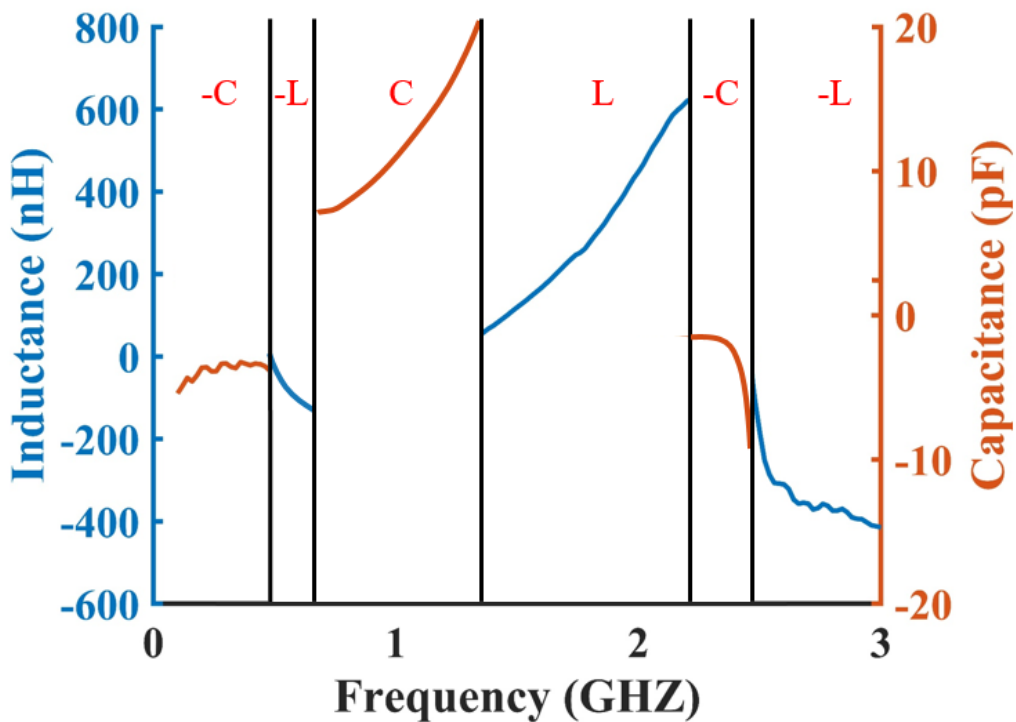


Figure 3.39 The Capacitance and Inductance of the De-Embedded BFR93A NIC

As noticed for SKY source topology, the circuit still does not show a pure negative capacitance response. Moreover, the circuit gives a -5pF in just a small frequency range. Our NIC circuit also have a real part, which leads to high insertion loss as seen in Figure3.36-b. This response highlights once more the difficulty of having a pure phase response over the desired bandwidth with a low attenuation. As the Sky-based circuit provides the best results among the XCP tested, we will focus on using this transistor to design our phase shifter.

3.5.2 2nd Design of Tunable PS

After achieving a stable NIC source topology, we have re-designed our phase shifter but based only on source topology and using SKY transistor as shown in Figure 3.40. Our first step is to re-simulate this circuit to get this new topology response which is given in Figure 3.41. As expected, the circuit exhibits losses and the phase flatness is degraded due to the presence of the real part generated by the source topology. The next step consists in studying the stability of the circuit using NDF, and the circuit shows a stable response without encirclements of the origin (Figure 3.42). The calculated number of encirclements is equal to zero (Figure 3.43) which confirms that our PS circuit is stable compared to the previous PS circuit.

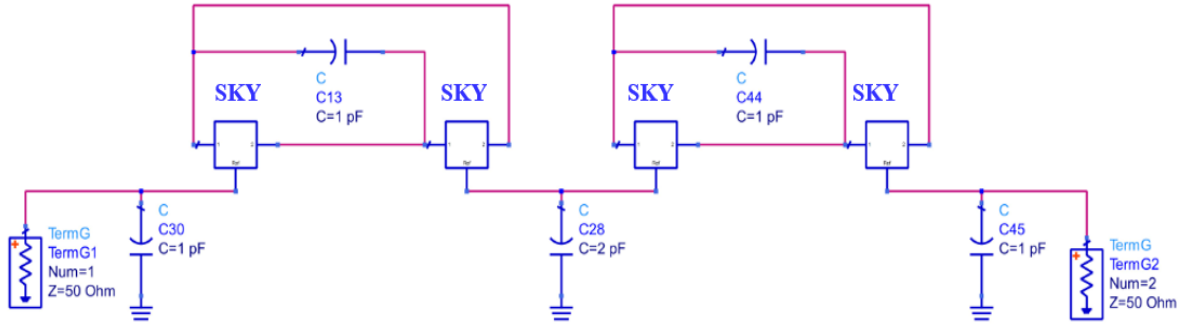


Figure 3.40 The Capacitance and Inductance of the De-Embedded NIC

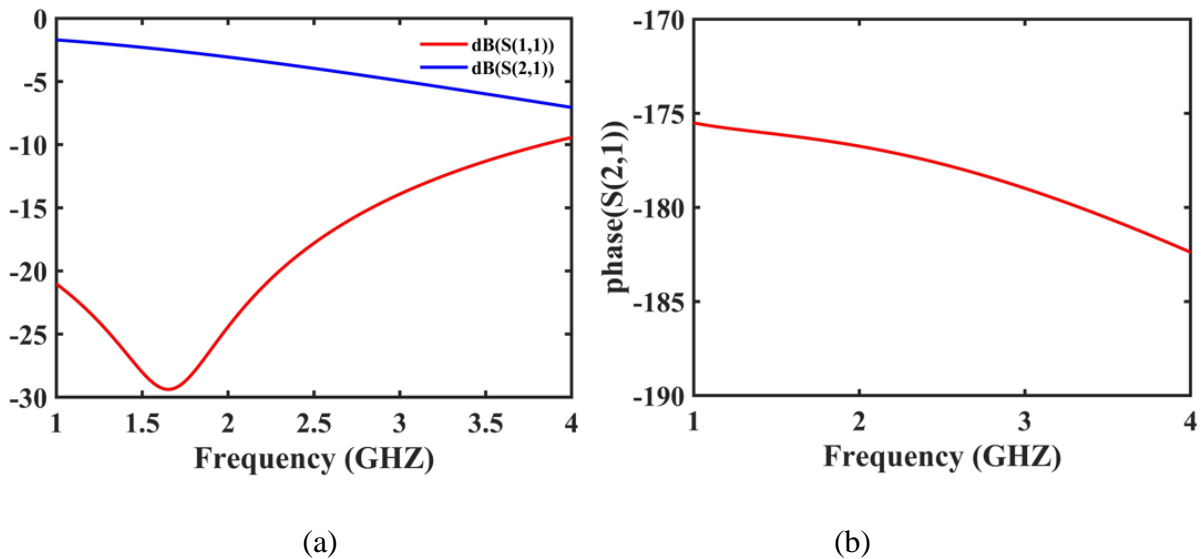


Figure 3.41 2nd PS reflection and transmission coefficients (a), and Phase transmission (b)

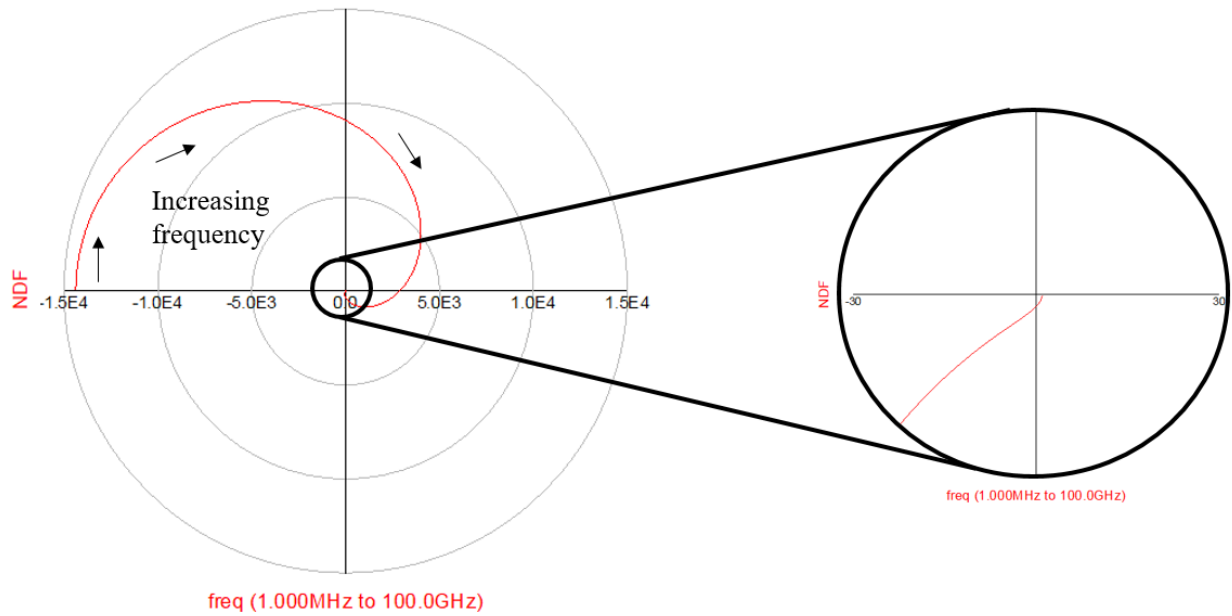


Figure 3.42 NDF of the 2nd Phase Shifter

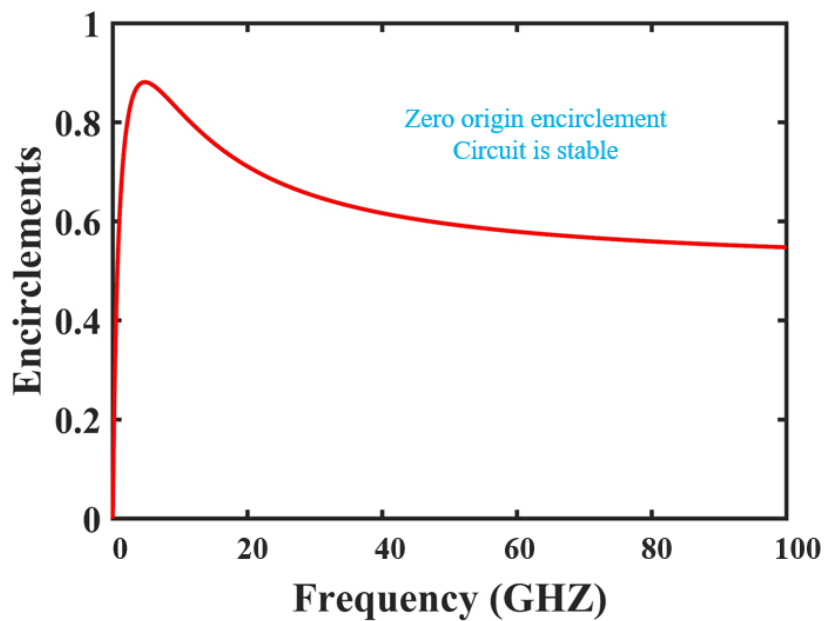
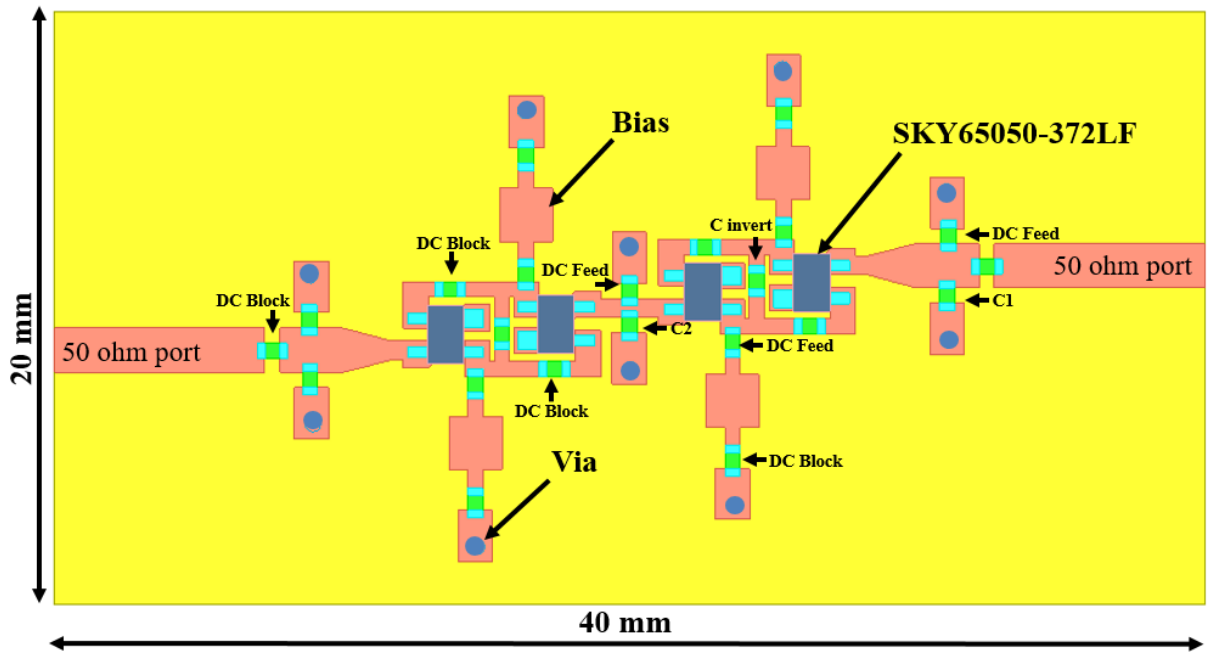
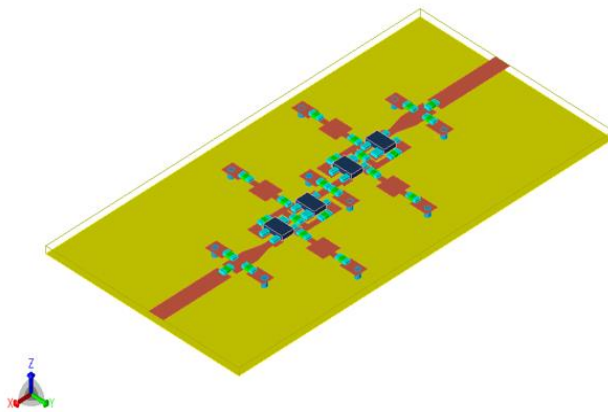


Figure 3.43 Number of Encirclement of NDF around the Origin for the 2nd PS

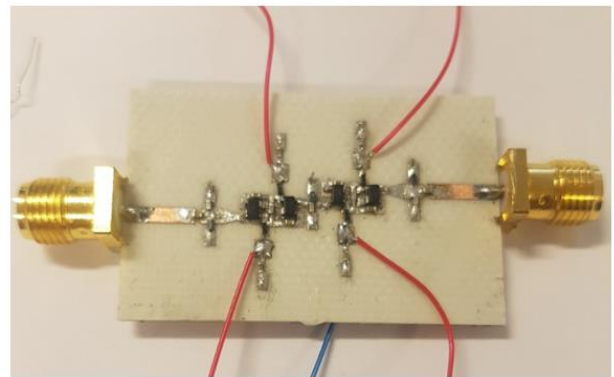
The final stage consists in designing and fabricating the PS. Figure 3.44 shows the whole view of the PS using SKY transistor (layout dimensions of 40mm x 20mm). Table 3.4 presents the values of the components used for this 2nd PS. The measured return and insertion losses given in Figure 3.45 show a good agreement with the simulated results. On the other hand, the measured transmission phase presents a slope greater than that of the simulated one, may be due to the tolerance and spurious effects of the circuit elements. Nevertheless, in the frequency range of 1GHz – 2GHz we can notice a phase shift around 180° (Figure 3.46). Indeed, the source topology generates the targeted -1pF capacitance in that frequency range.



(a)



(b)



(c)

Figure 3.44 2nd PS Structure: (a) Top View, (b) Perspective View, (c) Built View

Table 3.4 Components used in the implemented PS using SKY transistor

Component	Manufacturer	
Transistor	SKYWORKS	SKY65050-372LF
Capacitor (to invert)	Murata 0402	1pF
C1	Murata 0402	1pF
C2	Murata 0402	2pF
Capacitor (DC Block)	Murata 0402	10nF
Inductor (DC Feed)	Murata 0402	220nH

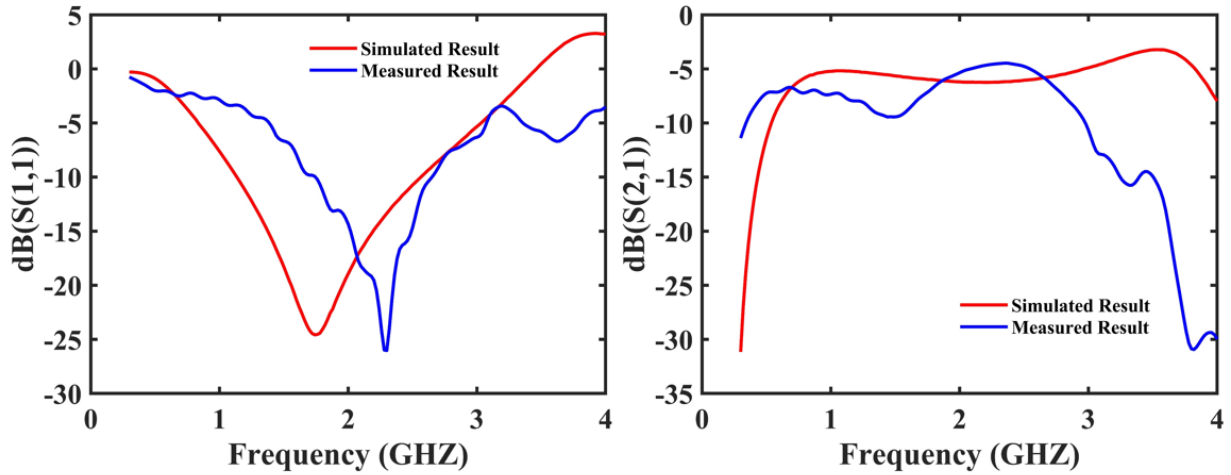


Figure 3.45 Comparison between Measured and Simulated Results for 2nd PS

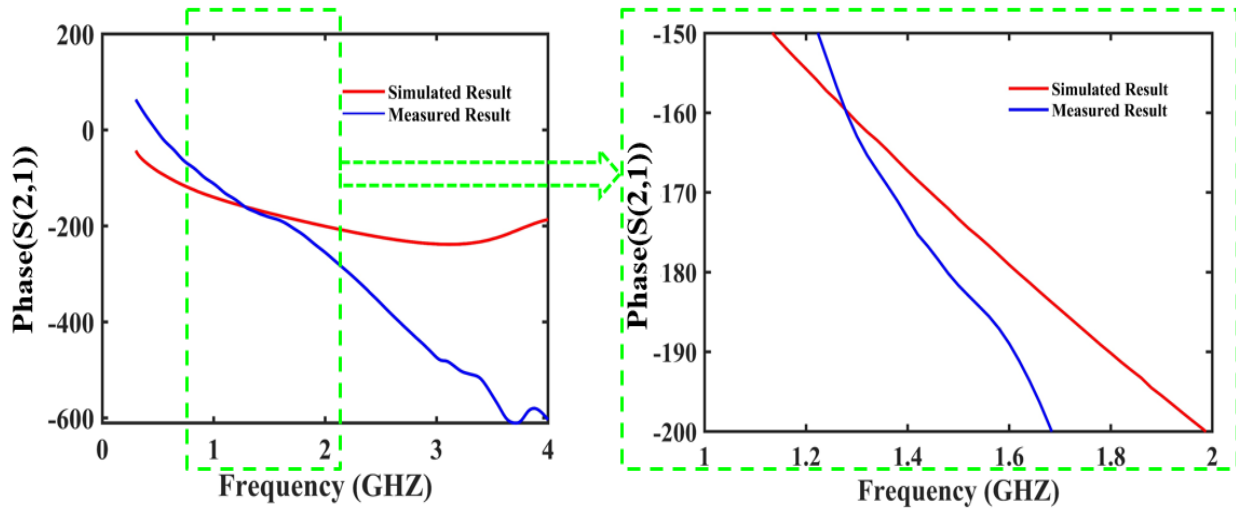


Figure 3.46 Comparison between Measured and Simulated Results for the transmission phase of the 2nd PS

3.6 Conclusion

In this chapter, we have put forward the idea of designing a “pure” or flat tunable 180° phase shifter using Non-Foster elements. We have proposed all the equations needed to synthesize source and drain topologies of cross coupled pairs (XCP). We have suggested to put these two different topologies in cascade to achieve a pure negative capacitance with a very low real part, in order to get a flat 180° phase response in transmission. Nevertheless, the stability study using NDF shows that the proposed PS is unstable. A thorough stability study allowed us to identify that the drain topology does not satisfy Linvill stability condition. Then, our study focuses only on using source topology in order to design a 2nd PS prototype.

This thorough stability analysis was also applied to the source topology. As a result, DC bias network was found to have a little effect on the stability of the circuit contrarily to interconnect lines (and above all the feedback line between the gate of the first transistor and the drain of the second transistor) which were found as the main source of instability. We have carried out equations to calculate the oscillating frequency based on the length of the feedback line, and noticed that in order for the Non-Foster circuit to be stable, the length of the feedback line has to be decreased to a very small value, actually difficult to implement in

hybrid technology. Another approach consists in choosing transistors with transition frequency lower than the frequency of oscillation.

Three transistors were tested to design a stable source topology (i.e. two FET transistors and one BJT). The best results were found by using the Sky transistor (pHEMT FET with $TF = 13\text{GHz}$) which was chosen to re-design a 2nd PS prototype. Nevertheless, due to tolerance and spurious effects, the two Non-Foster circuit are not giving a constant negative capacitance over the expected frequency range. As expected, the 2nd PS prototype based on SKY transistor was found to be stable but also shows losses and not a pure flat phase. This was due to the real part generated from the source topology. Nevertheless, the measured results were in good agreement with the simulation results, with a phase shift around 180° in a frequency region of 1GHz - 2GHz.

3.7 Perspectives on PS

As evidenced in this chapter, achieving a flat tunable PS is not an easy task when using XCP circuits that suffer from instability issues. The transistor choice and the length of the feedback line appear as the most important criteria when designing a Non-Foster circuit. Nevertheless, even though we manage to build a stable circuit that exhibits a NF behavior it does not give a constant negative reactance. Indeed, the response shifts from positive reactance to negative reactance and vice versa, which mainly relies to the tolerance and spurious effect of all the components including the transistor ones at these frequencies. All these reasons highlight the difficulty of implementing non-Foster circuits by XCP at high frequency range. At lower frequency range (i.e. $< 800\text{MHz}$), the influence of tolerance and spurious effects are lowered, and better responses in terms of negative reactance were evidenced. Thus, getting negative reactance at higher frequency range would require other approaches than Linvill XCP. NGD (Negative Group Delay) circuit which is more stable could be more suitable upon 1 GHz. NGD circuit can be used to generate constant negative reactance response but only over narrow frequency band because they are mainly based on resonant behavior. They can also be made tunable, but suffer from losses, which can be compensated by using an amplifier in series [29]. Another conclusion of this study is the effect of the transmission lines related to the implementation of the ZL inversion load being one of the main causes of instability, it appears necessary to use the integrated technology.

3.8 References

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Chapter 4

NF Decoupling and Matching Dedicated to FD Front-End with Close and Electrically Small Antennas (ESA)

This chapter first reviews the fundamental limitations of electrically small antennas and Gain-Bandwidth restriction of lossless passive matching networks. Second, it addresses the methodology study on how to overcome this limitation using a combination of foster and non-foster circuits. Third, it addresses the study on how to decouple TX and RX antennas, finishing up with how to achieve a full duplex system.

4.1 Introduction

The demand for wide-band small antennas is steadily increasing for future wireless communication systems, due to the need of compact multi-function and multi-standard devices. Electrically Small Antennas (ESA) are thus required due to the limited space available in the structures such as electronic mobile devices (5G), IoT (Internet of Things), medical equipment, etc. However when it comes to design small antennas, related to their operating wavelength (λ), it is important to have a proper knowledge on the fundamental concepts that relate to the antenna size [1], in order to find out alternatives to mitigate the inherent limitations.

4.1.1 Definition of an ESA

We define the antenna electrical size regarding to its occupied volume related to the radian-length ($\lambda/2\pi$) introduced by Wheeler in [1]. When the maximum dimension of an antenna is less than the radian-length, it is then considered as an ESA. Note that a sphere with a radius $\lambda/2\pi$ is referred to a radian sphere, which is a boundary of the transition between the near-field and far-field of a small antenna [2]. Figure 4.1 illustrates a dipole-type electrically small antenna with a maximum dimension of $2a$ fitted within a hypothetical sphere with radius a .

The definition of an electrically small antenna is given by:

$$2a < \frac{\lambda}{2\pi} \quad (4.1)$$

In terms of a wave-number (k), (4.1) can be rewritten as:

$$\frac{2\pi}{\lambda} * a = k * a < \frac{1}{2} \quad (4.2)$$

Therefore, an antenna, is considered to be an electrically small when $k*a < 0.5$.

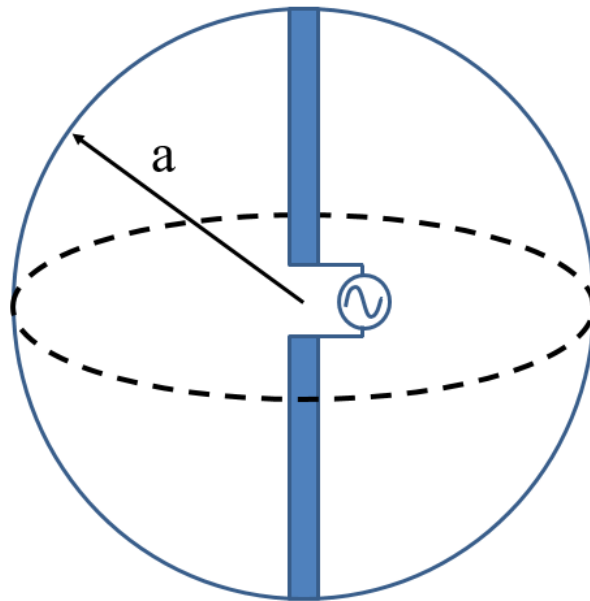


Figure 4.1 A dipole antenna circumscribed by a sphere with radius a

4.1.2 Typical Applications of ESAs

Beyond what any of us can imagine ESAs are used in an enormous variety of systems and embedded devices that are involved in our daily life. In addition to conventional communication handsets (cell phones) and similar transceivers, there are lots of other devices that rely on ESA such as wireless computers and multimedia links, remote control units (i.e. keyless gate entry, garage door openers (Figure 4.2.a) wireless doorbells etc.), wireless Internet, AM and FM receivers for home and vehicle (Figure 4.2.b), Radio Frequency Identification (RFID) devices (Figure 4.2.c), and so on.

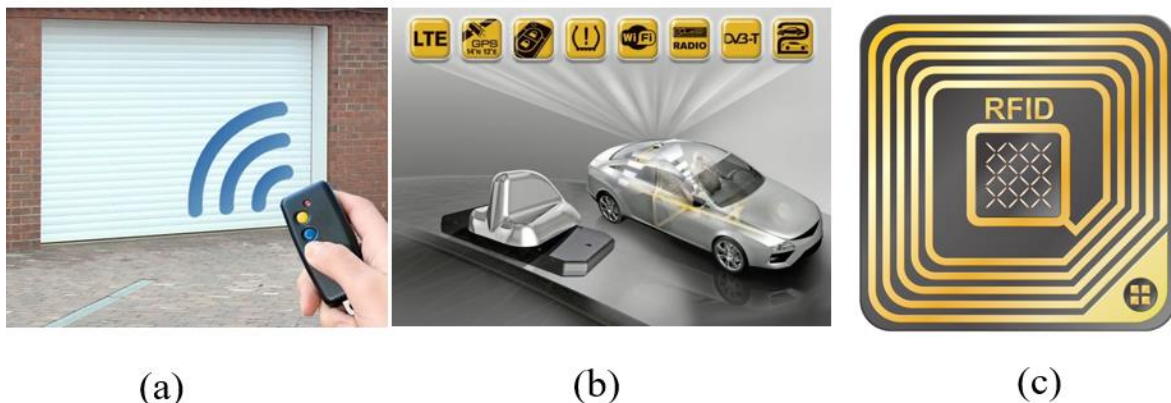


Figure 4.2 Some example of ESA used in everyday life system such as (a) garage keyless door opener [3], (b) vehicular multifunction antenna [4], (c) a RFID tag antenna [5]

4.1.3 Characteristic Impedance of ESA

ESAs can be divided into two types, electric small antenna (example: small dipole), or magnetic small antenna (example: small loop). Both are characterized by their highly reactive impedance. Such antennas impedances show a capacitive response for the electric element and an inductive response for the magnetic one, while their resistive parts are considered very low in both cases. This property highlights the difficulty to perfectly match

this kind of antennas toward 50Ω , over a wide bandwidth, other than a single frequency point.

The input impedance of an electric small dipole antenna with a radius “d” and a length “2a” (Figure 4.3.a), can be expressed in the form $Z_a = R_a + jX_a$ [7], where:

$$R_a = 20(Ka)^2 \quad (4.3)$$

$$X_a = 60 \left(\ln \left(\frac{2a}{d} \right) - 3.39 \right) \left(\frac{1}{ka} \right) \quad (4.4)$$

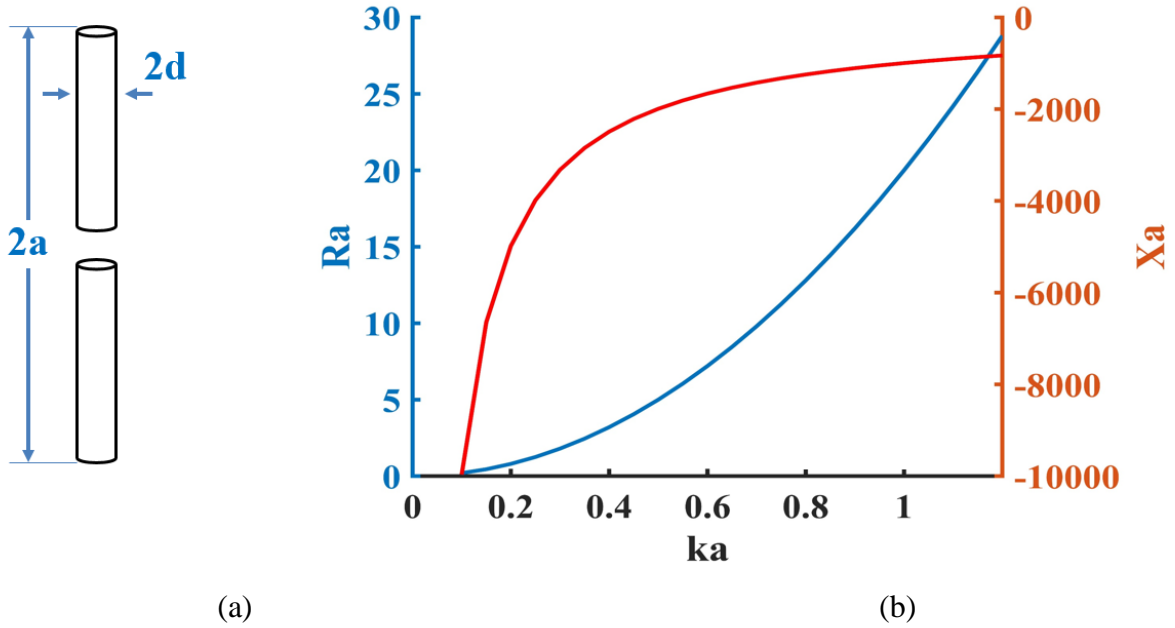


Figure 4.3 Small Electric Dipole (a), Impedance Z_a as Function of Size Factor Ka (b) [7]

The red curve in figure 4.3.b, represents the reactance X_a for $\ln(2a/d) = 20$ (as an example). As the antenna size decreases, the real and the imaginary part of Z_a varies significantly and in a different way.

A similar response is observed for the magnetically small antenna, represented by a small loop with radius “a” and wire radius “d”, as shown in Figure 4.4.a. In this figure the radiation resistance of the antenna is computed by equation 4.5, and the inductance is computed by equation 4.6 [7].

$$R_a = 20(\beta^2 A)^2 \quad (4.5)$$

$$L = a\mu_0\mu_r[\ln(8a/d) - 2] \quad (4.6)$$

Where $\mu_0 = 4\pi \times 10^{-7} H/m$, μ_r is relative permeability, $A = \pi a^2$ is the area of the loop, and $|\beta| = |k|$ for the lossless case ($\alpha = 0$), in $k = \alpha + j\beta$. A low Resistance value and high reactance value are observed for $ka \leq 0.5$. For value of $a = 10$ cm, and $d = 1$ mm ($a/d = 100$) as shown in Figure 4.4.b.

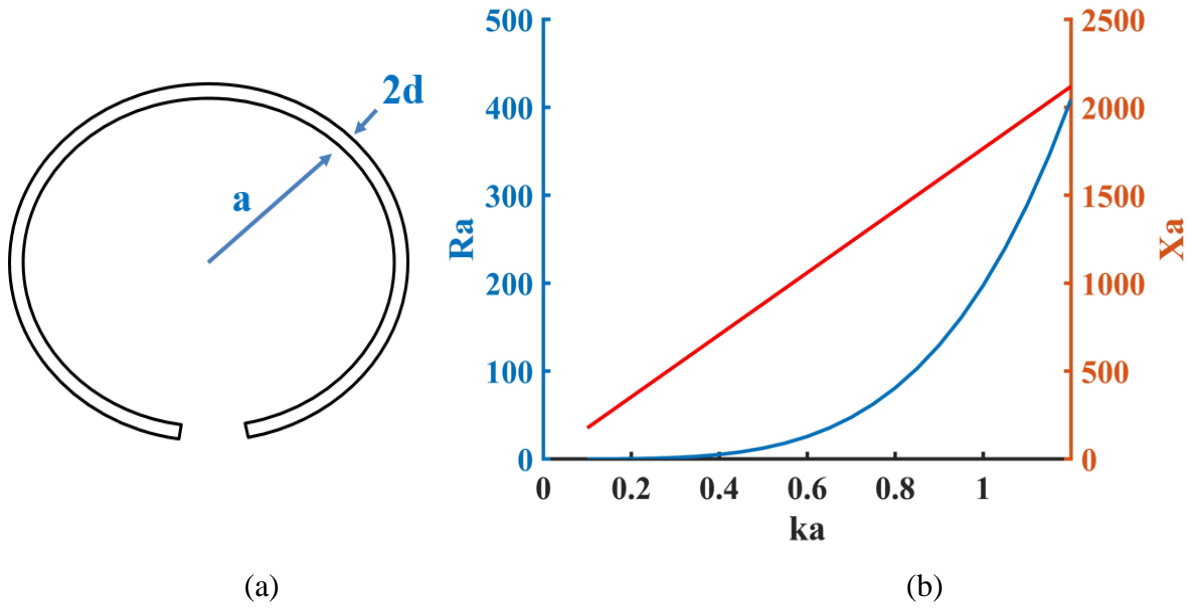


Figure 4.4 Single turn small loop antenna (a), resistive and reactive response of small loop with $a/d = 100$

4.1.4 Fundamental Parameters of ESA

In order to understand ESA, basic antenna parameters should be analyzed and their relationship related to their physical size should be investigated. One of the main parameters is the antenna quality factor, which is explained in the next section.

4.1.4.1 Quality factor Q

The antenna quality factor (Q) is a figure of merit that is used to relate radiated, stored and lost energy. It is defined as the ratio of the energy stored by the antenna to the energy radiated and dissipated by the antenna [8], and is given as follows:

$$Q = \frac{2 \cdot \omega_0 \cdot \max(W_E, W_M)}{P_A} \quad (4.7)$$

Where W_E and W_M are the averaged stored electric and magnetic energies, and P_A is the antenna received power.

Wheeler and Chu defined the Q-factor for an antenna in terms of its size factor “ka” as follows [1], [9];

$$Q = \frac{2 \cdot \omega_0 \cdot \max(W_E, W_M)}{P_A} = \frac{1}{Ka} + \frac{1}{K^3 a^3} \quad (4.8)$$

Equation (4.8) relates the maximum linear dimension of an antenna to the Q-factor. Since “a” is very small, and Q is inversely proportional to the third power of the length, an ESA has a high Q-factor. In addition, the quality factor can also be evaluated using the antenna impedance where the energy stored is given in terms of the antenna reactance, and the power loss is due to the resistive part of the antenna:

$$Q = \frac{|X|}{R} \quad (4.9)$$

4.1.4.2 Bandwidth

The absolute antenna bandwidth is defined as the difference between the upper and the lower frequency bounds ($f_1 - f_2$) taken at -10dB . Some useful relations are recalled hereafter:

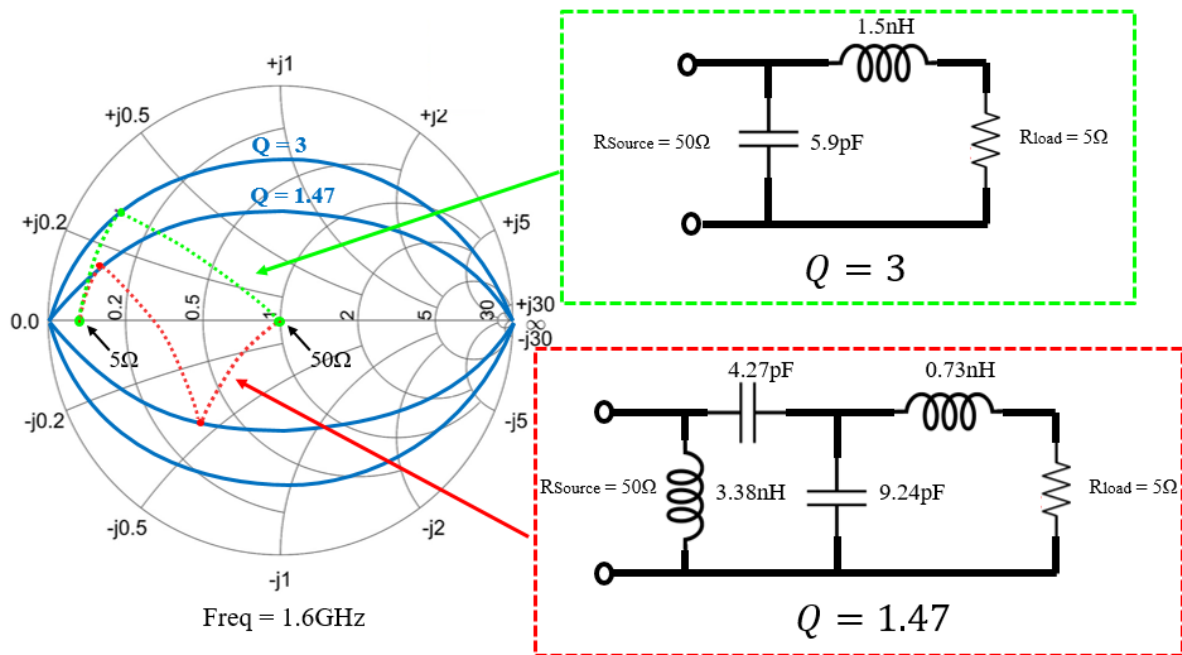
$$\Gamma_{in} = \frac{Z_a - Z_0}{Z_a + Z_0} \quad (4.10)$$

$$VSWR = \frac{(1 + |\Gamma_{in}|)}{(1 - |\Gamma_{in}|)} \quad (4.11)$$

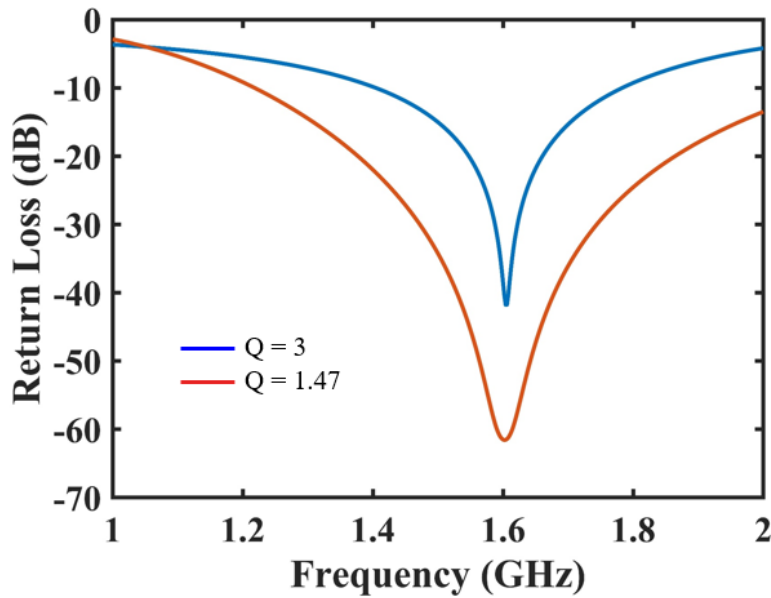
Where Γ_{IN} is the reflection coefficient looking towards the antenna. Z_a and Z_0 are the antenna and the reference characteristic impedances (i.e. 50Ω), respectively. The fractional bandwidth (FBW) is defined as the ratio of bandwidth to the central frequency (f_0) of the band (i.e. $FBW = (f_2 - f_1)/f_0$). This expression is widely used in antenna design. There is an important relation used for ESAs that relates antenna's fractional bandwidth, the Q factor, and the maximum allowable VSWR [10], [11], given as follows:

$$FBW \approx \left(\frac{1}{Q}\right) \left(\frac{VSWR - 1}{\sqrt{VSWR}}\right) \quad (4.12)$$

While the antenna dimensions are getting smaller, the Q factor is increasing and hence the operating bandwidth becomes narrower. Figure 4.5.a shows an example of how the Q factor of a 5Ω Load (at frequency = 1.6GHz) affects the FBW when matched by passive network, it is clear that when the Q factor of the system decreases, the FBW increases (Figure 4.5.b).



(a)



(b)

Figure 4.5 Comparison between 1 stage L-network and 2 stage L-network on Q factor (a), the effect of Q factor on bandwidth (b)

4.1.4.3 Gain-Bandwidth Limitation of Lossless Passive Matching Networks

ESA has extremely high quality factor because most of the input power (reactive energy) is stored in the near-field regions and little power is radiated in the far-field regions [12]. Therefore, it is critical to add external impedance matching networks to increase the transfer of power from a transmitter with a real impedance (usually 50Ω), to the highly reactive antenna (transmitting case) or from the antenna to the receiver (receiving case). Therefore, it allows also to improve the realized gain over a wide bandwidth.

When lossless passive matching networks are used between a resistive generator and a complex passive load, there is a fundamental Gain-Bandwidth restriction derived by Bode [13] and Fano [14]. Given the minimum reflection coefficient magnitude, Bode-Fano integral criterion on a complex passive load can be expressed as the Gain-Bandwidth restriction on the load within a flat pass-band [15]. According to the Bode-Fano criterion, there is a tradeoff between the bandwidth and the minimum acceptable reflection coefficient. Once the minimum reflection coefficient magnitude is determined, the bandwidth is limited, and vice-versa.

For most of electrically small dipole antennas, the input impedance can be simply modeled as a series combination of a resistor and a capacitor. From [15] the Gain-Bandwidth restriction of lossless passive matching networks for a series RC is then given by:

$$\int_0^{\infty} \frac{1}{\omega^2} \ln \frac{1}{|\Gamma(\omega)|} d\omega < \pi RC \quad (4.13)$$

Where $\Gamma(\omega)$ as shown in Figure 4.6 is the reflection coefficient looking into the lossless two-port matching network.

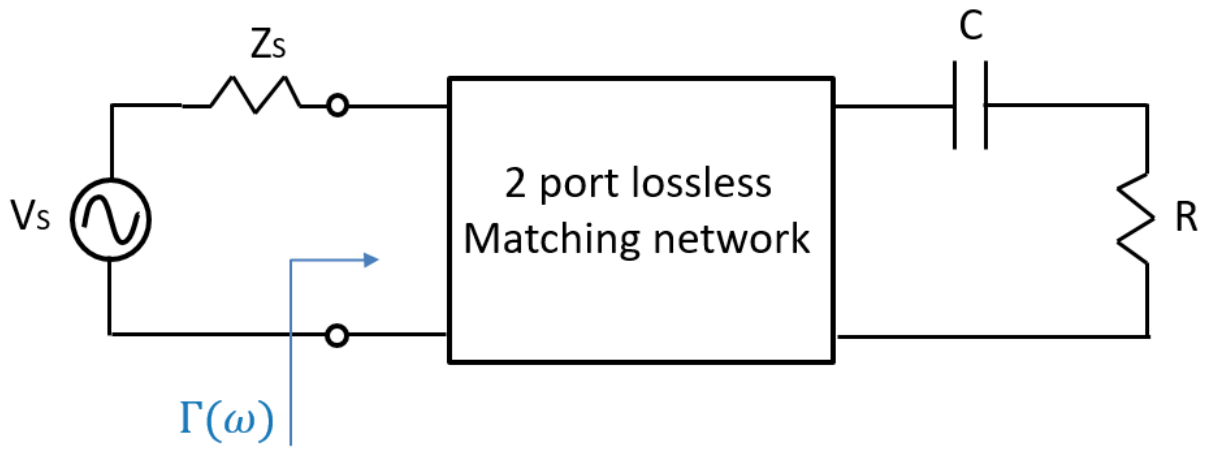


Figure 4.6 port Lossless matching network for a series passive RC

Let the minimum reflection coefficient magnitude be a constant (Γ_m) over the frequency ω_1 to ω_2 as shown in Figure 4.7. Then, (4.13) can be rewritten as [15].

$$\int_0^\infty \frac{1}{\omega^2} \ln \frac{1}{|\Gamma_m|} d\omega = \Delta\omega \ln \frac{1}{|\Gamma_m|} \leq \pi\omega_0^2 RC \quad (4.14)$$

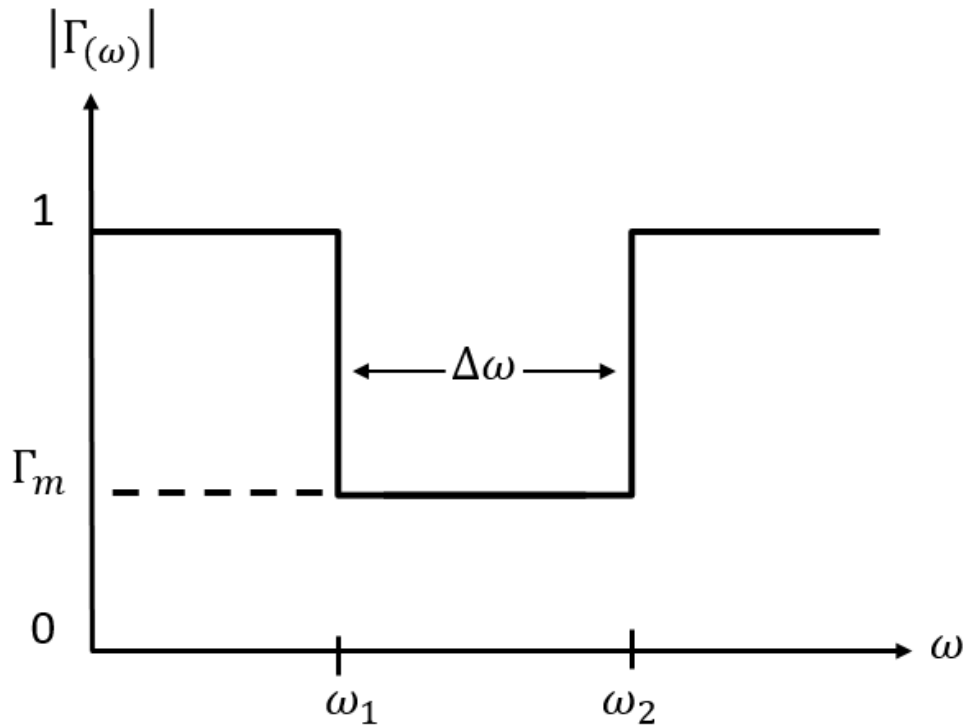


Figure 4.7 A possible reflection coefficient response with a 2-port matching network for a series passive RC [15]

Where $\omega_0 = \sqrt{\omega_1\omega_2}$ is the geometric mean of the frequency band of interest. When an infinite number of matching sections is used in the matching network, the equality in (4.14) is satisfied. Hence, the magnitude of the threshold reflection coefficient in (4.14) can be written as:

$$\exp\left(\frac{-\pi\omega_0^2 RC}{\Delta\omega}\right) \leq |\Gamma_m| \quad (4.15)$$

Equation (4.15) demonstrates that the threshold reflection coefficient can be lowered at the expense of the smaller bandwidth. That is why the obtainable matching bandwidth using passive matching networks for ESA is very limited [16]. To overcome this limit and to increase the matching bandwidth of ESA, active matching techniques, i.e. using non-Foster components, were used and studied in the next sections.

4.2 Active Circuits Applied to Impedance Matching

Since the passive matching in an ESA is strongly limited by the gain-bandwidth constraint mentioned above and by the maximum achievable bandwidth constraint for a small-size antenna (given by Wheeler [1] and Chu [9]), active-matching technique has become a very attractive topic in the last years. Authors have taken advantage of the negative slope property provided by NF elements, and have tried to use it in order to compensate the reactance of the antenna, not only at one single frequency but also over larger bandwidths. A NF circuit is a two-terminal device which has an impedance function that does not obey the Foster’s reactance theorem [17]. This theorem states that for a lossless passive two-terminal device, the slope of its reactance (and susceptance) plotted versus frequency must be strictly positive.

As mentioned before, the unique NIC characteristic used to obtain broadband impedance matching for ESAs is the negative slope of its impedance when looking into the port connected to the antenna. In this way, the reactive part of the antenna impedance can be compensated over a wider frequency range. This concept is illustrated in Figure 4.8.a and b, where respectively a simple antenna modeled by a capacitor is matched by a passive inductance (a) and by using a negative capacitance (b) (i.e. non-Foster capacitance).

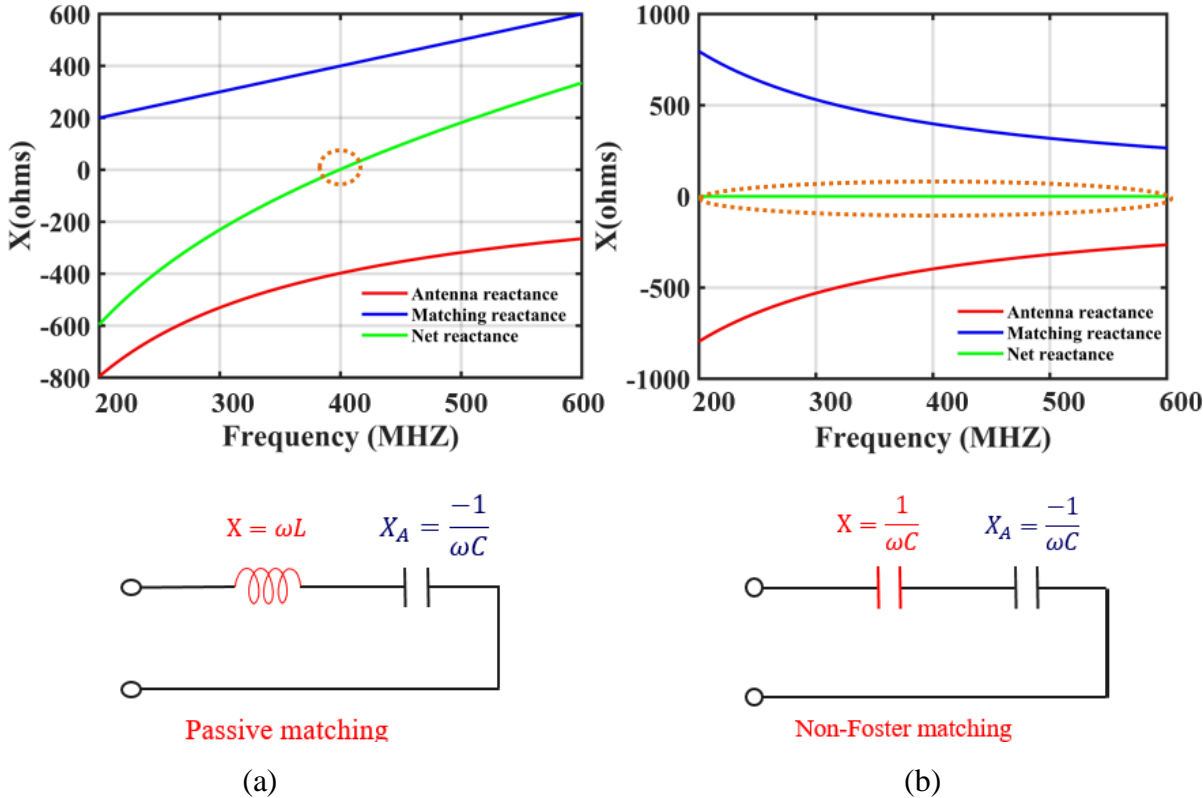


Figure 4.8 Comparison between (a) passive and (b) active matching for an ESA, represented as a series capacitor

When an ideal NF matching network is applied to an ESA to cancel out the net-reactance part of the antenna, the reflection coefficient of the antenna is then mapped onto the horizontal axis on the Smith chart. Note that, when the complex conjugate of a passive load is equal to the complex generator source impedance, it can transfer the maximum power to the passive load [18]. Even if the complex conjugate reactance of an ESA with NF matching networks is equal to that of the generator, there is still a mismatch between the two different resistances (the antenna with the real portion of the impedance and that of the generator; usually 50Ω) which can be matched using passive network. Hence, the efficiency and the antenna gain can be additionally increased.

In the next section, a methodology study is made upon three different ways of using Non-foster active matching along with passive matching in order to achieve wideband high efficiency antenna.

4.3 Methodology of combined Non-Foster and passive Broadband Matching Networks

In this section, three different topologies are studied and compared on how to use non-Foster matching along with passive matching in order to achieve a wideband high efficiency and electrically-small antenna.

- The first topology aims to match the antenna real part to that of the generator (i.e. toward 50 ohms), then the antenna reactance is cancelled using non-foster matching in order to realize a maximum power transfer from the generator to the antenna.
- Conversely, the second topology focuses first on cancelling the antenna reactance using non-foster matching, then on transferring the antenna real part towards 50 ohms. This approach has been already detailed and described in [19], [20].
- The third topology, that we propose, consists in decreasing the antenna quality factor by increasing the antenna real part using passive matching, after the antenna reactance is cancelled by using non-foster matching, and finally, a last passive network allows transferring the real part toward 50 ohms.

A comparison between these three topologies is performed on a planar monopole antenna and a discussion is carried out to highlight the drawbacks and limitations of each topology.

4.3.1 Conventional Monopole Antenna

Our study will rely on a planar monopole antenna, which was designed to resonate initially at 2.3 GHz. The antenna schematic and its simulated return loss are presented in Figure 4.9 while the antenna impedance simulated responses are given in Figure 4.10. The antenna is implemented on a 0.81 mm thick Rogers RO4003C ($\epsilon_r = 3.55$, $\tan(\delta) = 0.0027$) dielectric substrate with 0.035 mm thick copper metallization, the main dimensions of the printed monopole can be seen in Figure 4.9. As can be deduced from Figure 4.10, the antenna presents a high quality factor Q at low frequency due to a high reactance value compared to the real one that becomes small for $k.a < 0.5$, where “a” is the minimum radius of the radian sphere that cover the monopole antenna and is equal here to 12.5mm, which means that the antenna is considered ESA for frequencies below 1.9 GHz.

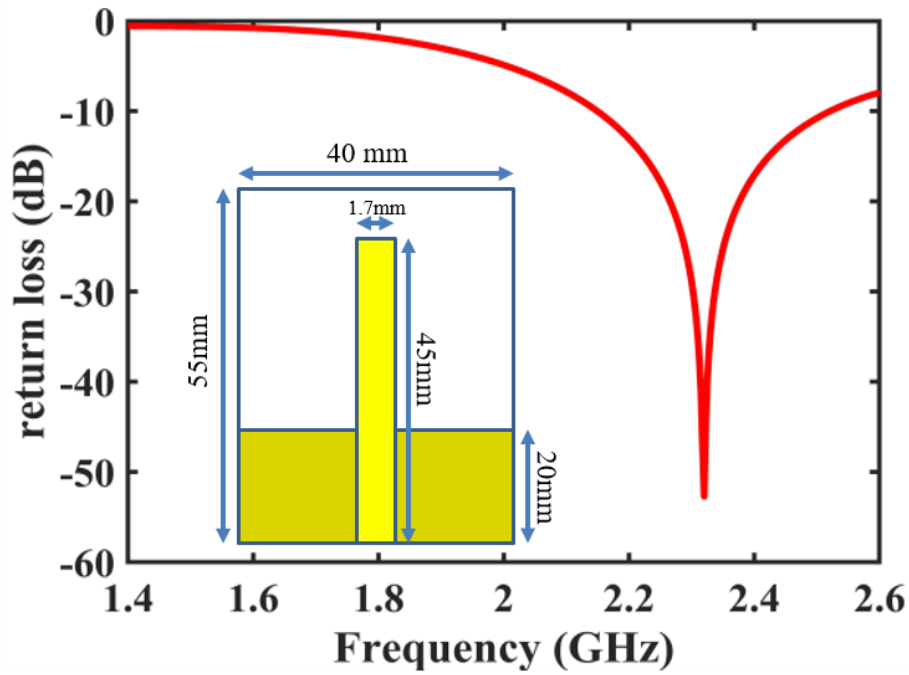


Figure 4.9 Antenna schematic and return loss

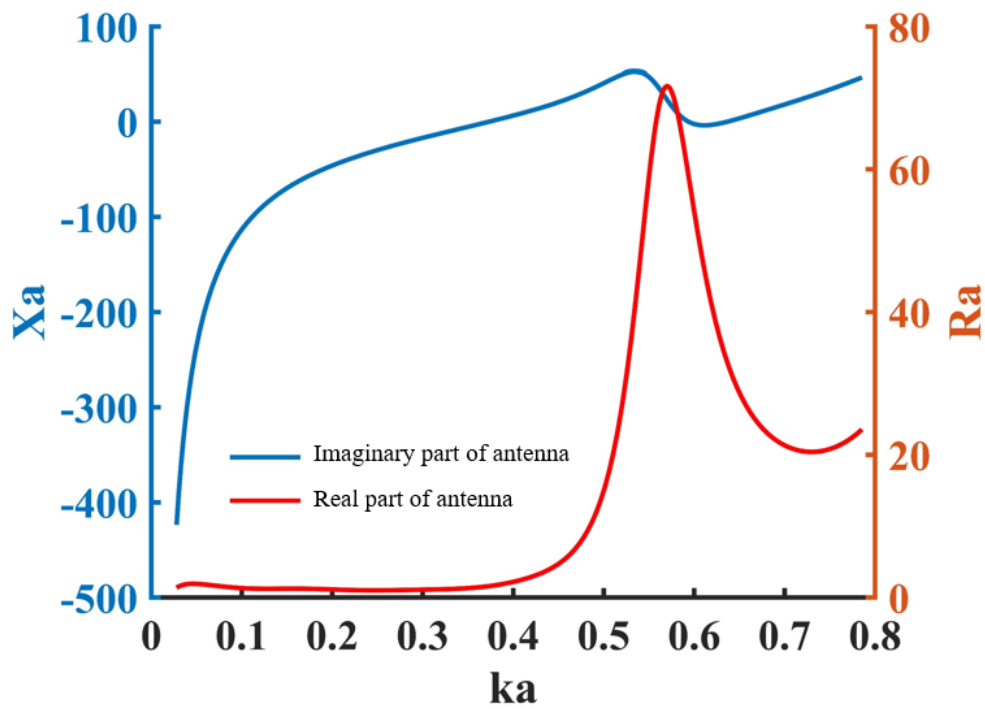


Figure 4.10 Antenna impedance (real and imaginary) parts

Our goal focus on decreasing the operating frequency to around 1.6 GHz (i.e. $ka = 0.4$), and on increasing its bandwidth by using a combination of passive and NF matching techniques. We willingly choose to match the antenna around 1.6 GHz and not below because at lower frequency the antenna has a very low radiation efficiency as seen in Figure 4.11.

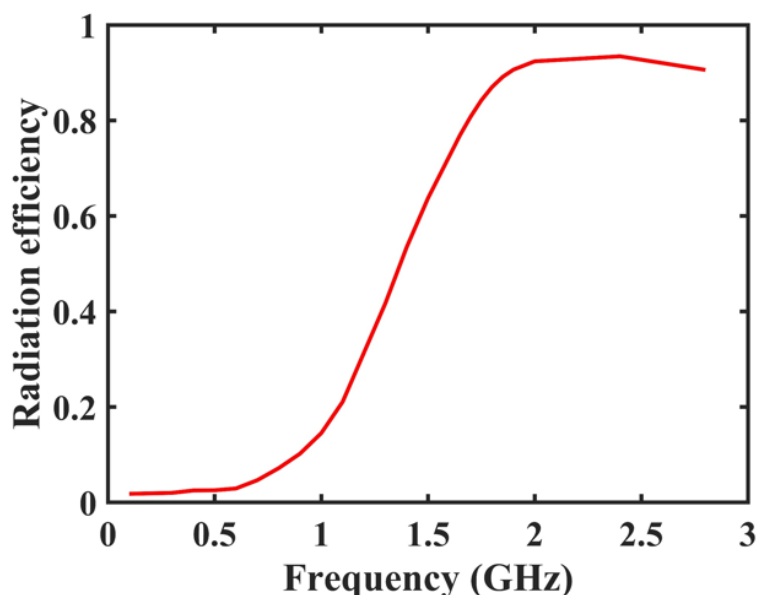


Figure 4.11 Maximum achievable antenna radiation efficiency

4.3.2 First Matching Topology: NF-Passive-Antenna

NF matching is initially used to cancel the reactive part of the antenna but is not sufficient for our antenna to be matched in the frequency band [1.5-1.7 GHz] (red curve in Figure 4.12 on Smith Chart). Indeed, the net impedance is far from the goal of VSWR less than 2 indicated by the blue circle in Figure 4.12 (i.e. any impedance within that 2-VSWR circle will lead to a power emitted from the source delivered to the load with a very little portion back scattered (10%)).

Therefore, to match the antenna, an increase of the real part is required. Figure 4.13 shows the real-part circles on Smith Chart with three different colored areas: red region corresponds to a real part between 0 and 25 Ω , the green region between 25 and 100 Ω , and the yellow area has a real part between 100 Ω and infinity.

If the antenna impedance gets inside the red region after using NF matching to cancel the antenna reactive part, a positive real resistor could be added in series to transform the net impedance within 2-VSWR area to complete the matching. Whereas, for an antenna impedance inside the yellow region, a negative resistance should be added in series to transfer the net impedance within 2-VSWR circle after canceling the reactive part. Nevertheless, adding a positive resistance is of course a wrong option leading to power dissipation and less power delivered to the antenna, and consequently the radiation efficiency of the whole system will decrease. On the other hand, adding a negative resistance is also not preferable because negative resistors are usually associated with a frequency dependent imaginary part, which in term will affect the matching bandwidth of the antenna. Finally, only the green area turns out to be relevant.

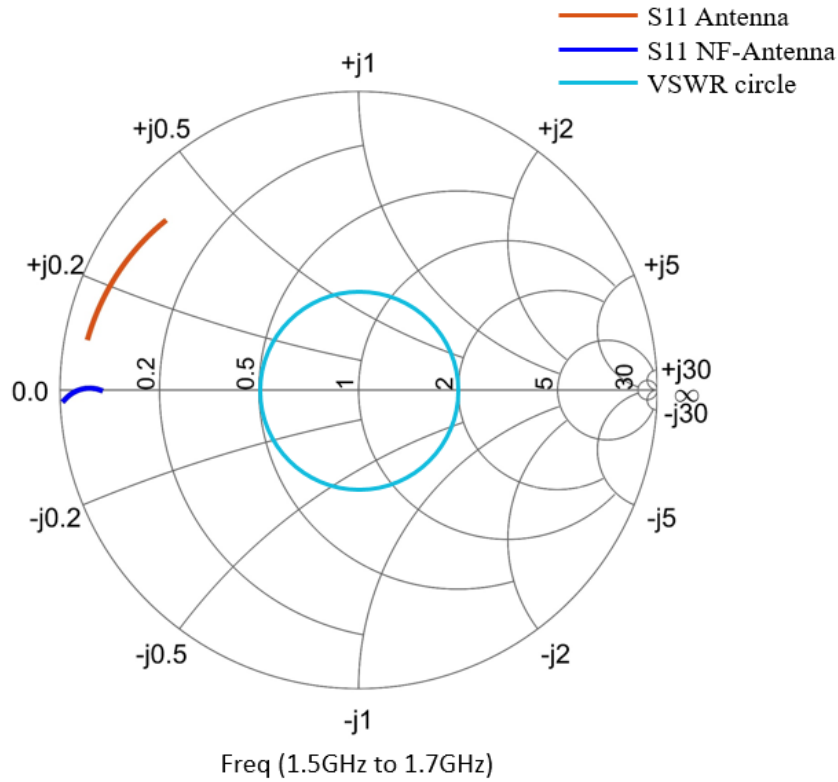


Figure 4.12 Antenna matching on Smith Chart

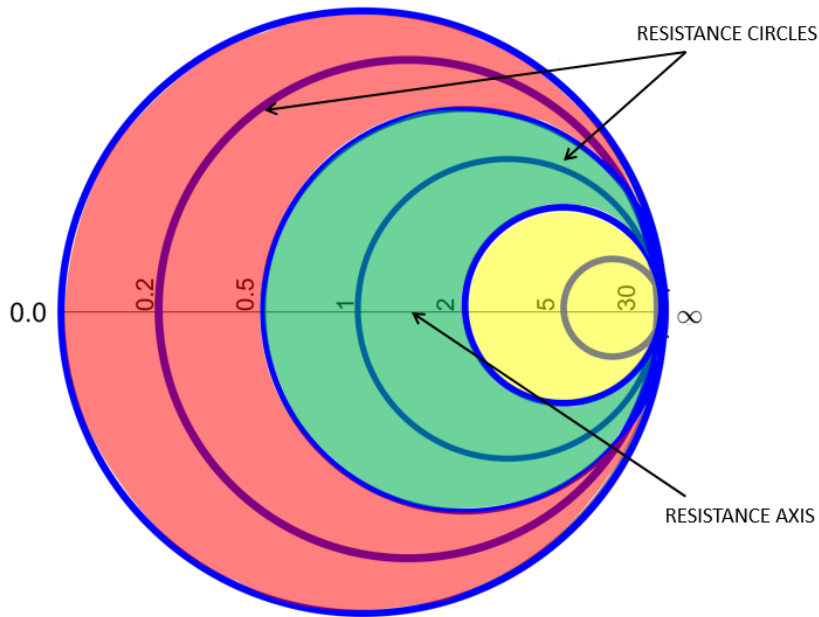


Figure 4.13 Resistance circles on Smith chart

Therefore, this requires transferring the antenna impedance inside the green region, and this can be done by using a passive matching network as seen in Figure 4.14.a. The values of the transformer are obtained by optimization in order to get a frequency range of the antenna real part as wide as possible inside the green region (red curve in Figure 4.15). Then, NF matching can be used to transfer the new impedance inside the 2-VSWR circle (yellow curve in Figure 4.15). It can be noticed that canceling the reactance part of the antenna associated with transformer system requires a parallel negative capacitance and negative

inductance in series with a negative capacitance and negative inductance as seen in Figure 4.14b. Their values were also optimized (Figure 4.14.b) and the step-by-step matching is shown in Figure 4.15 on Smith Chart.

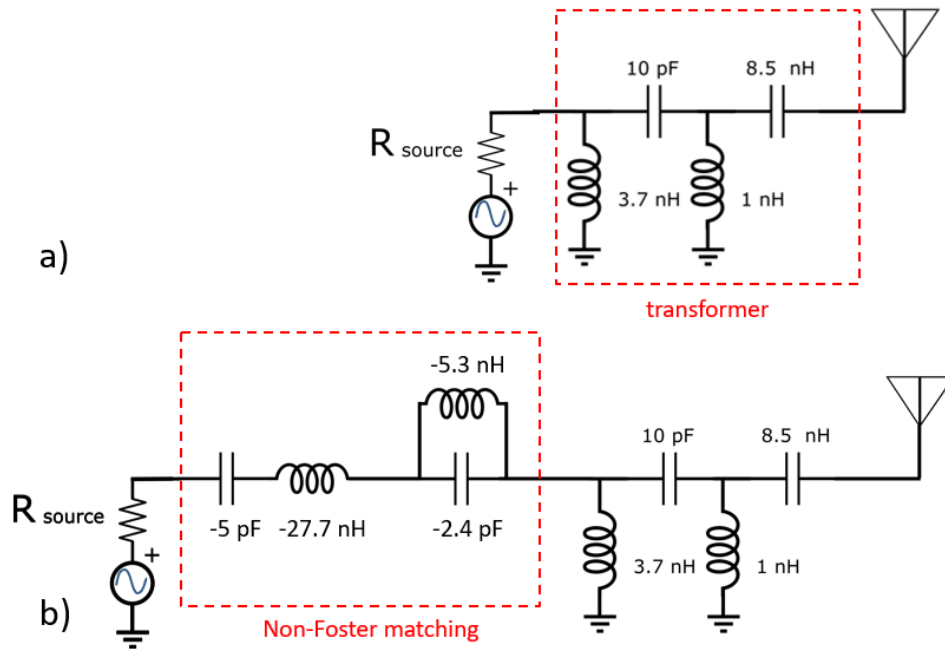


Figure 4.14 Antenna with Passive transformer (a), antenna with NF-Passive matching (b)

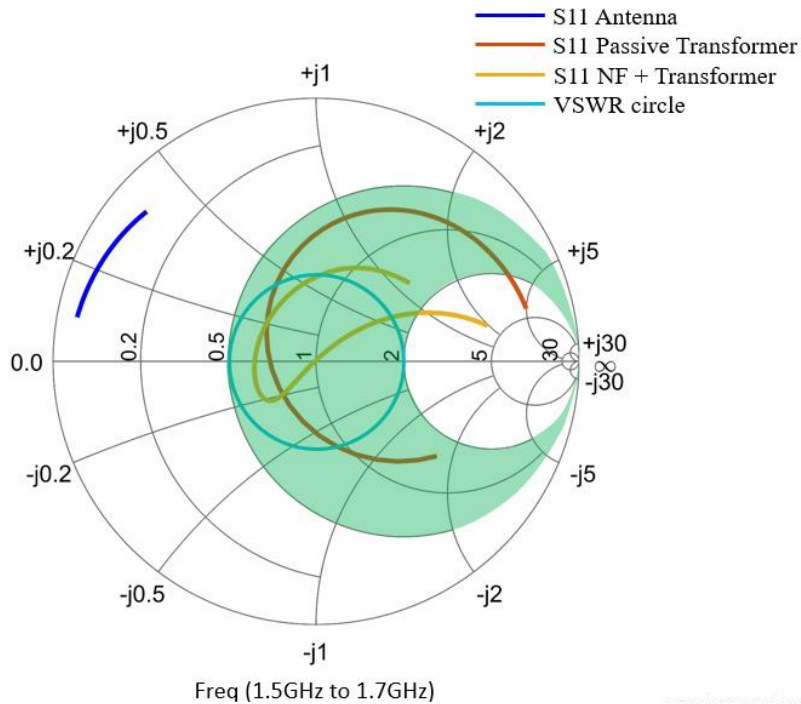


Figure 4.15 Antenna matching steps on Smith Chart

At this stage and before comparing to other combinations of passive and active networks we propose to compare this topology to a conventional multistage passive matching [21] in order to illustrate the bandwidth enhancement and matching improvements. 1 stage, 2 stages and 3 stages passive L-networks are used to increase the matching bandwidth of our antenna at low frequency range as seen in Figure 4.16. The values of the multistage passive elements are optimized to get an optimum return loss. As expected, Figure 4.17 illustrates that

using NF combined with passive matching provides a wider bandwidth compared to classical multistage passive matching, which confirms that NF matching can overcome the gain bandwidth limitation of an electrically small antenna regardless of its shape.

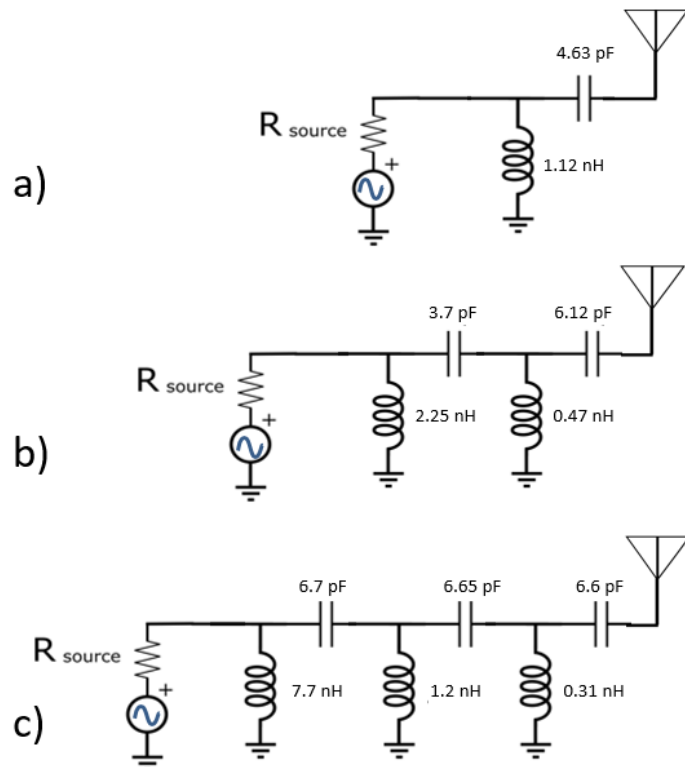


Figure 4.16 (a) One stage L passive matching (b) two stages L matching (c) three stages L matching

However, this topology is limited by how much the antenna impedance can be transferred within green area through passive matching, and how much active matching can cancel the reactive part to push the net impedance inside 2-VSWR circle. To overcome these limitations, a second topology that combines NF and passive matching in a different order [20] is put forward in next section.

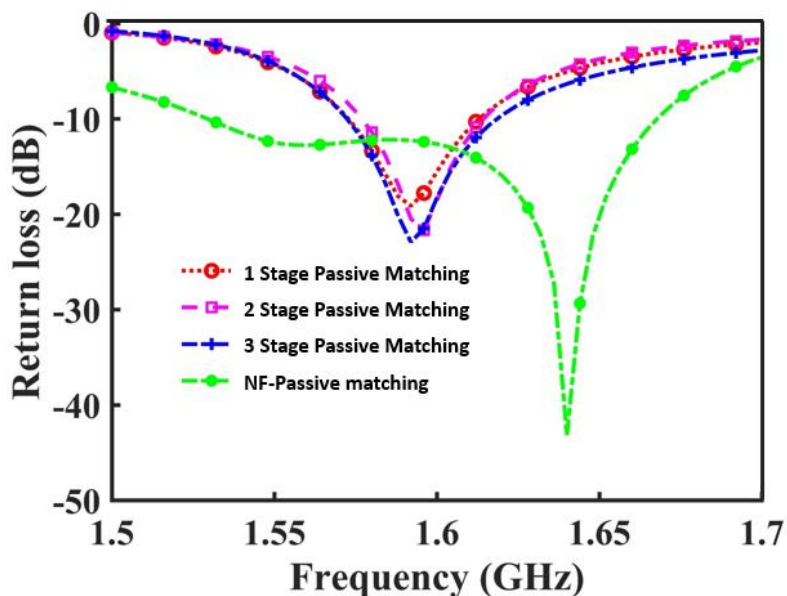


Figure 4.17 Multi-stage L-networks vs NF and passive matching

4.3.3 Second matching topology: Passive-NF-Antenna

As previously mentioned, multistage L-section passive matching is one of the simplest and widespread ways to widen the bandwidth of any load, but this method is efficient to widen the antenna bandwidth for purely resistive load (i.e. with null reactive part). However, in most practical applications with antenna loads, the antenna impedance includes a reactance part. Thus, the design procedure from [19]-[20] consists in canceling first the load reactance part and then in matching the remaining resistive component to the system impedance by using multi-stage passive matching to get a wide bandwidth. Canceling the reactance of the antenna will lead to lowering the quality factor and widening the bandwidth. The antenna quality factor Q is given by the following expression:

$$Q = \frac{Im(Z_{\text{matching circuit}}) + Im(Z_{\text{antenna}})}{Re(Z_{\text{matching circuit}}) + Re(Z_{\text{antenna}})} \quad (4.16)$$

When X_{Antenna} or $Im(Z_{\text{antenna}})$ is reduced or compensated by X_{circuit} or $Im(Z_{\text{circuit}})$, Q will decrease, leading to an increase of the antenna bandwidth (according to Yaghjian and Best [10] criterion). In order to identify and quantify the antenna reactance to be canceled, an inductor with a capacitor and a resistor in series are used as equivalent circuit to model the antenna (Figure 4.18.a). The reactance part can then be compensated by NF, leaving only net real impedance (Figure 4.19). The next step consists in using passive matching to transform the net impedance from NF matching of the antenna to 50Ω (Figure 4.18.c). The values for the passive matching networks were optimized to widen the matched bandwidth. Figure 4.20 presents the overall return loss obtained by this method.

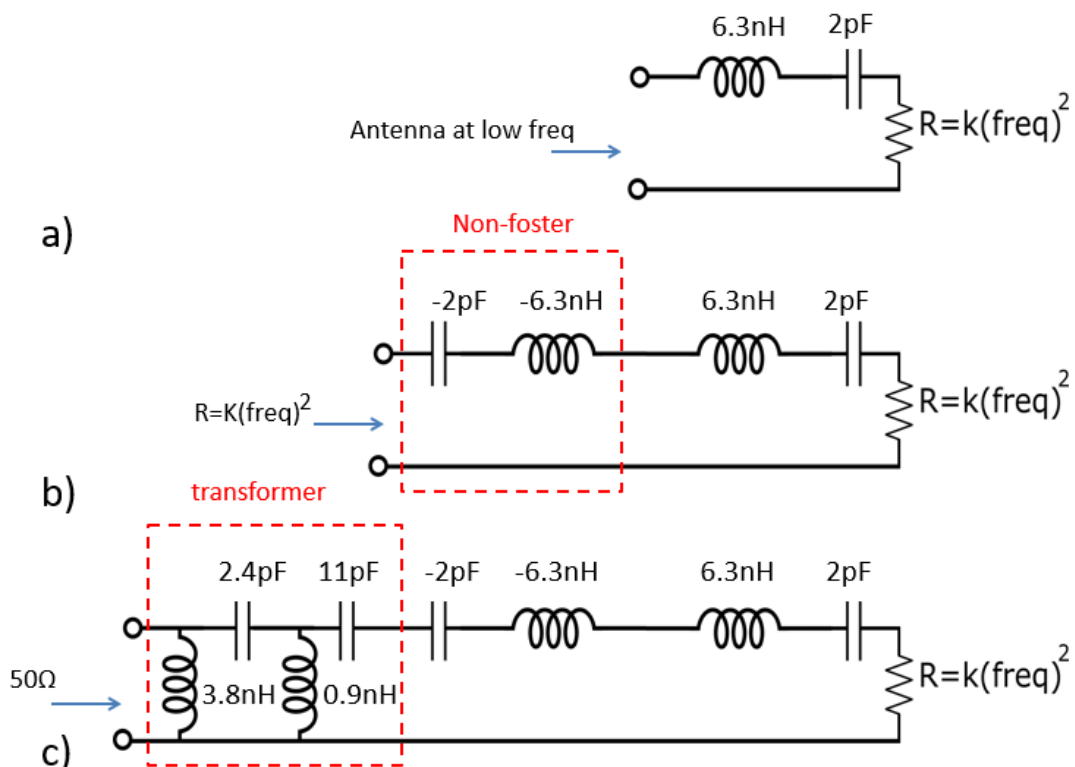


Figure 4.18 Antenna model at low frequency (a), NF reactive part compensation (b), complete matching (c)

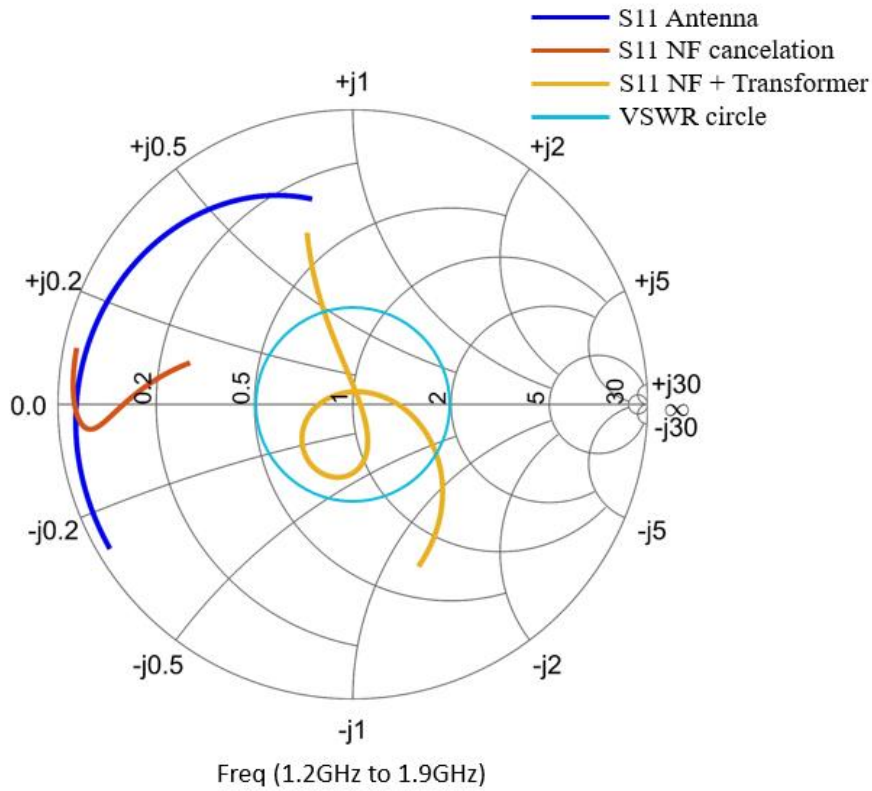


Figure 4.19 step by step matching on Smith Chart

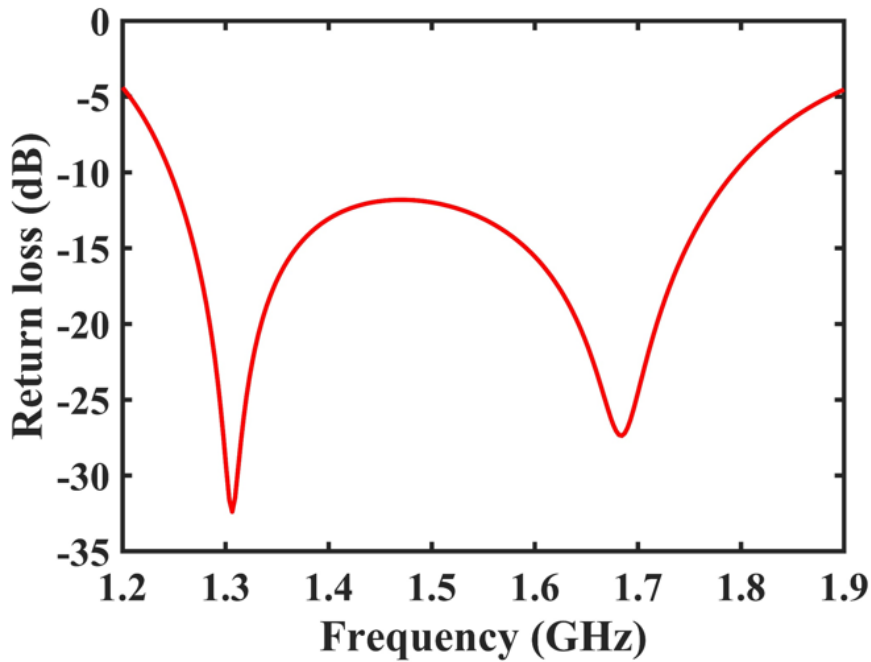


Figure 4.20 Passive-NF matching

Once more, the limit of this topology relies on how much and over which bandwidth can NF matching cancel the antenna reactive part which further allows the complementary task of passive matching to be effective. Moreover, decreasing the quality factor of the circuit in order to get a wide matching bandwidth still require multistage of L-networks. The third topology, that we put forward, merges the first two topologies and allows better performances in terms of matching bandwidth and efficiency.

4.3.4 Proposed matching topology: Passive-NF-Passive-Antenna

This proposed topology targets first a decrease of the antenna quality factor by using passive matching (i.e. by increasing the antenna resistive part). Second the reactive part is cancelled by introducing NF matching leading to decreasing more the quality factor. Finally, using passive matching allows shifting the input impedance around 50Ω . The topology steps are shown in Figure 4.21 and the corresponding impedances are plotted step-by-step on Figure 4.22. It can be noticed that by using first a passive matching circuit the antenna real part is increased by only 5Ω , because a larger increase will make it more difficult for active matching to cancel its reactive part. Furthermore, the effect of the second step (NF canceling) is clear in Figure 4.22 as the input impedance curve gets close to the real axis of the Smith Chart. Finally, a single L-section passive matching circuit is required to shift this impedance inside the 2-VSWR circle.

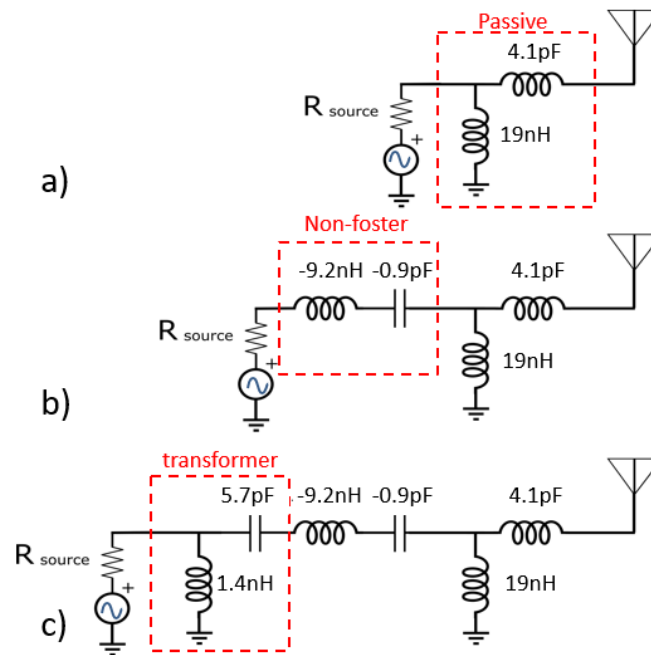


Figure 4.21 Illustration of the step-by-step matching using the 3rd topology (a) Passive matching, (b) Non-Foster matching, (c) Passive transformer

A comparison of the return loss between our proposed topology using passive-NF-passive matching sections and previously described topologies is shown in Figure 4.23. The third approach which merges the first two techniques together (i.e. it changes the antenna real part and cancels the reactive part like the first topology, and then it transfers the net impedance toward 50Ω just like the second topology) leads to the wider matched bandwidth. The method relies on the quality factor analysis (defined as the absolute ratio of the net reactance of the matching system to the ratio of its real part), which leads to a lower value compared to the first two topologies as shown in Figure 4.24. Note that Q-plot agrees perfectly with the return loss bandwidth graph. In addition, Table 4.1 shows the comparison between the bandwidth of the three topologies and the conventional passive matching and it confirms that our proposed topology gives a wider bandwidth compared to other matching approaches.

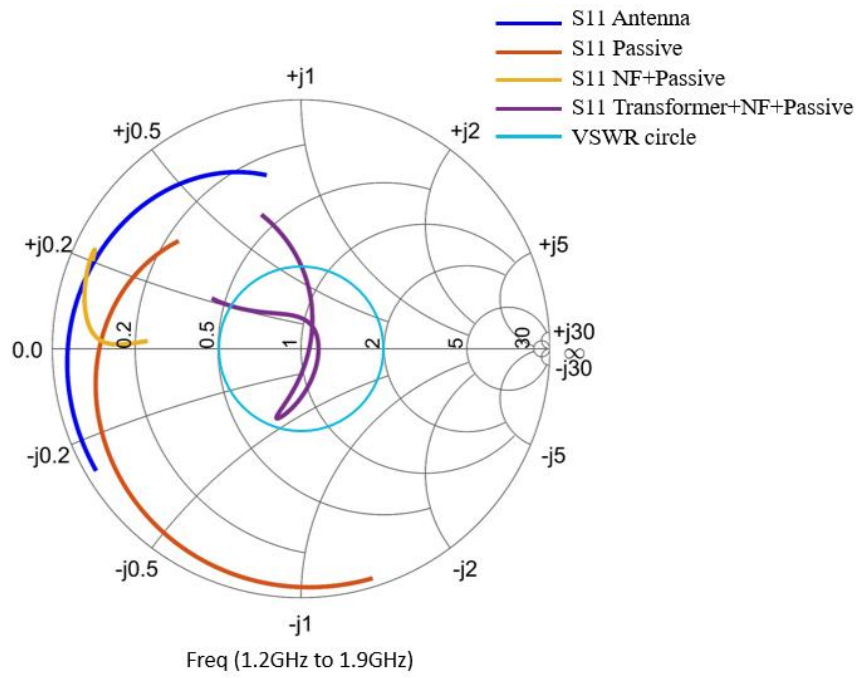


Figure 4.22 Step-by-step wideband matching for the 3rd topology

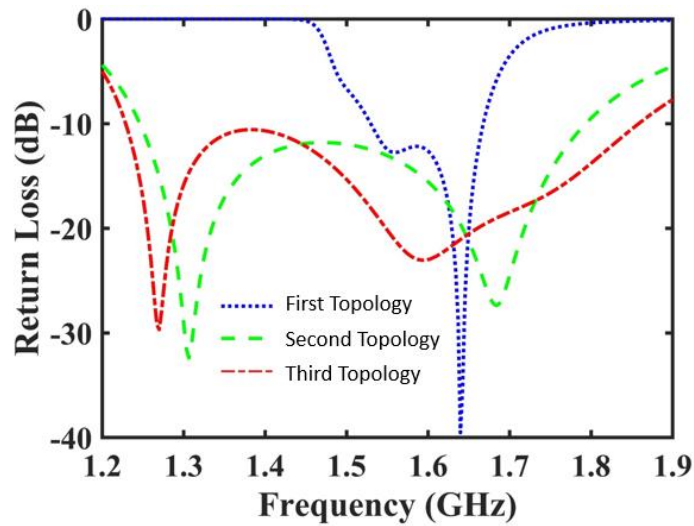


Figure 4.23 Comparison between the three topologies

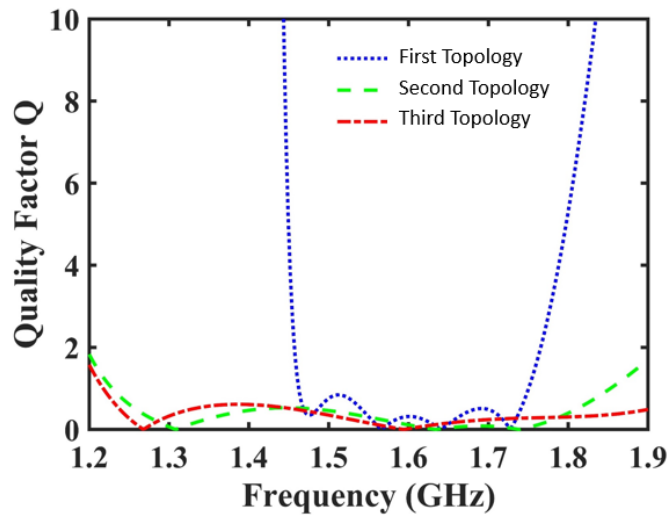


Figure 4.24 Comparison between quality factors of the three topologies

Table 4.1 Bandwidth comparison between different matching topologies

Topology	Bandwidth	Fractional Bandwidth
1 Stage Passive	0.028GHz	1.75%
2 Stage Passive	0.042GHz	2.62%
3 Stage Passive	0.061GHz	3.81%
First Topology	0.142GHz	8.87%
Second Topology	0.558GHz	37.2%
Third Topology	0.622GHz	41.46%

Our proposed topology limits depend on how much NF matching can perfectly cancels the reactive part obtained after adding the passive matching network. Antenna impedance matching (i.e. S_{11}) provides a necessary but insufficient requirement to ensure a satisfactory efficiency of the whole system. Indeed, it's of prime interest to estimate, compare and validate also the whole system radiation efficiency as done in the next section.

4.3.5 Topologies Comparison and Discussion

We suggest the introduction of a factor that we called “Total Transmission Coefficient”, TTC. This factor is the ratio of the delivered power to the antenna over the provided power by the source as illustrated by Figure 4.25 and as defined by Equations (4.18) and (4.19). This factor gives a rough value of the radiating efficiency of our system, which is rigorously defined as the ratio of the effective radiated power to the input power of the source as:

$$Eff \text{ Radiated} = \frac{\text{Power Radiated}}{\text{Power Incident}} \quad (4.17)$$

The TTC can be expressed as:

$$TTC = \frac{\sqrt{|b_2|^2 - |a_2|^2}}{\sqrt{|a_1|^2}} \quad (4.18)$$

$$TTC = \frac{\sqrt{|S_{21}|^2 * (1 - |\Gamma_{load}|^2)}}{|1 - S_{22} * \Gamma_{load}|^2} \quad (4.19)$$

If our matching circuit is perfectly lossless and the load is perfectly matched, then the TTC factor must be equal to one ($a_2 = \text{zero}$, and $b_2 = a_1$), meaning that all the source power is transmitted to the load. TTC presents the advantage of providing an idea about the efficiency of the whole antenna system including the matching network. Thus, there is no need to simulate the antenna with the matching circuit in CST or HFSS software (i.e. EM software) which is time consuming and therefore not calculated or presented in previous NF studies. Then, TTC can be used as targeted value by optimization algorithm of circuit simulation software (e.g. ADS from keysight) in order to increase the antenna efficiency and bandwidth.

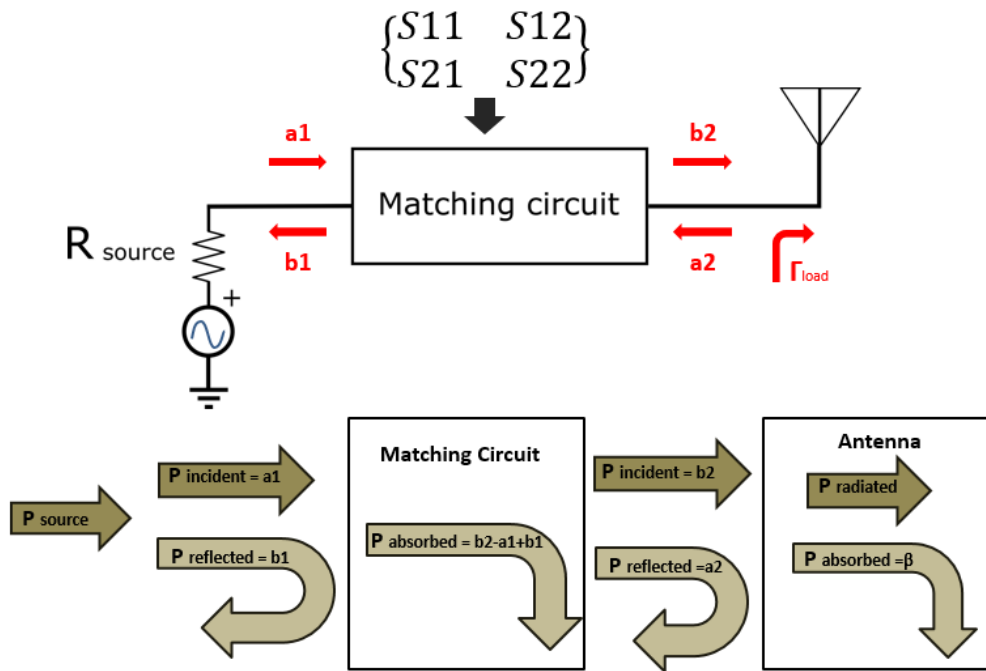


Figure 4.25 Incident and reflected waves at the matching circuit accesses

Figure 4.26 shows the calculated TTC of the three topologies. We can notice that using our passive-NF-passive matching topology provides a better result than the other two topologies. It must be noted that the radiated efficiency and TTC are related together by the following equation:

$$Eff\ Radiated = TTC - \beta \quad (4.20)$$

Where β accounts for the power absorbed inside the antenna, which can be divided in two parts: the first part is the loss resistance that transforms power into heat and the other part relies to the energy stored in its near field, which depends on the antenna reactive part. Regardless of the power loss, by calculating TTC we can know how much power is delivered to the antenna input and thus how much power is absorbed or reflected back by the matching circuit. The three curves have a maximum TTC value of 1, which means that, at these points, the power is being totally transferred to the antenna input port.

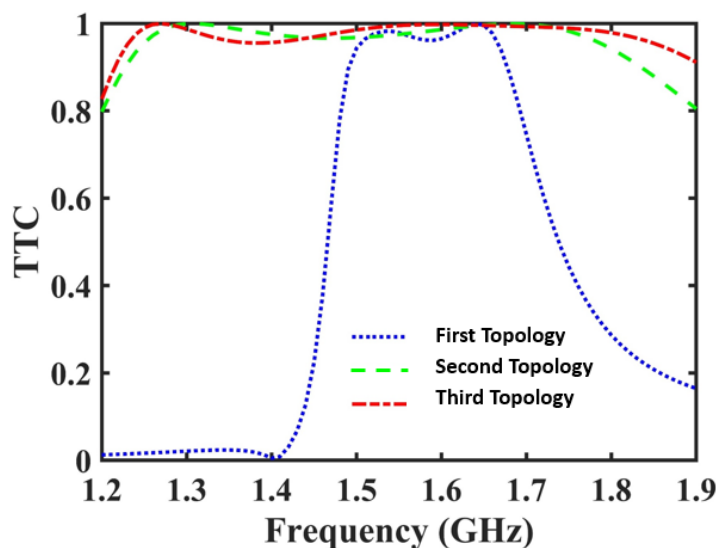


Figure 4.26 Comparison of TTC for the three topologies

Co-simulations between ADS and CST software have been done (Figure 4.27) in order to simulate the complete radiating efficiency and to compare it with TTC for the three topologies. It can be noticed that the three curves of the matching topologies are logically restricted within the maximal radiated efficiency of the antenna. Moreover, the efficiency of each system relatively to the maximum radiated efficiency fits with the TTC results and confirms the power delivered to the input port of the antenna. In addition, a global trend can be highlighted for all topologies: as we go lower in frequency the expected radiation efficiency of the antenna decreases, (i.e. the antenna quality factor increases). It means that losses inside the antenna will increase strongly at lower frequency. In other word, it is useless to try to match the antenna at very low frequency, because the power that is going to be delivered at the antenna input port would be mainly dissipated inside the antenna or even stored in its near field, while a very low percentage will be radiated whatever the matching network.

The obtained results show that our proposed topology (third topology) has a wider bandwidth and better radiation efficiency compared to the other two topologies. Hence, for the next section we are going to use our topology to match an antenna around 1.6 GHz. In the following section, we propose to implement this third approach for the realization of a broadband ESA dedicated to the intended Full-Duplex front-end.

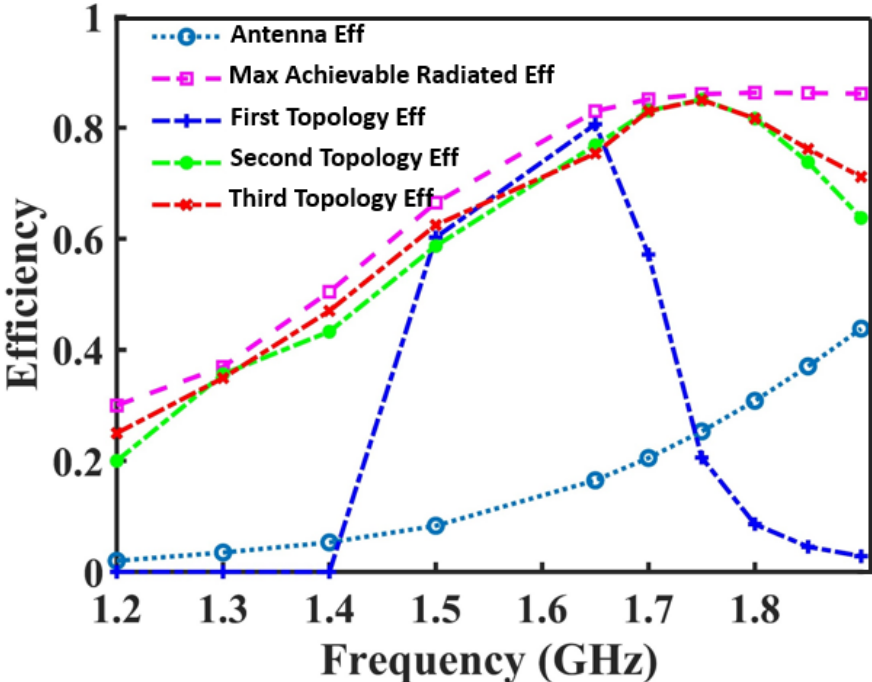


Figure 4.27 Efficiency of the system

4.4 Design of a Full-Duplex front-end dedicated to close and Electrically Small Antennas (ESA) by using NF circuits

Figure 4.28 recalls the Full-Duplex topology targeted in this project. This architecture proposal is dedicated to the implementation of a full-duplex wireless link in the case of small wireless object (e.g. IoT, ...) with two antennas (TX and RX) placed close to each other. As specified formerly, previous full-duplex proposals based on destructive interference (chap I) cannot be applied with only two antennas and in a position so close to each other. Additionally, the unsuitability of these techniques for our application is reinforced by the fact that TX and RX antennas should operate with the same linear polarization. Thus, we put forward the use of Non-Foster circuit as the key block to i) create a 180° phase shifter potentially tunable, ii) match the antenna at lower frequency and over a wide bandwidth to make it electrically small (i.e. leading to antenna miniaturization), and finally iii) isolate the two antennas to create the first level of self-interference cancellation at antenna level. As the first two goals have already been studied, we will focus in the following sections on matching and decoupling of two closely separated antennas. This study will start by matching and decoupling by using only passive elements and this first approach will serve as a comparison reference for the final proposal where active elements (i.e. NF) will be used.

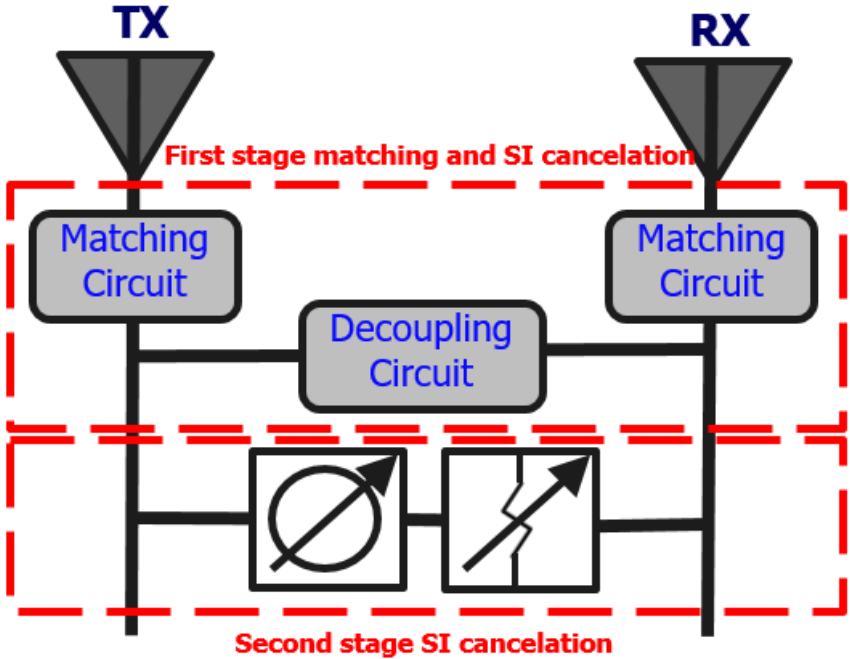


Figure 4.28 Proposed Full-Duplex system

4.4.1 Full Duplex Approach Using Passive Elements

Two closely separated monopole antennas having a resonance frequency of 2.3 GHz are used to achieve a Full-Duplex system. Figure 4.29 shows the return and insertion loss (S_{21} stands here for the antenna coupling) between the two monopoles. A matching and a decoupling networks are used to shift the resonance frequency towards 1.6 GHz and to achieve a good isolation level between them (decrease S_{21} level). Two topologies are compared: the first one, proposed in [22] in another context, is based on an implementation of the decoupling network close to the antennas and then of matching networks at the circuits outputs to shift down the resonance frequency. We suggest for the second one to switch the

networks order. Figure 4.30 shows the two topologies. The decoupling circuits consist of series combination of a resistive and a reactive element (R_d and X_d) while the matching networks use single L-sections (X_a and X_b). Since the two antennas are symmetric, then the matching components at both antenna feeds are the same.

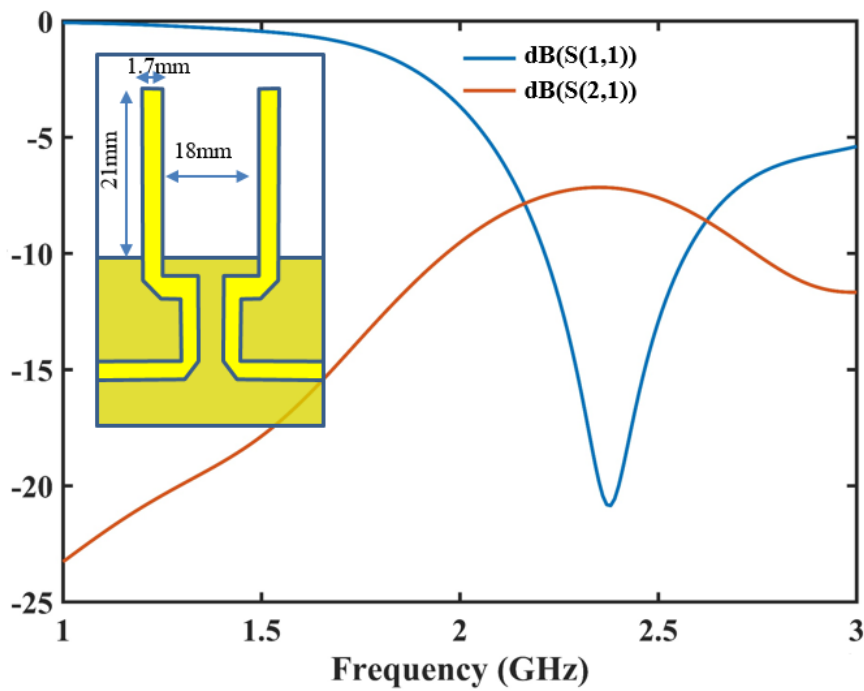


Figure 4.29 Return and insertion loss between two closely separated antennas

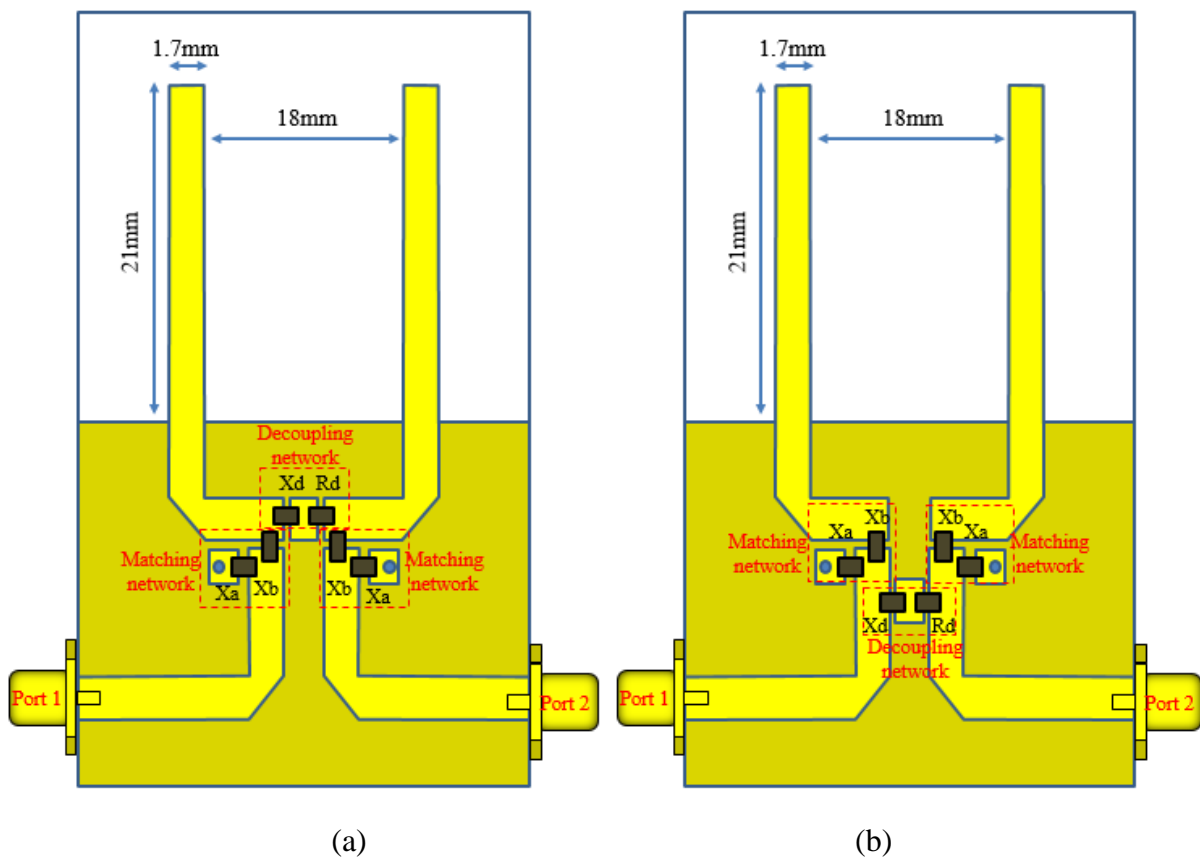


Figure 4.30 Schematic of two closely spaced monopoles as proposed in [22] (a), modified topology (b)

4.4.1.1 Analysis of topologies

A two port-network representation of the two topologies is given in figure 4.31, where an even-odd mode analysis is carried out in order to solve a system of perfectly matched and decoupled system. Figure 4.32 shows the even-odd representation of both topologies, where $Z_{in, even}$ and $Z_{in, odd}$ of both topologies are calculated as follows:

$$Z_{in, even, ref topology} = \frac{(X_a)(X_b + Z_{11} + Z_{21})}{X_a + X_b + Z_{11} + Z_{21}} \quad (4.21)$$

$$\begin{aligned} & Z_{in, odd, ref topology} \\ &= \frac{(X_a)(X_b(2(Z_{11} - Z_{21}) + X_d + R_d) + (Z_{11} - Z_{21})(X_d + R_d))}{(X_a + X_b)(2(Z_{11} - Z_{21}) + X_d + R_d) + (Z_{11} - Z_{21})(X_d + R_d)} \end{aligned} \quad (4.22)$$

$$Z_{in, even, modified topology} = Z_{in, even, ref topology} \quad (4.23)$$

$$\begin{aligned} & Z_{in, odd, modified topology} \\ &= \frac{(X_d + R_d)(X_a)(X_b + Z_{11} - Z_{21})}{(2X_a + X_d + R_d)(X_b + Z_{11} - Z_{21}) + (X_d + R_d)(X_a)} \end{aligned} \quad (4.24)$$

Where Z_{11} , and Z_{21} stands for the two monopole impedances as seen in figure 4.30. From $Z_{in, even}$ and $Z_{in, odd}$, we can calculate Z_{11} and Z_{21} for the whole system from:

$$Z_{11, whole system} = \frac{Z_{in, even} + Z_{in, odd}}{2} \quad (4.25)$$

$$Z_{21, whole system} = \frac{Z_{in, even} - Z_{in, odd}}{2} \quad (4.26)$$

Thus, the input return loss and transmission coefficient of the whole systems are given as follows:

$$\begin{aligned} & S_{11, whole system} \\ &= \frac{(Z_{11, whole system} - 50)(Z_{21, whole system} + 50) - Z_{21, whole system}^2}{(Z_{11, whole system} + 50)(Z_{21, whole system} + 50) - Z_{21, whole system}^2} \end{aligned} \quad (4.27)$$

$$\begin{aligned} & S_{21, whole system} \\ &= \frac{100 * Z_{21, whole system}}{(Z_{11, whole system} + 50)(Z_{21, whole system} + 50) - Z_{21, whole system}^2} \end{aligned} \quad (4.28)$$

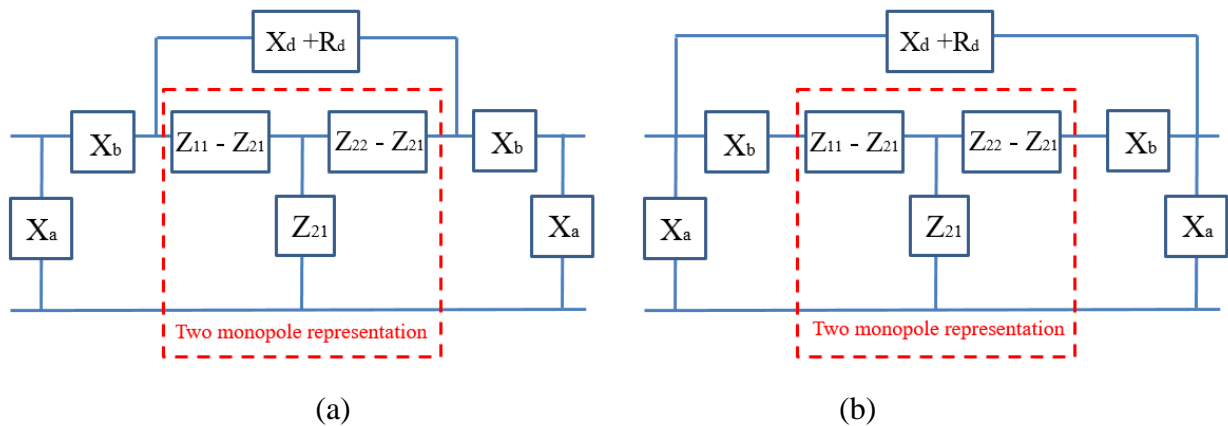


Figure 4.31 two-port network representation of reference topology (a), and modified one (b)

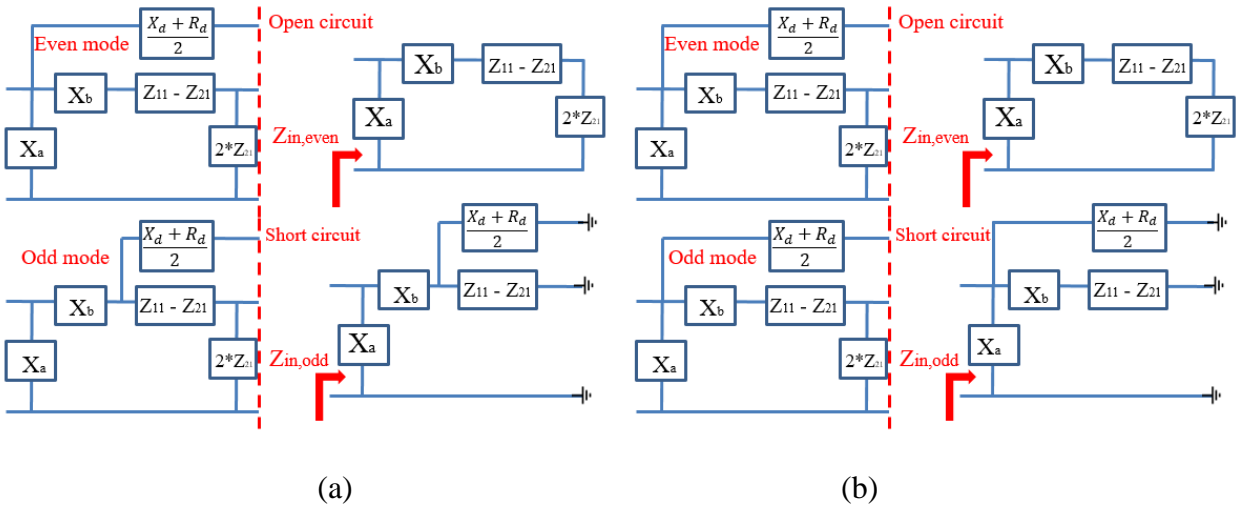


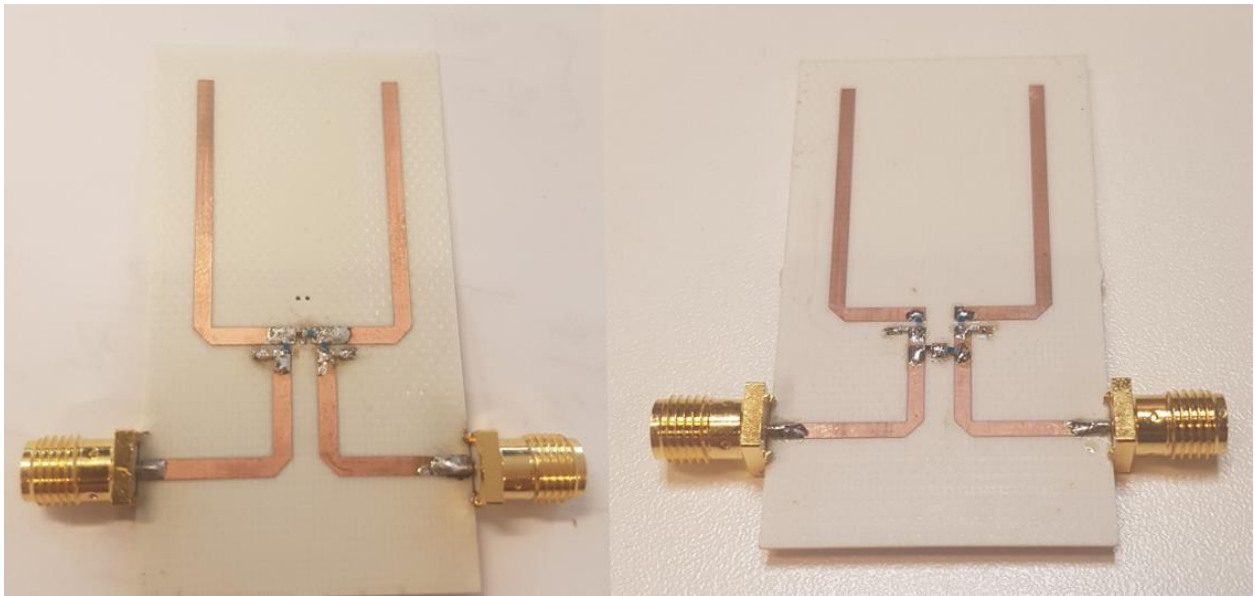
Figure 4.32 even odd mode representation of reference topology (a), and modified one (b)

For perfect matching and perfect decoupling, S_{11} and S_{21} must both be equal to zero in linear scale. Solving these two equations and dividing them into real and imaginary part will provide four equations equal to zero with four unknowns (i.e. X_d , R_d , X_a , X_b) which means that the system can be solved. It must be noted that solving the system with condition of perfectly matched and decoupled may not give acceptable or physical solutions. Thus, we suggest solving numerically the system as inequalities (i.e. $0 \leq S_{11} < 0.1$ and $0 \leq S_{21} < 0.1$). Moreover, after finding the best values for each topology, a slight tune is applied to take into account the effect of the transmission lines.

The system is solved first at the original resonance frequency of the antenna (i.e. 2.3GHz) as what was made in the original paper [22]. Then, we re-solve the system at our desired frequency (i.e. 1.6GHz). The corresponding simulation and measured results are discussed in the next section.

4.4.1.2 Simulations and Measured Results

Figure 4.33 shows the manufactured structure of both reference and modified topologies. Table 4.2 summarizes the calculated value of each element used in both topologies at 2.3GHz and at 1.6GHz. It must be noted that these values have been tune after calculation in order to take into account the effect of the transmission lines. This tuning step is done through co-simulation (distributed parts from EM associated to S-parameters of the lumped components). The simulation vs measured results are presented in Figure 4.34. From a global overview, it comes that simulated and experimental results show a good agreement with a slight frequency shift between measured and simulated results. This probably comes from a high sensitivity level of these topologies in function of the tolerance of passive elements. Both topologies are able to provide an isolation level around -20dB, which is less than expected in simulation but consistent with value obtained in [22]. We can conclude from Figure 4.34 that the modified topology shows a much wider isolation range compared to the reference topology at both frequencies.



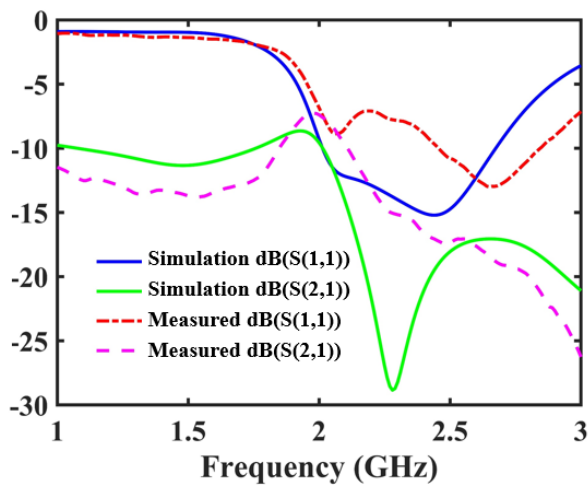
(a)

(b)

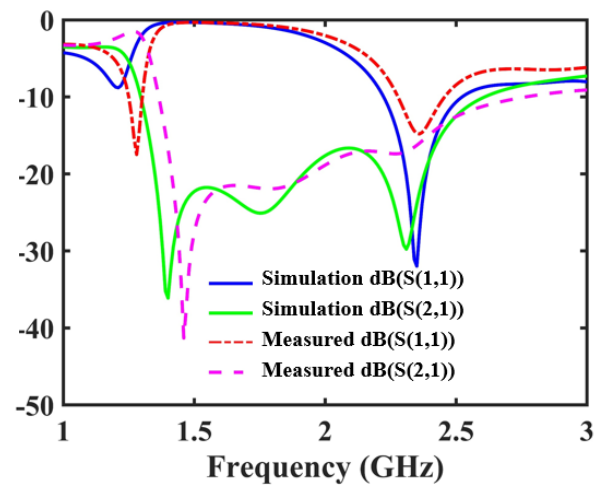
Figure 4.33 manufactured structure of reference topology (a), and modified one (b)

Table 4.2 Component Values for each topology

Components	Matching network		Decoupling network	
	X_a	X_b	X_d	R_d
Ref. Topology at 2.3GHz	1.4pF	1.9nH	1.5pF	20 Ω
Modified Topology at 2.3 GHz	1.5pF	1.7nH	2.7nH	4 Ω
Ref Topology at 1.6GHz	4.7pF	3.9nH	8.7nH	10 Ω
Modified Topology at 1.6 GHz	4.9pF	3.8nH	3.6nH	11 Ω



(a)



(b)

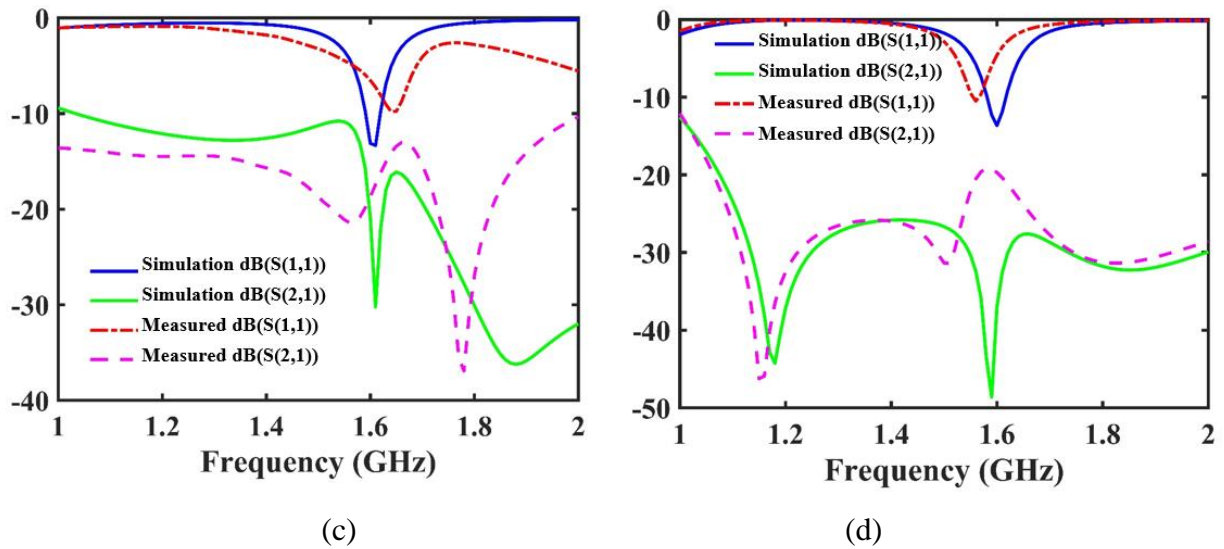


Figure 4.34 Manufactured structure of reference topology at 2.3 GHz (a), and modified one at 2.3 GHz (b), reference topology at 1.6 GHz (c), and modified one at 1.6 GHz (d)

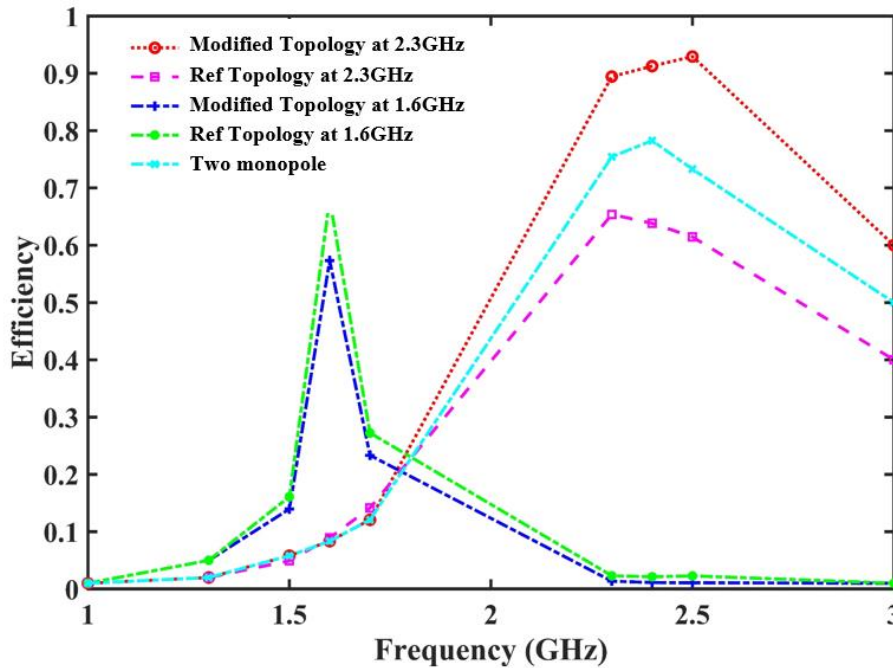


Figure 4.35 Simulated Efficiency of the five configurations

It should be noticed once again that S_{11} is not sufficient to characterize the antenna behavior. It's of prime interest to simulate and measure the efficiency of each system. Figure 4.35 presents the efficiency of the five cases under consideration (i.e. the two monopoles, the reference and modified topologies at 2.3 GHz and 1.6 GHz).

Globally, the modified topology exhibits an almost equivalent or higher efficiency than the initial one. The efficiency seems to be depended on the value of the resistor R_d . Indeed, looking simultaneously at Table 4.2 and Figure 4.35 clearly shows that for higher values of R_d the efficiency is decreased. Physically, it means that in the case of the modified topology, and particularly at 2.3 GHz, a higher contribution of the decoupling level is due to the reactive part than for the reference one. Thus, a lower value of R_d is required and then less power is dissipated in that decoupling resistor. Moreover, the better efficiency observed at 2.3 GHz for

the modified topology compared to two monopole antennas (i.e. without matching and decoupling) can also be explained as a reduced coupling level that is translated as gain in the efficiency.

All these results are confirmed in Figure 4.36.a that shows the increase in realized gain between the reference topology and the modified one with respect to the original two monopoles. At 1.6 GHz, both topologies have higher gain compared to the original two monopole antennas. At 2.3 GHz, the new topology confirms a higher realized gain value compared to the other architectures (Figure 4.36.b). As the initial efficiency is already high at 2.3 GHz, the improvement is not so awesome.

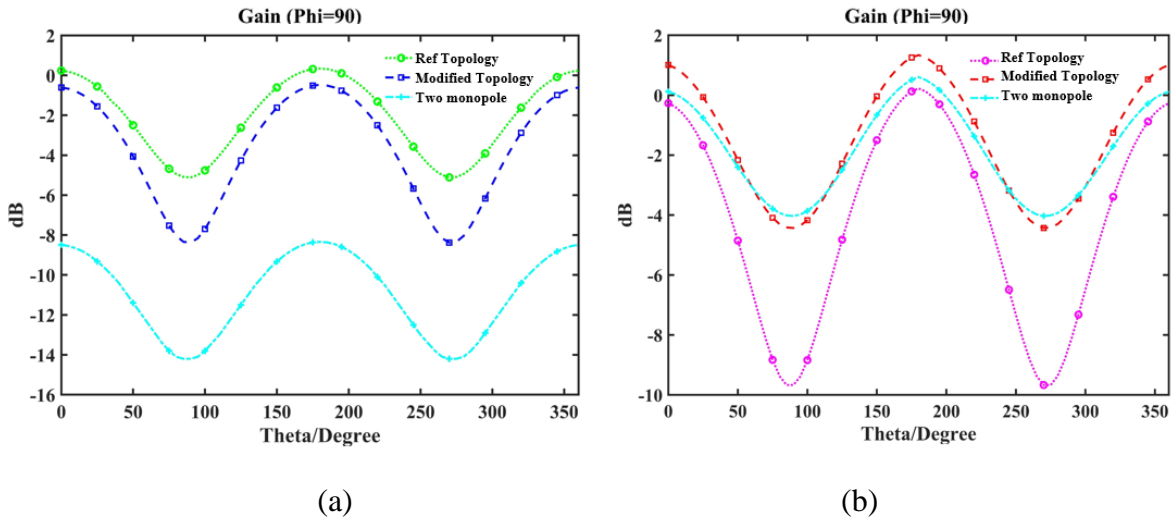


Figure 4.36 Realized Gain comparison between two monopole, reference topology, and modified one at 1.6 GHz (a), and 2.3 GHz (b)

This analysis and the associated experimental results clearly indicates that it is possible to create an ESA (i.e. to reduce the antenna size) and to isolate TX and RX antennas using only passive elements. However, in that case (here at 1.6 GHz), the obtained bandwidth is narrow. With the aim of improving the operating bandwidth and the decoupling band and level, the next section will address the implementation of Non-Foster element to match and decouple two closely separated antennas at low frequency.

4.4.2 Full Duplex topology using non-Foster elements

In this section, we will focus on using non-Foster topology to match and decouple two closely separated planar monopole antennas. The first part will address the wideband matching of a monopole antenna around 1.6 GHz, and the next part will be on matching and decoupling of the two monopole antennas and will give a comparison of the results obtained with NF to passive ones.

4.4.2.1 Non-Foster matching of one monopole antenna

A non-Foster circuit based on a XCP (Linville's circuit) as previously introduced in Chapter 2 and implemented in Chapter 3 is used here to match a 2.3 GHz monopole antenna around 1.6 GHz. Figure 4.37.a, b and .c respectively shows the antenna with the Non-Foster circuit, the corresponding layout and the photo of the fabricated circuits. In Figure 4.37.a, the current flow is depicted by red arrows to show how the current path is inverted between the port of the capacitance to invert (C_{invert}), which leads to generate a negative capacitance. A SKY6505 transistor was (SKY6505) used as in Chapter 3 in order to get a stable behavior. L_b

was chosen to be 220nH and $C_b = 1000\text{pF}$, $V_b = 2\text{V}$. Figure 4.38.a shows the simulated current path using CST software at 1.6GHz frequency, and confirms an inverted current path between the two ports of the capacitance to invert and consequently obtain a negative capacitance.

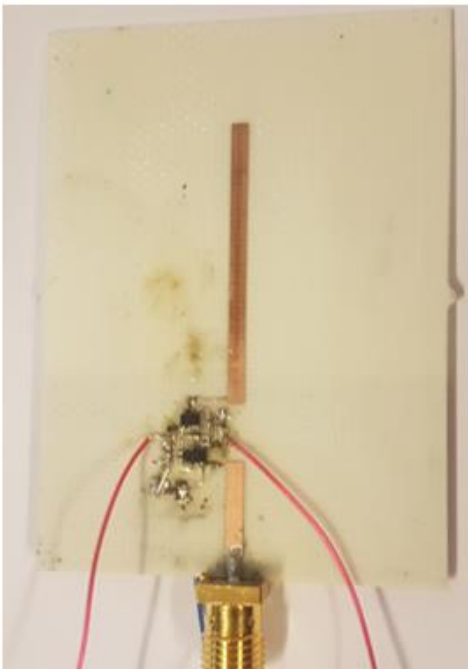
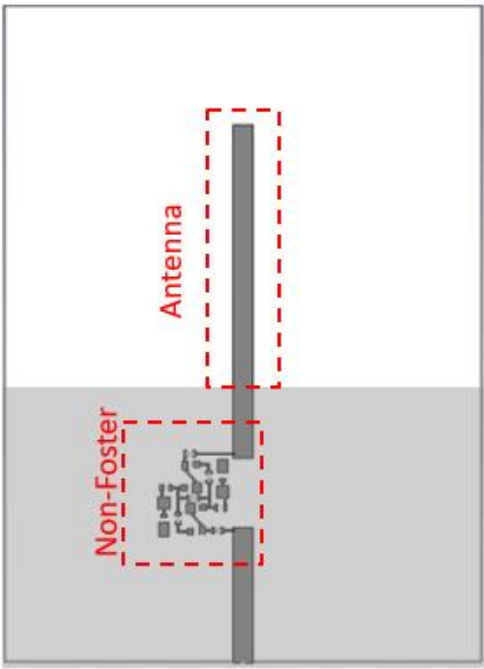
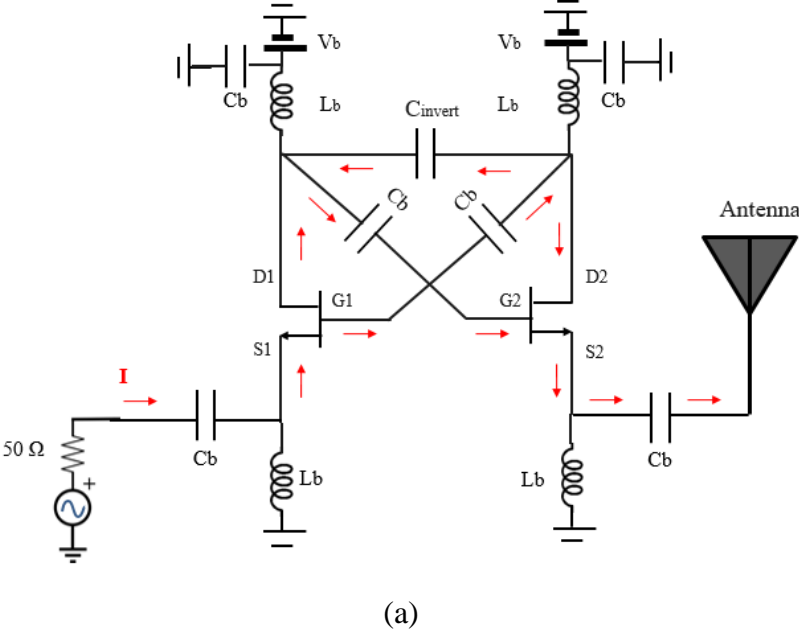
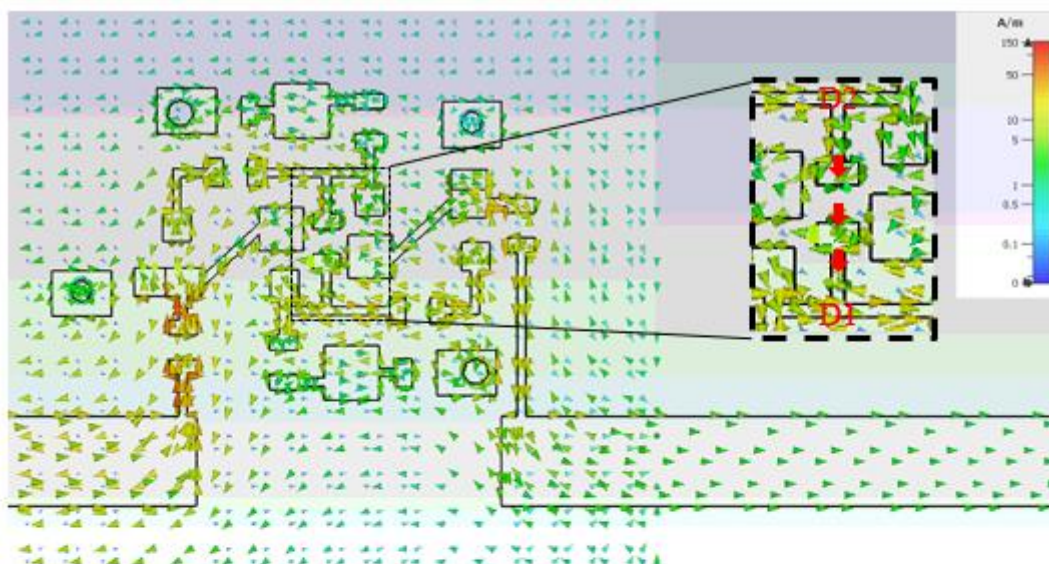
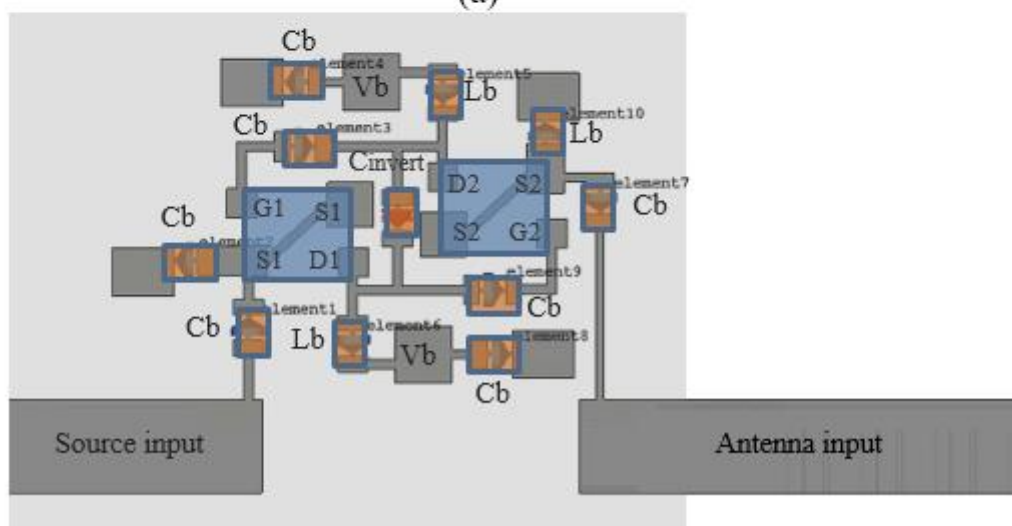


Figure 4.37 Schematic of Non-Foster circuit with antenna showing the current path (a), the corresponding layout (b), and the photo of the fabricated one (c)



(a)



(b)

Figure 4.38 Surface current distribution at 1.6GHz (a) geometry of non-foster circuit and antenna with all the associated elements (b)

The original antenna is intrinsically matched at 2.3GHz with a 17% fractional bandwidth. Figure 4.39 shows the simulated and measured return loss when the antenna is matched at 1.6 GHz by using non-Foster circuit. It can be noticed that the antenna is matched in the 1 GHz-2.5 GHz band resulting in a fractional bandwidth of 93% in simulation.

Globally, the measurements are in good agreement with the simulated results, moreover, as previously encountered, a frequency shift had been witnessed, and that may be due to the tolerance effect of the lumped element used in the Non-Foster circuit. Figure 4.40.a shows the simulated reactance cancelation (co-simulation) of the antenna using Non-Foster circuit. A value of 2pF was chosen to be inverted in order to ensure the system to be stable and to reduce the antenna reactance part around 1.6 GHz. But, as evidenced in figure 4.40.b , non-Foster circuit add a resistive value of around 20 Ω due to a residual resistive part of the non-Foster circuit This resistance will affects the radiation efficiency and leads to a lower gain. This resistance value greatly depends on the transistor transconductance g_m and was found to be close to $2/g_m$ in chapter 2. This value was confirmed experimentally in chapter 3 when we

have de-embedded the input impedance of the non-Foster circuit. Many attempts were tried (e.g. source and drain topologies in cascade, use of different transistors, ...) to reduce this spurious value but systematically failed due to stability issue. The radiation efficiency is shown in Figure 4.41, where it can be seen that the system has an overall efficiency which is lower than the original antenna efficiency. This is due to the power being dissipated in the resistance from NF circuit.

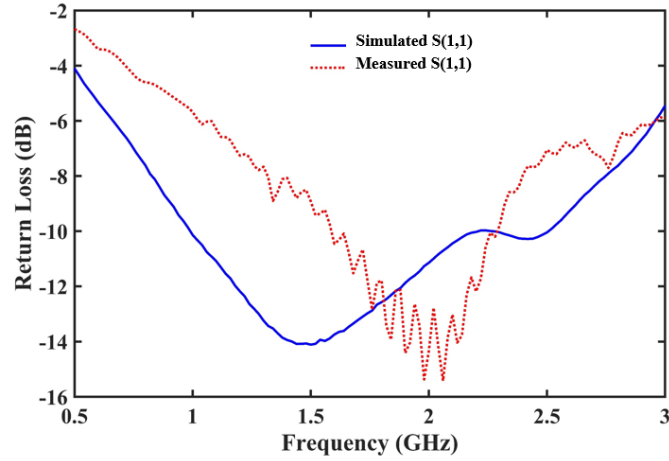


Figure 4.39 Comparison between simulated and measured return loss of a monopole antenna matched by NF circuit

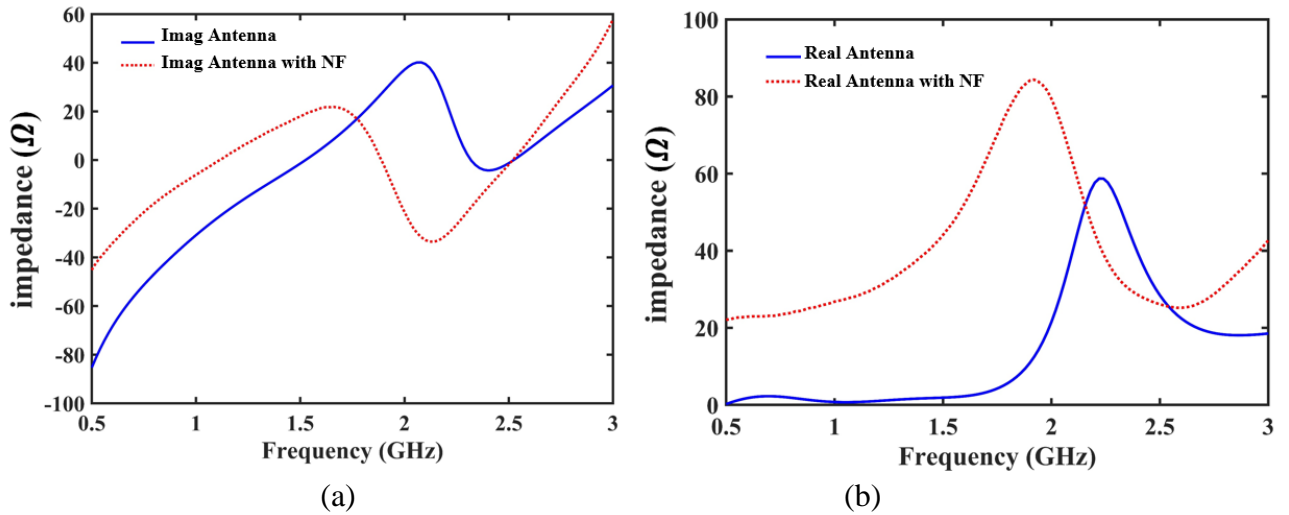


Figure 4.40 Comparison between antenna with/without NF matching for Imaginary part (a), and Real part (b)

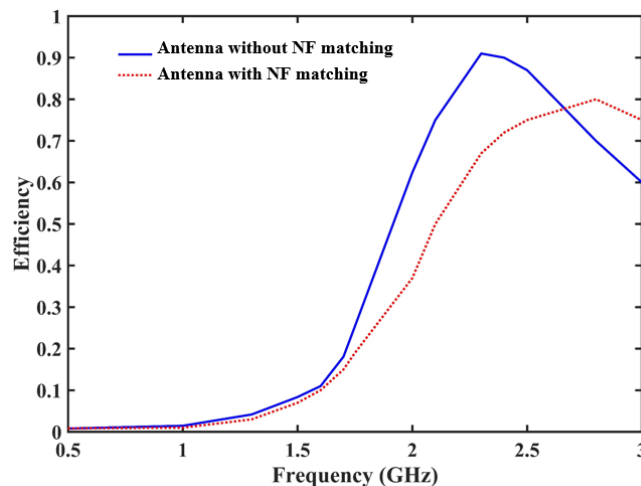


Figure 4.41 Efficiency comparison of antenna with/without NF matching

Despite the decrease of the antenna efficiency, it's interesting to verify on an actual case the bandwidth improvement that has been put forward in section 4.3 by combining Passive matching with NF matching. In that aim, two topologies have been simulated and compared by co-simulation (EM and S-parameters): the first topology cancels first the reactive part of the antenna, then transforms the net reactance to 50 Ω . While the second topology firstly decrease the antenna quality factor then cancels the reactive part finishing with transferring the net reactance to 50 Ω . The two topologies are given in Figure 4.42.

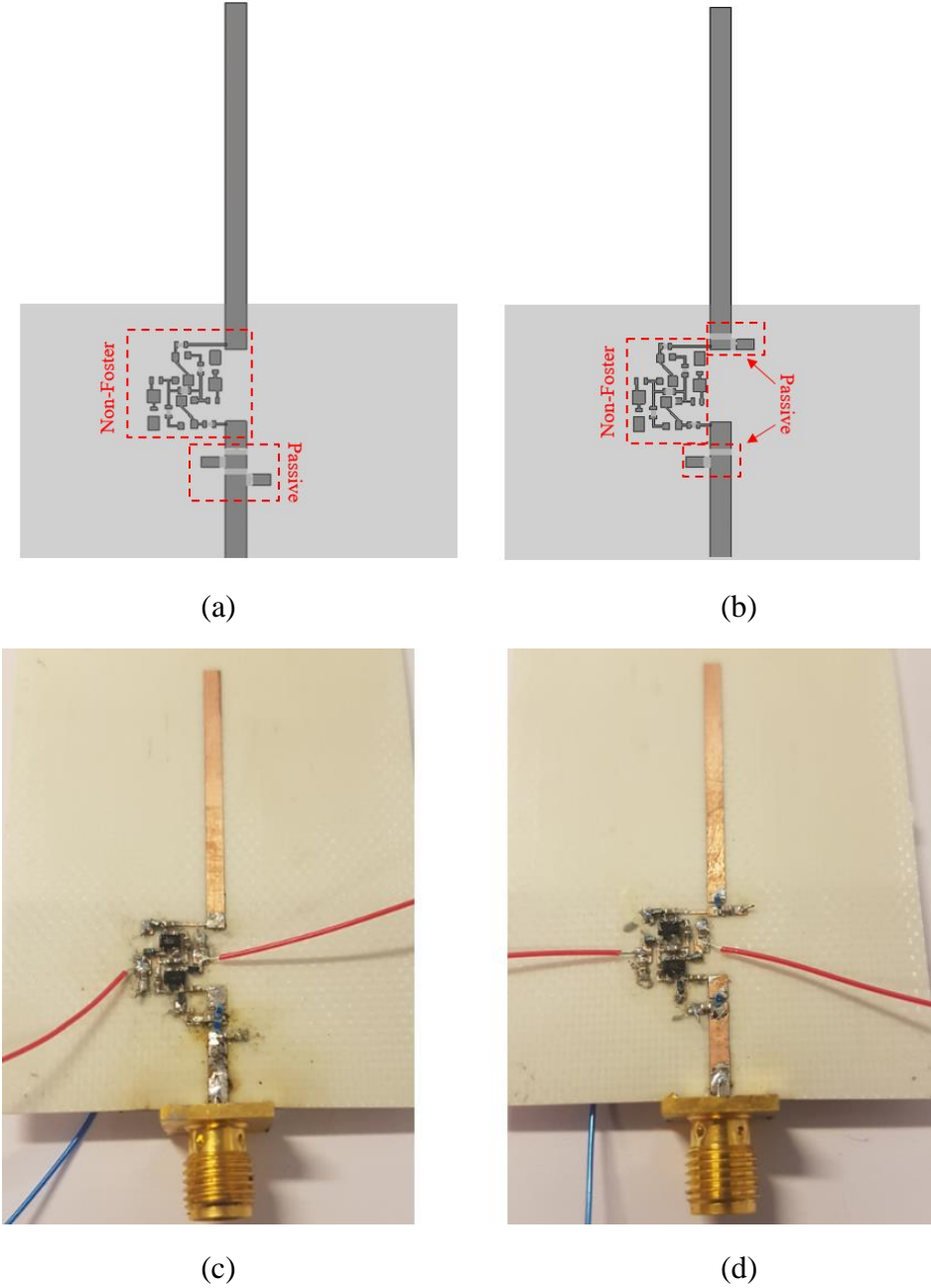


Figure 4.42 combined passive and NF matching first topology (a), second topology (b), fabricated first topology (c), and fabricated second topology (d)

Figure 4.43 shows a schematic view of the two topologies with all the elements used for passive and NF matching. Table 4.3 shows the value of the elements used in both topologies. A comparison between these two topologies and using only NF matching is given in Figure 4.44.

As expected, it can be noticed that using the combination of passive and NF has a wider matching bandwidth in simulation compared to using only NF circuit, particularly in the case of the 2nd topology (that corresponds to the third one studied in section 4.3.4.). In addition, Figure 4.45 shows a good agreement between simulated and measured results for both matching technique. Nevertheless, the issue of efficiency remains the same because the resistive part of the NF circuit dissipates a large portion of power coming from the source in both architectures.

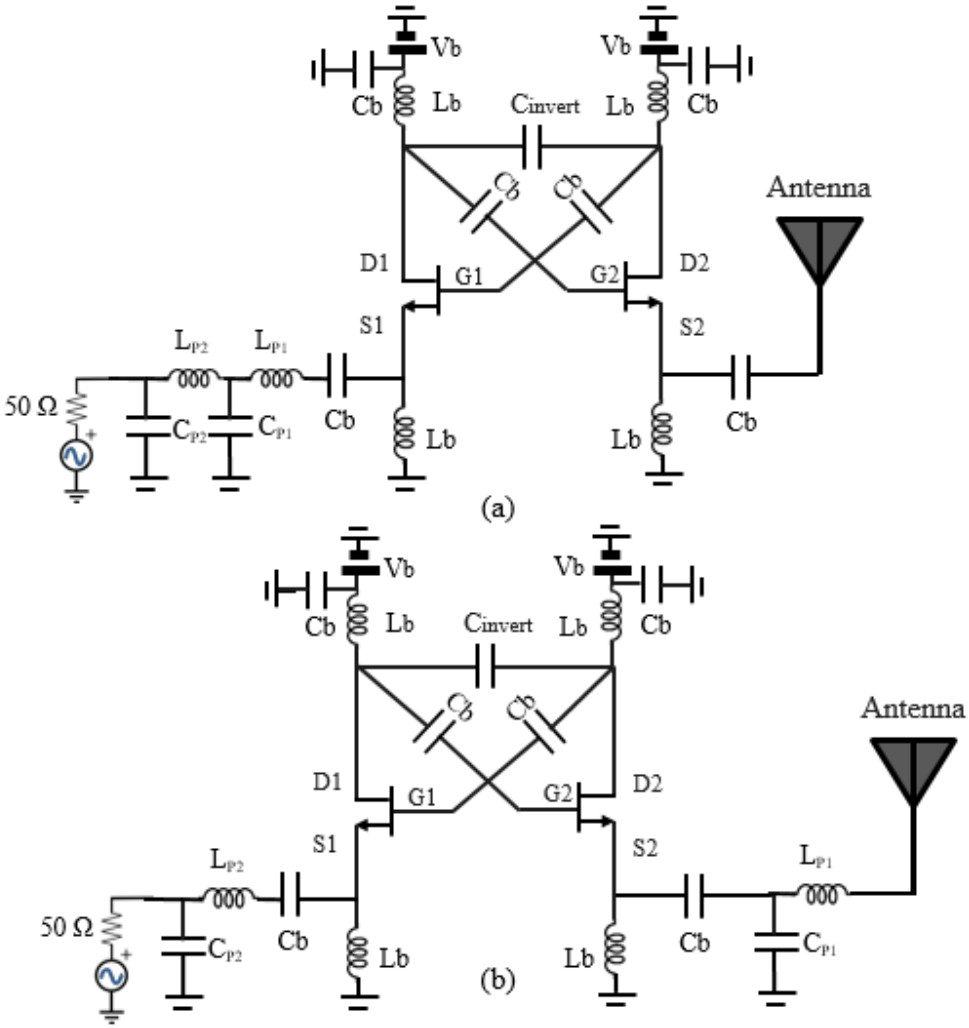


Figure 4.43 Schematic of combined Passive and NF matching, topology 1 (a), and topology 2 (b)

Table 4.3 Component values used in both topologies of combined passive and NF matching

Components	C _{invert}	C _{p1}	C _{p2}	L _{p1}	L _{p2}
Topology one	2pF	0.8PF	0.6pF	2.5nH	1nH
Topology two	3pF	0.6pF	0.5pF	0.7nH	0.5nH

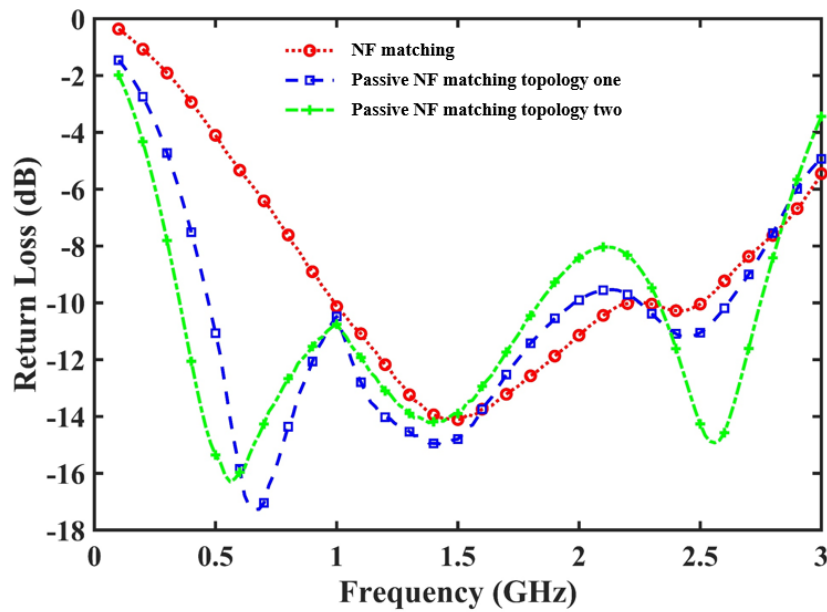


Figure 4.44 Comparison between NF matching and combined passive and NF matching

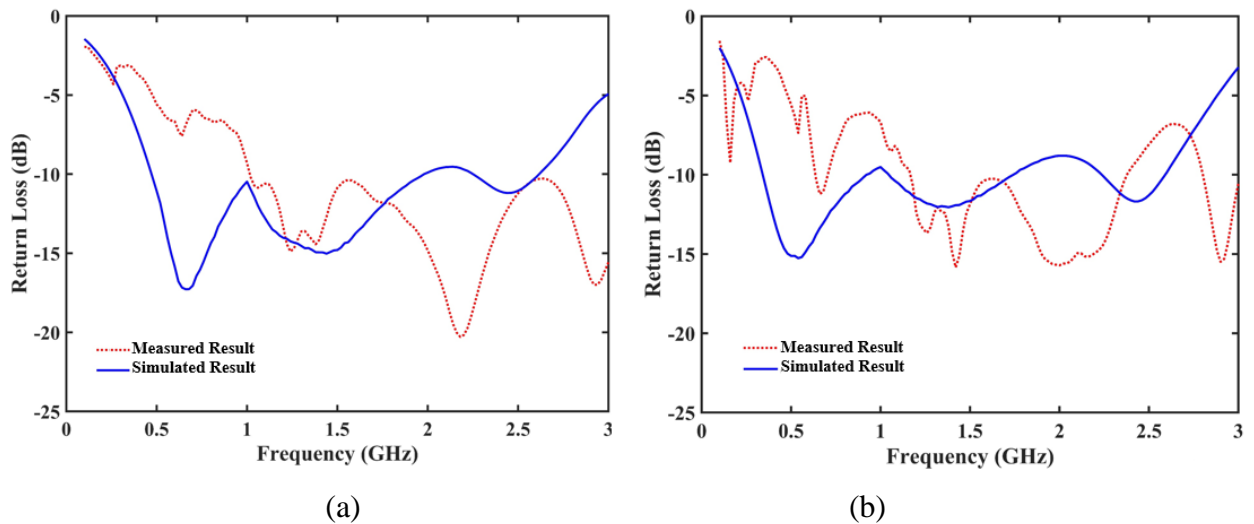


Figure 4.45 Simulated vs Measured Result of Passive NF matching of topology one (a), and topology two (b)

4.4.2.2 Non-Foster Matching and decoupling

In this section, NF circuits are used to both match and decouple the two closely separated monopole. The two topologies understudied are given in Figure 4.46. The topology shown in Figure 4.46.a involves only NF to match and decouple the antenna whereas NF circuits are used in Figure 4.46.b to match the antenna and a passive network to decouple. Indeed, in Figure 4.46.a a negative capacitance in series with a resistance are introduced to decouple the antenna. While in Figure 4.46.b, a positive inductance is used to mimic the negative capacitance, which is only valid at a single frequency point.

In order to synthesize the components values, a two-port representation of both topologies is provided in Figure 4.47.a. An even and odd analysis is carried out to find the value of the required reactance values for the matching and decoupling Circuit, that respectively correspond to X_a and X_d (Figure 4.47.b). $Z_{in,even}$ and $Z_{in,odd}$ are given in equations 4.29 and 4.30, and as in section 4-4-1, we have four equations with four unknowns, thus we can solve the system.

After numerically calculating the values needed for NF circuits, a tuning is also carried out to take into account the effect of the transmission lines. Note that the equations were solved at 1.6 GHz. Table 4.4 sums up the values of the chosen components for matching and decoupling networks.

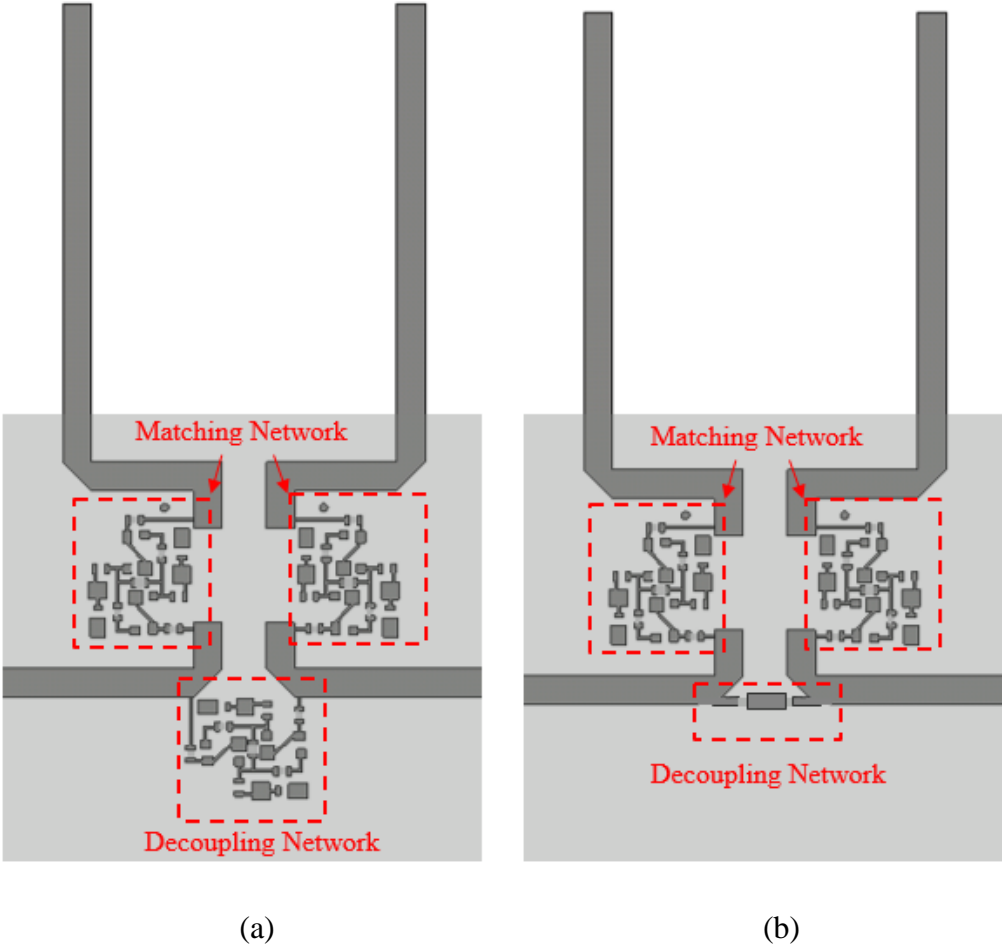
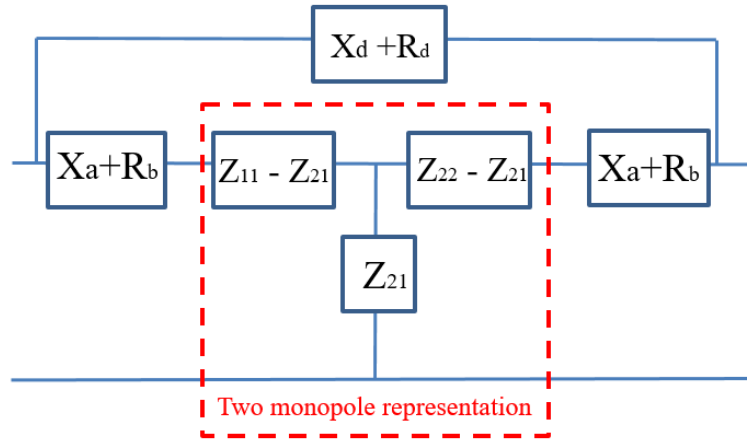
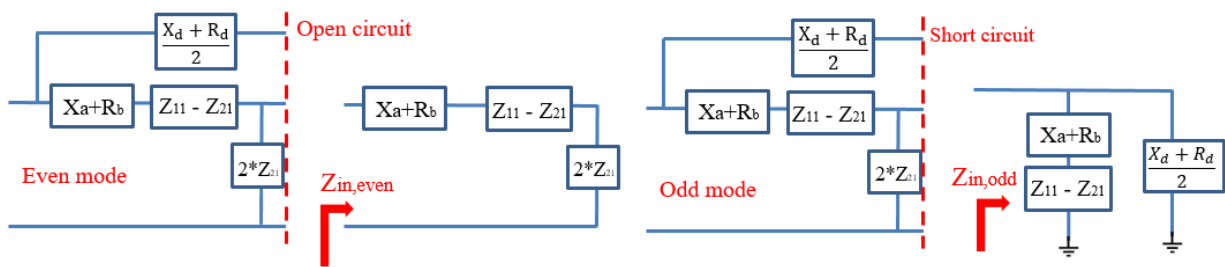


Figure 4.46 Two monopole antennas Matching and Decoupling using NF circuits (a), and matching using NF circuit and decoupling using passive circuit (b)



(a)



(b)

Figure 4.47 Two port network representation (a), even-odd mode representation (b)

$$Z_{in,even} = X_a + R_b + Z_{11} + Z_{21} \quad (4.29)$$

$$Z_{in,even} = \frac{(X_d + R_d)(X_a + R_b + Z_{11} - Z_{21})}{X_d + R_d + 2(X_a + R_b + Z_{11} - Z_{21})} \quad (4.30)$$

Table 4.4 Components values from calculation used in both Matching and decoupling topologies

Components	Matching X_a	Matching R_b	Decoupling X_d	Decoupling R_d
Topology one	2.8pF	45Ω	1.4pF	47Ω
Topology two	2.8pF	45Ω	7nH	47Ω

Figure 4.48 shows the simulated result of both topologies. It can be noticed that both topologies have a wideband matching performance, while using NF decoupling has a better isolation level compared to passive element and over a wider bandwidth as expected.

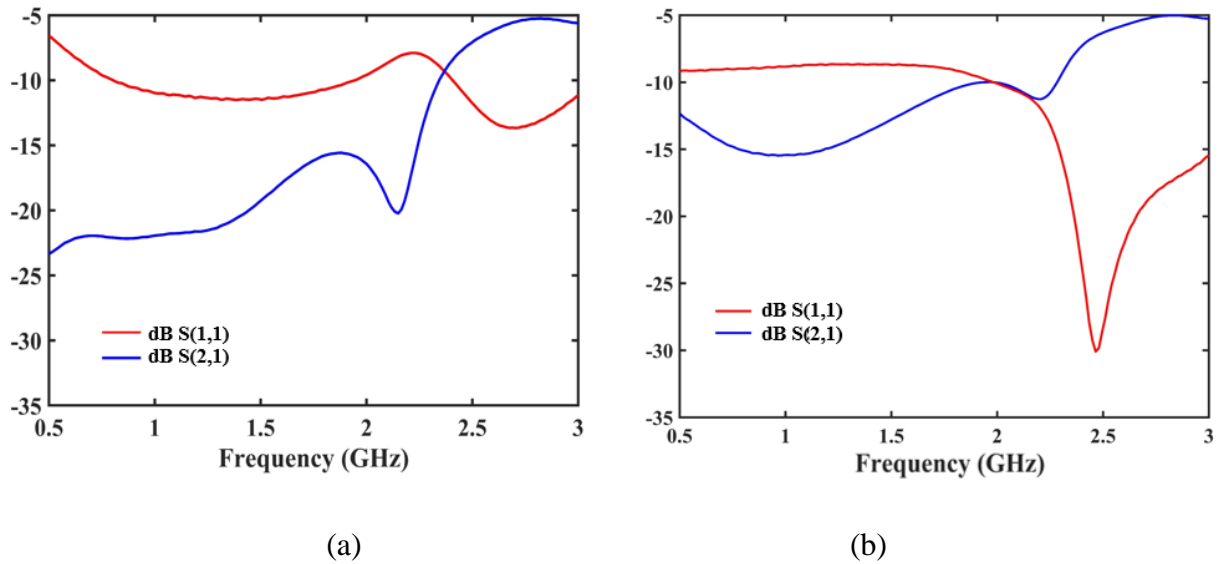


Figure 4.48 Simulated return and insertion loss of NF matching and decoupling (a), NF matching and passive decoupling (b)

Regardless of the system efficiency, we can conclude that using NF for matching and decoupling exhibits better responses in terms of level and bandwidth both for antenna matching (S_{11}) and isolation (S_{21}). These circuits are under completion and experimental results are expected to validate these simulations. Nevertheless, as the level of decoupling is not sufficient yet, we propose in the next section and, as initially planned, to combine two stages of self-interference cancellation: i.e. using phase shifter and decoupling network in order to achieve our desired goal (45dB of isolation between port 1 and port 2).

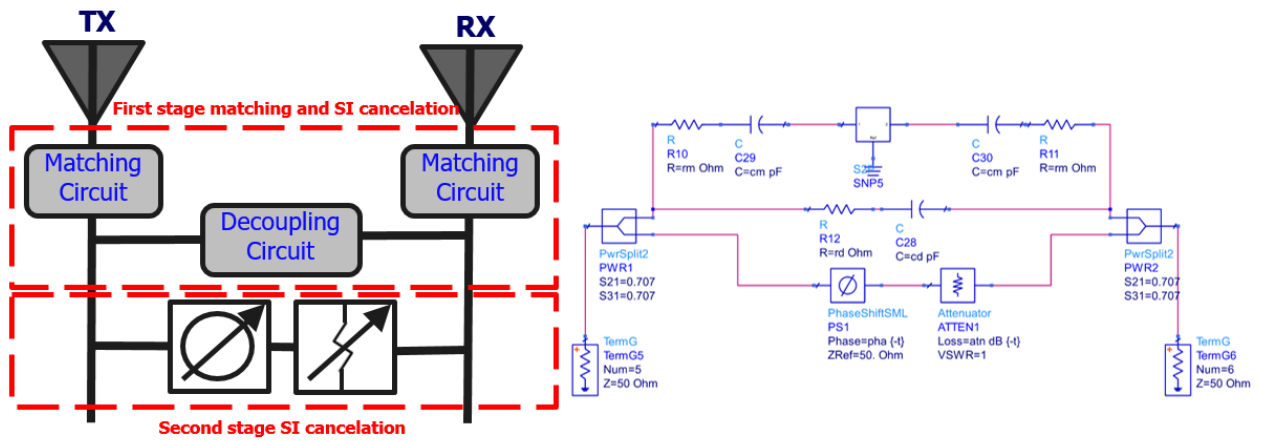
4.4.2.3 Combining Two Levels of Self-Interference Cancellation

As a first step, we want to estimate the level of SIC (Self-Interference Cancellation) that can be achieved by using this two-level technique in an ideal case (i.e. ideal components: ideal negative capacitance and ideal phase shifter).

The topology is depicted in Figure 4.49.a and consists in two stages: the first stage consist of the two closely separated monopole antennas matched and decoupled using NF circuit, while the second stage consists of a variable phase shifter with an attenuator. The two stages are connected together with a -3dB splitter as illustrated in ADS schematic of Figure 4.49.b.

The values for the ideal capacitance and resistance where based on the calculated values (for 1.6 GHz) from the even-odd analysis (previous section), while the value for the phase shifter was tuned to be around 171° with an attenuator level around 8dB. The simulation results using ideal elements are given in Figure 4.50, where we can notice a good performance in terms of return and insertion loss, especially around 1.6 GHz where the antenna is considered ESA.

The next steps consist in replacing the ideal phase shifter by our phase shifter that was studied in Chapter 3. Then, the ideal negative capacitance and resistance are replaced by the NF circuit in order to compare the result with the ideal ones.



(a)

(b)

Figure 4.49 Proposed FD topology (a), with ideal elements (b)

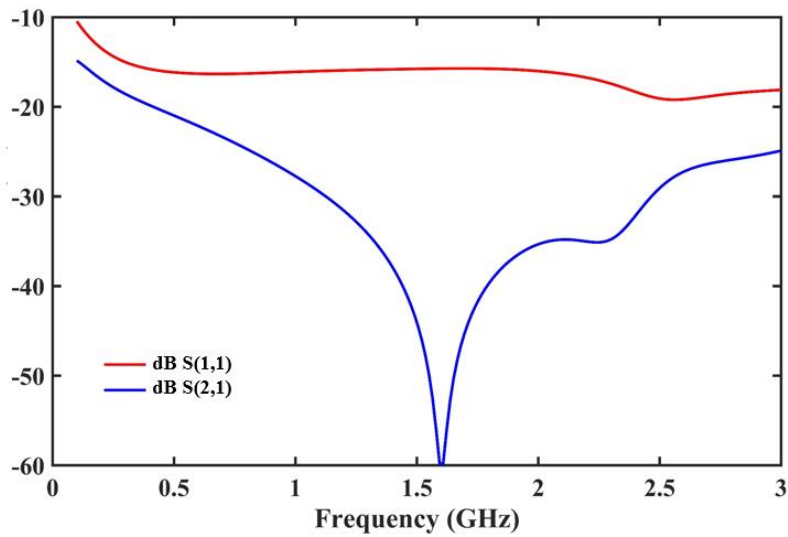


Figure 4.50 Simulated Return and insertion loss of Ideal FD system

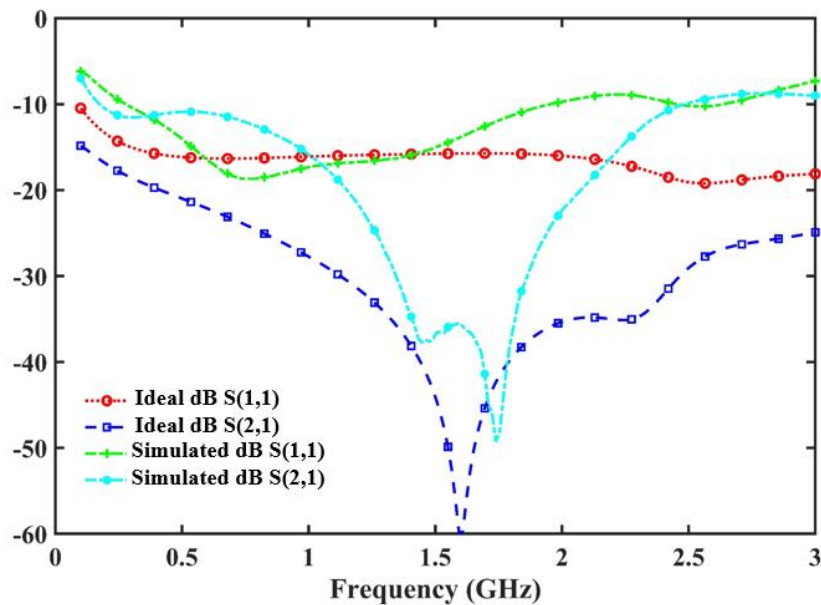


Figure 4.51 Comparison between simulated return and insertion loss with ideal ones

Figure 4.51 show the comparison in return and insertion loss between the ideal FD topology and the simulated one and a good agreement is observed. As an intermediate conclusion, we can put forward that the expected goal of achieving 45dB of isolation in a wide matching bandwidth with a good matching is achieved but still the efficiency issue is to be solved.

4.5 Conclusion

In this chapter, we have provided an overview about ESA and their gain-bandwidth limitation when using passive elements. We have described in details how to overcome this limitation by using NF circuit. We have also put forward a methodology study on how to improve the matching bandwidth by combining NF and passive elements. To do so, we have proposed a new topology that aims to decrease the antenna quality factor in order to achieve a wider matching bandwidth and higher gain compared to usual ways of using NF with passive elements.

Secondly, we have focused on studying and analyzing a topology of two closely separated monopole antennas in order to use them for our final FD system. The study started first with a reference topology that used only passive networks to match and decouple two monopole antennas. We have shown that adjusting the location of the decoupling network can be used to enhance the isolation level in a wider frequency range.

Then, we have simulated and fabricated one monopole antenna matched by using a NF circuit in order to validate this approach and the simulation and measurement results have shown a strong agreement with each other. However, in terms of efficiency, we have noticed that the system presents a slightly reduced efficiency compared to using only passive elements which is due to a spurious positive resistor from NF circuit. On the other hand, by using NF circuit to decouple the two planar monopole antennas, a wider isolation bandwidth with a higher level was obtained compared to only using passive compared to passive ones.

Finally, we have gathered all the knowledge that we have learned from chapter 3 and chapter 4, and we combined them together to build up a compact FD system. We have first simulated our proposed FD system with ideal elements (i.e. ideal negative capacitance and ideal phase shifter), and then replaced the ideal elements by the simulated results in ADS software. A strong agreement is obtained, especially at the targeted frequency of 1.6 GHz where an isolation of about 45 dB is achieved.

On the other hand, we have noticed that at the contrary of ideal XCP NF circuits, actual NF implementations generate spurious effects where the most detrimental is spurious positive resistor that limits or degrade the system efficiency. Therefore, at this stage, we would like to bring forth the need to take a step back to re-assess the choices that have been made by comparing the obtained results versus state-of-the-art ones.

First of all, a state-of-the-art summary on XCP NF circuit indicates that:

- Actual implementation is restricted below 1 GHz.
- Above 1 GHz, several examples have been published but most of them did not provide experimental results or seem to fail to obtain a stable behavior;
- Moreover, almost no previous works on antenna matching using NF have provided experimental or reliable rating of the whole radiating system efficiency.

In our study, we focused mainly on XCP Linvill's circuit to get NF behavior because, theoretically, more wideband negative components can be achieved. However, as discussed

theoretically and experimentally in chap. III, getting a negative capacitance (for example) above 1 GHz requires to respect some design rules to ensure a stable behavior which results in a non-ideal response. Particularly, the spurious residual resistor part contributes to a constant or slight decrease in the system efficiency.

Several ways could be explored to face out this issue:

- NGD circuit could be used to generate constant negative reactance response but only over narrow frequency band because they are mainly based on resonant behavior. Moreover, NGD is always associated with losses that should be compensated by amplifiers. This architecture is thus unidirectional and requires at least two antennas (TX and RX) in a full-duplex system.
- Integrated technologies (MOS, Bi-CMOS) could be applied to XCP NF circuit design both to get a high transconductance value for the transistor to lower the residual resistive part and also to minimize the feedback length required in the XCP topology to ensure the system stability. For example, cascode FET topology [23] could be used to try to increase the transconductance and thus reduce the resistive residual part.

4.6 References

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Chapter 5

General Conclusion

The main goal of this thesis targets the design of a wireless Full-Duplex front-end (i.e. Simultaneous Transmit and Receive) in the context of small electronic devices (e.g. IoT, ...). Moreover, as many standards and frequency bands have already been defined or are emerging currently, we also focus on a wide operating bandwidth.

The main issue when dealing with FD is the high level of Self-Interference (SI) that occurs between the transmitter and the receiver. This SI cancellation (SIC) architecture is usually divided into three main parts: passive suppression at the antenna level, analog cancellation and digital cancellation. Our work focus on using analog cancelation and passive suppression to provide around 45dB of SIC between the transmitter and the receiver in our context, i.e. a small system with closed TX and RX antennas.

From the state-of-the-art analysis given in Chapter I, we had shown that among the previously studied topologies, none of them is able to provide a wideband SIC with a minimum number of antennas (1 or 2) and even more if the antennas are really close to each other and for identical emitting direction and polarization for RX and TX antennas. We have then proposed a FD topology that consists of two first stages of SIC (i.e. antenna decoupling/isolation and analog cancelation). The first stage consists of a matching and a decoupling network between the two antennas and the second one is a tunable phase shifter (around 180°) with an attenuator. The antenna part of the front-end simply consists in two closely separated planar monopole antennas.

When dealing with small wireless things and objects, the antennas are supposed to be less bulky as possible. One way to miniaturize an antenna is to shift down its operating frequency band. Such antennas are known as ESA (Electrically Small Antenna). This can be done by classical passive matching networks over narrow band and for wider band by using non-Foster matching circuit (i.e. that use negative capacitances and inductances). An overview of the different kinds of non-Foster circuits from state-of-the-art are presented and compared in chap. II. Among them, XCP circuits have been chosen thanks to their frequency response potentially wider than other techniques. Their behavior (how NF circuit works) and a dedicated study of the stability analysis (NDF technique) of these active circuits have also been carried out in chap. II

NF circuit seems also promising to design tunable phase shifter (PS) suitable for our full-duplex topology. Therefore, we have studied in chap. III a topology to get a 180° phase shifter, which is based on negative capacitance. We have evidenced that the PS performance relies on the quality of the negative capacitance, i.e. no residual resistive part. So we proposed cascading two NF circuits (i.e. XCP with output at source and XCP with output at drain) because both topologies provide a negative capacitance but with opposite resistive parts. Thus by cascading them, we can cancel the resistive part. A further modification has also been put forward in order to decrease more the residual resistive part. The simulated phase shifter exhibited in simulation a perfect response in terms of return and insertion loss together with a tunable pure phase response around 180° as expected. However, when testing the system stability using NDF technique, the circuit was found to be unstable mostly due to the drain topology. In a second step, we re-designed the phase shifter by using only source topology. But as evidenced theoretically, the spurious residual resistive part should affect the PS response. Three transistors with different transition frequencies have been tried to build our source topology based NF circuit. It was demonstrated by the NDF technique that for our

system to be stable the feedback length between the drain of the first transistor and the gate of the second transistor should be minimized. Specific layouts for each transistor have been redesigned even so the required length is difficult to obtain in hybrid technology. Finally, the circuits (2 out of 3) built around the transistors with the lowest transition frequencies were found to be stable thanks to transition frequencies lower than the forecast frequency of oscillation. The NF circuit that exhibits the best performance has been used to build our phase shifter circuit. The PS measured results shows a good agreement with simulated ones and confirms a stable behavior with however, as expected, higher losses and a phase with a slope both due to the resistive part introduced by the source topology.

In chap. IV, we focused on the design of the full-duplex antenna level that included two antennas (TX and RX), their matching circuit to make them electrically small and the decoupling stage for the full-duplex application. First, we have recalled the definition of ESA and their limitations. As a reference system, we first used passive element to match and decouple the two closely separated antennas and we have also proposed an improvement of a previously published topology to get a better isolation performance. As passive matching and decoupling remain restricted to narrowband, antenna active matching and decoupling were implemented by using NF circuits. To identify the main benefits and drawbacks compared to passive circuits, the comparison was run first by comparing a single monopole antenna matching. A wideband matching performance was evidenced compared to passive matching, but no improvement in efficiency was obtained due to the NF residual resistive part that is introduced from the source topology. Nevertheless, we also studied the performance of using NF circuit on matching and decoupling the two closely separated planar monopole antennas, and we noticed a wide band matching and improved decoupling behavior compared to those from passive circuits.

Finally, we have summed up the two stages of SIC together (i.e. at the antenna level and by using PS and attenuator). First, our proposed FD topology was tested by using ideal negative capacitance and ideal phase shifter to quantify the maximum achievable level of SIC. When ideal elements were replaced by the reliable simulated ones, a good agreement between the two was obtained confirming that a wideband and compact FD system with a 45 dB of SIC was achieved.

However, an improvement of the system efficiency due to NF matching was expected but not achieved due to a spurious residual resistive part generated from the XCP source topology. It should be pointed out that almost no previous works on antenna matching using NF provided actual response on system efficiency! Moreover, very few experimental results beyond 1 GHz based on XCP can be found in the literature.

Thus, all the experience gained in this thesis allowed us to identify relevant proposals to further improve the implementation of such a FD topology by using NF circuits. Indeed, at the end of Chap. IV, some prospects are put forward in order to solve this issue. Thus, depending on the application bandwidth requirements, NF components based on NGD circuits could be implemented. It could be also interesting to investigate on the possibility of building transistors with high transconductance value in integrated circuit technologies (CMOS – BiCMOS) in order to minimized residual resistive parts in XCP NF circuits.

Résumé de la thèse

Présentation générale.

Cette thèse est un travail en cotutelle entre l'Université Libanaise et l'Université de Bretagne Occidentale (UBO, Brest). À l'UBO, elle s'est déroulée au laboratoire Lab-STICC (UMR CNRS 6285) du département MOM (micro-ondes, optoélectronique et matériaux) de l'équipe DIM (Dispositifs et Interfaces Multiphysiques). Le domaine d'investigation de l'équipe DIM est vaste et la conception de dispositifs et de systèmes RF et hyperfréquences est l'élément fédérateur de l'équipe qui apporte des solutions originales dans divers domaines : télécommunications, mer, défense et santé.

L'objectif principal de ce travail consiste à créer un système compact fonctionnant en mode Full-Duplex (FD) permettant à l'utilisateur de transmettre et de recevoir un signal utilisant la même bande de fréquences et aux mêmes instants. La compacité est recherchée dans le contexte de l'internet des objets (IoT, 5G,...). En outre, de nombreuses normes et bandes de fréquences émergent actuellement, ce qui nous amène à nous concentrer sur une relative large bande passante.

Dans le système FD, le problème principal est la Self-Interférence (SI) entre la réception et l'émission qui s'effectue au même endroit dans le cas d'une seule antenne ou à très faible distance dans le cas d'un système multi-antennaires. En effet, lors de l'émission et de la réception simultanée, il faut éviter que la puissance de l'émetteur ne masque le signal reçu. Pour cela il faut pouvoir atténuer le signal arrivant sur le récepteur d'un ordre de grandeur de 110 dB. Atteindre un tel niveau d'atténuation requiert deux couches analogiques et une couche numérique. L'architecture comporte donc un découplage ou isolation au niveau des antennes, une annulation analogique (en RF ou en bande de base) et une dernière, algorithmique. Cette thèse concerne les niveaux antenne et analogique afin d'atteindre un niveau d'isolation d'au moins 50 dB entre émission et réception.

Dans le contexte des IoT, la contrainte est d'autant plus forte que la compacité engendre une grande proximité des antennes. Idéalement, une seule antenne associée à un circulateur pourrait suffire à un fonctionnement en Full Duplex. Mais le niveau d'isolation typiquement de 20 dB du circulateur et le niveau d'adaptation de l'antenne (autour de 10 dB) rendent totalement insuffisant ce type simple de système. Il est alors nécessaire de disposer d'une ou plusieurs

antennes d'émission et au moins une en réception. Dans ce cas, la plupart des systèmes en FD reposent sur l'annulation de l'onde au niveau de l'antenne RX en utilisant le principe d'interférences destructives, les ondes émises devant alors arriver en opposition de phase sur l'antenne de réception, pour toute la bande passante de travail.

Faire un bilan de l'état actuel des systèmes FD est donc la première étape pour faire ressortir leurs avantages et inconvénients pour notre application. Les topologies principales sont comparées et identifiées comme étant à bande étroite et difficiles à transposer à notre contexte. Nous avons donc proposé une topologie FD comprenant les deux premières étapes analogiques (isolation d'antenne et annulation via la partie circuit). La première étape consiste à découpler les deux antennes tout en élargissant la largeur de bande de fréquences. La seconde consiste en la conception et réalisation d'un déphaseur pur 180° légèrement réglable. En combinant ces deux étapes, nous espérons atteindre un niveau d'isolation suffisant avant la dernière étape d'annulation réalisée par l'étage numérique.

Puisque notre objectif est dédié aux dispositifs de faibles dimensions (IoT), une antenne miniaturisée est donc nécessaire. Réduire la dimension d'une antenne est équivalent à décaler vers les plus basses fréquences sa bande de fréquence de fonctionnement. De telles antennes sont appelées ESA (Electrically Small Antenna). Les réseaux d'adaptation passifs classiques peuvent réaliser cette fonction, mais au détriment de la bande passante. Afin d'élargir la bande passante, nous pourrions introduire des pertes, ce qui réduirait par ailleurs le gain d'antenne. Aussi, pour assurer une bande passante plus large, nous introduisons ici un circuit d'adaptation de type Non Foster, c'est-à-dire générant des capacités et des inductances négatives. Les limites classiques imposées aux dimensions des antennes électriquement petites peuvent être alors franchies, mais au prix d'une plus grande complexité et d'une maîtrise des problèmes de stabilité en particulier, puisque des éléments actifs doivent être introduits.

Par la suite est présenté l'état de l'art des différents types de circuits Non Foster. Parmi eux, les circuits XCP (paire de transistors à couplage croisé) qui sont a priori les plus susceptibles de générer une réponse en fréquence des plus large. Par ailleurs, nous présentons en détail l'analyse du circuit NF au moyen d'équations et de synthèse permettant de mettre en avant la génération d'éléments réactifs à valeurs négatives du système mais aussi les effets parasites associés les plus significatifs. Enfin, la stabilité étant un point critique de ce type de circuit, une

partie non négligeable lui est consacrée et nous avons introduit la technique de la Fonction Déterminée Normalisée (NDF), technique efficace pour l'analyse de la stabilité des XCP.

Puis une topologie de déphaseur basée sur un circuit NF est introduite. Le déphaseur offre un déphasage de 180° potentiellement accordable (valeur de phase théoriquement pure, c'est-à-dire constante en fréquence) entre ses deux ports et nécessitant l'utilisation d'une capacité négative. Nous présenterons une étude approfondie de la topologie, y compris les équations et les performances idéales attendues. Les performances du déphaseur dépendent en grande partie de la qualité de la capacité négative, difficile à maintenir de manière idéale sur une large bande de fréquences. Aussi, nous testons expérimentalement différents prototypes de circuits XCP en vue d'obtenir un comportement non Foster avec le moins d'effets parasites possibles et surtout stable quel que soit la fréquence. Ainsi, la méthode de stabilité décrite au chapitre II est utilisée pour vérifier la fiabilité de cet élément clé. Les relations analytiques indiquent, confortées par les simulations, que plusieurs paramètres sont délicats à maîtriser lorsque la fréquence de travail se situe environ au-dessus de 1 GHz avec des circuits XCP. Au moins trois d'entre eux doivent être particulièrement surveillés: i) la partie réelle résiduelle du circuit XCP, ii) les lignes d'interconnexion et iii) la fréquence de transition du transistor sélectionné. La partie réelle résiduelle de la capacité négative a pour effet de générer des pertes en transmission. Les lignes d'interconnexion des transistors doivent être de longueur minimale pour éviter les problèmes de stabilité aux hautes fréquences. Par ailleurs, contrairement aux amplificateurs, la fréquence de coupure des transistors ne doit pas être trop élevée par rapport à la fréquence haute de la bande passante du dispositif, toujours pour éviter l'apparition d'instabilités.

Notre objectif se concentre enfin sur la réalisation du système FD dans son ensemble. La pertinence et les performances de la topologie proposée sont étudiées en considérant un système basé sur deux antennes monopole électriquement proches. Toutes les études et techniques explorées et validées dans les chapitres précédents sont mises en œuvre. Des circuits non Foster sont utilisés pour faire rayonner les antennes dans une large bande de fréquences très inférieure à leur fréquence de résonance initiale. Une étude méthodologique est réalisée afin d'obtenir le meilleur compromis entre les caractéristiques recherchées. A toutes les étapes, lorsque cela est possible, des relations analytiques sont données et les résultats obtenus en utilisant des composants non Foster réels qui sont comparés en simulation et expérimentalement à ceux des réseaux passifs. De plus, l'efficacité de l'ensemble des systèmes (passif et NF) est quantifiée et

comparée. Enfin, des conclusions sont tirées et des perspectives sont proposées pour améliorer notre système FD.

Résumé du chapitre 1

Dans ce chapitre, nous soulignons l'intérêt du système FD et de ses avantages par rapport au système semi-duplex traditionnel, en termes de multiplication potentielle par deux du gain en débit, et par conséquent de la diminution de la congestion des liaisons sans fil.

Les principales sources d'imperfection de l'annulation du signal sur l'antenne réceptrice sont analysées : elles sont divisées en trois types. Premièrement, les fuites ayant lieu dans le substrat. Elles peuvent être minimisées d'autant plus que le substrat utilisé sera fin, rejetant alors les modes parasites aux hautes fréquences. Deuxièmement, des ondes de surface ont lieu à l'interface air-diélectrique. Des solutions existent pour les contrer : matériaux absorbants ou métamatériaux par exemple. La troisième cause d'imperfection provient de la conjugaison d'ondes électromagnétiques de sources diverses, en champ proche et en champ lointain. En champ proche, l'annulation théorique sur l'antenne de réception par opposition de phase des antennes émettrices est à la base du Full Duplex, elle serait réalisée parfaitement si les sources émettrices étaient ponctuelles et situées exactement à la même distance. Mais les dimensions des antennes sont du même ordre de grandeur que la distance entre antennes TX et RX, ce qui crée des « effets de bord » qui dégradent le niveau d'annulation de la puissance des TX sur le RX. En champ lointain, les ondes émises subissent des réflexions plus ou moins importantes suivant l'environnement et une partie non négligeable revient vers la source et par conséquent se rajoute au signal de réception. De plus dans la majorité des applications le canal de transmission est non stationnaire, ce qui implique de faire un sondage de canal en temps réel. Cette partie de signal parasite est alors traitée par la couche numérique qui se situe après le convertisseur analogique-numérique. De ce fait, il est admis de manière empirique que l'annulation analogique de l'ordre de 60 dB est suffisante, les 110 dB étant obtenus grâce à la couche logicielle.

Pour des applications IoT un niveau sur la couche antennaire recherché est d'environ 50 dB. Nous étudions d'abord quatre topologies FD et en retirons les avantages et inconvénients. Ces topologies se concentrent principalement sur la séparation d'antenne et l'annulation du SI à l'aide d'un déphaseur, mais toutes sont dédiées à des applications en bande étroite.

Puisque nous nous intéressons au concept d'IoT et d'appareils compacts, nous avons proposé une topologie FD visant à faire rayonner l'antenne dans une plage de fréquences inférieure où elle peut être considérée comme une antenne électriquement petite. Les circuits d'adaptation utilisant des éléments passifs sont limités ; nous avons donc introduit l'utilisation de circuits non conventionnels à base de circuits Non Foster pour faire rayonner et découpler deux antennes monopolaires planes étroitement séparées.

Résumé du chapitre 2

Dans ce chapitre, nous présentons dans un premier temps le principe de fonctionnement d'une cellule Non-Foster, qui a pour conséquence que le courant circulant dans le dipôle inclus dans cette cellule s'effectue en sens inverse du sens « naturel », ce qui génère une impédance de signe opposé pour ce dipôle. Sur l'abaque de Smith, cela se traduit par un coefficient de réflexion tournant dans le sens inverse des aiguilles d'une montre en fonction de la fréquence, ce qui en fait sa signature en quelque sorte. Plusieurs topologies Non Foster sont présentées, en particulier celle de Linvill en raison de ses performances large bande par rapport aux autres topologies.

Ces autres topologies pouvant générer un comportement Non Foster autre que l'utilisation de deux transistors sont présentées, celle à conversion d'impédance négative (NIC), les topologies générant un temps de propagation de groupe négatif et un type particulier d'amplificateur distribué.

Une étude analytique complète a été réalisée sur le circuit Linvill en développant l'équation du circuit en tenant compte d'une des capacités du schéma équivalent, généralement ignorée. En outre, une étude de stabilité a également été réalisée. Premièrement, le circuit Linvill est divisé en deux types, en fonction du port considéré comme port d'entrée. Si l'entrée est située sur l'émetteur du transistor, la stabilité est analysée en circuit ouvert (OCS). Deuxièmement, si le circuit se trouve à la jonction du collecteur, elle sera analysée en court-circuit (SCS). La stabilité de l'OCS et du SCS peut être obtenue en modifiant la valeur de l'impédance qui va être inversée, afin qu'elle soit inférieure à l'impédance de charge pour SCS et supérieure à l'impédance de charge pour OCS. Par ailleurs, il a été démontré que les facteurs K de Rollet et le coefficient μ ne sont pas suffisants pour vérifier la stabilité du circuit ; une fonction normalisée a donc été introduite pour vérifier et tester la stabilité du circuit.

Résumé du chapitre 3

Dans ce chapitre, nous présentons les différents types de déphaseurs et leurs applications dans les systèmes actuels. Dans un premier temps, nous avons concentré notre intérêt sur les déphaseurs pur, qui présentent une phase en transmission constante en fonction de la fréquence dans. Les applications de ce type de déphaseur émergent actuellement, ils peuvent être utilisés pour résoudre le problème de déformation du lobe principal lors d'un dépointage d'antennes et en particulier pour les réseaux d'antennes en série. Ce type de déphaseur peut être mis en œuvre en utilisant des éléments non-Foster ou des circuits à temps de propagation de groupe négatif (NGD). Puisque nous sommes intéressés par un déphasage accordable pour une large bande passante et surtout réciproque, nous avons donc choisi de concevoir notre déphaseur en utilisant des éléments Non Foster au lieu des NGD.

Une topologie proposée a été étudiée sur la base d'un document de référence utilisant une topologie à capacité positive et négative. L'idée principale d'avoir une phase plate dépend fortement de la capacité négative pure du circuit Non Foster. En prenant en compte le schéma équivalent des transistors valable aux fréquences de travail, nous avons noté que dans la configuration originale que nous appellerons à source commune, il subsistait une valeur réelle non négligeable générant des pertes en transmission. Cependant, en connectant les drains au lieu des sources, il apparaît la même valeur réelle, mais de signe opposé. D'où l'idée de cascader les topologies source et drain. La topologie simulée a montré de bonnes performances en termes de d'adaptation, de perte d'insertion, et a montré la possibilité d'ajuster la phase constante en fréquence. Mais l'étude de la stabilité a mis en avant des problèmes de l'instabilité provenant de la topologie drain. Ainsi, une deuxième conception du déphaseur a été réalisée en utilisant uniquement la topologie source.

Une étude systématique de la stabilité de la topologie source Non Foster a été réalisée. Elle consistait à étudier l'effet de la longueur des lignes de connexion entre les deux transistors sur la stabilité. Il a été noté que pour que le circuit soit stable, il fallait soit diminuer la longueur de ces lignes de connexion en utilisant un transistor à plus basse fréquence de transition. Trois transistors à effet de champ différents, chacun avec une fréquence de transition différente, ont été utilisés pour la réalisation de trois circuits. Deux d'entre eux se sont révélés stables, confirmant que c'était une solution pour obtenir un circuit Non Foster stabilisé. Nous avons noté comment

les effets parasites des transistors affectent la performance du circuit, le fait d'avoir une partie réelle résiduelle non négligeable introduit des pertes en transmission et une pente de la phase.

Enfin, un déphaseur a été conçu sur la seule base de la topologie source, la réponse du circuit a été testée ainsi que sa stabilité, le circuit fabriqué présente un bon accord entre le résultat de la mesure et celui simulé, les PS ont une perte de l'ordre de 5dB avec environ 180° de déphasage entre 1GHz et 2GHz.

Résumé du chapitre 4

Dans ce chapitre, nous avons présenté un aperçu des antennes électriquement petites (ESA), en examinant le facteur de qualité Q et la relation avec la largeur de bande et le gain de l'antenne. Il a été noté que l'ESA a un facteur Q élevé, ce qui conduit à une bande passante étroite. L'appariement passif peut réduire le facteur Q de l'ESA, mais souffre d'une limitation gain / bande passante (c'est-à-dire que pour avoir une bande passante d'adaptation plus large, nous devons introduire une perte qui abaisse le gain de l'ESA). Mais l'utilisation de circuits Non Foster permet de surmonter cette limitation en offrant une largeur de bande plus large et un gain élevé par rapport à la correspondance passive.

Une étude méthodologique a été réalisée pour fournir un moyen efficace d'utiliser la technique passive avec la Non Foster pour obtenir adéquation large bande à gain élevé.

Après cela, deux antennes monopolaires planes étroitement séparées ont été étudiées afin de les utiliser pour notre système FD final. L'étude a commencé par une topologie de référence utilisant uniquement des réseaux passifs pour associer et découpler les deux antennes monopolaires. Nous avons montré qu'il est possible d'ajuster l'emplacement du réseau de découplage pour améliorer le niveau d'isolement dans une plage de fréquences plus étendue. Après cela, nous avons simulé et fabriqué une antenne unipolaire plane avec un circuit NF pour validation. Les résultats mesurés et simulés étaient toutefois proches les uns des autres, en raison de la partie réelle introduite. De plus, nous avons montré qu'en utilisant un circuit NF comme réseau de découplage pour les deux antennes unipolaires planes, on obtenait une largeur de bande d'isolation plus grande avec un niveau supérieur par rapport à l'utilisation exclusive de circuits d'adaptation purement passifs.

Enfin, nous avons combiné les deux circuits (déphaseur et circuits d'adaptation) en utilisant les résultats de la simulation du PS étudiés au chapitre 3, ainsi que l'adaptation et le découplage de deux antennes monopolaires planes avec la NF, et avons montré que nous avons environ 45dB de SCI en particulier à la fréquence cible de 1,6 GHz.

Conclusion

L'objectif principal de cette thèse était la conception de la partie analogique d'un système Full Duplex de faibles dimensions, en particulier les IoT,...). Dans ce domaine, de nombreuses normes et bandes de fréquences ont déjà été définies ou sont en train de naître, nous nous sommes concentré sur une large bande passante opérationnelle.

Le principal problème en matière de FD est la nécessité de la réjection du niveau élevé d'auto-interférence dit SIC (Self Interference Cancellation) qui se produit entre l'émetteur et le récepteur. Cette architecture d'annulation SI est généralement divisée en trois parties principales : suppression passive au niveau de l'antenne, annulation analogique et annulation numérique. Notre travail a consisté principalement à utiliser l'annulation analogique et la suppression passive pour fournir un niveau de SI d'environ -45 dB.

Dans l'analyse de l'état de l'art présentée au chapitre 1 nous avons montré que parmi les topologies précédemment étudiées, aucune d'entre elles n'est en mesure de fournir un SI large bande avec un nombre minimal d'antennes (1 ou 2) d'autant plus si les antennes sont très proches les unes des autres et pour des émissions identiques en direction et polarisation pour les antennes RX et TX. Nous avons ensuite proposé une topologie FD composée de parties. Le premier étage consiste en un réseau d'adaptation et de découplage entre les deux antennes et le second un déphaseur accordable (autour de 180 °).

Lorsqu'il s'agit d'IOT, les antennes doivent être les moins volumineuses possibles. Une façon de miniaturiser une antenne consiste à décaler sa bande de fréquence de fonctionnement vers les basses fréquences. De telles antennes sont appelées ESA (Electrically Small Antenna). Cela peut être réalisé avec des réseaux d'adaptation passifs classiques en bande étroite et pour une bande plus large en utilisant un circuit d'adaptation Non-Foster (c'est-à-dire utilisant des capacités et inductances négatives). Un aperçu des différents types de circuits Non-Foster issus de l'état de l'art est présenté et comparé au chap. II. Parmi eux, les circuits XCP (paire de transistors à couplage croisé) ont été choisis en raison de leur réponse en fréquence

potentiellement plus large que d'autres topologies. Leur comportement et une étude dédiée de la stabilité (technique NDF) de ces circuits actifs sont également présentés au chap. II.

Le circuit NF apparaît également prometteur pour concevoir un déphaseur accordable (PS) adapté à notre topologie Full Duplex. Nous avons étudié au chapitre III une topologie de déphaseur 180° basé sur l'utilisation de capacités négatives. Nous avons montré que la performance du PS dépend de la qualité de la capacité négative, à savoir que la partie résistive résiduelle doit être la plus faible possible. Nous avons donc proposé de mettre en cascade deux circuits NF, à savoir une XCP avec sortie à la source et une XCP avec sortie au drain car les deux topologies fournissent une capacité négative mais avec des parties résistives de valeur opposée. Ainsi en les cascadiant la partie résistive totale s'annule. Le déphaseur simulé a montré en simulation des réponses quasi parfaite en termes de perte de retour et d'insertion ainsi qu'une réponse en phase pure ajustable autour de 180° comme prévu. Cependant, lors du test de la stabilité du système à l'aide de la technique NDF, le circuit s'est avéré instable, principalement à cause de la topologie drain.

Dans un deuxième temps, nous avons repensé le déphaseur en utilisant uniquement la topologie source. Trois transistors avec différentes fréquences de coupure ont été testés pour construire notre circuit NF basé sur la topologie source. La technique NDF a démontré que pour que notre système soit stable, la longueur de la rétroaction entre le drain du premier transistor et la grille du deuxième transistor devait être minimisée. Les schémas spécifiques à chaque transistor ont été optimisés même si la longueur requise est difficile à obtenir en technologie hybride. En mesure, deux sur trois des circuits construits autour des transistors ayant les fréquences de coupure les plus basses se sont avérés stables. Le circuit NF qui présente les meilleures performances a été utilisé pour notre déphaseur. Les résultats de mesure montrent un bon accord avec ceux simulés et confirment un comportement stable avec cependant, comme prévu, des pertes et une phase avec une pente due à la partie résistive introduite par la topologie source.

Au chapitre IV, nous avons abordé la conception d'antennes en Full Duplex qui comprenait deux antennes (TX et RX), leur circuit d'adaptation et l'étage de découplage. En tant que système de référence, nous avons d'abord utilisé un circuit passif pour associer et découpler les deux antennes électriquement proches. Nous avons également proposé une amélioration

d'une topologie précédemment publiée afin d'améliorer les performances d'isolation. Pour identifier les principaux avantages et inconvénients par rapport aux circuits passifs, la comparaison a d'abord été effectuée en comparant l'adaptation d'une seule antenne unipolaire. Une adaptation large bande en utilisant un circuit NF a été mise en œuvre en comparaison avec celle à adaptation passive, mais sans amélioration de l'efficacité à cause de la partie résistive résiduelle. Nous avons également étudié les performances du circuit NF pour l'adaptation et le découplage des deux antennes et avons constaté une adaptation plus large bande et une amélioration du découplage par rapport aux circuits passifs.

Par ailleurs, notre topologie FD a été testée en utilisant une capacité négative idéale et un déphaseur idéal pour quantifier le niveau maximum réalisable de SIC. Lorsque les éléments idéaux ont été remplacés par les mesures des différents circuits constitutifs, un bon accord a été obtenu, confirmant qu'un système FD compact large bande avec une valeur SIC de -45 dB peut être obtenu.

Cependant, une amélioration de l'efficacité du système due à l'adaptation NF était attendue, mais n'a pas été atteinte en raison d'une partie résistive résiduelle parasite générée à partir de la topologie de source XCP. Il convient de noter que presque aucun travail précédent sur l'adaptation d'antenne utilisant des circuits NF n'a fourni d'information sur l'efficacité du système ! De plus, très peu de résultats expérimentaux au-delà de 1 GHz basés sur les XCP peuvent être trouvés dans la littérature.

Enfin, l'expérience acquise durant cette thèse nous a permis d'identifier des propositions pertinentes pour améliorer la mise en œuvre d'une telle topologie FD en utilisant des circuits NF. Ainsi, en fonction des besoins en bande passante de l'application, des composants NF basés sur des circuits NGD pourraient être implémentés. Il pourrait également être intéressant d'étudier la possibilité de construire des transistors à valeur de transconductance élevée avec les technologies de circuits intégrés (CMOS - BiCMOS) afin de minimiser les résistances résiduelles dans les circuits XCP NF.

Appendices

Appendix A

NIC Based on Transformer

The small signal model of the topology of NIC based on transformer is represented in the figure below where both $C\pi$ and $C\mu$ are taken as zero for simplicity, and based in that we can calculate the input impedance as follows:

$$\frac{V_2}{V_1} = N \quad (2.31)$$

Where V_2 is given as:

$$V_2 = -Z_L I_{in} \quad (2.32)$$

Substituting (2.32) in (2.31) we get:

$$V_1 = \frac{-Z_L I_{in}}{N} \quad (2.33)$$

V_{CE} can be calculated as:

$$V_{CE} = -r_0(I_{in} + gmV_{BE}) \quad (2.34)$$

V_{BE} can be expressed as:

$$\begin{aligned} V_{BE} &= V_1 + V_{CE} - I_{in}Z_L \\ &= -Z_L I_{in} \left(1 + \frac{1}{N}\right) + V_{CE} \end{aligned} \quad (2.35)$$

Replacing (2.35) in (2.34) we get:

$$V_{CE} = \frac{-r_0 I_{in} \left(1 - gmZ_L \left(1 + \frac{1}{N}\right)\right)}{(1 + r_0 gm)} \quad (2.36)$$

The input voltage is given as:

$$V_{in} = Z_L I_{in} - V_{CE}$$

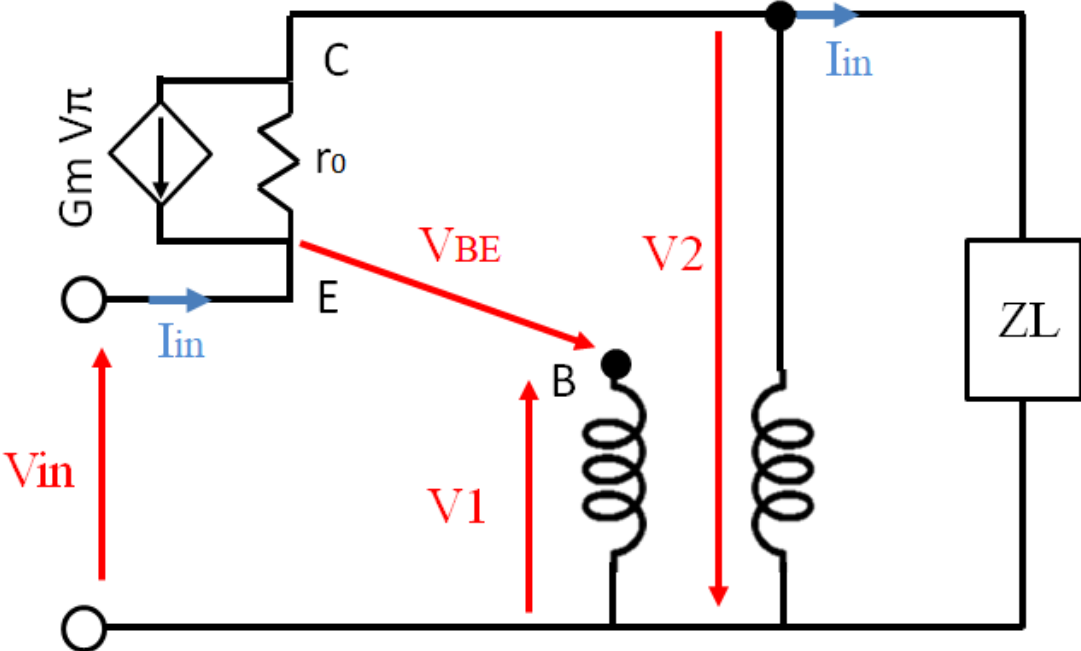
$$V_{in} = Z_L I_{in} + \frac{r_0 I_{in} \left(1 - gmZ_L \left(1 + \frac{1}{N}\right)\right)}{(1 + r_0 gm)} \quad (2.37)$$

Finally, the input impedance can be calculated as:

$$Z_{in} = \frac{r_0}{(1 + r_0 gm)} + \frac{Z_L \left(1 - \frac{r_0 gm}{N}\right)}{(1 + r_0 gm)} \quad (2.38)$$

For low frequency approximations ($r_0 \gg 1$ and $g_m \gg 1$), (2.38) can also be approximated by:

$$Z_{in} \approx -\frac{Z_L}{N} \tag{2.39}$$



Appendix B

Component Data Sheet

Avago VMMK-1218

VMMK-1218
0.5 to 18 GHz Low Noise E-PHEMT
in a Wafer Scale Package



Data Sheet



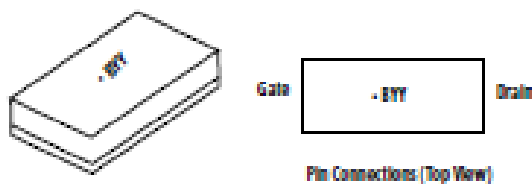
Description

Avago Technologies has combined its industry leading E-pHEMT technology with a revolutionary chip scale package. The VMMK-1218 can produce an LNA with high dynamic range, high gain and low noise figure that generates off of a single position DC power supply. The GaAsCap wafer scale sub-miniature leadless package is small and ultra thin, yet can be handled and placed with standard 0402 pick and place assembly.

The use of 0.25 micron gates allow a ultra low noise figure (below 1dB from 500 MHz to 12 GHz) with respectable associated gain. With a flat transconductance over bias and frequency the VMMK-1218 provides excellent linearity of over 30 dBm and power over 15 dBm at one dB compression. This product is easy to use since it requires only positive DC voltages for bias and low matching coefficients for simple impedance matching to 50 Ω systems.

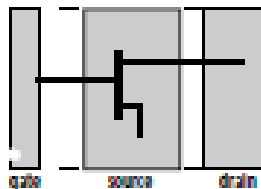
The VMMK-1218 is intended for any 500MHz to 18GHz application including 802.11abgn WLAN, WiMax, BWA 802.16 & 802.20 and military applications.

GaAsCap 0402, 1.0mm x 0.5mm x 0.25mm



Pin Connections (Top View)

Notes: Top view package marking provides orientation



Notes:
"b" = Device Code
"YY" = Year Code

Features

- Sub-miniature 0402 (1mm x 0.5mm) Surface Mount Leadless Package
- Low height (0.25mm)
- Frequency Range 0.5 to 18 GHz
- Enhancement Mode^[1]
- 0.25 micron gate width
- Tape and Reel packaging option available
- Point MTF > 300 years at 120°C channel temperature

Specifications

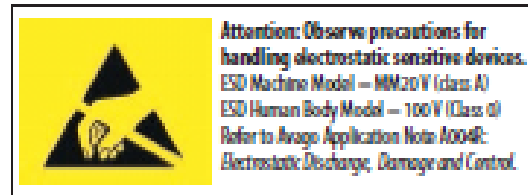
- 0.7 dB Fmin
- 9.0 dB Ga
- +22 dBm output 3rd order intercept
- +12 dBm output power

Applications

- Low Noise and Driver for Cellular/PCS and WCDMA Base Stations
- 2.4 GHz, 3.5GHz, 5-6GHz WLAN and WiMax notebook computer, access point and mobile wireless applications
- DBS 10 to 13 GHz receivers
- VSAT and SATCOM 13 to 18 GHz systems
- 802.16 & 802.20 BWA systems
- WLL and MMDS Transceivers
- General purpose discrete E-pHEMT for other ultra low noise applications

Notes:

1. The Avago enhancement mode pHEMT devices do not require a negative gate bias voltage as they are "normally off". They can help simplify the design and reduce the cost of receivers and transmitters in many applications from 500 MHz to 18 GHz



VMMK-1218 Absolute Maximum Ratings

Sym	Parameters/Condition	Unit	Max
Vds	Drain-Source Voltage ^[2]	V	5
Vgs	Gate-Source Voltage ^[2]	V	-5 to 1
Vgd	Gate-Drain Voltage ^[2]	V	-5 to 1
Ids	Drain Current ^[2]	mA	100
Igs	Gate Current	mA	1.6
Pdn	Total Power Dissipation ^[3]	mW	300
Pin	RF CW Input Power Max	dBm	10
Tch	Max channel temperature	C	+150
θjc	Thermal Resistance ^[4]	C/W	200

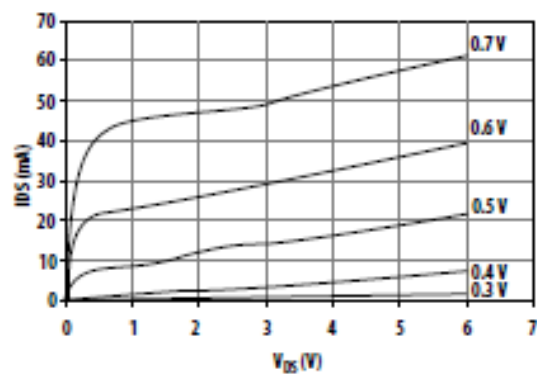


Figure 1. Typical I-V Curves. (VGS=0.1V per step)

Notes:

1. Operation in excess of any of these conditions may result in permanent damage to this device.
2. Assumes DC quiescent conditions
3. Ambient operational temperature $T_A=25^\circ\text{C}$ unless noted.
4. Thermal resistance measured using 150°C Liquid Crystal Measurement Method
5. The device can handle +10dBm RF Input power provided Igs is limited to 1mA

VMMK-1218 RF Specifications (on board)^[6,7]

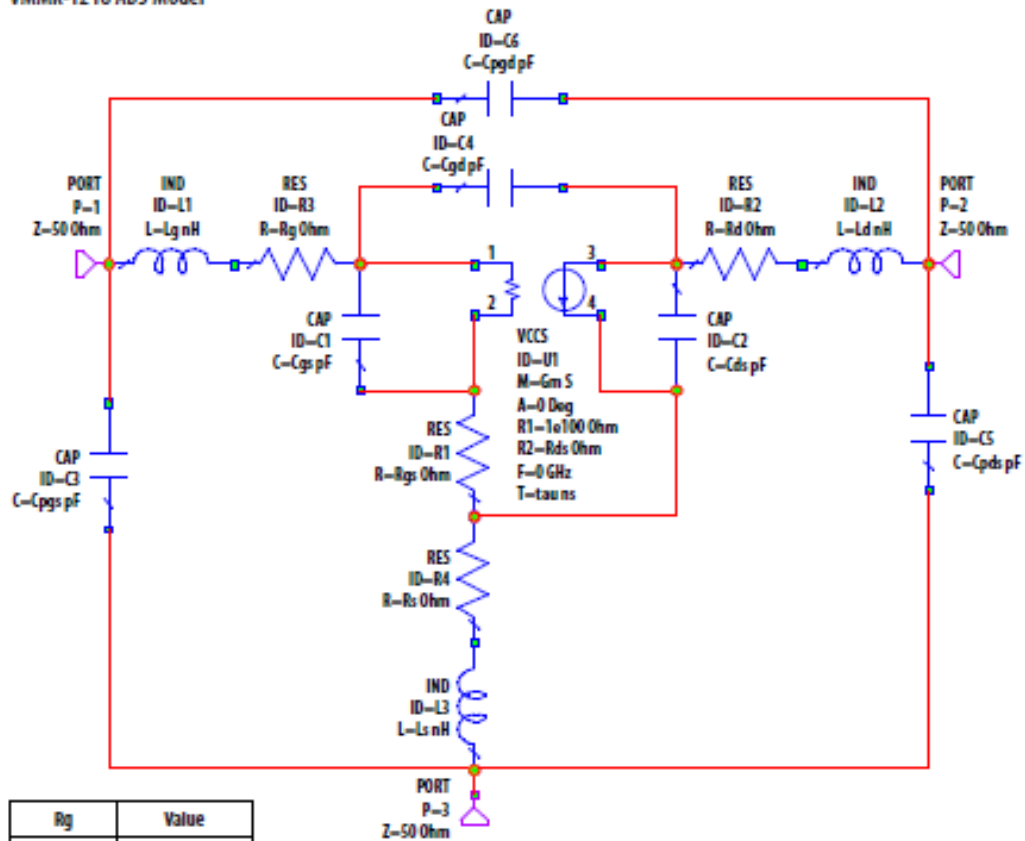
$T_A = 25^\circ\text{C}$, Freq = 10 GHz, Vds = 3V, Ids = 20mA, $Z_0 = 50 \Omega$ (unless otherwise specified)

Sym	Parameters/Condition	Units	Min	Typ.	Max
Vgs	Gate Voltage	V	0.48	0.58	0.68
Igs	Gate Current	μA		0.4	
Gm	Transconductance	mS		200	
Ga	Associated Gain	dB	6.7	9	10.2
NF	Noise Figure	dB		0.81	1.5
Fmin	Noise Figure min	dB		0.71	
P-1dB	1dB Compressed Output Power	dBm		+12	
OIP3	Output 3 rd Order Intercept Point	dBm		+22	

Notes:

6. Specifications are derived from measurements in a test circuit.
7. All tested parameters guaranteed with measurement accuracy $\pm 0.5\text{dB}$ for gain.

VMMK-1218 ADS Model



Rg	Value
Rg	4.729
Rd	1.29495
RdsG	2.283
Cpgs	0.0475
Cpds	0.0318
Cpgd	0.00417
Ls	0.000559
Lg	0.32446
Ld	0.2602

Appendix C

Component Data Sheet

SKYWORKS SKY65050-372LF



DATA SHEET

SKY65050-372LF: 0.45-6.0 GHz Low Noise Transistor

Applications

- Wireless infrastructure: WLAN, WiMAX, broadband, cellular base stations
- Test instrumentation
- LNA for GPS receivers
- Satellite receivers

Features

- Externally matched for wideband operation
- Noise Figure = 0.45 dB @ 2.4 GHz of device only
- Noise Figure = 0.65 dB @ 2.4 GHz including matching network loss
- Gain = 15.5 dB @ 2.4 GHz
- OIP3 = +23.5 dBm @ 2.4 GHz, $V_{DD} = 3\text{ V}$, $I_{DD} = 20\text{ mA}$
- P1dB = +10.5 dBm @ 2.4 GHz, $V_{DD} = 3\text{ V}$, $I_{DD} = 20\text{ mA}$
- Adjustable supply current, 5 to 55 mA
- Small, SC-70 (4-pin, 2.20 x 1.35 x 1.10 mm) package (MSL1, 260 °C per JEDEC J-STD-020)



Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to Skyworks Definition of Green™, document number SQ04-0074.

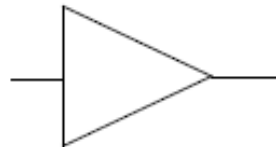


Figure 1. SKY65050-372LF Block Diagram

Description

The SKY65050-372LF is a high performance, n-channel low-noise transistor. The device is fabricated from Skyworks advanced depletion mode pHEMT process and is provided in a 2.20 x 1.35 x 1.10 mm, 4-pin SC-70 package.

The transistor's low Noise Figure (NF), high gain, and excellent 3rd Order Intercept Point (IP3) allow the device to be used in various receiver and transmitter applications.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

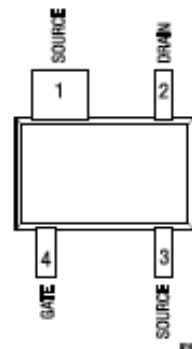


Figure 2. SKY65050-372LF Pinout - 4-Pin SC-70 (Top View)

Table 1. SKY65050-372LF Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	SOURCE	Source lead. Provides DC self-biasing point and AC ground.	3	SOURCE	Source lead. Provides DC self-biasing point and AC ground.
2	DRAIN	RF output. Requires external matching network for optimum performance. Supply voltage required through external RF choke.	4	GATE	RF input. Requires external matching network for optimum performance.

Table 2. Self-Biasing Resistors

Resistor Value (Ω)	Drain Current (mA)
130	5
47	10
27	15
20	20
15	25
10	30

Functional Description

The SKY65050-372LF is a depletion mode pHEMT designed for low noise, high frequency applications. The SKY65050-372LF has a typical NF of 0.65 dB tested at the 2.4 GHz wireless LAN frequency band. A gain of 15.5 dB typical is achieved using the same circuit. If the frequency of operation is lowered to the 1 GHz range, NF performance of the device can approach 0.5 dB including input matching network losses.

De-embedded scattering and noise parameters are provided in addition to typical circuit topologies for commonly used frequency bands. With an appropriate circuit, the SKY65050-372LF can be used for many applications from 450 MHz up to 6 GHz. The compact SC-70 package makes the SKY65050-372LF an ideal low noise and low cost solution.

Biasing

To properly bias a depletion mode pHEMT, both the gate and drain of the device must be properly biased. At $V_{GS} = 0$ V and $V_{DS} \geq 2$ V, the device is in a saturated state and draws the maximum amount of current, I_{DSS} . The device typically achieves the best noise performance at $V_{GS} = 3$ V and $I_{DSS} = 15$ mA. To control I_{DSS} , V_{GS} must be biased with a negative voltage supply.

To eliminate the need for a negative DC supply, self-biasing should be used when a resistor is placed between one of the source leads and ground. A bypass capacitor should be placed in parallel to this resistor to provide an RF ground and to ensure performance remains unchanged at the operating frequency.

When current flows from drain to source and through the resistor, the source voltage becomes biased above DC ground. The gate pin of the device should be left unbiased at 0 V, which creates the

desired negative V_{GS} value. This simplifies the design by eliminating the need for a second DC supply.

Table 2 provides the resistor values used to properly bias the SKY65050-372LF.

RF Matching Networks

The SKY65050-372LF Evaluation Board assembly diagram is shown in Figure 12 and a circuit schematic is provided in Figure 13. The schematic shows the recommended RF matching network used for the 2.4 GHz wireless LAN frequency band. The network was designed using de-embedded s- and n-parameters. The circuit was primarily tuned for gain, NF, and input and output return loss, while maintaining proper stability.

Optimal noise performance is attained when the impedance presented to the input of the amplifier is equal to its minimum NF impedance point. Components C1, C2, C3, L1, and L2 shown in Figures 12 and 13 provide the necessary impedance match for NF and input return loss. Circuit board and input matching structure losses on the input of the amplifier directly add to the overall NF of the amplifier. It is critical to minimize RF trace lengths and to use high-Q components to achieve optimal NF performance.

Components R2 and C14 provide self biasing for the device and RF grounding for one of the two source leads. Components C5 and L3 are placed on the opposing source lead and are used to tune the transistor's source inductance.

The effect of source inductance varies with frequency. Too little source inductance increases gain and high frequency stability, but at the cost of decreased in-band stability. Too much source inductance decreases high frequency stability and gain, but increases in-band stability. It is very important to find the optimum tuning of source inductance that balances all of these variables.

The output matching topology is typical for an RF transistor. Component L3 is the RF choke that prevents RF signals from reaching the DC supply. Component C4 is the DC blocking capacitor. Components C10 and C11 improve output return loss and 3rd Order Output Intercept Point (OIP3) performance.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY65050-372LF are provided in Table 3. The recommended operating conditions are specified in Table 4 and electrical specifications are provided in Table 5.

Performance characteristics for the SKY65050-372LF are illustrated in Figures 3 through 11.

Table 3. SKY65050-372LF Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input power	P _{in}			+10	dBm
Output power	P _{out}			+20	dBm
Drain source voltage	V _{ds}		6.0		V
Gate to source voltage	V _{gs}		-5.0		V
Gate to drain voltage	V _{gd}		-5.0		V
Drain current	I _{ds}		55		mA
Gate current	I _{gs}		100		μA
Power dissipation	P _{tot}		240		mW
Channel temperature	T _{ch}		150		°C
Storage temperature	T _{stg}	-65		+125	°C
Operating temperature	T _{op}	-40		+85	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to devices with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.



Attention: Observe Precautions for Handling Electrostatic Sensitive Devices

ESD Man-Machine (MM) Model = <50 V (Class A)

ESD Human Body Model (HBM) = 150 V (Class 0)

ESD Charge Device Model (CDM) = 500 V (Class 3)

Electrostatic Discharge (ESD) can damage this device, which must be protected from ESD at all times. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

Table 4. SKY65050-372LF Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage	V _{cc}	2	3	5	V
Supply current	I _{cc}	5	20	55	mA

Table 5. SKY65050-372LF Electrical Specifications (Note 1)

($T_{\text{or}} = +25\text{ }^{\circ}\text{C}$, Characteristic Impedance [Z_0] = 50 Ω , $V_{\text{DD}} = 3\text{ V}$, $I_{\text{DD}} = 20\text{ mA}$, Parameters include a 2.4 GHz Matching Network, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Saturated drain current	I_{DSS}	$V_{\text{GS}} = 2\text{ V}$, $V_{\text{DS}} = 0\text{ V}$	40	55	70	mA
Pinchoff voltage	V_{P}	$V_{\text{GS}} = 2\text{ V}$, $I_{\text{D}} = 2.5\%$ of I_{DSS}	-0.95	-0.80	-0.65	V
Transconductance	g_{m}	$V_{\text{GS}} = 2\text{ V}$, $g_{\text{m}} = \Delta I_{\text{D}} / \Delta V_{\text{GS}}$, measured at $I_{\text{D}} = 20\%$ of I_{DSS}	40	80	120	mS
Gate leakage current	I_{GSS}	$V_{\text{GS}} = V_{\text{DS}} = -3\text{ V}$		1	200	μA
Noise Figure	NF1 (Note 2) NF2 (Note 3)	@ 2.4 GHz		0.40 0.65	0.85	dB
Gain	IS211	@ 2.4 GHz	13.5	15.5	17.5	dB
Input return loss	IS111	@ 2.4 GHz		18.5		dB
Output return loss	IS221	@ 2.4 GHz		14		dB
Reverse isolation	IS121	@ 2.4 GHz		22.5		dB
3 rd Order Output Intercept Point	OIP3	$P_{\text{out}} = -10\text{ dBm/100e}$, $\Delta F = 1\text{ MHz}$, @ 2.4 GHz		+23.5		dBm
3 rd Order Input Intercept Point	IIP3	$P_{\text{out}} = -10\text{ dBm/100e}$, $\Delta F = 1\text{ MHz}$, @ 2.4 GHz		+8		dBm
1 dB Output Compression Point	OP1dB	@ 2.4 GHz		+10.5		dBm
1 dB Input Compression Point	IP1dB	@ 2.4 GHz		-4		dBm
Stability	K	Unconditionally stable, DC - 18 GHz		>1		-

Note 1: Performance is guaranteed only under the conditions listed in this Table and is not guaranteed over the full operating or storage temperature ranges. Operation at elevated temperatures may reduce reliability of the device.

Note 2: NF of device only. Input RF connector, board, and input matching network loss de-embedded from measurement.

Note 3: NF of device and matching network. Input RF connector and board loss de-embedded from measurement.

Typical Performance Characteristics

($T_{\text{or}} = +25\text{ }^{\circ}\text{C}$, Characteristic Impedance [Z_0] = 50 Ω , $V_{\text{DD}} = 3\text{ V}$, $I_{\text{DD}} = 20\text{ mA}$, Includes a 2.4 GHz Matching Network, Unless Otherwise Noted)

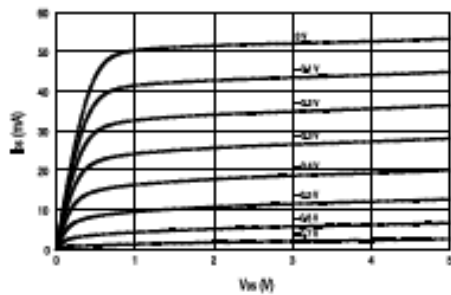


Figure 3. Typical IV Curves

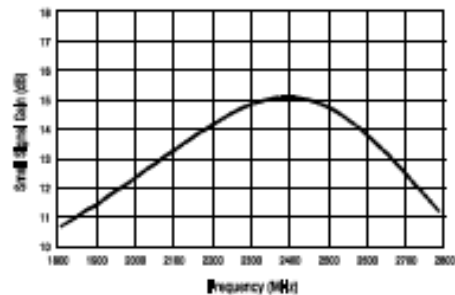


Figure 4. Small Signal Gain vs Frequency, $P_{\text{out}} = -20\text{ dBm}$

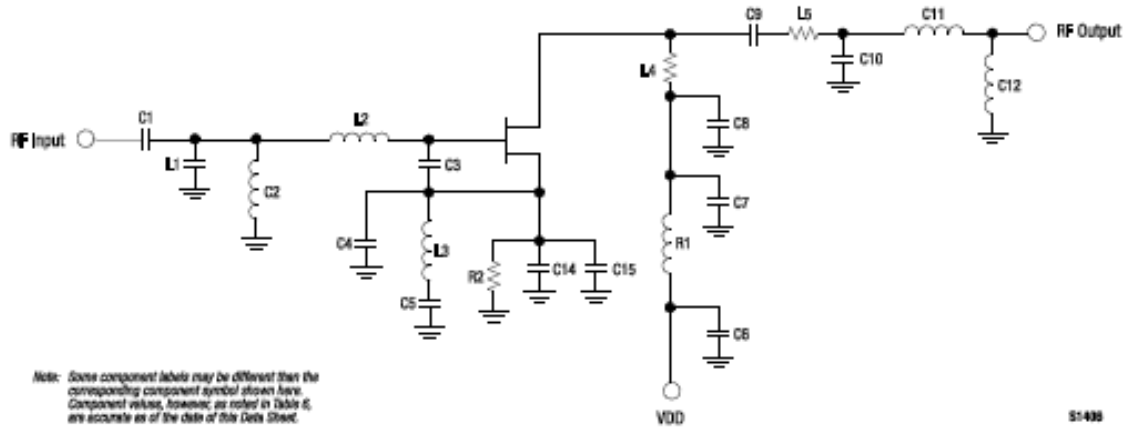


Figure 13. SKY65050-372LF Evaluation Board Schematic

Table 6. SKY65050-372LF (SC-70 Package) Evaluation Board Bill of Materials

Component	Value	Size	Manufacturer/Part Series
C1	20 pF	0402	Murata GJM
C2	8.2 nH	0402	Collicraft CS
C3	0.1 pF	0402	Murata GJM
C4, C7, C8, C13	DNP		
C5	1000 pF	0402	Murata GRM
C6	10 pF	0402	Murata GRM
C9	1.8 pF	0402	Murata GRM
C10	0.2 pF	0402	Murata GJM
C11	3.3 nH	0402	TDK MLG
C12	6.8 nH	0402	TDK MLG
C14	1000 pF	0402	Murata GRM
C15	1000 pF	0402	Murata GRM
L1	1.5 pF	0402	Murata GJM
L2	3.3 nH	0402	Collicraft CS
L3	1.6 nH	0402	TDK MLG
L4	3 Ω	0402	Panasonic
L5	0 Ω	0402	Panasonic
R1	2.2 nH	0402	TDK MLG
R2	20 Ω	0402	Panasonic

Appendix D

Component Data Sheet

NPX BRF93A

NXP Semiconductors

Product specification

NPN 6 GHz wideband transistor

BFR93A

FEATURES

- High power gain
- Low noise figure
- Very low intermodulation distortion.

APPLICATIONS

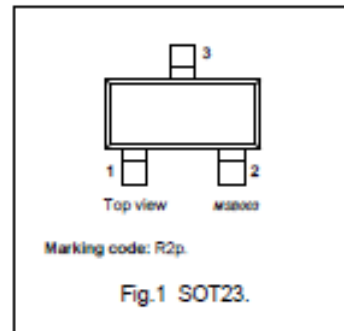
- RF wideband amplifiers and oscillators.

DESCRIPTION

NPN wideband transistor in a plastic SOT23 package.
PNP complement: BFT93.

PINNING

PIN	DESCRIPTION
1	base
2	emitter
3	collector



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{CB0}	collector-base voltage	open emitter	–	15	V
V_{CE0}	collector-emitter voltage	open base	–	12	V
I_C	collector current (DC)		–	35	mA
P_{tot}	total power dissipation	$T_s \leq 95\text{ }^\circ\text{C}$	–	300	mW
C_{re}	feedback capacitance	$I_C = 0$; $V_{CE} = 5\text{ V}$; $f = 1\text{ MHz}$	0.6	–	pF
f_T	transition frequency	$I_C = 30\text{ mA}$; $V_{CE} = 5\text{ V}$; $f = 500\text{ MHz}$	6	–	GHz
G_{UM}	maximum unilateral power gain	$I_C = 30\text{ mA}$; $V_{CE} = 8\text{ V}$; $f = 1\text{ GHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$	13	–	dB
		$I_C = 30\text{ mA}$; $V_{CE} = 8\text{ V}$; $f = 2\text{ GHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$	7	–	dB
F	noise figure	$I_C = 5\text{ mA}$; $V_{CE} = 8\text{ V}$; $f = 1\text{ GHz}$; $\Gamma_s = \Gamma_{opt}$; $T_{amb} = 25\text{ }^\circ\text{C}$	1.9	–	dB
V_O	output voltage	$d_{im} = -60\text{ dB}$; $I_C = 30\text{ mA}$; $V_{CE} = 8\text{ V}$; $R_L = 75\text{ }\Omega$; $T_{amb} = 25\text{ }^\circ\text{C}$; $f_p + f_q - f_r = 793.25\text{ MHz}$	425	–	mV

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CB0}	collector-base voltage	open emitter	–	15	V
V_{CE0}	collector-emitter voltage	open base	–	12	V
V_{EB0}	emitter-base voltage	open collector	–	2	V
I_C	collector current (DC)		–	35	mA
P_{tot}	total power dissipation	$T_s \leq 95\text{ }^\circ\text{C}$; note 1	–	300	mW
T_{stg}	storage temperature		–65	+150	$^\circ\text{C}$
T_j	junction temperature		–	+175	$^\circ\text{C}$

NPN 6 GHz wideband transistor

BFR93A

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to soldering point	$T_a \leq 95\text{ °C}$; note 1	260	K/W

Note

- T_a is the temperature at the soldering point of the collector pin.

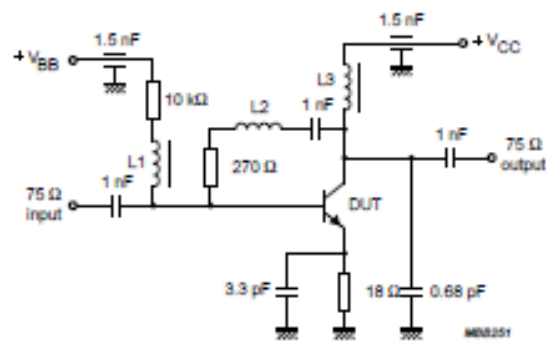
CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0$; $V_{CB} = 5\text{ V}$	–	–	50	nA
h_{FE}	DC current gain	$I_C = 30\text{ mA}$; $V_{CE} = 5\text{ V}$	40	90	–	
C_C	collector capacitance	$I_E = I_B = 0$; $V_{CB} = 5\text{ V}$; $f = 1\text{ MHz}$	–	0.7	–	pF
C_e	emitter capacitance	$I_C = I_C = 0$; $V_{EB} = 0.5\text{ V}$; $f = 1\text{ MHz}$	–	1.9	–	pF
C_{fb}	feedback capacitance	$I_C = I_C = 0$; $V_{CE} = 5\text{ V}$; $f = 1\text{ MHz}$; $T_{amb} = 25\text{ °C}$	–	0.6	–	pF
f_T	transition frequency	$I_C = 30\text{ mA}$; $V_{CE} = 5\text{ V}$; $f = 500\text{ MHz}$	4.5	6	–	GHz
G_{UM}	maximum unilateral power gain (note 1)	$I_C = 30\text{ mA}$; $V_{CE} = 8\text{ V}$; $f = 1\text{ GHz}$; $T_{amb} = 25\text{ °C}$	–	13	–	dB
		$I_C = 30\text{ mA}$; $V_{CE} = 8\text{ V}$; $f = 2\text{ GHz}$; $T_{amb} = 25\text{ °C}$	–	7	–	dB
F	noise figure (note 2)	$I_C = 5\text{ mA}$; $V_{CE} = 8\text{ V}$; $f = 1\text{ GHz}$; $\Gamma_s = \Gamma_{opt}$; $T_{amb} = 25\text{ °C}$	–	1.9	–	dB
		$I_C = 5\text{ mA}$; $V_{CE} = 8\text{ V}$; $f = 2\text{ GHz}$; $\Gamma_s = \Gamma_{opt}$; $T_{amb} = 25\text{ °C}$	–	3	–	dB
V_O	output voltage	notes 2 and 3	–	425	–	mV
d_2	second order intermodulation distortion	notes 2 and 4	–	–50	–	dB

Notes

- G_{UM} is the maximum unilateral power gain, assuming S_{12} is zero and $G_{UM} = 10 \log \frac{|S_{21}|^2}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)}$ dB.
- Measured on the same die in a SOT37 package (BFR91A).
- $d_{in} = -60\text{ dB}$ (DIN 45004B); $I_C = 30\text{ mA}$; $V_{CE} = 8\text{ V}$; $R_L = 75\ \Omega$; $T_{amb} = 25\text{ °C}$;
 $V_p = V_O$ at $d_{in} = -60\text{ dB}$; $f_p = 795.25\text{ MHz}$;
 $V_q = V_O - 6\text{ dB}$ at $f_q = 803.25\text{ MHz}$;
 $V_r = V_O - 6\text{ dB}$ at $f_r = 805.25\text{ MHz}$;
 measured at $f_p + f_q - f_r = 793.25\text{ MHz}$.
- $I_C = 30\text{ mA}$; $V_{CE} = 8\text{ V}$; $R_L = 75\ \Omega$; $T_{amb} = 25\text{ °C}$;
 $V_p = 200\text{ mV}$ at $f_p = 250\text{ MHz}$;
 $V_q = 200\text{ mV}$ at $f_q = 560\text{ MHz}$;
 measured at $f_p + f_q = 810\text{ MHz}$.



L1 = L3 = 5 μ H choke.
 L2 = 3 turns 0.4 mm copper wire; winding pitch 1 mm; internal diameter 3 mm.

Fig.2 Intermodulation distortion and second harmonic distortion MATV test circuit.

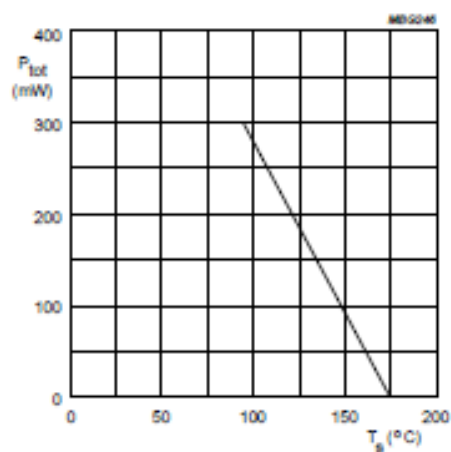
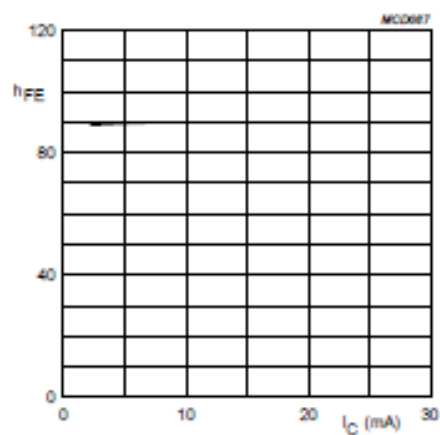


Fig.3 Power derating curve.



$V_{CE} = 5$ V; $T_j = 25$ °C.

Fig.4 DC current gain as a function of collector current.

Communications and publications

National communication

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Titre: Circuits Non Foster appliqués à un système Full-Duplex compact

Mots clés : Full-Duplex (FD), Non-Foster (NF), auto-interférence (SI), déphaseur, antenne électriquement petite (ESA), capacité négative, adaptation et découplage d'antennes

Résumé : Ce travail porte sur la réalisation d'un système FD compact (e.g. applications de type IoT) à partir de composants NF. Pour réaliser un Front-end FD, il est impératif de lutter contre l'auto-interférence (SI) élevée entre émission et réception. Le 1^{er} niveau de réduction de la SI intervient au plus près des antennes (1 TX et 1 RX) pour les miniaturiser puis pour les découpler/isoler l'une de l'autre. Le 2nd a pour fonction de supprimer la SI résiduelle en ajoutant à la réception un signal identique en amplitude à celle de cette interférence mais en opposition de phase. Cet étage requiert un déphaseur variable autour de 180° à environ 1.6GHz et un atténuateur. Comme la topologie retenue pour le déphaseur nécessite des capacités négatives, nos efforts ont d'abord ciblé la réalisation d'un circuit NF basé sur une paire croisée de transistors (XCP) qui constitue le bloc élémentaire de nos dispositifs. Plusieurs idées sont testées pour tendre vers une capacité négative large-bande idéale, mais un circuit stable n'a pu être obtenu qu'en conservant une résistance parasite résiduelle.

Ainsi le déphaseur 180° réalisé à base de composants NF voit ses performances être dégradées par rapport au cas idéal. La partie antennaire du front-end FD compact est constituée de 2 antennes planaires très rapprochées. La miniaturisation des antennes est faite en adaptant celles-ci à une fréquence plus basse (1.6 GHz) que leur bande initiale (2.3-2.4 GHz) ou elles sont alors considérées ESA. Une comparaison entre l'adaptation par des réseaux passifs et actifs NF montre que cette dernière permet un élargissement de la bande mais que l'efficacité du système n'est cependant pas améliorée en pratique. Cette limitation provient de la résistance parasite du circuit XCP NF. Le découplage entre antennes à l'aide de circuits NF montre à nouveau un meilleur niveau d'isolation et sur une bande élargie mais sans pénaliser l'efficacité dans ce cas. Au final, les 2 étapes découplage/annulation de la SI sont associés pour obtenir un système FD compact présentant un comportement large-bande de l'adaptation des antennes et de l'isolation (e.g. 45 dB d'isolation à 1,6 GHz). Des perspectives pour réduire la résistance parasite des circuits NF sont proposées pour améliorer l'efficacité du système.

Titre: Non-Foster circuits applied to Full-Duplex systems

Keywords : Full-Duplex, Non-Foster, Phase Shifter, Electrically small antenna (ESA), Antenna Quality factor

Abstract: This work focuses on achieving a compact FD system (e.g. for wireless IoT) based on NF circuit. The main issue when dealing with FD system is the high self-interference (SI) between transmitter and receiver chains. Thus a two stage-decoupling network is studied based on using NF circuits. In this two-level SI canceller, the 1st stage is placed close to the antennas in order to reduce their size, and also to decouple one from each other. The 2nd stage consists of a variable phase shifter and an attenuator. Our goal is to use NF circuit (based on cross-coupled pair of transistors: XCP) to build up a PS tunable around 180° at 1.6 GHz. We identified the origin and solved the stability issue while building a negative capacitance, but a spurious residual resistance remained whatever the improvements made. Our PS performance was thus degraded compared to ideal case.

SI cancellation at the antenna level was made by considering two planar monopole antennas (TX and RX). The antennas were miniaturized by making them operate at lower frequency than initially, and then they can be considered as ESA. A comparison between passive matching and NF matching networks showed a wider bandwidth for NF circuits but again the spurious resistor of NF circuit affects the system efficiency. NF circuits also allows improving the decoupling performance (bandwidth and level) compared to passive one but without degrading the efficiency in that case. Finally, we combined the two stages together to get a wideband matching and decoupling response (e.g. 45 dB of SIC at 1.6 GHz for our compact FD system). Some prospects are then put forward in order to face out the residual resistance issue.