Diamond MOSFET for power electronics

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Transistor MOS en diamant pour l'électronique de puissance

Diamond MOSFET for power electronics

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Introduction

Electrical energy production, distribution and consumption are at the core of our modern societies, necessary to support our standard of living. Following the increase of the global population and its quality of life in emerging countries, the electricity production is rapidly growing. The International Energy Agency evaluates the global electricity production at 25721 TWh in 2017, compared to 22829 TWh in 2012 and 19920 TWh in 2007 [1], and is expected to double by 2050 if following the same trend. This industrial activity is however not without serious collateral effects on the environment, in 2017 combustible fuels accounted for 66.8% of the total electricity production, at the origin of large amount of CO_2 production and air quality degradation amongst other things. Reducing the losses, occurring in transmission and distribution grids to deliver electricity to the population and industrial sites, is then an ecological stake. Part of these losses are due to power conversion systems based on semiconductor devices which convert the generated large AC power to a more suited form for transport or use by the consumer. Moreover, efficient power conversion is more and more needed in locomotive applications such as electric and hybrid cars whose use is rapidly growing.

At the heart of these systems, power semiconductor devices are crucial for their ability to sustain the high voltage, current and temperature required for such applications. At the moment, most of commercially available power converters are based on silicon thanks to the maturity of this technology. Silicon devices have an excellent ratio cost over performance supported by decades of extensive research and industrialization, but are now facing the limitations of this material physical properties. Device improvement is increasingly challenging and expensive as their design become more complex. At the opposite, a breakthrough is being achieved in recent years by the use of wide band gap semiconductors to replace silicon for high power applications, mainly supported by the already commercialized SiC and GaN. Other materials referred as ultra wide band gap semiconductors, the most studied ones being AlN, Ga_2O_3 and diamond, are under investigation for their possible use in power converters in the longer term. Their superior properties could lay the foundation for the next generation of power electronics devices. For example, for similar or higher current rating than bipolar silicon devices, unipolar wide band gap devices can be designed. This represents a huge gain in frequency operation and loss reduction.

Diamond as semiconductor is being researched for several decades. With intrinsic, p-type and n-type doping being controlled, diamond power devices have been demonstrated in recent years. But there are still technological challenges to solve before bringing these devices to exploit the full potential of diamond and produce them on a large scale. In

particular, toward the development of diamond MOSFETs which is the focus of this thesis, a number of issues have to be addressed:

(i) Implement reliable models for device design, taking into account the unique features of diamond.

(ii) Understand the physics of the interface between diamond and the oxide. Achieve a defect-free interface is key toward the fabrication of reliable and effective MOSFETs.

(iii) Describe and quantify the effect of the commonly used semi-insulating substrates on the lateral MOSFET devices.

(iv) Demonstrate experimentally the superior physical properties of diamond in a power MOSFET (higher off state blocking voltage and on state current).

To provide answers to these issues, this manuscript is organized as follows:

- Chapter 1: In this chapter, the context of power electronics will be introduced to show the superior properties of wide band gap semiconductors and diamond in particular for these applications. State of the art diamond power transistors will be presented at this occasion. Then, a particular architecture which is the focus of this work, the lateral deep depletion diamond MOSFET (D3MOSFET), will be introduced as a solution to obtain a MOSFET device taking advantage of the diamond bulk properties. The deep depletion concept will be described exhaustively and its originality in wide band gap materials evidenced. Next, state of the art physical models will be utilized to provide guiding rules to optimize the design of the D3MOSFET, as well as to benchmark the expected D3MOSFET performances.

- Chapter 2: The fabrication process will be detailed, including new steps added to the first demonstrated D3MOSFET by T. T. Pham during his PhD to improve performances, by reducing the contact resistances. The mask design will be established containing several different devices including MIM and MOS capacitors dedicated to the study of the oxide and the diamond/oxide interface.

- Chapter 3: A focus will be done on the diamond 1b semi-insulating substrate, commonly used for the fabrication of lateral diamond devices. The substrate electrical transport properties will be investigated to evidence in which cases it can be considered as a n-type doped semiconductor or an insulator, greatly impacting the device characteristics.

- Chapter 4: This chapter will address the parasitic charging effect occurring at the Al_2O_3/diamond interface, by means of impedance measurements, with a special care on their proper interpretation. The detrimental effect of the interface traps will be quantified and their dynamic discussed, leading to a discussion on previous reports of our group.

- Chapter 5: Finally, diamond resistivity and contact resistances will be extracted and compared to the model described in chapter 1. Then, the D3MOSFET transistor characteristics will be analysed for different temperatures and substrate bias conditions.

The impact of the effects evidenced in the chapters 3 and 4 on the D3MOSFET, originating from the oxide, the oxide/diamond interface and the substrate will be investigated. An on state and off state analysis will be provided to evaluate the device performances in comparison with other diamond FET.

Chapter 1

Diamond Deep Depletion MOSFET: concept and design

In this chapter, the context of power electronics will be introduced to show the superior properties of wide band gap semiconductors and diamond in particular for these applications. State of the art diamond power transistors will be presented at this occasion. Then, a particular architecture which is the focus of this work, the lateral deep depletion diamond MOSFET (D3MOSFET), will be introduced as a solution to obtain a MOSFET device taking advantage of the diamond bulk properties. The deep depletion concept will be described exhaustively and its originality in wide band gap materials evidenced. Next, state of the art physical models will be utilized to provide guiding rules to optimize the design of the D3MOSFET, as well as to benchmark the expected D3MOSFET performances.

1.1 Diamond and wide band gap materials, the future of power electronics devices

1.1.1 Specificity of power devices

Due to the wide range of production methods employed (fossil fuels, nuclear, wind, solar energy, hydroelectric, ...) and the constraints of the distribution, many conversions between Direct Current (DC) and Alternative Current (AC) may be required, as well as amplification, attenuation and close loop control (DC/DC and AC/AC conversions), between the production site and the delivery point. This is achieved by the use of transistors, thyristors and diodes semiconductor devices since the early 1950s as the first transistor was fabricated in 1947 by W. H. Brattain, J. Bardeen and W. Shockley and the first Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) in 1960 by M. Atalla and D. Kahng. They basically are electrical switches, with a conducting on state which is ideally a perfect conductor with no resistance, and an insulating off state with an infinite resistance. An example of a typical transistor characteristic is given in fig. 1.1 with the example of a three terminal enhancement mode n-type MOSFET. The current is flowing between the drain and source, while the transistor can be switched between on and off states by applying a gate to source bias.

Due to the inner physical limitations of the material, these devices have an on state resistance R_{ON}. This on state operation is generating heat losses, dependent on the designed breakdown voltage and the conductivity of the semiconductor. Moreover, MOSFETs are not perfect insulator in off state, a parasitic leakage current is flowing through the devices. For a high voltage, i.e. above the device capability, the breakdown occurs rendering the device conducting. The particularity of the power electronic devices is their capability to drive large amount of current in on state, typically in the order of 1 A to 100 A, and hold high voltages up to a few tens of Volts to dozens of kV with a low leakage current in off state. Due to the large current densities flowing through the device it is crucial for these applications to lower R_{ON} to improve the device efficiency and limit the conduction losses, as thermal management is a key design feature. Moreover, it is of importance that the devices are able to safely hold the large voltages needed to be converted in many applications. The maximum drain-source voltage that a device can sustain before breaking is referred as V_{BD}.

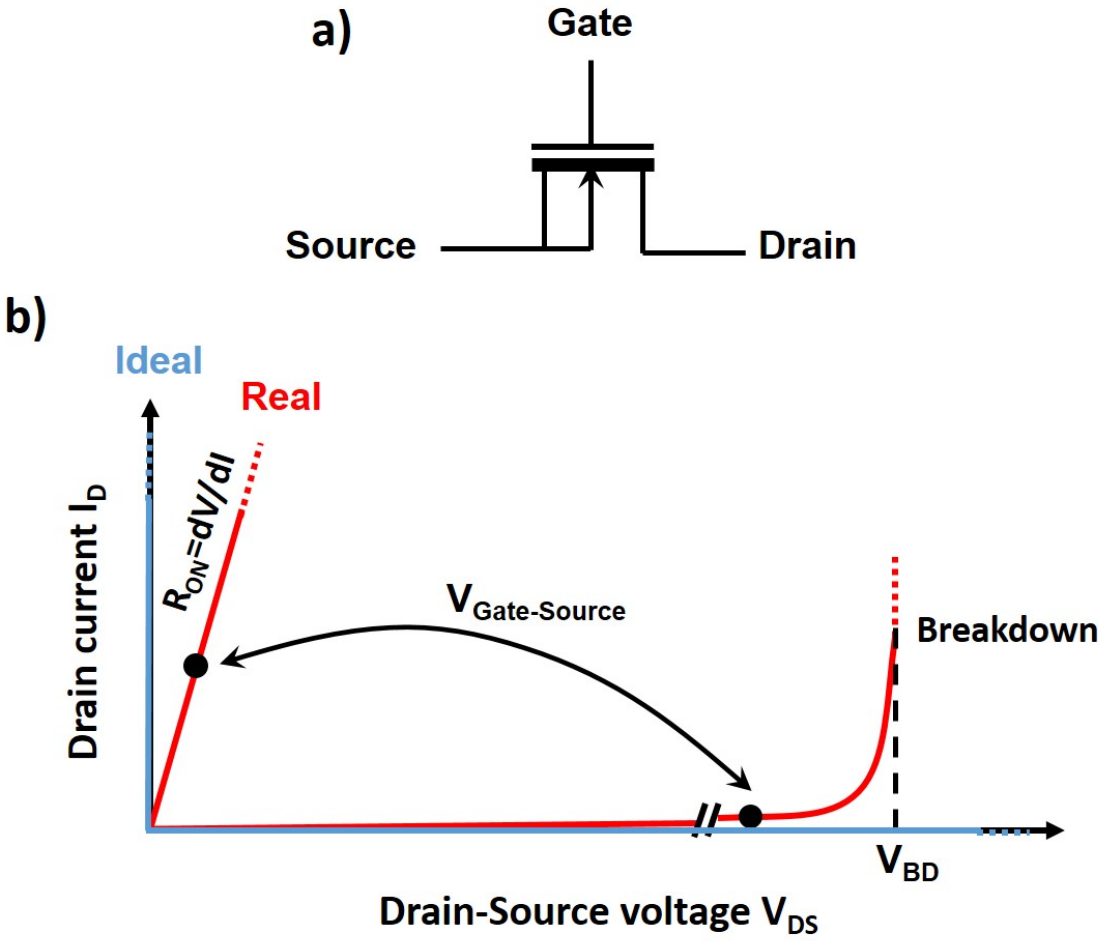


FIGURE 1.1: a) Enhancement mode n-type MOSFET symbol and b) its schematic transistor characteristic in on and off state for an ideal and a real transistor. In on state the device is biased with a low V_{DS} with the maximum drain current, in off state the device has to block a high V_{DS} with minimum leakage current.

1.1.2 Principle of power conversion

An example of DC/DC buck converter is shown in fig. 1.2 a) to illustrate the concept of power conversion. It uses the transistor to periodically open and close the circuit so the average output voltage is lower than the input voltage. The control of the transistor's gate to produce the periodic signal is done by using a gate driver. To remove the switching harmonics and obtain a constant output voltage, a L-C low-pass filter with a cut-off frequency much lower than the switching frequency is added.

As shown in fig. 1.2 c), in reality a power device cannot switch between on and off state instantaneously. The power converter requires a duration t_{ON} to switch from on to off state and t_{OFF} to switch from off to on state. Therefore for a short duration during each commutation cycle of period t_{cycle} there are significant switching energy losses E_{switch}^{ON} and E_{switch}^{OFF}. The average switching power loss during a cycle is:

$$P_{switch} = (E_{switch}^{ON} + E_{switch}^{OFF})/t_{cycle} = \frac{1}{t_{cycle}} \left(\int_{t_{ON}} V_{DS}(t) \times I_D(t) dt + \int_{t_{OFF}} V_{DS}(t) \times I_D(t) dt \right) \tag{1.1}$$

Assuming a constant on state drain current I_D^{ON}, the average conduction loss during a cycle is:

$$P_{cond} = t_\alpha \times R_{ON} \times {I_D^{ON}}^2 / t_{cycle} \tag{1.2}$$

The total losses is the sum of these two effects:

$$P_{loss} = P_{switch} + P_{cond} \tag{1.3}$$

Some of the interest of MOSFET devices for power electronics is their short theoretical t_{ON} and t_{OFF} and high switching frequency, limiting the switching losses, as well as the low power required to drive the gate compared to a bipolar design. But silicon MOSFETs usually have a low breakdown voltage compared to other designs, limiting their use to less than 1 kV applications or requiring them to be stacked which is cancelling their advantages. In this context, wide band gap semiconductors offer a solution to increase the performances of MOSFET power devices to allow their use in a much higher range of applications.

1.1.3 Wide band gap semiconductors for power electronics

As present time most of the power electronic market is dominated by silicon devices, due to its availability and the maturity of this technology. Thyristors can reach blocking voltages up to 10 kV, but with very low operating frequencies (100 Hz) and waveforms difficult to manage [2], which limits the range of applications they can be used in. On the other hand the Insulated Gate Bipolar transistors (IGBT), one of the most used power device, can operate at higher frequency up to 100 kHz with lower blocking voltages up to 6.5 kV [3]. Silicon MOSFETs are used in lower power applications as the blocking voltage is limited to around 1 kV, but have a higher switching speed up to a few MHz. Improving the

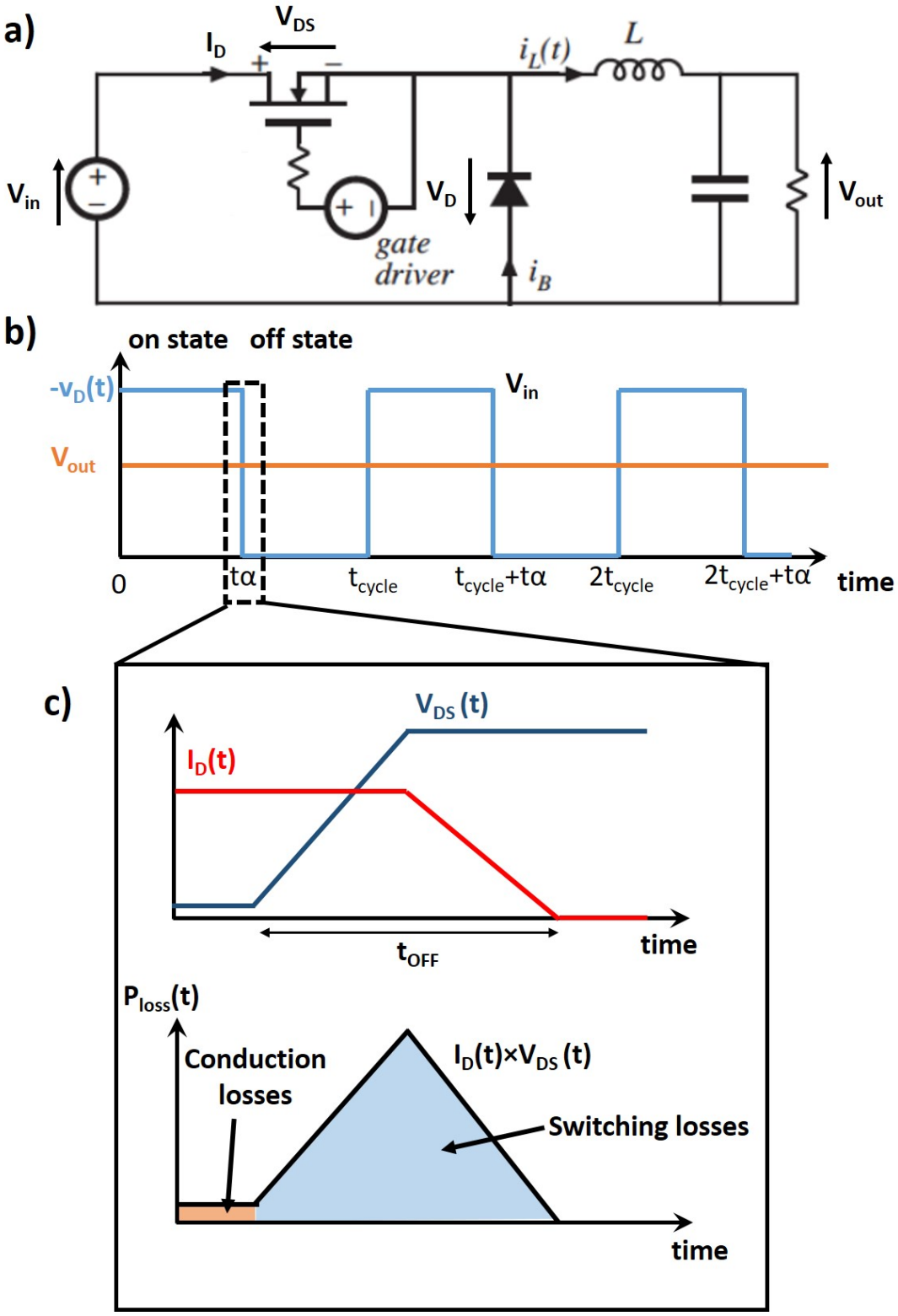


FIGURE 1.2: a) Electrical circuit of the power DC/DC buck converter, b) example of the ideal waveforms of the input voltage V_{in} and the output voltage V_{out} and c) drain current and drain-source voltage in the transistor. Due to the transition duration between on and off state there are losses at each cycle.

performances of the silicon power devices is increasingly challenging and costly, as they are intrinsically limited by the silicon physical properties. More and more complex architectures are required, which are more expensive to fabricate. They are facing limitations in terms of blocking voltage due to the relatively low breakdown field of silicon (0.2 to 0.8 MV/cm, depending on the device breakdown voltage rating), which requires to stack devices or power converters in series to match the high voltage applications requirements. Moreover the thermal management is a critical issue, limiting the operating temperature to less than 175 °C and necessitating cumbersome cooling systems.

In this context, research on wide band gap materials have been gaining interest in recent years and their integration improves performance of power converters. They possess more suitable properties for power electronics than silicon. The main physical properties are summarized in tab. 1.1, it has been chosen to not detail in this manuscript how they were determined. One can refer to [4] for more informations. Thanks to their wider band gap than silicon, more than three times its value, the energy required to provoke the avalanche breakdown phenomena is puched back. It results in a much higher critical field than silicon, meaning that higher doping levels can be used for devices with comparable blocking voltages. The benefit is double, there is a higher concentration of carriers as well as a reduced device size, for a comparable or higher carrier mobility. The device resistance is lowered by a factor 10 to 100 compared to silicon. Moreover, in wide band gap materials, electrons from the valence band needs more thermal energy to be excited to the conduction band. The intrinsic carrier concentration in these materials is much smaller than in classic semiconductors and does not, in most cases, constitute a limitation for high temperature operation as it is in silicon. They are well suited for high operating temperatures above the silicon limit and are instead limited by other temperature dependent physical effects or packaging issues. It is in fact common that the resistivity of ultra wide band gap semiconductors (>4 eV) is improved above room temperature, due to the incomplete ionization of dopant which is discussed in the present chapter.

	Si	4H-SiC	GaN	Ga_2O_3	Diamond
Bandgap E_G (eV)	1.10	3.26	3.43	4.9	5.5
Electron saturation drift velocity (10^7 cm/s)	1.1	1.9	2.5	2	2.7
Hole saturation drift velocity (10^7 cm/s)	0.8	1.2	-	-	1.1
Electron mobility (cm^2/V.s)	1500	1000	1500	300	1000
Hole mobility (cm^2/V.s)	450	120	200	-	2000
Breakdown field (MV/cm)	0.2-0.8	1-4	2-4	8	4-10
Relative dielectric constant	11.9	9.8	8.9	9.9	5.7
Thermal conductivity (W/mK)	150	490	130	23	2200

TABLE 1.1: Key physical properties at room temperature of Si, SiC, GaN, Ga_2O_3 and diamond. The breakdown field is dependent on the device voltage rating, a range is thus provided, excepted for Ga_2O_3 due to the lack of experimental data.

SiC devices are already commercialized and have in practice demonstrated the superior properties of wide band gap semiconductors, for high temperature and high voltage

applications with reduced size. SiC packaged MOSFETs are currently available with blocking voltages up to 1.7 kV but are demonstrated to hold more than 15 kV in off state [5, 6] and IGBT up to 27 kV [7] with lower $R_{ON,S}$ than silicon devices, as illustrated in fig. 1.3.

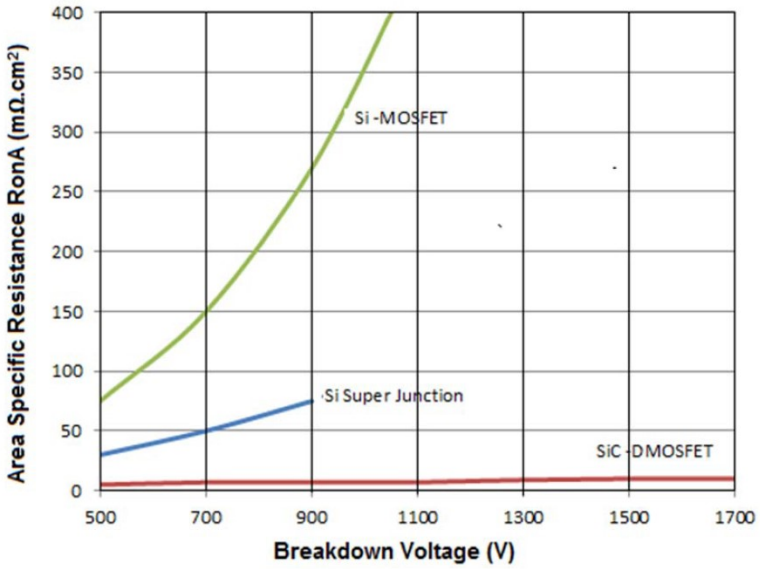


FIGURE 1.3: Comparison between Si and SiC MOSFET, courtesy to Alves et al. [8], Copyright ©2017, IEEE.

GaN devices are also recently commercialized, for lower voltage (<1 kV) and higher switching frequency (in the MHz range) applications than SiC devices. Due to the lack of affordable large surface and high quality GaN substrates, these devices use different designs than SiC and Si devices. Heteroepitaxial GaN layers grown on sapphire or silicon substrates are more economical, but have a lower crystalline quality due to bowing and cracking. For this reason most of GaN devices are lateral, such as the High Electron Mobility Transistor (HEMT). The 2D electron gas created at the hetero-junction of an AlGaN/GaN interface is used to conducts the current. Vertical devices are nonetheless investigated [9] but are not commercialized yet.

Diamond appears to have the best properties of the four semiconductors compared. It has a higher critical field, both high hole and electron mobility. Its exceptional thermal conductivity is also a property that considerably facilitate thermal management, requiring a less invasive cooling system and allowing to use higher power density without damaging the device.

In the recent years, the fabrication of diamond power devices has been made possible by progress in the control of doping and growth [10]. Since ion implantation doping is much more complicated in diamond than in other common semiconductors, especially for n-type [11], incorporation of dopant during the epitaxy by Chemical Vapour Deposition (CVD) is the preferred method. CVD growth of electronic grade p-type (boron doped) diamond is well controlled over a range of a few 10^{14} cm^{-3} to around 10^{21} cm^{-3} in (100) plane and is commercially available [12]. n-type (phosphorous doped) diamond growth

is also controlled, however in the (111) plane, but phosphorous atoms are less soluble in diamond than boron, limiting the maximum doping concentration to 5×10^{19} cm^{-3} up to now. It is however worth noting that boron and phosphorous are deep dopant, with ionization energy of 380 meV and 570 meV respectively, and that no shallow dopant have been found at the moment. The fabrication and control of diamond PN junction is challenging due to their different preferred crystallographic growth plane. Two approaches have been used, one is to perform lateral growth on the optimal growth plane, however an etching is necessary to create walls on which the growth occurs. This was commonly used for JFET fabrication [13, 14, 15, 16, 17, 18, 19]. The other approach is to grow layers on top of each others, either by using (100) or (111) oriented substrates. Despite the challenging incorporation of one of the dopant during growth, promising results could be obtained on p-i-n diodes [20, 21] thanks to the use of a miscut angle [22]. The control of both p-type and n-type with similar electron and holes mobilities, in contrast of GaN and SiC, is an important feature making possible the fabrication and integration of both diamond N-MOS and P-MOS.

Substrates are at the core of the development of diamond electronics. Device fabrication requires them to have a defect density as low as possible as they tend to propagate to the epitaxial layers during growth, significantly deteriorating the device performances. Most of the electronic grade substrates currently available are grown by High Pressure High Temperature (HPHT) method of which three types can be distinguished:

(i) Type Ib diamonds contain a large number of nitrogen impurities in isolated sites, giving it a yellow tint. This type of substrate is used for its insulating properties, as nitrogen is a deep donor in diamond which requires considerable thermal energy to ionize. Since most of demonstrated diamond transistor devices are lateral, they are commonly used to avoid substrate conduction. They also allow to fabricate multiple devices on the same substrate and isolate them by etching the conductive epitaxial layers between them, making it possible to parallelize them [23].

(ii) Type IIa diamonds contain less impurities and are colourless. They are less available and not frequently used to fabricate devices.

(iii) Type IIb diamonds contain a high concentration of boron atoms, typically in the order of $[B] = 10^{19}$ cm^{-3}. Their conductivity make them useful as a solution for the fabrication of vertical devices. Growing freestanding heavily boron doped layer by CVD is another possibility but is still challenging, requiring considerable optimizations to avoid the features described in [24], although demonstrated in [25] with thickness ranging from 100 μm to 260 μm with boron concentrations up to $[B] = 10^{20}$ cm^{-3}. The current low crystalline quality of diamond heteroepitaxial layers are however a challenge to device fabrication. The pseudo-vertical architecture is thus frequently employed to circumvent the need for thick layers. In that case less defective Ib and IIa diamond substrates can be used to grow a heavily doped layer from a few nm to a few μm, which does not severely increase the defect density. This is a less ideal solution in terms of design, but is much easier to fabricate at the moment. Similarly, the corner architecture [26] can be employed but is more complex to fabricate.

The ongoing concern for future diamond electronics is the substrate size. HPHT diamond plates have limited size. They can be purchased with a surface up to 1 cm^2, far from the standard wafer diameter in silicon technology (up to 300 mm), which is limiting the adaptability of many fabrication process and is increasing the eventual cost of commercial diamond devices. In order to make it competitive with other materials, wafers of a few inches of diameter would be a milestone. In recent years different methods have been investigated, H. Yamada et al. [27] achieved to fabricate a 40×60 mm^2 wafer by connecting multiple smaller plates in a mosaic. The process was then later improved to show no effect of the boundaries on the device performances [28]. Heteroepitaxy is another approach investigated to obtain large sized wafers, similarly to what is employed in GaN technologies. M. Schreck et al. succeeded in the growth of a 92 mm diameter freestanding diamond wafer by CVD on an iridium substrate [29]. These solutions however need more improvements to match the strict requirements of electronic device fabrication, in terms of crystalline quality and reproducibility, but offer promising results toward the future availability of inches-sized diamond wafers.

1.1.4 Diamond surface termination

Depending on the surface termination of diamond opposite surface properties can be observed, from conducting to insulating. The surface transfer doping describes the mechanism by which a diamond surface covered with electron accepting reservoirs is conducting [30, 31, 32, 33]. It is not a physical mechanism specific to diamond, but the absence of a solid native oxide able to passivate the surface makes the surface chemistry particularly important. Exposing the diamond surface to various species changes drastically its electron affinity and thus its conductivity [34, 35, 36, 37], finding application in bio-sensing for example [38]. Surface conduction is achieved by hydrogenating the diamond surface, typically with an hydrogen plasma, and the resulting material is referred as H-terminated diamond. Hydrogen termination can also be achieved electrochemically [39]. As shown in fig. 1.4, prior to charge exchange with the surface acceptors the conduction band in the neutral region is above the vacuum level, due to the negative electron affinity. The subsequent electron transfer from the valence band to the acceptor states creates a hole gas on the surface, with a typical surface density of the order of 10^{12} to 10^{13} cm^{-2}. It appears that even after an oxide or metal deposition the H-terminated diamond surface keeps its conducting property, allowing to use this concept to fabricate MOSFETs and MESFETs with a 2D surface hole conduction. One of the advantage of these designs is their relative simplicity to fabricate. No heterojunctions are needed as it is required for GaN/AlGaN HEMT. They moreover circumvent the low conductivity of bulk diamond at room temperature due to the high ionization energy of dopant, making easier to obtain larger current density devices at low and room temperature. The downside of this concept comes from the close proximity of the negatively charged surface acceptors with the 2D hole gas, the carrier mobility is limited by surface impurities to values ranging between 50 and 300 $cm^2/(V.s)$ [4] and increasing the carrier concentration dramatically decrease the hole mobility. A recent work by Sasama et al. [40], using hexagonal-BN as gate dielectric in a FET device,

has however obtained a hole mobility independent of the 2D gas hole concentration, indicating that another mechanism is limiting the mobility. This work is still recent and more studies have to be performed to understand this structure. In addition, the 2D hole gas is not stable over time and is difficult to control, making the fabrication of reliable device challenging.

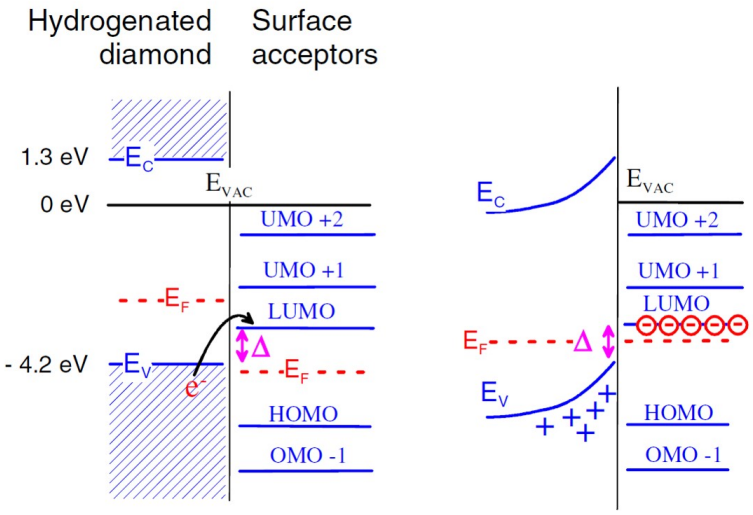


FIGURE 1.4: Schematic energy diagram to illustrate p-type surface transfer doping of hydrogenated diamond. The left-hand side refers to neutral diamond and neutral surface acceptors prior to charge exchange. The zero of the energy scale is the vacuum level. OMO and UMO refer to occcupied and unoccupied molecular orbitals, respectively and HOMO and LUMO to the highest and lowest OMO and UMO, respectively. The right-hand side displays the band diagram in equilibrium. Note that the alignment of energy levels intimately at the surface is unchanged. Courtesy to [30]

To passivate the diamond surface, oxygen termination is used. Electron affinity between O and H-terminated surfaces are different [41] so that a positive surface potential build up instead of a negative one for H-termination, depleting part of the surface. The most common and efficient way up to now to achieve oxygen termination is by the use of UV ozone treatment [42]. This treatment has the advantage of not deteriorating the surface, as it can otherwise be the case with a wet chemical oxidation. Insulating properties are conserved after oxide or metal deposition and are stable over time. The interest of O-terminated devices over H-terminated is to control the bulk properties of diamond, more reliable and stable, as well as opening the way for efficient vertical structures which are optimal in terms of power density integration.

1.1.5 Recent advance in diamond MOSFET devices

The progresses made within the past years regarding the doping and growth control of diamond, as well as the oxide/diamond and Schottky interfaces, have made possible the successful fabrication of diamond Field Effect Transistors: Metal Semiconductor FET (MESFET) [44, 51], H-terminated FET (HFET) [52, 53, 54, 45, 55, 56, 57], Junction FET

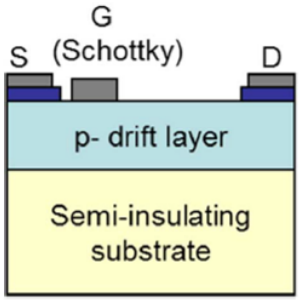
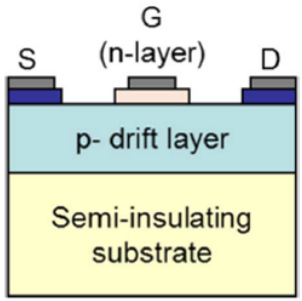
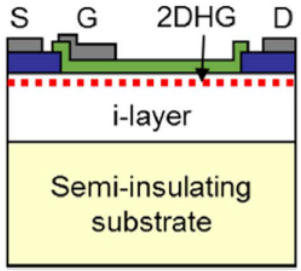
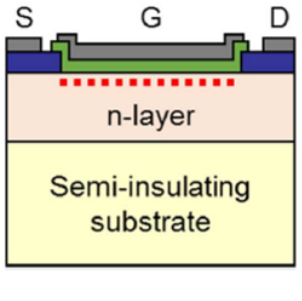
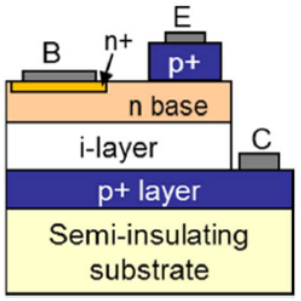
Type	Unipolar				Bipolar
Device	MESFET	JFET	H-FET	MOSFET	BJT
Structure					
V_{max}	2.2 kV [to be published]	> 600 V [55]	2 kV [68]	< 50 V	< 50 V
E_{max}	*2.1 MV/cm* [50]	*> 6 MV/cm* [55]	*3.6 MV/cm* [69]		
I_{max}	30 mA	*450 A/cm²* [57]	*1.3 A/mm* [62]	< 1 mA	< 1 mA
J_{max}	*< 3 mA/mm@250 C*	*(bipolar mode)*			
Remarks	Stable operation @ 500 °C & after 10 MGy X-rays	Normally off High T Bipolar mode	Shallow channel f_{max} > 100 GHz Normally-on/off Vertical structure	Inversion channel (normally-off)	
Challenge	Vertical structure	Vertical structure High n+ doping	Reliability Doping control	High Vr Vertical structure Mobility	Long lifetime of electron Low n+ layer resistivity

FIGURE 1.5: Summary of diamond switching devices, courtesy to H. Umezawa [43]. See references [44] for MESFET, [17, 15] for JFET and [45, 46, 47] for H-FET. For additional references on the D3MOSFET not shown in this figure, see [48, 49, 50].

(JFET) [15, 16, 17, 18, 19], inversion MOSFET [58] and Diamond Deep Depletion MOSFET (D3MOSFET) [48, 49, 50]. A summary of these devices designs and performances is shown in fig. 1.5 by H. Umezawa in ref.[43]. High breakdown voltage diamond FET devices have been successfully demonstrated, with a record of 1.5 kV [44] using a O-terminated diamond MESFET and 2 kV with a H-terminated diamond MOSFET [45]. These performances are promising considering the simple architectures of these devices, with basic or no edge terminations, which are a key design to improve the breakdown voltage.

However, the use of diamond as power electronic material is currently facing a number of limitations related to device fabrication. Due to these challenges, the lateral structure has been the preferred geometry because it generally requires less process fabrication steps, thinner diamond CVD layers and no deep etching.

In this context where diamond FETs are recent innovations, there is a need to explore and understand the underlying diamond FET physics. This work is focused on the D3MOSFET which take advantage of the deep depletion concept in wide band gap semiconductors to operate an O-terminated diamond MOSFET. This chapter will describe the deep depletion concept and its use to operate the D3MOSFET, key parameters and physical models will be explained in order to optimize the device's design.

1.2 The lateral deep depletion diamond MOSFET

1.2.1 The working principle of the lateral deep depletion diamond MOSFET

Basic working principle

The working principle of the D3MOSFET is detailed in [50], it can be summarized by the schematic cross section depicted in fig. 1.6. The lateral conduction between the drain and source ohmic contacts is made through the bulk of a p-type (boron doped) diamond layer grown on a 1b diamond semi-insulating substrate. The advantages of using the bulk conduction is to reach the bulk mobility of carriers (1000-2000 $cm^2/(V.s)$), which is higher than reported values in diamond H-terminated MOSFET (50-300 $cm^2/(V.s)$), as well as having a better understanding of the physical mechanism behind the electrical conduction and blocking capabilities. Indeed, the surface accumulation of 2D hole gas (2DHG) obtained by the surface transfer mechanism is difficult to control, with non reproducible characteristics and it is not clear how the electric field is distributed in the off state of these devices. They typically exhibit a linear relationship between the drain-gate distance L_{GD} and the breakdown voltage BV, with a ratio BV/L_{GD} around 1-2 MV/cm [52], far from the diamond breakdown field. However, a severe drawback of this bulk conduction design is caused by the high ionization energy of boron acceptor in p-type diamond (380 meV), at the origin of a large negative temperature coefficient above room temperature of the device resistance. These points will be discussed in this chapter. To modulate the conductivity of the device and observe the transistor field effect, a Metal-Oxide-Semiconductor (MOS) gate stack is used. When biased, the electric field created is repelling or accumulating majority carriers below the gate depending on the polarization sign, in an area called

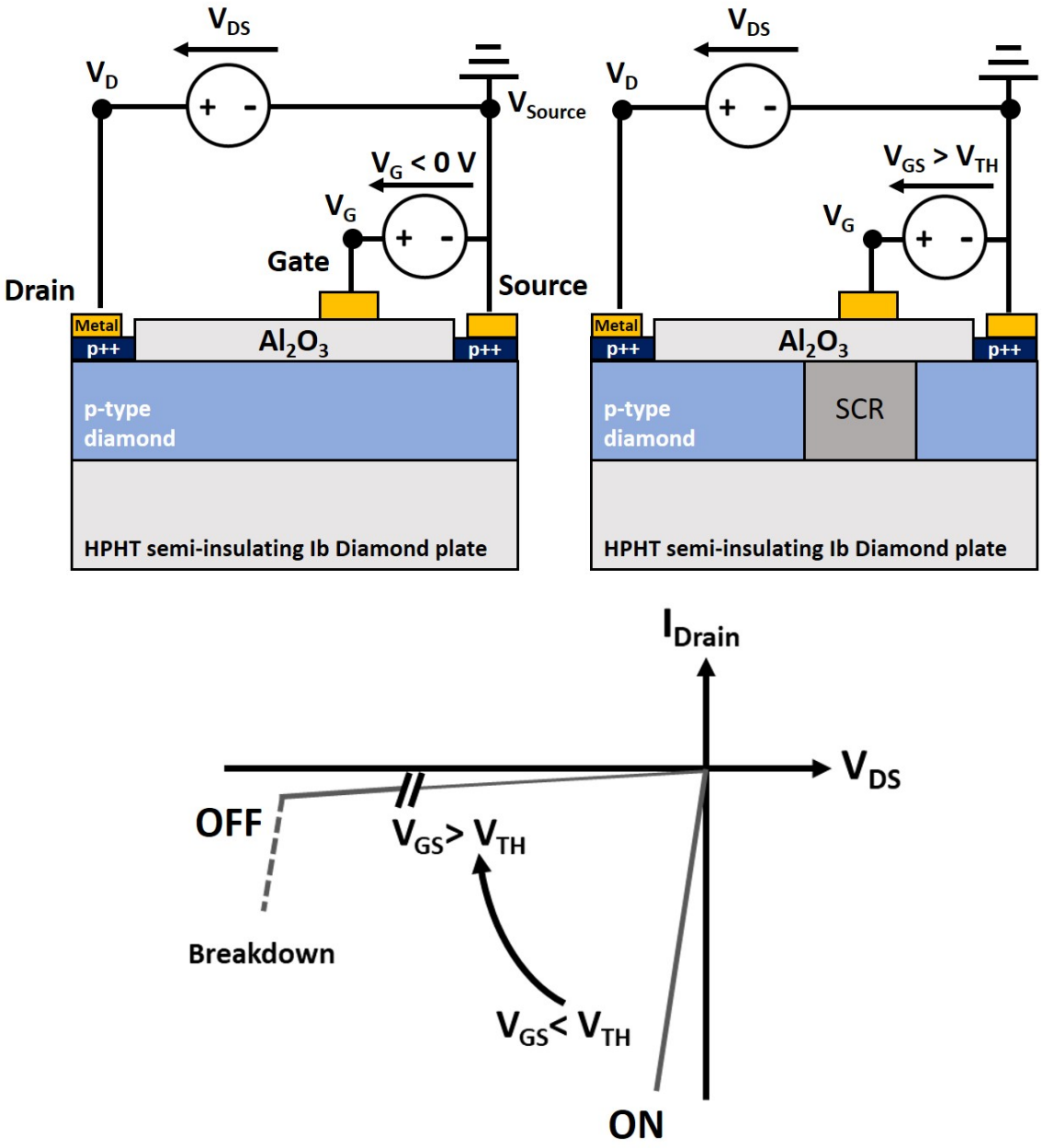


FIGURE 1.6: Schematic cross section of the p-type diamond deep depletion MOSFET device in on and off state with the corresponding schematic current voltage characteristic.

Space Charge Region (SCR) of thickness W_{SCR} . The device is typically normally-on and the off state is obtained for a gate bias equal or higher than the threshold voltage V_{TH}, at which W_{SCR} is equal to the channel thickness. Thanks to the deep depletion concept in wide band gap semiconductors, W_{SCR} can be designed much larger than when using a lower band gap material such as silicon.

The working regimes of this transistor design will be clarified in this chapter as well as the wide band gap deep depletion regime specificity.

Deep depletion regime: a concept for wide band gap semiconductor transistor

To explain the originality of the deep depletion regime in wide band gap semiconductors, it is useful to remind the working regimes of a MOS Capacitor (MOSCap). The fig. 1.7 represents the 3 main working regimes of a p-type MOSCap following the charge equilibrium equation [59]:

$$Q_{SC} = -sign(V_S)\frac{\sqrt{2}k_BT\epsilon_0\epsilon_{SC}}{qL_D}F(T,V_S,V_B) \tag{1.4}$$

Where Q_{SC} is the charge in the semiconductor side of the MOS, L_D[1] the Debye length , V_S[2] the surface potential and $V_B = \frac{k_BT}{2q}log(\frac{ni(T)^2}{p_0(T)^2})$[3], the potential difference between the Fermi level and the intrinsic Fermi level in the bulk neutral region. $q = 1.6^{-19}$ C is the elementary charge, $k_B = 1.38^{-23}$ J/K is the Boltzmann constant, $\epsilon_0 = 8.85^{-12}$ F/m is the vacuum permittivity, ϵ_{SC} is the relative dielectric constant of the semiconductor (5.7 for diamond) and T the temperature in Kelvin.

The function $F(T,V_S,V_B)$ describes the variations as function of the surface potential:

$$F(T,V_S,V_B) = \sqrt{[e^{\frac{-qV_S}{k_BT}} + \frac{qV_S}{k_BT} - 1] + e^{\frac{-2V_B}{k_BT}}[e^{\frac{qV_S}{k_BT}} - \frac{qV_S}{k_BT} - 1]} \tag{1.5}$$

(i) For V_S negative, the exponential part of the left term of equ. 1.5 is dominant, the MOS is in forward regime (also referred as accumulation regime) where majority carriers are accumulated in a 2D hole gas at diamond/oxide interface, no depletion layer occurs.

$$Q_{accumulation} \propto e^{\frac{-qV_S}{k_BT}} \tag{1.6}$$

(ii) For $V_S < 2V_B$, the MOS is biased in the depletion regime. An insulating depleted region extends in the semiconductor and equ. 1.5 is showing a square root dependence as function of the surface potential.

$$Q_{depletion} \propto \sqrt{V_S} \tag{1.7}$$

(iii) For $V_S > 2V_B$, the MOS is biased past the inversion threshold V_{Inv} defined by the condition $V_S = 2V_B$. Minority carriers are thermally generated from the conduction band to the valence band since at the oxide/semiconductor interface the Fermi level is closer to the conduction band, analogous to a n-type doping. It results in the creation of a 2D electron gas in what is called the inversion regime, described by the exponential part of the right term of equ. 1.5:

$$Q_{inversion} \propto e^{\frac{q(V_S-2V_B)}{k_BT}} \tag{1.8}$$

[1] $L_D = \sqrt{\frac{k_BT\epsilon_0\epsilon_{SC}}{q^2p}}$ where p is the neutral region hole density.

[2] The relation between V_S and the bias applied on the gate metal V_G is $V_G = V_S + V_{OX}$ depending on the potential drop across the oxide V_{OX}, given by $V_{OX} = \frac{Q_{SC}}{C_{OX}}$ where C_{OX} is the oxide capacitance.

[3] $n_i(T)$ is the intrinsic bulk carrier density

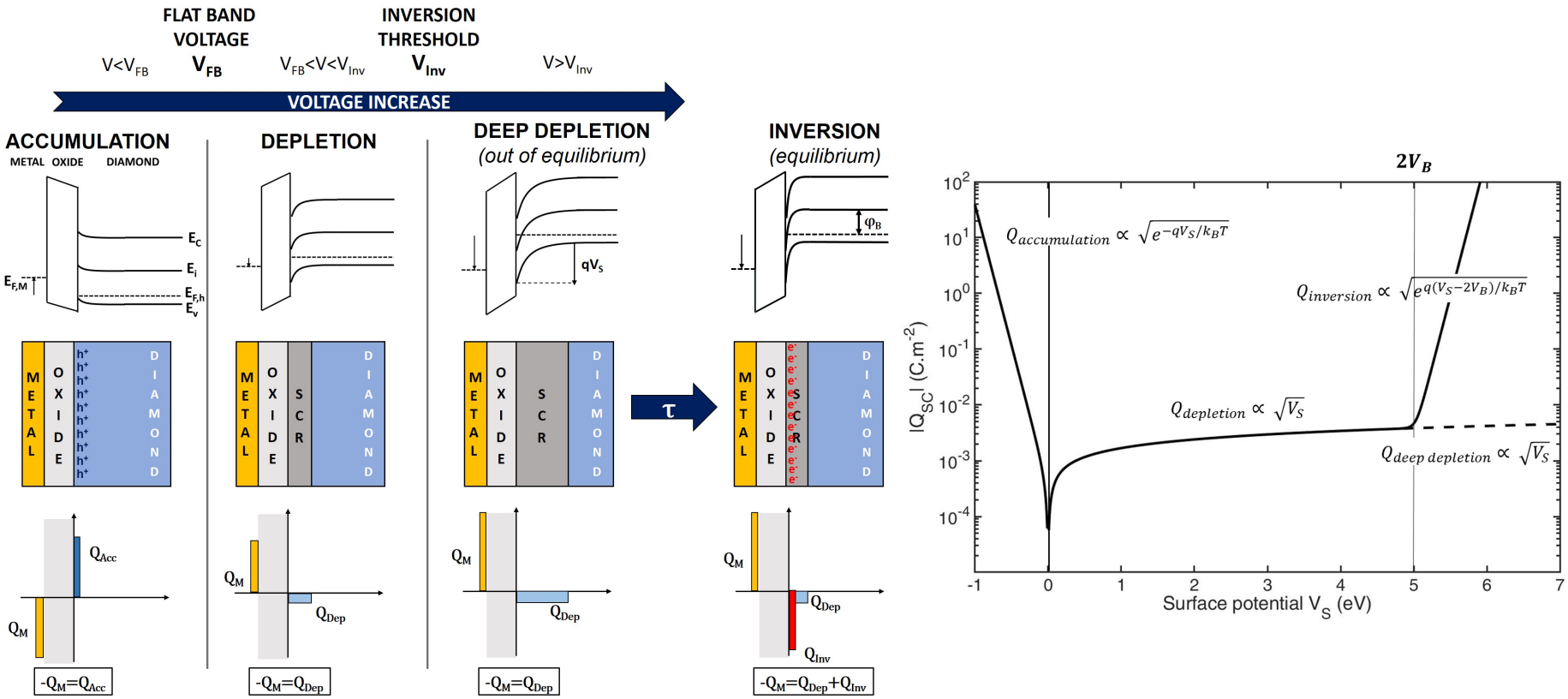


FIGURE 1.7: Working regimes of a p-type MOSCap with their respective schematic band diagram, cross section view and charge equilibrium equation.

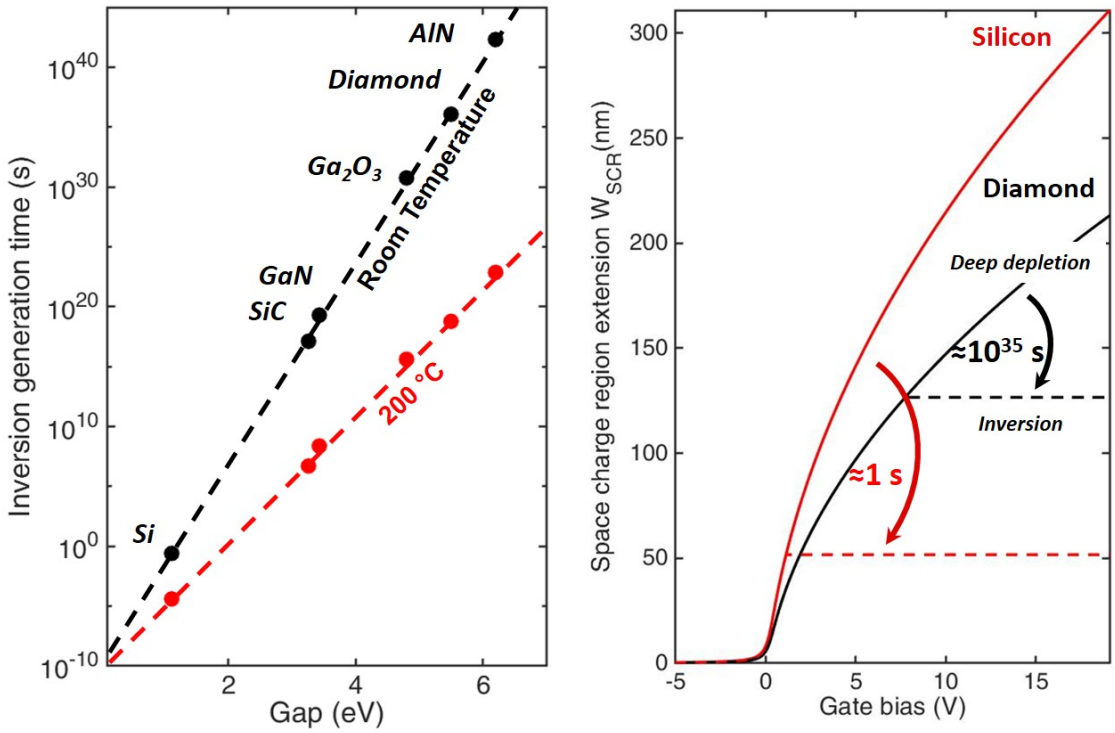


FIGURE 1.8: At left, approximated inversion generation time as function of band gap using equ. 4.11 for Si (1.11 eV), SiC (3.26 eV), GaN (3.43 eV), Ga_2O_3 (4.8 eV), diamond (5.5 eV) and AlN (6.2 eV). The dashed lines are only a guideline to show the exponential trend. At right, comparison between the SCR extension in a silicon and a diamond MOS for a doping level of 2×10^{17} cm^{-3} and an oxide (Al_2O_3) thickness of 50 nm, the typical values used in devices of this work. The threshold voltage V_{Inv} and W_{Inv} values are respectively 1.1 V and 52 nm in the Si MOS, 7.7 V and 126 nm in the diamond MOS.

In this regime, any change of the charge δQ_{SC} will result mostly in a change of the inversion layer charge, due to its exponential dependence, so that $\delta Q_{depletion} << \delta Q_{inversion}$. As a result the SCR thickness W_{SCR}, defined by $W_{SCR} = \frac{Q_{depletion}}{qN_A}$, appears to be pinned for $V_{GS} > V_{Inv}$ at a value W_{Inv}, limiting the channel thickness that can be used for the depletion MOSFET. The inversion regime at equilibrium is reached with a characteristic time constant τ_{Inv}, as minority carriers have to be generated from valence band to conduction band. It is considered here the favourable case of trap assisted thermal generation by a midgap state:

$$\tau_{Inv} = \frac{2}{v_{th}\sigma N_V} e^{\frac{E_C - E_V}{2k_B T}} \tag{1.9}$$

Where v_{th} is the mean thermal velocity of carriers $v_{th} = \sqrt{\frac{3k_B T}{m_h^*}} = 1.2 \times 10^7$ cm/s at room temperature using the diamond effective hole mass $m_h^* = 0.908 m_0$ [60], σ is the capture cross section of the midgap state typically in the order of 10^{-16} cm^2 and N_V is the equivalent density of states, evaluated at $N_V = 2(2\pi m_h^* k_B)^{3/2}/h^3 = 2.18 \times 10^{19}$ eV^{-1}.cm^{-3} at

room temperature.

The approximated values of τ_{Inv} for different semiconductors are plotted in fig 1.8 at room temperature and 200 °C. It appears that for wide band gap material, as opposed to silicon, the inversion charge generation time constant is very large. Even at high temperature, inversion regime cannot be observed without an external source of minority carriers. Instead, the depletion regime is not limited by W_{Inv} even for extreme temperatures during long times. The extension of depletion regime for larger biases than the inversion threshold is called deep depletion and allows for a thicker channel transistor design, and thus less resistive, without disturbance of minority carrier generation during the commutation of the device.

In the case of a MOSCap operated with a frequency measurement higher than the inversion frequency, $f >> 1/\tau_{Inv}$, the equ. 1.4 and equ. 1.5 can be rewritten:

$$Q_{SC} = sign(V_S)\sqrt{2\epsilon_0\epsilon_{SC}p_0(T)}F(T,V_S) \tag{1.10}$$

$$F(T,V_S) = \sqrt{[e^{\frac{-qV_S}{k_BT}} + \frac{qV_S}{k_BT} - 1]} \tag{1.11}$$

The deep depletion MOSFET transistor characteristic

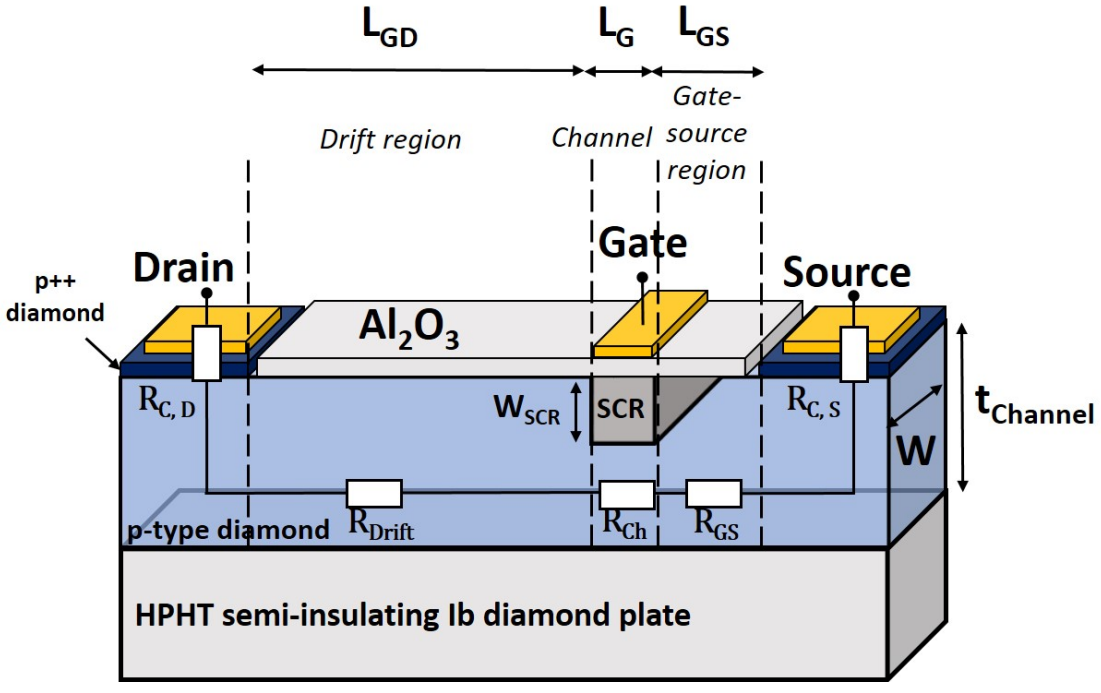


FIGURE 1.9: Schematic cross section of the D3MOSFET with the resistances corresponding to each region of the device. R_{ON} is the total resistance.

The total resistance R_{ON} is the sum of the resistances of the different parts of the device listed in fig. 1.9 : the drift region resistance R_{Drift}, the channel resistance R_{Ch}, the source region resistance R_{GS} and the access and contact resistances of source and drain contacts

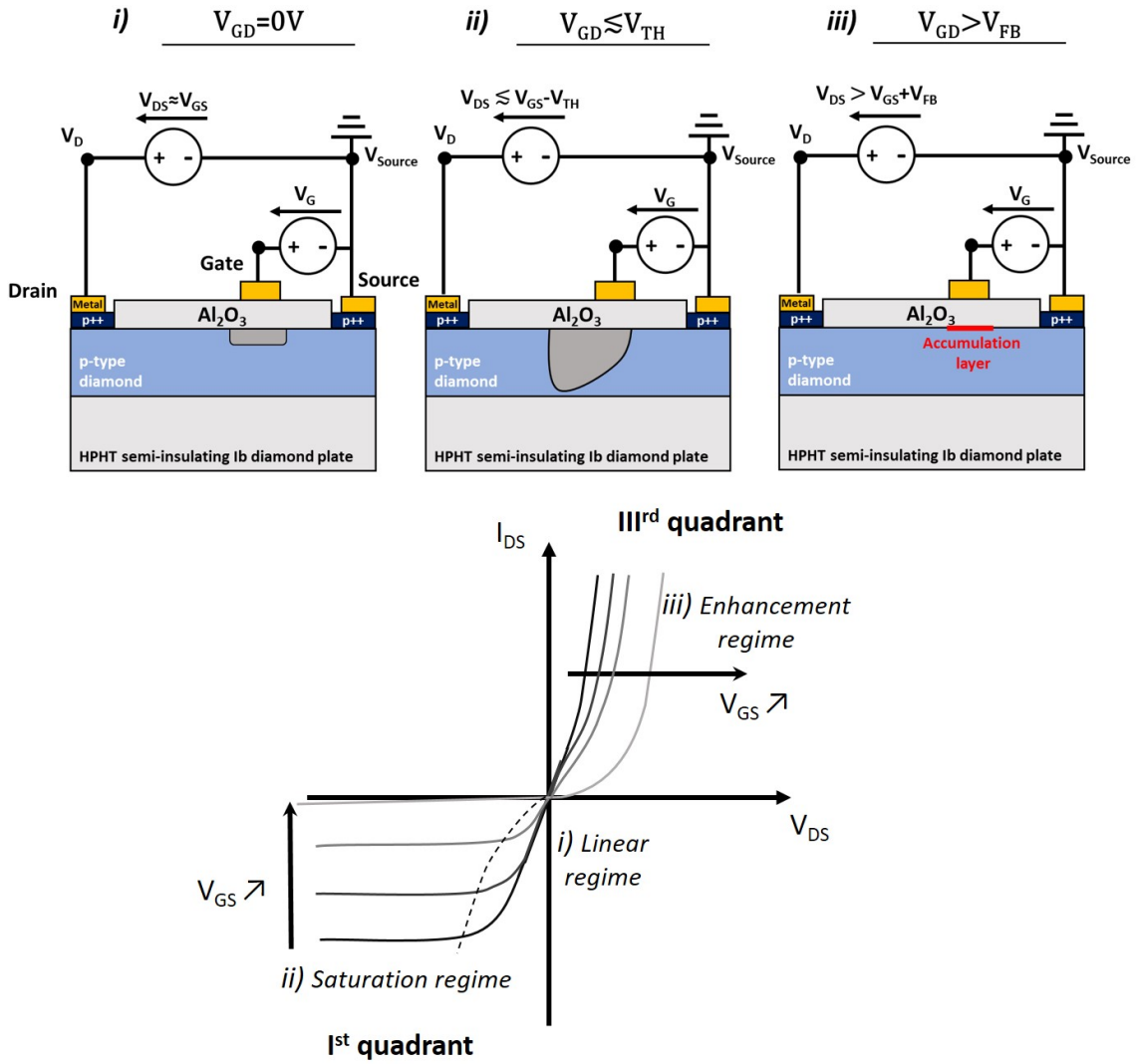


FIGURE 1.10: Schematic cross section of the transistor in on state: (i) The linear regime at low drain bias. (ii) The saturation regime, characteristic of the I^{st} quadrant, where the pinch-off of the channel occurs. (iii) The enhancement regime, characteristic of the III^{rd} quadrant, where the MOS stack is biased in accumulation.

$R_{C,S}$ and $R_{C,D}$. These contact resistances are neglected in the following discussion thanks to the use of selective p++ growth fabrication step detailed later.

$$R_{ON} = R_{Drift} + R_{Ch} + R_{GS} \tag{1.12}$$

A qualitative explanation of the transistor characteristic is shown in fig. 1.10:

(i) In the linear regime, for small variations of V_{DS} around 0 V at a fixed gate-source voltage V_{GS}, the variations of W_{SCR} induced by the drain-gate potential difference V_{GD} are too small to be observed, R_{ON} is approximated to not be bias dependent. The drain-source current characteristic then appears linear.

(ii) In the I^{st} quadrant at larger negative drain bias, there is a stronger asymmetry between V_{GD} and V_{GS}. The MOS gate is polarized more deeply in depletion at the drain side as V_{DS} is negative, causing a gradual increase of the channel resistance R_{Ch}. The transistor characteristic is then non-linear and eventually, if V_{GD} becomes close or more negative than the threshold voltage V_{TH}, the pinch-off effect occurs and the channel is reduced to a small effective thickness, where the electric field is elevated. The free carriers are therefore locally reaching their saturation velocity and the measured drain-source current is no more bias dependent. For power electronics, the transistors are not biased in the saturation regime, which regime occurs only during switching transients.

(iii) In the III^{rd} quadrant for positive drain bias, the effect is reversed, eventually biasing the MOS gate in accumulation. The 2DHG formed below the gate is greatly reducing the channel resistance and a lower R_{ON} has to be measured in this enhancement regime than in the linear regime. If the device was biased in off state, i.e. $V_{GS} > V_{TH}$, V_{GD} becomes lower than to V_{TH} due to the positive V_{DS} ($V_{GD} = V_{GS} - V_{DS}$), reducing the SCR thickness W_{SCR} and the device is switched on at the condition $V_{DS} > V_{GS} - V_{TH}$, thus exhibiting this diode-like behaviour.

The approach developed here gives a qualitative understanding of the D3MOSFET working regimes, the following discussion will then focus on a more quantitative approach on how to design the device accordingly to specific performances.

1.3 Deep depletion MOSFET: from key parameters (doping, thickness, oxide) to performances (R_{ON}, V_{BD}, V_{TH}).

The design is a crucial part prior the device fabrication process. Many parameters, during diamond growth or in the device geometry, have to be tuned in regards of the expected performances of the final component. Trade-off exists between several parameters, as such the understanding of the physics of diamond and the MOSFET, even in a simplified 1D model, is necessary to evaluate the capabilities of diamond devices and later to serve as a basis to compare with experimental results.

1.3.1 Physical models

Temperature, doping and compensation dependence of the electrical resistivity

A bulk conduction is used in the D3MOSFET, as such the resistance of the device is directly dependent on the bulk mobility and carrier concentration dependence with temperature. In most of the semiconductors, a temperature increase over room temperature is degrading the resistance, due to the decreasing mobility as phonon interaction become stronger. However, diamond possesses deep dopants: 380 meV ionization energy for boron acceptors and 570 meV ionization energy for phosphorus donors. Consequently, the resistivity of diamond is limited by the incomplete ionization of dopant, it results in a negative temperature coefficient up to an optimum in the range of 500 K - 700 K depending on the

doping level. The 1D electrical resistivity ρ (in $\Omega.cm$) of a semiconductor is expressed as :

$$\rho(T, N_A, N_D) = \frac{1}{qp(T, N_A, N_D)\mu(T, N_A, N_D)} \tag{1.13}$$

Where $\mu(T, N_A, N_D)$ is the hole mobility of carriers and $p(T, N_A, N_D)$ is the free hole density which are estimated as function of doping level and temperature using the empirical model developed in ref. [61].

(i) Boron ionization energy as function of doping level

Before considering temperature dependence, it is useful to describe the variation of the acceptor ionization energy as function of the doping level, as it will influence the hole concentration. This dependence is fitted by the Pearson and Bardeen model [62] with adjusted parameters to obtain the reported 0.38 eV boron ionization energy [63], shown in fig. 1.11.

$$E_A = E_{A,0} - \alpha \times N_A^{\frac{1}{3}} \tag{1.14}$$

Where $E_{A,0} = 0.38$ eV is the ionization energy at low doping level, $\alpha = 5.5 \times 10^{-8}$ eV.cm is a fitting parameter adjusted to obtain the metal-insulator transition at 3×10^{20} cm^{-3} [64] and N_A is the doping level in cm^{-3}.

As shown in fig. 1.11, for doping levels below 10^{19} cm^{-3} the experimental values of ionization energy of boron are stable at an approximate value of 380 meV, which corresponds to the energy difference of the boron acceptor level and the maximum of the valence band. For higher doping level values, 10^{19} cm^{-3} $< N_A < 3 \times 10^{20}$ cm^{-3}, E_A is decreasing due to the overlapping of the acceptor wave function. Moreover, the distance between dopant is small enough to allow carriers to hop from one site to another, with various hopping mechanisms depending on temperature, doping and compensation, decreasing the resistivity as function of dopant concentration. For a doping level above the metal-insulator transition, $N_A > 3 \times 10^{20}$ cm^{-3}, E_A is lowered down to zero as the boron impurity band conduction merges with the valence band, analogous to the conduction in a metal. In this metallic conduction regime, the resistivity is orders of magnitude lower than below the transition and almost no temperature dependence is observed. This is well suited to perform low resistivity ohmic contacts at the drain and source of diamond FET devices.

(ii) Free hole density as function of temperature, doping level and compensation

Besides the metallic conduction used to form ohmic contacts, the typical range of doping levels used in the active regions of power FETs is well below 10^{18} cm^{-3} since high doping levels lead to lower breakdown voltages as explained later. Therefore, only the case of a non degenerate semiconductor is considered, with a constant ionization energy equal to the low impurity concentration value, $E_A = E_{A,0} = 380$ meV, and no hopping conduction mechanisms. Then, the free hole concentration can be expressed as function of temperature T, doping level N_A and compensation N_D by [61]:

$$p(T) = 0.5(\phi_A + N_D)\left(\left[1 + \frac{4\phi_A(N_A - N_D)}{(\phi_A + N_D)^2}\right]^{0.5} - 1\right) \tag{1.15}$$

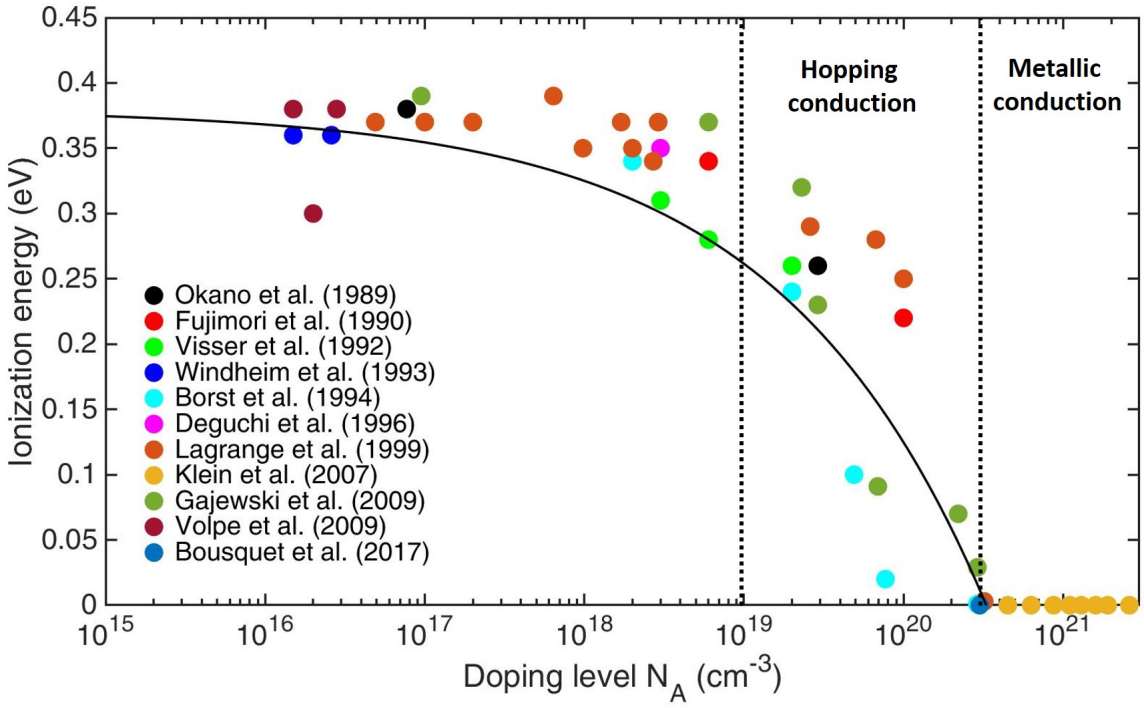


FIGURE 1.11: Ionization energy of boron in diamond as function of doping level. Experimental points are taken from [65, 66, 67, 68, 69, 70, 71, 72, 73, 61, 64] and the full line is a fit using the Pearson and Bardeen model [62] adjusted to obtain the metal-insulator transition at 3×10^{20} cm^{-3} and a ionization energy of 380 meV at low impurity concentration.

Where

$$\phi_A = 0.25 N_V(T) T^{1.5} e^{\frac{E_A}{k_B T}} \tag{1.16}$$

From this equation, the dramatic effect of compensation can be evaluated as shown in fig. 1.12 for a doping level of 2×10^{17} cm^{-3}. Hole concentrations with compensation ratios ranging between 0% and 10% are calculated, which corresponds to common reported values for various doping levels [74] and are close to the value measured in sample fabricated in this work. As few acceptors are ionized around room temperature, part of the carriers are trapped by donor atoms and the free hole density is drastically decreased. For example, the hole concentration at room temperature with no compensation is calculated to be $p(300K)_{0\%} = 1.15 \times 10^{15}$ cm^{-3}, corresponding to an ionization ratio of 0.58%. With a 6% compensation ratio, this value drops by an order of magnitude to $p(300K)_{6\%} = 1 \times 10^{14}$ cm^{-3}, corresponding to an ionization ratio of 0.05%. With increasing temperatures, the carrier concentration becomes large with respect to the donor density because of the thermal ionization of dopant, and the compensation effect tends to be reduced. Using the previous examples at 600K, one can estimate that $p(600K)_{0\%} = 5 \times 10^{16}$ cm^{-3} (25% ionization ratio) and $p(600K)_{6\%} = 4.4 \times 10^{16}$ cm^{-3} (22% ionization ratio).

The negative temperature coefficient in diamond is then greatly dependent on the compensation ratio, even for small donor concentration values, but this dependence is greatly reduced at higher temperature.

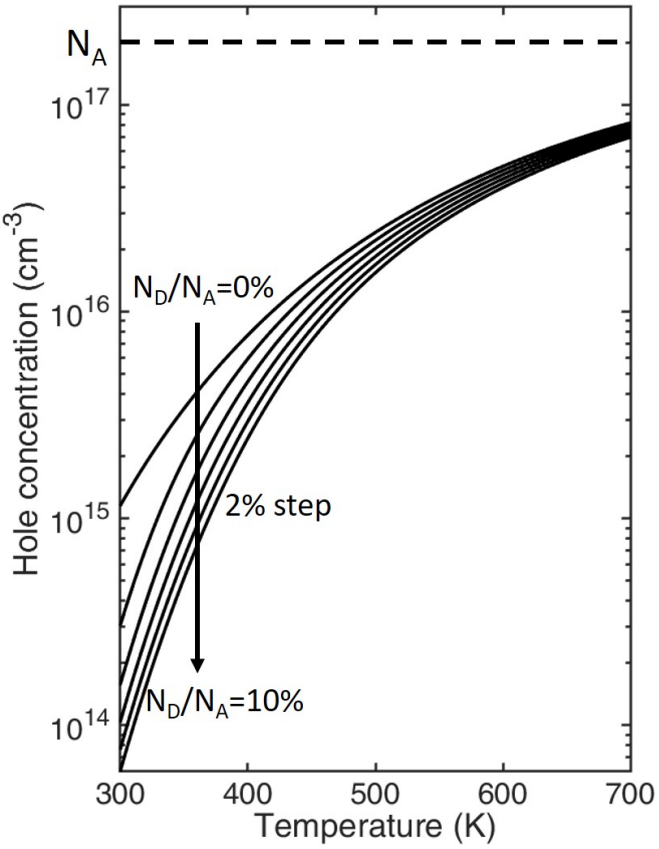


FIGURE 1.12: Calculated free hole concentration of p-type diamond as function of temperature for different compensation ratios on a layer doped at 2×10^{17} cm^{-3}.

(iii) Hole mobility versus doping level and temperature

Hole mobility is a temperature and doping level dependent parameter which greatly influences the resistivity of the material. In a bulk conduction device where surface effects are negligible, only phonon and impurities scattering are considered, as explained in more details in ref [75]. The empirical model developed in ref. [61] provides a reliable approach to evaluate the mobility in order to calculate the on state resistance of the final device. The dependence of μ as function of N_A and temperature are plotted in fig. 1.13, using the following fitting equation:

$$\mu(T) = \mu(300K) \left(\frac{T}{300K} \right)^{-\beta} \tag{1.17}$$

where

$$\beta = \beta^{min} + \frac{\beta^{max} - \beta^{min}}{1 + \left(\frac{N_{imp}}{N_\beta} \right)^{\gamma_\beta}} \tag{1.18}$$

Where N_{imp} is the total number of impurities $N_{imp} = N_A + N_D$

$$\mu(300K) = \mu^{min} + \frac{\mu^{max} - \mu^{min}}{1 + \left(\frac{N_{imp}}{N_\mu}\right)^{\gamma_\mu}} \tag{1.19}$$

β^{max}	β^{min}	N_β (cm^{-3})	γ_β	μ^{max} (cm^2/(V.s))	μ^{min} (cm^2/(V.s))	N_μ (cm^{-3})	γ_μ
3.11	0	4.1×10^{18}	0.617	2016	0	3.25×10^{17}	0.73

TABLE 1.2: List of parameters used in the hole mobility model described in ref. [61].

As shown in fig. 1.13, the mobility has weak variation versus doping level for $N_A < 10^{17}$ cm^{-3} due to the dominance of scattering by phonons. The mobility at 300K in a boron doped diamond at 10^{15} cm^{-3} is 1987 cm^2/(V.s) compared to 1417 cm^2/(V.s) at 10^{17} cm^{-3}. Above this value, a steeper decrease of the mobility is observed due to the impurities scattering mechanisms being dominant, dropping to 153 cm^2/(V.s) at 10^{19} cm^{-3}. With increasing temperature above room temperature, all scattering mechanisms (phonons and impurities) have a negative temperature coefficient. This cause the mobility of a layer doped at 10^{17} cm^{-3} to decrease from 1417 cm^2/(V.s) at room temperature to 392 cm^2/(V.s) at 200 °C.

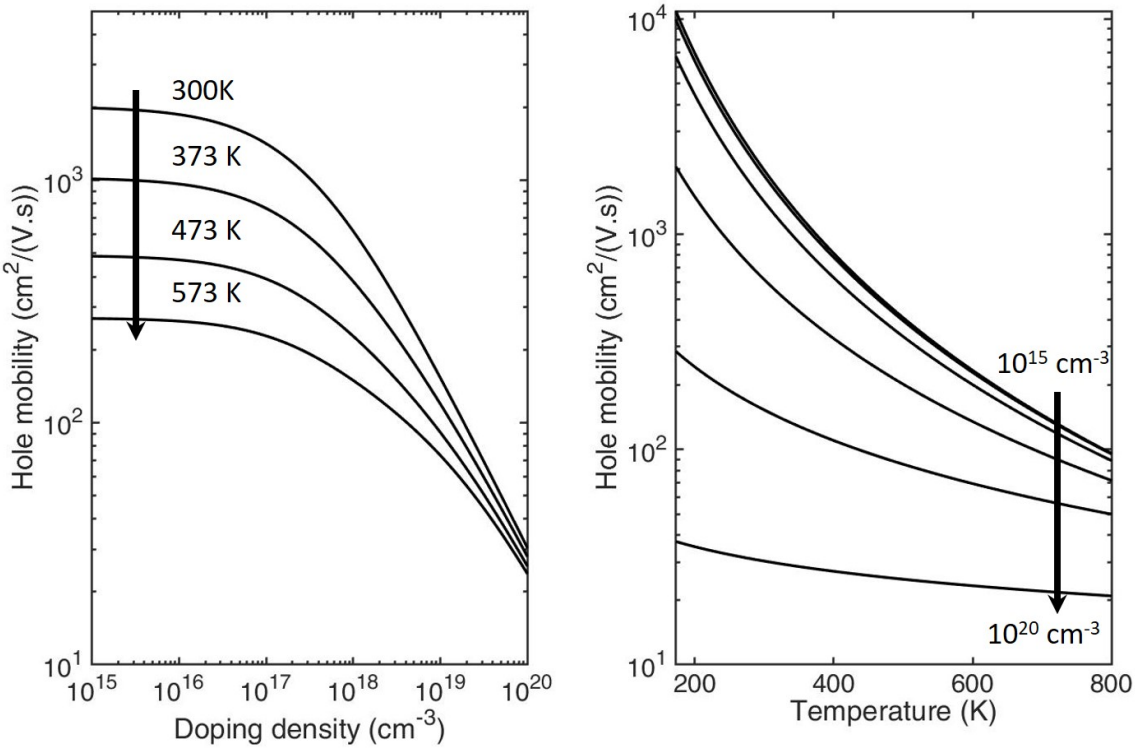


FIGURE 1.13: At left, calculated hole mobility as function of the doping density for different temperatures. At right, calculated hole mobility as function of the temperature for different doping densities between 10^{15} cm^{-3} and 10^{20} cm^{-3} with one decade step.

(iv) Resistivity as function of temperature, doping level and compensation

Using the models to calculate μ and p, the resistivity can be estimated as function of temperature, doping level and compensation with equ. 1.13, shown in fig. 1.14. Around room temperature and below, the ionization of dopants dominates the resistivity variation versus temperature, causing the negative temperature coefficient. Eventually when increasing temperature, the higher ionization ratio is hindered by the decrease of the mobility due to optical phonon scattering, inducing an increase of resistivity with temperature. The minimum of the resistivity is doping level dependent, around 450 K for 10^{15} cm^{-3}, but this value is strongly increasing as function of the doping level, to non practical temperatures for a device (550 K at 10^{16} cm^{-3} and 660 K at 10^{17} cm^{-3}). Then, except for very low doping level values, the negative temperature coefficient is expected in the full working temperature range of the diamond devices based on bulk conduction.

Electric field distribution

The scaling of the device parameters has a double objective: reducing as much as possible the total resistance of the device in on state R_{ON} and increasing its off state blocking voltage capability V_{BD}. However, even considering an optimized, ideal structure there is a trade off between these parameters, mainly determined by the doping level of the p-type diamond layer. To understand the effect of this parameter, it is necessary to predict the electric field distribution in the device. To do so, it is approximated by a 1D model considering an homogeneous doping level.

The 1D Gauss law can be expressed as:

$$\frac{\partial E(x)}{\partial x} = \frac{\rho}{\epsilon_{Diamond}\epsilon_0} \tag{1.20}$$

With $\rho = Q_{SCR}/W_{SCR}$ the charge density in the SCR in the depletion regime, which is constant assuming an homogeneous doping level. Integration of this equation gives a linear dependence of the field as function of the position in the SCR:

$$E(x) = \frac{qN_A}{\epsilon_{Diamond}\epsilon_0}(W_{SCR} - x) \tag{1.21}$$

Then, in the depletion layer, the electric field is linearly decreasing from the value $E_{Max} = \frac{qN_A}{\epsilon_{Diamond}\epsilon_0}W_{SCR}$ at the diamond/oxide interface, with a slope $\frac{qN_A}{\epsilon_{Diamond}\epsilon_0}$. When biased in off state at $V_{DS} = 0$, the potential V_{GS} is creating a SCR located below the gate with a lateral extension assumed to be negligible. For negative V_{DS} values, the difference between V_{GD} and V_{GS} is asymmetrically biasing the MOS in depletion at the drain side creating a lateral extension of the electric field. The fig. 1.15 represents an approximation of the electric field profile at the diamond/oxide interface for low and high V_{DS}, by assuming that the electric field under the gate contact is constant over its length (which can be considered a good approximation if $L_G >> W_{SCR}$). It can be seen that the maximum electric field is located below the gate at the drain side. When this value is reaching the critical field of

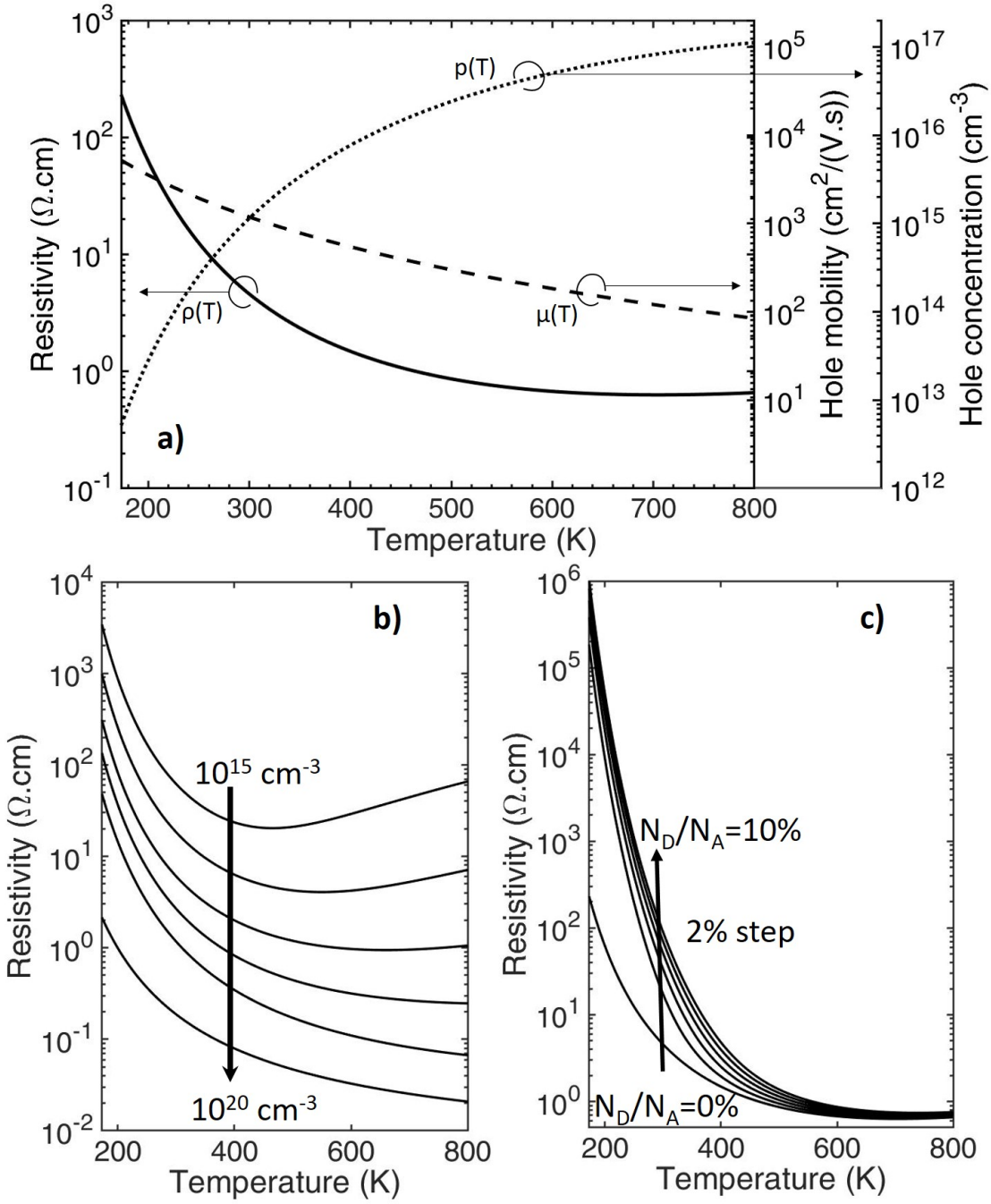


FIGURE 1.14: a) Resistivity, hole concentration and hole mobility as function of temperature for a doping level of 2×10^{17} cm^{-3} and no compensation. b) Resistivity as function of temperature for doping levels ranging between 10^{15} cm^{-3} and 10^{20} cm^{-3} with a decade step, compensation is set to 0. c) Resistivity as function of temperature for a doping level of 2×10^{17} cm^{-3} and a varying compensation ratio between 0% and 10%.

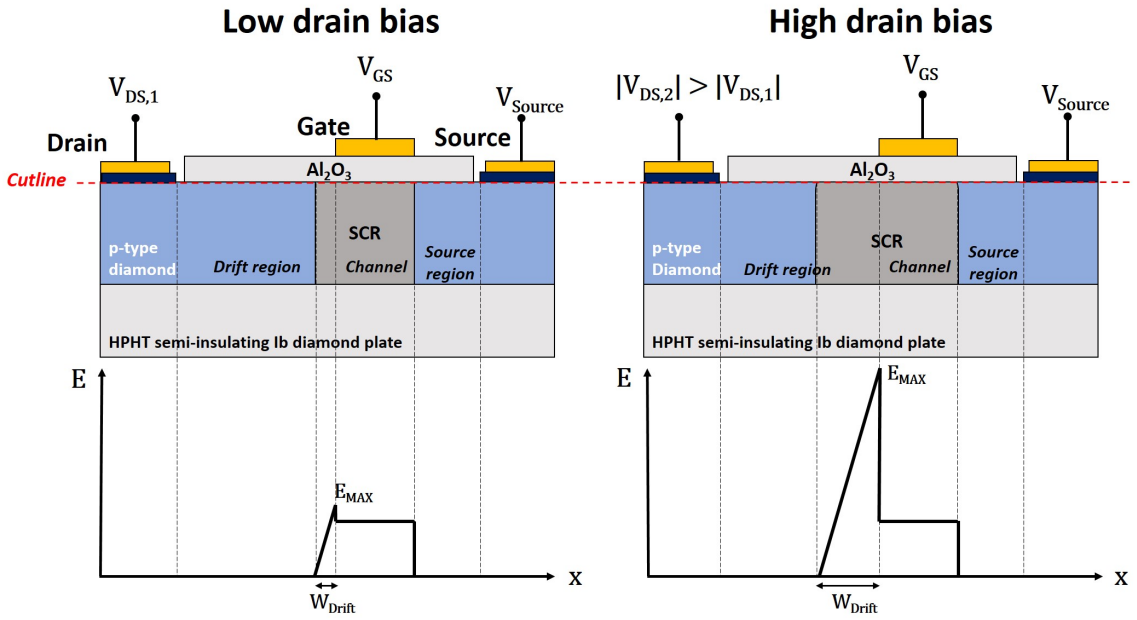


FIGURE 1.15: 1D representation of the electric field distribution along the cutline of the D3MOSFET at low and high drain-source bias in off state

diamond E_C, at the drain breakdown voltage V_{BD}, impact ionization effect will eventually lead to avalanche breakdown. Causing the device to conducts even in off state. The value of W_{Drift} when reaching the diamond critical field is considered the ideal drift length L_{GD}.

This simple model is very convenient for basic device design but has some limits: it is well known that edge effects can cause the presence of a peak electric field below the gate, especially in a lateral design as pointed out by [76] on Schottky diodes. However, there is no analytical solutions for it, in addition to be very dependent on the presence of an uncontrolled surface potential on diamond. Taking into account these parasitic effects would require extensive use of finite element simulation tools, which are not optimized for diamond.

Avalanche breakdown

In the general case, the ideal upper limit V_{BD} of the voltage that a FET can sustain in off state is determined by avalanche multiplication effect (or also referred as impact ionization effect). Under high field condition, incident carriers will drift across the SCR. They will eventually gain enough kinetic energy to ionize the lattice atoms, generating one or more electron-hole pairs, that will in turns also be accelerated to generate more pairs. This chain reaction multiplies any small current I_0 by a multiplication factor M, which can be very large and cause the breakdown of the device. In the following description, only the lateral extension of the SCR is considered since in the model considered here, the electric field below the gate is constant and only the lateral extension is drain bias dependent. When a ionization event occurs at the position x, a pair of electron-hole is created that will drift in opposite direction due to the electric field. The multiplication factor as function of the

position in the depletion region of a p-type semiconductor is then given by the sum of two integrals, for holes and for electrons:

$$M(x) = 1 + \int_0^x \alpha_n M(x)dx + \int_x^{W_{Drift}} \alpha_p M(x)dx \tag{1.22}$$

Where $x = 0$ at the gate edge at the drain side, α_n and α_p are the impact ionization rates of electrons and holes respectively. They are defined as the number of electron-hole pairs generated by a carrier per unit distance, in cm^{-1}. Equ. 1.22 has a solution written:

$$M(x) = \frac{\exp^{\int_0^x (\alpha_n - \alpha_p)dx}}{1 - \int_0^{W_{Drift}} \alpha_p \exp^{\int_0^{x'} (\alpha_n - \alpha_p)dx'} dx} \tag{1.23}$$

It is generally considered that avalanche breakdown occurs when the multiplication factor tends to infinity, i.e. when the denominator of equ. 1.23 is equal to zero:

$$\int_0^{W_{Drift}} \alpha_p \exp\left\{ \int_0^{x'} (\alpha_n - \alpha_p)dx' \right\} dx = 1 \tag{1.24}$$

As discussed in [77, 78] by Hiraiwa et al., equ. 1.24, called ionization integral, can be well approximated by considering a geometric average of impact ionization rate of electrons and holes: $\alpha = \sqrt{\alpha_n \alpha_p}$, such as equ. 1.24 becomes:

$$\int_0^{W_{Drift}} \alpha dx = 1 \tag{1.25}$$

Predicting the breakdown voltage of an ideal, optimized device is reduced to knowing these 2 parameters α_n and α_p. Up to now, there is no accurate extraction of diamond ionization rate coefficients in literature due to the difficulty to reliably measure the critical field of diamond, as it requires to minimize edge effects and leakage current in fabricated test structures. In this work, the ionization rates fitted to experimental data at room temperature in [78] are used:

$$\alpha = \sqrt{\alpha_n \alpha_p} = \frac{9.44 \times 10^4}{10^{0.5}} \exp\left\{ \frac{-10^{0.5} \times 1.90 \times 10^7}{|E|} \right\} \tag{1.26}$$

One can note that α is temperature dependent, but its dependence is not established in the literature up to now. Moreover, since the ionization integral in equ. 1.24 depends on W_{Drift}, the critical field of a semiconductor is strongly doping dependent, as shown in the fig. 1.16 from [77]. The critical field is evaluated at 3.8 MV/cm for $N_A = 10^{15}$ cm^{-3} and 9.5 MV/cm for $N_A = 10^{17}$ cm^{-3}, the approximation of a non doping dependent critical electric in diamond that is occasionally used is then rather inaccurate.

By knowing the critical field of diamond for any doping level values, the optimum drift length L_{GD} can be estimated, i.e. the lateral extension W_{Drift}^{BV} at breakdown:

$$W_{Drift}^{BV} = \frac{E_C \epsilon_{Diamond} \epsilon_0}{q N_A} \tag{1.27}$$

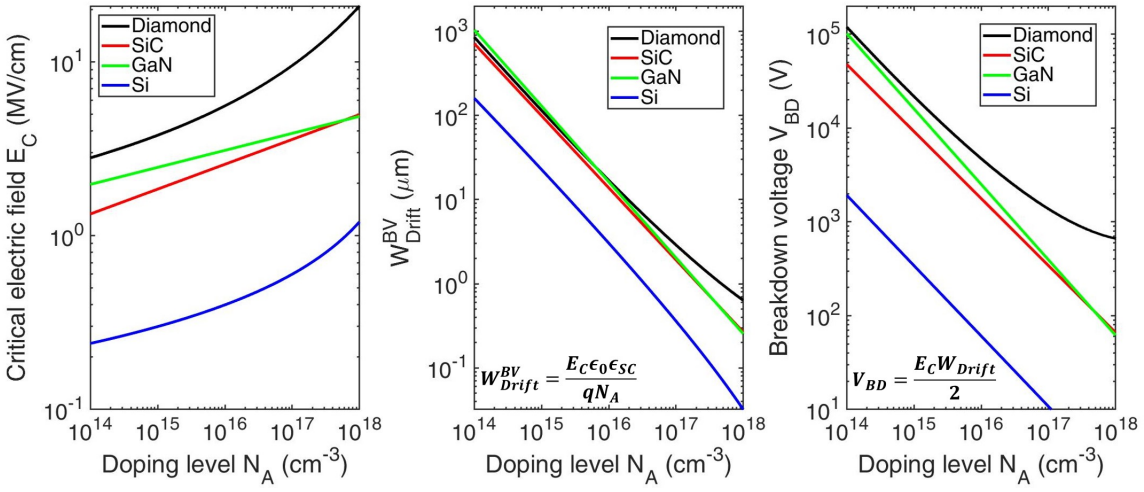


FIGURE 1.16: Estimated room temperature critical field, breakdown voltage and lateral expansion of the SCR at breakdown as function of the doping level for diamond using ref. [77], SiC using ref. [79], GaN using ref. [80] and Si using ref. [59].

This dependence is plotted in fig. 1.16. The breakdown potential is related to the critical field by:

$$V_{BD} = \frac{E_C \times W_{Drift}^{BV}}{2} \tag{1.28}$$

Even if the critical field is increasing with doping level, it has a weaker dependence than compared to W_{Drift} as illustrated in fig. 1.16. Overall, the variation of V_{BD} versus N_A is mostly governed by W_{Drift}, i.e. a high blocking voltage device requires a large L_{GD} and a low doped drift layer, increasing the on state resistance. In this regards, the high breakdown field of wide band gap semiconductors is a decisive advantage over silicon, achieving much higher breakdown voltages at equivalent doping density. The difference is less marked between diamond and SiC and GaN but is not negligible. For example for a doping level of 10^{17} cm^{-3}, the critical field of diamond is evaluated at 9.5 MV/cm compared to 3.6 MV/cm in SiC, 3.9 MV/cm in GaN and 0.6 MV/cm in Si. This leads to a breakdown voltage of 1.4 kV in diamond, 340 V in SiC, 390 V in GaN and 11V in Si. However, for low doping level values $N_A < 10^{16}$ cm^{-3}, this calculation gives a limited advantage to diamond over GaN for the V_{BD} versus W_{Drift} trade-off. This is explained by their close critical field values at low doping and the comparatively lower relative dielectric constant of diamond (5.5 for diamond and 8.9 for GaN).

Other wide band gap semiconductors are under study for power applications, such as AlN and Ga_2O_3, but their critical field versus doping dependencies are not established. A commonly reported value for Ga_2O_3 is 7-8 MV/cm [81], whereas AlN is attributed various values of several MV/cm to >10 MV/cm, but experimental evidences are lacking to conclude on the impact ionization rates. It is however expected that their breakdown field is high and comparable to diamond since their band gap values are close (diamond is 5.5 eV, AlN 6.2 eV and Ga_2O_3 is 4.8 eV).

1.3.2 R_{ON} vs V_{BD} trade-off

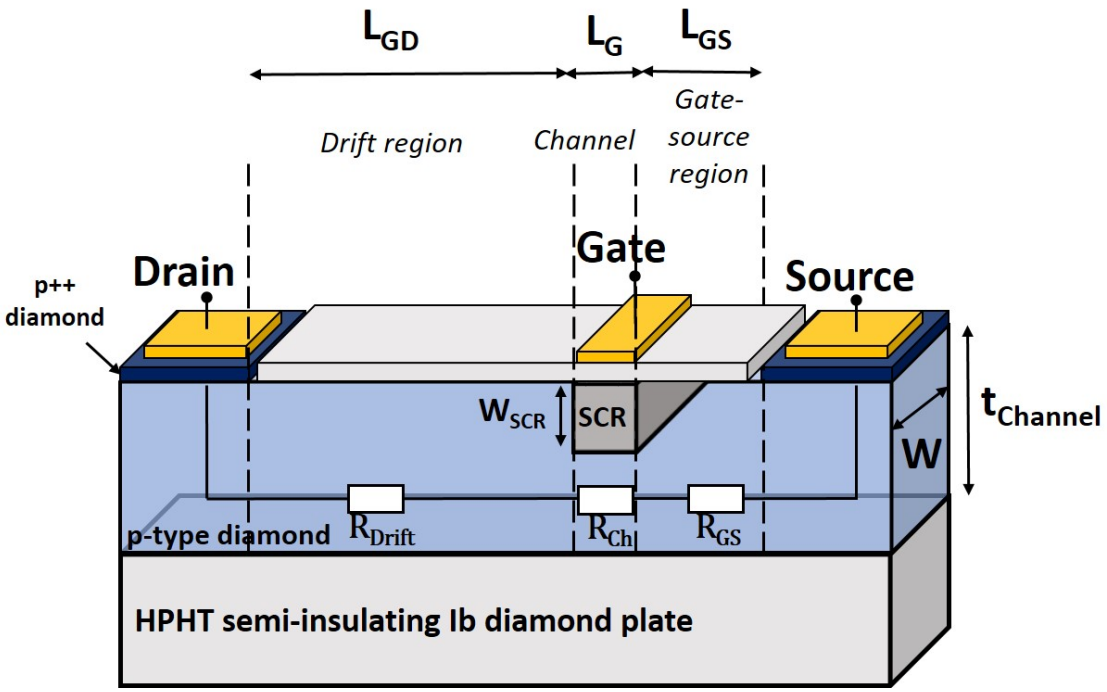


FIGURE 1.17: Schematic cross section of the D3MOSFET

When considering the case of a non depleted channel ($W_{SCR} = 0$), with no contact resistances ($R_{C,D}$ and $R_{C,S} = 0$) as shown in fig. 1.17, R_{ON} can be expressed by:

$$R_{ON} = \rho \times \frac{L_{Drift} + L_{Ch} + L_{GS}}{W \times t_{Channel}} \tag{1.29}$$

Where ρ is the resistivity of boron doped diamond given by equ. 1.13. It is useful to define and use a normalized resistance, the specific on-resistance $R_{ON,S}$, defined by: $R_{ON,S} = R_{ON} \times W \times (L_{Drift} + L_{Ch} + L_{GS})$, often given in m$\Omega$.cm^2. As $R_{ON,S}$ is normalized by the active surface area of the device, it can be used as a comparison between devices with varying designs and sizes.

$$R_{ON,S} = \rho \times \frac{(L_{Drift} + L_{Ch} + L_{GS})^2}{t_{Channel}} \tag{1.30}$$

A trade-off exists between the on state resistance R_{ON} and the maximum blocking voltage in off state V_{BD} of a device. Minimization of R_{ON} requires to maximize the doping level to decrease the resistivity and W^{BV}_{Drift}, as opposed to the maximization of V_{BD} which require to minimize the doping level as stated in fig. 1.16. For the sake of simplicity, the resistance of the drift layer in on state is supposed to be much greater than the channel and gate-source region resistances: $R_{ON} \approx R_{Drift}$, then this trade-off for different temperature is calculated and plotted in fig. 1.18.

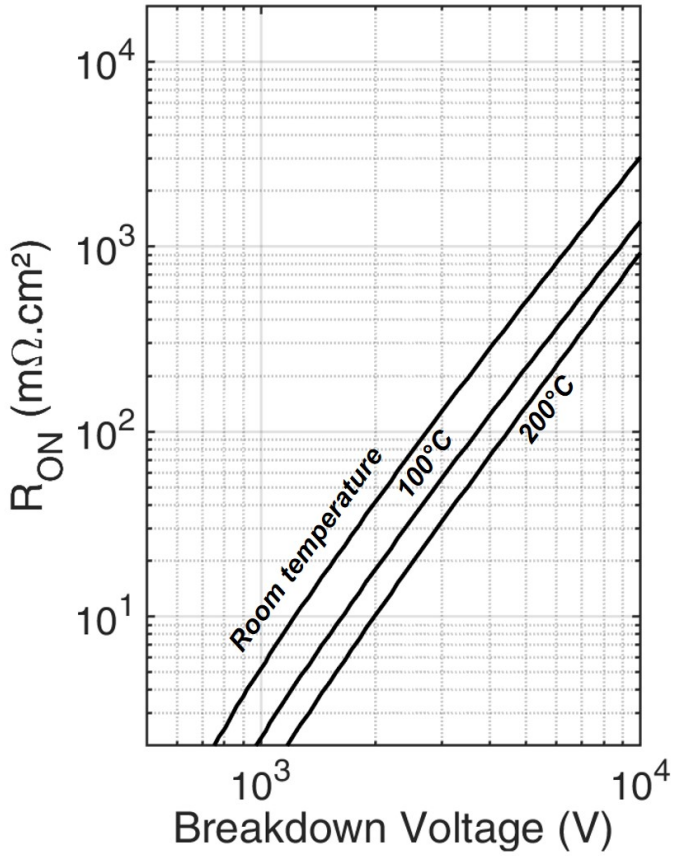


FIGURE 1.18: Calculated R_{ON} vs V_{BD} trade-off for the lateral D3MOSFET at room temperature, 100 °C and 200 °C. An ideal structure is considered (no parasitic effects, no compensation) and the p-type layer thickness is calculated to obtain a threshold voltage of 15 V with an oxide thickness of 50 nm. The $R_{ON} \approx R_{Drift}$ approximation is used.

1.3.3 R_{ON} vs V_{TH} trade-off

Thanks to the deep depletion concept in wide band gap semiconductors, it is possible to use thick epilayers as channel to reduce the resistance. This is however at the cost of an increasing threshold voltage V_{TH} to reach the off state as the SCR extension W_{SCR} is square root dependent on the applied bias:

$$W_{SCR} = \sqrt{\frac{2\epsilon_{Diamond}(V_G - V_{FB} - V_{OX})}{qN_A}} \tag{1.31}$$

Where V_{OX} the potential drop across the oxide layer, V_G the applied bias on the gate metal, V_{FB} the flat-band potential (-2.6 V in case of a titanium metal contact).

The threshold can be designed by the epilayer thickness from a normally-off, resistive, device to a more conducting one at high V_{TH} values, which requires in turn more charge to be switched off as represented in fig. 1.19.

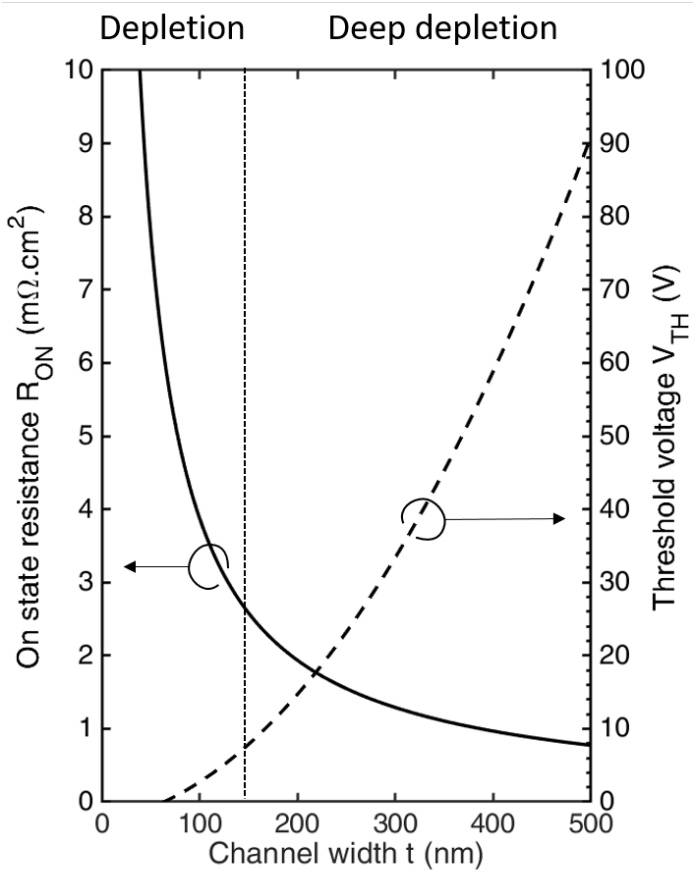


FIGURE 1.19: R_{ON} (full line) and V_{TH} (dashed line) trade-off as function of the channel thickness for a lateral device at 200 °C and a doping level $N_A = 2 \times 10^{17}$cm^{-3}. Oxide thickness is set at 50 nm and the flatband voltage at -2.6 V.

1.3.4 V_{TH} vs oxide thickness t_{OX}

The gate oxide thickness t_{OX} is an other important parameter which influences performances. As implied in equ. 1.31, the thickness of the SCR is dependent on the potential drop across the oxide, given by: $V_{OX} = Q_M/C_{OX}$ with $C_{OX} = \epsilon_0\epsilon_{OX}/t_{OX}$ the capacitance of the oxide layer and Q_M the charge applied on the gate metal. V_{OX} being linearly dependent on the oxide thickness, an increase of t_{OX} necessitates to apply a higher gate bias to reach the same surface potential. The threshold voltage V_{TH} versus t_{OX} dependence is shown in fig. 1.20 for Al_2O_3, SiO_2 and h-BN with relative dielectric constants of respectively $\epsilon_{Al_2O_3}$ =8.8 (measured on fabricated samples), ϵ_{SiO_2} =3.9 and ϵ_{h-BN} =3 [82]. In the fabricated samples Al_2O_3 has been chosen, as in most of other diamond MOSFETs, because of the simplicity and availability of Atomic Layer Deposition (ALD). This oxide is the most studied one in diamond MOS architectures and a fabrication process shown in chapter 2 has been optimized with it. Moreover its high dielectric constant is beneficial to reduce the threshold voltage as shown in fig. 1.20. SiO_2 has also been used occasionally, as well as h-BN which has recently shown promising results as a gate dielectric [40],

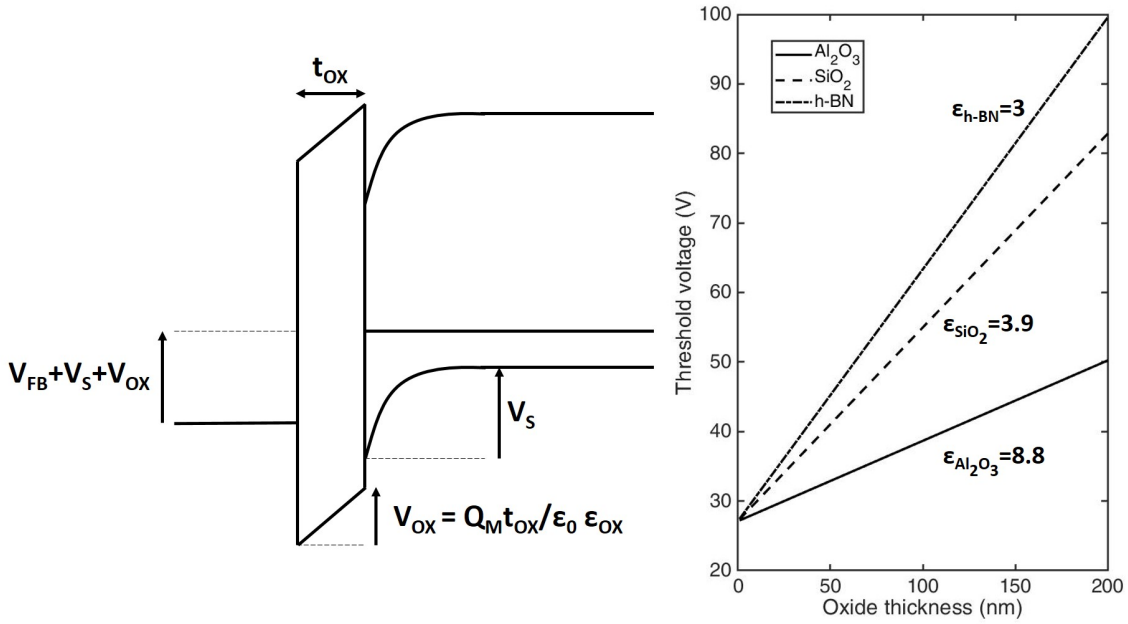


FIGURE 1.20: Calculated threshold voltage V_{TH} as function of the oxide thickness t_{OX} for a doping level $N_A = 2 \times 10^{17}\text{cm}^{-3}$ and a channel thickness of 300 nm. The relative dielectric constant of the oxide ϵ_{OX} is set at 9.4 for Al_2O_3 (determined experimentally in chapter 4), 3.9 for SiO_2 and 3 for h-BN [82]. The flatband voltage is set at -2.6 V.

with a breakdown field of 6.6 MV/cm and to obtain a relatively higher mobility diamond HMOSFET. The deposition method used so far, the Scotch tape exfoliation technique, is however rather complex to reproduce. The choice of the oxide is however an important and more complex topic, as in addition to their physical parameters many effects are related to the deposition method and the fabrication process in general. As such bulk traps, the chemistry at the diamond/oxide interface and the stability with temperature changes and an electrical stress are important factors for the device operation. Most of the literature on diamond MOS structures is focused on Al_2O_3 and steady improvements have been accomplished over the years with this material, allowing for the fabrication of MOSFETs. But it is still unclear if Al_2O_3 is the best gate oxide and achieving a sufficient control of the charge trapping effects still requires many efforts.

While in the ideal case considered here, the field in the oxide is independent on its thickness: $E_{OX} = Q_M/\epsilon_0\epsilon_{OX}$, large differences in oxide breakdown values are observed as function of t_{OX}. This can be due to edge effects but also to charging effects at the diamond/oxide interface as well as in the bulk of the oxide. The presence of traps can cause the electric field distribution in the oxide to not be uniform, which is exacerbated for thin layers and cause premature breakdown as well as increased leakage current. As a consequence H terminated diamond MOSFET with thick oxide layers are reported to exhibit higher breakdown values [54, 52], a study of oxide thickness effect as yet to be realized on O-terminated MOS.

1.4 Perspectives and partial conclusions

1.4.1 Edge terminations

In part due to the very high critical field of diamond, the reported MOS devices are always showing a breakdown of the oxide layer prior to the apparition of avalanche effect in diamond. Indeed, the Al_2O_3 has a breakdown field measured to be around 6 MV/cm, which is in many cases lower than diamond. To observe avalanche breakdown in a diamond MOS structure, reduction of electric field crowding effects is expected to be even more important than with other materials. The use of edge termination structures is a well known way to improve the breakdown voltage of devices by reducing the electric field crowding effect. In diamond Schottky diodes, floating metal rings have been investigated [83] as well as field plates architectures [84]. Although their benefits are evidenced, the demonstrated breakdown electric field are still low in comparison to diamond capabilities. Breakdown limitations are mostly due to fabrication process and epitaxial layers imperfections.

1.4.2 Recess gate

The on state resistance of the proposed D3MOSFET is dominated by the drift region resistance R_{Drift} especially at low doping density (high blocking voltage) where the drift region is much longer than the gate length and gate-source distances. It can be optimized by the use of a recess gate architecture represented in fig. 1.21, which consists in the use of a thicker p-type layer with a thinned channel by etching. The structure has been described in the patent[85]. The thickness of the channel and the choice of the gate metal is designed so the 0 V gate bias SCR extension is enough to deplete the layer completely, achieving the normally-off operation. The MOS stack is then biased in accumulation in on state to reduce the resistive channel region. One of the advantages of this structure over the standard lateral design is to obtain the normally-off characteristic, avoiding the necessary use of additional external devices needed in case of a normally-on transistor, for safety purpose. Moreover, the channel resistance R_{Ch} is greatly reduced by the hole accumulation layer and R_{Drift} and R_{GS} can be lowered by the use of a thicker p-layer as it is no more limited by the R_{ON} vs V_{TH} trade-off.

It is however, at the moment, challenging to obtain an accumulation layer in diamond MOS structures, to take the full advantage of this architecture. Reports based on capacitance measurements of O-terminated diamond MOS capacitors [86, 87, 88, 89] that claimed to obtain it had most probably misinterpreted the measurements as discussed in chapter 4. Accumulation layer has nonetheless been demonstrated in a diamond lateral FinFET [90] using ALD SiO_2 as gate oxide, but the authors could not extract the hole mobility of the channel as the accumulation layer may not be formed on the full channel surface.

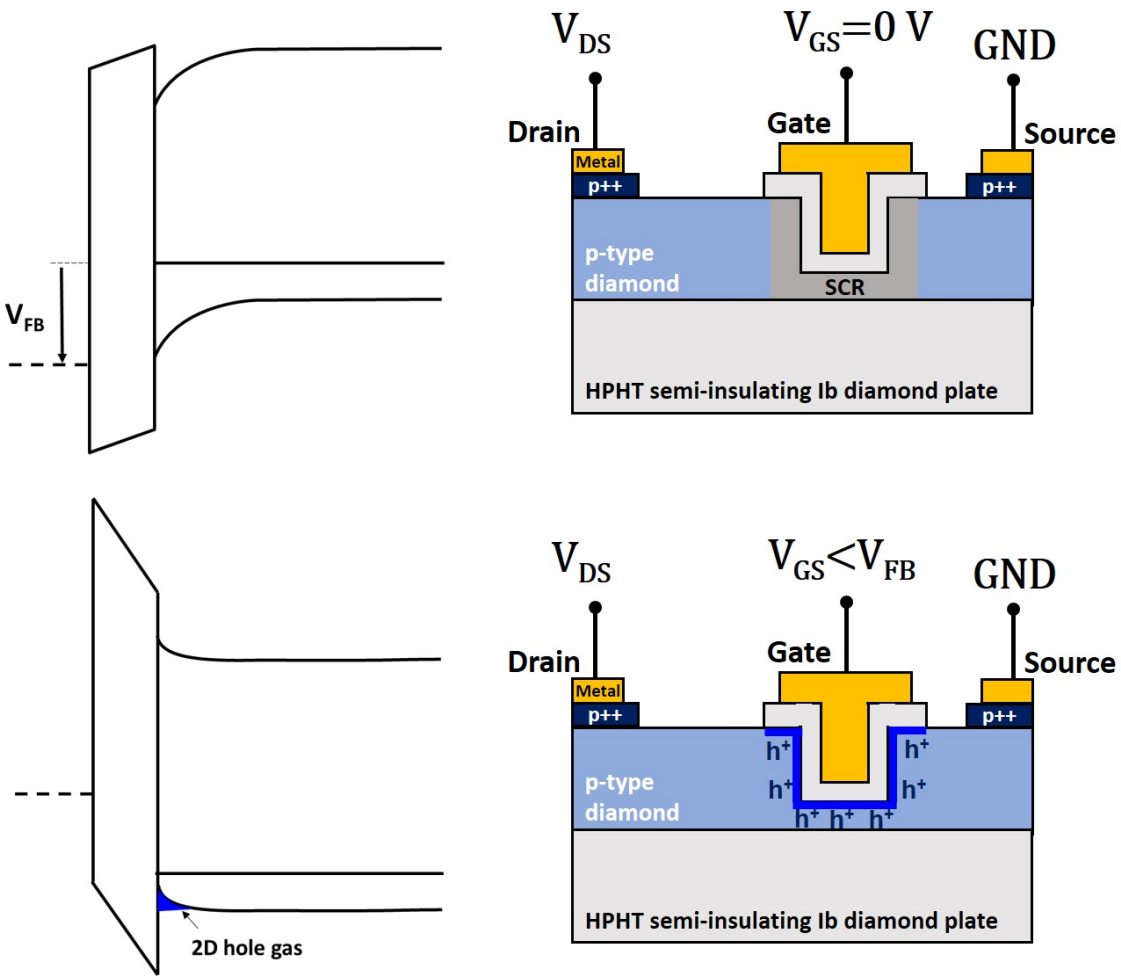


FIGURE 1.21: Schematic cross section of the recess gate diamond depletion MOSFET architecture.

1.4.3 Punch-through design

It is interesting to note that the breakdown voltage could eventually be improved by using a punch-through design [77, 91], i.e. by choosing $L_{GD} < W_{Drift}(E_C)$. The benefit is double, by reducing the drift length the total resistance is decreased and for the same drain bias applied, the maximum electric field is lowered. Moreover, because the ionization integral is calculated over W_{Drift} which is reduced, the critical electric field is also increased. This has not been discussed in details in this manuscript due to the large difference between expected performances and experimentally obtained breakdown voltage in this configuration. This could be due to a dramatic increase of edge effects that cause premature breakdown soon after reaching the punch-through condition. There is in fact one experimental evidence of a successful breakdown increase [92], which has not been reproduced yet.

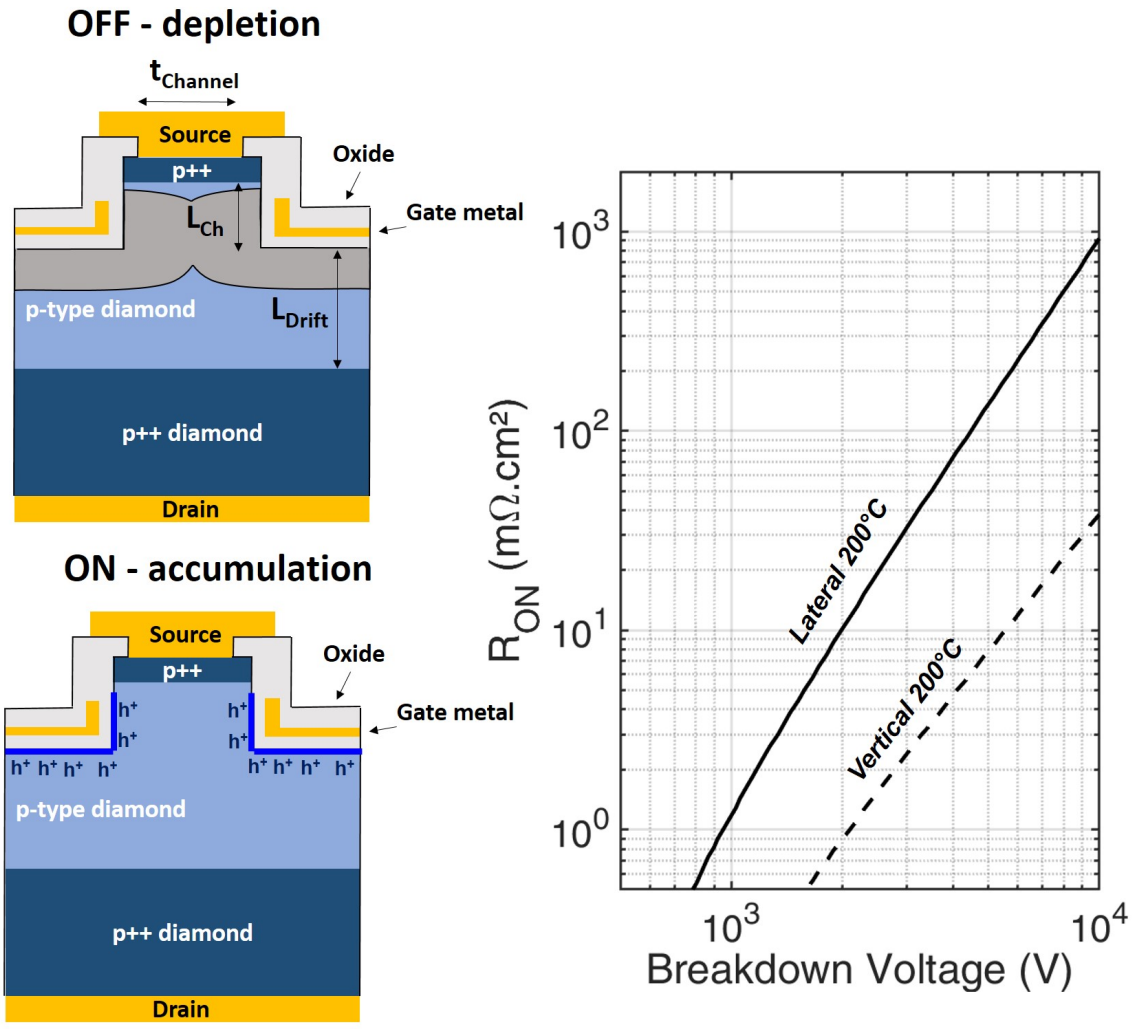


FIGURE 1.22: Schematic cross section of the vertical diamond depletion MOSFET proposed architecture and its calculated R_{ON} vs V_{BD} trade-off compared to the lateral architecture at 200 °C with $t_{ox} = 50$ nm and $V_{TH} = 15$ V.

1.4.4 Vertical depletion MOSFET

The lateral D3MOSFET is the most feasible architecture as for now considering the fabrication processes limitations. However, to compete with other wide band gap semiconductors devices, a vertical design is necessary to lower R_{ON} and to better control electric field crowding effects. The schematic cross section of this structure is represented in fig. 1.22, it is very similar to vertical FinFET designs demonstrated on GaN [93, 94, 95] and Ga_2O_3 [96, 97, 98]. By having the drift region vertical, the used surface area of the chip is much more efficient than a lateral drift design. To give an estimated benefit on the conduction capabilities, lateral and vertical R_{ON} vs BV characteristics are compared in fig. 1.22 at 200 °C. As a first approximation, only the drift resistance is considered to compare the specific on

state resistances with a 1D current distribution:

$$R_{ON,S}^{Lateral} = \rho \times \frac{L_{Drift}^2}{t_{Channel}} \tag{1.32}$$

$$R_{ON,S}^{Vertical} = \rho \times L_{Drift} \tag{1.33}$$

Then, the ratio of the vertical resistance over the lateral one can be approximated.

$$\frac{R_{ON,S}^{Vertical}}{R_{ON,S}^{Lateral}} = \frac{t_{Channel}}{L_{Drift}} \tag{1.34}$$

To have a benefit in using the lateral architecture, $t_{Channel}$ has to be greater than L_{Drift}. Considering L_{Drift} is designed as the SCR extension at breakdown, it is impossible to obtain off state by using a thicker channel than L_{Drift}. With this simple approximation, not taking into account the 2D and 3D effects of the distribution of the current, an improvement of at least one order of magnitude is expected.

However, a number of difficulties is making it challenging for now the fabrication of this vertical architecture with diamond: (i) The growth of a few micrometer thick defect free p++/p stack, as vertical designs are more susceptible to defects such as hillocks, for most of them expand vertically during growth. Threading dislocations are reported to be at the origin of leakage current [99]. (ii) The need for a reliable etching technique with smooth side walls and a process to remove etch pits which cause premature breakdown. (iii) The control of the MOS interface, especially on the side walls of an etched diamond surface. The large trap density at the oxide diamond interface is especially prohibitive in the case of a normally-off FinFET design.

1.4.5 Conclusion

The deep depletion regime in wide band gap semiconductors have been evaluated to be stable over time, allowing to use it in a depletion MOSFET design with a thick channel layer. Based on the physics of the MOS capacitors, the expected performances in terms of conductivity and blocking voltage capabilities of the simplest lateral design have been deduced, as well as the predicted transistor characteristic, thanks to the existing literature providing most of the needed models and parameters. Given the inherent difficulty of processing small sized diamond samples, the lateral architecture is preferred over a vertical design, limiting the number of technological steps. Some more advanced designs are however shown to achieve in principle higher performances and bring this deep depletion MOSFET concept toward the best it can achieve, yet needing more development in process fabrication and diamond growth control. The discussion developed in this chapter assumed an ideal MOS, i.e. no parasitic charges are present in the device and only 1D equations are used. As it will be described in chapter 4, unintentional impurities and structural defects can induce parasitic charging effects, introducing an unpredictable term in the charge neutrality equation altering the MOS characteristic. Moreover the 2D geometry effects have a dramatic impact on the device's performance, as edges are not considered

in the model used here. These considerations are difficult to predict and are intrinsically tied to the fabrication process, an attempt to evaluate their impact will be carried in the chapter 4.

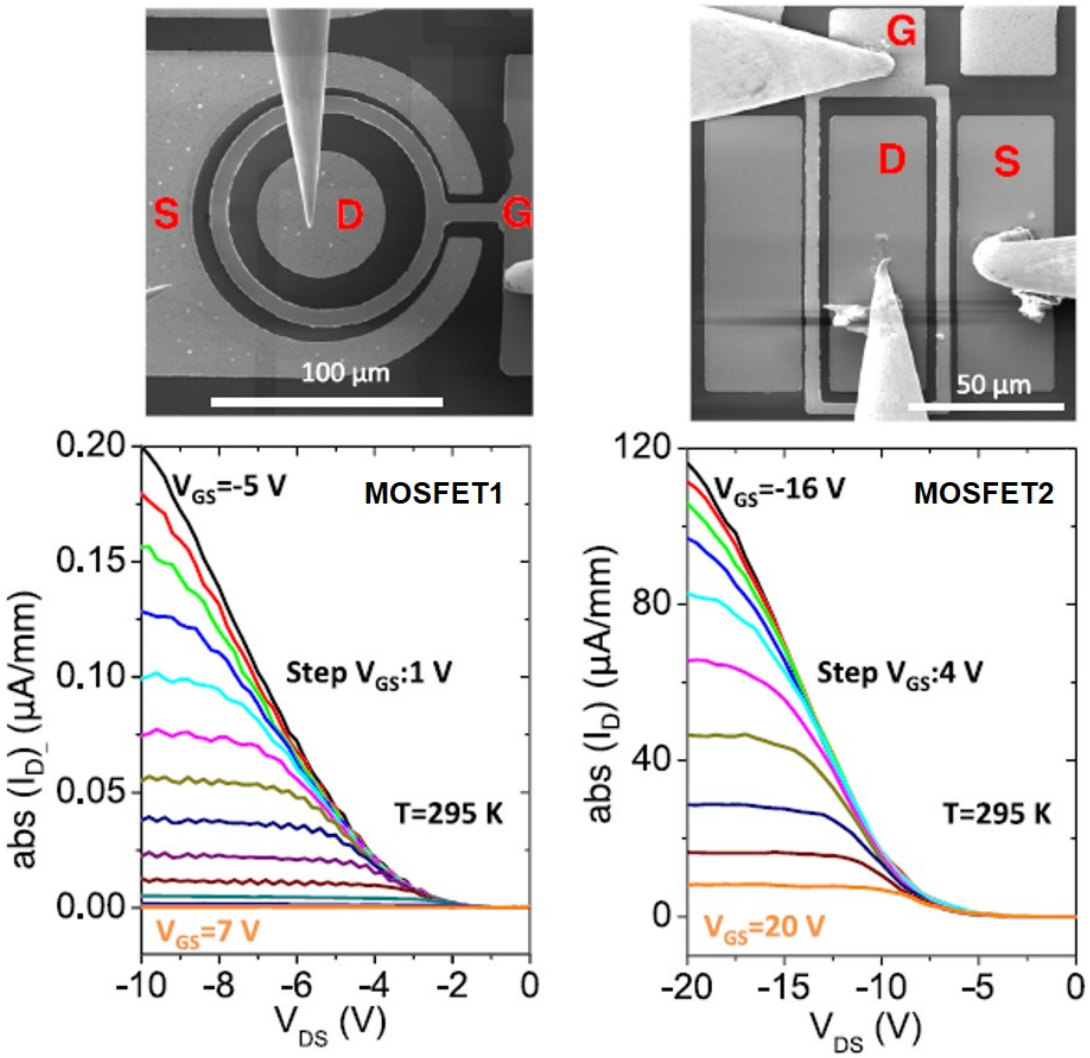
Chapter 2

Device fabrication process

The fabrication process will be detailed, including new steps added to the first demonstrated D3MOSFET by T. T. Pham during his PhD to improve performances, by reducing the contact resistances. The mask design will be established containing several different devices including MIM and MOS capacitors dedicated to the study of the oxide and the diamond/oxide interface.

The diamond deep depletion MOSFET was first demonstrated in [48, 49, 50], exhibiting the transistor characteristics shown in fig. 2.1. In these previous works, two samples were fabricated (MOS1 and MOS2, described in more details in T. T. Pham PhD manuscript [100]) with a boron doped p-type diamond layer grown by plasma CVD as channel, on top of a semi-insulating 1b diamond plate. Ti/Pt/Au stacks were used for source and drain ohmic contacts because Ti creates a good adherence on diamond thanks to carbide formation, the Pt layer is acting as a diffusion barrier between Au and Ti and Au is preventing the oxidation of Ti. After an UV ozone treatment, an alumina layer was deposited by ALD at 380 °C (the upper limit of our ALD setup), followed by a post annealing at 500 °C. This process has been reported to form a crystalline alumina layer [88] with a reduced leakage current and lower interface states density, compared to a lower temperature deposition [86, 101]. Other diamond FETs analysis are reported to use a 450 °C temperature deposition to reduce leakage current [52, 54, 45, 53].

MOS1 and MOS2 transistors are exhibiting a clear transistor effect with a maximum blocking voltage measured at $V_{BD} = -200\ V$ on MOS1. Transistors of MOS2 could not be switched off due to an excessive threshold voltage and so, breakdown was not characterized. These devices suffered from a much higher than expected on state resistance, with a barrier effect for low drain bias, partly due to a high contact resistance. Indeed, obtaining a ohmic behaviour by metal deposition on lightly doped p-diamond is challenging. To improve the contact resistance, a selective growth technique has been developed to produce reproducible source and drain ohmic contacts, in addition to the MOS1 and MOS2 sample process flow, as shown in fig. 2.2. Using a metallic mask deposited by lithography, a highly doped p-type diamond ($[B] > 5 \times 10^{20}$ cm^{-3}) is selectively grown at source and drain contact areas, which will be shown to result in low contact resistances, negligible with respect to the diamond p-layer resistance. A mesa structures was also performed by selective etching of diamond, down to the semi-insulating substrate, to obtain electrically insulated MOSFETs on the same sample with a view to parallelize them. Moreover, large area gate contacts can be shifted on the insulating etched surface, to be connected safely



Samples	t_{p-} (nm)	N_A (cm^{-3})	t_{ox} (nm)	Annealing
MOSCAP1 MOSFET1	230	2×10^{17}	20	No
MOSCAP2 MOSFET2	500	5×10^{16}	40	Yes

FIGURE 2.1: SEM image (top) and transistor characteristics (bottom) measured by sweeping VDS at different fixed VGS of (a) a circular D3MOSFET on a MOS1 with gate length $L_G = 5\ \mu$m, gate source length $L_{GS} = 3\ \mu$m, and gate drain length $L_{GD} = 9\ \mu$m and (b) a rectangular D3MOSFET on MOS2 with $L_G = 4\ \mu$m, gate $L_{GS} = l3\mu m$, and $L_{GD} = 4\ \mu$m. Graphs from [50, 48]

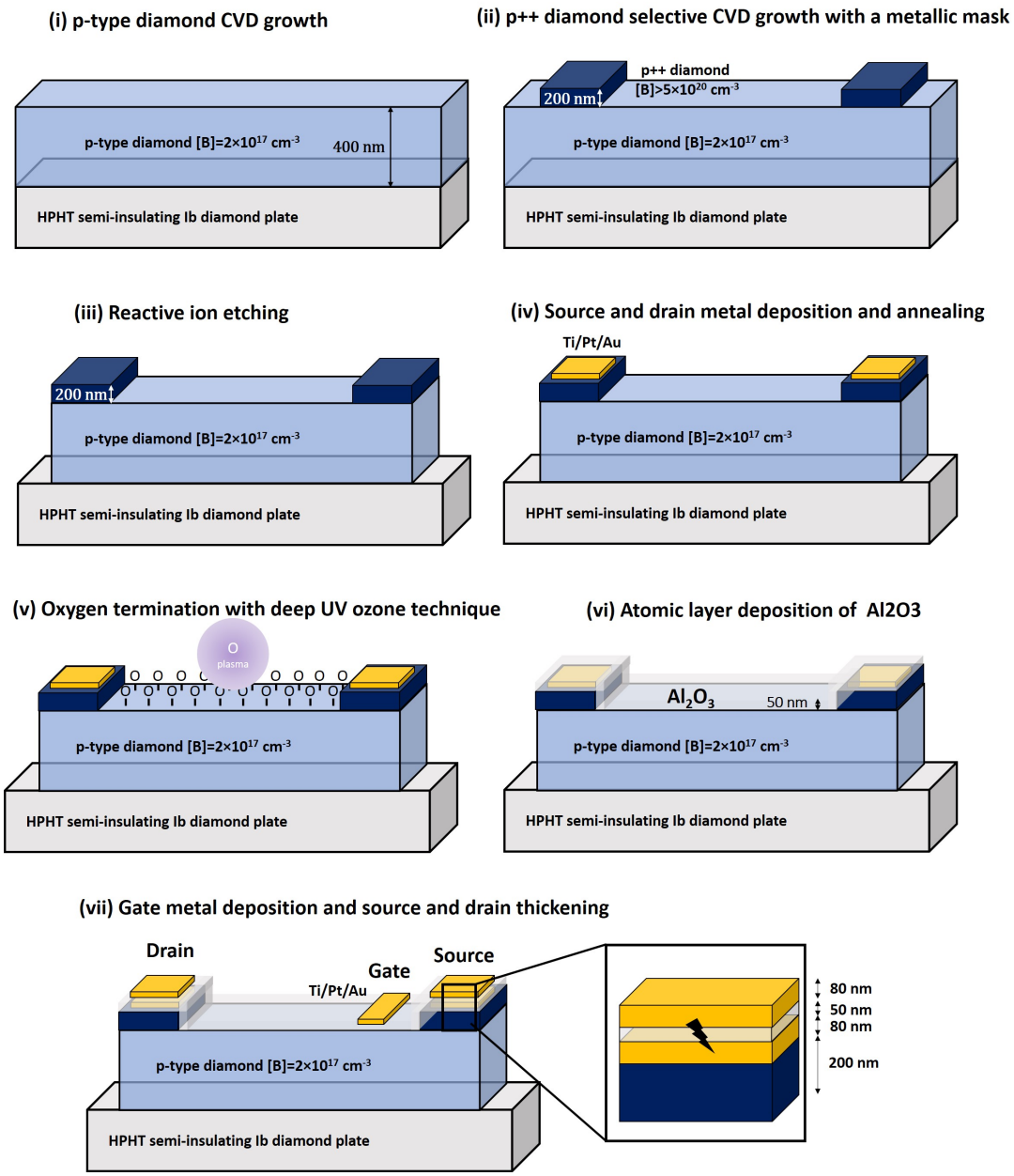


FIGURE 2.2: Schematic cross section of a D3MOSFET on MOS8 sample at the main fabrication steps.

by probe tips and reduce the leakage current. This process flow is however not straightforward considering the non-standard size of the diamond substrates ($4 \times 4 \times 0.5$ mm^3), requiring to adapt of the equipments to this unusual shape. As evidenced in fig. 2.2, no opening of the oxide is performed so the source and drain metal contacts deposited on step (iv) are covered by an alumina layer. This has been an issue to perform measurements in samples MOS1 and MOS2 as the oxide layer had to be mechanically broken with the probe tip each time a measurement was performed. Instead, it was decided to use the gate metal deposition step (vii) to deposit an additional layer on top of the source and drain contacts. The metal-oxide-metal stack formed is then electrically broken at the first measurement by applying a high bias voltage. Subsequent measurements are then easy to perform. It will be shown in the chapter 5 that this process, while not ideal, lead to a negligible contact resistance in comparison to the p-type diamond layer resistance. An etching of the oxide on the source and drain contact would ideally be preferable, but requires an additional lithography step. It was found that electrically breaking the oxide is an acceptable compromise in these lateral structures.

2.1 Mask design

Multiple small devices with different sizing parameters on a 1.3×1.3 mm^2 area were designed, duplicated 4 times with a safe margin of 500 μm from the edges of the substrate, due to the difficulty to get an homogeneous layer of photo-resist in this area after the spin-coating. There are often non uniformities of the p-layer characteristics, defects and lift-off imperfections that could severely affect a larger area device, let alone the risk of breaking the devices while manipulating it. This has been well highlighted by H. Umezawa et al. in ref. [102] using Schottky diodes, with a clear relation showing that higher area diodes exhibit a lower maximum electric field in off state, in addition to non uniformities of the on state resistances and ideality factors across the sample. It is then much safer to design numerous separate devices on the same substrate.

The mask used is shown in fig. 2.3 with the following structures:

(i) Transfer Length Measurement (TLM) contacts on the p-type layer and on the p++ layer to measure the diamond layers resistivity and the contact resistances.

(ii) Metal-Insulator-Metal Capacitors (MIMCaps) to get an accurate measure of the oxide capacitance.

(iii) MOSCaps to characterize the diamond/oxide interface by impedance measurements. The small surface of the D3MOSFETs gates makes difficult an in-depth analysis by capacitance measurement as the weak signal is close or under the detection limit of the measuring device used.

(iv) Circular and linear D3MOSFETs with varying L_G, L_{GD}, L_{GS} and contact length W.

(v) Circular and linear double gate D3MOSFETs, of which the interest will be discussed in chapter 5.

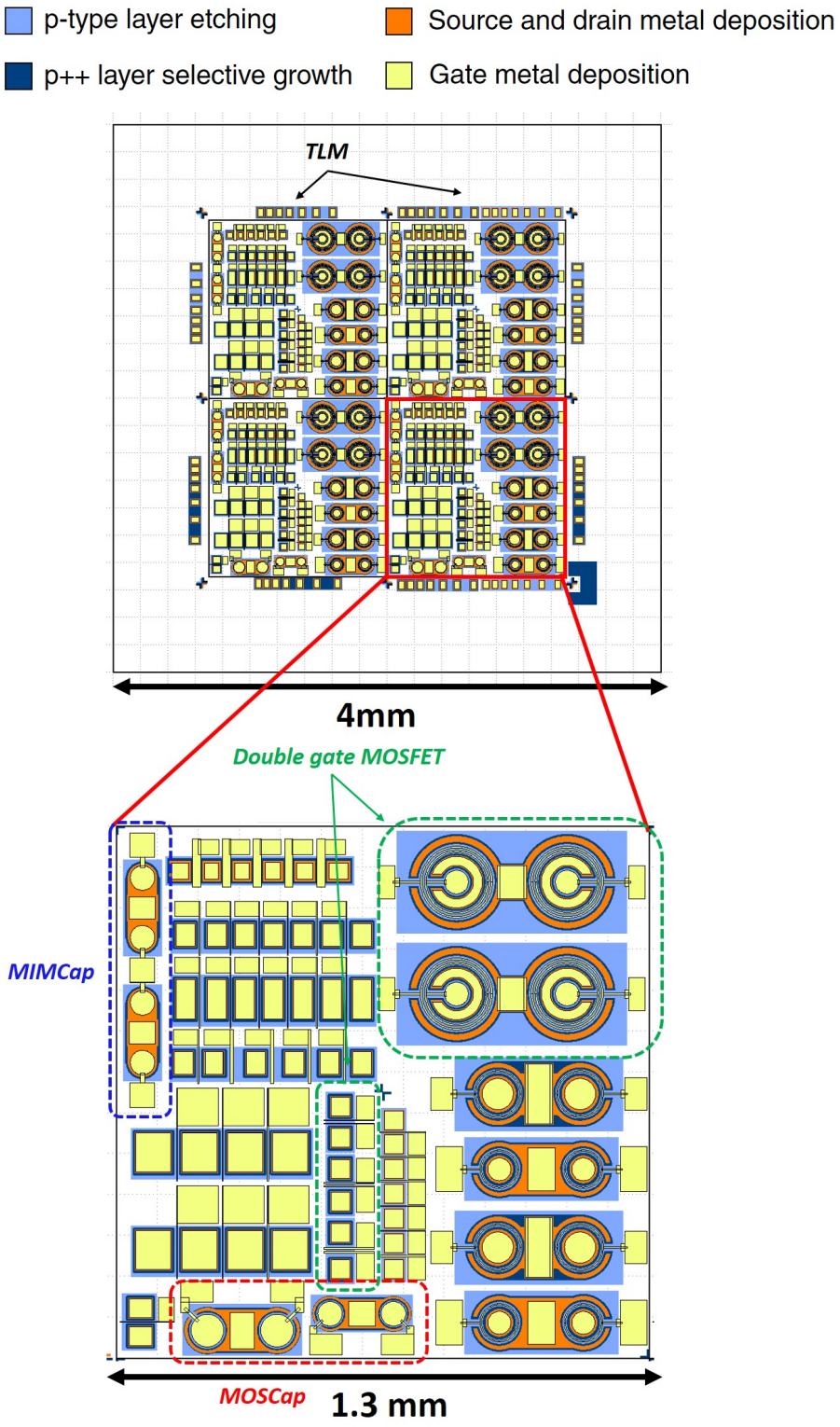


FIGURE 2.3: Full view of the mask at left composed of 4 identical reticules detailed at right, TLM bars and alignment crosses are placed around. Non-highlighted patterns are variations of the single gate D3MOSFET.

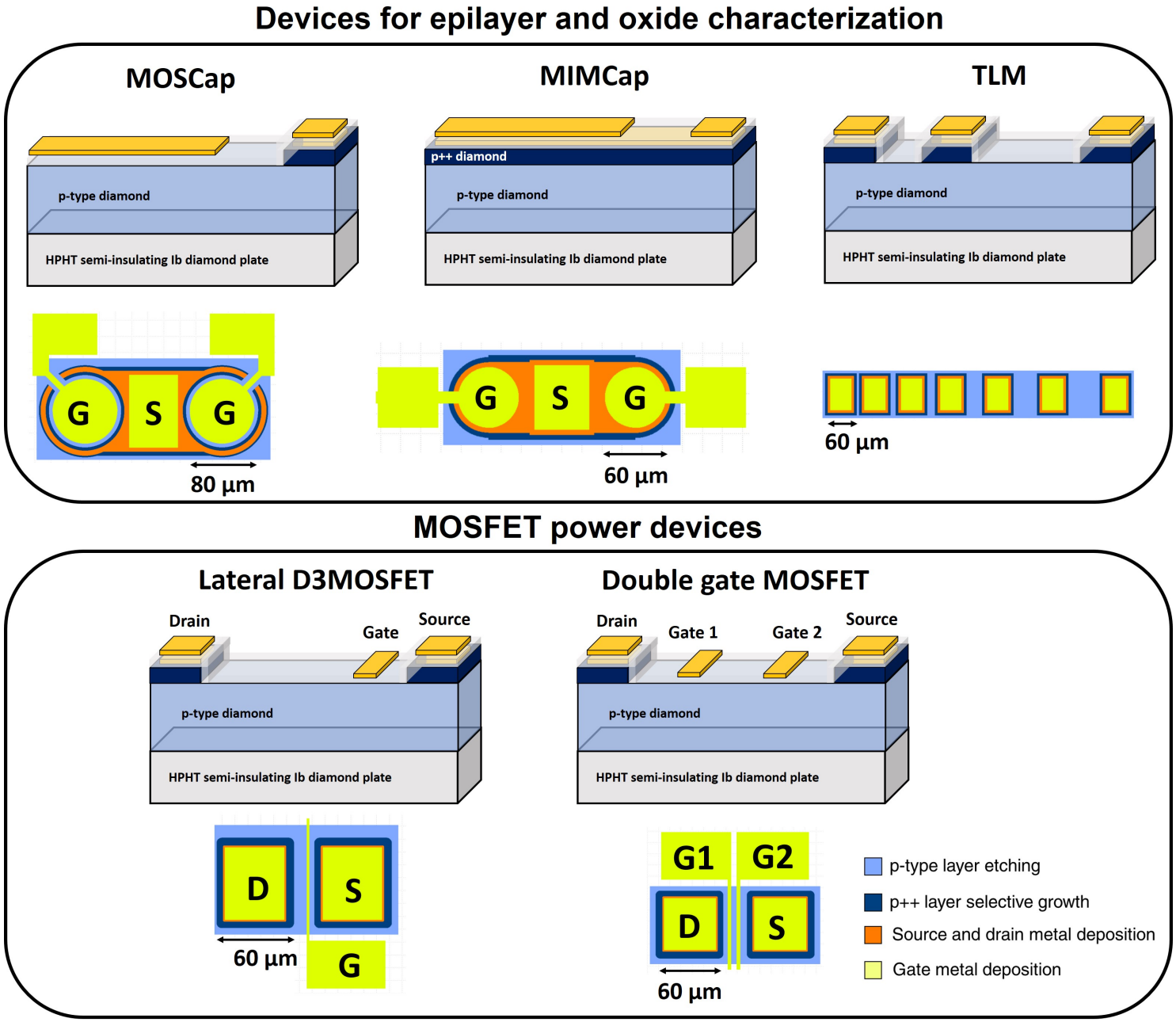


FIGURE 2.4: Cross sectional and top view of some of the designs used on the masks.

2.2 Sample fabrication

A total of 6 samples were processed, referred as MOS3 to MOS8. Amongst them, MOS4 and MOS5 where reclaimed from MOS1 and MOS2 respectively using a standard acid cleaning, their p-layers were already grown and characterized by T. T. Pham during his PhD [100]. Process flow main steps are described in fig. 2.2, with values corresponding to that of the sample MOS8.

2.2.1 Diamond p-layer growth on a HPHT diamond substrate

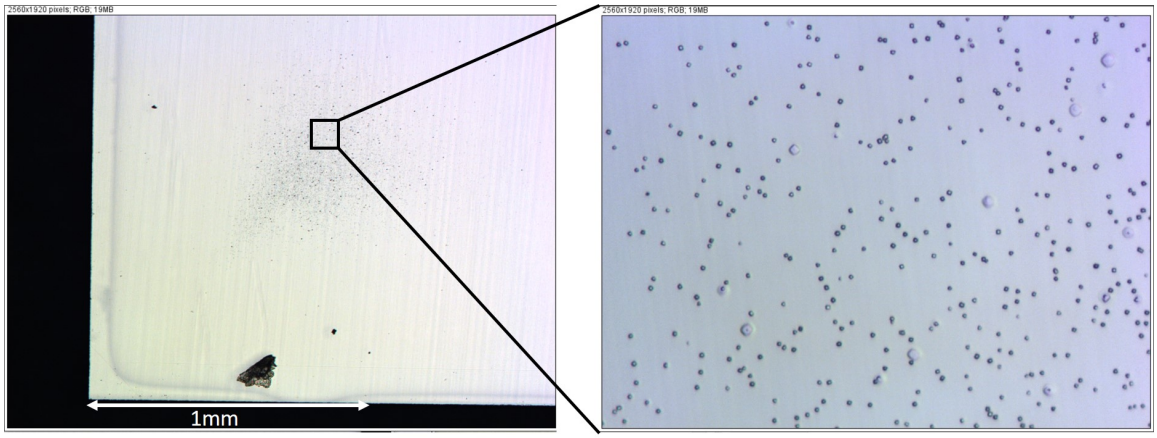


FIGURE 2.5: Optical image of the sample MOS3 after the p-layer growth. Defects are clearly visible with a non-homogeneous distribution.

Two types of substrates were used, 1b (100) HPHT diamond from Sumitomo and IIa (100) HPHT diamond from NDT, polished by Syntek to an average surface roughness between 1 and 2.5 nm. The 1b diamond is commonly used to fabricate lateral diamond device as it contains nitrogen up to several tens of ppm, according to the provider, ensuring good insulating properties (nitrogen is a deep donor with an activation energy >1.4 eV). The IIa substrates have a better crystalline quality due to their high purity [103], but have never been tried before in our research group for lateral devices. Before growth, the substrates are cleaned by a standard acid treatment, the epitaxy is then performed by Microwave Plasma-enhanced Chemical Vapor Deposition (MPCVD). The p-layer of MOS8 was grown by Juliette Letellier (PhD at Institut Neel) and all others by myself with her assistance and that of David Eon (lecturer at University Grenoble Alpes and Institut Neel). After growth, there is no noticeable roughness change however defects appeared on the surface, identified as hillocks and crystallites (fig. 2.5). Their distribution is not homogeneous and vary a lot from one sample to another but are always present. Due to the small number of sample processed and the important variability of results, we could not conclude if a IIa or Ib substrate is more beneficial in this regards.

2.2.2 Toward improved D3MOSFET device performances: the p++ selective growth and mesa etching

A 200 nm p++ selective growth is achieved by using a 400 nm thick Ti mask for its adherence, deposited by laser lithography and electron beam evaporation. However this method is not reliable and failure may occur during the CVD diamond growth as the mask can be removed by the plasma (MOS5) or growth under the mask can occur (MOS3), fortunately limited at the edge of the sample in this last case. The mask is then removed by acid cleaning. To form the mesa structure, a 600 nm etching was performed by Reactive Ion Etching (RIE) technique with a 150 nm aluminum mask deposited by laser lithography.

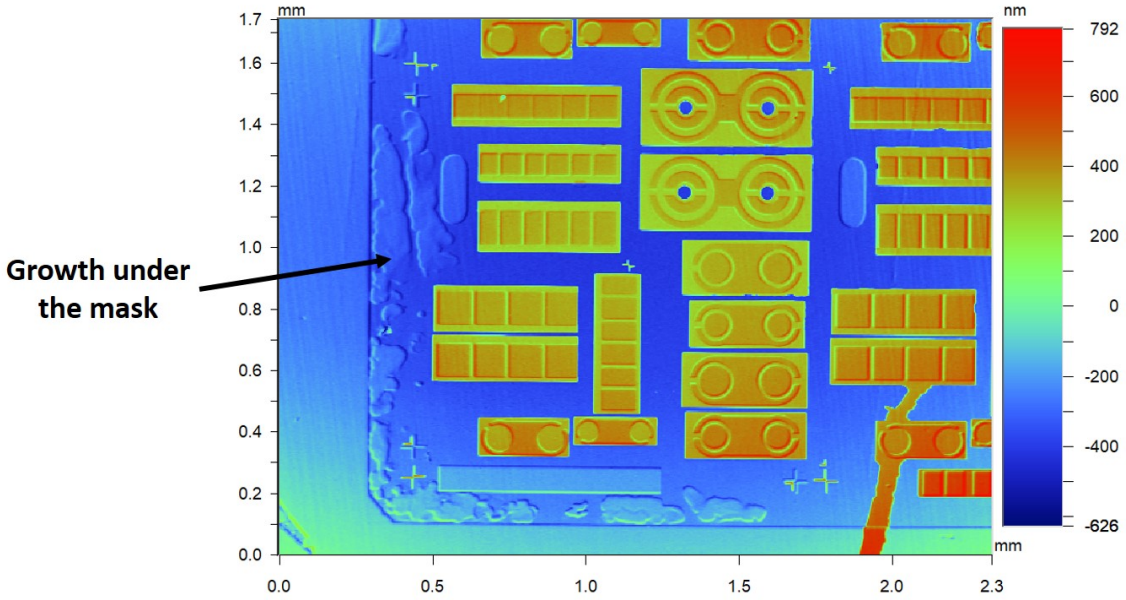


FIGURE 2.6: Optical profilometry image of the sample MOS3 after p++ selective growth and mesa etching. Growth under the Ti mask occurred at the edge of the sample.

At this point, it appeared that the IIa substrates of samples MOS6 and MOS7 were conducting as an Current-Voltage (IV) test between two contacts separated by a mesa etching yielded a significant current, while it was made sure that the etching was deep enough, down to the substrate. A previous test was performed before processing using metal contacts on the back side after a 1h 500 °C in high vacuum annealing, with no measurable current. An Electron Beam Induced Current technique (EBIC) imaging revealed that these contacts were actually Schottky diodes, due to the difficulty to obtain ohmic contact on low doped samples. When measuring two of these diodes in series one would always be in reverse blocking regime and no current can be measured. These substrates are found to be p-type (boron doped) with a non-homogeneous doping level between 10^{15} and 10^{16} cm^{-3}, making them unusable for lateral devices without a buffer layer.

At the opposite, MOS4 sample fabricated by reclaiming MOS1 was showing no conduction between ohmic contacts. Transistors fabricated on MOS1 were already very resistive, it could be possible that the acid cleaning etched a few nm of diamond making it

completely depleted by a high surface potential. An UV ozone treatment as well as a thin (5 nm) alumina layer deposition have been tried to unpin the surface without success.

2.2.3 Oxide and metal deposition

Source and drain contacts were deposited by laser lithography and metal evaporation (Ti/Pt/Au 30 nm/20 nm/30 nm), followed by an annealing at 500 °C in high vacuum ($< 10^{-7}$ mBar) during 30 min in order to create a carbide and thus improve the adherence and lower the contact resistance. The deep UV ozone technique was used to passivate the surface just before the alumina deposition by ALD at 380 °C (40 nm on MOS3 and 50 nm on MOS8). Then a 500 °C annealing in high vacuum during 30 min was performed and finally the gate metal stack (Ti/Pt/Au 30 nm/20 nm/30 nm) was deposited by laser lithography and metal evaporation.

Only MOS3 and MOS8 samples could be finished, yet MOS3 suffered from lift-off issues at the end of the process and only a few devices could be characterized with limited analysis, not shown in this manuscript. This was solved by using a thicker lithography resist deposition on MOS8 to facilitate the lift-off. A SEM image of the fabricated transistor on MOS8 is shown in fig. 2.8.

	MOS3	MOS4	MOS5	MOS6	MOS7	MOS8
Substrate	Ib	Ib	Ib	IIa	IIa	Ib
Doping	5×10^{16} cm^{-3}	2×10^{17} cm^{-3}	5×10^{16} cm^{-3}	1×10^{16} cm^{-3}	5×10^{16} cm^{-3}	2×10^{17} cm^{-3}
p-layer thickness	400 nm	230 nm	510 nm	700 nm	360 nm	400 nm
Oxide thickness	40 nm					50 nm
Comments	Poor lift-off	Fully depleted, high surface pinning effect	Selective growth failure, removal of the metallic mask during growth	Parasitic substrate conduction	Parasitic substrate conduction	OK

FIGURE 2.7: Summary of the sample fabricated during this PhD with the key fabrication parameters used.

2.3 Conclusion

As detailed in this chapter, compared to previously devices fabricated by T. T. Pham, two additional steps have been added to improve the performances: the selective growth of p++ diamond and the mesa etching. As failure can happen in any steps, only one fully working sample has been fabricated. As previously done, the fabricated sample consists of multiple small devices spread over its surface and separated by a mesa etching. MIMCaps,

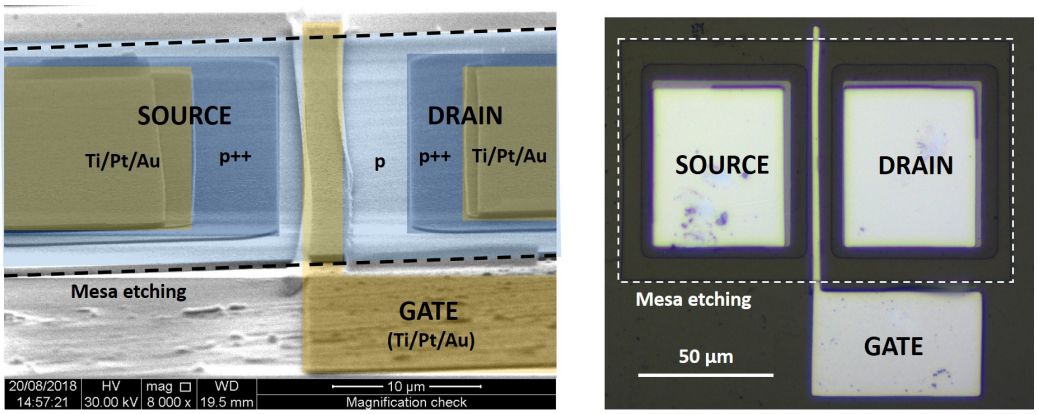


FIGURE 2.8: At left, SEM image of a fabricated transistor on MOS8 with a tilt angle close to 90°. At right, optical top view of the transistor.

MOSCaps, TLM contacts and MOSFETs of various shapes and sizes allow for a complete electrical characterization of the sample.

The diamond device fabrication is rendered difficult by the lack of standardized processes. The small sample size as well as the non perfect control of some decisive steps, such as the defect-free growth and the lift-off procedure, makes difficult the fabrication of large sized devices. Moreover, the number of available substrates being limited and the time required to complete one reaching several months depending on equipment availability. All the device measurements shown in this manuscript have been performed on the MOS8 sample.

Chapter 3

The 1b nitrogen doped substrate electrical characterization for lateral diamond FET

A focus will be done on the diamond 1b semi-insulating substrate, commonly used for the fabrication of lateral diamond devices. The substrate electrical transport properties will be investigated to evidence in which cases it can be considered as a n-type doped semiconductor or an insulator, greatly impacting the device characteristics.

With the lateral MOSFET design used, it is essential to isolate the p-type conducting layer from any other conduction path, typically through the substrate, to not introduce a significant leakage current. Most diamond lateral devices reported in literature make use of a semi-insulating 1b diamond substrate which contains a high level of nitrogen donor impurities ($\approx 10^{19}$ cm^{-3}), with a very high activation energy of >1.4 eV. At room temperature, close to no nitrogen donor are ionized and even at temperature up to 300 °C, the maximum temperature of our measurement set-up, the carrier concentration will be shown to remains less than 10^{10} cm^{-3}. The parasitic current flowing through the substrate is then negligible campared to the p-type layer conductivity for all the temperatures probed. However, it has been suggested in the PhD of T. T. Pham [100] that the substrate acts as a n-type semiconductor and forms a PN junction with the p-type layer, inducing a parasitic SCR. Nitrogen doped diamond has been previously used to fabricate Schottky-PN diodes [104], demonstrating that the Fermi level position is corresponding to that of a n-type layer. It was nonetheless still unclear if this SCR could be modulated and how it affects the device characteristics.

It will be demonstrated in this chapter that the PN diode, formed by the 1b substrate (500 μm thick) and the boron doped epitaxial layer, can indeed be modulated, intentionally or not, under high temperature (typically > 250 °C) as the few ionized donors are enough to allow for charge equilibrium. A PN diode current-voltage characteristic has been obtained for different temperatures (fig. 3.1). Moreover, biasing under visible light exposure at room temperature is also found to generate enough free carriers to modulate the PN diode, providing an original diamond light activated PN junction. The substrate polarization V_{Sub} is then an important parameter to control in these conditions to avoid parasitic

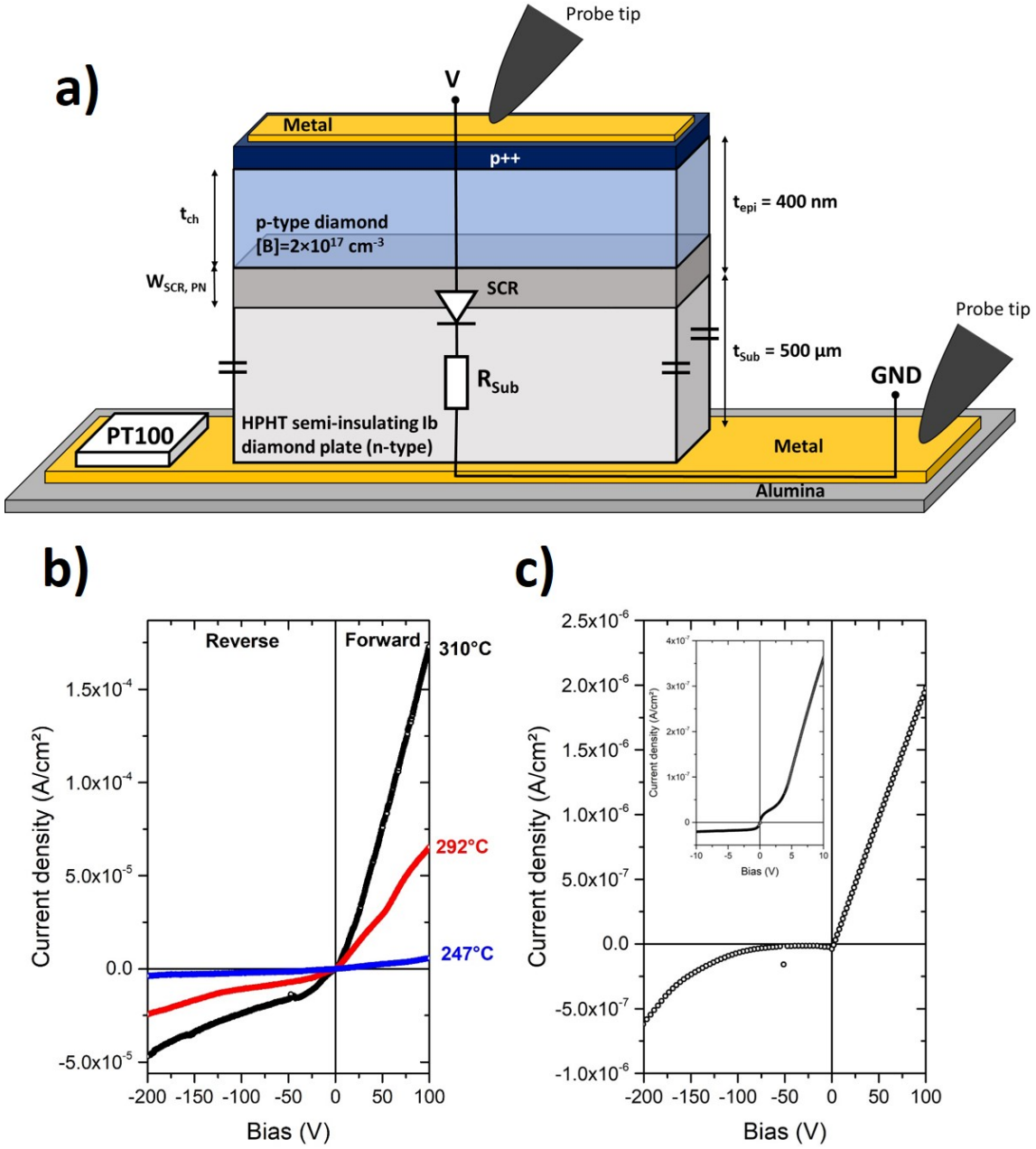


FIGURE 3.1: a) Schematic representation of the PN diode, the back side of the substrate is contacted with silver paste. b) Current-voltage characteristics of the PN diode formed by the p++/p/n-type substrate stack at 247 °C, 292 °C and 310 °C. Temperature was measured using a PT100 resistance temperature sensor located next to the sample, glued with metallic paste on the alumina plate. At right, room temperature IV characteristic under visible light exposure (microscope lamp), the dark current is below the detection limit. c) Current-voltage measured between -10 V and +10 V, the built-in voltage is extracted around 4 V.

effects during the MOSFET operation. First, the expected behaviour of such junction is presented and is then compared to experimental transport characterization obtained under high temperature or visible light optical excitation.

3.1 The one sided abrupt PN diode

In an abrupt PN diode at equilibrium, for a homogeneous doping in p-side and n-side regions and abrupt junction, the charge in the p-side must be equal to the one in the n-side so that:

$$N_A W_{SCR,p} = N_D W_{SCR,n} \tag{3.1}$$

Where $W_{SCR,p}$ and $W_{SCR,n}$ are respectively the SCR extension in the p-side and the n-side.

In the case of the one sided junction considered here where $N_D >> N_A$ we have: $\frac{W_{SCR,p}}{W_{SCR,n}} = \frac{N_D}{N_A} \approx 10^2$. So we can use the approximation that all the SCR extends in the p-side:

$$W_{SCR,PN} \approx W_{SCR,p} \tag{3.2}$$

Where $W_{SCR,PN}$ is the total width of the SCR in the diode, written as function of applied bias V on p-side:

$$W_{SCR,PN} = \sqrt{\frac{2\epsilon_0 \epsilon_{SC}(V_{bi} - V)}{qN_A}} \tag{3.3}$$

V_{bi} is the built-in potential of the diode, corresponding to the conduction and valence band potential difference between the p and n-side at zero applied bias. It can be expressed as:

$$V_{bi} = \frac{k_B T}{q} ln(\frac{p_0 n_0}{n_i^2}) \tag{3.4}$$

Where n_0 and p_0 are respectively the n-side and p-side bulk electron and hole concentration in the neutral region at thermal equilibrium.

For $N_A = 2 \times 10^{17}$ cm^{-3} at room temperature, $V_{bi} = 3.9$ V, yielding a built-in SCR extension $W_{SCR,PN}(0V) = 108$ nm.

A schematic representation of the band diagram of the one sided PN junction is shown in fig 3.2, at equilibrium and under a forward bias V.

3.2 Nitrogen ionization energy, thermal activation of the substrate / epilayer junction

Estimation of the ionization energy of nitrogen donors is made by fitting the slope at +10 V of the current versus temperature, yielding $E_A = 1.45 \pm 0.1$ eV. Experimental data measured by [105] plotted on fig. 3.3 as comparison gives $E_A = 1.74$ eV, similar to other reported values in literature [106]. A rough estimation of the free electrons density is made from the on state resistance of these characteristics. Since no exhaustive description of the

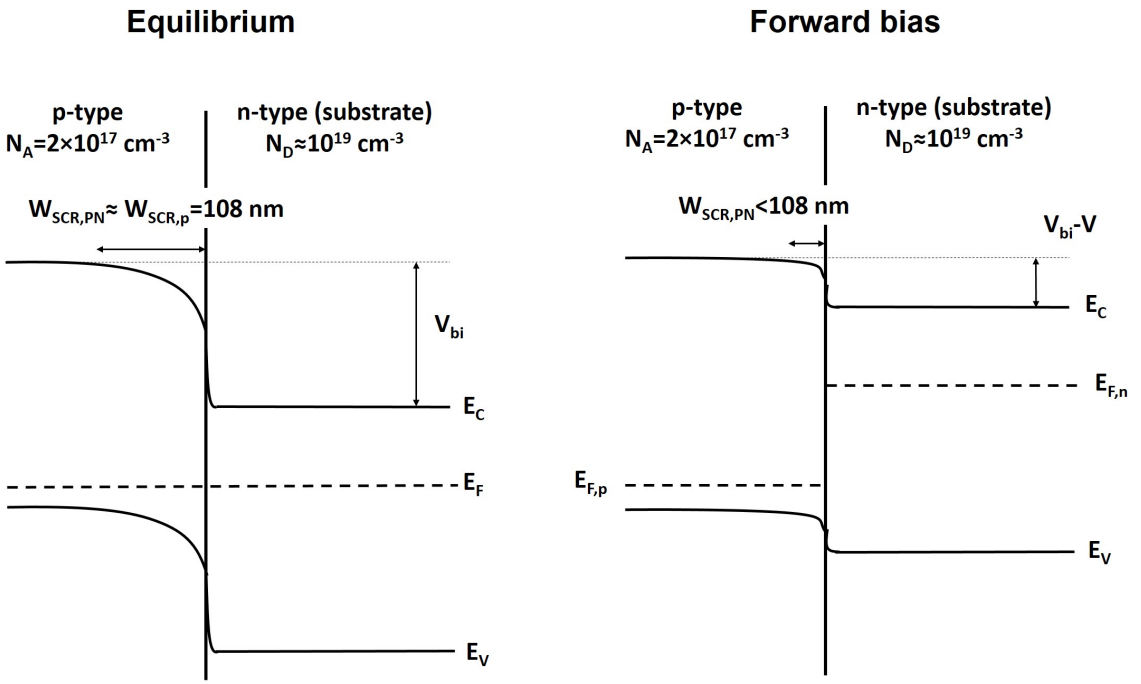


FIGURE 3.2: Schematic representation of the band diagram of a one sided PN junction at equilibrium and under a forward bias V.

mobility have been reported in literature regarding nitrogen doped diamond, a model of phosphorous doped diamond electron mobility was used from [107]. Whether free electrons come from nitrogen or phosphorous donor, they are in the conduction band with undifferentiated phonon interactions. As such the transport properties are the same and the model can be adapted by changing the ionization energy of the donor atom. The doping level was set to 1×10^{19} cm^{-3} and ionization energy at 1.45 eV, the acceptor density was then adjusted to 1×10^{16} cm^{-3} to get a fit on experimental data. This is coherent with SIMS measurements performed in ref. [108] on a 1b diamond sample from the same provider, where nitrogen density is extracted around 2×10^{19} cm^{-3} and the boron density between 5×10^{15} cm^{-3} and 1×10^{16} cm^{-3}.

3.3 Optical activation of the substrate/epilayer junction

The IV characteristic of the PN diode at room temperature under a visible light optical excitation of 11 mW/cm^2 is shown in fig. 3.4. A clear rectifying behaviour is observed with a built-in voltage V_{bi} around 4 V. The dark current remains below detection limit in the full bias range probed, from -30 V to +20 V.

To investigate the effect of the light irradiance on the back PN diode, IV characteristics shown in fig. 3.5 were measured under different irradiance conditions using the adjustable white light of the microscope. The irradiance values were determined thanks to a photodiode, but this method only gives a mean value as the power density of the light spot is not homogeneous.

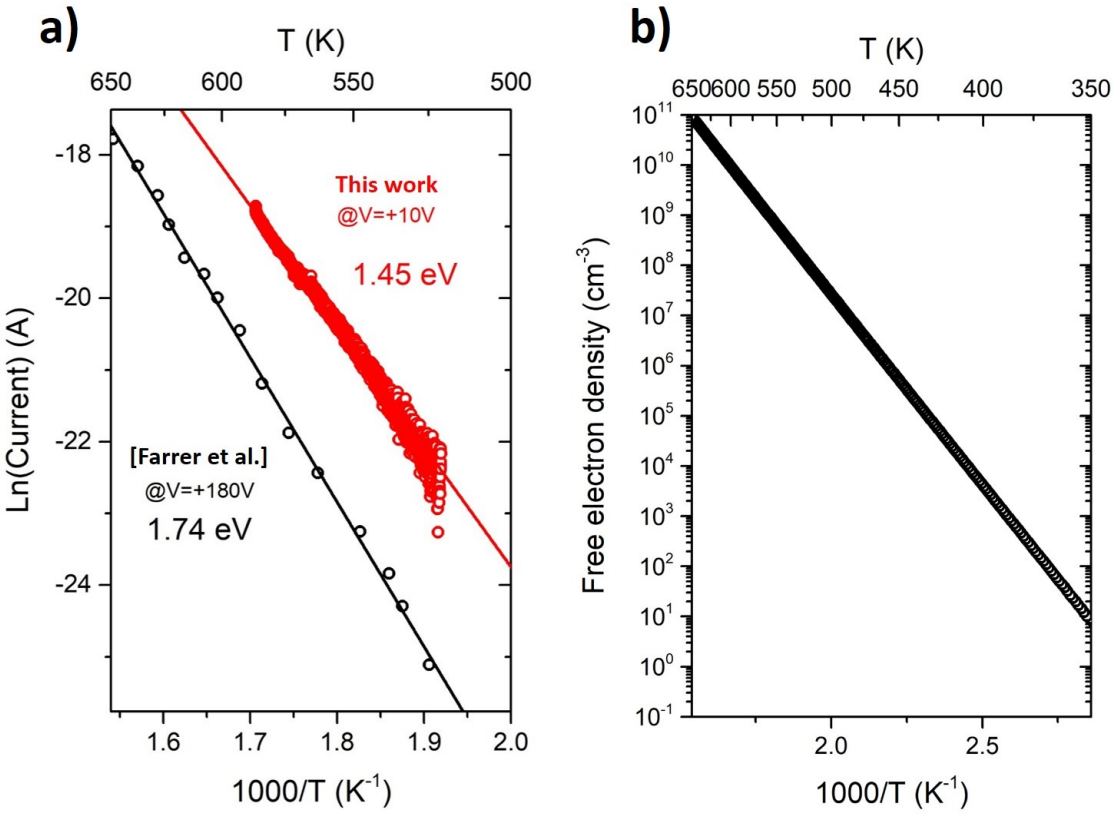


FIGURE 3.3: a) In red, natural logarithm of the current in forward regime at +10 V as function of 1000/T measured on the sample MOS8. An activation energy of $E_A = 1.45 \pm 0.1$ eV is extracted from the linear fit. In black, data from ref. [105] for a forward bias of +180 V giving the commonly reported value of around 1.7 eV. b) Calculated free electron density in the substrate as function of the temperature using a compensating acceptor density of 10^{16} cm^{-3} and a doping level of 10^{19} cm^{-3}.

It can clearly be seen that the forward characteristic of the diode is linear, limited by the substrate resistance R_{Sub}, and is dependent on the irradiance. Extraction of R_{Sub}^{-1} as function of the irradiance yields a linear dependence, as expected in the case of light generated carriers current. The dark current is below the detection limit due to the extremely low carrier concentration, $n < 1$ cm^{-3} according to the estimation shown in fig. 3.3 at room temperature. Due to the large indirect band gap of diamond, the photon wavelength required to observe intrinsic photoconductivity is expected to be lower than 225 nm, but the light used in this experiment does not emit in the UV range. The photoelectric effect observed is then understood as extrinsic photoconductivity, where nitrogen donors are ionized by incident photons and generate free electrons in the conduction band. Contrary to the intrinsic photoconductivity, only one type of carriers is generated. Assuming an ionization energy between 1.7 eV and 1.45 eV, the corresponding minimum wavelength is ranging between 730 nm and 856 nm. This mechanism is however not efficient and only a fraction of the incident power is generating carriers, due to the dispersion of nitrogen

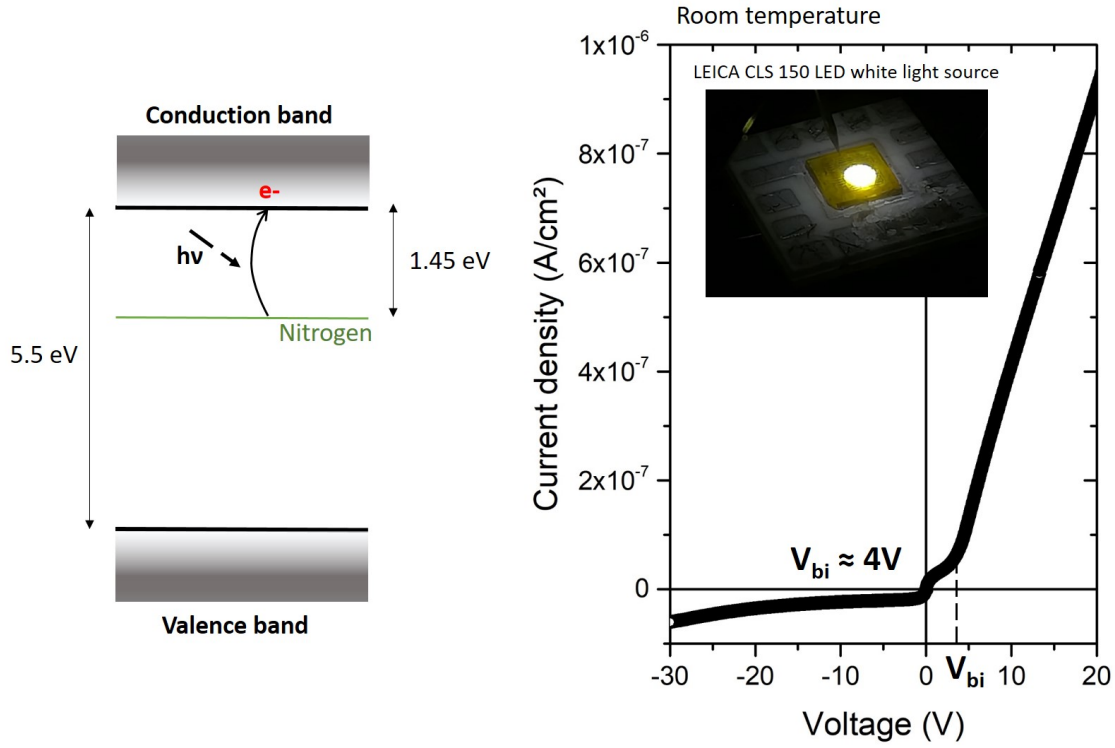


FIGURE 3.4: At left, schematic band diagram of the extrinsic photoelectric effect, where a photon ionize a nitrogen donor to generate a free electron in the conduction band. At right, room temperature IV characteristic measured under a white light irradiance of 11 mW/cm^2. V_{bi} is extracted around 4 V.

atoms in the lattice, i.e. $[N]/[C] \approx 10^{-4}$. For an irradiance of 11 mW/cm^2, the carrier density generated is in the order of 10^8 cm^{-3}, by comparing with the same resistivity value obtained in the dark by heating up the sample. The mobility and incomplete ionization models allow to correlate a resistivity value at a certain temperature to a carrier concentration. The maximum optical power obtained in this experiment is however relatively low due to the limited focus of the beam we could obtain, power densities in the order of 100 W/cm^2 could be realistically obtained with a specific setup. Moreover, the structures measured have opaque metallic contacts that limit the light exposure of the diode. Therefore, generated carrier densities in the order of 10^{12} cm^{-3} to 10^{13} cm^{-3} could be obtained with a higher irradiance and semi-transparent contacts.

3.4 Substrate blocking voltage capabilities

When the substrate is insulating (around room temperature in the dark), a large potential difference between the drain and the substrate can be used without disturbances of the device operation. A voltage as high as 1 kV was applied without any measurable current being probed. Due to the insulating nature of the material, the potential drop is held by the full thickness of the substrate and the electric field remains low for diamond (for 1 kV over

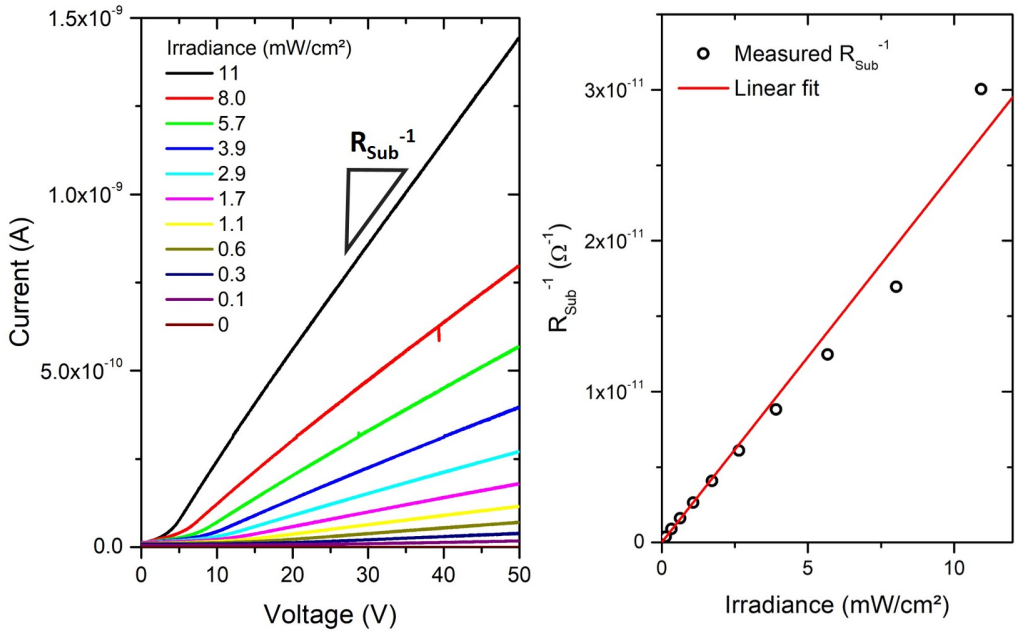


FIGURE 3.5: At left, IV characteristics in forward measured under different irradiances, the dark current is below the detection limit. At right, extracted R_{Sub}^{-1} as function of the irradiance, exhibiting a linear dependence.

0.5 mm, the electric field is 20 kV/cm). However if the substrate is activated and behaves as a n-type material (under optical excitation or at high temperature), then most of the potential drop would be held by the thin junction and breakdown may occur. It is important for the device operation in this condition that this vertical breakdown does not limit the device performances compared to the lateral breakdown of the MOSFET occurring below the gate.

Due to the very high resistivity of the substrate, isolating the hard breakdown of the device from the leakage current can be difficult at high temperature. To circumvent this issue, a low temperature measurement at $T = -50\,°C$ was performed under a light exposure of 11 mW/cm^2 to limit the leakage current which is temperature dependent, as shown in fig. 3.6. The serial resistance of the substrate was not significantly changed from room temperature.

(i) For $V > V_{bi}$, the PN junction is biased in forward regime. Due to the high resistance of the substrate ($R_{Sub} = 36.4\,G\Omega$) in comparison of the forward biased PN junction, all the potential drop is on the thick substrate and a linear IV characteristic is observed.

(ii) For $V_{BD} < V < V_{bi}$, the PN junction is biased in reverse regime, the current is much lower than in forward. In this case the reversed biased PN junction is more resistive than the substrate and almost all the potential drop is on the relatively thin junction, leading to a much higher maximum electric field than in forward. Assuming that the PN junction is one sided, the SCR eventually extends in the full epilayer thickness in a punch-through configuration.

(iii) For $V < V_{BD}$, an abrupt change of resistance is observed from the reverse regime,

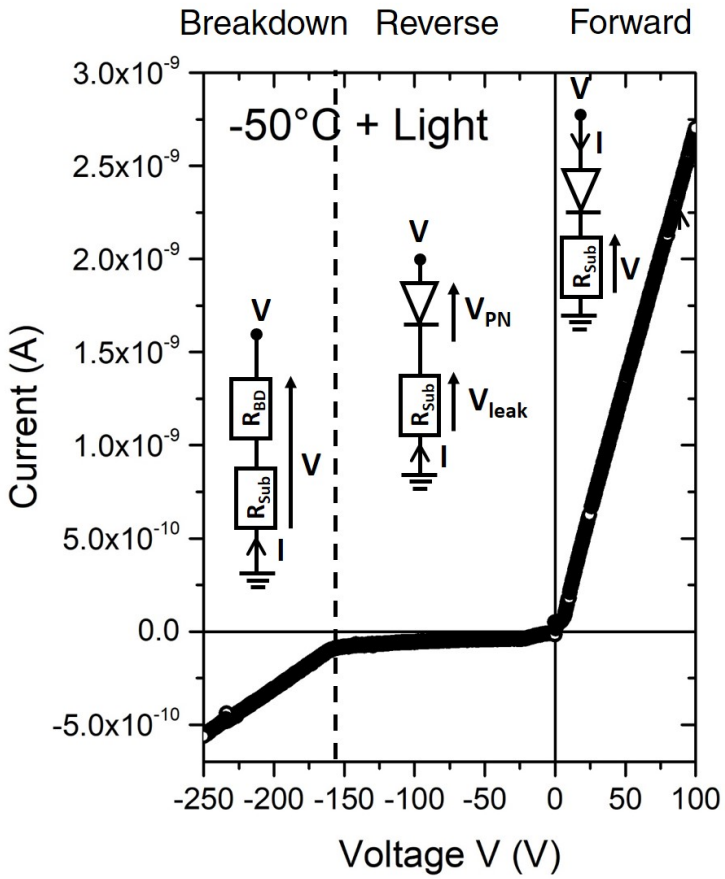


FIGURE 3.6: IV characteristic of a 5.4×10^{-4} cm^{-2} diode at $T = -50\,°C$ under an irradiance of 11 mW/cm^2.

characteristic of a breakdown that occurred at $V_{BD} = -160$ V. The diode is no more blocking and a constant resistance of 198 GΩ is measured. It is assumed that the breakdown did not occurred in the full device surface, but instead is the result of a local peak electric field due to edge effects. The device resistance is then higher than in forward regime because the current is flowing only in the broken area. This is modelled by adding an additional resistance R_{BD}. To find the maximum blocking voltage of the junction, the potential drop in the PN junction has to be corrected by the leakage current, that induce the presence of a parasitic potential drop in the substrate $V_{leak} = R_{Sub} \times I$:

$$V_{PN} = V - V_{leak} \tag{3.5}$$

It is found that at breakdown, $V_{PN} = -156$ V. Assuming that all the junction voltage drop is sustained in the 400 nm p-type layer with a doping $N_A = 2 \times 10^{17}$ cm^{-3}, and by using a 1D model neglecting 2D effects, one can show that the maximum electric field E_m at $V = V_{BD}$ in the punch through configuration is [109]:

$$E_m = \frac{V}{t_{epi}} + \frac{qN_A}{2\epsilon_0\epsilon_{SC}} t_{epi} \tag{3.6}$$

The electric field as function of the depth along the cutline of fig 3.6, where $x = 0$ on the surface, is then given by:

For $0 < x < t_{epi}$:

$$E(x) = \frac{V}{t_{epi}} + \frac{qN_A}{\epsilon_0 \epsilon_{SC}}(\frac{t_{epi}}{2} - x) \tag{3.7}$$

For $x > t_{epi}$:

$$E(x) = 0 \tag{3.8}$$

The calculated electric field distribution at $V_{PN} = -156$ V is shown in fig. 3.7.This calculation is relying on the assumptions made in Chapter 1, where no edge effects are considered. This is however not the case and a significant peak electric field is expected at the edge of the contact, especially in corners which promote the electric field crowding. The exact field at breakdown is then not known, but the maximum value of 5.2 MV/cm calculated in this simple case is a substantial underestimation of the real value. This is in good agreement with the expected breakdown field of 10 MV/cm for this doping level, as edge effects are notorious to cause a severe reduction of the breakdown voltage, particularly in a punch-through configuration. Reaching such a high electric field in this simple architecture, devoid of edge terminations, is encouraging to demonstrate the diamond capabilities. As a reminder, the critical fields of 4H-SiC and GaN are 1 to 4 MV/cm and 2 to 4 MV/cm respectively, lower than the underestimation obtained in this work. This is also among the highest values reported in diamond. As a comparison, a field of 6.2 MV/cm was reported by Iwasaki et al. in a JFET [16] using lateral growth, with a one sided PN junction and a low doped p-type region of 10^{17} cm^{-3}. Elevated values were also reported in p-i-n diodes, 3.9 MV/cm and 1.25 MV/cm by Dutta et al. in [20, 110] and 2.3 MV/cm by Suzuki et al. in [111]. Also, the typical reported breakdown fields in FET devices are in the range of 1 to 3 MV/cm.

3.5 JFET transistor characteristic

To further study the modulation of the PN junction SCR, an impedance analysis is not possible due to the very high substrate resistance (the effect of the serial resistance is discussed in the next section). Instead, the substrate has been used as a n-type gate to operate a JFET whose structure and room temperature transistor characteristic are shown in fig. 3.8. It consists of two ohmic contacts with a 10 μm gap on the p-type layer and a back contact made with silver paste on the back side of the substrate. A clear transistor effect is observed, exhibiting the characteristic ohmic regime at low drain bias and a saturation of the current at higher drain bias due to the pinch-off of the channel (see chapter 5 for further explanations on the transistor characteristic). This shows that the SCR created by the optical activation of the gate substrate behaves accordingly to a PN junction, and can effectively be used to create an optically activated JFET device, as no drain-source current modulation is observed in dark condition.

To measure more quantitatively how the substrate bias affects the drain to source resistance, a JFET IV characterization of the drain to source current as function of the substrate

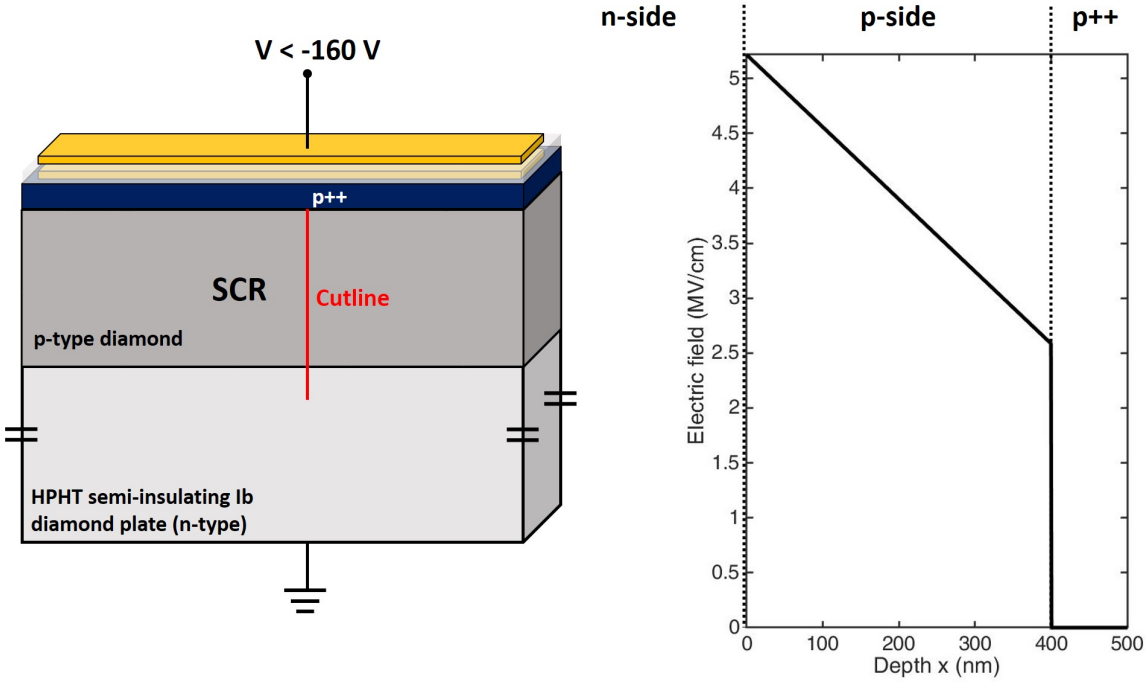


FIGURE 3.7: Schematic representation of the sample measured at high reverse bias and calculated 1D electric field profile along the cutline, for a voltage drop on the junction of $V_{PN} = -156$ V. The maximum electric field is 5.2 MV/cm.

bias has been performed as shown in fig. 3.9. A small constant bias of $V_{DS} = -1$ V between the drain and source contacts is fixed and the drain to source current is measured as function of the substrate bias V_{Sub}. V_{DS} is considered sufficiently small so that $V_{DS} << V_{Sub}$ and $W_{SCR,PN}$ is uniform in the p-type layer. The measurement is performed at 300 °C with a light irradiance of 11 mW/cm^2 and V_{Sub} is swept from -50V to +100V with a measurement time of 500s, fig. 3.9 shows the obtained transfer characteristic. The drain-source current I_{DS} is dependent on the effective thickness of the p-type layer $t_{ch} = t_{epi} - W_{SCR,PN}$, for $V_{DS} = -1$ it can be expressed as:

$$I_{DS}(V_{DS} = -1V) = -\frac{W(t_{epi} - W_{SCR,PN})}{\rho L} \tag{3.9}$$

Assuming that the current saturates at negative V_{Sub} when $W_{SCR,PN} = 0$ nm, to a value I_{max}, then the SCR extension is given by:

$$W_{SCR,PN} = t_{epi}(1 - \frac{I}{I_{max}}) \tag{3.10}$$

The p-layer thickness t_{epi} is estimated at 400 nm, but as it will be demonstrated in the next section, an uncontrolled surface potential causes the presence of a parasitic depletion layer of around 50 to 100 nm. To give an estimation of $W_{SCR,PN}$ and check the pertinence of the PN diode model applied to this original structure, an approximate value $t_{epi} = 350$ nm

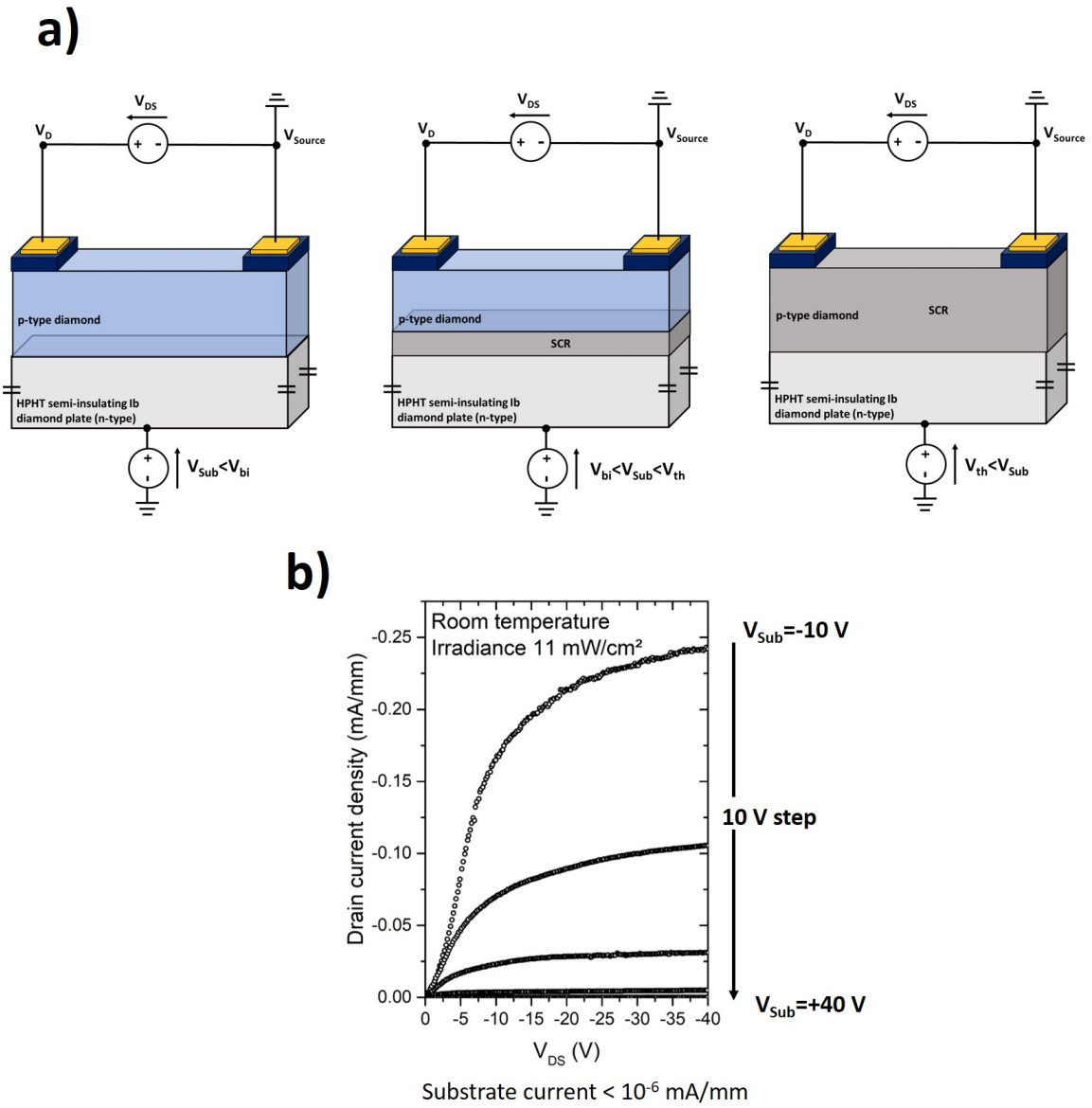


FIGURE 3.8: a) Schematic cross section of the measured structure under different bias voltage, the SCR extension is represented. b) JFET transistor characteristic at room temperature under white light irradiance of 11 mW/cm^2. The drain and source top contacts are separated by 10 μm and the substrate is used as the gate. A clear transistor effect is observed.

reduced by surface effects has been used. According to equ. 3.10, $W_{SCR,PN}$ has a square-root dependence as function of V_{Sub}, and the plot of $W^2_{SCR,PN}$ is linear for reverse biases with a doping level dependent slope.

$$W^2_{SCR,PN} = \frac{2\epsilon_0 \epsilon_{SC}}{qN_A}(V_{Sub} - V_{bi}) \tag{3.11}$$

The obtained $W_{SCR,PN}$ and $W^2_{SCR,PN}$ as function of the substrate voltage V_{Sub} characteristics are shown in fig. 3.10. The linear dependence of $W^2_{SCR,PN}$ as function of the bias is clearly

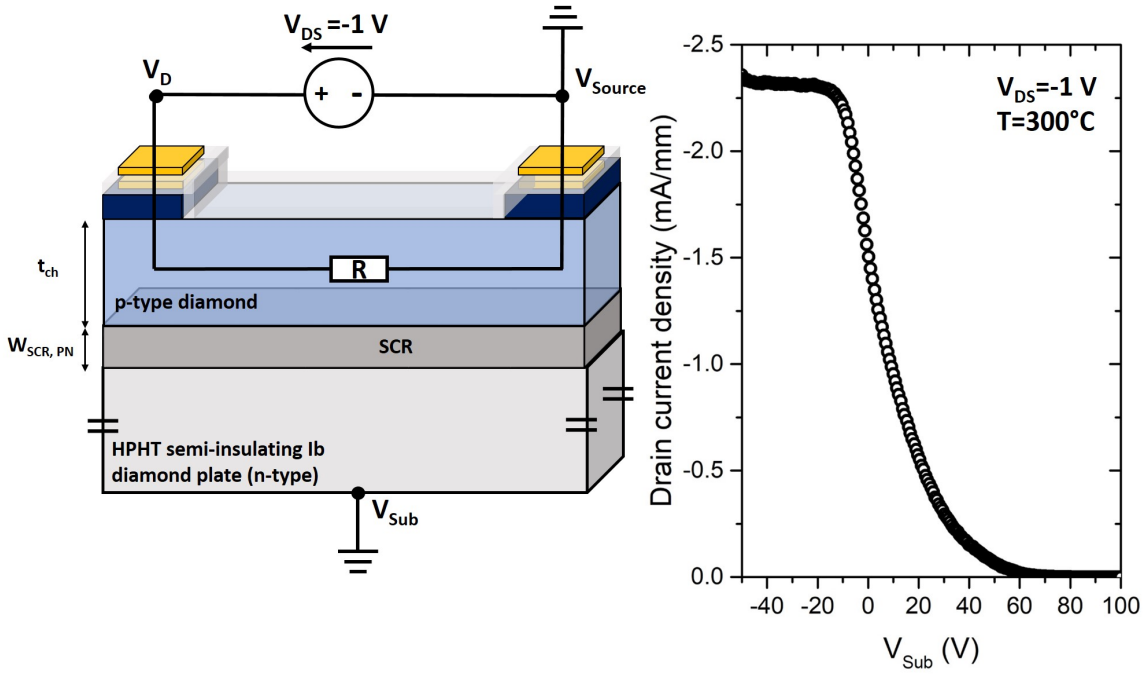


FIGURE 3.9: At left, schematic cross section of the structure. The current is measured between the top ohmic contacts at a fixed bias V_{DS} and t_{eff} is modulated by applying a voltage V_{Sub} between the substrate and the source. At right, the measured transfer characteristics measured at 300 °C under light exposure (11 mW/cm^2), to maximize the number of free carriers generated, with $V_{DS} = -1$ V. The total measurement time is 500 s, high enough for the measurement to be considered quasi-static despite the large substrate resistance inducing a parasitic RC constant.

evidenced in reverse regime, with an extracted doping level of $N_A = 2.2 \times 10^{17}$ cm^{-3} and built-in voltage $V_{bi} = -5.6$ V, compared to the expected value of $N_A = 2 \times 10^{17}$ cm^{-3} from growth conditions and $V_{bi} = -3.9$ V from calculations. Given the approximations made, the agreement between experimental and predicted values is relatively good. The 0 V value of $W_{SCR,PN}$ is extracted around 125 nm, which is a significant fraction of the total layer thickness.

It confirms that the MOSFET conductivity is seriously affected by the back PN junction and can leads to significant deviation of its characteristics if not taken into consideration.

3.6 Summary of the substrate characterization

The effect of the semi-insulating nitrogen doped diamond substrate on the top conducting p-type layer has been evidenced, exhibiting a PN diode behaviour. From IV characterization as function of temperature, the nitrogen ionization energy of 1.45 eV has been extracted, lower than the commonly reported values around 1.7 eV. Carrier concentrations have been estimated to less than 1 cm^{-3} at room temperature, making the junction insulating and unable to react to any applied bias, to 10^{10} cm^{-3} at 300 °C. A visible light excitation with irradiance of 11 mW/cm^2 was found to generate a free electron density

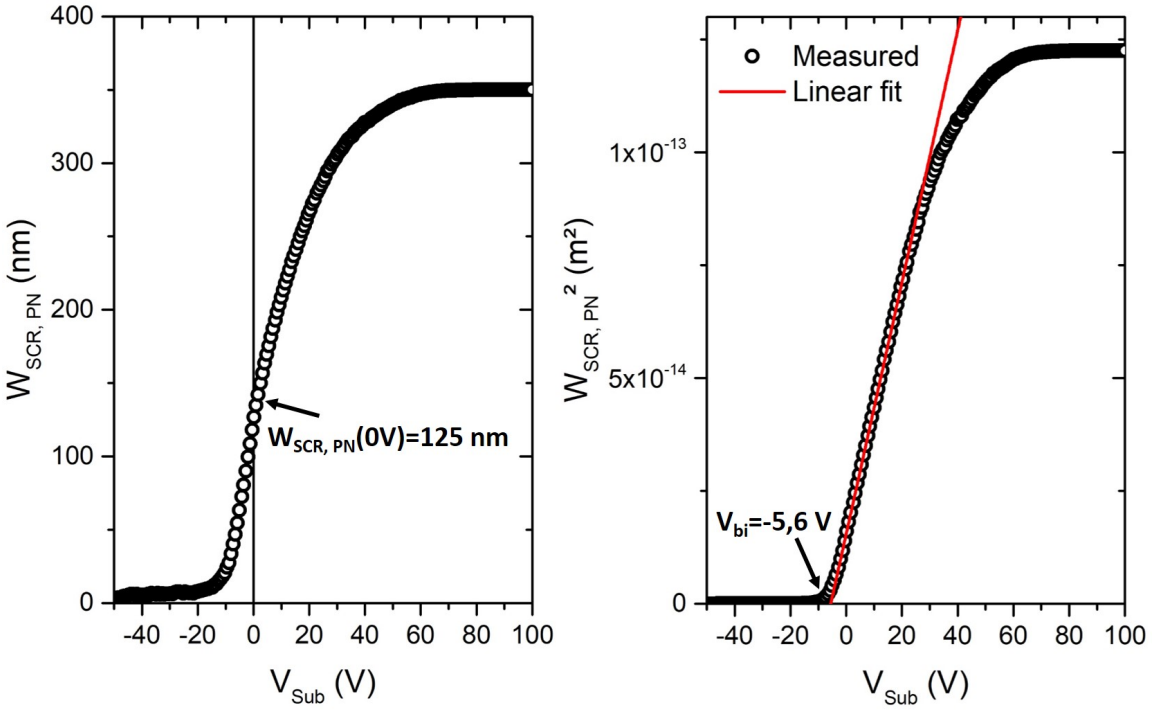


FIGURE 3.10: Extracted $W_{SCR,PN}$ and $W^2_{SCR,PN}$ as function of the substrate voltage V_{Sub} considering a p-layer thickness $t_{ch} = 350$ nm using equ.3.10. The linear fit of $W^2_{SCR,PN}(V_{Sub})$ yields a doping level of $N_A = 2.2 \times 10^{17}$ cm^{-3} and a built-in voltage $V_{bi} = -5.6$ V.

of the order of 10^8 cm^{-3} by the extrinsic photoelectric mechanism, as visible light is well adapted to ionize nitrogen donors in the substrate. Under a light exposure of 11 mW/cm^2, the breakdown voltage drop on the diode was measured to be -144 V, yielding an estimated breakdown field of 5.2 MV/cm, falling in the range of values reported in diamond junctions [77]. This is however an underestimation of the true value due to the calculation not taking into account edge effects, the expected breakdown field is 10 MV/cm. Since the modulation of the SCR as function of the substrate bias can not be obtained by capacitance-voltage characterization, due to the large substrate resistance, it has been deduced from a transfer characteristic. Thanks to a JFET-like configuration, it has been confirmed that the modulation of the SCR behaves closely to the expected ideal case. This study shows the importance of controlling the substrate polarization at high temperature or under illumination. During the MOSFET operation, the drain-substrate bias difference can modulate the back SCR, causing large disturbances of the IV characteristics.

3.7 Conclusion

The semi-insulating substrate, while insulating at room temperature and in the dark, is proven to behave as a PN diode with the conducting p-type layer at high temperature or under the white light exposure of the microscope. In these conditions, a PN diode IV

characteristic has been obtained, the resistance of the substrate as function of temperature could be obtained from the linear slope of the froward regime of the diode, yielding an activation energy of 1.45 eV, smaller than the commonly reported 1.7 eV value. The forward current was also found to exhibit a linear dependence as function of the light irradiance, with a current below detection limit in the dark at room temperature. This is attributed to an extrinsic photoelectric effect, as the wavelength emitted by the light used is not low enough to generate electron-hole pairs in diamond. Instead, a fraction of the nitrogen donors in the substrate are ionized by the incident light. Even for relatively low values of irradiance, up to 11 mW/cm^2, this effect is clearly observed. From the reverse regime, the breakdown value of the junction has been extracted at -144 V and the maximum electric field was estimated at 5.2 MV/cm by a 1D model. It most likely greatly underestimates the real peak electric field value, due to the expected presence of an electric field crowding effect, not taken into account, at the edges of the contacts. This measure is then coherent with the expected breakdown field of 11 MV/cm which would ideally give a breakdown voltage of -390 V, much higher than other commonly used wide band gap materials such as GaN and SiC. Additionally, by using two top contacts on the p-layer, a JFET-like transfer characteristic has demonstrated that the SCR is indeed modulated by a back contact substrate bias, with its extension being located almost only in the p-type layer due to the higher doping of the substrate, $N_D \approx 10^{19}$ cm^{-3}.

Thanks to the understanding of the effects of the substrate and the oxide, the MOSFETs and TLM contacts can be characterized and analysed by controlling the experimental conditions.

Chapter 4

Diamond, oxide and their interfaces electrical characterization

This chapter will address the parasitic charging effect occurring at the Al_2O_3/diamond interface, by means of impedance measurements, with a special care on their proper interpretation. The detrimental effect of the interface traps will be quantified and their dynamic discussed, leading to a discussion on previous reports of our group.

The choice of the oxide is important for the device performances. The top valence band offset with O-terminated diamond has to be large enough to avoid charge injection effects. It has been shown that alumina is suitable for high performance diamond devices [101] in addition to be an easily available high-k oxide as ALD of alumina is a standard process in micro and opto-electronics. Other oxides in bi-layers or monolayers have been intensively studied [112, 113, 114, 115, 116], but these works make use of H-terminated diamond with a different band alignment than with O-terminated diamond, due to their different electron affinities. In the framework of this study no optimization of the oxide have been conducted, the deposition process makes use of the work published by T. T. Pham et al. [88], greatly reducing the gate leakage current.

The present main problematic is the interface quality between the semiconductor and the oxide, which is known to be at the origin of a large density of traps estimated in the order of $10^{12} - 10^{13}$ $cm^{-2}.eV^{-1}$ in O-terminated MOSCap [89, 88, 117, 118]. This prevents the proper charge modulation in the MOS structure because an additional bias dependent parasitic charge is introduced. This issue is particularly difficult to manage in the case of a deposited oxide. Diamond having no native oxide, like SiO_2 with Si, an oxide formation by surface oxidation is not possible. The surface passivation treatment and the oxide deposition process are then critical and challenging to optimize.

At first, the oxide layer and the p-type epilayer will be characterized by an impedance analysis. Their relevant properties in terms of their impact on the device operation, such as the oxide dielectric constant, the epilayer effective doping level and the leakage current of the MOS stack, will be extracted. For this purpose it is necessary to introduce the Capacitance-voltage (CV) and Capacitance-frequency (Cf) characterizations, and the proper method to interpret the measurements by correcting by parasitic effects. Then charging effects will be analysed and compared with literature, with comments about published results in light of the discussion developed in this section.

4.1 Characterization of the oxide and epilayer by impedance analysis

4.1.1 Properties of Al_2O_3 deposited by ALD: relative dielectric constant

CV and Cf measurements are widely used techniques to characterize MOS stacks due to the amount of informations they can provide with a relatively light measurement setup. To measure the impedance, a small AC bias of amplitude $V_{AC} = 30$ mV and frequency f is superimposed to a quasi-static DC input bias. A Modulab XM MTS was used, able to probe at frequencies below 1 Hz up to 1 MHz and at DC voltages up to 100 V. The software is converting the measured impedance to capacitance using a parallel RC equivalent circuit. Considering a circuit of impedance $Z = Z' + jZ''$, the equivalent parallel capacitance C_P and conductance G_P are:

$$C_P = \frac{Z''}{Z'^2 + Z''^2}\frac{1}{\omega} \tag{4.1}$$

Where $\omega = 2\pi f$.

$$G_P = \frac{Z'}{Z'^2 + Z''^2} \tag{4.2}$$

The oxide capacitance C_{OX} is an important parameter, accurate knowledge of its value is necessary to isolate its contribution to the total measured capacitance C. These devices are expected to exhibit large alterations of their CV due to interface states, making the extraction of C_{OX} from the CV signal of the MOSCap challenging. In such case, the fabrication of MIMCaps structures is a necessary precaution to reliably measure C_{OX} and additionally extract the relative dielectric constant of the oxide $\epsilon_{Al_2O_3}$ using:

$$C_{OX} = \frac{\epsilon_0 \epsilon_{Al_2O_3} S}{t_{OX}} \tag{4.3}$$

Where S is the surface of the metallic gate contact on the oxide ($S = 3 \times 10^{-5}$ cm^{-2} for the designed MIMCaps) and $t_{OX} = 50$ nm is the alumina layer thickness, determined from an ellipsometry measurement performed on a silicon substrate on which the same oxide deposition was performed.

Thanks to the MIMCaps structures, the relative dielectric constant of the alumina layer was extracted from the CV characteristics shown in fig. 4.1 to be $\epsilon_{Al_2O_3} = 8.8 \pm 0.2$. This is comparable to already reported values in previous studies for high temperature alumina deposition by ALD. A small linear increase of the capacitance is however observed as function of the bias, possibly due to charging effects occurring during the measurement. This leads to an acceptable 1% error over a 10 V bias difference, that was not considered in the following study.

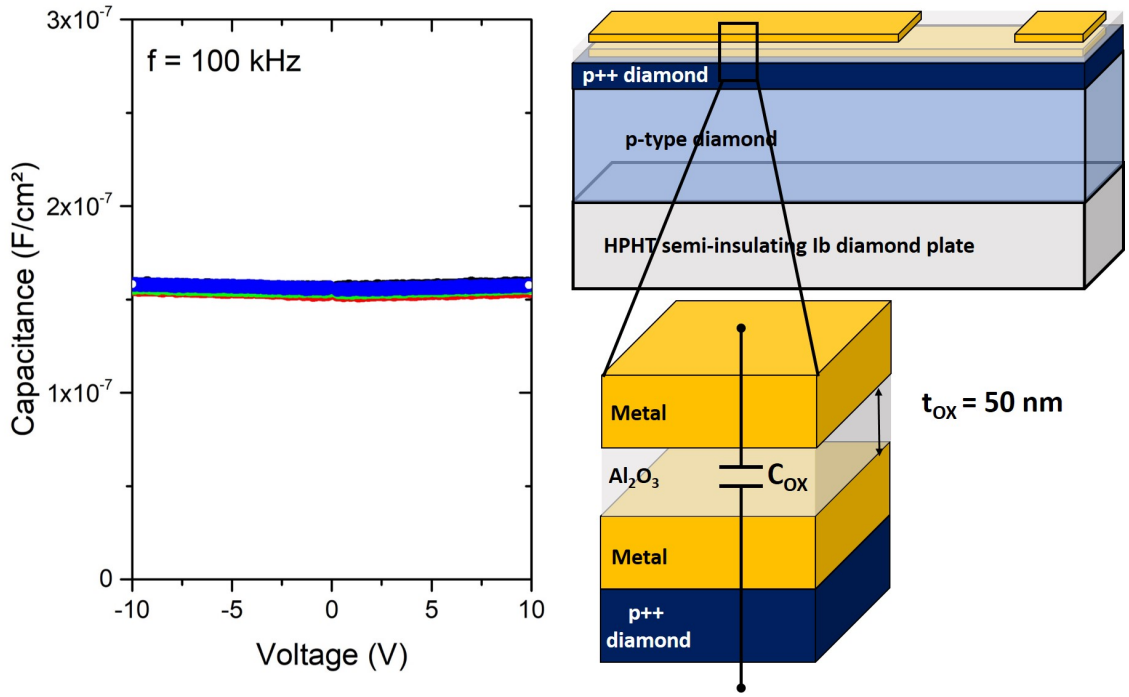


FIGURE 4.1: CV characteristic between -10 V and +10 V at 100 kHz performed on 4 circular MIMCaps of radius 30 μm. The oxide relative dielectric constant is extracted to be 8.8±0.2.

4.1.2 Experimental epilayer impedance analysis

The ideal MOSCap CV characteristic

The equivalent circuit and detailed structure of an ideal MOSCap is shown in fig. 4.2, the oxide capacitance C_{OX} and the bias dependent SCR capacitance C_{SCR} are in series. The total capacitance C using the parallel RC equivalent circuit used by the Modulab capacitance meter, shown in fig. 4.3, is then:

$$C(V) = C_P(V) = \frac{C_{OX}C_{SCR}(V)}{C_{OX} + C_{SCR}(V)} \tag{4.4}$$

One can refer to the charge equilibrium equation of chapter 1 to calculate $C_{SCR}(V)$ using:

$$C_{SCR}(V) = \left|\frac{dQ_{SCR}}{dV_G}\right| = \frac{\epsilon_0\epsilon_{Diam}S}{W_{SCR}(V)} \tag{4.5}$$

(i) In accumulation for $V_G < V_{FB}$, W_{SCR} is thin as the hole accumulation layer extend only over a thickness of a few Debye lengths, so that $C_{OX} << C_{SCR}$ and equ. 4.4 is reduced to $C \approx C_{OX}$.

(ii) In depletion and deep depletion W_{SCR} extends with a square-root dependence as function of the gate bias so that the approximation $C_{OX} << C_{SCR}$ is not applicable anymore. Assuming that the effective doping level $N_A - N_D$ is uniform, the plot of $\frac{1}{C^2} - \frac{1}{C_{OX}^2}$, commonly referred as Mott-Schottky plot, yields a linear dependence as function of V_G

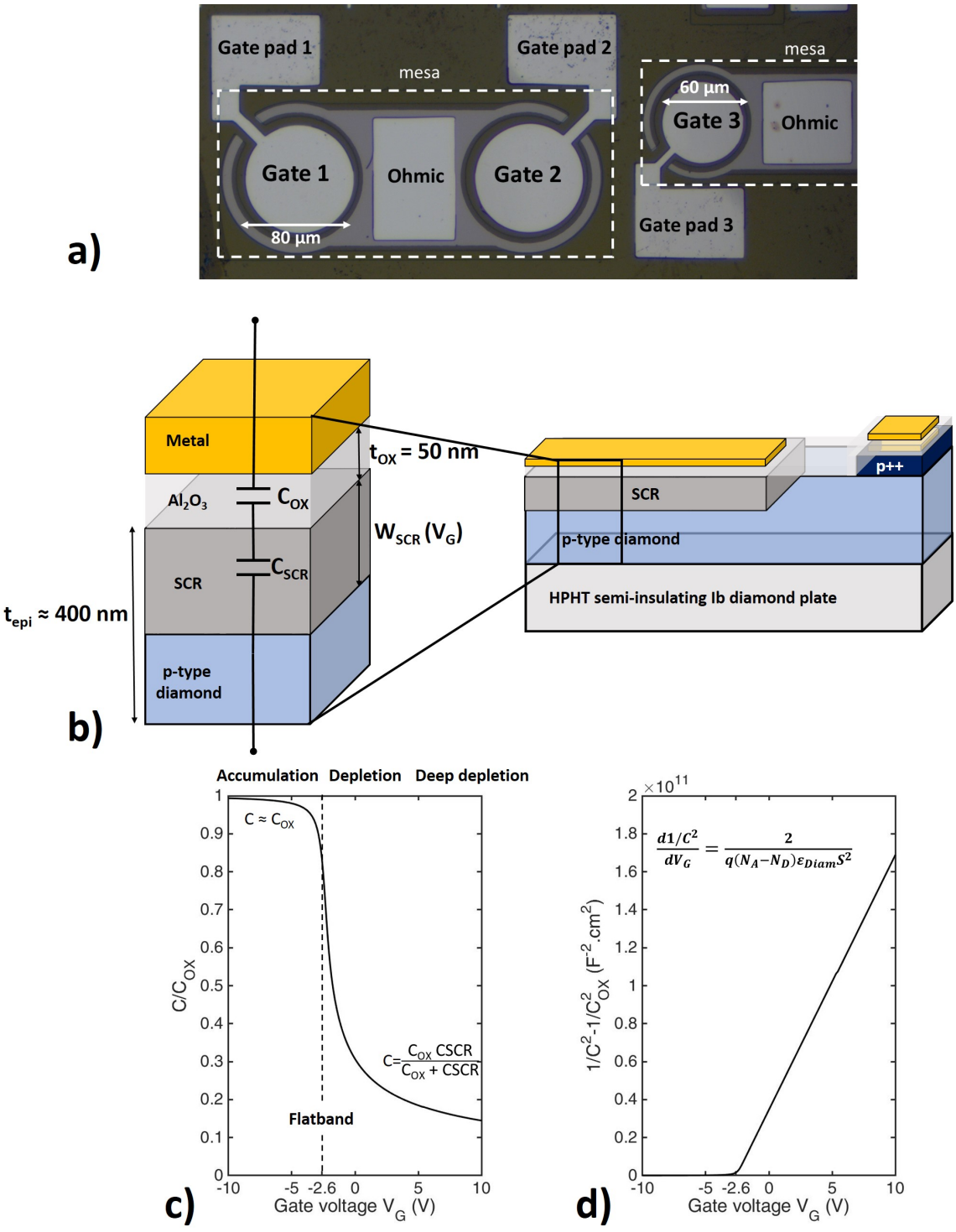


FIGURE 4.2: a) Optical top view of the measured MOSCap structure and b) its schematic cross section. c) Calculated ideal CV characteristic at RT with $t_{OX} = 50$ nm and $N_A - N_D = 2 \times 10^{17}$ cm^{-3}. d) Calculated $1/C^2 - 1/C_{OX}^2$ plot, the slope of the linear curve is effective doping level $N_A - N_D$ dependent.

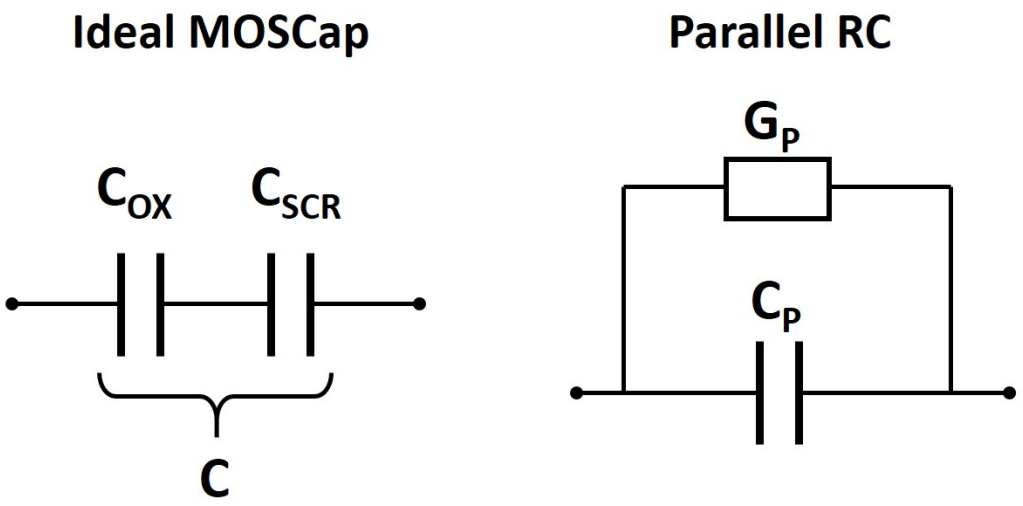


FIGURE 4.3: Equivalent circuit of an ideal MOSCap and the parallel RC circuit used by the Modulab software.

in depletion, of which the slope is proportional to $N_A - N_D$ and crosses the x-axis at the flatband voltage:

$$N_A - N_D = \frac{2}{q\frac{d1/C^2}{dV_G}\epsilon_0\epsilon_{Diam}S^2} \tag{4.6}$$

16 MOSCaps were fabricated on the sample MOS8 with a typical CV measured on a 60 μm diameter MOSCap plotted in fig. 4.4, exhibiting a large difference with the ideal calculated curve.

(i) The flatband voltage is shifted, to $V_{FB} = +5$ V from the ideal one at $V_{FB} = -2.6$ V. This effect is usually attributed to fixed bulk oxide charges in literature, but as we'll see later, the presence of a large hysteresis effect on the CV and the shift of V_{FB} after successive measurements can be assigned to slow traps, either in the bulk of the oxide or at the diamond/oxide interface, with typical time constant reaching minutes or hours.

(ii) Considerable stretch-out of the CV are observed, exhibiting the so called Fermi level pinning in the bias range $V_G = -10$ V to $V_G = +10$ V where the capacitance signal is almost insensitive to the gate bias. This is characteristic of the presence of a large density of traps located near or at the diamond/oxide interface, in the band gap of diamond, that cause parasitic charging effects as already observed in ref.[89, 88, 117, 118]. This issue is crippling the performances of MOSFETs, which requires a fast and efficient control of the SCR.

(iii) Other well known parasitic effects, such as a high serial resistance and the presence of an oxide leakage current, have to be analysed and corrected if necessary in the first place to correctly interpret the features of the CV. Understanding their effect is a prerequisite to perform a proper CV measurement.

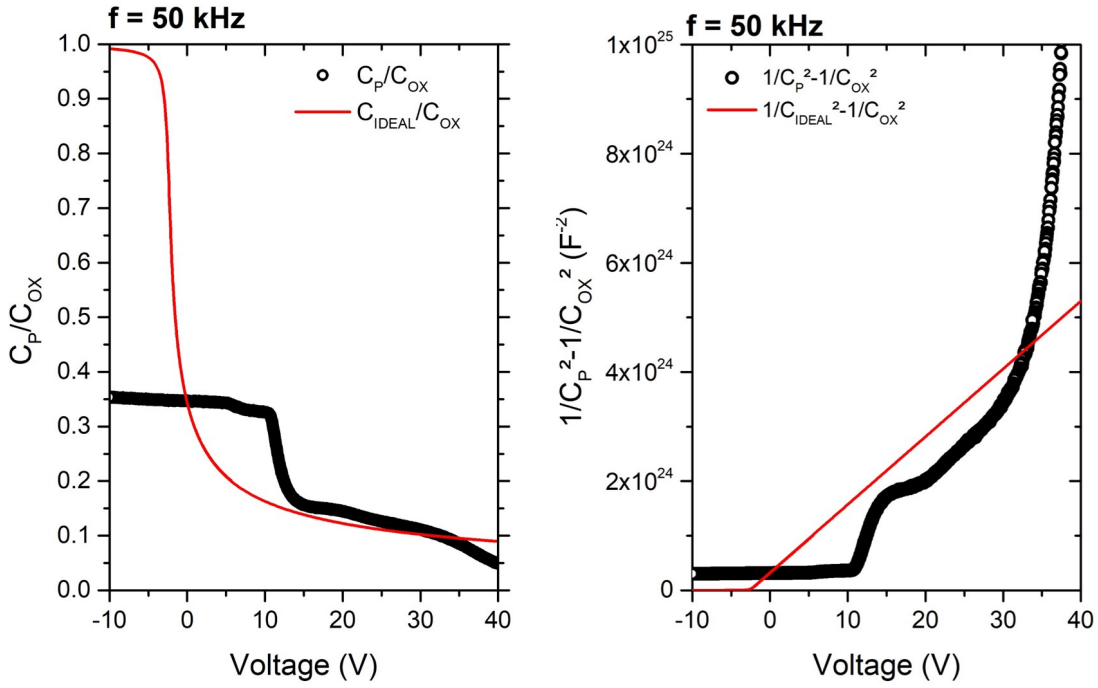


FIGURE 4.4: CV and Mott-Schottky plot compared with the ideal CV, the best fit was obtained with a doping level of $N_A - N_D = 2.3 \times 10^{17}$ cm^{-3}. The experimental flat band voltage is $V_{FB} = +5$ V. The measurement was performed at room temperature with $V_{AC} = 30$ mV, $f = 50$ kHz and by biasing from +40 V to -10 V.

Correction of the experimental data by the serial resistance and leakage current

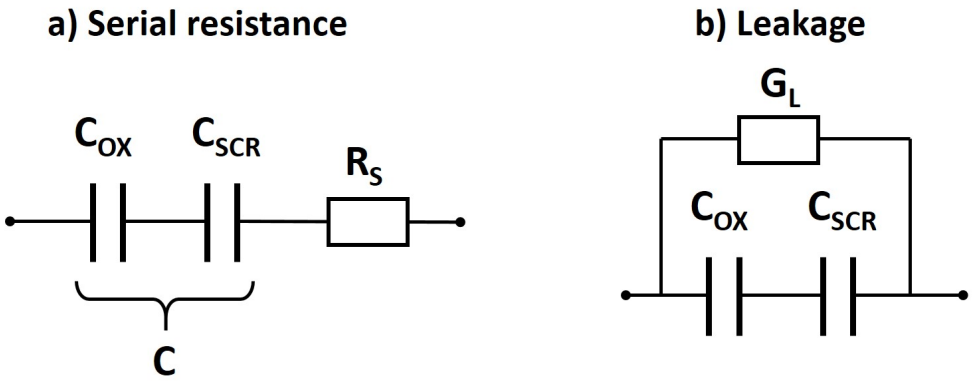


FIGURE 4.5: Equivalent circuit in presence of a) a serial resistance and b) leakage current.

When characterizing a MOSCap, one has to be cautious on the effect of the serial resistance R_S, as it can alter the CV and Cf response of the sample. The equivalent circuit of the MOSCap is modified to the one shown at left in fig. 4.5 a), equivalent to a RC series circuit,

which is a high-pass filter. The expression of the parallel capacitance C_P and conductance G_P are then given by:

$$C_P = \frac{C}{1 + (\omega R_S C)^2} \tag{4.7}$$

$$G_P = \frac{R_S C^2 \omega^2}{1 + (\omega R_S C)^2} \tag{4.8}$$

And R_S is estimated by[119]:

$$R_S = \frac{G_P}{G_P^2 + \omega^2 C_P^2} \tag{4.9}$$

Where $(\omega R_S C)^2$ is not negligible compared to 1, the measured capacitance C_P can be significantly lower than the true capacitance C. In that case it is necessary to lower the frequency measurement to met the condition $(\omega R_S C)^2 << 1$, limiting the frequency range than can be probed. In a vertical design, it is generally considered that R_S is a constant independent of the gate bias, determined from the measured C_P and G_P in accumulation regime to avoid parasitic effects from interface states [119]. However, in a lateral design with an insulating material as substrate, R_S is dependent on the effective channel thickness t_{ch} of the conducting semiconductor material. When biasing the MOSCap in depletion the SCR extends, W_{SCR} is increased and t_{ch} is then reduced, eventually leading to a large R_S causing a considerable distortion of the CV characteristic.

It's even more problematic since it has been shown that there exists a junction between the substrate and the epilayer, reducing t_{ch}. The fig. 4.6 compares a room temperature MOSCap CV and Mott-Schottky characteristics under white light optical excitation, with the substrate grounded or biased at -100 V. In both case, the drop of the measured capacitance can be observed at positive bias. However, without biasing the substrate, the CV is not significantly affected by R_S only up to a +10 V gate bias, compared to +30 V in the case where a -100 V substrate bias is applied, for a frequency of 10 kHz. Consequently measurements were done using a substrate bias of -100 V under white light exposure.

An other common parasitic effect that can be particularly impairing for the study of MOSCaps is the leakage current through the oxide, modelled as a conductance G_L in parallel of the capacitance C. T. T. Pham et al. proposed in ref.[117] that a variable range hopping mechanism in the oxide explains the observed IV characteristics. In the simple case of the equivalent parallel RC circuit of fig 4.5, the measured conductance G_P is directly equal to G_L and the capacitance measured is not affected by the leakage. However, in case of a large gate oxide current so that the resistive part of the device is much larger than the capacitive part, $G_P >> \omega C_P$, the measurement of C_P becomes inefficient and cannot be exploited anymore, it is then necessary to increase the measurement frequency. The leakage induced capacitance overestimation has been a source of misinterpretation in previous works on O-terminated p-type MOSCaps [86, 87] which concluded on the observation of the accumulation regime whereas it was clear that $G_P >> \omega C_P$, as discussed in ref.[117].

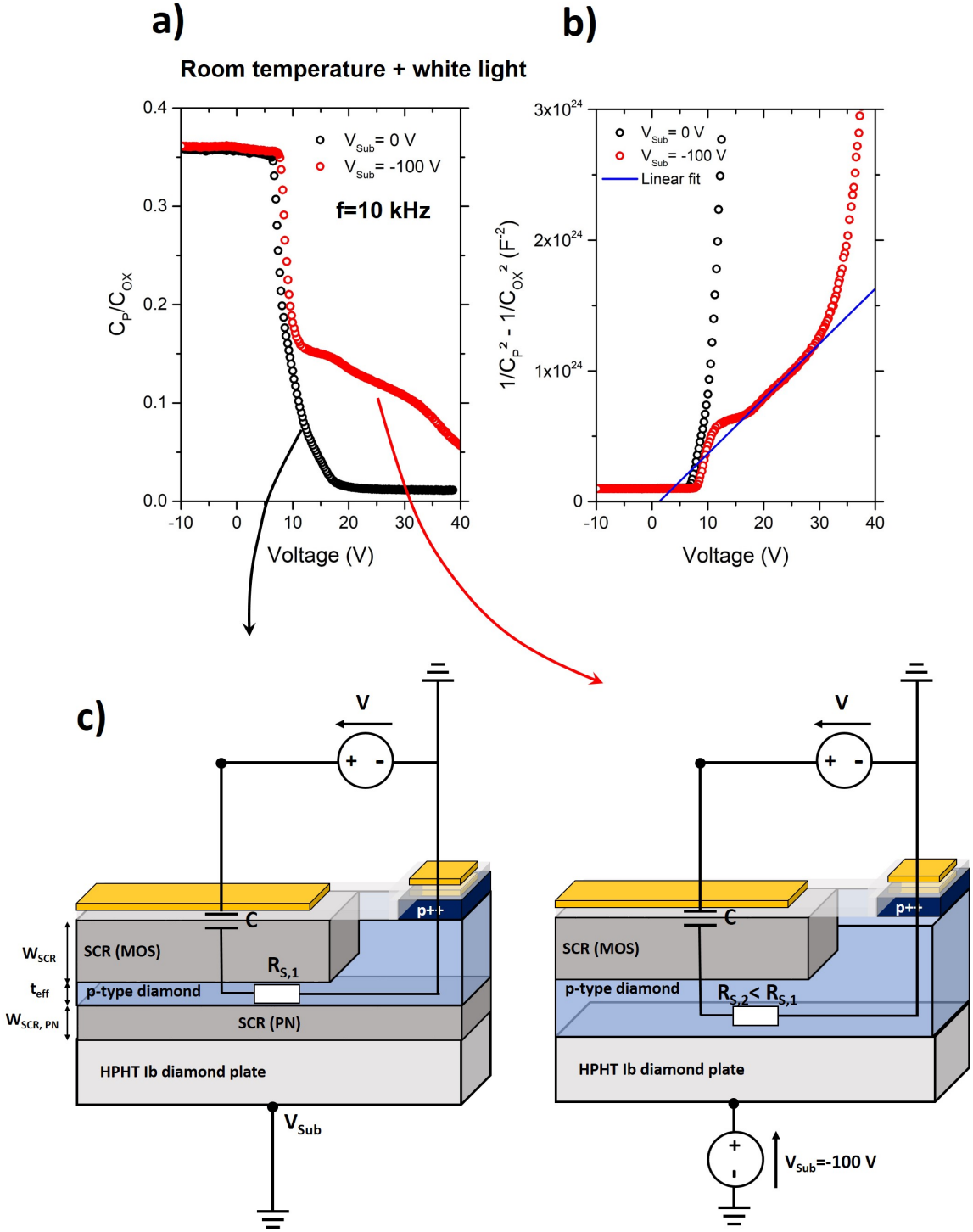


FIGURE 4.6: At left, room temperature under white light optical excitation CV characteristic of a circular MOSCap of radius 40 μm. C_P/C_{OX} is plotted with black dots when V_{Sub} is grounded and with red dots when a bias $V_{Sub} = -100$ V is applied. At right, the Mott-Schottky plot is shown where the linear dependence in depletion is observed when $V_{Sub} = -100$ V is applied. The effective doping level extracted from the linear fit is $N_A - N_D = 2.2 \times 10^{17}$ cm^{-3}, in agreement with the doping level extracted previously.

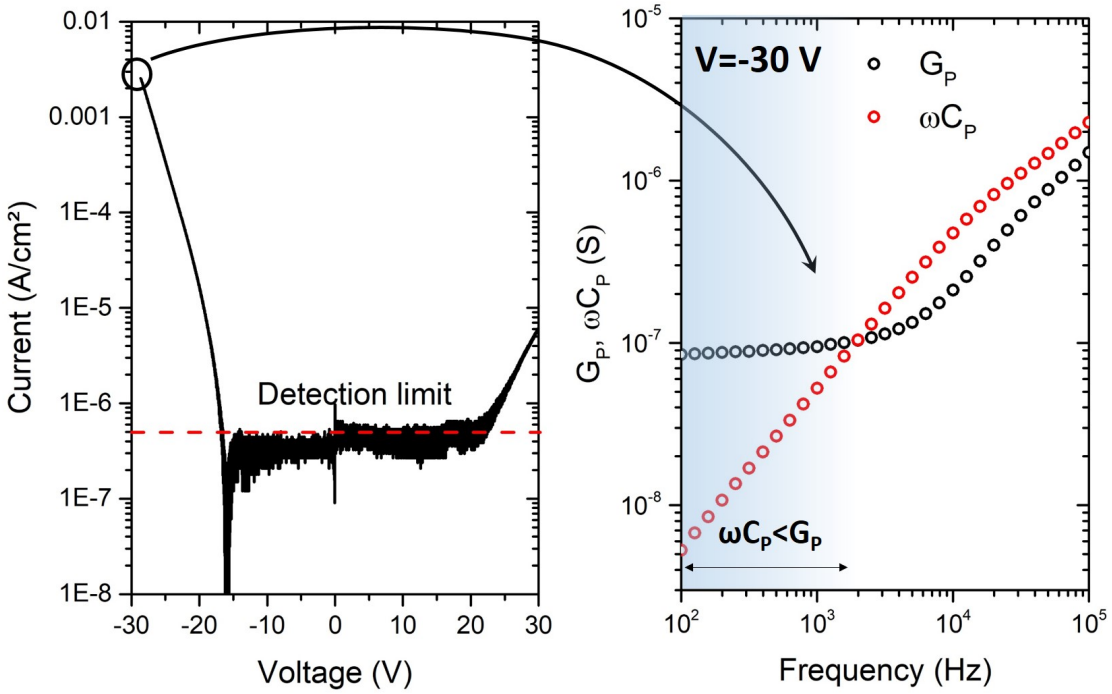


FIGURE 4.7: At left, static IV characteristic of a MOSCap of radius 40 μm. At right, its Cf characteristic at $V_G = -30$ V, ωC_P is plotted with black dots and G_P with red dots. At low frequency the condition $G_P \leq \omega C_P$ is not met, $G_P = 10\omega C_P$ at 200 Hz.

Compared to these previous studies, the post annealing and higher oxide temperature deposition reduced considerably the parasitic leakage current [88] so that a wider gate bias range can be probed. A static IV characteristic between $V_G = -30$ V and +30 V is shown in fig. 4.7, with the extracted G_P and ωC_P at $V_G = -30$ V where the leakage is maximum in the measured bias range. It is shown that for a leakage current of 1.5×10^{-3} A/cm^2 the condition where $G_P >> \omega C_P$ occurs at relatively low frequency, typically $G_P = 10\omega C_P$ at $f = 200$ Hz. Any higher measurement frequency is valid in regard of the leakage current, this highlight the quality of the oxide layer which is able to withstand a high electric field with a moderate leakage current. The electric field in the oxide E_{OX} is estimated at $E_{OX} = 5.8$ MV/cm for $V_G = -30$ V, without considering 2D effects. A lower gate bias value would results in the destructive breakdown of the MOSCap.

Effective doping level $N_A - N_D$ of the drift and channel layer of the D3MOSFET

The doping level is an important parameter as it influences the device on state resistance, blocking voltage and threshold voltage. Dispersion has been measured by CV characteristics of MOSCaps at different locations of the sample, the effective doping level $N_A - N_D$ can be extracted from the slope of the Mott-Schottky plot. However, the study of the doping level dispersion on the sample has been limited by the weak adherence of the titanium gate metal layer on the alumina. The gate pads tend to coming off the sample easily when

contacted with probe tips, but 7 MOSCaps out of 16 could be characterized and the measurements have been compiled in fig. 4.8. Doping levels between 1.8×10^{17} cm^{-3} and 2.9×10^{17} cm^{-3} have been obtained with an average value of 2.4×10^{17} cm^{-3}, not far from the targeted 1×10^{17} cm^{-3} value during growth.

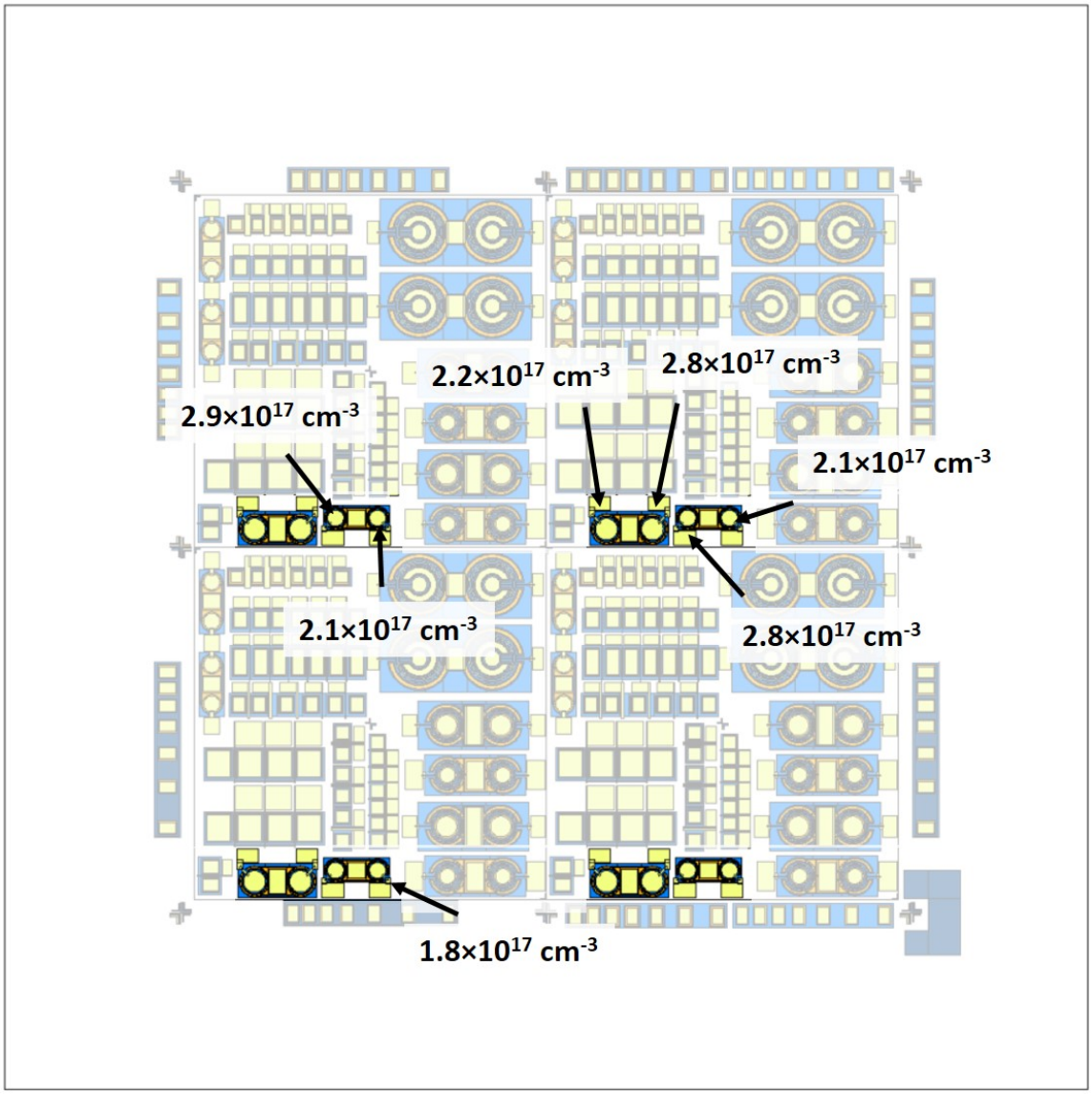


FIGURE 4.8: Extracted effective doping level from the Mott-Schottky plot of the measured MOSCap with their location on the sample.

4.2 Charging effects from interface and bulk traps

4.2.1 Large threshold voltage shift induced by a Capacitance-Voltage hysteresis

By biasing the MOSCap, the flatband voltage can shift significantly due to the ionization of bulk oxide traps and oxide charge trapping. This has been evidenced in ref.[89] using

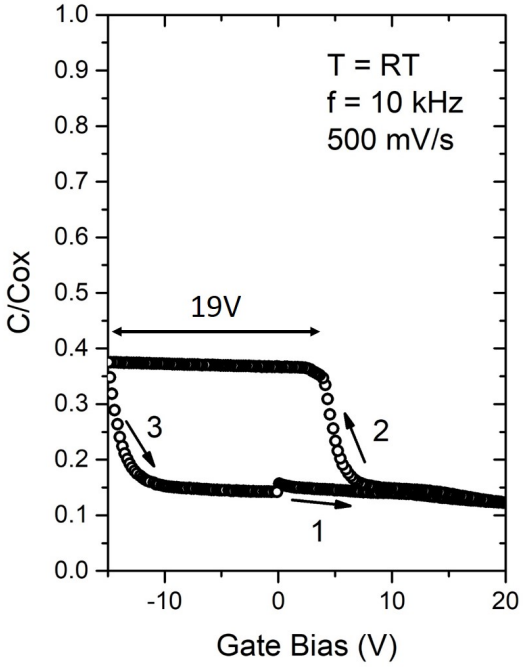


FIGURE 4.9: At left CV hysteresis measurement on a MOSCap with a bias sequence: 0 V to +20 V to -15 V to 0 V, the maximum bias difference between two points of same capacitance value is 19 V. The DC scan rate was set at 500 mV/s with an AC frequency of $f = 10$ kHz.

p-type diamond O-terminated MOSCaps, with a very similar oxide deposition thickness, temperature deposition and post annealing as performed on MOS8 sample. It is concluded that successive measurements shifts the flatband voltage towards the ideal one at -2.6 V, without ever reaching it. The benefit of the oxide annealing process is also evidenced, with a reduction of the charge density. However, this study cannot discriminate between bulk oxide charges and interface charges, with a total effective charge density of around 1×10^{12} cm^{-2} extracted, causing the flatband voltage to shift down to -5.8 V from the ideal value of -2.6 V.

A similar study has not been performed on MOS8, however considerable shifts of flatband voltages and a large hysteresis effect were observed as shown in fig. 4.9, exhibiting a maximum 19 V voltage shift. A maximum total effective charge N_{eff} can be extracted, given by:

$$N_{eff} = \frac{\Delta V C_{OX}}{qS} = 1.85 \times 10^{13} cm^{-2} \tag{4.10}$$

Where $\Delta V = 19$ V is the maximum voltage shift, $C_{OX} = 8.26$ pF and $S = 5.3 \times 10^{-5}$ cm^{-2}.

The hysteresis cycle is similar to the difference observed between the first and second measurement in ref.[89] before annealing, with a voltage shift $\Delta V = 12$ V. A preliminary conclusion is that the first measurement from deep depletion toward accumulation cause emission of carriers from traps, either at the interface or in the bulk of the oxide, building

a charge Q_{it}. The CV from negative bias to deep depletion is then shifted but does not exhibit the Fermi level pinning effect. This would indicate that the dynamic of carrier capture to these traps is slower than the emission dynamic, the measurement time is not long enough to fill the traps and the charge Q_{it} is varying slowly, almost insensitive to V_G. These slow variations of V_{FB} versus time are in agreement with those reported in ref.[89], taking several hours to stabilize.

This hysteresis effect can induce a large threshold voltage shift during the D3MOSFET operation, as well as significant changes of the transistor characteristic depending on the gate bias sweep direction. Reducing this charging effect is of particular importance in view of the device integration, as its characteristics have to be reproducible.

4.2.2 Interface states detrimental effect on the MOS gate modulation

Interface charge definition and dynamic in wide band gap semiconductors

A significant number of defects is present at the oxide/semiconductor interface, from dangling, unsaturated bonds, surface defects or impurities [120]. They induce the presence of discretized states in the band gap of diamond, but are generally described by a continuum of states as they are so closely spaced in energy that they cannot be distinguished in most cases. Then, the interface states density D_{it} is defined as the number of interface trap states per unit area of the interface and per unit energy in the semiconductor band gap ($cm^{-2}.eV^{-1}$). The presence of this density of states introduces an additional charge Q_{it} in the system which is particularly detrimental for the MOSCap modulation, due to its gate bias and frequency dependence. The schematic principle of the filling and emptying process is shown in fig. 4.10.

There exists two types of traps, acceptors and donors, whose energy levels in the band gap are respectively closer to the conduction band and the valence band. Donor interface traps are positive when empty and neutral when filled, acceptor traps are neutral when empty and negative when full. It is not possible experimentally to measure the charge induced by each of those traps separately, instead what is observed is the net interface states charge $Q_{it} = Q_{it}^{Donor} - Q_{it}^{Acceptor}$. It is then useful to define the energy position in the band gap where the density of acceptors is equal to the density of donors, as shown in fig 4.10, referred as Charge Neutrality Level (CNL) where $Q_{it} = 0$. At thermodynamic equilibrium, if the Fermi level is below the CNL, the net charge is positive $Q_{it} > 0$ and if it is above, the net charge is negative $Q_{it} < 0$. The position of the CNL is experimentally observed in silicon devices, as the charge Q_{it} changes sign. However, in wide band gap materials the CNL is located deep in the band gap and reaching thermodynamic equilibrium may take an extremely long time. The interface state emission time constant is generally described by thermal generation of carriers from the valence band [121] to the trap energy level by:

$$\tau_{it} = \frac{1}{\sigma v_{th} N_V} e^{\frac{(E_{it}-E_V)}{k_B T}} \tag{4.11}$$

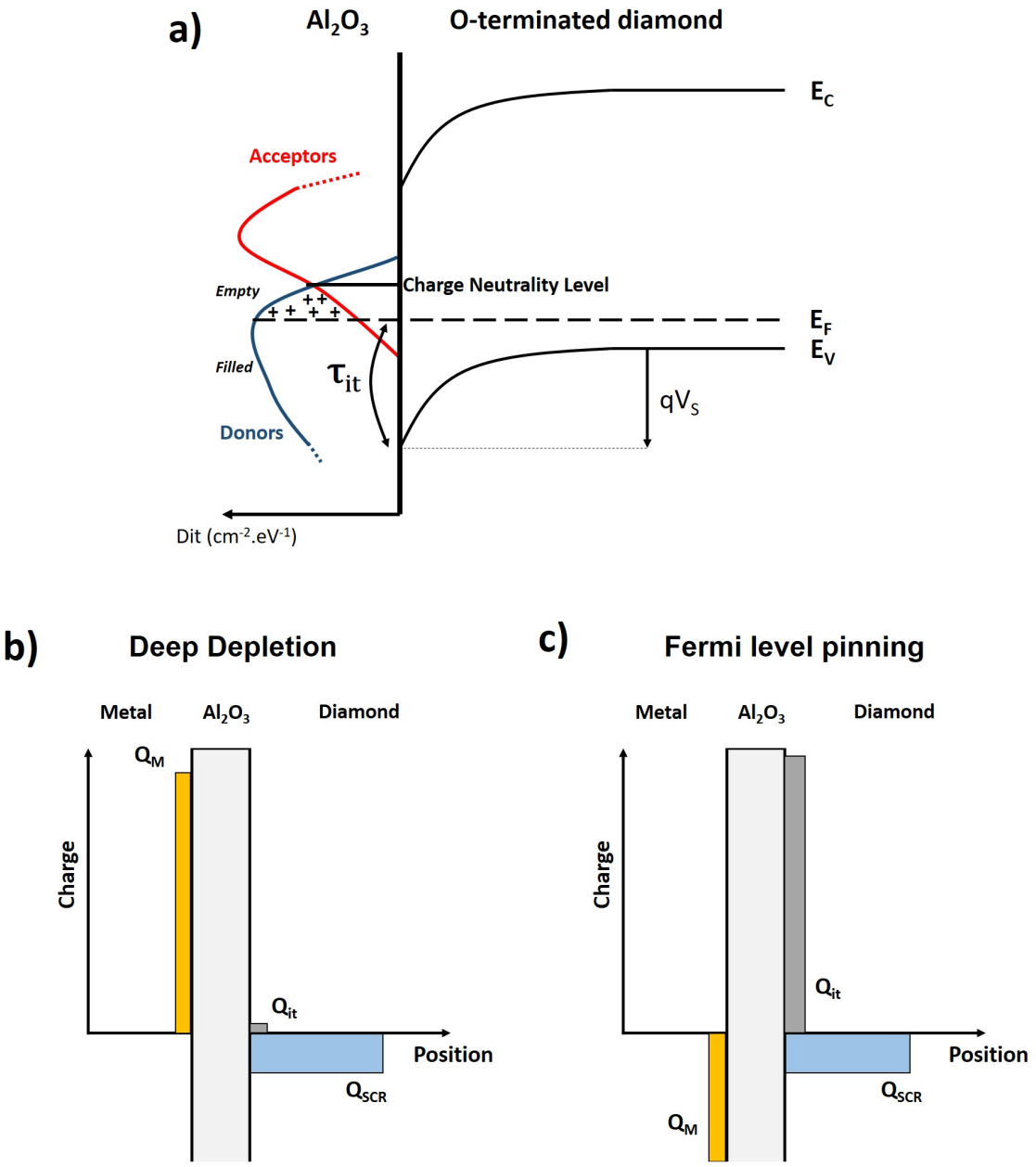


FIGURE 4.10: a) Schematic band diagram with an arbitrary interface state density at the diamond/oxide interface in depletion. On the bottom, schematic distribution of the charges in the metal, interface and diamond space charge region in b) deep depletion, where $\tau_{it} >> \tau_{DC}$ so the charge Q_{it} doesn't have time to build up and c) at the Fermi level pinning, where $\delta Q_{it} >> \delta Q_{SCR}$ so the charge applied on the metal is screened by the interface trap charges.

With σ the hole capture cross section of the trap, typically in the order of 10^{-16} cm^{-2} to 10^{-20} cm^{-2} for donor traps, v_{th} the mean hole thermal velocity[1], N_V the valence band equivalent density and E_{it} the trap energy level.

Due to the exponential dependence of τ_{it} as function of the Fermi level position, represented in fig. 4.11 with a typical capture cross section $\sigma = 10^{-18}$ cm^{-2} for donor states, the frequency response of traps is strongly dependent on the gate bias. This is modelled by the equivalent circuits shown in fig. 4.11 with an additional capacitance C_{it} and resistance R_{it} in parallel on the SCR capacitance. Three cases can be considered depending on the duration of each measurement point τ_{DC} and the period of the AC signal $\tau_{AC} = 1/(2\pi f)$:

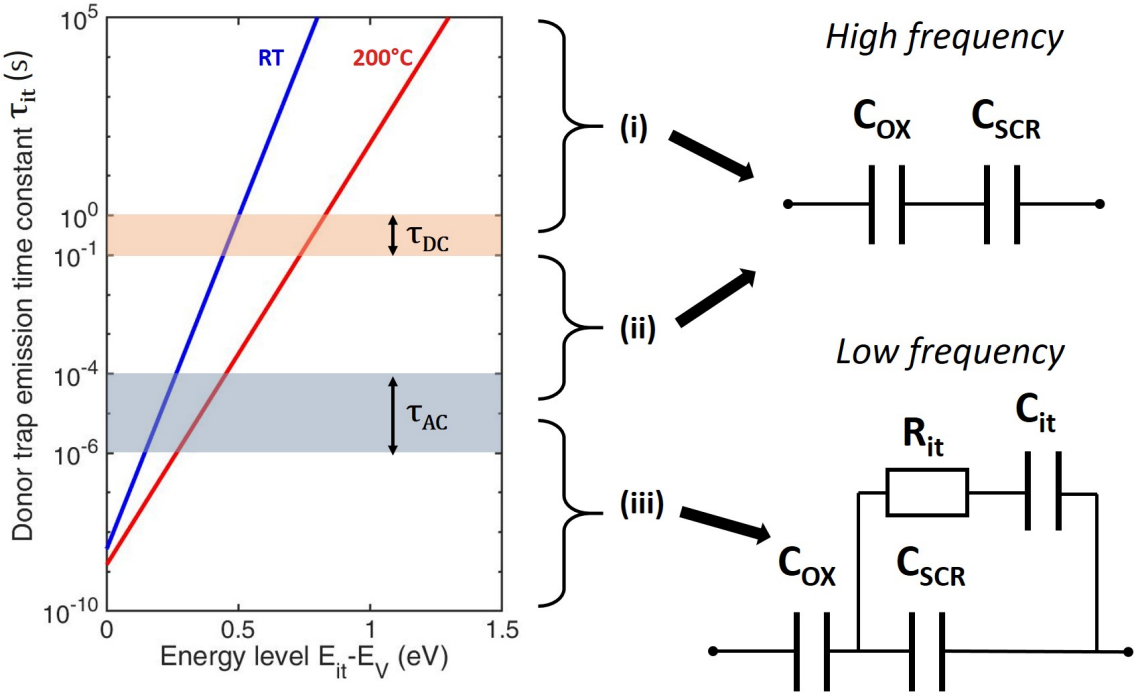


FIGURE 4.11: Calculated τ_{it} from equ. 4.11, with a typical donor state capture cross section $\sigma = 10^{-18}$ cm^{-2}, as function of the position of the trap in the bad gap relative to the valence band. Depending on the value of τ_{it} relatively to τ_{AC} and τ_{DC}, the low frequency equivalent circuit, for $\tau_{it} << \tau_{AC}$ and the high frequency, for $\tau_{AC} << \tau_{it}$ can be used.

(i) For $\tau_{it} >> \tau_{DC} >> \tau_{AC}$, at large positive bias in deep depletion regime, the Fermi level at the interface is deep in the band gap such that the trapping time constant from equ. 4.11 is much larger than the measurement duration τ_{DC}. The state occupancy of these slow traps is bias independent and Q_{it} can be considered constant. The high frequency equivalent circuit of fig. 4.11 is then a good approximation to interpret the CV. This corresponds to the fig. 4.12 for $V_{DC} > +15$ V, where the measured characteristics is in good agreement with the ideal curve.

(ii) For $\tau_{DC} >> \tau_{it} >> \tau_{AC}$, when biased toward flatband, the Fermi level position at the interface is being closer to the valence band. τ_{it} is reduced and the traps are able to

[1] $v_{th} = \sqrt{3k_BT/m^*}$

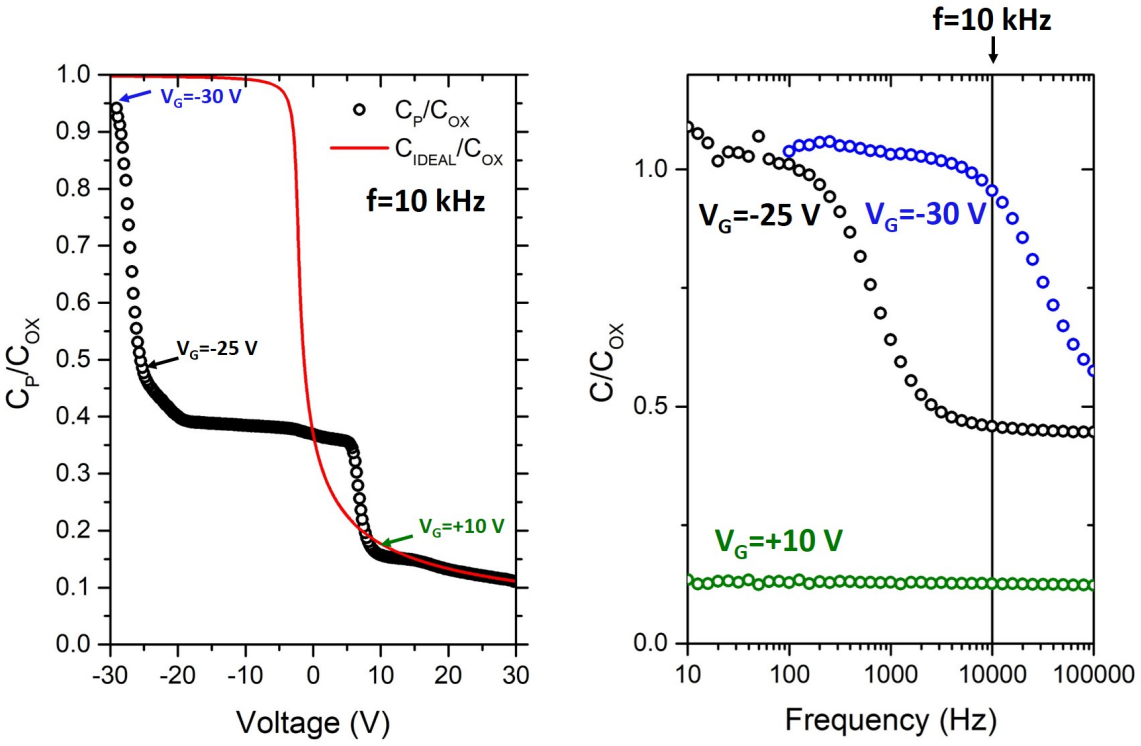


FIGURE 4.12: CV of a MOSCap from $V_G = +30$ V to $V_G = -30$ V at 10 kHz. Cf characteristics of the same MOSCap are plotted at $V_G = +30$ V, $V_G = +25$ V and $V_G = +10$ V, highlighting the frequency response of traps as function of the gate bias.

follow the slow DC signal variation, Q_{it} is then bias dependent and the charge equilibrium is:

$$Q_M = Q_{SCR} + Q_{it} \tag{4.12}$$

The charge response as function of the DC bias in the SCR is then modified, as a small change of gate metal charge δQ_M causes both a response of interface states δQ_{it} and the SCR δQ_{SCR}. However, because $\tau_{it} >> \tau_{AC}$, traps are not able to follow the fast AC signal:

$$\frac{\partial Q_{SCR}}{\partial V_{AC}} >> \frac{\partial Q_{it}}{\partial V_{AC}} \tag{4.13}$$

The measured capacitance is then:

$$C \approx \frac{\partial Q_{SCR}}{\partial V_{AC}} \tag{4.14}$$

Therefore the equivalent circuit is still corresponding to the high frequency one of fig. 4.11.

In the extreme case where the Fermi level pinning effect occurs, in the range -20 V<V_{DC}<+5 V in the fig. 4.12, $\delta Q_{it} >> \delta Q_{SCR}$, i.e. the potential variations of the gate metal are strongly screened by the interface states. Hence, in this condition Q_{SCR} is almost bias independent and the measured capacitance appears to be almost constant versus the DC gate bias. A plateau is then observed at a value of $C \approx 0.35 C_{OX}$. This effect has also been evidenced

by previous works on alumina/oxygen-terminated diamond interface [89, 88, 117]. The post-annealing of the oxide performed in these studies is always reported to lower this density of states, the pinning disappearing or higher C/C_{OX} values can be reached.

(iii) For $\tau_{DC} >> \tau_{AC} >> \tau_{it}$, corresponding to $V_{DC} < -25$ V in fig. 4.12, the traps response is fast. The trapping emitting process is able to follow the AC signal. The high frequency approximation is incorrect and taking into account the contribution of the differential capacitance C_{it} in the total measured capacitance is necessary. Therefore, the low frequency equivalent circuit of fig. 4.11 has to be considered and the total capacitance writes:

$$C = (\frac{1}{C_{OX}} + \frac{1}{C_{SCR} + C_{it}}) \tag{4.15}$$

C_{it} is related to density of interface states by $C_{it} = qSD_{it}$, in the case of a large D_{it}, i.e. in the order of $10^{12} - 10^{13}$ cm^{-2}.eV^{-1}, C_{it} is equal to a few times C_{OX} value. Taking the approximation $C_{it} >> C_{OX}$, the total capacitance at low frequency is then:

$$C \approx C_{OX} \tag{4.16}$$

This approximation is well supported by the Cf characteristic at $V_G = -30$ V, shown in fig. 4.12, where the transition from the low to high frequency case is clearly evidenced, with a maximum capacitance approximately equals to C_{OX}. This could lead to the misinterpretation that the MOSCap is biased in accumulation. However, it is important to note that this is only due to the effect of the fast response of traps. The C_{SCR} value is still pinned, as it is extracted from the high frequency condition, and it was not possible to modulate further the SCR extension even at $V_G = -30$V. As a consequence, there exists an unwanted depleted layer created by the surface depletion on the full surface of the drain to source area. Its width can be estimated from C_{SCR}:

$$C_{SCR} = \frac{CC_{OX}}{C_{OX} - C} = \frac{\epsilon_{Diam} S}{W_{SCR}} \tag{4.17}$$

The extracted value of W_{SCR} at the pinning is 50 nm but is found to vary between 50 nm (RT) and 100 nm (300 °C) depending on the device measured and more strongly on the temperature. Indeed, temperature is lowering τ_{it} and the strong pinning can occur at higher $E_F - E_V$ values as shown in fig 4.11, deeper in depletion. Out of the 400 nm total width of the channel, a substantial part of it cannot be modulated and the accumulation regime can not be reached.

Experimental extraction of τ_{it}

To support this analysis, values of τ_{it} as function of the trap energy position were experimentally extracted by admittance measurements. The temperature was set at 200 °C and the analysis could not be performed at room temperature afterwards due to failure of the MOSCap devices. The working principle of this measurement is detailed in ref. [117], it relies on the measurement of losses induced by the carrier transfer between the band edge and the interface states close to the Fermi level. The losses are maximized when interface

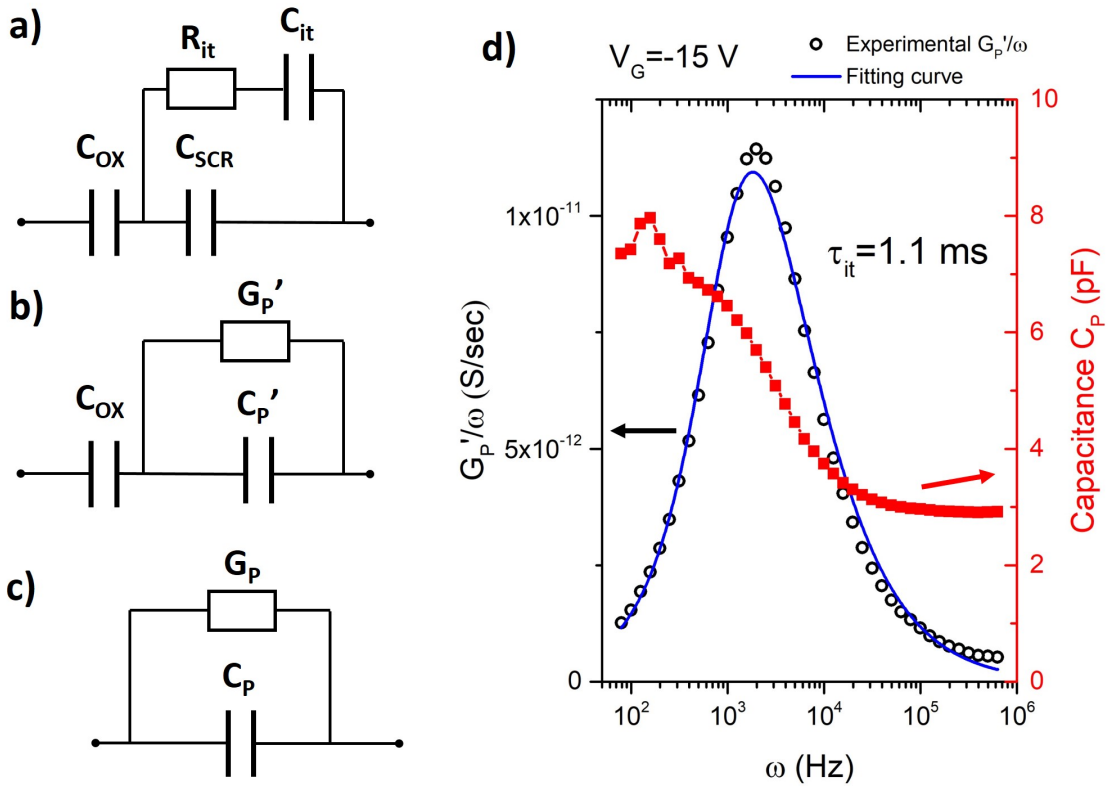


FIGURE 4.13: Equivalent MOSCap circuit with: a) all the components of the MOSCap considered, leakage and serial resistances are neglected, b) the parallel conductance G'_P relevant to measure the interface states induced losses and c) the measured capacitance and conductance C_P and G_P.

traps are in resonance with the applied signal ($\omega\tau_{it} = 1$), i.e. when the Fermi level crosses the trap energy level. It is necessary in the first place to correct the measured conductance by the oxide capacitance, the parallel conductance G'_P of fig. 4.13 b) as function of the measured conductance G_P is given by [121]:

$$G'_P = \frac{\omega^2 C_{OX}^2 G_P}{G_P^2 + \omega^2 (C_{OX} - C_P)^2} \tag{4.18}$$

The plot of G'_P/ω as function of ω for a gate bias $V_G = -15$ V is shown in fig. 4.13. To extract τ_{it}, a fit was performed using the expression of G'_P/ω in the case of a continuum of interface states [122]:

$$\frac{G'_P}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} ln(1 + (\omega\tau_{it})^2) \tag{4.19}$$

This expression fits closely the experimental data and τ_{it} could be extracted as function of the gate bias. However, to find the value of the position of the trap relative to the valence band $E_{it} - E_V$, the surface potential had to be extracted. To do so, it was deduced from the high frequency capacitance of the Cf plot since the equivalent circuit in this case, as already discussed, is only C_{OX} in parallel to C_{SCR}. Knowing C_{OX}, C_{SCR} can easily be deduced and

the surface potential is then given by:

$$V_S = \frac{qN_A\epsilon_0\epsilon_{Diamond}S^2}{2C_{SCR}^2} \tag{4.20}$$

The position of the trap relative to the diamond valence band is then deduced using:

$$E_{it} - E_V = qV_S + q\phi_P \tag{4.21}$$

Where ϕ_P is the energy difference between the Fermi level and the maximum of the valence band at thermodynamic equilibrium in the neutral region of diamond. It can be expressed as $\phi_P = E_g/2 - k_BTln(p/n_i)$ which is around 0.36 eV at 200 °C.

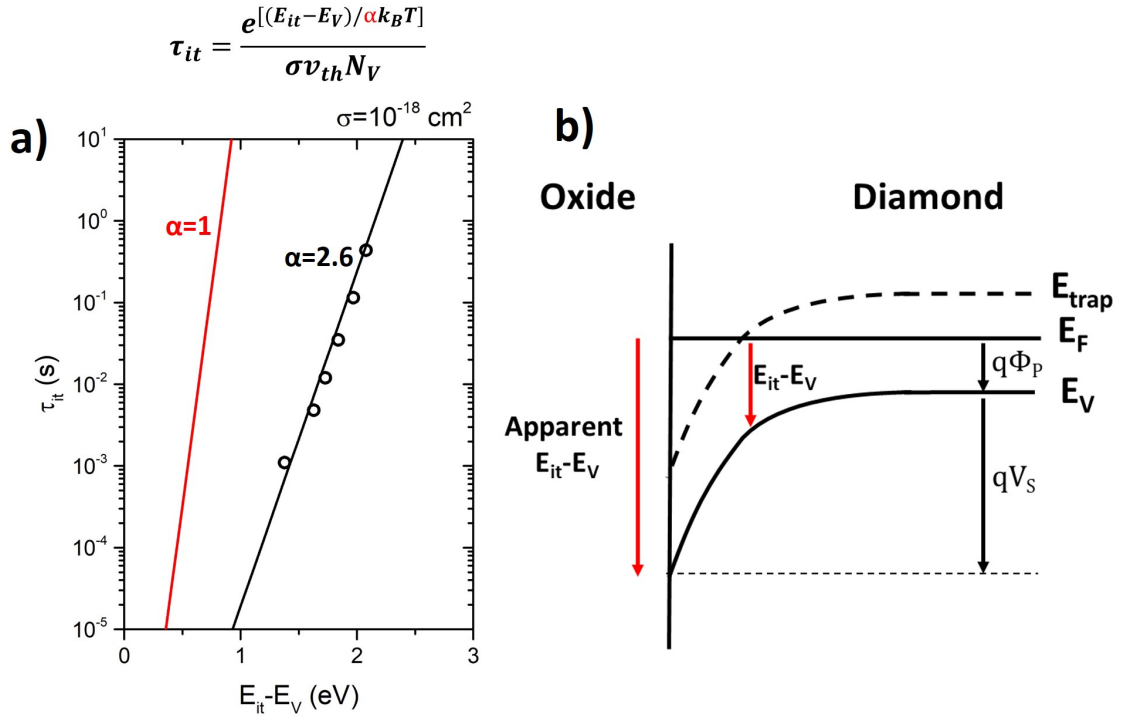


FIGURE 4.14: a) Extracted τ_{it} as function of the trap energy position relative to the valence band. It is shown that equ. 4.11 is not fitting well the experimental values, but adding a correction factor α in the exponential part allows to obtain a good fit, with $\sigma = 10^{-18}$ cm^2 which is typical of donor interface states. b) A possible explanation is the presence of a bulk trap level in diamond. The $E_{it} - E_V$ values cannot be extracted from the surface potential and are then overestimated.

Experimental extraction of τ_{it} as function of $E_{it} - E_V$ is shown in fig. 4.14, it exhibits a characteristic exponential dependence, however it was not possible to fit using equ. 4.11. It was found that introducing a correction factor α in the exponential part leads to a much better fit such that:

$$\tau_{it} = \frac{1}{\sigma v_{th} N_V} e^{\frac{(E_{it}-E_V)}{\alpha k_B T}} \tag{4.22}$$

The best fit was obtained with $\sigma = 10^{-18}$ cm^2, in good agreement with an interface donor state density and $\alpha = 2.6$.

It was not possible to conclude on the correct interpretation of the presence of α in equ. 4.22 using the experiment performed in this work. Other physical mechanisms could be at the origin of such discrepancy, one of them is the presence of bulk diamond traps, schematically represented in fig. 4.14 b) for a single trap level. In depletion, diamond bulk traps could respond to the AC signal where the trap level crosses the Fermi level, somewhere in the bulk. Therefore, in this case the procedure used to extract $E_{it} - E_V$ is not adapted because the surface potential is not relevant anymore. This leads to an overestimation of the trap level in the band gap that could explain the discrepancy shown in fig. 4.14 a).

Additional studies would be necessary to conclude on the origin of the traps. For example, Deep Level Transient Spectroscopy (DLTS) has been extensively used and is a efficient tool to map the defect levels in the semiconductor bulk.

There is also an open question on the effect of the selective growth on the diamond surface. Indeed, a Ti mask was used during growth at high temperature (around 800 °C). The formed carbide was then removed by acid cleaning, but such procedure could lead to a degraded surface and possibly titanium diffusion in diamond. There is a possibility that the electrostatic at the surface is affected, with a discrepancy between the calculated band bending and the real one.

The difficulty of large D_{it} extraction

Accurate estimation of the interface states density D_{it} can be challenging in case large values. As discussed in [121], the conductance method is underestimating D_{it} when the interface state capacitance C_{it} is large in comparison to the oxide capacitance, $C_{it} >> C_{OX}$. As shown before, the measured capacitance in low frequency condition is $C \approx C_{OX}$, therefore C_{it} can not be deduced. Also, it is not possible to identify the origin of the parasitic charge and apply the correct model, undifferentiated interface traps and diamond bulk traps could respond during the measurements. In that regard, DLTS in constant capacitance mode analysis would be the most efficient way to quantify it, in addition to allow for the differentiation of interface states from bulk traps in the oxide or diamond. This method relies on measuring the decay of the capacitance over time after a bias pulse, as the interface states need time to emit or capture charges. DLTS studies have been performed in our research group using Schottky diodes [123, 124, 125] and the new equipment (delivered end of 2019) should be useful for these MOS structures characterization.

4.2.3 Discussion on accumulation regime reported in O-terminated MOSCaps

Improving the oxide/diamond interface so that the accumulation regime of a MOSCap can be reliably obtained is a great challenge for diamond devices. Accumulation regime and its control paves the way for 2D Hole Gas (2DHG) enhancement devices. Such already existing devices, the H-terminated FETs, use the surface transfer doping effect to create a

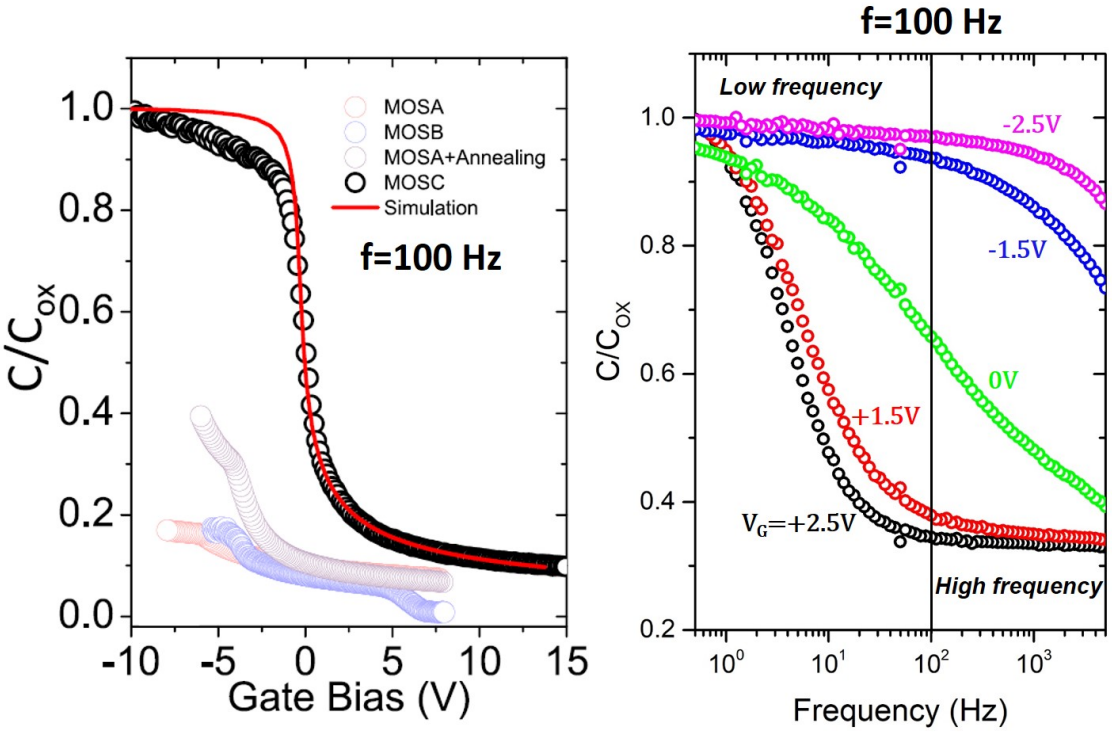


FIGURE 4.15: At left, CV characteristic of a MOSCap published in [88] at $f = 100$ Hz. At right, capacitance versus frequency plot for varying gate biases. The cut-off frequency between low and high frequency regimes is clearly shifting to higher values as the Fermi level is moving toward the diamond valence band. In the case of $C_{it} >> C_{OX}, C_{SCR}$, which seems to be the case, the capacitance measured is approximately C_{OX} in the low frequency condition, leading to the false interpretation that accumulation is measured in the CV plot.

2DHG. They are therefore, for most of them, normally-on and due to the close proximity of acceptors species with the 2DHG, moreover the mobility is limited by coulombic interactions to typical values between 50 and 300 $cm^2/(V.s)$. An accumulated hole gas using O-terminated diamond would allow normally-off devices with mobilities not limited by this effect as the negative charge layer would be located at the opposite side of the oxide. There are however very few experimental demonstrations of the observation of the MOSCap accumulation regime and this part will discuss their validity.

In two of our earlier reports [50, 88], we have claimed to obtain the accumulation regime in an O-terminated lateral MOSCap, similar to the process used in sample MOS8, based on CV characterization. In these reports, a 40 nm alumina layer was deposited by ALD at 380 °C on a 500 nm p-type layer with $[B] = 5 \times 10^{16}$ cm^{-3}, and annealed at 500 °C in high vacuum. The CV characteristic at $f = 100$ Hz in [88], from negative to positive bias, is shown in fig. 4.15 with the measured capacitance C reaching C_{OX} at $V = -10$ V, as expected for the accumulation regime. However, as discussed previously, a large density of fast responding traps could induce a measured capacitance value close to C_{OX}, while the Fermi level still being pinned. A frequency dispersion analysis must therefore

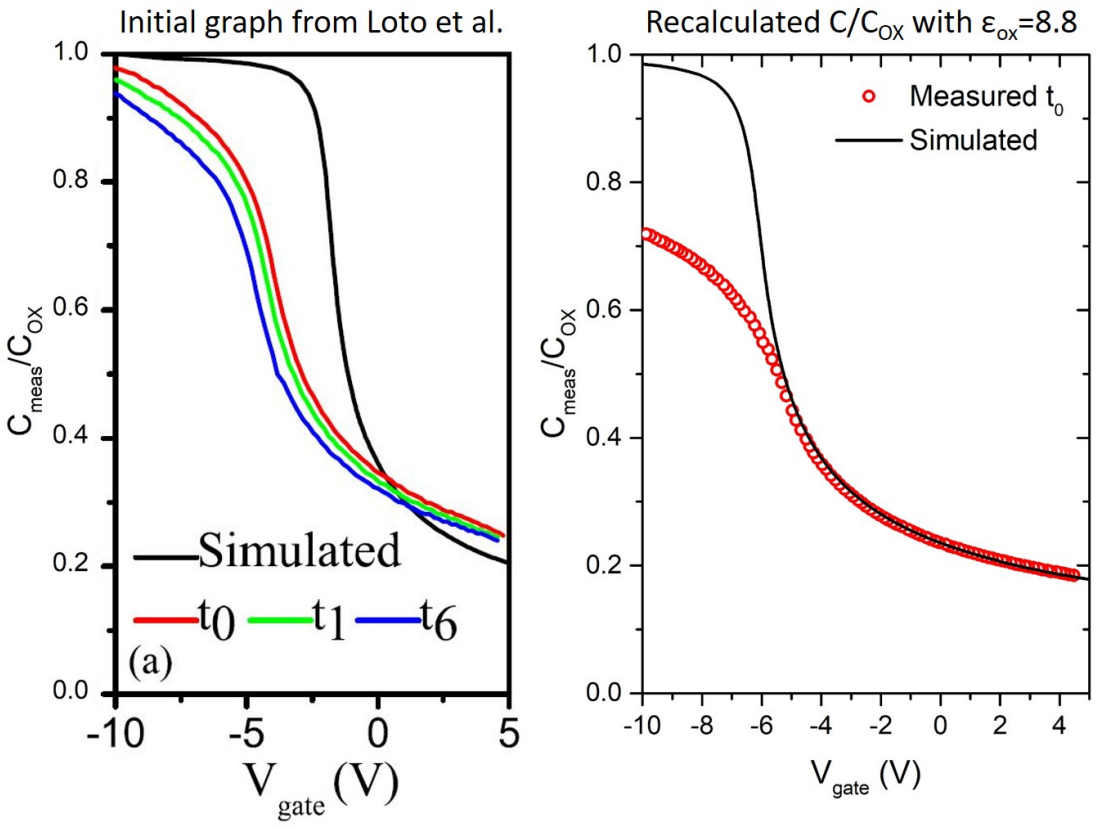


FIGURE 4.16: At left capacitance versus voltage plot of [89] (Copyright ©2018, IEEE) for different bias stress conditions detailed in the publication, the simulated curve is not fitting closely the measured data. At right, calculated ideal CV using $\epsilon_{OX} = 8.8$ compared with the experimental curve after the stress condition t_0.

be performed in order to conclude on the presence of a pinning or not. Capacitance versus frequency characterizations at different gate biases on the same sample are shown in fig. 4.15, a transition from high to low frequency interface states regimes is clearly evidenced, in the bias range where the transition to accumulation-like regime is observed. We could not conclude on the real value of the surface potential since the high frequency condition could not be match in the frequency range measured, for biases lower than 0V. Cf were not measured for lower biases than -2.5 V, but based on these measurements, the C/C_{OX} value measured at -10 V is must likely also due to a large density of fast interface states.

Another paper of our group [89] claimed to reach accumulation regime as well. Similarly, a 40 nm alumina layer was deposited by ALD at 380 °C on a p-type layer, doped at 2×10^{17} cm^{-3}, and annealed at 500 °C in high vacuum. The CV characteristics measured at $f = 100$ kHz under different stress time, detailed in the publication, are shown in fig. 4.16 along with the ideal calculated curve. Due to the absence of working MIMCaps on the sample, the oxide capacitance could not be determined accurately. However, thanks to the closeness of the oxide deposition process used compared to sample MOS8, an estimation

of the ideal curve with $\epsilon_{OX} = 8.8$ is shown in fig. 4.16, a flatband shift has been added to fit the experimental data. The curve with the bias stress condition t_0 was used as reference. The ideal curve in this later case fits much better the data than previously reported, but the experimental CV exhibits a large stretch-out for a bias $V < -5$ V and does not reach the C_{OX} value. Considering this, it is very likely that the C_{OX} value was unreliably estimated leading to the misinterpretation that accumulation regime was reached. Nevertheless, the pinning effect after annealing seems to be less strong and at a higher C/C_{OX} value than in MOS8 sample, despite the similar fabrication process. It highlights the difficulty to control and obtain reproducible results regarding the diamond/oxide interface.

We can notice however that accumulation regime has most probably been observed in [90], using ALD SiO_2 as gate oxide. In this study, a normally-off FinFET device was fabricated using 45 nm of ALD SiO_2 as gate oxide, the presence of a 2DHG at negative gate bias was evidenced by IV characterization. It is not clear what surface treatment was used and no mention of an oxygen treatment was done. It might be possible that ALD SiO_2 forms a less defective interface with diamond or that a different surface termination led to a weaker surface pinning. Even if hydrogen and oxygen terminations are the most widely used, a mix a O and H termination can also be considered to tune the surface electron affinity, but is challenging to control.

4.3 Conclusion

As early measurements on MOSCaps and MOSFETs were exhibiting large discrepancies with the ideal case as well as being affected by white light exposure, a careful study of parasitics effects introduced by the oxide and the substrate as been carried out. A large density of states between the alumina and diamond has been evidenced, impacting significantly the ability to modulate the SCR width as function of the gate bias. The Fermi level pinning effect, present in all previously reported O-terminated MOSCap reported by our research team, causes the presence of a fixed SCR extension of about 50 nm to 100 nm at negative gate bias, which limit the effective channel width of the MOSFET as well as prevents from obtaining the 2DHG in accumulation regime.

The slow emission time constants of some of these traps, in the order of seconds to minutes, are particularly problematic for the D3MOSFET operation. It limits the performances while commuting, an example will be provided in the chapter 5.

The origin of these traps and their energy level in the diamond band gap is still unclear. Diamond bulk traps could play a significant role, but a DLTS analysis is required. As a prospective, the effect of the selective growth process on the interface would be interesting to analyse. The damage caused by the titanium mask under the high temperature required for diamond CVD growth, and also the subsequent acid cleaning to remove it, are significantly detrimental for the oxide/diamond interface.

Despite these issues, it is remarkable to note that the leakage current in the MOS structures is low, able to sustain high fields. The MOSCaps, with a 50 nm alumina layer, could

safely sustain a gate bias of +50 V in reverse and down to -30 V in forward. Such feature is key to operate the D3MOSFET.

Chapter 5

Characterization of the lateral deep depletion diamond MOSFET

Diamond resistivity and contact resistances will be extracted and compared to the model described in chapter 1. Then, the D3MOSFET transistor characteristics will be analysed for different temperatures and substrate bias conditions. The impact of the effects evidenced in the chapters 3 and 4 on the D3MOSFET, originating from the oxide, the oxide/diamond interface and the substrate will be investigated. An on state and off state analysis will be provided to evaluate the device performances in comparison with other diamond FET. Finally, evaluation of optimized structures will be given as a perspective.

This chapter will focus on the electrical transport characterization of the D3MOSFET, toward the demonstration of the diamond potential for power electronics. Results will be compared to the physical models previously developed. One of the objectives is to demonstrate the performances gains thanks to adding the selective growth and the mesa etching to the fabrication process, in comparison to the D3MOSFETs fabricated by T. T. Pham et al. [48, 49, 50]. They faced on state limitations due to poor ohmic contacts. To that end, specifically design structures will be characterized to extract the resistivity of the diamond layers and the source and drain contact resistances. Moreover, the impact of the interface physical mechanisms on the device operation, described in the chapters 3 and 4, will be discussed. They are illsutrated in fig. 5.1 in the D3MOSFET structure:

(i) The optically and thermally activated back PN junction with the substrate, which causes the existence of a SCR that can be controlled by biasing the substrate.

(ii) The uncontrolled surface potential that deplete between 50 nm and 100 nm of the p-type layer.

Then, the double top-gate design will be introduced and described, as a mean to obtain a bi-directional D3MOSFET. Finally the fabricated devices will be compared to the literature and to the theoretical performances expected for optimized devices, according to the models developed in chapter 1.

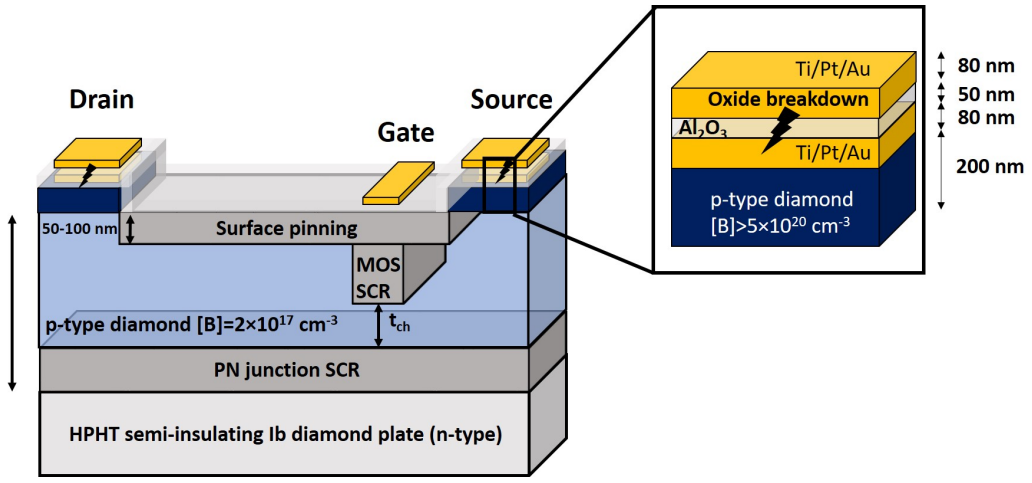


FIGURE 5.1: Schematic representation of the D3MOSFET including the features demonstrated in the chapter 3 and 4: the uncontrolled surface pinning and the optically activated back PN junction with the substrate.

5.1 Channel resistance and source and drain contact resistances measurements

The diamond resistivity and the contact resistances are key parameters that define the on state resistance of the device. In this section, they will be determined using specifically design structures on the sample, by measuring the resistance between contacts patterns for varying distances. In this part, only the linear geometry described in fig. 5.2 is considered. A circular one could be envisaged with the advantage to not require a mesa etching, but needs to be corrected by a geometric factor and requires more space on the sample. Three variants have been designed and compared:

(i) Contacts on the p-type layer with selective p++ growth to obtain a good ohmic behaviour. This is the design used for the fabrication of D3MOSFETs, the objective is to lower the contact resistances, and so the p-type layer resistivity can easily be extracted.

(ii) Contacts on the p-type layer formed by direct deposition of metal without p++. This was the previous design used by T. T. Pham et al. [48, 49, 50] which showed a very large contact resistance. Current-voltage characteristics will be compared to the design (i).

(iii) Contacts on the p++ layer, in order to extract the heavily doped layer resistivity as well as the contact resistances.

Considering that the metal resistance is negligible and that $L >> t_{epi}$, the total resistance can be well approximated by a 1D model where the total resistance R is the sum of the channel resistance and the contact resistances $R = R_{Diam} + 2 \times R_C$ (2D effects are neglected). R can be expressed as function of the diamond resistivity:

$$R = \frac{\rho L}{W \times t_{ch}} + 2R_C \tag{5.1}$$

Where t_{ch} is the effective channel thickness of the p-layer. As illustrated in fig. 5.2, the surface covered by the oxide layer of the sample has been demonstrated to exhibit a large surface potential, depleting part of the p-layer. This depleted layer thickness was determined to range between 50 nm and 100 nm from CV measurements. Moreover the substrate causes the presence of a back SCR extending in the p-layer, further limiting the effective conducting p-layer thickness. It can be mitigated by applying a negative bias under light exposure on the substrate, to polarize the PN diode in forward regime, removing the back SCR. Due to the large resistance of the substrate, the current injected in the structure is negligible. In all subsequent measurements, a fixed bias of -100 V under white light optical excitation is then applied to the substrate. In order to extract the resistivity, a t_{ch} value between 300 nm and 400 nm was assumed.

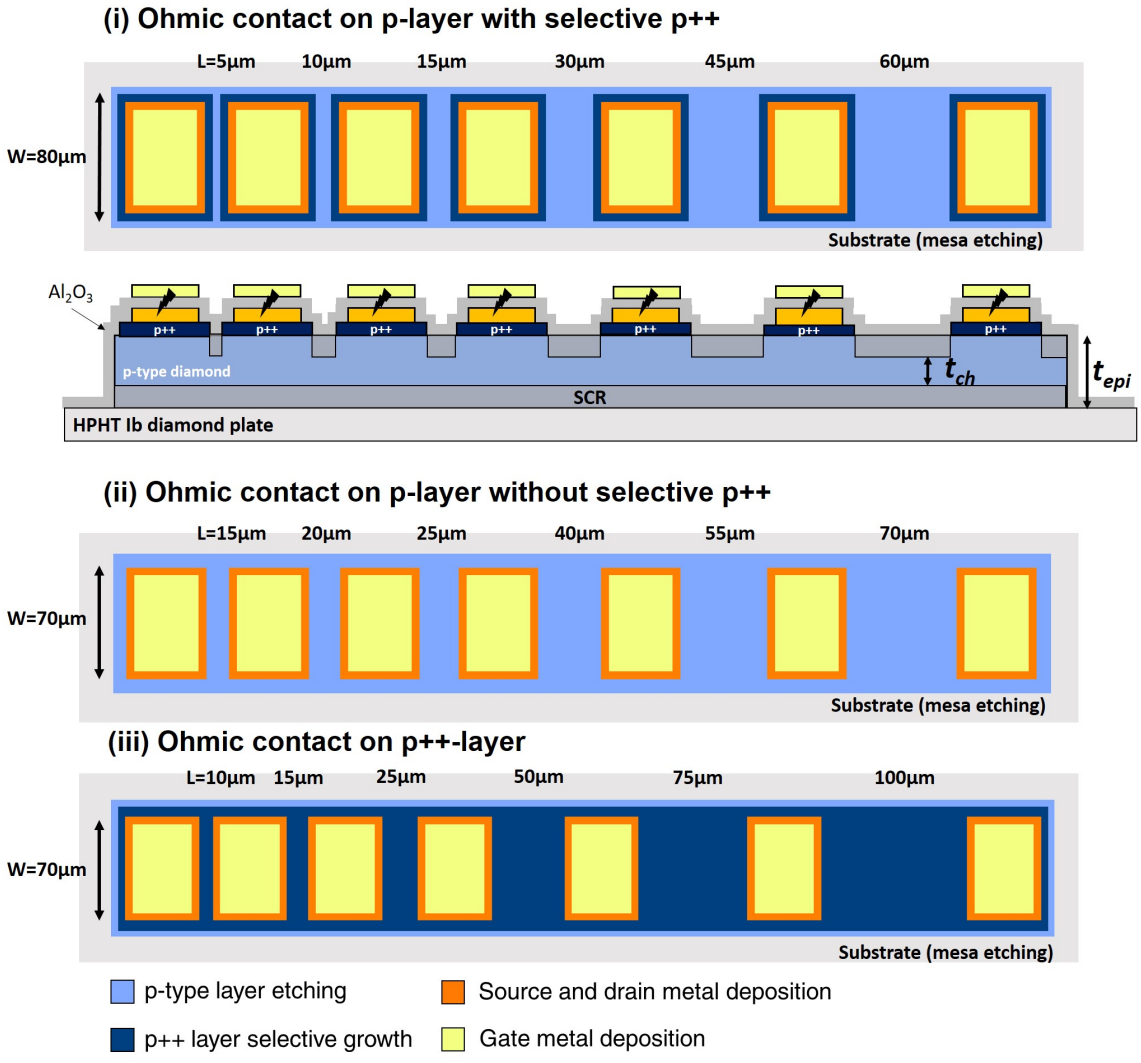


FIGURE 5.2: Top view and side view of the mask used to fabricate the structures measured to analyse the diamond resistivity and contact resistance.

5.1.1 p-type epilayer electrical transport characterization

Boron doped diamond resistivity extraction using contacts made with selective growth of heavily doped diamond

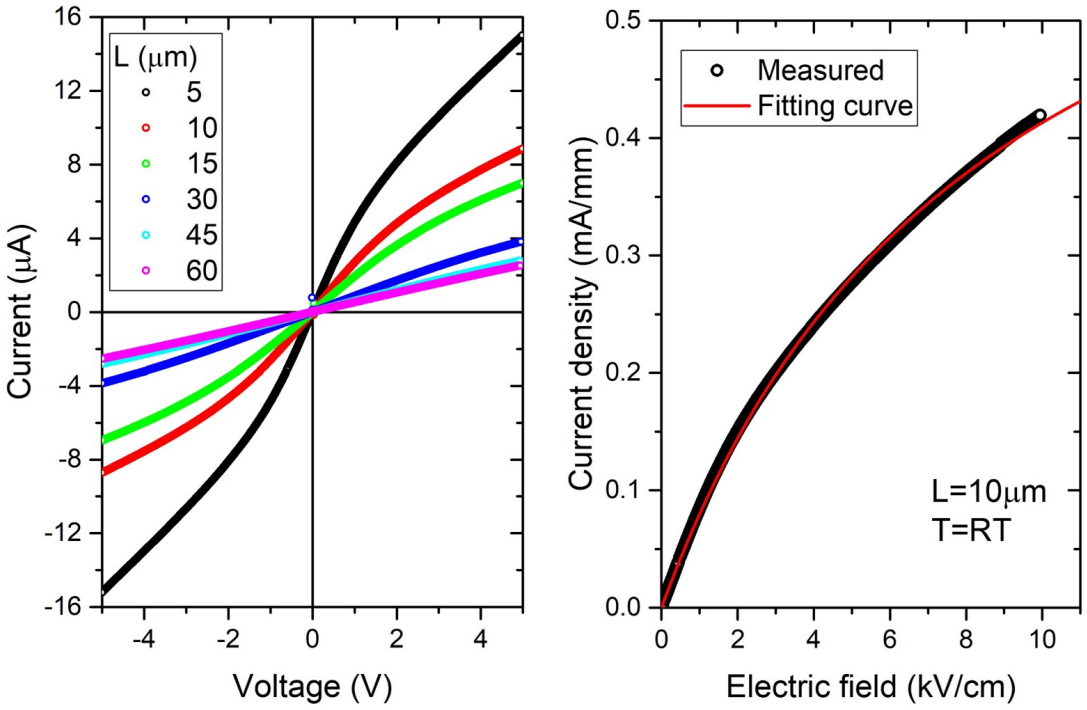


FIGURE 5.3: Left, IV characteristics measured on the structure (i) of fig. 5.2 for different distances between pads at room temperature. Right, measured IV characteristic (black) between two contacts of pattern (i) with $L = 10$ μm at room temperature. The best fit is obtained for $v_{sat} = 1 \times 10^7$ cm/s.

Typical room temperature IV measurements of the design (i) of fig. 5.2 are shown in fig. 5.3. These contacts exhibit good ohmic behaviour at low electric field (<1kV/cm), thanks to the selective growth of heavily doped diamond, with an increase of the resistance at higher field ($\approx$ few kV/cm). This is due to inelastic scattering of carriers by optical phonon, when a significant fraction of them are sufficiently accelerated to reach a kinetic energy higher than the optical phonon energy. Eventually, at very high field, this energy loss mechanism completely balance the energy gain by increasing the electric field. In this situation, the carriers velocity becomes completely independent from the electric field and current saturation is observed. This complete saturation is however not observed experimentally as the measurement at higher fields would induce significant self-heating.

A first approximation of the hole saturation velocity can be obtained by [126]:

$$v_{sat} = \sqrt{E_{op}/m_h^*} = 1.8 \times 10^7 cm/s \tag{5.2}$$

Where $E_{op} = 165$ meV is the optical phonon energy in diamond [127] and m_h^* the density of states hole effective mass $m_h^* = 0.908 m_0$.

The electric field dependence of the current can be expressed as function of v_{sat} by:

$$I = I_0 \frac{\mu_{LF} E}{1 + \frac{\mu_{LF} E}{v_{sat}}} \tag{5.3}$$

where I_0 is a constant independent of E and μ_{LF} is the low field mobility, calculated using the previously described empirical model of ref. [61] to be $\mu_{LF} = 1165$ cm^2/(V.s) at room temperature. A fit of an experimental IV curve using equ. 5.3 is performed in fig. 5.3, with a best fit for $v_{sat} = 1 \times 10^7$ cm/s, close to the approximated value.

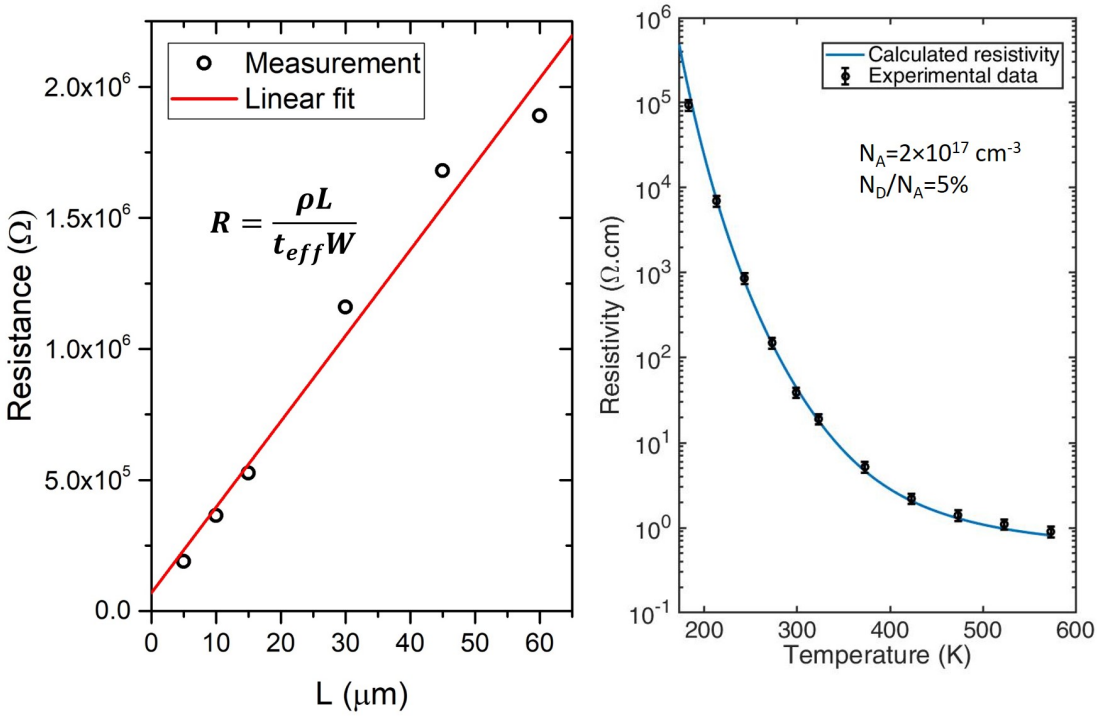


FIGURE 5.4: Left, plot of the resistance as function of L at room temperature, the resisitivity is extracted from the slope of the linear fit. Right, experimental resistivity using $t_{eff} = 350 \pm 50$ nm. The calculated curve is found to fit best the data using a doping level of 2×10^{17} cm^{-3} and a compensation ratio of 5% ($N_D = 1 \times 10^{16}$ cm^{-3}).

To determine the low field resistivity of the conducting p-type channel, the resistance is extracted from the linear slope at low field and its variation against L is plotted in fig. 5.4. The resistivity as function of temperature is extracted and compared with the empirical model [61] described in chapter 1 in fig. 5.4. The doping level of 2×10^{17} cm^{-3} with a compensation ratio of 5% ($N_D = 1 \times 10^{16}$ cm^{-3}) is extracted by fitting the measured data over 5 decades in all the temperature range, from 183 K to 573 K, in agreement with the doping level extracted by CV measurements. A comparison of this ratio to literature is shown in fig. 5.5, compiled by Traore et al. [74]. The compensation ratio values reported in literature

have a very wide range, and obtaining 5% is not uncommon. Reducing it would decrease the resistivity variation as function of temperature, but in case of a high temperature operation, around 500 K, the effect of compensation on the resistivity is almost negligible.

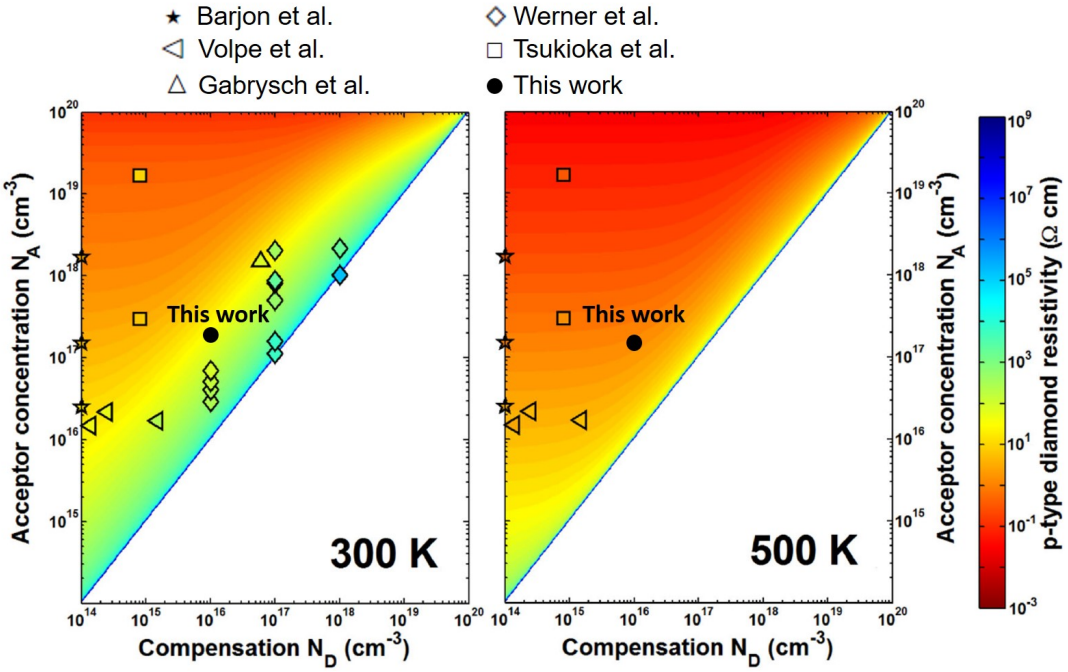


FIGURE 5.5: Resistivity as function of acceptor concentration and donor concentration in various p-type diamond layers reported in literature, from [74]. Experimental data are taken from Barjon et al. [128], Volpe et al. [61], Gabrysch et al. [129], Werner et al. [130], Tsukioka et al. [131] and this work.

The dispersion of measured data is too large to extract an accurate contact resistance value. It is assumed that t_{ch} is not homogeneous over all the structure, caused by the uncontrolled surface potential partially depleting the channel.

High resistance of metallic contacts on lightly boron doped diamond

A comparison between the IV characteristic of contacts from designs (i) and (ii) of fig. 5.2 with an identical length of 15 μm is shown in fig. 5.6. Despite the annealing of contacts after deposition at 773K to form a carbide at the metal/diamond interface [132] and the similar doping density of the sample than used in [133], the linearity of the IV characteristics in pattern (ii) could not be achieved as shown in fig. 5.6. A significant barrier at the interface is limiting the current density, due to the surface potential of diamond. The formed TiC layer is not sufficient enough to lower the contact resistance down to negligible values, it introduces traps on which carriers can tunnel to from the metal, but it seems to be the limiting mechanism instead of the diamond resistivity. It is compared to values measured on pattern (i) where the very high doping of the p++ makes the depleted surface layer very thin, carriers are able to efficiently tunnel through the barrier. The non-linear

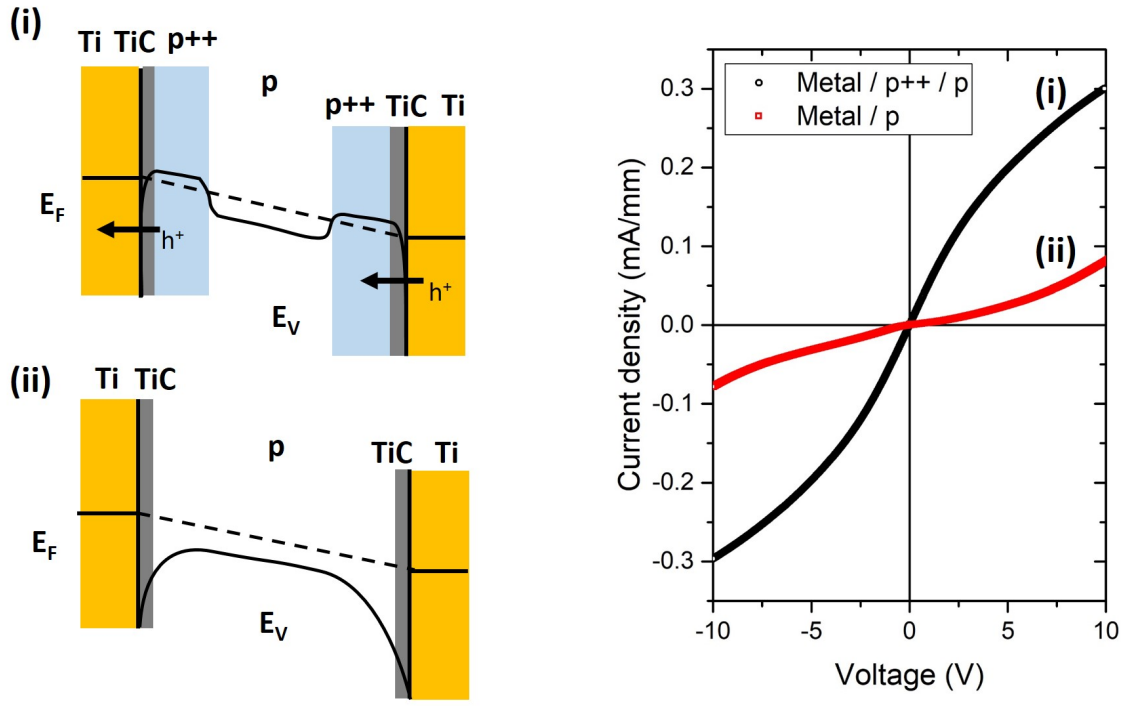


FIGURE 5.6: Band diagram of the patterns (i) and (ii) under bias and their IV characteristics measured between two contacts with $L = 15\ \mu$m.

shape of the IV in this case is due to the high field regime in which the carriers velocity saturates.

5.1.2 Resistivity extraction of heavily doped diamond and its contact resistance with the metal

The resistivity of the 200 nm heavily doped layer, extracted from the resistance versus distance plot measured on the design (iii) shown in fig. 5.7, is 3 mΩ.cm. This value is much lower than the channel layer resistivity, a comparison is shown in fig. 5.8 where it can be seen that there are several orders of magnitude difference. It is in good agreement with a doping density expected between 5×10^{20} cm^{-3} and 1×10^{21} cm^{-3} [134, 135, 136]. The weak temperature dependence is also an indication that the heavily doped diamond layer is degenerate, with a doping level above the critical concentration between 2×10^{20} cm^{-3} and 5×10^{20} cm^{-3} [64, 72]. The contact resistance R_C is extracted to be 14 Ω at RT, which can be due to the metal/diamond interface barrier as well as the broken oxide layer between the two metal contacts. The contribution from these two effects couldn't be isolated and only the total is considered to extract the specific contact resistivity expressed as:

$$\rho_C = R_C \times S_C \tag{5.4}$$

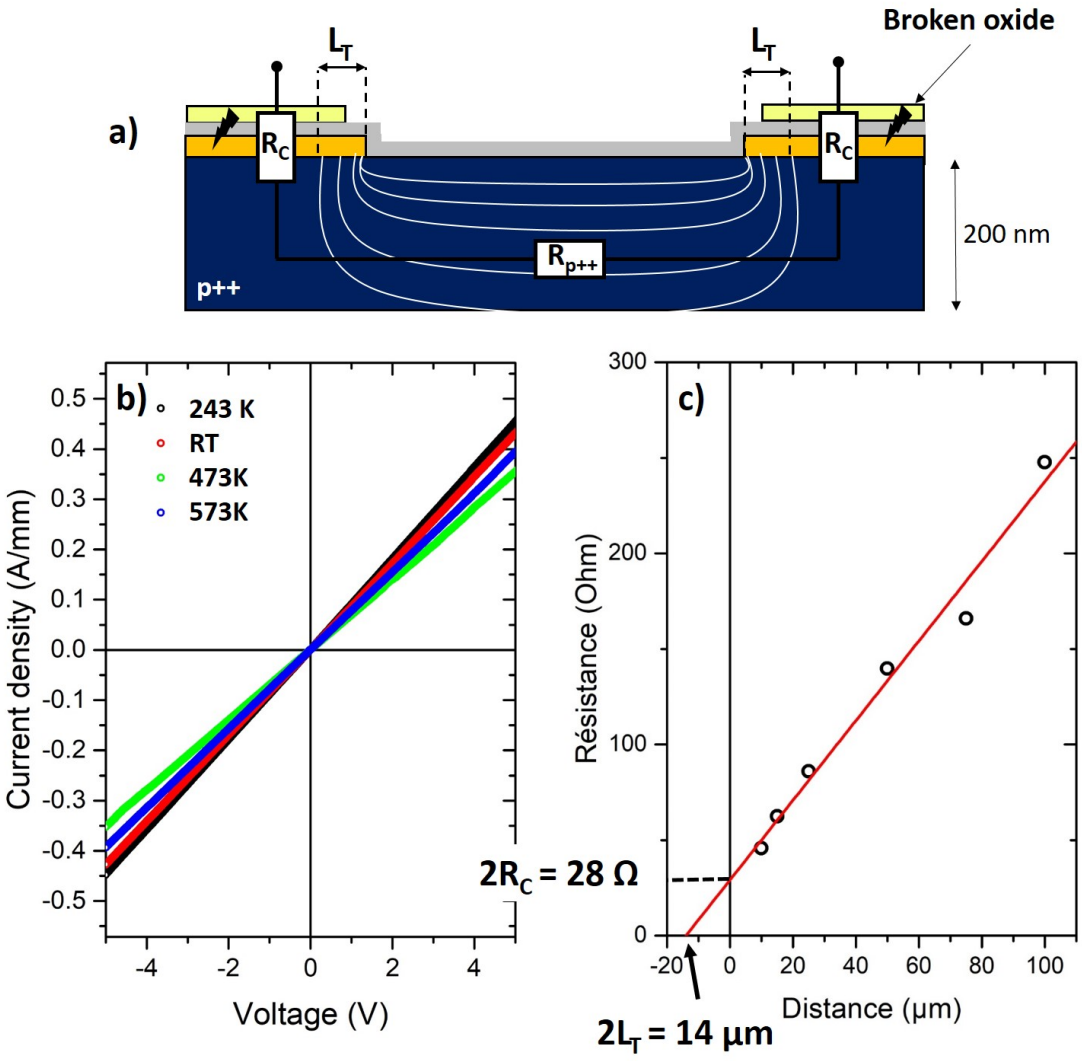


FIGURE 5.7: a) Schematic cross section of the structure (iii) used to measure the p++ layer resistivity. The current flowlines are represented by the white lines, extending up to a length L_T below the metallic contacts. b) IV characteristics for different temperatures with 75 μm between contacts. c) Extracted resistance as function of the distance between the contacts at RT.

Where S_C is the surface contact area. In a lateral geometry, the current is flowing only through the edge of the contact, up to the transfer length L_T determined by the resistance versus distance plot of fig. 5.7, then:

$$\rho_C = R_C \times L_T \times W \tag{5.5}$$

Using $L_T = 7\,\mu$m, $R_C = 14\,\Omega$ and $W = 70\,\mu$m, $\rho_C = 7 \times 10^{-5}\,\Omega.\text{cm}^2$ was obtained. This is a higher value than reported in [137], in the range of $10^{-7}\,\Omega.\text{cm}^2$, or in [51], extracted to be $7.4 \times 10^{-6}\,\Omega.\text{cm}^2$. This is probably due to the presence of the oxide layer, but the added resistance still remains orders of magnitude lower than the lateral D3MOSFET total resistance and does not disturb its operation. As an example, the calculated resistance of

the lightly doped p-type layer with $W = 70$ μm, $L_{DS} = 10$ μm and $t_{ch} = 400$ nm at 473 K is 5 kΩ. Much higher than the 200 nm thick heavily doped source and drain layers resistance, assuming a transfer length of 7 μm, evaluated at 15 Ω.

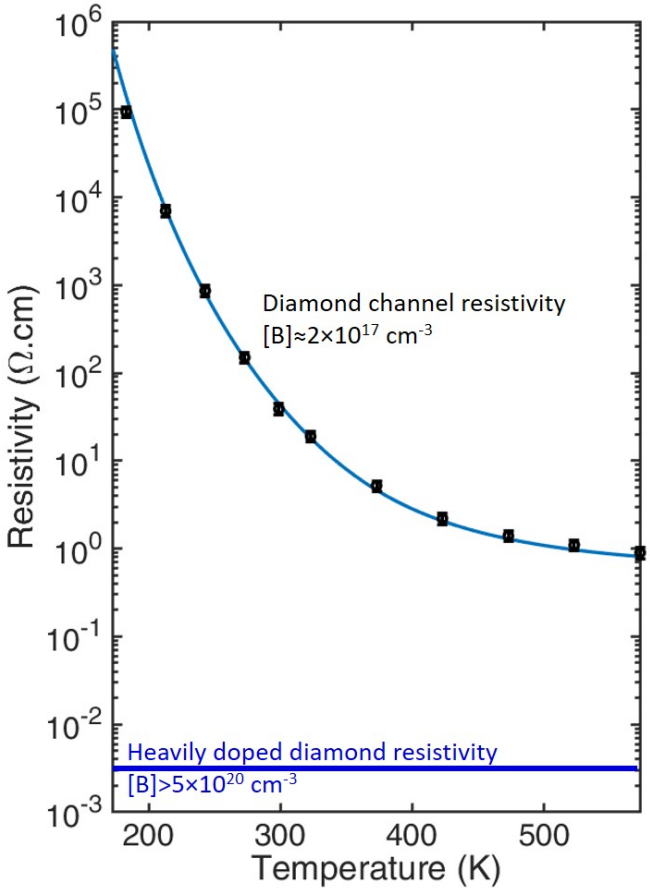


FIGURE 5.8: Heavily doped diamond layer resistivity compared to the lightly doped channel layer shown in fig. 5.4.

5.2 Quasi-static transistor characteristics (I_{DS} vs V_{DS}, I_{DS} vs V_{GS}) with an insulating or n-type activated substrate

All the physical models developed previously are not taking into account dynamic effects occurring during fast commutation times. But the limiting processes to reach a quasi-static case are the interface defects and the back PN junction, both of which having a characteristic time to reach equilibrium of the order of several seconds to minutes. Obtaining true quasi-static characteristics is requiring long measurement durations that are difficult to reach in practice, as the measurement setup used is sensible to vibrations and contact loss between the metallic pads and the tips, which can occur during measurement. The measurements were performed using a Keithley 2612 SourceMeter for the drain, source and

gate bias. The substrate bias was applied using an additional Keithley 2410 SourceMeter whose ground is common to the Keithley 2612 ground. The LabTracer software was used to operate them. All the measurements shown in this section have been obtained on the same transistor which is represented in fig. 5.9, with $W = 110$ μm, $L_{GS} = 4$ μm, $L_G = 2$ μm and $L_{GD} = 10$ μm. These values are not optimized for the doping level used, due to constraints in the fabrication process, but can be extrapolated to different device sizes.

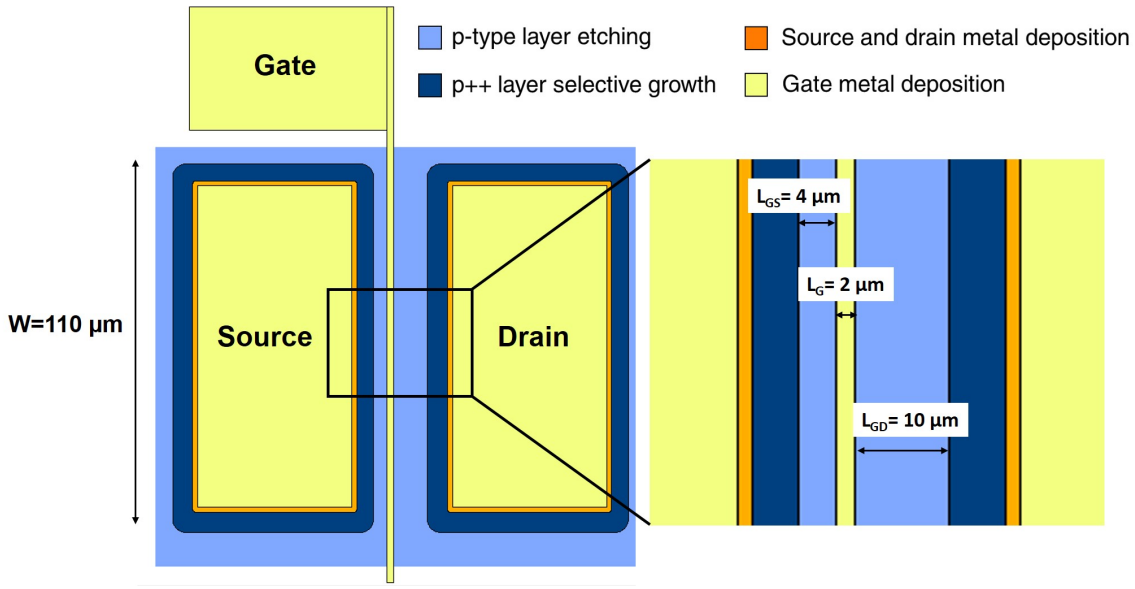


FIGURE 5.9: Schematic top view of the measured MOSFET in the following section.

5.2.1 The quasi-static regime: effect of the V_{DS} sweep rate

The back PN junction between the p-layer and the substrate is very resistive, as such when the SCR is modulated by a bias V_{Sub} there is a large RC characteristic time to reach equilibrium. An order of magnitude calculation assuming a SCR of 100 nm width with a typical substrate resistivity of 0.3 GΩ.cm, under light excitation or at 250 °C, gives $\tau = RC = 0.7$ s. Additionally, the presence of slow traps at the diamond/oxide interface has been evidenced previously, with time constants in the same orders of seconds to minutes. It is then not possible to reach the true quasi-static condition, but we can approach it by testing different V_{DS} sweep rates and choosing the more adapted to the measurement, as depicted in fig. 5.10. In the measurement conditions used, the substrate and the source are shorted and grounded, the back PN junction is activated by light and temperature. Then, when V_{DS} is swept, the voltages V_{GD} and V_{Sub-G} are being swept as well. As the modulation of the back and gate SCRs is time dependent, a longer sweep rate of V_{DS} results in a wider SCR that reduces the drain current. This corresponds to what is observed in fig. 5.10 where the fastest sweep rate of 20 V/s yields a significantly higher maximum drain current at $V_{DS} = -40$ V. Slower sweep rates tends to converge to an IV characteristic which is assumed to be the quasi-static regime. The 0.8 V/s and 0.4 V/s characteristics are almost

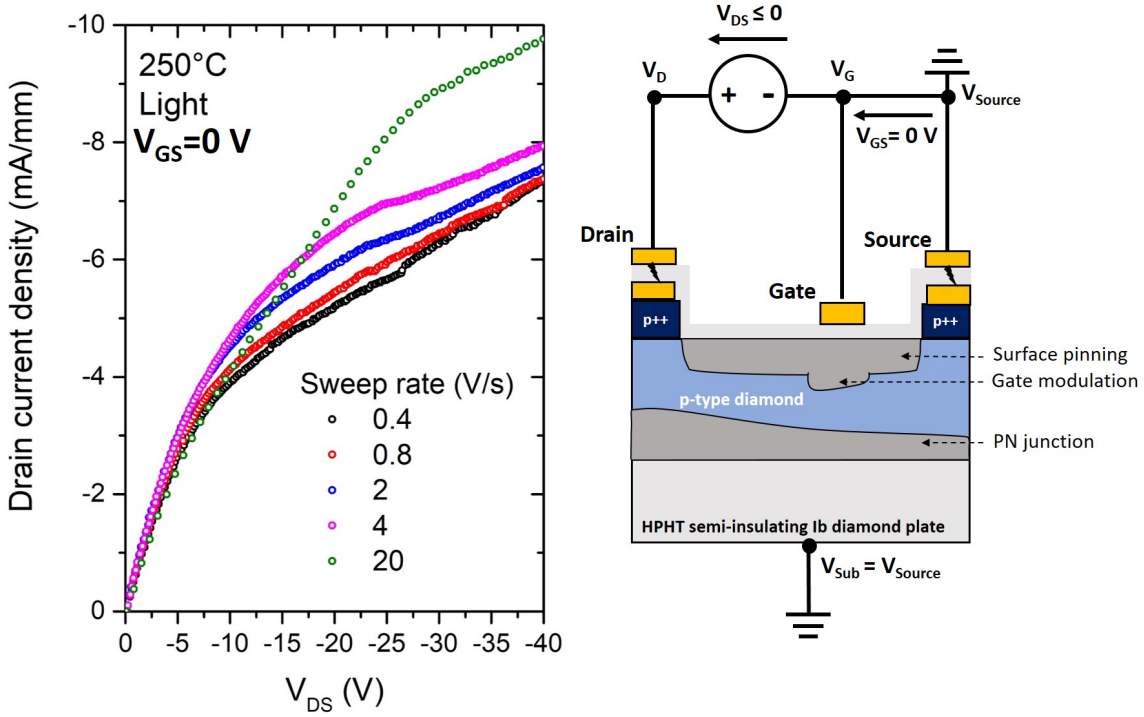


FIGURE 5.10: Drain current density as function of V_{DS} for different V_{DS} sweep rates, with $V_{Sub} = V_{Source}$ and $V_{GS} = 0$ V. The measurement was performed at 250 °C under a 11 mW/cm^2 white light irradiance.

identical. Consequently, all the following measurements have been performed using a sweep rate of 0.4 V/s.

5.2.2 Optical activation of the n-type substrate effect on the D3MOSFET

The successful operation of the D3MOSFET is shown in fig. 5.11 in light and in dark, with a clear on and off state in both conditions with $V_{TH} \approx 35$ V. At room temperature, the n-type substrate is activated by a white light irradiance of 11 mW/cm^2 in order to modulate the back PN junction. Whereas in the dark the substrate can be considered as an insulator, the PN junction electrostatic is frozen. The configuration $V_{Sub} = V_{Source}$ was used to control the substrate instead of letting it floating, inducing a stronger pinch-off effect. The polarization of the back PN junction in reverse toward the drain contact, shown in fig. 5.12, acts as a second gate. Indeed, a clear saturation regime is observed under light exposure that is not present in the dark. The room temperature drain-source saturation current under light exposure at $V_{DS} = -40$ V in on state at $V_{GS} = -10$ V is 0.12 mA/mm and more than 5 order of magnitude lower in off state, below the detection limit of 1 nA/mm for $V_{GS} = +40$ V. The gate leakage current also remained below detection limit, $I_{GS} < 1$ nA/mm, in the range of V_{DS} (0 to -40 V) and V_{GS} (-10 to +40 V) measured.

However, it is not clear why the on state resistance $R_{ON,S}$ is significantly higher in the dark, from 8.8 Ω.cm^2 to 40.5 Ω.cm^2. A preliminary hypothesis is that the surface pinning

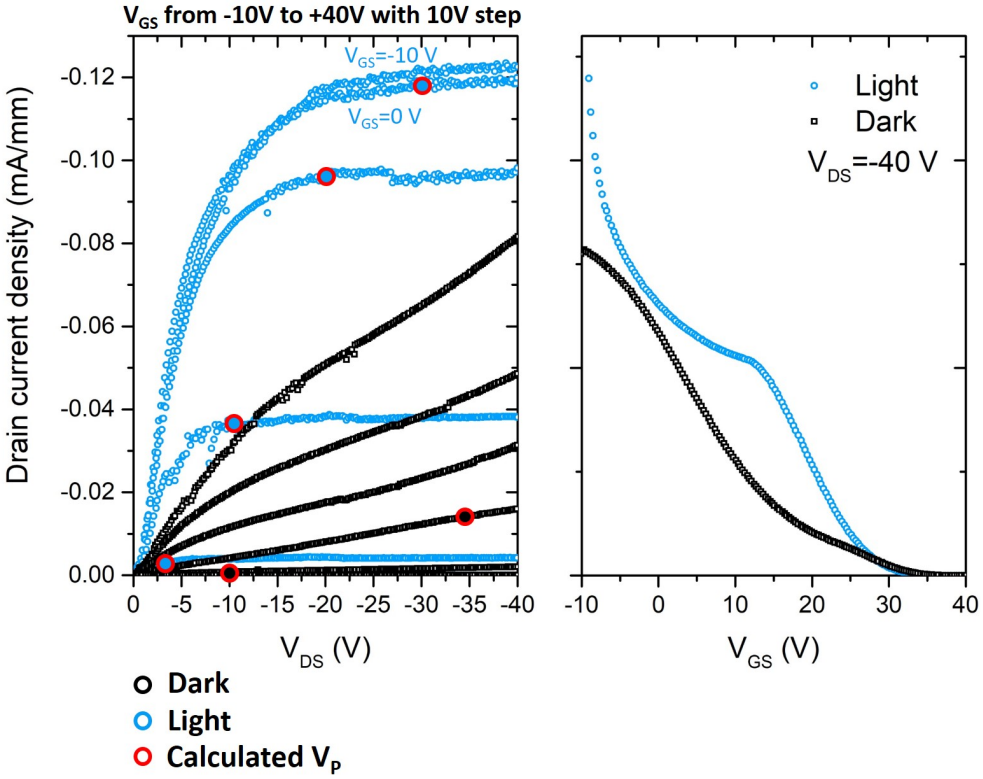


FIGURE 5.11: At left, I_{DS} vs V_{DS} for V_{GS} from -10 V to +40 V with a 10 V step. The calculated pinch-off voltages V_P in both light and dark are shown with red circles. At right, transfer characteristic I_{DS} vs V_{GS} at $V_{DS} = -40$ V. The configuration $V_{Sub} = V_{Source}$ is used and the measurement was performed at room temperature under a white light 11 mW/cm^2 irradiance (blue) and in the dark (dark). The gate leakage current remains below the detection limit of 1 nA/mm during all the measurements.

is reduced by the optical excitation, but this has not been investigated in this work. Additionally, there is a discrepancy between the I_{DS} vs V_{DS} and the I_{DS} vs V_{GS} characteristics which highlight the influence measurements conditions on the results. Despite the attention made to measure using a slow V_{GS} and V_{DS} sweeping rate, the large hysteresis effect with the large density of slow interface traps, evidenced in chapter 4, have a detrimental effect on the reproducibility of the measurements. Likewise, the very close I_{DS} vs V_{DS} characteristics at $V_{GS} = -10$ V and $V_{GS} = 0$ V is in good agreement with the Fermi level pinning effect. The modulation of the SCR by the MOS stack becomes inefficient in this bias range.

To account for the drain bias dependent extension of the top SCR, from the MOS gate, and also the one from the back PN junction SCR, a 1D model is used. The potential drop between the drain and source contacts is assumed linear. Therefore, the back SCR extension as function of the position, with $V_{Sub} = V_{Source}$ under light exposure, can be expressed by:

$$W_{SCR,PN}^{Light}(x) = \sqrt{\frac{2\epsilon_0\epsilon_{SC}}{qN_A}[V_{bi} - V_{DS}(1 - \frac{x}{L_{DS}})]} \tag{5.6}$$

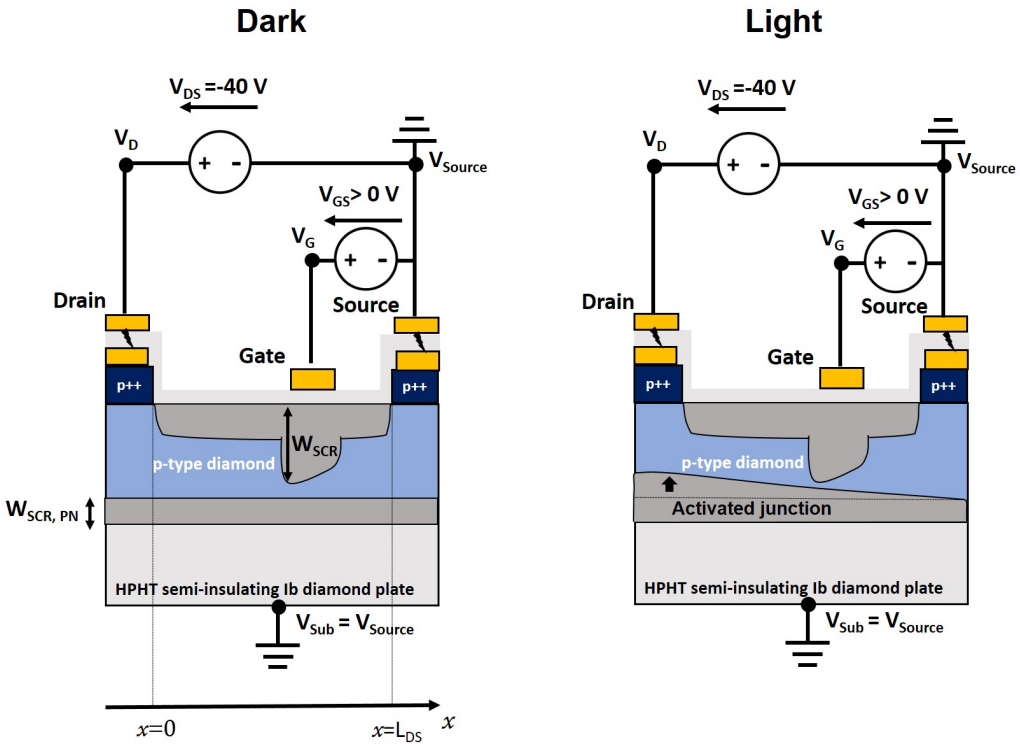


FIGURE 5.12: Schematic cross section of the D3MOSFET at $V_{DS} = -40$ V under light and in the dark. The optical activation of the PN junction causes a stronger pinch-off effect

Where $x = 0$ at the drain contact edge and $x = L_{DS}$ at the source contact edge. At $x = L_{GD}$, where the pinch-off occurs:

$$W_{SCR,PN}^{Light}(L_{GD}) = \sqrt{\frac{2\epsilon_0\epsilon_{SC}}{qN_A}[V_{bi} - V_{DS}(1 - \frac{L_{GD}}{L_{DS}})]} \tag{5.7}$$

In the dark, the potential drop across the junction is V_{bi}. Indeed, the SCR is grounded under light exposure before switching off the light. Then, its thickness is constant and writes:

$$W_{SCR,PN}^{Dark} = \sqrt{\frac{2\epsilon_0\epsilon_{SC}}{qN_A}V_{bi}} \tag{5.8}$$

Similarly, the top SCR extension from the MOS gate at the gate edge ($x = L_{GD}$) expressed by:

$$W_{SCR}(L_{GD}) = \sqrt{\frac{2\epsilon_0\epsilon_{SC}}{qN_A}[V_{GS} - V_{FB} - V_{OX} - V_{DS}(1 - \frac{L_{GD}}{L_{DS}})]} \tag{5.9}$$

Unfortunately V_{FB} is not well defined and may vary significantly between measurements due to interface traps charging effect, in addition to the channel thickness not being well know. Assuming a channel thickness $t_{ch} = 400$ nm, $V_{FB} = 0$ V, $V_{bi} = -3.9$ V, $L_{GD} = 10$ μm, $L_{DS} = 16$ μm and an effective doping level $N_A = 2 \times 10^{17}$ cm^{-3}, the pinch-off voltages V_P at which the drain current saturates are compiled in tab. 5.1 for different V_{GS}.

$V_{GS}(V)$	0	10	20	30
V_P (Light) (V)	-30	-21	-11	-2.8
V_P (Dark) (V)	-75	-56	-34	-10

TABLE 5.1: Calculated V_P for different V_{GS} under light and in the dark.

As it can be seen in fig. 5.11, under light exposure the current saturation due to the pinch-off effect is clearly evidenced. There is a good agreement between the calculated V_P values and the experiment under light exposure despite the rough assumptions of the model. In particular V_P is overestimated at $V_{GS} = 0$ V because the surface pinning is not considered in these calculations. However in the dark the values of V_P are much higher, the observed change of slope is mostly due to a high field mobility saturation effect, similar to the one observed in fig. 5.3 and not due to SCR modulations.

An original corollary is that the back SCR thickness can be modulated under light exposure to tune the threshold voltage to a targeted value. Then, after light extinction the electrostatic of the system remains frozen, being no more dependent of the substrate bias. Any subsequent change of V_{Sub} will not affect V_{TH}, providing a way to control it.

5.2.3 Fixed negative V_{Sub} configuration

In order to decrease the $R_{ON,S}$ the back PN junction can be biased in forward to remove the SCR and then increase the effective thickness of the conductive p-layer. In order to achieve a full channel operation, except for the surface pinning, the condition $V_{DS} - V_{sub} > V_{bi}$ has to be met. This can be done by fixing the substrate to drain potential difference $V_{Sub-D} = V_{bi}$ using an additional sourcemeter, so the SCR is removed. This is not detrimental for the device because the substrate is 0.5 mm thick and highly resistive, the forward current flowing through the back PN junction can be neglected. It was however found to be easier to fix V_{sub} to a value much lower than the minimum V_{DS} measured i.e. $V_{Sub} = -100$ V, while the V_{DS} minimum is -40 V. The obtained transistor characteristics are shown in fig. 5.13. The removal of the back SCR is significantly decreasing the $R_{ON,S}$, from 8.8 Ω.cm^2 to 3.9 Ω.cm^2 at room temperature and from 210 mΩ.cm^2 to 100 mΩ.cm^2 at 250 °C. However, due to the larger thickness that has to be depleted by the gate MOS stack, the threshold voltage is shifted to higher values, from $V_{TH} \approx 30V$ to $V_{TH} > 50V$. The measurement has been stopped at $V_{GS} = +50$ V in order to not damage the gate oxide layer, which tends to break at V_{GS} values ranging between +40 V and +60 V depending on the devices. Thereby the MOSFET could not be switched off in this configuration.

An increase of gate leakage current was observed when heating the sample up to 250 °C, although remaining relatively low. For example, at $V_{DS} = -40$ V and $V_{GS} = 40$ V it was measured at $I_G = 15$ nA/mm which is acceptable. It accounts for the off state drain current, measured for the $V_{sub} = 0$ V configuration with $V_{GS} = 40$ V at $I_D = 11$ nA/mm. The D3MOSFET exhibits a high on state over off state drain current ratio $I_D^{ON}/I_D^{OFF} \approx 5 \times 10^5$ at 250 °C. This is of importance as diamond is the best semiconductor candidate for high temperature applications. The transistor characteristic does not seems to suffer

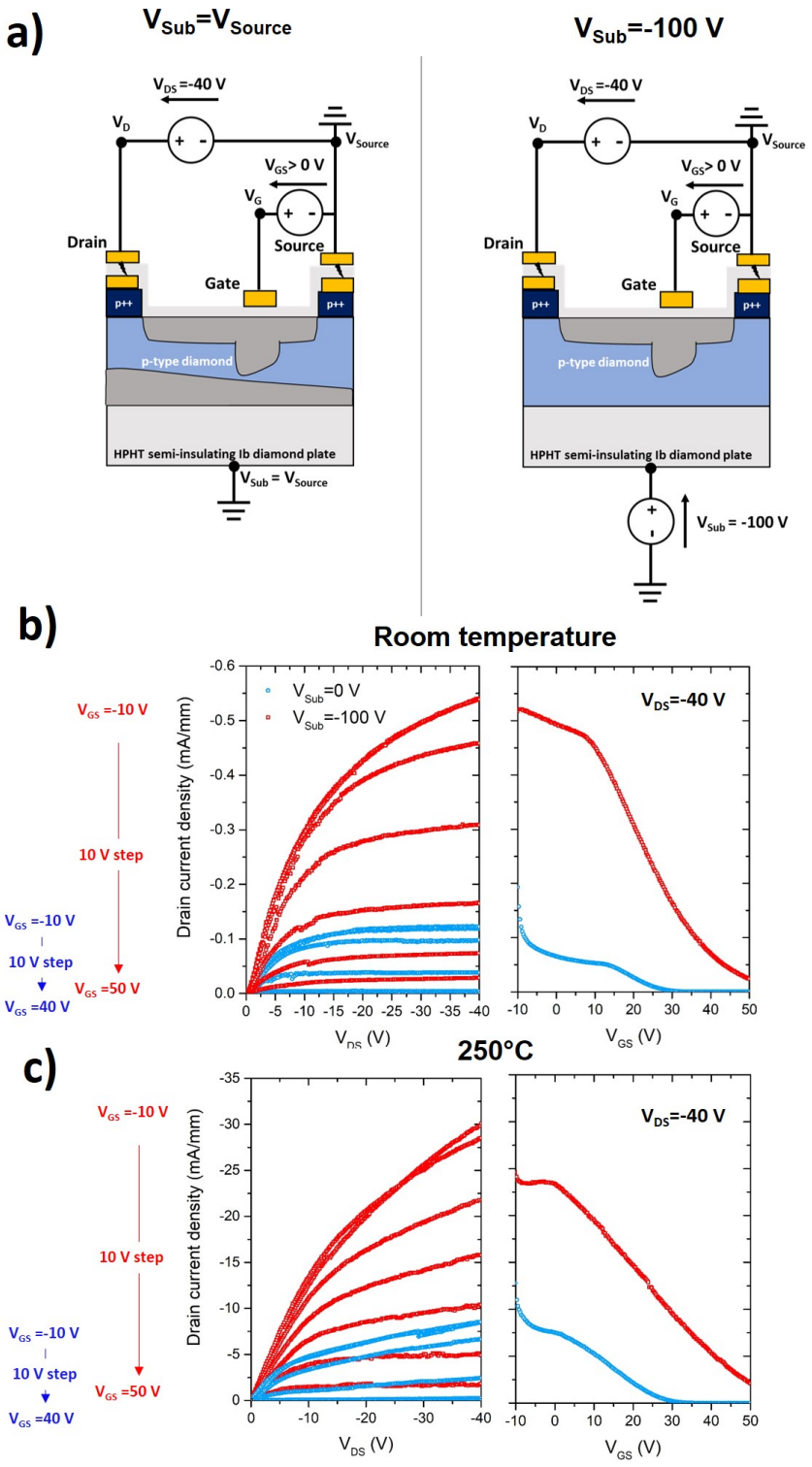


FIGURE 5.13: a) Schematic cross sections of both configurations $V_{Sub} = -100$ V and $V_{Sub} = 0$ V. I_{DS} vs V_{DS} for V_{GS} from -10 V to +40 V with a 10 V step and transfer characteristic I_{DS} vs V_{GS} at $V_{DS} = -40$ V, at b) room temperature and at c) 250 °C under a 11 mW/cm^2 irradiance. The configuration $V_{Sub} = -100$ V (red) is compared with the previously measured with no substrate-source potential difference $V_{Sub} = 0$V (blue).

from such elevated temperatures. Prior to the measurements shown in this chapter, for this particular MOSFET device, the sample suffered several thermal cycles, i.e. heated up to 250 °C and cooled down to room temperature for the need of the measurements. Yet, an excellent I_D^{ON}/I_D^{OFF} is obtained and the gate leakage current is negligible. No particular features could be identified between the first measurements, on the newly fabricated sample, and the last ones months later.

5.2.4 Dual gate $V_{Sub} = V_{GS}$ configuration

The possibility to control the substrate bias allows to use the back PN junction in a JFET mode, as an additional gate. In the dual gate configuration, the top MOS gate is biased synchronously with the back JFET gate to decrease the threshold voltage and the $R_{ON,S}$ is compared with the $V_{Sub} = V_{Source}$ configuration. To simplify the understanding of the measurement, the top gate was shorted with the back gate such that $V_{Sub} = V_{GS}$. In that case, the schematic cross sections in on and off states are shown in fig. 5.14, the $R_{ON,S}$ is reduced for $V_{GS} < 0$ because the back SCR width is decreased, while the top SCR is pinned. At the opposite, for an increasing gate bias both SCR are modulated and the transfer characteristic is clearly exhibiting a significantly lower threshold voltage. According to the transfer characteristics shown in fig. 5.14, from $V_{TH} \approx 30$ V to $V_{TH} \approx 13$ V at room temperature and $V_{TH} \approx 24$ V at 250 °C. The V_{TH} variation versus temperature is still not understood, but its decrease compared to the other configurations is clear. The evidenced $R_{ON,S}$ reduction at $V_{GS} = V_{Sub} = -10$ V is also significant, from 8.8 Ω.cm^2 to 5.6 mΩ.cm^2 at room temperature and from 210 mΩ.cm^2 to 166 mΩ.cm^2 at 250 °C.

The pinch-off voltages can be estimated by considering that $W_{SCR,PN}$ is not gate bias independent anymore:

$$W_{SCR,PN}(L_{GD}) = \sqrt{\frac{2\epsilon_0\epsilon_{SC}}{qN_A}[(V_{bi} + V_{GS}) - V_{DS}(1 - \frac{L_{GD}}{L_{DS}})]} \tag{5.10}$$

This significantly lower the values of V_P compared to the case $V_{Sub} = V_{Source}$.

5.2.5 IIIrd quadrant characteristic

Typical n-type Silicon and SiC inversion-mode MOSFETS have a body diode, which is coming from the structural bipolar PN junction between source (p-type) and drain (n-type). This body diode withstand the drain to source positive bias in OFF state (Ist quadrant), when the MOSFET's inversion channel is not formed. Consequently to this PN body diode, such MOSFETs are not able to reach a OFF state in the IIIrd quadrant, where a reverse current is flowing either through the forward biased PN junction or the inversion channel, or a combination of both, as a function of the gate to source biasing condition (above or below threshold). This can be clearly observed in SiC MOSFET [138], GaN HEMT [139] and other low voltage and high voltage silicon MOSFET.

The reverse conduction in the IIIrd quadrant is quite useful for power converters, where MOSFETs can be used as freewheeling diodes [140]. However, the body diode typically

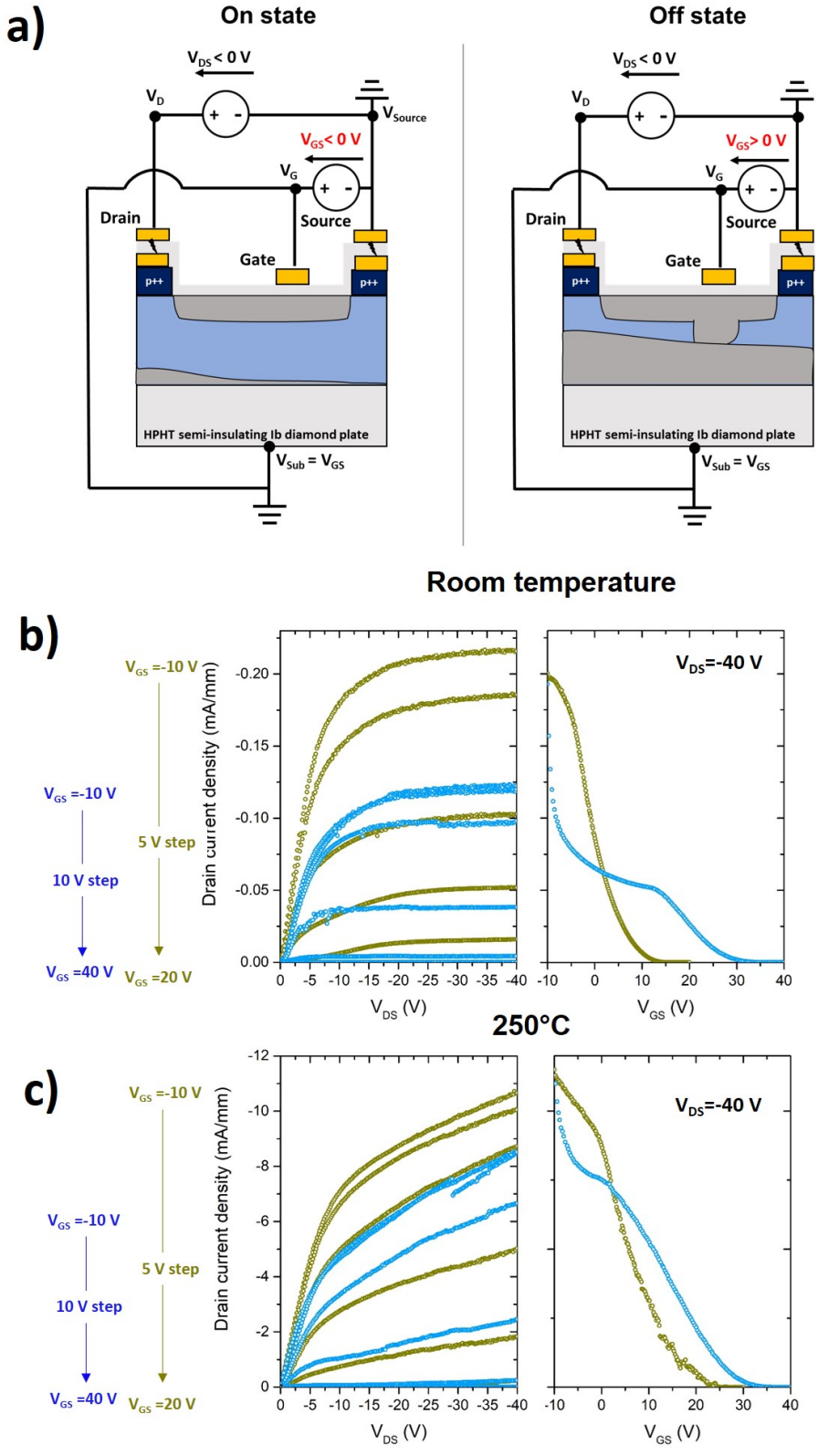


FIGURE 5.14: a) Schematic cross sections of the $V_{Sub} = V_{GS}$ configuration in on and off state highlighting the lower threshold voltage. I_{DS} vs V_{DS} transistor characteristic I_{DS} vs V_{GS} at $V_{DS} = -40$ V, at b) room temperature and at c) 250 °C under a 11 mW/cm^2 irradiance. The configuration $V_{Sub} = V_{GS}$ (green) is compared with the previously measured with no substrate-source potential difference $V_{Sub} = 0$V (blue).

has large ON state voltage drop, especially for low load current and regular or low temperatures. Therefore, the channel conduction in preferred in the IIIrd quadrant, since it typically exhibits lower conduction losses than the intrinsic body diode. Using the reverse conduction of MOSFETs through the inversion channel has been extensively used in low voltage synchronous DC/DC converters ($\leq$ 48 V) with silicon MOSFETs, and is now considered for higher voltages with SiC MOSFETs (>400 V). However, there is a strong risk of "shoot through" in the power commutation cell, where both high side and low side power MOSFETS can be in ON state at the same time, leading to catastrophic failure. Hence, the body diode is used during the dead time.

For all these reasons, it is important to check the ability of the D3MOSFET to operate in reverse conduction (IIIrd quadrant), with a body-diode like and the channel characteristics. Similarly to GaN n-type HEMTs which do not have any PN junction between drain and source, the p-type D3MOSFET can have a body-diode like characteristics. For the normally-on D3MOSFET in the dark or with a controlled substrate bias, so the back SCR is constant, the Ist quadrant is biased in off state at $V_{GS} > V_{TH}$. A current can still flow in the IIIrd quadrant for $V_{DS} > V_{GS} - V_{TH}$, as the channel is opened. When increasing V_{DS}, the SCR reduces and the channel resistance decreases until it becomes negligible in comparison to the drift resistance. The IIIrd quadrant characteristics in the three defined substrate bias configurations are shown in fig. 5.15. Except in the $V_{Sub} = -100$ V configuration, where the off state could not be obtained, the IIIrd quadrant diode-like conduction is clearly measured. This constitute the first demonstration of the IIIrd quadrant conduction in a bulk conduction FET.

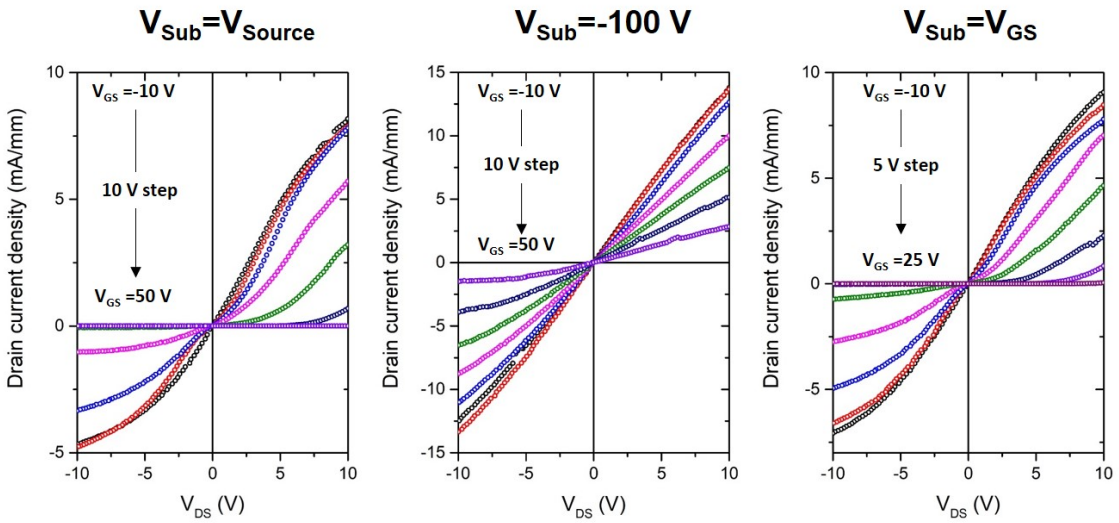


FIGURE 5.15: IIIrd quadrant characteristic of the D3MOSFET at 250 °C in the three substrate configurations, $V_{Sub} = V_{Source}$, $V_{Sub} = -100$ V and $V_{Sub} = V_{GS}$.

5.3 Off state blocking capabilities

The blocking voltage of the device is of particular importance for power devices and is a major advantage of wide and ultra wide band gap semiconductors over silicon. This is however a very challenging parameter to optimize, as the reduction of the electric field crowding effect requires specific architectures such as field plates in lateral devices. Due to the complexity of the fabrication process, it has been decided not to use them and thus a peak electric field is suspected to be present at the gate edge, in the oxide and at the oxide/diamond interface.

5.3.1 Experimental I_{DS} vs V_{DS} in off state

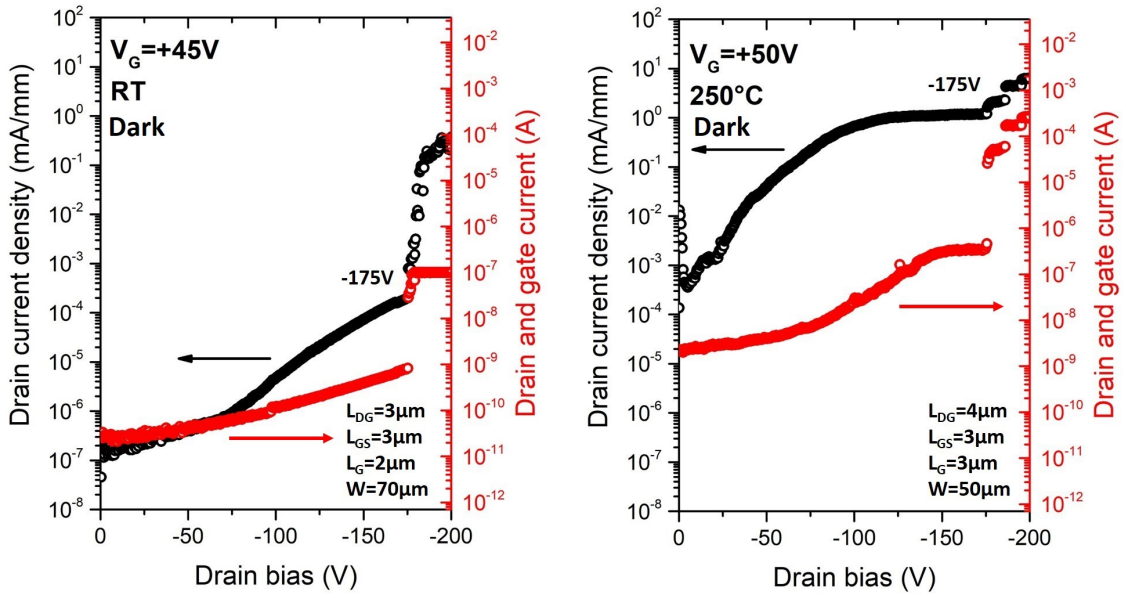


FIGURE 5.16: Breakdown characteristics of two different D3MOSFETs with a rectangular shape at room temperature and 250 °C with $V_{Sub} = V_{Source}$ in the dark. Due to the destructive nature of the breakdown, the same transistor could not be measured several time with different conditions. The drain current density is plotted on left axis and the absolute value of the gate and drain current are plotted on right axis.

The measurement was performed in the dark with the $V_{Sub} = V_{Source}$ configuration. The highest drain to source breakdown voltage was measured to be $V_{BD} = -175$ V ($V_{DG,max} = -220$ V) at room temperature and $V_{BD} = -175$ V ($V_{DG,max} = -225$ V) at 250 °C with the current-voltage characteristics shown in fig. 5.16. The strong increase of the gate current indicates that breakdown occurs in the oxide, as such the avalanche breakdown could not be observed in diamond and the gate is destroyed after the measurement, no modulation of the MOS stack is possible afterwards. At 250 °C, the control of the off state is less efficient, with a gradual reopening of the channel. Nonetheless, the oxide induced

breakdown voltage is clearly identified and these values are close to the one measured on MOS1 sample at $V_{BD} = -200$ V ($V_{DG,max} = -212$ V) for the same doping level value.

At room temperature, the back SCR from the PN junction is "frozen" due to the low carrier concentration in the substrate and it cannot affect the measurement. However, at 250 °C there is a sufficient thermal carrier generation in the substrate to activate it. The drain to substrate potential difference is sustained by the PN junction and a large V_{DS} can induce a significant peak electric field at the junction. It eventually leads to the breakdown, measured to be -160 V in the chapter 3. Even if it was found to induce a negligible substrate parasitic current, the back SCR can be greatly distorted or eventually removed which in turns causes a re-opening of the channel, as observed in the characteristic at 250 °C. It could be fixed by increasing the gate bias V_{GS}, so the removal of the back SCR does not induce an increase of the channel conduction. But, as seen previously, the gate voltage needed to deplete the full epilayer thickness is higher than +50 V and would induce an oxide breakdown.

Improving the blocking characteristic would require specific architectures to reduce the electric field crowding in the oxide, which was not the focus of this work. Due to the nature of the breakdown, the V_{BD} value is dependent on local defects in the oxide, or gate metal lithography imperfections, and thus dispersed between -50 V and -175 V. No correlation was found between L_{DG}, L_G and V_{BD}, in contrast to MESFETs [44] and H-terminated MOSFETs [52], due to the relatively high doping level used. The electric field in the drift region never extends more than L_{GD}.

5.3.2 Simulation of the maximum electric field

In spite of the relatively low breakdown voltage demonstrated here in comparison to other diamond FETs, the maximum electric field in the structure is still high, due to the relatively elevated doping level of the p-type layer. Estimations in fig. 5.17 of this peak electric field value at breakdown voltage had been performed using a 2D finite element simulation tool, and compared with a simple 1D analytical model. The later is believed to give an underestimation of the peak electric field as it omits to take into account edge effects. The physical models developed in chapter 1 have been implemented in the software except for the diamond avalanche effect which is not considered here, as the breakdown occurs prematurely. This simulation relies on solving the Poisson equation in the quasi-static case for each point of a defined grid. It has been performed assuming no fixed or mobile charges in the oxide, or at the diamond/oxide interface, and the substrate is treated as an insulator which is valid in the case of the room temperature measurement in the dark. Implementing these additional effects has been tried, but optimizing the software parameters to an ultra wide band gap material was found to be particularly challenging and the simulation did not converge. As an example, it is challenging to manage the extremely low intrinsic carrier concentration value during calculations, in the order of 10^{-27} cm^{-3} at room temperature.

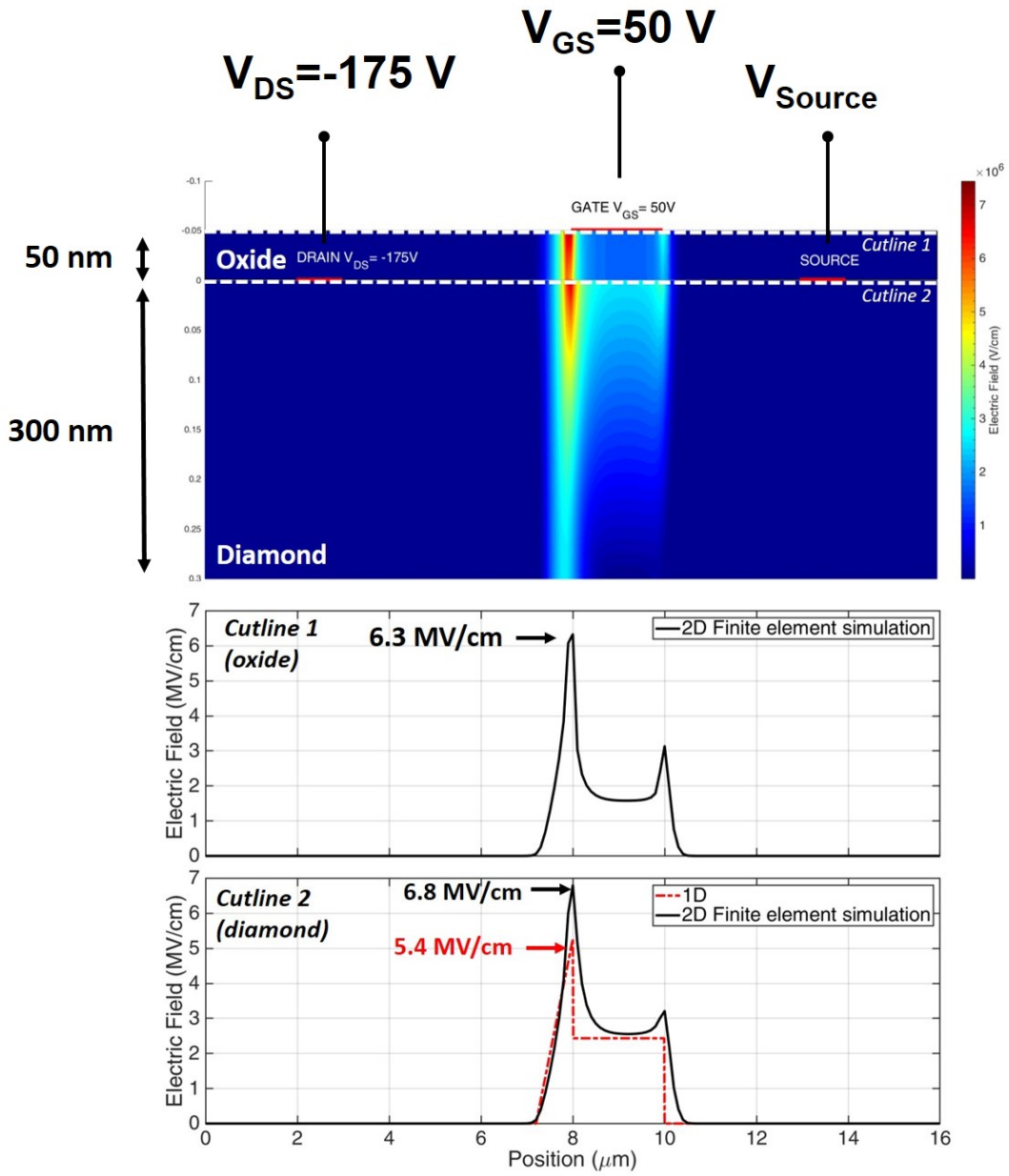


FIGURE 5.17: Finite element simulation of the electric field distribution in off state with a drain bias of -175 V and a gate bias of +50 V. Without a specific field plate edge termination, the electric field crowding effect causes a very high electric field peak under the gate, which reduces the maximum voltage breakdown capability. The lateral electric field profiles on the top surfaces of diamond and oxide are extracted from the above simulation (black) and calculated using 1D electrostatic analysis (red).

The peak electric field value of 6.3 MV/cm calculated in the oxide at breakdown is nonetheless in good agreement with the experimental values measured in MIMCap fabricated on the same sample, shown in fig. 5.18. A simplified structure with no oxide/diamond interfaces has been used to only probe the alumina layer. The 4 measured MIMCaps exhibit breakdown fields between 5.7 MV/cm and 6.3 MV/cm assuming a constant electric field in the oxide, with a reproducible leakage current at first measurement. Successive

measurements on the same MIMCap at high field tends to degrade the alumina layer and the leakage can increase by few orders of magnitude. A maximum electric field of 6.8 MV/cm is calculated in diamond, which is amongst the highest reported in diamond FETs. Yet, it is not enough to observe the avalanche breakdown in diamond. Estimation based on impact ionization rates reported by Hiraiwa et al. [78] suggests that the critical field is about 10 MV/cm, leading to an ideal breakdown voltage of 1 kV by neglecting the edge effects. As for any other semiconductors power devices, improving the breakdown voltage requires the use of specific features such as field plate to reduce edge effects, as discussed previously.

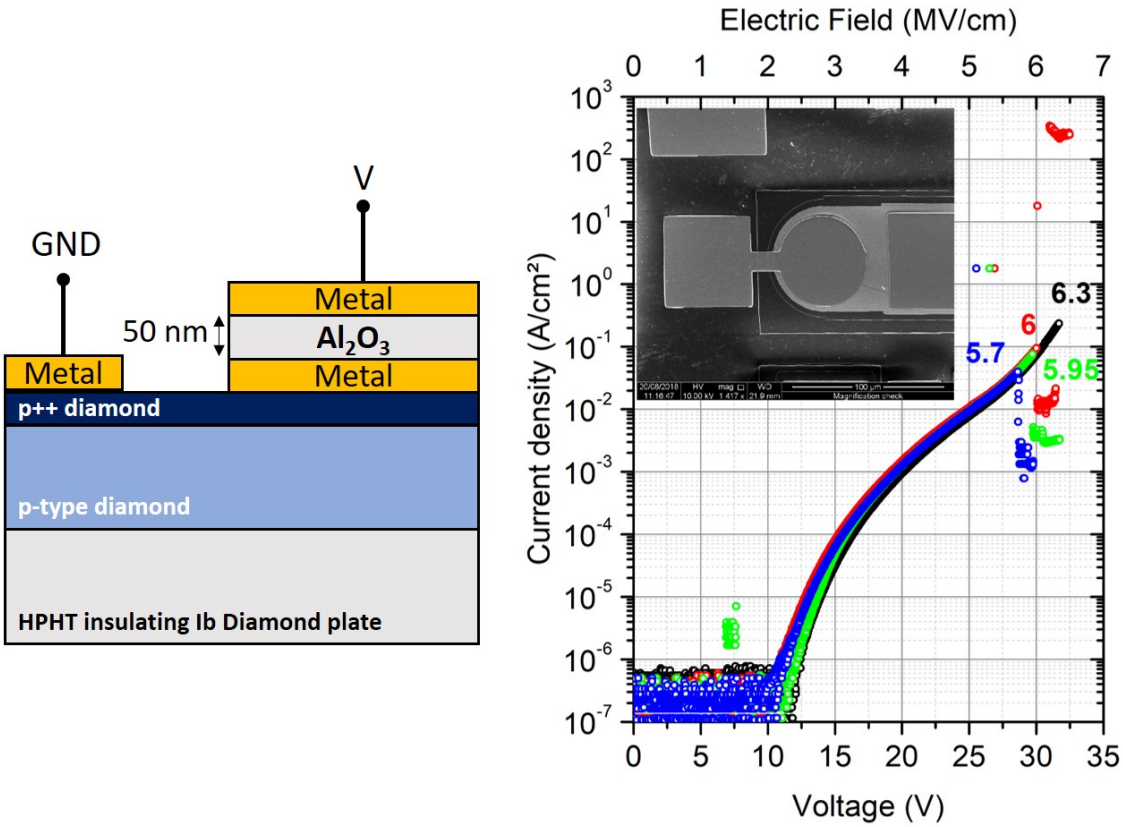


FIGURE 5.18: At left, schematic cross section of the MIMCaps. At right, current-voltage breakdown characteristic at room temperature of 4 MIM-Caps, exhibiting a high destructive breakdown field between 5.7 MV/cm and 6.3 MV/cm.

5.4 The reverse blocking double top-gate lateral D3MOSFET

The single gate D3MOSFET demonstrated up to now is a unidirectional switch, i.e. a ON-OFF switch in the Ist quadrant and a resistor in the IIIrd quadrant. While this asymmetry is an interesting feature for many applications, bidirectional switches that are able to block voltages for $V_{DS} < 0$ and $V_{DS} > 0$ are useful devices for compact matrix converters and other multi-level power converters.

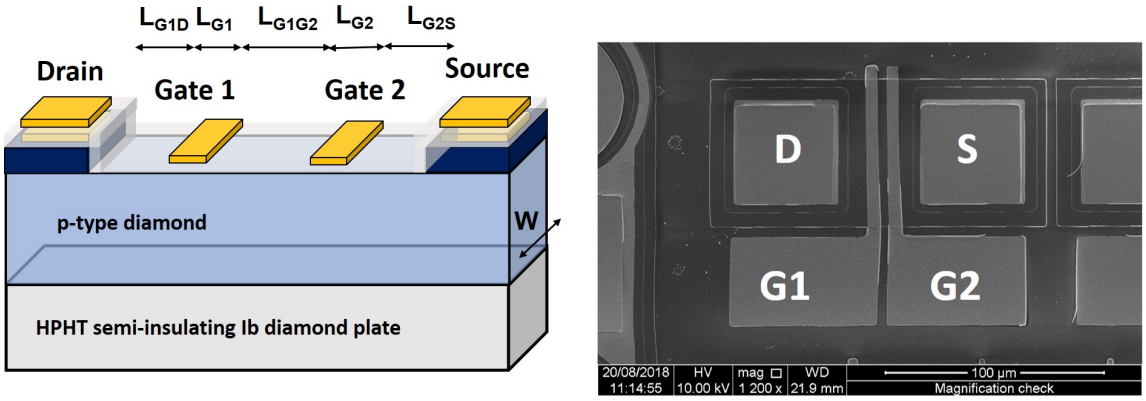


FIGURE 5.19: Schematic representation of the double gate lateral D3MOSFET at left and SEM top view of one of the fabricated device at right. The measured MOSFET parameters are $L_{G1D} = 4$ μm, $L_{G1} = L_{G2} = 2$ μm, $L_{G1G2} = L_{G2S} = 5$ μm and $W = 60$ μm.

The D3MOSFET design can be adapted to be turned into a bidirectional switch by adding an additional gate as shown in fig. 5.19. The working principle of this double gate design is to modulate the gate 2 if $V_{DS} < 0$ so the drift length is $L_{G1D} + L_{G1} + L_{G1G2}$ and to modulate the gate 1 if $V_{DS} > 0$ so the drift length is $L_{G1} + L_{G1G2} + L_{G2S}$. In this second case, we can consider that the drain and source contacts defined in fig. 5.19 are inverted since the current is flowing in the opposite direction. So that, the unused gate does not significantly affect the measurement, its potential is equal to the closest contact, which acts as a drain. Since this gate is close to the drain, their potential difference is small and its SCR extension is assumed much smaller than the one created below the modulated gate.

The operation of this device requires 4 probes and an additional one to control the substrate, however the measurement set-up used is limited to four. For this fist demonstration the substrate has then been left floating, a micro-bounding of the back contact to a connector will eventually be done to solve this issue. When a change of the sign of V_{DS} occurs in this device, the switching of the modulated gate has to be done by a gate driver. However it was not possible at that time to realize this kind of integration of the device, instead its expected IV characteristic is reconstructed from two separate measurements shown in fig. 5.20. A dual channel Keithley 2612 is used to record both I^{st} and III^{rd} quadrant of each configuration where either the gate 1 or 2 is modulated, switching manually between the two. Then, only their respective I^{st} quadrant are kept to reconstruct the final double gate D3MOSFET transistor characteristic, shown in fig. 5.21 at 250 °C.

Due to the floating substrate, the asymmetry of the device and imperfections caused by the fabrication process, the measured transistor characteristics of the two configurations are not identical, with a different gate leakage current of 100 nA/mm in gate 2 and 217 μA/mm in gate 1 at $V_G = 50$ V. However, the on resistance is almost the same in both cases, 152 mΩ.cm^2 in configuration A and 159 mΩ.cm^2 in configuration B.

This design working principle has been demonstrated, but further improvements in

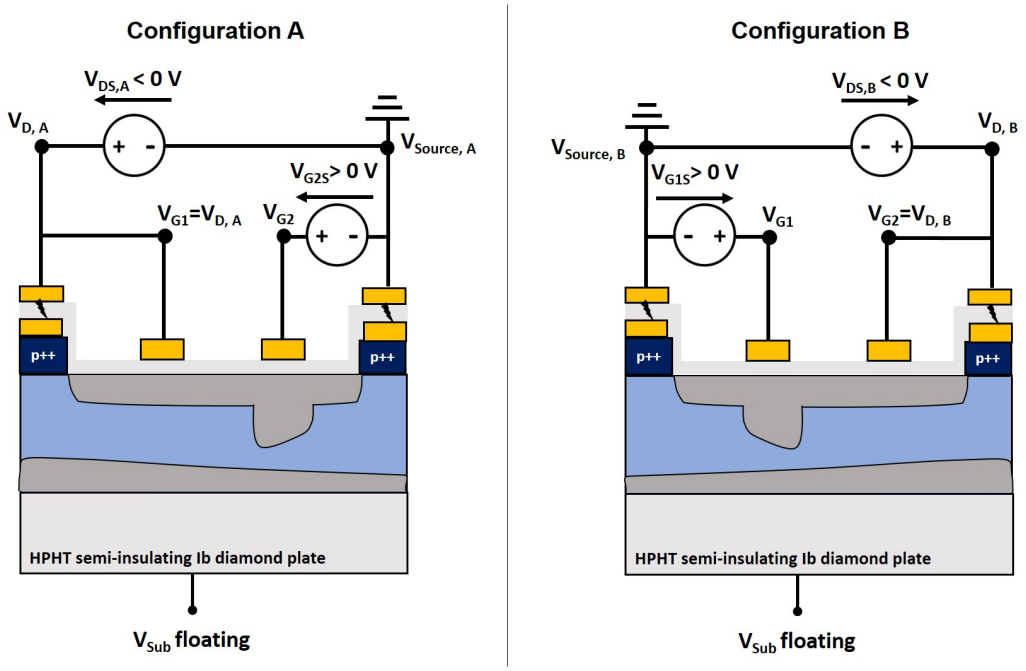


FIGURE 5.20: Schematic representation of the double gate lateral D3MOSFET in the 2 configuration tested. When one of the gate is controlled, the other one is shorted with the closest ohmic contact. Because the experimental set-up is limited to 4 probes, the substrate is left floating.

terms of interface and oxide control are required to make it reliable. In particular, it has been observed that a gate oxide failure would often occur in one of the two gates for $V_G >$ 40 V, making difficult to measure both configurations A and B transistor characteristics. For this reason in addition to the limited number of double gate devices fabricated on the sample, the off state capability could not be evaluated.

5.5 Effect of the interface charges on the D3MOSFET commutation

Because of the large emission time constant of interface traps, their effect is particularly detrimental on the performances during commutation of the D3MOSFET. The experimental setup used is described in fig. 5.22 a), the $V_{Sub} = V_{Source}$ configuration is used with a fixed low drain-source bias, i.e. $V_{DS} = -1$ V, to not observe pinch-off effect. The transistor commutation is performed by applying a square signal of 2 s period on the gate, $V_{GS} = 0$ V in on state and +40 V in off state. Then, the waveform of I_D is measured by using a current-voltage converter, in order to get a voltage at the input of a 16-bit resolution oscilloscope. The obtained signal data are then converted back to current values and normalised by the quasi-static drain current value $I_{D,max}$. Both V_{GS} and $I_D/I_{D,max}$ waveforms are shown in fig. 5.22 b), with light exposure and in the dark.

It is assumed that in the dark the back PN junction electrostatic is frozen. Therefore the commutation durations to switch from off to on state t_{ON} and from on to off state t_{OFF}

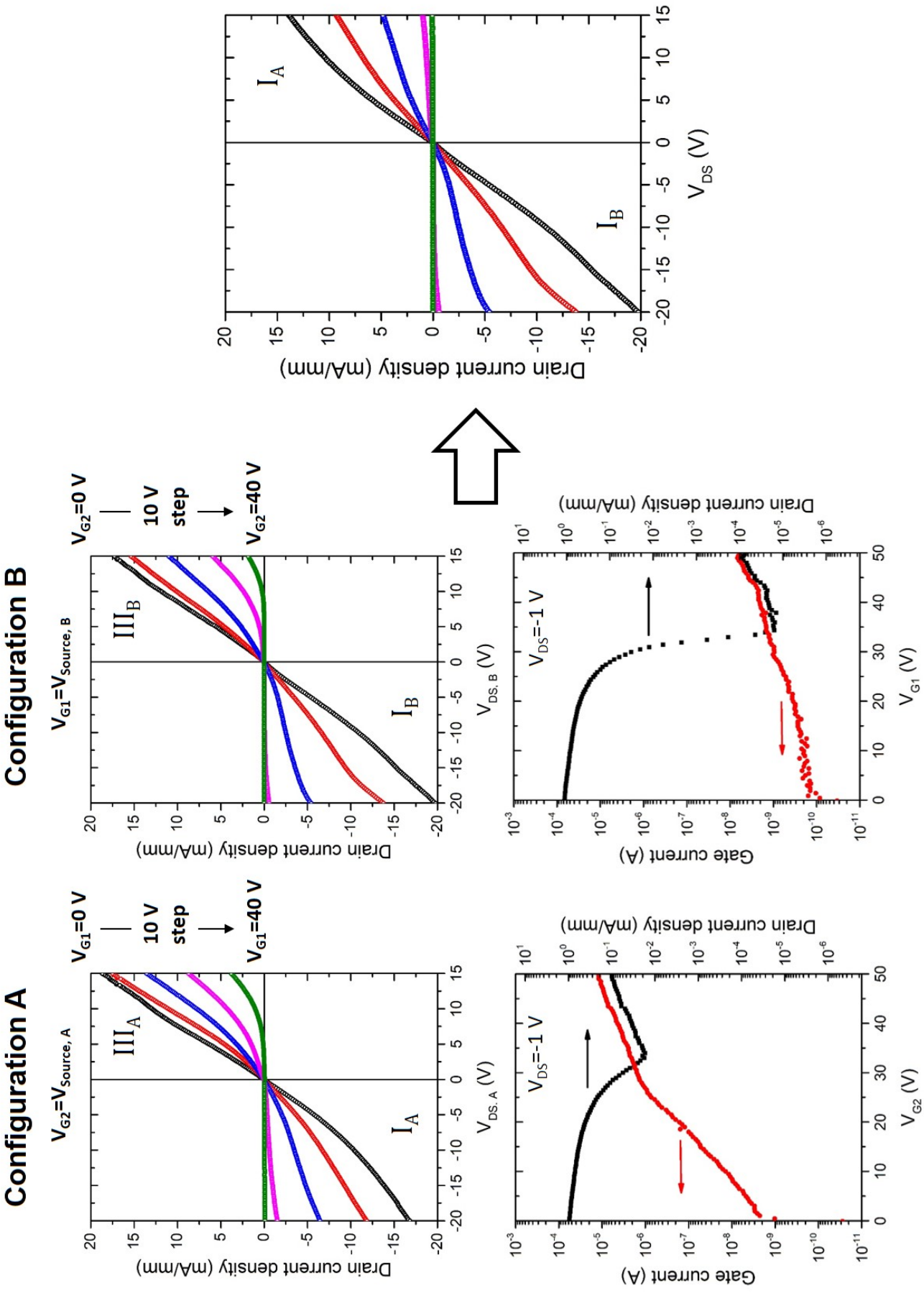


FIGURE 5.21: Transistor characteristic at 250 °C in the 2 configurations, separately testing the 2 gates. The I^{st} quadrant of each configuration are then use to reconstruct the transistor characteristic of the double gate lateral D3MOSFET. At the bottom, the transfer characteristics of each gates at $V_{DS} = -1$ V are shown with the gate leakage current.

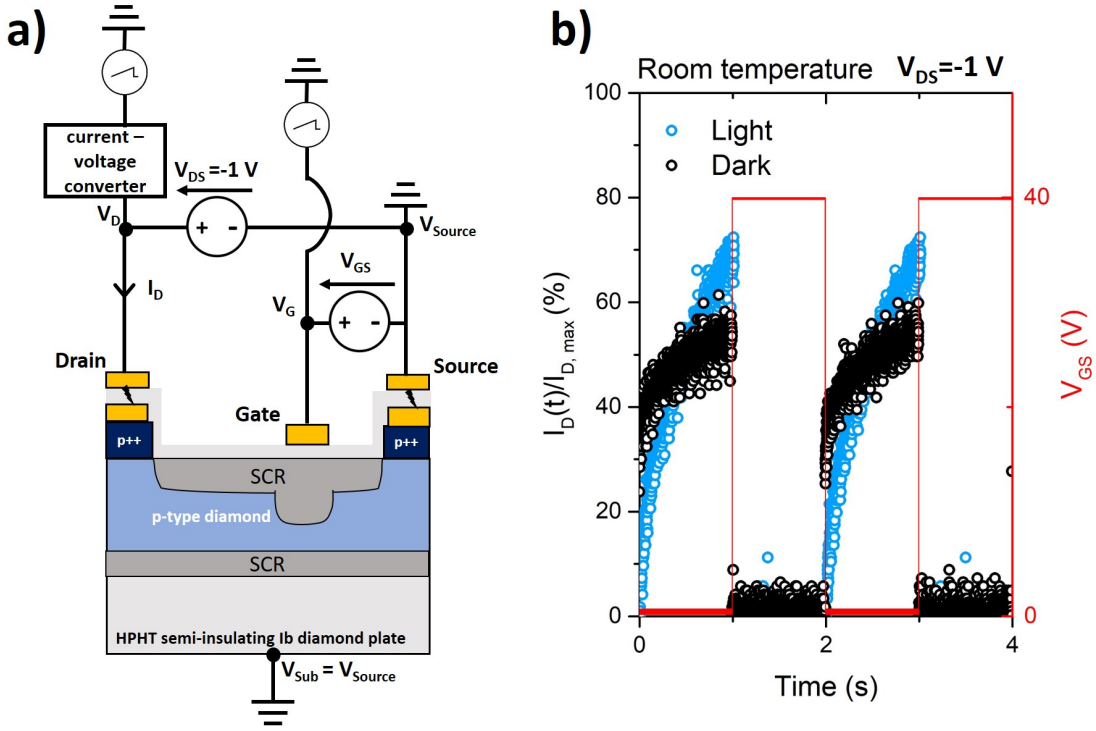


FIGURE 5.22: a) Experimental setup and schematic cross section of the D3MOSFET operated in the $V_{Sub} = V_{Source}$ configuration with fixed $V_{DS} = -1$ V. V_{GS} and I_D are monitored using a 16-bit resolution oscilloscope. To obtain the waveform of I_D, a current voltage converter is used to get a voltage at the input of the oscilloscope. b) Obtained room temperature waveform of I_D, normalised by the quasi-static current $I_{D,max}$ in dark and light conditions. The V_{GS} square signal (in red) has a 40 V amplitude, from 0 V (on state) to +40 V (off state). The period of the signal is 2s.

are only related to the MOS gate. Due to the large density of slow traps in the MOS stack, both in the dark and with light, t_{ON} is long. After 1s duration in on state at $V_{GS} = 0$ V, $I_D/I_{D,max} = 50$ % in the dark and $I_D/I_{D,max} = 65$ % with a white light optical excitation. The effect of light on these traps is not understood at the moment but seems to play a significant role on the waveform. When V_{GS} is biased from +40 V to 0V, these traps emit electrons to the valence band with large time constants, however in the opposite direction, when V_{GS} is biased from 0 V to +40V, the traps capture time constants are much smaller. It results in a lower t_{OFF} than t_{ON}, that could not be characterized due to the limit of the measurement setup. The Modulab Solartron, used to generate the V_{GS} waveform, is not able to produce a square signal with a low enough dV_{GS}/dt for period durations below 1 ms. Therefore, t_{OFF} is evaluated to be below 1 ms.

These are only preliminary measurements that need to be completed, in particular as function of temperature. However, they already demonstrate the importance to control the measurement conditions as well as the critical importance of reducing the trap density in the MOS stack. Identifying the traps origin is of importance to understand what need to be improved in the fabrication process.

5.6 Conclusion and roadmap

The successful operation of the D3MOSFET with diamond selective growth and mesa etching has been achieved. It has been demonstrated, thanks to specifically designed structures, that the contact resistance has been reduced to a negligible value, $\rho_C = 7 \times 10^{-5}$ $\Omega.cm^2$, in regards of the device total resistance (typically two orders of magnitude higher). This allowed to measure the resistivity of the diamond p-type layer, which is found to be well described over five order of magnitude by the hole mobility and carrier concentration models developed in chapter 1, with a compensation of $N_D = 1 \times 10^{16}$ cm^{-3} for a doping level of $N_A = 2 \times 10^{17}$ cm^{-3}.

The measured transistor characteristics of the fabricated single gate and double top-gate D3MOSFETs have been measured in the I^{st} and III^{rd}, from room temperature to 250 °C, exhibiting a transistor effect. Thanks to the demonstrated n-type nature of the substrate under light or high temperature condition, the substrate bias effect on the device characteristics has been quantified. The on state resistance R_{ON} and the pinch-off voltage V_P were found to significantly vary depending on the substrate bias. However, reproducibility of the measurements is still difficult to achieve due to the large back PN junction time constant to reach equilibrium, in the order of the second. Traps with long emission time constants in the MOS stack are also particularly problematic in this regard. Slow measurements are then required to be close to the quasi-static condition.

The lowest specific on state resistance was measured at $R_{ON,S} = 50$ $m\Omega.cm^2$ at 250 °C [141], while keeping a channel closure. However, this measurement was performed in the dark and the substrate was left floating. Due to the destructive nature of the breakdown, occurring during the I_{DS} versus V_{DS} measurement in off state, a substrate controlled transistor characteristic could not be obtained on this particular device.

The maximum breakdown voltage was measured to be $V_{BD} = -175$ V [141], corresponding to a peak electric field superior to 5.4 MV/cm (estimated at 6.8 MV/cm by 2D finite element simulation) in the diamond. As expected, the breakdown occurred in the oxide layer due to its lower breakdown field, measured to be 6.3 MV/cm without considering edge effects, and the lack of edge termination features. Nonetheless, this value is much larger than in silicon (0.2 to 0.8 MV/cm), SiC and GaN ($\approx$ 3 MV/cm). Thanks to gate oxide control, in most of the devices tested the gate leakage current remained below 1 nA/mm at room temperature and in the order of 10 nA/mm at 250 °C. Large variations from one device to an other are however observed, with values that can vary by several orders of magnitude due to local defects in the oxide.

The performances of the D3MOSFET are compared to the other demonstrated diamond power FETs in terms of the R_{ON} vs V_{BD} trade-off in fig. 5.23. All of these devices have a lateral design, due to the constraints of the fabrication process or due to the use of a 2D hole gas as channel. The estimated optimal performances of the lateral and vertical design are based on the 1D models of the first chapter with a 50 nm oxide layer and a threshold voltage $V_{TH} = 15$ V. It has been assumed that the drift layer resistance is much higher than the channel resistance and that $L_{SD} \approx L_{GD}$. For the vertical design, only the

bulk conduction is considered and the R_{ON} could be further decreased by operating it in enhancement mode. As it can been seen, all shown devices require optimizations to fully take advantage of the diamond capabilities. The next key step toward demonstrating outstanding performances is a better electric field crowding effect management, by the use of edge terminations. The measured D3MOSFET breakdown is a factor 5 below the calculated 1D breakdown of diamond. On the longer term, the vertical design is well known to be more suited than the lateral one to reduce the electric field crowding. The maximum current per chip surface area is also much higher than in the lateral design.

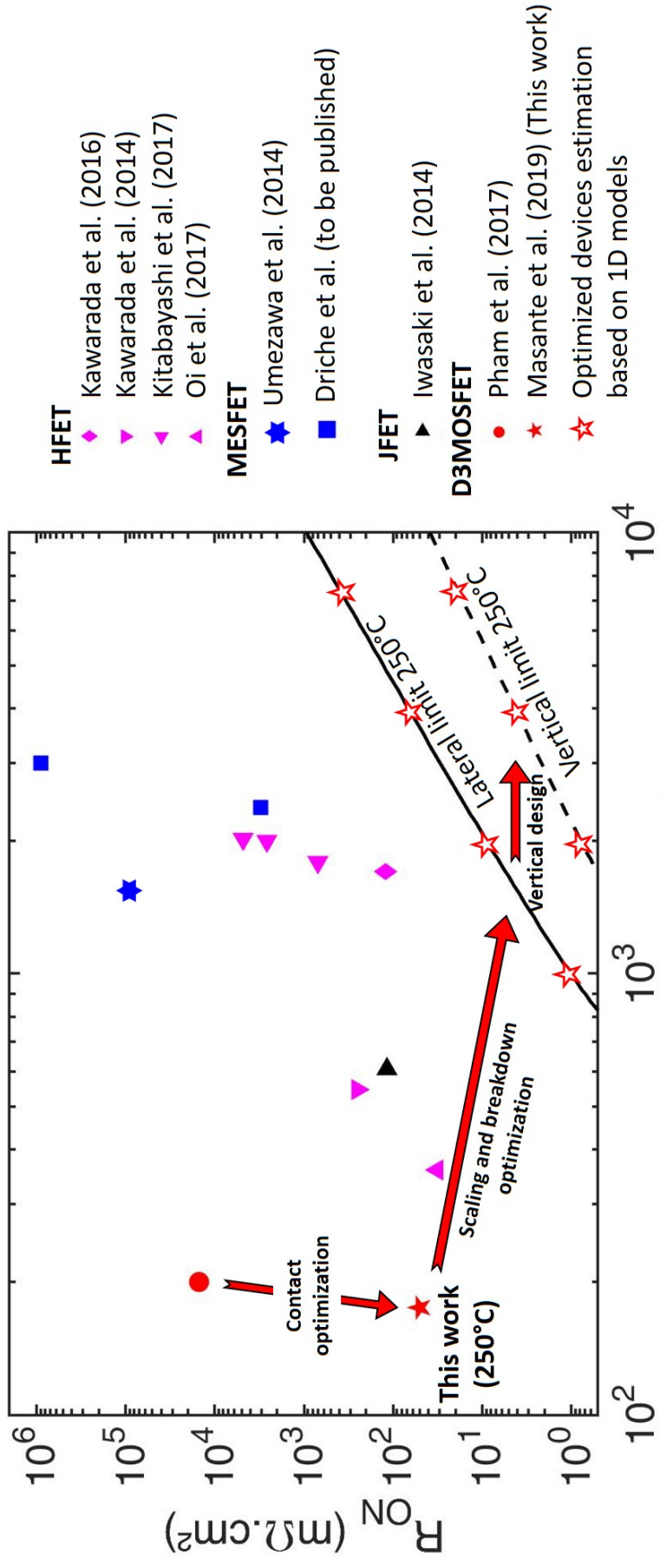


FIGURE 5.23: $R_{ON,S}$ vs V_{BD} performances of reported power diamond FETs in the literature, compared to the expected performances of the optimized lateral and vertical design of the D3MOSFET at 250 °C. Improvements from the previous work of T. T. Pham et al. thanks to the contacts optimization is shown, along further performance gains that can be achieved with an improved sizing, electric field crowding management and a change to the vertical design. Experimental points are taken from ref. [52, 54, 45, 53, 44, 16, 49, 141].

General conclusion

Diamond power MOS transistors relying of the original time stable deep depletion property of wide band gap semiconductors were fabricated and characterized.

- The design optimization was first discussed and established in chapter 1, using state of the art physical model from literature. In this chapter, only 1D equations were used and no parasitic effects were considered to provide the expected performances in terms of conductivity and blocking voltage capabilities of the simplest lateral design. Lateral structure was chosen over vertical due its challenging fabrication process at the moment, particularly because of the difficulty to grow defect-free thick epilayers and the limitations of the diamond etching process available. In real devices, parasitic charging due to defects and 2D geometrical effects can significantly deteriorate the transistor's performances, but would require to develop reliable simulation tools adapted to diamond and ultra wide band gap materials in general to take into consideration. Still, this simplified analysis provide useful guiding lines for device design and allow to extrapolate the performance of the vertical architecture, showing the potential of diamond as leading material for next generations of power devices.

- In chapter 2, the fabrication process was detailed with the aim at reducing the contact resistance compared to the first demonstrated D3MOSFETs by T. T. Pham, by using selectively grown heavily doped diamond at source and drain contacts. A mesa etching was also performed with a threefold objective: (i) reducing the surface area of the gate contact on the conductive p-type channel, (ii) electrically isolate the gate metal pad from the p-type layer, in order to prevent damages caused by contacting the probe tips, and finally, (iii) isolate devices from each others. The challenges involved in processing diamond samples were discussed and one sample has been successfully achieved containing MOSFETs, MOSCaps, MIMCaps and specific structures for resistivity and contact resistance extraction.

Prior to the transistor measurements analysis, interface related effects having a substantial impact of the device characteristic were identified. The comprehension of their physical mechanisms are key for future improvements.

- First, in chapter 3, the influence of the substrate was evidenced. It has been several times mentioned that a SCR could be present at the interface between a p-type diamond and a nitrogen doped semi-insulating substrate, due to its n-type nature with very deep donor (> 1.45 eV). The PN junction was evidenced in this work by electrical transport measurements, showing that this material has conductive properties

under white light optical excitation as well as at high temperature. Under such experimental conditions, the junction can be controlled and is well described by a one sided, abrupt PN junction model. A breakdown could be observed at an estimated critical field of 5.2 MV/cm, without taking into account 2D effects inducing peak electric field at the edge of contacts. Despite the unoptimized structure, this value is larger than in other common wide band gap semiconductors (GaN and SiC) and is amongst the highest reported in a diamond devices. It has been deduced that controlling the substrate bias is necessary to correctly interpret the measurements.

- Then in chapter 4, parasitic charging effects occurring at the Al_2O_3/diamond interface traps were investigated, using MOSCaps and MIMCaps structures, by impedance analysis. Large densities of traps were demonstrated, superior to 10^{13} $cm^{-2}.eV^{-1}$, causing a large discrepancy between the ideal MOSCap characteristic and the experimental one. In particular, the Fermi level pinning effect prevented to obtain the accumulation regime that could be a key achievement toward efficient diamond MOSFETs devices. Unfortunately, the experimental methods employed in this work are not well adapted to extract the exact value of the density of interface states, for this order of magnitude. It thus led to a discussion, and reconsideration, on previously reported observations of accumulation regime in O-terminated MOSCaps in the literature, making use of impedance measurements. Reducing the defect density at this interface is challenging, yet obtaining trap densities in the order of 10^{10} to 10^{11} $cm^{-2}.eV^{-1}$ or lower is necessary to match the strict requirements for electronic devices.

Finally, the D3MOSFET devices was characterized with particular attention to the substrate bias and experimental conditions.

- In chapter 5, a D3MOSFET was characterized as function of temperature for different substrate bias configurations. The resistivity of the channel and drift lightly doped p-type layer as function of temperature was extracted. An excellent agreement with the state of the art models used in chapter 1 was found, exhibiting the expected negative temperature coefficient, due to incomplete ionization of dopant. Contact resistances between the metal and the selectively grown, heavily doped, p-type diamond was shown to be negligible in regard to the channel and drift resistances. This work validated the use of the selective growth technique as a solution for the source and drain contact formation.

  Successful transistor characteristics, with excellent on state current over off state current ratio in the order of 10^5, were obtained both at room temperature and at 250 °C. This achievement was possible thanks to the optimization of the Al_2O_3 deposition process, and also the post annealing, developed successively by G. Chicot, A. Marechal and T. T. Pham. The high temperature operation is key for diamond power devices, indeed, many applications could take advantage of its low intrinsic

carrier concentration and its superior thermal conductivity, in order to reach operation temperatures well above the silicon limit at $T \approx 175\,°C$ with a limited cooling system size.

A better understanding of the D3MOSFET transistor characteristics has been achieved, thanks to the control of the n-type substrate/p-type epilayer junction electrostatic. The lowest $R_{ON,S}$ was measured to be $R_{ON,S} = 50\ m\Omega.cm^2$ at 250 °C and is shown in fig. 5.24 [141], with a drain-source breakdown voltage $V_{BD} = -175$ V, corresponding to an outstanding 6.8 MV/cm calculated maximum electric field. However, this measurement was performed in the dark and the substrate was left floating. Due to the destructive nature of the oxide breakdown, a substrate controlled transistor characteristic could not be obtained on this particular device.

Controlling the back PN junction with the substrate opens new possibilities, removing completely this SCR by biasing it in forward is possible without injecting any significant current in the device due to its high resistivity. It allows to lower, for example in the described device of this work, $R_{ON,S}$ from 210 $m\Omega.cm^2$ to 100 $m\Omega.cm^2$ at 250 °C. The $R_{ON,S}$ reduction however comes at the cost of a higher threshold voltage, because the channel thickness to deplete is increased.

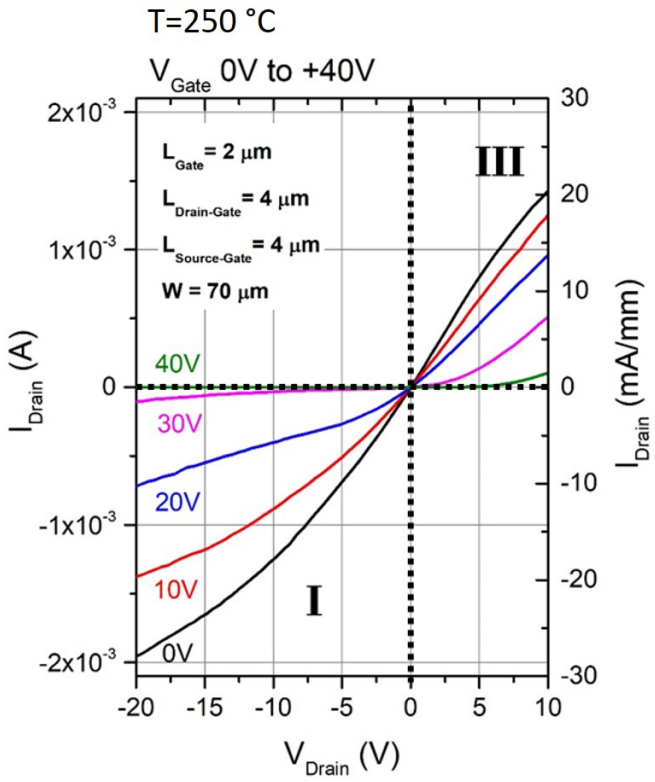


FIGURE 5.24: Measured current-voltage characteristic of one of the fabricated D3MOSFETs at 250°C, exhibiting a minimum specific on state resistance of $R_{ON,S} = 50\ m\Omega.cm^2$, the substrate was left floating. Published in ref. [141] Copyright ©2019, IEEE

5.7 Perspectives

Open questions need to be addressed in the near future to bring the D3MOSFET toward its full capabilities:

- Are there bulk diamond or bulk oxide traps in addition to diamond/oxide interface states?
- What is the impact of the selective growth process on the diamond surface?
- How the surface miscut angle and polishing affect the diamond/oxide interface
- Is there a more suited oxide than alumina to lower the interface state density?
- How to improve to blocking voltage capability of the device and the oxide?

Part of the answer to these questions could be provided by DLTS analysis of MOSCap devices, lacking in the literature. To that end, a DLTS setup is coming toward the end of 2019 in our group, with a high temperature controller up to 800 K and a window to use optical excitations in the visible range. Both high temperature, above our current setup limit of 300 °C, and optical excitation would be interesting to probe traps deep in the diamond band gap. Furthermore, SiO_2 deposited by ALD seems to form a better interface, but with little evidence at the moment. A comparison of SiO_2 and alumina MOSCap's CV, Cf and IV characteristics as function of temperature would provide some answers regarding the use of SiO_2 in diamond devices. Additionally, the UV ozone treatment might not be well optimized to oxidize the diamond surface. Because oxygen atoms are bigger than carbon atoms, it is assumed than the diamond surface is not fully oxidized and carbon dangling bonds remains, inducing interface traps in MOSCaps devices. Other surface treatments need to be investigated, with other species or with a mix of hydrogen and oxygen atoms. Because hydrogen is small the surface coverage is much better, but the impact on the electron affinity has to be quantified.

On the longer term, the development of the diamond MOSFET has several challenges to overcome:

- The fabrication of larger area device, in the order of the mm^2, is possible regarding the available substrate size and is necessary to reach current in the order of a few A. This is the typical current rating necessary to demonstrate the use of a diamond MOSFET in a power converter system. This, of course, require extensive optimization of the fabrication process to lower the defect density in the oxide and diamond epilayers.
- To improve the lateral design by using the recess gate architecture and edge terminations to optimize the blocking voltage. These features are key to demonstrate the high estimated diamond performances.

- The fabrication of a vertical D3MOSFET, the example of vertical design shown in chapter 1 is reminded in fig. 5.25. This architecture has performances well beyond that of the lateral architecture, in terms of current integration by chip surface area. This however represents a challenge to achieve its fabrication: (i) the growth of defect-free thick epilayers (several μm), (ii) a well controlled etching process over thicknesses of several μm, (iii) the optimization of the lithography process to make it accurate and reliable despite the small substrate size.

The global feeling of myself, and our research team, is that the progress achieved in recent years in diamond electronics are showing its interest for power electronics. More generally, the industry is opening up to the use of wide band gap semiconductors, the interest on these materials is growing. Moreover, diamond as semiconductor is not limited to high power applications. Bio-sensors and particle detectors are also innovative active fields of research, playing a significant role in the basic understanding of diamond physics.

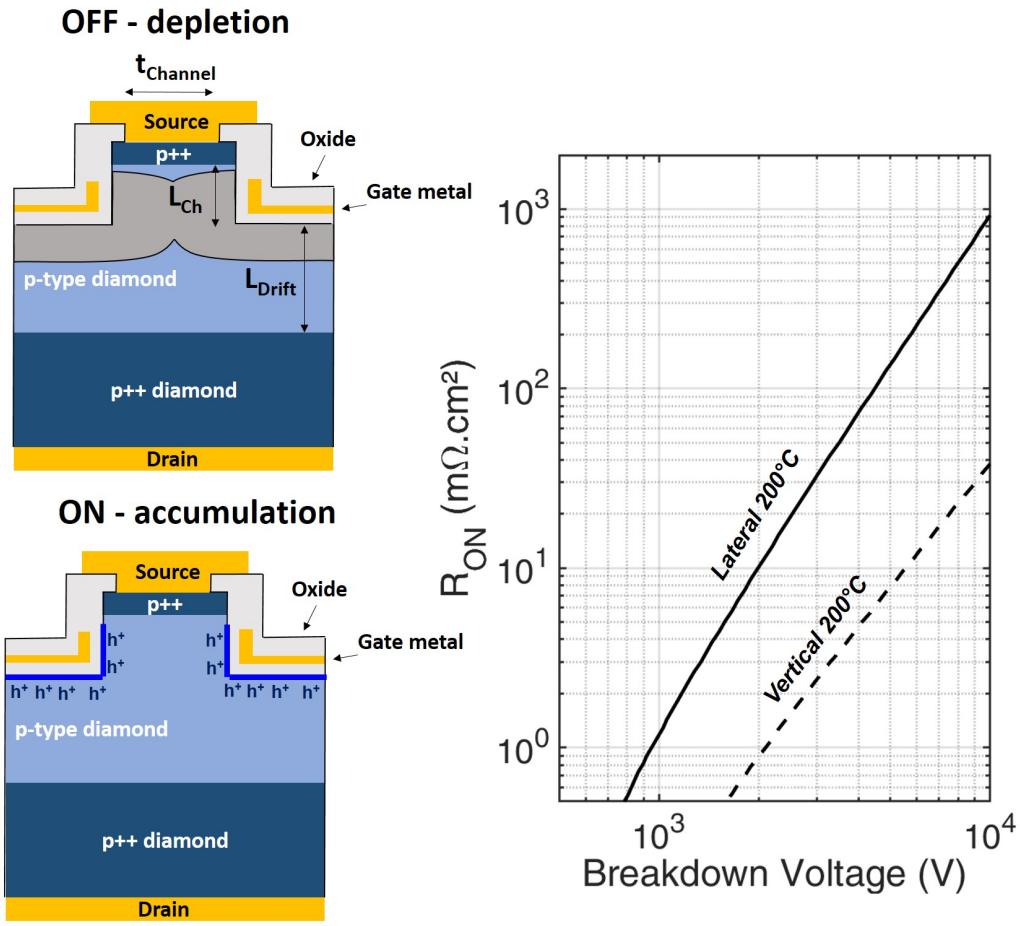


FIGURE 5.25: Schematic cross section of the vertical diamond depletion MOSFET proposed architecture and its calculated R_{ON} vs V_{BD} trade-off compared to the lateral architecture at 200 °C with t_{ox} = 50 nm and V_{TH} = 15 V.

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- **C. Masante** (oral), M. Kah, N. Rouger and J. Pernot, "Optically modulated PN diode with nitrogen doped diamond", 30th International Conference on Diamond and Carbon Materials 8-12 September 2019, Melia Lebreros, Seville, Spain.
- **C. Masante** (poster), J. Pernot, J. Letellier and D. Eon, "175V, > 5.4 MV/cm, 50 mΩ.cm^2 at 250°C Diamond MOSFET and its reverse conduction", 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), Shanghai.
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Diamond MOSFET for power electronics

In the context of a growing need for power semiconductor devices, as more and more applications from motor drives to power grids requires DC/AC, AC-DC or DC-DC converters with higher efficiencies and higher power densities, the research on new solutions is essential. Wide band gap materials have already shown their superior physical properties for this kind of applications, due to their ability to sustain larger current power densities and voltages compared to silicon based devices. Amongst them, diamond is an ultra-wide band gap material (5.5 eV) with one of the highest critical electric field capability , which coupled with its great thermal conductivity (22 W/cm.K) and hole mobility (2000 $cm^2/V.s$) makes it a particularly interesting semiconductor for power electronics. Despite the challenging fabrication of diamond based devices due to the small standard substrate size (a few mm^2), diamond is still being actively studied with constant progresses.

This thesis is focused on the design , fabrication and characterization of diamond Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) which takes advantage of the wide band gap of diamond to design an original device architecture based on a stable deep depletion regime. The design optimization of such devices will be established according to the state of the art physical models, then experimental test devices will be analysed to better understand the physics of the diamond MOSFET. Finally, a performance evaluation in comparison to other semiconductors and existing diamond devices will be presented. Several perspectives from these performances as well as from original architectures specific to diamond will be drawn.

Transistor MOS en diamant pour l'électronique de puissance

Dans le contexte d'un besoin croissant de dispositifs semi-conducteurs de puissance, étant donné que de plus en plus d'applications, des moteurs aux réseaux de ditribution électriques, nécessitent des convertisseurs DC/AC, AC-DC ou DC-DC avec des rendements et des densités de puissance de plus en plus élevées, la recherche de nouvelles solutions est essentielle. Les matériaux à large bande interdite ont déjà démontré leurs propriétés physiques supérieures pour ce type d'applications, en raison de leur capacité à supporter des densités de courant et des tensions plus élevées que les dispositifs à base de silicium. Parmi eux, le diamant est un matériau à ultra-large bande interdite (5,5 eV) avec l'un des champ électrique critiques le plus élevé, ce qui, associé à sa grande conductivité thermique (22 W/cm.K) et à sa mobilité des trous (2000 $cm^2/V.s$) en fait un semi-conducteur particulièrement intéressant pour l'électronique de puissance. Malgré la fabrication difficile des dispositifs à base de diamant en raison de la petite taille des substrats disponibles à l'heure actuelle (quelques mm^2), le diamant est toujours activement étudié avec des progrès constants.

Cette thèse porte sur la conception, la fabrication et la caractérisation de Transistors Métal-Oxyde-Semiconducteur à Effet de Champ (MOSFET), qui tirent parti de la large bande interdite du diamant pour concevoir une architecture originale de dispositif basée sur un régime stable d'appauvrissement profond. L'optimisation de ces dispositifs sera établie en fonction des modèles physiques à l'état de l'art, puis des dispositifs de test expérimentaux seront analysés pour mieux comprendre la physique du MOSFET sur diamant. Enfin, une évaluation des performances par rapport à d'autres semi-conducteurs et aux dispositifs en diamant existants sera présentée. Plusieurs perspectives de ces performances ainsi que d'architectures originales spécifiques au diamant seront présentées.